A Very Wideband Operational Transconductance Amplifier and Capacitor (OTA-C) Filter in CMOS VLSI Technology

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ABSTRACT

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Rong Ding Li

Wideband analog signal processing systems are useful in many applications, such as telecommunication, multimedia and consumer electronics. An analog filter is an important subsystem in such systems. Among the existing realization methods of continuous-time domain integrated analog filter, OTA-C topology is the most useful one, and it offers good performances with lower power consumption and high frequency operation.

In this work, several existing OTA cells selected from literature are studied. Based on the comparison of g_m value, bandwidth, output resistance, and dynamic range in terms of DC power dissipation and substrate area requirement, an optimum OTA cell is selected for the implementation of wideband OTA-C filter.

Using selected OTA cell as the basic building block, a fully differential highly linear, very wideband sixth-order filter is designed using 0.18 μm CMOS technological process. Three identical biquads are connected using PRB (Primary Resonator Block) technique to realized a sixth order bandpass filter that has a passband from 2 MHz to 400 MHz. Simulation results show that the filter consumes 80.70 mW of power with supply voltages of ±1.5 V. The dynamic range for 1% THD with 0.42 V (peak-to-peak) at 100 MHz is close to 40 dB and the third order intermodulation intercept (IIP_3) is -27.29 dBW (i.e. 2.71 dBm).

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List of Symbols and Abbreviations

C	Capacitor
I	Current
L	Channel Length of a MOS Transistor
Q	Quality Factor
R	Resistor
S	Sensitivity
μ	Mobility of Carrier
V	Voltage
W	Channel Width of a MOS Transistor
ω	Frequency in Radians
g_m	AC Transconductance
H(s)	Transfer Function
T(S)	Transfer Function
V_{th}	Threshold Voltage of a MOS Transistor
BP	Bandpass
BR	Bandreject
BW	Bandwidth
dB	Decibel
HP	Highpass
IC	Integrated Circuit
IM	Intermodulation Product
LC	Inductor and Capacitor
LF	Leapfrog
LP	Lowpass
PB	Passband
SB	Stopband

SB_H	Upper Stopband
SB_L	Lower Stopband
TB	Transition Band
DIP	Dual In-line Package
FLF	Follow-the-leader Feedback
GIC	Generalized Immittance Converter
HIC	Hybrid Integrated Circuit
LCR	Inductor, Capacitor and Resistor
MOS	Metal Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PBH	Upper Frequency Passband
PBL	Lower Frequency Passband
PRB	Primary Resonator Block
THD	Total Harmonic Distortions
VCT	Voltage to Current Transducer
VDD	Positive Supply Voltage
VSS	Negative Supply Voltage
IIP_3	Third Order Input Intercept Point
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
VCVS	Voltage Controlled Voltage Source
VLSI	Very Large Scale Integration
OP-AMP	Operational Amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

Chapter 1

Introduction

1.1 Motivation

Analog filters are electrical networks which consist of an interconnection of components, such as resistors, capacitors, inductors and active devices (transistors, amplifiers, controlled sources, etc.). Analog filters process signals with a frequency selectivity. The signals of certain frequencies are transmitted through the filters with zero (or very little) attenuation while signals at other frequencies are passed with larger (ideally infinite) attenuation.

Analog filters are important signal-processing subsystems and have a wide range of applications. Almost every analog signal-processing system consists of one or more analog filters, even signal-processing systems that appear to be entirely digital often contain one or more analog filters internally or as interface with the analog world [1].

With the arrival of VLSI (very large-scale integration), the designer of analog filters has many powerful incentives for trying to develop the filter circuitry in a form that is compatible with appropriate integrated circuit (IC) technology (MOS or bipolar). In recent years, considerable effort is being devoted to the design of filter circuits which consist only of components that are conveniently realizable on an IC chip.

Integrated analog filters can be realized using two different approaches: discrete-time and continuous-time implementations. The discrete-time filters are limited to low frequency applications due to the sampling process. Performances of integrated continuous-time filter have always been limited by employed circuits and design techniques. Active-RC and MOSFET-C filters use Operational Amplifiers (OP-AMP), capacitors, and resistors (or MOSFET resistances). They are limited to relatively low frequency applications because of the limitation of OP-AMP bandwidth. Operational Transconductance Amplifier (OTA) cells are extensively used to design continuous-time filters, since they offer good performance with low power consumption and high frequency operation [1].

Wideband analog signal processing system can be used in many applications, such as telecommunication, multimedia and consumer electronics [2]. An electronics filter is an important subsystem in such systems. For example, wideband high frequency integrated bandpass filters are an important building block for the implementation of integrated front-end receivers for emerging new generation of communication systems.

OTA-C filter has better frequency response, electronic tuning capability, and is easy to be implemented in monolithic environment. It has received considered attention in recent years. There are lots of reports in literature on the realizations of high frequency,

turnable analog filters using OTA-C topology, such as [3] [4] [5] [6]. But filters like wide band vestigial side band, have not been reported yet. This project is to study existing OTA cells and come up with an optimum OTA cell and then use it for the implementation of high frequency, very wideband OTA-C filter.

1.2 Research Goals

The primary aim of this project is to design a low voltage, fully differential, very wideband and highly linear OTA-C filter in modern CMOS technology. The filter specifications are assumed as: sixth order Chebyshev bandpass filter with 1 dB passband ripple and the bandwidth is from 2 MHz to 400 MHz.

The achievements of this project are summarized below:

• Designed of a fully differential wideband OTA-C filter which fulfills the specification. The filter was implemented using 0.18 μm CMOS technological process. Simulation results showed that the filter consumed 80.70 mW of power with supply voltages of ±1.5 V. The dynamic range for 1% THD with 0.42 V (peak-to-peak) at 100 MHz was close to 40 dB and the third order intermodulation intercept (IIP_3) was -27.29 dBW (i.e., 2.71 dBm).

• Studied of different existing high order filter architecture. Analysis of the advantages and disadvantages of these approaches lead to the selection of the filter architecture for in the work.

• Studied and compared of various OTA cells reported in the literature. Based on the comparison criteria of performance v.s. cost, the optimum cell had been selected to implement in the filter.

• Established the possibility of realization high frequency, wideband continuous-time filter in monolithic environment.

1.3 Thesis Organization

Following this chapter, Chapter 2 provides a brief overview of filter fundamentals. Various aspects regarding the filter mathematical model, filter types, filter development history and realization methods are introduced in this chapter.

Chapter 3 deals with the high order (i.e., order greater than two) filter architecture selection. The main advantages and disadvantages of three existing high order filter architectures - the cascade, the multiple-loop feedback, and the ladder simulation are discussed. The trade-off between filter sensitivity performance and hardware realization complexity of different high order filter architecture leads to the selection of filter architecture in this work.

In continuous-time domain, integrated analog filters can normally be realized in three topologies: Active-RC filter, MOSFET-C filter, and OTA-C filter. For filters operating in high frequency, the OTA-C topology is the best choice since OTA cells offer good performances with low power consumption and high frequency operation. In Chapter 4,

several existing OTA cells selected in the literature are studied. Based on the comparison of the g_m value, bandwidth, output resistance and dynamic range in terms of DC power dissipation and substrate area requirement for these selected OTA cells, an optimum OTA cell was selected to implement the wideband filter.

According to the filter specification we assumed, Chapter 5 gives the detail aspects of the fully differential, wideband filter design. Starting from the synthesis of the filter, the design methods and techniques of biquad filter section and high-order filter built by biquad sections are illustrated, as well as the layout techniques in order to minimize the side effects of transistor pair mismatch and parasitic.

The measurement results of a fabricated chip that consists of 4 different structured OTA cells and the simulation results of the designed sixth order fully differential wide-band filter are presented in Chapter 6.

Conclusions drawn from this work are given in Chapter 7.

Chapter 2

Filter Fundamentals

2.1 Introduction

This chapter gives brief review on the filter fundamentals, such as filter mathematical model, types of various filters, filter history and various realization methods.

2.2 Filter Mathematical Model

Filters as linear systems can be easily analyzed and synthesized with network transfer functions in frequency domain. In continuous-time domain, Laplace transform technique can be used to model the transfer functions, while in discrete-time domain, Z transform technique is applied. Referring to Figure 2.1, the schematic representation of a

filter system, in continuous-time domain, the filter transfer function can be defined in terms of Laplace-transformed excitation *X(s)* and the zero-state response *Y(s)*:

$$H(s) = \frac{L[y(t)]}{L[x(t)]} = \frac{Y(s)}{X(s)}$$

$$= \frac{a_m s^m + a_{m-1} s^{m-1} + \ldots + a_0}{b_n s^n + b_{n-1} s^{n-1} + \ldots + b_0} = \frac{N(s)}{D(s)} \tag{2.1}$$

where $m \leq n$ for any realizable practical network and N and D are the numerator and denominator polynomials, respectively, and n is the order of the filter.

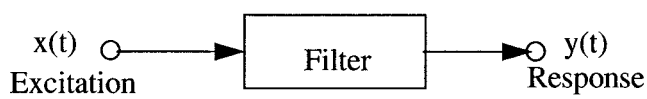


Figure 2.1 Schematic representation of a filter system

In normal case for filters, *Y(s)* and *X(s)* in Eq. (2.1) are voltage transforms [i.e. $V_{out}(s)$ and $V_{in}(s)$, respectively], $H(s) = V_{out}/V_{in}$ is referred to as the voltage transfer function. In other situation, however current transfer function [$Y(s) = I_{out}(s)$, $X(s) = I_{in}(s)$] is also encountered.

If the numerator and denominator polynomials of Eq. (2.1) are factored, H(s) can be written in the following alternative representation

$$H(s) = \frac{N(s)}{D(s)} = \frac{a_m(s-z_1)(s-z_2)\ldots(s-z_m)}{b_n(s-p_1)(s-p_2)\ldots(s-p_n)} \tag{2.2}$$

In Eq. (2.2), z_1, z_2,..., z_m are referred to as the zeros of H(s) and p_1, p_2,..., p_n are referred as the poles of H(s).

Under steady-state conditions, the transfer function of Eq. (2.1) can be written as

$$H(s) = H(j\omega) = |H(j\omega)|e^{j\phi(\omega)} \tag{2.3}$$

where $|H(j\omega)|$ is the magnitude response and $\phi(\omega)$ is the phase response of the filter. Normally, the filter magnitude response requirements are specified as gain in decibels [dB] which is defined as

$$G(\omega) = 20\log|H(j\omega)| \qquad [dB] \tag{2.4}$$

while $\phi(\omega)$, in radians, is the phase response of the filter. Sometimes it is prescribed via the group delay $\tau(\omega)$, defined as

$$\tau(\omega) = -\frac{d\phi(\omega)}{d\omega} \tag{2.5}$$

$\tau(\omega)$ represents the delay experienced by a component of frequency ω of the input spectrum.

Normally, filter magnitude characteristics are specified by four basic parameters, (a) the maximum loss in the passband, A_p [dB], (b) the passband edge frequency ω_c [rad/s], (c) the attenuation in the stopband, A_a [dB], and (d) the stopband edge frequency ω_a where the attenuation is at least A_a [dB].

The order of denominator of a filter transfer function is called the order of the filter. The filter order decides the frequency selectivity of the filter. Under the same magnitude approximation method, a higher order means a high frequency selectivity.

2.3 Filter Types

Filters are typically categorized according to the filtering function performed. If magnitude (gain, attenuation) requirements are of primary importance, the filters are classified as lowpass, highpass, bandpass, or bandreject networks. In some applications, one is mainly concerned with phase or delay specifications with no change in magnitude, the filters typically will be either allpass networks or delay equalizers.

2.3.1 Lowpass Filter

The function of the lowpass (LP) filter is to pass low frequencies from dc to some desired cutoff frequency and to attenuate high frequencies. The filter is specified by its cutoff frequency ω_c, stopband (SB) frequency ω_s, dc gain, passband (PB) loss, and stopband attenuation. The filter passband is defined as the frequency range $0 \le \omega \le \omega_c$, the stopband as the frequency range $\omega \ge \omega_s$, and the transition band (TB) as the frequency range $\omega_c < \omega < \omega_s$. These specifications are shown graphically in Figure 2.2.

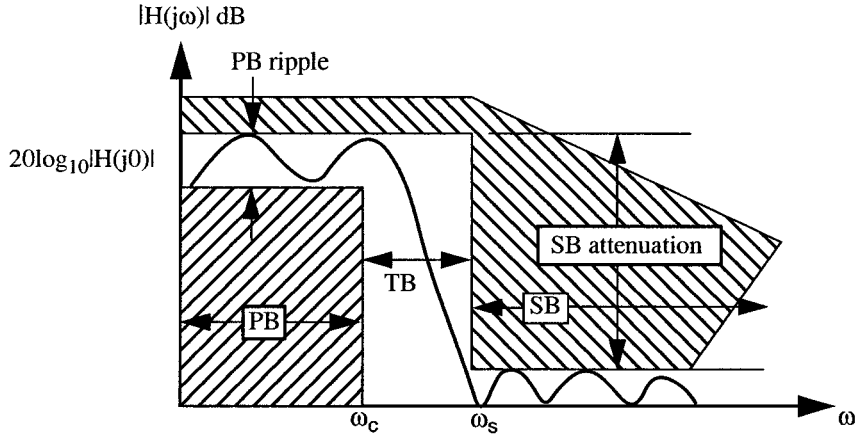


Figure 2.2 Lowpass filter characteristic

2.3.2 Highpass Filter

The function of the highpass (HP) filer is to pass high frequencies above some specified cutoff frequency ω_c, and to attenuate low frequencies from dc to some specified stopband frequency ω_s. Figure 2.3 shows the highpass filter characteristic.

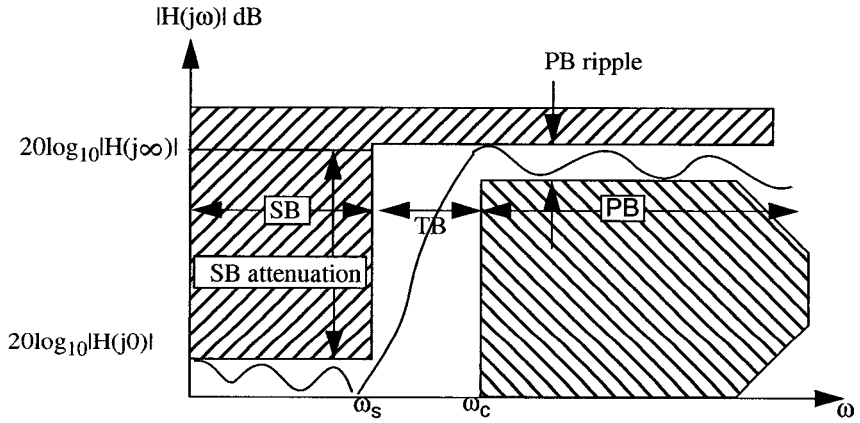


Figure 2.3 Highpass filter characteristic

2.3.3 Bandpass Filter

The function of the bandpass (BP) filter is to pass a finite band of frequencies while attenuate both lower and high frequencies. The filter has both a lower stopband, SB_L, and an upper stopband, SB_H as illustrated in Figure 2.4.

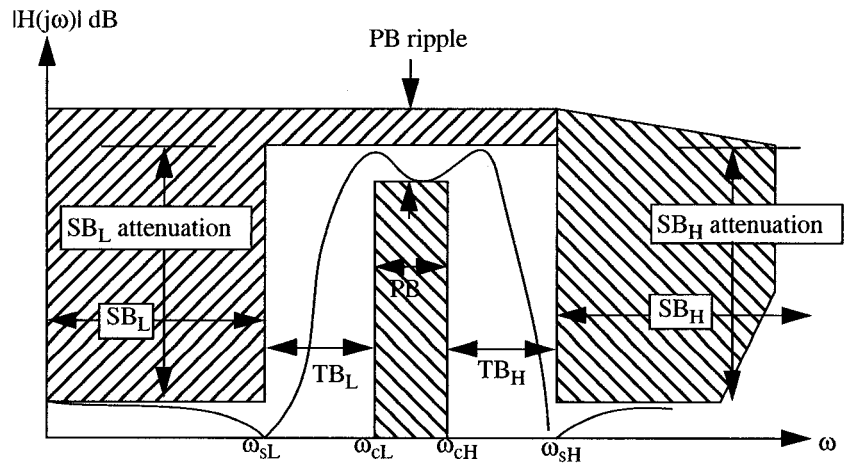


Figure 2.4 Bandpass filter characteristic

2.3.4 Bandreject Filter

The function of the bandreject (BR) filter is to attenuate a finite band of frequencies while passing both lower and higher frequencies. As a result, this filter has both lower- and upper-frequency passband, PBL and PBH. The characteristic is illustrated in Figure 2.5. In reality the upper passband is limited due to the band-limited active devices and parasitic.

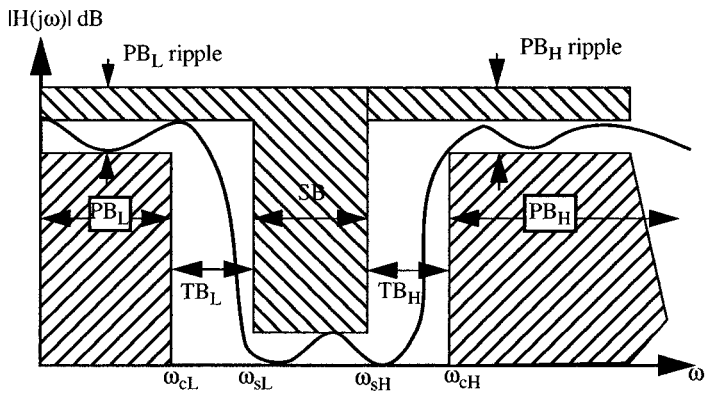


Figure 2.5 Bandreject filter characteristic

2.4 Filter History and Realization

Typically in the 1920s filters were used as impedance matching networks between a given pair of source and load impedances to facilitate transfer of maximum power in a desired band of frequencies. From 1920 to the latter 1960s the majority of filters were realized as discrete LCR networks. However, in the 1960s the size and cost reductions were achieved by replacing the larger, costly inductors with active networks, which were referred to as active RC networks. For high frequency applications (higher than 30 KHz), the LCR filters remained popular while some other devices (such as crystal filters, surface acoustic wave devices) were invented to bring in high selectivity and miniaturization. In the early 1970s, the economic potential envisioned for active RC filters began to be achievable with batch-processed thin-film hybrid integrated circuits (HICs). The HIC composed of capacitors, thin-film resistors and silicon integrated-circuit operational

amplifiers. While filters were used to process continuous analog signals, digital technology opened the avenue of filtering using sampling, encoding and logical mathematical operations (add, multiply, delay). In the 1980s switched capacitor technique was invented to effect filtering of analog signals using capacitance, OP-AMPs, switches and capacitors. The switching mechanism brought in the phenomenon of sampling in analog filtering.

Nowadays, there are two trends of the types of signal processing, i.e. (1) Continuous-time domain, which encompasses the classical LCR to modern active RC, OTA, Current Conveyor and Transconductor based implementations, and (2) Discrete-time domain, which comprises the digital, switched capacitor and switched current implementations. Figure 2.6 show the technology base of filter realization [7].

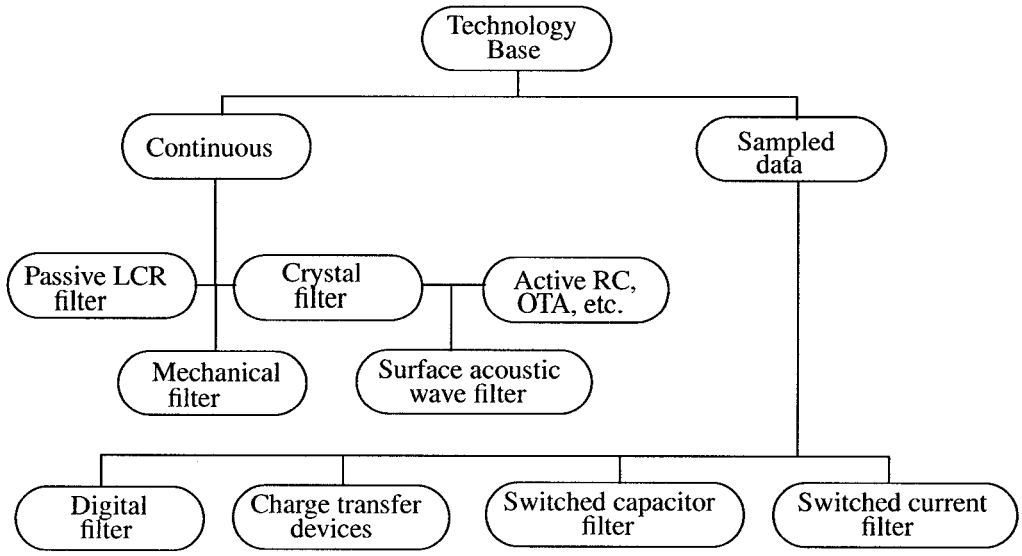


Figure 2.6 Realization of filters in technology viewpoint

2.5 Summary

Analog filters are modeled with network transfer functions using Laplace transform technique mathematically. The magnitude characteristics of an analog filter are specified by four basic parameters, (a) the maximum loss in the passband, A_p, (b) the passband edge frequency ω_c, (c) the attenuation in the stopband, A_a, and (d) the stopband edge frequency ω_a where the attenuation is at least A_a.

Typically, filters are categorized according to the filtering function performed. If magnitude requirements are of primary importance, the filters are classified as lowpass, highpass, bandpass, or bandreject networks. In some applications, one is mainly concerned with phase or delay specifications with no change in magnitude, the filters typically will be either allpass networks or delay equalizers.

In modern IC technology, analog filters can be realized both in discrete-time domain and continuous-time domain. In discrete-time domain, the main topologies are switched capacitor and switched current, while in continuous-time domain, active RC filter, MOSFET-C filter and OTA-C filter are the main methods.

Chapter 3

Filter Architecture

3.1 Introduction

There are mainly three methods to realize high order analog filters, namely the cascade approach, the multiple-loop feedback or coupled-biquad approach, and the ladder simulation approach.

For both cascade and multiple-loop feedback techniques, high order filters are realized by constructing first and second-order filter sub-networks. The ladder simulation technique attempts to find active realization methods that inherit the recognized excellent low-sensitivity properties of passive doubly terminated LC ladder filters.

This chapter gives brief introduction of three existing high order analog filter realization approaches, as well as the main advantages and disadvantages of the three methods. The trade-off between filter sensitivity performance and hardware realization

complexity of different high order filter architecture leads to the selection of filter architecture in this work.

3.2 Sensitivity

Analog filters are realized by interconnecting electrical components. These components may deviate from their nominal design values due to fabrication tolerances, environmental effects such as temperature and humidity variations, and chemical changes that occur during the circuit life. Consequently, the filters performances will deviate from the desired design values. Presumably, these deviations may differ due to different filter architecture adopted. Sensitivity is one of the most important criteria for comparing different filter architecture.

Given a component x, then in general any performance criterion P, such as the quality factor, a pole or zero frequency, or the magnitude response, will depend on x; suchthat, P = P(x). The sensitivity is defined as the deviation in P caused by any error Δx, as expressed as [1]

$$S_x^{\ P} = \frac{dP/P}{dx/x} = \frac{d(\ln P)}{d(\ln x)} \tag{3.1}$$

The Eq. (3.1) indicates that the relative change of a performance measure P, is S_x^P times as large as the relative change of the circuit parameter x on which P depends.

Thus

$$\frac{\Delta P}{P} = S_x^P\left(\frac{\Delta x}{x}\right) \tag{3.2}$$

Therefore, good circuits should have low sensitivities to variation of their components.

The deviation in performance P caused by tolerance of one single component x is measured by single-parameter sensitivity. In reality, a filter consists of many components which will all contribute to the performance P variation. This is studied by multiparameter sensitivity[8]. In this article, we will only use the single-parameter sensitivity to compare the advantages and disadvantages of different high order filer architecture.

3.3 Cascade Realizations

The voltage transfer functions of a high order filter can be expressed as

$$H(s) = \frac{V_o}{V_i} = \frac{N(s)}{D(s)} = \frac{a_m s^m + a_{m-1}s^{m-1} + \ldots + a_1 s + a_0}{s^n + b_{n-1}s^{n-1} + \ldots\ldots + b_1 s + b_0} \tag{3.3}$$

with $n \geq m$ and $n > 2$. We may assume that both n and m are even, so that both numerator and denominator polynomials, N(s) and D(s), can be factored into the product of second-order pole-zero pairs. In case of that N(s) and D(s) are odd functions, they can always be factored into the product of even functions and a first-order function.

Therefore, Eq. (3.3) can be rewritten as the product of second order functions

$$H_k(s) = \frac{a_{2k}s^2 + a_{1k}s + a_{ok}}{s^2 + s(\omega_{pk}/Q_{pk}) + \omega_{pk}^2} \tag{3.4}$$

such that

$$H(s) = \prod_{k=1}^{n/2} H_k(s) = \prod_{k=1}^{n/2} \frac{a_{2k}s^2 + a_{1k}s + a_{ok}}{s^2 + s(\omega_{pk}/Q_{pk}) + \omega_{pk}^2} \tag{3.5}$$

The transfer functions of the individual biquads are labeled $H_k(s)$.

If it is assumed that the output impedances of the biquads are sufficiently small (compared to the input impedances), each second-order block will produce a voltage transfer function of order 2. Several second-order blocks can be connected in cascade to realize a high order voltage mode filter as illustrated in Figure 3.1.

Therefore, the overall transfer function can be expressed as

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{V_{o1}}{Vin}\frac{V_{o2}}{V_{o1}}\cdots\frac{V_{n/2-1}}{V_{n/2-2}}\frac{V_{out}}{V_{n/2-1}}$$

$$= H_1 H_2 \ldots H_{n/2-1} H_{n/2} \tag{3.6}$$

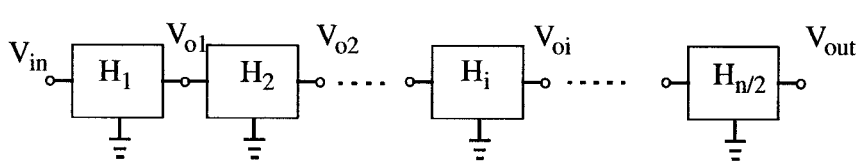


Figure 3.1 Cascade realization of nth-order transfer function

We assume that the component x exists in biquadratic section H_j only. Since the n/2 biquad sections have no interaction with each other, the performance impact on H(s) cased by the variations Δx can be derived as [1]

$$S_x^{H(s)} = S_{H_j(s)}^{H(s)} S_x^{H_j(s)} = S_x^{H_j(s)} \tag{3.7}$$

Eq. (3.7) indicates that in cascade connection the sensitivity of the high order transfer function to the element x and its variations in relation to x are as large as those of the second order building block which contains the element.

3.4 The Multiple-loop Feedback Realization

The Multiple-loop feedback topologies are also based on biquad building blocks which are embedded into a resistive feedback configuration. The resulting coupling between sections is selected such that transfer function sensitivities are reduced. Quite a number of such topologies have been found useful in practices. Figures 3.2(a) - (b) show typical examples of follow-the-leader feedback (FLF) [9] and leapfrog (LF) configurations respectively.

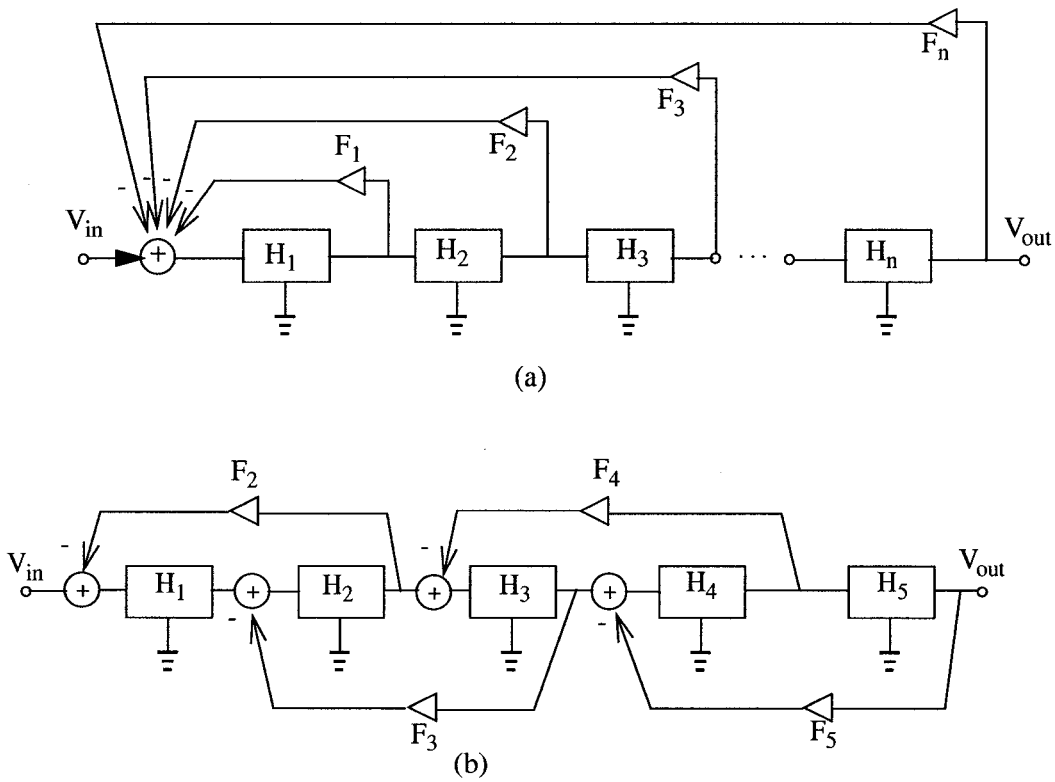


Figure 3.2 (a) Follow-the-leader feedback (b) leapfrog topologies of high order active filters.

The associated transfer functions are:

For figure 3.2(a)

$$H_{FLF}(s) = \frac{V_{out}}{V_{in}} = \frac{\prod_{i=1}^{n} H_i(s)}{1 + \sum_{k=1}^{n} F_k \prod_{j=1}^{k} H_j(s)} \tag{3.8}$$

and, for figure 3.2(b)

$$H_{LF}(s) = \frac{\prod_{j=1}^{5} H_j(s)}{1 + F_2H_1H_2 + F_3H_2H_3 + F_4H_3H_4 + F_5H_4H_5 + F_2F_4H_1H_2H_3H_4 + F_2F_5H_1H_2H_4H_5 + F_3F_5H_2H_3H_4H_5} \tag{3.9}$$

Obviously, in multiple-loop feedback filters, the transfer function H(s) is not simple product of the sections $H_k(s)$, but rather a more general function

$$H(s) = f(H_k(s)) \qquad k = 1, 2, \ldots, n \tag{3.10}$$

So that the sensitivity of H(s) to an component x in section j becomes,

$$S_x^{H(s)} = S_{H_j(s)}^{H(s)} S_x^{H_j(s)} \tag{3.11}$$

If the function f{} of Eq. (3.10) is selected such that $\left|S_{H_j(s)}^{H(s)}\right| < 1$ in the frequency range of interest, the overall sensitivity will be $S_x^{H(s)} = S_{H_j(s)}^{H(s)} S_x^{H_j(s)} < S_x^{H_j(s)}$, which means that the sensitivities of multiple-loop feedback filters can be made smaller than those of the cascade filters.

3.5 The Ladder Simulation Realization

Ladder simulation can be classified into two groups: operational simulation and element substitution. Both methods start from an existing LC prototype ladder. Figure 3.3 shows an example of LC ladder filter, a lossless transmission network N consisting of only inductors and capacitors is embedded between a source (V_s, R_s) and a resistive load (R_L).

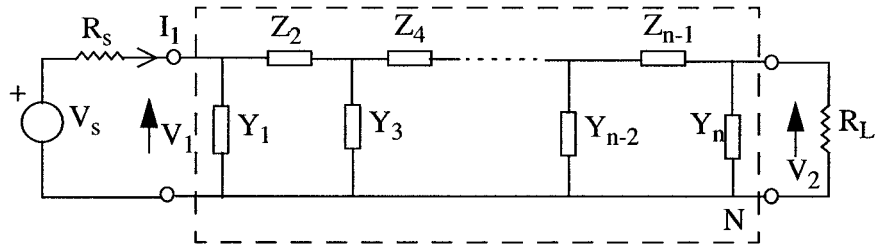


Figure 3.3 Resistively terminated ladder structure

Let us study the H(s) deviation caused by the tolerances of one components x in the network N.

We can write the transfer function is this way:

$$H(j\omega, x) = \exp[-\alpha(\omega, x) + j\phi(\omega, x)] \tag{3.12}$$

From Eq. (3.12) we can calculate the attenuation α,

$$\alpha(\omega, x) = -\ln|H(j\omega, x)| \tag{3.13}$$

If the circuit parameter x varies, the attenuation sensitivity is obtained as:

$$x\frac{\partial\alpha}{\partial x} = -\frac{x}{|H(j\omega, x)|}\frac{\partial|H(j\omega, x)|}{\partial x} = -S_x^{|H(j\omega, x)|} = -ReS_x^{H(j\omega, x)} \tag{3.14}$$

For the passive lossless network N designed for maximum power transfer, we have $|H(j\omega, x)| \leq 1$ with $|H(j\omega, x)| = 1$ for $x = x_{nominal}$ at the reflection zeros ω_{ri}. Consequently, $\alpha(\omega, x) = 0$ at these points of perfect transmission, and for a change in

frequency or in any component, the attenuation α of the passive network can only increase.

When x_i represents any inductors and capacitors inside the lossless network N, we have [10],

$$\left| x_i \frac{\partial \alpha}{\partial x_i} \right| \leq \frac{\omega \varepsilon_i}{P_L} \sqrt{1 - e^{-2\alpha}} \tag{3.15}$$

Where ε_i is the average energy stored in the component x_i, and P_L is the power transmitted to the load R_L.

Therefore, for passive lossless filters designed for maximum power transfer the magnitude sensitivity $S_x^{|H(j\omega, x)|}$ to any component x is zero in the passband at all the reflection zeros ω_{ri}, and $(\partial\alpha)/(\partial x_i)$ remains small everywhere else in the passband [10].

3.5.1 Operational Simulation Method

Operational simulation attempts to represent the internal operation of the ladder by simulating the equations describing the circuit's performance, i.e., Kirchhoff's voltage and current laws and the I-V relationships of the ladder arms. Fundamentally, this procedure is based on simulating the signal-flow graph of the ladder where all voltages and all currents are considered as signals which propagate through the circuit.

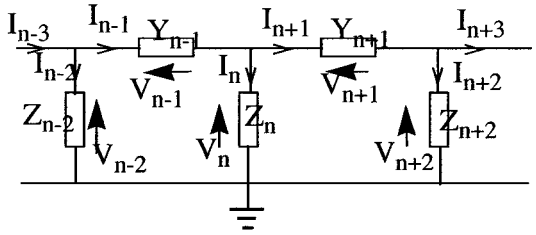


Figure 3.4 A section of a ladder network

Figure 3.4 shows a section of a ladder network. The I-V relationships for the ladder arms are as follows:

.....

$$V_{n-1} = V_{n-2} - V_n \qquad I_{n-1} = Y_{n-1}V_{n-1} = Y_{n-1}(V_{n-2} - V_n) \tag{3.16a}$$

$$I_n = I_{n-1} - I_{n+1} \qquad V_n = Z_n I_n = Z_n(I_{n-1} - I_{n+1}) \tag{3.16b}$$

$$V_{n+1} = V_n - V_{n+2} \qquad I_{n+1} = Y_{n+1}V_{n+1} = Y_{n+1}(V_n - V_{n+2}) \tag{3.16c}$$

.....

In the active simulation of this circuit, all currents and voltages are to be represented as voltage signals, which can be achieved by using a resistive scaling factor R. As an example, Eq. (3.16b) is scaled as

$$I_n R = I_{n-1}R - I_{n+1}R \qquad V_n = \frac{Z_n}{R} I_n R = \frac{Z_n}{R}(I_{n-1}R - I_{n+1}R) \tag{3.17}$$

With the introduction of the notation

$$I_k R = i_k \qquad V_k = v_k \qquad \frac{Z_k}{R} = z_k \qquad Y_k R = y_k,$$

Eq. (3.16) can be expressed as:

.....

$$v_{n-1} = v_{n-2} - v_n \qquad i_{n-1} = y_{n-1}v_{n-1} = y_{n-1}(v_{n-2} - v_n) \tag{3.18a}$$

$$i_n = i_{n-1} - i_{n+1} \qquad v_n = z_n i_n = z_n(i_{n-1} - i_{n+1}) \tag{3.18b}$$

$$v_{n+1} = v_n - v_{n+2} \qquad i_{n+1} = y_{n+1}v_{n+1} = y_{n+1}(v_n - v_{n+2}) \tag{3.18c}$$

.....

Eq. (3.18) indicate that to realize operational simulation of LC ladder filter, one needs to build voltage summation to implement Kirchhoff's laws and to realize the frequency dependent multipliers z_k or y_k. These are all available with modern technology.

3.5.2 Element Substitution Method

For a LC ladder filter, one could have either a grounded or a floating inductor. The element substitution procedure replaces all inductors by an active network whose input impedance over the appropriate frequency ranges inductive, such as gyrators or generalized immittance converters (GIC).

Gyrators or positive impedance inverters are special networks realized with transconductance building blocks. The input impedance in a gyrator is $Z_{in} = \frac{1}{K_1 K_2 Z_L}$, so that if $Z_L = \frac{1}{sC_L}$, terminating the gyrator with a capacitive load will result in

$Z_{in} = \frac{sC_L}{K_1 K_2}$, which represents an inductance. Figure 3.5 shows the grounded and the floating inductor realized by gyrators. g_1, g_2 in Figure 3.5(a) are OTAs.

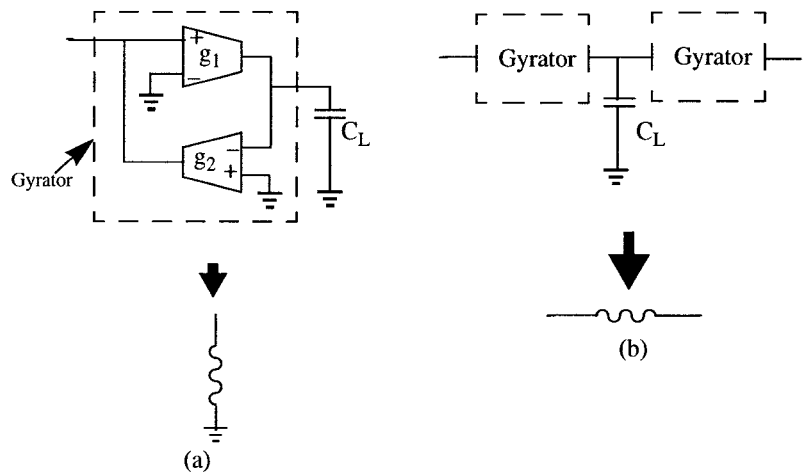


Figure 3.5 Gyrators simulation of (a) grounded inductor (b) floating inductor

GIC's are widely used for realizing inductors. A very versatile architecture was introduced by A. Antoniou and is known as Antoniou's GIC which is shown below

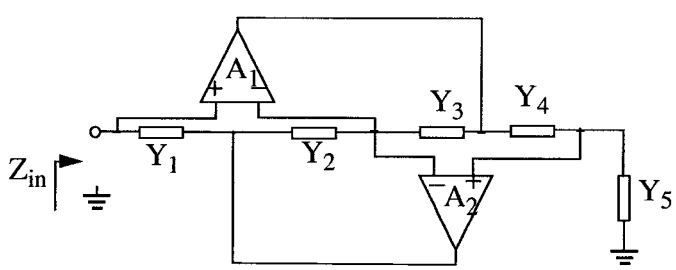


Figure 3.6 Antoniou's GIC for inductor simulation

In Figure 3.6, A_1 and A_2 are OP-AMPs. Nodal analysis yields $Z_{in} = \frac{Y_2 Y_4}{Y_1 Y_3 Y_5}$. If we set $Y_2 = sC, Y_1 = Y_3 = Y_4 = Y_5 = 1/R$, one finds $Z_{in} = sCR^2$, so $L = CR^2$ is the equivalent realized inductance. If Y_2 and Y_4 are interchanged, the circuit in figure 3.6 also simulates an inductor.

Another method of element substitution simulation involves impedance scaling by a frequency dependent function, f(s) = ks. Thus inductors L become $\frac{L}{f(s)} \rightarrow resistors$, resistors R become $\frac{R}{f(s)} \rightarrow capacitors$ while capacitors C become $\frac{C}{f(s)} = \frac{1}{sC^2} = -\frac{1}{\omega^2 C}$, a negative reactance which can be realized using GIC.

3.6 Performance Comparison of the Three Different Architecture

The cascade method is used widely in industry because it is very easy to implement, and efficient in its use of active devices. It uses a modular approach and results in filters that show satisfactory performance in practice. The main advantages of cascade filters is that they are very easy to tune because each biquad is responsible for the realization of only one pole pair (and zero pair), the realizations of the individual critical frequencies of the filter are decoupled from each other. The main disadvantage of this decoupling is

that for the filters of high order with stringent requirements and tight tolerances, cascade designs are often found to be too sensitive to component variations in the passband.

Compared with the cascade approach, the multiple-loop feedback approach shows superior sensitivity performance in high order filter realization due to the nature of coupling between biquad sections. The main disadvantage is that multiple-loop feedback is normally quite complicated to synthesize.

Active filters simulating the behavior of LC ladders have been found to have the lowest sensitivities and consequently to be the most appropriate for filters with stringent requirement. The main disadvantage of this design method is that a passive LC prototype must exist before an active simulation can be attempted. Also, usually a relatively large number of active devices are required for this approach.

In summary, among high order active filter realizations, those that simulate the behavior of LC ladders have been found to have the lowest sensitivity to component variations. Cascade realizations often have transfer function variabilities that are quite unacceptable in practice, while the multiple-loop feedback method is in between for the sensitivity performance. On the other hand, the ladder simulation filters consume maximum active devices among the three methods. The Cascade realized filters take minimum active devices while the multiple-loop feedback realized filters are also in between. To trade-off between sensitivity performance and hardware area consumption, the multiple-loop feedback approach is selected for this work.

3.7 The Primary Resonator Block Technique

Referring to Figure 3.7, which is a typical case of FLF topology, we assume that there are n noninteracting second-order sections so that the order of the realized transfer function H(s) is 2n. Assuming further that the two summation OP-AMPs are ideal, simple analysis yields

$$-V_o = \frac{R_{Fo}}{R_{in}} V_{in} + \sum_{i=1}^{n} \frac{R_{Fo}}{R_{Fi}} V_i = \alpha V_{in} + \sum_{i=1}^{n} F_i V_i \tag{3.19}$$

where we define α and the feedback factors F_i as

$$\alpha = \frac{R_{Fo}}{R_{in}} \text{ and } F_i = \frac{R_{Fo}}{R_{Fi}} \tag{3.20}$$

respectively. Similarly, the output summation

$$V_{out} = -\sum_{i=0}^{n} K_i V_i = -\sum_{i=0}^{n} \frac{R_A}{R_{oi}} V_i \tag{3.21}$$

where the definition of the resistor ratios K_i is apparent. Finally, the internal voltages V_i can be computed from

$$V_i = V_o \prod_{j=1}^{i} H_j(s) \qquad i = 1, \ldots, n \tag{3.22}$$

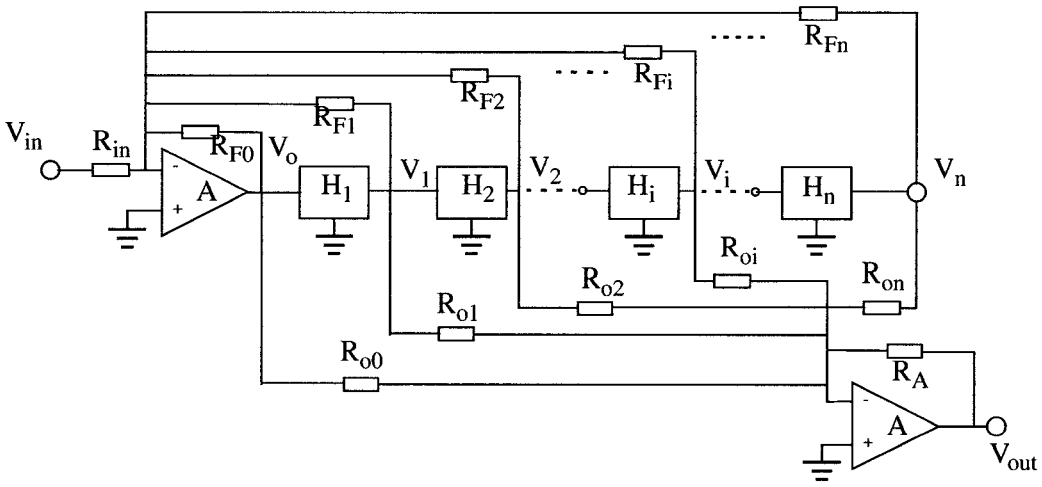


Figure 3.7 FLF circuit built from second-order section $T_i(s)$ and a feedback network consisting of OP-AMP summation and resistors R_{Fi}

With Eq. (3.19), we have

$$H_o(s) = \frac{V_o}{V_{in}} = -\frac{\alpha}{1 + \sum_{k=1}^{n}\left[F_k \prod_{j=1}^{k} H_j(s)\right]} \tag{3.23}$$

and with Eq. (3.22), yields

$$H_n(s) = \frac{V_n}{V_{in}} = -\frac{\alpha \prod_{j=1}^{n} H_j(s)}{1 + \sum_{k=1}^{n}\left[F_k \prod_{j=1}^{k} H_j(s)\right]} \tag{3.24}$$

Eq. (3.24) is the transfer function of the FLF network without the output summation.

When all the biquads are identical, the analysis and synthesis of the FLF filter are considerably simplified. The resulting system is known as Primary Resonator Block (PRB) [11]. Figure 3.8 shows the general structure of high order active filter using PRB technique.

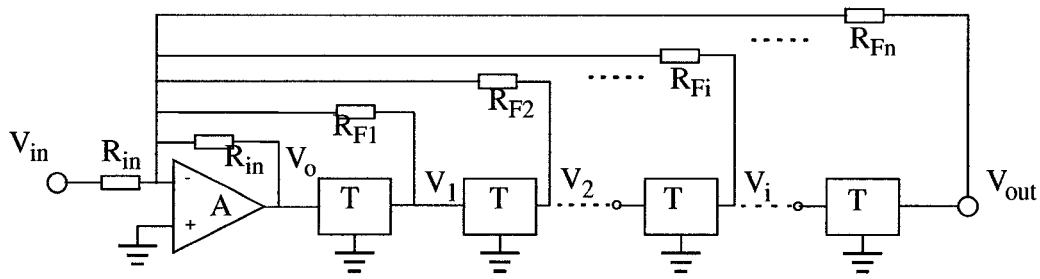


Figure 3.8 General structure of PRB high order filter

The overall voltage transfer function is given by:

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{\alpha T^n(s)}{1 + \sum_{k=1}^{n} [F_k T^k(s)]} \tag{3.25}$$

3.8 Single-ended v.s. Differential Structure

Analog filters with IC implementation are usually built in fully balanced differential structure rather than single-ended structure. By doing this, the dynamic range performance of the circuit will benefit in two ways.

Fully balanced differential structure can reduce the effect of common-mode noise caused by other parts of the system on a single IC chip. Normally these parts will often perform digital or sampled-data-signal-processing tasks. And the clock noise may be coupled into the filter circuit either directly or via the substrate, the power supply, or the ground lines. To reduce or further eliminate these problems, differential structure is adopted.

Furthermore, fully balanced differential structure can eliminate even order harmonic distortion signals, therefore improves the dynamic range performance of the filter.

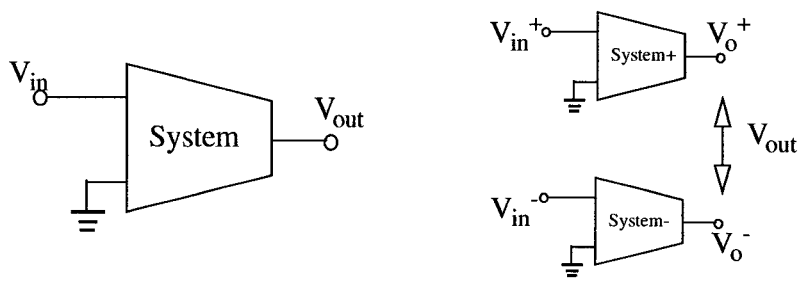


Figure 3.9 Single-ended system v.s. differential system

Refer to Figure 3.9, in general the system output V_{out} with refer to input $V_{in} = v$ can be expressed as;

$$V_{out} = a_1 v + a_2 v^2 + a_3 v^3 + \ldots + a_n v^n \tag{3.26}$$

In Eq. (3.26) $a_2 v^2$, $a_3 v^3$,..., $a_n v^n$ are undesired harmonic distortions.

Now if the system is fully balanced with referenced to ground. And $V_{in}^{+} = \frac{v}{2}$, $V_{in}^{-} = -\frac{v}{2}$, then the output would be:

$$V_o^{+} = a_1\frac{v}{2} + a_2\left(\frac{v}{2}\right)^2 + a_3\left(\frac{v}{2}\right)^3 + \ldots + a_n\left(\frac{v}{2}\right)^n \tag{3.27}$$

$$V_o^{-} = a_1\left(-\frac{v}{2}\right) + a_2\left(-\frac{v}{2}\right)^2 + a_3\left(-\frac{v}{2}\right)^3 + \ldots + a_n\left(-\frac{v}{2}\right)^n \tag{3.28}$$

The overall output is:

$$V_{out} = V_o^{+} - V_o^{-} = a_1 v + \frac{a_3}{4}v^3 + \frac{a_5}{16}v^5 + \ldots \tag{3.29}$$

From Eq. (3.29) one can see that by fully balanced differential arrangement, the even order distortions are eliminated.

3.9 Summary

There are mainly three methods to realize high order analog filters, namely the cascade approach, the multiple-loop feedback, and the ladder simulation approach. The cascade filter is the easiest one to design, but has higher sensitivity to the components variation. The multiple-loop feedback approach gives relatively low sensitivity as compared with the cascade approach. The ladder simulation realized filter has the lowest sensitivity and but needs lots of active devices.

In this project, to trade-off between sensitivity performance and hardware complexity, the multiple-loop feedback topology is adopted as the high order filter architecture. Among the various configurations of multiple-loop feedback filters, the PRB structure simplifies the design work by setting the biquad sections identical.

In IC implemenation, fully balanced differential structure is used to gain good dynamic range performance of the filter by the means of common-mode noise reduction and even order harmonic distortion signals elimination.

Thus, the fully balanced differential PRB structure is adopted to design the filter in this work.

Chapter 4

Selection of the Operational Transconductance Amplifier

4.1 Introduction

There are three main techniques to implement integrated filters in continuous-time domain: active-RC, MOSFET-C, and OTA-C. Active-RC or MOSTFET-C configurations use OP-AMPs, and resistors (or MOSFET resistances) and capacitors as passive frequency-determining components. For design purpose, the assumption that OP-AMP is ideal is generally made, and large amounts of feedback are used to make filter gain essentially independent of the gain of the OP-AMP. However, OP-AMP limitations preclude the use of these filters at high frequencies, and convenient voltage or current control schemes for externally adjusting the filter characteristics do not exist.

The knowledge that BJT and MOSFET are inherently current and transconductance amplifiers, operational transconductance amplifier, as voltage to current transducer

opened up a new era of design easy turnable, high frequency, wideband analog integrated filters.

This chapter starts with a brief introduction of the OTA model. Afterwards, several existing OTA cells reported in the literature are studied and compared with the goal to choose the optimum one for the implementation of the wideband filter. The selection criteria are based on the g_m value, bandwidth, output resistance and dynamic range in terms of DC power dissipation and the substrate area requirements.

4.2 OTA Model

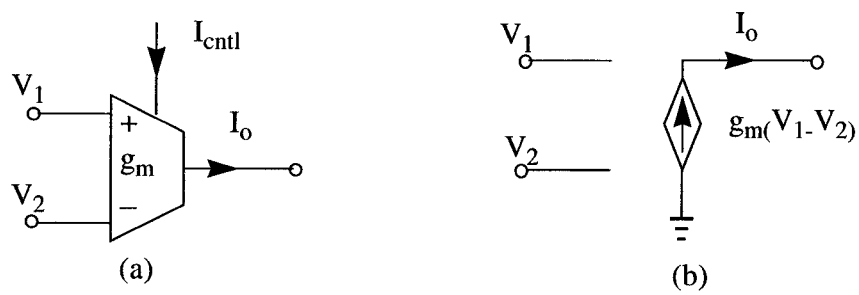


Figure 4.1 Circuit symbol (a) and small-signal equivalent circuit (b) of an OTA

The circuit symbol and the equivalent circuit of an ideal operational transconductance amplifier are shown in Figure 4.1. An ideal OTA is a voltage controlled current source described by

$$I_o = g_m(V_1 - V_2) \tag{4.1}$$

whose input and output impedances are both infinite, as illustrated in the diagram of Figure 4-1b. Normally, the transconductance g_m is variable by setting a control bias current I_{cntl}, such that g_m is proportional to I_{cntl}, or $g_m = kI_{cntl}$.

A more realistic OTA small-signal model is shown in Figure 4.2. Besides the frequency-dependent g_m, the OTA also has finite input and output impedances.

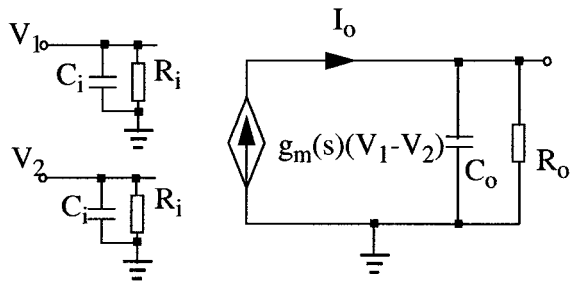


Figure 4.2 OTA model with frequency-dependent g_m and finite input and output impedances. The impedances between the input terminals and coupling between input and output terminals are neglected.

The main characteristics of a practical OTA are: (i) limited linear input voltage range, (ii) finite bandwidth, (iii) finite signal to noise ratio (S/N), and (iv) finite output impedance [12].

4.3 Several Existing OTA Cells

One of the first papers on OTAs in the literature appeared nearly 30 years ago, with a limited linearity performance, only in the order of 30 mV [13]. Since then, OTA, as volt-

age to current transducer (VCT), has received considerable attention due to its usefulness and versatility in many filtering and signal processing application [14]. Many efforts have been put by researchers to improve the OTA performances in term of bandwidth [15], linearity, power dissipation [16], and so on. Since so many varieties of OTAs have been reported in the literature, we decided to study several of these [16], [17] - [22], compare their performances and select the optimum one as the OTA cell to implement the wide-band filter.

4.3.1 Assi's OTA

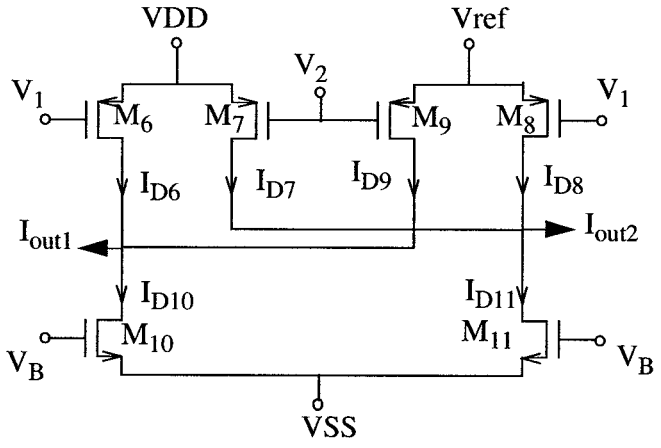


Figure 4.3 Circuit diagram of Assi's OTA

Figure 4.3 show the transconductance circuit proposed by Assi [17]. It uses six CMOS transistors interconnected in a fully differential structure. The circuit has no internal node which is a desirable characteristic for high-frequency operation. The tunability of transconductor is realized by control voltage Vref.

Assuming matching between the geometrically identical PMOS devices M_6-M_9 and between the NMOS devices M_{10}-M_{11} and using the standard square-law model for MOS devices in their saturation region, the currents I_{out1} and I_{out2} are easily derived as

$$I_{out1} = I_{D6} + I_{D9} - I_{D10} \tag{4.2a}$$

$$I_{out2} = I_{D7} + I_{D8} - I_{D11} \tag{4.2b}$$

Thus the differential output current $I_{out} = I_{out1} - I_{out2}$ equals (assuming a differential input voltage $V_1 = V_{in}/2$, $V_2 = -V_{in}/2$, around a common mode voltage $V_{cm} = 0$):

$$I_{out} = -V_{in}[\beta_p(VDD - Vref)] = -V_{in}g_m \tag{4.3}$$

where $\beta_p = \mu_p C_{ox}\frac{W_p}{L_p}$ is the transconductance parameter. μ_p, C_{ox}, W_p and L_p are the mobility, oxide capacitance per unit area, channel width and length respectively. VDD and Vref are the supply voltage and reference voltage respectively, V_1 and V_2 are the input voltages and V_B is a bias voltage for the NMOS transistors. For proper operation, $|VSS| \geq |V_B| - |VSS| > |V_{TN}|$, and $|V_{ref}| \geq |V_{ref}| - |V_1| > |V_{TP}|$, VTN and VTP are threshold voltages for NMOS and PMOS respectively.

Eq. (4.3) reveals the function of the circuit in Figure 4.3 as a linear voltage to current transducer, $I_{out} = -g_m V_{in}$, where $g_m = \beta_p(VDD-Vref)$ is the total transconductance parameter that can be tuned easily by varying Vref.

The AC equivalent model of the transconductance circuit is shown in figure 4.4. The short circuit output current i_{01} and i_{o2} are given by:

$$i_{o1} = v_1(g_6 - sC_{gd6}) + v_2(g_9 - sC_{gd9}) \tag{4.4a}$$

$$i_{o2} = v_1(g_8 - sC_{gd8}) + v_2(g_7 - sC_{gd7}) \tag{4.4b}$$

where $g_i = \sqrt{2I_{Di}\mu_p C_{ox}\frac{W_i}{L}}$ $(i = 1, 2, 3, 4)$ are the transconductances, C_{gdi} are the gate-drain parasitic capacitances of the corresponding devices.

Assuming a fully differential AC input signal ($v_1 = v_{in}/2$, $v_2 = -v_{in}/2$) around a common mode voltage $v_{cm} = 0$, the output current $i_{out} = i_{o1} - i_{02}$ can be written as

$$i_{out} = \frac{v_{in}}{2}(g_6 + g_7 - g_8 - g_9 - sC_{gd6} - sC_{gd7} + sC_{gd6} + sC_{gd9}) \tag{4.5}$$

If the geometric layout of the devices is arrange to make $sC_{gd8} + sC_{gd9} = sC_{gd6} + sC_{gd7}$, then the output current i_{out} can be expressed as $i_{out} = \frac{v_{in}}{2}(g_6 + g_7 - g_8 - g_9)$. Thus the transconductor exhibits the following transconductance value $g_m = \frac{1}{2}(g_6 + g_7 - g_8 - g_9)$, which is independent of the frequency to the first order approximation.

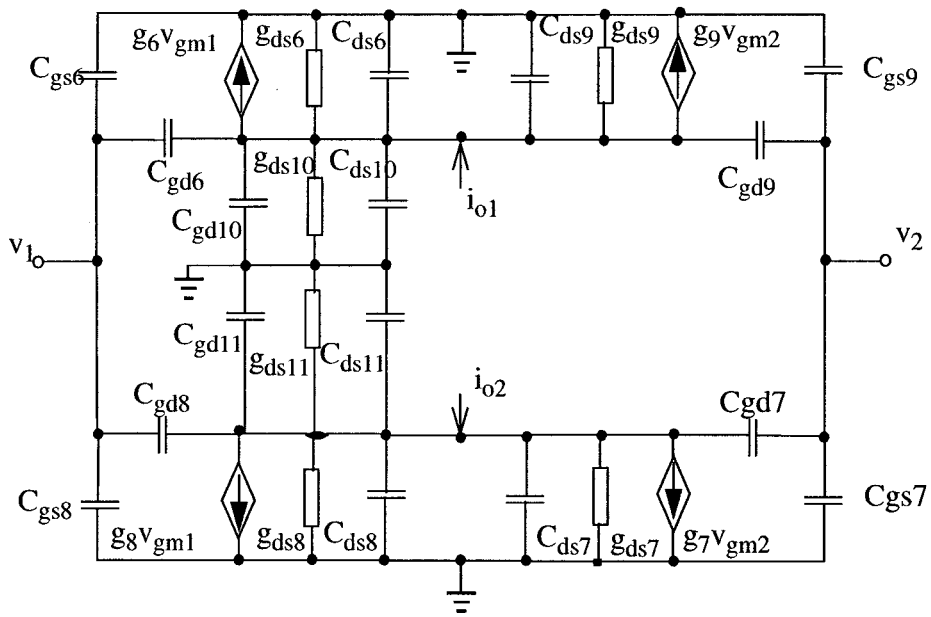


Figure 4.4 Small signal equivalent circuit of Assi's OTA

The output resistance of the transconductance is given by (the symbol || implies parallel connection)

$$R_{out} = (r_{ds6} \parallel r_{ds9} \parallel r_{ds10}) + (r_{ds7} \parallel r_{ds8} \parallel r_{ds11}) \tag{4.6}$$

In summary, the most important features of this OTA are:

- Voltage controlled tunable g_m value with very simple circuit.

- Absence of internal nodes, effect of gate-drain capacitances is cancelled to minimize the excess phase shift.

- Relatively low output resistance.

4.3.2 Raut's OTA

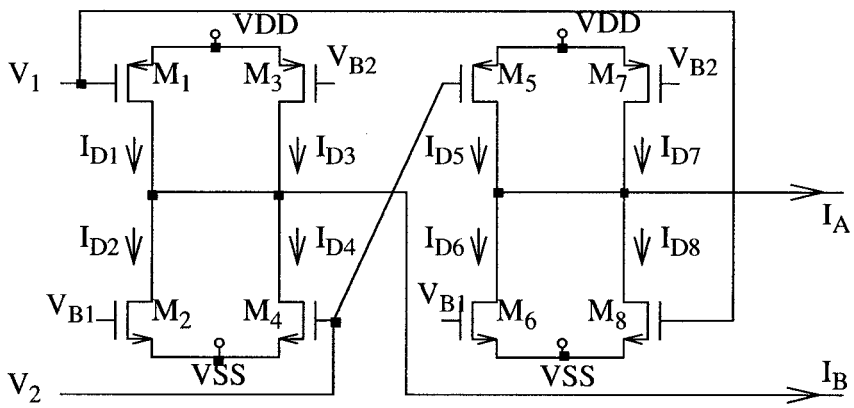


Figure 4.5 Circuit diagram of Raut's OTA

Figure 4.5 shows the OTA circuit diagram proposed by Raut [15]. It consists of 8 transistors connected in a fully differential structure. V_1, V_2 are the differential inputs, while V_{B1} and V_{B2} are the bias voltages.

Refer to the first half circuit, using the standard square-law model for MOS devices in saturation region, the currents I_A and I_B are easily derived as:

$$I_B = I_{D1} + I_{D3} - I_{D2} - I_{D4} \tag{4.7a}$$

$$I_A = I_{D5} + I_{D7} - I_{D6} - I_{D8} \tag{4.7b}$$

Thus the differential output current $I_{out} = I_A - I_B$ equals to

$$I_{out} = I_A - I_B = V_{in}[2\beta_1(VDD - |V_{TP}|) + 2\beta_4(VSS + V_{TN})] \tag{4.8}$$

where $\beta_1 = \frac{\mu_p C_{ox}}{2}\frac{W_1}{L_1}$, $\beta_4 = \frac{\mu_n C_{ox}}{2}\frac{W_4}{L_4}$, $|V_{TP}|$ is the PMOS threshold voltage, V_{TN} is the threshold voltage for NMOS, and $V_{in} = V_1 - V_2$ is differential input voltages. Here we assume that M_1-M_5, M_2-M_6, M_3-M_7 and M_4-M_8 are matched pairs.

Eq. (4.8) reveals the function of the circuit in Figure 4.5 as a linear voltage to current transducer, $I_{out} = g_m V_{in}$, where $g_m = [2\beta_1(VDD - |V_{TP}|) + 2\beta_4(VSS + V_{TN})]$ is the total transconductance parameter.

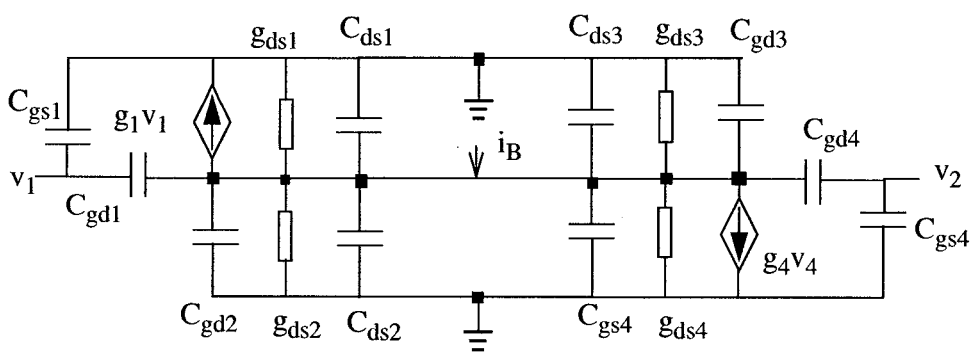


Figure 4.6 Half circuit of AC equivalent model

Refer to Figure 4.6, the half circuit of AC equivalent model, we can have:

$$-i_B = g_1 v_1 + g_4 v_2 - sC_{gd1} v_1 - sC_{gd4} v_2 \tag{4.9a}$$

Similarly, from another half part, we have:

$$-i_A = g_5 v_2 + g_8 v_1 - sC_{gd5} v_2 - sC_{gd8} v_1 \tag{4.9b}$$

Therefore, the differential small signal output current equals to:

$$i_{out} = i_A - i_B$$

$$= (g_1 - g_8)v_1 + (g_4 - g_5)v_2 - s(C_{gd1} - C_{gd8})v_1 - s(C_{gd4} - C_{gd5})v_2 \qquad (4.10)$$

As we mentioned before, we have assume $M_1 = M_5$, $M_4 = M_8$, which means that $g_1 = g_5$, $g_4 = g_8$, $C_{gd1} = C_{gd5}$, and $C_{gd4} = C_{gd8}$. We also assume here that a fully differential AC input signal ($v_1 = v_{in}/2$, $v_2 = -v_{in}/2$) around a common mode voltage $v_{cm} = 0$. Therefore, Eq.(4.10) goes to

$$i_{out} = 2(g_1 - g_8)v_{in} - 2s(C_{gd1} - C_{gd8})v_{in} \qquad (4.11)$$

If the geometric layout of the devices is arrange to make $C_{gd1} = C_{gd8}$, then the output current i_{out} can be expressed as $i_{out} = 2(g_1 - g_8)v_{in}$. Thus the transconductor exhibits the following transconductance value $g_m = 2(g_1 - g_8)$, which is independent of the frequency to the first order approximation.

The output resistance is given by:

$$R_{out} = r_{ds1} \parallel r_{ds2} \parallel r_{ds3} \parallel r_{ds4} + r_{ds5} \parallel r_{ds6} \parallel r_{ds7} \parallel r_{ds8} \qquad (4.12)$$

In summary, the most important features of this OTA are:

- Absence of internal nodes, effect of gate-drain capacitances is cancelled to minimize the excess phase shift.

- Relatively low output resistance.

4.3.3 Nauta's OTA

Figure 4.7 shows the OTA cell first proposed by Nauta [18].

The transconductor is based on the well-known CMOS inverter. The CMOS inverter has no internal nodes and has a good linearity in V-I conversion if the β factors of the NMOS and PMOS are perfectly matched.

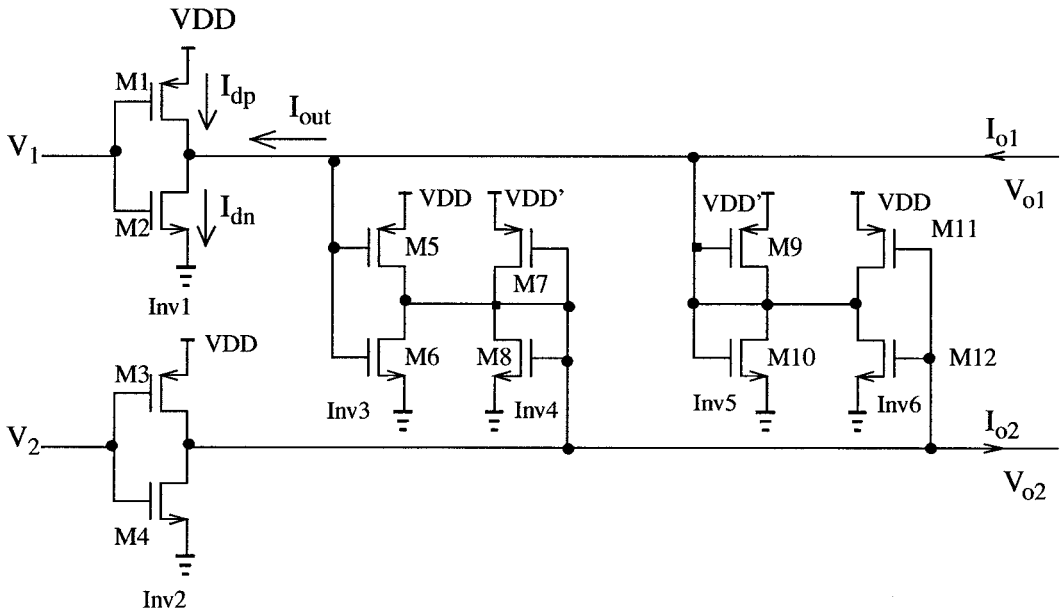


Figure 4.7 Nauta's inverter based OTA

Refer to the inverter 1 in Figure 4.7, if the NMOS and PMOS are both in saturation, the drain currents can be written as [18]

$$I_{dn} = \frac{\beta_n}{2}(V_{gsn} - V_{tn})^2 \qquad ,with \qquad \beta_n = \frac{\mu_n C_{ox} W_n}{L_n} \tag{4.13a}$$

$$I_{dp} = \frac{\beta_p}{2}(V_{gsp} - V_{tp})^2 \qquad ,with \qquad \beta_p = \frac{\mu_p C_{ox} W_p}{L_p} \tag{4.13b}$$

Then the output current of the single inverter can be written as:

$$I_{out} = I_{dn} - I_{dp} = a(V_1 - V_{tn})^2 + bV_1 + c \tag{4.14}$$

with

$$a = \frac{1}{2}(\beta_n - \beta_p) \tag{4.14a}$$

$$b = \beta_p(VDD + V_{tp} - V_{tn}) \tag{4.14b}$$

$$c = \frac{1}{2}\beta_p(V_{tn}{}^2 - (VDD + V_{tp})^2) \tag{4.14c}$$

If $\beta_n \neq \beta_p$, i.e. $a \neq 0$, the V-I conversion will not be linear. Anyhow, this error can be canceled by using a balanced structure.

Assume the two inverters Inv1 and Inv2 are matched and driven by a differential input voltage V_{id}, which is balanced around the common-mode voltage level V_c. The output current I_{o1} and I_{o2} can be calculated, and subtraction results in the differential output current I_{od}.

$$I_{od} = I_{o1} - I_{o2} = V_{id}(VDD + V_{tp} - V_{tn})\sqrt{\beta_n \beta_p} \tag{4.15}$$

here V_c is given by

$$V_c = \frac{VDD + V_{tp} - V_{tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} + V_{tn} \tag{4.16}$$

Thus the circuit has a linear differential transconductance $G_m = (VDD + V_{tp} - V_{tn})\sqrt{\beta_n \beta_p}$.

The other four inverters Inv3 - Inv6 serve as the common-mode control and DC-gain enhancement. If inverter Invi has transconductance g_{mi} and parasitic output conductance g_{di}, the common-mode output resistance at the node V_{o1} is

$$R_{cm} = \frac{1}{g_{d1} + g_{d5} + g_{d6} + g_{m5} + g_{m6}} \tag{4.17}$$

$$R_{dm} = \frac{1}{g_{d1} + g_{d5} + g_{d6} + g_{m5} - g_{m6}} \tag{4.18}$$

If for simplicity, we assume that for all i, $g_{di} = g_d$, and $g_{mi} = g_m$, the common-mode gain at either output node is $A_{cm} = \frac{g_m}{3g_d + 2g_m}$, which is less than unity, that means common-mode stability follows. On other hand, if we carefully design the circuit to obtain $g_{m5} \approx g_{m6} - (g_{d1} + g_{d5} + g_{d6})$, we can boost the output resistance to very large, theoretical to infinite.

The transconductor has no internal nodes (except ground and VDD), which opens for the possibility to merge the parasitic capacitances of the transconductor with those of the g_m-C filter. This enables the implementation of very high frequency filters.

In summary, the most important features of this circuit are:

- Absence of internal node, feasibly for high frequency wide band operation
- Negative resistance load to boost the output resistance.

4.3.4 Szcezpanski's OTA

The OTA first proposed by Szcezpanski [19] is shown in Figure 4.8. It is based on two cross-coupled differential pairs with identical MOS devices M_1-M_2, M_3 - M_4 operating in saturation region. M_{a3} works in linear region and provides an adjustable floating voltage V_B and an associated resistance r_{outB} between the source pair M_1-M_2 and M_3-M_4. M_{b4} provides dc biasing current $2I_o$.

First, we assume $r_{outB} = 0$. Then using the standard square-law model, we have:

$$I_{out} = I_1 - I_2 = 2k_n V_B V_{id} \tag{4.19}$$

Where $V_{id} = V_{in+} - V_{in-}$ is the differential input voltage. $k_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ is the transconductance parameter, and μ_n, C_{ox}, W, and L are the mobility, oxide capacitance per unit area, channel width and length respectively. Thus the circuit exhibits a perfectly tunable linear transconductance of value $G_m = 2k_n V_B$.

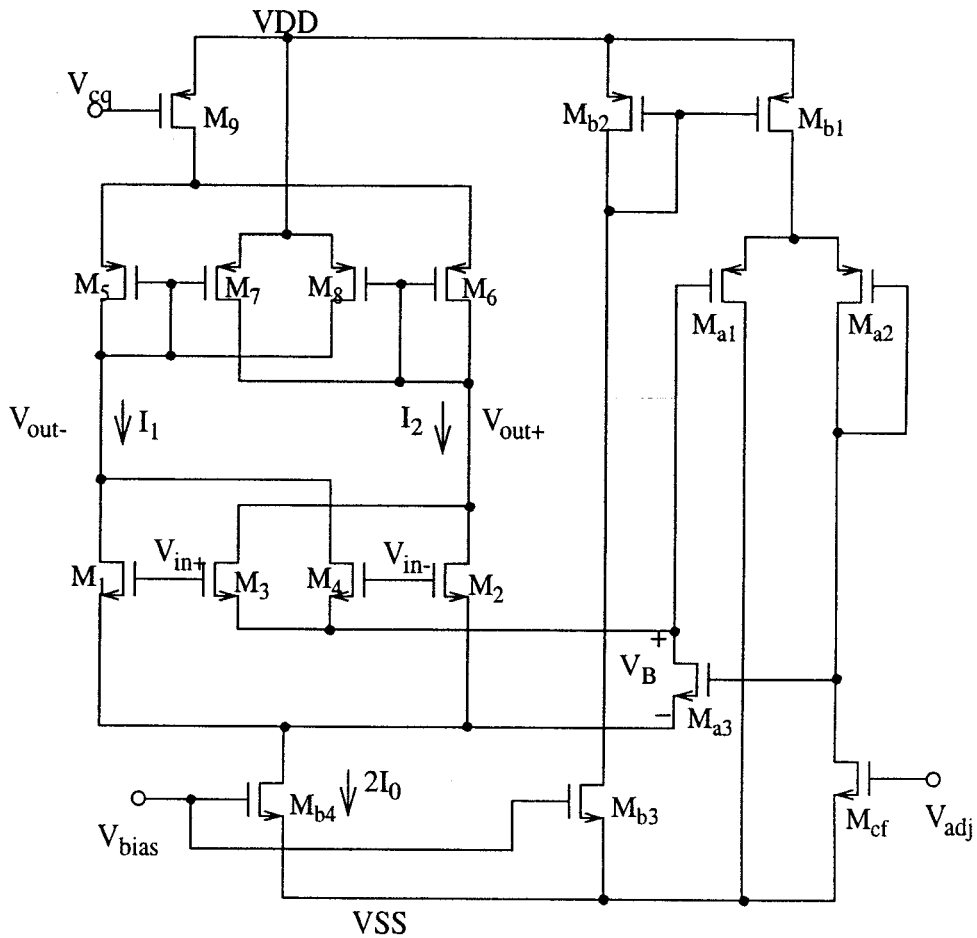


Figure 4.8 The circuit diagram of Szcezpanski's OTA cell

In reality, r_{outB} will never be zero, then the output current becomes,

$$I_{out} = 2k_n[V_B + r_{outB}(I_{d3} + I_{d4})]V_{id} \tag{4.20}$$

I_{d3} and I_{d4} are drain currents of devices M_3 and M_4. given by

$$I_{d3} + I_{d4} = I_o - k_n V_B \sqrt{\frac{2I_o}{k_n} - V_B^{\ 2} - V_{id}^{\ 2}} \tag{4.21}$$

When r_{outB} is small, the transconductance remains quite linear over a certain input range.

M_5 - M_8 serves as the voltage -controllable negative resistance load (NRL) to the transconductor. The NRL cancels out the small-signal drain-source resistances of M_1 - M_4, therefore, boost the output resistance of the transconductor, theoretically to infinite with proper design.

Owing to the absence of internal nodes, the OTA has excellent high-frequency performance. Using the simplified half-circuit equivalent in Figure 4.9, we can use nodal analysis technique to derive:

$$\frac{V_{out}}{V_{id}} = G_m + s(C_{gd4} - C_{gd1}) \tag{4.22}$$

Obviously, if we make the gate-drain capacitances C_{gd} of M_1, M_2 and M_3, M_4 equal, the OTA transconductance frequency dependent component caused by MOS devices gate-drain capacitances is cancelled out, resulting a very wideband frequency response. This can be achieved by select $W_{M1} = W_{M2} = W_{M3} = W_{M4}$.

In summary, the most important features of this OTA are,

- Cross-coupled differential pairs input with equivalent floating voltage adjustment.

• Absence of internal nodes, output resistance enhanced by negative resistance load.

• Effect of gate-drain capacitances is cancelled to minimize the excess phase shift.

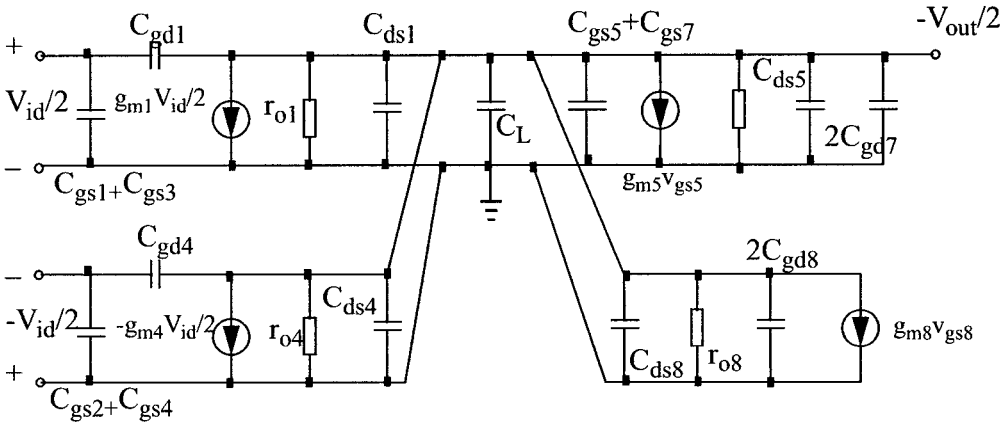


Figure 4.9 Half circuit of ac equivalent circuit of Szczepanski's OTA

4.3.5 Voghell's OTA

Figure 4.10 shows the OTA cell first proposed by Voghell [20]. It is composed of two cross-coupled differential PMOS pairs as input stage and a folded cascade output stage that gives a high output resistance. Anyhow, this additional introduced internal nodes will limit the operation frequency.

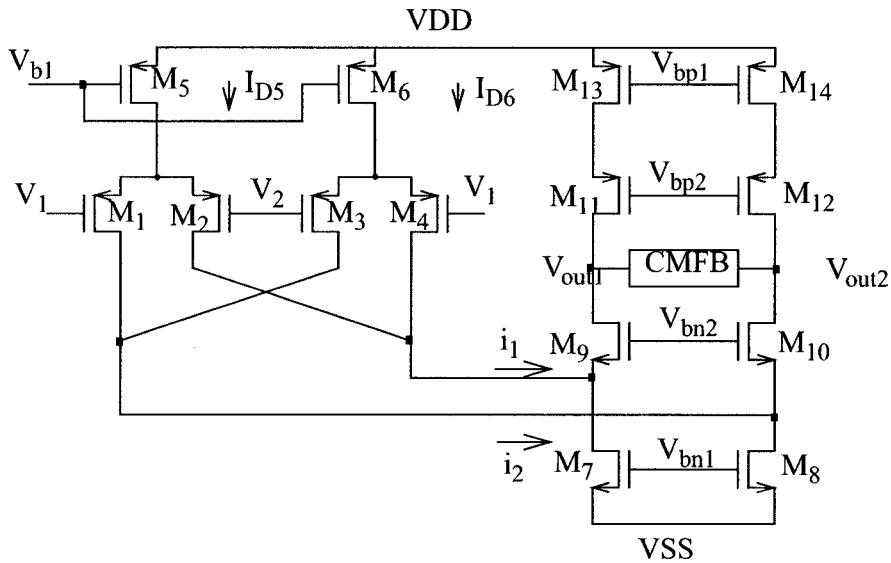


Figure 4.10 Circuit diagram of Voghell's OTA

Refer to Figure 4.10, V_1 and V_2 are differential input terminals. Vb1, Vbp1, Vbp2, Vbn1, Vbn2 are the bias voltages which can be used to adjust the transconductance value of the circuit. The CMFB block is used to stabilize the output DC voltage.

Assume $v_1 = \frac{v_{in}}{2}$, $v_2 = -\frac{v_{in}}{2}$, and by neglecting the output stage effect, we may have following equations:

$$i_{out} = i_2 - i_1 \tag{4.23}$$

$$i_{out} = (v_1 g_{m1} + v_2 g_{m3}) - (v_1 g_{m4} + v_2 g_{m2}) \tag{4.24}$$

We set $M_1 = M_2 = M_3 = M_4$, which means:

$$g_{m1} = g_{m2} = \sqrt{2\mu_p C_{ox} \frac{W}{L} I_{D5}} \tag{4.25a}$$

$$g_{m3} = g_{m4} = \sqrt{2\mu_p C_{ox}\frac{W}{L}I_{D6}} \tag{4.25b}$$

Therefore, we get

$$g_m = \frac{i_{out}}{v_{in}} = \sqrt{2\mu_p C_{ox}\frac{W}{L}}(\sqrt{I_{D5}} - \sqrt{I_{D6}}) \tag{4.26}$$

The output resistance is given by:

$$\begin{aligned} R_{out} \approx & [r_{ds11}(1 + g_{m11}r_{ds13})] \parallel [r_{ds9}(1 + g_{m9}r_{ds7})] \\ & + [r_{ds12}(1 + g_{m12}r_{ds14})] \parallel [r_{ds10}(1 + g_{m10}r_{ds8})] \end{aligned} \tag{4.27}$$

The most important features of this transconductance are:

- Folded cascade output stage to enhance the output resistance
- Limited bandwidth due to the introduction of internal node

4.3.6 Martinez's OTA

The Martinez's OTA [21] shown in Figure 4.11 is based on complementary differential paris (M_p and M_n). M_3 and M_4 are biased in the triode region which serve as source degeneration to improve the linearity performance of the OTA. The N type source degeneration transistor M_3 is split into two transistors to take advantage of the V_{cm} node to sense the common-mode voltage needed for the design of CMFB. The common -mode control voltage is applied to the V_n node to adjust the bias current I_B.

V_{DSsatn} and V_{DSsatp} are the saturation voltage of M_n and M_p respectively. $N_{n,p}$ is the source degeneration factor, given by

$$N_n \approx \frac{2g_{mn}}{\beta_3(V_{GS3} - V_{tn})} \qquad N_p \approx \frac{g_{mp}}{\beta_4(V_{GS4} - V_{tp})} \tag{4.30}$$

Thus, the small-signal transconductance of the OTA becomes,

$$G_m = \left[\frac{\partial I}{\partial V}\right]\Bigg|_{V=0} = \frac{g_{mn}}{N_n + 1} + \frac{g_{mp}}{N_p + 1} \tag{4.31}$$

The most importance features of this transconductance cells:

- Source degeneration technique is used to linearize the transconductance

4.3.7 Koziel's OTA

The OTA cell proposed by Koziel [22] is presented in Figure 4.12. It this circuit the input stage is the cross-coupled quad cell formed by two unsymmetrical differential pairs (M_1 - M_4) and a conventional symmetrical differential pair (M_5, M_6) to increase the linearity performance of the OTA. M_9 - M_{10}, M_{13} - M_{14}, M_{19} -M_{20}, and M_{25} -M_{26} form the folded cascade output stage to enhance the output resistance. Other MOS devices are connected as the classical current mirror circuits.

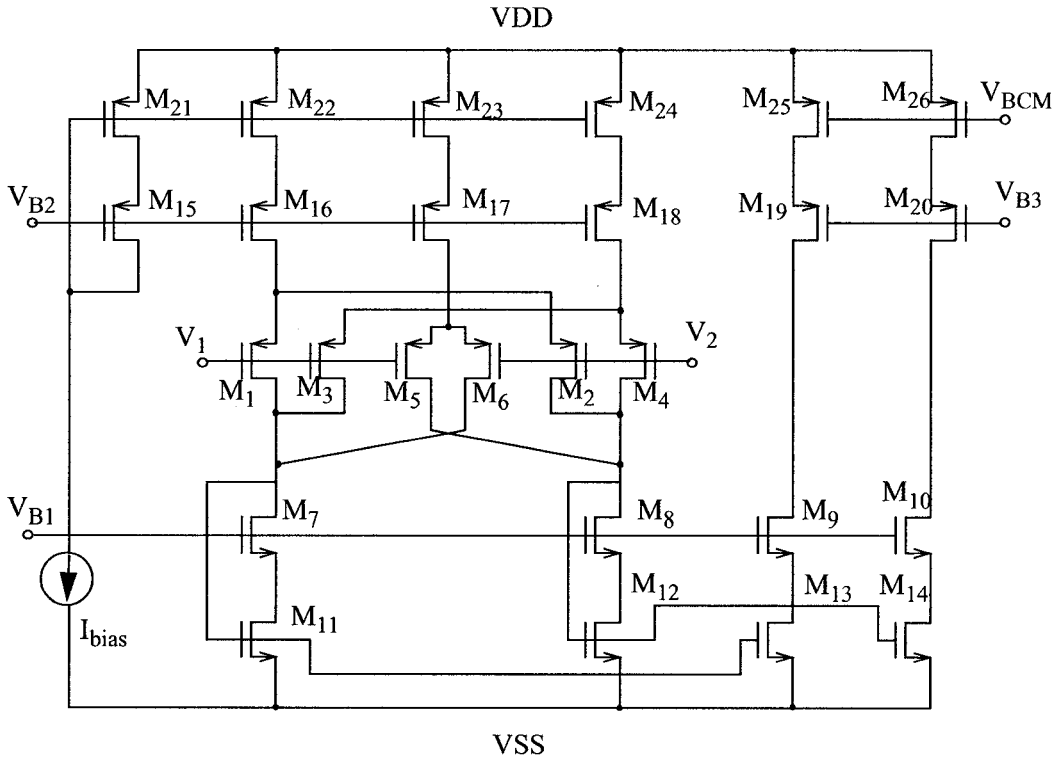


Figure 4.12 OTA cell proposed by Koziel

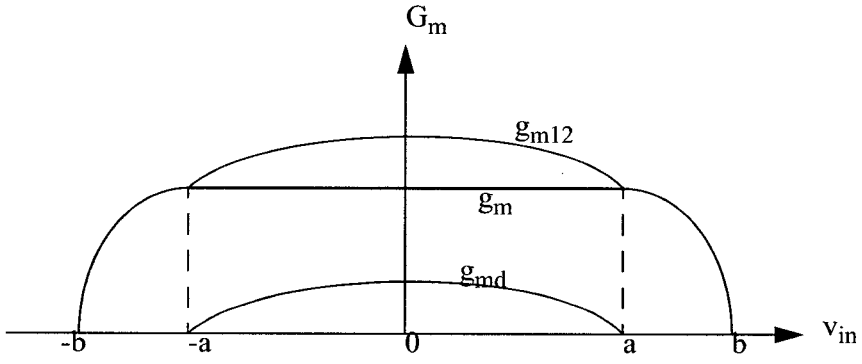


Figure 4.13 The linearity characteristic of Koziel's OTA

Refer to Figure 4.13. The curve g_{m12} is the transconductance caused by M_1 - M_4, and the g_{md} is the transconductance given by M_5 - M_6. The transistor size of input stage (M1- M6) is arranged is such a way so that the non-linearity of g_{m12} in the input range (-a, a) is equal to the transconductance g_{md} of M5 - M6. The overall transconductance of the OTA cell is g_{m12} minus g_{md}, therefore can remain in quite good linear in the input range (-a, a).

The most important features of this transconductance cell are:

- Quite complex input stage to improve the linearity of the OTA.
- Folded cascade output stage to increase the output resistance.

4.4 OTA Cells Performances Comparison

As mentioned before, the main characteristics of a practical OTA are: (i) limited linear input voltage range, (ii) finite bandwidth, (iii) finite signal to noise ratio (S/N), and (iv) finite output impedance. In order to select an optimum OTA cell to implement the wideband filter, we compared these OTA cells' performances in terms of DC power dissipation and substrate area requirement. The DC power consumption and the silicon area requirement are considered to be the cost factors associated with each device. All the circuits are simulated using 0.35 μm CMOS technical process model in level 49. The DC power supply employed was $\pm 1.5V$. The transconductance value and bandwidth of the OTA cells are simulated with 1 ohm resistor load to ground. The dynamic range is calcu-

ated from the simulation results of the input harmonic signal rms levels at 1% total harmonic distortions (THD) (transient simulation with the load open circuit) and the rms values of the noise floor. The output resistance is simulated by injecting current at the output terminals with the input open circuit. The comparison results are tabulated in Table 1.

Table 1: Comparison results on several OTAs selected from literature

Work by	Assi [17]	Raut [15]	Nauta [18]	Szczepanski [19]	Voghell [20]	Martinez [21]	Koziel [22]
Transconductance (g_m, uA/V)	180.5	117.0	584.6	284.4	80.3	421.5	215.5
Bandwidth (bw, Hz)	10 G	10 G	3 G	10 G	100 M	100 M	100 M
Dynamic Range (dr, dB)	82.8	76.0	90.8	84.0	55.0	88.5	70.6
Output resistance (R_o,ohm)	16.7 K	12.0 K	229.0 M	314.0 M	1.2 M	195.4 K	3.4 M
Power dissipation (Pdc,mW)	4.48	7.48	12.87	4.38	2.50	2.00	5.50
Area (Ar, μm^2)	3.336	3.728	3.488	13.808	10.522	7.388	144.360
Sum performance	0.001	0.0009	8.34	9.44	0.059	0.013	0.064

Row 7 in the table represents the sum $\sum\left(\frac{g_{mi}}{P_{dc}}+\frac{bw_i}{P_{dc}}+\frac{dr_i}{P_{dc}}+\frac{R_{oi}}{P_{dc}}+\frac{g_{mi}}{Ar}+\frac{bw_i}{Ar}+\frac{dr_i}{Ar}+\frac{R_{oi}}{Ar}\right)$, where $i = 1, 2, \ldots, 7$ for the seven OTA circuits studied.

The comparison results show that the OTA cell reported in [19] will be a good choice for implementing a wideband, highly linear system. Thus this OTA cell is selected to use in the design of the filter in this project.

Based on the comparison results, the best four OTA cells [17] [18] [19] [21] from the seven are selected to fabricate a chip. The layout is done with 0.35 μm one-poly-three-metal CMOS technological process. The layout diagram is shown in Figure 4.14. The measurement results are presented in Chapter 6.

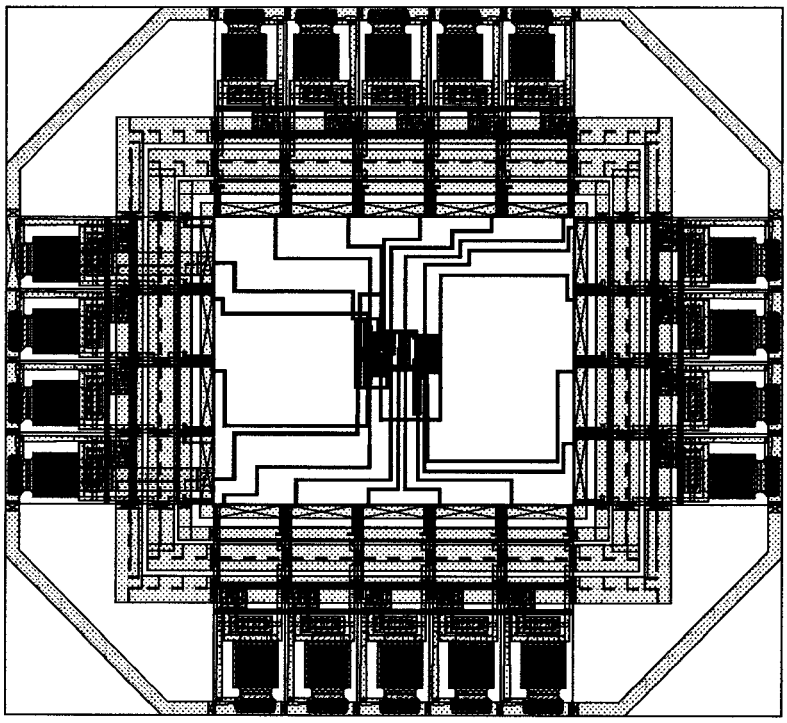


Figure 4.14 Chip layout for OTA cells (Area 1750 x 1600 μm^2)

4.5 Summary

OTA is a voltage controlled current source (VCCS). Ideally, it has infinite input and output impedances and infinite bandwidth. In reality, the main characteristics of a practical OTA are: (i) limited linear input voltage range, (ii) finite bandwidth, (iii) finite signal to noise ration, and (iv) finite output impedance.

OTA cells are extensively used to design easy tunable, high frequency, wideband analog integrated filters since they offer good performances with low power consumption and high frequency operation.

In this work, several existing OTA cells reported in the literature are studied and compared with the goal to choose the optimum one for the implementation of the wide-band filter. The selection criteria are based on the g_m value, bandwidth, output resistance and dynamic range in terms of DC power dissipation and the substrate area requirements. The comparison shows that the OTA cell proposed by Szczepanski gives best overall performance among those OTA cells studied. Thus this cell is the candidate for the filter design in this work

Chapter 5

Filter Design

5.1 Introduction

After the filter architecture and the Operational Transconductance Amplifier cell have been chosen, this chapter gives the details on the design of a sixth order Chebyshev bandpass filter which has a bandwidth from 2 MHz to 400 MHz with 1 dB ripple in the passband. The filter is realized using 0.18 μm one-poly-six-metal CMOS technology. (At that time, Canadian Microelectronics Corporation was planning to phase out the technical support of 0.35 μm CMOS process technology, so the 0.18 μm CMOS technology was used to design the filter instead of 0.35 μm CMOS technology which was used to compare the OTA cells performance)

5.2 Filter Synthesis

Referring to the general primary resonator block technique structure discussed in Chapter 3, for a sixth order fully differential filter design using PRB technique, the structure is shown in Figure 5.1. The T(s) blocks are biquad filters realized using OTAs.

The corresponding voltage transfer function is given by:

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{\alpha T^3(s)}{1 + F_1 T(s) + F_2 T^2(s) + F_3 T^3(s)} \tag{5.1}$$

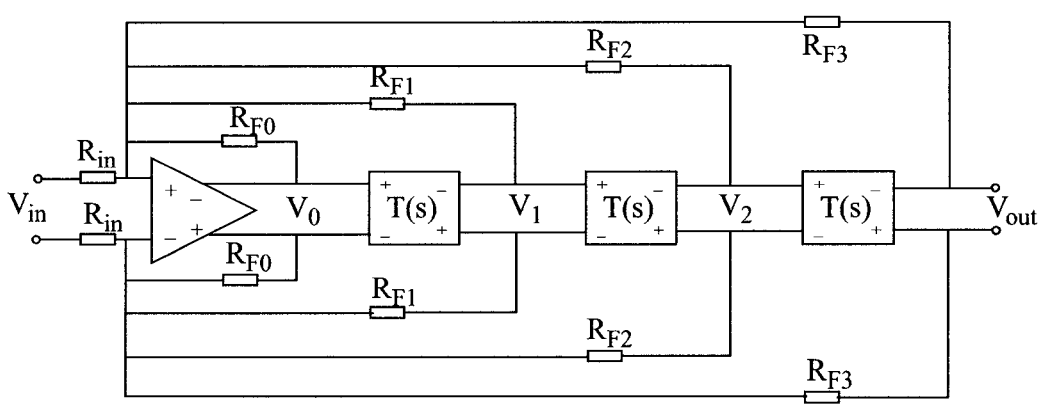


Figure 5.1 Fully differential sixth order bandpass filter in PRB structure

In the above, we define α, the feedback factor F_i as: $\alpha = \frac{R_{F0}}{R_{in}}$, and $F_i = \frac{R_{F0}}{R_{Fi}}$, i= 1, 2, 3.

The standard procedure to synthesize the bandpass filter transfer function is to use a prototype lowpass function and apply the $LP \leftrightarrow BP$ transformation to derive the bandpass transfer function. The pertinent equation is:

$$p \leftrightarrow Q\frac{s^2+1}{s} \tag{5.2}$$

Each second-order bandpass section has a transfer function (with normalized center frequency=1 rad/sec)

$$T(s) = A\frac{s/Q_i}{s^2+s/Q_i+1} \tag{5.3}$$

The associated first-order lowpass filter transfer function is:

$$T_{LP}(p) = A\frac{q}{p+q} \tag{5.4}$$

where $q = Q/Q_i$, Q_i is the quality factor of the individual second order section (i = 1, 2, 3), and A is the dc gain of the lowpass section.

The lowpass function associated with the sixth order filter realized with three PRB biquads is then obtain by replacing each T(s) with $T_{LP}(s)$ as above.

The lowpass function is given by:

$$H_{LP}(p) = -\frac{\alpha A^3 q^3}{(p+q)^3 + f_1(p+q)^2 + f_2(p+q) + f_3} \tag{5.5}$$

Here we introduced the symbol $f_i = F_i \prod_{j=1}^{i} A_j q_j$, i=1, 2, 3. For primary resonator block technique, A_i and q_i (i=1, 2, 3) are made all identical.

Standard filter function tables, however, give the normalized lowpass function for a sixth order bandpass filter, as

$$\overline{H}_{Lp}(p) = -\frac{a_0}{b_3 p^3 + b_2 p^2 + b_1 p + b_0} \tag{5.6}$$

Compare Eq. (5.5) with (5.6), we can have following design equations:

$$a_0/b_3 = \alpha A^3 q^3 \tag{5.7a}$$

$$b_2/b_3 = 3q + f_1 \tag{5.7b}$$

$$b_1/b_3 = 3q^2 + 2f_1 q + f_2 \tag{5.7c}$$

$$b_0/b_3 = q^3 + f_1 q^2 + f_2 q + f_3 \tag{5.7d}$$

The system in equation (5.7) represents four equations for six unknowns, α, A, q, f_i, i =1, 2, 3, which indicated that two parameter can be used for optimization purposes.

The optimization is emphasized on the gain constant A which is selected to maximize the circuit's dynamic range. The gain constant A is selected in such a way that peak magnitude response of three biquad sections are almost equal which will lead to a maximum dynamic range for the overall circuit [1].

The output voltage of the bandpass filter can be expressed as follows:

$$V_{out} = H(j\omega)V_{in} \tag{5.8}$$

with $0 \le \omega \le \infty$.

The internal output voltages can be written as:

$$V_2 = \frac{V_{out}}{T(j\omega)} = \frac{H(j\omega)}{T(j\omega)}V_{in} \tag{5.9a}$$

$$V_1 = \frac{V_{out}}{T^2(j\omega)} = \frac{H(j\omega)}{T^2(j\omega)}V_{in} \tag{5.9b}$$

$$V_0 = \frac{V_{out}}{T^3(j\omega)} = \frac{H(j\omega)}{T^3(j\omega)}V_{in} \tag{5.9c}$$

T(s) is the second order bandpass filter transfer function, from Eq.(5.3), we get the magnitude of the second order bandpass filter as:

$$|T(j\omega)| = \frac{A}{\sqrt{1 + Q_i^2\left(\omega - \frac{1}{\omega}\right)^2}} \tag{5.10}$$

From Eq. (5.9) and (5.10), we have the magnitude of internal output voltages are:

$$|V_2| = |H(j\omega)|\frac{\sqrt{1 + Q_i^2\left(\omega - \frac{1}{\omega}\right)^2}}{A}V_{in} \tag{5.11a}$$

$$|V_1| = |H(j\omega)|\left[\frac{\sqrt{1 + Q_i^2\left(\omega - \frac{1}{\omega}\right)^2}}{A}\right]^2 V_{in} \tag{5.11b}$$

$$|V_0| = |H(j\omega)|\left[\frac{\sqrt{1+Q_i^2\left(\omega-\frac{1}{\omega}\right)^2}}{A}\right]^3 V_{in} \tag{5.11c}$$

and $|V_{out}| = |H(j\omega)|V_{in}$ (5.11d)

To maximize the overall filter dynamic range, we need to arrange

$$max\{|V_0|\} \approx max\{|V_1|\} \approx max\{|V_2|\} \approx max\{|V_{out}|\} \quad . \tag{5.12}$$

Which means that the optimum gain constant of the second order bandpass filter is given by:

$$A \approx max\left[\sqrt{1+Q_i^2\left(\omega-\frac{1}{\omega}\right)^2}\right] \tag{5.13}$$

As we know, the term $\sqrt{1+Q_i^2\left(\omega-\frac{1}{\omega}\right)^2}$ reach the maximum value when the frequency close to the bandedge of the high order bandpass filter [1], where by definition

$$\left(\omega-\frac{1}{\omega}\right)^2 \approx \frac{1}{Q^2} \tag{5.14}$$

here Q is quality factor of high order bandpass filter given by $Q = \frac{\omega_p}{BW}$.

Thus the second order bandpass filter section gain constant for dynamic range optimization is:

$$A \approx \sqrt{1 + \left(\frac{Q_i}{Q}\right)^2} = \sqrt{1 + \frac{1}{q^2{}_i}} \tag{5.15}$$

For 1 dB ripple Chebyshev filter, the normalized lowpass transfer function is given by:

$$H_{LP}(p) = -\frac{0.491}{p^3 + 0.988p^2 + 1.238p + 0.491} \tag{5.16}$$

And the specification of the bandpass filter is given by:

the center frequency $\omega_p = 2\pi\sqrt{2M \times 400M} = 177.7153 Mrad/s$;

the bandwidth $BW = 2\pi(400M - 2M) = 2\pi \cdot 398 Mrad/s$;

and the quality factor $Q = \frac{\omega_p}{BW} = 0.07107$.

With the above equations and filter specification, we can synthesis the optimized biquad specification and feedback factors as tabulated in table 2.

Table 2: Biquad specification and feedback factors

H_0	2.38
Q_p	0.1535
ω_p (Mrad/s)	177.7153
α	0.367
F_i (i=1,2,3)	-0.3639, 0.7957, 0.02268

With reference to Figure 5.1, $\alpha = \frac{R_{F0}}{R_{in}}$, $F_i = \frac{R_{F0}}{R_{Fi}}$ (i =1, 2, 3). ω_p, Q_p and H_0 are the center frequency, quality factor and magnitude at the center frequency of a standard second order bandpass filter transfer function $H(s) = \dfrac{H_0 \frac{\omega_p}{Q_p} s}{s^2 + \frac{\omega_p}{Q_p} s + \omega^2{}_p}$.

5.3 Biquad Section

Second order filter function is constructed by integrator, feedback and summation which can be easily realized using OTA cells. Figure 5.2 shows those basic building blocks.

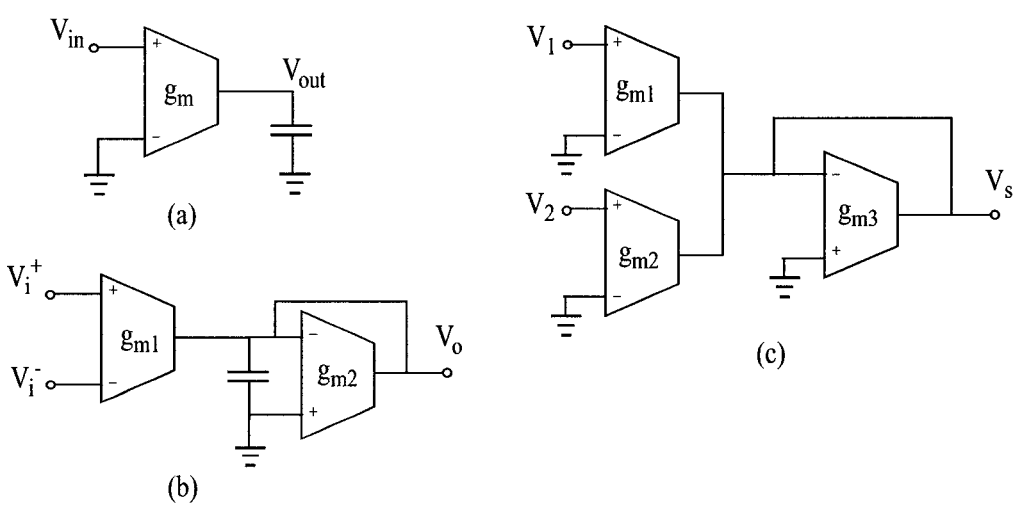


Figure 5.2 g_m-C building block (a) lossless integrator (b) lossy differential integrator (c) summation

There are many structure available for OTA-C second order bandpass filter. In this work, we chose the structure whose capacitors are not floating. Figure 5.3 shows the fully differential second order bandpass filter circuit diagram.

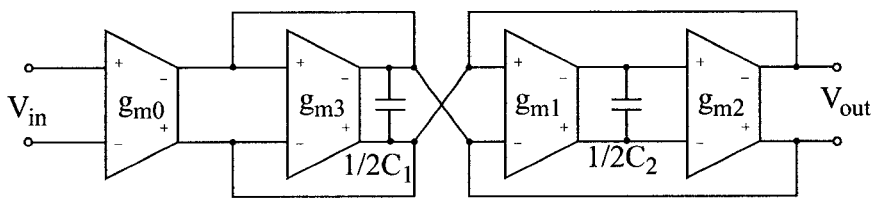


Figure 5.3 OTA-C fully differential second order bandpass filter

The ideal transfer function is determined by the small signal transconductances and load capacitors, as shown below

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{sg_{m0}C_2}{s^2C_1C_2 + sg_{m3}C_2 + g_{m1}g_{m2}} \tag{5.17}$$

The center frequency is $\omega_p = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$, the quality factor is $Q_p = \frac{1}{g_{m3}}\sqrt{\frac{g_{m1}g_{m2}C_1}{C_2}}$ and the magnitude at the center frequency is $H_0 = \frac{g_{m0}}{g_{m3}}$.

Setting $g_{m1} = g_{m2}$, we get following design equations:

$$g_{m1} = g_{m2} = \omega_p\sqrt{C_1C_2} \tag{5.18a}$$

$$g_{m3} = \frac{\omega_p}{Q_p}C_1 \tag{5.18b}$$

$$g_{m0} = H_0 \frac{\omega_p}{Q_p} C_1 \tag{5.18c}$$

Assume C_1 = 1 pF and C_2 = 4 pF, from the data in Table 2, we have following data for the biquad section as listed in table 3.

TABLE 3. Biquad design data

$g_{m1} = g_{m2}$	355.4 uA/V
g_{m3}	1157.8 uA/V
g_{m0}	2755.5 uA/V
C_1	1 pF
C_2	4 pF

In high frequency operation, the input and output parasitic capacitors of the OTA must be taken into consideration, which means actual value of C_1, C_2 need to deduct the parasitic capacitors values from their theoretical calculated values. Therefore,

$$C_{1actual} = C_{1cal} - (C_{ingm1} + C_{outgm2} + C_{ingm3} + C_{outgm3} + C_{outgm0}) \tag{5.19a}$$

$$C_{2actual} = C_{2cal} - (C_{outgm1} + C_{ingm2}) \tag{5.19b}$$

Refer to Figure 4.8 the input and output parasitic capacitors of the OTA cell are given by:

$$C_{in} = C_{gs1} + C_{gs3} + 2C_{gd1} \tag{5.20a}$$

$$C_{out} = C_{ds1} + C_{ds4} + C_{ds5} + C_{ds8} + C_{gs5} + C_{gs7} + 2C_{gd1} + 2C_{gd7} + 2C_{gd8} \tag{5.20b}$$

5.4 Biquad Sections Connection

5.4.1 Buffer

The principle used in relation with Figure 5.1 assumes that the biquadratic blocks T(s) will be implemented by VCVS elements (i.e. OP-AMP). Since our building blocks are OTA based biquads, we used a low output impedance buffer at the end of each OTA-based biquad section. The biquad sections were than cascaded as in the system diagram of figure 5.1. For high frequency operation, it is essential to have a wideband buffer. Figure 5.4 shows a high frequency buffer circuit [23].

An ideal buffer circuit should have very high input impedance, very low output impedance, gain near unity, highly linearity and wide frequency response.

The buffer circuit comprises of two compound transistors, one p-type and one n-type connected in a push-pull arrangement. M_3 - M_4 and M_7 - M_8 are current mirror circuits which are arranged acting as NMOS-PMOS gate-source voltage matching circuit [24]. In this way, the output DC voltage of the buffer is forced to be equal to the input DC voltage automatically.

Since we are using 0.18 μm CMOS technological process, which is an NWELL process, we connect the bulk terminals of PMOS devices M_2, M_4 and M_5 to their source terminals to bring the buffer gain close to unity.

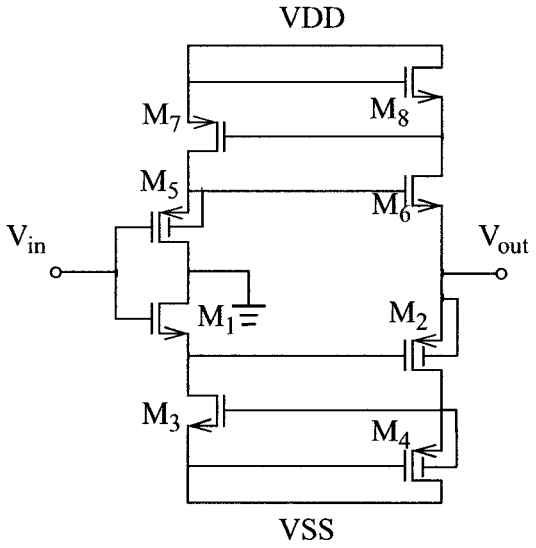


Figure 5.4 Wideband buffer circuit

When the biquad section of Figure 5.3 is terminated with the buffer, the H_0 needs to be adjusted to compensate for the loss due to non unity gain of the buffer.

5.4.2 OP-AMP

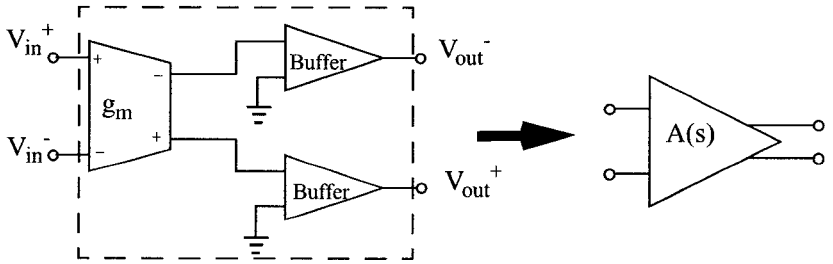


Figure 5.5 A fully differential OP-AMP constructed by an OTA and two buffers

Refer to Figure 5.1, an OP-AMP is used to sum up the input signals and feedback signals. The fully differential OP-AMP is constructed by an OTA followed by a buffer as shown in Figure 5.5.

5.4.3 High Frequency Compensation

The OP-AMP shown in Figure 5.5 has limited bandwidth which will affect the performance of the filter in the high frequency range. A small capacitor can be connected in parallel with the input resistor to compensate for the loss of gain of the OP-AMP at high frequency [1]. This arrangement is shown in figure 5.6

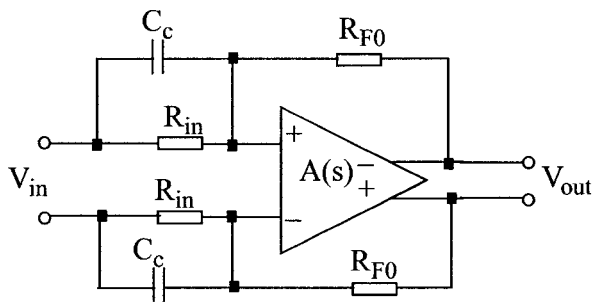


Figure5.6 High frequency compensation circuit

Simple analysis yields,

$$\frac{V_{out}}{V_{in}} = -\frac{R_{F0}}{R_{in}} \frac{1 + sC_c R_{in}}{1 + \left(1 + \frac{R_{F0}}{R_{in}}\right)\frac{s}{\omega_t}} \tag{5.21}$$

where ω_t is the gain-bandwidth product of the OP-AMP. Thus the small capacitor value can be determined by

$$C_c = \frac{1 + R_{F0}/R_{in}}{\omega_t R_{in}} \tag{5.22}$$

5.4.4 MOS Resistors

The resistors in Figure 5.1 are in fully differential structure. The transistor pair can be realized using MOS devices working in linear region in differential configuration [25] which is shown in Figure 5.7. The equivalent resistance is given by

$$R_{equiv} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{c1} - V_{c2})} \tag{5.23}$$

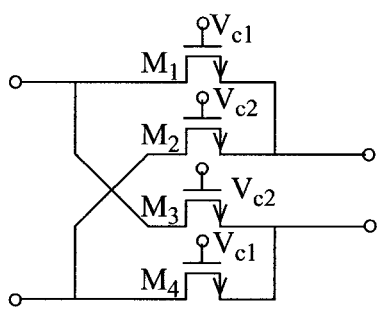


Figure 5.7 MOS transistors realization of fully differential resistors

5.5 Filter Design Data

Based on the theoretical calculation, the filter design data are finalized with the help of HSPICE simulation. Following tables give the transistor sizes of OTA cells, buffer circuits, MOS resistances, as well as the control voltages. The power supply employed are ±1.5 V.

Table 4: OTA cells transistor sizes (μm) (refer to Figures 4.8 and 5.3)

	M1	M2	M3	M4	M5	M6
g_{m1}, g_{m2}	2.08/0.5	2.08/0.5	2.08/1.35	2.08/1.35	3.16/0.5	3.16/0.5
g_{m3}	6.25/0.5	6.25/0.5	6.25/1.5	6.25/1.5	9.2/0.5	9.2/0.5
g_{m0}	18.65/0.5	18.65/0.5	18.65/1.65	18.65/1.65	20.4/0.5	20.4/0.5
	M7	M8	M9	Ma1	Ma2	Ma3
g_{m1}, g_{m2}	3.16/0.5	3.16/0.5	37.19/0.5	0.6/0.5	0.6/0.5	20/0.5
g_{m3}	9.2/0.5	9.2/0.5	113.2/0.5	0.6/0.5	0.6/0.5	45/0.5
g_{m0}	20.4/0.5	20.4/0.5	241.48/0.5	0.6/0.5	0.6/.5	65/0.5
	Mb1	Mb2	Mb3	Mb4	Mcf	
g_{m1}, g_{m2}	4.5/0.5	0.7/0.5	0.5/1.0	30/0.5	1.1/1.0	
g_{m3}	4.5/0.5	0.7/0.5	0.5/1.0	90/0.5	1.1/1.0	
g_{m0}	4.5/0.5	0.7/0.5	0.5/1.0	195/0.5	1.1/1.0	

Table 5: Buffer transistor sizes (μm) (refer to Figure 5.4)

M1	M2	M3	M4	M5	M6	M7	M8
4/0.18	16/0.18	2/0.18	16/0.18	8/0.18	20/0.18	20/0.18	7/0.18

Table 6: MOS resistance data (refer to Figure 5.7)

	W	L	V_{C1}	V_{C2}
R_{in}	0.80 μm	0.51 μm	1.5 V	1.0 V
R_{F0}	2.0 μm	0.50 μm	1.5 V	1.0 V
R_{F1}	0.80 μm	0.51 μm	1.5 V	1.0 V
R_{F2}	1.62 μm	0.50 μm	1.5 V	1.0 V
R_{F3}	1.0 μm	2.0 μm	1.5 V	1.4 V

Table 7: Capacitors values (refer to Figure 5.3)

C_1	560 fF	C_2	3.8 pF

Table 8: OTA cells control voltages (refer to Figure 4.7)

	V_{bias}	V_{adj}	V_{cq}
g_{m1}, g_{m2}	-0.8 V	-0.8 V	0.5 V
g_{m3}	-0.8 V	-0.8 V	0.5 V
g_{m0}	-0.8 V	-0.8 V	0.5 V

5.6 Physical Layout Consideration

A number of strategies are adopted for the filter layout design. These include the common-centroid layout for the differential source-coupled pair to minimize mismatching effects; large size transistors are done in fingered style to reduce the junction capacitance; capacitors are arranged in NWELL and shielded with VDD-ring to minimize the interference from substrate noise.

5.6.1 Matching issues

When integrated components are realized using lithographic techniques, a variety of two-dimensional effects can cause the effective sizes of the components to differ from the sizes of the glass layout masks. For example, overetching effect will cause the transistor polysilicon layer to be smaller than the corresponding mask layout [26]. For example, referring to the n-channel transistor shown in Figure 5.8(b), the p^+ field implant under the field oxide cause the effective substrate doping to be greater at the sides of the transistors than elsewhere. This increased doping raises the effective transistor threshold voltage near the sides of the transistors and therefore decreases the channel-charge density at the edges, which results in that the effective width of the transistor is less than the width drawn on the layout mask.

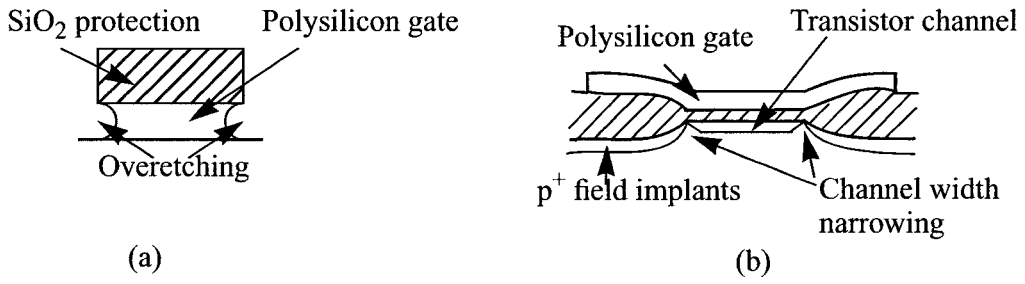


Figure 5.8 Examples of two-dimensional effects causing sizes of realized transistors to differ from sizes of layout masks.

The OTA cell we used to design the filter contains lots of source-coupled transistor pairs which are needed to be matched precisely. To minimize these second-order size error

effects, the source-coupled pairs are realized using common-centroid layout technique [27]. Figure 5.9 shows the sample of the common-centroid layout technique.

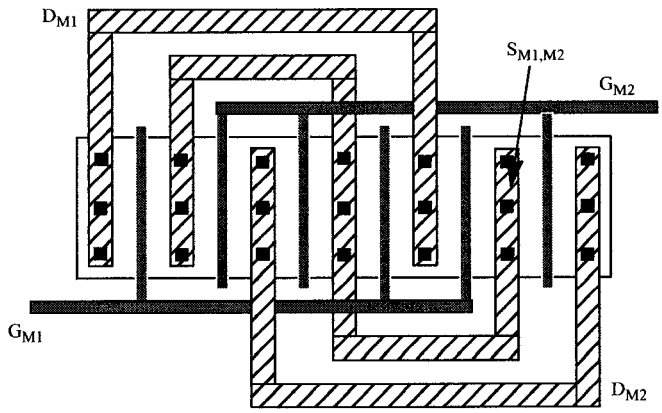


Figure 5.9 A common-centroid layout for a differential source-coupled pair

5.6.2 Larger Size Transistor

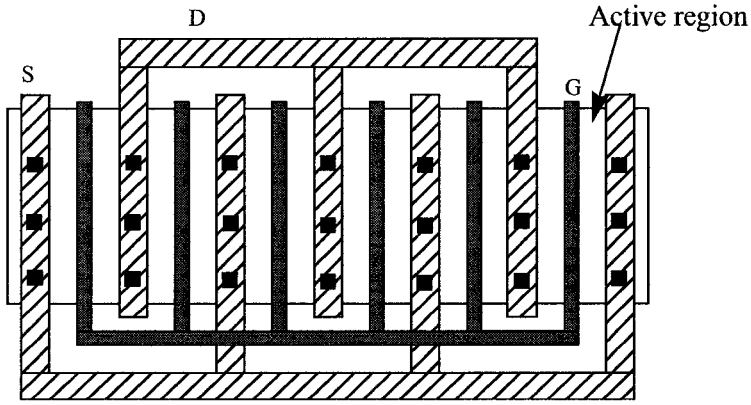


Figure 5.10 Fingered devices to reduce parasitic drain capacitances

The large size transistors are fingered to share the drains of the devices. This reduces the parasitic junction (drain) capacitances of the transistors which are quite critical for high frequency operations. Figure 5.10 shows this kind of layout arrangment.

5.6.3 Capacitor Layout

The capacitors are realized using MIM-CAP in 0.18 μm CMOS technological process from TSMC. The two plates of the capacitors are metal-6 layer and the ctm layer which is in between metal-5 layer and metal-6 layer. Figure5.11 (a) shows the layer structure. The capacitors are done on NWELL with a VDD-ring for shielding to minimize the noise interference from the common substrate. A sample of the capacitor layout view is shown in Figure 5.11 (b).

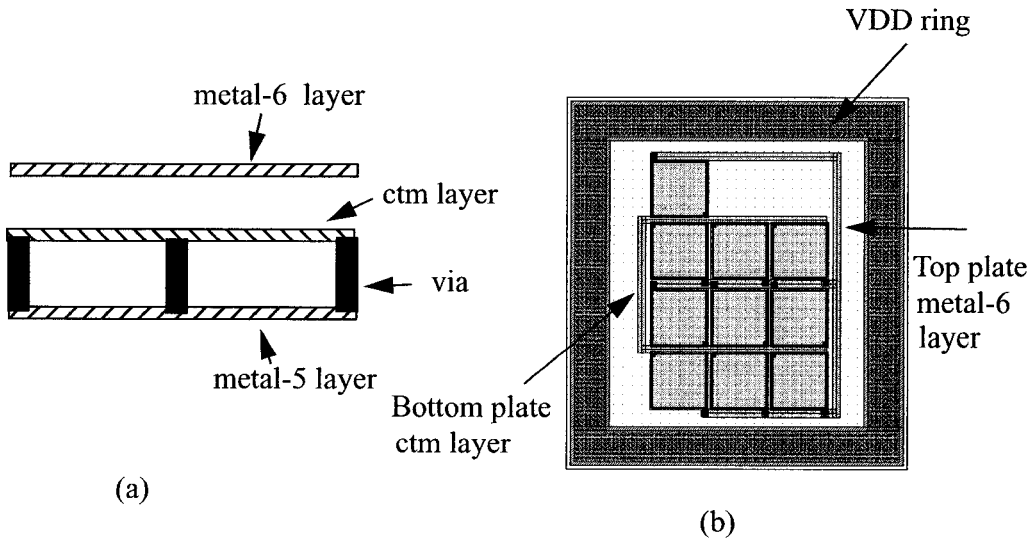


Figure 5.11 (a) ctm layer structure, (b) Capacitor layout diagram

5.6.4 Filter Layout

With above layout techniques, the filter is realized in 0.18 μm CMOS, one-poly-six-metal technological process. The layout diagram of the filter core is shown in Figure 5.12.

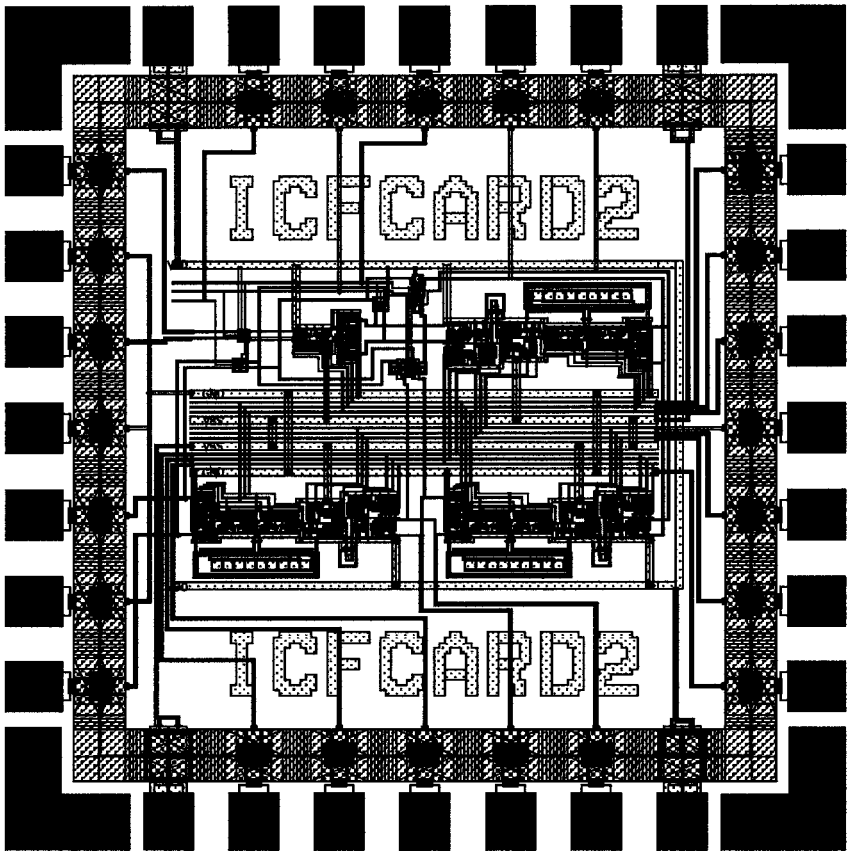


Figure 5.12 The bandpass filter layout view (Area: 1180 x 1180 μm^2)

5.7 Summary

This chapter describes the design of the fully balanced differential wideband PRB filter in 0.18 μm CMOS process technology. Starting from the synthesis of the biquad transfer function and feedback factors, the design precedure and technique are given in details. The design data are tabulated in this chapter as well as the layout view of the designed filter.

Chapter 6

Simulation and Measurement Results

6.1 Introduction

This chapter presents the measurement set-up and results on the fabricated chip which consists of 4 different structured OTA cells and the simulation results on the designed sixth order fully differential wideband filter.

6.2 OTA Chip Measurement Results

Based on the comparison results stated in Chapter 4, four OTA cells are selected to fabricate a chip using 0.35 μm CMOS process technology. The design data are given in following tables. (Note: the common-mode control node is not included in the Martinez's OTA for the chip fabrication)

Table 9: Design data for Assi's OTA

Transistor Size (μm) (W/L)	M_6	10/0.7	M_7	10/0.7
	M_8	10/0.7	M_9	10/0.7
	M_{10}	3.3/0.7	M_{11}	3.3/0.7
Power supply (V)	VDD	1.5	VSS	-1.5
Reference Voltage (V)	Vref	1.2	V_B	0

Table 10: Design data for Nauta's OTA

Transistor Size (μm) (W/L)	M_1/M_3	5/0.7	M_2/M_4	1.35/0.7
	M_5/M_{11}	5/0.7	M_6/M_{12}	1.35/0.75
	M_7/M_9	4.7/0.7	M_8/M_{10}	1.2/0.7
Power supply (V)	VDD	1.5	VSS	-1.5
Reference Voltage (V)	VDD'	1.5		

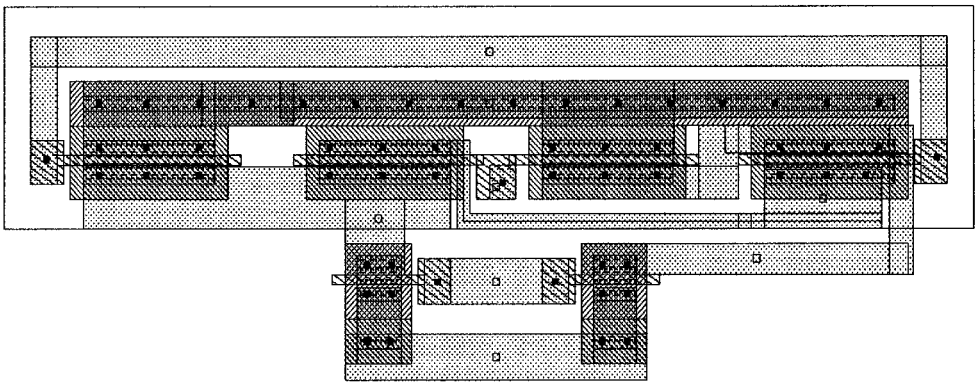
Table 11: Design data for Szcezpanski's OTA

Transistor Size (μm) (W/L)	M_1/M_2	6/0.7	M_3/M_4	6/1.68
	M_5/M_6	6.8/0.7	M_7/M_8	6.8/0.7
	M_9	160/0.7	M_{a1}	3/0.7
	M_{a2}	3/0.7	M_{a3}	60/0.7
	M_{b1}	10/0.7	M_{b2}	1.6/0.7
	M_{b3}	1.6/0.7	M_{b4}	68/0.7
	M_{cf}	1/0.7		
Power supply (V)	VDD	1.5	VSS	-1.5
Reference Voltage (V)	Vbias	-0.7	Vadj	-0.8
	Vcq	0.46		

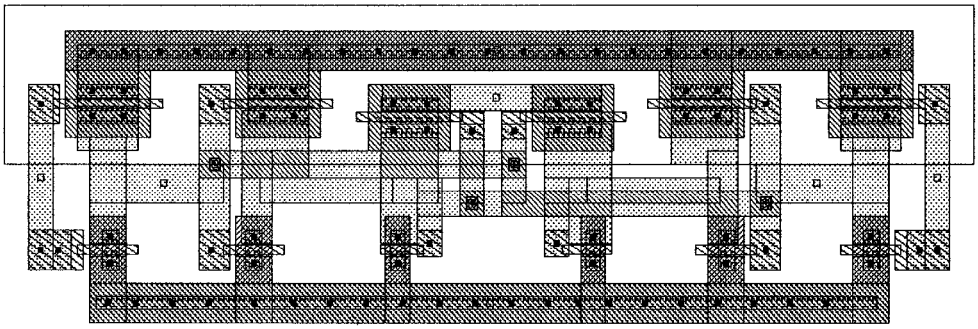
Table 12: Design data for Martinez's OTA

Transistor Size (μm) (W/L)	M_p	56/0.7	M_n	10/0.7
	M_3	3.6/0.7	M_4	17/0.7
	M_5	27.3/0.7	M_6	68.5/0.7
Power supply (V)	VDD	1.5	VSS	-1.5
Reference Voltage (V)	V_p	0.5	V_n	-0.7
	V_{gp}	0	V_{gn}	0

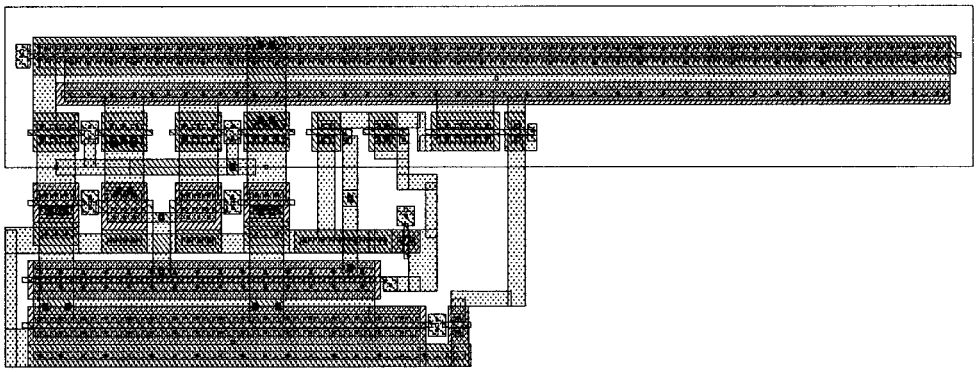
The individual layout views of the four OTA cells are shown in Figure 6.1.



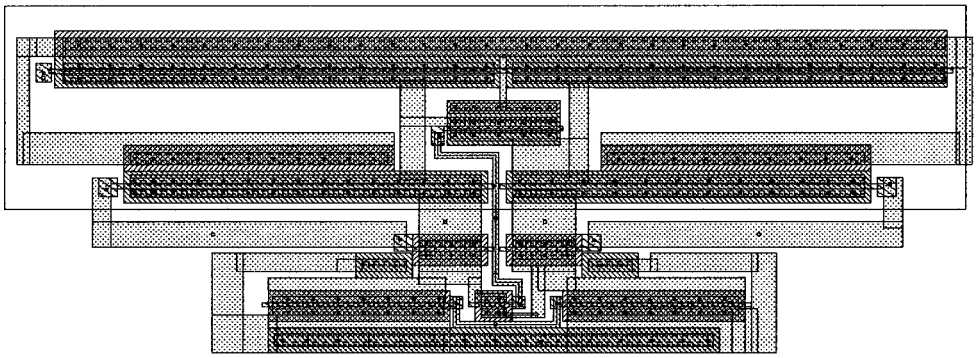
(a)



(b)



(c)



(d)

Figure 6.1 Layout view for (a) Assi' OTA (b) Nauta's OTA
(c) Szczepanski's OTA (d) Martinez's OTA in 0.35 μm technology

When we combined them into one chip for fabrication, to save substrate area, one input pad pair is used for all the input terminals of the four OTA cells, and all the four OTA cells share same VDD and VSS pins. Also, some voltage control terminals are combined together. Thus the whole die area is 1600 x 1750 μm^2 inclusive of the pad frame. The package is selected with 40 pins of DIP (Dual In-line Package). The pin enumeration mapping is shown in Table 13.

Table 13: Pin enumberation of the fabricated chip

Component Name	Node Name	Pin Number	Component Name	Node Name	Pin Number
	VDD	32		VSS	29
	V_{in}^{+}	31		V_{in}^{-}	30
Assi	Vref	21	Nauta	VDD'	1
	GND	22		Out^{-}	2
	Out^{-}	20		Out^{+}	19
	Out^{+}	40	Martinez	Vp	21
Szcezpanski	Vbias	11		Vn	11
	Vadj	10		Vgp	22
	Vcq	3		Vgn	22
	Out^{-}	12		Out^{-}	23
	Out^{+}	9		Out^{+}	39

6.2.1 Measurement Setup

The fabricated chip is measured according to following setup.

6.2.1.1 DC Characteristics

The test bench for DC characteristics measurement is given in Figure 6.2. A sweeping DC voltage is applied to the input terminals of the OTA. The OTA outputs are terminated with 1K resistors to ground, the probes are the voltage meters to detect the out-

put voltage. From the measured the voltage, we can easily derive the output current as

$I = \frac{V}{1k}$.

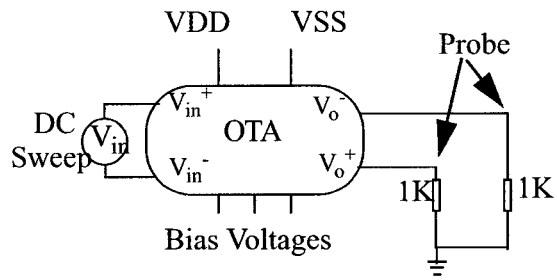


Figure 6.2 Measurement setup for DC characteristics

6.2.1.2 AC Characteristics

The test bench for AC characteristics is similar to that of Figure 6.2, with the change on the input signal, and the probe here is the oscilloscope. Again, we measure the output voltage and covert the voltage signal to its corresponding current represenations.

Due to the lack of high speed analog signal generator with differential outputs, the AC measurement is split into two steps. The first step is to determine the g_m value of the OTA. A set of low frequency differential pulse signals are applied to the differential inputs of the OTA. The output value gives the g_m value of the OTA.

The next step is to measure the frequency dependence of the OTA. A single-ended sinewave signal is applied to one input of the OTA while the another input terminal is shorted to ground. The output is measured in the corresponding output terminal. With the

frequency changing of the input signal, the output amplitude changes are recorded. The measurement is up to 80MHz due to the limitation of the equipment.

6.2.2 Measurement Results and Summary

The DC characteristics measured are shown in Figure 6.3 and Figure 6.4. For comparison purpose, the simulated curves are also included in the same figure respectively in bold lines. (I, II, III, represent the chip numbers)

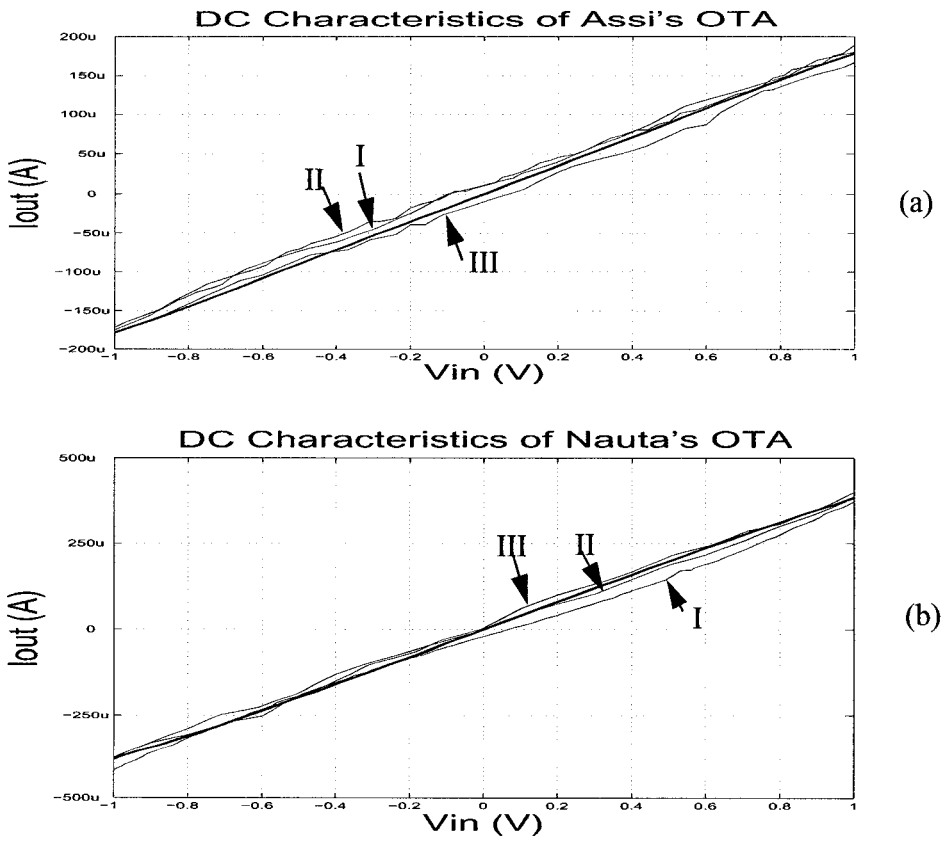
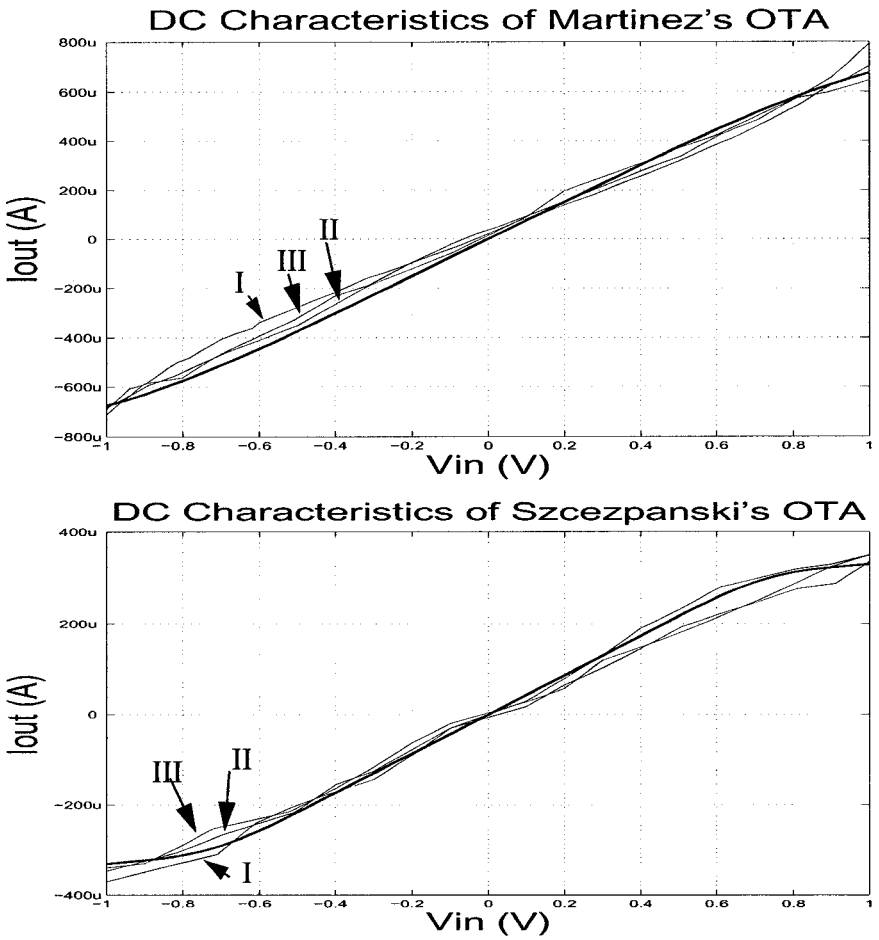


Figure 6.3 DC characteristics of Assi's OTA (a) and Nauta's OTA (b)



(a)

(b)

Figure 6.4 DC characteristics of Martinez's OTA (a) & Szcezpanski's OTA (b)

It can be seen from the test results, due to the variable electrical parameters, the transconductances are not same as those of simulated, but quite close. Also, the characteristics reveal small variations from sample to sample as a result of statistical tolerance which exists in the integrated circuit process technology.

The AC characteristics measured are shown in Figure 6.5. Again, the simulated curves are also illustrated in the same figure respectively for comparison. Since all the

three chips tested showed almost identical AC response, the characteristics of only one sample chip is given in the figures. The bold lines are simulation results.

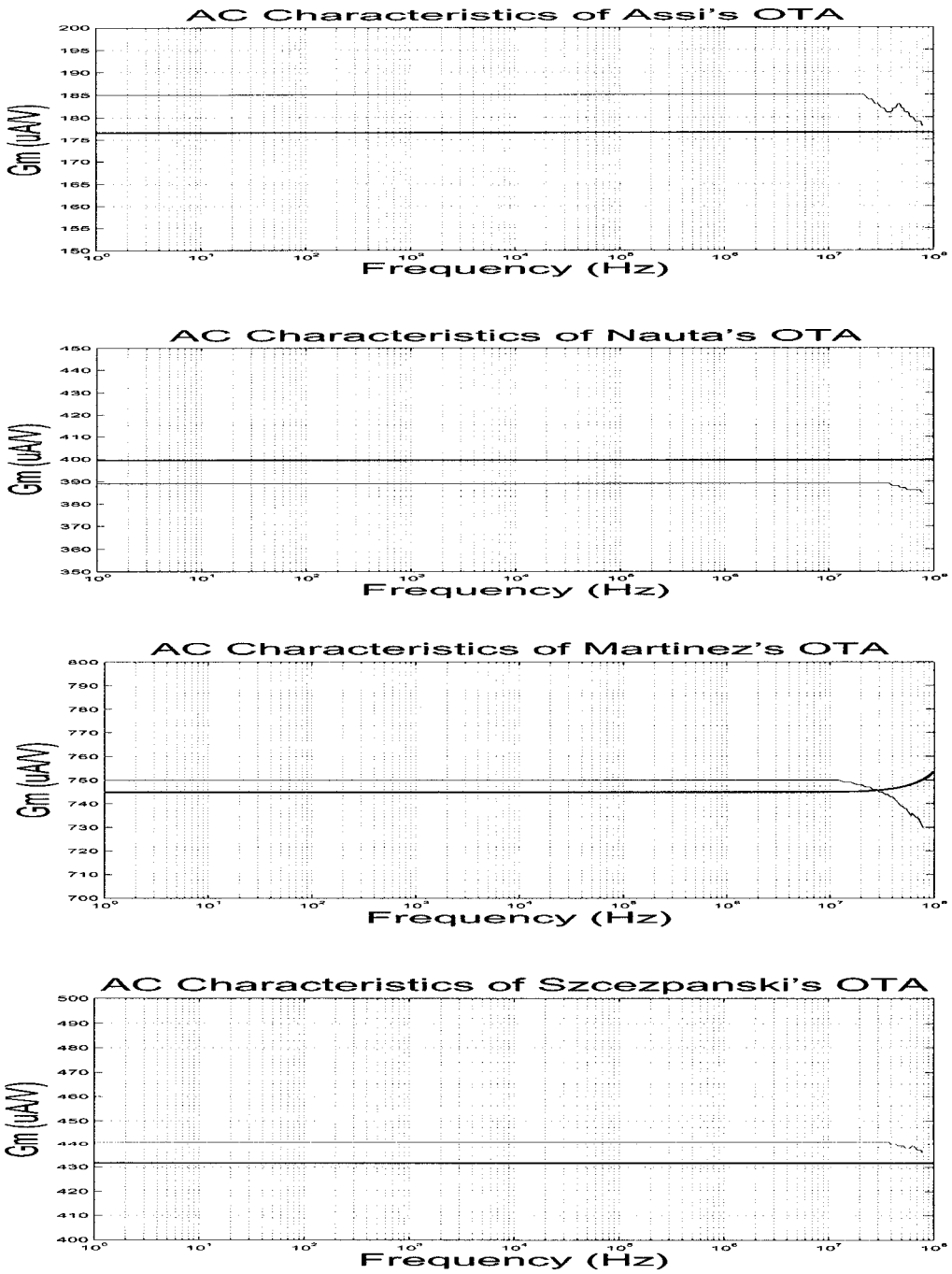


Figure 6.5 AC characteristics of the OTA cells

From the curves, we can seen that the OTA cells have quite good frequency characteristics as shown in the simulation results.

6.3 Filter Simulation Results

Hspice simulation was conducted to verify the design of the filter. The simulation netlist was generated from the layout extraction file with consideration of parasitics.

6.3.1 AC and Transient Characteristics

For a bandpass filter, the magnitude response is the most important characteristic which can be simulated via AC analysis in HSPICE simulation.

The test bench of simulating AC characteristics is built as shown in Figure 6.6. A frequency sweeping signal is connected to the differential input terminals of the filter with 100Mohm dummy resistors to ground. The differential output voltages are connected to an ideal VCVS device to get the single-ended output signal. The frequency sweep is from 100 KHz to 1GHz.

The MOS device models are typical model (TT model) both for NMOS and PMOS in level 49. The temperature is set to 25 ^{o}C.

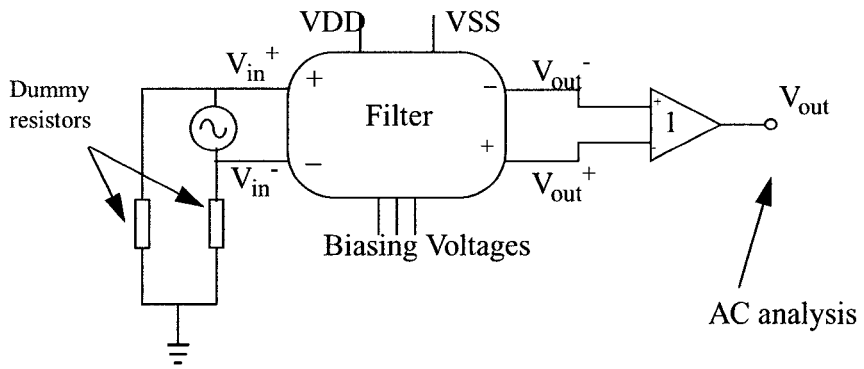


Figure 6.6 Filter AC response simulation test bench

The magnitude and response of the filter under typical condition is shown in Figure 6.7. The center frequency is 28.28 MHz. The passband is from 2 MHz to 400 MHz, with 1 dB ripple.

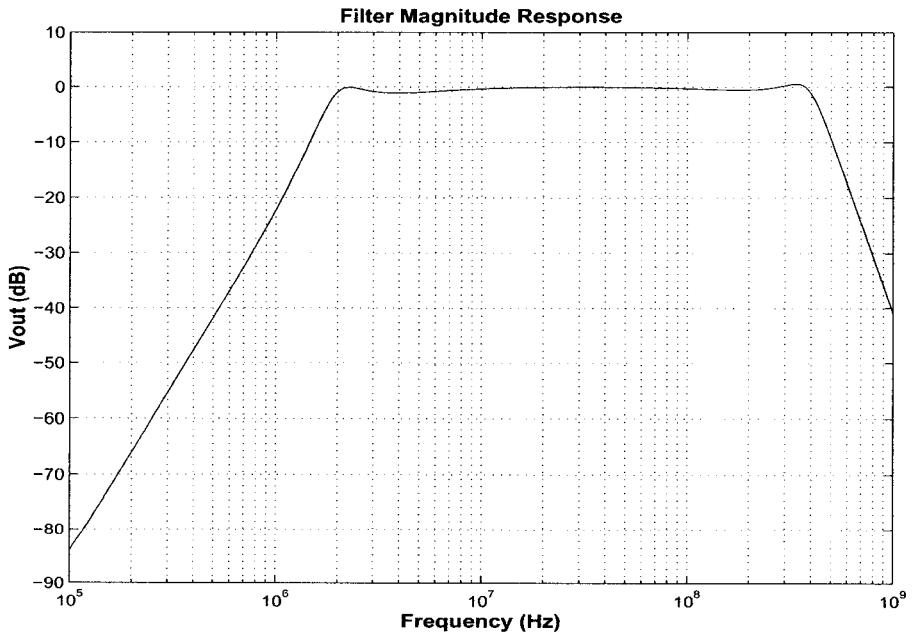


Figure 6.7 (a) Simulation results - magnitude response

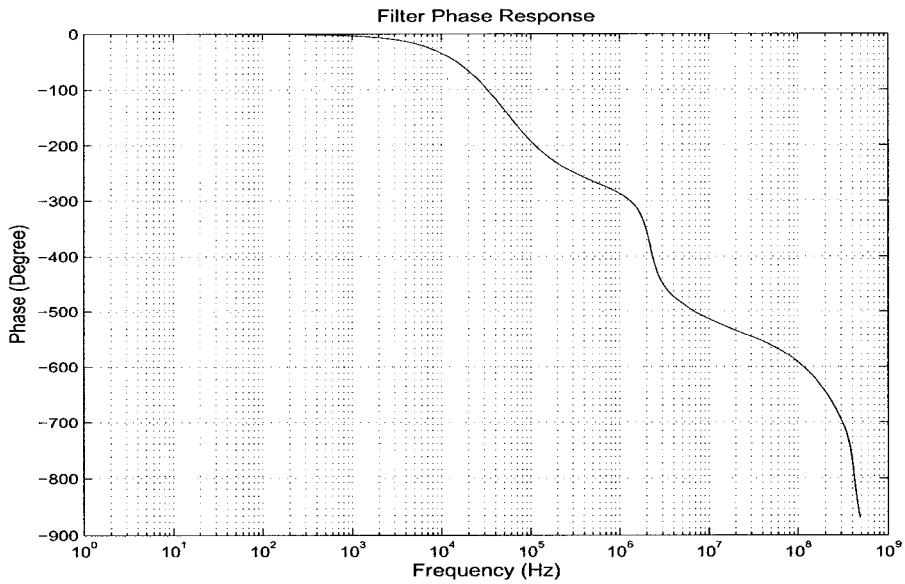


Figure 6.7 (b) Simulation results - phase response

The test bench for transient simulation is similar to that of AC simulation with the only change of the input signal. The input signal for transient simulation is sinusoid with frequency of 100 MHz (in band), 1.5 MHz and 500 MHz (out of the band). Graphical exhibition of the simulation results is given in Figure 6.8. The device model type and temperature setting are same as above. It can be seen from the curves that the transient characteristics of the output voltage are in line with the AC simulation results.

The DC power dissipation simulated is 80.70 mW for the whole circuit.

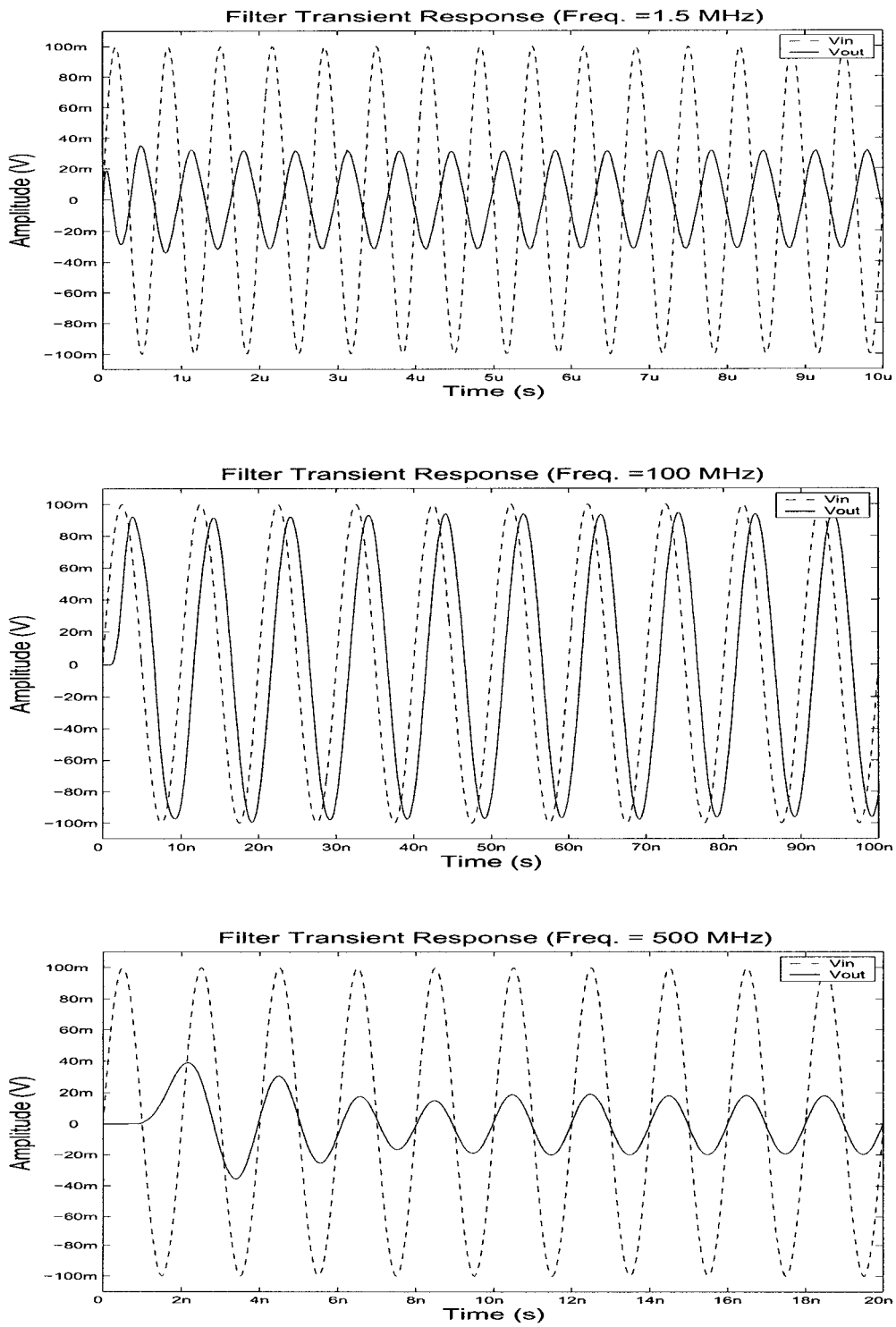


Figure 6.8 Filter transient responses

6.3.2 Dynamic Range

Dynamic range is used to measure the signal-processing capability of an electrical system. Dynamic range is defined as the ratio between the maximum input signal power under certain total harmonic distortions (THD) and the power of the noise floor, normally in decibel, i.e.,

$$DR = 10\log\frac{P_{in}}{P_{noise}} \tag{6.1}$$

If a sinusoidal waveform is applied to a linear system, it is known that the output will also be a sinusoidal waveform at the same frequency, the only changes are possibly magnitude and phase values. However, if the same input is applied to a nonlinear system, the output signal will have frequency components at harmonics of the input waveform, including the fundamental harmonic. The THD of a signal is defined to be the ratio of the total power of the second and higher harmonic components to the power of the fundamental for that signal. In units of dB, THD is found using the following relation:

$$THD = 10\log\left(\frac{V^2{}_{h2} + V^2{}_{h3} + V^2{}_{h4} + \ldots}{V^2{}_f}\right) \tag{6.2}$$

where V_f is the amplitude of the fundamental and V_{hi} is the amplitude of the ith harmonic component.

Sometimes, THD is presented as a percentage value. In this case,

$$THD = \frac{\sqrt{V^2_{h2} + V^2_{h3} + V^2_{h4} + \ldots}}{V_f} \times 100 \tag{6.3}$$

Noise in active devices and passive components is one of the most important factors that determines the performance of low level voltage/current signal processing systems. It represents a lower limit to the size of the electrical signal that can be handled by an integrated circuit without significant deterioration in signal quality.

Noise sources in an integrated circuit can be distinguished as four major categories[28]:

(1) Thermal noise associated with the conducting resistive channel.

(2) Flicker of 1/f noise.

(3) The noise associated with resistive poly-gate.

(4) The noise due to the distributed substrate resistance.

The thermal noise (also called channel thermal noise) of a MOSFET is associated with the conducting resistive channel. The inverse resistive channel is formed by the minority carries in the substrate under the appropriate control of the gate voltage. The noise is generated due to the random motion of free carriers within the channel. To predict the channel thermal noise behavior of MOSFETs with negligible substrate effect, a simple and widely used expression for the mean square value current is given as follows,

$$\bar{I}^2{}_d(f) = 4KT\left(\frac{2}{3}\right)g_m \tag{6.4}$$

where g_m is the transconductance of the MOSFET device, K is the Boltaman constant, and T is the absolute temperature.

The flicker or 1/f noise has been observed in almost all kinds of devices. The mechanism of producing this kind of noise in not quite understood very well so far and intensive research is still on its way. Among all active integrated devices, MOS transistors have the highest 1/f noise of all due to their surface conduction mechanism. The flicker noise is modelled as a voltage source in series with the gate. The mean square value is,

$$\bar{V}^2{}_g(f) = \frac{K}{C_{ox}WLf} \tag{6.5}$$

where K is a constant dependent on device characteristics and can very widely for different devices in the same process, The variables W, L and C_{ox} represent the transistor's width, length and gate oxide capacitance per unit area. The 1/f noise is inversely proportional to the transistor area and typically dominates at low frequencies.

The resistive poly-gate related noise is a layout-oriented noise source [28]. It can be greatly reduced by fingered-layout structure for large W/L ratio transistors. This finger structure divides the total width of a transistor into n poly stripes with an equal width. That is a wider MOS transistor can be replaced by n small parallel connected transistors with equal dimensions. The total output drain noise spectrum due to all the n gates is modelled by [28]:

$$\overline{i}^2_d = 4KT\frac{R_g}{12n^2}g^2_m \tag{6.6}$$

where R_g is the total gate resistance for n gates and g_m is the total transconductance of the MOSFET under consideration.

A lumped resistor R_b will be used to describe the nature of the substrate resistaance. The dominate factor can be viewed as the resistor lumped from the equivalent distributed resistance between the point underneath the channel and the bulk contact on the top of the wafer. If the device layout is a finger structure composed of n poly stripes, the total noise current due to all stripes is given by [28]

$$\overline{i}^2_{dB} = 4kTB\frac{b}{W}g^2_{mb} \tag{6.7}$$

where B is a proportionality constant, g_{mb} is the bulk transconductance, b is the distance between the channel and the substrate pole connecting to the outside. This resistance noise related to the substrate can be minimized by making g_{mb} minimal through smart and careful biasing on the potential difference between the bulk and source terminals.

Compared to the thermal noise and 1/f noise sources of the MOS devices, the later two noise sources are quite small and can be neglected unless under low-noise design requirement.

The total harmonic distortions performance and noise performance of the filter are simulate using HSPICE fourier analysis and noise analysis. Simulation results show that

the THD reaches 1% for a 0.21 V peak sinewave at 100 MHz frequency, and the equivalent input referred noise is around 171.5 nV/rt. Hz in the passband. This corresponds to a dynamic range (with 1% THD) of about 40 dB.

6.3.3. Intermodulation Products

While dynamic range is used to measure the signal handling capability of the a system, the intercept point is used to measure the linearity performance of the system in a straightforward way.

Assume that for a nonlinear system, the response y to an input signal v can be expressed as:

$$y = a_1 v + a_2 v^2 + a_3 v^3 + a_4 v^4 + \ldots \tag{6.8}$$

When the input signal is the sum of two harmonic signals such as:

$$v = e_1 \cos\phi_1 + e_2 \cos\phi_2 \tag{6.9}$$

where $\phi_i = 2\pi f_i t = \omega_i t \qquad i = 1, 2.$

The various frequencies and amplitudes of the output components produced by these input harmonics are:

The linear term is:

$$a_1 v = a_1 e_1 \cos\phi_1 + a_1 e_2 \cos\phi_2 \tag{6.10}$$

The second order term is:

$$\begin{aligned} a_2 v^2 &= a_2 (e_1 \cos\phi_1 + e_2 \cos\phi_2)^2 && (6.11) \\ &= \frac{a_2 e^2{}_1 + a_2 e^2{}_2}{2} && \text{zero-frequency constant terms} \\ &+ \frac{a_2 e^2{}_1}{2}\cos 2\phi_1 + \frac{a_2 e^2{}_2}{2}\cos 2\phi_2 && \text{2nd harmonics} \\ &+ a_2 e_1 e_2 [\cos(\phi_1 + \phi_2) + \cos(\phi_1 - \phi_2)] && \text{second order IM products} \end{aligned}$$

The second order nonlinear term produces, in addition to the constants and 2nd harmonics of both input frequencies, two equal-amplitude components whose frequencies are given by the sum and the difference of the two input frequencies, which are called as second order intermodulation (IM) products.

The third order term is

$$\begin{aligned} a_3 v^3 &= a_3 (e_1 \cos\phi_1 + e_2 \cos\phi_2)^3 && (6.12) \\ &= \frac{3a_3}{2}\left(e_1 e^2{}_2 + \frac{e^3{}_1}{2}\right)\cos\phi_1 + \frac{3a_3}{2}\left(e^2{}_1 e_2 + \frac{e^3{}_2}{2}\right)\cos\phi_2 && \text{fundamentals} \\ &+ \frac{a_3 e^3{}_1}{4}\cos 3\phi_1 + \frac{a_3 e^3{}_2}{4}\cos 3\phi_2 && \text{3rd harmonics} \\ &+ \frac{3a_3 e^2{}_1 e_2}{4}[\cos(2\phi_1 + \phi_2) + \cos(2\phi_1 - \phi_2)] && \text{third order IM products} \\ &+ \frac{3a_3 e_1 e^2{}_2}{4}[\cos(2\phi_2 + \phi_1) + \cos(2\phi_2 - \phi_1)] && \text{third order IM products} \end{aligned}$$

It is seen that the third order nonlinearity produces the 3rd harmonics and the fundamentals of both input frequencies, and the third order IM products, whose frequencies are $2f_1 \pm f_2$ and $2f_2 \pm f_1$.

With similar situation, the other high order terms contain high order harmonics and high order IM products.

Recalled from chapter 3, analog circuits in IC environment are normally built in fully differential structure, which will eliminate the even order nonlinearity. Thus, the third order intermodulation products are used to measure the linearity performance of the analog systems. Also, normally, we only consider the IM products of $2f_1 - f_2$ and $2f_2 - f_1$, since the other two components are far away from the fundamentals.

It is usual to let the amplitudes of the two input harmonics be equal when using them together to test a system for the consequences of its nonlinearity.

Let $e_1 = e_2 = e$, refer to the input resistance R_{in}, the input power of each signal in dBm (the reference being 1mW) becomes

$$\begin{aligned} P_i &= 10\log\frac{P_{in}}{10^{-3}} = 10\log\frac{e^2}{2R_{in}10^{-3}} \\ &= 10\log e^2 - 10\log R_{in} + 27 \quad \text{dBm} \end{aligned} \tag{6.13}$$

The output power of each fundamental component owing to the linear term with refer to output resistance R_L is, in dBm:

$$P_o = 10\log\frac{P_{out}}{10^{-2}} = 10\log\frac{a^2{}_1 e^2}{2R_L 10^{-3}} \tag{6.14}$$

$$= 10\log e^2 + 10\log a^2{}_1 - 10\log R_L + 27$$

The fundamental power gain is $G_p = P_{out}/P_{in}$. When expressed in dB, this becomes

$$G = 10\log G_p = 10\log a^2{}_1 + 10\log R_{in} - 10\log R_L \tag{6.15}$$

Combine Eq. (6.13), (6.14), and (6.15) into

$$P_o = P_i + G \tag{6.16}$$

When we neglect the fifth and higher order terms, the output voltages of the third order IM products are both equal to $3a_3e^3/4$. When expressed in dBm, this becomes:

$$P_3 = 10\log\frac{\left(\frac{3}{4}a_3e^3\right)^2}{2R_L 10^{-3}} \tag{6.17}$$

When combined with Eq. (6.13), this becomes

$$P_3 = 3P_1 - 56.5 + 20\log a_3 + 10\log\frac{R^3{}_{in}}{R_L} \tag{6.18}$$

or

$$P_3 = 3P_i + K \tag{6.19}$$

When plotted on rectangular coordinates, Eq. (6.16) is a straight line whose slope is unity and whose vertical axis intercept is G. Eq. (6.19) is also a straight line with slope of 3 and vertical axis intercept is K.

The point where these two lines intersect is called the third order intercept point. Its location can be specified by its projection IIP onto the P_i axis (i.e., referred to the input), or by its projection OIP onto the P_o axis (i.e., referred to the output).

The intercept point cannot be measured directly because compression, desensitization, and high order IM products destroy the linearity of the lines at the high power levels required. It can be estimated using relatively low input power and the above mentioned effects are neglected.

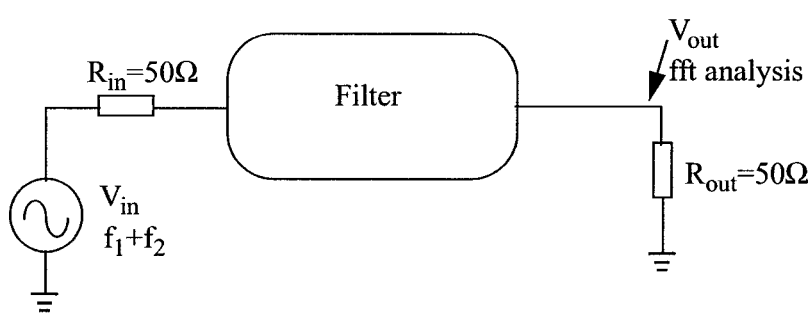


Figure 6.9 Intermodulation products measurement setup

FFT analysis in HSPICE is used to estimate the third order intercept point of the designed filter. The measurement setup is illustrated in Figure 6.9. Two interfering signals of equal amplitudes at 100 MHz and 102 MHz are injected into the filter, and the third

order intermodulation product at 98 MHz is measured at the output. The measurement data is given in Table . The results of simulation are plotted in figure 6.10. The input referred intercept point (IIP3) is around 2.71 dBm (i.e. -27.29 dBW). The simulation is referred ot 50 ohm input and output resistances.

Table 14: FFT measuremnt results

P_{in}(dBm)	P_o(dBm)	P_3(dBm)	G(dBm)	K(dBm)	IIP_3(dBm)
-29.86	-36.32	-101.45	-6.46	-11.87	2.71
-26.43	-32.87	-91.17	-6.44	-11.88	2.72
-23.98	-30.43	-83.80	-6.45	-11.86	2.71
-20.46	-26.92	-73.24	-6.46	-11.86	2.70
-17.96	-24.44	-65.78	-6.48	-11.90	2.71
-16.02	-22.53	-60.03	-6.51	-11.97	2.73
-14.44	-20.97	-55.33	-6.53	-12.01	2.74
-13.10	-19.64	-51.36	-6.54	-12.06	2.76

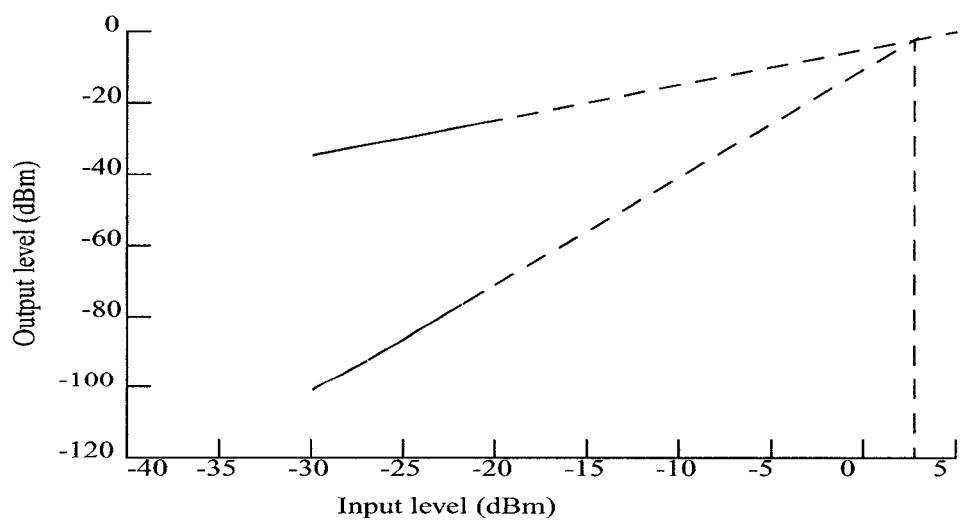


Figure 6.10 IIP_3 plot of the filter

6.3.4 Worst Case Scenarios and Statistical Characteristics

The IC chip fabrication process is a long sequence of chemical reactions that result in device characteristics deviations. These variations can be caused by variations in doping densities, implant doses and variations in the width and thickness of active diffusion and oxides layer and passive conductors [29]. These effects will cause the gate oxide thickness (Tox), channel length and width and threshold voltage of MOSFET variation from its nominal values. Therefore, the MOS transistors are modeled with 'fast' and 'slow' boundary cases to take care of these variations.

Also, the mobility of MOS transistors is temperature dependent. The dependence of MOS transistor drain current was found to be proportional to $T^{-1.5}$ [29]. That is, as the temperature is increased, the drain current is reduced for a given set of operating conditions. Industrially, temperature spread of -30°C to 85°C is to be considered.

To predict the worst case scenarios of the designed filter magnitude responses, the simulation was conducted under following worst cases:

- Fast NMOS, fast PMOS at temperature -30°C
- Slow NMOS, slow PMOS at temperature 85°C

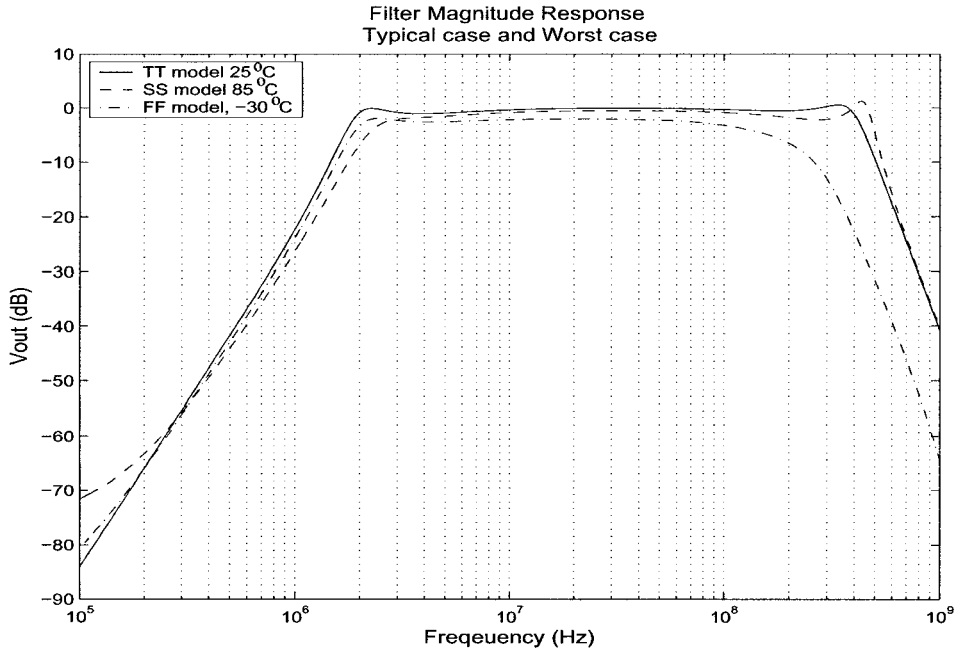


Figure 6.11 Worst case scenarios of filter magnitude response

The simulation results are show in Figure 6.11, with the comparison with Typical NMOS and PMOS at room temperature (25°C) response. Simulation results shows the filter magnitude response variations with respect to the models and temperature changing. In the fast case, the passband ripple is around 1.8 dB, and the bandwidth is around 480 MHz, while in the slow case, the passband ripple degraded to 3.2 dB, and the bandwidth is around 240 MHz.

On the other hand, an electrical system must be designed to lead a maximum process yield. This implies the number of parts (as a percentage) that are within the given specifications. HSPICE can be used to analyze the effects of elements and model parameter variations via Monte-Carlo analysis.

The iteration number (i.e. independent samples) is set to 30; this value is derived based on the fact that the statistical significance of 30 iterations is quite high. It has been shown that if the system operates correctly for all 30 iterations, there is a 99% probability that over 80% of the samples will operate correctly [30]. Here we will consider AC sweep analysis in terms of the statistical variations of the channel length and width, threshold voltages, and the gate oxide thickness of each MOSFET. Each MOSFET is assumed to have a random Gaussian characteristic for the variation of its channel length and width. It is assumed to be 5% of the ±3 sigma level. Similarly, the threshold voltage and the Tox variations are assumed to have the same characteristic. Figure 6.12 shows the Gaussian distribution of process parameters.

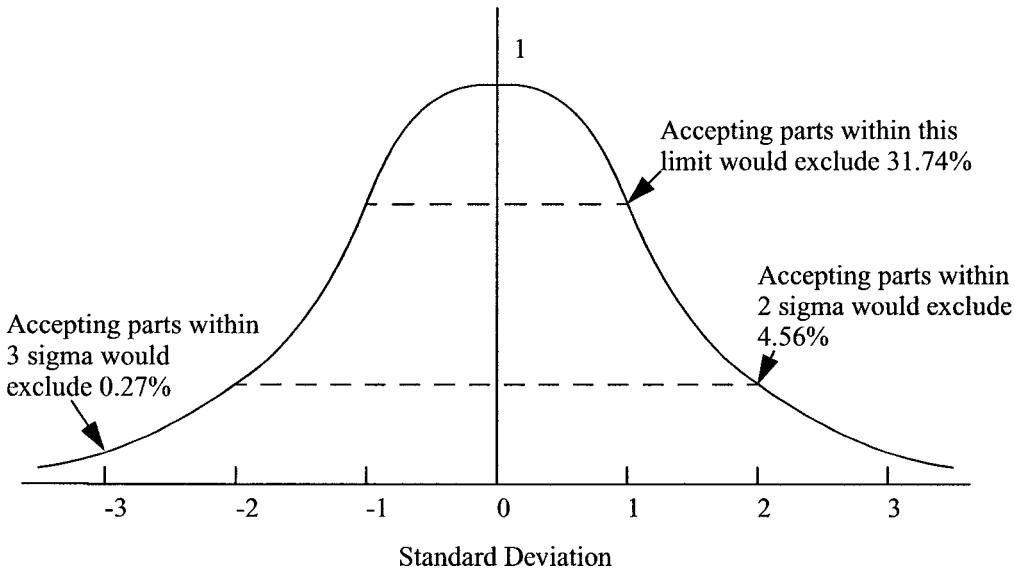


Figure 6.12 The probability density function (PDF) of process parameters

The Monte Carlo simulation results are shown in Figure 6.13. One may find the variations in the frequency response as expected.

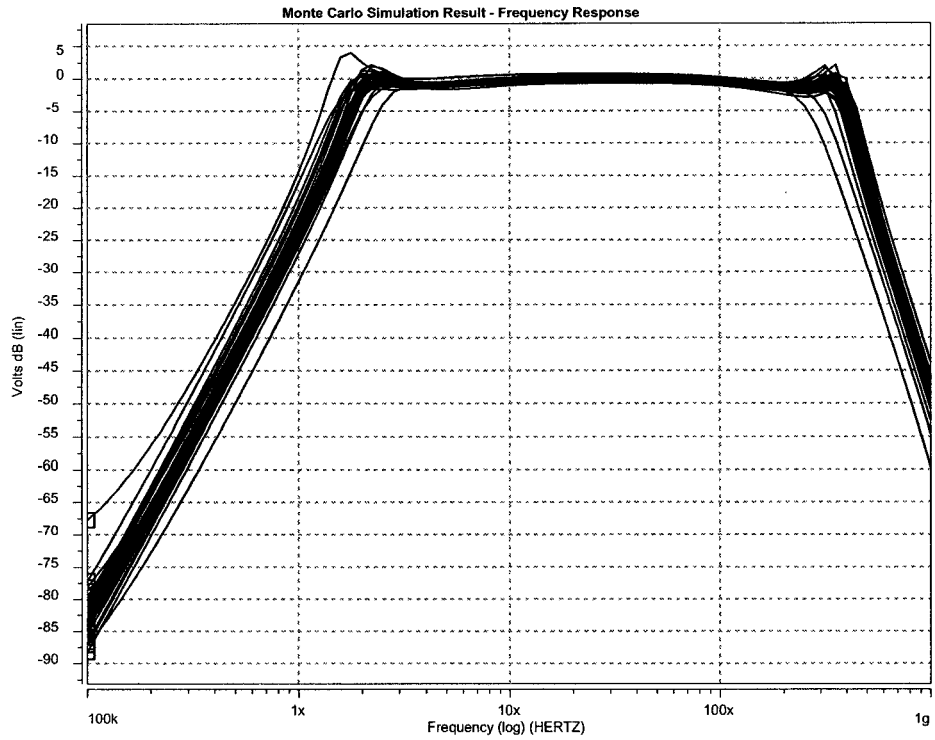


Figure 6.13 Monte Carlo Simulation results

From the simulation results, we can see that, for the most parts of the passband, the ripple is within 1.8 dB. At the low end passband edge the passband edge frequency = 2 MHz, the majority of magnitude attenuation (86.7%) is between -3 dB and +1 dB, 3.3% possibly the loss is larger than 10 dB, and there is a 3.3% possibility, the magnitude has a gain around +2 dB.

As for the high end passband edge, frequency at 400 Hz, the performance has a little bit larger degrade. There are 10% chances the attenuation will be larger than 10 dB, 26.7% chances the loss is less than 3 dB, and 63.3% chances, the attenuation is between 4 dB and 8 dB.

6.3.5 Summary of Simulated Performance

Some important characteristics of the filter are presented in Table 14. The power dissipation is 80.70 mW for the whole circuit. The equivalent input noise is around 171.5 nV/rt.Hz in the passband. The total harmonics distortions reaches 1% for 0.21 V peak sinewave at 100 MHz. This corresponds to a dynamics range (with 1% THD) of about 40 dB. The three order intercept point (IIP3) is around 2.71 dBm (i.e. -27.29 dBW) with reference to 50 ohm input and output resistances.

Table 15: Filter performance

Center Frequency	28.28 MHz
Bandwidth	398 MHz
Pdc	80.70 mW
Gain	1
Noise	171.5 nV/rt Hz
THD (1%, 100 MHz)	0.42 V_{pp}
Linearity IIP_3	2.71 dBm

While attempting to compare the results of the present work with the work of other researchers, we could not find an wideband filter with bandwidth in the range of 400 MHz. Consequently, we collected information for some good bandpass filters that have been reported in the open literature. The key specifications and performances of the filters are tabulated in Table 16, and compared with similar specifications for our filter.

Table 16: Comparison with other similar filters

	Andreani [4]	Elhallabi [5]	Choi [6]	This work
Center Freq.	100 MHz	70 MHz	70 MHz	28.28 MHz
Bandwidth	10 MHz	600 KHz	200 KHz	398 MHz
Order	6	4	6	6
Gain	0 dB	0 - 30 dB	30 dB	0 dB
Pdc	29.5 mW	-	90 mW	80.7 mW
Noise	800 uVrms (B_N = 20M)	19.5 V/rt Hz	81 nV/rt Hz	171.5 nV/rt Hz
Technology	0.6 μm CMOS	0.35 μm CMOS	0.5 μm CMOS	0.18 μm CMOS

It can be seen that our system has lower power consumption per MHz of bandwidth. In noise performance also the system here appears superior to the other works. The work in [4] corresponds to (with BN = 20 MHz) an input referred noise of 178.9 nV/rt. Hz. The work in [6] has a lower input referred noise, but the power consumption is 90 mW with only 200 KHz of bandwidth. The IIP_3 reported in [5] and [6] are -0,25 dBm and -10 dBm respectively, while it is +2.71 dBm in this work. The dynamic range of the filter compares well with the 38 dB dynamic range reported in [4].

6.4 Summary

In this chapter, the measurement results on the fabricated chip that contains 4 different structured OTA cells and simulation results on the designed filter are presented.

The measurements are conducted for the DC and AC characteristics of the OTA cells. The results show that the performance of the fabricated OTA cells are very close to the simulation results.

The performance of the designed sixth order wideband OTA-C filter is verified using HSPICE simulation. Simulation results show that the magnitude response of the filter meets the specifications exactly. The filter performance deviations due to the temperature changes and process variations are estimated. Monte-Carlo simulation is also conducted to predict the yields.

This work is compared with other similar works reported in literature. The comparison shows that our system has better linearity performance, lower power consumption and competitive noise performance in term of bandwidth.

Chapter 7

Conclusion

This chapter summarizes the key contributions in the design of highly linear, wide-band OTA-C filter and gives the recommendations for future work.

7.1 Conclusion

The key contributions of this project are claimed as follows.

•Three existing high order filter architecture: the cascade approach, the multiple-loop feedback approach, and the ladder simulation approach were studied. The main advantages and disadvantages in terms of sensitivity performance and hardware realization complexity were reviewed. This justified our selection of primary resonator block techniques as the architecture of this work.

•Studied several existing OTA cells selected from the literature. Based on the comparison of the g_m value, bandwidth, output resistance and dynamic range in terms of DC power dissipation and substrate area requirement for these selected OTA cells, we selected the optimum one as the OTA cell to implement the wideband filter.

•Designed a full differential wideband OTA-C filter using the selected optimum OTA cell in primary resonator techniques. The filter is implemented using 0.18 μm CMOS technological process. HSPICE simulation verifies the design. Simulation results show that the filter consumes 80.70 mW of power with supply voltages of ±1.5 V. The dynamic range for 1% THD with 0.42 V (peak-to-peak) at 100 MHz is close to 40 dB and the third order intermodulation intercept (IIP_3) is -27.29 dBW (i.e., 2.71 dBm).

•This project demonstrated the feasibility of implementation of highly linear, high frequency, wide band continuous time filter in monolithic environment.

7.2 Future Work

When possible, the filter is to be fabricated and tested to verify the design.

As the worst case scenarios simulation and statistical simulation indicate, the filter performances deviate from the nominal design values when considering the effects of fabrication tolerances, environmental effects such as temperature and humidity variations, and chemical changes that occur as the circuit ages. Due to the overall effects of tolerances, the OTA transconductance values and capacitance values change. Thus, the tuning

circuitry is needed to modify transconductance and/or capacitance values such that the overall filter performances remain stable when fabrication tolerances, and environmental effects are encountered.

With the available of the filter with such a wide bandwidth, another interesting work is to adapt the design to realize a filter with programmable bandwidth and center frequency. In wideband multi-channel communication system, it is necessary to have available a band of high frequency filters with preset bandwidths and center frequencies, which can be switched on to the system on demand.

References

[1] R. Schaumann, M. S. Ghausi, and K. R. Laker, "Design of Analog Filters: Passive, Active RC, and Switched Capacitor," Prentice Hall, 1990

[2] K. Bult, H. Wallinga, "A CMOS Analog Continuous-Time Delay Line with Adaptive Delay-time Control," IEEE J. Solid-State Circuits, Vol. 23, pp759-766, Jun. 1988

[3] C. S. Park, R. Schaumann, "Design of a 4-MHz Analog Integrated CMOS Transconductance-C Bandpass Filter," IEEE J. of Solid-State Circuits, Vol. 23, No. 4, Aug. 1988

[4] P. Andreani, S. Mattisson, "A 100 MHz CMOS g_m-C Bandpass Filter," In Proceedings of ESSCIRC'99, pp. 374-377, Sept. 1999

[5] H. Elhallabi, M. Sawan, "High Frequency and High Q CMOS GM-C Bandpass Filter With Automatic On-Chip Tuning," Microelectronics, 2001, ICM 2001 Proceedings. The 13th International Conference on, 2001, pp. 169-172.

[6] Y.W. Choi, H. C. Luong, "A High-Q and Wide-Dynamic-Range 70-MHz CMOS Bandpass Filter for Wireless Receivers," IEEE Trans. on Circuits and Systems II, Vol. 48, No. 5, pp. 433-440, May 2001

[7] R. Raut, "Modern Filter Design Course Notes," Concordia University

[8] M. S. Ghausi, and K. R. Laker, "Modern Filter Design," Prentice-Hall, 1981

[9] K. R. Laker, R. Schaumann, and M.S. Ghausi, "Multiple-Loop Feedback Topologies for the Design of Low-Sensitivity Active Filters", IEEE Trans. Circuit and System, Vol. CAS. 26, pp. 1-21, Jan. 1979

[10] H. J. Orchard, "Loss Sensitivities in singly and doubly terminated filters,", IEEE Trans. on Circuits and Systems, Vol. CAS-26, pp. 293-297, May 197

[11] G. Hurtig III, "The Primary Resonator Block Technique for Filter Synthesis", Proc. Int. Filter Symp., 1972, 84.

[12] E. Sanchez-Sinencio and J. Silva-Martinez, "CMOS Transconductance Amplifiers, Architectures and Active Filters: A Tutorial," IEE Proc. -Circuits Devices Syst., Vol. 147, No. 1, pp. 3 -12, Feb. 2000

[13] C. F. Wheatley and H. A. Wittlinge, "OTA obsoletes OP. AMP," Proceedings of Nat. Econ. Conference I, pp 152-157, 1969.

[14] R. Raut, "A CMOS building block for analog VLSI systems", Int. J. Electronics, Vol. 8, No. 1, pp. 77-98, 1996

[15] R. Raut, "Wideband CMOS Transconductor for Analog VLSI System", IEEE Trans. on Circuits and Systems II, Vol. 43, No. 11, pp. 775-776, Nov. 1996

[16] N. Guo and R. Raut, "Optimizing CMOS Transconductor-C Filters for Low Power Wide Band Operation", Analog Integrated Circuit and Signal Processing, Vol. 28, No. 1, pp. 107-114, July 2001.

[17] A. Assi, M. Sawan and R. Raut, "A New VCT for Analog IC Applications", The Eighth International Conference on Microelectronics, Cairo, pp. 169-172, Dec. 1996

[18] B. Nauta, "A CMOS Transconductance-C Filter Technique for Very High Frequencies", IEEE J. Solid-State Circuits, Vol. 27, No. 2, pp. 142-153, Feb. 1992

[19] S. Szcezpanski, J. Jakusz, and R. Schaumann, "A Linear Fully Balanced CMOS OTA for VHF Filtering Applications", IEEE Trans. on Circuits and Systems II, Vol. 44, pp. 174-187, Mar. 1997

[20] J.-C. Voghell, M. Sawan, "Current tunable CMOS transconductor for filtering applications", Circuits and Systems, 2000, Proceedings, ISCAS 2000 Geneva, The 2000 IEEE International Symposium on, Vol. 5, pp. 165-168, 2000

[21] A. Lopez-Martinez, R. Antonio-Chavez, "A Full CMOS 150 MHz OTA-C 7th Order Linear Phase Filter", Low Power/Low Voltage Mixed-Signal Circuits and Systems, 2001, Proceedings of the IEEE 2nd Dallas CAD Workshop on, pp. 11-14, 2001

[22] S. Koziel, S. Szcezpanski, "Design of Highly Linear Tunable CMOS OTA for Continuous-Time Filters", IEEE Trans. on Circuits and Systems II, Vol. 49, No. 2, pp. 110-122, Feb. 2002

[23] K. Manetakis, C. Toumazou, "A New High-Frequency Very Low Output-Impedance CMOS Buffer", IEEE International Symposium on Circuits and Systems, Vol. 1, pp. 12-15, May 1996

[24] M. C. H. Cheng and C. Toumazou, "3V MOS Current Converyor Cell for VLSI Technology," Electronic Letters, Vol. 29, No. 3, 4th Feb. 1993

[25] Z. Czarnul, "Modification of the Banu-Tsividis continuous-Tine Integrator Structure", IEEE Trans. on Circuits and Systems, Vol. 33, pp. 714-716, Jul. 1986

[26] D. Johns, K. Martin, "Analog Integrated Circuit Design," John Wiley & Sons, Inc., 1997

[27] F. Maloberti, "Layout of Analog and Mixed Analog-Digital Circuits," in Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing, ed. J. Franca and Y. Tsividis. Prentice Hall, 1994.

[28] Z. Y. Chang and W. M. C. Sansen, "Low-noise wideband amplifiers in bipolar and CMOS technology," Kluwer Academic Publishers, 1991

[29] N. H. E. Weste, K. Eshraghian, "Principles of CMOS VLSI Desing", Addison-Wesley, 1993

[30] Meta-Software, HSPICE User's Manual, Vol. 3, Chapter 7, 1992

Appendix: Published Paper

R. Li and R. Raut, "A Very Wideband OTA-C Filter in CMOS VLSI Technology", 7th World Multiconference on Systemics, Cyberetics and Informatics, Orland, USA, July, 2003

A Very Wideband OTA-C Filter in CMOS VLSI Technology

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ABSTRACT

This paper describes the design of a fully differential, highly linear, very wide band OTA-C filter implemented using a modern 0.18 μm CMOS technological process. The filter is a sixth order Chebyshev bandpass filter with passband from 2 MHz to 400 MHz and 1 dB ripple in the passband. The filter consumes 80.70 mW of power with supply voltages of ±1.5 V. The dynamic rage is close to 40 dB and the third order intermodulation intercept (IIP_3) is -27.29 dBW (i.e., 2.71 dBm). This filter could be used as a wideband vestigial sideband filter.

I. INTRODUCTION

Wideband analog signal processing systems find applications in telecommunication, multimedia and consumer electronics [1]. An electronic filter is an important subsystem in such systems. For example, wideband high frequency integrated bandpass filters are an important building block for the implementation of integrated front-end receivers for emerging new generation of communication system. In integrated circuict technology Operational Transconductor Amplifier (OTA) cells are extensively used in the design continuous-time wideband filters [2]. In this paper we present a very wideband filter realized using OTA cells in a modern CMOS VLSI technology. The filter is of sixth order consisting of three second order OTA-C filter sections connected in multiple feedback topology [3].

In section II we present a comparison among several candidate OTA networks before selecting an optimum device used for implementing the filter. Section III presents the architecture of the filter with some details related to the design of the filter. Simulation results for several important characteristics of the filter are presented in Section IV, followed by the conclusion in Section V.

II. SELECTION OF THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

In recent years, OTA, as voltage to current transducer (VCT), has received considerable attention due to its usefulness and versatility in many filtering and signal processing applications[4]. Many efforts have been put by researchers to improve the OTA performances in term of bandwidth [5], linearity, power dissipation [6], and so on. Table 1 presents a comparison among several such wideband OTA reported in the open literarature, in the past decade[5], [7]-[12]. A 0.35 μm CMOS technology has been used to implement these OTAs. The performance parameters compared were the g_m value, bandwidth, output resistance and dynamic range in terms of DC power dissipation and substrate area required. The power supply is only ±1.5 Volts. The last row in the table represents the sum

$$\Sigma_i\left(\frac{gm_i}{P_{dc}}+\frac{bw_i}{P_{dc}}+\frac{dr_i}{P_{dc}}+\frac{R_{oi}}{P_{dc}}+\frac{gm_i}{Ar}+\frac{bw_i}{Ar}+\frac{dr_i}{Ar}+\frac{R_{oi}}{Ar}\right)$$

where, i=1,.. 7 for the seven OTA circuits studied. It seems that the OTA reported in [9] will be a good choice for implementing a wideband, and highly linear (i.e., wide dynamic range) system. The salient features of this OTA can be noted as follows.

- Cross-coupled differential pairs input with equivalent floating voltage adjustment.

- Absence of internal nodes, output resistance enhanced by negative resistance load.

- Effect of gate-drain capacitances is cancelled to minimize the excess phase shift.

III. FILTER DESIGN

Figure 1 shows the general structure of FLF topology. In this $T_j(s)$ is a typical second order voltage transfer function realized using a voltage amplifiers, such as operational amplifiers. When all the second order sections (biquads) are identical, the design strategy is known as primary resonator block (PRB) technique [13]. A sixth order fully differential filter using the PRB technique is shown in figure 2. The T(s) blocks will be realized using OTAs. The overall transfer function is given by:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{\alpha T(s)^3}{1 + F_1 T(s) + F_2 T(s)^2 + F_3 T(s)^3} \qquad (1)$$

In accordance with the formulae presented in [3], we can synthesize the specifications of the biquad section and the feedback factors F_1, F_2 and so on. Carrying out the procedure, we arrive at the design specifications as shown in table 2. With reference to figure 2, $\alpha = \frac{R_{F0}}{R_{in}}$, $F_i = \frac{R_{F0}}{R_{Fi}}$ $(i = 1, 2, 3)$. ω_p, Q_p and H_0 are the center frequency, quality factor and magnitude at the center frequency, of a standard second order bandpass filter transfer function .

Figure 3 depicts the fully differential second order bandpass filter using four OTAs [2]. The ideal transfer function is given by

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{s g_{mo} C_2}{s^2 C_1 C_2 + s g_{m3} C_2 + g_{m1} g_{m2}} \qquad (5)$$

The center frequency is $\omega_p = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}$, the quality factor is $Q_p = \frac{1}{g_{m3}}\sqrt{\frac{g_{m1} g_{m2} C_1}{C_2}}$ and the magnitude at the center frequency is $H_0 = \frac{g_{m0}}{g_{m3}}$.

By using the data in table 2, we have derived the component values required for implementing the second order sections. These are presented in table 3.

The principle used in relation with figure 2 assumes that the biquadratic blocks T(s) will be implemented by VCVS elements(i.e. op-amp). Since our building blocks are OTA based biquads, we used a low output impedance buffer at the end of each OTA-based biquad section. Figure 4 shows an wideband buffer circuit [14].

The summing OP_AMP at the input of the FLF system has been constructed by an OTA followed by a buffer. A small capacitor is connected in parallel with the input resistor to compensate for the loss of gain of the op-amp at high frequency [2]. The arrangement is shown in figure 5.

The resistors in figure 2 are in fully differential structure. These have been realized using MOS devices working in linear region in differential configuration [15].

The filter has ben implemented using a 0.18 micron CMOS process. Table 4 presents the sizes of the MOS transistors used in implementing the OTAs, the wiseband buffer and the floating resistor systems. The layout diagram of the filter core is shown in figure 6.

IV. SIMULATION RESULTS

The magnitude response of the filter is shown in figure 7. The center frequency is 28.28 MHz. The passband is from 2 MHz to 400 MHz, with 1 dB ripple. The power supply employed is ±1.5 V.

Some important characteristics of the filter is presented and compared with similar work that have been reported in the open literature[16]-[18]. Table 5 shows the results. The total harmonic distortions reaches 1% for a 0. 21 V peak sinewave at 100MHz. This corresponds to a dynamic range (with 1% THD) of about 40dB. The third order intercept has been determined by using two interfering signals of equal amplitudes at 100 MHz and 102 MHz and by monitoring the intermodulation product at 98 MHz. The results of simulation are plotted in figure 8. The intercept point (IIP_3) is around 2.71 dBm (i.e., -27.29 dBW). The simulation is referred to 50 ohms input and output resistances.

V. CONCLUSION

A fully differential, very wideband and highly linear, sixth order, OTA-C Chebyshev band-pass filter design has been presented. The filter consumes lower power (per Hz of bandwidth) than similar filters reported in the literature, has substantially wider bandwidth compared with other wide band filters reported so far, and has superior linearity (an IIP_3 of +2.71 dBm).

ACKNOWLEDGEMENTS

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REFERENCES

[1] K.Bult, and H. Wallinga, "A CMOS Analog Continuous-Time Delay Line with Adaptive Delay-time Control," IEEE J. Solid-State Circuits, Vol. 23, pp 759-766, Jun 1988.

[2] R. Schaumann, M.S. Ghausi, and Kenneth R. Laker, "Design of Analog Filters: Passive, Active RC, and Switched Capacitor," Prentice Hall, 1981, ch.6.

[3] K.R. Laker, R. Schaumann, and M.S. Ghausi, "Multiple-Loop Feedback Topologies for the Design of Low-Sensitivity Active Filters,' IEEE Trans. Circuit System, Vol. CAS. 26, pp. 1-21, January 1979.

[4] R. Raut, "A CMOS building block for analog VLSI systems", Int. J. Electronics, Vol.80, No.1, pp.77-98, 1996.

[5] R. Raut, "Wideband CMOS Transconductor for Analog VLSI Systems," IEEE Transactions on Circuits and Systems II, Vol. 43, No. 11, pp. 775-776, Nov. 1996

[6] N.Guo, and R. Raut, "Optimizing CMOS Transcoductor-C Filters for Low Power Wide Band Operation", Analog Integrated Circuit and Signal Processing, Vol.28, No.1, pp.107-114, July 2001.

[7] A. Assi, M. Sawan and R. Raut, "A New VCT for Analog IC Applications," The Eighth International Conference on Microelectronics, Cairo, pp. 169-172, Dec. 1996

[8] B. Nauta, "A CMOS Transconductance -C Filter Technique for Very High Frequencies," IEEE Journal of Solid-State Circuits, Vol. 27, No. 2, pp. 142-153, Feb. 1992

[9] S. Szczepanski, J. Jakusz, and R. Schaumann, "A Liner Fully Balanced CMOS OTA for VHF Filtering Applications," IEEE Trans. on Circuits and Systems II, Vol. 44, pp. 174 - 187, Mar. 1997.

[10] J.-C. Voghell, and M. Sawan, "Current tunable CMOS transconductor for filtering applications," Circuits and Systems, 2000, Proceedings, ISCAS 2000 Geneva. The 2000 IEEE International Symposium on, Vol. 5, pp. 165-168, 2000

[11] A. Lopez-Martinez, and R. Antonio-Chavez, "A Full CMOS 150 Mhz OTA-C 7th Order Linear Phase Filter," Low Power/ Low Voltage Mixed-Signal Circuits and Systems, 2001, Proceedings of the IEEE 2nd Dallas CAS Workshop on, pp. 11-14, 2001

[12] S. Koziel, and S. Szczepanski, "Design of Highly Linear Tunable CMOS OTA for Continuous-Time Filters," IEEE Transactions on Circuit and System II, Vol. 49, No. 2, pp. 110 -122, Feb. 2002

[13] G. Hurtig III, "The Primary Resonator Block Technique for Filter Synthesis," Proc. Int. Filter Symp., 1972, 84.

[14] K. Manetakis, and C. Toumazou, "A New High-Frequency Very Low Output-Impedance CMOS Buffer", IEEE International Symposium on Circuits and Systems, Vol. 1, pp. 12 - 15, May 1996

[15] Z. Czarnul, "Modification of the Banu-Tsividis continuous-Time Integrator Structure," IEEE Trans. on Circuits and Systems, Vol. 33, pp. 714-716, July 1986

[16] P. Andreani, and S. Mattisson, "A 100 MHz CMOS g_m-C Bandpass Filter," In Proceedings of ESSCIRC'99, pp. 374-377, Sept. 1999

[17] H. Elhallabi, and M. Sawan, "High Frequency and High Q CMOS GM-C Bandpass Filter With Automatic On-Chip Tuning," Microelectronics, 2001, ICM 2001 Proceedings. The 13th International Conference on, 2001, pp. 169-172.

[18] Y. W. Choi, and H. C. Luong, "A High-Q and Wide-Dynamic-Range 70-MHz CMOS Bandpass Filter for Wireless Receivers," IEEE Transactions on Circuits and Systems II, Vol. 48, No. 5, pp. 433-440, May 2001

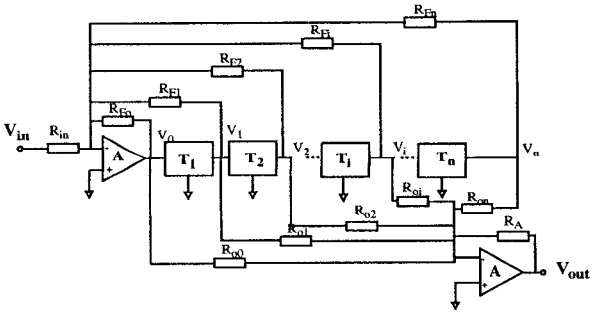

Fig. 1: FLF circuit built from 2nd order sections and feedback network

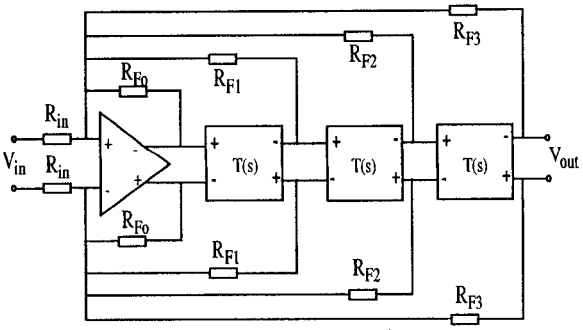

Fig. 2: Sixth order bandpass filter using PRB structure

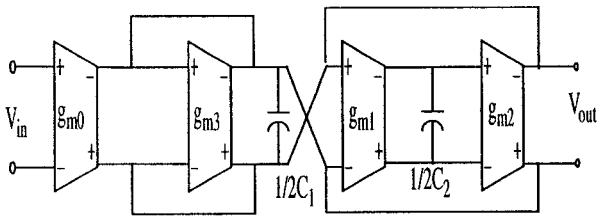

Fig. 3: Fully differential Gm-C biquad

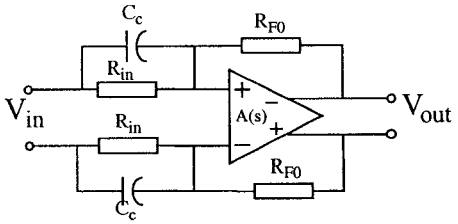

Fig. 5 High frequency compensation circuit

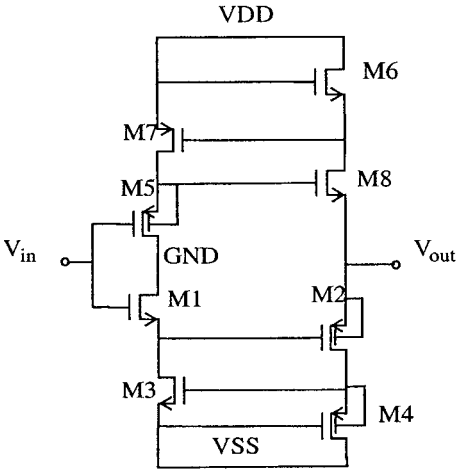

Fig. 4: Wideband buffer circuit

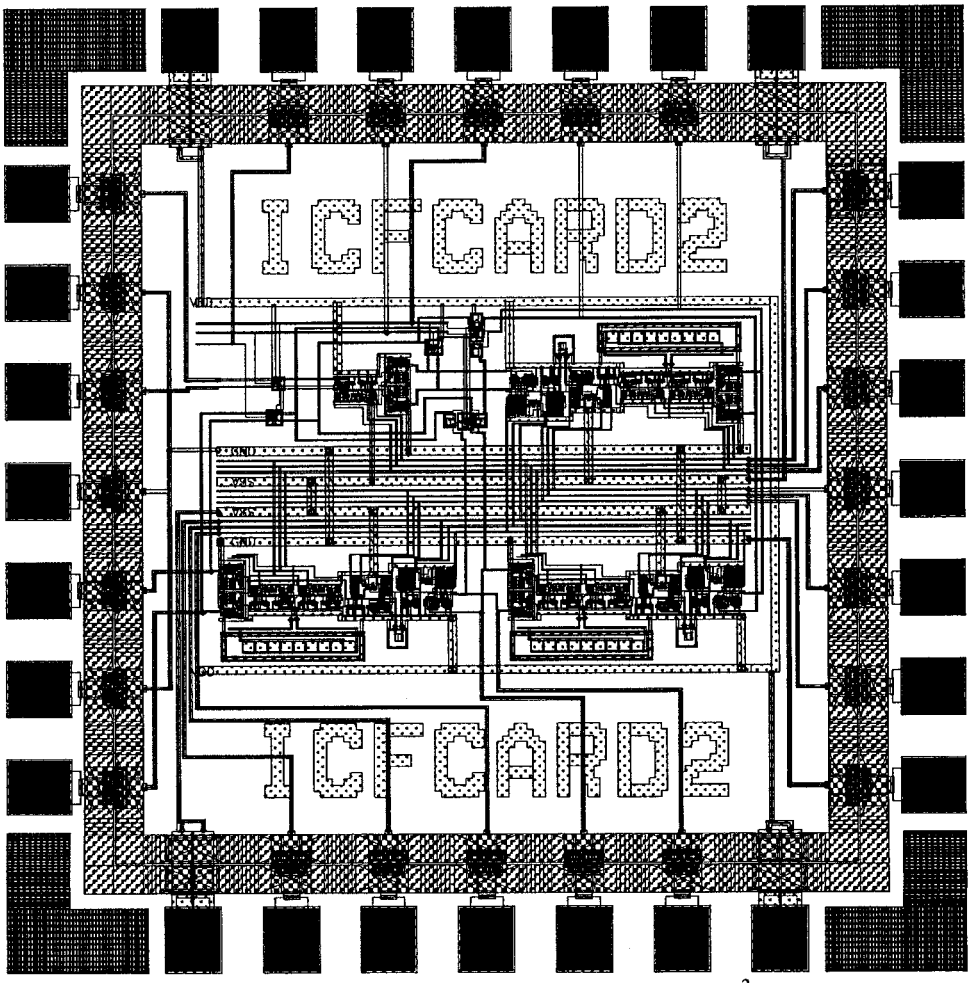

Fig. 6 The bandpass filter layout (Area: 1180 x 1180 μm^2)

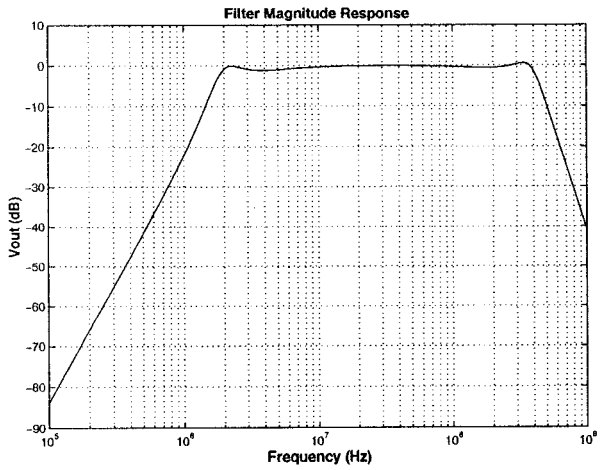

Fig. 7 Filter magnitude response

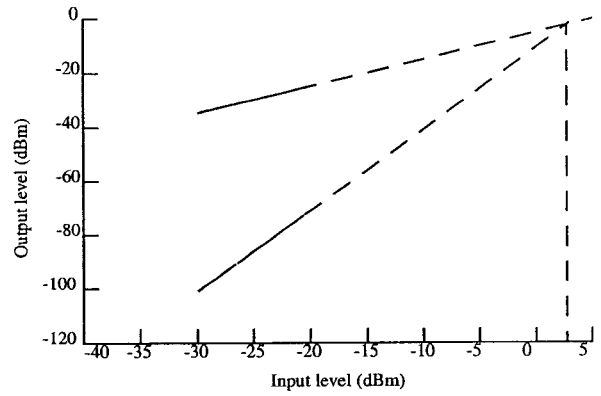

Fig. 8 IIP_3 plot of the filter

Table 1: Comparison results on several OTAs selected from literature

Work by	Assi [7]	Raut [5]	Nauta [8]	Szczepanski [9]	Voghell [10]	Martinez [11]	Koziel [12]
Transconductance (g_m, uA/V)	180.5	117.0	584.6	284.4	80.3	421.5	215.5
Bandwidth (bw, Hz)	10 G	10 G	3 G	10 G	100 M	100 M	100 M
Dynamic Range (dr, dB)	82.8	76.0	90.8	84.0	55.0	88.5	70.6
Output resistance (R_o,ohm)	16.7 K	12.0 K	229.0 M	314.0 M	1.2 M	195.4 K	3.4 M
Power dissipation (Pdc, mW)	4.48	7.48	12.87	4.38	2.50	2.00	5.50
Area (Ar, μm^2)	3.336	3.728	3.488	13.808	10.522	7.388	144.360
Sum performance	0.001	0.0009	8.34	9.44	0.059	0.013	0.064

Table2: Specifications and feedback factors for the biquads

H_0	2.38
Q_p	0.1535
ω_p (M rad/s)	177.715
α	0.367
F_i (i=1,2, 3)	-0.3639, 0.7957, 0.02268

Table 3: Biquad design data

$g_{m1} = g_{m2}$	355.4 uA/V
g_{m3}	1157.8 uA/V
g_{m0}	2755.5 uA/V
C_1	1 pF
C_2	4 pF

Table 4: Transistors aspect ratios (W/L) for the OTA, buffer and the floating resistance

Device	OTA(1)	Buffer	Floating resistance(1)
M1	2.08/0.5	4/0.18	0.8/0.51
M2	2.08/0.5	16/0.18	0.8/0.51
M4	2.08/1.35	2/0.18	0.8/0.51
M4	2.08/1.35	16/0.18	0.8/0.51
M5	3.16/0.6	8/01.8	-
M6	3.16/0.5	20/0.18	-
M7	3.16/0.5	20/0.18	-
M8	3.16/0.5	7/0.18	-
M9	37.19/0.5	-	-
Ma1	0.6/0.5	-	-
Ma2	0.6/0.5	-	-
Ma3	20/0.5	-	-
Mb1	4.5/0.5	-	-
Mb2	0.7/0.5	-	-
Mb3	0.5/1.0	-	-
Mb4	30/0.5	-	-
Mcf	1.1/1.0	-	-

(1) To save space, data for only one OTA, and floating resistance (R_{in}) are given. The actual dimensions of W and L for all transistors are in microns.

Table 5: Filter characteristics and comparison

	Andreani [16]	Elhallabi [17]	Choi [18]	This work
Center Freq.	100 MHz	70 MHz	70 MHz	28.28 MHz
Bandwidth	10 MHz	600 KHz	200 KHz	398 MHz
Order	6	4	6	6
Gain	0 dB	0 - 30 dB	30 dB	0 dB
Pdc	29.5 mW	-	90 mW	80.7 mW
Noise	800 μV_{rms} (B_N=20M)	19.5 μV/rt Hz	81 nV/rt Hz	171.5 nV/rt Hz
Dynamic range	38 dB	-	-	40 dB
Linearity IIP_3	-	-9.25 dBm	-10 dBm	2.71 dBm
Technology	0.6 μm CMOS	0.35 μm CMOS	0.5 μm CMOS	0.18 μm CMOS