An Approach to Design and Implementation of Electrical-Supply-Free VLSI Circuits

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Abstract

In this paper, we propose an approach to design and implementation of VLSI circuits free of electrical supply and power rails. With this approach, the circuits can be made to use the power carried by the incident light for supply, control, and optical charge pumping. The circuits can be fabricated in a standard CMOS technology without additional process. A test circuit involving basic gates and a pulse generator has been designed and fabricated in a 0.18 μm process, and successfully tested.

1 Introduction

The power supply and management has become an obsessive concern in the design and implementation of VLSI circuits with the development of the technology. The objective of this work is to develop VLSI circuits operating without electrical supply, free of power rails, and controlled by the incident light. If it is achieved, the circuits can be made independent of wire connection and battery supply. To this end, using optical power has been taken into consideration.

The circuits dealing with incident power can be divided into two kinds. In the circuits of the first kind, optical power is used, by means of certain devices, such as solar cells, or photovoltaic cells [1] [2], to maintain the level of the supply voltage, and it is not part of the signals determining the state of the output. These devices are usually made of amorphous silicon or III-V element and are not technologically compatible with silicon VLSI circuits. The circuits of the second kind receive optical signals [3], but need electric supply sources. The optical power brought by the incident light is not used to power the circuits.

In this paper, we propose an approach of circuit design and implementation. The principle of the this approach is simply to use the energy carried by the optical input, optical signals or illumination, to support the circuit operation. The description of this work consists of the principle of operation, the physical structure of the basic cell, the schemes of designing VLSI circuits on the basis of the basic cell, and the experimental results.

2 Circuit Description

2.1 Basic Cell

The circuit diagram of the proposed basic cell is illustrated in Fig. 1. The cell consists of a NMOS transistor and a diode D_o, connected between the drain of the transistor and the ground. The output voltage of the cell, V_f, is determined by the input voltage V_x and the incident light Φ_y shining on the area of the diode. The currents flowing through the output node V_f are as shown in Fig. 1. The NMOS transistor current is denoted by i_N and it is controlled by V_x. The diode has two currents, i_Φ and i_{fw}. The former is the photocurrent related to Φ_y, as the area of the diode is open to receive the incident light. The latter is the forward currents of the diode, and it is related to V_f that is the forward voltage of the diode. If $i_N = i_\Phi - i_{fw}$, a charge equilibrium is established and V_f is stabilized, otherwise a charge accumulation would occur.

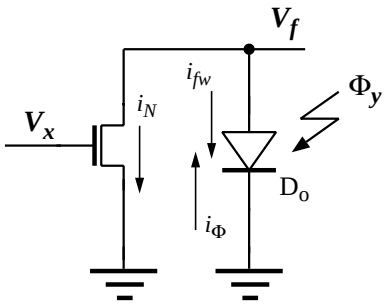

Fig. 1 Circuit diagram of the basic cell. The output voltage level depends on the level of the incident flux and the conductivity of the transistor. The output voltage will be high if $V_x = 0$ and $\Phi_y > 0$. If the inputs V_x and Φ_y, and the output V_f represent logic signals x, y, and f, respectively, this cell will serve as a logic gate performing a logic function $f = \bar{x}\, y$.

If the diode is exposed to the light, $\Phi_y > 0$. The output voltage (V_f) depends on the input voltage V_x, and the cases to be considered are as follows.

1. If V_x is high enough to turn the NMOS transistor on, the transistor and the diode form a closed current path. In this case, the photocurrent i_Φ flows to the ground via the NMOS transistor. As there is no charge accumulation across the junction of the diode, the diode is not significantly forward biased, and there is practically no significant forward current. Let i_{Non} denote the transistor current when V_x is high. We have $V_f \approx 0$, $i_N = i_{Non} \approx i_\Phi$ and $i_\Phi >> i_{fw}$.

2. If V_x is low enough that the conductivity of the transistor is significantly reduced, compared to the first case, its current i_N, denoted now by i_{Noff}, will be significantly smaller than i_Φ. If V_f is initially low, the

forward current i_{fw} will temporally be insignificant. The excess charge, due to the current difference (i_{Φ} - i_{Noff}), is then accumulated across the P-N junction of the diode, making the diode more and more forward biased and increasing the forward current i_{fw}. When the diode is forward biased enough to make $i_{fw} = i_{\Phi} - i_{Noff}$, the charge accumulation stops and V_f is stabilized at the level of this forward voltage.

In case that no optical radiation is incident on the diode, $\Phi_y = 0$, the output V_f will stay at the low level, irrespective of the level of V_x. The cell is, therefore, not activated.

The following issues of the basic cell should be noted:

- The level of the output voltage V_f of the basic cell results from a current comparison involving the transistor current i_N and ($i_{\Phi} - i_{fw}$), the combined currents of the diode. A positive V_f results from a charge accumulation that is caused by a temporal inequality of currents, $(i_{\Phi} - i_{fw}) > i_N$. To make it happen, V_x should be low, i.e.,$V_x = 0$, to make $i_N = i_{Noff}$ and, meanwhile, the diode be illuminated to have a significant i_{Φ}.

- If V_x, Φ_y, and V_f are signals representing binary variables *x*, *y* and *f*, respectively, the logic function $f = \bar{x}\, y$ is performed in this cell. The incident light Φ_y can also be considered as the *enable* signal activating the cell to perform an inversion function.

- The low level of the output voltage, V_{fL}, is approximately 0 V. Its high level, V_{fH}, is determined by the forward current i_{fw} that makes up for the difference ($i_{\Phi} - i_{Noff}$) in order to reach a current equilibrium of $i_{fw} = (i_{\Phi} - i_{Noff})$. For a given i_{Φ}, when $i_{Noff} \approx 0$, i_{fw} gets its maximum value $i_{fw} \approx i_{\Phi}$, and V_f is set at its maximum level. If the incident intensity is very low or the area of the diode D_o is very small, i_{Φ} may be very weak. In this case, the transistor should be in a clean cut-off state to minimize i_{Noff} so that the weak i_{Φ} is still much stronger than i_{Noff} to make a significant ($i_{\Phi} - i_{Noff}$). In such a situation, to reach the current equilibrium, a significant forward current is needed, and thus a significantly positive V_f will be established. A voltage swing of about 400 mV is expected for the input and output voltages under an office-illumination condition.

- The NMOS transistor operates in the subthreshold mode. The characteristic of the current versus the gate-to-source voltage is approximately exponential. If the voltage swing of V_x is 400 mV and the nominal value of the threshold voltage of the transistor is 400 mV or above, the ratio i_{Non} /i_{Noff} will be greater than 10^4, which is sufficient to distinguish the two logic states if the circuit is used for logic operations. Therefore, despite the small voltage swing of V_x, the circuit operation is robust.

- The basic cell does not dissipate any power from electrical sources. The output voltage is "pulled up" by the energy carried by the incident light Φ_y, instead of the electrical supply.

2.2 Voltage Booster and Effective Threshold Voltage

As described in the previous sub-section, the output voltage of the basic cell shown in Fig. 1 is expected to swing between 0 V and 0.4 V. If the threshold voltage of the NMOS transistor is about 0.4 V, the output voltage of such a cell can be directly applied to the MOS gate terminal of another cell of the same structure to switch the transistor from its on-state to its off-state or vise versa. However, depending on the fabrication process, the threshold voltage may be higher, e.g. 0.7 V. With such a higher threshold voltage, if the input voltage still swings between 0 and 0.4 V, the transistor would not be able to have distinct i_{Non} and i_{Noff}, as it can never be turned on. Thus, the threshold voltage needs to be lowered. To this end, a voltage boost module is connected to the gate of the transistor, as shown in Fig. 2. The input voltage V_x is now applied at the negative end of the module to drive the cell. Considering the added voltage of V_{bst}, the transistor can be turned on when $(V_x + V_{bst}) \geq V_{tn}$, i.e., $V_x \geq (V_{tn} - V_{bst})$, as if the effective threshold voltage decremented by V_{bst}. Thus, even if the amplitude of the input voltage V_x is smaller than the nominal threshold voltage of the transistor, the cell can still be driven in operation.

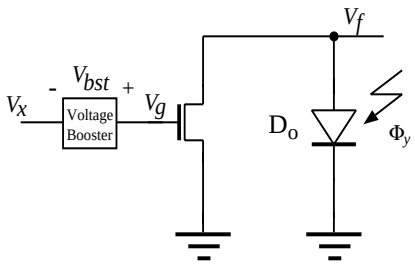

Fig. 2 Voltage booster added to the basic cell to change the threshold voltage of the cell. The transistor can be switched from its on-state to its off-state, or vice versa, if the input voltage V_x swings between 0 and (V_{tn} - V_{bst}), where V_{tn} is the threshold voltage of the NMOS transistor. The threshold voltage of the cell is effectively lowered by V_{bst}, compared to that of the cell shown in Fig. 1.

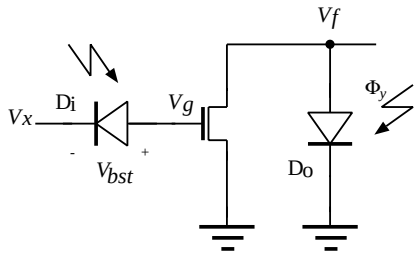

Fig. 3 Practical implementation of the voltage booster using a diode D_i functioning as a photovoltaic device.

Diodes can be used to make a voltage shift [4]. The voltage boost module can be easily implemented by means of a diode acting as a photovoltaic device. As shown in Fig. 3, the diode D_i has its anode connected to the gate of the NMOS transistor and its cathode used as the input node of the cell. When D_i is illuminated, a voltage V_{bst} of 0.3 ~ 0.5V is established. If multiple diodes connected in series to the MOS gate, a larger V_{bst} will be obtained. It should be underlined that, like the logic operation of the cell, this voltage boost is also realized optically without dissipating any power from electrical sources.

The basic cell, with or without the voltage booster, can be easily implemented in a standard CMOS process. Fig. 4 illustrates the physical structure of the cell shown in Fig. 3 using a N-well CMOS technology.

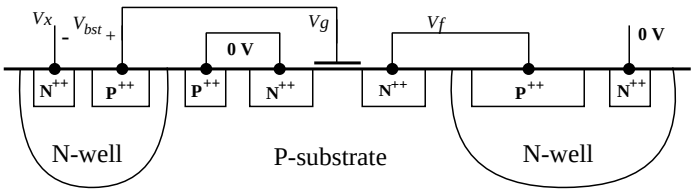

Fig. 4 Cross-section of the structure of the basic cell with a diode for voltage boost at the gate of the MOS transistor.

It should be mentioned that, to implement the voltage boost module, a structure of P-diffusion/N-well/P-substrate is used, as shown in Fig. 4. In addition to the boost diode D_i, a parasitic diode of the N-well/P-

substrate and a parasitic BJT are also formed. This structure features a zero-DC-path at the anode of D_i, or the emitter of the BJT, as the P-diffusion layer is connected to the MOS gate node. With this feature, a charge accumulation will take place across the P-diffusion/N-well junction, if the reverse current is enhanced by the incident photons, and V_{bst}, the forward voltage can be easily established, resulting in a forward currents that can be considered as the emitter current of the parasitic BJT. Also because of the zero-DC-path, the forward current is equal to the reverse one, which makes un charge equilibrium across the junction. The voltage V_{bst} is thus sustained.

If the input voltage of the cell shown in Fig. 4 is positive, the N-well/P-substrate junction is reverse biased. When the forward current mentioned above arrives the N-well region, it will be swept through the junction, becoming the collector current. Meanwhile, there is another current crossing the N-well/P-substrate junction. It is the photocurrent, contributed by the charge converted from incident photons, of the parasitic diode. The input current of the cell is the sum of the reverse current of the boost diode D_i and the photocurrent of the parasitic diode. Both currents are related to the area of the boost diode. If the input V_x is the output of a cell identical to that shown in Fig.4, as long as the diode D_o is much larger than that of D_i, the input current of the succeeding stage would have little effect on the preceding one. In case of two or more voltage boost modules cascaded to achieve a larger boost voltage, the area of the boost diode D_i in the first module should be made about three times larger than that in the second one so that the first module is able to provide a current to the second one while achieving a forward voltage in its D_i.

2.3 Developing Electrical-Supply-Free and Optically-Supplied-Controlled VLSI Circuits

The basic cell presented above is the nucleus of the proposed approach to developing new VLSI circuits. The cell can be used for analog operation as the output signal V_x varies continuously with the input signals V_x and Φ_y. This aspect of the circuit design will be elaborated later in other reports. In this sub-section, the aspect of digital VLSI design is presented.

The concept for the basic cell can be extended for the design of logic blocks and processing circuits. The simplest logic gates to implement using this concept are optically controlled NOR gates. An example of

such gates is illustrated in Fig. 5. Using the postulates and theorems of Boolean Algebra, a logic function can be expressed in OR/NOR forms. Thus, a library of electrical-supply-free logic gates can be created. With these logic gates, new circuits, combinational or sequential, can be easily designed and implemented. It should be noted that each of the logic gates has an optical control input. Therefore, these gates can be activated or inactivated collectively or individually by means of optical signal projection. In particular, some functions, such as signal generation, distribution, and control can be implemented in a very simple manner, and electrical-supply-free and optically-supplied-controlled circuits can be easily developed. Here are some examples.

- Optically controlled signal generation. An odd number of the basic cells makes a ring oscillator, as an example illustrated in Fig. 6. The frequency of the signal can be modulated by the incident intensity.
- Optical system timing and control. As each gate cell of the circuits having an optical *enable* input, the system timing, synchronous or asynchronous control can be realized by simply projecting optical control signal sequences on specific circuit areas. Circuit units for clock distribution or control may not be needed, and some problems, such as clock skew, can be avoided in the new circuits.
- Optical data transmission to a multi-port reception/processing circuit. If different optical signal beams should be received, respectively, by transmission ports, aiming a signal beam at its destination circuit area activates the data reception and processing in the target circuit port. The optical signals can get their respective destinations without electronic addressing and without electrical supply to the ports.

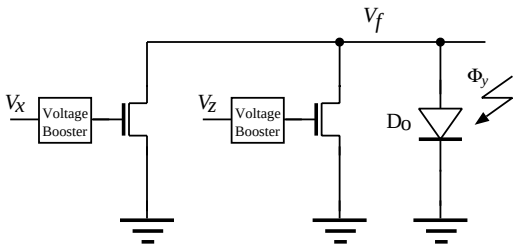

Fig. 5 Gate implementing $f = \overline{x+z} \cdot y$.

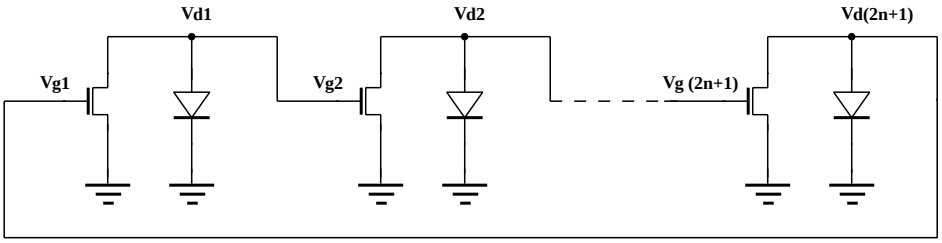

Fig. 6 Example of a ring oscillator implemented with the basic cells.

3 Experimental Results and Analysis

A test circuit, involving a basic cell and a ring oscillator consisting of fifteen cells shown in Fig. 6, as well as some photodiode cells for other designs, has been integrated in a silicon chip fabricated using a 0.18 μm CMOS technology. Fig. 7 shows the die photo of the chip. Several voltage followers have been integrated in the circuit for the observation and measurements of some internal node voltages. The circuit has been tested in two phases, the characterization of the basic cell and the test of the logic gates.

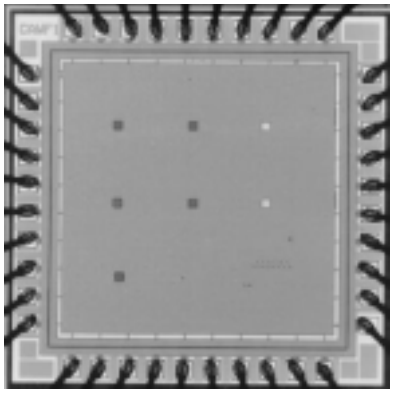

Fig. 7 Die micrograph. The surface of the circuit is covered by a metal layer for light shielding except the areas of the integrated diodes. The units of the basic cell and the ring oscillator described in the paper are placed in the lower-right part of the chip area. The exposed diodes in these units are not visible by naked eyes as each of the cells occupies only a very small space of 4x7 μm^2.

3.1 Characterization of the Basic Cell

The structure of the basic cell tested is shown in Fig. 3, and it occupies a space of 4x7 μm^2, including the two diodes. The first step of the characterization is to measure V_{bst}, the voltage across the diode D_i

connected to the gate of the NMOS transistor, while incrementing the input optical intensity. The results are illustrated in Fig. 8. The diode, used as a photovoltaic device, is able to make a voltage boost by means of the incident optical power. The magnitude of the boost voltage is related to the incident flux. As the anode of the diode is connected to the MOS gate, there is no current flowing in or out of the diode in steady state. Under this condition, an equilibrium of motion of charge should be built inside the diode, i.e., the two currents, that directed by the built-in junction voltage and that by the forward voltage, being equal. A strong radiation results in a strong photocurrent which matches a strong forward current, and, in this case, a strong forward voltage is established. Therefore, when the incident intensity increases, V_{bst}, the forward voltage of the diode is modulated.

The second step of the characterization is to test the "threshold behavior" of the basic cell. In this step, the input voltage is applied at the gate of the NMOS transistor, instead of the cathode of the diode D_i, so that the effect of the voltage shift by D_i is not included.

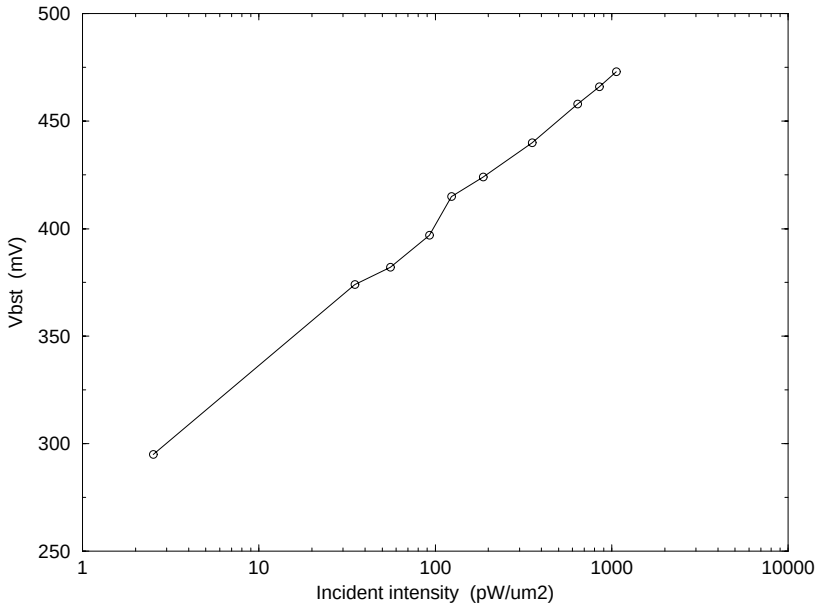

Fig. 8 Voltage across the diode D_i for optical voltage boost versus the incident intensity.

As the logic operation of the cell involves an inversion function, when the input voltage is raised above a threshold level, the output voltage will fall. To investigate this threshold behavior of the cell, two elements need to be taken into consideration. On one hand, the NMOS transistor of the cell operates under the

subthreshold condition, and, on the other hand, the drain of the transistor is connected to the diode D_o that is open to receive the incident light and provides a photocurrent. Moreover, as described in sub-Section 2.1, the level of the output signal is related to a current comparison between the transistor current i_N and the two diode currents combined (i_Φ - i_{fw}). Thus, the threshold voltage of the cell is related to the conductivity of the NMOS transistor with respect to the combined current (i_Φ - i_{fw}) of the diode D_o. If the conductivity of the transistor is strong enough to have its current i_N > (i_Φ - i_{fw}), the charge accumulated in D_o will be removed and the voltage level of V_f will be low. In this case, the transistor is considered in its on-state and the voltage applied at the gate is considered above the threshold voltage of the cell. Therefore, this threshold voltage is defined as the minimum gate voltage required to make the output voltage V_f to change from its high level to its low level under a given illumination condition. The characteristic of the threshold voltage versus the incident intensity is obtained and illustrated in Fig. 9. It shows that the threshold is below 300 mV in the entire range of the optical input signal applied for testing the cell. Also, it suggests that the low level of the gate voltage should be well below 100 mV in order to cut the NMOS transistor off. Furthermore, although this test aims at measuring the threshold voltage of the cell, the results can also be used for analyzing the subthreshold conduction of the transistor.

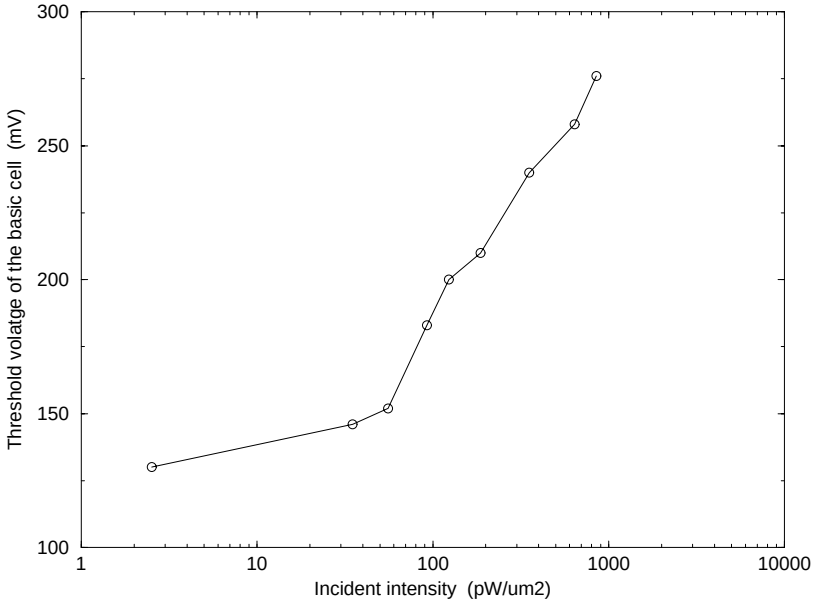

Fig. 9 Threshold voltage of the basic cell versus the incident intensity. This threshold voltage is the minimum gate voltage required to make the output voltage V_f to fall, which implies $i_N \geq (i_\Phi - i_{fw})$, with a given incident intensity.

The characteristic of the magnitude of the output voltage V_f versus the incident intensity is illustrated, together with that of the threshold voltage of the basic cell, in Fig. 10. This curve shows that, when the input voltage V_x is 0 V, the amplitude of the output voltage increases with the incident intensity. The amplitude is about 375 mV under the condition of the weakest illumination (2.5 pW/μm^2) during the chip test, while the threshold voltage of the cell is about 125 mV. The signal V_f has a sufficient voltage swing to make the cell to operate robustly.

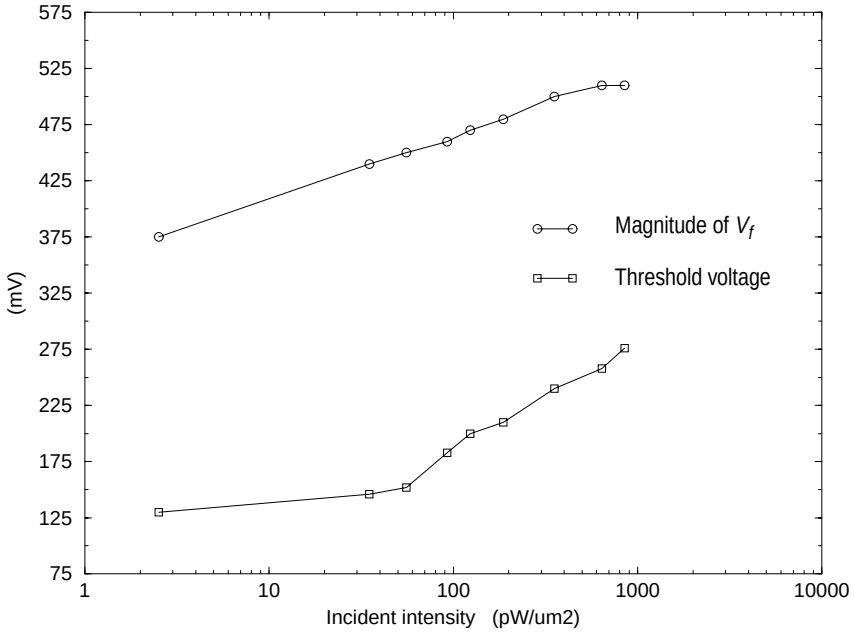

Fig. 10 Amplitude of the output signal V_f versus the incident intensity in comparison with the threshold voltage of the cell. The magnitude of V_f is sufficient to switch the logic state of the cell.

The test results of the device characterization confirm the following points.

- The diode D_o has the capacity of photovoltaic device. When the transistor is turned off and the diode is lit, the output voltage V_f can be “pulled - up” to a level around 400 mV without electrical supply. This magnitude is modified logarithmically by the incident intensity. With the given surface dimension of D_o

and the chosen 0.18 μm fabrication technology, the rate is about 60 mV per decade of intensity change. Hence, if the weakest incident light is 0.25 pW/μm^2 instead of 2.5 pW/μm^2, it can be predicted that the amplitude of the output voltage will still be greater than 300 mV. Thus, the circuit can operate with very weak incident light.

- The threshold voltage of the cell, defined in this sub-section, is always lower than 300 mV, if the transistor is fabricated in the 0.18 μm process employed. The amplitude of the voltage V_f is above 300 mV. Hence, no voltage boosters should be placed if the multiple of cells are cascaded.

- The diode D_i functions as a photovoltaic device to provide a voltage boost V_{bst}. When it is illuminated, the magnitude of V_{bst} is about 300 mV or higher. This additional voltage can be used, if needed, to produce a voltage higher than the high-level of the output voltage of the basic cell. This provides a feasibility of implementing the proposed electrical-supply-free circuits using an available CMOS process without limitation of the threshold voltage of the transistors.

- The surface of the diode D_i is about ten times smaller than that of D_o. However, the magnitude of V_{bst} is only a little smaller than that of V_f (Figs. 8 and 10). Hence, if D_o is made smaller, the magnitude of V_f will be not be reduced significantly. This feature can be used to minimize the area of the circuits. However, it should be underlined that, to minimize the space without reducing the swing of the output voltage, the transistor current during the cut-off periods needs to be reduced, or the level of the incident light needs to be raised.

3.2 Test of the Logic Gate and the Ring Oscillator

In the second phase of the test, the voltage transfer characteristic of the basic cell has been obtained and the function of the ring oscillator has been validated.

The circuit of the basic cell for the test is identical to that shown in Fig. 3. A diode (D_i) is placed in the cell as a voltage booster. A triangle signal is applied at the input terminal of the cell and both the input and output voltages are observed. Fig. 11 shows three waveforms obtained when the incident light intensity is about 2.5 pW/μm^2. When V_x (the triangle waveform) swings linearly between - 0.37 V and 0.1V, the

transistor is turned off and on alternatively, and V_f (the pulse waveform) is switched between two distinctly different levels. The third curve shown in Fig. 11 is the characteristic of V_f versus V_x. This curve is hysteresis-like because it is obtained when V_x changes continuously from the low level to the high level and then changes back to the low level. There is a delay of V_f with respect to V_x.

The basic cells used in the ring oscillator do not have voltage booster at the NMOS gate. As mention in Section 3.1, the amplitude of the output voltage of such a cell is about 400 mV or higher, and the threshold voltage of the transistors integrated in the test circuit is lower than 400 mV, as shown in Fig. 9. Thus, no voltage booster should be placed when the cells are cascaded. The waveforms obtained in the test of the ring oscillator are shown in Fig. 12. The input and output voltages of one of the cells are placed together on the oscilloscope to show their complementarity. The incident light intensity is about 852 W/m^2. As the illumination is stronger than that in the case described in the preceding paragraph, the charge flow in the diode is stronger, the time required for the output voltage to change from one level to the other is shorter, thus the “hysteresis” in the curve of the output voltage versus the input one is much less visible. It has been confirmed that the frequency of the oscillation is determined by the incident intensity.

The results of the test of the second phase are coherent with those of the first phase described in sub-Section 3.1. All of them are in a good agreement on the analysis presented in Section 2.

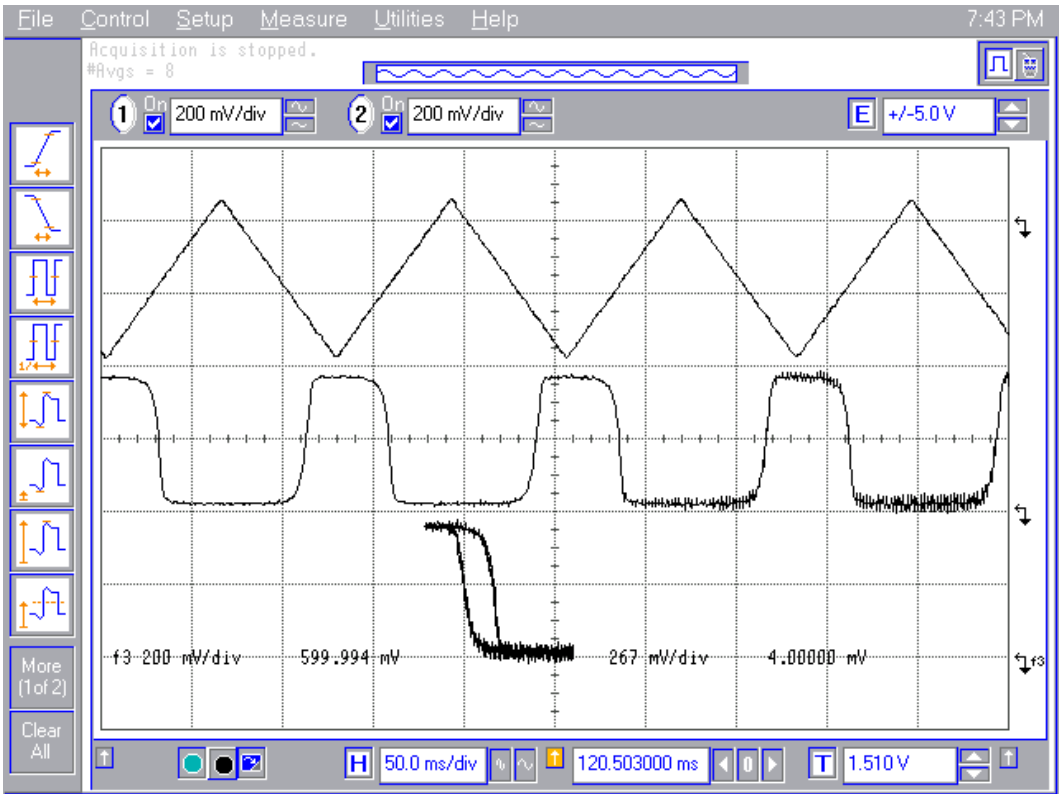

Fig. 11 Test waveforms of the logic cell shown in Fig. 3. The incident light intensity is about 2.5 W/m^2. On the screen there are three waveforms: that on the top is the input V_x, in the middle is the output V_f and the other is the curve of V_f versus V_x when V_x varies continuously.

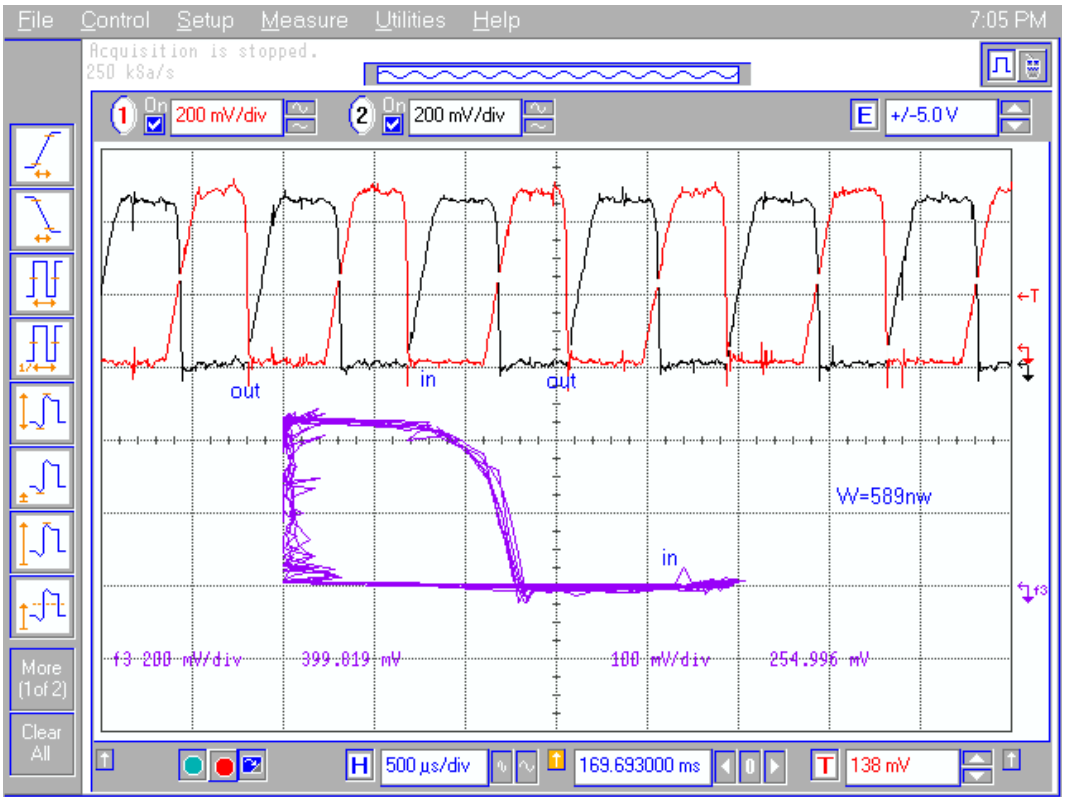

Fig. 12 Test waveforms of the ring oscillator consisting of fifteen cells shown in Fig. 6. The input and output voltages of one of the cells are placed together to show their complementarity. The third waveform is the curve of the output voltage versus the input one. The incident light intensity is about 852 W/m^2.

4 Conclusion

We have proposed an approach of developing electrical-supply free VLSI circuits. The power brought by the circuit input, the incident light in particular, is used to support the circuit operation. Moreover, this optical power can serve not only as supply sources, but also as data or control inputs. Furthermore, part of the power can also be used for optical charge pumping to provide a voltage boost in the circuits. A test circuit has been designed, implemented in a standard 0.18 µm CMOS process, and successfully tested in our laboratory. By means of the circuit test, the principle of the design approach has been confirmed, the feasibility of this kind of circuits proved, the suitability to deep-sub-micron technology verified, and characteristics of the basic cell obtained.

To make the electrical-supply free VLSI circuits operate autonomously, the signal output should be made through free space. Optical coupling, e.g. that with liquid crystal reflection, can be one of the options. With

the technique of the optically powered voltage boost described in sub-Section 2.2, voltages higher than 0.4 V can be generated on-chip. This optical coupling for the signal output can thus be proven feasible.

The proposed approach make it possible to develop VLSI circuits free of power and control lines, and free of battery supports. This approach provides an alternative way to solve efficiently the problems of power supply, distribution, interconnection and interfacing in VLSI circuits. The circuits designed with this approach are particularly interesting and significant in battery-free applications, such as smart cards, and remote signal detection/processing systems.

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