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Title: Wide-Dynamic-Range and High-Sensitivity Current-to-Voltage Converters

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Key words: Analog VLSI, current-to-voltage conversion, adaptive circuits, current filter

Wide-Dynamic-Range and High-Sensitivity Current-to-Voltage Converters

Chunyan Wang

A wide dynamic range and a high sensitivity are often incompatible with each other in analog circuits, such as signal converters or amplifiers. In this paper, we present a method of developing current-to-voltage converters featuring both. It comprises two current-to-voltage conversions. One is to convert the DC component, i.e. the average level of the current input, into a voltage with a nonlinear compression. The other is to apply a “linear” conversion to the signal component of the input current. This conversion is considered to be “linear” as the gain is made to be almost constant if the varying signal is rippling at a given current level, and to increase if the level is changed to be lower. Hence, the gain is adaptive to the input current, i.e. getting stronger if the current signal is weaker and vice versa. This adaptability is implemented by **(a)** an adaptive bias by means of the voltage converted from the DC component of the input current, and **(b)** the current-dependent finite drain-source resistances of MOS transistors. A low-pass current filter is used, in the proposed conversion operation, to separate the DC component of the input current from the signal one. We propose, in this paper, a basic structure of the filter and techniques to improve the filtering quality over a wide current range, also an approach to an effective reduction of the effect of the device mismatch as well. A design example of the proposed conversion is presented in this paper. The simulation results have shown its dynamic range of 5-decades and its sensitivity high enough to detect sub-nA current variations.

Key words: Analog VLSI, dynamic range and sensitivity, current-to-voltage conversion, adaptive circuits, current filter, current compensation for device mismatch

I. Introduction

In many analog circuits, the dynamic range and sensitivity seem to conflict with each other. However, the need for both becomes more and more evident for analog processing circuits to get more

applications. Current-to-voltage converters are often used in current-mode circuits and optical sensors. The variation of a current signal can be over a wide range as it is not directly limited by the supply voltage V_{DD}. If a current-to-voltage converter is involved in a current-mode circuit, the dynamic range of the converter determines that of the circuit. In case of an optical sensor, the photocurrent is usually proportional to the flow of incident photons that can vary over a range of 5 decades or more. It is also often the case that the sensor can not operate over the entire range of the optical signal due to the limited dynamic range of the current-to-voltage converter employed in it.

A converter of linear transconductance may provide a good conversion gain but usually not able to cover a wide range of signal variation. A converter of logarithmic current-to-voltage characteristic [1] [4] may have a wide coverage as the input current is logarithmically compressed, but the same compression results in a low sensitivity to the signal variation. Thus, it is challenging to design a circuit that features a wide dynamic range and a high sensitivity at any given level within the range.

Making the circuit characteristics adaptive to the input current level is an effective approach to the combination of wide dynamic range and high sensitivity. A circuit can be made very sensitive to a weak signal at a given DC level by preset the operating point at this particular level. However, the sensitivity will be significantly lowered if the DC level of the input current is slightly shifted, i.e. the input range for this high sensitivity being very narrow. If the circuit is able to shift its operating point automatically according to the change of the input level, the circuit may still be able to respond very sensitively to the input variation even though it has gone out of its initial range. This shiftable “narrow range of high sensitivity” makes it possible for a circuit with a single input channel to be able to provide a high sensitivity to the signal variation over a wide range. Delbruck’s adaptive sensor may be the first current-to-voltage conversion circuit of this kind. It has a feedback loop for the bias set-up and the feedback factor is made “frequency-dependent” in order to have a low overall gain for the DC component and a higher one for signal variations [2 - 3]. The stability of the loop is secured by an appropriate set of the bias and the device parameters. Another adaptive sensor circuit has been reported in [5]. It makes good

use of a current memory for the automatic tuning of the bias level and the dependency of the MOS drain-source resistance on the current level for the gain adaptive to the input. As the circuit involves an analog switch, making the switching noise low is a critical issue to secure a good operation.

In this paper, a method of developing wide dynamic range and high sensitivity current-to-voltage converters is presented. It is based on the same principle of the shiftable “narrow range of high sensitivity” described above. This method is two-fold. The first is to separate the DC component of the input current from the signal one by a low-pass current filter. The DC current is used, after a compression, to set up the device bias. The second is to convert the input current signal component, not the DC one, into a voltage signal with an adaptive gain. A design example using this method and the simulation results are also presented. The basic scheme of the work in its early stage has been briefly reported in [6]. The present paper aims at providing the readers with a comprehensive grasp of the method and its fundamentals, and that of the practical designs with details.

II. Description of the proposed method

2-1 Principle and the basic scheme

The input current of a current-to-voltage converter can be expressed as $i_{IN} = I_{IN} + i_{in}$, the sum of its DC component and signal variation. The response to the input is the output voltage $v_{OUT} = V_{OUT} + v_{out}$. It is usually the case that **(a)** $i_{in} << I_{IN}$ and (**b)** i_{in} with a higher I_{IN} is statistically greater than i_{in} with a lower I_{IN}. The components of the input current are to be converted differently so that each of them can be used for different purposes. The “main” conversion is that of the small signal component and a high gain is needed for a high sensitivity. The DC one of the input current is to be converted into a DC voltage for the circuit biasing to be adaptive to the input level, and a compression is evidently needed if the current varies over a wide range, e.g. from 1 nA to 100 μA, while the bias voltage should be confined within a window of less than 1 V.

The separation of the DC component I_{IN} from the signal component i_{in} can be done by means of a low-pass current filter. This filter is used to extract I_{IN} and a current copier is used to produce a copy of i_{IN}. Then, as illustrated in Fig. 1, $i_{in} = i_{IN} - I_{IN}$ can be obtained at the node v_{OUT} and converted to the voltage signal v_{out} by using the output resistance at the node. The components of the output voltage should be produced in such way that

$$V_{OUT} = F_{CM}(I_{IN}) \qquad v_{out} = r_m(I_{IN})\, i_{in} \tag{EQ 1}$$

where $F_{CM}(I_{IN})$ is a compression function of I_{IN} and $r_m(I_{IN})$ is a resistive coefficient, both being dependent on I_{IN}. The compression function $F_{CM}(I_{IN})$ needs to be nonlinear, e.g. logarithmic, so that a larger I_{IN} is compressed with a strong compression rate, which results in V_{OUT} that is able to vary with I_{IN} without going beyond the boundaries of the voltage range. Both I_{IN} and V_{OUT} are then used to bias the devices connected to the output terminal where i_{in} is converted into v_{out}. Thus, the biasing point is made input-current-dependent, i.e. shiftable according to the input current level. Also, this shiftable biasing can also make $r_m(I_{IN})$ adaptive to the input current, if r_{o1} and r_{o2} are determined by the current.

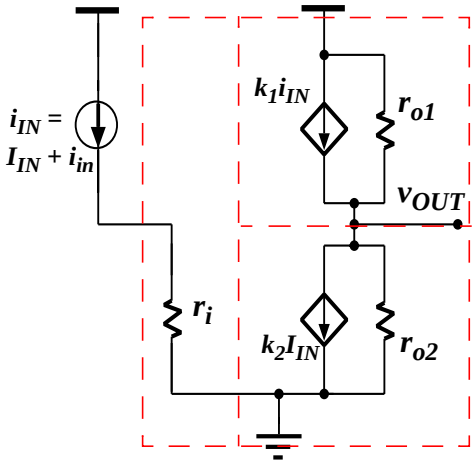

Fig. 1 Diagram illustrating the principle of the proposed method for the design of wide dynamic range current-to-voltage converters. Such a converter consists of three parts. The left part is the input stage, the upper-right one is a current copier, and the lower-right one a low-pass current filter that extracts I_{IN} from i_{IN}. If $k_1 = k_2 = k$, the voltage variation v_{out} will be determined by $k \dfrac{r_{o1} \cdot r_{o2}}{r_{o1} + r_{o2}} (i_{IN} - I_{IN}) = r_m i_{in}$. The conversion can be made linear if the resistances r_{o1} and r_{o2} are voltage-independent.

A low-pass filter can be built based on a current mirror, as shown in Fig. 2 [6], in which the time constant $\tau = C/g_{m1}$,with g_{m1} being the transconductance of N_1, is greater than $1/f_{min}$, where f_{min} is the lowest frequency component of the signal i_{in}. This circuit can also provide a logarithmic compression of I_{IN} at the node V_{gn}, if the current of N_1 is weak enough to drive the device in the weak inversion region. If the transistors are matched, the drain voltage of N_2, the NMOS in the right side, should be equal to V_{gn}.

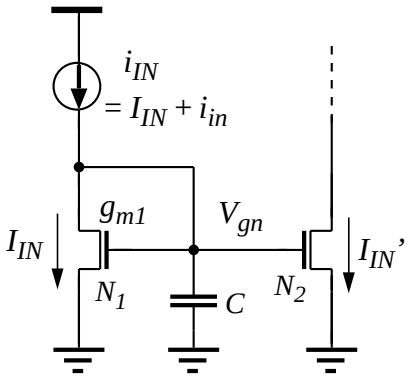

Fig. 2 Current-mirror-based low-pass current filter. If the time constant $\tau = C/g_{m1}$ is large enough, the common gate voltage V_{gn} will be able to respond only to slow-changing component I_{IN}, and thus only I_{IN} is mirrored to the right side of the circuit.

Using the current-mirror-based low-pass current filter, we propose a basic circuit structure, as shown in Fig. 3 [6], for a wide dynamic range and high sensitivity current-to-voltage conversion. In this circuit, two copies of the input current i_{IN} are made by means of the PMOS transistors P_1 and P_2. From the first copy i_{P1}, the DC component I_{N1} is obtained in the NMOS N_1, and then I_{IN}' is generated in N_2. The second copy i_{IN}' is combined with I_{IN}' at the node v_{OUT} to extract the small current signal i_{in}. The output voltage signal v_{out} is converted from i_{in}, by means of r_{dsP2} combined with r_{dsN2}, the finite drain-source resistance of P_2 and that of N_2 [5]. The gain for the signal variation, $r_m(I_{IN}) = v_{out}/i_{in}$, is evaluated by $\frac{r_{dsP2} \cdot r_{dsN2}}{r_{dsP2} + r_{dsN2}}$. Please note that r_{dsP2} and r_{dsN2} are almost constant if P_2 and N_2 are in the saturation mode and their gate voltages are fixed, which makes a “linear” conversion from i_{in} to v_{out}.

However, if the current level I_{IN}' changes, the voltages will be modified, making the resistances change. A lower I_{IN}' results in higher r_{dsP2} and r_{dsN2}, which makes a strong $r_m(I_{IN})$ to a weaker input current. Thus, the conversion gain is adaptive to the signal.

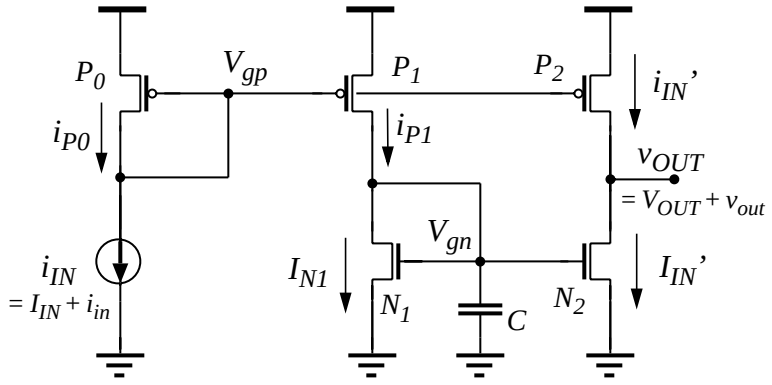

Fig. 3 Basic structure of the proposed current-to-voltage converter. The current filter shown in Fig. 2 is incorporated to make I_{IN}', a copy of the DC component of the input current i_{IN}. The output voltage v_{OUT} is modulated by $v_{out} = r_m(I_{IN})\, i_{in}$, where $r_m(I_{IN}) \approx \dfrac{r_{dsP2} \cdot r_{dsN2}}{r_{dsP2} + r_{dsN2}}$. Its DC component V_{OUT} is expected to be approximately at the same level as V_{gn}.

Consisting of only five transistors, the circuit shown in Fig. 3 can be expected to perform a low-pass current filtering, a logarithmic compression of the DC component and a current-to-voltage conversion with a variable gain. In the next sub-section, an analysis of its performance is presented and the design of a complete circuit for a wide dynamic range and high sensitivity conversion proposed.

2-2 Design example and analysis

The basic scheme shown in Fig. 3 illustrates how the proposed method can be applied in CMOS circuit design. For a given dynamic range, one needs to take the following issues into consideration.

- The condition for the low-pass filtering, $\tau = C/g_{m1} > 1/f_{min}$. It should be noted that $g_{m1}$is determined by the size of the transistor N_1 and the current flowing in it. If the current gets very strong, $1/g_{m1}$ may become too small for the condition to be satisfied, making the upper limit of the current range.

- The minimum current in each of the transistors. It determines the lower end of the current range.
- The voltage limit for V_{gp} and V_{gn}. All the transistors in Fig. 3 need to operate in the saturation region, which may not be the case if (V_{DD} - V_{gp}) or V_{gn} gets too large.
- The speed concern of the circuit. The time constant τ needs to be large for a good low-pass filtering. However, if τ is too large, the circuit may not able to adjust its biasing point quickly to respond to a fast change of the input DC level, in particular, when the current is at the lower end of its range.

The most critical issue is to make $\tau = C/g_{m1} > 1/f_{min}$ in the current filter, as it concerns the quality of the separation of the DC current from the signal current. One can look into the two elements, C and g_{m1}, and their dependencies on the input current. The capacitance C could be voltage dependent, but as V_{gs}, the voltage across C, is not going to change in a large scale when the current changes, C is relatively stable and not sensitive to the current variation. The transconductance g_{m1}, however, depends very much on I_{N1} that is, in its turn, dependent on i_{IN}. The dependency of I_{N1} on i_{IN} needs to be reduced in order that g_{m1} will be made less i_{IN}-dependent. As I_{N1} is the DC component of i_{P1}, if i_{P1} is made to vary in a smaller scale than i_{IN}, the variation of I_{N1} will be down-scaled, making g_{m1} less sensitive to i_{IN}. Let us define the scaling factor $k = i_{P1}/i_{IN}$, i.e. $k = I_{N1}/I_{IN}$ if the low-pass filter functions correctly, and make $k < 1$ in a linear or nonlinear manner described as follows.

1. A linear down-scaling can be done by setting the size ratios of PMOS transistors P_1 and P_0 as $(W/L)_{P1} = k\,(W/L)_{P0}$ to make $i_{P1} = k\,i_{IN}$. The dependency of g_{m1} on i_{IN} is then down-scaled by a factor of k. A smaller value of k makes a stronger down-scaling and more extension of the upper end of the input current range. However, one should also take the lower end of the current range into consideration while selecting the value of k. If the minimum input current is, for instance, 0.1 nA and $k = 0.1$, the currents in the transistors P_1, P_2, N_1 and N_2 will be in the level of tens of pico-Amperes that may be too low to drive the MOS device properly and result in a poor signal-to-noise ratio. Also, the operation speed would suffer in this case.

2. A desirable down-scaling is nonlinear with k variable according to the level of the input current i_{IN}. As g_{m1} increases with the current, the concern of the filtering condition $\tau = C/g_{m1} > 1/f_{min}$ arises when the input current i_{IN} is in the upper part of its current range. If i_{IN} is in the lower part of the range, the critical issue is to make the circuit sensitive enough to respond to the weak signal current i_{in}, instead of $\tau > 1/f_{min}$. Therefore, one would wish the down-scaling factor to be dependent on I_{IN} and it should be effective only when i_{IN} is above a certain level.

A nonlinear down-scaling can be implemented by adding a current bypass branch controlled by the level of the input current. In the example shown in Fig. 4, the branch is in parallel with the PMOS transistor P_0 to make $i_{P0} = i_{IN} - i_{BP}$, i_{BP} denoting the bypass current. If $i_{BP} \neq 0$, only a portion of i_{IN} will be mirrored to produce I_{N1} in the NMOS transistor N_1. Thus, if the DC component of i_{IN} increases, the change of I_{N1} is down-scaled. The bypass current i_{BP} is controlled by V_{gn} in context of a negative feedback loop with the closed-loop gain smaller than unity. The down-scaling may not be effective if the loop is open, i.e. the NMOS transistor N_3 is not conducting and $i_{BP} = 0$ when i_{IN} is weak.

The linear and nonlinear scaling methods can be applied in the same circuit. In the circuit shown in Fig. 4, the open-loop gain A is the linear scaling factor and the feedback gain $\frac{1}{1 + fA}$ the nonlinear down-scaling one. A linear up-scaling, i.e. $A > 1$, can help to extend the lower end of the input current range, as it provides a current amplification when i_{IN} is very weak while the feedback loop is open. If the loop is closed because i_{IN} gets stronger, the overall gain of $\frac{A}{1 + fA}$ can be made to be smaller than unity for a nonlinear down-scaling in order to extend the upper end of the current range.

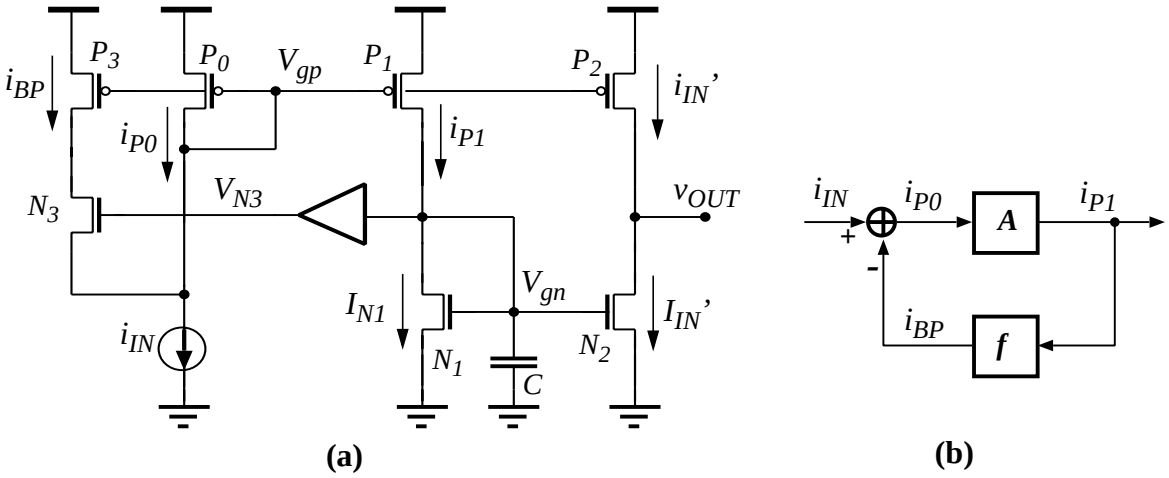

Fig. 4 Current-to-voltage converter with an input current bypass branch added to make $i_{P0} = i_{IN} - i_{BP}$ in order to scale I_{N1} down in case that i_{IN} is high. The current i_{P0} is mirrored to determine i_{P1}, I_{N1} and V_{gn}. The same V_{gn} is then used, via a voltage shifter shown as a triangle symbol, to control i_{BP}. This is a negative feedback loop and its block diagram is shown in (b). The close-loop gain $\frac{i_{P1}}{i_{IN}} = \frac{A}{1 + fA} < 1$, where $A = i_{P1}/i_{P0}$ is related to the ratio of $(W/L)_{P1}$ to $(W/L)_{P0}$, and f is determined by the transconductances of N_1, N_3, and P_3, and the input i_{IN} as well. The loop may not be effective, i.e. $i_{BP} = 0$ and $i_{P0} = i_{IN}$, if i_{IN} is too weak to make V_{gn} high enough to turn N_3 on.

Besides the dynamic range, the operation speed is another important issue. One wishes that the circuit should be able to adjust its biasing point quickly if the level of the input current changes. However, if the input current is very weak, this adjustment may be very slow, in particular when the capacitance at the common gate of N_1 and N_2 is large to have the time constant large enough for a decent low-pass filtering. One of the solutions to this kind of problem is to add a charging current when I_{IN}' is lower than the average of i_{IN}'. It can be implemented by means of a transistor, such as the NMOS transistor N_4 shown in Fig. 5. This transistor provides a "transient current" to accelerate the charging process at V_{gn}. When V_{gn} becomes high enough to make I_{IN}' equal to the average level of i_{P1}, V_{OUT} will be lowered to a level similar to that of V_{gn} and N_4 will be turned off.

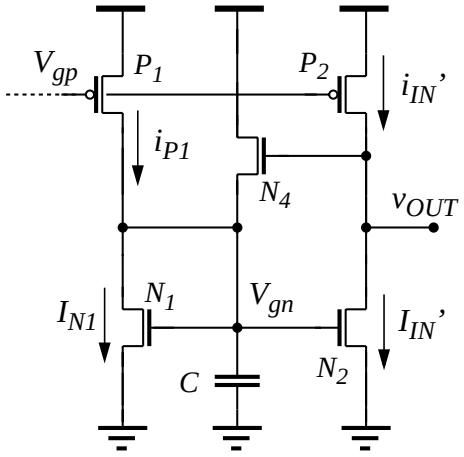

Fig. 5 Additional charging current by the NMOS transistor N_4 to accelerate the rise of V_{gn}. This current is effective when V_{OUT} reaches a level high enough to turn N_4 on. Such a high level V_{OUT} occurs when I_{IN}' is smaller than the DC component of i_{IN}'.

The diagram shown in Fig. 6 is a current-to-voltage conversion circuit designed with the proposed method. It has a negative feedback loop for the nonlinear down-scaling. The difference between this loop and that in Fig. 4 is that its feedback signal i_{BP} is able to vary more widely, by means of a master-slave structure, to match a wider range of the input i_{IN}. Also, the circuit involves the additional charging current path, the same as that in Fig. 5, to accelerate the charging process at the node V_{gn} in case of weak i_{P1}, to improve the operation speed and to maintain V_{OUT} at approximately the same level as V_{gn}. This design shows that the proposed method can be easily implemented in a CMOS circuit with the measures for the signal range and processing speed incorporated. Its performance evaluation by electrical simulation is presented in the next section.

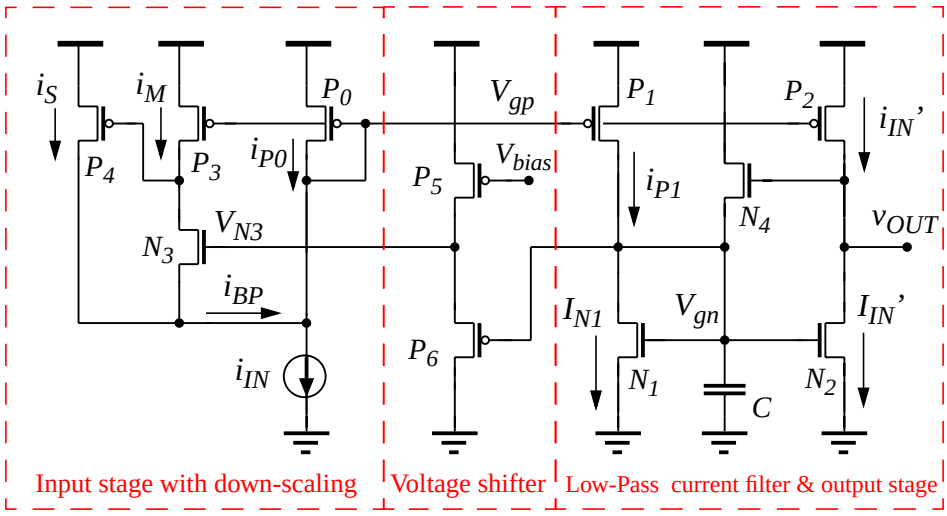

Fig. 6 Complete circuit of a wide dynamic range and high sensitivity current-to-voltage converter. The bypass current i_{BP} is given by $i_M + i_S$, the sum of the master and slave currents. The slave current i_S is effectively added to i_{BP} if the drain voltage of P_3 is lowered enough to drive P_4 on, which can happen when i_M is reaching its full scale. Thus, the range of the feedback signal i_{BP} is made larger to extend the upper limit of the dynamic range of i_{IN}. The NMOS transistor N_4 provides an extra charging current to accelerate V_{gn} rising when $I_{IN}' < i_{IN}'$ is detected.

III. Simulation results

The circuit shown in Fig. 6 has been simulated using Hspice with the transistor models of a 0.18 μm CMOS technology. The supply voltage V_{DD} is 1.8 V and the voltage V_{bias} is 0V. The input current i_{IN} is a DC current I_{IN} modulated by a sinusoidal signal i_{in}. The range of I_{IN} is from 4 nA to 411 μA. For a given I_{IN}, the modulation depth h, i.e. the ratio of the amplitude of i_{in} to I_{IN}, is from 5% to 20% in the simulations.

In the circuit shown in Fig. 6, the DC currents in the transistors P_0, P_1, and P_2 are determined by I_{IN}, the DC level of the input signal i_{IN}, and the aspect ratio of the transistors that are listed in Table 1. The ratio of $(W/L)_{P1}$ over $(W/L)_{P0}$ is equal to 0.1, which gives a linear down-scaling, making I_{N1} and I_{IN}' be approximately one tenth of I_{IN}. The capacitance C at the common gate of N_1 and N_2 is made large by placing a drain-source grounded NMOS of 400 μm^2 in order to secure the low-pass filtering condition $C/g_{m1} > 1/f_{min}$ when I_{IN} reaches 411 μA.

TABLE 1.

W_m: minimum gate width L_m: minimum gate length			
P_0	W_m/L_m		
P_1	$W_m/10L_m$	N_1	$W_m/1.2L_m$
P_2	$W_m/10L_m$	N_2	$W_m/1.2L_m$
P_3	$4.5W_m/L_m$	N_3	$3W_m/1.2L_m$
P_4	$9W_m/L_m$	N_4	W_m/L_m
P_5	$W_m/2.8L_m$	P_6	W_m/L_m

The simulation waveforms of the circuit shown in Fig. 6 are illustrated in Fig. 7. They demonstrate that the circuit is able to respond to the variation of the input current over the entire range. The DC level of the input signal i_{IN} changes over the range of 5-decades, and the DC level of the output voltage v_{OUT} is "confined" within a small voltage window of less than 350 mV, which permits the MOS transistors to operate within the region of the current-source mode where the drain-source resistance is high. The output voltage signal v_{out} is measured under different conditions of i_{IN}, and the results are shown in Fig. 8. It illustrates the shiftable "narrow range of high sensitivity" characteristics described in Section I. Using these results, the conversion gain, defined as the ratio of the amplitude of v_{out} to that of i_{in}, are presented in Table 2. It has been observed that, at a given level of I_{IN}, i_{in} is converted into v_{out} with an almost constant gain. However, this gain depends on I_{IN} in a nonlinear manner, because of the nonlinear characteristics of MOS transconductance and the nonlinear down-scaling. This dependency make the gain adapt to the input current, i.e. a higher gain for a lower level current. It has been measured that, at I_{IN} = 4 nA, the conversion gain is about 80 mV/nA, which makes the circuit to be able to produce a detectable voltage signal when i_{in} is in a sub-nA range. This gain is reduced about 47000 times, when I_{IN} is about 10^5 times stronger to reach 411 μA, in order that the transistors still operate in the saturation region. It should be noted that, at this I_{IN} level, the conversion gain is still much higher than that a logarithmic converter can provide, as the logarithmic compression is not applied to i_{in}. Hence, a wide dynamic range and high sensitivity conversion have been made compatible with each other in this circuit.

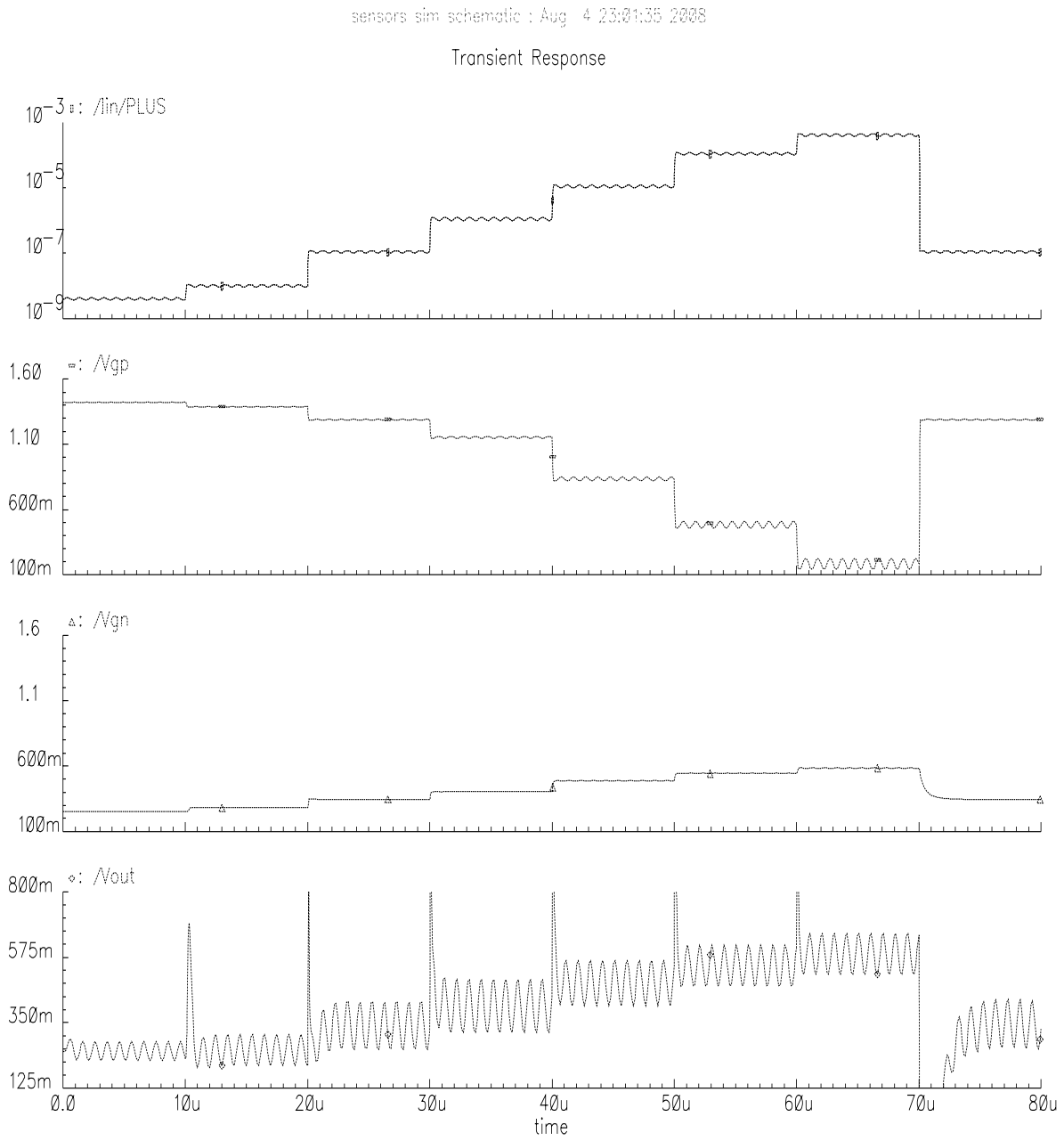

Fig. 7 Simulation waveforms of the circuit shown in Fig. 6. The waveforms are obtained when the frequency of the sinusoidal i_{in} is 1 MHz and the ratio of the amplitude of i_{in} to I_{IN} is 10%. The first waveform, i.e. that on the top, is the input current i_{IN}, displayed in a logarithmic scale. The second and third waveforms illustrate that V_{gp} responds to the current ripple of the input but V_{gn} follows only the change of the average current level, filtering out the signal variation. The DC component V_{OUT} of the output voltage v_{OUT} is ranged from 250 mV to 590 mV, corresponding to the range of I_{IN} from 4 nA to 411 μA. The voltage signal v_{out}. varies in the same way as the the input current signal i_{in}, over the entire range of 5 decades.

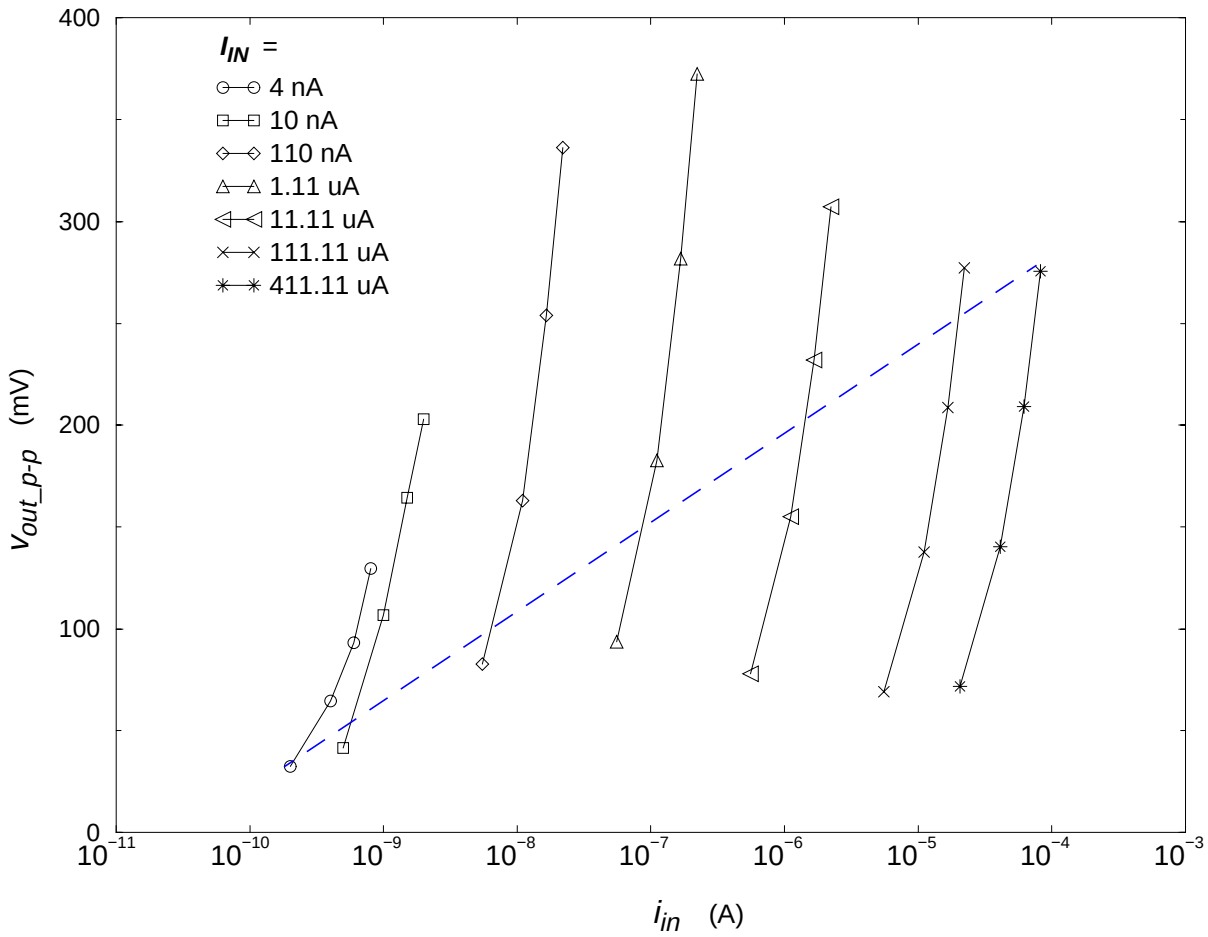

Fig. 8 Characteristics of the peak-peak amplitude of the output voltage variation v_{out} versus the amplitude of the sinusoidal current signal i_{in} rippling over the DC component I_{IN}. Please note that the x-axis is logarithmically scaled. Each curve is obtained with a given I_{IN} and four different i_{in}, i.e. the modulation depth h = 5%, 10%, 15% and 20%. If I_{IN} is set at a higher level, the characteristic curve will be shifted rightwards and its slope will be reduced. The ratio of the amplitude of v_{out} to that of i_{in} for each set of (I_{IN}, h) is calculated and presented in Table 2. The dashed line indicates a characteristic curve that a logarithmic current-to-voltage converter could have.

TABLE 2. Conversion Gain of the Circuit Shown in Fig. 6

I_{IN}	*Conv. Gain* **(mV/nA)**		I_{IN}	*Conv. Gain* **(mV/μA)**	
4 nA	h = 0.05	81.25	11.11 μA	h = 0.05	70.27
	h = 0.10	80.88		h = 0.10	69.85
	h = 0.15	77.58		h = 0.15	69.64
	h = 0.20	81,00		h = 0.20	69.12
10 nA	h = 0.05	41.69	111.1 μA	h = 0.05	6.229
	h = 0.10	53.40		h = 0.10	6.20
	h = 0.15	54.80		h = 0.15	6.085
	h = 0.20	50.75		h = 0.20	6.238
110 nA	h = 0.05	8.27	411.1 μA	h = 0.05	1.744
	h = 0.10	7.409		h = 0.10	1.707
	h = 0.15	7.694		h = 0.15	1.696
	h = 0.20	7.64		h = 0.20	1.676
1.11 μA	h = 0.05	.844	The conversion gain is the ratio of the amplitude of v_{out} to that of i_{in}. The modulation depth h is the ratio of the amplitude of i_{in} to I_{IN}.		
	h = 0.10	.822			
	h = 0.15	.846			
	h = 0.20	.843			

The above simulation results are obtained without considering the effect of device mismatch. The circuit illustrated in Fig. 6 involves two pairs of MOS transistors, namely (P_1, P_2) and (N_1, N_2), in its low-pass current filtering block. If N_1 and N_2 match, or mismatch, each other in the same way as P_1 and P_2, the DC component of the current in P_2 and the current in N_2 will be equal to cancel each other, resulting in $V_{OUT} = V_{gn}$. Otherwise, the difference of the two currents will be $i_{in}' + \Delta I_{IN}'$, instead of i_{in}', with $\Delta I_{IN}'$ resulting from the device mismatch. This $\Delta I_{IN}'$ is then converted into a DC component $\Delta V_{OUT} = r_m(I_{IN}) \Delta I_{IN}'$, making $V_{OUT} = V_{gn} + \Delta V_{OUT}$, instead of V_{gn}, which we call the DC mismatch. The deviation of V_{OUT} from V_{gn} could make P_2 or N_2 out of the normal operation in the saturation region, in case of a strong v_{out}, and thus causes a signal distortion. This DC mismatch, however, can be corrected by injecting a DC current into, or removing it from, the drain of N_1 to compensate I_{N1} in such a way that I_{IN}', the mirrored copy of I_{N1}, is equal to the DC component of the current in P_2. Evidently, when the correction is done, i.e.V_{OUT} being brought back to the level of V_{gn}, the compensated I_{N1} needs to be maintained. The transistor N_4 shown in Fig. 5 is not able to provide a DC current for the

compensation while $V_{OUT} \approx V_{gn}$. One can use the voltage difference (V_{OUT} - V_{gn}) to generate a current compensating for the mismatch. Fig. 9 illustrates the low-pass current filter with such a compensation current provided by the two transistors N_5 and N_7 combined. Replacing the low-pass current filter in the current-to-voltage converter shown in Fig. 6 by that illustrated in Fig. 9, we make the converter have the DC mismatch compensation and it has then been simulated with Hspice. The simulation waveforms, illustrated in Fig. 10, demonstrated that this circuit is able to make the DC level of the output voltage uniformed at the level approximately equal to V_{gn} despite the device mismatch. The current compensation is, therefore, an effective solution to the problem of the DC mismatch.

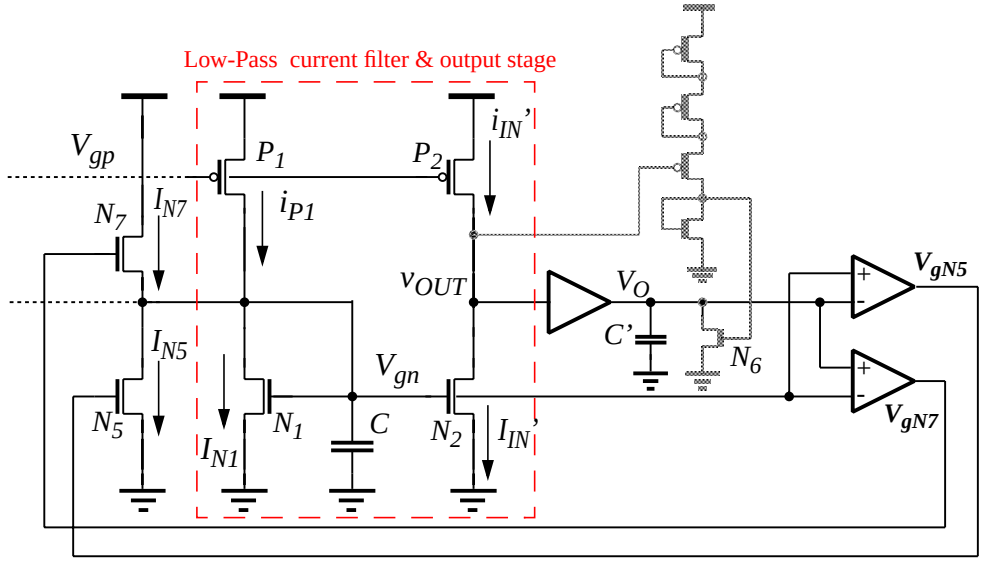

Fig. 9 Low-pass current filter with a DC current compensation for device mismatch. The average level of v_{OUT}, denoted as V_O, is compared with V_{gn} to produce two voltages V_{gN7} and V_{gN5} that are used to control the currents of N_7 and N_5, respectively. The current difference (I_{N7} - I_{N5}) compensates for the device mismatch to make I_{IN}' equal to the DC component of i_{IN}'. In this case, the transistor N_4 shown in Fig. 6 is removed as N_7 can provide the gate capacitance C with an additional current. The devices drawn in dashed lines are used to have a fast pull-down of V_O, when I_{IN}' >> i_{IN}' due to sudden change of the input level I_{IN}, by the "normally-off" NMOS transistor N_6 in order to reduce I_{IN}' quickly. The voltage follower used in this circuit consists of 2 transistors, namely P_5 and P_6 shown in Fig. 6. Each of the voltage comparators is a single-stage differential amplifier consisting of five transistors.

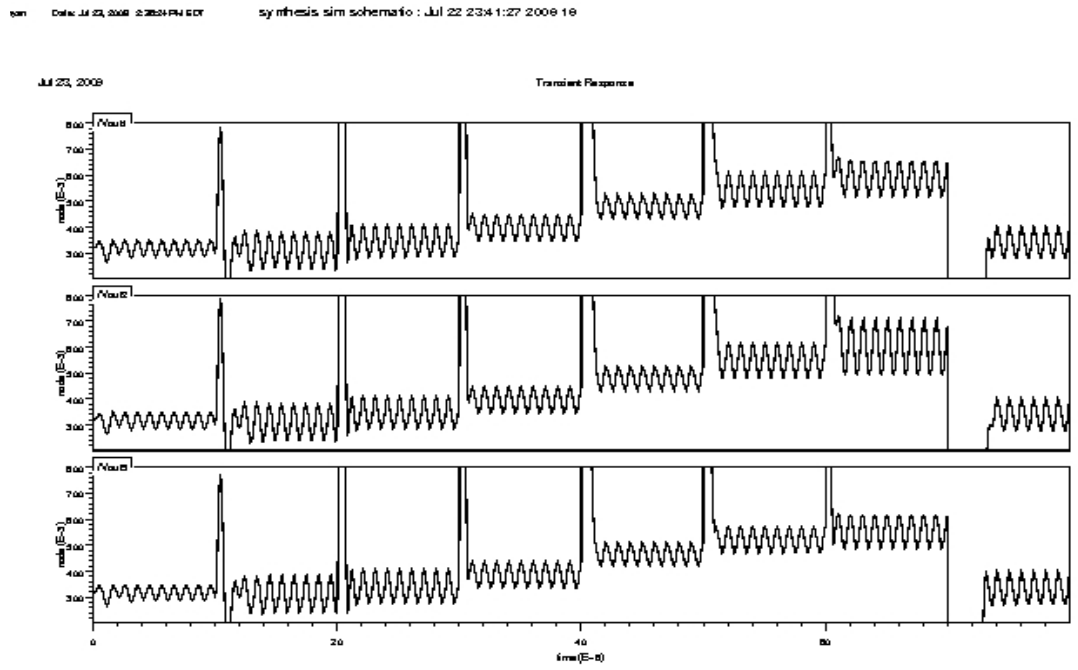

Fig. 10 Simulation waveforms of the three current-to-voltage converters of which the structures are identical and involve the same current compensation shown in Fig. 9, but device mismatch is different. The input signal is identical to that producing the waveforms shown in Fig. 7. The first waveform v_{OUT1} is the output voltage of the converter without device mismatch. The second one, v_{OUT2}, is produced by the circuit in which g_{mN1}, the transconductance of N_1, is 36% smaller than g_{mN2}, and v_{OUT3} by the one with g_{mN1} being 36% larger than g_{mN2}. The three waveforms have the almost identical DC level V_{OUT} by means of the compensation.

It should be noted that the low-pass current filter involves the capacitance C made of a large drain-source grounded NMOS transistor in order to operate at an input current level of 411 μA. Such a large device makes the circuit too bulky to be placed in a pixel of an image sensor. However, in a CMOS image sensor, the current delivered by a tiny photodiode could hardly reach any micro-Ampere level and the input range is shifted toward a much lower end. If the proposed current-to-voltage converter is used in such a sensor, the capacitance can be made much smaller. Another issue to be noticed is the nonlinear nature of the conversion. This conversion is globally nonlinear and locally “linear”. The compression of the DC component, by means of the device nonlinearity, permits the wide input range. The “linear” high gain conversion, is based on the linearity of MOSFET drain-source resistances in the

saturation mode when the DC component of the input current is fixed. However, like all the other cases of using nonlinear devices for “linear” operations, this linearity is limited. Moreover, the drain-source resistances of the transistors of the same design but placed in different places can not be exactly identical. If the circuit is used in a CMOS image sensor, the converters in different locations will have non-uniform outputs while the input is uniform. A compensation for this mismatch requires more research efforts.

IV. Conclusion

The work presented in this paper aims at solving the problem caused by the conflict of dynamic range and sensitivity in current-to-voltage conversion circuits. The proposed solution is to employ a low-pass current filter to separate the DC component from the signal one of the input current, to use the DC one, after a compression, for an input-dependent biasing, and to convert the signal one with an adaptive gain. This solution can be easily implemented in a CMOS circuit. A current mirror consisting of a transistor pair can be used as such a filter if its time constant is made to satisfy the low-pass filtering condition. This time constant is current-dependent. But the dependency can be reduced by applying the current down-scaling proposed in this paper. The compression function is based on nonlinear current-dependent characteristics of MOS transconductance. The voltage resulting from this compression is biasing the MOS transistors that determine the conversion gain applied to the signal component, which makes the gain adaptive to the input current. A design example of the proposed current-to-voltage conversion has been provided and its performance evaluated by the simulation with CMOS 0.18 μm models. The results have shown that the circuit is able to operate with an input current varying over a range of 5 decades. It is sensitive enough to respond to a current signal of a fraction of a nano-Ampere. A conversion gain is almost constant if the DC level of the input stays the same, and decrements if the level increments, which allows the circuit to detect the signal current when it is in the higher end of the 5-decade range without saturation.

Besides the dynamic range and sensitivity, the converters designed with the proposed method feature low power dissipation. The biasing currents are the DC component of the input current and its copies, if the current in the voltage shifter in Fig. 6 can be ignored. It should also be mentioned that, unlike many current-mode circuits, these converters do not need clock and switches, and the conversion is performed on a continuous time basis. Thus the problems such as switching noise and preparation phases do not arise. Moreover, sparing from clocks makes the circuits to spare from many clock-related problems and facilitate their applications. Furthermore, to reduce the effect of device mismatch, a DC current compensation method has been presented in this paper and its effectiveness verified by the simulation results.

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