NOTE TO USERS

A MULTI-FEATURED SINGLE-PHASE UTILITY INTERFACE WITH REDUCED DC LINK CAPACITOR FOR DISTRIBUTED POWER SOURCES

Zhixiang Luo

A Thesis

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Of

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ABSTRACT

A MULTI-FEATURED SINGLE-PHASE UTILITY INTERFACE WITH REDUCED DC LINK CAPACITOR FOR DISTRIBUTED POWER SOURCES

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The traditional, regulated electric power systems are based on large power generation plants located far from load centers. In a deregulated market, however, small and environmentally friendly power plants using wind power, photovoltaic cells, fuel cells and micro-turbines can be installed through a given distribution system. This concept of distributed generation tends to reduce the cost of electricity and to reduce or postpone major investments in the transmission system.

Many of these small power plants are typically consumer owned and are connected to the utility grid by means of single-phase power electronic voltage source converters. This type of converter that supplies active power to the ac grid can also be controlled to provide active filtering and Var generation, thus enhancing the quality of the power at a given point and providing added value to the distributed power source.

This Thesis focuses on the practical issues of a multi-featured single-phase utility interface. It focuses on three important aspects: 1) the management of the low order voltage harmonics present in the dc bus of the interface. 2) The design of fast and robust single phase phase-locked loop for the synchronization of the power interface. 3) A new control circuit for a three-level hysteresis current controller.

Finally, a digital signal processor based prototype test circuit that satisfies all the aforementioned functions and allows active power filtering and reactive power compensation is built in the laboratory to demonstrate the effectiveness of the proposed techniques.

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List of Acronyms

AD	Analog to Digital
DA	Digital to Analog
DSP	Digital Signal Processing
FPGA	Field-programmable Gate Array
HCC	Hysteresis Current Controller
IGBT	Insulated Gate Bipolar Transistor
MPPT	Maximum Power Point Tracking
PI	Proportional and Integrated
PV	Photovoltaic
PWM	Pulse Width Modulation
PLL	Phase-locked Loop
THD	The total harmonics distortion level
VSI	Voltage Source Inverter
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VCO	Voltage Controller Oscillator

List of Principal Symbols

$v_{ac(t)}$	The ac grid voltage;
V_{ac}	The magnitude (peak value) of ac grid voltage;
$v_{dc(t)}$	The dc bus voltage;
V_{dc_ref}	The dc bus reference voltage;
$\nabla v_{dc(t)}$	The dc bus voltage ripple;
$i_{ac(t)}$	The ac grid current;
$i_{ac\_ref(t)}$	The ac grid reference current;
$i_{load(t)}$	The load current;
$i_{inv(t)}$	The inverter current;
$i_{pv(t)}$	The PV panels output current;
$p_{ac(t)}$	The power supplied by the ac grid;
$p_{load(t)}$	The power consumed by the load;
$p_{pv(t)}$	The power supplied by the PV panels ;
$p_{c(t)}$	The power supplied by the dc bus capacitor ;
$p_{L(t)}$	The power absorbed by the inverter inductor ;
L_{inv}	The inverter inductance;
w_l	The cut-off angular frequency of the low pass filter;
$u_{i(t)}$	The PLL input voltage;
$u_{o(t)}$	The PLL output voltage;
U_o	The PLL output voltage magnitude;
$u_{d1(t)}$	The PLL phase detector output voltage;
$u_{d2(t)}$	The PLL magnitude detector output voltage;

$u_{f(t)}$	The PLL loop filter output voltage;
w_o	The central angular frequency of the PLL system;
w_n	The natural angular frequency of the PLL system;
ζ	The damping ratio of the system;
τ	The time constant of the system;
f_{2level}	The switching frequency of the switches of the two level hysteresis current controller;
f_{3level}	The switching frequency of the switches of the three level hysteresis current controller;
f_{3level_inv}	The switching frequency of the inverter of the three level hysteresis current controller;
h	The inner bandwidth of three level hysteresis current controller;
h_o	The outer bandwidth of three level hysteresis current controller;

1. INTRODUCTION

1.1. General Introduction

Global and national scenarios of electrical energy consumption for the coming decades predict a strong increase in the utilization of renewable energies source (RES). Only a significant increase in the use of RES satisfies the requirement of climate protection and allows suitable growth in energy consumption for newly developed and developing countries [1]. Among the RES, solar radiation is expected to become a major contributor to the global renewable energy supply because of its virtually unlimited potential. Photovoltaic (PV) cells create electricity from sunlight, cleanly and silently, over a period of more than 25 years with very little maintenance and no moving parts. Recently, there has been a tremendous surge in PV technology, efficiency and cost reduction, resulting in a ground swell of new interest and imaginative applications [2]. Grid-connected photovoltaic electricity generation systems, which are being introduced in large quantities in several national programs, can play a key role in distributed power generations in the future.

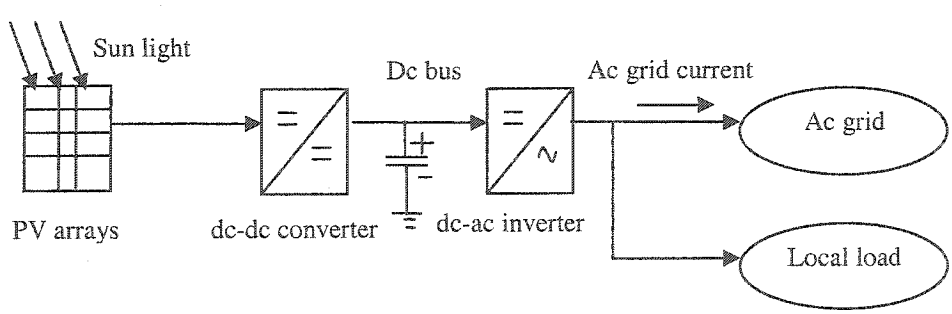

Figure 1.1. Block diagram of a grid-connected photovoltaic system

This thesis focuses on small grid connected consumer owned PV systems that are single phase, without energy storage and in parallel with a non-linear local load. As illustrated in Fig.1.1, photovoltaic arrays (PV) convert sunlight directly into electricity, which can be considered as a dc component since the solar radiation variations are slow compared to the ac grid frequency (60Hz). A dc-dc converter is used to control the voltage level and to implement the maximum power point tracking (MPPT) algorithm that will maximize the generated power of PV arrays. Then, a single-phase full bridge dc-ac inverter is utilized to convert the dc voltage to an ac voltage and to transfer the power from the dc side of the inverter to the ac side. The dc-ac inverter can also compensate for the reactive power component and the harmonic component of the non-linear local loads for unity power factor operation. A capacitor is placed in the dc bus to buffer the extra power caused by the difference between the instantaneous power supplied by the ac grid and that consumed by the local load. It is worth mentioning that with the added features, the photovoltaic system can still work on cloudy days as a power conditioner which can improve the power factor and reduce the total harmonic distortion (THD) of the voltage at the consumer bus.

1.2. Objectives and Challenges

This thesis focus on the control of the above mentioned full bridge dc-ac inverter. Fig.1.2 illustrates the detailed PV system block diagram with the voltage feedback control loop. The objective is to control the ac grid current $i_{ac}(t)$ so that it is sinusoidal and in phase with the ac grid voltage $v_{ac}(t)$, while at the same time keeping the dc bus voltage $v_{dc}(t)$ regulated and equal to its reference value.

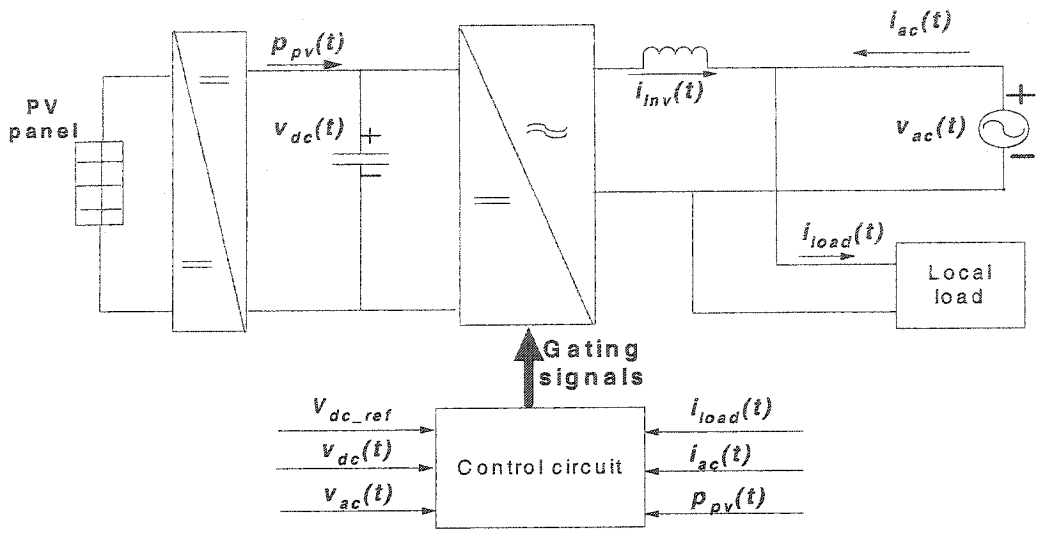

Fig.1.2. Block diagram of the PV system utility interface

Here the gating signals for the dc-ac inverter are obtained by comparing the ac grid current with its reference counterpart, instead of by comparing the inverter output current with its reference counterpart. This is done because grid current sensing offers better performance, especially in eliminating the switching ripple during the moments of load variation [3]. The three specific issues that will be studied in this thesis are:

1) Design of the dc bus voltage control loop which keeps the dc bus voltage regulated and equal to its reference value.
2) Single phase phase-locked loop (PLL) for synchronization of the PV interface.
3) A fast acting current control scheme to control the ac grid current to track its reference counterpart.

The PLL obtains the phase and frequency information of the ac grid voltage which is subject to harmonics, flicker and frequency variations. This information will be used to generate the ac grid reference current. In order to realize the current control scheme, a hysteresis current controller (HCC) instead of a ramp comparison PWM controller, is

chosen since the HCC has much better performance in active power filter applications where fast response speed and good accuracy is needed [4]. However, there exist three challenges:

1) Large dc bus voltage ripple resulted from the reduction of dc capacitor size may cause distortions in the ac grid current.
2) The conventional single phase PLL is not suitable for applications where the operation frequency is low (60 Hz), because of the second order harmonic problem.
3) The switching frequency of the conventional hysteresis current controller is high, thus results in large switching losses.

Reduction of dc capacitor size, which enables the use of a non-electrolytic capacitor, results in large dc bus voltage ripple which may feeds through the inverter and causes distortions in the ac grid current. It is important to find a measure which keeps the distortion of the ac current low in the steady state, while assuring fast system response in the transient state. Unlike three phase PLL, where the second order harmonics from the output of the phase detector can be cancelled by using a d-q transform [5], the second order harmonics constitutes a challenge for the single phase PLL. Since the frequency of the input signal is low (usually 60 Hz), it is extremely difficult to filter out the unwanted low order harmonics without significantly slowing down the system response speed. In order to obtain good output current waveform, the tolerance band of the hysteresis controller should be small and hence the switching frequency will be high and switching losses will be large. The challenge is how to reduce the switching frequency of the hysteresis current controller while retaining all its advantages.

1.3. Contributions of the Thesis

The three principle contributions of thesis are:

1) A voltage ripple estimator is built to estimate the dc bus voltage ripple and cancel it from the voltage feedback signal, thus ensuring low ac grid current distortion in the steady state and fast response speed in the transient state.
2) A single phase PLL, which has solved the second order harmonic problem by using the new phase detection scheme proposed by [6], is designed and implemented.
3) An improved single phase three level HCC is developed, which can reduce 70% of the average switching frequency while achieving the same output performance when compared with the conventional two level HCC.

Because of the new phase detection scheme, the PLL obtains not only the phase, but also the magnitude information of the input signal. It has fast response speed and good harmonic rejection capabilities and is especially suitable for power electronic applications where the input signal frequency is low. Two techniques have been proposed to implement the three level HCC. The first technique is building an analog circuit composed of two hysteresis comparators, one D flip flop, and a few logic gates. The implementation of the proposed control circuit is simpler than the three level HCC described in the literature [7, 8]. The second technique is using FPGA by writing the VHDL code. The major advantage of FPGA implementation over analog circuit implementation is that the implementation can be easily modified, maintained and upgraded.

1.4. Thesis Outline

This Thesis is composed of six chapters and an appendix. Chapter 2 discusses the control strategy for the system with emphasis on the estimation of the dc bus voltage ripple and calculation of the reference current for the ac grid. Chapter 3 designs and implements a single phase PLL which use a special phase detector to solve the second order harmonic problem. Chapter 4 presents and implements a three level hysteresis current controller, which can reduce 70% of the average switching frequency. The principle of operation is illustrated and the prototype is implemented using FPGA. Chapter 5 describes the implementation details of the grid-connected PV utility interface, including parameters design and introduction of the dSPACE system. Experimental results based on the digital signal processor are also provided. Conclusions of the thesis work are drawn in Chapter 6, followed by suggestions for future work.

2. OPERATION AND CONTROL SCHEME OF THE POWER INTERFACE

2.1. Introduction

Small (< 10 kW) consumer owned renewable energy sources are usually connected to the ac grid at the power meter point, which is typically single-phase and low voltage (110-220V). Fig.2.1 shows a typical system where a single-phase voltage source inverter (VSI), in parallel with a local load, interfaces a photovoltaic (PV) system with the utility grid. A dc-dc converter is used to implement maximum power point tracking (MPPT) on the PV array. With supplementary control loops, the VSI can compensate for

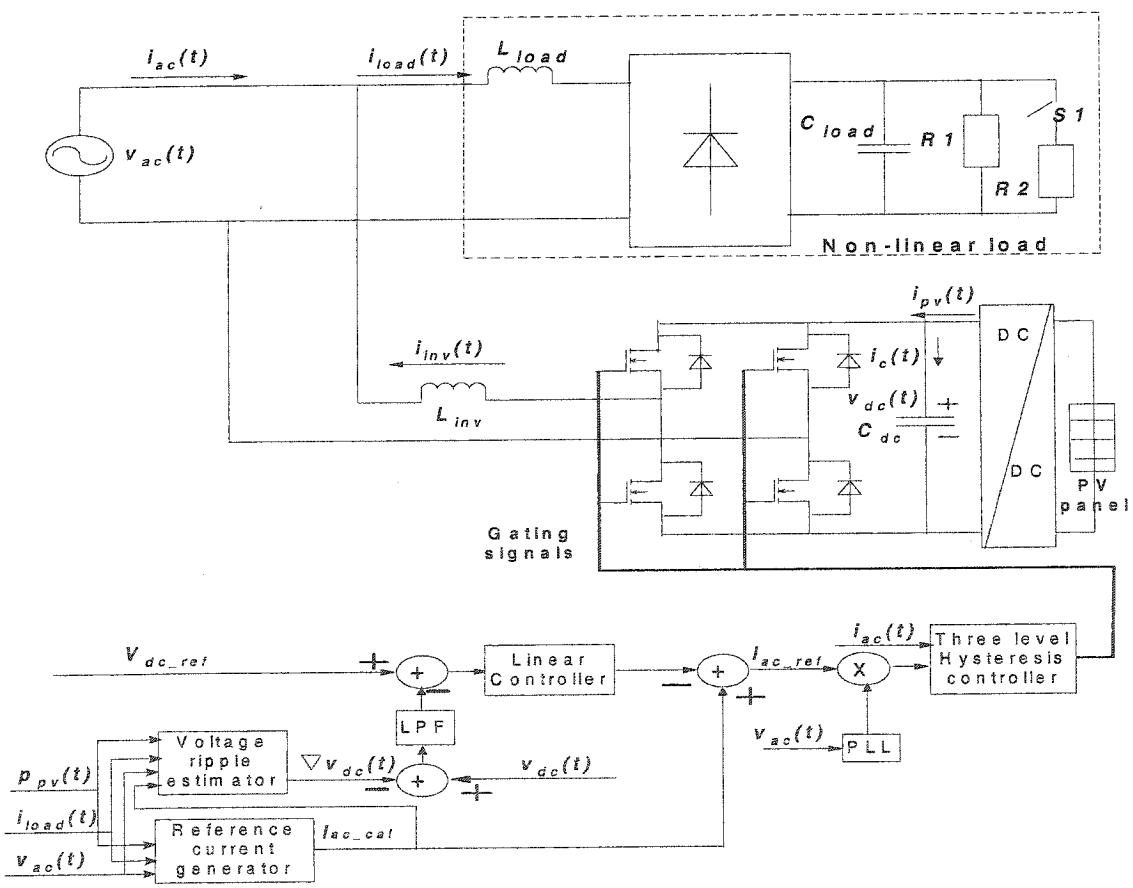

Figure 2.1. Grid-connected PV system block diagram

the reactive power consumed and the current harmonic injected by the local load, yielding a grid current that is sinusoidal and in phase with the grid voltage [8-11].

A major drawback of single-phase VSI is the double line-frequency voltage ripple on the dc bus and a large capacitor is usually employed at the dc terminal to attenuate this low order component. Using a small capacitor in the dc bus of a single-phase grid connected distributed power interface requires effective means for preventing the low frequency ripple from propagating through the inverter and distorting the line current [12]. In this thesis, it is assumed that the PV array is decoupled from the dc link by means of the dc-dc MPPT converter and that dc bus voltage ripple does not interfere with the PV generation.

A number of solutions have been proposed in the literature for dealing with the double line-frequency voltage ripple in the dc bus. It was shown in [13] that a dc bus voltage can operate with large voltage ripple (peak to peak 25%) without causing distortion in the ac grid current when the voltage control loop bandwidth is designed to be only 10 Hz. The low order dc bus voltage harmonic is highly attenuated but the voltage loop has a slow speed of response making the dc bus voltage more susceptible to large variations due to sudden source and load transients. Some schemes as in [14] require an extra converter such as a high frequency current-fed type active filter to circulate the harmonics. Others employ a tuned notch filter to eliminate the double-line-frequency component from the feedback signal [15]. This solution, however, is not suitable when the inverter also operates as an active power filter since the line current is not sinusoidal and other low order even harmonics (4th, 6th...) appear at the dc side.

The approach presented in this chapter is based on the principle of voltage ripple cancellation [16]. That is, the voltage ripple of the dc bus voltage is estimated and subtracted from the actual dc bus voltage. In this way, the feedback signal used in the regulation of the average value of the dc voltage should be ripple free in the steady state and no distortion would be created in the ac line current. As an additional advantage for the distributed power source, the inverter is controlled in such a way that the grid current is sinusoidal and in phase with the grid voltage. It is worth mentioning that even when the PV system is not generating any active power, the inverter can still operate as an active filter and a reactive power compensator.

2.2. Modeling and Analysis of the Control System

The control scheme for the proposed system is shown in Fig.2.1. The inverter is controlled with a fast current controller to impose a sinusoidal grid current in phase with the grid voltage. The magnitude of the current drawn from the grid should be equal to the active component of the load current minus the active component of the ac current of the inverter. In this way, the inverter automatically compensates for the reactive power and the current harmonics of the local load.

The system modeling and analysis are carried out by considering the balance between the instantaneous power supplied by the ac grid and dc source (dc-dc MPPT converter), stored in the dc link capacitor and ac filter inductor and the power consumed by the local load. Subsection 2.2.1 presents a way for calculating the ac grid current in the steady state. Subsection 2.2.2 presents the proposed scheme for estimating the voltage

ripple of the dc bus and subsection 2.2.3 presents a dc voltage control loop that provides regulation for the average value of the dc bus voltage.

2.2.1. Calculating the Magnitude of AC Grid Current

The analysis of the proposed system is carried out assuming that the grid voltage and load current can be represented by

$$v_{ac}(t) = V_{ac}\sin(\omega t) \tag{2-1}$$

$$i_{load}(t) = I_p \sin\omega t + I_q \cos\omega t + \sum_{k=2}^{\infty} I_k \sin(k\omega t + \phi_k). \tag{2-2}$$

According to [10] the magnitude of the active component of the load current can be calculated from the average power consumed by the load. In the proposed application, since the inverter also injects active power into the grid, one needs first to calculate the magnitude of the active component of the inverter current. This part of the inverter current is subtracted from the active component of the load current to obtain the magnitude of the net ac grid current. This can be obtained by integrating the product of the grid voltage and the load current, deducted by the PV panel power, for one line cycle as shown below

$$I_{ac\_cal} = \frac{2\int_{-T}(v_{ac}(t)\, i_{load}(t) - \mathrm{p_{pv}}(\mathrm{t}))dt}{V_{ac}}. \tag{2-3}$$

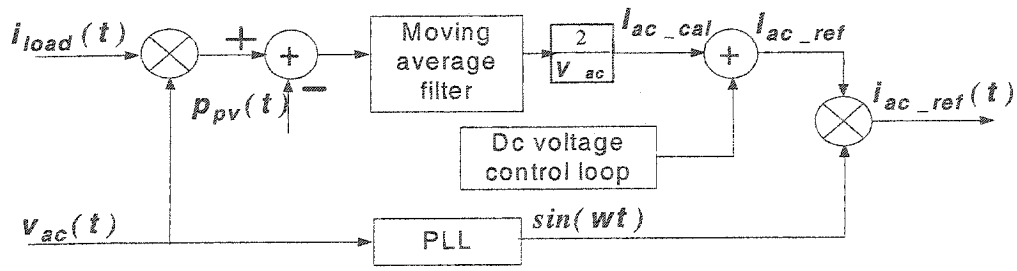

Figure 2.2: Calculation of the ac reference current

As shown in Fig.2.2, a moving average filter is used to calculate the magnitude of the net ac grid current, which is summed up with the output of the dc voltage control loop, yielding the magnitude of the ac grid reference current. Then, the result is multiplied by the output of the PLL, which is a sinusoid current template with unit magnitude in phase with the grid voltage, to obtain the reference current for the ac grid ($i_{ac\_ref}(t)$).

2.2.2. Estimation of the DC Bus Voltage Ripple

The main task of the inverter as an interface for a distributed power source is to control the active power injected into the grid so as to regulate the average value of the dc bus voltage. This is done by comparing the dc bus voltage, which contains low order harmonics (2nd, 4th ...) to a reference signal. The use of a small capacitor in the dc link imposes two serious requirements on the system:

1) The magnitude of the dc bus voltage ripple and low order components is substantially increased. They should not propagate through the inverter or they will distort the line current.

2) A dc bus voltage control loop with high bandwidth should be used to avoid large voltage variations (overshoots) that can damage the switches during transients.

The approach used in this paper to solve the first problem is to estimate and cancel the low order harmonics. This should allow, in principle, the use of a dc bus voltage control loop with higher bandwidth.

The dc bus voltage ripple in the steady state can be calculated from the power balance equation of the system solved for the instantaneous power supplied by the capacitor. The grid and inverter losses are neglected here since they are relatively small. Thus

$$\begin{aligned} p_C(t) &= p_{load}(t) - p_{ac}(t) - p_{PV}(t) + p_L(t) \\ &= -C\, v_{dc}(t) \frac{dv_{dc}(t)}{dt}. \end{aligned} \tag{2-4}$$

The voltage waveform at the dc bus can be defined by

$$v_{dc}(t) = V_{dc\_ref} + \nabla v_{dc}(t)\,. \tag{2-5}$$

The second term in the right hand side of (2-5) is the error between the reference and the actual capacitor voltage. In the steady state, it presents only ac components (ripple) assuming that the dc bus voltage control loop yields zero error for the average voltage. Since the reference value for the dc bus average voltage is larger than the voltage ripple, one can use the following approximation

$$p_C(t) = -C\, V_{dc\_ref} \frac{d\nabla v_{dc}(t)}{dt} \tag{2-6}$$

Therefore,

$$\nabla v_{dc}(t) = \frac{-1}{CV_{dc\_ref}} \int_0^t [p_{load}(t) - p_{ac}(t) - p_{PV}(t) + p_L(t)]dt \tag{2-7}$$

where

$$p_{load}(t) = v_{ac}(t)\, i_{load}(t) \tag{2-8}$$

$$p_{ac}(t) = v_{ac}(t)\, i_{ac}(t) \tag{2-9}$$

$$p_{PV}(t) = V_{dc\_ref}\, i_{PV}(t) \tag{2-10}$$

$$p_L(t) = \frac{d(0.5\, L_{inv}\, i_{inv}^2(t))}{dt} \tag{2-11}$$

There are a few issues that make the implementation of (2-7) difficult:

1) The integrator should start from the "zero" time instant to make sure that its output equals to $\nabla v_{dc}(t)$.

2) Since the inverter output current contains many harmonics, it is not practical to calculate $p_L(t)$ using a differentiator as defined in (2-11)

3) The measuring and calculating errors of $p_{load}(t)$, $p_{ac}(t)$, $p_{PV}(t)$ and $p_L(t)$ may cause the integrator output to be very large, exceeding the computer data processing range and making the implementation impractical.

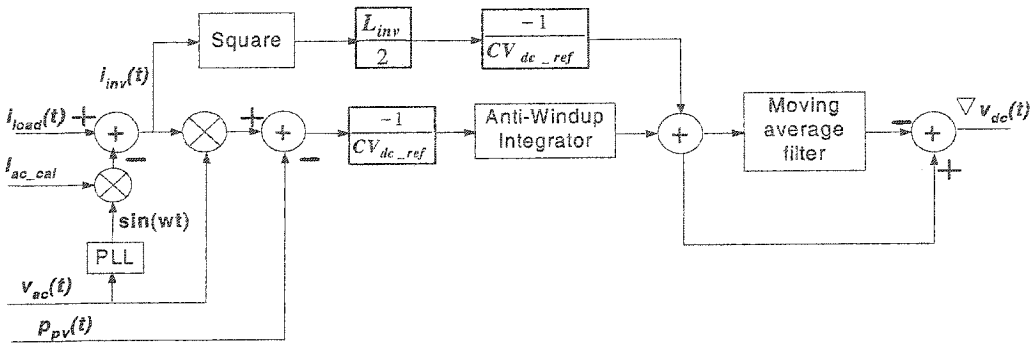

Figure 2.3. Dc bus voltage ripple estimator

Problem 1 can be solved by taking advantage of the fact that the dc capacitor voltage ripple $\nabla v_{dc}(t)$ should not contain any dc components in the steady state. Again, a moving average filter is used to obtain the dc bias component of the integrator output by calculating its average value over one line cycle (1/60 s). So $\nabla v_{dc}(t)$ can be obtained by subtracting the dc bias component from the integrator output as shown in Fig.2.3. Problem 2 can be solved by using the integrator in (2-7) to cancel the differentiator in (2-11). Problem 3 is overcome by using an anti wind up integrator with saturation limits set to ± 15 % of the dc bus reference voltage. This is the expected dc voltage ripple variation range in the steady state. Fig.2.4 compares the obtained voltage ripple from direct implementation of (2-7) with that from ripple estimator illustrated in Fig.2.3. The transient was caused by a step increase of the load at 0.1 s. The premier does not reflect the correct capacitor voltage ripple since it contains a positive dc bias before the step change and a negative dc bias after the step change, while the latter just contains the ac component which represents the capacitor voltage ripple. More details of the performance

of the dc bus voltage ripple estimator are presented in Chapter V, with other experimental results.

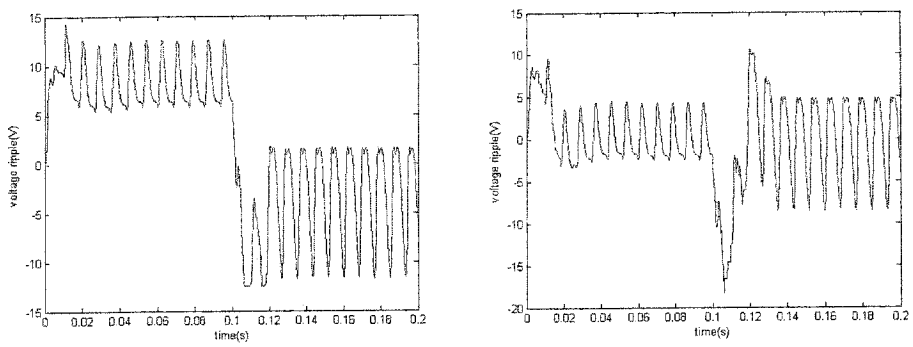

Fig.2.4. Dc capacitor voltage ripple. Left: response from direct implementation of (2-7). Right: response from ripple estimator illustrated in Fig.2.3

2.2.3. Design of the DC Bus Voltage Control Loop

The dc capacitor is a buffer for the reactive and harmonic power flow of the system. The fluctuation of the dc bus voltage is determined by the power balance of the system and can be expressed as

$$v_{dc}(t) = \frac{-1}{CV_{dc\_ref}} \int [p_{load}(t) - p_{ac}(t) - p_{PV}(t) + p_L(t)]dt \tag{2-12}$$

After Laplace transform, (2-12) becomes

$$v_{dc}(s) = \frac{p_{ac}(s) + p_{PV}(s) - p_{load}(s) - p_L(s)}{CV_{dc\_ref}S} \tag{2-13}$$

Fig.2.5 illustrates the dc bus voltage control loop. The dc bus voltage feedback signal is obtained by subtracting the estimated dc bus voltage ripple $\nabla v_{dc}(t)$ from the capacitor voltage signal $v_{dc}(t)$. A low-pass filter LPF is used in the feedback path to attenuate the residues of the ripple cancellation. The error between the reference and feedback signals

is processed by the controller to adjust the magnitude of the ac grid current so as to keep the average value of the dc bus voltage equal to the reference value.

The pulsating (time-varying) characteristics of the active power injected by the inverter into the ac grid ($\sin^2 \omega t$) make this system a periodic linear system, which can be approximated by an average equivalent [17], as shown in Fig.2.6.

The open loop transfer function is then given by

$$LTF(s) = \frac{K(1+s\tau)}{s\tau} \frac{V_{ac}}{2C\,V_{dc\_ref}\,s} \frac{\omega_l}{s+\omega_l}. \tag{2-14}$$

The cut-off frequency of the LPF is chosen as 60 Hz. The PI controller is designed so that one obtains a phase margin of 45.2° at a crossover frequency (bandwidth) of 40 Hz (248 rad/s), as illustrated in Fig.2.7. Appendix 2 illustrates the detailed design procedure for the PI controller.

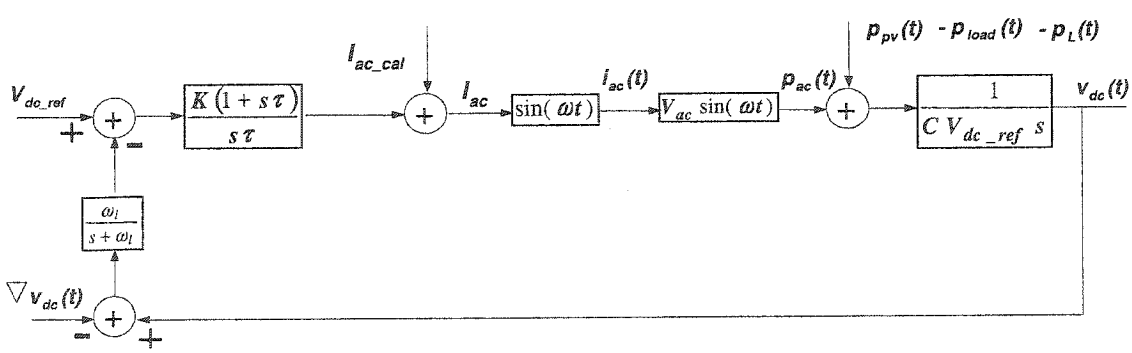

Figure 2.5. The voltage feedback control loop

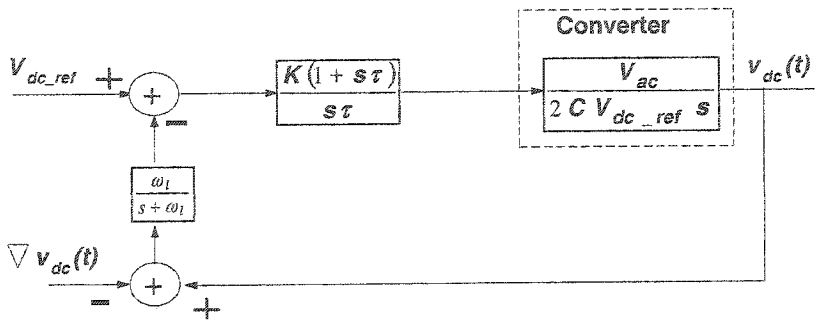

Figure 2.6. The simplified voltage feedback control loop

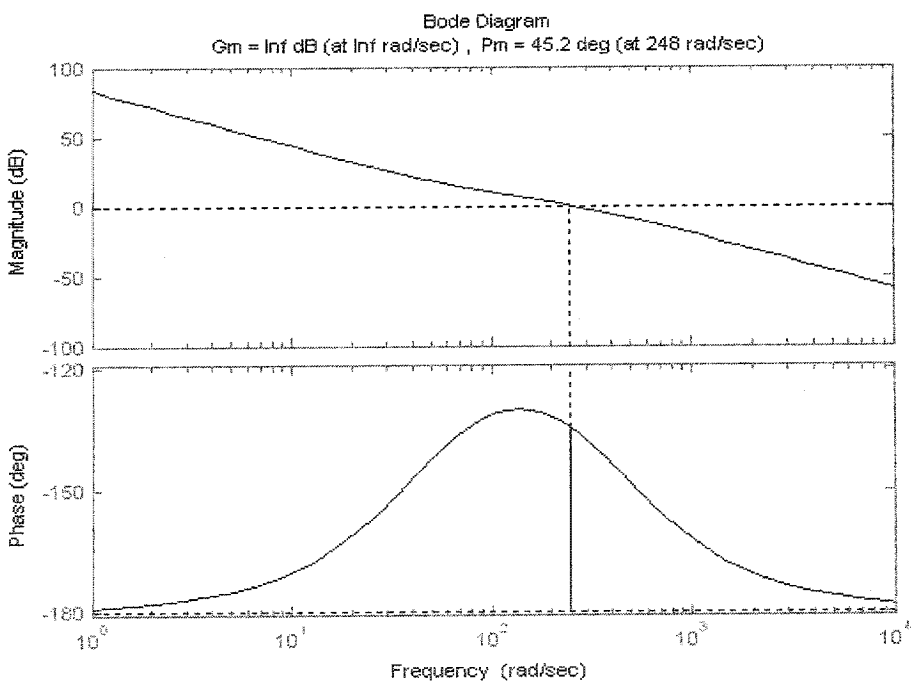

Figure 2.7. The bode diagram of the system

2.3. Conclusions

This chapter describes the proposed control scheme of a grid-connected PV system with additional features, namely reactive power compensation and active power filtering. These yield additional current components at the dc side of the inverter that tend to increase the voltage ripple. The usual approach for coping with the problem of dc bus voltage ripple by using large electrolytic capacitors is not adequate since these usually reduce system reliability. Instead, a voltage ripple cancellation technique is utilized in this thesis which enables the use of an even smaller capacitor in the dc bus. This way, one can prevent the propagation of the dc bus voltage harmonics through the inverter that would otherwise distort the ac side current of the inverter.

The main elements of the multi-featured grid interface have been introduced. The reference current generator for the inverter is designed to impose a grid current that is sinusoidal and in phase with the grid voltage. The inverter supplies all the reactive power required by the load and cancels the current harmonics. A dc voltage ripple estimator based on the power balance concept has been presented and solutions for some practical implementation problems have been discussed. Finally, this chapter discussed the modeling of the dc voltage feedback loop. A linearized average model has been presented and will be used for the design of a PI type controller. The DSP implementation, including the parameters design, experiment setup, as well as experimental result will be provided in Chapter 5.

3. SINGLE PHASE PHASE-LOCKED LOOP

3.1. Introduction

As discussed in Chapter 2, a phase-locked loop (PLL) is required to obtain the phase information of the ac grid voltage which is subject to harmonics, flicker and frequency variations. A PLL with a fast response speed, no steady-state error, a broad frequency acquisition range and excellent noise rejection plays an important role in the performance of the utility interface. Thus, this chapter details the design of a single phase PLL that satisfies all the above requirements.

The basic function of the PLL is to provide a sinusoidal signal that locks to the fundamental component of the ac grid voltage $u_{i(t)}$. Its structure is shown in Fig. 3.1. In a conventional PLL, the phase detector is made up of one multiplier, while relying on the low-pass filter to filter out the double and higher frequency harmonics in the output of the phase detector [18]. This is feasible for audio or higher frequency ranges, where the operating frequency is several thousands of Hz or more. In this case the harmonics can be easily filtered by a low-pass filter [19].

The nominal operation frequency of the power system, however, is a low 60 Hz and in application such as variable speed wind energy generation, the fundamental frequency of the output voltage of the generator can vary from 10 Hz to 90 Hz. To filter out all unwanted harmonics means that the low-pass filter has to have its cut-off frequency well below 20 Hz, twice the fundamental frequency. A low pass filter for 20 Hz is not only expensive to realize, but also conflicts with the requirements of the board frequency-acquisition range and fast response.

An alternative is to use a notched filter instead of a low pass filter to attenuate the harmonics created by the phase detector. However, this method is not feasible if the frequency of the PLL input signal is not fixed.

Another approach is to use a zero-crossing phase detector, which is easy to implement and will not create the double frequency harmonics [20]. However, the PLL response speed during the transient state is slow since the zero-crossing phase detector compares the phase difference once per line cycle. Besides, its noise rejection capability is poor and its performance is sensitive to switching-type transients.

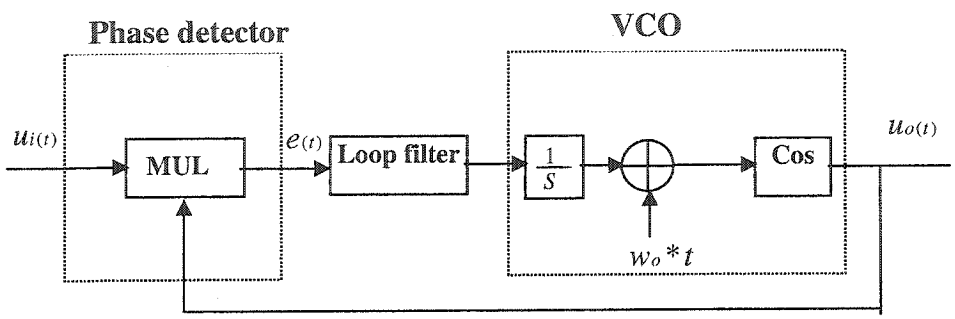

Figure 3.1. The conventional phase-locked loop

This thesis has developed a single phase PLL which uses a new phase detection scheme proposed by [6]. Its special phase detection scheme ensures the elimination of the second-order harmonic in the steady state. The new PLL system has fast response speed, good noise rejection performance, and zero steady state error. A detailed description of its operating principles, parameters design, as well as simulation and experimental results are discussed in the following sections.

3.2. Structure of the Phase-locked Loop

As shown in Fig.3.2, the PLL contains two loops. Loop 1 (the upper loop) consists of a phase detector (PD), a low pass filter (loop filter), and a voltage controlled oscillator (VCO). The VCO is comprised of an integrator, and two function generators (sine and cosine). The phase detector contains an adder and a multiplier. It compares the phase of the input signal $u_{i(t)}$ with that of the PLL output $u_{o(t)}$ and gives an error signal $u_{d1}(t)$, which passes through the low pass filter whose output $u_f(t)$ drives the VCO. The frequency of the VCO is $w = w_o + u_f(t)$, and w_o is the central frequency of the PLL. The phase of the PLL output $w_o t + \theta_o(t)$, is obtained after the integrator.

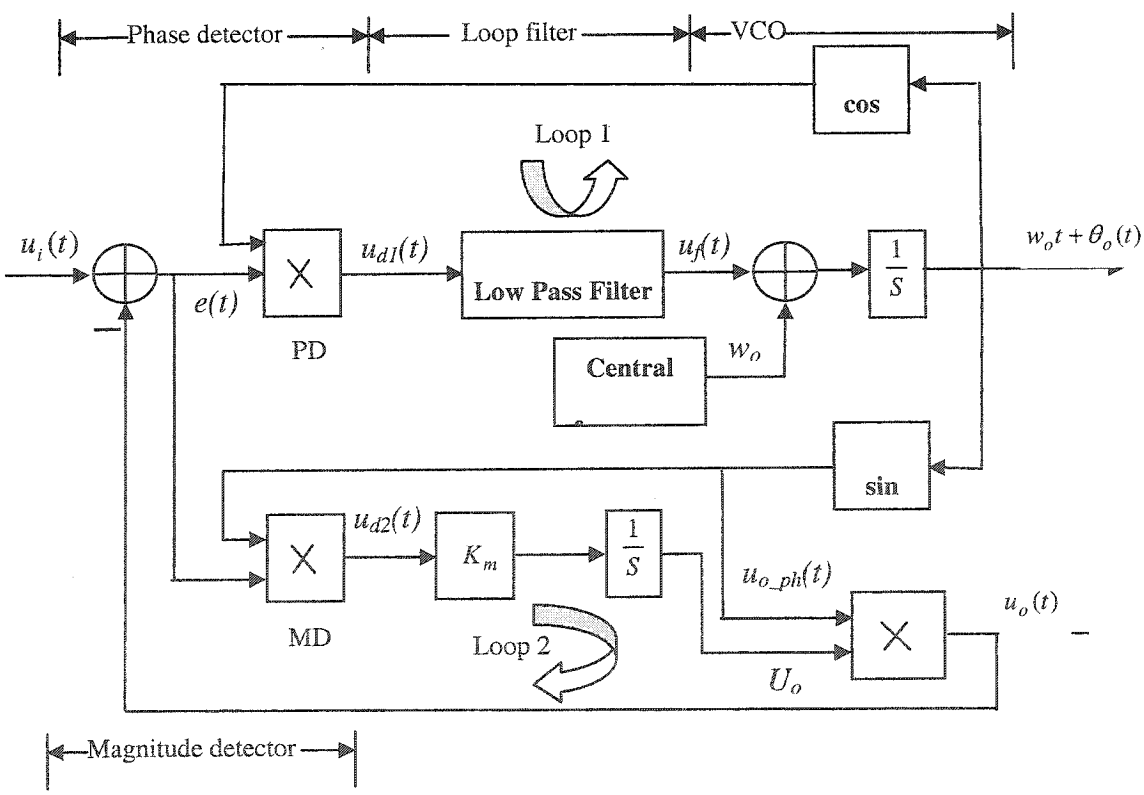

Figure 3.2. The new phase-locked loop block diagram

The second loop (loop 2) contains a magnitude detector, a gain K_m, an integrator, and a multiplier. The magnitude detector (MD) is composed of an adder (the same adder as the phase detector) and a multiplier. It compares the magnitude of the input signal with that of the PLL output and gives an error signal $u_{d2}(t)$ which passes through a gain K_m and an integrator. U_o . U_o , which equals the magnitude of the fundamental component of the input voltage U_i in the steady state, is obtained after the integrator. The output of loop1 ($u_{o\_ph}(t)$), is a sinusoid with unity magnitude. It is multiplied by the output of loop 2(U_o), gives out the PLL output

$$u_o(t) = U_o \sin(w_o t + \theta_o(t)) \tag{3-1}$$

3.3. Principles of Operation

The input signal is $u_i(t) = U_i \sin(w_i t + \varphi_i)$, which can also be expressed as

$$u_i(t) = U_i \sin(w_o t + \theta_i(t)) \tag{3-2}$$

where

$$\theta_i(t) = (w_i - w_o)t + \varphi_i \tag{3-3}$$

When the frequency of the input signal, w_i, equals the PLL central frequency w_o, $\theta_i(t)$ is a constant. Otherwise, $\theta_i(t)$ is a ramp signal.

Let $U_e = U_i - U_o$, $\theta_e(t) = \theta_i(t) - \theta_o(t)$, then the output of the adder can be expressed as

$$e(t) = u_i(t) - u_o(t) = U_i \sin(w_o t + \theta_i(t)) - U_o \sin(w_o t + \theta_o(t))$$

$$= U_i \sin(w_o t + \theta_i(t)) - U_i \sin(w_o t + \theta_o(t)) + U_e \sin(w_o t + \theta_o(t))$$

$$= 2U_i \sin(\frac{\theta_i(t) - \theta_o(t)}{2}) \cos(w_o t + \frac{\theta_i(t) + \theta_o(t)}{2}) + U_e \sin(w_o t + \theta_o(t)) \tag{3-4}$$

$$= 2U_i \sin(\frac{\theta_e(t)}{2}) \cos(w_o t + \theta_o(t) + \frac{\theta_e(t)}{2}) + U_e \sin(w_o t + \theta_o(t))$$

Since both loop 1 and loop 2 of the PLL are nonlinear and are difficult to analyze, simplifications should be made to obtain their linear models.

3.4. Linear Model of Loop 1

Loop 1 mainly tracks the phase of the input signal. Its structure is similar to that of a conventional PLL and will be discussed in detail in the following subsections.

3.4.1. Phase Detector

Considering (3-4), the output of phase detector can be expressed as

$$u_{d1}(t) = e(t)\cos[w_o t + \theta_o(t)]$$

$$= 2U_i \sin\left[\frac{\theta_e(t)}{2}\right] \cos\left[w_o t + \theta_o(t) + \frac{\theta_e(t)}{2}\right] \cos[w_o t + \theta_o(t)] + U_e \sin[w_o t + \theta_o(t)] \cos[w_o t + \theta_o(t)]$$

$$= U_i \sin\left[\frac{\theta_e(t)}{2}\right]\left(\cos\left[\frac{\theta_e(t)}{2}\right] + \cos\left[2w_o t + 2\theta_o(t) + \frac{\theta_e(t)}{2}\right]\right) + \frac{1}{2} U_e \sin[2w_o t + 2\theta_o(t)] \tag{3-5}$$

If we postulate that the PLL system stays locked at all times, the magnitude and the phase of the output signal, U_o and $\theta_o(t)$, should be close to that of the input signal U_i and $\theta_i(t)$. Then

$$\sin\left[\frac{\theta_e(t)}{2}\right] \approx \frac{\theta_e(t)}{2}$$

and $$\cos\left[\frac{\theta_e(t)}{2}\right] \approx 1 \tag{3-6}$$

Thus $u_{d1}(t)$ in (3-5) can be simplified as

$$u_{d1}(t) = \frac{1}{2}U_i\theta_e(t) + \left(\frac{1}{2}U_i\theta_e(t)\cos\left[2w_o t + 2\theta_o(t) + \frac{\theta_e(t)}{2}\right] + \frac{1}{2}U_e \sin 2(w_o t + \theta_o(t))\right) \tag{3-7}$$

The first term on the right hand side of (3-7) is the term that detects the phase error between the input signal and the PLL output. The second term is an ac component with very small magnitude, since the values of U_e and $\theta_e(t)$ are very small. Its effect can be ignored after being attenuated by the low pass filter of the loop. Finally, the output of the phase detector $u_{d1}(t)$ can be expressed as

$$u_{d1}(t) \approx \frac{1}{2}U_i\theta_e(t) \;=\; \frac{1}{2}U_i[\theta_i(t) - \theta_o(t)] \tag{3-8}$$

With (3-8), loop1 can be linearized and Fig.2.3 illustrates the linear model.

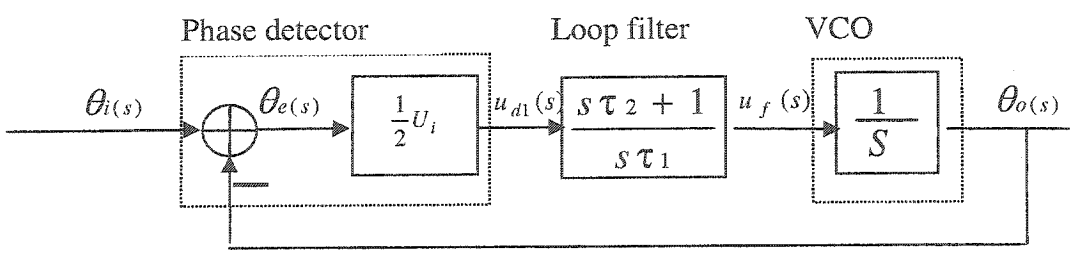

Figure 3.3. The linear model of loop 1 of the PLL

3.4.2. Loop Filter

Since the magnitude of the ac component after the phase detector is very small, the loop filter was designed to be a first-order low pass filter, which can be expressed as

$$\frac{u_f(s)}{u_{d1}(s)} = \frac{1+s\tau_2}{s\tau_1} \tag{3-9}$$

where $u_f(s)$ is the output signal, and $u_{d1}(s)$ is the input signal of the loop filter. It is easily seen that the loop filter is, in fact, a proportional-integral (PI) control element, where $K_p = \frac{\tau_2}{\tau_1}$, and $K_i = \frac{1}{\tau_1}$.

3.4.3 Voltage Controlled Oscillator

The input to the VCO is the output of the low pass filter $u_f(t)$, and its output can be expressed as

$$w_o t + \theta_o(t) = \int_0^t (w_o + u_f(\tau))d\tau \tag{3-10}$$

(3-10) can be simplified as

$$\theta_o(t) = \int_0^t u_f(\tau))d\tau \tag{3-11}$$

(3-11) illustrates that the VCO consists simply of an integrator. Its transfer function can be expressed as:

$$\frac{\theta_o(s)}{u_f(s)} = \frac{1}{s} \tag{3-12}$$

3.4.4. Closed Loop Transfer Function

According to Fig.3.3, the closed loop transfer function of loop1 is:

$$H_1(s) = \frac{\theta_{o(s)}}{\theta_{i(s)}} = \frac{\frac{U_i\tau_2}{2\tau_1}s + \frac{U_i}{2\tau_1}}{s^2 + \frac{U_i\tau_2}{2\tau_1}s + \frac{U_i}{2\tau_1}} = \frac{2\xi w_n s + w_n^2}{s^2 + 2\xi w_n s + w_n^2} \tag{3-13}$$

where

$$\tau_1 = U_i/2w_n^2 \text{, and } \tau_2 = 4\xi w_n \tau_1 / U_i = 2\xi / w_n \tag{3-14}$$

The damping factor ξ was selected to be 0.707 for an overshoot of less than 5% in the transient state. The selection of w_n is a compromise between the response speed and the noise rejection performance, and should be selected according to the requirements of a specific circuit design. In the prototype w_n is designed to be 251.2 rad/s (40 Hz). So the values of τ_1 and τ_2 are:

$$\tau_1 = U_i / 2w_n^2 = 0.000396, \text{and } \tau_2 = 2\xi / w_n = 0.0056$$

3.4.5. Steady state error

The error transfer function is

$$H_{e1(s)} = \frac{s^2}{s^2 + 2\xi w_n + w_n^2} \tag{3-15}$$

The Laplace transform of (3-3) yields

$$\theta_{i(s)} = \frac{(w_i - w_o)}{s^2} + \frac{\varphi_i}{s} \tag{3-16}$$

The steady state error is

$$\theta_{e(\infty)} = \lim_{s \to 0}(sH_{e1(S)}\theta_{i(s)}) = \lim_{s \to 0}\frac{s(w_i - w_o) + s^2\varphi_i}{s^2 + 2\xi w_n + w_n^2} = 0 \tag{3-17}$$

(3-17) shows that the PLL can track the input signal without any phase error in the steady state even when the frequency of the input signal is different than the central frequency of the PLL.

3.4.6. Frequency response

The open loop transfer function is

$$G_1(s) = \frac{U_i}{2}\frac{s\tau_2 + 1}{s\tau_1 \, s} \tag{3-18}$$

Fig.3.4 illustrates the open loop bode diagram. The phase margin is 65.3^{o}, which means that the PLL system is quite stable.

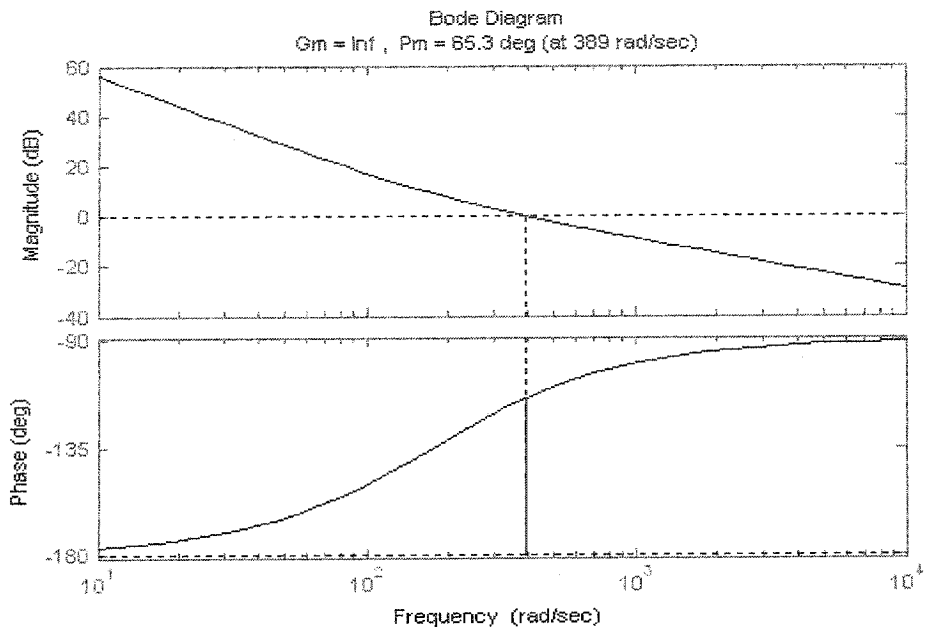

Figure 3.4. The Bode diagram of the open loop system of loop 1 of the PLL

3.5. Linear Model of Loop 2

The output of magnitude detector (MD) can be expressed as

$$u_{d2}(t) = e(t)\sin[w_o t + \theta_o(t)]$$

$$= 2U_i \sin\left[\frac{\theta_e(t)}{2}\right]\cos\left[w_o t + \theta_o(t) + \frac{\theta_e(t)}{2}\right]\sin[w_o t + \theta_o(t)] + U_e \sin[w_o t + \theta_o(t)]\sin[w_o t + \theta_o(t)]$$

$$= U_i \sin\left[\frac{\theta_e(t)}{2}\right]\left(\sin\left[2w_o t + 2\theta_o(t) + \frac{\theta_e(t)}{2}\right] - \sin\left[\frac{\theta_e(t)}{2}\right]\right) + \frac{1}{2}U_e\left(1 - \cos[2w_o t + 2\theta_o(t)]\right)$$

$$= \frac{1}{2}U_e - U_i \sin^2\left[\frac{\theta_e(t)}{2}\right] + \left(U_i \sin\left[\frac{\theta_e(t)}{2}\right]\sin\left[2w_o t + 2\theta_o(t) + \frac{\theta_e(t)}{2}\right] - \frac{1}{2}U_e \cos[2w_o t + 2\theta_o(t)]\right) \quad (3\text{-}19)$$

The first term on the right hand side of (3-19) is the term that detects the magnitude error between the input signal and the PLL output. The second term is caused by the phase error and should be equal to zero in the steady state, since $\theta_e(t)$ equals zero in the steady state, as proved in (3-17). The third term is an ac component and will be fully attenuated by the integrator of the loop since its magnitude is very small. Finally (3-19) can be simplified as

$$u_{d2}(t) \approx \frac{1}{2}U_e - U_i \sin^2\left[\frac{\theta_e(t)}{2}\right] \tag{3-20}$$

Fig.3-5 shows the linear model of loop 2. Here $U_i \sin^2(\frac{\theta_e(t)}{2})$ is considered as a disturbance and should be equal to zero in the steady state.

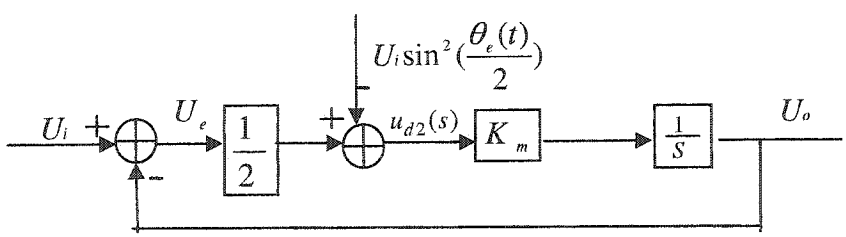

Figure 3.5: Linear model of loop2 of the PLL

The closed loop transfer function is

$$H_2(s) = \frac{U_{o(s)}}{U_{i(s)}} = \frac{\frac{K_m}{2s}}{1+\frac{K_m}{2s}} = \frac{1}{\frac{2}{K_m}s+1} = \frac{1}{\tau s+1} \tag{3-21}$$

Here, τ is the time constant and will determine the response speed of the system, and can be expressed as

$$\tau = \frac{2}{K_m} \tag{3-22}$$

In the prototype, time constant τ is designed to be 5 ms, which results in $K_m = \frac{2}{\tau} = 400$.

This value allows the system to reach a new steady state in one line cycle (1/60 s) after a step change of the magnitude of the input signal.

The error transfer function is

$$H_{e2(s)} = \frac{s}{s + \frac{K_m}{2}} \tag{3-23}$$

and the Laplace transform of U_i is $U_i(s) = \frac{U_i}{s}$

Hence the steady state error is

$$Ue = \lim_{s \to 0}(sH_{e2}(s)U_i(s)) = 0 \tag{3-24}$$

(3-24) indicates that the magnitude of the PLL output will track that of the input signal without steady state error.

3.6 Simulation and Experimental Results

The simulation results were obtained using Matlab Simulink. The experimental results of PLL were obtained with digital signal processing development kit DS1103 from dSPACE. The feature of the dSPACE development kit is discussed in Chapter 5.

3.6.1. Parameter Design

The magnitude of the input voltage U_i is 50 V. Fig.3.3 illustrates that loop 1 is a second order system and its characteristic will be determined by two parameters; τ_1 and τ_2. These two constants will uniquely define the damping ratio ξ and the natural frequency w_n of the system, as shown in (3-14). In the prototype, ξ is selected to be

0.707 for an overshoot of less than 5%, and w_n is designed to be 251.2 rad/s (40 Hz). The values of τ_1 and τ_2 are

$$\tau_1 = U_i / 2w_n^2 = 0.000396, \text{and}$$

$$\tau_2 = 2\xi / w_n = 0.0056 \, (k_p = 14.2, K_i = 2524)$$

Fig.3.5 shows that loop 2 is a first order system and its characteristics will be determined by K_m, which will uniquely define the time constant τ of the system. τ is designed to be 5 ms in the prototype, so that the system can reach a new steady state in one line cycle (1/60 s) after a step change of the magnitude of the input signal. According to (3-22),

$$K_m = \frac{2}{\tau} = 400 \tag{3-25}$$

3.6.2. PLL Performance Test

The PLL has been tested under different situations. A function generator (LFG 1300-C) is used to perform the noise rejection capability test. For other tests that require a step change of the input signal, only simulations results are provided since the function generator can not create the specific step change of the input signal as required.

3.6.2.1. Phase Step Change of the Input Signal

Fig.3.6 shows the response of the phase-locked loop when a phase step of 180° is applied to its input whose frequency is 60 Hz. The PLL exhibits fast response with no steady state error by re-tracking the input reference signal within two cycles of its input signal (0.018 s ~ 0.048 s). It is worth noting that the response speed is mainly determined by the natural frequency w_n, and hence can be increased by increasing its value. Note,

however, that a higher value of w_n will lead to weaker noise rejection capability of the system.

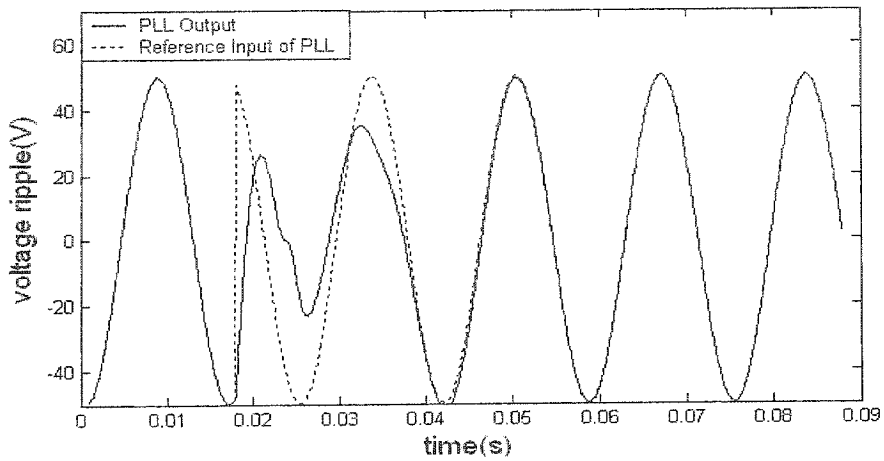

Figure 3.6. The simulated performance of the PLL to a phase step change of 180°

3.6.2.2. Frequency Step Change of the Input Signal

Fig.3.7 shows the response of the PLL when the frequency of the input signal change from 60 Hz to 100 Hz. Again, it demonstrates fast response speed by tracking the input in 22 ms (0.018 s ~ 0.0 4 s).

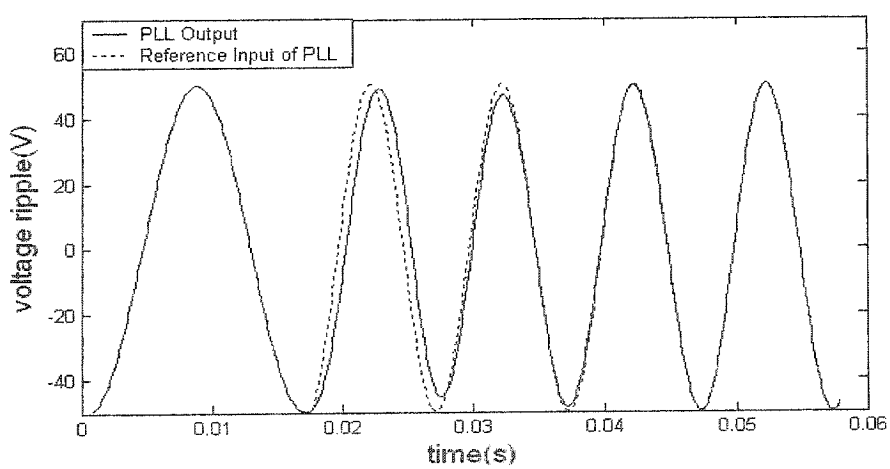

Figure 3.7. The simulated performance of the PLL to a frequency step change from 60 Hz to 100 Hz

3.6.2.3. Magnitude Step Change of the Input Signal

Fig.3.8 shows the response of the PLL when the magnitude of the input signal is a step from 50 V to 100 V (100%), whose frequency is 60 Hz. The PLL re-tracks the input signal in one line cycle (0.018 s ~ 0.034 s), which conforms to the design criteria given in (3-25).

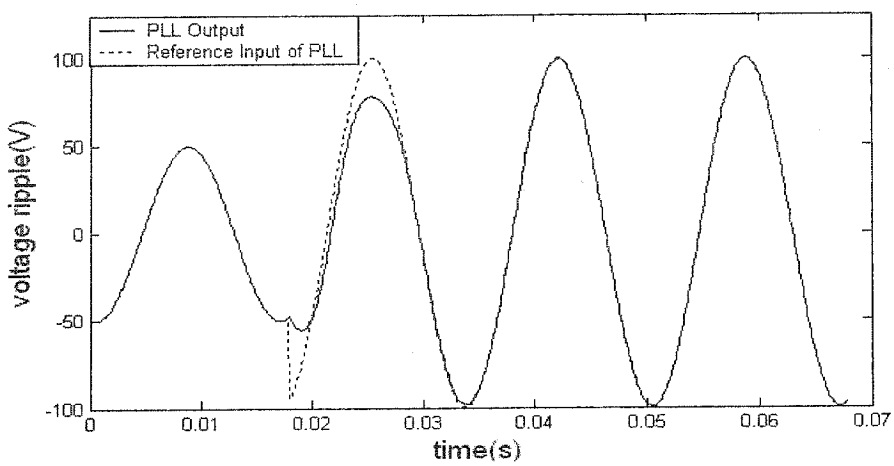

Figure 3.8. The simulated performance of PLL to a magnitude step change of 100%

3.6.2.4. Harmonic Rejection Capability

Usually it is much more difficult for a PLL to filter out the low order harmonics of the input signal than those of high order. Here a triangular waveform is used to verify the noise rejection feature of the PLL. It contains significant low order harmonics (11% 3rd, 4% 5th...). Fig.3.9 shows that the PLL can still extract its fundamental component, which means that the PLL can effectively attenuate the low order harmonics of the input signal and can be used in highly polluted environment.

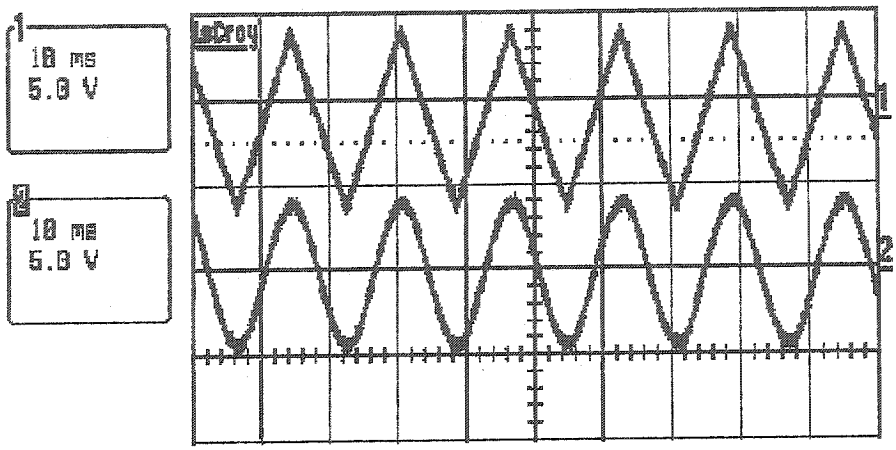

Figure 3.9. The experimental performance of the PLL under large noises; 1) input signal; 2) PLL output

3.7. Conclusions

The generation of the gating signals for the inverter switches requires a sinusoidal signal that is synchronized to the fundamental component of the grid voltage. The latter can present distortions due the presence of low and high order harmonics. The use of a low pass filter can attenuate the harmonics but would introduce an inherent delay in the synchronization signal. The best solution is the use of a phase lock loop (PLL).

This chapter has presented the operating principles and the detailed design procedure of a single-phase PLL with improved performance. It uses a new phase detector scheme to detect the phase errors between the input and the output signals of the PLL. This approach mitigates the problem of the second order harmonic that appears in the conventional PLL. This phase detector allows the use of an internal filter with higher bandwidth that results in a faster speed of response for the PLL with excellent phase tracking performance. Further, it presents a broader frequency acquisition range that

makes this device suitable for operation in wind power systems that operate with variable speed for maximum power capture by the wind turbine.

It was also shown that this PLL has very good noise rejection capabilities by effectively attenuating the low order harmonics of the input signal. Its ability to extract the fundamental component from a triangular input waveform proves that it can be used in highly polluted environments. Another advantage of this PLL is that it can obtain not only obtain the phase and frequency, but also the magnitude of the fundamental component of the input signal. Thus, its range of applications is wider than that of a conventional PLL.

4. THREE-LEVEL HYSTERESIS CURRENT CONTROL SCHEME

4.1. Introduction

There are many applications such as active filters and high-precision drives where a voltage source converter (VSC) needs to accurately impose a given set of current waveforms at the ac side. Typically, these currents have a large harmonic content and large derivative. This can be achieved with a current controlled inverter which presents a large bandwidth current control loop.

In general, current-controlled VSC schemes can be roughly classified into ramp comparison and hysteresis controllers [21]. The ramp comparison method, which yields a fixed switching frequency and superior harmonic characteristics, is the most commonly used one for power electronic systems. However, it can not obtain completely satisfactory quality of harmonic compensation in active power filter applications where fast tracking and high accuracy are required. This is because an inherent current tracking error exists, especially for the high frequency components of the reference current [4]. As an alternative, one can use hysteresis current controllers (HCC) that are well-known for their excellent transient response, inherent peak current limiting, and their stability and robustness under varying load conditions. However, the average switching frequency of basic two-level HCC is very high since at any switching instant, four switches of the bridge switch simultaneously.

It has been shown in [7, 8] that a three-level HCC can be implemented with the use of a zero-state when the inverter free-wheels the ac current The current controller proposed in [8] was implemented simply with two hysteresis comparators and two logic gates as shown in Fig.1. The main shortcoming of this control circuit is that the switching between the four switches of the bridge is not balanced. Two switches on one leg switch at about twice the average switching frequency, while the other two switches operate at a very low (line) frequency. This is shown in Fig.4.2 for a sinusoidal reference current.

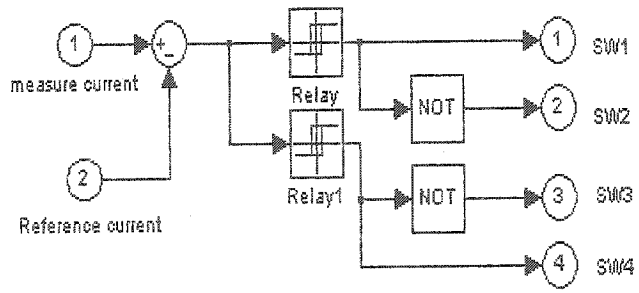

Fig. 4.1. Three-level hysteresis current controller

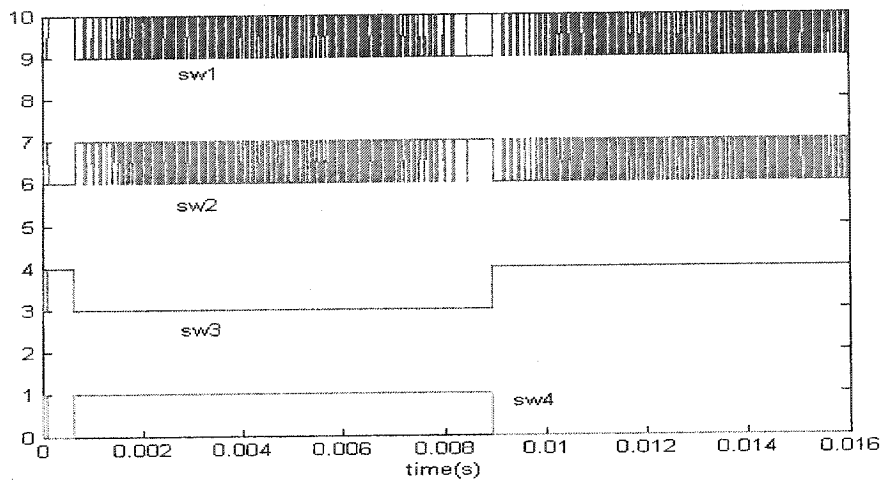

Fig. 4.2. Switching pattern of the controller shown in Fig. 4.1.

The current controller proposed in [7] utilizes two hysteresis bandwidths which are overlapped and displaced by a small dc offset. It balances the switching between the four switches by ensuring opposite zero conditions (00 or 11) between any neighboring inverter zero states. However, the control circuit needs to compensate for a resulting dc offset error which will otherwise increase the THD of the ac side current. The compensator used in [7] was implemented with an adder and an analog switch which increased the complexity and the cost of implementation.

This chapter proposes a three-level hysteresis current controller which uses two hysteresis comparators to compare the current error with the inner and the outer hysteresis boundaries. Unlike [7], where the inverter output will be set to the zero state whenever the current error reaches the inner boundary, here it will be decided by the previous inverter state. If the previous state is positive or negative, then the inverter

output will be set to zero state. Otherwise, it will be set to be positive or negative state, depending on whether the upper boundary or the lower boundary has just been crossed. In this way, the dc offset error can be avoided and a simple three-level single-phase hysteresis controller can be implemented with just two hysteresis comparators, one D flipflop, and a few logic gates. Alternatively, the proposed logic can be implemented with field programmable gate arrays (FPGA) by simply writing the VHDL code.

The operating principles and the calculation of the instantaneous and average switching frequencies for the two-level and three-level hysteresis current control schemes are presented in sections 4.2 and 4.3, respectively. A new control circuit for a three-level HCC is presented in section 4.4. The verification of the feasibility of the proposed three-level hysteresis controller has been done with an active power filter in section 4.5. It is intended to compensate the current harmonics of a highly non-linear load where fast response speed and good accuracy are mandatory. Finally, the superior performance of three-level hysteresis controller with respect to a two-level scheme is demonstrated with experimental results.

4.2. Conventional Hysteresis Control Scheme

Fig. 4.3 shows a full-bridge single-phase voltage source converter (VSC). The switching states for the inverter legs S_A and S_B are defined according to the state of the top switch of each leg. If U_A is ON, S_A is 1, otherwise it is 0. Similarly, if U_B is ON, S_B is 1, otherwise it is 0. The bottom switch of each leg operates as a complement to the top leg switch to prevent a dc bus short-circuit.

Fig. 4.4 illustrates the current trajectory of the conventional (two-level) hysteresis current controller, where the converter always switches between the positive state (S_A, S_B = 0, 1) and the negative state (S_A, S_B = 1, 0) to drive the output current to move between the upper hysteresis band ($i_{ref}+h$) and the lower band ($i_{ref}-h$).

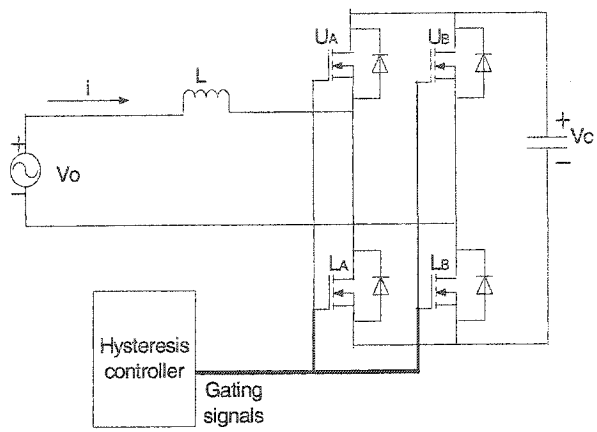

Fig. 4.3. VSI schematic diagram.

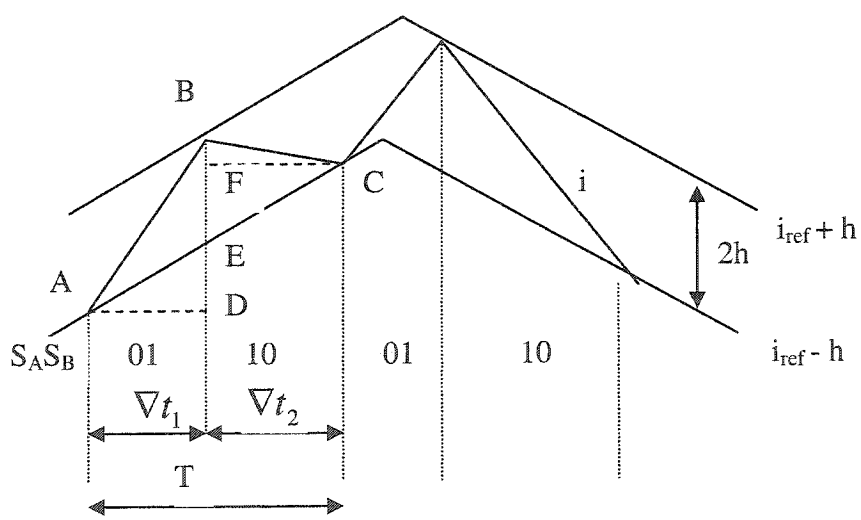

Fig. 4.4. Current trajectory of the conventional hysteresis current controller

According to [22], the expression for the instantaneous switching frequency of the two-level HCC can be obtained using the following approach.

The gradient of trajectory AB can be expressed as

$$\frac{di}{dt} = \frac{v_o + v_c}{L} = \frac{BD}{AD} = \frac{BE + ED}{AD} = \frac{2h + \nabla t_1 \dfrac{di_{ref}}{dt}}{\nabla t_1} \tag{4-1}$$

So

$$\nabla t_1 = \frac{2hL}{v_c + v_o - L\frac{di_{ref}}{dt}} \tag{4-2}$$

Along the trajectory BC

$$\frac{di}{dt} = \frac{v_o - v_c}{L} = \frac{-BF}{FC} = \frac{-(BE - FE)}{FC} = \frac{-(2h - \nabla t_2 \frac{di_{ref}}{dt})}{\nabla t_2} \tag{4-3}$$

and

$$\nabla t_2 = \frac{2hL}{v_c - (v_o - L\frac{di_{ref}}{dt})} \tag{4-4}$$

Thus the period of one switching cycle is

$$T = \nabla t_1 + \nabla t_2 = \frac{4hLv_c}{v_c^{\ 2} - (v_o - L\frac{di_{ref}}{dt})^2} \tag{4-5}$$

The instantaneous switching frequency of the converter is

$$f_{2level} = \frac{v_c^{\ 2} - (v_o - L\frac{di_{ref}}{dt})^2}{4hLv_c} \tag{4-6}$$

At all switching instants, all four switches commutate simultaneously, so the switching frequency of each of them is the same as that of the converter. When $v_o - L\frac{di_{ref}}{dt}$ equals zero, the converter has the maximum instantaneous switching frequency

$$f_{2level\_\max} = \frac{v_c}{4hL} \tag{4-7}$$

Alternatively, when $\left| v_o - L\frac{di_{ref}}{dt} \right| > v_c$, the value of f_{2level} in (4-6) becomes negative which means that there will be a distortion in the ac side current, *i*. This is because the voltage across the inductor *L* is not large enough to force the converter output current, *i*, to track the reference current i_{ref} at this moment. Hence in the design process, the capacitor voltage v_c and the converter inductor *L* should be chosen carefully to make

sure $\left| v_o - L\frac{di_{ref}}{dt} \right| < v_c$. This statement also applies for the three-level hysteresis current controller in the next section.

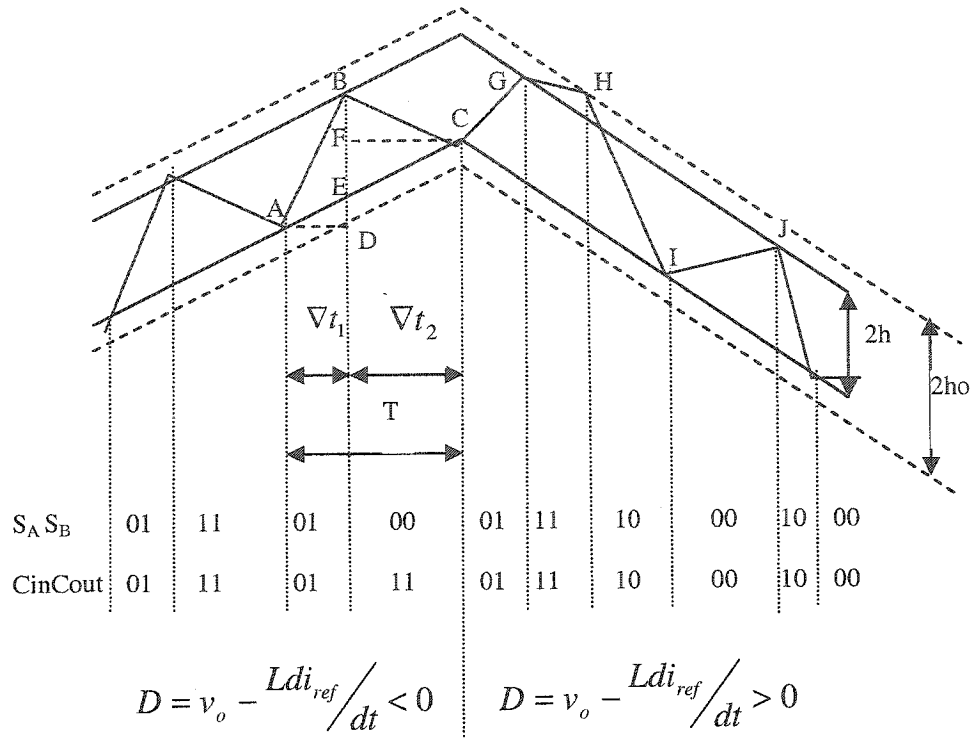

Fig. 4.5. Current trajectory of the proposed three level HCC

4.3. Three-Level Hysteresis Current Controller

In addition to the positive state (S_A, S_B=0, 1) and the negative state (S_A, S_B=1, 0), the three-level hysteresis current controllers also utilize the zero state (S_A, S_B=0, 0 or 1, 1). In this state, the converter flywheels the converter current i whose gradient is only determined by the voltage v_o, and D = $v_o - L\frac{di_{ref}}{dt}$ determines whether the converter current i moves toward the upper hysteresis bound or the lower hysteresis bound. As shown by trajectory IJ in Fig.4.5, during the zero state, the trajectory of converter current

i will move towards the upper bound (i_{ref} + h) when $D > 0$, since the gradient of the converter current i is bigger than that of the reference current i_{ref}. It is worth noting that this statement applies even when $v_o < 0 \; and \; L\frac{di_{ref}}{dt} < 0$, as illustrated by trajectory GH. Similarly, i will move towards the lower bound (i_{ref} - h) during the zero state when $D < 0$, as illustrated by trajectory BC.

4.3.1. Three-Level HCC Logic

The proposed three-level hysteresis control logic starts with four initial conditions:

- When the ac side current crosses the inner upper hysteresis boundary (i_{ref} + h), if the converter is in the positive state (S_A, S_B = 0, 1), the converter will be set to the zero state (as shown in point B and point G in Fig. 4.5.). Otherwise, the converter will be set to the negative state (S_A, S_B = 1, 0, as shown in point J in Fig. 4.5.).
- Whenever the output current cross the inner lower hysteresis boundary (i_{ref} - h), if the converter is in the negative state (S_A, S_B = 1, 0), the converter will be set to the zero state (as shown in point I in Fig. 4.5.). Otherwise, the converter will be set to the positive state (S_A, S_B = 0, 1, as shown in point A and point C in Fig. 4.5.).
- Whenever the output current reaches the outer upper hysteresis boundary (i_{ref} + ho), the converter will be set to negative state (S_A, S_B = 1, 0, as shown in point H in Fig. 4.5.).
- Whenever the output current reaches the outer lower hysteresis boundary (i_{ref} - ho), the converter will be set to positive state (S_A, S_B = 0, 1).

It is worth noting that the converter has two zero states: $S_A, S_B = 0, 0$ and $S_A, S_B = 1, 1$, and they should occur alternatively. In other words, the converter should output '00' if the previous zero state is '11', and vice versa. In this way, the switching between the four switches will be balanced.

4.3.2. Switching Frequency of the Three-Level HCC

Obviously only two switches need to switch simultaneously when the converter changes between the zero state and the positive state, or between the zero state and the negative state. The instantaneous and the average switching frequency of this scheme should be reduced by about 50% when compared with the conventional two-level HCC since the latter requires the converter to switch between the positive state and negative state and all four switches need to switch simultaneously. In addition, the absolute value of the gradient of current i in the zero state is usually much smaller than that in the positive state or negative state and it will take longer for the converter current i to move between the upper and lower hysteresis boundaries. Experiment result shows that the length of one period of the three level HCC is about twice that of the conventional two level HCC at the same condition. Thus the switching frequency can be reduced by another 50%. An expression for the maximum instantaneous switching frequency of the three-level HCC can be obtained as follows.

When $D < 0$, along trajectory AB, the gradient of the ac side current is

$$\frac{di}{dt} = \frac{v_o + v_c}{L} = \frac{BD}{AD} = \frac{BE + ED}{AD} = \frac{2h + \nabla t_1 \dfrac{di_{ref}}{dt}}{\nabla t_1} \tag{4-8}$$

So that

$$\nabla t_1 = \frac{2hL}{v_c + v_o - L\dfrac{di_{ref}}{dt}} = \frac{2hL}{v_c - \left|v_o - L\dfrac{di_{ref}}{dt}\right|} = \frac{2hL}{v_c - |D|} \tag{4-9}$$

Along trajectory BC, the gradient of the ac side current is

$$\frac{di}{dt}=\frac{v_o}{L}=\frac{-BF}{FC}=\frac{-(BE-FE)}{FC}=\frac{-(2h-\nabla t_2\frac{di_{ref}}{dt})}{\nabla t_2} \tag{4-10}$$

Thus

$$\nabla t_2=\frac{2hL}{-(v_o-L\frac{di_{ref}}{dt})}=\frac{2hL}{\left|v_o-L\frac{di_{ref}}{dt}\right|}=\frac{2hL}{|D|} \tag{4-11}$$

The time period T is

$$T=\nabla t_1+\nabla t_2=\frac{2hLv_c}{|D|(v_c-|D|)} \tag{4-12}$$

(4-12) is also valid when $D>0$, and the analysis is similar.

The equivalent switching frequency of the converter is

$$f_{3level\_inv}=\frac{|D|(v_c-|D|)}{2hLv_c} \tag{4-13}$$

Since only two switches switch simultaneously at any switching moment, the switching frequency of the switch is

$$f_{3level}=\frac{|D|(v_c-|D|)}{4hLv_c} \tag{4-14}$$

Combining (4-6) and (4-14) yields a ratio

$$\frac{f_{3level}}{f_{2level}}=\frac{|D|}{v_c+|D|} \tag{4-15}$$

(4-15) compares the instantaneous switching frequency between the three level HCC and that of the two level HCC. The value of $|D|$, which is an ac component and varies according to the values of v_o and i_{ref}, should be smaller than v_c. Otherwise, there will be a distortion in the converter ac side current i since the voltage across the inductor L is not big enough to force the converter ac side current i to track the reference current i_{ref}. This has been previously discussed in section 4.2. Thus the result of (4-15), should be less than 0.5, which means that the instantaneous switching frequency of three level HCC should be at least 50% less than that of two level HCC. Simulation and experimental results

show that the average value of (4-15) over one line cycle (1/60 s) is about 0.3. Finally, When $|D| = \frac{v_c}{2}$, the converter has the maximum switching frequency as:

$$f_{3level\_\max} = \frac{v_c}{16hL} \tag{4-16}$$

Comparing (4-7) and (4-16), one sees that the maximum switching frequency of the proposed three-level HCC is only one fourth of that of the conventional two-level HCC.

4.4. Implementation of the Three Level HCC

Fig. 4.6 shows the proposed control circuit for a three-level HCC. Two hysteresis comparators (comp_in and comp_out) compare the current error with the inner boundary and the outer boundary, respectively. The comparators are configured in this way: Cin changes to "1" when the current error reaches the inner upper hysteresis boundary, and changes to "0" when the current error reaches the inner lower hysteresis boundary. Cout changes to "0" when the current error reaches the outer upper hysteresis boundary, and changes to "1" when the current error reaches the outer lower hysteresis boundary, as illustrated in Fig.4.5. Obviously the transition of Cin between 0 and 1 is much more frequent than that of Cout. In order to balance the switching, a D flip flop along with a few logic gates are utilized to ensure that opposite zero states will appear alternately. When the comparator outputs (Cin, Cout) are 0, 1 or 1, 0, the XOR logic gate will output 1 and the gating signals for UA and UB will be equal to the values of Cin and Cout, respectively. When the comparator outputs (Cin Cout) are 0, 0 or 1, 1, the XOR logic gate will output 0 and the gating signals for UA and UB will be equal to the output of the D flip flop. The clock input for the D flip flop comes from the XOR logic gate output (K), thus ensuring that the D flip flop will toggle each time when the inverter output changes from a zero state.

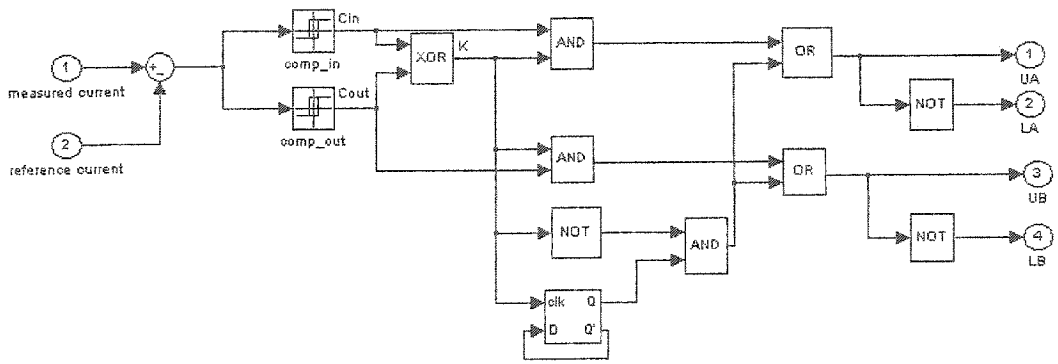

Fig. 4.6. Proposed control circuit for three-level HCC.

The proposed three-level hysteresis current controller was tested as shown in Fig. 4.3 by simulation using Matlab. The circuit operated as a static var compensator supplying reactive power. The reference current was a sinusoidal signal that leads the source voltage waveform by 90°. The switches were modeled as ideal devices so there was no need for dead time circuits. Fig. 4.7 shows the gating signals generated for each switch. Unlike Fig. 4.2, here one sees that the gating signals are balanced. This means that the switching balance circuit works as expected and opposite zero states appear alternately.

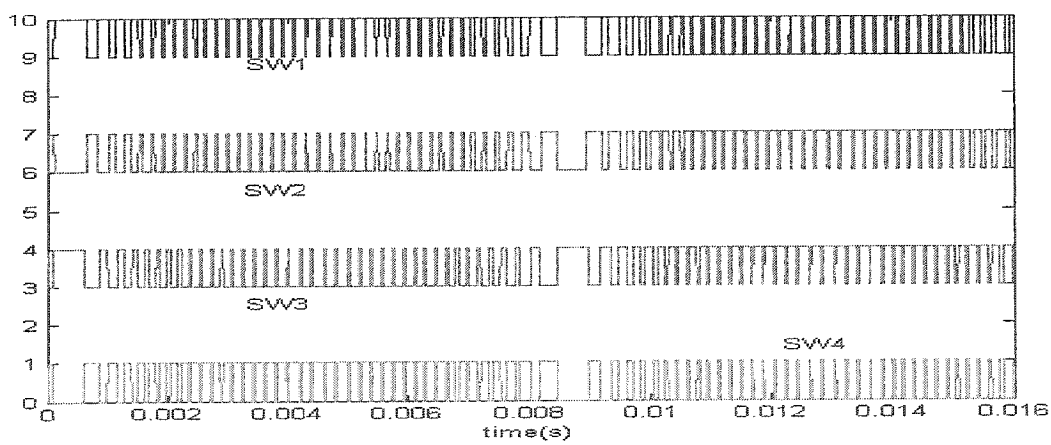

Fig. 4.7. Gating signals for the four switches of the inverter.

4.5. Experimental Results

A laboratory prototype test system was built to verify the performance of the proposed three-level HCC in a practical circuit. An IGBT bridge without snubber circuits was used to implement the VSC and a standard dead time circuit realized with diodes and RC components was included to prevent dc bus short-circuits through the real switches.

The ac current waveform seen in the oscilloscope presented oscillations after each switching of the inverter that were brief (3 μs) but large (1 A) enough to cause a malfunction of the HCC. Recall that the inner and outer hysteresis boundaries were selected as 0.4 and 0.5 A respectively. This explains why the comparators gave out unexpected results, which deteriorated the performance of the three-level HCC. One alternative solution is to include a circuit in the output of the comparators that prevents the oscillatory signal of the comparators from propagating though the controller. This can be done by holding constant the output signal of the comparators for the estimated oscillation time after each transition. However, the implementation of this logic, that is not the inclusion of a simple monostable multivibrator, will make the above-mentioned analog circuit more complicated.

Therefore, a field programmable gate array (FPGA) was chosen to implement the proposed three-level HCC, including the dead-time circuits for the switches. The major advantage of FPGA implementation over analog circuit implementation is that the implementation can be easily modified, maintained and upgraded. By rewriting the VHDL code, the length of the hold-time and of the dead-time can be easily adjusted according to the power level of the converter and type of switches. Appendix 3 illustrates the flow diagram of the three-level HCC. The source code is shown in Appendix 4. Since there are two zero states ($S_A, S_B = 0, 0$ or $1, 1$), the variable S_Z is introduced to ensure that the opposite zero state occurs alternatively to balance the phase leg switching.

$$S_Z = 1: \text{ when the previous zero state is } S_A, S_B = 1, 1 \qquad (4\text{-}17)$$

$$S_Z = 0: \text{ when the previous zero state is } S_A, S_B = 0, 0$$

Since the FPGA development kit in the prototype does not contain suitable AD converters, it can not sample the converter current i and the reference current i_{ref} directly. In order to solve the problem, four comparators (LM339A) have been utilized to compare the converter current i with the hysteresis current boundaries.

Their outputs, which are digital signals, become the input of the FPGA, as shown in the diagram of Appendix 1.

As mentioned in [7], the minimum possible difference between the inner and the outer boundaries is primarily determined by the dead-time of the inverter switches and can be calculated as

$$\Delta h = ho - h = \frac{Vc}{L} deadtime \tag{4-18}$$

Where Vc is the dc bus voltage, and L is the inverter inductance. The hysteresis controller was used in the active power filter which requires a fast, accurate response in order to compensate for the reactive power and harmonic components of the highly non-linear load current. Fig.4.8 shows the circuit diagram of an active power filter.

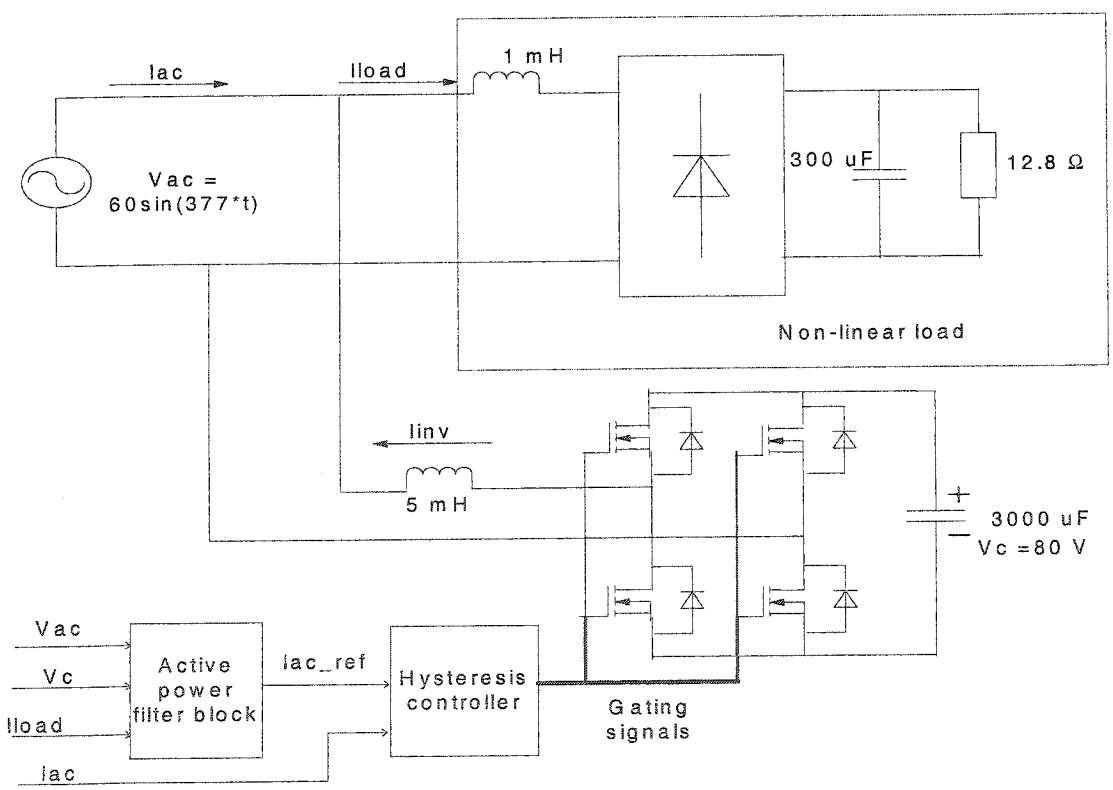

Figure 4.8: Schematic diagram of the active power filter

In the prototype circuit, a digital signal processing (DSP) development kit (DS1103 from dSPACE) was used to implement the control scheme of the active power filter. The DSP created the reference signal for the ac grid current which was sinusoidal and in phase with the ac grid voltage. A Xilinx FPGA (Spartan II ELC) was used to implement the hysteresis controller which also contained the hold-time and the dead-time logic. The clock frequency of the FPGA was 780 kHz, and the hold time after each switching action was equal to three clock cycles (3.84 μs). The dead time was one clock cycle (1.28 μs).

The experimental results shown in Fig.4.9 to Fig.4.13 allow the comparison of the performance of the proposed three-level HCC with that of the conventional two-level HCC.

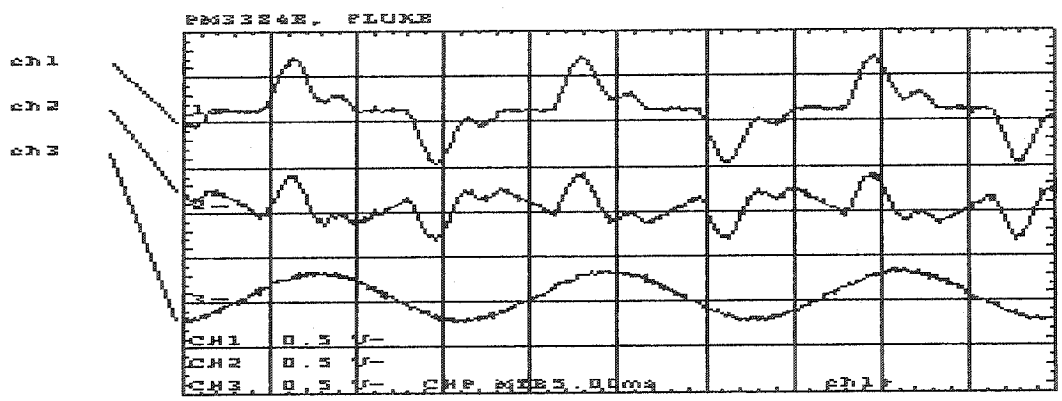

Figure 4.9. The current waveforms of the three level HCC. The average switching frequency = 1500 Hz, bandwidth h = 0.4 A, and ho = 0.5 A; ch1) Load current; ch2) Converter output current; ch3) Ac grid current

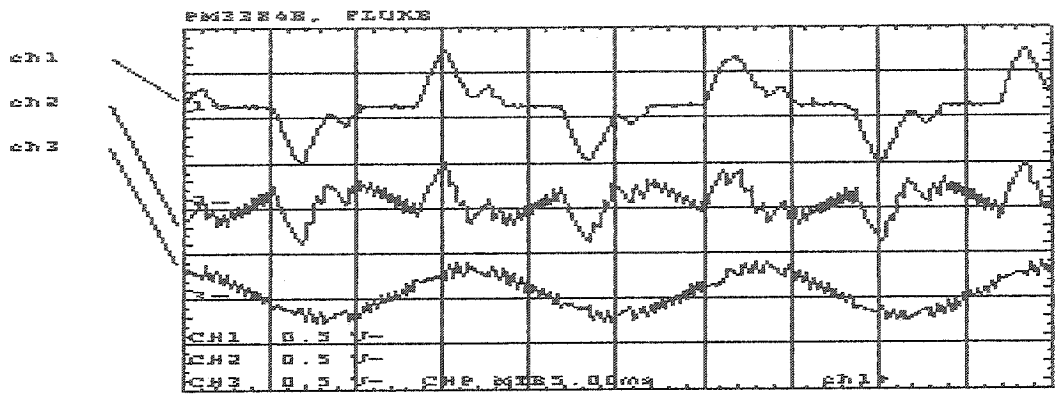

Figure 4.10. The current waveforms of the two level HCC. The average switching frequency = 1500 Hz, bandwidth h = 1.5 A; ch1) Load current; ch2) Converter output current; ch3) Ac grid current

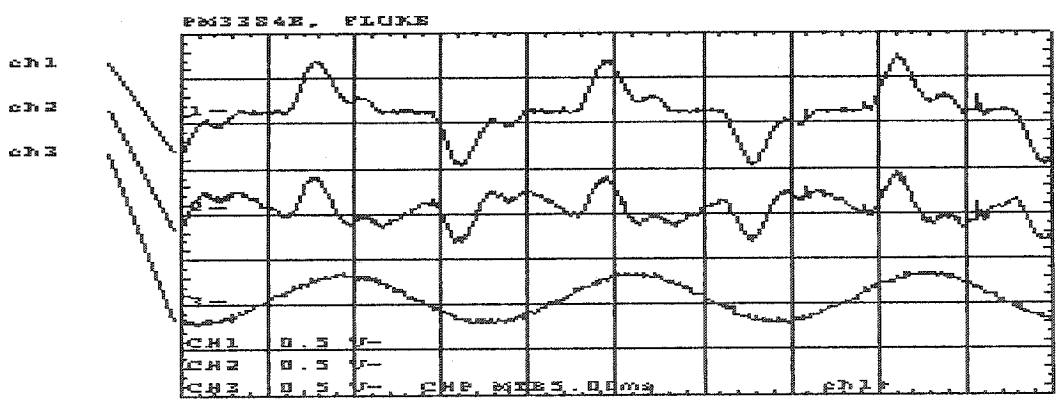

Figure 4.11. The current waveforms of the two level HCC. The average switching frequency = 5800 Hz, bandwidth h = 0.4 A; ch1) Load current; ch2) Converter output current; ch3) Ac grid current

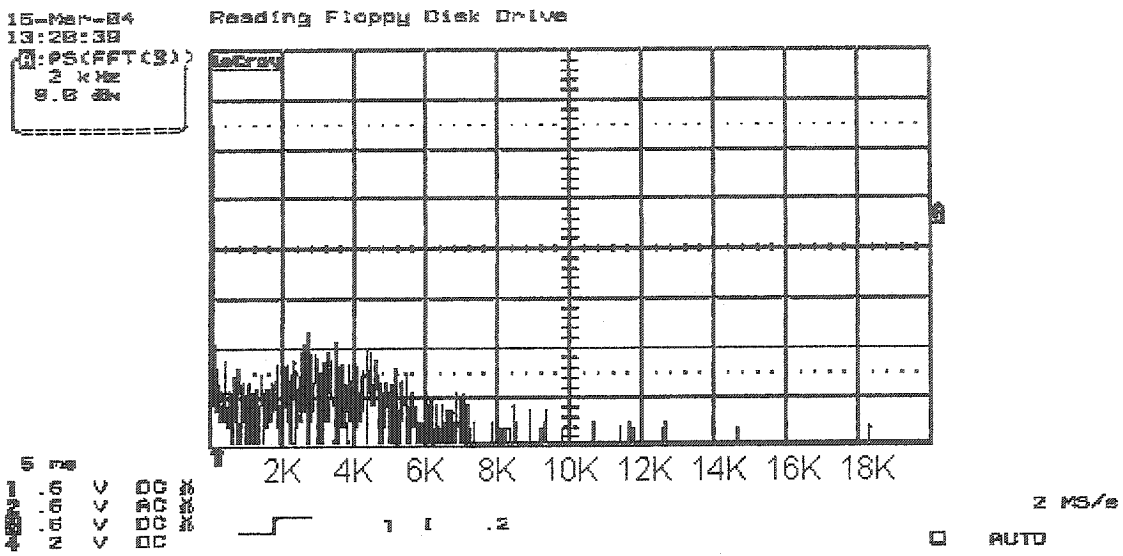

Figure 4.12. The harmonic spectrum of the three level HCC. The average switching frequency = 1500 Hz, bandwidth h = 0.4 A, ho = 0.5 A

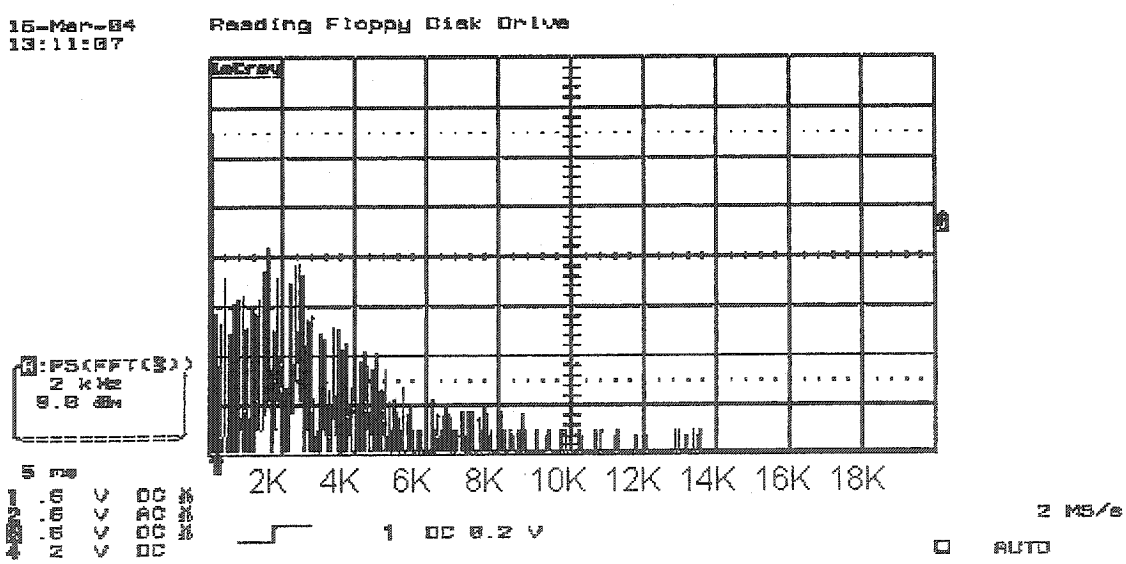

Figure 4.13. The harmonic spectrum of the two level HCC. The average switching frequency = 1500 Hz, bandwidth h = 1.5 A

Comparing Fig.4.9 with Fig.4.10, one sees that the proposed controller can results in much better performance at the same switching frequency (bandwidth h = 0.4 A v.s. h = 1.5A)

Comparing Fig.4.9 with Fig.4.11, one sees that the proposed three level HCC can significantly reduce the switching frequency for the same output performance. (f = 1500 Hz vs. 5800 Hz)

Comparing Fig.4.12 with Fig.4.13, one sees that three level HCC can significantly reduce the harmonics level at the same switching frequency. The harmonic spectrum also shows that the harmonic of the converter output concentrates on twice the average switching frequency for the three level HCC, while concentrates on the average switching frequency for the two level HCC. This means that the three level HCC effectively 'doubles' the switching frequency.

4.6 Conclusions

In this chapter, a three-level HCC was proposed that utilizes the zero state of the converter and results in significant switching frequency reduction. Its superior performance over the conventional two level HCC has been verified by experimental results. The three level HCC has three advantages:

1) It has very fast response speed and good accuracy, which enable it to easily compensate for the high order harmonics of a non-linear load current.

2) Compared with the conventional two-level HCC, it greatly reduces the switching frequency (1.5 kHz versus 5.8 kHz) for the same performance, thus resulting in substantial reduction of switching losses. At the same switching frequency, it yields much better output waveforms and greatly reduces the harmonic level.

3) The implementation of the proposed control circuit is simpler than that previously described in the literature. It employs two hysteresis comparators, one flip flop type D and a few logic gates.

This chapter also presents another way to implement the proposed HCC, together with the time delay logic and the dead time logic by utilizing FPGA. The advantage of FPGA implementation is that it can easily realize complicated logic by writing the VHDL code, and its price is becoming more and more affordable (A 100,000 gate XC2S100 family member FPGA costs $10 [23]. It should be noted that the implementation of the proposed three-level HCC only uses 800 gates).

5. DSP IMPLEMENTATION AND EXPERIMENT RESULT

5.1. Introduction

The circuit used for the verification of the proposed utility interface for distributed resources is the one shown in Fig.5.1. A solar array simulator (Agilent E4350B) operating in the constant current mode emulates the dc-dc MPPT converter and PV array. It allows step variations of the current injected into the dc bus to verify the response of the system to variations of the PV generation. The full-bridge voltage source inverter was implemented with an IGBT module (CM50MD-12H). A DSP development kit DS-1103

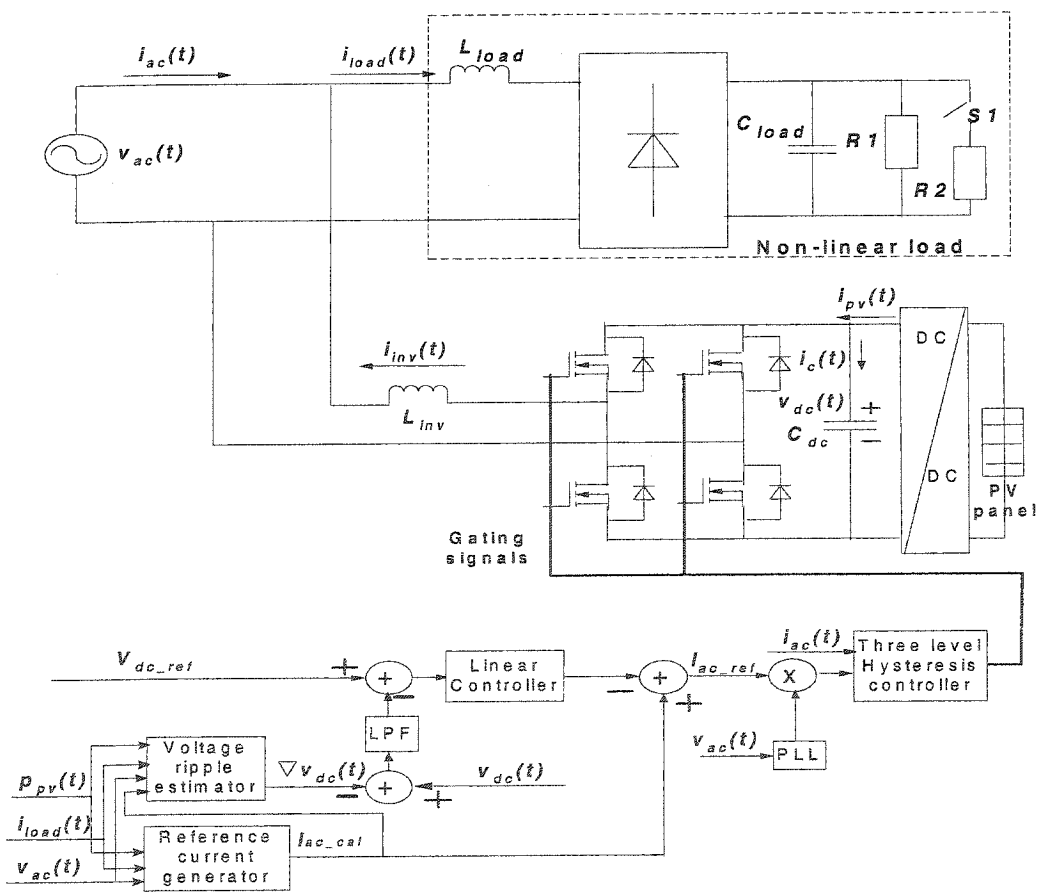

Fig.5.1. Grid-connected PV system

from dSPACE was employed to implement the control circuit, which includes the single-phase PLL, the ac grid reference current generator, the dc bus voltage ripple estimator and the dc bus voltage control loop. The three-level hysteresis current controller was implemented using FPGA (Xilinx Spartan IIE™ LC). The inner and outer boundary values used were 0.4A and 0.5 A, respectively.

5.2. Parameters Design

Since the maximum output dc voltage of the solar array simulator (Agilent E4350B) is 60V, the dc bus nominal voltage V_{dc_ref} is designed to be 50 V, with the steady state variation range of $\pm 15\%$. The magnitude of ac grid voltage V_{ac} was selected to be 35 V. The load is a single phase diode rectifier in parallel with a capacitor and a resistor. The rated apparent power of the load S_{load} is 125 VA, power factor PF= 0.8. Simulation result shows that the maximum gradient of load current is $(di/dt)_{\max}$=4.5 kA/s.

5.2.1 Converter Inductor L_{inv} Design

According to [24], the instantaneous di/dt generated by the active filter should be greater than the di/dt of the harmonic component of the load, so that proper harmonic cancellation can take place. This can be expressed as

$$V_{ac} + L_{inv}\left[\frac{di_{load}}{dt}\right]_{\max} < V_{dc\_ref} \tag{5-1}$$

So

$$L_{inv} < \frac{V_{dc\_ref} - V_{ac}}{\left[\frac{di_{load}}{dt}\right]_{\max}} \tag{5-2}$$

Using the values of $\left[\frac{di_{load}}{dt}\right]_{\max}$, V_{dc_ref}, V_{ac} mentioned above, (5-2) becomes

$$L_{inv} < 3.33\,mH \tag{5-3}$$

For good dynamic response, the size of this inductor must be as small as possible. Nevertheless, if the inductor is too small, it can not suppress the switching ripple current. Besides, the switching frequency of the converter will be too higher which will cause considerable switching losses. So the inverter inductor L_{inv} was chosen to be 3 mH.

5.2.2. Dc Bus Capacitor *C* Design

During the steady state, the dc bus voltage ripple is caused by two elements. The first is the reactive and harmonic components of the load current that charge and discharge the energy-storage capacitor during the line period. The second is the difference between the power supplied by the PV panel, which is basically a dc component, and the active power absorbed by the inverter, which is a second order ac component.

5.2.2.1. Dc Capacitor Voltage Ripple Caused by the Nonlinear Load.

Since the even order harmonic components of the load current are usually very small, their effects on the dc voltage ripple can be neglected. So the reactive and harmonic components of the load current can be expressed as:

$$i_{gh}(t) = I_q \cos\omega t + \sum_{k=3,5,\ldots}^{\infty} I_k \sin(k\omega t + \phi_k) \tag{5-4}$$

The reactive power and the harmonic power component can be expressed as:

$$
\begin{aligned}
p_{qh} &= v_{ac}(t) i_{qh}(t) \\
&= V_{ac} \sin(wt)(I_q \cos \omega t + \sum_{k=3,5,\ldots}^{\infty} I_k \sin(k\omega t + \phi_k)) \\
&= 0.5 V_{ac} (Iq \sin(2wt) + \sum_{k=3,5,\ldots}^{\infty} I_k (\cos((k-1)\omega t + \phi_k) - \cos((k+1)\omega t + \phi_k))
\end{aligned}
\tag{5-5}
$$

(5-5) shows that p_{qh} consist of 2nd, 4th and other even order harmonic components, whose periods are equal to or less than T/2. Therefore, the maximum charging or discharging time of the reactive and harmonic components will be less than T/4. According to energy balance concept [25], the following equation can be used to determine the first part:

$$
0.5 C_1 (V_{dc\_\max}{}^2 - V_{dc-\min}{}^2) = S_{load} \sqrt{1 - PF^2} \frac{T}{4} \tag{5-6}
$$

Where $V_{dc-\min}$, and $V_{dc-\max}$ represent the minimum and the maximum dc capacitor voltage during one period. S_{load} represents the apparent power of the load, while PF represents its power factor. $S_{load}\sqrt{1-PF^2}$ represents the reactive and harmonic power component of the load. Here T/4 was used since the maximum charging or discharging time will be less than T/4, as mentioned in the previous paragraph. The energy stored in the capacitor is proportional to the square of the voltage across it. The left hand side of (5-6) represents the difference between its maximum and its minimum value. The right hand side represents the maximum energy that may be charged of discharge to the capacitor by the reactive and harmonic power of the load. From (5-6), the size of the capacitor can be expressed as:

$$
C_1 = \frac{0.5 T S_{load} \sqrt{1 - PF^2}}{V_{dc\_\max}{}^2 - V_{dc-\min}{}^2} \tag{5-7}
$$

5.2.2.2. Dc Capacitor Voltage Ripple Caused by the PV Power.

If the power supplied by the PV panel P_{pv} all flows into the ac grid, the magnitude of the current flowing into the ac grid should be

$$I_{ac} = \frac{2P_{pv}}{V_{ac}} \tag{5-8}$$

Where V_{ac} is the magnitude of ac grid voltage. Since the grid current is in phase with the grid voltage for unity power factor operation, the power flowing into the ac grid is

$$P_{ac} = V_{ac} I_{ac} \sin^2(wt) = P_{pv}(1 - \cos(2wt)) \tag{5-9}$$

So the dc capacitor needs to buffer the power difference between the power supplied by the PV panel and that absorbed by the ac grid. Fig.5.2 illustrates that the average value of P_{pv} equals to that of P_{ac} in one period. The shaded area shows that the maximum discharging or charging period is T/4 (T=1/60 s). Based on the power balance concept, the following equation can be utilized to determine the dc capacitor size

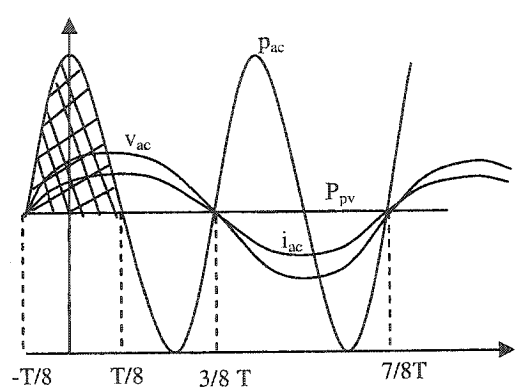

Fig.5.2: Power supplied by the PV panel

$$0.5C_2(V_{dc\_max}{}^2 - V_{dc-min}{}^2) = \int_{-T/8}^{T/8} (p_{ac} - P_{pv})dt \tag{5-10}$$

So

$$C_2 = \frac{2\int_{T/8}^{T/8}(p_{ac} - P_{pv})dt}{V_{dc\_\max}{}^2 - V_{dc-\min}{}^2}$$

$$= \frac{2\int_{T/8}^{T/8} P_{pv}\cos(2wt)dt}{V_{dc\_\max}{}^2 - V_{dc-\min}{}^2} \tag{5-11}$$

$$= \frac{2P_{pv}}{(V_{dc\_\max}{}^2 - V_{dc-\min}{}^2)w}$$

Combining (5-7) and (5-11), the minimum dc capacitor size is

$$C = C_1 + C_2 = \frac{0.5TS_{load}\sqrt{1-PF^2}}{V_{dc\_\max}{}^2 - V_{dc-\min}{}^2} + \frac{2P_{pv}/w}{(V_{dc\_\max}{}^2 - V_{dc-\min}{}^2)}$$

$$= \frac{0.5/60\times125\sqrt{1-0.8^2} + 2\times125/377}{57.5^2 - 42.5^2} \tag{5-12}$$

$$= 858\,\mu F$$

where $T = 1/60\,s$, $w = 377\,rad/s$, $V_{dc\_\max} = V_{dc\_ref}(1+15\%) = 57.5\,V$, $V_{dc\_\min} = V_{dc\_ref}(1-15\%) = 42.5\,V$

So a dc capacitor of 858 μF will ensure that the steady state voltage ripple is within $\pm15\%$ of the nominal dc bus voltage. In reality, the actual size of the capacitor may be a little smaller since the maximum voltage ripple caused by the reactive and harmonic components of the load and that caused by the PV panel power usually do not occur at the same moment. Sometimes they may even cancel with each other. In the prototype, the actual dc capacitor is 600 μF, which is the only available volume at hand that is most closed to the value obtained in (5-12). Experiment results show that the steady state

voltage ripple is within ±12% of the nominal dc voltage. This means that (5-12) provides a reasonable estimation of the required dc capacitor size.

Table 2.1 lists the specifications of the circuit parameters of Fig.2.1 used in the experimental tests.

TABLE 2.1 – MAIN PARAMETERS OF THE SCALED-DOWN SYSTEM

Dc link nominal voltage (V_{dc_ref})	50 volts
Magnitude of ac grid voltage (V_{ac})	35 volts
Utility frequency	60 Hz
Dc bus capacitor (C)	600 μF
Inverter inductor (L_{inv})	3 mH
Load capacitor (C_{load})	300 μF
Load inductor (L_{load})	1 mH
Load resistor ($R1$)	10 Ω
Load resistor ($R2$)	10 Ω
Maximum load current gradient($[di/dt]_{max}$)	4.5 KA/s
Average switching frequency	1.7 KHz

5.3. Introduction to the dSPACE System

The dSPACE system is a hardware architecture used for rapid prototyping of electrical control systems, which is comprised of DS1103 PPC controller board. It is equipped with a Motorola PowerPC 604e processor, whose computing power allows for the simulation of large-scale floating-point control algorithms in real-time. A full range of I/O devices including a TMS320F240 slave DSP is available on-board. Using the Real-Time Interface to Simulink, automatic code generation from block diagrams is possible. I/O functions are specified graphically as part of the simulation model.

5.3.1 Real-Time Interface to Simulink

Using MATLAB and Simulink for modeling, analysis, design and offline simulation has become a de-facto standard for control system development. The Real-Time Interface enhances the Simulink block library with additional blocks, which provide the link between Simulink and the real-time hardware, as shown in Fig.5.3. To graphically specify an I/O channel the corresponding block icon has to be picked up from the I/O block library and attached to the Simulink controller model. I/O parameters, such as voltage ranges or resolutions, can be set in appropriate dialog boxes. The Simulink model then is transferred into real-time code, using the Real-Time Workshop, state flow control, and the Real-Time Interface. Code generation includes the I/O channel specification and the multitasking setup, which are translated into appropriate function calls of the Real-Time Library. The library is a C function library providing a high-level programming interface to the hardware. The Real-Time Library also includes access functions for the slave DSP. These blocks cover the I/O functionality of the prototyping hardware.

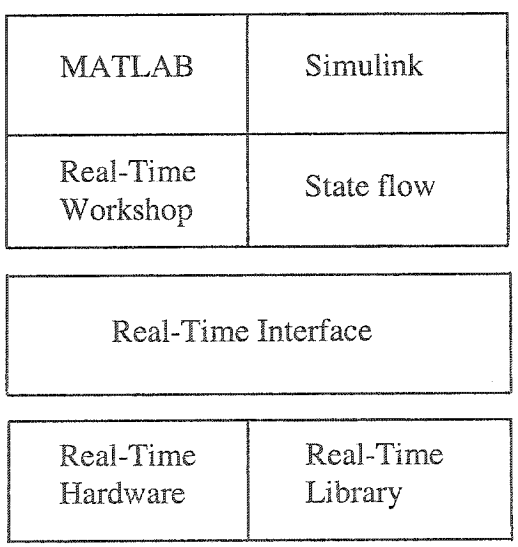

Fig.5.3. The Real-Time Interface in the MATLAB/Simulink environment

5.3.2 Simulink Block Library for DS1103

The block library for the DS1103 PowerPC Controller Board is subdivided into two major parts according to the two microprocessor units on the board. The library shown in Fig. 5.4 comprises all I/O units that are directly served by the PowerPC master processor. Block icons for the standard I/O channels such as A/D, D/A converters, and digital I/O are included as well as the more complex incremental encoder blocks.

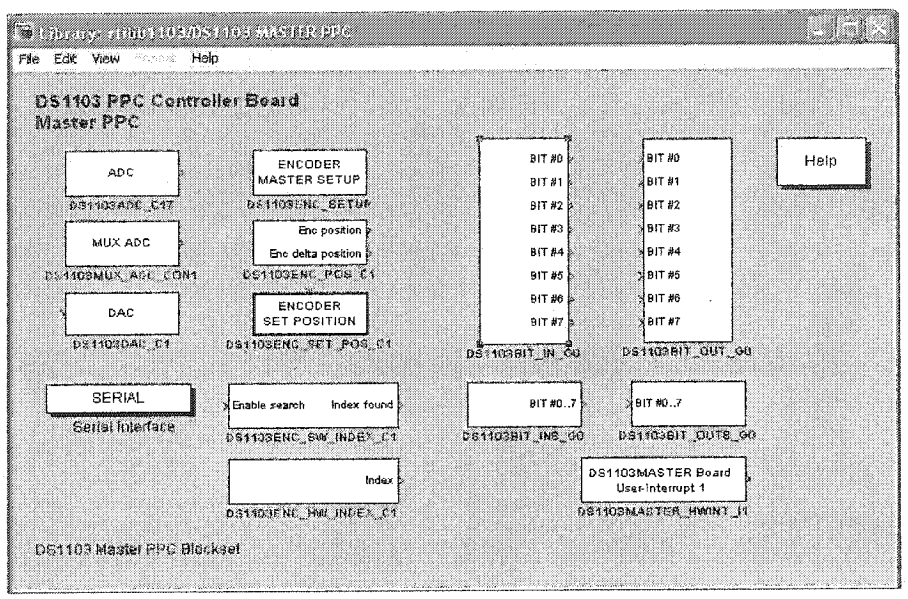

Fig.5.4. Master Processor block library for Simulink

The slave DSP library, shown in Fig.5.5, offers frequently used functions of the TMS320F240, such as single-phase and three-phase PWM signal generation, frequency measurement, A/D conversion, and digital I/O. Because the real-time simulation is executed in the master PPC board, it is wished to employ the functions provided by the slave DSP as much as possible to save the computation time on the Master PPC board.

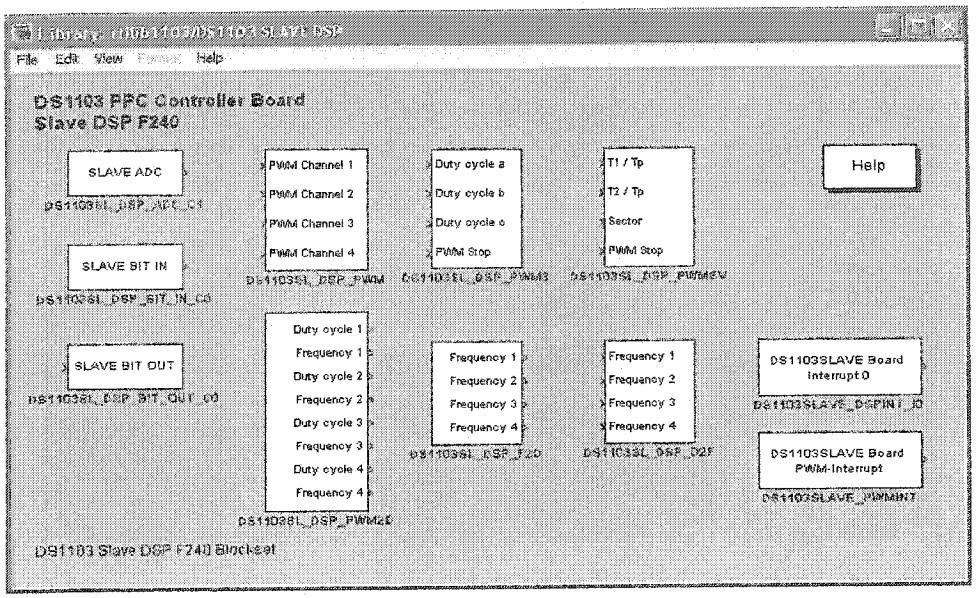

Fig. 5.5. Slave DSP block library for Simulilnk

5.4. Experimental Results

Fig.5.1 shows the experiment setup circuit. Without solar irradiation, the utility interface cannot inject active power into the grid but it can still work as a power conditioner. This is shown in Fig.5.6, where the reactive power and harmonic component of the nonlinear load have been completely compensated, and the ac grid current is in phase with the ac grid voltage. The voltage waveform at the dc side of the inverter and the effectiveness of the dc bus voltage ripple estimator in the steady-state are shown in Fig.5.7. There one sees that the estimated dc voltage ripple matches very well that of the dc bus voltage. The magnitude of the ac grid reference current is basically a dc component, which means that the distortion caused by the dc voltage ripple is negligible as a result of the estimation and cancellation of the dc bus voltage ripple.

Next we investigate the system performance under transient conditions. Fig.5.8 shows the relevant system waveforms when there is a sudden variation on the power

injected into the dc bus (from 0 to 125 W) by the MPPT and PV array. The inverter operates initially as a power conditioner, supplying reactive power and compensating for the harmonics of the local load. When PV power starts to be injected into the dc bus, the average value of the dc bus voltage increases, reaching a maximum value of 60 V. The dc bus voltage regulation loop identifies the error and the inverter starts injecting active power into the grid. The ac grid current and the capacitor voltage settle to the new steady-state values in about two line cycles. Since the active power consumed by the local load is only 53 W, the flow of power in the grid reverses as can be seen by observing the phase angle between the load current and grid current waveforms. One can also see from Fig.5.8 that the dc bus voltage ripple increases as a result of the increased current in the ac side of the inverter.

Fig.5.9 and Fig.5.10 compare the actual and estimated voltage ripple in the dc bus when the inverter supplies active and reactive power and compensates for the load harmonics. One can see that the two waveforms are very similar under steady-state conditions. In the transient state, they do not match well, since the moving average filter utilized in the voltage ripple estimator need one line cycle to yield the correct value after a step change of the dc bus voltage.

Fig.5.11 shows the performance of the system for a sudden variation of the active power consumed by the local load (53 W to 106 W) while the power supplied by the dc-dc MPPT converter and PV array is kept constant at 15 W. There one sees that the voltage in the capacitor voltage decreases immediately when the active power consumed by the local load increases. Recall that the inverter is controlled to compensate for the load's reactive power and harmonics yielding a constant, sinusoidal ac grid current in the

steady state. Therefore, any sudden variation of the active power consumed by the load is supplied or absorbed by the dc bus capacitor until the dc bus voltage regulation loop adjusts the magnitude of the current drawn from the grid. With a small dc bus capacitor, it is crucial that the voltage control loop presents a high bandwidth to minimize the magnitude and duration of the dc bus voltage variations.

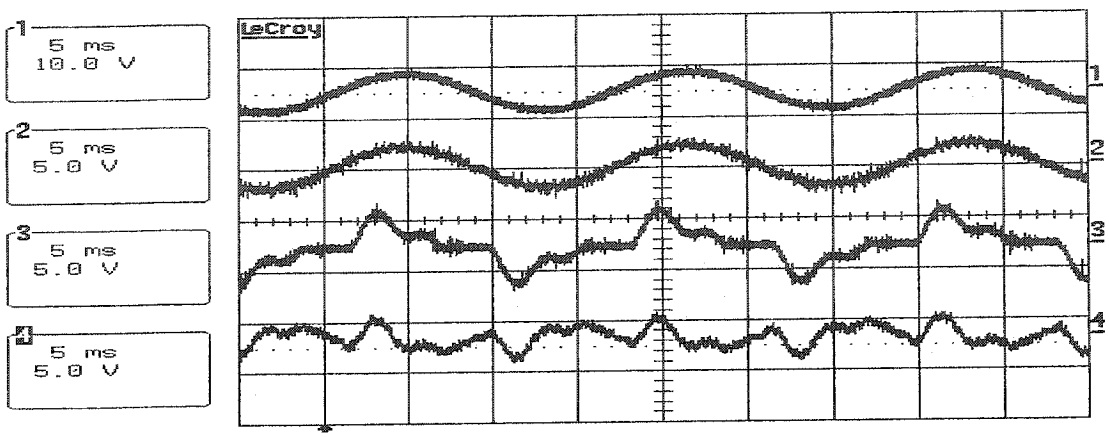

Figure 5.6. Performance of the PV interface when working as a power conditioner. 1) Ac grid voltage; 2) Ac grid current; 3) load current; 4) Inverter current

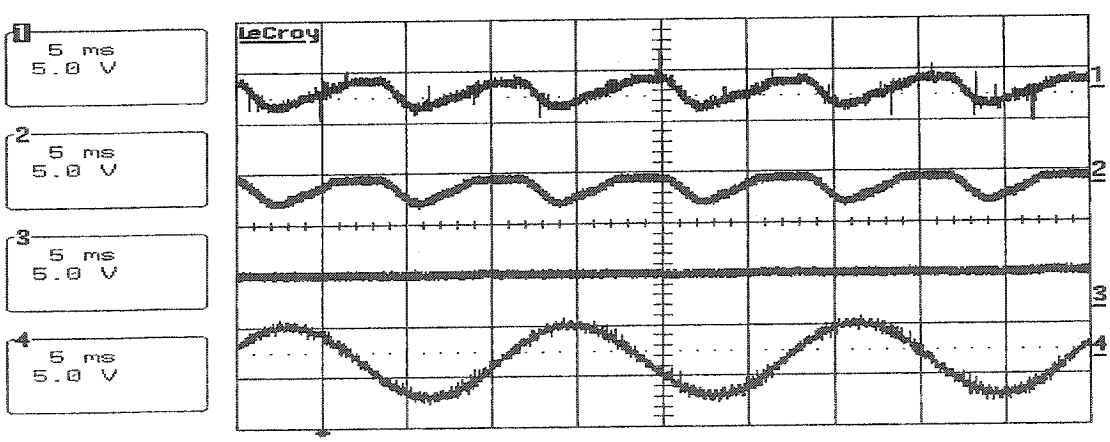

Figure 5.7. Performance of the PV interface when working as a power conditioner 1) Dc bus voltage; 2) Estimated voltage ripple; 3) Magnitude of the ac grid reference current; 4) Ac grid current

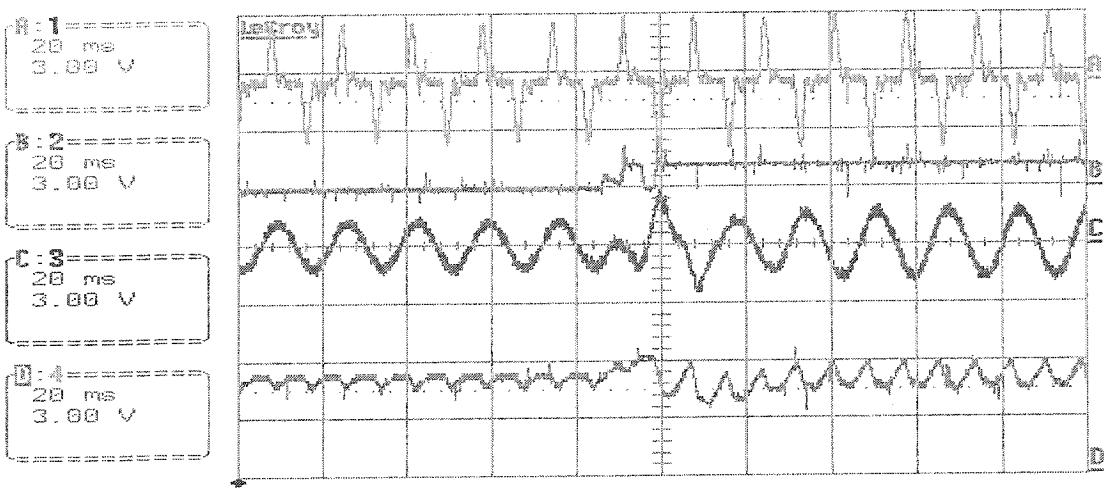

Figure 5.8: Step variation in the PV current. a) Load current; b) MPPT - PV panel current; c) Ac grid current and d) Dc bus capacitor voltage.

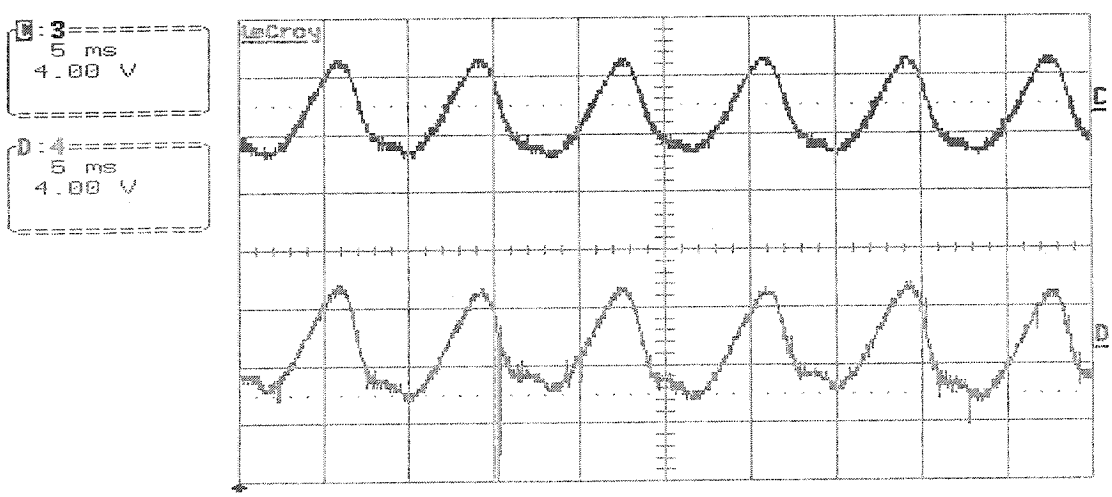

Figure 5.9: (c) Estimated and (d) actual dc bus voltage ripple.

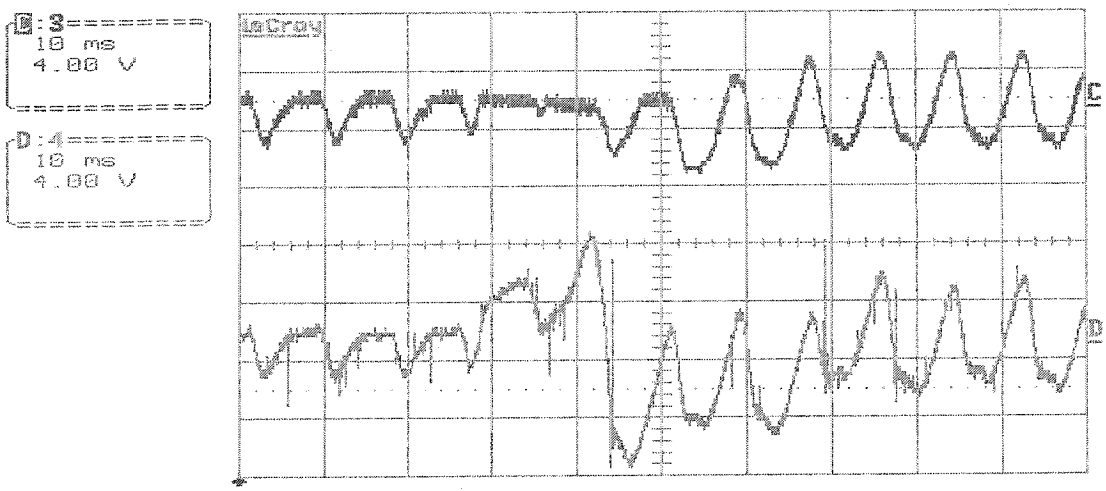

Figure 5.10: (c) Estimated and (d) actual dc bus voltage ripple.

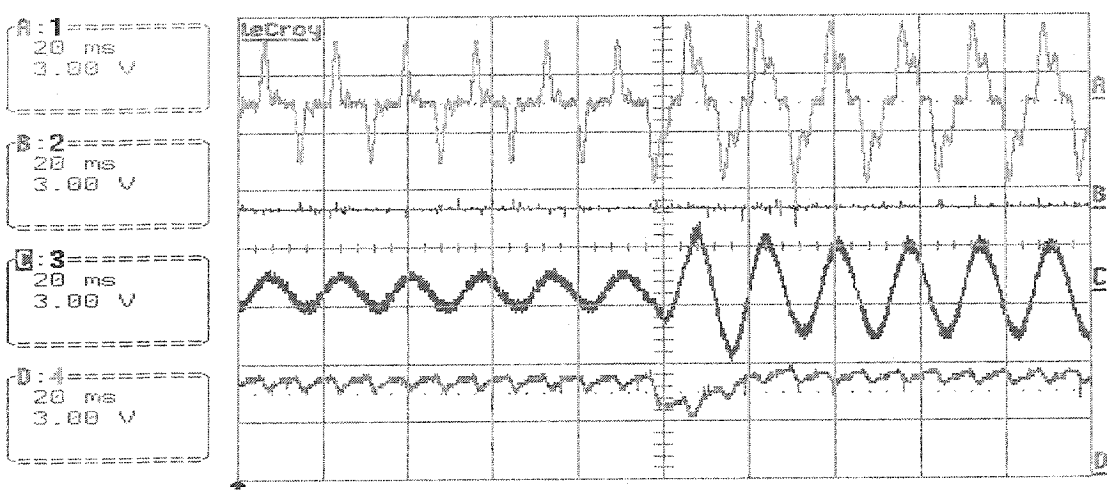

Figure 5.11: Step variation in the load power; a) Load current; b) MPPT - PV panel current; c) Ac grid current and d) Dc bus capacitor voltage.

5.5. Conclusions

This chapter has presented details of the practical implementation of the grid-connected PV interface with active power filtering and reactive power compensation. First, it discussed the design procedure for the main passive elements used in the power circuit: the inverter inductor L_{inv} and the dc bus capacitor C. It has been shown that if the interface is to implement active filtering, the inductor has to be small to allow high di/dts but will result in larger high order current components. If these need to be attenuated to reduce the voltage distortion under stand-alone conditions, one can include an ac capacitor to create a second order low pass filter. Regarding the size of the dc bus capacitor, the design equations show that it should be larger than those used in sinusoidal unity power factor inverters due to the extra current reflected to the dc side. However, the approach used in this thesis was to keep the dc side capacitor small and prevent the propagation of the dc bus voltage ripple, and consequent distortion of the ac current with low order components, by estimating and canceling the ripple.

A small-scale laboratory prototype controlled with a DSP development kit was implemented to verify the performance of the multi-featured grid connected inverter. It employed the dc bus voltage ripple estimator, the reference current calculator, the PLL and the three-level hysteresis current controller described in previous Chapters. The experimental results showed that the proposed implementation can successfully provide power conditioning yielding a grid current that is either in phase or anti-phase with the grid voltage, depending on the direction of the active power, and presents only high order components. The absence of low order distortion under steady-state conditions despite the increased dc bus voltage ripple demonstrates the efficacy of the dc bus voltage ripple

estimator under steady state conditions. However, the effectiveness of the ripple estimation and cancellation approach is not as good when the power produced by the dc source varies suddenly, resulting in distortions in the ac current and a larger than expected variation in the dc bus voltage values. This should not be a problem for PV systems where the solar irradiation level varies slowly but would be of concern for wind power systems that are subject to wind gusts. Regarding the variation of the average value of the dc bus voltage, it was shown that the speed of response was relatively slow due to the type of controller used in the application: A classical PI controller with constant gains.

6. CONCLUSIONS

This Thesis describes a control scheme for a single-phase grid-connected inverter for distributed power sources. It has been described with a photovoltaic (PV) system, but it can be used with other power sources that have been converted to a dc form. The main, and usually the only, objective of grid-connected inverters is to transfer active power into the ac side, to be consumed by local loads and injected into the utility. However, with adequate control scheme, the inverter can also provide active filtering and var compensation, thus behaving also as a power quality conditioner for the local bus. This makes the use of renewable energy sources more attractive to the user.

An important issue for the operation of grid connected inverters is the regulation of the dc bus voltage. The error between the reference and actual dc bus voltage values is used to control the amount of active power injected by the inverter into the ac grid and the load. Most single-phase inverters suffer a loss of system reliability by using a large electrolytic type dc capacitor to limit 2nd order voltage harmonic. Low non-electrolytic capacitor yield large dc bus voltage ripple that can lead to the distortion of the ac line current with low order components. It has been shown that if the inverter is operated to provide active filtering, other low order harmonics (4th, 6th...) appearing in the dc bus will make the problem even more difficult to solve. In order to reduce the effects of the dc bus voltage ripple, this Thesis has discussed the use of a dc bus voltage ripple estimator. It has been shown that the proposed estimator presents good performance in steady state conditions but the transient response is relative slow. However, this should not be a serious problem for PV systems where the output power varies relatively slowly.

This Thesis also dealt with the design of a phase-locked loop (PLL) for grid connected single-phase inverters. These are used to provide a synchronization signal to the inverter control system. An enhanced single phase PLL that uses a new phase detection scheme is developed. Its major advantage over the conventional PLL is that its phase detector output does not contain the second order harmonics when the PLL stays locked. This feature makes it easy to design the loop filter yielding a system which has not only fast response speed, but also good noise rejection capabilities. The enhanced single phase PLL contains two loops; one for phase tracking, the other for magnitude tracking. It is especially suitable for power electronic applications where the operating frequency is usually low (60 Hz or 50 Hz) and can vary significantly such as in wind energy conversion systems that operate with variable speed.

The last issue discussed in this thesis was the implementation of a current control scheme with high bandwidth. Two-level hysteresis type current controllers have been used in applications such as active power filtering. However, they result in high switching frequencies and high switching losses. Three-level hysteresis controllers can reduce this problem but their implementation can be troublesome. A new control circuit for three-level hysteresis current controller that presents balanced switching signals and does not risk creating dc offsets in the ac current was developed in this thesis. It can be implemented with simple discrete components or with a field programmable gate array (FPGA). The results obtained from the experiment prototype illustrated a significant reduction of the average switching frequency (5.5 kHz to 1.7 kHz), with respect to the tradition two-level type, while maintaining the same performance.

A prototype of the proposed grid connected inverter with all the aforementioned control blocks has been implemented with a digital signal processing (DSP) and a FPGA development kits. A number of tests that demonstrate the good performance of the system under steady state and transient conditions have been presented.

Suggestions for the Future Work

Experimental results show that during the transient state, the delay caused by the voltage ripple estimation technique slows down the system response speed. Besides, system oscillation was sometimes observed. The future work could focus on:

1) Develop a model for the voltage source inverter. The bandwidth of its dc bus voltage control loop is around 100 Hz, as have been developed for ac-dc power factor pre-regulators.
2) Employ a more advanced control scheme that is more adequate to deal with the inherent oscillatory characteristics of the power injected by a single-phase inverter into the grid.
3) Develop a modified version of the dc bus voltage ripple estimator that presents a better transient response.

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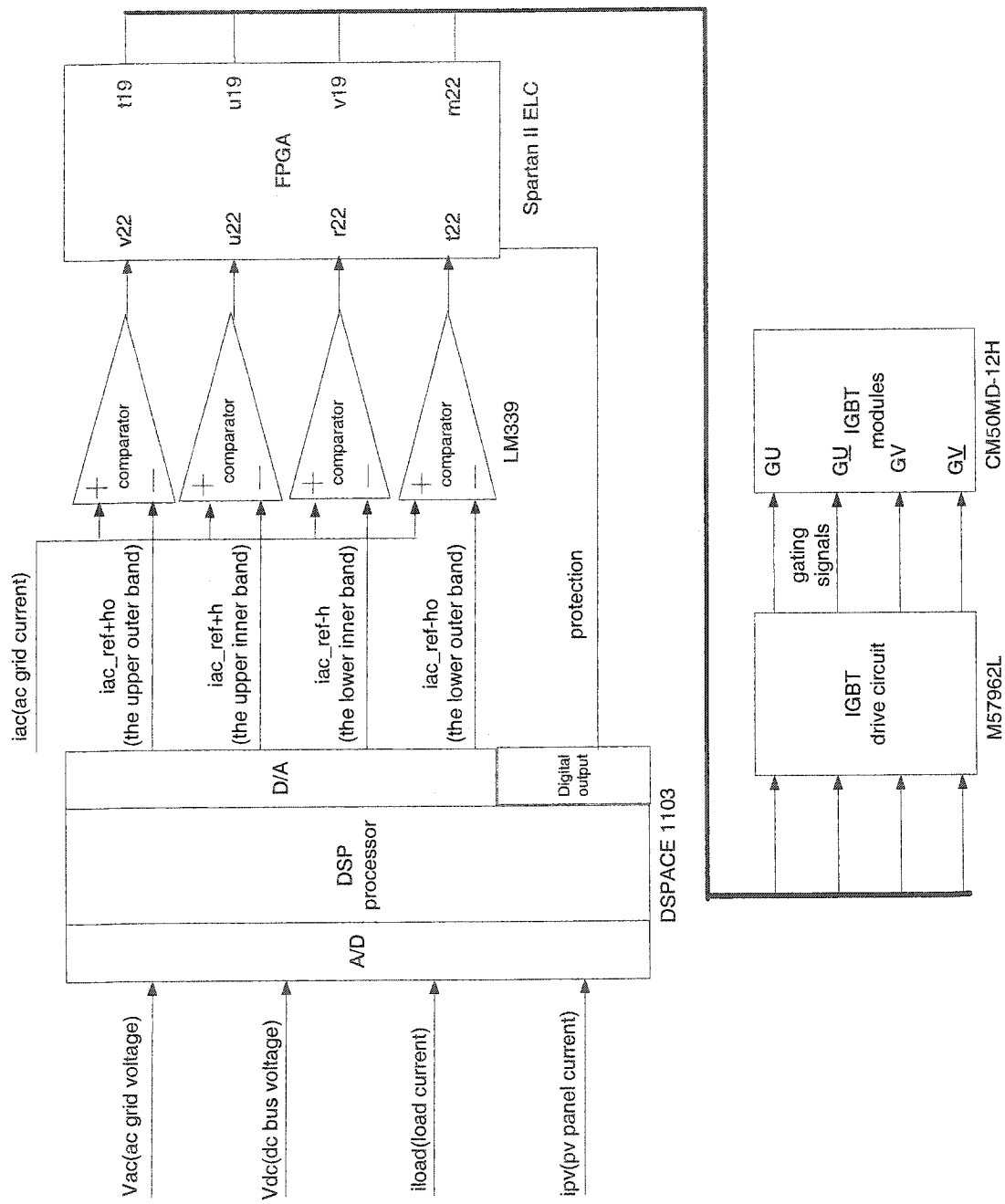
APPENDIX

A.1. Implementation Scheme of the System



A.2. PI Controller Design in the Frequency Domain

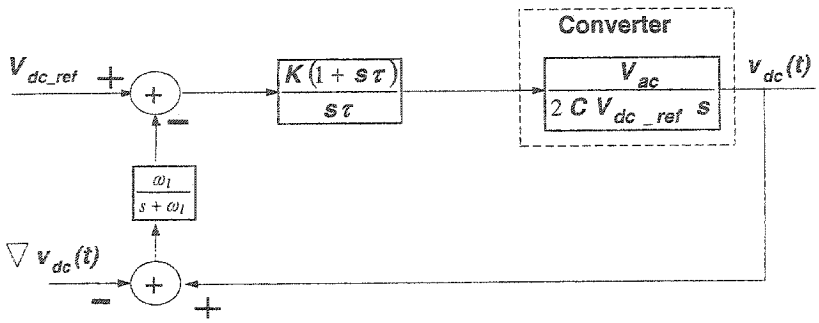


Fig.II.1: voltage feedback control loop diagram

Designing aim: The phase margin of the open-loop system (including PI controller) should be about 45°, at the crossover frequency (w_s) of 45 HZ (282.6 rad/s).

The PI controller can be expressed as:

$$G_{(PI)} = \frac{K(1+s\tau)}{s\tau} = K_p + \frac{K_i}{s}$$

The loop transfer function of the plant and feedback block is

$$LTF(s) = \frac{V_{ac}}{2C\,V_{dc\_ref}\,s}\,\frac{\omega_l}{s+\omega_l} = \frac{13195}{0.06S^2 + 22.62S}$$

Where $\omega_l = 377 rad/s$, $V_{ac} = 35V$, $V_{dc\_ref} = 50V$, $C = 600\mu F$

1. Draw the bode diagram of the above open-loop transfer function

Matlab commands:

```
a=tf([13195],[0.06,22.62,0]);

Margin(a);
```

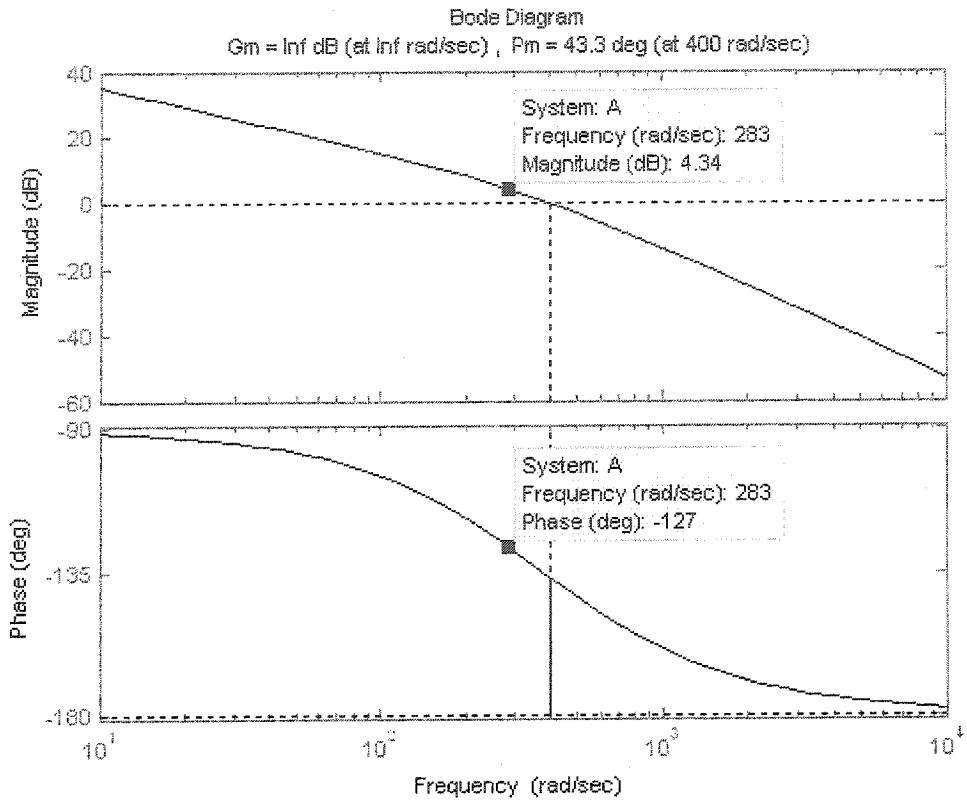


Fig.II.2: Bode diagram of the open-loop system (without PI controller)

2. Fig.II.2 indicates that the phase and the magnitude of the open loop system (without PI controller) are -127° and 4.34 dB respectively at the crossover point where the frequency is 282.6 rad/s. Since the required phase margin is 45°, the phase of the PI controller at the crossover frequency point (w_s = 282.6 rad/s) should be:

$$\angle G_{(PI)} = \arctan(s\tau) - 90 = -(180° - 127° - 45°) = -8°$$

So $s\tau = 7.1$, and $\tau = \dfrac{7.1}{282.6} = 0.025\,(s = w_s = 282.6\ rad/s)$

3. Let $K = 1$, the magnitude of the open loop system (containing the PI controller) at the crossover point is:

$$4.34+20\lg(G_{(PI)}) = 4.34 + 20\lg(\frac{K(1+s\tau)}{s\tau}) = 4.34 + 20\ \lg(\frac{1\times(1+7.1)}{7.1}) = 5.5$$

In order to adjust the magnitude of the system to be 0 dB at the crossover point, the value of K should be calculated as:

$$20\lg K = -5.5, and\ K = 10^{\frac{-5.5}{20}} = 0.53$$

4. So K_p, K_i can be obtained as:

$$K_p = K = 0.53$$

$$K_i = \frac{K_p}{\tau} = \frac{0.53}{0.025} = 21.2$$

The PI controller can be expressed as:

$$G_{(PI)} = \frac{K(1+s\tau)}{s\tau} = \frac{0.53(1+0.025s)}{0.025s} = \frac{0.53s+21.2}{s}$$

The open loop transfer function of the system, including the PI controller, is:

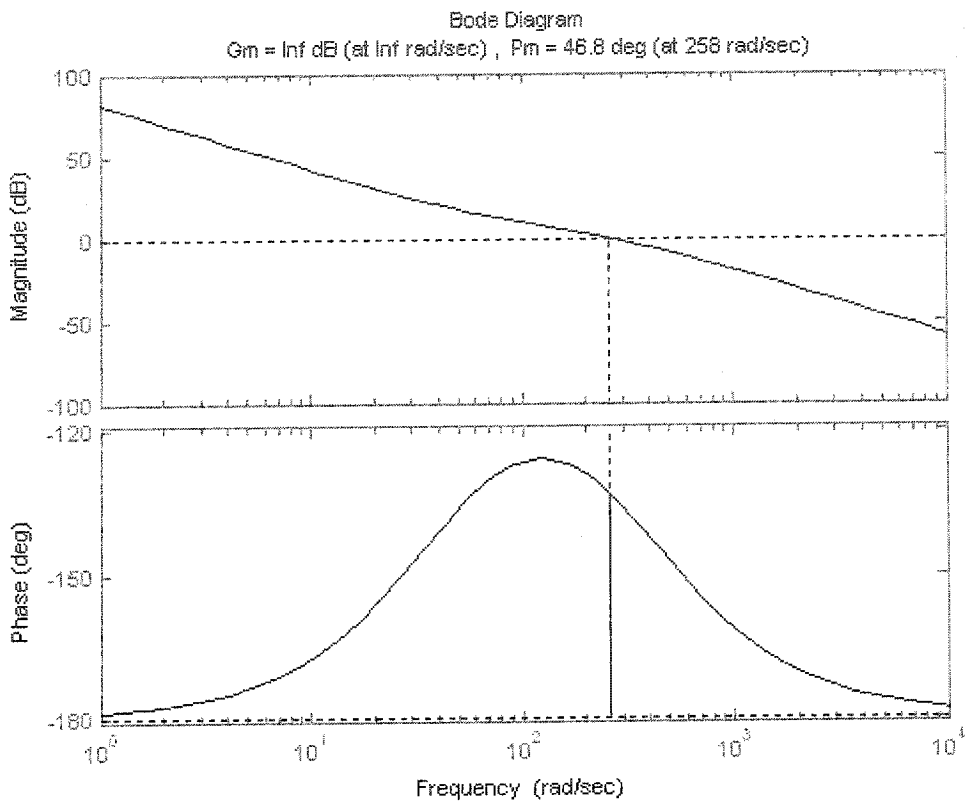
$$LTF_{PI}(s) = \frac{13195(0.53s+21.2)}{0.06S^3+22.62S^2} = \frac{6993s+279734}{0.06S^3+22.62S^2}$$

Draw the bode diagram of the above open-loop transfer function

Matlab commands:

```
a=tf([6993,279734],[0.06,22.62,0,0]);

Margin(a);
```



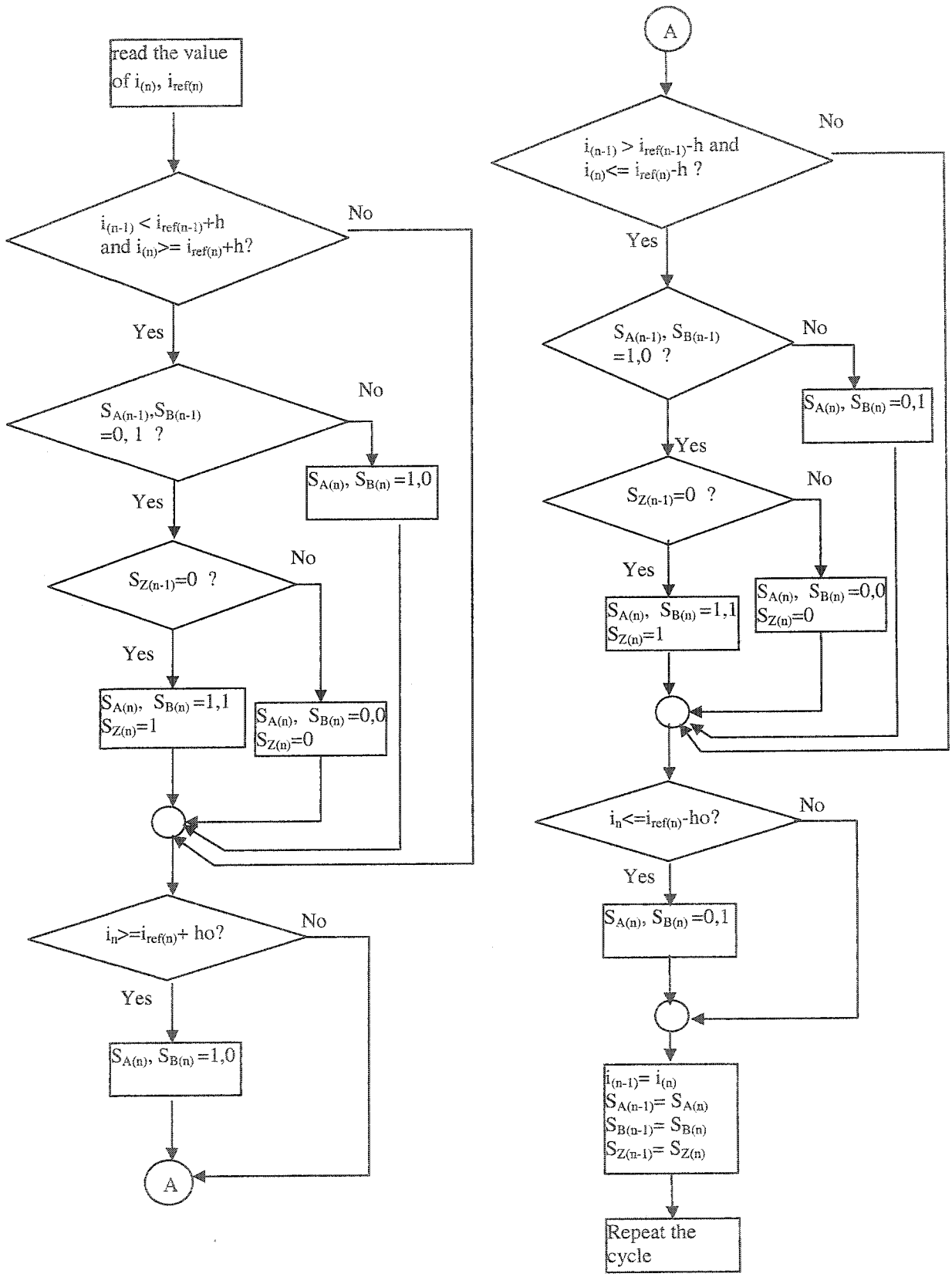
One sees that the system has a phase margin of 46.8°, at the crossover frequency of 258 rad/s, which basically matches the design specifications.

After simulations, the values of K_p, K_i have been adjusted to be

$K_p = 0.5, K_i = 25$

This results in a system with a phase margin of 45.2° at a crossover frequency (bandwidth) of 40 Hz (248 rad/s).

A.3. Flow Chart for the Three Level HCC



A.4. VHDL Codes for the Three Level HCC

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following lines to use the declarations that are
-- provided for instantiating Xilinx primitive components.
--library UNISIM;
--use UNISIM.VComponents.all;
--the current flows from the converter to the load

entity hys_3 is
   Port ( in_up_out : in std_logic;    --input signals
        in_up : in std_logic;
                in_low : in std_logic;
                in_low_out : in std_logic;
                in_clock: in std_logic;
                in_reset : in std_logic;
        out_gate1 : out std_logic;      --gating signals for the converter
        out_gate2 : out std_logic;
        out_gate3 : out std_logic;
        out_gate4 : out std_logic);
                );
end hys_3;

architecture Behavioral of hys_3 is
signal temp1 : std_logic;  --temporary gating signal
signal temp2 : std_logic;
signal temp3 : std_logic;
```

```
signal temp4 : std_logic;
signal temp_d1 : std_logic; -- delay one cycle in order to create deadtime
signal temp_d2 : std_logic; -- for the switch
signal temp_d3 : std_logic;
signal temp_d4 : std_logic;
signal up_pre : std_logic;
signal low_pre : std_logic;
signal zo :std_logic;        --the converter is in the zero state in the previous   cycle
signal counter :  std_logic_vector(7 downto 0);
signal clk1u : std_logic;

begin
process(in_clock,in_reset)  -- divide the clock frequency from
begin                        --100 MH to 100/128 MH
if (in_reset = '0') then
counter <= "00000000" ;
elsif (in_clock'event and in_clock = '1') then
counter <= counter + 1;
end if;
end process;

clk1u <= counter(6);

process(clk1u,in_reset)
variable pause_one : std_logic_vector(1 downto 0); --if the switch has switched in
begin   --the first clock cycle, then it will not switch in the second clock cycle,
if (in_reset = '0') then                -- to avoid the current surge after the switching

        temp1 <= '0';
        temp2 <= '0';
        temp3 <= '0';
```

```
        temp4 <= '0';
        temp_d1 <= '0';
        temp_d2 <= '0';
        temp_d3 <= '0';
        temp_d4 <= '0';
        zo <= '0';
        pause_one := "00";
        up_pre <= '0';
        low_pre <= '0';
elsif (clk1u'event and clk1u = '1') then
        if (pause_one = "00") then
           if (up_pre = '0') and (in_up = '1') then
                    if (temp1 = '1') and (temp3 = '0') and (zo = '0') then
                            temp1 <= '1';
                    temp2 <= '0';
                            temp3 <= '1';
                            temp4 <= '0';
                            zo <= '1';
                            pause_one := "01";

                    elsif (temp1 = '1') and (temp3 = '0') and (zo = '1') then
                            temp1 <= '0';
                    temp2 <= '1';
                            temp3 <= '0';
                            temp4 <= '1';
                            zo <= '0';
                            pause_one := "01";

                    else
                            temp1 <= '0';
                    temp2 <= '1';
```

```
                temp3 <= '1';
                temp4 <= '0';
                pause_one := "01";
        end if;
end if;
if (in_up_out = '1') then
        temp1 <= '0';
        temp2 <= '1';
        temp3 <= '1';
        temp4 <= '0';
        pause_one := "01";
end if;

if (low_pre = '0') and (in_low = '1') then
        if (temp1 = '0') and (temp3 = '1') and (zo = '0')  then
                temp1 <= '1';
        temp2 <= '0';
                temp3 <= '1';
                temp4 <= '0';
                zo <= '1';
                pause_one := "01";
        elsif (temp1 = '0') and (temp3 = '1') and (zo = '1')  then
                temp1 <= '0';
        temp2 <= '1';
                temp3 <= '0';
                temp4 <= '1';
                zo <= '0';
                pause_one := "01";

        else
                temp1 <= '1';
```

```
                temp2 <= '0';
                        temp3 <= '0';
                        temp4 <= '1';
                        pause_one := "01";
                end if;
        end if;
        if (in_low_out = '1') then
                temp1 <= '1';
                temp2 <= '0';
                temp3 <= '0';
                temp4 <= '1';
                pause_one := "01";
        end if;

        up_pre <= in_up;            --it is put inside the "endif" statement in
        low_pre <= in_low;          --order not to measure the
                                    --wrong curent surge
    else
                pause_one := pause_one + 1;
    end if;
    temp_d1 <= temp1;       --create the deadtime for the switches
    temp_d2 <= temp2;       -- in order to make the deadtime
    temp_d3 <= temp3;       -- be one clock cycle
    temp_d4 <= temp4;
end if;
end process;

 --current flow from ac source
out_gate2     <= temp1 and temp_d1; --create the deadtime for the switches
out_gate1 <= temp2 and temp_d2;
out_gate4 <= temp3 and temp_d3;
```

```
out_gate3        <= temp4 and temp_d4;
end Behavioral;
```