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A SINGLE STAGE POWER FACTOR CORRECTED AC/DC CONVERTER

Matteo Daniele

A Thesis

in

The Department

of

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Abstract

A Single Stage Power Factor Corrected AC/DC Converter

Matteo Daniele

Applications for AC/DC converters that require high input power factor has been traditionally implemented by two power stages. In order to provide a cost effective and high density solution for low power applications, this thesis proposes a single stage isolated converter topology designed to achieve a regulated dc output voltage having no low frequency components and a high input power factor. The topology is derived from the basic two switch forward converter, but incorporates an additional transformer winding, an inductor, and a few diodes. The proposed circuit inherently forces the input current to be discontinuous and ac modulated to achieve high input power factor. The converter's output is operated in discontinuous conduction mode to minimize the bulk capacitor's voltage variations with variations in the output load current. Analysis of the converter is presented and performance characteristics are given. Design guidelines to select critical components of the circuit are presented. Experimental results on a 150 W, 50 kHz, universal input (90 - 265 V), 54.75 V output AC/DC converter are given which confirm the predicted performance of the proposed topology.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF PRINCIPAL SYMBOLS

C_l	DC bus capacitance
C_o	output filter capacitor
C_{S1}, C_{S2}	input EMI capacitor
D	duty cycle
D_7 *to* D_{10}	diodes of the bridge rectifier
f_{sw}	switching frequency
i_{in}	input current drawn by the power supply
i_{aux}	auxiliary inductor current
i_C	DC bulk capacitor current
i_{Ll}	Auxiliary inductor current
I_1	rms value of fundamental frequency current component
$I_{\text{in rms}}$	rms value of the total current
I_o	output load current
L_o	output filter inductor
L_l	auxiliary inductor
N_{aux}	Auxiliary winding
N_p	primary winding
N_s	secondary winding
N_{ps}	turns ratio between primary and secondary windings
P_o	output power
S_1, S_2	MOSFET switches

t_{on}	on-time of the switch
t_{off}	off-time of the switch
T_{sw}	switching time period
V_{out}	output voltage
V_m	peak input voltage
V_s	secondary voltage
V_c	bulk capacitor voltage
V_{in}	RMS input voltage
V_{LI}	voltage across auxiliary inductor

CHAPTER 1

INTRODUCTION

1.1 GENERAL INTRODUCTION

Today an increasing number of equipment require a DC power source. The power rating of such applications may range from low power, in the electronic circuits within computers, to high power, in central office equipment in the telecommunication industry. Irrespective of the power level most electronic circuits are very sensitive to variations in the input DC voltage source and therefore require a regulated (stiff) DC bus. The AC mains, provided by the utility, is the primary source for the DC power which is derived by a suitable conversion process using AC to DC power converters.

In traditional AC to DC converters, the input stage converts the AC input voltage to an unregulated DC bus voltage which is the input to the downstream converter providing a well-regulated DC output. The basic method of generating the unregulated DC bus voltage is to use the bridge rectifier-capacitor arrangement as shown in Fig.1.1.

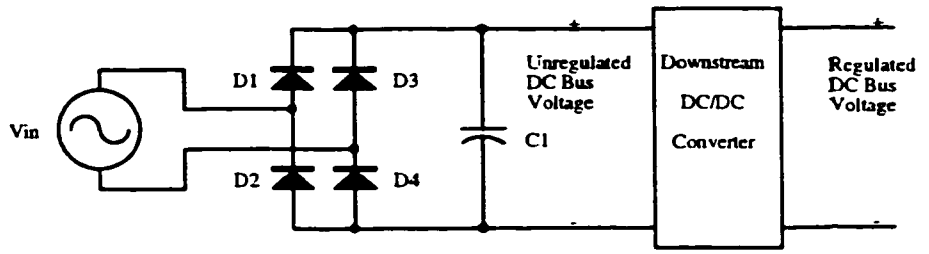


Fig. 1.1 Traditional AC to DC conversion scheme.

The DC bus Capacitor (C1) gets charged to a voltage close to the peak of the AC input voltage. The line current which flows through the bridge diode (D1-D4) does not flow continuously during the 60 Hz cycle. The current becomes zero for a finite duration during each half-cycle of the line frequency, as shown in Fig. 1.2. The input line current deviates significantly from a sinusoidal waveform.

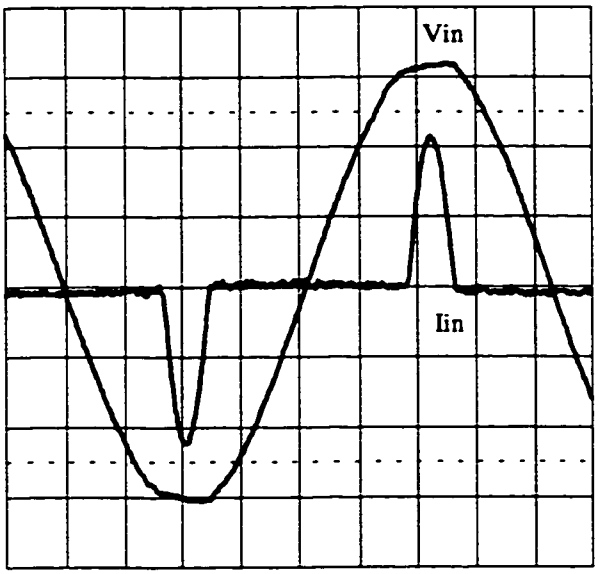


Fig. 1.2 Input AC line voltage and current with conventional front end conversion scheme.

Also, from Fig. 1.2, it is shown that the converter loads the line near its peak voltage level. This, in conjunction with the source impedance of the line, produces an undesirable distortion of the voltage waveform. This distorted waveform will also be impressed on any other piece of equipment connected to the same line. The disadvantages posed due to the phenomenon of 'harmonic pollution' have been of interest in the power electronics community for more than a decade. Harmonic currents cause power system heating and add to user power bills. The input current waveform introduces harmonics into the line also disturbing nearby sensitive equipment like computers thereby adversely effecting their performance [1, 2].

As shown in Fig. 1.2, the RMS value of the input current is also higher than the corresponding sinusoidal current required to produce the same power. This translates into a reduction in the amount of available real power from the line. The peak current conducted also places a high stress on the bridge rectifier, the bulk capacitor and other components located along the input current path. The fuse rating at the input and input line losses are also affected.

Therefore, it is desirable to operate an AC to DC converter so as to eliminate the conducted harmonic content as well as to maximize the use of available power from the mains. Power line quality is becoming an important factor in modern electronic designs. With current regulation such as EN 61000-3-2, use of power factor correction (PFC) circuits is becoming widespread in power converter designs. Thus, operation of the AC to DC converter at unity power factor is desirable.

Power factor is defined as the ratio of real power to total apparent power, where the total apparent power is the product of the RMS voltage and the RMS current [3].

$$PF = \frac{V_{in_{rms}} \cdot I_1 \cdot \cos\theta}{V_{in_{rms}} \cdot I_{in_{rms}}} = \frac{I_1}{I_{in_{rms}}} \cdot \cos\theta \tag{1.1}$$

where,

I_1 is the fundamental component of the input current

cos θ is the phase angle between the fundamental component of the current I_1 and the line voltage, and

The distortion factor (DF) is defined as the ratio of the fundamental current I_1 to the RMS current.

A Fourier series analysis of the line current waveform of Fig. 1.2 would show a small lagging displacement angle between the fundamental line current and AC input voltage [3]. Most of the reduction in power factor is not attributed to reactive power but to distortion power which includes the effects of the harmonics. Hence harmonics in the current cause lower power factor.

1.2 POWER FACTOR CORRECTION: THEORY AND TECHNIQUES

Reducing the harmonics, Power Factor Correction (PFC), can be accomplished by shaping the input current waveform so that the power converter, which is a nonlinear output load, looks like a resistive load to the input. PFC can be implemented using two approaches.[1, 4-6]

1.2.1 Passive PFC

One approach to PFC is to add passive components to provide leading or lagging phase-angle. This technique is quite successful when dealing with inductive loads such as ac motors. For AC to DC converters, this approach will not be successful as the problem is not with the phase lag but with the nonsinusoidal input current waveform caused by harmonic distortion. A choke input type of filter rather than a capacitive input type can be used. But such chokes tend to be very large and bulky. Three-phase power distribution will improve the power factor a little to about 0.85. The problem with such distribution is that it is often not found in residential and office environment [5].

1.2.2 Active PFC

The second approach is an active solution which incorporates a switching DC/DC converter as a pre-regulator to the downstream converter as shown in Fig. 1.3 [1,4-6].

The pre-regulator provides an input current waveform exactly matching the input voltage and is thus capable of producing an input current waveform that is a sinusoid with no phase shift [5].

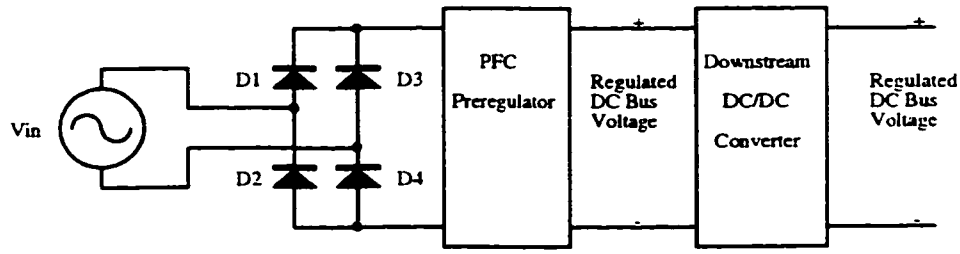


Fig. 1.3 Two stage PFC AC to DC converter.

The pre-regulators which improve power factor can be of any switch-mode power converter topology. There are three basic circuit topologies which are the Buck, Boost and Flyback. The characteristics of the three circuits are different and each has their set of advantages and disadvantages to power factor applications [1,6-8].

The boost pre-regulator, Fig. 1.4, remains the most popular approach for PFC applications [7, 8]. For higher power applications, the boost converter operates in continuous conduction mode(CCM). For low power applications the boost can operate in discontinuous conduction mode (DCM).

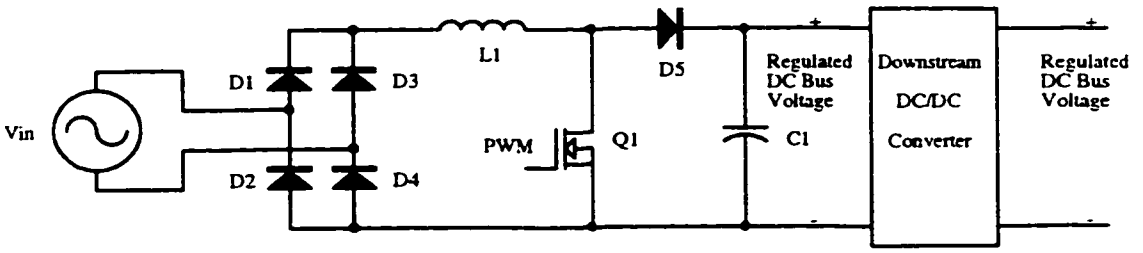


Fig. 1.4 Two stage PFC AC to DC converter with Boost pre-regulator.

The input current is not chopped when the boost pre-regulator operates in CCM. Thus, generating very low harmonics in the input current. This type of pre-regulator provides good holdup time and quickly reacts to load changes [6, 7, 9-11]. However, the use of pre-regulators results in a two-stage power supply converter. This adds to the complexity, cost and a higher component count. At low power levels, low implementation costs and simplicity are of great importance.

In order to provide a cost effective and high density solution for power factor corrected AC/DC power supplies, a number of high power [12, 13] and low power [14-17] single-stage PFC circuits have been recently developed and reported in the literature. However, the low power single-stage circuits reported so far present one or more of the following disadvantages:

(a) low output power rating [14],

(b) variable frequency control [14, 15],

(c) control and power circuits are complex [16],

(d) dc output voltage contains a large low frequency voltage ripple component [17],

(e) hold-up time is reduced because small dc bus capacitors are used [17].

The circuits proposed in [18, 19] overcome the above limitations. However, their use is restricted due to patent rights. Another single stage two-switch isolated converter topology [20] was presented, which achieved a regulated DC output voltage having no low frequency components and a high input power factor.

1.3 SCOPE AND CONTRIBUTION OF THE THESIS

This thesis is concerned with a Single Stage PFC for low power applications. The purpose is to present a topology that attempts to overcome the drawbacks in the existing single stage PFC topologies. The final topology is derived from the basic two-switch forward converter and is the principal contribution of this thesis. The main objectives of the thesis are:

i) To propose a new single switch PFC AC/DC converter topology that is simple and cost effective for low power applications.

ii) To present the steady-state analysis in both continuous and discontinuous modes of operation.

iii) Selection of the proper mode of operation of the output filter.

iv) To verify the feasibility of the proposed converter by experimental results obtained from the practical setup of the converter.

1.4 THESIS OUTLINE

The contents of the thesis are organized as follows:

Chapter 2 presents the steady-state analysis of the converter for continuous output current with a fixed operating frequency. The analysis is used to generate characteristic curves which are used in selecting and rating the various components. The experimental results from the prototype are used to verify the analysis.

Chapter 3 presents a method to reduce the high bus voltage by operating the proposed converter in a variable frequency mode at light loads. The control method to implement the variable frequency control is described. Performance characteristics of the prototype converter are presented with experimental results.

Chapter 4 presents the final topology of a single stage PFC AC-DC converter in which the converter's output current is discontinuous. This converter eliminates variations in the DC bus voltage from no load to full load conditions. A detailed analysis provides design guidelines for implementing the proposed converter topology.

Experimental results from a prototype are given for a converter operating from a universal input voltage range.

Chapter 5 presents the contributions and conclusions of the thesis and suggestions for future work.

CHAPTER 2

A SINGLE STAGE SINGLE SWITCH POWER FACTOR CORRECTED AC/DC CONVERTER

2.1 Introduction

This chapter presents a single stage single switch isolated converter topology which achieves a regulated dc output voltage having no low frequency components and a high input factor. The proposed converter operates with a fixed frequency of 50 kHz and with an input voltage range of 90 V - 135 V. The maximum output power of the converter is 50 Watts with an output voltage of 5V at a maximum output current of 10 Amps. The operation of the proposed converter requires the output inductor to operate in continuous current mode upto a minimum load current of 1 Ampere.

In the following sections, the description of the proposed converter, the analysis and performance characteristics will be given.

2.2 Circuit Description of the Proposed Converter

The proposed converter circuit is shown in Fig. 2.1. The converter is derived from the basic one switch forward with the addition of the auxiliary circuit. This auxiliary circuit consists of a bypass diode D_1, an inductor L_1, a rectifying diode D_2 and a free wheeling diode D_3. The auxiliary circuit also includes an auxiliary winding N_{aux} on the main

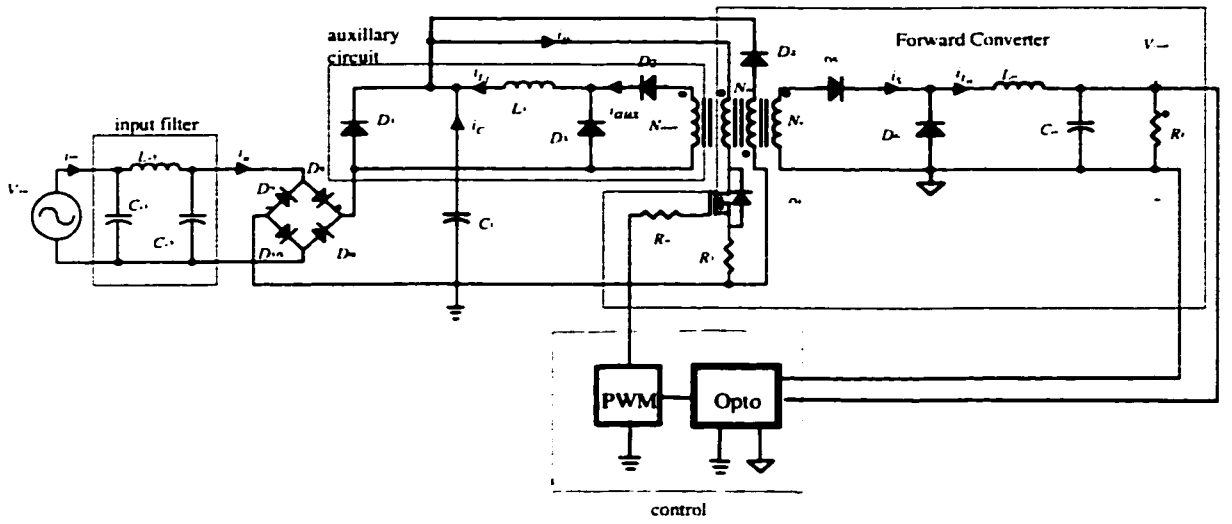


Fig. 2.1 Power and control circuits of the proposed converter.

transformer of the forward converter. The purpose of this circuit is to force the input current to be discontinuous and ac modulated to achieve high input power factor. The auxiliary circuit functions as a discontinuous-mode boost converter.

The proposed converter circuit shown in Fig. 2.1 consists of the following:

Input Filter. The input filter is compromised of high frequency capacitors C_{s1}, C_{s2} and an inductor L_{s1}. This filter is used to filter out the high frequency harmonic contents of the input current.

Diode Rectifier. The diode rectifier consists of D_7 to D_{10} which are used to convert the input ac voltage to a uncontrolled dc voltage across capacitor C_1.

DC Capacitor C_1. The dc bulk capacitor C_1 serves two functions: (a) it filters out the low frequency voltage harmonic of the rectified voltage and (b) it provides the hold-up time for the converter.

Forward Converter. The forward converter is compromised of a transformer with primary, secondary and reset windings, MOSFET switch Q_1, rectifying diode D_5, free

wheeling diode D_6 and output filter L_o and C_o. This converter converts the unregulated input voltage to a regulated output voltage.

Auxiliary Circuit. This circuit consists of bypass diode D_1, and inductor L_1, rectifying diode D_2 and free wheeling diode D_3. It also includes an auxiliary winding N_{aux} on the main transformer of the forward converter. The function of D_1 is to charge the bulk capacitor at start-up. Under normal operation, the voltage V_c is larger than the peak line voltage. Diode D_1 is reverse biased and does not play a role in the normal operation of the converter. The purpose of this circuit is to force the input current to be discontinuous and ac modulated for high input power factor.

Control Circuit. The circuit consists of a PWM and Opto-coupler circuitry. This combination is exactly the same seen on a standard isolated forward converter.

2.3 Principles of Operation

The operation of the circuit is as follow:

(a) When switch Q_1 is turned on, power is transferred from capacitor C_1 to the secondary. If the turns ratio from primary to auxiliary winding is unity, the rectified input line voltage is applied across inductor L_1, causing the inductor current to rise linearly as shown in Fig. 2.2.

(b) When switch Q1 is turned off, power from the primary ceases to be delivered to the output load. At the same time the current flowing through inductor L_1 forces diodes D_3 and either D_7, D_9 or D_8, D_{10} to conduct. A net negative voltage appears across the inductor L_1 which decreases the current to zero. Since no power is delivered to the load, the inductor current charges the capacitor C_1.

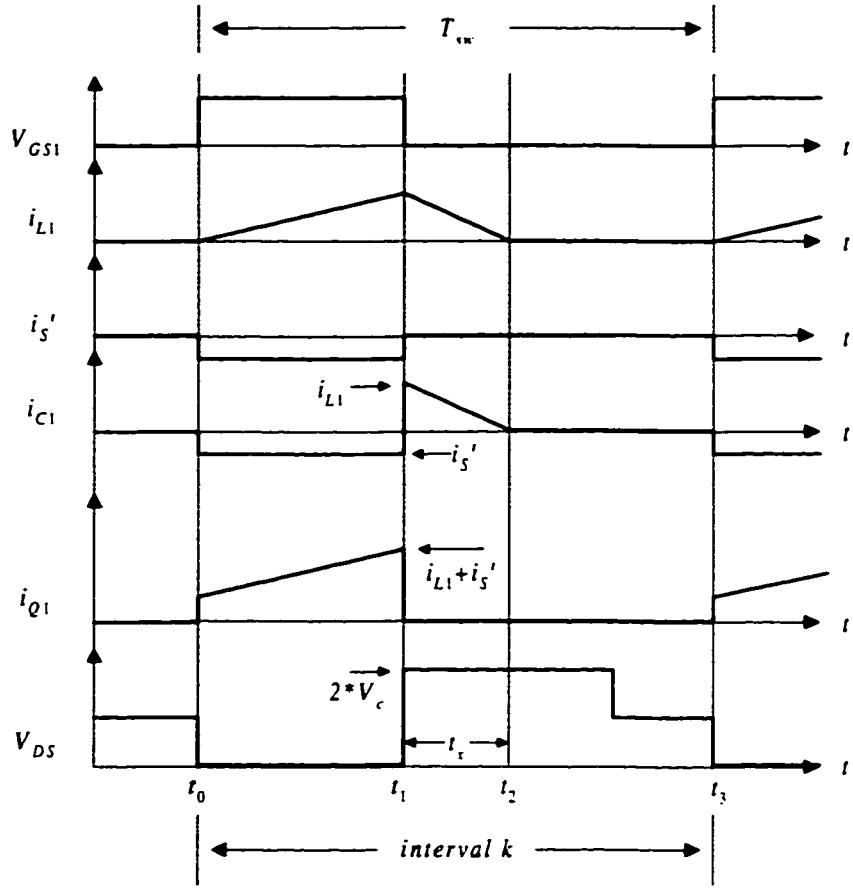


Fig. 2.2 Operational waveforms of the proposed converter.

From the above principles, the auxiliary circuit forces the ac line current to have a sinusoidal envelope at the fundamental supply frequency with high frequency components, Fig. 2.3. These high frequency components are filtered at the source providing a nearly sinusoidal current waveform. This results in low harmonic distortion and a high input power factor.

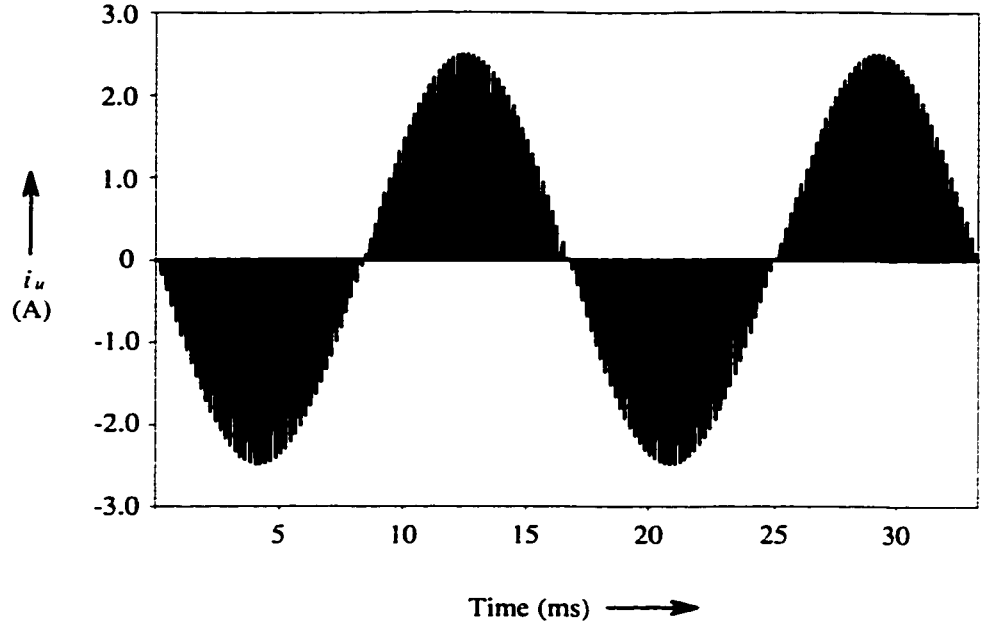


Fig. 2.3 Simulated ac line current before high frequency input filtering (V_{in} = 110 V, I_o = 10 A, V_{out} = 5 Vdc, V_c = 230 V)

The bulk capacitor's voltage varies with the output load. The voltage rises under light-load conditions and drops with the increasing load. There is large voltage variation from no-load to full load conditions.

2.4 Steady State Analysis

In this section, the various intervals of the converter's operation are explained. A simplified analysis is performed by dividing the operation of the converter into three different intervals. The analysis is based on the following assumptions:

(i) The output inductor L_o, is large enough so that the current in the inductor is always continuous.

(ii) The bulk capacitor voltage V_c is considered constant for a given input voltage and output load.

(iii) The magnetizing inductance of the transformer is assumed infinite.

(*iv*) The input voltage is assumed to be constant within an arbitrary interval *k*, Fig. 2.2.

Under the above assumptions, the operational waveforms of the converter with the transformer turns ratio $N_{aux} : N_p : N_s = 1 : 1 : 1$ are shown in Fig. 2.2.

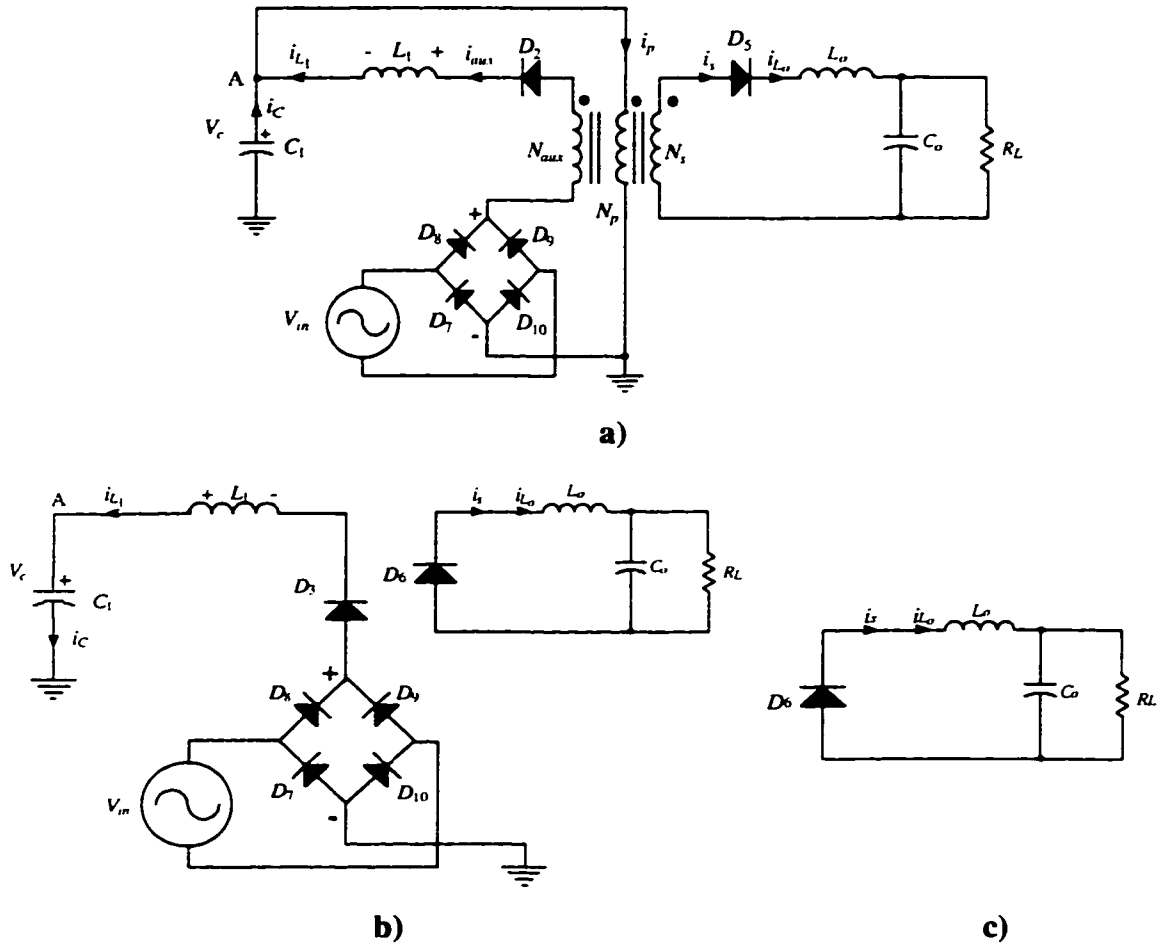


Fig. 2.4 Equivalent circuits of the converter of Fig. 2.1 during various operating intervals **(a)** Interval 1, **(b)** Interval 2, **(c)** Interval 3

Interval 1, ($t_0 < t < t_1$)

During this interval, switch Q_1 is on. Power is transferred from capacitor C_1 to the main dc output via the transformer. Power is also circulated from the ac mains into the loop formed by either diodes D_8 or D_9, the auxiliary winding, the diode D_2, the inductor L_1 , primary winding and either of the diodes D_7 or D_{10}. Fig. 2.4(a) shows the equivalent circuit during this mode of operation. If the turns ratio from primary to auxiliary winding is unity, a voltage of approximately ($V_m \cdot \sin \omega t$) is applied across inductor L_1, causing the inductor current to rise linearly as shown in Fig. 2.2. The current through the switch is the sum of the currents in L_1 and L_m. By applying KVL, we get the following equation

$$V_{L_1} + V_C\left(1 - \frac{N_{aux}}{N_p}\right) = |V_m \sin \omega t| \tag{2.1}$$

where $V_m = V_m \cdot \sin \omega t$

If, $N_{aux} = N_p$, (2.1) yields,

$$V_{L_1} = |V_m \sin \omega t| \tag{2.2}$$

This indicates that the voltage impressed on the inductor is the rectified input sine wave. The rate of change of the inductor current is given by

$$\frac{di_{L_1}}{dt} = \frac{|V_m \cdot \sin \omega t|}{L_1} \tag{2.3}$$

This indicates that the inductor current is modulated by the rectified sinusoidal input voltage.

By taking KCL at node A, we get

$$i_c + i_{L_1} = i_p \tag{2.4}$$

Transformer equations are given by

$$P_{in} = P_{out} \tag{2.5}$$

$$v_p \cdot i_p = v_s \cdot i_s + v_{aux} \cdot i_{aux} \tag{2.6}$$

$$N_p \cdot i_p = N_s \cdot i_s + N_{aux} \cdot i_{aux} \tag{2.7}$$

Equation (2.7) can be written as

$$i_p = \frac{N_s}{N_p} . i_s + \frac{N_{aux}}{N_p} . i_{aux} \tag{2.8}$$

From Fig. 2.4(a) we have

$$i_{aux} = i_{L_1} \tag{2.9}$$

$$\frac{N_s}{N_p} . i_s = i_s' \tag{2.10}$$

where i_s' is the reflected output current at the primary. From (2.8)-(2.10), the primary current is given by

$$i_p = i_s' + \frac{N_{aux}}{N_p} . i_{L_1} \tag{2.11}$$

From (2.4) and (2.11)

$$i_c + i_{L_1} = i_s' + \frac{N_{aux}}{N_p} . i_{L_1} \tag{2.12}$$

or

$$i_c = i_s' + i_{L_1} \left(\frac{N_{aux}}{N_p} - 1 \right) \tag{2.13}$$

This is the current being drawn from the capacitor when the switch is turned on.

If $N_{aux} = N_p$ then,

$$i_c = i_s' \tag{2.14}$$

This indicates that when $N_{aux} = N_p$, the current that is drawn from the capacitor is sent to the load when the switch is on.

The output inductor current i_{L_2} is constant and is reflected back to the primary as i_s'.

Interval 2, ($t_1 < t < t_2$)

Interval 2 begins when switch Q_1 is turned off. The current that was flowing through the inductor L_1 at the end of interval 1, forces diode D_3 to conduct. This current circulates through capacitor C_1 and input source V_m until it becomes zero. The equivalent circuit during this interval is shown in Fig. 2.4(b).

Applying KCL at node A, we get

$$i_{L_1} = i_c \tag{2.15}$$

This indicates that the inductor current is flowing into the capacitor C_1.

Applying KVL in Fig. 2.4(b) the capacitor voltage is given by

$$V_c = |V_m . \sin \omega t| + V_{L_1} \tag{2.16}$$

Since voltage across an inductor is given by $V_L = L\ di/dt$, (2.16) yields

$$\frac{di_{L_1}}{dt} = \frac{(V_c - |V_m . \sin \omega t|)}{L_1} \tag{2.17}$$

It can be seen from (2.17) that the rate of change of the decaying current i_{L_1} varies with the rectified input voltage. The time during which i_{L_1} , flows into C_1 during interval 2, is defined as t_x and is shown in Fig. 2.2.. During interval k, t_x varies between t_1 and t_3 as it is being modulated by the rectified input line voltage. At the peak of the rectified input voltage, the duration of t_x is at it's maximum. In a correct design, the value of L_1 is chosen so that the current i_{L_1} decays to zero before the next switching period begins.

The output inductor current is constant and is freewheeling through diode D_6 supplying the load during this interval.

Interval 3($t_2 < t < t_3$)

At the end of interval 2, all the energy stored in L_1 has been transferred to capacitor C_1 .There is no current flowing in any part of the primary circuit. The output inductor current continues to free wheel and supply the output load while the transformer resets during this interval. The equivalent circuit is shown in Fig. 2.4(c).

2.5 Performance Characteristics

In this section, the performance of the converter is studied. A mathematical presentation of effective current in various components will be shown. Characteristic curves of the proposed converter will be shown. These curves are used in selecting and rating the various components. The turns ratio of the transformer between the primary and secondary (N_p : N_s) is 11.6:1 and turns ratio between the primary and auxiliary (N_p : N_{aux}) is 1:1.

2.5.1 Effect of Transformer Turns Ratio on the Input Power Factor.

The primary to secondary turns ratio ($N_p : N_s$) is determined by the dc bulk voltage and the output voltage. However, the turns ratio between primary and auxiliary ($N_p : N_{aux}$) is some what arbitrary. In this section an optimum turns ratio between N_p and N_{aux} is determined by the use of PSPICE simulation. Fig 2.5 shows the unfiltered input line current of the converter for the three possible conditions, namely, (a). $N_{aux} = N_p$, (b). $N_{aux} < N_p$, and (c) $N_{aux} > N_p$.

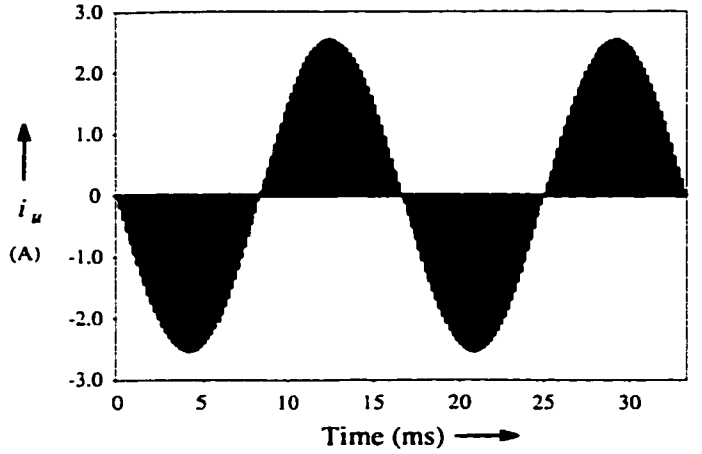
The following points are observed from Fig. 2.5 ;

(a) For $N_{aux} = N_p$, the input current has near sinusoidal current envelope, therefore a high input power factor.

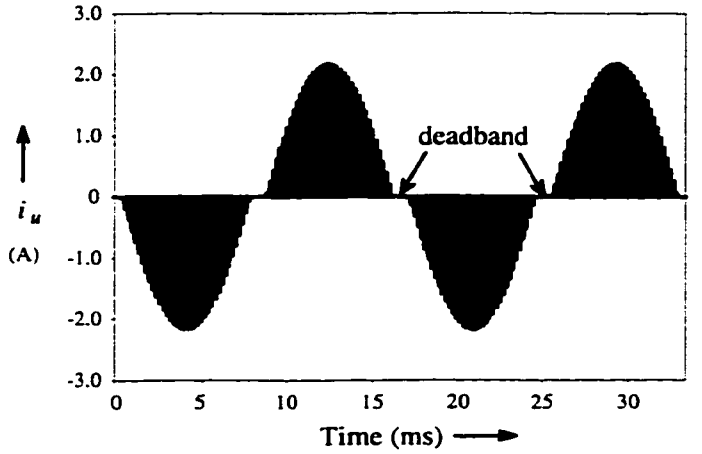
(b) For $N_{aux} < N_p$, the input current has dead-bands in each half cycle resulting in higher distortion in the current waveform and therefore a lower power factor.

(c) For $N_{aux} > N_p$, the input current has over-laps near the zero crossings and therefore a lower power factor.

The above points lead to a conclusion that in order to obtain a high input power factor, the primary to auxiliary turns ratio should be close to unity.



a)



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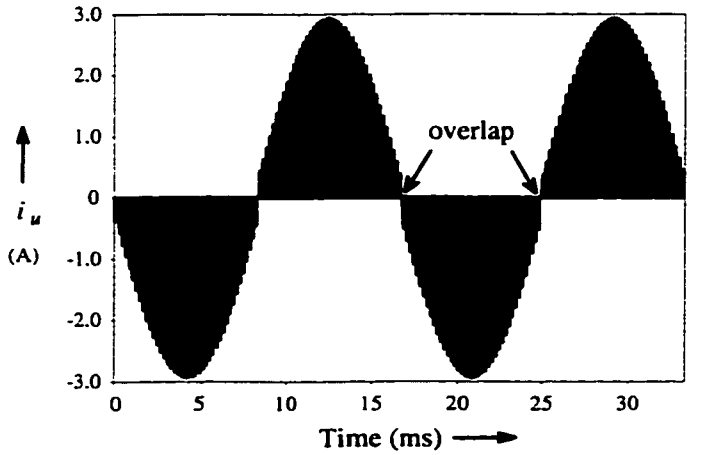


c)

Fig. 2.5 Typical simulated ac line current before filtering the high frequency components (a) $N_{aux}=N_p$. (b) $N_{aux} = 0.9N_p$. (c) $N_{aux} = 1.1N_p$. (V_{in}= 110 V , I_o = 10 A, V_{out} = 5 V, f_{sw} = 5 kHz)

2.5.2 DC Bulk Capacitor Current and Voltage

The dc bulk capacitor voltage determines the voltage stress across almost all the components of the converter, therefore, it is an important design factor. In this section, expressions which relate the capacitor voltage to the circuit parameters are derived and characteristic curves presented.

The input ac voltage is given by

$$V_{in} = V_m \sin \omega t \tag{2.18}$$

The input line voltage can be divided into n switching intervals within each half cycle. The number of switching cycles per half cycle of the line frequency is given by

$$n = \frac{T_{ac}}{T_{sw}} \tag{2.19}$$

where T_{ac} is the half period of the input voltage V_{in} and T_{sw} is the switching time. Assuming that k is the number of intervals corresponding to the switching cycle and varies between 0 to n. If t_k is the length of the k^{th} interval, the input voltage for this interval is given by,

$$V_{in_k} = V_m \sin [\omega \cdot (kT_{sw} + t_k)] \tag{2.20}$$

The peak inductor current of L_1 can be expressed as

$$i_{L1\,peak_k} = \frac{V_{in_k}}{L_1} \cdot t_{on} \tag{2.21}$$

where t_{on} is the on time of the switch (interval 1). Also, (2.17) can be written as

$$t_{x_k} = i_{L1\,peak_k} \frac{L_1}{(V_c - V_{in\,k})} \tag{2.22}$$

where t_{x_k} is the duration in time of the boost inductor current decaying from i_{L1peak_k} to 0 A.

The capacitor voltage V_c can be found by summing the charge during interval 2 and subtracting the charge leaving the capacitor during interval 1 for n intervals. The summation of all the currents leaving and entering the bulk capacitor shall give the net sum of zero amps. This is expressed by

$$\left[\sum_{k=0}^{n}\int_{0}^{txk}\left(\frac{V_c - V_{ink}}{L_1}\right)\cdot t\cdot dt\right]-\left[n\cdot\int_{0}^{t_{on}} i_s^{'}\cdot dt\right]=0 \tag{2.23}$$

Note that L_1 and $i_s^{'}$ determine the currents to and from the capacitor, and these determines the capacitor voltage.

Expanding (2.23) results in

$$\left[\sum_{k=0}^{n}\frac{1}{2}\cdot V_{ink}{}^{2}\cdot\frac{t_{on}{}^{2}}{L_1}\cdot\left(\frac{1}{V_c - V_{ink}}\right)\right]-\left[n\cdot i_s^{'}\cdot t_{on}\right]=0 \tag{2.24}$$

The output voltage of the converter operating with i_{L_o} in the continuous current mode is given by

$$V_o = \frac{V_c\cdot t_{on}}{T_{sw}\cdot N_{ps}} \tag{2.25}$$

where N_{ps} is the turns ratio between primary to secondary.

V_c and t_{on} can be obtained by solving equations (2.24) and (2.25) using mathematical software such as MathCad.

The bulk capacitor voltage V_c is a function of output load, primary to secondary turns ratio, duty cycle, value of auxiliary inductor L_1 and the input voltage. Fig. 2.6 shows the effect on the bulk capacitor voltage during changes in output current. The capacitor voltage increases for decreasing output load current.

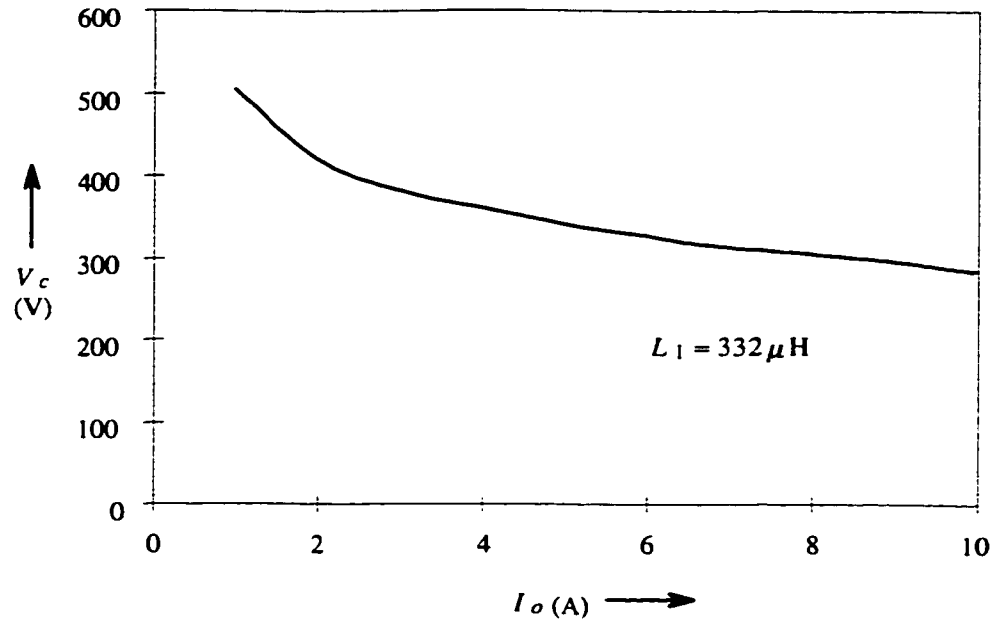


Fig. 2.6 Bulk voltage versus output current.

In Fig. 2.2, the bulk capacitor current i_{C1}, is shown for a switching interval within a half cycle of the input voltage. In Fig. 2.7, i_{C1} is shown for a typical case during one cycle of the input voltage. It can be seen that i_{C1} during interval 2 is modulated by the ac input voltage.

The current leaving the bulk capacitor during interval 1 results in slight discharging of the capacitor. During interval 2, the current in the bulk capacitor can be either positive or negative, thus slightly discharging or charging the capacitor. The voltage ripple on the capacitor can be determined by calculating the net current per switching interval.

The net or average current during the switching interval can be either positive or negative. We will denote this term as i_{cavg_k}.

Therefore,

$$i_{cavgk} = \frac{\left(0.5 \cdot t_{x_k} \cdot i_{L1\,peak_k}\right) - \left(i_s' \cdot t_{on}\right)}{T_{sw}} \tag{2.26}$$

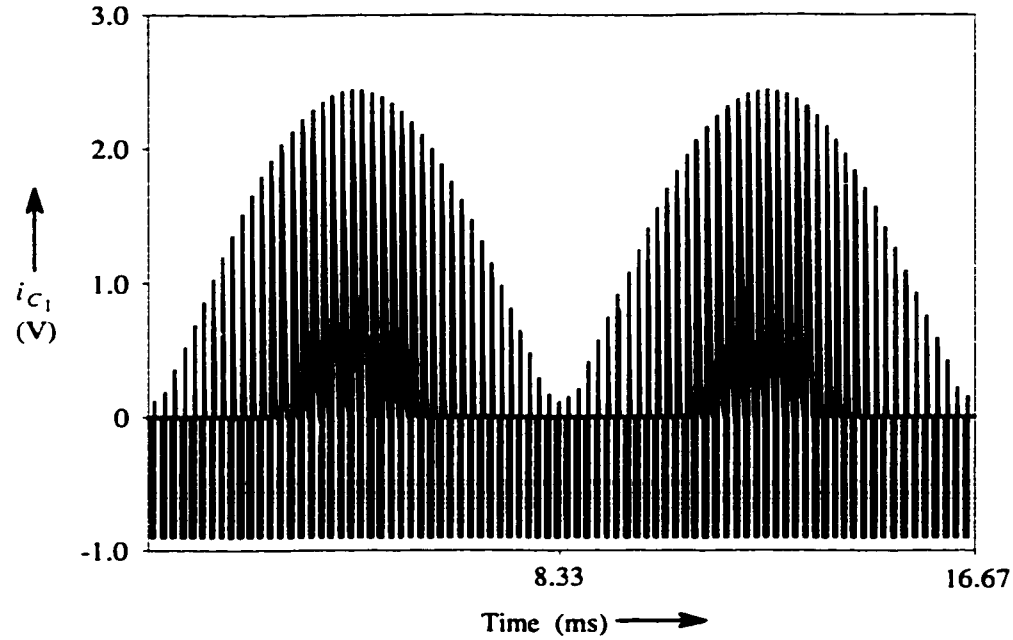


Fig. 2.7 DC bulk capacitor current.

In Fig. 2.8, i_{cavg_k} is shown for a typical case. The net current of the bulk capacitor during the half cycle of the ac input is determined by

$$i_{cavg} = \sum_{k=0}^{n} i_{cavg_k} \tag{2.27}$$

and is equal to zero amps during steady state conditions. If the bulk capacitor value is assumed to be 100 μF, the rate of voltage change in the bulk capacitor can be determined by (2.26) and the equation $I = C\frac{dv}{dt}$. We will denote this term dv_{avg_k}.

Therefore,

$$dv_{avg_k} = \frac{i_{cavg_k} T_{sw}}{C} \tag{2.28}$$

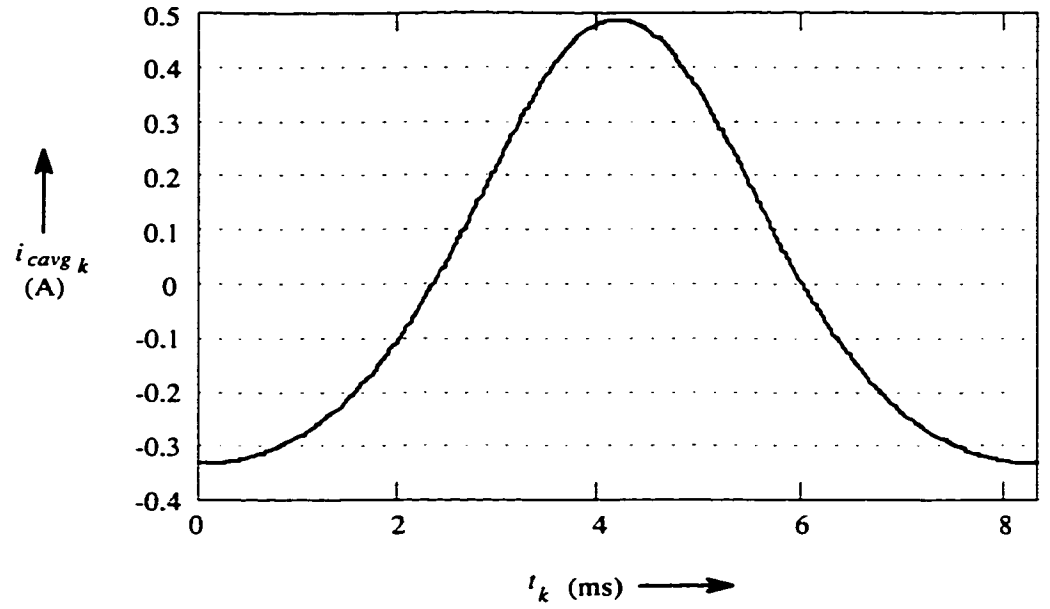


Fig. 2.8 Average current per switching cycle of the capacitor.

Fig. 2.9 iilustrates dv_{avg_k} during a half cycle of the 60 Hz input.

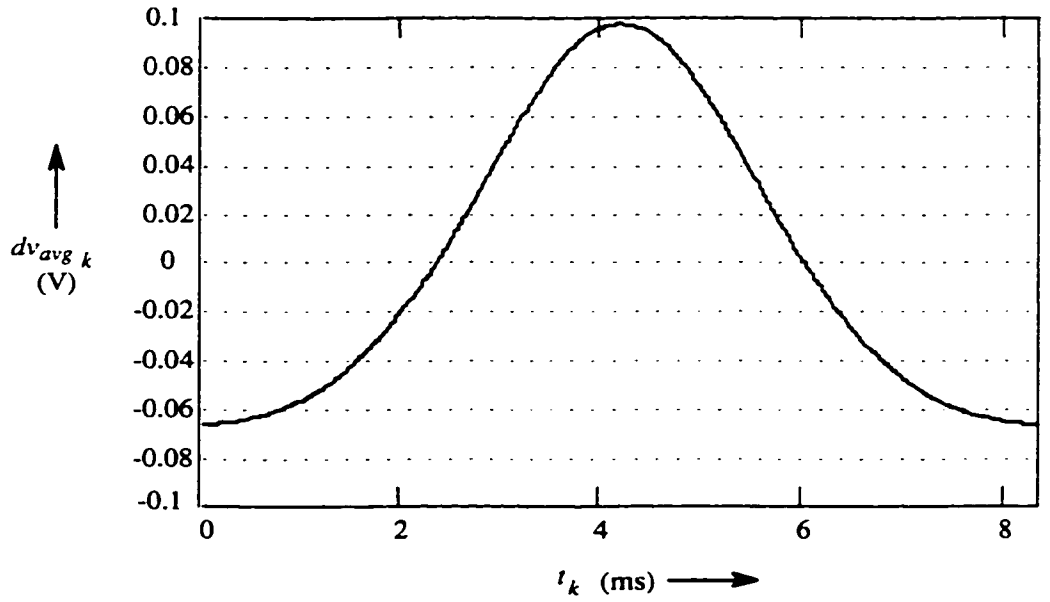


Fig. 2.9 Average voltage per switching interval of the capacitor.

The net voltage of the bulk capacitor during the half cycle of the ac input is determined by

$$dv_{avg} = \sum_{k=0}^{n} dv_{avg_k} \tag{2.29}$$

and is equal to zero volts during steady state conditions. By summing the voltage change in the capacitor per switching interval T_{sw}, the voltage ripple of the capacitor is determined and shown in Fig. 2.10. The voltage ripple of the bulk capacitor is denoted by v_c.

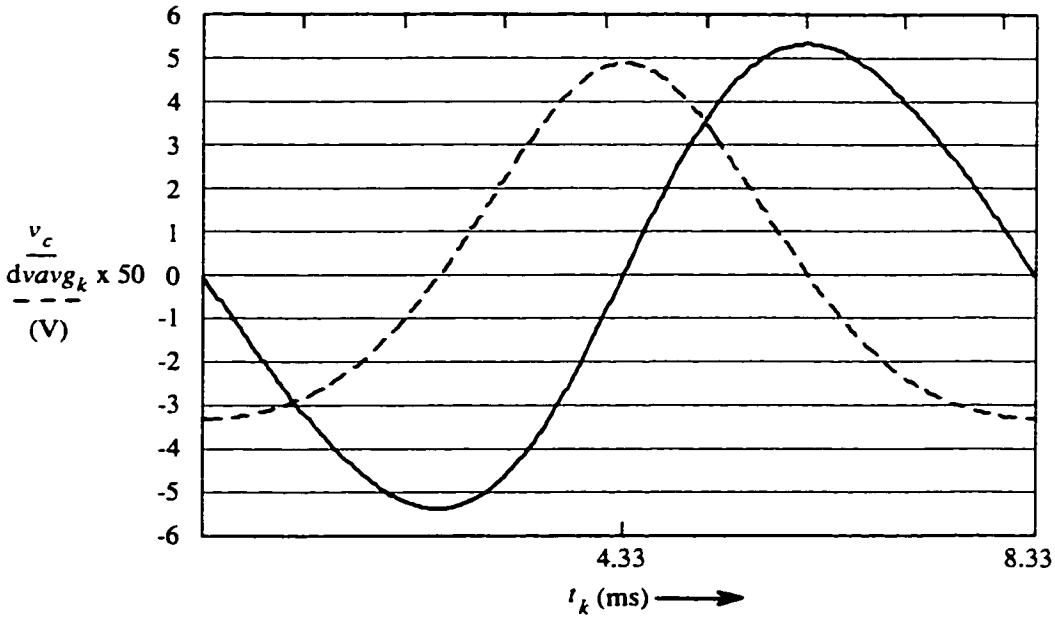


Fig. 2.10 Ripple voltage and average voltage per switching interval of the capacitor.

It should be noted that there is a 90° phase shift between v_c and dv_{avg_k}. The voltage dv_{avg_k} is the complement of i_{cavg_k} and therefore these two are in phase. This 90° phase shift between v_c and dv_{avg_k} is due to the fact that current leads voltage in a capacitor.

The RMS current of the DC bulk capacitor can be expressed as:

$$I_{C1rms} = \sqrt{\frac{1}{T_{ac}}\left[\sum_{k=0}^{n}\left[i_s{}'\right]^2 \cdot t_{on} + \left(i_{L1peak_k}\right)^2 \cdot \frac{t_{x_k}}{3}\right]} \qquad (2.30)$$

where $i_s{}'$ is the secondary output current divided by the turns ratio between primary and secondary.

As seen in the above calculations, the DC bulk capacitor voltage is a function of many variables and it determines the voltage stress across almost all the power components.

2.5.3 Auxiliary Inductor Current

The auxiliary inductor current i_{L_1} is designed to remain discontinuous throughout the operating points of the converter. In Fig. 2.11, the auxiliary inductor current is shown during one cycle of the 60 Hz input voltage. The auxiliary inductor current is shown to be modulated by the rectified input voltage.

A closer look at Fig. 2.11 is shown in Fig. 2.12 and Fig. 2.13 at two different time intervals. It can be seen that the current peaks and the dead times (interval 3) are different at these intervals. This current that flows through L_1 is the same as the unfiltered line current.

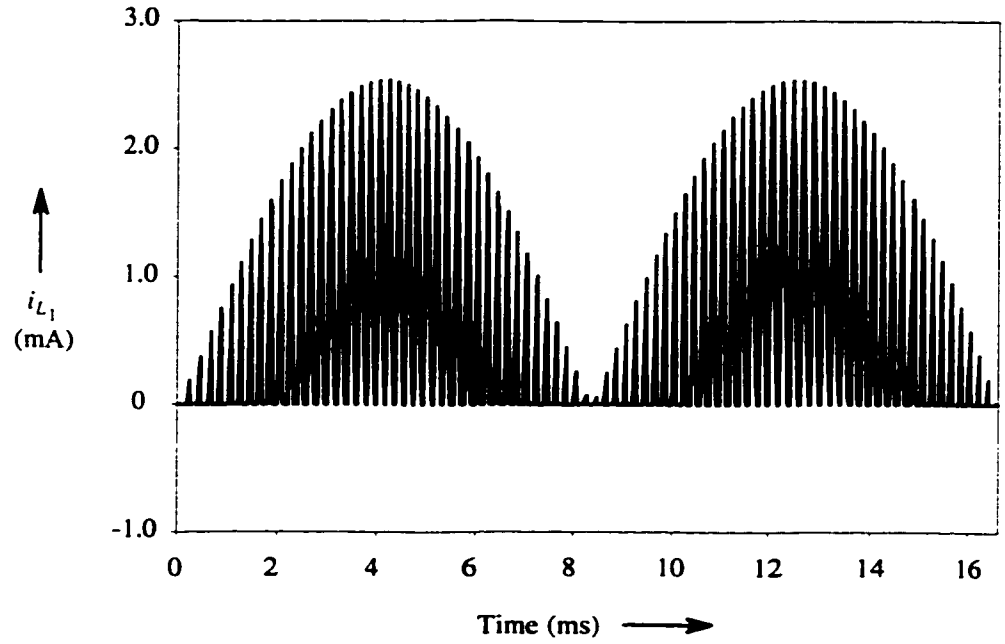


Fig. 2.11 Auxiliary inductor current modulated by the rectified line voltage

The effective current in the auxiliary inductor can be expressed by

$$I_{L_1 rms} = \sqrt{\frac{1}{T}\int_0^T i^2 t\, dt} \tag{2.31}$$

As seen in Fig. 2.12 and Fig. 2.13, the peak current is the same for intervals 1 and 2 within a switching interval. Using (2.20), (2.21), (2.22) the RMS current in the auxiliary inductor can be expressed as

$$I_{L_1 rms} = \sqrt{\frac{1}{3 \cdot T_{ac}}\left[\sum_{k=0}^{n}\left(i_{L1\,peak_k}\right)^2 \cdot t_{on} + \left(i_{L1\,peak_k}\right)^2 \cdot t_{x_k}\right]} \tag{2.32}$$

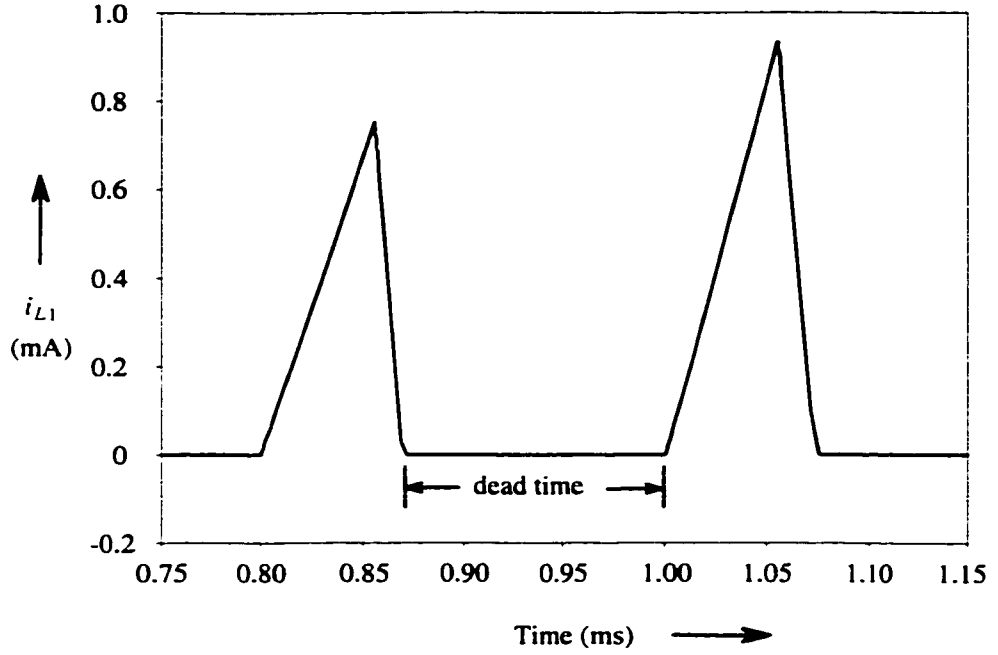


Fig. 2.12 Auxiliary inductor current modulated by the rectified line voltage

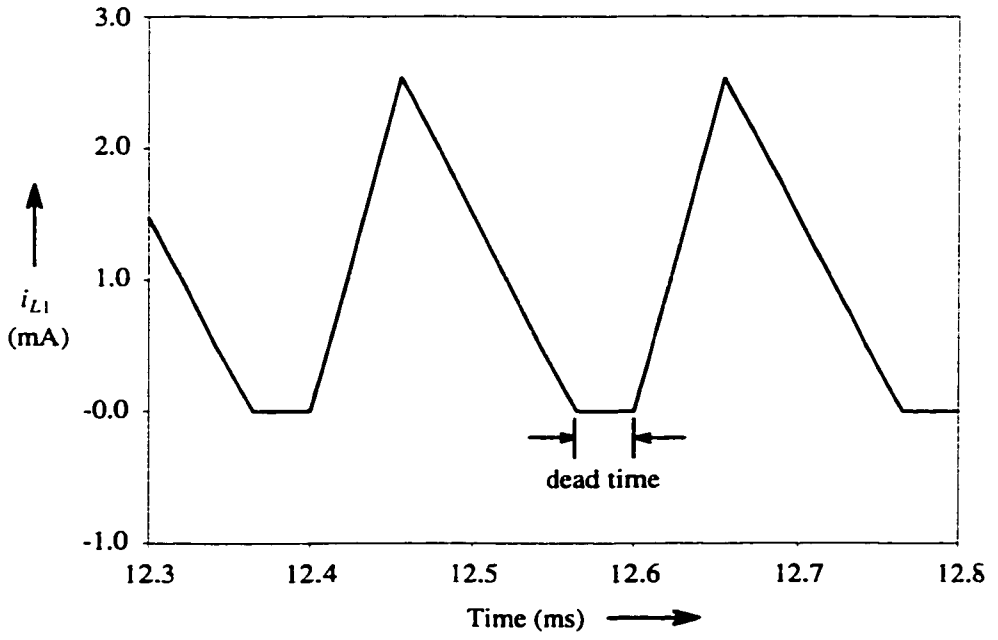


Fig. 2.13 Auxiliary inductor current modulated by the rectified line voltage

2.5.3.1 Effects on the value of the Auxiliary Inductor

The value of the auxiliary inductor affects the bulk capacitor voltage which determines the maximum load capability and the voltage rating of the semiconductors of the converter.

If the value of the auxiliary inductor is decreased, a larger current in the inductor is produced (i_{Llpeak_1}), which in effect increases the bulk capacitor voltage. The voltage ratings of the switch and output diodes may be increased in this case.

If the value of the auxiliary inductor is increased, a smaller current in the inductor is produced (i_{Llpeak_1}), which in effect decreases the bulk capacitor voltage. The voltage ratings of the semiconductors can be decreased in this case.

The effect with different values of auxiliary inductor on the bulk capacitor voltage with various output current levels are shown in Fig. 2.14.

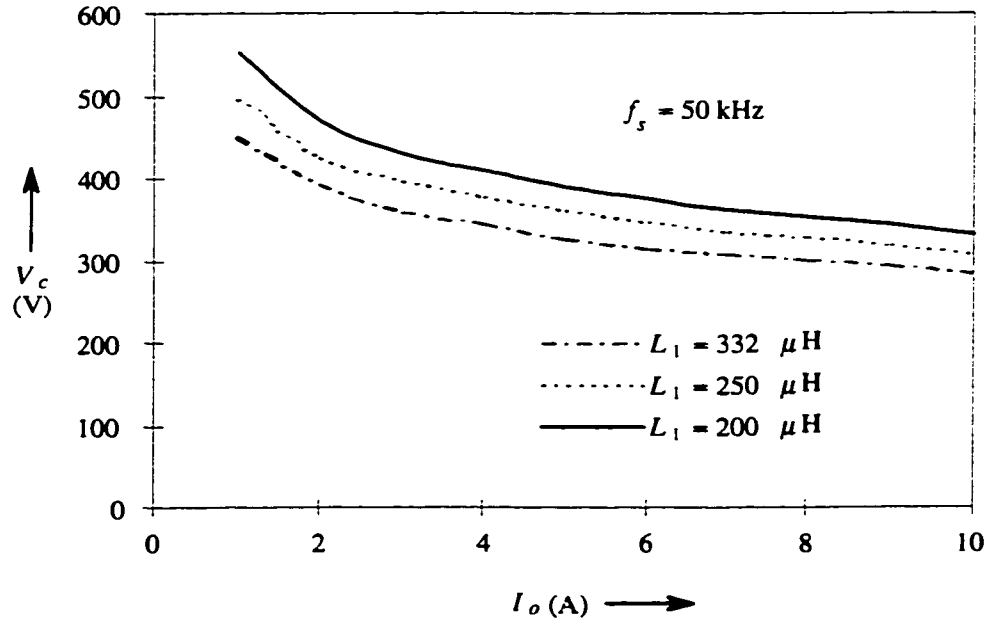


Fig. 2.14 Capacitor voltage versus output current for various values of L_l

The following points are observed from Fig. 2.14;

i) For a given output load, the capacitor voltage is higher for a lower value of L_1.

ii) The DC capacitor voltage increases for decreasing output load current.

2.5.3.2 Boundary of Continuous and Discontinuous current in the auxiliary Inductor

The converter's auxiliary circuit is designed to operate in the discontinuous current mode. As long as the current in L_1 is always discontinuous, the input current will be sinusoidally modulated and the power factor will be close to unity. In the correct design of the converter, the current in the auxiliary inductor is on the boundary of continuous mode of operation when the input voltage is at low line and the output load current is at maximum. The continuous current mode of operation is entered when the duration t_x of interval 2, exceeds t_3 as shown in Fig. 2.2. This mode can occur at the peak of the input sine wave where the differential voltage between V_c and the peak rectified input voltage is the smallest. Fig. 2.15 illustrates the current in the auxiliary inductor at the boundary of continuous current. Note the bump at the peak of the auxiliary inductor current. Fig. 2.16 illustrates the current in the auxiliary inductor with profound region of continuous conduction, including an exploded view in Fig. 2.17.

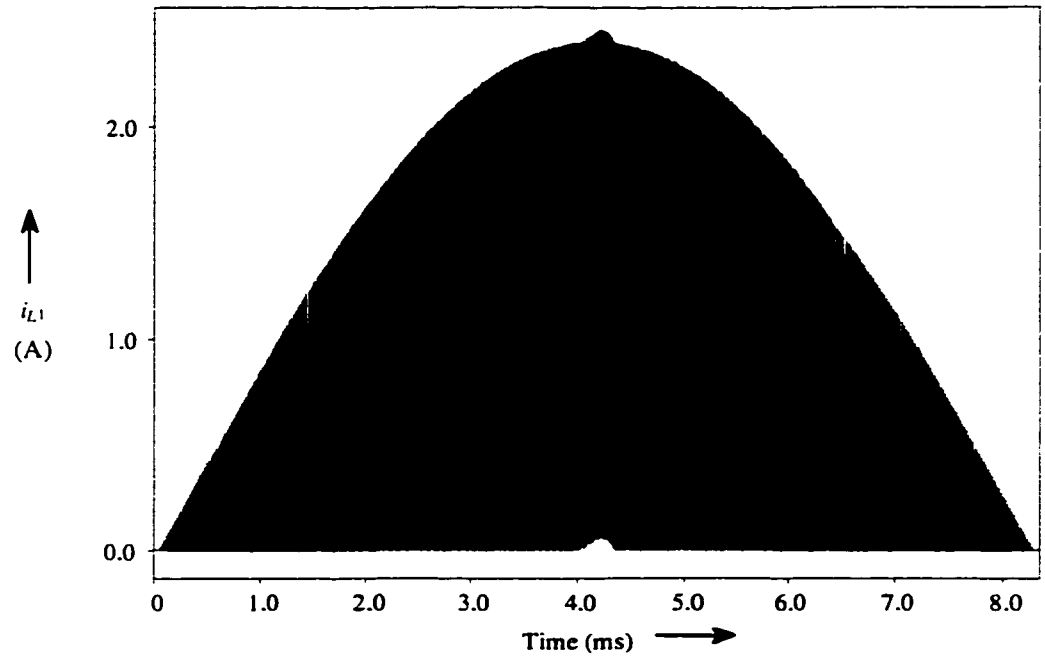


Fig.2.15 Current in the auxiliary inductor at the boundary of continuous current

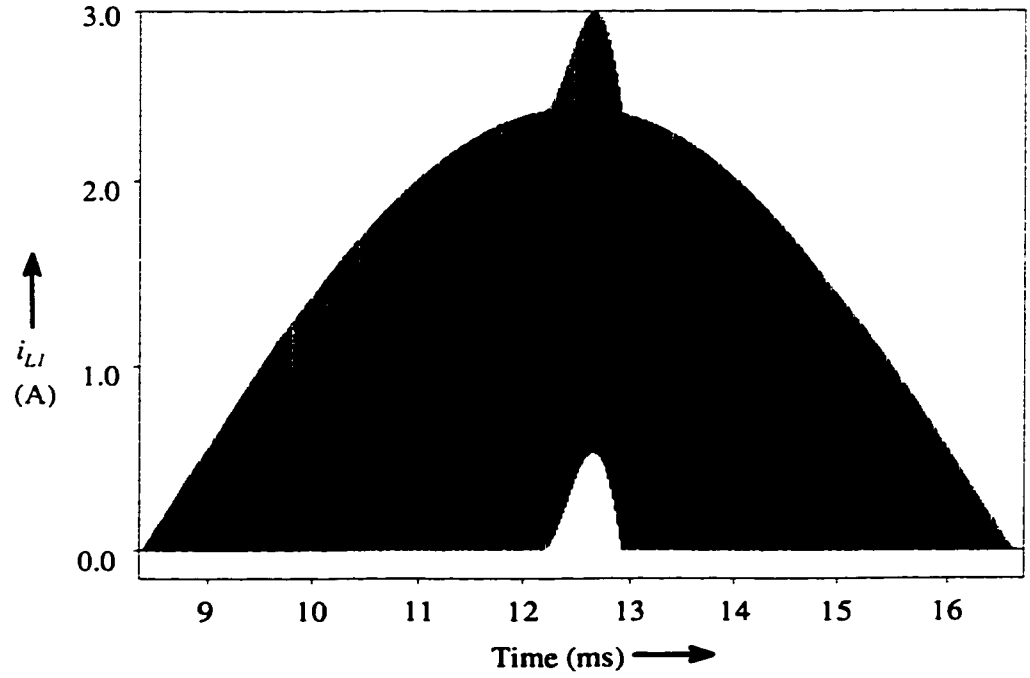


Fig.2.16 Current in the auxiliary inductor in profound continuous current

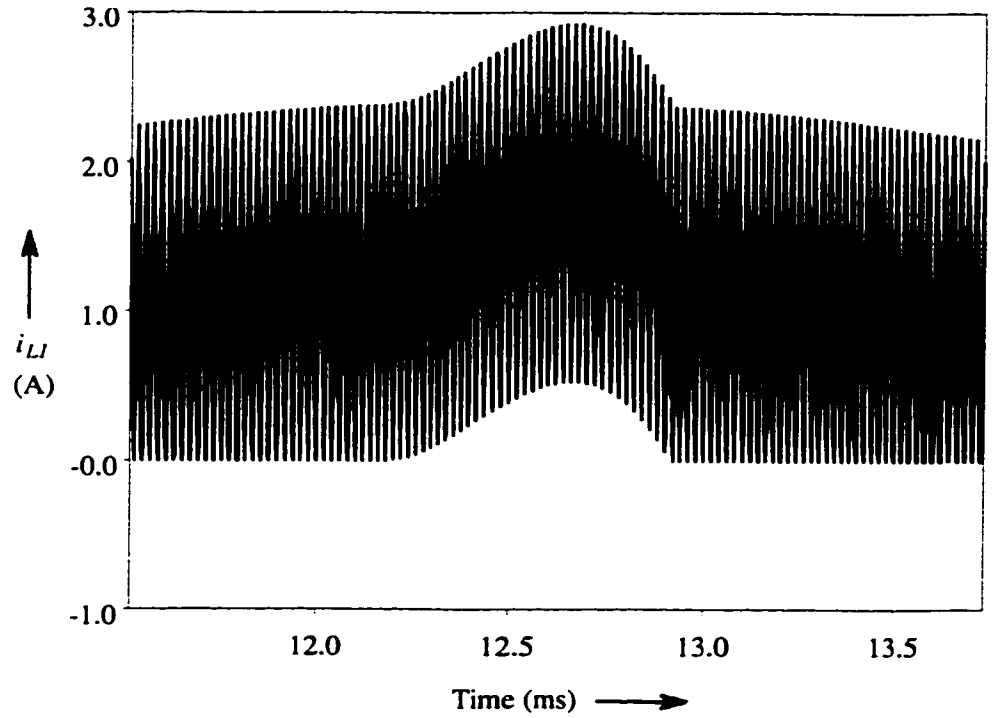


Fig. 2.17 Exploded view of the Current in the auxiliary inductor in profound continuous current.

From Fig. 2.15, Fig. 2.16, and Fig. 2.17, it can be said that the specific converter is operating beyond its maximum power level.

Fig. 2.18 illustrates a typical rectified input voltage V_c and during one period of the 60 Hz input voltage.

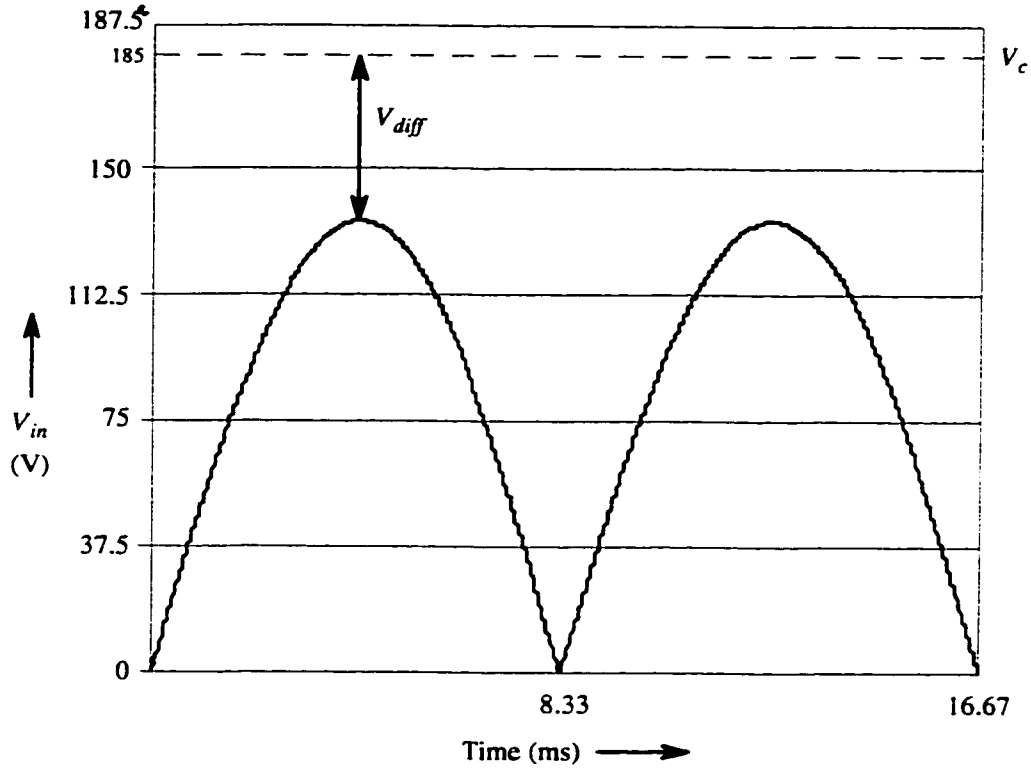


Fig. 2.18 Rectified input voltage

The minimum differential voltage required so that current in L_1 remains discontinuous is determined by

$$V_{diff} = \sqrt{2} \cdot V_{in} \cdot \left(\frac{D}{(1-D)} \right) \tag{2.33}$$

Thus the capacitor voltage V_c at the boundary is given by

$$V_{cboundary} = \sqrt{2} \cdot V_{in} \cdot \left(1 + \frac{D}{(1-D)} \right) \tag{2.34}$$

From equations (2.25) and (2.34), D can be found at the boundary to be

$$D = \frac{V_o \cdot N_{ps}}{\left(V_o \cdot N_{ps} + \sqrt{2} \cdot V_{in} \right)} \tag{2.35}$$

The value of L_1 to maintain discontinuous current flow can easily be solved by

$$\left[\sum_{k=0}^{n}\frac{1}{2}\cdot V_{ink}{}^{2}\cdot\frac{t_{on}{}^{2}}{L_1}\cdot\left(\frac{1}{V_{cboundary}-V_{ink}}\right)\right]-\left[n\cdot i_s{}'\cdot t_{on}\right]=0 \qquad (2.36)$$

as L_1 is the only unknown variable.

2.5.4 Input Current, Harmonic Content and power factor

The current through the auxiliary inductor i_{L_1} follows the same path as the input current. Thus, the unfiltered input current is the same as the auxiliary inductor current except that the current's magnitude is negative during alternative half cycles. This unfiltered input current was shown in Fig. 2.3. If the average current per switching interval is taken, the filtered input current is obtained. The average current per switching interval is determined by

$$i_{in}=i_{L1\,avg_k}=\frac{1}{2T_{sw}}\cdot i_{L1\,peak_k}\left(t_{on}+t_{x_k}\right) \qquad (2.37)$$

This filtered waveform is shown in Fig. 2.19.

It can be seen from Fig. 2.19 that the filtered input current is not purely sinusoidal but distorted.

By taking the Fourier transform of the filtered input current, the harmonic content is determined. Fig. 2.20 illustrates the harmonic content of the waveform of Fig. 2.19.

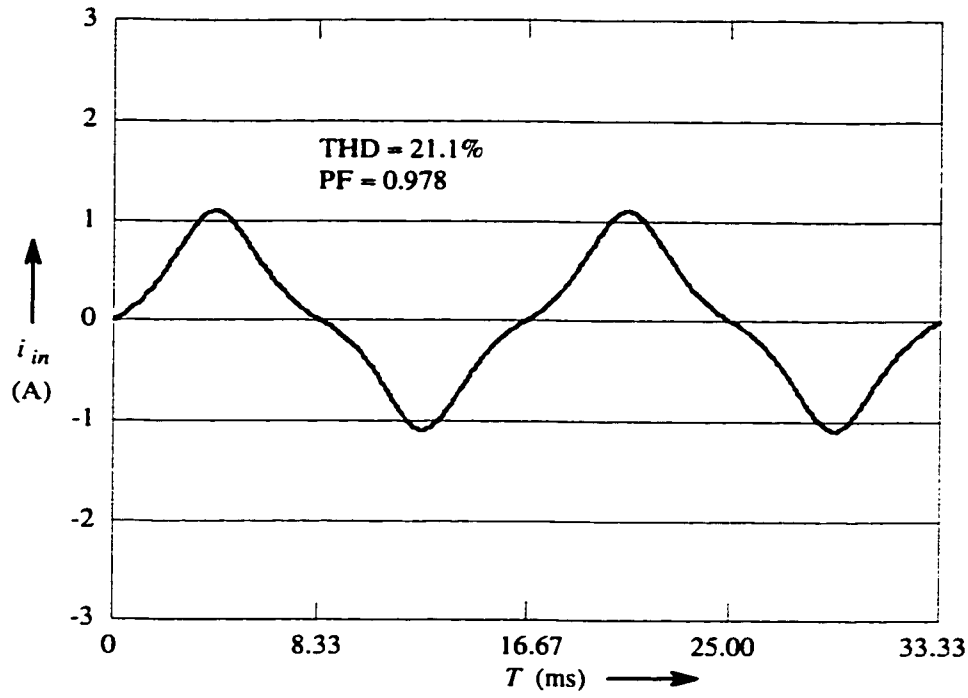


Fig. 2.19 Filtered input current (V_{in} = 110 V, V_o = 5 V, V_c = 230 V, I_o = 10 A)

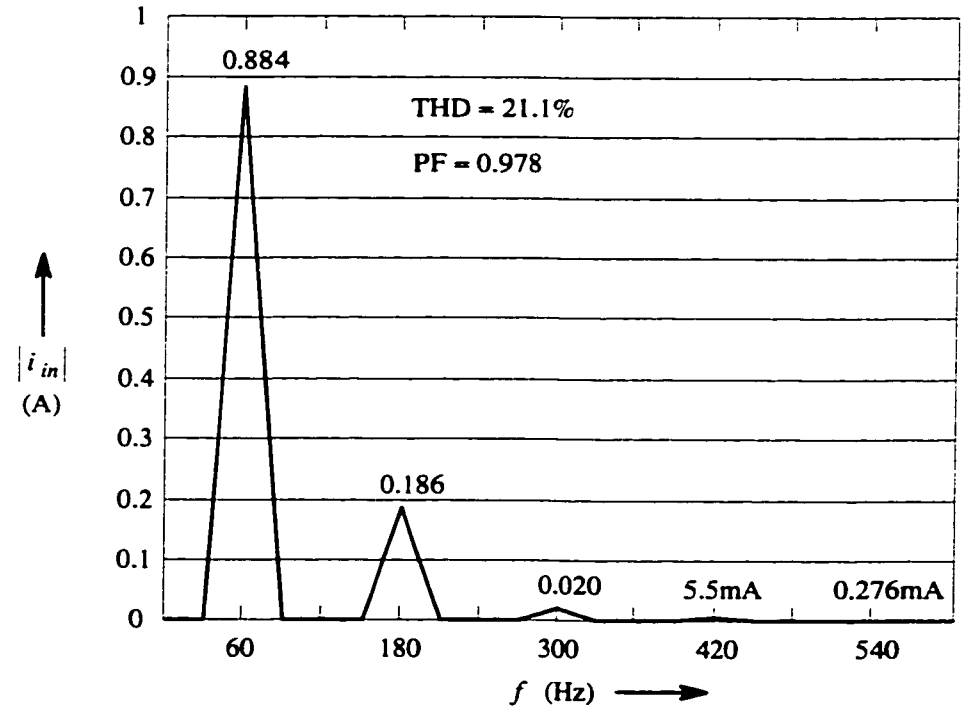


Fig. 2.20 Harmonic spectrum of the filtered current waveform of Fig. 2.19

Figure 2.20 shows the 3rd and 5th harmonic are approximately 21% and 2.2% of the fundamental current respectively.

The total harmonic distortion (*THD*) is determined by

$$THD = \frac{\sqrt{\left(I_3^2 + I_5^2 + I_7^2 + I_9^2\right)}}{I_1} \tag{2.38}$$

The power factor (*PF*) is given by

$$PF = \frac{1}{\sqrt{1+(THD)^2}} \tag{2.39}$$

The filtered input current waveform from Fig. 2.19 contains a large 3rd harmonic. The large third harmonic is caused by the modulation of the inductor current i_{L_1} during interval 2. An analysis of this effect was reported in [22].

The effective filtered current is given by

$$i_{inrms} = \sqrt{\frac{T_{sw}}{T_{ac}} \cdot \left[\sum_{k=0}^{n} \left(i_{L1avg_k}\right)^2\right]} \tag{2.40}$$

2.5.5 Current and Voltage Rating of the MOSFET Switches

The MOSFET switch Q1, carries the sum of the auxiliary inductor current and the reflected output current during interval 1 as shown in Fig. 2.2. The effective current is determined by

$$I_{swrms} = \sqrt{\frac{1}{3 \cdot T_{ac}} \left[\sum_{k=0}^{n} \left[i_s' + \frac{(V_{in_k})}{L_1} \cdot t_{on} \right]^2 \cdot t_{on} \right]} \tag{2.41}$$

The RMS current is greatest when the converter is operating at full load and at minimum input voltage. The maximum voltage stress across the switch occurs during high line when twice the bulk capacitor voltage is applied across the switch Q1.

Conduction losses can be calculated from equations (2.41) and

$$P_{swcond} = (i_{swrms})^2 \cdot R_{dson} \tag{2.42}$$

The charging and discharging of the body drain-source capacitance will be dissipated in the switches and can be calculated by

$$P_{cv} = \frac{1}{2} \cdot C_{oss} \cdot V_c^2 \cdot f \tag{2.43}$$

The turn on losses is determined by

$$P_{swon} = \frac{1}{2} \cdot i_s' \cdot V_c \cdot t_{rise} \cdot f \tag{2.44}$$

where t_{rise} is the time required for the current in the switch to increase from zero to rated current.

The turn off losses is determined by

$$P_{swoff} = \left[\sum_{k=0}^{n} \frac{1}{2} \cdot \left[i_{Lipeak_k} + i_s' \cdot t_{on} \right] \cdot V_c \cdot t_{fall} \right] \cdot \frac{1}{T_{ac}} \tag{2.45}$$

where t_{fall} is the time required for the current in the switch to decay to zero Ampere. The power losses in the switch consists mostly of turn-off losses.

2.5.6 Output Filter Characteristics

The output inductor is designed exactly the same manner as per a standard forward converter. The minimum output current required before i_{L_o} enters the boundary of discontinuous is assumed to be 10 percent of the maximum rated current.Thus, the ac ripple is small compared to the output current. The value of L_o is determined by

$$L_o = \frac{t_{on} \cdot \left(\frac{V_c}{N_{ps}} - V_o \right)}{(0.2 \cdot I_o)} \tag{2.46}$$

The output voltage ripple is determined by

$$\Delta V_{C_o} = \frac{(T_{sw})^2 \cdot (1 - D)}{8 \cdot L_o \cdot C_o} \tag{2.47}$$

For a given specification for the output voltage ripple, C_o is solved using equation (2.47). This equation excludes the ESR value of the output capacitor which also contributes to the output voltage ripple. Another criteria in determining the value of the output capacitor is from load transients. The energy stored in the output inductor is dumped to the output capacitor under a load removal transient,

Thus, C_o is determined by the maximum overshoot allowed at the output and given by

$$C_o = \frac{L_o \cdot I_o^2}{(V_p^2 - V_o^2)} \tag{2.48}$$

where V_p is the maximum allowable voltage at the output under transient load condition.

2.5.7 Experimental Results

A 50W prototype to convert 110 Vac (± 20%) to a regulated 5 Vdc was built in the laboratory to validate the theoretical results. Fig. 2.21 shows the experimental input line current while Fig. 2.19 shows the theoretical input line current. The comparison of the two show that they are very similar waveforms.

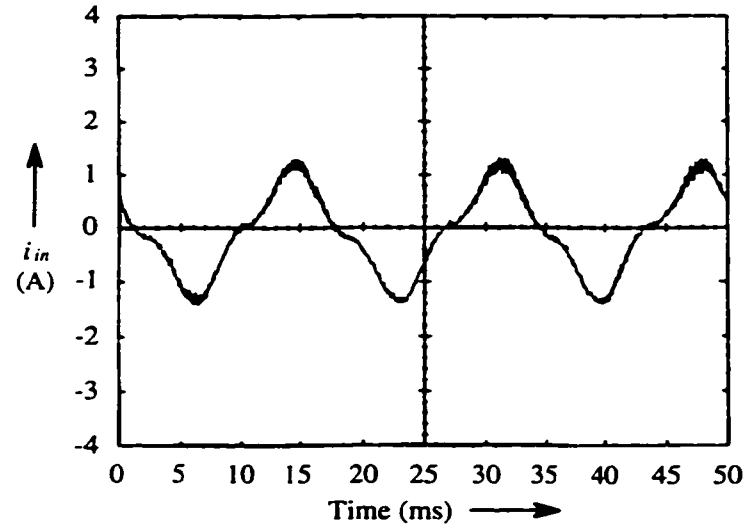


Fig. 2.21 Experimental input line current waveform at rated full load.
(V_{in} = 110 V, I_o = 10 A, V_{out} = 5 V, f_{sw} = 50 kHz, V_{dc} = 387 V, PF = 0.96, efficiency = 78 %).

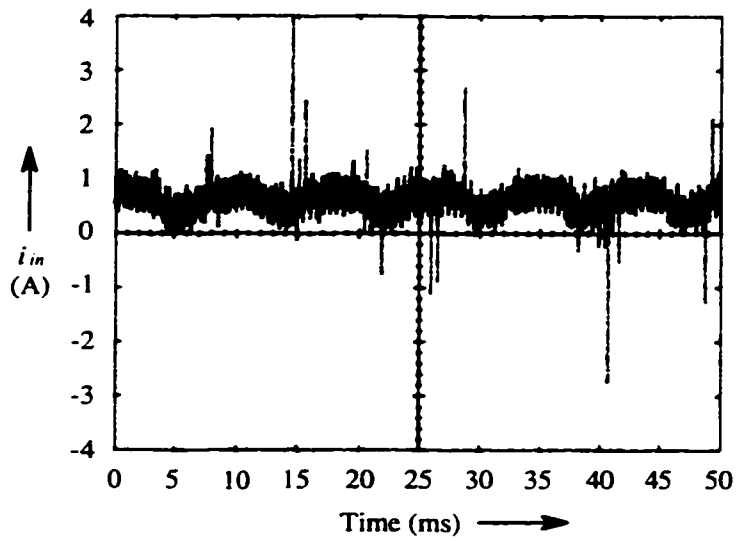


Fig. 2.22 Experimental output dc bus ripple waveform at rated full load.
(V_{in} = 110 V, I_o = 10 A, V_{out} = 5 V, f_{sw} = 50 kHz, V_{dc} = 387 V, PF = 0.96, efficiency = 78 %).

The experimental output voltage ripple is shown in Fig. 2.22. As expected, the high loop gain of the controller rejects the 120 Hz ripple at the output as in a standard forward converter. The 120Hz ripple is less than 25mVp-p as shown in Fig. 2.22.

The efficiency of the converter is shown in Fig. 2.23 for various operating conditions. It can be seen from this figure that the efficiency rapidly drops when the load current decreases from approximately 80% of full load with an input voltage of 135 Vac.

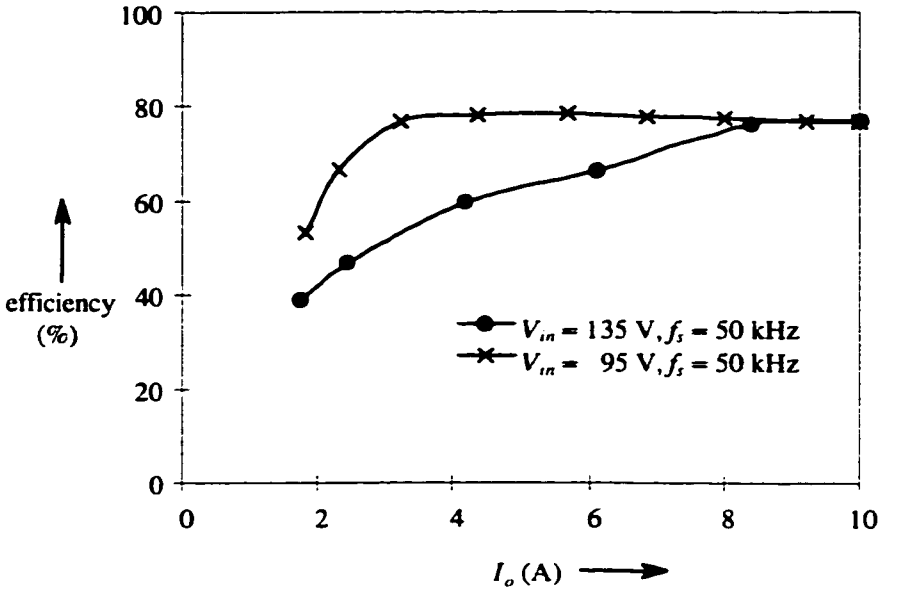


Fig. 2.23 Experimental efficiency of the converter for various operating conditions.

This effect is due to the processing of the auxiliary inductor current i_{L1} by the MOSFET switch as it is modulated by the input line voltage.The higher magnitude in line voltage gives rise to higher current in the auxiliary inductor which is processed through the MOSFET switch. Therefore the ratio between the auxiliary inductor current to the reflected output current (i_{L1}: i_s') is higher at light loads in effect degrading the efficiency of the converter.

The experimental input power factor for various operating conditions is shown in Fig. 2.24. The power factor obtained is high and meets the IEC10003-2 specification.

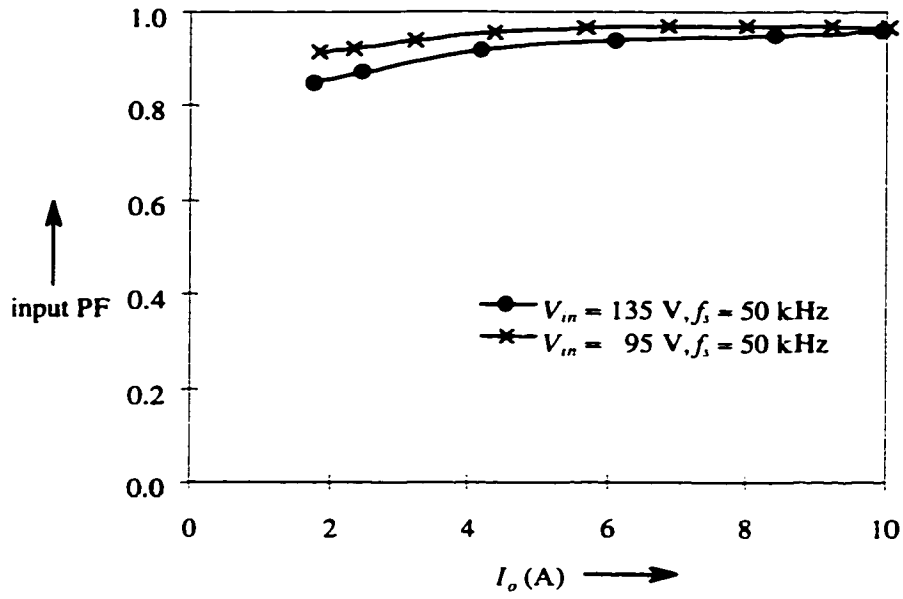


Fig. 2.24 Experimental input power factor for various operating conditions.

Table 2-1 shows values of various components used in the prototype.

Table 2-1

Component	Value	Manufacturer
L_1	332 µH	In House
C_1	100 µF / 400 V	Nipon Chemi-Con
PWM	UC3844	Unitrode
Q_1	IRFPE50	IR
D_5, D_6	10 A / 45 V schotky	Mototrola
D_4	MUR1100E	Motorola
D_1-D_3, D_7-D_{10}	MUR460	Motorola
C_{s1}, C_{s2}	1 µF / 200 Vdc	Sprague
L_{s1}	-	-
C_o	4000 µF / 25 Vdc	United Chemi-Con
L_o	100 µH	In House

2.6 Conclusions

A single stage, single switch isolated ac/dc converter topology which has high input power factor, hold-up time capability and no low frequency component in the output voltage has been presented in this chapter.

However, there are a few disadvantages which compromises the usefulness of this converter. The most important draw back is the bulk voltage variation which is load dependent. The bulk voltage is to high at light loads which hinders the operation of the converter to operate from a universal input voltage range. Therefor, the operation of the converter is restricted to an input voltage range of 90 V - 135 V.

Based on the theoretical and experimental results, it is concluded that the proposed converter is best suited for low power applications where cost is one prime objective.

CHAPTER 3

A VARIABLE FREQUENCY, SINGLE STAGE, SINGLE SWITCH POWER FACTOR CORRECTED AC/DC CONVERTER

3.1 INTRODUCTION

The proposed converter of chapter 2 is simple and obtains input current wave shaping with a regulated output dc voltage. However, the bulk voltage has a large variation from minimum to maximum load output currents. A method in reducing this large voltage variation will be introduced in this chapter.

This chapter presents a variable frequency, single stage, single switch isolated converter topology which achieves a regulated dc output voltage having no low frequency components and a high input factor. By operating the converter with a higher frequency at light loads, lower voltage stresses on the power components and an increase in the efficiency of the converter at light loads can be achieved. The proposed converter is designed to operate with a variable frequency range of 50 to 90kHz. The proposed converter operates with the same load and line requirements as with the converter of chapter 2. The proposed converter operates with the output inductor in continuous current mode.

In the following sections, the description of the proposed converter, the analysis, performance characteristics and experimental results will be given.

3.2 CIRCUIT DESCRIPTION OF THE PROPOSED CONVERTER

The proposed converter circuit is shown in Fig. 3.1. The circuit is almost identical to the circuit of chapter 2 except for the difference in the control circuitry. The control circuit consists of a PWM, Opto-coupler, and a variable frequency control circuitry. The variable frequency control (VFC) circuitry is shown in Fig. 3.2. The VFC circuit consists of a few resistors a zener diode and an operational amplifier.

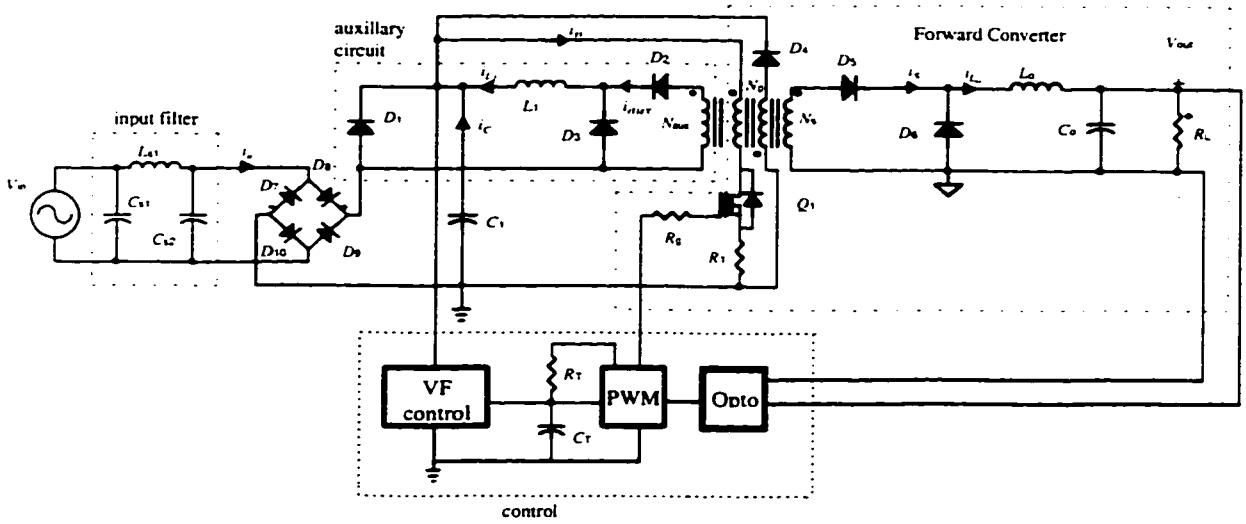


Fig. 3.1 Power and control circuits of the proposed converter.

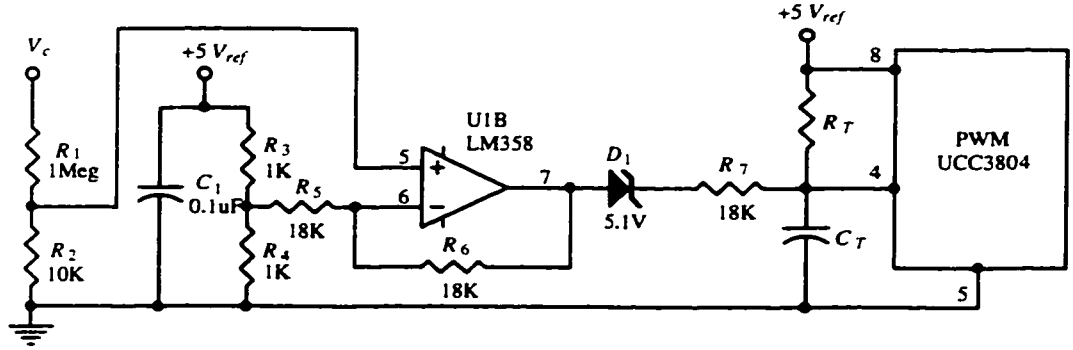


Fig. 3.2 Variable Frequency Circuit.

3.3 PRINCIPLES OF OPERATION

The operation of the converter is almost identical to the converter of chapter 2 except that the operating frequency increases at light loads. This section will focus on the operation of the VFC circuit.

From Fig. 3.2, R_3 and R_4 forms a voltage divider of 2.5 Volts and R_1 and R_2 form a voltage divider of approximately 1 percent of the bulk voltage.

The bulk voltage is below 250 Volts at high output currents. The negative input of the operational amplifier is at a higher potential than the positive input, therefore the output voltage of the op-amp is zero volt. D_1 is reversed biased and there is no current flow through R_7. C_T is charged only from R_T as no additional current is supplied from the op-amp to help charge C_T. The rate which C_T charges in this condition would give the lowest operating frequency of the converter.

As the load current is decreased, the bulk voltage increases above 250 Volts and the output voltage of the op-amp increases from zero volts. As the bulk voltage further increases, D_1 starts to conduct and current flows through R_7 to C_T. This additional current from R_7 with the charging current of R_T, charges C_T quicker thus increasing the frequency of the PWM which in effect increases the frequency of the converter.

3.4 STEADY STATE ANALYSIS

The steady state analysis of the converter is the same as section 2.4 of chapter 2.

3.5 PERFORMANCE CHARACTERISTICS

The effect on the operation of the converter with variable frequency control will be examined in this section.

3.5.1 Effect of Transformer Turns Ratio on the Input Power Factor

This effect is the same as section 2.5.1 of chapter 2.

3.5.2 Dc Bulk Capacitor Current and Voltage

The proposed converter tries to eliminate the large bulk voltage variations seen with the converter of chapter 2. Fig. 2.6 in chapter 2 illustrated the variation of the bulk voltage with changes to the output load current. In trying to reduce this effect, the proposed converter's operating frequency is increased at light loads. It can be seen from equation (2.21) that i_{L_1} is a function of t_{on} . If t_{on} can be reduced, then i_{L1peak_i} will be reduced which in effect reduces the current charging the bulk capacitor during interval 2. Therefore, by increasing the frequency, t_{on} is reduced. The theoretical variation in frequency versus output current for a fixed bulk voltage is shown in Fig. 3.3.

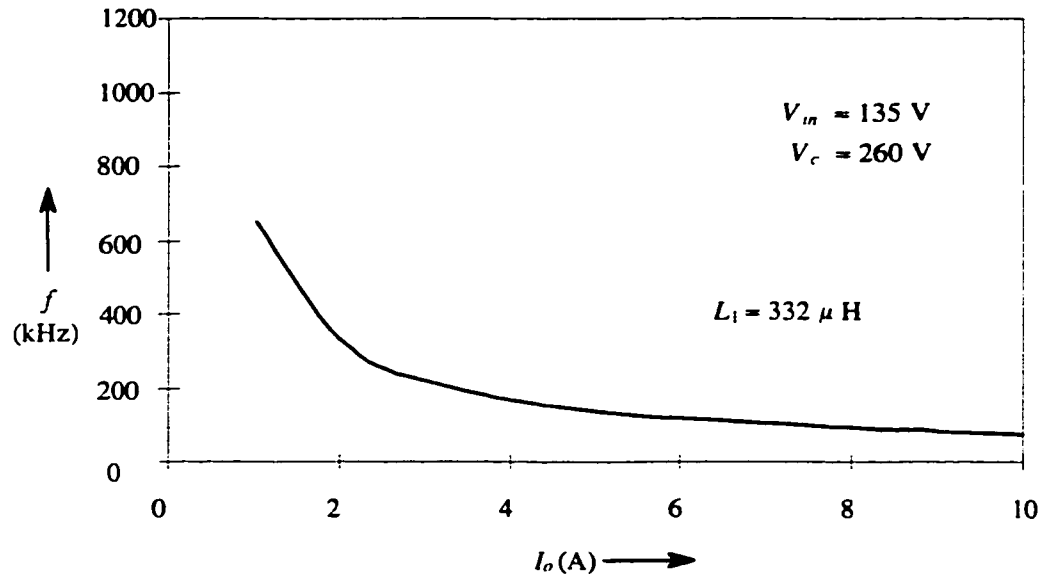


Fig. 3.3 Variation in frequency for various operating conditions of the converter.

It can be seen from Fig. 3.3 that there is a variation in frequency of approximately 15 times from minimum to maximum load while maintaining a fixed bulk voltage. This large variation in frequency is difficult to implement practically. The proposed converter has a frequency variation of approximately two times. The frequency range of the proposed converter is not enough to cover the entire load variation. As the highest frequency of the converter is reached, the bulk voltage will start to rise as the output load current is further decreased.

3.5.3 Auxiliary Inductor Current

The auxiliary inductor current analysis is the same as section 2.5.3 of chapter 2.

3.5.3.1 Effects on the value of the Auxiliary Inductor

Fig. 3.4 illustrates different required operating frequencies for various values of L_1 while maintaining the same bulk voltage variation over the output current range. The operating frequency of the converter is different for different values of L_1. It is shown that with a value of L_1 = 332 μH, the operating frequency of the converter is 50 kHz for the indicated bulk voltage. For a value of L_1 = 250 μH and L_1 = 200 μH, the operating frequency is 66 kHz and 83 kHz respectively.

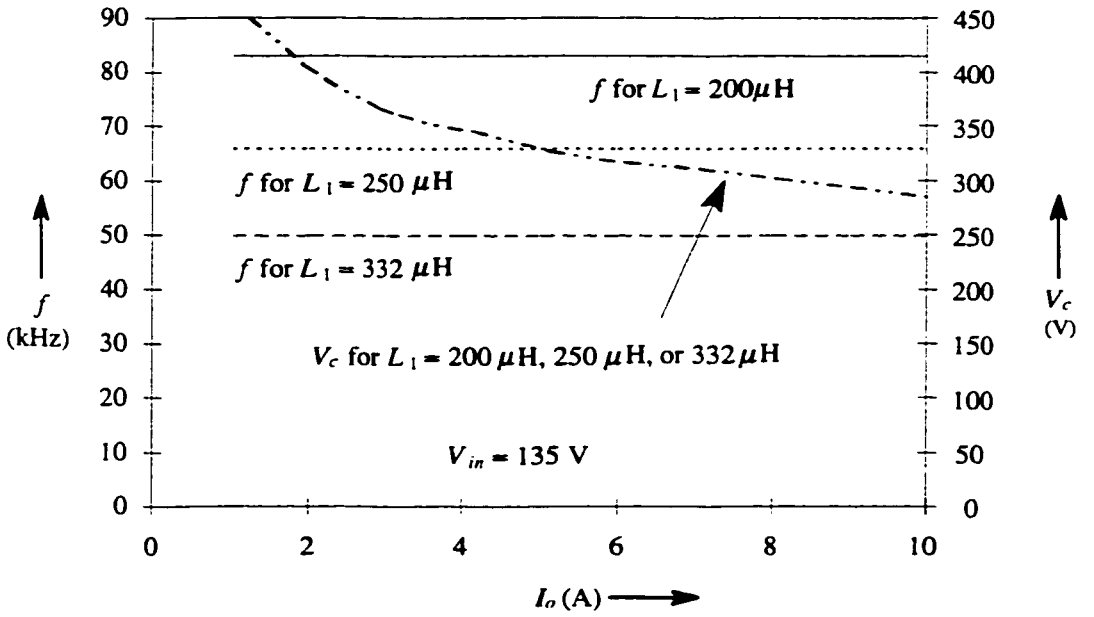


Fig. 3.4 Capacitor voltage versus output current for a fixed switching frequency for different values of L_1 .

3.5.3.2 Boundary of Continuous and Discontinuous current in the Auxiliary Inductor

The frequency variation versus output current for three different values of L_1 is shown in Fig. 3.5. The discontinuous boundary for all three curves is the area below their respective curve. The continuous boundary for all three curves is the area above their respective curve. It can be seen from Fig. 3.5 that the large frequency variation occurs below an output load current of approximately three amps.

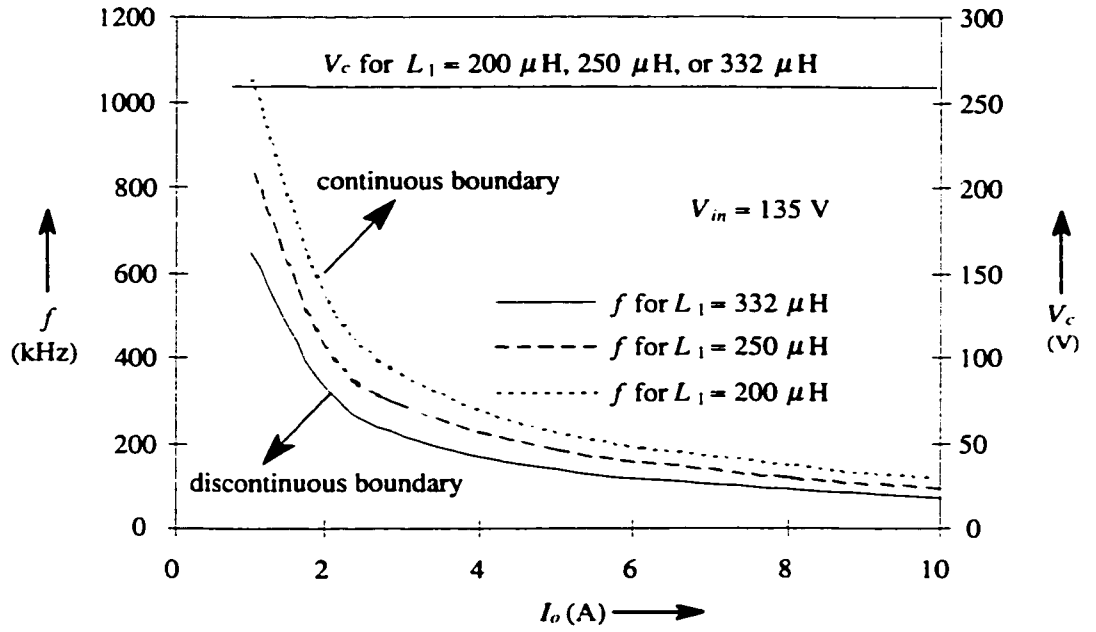


Fig. 3.5 Boundary of continuous and discontinuous mode of operation for different values of L_1 .

3.5.4 Input Current, Harmonic Content and power factor

The input current has the same waveshape as Fig. 2.19 of chapter 2. The high frequency harmonics are filtered by the EMI filter.

3.5.5 Current and Voltage Ratings of the Mosfet Switch

The ratings of the mosfet switch will be the same as section 2.5.5 of chapter 2.

3.5.6 Output Filter Characteristics

The output filter characteristics are the same as section 2.5.6 of chapter 2.

3.5.7 Experimental Results

The same prototype as in chapter 2 was used with the addition of the VFC components of Fig. 3.2. Fig. 3.6 illustrates the performance on the bulk voltage V_c between the converter of chapter 2 and with the proposed converter with the VFC circuitry. The frequency range of the proposed converter was from 50 kHz to 90 kHz. At the maximum output load current, the VFC circuitry was already active due to the bulk voltage being above 250 Vdc. This is why the two curves do not merge at full load. The VFC circuitry is at its maximum frequency when the output load current is about 6 A. Further decreasing the load current gives rise in the bulk voltage as shown.

The efficiency of the converters are shown in Fig. 3.7 and illustrates that when the converters are operating with an input voltage of 135 Vac, the variable frequency converter has a greater efficiency throughout the output current range. This was expected as i_{Lipeak_i} is reduced with the implementation of the VFC circuitry.

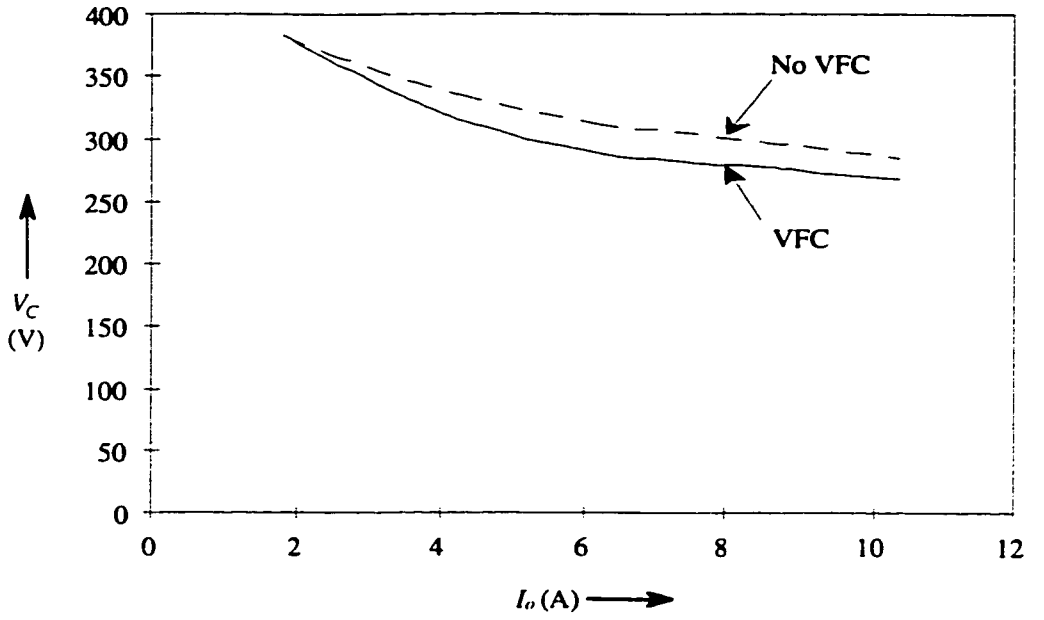


Fig. 3.6 Bulk voltage comparison between converter with and without VFC.

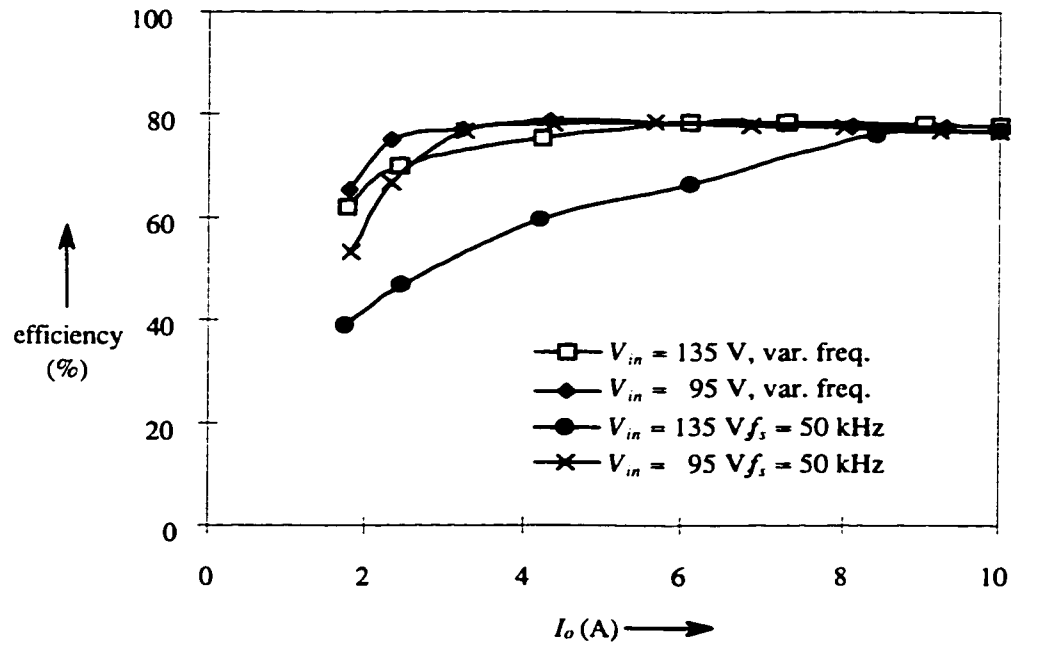


Fig. 3.7 Experimental results showing efficiency for prototype converters. Efficiency for fixed frequency and variable frequency single stage converters.

The experimental power factor of both converters is shown in Fig. 3.8. At light loads, a degradation of power factor is seen. This is due to the increasing capacitive displacement factor at light loads caused by the EMI filter capacitor connected across the line.

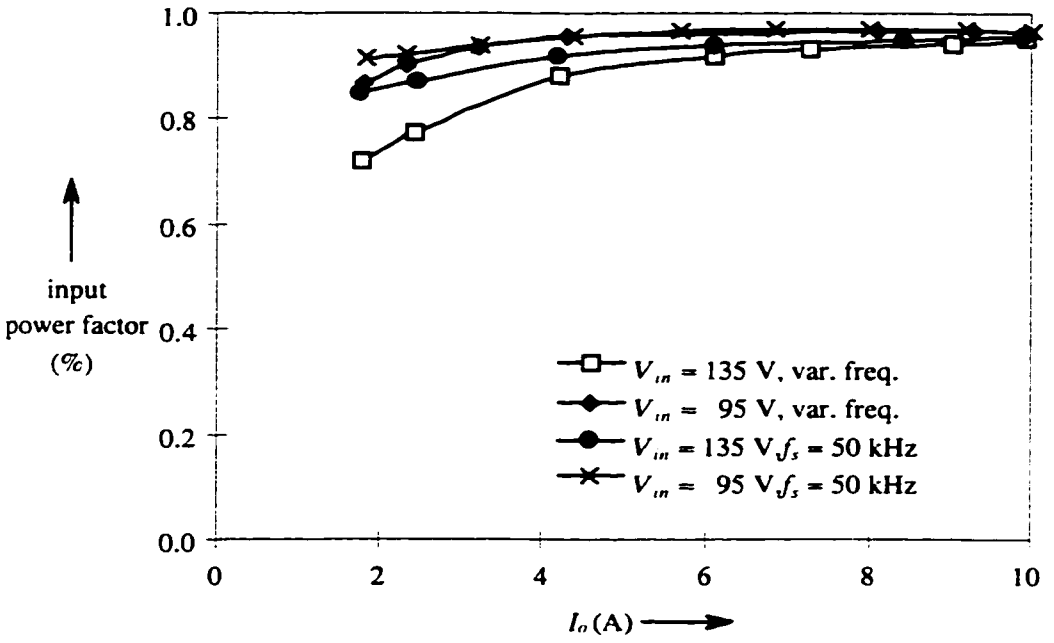


Fig. 3.8 Experimental results showing the power factor for the proposed converters. Power factor for fixed frequency and variable frequency single stage converters.

3.6 CONCLUSION

A variable frequency control circuitry added to the proposed converter of chapter 2 improved the efficiency of the converter at light loads. However, the frequency variation needed to reduce or eliminate the large bulk voltage variation is very wide and therefore difficult to implement practically.

Based on the obtained results, this converter is also best suited for low power applications.

CHAPTER 4

A SINGLE STAGE POWER FACTOR CORRECTED AC/DC CONVERTER

4.1 INTRODUCTION

The proposed converters of Chapter 2 and 3 are simple and obtain input current wave shaping with a regulated dc output voltage. However, there is large bulk voltage variations with both converters. They are also restricted to operate from the North American ac mains due to the large voltage stress on the MOSFET switch.

This chapter presents a single stage isolated converter topology designed to achieve a regulated dc output voltage having no low frequency components and a high input power factor. The topology is derived from the basic two switch forward converter. The converter's output inductor is operated in discontinuous current mode to eliminate the bulk voltage variations due to the output load current variation. The proposed converter operates from a universal input voltage of (90 - 265 V). The converter has an output power of 150 Watts and operates with a switching frequency of 50 kHz. The output voltage of the converter is 54.75 Vdc .

Analysis of the converter is presented and performance characteristics are given. Design guidelines to select critical components of the circuit are presented. Experimental results are given which confirm the predicted performance of the proposed topology.

4.2 CIRCUIT DESCRIPTION OF THE PROPOSED CONVERTER

The proposed converter circuit is shown in Fig. 4.1 **Power**. The converter is derived from the basic two switch forward with the addition of the auxiliary circuit. The control of the output voltage of the proposed circuit is identical to a conventional two switch forward converter.

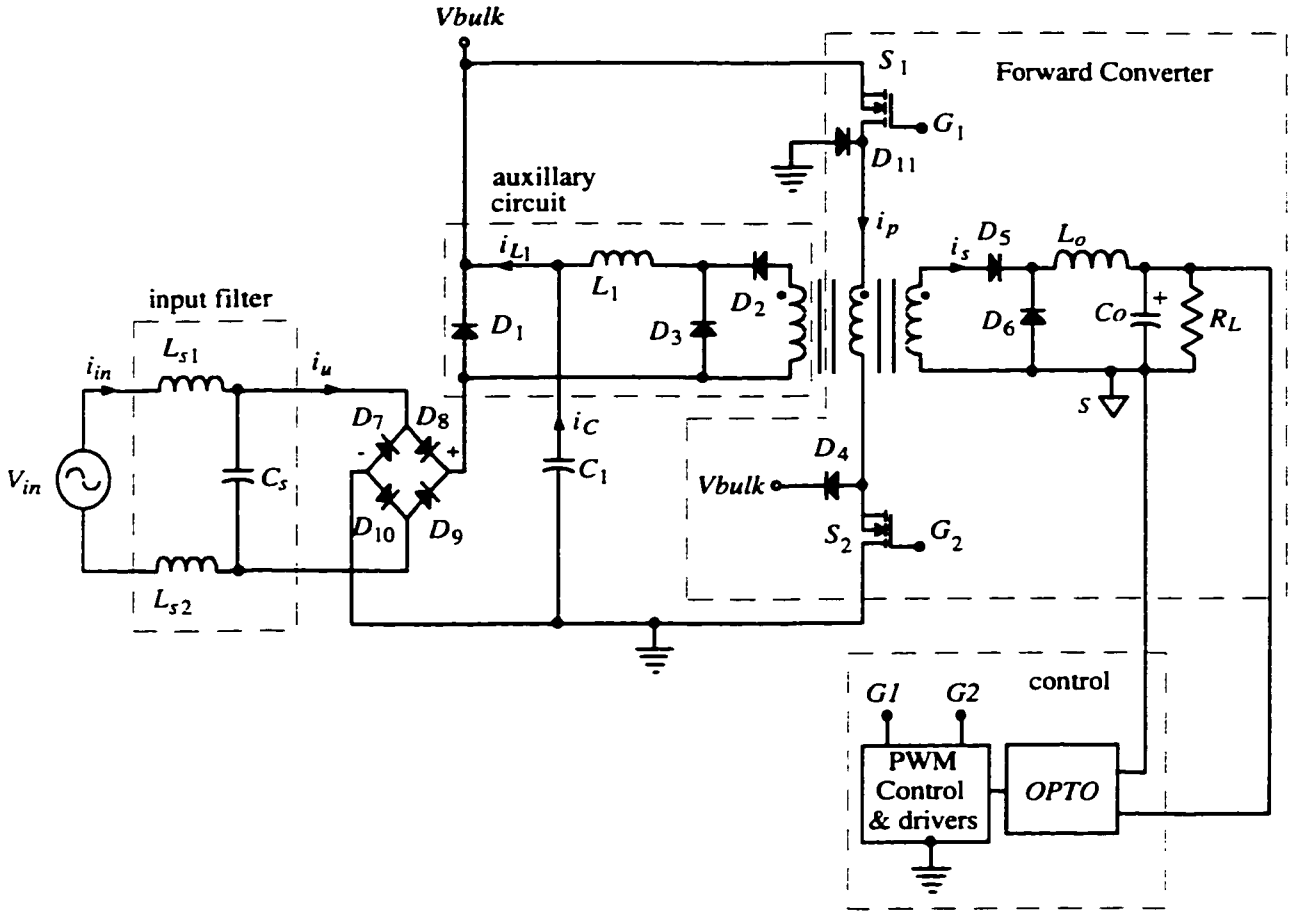


Fig. 4.1 Power and control circuits of the proposed converter.

4.3 PRINCIPLES OF OPERATION

The operation of the circuit is similar to the converter of Chapter 2. The difference lies with the operation of the output inductor in discontinuous current mode which affects the auxiliary circuit. The effect is shown in Fig. 4.2 where the bulk capacitor current (i_{c1}) commences from zero and decays with a slope equal to the output inductor current during interval 1. As the load is decreased from the maximum rated output current, the converter regulates the output voltage by decreasing the duty cycle. This results in a smaller peak auxiliary inductor current therefore charging the bulk capacitor less during interval 2. In effect, the bulk voltage does not increase as the load is decreased.

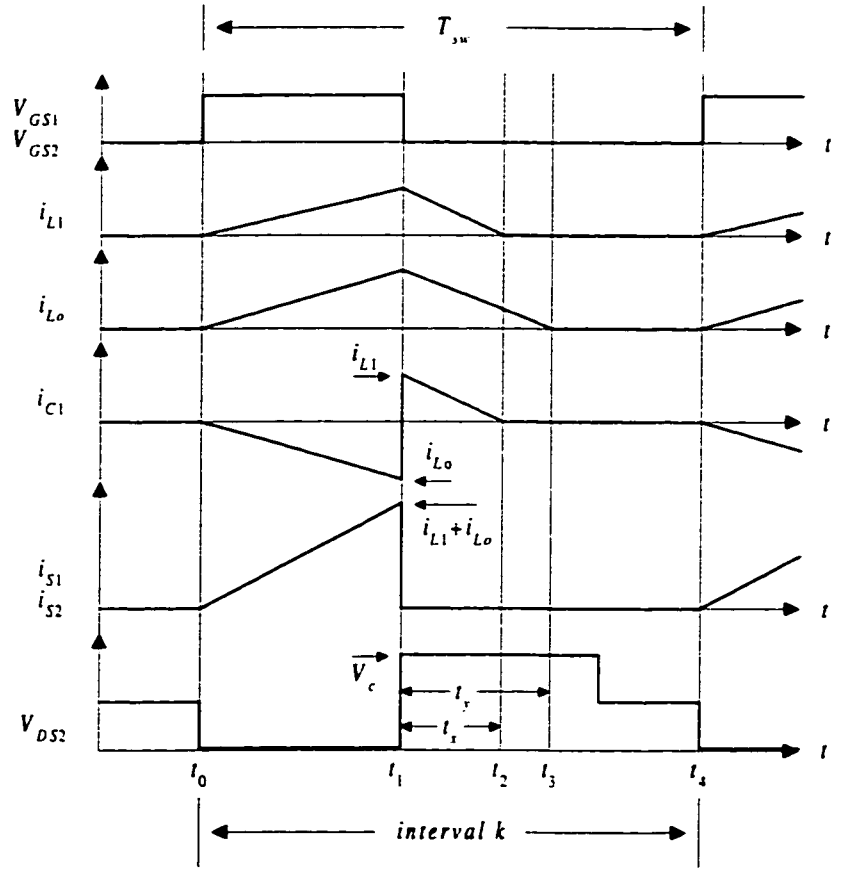


Fig. 4.2 Operational waveforms of the proposed converter.

4.4 STEADY STATE ANALYSIS

A simplified analysis is performed by dividing the operation of the converter into three different intervals. The analysis is based on the same assumptions of Chapter 2 except for:

(*i*) The output inductor L_o, is small enough so that the current in the inductor is discontinuous below rated output load current.

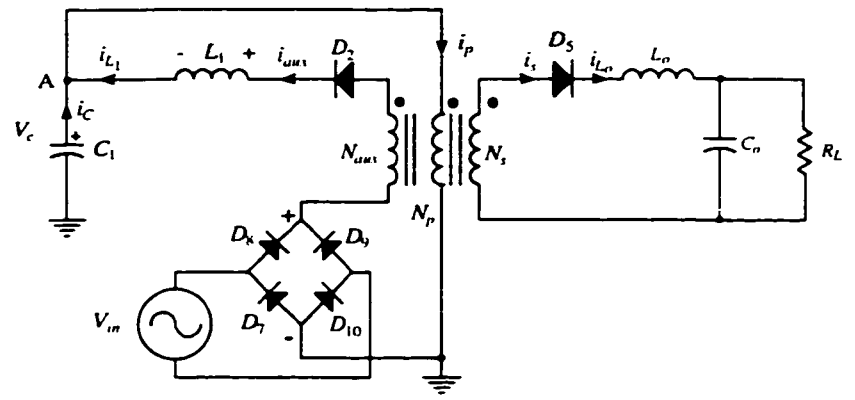
The operational waveforms of the converter with a transformer turns ratio of $N_p : N_{aux} : N_s$ = 1: 1 : 1 under the above assumptions are shown in Fig. 4.2.

Interval 1, ($t_0 < t < t_1$)

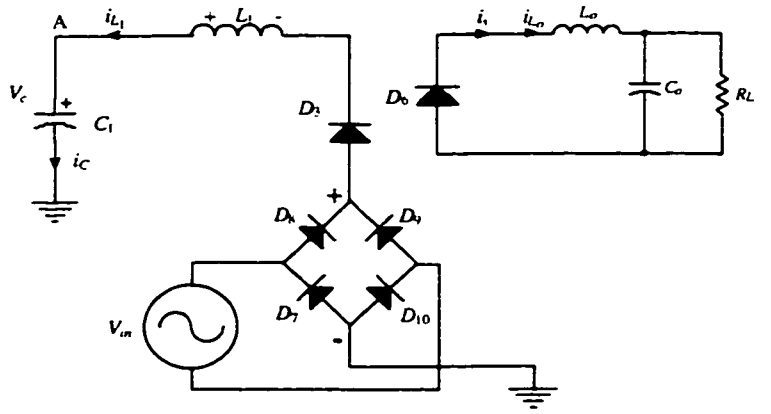
During this interval, switches S_1 and S_2 are on. Power is transferred from capacitor C_1 to the main dc output via the transformer. Power is also circulated from the ac mains into the loop formed by either diodes D_8 or D_9, the auxiliary winding, the diode D_2, the inductor L_1 , primary winding and either of the diodes D_7 or D_{10}. Fig. 4.3(a) shows the equivalent circuit during this mode of operation. As the turns ratio from primary to auxiliary winding is unity, a voltage of approximately ($V_m \cdot \sin \omega t$) is applied across inductor L_1, causing the inductor current to rise linearly as shown in Fig. 4.2. The current through the switches is the sum of the currents in L_1 and L_o. The steady state analysis of interval 1 of Chapter 2 is also valid here where it was shown mathematically that the current drawn from the capacitor was sent to the load when the switch was on.

The output inductor current i_{L_o} rises linearly with a rate determined by (4.1), during this interval as shown in Fig. 4.2.

$$\frac{di_{L_o}}{dt} = \frac{(V_c - V_o)}{L_o} \tag{4.1}$$



a)



b)

Fig. 4.3 Equivalent circuits of the converter of 4.1 during various operating intervals (a) Interval 1, (b) Interval 2,

Interval 2, ($t_1 < t < t_3$)

Interval 2 begins when switches S_1 and S_2 are turned off. The current that was flowing through the inductor L_1 at the end of interval 1, forces diode D_3 to conduct. This current circulates through capacitor C_1 and input source V_{in} until it becomes zero. The equivalent circuit during this interval is shown in Fig. 4.3(b).

During interval k, t_x varies between t_1 and t_4 as it is being modulated by the rectified input line voltage. At the peak of the rectified input voltage, the duration of t_x is at it's maximum. The same design criteria for L_1 of Chapter 2 is applied such that the value of L_1 is chosen so that the current i_{L_1} decays to zero before the next switching period begins.

The output inductor current decays with a rate determined by

$$\frac{di_{L_o}}{dt} = \frac{V_o}{L_o} \tag{4.2}$$

shown in Fig. 4.2. The duration of the free-wheeling period is defined as t_y. If the output load is constant, then t_y does not change during interval k. The duration of t_y varies between t_1 and t_4, depending on the value of output current. With a proper value of L_o, the current i_{L_o} decays to zero before the next switching period begins.

Interval 3($t_3 < t < t_4$)

At the end of interval 2, all the energy stored in L_1 has been transferred to capacitor C_1 and all the energy stored in the output inductor L_o has been transferred to the load during this interval. The output capacitor supplies the output load while the transformer resets.

4.5 PERFORMANCE CHARACTERISTICS

This section presents the characteristics and performance of the proposed converter. The turns ratio of the transformer between primary, auxiliary and secondary is N_p: N_{aux}: N_s = 1 : 1 : 1.

4.5.1 Effect of Transformer Turns Ratio on the Input Power Factor

This effect is the same as section 2.5.1 of Chapter 2

4.5.2 Dc Bulk Capacitor Current and Voltage

The proposed converter eliminates the large bulk voltage variations seen with the converters of Chapter 2 and 3.

The capacitor voltage V_c can be found by summing the currents that charge the capacitor during interval 2 and subtracting the currents leaving the capacitor during interval 1 for n intervals. This is expressed by

$$\left[\sum_{k=0}^{n}\int_0^{tx_k}\left(\frac{V_c - V_{in_k}}{L_1}\right)\cdot t\cdot dt\right]-\left[n\cdot\int_0^{t_{on}}\left(\frac{V_c - V_o}{L_o}\right)\cdot t\cdot dt\right]=0 \qquad (4.3)$$

Note that L_1 and L_o determine the currents to and from the capacitor, and these determines the capacitor voltage. Therefore, the ratio between L_1 and L_o determines the capacitor voltage. This effect was also reported in [18] and [19].

Expanding (4.3) results in

$$\left[\sum_{k=0}^{n}\frac{1}{2}\cdot {V_{in_k}}^2\cdot\frac{{t_{on}}^2}{L_1}\cdot\frac{1}{(V_c - V_{in_k})}\right]-\left[\frac{1}{2}\cdot n\cdot {t_{on}}^2\cdot\frac{(V_c - V_o)}{L_o}\right]=0 \qquad (4.4)$$

The output voltage of the converter in the discontinuos mode is given by [21]

$$V_o = \frac{2 \cdot V_c \cdot t_{on}}{t_{on} + \sqrt{t_{on}^2 + \frac{8 \cdot L_o \cdot T_{sw}}{R_L}}} \tag{4.5}$$

V_c and t_{on} can be obtained by solving equations (4) and (5) using mathematical software such as MathCad.

The capacitor voltage V_c is a function of input voltage and the value of inductors L_1 and L_o. Fig. 4.4 shows the theoretical capacitor voltage V_c as a function of output load. The curves show that by operating both the auxiliary and output circuits in discontinuous current mode, the capacitor voltage is constant from no load to full load.

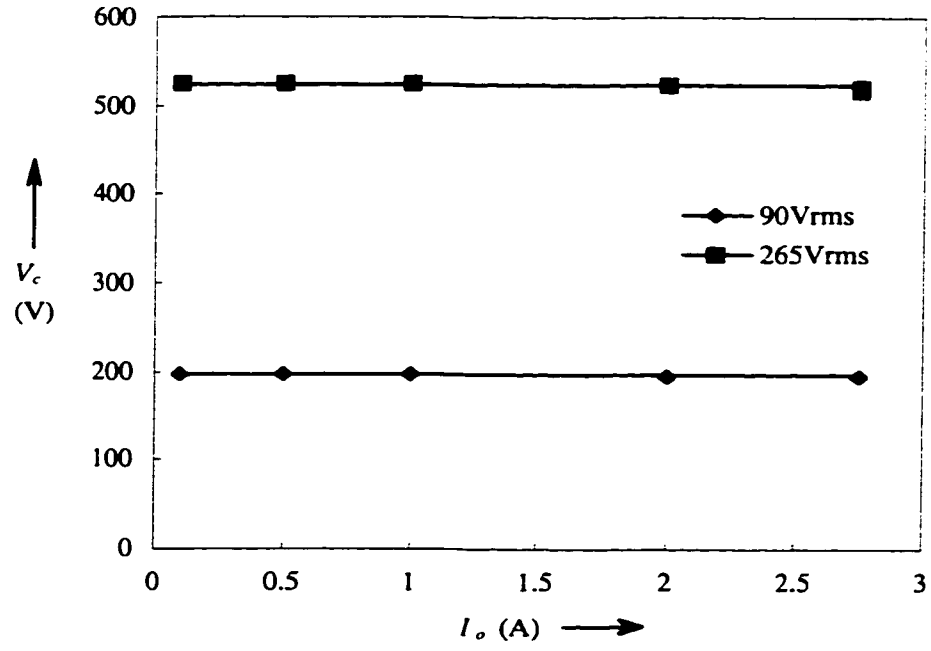


Fig. 4.4 Theoretical capacitor voltage versus output current. ($L_1/L_o = 1$).

Fig. 4.5 shows the theoretical capacitor voltage versus the input line voltage for different ratios of L_1 and L_o.

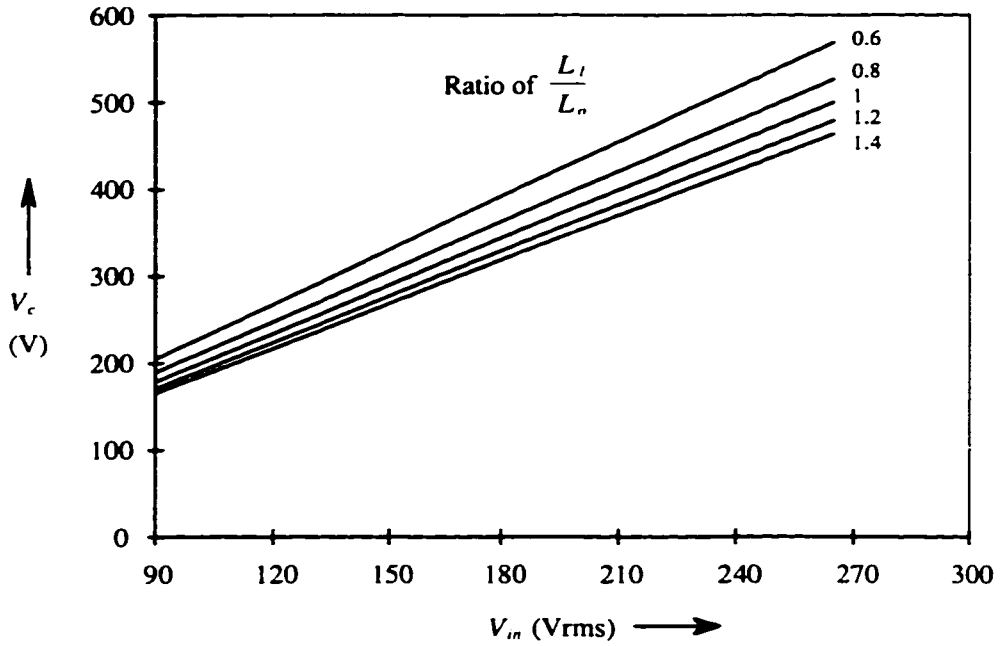


Fig. 4.5 Theoretical capacitor voltage versus input line voltage for different ratios of L_1 and L_o (L_o = 130 μH).

The average current per switching interval i_{cavg_k} is defined by

$$i_{cavgk} = \frac{\left(\frac{1}{2}\cdot t_{x_k}\cdot i_{L1\,peak_k}\right) - \left(\frac{1}{2}\cdot t_{on}{}^2\cdot\frac{(V_c - V_o)}{L_o}\right)}{T_{sw}} \tag{4.6}$$

If the bulk capacitor value is assumed to be 390uF, the voltage ripple of the capacitor v_c with an input voltage of 120V at full rated output power is illustrated in Fig. 4.6.

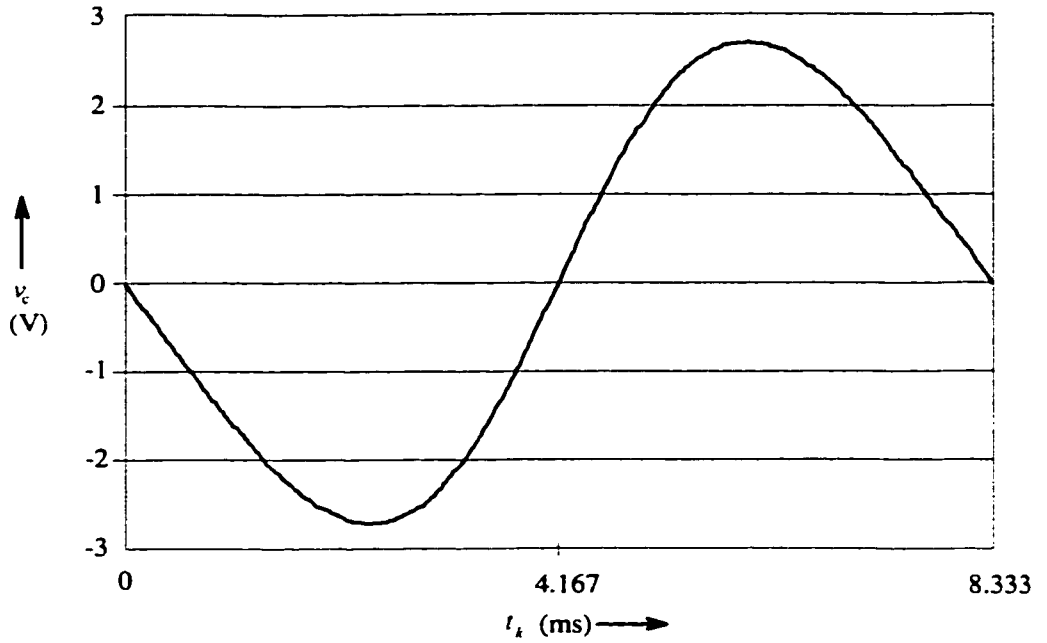


Fig. 4.6 Ripple voltage of bulk capacitor.

The RMS current of C_1 is given by

$$I_{C1\,rms} = \sqrt{\frac{1}{3 \cdot T_{ac}} \left[\sum_{k=0}^{n} \left[\frac{(V_c - V_o)}{L_o} \cdot t_{on} \right]^2 \cdot t_{on} + \left(i_{L1\,peak_k} \right)^2 \cdot t_{x_k} \right]} \tag{4.7}$$

4.5.3 Auxiliary Inductor Current

The analysis of the auxiliary inductor current is the same as section 2.5.3 of Chapter 2. The RMS current through L_1 is given by

$$I_{L1\,rms} = \sqrt{\frac{1}{3 \cdot T_{ac}} \left[\sum_{k=0}^{n} \left(i_{L1\,peak_k} \right)^2 \cdot t_{on} + \left(i_{L1\,peak_k} \right)^2 \cdot t_{x_k} \right]} \tag{4.8}$$

4.5.3.1 Effects on the value of the Auxiliary Inductor

By decreasing the value of the auxiliary inductor, the peak current in it is increased. The bulk voltage is thus increased.

By increasing the value of the auxiliary inductor, the peak current in it is decreased. The bulk voltage is thus decreased.

The effects on the bulk voltage by the different values of auxiliary inductor is shown in Fig. 4.5.

4.5.3.2 Boundary of Continuous and Discontinuous current in the Auxiliary Inductor

The same criteria for the minimum differential voltage required to maintain the current in L_1 discontinuous is applied in this converter as in the one in Chapter 2. The differential and capacitor voltage at the boundary are also given by equations (2.33) and (2.34). The duty cycle at the boundary can be determined by equations (2.34) and (4.5).

4.5.4 Input Current, Harmonic Content and power factor

The input current will have the same waveshape as with the converters of Chapter 2 and 3 and can be found using equation (2.37). The input RMS current is also found by equation (2.38).

Fig. 4.7 shows the theoretical filtered input current at two different input voltages. The waveforms are not sinusoidal and contain large 3rd harmonics. The large third harmonic is caused by the modulation of the inductor current i_{L_1} during interval 2. An analysis of this effect was reported in [22].

Fig. 4.8 shows the theoretical peak input current 3rd and 5th harmonic components for different load and supply conditions. The peak 3rd and 5th harmonics are within the IEC-1000-3-2 Class A and D requirements. The limits for the 3rd and 5th harmonics for a 150 W converter operating from a 120 V input are 0.98 A peak and 0.55 A peak respectively. The 3rd harmonic is the major contributor to the total harmonic distortion. THD and power factor are also found by equation (2.39) and (2.40).

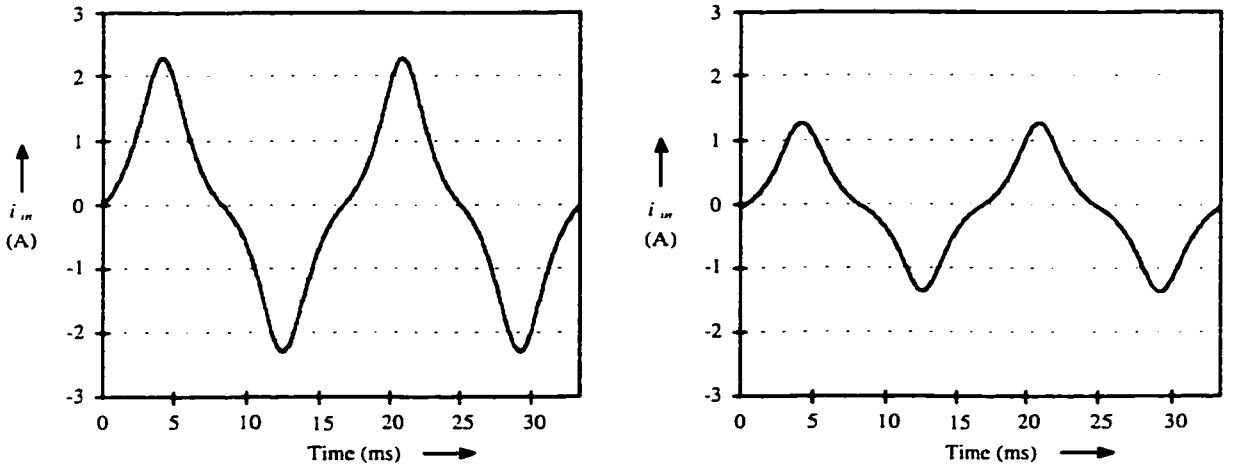


Fig. 4.7 Theoretical filtered input current (Po=150W).
(a) V_{in} = 120 V. (b) V_{in} = 220 V.

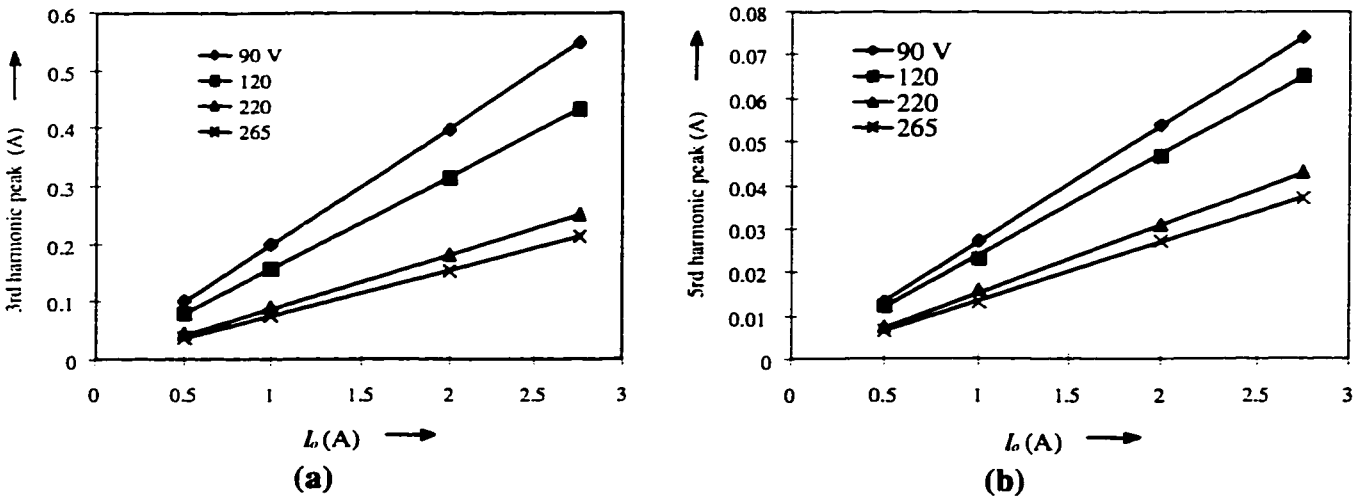


Fig. 4.8 Theoretical peak input current harmonic spectrum for different load and supply conditions.
(a) 3rd harmonic. (b) 5th harmonic.

4.5.5 Current and Voltage Ratings of the MOSFET Switch

The MOSFET switches during interval 1 carry the sums of the auxiliary inductor current and the output inductor current as shown in Fig. 4.2. The RMS current for S_1 and S_2 is determined by

$$I_{swrms} = \sqrt{\frac{1}{3 \cdot T_{ac}} \left[\sum_{k=0}^{n} \left[\frac{(V_c - V_o)}{L_o} \cdot t_{on} + \frac{(V_{in_k})}{L_1} \cdot t_{on} \right]^2 \cdot t_{on} \right]} \tag{4.9}$$

The conduction losses for each MOSFET can be calculated by equations (4.9) and (2.42) while the charging and discharging of the body drain-source capacitance will be dissipated in the switches and can be calculated by

$$P_{cv} = \frac{1}{2} \cdot C_{oss} \cdot V_c^2 \cdot f \tag{4.10}$$

Turn on losses are negligable as the switches turn on with zero current.

The turn off losses is determined by

$$P_{swoff} = \left[\sum_{k=0}^{n} \frac{1}{2} \cdot \left[i_{Lipeak_k} + \left(\frac{V_c - V_o}{Lo} \right) \cdot t_{on} \right] \cdot V_c \cdot t_{fall} \right] \cdot \frac{1}{T_{ac}} \tag{4.11}$$

where t_{fall} is the time required for the current in the switch to decay to zero. The power losses in the switches consist mainly of turn-off losses.

4.5.6 Output Filter Characteristics

The key performance of the converter relies on the ratio between L_1 and L_o. Thus, the design of L_o is crucial to the operation of the converter. The value L_o is designed so that the ripple current is twice the rated full load output current. The output inductor current is at the boundary of continuous current mode during rated full load. As the load is decreased, the inductor current enters discontinuous current mode. The converter regulates the output voltage by decreasing the duty cycle as shown in equation (4.5). The large ripple current in L_o produces a large flux swing in the core. In effect, the ac core losses are high compared to those of Chapter 2 and 3 as the output peak to peak ripple current is only twenty percent of the rated output current.

The output capacitors must be able to handle the high ripple currents. Therefore, lower ESR capacitors must be chosen as this will also affect the ripple voltage at the output of the converter.

The peak output inductor load current can be found by

$$I_{Lopeak} = \left(\frac{V_c - V_o}{L_o} \right) \cdot t_{on} \tag{4.12}$$

The RMS current of L_o is determined by

$$I_{Lorms} = \sqrt{\frac{1}{3 \cdot T_{sw}} \cdot \left[(i_{Lopeak})^2 \cdot t_{on} + (i_{Lopeak})^2 \cdot t_y \right]} \tag{4.13}$$

where t_y is determined from equation (4.1) and is given by

$$t_y = i_{Lopeak} \cdot \frac{L_o}{V_o} \tag{4.14}$$

4.5.7 Experimental Results

A 150 W, 90-265 Vac to 54.75 Vdc prototype converter has been built in the laboratory to validate the theoretical results. The operating frequency of the converter is 50 kHz. Table 1 gives the values of the components used in the prototype.

TABLE I

COMPONENT VALUES FOR THE EXPERIMENTAL PROTOTYPE (FIG. 1)

Component	Value	Manufacturer
L_1	130μH	Magnetics (MPP55254)
L_o	130μH	Magnetics (MPP55254)
C_1	50 μF / 800 V	Nipon Chemi-Con
PWM	UCC3804	Unitrode
S_1, S_2	IRFPC60	IR
D_5, D_6	MUR860	Motorola
D_1, D_4, D_{11}	MUR1100E	Motorola
D_2-D_3, D_7-D_{10}	MUR480	Motorola
C_{s1}, C_{s2}	1 μF / 400 Vdc	Sprague
L_{s1}	-	-
C_o	2000 μF / 63 Vdc	United Chemi-Con

Fig. 4.9 shows the efficiency versus the output current for different nominal input voltages. The universal input range converter has a L_1 / L_o ratio of one and operates with an input voltage from 90 V to 265 V. The high voltage range or European type converter has a L_1 / L_o ratio of 2 and operates with an input voltage from 170 V to 265 V. Fig. 4.9 also shows that the converter has a rated efficiency of about 85% and 80% for European and universal input voltage ranges, respectively.

Fig. 4.10 gives the power factor versus different values of output current for different nominal input voltages. This figure shows that the converter has reasonably high input power factor for universal range (in the range of 0.96) and a moderately high power factor for the European range (in the range of 0.94).

The input current harmonics and the waveforms for the input line current with applied input voltages of 120 V and 220 V are given in Fig. 4.11 and Fig. 4.12, respectively. Both figures show that the magnitude of these harmonics is lower than the permissible values defined by the IEC 1000-3-2 standard.

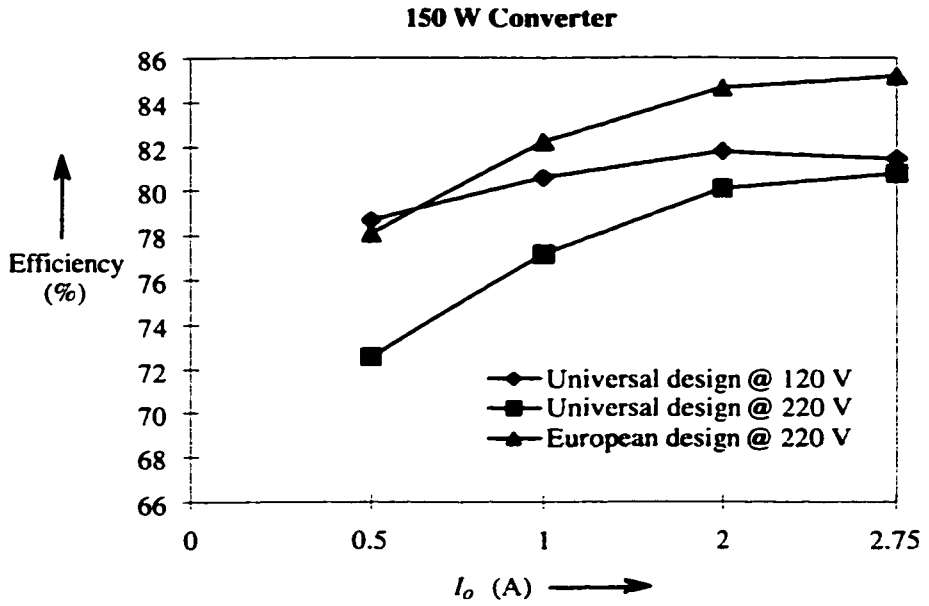


Fig. 4.9 Experimental efficiency versus output current (V_{out} = 54.75 V, f_{sw} = 50 kHz).

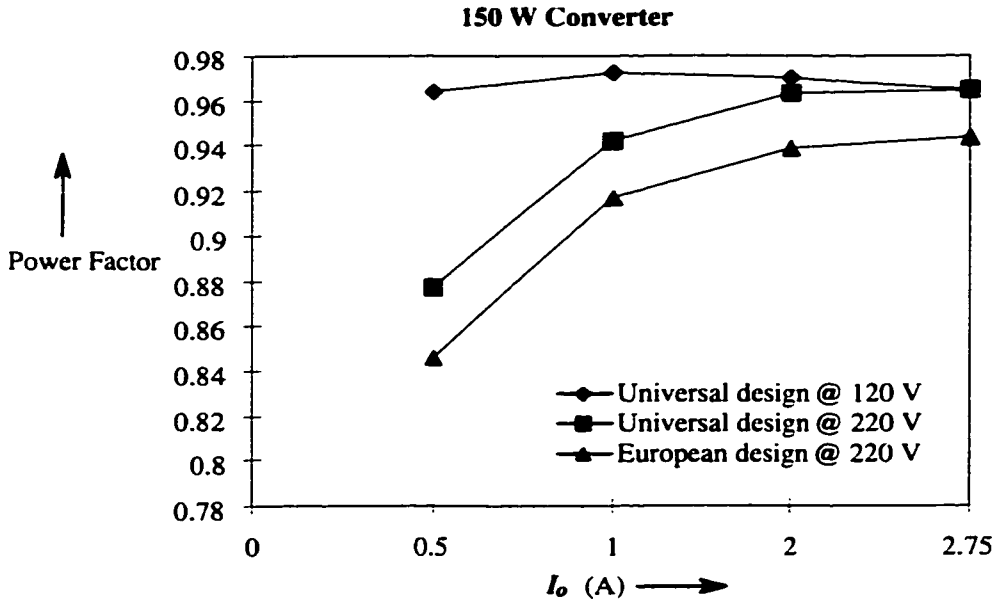


Fig. 4.10 Experimental input power factor versus output current (V_{out} = 54.75 V, f_{sw} = 50 kHz).

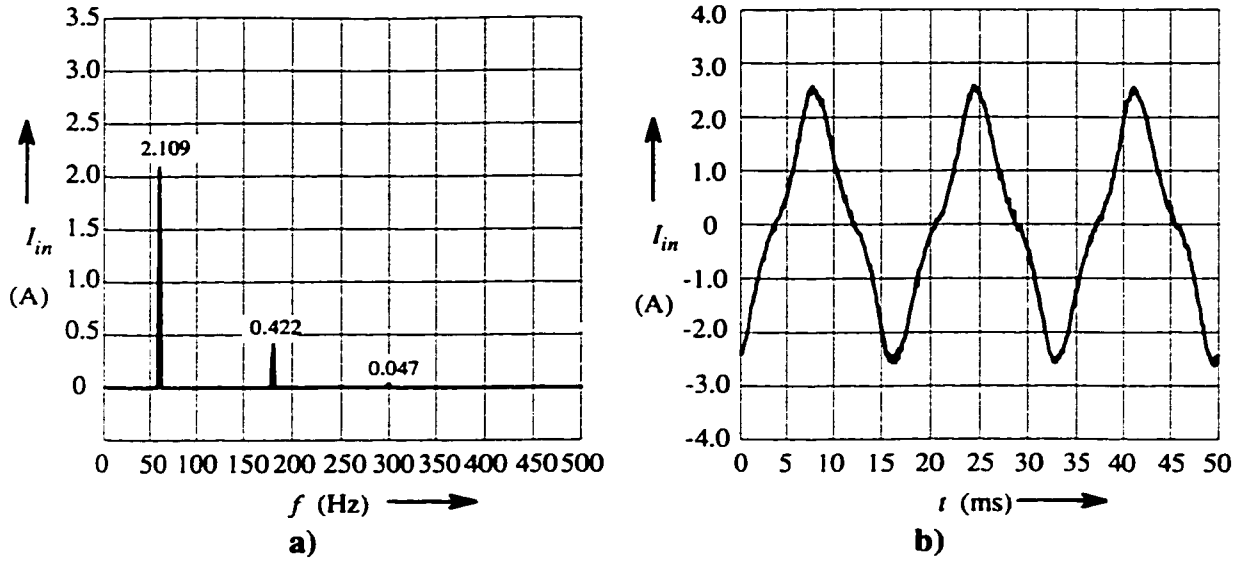


Fig. 4.11 Experimental waveforms at full load (a) Peak line current harmonic spectrum, (b) Line current.
(V_{in}= 120 V, I_o = 2.75 A, V_{out} = 54.75 V, V_{dc}= 252 V, pf = 0.969)
(L_1 = L_o = 130 μH, f_{sw} = 50 kHz).

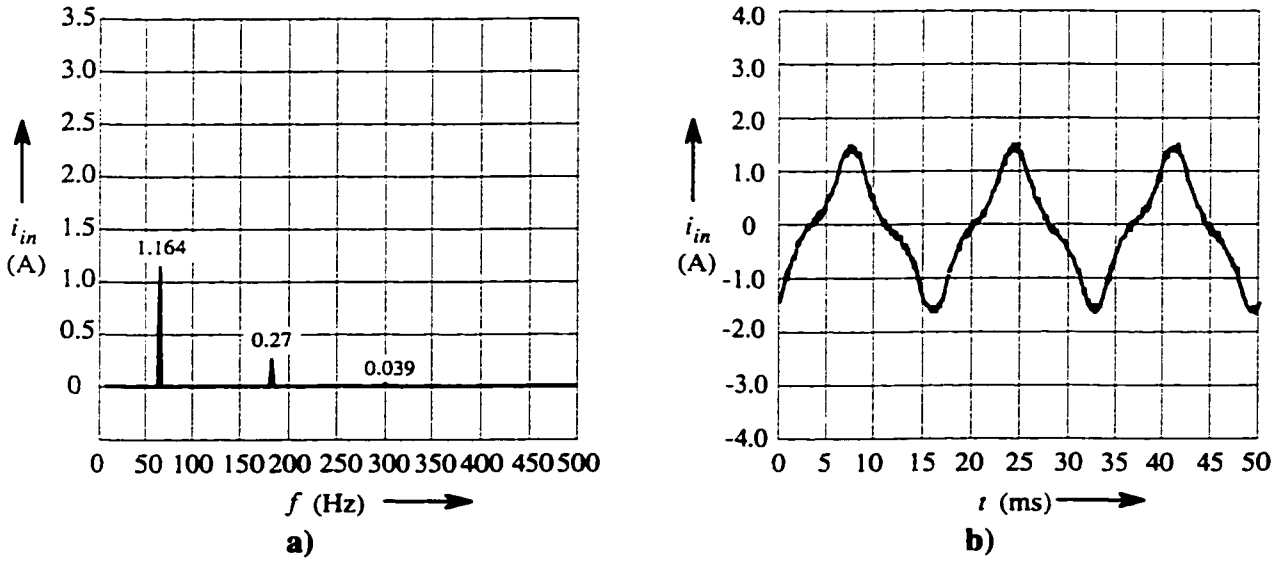


Fig. 4.12 Experimental waveforms at full load. (a) Peak line current harmonic spectrum, b) Line current.
(V_{in}= 220 V , I_o = 2.75 A, V_{out} = 54.75 V, V_{dc}= 444 V, pf = 0.965)
(L_1 = L_o = 130 μH, f_{sw} = 50 kHz)

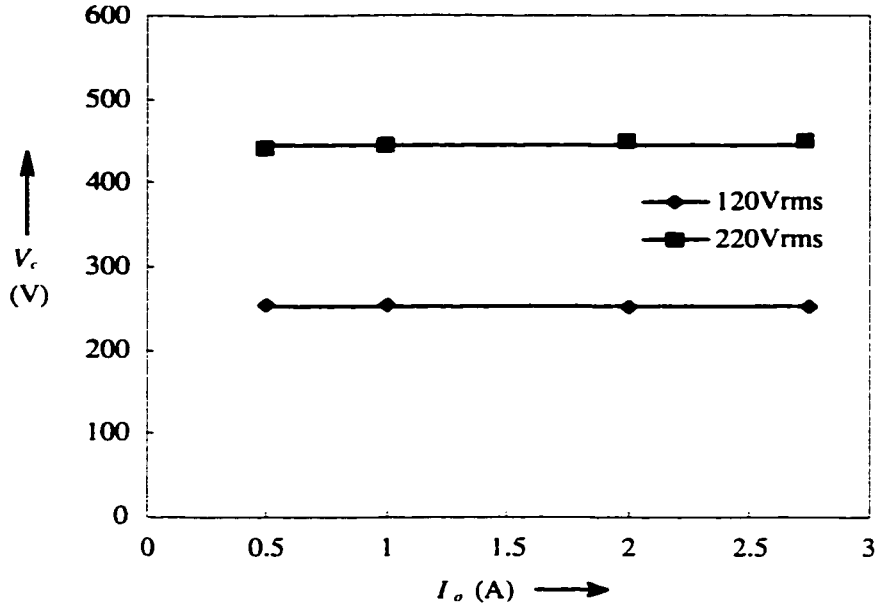


Fig. 4.13 Variation in bulk voltage versus load for two input line voltages.

4.6 DESIGN CONSIDERATIONS

The proper operation of the converter is assured by the appropriate selection of the transformer turns ratio, the auxiliary inductor L_1, the dc bulk capacitor C_1, and the output inductor L_o.

The dc bulk capacitor voltage establishes the performance of the converter as it determines the voltage stress across almost all the components. The value of the capacitor determines the hold-up time of the power supply and the 120 Hz voltage ripple across C_1. The hold-up time should be determined at the minimum input voltage and at the rated output power. The capacitor voltage varies approximately three to one with an input voltage varying from 90 V to 265 V. Therefore, the hold-up time is much longer with an input voltage of 265 V as compared to an input voltage of 90 V.

A compromise must be made between the magnitude of the capacitor voltage V_c and the distortion of the input current. The distorted input current is proportional to the differential voltage between the rectified input peak voltage and V_c. The larger the differential voltage, the less distortion is present in the input current.

It is found that $N_{aux} = N_p$ gives the optimum results in terms of high input power factor and lower voltage stress across the power circuit components. If the turns ratio is less or greater than unity a higher distortion in the input current is present.

The turns ratio between N_p and N_s of the transformer should be selected so that the duty cycle D of the converter is small. Equation (2.34) shows that to obtain a low capacitor voltage the duty cycle should be small.

The value of inductors L_1 and L_o should be selected so that the currents in them are at the boundary of the continuous conduction mode at rated output power with minimum input voltage. The ratio of L_1 / L_o should be made large as it reduces the bulk capacitor voltage. This means that for a universal range (90V-265V) the ratio of L_1 / L_o is different than for the European voltage range (170V-265V).

Operation of the converter at high input voltage range (170 V-265 V) can be achieved by selecting a larger value of L_1 . A higher efficiency is obtained with this voltage range since lower values of current and voltage are processed by the switches.

For a given ratio of L_1 / L_o , the value of L_o is chosen in such a way that the current through it is at the boundary of continuous and discontinuous mode at the rated current and minimum AC input voltage. Inductor L_o selected in this way will minimize the ac cor losses and ripple current through the output capacitor C_o .

The drain current in the switches at turn-on will ramp up from zero to a level determined by the load current and line voltage. The converter will have zero current switching at turn-on. There will be large losses at turn-off. Therefore, the speed at which the switches turn-off must be fast.

4.7 ADVANTAGES AND LIMITATIONS OF THE PROPOSED AC/DC CONVERTER

The proposed converter topology maintains the advantages of conventional two stage PFC circuits in terms of high input power factor, hold-up time capability and no low frequency ripple in the output voltage. In addition to these advantages, the proposed single stage converter employs fewer components particularly in the control circuit, which results in smaller board area and lower power components and manufacturing costs. However, these benefits come at the expense of increased current stresses in the power circuit components as both the auxiliary and main output inductor currents have to be discontinuous to reduce the voltage stress across the switches. This results in higher switching and conduction losses in the converter and negatively impacts the efficiency. In order to keep these losses low, and taking into account the available switches, the output power rating of the proposed converter is limited (below 200 W).

4.8 CONCLUSIONS

A single stage two-switch isolated AC/DC converter topology with high input power factor, hold-up time capability and no low frequency component in the output voltage has been presented. The steady state behavior has been studied, analyzed and

performance characteristics presented. It has been shown that by operating the converter output in the discontinuous conduction mode, the voltage stress across the components is minimized while operating the converter at constant frequency.

Experimental results show that the converter has high input power factor and good overall efficiency both for the European as well universal input voltage range. The proposed converter is best suited for low to medium power applications with high output voltages.

CHAPTER 5

SUMMARY AND CONCLUSIONS

5.1 SUMMARY

Conventionally, AC to DC converters with power factor correction are implemented using two stages. This thesis presents three low power AC to DC converters with PFC implemented in a single stage.

Three converters were analysed;

i) Singie Switch, fixed frequency, continuous output current forward converter.

ii) Single Switch, variable frequency, continuous output current forward converter.

iii) Two Switch, fixed frequency, discontinuous output current forward converter.

The steady state analysis and operating principals were performed. The results of the analysis used to generate characteristic curves which aid in the understanding of the operation of the converters. Experiment results are used to verify the theoretical analysis.

5.2 CONCLUSIONS

Three new single stage PFC AC/DC converters were presented. All three converters have high input power factor, hold-up time capability and no low frequency component in the output voltage.

However, there are a few disadvantages which compromises the usefulness of the converters of chapter 2 and chapter 3. The most important draw back is the bulk voltage variation which is load dependent. This voltage is to high at light loads which hinders the operation of the converters to operate from a universal input voltage range. Therefor, the operation of the converters are restricted to an input voltage range of 90 V - 135 V.

With the final proposed converter of chapter 4, it was shown that by operating the converter's output in the discontinuous conduction mode, the bulk voltage was not load dependant and the converter's operation includes the universal input voltage range.

5.3 SUGGESTIONS FOR FUTURE WORK

As an extension to the research work presented in this thesis, the following topics are suggested:

i) Implementation of loss-less snubbing for the improvement in efficiency of turn-off losses of the MOSFET.

ii) Analyze the possible feasibility of operating the converter's auxiliary circuit in continuous current mode.

iii) Analyze and compare other topological combinations for possible improvements to the new single switch converter.

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