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A ZERO VOLTAGE SWITCHING BOOST CONVERTER USING A SOFT SWITCHING AUXILIARY CIRCUIT WITH REDUCED CONDUCTION LOSSES

Nikhil Jain

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In
The Department
Of
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ABSTRACT

A ZERO VOLTAGE SWITCHING BOOST CONVERTER USING A SOFT SWITCHING AUXILIARY CIRCUIT WITH REDUCED CONDUCTION LOSSES.

NIKHIL JAIN

Modern AC-DC power supplies utilize power factor correction in order to minimize the harmonics in the input current drawn from the utility. The Boost topology is the most popular topology for power factor correction today but it has some disadvantages like very high EMI due to reverse recovery of the boost diode and high switching losses caused by hard switching of the boost switch.

Many variations of the original boost topology have been suggested to overcome these problems. The Zero Voltage Transition Boost converter is one such solution. In such a converter an auxiliary resonant circuit is employed which is activated only when the boost switch is turning on or off. This auxiliary circuit allows the boost switch to turn on and off under zero voltage conditions thus reducing the switching losses. However the auxiliary circuit might be very complex and conduction losses in it might offset the expected rise in efficiency.

In this thesis a soft-switching boost power converter is proposed and analyzed. This converter reduces the EMI and increases the efficiency because the auxiliary circuit is itself soft-switching and has low conduction losses due to creative placement of the resonant capacitors. Characteristic curves are generated for the proposed converter which not only give valuable insight on the behavior of the converter but also aid in designing the converter. The feasibility of the proposed converter is examined by means of results obtained from an experimental prototype.
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Dedicated to my parents
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<table>
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<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>EMI</td>
<td>electro-magnetic interference</td>
</tr>
<tr>
<td>MOSFET</td>
<td>metal–oxide semiconductor field–effect transistor.</td>
</tr>
<tr>
<td>PFC</td>
<td>power factor correction</td>
</tr>
<tr>
<td>PWM</td>
<td>pulse–width modulation</td>
</tr>
<tr>
<td>QRC</td>
<td>quasi–resonant converter</td>
</tr>
<tr>
<td>rms</td>
<td>root mean square</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>ZCS</td>
<td>zero current switching</td>
</tr>
<tr>
<td>ZVS</td>
<td>zero voltage switching</td>
</tr>
<tr>
<td>ZVT</td>
<td>zero voltage transition</td>
</tr>
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</table>
LIST OF MAIN SYMBOLS

\( C \)  capacitor, capacitance

\( C_o \)  output capacitor

\( C_b \)  reverse charging capacitor of the auxiliary circuit

\( C_p \)  equivalent capacitance when boost switch capacitance is discharging

\( C_r \)  auxiliary circuit resonant capacitor

\( C_s \)  parasitic capacitance of main boost switch

\( C_{pb} \)  equivalent capacitance when auxiliary circuit current reverses

\( D(\omega t) \)  duty cycle as a time varying function

\( D_{min} \)  minimum duty cycle

\( D_{min,1} \)  minimum duty cycle under Mode 1

\( D_{pk} \)  duty cycle when input current is maximum

\( D_1 \)  boost diode

\( D_2 \)  auxiliary circuit series blocking diode

\( D_3 \)  auxiliary capacitor discharge diode

\( D_4 \)  auxiliary circuit series blocking diode

\( D_5 \)  auxiliary circuit anti-parallel diode

\( F_{sw} \)  switching frequency of converter

\( f_r \)  ripple frequency which is 2\(^{nd}\) harmonic of input line frequency

\( I_b \)  base current

\( I_{chg, pk} \)  amplitude of 2\(^{nd}\) harmonic current fed into the output capacitor

\( I_{Di_{avg}} \)  average current flowing through diode i

xv
\( I_{\text{Din,avg}} \) average current flowing through an input diode

\( I_{in} \) Input current

\( I_{in,D} \) Input current through boost inductor when duty cycle is \( D \)

\( I_{in,D_{\text{min}}} \) Input current through boost inductor at minimum duty cycle \( D_{\text{min}} \)

\( I_{\text{in, pk}} \) peak input current

\( I_{Lr} \) current through auxiliary circuit resonant inductor

\( I_{\text{rpk, max}} \) maximum input current with ripple in converter

\( I_{S_i, \text{pk}} \) peak current through switch \( S_i \)

\( I_{S_i, \text{rms}} \) rms current of switch \( S_i \)

\( K \) ratio of capacitor \( C_t \) to \( C_b \)

\( L_{in} \) input inductor

\( L_r \) auxiliary circuit resonant inductor

\( P_o \) output power

\( R_r \) on-state resistance of auxiliary switch

\( S_1 \) main boost switch

\( S_2 \) auxiliary switch

\( t_0 \) instant at which the auxiliary switch is turned on

\( t_0^* \) instant at which the main switch is turned on with ZVS

\( t_2 \) earliest instant at which the main switch can be turned on with ZVS

\( t_3 \) latest instant at which the main switch can be turned on with ZVS

\( t_i \) the \( i^{\text{th}} \) time instant

\( t_{rr} \) boost diode reverse recovery time

\( T_r \) length of the natural resonant cycle of the auxiliary circuit

\( V_b \) base voltage

\( V_{\text{chg, pk}} \) output voltage peak ripple
\[ V_{Ch} \] voltage across reverse charging capacitor

\[ V_{Cr} \] voltage across the resonant capacitor

\[ V_{Ct} \] voltage across the capacitor \( C_t \)

\[ V_{g_{at} Si} \] gating signal of the \( i^{th} \) switch

\[ V_{in} \] input rms voltage

\[ V_{in_{max}} \] maximum rms input voltage

\[ V_{in_{min}} \] minimum rms input voltage

\[ V_{in_{pk}} \] peak input voltage

\[ V_o \] output voltage

\[ V_{S2_{pk}} \] peak voltage across auxiliary switch

\[ Z_t \] auxiliary circuit resistance

\[ Z_{rb} \] base impedance

\[ \Delta I_{pp} \] peak-to-peak input current ripple

\[ \eta \] efficiency

\[ \xi \] damping constant

\[ \omega \] angular frequency in radians

\[ \omega_b \] natural frequency of auxiliary circuit in radians

\[ \omega_{opp} \] natural frequency of auxiliary circuit when current is reversing

\[ \omega_r \] resonant frequency

\[ \omega_{rp} \] resonant frequency of auxiliary circuit when current is reversing

\[ \psi \] phase angle during first operating interval of the switching cycle
CHAPTER 1

INTRODUCTION

1.1 General Introduction

In modern power applications a reliable ac–dc power converter is required. For power applications above 250 W, a two stage process is usually used to provide an isolated and regulated dc output voltage. The first stage of such a converter is a rectifying stage that converts the ac voltage to dc and the second stage is an isolated dc–dc converter that converts the dc input voltage into a regulated dc voltage at the output as shown in Fig. 1.1. One of the most important functions of the rectifying stage is to provide Power Factor Correction (PFC) of the input current in order to minimise the harmonics in it.

Historically diode bridge rectifiers with a large capacitor at the dc bus have been used to convert the ac voltage to a dc voltage. But diode bridge rectifiers draw a very high peak current from the ac utility as shown in Fig. 1.2(b) which is rich in harmonics and thus gives a very poor power factor of about 0.6. International standards such IEC 61000 and IEEE 519–92 lay down the maximum amount of harmonics that can be tolerated in the system and diode bridge rectifiers cannot match these criteria.

Many topologies such as Buck, Boost, Single Stage converters etc. can be used for PFC applications to overcome these problems. These topologies are shown in Fig. 1.3 and their input currents are shown in Fig. 1.4. The filtered input current in most of these topologies resembles Fig. 1.2 (c) closely giving a power factor close to unity.
Fig. 1.1 Conventional Two stage Rectifier

Fig. 1.2 (a) Diode Bridge Rectifier (b) Input current Waveform of Diode Bridge  
(c) Desired input current.
Fig. 1.3 Common Power Factor Correction Topologies (a) Boost topology (b) Buck topology (c) Block Diagram of Single Stage topology.
Fig. 1.4 Input current waveforms for different topologies (a) for Boost topology (b) for Buck topology (c) Unfiltered input current for Single Stage topology operating in Discontinuous Mode.
The most popular among these topologies is the Pulse–Width–Modulated (PWM) boost converter which is used in almost 85% of PFC applications today [1] – [5].

The reasons why boost topology is preferred as a PFC pre-regulator are:

1) The input current in the boost topology has the smallest current ripple as can be seen from Fig. 1.4(a). Thus the filtering requirements for this topology are the lowest resulting in a small filter.

2) Buck pre-regulators require a larger filter at the input since the input current is “chopped up.” They also provide an output voltage that is always lower than the minimum input voltage and this causes problems at zero crossings of the input ac voltage. Although with some modifications buck pre-regulators can give an almost-unity power factor the solutions require a large output inductance for continuous conduction [6] – [7]. This increases the size of the converter as well as cost. For same power level the boost topology gives same Total Harmonic Distortion (THD) with a much smaller inductance.

3) Single-stage converters improve efficiency over two-stage converters by processing power only once to give a regulated dc output voltage which also reduces the cost of the overall control circuit. However they require a larger high voltage dc bus capacitor than the two stage approach which increases cost of converter as the power level increases [8]. Also it is preferable to operate these converters in discontinuous conduction mode to keep the control simple but this increases both the input rms currents resulting in higher conduction losses as well as higher Electro Magnetic Interference (EMI). A large EMI filter has to be provided at input [9] to filter the input current shown in Fig. 1.4(c). Some of the converters rely on variable frequency
control making design of filter complex [10] so the power level of single-stage converters is limited to a maximum power of 150-250 W.

1.2 PWM BOOST CONVERTER FOR PFC APPLICATIONS

The switch mode boost converter can perform power factor correction by shaping the input current to be sinusoidal and forcing it to follow the input voltage waveform. This achieves a power factor close to unity and the harmonics are also reduced. However boost converters suffer from their own set of disadvantages:

1) The output of a boost converter is always greater than the peak input voltage. So if a converter is designed for Universal Input Line Applications (90–265 Volt) the output dc bus voltage must be greater than the peak of the 265 Volt ac wave. Thus the output voltage of the boost must be kept at least 400 V and turning on the main switch of the converter at such a high voltage causes a lot of turn–on losses in the switch.

2) The boost switch has hard turn-on as well as hard turn-off and the boost diode has a hard turn–off and as can be seen from Fig. 1.4(a). This causes additional losses. During the reverse recovery of the boost diode the output capacitor is shorted to ground and this causes a very large and negative current spike to appear in the converter switching waveforms. This current spike causes a large amount of EMI in the circuit and can cause problems in telecommunication systems.

Thus a converter which can minimise these switching losses and reduce the EMI is required. The losses can be substantially reduced by using soft switching techniques
1.3 **Losses in Hard Switching**

The reason why there are switching losses in any switch mode power converter is that when the switching element turns on or off, high voltage and current are present simultaneously in the switch. This leads to very high instantaneous power loss in the switch resulting in a low efficiency of the converter as shown in the following Fig.

![Diagram](image)

**Fig. 1.1.1 Generic Switching Waveforms a) Control Signal b) Switch Current and Voltage, c) Instantaneous Switch power loss.**

As there are \( f_s \) such turn–on and turn–off transitions during each switching cycle then the switching loss in the switch as given in [1] shall be:

\[
P_s = \frac{V_o \cdot I_o \cdot f_s}{2} \cdot (t_{on} + t_{off})
\]  

(1.1)
This equation shows that the switching loss in any semiconductor switch varies linearly with switching frequency $f_s$ and the delay times. Such a switch mode converter is therefore unsuitable for operation at high frequencies above 20 kHz. Although switching stresses can be reduced by using simple dissipative snubbers across the switch the efficiency of the converter is not improved as the switching power loss shifts from the switch to the snubbers.

From equation (1-1) an important result can be deduced that switching losses can be reduced by two methods:

(i) By reducing the turn–on and turn–off delay times. This is done by using faster and more efficient switches in the converter.

(ii) By making the current or voltage across the switch zero before turning it on or off. Soft switching resonant converters are based on this concept.

1.3.1 **Resonant Soft Switching Schemes**

There are two types of resonant soft switching depending on whether the voltage across switch or the current through switch is made zero:

(i) Zero–Current Switching (ZCS): A switch that operates with ZCS has an inductor in series with it and a series blocking diode if the switch is bi-directional. The switch is turned on with ZCS as the series inductor slows down the rate of rise of current after voltage across switch goes to zero. If a negative voltage from a resonant circuit is made to appear across the switch–inductor combination, then the current through switch will naturally reduce to zero and switch is turned off with ZCS as shown in Fig. 1.1 (a).
(ii) Zero-Voltage Switching (ZVS): A switch that operates with ZVS has an anti-parallel diode and a capacitor across it. If negative current is forced to flow through the anti-parallel diode then voltage across switch reduces to zero and then the switch is turned on with ZVS. During turn-off the capacitor across switch reduces the rate of rise of voltage across device as current reduces to zero as in Fig. 1.1 (b).

Fig. 1.1 (a) ZCS turn–off using negative voltage (b) ZVS turn–on using negative current.
ZVS is preferred over ZCS because with ZVS the parasitic switch capacitance dissipates its energy into the load. If there were no ZVS this parasitic capacitance would dissipate as heat in the switch which lowers the efficiency of the system.

There are three main types of resonant converters – 1) Series resonant 2) Parallel resonant and 3) Series-parallel resonant converter. These converters have been discussed in [11] and operate with variable frequency control. They are suitable for the dc-dc converter stage only since it is difficult to implement power factor correction as well as output voltage regulation in the control circuit. Several modifications of the original topologies have been proposed which work under fixed switching frequency but almost all are suitable for use as dc-dc converters only.

For use as ac-dc converter, a new class of resonant converters utilising PWM techniques called Quasi-Resonant Converters (QRC) was developed in [12]–[13]. These converters have ZVS of the main switch but they suffer from parasitic oscillations between the resonant inductor and parasitic capacitance of the rectifying diode. These oscillations affect the stability of the system and damping them results in power loss in the converter. Multi-resonant converters solved this problem by using the various parasitics of the converter as a part of the resonant network [14]-[15]. But they suffer from increased complexity of converter leading to more cost. Also the size of the converters is not reduced much even though the switching frequency can be pushed to as high as 10 MHz.

Another approach to achieve high efficiency in ac-dc converters was to integrate the diode bridge with a resonant boost PFC pre-regulator by using controllable switches in the diode bridge [16]. This resulted in lesser conduction losses in the converter as the input current flowed through two switches only instead of three which was the case when the
diode bridge and boost stage were separate. But these did not result in high efficiency [16] because of hard switching or because the switches had ZCS and not ZVS which is more efficient [17]. The converter in [18] works with slightly higher efficiency but with variable frequency operation. Some of the converters were very complex [19] – [20] which have isolated sensing of voltage and current which makes converter expensive as well. The converter in [21] has many sub-circuit modes which makes converter design difficult.

1.3.2 **ZERO VOLTAGE TRANSITION CONVERTERS**

Zero Voltage Transition (ZVT) converters were proposed in [22] and [23]. In ZVT converters there is an auxiliary resonant circuit across the main switch. The auxiliary circuit is activated only during the main switch transitions and so it is on for only a small time during the switching cycle. Therefore resonance occurs only during the switch transitions. This limits the auxiliary circuit losses. As the resonant inductor slows down the rate of fall of current through the boost diode, the EMI of the ZVT boost converter is also low.

Although highest efficiency of the rectifier is achieved using the ZVT boost converter, some common disadvantages of this class of converter are:

1) The circuit suffers from high stress in across the auxiliary switch as in [22] – [26].

2) The converter in [27] suffers from higher conduction loss due to high rms currents in auxiliary circuit and the boost diode.

3) The converter in [28] suffers from parasitic resonance between the resonant inductor and parasitic capacitance of the auxiliary switch. The saturable inductor limits the switching frequency also.
4) Control of the converter in [29] is very complex.

5) The converter in [30] cannot be used for PFC applications as optimum design for ac input is difficult.

The converter proposed in [31] and [32] overcomes all the above problems at the cost of slightly greater voltage stress across the auxiliary switch. However it makes use of an auxiliary transformer to feed-forward some of the energy of the auxiliary circuit to the output. The design of this transformer is difficult as the leakage inductance of this transformer causes severe oscillations in the current through the main switch. Also there are conduction losses in the auxiliary circuit which limit the rise in efficiency. So it is desirable to have a feed-forward mechanism in the auxiliary circuit without using this transformer.

1.4 Thesis Objectives

This thesis presents a ZVT converter with a soft switching auxiliary circuit which has reduced conduction losses, for PFC applications. The main objectives of the thesis are to:

(i) Analyse the steady-state operation of the proposed converter under the worst case condition that is defined as the peak of the input ac voltage wave when input current is maximum and the ZVS interval is the least.

(ii) Present design characteristics of the converter based on the steady state analysis, which help in understanding the internal working of the converter.

(iii) Present the control scheme used to achieve power factor correction.

(iv) Specify the design guidelines with a design example to assist in the design process.
(v) Verify with results from an experimental prototype the design procedure and feasibility of the proposed converter.

1.5 Thesis Outline

The contents of the thesis are as follows:

In Chapter 2 the proposed ZVT converter is described and its operation explained. The steady state analysis is performed during a single switching cycle of the main switch. Analytical results are given at the end of the chapter.

In Chapter 3 characteristic curves of the converter are obtained based on the steady state analysis of Chapter 2. These curves help provide insights into the working of the converter.

In Chapter 4 control of the proposed converter for PFC applications is described.

In Chapter 5 a design example is given which makes use of the design curves of Chapter 3. Experimental results from a laboratory prototype are given which verify the design procedure and the usefulness of the topology.

In Chapter 6, a summary of the thesis is given. Conclusions and contributions of this thesis are discussed. Suggestions for future work in this area are also suggested.
CHAPTER 2
A ZERO VOLTAGE SWITCHING BOOST
CONVERTER USING A SOFT SWITCHING
AUXILIARY CIRCUIT

2.1 INTRODUCTION

In examining previous ZVT converters it is found that many [22]-[25] do not offer
a lossless turn–on and turn–off of the auxiliary switch which results in lower efficiency in
the converter. These converters also have to incorporate a capacitor as a snubber across
the main switch in order to achieve its zero voltage turn–off. The addition of this
capacitor results in higher rms current in the auxiliary switch that results in more
conduction losses in the auxiliary circuit. Also it is seen from [31] that adding this
capacitor also results in lesser ZVS turn–on interval of the main switch if other
parameters in the auxiliary circuit are kept the same. All these points indicate that it is
desirable to keep the value of this capacitor the least possible. As the switch always has
some parasitic capacitance associated with it so this capacitance is the minimum which a
converter should have across the main switch.

This chapter presents a new topology which overcomes the above mentioned
drawbacks. Steady state analysis of the proposed converter during a switching cycle is
presented from which design curves are obtained in Chapter 3 which are then used in
Chapter 5 in designing the ZVT converter. Experimental results obtained from a
prototype are shown and finally the main points of this chapter are summarised.
The outline of this chapter is as follows:

Section 2.2 gives a short functional description of the proposed converter.

The converter’s features are presented in Section 2.3.

The steady state analysis of the ZVT converter is presented in Section 2.4.

Section 2.5 presents analytical waveforms obtained from the steady-state analysis.

Section 2.6 summarises the key points of this chapter.

2.2 **FUNCTIONAL DESCRIPTION**

Fig. 2.1 shows the ZVT converter that is being presented and analysed in this thesis. The circuit can be assumed to be made up of two parts:

1. The main power circuit consisting of a diode bridge, main boost switch $S_1$, boost inductor $L_{in}$, the boost diode $D_1$, and the output capacitor $C_o$.

2. The auxiliary circuit consisting of the resonant inductor $L_r$, resonant capacitor $C_r$ and another capacitor $C_b$, auxiliary switch $S_2$ and diodes $D_2, D_3, D_4$ and $D_5$.

The output load is represented by an output resistance $R_{load}$. The diode bridge rectifies the variable input AC source voltage at 60 Hz into an uncontrolled DC voltage. The boost inductor $L_{in}$, main switch $S_1$ and boost diode $D_1$ form a simple boost converter which converts the uncontrolled DC into a controlled DC bus voltage at the output capacitor $C_o$. Capacitor $C_o$ filters the second harmonic current and prevents its appearing at the load. Switch $S_2$ is turned on just before $S_1$ and serves to achieve a zero current turn–off of the diode $D_1$ and also discharges the parasitic capacitance across $S_1$ to ensure ZVS of $S_1$. Auxiliary circuit resonant components $C_r$ and $L_r$ make possible the ZCS turn–on
and ZVS turn–off in $S_2$.

Diode $D_2$ is placed in series with $S_2$ to prevent conduction of the body diode of the auxiliary switch which is a slow recovery diode. This will also prevent the parasitic capacitance of $S_2$ from resonating with $L_r$. Diode $D_5$ is a fast recovery diode which is placed across $S_2$ and allows current to flow in direction opposite to switch $S_2$ current.

Diode $D_4$ forces this reverse current to flow through capacitor $C_b$ which will store a part of the energy from the resonant capacitor $C_r$ and will acquire a negative voltage. If capacitor $C_b$ was not present then all the energy from the resonant circuit would have been dissipated in the main switch as conduction losses. But $C_b$ is able to store some of this energy which is sent to the output load at the end of the switching cycle.

When the switch $S_f$ is turned off it will do so with ZVS because the net voltage across $S_f$ will not be the output voltage $V_o$ but voltage $V_o$ minus voltage across $C_b$. The
resonant peak current through the main switch is also reduced because capacitor $C_b$ is able to store some of the energy of the resonant circuit which would have otherwise been wasted as conduction losses. Diode $D_f$ is prevented from turning on by the negative voltage across $C_b$ and so the current first discharges $C_b$ into the load through diode $D_f$ and only then does $D_f$ conduct.

The brief description of the converter's principle of operation is:

The auxiliary switch $S_2$ is turned on before $S_f$. $L_r$ limits the rate at which current falls from diode $D_f$ to $S_2$. When $D_f$ is turned off then the parasitic capacitance of $S_f$ begins to discharge into the auxiliary circuit. The voltage across $S_f$ begins to fall as it is no longer clamped to output voltage $V_o$. Switch $S_f$ is turned on with ZVS when voltage across it goes to zero. Sometime after this turn–on the resonant current in auxiliary circuit reverses direction and current begins to flow through $S_f$. Diode $D_5$ begins conduction and as voltage across $S_2$ goes to zero it is turned off with ZVS. Capacitor $C_b$ is charged by this resonant current and is latched to a particular voltage after the auxiliary circuit stops conduction. When $S_f$ turns off then the full output voltage $V_o$ does not appear across it as diode $D_f$ cannot conduct and so it turns off with ZVS. When capacitor $C_b$ discharges its energy into the load through diode $D_3$, then circuit is reset for the next switching cycle and behaves as a conventional boost converter.
2.3 Converter Features

The main feature of this converter is the simple auxiliary circuit containing few components. A floating gate drive for the auxiliary switch \( S_2 \) is not required as it is connected to ground.

The auxiliary switch \( S_2 \) has a soft turn-off in this converter which is a feature not found in many ZVT converter topologies. This soft turn-off is important as without it some of the reduction in switching losses of the main switch is offset by increased switching loss in the auxiliary switch. Most ZVT topologies use a dissipative snubber in the auxiliary circuit to minimise the oscillations caused by resonance between inductor and output capacitance inside the auxiliary switch. However these problems do not arise in the proposed converter as switch \( S_2 \) has a ZVS turn-off because of conduction of anti-parallel diode \( D_3 \). This makes the voltage across the parasitic capacitance of \( S_2 \) zero while it is being turned off and so these oscillations are reduced to a minimum.

Another feature in the converter is that feed-forward of part of the auxiliary resonant circuit energy is made possible by using only a single capacitor \( C_b \). In [31] and [32] the same feature is implemented by using a transformer in the auxiliary circuit. The leakage inductance of this transformer causes ringing in the auxiliary circuit current and selection of the turns-ratio of this transformer is also difficult.

Another feature is the ZVS turn-off in the main switch \( S_I \) without using an external capacitor across it. This is because during turn-off the whole output voltage does not appear across \( S_I \). The voltage across \( C_b \) prevents \( D_I \) from conducting and the voltage that appears across \( S_I \) is the difference of the output voltage and voltage across \( C_b \).
2.4 **Steady State Analysis**

This section describes the steady state analysis of the auxiliary circuit of the converter during one switching cycle. The purpose of this analysis is to obtain characteristic curves of the converter which aid in designing the converter.

The converter has two modes of operation – Mode 1 occurring at larger duty cycles when current in auxiliary circuit goes to zero before the main switch $S_I$ is turned off and Mode 2 occurring at lower duty cycles when switch $S_I$ turns-off before current in auxiliary circuit has gone to zero. The difference between these two Modes is that in Mode 1 the auxiliary circuit stops conduction before $S_I$ is turned off while in Mode 2, $S_I$ turns-off while the auxiliary circuit is still conducting and this leads to partial charging up of capacitor $C_b$ and more turn-off losses. However Mode 2 occurs at high input voltages only when the input current is low and so conduction losses in this mode will also be low. Later on it will become clear from the design curves of Chapter 3 that converter must be designed in Mode 1 because ZVS interval under it is lesser than under Mode 2.

2.4.1 **Simplifying Assumptions**

The steady state analysis of the auxiliary circuit is carried out using the following assumptions:

1. The input inductor $L_{in}$ is assumed to be large enough to be considered a constant current source, $I_{in}$ during the working of the auxiliary circuit in one switching cycle.

2. Output voltage $V_o$ across the load is constant over one switching cycle of the auxiliary circuit as the output capacitor $C_o$ is large.
3. Diodes $D_1, D_2, D_3, D_4$ and $D_5$ are all assumed to be ideal with no voltage drop or on-state resistance.

4. Auxiliary switch $S_2$ is assumed to have a small on-state resistance $R_s$ of 1 Ohm and zero parasitic capacitance while main switch $S_1$ has a parasitic capacitance $C_s$ and no on state resistance.

5. All inductors and capacitors are ideal with no ESR of capacitors or parasitic resistance of inductors.

2.4.2 Description and Analysis of the Converter Switching Intervals in Mode 1

The proposed converter has eight different operating intervals for a single steady state switching cycle under this Mode. The key waveforms of the converter are shown in Fig. 2.1 and the equivalent circuit for each interval is shown in Fig. 2.2. Mathematical equations which define the converter's behaviour during each of the switching intervals are derived here.

1) Interval 0 [$t < t_o$]

Before time $t = t_o$ the main boost switch $S_1$ is on and conducting the full input current $I_{in}$. The auxiliary circuit is inactive and the converter is behaving as a simple PWM boost converter. The resonant capacitor has a voltage $V_{Cro}$ and the voltage across the auxiliary switch is $V_o - V_{Cro}$.
2) **Interval I** \([t_0 - t_f]\)

At instant to the auxiliary switch \(S_2\) is turned on. The whole output voltage \(V_o\) appears across the auxiliary circuit and current through resonant inductor \(L_r\) begins to rise from zero. This rate of current rise is limited by \(L_r\) and so current is slowly diverted from the boost diode \(D1\). The equations characterising this interval are:

\[
L_r \frac{dI_{Lr}}{dt} = V_o - \frac{1}{C_r} \int_0^t I_{Lr} dt - V_{C_{ro}} - I_{Lr} \cdot R_r
\]  
\hspace{1cm} (2.1)

\[
C_r \cdot \frac{d}{dt} V_{Cr} = I_{Lr}
\]  
\hspace{1cm} (2.2)

Using the initial conditions \(I_{Lr} = 0\), and \(V_{Cr} = V_{C_{ro}}\), eq. (2.1) and (2.2) can be solved to give:

\[
I_{Lr} = \frac{-(V_{C_{ro}} - V_o) \cdot e^{-\xi t} \cdot \sin(\omega_r t)}{\omega_r \cdot L_r}
\]  
\hspace{1cm} (2.3)

\[
V_{Cr} = \frac{\omega_r}{\omega_o} (V_{C_{ro}} - V_o) \cdot e^{-\xi t} \cdot \cos(\omega t - \psi) + V_o
\]  
\hspace{1cm} (2.4)

where

\[
\xi = \frac{R_r}{2 \cdot L_r}
\]  
\hspace{1cm} (2.5)

\[
\omega_o = \frac{1}{\sqrt{L_r \cdot C_r}}
\]  
\hspace{1cm} (2.6)

\[
\omega_r = \sqrt{\omega_o^2 - \xi^2}
\]  
\hspace{1cm} (2.7)
\[ \psi = \tan^{-1}\left(\frac{\xi}{\omega_r}\right) \]  \hspace{1cm} (2.8)

The current flowing in the auxiliary circuit at the end of this interval equals the input current \( I_{in} \) and the resonant capacitor acquires a negative voltage \( V_{Crl} \).
Fig. 2.1 Ideal Auxiliary circuit switching waveforms under Mode 1.
Fig. 2.2 Operating intervals for a single switching cycle of the proposed ZVT converter under Mode 1.
3) **Interval 2 \([t_1 - t_2]\)**

As the whole input current is flowing through auxiliary circuit at instant \(t_1\) there is no current through diode \(D_1\). At this point the parasitic capacitance of switch \(S_1\) begins to discharge into the auxiliary circuit. The auxiliary circuit current \(I_{Lr}\) continues to rise in this interval and will be the sum of the input current and the current through \(C_s\). The equations in this interval are:

\[
L_r \frac{d}{dt} I_{Lr} = -V_{Cr1} - \frac{1}{C_r} \int_0^t I_{Lr} \cdot dt - R_r \cdot I_{Lr} + V_{Cs} \tag{2.9}
\]

\[
C_r \frac{d}{dt} V_{Cr} = I_{Lr} \tag{2.10}
\]

\[
C_s \frac{d}{dt} V_{Cs} = (I_{in} - I_{Lr}) \tag{2.11}
\]

Using the initial conditions \(I_{Lr} = I_{in}\) and \(V_{Cr} = V_{Cr1}\) and \(V_{Cs} = V_0\) the eq. (2.9)-(2.11) can be solved to give:

\[
I_{Lr} = e^{-\xi t} \cdot \left( A \cdot \cos(\omega_{rp} t) + B \cdot \sin(\omega_{rp} t) \right) + I_{in} \cdot \frac{C_p}{C_s} \tag{2.12}
\]

\[
V_{Cs} = e^{-\xi t} \cdot \left( \frac{E}{C_s} \cdot \cos(\omega_{rp} t) + \frac{F}{C_s} \cdot \sin(\omega_{rp} t) \right) + I_{in} \cdot \frac{C_s - C_r}{C_s^2} \cdot t + V_0 - \frac{E}{C_s} \tag{2.13}
\]

\[
V_{Cr} = \left[ e^{-\xi t} \cdot \left( \frac{E}{C_r} \cdot \cos(\omega_{rp} t) + \frac{F}{C_r} \cdot \sin(\omega_{rp} t) \right) \right] + I_{in} \cdot \frac{C_p}{C_r \cdot C_s} \cdot t + V_{Cr1} + \frac{E}{C_r} \tag{2.14}
\]
where

\[ C_p = \frac{C_r \cdot C_s}{C_r + C_s} \]  \hspace{1cm} (2.15)

\[ \omega_{op} = \frac{1}{\sqrt{L_r \cdot C_p}} \]  \hspace{1cm} (2.16)

\[ \omega_{rp} = \sqrt{\omega_{op}^2 - \xi^2} \]  \hspace{1cm} (2.17)

\[ A = I_b \cdot \frac{C_p}{C_r} \]  \hspace{1cm} (2.18)

\[ B = \frac{V_e - V_{CR1} - I_b \cdot R_x + L_x \cdot \xi \cdot A}{\omega_{rp} \cdot L_r} \]  \hspace{1cm} (2.19)

\[ E = \frac{\xi \cdot A + B \cdot \omega_{rp}}{\omega_{op}^2} \]  \hspace{1cm} (2.20)

\[ F = \frac{\xi \cdot B - A \cdot \omega_{rp}}{\omega_{op}^2} \]  \hspace{1cm} (2.21)

This interval ends when the capacitance \( C_s \) has been fully discharged into the auxiliary circuit. At end of this interval the current in the resonant inductor equals \( I_{LR2} \) and the voltage across resonant capacitor becomes \( V_{CR2} \).
4) Interval 3 \([t_2 - t_3]\)

At instant \(t_2\) the capacitance \(C_r\) has been fully discharged and now the current starts flowing through the anti-parallel diode. This is because the current drawn by the resonant inductor \(L_r\) is still greater than the input current \(I_{in}\) and Kirchhoff's current law must be satisfied. The main switch \(S_I\) is turned on with ZVS during this interval as conduction of the body diode make voltage across \(S_I\) zero. The equations in this interval are:

\[
L_r \cdot \frac{d}{dt} I_{Lr} = -V_{Cr2} - \frac{1}{C_r} \int_0^t I_{Lr} \cdot dt - I_{Lr} \cdot R,\quad (2.22)
\]

\[C_r \cdot \frac{d}{dt} V_{Cr} = I_{Lr},\quad (2.23)
\]

Using initial conditions \(I_{Lr} = I_{Lr2}\) and \(V_{Cr} = V_{Cr2}\) eq. (2.22) - (2.23) can be solved to give:

\[
I_{Lr} = e^{-\xi t} \cdot \left( I_{Lr2} \cdot \cos(\omega_r t) - \frac{V_{Cr2} + L_r \cdot \xi \cdot I_{Lr2}}{\omega_r \cdot L_r} \cdot \sin(\omega_r t) \right),\quad (2.24)
\]

\[
V_{Cr} = e^{-\xi t} \cdot \left( V_{Cr2} \cdot \cos(\omega_r t) + \frac{I_{Lr2} + \xi \cdot V_{Cr2} \cdot C_r}{\omega_r \cdot C_r} \cdot \sin(\omega_r t) \right),\quad (2.25)
\]
This interval ends when the current in the auxiliary circuit becomes equal to the input current. The current in the auxiliary circuit becomes $I_{Lr3}$ and the voltage across the resonant capacitor becomes $V_{Cr3}$.

5) Interval 4 [$t_3 - t_4$]

After instant $t_3$ the current in the auxiliary circuit becomes less than the input current. The difference between the input current and auxiliary circuit current will flow into the main switch $S_1$. This interval has the same equations as those for the previous interval except $I_{Lr2}$ is replaced by $I_{Lr3}$ and $V_{Cr2}$ is replaced by $V_{Cr3}$ in eq. (2.24)-(2.25). This interval ends when the current in the auxiliary circuit becomes zero at instant $t_4$. At the end of this interval the voltage across resonant capacitor becomes $V_{Cr4}$ and current $I_{Lr}$ becomes zero.

6) Interval 5 [$t_4 - t_5$]

In this interval the current in the auxiliary circuit reverses and begins the negative portion of the resonant current. Current through the main switch $S_1$ becomes the sum of the sum of the input current and the auxiliary circuit current. The diode $D_2$ in series with auxiliary switch $S_2$ prevents the body diode of $S_2$ from conducting and as a result anti-parallel diode $D_3$ across $S_2$ is forced to conduct. The voltage across $S_2$ goes zero and the auxiliary switch can be turned off with ZVS during this interval. Typically the switch $S_2$ is turned off between time $0.6 \ T_r$ to $0.9 \ T_r$. The current causes capacitor $C_b$ to charge. The equations are:

$$L_r \frac{d}{dt} I_{Lr} = -V_{Cr4} - \frac{1}{C_r} \int_0^t I_{Lr} \cdot dt - \frac{1}{C_b} \int_0^t I_{Lr} \cdot dt$$  \hspace{1cm} (2.26)
\[ C_b \cdot \frac{d}{dt} V_{cb} = I_{lr} \quad (2.27) \]

\[ C_r \cdot \frac{d}{dt} V_{cr} = I_{lr} \quad (2.28) \]

Using initial conditions \( I_{lr} = 0 \) and \( V_{cr} = V_{Cr4} \) eq. (2.26) – (2.28) can be solved to give:

\[ I_{lr} = -(C_{pb} \cdot \omega_{opb} \cdot V_{Cr4} \cdot \sin(\omega_{opb} t)) \quad (2.29) \]

\[ V_{cr} = \frac{C_{pb}}{C_r} \cdot V_{Cr4} \cdot \cos(\omega_{opb} t) + \frac{C_{pb}}{C_b} \cdot V_{Cr4} \quad (2.30) \]

\[ V_{cb} = \frac{C_{pb}}{C_b} \cdot V_{Cr4} \cdot \cos(\omega_{opb} t) - \frac{C_{pb}}{C_b} \cdot V_{Cr4} \quad (2.31) \]

where

\[ C_{pb} = \frac{C_r \cdot C_b}{C_r + C_b} \quad (2.32) \]

\[ \omega_{opb} = \frac{1}{\sqrt{L_r \cdot C_{pb}}} \quad (2.33) \]

This interval ends when the current \( I_{lr} \) goes to zero and the auxiliary circuit becomes inactive for the duration of the switching cycle. The voltage on the resonant capacitor goes back to \( V_{Cr0} \) at the end of this interval and \( C_b \) is charged to \( V_{Cb5} \).
7) Interval 6 \([t_5 - t_6]\)

The converter operates exactly like a standard PWM boost converter during this interval as the auxiliary circuit is not in operation. The input current drawn from the input inductor increases linearly to \(I_{in,D}\) if \(D\) is the duty cycle of the converter. The equations in this interval are:

\[
I_{in,D} = I_m + \frac{V_m}{L_{boost}} \cdot D \cdot T_{sw} \tag{2.34}
\]

This interval lasts until the main switch is turned off at instant \(t_6\).

8) Interval 7 \([t_6 - t_7]\)

When main switch \(S_f\) is turned off at the beginning of this interval the voltage across capacitor \(C_b\) prevents boost diode \(D_f\) from conducting. As a result the voltage that appears across \(S_f\) is the difference of output voltage and voltage across \(C_b\). The internal capacitance of \(S_f\) also limits the rate of rise of voltage across the switch and so \(S_f\) is turned-off with ZVS. The input current \(I_{in,D}\) begins to discharge the capacitor \(C_b\) into the output through the diode \(D_3\). The equations in this interval are:

\[
C_b \cdot \frac{d}{dt} V_{cb} = I_{in,D} \tag{2.35}
\]

The above equation can be solved using the final condition that \(V_{cb} = 0\) at the end of this interval. eq. (2.35) gives:
\[ V_{cb} = \frac{I_{in-D}}{C_b} \cdot t + V_{css} \] (2.36)

This interval lasts until the capacitor \( C_b \) has discharged fully into the output.

9) Interval 8 \([t_7-t_8]\) (same as Interval 0)

As soon as \( C_b \) is discharged it is no longer able to latch diode \( D_I \) which begins to conduct the current. The current continues to flow through diode \( D_I \) until the next switching cycle begins and auxiliary switch \( S_2 \) is turned on again.

2.4.3 Description and Analysis of the Converter Switching Intervals in Mode 2

The auxiliary circuit switching waveforms in Mode 2 are given in Fig. 2.1. The equations (2.1) – (2.25) hold true under this mode also. The difference occurs in the rest of the equations which are:

1) Interval 5 \([t_4-t_5]\):

The equations in this interval are same as (2.26) – (2.33) above. However the interval ends suddenly when \( S_I \) turns-off at minimum duty cycle given by:

\[ D_{\text{min}} = 1 - \frac{\sqrt{2} \cdot V_{I_{\text{max}}}}{V_o} \] (2.37)
Fig. 2.1 Ideal Auxiliary circuit switching waveforms in Mode 2.
Fig. 2.2 Operating intervals for a single switching cycle of the proposed ZVT converter under Mode 2.
By finding out \( D_{\text{min}} \) from above and multiplying it by \( T_{\text{sw}} \) instant \( t_5 \) can be found. Replacing variable \( t \) in (2.29)-(2.31) by \((t_5-t_4)\) the equations can be solved. At the end of this interval the current through \( L_r \) is \( I_{Lrs} \) and voltage across \( C_r \) is \( V_{Cr5} \).

2) **Interval 6 \([t_5 - t_6]\):**

In this interval the remaining resonant current \( I_{Lrs} \) is discharged directly into the output via diode \( D_3 \) without charging up the capacitor \( C_b \) fully. At the same time the partial voltage across \( C_b \) prevents boost diode \( D_7 \) from conducting and the boost inductor current starts discharging \( C_b \) into the output through diode \( D_3 \) only. The equations are:

\[
V_{Cb} = V_{CB5} + \frac{I_{in} \cdot t}{C_b} \tag{2.38}
\]

\[
I_{Lr} = C_r \cdot \omega_o \left[ -(2 \cdot V_{CR5} - V_o) \cdot \sin(\omega_o t) \right] + \frac{I_{Lrs}}{C_r \cdot \omega_o} \cdot \cos(\omega_o t) \tag{2.39}
\]

\[
V_{Cr} = (2 \cdot V_{CR5} - V_o) \cdot \cos(\omega_o t) + \frac{I_{Lrs}}{C_r \cdot \omega_o} \cdot \sin(\omega_o t) - (V_{CR5} - V_o) \tag{2.40}
\]

This interval ends at instant \( t_6 \) when current through \( L_r \) has gone down to zero and voltage across \( C_r \) goes back to \( V_{Cro} \). Note that the value of \( V_{Cro} \) under Mode 2 is different from that under Mode 1 for the same set of parameters. During this interval capacitor \( C_b \) is also discharging into the output and the equation for its discharge is given by
\[ V_{cb} = \frac{I_{in \cdot D_{\min}}}{C_b} \cdot t + V_{cb5} \]  

(2.41)

where

\[ I_{in \cdot D_{\min}} = I_{in} + \frac{V_{in}}{L_{in}} \cdot D_{\min} \cdot T_{sw} \]  

(2.34)

3) **Interval 7 \([t_6 - t_7]\):**

In this interval also \(C_b\) is discharging to the output and the interval lasts until \(t_7\) by which capacitor \(C_b\) has completely discharged and the auxiliary circuit is reset for another switching cycle.

2.5 **ANALYTICAL AND SIMULATED WAVEFORMS OF THE PROPOSED CONVERTER**

The steady state analysis in the previous section can be verified by using selected values of resonant inductance \(L_r\), resonant capacitance \(C_r\), capacitor \(C_b\), variable \(K\) etc. in the program and plotting the waveforms so obtained. Then these waveforms can be checked by simulated waveforms obtained by using the same values of components in a circuit simulator tool such as Psim. These results can also be compared to the ideal waveforms in Fig. 2.1 and Fig. 2.1 to test the accuracy of the mathematical model defined by the equations in the previous section.

The values used to obtain these analytical and simulated waveforms were selected to be in accordance with the design example in Chapter 5. It will be seen later that these analytical waveforms match very closely the experimental waveforms of Chapter 5.
Fig. 2.1 Analytical waveforms of the Auxiliary circuit in Mode 1.
Fig. 2.2 Simulated waveforms of the auxiliary circuit in Mode 1.
Fig. 2.3 Exploded Simulation waveforms of the auxiliary circuit in Mode 1 emphasizing the turn-on and turn-off periods of main switch.
Fig. 2.4 Analytical waveforms of the Auxiliary circuit in Mode 2.
Fig. 2.1 shows the analytical waveforms obtained from the program and Fig. 2.2 shows simulated waveforms from Psim. On comparing the two figs. it is seen that they match to a great extent. The only significant difference is that in the analysis the input current $I_{in}$ from input inductor is assumed to be constant while in the simulated results of Fig. 2.2 this current rises to $I_{in_{\text{actual}}}$ due to boost action.

Fig. 2.3 shows the exploded simulation waveforms which emphasize the turn-on and turn-off conditions in the auxiliary circuit. This fig. is the same as Fig. 2.2 except that it shows more clearly what is happening in the auxiliary circuit. This fig. is seen to match the ideal auxiliary circuit waveforms of Fig. 2.1 except that at turn-off the voltage across the main switch $V_{sl}$ starts not from zero but at a voltage level slightly higher than zero. The reason for this will be made clear in Chapter 3 and Chapter 5.

Fig. 2.4 shows the analytical waveforms for Mode 2 of operation. The values for which this fig. has been drawn is different from those used in the design example of Chapter 5. This is because the values chosen in Chapter 5 allow the converter to work in Mode 1 throughout the input Universal Voltage range. This will be clarified further in Chapter 5.

So it can be deduced that the steady state analysis of this chapter is valid as it has been verified by simulation results.

2.6 Conclusions

The proposed ZVT Boost converter was introduced in this Chapter. This converter has an auxiliary circuit which has low conduction losses and simple construction.
The steady state analysis of this converter was also covered in this chapter. Analytical waveforms were then obtained from the equations and were found to be in good conformance with the ideal waveforms of the auxiliary circuit. This steady state analysis will then be used in Chapter 3 to obtain characteristic curves of this converter which help in the design process.
CHAPTER 3

CHARACTERISTIC CURVES OF THE ZERO VOLTAGE TRANSITION CONVERTER

3.1 INTRODUCTION

In order to properly design the converter, characteristic curves showing the relationship between switch voltages, currents and various auxiliary circuit component values are needed. Using the analytical equations derived in Section 2.4 of Chapter 2 these curves can be drawn both for Mode 1 and for Mode 2. Due to the nature of equations in Section 2.4, the closed form solution of the equations can only be obtained by using an iterative method. So the Newton–Raphson method is implemented using a simple computer program built in Mathcad.

The underlying principle which makes the program work is that for the converter to be in steady state the voltage \( V_{Cr} \) across the resonant capacitor at the beginning of a switching cycle must equal the voltage across it when the switching cycle has ended. This is as a consequence of principle of conservation of energy. If input is a dc source and converter is in steady–state then the energy put into the converter must equal the energy drawn out of converter and the energy dissipated in it assuming auxiliary circuit is in equilibrium. If there is a difference between the two as in transient conditions then the difference must be accounted for by an increase or decrease in the energy stored by the resonant capacitor \( C_r \) until energy balance is reached. Therefore if voltage across \( C_r \) is \( V_{C_{ro}} \) at the beginning of the switching cycle it must remain \( V_{C_{ro}} \) after the switching cycle.
has ended for converter to be in steady-state. This holds true whether the converter operates in Mode 1 or Mode 2.

The outline of this chapter is as follows:

Section 3.2 gives a brief description of the program used in the steady state analysis.

Section 3.3 presents the characteristic curves for Mode 1 and Mode 2 obtained from the steady state analysis of Chapter 2.

The main points of this chapter are summarised and some conclusions made in Section 3.4.

3.2 **Description of Program**

The working of the program in Mode 1 is as follows:

1). An initial value $V_{C_{ro}}$ which is the voltage across the resonant capacitor before the switching cycle begins, is assumed.

2). Step by step the equations derived in Chapter 2 for Mode 1 are solved for each interval using the initial and final operating conditions of each interval.

3). When all the equations have been solved the final value of voltage across $C_r$ is compared with the initial value i.e. $V_{C_{ro}}$. If the difference between these two values is small the circuit is in steady state and values for voltages and currents in the circuit can be extracted. If difference is greater than a specified tolerance then a new value of $V_{C_{ro}}$ is assumed and the process is repeated until the solution converges.

A similar procedure is followed for obtaining the design curves for Mode 2 using the equations for Mode 2.
3.3 Characteristic Curves of the Converter

In this section the characteristic curves of the converter operating in Mode 1 are derived.

3.3.1 Definition of Variables Used in Characteristic Curves

The variables used in drawing the characteristic curves are defined in this section as follows:

1) Base voltage is the constant dc output voltage required from the converter. Thus base voltage is \( V_b = 400 \) V.

2) Base current \( I_b \) is taken as the maximum current that is drawn from the input of the converter just before the auxiliary circuit is activated. For ac input with PFC the maximum current drawn will be at the peak of the ac voltage wave. The maximum current also depends on the rms magnitude of the input voltage. This is because for constant power output the ac input current is inversely proportional to the input ac voltage as given by the equation:

\[
P_o = V_{in} \cdot I_{in} \cdot \cos(\theta)
\]  \hspace{1cm} (3.1)

So the base current is a function of the input voltage and the power level of the converter if the power factor \( \cos(\theta) \) is assumed to be 1. Assuming output power of the converter to be 250 W, the maximum current will occur at minimum value \( V_{in\_\text{min}} \) of input voltage as given by eq. (3.1) and is found out as follows:
Peak input current for minimum input voltage is

$$I_{pk_{\text{max}}} = \frac{\sqrt{2} \cdot \frac{P_o}{\eta}}{V_{in}}$$

$$= \frac{\sqrt{2} \cdot \frac{250}{0.95}}{90} = 4.135 \text{ A} \quad (3.2)$$

Maximum peak-peak ripple current:

$$\Delta I_{pp} = I_{pk_{\text{max}}} \cdot \Delta I = 4.135 \cdot 20\% = 0.827 \text{ A} \quad (3.3)$$

Therefore maximum base current according to definition is:

$$I_b = I_{pk_{\text{max}}} - \frac{\Delta I_{pp}}{2} = 4.135 - \frac{0.827}{2} = 3.722 \text{ A} \quad (3.4)$$

A plot of the variation of base current with input voltage is shown in Fig. 3.1. From this characteristic curve the base current for different values of input voltage can be easily found out.

3) Variable $Z_{rb}$ is defined as the base impedance and is given mathematically by the ratio of the base voltage to the base current:

$$Z_{rb} = \frac{V_b}{I_b} = 107.48 \Omega \quad (3.5)$$
Fig. 3.1 Variation of Base Current as a function of Input Voltage for Output Power 250 Watt.

4) Variable \( Z_r \) is defined as the characteristic impedance of the auxiliary circuit:

\[
Z_r = \sqrt{\frac{L_r}{C_r}}
\]  \hspace{1cm} (3.6)

5) Variable \( T_r \) is defined as the natural resonant cycle of the auxiliary circuit given by:

\[
T_r = 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r}
\]  \hspace{1cm} (3.7)

6) Variable \( K \) is defined as the ratio of capacitor \( C_r \) to capacitor \( C_b \):

\[
K = \frac{C_r}{C_b}
\]  \hspace{1cm} (3.8)
3.3.2 Soft-Switching of the Main Switch in Mode 1

Characteristic curves to determine the boundary of the soft-switching operation are easily drawn using the steady state analysis of Chapter 2. The characteristic curves presented in this section have been drawn using certain selected values of components in the converter. However this component selection does not affect the curves as they are plotted for per unit values and will give the same results for a different set of base values. General conclusions about the performance of the converter can still be made using these curves.

The curves are plotted with respect to resonant impedance \( Z_r \) for various values of \( K \) keeping \( R_r \) is fixed at 1 ohm. The base impedance \( Z_{rb} \) is fixed at its minimum value because this is the case when maximum current \( I_B \) is drawn from the input and the ZVS interval is the least. If the circuit is able to achieve ZVS for this worst case condition then it will have ZVS over all other conditions. From the curves the effect the values of \( L_r \) and \( C_r \) and \( C_b \) have on the vertical axis parameter can be studied. Per unit values are used and actual values can simply be obtained by multiplying the per unit value by the corresponding base value.

\( S_f \) will have a soft turn-on only if it is turned on at some appropriate time instant \( t = t_0 \) after the auxiliary switch \( S_2 \) has been turned on at instant \( t_0 \). The ZVS time interval is bounded between instant \( [t_2 - t_3] \) as shown in Fig. 3.1 because at \( t = t_2 \) the parasitic capacitance \( C_c \) has been fully discharged and after \( t = t_3 \) this capacitance begins charging up again if \( S_f \) has not been turned on by that time.

As the input is an ac source, the ZVS interval length does not remain fixed but changes as the input current changes. For example the ZVS interval at peak of input
current ($\omega t = 90$) is different from the ZVS interval when input current is zero ($\omega t = 0$). There are two possible approaches to ensure ZVS over the whole ac cycle. One is to sense the voltage across the main switch and turn it on when the voltage across it goes to zero. This results in a variable instant $t_0^\ast$ with respect to $t_0$.

![Diagram](image)

Fig. 3.1 ZVS Interval for Soft turn–on of $S_1$.

The other approach is to fix the instant $t_0^\ast$ that is always in the ZVS interval no matter what the input current. The disadvantage of this approach is that this gives a longer than necessary ZVS interval at lighter loads which leads to increasing ZVT circuit conduction losses as shown in [34]. Therefore the preferred approach is to use a voltage sensor across the main switch.
Fig. 3.2 shows the ZVS interval \([t_3-t_2]\) with respect to \(Z_r\) for different values of \(K\). The ZVS interval is plotted with respect to the natural resonant cycle \(T_r\) of the auxiliary circuit and its actual value can be found by reading the appropriate value off the graph and multiplying by \(T_r\). These curves are plotted for minimum value of \(Z_{rb}\) i.e. at maximum value of input current, as at this point the ZVS interval is least.

It is seen from Fig. 3.2 that higher the value of \(Z_r\) lower is the ZVS interval. This is because higher \(Z_r\) implies lower auxiliary circuit current from Ohm’s Law. As this current is responsible for discharging \(C_r\) so if this current is low obviously the ZVS interval will be also low. Similarly lower value of \(K\) means larger value of \(C_b\) which results in higher auxiliary circuit current and higher ZVS interval. For \(K > 1\) the ZVS interval disappears very fast. For example for \(K = 1.5\) ZVS turn-on interval becomes negligible above \(Z_r = 0.55\) pu.

As ratio \(C_r/C_s\) gets smaller it implies \(C_r\) is getting larger which will discharge more energy into capacitor \(C_r\). This means that the discharge current which flows into the auxiliary circuit becomes greater and this means larger ZVS interval as explained above.

The characteristic curves drawn in this section have been generated for those conditions which have a ZVS interval. Some curves terminate abruptly in the graphs because after that point the ZVS interval \(3[t_2-t_3]\) disappears completely and the steady state analysis of Section 2.4 does not apply. For example in Fig. 3.2 for curve \(K = 1\) the ZVS interval disappears for \(Z_r > 0.63\) pu and so for all following graphs drawn in this section, the curve for \(K = 1\) does not extend beyond \(Z_r = 0.63\) pu. After this limit the steady-state analysis of Chapter 2 no longer applies.
Fig. 3.2 ZVS Interval for $R_r = 1 \, \Omega$ and (a) $C_r/C_s = 20$ and (b) $C_r/C_s = 30$. 

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From the graphs we can deduce that the length of ZVS interval depends mainly on the discharge current that flows into the auxiliary circuit. Any factor which results in larger value of this current will also result in larger ZVS interval and vice-versa.

An important point to consider is the effect the value of $K$ has on the polarity of voltage across the resonant capacitor $C_r$ just before the auxiliary circuit is activated. For $K < 1$ the voltage is negative and for $K > 1$ the voltage is positive as shown in Fig. 3.3. For $K = 1$ the voltage across $C_r$ is essentially zero. From Fig. 3.3 it can be seen that negative voltage across $C_r$ results in larger voltage across the resonant inductor $L_r$ when the auxiliary circuit is activated and positive voltage across $C_r$ results in lower voltage across $L_r$. If voltage across $L_r$ is larger then the build-up of auxiliary circuit current will be faster and larger. This gives a larger ZVS interval as explained above. Lesser the value of $K$ from 1, larger will be the negative voltage across $C_r$ and vice-versa. This increase of the ZVS interval with decreasing value of $K$ is verified by Fig. 3.2.

![Figure 3.3](image)

Fig. 3.3 Polarity of Voltage across resonant capacitor $C_r$ for (a) $K < 1$

(b) $K > 1$.  

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3.3.3 Auxiliary Circuit Characteristic Curves when Converter Operates

In Mode 1

Most of the curves drawn here are to aid in the rating of the auxiliary circuit devices. Peak and rms values are used to rate switches while peak and average values are used for selection of the diodes. As the converter is operating in Mode 1 it is assumed that the duty cycle of main switch $S_I$ is large enough to allow the resonant cycle of auxiliary circuit to complete before $S_I$ is turned off.

The method of reading the auxiliary circuit characteristic curves is as follows:

If the value of the resonant inductor $L_r$ is known then by properly selecting $Z_r$ from the design curves the value of the resonant capacitor $C_r$ can be found using eq. (3.7). Then a proper value of variable $K$ is selected from the value of $C_b$ can be found using eq. (3.8).

3.3.3.1 Peak Voltage and Peak Current Graph for the Converter Switches

In Mode 1

These graphs are plotted with respect to $Z_r$ for various values of $K$ and ratio $C_r/C_s$. No graph of main switch peak voltage is presented as it is simply the sum of the output voltage and peak to peak voltage ripple and is independent of the auxiliary circuit parameters.

(i) Peak Voltage across Auxiliary Switch Graph

Characteristic curve of auxiliary switch peak voltage $V_{S_{2, pk}}$ is shown in Fig. 3.1.
increases for $K < 1$ but decreases for $K > 1$ and for $K = 1$ the voltage across $S_2$ remains 1 pu. The reason for this behavior is twofold:

1) For $K < 1$ the voltage polarity across $C_r$ is negative and for $K > 1$ this voltage is positive as shown in Fig. 3.3. Just before the auxiliary circuit is activated the voltage across resonant inductor $L_r$ is zero. Fig. 3.3 (a) shows that for $K < 1$ the voltage across $C_r$ is negative and this adds up with voltage across $C_s$ to give the voltage across $S_2$. In such a case the voltage $V_{S2, pk}$ is always greater than 1 pu. Fig. 3.3 (b) shows that for $K > 1$ the voltage across $C_r$ is positive and is subtracted from voltage across $C_s$ to give voltage across $S_2$. In this case the voltage $V_{S2, pk}$ will always be less than 1 pu.

2) Regardless of auxiliary circuit parameters the current flowing through resonant inductor $L_r$ at end of interval 1 $[t_0-t_1]$ is always the input current $I_{in}$. Thus the energy in $L_r$ at end of this interval is $\frac{1}{2} L_r I_{in}^2$. By increasing the resonant impedance $Z_r$ the value of $L_r$ is actually increasing as seen from eq.(3.6) and increasing $L_r$ means increasing the energy which $L_r$ will transfer to resonant capacitor $C_r$. The resonant capacitor can store more energy only if its voltage $V_{C_r}$ increases.

From above two points it is concluded that as $Z_r$ increases the value of $L_r$ also increases as in eq. (3.6) and this means energy stored in $C_r$ increases. For $K < 1$ the resonant capacitor $C_r$ stores this increased energy as an increasing negative voltage and for $K > 1$ the energy is stored as an increasing positive voltage. The negative voltage adds to the voltage $V_{S2, pk}$ and positive voltage decreases $V_{S2, pk}$. This explains the trend of the graph of Fig. 3.1.

Lower the value of $K$ from 1, larger is the increase of peak voltage across. Too low values of $K$ are to be avoided because these give an excessive voltage stress across
the auxiliary switch $S_2$. For example from the graph it is seen that for $K = 0.25$ over-voltage can go as high as 1.7 pu which in this case means 680 Volt. A higher value of $K$ gives a lower peak voltage across $S_2$ but it is clear from Fig. 3.2 that this will result in a lower ZVS interval. So one of the design guidelines is to keep $K < 1$ so as to keep voltage stress across $S_2$ lower than 1 pu and at same time have an adequate ZVS turn-on interval.

From the graph it is also seen that as $C_s$ gets larger (ratio $C_r/C_s$ gets lower) the peak voltage $V_{S2, pk}$ increases more if $K < 1$ and will decrease more if $K > 1$. This is because larger value of $C_s$ means more energy stored in $C_r$ which affects the voltage $V_{S2, pk}$ as explained above.
Fig. 3.1 Peak Voltage Across auxiliary switch $S_2$ vs. resonant impedance $Z_r$
for $R_r = 1 \, \Omega$ and (a) $C_r/C_s = 20$ and (b) $C_r/C_s = 30$
(ii) Auxiliary Switch Peak Current Graph

The characteristic curve showing $I_{S2,pk}$ vs. $Z_r$ is shown in Fig. 3.2. From the curve it is seen that as resonant impedance of the auxiliary circuit $Z_r$ is increased, the current $I_{S2,pk}$ decreases. This is easily seen as a consequence of Ohm’s Law.

Another thing to note is that as $K$ is decreased the peak current increases. This is because by decreasing $K$ the auxiliary circuit current is being increased as explained in Section 3.3.2. Increased auxiliary circuit current also means increased auxiliary circuit peak current and hence higher $I_{S2,pk}$. This is also why $I_{S2,pk}$ increases for lower values of ratio $C_r/C_s$.

(iii) Main Switch Peak Current Graph

A graph of the main switch peak current $I_{S1,pk}$ vs. $Z_r$ is shown in Fig. 3.3. The basic characteristics of these curves are the same as those of the auxiliary switch peak current graph. This is because the peak current through the main switch is simply the sum of input current $I_{in}$ and the peak resonant current flowing in interval $5 \{t_e - t_s\}$ of the switching cycle. It is because of this reason that the current $I_{S1,pk}$ will never be lower than the input current $I_{in} = 1$ pu.
Fig. 3.2 Graph of Peak Current Of Auxiliary Switch for $R_r = 1$ $\Omega$ and

(a) $C_r/C_s = 20$ (b) $C_r/C_s = 30$. 

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Fig. 3.3 Graph of Peak current of Main Switch for $R_r = 1 \, \Omega$ and

(a) for $C_r / C_s = 20$ (b) for $C_r / C_s = 30$. 

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(iv) Voltage Across Capacitor $C_b$ just before Main Switch is turned off

A graph showing voltage $V_{Cb}$ vs. $Z_r$ where $V_{Cb}$ is the voltage across the capacitor $C_b$ just before switch $S_I$ is turned-off is shown in Fig. 3.4 This graph is important as it provides guidelines on the selection of capacitor $C_b$. The voltage $V_{Cb}$ should be as close to $-1$ pu as possible because it is the sum of the output voltage $V_o$ and $V_{Cb}$ that appears across the switch $S_I$ when it is turned-off. If $V_{Cb}$ is close to $-1$ pu then $V_o$ which is $1$ pu on addition to $V_{Cb}$ will give a zero resultant voltage across $S_I$. Thus $S_I$ will be turned-off with ZVS.

From Fig. 3.4 it is seen that as $K$ decreases keeping $Z_r$ and ratio $C_r/C_r$ the same the negative voltage $V_{Cb}$ decreases. This is because decreasing $K$ is equivalent to increasing $C_b$ as in eq. (2.45) and as energy stored in $C_b$ is $\frac{1}{2}C_b V_{Cb}^2$ therefore as $C_b$ increases $V_{Cb}$ has to reduce. As this affects turn-off, so the value of $K$ must be kept lower than $1$ to get as high rise of voltage $V_{Cb}$ as possible.

Decreasing ratio $C_r/C_r$ or increasing resonant impedance $Z_r$ increases the negative voltage across $C_b$. This is because both situations result in an increase of energy stored in the resonant capacitor $C_r$ as explained earlier. This increased energy is transferred to capacitor $C_b$ during interval $5 [t_4-t_5]$ and this results in an increase of the negative voltage across $C_b$. 

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Voltage across $C_b$ for $C_r/C_s = 20$

![Graph showing voltage across $C_b$ for $C_r/C_s = 20$.](a)

Voltage across $C_b$ for $C_r/C_s = 30$

![Graph showing voltage across $C_b$ for $C_r/C_s = 30$.](b)

Fig. 3.4 Graph Showing Voltage $V_{Cb}$ across Capacitor $C_b$ for $R_r = 1 \Omega$ and (a) $C_r/C_z = 20$ (b) $C_r/C_z = 30$
3.3.3.2 **Graphs of RMS current for auxiliary switch and average current for auxiliary circuit diodes in mode 1**

Unlike peak values rms and average values are time dependent. The vertical axis parameters of the following graphs have therefore been per unitised with respect to the length of the resonant cycle $T_r$ of the auxiliary circuit and the switching frequency $F_{sw}$. So the graphs can be read in the same way as peak value graphs in the previous section.

(i) Auxiliary Switch RMS Current Graph

The characteristic curve of auxiliary switch rms current $I_{s2\_rms}$ vs. $Z_r$ is shown in Fig. 3.1. The actual value of $I_{s2\_rms}$ can be found by reading off its value from Fig. 3.1 and multiplying the per unit value by:

$$X = I_b \cdot \sqrt{T_r \cdot F_{sw}}$$

where $T_r$ is given by eq. (3.8) and $F_{sw}$ is the switching frequency.

(ii) Average Current of Series Diode D2

A graph of the series diode average current $I_{D2\_avg}$ vs. $Z_r$ is shown in Fig. 3.2. Similar to the above graph the actual value of diode average current can be found by multiplying the value from the vertical axis of Fig. 3.2 by:

$$X = I_b \cdot T_r \cdot F_{sw}$$
The current $I_{D2\_avg}$ is exactly same as average current $I_{D4\_avg}$ of diode $D_4$ as both diode are in series in the auxiliary circuit. The average current of diode $D_1$ is approximately the same as $I_{D2\_avg}$.

From the rms and average current graphs it is clear that as $Z_r$ increases the currents decrease. This is a consequence of Ohm’s Law. Also as ratio $C_d/C_r$ decreases or variable $K$ decreases, the currents increase. This behaviour is because both these conditions result in an increase of the negative voltage across resonant capacitor $C_r$ as shown in Section 3.3.2 and this leads to an increase in the auxiliary circuit current.
Fig. 3.1 Graph of RMS current of Auxiliary Switch $I_{S2_{rms}}$ for $R_r = 1 \Omega$ and (a) for $C_r/C_s = 20$ and (b) for $C_r/C_s = 30$. 
Fig. 3.2 Graph Of Average Current $I_{D2\_avg}$ of diode D2 for $R_r = 1 \, \Omega$ and

(a) for $C_r/C_s = 20$ and (b) for $C_r/C_s = 30$. 
3.3.3.3 **Boundary between Mode 1 and Mode 2 Operation of the Converter**

As the input voltage to the ZVT converter goes higher and higher the duty cycle of the main switch \( S_t \) keeps getting lower and lower according to eq.(2.37) which is reproduced below:

\[
D = 1 - \frac{\sqrt{2} \cdot V_{in}}{V_o}
\]  

(3.11)

From eq. (3.11) it is seen that greater the value of input rms voltage lesser will be the duty cycle. So at the maximum value of \( V_{in} = 265 \) Volts, the value of \( D \) will be minimum at \( D_{min} = 6.3\% \). At this low value of duty cycle it may be possible that the main switch \( S_t \) is not on long enough to allow the auxiliary resonant circuit to complete its resonant cycle. If the main switch turns off before auxiliary circuit current has gone down to zero then the steady state analysis of Mode 1 will fail and the converter begins to operate under Mode 2 for high input voltages.

Characteristic curves depicting the minimum time that the main switch \( S_t \) has to remain on so that the proposed ZVT converter can still operate in Mode 1 is shown in Fig. 3.1. These curves are similar to previous curves of the auxiliary circuit as they are per unitized and plotted with respect to the per unit resonant impedance \( Z_r \) of the auxiliary circuit. Form the curves of Fig. 3.1 the minimum duty cycle of the converter for it to operate in Mode 1 i.e. \( D_{min,l} \) can be found out by multiplying the appropriate value on Y-axis by:

\[
X = T_r \cdot F_{sc}
\]  

(3.12)
Fig. 3.1 Graph showing the Minimum Time that Switch S₁ has to remain on for the converter to operate under Mode 1, for (a) $C_r/C_s = 20$ and (b) $C_r/C_s = 30$. 
If the value of $D_{min_i}$ from above curves comes out to be less than $D_{min}$ then the steady state analysis for Mode 2 has to be carried out. Another set of curves has to be drawn for Mode 2 so that it can be found out whether there are any over-voltages, over-currents or any other abnormal behavior of the converter in this mode.

3.3.4 Auxiliary Circuit Characteristic Curves When Converter Operates in Mode 2

In this mode of operation it is assumed that the main switch $S_I$ does not remain on long enough to allow the resonant current in the auxiliary circuit to complete its cycle. It should be noted that these curves are drawn for a peak input rms voltage $V_{in_{max}} = 265$ V which is the maximum voltage this converter is designed to operate on. The base impedance of the circuit remains $Z_{rb} = 107.48$ Ω which is the same value as for 90 V. The reason for not changing the base impedance is that the auxiliary circuit should be designed for optimum operation at the minimum rms input voltage which the converter is expected to handle. After designing for this minimum voltage, it is to be seen whether the design can work at high voltages also. Mode 2 operation occurs at high voltages only where duty cycle of the converter will be low. As the design which was done on low voltage is now being tested for high voltage, so the base values for both must be the same.
3.3.4.1 **Peak Voltage and Peak Current Graph for the Converter Switches in Mode 2**

These graphs are plotted with respect to \( Z_r \) for various values of \( K \). The value of the ratio \( C_r/C_s \) is kept 20 only as looking at the design curves for Mode 1 it is seen that lower the value of this ratio the larger are the current and voltage stresses on the converter components.

(i) **Peak Voltage across Auxiliary Switch Graph**

Characteristic curve of auxiliary switch peak voltage \( V_{S2,pk} \) is shown in Fig. 3.1. It is seen from curves that as resonant impedance \( Z_r \) increases the voltage across \( S_2 \) increases up to \( Z_r = 0.86 \) pu and then starts to decrease. On comparing this graph with Fig. 3.1 it is seen that peak voltage across \( S_2 \) in Mode 2 are much less than in Mode 1. This behaviour is easily explained because Mode 2 is at higher input voltage which also implies lesser input current according to eq. (3.1). Lesser input current means lesser energy is stored into the resonant capacitor \( C_r \) of the auxiliary circuit. Lesser energy in \( C_r \) means voltage across it will be less and as voltage across \( S_2 \) is sum of output voltage \( V_o \) and voltage across \( C_r \), so voltage across \( S_2 \) will also be less.

(ii) **Auxiliary Switch Peak Current Graph**

Graph of peak current through auxiliary switch \( S_2 \) is given in Fig. 3.2. From the graph it is seen that the peak currents are much less as compared to peak currents in Fig. 3.2. This is also because Mode 2 occurs at high input voltage and low input current. The low input current means less energy transferred to the auxiliary circuit. Hence the lower peak currents.
Fig. 3.1 Graph of peak voltage across Switch S1 for $R_r = 1 \ \Omega$ when the converter operates in Mode 2.

Fig. 3.2 Graph of peak current through switch S2 for $R_r = 1 \ \Omega$ when converter operates in Mode 2.
(iii) Main switch peak current graph.

The graph showing peak current through main switch $S_1$ in Mode 2 is given in Fig. 3.3. This graph also shows lesser peak currents as compared to Fig. 3.3. The reason is same as for peak current graph of auxiliary switch $S_2$ above.

![Graph of peak current through main switch $S_1$ for $Cr/Cs = 20$.](image)

Fig. 3.3 Graph of peak current through main switch $S_1$ for $R_r = 1 \, \Omega$ when the converter operates in Mode 2.

(iv) Voltage Across Capacitor $C_b$ just before Main Switch is turned off

The graph showing the peak voltage $V_Cb$ across capacitor $C_b$ just before the main switch $S_1$ is turned off in Mode 2 is given in Fig. 3.4. On comparing this graph with Fig. 3.4 it becomes apparent that peak voltage across $C_b$ is lesser in magnitude than that predicted under Mode 1. This behavior becomes obvious on examining Fig 2.5 and 2.7. From these figures it is clear that the flow of resonant current through capacitor $C_b$ is
interrupted suddenly at instant $t_5$ of the resonant cycle. The voltage $V_{Cb}$ stops rising at $t_5$ and starts decreasing until it becomes zero at instant $t_7$. If the whole of the resonant current had been allowed to pass through $C_b$ as in Mode 1, then rise of voltage $V_{Cb}$ would have been greater.

The lesser negative voltage across $C_b$ when $S_I$ turns off, forms the main disadvantage of operating the converter in Mode 2. When $S_I$ turns off the voltage that appears across it is the sum of the output voltage $V_o$ and voltage across $V_{Cb}$. A large negative value of $V_{Cb}$ will thus result in lesser voltage across $S_I$ and the switch will have a soft turn-off. But in Mode 2 the voltage $V_{Cb}$ is not allowed to rise to its full extent and this will affect the soft turn-off of switch $S_I$. It is to be noted that $S_I$ still has a ZVS turn-off under Mode 2 but it is not as efficient as Mode 1 turn-off.

![Voltage across $C_b$ for $\frac{Cr}{Cs} = 20$](image)

**Fig. 3.4** Graph showing the Voltage $V_{Cb}$ across Capacitor $C_b$ for $R_r = 1 \, \Omega$ when $S_I$ turns Off in Mode 2.
3.3.4.2 **Graphs of RMS Current for Auxiliary Switch and Average Current for Auxiliary Circuit Diodes in Mode 2**

Like the average and rms current graphs of Fig. 3.1 and Fig. 3.2 the characteristic curves in this section have also been per unitised with respect to the length of the resonant cycle $T_r$ of the auxiliary circuit and the switching frequency $F_{sw}$. So the graphs can be read in the same way as peak value graphs in the previous section.

(i) Auxiliary Switch RMS Current Graph

The graph of auxiliary switch rms current $I_{S2\_rms}$ vs. $Z_r$ in Mode 2 is shown in Fig. 3.1. The actual value of $I_{S2\_rms}$ can be found by reading off its value from the graph and multiplying the per unit value by a constant given by eq. (3.9) which is reproduced below:

$$X = I_{in} \cdot \sqrt{T_r \cdot F_{sw}}$$

where $T_r$ is given by eq. (3.8) and $F_{sw}$ is the switching frequency.

(ii) Average Current of Series Diode $D_2$

The graph of the series diode average current $I_{D2\_avg}$ vs. $Z_r$ in Mode 2 is shown in Fig. 3.2. Similar to the above graph the actual value of diode average current can be found by multiplying the value from the vertical axis of Fig. 3.2 by a constant given by eq.(3.10) which is reproduced below:

$$X = I_{in} \cdot T_r \cdot F_{sw}$$
Fig. 3.1 Graph of rms current of Auxiliary Switch S2 for R_r =1 Ω when the converter is operating in Mode 2.

Fig. 3.2 Graph of Average current in Series diode D2 for R_r =1 Ω when the converter is operating in Mode 2.
The current $I_{D2,\text{avg}}$ is exactly same as average current $I_{D4,\text{avg}}$ of diode $D_4$ as both diodes are in series in the auxiliary circuit. The average current of diode $D_3$ is approximately the same as $I_{D2,\text{avg}}$.

Comparing the above graph of rms switch current $I_{S2,\text{rms}}$ with Fig. 3.1 and the graph of average diode current $I_{D2,\text{avg}}$ with Fig. 3.2, it is again seen that the above graphs predict a much lower value of these currents than the graphs of Mode 1. This is to be expected as the input current in Mode 2 is lower than in Mode 1 and so lesser energy is transferred to auxiliary circuit. This causes the average and rms currents to be lower.

3.3.5 Soft switching of the main switch in Mode 2

The graph showing the ZVS interval vs. per unit resonant impedance $Z_r$ for different values of variable $K$ is given in Fig. 3.1. Although the graph is different from that in Fig. 3.2 it can still be said that for proper design of the converter the value of variable $K$ and $Z_r$ should be such that the ZVS interval in both Mode 1 and Mode 2 is adequate.
Fig. 3.1 Graph of the ZVS interval for $R_r = 1 \, \Omega$ when the converter operates in Mode 2.

3.4 CONCLUSIONS

In this chapter characteristic curves based on the steady state analysis of Chapter 2 were presented. From these curves certain insights towards the working of the converter were gained. The curves were drawn for that particular point on the input AC wave where the ZVS turn-on interval is the least which is same as the point when input current is maximum. This makes up the worst case condition of the converter.

From the curves it can be concluded that $K$ should be kept equal to or below 1 to keep the voltage stress across auxiliary switch less than 1 pu. Although the ZVS turn-on interval will be reduced, by keeping resonant impedance $Z_r$ low, an adequate interval can still be achieved. A higher value of $K$ also causes capacitor $C_b$ to charge up to a higher voltage $V_{C_b}$ which assists in turn-off of main switch $S_f$. 

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CHAPTER 4

CONTROL OF THE ZERO VOLTAGE TRANSITION CONVERTER

4.1 Introduction

The objective of the control circuit of any power factor correction converter is to make the non-linear rectifier look like a simple resistor with respect to the input mains. If this is the case then the input current will track the voltage like it does in case of a simple resistor and the input power factor shall be 1.0. An active power factor corrector does this by programming the input current to follow the instantaneous input rectified voltage.

In practice there is always some distortion in the input current. This harmonic distortion can be as a result of many factors like the ripple across the output capacitor, the input inductor, feedback loop and input rectifiers. This distortion is harmful because it increases the rms value of input current without increasing the power delivered to load. Also any other equipment which is connected in parallel with the power converter will be affected by the harmonic currents. So regulatory agencies have set up standards such as the IEC-1000-3-2 which specify the maximum limits for the amount of these harmonic currents. This chapter deals with the control circuit which is used to implement PFC in the ZVT converter.

The outline of this chapter is as follows:

Section 4.2 gives a brief description of the average current control scheme for power factor correction applications.
Section 4.3 gives the step-by-step procedure for designing the voltage loop compensator and current loop compensator.

Conclusions are made at the end in Section 4.4

4.2 **ACTIVE POWER FACTOR CORRECTION CONTROL CIRCUIT**

An active power factor corrector can program the input current to follow the input voltage using two methods of current mode control:

(i) Peak current mode control:

(ii) Average current mode control

Average current mode control is preferred as the peak current method has lower gain, wide bandwidth current loop and results in significant error between programmed signal and actual current [33]-[35]. Also slope compensation is a must with peak current control otherwise the converter will not be stable and can go into sub-harmonic oscillations.

The active power factor corrector control circuit uses a voltage error amplifier in the feedback loop to control the output voltage. A current error amplifier is also provided in an inner current loop so that the programmed current signal can be compared with actual input current which can then be forced to follow the rectified input voltage. The inner current loop is at least ten times faster than outer voltage loop and this increases the transient response of the converter. The basic control circuit is given in the Fig. 4.1.

The Fig. 4.1 shows some circuitry other than the current and voltage error amplifiers. The additional circuitry is a squarer, divider and multiplier network. The function of this network is to detect the input voltage $V_{in}$ and feed-forward it as voltage
$V_{fr}$. The output of the voltage error amplifier is divided by the square of $V_{fr}$ before being multiplied by the rectified input voltage signal. All this is done to keep the gain of the voltage loop constant and independent of the input voltage variations. The output of the voltage error amplifier will become a power control in this case. This can be proved by an example:

Assuming the output $V_{ea}$ of voltage error amplifier to be constant and the input voltage increases two times. So the output of the voltage error amplifier will be divided by square of input voltage signal or by four times the previous value $V_{fr}$. The multiplier will then multiply this by the input voltage signal which will become twice because of $V_{in}$ becoming two times. The result is that twice the input voltage signal divided by four times feed-forward voltage will give half the current programming signal. Half the input current signal to twice the input voltage gives the same amount of power. This means that the actual control is constant power control.
Fig. 4.1 Design of Control loop for Power Factor Correction Applications.
4.3 CONTROL LOOP DESIGN

In the control loop design of the proposed ZVT converter it is assumed that a PFC controller like UC – 3855A/B is used. Therefore the following results hold true for this controller although the general design approach will be the same.

4.3.1 SMALL SIGNAL MODEL OF THE CONVERTER

The small signal model of the proposed ZVT converter is the same as that of the basic PFC boost converter as both of the converters operate similarly during most of their switching cycle. The only difference is during the turn-on and turn-off transitions of the main switch and this has no bearing on the design of the control loop.

The small signal model of the boost converter is given by the following eq.:

\[ G_{ps} = \frac{V_o}{s \cdot L_{in}} \]  \hspace{1cm} (4.1)

This is a simplified model in which the effect of the ESR of the output capacitor has been neglected. However this model is still accurate and matches the exact model at higher frequencies. The power stage has a single pole response with a 20 dB/decade roll-off rate and a phase lag of −90 degrees as shown in Fig. 4.1.
Fig. 4.1 Gain characteristic and Phase characteristic of power stage.

4.3.2 Compensation of the Current Loop

A type 2 error amplifier is used to provide the required compensation. This compensator has the gain characteristic given in Fig. 4.1 (b) with a zero placed at the cross over frequency $f_c$ to give adequate phase margin of about 45 degrees at cross over. This makes for a very stable system with low overshoots. A pole is put at half the switching frequency in order to reduce the switching noise.

The first step in designing the current error amplifier is to fix the cross over frequency $f_c$ after which signals of higher frequency will be attenuated. The frequency $f_c$ must be high enough to give a wide bandwidth which translates into a fast transient response but should also be low enough to attenuate any noise in the circuit. Usually
frequency \( fc \) is chosen to be a tenth of the switching frequency and so a cross over frequency of 10kHz will be adequate for the current error amplifier.

Due to the specific UC - 3855 A/B being used the gain of the power stage at 10kHz is given by:

\[
G_{ps} = \frac{V_o \cdot R_{sense}}{s \cdot L_{in} \cdot V_s} \tag{4.2}
\]

where \( R_{sense} \) is the current sense resistor used to sense the actual output current and \( V_s \) is the peak of the internally generated oscillator ramp. As can be seen by comparison eq.(4.1) is the same as eq.(4.2). For this design \( R_{sense} = 2.9 \ \Omega \) with a current transformer of turns ratio 50:1 is used and \( V_s = 5.2 \ \text{V} \) for the specific IC. So gain at cross over becomes:

\[
G_{ps \_ fc} = \frac{400 \cdot \left( \frac{2.9}{50} \right)}{2 \cdot \pi \cdot 10kHz \cdot 1050 \mu F \cdot 5.2} = 0.0675 \tag{4.3}
\]

So in order to keep cross over 10kHz the overall gain at this frequency must be 1. Therefore the gain of the current error amplifier at cross over frequency must be:

\[
G_{CEA \_ fc} = \frac{1}{G_{ps \_ fc}} = \frac{1}{0.0675} = 14.81 \tag{4.4}
\]

but looking at Fig. 4.1 of current amplifier the gain is given by:

\[
G_{CEA \_ fc} = \frac{R_{e}}{R_{ci}} = \frac{R_{e}}{3k\Omega} \tag{4.5}
\]
Fig. 4.1 (a) Type 2 Current Error Amplifier (b) Ideal Gain characteristic of the Error Amplifier
Taking value of \( G_{CEA, fe} \) from eq.(4.4), the value of \( R_f \) from eq. is found to be 44.44 \( K\Omega \).

For a type 2 error amplifier the relationship between zero at cross over frequency \( f_{cz} \), and circuit parameters is given by:

\[
f_{cz} = f_{cx} = \frac{1}{2 \cdot \pi \cdot R_{cf} \cdot C_{ce}}
\]  

(4.6)

Therefore rearranging above eq. gives the value of capacitor \( C_{ce} \):

\[
C_{ce} = \frac{1}{2 \cdot \pi \cdot 10kHz \cdot 44K\Omega} = 350 \text{ pF}
\]  

(4.7)

The high frequency pole placed at \( f_{cp} = 50kHz \) is given by following eq.:

\[
f_{cp} = \frac{1}{2 \cdot \pi \cdot R_{cf} \cdot \left( \frac{C_{cp} \cdot C_{ce}}{C_{cp} + C_{ce}} \right)} = \frac{1}{2 \cdot \pi \cdot R_{cf} \cdot C_{cp}}
\]  

(4.8)

This equation is true since \( f_{cp} \) is a high frequency pole and \( C_{cp} \) is low compared to \( C_{ce} \). So value of capacitor \( C_{cp} \) can be found from above eq.(4.8) as:

\[
C_{cp} = \frac{1}{2 \cdot \pi \cdot 44K\Omega \cdot 50kHz} = 70 \text{ pF}
\]  

(4.9)

The open loop gain plot of the current compensator and power stage is given in Fig. 4.2. From the figure it is clear that cross over frequency is about 11kHz and phase margin is 35 degrees which is adequate.
Fig. 4.2 Gain and Phase characteristic of the Open Loop Current Regulator with Power Stage.
4.3.3 Compensation of the Voltage Loop

The design of the voltage loop is given in [34]. The primary function which the voltage loop has to meet is to keep the input current distortion to a minimum. The bandwidth of the voltage loop is typically about 15 Hz and for such a low bandwidth stability is not a problem. The reason for such a low bandwidth is that the output voltage on DC bus contains a small 2\textsuperscript{nd} harmonic voltage and if this voltage is fed back to the voltage error amplifier it will modulate the output of the amplifier. This modulation by the 2\textsuperscript{nd} harmonic voltage will cause a considerable 3\textsuperscript{rd} harmonic distortion in the input current. So by keeping the bandwidth of voltage control loop low, the unwanted modulation of the error amplifier output by the 2\textsuperscript{nd} harmonic ripple voltage is minimised.

At the low frequency of the voltage loop the power stage with the closed current loop form an integrator. This has a gain characteristic which rolls off at 20 dB/decade and has a 90 degree phase lag. The voltage loop must have a pole in order to reduce the second harmonic ripple and to shift the phase by 90 degrees. The Fig. 4.1 shows a type – 1 voltage error amplifier with the characteristic gain curve.

The first step is to determine the amount of 2\textsuperscript{nd} harmonic ripple in the output. This can be found from eq.(3.16) and eq. (3.17) as shown below:

\[
V_{\text{chg}_{-pk}} = \frac{I_{\text{chg}_{-pk}}}{2 \cdot \pi \cdot F_r \cdot C_o} = \frac{0.625}{2 \cdot \pi \cdot 120Hz \cdot 207\mu F} = 4 \text{ V} \quad (4.10)
\]

\[
V_{\text{chg}_{-pk-pk}} = 2 \cdot V_{\text{chg}_{-pk}} = 8 \text{ Vp-p} \quad (4.11)
\]
Fig. 4.1 (a) Type–1 Voltage Error Amplifier (b) Ideal Characteristic Curve of given Amplifier
The next step is to determine the maximum ripple which can be tolerated on $V_{\text{VEA}}$ which is the output of the voltage error amplifier. The converter should meet the 3% THD specification. The distortion due to the multiplier which feeds forward the input voltage to the control is limited to 1.5%. Allowance for distortion due to other sources is limited to 0.75% and so distortion due to 2nd harmonic output ripple must be limited to 0.75%. According to ref [35] for 0.75% distortion the ripple on Voltage Error Amplifier must be limited to 1.5%. The output of the voltage error amplifier of UC-3855A/B is 1–6 V. So peak ripple voltage on output of error amplifier is:

$$V_{\text{EA}_{-\text{pk}}} = \%\text{ripple} \cdot V_{\text{vea}} = \frac{1.5}{100} \cdot (6 - 1) = 0.075 \text{ V} \quad (4.12)$$

The required gain of the error amplifier at 2nd harmonic ripple must be the allowable error amplifier ripple divided by the output ripple:

$$G_{\text{VEA}_{-\text{fr}}} = \frac{V_{\text{EA}_{-\text{pk}}}}{V_{\text{chg}_{-\text{pk}}}} = \frac{0.075}{8} = 0.0093 = -40.6 \text{ dB} \quad (4.13)$$

The value of resistors of the voltage divider network shown in Fig. 4.1 is arbitrary. Resistor $R_{vi}$ is chosen to be 1.32 MΩ to keep power dissipation low and so resistor $R_{vf}$ becomes 10 KΩ. This divider network will scale down the output 400 V to 3 V and this is compared with the internally generated reference which is 3 V also. The value of capacitor $C_{vf}$ can be found easily as:

$$C_{vf} = \frac{1}{2 \cdot \pi \cdot f_r \cdot G_{\text{VEA}_{-\text{fr}}} \cdot R_{vi}} = \frac{1}{2 \cdot \pi \cdot 120 \text{Hz} \cdot 0.0093 \cdot 1.32 \text{MΩ}} = 0.1 \mu\text{F} \quad (4.14)$$
Now a pole due to combination of $R_{cf}$ and $C_{cf}$ has to placed at cross over frequency so that 2$^{\text{nd}}$ harmonic ripple frequency is attenuated as well as an adequate phase margin of 45 degrees is provided. The cross over frequency $f_{vr}$ can be found from the fact that at cross over frequency the voltage loop gain which is the product of the gain of error amplifier and power stage shall be 1.

For all cases of Average Current Mode Control, the gain of the power stage is expressed as:

$$G_{ps_{-fvr}} = \frac{V_p}{V_{VEA}} = \frac{P_{in}}{\Delta V_{VEA}} \cdot \frac{-jX_{Cf}}{V_o} = \left( \frac{250}{0.95} \right) \cdot \frac{1}{(6-1) \cdot \frac{2 \cdot \pi \cdot f_{vr} \cdot 207 \, \mu F}{400}} = -j \cdot 101.2 \cdot \frac{f_{vr}}{f_{vr}} \quad (4.15)$$

The error amplifier gain is:

$$G_{VEA_{-fvr}} = \frac{-j}{2 \cdot \pi \cdot f_{vr} \cdot R_{vi} \cdot C_{cf}} = \frac{-j}{2 \cdot \pi \cdot f_{vr} \cdot 1.32 \, MS \cdot 0.1 \, \mu F} = -j \cdot 1.206 \cdot \frac{1}{f_{vr}} \quad (4.16)$$

The product of $G_{VEA_{-fvr}}$ and $G_{ps_{-fvr}}$ is 1 at cross over frequency $f_{vr}$. Therefore solving above eq.(4.15) and eq.(4.16) for $f_{vr}$ we get:

$$1 = G_{ps_{-fvr}} \cdot G_{VEA_{-fvr}} = \frac{-j \cdot 101.2}{f_{vr}} \cdot \frac{-j \cdot 1.206}{f_{vr}} \quad (4.17)$$

Solving above eq. $f_{vr}$ if found to be 11 Hz. Now the feedback resistor $R_{cf}$ can be easily found as:
\[ R_f = \frac{1}{2 \cdot \pi \cdot f_v \cdot C_v} = \frac{1}{2 \cdot \pi \cdot 11\text{Hz} \cdot 0.1\mu\text{F}} \approx 145\text{K}\Omega \quad (4.18) \]

The closed loop response of the voltage loop and power stage is given in Fig. 4.2. As can be seen the bandwidth is about 12 Hz and there is no steady state error in the output of converter.

![Gain characteristic of closed Voltage Loop and Power Stage](image)

**Fig. 4.2 Gain Characteristic of Closed Voltage Loop and Power Stage**
4.4 CONCLUSIONS

In this chapter the control circuit for the proposed ZVT converter was designed for PFC application. A compensated current error amplifier was designed for the inner current loop and a compensated voltage error amplifier was designed for the outer voltage loop. The closed loop performance is judged on the basis of Bode Plots drawn for each error amplifier. The final design satisfies all requirements of minimum THD in input current.
CHAPTER 5

PROTOTYPING AND DESIGN

5.1 INTRODUCTION

This chapter presents the design procedure to be followed when designing the proposed converter. The design procedure is followed by a design example to illustrate the design process and help in the selection of proper converter components. The design of the converter is based on the characteristic curves derived in Chapter 3 and other considerations such as proper ZVS interval, proper turn-off, output voltage ripple, input current ripple, duty cycle range among others.

Although the example utilizes characteristic curves, which have been generated for a specific operating point, the basic principles are the same for all operating points. Characteristic curves that are generated for values other than the ones used in the example will yield the same results as those already derived.

The outline of this chapter is as follows:

Section 5.2 presents the design objectives for the ZVT converter that was proposed and analyzed in Chapter 2. A design example follows and demonstrates the selection of components of the converter.

Section 5.3 presents simulated and experimental waveforms which validate the design process

Section 5.4 summarizes the main points of this chapter.
5.2 **Design of the Proposed ZVT Converter**

The design specifications and design procedure of the proposed ZVT converter are presented in this section.

5.2.1 **Design Objectives and Specifications**

The converter is designed to meet the following objectives:

1) The main switch must have a ZVS turn-on to minimize the switching losses.

2) The main switch must have proper ZVS turn-off to minimize turn-off losses.

3) The reverse-recovery current of the boost diode must be eliminated in order to reduce the EMI that results from such a current.

4) The resonant cycle of the auxiliary circuit $T_r$, must be kept as short as possible because larger the cycle length, larger will be the losses in the auxiliary circuit. Also smaller the value of $T_r$, larger will be the length of the period over which the converter operates in Mode 1 at high voltages.

The specifications for the design of the converter are as follows:

(i) Output Power, $P_o = 250$ W

(ii) Output Voltage, $V_o = 400$ V

(iii) Input Voltage $V_{in} = 90 - 265$ V rms

(iv) Switching Frequency, $F_{sw} = 100$ kHz

(v) Desired Efficiency, $\eta > 95 \%$.

(vi) Input Current peak – to peak ripple, $\Delta I = 20 \%$

(vii) Output Voltage peak ripple, $V_{pp, pk} < 1 \%$
5.2.2 Design Procedure and Example

The design procedure is divided into two parts:

(i) Design of the Power Circuit.

(ii) Design of the Auxiliary resonant Circuit.

5.2.2.1 Design of the Power Circuit

The guidelines for the design of the power circuit are presented in this section except for the main boost switch as its peak current rating depends upon the operation of the auxiliary circuit. The equations used have been previously derived in Section 2.4 of Chapter 2.

a) Input Inductor

The value of the input inductor \( L_{in} \), must be determined first because its value sets the peak input current which the converter switches have to withstand and therefore this current is necessary to rate other power circuit components. As PFC is required the peak current at input of converter shall occur at the peak of the minimum rms AC input voltage, \( V_{in\_min} = 90 \) V. This maximum current without ripple is:

\[
I_{in\_pk} = \frac{\sqrt{2} \cdot \frac{P_o}{\eta}}{V_{in}} = \frac{\sqrt{2} \cdot 250}{0.95 \cdot 90} = 4.135 \ A
\]  

\[ (5.1) \]

The maximum peak – peak ripple current is

\[
\Delta I_{rpp} = I_{pk\_max} \cdot \Delta I = 4.135 \times 20\% = 0.827 \ A
\]  

\[ (5.2) \]
Therefore the maximum peak input current with ripple is

\[
I_{\text{peak max}} = I_{\text{pk max}} + \frac{\Delta I_{\text{pp}}}{2} = 4.135 + \frac{0.827}{2} = 4.55 \text{ A}\quad (5.3)
\]

Since the input current is a sinusoid with some ripple, the peak current occurs around \(\alpha = 90^\circ\). The duty cycle of the converter at this point when the maximum current occurs can be found by applying the following eq. (5.4), which holds true for any boost converter:

\[
D_{\text{pk}} = 1 - \frac{\sqrt{2} \cdot V_{\text{in min}}}{V_o} = 1 - \frac{\sqrt{2} \cdot 90}{400} = 0.682\quad (5.4)
\]

The input inductor value can be simply found from the following equation which holds true for any boost converter:

\[
L_{\text{in}} = \frac{\sqrt{2} \cdot V_{\text{in min}} \cdot D_{\text{pk}}}{\Delta I_{\text{pp}} \cdot F_{\text{sw}}} = \frac{\sqrt{2} \cdot 90 \cdot 0.682}{0.827 \cdot 100 \text{kHz}} = 1050 \mu\text{H.}\quad (5.5)
\]

Where \(F_{\text{sw}}\) is the switching frequency.

b) Output Capacitor

The output capacitor acts as an energy storage element. It stores energy when the input voltage and current are near their peak and provides this energy to the output load when the line is low. The output capacitor filters the 2\(^{nd}\) harmonic current that flows
through the boost diode. The criterion for selection of this capacitor is the amount of tolerable ripple in the output voltage.

Since the converter operates with PFC the input current and voltage are sinusoids and the input power is therefore a $\sin^2$ function which is equivalent to $K^*(1 - \cos(2\omega t))$ where $K^*$ is the average value. The average output power has the same waveform as the average input power and so the output current must also be a $\sin^2$ function as output voltage is a constant DC. The amplitude of this AC component of output current is the same as the DC component which is given by:

$$I_{\text{chg- pk}} = \frac{P_o}{V_o} = \frac{250}{400} = 0.625\ A$$  \hspace{1cm} (5.6)

The amplitude of the ripple voltage across $C_o$ is:

$$V_{\text{chg- pk}} = \frac{I_{\text{chg- pk}}}{2 \cdot \pi \cdot f_r \cdot C_o}$$  \hspace{1cm} (5.7)

Eq. (5.7) can be re-arranged to give:

$$C_o = \frac{I_{\text{chg- pk}}}{2 \cdot \pi \cdot f_r \cdot V_{\text{chg- pk}}} = \frac{0.625}{2 \cdot \pi \cdot 120\ Hz \cdot (0.01 \cdot 400)} = 207 \ \mu F$$  \hspace{1cm} (5.8)

c) Boost Diode

The maximum voltage across the boost diode is the output voltage $V_o = 400\ V$ which appears across the diode when the main switch is turned-on. The peak current that flows through the diode is the peak current with ripple that flows through the converter
namely $I_{rpk\_max} = 4.55\ A$ as obtained from eq. (5.3). The average current that flows through the diode is:

$$I_{D_{1\_avg}} = \frac{P_o}{V_o} = \frac{250}{400} = 0.625\ A$$

(5.9)

d) Input Rectifier Diodes

The maximum voltage that appears across an input bridge diode is the maximum input voltage that is encountered during high line conditions $V_{in\_max}$ at input of the converter:

$$V_{in\_pk} = V_{in\_max} \cdot \sqrt{2} = 265 \cdot \sqrt{2} = 375\ V$$

(5.10)

The peak current that flows through them is $I_{rpk\_max} = 4.55\ A$ as obtained from eq. (5.3). The average current that an input diode must conduct is the average of half a sinusoid:

$$I_{Din\_avg} = \frac{1}{\pi} \int_0^{\pi} I_{in\_avg} \cdot \sin(\alpha x) \cdot d(\alpha x) = \frac{2 \cdot I_{in\_pk}}{\pi}$$

(5.11)

Therefore

$$I_{Din\_avg} = \frac{2 \cdot 4.135}{\pi} = 2.63\ A$$

(5.12)
5.2.2.2 Design of the Auxiliary Circuit and Main Switch

Guidelines for designing the auxiliary circuit are presented in this section.

(i) Base Values

The graphs of characteristic curves for auxiliary circuit voltages and currents that are presented in Chapter 3 are per unitized graphs. In order to correctly use these graphs proper base values are to be selected. The base voltage is defined as:

\[ V_b = V_o = 400 \, V \]  \hspace{1cm} (5.13)

The base current is defined as:

\[ I_b = I_{pk \_{max}} \frac{\Delta I_{rep}}{2} = 4.135 - \frac{0.827}{2} = 3.722 \, A \]  \hspace{1cm} (5.14)

The base impedance is therefore defined as:

\[ Z_{rb} = \frac{V_b}{I_b} = \frac{400}{3.722} = 107.48 \, \Omega \]  \hspace{1cm} (5.15)

The base time is defined as the length of the natural resonant cycle of the auxiliary circuit:

\[ T_r = 2 \cdot \pi \cdot \sqrt{L_r \cdot C_r} \]  \hspace{1cm} (5.16)
The worst case condition where the ZVS interval is the least occurs when the input current is at its maximum peak. At this value of peak current the impedance is \( Z_{rb} = 1 \text{ pu} \) and so the auxiliary circuit should be designed for this value only.

(ii) Resonant Inductor

The selection of the resonant inductor \( L_r \) is made keeping in mind that the reverse recovery current of the boost diode is to be made zero. Therefore the selection of resonant inductor depends on the boost diode’s turn-off \( \text{di/dt} \) and this can be controlled by slowly diverting the current flowing through it to the resonant inductor.

Increasing the value of \( L_r \) increases the rise time of the current flowing through it which in turn decreases the reverse recovery current of the boost diode. But this results in an increase in duration of the resonant cycle \( T_r \), which leads to increased rms currents in the auxiliary circuit and increased conduction losses. So a compromise must be made in the selection of the resonant inductor. \( L_r \) is so chosen that it allows the auxiliary circuit current to ramp up to the maximum input current \( I_{in, pk} \), within three times the specified reverse recovery time \( t_{rr} \) as determined experimentally in [36]. The boost diode must be an ultra-fast recovery diode with as low a value of \( t_{rr} \) as possible because a slower diode would require a larger value of \( L_r \). Increasing \( L_r \) would increase resonant cycle length \( T_r \) and this would increase the conduction losses in the auxiliary circuit. So an ultra-fast diode which will satisfy all voltage and current requirements as outlined in Section 5.2.2.1 and have minimum \( t_{rr} \) is selected. Assuming that \( t_{rr} = 30 \text{ ns} \) the value of \( L_r \) can be found from following eq.:

\[
L_r = \frac{3 \cdot t_{rr} \cdot V_{S2, pk}}{I_b} = \frac{3 \cdot 30 \text{ ns} \cdot (0.7 \cdot 400)}{3.722} = 5.8 \mu\text{H}
\]

\[ (5.17) \]
where $V_{S2, pk}$ is the peak voltage across switch $S_2$ and is assumed 0.7 pu and has been obtained by iteration as will be explained later.

(iii) Resonant Capacitor

The value of the resonant capacitor $C_r$ is selected from the graph of ZVS interval vs. resonant impedance $Z_r$ shown in Fig. 3.3 (a) Since $L_r$ has already been selected, we have to look for the least value of $C_r$ that will give an adequate ZVS turn-on interval as well as good turn-off. Also a low value of resonant period $T_r$ is required so that auxiliary circuit conduction losses are low. For proper design we select from Fig. 3.3 (a) the curve $K = 3$ and $Z_r = 0.21$ pu and the value of $C_r$ can be determined from eq (3.6) to be:

$$C_r = \frac{L_r}{(Z_r \cdot Z_{rb})^2} = \frac{5.8 \mu H}{(0.21 \cdot 107.48)^2} = 11 \text{ nF}$$

(5.18)

Addition of a capacitor across Switch $S_I$ is not required as it gives higher rms currents in the auxiliary circuit which leads to more conduction losses. ZVS at turn-off is provided by capacitor $C_b$. The main switch has an internal capacitance of about 500 pF and so ratio $C_r/C_s$ becomes:

$$\frac{C_r}{C_s} = \frac{11}{0.5} = 22$$

(5.19)

Although this value is different from the values of $C_r/C_s$ for which the characteristic curves in Chapter 3 have been drawn, the graph for $C_r/C_s = 20$ can still be used to design the circuit as the difference is not that much as far as auxiliary circuit design is concerned.

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From the values of $K$, $Z_r$, and ratio $C_r/C_r$ chosen it can be found Fig. 3.5 (a) that the peak voltage across auxiliary switch $V_{S2.pk}$ will be 0.64 pu. x 400 = 256 V. This value of $V_{S2.pk}$ is almost the same as the one used in eq.(5.17). $T_r$ can be found out from eq. (5.16) to be $= 1.587 \mu s$. From the graph of Fig. 3.3 (a) the value of the ZVS time interval for $Z_r = 0.21$ pu and $K = 3$ is found to be 0.025 pu. The actual value of the interval can be found by multiplying this value by $T_r$ to give $0.025 \times 1.587 \mu s = 40$ ns.

(iv) Auxiliary Capacitor $C_b$

The selection of capacitor $C_b$ is easy. By fixing the value of parameter $K = 3$ and knowing the value of the resonant capacitor $C_r$ then by applying eq. (3.8) the value of $C_b$ becomes:

\[
C_b = \frac{C_r}{K} = \frac{11nF}{3} = 3.67 \text{ nF.}
\]  

(v) Rating of the Auxiliary Switch

The peak voltage across the switch is 0.64 pu. or 256 V as found above. Knowing $Z_r$ and $K$ the peak current $I_{S2.pk}$ can be determined from Fig. 3.6 (a) to be 1.61 pu. x 3.722 = 5.99 A. The rms current of the switch is found from graph of Fig. 3.9 (a) to be:

\[
I_{S2.rms} = (I_{S2.rms, pu}) \cdot I_b \cdot \sqrt{T_r \cdot F_{sw}} = (0.53) \cdot 3.722 \cdot \sqrt{1.587 \mu s \cdot 100kHz} = 0.786 A
\]  

(v) Rating of auxiliary circuit diodes

The auxiliary circuit diodes have the same voltage rating as that of boost diode. This is simply done to simplify the selection of the diodes because in actual practice the
voltage appearing across the auxiliary circuit diodes will be less than that appearing across the boost diode.

The two series diodes $D_2$ and $D_4$ will conduct the same peak current as the auxiliary switch $S_2$. This peak current $I_{S2,pk}$ was found from above to be $1.6 \text{ pu.}=5.95 \text{ A}$. The peak current through diode $D_3$ will also be somewhat the same as for diodes $D_2$ and $D_4$. The peak current through diode $D_3$ is the peak current with ripple $I_{rpk\_max}$ that flows in the converter which was found to be 4.55 A from eq. (5.3).

For $Z_r = 0.21 \text{ pu}$ and $K = 3$ the average current through diode $D_2$ is found from Fig. 3.10 (a) to be $0.21 \text{ pu}$ which is:

$$I_{D2\_avg} = (I_{D2\_avg\_pu} \cdot I_b \cdot T_r \cdot F_{sw} = (0.21 \text{ pu}) \cdot (3.722 \text{ A}) \cdot 1.587 \mu \text{s} \cdot 100 \text{ kHz} = 0.12 \text{ A}$$  

(5.22)

The rest of the diodes in the auxiliary circuit also have approximately the same average current.

(vi) Rating of Main Switch

The maximum voltage that this switch must be able to handle is the output voltage $V_o$ with ripple. The ripple in the output voltage can be found as

$$V_{chg\_pk} = 0.1 \times 400 = 4 \text{ V.}$$  

(5.23)

Thus the switch $S_i$ must handle 404 V.
The peak current that flows through the main switch can be found from graph of Fig. 3.7 (a) for \( Z_r = 0.21 \) pu and \( K = 3 \) to be \( 2.27 \) pu x \( 3.722 = 8.448 \) A. In order to find the rms current of main switch an assumption is made that the current flowing in auxiliary circuit does not significantly increase the rms current through this switch. The duty cycle of the main switch is expressed as a time varying function as follows:

\[
D(\alpha t) = \frac{V_o - V_{inpeak} \cdot \sin(\alpha t)}{V_o} \quad (5.24)
\]

From the definition of rms, the maximum rms current for the switch can be found out to be:

\[
I_{s1_{-rms}} = \frac{1}{\sqrt{\pi}} \int_0^\pi (I_{pk_{-max}} \cdot \sin(\alpha t))^2 \cdot D(\alpha t) \cdot d(\alpha t) \quad (5.25)
\]

eq. (5.25) can be simplified to give:

\[
I_{s1_{-rms}} = I_{pk_{-max}} \cdot \sqrt{\frac{1 - 4 \cdot V_{in_{-min}} \cdot \sqrt{2}}{3 \cdot \pi \cdot V_o}} = 3.722 \cdot \sqrt{\frac{1 - 4 \cdot 0.90 \cdot \sqrt{2}}{3 \cdot \pi \cdot 400}} = 2.25 \text{ A} \quad (5.26)
\]

(vii) Voltage across Main Switch at turn-off

From Fig. 3.8 (a) it can be seen that for \( K = 3 \) and \( Z_r = 0.21 \) the voltage across capacitor \( C_b = -0.87 \) pu. This means that at turn-off switch \( S_f \) has a net voltage across it of only \( 1 - 0.87 = 0.13 \) pu. Multiplying this by the base value \( V_b = 400 \text{ V} \) the actual voltage across \( S_f \) comes out to be \( 0.13 \times 400 = 52 \text{ V} \). Therefore turn-off losses are also greatly reduced.
(viii) Boundary between Mode 1 and Mode 2 of Operation

The boundary between Mode 1 and Mode 2 of operation can easily seen from Fig. 3.11. From the fig, it can be seen that the minimum time that switch S1 has to remain on to operate in Mode 1 for $K = 3$, $Zr = 0.21$ and $Cr/Cb = 20$ is 0.31 pu. So the minimum duty cycle in Mode 1 will be:

$$D_{\text{min}} = T_{on} \cdot T_r \cdot F_{sw} = 0.31 \cdot 1.587 \mu s \cdot 100kHz = 0.05$$  \hspace{1cm} (5.27)

As this value is below 0.063 which is the duty cycle of the converter at peak of the 265 V input ac wave, so it is concluded that the converter is designed to operate under Mode 1 only.

5.3 SIMULATED AND EXPERIMENTAL RESULTS OF THE PROPOSED CONVERTER

The feasibility of the converter presented in this chapter was verified by results obtained from a 250 W experimental prototype switching at 100 kHz. The value of resonant inductor used was $L_r = 6 \mu H$, resonant inductor $C_r = 15$ nF and $C_b = 2.5$ nF. A higher value of resonant capacitor was used than that predicted theoretically as the capacitor $C_b$ charges up to the expected value only by using a larger resonant capacitor. As voltage across $C_b$ causes ZVS of $S_t$ so this change was necessary. IRF840 was the Mosfet used for both the main switch $S_t$ and auxiliary switch $S_2$. Although a larger switch such as IRFP460 can be used as main switch to give lower conduction losses, it was not used because a larger switch also requires a faster gate driver to charge up its large gate-
source capacitance. As this requires a Mosfet driver with higher current capability so a smaller switch which requires a smaller gate driver was used. The components used are listed in Table 5.1.

The experimental setup was not exactly as that shown in Fig. 2.1. In the experimental setup a large dc capacitor was placed in the input as shown in Fig. 5.1. The purpose of doing so is that the analysis and design of the proposed converter have been done for one particular point of the input ac wave. This point is the peak of the 90 V input ac wave at which the input current will be the maximum. This point is also the point where the ZVS turn-on interval is the least. So by putting a large dc capacitor at the input and adjusting the voltage across it to be the same as the peak of the 90 V input ac wave, the circuit conditions are being set for this particular point only. This setup will thus verify the analysis and design procedure of the converter.

From Fig. 5.2 and Fig. 5.3 it can be seen that \( S_I \) has ZVS at both turn-on and turn-off. The negative current through \( S_I \) at turn-on decreases the voltage across it slowly and then its body diode starts conduction. As voltage across switch is zero at turn-on there are no switching losses. At turn-off the voltage appearing across \( S_I \) is not absolutely zero but around 80 V. This means that the voltage across \( C_b \) is around 320 V or 0.8 pu. The characteristic curves of Fig. 3.8(a) predict a voltage of 0.76 across \( C_b \) at turn-off for the selected parameters and this is quite close to the actual value. The rate of voltage rise across the switch is lesser than in hard switching and so turn-off losses are also reduced.

Fig. 5.4 shows the auxiliary switch \( S_2 \) switching waveforms. As shown in figure the turn-on of \( S_2 \) is at ZCS. Also the voltage appearing across \( S_2 \) i.e. \( V_{S2\_peak} \) is only 220 V instead of the full output voltage of 350 V. The value of \( V_{S2\_peak} \) predicted by
characteristic curve Fig. 3.5(a) is 0.64 pu or 256 V. The reason for this small mismatch is that the output voltage \( V_o \) has been kept low to 350 V for safety reasons and so experimental value of \( V_{S2,peak} \) will be lower. Turn-on losses of \( S_I \) will be low due to reduced voltage. Turn-off losses are eliminated as switch is tuned off at negative voltage. Fig. 5.5 shows the switching waveforms of \( S_I \) on a larger time scale.

Fig. 5.6 and Fig. 5.7 show the turn-on and turn-off of \( S_I \) under reduced load of 200 W. It is seen from these figs. that turn-on of S1 is still under ZVS but the turn-off is at slightly higher voltage than that under full load as shown in Fig. 5.3. This means that turn-off of \( S_I \) depends on the input current and therefore at low load conditions or near zero crossing of the input ac wave where input current is lesser, the turn-off will become more and more lossy.
Fig. 5.1 Experimental Setup for obtaining the Switching Waveforms of the proposed Converter.

Table 5.1 Components Used in the Design Prototype.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant Inductor $L_r$</td>
<td>6 $\mu$H (Self wound)</td>
</tr>
<tr>
<td>Resonant capacitor $C_r$</td>
<td>15 nF (Vishay)</td>
</tr>
<tr>
<td>Capacitor $C_b$</td>
<td>3.5 nF (Vishay)</td>
</tr>
<tr>
<td>Switches $S_1, S_2$</td>
<td>IRFP840 (International Rectifier)</td>
</tr>
<tr>
<td>Boost diode $D_1$</td>
<td>HFA08TB60 (International Rectifier)</td>
</tr>
<tr>
<td>Auxiliary diodes $D_2$-$D_5$</td>
<td>MUR1540 (Motorola)</td>
</tr>
<tr>
<td>Boost Inductor $L_{in}$</td>
<td>1050 $\mu$H (wound on Magnetics Kool-Mu 77716A7 core)</td>
</tr>
<tr>
<td>Output Capacitor $C_o$</td>
<td>470 $\mu$F (Nippon Chemi-Con)</td>
</tr>
</tbody>
</table>
Fig. 5.2 Switching waveforms of the main switch $S_1$ at turn-on for $V_{in}=127\text{V},$

$$V_o = 350 \text{ V}, \ P_o = 250 \text{ W}, \ F_{sw} = 100\text{kHz}.$$ 

Fig. 5.4 Switching waveforms of main switch $S_1$ at turn-off for $V_{in}=127\text{V},$

$$V_o = 350 \text{ V}, \ P_o = 250 \text{ W}, \ F_{sw} = 100\text{kHz}.$$ 

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Fig. 5.5 Auxiliary switch $S_2$ voltage and current waveforms at turn-on and
turn-off for $V_{in}=127\, V$, $V_o = 3.50\, V$, $P_0 = 250\, W$, $F_{sw} = 100\, kHz$.

Fig. 5.6 Switching waveforms of main switch $S_1$ on a larger time scale for
$V_{in}=127\, V$, $V_o = 350\, V$, $P_0 = 250\, W$, $F_{sw} = 100\, kHz$. 

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Fig. 5.6 Switching waveforms of the main switch $S_1$ at turn-on for Output Power $P_0 = 200$ W.

Fig. 5.7 Switching waveforms of the main switch $S_1$ at turn-off for Power Output $P_0 = 200$ W.
Fig. 5.9 Simulated waveforms of the main switch $S_1$ showing switch current $I_{S1}$ and voltage $V_{S1}$ (upper waveform) and gating $V_{S1,\text{gat}}$ for $V_{\text{in}}$=127 V, $V_o$ =350 V, $P_o$ = 250 W, $F_{sw}$ = 100kHz.

Fig. 5.10 Simulated waveforms of the auxiliary switch $S_2$ showing switch current $I_{S2}$ and voltage $V_{S2}$ (upper waveform) and gating $V_{S2,\text{gat}}$ for $V_{\text{in}}$=127 V, $V_o$ =350 V, $P_o$ = 250 W, $F_{sw}$ = 100kHz.
Fig. 5.11 Turn-on of the main switch under (a) Hard switching (b) Soft switching.

Fig. 5.12 Turn-off of the main switch under (a) Hard switching (b) Soft switching
Fig. 5.10 (a) and Fig. 5.10 (b) shows the turn-on of main switch $S_t$ under hard switching and soft switching respectively. Fig. 5.11 (a) and Fig. 5.11 (b) show the turn-off of $S_t$ under hard switching and soft switching conditions respectively. From both the figures it is seen that the instantaneous power loss during these switch transitions is lower under soft-switching than under hard switching because the area under the current and voltage waveforms in soft-switching is lesser than the area under hard-switching. Thus the efficiency of the converter will be more.

There is some ringing in the switching waveforms of switch $S_2$. This is because the ant-parallel diode $D_3$ is not ideal and for the reverse recovery duration it conducts the resonant current in the reverse direction. As soon as it recovers reverse blocking capability the current across resonant inductor $L_r$ is abruptly terminated resulting in a large voltage spike across $S_2$.

From these experimental results the advantages of this converter can easily be seen. The only disadvantage is that turn-off of switch $S_t$ is dependent on input current also instead of on only the output voltage. This means that under reduced loads or near zero-crossings the soft turn-off of $S_t$ will be at higher voltages. This might not be a big disadvantage because at reduced input currents the rate of fall of switch $S_1$ current will be faster and so the overlap of higher switch voltage and lesser switch current will be smaller. This will lead to smaller losses.

The only reason for keeping the output voltage $V_o$ at 350 V instead of 400 V is because of safety considerations as the maximum voltage that can be measured by a probe in the experiment is 400 V only.
5.4 Conclusions

In this chapter design guidelines were laid down and a design example was presented for designing the proposed converter. Use was made of the characteristic curves presented in Section 2.5 and equations were developed in this chapter to assist in the selection of the component values of the converter.

From the design example a prototype was developed from which experimental results were taken. Simulation results were also presented. Both simulation and the experimental results verify that the main switch has ZVS at both turn-on and turn-off. The losses in auxiliary switch are also low. These results match the simulated results too and prove the validity of the design procedure used.

Experimental results in Mode 2 were not obtained as it is more difficult to have ZVS in Mode 1 than in Mode 2 as proved by the graphs of Chapter 3. So if the converter has ZVS in Mode 1 it will surely have ZVS in Mode 2 also.
CHAPTER 6

CONCLUSIONS

6.1 SUMMARY

This thesis proposed a new ac–dc power factor corrected ZVT converter as the first stage of the conventional two stage converter. The primary objective was to achieve a high efficiency for the boost stage by achieving ZVS turn-on and turn-off of the main switch and boost diode which leads to smaller losses and hence smaller heat sinks. This decreases the size and cost of this converter.

The basic principle of operation for this ZVS converter was explained and steady state analysis was performed. The steady state analysis was verified from analytical waveforms which match the simulated waveforms from Psim. The steady state analysis was then used to draw characteristic curves which give valuable insights into the working of the proposed converter and its design. Control theory for the PFC boost converter was explained and a proper voltage compensator and current compensator were designed. The characteristic curves were later used for designing an experimental prototype which was used to test the usefulness of the converter and verify the design procedure.
6.2 **Conclusions**

From this thesis it can be concluded that:

1. ZVS occurs for the main switch $S_t$ at that point on the input ac voltage wave where the ZVS turn-on interval is the least. At that point auxiliary switch $S_2$ has ZCS turn-on and ZVS turn-off. The boost diode $D_f$ also has a soft turn-off at that point.

2. From design curves it is apparent that in order to have a large ZVS interval the value of resonant impedance $Z_r$ should be low. Also to keep low voltage stress on the auxiliary switch low and at same time achieve a proper turn-off of main switch $S_t$ the value of $K = C_r/C_b$ should be less than 1. But the price paid is larger rms and peak currents in the auxiliary circuit which lead to increased losses. So a compromise must be made.

3. The converter should be designed for values of $K$ less than 1 and for low values of resonant impedance $Z_r$ as possible in order to ensure that the converter operates mostly in Mode 1, which is more efficient than Mode 2, for high input voltages.

4. By decreasing the value of variable $K = C_r/C_b$, the length of the ZVS interval can be increased but at the cost of increased voltage stress on the auxiliary switch $S_2$ and lesser ZVS turn-off of the main switch $S_t$.

5. The selection of the resonant inductor $L_r$ is based on the reverse recovery time $t_{rr}$ of the boost diode. This places a limit on the minimum length of the resonant cycle of the auxiliary circuit and by extension a limit on the switching frequency.

6. The optimum design of the converter is obtained by keeping the value of variable $K$ at 3 and selecting resonant impedance $Z_r$ in such a way as to achieve sufficient ZVS
turn-on interval. At this value of $K$ the main switch $S_1$ has a proper ZVS turn-off as well.

6.3 Suggestions for future work

In order to extend the work presented in this thesis the following topics can be examined:

(i) It was seen that there is a sharp voltage spike at the auxiliary switch $S_2$ because diode $D_3$ is not able to regain reverse blocking capability instantly. Ways of reducing this spike while keeping the auxiliary circuit simple would greatly improve reliability of the converter.

(ii) A limitation was imposed on how high the switching frequency of the converter can be extended due to the limitation of reverse recovery time $t_{rr}$ of the boost diode. By using better fabrication methods a better device might be produced which has a reduced reverse recovery time and this will improve the performance of the converter.

(iii) It can be examined whether the results of this thesis can be extended to three phase circuits as well.
REFERENCES


[33] Philip C. Todd, "UC3854 Controlled power factor Correction circuit design,"


