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The Design and Implementation of a C-band Dual-Transistor Power Amplifier

Jamal Abdou

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

For the Degree of Masters of Science in Electrical Engineering at

Concordia University

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Abstract

The Design and Implementation of A C-Band Dual Transistor Power Amplifier

Jamal Abdou. M.Sc.

Concordia University, 2002

Power amplifiers are at the heart of any high frequency communications network. Increasing the output power of amplifiers is conventionally carried out through 90-degree hybrids at frequencies above 3GHz and through 180-degree hybrids at lower frequencies. In this thesis, we go through the design, simulation, and prototype building and testing phases of a C-band, 47dBm solid-state microwave power amplifier and investigate its performance using the two types of hybrids. The device used is a Fujitsu device consisting of two independent transistors; each has a 10dB linear gain and a saturated output power of 44dBm. Three simulation packages were used in the design phase, ADS, a product of Hewlett-Packard, Zeland, a product of Zeland Software Inc, and Sonnet 6, a product of Sonnet Software Inc. The results of tests revealed that, when a 180-degree hybrid was used, the amplifier exhibited better performance in terms of output power, power-added efficiency, and inter-modulation distortion. However, the amplifier utilizing a 90-degree hybrid exhibited better return loss results. The design, simulation, and testing of the amplifier were carried out at Fujitsu FCSI under the guidance and appreciated help of the applications lab engineering team.

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Jamal Abdou

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CHAPTER I

Introduction and Review of Literature

1.1 Introduction

Microwave amplifiers are essential elements in a broad spectrum of microwave systems applications including space borne, airborne, and ground based satellite communications, terrestrial broadcast and telecommunications, radar and electronic warfare, together with a wide range of medical, scientific, and industrial instrumentation. In the past, microwave amplifiers generally used vacuum tubes as the amplifying devices or diodes in a negative resistance reflection- type circuit. Tube-based circuits were bulky, required high voltage power supplies and had a limited lifetime. On the other hand, diode-based circuits were noisy, had a narrow bandwidth, and required isolators to separate transmitted and reflected signals. Today, aside from high power applications where tubes are exclusively used, most microwave amplifiers use transistors as the basic active devices. Transistor amplifiers in their hybrid or monolithic form are rugged, low cost, and very reliable. Their small size and weight coupled with other advantages such as instant turn-on and long maintenance-free storage time make microwave transistor amplifiers ideal for commercial, military and space applications.

The design process of a microwave power amplifier goes through several stages and requires extensive modeling, simulation, and testing before the final product is ready for operation. After the transistor small signal and large signal parameters are extracted, input and output matching circuits are designed so that the transistor delivers maximum output power and maximum possible gain. The DC biasing of the transistors has to be

carried out through networks that allow the flow of DC power while blocking the microwave signal from getting coupled to the DC supply. Finally, depending on the application, more output power may be needed and outputs of several transistors might have to be combined. For that, splitting and combining stages are designed so that the individual output powers of the transistors are efficiently combined and delivered to the load.

This work utilizes a Fujitsu GaAs device to design and build a transistor amplifier and evaluate its performance when two types of combining networks are employed. The power amplifier is intended for terrestrial and satellite communications and has the following specifications:

1. Output power (Psat): 47dBm

2. Linear gain: 10 +/- 0.25dB

3. Power-Added Efficiency⁽¹⁾: 41%

4. IM3⁽²⁾: -33dBc at 37.4dBm carrier output power

The Fujitsu device consists of two independent transistors operating over a frequency band of 5.8-6.6GHz. Each transistor has a linear gain of 10dB and a saturated output power of 44dBm. The transistors were combined using a branch-line hybrid (balanced format) and a rat-race hybrid (push-pull format). Prototypes of individual hybrids and other passive networks were built and tested and the performance of each amplifier format was evaluated against the intended specifications. The simulation was carried out with three software packages, ADS, a product of Hewlett-Packard, Zeland, a product of

¹ Power added efficiency (P.A.E.) is defined as (Pout-Pin)/Pdc. Pout is the RF output power, Pin is the RF input power, Pdc is the supplied DC power.

² IM3 is the third order intermodulation product. It is measured as the difference in dBc between carrier power and the third order product power generated by the beating of two input signals $V(f_1)$ and $V(f_2)$.

Zeland Software Inc, and Sonnet 6, a product of Sonnet Software inc. The performance of each software package was evaluated against data collected from prototype testing.

1.2 Review of the literature

The development of C-band and higher frequency transistor power amplifiers may be attributed to two factors.

- a. The introduction of GaAs based transistors.
- b. The development of powerful computer simulation packages.

The early microwave transistors were silicon bipolar and were limited to a maximum operating frequency of 4GHz. However, the situation changed in the early 1970's with the advent of GaAs FET transistors with usable gain up to the X and Ku bands [1.1-1.2]. These were small signal devices but device designers were quick to realize their potential for power amplification and monolithic integration and soon after commercial MMIC's and discrete power GaAs FETs were commercially available. The wide utilization of GaAs FETs can be attributed to their high operating frequency and their versatility. GaAs semi-insulating substrates provide sufficient isolation up to 100GHz. This combined with a very high electron mobility (5 to 6 times that of silicon) allowed the development of transistor amplifiers with operating frequency up to 60GHz. The development of more powerful GaAs FETs faced several obstacles namely:

- 1. The high thermal resistivity of GaAs material.
- 2. The low break down voltage of the existing GaAs transistors.
- 3. The electrode layout of the parallel GaAs transistor cells.

In 1973, working independently, Fukuta et al [1.3] and Napoli et al. [1.4] tackled those problems and announced GaAs FETs of 0.4W and 0.8W at 4GHz respectively. The work of those two research teams had a major influence on the subsequent development and production of high power FETs to this day. Presently commercially available GaAs FETs deliver output power in excess of 50W at C band frequencies and 15W at Ku band frequencies.

The development of computer simulation packages had a profound influence on commercializing microwave products and allowed the proliferation of systems that were otherwise not feasible. The use of computer simulation cuts down on production costs by minimizing the laborious cut-and try methods and accounts for process and device variation through the implementation of yield analysis. There are two types of software tools, ones that are model-based and electromagnetic simulators. Model-based tools use derived models of microstrip structures and other waveguides to analyze microwave networks. Such tools have limitations based on the range of applicability of the utilized models. Model-based tools are usually incorporated into software packages that perform a variety of analysis and synthesis tasks. Among the most common packages are the ADS package, a product of HP, Microwave Office, a product of Applied Wave Research, and Serenade, a product of Ansoft. Electromagnetic simulators are relatively new and were made available because of the tremendous development in computing power. Such simulators treat microwave structures as boundary value problems and solve for currents and fields in the whole structure. Electromagnetic simulators are classified according to their ability to analyze complicated structures. 2D tools such as PCAAD, a product of Antenna Design Associates, examines single planar structures, 2.5D tools such as Sonnet,

a product of Sonnet Inc, examine multiple layered structures, and 3D tools such as HFSS, a product of HP, examine any arbitrary volume. The solution time of an EM solver is generally proportional to a factor between N² and N³, where N is the number of nodes in a Y-matrix form of the structure being modeled. Model-based simulation tools are considerably faster than most EM simulators although less accurate in most cases.

More powerful transistor amplifiers can be implemented by combining the powers of single transistors through the use of hybrids. The most common hybrid used for frequencies above 3 GHz is the 90- degree hybrid [1.5]. This type of hybrid combines the powers of two single transistors to achieve twice the output power. Amplifiers utilizing 90-degree hybrids are known to have good return loss and good stability. At lower frequencies, the most common type of hybrid used is the 180-degree hybrid. This hybrid also combines the output powers of two single transistors to achieve twice the output power. Amplifiers operating over a wide band and utilizing a 180-degree hybrid are known to have good efficiency and linearity. Interest was generated at Fujitsu FCSI as to how narrow band amplifiers with 180-degree hybrids would perform at high frequencies, namely in the 5.8-6.6GHz frequency range. This problem, to our knowledge has not been addressed in printed literature.

This thesis utilizes present day software tools and measurement technologies to design and build a microwave transistor power amplifier and evaluate its performance utilizing two types of hybrids, the 90-degree hybrid, and the 180-degree hybrid. Model-based software tools and electromagnetic simulators will be used to design the microstrip passive networks. The parameters of the transistors will be extracted using Load-Pull measurement techniques and S parameter measurement tools. Prototypes of the amplifier

will be built and compared to initial specifications. Chapter II of the thesis discusses the design procedure and characteristics of the passive networks involved. The design procedure for hybrids is presented and the performance of four different hybrids is evaluated over the design bandwidth. The effects of network losses and mismatches on the performance of hybrids are studied in detail. The chapter concludes with the design guidelines for DC injection networks. Chapter III presents the measurement procedures for the extraction of small-signal and large signal device models namely the S parameter extraction setup and the Load pull setup. The stability of the device is evaluated in terms of stability pointers that are functions of the extracted S parameters. The chapter concludes with practical limitation for design with microstrip environment and factors involved in the choice of microstrip substrates. In chapter IV, the evolution of computeraided design along with a brief introduction to each software package is presented. Simulation results are compared to measured data gathered from prototypes of passive networks and the 90-degree and the 180-degree amplifier formats. A discussion of the simulated and measured data is presented followed by a derivation of the uncertainty in power measurement. In Chapter V a conclusion is presented along with a discussion of future trends in solid-state power amplifier design.

CHAPTER II

Design of Passive networks

2.1 Introduction

Many applications require more power than is available from a single transistor. In this case, many transistors can be combined in parallel to achieve a specified output power. However, simply connecting transistors in parallel has its drawbacks. For example, the input and output RF impedance of a group of paralleled transistors is very small (less than one Ohm at the input) that designing matching networks is extremely difficult. Also, a group of parallel transistors does not exhibit graceful degradation and if one transistor fails, the whole amplifier fails. A better way of power combining is through the use of hybrids. Hybrids provide matching to the transistors and isolation between the individual amplifier stages. Figure 2.1 shows a two-transistor power amplifier block diagram using hybrids as splitters and combiners. A signal incident at the input port gets split into two equal-amplitude signals. The split signals get amplified by the transistors and then combined at the output port by the output combiner. The matching networks provide conditions for which each transistor delivers the maximum output power to the combiner stage and the DC network provides adequate DC supply to the transistor while acting as a low pass filter for RF signals. The phase of the split signals determines the amplifier type. A 180-degrees phase-difference split is referred to as Push-Pull architecture while a 90degrees split is referred to as balanced architecture. The two architectures have their special characteristics regarding frequency response and operating bandwidth.

This chapter discusses the design theory of hybrids and the DC injection circuits. Four types of hybrids are studied, namely:

- 1. The two-branch hybrid.
- 2. The broad-banded two-branch hybrid.
- 3. The three-branch hybrid.
- 4. The rat-race hybrid.

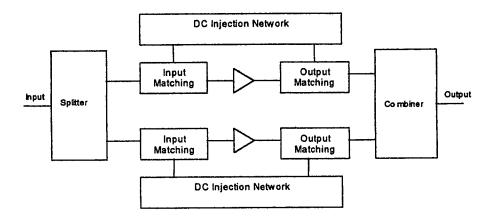


Figure 2.1 Block diagram of a two-transistor power amplifier.

The discussion begins with a definition of the matrix representation of networks in general and couplers in particular. The even-odd analysis method is then introduced and used to analyze the performance of the hybrids used in this work. The effects of network imperfections such as mismatch, loss, and phase and amplitude imbalance on the parameters of a hybrid are discussed afterwards. Finally, DC injection circuit design is addressed and the minimum allowable width of a microstrip line as a function of current is defined.

The transmission medium used in this work is microstrip. This medium lends itself well to designs using transistors and other surface-mount components. The analysis procedure assumes that the modes of propagation along the microstrip lines are quasi TEM and no

dispersion effects occur in the design bandwidth. The ratio of wavelength to line size is assumed to be large enough so that junction effects and discontinuities have negligible effect on the design problem. These approximations simplify the design procedure and serve as a good starting point for computer simulation.

2.2 Matrix representation of networks

Linear networks may be fully characterized by a variety of matrix representations. In this work, the normalized *ABCD* matrix representation, and the scattering matrix representations will be utilized.

The normalized ABCD matrix is useful for the analysis of two-port networks. It relates input and output quantities by the following relationship:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A & B & V_2 \\ C & D & I_2 \end{vmatrix}$$
 (2.1)

where V_1 and I_2 are the phasor voltage and phasor current at the input port, and V_2 and I_2 are the phasor voltage and phasor current at the output port. The "B" and "C" elements of the matrix are normalized to reference characteristic impedance. When the linear network is passive and reciprocal the following condition is true:

$$AD-BC=1 (2.2)$$

Furthermore, when the network is symmetric then:

$$A = D \tag{2.3}$$

One of the advantages of this matrix representation is that in a cascade of various networks, the normalized *ABCD* matrix of the cascade may be determined by multiplying the matrices of the individual networks. Another advantage is that when the output port is terminated with an impedance equal to the reference characteristic impedance, the input

reflection coefficient Γ and the transmission coefficient T may be simply expressed by [2.1]:

$$\Gamma = \frac{A+B-C-D}{A+B+C+D} \tag{2.4}$$

$$T = \frac{2}{A + B + C + D} \tag{2.5}$$

Equation (2.4) can be used to establish the requirement for a network matched at both ports. Setting Γ =0 results in:

$$A+B = C+D (2.6)$$

For symmetrical networks, equation (2.6) reduces to:

$$B = C (2.7)$$

Table 2.1 lists the ABCD matrix elements of some basic two-port Networks.

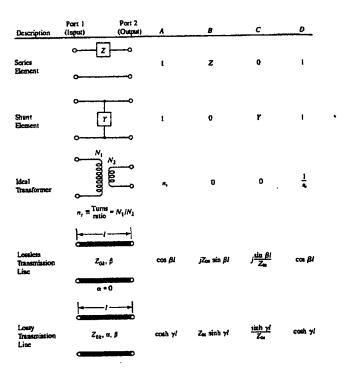


Table 2.1 The ABCD representations of some basic two-port networks (Reprinted from [2.0]).

The scattering matrix S is a useful representation for studying multi-port microwave networks. It relates incident and scattered waves at the various ports of the network. S parameters can easily be measured and do not require undesirable load terminations like a short circuit or an open circuit that may damage the network under test. For a four-port network, the incident and scattered waves are related by the following equation:

$$\begin{vmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{vmatrix} = \begin{vmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{333} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{vmatrix} a_1$$
(2.8)

where a_i and b_i are defined as:

$$a_{i} = V^{+} / \sqrt{Z_{oi}} = I^{+} \sqrt{Z_{oi}}$$

$$b_{i} = V^{-} / \sqrt{Z_{oi}} = I^{-} \sqrt{Z_{oi}}$$
(2.9)

 V^{\dagger} , and V are the forward and reverse voltage waves. I^{\dagger} and I are the forward and reverse current waves. Z_{0i} is the characteristic impedance of the transmission line at the ith port.

Network characteristics impose constraints on S matrix elements. When a network is lossless, the following relationships are true [2.1]:

$$\sum_{n=1}^{N} S_{np} S_{np}^{*} = 1$$

$$\sum_{n=1}^{N} S_{np} S_{nq}^{*} = 0$$
(2.10)

Furthermore, when the network is reciprocal, then

$$S=S^{T} \tag{2.11}$$

2.3 General characteristics of directional couplers

Directional couplers are passive networks used for power sampling and power splitting and combining applications [2.2]. Referring to Figure 2.2, power incident on port 1 (the input port) of a coupler is coupled to port 3 (the coupled port). The remainder of the power is delivered to port 2 (the thru port) and no power leaves out of port 4 (the decoupled port). The numbering of the ports is by no means standard and different texts use different numbering procedures. However, in this work, the port numbering of Figure 2.2 will be adopted.

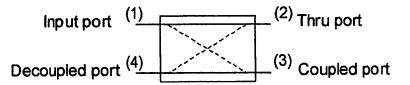


Figure 2.2 A four-port directional coupler.

Using a scattering matrix representation, a directional coupler may be characterized in terms of four parameters:

• The coupling factor C defined by:

$$C = 20Log |1 / S_{31}| (2.12)$$

C is a measure of how much of the input wave is being sampled.

• Isolation I defined by:

$$I = 20Log |1/S_{41}| (2.13)$$

I is a measure of how much of the input wave is leaking out of the decoupled port

• Insertion loss *IL* defined by:

$$IL = 20Log |1/S_{2l}|$$
 (2.14)

Insertion loss is a measure of the loss suffered by the wave in traveling from port 1 to port 2.

• Return loss *RL* defined by:

$$RL = 20Log |1/S_{II}|$$
 (2.15)

RL measures the degree of mismatch of a coupler.

Ideally *RL*, and *I* are infinite, but mismatches and network losses limits the maximum values that could be achieved.

Applying the conditions of losslessness and reciprocity given by equations (2.10) and (2.11), the S matrix of a directional coupler reduces to:

$$S = \begin{vmatrix} 0 & \alpha & \beta e^{j\phi_1} & 0 \\ \alpha & 0 & 0 & \beta e^{j\phi_2} \\ \beta e^{j\phi_1} & 0 & 0 & \alpha \\ 0 & \beta e^{j\phi_2} & \alpha & 0 \end{vmatrix}$$
 (2.16)

where α , β , ϕ_1 , and ϕ_2 are real numbers constrained by the following relationship:

$$\alpha^2 + \beta^2 = 1 \tag{2.17}$$

$$\phi_1 + \phi_2 = \pi \pm 2k\pi \tag{2.18}$$

(n is an integer).

A hybrid is a special case of a directional coupler where $\alpha = \beta = 1/\sqrt{2}$. A wave incident on port 1 of a hybrid is split into two waves of equal amplitude at ports 2 and 3; the phase difference between those two waves is ϕ_l and port 4 is completely decoupled. There are two classes of hybrids, the quadrature hybrid where the waves exiting ports 2 and 3 are 90 degrees out of phase ($\phi_l = \phi_2 = \pi/2$). Branch-line hybrids are examples of this class. The other type is the 180-degree hybrid where the waves exiting ports 2 and 3 are 180 degrees out of phase ($\phi_l = 0$, $\phi_z = \pi$). Rat-race hybrids are examples of this class. Hybrids

are widely used in microwave mixer and amplifier networks. They find use as phase shifters, amplitude attenuators, and antenna feed systems. In this work, hybrids will be used as power splitters and power combiners in the microwave amplifier network.

2.4 Even-odd mode analysis method

Introduced by Wheeler and Reed [2.3], the even-odd mode analysis presents a simple way of analyzing linear symmetrical networks in general and directional couplers in particular. Referring to Figure 2.3, a wave of amplitude a_I and phase angle φ incident on port 1 of a symmetrical network may be expressed in terms of sets of even and odd waves, each of amplitude $a_I/2$ and phase angle φ , incident on ports 1 and 4. Since the network is linear, the response due to a_I is the superposition of the responses due to the two sets of waves. For the even mode pair, a voltage maximum and current zero occurs at all points along the line of symmetry (indicated by the dashed line) which is equivalent to an open circuit. For the odd mode pair, a voltage zero and current maximum occurs along the line of symmetry, which is equivalent to a short circuit. For a given mode pair, the transmission and reflection characteristics of the top and bottom halves of the symmetrical four port network are the same, and the problem reduces to analyzing the corresponding 2-port network as shown in Figure 2.4.

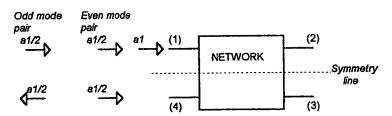


Figure 2.3 A wave incident on port 1 of a four-port symmetrical network and its equivalent evenodd mode pair.

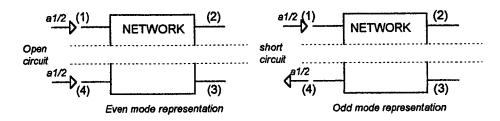


Figure 2.4 Even and odd mode representations of the network.

The exiting waves out of each port can be expressed in terms of even and odd transmission and reflection coefficients as:

$$b_1 = (\Gamma_e + \Gamma_o)a_1/2 \tag{2.19}$$

$$b_2 = (T_e + T_o)a_1 / 2 (2.20)$$

$$b_3 = (T_e - T_o)a_1 / 2 (2.21)$$

$$b_4 = (\Gamma_e - \Gamma_o)a_1 / 2 \tag{2.22}$$

Where Γ_e , and Γ_o are the even and odd mode reflection coefficients respectively. T_e , and T_o are the even and odd transmission coefficients.

Setting Γ_e and Γ_o in equation (2.19) and equation (2.22) equal to zero respectively, port 1 is matched and port 4 is decoupled; due to network symmetry, this means that all ports are matched and port 3 is decoupled when the hybrid is fed at port 2. The even and odd reflection coefficients can be forced to zero by applying equation (2.7) to the *ABCD* matrices of the even and odd two port networks.

In summary, four steps are needed to characterize a linear symmetrical four-port, matched network:

- 1. Find the ABCD matrices of the even and odd two-port networks.
- 2. Apply the condition of matched and decoupled ports (equation (2.7)).
- 3. Determine the transmission coefficients (equation (2.5)).

4. Determine the waves leaving ports 2 and 3 of the network (equations (2.19-2.22)).

2.5 Two-branch hybrid

Figure 2.5 shows the schematic of a two-branch hybrid. The series arm consists of a transmission line of length l, propagation constant γ , and characteristic admittance Y_s , The branch arm consists of a transmission line of length l, propagation constant γ , and characteristic admittance Y_p . The admittances of the arms are normalized to 50 Ohm. The length l is quarter wavelength at the design frequency.

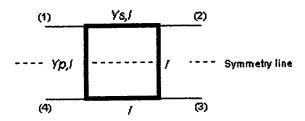


Figure 2.5 A schematic of a two-branch hybrid.

Using the analysis procedure described in section (2.4), the 4-port symmetrical network is transformed into two sets of 2-port networks. The even mode 2-port network consists of two open circuited stubs of length l/2 separated by a transmission line of length l (Figure 2.6-a), and the odd mode 2-port network consists of two short-circuited stubs of length l/2 separated by a transmission line of length l (Figure 2.6-b).

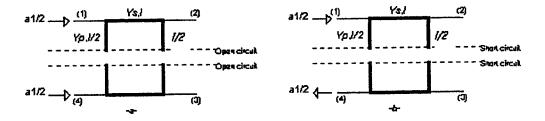


Figure 2.6 a) The even mode two-branch network b) The odd mode two-branch network.

Using Table 2.1, The ABCD matrices of the even and odd networks are given by:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & 0 \\ Y_{p}(\tanh \frac{1}{2})^{\pm 1} & 1 \end{vmatrix} \begin{vmatrix} \cosh \mu & \frac{1}{Y_{s}} \sinh \mu \\ Y_{s} \sinh \mu & \cosh \mu \end{vmatrix} \begin{vmatrix} 1 & 0 \\ Y_{p}(\tanh \frac{1}{2})^{\pm 1} & 1 \end{vmatrix}$$
(2.23)

where the upper sign is for the even mode solution and the lower sign is for the odd mode solution. At the design frequency and assuming lossless transmission lines, the ABCD matrices reduce to:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} \mp Y_p / Y_s & j / Y_s \\ j (Y_s - Y_p^2 / Y_s) & \mp Y_p / Y_s \end{vmatrix}$$
 (2.24)

Perfect matching and isolation results in the following constraint on Y_s and Y_p :

$$Y_s^2 - Y_n^2 = 1 (2.25)$$

Using equation (2.5), the even and odd transmission coefficients are given by:

$$T_e = \frac{-Y_s}{j - Y_p} \tag{2.26}$$

$$T_o = \frac{-Y_s}{j + Y_p} \tag{2.27}$$

Finally, using equations (2.20-2.21) the waves exiting ports 2 and 3 can be written as:

$$b_2 = -(j/Y_s)a_1 \tag{2.28}$$

$$b_3 = -(Y_p/Y_s)a_1 \tag{2.29}$$

A choice of $Y_p=1$, and $Y_s=\sqrt{2}$ results in a 3-dB hybrid with equal power split. The S matrix of a quadrature hybrid may now be written as:

$$S = \frac{-1}{\sqrt{2}} \begin{vmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{vmatrix}$$
 (2.30)

As we move away from the design frequency, the hybrid characteristics change and this might limit the usable bandwidth. A Matlab program was developed to plot the variation of the hybrid parameters with frequency. The plot of Figure 2.7-a reveals that for a minimum isolation and return loss of 20dB, the usable bandwidth of a two-branch hybrid is about 10%. Assuming lossy transmission lines, Figure 2.7-b confirms that the split in power at the output ports is not affected [2.5] while the isolation and return loss are degraded.

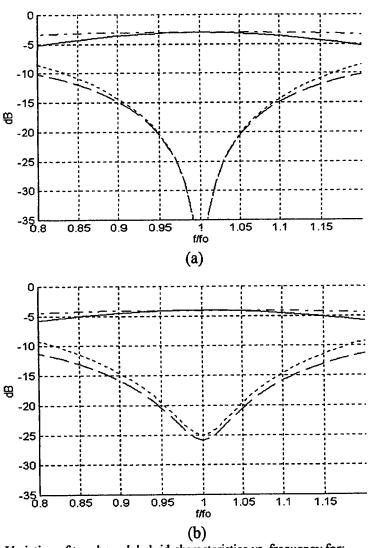


Figure 2.7 Variation of two-branch hybrid characteristics vs. frequency for: a) $\alpha l = 0$, b) $\alpha l = .05$ Np. S_{11} (dotted), S_{21} (solid, S_{31} (dash-dotted), S_{41} (dashed), S_{01} is the design frequency.

2.6 Broad-banded two-branch hybrid

At the design frequency, the coupling of a quadrature hybrid is given by the ratio of the admittances of the series and parallel branches (equation (2.29)). This coupling value is true whenever the ports are matched irrespective of the frequency. Therefore, if networks were designed to match the four ports at a set of frequencies, the coupling will be the same at all those frequencies. This property was used by Riblet to obtain hybrids with very flat coupling (<0.01dB) over a bandwidth of 12.5% [2.4]. Other authors used the same property to improve the bandwidth of the two-branch hybrid and reported an operating bandwidth of 40% [2.5]. Figure 2.8 shows a schematic of a two-branch hybrid matched at the ports by identical networks. The transmission lines are assumed lossless with electrical length βl , where β is the wave number of the microstrip line.

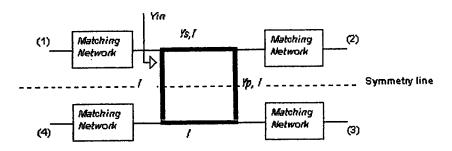


Figure 2.8 Schematic of a quadrature hybrid with identical matching networks connected to the four ports.

For $\beta l \approx \pi/2$, the input admittance Y_{in} is approximated by:

$$Y_{in} = \frac{1}{\sin \beta l} - j\left(1 + \sqrt{2}\right)\cot \beta l \tag{2.31}$$

This type of load can be broad-banded by a transmission line of length l and characteristic admittance Y_l shunted by an open-circuited stub of length 2l and normalized characteristic admittance Y_2 [2.6]. This matching network results in the

hybrid being matched at two frequencies corresponding to electrical lengths βl and π - βl respectively. Y_1, Y_2 , and l may be determined from the following equations [2.4]:

$$\frac{\left(t^4 + t^2\right)Y_1^2}{\left(Y_1Y_2 - Y_1^2t^2\right) + t^2\left(Y_1 + Y_2\right)^2} = \frac{1}{\sqrt{1 + t^2}}$$
(2.32)

$$\frac{t^{3}(Y_{1}+Y_{2})+tY_{1}(Y_{1}Y_{2}-Y_{1}t^{2})}{(Y_{1}Y_{2}-Y_{1}^{2}t^{2})+t^{2}(Y_{1}+Y_{2})^{2}}=-\frac{1+\sqrt{2}}{t}$$
(2.33)

$$\beta l = \cos^{-1}\left(\sqrt{\frac{1}{2}}\cos\left(\frac{\pi}{2}\left(1 - \Delta f/4f_0\right)\right)\right)$$
 (2.34)

 $t = \tan(\beta l)$, $\Delta f/f_o$ is the required bandwidth.

Since the symmetry of the network was not violated, the even-odd method can be used to determine the frequency variation of network characteristics. Figure 2.9 shows the variation of hybrid characteristics with frequency. The hybrid parameters were optimized for an operating bandwidth of about 20%.

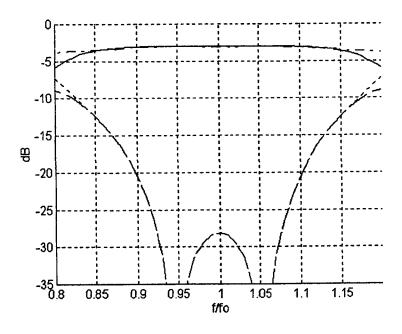


Figure 2.9 Variation of the characteristics of broad-banded hybrid vs. frequency for $Y_1 = 1.04$, $Y_2 = 2$. S_{11} (dotted), S_{21} (solid, S_{31} (dash-dotted), S_{4} (dashed), S_{0} is the design frequency.

2.7 Three-branch hybrid

Another way of broad-banding a quadrature hybrid is by adding more sections. Hybrids with up to five branches were analyzed by Wheeler and Reed [2.3], and synthesis techniques for couplers with up two nine branches were presented by Levy and Lind [2.7]. However, for microstrip networks, it is difficult to realize hybrids with more than three branches due to the limitations on the characteristic impedances that could be achieved. Several three-branch versions are possible, but the broadest band version is the one described by Wheeler and Reed [2.3] and presented in this work.

The schematic of a three-branch hybrid is presented in Figure 2.10-a. The normalized admittance of the outer branches is Y_{pl} and that of the inner branch is Y_p . The normalized admittances of the series branches are Y_s . All sections are quarter-wavelength long at the design frequency. The even and odd networks consist of a cascade of stubs and transmission lines. The stubs are open-circuited for the even mode and short-circuited for the odd mode. Using Table 2.1, the respective *ABCD* matrices are given by:

$$[ABCD] = M_{sl}M_lM_sM_lM_{sl} (2.35)$$

where:

$$M_{s1} = \begin{vmatrix} 1 & 0 \\ Y_{p1} \left(\tanh(\gamma l/2) \right)^{\pm 1} & 1 \end{vmatrix}$$

$$M_{I} = \begin{vmatrix} \cosh \gamma I & \frac{1}{Y_{s}} \sinh \gamma I \\ Y_{s} \sinh \gamma I & \cosh \gamma I \end{vmatrix}$$

$$M_s = \begin{vmatrix} 1 & 0 \\ Y_p(\tanh(1/2))^{\pm 1} & 1 \end{vmatrix}$$

where the upper sign is for the even mode solution and the lower sign is for the odd mode solution.

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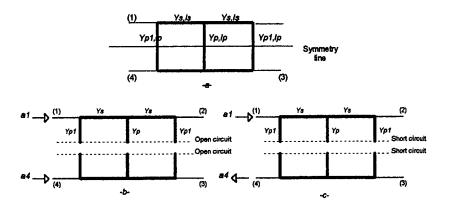


Figure 2.10

- a) Schematic of a three-branch hybrid.
- b) Even-mode equivalent.
- c) Odd-mode equivalent.

At the design frequency, The ABCD matrices reduce to:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} Y_{p1}Y_{p}/Y_{s}^{2} - 1 & \mp jY_{p}/Y_{s}^{2} \\ \mp j(2Y_{p1} - Y_{p1}^{2}Y_{p}/Y_{s}^{2}) & Y_{p1}Y_{p}/Y_{s}^{2} - 1 \end{vmatrix}$$
(2.36)

The condition for perfect matching and isolation given by equation (2.7), results in:

$$Y_{p} = \frac{2Y_{p1}Y_{s}^{2}}{1 + Y_{p1}^{2}} \tag{2.37}$$

Using equations (2.5) and (2.37), the even and odd transmission coefficients are given by:

$$T_e = \frac{1 + Y_{pl}^2}{Y_{pl}^2 - 1 - j2Y_{pl}} \tag{2.38}$$

$$T_o = \frac{1 + Y_{\rho 1}^2}{Y_{\rho 1}^2 - 1 + j2Y_{\rho 1}} \tag{2.39}$$

Using equations (2.20-2.21), the waves exiting ports 2 and 3 are given by:

$$b_2 = \left(\frac{Y_{pl}^4 - 1}{(Y_{pl}^2 - 1)^2 + 4Y_{pl}^2}\right) a_1 \tag{2.40}$$

$$b_3 = j \left(\frac{2Y_{P1}(1 + Y_{P1}^2)}{(Y_{P1}^2 - 1)^2 + 4Y_{P1}^2} \right) a_1$$
 (2.41)

A choice of $Y_p = \sqrt{2}$, and $Y_s = \sqrt{2}$, and $Y_{pl} = \sqrt{2} - 1$ results in a 3-dB hybrid with equal power split at the output ports.

Figure 2.11 shows the variation of the hybrid characteristics vs. frequency normalized to the design frequency f_o for the case of a lossless network. The plot shows that the usable bandwidth of a 3 dB branch line hybrid is about 30%.

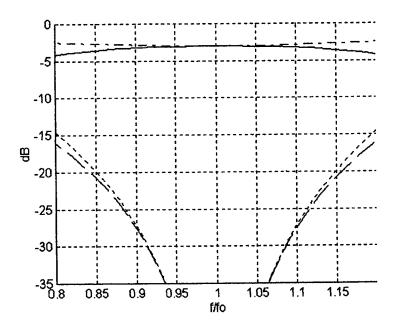


Figure 2.11 Variation of three-branch hybrid characteristics vs. frequency. S_{11} (dotted), S_{21} (solid, S_{31} (dash-dotted), S_{41} (dashed), f_0 is the design frequency.

2.8 Rat-race Hybrid

The schematic of a microstrip rat-race hybrid is shown in Figure 2.12. Unlike the quadrature hybrids, the rat-race hybrid possesses lateral symmetry only and the even and

odd pairs of waves have to be fed through ports 1 and 3 instead of 1 and 4. The normalized characteristic admittance Y_s of the circular transmission line is normalized to 50 ohm, and l is quarter wavelength long at the design frequency. The even and odd ABCD matrices are given by:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & 1 & 0 \\ Y_s \left(\tanh\left(\frac{3}{2}\mathcal{H}\right) \right)^{\pm i} & 1 \begin{vmatrix} \cosh \mathcal{H} & \frac{1}{Y_s} \sinh \mathcal{H} \\ Y_s \sinh \mathcal{H} & \cosh \mathcal{H} \end{vmatrix} \begin{vmatrix} 1 & 0 \\ Y_s \left(\tanh\left(\frac{\mathcal{H}}{2}\right) \right)^{\pm i} & 1 \end{vmatrix}$$
(2.42)

where the upper sign is for the even mode solution and the lower sign is for the odd mode solution.

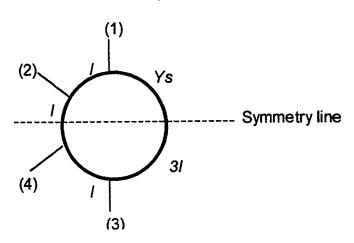


Figure 2.12 The schematic of a rat-race hybrid. The normalized characteristic admittance of the circular transmission line is Y_s . The length I is quarter wavelength long at the design frequency.

At the design frequency, equation (2.42) reduces to:

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} \mp 1 & \frac{j}{Y_s} \\ 2jY_s & 1 \end{vmatrix}$$
 (2.43)

The condition of perfect matching and isolation given by equation (2.7) results in $Y_s = 1/\sqrt{2}$. Substituting the value of the normalized characteristic impedance in the ABCD

matrices and using equations (2.4-2.7), the even and odd reflection and transmission coefficients can be written as:

$$\Gamma_{\rm e} = j/\sqrt{2} \tag{2.44}$$

$$T_{\rm e} = -j/\sqrt{2} \tag{2.45}$$

$$\Gamma_{\rm o} = -j/\sqrt{2} \tag{2.46}$$

$$T_{o} = -j/\sqrt{2} \tag{2.47}$$

The scattered waves as given by equations (2.19-2.22) have to be modified because the sets of even and odd waves are now incident on ports 1 and 3 instead of at ports 1 and 4. The scattered waves for a rat-race are given by:

$$b_{I} = (\Gamma_{e} + \Gamma_{o})a_{I} / 2 = 0 \tag{2.48}$$

$$b_{2} = (T_{e} + T_{o})a_{1} / 2 = j / \sqrt{2} a_{1}$$
 (2.49)

$$b_{3} = (\Gamma_{e} - \Gamma_{o})a_{1} / 2 = -j / \sqrt{2} a_{1}$$
 (2.50)

$$b_{4} = (T_{e} - T_{o})a_{I} / 2 = 0 (2.51)$$

The waves out of ports 2 and 3 are equal in amplitude and 180 degrees out of phase. The S matrix of a rat-race hybrid may be written as:

$$S = \frac{-j}{\sqrt{2}} \begin{vmatrix} 0 & 1 & -1 & 0 \\ 1 & 0 & 0 & 1 \\ -1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{vmatrix}$$
 (2.52)

Figure 2.13-a shows the variation of hybrid characteristics vs. frequency. For a minimum isolation and return loss of 20dB, the usable bandwidth of a rat race hybrid is about 30%. Assuming lossy transmission line, Figure 2.13-b confirms that the split in power at the output ports is affected [2.8].

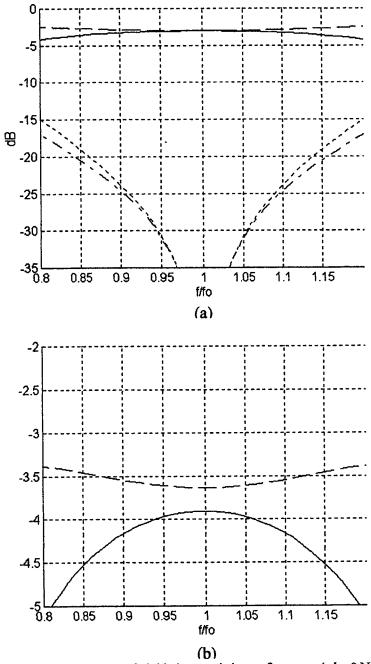


Figure 2.13

a) Variation of rat-race hybrid characteristics vs. frequency ($\alpha l = 0$ Np, $S_{11}(\text{dotted})$, $S_{21}(\text{solid}, S_{31}(\text{dash-dotted}), S_{41}(\text{dashed})$, f_0 is the design frequency).

b) Variation of S_{21} , and S_{31} vs. frequency for $\alpha l = 0.05$ Np ($S_{21}(\text{solid})$, $S_{31}(\text{dash-dotted})$. fo is the design frequency.

2.9 Effect of mismatches on hybrid parameters

Thus far, the ports of a hybrid were assumed to be perfectly matched. In reality this is not the case. Networks usually are designed to operate over a certain bandwidth and while the matching might be perfect at certain frequencies, it is not elsewhere in the band. In other applications, mismatch might be part of the design as in the case of amplitude attenuators.

The dependence of hybrid parameters on port reflections was presented in [2.9] and is repeated in Table 2.2 for reference.

Parameter	180 degree hybrid	90 degree hybrid
С	$20Log\left(\frac{\Phi_1}{\sqrt{2}(1+\Gamma_2)(1+\Gamma_2\Gamma_3)}\right)$	$20Log\left(\frac{\Phi_2}{\sqrt{2}(1+\Gamma_3)(1-\Gamma_2\Gamma_4)}\right)$
I	$20Log\left(\frac{\Phi_{1}}{(1+\Gamma_{4})(\Gamma_{3}-\Gamma_{2})}\right)$	$20Log\left(\frac{\Phi_2}{(1+\Gamma_4)(\Gamma_2+\Gamma_3)}\right)$
RL	$20Log\left(\frac{2\Gamma_{2}\Gamma_{3}\Gamma_{4}+\Gamma_{2}+\Gamma_{4}}{2+\Gamma_{4}\left(\Gamma_{3}+\Gamma_{2}\right)}\right)$	$20Log\left(\frac{2\Gamma_{2}\Gamma_{3}\Gamma_{4}+\Gamma_{2}-\Gamma_{3}}{2+\Gamma_{4}(\Gamma_{3}-\Gamma_{2})}\right)$
	$\Phi_1 = 2(1 + \Gamma_2 \Gamma_3 \Gamma_4) + (1 + \Gamma_3)(\Gamma_2 + \Gamma_4)$	$\Phi_1 = 2(1 + \Gamma_2 \Gamma_3 \Gamma_4) + (1 - \Gamma_4)(\Gamma_2 - \Gamma_3)$

Table 2.2 Hybrid characteristics in terms of port reflections (Γ_i is the reflection coefficient at the ith port).

Table 2.2 reveals that when hybrids serve as input stages to identical loads ($\Gamma_2 = \Gamma_3$) and assuming perfect termination at the decoupled port (($\Gamma_4 = 0$), the return loss of the quadrature hybrid remains ideal and is not affected while isolation is degraded. On the other hand the isolation of the 180-degree hybrid remains perfect while its return loss is degraded. For configurations where a 180-degree hybrid is used as a splitter, it is

customary to place an isolator at the input port to protect driving stages from damage.

Such an isolator is not needed when a quadrature hybrid is employed.

2.10 Effect of loss

Network losses place a constraint on the maximum return loss and isolation that could be attained [2.10 –2.11]. For small losses, and near the design frequency, the effect of loss on the hybrid parameters may be expressed as shown in Table 2.3. An interesting feature of quadrature hybrids is that although Isolation, and return loss decrease with losses, the power split between the ports 2 and 3 is not affected by transmission line losses. Such is not the case for 180-degree hybrids and we see that the power split at the output ports is a function of line losses. This is a consequence of the lateral and transverse symmetry of the quadrature hybrids.

Parameter	180-degreee Hybrid	Quadrature hybrid
IL	$20Log\left(\frac{6\sqrt{2}\alpha l+2}{4\alpha l+\sqrt{2}}\right)$	$3.01 + 20 Log(1 + 2.414\alpha l)$
С	$20Log\left(\frac{6\sqrt{2}\alpha l + 2}{3\alpha l + \sqrt{2}}\right)$	3.01 + 20Log(1 + 2.414\alphal)
I	$20Log\left(\frac{12\sqrt{2}\alpha l+4}{\sqrt{2}\alpha l}\right)$	$6.02 + 20Log\left(1 + \frac{0.414}{\alpha l}\right)$
RL	$\frac{\sqrt{2}\alpha l}{12\sqrt{2}\alpha l + 4}$	$\frac{2.41\alpha l}{2+4.83\alpha l}$

Table 2.3 Effect of network losses on parameters of quadrature and 180-degree hybrids

2.11 Effect of amplitude and phase imbalance

Amplitude and phase imbalance refer to the condition when a wave incident at port 1 of a hybrid no longer results in waves of equal amplitudes and proper phase difference (90 degrees for 90-degree hybrids or 180 degrees for 180-degree hybrids). This imbalance occurs when a hybrid is operated at a frequency different from the design frequency or it may be due to fabrication imperfections. When such a hybrid is used as a combiner, some of the power will be diverted away from the load and gets absorbed in the termination. The ratio of absorbed power P_3 to the total incident power P_T is given by:

$$\frac{P_3}{P_r}(dB) = 20Log|\sin(\delta/2)| \tag{2.53}$$

where, in the case of phase imbalance, δ is given by:

$$\delta = \left| \angle S_{12} - \angle S_{13} \right| - \pi/2 \text{ (Quadrature hybrid)}$$
 (2.54)

$$\delta = \left| \angle S_{12} - \angle S_{13} \right| - \pi \quad \text{(Rat race hybrid)}$$
 (2.55)

In case of amplitude imbalance:

$$\delta = 2 \left(\tan^{-1} \left(\left| \frac{S_{12}}{S_{13}} \right| \right) - \frac{\pi}{4} \right) \tag{2.56}$$

 S_{12} and S_{13} are **S** matrix elements of the hybrid.

Plots of equation (2.53) were developed for each imbalance type and shown in Figures 2.14-2.15. For a 10 degrees phase imbalance, the ratio of absorbed power to incident power is -21dB.

For a 1dB amplitude imbalance, the ratio is -25dB.

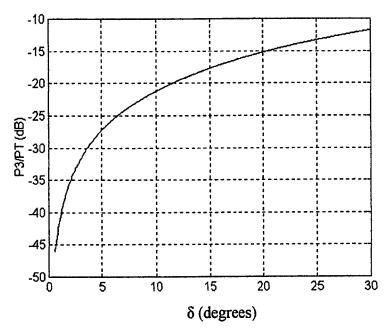


Figure 2.14 Variation of the power absorbed by the termination P_3 vs. phase imbalance.

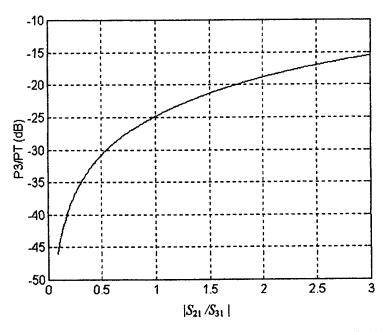


Figure 2.15 Variation of the power absorbed by the termination P_3 vs. amplitude imbalance (P_T is the total input incident power).

2.12 DC injection circuits

Besides their primary function as sources of DC control to active devices. DC injection circuits perform other tasks such as suppressing unwanted oscillations and filtering of harmonics and spurious signals. Figure 2.16-a shows a simple lumped-element version of a DC injection circuit. The capacitance of capacitor C is chosen such that it acts as a short circuit at the design frequency and the inductance of inductor L is chosen such that it presents a very high RF impedance to incoming signals. As a result, an ideal DC injection circuit will not affect the RF performance of the network. However, unwanted parallel resonance might occur between C and the inductance of the "DC-IN" feed lines. This resonance must be dampened otherwise the very high RF impedance created at plane A is transformed to a short circuit at plane B and the RF signal is reflected back. Figure 2.16b shows a distributed version of the DC-injection circuit that function similar to the lumped-element version. This version consists of a transmission line of characteristic impedance Z_{Ol} and length $l = \lambda/4$ at the design frequency shunted by an open-ended transmission line of characteristic impedance Z_{O2} and length $l=\lambda/4$ at the design frequency. The RF impedance at plane A is given by:

$$Z_A = Z_{O2} / j \tan(\beta l) \tag{2.57}$$

 Z_A is zero at $l = \lambda/4$, and for $l < \lambda/4$, the Z_{O2} transmission line acts like the capacitor in the lumped-element version. To insure that Z_A remains small over the design bandwidth, Z_{O2} is chosen to be as small as possible. The function of the Z_{O1} transmission line is to transform the RF impedance seen at plane A to large impedance at plane B of the network. The RF impedance at plane B is approximately given by:

$$Z_B \approx j Z_{OI} \tan(\beta l) \tag{2.58}$$

At the design frequency, the impedance at plane B is infinite and The DC injection circuit does not affect the RF performance of the network. To insure that Z_B remains high over the operating bandwidth, the characteristic impedance Z_{OI} is chosen as high as physically possible. However, as stated in the lumped element version, parallel resonance might occur between the open-ended transmission line and the "DC-IN" feed lines. This happens when

$$L = Z_{O2}/\tan(\beta l) \tag{2.59}$$

L is the inductance of the "DC-IN" feed lines

Therefore, care should be taken in choosing the proper characteristic impedance values.

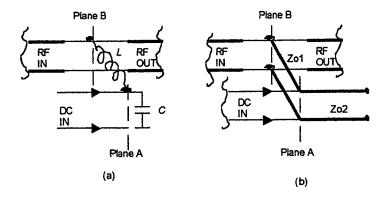


Figure 2.16 a) Lumped-element DC injection circuit. b) Distributed element DC injection circuit.

Common practice is to use a radial stub microstrip structure in place of the Z_{02} transmission line. The radial stub is favored because it has a well-defined input port that can be tailored to any dimension desired. Furthermore it has less physical length and operates over a larger bandwidth than regular low impedance microstrip resonators. The

radius of the stub is inversely proportional to the resonant frequency; for an arc angle of 60 degrees, the radius can be approximated by the following equation [2.12]:

$$LogR_2 = -0.8232 Log \sqrt{\varepsilon_r f_{res}} + 0.0572 Logh + 0.1169 LogR_1 - 0.8082$$
 (2.60)

 R_2 is the outer radius.

 $\epsilon_{\!r}$ is the relative dielectric constant of the substrate.

h is the height of the substrate.

 R_l is the defined as the radius subtending the straight-line chord of arc representing the intersection of the stub area with the connected transmission line.

This formula gives results within 1-2 % accuracy for $2 < \varepsilon_r < 15$ and $0.1 \text{GHz} < f_{res} < 30 \text{GHz}$. Figure 2.17 shows a typical DC injection circuit with shunting radial stub.

The Z_{OI} transmission line is physically narrow since the characteristic impedance of a microstrip line is inversely proportional to its physical width. Therefore, care has to be taken not to render the transmission line too narrow it cannot carry the required DC current. This is especially a concern for drain DC injection circuit where large DC currents are involved. For a certain DC current, a conservative estimate of the minimum width of a microstrip line is given by [2.13]:

$$w = \left(\sqrt{\frac{h}{\sigma_{elect}\sigma_{therm}t\Delta T}}\right)I \tag{2.61}$$

- ΔT is the maximum allowable temperature difference between the top and bottom of substrate (typically 100 degrees centigrade).
- σ_{therm} is the thermal conductivity of the substrate.
- $\sigma_{\rm elect}$ and t are the electrical conductivity and the thickness of the microstrip line.

- I is the current through the microstrip line.
- w is the minimum allowable width of the transmission line.
- h is the substrate thickness.

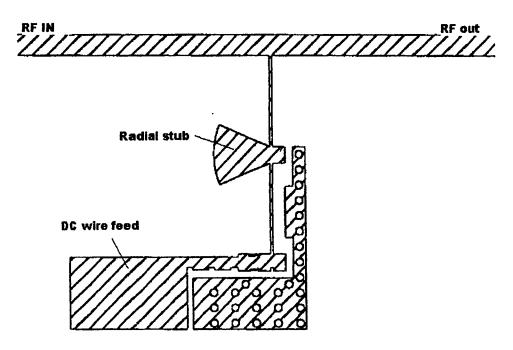


Figure 2.17 A typical DC injection microstrip structure connected in shunt to a 50-ohm transmission line. The small circles are plated-through via holes that provide ground connection from the back plane of the microstrip to the top surface.

CHAPTER III

Device Modeling and Stability Considerations

Internally matched transistors are high frequency devices that have built-in matching

3.1 Introduction

Microwave power transistors generally fall into two categories:

- 1. Internally matched transistors (IMFETs).
- 2. Partially matched transistors.

networks such that a transistor can be readily used in a 50-Ohm system. Partially matched transistors operate at lower frequencies where it is impractical to include all the matching networks in the device package. As a result, part of the matching networks is included in the device package and the rest is implemented outside the device. When partially matched devices are used in a power amplifier design, it is important to extract the device small-signal and large-signal models so that proper matching networks are designed. This chapter deals with the measurement of device parameters and the establishment of the small signal model and the large signal model. The small signal model consists of the measured S parameters of the transistor under small signal conditions. The model is important in studying stability over frequency and is instrumental in the design of the input-matching network. The large signal model consists of the measured input and output impedance of the transistor at which maximum power is delivered to the load. The large signal model is used to design the output-matching network. The extraction of the transistor parameters requires precise measurements and special calibration techniques to cancel the errors introduced by the measurement system.

The chapter begins with a presentation of the types of errors inherent in a microwave measurement setup and a description of two error correction procedures, the SOLT procedure and the TRL procedure. The large signal model is extracted using the load-pull measurement technique. A detailed explanation of this technique is provided along with the measurement setup used to collect the RF impedance data. The setup used to measure the S parameters of the transistor is presented and two stability factors that serve as indicators to the stability of the transistor at a given frequency are defined. The chapter concludes with a discussion of the operating frequency limitations of microstrip networks and the factors involved in choosing an appropriate substrate for the design.

3.2 Types of errors and error correction procedures

In a microwave measurement setup, there are measurement errors associated with the system that contribute uncertainty to the results. Parts of the measurement setup such as interconnecting cables and signal separation devices as well as the network analyzer itself introduce variations in magnitude and phase that can mask the actual performance of the device under test. Generally, errors can be subdivided into three categories [3.1]:

- Systematic errors.
- Random errors.
- Drift errors.

Systematic errors are caused by setup imperfections. They can be completely characterized through calibration and mathematically removed from the measurement process. Random errors are caused by noise inherent in the measurement system. While unpredictable, the effect of noise can be minimized by data averaging routines and by

reducing IF monitoring bandwidth of the measuring device. Drift errors are caused by the variation of the setup performance due to changes in temperature and humidity. Stabilizing the environment in which a measurement is carried out minimizes the effect of these errors.

Out of the various systematic-error-correction methods available, the ones that are relevant to this work are the SOLT method, and the TRL method. The SOLT (Short-Open-Load-Thru) correction procedure relies on the use of standard calibration loads to identify setup imperfections. Measurements of a short circuit load, an open circuit load, a 50-Ohm load, and a thru load (the ports of a network analyzer directly connected) are enough to identify and offset the systematic errors of a measurement setup. The accuracy of the SOLT procedure is a direct function of the quality of the standard loads. The SOLT procedure applies to coaxial media and can be used on scalar network analyzers, where phase cannot be measured, as well as on vector network analyzers. In this thesis the SOLT method will be used to evaluate the overall performance of the amplifier.

The TRL procedure [3.2] applies to coaxial and mixed transmission media. It is the method of choice to extract device characteristics because the effect of the device test fixture is eliminated and the measurement planes are the actual input and output of the device. The TRL (Thru-Reflect-Line) calibration procedure does not require high precision calibration loads to identify setup errors. All that is needed to identify system errors are the test fixture itself and a section of transmission line of known characteristic impedance. This line acts as the reference impedance for all subsequent measurements.

The accuracy of the TRL method is related to how well the characteristic impedance of the transmission line is known. This does not present a limitation because closed formulas are able to predict the characteristic impedance of transmission lines to a high degree of accuracy [3.3].

3.3 Load-pull method and the large signal model

One of the main objectives of a microwave power amplifier is to deliver the maximum RF power possible. This is usually achieved by designing the output-matching network to conjugate match the output impedance of the transistor. The problem is that the output impedance is a function of output power and it is difficult to predict the relationship for large signal applications. While S parameter characterization is satisfactory for small signal applications, it is useless for large signal applications and different characterization techniques are employed.

The load-pull method is one such technique. It was originally developed to match a varactor multiplier to a power transistor stage and later successfully applied to broadband optimization of transistor power amplifiers [3.4]. The basic idea of load-pull measurement consists of presenting known load and source impedance to a device under test at a given frequency and then performing several measurements to observe the performance of the device under a range of impedances. Such measurements consist of the associated input power, output power, reflection coefficients, and DC bias conditions. As source and load impedances are varied, device characteristics will vary accordingly. Measurements are made as a function of the input power levels and device termination. The impedances of the device terminations are the key variables in this type of measurement.

Figure 3.1 shows a basic block diagram of a load-pull system. It consists of the RF source, tuners, and the test fixture. A main computer controls the set up.

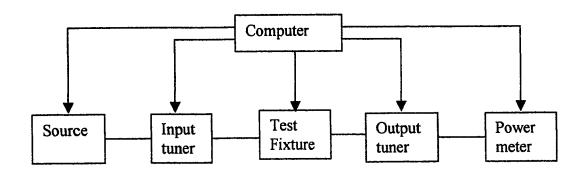


Figure 3.1 Block diagram of a load-pull system.

The basic block of the load-pull system is the tuner that presents the different impedances to the device under test. There are passive electromechanical tuners and active electronic tuners. The difference between the two types is in the way impedance is presented to a device and in the range of impedances possible. The tuner used in this work is the electromechanical tuner manufactured by Focus microwaves (model#1808). This tuner consists of a 50-ohm slab line, which has an open structure allowing the insertion of a small metallic slug. Figure 3.2 shows a schematic of the tuner. As the slug is inserted into the slotted line, a shunt reactance between the outer and inner conductors is created and the magnitude of the reflection coefficient Γ_{TUNER} observed looking into the tuner is varied with the insertion depth; increasing the insertion depth d of the slug increases Γ_{TUNER} . The phase of the reflection coefficient is adjusted by varying the length l_{PHASE} between the reflection coefficient reference plane and the slug. Computer controlled stepper motors allow for both horizontal and vertical movement of the slug thus insuring repeatability of the process.

The first commercial automatic load-pull system was designed and assembled at RCA David Sarnoff Research Laboratory in New Jersey in the mid seventies [3.5], Soon after a few other companies, such as Focus Microwaves and Maury Microwaves have also developed their own systems.

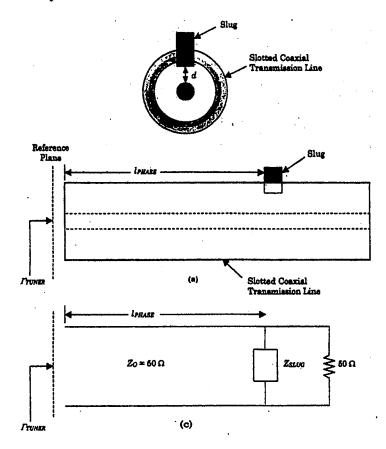


Figure 3.2 (a) Basic schematic of the mechanical tuner. (b) The equivalent circuit. (Reprinted from [3.5]).

Figure 3.3 shows a block diagram of the load pull measurement setup used. The maximum output power of the signal source is 20dBm and it is not enough to drive the device under test; an amplifier was introduced in the input circuit to boost the RF signal power. Isolators and attenuators are introduced at various points in the setup to insure that unwanted reflected power does not reach the power sensors (former) and to protect measurement meters (latter). Computer software developed by Focus microwaves

controls the setup using an HPIB interface system. TRL calibration was performed to account for all setup losses up to the device under test. The resultant optimum impedance data are listed in Table 3.1. The parts used in the setup are listed Table 3.2.

Freq (GHz)	Zin (Ohm)	Zout (Ohm)	Gain (dB)	Psat (dBm)	P.A.E.max (%)	IDRFmax (mA)
5.6	5.7 + j8.6	21.2 - j4.4	10.2	44.5	42	4488
5.7	4.7 + j11.6	20.1 - j3.6	10.4	44.8	45	4575
5.8	4.3 + j18.5	20.8 - j4.1	10.9	44.4	41	4488
5.9	3.9 + j13.9	21.3 - j3.6	11.2	44.8	49	4463
6.0	8.0 + j18.5	19.8 - j5.1	11.4	44.8	50	4325
6.1	9.3 + j17.1	16.7 - j6.6	10.9	44.8	51	4188
6.2	15.9 + j23.0	18.3 - j7.6	11.1	44.8	50	4100
6.3	18.2 + j25.4	14.8 - j7.2	11.6	44.6	47	4188
6.4	23.2 + j23.7	10.6 - j7.1	12.0	44.3	42	4750
6.5	20.9 + j22.4	10.2 - j9.1	11.7	44	39	4513
6.6	32.8 + j7.5	13.5 - j6.9	11.2	43.7		
6.7	41.8 + j12.9	9.3 - j3.7	11.4	44.8		

Table 3.1 Load-pull measured data (Zin and Zout are the input impedance and output impedance of the device. P_{SAT} is the maximum output power. I_{DRF} is the drain current at P_{SAT} . P.A.E. is power added efficiency.

C-Band 50W Load-Pull Evaluation Set-Up

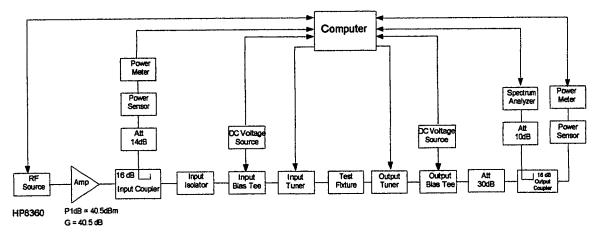


Figure 3.3 The load pull measurement setup.

Output Bias Tee	Hwelett Packard
•	30V/20A, 5BT-H1204, TO99014
re-Amplifier	Fujitsu FCSI
•	Model #:CG647110-51
nput Cable	Huber&Suhner Inc.
•	Sucoflex 104EA
	S/N 0076/4EA
nput Bias Tee	11590B Opt001
nput Isolator	Western Microwave
•	Model # 2JC-4082
	S/N 0562
nput Coupler	Krytar
•	Model # 1820
OdB Attenuator	Hwelett Packard
	S/N 2702A05986
Output Coupler	Narda
	Model #5292
Power meter	Anritsu
	Model #:ML2438A
Signal Source	Hwelett Packard
	Model # 8360A

Table 3.2 the components used in the load-pull setup and their manufacturers.

3.4 Transistor S parameters, stability, and matching circuit design considerations

Figure 3.4 shows the set up used to extract the S parameters of the transistor and plots of the magnitudes of the extracted parameters. Measurement was performed over a bandwidth of 0.1GHz - 8GHz.

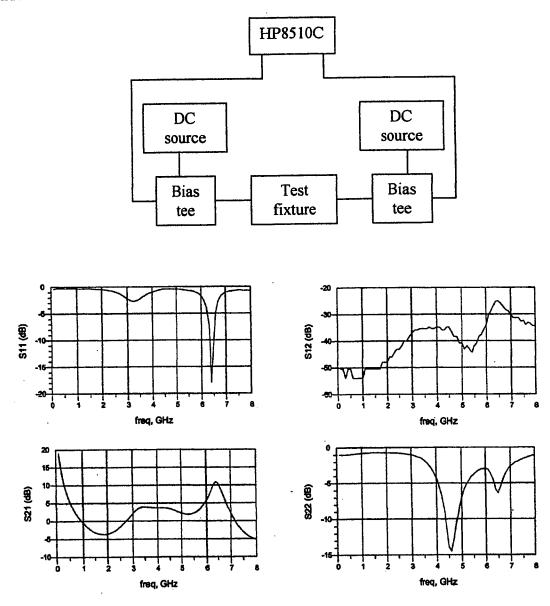


Figure 3.4 The measurement setup and the magnitudes of the measured S parameters of the Fujitsu transistor.

The stability of a transistor or its resistance to oscillate is an important design consideration and can be determined from the S parameters of the transistor, the matching

structures, and the termination. Referring to Figure 3.5, a transistor is said to be unconditionally stable at a given frequency if the real parts of Zin and Zout are greater than zero for all passive load and source impedances; Zin and Zout are the impedances at the input and output ports looking into the transistor. In terms of reflection coefficients, the conditions for unconditional stability at a given frequency can be stated as follows:

$$|\Gamma_{\mathcal{S}}| < 1 \tag{3.1}$$

$$|\Gamma_L| < 1 \tag{3.2}$$

$$\left|\Gamma_{IN}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1$$
 (3.3)

$$\left|\Gamma_{OUT}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{22}\Gamma_S}\right| < 1$$
 (3.4)

 Γ_S is the reflection coefficient at the device input port looking into the RF source.

 Γ_L is the reflection coefficient at the device output port looking into the load.

 $\Gamma_{I\!N}$ is the reflection coefficient at the device input port looking into the device.

 Γ_{OUT} is the reflection coefficient at the device output looking into the device.

 S_{11} , S_{12} , S_{21} , S_{22} are the **S** parameters of the network.

Algebraic manipulation of equations (3.1-3.4) results in two necessary and sufficient condition for unconditional stability given by [3.6]:

$$K = \frac{1 - \left| S_{11} \right|^2 - \left| S_{22} \right|^2 + \left| \Delta \right|^2}{2 \left| S_{12} S_{21} \right|} > 1 \tag{3.5}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{3.6}$$

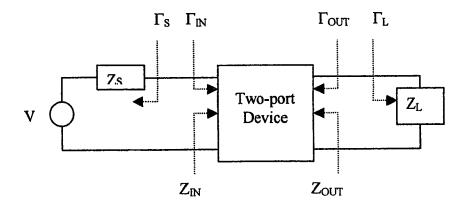


Figure 3.5 RF Impedance definitions of a two-port network connected to a source and a load.

The K and Δ factors of the Fujitsu transistor are plotted in Figure 3.6. The transistor is unconditionally stable everywhere in the band except for frequencies less than 750MHz where K is less than 1.

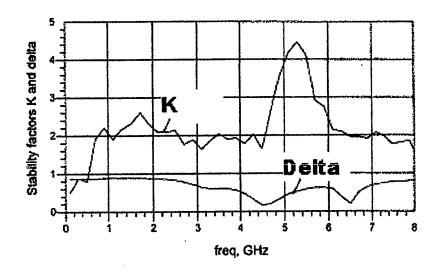


Figure 3.6 Plots of the K and Δ stability factors of the Fujitsu transistor.

The design of matching networks is tailored to the intended application of the amplifier. For front-end receivers, the matching networks are designed so that the overall amplifier contributes the minimum possible noise to the RF signal. In this work, power is the main concern; therefore, the optimum output matching circuit is the one that conjugate matches the load-pull data over the design bandwidth. Once the output matching circuit is

designed and connected to the device, the *S* parameter data of the device are used to design the input matching circuit so that the small signal power gain is flat. Since the power gain of a transistor rolls off with frequency at the rate of 6dB per octave, the gain at the highest end of the bandwidth determines the maximum possible gain. Therefore, the input-matching network is designed to conjugate match the transistor-output matching network at the highest frequency of the band, then by introducing mismatch at lower frequencies, the gain is flattened. It is worth mentioning at this point that the choice between using the source-pull data in Table 3.1 or the *S* parameters for the input matching circuit design is a matter of application. If the transistor is meant to run always at saturated power levels, then the source-pull data should be used. If on the other hand the amplifier is to operate in the linear region, or under restricted IM3 specifications, as is the case in this work, then using the *S* parameter data is preferred.

3.5 Operating frequency limitations of microstrip networks

As the signal frequency applied to a microwave network is steadily increased some characteristic frequency may be reached at which undesirable effects occur. Two possible spurious effects restrict the desirable operating frequency. These are:

- a) The lowest order TM mode.
- b) The lowest order transverse microstrip resonance.

In practice, one of these modes will be experienced at some frequency lower than the other and will thus set the frequency limitation.

Vendelin [3.7] has indicated that the most significant frequency forming modal limitations in microstrip is associated with strong coupling between the quasi TEM mode

and the lowest order TM mode. This TM mode results from approximating the microstrip environment as a dielectric slab on a ground plane. The maximum coupling between the two modes occurs when the operating frequency reaches the threshold value:

$$f_{TH} = \frac{c \tan^{-1} \varepsilon_r}{\sqrt{2}\pi h \sqrt{\varepsilon_r - 1}}$$
 (3.7)

Therefore, the choice of a substrate thickness must take into consideration that the TM mode not be launched over the frequency band of operation.

Transverse resonance occurs when the width w of a microstrip line becomes comparable to half a wavelength. In this case, the microstrip acts as a resonant transmission line of length w + 2d, where d accounts for the side fringing capacitance: d = 0.2h. The resonance frequency is given by:

$$f = \frac{c}{2\sqrt{\varepsilon_r(w + 0.4h)}} \tag{3.8}$$

For a given frequency, equation (3.8) sets a limit on the maximum allowable microstrip width.

Radiation and surface wave propagation are other important factors in high frequency applications and they add to the loss of the overall network. The main causes for such effects are abruptly open ended microstrip lines, bends, steps, and other discontinuities. However, the following design guidelines help reduce these effects:

- 1) Metallic shielding or screening of the total network.
- 2) The introduction of a small specimen of absorbent material near any radiative discontinuity.
- 3) Shape the discontinuities in some way to reduce radiative efficiency such as mitered corners and large radial bends.

4) Introducing grounded via holes near discontinuities.

3.6 Choice of substrates

Many facets, mechanical and thermal as well as electronic and economic influence the decision process leading to the correct choice of a particular substrate. The issues addressed include:

1. The loss tangent of the material at the frequency band of interest.

This factor is crucial for microstrip high power applications. A higher material loss results in lower output power and elevated operating temperatures, which ultimately may lead to damage of the network.

2. The dielectric constant of the material.

For a given substrate thickness, the width of a microstrip line is inversely proportional to the dielectric constant. For high powers applications, large currents flow and a narrow trace might not be adequate. The increase in temperature due to dissipated power might ultimately burn out the trace or peel it off the substrate. The variation of the dielectric constant with temperature is also of concern since it leads to altered network performance at different temperatures. Normally, materials with lower ε_r variations with temperature are more expensive.

3. Thermal conductivity of the material.

This factor is important in high power applications because it determines the ability of the material to draw heat from metal traces carrying high currents to the back of the substrate which is attached to a heat sink. A material with lower thermal conductivity factor might lead to a temperature rise beyond 125 degrees

centigrade which is the maximum temperature endured by the adhesion before the metal trace starts peeling off the substrate.

4. Cost and availability.

Cost is always a concern since microwave applications -as all applications, run on a specified budget. A financial decision is usually a balance of acceptable performance tolerance against cost.

Chapter IV

SIMULATION AND RESULTS

4.1 Introduction

In this chapter, we will use CAD tools to predict the RF performance of the (a) 90-degree and 180-degree hybrids, (b) gate and drain DC injection networks, and (c) transistor input and output matching networks (using the measured transistor parameters). In the core of the hybrids and DC injection networks, we are able to make comparisons between CAD models and measured data. The CAD tools are also useful for the design of matching networks between the transistor and the hybrids. However, we do not carry out an end-to-end simulation of the entire amplifier due to the large dimensions of the structure. Rather, the CAD tools are used to assist in the design process of the sub networks comprising the whole amplifier.

The chapter commences with a brief historical overview of computer-aided design packages (CAD) from their inception in the 1960's to the present day. Three CAD packages are used in this work, Advanced Design System (ADS) offered by HP, Sonnet, offered by Sonnet Software, and Zeland, offered by Zeland software. The microstrip model utilized by ADS model-based analysis tool is presented followed by a description of the differences in the meshing procedure between Sonnet and Zeland. The meshing procedure is a necessary tool for electromagnetic simulators to solve for current densities on metal surfaces. The design objectives of the passive networks and the amplifier are stated followed by simulation and measurement results. A commentary on the performance of the software packages is presented. The chapter concludes with a calculation of the uncertainty of the power measurement.

4.2 Historical overview

Through out the 1960's and into the 1970's, the operating frequency of transistors steadily increased and these devices were increasingly connected to thick-film and thinfilm integrated circuits to create the early hybrid microwave circuits (MIC's). Over those decades, many organizations developed their own computer based circuit simulators to be able to predict the performance of MIC's and meet the demand of minimum labor cost. The software was not interactive and ran on the large mainframe computers of the day. One of the first commercially available simulators was known as "Magic" and developed by John Trudell in the U.S.A [4.1]. Although Magic played a significant role in several important microwave designs of the early 1970's it ultimately failed due to lack of support. Later in the 1970's Leo Besser, as president of Compact Engineering introduced a well-supported set of microwave CAD tools that was used for many successful microwave designs. Compact Engineering later, renamed as compact software, was acquired by Communications Satellite Corporation who developed the SuperCompact to run on interactive machines. SuperCompact continues to this day as a strong product in the market. In 1984 a start-up North-American company named EEsof introduced its Touchstone family of microwave CAD tools for use on personal computer workstations. HP which introduced its own microwave CAD tools known as MDS in 1987, later acquired EESof and released the ADS software package and the Libra non linear design tool in 1989. Presently a variety of CAD tools exist in the market. Among the most common are "the Microwave Office" offered by Applied Wave Research, "Serenade" offered by Ansoft, "TeMCAD" offered by British Telecom, and Esope offered by Thompson France. Lower priced packages oriented towards specific applications are also finding more and more use. Examples of such packages are MMICAD provided by Optotek which is oriented towards the development of designs at MMIC foundries (both analog and digital), Tecad package provided by the Defense Technology Enterprises (England) oriented towards designing parallel-coupled band pass filters in microstrip or strip line environment.

The increase in computing power gave rise to electromagnetic (EM) simulators. Those tools provide electromagnetic field solutions to microwave problems by solving Maxwell's field equations thus giving an accurate and detailed picture of the fields and currents induced in a given structure. Existing software for EM simulation basically examine a structure in one of four ways - in two dimensions (2D) such as along one layered structures, in two-and-one-half dimensions open-box structures (2.5D) such as open multiple layered structures, in two-and-one-half dimensions closed-box structures (2.5D) such as closed multiple layered structures, as well as in three dimensions (3D) throughout the volume of an arbitrary geometry. Programs for 2D analyses usually apply to conductive strips or slots with uniform cross-section. Software for 2.5D analyses usually applies to structures with an arbitrary number of homogeneous dielectric layers, with arbitrary patterns in one or more planes. Simulations with 3D capability can study the entire volume of a structure, such as a waveguide. The most common electromagnetic simulators present today are the High Frequency Structure Simulator (HFSS), a 3D EM simulator released by HP in 1990, Sonnett, a 2.5D simulator release by Sonnet software in 1989, and Zeland, a 2.5D simulator released by Zeland software inc. in 1993.

4.3 Microstrip modeling in ADS, Sonnet, and Zeland

The ADS model-based tool utilizes microstrip transmission line models based on the Hammerstad and Jensen formula [4.2] to calculate the static characteristic impedance Z_0 and the effective dielectric constant ε_{eff} . This formula is based on the assumption that at low frequencies, the propagating mode is quasi TEM and as a result, Z_0 and ε_{eff} are calculated according to the following equations:

$$Z_0 = 1/(cCC_l) \tag{4.1}$$

$$\varepsilon_{eff} = C/C_1 \tag{4.2}$$

C is the capacitance per unit length of the microstrip line

 C_1 is the capacitance per unit length of the microstrip line without the substrate.

c is the speed of light.

To account for high frequency variations and dispersion effects, the effective dielectric constant is modified according to the Kirschning and Jansen formula [4.3]:

$$\varepsilon_{eff}(f) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{eff}}{1 + P(f)} \tag{4.3}$$

 ε_r is the relative dielectric constant of the substrate

 ε_{eff} is the effective dielectric constant at low frequency

P(f) is a function of frequency and microstrip dimensions. At low frequencies, P(f) tends to zero and $\varepsilon_{eff}(f)$ tends to ε_{eff} . At very high frequencies P(f) tends to infinity and $\varepsilon_{eff}(f)$ tends to ε_r . In between these asymptotic values, P(f) is determined by curve fitting equation (4.3) to numerical data obtained from electromagnetic simulation and measured data.

Zeland and Sonnet microstrip models rely basically on sub-sectioning the metal of the microstrip into small regions and then using the moment method to solve for current

densities on the metal surface. Once the current densities are known, impedances, S parameters, and electromagnetic fields can be determined. The default setting of the Zeland tool assumes an open-box environment, which means that the electromagnetic field does not get reflected by the top cover. On the other hand, the Sonnet default setting assumes a closed-box environment, which means that the structure would behave like a partially dielectric-loaded rectangular waveguide. This difference in approach between the two software tools affects the way a microstrip structure is meshed for efficient computations. With Sonnet, a metal structure to be analyzed is overlaid on a grid of prespecified cell dimensions. If the structure does not fit the grid, the dimensions of the structure have to be altered or the dimensions of the cells constituting the grid have to be made finer. As the distance from the edges of the metal structure increases, the cells gradually merge into larger subsections to cut down on computation time. With Zeland, the grid is made to fit the metal structure. The cell size specified with Zeland determines the dimensions of the edge cells only. And inside it is one large metal subsection. For a given structure, and a given cell dimension, the number of cells using Sonnet is larger than that using Zeland. Consequently, the processing time using Sonnet is much longer than that using Zeland. Figure 4.1 shows Zeland gridding as opposed to that of Sonnet.

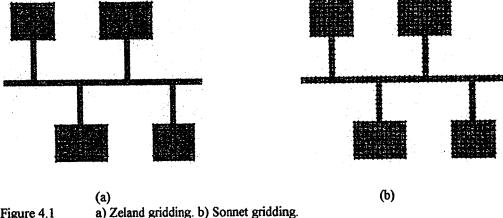


Figure 4.1

4.4 Design objectives

The design objectives of the hybrids, DC feed networks and amplifier are listed below:

1. Design bandwidth:

5.8 - 6.6GHz

2. Hybrid port isolation:

>20dB

3. Hybrid return loss:

>20dB

4. Hybrid coupling:

3dB

5. Hybrid insertion loss:

<0.3dB

6. DC injection network return loss:

>20dB

7. DC injection network insertion loss: <0.1dB

8. Amplifier small signal gain:

10dB (Typical)

9. Amplifier small signal gain flatness: <0.5dB

10. Amplifier Psat:

47dBm

11. Amplifier P.A.E.:

41%

12. IM3:

-33dBc at 40.5dBm total output power

4.5 Simulation and results of the hybrids and the DC feed networks

The substrate chosen for the development of the RF circuits is the Arlon 522T0311160 provided by Arlon Company. The general specifications of this substrate are:

Type:

ARLON 522T0311160

Material:

Teflon glass

Thickness:

0.031 in +/- 0.002

 ϵ_{r} :

2.60 +/-0.05

Metal:

loz Cu on both sides

• Loss tangent: 0.002 +/- .0001 (@10 GHz)

The threshold frequency of the TM mode as specified by equation (3.7) is 89GHz and the maximum microstrip line width before transverse resonance occurs as specified by equation (3.8) is 13 mm. The minimum allowable microstrip line width for drain feed as specified by equation (2.61) is 1.3 mm.

Figures 4.2-4.13 show the schematics, layouts, simulated and measured S parameter plots of the hybrids, and DC injection networks designed. The back-to-back loss plots of hybrids represent the total insertion loss of two cascaded hybrids. In this way, the loss figure includes copper losses, substrate losses, amplitude and phase imbalance losses. The cell dimensions used for Zeland and Sonnet simulation were $\lambda/30 \times \lambda/30$ where λ is the microstrip wavelength at the highest frequency of the bandwidth. Such dimensions provide a satisfactory margin from the maximum recommended by the software providers, which is $\lambda/20 \times \lambda/20$. The simulation time using Sonnet was much longer than the simulation time using Zeland. To speed up Sonnet processing time, whenever possible, a network was divided into symmetrical sub networks; the sub networks were simulated and then reconnected in ADS to determine the performance of the whole network. The setup used to measure the S parameters of the hybrids and DC feed networks is the same as that shown in Figure 3.4. TRL calibration scales were developed to cancel the effects of the connectors and the feed transmission lines.

The measured S parameters of the two-branch hybrid (Figure 4.3) reveal an operating bandwidth of 10% over which the return loss RL > 20dB, the isolation I > 18dB, and the insertion loss IL < 0.3 dB. The difference in simulation results between Zeland and Sonnet packages is attributed to the fact that, when using Sonnet, the dimensions of the hybrid

had to be modified to fit the predetermined grid dimensions. The discrepancy between the simulated and measured data of S_{11} and S_{14} is attributed mainly to the 50-Ohm terminations at ports 2 and 3. Such terminations are not ideal as assumed in simulation and cause small reflections that modulate measured data at ports 1 and 4. In fact, the measured return loss of each termination used is 27dB over the design bandwidth, which results in a worst case return loss of 21dB when the reflections of the two terminations add up in phase [2.0]. Since, for a two-branch hybrid, reflections at ports 2 and 3 tend to appear at port 4, the S_{14} measurement represents the vector addition of the true isolation and the reflections of the terminations as they appear at port 4. This is why the maximum isolation we could measure was 20dB. The effect of terminations reflections on S_{11} was minimal albeit a slight frequency shift in the resonant frequency. Simulation results of S_{12} , S_{13} , and IL were in good agreement with measurement data. This is due to the fact that the measured signals are relatively large and are not affected by the small reflections of the terminations. The three software packages predicted losses within 0.25dB of the measured results in the operating bandwidth.

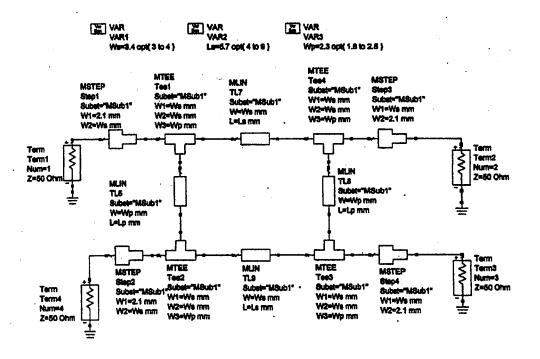
The measured S parameters of the three-branch hybrid (Figure 4.5) reveal an operating bandwidth of 18% over which the return loss $RL > 20 \,\mathrm{dB}$, the isolation $I > 19 \,\mathrm{dB}$, and the insertion loss $IL < 0.15 \,\mathrm{dB}$. Sonnet and Zeland simulation results varied because the hybrid dimensions had to be modified slightly to fit the predefined grid dimensions of Sonnet. ADS simulation results did not correlate well with measured data. This is to be expected since, for model-based tools, residual errors tend to accumulate, as the structure to be analyzed gets more complex. Zeland simulation results for S_{11} , S_{12} , S_{13} , and I were close to the measured data and predicted an insertion loss within 0.1dB of the measured

data over the design bandwidth. S_{14} simulation results could not be correlated with measured data because of the reflection of the terminations at ports 2 and 3.

The rat-race hybrid measured data (Figures 4.6-4.7) reveal an operating bandwidth of 21% over which the return loss $RL > 20 \, \text{dB}$, the isolation $I > 20 \, \text{dB}$ and an insertion loss $IL < 0.25 \, \text{dB}$. The simulation was performed only with Sonnet and Zeland because ADS does not incorporate a model for microstrip ring-shaped structures to which four ports could be added. Carrying out Sonnet simulation, two problems emerged, the first problem was overlaying the structure on the predefined grid; the second one was the inability to define the angled ports required for the rat-race hybrid. The problems were circumvented by modifying the dimensions of the structure and by introducing bends to render the ports horizontal. However, The simulated results deviated considerably from measured data as Figure 4.7 suggests. Zeland simulation results for S_{12} , S_{13} , and I were in good agreement with measured data and predicted an insertion loss within 0.1dB of measured data. The reflections of the terminations at ports 2 and 3 modulated measured S_{11} data and caused a shift in the resonant frequency. Terminations reflections corrupted S_{14} data also and limited the minimum signal measured at port 4 to $-30 \, \text{dB}$.

The broad-banded two-branch hybrid (Figures 4.8-4.9) did not exhibit good performance over the design bandwidth. The measured insertion loss was the highest among the hybrids considered so far and the difference between the simulated and measured S_{11} , and S_{14} values could not be attributed to the reflections of the terminations alone. We believe that the poor performance of this hybrid was due to the bend that was introduced in the matching stub to economize board area. To determine how sensitive the hybrid is to small increases in stub length such as that introduced by the bend, a simulation run was

conducted with the stub length increased by 5%. The results plotted in Figure 4.10 show that for a 5% increase in stub length, return loss and isolation degrade by almost 10dB. The measured S parameters of the DC injection networks (Figures 4.11 - 4.14) reveal a measured return loss RL > 20dB and a measured insertion loss IL < 0.1dB over an operating bandwidth of 36% for the gate network and 21% for the drain network. The microstrip structures to the left of plane AB in the gate network (Figure 4.11) and to the right of plane AB in the drain network (Figure 4.12) accommodate capacitors to enforce stability at low frequencies. The RF effects of these structures are nulled by connecting a low loss capacitor to ground at plane AB. Simulation plots for the drain network correlated well with measured data. The drastic increase in losses of the drain network at 5.4 GHz (Figure 4.14) is attributed to the parallel resonance of the radial stub with the rest of the microstrip structure as explained in section (2.12). This resonance is of no concern since it occurs outside the design bandwidth. The gate network simulated S_{11} plots (Figure 4.12) did not correlate well with measured data. The cause of this discrepancy may be attributed to a mismatch that was introduced into the setup after the calibration procedure was carried out. Over-torquing the network analyzer cables when joined to the SMA connectors of the gate network may cause such mismatches. Table 4.1 lists a summary of the measured data of the hybrid and the DC feed networks.



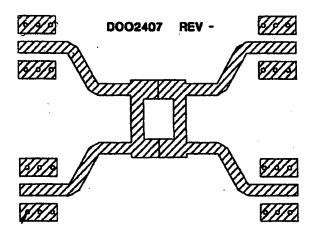


Figure 4.2 Schematic and layout of two-branch hybrid.

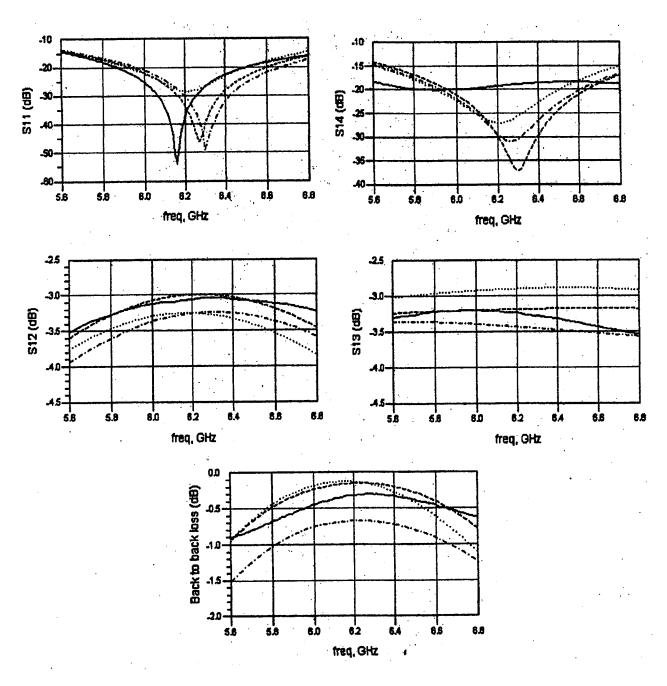
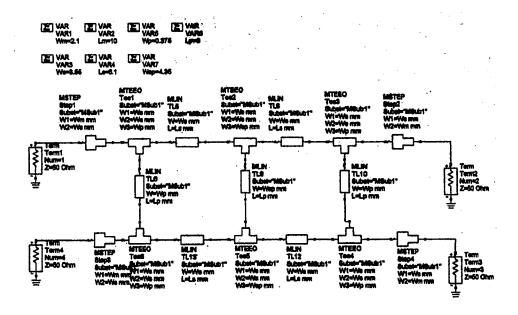


Figure 4.3 Simulated and measured S parameters of two-branch hybrid. (ADS simulation (dashed), Zeland simulation (dash-dotted), Sonnet simulation (dotted), measured (solid)).



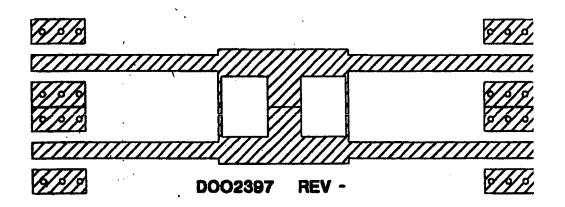


Figure 4.4 Schematic and layout of three-branch hybrid.

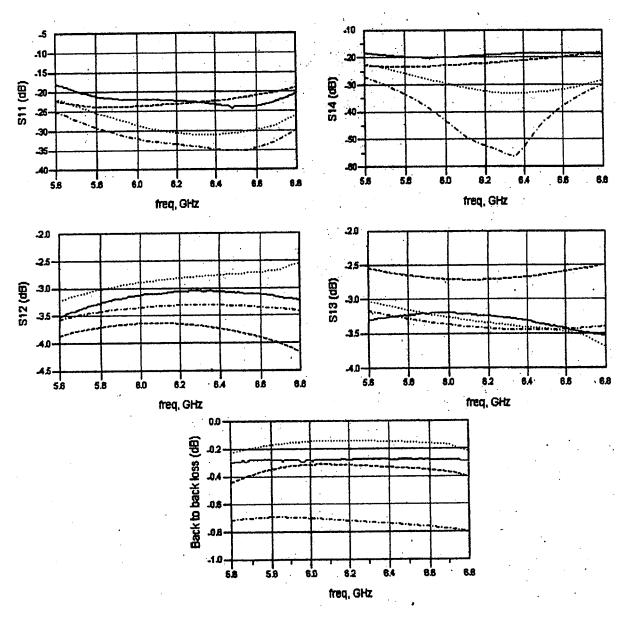
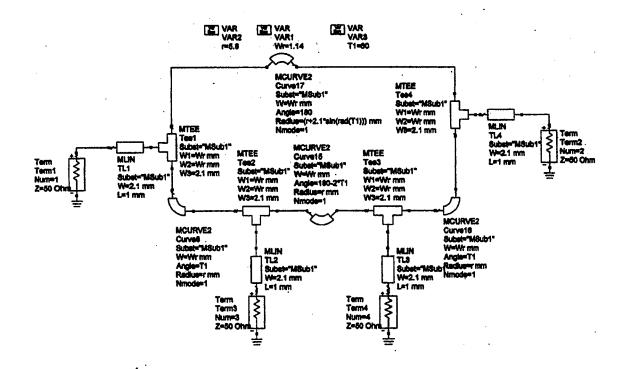


Figure 4.5 Simulated and measured S parameters of three-branch hybrid. (ADS simulation (dashed), Zeland simulation (dashed), Sonnet simulation (dotted), measured (solid)).





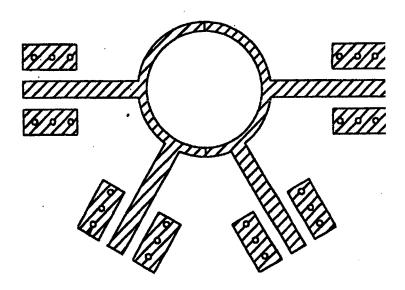


Figure 4.6 Schematic and layout of rat-race hybrid.

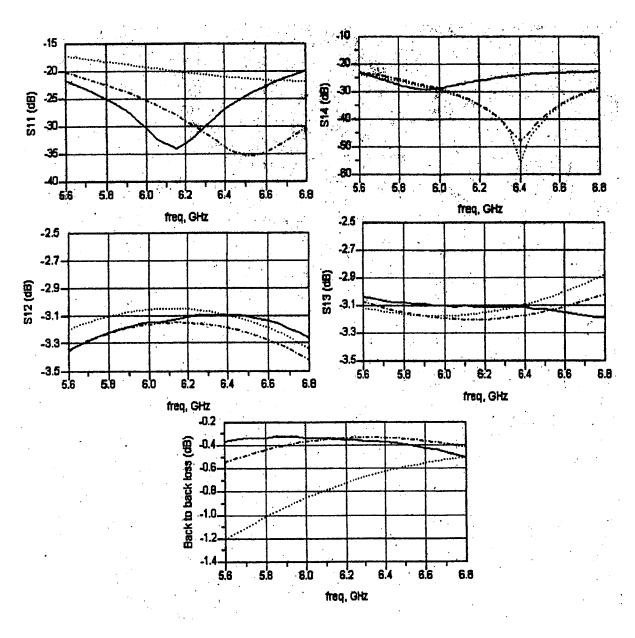
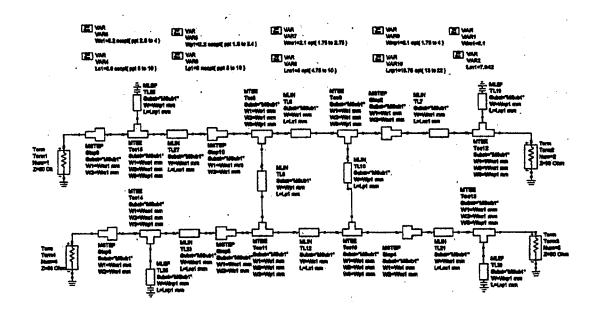


Figure 4.7 Simulated and measured S parameters of rat-race hybrid. (Zeland simulation (dash-dotted), Sonnet simulation (dotted), measured (solid)).



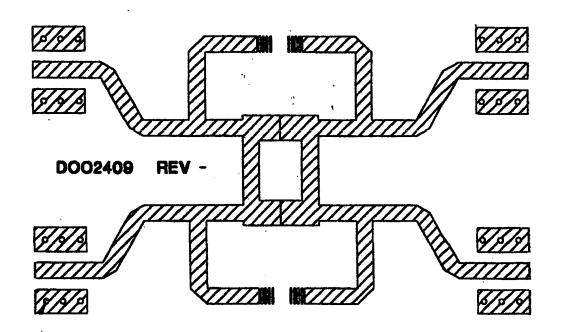


Figure 4.8 Schematic and layout of broad-banded two-branch hybrid.

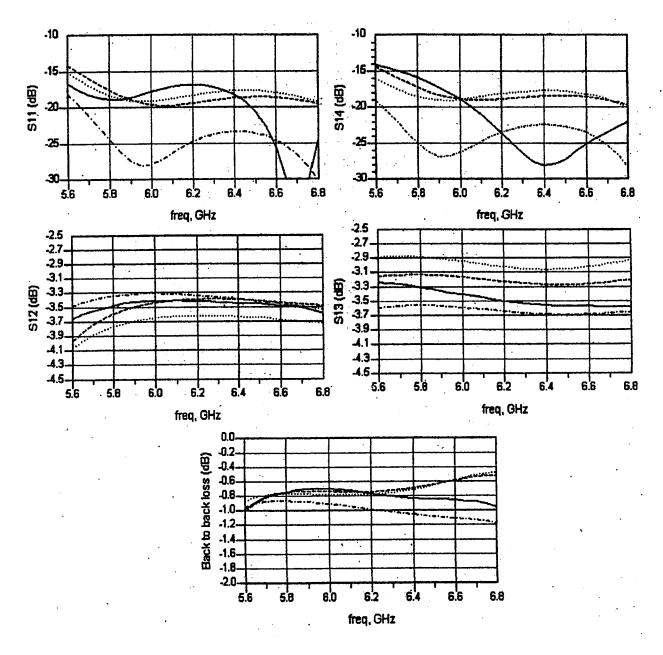


Figure 4.9 Simulated and measured S parameters of Broad-banded two-branch hybrid. (ADS simulation (dashed), Zeland simulation (dash-dotted), Sonnet simulation (dotted), measured (solid)).

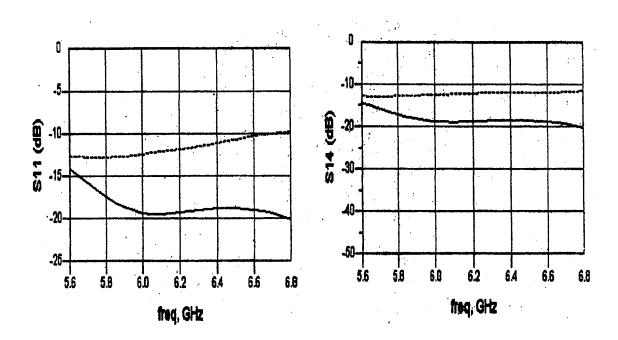
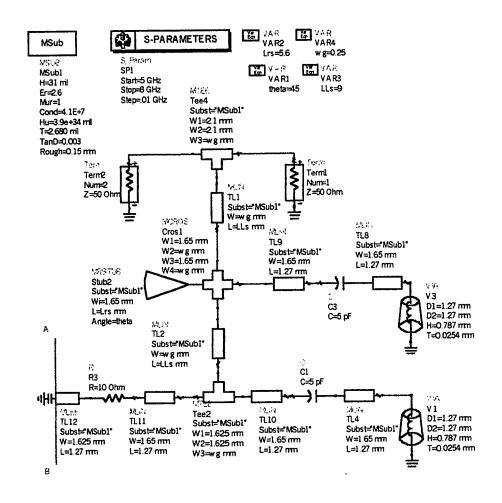


Figure 4.10 The degradation in return loss and isolation of a broad-banded two-branch hybrid as the length of the matching stub is increased by 5%. (ADS design value (solid line), 5% length increase (dotted line)).



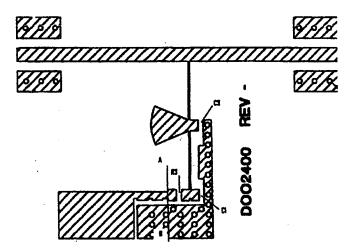


Figure 4.11 Schematic and layout of the gate DC injection network. The positions of C3, C1, and R3 are shown on the layout. The structure to the left of plane AB in the layout is not included in the simulation.

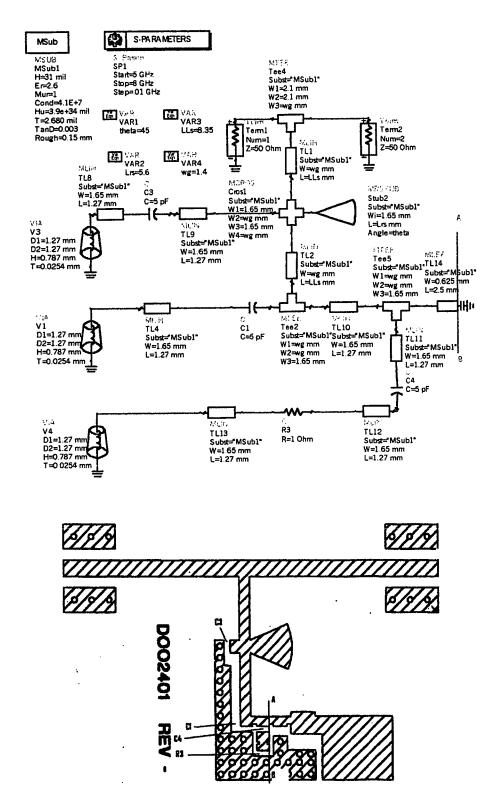


Figure 4.12 Schematic and layout of the drain DC injection network (The positions of C3, C1, C4, R3 are shown on the layout. The structure to the right of plane AB in the layout is not included in the simulation.

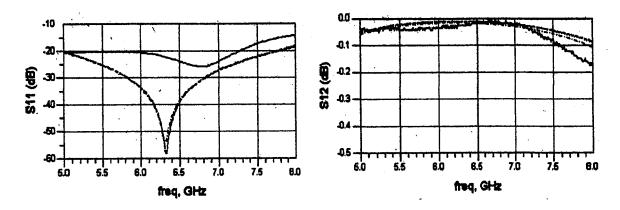


Figure 4.13 Simulated and measured S parameters of gate DC injection network. (ADS simulation (dashed), Zeland simulation (dash-dotted), Sonnet simulation (dotted), measured (solid)).

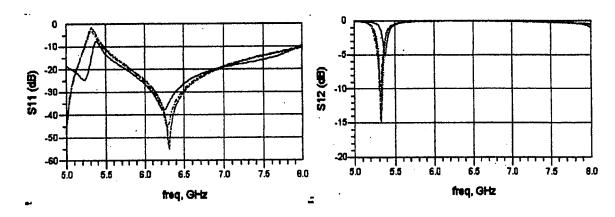


Figure 4.14 Simulated and measured S parameters of drain DC injection network. (ADS simulation (dashed), Zeland simulation (dash-dotted), Sonnet simulation (dotted), measured (solid)).

Network	Bandwidth (GHz)	Return Loss (dB)	Isolation (dB)	Insertion Loss (dB)
2-branch hybrid	5.9-6.5 (10%)	>20	>18	<0.3
3-branch hybrid	5.7-6.8 (18%)	>20	>19	< 0.15
Rat-race hybrid	5.5-6.8 (21%)	>20	>20	<0.25
Broad-banded 2-branch hybrid	5.7-6.8 (18%)	>17	>15	<0.5
Gate DC	5-7.2 (36%)	>20	1	<0.1
Drain DC	5.7-6.9 (21%)	>20	1	<0.1

Table 4.1 Summary of the measured data of the hybrids and the DC feed networks.

4.6 Simulation of matching networks and measurement of amplifier parameters

The design of the transistor matching networks followed the steps outlined in section (3.4). The output-matching network was designed using the transistor load-pull data to achieve maximum power output. Figure 4.15-a shows the transistor output RF impedance for optimum output power as it appears on the Smith chart. Using a 2-section seriesparallel microstrip transmission lines consisting of TLA1, TLA4, TLA3, TLA5 (Figure 4.15-c), the center band RF impedance was moved close to the 50-ohm area and the microstrip dimensions are then optimized to achieve broadband performance. Figure 4.15-b shows the output RF impedance after the output matching was applied. Figure (4.15-c) shows the schematic of the output-matching network. The input matching network design followed a similar procedure. Loading the transistor with the output matching network and using the transistor S parameter data, the RF impedance at the highest bandwidth frequency was moved closer to the 50-Ohm area of the Smith chart using a two-section series-parallel microstrip transmission lines consisting of TL51, TL54, TL52, and TL53 (Figure 4.16-c). The network was then optimized for maximum possible gain with 0.5dB flatness. Figures 4.16-a and 4.16-b show the RF impedance looking into the input of the transistor before and after matching. Figure 4.16-c shows the schematic of the input and output matching networks. The ADS simulation was confirmed by running Zeland simulation also. Figures 4.17 and 4.18 show the layout of the matching circuits and the simulated S parameters.

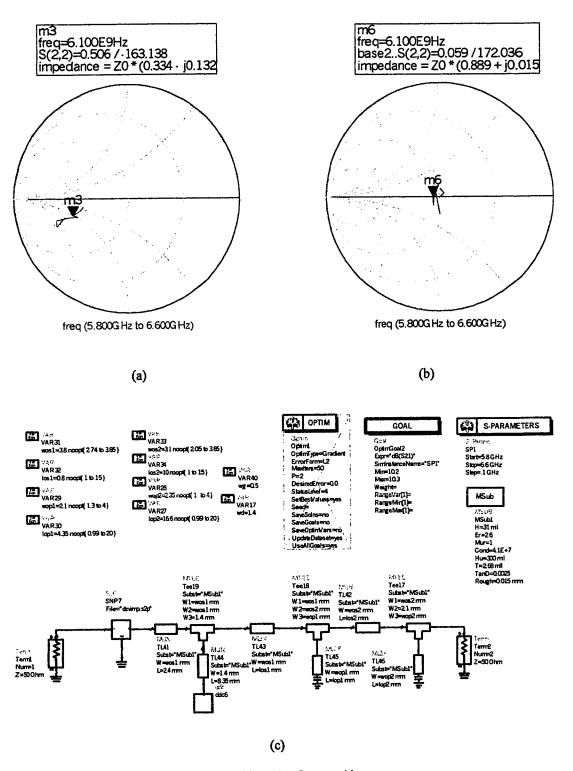


Figure 4.15 a) Transistor S22 before matching, b) After matching. c) Output matching network schematic.

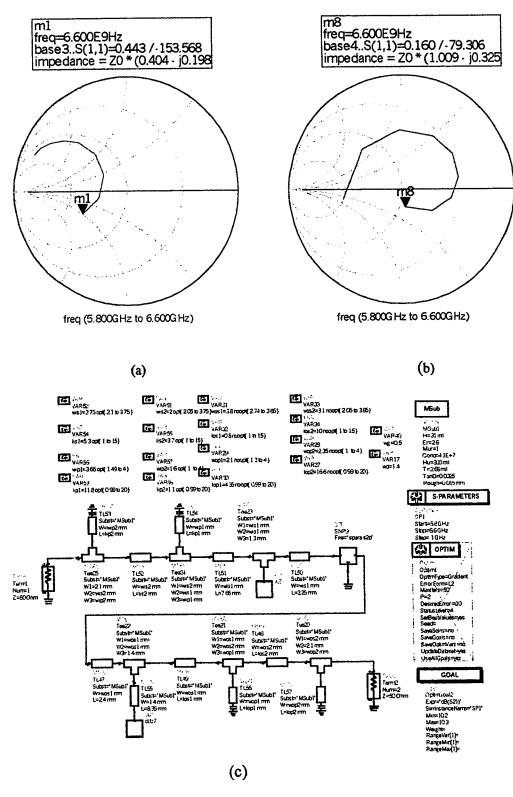


Figure 4.16 a) Transistor S_{11} before matching. b) after matching. c) Input and output matching network schematic.

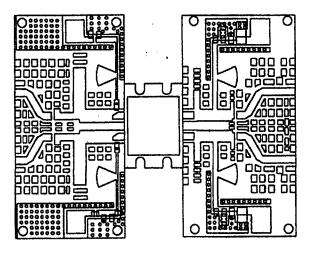


Figure 4.17 Layout showing the transistor pair, two input matching networks, two output matching networks, two gate DC injection networks, and two Drain DC injection networks.

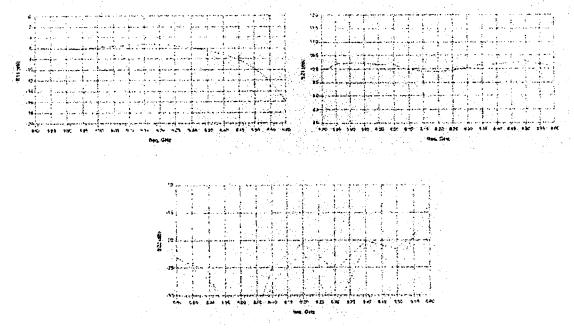


Figure 4.18 Simulated S parameters (solid (ADS), dash-dotted (Zeland)) of the transistor with matching networks and DC injection circuits.

With all the amplifier building blocks implemented, a test fixture was designed to evaluate the performance of the whole amplifier including the matching structures with the DC networks, and the hybrids. The test fixture consisted of 5 blocks, a device block, two blocks for input and output matching networks and two blocks for the input and output hybrids. The modular design of the test fixture allowed the exchange of hybrids without having to change the input and output matching networks. Figure 4.19 shows a photograph of the test fixture. The device was biased to a drain voltage of 12 volts and a drain current of 4.5Amps. A 10-Ohm resistor was connected in series with the gate as recommended by the device manufacturer to insure stability. The setup used to test the amplifier was computer-controlled through HPVEETM software provided by HP. The software allows the automated gathering of all relevant amplifier data such as power measurements, gain measurements, P.A.E and inter-modulation distortion measurements. Figure 4.20 shows a block diagram of the setup used. The amplifier was tested with the three-branch hybrid (balanced format) and with the rat-race hybrid (push-pull format). Figures 4.21 and 4.22 show a sample of the gain measurements and the amplifier input mismatch for each hybrid used. IM3 measurement was carried out over a bandwidth of 5.425-6.425GHz due to lack of a broadband driver amplifier.

For the 90-degree and 180-degree formats, the amplifier measured small signal gain (Figures 4.21-a, 4.22-a) was close to the simulated transistor small signal gain (Figure 4.18). Keeping in mind that the simulated transistor small signal gain did not include the losses of the hybrids and the coupling capacitors, which total to about 0.6dB, roughly the difference between the simulated and measured linear gain. The measured amplifier return loss for both formats (Figures 4.21-b, and 4.22-b) revealed a frequency variation

similar to the simulated results of Figure 4.18. By that we mean the matching occurred at the highest bandwidth frequency and degraded as frequency decreased. However, with the balanced format, the worst return loss measured was 15dB compared to a worst return loss of 5.5dB for the push-pull format. This difference in performance is due to the fact that for a three-branch hybrid, reflections at the output ports appear at the decoupled while for the case of the rat-race, all reflections appear at the input port and degrade the return loss

The coupling between the individual matching networks was a concern especially at the output side where high RF power is being transmitted. A Zeland simulation of the complete output structure was carried out and it was found that the coupling between the output matching circuits is miniscule (<-23dB) and does not affect the overall output performance. The Fujitsu transistor showed potential instabilities for frequencies below 750MHz where the stability factor K dipped below the threshold value of 1. During measurement, no resonance occurred at that frequency band. This is due to the losses imposed by the decoupling capacitors. Such losses counter the high device gain at low frequencies and stabilize the overall amplifier. Table 4.2 lists a summary of the balanced and push-pull format data. The Table reveals slightly better values for Psat, IM3, and P.A.E when the 180-degree hybrid format is employed. However, the 90-degree hybrid format revealed better return loss,

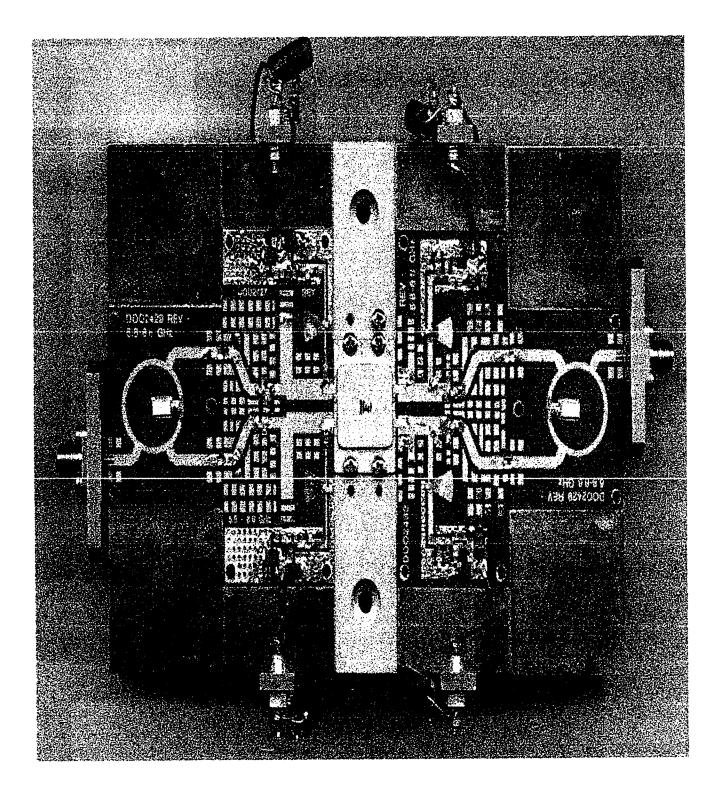


Figure 4.19 The amplifier test fixture with two rat-race hybrids at the input and output.

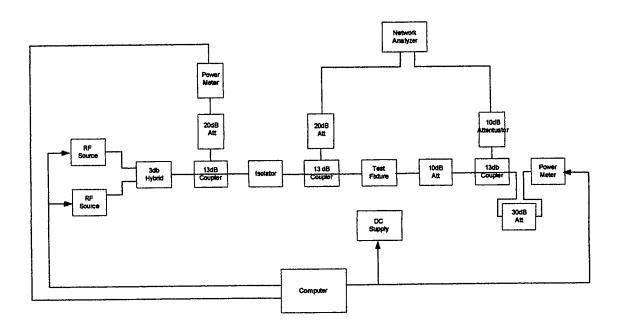
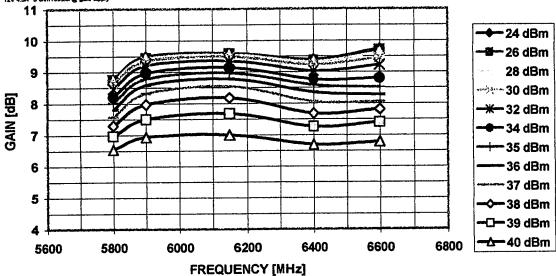


Figure 4.20 The amplifier measurement setup.

GAIN at INPUT POWER STEPS vs. FREQUENCY TEST DATE/TIME: 27/80p/2001 14:45.51 TESTED BY: JA CW POWER MEASUREMENT

FILITSU COMPOUND SEMICONDUCTOR, INC. TEST DATE/TIME: 27/Sep/2001 14:45:51 TESTED BY: IA CW POWER MEASUREMENT HYBRID TYPE: RATRACE VIDS= 12 VIDC, IDS= 4500 mA LOT #: SERIAL #: POA #: FIXTURE: SER. #: TYPE: 12V 4.5A 5 ohm resistor @ gette supply



(a)

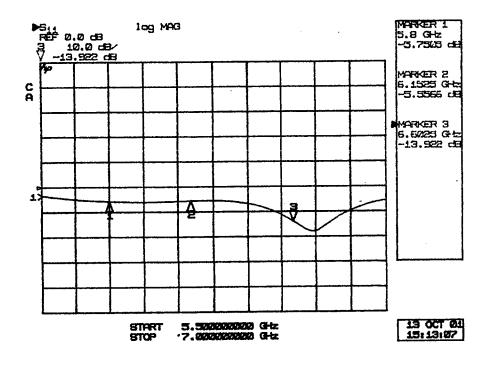


Figure 4.21

a) Variation of amplifier measured gain vs. frequency and power with rat-race hybrid (Plot captured by HPVEE software).

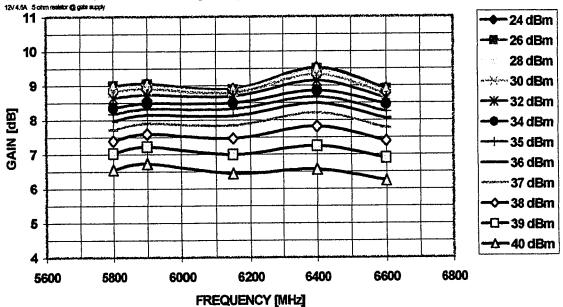
b) Amplifier input mismatch (Plot captured by network analyzer).

(b)

80

GAIN at INPUT POWER STEPS vs. FREQUENCY

RUITSU COMPOUND SEMICONDUCTOR, INC. TEST DATETIME: 27/Sep/2001 16:3955 TESTED BY, A OW POWER MEASUREMENT HYBRID TYPE THREE-BRANCH, VIDS-12 VDC, IDS-4500 mA LOT #_ SERAL #_ POA #- PIXTURE SER. #_ TYPE_



(a)

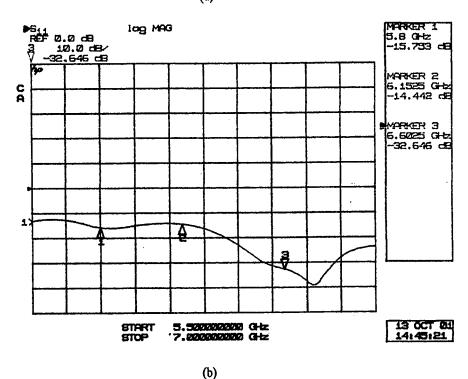


Figure 4.22

a) Variation of amplifier measured gain vs. frequency and power with three-branch hybrid (Plot captured by HPVEE software).

b) Amplifier input mismatch (Plot captured by network analyzer).

	F	Psat	G	ΔG	P.A.E	RL	IM3(L)	IM3(U)
Hybrid	(GHz)	(dBm)	(dB)	(dB)	(%)	(dB)	(dBc)	(dBc)
	5.8	46.5	8.8		38.4			
Rat race	6.15	47	9.6	1	43.7	5.5	-31.1	-32.5
	6.6	46.8	9.7	1	33.9			
	5.8	46.6	9		37			
3-branch	6.15	46.3	8.7	0.5	38	16.7	-29.2	-30.7
	6.6	45.9	9.1		28.3	1		

Table 4.2 A summary of amplifier measured data). G is the small signal gain, ΔG is gain flatness, RL is the minimum return loss, IM3(L) is the distortion at the lower side of the two tones, IM3(U) is the distortion at the upper side of the two tones. Psat is the saturated output power at an input power of 40dBm.

4.7 Power measurement uncertainty

The computer setup used to test the amplifier relied on power meters to record power measurements, compute gain and P.A.E data. Due to the attenuators and couplers placed in the output section of the setup, every power meter recording requires three actual power measurements. Hence, power meter measurement uncertainty becomes a factor in determining how reliable the measured data is. In this section an equation is developed to determine the uncertainty of the power measurement. Figure 4.23 shows a power meter connected to a microwave generator through a power sensor. Ideally, The input reflection coefficient of the sensor is zero and all the power P_o of the generator is transmitted to the sensor but due to mismatch, part of P_o gets reflected and the other part P_{sens} is transmitted to the sensor.

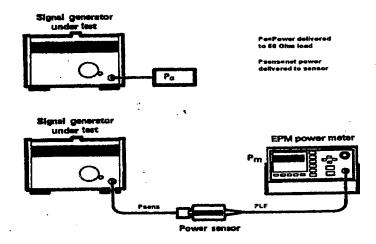


Figure 4.23 A power generator connected to a power meter through a power sensor (Reprinted from [4.4]).

The relationship between P_o and P_{sens} is given by [4.3]

$$P_o = \frac{\left|1 - \Gamma_g \Gamma_{sens}\right|^2}{1 - \left|\Gamma_{sens}\right|^2} P_{sens}$$
 (4.4)

where Γ_{sens} , and Γ_g are the reflection coefficients looking into the sensor and into the generator respectively. The transmitted power P_{sens} is then converted by the sensor to a DC or a low frequency signal of power P_{LF} . A conversion efficiency η is defined to characterize this process as:

$$\eta = P_{LF} / P_{sens} \tag{4.5}$$

Finally the converted power P_{LF} is amplified and conditioned by power meter circuitry to give the displayed power P_m . P_m is related to P_{LF} by the linear relationship:

$$P_m = mP_{sens} + t (4.6)$$

Where m is the amplification of the power meter and t is an unavoidable residual term introduced by the power meter circuitry. Combining equations (4.4), (4.5) and (4.6) results in the general relationship between the power P_o of a source and the registered power P_m of a power meter as:

$$P_o = \left(1 - \Gamma_g \Gamma_{sens}\right)^2 \left(\frac{1}{m\eta(1 - |\Gamma_{sens}|^2)}\right) (P_m - t)$$
 (4.7)

or equivalently:

$$P_o = M_u \left(\frac{1}{mK}\right) (P_m - t) \tag{4.8}$$

 $M_u = |1 - \Gamma_g \Gamma_{sens}|^2$ and is known as the mismatch uncertainty term.

 $K=\eta(1-|\Gamma_{sens}|)^2$ and is known as the calibration factor of the power meter.

The uncertainty introduced by M_u is due to the fact that only the magnitudes of Γ_g and Γ_{sens} are known with no information about their respective phases. Hence the value of M_u could be anywhere between $(1-|\Gamma_g||\Gamma_{sens}|)^2$ and $(1+|\Gamma_g||\Gamma_{sens}|)^2$ depending on how the complex product $\Gamma_g\Gamma_{sens}$ adds up with 1. The uncertainty introduced by magnification mis due to several factors such as instrumentation uncertainties (range-changing attenuator errors, tracking circuitry errors), and reference source uncertainties (mismatch and power value uncertainties). The total uncertainty of m is calculated either as a product of all the constituent uncertainties (worst case) or as a root sum of squares of uncertainties (most probable case). The calibration factor K is a function of frequency and a calibration table is usually supplied with the sensor to offset the frequency variation. However, there is inherent uncertainty in the values of the calibration table and the manufacturer usually supplies a tolerance table for K along with the calibration table. The contribution of the residual term "t" in equation (4.7) is usually nulled by "zeroing" the power meter before carrying out a measurement. However, noise, temperature drift, and other factors contribute uncertainty to the zeroing process and add up to the overall uncertainty of the power measurements.

The total measurement uncertainty may be calculated on a worst-case basis where all possible sources of error are at their extreme values and in such a direction as to add together constructively, hence achieve the maximum possible deviation between the registered power P_m and the incident power P_o . In this case, P_o is in an interval of values $[P_{o1}, P_{o2}]$ given by:

$$P_{o1} = M_{uMAX} \left(\frac{1}{m_{MIN} K_{MIN}} \right) (P_m - t_{MAX})$$
 (4.9)

$$P_{o2} = M_{uMIN} \left(\frac{1}{m_{MAX} K_{MAX}} \right) (P_m - t_{MIN})$$
 (4.10)

A more realistic method of combining uncertainties is the root sum of squares method (RSS). The RSS uncertainty is based on the fact that most errors of power measurement are independent of each other and the individual uncertainties can be added according to the following equation:

$$\frac{\Delta P_0}{P_0} = \sqrt{\left(\frac{\Delta M}{M}\right)^2 + \left(\frac{\Delta K}{K}\right)^2 + \left(\frac{\Delta m}{m}\right)^2 + \left(\frac{\Delta t}{P_m}\right)^2}$$
(4.11)

The data supplied by the manufacturer for the uncertainty calculations of the HP438A power meter with the HP8485A power sensor in the frequency band of interest is as follows:

- Sensor reflection coefficient $|\Gamma_{sens}| = 0.07$ (worst case).
- Calibration factor K uncertainty = \pm 4% (worst case), \pm 2.3% (probable).
- Magnification m uncertainties:
 - Power reference accuracy = \pm 1.2% (Worst case), \pm 0.9(Probable).
 - Instrumentation accuracy = ± 0.02 dB.
- Residual term "t" uncertainties:

- Digital settability of zero \pm 0.5% full-scale power (Most sensitive range. Decrease percentage by a factor of 10 for each higher range).

Table 4.3 summarizes the uncertainty calculations for a single power measurement at Pm=7dBm, a full scale power $P_{f.s.}$ =10dBm, and a source reflection coefficient of $|\Gamma_g|$ = 0.01. The residual term contributions where discarded from uncertainty calculations because the uncertainty due to t at a full-scale power of 20dBm, is estimated at 0.0005%.

Error	Worst case	values	RSS components		
	Max	Min	ΔX/X		
M_{μ}	1.001	0.999	0.001		
K	1.04	0.96	0.023		
Components of m					
-Power ref.	1.012	0.988	(0.012)		
-Instrumentation	1.005	0.995	(0.005)		
Total m	1.017	0.983	(0.013)		
Power uncertainty for a 7dBm readout	+0.26dB	-0.25dB	+0.11dB -0.12dB		

Table 4.4 Uncertainty of a single power measurement.

Table 4.4 gives the uncertainty of a single power measurement. However, since the amplifier output power is the measured power plus the power lost in the output section of the setup, three power measurements are needed to get at the actual output power of the amplifier. Therefore the total uncertainty of the power measurement is given by:

$$P_o = P_m \pm 0.8 dB$$
 (worst case)
 $P_o = P_m \pm 0.2 dB$ (most probable case)

CHAPTER V

Conclusion and Future Trends in Microwave Power Amplifier Design

5.1 Conclusion

In this thesis, the design, simulation, and implementation issues of a C-band microwave power amplifier were tackled. Different hybrid networks were studied and their properties derived. Microstrip design guidelines for DC injection circuits and matching networks were presented. Prototypes of hybrids and other networks were built, tested, and compared for best performance. The characteristics of the transistor were extracted using small signal S parameter measurement techniques and the transistor impedance for optimum output power was extracted using a load-pull measurement system. The extracted parameters were used to design the input and output matching networks of the transistor. An amplifier circuit was assembled in a push-pull format using a rat-race hybrid and in a balanced format using a three-branch-line hybrid. It was found that the push-pull format exhibited slightly better characteristics than the balanced format in terms of inter-modulation distortion, P.A.E., and saturated output power. On the other hand, the push-pull format exhibited bad return loss compared to the balanced format. Three simulation tools were used for the simulation phase: the model-based tool of the ADS package, and the Sonnet and Zeland electromagnetic simulators. The software packages predicted results that were relatively close to measurement for the cases of S_{12} and S_{13} for the passive networks, and S_{21} for the amplifier. However, large discrepancies were observed between the simulated and measured values of S_{11} and S_{14} . This is attributed to the fact that the measured signals S_{12} , S_{13} , and S_{21} were relatively large in amplitude and the measurements were not affected by the reflections form the 50-Ohm terminations connected to the rest of the ports. Such was not the case for the small signals S_{11} and S_{14} where the measured data were corrupted by the reflections of the terminations. The ADS S parameter model-based tool simulation results were close to those of the EM simulators for the cases of S_{12} and S_{13} for the passive networks, and S_{21} for the amplifier. This is due to the fact that the analyzed microwave structures were not complex. That is, there was no coupling issues or radiation patterns to be studied, in which case the EM simulators would have clearly given a better understanding of the microwave environment. Zeland software with its nonuniform gridding scheme was much faster than Sonnet package in analyzing the networks at hand. However, the amplifier was tested in an open-box environment and that is ideal for the default settings of the Zeland tool. Had their been a closed-box environment with a restriction on the allowable box dimensions, The Sonnet tool would have predicted more accurate results than the Zeland tool.

5.2 Future Trends in microwave power amplifier design

Microwave transistors continue to evolve driven by market demands for higher power, higher operating frequency, and higher efficiency devices. Advances in material technology and processing technology continue to refine existing transistor architectures and test for new materials. Derivatives of GaAs FETs like the HEMT (High Electron Mobility Transfer) transistors with their superior noise performance and small-signal gain have already replaced the FETs in low power applications and current work is focusing on improving their power performance. Heterojunction Bipolar transistors (HBTs) are another types of transistor architectures that are already being used for up to millimeter

wave applications and current research is carried out at improving the process technology of those transistors. Alternative materials to GaAs are being investigated for microwave performance. InP with its superior thermal conductivity seems a promising candidate in high power applications.

Perhaps the most impressive current development is in the field of power combining. Spatial combining, where individual amplifiers get combined in free space is emerging as an alternative to the traditional power combining techniques used today. Tens of devices have been combined in research labs using spatial combining methods thus breaking the limits set by traditional methods on the maximum number of devices that could be combined. Two approaches have already demonstrated impressive results; they are the tray array approach and the tile array approach. Using a tray array approach, researchers at the University of California were able to combine 32 MMICs and achieve a maximum power 150W over a bandwidth of 8-11GHz [5.1]. Using a tile array approach, researchers at Lockheed-Martin and North Carolina State University were able to combine 45 MMICs and achieve a 25W at 34GHz with a bandwidth of 800MHz [5.2]. The most stunning accomplishment has been the reported results from Sanders where researchers, using a tile approach, were able to combine 272 MMICs and achieve an output power of 35W at 61GHz [5.3].

Spatial combining is still in its infancy but it is promising to lead to the eventual replacement of tube-based amplifiers with solid-state amplifiers.

End

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