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INTERPOLATION METHODS IN THE SIMULATION OF

POWER ELECTRONIC CONVERTERS

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A Thesis

In

The Department

Of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements
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ABSTRACT

INTERPOLATION METHODS IN THE SIMULATION OF POWER ELECTRONIC CONVERTERS

Ming Zou

This thesis is devoted to the simulation of switching events in power systems and power electronics circuits. It addresses issues related to algorithms using fixed time step integration methods. In power electronic circuits simulation, the high repetitive rate of switching events causes numerical difficulties that require development of techniques to achieve an accurate representation of switching events. Various techniques are proposed in the literature to accurately determine switching instants. The thesis proposes an interpolation-extrapolation (IE) algorithm, which eliminates numerical oscillations and provides a sufficiently precise solution. The method gives accurate results even with larger time steps. The proposed method is tested in a number of circuits using electronic switches and to power electronic circuits. To solve the problems resulting from natural commutation of diode and forced commutation of transistors and Gate Turn Off Thyristors, an extension of the IE technique is proposed. Contrary to existing methods, the proposed method eliminates the need to force the semiconductors to work as pairs, or to add snubber circuits across every switch. To test the applicability of the method, it has been successfully implemented and tested in commercial packages under development at IREQ (Institut de Recherche d'Hydro-Québec).

ACKNOWLEDGEMENTS

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CHAPTER 1

PROBLEM REVIEW

1.1   INTRODUCTION

Recent developments in power systems. particularly in the application of power electronics. require the power system simulation tools be adapted to the specific behavior of these devices. The most common approach for detailed simulation of transients in power systems uses a fixed integration time-step with the trapezoidal integration method. Problems arise with the introduction of natural and forced commutated devices.

1.2   DESCRIPTION OF THE PROBLEM

In power system digital simulation. there are several powerful software packages such as DCG-EMTP (Electromagnetic Transient Program) [1] [4]. NETOMAC (Network Torsion Machine Control) [2] and SPICE (Simulation Program with Integrated Circuit Emphasis) [3]. which can accurately simulate the transient states by the trapezoidal integration method with fixed time-step. However. a discontinuity problem is generated because of characteristics of the trapezoidal rule and numerical discretization. Many numerical methods were pointed out trying to eliminate the effect of discontinuity [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15] [21] [22]. In addition. some other numerical integration methods were developed to replace the trapezoidal rule in electromagnetic transient simulations [16] [17] [18] [19] [20]. However. they have not been implemented

in large-scale power system applications. The trapezoidal rule remains widely used and accepted in fixed time-step simulations due to its precision and stability.

An important drawback of the trapezoidal integration is its oscillatory behaviors at discontinuities.

This can be illustrated by a simple RLC case shown in Fig 1.1. The switch (ideal model) is turned on at time t_1 ($0.016666s$) and turned off at time t_2 ($0.0285s$). Assume that at time t_d it is found that the switch current has crossed zero.
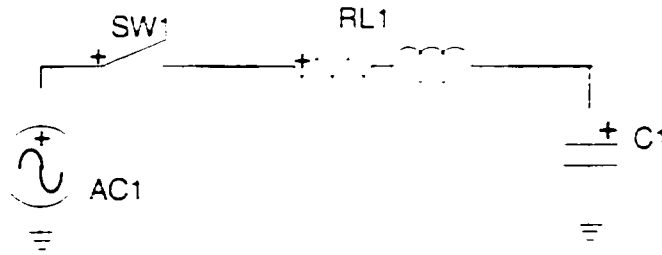
Fig 1.1   RLC circuit case

With the trapezoidal rule the inductance equation (i_{L_d} is the inductance current at time t_d . v_{L_d} is the inductance voltage at time t_d) is given by

$$i_{L_d} = \frac{\Delta t}{2L} v_{L_d} + \frac{\Delta t}{2L} v_{L_d - \Delta t} + i_{L_d - \Delta t}$$

(1.1)

Which means that at $t_d + \Delta t$ we have

$$0 = \frac{\Delta t}{2L} v_{t_d - \Delta t} + \frac{\Delta t}{2L} v_{t_d} + i_{t_d} \qquad (1.2)$$

At $t_d + 2\Delta t$ we get

$$0 = \frac{\Delta t}{2L} v_{t_d + 2\Delta t} + \frac{\Delta t}{2L} v_{t_d + \Delta t} \qquad (1.3)$$

It appears from this step that the inductance voltage enters into oscillations. There are numerical oscillations unrelated to actual physical phenomena.

$$v_{t_d + 2\Delta t} = -v_{t_d + \Delta t} \qquad (1.4)$$

In general,

$$v_{t_d + \Delta t} = -v_{t_d} \qquad (1.5)$$

The simulations results are shown in Fig 1.2. This is a typical situation with EMTP.

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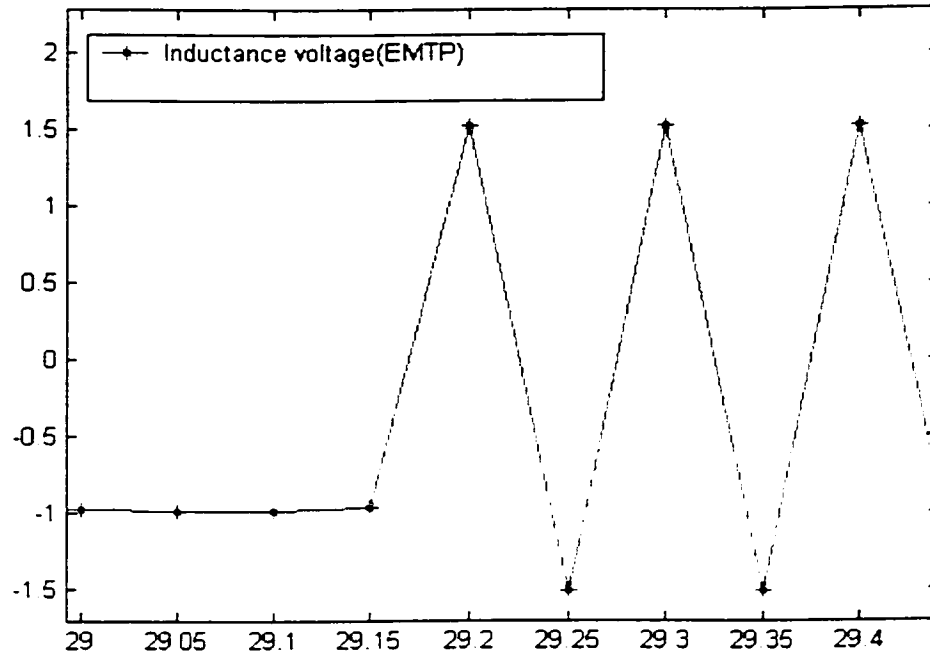
Fig 1.2   Inductance voltage oscillations (x axis: ms; y axis: inductor voltage, in V)

Although implementing Backward Euler [5] [6] at discontinuity points removes numerical oscillations and simplifies switching device modeling by eliminating the conventional numerical snubbers. the fixed integration time-step remains an important drawback. If the simulation engine cannot precisely account for the possibility of firing and extinction between two discrete simulation points. errors occur. non-characteristic harmonics are generated and abnormal operating modes appear. One corrective measure is to decrease the integration time-step at the expense of much longer computation time. This can increase the precision in some cases. but does not resolve the issue of simultaneous switching transition. The difficulty is that a variable time-step problem is being solved with a fixed time-step and ideal or linear switching device models. The fixed time-step remains a requirement to avoid unaffordable long computer execution

times in addition to significantly increased complexity in device model programming. Moreover, at the power system analysis level, it is not necessary to model the switching devices with great detail since this has no significant impact on power system behavior.

1.3 SUMMARY OF PREVIOUS WORK AND LITERATURE REVIEW

1.3.1 EMTP simulator

EMTP is based on trapezoidal integration and uses a method called CDA [5] [6]. The Critical Damping Adjustment (CDA) is achieved by means of two $\dfrac{\Delta t}{2}$ integration steps using Backward Euler rule. In Fig 1.3, with CDA scheme, the trapezoidal rule can be used throughout the entire simulation without oscillations at discontinuities.
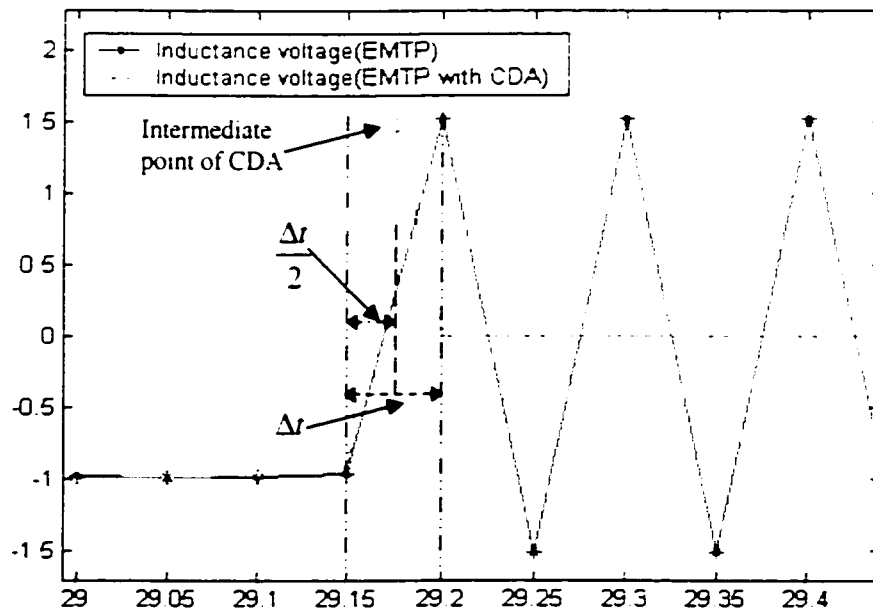
Fig 1.3   Eliminating oscillations of inductance voltage in CDA (x axis: ms: y axis: inductor voltage, in V)

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However, the CDA algorithm does not offer a complete solution. On one hand, it cannot find the exact turn-on instant or extinction instant. Besides, CDA cannot calculate the re-initialization values of state variables after discontinuities.

CDA cannot account for instantaneous switching conditions. There is a problem on the significance of the intermediate solution. This can be illustrated using the circuit of Fig 1.4. If the switch is forced to become open, then an impulse voltage will result on the inductance and if the intermediate solution is neglected, it will simply eliminate the impulse and the diode will not turn on. This problem has been demonstrated in [11] and recognized in [21]. One possible solution to this problem is to account for the intermediate computation step [21]. But this is not a complete solution since it is not simple to derive a rule for distinguishing between true and false impulse conditions. Indeed for the natural commutation case, the resulting impulse is only numeric and should be discarded. There is also the possible simultaneous (within the same time-step) occurrence of true and false impulses in separate circuit sections, which may require using complicated topological recognition.

One more problem illustrated by the circuit of this ideal case is the need for a simultaneous solution. The diode must operate simultaneously with the switch. If, for example, the diode opening is delayed after the switch closing, then the dc voltage will be forced onto the capacitor and the solution will become totally wrong. A simple solution to the simultaneous switching problem is to restart the circuit solution without advancing in time until all switches have settled. This will not cover for switching occurring within a time-step.

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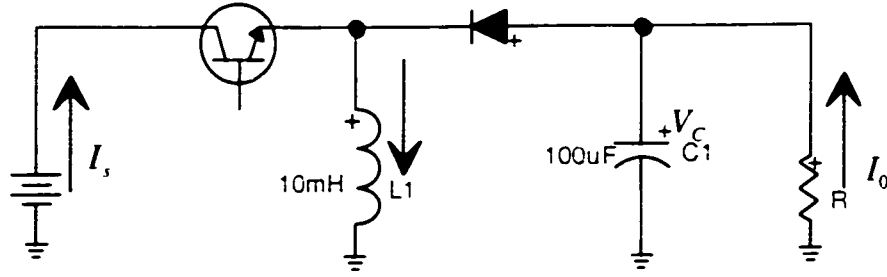
Fig 1.4   Converter circuit used to demonstrate switching problems

1.3.2   EMTDC simulator

The EMTDC program [7] [13] [15] is another widely used power system simulator. It has a built-in interpolation method for finding the exact switching time between two discrete time points. Interpolation is also used to return to the original time-mesh. As for the problem of numerical oscillations. EMTDC also applies numerical interpolation.

The drawback of EMTDC is that it lacks an appropriate method to properly resume simulation after discontinuities. The algorithm of the interpolation technique is not mathematically supported. Adequate precision cannot be obtained and the method's behavior cannot be generalized.

1.3.3   NETOMAC simulator

In addition to the simulators mentioned above, NETOMAC [2], another fixed time-step simulator, uses interpolation to account for switching points, and to make a prediction on state variables. In contrast with EMTDC. this method accounts for state variable

continuity. There is also a mathematical basis for the algorithm. The drawbacks of both modified EMTDC and NETOMAC are discussed in detail in Chapter 3.

1.4 PROPOSED SOLUTION

The ultimate solver will not allow jumps in state variables and will be able to reinitialize correctly to minimize errors for the following time-points. There would be no numerical oscillations and all computed points should be consistent.

A theoretical approach of solving discontinuities is that, at the exact switching time, the simulator performs the switching operation. At the instant of state variable discontinuity, it reinitializes all state variables and begins new calculations for the following simulation time-points.

The proposed approach is able to solve simultaneous switching case without loss of generality. It also eliminates numerical oscillation and does not require extra interpolation steps.

The proposed approach provides a simple yet effective method to achieve an accurate switching representation in fixed time-step simulations. It presents a way to solve the whole network twice at the switching instant and to obtain the initial conditions required to resume simulation after discontinuity. With this method, the accuracy of re-initialization is more independent of the time-step.

The New Method is an extension of the NETOMAC algorithm. It uses the state variables

(inductance current and capacitor voltage) at the discontinuity time point t_d^- and $t_d + \dfrac{\Delta t}{2}$

to extrapolate the artificial initial conditions at $t_d - \dfrac{\Delta t}{2}$ and recalculates the whole

network at t_d^-.

Extrapolation provides an improvement over the existing NETOMAC method. There is

also the added ability to account for forced commutation cases.

Fig 1.5 shows the inductance current for the case shown in Fig 1.4. The theoretical

minimum value is 9A. The New Method finds 8.995A. It is noticed that EMTDC does

not show current continuity.
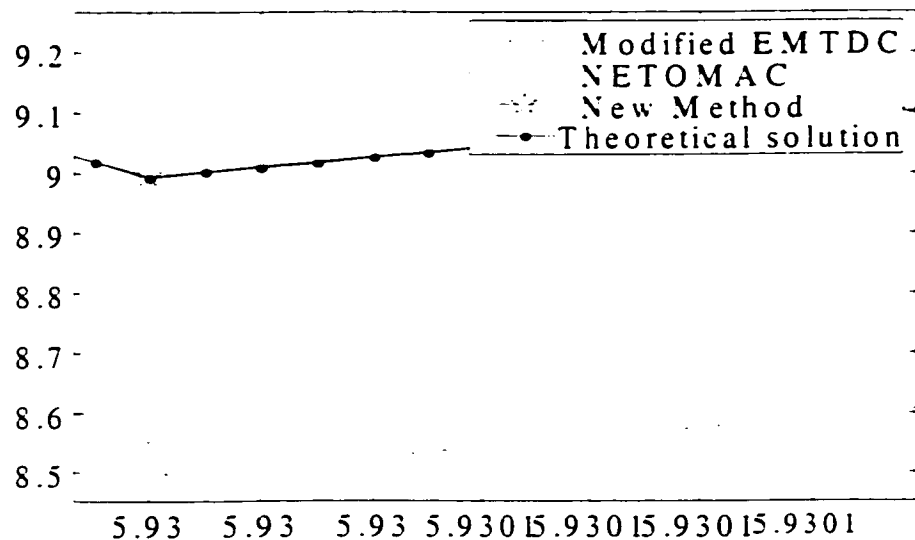
Fig 1.5   The enlargement waveforms of inductance current (x axis: ms; y axis:

inductor current, in A)

1.5   THESIS OBJECTIVES

The objectives of this thesis are to:

- Propose a new algorithm for solving discontinuity problems in the simulation of transients.

- Provide a background and a systematic approach for the analysis of available techniques and a comparison with the new technique.

- Implement the new method in a commercial simulator and demonstrate its capabilities for arbitrary circuits.

- Provide solved test cases for the most demanding power electronic circuits where frequent and repetitive discontinuity problems exist.

1.6   THESIS OUTLINE

The contents of this thesis are organized as follows:

Chapter 2 presents a review of different numerical methods and two main methods for formulating circuit equations.

Chapter 3 presents a systematic evaluation of the existing methods and the proposed method, and a theoretical analysis and comparison.

Chapter 4 implements the new algorithm in the simulation of different cases. The simulation results of each method are presented at the end to illustrate the advantages of New Method.

Chapter 5 presents a summary of the thesis, conclusions regarding feasibility and performance of the proposed method and suggestions for future work.

CHAPTER 2

THEORETICAL ANALYSIS OF NUMERICAL METHODS

2.1 INTRODUCTION

This chapter presents a theoretical review of numerical integration methods. The characteristics of each method such as convergence, stability and explicit or implicit properties are discussed. The suitability of the methods used in practical simulators is validated.

What's more, there are several methods for formulating circuit equations. The most commonly used methods are *nodal* or *modified-augmented-nodal* analysis [23] [25] and *state-space*. Both methods can be implemented using numerical solution techniques offering various advantages within mathematically explicable limitations.

2.2 NUMERICAL INTEGRATION

Circuits and related control systems must be solved in frequency-domain for steady-state conditions and in time-domain for transient analysis. In time-domain, it needs a numerical solution for a set of differential equations. Generally speaking, it needs the solution for an ordinary differential equation (ODE) system given by

$$\frac{dx}{dt} = f(x,t)$$

$$x(0) = x_0 \tag{2.1}$$

2.2.1 Trapezoidal integration

Trapezoidal rule is among the most popular numerical integration techniques. It is used in large-scale circuit analysis software packages such as EMTP and SPICE. At a given time-point t and with a given time-step Δt, the trapezoidal method for equation (2.1) is given by

$$x_t = x_{t-\Delta t} + \frac{\Delta t}{2} \left[f_t - f_{t-\Delta t} \right] \tag{2.2}$$

or

$$x_{k-1} = x_k - \frac{\Delta t}{2} \left[f_k - f_{k-1} \right] \tag{2.3}$$

If equation (2.1) is replaced into (2.3):

$$x_{k-1} = x_k - \frac{\Delta t}{2} \left[\dot{x}_k - \dot{x}_{k-1} \right] \tag{2.4}$$

$$x_{k-1} = x_k - \frac{\Delta t_k}{2} \left[\dot{x}_{k-1} - \dot{x}_k \right] - \frac{\Delta t_k^3}{12} \frac{d^3 x(\varsigma)}{dt^3} \tag{2.5}$$

The time-step Δt can be fixed or variable. For both cases, the solution becomes available at discrete time-points and linear interpolation is used between these time-points. Topological discontinuities occurring between time-points encounter a delayed detection in the fixed time-step approach.

2.2.2 Other Taylor series based methods

As indicated in the previous section, trapezoidal integration can be derived from Taylor series expansion about the point $t = t_k$. Other methods can be created by manipulating the series expansion order.

2.2.2.1 Forward Euler

Forward Euler or first-order Taylor algorithm is given by:

$$x_{k-1} = x_k + \Delta t_k \dot{x}_k + \frac{\Delta t_k^2}{2} \frac{d^2 x(\varsigma)}{dt^2}$$

(2.6)

It corresponds to the first two terms of the Taylor series expansion. It is an explicit algorithm. The LTE (local truncation error) is quite large. Hence, to obtain reasonable accuracy, the time-step size must be made very small. As it will be shown later, it also has stability problems. This is why this method is seldom used.

2.2.2.2 Backward Euler

Euler Backward or Backward Euler integration is found by expanding both x_{k-1} and $\dot{x}_{k-1}$ about the time-point $t = t_k$:

$$x_{k-1} = x_k + \Delta t_k \dot{x}_{k-1} - \frac{\Delta t_k^2}{2} \frac{d^2 x(\varsigma)}{dt^2}$$

(2.7)

As the trapezoidal method. Backward Euler is an implicit algorithm since it yields a relation between x_{k-1} and $\dot{x}_{k-1}$. It is noticed that when a halved fixed time-step is used and the LTE is omitted, this equation becomes:

$$x_{k-1} = x_k + \frac{\Delta t}{2}\dot{x}_{k-1} \tag{2.8}$$

and differs from the trapezoidal method equation (2.4) only by missing the term $\frac{\Delta t}{2}\dot{x}_k$.

Which indicates that switching from trapezoidal to Backward Euler can be achieved very efficiently. This property can be exploited for initializing or reinitializing the trapezoidal integration method.

2.2.3 Regions of stability

According to equations (2.6) and (2.7) the Forward Euler and Backward Euler methods have an LTE term of equal magnitude. However, these two methods have significantly different stability properties. To study stability properties it is convenient to use a simple test equation:

$$\dot{x} = \lambda x \tag{2.9}$$

with the exact solution given by

$$\dot{x} = x_0 e^{(\lambda t)} \tag{2.10}$$

If the eigenvalue λ has a real negative part then equation (2.9) is stable. If the exact solution is stable, it is required that the numerical solution is also stable.

The solution of (2.9) with the Forward Euler constant time-step method is

$$x_{k-1} = x_k \left[1 + \Delta t \lambda \right] \tag{2.11}$$

which reduces to

$$x_k = x_0 \left[1 + \Delta t \lambda \right]^k \tag{2.12}$$

When the eigenvalue is real and negative, then the Forward Euler method is stable only if $x_k \rightarrow 0$ for $k \rightarrow \infty$, and necessitates:

$$\left| 1 + \Delta t \lambda \right| \leq 1 \tag{2.13}$$

$$-2 \leq \Delta t \lambda \leq 0 \tag{2.14}$$

In a more general sense the constraint equation is:

$$\left(1 + \mathrm{Re}\left\{ \Delta t \lambda \right\} \right)^2 + \left(\mathrm{Im}\left\{ \Delta t \lambda \right\} \right)^2 \leq 1 \tag{2.15}$$

and describes the stability region shown in Fig 2.1.
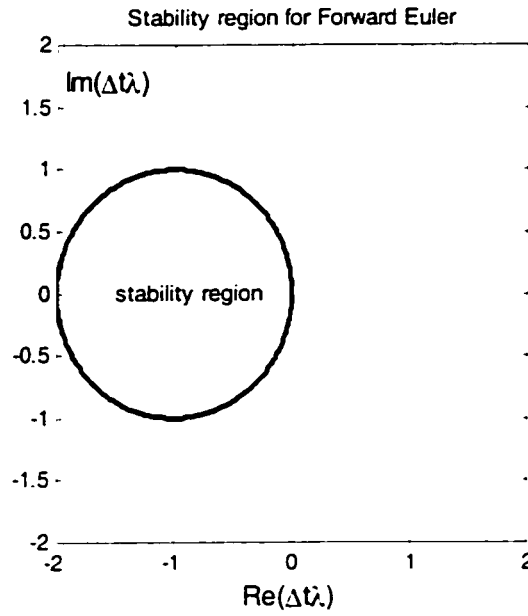
Fig 2.1   Stability region of Forward Euler algorithm

When equation (2.9) is solved with the Backward Euler method it gives:

$$x_{k+1} = x_k \left[1 - \Delta t \lambda\right]^{-1} \qquad (2.16)$$

and reduces to:

$$x_k = x_0 \left[1 - \Delta t \lambda\right]^{-1} \qquad (2.17)$$

The stability region is now given by:

$$\left(1 - \mathrm{Re}\left\{\Delta t \lambda\right\}\right)^2 + \left(\mathrm{Im}\left\{\Delta t \lambda\right\}\right)^2 \leq 1 \qquad (2.18)$$

and shown in Fig 2.2. It appears that contrary to Forward Euler, Backward Euler is stable for any time-step value.
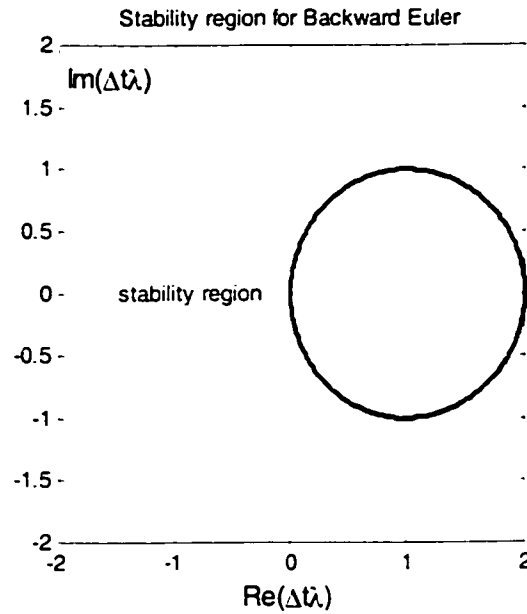
Fig 2.2   Stability region for Backward Euler algorithm

An integration algorithm is A-stable if its region of stability includes the entire left-hand side of the $\Delta t\lambda$ plane. Practical differential equations can be solved using stiffly stable algorithms. A numerical integration algorithm is stiffly stable if the algorithm is stable when the time-step approaches large values.

When trapezoidal integration is applied to solve equation (2.9) the following relation is obtained:

$$x_{k+1} = x_k \left| \frac{1 + \dfrac{\Delta t\lambda}{2}}{1 - \dfrac{\Delta t\lambda}{2}} \right| \tag{2.19}$$

It is simplified to become:

$$x_k = x_0 \left[\frac{1 + \frac{\Delta t \lambda}{2}}{1 - \frac{\Delta t \lambda}{2}} \right]^k \tag{2.20}$$

Therefore the stability region is the entire left-hand side plane given by:

$$\text{Re}\left\{\Delta t \lambda\right\} \leq 0 \tag{2.21}$$

It means that trapezoidal integration is stable if the exact solution is stable and unstable if the exact solution is unstable. It is an A-stable method.

It is noticed that if $|\Delta t \lambda| > 2$ then the numerator in equation (2.20) is negative and x_k is positive for even values of k and negative for odd values of k. The solution oscillates around the correct solution. In practical cases, oscillations will occur when a state variable (inductance current or capacitor voltage) encounters a discontinuity. An efficient approach in such situations is to reinitialize the trapezoidal method using the previously described halved time-step Backward Euler method.

2.3 NODAL OR MODIFIED-AUGMENTED-NODAL ANALYSIS

The standard nodal analysis is based on the Kirchoff law:

$$\mathbf{Y_n V_n = I_n} \tag{2.22}$$

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More sophistication is available in a *modified-augmented-nodal* analysis [23] [25] to account for the presence of generalized nodal relations, such as voltage sources and switches, and branch type relations such as an ideal transformer. The main system of equations in both time-domain and steady-state is given by:

$$
\begin{bmatrix}
\mathbf{Y_n} & \mathbf{V_{adj}^t} & \mathbf{D_{bdepc}} & \mathbf{S_{adj}^t} \\
\mathbf{V_{adj}} & 0 & 0 & 0 \\
\mathbf{D_{bdepr}} & 0 & 0 & 0 \\
\mathbf{S_{adj}} & 0 & 0 & \mathbf{S_0}
\end{bmatrix}
\begin{bmatrix}
\mathbf{V_n} \\
\mathbf{I_{V_s}} \\
\mathbf{I_{V_d}} \\
\mathbf{I_S}
\end{bmatrix}
=
\begin{bmatrix}
\mathbf{I_n} \\
\mathbf{V_s} \\
0 \\
0
\end{bmatrix}
\tag{2.23}
$$

where $\mathbf{Y_n}$ is the linear network admittance matrix, non-symmetric

$\quad$ $\mathbf{V_{adj}}$ is the voltage source adjacency matrix, for all voltages source types

$\quad$ $\mathbf{D_{bdepr}}$ and $\mathbf{D_{bdepc}}$ (row and column contribution matrices) are used for holding branch dependent relations

$\quad$ $\mathbf{S_{adj}}$ is the adjacency matrix of closed switch type devices

$\quad$ $\mathbf{S_0}$ is a diagonal and unitary matrix for open switch type devices

$\quad$ $\mathbf{V_n}$ is the vector of unknown node voltages

$\quad$ $\mathbf{I_{V_s}}$ is the vector of unknown voltage source currents

$\quad$ $\mathbf{I_{V_d}}$ is the vector of unknown currents in dependent voltage source branches

$\quad$ $\mathbf{I_S}$ is the vector of unknown switch currents

$\quad$ $\mathbf{I_n}$ is the vector of known nodal current injections

$\quad$ $\mathbf{V_s}$ is the vector of known voltage sources

In steady-state it is a complex system and in time-domain it is a real and discrete system.

The time-domain representation is more complex. It requires circuit discretization for a chosen integration method. Programs such as EMTP (Electromagnetic Transients Program) use trapezoidal integration as the main integration method and halved time-step Backward Euler for handling discontinuities. Using the trapezoidal method as the main algorithm, is justified by its increased precision.

The inductor equation $v_{km} = L\dfrac{di_{km}}{dt}$ is discredited with trapezoidal algorithm equation (2.4) to become:

$$i_{km_t} = \frac{\Delta t}{2L}v_{km_t} + \frac{\Delta t}{2L}v_{km_{t-\Delta t}} + i_{km_{t-\Delta t}} \tag{2.24}$$

When Backward Euler (see equation (2.8)) is used:

$$i_{km_t} = \frac{\Delta t}{2L}v_{km_t} + i_{km_{t-\Delta t/2}} \tag{2.25}$$

The schematic representation for an inductor is shown in Fig 2.3 where i_{Lh} is the history current found at the previous solution time-point (with trapezoidal algorithm).

$$i_{Lh} = \frac{\Delta t}{2L}v_{km_{t-\Delta t}} + i_{km_{t-\Delta t}} \tag{2.26}$$

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For the capacitor equation $i_{km} = C \dfrac{dv_{km}}{dt}$, with trapezoidal integration

$$i_{km_t} = \frac{2C}{\Delta t} v_{km_t} - \frac{2C}{\Delta t} v_{km_{t-\Delta t}} - i_{km_{t-\Delta t}} \qquad (2.27)$$

and with Backward Euler integration

$$i_{km_t} = \frac{2C}{\Delta t} v_{km_t} - \frac{2C}{\Delta t} v_{km_{t-\Delta t/2}} \qquad (2.28)$$

A resistive circuit similar to the one in Fig 2.3 can be drawn for the capacitor.
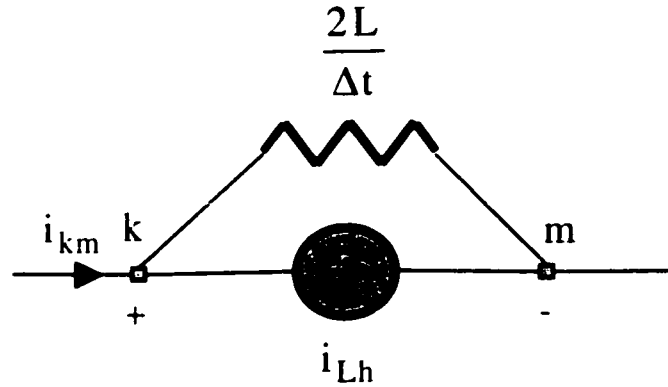
Fig 2.3   The discrete inductance model

It is also feasible to create a combined RLC branch model. If i_{km_t} is the RLC branch current then:

$$i_{km_t} = G_{RLC} v_{km_t} + i_{RLCh_t} \qquad (2.29)$$

Where

$$G_{RLC} = 1/\left(R + \frac{2L}{\Delta t} + \frac{\Delta t}{2C}\right) \qquad (2.30)$$

For trapezoidal integration:

$$i_{RLCh_t} = G_{RLC}\left[2v_{Lkm_{t-\Delta t}} - v_{km_{t-\Delta t}} + \left(\frac{2L}{\Delta t} + R - \frac{\Delta t}{2C}\right)i_{km_{t-\Delta t}}\right] \qquad (2.31)$$

$$v_{Lkm_{t-\Delta t}} = \frac{2L}{\Delta t}i_{km_{t-\Delta t}} - \frac{2L}{\Delta t}i_{km_{t-2\Delta t}} - v_{Lkm_{t-2\Delta t}} \qquad (2.32)$$

For Backward Euler integration:

$$i_{RLCh_t} = G_{RLC}\left[v_{Lkm_{t-\Delta t/2}} - v_{km_{t-\Delta t/2}} + \left(\frac{2L}{\Delta t} + R\right)i_{km_{t-\Delta t/2}}\right] \qquad (2.33)$$

$$v_{Lkm_{t-\Delta t/2}} = \frac{2L}{\Delta t}i_{km_{t-\Delta t/2}} - \frac{2L}{\Delta t}i_{km_{t-\Delta t}} \qquad (2.34)$$

2.4 STATE-SPACE EQUATIONS

An arbitrary circuit can be described through state-variable equations:

$$\dot{x} = Ax + Bu \qquad (2.35)$$

And the output equation:

$$y = Cx + Du \qquad (2.36)$$

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Where **x** is the vector of state variables, **u** is the vector of sources and **y** is the vector of outputs.

Applications of using state-space formulation have been succeeded to solve large-scale networks.

The automatic generation of state equations is not simple. It requires the knowledge of the circuit proper-tree to determine the state variables and possible dependencies among them. We don't mention this method here in detail because of its well-known drawbacks [23]:

❏ Problems in representing nonlinear functions.

❏ Problems in assembling the system of equation for arbitrary topologies.

❏ Problems for reformulating equations at topological changes.

2.5 CONCLUSIONS

This chapter has presented a brief summary on the currently available basic techniques for the simulation of transients. At this time, the well-known trapezoidal integration technique remains the most efficient for solving systems of ordinary differential equations of electrical networks. On the other hand, the modified-augmented-nodal analysis is relatively new. It has replaced the nodal analysis formulation and the state-space equation method in MATTRAN [23] [25] and EMTPRV [26]. The new interpolation-extrapolation technique presented in this thesis has been implemented and tested in these two packages.

CHAPTER 3

EVALUATION OF INTERPOLATION TECHNIQUES

3.1 INTRODUCTION

The objective of this chapter is to provide a survey and a critical evaluation of available interpolation techniques for the treatment of discontinuities occurring during topological changes.

The currently available techniques are interpolation in EMTDC [7] [13], NETOMAC [2] and HYPERSIM [9]. The CDA method is not an interpolation technique, but it has the ability to eliminate numerical oscillation. Some other methods, not discussed here, are related to real-time simulations [10] [14]. They have inherent constraints (in order to coincide with time mesh, they always have low accuracy) that are not applicable to the case of non real-time simulations.

3.2 SURVEY OF EXISTING ALGORITHMS

3.2.1 Methodology

Various methods are studied using basic diagrams of the type shown in Fig 3.1. This figure displays the evolution of i_{sw}, the current of a forced turn-off switch such as an IGBT.

The proposed approach for visualizing an interpolation technique is to present the switching device current (i_{sw}) trajectory in conjunction with the various solution time-points. The algorithm should be able to solve equally well the forced and natural commutation conditions. A diagram for the forced turn-off (GTO, for example) case is shown in Fig 3.1. A solution is normally taken from the time-point t to $t + \Delta t$. A discontinuity due to turn-off is encountered when moving to $t + 2\Delta t$. The difference with a thyristor is that the current between points 0 and 1 cannot be assumed to be linear (shown by the dashed line). If the solved system at each time-point is expressed through generic nodal analysis ($\mathbf{YV = I}$) then an interpolated solution can be found at t_d^-. The dotted trajectory represents the case of natural commutation. The dotted vertical lines are used here to denote the original time-mesh.
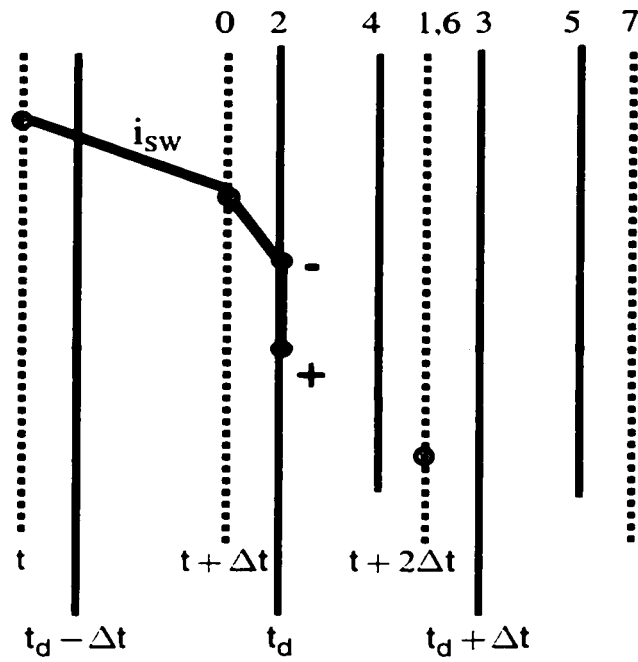
Fig 3.1 Current trajectory and interpolation for forced turn-off

3.2.2 The EMTDC method

This method works only for the natural commutation cases.
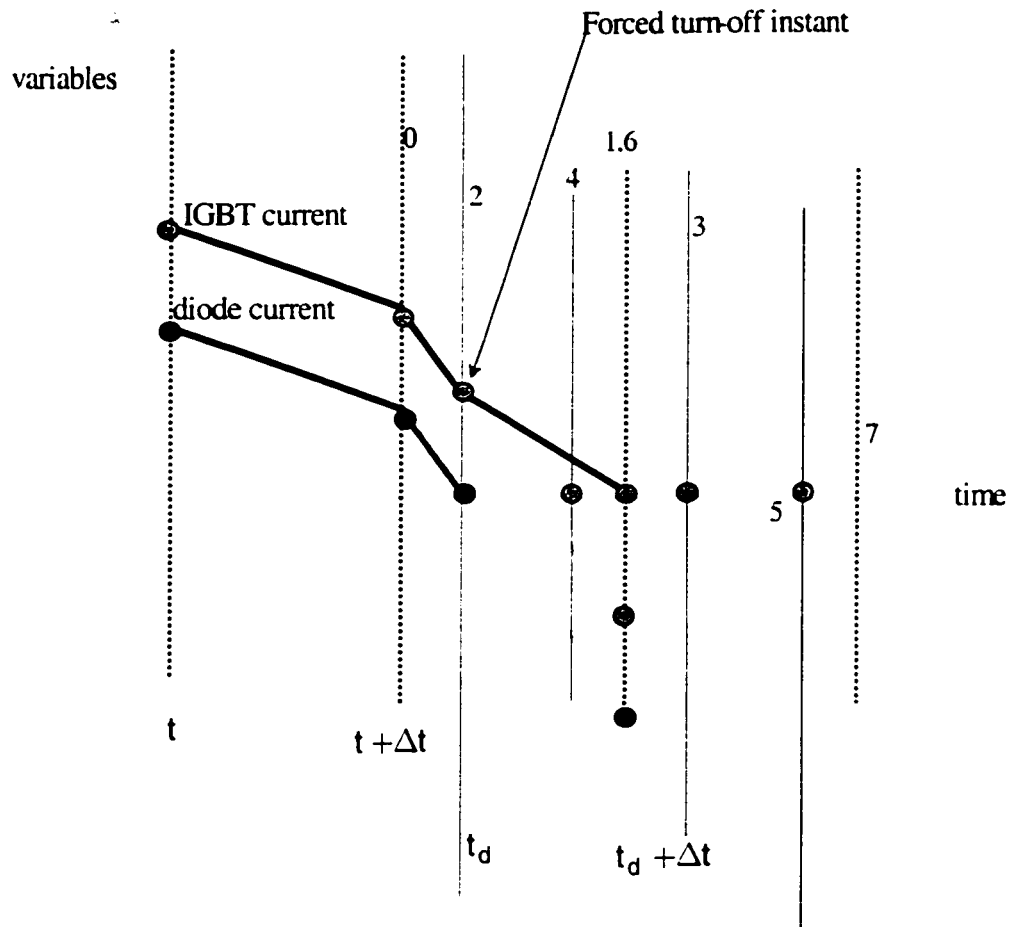
Fig 3.2 EMTDC algorithm for solving discontinuity and for re-initialization

The complete algorithm is given by the following steps.

1. Interpolate to find t_d (point2).

2. Find V_n at t_d using interpolation.

3. Prepare history terms for $t_d + \Delta t$.

4. Recalculate Y_n for the new switch status.

5. Find the solution at $t_d + \Delta t$ (point 3).

6. Check with status changes at $t_d + \Delta t$. If at least one switch has changed status then go back to step 1 and repeat.

7. Perform an extra interpolation to find the solution at time-point 4. This technique is used to eliminate numerical oscillation [7]. It will be explained in the following paragraph.

8. Perform a normal solution to move to time-point 5.

9. Perform an extra interpolation to go back to the original time-mesh point 6.

The method used in step 7 is explained as follows. If a numerical oscillation condition occurs, the all quantities at time-point 3 are assumed to be the negative of those at time – point 2. Interpolation will make them equal to zero.

This method is designed only for natural commutation, since in the forced commutation case the current can be interrupted abruptly. For the IGBT trajectory, it results in delayed interception and will create extra errors in PWM converters.

This problem has been recognized in [13] and a new method has been suggested.

It is summarized in [13]. The method performs two solutions at t_d, one at t_d^- with the switch closed (Y_n^-) and one at t_d^+ with the switch open (Y_n^+). The solution then moves to the time-point 3 and the following steps are similar to the previous algorithm.
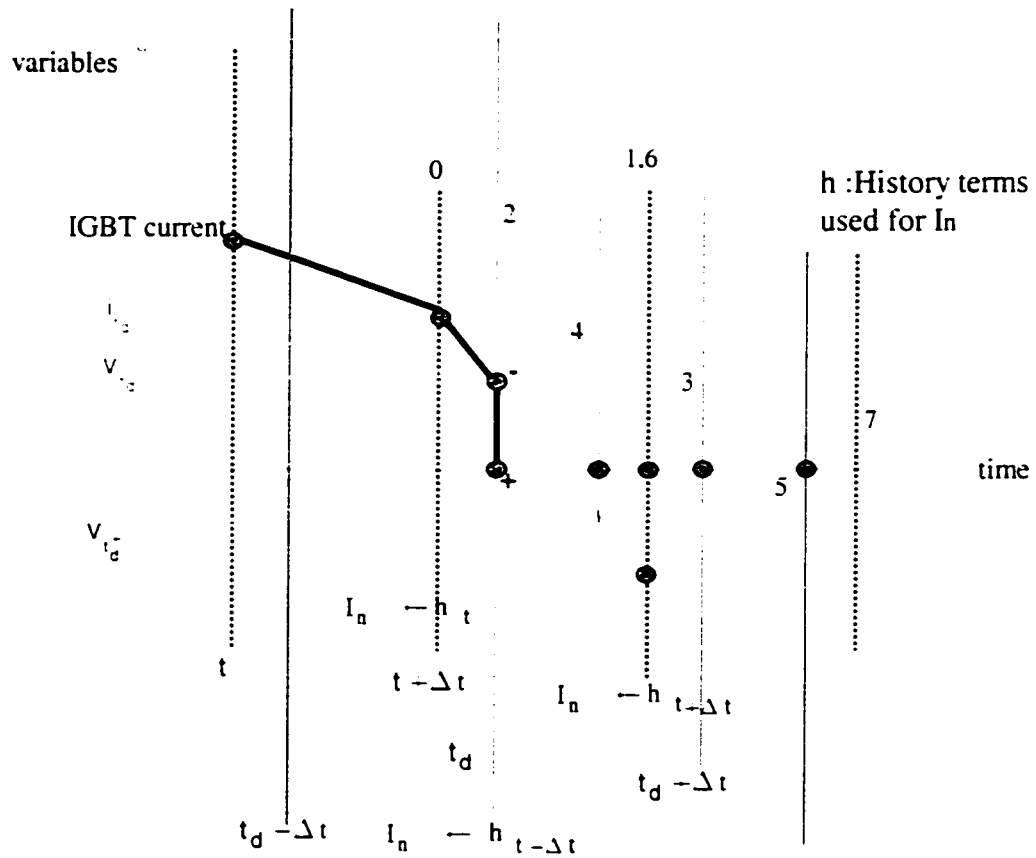
Fig 3.3   Modified EMTDC algorithm for forced commutation

For the solution at t_d^- it is assumed that $\mathbf{I_n}^-$ is equal to the interpolated $\mathbf{I_n}^-$. Although it may be acceptable in some practical cases within integration time-step limits, this assumption is questionable, since a discontinuity has occurred and the history $h_{t-\Delta t}^-$ leading to the solution at t_d^- should be different from the history $h_{t-\Delta t}^-$ leading to the solution at t_d^-. There is no state variable continuity criterion.

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3.2.3 The NETOMAC method

Extra solution

variables

h : History terms
used for In

time

$I_n \leftarrow h_t$

$t + \Delta t$

t

$t_d - \Delta$

$I_n \leftarrow h_{t-\Delta t}$

t_d

$I_n \leftarrow h_{t-\Delta t}$

$I_n \leftarrow h_d$

$t_d + \Delta t$

$t_d + \dfrac{\Delta t}{2}$
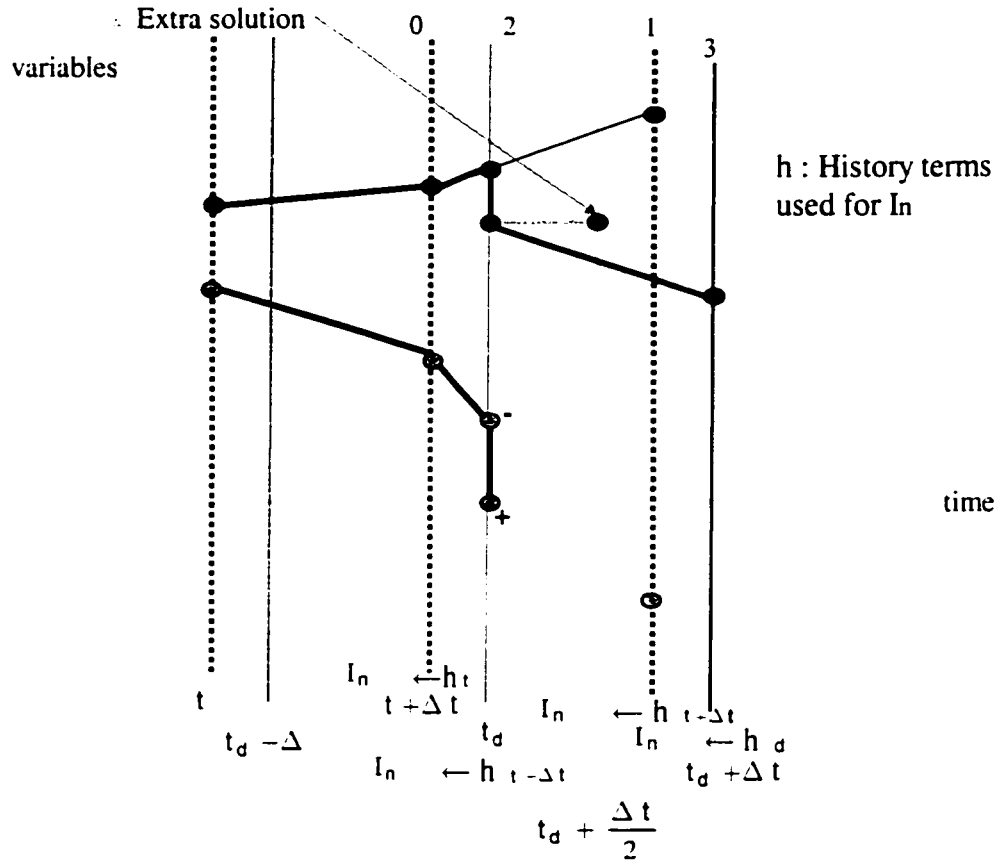
Fig 3.4   NETOMAC algorithm for solving discontinuity and for re-initialization

NETOMAC [2] finds t_d using interpolation on V_n at t_d. The algorithm steps are:

1. Interpolate to find t_d.

2. Find the new Y_n (after switching) and prepare history terms for performing the next step solutions.

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3. Find an exploratory solution at $t_d + \dfrac{\Delta t}{2}$ using Backward Euler rule. Since the inductance current moves linearly, this extra solution allows finding the voltage for the re-initialization of the solution at t_d. A similar reasoning is applied to the capacitance current.

The following operations are applicable:

$$i_L(t_d^{\cdot}) = i_L(t_d^{-})$$ (3.1)

$$v_C(t_d^{\cdot}) = v_C(t_d^{-})$$ (3.2)

The re-initialization equations are:

$$i_C(t_d + \frac{\Delta t}{2}) = i_{\cdot}(t_d^{-})$$ (3.3)

$$v_L(t_d + \frac{\Delta t}{2}) = v_L(t_d^{-})$$ (3.4)

where $i_L(t_d^{-})$ is found from interpolation and $i_L(t_d^{\cdot}) = i_L(t_d^{-})$ ensures state variable continuity. A similar equation can be written for the capacitor. An extra interpolation can be taken to resynchronize with the original time-mesh, but it is less important for non-real-time simulators and the extra computational burden can be avoided. Numerical oscillations are automatically eliminated during the re-initialization procedure and due to Backward Euler usage.

The main limitation of this method is that it does not provide a method for finding nodal

voltage at t_d^*. The assumption of equation (3.3) (3.4) is questionable.

3.2.4 The EMTP CDA

The CDA [5] [6] method has been designed only for natural commutation cases. It is

illustrated for the inductance current interruption in Fig 3.5.

When a current interruption is detected (current becoming negative), the CDA method

performs two extra Backward Euler solutions.

$$i_{t_d + \Delta t/2} = \frac{\Delta t}{2L} v_{t_d + \Delta t/2} + i_{t_d} = 0 \tag{3.5}$$

$$v_{t_d + \Delta t/2} = -\frac{2L}{\Delta t} i_{t_d} \tag{3.6}$$

$$0 = v_{t_d + \Delta t} \tag{3.7}$$

This method eliminates the numerical oscillations.
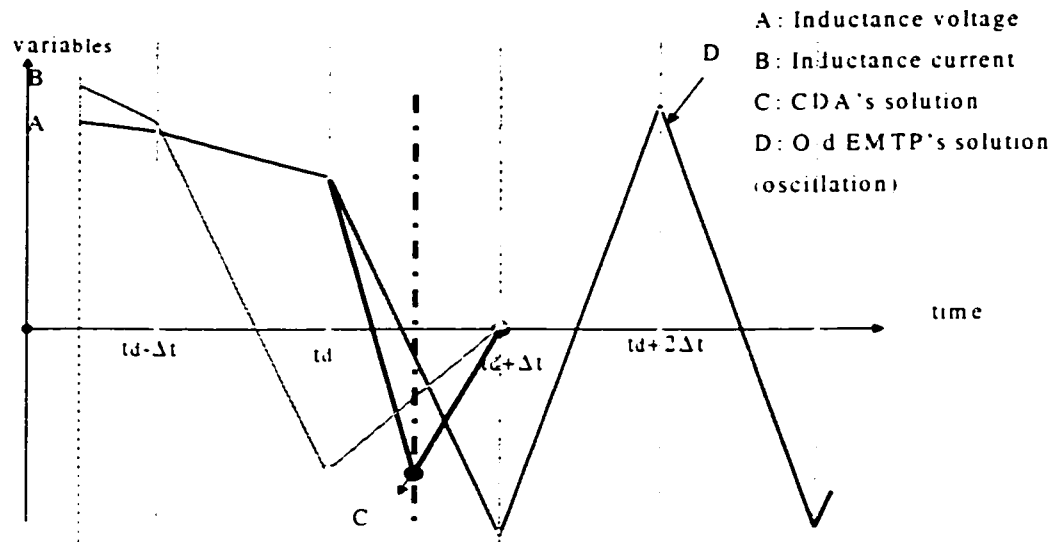
Fig 3.5   The CDA method

The CDA algorithm does not offer a complete solution. On one hand, it cannot find the exact turn-on instant of line commutated switches or extinction instant of forced commutated switches. On the other hand, CDA cannot calculate the re-initialization values of state variables after discontinuities. Furthermore, CDA cannot account for instantaneous switching conditions.

3.2.5 The HYPERSIM method
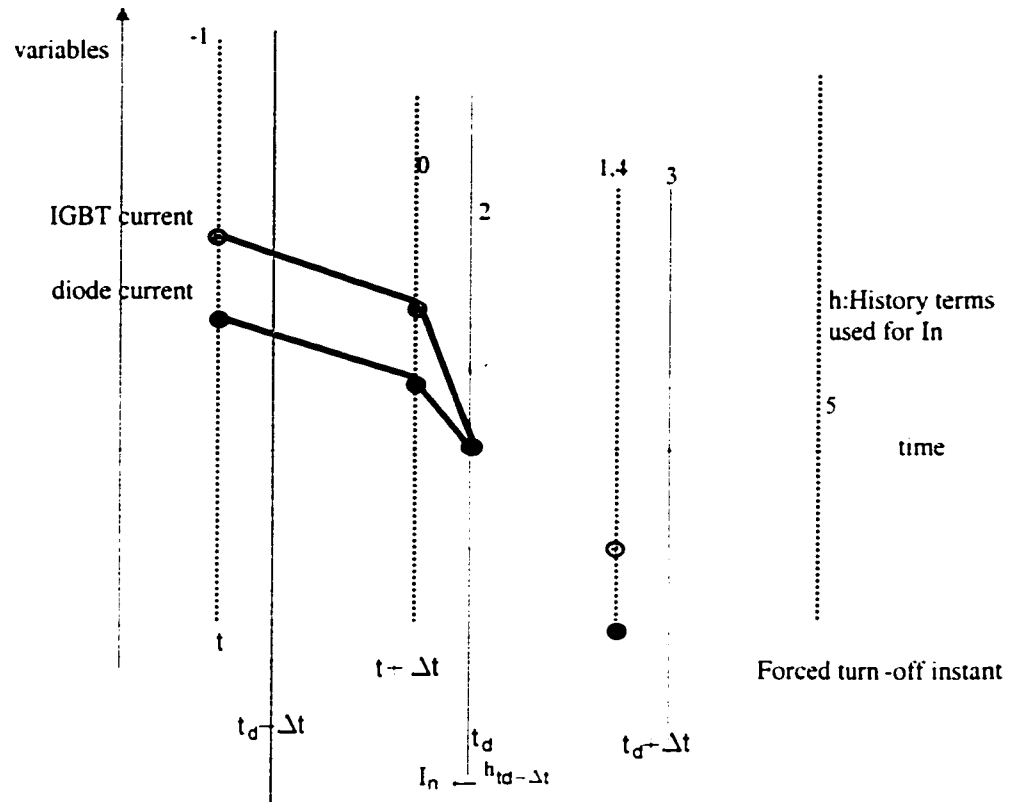
Fig 3.6   HYPERSIM algorithm for solving discontinuity and for re-initialization

The HYPERSIM [9] method is limited to natural commutation.

The algorithm is given by the following steps:

1. Interpolate to find t_d (point2).

2. Find V_n at t_d using interpolation.

3. Interpolate history terms (between point -1 and 0) for t_d^+.

4. Recalculate Y_n for the new switch status.

5. Formulate new I_n^+ with history terms getting in step 3.

6. Find the solution at t_d^- (point 2).

7. Perform a normal solution to move to $t_d + \Delta t$.

8. Perform an interpolation (between points 2 and 3) to go back to the original time-mesh point 4.

The HYPERSIM method is to move the exact switching time one time-step forward. When there are multiple switching operations happening in one time-step, it would cause the wrong simulation results. Let us take an example. In Fig 3.6, if there is another switching happened between point 2 and point 4, HYPERSIM still uses the history terms at point -1 and 0 to get the history terms needed by the new switching operation. In fact, it should use the new history terms, which come from the new network after switching operation at point 4.

3.2.6 Complete continuity method
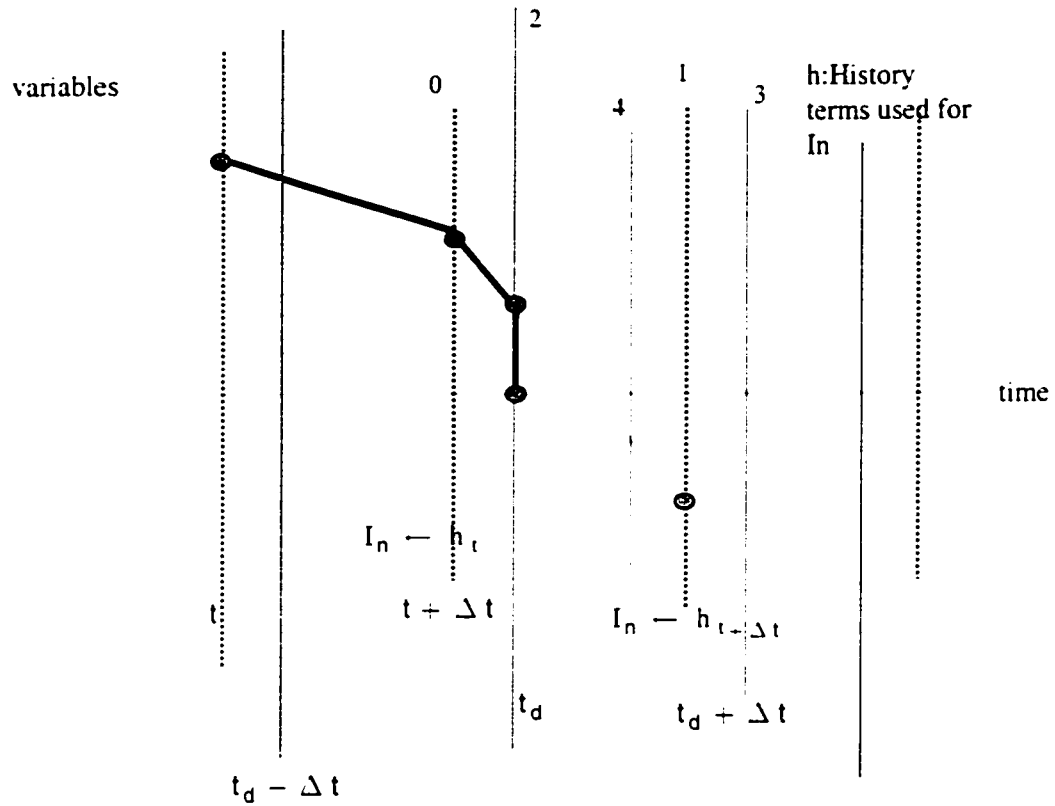
Fig 3.7   Complete continuity method

This method is presented in [8]. It also starts by interpolating for finding t_d and the solutions at t_d. To enforce perfect state-variable continuation, this method formulates a new $\mathbf{Y_n}$ at t_d^- by replacing all capacitors by dc voltage sources and all inductances by dc current sources. The dc voltage and dc current values are taken from the solution at t_d^-.

The solution at t_d^- provides history for moving to the time-point 3 (see Fig 3.7). The idea appears appealing, but the capability to formulate the proposed $\mathbf{Y_n}^-$ for large scale

networks remains to be proven. Particularly difficult condition may arise for some specific models that cannot be replaced by dc voltage sources and current sources.

There is one more fundamental problem. It is illustrated in Fig 3.8. A simple case is shown in Fig 3.8 a. If the switch opens at t_d then its equivalent circuit at t_d^- becomes the one shown in Fig 3.8 b. Since the two inductances are not equal, their current sources are different and this circuit is inconsistent.
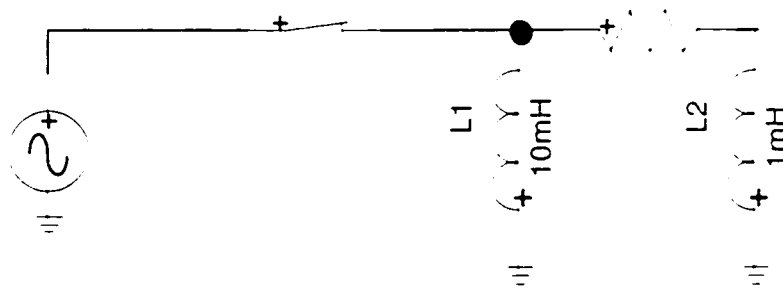
a)   A simple case
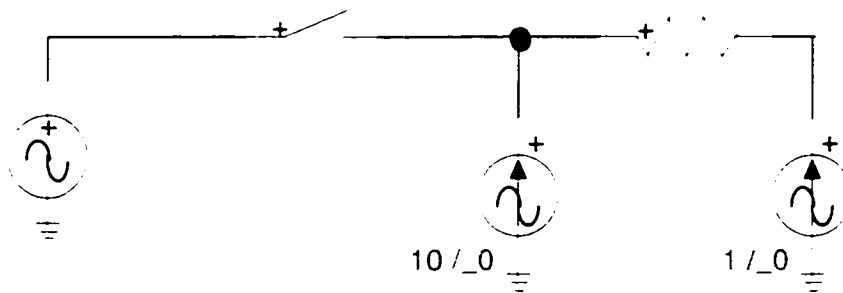
Fig 3.8 b)   Equivalent circuit of the case at discontinuity time-point t_d.

3.3   THE PROPOSED NEW APPROACH
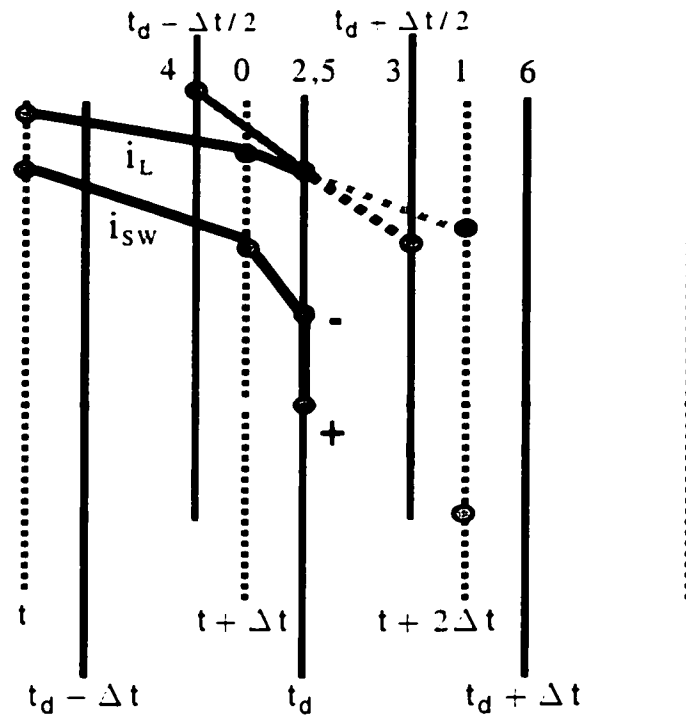
Fig 3.9   New algorithm for solving discontinuity and for re-initialization

This method has been implemented and tested in MATTRAN [23] [25] and EMTPRV [26]. A more general network is used in these software programs, described by:

$$Y_{aug} V_{aug} = I_{aug} \qquad (3.8)$$

3.3.1   Principle of the New Method

The method [27] proposed is based on [2]. It is illustrated in Fig 3.9, which shows, in addition to the switch current, the possible inductance current trajectory. A similar

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presentation can be made for a capacitor voltage. The overall algorithm steps (corresponding to the times described by the vertical time lines) are:

1. Find the normal time-mesh solution at $t + 2\Delta t$ and detect that a discontinuity has occurred.

2. Find the interpolated solution for state variables at t_d and the new system matrix $\mathbf{Y_{aug}}^\tau$.

3. Find the exploratory solution at $t_d + \dfrac{\Delta t}{2}$ using equation (3.9).

$$i_{L_{t_d - \Delta t/2}} = \frac{\Delta t}{2L} v_{L_{t_d - \Delta t/2}} + i_{L_{t_d -}} \qquad (3.9)$$

4. Extrapolate the solution for state variables at $t_d - \dfrac{\Delta t}{2}$. The extrapolated solution for i_L is:

$$i_{L_{t_d - \Delta t/2}} = 2i_{L_{t_d -}} - i_{L_{t_d + \Delta t/2}} \qquad (3.10)$$

5. Move from the time-point of step 4 back to the time-point 2 using Backward Euler:

$$\hat{i}_{L_{t_d}} = \frac{\Delta t}{2L} v_{L_{t_d -}} + i_{L_{t_d - \Delta t/2}} \qquad (3.11)$$

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6. Move from time-point 2 at t_d to $t_d + \Delta t$ using the trapezoidal integration equation.

3.3.2 Discussion on the New Method

NETOMAC uses the values at $t_d + \dfrac{\Delta t}{2}$ to be the initial conditions. The Modified EMTDC method calculates the solution at t_d^+ from t_d^-. From the viewpoint of mathematical approximation, these two approaches can get reasonable results if the time-step sufficiently small. However, when the time-step increases, the approximation is not valid. In NETOMAC the difference between the values at $t_d + \dfrac{\Delta t}{2}$ and t_d^+ will become too large. The Modified EMTDC approximation is simply not valid.

3.4 CONCLUSIONS

The method proposed in this thesis has the capability of predicting a value at t_d^+ closer to the exact solution, in addition to reinitializing the solution of history terms for the following time-point. The method however is based on the assumption of linear variation between the solved time-points of the trapezoidal method.

CHAPTER 4

TEST CASES

4.1   INTRODUCTION

This chapter presents the results of the implementation of the proposed method for a number of test cases designed to verify its performance and compare it with other available techniques.

Generally speaking, it is not necessary to present circuit with a large number of devices. In fact, the capability of a method to treat discontinuities can be better verified in simple circuit under controlled conditions.

4.2   SIMPLE SWITCHING SIMULATION
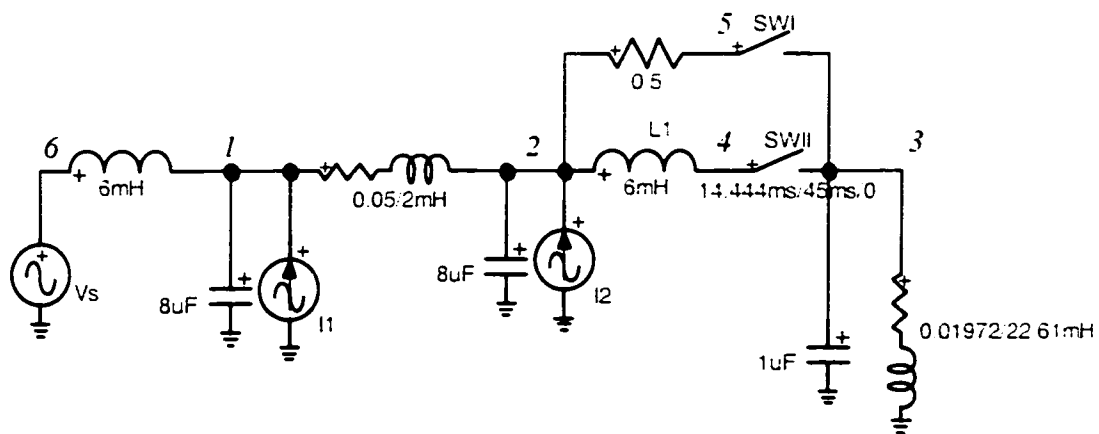
Fig 4.1   RLC model presentation

This circuit, Fig 4.1, is a simple example for analyzing the response during a normal switching operation. It creates both capacitor current and inductance voltage discontinuities.

At the beginning, the switches II and I are open. Switch I is connected between nodes 5 and 3. Switch II is connected between nodes 4 and 3. At time t_d, Switch II closes while Switch I remains open. The theoretical equations are:

$$v_{L1_{t_d}} = v_{2_{t_d}} - v_{4_{t_d}} = 0 ; \qquad (4.1)$$

$$v_{4_{t_d^-}} = v_{3_{t_d^-}} ; \qquad (4.2)$$

However, the voltage of node 3 is zero before closing Switch II. After closing Switch II, the voltage of node 3 remains zero because the capacitor voltage cannot jump instantaneously:

$$v_{3_{t_d}} = v_{3_{t_d^-}} = 0 ; \qquad (4.3)$$

$$i_{L1_{t_d}} = i_{L1_{t_d^-}} ; \qquad (4.4)$$

Generally speaking, the current of the inductance L1 cannot jump and the voltage of the capacitor cannot jump.

The following table and waveforms present a comparison between existing methods and the New Method. The theoretical solution is obtained using a very small time-step.

For example, if we use a large time-step ($\Delta t = 100\mu s$ considering close the switch II, the time period of the entire circuit is about $950\mu s$) when $t_d = 0.014444s$ (This t_d is selected to force interpolation), Switch I closes, at t_d^- :

	Theoretical solution	Modified EMTDC	NETOMAC	New Method
time-step	$1\mu s$	$100\mu s$	$100\mu s$	$100\mu s$
$V_{L1_{t_d}^-}$ (V)	35.4432	21.632	21.3799	34.0529
Error (%)	0	38.967	39.678	3.922

Table 4.1   Inductance voltage error for each method
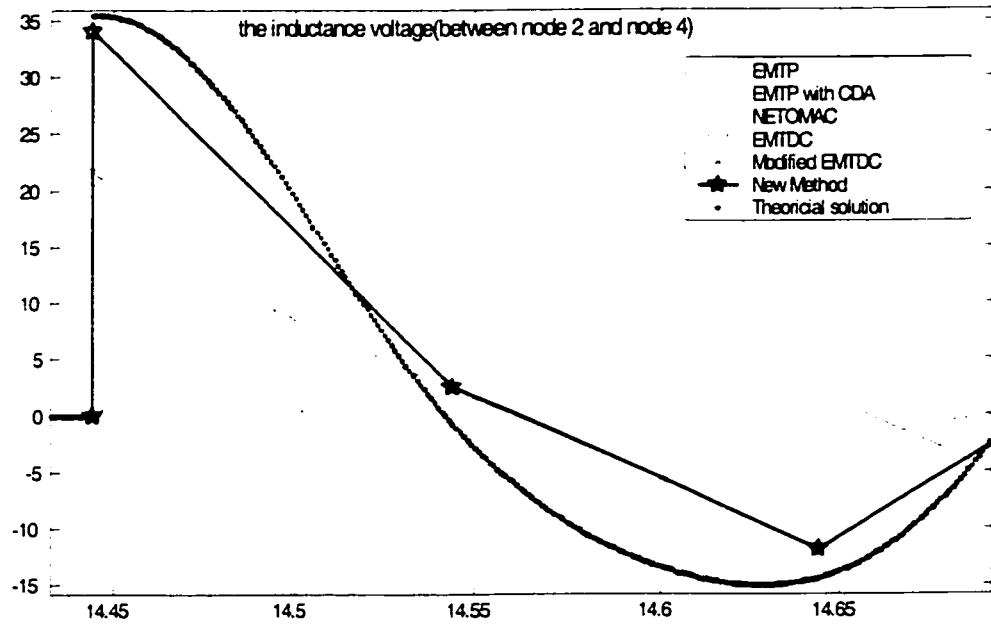
Fig 4.2   Inductance voltages at Switch II closing (x axis: ms; y axis: inductor voltage, in V)

Fig 4.2 shows the inductance voltage at switch closing time t_d. It is apparent that the New

Method obtains the best results.
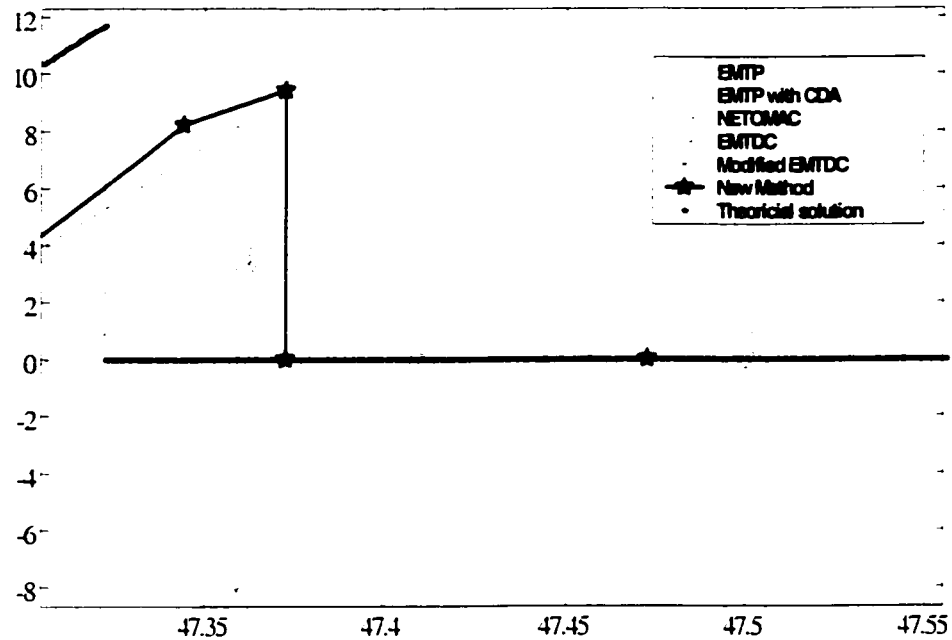
Fig 4.3   Inductance voltages at switch II opening (x axis: ms; y axis: inductor voltage, in V)

Fig 4.3 shows the inductance voltage at the switch opening time-point. The Switch II is

allowed to open after some delay and current crossing zero.

When Switch II opens, each technique finds a different switch opening time due to the

different current zero point. From Fig 4.3 we can see that modified EMTDC has a

negative jump. This result is caused by the numerical oscillations of the trapezoidal rule

and does not have any real meaning.

When $\Delta t = 10\mu s$, the simulated results will naturally get close to theoretical results.

From Fig 4.4, we can see the New Method matches the theoretical solution very well.

The other methods still show some errors.
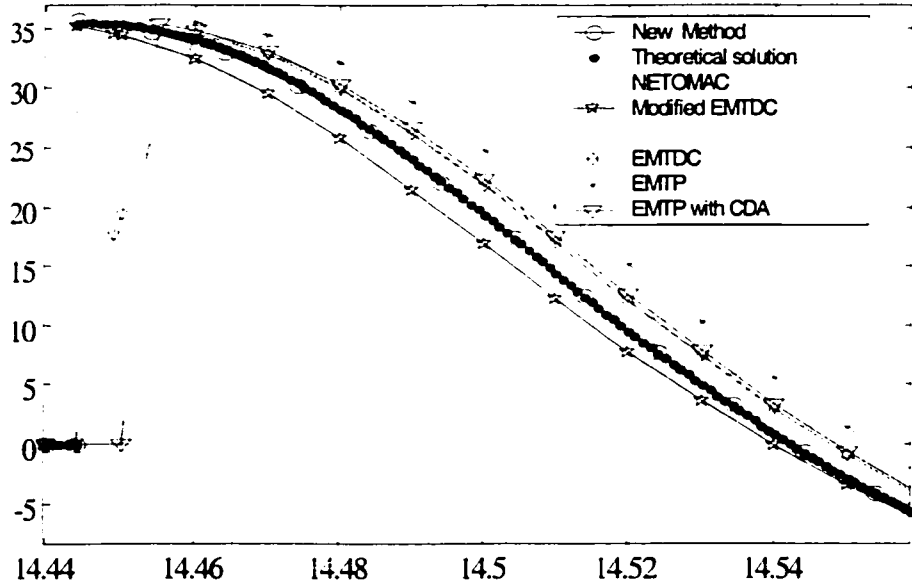
Fig 4.4   Simulation results comparisons (x axis: ms; y axis: inductor voltage, in V)

In the following tables, we vary the time-step from $10\mu s$ to $140\mu s$ to test the accuracy of

each method and co-relation with time-step.

	$10\mu s$	$20\mu s$	$30\mu s$	$40\mu s$	$50\mu s$	$60\mu s$	$70\mu s$
New Method (inductance voltage V)	34.849	35.688	36.675	37.382	37.174	36.584	36.972
NETOMAC solution	34.311	33.549	32.386	30.931	29.118	27.139	25.786
Modified EMTDC	34.400	33.703	32.569	31.157	29.591	27.965	26.710
Error between I and T (error percentage %)	1.6776	-0.690	-3.476	-5.471	-4.882	-3.218	-4.313
Error between N and T	3.1944	5.3449	8.6265	12.732	17.845	23.430	27.246
Error between M and T	2.9422	4.9104	8.1082	12.094	16.511	21.101	24.641

	80μs	90μs	100μs	110μs	120μs	130μs	140μs
New Method	37.983	36.047	34.053	33.550	33.969	29.654	28.654
NETOMAC solution	24.543	23.158	21.380	19.747	19.600	18.440	16.373
Modified EMTDC	24.829	23.400	21.632	20.923	19.687	19.120	18.001
Error between I and T	-7.167	-1.702	3.9226	5.3407	4.1590	16.335	19.156
Error between N and T	30.753	34.663	39.678	44.287	44.700	47.973	53.805
Error between M and T	29.947	33.978	38.967	40.967	44.454	46.055	49.213

(I is New Method, N is NETOMAC and M is Modified EMTDC, T is the theoretical solution)

Table 4.2   Error comparison among different algorithms (the values are the initial

inductance voltage L1 at t_d^-)
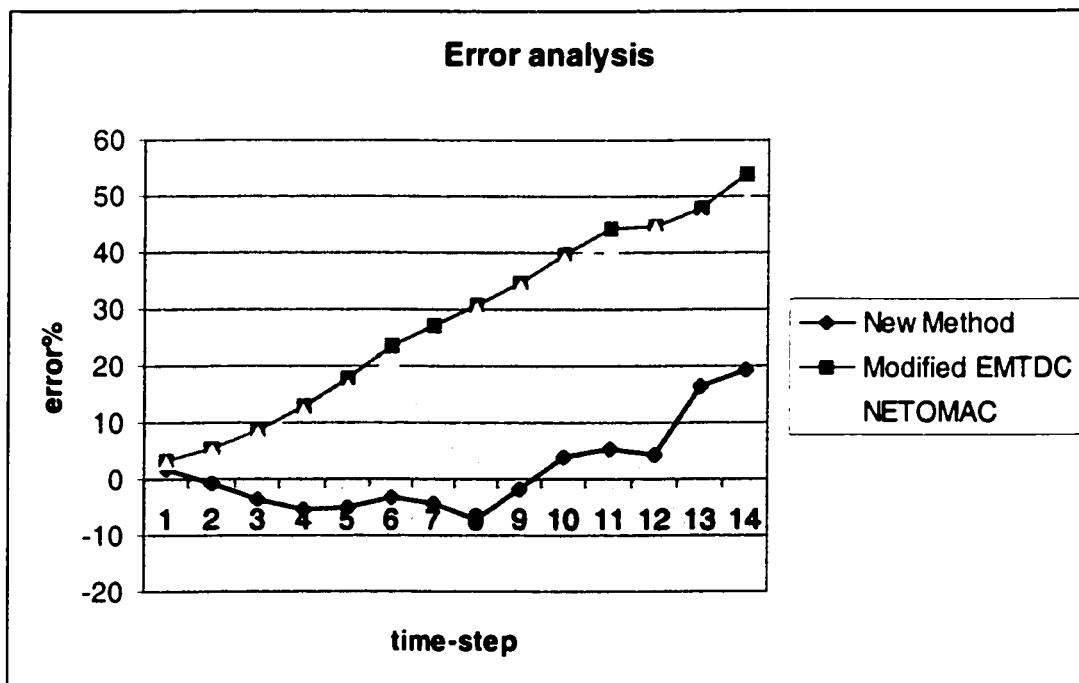
Fig 4.5   Relations between errors and time-steps(x axis: ×10ms ; y axis: error

percentage of inductor voltage)

Fig 4.5 shows the errors of Modified EMTDC and NETOMAC will build up linearly with the increase of time-step. The errors of the New Method don't change linearly. It is verified that the New Method is less time-step dependent.

4.3 POWER ELECTRONIC SWITCHES

4.3.1 Power semiconductor switch models

These switches, typically diodes, thyristors, GTOs and IGBTs can be simulated using a number of techniques, in increasing order of complexity and increasing simulation time [24]:

- ❑ Ideal switches: infinite resistance when open and zero resistance when closed. It requires the reformulation of network equations.

- ❑ Non-ideal switches (or quasi-ideal): used to obtain a more accurate representation, for example by taking into account forward voltage drop and resistance or turn-on and turn-off times. It is achieved by adding resistance, and capacitor in parallel and inductors in series with the ideal model.

- ❑ Physical models: these are based on the physical behavior of the switches and the associated equations derived from semiconductor physics. The level of details can become extremely high. These are physical intrinsic micro-models of the appropriate semiconductor technology, usually available (in applications based on SPICE) from a library of parts provided by various manufacturers.

The micro-models are not practical at the converter circuit and system levels. Power system simulators can provide acceptable results using the ideal and non-ideal switch models. For computational speed reasons, the fixed integration time-step remains the most popular choice. It must be implemented with an appropriate interpolation technique.

4.3.2 DC-DC buck-boost converter

DC-DC converters (see Fig 1.4) are used in regulated switch mode dc power supplies and in dc motor drive applications.

If the gate signal is a pulse of duty cycle D_1 of period T, the steady-state waveforms of the circuit in both continuous and discontinuous modes can be found from theoretical analysis.

The mean value model equations for the continuous mode are given by:

$$\frac{V_o}{V_i} = \frac{D_1}{1-D_1} = \frac{I_i}{I_o} \tag{4.5}$$

$$V_o = RI_o \tag{4.6}$$

$$I_L = 0.5D_1T\frac{V_i}{L} + i_{mn} \tag{4.7}$$

$$i_{mn} = \frac{1}{D_1}\left(I_s - D_1^2\frac{TV_i}{2L}\right) \tag{4.8}$$

The discontinuous mode equations are given by:

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$$\frac{v_o}{v_s} = \frac{D_1}{D_2} = \frac{i_s}{i_o} \qquad (4.9)$$

$$D_2 = \sqrt{\frac{2L}{RT}} \qquad (4.10)$$

$$I_L = 0.5 D_1 T \frac{V_s}{L} (D_1 + D_2) \qquad (4.11)$$

$$i_{max} = D_1 T \frac{V_s}{L} \qquad (4.12)$$

The general data is: $v_s = 8V, L = 0.01mH, C = 100\mu F, T = 1.0E - 0.5s, D_1 = 0.75$;

For the continuous mode:

$R = 8\Omega$; Initial conditions: $v_c = -24V, i_L = i_{min} = 9A$;

For the discontinuous mode:

$R = 80\Omega, D_2 = 0.16$; Initial conditions $v_c = -37.5V$

The theoretical quantities in the continuous mode are:

$$i_{min} = 9A; v_o = 24V; i_L = 12A; \qquad (4.13)$$

The theoretical quantities in the discontinuous mode are:

$$i_{max} = 6A; v_o = -37.95V; i_L = 2.7243A; \qquad (4.14)$$

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Fig 4.6 shows the continuous operating mode output voltage v_0. The forced commutated

switch is modeled as an ideal switch and the diode has a 0.7V voltage drop when

conducting and becomes an open circuit when turned-off. The expected theoretical mean

value of voltage output is -24V. The simulation starts by initializing the capacitor voltage

to -24V in order to achieve a faster steady state. EMTP is not shown here since it is

unable to provide a simultaneous switching solution and will fail completely. It appears

that due to the repetitive re-initialization and related errors, EMTDC and NETOMAC

find a different steady state. The actual mean value voltage found by the New Method is

-23.9875V (an error of 0.05%). NETOMAC and modified EMTDC find -24.315V and -

23.365V respectively. The New Method is also able to closely follow the theoretical

envelope and the superposition makes both waveforms almost indistinguishable. Fig 4.7

shows the detailed waveforms of output voltages. The error comparisons are shown in

Table 4.3. If the time-step is increased to 1μs then New Method's error is only 0.4%.
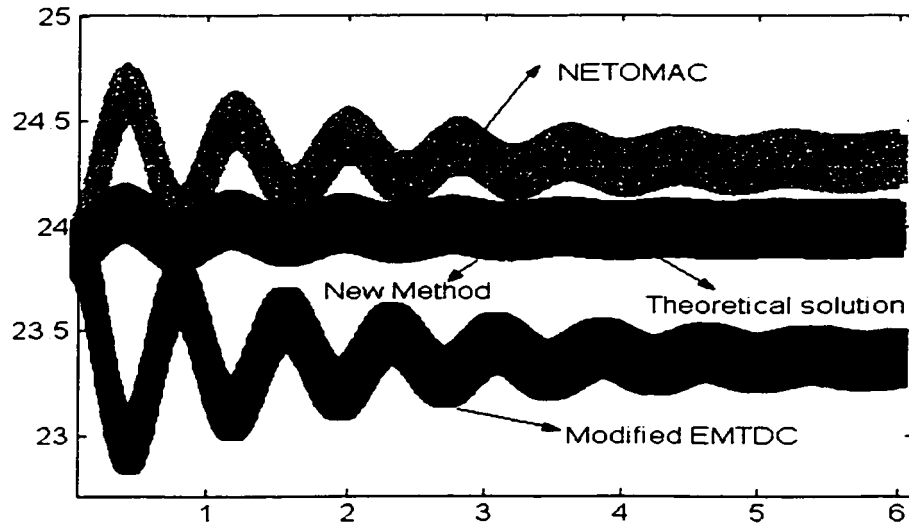
Fig 4.6 **Converter output voltage** $(-v_0)$**, continuous mode** $(\Delta t = 0.1\mu s$**, x axis: ms; y**

axis: output voltage, in V)
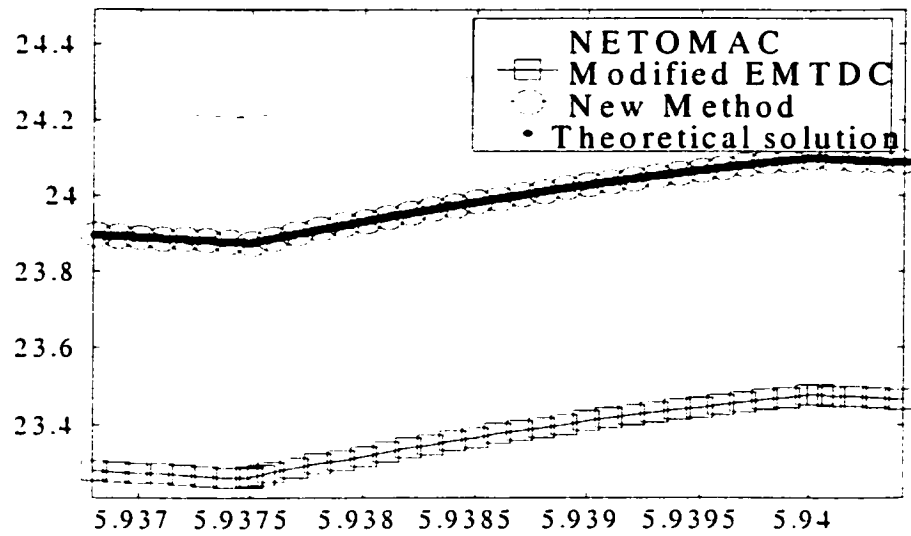
Fig 4.7 Detailed waveforms of Converter output voltage (x axis: ms; y axis:

output voltage, in V)

	Theoretical solution	Modified EMTDC	NETOMAC	New Method
v_s (V)	-24	-23.365	-24.315	-23.9875
Error (%)	0	2.646	1.3125	0.052

Table 4.3 Comparisons of output voltage

It must be noted that there are no numerical oscillations in Fig 4.6. What is shown is high frequency switching. The apparent modulation effect of some methods is due to the initial transients and errors in re-initialization, which cause errors in switching instants. It is impossible to achieve perfect steady state, especially at such high frequencies, but the New Method is the one that shows the best performance and enters steady state much faster.

Fig 4.8, Fig 4.9 and Fig 4.10 show the inductance current. The theoretical minimum

value is 9A. The New Method finds 8.9958A. The error comparisons are shown in Table

4.4. It is noticed here that modified EMTDC does not achieve current continuity.
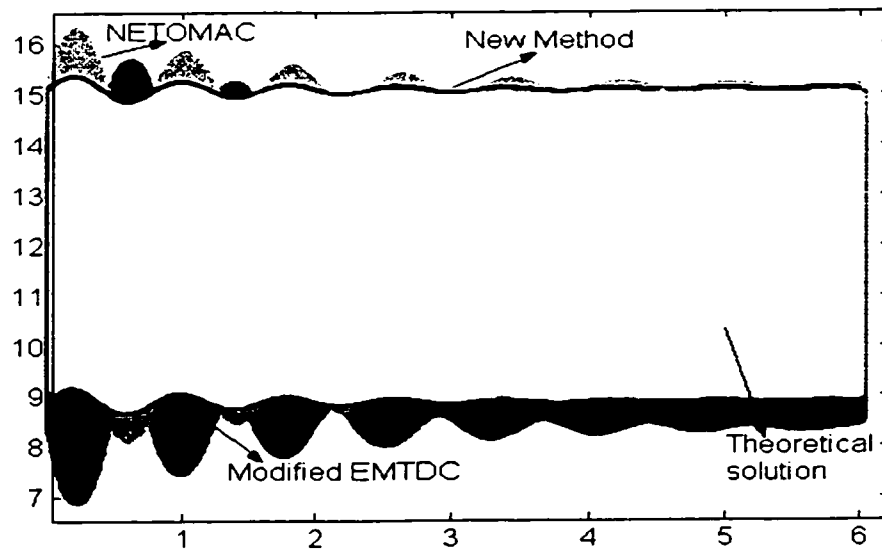
Fig 4.8 Converter inductance current, continuous mode ($\Delta t = 0.1\mu s$, x axis: ms; y

axis: inductor current, in A)
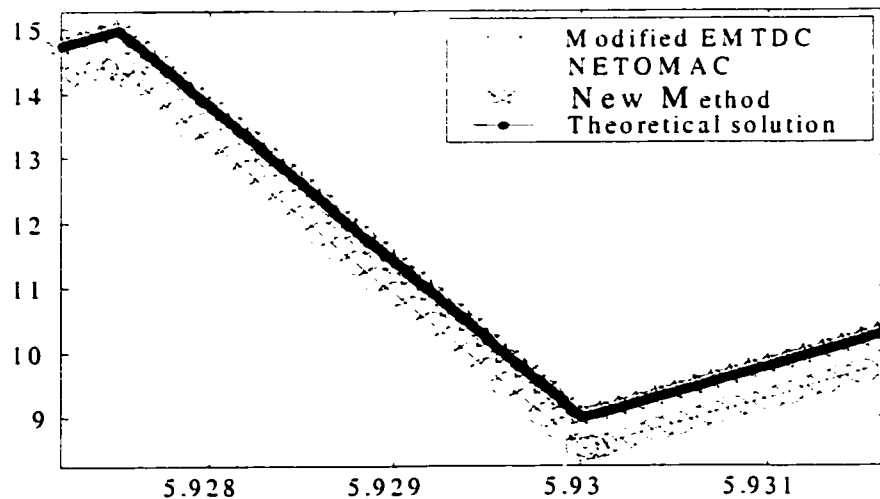
Fig 4.9 Detailed waveforms of Converter inductance current, continuous mode

(x axis: ms; y axis: inductor current, in A)
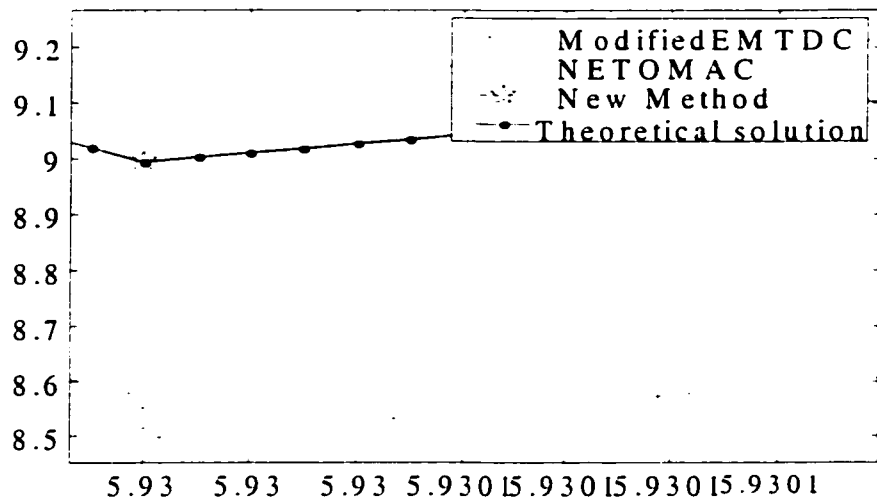
Fig 4.10   The enlargement waveforms of inductance current (x axis: ms; y axis:

inductor current, in A)

	Theoretical solution	Modified EMTDC	NETOMAC	New Method
i_{min} (A)	9	8.5	9.15	8.9958
Error (%)	0	5.56	1.67	0.047

Table 4.4   Comparisons of inductance current

The discontinuous mode is more complex due to the increased number of re-initializations. Simulation results are shown in Fig 4.11. The theoretical steady-state mean value voltage is −37.85V. The New Method finds −37.81V when it enters into steady state. NETOMAC finds −38.525V and modified EMTDC finds −37.74V . Table 4.5 shows the error comparisons of output voltage. A distinctive feature is the ability to maintain current continuity. Fig 4.12 compares currents at switching point. The New

Method results are very close to the theoretical solution. Table 4.6 shows the error comparisons of inductance current.

Fig 4.11   Output voltage comparison, discontinuous mode (x axis: ms; y axis:

output voltage, in V)

	Theoretical solution (when $t = 6\text{ms}$)	Modified EMTDC	NETOMAC	New Method
$v_s(V)$	-37.85	-37.74	-38.525	-37.81
Error (%)	0	0.29	1.78	0.1

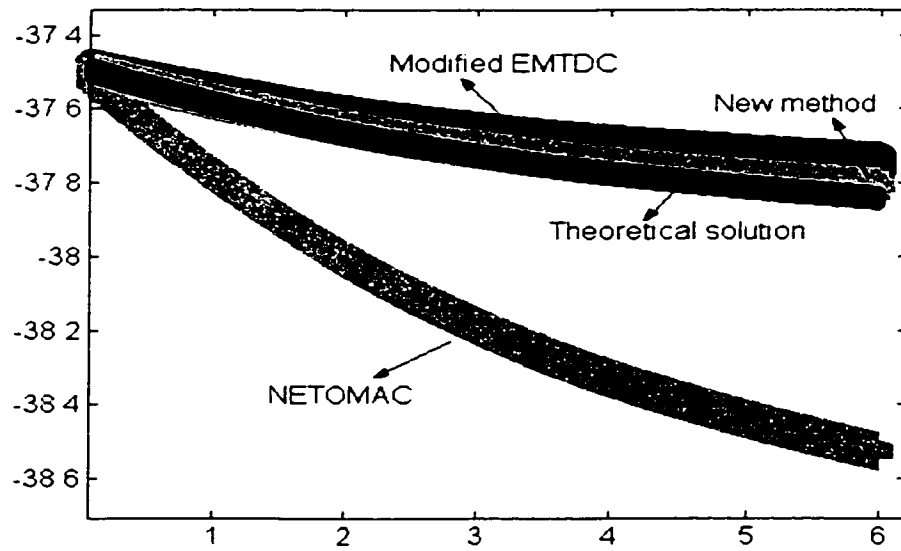Table 4.5   Comparisons of output voltage (discontinuous mode)
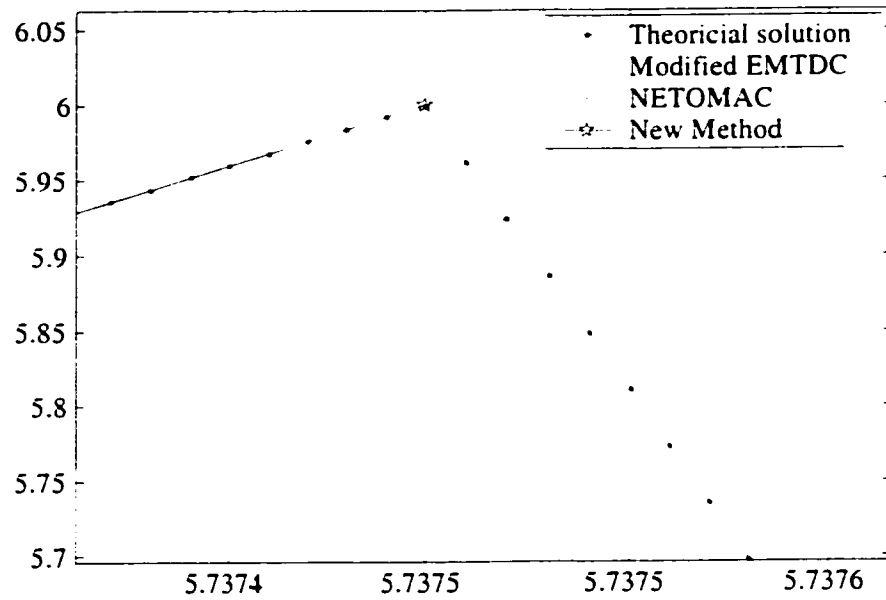
Fig 4.12 The enlargement waveform of inductance current(x axis: ms; y axis: inductor current, in A)

	Theoretical solution	Modified EMTDC	NETOMAC	New Method
i_{max} (A)	6	6.04	5.96	6.00005
Error (%)	0	0.667	0.667	0.0008

Table 4.6 Comparisons of inductance current (discontinuous mode)
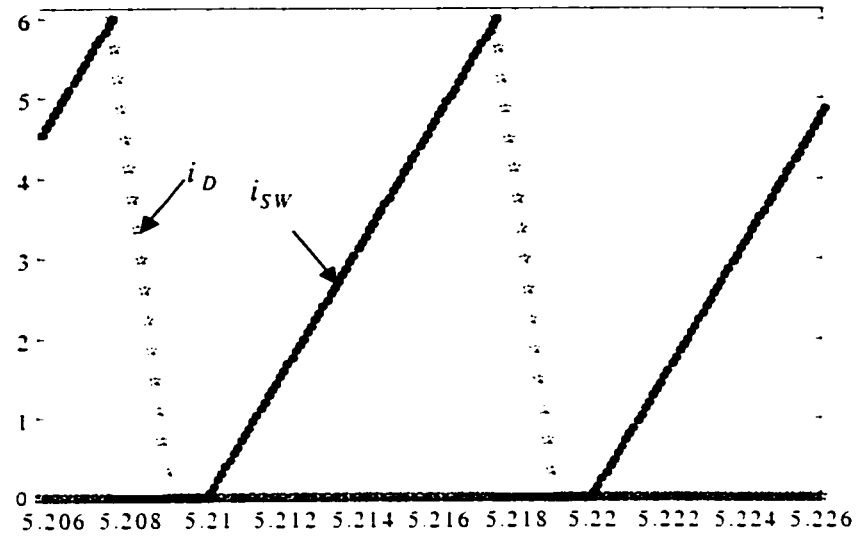
Fig 4.13   Superposed switch (i_{sw}) and diode (i_D) currents, New Method(x axis: ms;

y axis: inductor current, in A)

The demonstration of simultaneous switching between the diode and the switch is given

in Fig 4.13.

4.4   DIODE BRIDGE RECTIFIER
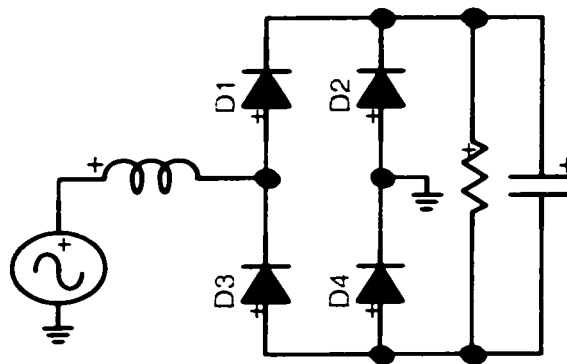
Fig 4.14   A signal phase diode rectifier

A diode bridge rectifier (Fig 4.14) is used here to test a purely natural commutation case. Diodes are modeled again as ideal switches with a 0.7V turn-on criterion. It is shown in Fig 4.15 that again EMTDC is less precise and noisy at the discontinuity time-point. NETOMAC cannot provide a continuous transition because both closely linked inductance voltage and capacitance current must be reinitialized at the same time-point. The New Method offers the best performance. In the case of EMTP, its apparent precision is related to an averaging effect in the computation of the capacitor voltage and its other quantities remain noisy at the discontinuity treatment time-point.
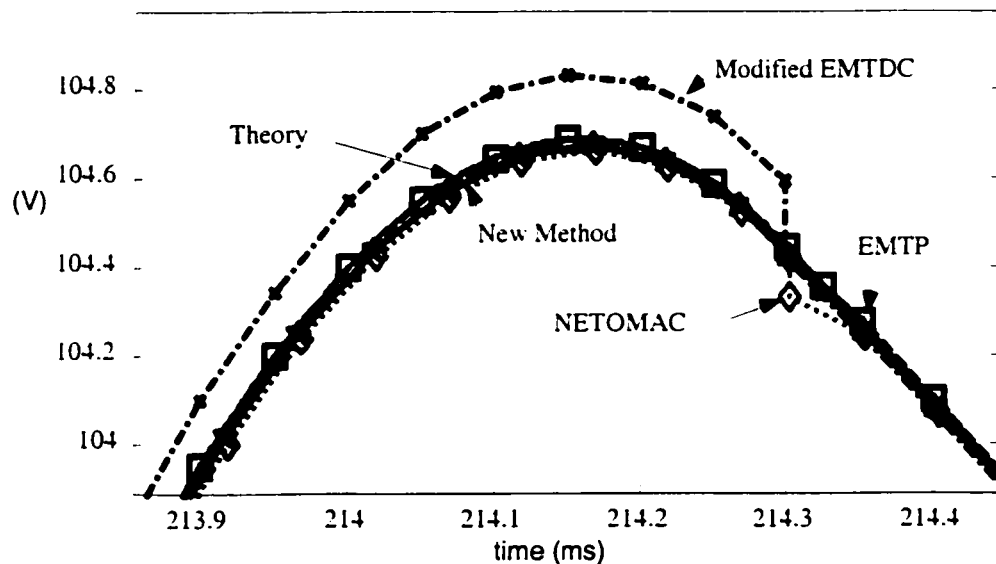
Fig 4.15 **Capacitor voltage for the diode bridge rectifier (x axis: ms; y axis: output voltage, in V)**

4.5 SIMULATING OF PWM CONVERTERS

4.5.1 Principle of operation and simulation results for bipolar switching case
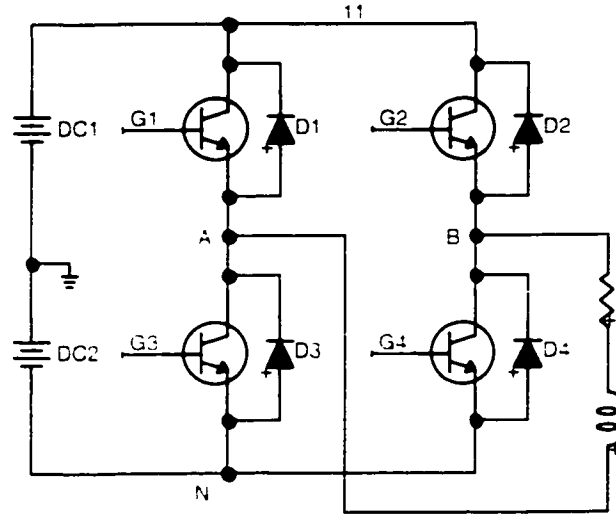
Fig 4.16   Single-phase full bridge SPWM inverter

A single-phase full bridge PWM inverter is shown in Fig 4.16. The basic principles of the PWM with bipolar voltage switching are shown in [28].

The amplitude modulation ratio is defined as

$$m_a = \frac{V_{sin}}{V_{tri}} = 1.0 \tag{4.15}$$

Where V_{sin} is the peak amplitude of the sinusoidal waveform and V_{tri} is the peak amplitude of the triangular signal.

The frequency modulation ratio is defined as

$$m_f = \frac{f_s}{f_1} = 15 \qquad (4.16)$$

Where f_s is the frequency of the triangular waveform and f_1 is the desired fundamental frequency of the output ac waveform. Because of the heavy inductive load, the output current is lagging the output voltage.
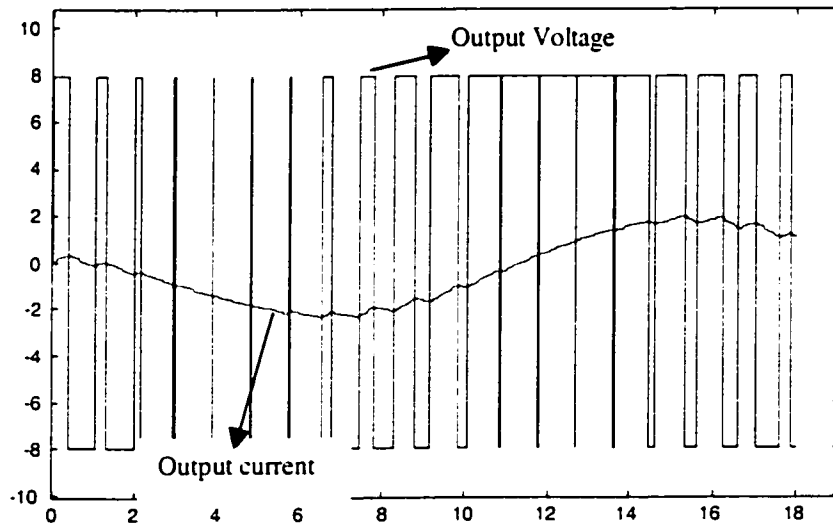
Fig 4.17   Output ac voltage and current (x axis: ms; y axis: output voltage and current, in V and A)

Fig 4.17 shows the waveform of output voltage. The shown load current is for a large inductive load ($L = 10\text{mH}, R = 2\Omega$). If the load is resistive, the waveform of the load current will be almost the same as the waveform of output voltage.

4.5.2 The current transition in bipolar switching

The switches are modeled as ideal, which allows the two switches in the same inverter leg to change simultaneously from on to off and vice versa.

In practice, most of the loads are inductive. So when the two IGBTs switch off, the current of inductance cannot change immediately. Therefore, the current should flow through diode D2 and D3.

In bipolar switching, there are three kinds of processes of basic current transition.

The first kind (CASE1) occurs when the load is purely resistive. The current can change its direction instantly, for example from G1, G4 to G2, G3.

The second kind, illustrated in Fig 4.18 (CASE2) is more complicated. For example, G1 and G4 conduct first. The output current in the inductive load is built up in state I. When the gating signal changes (from G1 and G4 to G2 and G3), the G1 and G4 are turned off; G2 and G3 are turned on. However the current in inductance cannot change direction instantly, it should find a way to flow. Current will flow in its original direction by conducting D2 and D3 alternatively in state II. After current reaching zero, the circuit goes to state III. G2 and G3 conduct and the circuit goes into the next switching cycle.

STATE I
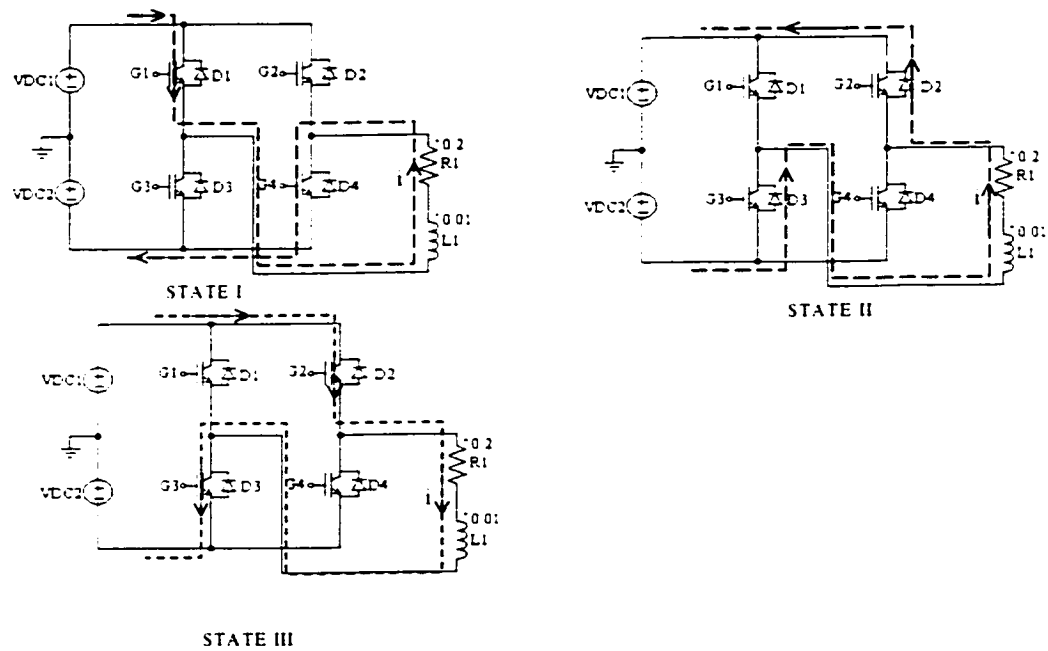
STATE II

STATE III

Fig 4.18   Current transition (CASE2)

The simulation results are shown below.
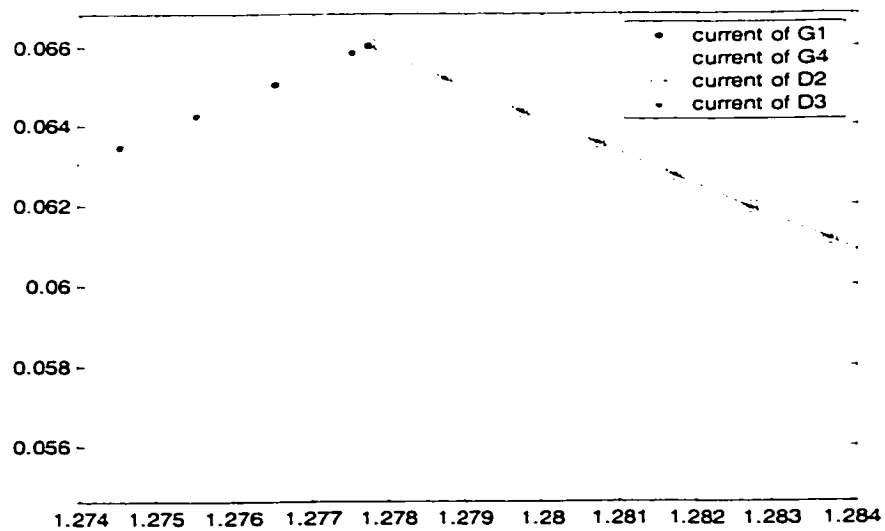
Fig 4.19   Current transition from switches to diodes (state I to state II, x axis: ms; y axis: output current, in A)
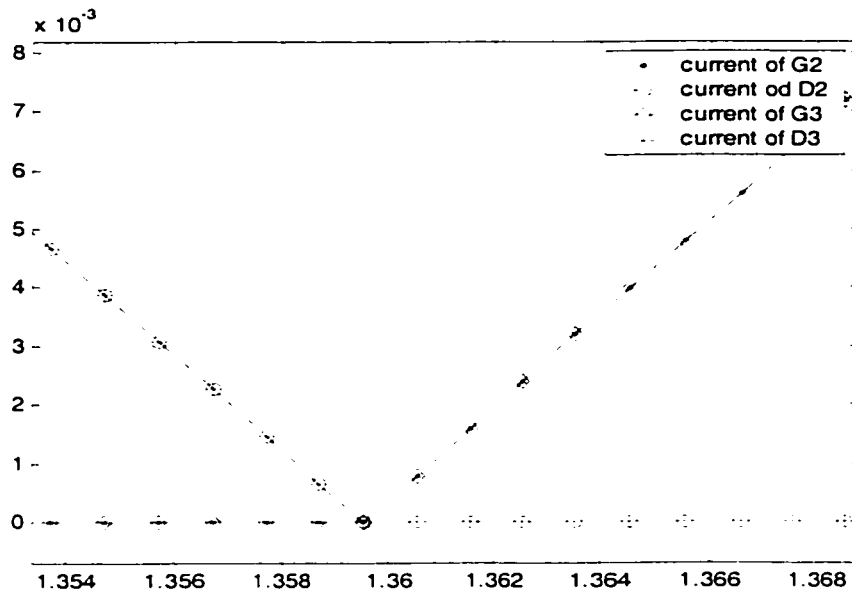
Fig 4.20 Current transition from diodes to switches (state II to state III, x axis: ms; y axis: output current, in A)

The third kind of transition is shown in Fig 4.21 (CASE3). First, G1 and G4 are forced to conduct, the output current in the inductive load is built up in state I. When the gating signal has been changed (from G1 and G4 to G2 and G3), the G1 and G4 are turned off while G2 and G3 are turned on. However the current in inductance cannot change direction simultaneously, the diode D2 and D3 are turned on as the inductor current commutates to them in state II. The difference here is that due to the time constant of the circuit, the current in D2 and D3 may not become zero when G2 and G3 are gated to turn on. G1 and G4 are fired again and the circuit goes into state III that is the same as state I.

Fig 4.22 shows the current transitions of case3. At point A in Fig 4.22, there are current transitions between diodes and switches shown in Fig 4.23.

STATE I

STATE II

STATE III
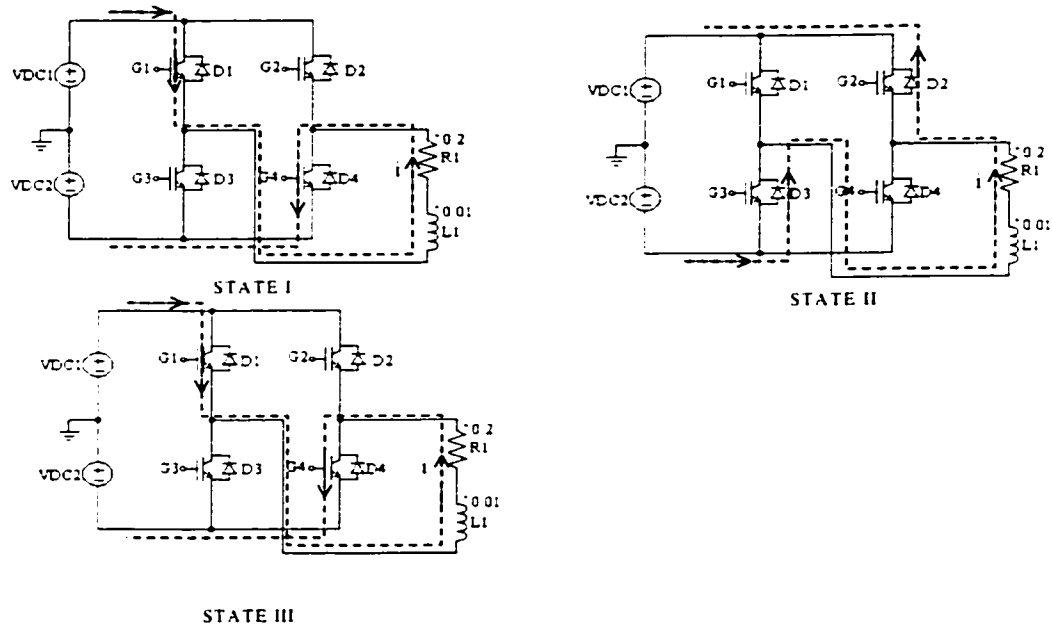
Fig 4.21   Current transition (CASE3)
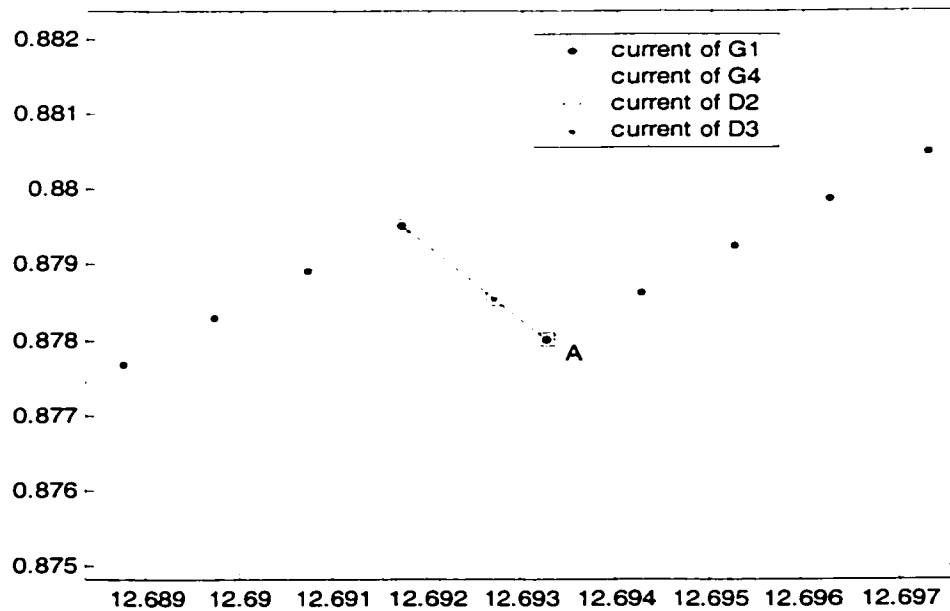
Fig 4.22   Current transition from switches to diodes to switches (CASE3, x axis: ms; y axis: output current, in A)
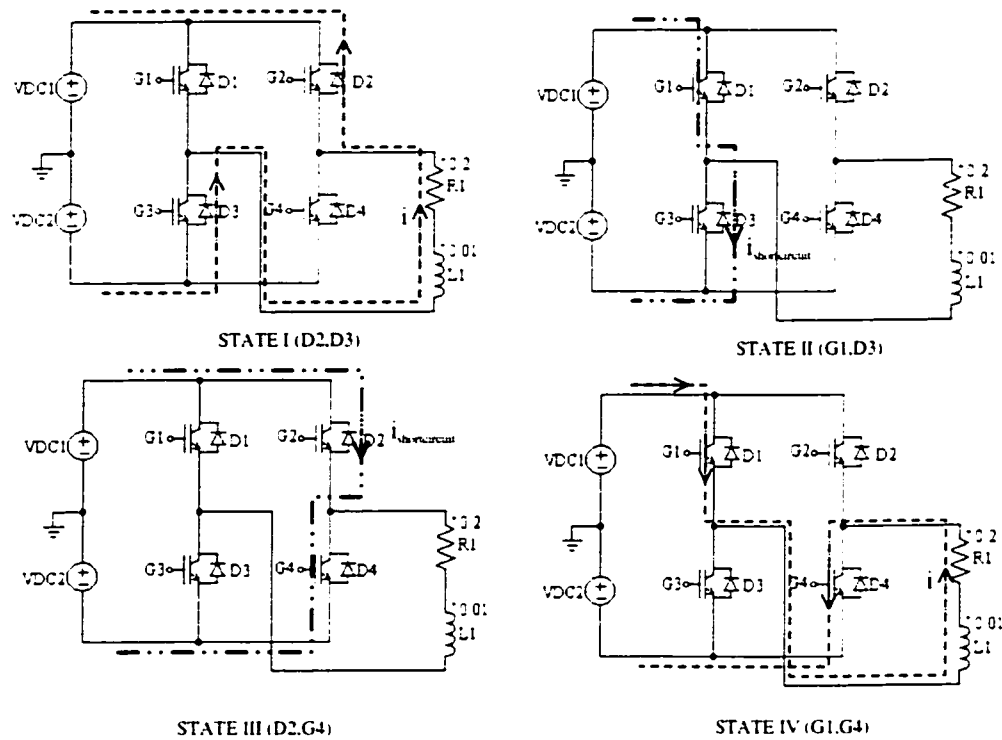
Fig 4.23   Process of current transition (point A)

At the beginning, the current flows through D2 and D3. The current decreases slowly. After some time G2 and G3 are turned off and G1 and G4 are ok to turn on. In state II, there is a short circuit through G1 and D3 in the first leg because of G1's turning on. The program finds the current in D3 is reversed and turns it off. The circuit now goes into the state III. The current finds another way by flowing through D2 and G4 because D2 is still on. The main program then turns off D2. Finally, the circuit goes into state IV and G1, G4 are turned on and the circuit goes into the next switching cycle.

Around point A in Fig 4.22, the new method performs calculations four times.

4.5.3   Principle of operation and simulation results for unipolar switching case

The operation principles of PWM with unipolar voltage switching can be found in [28] and the values of m_a and m_f are the same as bipolar voltage switching case.

The waveforms of Fig 4.24 show that there are four combinations of switch on-states and the corresponding voltage levels, which mentioned in [28] are as follows:

$$G_1, G_4 \text{ on} : v_0 = v_{C1} + v_{C2}$$
$$G_3, G_2 \text{ on} : v_0 = -(v_{C1} + v_{C2})$$
$$G_1, G_2 \text{ on} : v_0 = 0$$
$$G_3, G_4 \text{ on} : v_0 = 0$$

$$(4.17)$$

In equation (4.17), v_{C1}, v_{C2} are the voltages of the voltage sources DC1, DC2 in Fig 4.16. When both the upper switches are on, the output voltage is zero. The output current circulates in a loop through G_1 and D_2 or G_2 and D_1 depending on the direction of current. During this interval, the input current is zero. A similar condition occurs when both bottom switches G_3 and G_4 are on.
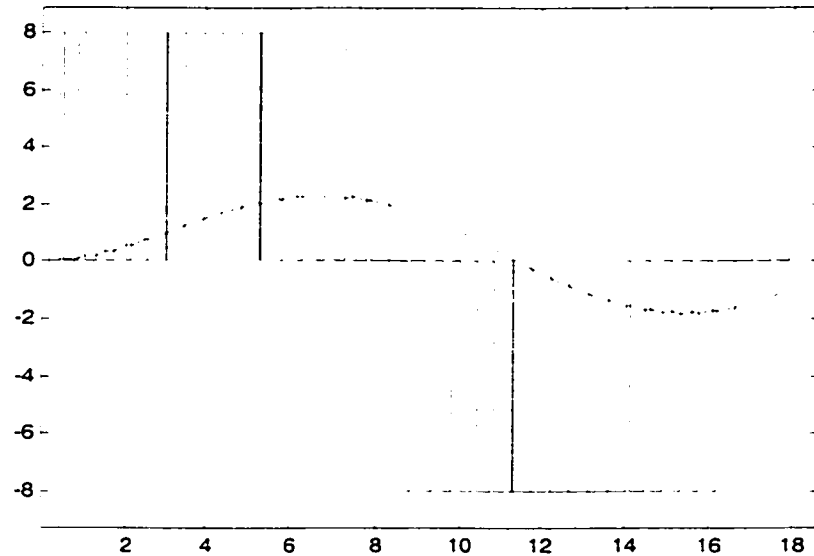
Fig 4.24   Output ac voltage and current (x axis: ms; y axis: output voltage and

current, in V and A)

4.5.4   The current transition in unipolar switching

In unipolar switching, there are two kinds of current transition in the positive cycle of output current. The current transition in negative cycle is as in the positive cycle.

The first kind (CASE1) of current transition is shown in Fig 4.25.

STATE I (G1.G4)

STATE II (G1.D2)

STATE III (G1.G4)

STATE IV (D3.G4)
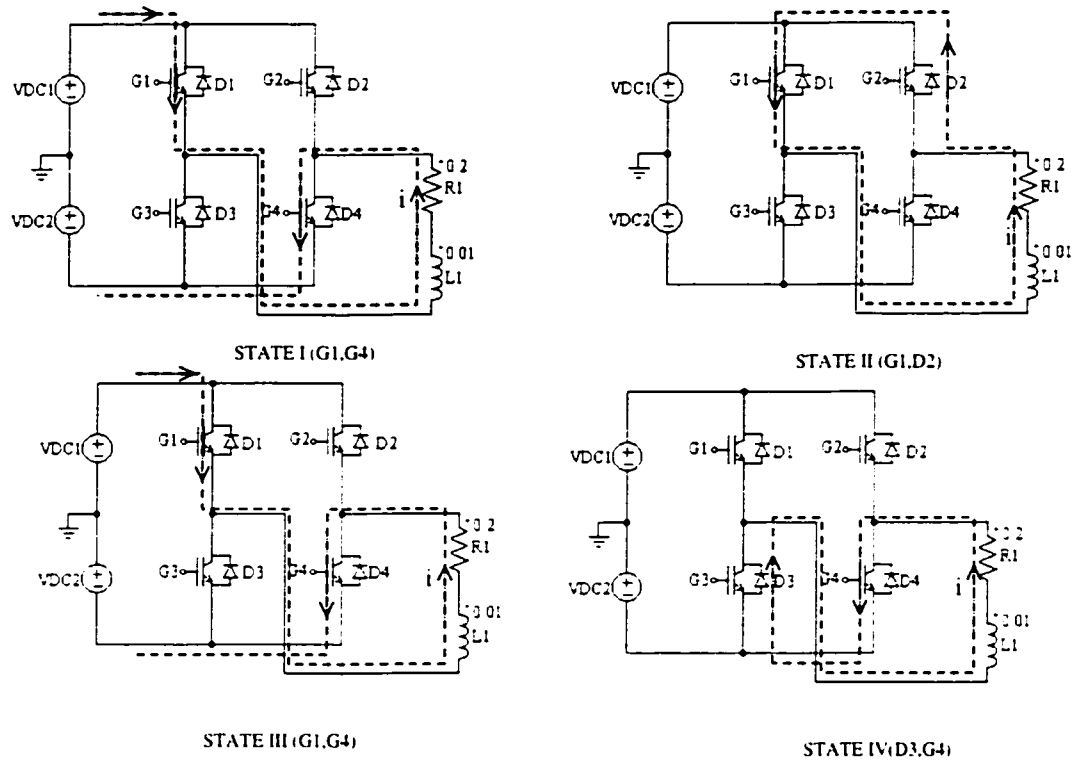
Fig 4.25   Current transition (CASE1)

For example, at the beginning G1 and G4 are turned on. After certain time, G2 is fired to turn on and at the same time G4 is turned off. The circuit goes into state II and current flows in the loop of G1 and D2. When G4 is fired again, the circuit goes into the state III. During the period of G3 and G4 turning on, the circuit goes into state IV, in which D3 and G4 are turned on. After that, the circuit goes into the next switching cycle. The simulation results are shown below.
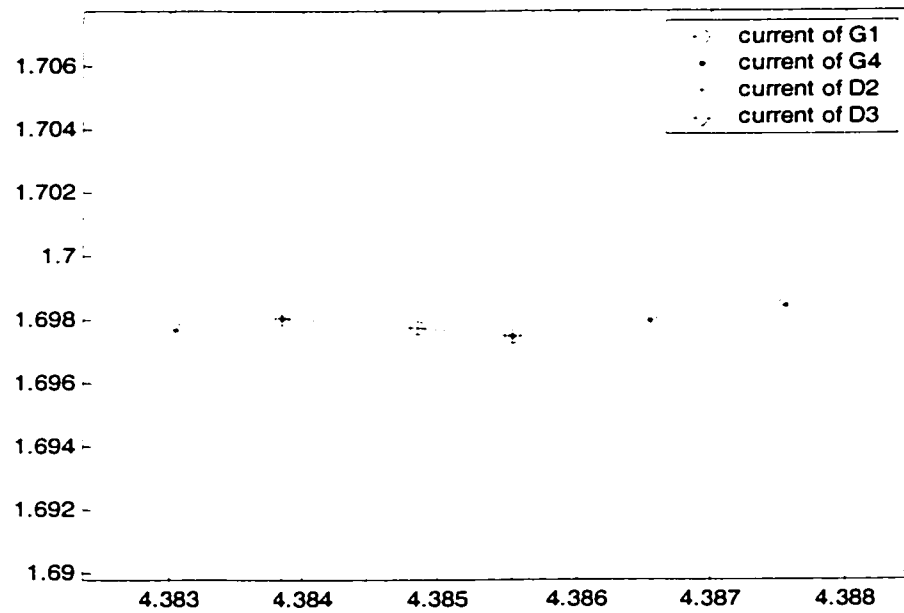
Fig 4.26 Current transitions (state I to state II to state III, x axis: ms; y axis: output current, in A)
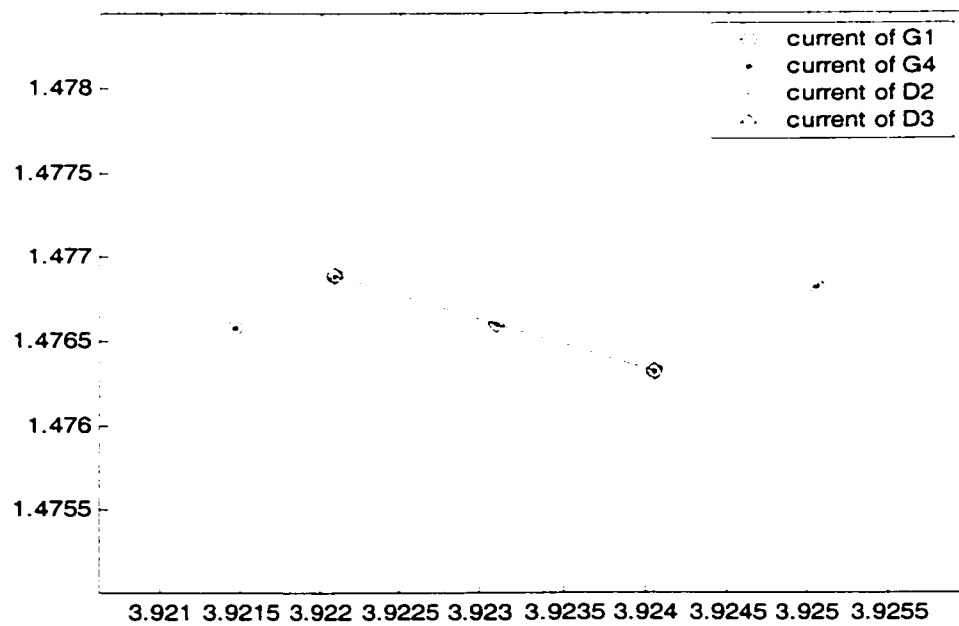
Fig 4.27 Current transitions (state IV to state I, x axis: ms; y axis: output current, in A)

The second kind (CASE2) of current transition is shown in Fig 4.28.

STATE I(D3.G4)

STATE II(D3.D2)

STATE III(G1.D2)

STATE IV(D3.D2)
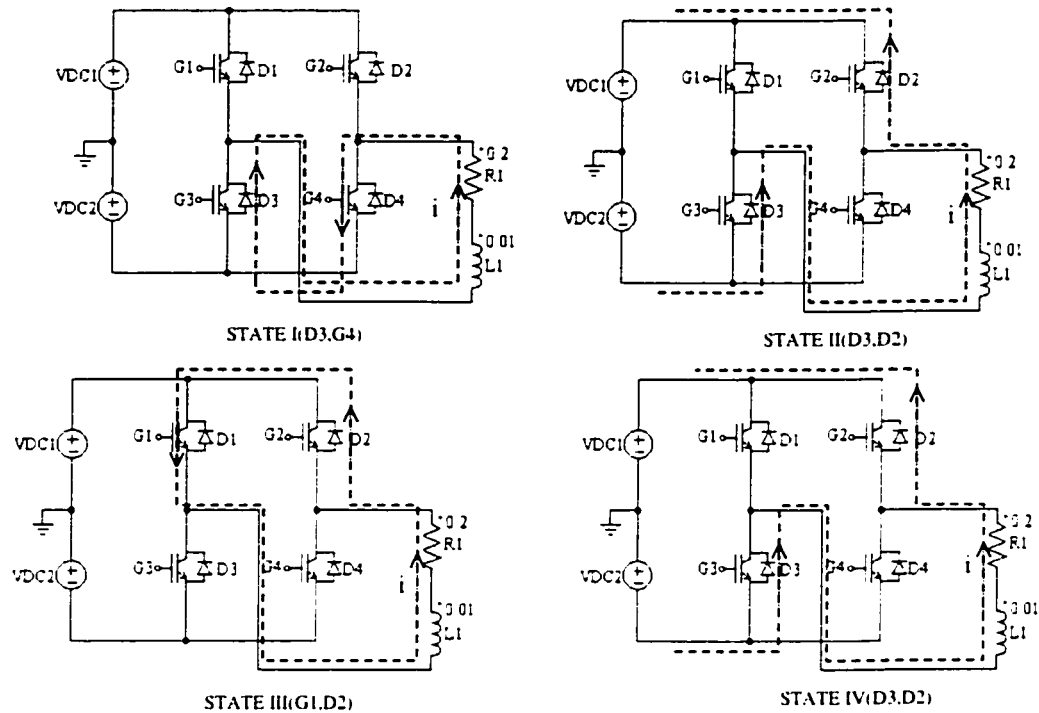
Fig 4.28   Current transition (CASE2)

When the output voltage goes to negative (the current is still positive due to the inductive load), the current transitions are a little bit different from the first manner. For example when voltage is zero in Fig 4.29, G4 and D3 are turned on as in state I in Fig 4.28. After certain time, G2 and G3 are fired to turn on because voltage becomes negative. However the current is still positive, D2 and D3 are forced to turn on. The circuit goes into state II and current flows through D2 and D3. After a while, G1 and G2 are fired again, output voltage become zero. The current flows through the loop G1 and D2 and the circuit goes into the state III. When G2 and G3 are fired again, the circuit goes into state IV, D2 and

D3 are turned on. After current becomes negative this circuit goes into the next switching

cycle. The simulation results are shown below.

Fig 4.29   Voltage crossing zero point (x axis: ms; y axis: output voltage, in V)
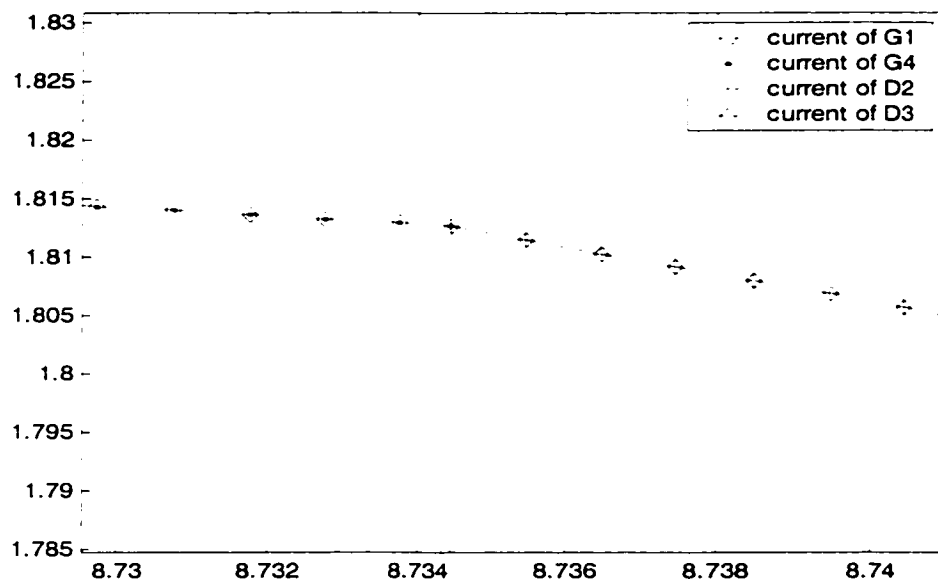
**Fig 4.30   Current transition (state I to state II, x axis: ms; y axis: output current, in A)**
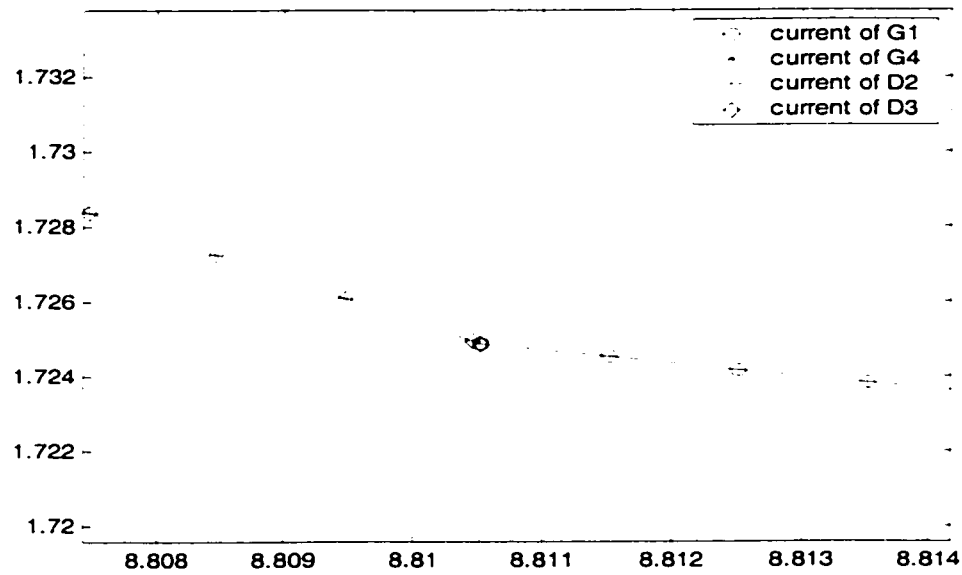
Fig 4.31   Current transition (state II to state III, x axis: ms; y axis: output current, in A)
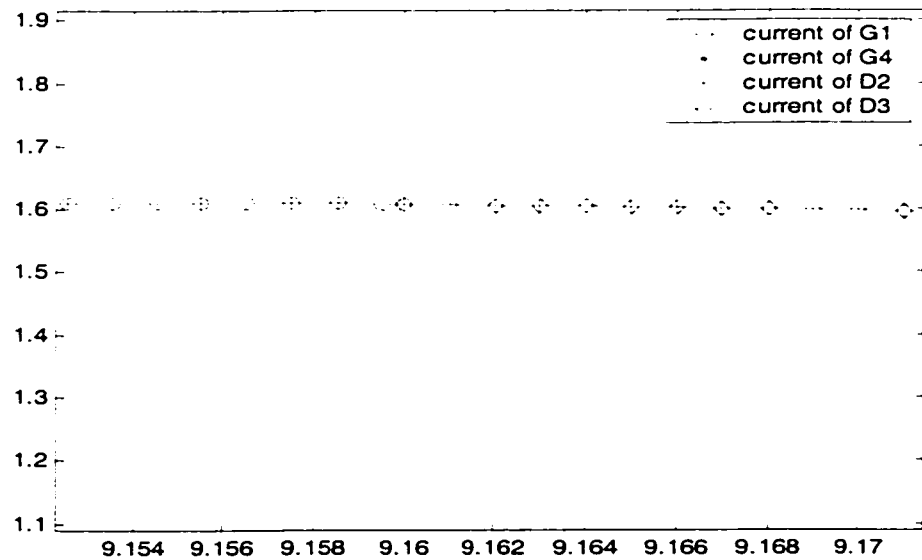
Fig 4.32   Current transition (state III to state IV, x axis: ms; y axis: output current, in A)
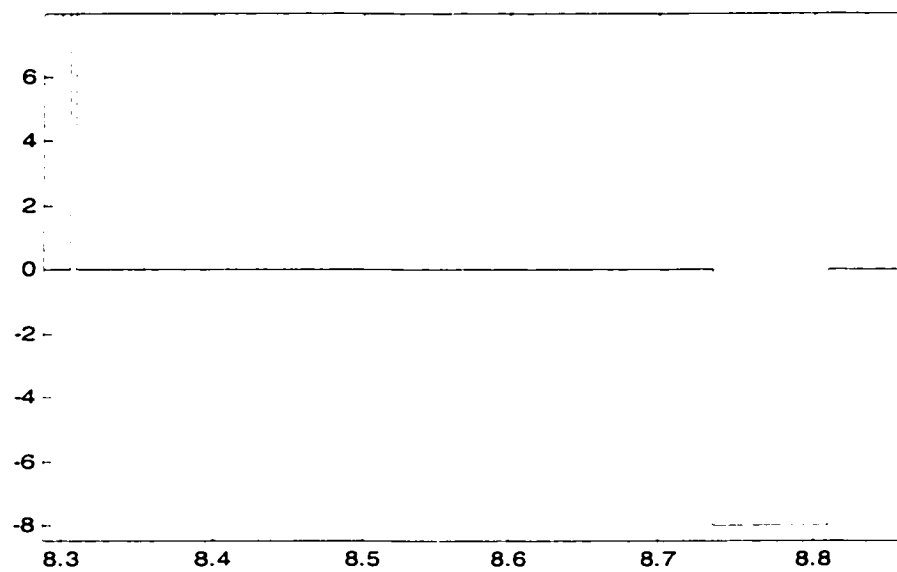
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4.5.5 Speed comparisons with PSPICE

	PSPICE	New Method
Bi-polar PWM controller (*30*ms)	3.94s	0.086s
Uni-polar PWM controller (*50*ms)	9.4s	0.16s

(In same computer, same simulation time)

Table 4.7   Computer timing comparison

Table 4.7 shows computer timing comparison with PSPICE. It appears that new method due to its fixed time-step usage and interpolation is much faster than PSPICE. PSPICE can achieve high quality simulation results due to its variable time-step algorithm.

4.6   CONCLUSIONS

This chapter has presented simulation results for a number of circuits containing switching elements, typically power electronic converters. Results obtained using the proposed new method were compared with those obtained with other methods. These comparisons show that the proposed method yields more stable and accurate results and does not introduce non-existent solutions and nor produce incorrect waveforms. It is also verified that the current transition between switches in power electronic converters takes place properly. Finally, based on a comparison of execution times, it can be concluded that the proposed method, despite the additional computations required, still requires less computational effort than variable time step simulation methods, indicating that the fixed time step routines, with a proper treatment of discontinuities, have a definite computational advantage.

CHAPTER 5

CONCLUSIONS

5.1 SUMMARY

This thesis deals with the handling of discontinuities in fixed time-step simulation programs designed for power system transient analysis. The more common methods are summarized and compared. A new method is proposed, which is based on re-initialization through interpolation and extrapolation. It assumes linear variations for quantities within the main trapezoidal integration time-step during continuous conditions. The proposed method has been extensively tested and shown to provide superior results for the demonstrated cases to other available techniques.

5.2 CONTRIBUTIONS

The major contributions of this thesis are:

(1) A systematic presentation of existing techniques developed for dealing with discontinuities.

(2) The development, implementation and validation of a new method to deal with discontinuities.

(3) A detailed and critical assessment of and comparison between the existing methods and the proposed method.

It should be mentioned that any method developed to deal with discontinuities must not target a particular topology, but behave equally well in arbitrary switching situations. To the best of our knowledge and taking into account the extensive testing carried out, we consider that the proposed method meets this requirement.

5.3   SUGGESTIONS FOR FUTURE WORK

Future developments can include application of the proposed algorithm to other power system elements operating in a discontinuous environment, including non-linear components, transmission lines, electrical machines, and control circuits.

REFERENCES

[1]   DCG-EMTP Version 3.0.

[2]   B. Kulicke, "Simulations programm NETOMAC: Differenzleitwertverfahren bei kontinuierlichen und diskontinuierlichen systemen," *Siemens Forshungs - und Entwicklungsberichte*, vol. 10, no. 5, pp. 299-302, 1981.

[3]   L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," University of California at Berkeley, ERL/M520, 1975.

[4]   H. W. Dommel, "Digital computer solution of electromagnetic transient in single and multiphase networks," *IEEE Trans. Power Application System*, vol. PA(S-88), no. 4, pp. 388-399, Apr. 1969.

[5]   J. R. Marti and J. Lin, "Suppression of numerical oscillations in the EMTP power systems," *IEEE Trans. Power System*, vol. 4, Issue: 2, pp. 739 –747, May 1989.

[6]   J. Lin and J. R. Marti, "Implementation of the CDA procedure in the EMTP," *IEEE Trans. Power System*, vol. 5, Issue: 2, pp. 394 –402, May 1990.

[7]   P. Kuffel, K. Kent, and G. Irwin, "The implementation and effectiveness of linear interpolation within digital simulation," in *Proc. 1995 Int. Conf. Power Systems Transients*, pp. 499-504.

[8]   B. De. Kelper, L. A. Dessaint, V. Q. Do, and J. C. Soumagne, "An algorithm for accurate switching representation in fixed-step simulation of power electronics," in *Proc. 2000 IEEE Power Engineering Society Winter Meeting*, pp. 762 -767.

[9]   V. Q. Do, D. McCallum, P. Giroux, and B. D. Kelper, "A backward-forward interpolation technique for a precise modeling of power electronic in HYPERSIM," in *Proc. 2001 Int. Conf. Power Systems Transients*, pp.337-342.

[10]   K. Strunz, L. Linares, J. R. Marti, O. Huet, and X. Lombard, "Efficient and accurate representation of asynchronous network structure changing phenomena in digital real time simulators," *IEEE Trans. Power System*, vol. 15, pp. 586 –592, May 2000.

[11]   A. R. Sana, J. Mahseredjian, X. D. Do, and H. Dommel, "Treatment of discontinuities in time-domain simulation of switched networks," *Mathematics and Computers in Simulation* 38(1995), pp. 377-387.

[12]   C. T. Liu, "An efficient EMTP compatible algorithm for modeling switch-controlled drive circuits," *IEEE Trans. Power Delivery*, vol. 9, pp. 2018–2025, Oct. 1994.

[13]   G. Irwin, D. Woodford, and A. Gole, "Precision simulation of PWM controllers," in *Proc. 2001 Int. Conf. Power Systems Transients*, pp. 161.

[14]   K. Strunz, X. Lombard, O. Huet, J. R. Marti, L. Linares, and H. W. Dommel, "Real time nodal-analysis based solution techniques for simulations of electromagnetic transients in power electronic systems," in *13th Power System Computation Conf.*, pp1047-1053, June 1999.

[15]   A. M. Gole, I. T. Fernando, G. D. Irwin, O. B. Nayak, "Modeling of power electronic apparatus: Additional interpolation issues, " in *Proc. 1997 Int. Conf. Power Systems Transients*, pp. 23-28.

[16] X. S. Cai and Y. Xing, "A new algorithm for the discrete time-domain simulation of switching regulators," *IEEE Workshop, Computers in Power Electronics*, pp. 29 –35, 1990.

[17] F. Q. Fang, J. Dai, "Eliminating the numerical oscillations in the transient simulations of power systems using novel mathematical models," in *Proc. 1992 IEEE Region 10 Int. Conf.*, vol. 1, pp. 377-380.

[18] E. V. Solodovnik, G. J. Cokkinides, and A. P. Meliopoulos, "On stability of implicit numerical methods in nonlinear dynamical systems simulation," in *System Theory, Proc. 1998 the Thirtieth Southeastern Symposium*, pp. 27 –31.

[19] X. Cao, A. Kurita, T. Yamanaka, Y. Tada, and H. Mitsuma, "Suppression of numerical oscillation caused by the EMTP-TACS interface using filter interposition," *IEEE Trans. Power Delivery*, vol. 11, pp.2049 –2055, Oct. 1996.

[20] N. R. Watson and G. D. Irwin, "Comparisons of root-matching techniques for electromagnetic transient simulation," *IEEE Trans. Power Delivery*, vol. 15, pp. 629 –634, Apr. 2000.

[21] J. Lin, "Elimination of indemonstrable phenomena in the EMTP," in *Proc. 1998 Power System Technology Int. Conf.*, vol. 2, pp. 895-899.

[22] C. T. Liu and W. L. Chang, "Synchronized solution of power electronics system equations using flexible MODELS component connected to the EMTP," *IEEE Trans. Power Delivery*, vol. 11, pp. 1868–1873, Oct. 1996.

[23] J. Mahseredjian and F. Alvarado, "MatTran manual," 1999.

[24] J. Mahseredjian and G. Joos, "Solution methods for varying topology networks," in *Proc. 2002 IEEE Power Engineering Society Winter Meeting*, vol. 1, pp. 479–483.

[25] J. Mahseredjian and F. Alvarado, "Creating an electromagnetic transients program in MATLAB: MatEMTP," *IEEE Trans. Power Delivery*, vol. 12, pp. 380–388, Jan. 1997.

[26] EMTPRV version 1.0.

[27] M. Zou, J. Mahseredjian, and G. Joos, B. Delourme "On interpolation and re-initialization in the simulation of transients in power electronic systems," presented at the 14th Power Systems Computation Conf., Sevilla, section. 32, pp.1-7, June 2002.

[28] N. Mohan, T. Undeland and W. P. Robbins, "Power Electronics: Converters, applications and design," 2nd ed., John Wiley&Sons Inc., 1995, pp 211-218.