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Diagnosis and Yield Analysis of a Complex Interconnection Architecture

Bing Qiu

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfilment of the Requirements
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ABSTRACT

Diagnosis and Yield Analysis of a Complex Interconnection Architecture

Bing Qiu

This thesis investigates problems associated with the integration of very large fault-tolerant networks. The focus of the research is on the diagnosis and yield analysis of a complex interconnection architecture. In this thesis, a closed form yield model that takes into account constraints of an architecture has been proposed. It applies to architectures that approximate global redundancy and for which the constraints translate into yield losses. The impact of the constraints on yield can be evaluated by calculating the probability of observing non-tolerable defect patterns and by subtracting these probabilities from yield of arrays with global redundancy. It has been shown that most of the yield losses come from a few patterns comprising small number of defects. According to the characteristics of the analyzed architecture and the nature of defect distributions, different yield models have been derived. With these models, the sensitivity of the yield of the analyzed architecture to variations of the defect density has been investigated. This thesis also proposes regression yield models that can be used to quickly predict the redundancy needed for given array and cell sizes as part of a design flow.

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Table of Contents

List of Figures viii

List of Tables xi

List of Acronyms xii

List of Primary Symbols xiii

1. Introduction 1

1.1 Introduction 1

1.2 Motivation and objective 4

1.3 Scope and organization of the thesis 5

2. Analysis of a Complex Interconnection Architecture 7

2.1 Introduction to fault tolerance mechanism 7

2.2 Complex interconnection architecture 9

2.2.1 Overview of the fault-tolerant architecture 11

2.2.2 Configuration of the transmitter multiplexers of a cell 13

2.2.3 Configuration of the receiver multiplexers of a cell 14

2.3 Reconfiguration strategies of the fault-tolerant structure 15

2.3.1 Basic reconfiguration strategies 16

2.3.2 Reconfiguration of cells in the fault-tolerant structure 19

2.3.3 Reconfiguration of bundles in the fault-tolerant structure 23

2.4 Summary 25

3. Yield Modeling of a Complex Interconnection Architecture 27

3.1 Introduction to yield analysis and yield models 27

3.1.1 Defects and faults 27

3.1.2 Review of basic yield models 28

3.1.3 Yield modeling for circuits with redundant structures 31

3.2 Yield modeling for a complex interconnection architecture 33
3.2.1 Constraints-based yield model 33
3.2.2 Non-tolerable patterns in an array of designated size 41
3.2.2.1 Non-tolerable patterns in the array with fault-free bundles 41
3.2.2.2 Non-tolerable patterns with defective bundles and cells 44
3.3 Defect density impact on forming a logical array 56
3.4 Yield model regression 57
3.5 Summary 60

4. Analysis of the effects of clustered defects on yield 62
4.1 Introduction to yield formulas when defects are clustered 62
4.2 Yield modeling for the architecture assuming clustered defects 65
4.2.1 Yield modeling with identical sub-circuits assumed statistically dependent ...65
4.2.2 Yield modeling with all sub-circuits assumed statistically dependent 70
4.3 Numerical result of the yield with clustered defects 78
4.3.1 Effects of clustered defects on yield losses 78
4.3.2 Effects of clustered defects on the yield of forming logical arrays 85
4.4 Yield model regression with clustered defects 89
4.5 Summary 93

5. Conclusion 95
5.1 Summary of the work 95
5.2 Suggestion for future research 98

References 99

Appendix A Terminology and replacement rules of the fault-tolerant structure ...105
Appendix B Thirteen kinds of non-tolerable patterns 110
Appendix C Analytical proof related to the second most significant non-tolerable pattern 120
Appendix D Derivation of the regression yield model 125

Appendix E Derivation of Y_{cell} with Maxwell-Boltzman combinatorial statistics ..127

Appendix F Derivation of the formulas with *Maxwell-Boltzman* statistics and *Bose-Einstein* statistics 129

List of Figures

Figure 1.1 A proposed architecture organized as a processing array of size 20 x20 4

Figure 2.1 Processing array of size *K* x *L* based on the architecture in [27]-[29] 10

Figure 2.2 Interconnection structure of a physical array of size 3x3 based on the architecture in [27]-[29] 12

Figure 2.3 Configuration of the transmitter multiplexers of cells 13

Figure 2.4 Configuration of receiver multiplexers of cells in a 3x3 physical array 15

Figure 2.5 Example of using the cell-stealing strategy to construct a logical array of 2x3 out of a physical array of 3x3 17

Figure 2.6 Example of using the cell-shifting strategy to construct a logical array of 2x2 out of a physical array of 3x2 18

Figure 2.7 Example of using the column or row exclusion strategy to construct a logical array of 2x2 from a physical array of 3x2 19

Figure 2.8 Using the cell-stealing strategy to construct a 3x2 logical array from 3x3 physical array based on the architecture in [27]-[29] 20

Figure 2.9 Using the perfect replacement with cell-shifting strategy to build a 2x2 logical array from a 3x3 physical array 21

Figure 2.10 Using the imperfect replacement with cell-shifting strategy to construct a 2x2 logical array from a 3x3 physical array 22

Figure 2.11 Intra-bus replacement in the fault-tolerant structure 24

Figure 2.12 Inter-bus replacement in the fault-tolerant structure 25

Figure 3.1 Simplified diagram of a 8 by 8 physical array based on the architecture in [27]-[29] 36

Figure 3.2 Pattern preventing the construction of a logical array size of 3 by 3 out of a physical array of 4x3 38

Figure 3.3 Flow chart of the probability of forming a logical array 38

Figure 3.4 Non-tolerable pattern is composed of the least number of defective cells in an array without defective bundles 42
Figure 3.5 Six defective cells in a corner prevent the construction of a logical array of NxN 42
Figure 3.6 Non-tolerable Pattern 1 in a physical array of $(N+1) \times N$ 45
Figure 3.7 Not allowed replacement for two defective vertical bundles 47
Figure 3.8 Non-tolerable Pattern 2 in a physical array of $(N+1) \times N$....48
Figure 3.9 The first possibility of forming a logical array of NxN from a physical array of $(N+1)$xN with the existence of non-tolerable Pattern 2....49
Figure 3.10 The second possibility of forming a logical array of NxN from a physical array of $(N+1)$xN with the existence of non-tolerable Pattern 2....50
Figure 3.11 Yield loss contributed by the most significant non-tolerated pattern 53
Figure 3.12 Yield loss contributed by the second most significant non-tolerable pattern..53
Figure 3.13 Yield of the structure with global redundancy 54
Figure 3.14 Comparison between Y_{loss} and Y_{global} 54
Figure 3.15 Yield loss by the first most significant non-tolerable pattern when a bundle comprises 40 wires 56
Figure 3.16 Yield loss by the second most significant non-tolerable pattern when a bundle comprises 40 wires 56
Figure 3.17 Yield of forming a logical array of 20x20 from physical arrays of 21x20, 21x21, and 22x22 57
Figure 3.18 Cross points for arrays of different sizes with equivalent redundancy ratio ..58
Figure 3.19 Comparison of the regression model and the complete yield model 60
Figure 4.1 Effect of clustered defects on a conventional chip yield(from [17])....63
Figure 4.2 Effects of clustered defects on the yield of forming a logical array of 20x20 from a physical array of 21x20 79
Figure 4.3 Effects of clustered defects on the yield loss contributed by the first most significant non-tolerable pattern in forming a logical array of 20 by 20 from a physical arrays of 21x20....80
Figure 4.4 Effects of clustered defects on the yield loss contributed by the second most significant non-tolerated pattern 81

Figure 4.5 Yield and yield losses due to two most significant non-tolerable patterns at higher clustered defect density in forming a logical array of size 20x20 out of a physical array of size 21x20 82
Figure 4.6 Yield loss contributed by the first most significant non-tolerant pattern in forming a logical array of 5x5 from a physical array of 6x5 84
Figure 4.7 Yield loss contributed by the second most significant non-tolerant pattern in forming a logical array of 5x5 from a physical array of 6x5 84
Figure 4.8 Yield of forming logical arrays size of 20x20 from physical array of 21x20, 21x21, and 22x22 86
Figure 4.9 Comparison of the yields computed with different equations in constructing a logical array of 4x4 from a physical array of 5x4 88
Figure 4.10 Comparison of the yields calculated with different equations in constructing a logical array of 4x4 from a physical array of 5x5 88
Figure 4.11 Yield of arrays with equivalent redundancy ratio, computed with (4.27), (4.35), and (4.36) using *Bose-Einstein* statistics 89
Figure 4.12 Comparison between the regression model and the yield model assuming *Bose-Einstein* distribution 91
Figure 4.13 Comparison of the yield predicted by regression model with the clustered defect distribution and the random defect distribution 92

List of Tables

Table 3.1 Yield of a bundle, a cell, and the reconfiguration logic within one cell. The data comes from a WSI demonstration chip....33

Table 3.2 Yield of a bundle, a cell and the reconfiguration logics within one cell. The data comes from the proposed WSI architecture....33

Table 3.3 Yield losses contributed by thirteen kinds of significant non-tolerable patterns in the construction of a logical array of Nxn from a physical array of (N+1)xN....43

Table 3.4 Numerical value of the pivot points of physical arrays of different sizes with redundancy ratio equal to 0.1....58

Table 4.1 Computation time of one numerical point of the yield loss curves in forming a logical array of size 20x20 from a physical array of size 21x20, where a bundle comprises 40 wires with an area $11mm^2$ and the area of a cell is $25mm^2$....83

Table 4.2 Numerical value of the approximate pivot points for arrays with redundancy ratio equal to 0.1. It is assumed that defects comply to *Bose-Einstein* distribution....90

Table 4.3 Computation time for one numerical point of different yield curves in forming a logical array of 20x20 from a physical array of 21x21, where a bundle comprises 40 wires with an area $11mm^2$ and the area of a cell is $25mm^2$....93

List of Acronyms

ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
EE	an Equivalent-area Element
IC	Integration Circuit
JTAG	Joint Test Action Group
LSI	Large-Scale Integration
MSI	Medium-Scale Integration
SoC	System on Chip
SSI	Small-Scale Integration
VLSI	Very Large Scale Integration
WSI	Wafer Scale Integration

List of Primary Symbols

A	the critical area of a circuit
α	a clustering parameter
D	the defect density of a chip
G_{xy_i}	the probability of all x defects being distributed over y_i EEs so that each of these y_i EEs has at least one defect
F_c	number of defective cells
F_{HB}	number of defective horizontal bundles
F_{VB}	number of defective vertical bundles
i_m	the number of the defective EEs in the cells
j_t	the number of the defective EEs in the vertical bundles
k_p	the number of the defective EEs in the horizontal bundles
λ	the expected number of defects per chip
m	the number of cells in a physical array of size K by L, i.e., $m=K$xL
n_c	the total number of EEs in a cell
n_{VB}	the total number of EEs in a vertical bundle
n_{HB}	the total number of EEs in a horizontal bundle
N_c	number of cells in a column or a row
N_{HB}	number of horizontal bundles in a column or a row
N_{VB}	number of vertical bundles in a column or a row
NTC_{cell}	number of non-tolerable patterns when F_C defective cells are distributed over a complete array
NTC_{HB}	number of non-tolerable patterns when F_{HB} defective horizontal bundles are distributed over a complete array

NTC_{VB}	number of non-tolerable patterns when F_{VB} defective vertical bundles are distributed over a complete array
Q_c	total number of cells
Q_{VB}	total number of vertical bundles
Q_{HB}	total number of horizontal bundles
P_{xF_c}	the probability of having all x defects distributed over F_c cells such that each cell has at least one defect
$P_{yF_{VB}}$	the probability of having all y defects distributed over F_{VB} vertical bundles such that each vertical bundle has at least one defect
$P_{zF_{HB}}$	the probability of having all z defects distributed over F_{HB} horizontal bundles such that each horizontal bundle has at least one defect
P_{tx}	the probability that x defects in the structure can be tolerated
r	the redundancy ratio of a physical array of size K by L
S_c	number of spare cells
S_{VB}	number of spare vertical bundles
S_{HB}	number of spare horizontal bundles
$y_i(i=1,2,...,7)$	the total number of defective EEs in the ith item
y_{cell}	the yield of a cell
y_{HB}	the yield of a horizontal bundle
y_{VB}	the yield of a vertical bundle
Y_{chip}	the true yield of the structure
Y_{global}	the yield of the structure assuming global redundancy
Y_{loss}	the operability of having non-tolerable defect patterns in the structure
$(Y_{NTP})_i$	the yield loss due to the ith non-tolerable pattern of the structure

Chapter 1
Introduction

1.1 Introduction

Since the implementation of the first integrated circuits (ICs) in the mid 1960s, the IC technologies have developed rapidly. Early small-scale integration (SSI) ICs contained several logic gates amounting to tens of transistors. Then, medium-scale integration (MSI) increased the range of integrated logic gates available to larger scale functions. In the era of large-scale integration (LSI), much complex logic functions, such as those of the first microprocessors, were packed into a single chip. The further improvement of CMOS process technologies led to the advent of very large scale integration (VLSI) in the 1980s. In this era, VLSI technologies could offer complete 64-bit microprocessors with cache memory circuits and floating-point arithmetic units on a single piece of silicon. More than a million transistors can be integrated in a chip with these technologies. Today, advanced VLSI technologies, particularly deep-submicron technologies, can integrate almost one billion transistors in a single chip. These state-of-the-art technologies make it possible to implement all aspects of a system design on a single chip, referred to System-on-Chip (SoC) circuits. SoC eliminates many off-chip driver circuits, the associated delay time and power consumption. Furthermore, the availability of rich on-chip wiring may allow a substantial increase in the data bandwidth between cores in the chip, thus improving the performance.

Implementing a system on a single chip implies that the integration density of a chip needs to increase greatly. Evidently there are two ways to achieve this target. One is to reduce the transistor size, and the other is to increase the area of a single chip. The former is the well-known feature size scaling technology, the dominant approach in the semiconductor industry. With the advent of deep submicron VLSI technologies, the feature size of a CMOS transistor has been scaled down to 0.10 μm from 1.0 μm of ten years ago. Different from the feature size scaling, enlarging the area of a single chip to increase the integration density of ICs is also very attractive to the semiconductor industry. A fascinating technology to enlarge the chip area is Wafer Scale Integration (WSI). This technology enables the fabrication of a single chip as large as the maximum wafer diameter in commercial manufacturing. Since Sack and his colleagues first attempted to implement an array comprising some simple logical circuits on a single wafer in 1964 [32], WSI technology has attracted the interest of the electronics industry and the academic community for decades. A large number of issues associated with WSI have been studied. The technological features to distinguish WSI from other integrated circuit arts are associated with the management of the special problems of large substrates, such as yield, interconnection, packaging and thermal dissipation. Among them, a very typical feature is using fault tolerance techniques to lower the impact of manufacturing defects and to increase the yield of WSI components [7].

Wafer scale integration emerges as a natural evolution from the device-oriented VLSI chip technologies to system-oriented wafer-level technologies. Due to the limitation of the VLSI technologies in the past years, the broad investigations of WSI issues have not led to mass commercial wafer-scale production. With the advent of deep submicron VLSI

technology, WSI is widely regarded as a technically feasible proposal for systems that possess enough regularity and reconfigurability in their architectures. WSI technology allows building a system with two orders of magnitude more active devices than VLSI circuits, and it eliminates all intermediate levels of packaging or bonding. Compared with systems implemented with VLSI circuit chips mounted on printed circuit boards, WSI systems provide much more potential benefits such as significant speed improvement and higher data communication bandwidth. Although WSI systems possess many attractive potential advantages, there exist a number of practical problems associated with WSI design and manufacturing. The problems can be classified as physical design problems and electrical design problems [43]. For instance, in the physical design problems, packaging is the most difficult problem facing WSI. A WSI package should provide the mechanical support and hermetic sealing with a cavity size large enough to accommodate an entire wafer. Moreover, a suitable packaging technology must take into account heat dissipation and thermal expansion. The latter problem represents serious challenges when packaging materials and the wafer material have differences in thermal expansion coefficients. Among the electrical design problems, power supply distribution, synchronization, signal integrity, extremely long interconnections, fault tolerance and the yield of a WSI system, all pose unique challenges to the implementation of WSI technology.

1.2 Motivation and objective

A system implemented with WSI can potentially provide multi-terabit switching and rich data communication bandwidth between cores in the system. These potential benefits

address special circuit needs for ever-increasing speed and bandwidth in telecommunication applications. For telecom routers, the demand for increased bandwidth to process large amount of data requires growing performances. Chip-based router architectures are already reaching their limits, and a superior technology is needed to alleviate this bottleneck. To meet this requirement, a highly parallel router architecture involving a large number of routing nodes was proposed by Richard S. Norman of Hyperchip Inc. [27]-[29], and the related circuit structures have been designed to enable WSI [1].

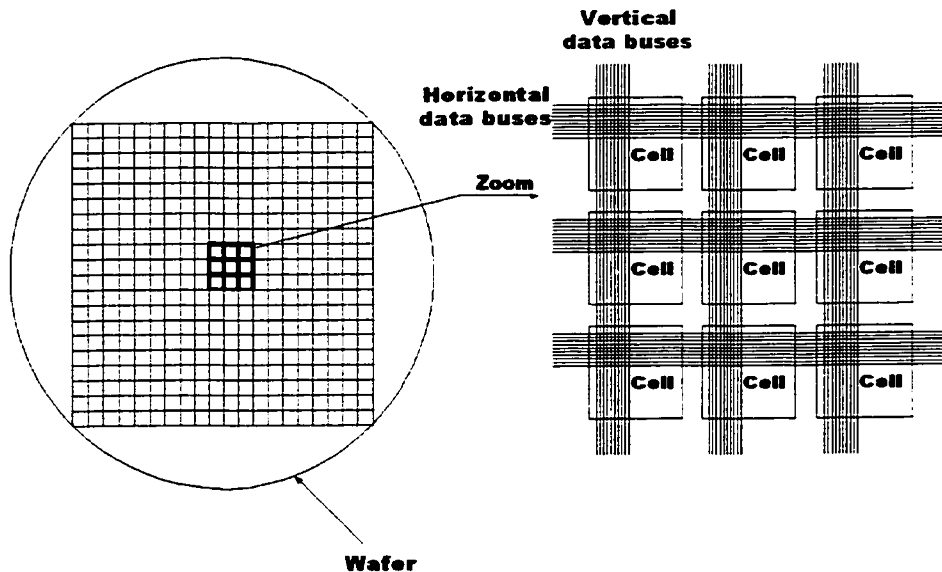


Figure 1.1 A proposed architecture organized as a processing array of size 20 x20.

The proposed architecture, as shown in Figure 1.1, contains complex vertical and horizontal interconnections running across a whole wafer. In a typical design, long wires are driven at more than 100 MHz, and as many as 400 cells could be organized as an array of size 20 by 20. When the architecture is implemented with WSI technology, it provides extreme-performance computing at low costs. However, the targeted unusual scale of

integration results in new problems that are not encountered in conventional ICs. In a nutshell, interconnection methods, electromagnetic compatibility, clocking and synchronization, power distribution, packaging, reconfiguration and yield analysis, testing, and thermal management need to be extensively studied.

The study in this thesis focuses on the yield analysis and modeling of the complex interconnection architecture that supports fault tolerance. Several authors have explored the design and analysis of fault-tolerant arrays [5][9][42]. Successful integration of these structures using large area ICs requires careful diagnosis and yield analysis [5][40]. Predicting the yield is necessary in order to define the number of redundant elements that must be added to the structure. Additionally, due to the interaction of sub-structures in this structure, the smaller defects may cause unusual constraints that cause the circuits unoperational even if fault tolerance schemes have been employed. As the structures involves these unusual constraints that are not taken into account in conventional reconfiguration strategies, existing yield models and reconfiguration strategies [4][16][17][18][20][38][39][46] cannot be applied directly. They must be revised and modified to take these constraints into account. Therefore, to determine the necessary redundancy for a given scale of integration, and to estimate the impact of varying defect densities, a yield model of this architecture needs to be developed.

1.3 Scope and organization of the thesis

In this thesis, a closed form yield model that takes into account constraints of the considered complex interconnection architecture is proposed. The impacts of the architectural constraints to yield are translated into yield losses. Yield losses are evaluated

by calculating the probability of observing non-tolerable defect patterns and by subtracting these probabilities from the yield of the arrays with global redundancy. Based on possible defect distributions in this architecture, corresponding yield models are developed. With these models, the sensitivity of the yield of the architecture to variations of the defect density is investigated. This thesis also proposes regression yield models that can be used to quickly predict when more redundancy is needed for given array and cell sizes.

This thesis is organized as follows. In chapter 2, the analysis of a complex interconnection architecture and the reconfiguration techniques used in the related circuit structure are presented. With the assumption of a random defect distribution, a yield model of the considered architecture that captures its specific constraints is presented in Chapter 3. A regression model that approximately predicts the yield of variable size arrays subject to changing defect density is proposed in this chapter as well. In Chapter 4, yield models of the architecture based on a clustered defect distribution are presented. Finally, in Chapter 5, the results of these investigations are summarized, the contributions are highlighted, and some directions for future study are suggested.

Chapter 2
Analysis of a Complex Interconnection Architecture

2.1 Introduction to fault tolerance mechanisms

Fault tolerance is the capability of a system to maintain its normal performance in an environment where faults occur. Applying fault tolerance techniques to the design of a large-area integrated circuit is required not only to enhance yield, but also to ensure reliability of a circuit. Especially for wafer-scale circuits, without fault tolerance, the yield of the circuits would be almost zero [6]. Therefore, to increase the yield of large-area circuits, on-chip fault tolerance is needed. Fault tolerance can be achieved by many techniques [2][11][13][14]. Among them, hardware redundancy and reconfiguration are of primary interest in this research.

The development of VLSI technology facilitates the physical replication of hardware units that provide the hardware redundancy in digital systems. Such redundancy is usually implemented by two approaches: the passive one and the active one. The passive approach uses the concept of fault masking to hide occurrence of faults and to prevent the faults from producing logical errors in a system. In a circuit with passive redundancy, the hardware is totally or partially triplicated or multiplicated to perform a majority vote to determine the output of the system. In other words, this approach achieves fault tolerance by masking the faults rather than detecting them. The active approach, however, aims at detecting the faults and reconfiguring the system in order to replace faulty modules with

spare modules. The major advantage of the active approach is that fault tolerance can be achieved with less redundant hardware in a system. Due to the need to implement fault detection and recovery mechanisms, the design of the system with active redundancy is more complicated. Moreover, the recovery process may disrupt the normal operation of a system.

When using active hardware redundancy in a system, a fault recovery mechanism is important. Fault recovery is part of a reconfiguration process that eliminates faulty units and restores the system to an operational state. Reconfiguration in VLSI systems has been broadly explored and investigated [25][43], particularly for a fault-tolerant array structure composed of a larger number of identical processing elements in a chip. Three specific types of reconfigurations can be identified: fabrication-time reconfiguration, compile-time reconfiguration and run-time reconfiguration. The key differences among them are the time when the reconfiguration is performed and whether the reconfiguration is permanent, as illustrated in the following.

(1)Fabrication-time reconfiguration is performed in a foundry, immediately after the fabrication of a processing array. So the reconfiguration can be done only once.

(2)Compile-time reconfiguration is performed in the field after an array has been operational for some period of time, and configuration is changeable.

(3)Run-time reconfiguration is used to achieve fault tolerance during the normal operation of a processing array. The configuration can be changed as needed.

Besides these differences, these reconfiguration processes are similar. Firstly, faulty processing elements are identified by test vectors. Then, a reconfiguration algorithm is used to determine an interconnection pattern that is to be used to connect fault-free

elements. Finally, a fully functional array is formed. Recovery techniques used to implement desired connections include physical repair techniques and electronic switch techniques. With the former, the interconnections of the array are physically altered by cutting or adding interconnections. This reconfiguration action is usually irreversible. Whereas, with the latter, the reconfiguration is reversible.

In general, run-time reconfiguration is the most difficult process, and fabrication-time reconfiguration may be the easiest. However, fabrication-time reconfiguration is not suitable for field applications, due to its permanent reconfiguration decisions. Compared with these two kinds of reconfigurations, the compile-time reconfiguration provides a good compromise in many cases. This reconfiguration is reversible and the design is not too complex, which makes it widely used in fault-tolerant arrays.

In the next section, a complex interconnection architecture using a compile-time reconfiguration technique is analyzed and discussed.

2.2 Complex interconnection architecture

In this sub-section, a complex interconnection architecture with fault tolerance schemes is investigated in order to undertake its subsequent yield analysis study. This architecture is a highly parallel processing array architecture that is proposed by Richard S.Norman of Hyperchip Inc. [27]-[29]. To make the related circuit structure of this architecture implementable with WSI, the new constraints that are encountered in this unusual scale of integration described in Chapter 1 are studied in our WSI project. Among these studies, Zhongfang Jing concentrated on the study of the signal integrity [49], Claude Thibeault

[50] proposed a basic implementation of the fault-tolerant structure, Meng Lu and others [47] implemented a demonstration chip to verify the concept of fault tolerance.

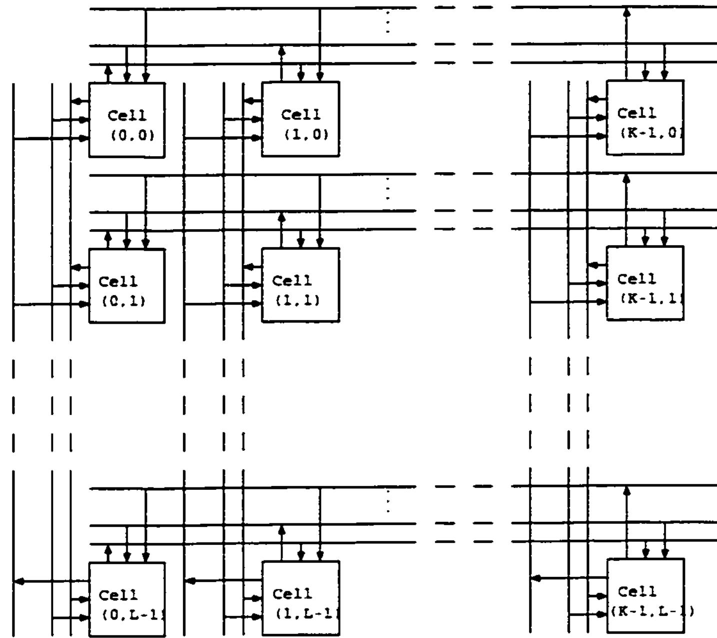


Figure 2.1 Processing array of size $K x L$ based on the architecture [27]-[29].

The architecture aims at implementing high speed computation for large data processing problems. To increase its bandwidth and realize a high throughput, a unique parallel interconnection structure is proposed. With this interconnection structure, each processing element, referring to a cell in this thesis, owns two communication bundles in each of horizontal and vertical directions. A cell can communicate with the other cells in the same row or column through its bundles as shown in Figure 2.1. Consequently, the considered architecture will possess a large number of horizontal and vertical interconnections when it comprises hundreds of cells. In addition, since wires are unidirectional and the structure must be completely regular, the number of the receivers and transmitters of a cell is doubled. For example, a physical array of size K x L based on this architecture has total $2K$ bundles in a row and $2L$ bundles in a column, and each cell

has (K+L-2) receivers and 2 transmitters. Because each bundle contains multiple wires, the number of interconnection wires across the array becomes very large. When the related circuit structure is implemented with WSI, fault tolerance is essential to attain an acceptable yield.

2.1.1 Overview of the fault-tolerant architecture

The purpose of fault tolerance in the architecture [27]-[29] is to enable forming a target array of N by M out of a physical array of K by L, with $N \le K$ and $M \le L$. A key point in the fault tolerance design is to minimize critical areas, also called chip-killing areas. Therefore, a reconfiguration logic connecting cells and bundles should be designed in such way that none of the faults in those cells and bundles is critical to the construction of the target arrays. Several different topologies of reconfiguration logic were taken into consideration. Generally, with more connections available for reconfiguration, arrays with increased robustness can be designed. But it should be noted that the larger number of the connections, the larger the area overhead and possibly lower the performance. Finally, the reconfiguration logic in this architecture was selected on the basis of an engineering trade-off.

An in-depth discussion of the fault-tolerant structure is beyond the scope of this thesis. We only describe the basic framework of the structure. In order to minimize the interference between long interconnection lines, a transposed line structure is designed for the interconnections of the array. Figure 2.2 presents the interconnection structure of such array of size 3x3. In addition, the compile-time reconfiguration with the electronic switching technique is used to reconfigure the system and to achieve fault tolerance when defects are present. In order to reduce the complexity of the reconfiguration logic, fault

detection can be implemented by a host computer. The obtained fault map is stored in an external storage. Thus, the reconfiguration circuits are limited to the links that carry reconfiguration signals to multiplexers. The setup of these multiplexers is implemented through a fault-tolerant scan chain across each cell [47], which is based on a boundary scan architecture (JTAG IEEE1149.1) [30].

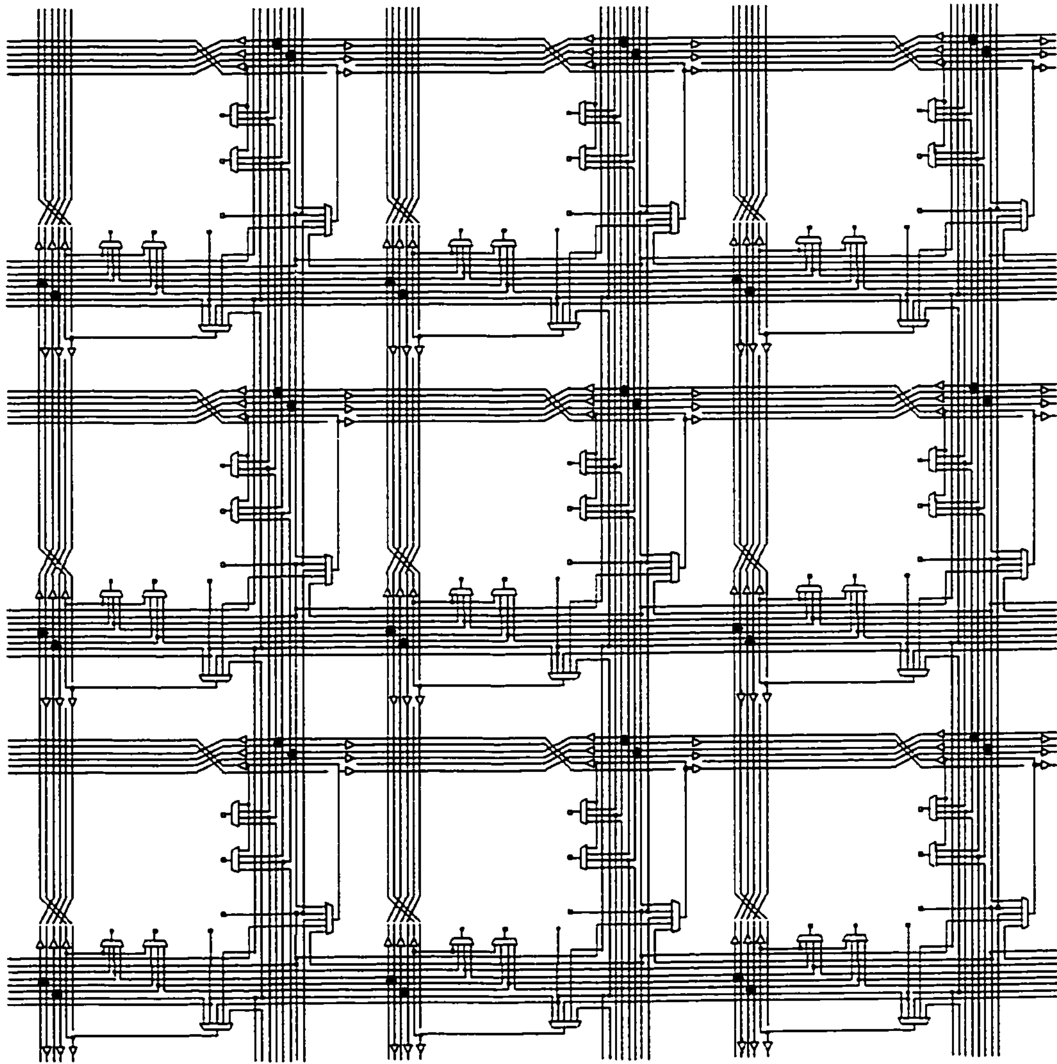


Figure 2.2 Interconnection structure of a physical array of size 3x3 based on the architecture [27]-[29].

2.2.2 Configuration of the transmitter multiplexers of a cell

The configuration of the transmitter multiplexers of a cell should be designed to make the cell not critical to the building of a target array, i.e., the cell can be replaced in case of fault. According to this rule, the configuration of the multiplexers is designed to enable 5 cells, the cell in question and its four nearest neighbors, to send their signals through these multiplexers. The configuration is shown in Figure 2.3. When a cell is defective, a good neighboring cell can replace it by using its natural bundles through the corresponding multiplexers. Moreover, when its multiplexers are defective, the cell can also send its signals through the multiplexers of one of its neighboring cells.

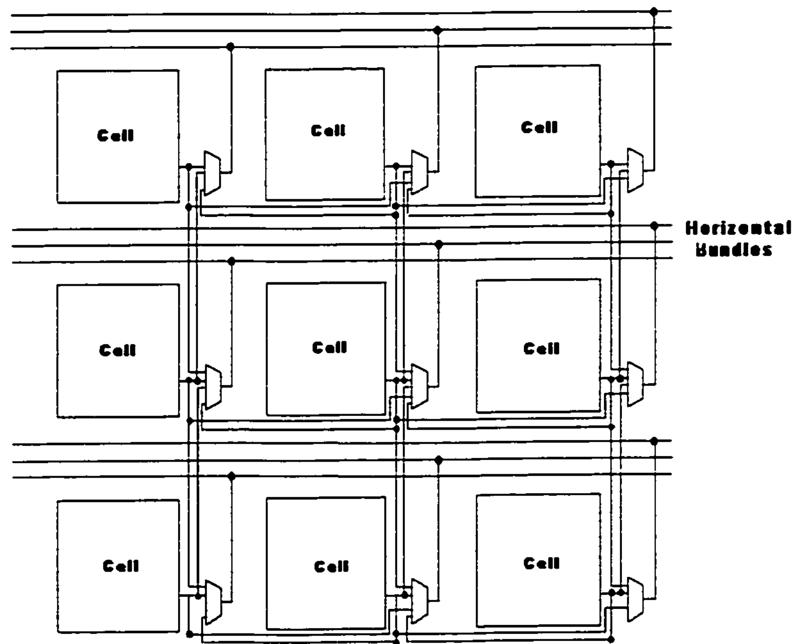


Figure 2.3 Configuration of the transmitter multiplexers of cells. In this diagram, only the multiplexers in the vertical direction are illustrated. Similar multiplexers are used in the horizontal direction.

In addition, it is clearly shown in Figure 2.4 that the configuration of a transmitter multiplexer makes a bundle replaceable. Through the multiplexers, a cell may use the

bundles originally owned by one of its four nearest neighboring when its natural bundles are defective. Similar to that, when a defective cell is replaced with a good neighboring cell, this good cell can send its signals through the bundles originally owned by the defective cell. For other cells receiving these signals, the defects in the cell are not perceptible. This provides a perfect replacement for defective cells. However, to implement this scheme, the configuration of the receiver multiplexers of a cell needs to possess the corresponding fault tolerance capability.

2.2.3 Configuration of the receiver multiplexers of a cell

In a K x L physical array that is used to form a logical array of N by M, each cell has (L+K-2) receivers to receive signals from (K-1) horizontal bundles and (L-1) vertical bundles. The physical array comprises (K-N) spare horizontal bundles and (L-M) spare vertical bundles. If no defect is present in the array, each cell can broadcast to the others in a physical row through its horizontal bundle. If a horizontal bundle is defective, the cell originally owning this bundle may send its signals through a spare horizontal bundle of one of its nearest neighboring cells. Other cells in the physical row must be capable of receiving the signals from the spare bundle. Therefore, in the horizontal direction, the configuration of the receiver multiplexers of each cell must be designed in such way that a cell can receive signals through bundles in its natural row and those in its nearest neighboring rows. The same is required in the vertical direction. A possible configuration of the receiver multiplexers of a cell is illustrated in Figure 2.4. In this figure, a physical array of 3x3 is taken as an example. From the figure, it is clear that each cell can communicate with other cells through bundles in its natural row or its two nearest rows. It can be noted that specific connections shown with thick lines, proposed by Meng Lu [47],

make it possible for the cells to receive signals from their natural bundles. This connections make bundle replacements more flexible. As a result, a defective bundle in a row can be replaced by a good spare bundle either in one of its two nearest rows, or within the same row. The former is called inter-bus replacement and the latter is called intra-bus replacement. The same is true for a bundle in a column.

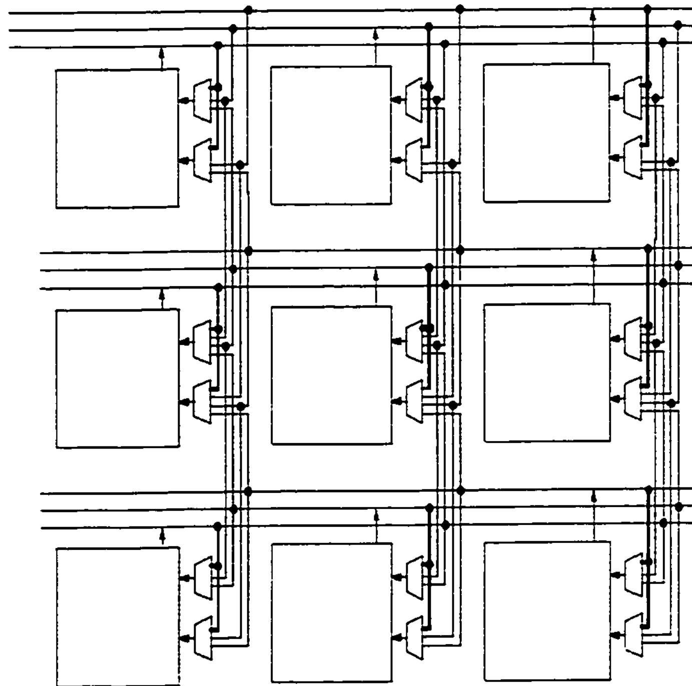


Figure 2.4 Configuration of the receiver multiplexers of cells in a 3x3 physical array. In this diagram, only the multiplexers in the vertical direction are illustrated. Similar multiplexers are also used in the horizontal direction.

With these multiplexers, a reconfiguration strategy is needed to implement the reconfiguration of the architecture when defects are present.

2.3 Reconfiguration strategies of the fault-tolerant structure

In this sub-section, because the yield of forming a target array relies heavily on the adopted strategies, the reconfiguration strategies used in the fault-tolerant structure are presented and analyzed. Two commonly used concepts in the theoretical analysis of the reconfiguration of processing arrays are first explained. These two concepts are physical array and logical array [21]. A physical array is an array that maps directly on the physical implementation and whose cells may be contaminated by manufacturing defects. A cell of a physical array is denoted by P(x,y), where x and y indicate the column and row position of the cell in the physical array, respectively. A logical array represents the desired array structure specified by the intended application as seen from external system parts. A cell in a logical array is denoted by L(x,y), where x and y indicate the logical column and row position of the cell in the desired array. In order to maximize the probability of a desired logical array being mapped to a physical array, reconfiguration strategies are needed.

2.3.1 Basic reconfiguration strategies

Using a reconfiguration strategy to map a logical array into a physical array aims at isolating, confining and overcoming defects in a physical array. The applications of reconfiguration strategies depend on constraints related to an architecture [8][9]. Because of the features of the fault-tolerant structure described in section 2.2, several basic reconfiguration strategies can be used. They are cell-stealing and cell-shifting, bundle-stealing and bundle-shifting, column or row exclusion strategy [25]. Some examples are presented below to illustrate applications of these strategies.

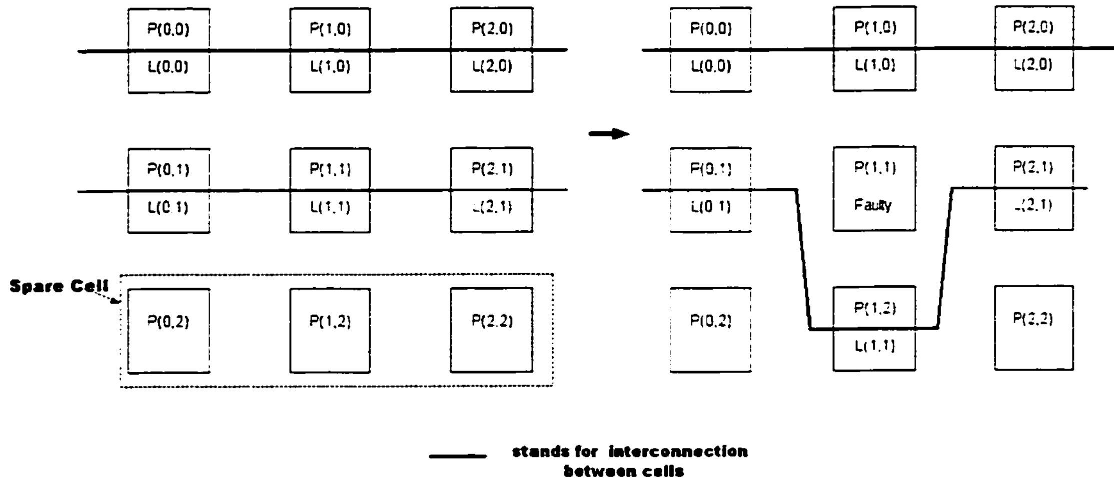


Figure 2.5 Example of using the cell-stealing strategy to construct a logical array of 2x3 out of a physical array of 3x3.

The cell-stealing strategy forms a logical array by replacing a defective cell with one of its nearest neighbors spare cells. Figure 2.5 shows such an example in which a logical array of 2x3 is formed out of a physical array of 3x3. Evidently a logical array of 2x3 can be directly constructed from the physical array of 3x3 if there is no defect in all cells. For instance, the logical cells L(i,j) (i=0,1 and j=0,1) of the logical array can be mapped directly into the physical cells P(i,j) (i=0,1 and j=0,1). When the physical cell P(1,1) is defective, a good spare cell in other row needs to be reconfigured to build a logical array. In this case, a good spare physical cell P(1,2) is stolen from the second row to form the logical array. Finally, the logical array is constructed by replacing the defective cell P(1,1) with the spare good cell P(1,2).

The cell-shifting strategy is to form a logical array by replacing a defective cell with a good spare cell that is not in its nearest neighboring position. Figure 2.6 shows the procedure of using the cell-shifting strategy to form a logical array of 2x2 from a physical

array of 3x2. When the cell P(0,0) is defective, the good spare cell P(2,0) is used to replace the defective one by shifting a cell one position at a time. Then, the logical array is obtained with L(0,0) being mapped to P(1,0) and L(1,0) to P(2,0).

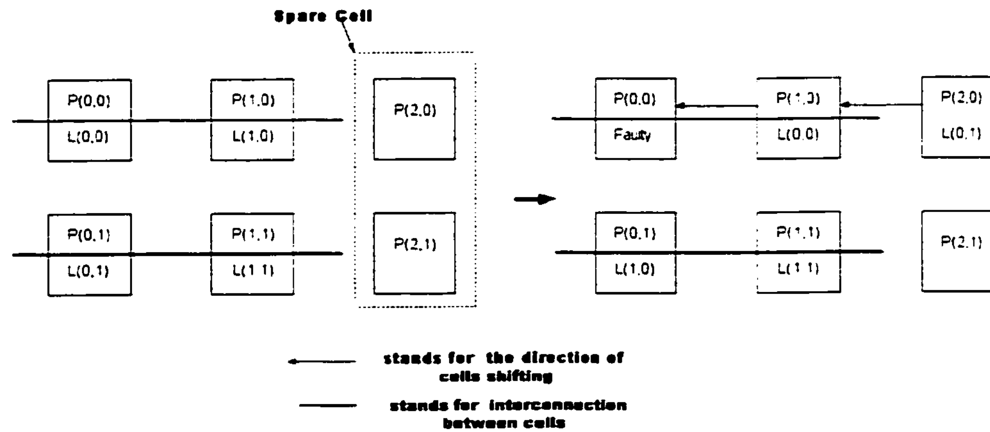


Figure 2.6 Example of using the cell-shifting strategy to construct a logical array of 2x2 out of a physical array of 3x2.

Similar to the cell-stealing strategy, the bundle-stealing strategy is to construct a logical array by replacing one defective bundle with one good spare bundle that is in a nearest neighbor position. Also the bundle-shifting strategy replaces a defective bundle with a good spare bundle that is not in its nearest neighbor position. Similar to the operation of cells, this replacement needs to be operated one position at a time as well.

The column or row exclusion strategy consists in eliminating a suitable set of columns or rows containing defective cells from a physical array to form a desired logical array. In this case, a number of good cells can be eliminated by the reconfiguration process. The set to be excluded should be carefully chosen to lower the cost. It is also a common practice to use good cells in the eliminated columns or rows as a pool of spare cells exploited through a cell shifting strategy. Figure 2.7 shows that a logical array of 2x2 is constructed from a physical array of 3x2 by excluding a column containing defective cells. In this case, the

position of spare cells is not specified. Because there are two defective cells in the second column, this column is excluded. Then, the logical 2x2 array is built with the physical cells in the first column and the third column.

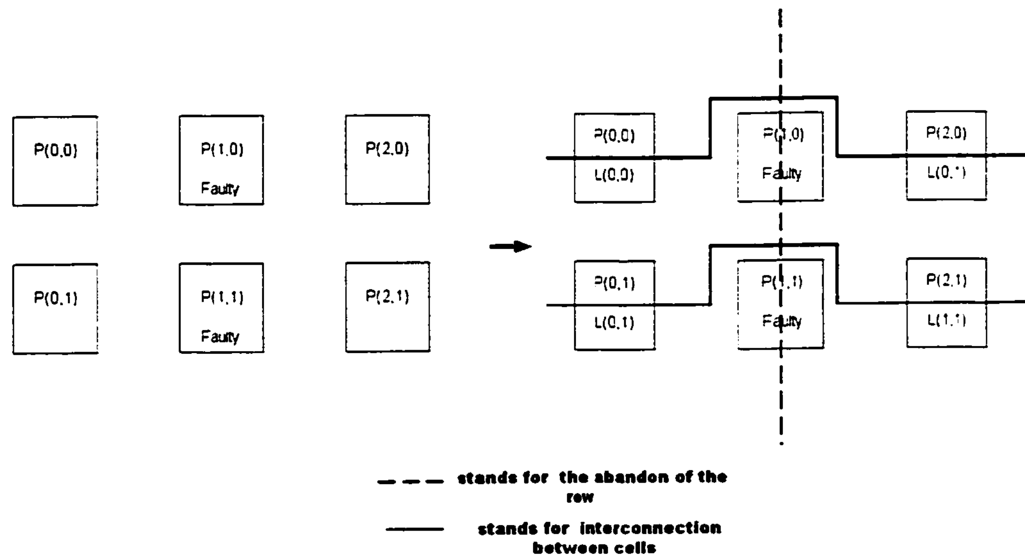


Figure 2.7 Example of using the column or row exclusion strategy to construct a logical array of 2x2 from a physical array of 3x2.

2.3.2 Reconfiguration of the cells in the fault-tolerant structure

In the fault-tolerant structure shown in the section 2.2, a cell can communicate with other cells in the same physical row or column through its natural bundles and other bundles of its four nearest neighbors as well. Accordingly, the cell-stealing and cell-shifting strategies can be accomplished by controlling the multiplexers of receivers and transmitters if the corresponding bundles are not defective.

Without loss of generality, Figure 2.8 shows an example of forming a logical array of 3x2 from a physical array of 3x3 with the cell-stealing strategy in the fault-tolerant structure. In this case, it is assumed that all spare cells are in the third row and bundles are

not defective. When the cell P(1,1) is defective, the good spare cell P(1,2) needs to be used to replace the defective one. Through reconfiguring the transmitter multiplexers of the cell P(1,1), its horizontal and vertical bundles can be used as the data channels of cell P(1,2). The cell P(1,2) can also receive signals from cells P(1,0) and P (0,1) by reconfiguring the multiplexers of its receivers. After reconfiguration, the targeted logical array is formed with logical cell L(1,1) being mapped into the physical cell P(1,2).

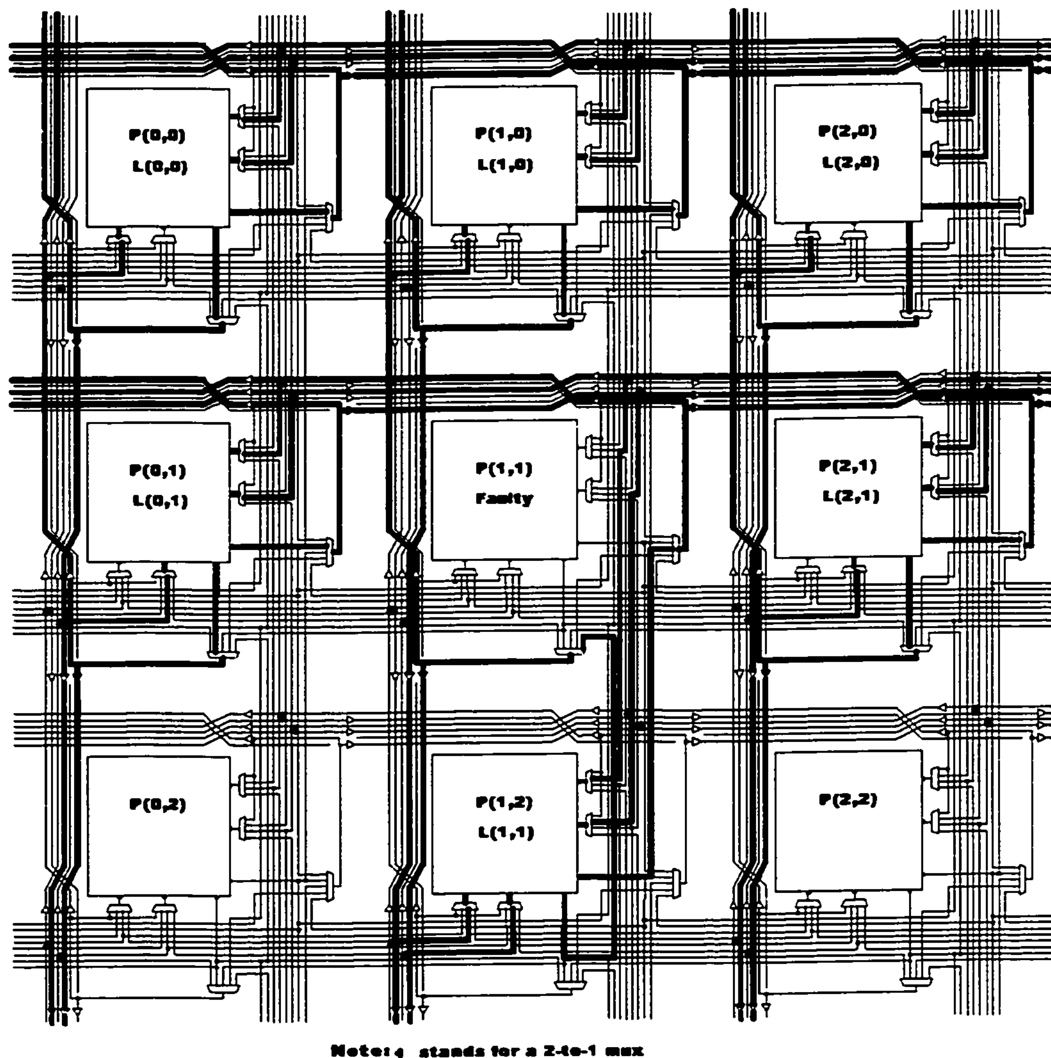
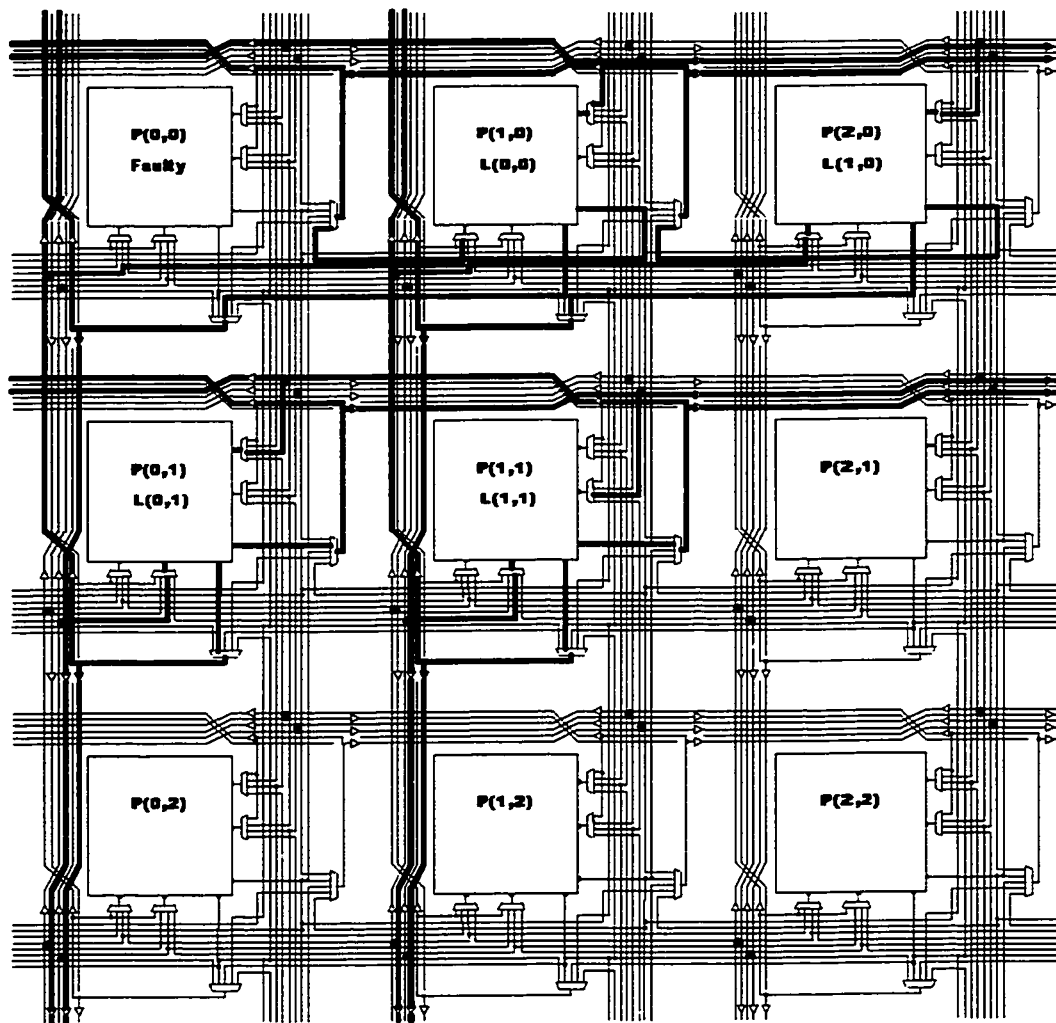


Figure 2.8 Using the cell-stealing strategy to construct a 3x2 logical array from 3x3 physical array based on the architecture in [27]-[29]. The thick lines illustrate the final reconfiguration.

The use of the cell-shifting strategy is shown in Figure 2.9 and Figure 2.10 with two example of building a 2x2 logical array from a 3x3 physical array. In these examples, it is assumed that no bundle is defective and the spare cells are in the third column and the third row. There are two possible approaches to realize this reconfiguration.



Note: stands for a 2-to-1 mux

Figure 2.9 Using the perfect replacement with the cell-shifting strategy to build a 2x2 logical array from 3x3 physical array.

The first is using the natural bundles of defective cells as shown in Figure 2.9. Because two bundles of the defective cell P(0,0) are finally owned by cell P(1,0), the defective cell

P(0,0) is perfectly replaced by left shifting the spare cell P(2,0). The perfect replacement can only be accomplished under the condition of the corresponding bundles being defect-free.

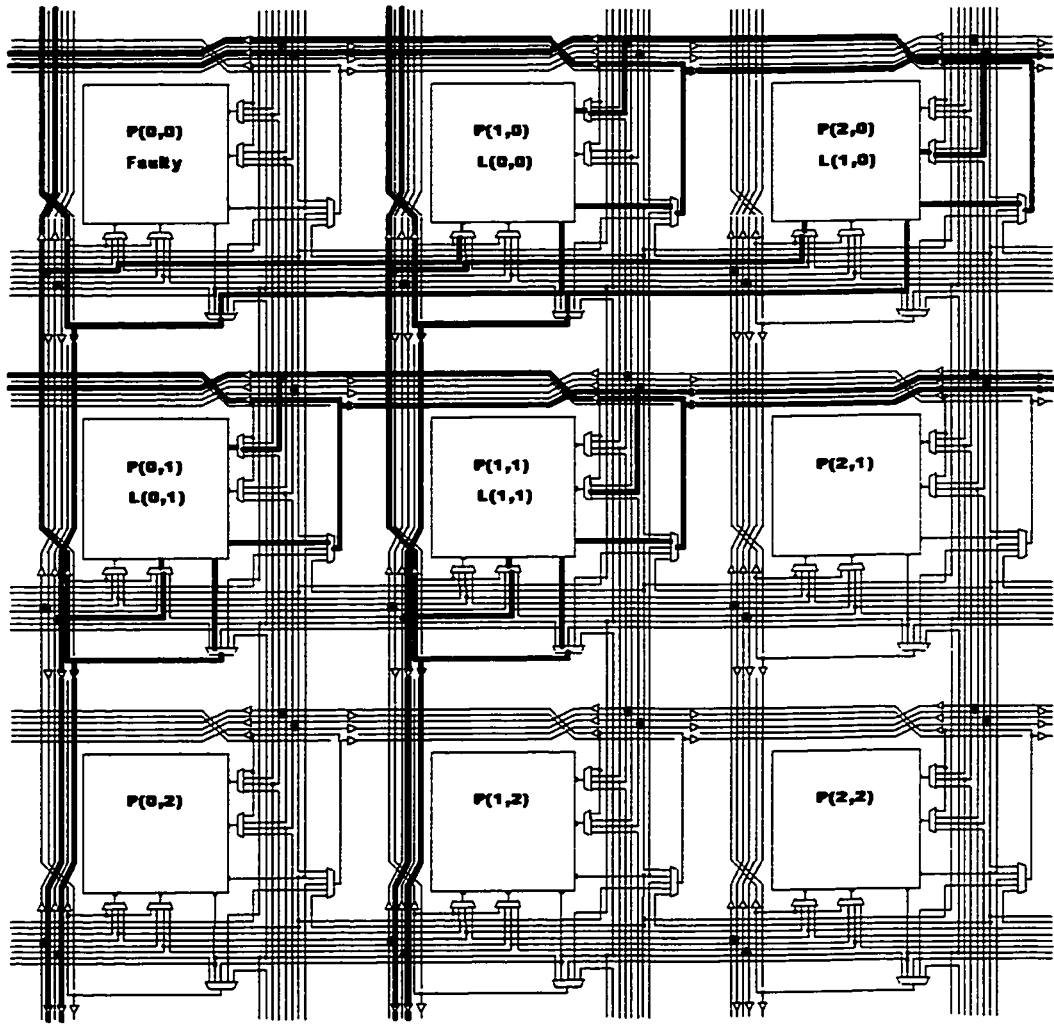


Figure 2.10 Using the imperfect replacement with cell-shifting strategy to construct a 2x2 logical array from a 3x3 physical array.

The second is that the bundles of defective cells are not be used. Figure 2.10 shows how this cell-shifting strategy can form a logical array of 2x2 out of a physical array of 3x3. In this case, the natural horizontal bundles of the defective cell P(0,0) are not used

when the good spare cell P(2,0) is left shifted. Because the spare cell and the defective cell are in the same physical row, the spare cell can communicate with the others in the same physical row with its original bundles.

2.3.3 Reconfiguration of the bundles in the fault-tolerant structure

The process of reconfiguring bundles in this structure is similar to that of cells. However, two kinds of bundle replacement methods somewhat different from cell replacement methods exist. They are intra-bus replacement and inter-bus replacement. The former replaces a defective bundle with a spare one in the same physical row and the latter operates in a different physical row. The operation of the intra-bus replacement is shown in Figure 2.11. In this case, the defective bundle is originally owned by the physical cell P(0,0) and the spare bundle is originally owned by the spare cell P(2,0). After reconfiguration, the cell P(0,0) owns the bundles originally belonging to the cell P(1,0), and the cell P(1,0) owns the spare bundle. Then, an intra-bus replacement operation is accomplished.

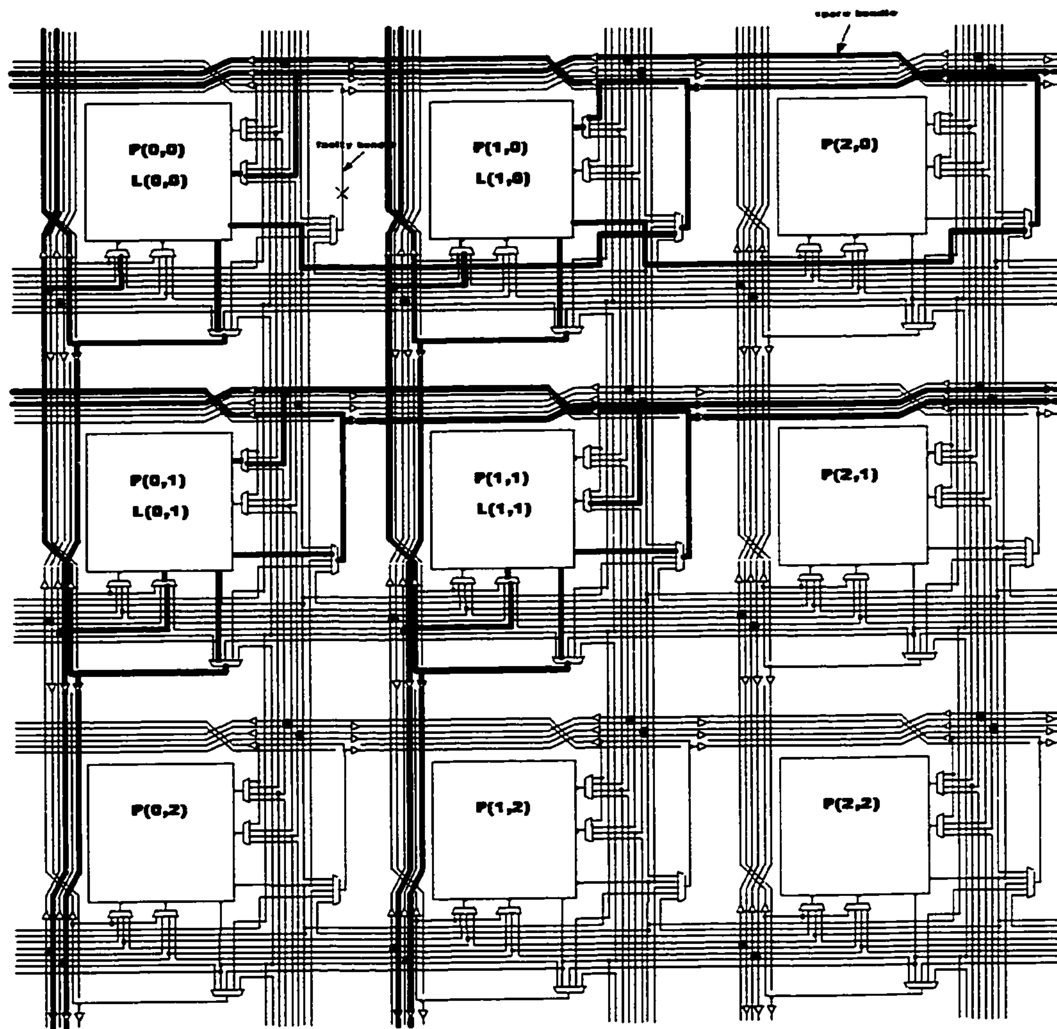


Figure 2.11 Intra-bus replacement in the fault-tolerant structure.

Figure 2.12 shows the inter-bus replacement operation. In this case, the bundle replacement is operated between three different physical rows. Through shifting the bundles one position at a time, the cell P(0,0) uses the bundle in the second row and the cell P(0,1) uses the bundle in the third row. Finally, a logical array of size of 2x2 is constructed.

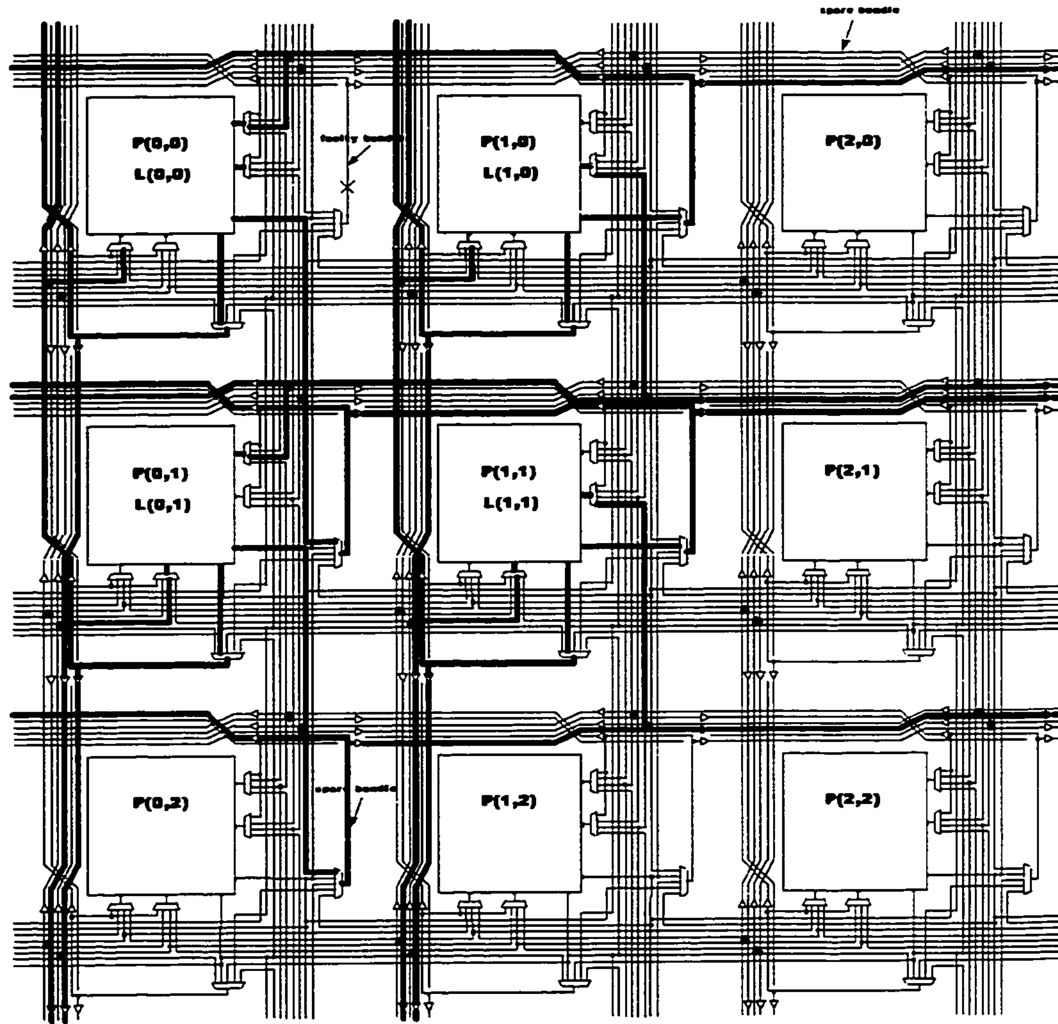


Figure 2.12 Inter-bus replacement in the fault-tolerant structure.

2.4 Summary

In this chapter, some fault tolerance mechanisms and a fault-tolerant architecture with complex interconnections have been described. A detailed analysis of the fault-tolerant configuration of this architecture and the basic reconfiguration strategies have been presented as well.

The architecture is a highly parallel processing array architecture that involves a large number of routing nodes. To enhance the yield, the reconfiguration logic is designed to enable the replacement of a defective cell with any of its nearest neighbor cells, as well as the replacement of the inter-bus or intra-bus bundles. Also, the structure can repair defects by repeatedly shifting spare cells and bundles one position at a time when building a logical array. As a first approximation, the structure can provide a global redundancy.

Chapter 3
Yield Modeling of a Complex Interconnection Architecture

3.1 Introduction to yield analysis and yield models

3.1.1 Defects and faults

The profitability of IC manufacturing depends heavily on the fabrication yield, which is defined as the fraction of the manufactured circuits that are good. Due to various manufacturing defects, 100% yield is impossible. Manufacturing defects, referring primarily to failures appearing during a production process and affecting the yield, can be classified into gross defects and random defects [35]. Gross defects are caused by manufacturing imperfections that result from the process being completely out of acceptable bound. They destroy a whole wafer or large parts of a wafer having no operational chip. Gross defects can usually not be recovered through fault tolerance techniques. Random defects are due to localized imperfections that occur during processing. Examples of random defects include missing contact windows, misaligned gates, and missing devices. Random defects are characterized as spot defects that are localized and randomly distributed over the whole wafer.

Both types of defects can contribute to yield losses. However, gross defects can be minimized and almost eliminated in mature and well-controlled manufacturing lines [20]. Comparatively, it is much more difficult to control spot defects in production lines. Consequently, the yield losses due to spot defects are much higher than those due to gross

defects. This is especially true for large area integrated circuits, since the occurrence of gross defects is almost independent of the chip size and the expected number of spot defects increases with the chip area [20]. Therefore, spot defects are of greater significance when yield enhancement is taken into account. In this thesis, only spot defects are taken into consideration in the yield analysis.

Not all spot defects result in circuit faults. A fault in a digital circuit is a logical difference between the behavior of a good and a bad circuit. Whether or not a defect will cause a fault depends on its location, its size, the layout and the density of the circuit. Only those defects that actually affect the circuit operation are called faults and are the ones causing yield losses [40]. Thus, for the purpose of yield estimation, the distribution of faults rather than that of defects is of interest.

3.1.2 Review of basic yield models

To model the yield for a circuit, some analytical probability functions that describe the expected spatial distribution of defects that cause faults are needed. From this point defects and faults will be used interchangeably to refer to defects that cause faults and impact on yield. Moreover, the yield models with respect to a certain defect distribution for the circuits that use fault tolerance techniques differ from those for the circuits that do not. In this sub-section, the yield models of a circuit without fault tolerance scheme is discussed.

The yield of a circuit without fault tolerance schemes can be evaluated with the probability of no defect occurring in the whole circuit area. If x denotes the number of defects in the circuit, the yield, $Y_{circuit}$, is given by

$$Y_{circuit} = P(x = 0) \qquad (3.1)$$

Where, $P(x)$ is a probability distribution function of defects.

The earliest probability distribution function used to predict the yield of ICs was derived from the random Poisson model. Using that model, the probability of a circuit having x defects is given as follows.

$$P(x) = \frac{e^{-\lambda}\lambda^{x}}{x!} \tag{3.2}$$

Here, λ is the expected number of defects in the circuit.

When there is no defect in a circuit, the yield is obtained by substituting $x=0$ into (3.2). Then, (3.1) becomes,

$$Y_{circuit} = e^{-\lambda} = e^{-DA} \tag{3.3}$$

Where, D is the defect density of the circuit and A is its critical area, with $\lambda = DA$.

For small area circuits, the Poisson model works reasonably well. However, when the sizes of circuits grow, using the Poisson model to predict yields becomes increasingly inappropriate, because it tends to underestimate the yield of larger circuits [19][24][37]. Several approaches have been proposed to modify the Poisson model to reflect clustered yields. Among them, B.T.Murphy [23] assumed the defect density D is a random variable and proposed the following yield equation.

$$Y_{circuit} = \int_{0}^{\infty} e^{-DA} f(D)\,dD \tag{3.4}$$

Here, $f(D)$ is a normalized probability distribution function of the defect density D.

Based on (3.4), using the gamma distribution for $f(D)$, Stapper [33] proposed the probability distribution function presented in (3.5). This is the well-known negative

Binomial distribution, which leads to a corresponding yield model, the negative Binomial model given in (3.6).

$$P(x) = \frac{\Gamma(x+\alpha)(\lambda/\alpha)^x}{x!\Gamma(\alpha)(1+\lambda)^{x+\alpha}} \tag{3.5}$$

$$Y_{circuit} = \left(1 + \frac{\lambda}{\alpha}\right)^{-\alpha} \tag{3.6}$$

where α is referred to the clustering parameter, a property of the IC manufacturing process.

With (3.6), the Poisson model and the other yield models proposed in [41] can also be evaluated by selecting an appropriate clustering parameter α. When α is low, the defects tend to be more clustered [33]. Conversely, when α is high, the shape of the gamma distribution approaches that of the Poisson distribution, and the defects tend to be randomly distributed.

In fact, because the random defect distribution does not reflect the phenomenon of clustering defects in ICs, it can lead to predicting low yields in many cases. Stapper and his colleagues [40] investigated yield modeling issues extensively throughout the 1980s. They came to the important conclusion that the yield of large chips such as microprocessors and application specific integrated circuits (ASICs) is not only a function of the chip area, but also is related to features of different manufacturing processes. The introduction of the defect clustering parameter in the negative Binomial model can reflect the chip-to-chip variations in defect densities.

The negative Binomial yield model is found to be satisfactory for the yield prediction of a circuit without fault tolerance schemes. However, if the circuit uses fault tolerance

schemes in the form of redundant components, the evaluation of its yield requires a more elaborate statistical model.

3.1.3 Yield modeling for circuits with redundant structures

A well-known method to tolerate faults and defects in an integrated circuit is adding redundancy in the circuit. Its yield can be evaluated by calculating the probability that it contains enough defect-free basic blocks for proper operation. To compute the probability, a detailed statistical model is needed. This model should provide information about the distribution of defects over partial areas of the circuit, and possible correlations among defects in different sub-areas. Several authors have explored and developed yield models for circuits with redundancy [17][18][26][34][44]. Developing an accurate yield model needs a great deal of insight regarding the structure of a circuit and the fault tolerance schemes used in this circuit.

A general yield formula was proposed based on the Poisson model (3.1), and its derivative, the compound Poisson model [17][26]. In this approach, it is assumed that a circuit is composed of N identical sub-circuits, called modules in the literature, including R spare modules. The circuit can function correctly when it contains at least N-R defect-free modules. Therefore, the yield equation of the circuit is derived by calculating the probability of M out of N modules being defect-free, where $M \geq N - R$. This expression assumes that defects in any module are distributed according to the Poisson distribution, and that modules are statistically independent of each other. In that case, the yield formula is given by

$$Y = \sum_{M = N - R}^{N} \binom{N}{M} (e^{-AD})^{M} (1 - e^{-AD})^{N - M} \tag{3.7}$$

Where, $A(\text{cm}^2)$ is the area of a module and $D(\text{cm}^{-2})$ is the defect density of a module.

This formula corresponds to an idealization. Indeed, in practice, circuits rarely consist entirely of identical modules. A more general case is that a circuit is composed of multiple types of modules, each with its own redundancy. In that case, the yield equation of the circuit composed of n types of modules can be derived. Let N_i denote the number of type i modules, out of which R_i are spares. In this case, the yield is given by the following equation.

$$Y = \sum_{M_1 = N_1 - R_1}^{N_1} \cdots \sum_{M_i = N_i - R_i}^{N_i} \cdots \sum_{M_n = N_n - R_n}^{N_n} \binom{N_1}{M_1}\left(e^{-A_1 D_1}\right)^{M_1}\left(1 - e^{-A_1 D_1}\right)^{N_1 - M_1} \cdots$$

$$\binom{N_i}{M_i}\left(e^{-A_i D_i}\right)^{M_i}\left(1 - e^{-A_i D_i}\right)^{N_i - M_i} \cdots \binom{N_n}{M_n}\left(e^{-A_n D_n}\right)\left(1 - e^{-A_n D_n}\right)^{N_n - M_n} \quad (3.8)$$

Here, M_i is the number of defect-free type i modules, A_i is the area of type i modules, and D_i is the defect density of type i modules.

Equations (3.7) and (3.8) show a general method to develop the yield model of a chip with redundancy. Although the Poisson distribution used in both equations does not match actual defect and fault data very well, it provides an easy way to calculate the yield with an approximation that indicates the yield trend. Moreover, these equations were deduced by using an ideal model that does not take into account the interaction of different modules even though such interaction often exists. For example, when a module is defective, it can affect other modules, and make a circuit dysfunctional. Therefore, even if there are available spare modules, specific combinations of defective modules can also make a circuit operate incorrectly. To model the yield for a complex interconnection architecture,

we need to take into account not only several kinds of modules in the structure, but also some specific combinations of them.

3.2 Yield modeling for a complex interconnection architecture

3.2.1 Constraints-based yield model

The architecture proposed in [27]-[29] is mainly composed of four parts as described in Chapter 2: identical cells, vertical and horizontal interconnection bundles between cells, and reconfiguration logic. The reconfiguration of the structure is implemented through a scan chain across all cells, which is based on the boundary scan architecture (JTAG[27]). These parts and the scan chain have different effects on the yield of the structure, and the impact of these effects on the yield can be estimated respectively with a simple yield model (3.6). The results of the computation of the yield of those parts are illustrated in Table 3.1 and 3.2. In this numerical analysis, an array of 20x20 based on [27]-[29] is used, and the parameters used are obtained from the proposed WSI architecture and the fault-tolerant demonstration chip that is presented in [47]. In the demonstration chip, the scan chain was designed without fault tolerance. Consequently, the scan chain may become the only critical circuit in this chip, i.e., any fault of the scan chain cannot be tolerated.

Table 3.1 Yield of a bundle, a cell, and the reconfiguration logic belonging to one cell. The data is obtained from a WSI demonstration chip designed and fabricated as part of a Hyperchip R&D projects. In this chip, each bundle comprises 4 wires. Random defect density D_0=1963 m^{-2} and the clustering parameter α=5 were used from ITRS[12]. The yield of a 20x20 array, with an area 1.04×10^2 cm^2, without fault tolerance is 2.94×10^{-4}.

	Reconfiguation logic in a cell	Bundle	Cell	Scan chain within a cell
Critical Area (cm^2)	1.1×10^{-4}	4.3×10^{-3}	2.5×10^{-1}	4.0×10^{-4}
D_0A	2.16×10^{-5}	8.44×10^{-4}	4.91×10^{-2}	7.85×10^{-5}
Yield	0.999978	0.999156	0.952314	0.999922

Table 3.2 Yield of a bundle, a cell, and the reconfiguration logic belonging to one cell. The data is obtained from the proposed WSI architecture in Hyperchip R&D projects. In this case, each bundle comprises 40 wires. Random defect density D_0=1963 m^{-2} and the clustering parameter α=5 were used from ITRS[12]. The yield of a 20x20 array with an area 2.56×10^2 cm^2 is 6.06×10^{-4}.

	Reconfiguation logic in a cell	Bundle	Cell	Scan chain within a cell
Critical Area (cm^2)	2.8×10^{-2}	9.6×10^{-2}	2.5×10^{-1}	1.4×10^{-3}
D_0A	5.50×10^{-3}	1.88×10^{-2}	4.91×10^{-2}	2.75×10^{-4}
Yield	0.994522	0.981366	0.952314	0.999725

From Table 3.1 and 3.2, it is seen that the yield of the reconfiguration logic of a cell is much higher than that of a cell or a bundle because of its relatively small area. Thus, the yield loss contributed by the reconfiguration logic is not significant. Furthermore, available design techniques can make potentially critical signals robust to the presence of defects [3][15][31]. Applying such techniques to the low complexity reconfiguration logic can make its yield much closer to 1 than computed in Table 3.1 and 3.2. The small

resulting yield reduction, due to defects in the simple robust reconfiguration logic described in Chapter 2, can be accounted for by a multiplying factor close to 1 that would derate the yield. Accordingly, in the yield analysis of this structure, the assumption of reconfiguration logic being defect-free is reasonable. From Table 3.1, it is clear, that the yield loss contributed by the scan chain in the demonstration chip is insignificant and the effect of the scan chain on the yield can also be expressed as a multiplying factor close to 1. But when a scan chain without fault tolerance schemes is used in the proposed WSI architecture, with each part of the scan chain within a cell assumed statistically independent, the yield of the scan chain across 400 cells is equal to 0.8958. When the scan chain is designed with fault tolerance [47], it is no longer critical to the structure and the yield loss contributed by the scan chain can be incorporated into that of cells. Form the above analysis, it is concluded that, in the yield modeling, cells, vertical bundles and horizontal bundles are the main concern. In addition, it is also implicitly assumed that existing robust methods of dealing with defects in critical signals are applied, such that normal spot-defects almost always lead to unusable cells or bundles, and do not invalidate the test and reconfiguration mechanisms. With the assumption of fault-free reconfiguration logic, a simplified diagram of the fault-tolerant structure is used to illustrate our model. Figure 3.1 shows a simplified diagram for a typical 8x8 array.

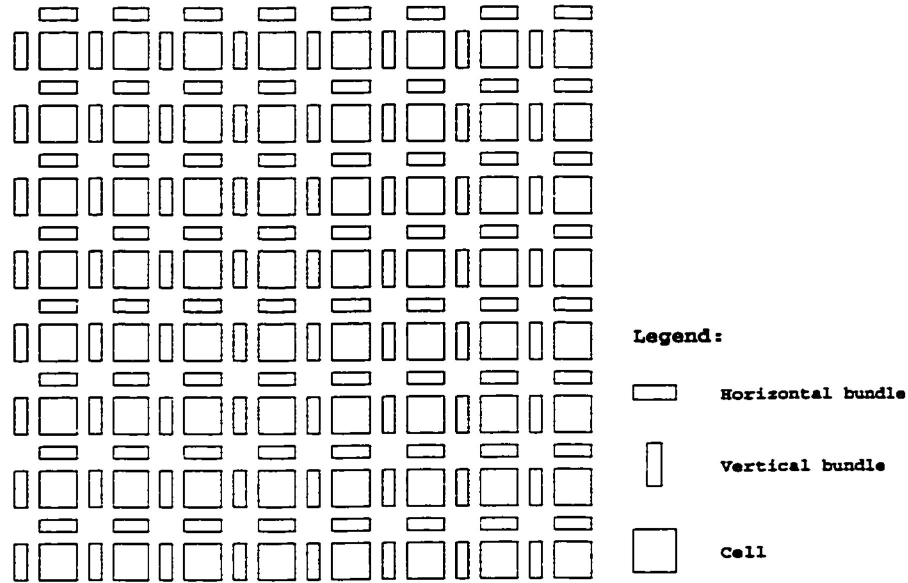


Figure 3.1 Simplified diagram of a 8 by 8 physical array based on the architecture in [27]-[29].

In this figure, a horizontal rectangle represents a horizontal bundle and a vertical rectangle represents a vertical bundle, while the squares represent cells. Each cell owns one bundle in the horizontal direction and another one in the vertical direction, and can communicate with the other cells in the same column or row through its bundles. To simplify the diagram, the connections between bundles and cells are not shown. The objective with this fault-tolerant architecture is to form a logical array sized N by M out of a physical array of size K by L with $N \leq K$ and $M \leq L$. With the reconfiguration logic, a physical cell in the physical array can replace any of its nearest neighbors. When a cell broadcasts to other cells of a physical row, it can do so by using bundles from its natural row or from nearby spare bundles. The same is true for vertical bundles. It may appear that this architecture can only repair defects by shifting cells by one or a few positions, but by repeatedly shifting cells and bundles one position at a time, a spare at one corner of the array can be used to replace a defect at the other corner of the array, when building a

logical array that is arranged to use only good cells and bundles. As a first approximation, the structure provides global redundancy. It does so successfully when defects are sparse, which is the case when the probability of individual cell and bundle being defective is low. However, practical implementations are limited by the number of reconfiguration wires. Several different topologies of the reconfiguration multiplexers were considered. Generally, with more reconfiguration wires, we can design arrays with an increased robustness. In a configuration that is based on an engineering trade-off, the array has constraints. Some distributions of defective bundles and defective cells prevent construction of an adequate logical array. An example of this kind of patterns is illustrated in Figure 3.2. In this example, a logical array of 3 by 3 intends to be built from a physical 4 by 3 array. The physical array contains 3 spare cells, 3 spare vertical bundles and 3 spare horizontal bundles. However, when three cells (C1 to C3) and three horizontal bundles (HB1 to HB3) are defective as shown in Figure 3.2, the position of three defective horizontal bundles prevents the usage of the good cell, C0. Thus, only 8 good cells instead of 9 ones are available, and the logical array cannot be formed. Therefore, this kind of defective cells and bundles cannot be tolerated. In this thesis, this kind of distributions that cannot be tolerated are referred as non-tolerable patterns.

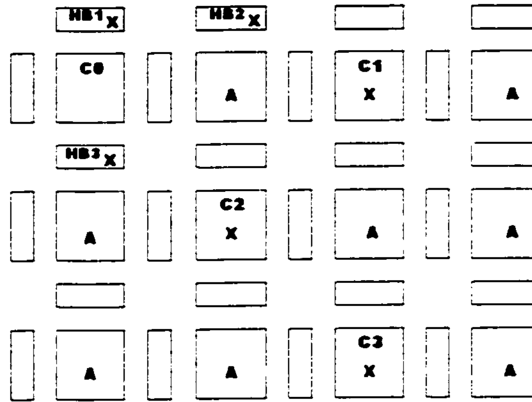


Figure 3.2 Pattern preventing the construction of a logical array size of 3 by 3 out of a physical array of 4x3. The symbol "X" stands for defective cell or bundle, and "A" for available cells

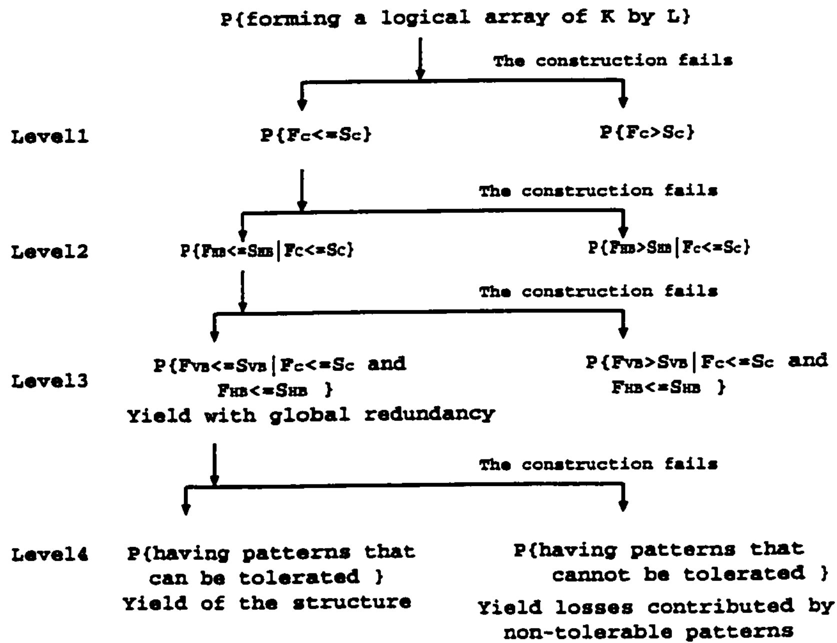


Figure 3.3 Flow chart of the probability of forming a logical array. F_c is the number of defective cells, F_{HB} is the number of defective horizontal bundle, F_{VB} is the number of defective vertical bundle, S_c is the number of spare cells, S_{VB} is the number of spare vertical bundles, and S_{HB} is the number of spare horizontal bundles.

Generally, there are several possibilities that prevent the construction of a logical array. According to the cause that prevents the construction of a logical array, they are classified as two major types. First, when there are not enough spares to replace the defects in the

structure, the construction fails. In other word, the structure must simultaneously contain enough spare cells, spare horizontal bundles and spare vertical bundles to tolerate the respective defects. Second, non-tolerable patterns occur in the structure. Figure 3.3 shows the probability of the events of forming a logical array. From this figure, it is known that the yield of the architecture can be evaluated with the probability of having tolerable patterns in the structure and it can be expressed as in (3.9).

$$Y_{chip} = Y_{global} - Y_{loss} \tag{3.9}$$

where Y_{chip} is the true yield of the structure, Y_{global} is the yield of the structure with global redundancy, which would be observed if the structure had no constraint, and Y_{loss} is the probability to have non-tolerable defect patterns. In addition, the number of defective cells and bundles must be smaller than the respective number of spare cells and bundles.

Based on Equation (3.8), an analytical expression of Y_{global} is presented in (3.10). This expression assumes that defects in cells, vertical bundles and horizontal bundles are statistically independent, and that they comply with the binomial distribution.

$$Y_{global} = \sum_{F_c=0}^{S_C} \sum_{F_{VB}=0}^{S_{VB}} \sum_{F_{HB}=0}^{S_{HB}} \binom{Q_c}{F_c}\binom{Q_{VB}}{F_{VB}}\binom{Q_{HB}}{F_{HB}} (y_{cell})^{Q_c-F_c} (1-y_{cell})^{F_c} (y_{VB})^{Q_{VB}-F_{VB}} (1-y_{VB})^{F_{VB}} (y_{HB})^{Q_{HB}-F_{HB}} (1-y_{HB})^{F_{HB}} \tag{3.10}$$

In (3.10), y_{cell} is the yield of a cell, y_{HB} is the yield of a horizontal bundle, and y_{VB} is the yield of a vertical bundle. Q_c is the total number of cells, Q_{VB} is the total number of vertical bundles, and Q_{HB} is the total number of horizontal bundles. F_c is the number of defective cells, F_{HB} is the number of defective horizontal bundle, and F_{VB} is the number of defective vertical bundle. S_c is the number of spare cells, S_{VB} is the number of spare

vertical bundles, and S_{HB} is the number of spare horizontal bundles. In this case, y_{cell}, y_{HB} and y_{VB} can be expressed by the negative Binomial yield model (3.6) or the Poisson yield model (3.3). Using the negative Binomial yield model, they are given as:

$$y_{cell} = \left(1 + \frac{D_c A_c}{\alpha}\right)^{-\alpha} \quad (3.11)$$

$$y_{VB} = \left(1 + \frac{D_{VB} A_{VB}}{\alpha}\right)^{-\alpha} \quad (3.12)$$

$$y_{HB} = \left(1 + \frac{D_{HB} A_{HB}}{\alpha}\right)^{-\alpha} \quad (3.13)$$

The equation of Y_{loss} is expressed as:

$$Y_{loss} = \sum_{i} (Y_{NTP})_i \quad (3.14)$$

Where, $(Y_{NTP})_i$ is the yield loss contributed by the ith non-tolerable pattern of the structure.

An analytical expression for $(Y_{NTP})_i$ is attained from (3.10) by replacing the binomial coefficient $\binom{Q_c}{F_c}$ with NTC_{cell}, $\binom{Q_{VB}}{F_{VB}}$ with NTC_{VB} and $\binom{Q_{HB}}{F_{HB}}$ with NTC_{HB}. The expression of $(Y_{NTP})_i$ is given by:

$$(Y_{NTP})_i = \sum_{F_c=0}^{S_C} \sum_{F_{VB}=0}^{S_{VB}} \sum_{F_{HB}=0}^{S_{HB}} (NTC_{HB})(NTC_{VB})(NTC_{cell})(y_{cell})^{Q_c - F_c}(1 - y_{cell})^{F_c}$$

$$(y_{VB})^{Q_{VB} - F_{VB}}(1 - y_{VB})^{F_{VB}}(y_{HB})^{Q_{HB} - F_{HB}}(1 - y_{HB})^{F_{HB}} \quad (3.15)$$

Here, NTC_{cell} is the number of non-tolerable patterns when F_c defective cells are distributed over the physical array, NTC_{VB} is the number of non-tolerable patterns when F_{VB} defective vertical bundles are distributed over the array, and NTC_{HB} is the number of non-tolerable patterns when F_{HB} defective horizontal bundles are distributed over the array.

From (3.15), it is clear that the non-tolerable patterns resulting in significant yield losses need to be identified in order to evaluate the yield loss.

3.2.2 Non-tolerable patterns in an array of designated size

Finding all significant non-tolerable basic patterns proved difficult but tractable. It requires a great deal of insight regarding the operation of the fault-tolerant structure. Our study is focused on analyzing an array of physical size $(N+1)\text{x}N$, out of which a $N\text{x}N$ logical array is targeted. The significant patterns that cannot be tolerated can be found through studying the limits of the interconnection structure.

3.2.2.1 Non-tolerable patterns in an array with fault-free bundles.

In this subsection, the non-tolerable patterns are studied from a simple case with the assumption that bundles are defect-free in an array. The conclusion obtained from these non-tolerable patterns can be extended to the case where defects can be distributed to the whole structure. From the previous analysis, it is known that the yield loss depends on the distribution and the number of non-tolerable patterns in the structure. Thus, the study of non-tolerable patterns is concentrated on these issues.

After a detailed analysis of the operation and the constraints of the fault-tolerant structure, thirteen kinds of important non-tolerable patterns are identified. For brevity, only the pattern that contributes most yield loss is illustrated here and others are explained in Appendix B. Figure 3.4 shows this pattern corresponding to the case where six cells (C1-C6) in the corner of an array are defective. In this case, because a spare cell can be shifted only one position at a time, the position of this pattern composed of defective cells (C1-C6) prevents two defective cells C1 and C2 from being replaced by good spare cells. Moreover, because of the limit of the number of spare columns in the physical array of

(N+1)xN, only one column can be excluded to form the targeted logical array of NxN with the row or column exclusion strategy described in Chapter 2. Consequently, there must be a logical column that cannot be formed because of the lack of enough good cells. Figure 3.5 shows one typical example of unsuccessful construction of the logical array. In this example, the first physical column is excluded and its cells are used as spares. With this pattern, the defective cell C2 cannot be replaced. As a result, the second physical column can not be mapped as a logical column.

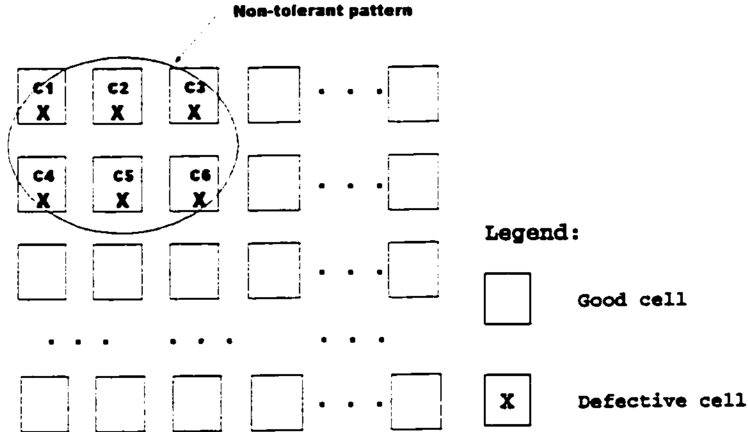


Figure 3.4 Non-tolerable pattern composed of the least number of defective cells in an array without defective bundles.

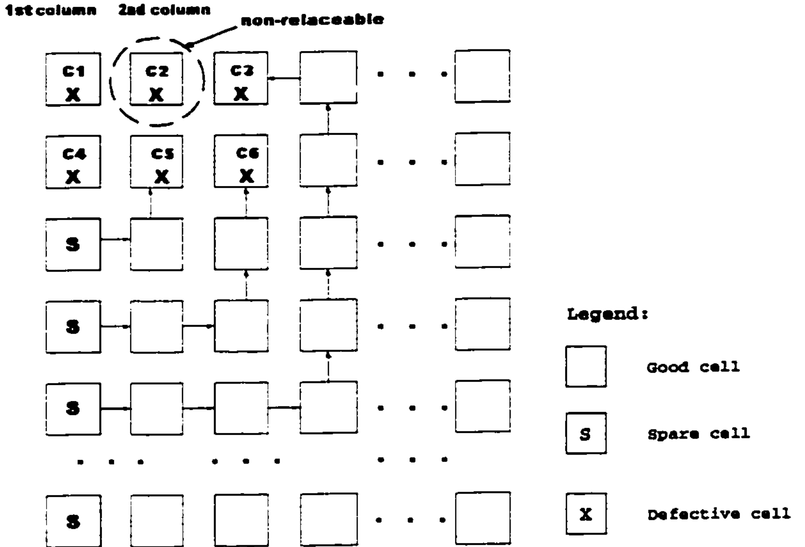


Figure 3.5 Six defective cells in a corner prevent the construction of a logical array of NxN. The arrow shows the direction of cell-shifting.

The total number of this kind of non-tolerable patterns can be computed with the equation $NTC_{cell} = \binom{4}{1}\binom{(N_c+1)N_c-6}{F_c-6}$. Although this total number contains some intersections with every two to 4 corner cell combinations, these intersections contain very few patterns and they are neglected.

The probability of a non-tolerable pattern occurring in the structure can be calculated with (3.16) which is based on (3.7) with $\binom{N}{M}$ replaced by NTC_{cell}.

$$Y_{(NTP)_1} = \sum_{F_C=0}^{S_C} NTC_{cell}(y_{cell})^{Q_c-F_C}(1-y_{cell})^{F_C} \tag{3.16}$$

Using (3.16) and (3.11), the numerical results of the yield losses contributed by thirteen kinds of non-tolerable patterns are obtained and they are shown in Table 3.3. From Table 3.3, it is clear that the yield losses contributed by the first five kinds of patterns constitute most of the yield losses due to non-tolerable cell patterns, and that most of the patterns that contribute significant yield losses are distributed in the corner or edge of the physical array. This shows the fact that yield losses contributed by those patterns with large number of defects decrease very rapidly; thus, they become neglectable.

Table 3.3 Yield losses contributed by thirteen kinds of significant non-tolerable patterns in the construction of a logical array of NxN from a physical array of (N+1)xN. The results are obtained with the area of a cell 25 mm^2, random defect density D_0=1963 m^{-2}, the clustering parameter α=5, and the yield of a cell is 0.95.

Pattern Number	Number of defective cells	Yield Loss	Relative Contribution	Cumulative Ratio
1	6	1.44×10^{-9}	96.9612%	96.9612%
2	7	3.59×10^{-11}	2.4173%	99.3785%
4	8	8.18×10^{-12}	0.5508%	99.9293%
3	8	8.61×10^{-13}	0.0579%	99.9872%
5	9	1.77×10^{-13}	0.0119%	99.9991%
6	10	7.64×10^{-15}	5.1448×10^{-6}	99.99999%
7	10	4.03×10^{-15}	2.7138×10^{-6}	99.99999%
8	12	1.28×10^{-17}	8.6195×10^{-9}	99.99999%
9	12	1.28×10^{-17}	8.6195×10^{-9}	99.99999%
10	12	1.08×10^{-17}	7.2727×10^{-9}	99.99999%
11	13	9.11×10^{-19}	6.134×10^{-10}	99.99999%
12	15	7.87×10^{-22}	5.2997×10^{-13}	99.99999%
13	18	4.46×10^{-27}	3.0034×10^{-18}	100%
Sum		1.48513×10^{-9}		

3.2.2.2 Non-tolerable patterns with defective bundles and cells.

From the above study, it is shown that the most significant non-tolerable patterns should be those comprising small number of defective cells and bundles. Because the smallest number of defects in the non-tolerable patterns without defective bundles is six as shown in Table 3.3, the search for non-tolerable patterns in the array with defects can be focused on those comprising less than or equal to six defects. Two kinds of significant

patterns in accordance with the above condition were found and are discussed in the following. It is noted that all symbols used in the following discussion are illustrated in Appendix A.

(1) Pattern 1: corresponding to the case where two vertical bundles in the same row are defective.

Figure 3.6 shows this kind of non-tolerable patterns in a phycial array of (N+1)xN. This pattern does not prevent a physical cell from being used but it prevents the construction of a logical array. In the following paragraph, the reason why this pattern can not be tolerated is discussed.

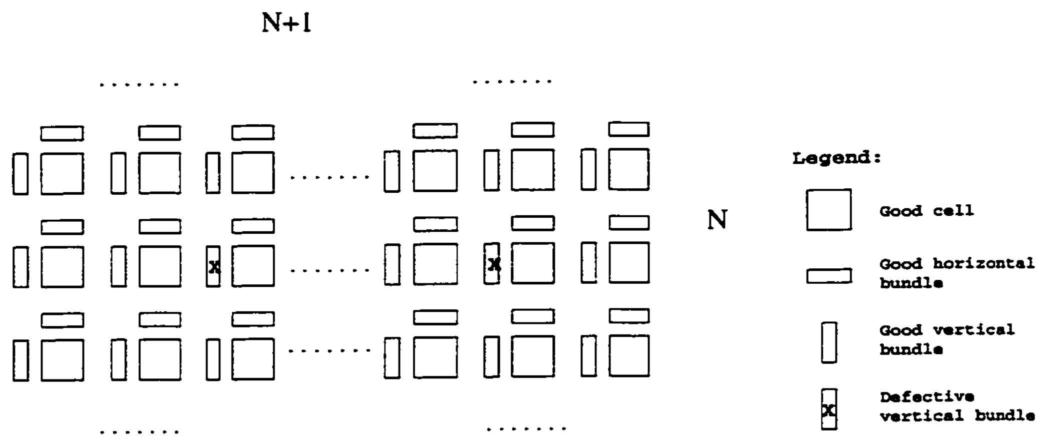


Figure 3.6 Non-tolerable Pattern 1 in a phycial array of (N+1)xN

Without loss of generality, two defective bundles are assumed as a vertical bundle VB(i_1,j,i_1,j) with the status of vertical bundle SVB(i_1,j)=1, and VB(i_2,j,i_2,j) with the status SVB(i_2,j)=1, where $i_1 \neq i_2$. To form a logical array of N by N from a physical array of (N+1) by N, VB(i_1,j,i_1,j) and VB(i_2,j,i_2,j) should be replaced with two good spare bundles. Because each row contains only one spare vertical bundle, one of these two defective vertical bundles must be replaced by a good spare bundle from another row. It is assumed

that $VB(i_2,j,i_2,j)$ is replaced with a good spare vertical bundle in the kth row, $VB(i_3,k,i_3,k)$ with $SVB(i_3,k)=0$. According to the features of the fault-tolerant structure, if this replacement were accomplished, two vertical bundles in the same physical row would be owned by two cells in the logical column that contains the phycial cell $P(i_2,j)$. Without loss of generality, these two cells are the physical cell $P(i_2,k-1)$ mapped with the logical cell $L(i_2,k-1)$ and the physical cell $P(i_2,k)$ mapped with the logical cell $L(i_2,k)$. Then, $P(i_2,k-1)$ owns the vertical bundle $VB(i_2,k,i_2,k-1)$, and $P(i_2,k)$ owns the vertical bundle $VB(i_2-1,k,i_2,k)$. Figure 3.7 illustrates this replacement. Consequently, the vertical receivers of the physical cell $P(i_2,h)$ mapped with $L(i_2,h)$ must accept signals from two cells, $P(i_2,k-1)$ with $L(i_2,k-1)$ and $P(i_2,k)$ with $L(i_2,k)$. Thus, the two vertical receiver multiplexers of the cell $P(i_2,h)$ become $C_R(k-1)_V(i_2,h,i_2,k)$ and $C_R(k)_V(i_2,h,i_2-1,k)$. It shows that this cell needs to communicate with other cells in the same logical column through two vertical bundles in the kth physical row. However, due to the limitation of the number of reconfiguration wires, a cell can only receive signals from vertical bundles located in different physical rows after the reconfiguration. This kind of constraints in the fault-tolerant structure is referred as a rule of not allowed replacements, the receiver source exclusive rule [47], described in Appendix A. Therefore, This kind of configuration is impossible and this kind of patterns cannot be tolerated.

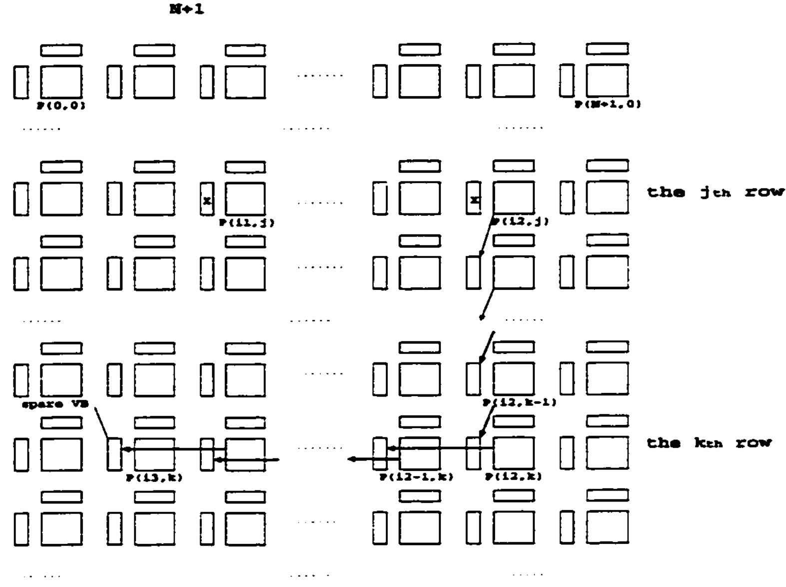


Figure 3.7 Not allowed replacement for two defective vertical bundles.

The analytical expression for the total number of Pattern 1 is presented as follows:

$$Total = NTC_{cell} x NTC_{VB} x NTC_{HB} \tag{3.17}$$

Here,

$$NTC_{cell} = \binom{Q_c}{F_c},\ 0 \le F_c \le S_c \tag{3.18}$$

$$NTC_{VB} = \binom{Q_{VB}}{F_{VB}} - \binom{N_{VB}}{F_{VB}}(N_{VB}+1)^{F_{VB}}, 2 \le F_{VB} \le S_{VB} \tag{3.19}$$

$$NTC_{HB} = \binom{Q_{HB}}{F_{HB}},\ 0 \le F_{HB} \le S_{HB} \tag{3.20}$$

The definitions of the variables in above equations are the same as those in (3.10). Equation (3.18) indicates the number of defective cells in Pattern 1, and it implies that the defective cells of this pattern may be distributed anywhere in the physical array. Equation (3.19) is composed of two terms. The first one gives the number of patterns of F_{VB} defective vertical bundles over a complete array, and the second one is the number of

tolerable patterns of F_{VB} defective vertical bundles distributed over the array. The second term represents the number of patterns where F_{VB} defective bundles are distributed on 2 to S_{VB} rows with only one defective bundles in each row. Thus, $\binom{N_{VB}}{F_{VB}}$ is the number of different selections of F_{VB} rows out of N_{VB} rows since there is at most one defective vertical bundle in any of the N_{VB} rows. The component $(N_{VB}+1)^{F_{VB}}$ represents the number of combination over F_{VB} rows since there are (N_{VB}+1) possible places for a defective vertical bundle. Equation(3.20) shows that the defective horizontal bundles of this pattern can be distributed anywhere of the array.

(2) Pattern 2: corresponding to the case where three cells in a corner and one vertical bundle in the first row are defective.

Figure 3.8 shows a typical example of this kind of non-tolerable patterns. Generally, this patterns prevents a physical cell from being used and a logical array from being constituted. The fact that Pattern 2 cannot be tolerated is analytically proven as follows.

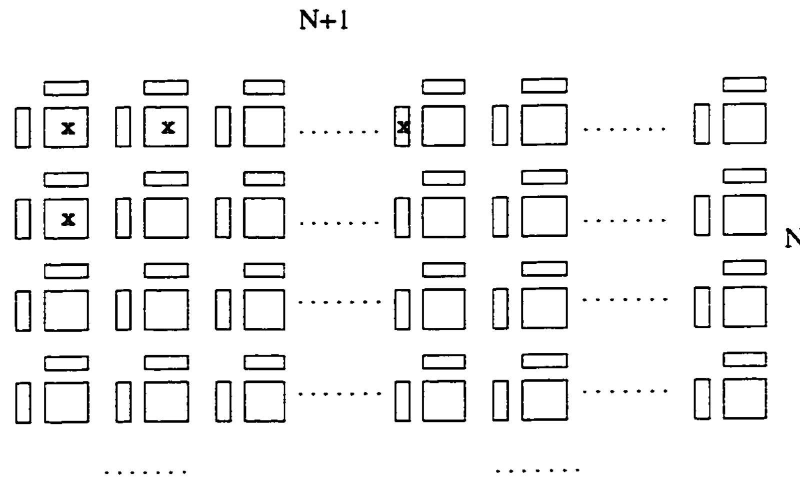


Figure 3.8 Non-tolerable Pattern 2 in a physical array of (N+1) x N

In Figure3.8, vertical bundle VB(0,0,0,0) and horizontal bundle HB(0,0,0,0) cannot be used in the physical array, because three cells P(0,0) and P(1,0) and P(0,1) are defective

simultaneously. There are only two possibilities of forming a logical array of size NxN from a physical array of (N+1)xN. One is that the first column containing two defective cells P(0,0) and P(0,1) is used as a spare column as shown in Figure 3.9. The other is to use the good vertical bundle VB(1,0,1,0) as a spare one to replace the defective vertical bundle VB(i,0,i,0) as shown in Figure 3.10. These two possibilities are discussed as the following. First, for the case one, the first column is treated as a spare column, and one good spare vertical bundle located in a physical row other than the first physical row must be used to replace the defective one. Unfortunately, this kind of construction proves impossible for the reason that has been explained in the analysis of Pattern 1.

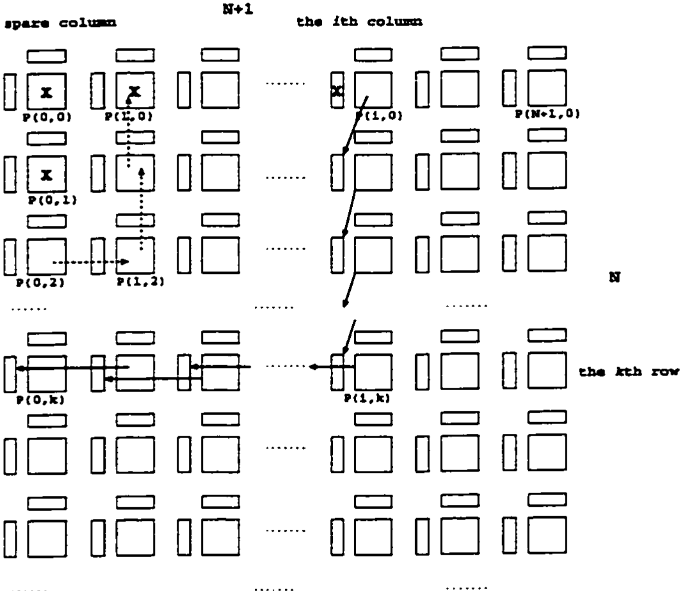


Figure 3.9 The first possibility of forming a logical array of NxN from a physical array of (N+1)xN with the existence of non-tolerable Pattern 2. This case is actually not allowed in the reconfiguration of the fault-tolerant structure. The arrow with virtual line indicates the cell shifting direction, and the arrow with real line indicates which bundle a cell owns after reconfiguration.

Then, for the case two, the first logical column would be built as shown in Figure 3.10. In this configuration, the physical cells P(0,2) and P(1,2) are selected to be in the same

logical column. Because of constraints of the fault-tolerant structure, referred to the receiver connectivity rule [47] presented in Appendix A, P(0,2) and P(1,2) cannot communicate with each other if they use their natural vertical bundles. Thus, either VB(0,2,0,2) should be changed to VB(0,2,1,2) and VB(1,2,1,2) to VB(1,2,0,2). This is illustrated with solid arrows in Figure 3.10. Alternately VB(0,2,0,2) should be changed to VB(0,2,1,2) and VB(0,1,0,1) to VB(0,1,0,2) as illustrated with virtual arrows in Figure 3.10. Evidently, the other cells in this logical column will receive signals from two vertical bundles of the same physical row: either VB(0,2,1,2) and VB(1,2,0,2), or VB(0,1,0,2) and VB(1,1,1,1). Similar to the analysis for Pattern 1, it is impossible and this case will violate the receiver source exclusive rule described in Appendix A. Therefore, Pattern 2 cannot be tolerated in this fault-tolerant structure. It is also shown that Pattern 2 is the non-tolerable pattern comprising the smallest number of defective cells and defective bundles at the same time (the details are presented in Appendix C).

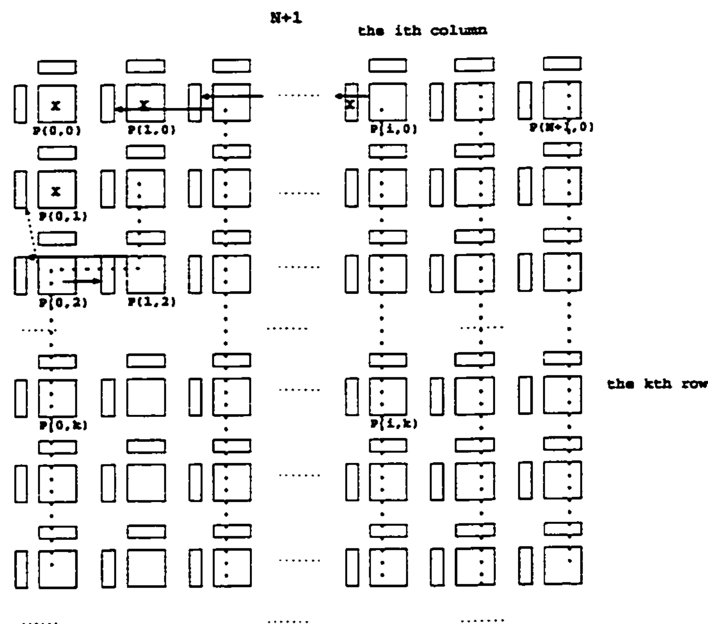


Figure 3.10 The second possibility of forming a NxN logical array out of a (N+1)xN physical array with the presence of non-tolerable Pattern 2. The case is actually not allowed in the reconfiguration of the fault-tolerant structure.

To summarize, Pattern 2 cannot be tolerated in forming a logical array of NxN out of a physical array of (N+1)xN. In addition, it is the one that comprises the smallest number of defective cells and defective bundles simultaneously. Equations (3.21)-(3.23) present the analytical expressions that allow calculating the total number of Pattern 2.

$$NTC_{cell} = \binom{4}{1}\binom{Q_c - 3}{F_c - 3}, \quad 3 \le F_c \le S_c \tag{3.21}$$

$$NTC_{VB} = \binom{N_{VB}}{1}\binom{N_{VB} - 1}{F_{VB} - 1}(N_{VB} + 1)^{F_{VB} - 1}, \ 1 \le F_{VB} \le S_{VB} \tag{3.22}$$

$$NTC_{HB} = \binom{Q_{HB}}{F_{HB}}, \quad 0 \le F_{HB} \le S_{HB} \tag{3.23}$$

In (3.21), $\binom{4}{1}$ indicates that there is a total of 4 different distributions of these three defective cells to any of the 4 corners of the physical array, and $\binom{Q_c - 3}{F_c - 3}$ the number of different distributions of the remaining $(F_c - 3)$ defective cells over the remaining $(Q_c - 3)$ positions in the physical array. Equation (3.22) gives the number of Pattern 2 associated with defective vertical bundles. In this expression, $\binom{N_{VB}}{1}$ is the number of possibilities to select one out of N_{VB} positions in the top row and $\binom{N_{VB} - 1}{F_{VB} - 1}$ the number of possibilities to select (F_{VB}-1) rows out of the remaining (N_{VB}-1) rows for the remaining (F_{VB}-1) vertical bundles such that there is at most one defective vertical bundle in each row. This makes Pattern 1 and Pattern 2 disjoint. The term $(N_{VB} + 1)^{F_{VB} - 1}$ indicates that each row of the total $(F_{VB} - 1)$ rows has (N_{VB}+1) ways to distribute a defective vertical bundle. As for (3.23), $\binom{Q_{HB}}{F_{HB}}$ is the number of different ways to select F_{HB} out of Q_{HB}. It

should be mentioned that the number calculated by Equation(3.21) contains some intersection with combinations of cells in two to four corners. Because these intersections contain very few patterns associated with large number of defects (thus much lower probability of occurrence), they are neglected.

Because Pattern 1 and Pattern 2 comprise the smallest number of defective cells and bundles, the yield losses contributed by these two kinds of defect patterns are the most significant. Their impact on the yield of the structure can be evaluated with (3.15) and (3.17)-(3.23). A numerical analysis has been done using the data presented in Table 3.1 and 3.2. The size of the logical array is 20x20 out of a physical array of 21x20. The first analysis is with data in Table 3.1 and then with data in Table 3.2. Figure 3.11 and 3.12 show the characteristics of the yield loss versus variation of the defect density. It is observed that the yield loss curves reach a maximum and then fall down when the defect density increases. It can be explained as follows. If the defect density is low, an increase of the defect density increases the probability to observe a modest number of defects and the yield losses increase. As the defect density gets large, the distribution shift towards larger defect patterns that exhaust the available number of spares and the yield decreases due to factors other than the non-tolerable patterns. Generally, the yield losses contributed by these two patterns are much smaller.

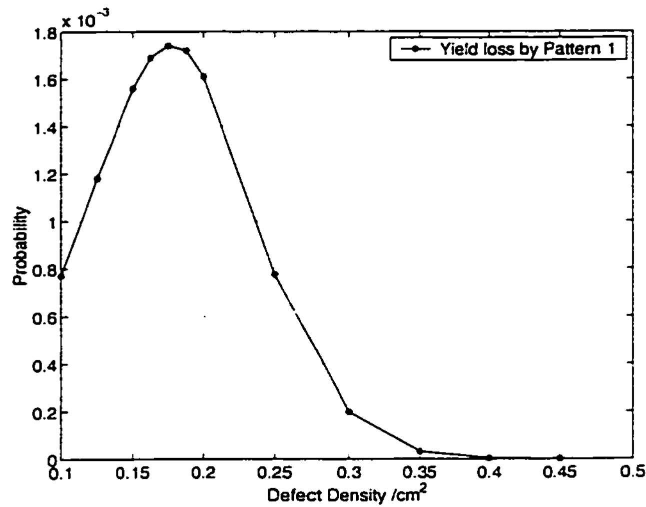


Figure 3.11 Yield loss contributed by the most significant non-tolerated pattern. The relevant data is from Table 3.1.

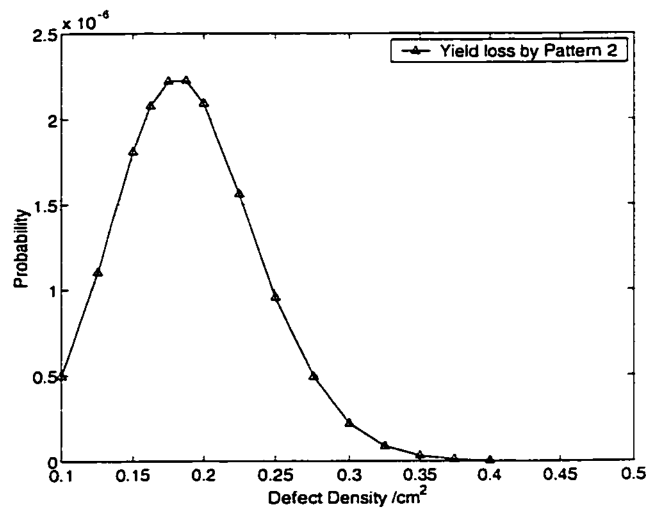


Figure 3.12 Yield loss contributed by the second most significant non-tolerable pattern. The relevant data is from Table 3.1.

With (3.10)-(3.13), the yield of a structure assuming a global redundancy was evaluated, and the results are shown in Figure 3.13. The comparison between the yield losses and yield of the structure assuming global redundancy is shown in Figure 3.14. These figures show that the yield losses contributed by the two most significant defect patterns is small enough to be neglected in practice. Thus, equation (3.9) becomes:

$$Y_{chip} \approx Y_{global} \tag{3.24}$$

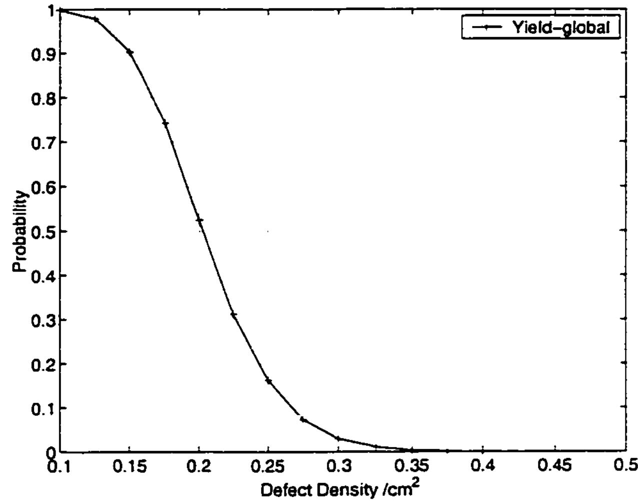


Figure 3.13 Yield of the structure with global redundancy.

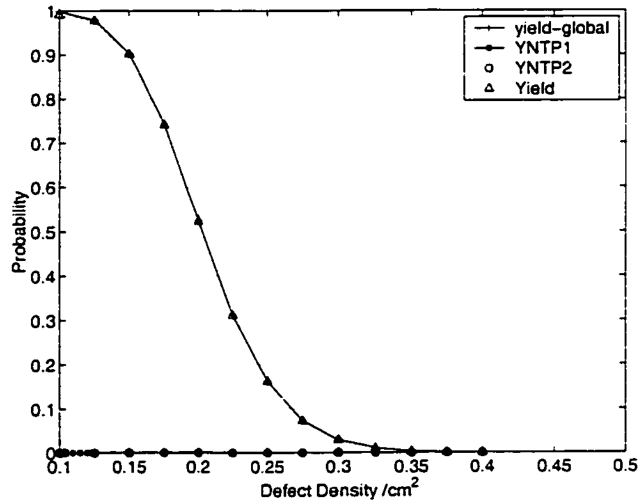


Figure 3.14 Comparison between Y_{loss} and Y_{global}. "YNTP1" represents the yield loss contributed by Pattern 1 and "YNTP2" represents the yield loss by Pattern 2, "Yield" represents for Y_{chip}. The relevant data is from Table 3.1.

When a bundle contains many more wires, the area of a bundle increases and then the yield losses due to bundles also increases. Thus, the yield losses contributed by those two most significant non-tolerable patterns may rise to become significant. In the case of a

WSI architecture described in Table 3.2, a bundle is composed of 40 wires and its area increases to $9.6\text{x}10^{-2}$ cm^2 for a physical array of 20x20. The yield losses increase as shown in Figure 3.15 and Figure 3.16. From Figure 3.15, it is observed that the yield loss contributed by Pattern 1 increases greatly and it becomes significant. Fortunately, in this fault-tolerant structure, the number of defects in the smallest non-tolerable pattern rapidly grows with the addition of one spare row and one spare column in a physical array to form a logical array of NxN. Consequently, those two most significant non-tolerable patterns in the physical array of $(N+1)$xN, Pattern1 and Pattern 2, can be tolerated in a physical array of $(N+1)$x$(N+1)$. Evidently smallest non-tolerable patterns will comprise more defects than 2. It has been shown that the yield losses contributed by non-tolerable patterns that comprise large number of defects are insignificant and can be neglected in the yield evaluation. Therefore, when the area of a bundle increases due to increased bandwidth, in order to obtain an acceptable yield of forming a logical array of NxN, a physical array size with more redundancy is needed. Under this condition, with non-tolerable patterns being under control, the yield model of this structure can also be approximated by the yield formula of the structure assuming global redundancy.

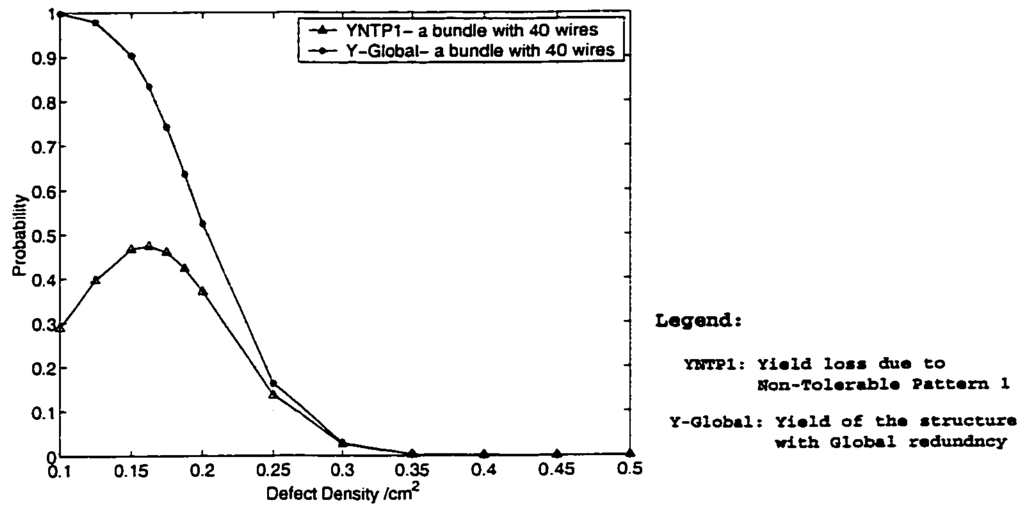


Figure 3.15 Yield loss by the first most significant non-tolerable pattern when a bundle comprises 40 wires. The relevant data is from Table 3.2.

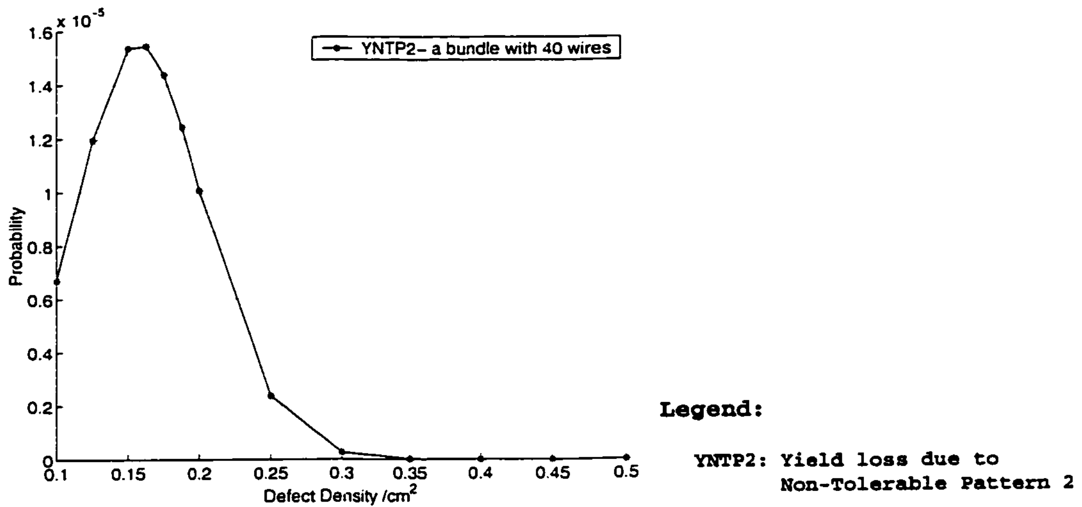


Figure 3.16 Yield loss by the second most significant non-tolerable pattern when a bundle comprises 40 wires. The relevant data is from Table 3.2.

3.3 Defect density impact on forming a logical array

From the previous results, the sensitivity of the yield to variations of the defect density in the fault-tolerant structure can be evaluated with (3.10). Let us consider the problem of

building logical arrays of size 20x20 from physical arrays of 21x20, 21x21 and 22x22. Figure 3.16 shows the yield of arrays of various sizes.

It is observed in Figure 3.17 that the yield curves shift right when the fraction of the array used as spares increases. It is also clear from these results that, for a given fraction of redundancy, below some defect density threshold, the array is very robust to variations of the defect density, however, beyond that threshold, the array yield degrades rapidly.

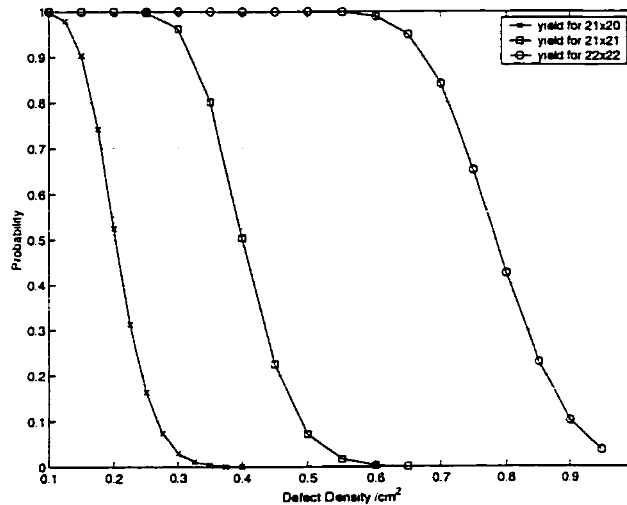


Figure 3.17 Yield of forming a logical array of 20x20 from physical arrays of 21x20, 21x21, and 22x22.

3.4 Yield model regression

In order to have a quick evaluation of the yield of large arrays, a simple regression model is developed. It can be used to predict the defect density threshold where the yield of a large array degrades.

The yield was computed with the expressions presented earlier for arrays of various size and redundancy ratio. It was found that, for arrays of different sizes but equivalent

redundancy ratio, the yield curves tend to cross around the point where the probability is equal to $1 - e^{-1}$ as shown in Figure 3.18.

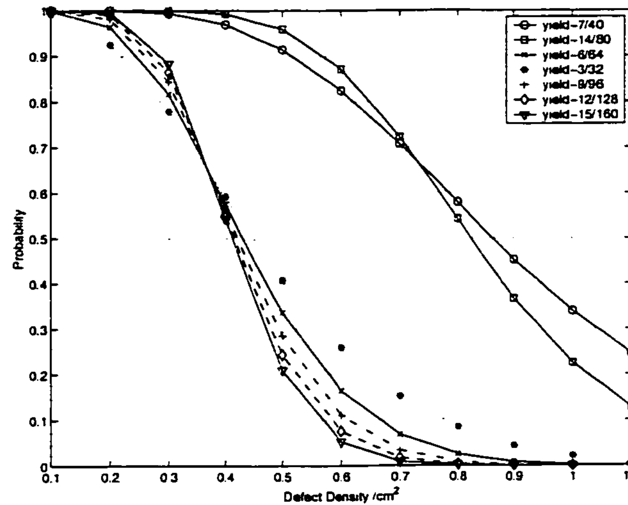


Figure 3.18 Cross points for arrays of different sizes with equivalent redundancy ratio. 7/40 for a physical array with 40 cells including 7 spares, 6/64 array for one with 64 cells including 6 spare.The other arrays of different sizes have the same redundancy ratio as 7/40 and 6/64 respectively.

Table 3.4 Numerical value of the pivot points of physical arrays of different sizes with redundancy ratio equal to 0.1

Size of Array	Number of Spares	$D_{pivot}(cm^{-1})$	Yield
30	3	0.40550453	$1-e^{-1}$
40	4	0.40494685	$1-e^{-1}$
50	5	0.40479842	$1-e^{-1}$
60	6	0.40465372	$1-e^{-1}$
70	7	0.40447338	$1-e^{-1}$
100	10	0.40394883	$1-e^{-1}$
430	43	0.40650498	$1-e^{-1}$
600	60	0.40793823	$1-e^{-1}$
700	70	0.40861149	$1-e^{-1}$

The numerical results of the points where the probability is equal $1-e^{-1}$ are presented in Table 3.4. These results show that the numerical values of the defect density of different arrays are very close at the point where the probability is equal to $1-e^{-1}$. As an approximation, the point can be thought as a pivot point.

By the method of least square in numerical mathematics [10], a regression model is developed to predict this pivot point and the slope of the yield curve in that region. The details of the derivation are presented in Appendix D. These parameters would be useful to assess the suitability of a fault tolerant array design as a function of array size, expected defect density and redundancy ratio. The defect density, *D(r)*, where the probability is equal to $1-e^{-1}$, and the slope at the pivot point, *S(r,m)*, can be approximated by:

$$D(r) = -0.0208 + 4.3111r \tag{3.25}$$

$$S(r, m) = 0.3166r^{-0.8} + (0.0130 - 0.0337r)m \tag{3.26}$$

Where r is the redundancy ratio of the physical array of K by L, and m is the number of cells in the physical array, m=KxL. S(r,m) is an absolute value in (3.26).

Figure 3.19 compares the yields predicted by the regression models with those computed with the complete model (3.10). It is observed that there is a good agreement between the results computed with these two models. Thus, this regression model can be used for quick yield prediction as part of a design flow. In particular, it can help identify arrays likely to produce poor yield or those that are excessively sensitive to defect density variations.

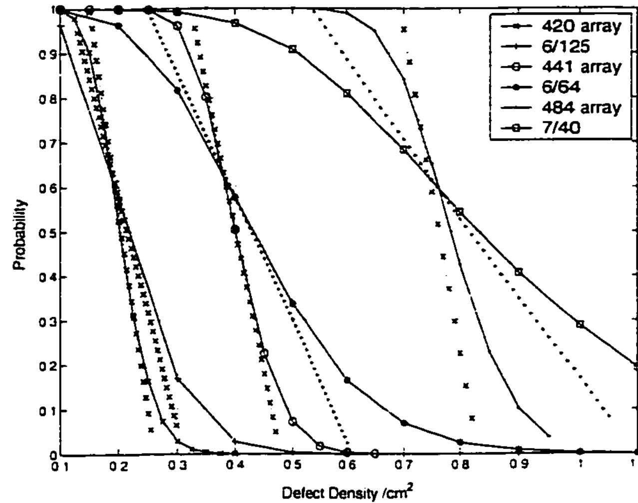


Figure 3.19 Comparison of the regression model and the complete yield model. 420 array stands for a physical array of 21x20, 441 array for one of 21x21, 484 array for one of 22x22, 6/125 for one with 125 cells including 6 spares, 6/64 array for one with 64 cells including 6 spares, and 7/40 for one with 40 cells including 7 spares. The solid lines are obtained from the complete yield model and the dotted lines from the regression model

3.5 Summary

In this chapter, a method of developing a closed form yield model taking into account constraints of a fault-tolerant architecture has been presented. The impact of such constraints on the yield is evaluated by computing the probability of observing non-tolerable defect patterns and by subtracting these probabilities from yield of the architecture with global redundancy.

Non-tolerable patterns can be found by a detailed analysis of a fault-tolerant structure. It is shown that most of the yield losses come from a few patterns comprising small number of defects. It becomes clear that many complex patterns with large number of defects cannot be tolerated, but the yield losses due to patterns comprising large number of defects decreases very rapidly with the increase of the number of defects, and they can

become insignificant. Thus, even though finding all non-tolerable patterns is intractable, we only need to find the set of small defect patterns that cannot be tolerated. Neglecting the yield losses due to large patterns leads to overestimating the yield, but in practice, the error is quite small. Approximately, the yield of the fault-tolerant architecture can be approximated by the yield of the structure with global redundancy.

In this chapter, using the yield model of the structure assuming global redundancy, the sensitivity of the yield to variations of the defect density in a fault-tolerant architecture has been investigated. The analyzed array is fairly robust because the yield loss is never found to be very significant in the region of interest where replaceable modules have a high enough individual yield. A relatively sharp threshold in the yield versus defect density relationship has been observed. When the level of redundancy is not suitably adjusted, the yield rapidly degrades.

A regression yield model is also proposed in this chapter. Using a simple regression analysis, a simplified yield model can accurately predict the slope and the pivot point of true yield curves. These parameters, which act as a function of array size, expected defect density and redundancy ratio, are useful to assess the suitability of the design of a fault-tolerant array. With the regression yield models, it can be predicted when more redundancy is needed for given defect density, and array and cell sizes.

Chapter 4
Analysis of the effects of clustered defects on yield

4.1 Introduction to yield models when defects are clustered

Using a Poisson model may lead to a underestimation of the yield because defects tend to cluster while the Poisson distribution assumes not clustering [35]-[38]. Defects clustering make it possible for certain areas of a wafer to have fewer defects than expected with a random distribution. Figure 4.1 shows how defects clustering can increase the yield. In this case, two wafers have the same number of defects, but the wafer at the bottom has a higher yield because of the defects being clustered. This example illustrates clustered defects may lead to a higher yield. To account for this phenomenon, other statistical models must be applied to develop yield models. As presented in chapter 3, the negative binomial distribution is commonly used to take into account clustered defects. When modeling the yield for a chip without redundancy, the negative binomial model derived from this statistical distribution can be used to predict the yield. However, for a chip with redundancy, some non-trivial combinatorial statistical models need to be employed to develop yield models taking clustered defects into consideration. Several approaches taking clustered defect distributions into account have been proposed [18][19][20][38][45]. The way of dealing with the correlation of defect locations is crucial in modeling the yield for a fault-tolerant structure.

	x x		x	x
		x		x

(i)Non-clustered defects, Y=0.5

		x x	x	
		x x x		

(ii)Clustered defects, Y=0.7

Figure 4.1 Effect of clustered defects on a conventional chip yield (from [17]).

One approach deriving yield models with clustered defect distributions is based on two combinatorial statistics, *Maxwell-Boltzman* and *Bose-Einstein* combinatorial statistics. For a circuit with only one kind of sub-circuits, called modules, the yield of the circuit can be expressed as follows:

$$Y_{circuit} = \sum_{m} Q(m)E(n, m) \tag{4.1}$$

Here, n is the number of total modules in the circuit, $Q(m)$ is the number of different selections of m modules out of n such that these m modules are defective but the circuit is still functional, and $E(n,m)$ is the probability of the event where only and exactly these m modules have defects. Because defects are clustered, each defective module may have more than one defect. Thus, $E(n,m)$ can be written as the following:

$$E(n, m) = \sum_{x=0}^{\infty} P\{x\}P_{xm} \tag{4.2}$$

where P{x} is the probability of having x defects in the circuit, and P_{xm} is the probability that these x defects are distributed over m modules in such way that each module has at least one defect. According to the negative Binomial distribution described in Chapter 3, P{x} is given as follows.

$$P\{x\} = \frac{\Gamma(x+\alpha)}{x!\Gamma(\alpha)} \frac{(\bar{\lambda}/\alpha)^x}{(1+\bar{\lambda}/\alpha)^{\alpha+x}} \tag{4.3}$$

where α is a clustering parameter, $\bar{\lambda}$ is the average number of defects in the circuit, x is the number of defects in the circuit, $\Gamma(x)$ is the Gamma function.

To derive the expression of P_{xm}, two assumptions about the defects were made. The first is that the defects are distinguishable. With *Maxwell-Boltzman* combinatorial statistics, P_{xm} is given in (4.4). The details of the derivation is presented in Appendix E.

$$P_{xm} = \frac{\left[\sum_{k=0}^{m} \binom{m}{k} (-1)^k (m-k)^x\right]}{n^x} \qquad x \geq m \tag{4.4}$$

In the second assumption, defects are considered undistinguishable. In this case, P_{xm} can be derived with *Bose-Einstein* combinatorial statistics. A detailed derivation is also found in Appendix E. The expression for P_{xm} with *Bose-Einstein* statistics is,

$$P_{xm} = \frac{\binom{x-1}{m-1}}{\binom{x+n-1}{x}} \qquad x \geq m \tag{4.5}$$

When the circuit uses global redundancy, $Q(m) = \binom{n}{m}$ and (4.1) is rewritten as follows:

$$Y_{circuit} = \sum_{m} \binom{n}{m} \sum_{x=0}^{\infty} P\{x\} P_{xm} \tag{4.6}$$

In (4.6), as the defects are assumed to be independent of each other, *Maxwell-Boltzman* combinatorial statistics is used. By contrast, as the defects are undistinguishable and these defects can be clustered in a module, *Bose-Einstein* combinatorial statistics is used. It implies that the defects are dependant. Generally, any of these two kinds of combinatorial statistics is used to infer a yield model, taking a form of clustered defects into account.

4.2 Yield modeling for the architecture assuming clustered defects

In this section, a yield model of the complex architecture presented in Chapter 2 is developed and clustered defects are taken into account. As described in Chapter 3, in a physical array based on this architecture, only three kinds of main sub-circuits, cells, vertical bundles and horizontal bundles, need to be taken into consideration in the yield analysis. To study the effects of clustered defects on the yield of this structure, two assumptions are made in developing different yield models. First, it is assumed that the defects in identical sub-circuits are statistically dependent, but those in different sub-circuits are independent. In the second case, it is assumed that the defects in all sub-circuits are statistically dependent.

4.2.1 Yield modeling with identical sub-circuits assumed statistically dependent

When defects in the three kinds of different sub-circuits, cells, vertical bundles and horizontal bundles, are statistically independent, the yield of the fault-tolerant structure assuming global redundancy is given as:

$$Y_{global} = Y_{cell} Y_{VB} Y_{HB} \tag{4.7}$$

Meanwhile, to consider the effect of clustered defects, it is assumed that the identical sub-circuits are statistically dependent. In other word, defects in cells are dependent of each other, those in vertical bundles are dependent, and those in horizontal bundles are dependent. The yield models of the cells, the vertical bundles, and the horizontal bundles are respectively expressed as follows:

$$Y_{cell} = \sum_{F_c=0}^{S_c} \binom{Q_c}{F_c} \sum_{x=0}^{\infty} P\{x\} P_{xF_c} \tag{4.8}$$

$$Y_{VB} = \sum_{F_{VB}=0}^{S_{VB}} \binom{Q_{VB}}{F_{VB}} \sum_{y=0}^{\infty} P\{y\} P_{yF_{VB}} \tag{4.9}$$

$$Y_{HB} = \sum_{F_{HB}=0}^{S_{HB}} \binom{Q_{HB}}{F_{HB}} \sum_{z=0}^{\infty} P\{z\} P_{zF_{HB}} \tag{4.10}$$

In (4.8), the binomial coefficient $\binom{Q_c}{F_c}$ gives the number of different distributions of the defects in F_c cells out of Q_c cells with the assumption that all these defective cells can be tolerated by spare cells. P{x} is the probability of having x defects in cells and P_{xF_c} is the probability of having all x defects distributed over F_c cells such that each cell has at least one defect. The same conditions and assumptions of the defect distributions are applied to (4.9) and (4.10), except for the different subscripts that refer to vertical or horizontal bundles instead of cells. In (4.8), (4.9) and (4.10), x, y and z are the number of defects in cells, vertical bundles and horizontal bundles, respectively.

By substituting (4.8)-(4.10) into (4.7), the equation can be written as follows:

$$Y_{global} = \sum_{F_c=0}^{S_c} \sum_{F_{VB}=0}^{S_{VB}} \sum_{F_{HB}=0}^{S_{HB}} \binom{Q_c}{F_c}\binom{Q_{VB}}{F_{VB}}\binom{Q_{HB}}{F_{HB}} \sum_{x=0}^{\infty} P\{x\} P_{xF_c} \sum_{y=0}^{\infty} P\{y\} P_{yF_{VB}} \sum_{z=0}^{\infty} P\{z\} P_{zF_{HB}} \tag{4.11}$$

When defects are distributed according to the negative binomial distribution, P{x}, P{y}, and P{z} can be expressed by (4.3). With a procedure similar to that used in (4.4) and (4.5), the probabilities P_{xF_c}, $P_{yF_{VB}}$ and $P_{zF_{HB}}$ can be derived. Depending on the assumption of distinguishable or undistinguishable defects, two different yield expressions can be obtained.

(1) Yield models with the assumption of distinguishable defects.

When defects are distinguishable, the yield expression is derived by using *Maxwell-Boltzman* combinatorial statistics. Without loss of generality, the procedure to derive P_{xF_c}, the part associated with cells in (4.11), is presented as the following.

Using the subscript "F_c" instead of "m" of (4.4), P_{xF_c} is given in (4.12).

$$P_{xF_c} = \frac{\left[\sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k (F_c - k)^x\right]}{Q_c^x}, \ x \geq F_c \tag{4.12}$$

let $P_{xF_c} = 0$ if $x < F_c$. Then, it is given,

$$\sum_{x=0}^{\infty} P\{x\} P_{xF_c} = \sum_{x=0}^{\infty} P\{x\} \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \left(\frac{F_c - k}{Q_c}\right)^x \tag{4.13}$$

For the generalized negative Binomial distribution P{x}, similar to [17][46], (4.13) can becomes (the detail derivation is presented in Appendix E)

$$\sum_{x=0}^{\infty} P\{x\} P_{xF_c} = \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \left(1 + \frac{(Q_c - F_c + k)\bar{\lambda}_c}{\alpha}\right)^{-\alpha} \tag{4.14}$$

Therefore, (4.8) can be written as (4.15).

$$Y_{cell} = \sum_{F_c = 0}^{S_c} \binom{Q_c}{F_c} \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \left(1 + \frac{(Q_c - F_c + k)\bar{\lambda}_c}{\alpha}\right)^{-\alpha} \tag{4.15}$$

Using the same method, Y_{HB} and Y_{VB} can be presented as follows:

$$Y_{HB} = \sum_{F_{HB} = 0}^{S_{HB}} \binom{Q_{HB}}{F_{HB}} \sum_{j=0}^{F_{HB}} \binom{F_{HB}}{j} (-1)^j \left(1 + \frac{(Q_{HB} - F_{HB} + j)\bar{\lambda}_{HB}}{\alpha}\right)^{-\alpha} \tag{4.16}$$

$$Y_{VB} = \sum_{F_{VB} = 0}^{S_{VB}} \binom{Q_{HB}}{F_{VB}} \sum_{i=0}^{F_{VB}} \binom{F_{VB}}{i} (-1)^i \left(1 + \frac{(Q_{VB} - F_{VB} + i)\bar{\lambda}_{VB}}{\alpha}\right)^{-\alpha} \tag{4.17}$$

where $\bar{\lambda}_C$, $\bar{\lambda}_{VB}$ and $\bar{\lambda}_{HB}$ are the average number of defects in a cell, a vertical bundle, and a horizontal bundle, respectively. It is assumed that, α, the clustering parameter of these three kinds of sub-circuits is identical.

Substituting the respective terms into (4.11) with (4.15), (4.16), and (4.17), the yield of the structure assuming global redundancy can be expressed as follows:

$$Y_{global} = \sum_{F_c = 0}^{S_c} \sum_{F_{VB} = 0}^{S_{VB}} \sum_{F_{HB} = 0}^{S_{HB}} \binom{Q_c}{F_c} \binom{Q_{VB}}{F_{VB}} \binom{Q_{HB}}{F_{HB}} \sum_{k=0}^{F_c} \sum_{j=0}^{F_{VB}} \sum_{i=0}^{F_{HB}} \binom{F_c}{k} \binom{F_{HB}}{j} \binom{F_{VB}}{i} (-1)^{i+j+k}$$

$$\left(1 + \frac{(Q_c - F_c + k)\bar{\lambda}_c}{\alpha}\right)^{-\alpha} \left(1 + \frac{(Q_{HB} - F_{HB} + j)\bar{\lambda}_{HB}}{\alpha}\right)^{-\alpha} \left(1 + \frac{(Q_{VB} - F_{VB} + i)\bar{\lambda}_{VB}}{\alpha}\right)^{-\alpha} \tag{4.18}$$

According to the study presented in Chapter 3, the equation for evaluating the yield loss contributed by non-tolerable patterns can be expressed as follows:

$$(Y_{NTP})_i = \sum_{F_c = 0}^{S_c} \sum_{F_{VB} = 0}^{S_{VB}} \sum_{F_{HB} = 0}^{S_{HB}} (NTC_{HB})(NTC_{VB})(NTC_{cell}) \sum_{k=0}^{F_c} \sum_{j=0}^{F_{VB}} \sum_{i=0}^{F_{HB}} \binom{F_c}{k} \binom{F_{HB}}{j} \binom{F_{VB}}{i} (-1)^{i+j+k}$$

$$\left(1 + \frac{(Q_c - F_c + k)\bar{\lambda}_c}{\alpha}\right)^{-\alpha} \left(1 + \frac{(Q_{HB} - F_{HB} + j)\bar{\lambda}_{HB}}{\alpha}\right)^{-\alpha} \left(1 + \frac{(Q_{VB} - F_{VB} + i)\bar{\lambda}_{VB}}{\alpha}\right)^{-\alpha} \tag{4.19}$$

(2) Yield models with the assumption of undistinguishable defects

In this case, it is assumed that the defects are undistinguishable. To model the yield of the architecture, *Bose-Einstein* combinatorial statistics is used. With (4.5), we have,

$$P_{xF_c} = \frac{\binom{x-1}{F_c-1}}{\binom{x+Q_c-1}{x}}, \quad x \geq F_c$$

$$P_{yF_{VB}} = \frac{\binom{y-1}{F_{VB}-1}}{\binom{y+Q_{VB}-1}{y}}, \quad y \geq F_{VB}$$

$$P_{zF_{HB}} = \frac{\binom{z-1}{F_{HB}-1}}{\binom{z+Q_{HB}-1}{z}}, \quad z \geq F_{HB}$$

Substituting above three equations and the negative Binomial distribution into equations (4.8)-(4.10) respectively, the yield of the fault-tolerant structure assuming global redundancy can be rewritten as follows:

$$Y_{cell} = \sum_{F_c=0}^{S_c} \binom{Q_c}{F_c} \sum_{x=F_c}^{\infty} \frac{\Gamma(x+\alpha)}{x!\Gamma(\alpha)} \frac{(Q_c\bar{\lambda}_c/\alpha)^x}{(1+Q_c\bar{\lambda}_c/\alpha)^{\alpha+x}} \frac{\binom{x-1}{F_c-1}}{\binom{x+Q_c-1}{x}} \tag{4.20}$$

$$Y_{VB} = \sum_{F_{VB}=0}^{S_{VB}} \binom{Q_{VB}}{F_{VB}} \sum_{y=F_{VB}}^{\infty} \frac{\Gamma(y+\alpha)}{y!\Gamma(\alpha)} \frac{(Q_{VB}\bar{\lambda}_{VB}/\alpha)^y}{(1+Q_{VB}\bar{\lambda}_{VB}/\alpha)^{\alpha+y}} \frac{\binom{y-1}{F_{VB}-1}}{\binom{y+Q_{VB}-1}{y}} \tag{4.21}$$

$$Y_{HB} = \sum_{F_{HB}=0}^{S_{HB}} \binom{Q_{HB}}{F_{HB}} \sum_{z=F_{HB}}^{\infty} \frac{\Gamma(z+\alpha)}{z!\Gamma(\alpha)} \frac{(Q_{HB}\bar{\lambda}_{HB}/\alpha)^z}{(1+Q_{HB}\bar{\lambda}_{HB}/\alpha)^{\alpha+z}} \frac{\binom{z-1}{F_{HB}-1}}{\binom{z+Q_{HB}-1}{z}} \tag{4.22}$$

In (4.20), if $x-1 = F_c - 1$, $\binom{x-1}{F_c-1} = 1$. If $x < F_c$, $\binom{x-1}{F_c-1} = 0$. These conditions for (4.20) are applied to (4.21) and (4.22), with the subscripts "y" or "z" instead of "x" and with the subscripts "VB" or "HB" instead of "c".

Substituting (4.20), (4.21), and (4.22) into (4.7), the yield equation of the fault- tolerant structure is presented in (4.23).

$$Y_{global} = \sum_{F_c=0}^{S_c} \sum_{F_{VB}=0}^{S_{VB}} \sum_{F_{HB}=0}^{S_{HB}} \binom{Q_c}{F_c}\binom{Q_{VB}}{F_{VB}}\binom{Q_{HB}}{F_{HB}} \sum_{x=F_c}^{\infty} \sum_{y=F_{VB}}^{\infty} \sum_{z=F_{HB}}^{\infty} \frac{\Gamma(x+\alpha)}{x!\Gamma(\alpha)} \frac{(Q_c\bar{\lambda}_c/\alpha)^x}{(1+Q_c(\bar{\lambda}_c/\alpha))^{\alpha+x}} \frac{\Gamma(y+\alpha)}{y!\Gamma(\alpha)} \frac{(Q_{VB}\bar{\lambda}_{VB}/\alpha)^y}{(1+Q_{VB}\bar{\lambda}_{VB}/\alpha)^{\alpha+y}} \frac{\Gamma(z+\alpha)}{z!\Gamma(\alpha)} \frac{(Q_{HB}\bar{\lambda}_{HB}/\alpha)^z}{(1+Q_{HB}\bar{\lambda}_{HB}/\alpha)^{\alpha+z}} \frac{\binom{x-1}{F_c-1}}{\binom{x+Q_c-1}{x}} \frac{\binom{y-1}{F_{VB}-1}}{\binom{y+Q_{VB}-1}{y}} \frac{\binom{z-1}{F_{HB}-1}}{\binom{z+Q_{HB}-1}{z}} \qquad (4.23)$$

Based on (4.23), the equation for evaluating the yield loss due to non-tolerable patterns can be expressed as follows:

$$(Y_{NTP})_i = \sum_{F_c=0}^{S_c} \sum_{F_{VB}=0}^{S_{VB}} \sum_{F_{HB}=0}^{S_{HB}} (NTC_{HB})(NTC_{VB})(NTC_{cell}) \sum_{x=F_c}^{\infty} \sum_{y=F_{VB}}^{\infty} \sum_{z=F_{HB}}^{\infty} \frac{\Gamma(x+\alpha)}{x!\Gamma(\alpha)} \frac{(Q_c\bar{\lambda}_c/\alpha)^x}{(1+Q_c\bar{\lambda}_c/\alpha)^{\alpha+x}} \frac{\Gamma(y+\alpha)}{y!\Gamma(\alpha)} \frac{(Q_{VB}\bar{\lambda}_{VB}/\alpha)^y}{(1+Q_{VB}\bar{\lambda}_{VB}/\alpha)^{\alpha+y}} \frac{\Gamma(z+\alpha)}{z!\Gamma(\alpha)} \frac{(Q_{HB}\bar{\lambda}_{HB}/\alpha)^z}{(1+Q_{HB}\bar{\lambda}_{HB}/\alpha)^{\alpha+z}} \frac{\binom{x-1}{F_c-1}}{\binom{x+Q_c-1}{x}} \frac{\binom{y-1}{F_{VB}-1}}{\binom{y+Q_{VB}-1}{y}} \frac{\binom{z-1}{F_{HB}-1}}{\binom{z+Q_{HB}-1}{z}} \qquad (4.24)$$

Equation (4.18) and (4.23) present two kinds of yield models with the assumption that defects are partially clustered in the structure, i.e., the defects in identical sub-circuits comply with a clustered distribution but those in different sub-circuits with a random distribution. With (4.19) and (4.24), the impact of partial clustered defects on the yield loss can also be evaluated.

4.2.2 Yield modeling with all sub-circuits assumed statistically dependent

In this sub-section, it is assumed that the defects in all sub-circuits are statistically dependent of each other. The defects are distributed over the fault-tolerant structure

described in chapter 2 according to the negative binomial distribution. The yield formula of the structure assuming global redundancy is as follows:

$$Y_{global} = \sum_{x=0}^{\infty} P\{x\} P_{tx} \tag{4.25}$$

where, P{x} is the probability that x defects are distributed in the structure, and P_{tx} is the probability that those x defects can be tolerated.

According to the above assumption, P{x} is expressed with the negative binomial distribution (4.3). To obtain P_{tx}, it is of prime importance to identify what defective parts can be tolerated in this fault-tolerant structure. Fortunately, when the structure provides global redundancy, all defects can be tolerated if the numbers of defective cells, defective vertical bundles, and defective horizontal bundles are not larger than the number of respective spares. Because the function of all sub-circuits are assumed to have the same sensitivity to defects, each sub-circuit is considered to be composed of a certain number of equivalent-area elements, called EEs[44], according to their effective areas. In fact, these EEs have no other functions than helping to formulate the yield expression. Denote by n_c, the number of EEs in each cell, n_{VB}, that in each vertical bundle, and n_{HB}, that in each horizontal bundle. The structure is considered to be composed of z EEs, $z = Q_c \times n_c + Q_{VB} \times n_{VB} + Q_{HB} \times n_{HB}$. Then, P_{tx} can be expressed as follows:

$$P_{tx} = \frac{C_x}{D_x} \tag{4.26}$$

Here, C_x is the number of the different distribution of x defects over EEs such that these x defects can be tolerated, and D_x is the total number of different distribution x defects over the structure.

If the number of the defects is less than or equal to the smallest number among the number of spare cells, spare vertical bundles, and spare horizontal bundles, namely $x \le \min(S_C, S_{VB}, S_{HB})$, it is evident that $P_{tx}=1$. If $S_C=\min(S_C, S_{VB}, S_{HB})$, and the number of defects is greater than S_C, only when the number of the defective cells and defective bundles caused by these defects is not larger than the number of respective spares, the defects can be tolerated. Therefore, (4.25) is rewritten as follows:

$$Y_{global} = \sum_{x=0}^{S_c} P\{x\} + \sum_{x=S_c+1}^{\infty} P\{x\}\frac{C_x}{D_x} \tag{4.27}$$

where

$$C_x = \sum_{F_c=1}^{S_c} \binom{Q_c}{F_c} \sum_{i_1=1}^{n_c} \cdots \sum_{i_{F_C}=1}^{n_c} G_{xy_1} \prod_{m=1}^{F_c} \binom{n_c}{i_m} + \tag{4.28}$$

$$\sum_{F_{VB}=1}^{S_{VB}} \binom{Q_{VB}}{F_{VB}} \sum_{j_1=1}^{n_{VB}} \cdots \sum_{j_{F_{VB}}=1}^{n_{VB}} G_{xy_2} \prod_{t=1}^{F_{VB}} \binom{n_{VB}}{j_t} + \tag{4.29}$$

$$\sum_{F_{HB}=1}^{S_{HB}} \binom{Q_{HB}}{F_{HB}} \sum_{k_1=1}^{n_{HB}} \cdots \sum_{k_{F_{HB}}=1}^{n_{HB}} G_{xy_3} \prod_{p=1}^{F_{HB}} \binom{n_{HB}}{k_p} + \tag{4.30}$$

$$\sum_{F_c=1}^{S_c} \sum_{F_{VB}=1}^{S_{VB}} \binom{Q_c}{F_c}\binom{Q_{VB}}{F_{VB}} \sum_{i_1=1}^{n_c} \cdots \sum_{i_{F_C}=1}^{n_c} \sum_{j_1=1}^{n_{VB}} \cdots \sum_{j_{F_{VB}}=1}^{n_{VB}} G_{xy_4} \prod_{m=1}^{F_c} \binom{n_c}{i_m} \prod_{t=1}^{F_{VB}} \binom{n_{VB}}{j_t} + \tag{4.31}$$

$$\sum_{F_c=1}^{S_c} \sum_{F_{HB}=1}^{S_{HB}} \binom{Q_c}{F_c}\binom{Q_{HB}}{F_{HB}} \sum_{i_1=1}^{n_c} \cdots \sum_{i_{F_C}=1}^{n_c} \sum_{k_1=1}^{n_{HB}} \cdots \sum_{k_{F_{HB}}=1}^{n_{HB}} G_{xy_5} \prod_{m=1}^{F_c} \binom{n_c}{i_m} \prod_{p=1}^{F_{HB}} \binom{n_{HB}}{k_p} + \tag{4.32}$$

$$\sum_{F_{VB}=1}^{S_{VB}} \sum_{F_{HB}=1}^{S_{HB}} \binom{Q_{VB}}{F_{VB}}\binom{Q_{HB}}{F_{HB}} \sum_{j_1=1}^{n_{VB}} \cdots \sum_{j_{F_{VB}}=1}^{n_{VB}} \sum_{k_1=1}^{n_{HB}} \cdots \sum_{k_{F_{HB}}=1}^{n_{HB}} G_{xy_6} \prod_{t=1}^{F_{VB}} \binom{n_{VB}}{j_t} \prod_{p=1}^{F_{HB}} \binom{n_{HB}}{k_p} + \tag{4.33}$$

$$\sum_{F_c=1}^{S_c} \sum_{F_{VB}=1}^{S_{VB}} \sum_{F_{HB}=1}^{S_{HB}} \binom{Q_c}{F_c}\binom{Q_{VB}}{F_{VB}}\binom{Q_{HB}}{F_{HB}} \sum_{i_1=1}^{n_c} \cdots \sum_{i_{F_C}=1}^{n_c} \sum_{j_1=1}^{n_{VB}} \cdots \sum_{j_{F_{VB}}=1}^{n_{VB}} \sum_{k_1=1}^{n_{HB}} \cdots \sum_{k_{F_{HB}}=1}^{n_{HB}} G_{xy_7} \prod_{m=1}^{F_c} \binom{n_c}{i_m} \prod_{t=1}^{F_{VB}} \binom{n_{VB}}{j_t} \prod_{p=1}^{F_{HB}} \binom{n_{HB}}{k_p} \tag{4.34}$$

Here, $G_{xy_i} = 0$ if $x < y_i$. $y_1 = \sum_{m=1}^{F_c} i_m$, $y_2 = \sum_{t=1}^{F_{VB}} j_t$, $y_3 = \sum_{p=1}^{F_{HB}} k_p$, $y_4 = \sum_{m=1}^{F_c} i_m + \sum_{t=1}^{F_{VB}} j_t$,

$y_5 = \sum_{m=1}^{F_c} i_m + \sum_{p=1}^{F_{HB}} k_p$, $y_6 = \sum_{t=1}^{F_{VB}} j_t + \sum_{p=1}^{F_{HB}} k_p$, $y_7 = \sum_{m=1}^{F_c} i_m + \sum_{t=1}^{F_{VB}} j_t + \sum_{p=1}^{F_{HB}} k_p$.

The symbols used in the above equations are defined as the following:

G_{xy_i}: the probability that all x defects are distributed over y_i EEs so that each of these y_i EEs has at least one defect

$y_i(i=1,2,..,7)$: the total number of defective EEs in the ith term;

i_m: the number of the defective EEs in the cells;

j_t: the number of the defective EEs in the vertical bundles;

k_p: the number of the defective EEs in the horizontal bundles;

n_c: the total number of EEs in a cell;

n_{VB}: the total number of EEs in a vertical bundle;

n_{HB}: the total number of EEs in a horizontal bundle;

When the defects are distinguishable, using *Maxwell-Boltzman* combinatorial statistics, G_{xy_i} and D_x are given by,

$$G_{xy_i} = \sum_{k=0}^{y_i} (-1)^k \binom{y_i}{k} (y_i - k)^x, \; x \geq y_i \tag{4.35}$$

$$D_x = z^x \tag{4.36}$$

When the defects are undistinguishable, using *Bose-Einstein* combinatorial statistics, G_{xy_i} and D_x are given by

$$G_{xy_i} = \binom{x-1}{y_i - 1}, \; x \geq y_i \tag{4.37}$$

$$D_x = \binom{x+z-1}{x} \tag{4.38}$$

The yield model of the fault-tolerant structure with all sub-circuits assumed dependents contains seven terms, (4.28) ~ (4.34), associated with different cases of defects distributed into the whole structure.

(1) The (4.28) term corresponds to the case that defects are only distributed in cells. In this equation, the component $\sum_{F_c=1}^{S_c} \binom{Q_c}{F_c}$ gives the total number of selections of F_c defective cells out of a total Q_c cells, such that the defects can be tolerated. Each defective cell may be caused by one or more, up to n_c, defective EEs. Thus, a total of $\sum_{i_m=1}^{n_n} \binom{n_c}{i_m}$ selections can be chosen for the mth defective cell, $m = 1, 2, \ldots, F_c$. As a result, there is a total of $\sum_{i_1=1}^{n_c} \cdots \sum_{i_{F_C}=1}^{n_c} \prod_{m=1}^{F_c} \binom{n_c}{i_m}$ selections. G_{xy_1} is the number of different distributions of x defects into y_l EEs, such that each EE contains at least one defect.

(2) The (4.29) term corresponds to the case that defects are present only in vertical bundles. Term (4.29) is the same as (4.28), except that the subscript "VB" is used instead of "c", "j_t" instead of "i_m", and "t" instead of "m".

(3) The (4.30) term corresponds to the case that defects are distributed only in horizontal bundles. Term (4.30) is the same as (4.30), except that the subscript "HB" is used instead of "c", "k_p" instead of "i_m", and "p" instead of "m".

(4) The (4.31) term corresponds to the case that defects are distributed only in cells and vertical bundles while there is none in horizontal bundles. $\binom{Q_c}{F_c}\binom{Q_{VB}}{F_{VB}}$ is the number of different selections of F_c defective cells out of Q_c cells and selections of F_{VB} defective vertical bundles out of Q_{VB} vertical bundles. $\sum_{i_1=1}^{n_c} \cdots \sum_{i_{F_C}=1}^{n_c} \sum_{j_1=1}^{n_{vb}} \cdots \sum_{j_{F_{VB}}=1}^{n_{vb}} \prod_{m=1}^{F_c} \binom{n_c}{i_m} \prod_{t=1}^{F_{VB}} \binom{n_{vb}}{j_t}$ gives the number of different selections of i_m defective EEs from n_c in each cell and selection of j_t EEs from n_{VB} in each vertical bundle.

(5) The (4.32) term corresponds to the case that defects are only distributed in both cells and horizontal bundles while there is none in vertical bundles. The expression of (4.32) is the same as (4.31) after replacing the subscript "VB" with "HB", "j_t" with "k_p", and "t" with "p";

(6) The (4.33) term corresponds to the case that defects are present in both vertical and horizontal bundles while there is none in cells. Term (4.33) is the same as (4.31) except for using subscript "HB" instead of "c", "k_p" instead of "i_m", and "p" instead of "m".

(7) The (4.34) term corresponds to the case that each cell and bundle contain at least one defect simultaneously. The components in (4.34) have the same meaning as in previous expressions.

Based on the above yield model of the structure, the equation for evaluating the yield loss contributed by non-tolerable patterns can be developed as follows.

$$(Y_{NTP})_i = \sum_{x=0}^{\infty} P\{x\}(P_{ntx})_i$$

where $P\{x\}$ is the probability that x defects are distributed in the structure, $(P_{ntx})_i$ is the probability that those x defects are distributed in the ith non-tolerable pattern. Then, $(P_{ntx})_i$ can be presented as follows:

$$(P_{ntx})_i = \frac{(NTP_x)_i}{D_x} \tag{4.39}$$

where $(NTP_x)_i$ is the number of type i defect patterns where x defects are not tolerable, and D_x is the number of different distribution of x defects in the structure.

Based on (4.39), the equations for evaluating the yield loss due to two most significant non-tolerable patterns presented in Chapter 3 in forming a logical array of NxN from a physical array of $(N+1)$xN are developed as follows:

Pattern 1: it corresponds to the case where two vertical bundles in the same row of a $(N+1)$xN physical array are defective.

It is evident that $(P_{ntx})_1 = 0$ if $x < 2$. Therefore, the equation for evaluating the yield loss due to Pattern 2 can be written as follows:

$$(Y_{NTP})_1 = \sum_{x=2}^{\infty} P\{x\} \frac{(NTP_x)_1}{D_x} \tag{4.40}$$

where,

$$(NTP_x)_1 = \sum_{F_{VB}=2}^{S_{VB}} \left[\binom{Q_{VB}}{F_{VB}} - \binom{N_{VB}}{F_{VB}} (N_{VB}+1)^{F_{VB}} \right] \sum_{j_1=1}^{n_{VB}} \cdots \sum_{j_{F_{VB}}=1}^{n_{VB}} G_{xy_1} \prod_{t=1}^{F_{VB}} \binom{n_{VB}}{j_t} +$$

$$\sum_{F_c=1}^{S_c} \sum_{F_{VB}=2}^{S_{VB}} \binom{Q_c}{F_c} \left[\binom{Q_{VB}}{F_{VB}} - \binom{N_{VB}}{F_{VB}} (N_{VB}+1)^{F_{VB}} \right] \sum_{i_1=1}^{n_c} \cdots \sum_{i_{F_C}=1}^{n_c} \sum_{j_1=1}^{n_{VB}} \cdots \sum_{j_{F_{VB}}=1}^{n_{VB}} G_{xy_2} \prod_{m=1}^{F_c} \binom{n_c}{i_m} \prod_{t=1}^{F_{VB}} \binom{n_{VB}}{j_t} +$$

$$\sum_{F_{HB}=1}^{S_{HB}} \sum_{F_{VB}=2}^{S_{VB}} \binom{Q_{HB}}{F_{HB}} \left[\binom{Q_{VB}}{F_{VB}} - \binom{N_{VB}}{F_{VB}} (N_{VB}+1)^{F_{VB}} \right] \sum_{k_1=1}^{n_{HB}} \cdots \sum_{k_{F_{HB}}=1}^{n_{HB}} \sum_{j_1=1}^{n_{VB}} \cdots \sum_{j_{F_{VB}}=1}^{n_{VB}} G_{xy_3} \prod_{p=1}^{F_c} \binom{n_{HB}}{k_p} \prod_{t=1}^{F_{VB}} \binom{n_{VB}}{j_t} +$$

$$\sum_{F_c=1}^{S_c}\sum_{F_{HB}=1}^{S_{HB}}\sum_{F_{VB}=2}^{S_{VB}}\binom{Q_c}{F_c}\binom{Q_{HB}}{F_{HB}}\left[\binom{Q_{VB}}{F_{VB}}-\binom{N_{VB}}{F_{VB}}(N_{VB}+1)^{F_{VB}}\right]\sum_{i_1=1}^{n_c}\cdots\sum_{i_{F_C}=1}^{n_c}\sum_{j_1=1}^{n_{VB}}\cdots\sum_{j_{F_{VB}}=1}^{n_{VB}}\sum_{k_1=1}^{n_{HB}}\cdots\sum_{k_{F_{HB}}=1}^{n_{HB}} G_{xy_4}\prod_{m=1}^{F_c}\binom{n_c}{i_m}\prod_{t=1}^{F_{VB}}\binom{n_{VB}}{j_t}\prod_{p=1}^{F_{HB}}\binom{n_{HB}}{k_p}$$

Here, $G_{xy_i}=0$ if $x<y_i$. $y_1=\sum_{t=1}^{F_{VB}} i_t$, $y_2=\sum_{m=1}^{F_c} i_m+\sum_{t=1}^{F_{VB}} j_t$, $y_3=\sum_{t=1}^{F_{VB}} j_t+\sum_{p=1}^{F_{HB}} k_p$,

$y_4=\sum_{m=1}^{F_c} i_m+\sum_{t=1}^{F_{VB}} j_t+\sum_{p=1}^{F_{HB}} k_p$. The component $\binom{Q_C}{F_C}\binom{Q_{HB}}{F_{HB}}\left[\binom{Q_{VB}}{F_{VB}}-\binom{N_{VB}}{F_{VB}}(N_{VB}+1)^{F_{VB}}\right]$

gives the total number of Pattern 1 as described in Chapter 3. The other components of (4.40) are similar to those of (4.28)-(4.34).

Pattern 2: it corresponds to the case where three cells in a corner and one vertical bundle in the first row of a physical array of $(N+1)$xN are defective.

According to the features of Pattern 2, evidently $(P_{ntx})_2=0$ if $x<4$. Thus, the formula for evaluating the yield loss contributed by Pattern 2 is rewritten as follows:

$$(Y_{NTP})_2=\sum_{x=4}^{\infty}P\{x\}\frac{(NTP_x)_2}{D_x} \tag{4.41}$$

Where,

$$(NTP_x)_2=\sum_{F_c=3}^{S_c}\sum_{F_{VB}=1}^{S_{VB}}\left[\binom{4}{1}\binom{Q_c-3}{F_c-3}\right]\left[\binom{N_{VB}}{1}\binom{N_{VB}-1}{F_{VB}-1}(N_{VB}+1)^{F_{VB}-1}\right]\sum_{i_1=1}^{n_c}\cdots\sum_{i_{F_c}=1}^{n_c}\sum_{j_1=1}^{n_{VB}}\cdots\sum_{j_{F_{VB}}=1}^{n_{VB}} G_{xy_5}\prod_{m=1}^{F_c}\binom{n_c}{i_m}\prod_{t=1}^{F_{VB}}\binom{n_{VB}}{j_t}+$$

$$\sum_{F_c=3}^{S_c}\sum_{F_{HB}=1}^{S_{HB}}\sum_{F_{VB}=1}^{S_{VB}}\left[\binom{4}{1}\binom{Q_c-3}{F_c-3}\right]\binom{Q_{HB}}{F_{HB}}\left[\binom{N_{VB}}{1}\binom{N_{VB}-1}{F_{VB}-1}(N_{VB}+1)^{F_{VB}-1}\right]\sum_{i_1=1}^{n_c}\cdots\sum_{i_{F_c}=1}^{n_c}\sum_{j_1=1}^{n_{VB}}\cdots\sum_{j_{F_{VB}}=1}^{n_{VB}}\sum_{k_1=1}^{n_{HB}}\cdots\sum_{k_{F_{HB}}=1}^{n_{HB}} G_{xy_6}\prod_{m=1}^{F_c}\binom{n_c}{i_m}\prod_{t=1}^{F_{VB}}\binom{n_{VB}}{j_t}\prod_{p=1}^{F_{HB}}\binom{n_{HB}}{k_p}$$

Where $G_{xy_i}=0$ if $x<y_i$, $y_5=\sum_{m=1}^{F_c} i_m+\sum_{t=1}^{F_{VB}} j_t$, $y_6=\sum_{m=1}^{F_c} i_m+\sum_{t=1}^{F_{VB}} j_t+\sum_{p=1}^{F_{HB}} k_p$.

$\left[\binom{4}{1}\binom{Q_c-3}{F_c-3}\right]\binom{Q_{HB}}{F_{HB}}\left[\binom{N_{VB}}{1}\binom{N_{VB}-1}{F_{VB}-1}(N_{VB}+1)^{F_{VB}-1}\right]$ gives the total number of Pattern 2 as presented in Chapter 3. The other components of (4.41) are similar to those of (4.28)-

(4.34). Depending on the considered combinatorial statistics, G_{xy_i} and D_x can be expressed with (4.35)-(4.38) respectively.

4.3 Numerical results of the yield with clustered defects

In this section, to investigate the effect of clustered defects on the yield and yield loss of the fault-tolerant structure described in Chapter 2, results of quantitative studies based on models developed in the previous section are presented and analyzed.

4.3.1 Effects of clustered defects on yield losses

In constructing a logical array of 20 by 20 from a physical array of 21x20, Pattern 1 and Pattern 2 presented in Chapter 3 are the two most significant non-tolerable patterns. Therefore, analyzing the yield losses due to these patterns may lead to revealing the typical characteristics of the effects of defect clustering on the yield loss.

The parameters that need to be taken into consideration in the numerical analysis are as follows. Variables Q_C, Q_{VB}, and Q_{HB} are the total number of cells, vertical bundles, and horizontal bundles respectively, Variables S_C, S_{VB}, and S_{HB}, the number of spare cells, spare vertical bundles, and spare horizontal bundles, λ_C,λ_{VB}, and λ_{HB}, the expected number of defects per cell, per vertical bundle, and per horizontal bundle, and α, the clustering parameter.

In this case study, $Q_C = Q_{VB} = Q_{HB} = 420$, $S_C = S_{VB} = S_{HB} = 20$, and $\alpha = 5$ is assumed. Also, according to the proposed WSI architecture, the area of a cell is

0.25cm^2, that of a vertical bundles or a horizontal bundle with 4 wires is 0.4mm^2. With $\lambda = A \times D$, the expected number of defects, λ_c, λ_{VB} and λ_{HB} can be obtained.

The yield curves computed with (4.18) and (4.23), respectively, are presented in Figure 4.2. For comparison, the yield curve computed with (3.10) is also presented in Figure 4.2. The curve with (3.10) represents the case where defects comply with random distributions. Form this figure, it is observed that the yield with clustered defect distributions is lower than that with a random defect distribution when the defect density is below a certain value. It implies that arrays subjected to clustered defects are not so robust as those subjected to random defects at low defect density. However, when the defect density increases, the curves obtained with clustered defects decrease slowly, with "long tails", a sharp contrast to the rapid fall of those with random defects. It shows that the arrays subjected to clustered defects perform much better at high defect density.

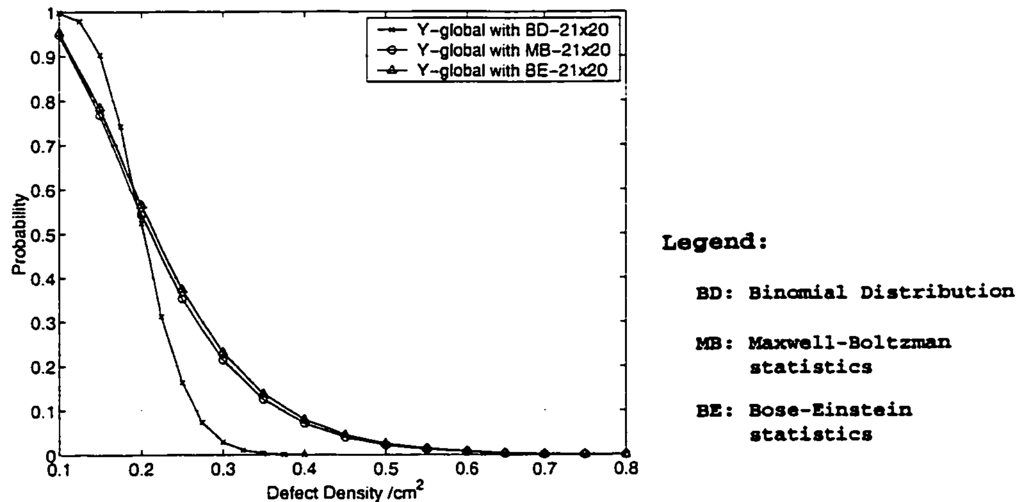


Figure 4.2 Effects of clustered defects on the yield of forming a logical array of 20x20 from a physical array of 21x20. The curve "Y-global with BD-21x20" is derived from (3.10), the one "Y-global with MB-21x20" from (4.18), and the one "Y-global with BE-21x20" from (4.23).

Substituting those respective data into equations (4.19) and (4.24), the numerical results of the yield losses due to these two most significant non-tolerable patterns are also computed. Figure 4.3 and Figure 4.4 show the characteristics of these curves in the two case, respectively. To compare the effect of the clustered defects with that of the random defects, the results of the yield loss computed with (3.15) assuming random defects are also presented in these figures. From Figure 4.3, it is observed that the maximums of the three curves of the yield loss are of the same order of magnitude, which is also observed in Figure 4.4. These figures show that the yield losses contributed by these two most significant non-tolerable patterns at low defect density are insignificant.

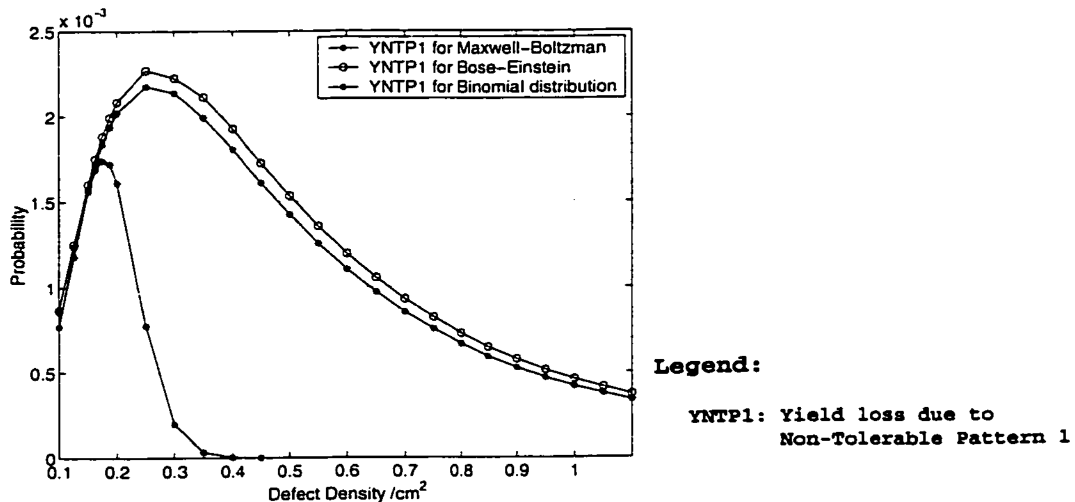


Figure 4.3 Effects of clustered defects on the yield loss contributed by the first most significant non-tolerable pattern in forming a logical array of 20 by 20 from a physical array of 21x20. The curve "YNTP1 for Maxwell-Boltzman" is computed with (4.19), the curve "YNTP1 for Bose-Einstein" is computed with (4.24), and the curve "YNTP1 for Binomial distribution" is computed with (3.15).

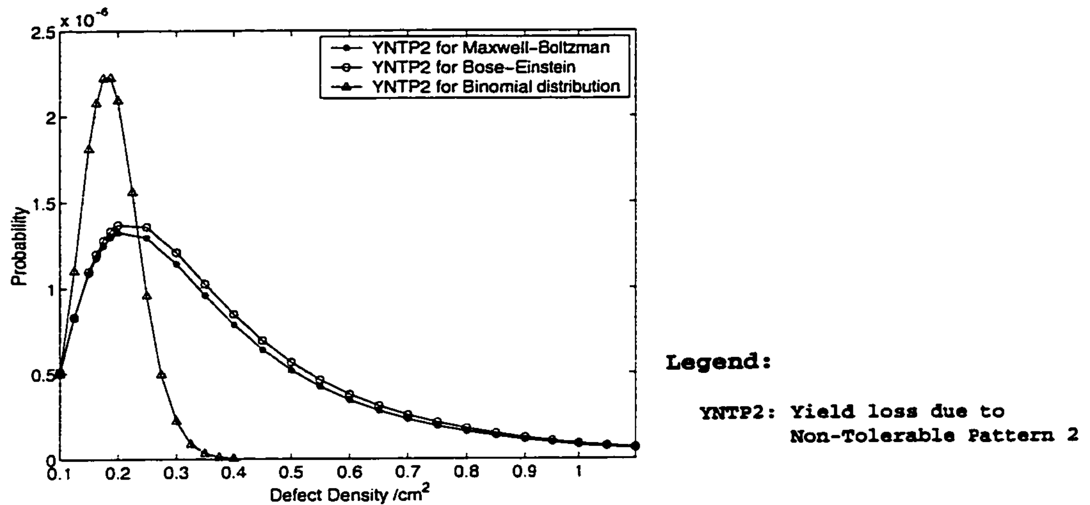


Figure 4.4 Effects of clustered defects on the yield loss contributed by the second most significant non-tolerable pattern.The equations used to compute the results are the same as in Figure 4.3.

For comparison, Figure 4.5 presents the yield curves of the structure assuming global redundancy and the yield loss curves at the region of higher clustered defect density. From Figure 4.5, it is observed that the yield degrades rapidly when defect density is above 1.0 defect per cm^2 and then the yield losses due to the defect Pattern 1 become comparable with the yield of the structure with global redundancy. However, it is noted that the yield has become unacceptable at this higher defect density level and more redundancy is needed to add in the physical array. To summarize, considering the limit of acceptable yields, the yield losses due to non-tolerable patterns in this structure are insignificant when defects are distributed according to the studied clustered distribution. As a result, under the condition of a clustered defect distribution, the yield of the structure can be considered to be approximately equivalent to the yield of the structure assuming global redundancy when the redundancy is suitable.

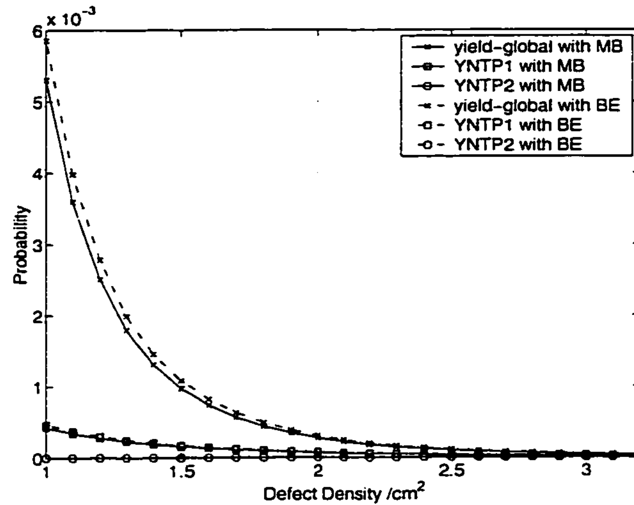


Figure 4.5 Yield and yield losses due to two most significant non-tolerant patterns at higher clustered defect density in forming a logical array of size 20x20 out of a physical array of size 21x20.

Figure 4.2 to 4.5 show that the curves computed with *Maxwell-Boltzman* statistics and *Bose-Einstein* statistics have very similar characteristics. On the limited set of experiments, it appears that the equations developed with the two kinds of combinatorial statistics do not make much difference in the computation of the yield losses.

Computing the yield loss with (4.40) and (4.41) for large arrays is very time-consuming as illustrated in Table 4.1. Thus, the yield loss of forming smaller arrays is investigated to analyze the effects of clustered defects. In this case, it is assumed that a logical array of 5 by 5 is constructed from a physical array of 6x5. The yield losses are evaluated with equations, (3.15), (4.19), (4.24), (4.40) and (4.41), with different assumptions with respect to defect distributions, from the purely random one to the fully clustered one. In the numerical calculations, it is assumed that bundles are composed of 40 wires and that they have an area of $0.11cm^{-2}$. The area of a cell is $0.25cm^{-2}$. The clustering parameter is assumed to be $\alpha=5$ [12]. Figure 4.6 and Figure 4.7 show the results. From these figures, it

is shown that the yield loss computed with the Poisson random distribution Equation (3.15) is larger than the others when the defect density is below a certain value. The yield loss curve with the random defect distribution go down rapidly with the increase of the defect density. However, the curves of the yield losses with clustered defects fall relatively slowly, and the yield losses become larger than those obtained with the random defect distribution beyond a certain value of the defect density. For instance, the yield losses evaluated by (4.40) and (4.41) decrease at the slowest rate among all these yield losses with the increase of the defect density. In the equations (4.40) and (4.41), the defects in all sub-circuits are assumed statistically dependent. It implies that the defects tend to be clustered over the structure, which is also called as large area clustering [17]. It is observed that clustering changes the rate at which yield decreases with defect density.

Table4. 1 Computation time of one numerical point of the yield loss curves in forming a logical array of size 20x20 from a physical array of size 21x20, where a bundle comprises 40 wires with an area 11 mm^2 and the area of a cell is 25mm^2. The clustering parameter α=5 were used based on ITRS[12].

Computer information	Yield loss (YNTP1) model	CPU time
Manufacturer: Sun Microsystems System Model: Ultra 10 Real Memory: 512 M Virtual Memory: 2048 M Number of CPUs: 1 CPU type: sparcv9 OS name: SunOS OS version: 5.8	Equation (3.15) assuming pure random defect	42 ms
	Equation (4.19) assuming partial clustered defect, with Maxwell-Boltzman statistics	386 s
	Equation (4.24) assuming partial clustered defect, with Bose-Einstein statistics	189 s
	Equation (4.40) assuming large clustered defect, with Maxwell-Boltzman statistics	159225 h (Estimation)
	Equation (4.40) assuming large clustered defect, with Bose-Einstein statistics	12332 h (Estimation)

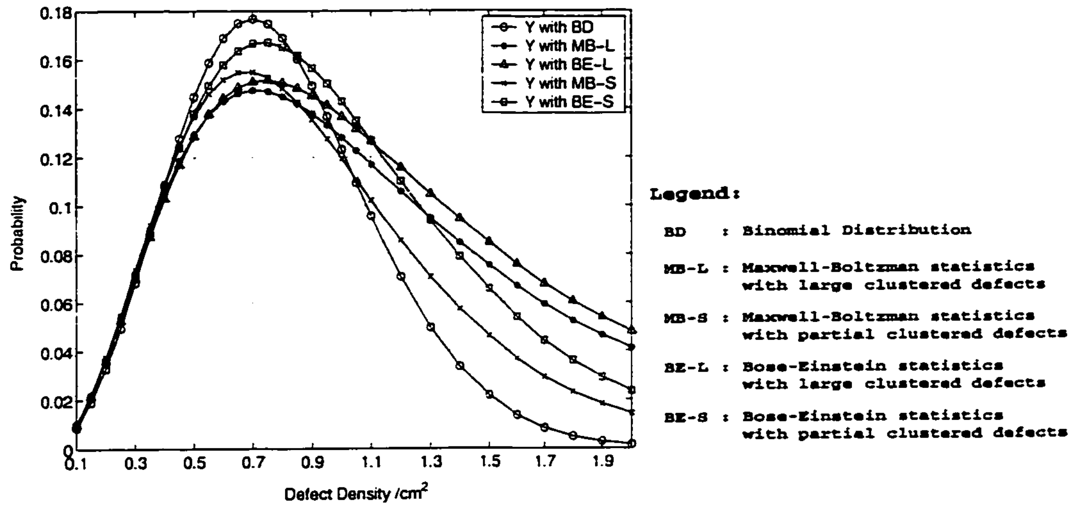


Figure 4.6 Yield loss contributed by the first most significant non-tolerable pattern in forming a logical array of 5x5 from a physical array of 6x5. The curve of "Y with BD" is derived from (3.15), "Y with MB-L" from (4.40) using Maxwell-Boltzman statistics, "Y with BE-L" from (4.40) using Bose-Einstein statistics, "Y with MB-S" from (4.19) and "Y with BE-S" from (4.24)

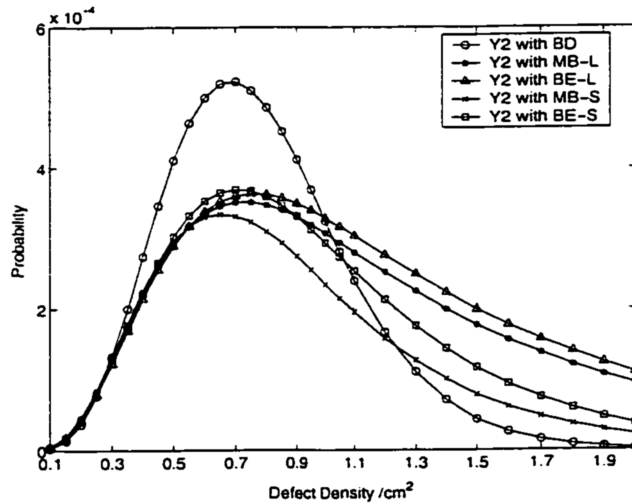


Figure 4.7 Yield loss contributed by the second most significant non-tolerable pattern in forming a logical array of 5x5 from a physical array of 6x5. The curve of "Y2 with BD" is derived from (3.15), "Y2 with MB-L" from (4.41) using Maxwell-Boltzman statistics, "Y2 with BE-L" from (4.41) using Bose-Einstein, "Y2 with MB-S" from (4.19) and "Y2 with BE-S" from (4.24).

4.3.2 Effects of the clustered defects on the yield of forming logical arrays

To study the effects of clustering on the yield of the fault-tolerant structure described in Chapter 2, the case of 3 logical arrays of size 20x20 constructed from physical arrays of size of 21x20, 21x21 and 22x22, respectively, is used. The yield of the various structures assuming global redundancy are computed with equations developed in previous sections. In the numerical calculation, it is assumed that a bundle is composed of 40 wires, and the areas of a bundle in these physical arrays are different, $0.096cm^{-2}$ for the physical array of size 21x20, $0.10cm^{-2}$ for that of 21x21, and $0.11cm^{-2}$ for that of 22x22, respectively. The area of a cell is $0.25\ cm^{-2}$. It is also assumed that $\alpha = 5$ when (4.18) and (4.23) are used.

Figure 4.8 presents the characteristics of the yield computed with (4.18) and (4.23) assuming partially clustered defects in the array structure, i.e., the defects only in identical sub-circuits are statistically dependent. For comparison, the yield curves computed according to (3.10) with a completely random distribution are also shown in this figure. In this figure, it should be noted that the yield curves with clustered defects shift right when the number of the spares of the physical array increases. Evidently, clustered defects have no major impact on the yield trends when the redundancy of a physical array increases. With suitable redundancy, the array is rather robust to variations of the defect density when it is below some threshold values. However, it is shown that clustering reduces the yield when the defect density is smaller. For example, in forming a 20x20 logical array from the physical array of size 22x22, the yield with the clustered defects are lower than the yield with the random defects when the defect density is below $0.7cm^{-2}$. It implies, for fault-tolerant circuits, that clustered defects tend to lower the effectiveness of fault tolerance as described by several authors [22][34].

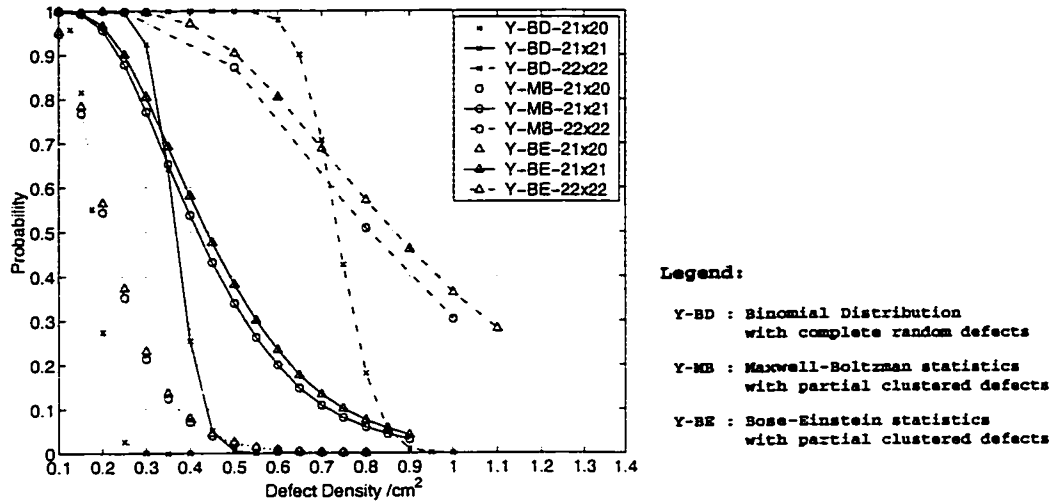


Figure 4.8 Yield of forming logical arrays of size 20x20 from physical array of size 21x20, 21x21, and 22x22. "BD", "MB" and "BE" indicate that the curves are obtained from equations (3.10), (4.18), and (4.23) respectively.

In Figure 4.8, it is also shown that the yield computed by (4.23), with *Bose-Einstein* statistics, is a little higher than that by (4.18), with *Maxwell-Boltzman* statistics. However, both curves have the same shape. Let us note that numerical yield computation with (4.18) needs careful consideration in programing the computation. To avoid overflows, it is necessary to deal with alternating series in the equation. Thus, the numerical computation of Equation (4.18) requires a much longer computation than that of (4.23), but both produces very similar results. Moreover, if the effect of completely clustered defects is considered for a large physical array, the computation process will be more complex and time-consuming.

Due to limitation in computational power, the computation of yields for larger arrays with (4.27) is difficult. To illustrate the impacts of large area clustered on yields, a smaller physical array is used. In the numerical analysis, it is assumed that a logical array of 4 by 4 is constructed from physical arrays of 5 by 4 and 5 by 5, respectively. The area of a

bundle is $0.11cm^{-2}$, the same as that used with a physical array of size 22x22. The area of a cell is $0.25\ cm^{-2}$ and the clustering parameter is 5. Figure 4.9 and Figure 4.10 present the results of the yield as a function of the defect density. From Figure 4.9 and Figure 4.10, it is observed that all yield curves shift right with the increase of the redundancy ratio in the physical arrays. It is shown that a clustered defect distribution does not impact the general yield trends as described in Chapter 3. Also it is observed that large area clustering tends to lower the yield when the defect density is below some levels. It implies that, due to the interaction of the yield of the sub-circuits, clustered defects in a wafer scale system partitioned into sub-circuits can potentially result in reduced yield, as described in [16][22][36]. Figure 4.10 illustrates that the yield curves computed with (4.18) and (4.23) fall rapidly above some defect density threshold, as those obtained with (3.10), but those computed with (4.27) go down slower. As for (4.27), it is derived with the assumption of completely clustered defects. From these figures, it is clear that the yield computed with different yield equations present some significant differences when the defect density is higher. Thus, clustering has a great impact on yield when defect densities are higher.

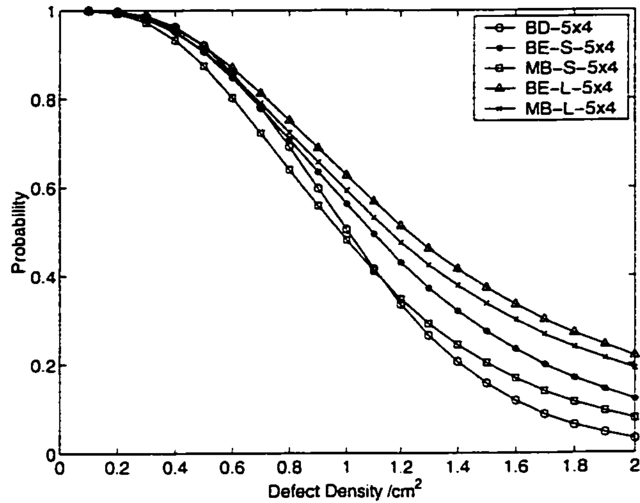


Figure 4.9 Comparison of the yield computed with different equations in constructing a logical array of 4x4 from a physical array of 5x4. "BD", "BE-S", "MB-S" indicate that the curves are obtained with(3.10), (4.23) and (4.18), respectively. The curve indicated by "BE-L" is computed with (4.27), (4.37) and (4.38). The one indicated by "MB-L" is done with (4.27), (4.35) and (4.36). The symbols in the legend are the same as those in Figure 4.6.

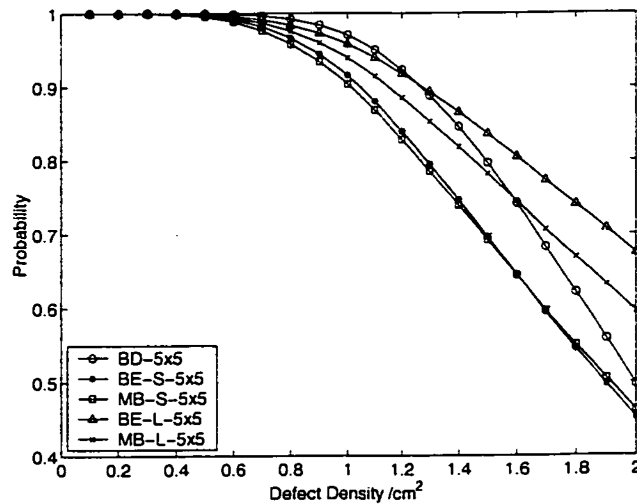


Figure 4.10 Comparison of the yield computed with different equations in constructing a logical array of 4x4 from a physical array of 5x5. "BD", "BE-S", "MB-S" indicate that the curves are obtained with(3.10), (4.23), and (4.18), respectively. The curves labeled "BE-L" are computed with (4.27), (4.37), and (4.38). The ones labeled "MB-L" are computed with (4.27), (4.35), and (4.36). the symbols in the legend are the same as those in Figure 4.6.

4.4 Yield model regression with clustered defects

In this section, to find a simple method to evaluate the yield of large arrays subjected to clustered defects, the regression model introduced in Chapter 3 is extended to the clustered defect distribution such as *Bose-Einstein*.

In this study, the yield of arrays of equivalent redundancy ratio, but different sizes are evaluated according to Equation (4.27). The results are shown in Figure 4.11. it should be noted that the obtained yield curves tend to cross approximately the point where the probability is equal to $1-e^{-1}$, which has been mentioned in Chapter 3. Table 4.1 presents numerical calculation results of the approximate cross points. From the table, it is shown that, regardless of the array size, in each of the arrays, the defect density that results in a yield of $1-e^{-1}$ is around a certain value of 0.47. As an approximation, the point can again be considered as a pivot point.

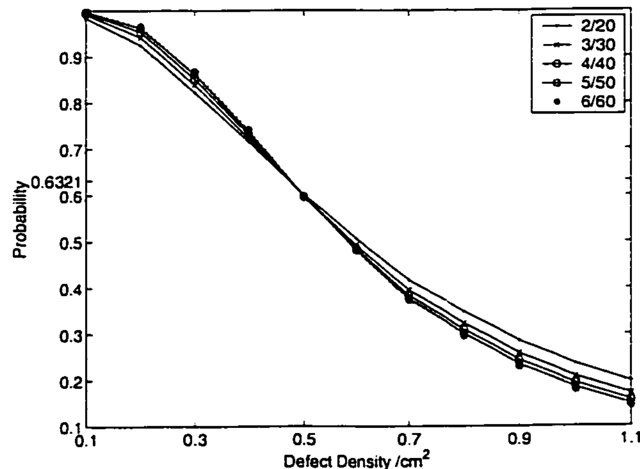


Figure 4.11 Yield of arrays with equivalent redundancy ratio, computed with (4.27), (4.35), and (4.36) using *Bose-Einstein* statistics. 2/20 array for a physical array with 20 cells including 2 spares, and the other arrays of different sizes have the same redundancy ratio as 2/20.

Table 4.2 Numerical value of the approximate pivot points for arrays with redundancy ratio equal to 0.1. It is assumed that defects comply with *Bose-Einstein* distribution.

Size of arrays	Number of spares	Defect density (cm^{-1})	Probability
20	2	0.47279923	$1-e^{-1}$
30	3	0.47161067	$1-e^{-1}$
40	4	0.47334149	$1-e^{-1}$
50	5	0.47512312	$1-e^{-1}$
60	6	0.47650617	$1-e^{-1}$
70	7	0.47748665	$1-e^{-1}$
80	8	0.47814201	$1-e^{-1}$

Similar to the method used to develop the regression model with the random defect distribution in Chapter 3, a simple regression model with the clustered distribution can be derived by using these approximate pivot points. This regression model can be used to predict the yield of larger arrays in the region around the pivot point. Especially, when it is difficult to compute the true yield of large arrays with the clustered defects, the regression yield model can help to determine the characteristics of the true yield curves in the region of interest. The defect density, δ(r), where the probability is equal to $1-e^{-1}$, and the slope at the pivot point, κ(r,m), can be approximated by (4.42) and (4.43), respectively.

$$\delta(r) = -0.0407 + 5.1175r \tag{4.42}$$

$$\kappa(r, m) = 0.0860r^{-1.12} + (4.0352\times 10^{-3} - 8.7529\times 10^{-4}r)m \tag{4.43}$$

where r is the redundancy ratio of a physical array of size K by L, and m is the number of cells in the physical array, i.e., $m=KxL$. $\kappa(r,m)$ is expressed with an absolute value in (4.43). Figure 4.12 presents the yield curves predicted by the regression models and the complete yield curves computed with *Bose-Einstein* distribution represented by (4.27), (4.37) and (4.38). It is observed that the yield predicted by the regression models is a good agreement with those computed with the complete yield models. In this figure, the yield curves of large arrays of 21x20 and 22x22, predicted with the regression models, indicate that the characteristic curve around the threshold become steeper with the increase of the physical array sizes.

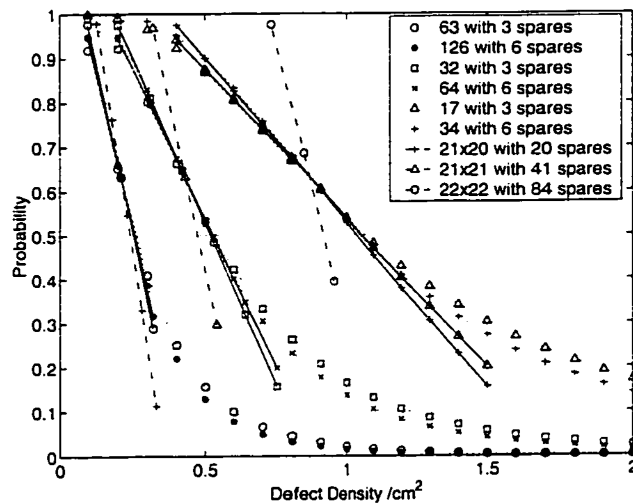


Figure 4.12 Comparison between the regression model and the yield model assuming *Bose-Einstein* distribution. The dotted lines are obtained from the complete yield model, the solid lines and the dash-dot ones from the regression models.

Figure 4.13 presents the yields predicted by the regression models in (4.43) and (4.44) with those computed with the regression model based on random defect distributions in (3.25) and (3.26). For comparison, the yield curves computed with the Binomial distribution are also presented in this figure. From Figure (4.13), it is shown that, for

physical arrays of the same size, the curve of the yield predicted by the regression model based on random defect distributions is much steeper than that based on a clustered defect distribution. This results agree with the previous studies presented in Figure 4.6. Furthermore, using this regression model to estimate the yield is very time-efficient. Table 4.3 illustrates required CPU time for the computations of different yield models. It should be noted that the computation for the regression models cost the least CPU time among all. Therefore, using this model can give a quick yield prediction of large size arrays subjected to a clustered defect distribution.

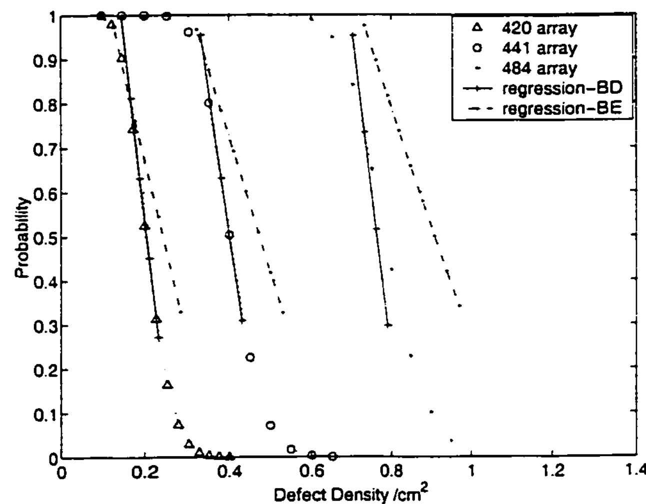


Figure 4.13 Comparison of the yield predicted by regression model with the clustered defect distribution and the random defects distribution. The dotted lines are obtained from complete random defect models, the solid line from the regression yield models with random defects, and the dash-dot lines from the regression yield models with clustered defects.

Table 4. 3 Computation time for one numerical point of different yield curves in forming a logical array of 20x20 from a physical array of 21x21, where a bundle comprises 40 wires with an area 11 mm^2 and the area of a cell is 25mm^2.

Computer information	Yield model	CPU time
Manufacturer: Sun Microsystems System Model: Ultra 10 Real Memory: 512 M Virtual Memory: 2048M Number of CPUs: 1 CPU type: sparcv9 OS name: SunOS OS version: 5.8	Equation (3.10)- random defect, with Binomial distribution.	833 ms
	Equation (4.18)-partial clustered defects, with Maxwell-Boltzman statistics	237 min.
	Equation (4.23)-partial clustered defects, with Bose-Einstein statistics	12 min.
	Equation (4.42) and (4.43), regression model assuming large clustered defect	< 1ms
	Equation (4.27) -large clustered defect, with Maxwell-Boltzman statistics	1.97×10^{12} h (Estimation)
	Equation (4.27) assuming large clustered defect, with Bose-Einstein statistics	4.24×10^{11} h (Estimation)

4.5 Summary

In this chapter, yield losses due to non-tolerable defect patterns have been re-evaluated with the assumption of clustered defects. Based on this assumption, the defect distribution is expressed with the negative binomial distribution. Two kinds of combinatorial statistics are used to deal with the two cases of clustered defects to derive the yield models. The first case is assumed distinguishable defects and *Maxwell-Boltzman* combinatorial statistics is used. In the second case, defects are assumed indistinguishable *and Bose-Einstein* combinatorial statistics is applied. By assuming different statistical correlations among cells, vertical bundles and horizontal bundles, respective yield models are derived and the corresponding equations for evaluating yield losses are obtained in this chapter.

It has been found that the results obtained by using yield models assuming clustered defect distributions agree with those based on a random defect distribution. It shows that the non-tolerable patterns have no significant effect in terms of yield loss in the region of interest when the array structure possesses suitable redundancy. A numerical analysis of the yield with clustered defects has been conducted. It is found that, when the defect density is below a certain value, the yields are lower than those obtained with random defects. It implies that, in the case of fault-tolerant circuits, clustered defects tend to reduce the effectiveness of fault tolerance. However, the clustered defects also reduced the rate at which yield decrease with defect density. Consequently, the yield with clustered defect distributions can be very different from the one with random defects when the defect density is higher.

In this chapter, the regression yield model proposed in the previous chapter has been extended to reflect clustered defects distribution such as *Bose-Einstein*. Using these simplified yield models, one can quickly predict the slope and pivot point of true yield curves of large arrays subjected to clustered defect distributions.

Chapter 5
Conclusion

5.1 Summary of the work

In this thesis, a closed form yield model has been proposed. In this model, the constraints of a complex interconnection architecture has been taken into account. It is applicable to the architectures in which approximate global redundancy is involved and for which constraints are interpreted into yield losses. The impact of such yield losses can be evaluated as follows. First, the probabilities of the existence of non-tolerable defect patterns is calculated. Then, the impact can be assessed by comparing the yield of the architecture with global redundancy and these probabilities.

With this approach, the diagnosis and analysis of a complex interconnect architecture with fault tolerance has been processed. It is shown that it is difficult to find all the significant non-tolerable patterns but they are tractable. After a great deal of study on the operation of the fault-tolerant structure, the most significant non-tolerable defect patterns have been identified and proved. To study the impact of these defect patterns on the yield of the architecture, yield loss equations for evaluating these defect patterns have been developed. With these equations, the numerical results of the yield losses contributed by the significant non-tolerable patterns were computed. It has been proved that many complex patterns with large number of defects can not be tolerated, but the yield loss due to these patterns decreases very rapidly; thus, they become insignificant. It has also been shown that most of the yield losses in this structure result from a few non-tolerable

patterns comprising small number of defects, and that the yield losses sharply decrease with the increase of the number of defects involved in a pattern. The amount of reduction is in the order of several decades of magnitude with one or two additional defects in a pattern. Thus, even though finding all non-tolerable patterns is intractable, it is only needed to find the set of small defect patterns that cannot be tolerated. The yield losses contributed by small defect patterns of this structure have also been studied. If a suitable redundancy is added in the structure, it has been shown that the yield losses are small enough to be neglected. It is commonly known that neglecting the yield losses due to non-tolerable patterns leads to an overestimation of the yield. However, because of the very low probability of non-tolerable patterns in this structure, the error is quite small in practice. Approximately, with suitable redundancy, the yield of the fault-tolerant structure with constraints can be expressed by the yield of the structure with global redundancy.

In this thesis, based on the study on the yield of the structure assuming global redundancy, the sensitivity of the yield of the targeted array to variations of the defect density has been investigated. To develop the yield models, several assumptions are made in terms of different kinds of sub-circuits in the structure and nature of defects. This structure has three kinds of main sub-circuits, cells, vertical bundles and horizontal bundles. Defects in each kind of the sub-circuit are assumed statistically independent. In this case, the yield models are obtained. The results of the yield computed with these models show that the circuit array is fairly robust because the yield losses are proved to be insignificant in the region of interest. It is noted that the yield is very sensitive to the defect density around an observed certain points called the threshold. A relatively steep curve of the yield to defect density relationship around the threshold is observed. When the level of

redundancy is not suitably adjusted, the yield rapidly degrades. With these yield models, the required redundancy of a physical array for forming a logical array with robust yield is also predicted.

Yield model have also been developed for the case of a clustered defect distribution. To deal with clustering, *Maxwell-Boltzman* combinatorial statistics and *Bose-Einstein* combinatorial statistics are used. By establishing different statistical correlations of the sub-circuits, the yield models with clustered defects are developed. Based on these models, the equations for evaluating yield losses under the condition of the clustered defect distribution have been derived. The numerical results computed with these equations show that the non-tolerable patterns in a physical array with suitable redundancy are proved to be insignificant in the region of interest when defects comply with a clustered defect distribution. These results are consistent with those obtained with a random defect distribution. In addition, a relatively steep characteristic curve in the yield versus clustered defect density relationship is also observed. When the redundancy level is suitable, below some defect density threshold, a circuit array can be made robust. The study shows that defect clustering changes the rate at which yield decreases when the defect density increases. As a result, around the threshold, the yield curves with clustered defects is not as steep as those with random defects. Furthermore, it is demonstrated that, when the defect density is lower, the yield of the fault-tolerant structure can be reduced by the clustered defects. It implies that, in the case of fault-tolerant circuits, clustered defects tend to decrease the effectiveness of fault tolerance.

In this thesis, regression yield models have also been proposed. Using a simple regression analysis, a simplified yield model with random defects is developed to

reasonably predict the slope and pivot points of the true yield curves. Additionally, these models can be used to predict the redundancy needed for given array and cell sizes. Furthermore, the proposed regression models and results are extended to clustered defect density distributions such as the *Bose-Einstein* distribution. With these simplified yield models, the slope and pivot points of the yield curves of large arrays can be easily evaluated. Whereas, with complete yield models, the numerical computation for those data is a very time-consuming.

5.2 Suggestions for future research

For the circuit architecture studied in this thesis, the yield modeling is based on the assumption that the reconfiguration logic is fault-free. The fault tolerance schemes used in the architecture make the reconfiguration logic mostly non-critical to the existence of defects in the structure. However, when a bundle contains many wires, the reconfiguration wire complexity increases correspondingly. A study on the impact of defective reconfiguration logics on the yield needs to be undertaken as a future study.

When this complex interconnection architecture is implemented with WSI, there will exist a misalignment problem of the connection of the data buses between neighboring cells in the fabrication. The study of how this potential misalignment impacts the yield and yield model of the structure should be conducted.

Finally, the yield of harvesting a logical array depends heavily on the practical reconfiguration algorithms applied to a fault-tolerant structure. Therefore, the yield model needs to be adjusted to reflect the practical impact of reconfiguration algorithms.

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Appendix A. Terminology and replacement rules of the fault-tolerant structure

The terminologies used in the yield analysis of this thesis are defined in this appendix. Due to the limitation of the number of recofiguration wires, there are some constraints in the replacement of the defects in the structure. These constraints are generalized as some basic replacement rules (detail analysis of these rules are shown in [47]). For convenience of the study, the corresponding analysis expresses of these rules are presented as follows.

A.1 Terminology of the fault-tolerant structure

The fault-tolerant structure is divided into several basic sub-circuits. Among them, cells, vertical bundles and horizontal bundles, are basic replaceable units. The respective redundancy is added in this structure to achieve fault tolerance. In the yield analysis of the structure, all basic sub-circuits are defined as following:

(1)Cell: comprising processing elements and its related reconfiguration circuits that include JTAG controller, configuration registers and receiver multiplexers of the cells.

(2)Horizontal bundles: comprising the vertical transmitter multiplexers and the horizontal interconnections between cells.

(3)Vertical bundles: comprising the horizontal transmitter multiplexers and the vertical interconnections between cells.

(4)Reconfiguration logic: the interconnections between cells and bundles for the reconfiguration of cell replacements and bundle replacements.

The properties and symbols of a cells and a bundle in a physical array of size (N+S)x(N+S) based on the architecture[27]-[29] are also defined as the following.

(1)P(i,j): a physical cell of a physical array, where i and j indicate the column and the row where the cell is located. L(i,j): a logical cell of a target logical array.

(2)SC(i,j): the status of the physical cell P(i,j).

$SC(i,j) = \begin{cases} 1 \\ 0 \end{cases}$, where 1 indicates that the cell is defective and 0 indicates that the cell is good.

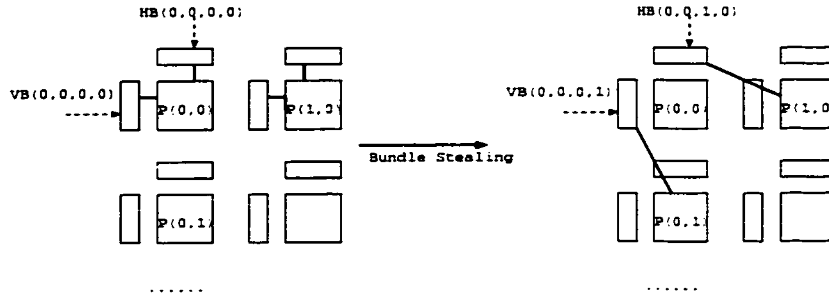


Figure A.1 An example of the expression of VB(i,j,k,l) and HB(i,j,k,l).

(3)VB(i,j,k,l): a vertical bundle, as shown in Figure A.1. Where i and j indicate the physical column and row of the cell originally owning this bundle, k and l indicate the physical column and row of the cell that is current owner of this bundle. $|i-k| \le 1$ and $|j-l| \le 1$.

(4)HB(i,j,k,l): a horizontal bundle, as shown in Figure A.1. Where i and j indicate the physical column and row of the cell originally owning this bundle, k and l indicate the physical column and row of the cell that is current owner of this bundles. $|i-k| \le 1$ and $|j-l| \le 1$.

(5) SVB(i,j): the status of a vertical bundle that originally belongs to the cell P(i,j).

$SVB(i,j) = \begin{cases} 1 \\ 0 \end{cases}$ 1: defective, 0: good.

(6)SHB(i,j): the status of a horizontal bundle that originally belongs to the cell P(i,j).

$$SHB(i,j) = \begin{cases} 1 \\ 0 \end{cases} \text{ 1:defective; 0: good.}$$

(7)C_R(x)_H(i,j,k,l): representing the multiplexer of the xth horizontal receiver of the cell P(i,j). Here, k and l indicate the selected signals from the vertical transmitter of the cell P(k,l), and x=1,2,...,(N+S)-1.

C_R(y)_V(i,j,k,l): representing the multiplexer of the yth vertical receiver of the cell P(i,j). Here, k and l indicate the selected signal from the horizontal transmitter of the cell P(k,l), and y=1,2,...,(N+S)-1

C_Tran_H(i,j,k,l): representing the multiplexer of the horizontal transmitter of the cell P(i,j) and it is currently owned by the cell P(k,l). where $|i-j| \le 1$ and $|k-l| \le 1$.

C_Tran_V(i,j,k,l): representing the multiplexer of the vertical transmitter of the cell P(i,j) and it is currently owned by the cell P(k,l), where $|i-j| \le 1$ and $|k-l| \le 1$.

A.2 Replacement rules of the fault-tolerant structure

In the structure a defective cell or bundle in a corner can be replaced with a respective spare one in the other corner through shifting the space one by one position at a time. As an approximation, the structure provides global redundancy. However, due to the limit of the number of reconfiguration wires, constraints are present in the structure and replacing defects must comply with the rules as the follows (the detail analysis is shown in [47]).

(1)Cell replacement rule

A defective cell can directly be replaced by any of its nearest neighbors.

(2)Bundle replacement rule

A defective horizontal bundle can directly be replaced with a good bundle in the same row or its nearest neighboring rows, the same is true for the vertical bundle. In analytical

expression, for any vertical bundle VB(i,j,k,l) and horizontal bundle HB(i,j,k,l), two condition, $|i-j| \le 1$ and $|k-l| \le 1$, must be satisfied if the replacement succeeds.

(3)Transmitter connectivity rule

For the transmitter multiplexer of a vertical transmitter, C_R(y)_V(i,j,k,l), two condition, $|i-k| \le 1$ and $|j-l| \le 1$, should be satisfied in order to establish successful connections. The same is true for the transmitter multiplexer of a horizontal transmitter C_R(y)_H(i,j,k,l), where $|i-k| \le 1$ and $|j-l| \le 1$

(4)Receiver connectivity rule

Any horizontal receiver of a cell can only receive signals from the transmitters of cells that are located in the same row or in its nearest neighbor rows. The analytical expression is as the following.

For the receiver multiplexer of any horizontal receiver of a cell, C_R(x)_H(i,j,k,l), where, x=1,2,...,(N+S)-1, $|j-l| \le 1$, and $i \ne k$ if $j \ne l$.

The receiver multiplexer of any vertical receiver of a cell can only receive signals from the transmitters of cells located in the same column or in its nearest neighbor column.

For the receiver multiplexer of any vertical receiver of a cell, C_R(x)_V(i,j,k,l), where, x=1,2,...,(N+S)-1, $|i-k| \le 1$, and $j \ne l$ if $i \ne k$.

(5)Receiver source exclusion rule

The horizontal receivers of a cell cannot receive signals simultaneously from more than one transmitter of cells located in the same physical column.

For the two receiver multiplexers of any two horizontal receivers of a cell, C_R(x_1)_H(i,j,m_1,n_1) and C_R(x_2)_H(i,j,m_2,n_2), if $x_1 \ne x_2$, then $n_1 \ne n_2$.

The vertical receivers of a cell cannot receive signals simultaneously from more than one transmitter of cells that are located in the same physical row.

For the two receiver multiplexers of any two vertical receivers of the cell, C_R(y_1)_H(i,j,m_1,n_1) and C_Ry_2_H(i,j,m_2,n_2), if $y_1 \neq y_2$ then $m_1 \neq m_2$

Appendix B. Thirteen kinds of non-tolerable patterns

Thirteen kinds of non-tolerable patterns in a physical array of $(N+1) \times N$ are presented in this appendix. In this case, all bundles are assumed to be good and they are not shown in the graphs to simplify the configuration.

(1)**Pattern 1**: Corresponding to the case where six cells in any of four corners of the array are defective, as shown in Figure B.1.

In this case, the position of defective cells C1-C6 prevents two defective cells C1 and C2 from being replaced with good spare cells although there are available spares in the array. Moreover, because of the limit of the number of spare columns, only one physical column in the array can be excluded with the row or column exclusion strategy described in Chapter 2. Consequently, there are not enough good cells for a certain logical column of the logical array of $N \times N$ no matter what kind of construction method is used.

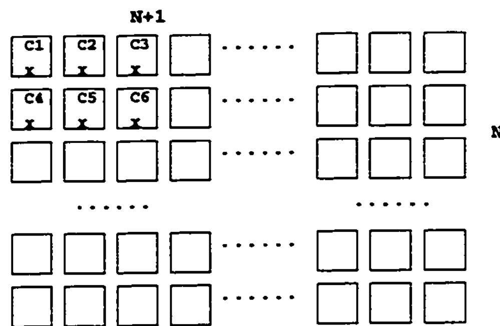


Figure B.1 Non-tolerable Pattern 1.

The equation for calculating the total number of this kind of non-tolerable pattern is presented as the following.

$$NTC_{cell} = \binom{4}{1}\binom{(N+1)N-6}{F_c-6}$$

(2)**Pattern 2**: corresponding to the case where seven defective cells in any of four corners of the array are defective as shown in Figure B.2.

In this case, if the second column containing three defective cells (C1, C4 and C7) is used as spare column, defective cell C2 cannot be replaced by a good spare cell in the second column. Moreover, due to the presence of defective C7, only one defective cell C1 or C2 can be replaced by the good spare cell if the other column is used as spare column other than the second column. Consequently, it is sure that there are not enough good cells for a certain column of the logical array of *N*x*N* no matter what kind of construction method is used.

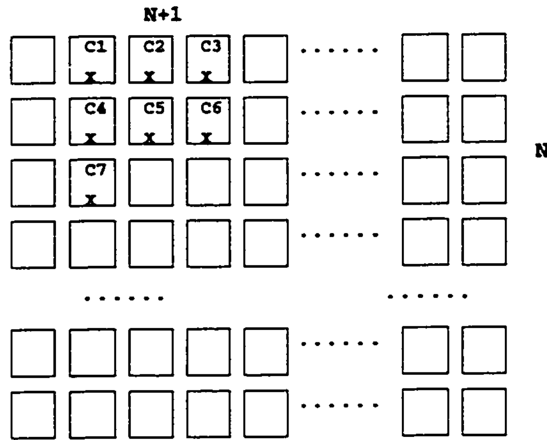


Figure B.2 Non-tolerable Pattern 2.

The equation for calculating the total number of this kinds of non-tolerable patterns is presented as $NTC_{cell} = \binom{4}{1}\binom{(N+1)N-7}{F_c-7}$.

(3)**Pattern 3**: corresponding to the case where eight cells in the two corner of the array are defective as shown in Figure B.3.

In this case, because only one spare column in a physical array of (*N*+1) x *N* can be used to form a logical array of *N* x *N*, there must be one defective cell, C1 or C6, cannot be

replaced with a good spare cell. Consequently, there must be not enough good cells for a certain column of the logical array of NxN no matter what kind of construction method is used.

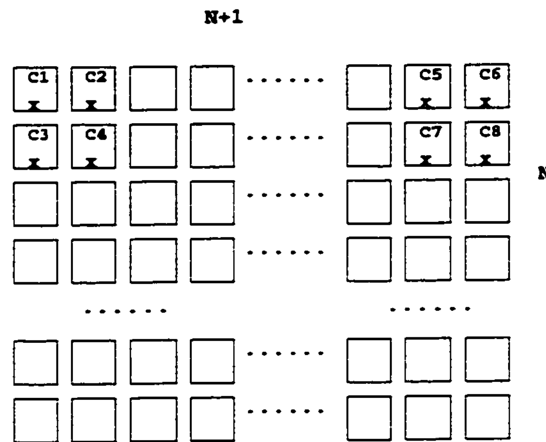


Figure B.3 Non-tolerable Pattern 3.

The equation for calculating the total number of this kinds of non-tolerable pattern is presented as $NTC_{cell} = \binom{2}{1}\binom{2}{1}\binom{(N+1)N-8}{F_c-8}$.

(4)**Pattern 4**: corresponding to the case where eight cells in the top or bottom of the physical array are defective as shown in Figure B.4.

In the case, there must be one defective cell, C2 or C3, can not be tolerated.

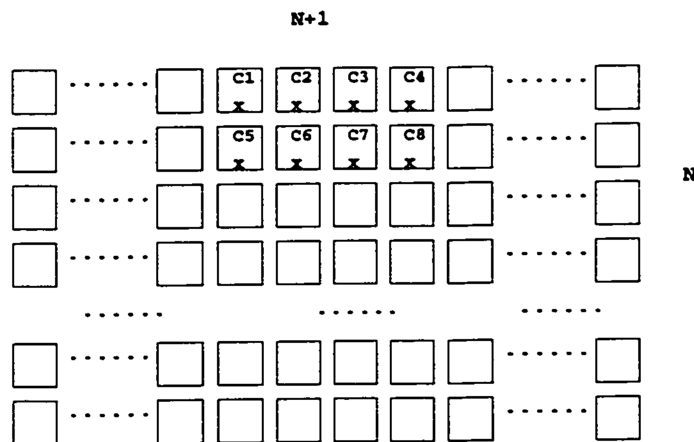


Figure B.4 Non-tolerable Pattern 4.

The equation for calculating the number of this kind of non-tolerable pattern is presented as the following.

$$NTC_{cell} = \binom{2}{1}(N-1)\binom{(N+1)N-8}{F-8}$$

(5)**Pattern 5**: corresponding to the case where nine cells in any of two edges of the array are defective, as shown in Figure B.5.

In this case, one defective cell, C4 or C5, are not tolerable.

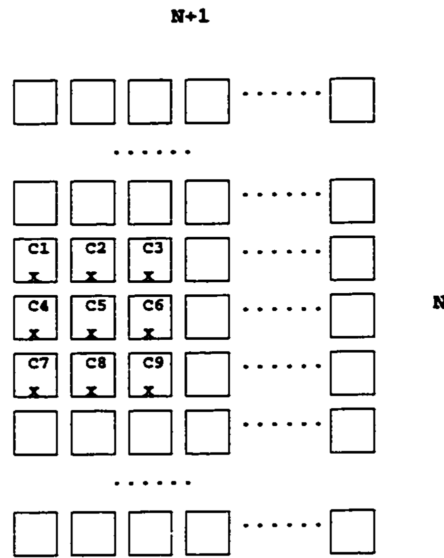


Figure B.5 Non-tolerable Pattern 5.

The equation for calculating the number of this kind of non-tolerable pattern is presented as the following.

$$NTC_{cell} = \binom{2}{1}(N-2)\binom{(N+1)N-9}{F_c-9}$$

(6)**Pattern 6**: corresponding to the case where at least ten cells that are shown in Figure B.6 are defective.

In this case, because the limit of spare column in the physical array, one defective cell, C1 or C8, can not be tolerated.

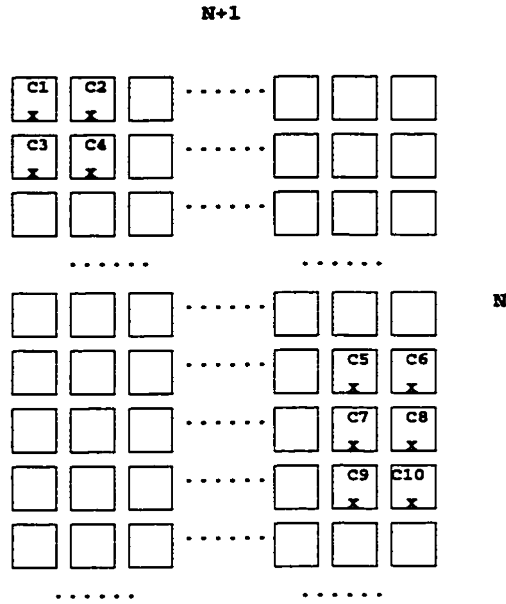


Figure B.6 Non-tolerable Pattern 6.

The equation for calculating the total number of this kind of non-tolerable pattern is presented as: $NTC_{cell} = \binom{2}{1}\binom{2}{1}(N-2)\binom{(N+1)N-10}{F_c-10}$

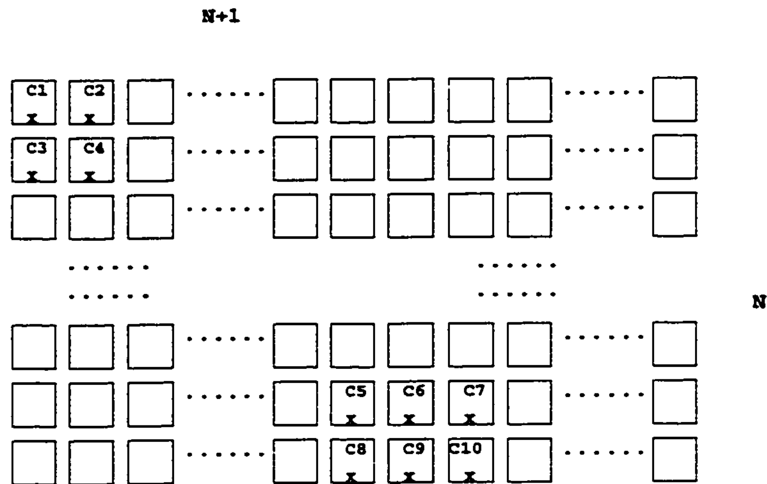
(7)**Pattern 7**: corresponding to the case where 10 cells that are shown in Figure B.7 are defective.

In this case, there must be one defective cell, C1 or C9, are not tolerable.

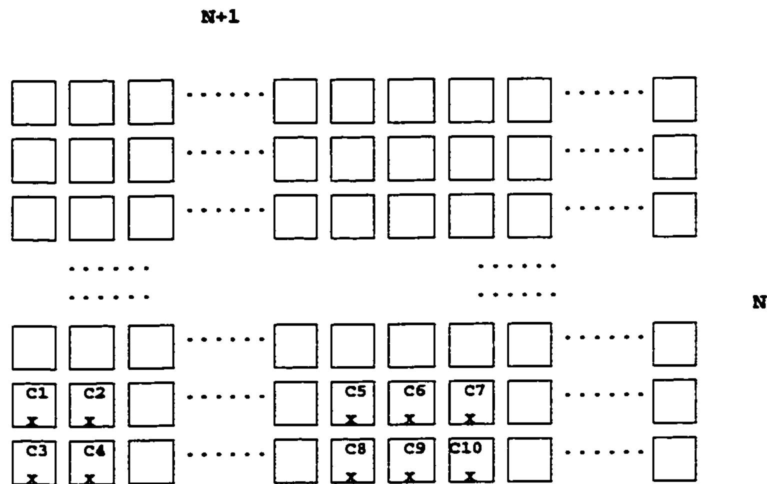
The equation for calculating the total number of this kinds of non-tolerable pattern is presented as the following:

For case (a): $NTC_{cell} = 2(N-1)\binom{(N+1)N-10}{F_c-10}$

For case (b): $NTC_{cell} = 2(N-2)\binom{(N+1)N-10}{F_c-10}$



(a)Four defective cells and the other six defective cells are not in the top or bottom rows simultaneously



(b)Ten defective cells are in the top or bottom rows simultaneously.

Figure B.7 Non-tolerable Pattern 7.

(8)**Pattern 8**: corresponding to the case where 12 cells that are in the position as shown in Figure B.8 are defective.

In this case, one defective cell, C6 or C7, can not be tolerated.

The equation for calculating the total number of this kind of patterns is expressed as follows:

$$NTC_{cell} = (N-2)(N-2)\binom{(N+1)N-12}{F_c-12}$$

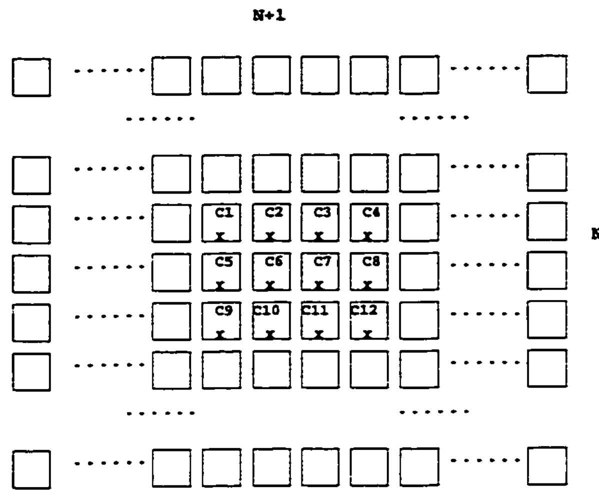


Figure B.8 Non-tolerable Pattern 8.

(9)**Pattern 9**: corresponding to the case where 12 cells that are in the position shown in Figure B.9 are defective.

In this case, due to the limit of the number of spare columns, there must be one defective cell, C2 or C10, cannot be tolerated.

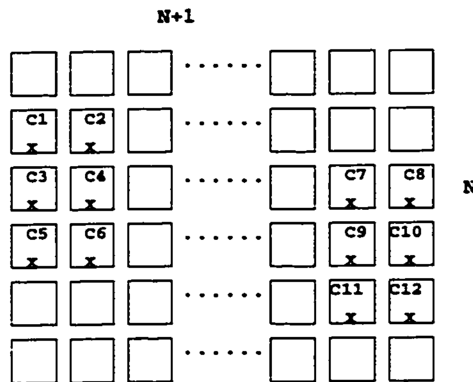


Figure B.9 Non-tolerable Pattern 9.

The equation for calculating the total number of this kind of patterns is presented as

$$NTC_{cell} = (N-2)^2\binom{(N+1)N-12}{F_c-12}$$

(10)**Pattern 10**: corresponding to the case where 12 cells in the top or bottom rows as shown in Figure B.10 are defective.

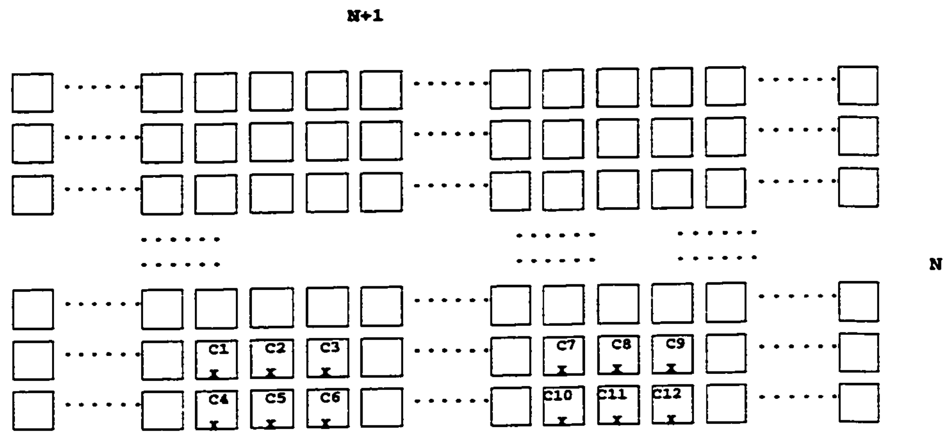


Figure B.10 Non-tolerable Pattern 10.

The equation for calculating the total number of this kind of patterns is

$$NTC_{cell} = (N-3)(N-4)\binom{(N+1)N-12}{F_c-12}$$

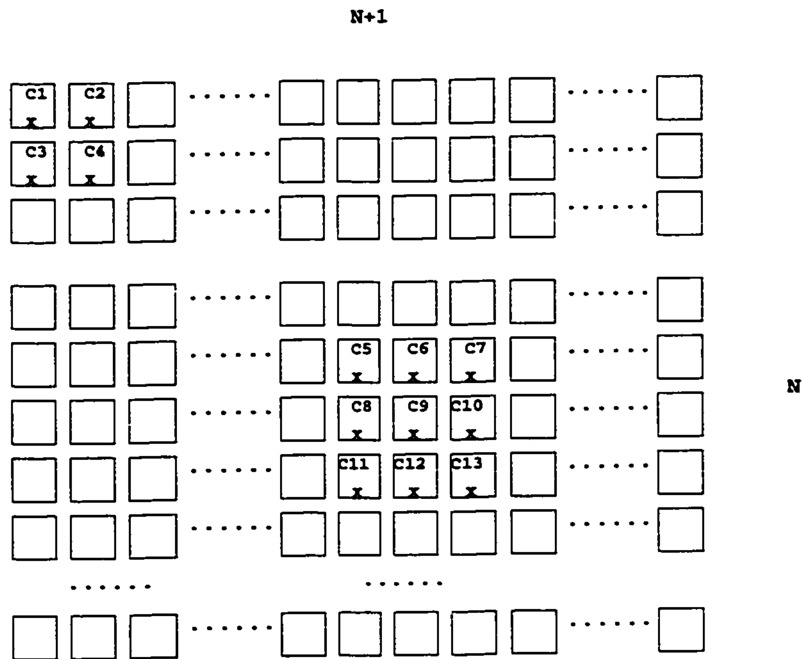


Figure B.11 Non-tolerable Pattern 11.

(11) **Pattern 11**: corresponding to the case where 13 cells shown in Figure B.11 are defective.

In this case, there must exit one defective cell, C1 or C9, that cannot be tolerated.

The equation for calculating the total number of Pattern 11 is presented as the following.

$$NTC_{cell} = \binom{4}{1}(N(N-3)+1)\binom{(N+1)N-13}{F_c-13}$$

(12)**Pattern 12**: corresponding to the case where 15 cells, of which six are in the edge position of the array as shown in Figure B.12, are defective.

In this case, there is at least one defective cell, C3 or C11, that cannot be tolerated.

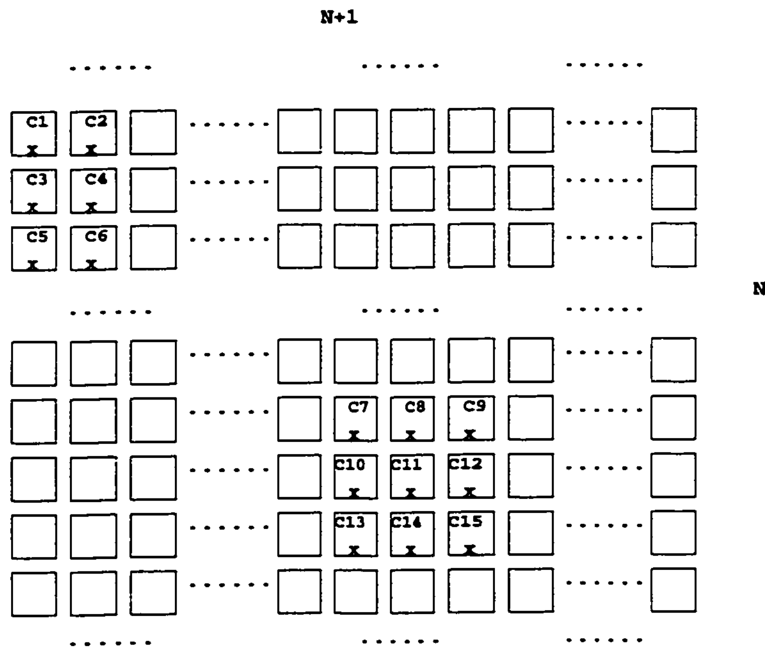


Figure B.12 Non-tolerable Pattern 12.

The equation for calculating the total number of this kind of pattern is presented as the following.

$$NTC_{cell} = ((N-4)(N-3)(N-1)+(N-2)(3N-8))\binom{(N+1)N-15}{F_c-15}$$

(13)**Pattern 13**: corresponding to the case where 18 cells shown in Figure B.13 are defective.

In this case, there must be at least one defective cell, C5 or C14, that are not tolerable.

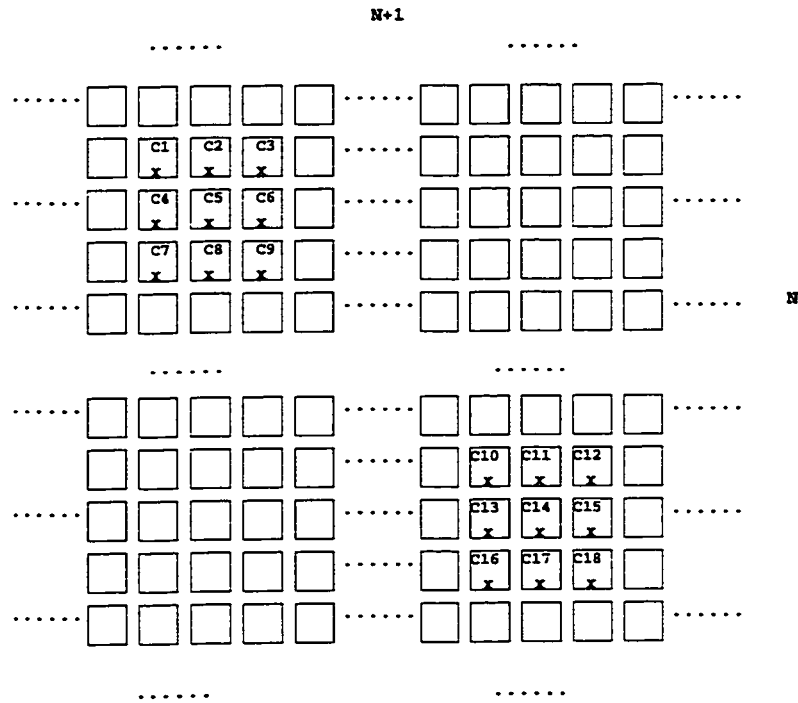


Figure B.13 Non-tolerable Pattern 13.

The equation for calculating the total number of this kind of pattern is presented as the following.

$$NTC_{cell} = \left((N-4)(N-3)(5N-16)/2 + (N-1)(N-2)\frac{(4N-22+(N-6)(N-7))}{2}\right)\binom{(N+1)N-18}{F_c-18}$$

Appendix C. Analytical proof related to the second most significant non-tolerable pattern

Analytically prove that the non-tolerable pattern, called Pattern M in this analysis, which corresponds to the case where two cell in a corner and one vertical bundle in the first row are defective, is the one which comprises smallest number of defective cells and bundles among the non-tolerable patterns that cannot be tolerated and comprise at least one defective cell.

A counterevidence method is used to prove this case. it is assumed that there exists a non-tolerable pattern that comprises less number of defective cells and bundles than Pattern M, i.e., the number of defective cells in this pattern must be 1 or 2 and the number of defective bundles is no more than one.

(1)A pattern comprising one defective cells and one defective vertical bundle.

Without loss of general, it is assumed that this pattern comprises one defective cell plus one defective vertical bundle: the defective cell is the cell P(i, j) with SC(i, j)=1, where $0 \le i \le N$ and $0 \le j \le (N-1)$, and the defective vertical bundle VB(k, l, k, l) with SVB(k, l)=1.

If $k = i$ and $j = l$, it means that the defective vertical bundle originally belongs to the cell $P(i, j)$. Evidently we can form a logical array of N x N by dropping the ith column as shown in Figure C.1.

If the defective vertical bundle does not belong to the defective cell, we can use the kth column containing the defective vertical bundle as a spare column. Then any good spare cell except the cell P(k, l) can be used to replace the defective cell P(i, j) with cell-shifting reconfiguration strategy. For example, using the spare cell P(k, h) with SC(k, h)=0. The cell shifting operation is presented as the following. First of all is the cell shifting in the

row direction. The corresponding change of bundles can be expressed as VB(k-1,h,k,h) and HB(k-1, h, k, h), VB(k-2, h, k-1, h) and HB(k-2, h, k-1, h),.....,VB(i, h, i-1, h) and HB(i, h, i-1, h). Then, the operation of cell shifting in the column direction is processed. The corresponding change of bundles is: VB(i, h+1, i, h) and HB(i, h+1, i, h),VB(i, h+2, i, h+1) and HB(i, h+2, i, h+1),....., VB(i, j, i, j-1) and HB(i, j, i, j-1). The process is shown in Figure C.2.

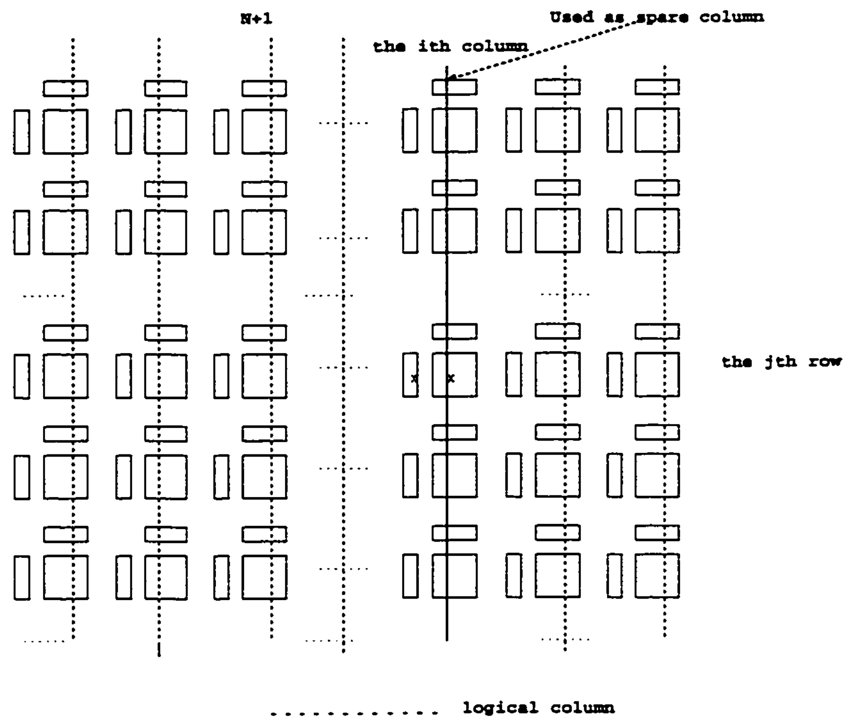


Figure C.1 Using column elimination strategy to form the logical array.

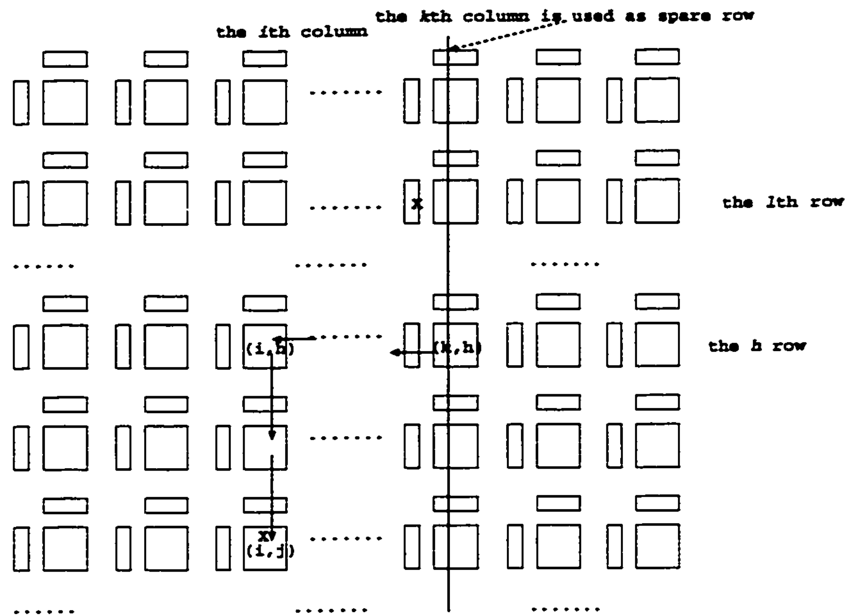


Figure C.2 Using the cell-shifting strategy to form the logical array.

Therefore, the pattern comprising one defective cell and one defective vertical bundle can be tolerated in this structure.

(2)A pattern comprising two defective cells and one defective vertical bundle.

Without loss of generality, it is assumed that two defective cells are: $P(i_1, j_1)$ with $SC(i_1, j_1)=1$ and $P(i_2, j_2)$ with $SC(i_2, j_2)=1$, and that one defective vertical bundle is: $VB(i_3, j_3, i_3, j_3)$ with $SC(i_3, j_3, i_3, j_3)=1$. There are several possibilities as follows:

(i)If $i_1=i_2=i_3$, they are in the same column. Under this condition, it is evident that this pattern can be tolerated;

(ii)If $i_3=i_1$ or $i_3= i_2$,but $i_1 \neq i_2$, the defective vertical bundle and one defective cell are in the same column. The i_3^{th} column can be used as a spare column. Any good cell in the spare column can replace the other defective cell by the same procedure as shown in Figure C.2. Thus, this kind of pattern can be tolerated as well;

(iii)If $i_1 \neq i_2 \neq i_3$, they belong to three different physical columns. There are two possible cases: One is that they belong to the same physical row. i.e., $j_1 = j_2 = j_3$. The column containing one defective cell or one defective vertical bundle can be used as a spare column. An example of tolerating these defects is shown in Figure C.3. Therefore, this pattern can be tolerated.

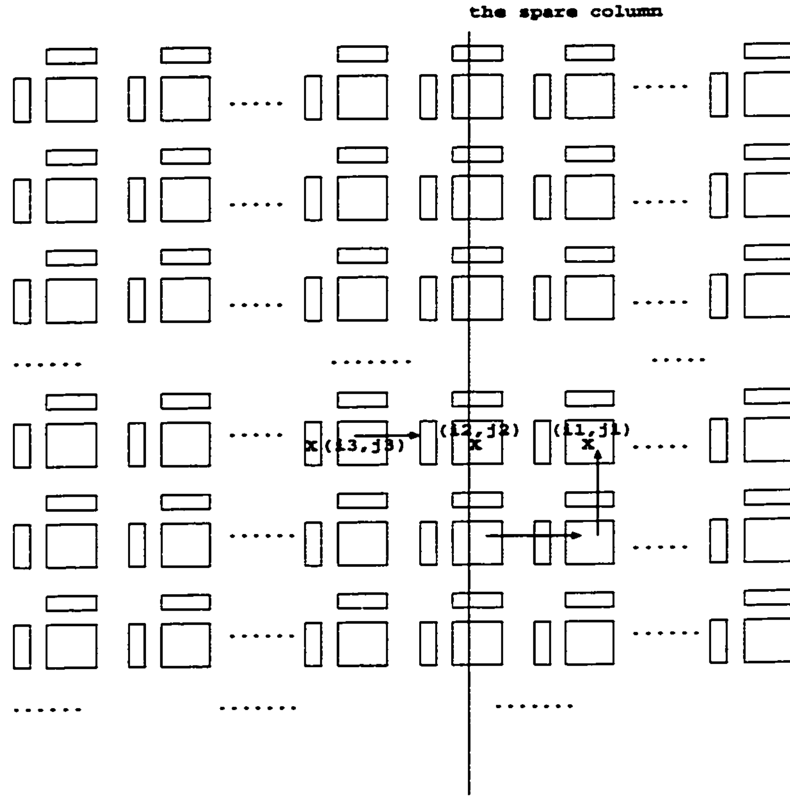


Figure C.3 Tolerating three defects by dropping a column containing one defects.

The other case is that they belong to different physical rows, i.e., $j_1 \neq j_2 \neq j_3$. An example of tolerating these defects is shown in Figure C.4. In this case, the i_2^{th} column is used as a spare column. Then, the good spare bundle VB(i_2, j_3, i_2, j_3) can be used to replace the defective bundle naturally owned by cell P(i_3,j_3) through bundle-shifting strategy, and defective cell P(i_1, j_1) can be replaced with the good spare cell P(i_2, j_1). Conclusively, the

pattern that comprises two defective cells and one defective vertical bundle can be tolerated.

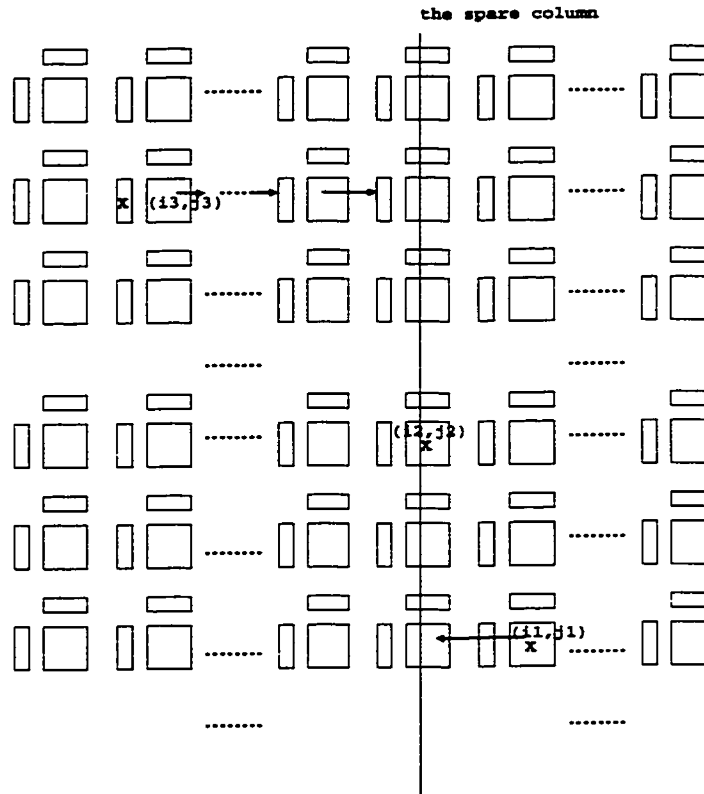


Figure C.4 An example of tolerating three defects that are not in the same physical row.

From the above analysis, the results is contradictory to the assumption that there is a pattern that comprise smaller number of defective cells and defective bundles than Pattern *M*. Therefore, among the non-tolerable patterns that comprise at least one defective cell and one defective bundle, the non-tolerable pattern, Pattern *M*, is the one that consists of smallest number of defective cells and bundles.

Appendix D. Derivation of the regression yield model

Figure D.1 shows the characteristic of the measured slope to the size of different array, but equivalent redundancy ratio. These measured slope is calculated from the points around the pivot point where the probability is equal to $1-e^{-1}$ in the complete yield curve. From the figure, it is observed that these curves can be approximated with straight lines. Therefore, it is assumed a linear function, $y = a_0 + a_1 x$, is used to fit these curves. Using the normal equation based on the method of least square [10], these curves can be fitted with three linear functions presented in the following:

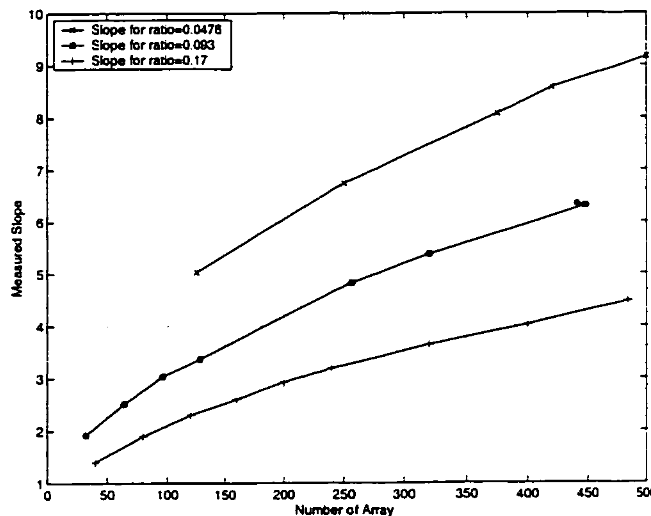


Figure D.1 Relationship in the measured slopes to the size of the array with the same spare ratio.

For the spare ratio equal to 0.0476

$$y = 3.82 + 0.0111x \tag{D.1}$$

For the spare ratio equal to 0.093

$$y = 1.92 + 0.0103x \tag{D.2}$$

For the spare ratio equal to 0.17

$$y = 1.37 + 0.00706x \tag{D.3}$$

Figure D.2 shows the curves of above functions. They agree with the measured data very well.

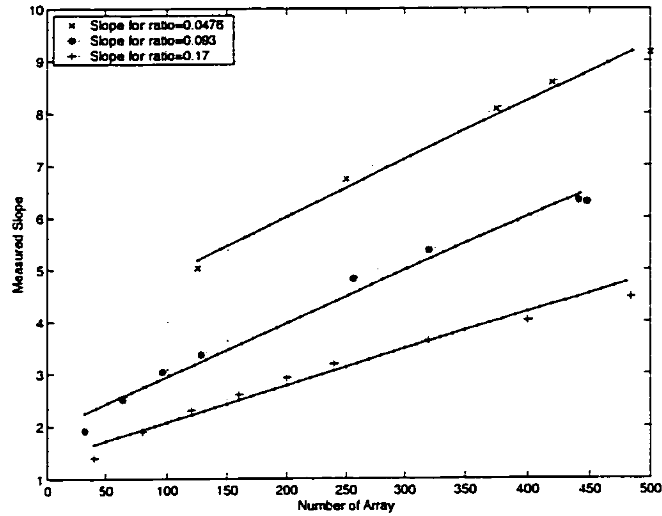


Figure D.2 Comparison between linear function and measured data.

With (D.1), (D.2) and (D.3), the slope $S(r,m)$ expressed with the spare ratio r and array size m, at the pivot point is approximated as (D.4)

$$S(r,m) = 0.3166r^{-0.8} + (0.0130 - 0.0337r)m \quad \text{(D.4)}$$

Where, r is the redundancy ratio of a physical array of K by L, and m is the number of cells in the physical array, i.e., m=KxL. In (D.4), the slope $S(r,m)$ is expressed in absolute value.

Similar to the above derivation, the defect density, D(r), where the probability is equal to $1\text{-}e^{-1}$, can be approximated with (D.5)

$$D(r) = -0.0208 + 4.3111r \quad \text{(D.5)}$$

Appendix E. Derivation of Y_{cell} with *Maxwell-Boltzman* combinatorial statistics

Without loss of generality, the procedure to derive P_{xF_c}, the part associated with cells in (4.14), is presented as the following.

Using the subscript "F_c" stead of "m" of (4.4), P_{xF_c} is given in (E.1).

$$P_{xF_c} = \frac{\left[\sum_{k=0}^{F_c}\binom{F_c}{k}(-1)^k(F_c-k)^x\right]}{Q_c^x},\ x \ge F_c \tag{E.1}$$

let $P_{xF_c} = 0$ if $x < F_c$. Then, it is given,

$$\sum_{x=0}^{\infty} P\{x\}P_{xF_c} = \sum_{x=0}^{\infty} \frac{\Gamma(x+\alpha)}{x!\Gamma(\alpha)} \frac{(Q_c\bar{\lambda}_c/\alpha)^x}{(1+Q_c\bar{\lambda}_c/\alpha)^{\alpha+x}} \sum_{k=0}^{F_c}\binom{F_c}{k}(-1)^k\left(\frac{F_c-k}{Q_c}\right)^x$$

$$= \sum_{k=0}^{F_c}\binom{F_c}{k}(-1)^k \sum_{x=0}^{\infty} \frac{\Gamma(x+\alpha)}{x!\Gamma(\alpha)} \frac{(Q_c\bar{\lambda}_c/\alpha)^x}{(1+Q_c\bar{\lambda}_c/\alpha)^{\alpha+x}}\left(\frac{F_c-k}{Q_c}\right)^x \tag{E.2}$$

To simplify (E.2), similar to [17][46], replace the gamma function with its definition $\Gamma(\alpha) = \int_0^{\infty} t^{\alpha-1}e^{-t}dt$, and let $b = \left(\frac{F_c-k}{Q_c}\right)$ and $\eta = \frac{Q_c\bar{\lambda}_c}{\alpha}$, (E.2) becomes,

$$\sum_{x=0}^{\infty} P\{x\}P_{xF_c} = \sum_{k=0}^{F_c}\binom{F_c}{k}(-1)^k \sum_{x=0}^{\infty} \frac{1}{\Gamma(\alpha)(1+\eta)^{\alpha}}\int_0^{\infty} t^{x+\alpha-1}e^{-t}\left(\frac{\eta^x b^x}{x!(1+\eta)^x}\right)dt \tag{E.3}$$

Let $\gamma = \frac{\eta b}{(1+\eta)}$, (E.3) is rewritten as the following.

$$\sum_{x=0}^{\infty} P\{x\}P_{xF_c} = \sum_{k=0}^{F_c}\binom{F_c}{k}(-1)^k \frac{1}{\Gamma(\alpha)(1+\eta)^{\alpha}}\int_0^{\infty}\left(\sum_{x=0}^{\infty}\frac{(\gamma t)^x}{x!}\right)t^{\alpha-1}e^{-t}dt$$

$$= \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \frac{1}{\Gamma(\alpha)(1+\eta)^{\alpha}} \int_0^{\infty} e^{\gamma t} t^{\alpha - 1} e^{-t} dt$$

$$= \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \frac{1}{\Gamma(\alpha)(1+\eta)^{\alpha}} \int_0^{\infty} t^{\alpha - 1} e^{-(1-\gamma)t} dt$$

$$= \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \frac{1}{\Gamma(\alpha)(1+\eta)^{\alpha}} \frac{\Gamma(\alpha)}{(1-\gamma)^{\alpha}} \tag{E.4}$$

Substituting γ with $\frac{\eta b}{(1+\eta)}$, b with $\left(\frac{F_c - k}{Q_c}\right)$, and η with $\frac{Q_c \bar{\lambda}_c}{\alpha}$ in (E.4):

$$\sum_{x=0}^{\infty} P\{x\} P_{xF_c} = \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \left(1 + \frac{(Q_c - F_c + k)\bar{\lambda}_c}{\alpha}\right)^{-\alpha} \tag{E.5}$$

Therefore, (E.5) can be rewritten as (E.6).

$$Y_{cell} = \sum_{F_c = 0}^{S_c} \binom{Q_c}{F_c} \sum_{k=0}^{F_c} \binom{F_c}{k} (-1)^k \left(1 + \frac{(Q_c - F_c + k)\bar{\lambda}_c}{\alpha}\right)^{-\alpha} \tag{E.6}$$

Appendix F. *Derivation of the formulas with Maxwell-Boltzman* statistics and *Bose-Einstein* statistics

F.1 Deduction of the formula by *Maxwell-Boltzman* statistics

This question can be solved as a mathematical occupancy problem of distinct balls distributed over a number of distinct boxes.

Question: How many ways are there to distribute *m* distinct balls into *n* distinct boxes with at least one ball in each box? ($m>n$)

Define the universe υ to be all ways to distribute *m* distinct balls into *n* distinct boxes. Denote by $A_i(i=1,2,\ldots,n)$ the set of distributing *m* distinct balls into *n* distinct boxes with a void in the ith box and $\overline{A_i}$ the complement set of A_i. Denote by N(S) the number of elements in set S. Then, there are $N(\overline{A}_1\overline{A}_2\overline{A}_3\overline{A}_4.\overline{A}_{n-1}\overline{A}_n)$ ways for this question. We have $N(\upsilon) = n^m$, $N(A_i) = (n-1)^m$, $N(A_iA_j) = (n-2)^m$ and $N(A_{i_1}A_{i_2}\ldots A_{i_k}) = (n-k)^m$. Denote $S_1 = \sum_{i=1}^{n} N(A_i)$, $S_2 = \sum_{i,j}^{n} N(A_iA_j)$ and S_k is the sum of the size of all k-tuple intersections of A_i's. It is evident that $S_1 = \binom{n}{1}(n-1)^m$, $S_2 = \binom{n}{2}(n-2)^m$ and $S_k = \binom{n}{k}(n-k)^m$. According to the principle of Inclusion-Exclusion[48], it is given,

$$N(\bar{A}_1\bar{A}_2\ldots\bar{A}_n) = N(\upsilon) - S_1 + S_2 - S_3 + \ldots + (-1)^k S_k + \ldots + (-1)^n S_n$$

Therefore, the number of all ways to distribute *m* distinct balls into *n* distinct boxes with at least one ball in each box is:

$$\sum_{k=0}^{n} (-1)^k \binom{n}{k} (n-k)^m$$

Similar to above, we can derive the formula of the ways to distribute all x defects into F_c cells so that each of these F_c cells has at least one defect. Assume that defects are distinguishable. Then, we have:

$$\sum_{k=0}^{F_c} (-1)^k \binom{F_c}{k} (F_c - k)^m$$

where, k: the number of cells that have no defects

F_c: the number of cells that are defective

F.2 Deduction of the formula by Bose-Einstein statistics:

This question can be solved as a mathematical occupancy problem of indistinguishable balls distributed over a number of distinct boxes

Question 1: How many ways are there to distribute *m* indistinguishable balls into *n* distinct boxes?

Distributing *m* balls into *n* boxes is similar to the process of dividing *m* balls into n parts. Arrange balls into a straight line and using (*n*-1) slashes to divide them into *n* parts as shown in Figure F.1

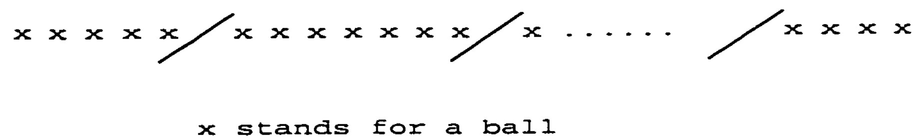


Figure F.1 Illustration of *m* balls being divided into *n* parts.

The x's before the first slash belong to the first box, and the x's between the first and second slash belong to the second box,..., and the x's after the $(n\text{-}1)^{th}$ slash belong to the nth box. The distribution problem becomes to select possible positions for (*n*-1) slash.

Because the situation of no ball in a box exists, there are total $(m+n-1)$ positions in this sequence. The answer is $\binom{m+n-1}{n-1}$.

Question 2: How many ways are there to distribute m indistinguishable balls into n distinct boxes with at least one ball in each box?

In this case, each box has at least one ball, so there are only $(m-1)$ positions, each between any two neighbor x's, to select for $(n-1)$ slashes. The answer is $\binom{m-1}{n-1}$.

From the above derivation, we can obtain the formula of the ways to distribute all x indistinguishable defects into F_c cells so that each of these F_c cells has at least one defect. It is presented as $\binom{x-1}{F_c-1}$. The number of all ways to distribute x indistinguishable defects into F_c cells can be expressed as $\binom{x+F_c-1}{x}$.