INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps.

ProQuest Information and Learning
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
800-521-0600

Modeling and Design of Parallel Regeneration Techniques for High-Speed SOC RLC Interconnects

Tawfeeq Lammoshi

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the requirements

for the degree of Master of Applied Science at

Concordia University

Montreal, Quebec, Canada

April 2003

Abstract

Modeling and Design of Parallel Regeneration Techniques for High-Speed SOC RLC Interconnects

By Tawfeeq Lammoshi

On-Chip inductance has become of significance in the design of high-speed interconnects. Repeaters are now widely used to enhance the performance of long On-Chip interconnects in CMOS SOC / VLSI. These repeaters are inserted in the interconnect according to a criterion. One example of criterion is to insert the repeaters so as to keep the signal driving capability uniform along the interconnect. While the size of the repeaters is kept constant, the length of the interconnect segments is increased when we move towards the interconnect end. This technique is called VSRT (Variable-Segment Regeneration Technique). Moreover, in order to calculate optimal design parameters, while saving a large numbers of electrical simulations, two models of the repeater are compared in this thesis: a transistor-based model and, a parallel-resistance RC-based model for which an analytical model was developed. The technology used in our experimentation is a 0.5 μm (Taiwan Semiconductor Manufacturing Company) TSMC technology, and the simulation was performed using HSPICE. The simulation results showed that our parallel-resistance RC-based VSRT gives accurate results. A software package was extracted from the analytical model to advice the designer on how to optimally set design parameters.

Acknowledgments

I would like to express my sincere gratitude to my supervisor, professor Mohamed Nekili for his excellent technical guidance during my graduate career, and his continuous concern for accuracy and completeness of the thesis.

I would like to thank my friend Falah R. Awwad for his valuable advice, his close collaboration, and his continuous support.

Sincere acknowledgments go to professor Ramachendran for his help with regard to the mathematical background in Chapter 4.

My thanks to the helpdesk group of technicians and in particular, Henry Kovalcik, Tadeusz Obuchwicz, and Wojciech Galuszka for their prompt response when technical support was needed.

Finally, I would like to express my deepest gratitude to my beloved family. Most important of all, I would like to thank my parents for their support, my three sons, my little daughter and my wife, Intsar, for her understanding and endless devotion. She is truly the wind beneath my wings.

Contents

List of Tables

List of Figures

CHAPTER 1

Introduction and Overview

1.1. Background

For late 1980 1.0 μm technology, the intrinsic switching delay of an unloaded MOSFET approaches 10 ps while the response time of a 1.0 mm interconnect is approximately 1 ps. But, for early 2000's 0.1 μm technology, the intrinsic delay of a MOSEFT decreases to about 1.0 ps while the response time of a 1.0 mm interconnect increases to 100 ps. Interconnect latency regresses from one decade faster to two decades slower than transistor delay. Since the propagation delay has a square dependence on the length of an RC interconnect wire, subdividing the wire into shorter sections is an effective strategy to reduce the total propagation delay. This can be done by inserting repeaters, which breaks the quadratic dependence of the delay on the interconnect length but adds additional parasitic capacitance due to the inserted repeaters. By including inductance in the repeater insertion methodology, the interconnect is modeled more accurately as compared to an RC model permitting average saving in area, power, and delay, for a variety of interconnect trees from a 0.5 micron CMOS technology.

1.2. Previous Work

This thesis is based on a previous work performed by Awwad and Nekili in [34], who presented an optimum method for regenerating RLC interconnects using parallel repeaters which were introduced by Nekili and Savaria [27]. The main criterion in [34] is based on

ensuring the signal driving capability is uniform along the interconnect. As a result, the size of repeaters is kept constant throughout the interconnect, and the segment length is increased as we move towards the interconnect end. This method was called Variable-Segment Regeneration Technique (VSRT). Awwad and Nekili modeled the repeaters as a gate capacitance and the resistance of the pull-down transistor in series with the interconnect. However, this type of modeling suffers from a number of weaknesses. Indeed, in such a case, the signal driving capability decreases with the distance from the interconnect input while it is, in reality, increasing because of the additional driving capability added by inserting repeaters.

1.3 Methodology of the thesis

Assuming a uniform signal driving capability along the interconnect, and in order to overcome the weaknesses of the previous work, this thesis models the repeater resistance in parallel with the interconnect.

As a consequence, unlike the previous work, building an analytical model for the whole interconnect does unfortunately not reduce to a simple application of the basic theory developed by Kahng and Muddu [21]. Therefore, in this thesis, we had to build the analytical model form scratch by writing the transfer function in the s-domain. Also, as there are N interconnect segments (each with 3 passive elements) and N repeaters (each with 2 electrical parameters), the overall solution involves an intensive calculation of coefficient because, unlike previous Elmore delay models for RC interconnects, to capture the inductance effects, one has to consider two moments in the transfer function instead of one. Given this modeling, called parallel-resistance RC-based repeater VSRT, the problem can be formulated as follows:

Given:

-an interconnect length (e.g., 10 cm),

-an interconnect width(e.g., 0.9 μm), and

- a fabrication technology,

assuming the repeater size is constant along the interconnect, determine the design parameters N and l_1 (length of the first segment) and δ (the length increase between two consecutive segments) so that the total propagation delay is minimized.

Note that, because of the precharge mechanism involved in this method, the only propagation considered is that of a logical '0', as the propagation of a logical '1' requires zero delay. For the sake of simplicity and illustration in this thesis, l_1, and δ are kept constant thus only N is determined. In order to save the time needed for simulating the overall interconnect with repeaters for every value of N, our analytical model can be used by the designer (through Java language and Matlab) to plot the function of propagation delay versus the design parameter N and the designer can visually inspect the optimum on the curve.

1.4. Organization of the thesis

This thesis is organized as follows. Chapter 2 reviews the literature addressing the design and modeling of RLC interconnects. Chapter 3 compares the delay performance of both:

-a VSRT where the repeaters are modeled as transistors, and

-a VSRT where the repeaters are modeled as a gate capacitance with a pull-down transistor resistance in parallel with the interconnect in order to check the accuracy of our method.

To achieve this comparison HSPICE simulations are used with a 0.5 μm TSMC (Taiwan Semiconductor Manufacturing Company) fabrication technology. Chapter 4 presents an

analytical model which allows the designer to determine optimum parameters without going through time-consuming simulations for all the design parameters involved. Possible future work is addressed in Chapter 5.

Chapter 2

Importance of On-Chip Inductance in Designing RLC VLSI Interconnects

2.1. Introduction

As modern VLSI technology moves into a very deep submicrometer (VDSM) regime, millions of transistors will be integrated onto a single chip, operating at frequencies greater than Giga-Hertz. The die size is expected to increase from 385 mm^2 in 2001 to 620 mm^2 by 2009, while average on-chip currents will increase from 70 Amperes in 2001 to 190 Amperes. Power distribution networks in highly complex CMOS integrated circuits will achieve this. These circuits must be able to provide sufficient current to support average and peak power demand within all parts of an integrated circuit. The large chip dimensions and average currents require special design strategies to maintain a constant voltage supply within a power distribution network. The voltage supply is expected to decrease from 1.5 volts in 2001 to 0.9 volts by 2009, reducing the tolerance to voltage changes within a power distribution network. With each technology generation, the requirements placed on the on-chip power and ground distribution networks increase. The stricter specifications are due to justify shorter rise times, smaller noise margins, higher current, and increased current densities. The higher speed switching of smaller transistors produce faster current transients in the power distribution network. The higher currents cause large Ohms IR voltage drops while fast current transients cause large inductive L di/dt voltage

drops (ΔI noise). The power distribution networks are typically designed to minimize these current transients, maintaining the local supply voltage within specified design margins. With transistor switching as low as few Picoseconds, the on-chip signals typically contain significant harmonics at frequencies as gigh as 100 GHz. For on-chip wires, the inductive reactance ωL dominates the overall wire impedance beyond ~ 10 GHz [1]. Currently, RC models are used for high-resistance nets and capacitive models are used for less resistive interconnects. However, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Furthermore, performance requirements are pushing manufacturers to create new materials with low-resistance interconnects. Inductances are, therefore, becoming an integral element in VLSI design methodologies [2].

The reader is referred to [39] for a complement of details.

2.2. Problems Associated with On-Chip Inductance

The absence of reliable practical understanding of the related inductive effects and the insufficient sophistication of the tools and methods that are used in designing and analyzing the high performance ICs are the reasons for the problems that arise when dealing with on-chip inductance. The problems that must be considered are as follows:

1. The essential of efficient extraction methods when dealing with on-chip inductance.

2. On-chip inductance would increase the processing time of CAD tools, which are used in simulation and design.

3. Signal reliability problems and the increase of noise in ICs are some drawback effects of the underdamped response that results from including On-Chip inductance.

2.3. Characteristics of On-Chip inductance

Ismail and Friedman [3] reported that two characteristics of On-Chip inductance can be exploited to simplify the extraction process of on-chip inductance. These two characteristics are as follows:

1. The response level of a signal waveform to errors in the inductance values is low, particularly the propagation delay and rise time.

2. The value of the On-Chip inductance is slow varying with respect to the width of the wire and the geometry of the surrounding wires.

2.4. Useful Inductance Effects

We have studied the effects of inductive interconnects on the propagation delay, repeater insertion and power dissipation. The following subsections illustrate these positive effects.

A number of publications have proposed criteria for whether or not inductive effects are important; they essentially boil down to whether or not the signal near-end rise time is much faster than the propagation velocity down the wire, and whether the attenuation constant ($Z_o/2R_{wire}$) is greater than one. The internal propagation delay on the interconnection grows as the square of their length thus leading to a speed reduction with length increase. With the scaling of technology and increased chip sizes the cross-sectional area of wires has been increased. Therefore, the resistance of the interconnect has increased in significance. Currently, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks, data busses, and upper metal layers. These wires are low resistance lines that can

exhibit significant inductive effects. The inductance leads to faster signal rise times, lower power consumption, and less active device area. Design methodologies can be developed to exploit these useful effects of On-Chip inductance while maintaining noise at acceptable levels, so as to guarantee the reliable performance of an integrated circuit. The following subsections briefly explain these beneficial effects of inductance on the performance of integrated circuits.

2.4.1 Effects of Inductance on the Signal Rise Time

Ismail [4] showed that the inductance effects increase the propagation delay along an RLC interconnect, maintaining the high frequency components in the edges, and that improves the signal rise and fall times. Thus, On-Chip inductance improves the signal slew rate. In the limiting case of lossless line representing maximum inductance effects, the attenuation constant α is zero and the propagation speed becomes frequency independent and the speed can be defined as

$$v = \frac{1}{\sqrt{LC}}$$

2.4.2 Effects of Inductance on the Propagation Delay

Kahng and Muddu [5] and Ismail and Friedman [4] presented different closed-form expressions for the propagation delay of a gate driving a distributed RLC interconnect. Ismail and Friedman [4] found that the delay expression is within 5% of a dynamic circuit simulation for a wide range of RLC loads. They showed that the error in the propagation delay, if inductance is neglected and interconnect is treated as a distributed RC line, can be

over 35% for current On-Chip interconnects.

2.4.3. Effects of Inductance on the Repeater Insertion Process

Repeater insertion is becoming an increasingly common design methodology for driving long resistive interconnects. Ismail and Friedman [6] proved that, as the inductance effects increase, both the number of repeaters and the size of each repeater decrease. This trend means significantly less repeater area and power consumption due to decreased repeater capacitance. In addition, including inductance within the interconnect model will reduce the number of inserted repeaters. Hence, this will simplify the layout and routing constraints.

2.4.4. Effects of Inductance on Power Dissipation

Power consumption is an increasingly important design parameter with mobile and high performance systems. If the frequency of switching is f cycles per second then the dynamic power consumption is given by

$$P_{avg} = C_t V_{DD}^2 f$$

where C_t is the total interconnect capacitance and V_{DD} is the power supply.

Increasing inductance effects results in less number of repeaters as well as a smaller repeater size, which significantly reduces the total capacitance of the repeater and the total dynamic power consumption.

2.4.5. Effects of Self and Mutual Inductances

Masud et al. [7] presented the estimation of the circuit behavior such as propagation delay, oscillation, overshoots in the presence of self and mutual inductance, and a set of simple

closed-form expressions. They found that their results were fairly close to simulation data (within 15% of AS/X simulations) and can be evaluated in a time comparable to Elmore delay. They showed that the following equation allowed calculating all the moments.

$V_{inp}(s) = \frac{m_{0,inp}}{s} + m_{1,inp} + m_{2,inp}s + m_{3,inp}s^2$, where V_i is the input voltage, $m_{0,i}$ are the moments in the s-domain.

2.5. Moment Matching

Of particular interest is the class of moment matching approaches, which provide acceptable accuracy without sacrificing computational efficiency. Examples of this approach include the following:

1. Horowitz [8] proposed a method for estimating the delay through RC trees using both single-pole and two-pole methods: he calculated the poles of the estimated system response from the first and second moments of the main path(i.e., the unique path from the input node to the output node) in the RC trees. His paper with Rubinstein et al. [9] points out that for delay analysis of RC tree, each distributed RC wire should be replaced by a finite number of lumped RC segments to achieve the required accuracy.

2. Zhou et al. [10] considered the polynomial describing the poles of a distributed transmission wire that is modeled as a single RLC segment driving a small capacitive load. Based on this model, the voltage response in a general interconnection tree is computed from the two dominant poles. To achieve improved accuracy, the authors of [10] propose modeling each tree branch by many shorter segments (but this deviates from the underlying assumptions in that not every branch of the tree drives the small capacitive load).

3. McCormick [11] also proposed a general technique for approximating the time-domain response of a system from its moment representation, using basic waveforms, which are linear, exponentially decaying, underdamped decaying, etc. This method of obtaining

waveforms whose moments match those of interest can be used instead of the more traditional two-pole techniques in [8] [12].

From the recent literature, it is clear that moment-matching methods have become increasingly attractive due to their combined efficiency and accuracy.

2.6. RLC Interconnect Delay Models

Although RC models are widely used, the trend of shrinking feature size in IC design shows that the scaling-down of wire width will increase both the wire resistance and inductance. As the switching speed and operating frequency increase, the inductive effect of metal interconnect wires becomes important and must be taken into consideration in the timing simulation. Under these circumstances, the interconnects must be modeled as RLC devices instead of RC components. As VLSI design reaches deep submicron technology, the delay model used to estimate interconnects delay in interconnect design has evolved from the simplistic capacitive model to the sophisticated high-order moment matching delay model [13]. Whenever inductance is considered to be negligible, the RC model can be viewed as a limiting case of the RLC transmission wire model. The other limiting case is an inductance-capacitance (LC) transmission wire where the resistance is negligible. Although it is highly improbable that the resistance of On-Chip interconnect will become negligible in the near term, this LC analysis provides an upper limit for analyzing inductive effects in VLSI circuits. Analyzing the behavior of the RC and LC case therefore bound the behavior of an RLC transmission wire case. Various techniques have been proposed for the delay analysis of interconnects. These techniques are based on either one of the following:

A- Simulation techniques such as SPICE tool. Such techniques give the most accurate insight into arbitrary interconnect structures but are computationally expensive. Also, transient simulation methods of lossy interconnects based on convolution techniques were presented in [14].

B- Closed-form analytical formulas: These are faster techniques based on moment computations that were proposed in [15]. These methods are too expensive to be used during iterative layout optimization. Therefore, designers began to use the Elmore delay model [16] in the performance-driven design of clock distribution and Steiner global routing topologies. In the following subsections, we present some of the delay models, which were developed for RC, and RLC interconnects.

2.6.1. Elmore Delay for RLC interconnects

Elmore delay approximation represents the first moment of the transfer function. Despite not being highly accurate, the Elmore delay is widely used by industry for fast delay estimation. With ICs composed of tens of millions of gates, it is often impractical to use highly accurate time consuming methods to evaluate the delay at each node in the circuit. The Elmore delay is therefore used to quickly estimate the relative delays of different paths in the circuit, permitting more exhaustive simulations to be performed for only the critical paths. Also, Elmore delay is widely used as a delay model for the synthesis of VLSI circuits such as buffer insertion in RC trees and wire sizing [17]. The main reasons for the wide use of the Elmore delays as a basis for design methodologies are:

A- The Elmore delay has a high degree of fidelity. An optimal or near-optimal solution achieved by a design methodology based on the Elmore delay is also near optimal based on more accurate delay (e.g. SPICE-computed [18]) for routing constructions [19] and

wire sizing optimization [17]. Simulations [20] have shown that the clock skew derived under the Elmore delay model has a high correlation with SPICE-derived skew data [2].

B- The existence of a simple tractable formula for the delay [21] that has recursive properties [22], makes the calculation of the circuit delays highly sufficient even in large circuits. Unfortunately, Elmore delay cannot accurately estimate the delay for RLC interconnect and trees. i.e., the representation for interconnects whose inductive impedance cannot be neglected [23]. This is primarily due to the fact that Elmore delay is not over non-monotonic responses [16], which can occur in RLC circuits [2]. This inaccuracy of Elmore delay is harmful to current performance-driven routing methods, which try to optimize interconnect segment lengths and widths as well as driver and buffer sizes. Previous moment-based approaches compute the delay estimates only from simulated response but not from an analytical formula as in [23].

2.6.2. Asymptotic Waveform Evaluation (AWE) Delay Model

Asymptotic Waveform Evaluation (AWE) was published for an approximation of the waveform response of general linear lumped circuits. Pillag, and Roher [22] showed that (AWE)-based algorithms have gained popularity as a more accurate delay model as compared to the Elmore delay model. AWE and its extensions are the most well-known methods to approximate general linear networks using moment-matching techniques to determine a set of low frequency dominant poles that approximates the transient response at the nodes of an RLC tree. However, AWE suffers two primary problems. The first problem is that this method can lead to an approximation with unstable poles even for low-order approximation. The second problem is that AWE becomes numerically unstable for higher order approximations which limits the order of approximations to less than approximately eight poles. This limited number of poles is inappropriate for evaluating the tran-

sient response of an under damped RLC tree, which requires a much greater number of poles to accurately capture the transient response at all the nodes. To overcome this limitation, a set of model order reduction algorithms has been developed to determine higher order approximations appropriate for RLC circuits based on the state space representation of an RLC network.

2.6.3. Zhou et al. Method

Since the above-mentioned single-pole delay estimate cannot accurately estimate the delay for RLC interconnects, Zhou et al. [13] proposed a two-pole approximation for the transfer function to compute the response at the load for RLC interconnect trees. However, the response computation does not provide any analytical expression for delay. It is also time consuming to be used in iterative optimization of layout.

2.6.4. Krater et al. Delay Model.

In 1995, Krauter et al. [23] proposed to improve the Elmore delay model by using higher order moments; this work led to a heuristic net delay model equal to the sum of the first moment (M_1) and its standard deviation.

2.6.5. Kahng and Muddu Analytical Delay Model.

Kahng and Muddu [24] used the Krauater et al [23]. delay model. However, they realized that it is not accurate for various sources and load parameters. They studied various combinations of first and second moments, from which they have developed their first delay analytical model of RLC interconnects [23], incorporating inductance effects while

assuming step input. The solutions developed by Kahng and Muddu [24] are composed of three different formulas for the cases of real, complex, and multiple poles. At that time, there were no closed-form solutions for the moments of a tree that can be directly incorporated into the delay mode. They showed that Elmore delay estimates could be as much as 50% from the SPICE-computed delays, while their proposed analytical delay model estimates are within 15% of the SPICE delay. They have also extended their delay model to estimate source-sink delays in arbitrary interconnect trees.

2.6.6. Ismail et al. Analytical Melay Model.

Ismail et al. [2] introduced a simple tractable delay formula for RLC trees. In fact, they tried to preserve the useful characteristics of the inductance effects. This delay model with the closed-form expressions considers all damping conditions of an RLC circuit including the under damped response, which was not considered by the Elmore delay due to the non-monotonic nature of the response. These solutions are presented for the 50% delay, rise time, overshoots, and settling time of signals in an RLC tree. Their generated delay expressions for an RLC tree have the same accuracy characteristics as the Elmore's [14] approximation for an RLC tree. These expressions consider both monotonic and non-monotonic signal responses. Due to this continuity, this delay model [2] is claimed to be, first, always stable and used with arbitrary inputs. Second, it is computationally efficient since the number of multiplication operations required to evaluate the approximation at all of the nodes of an RLC tree is linearly proportional to the number of branches in the tree.

2.7. Optimal Repeater Insertion.

The long delay and low bandwidth of the global wires clearly indicates a problem caused by the large resistance of these wires. Fortunately, there is a simple way to dramatically reduce the effect this resistance has on circuit performance which is to break these long wires into a number of shorter segments by adding gain stages between the segments. These stages are called repeaters. Regular insertion of repeaters into the interconnect avoids dependence of delay and wire length. Optimal spacing between repeaters is obtained when the delay throughout a repeater equals that of its wire segment [27]. Basically, two works are related to the regeneration of RLC interconnects. The first work was proposed by Ismail and Friedman [26]. They used the conventional serial technique for the repeater; while the second work was introduced by Awwad and Nekili [28] who looked at various repeater configurations for driving the RLC interconnect. Awwad and Nekili [28] used three techniques to regenerate an RLC interconnect in series, in parallel and without regeneration. They showed that the parallel regeneration starts achieving a better speed than the non-regenerated line at wire lengths smaller than that achieved when the wire is serially regenerated. It also featured a 47% time delay saving and a 96% area-delay product saving over the serial regeneration. They concluded with the need for parallel regeneration techniques to be used in RLC interconnects over the commonly used serial regeneration techniques. The third work was proposed by Awwad and Nekili [31], where they applied a variable-driver parallel regeneration technique to regenerate RLC interconnects. This technique was used by Nekili and Savaria [27] to regenerate RC interconnects. Secareanu and Friedman [30] proposed a High-Driver Transparent Repeater (HDTR) to drive highly capacitive RC interconnects with specific characteristics. They [31] applied some analog techniques such as differential mode rejection and a differential redundant

circuit architecture to the HDR, which led to higher speed, and higher noise immunity, thus introducing an HDR buffer circuit with improved noise HDRN. Awwad and Nekili [34] used the High-Driver Transparent Repeater (HDTR) to drive RLC interconnects. They showed that, the variable- driver parallel regeneration technique features 62% time delay saving and 315% area-delay product saving over the High Drive Transparent Repeater. In addition, they introduced the Variable-Segment Regeneration Technique (VSRT) to regenerate RLC interconnects. They proved that the new technique is the most preferment in terms of area-delay products among all known regeneration techniques.

Chapter 3

Accuracy Measurement of

the Parallel-Resistance RC-based Repeater VSRT

3.1. Introduction

The speed of On-Chip circuits with nowadays miniaturized devices and high levels of integration is so high, that high speed is an essential part of the total delay in processing units comes from the time needed for a signal to travel from one chip to another and from one part to another part inside the chip.

Signal velocities on integrated circuits are far less limited by the speed of light than by the resistance and capacitance of the wire. It is not possible to build good transmission wires on a chip and that is because the sensitivity of integrated circuit wires is high. Instead, On-Chip signal wires are lossy transmission wires with a delay proportional to the square of their length.

Historically, the main issue that determined the delay at each node of a MOS structure is the product of the parasitic capacitance by the resistance. Regular insertion of repeaters on the interconnect wire, as shown in Figure 3.1, avoids delay and wire length dependence. Ideal spacing between repeaters is obtained when the delay through a repeater is equal to the wire segment it drives.

In the last few years, technological advances made On-Chip interconnect inductance to be of significant especially with the usage of new low resistance materials in making interconnect wires, in addition to the discovery of new dielectrics which contributes in reduc-

ing the interconnect capacitance. In addition, using higher operation frequencies, fast-rise time signals and longer wires are contributes in increasing the importance of inductance as well.

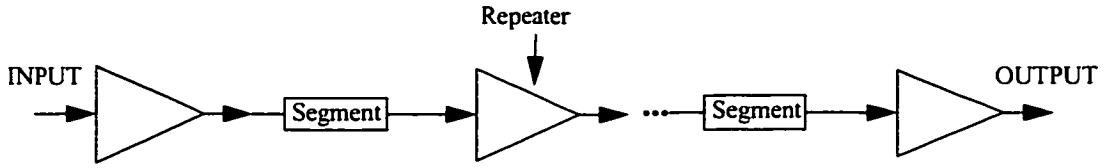

Figure 3.1 Driving an RLC wire with regularly inserted repeaters

The rest of this chapter is structured as follows. Section 3.2 reviews the previous modeling of the parallel repeater. Section 3.3 introduces a parallel for the repeater as opposed to the serial model. And finally, sections 3.4 presents simulation results and conclusion.

3.2 Modeling of the Parallel Repeater

To model the parallel repeater, Awwad and Nekili [34] applied a methodology which was presented by Kahng and Muddu [24]. To our knowledge, they were the first to present an analytical model of the parallel regeneration technique as mentioned earlier in Chapter 1. The basic circuit Figure 3.2 that led to this structure was originally proposed for the design of fast adders by Glasser and Dobberpuhl [38]. In a first step, this circuit was used by Nekili and Savaria [27] to regenerate RC interconnects, which allows an enhancement of performances compared to conventional methods. In a second step, this parallel repeater, shown in Figure 3.2, was used by Awwad and Nekili [31] to drive RLC interconnects.

Figure 3.2 shows the basic circuit of a parallel repeater. In this chapter, this circuit is used to drive an interconnect where inductance is significant. The network shown in Figure 3.2 is an arbitrary pass gate network. A p type transistor P_1 is used to pre-charge the wire(pre-charge phase). A logic level "0" generated from the network will discharge the wire in the

evaluation phase. A transistor N_3 mounted in parallel with the wire can accelerate the discharge as soon as a sense gate detects this transition. Since the discharging transistor has to be activated by the falling transitions on the wire, it must be related to the wire through an inverter. This configuration needs a precharging dynamic logic which is also required in the rest of the system and does not imply any time overhead. Moreover, the transistor-based model of Figure 3.2 adds no delay to the wire if inserted at regular intervals in parallel with the wire interconnects.

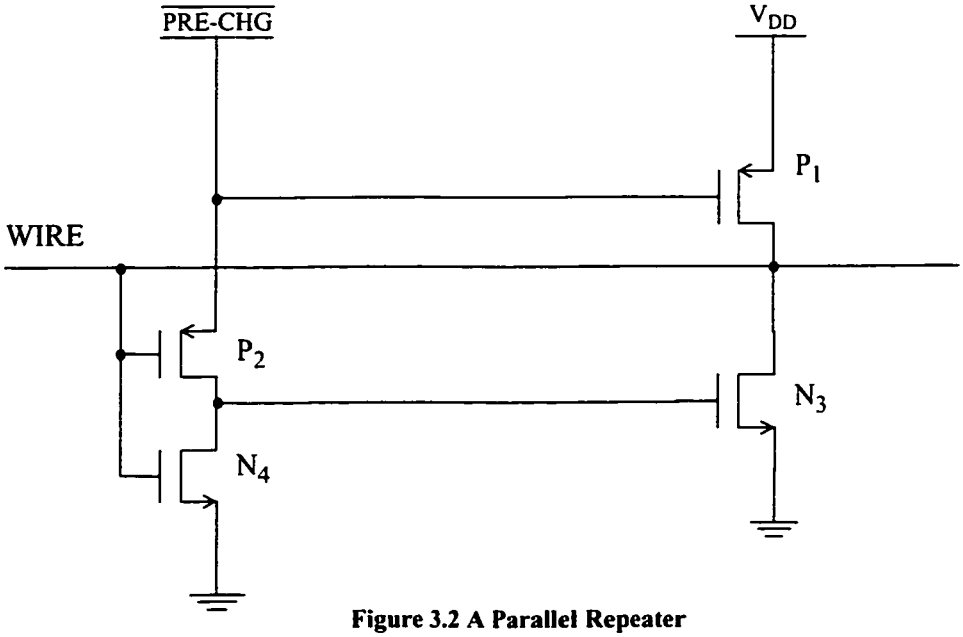

Figure 3.2 A Parallel Repeater

Awwad and Nekili [34] have modeled the parallel repeater using an inverter driving an NMOS3 (N_3) transistor, as shown in Figure 3.3.

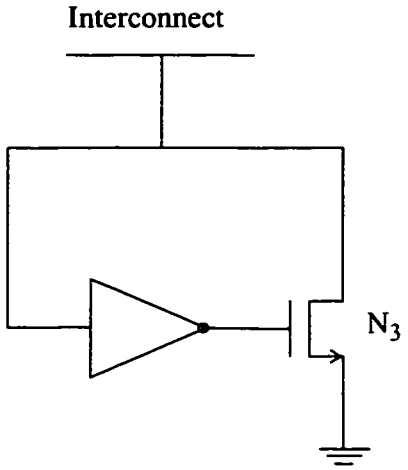

Figure 3.3 Simplified form of the parallel repeater

Then, they modeled the circuit of Figure 3.3 as an RC time constant (Figure 3.4), which they used a serial resistance with the wire to represent the drain-source resistance of the transistor N_3. This way of modeling was adopted previously by Dally[37] for serial repeaters.

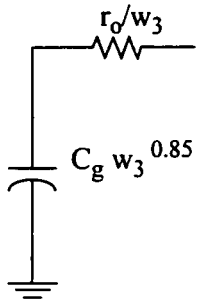

Figure 3.4 RC simplified model of the parallel repeater

The capacitance, in Figure 3.4, represents the parasitic gate capacitance of the driving inverter, which has a driving capability controlled by PMOS2 (P_2) that has a width of

$W_2=W_3^{0.85}$, in [31], the value of this capacitance is $w_2 C_g = w_3^{0.85} C_g$ is the gate parasitic capacitance of a minimum-size inverter. The in-series resistance is r_o/w_3, which represents the output impedance of NMOS3 transistor that pulls the interconnect down to V_{ss}. Note that r_o represents the output impedance of a minimum-size inverter.

In spite of its significant accuracy, modeling in-series the repeater resistance does not account for the interaction of the inserted repeaters and keeps this resistance effect local. Indeed, it does not reflect how the driving capabilities of the inserted repeaters combine along the interconnect. With this serial model, the signal driving capability decreases with distance from the input of the interconnect. Instead of increasing, as would be expected because of the parallel nature of the repeater.

3.3 Introducing a Parallel Model for the Repeater

The parallel regeneration shown in Figure 3.2, used by Awwad and Nekili [34] within their Variable-Segment Regeneration Technique (VSRT), can be simplified using the small signal ac-model shown in Figure 3.5.

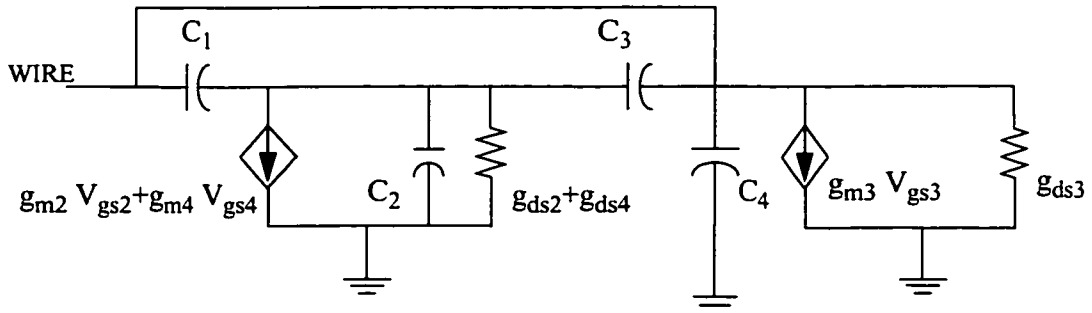

Figure 3.5 Small signal ac-model of the parallel repeater

where,

V_{gsi} is the gate-source voltage of the ith transistor,

g_{mi} is the transconductance of the ith transistor,

g_{dsi} is the drain-source conductance of the ith transistor,

$C_1 = C_{gs2} + C_{gd2} + C_{gs4} + C_{gb4}$

$C_2 = C_{db2} + C_{db4}$

$C_3 = C_{gs3} + C_{gb3} + C_{gd3}$

$C_4 = C_{db3}$

where C_{gsi} is the parasitic gate-source capacitance of the ith transistor,

C_{gdi} is the parasitic gate-drain capacitance of the ith transistor,

C_{gbi} is the parasitic gate-bulk capacitance of the ith transistor,

C_{dbi} is the parasitic drain-bulk capacitance of the ith transistor,

The inverter shown in Figure 3.5 can be simplified into two parallel components which are C_4 and g_{ds3} (Figure 3.6).

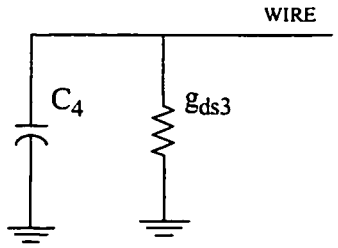

Figure 3.6 Parallel RC-based simplified model of the repeater

Figure 3.7 shows that PRT repeaters are placed between the VSRT segments to regenerate the signal along the wire, which was proposed by Nekili et al.[31] to regenerate RC interconnects and used here to regenerate RLC interconnects; the interconnected VSRTs. Here, the PRT repeaters represent transistors as opposed to passive elements.

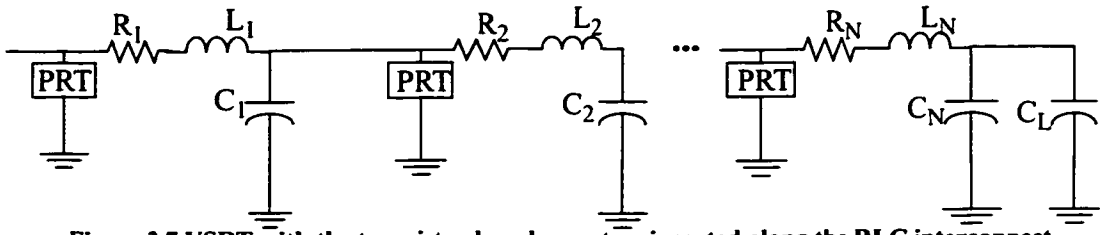

Figure 3.7 VSRT with the transistor-based repeaters inserted along the RLC interconnect

Figure 3.8, shown below, is similar to Figure 3.7 with the exception that the PRT repeaters can be replaced by parallel RC equivalent models; in other words, shunt resistances.

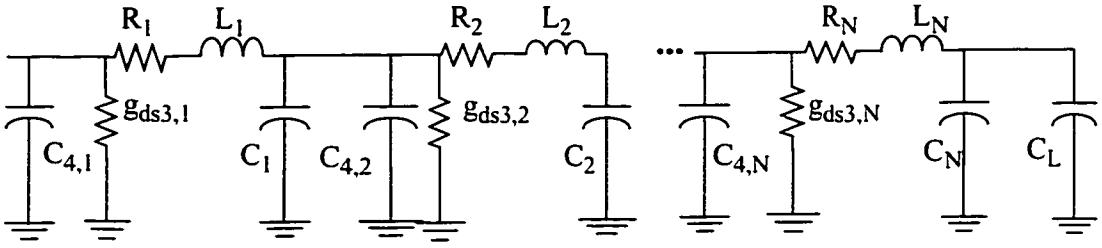

Figure 3.8 VSRT with the parallel RC model of the repeaters inserted along the RLC interconnect

3.4. Simulation Results and Conclusion

For the purpose of simulation, we are using Figure 3.8 with our parallel modeling of the PRT repeater resistance. The same value is used for all the parameters in the circuits of Figures 3.7 & 3.8, where $C_{4,i}$ and $g_{ds3,i}$ are the drain-bulk parasitic capacitance and the drain-source conductance, respectively, of the NMOS transistor N_3 in the ith segment of the wire. Also, C_L is the load capacitance of the interconnect in Figure 3.8. The technology used in our experimentation is a 0.5 μm (Taiwan Semiconductor Manufacturing Company) TSMC technology, and the simulation was performed using HSPICE. The circuit in Figure 3.8 was simulated with the RLC values shown in Table 3.1 for 22 segments, where R_i, L_i, C_i represented the interconnect ith segment resistance, inductance and capacitance,

respectively. C_r represents the drain-bulk parasitic capacitance of the transistor N_3 and R_r represents the drain resistance of the transistor N_3. Note that we are using the same transistors (channel length and width) N_3 in all PRT repeaters. Therefore, the capacitance C_r is the same in all repeaters. However, we see from Table 3.1 that R_r is not the same for all segments. The reason for this counter-intuitive fact of simulation is as follows: both the drain-source resistance (r_{ds}) and drain-bulk parasitic capacitance (C_{db}) of the transistor NMOS3 of each repeater are extracted from netlist, which is generated by simulating the transistor-based VSRT shown in Figure 3.7 using HSpice. Note that, $r_{ds} = 1/g_{ds}$ and $C_{db} = C_{dtot} - C_{gd}$, where, g_{ds} is the drain-source conductance, C_{dtot} is the total parasitic capacitance, and C_{gd} is the drain parasitic capacitance, all obtained from the circuit netlist. In Figure 3.8 we have two unknown components: the first component is the drain to bulk parasitic capacitance C_r of the transistor NMOS3 (N_3), and the second component is the drain to source resistance R_r of the same transistor. Both components are in shunt and attached to the wire from the wire side (one terminal) and to the ground (the second terminal), as shown in Figure 3.6. We calculate the value of these two components though an ac simulation. Then, we setup the wire in an initial condition in the simulator. Finally, we transmit a logical '0' that would be received at the load terminal. Note that transmitting a logical '1' with the repeater of Figure 3.2 is done with no propagation delay due to the prechagre mechanism.

Table 3.1: RLC values of Figure 3.8

Segments	$R_i(\Omega)$	L_i (*nH*)	C_i (*fF*)	C_r (*fF*)	$R_r(\Omega)$
S_1	172.90	1.6625	605.5	$7.406*10^{-15}$	$18.096*10^3$
S_2	176.7	1.6991	618.834	$7.406*10^{-15}$	$20.517*10^3$
S_3	180.5	1.7457	632.168	$7.406*10^{-15}$	$20.925*10^3$
S_4	184.3	1.7723	645.502	$7.406*10^{-15}$	$14.188*10^3$
S_5	188.1	1.8089	658.836	$7.406*10^{-15}$	$16.093*10^3$
S_6	191.9	1.8456	672.17	$7.406*10^{-15}$	$17.376*10^3$
S_7	195.7	1.882	685.5	$7.406*10^{-15}$	$16.835*10^3$
S_8	199.6	1.9188	698.838	$7.406*10^{-15}$	$15.974*10^3$
S_9	203.4	1.9554	712.172	$7.406*10^{-15}$	$15.501*10^3$
S_{10}	207.2	1.992	725.506	$7.406*10^{-15}$	$16.972*10^3$
S_{11}	211	2.0286	738.84	$7.406*10^{-15}$	$17.085*10^3$
S_{12}	214.78	2.065	752.1739	$7.406*10^{-15}$	$16.319*10^3$
S_{13}	218.6	2.1018	765.508	$7.406*10^{-15}$	$15.547*10^3$
S_{14}	222.4	2.138	778.842	$7.406*10^{-15}$	$15.603*10^3$
S_{15}	226.2	2.175	792.176	$7.406*10^{-15}$	$15.941*10^3$
S_{16}	230	2.2117	805.51	$7.406*10^{-15}$	$15.911*10^3$
S_{17}	233.8	2.2483	818.844	$7.406*10^{-15}$	$15.664*10^3$
S_{18}	237.6	2.2849	832.178	$7.406*10^{-15}$	$15.591*10^3$
S_{19}	214.4	2.3215	845.512	$7.406*10^{-15}$	$16.38*10^3$
S_{20}	245.2	2.3581	858.846	$7.406*10^{-15}$	$16.445*10^3$
S_{21}	249	2.3947	872.18	$7.406*10^{-15}$	$15.608*10^3$
S_{22}	252.9	2.4313	885.514	$7.406*10^{-15}$	$16.787*10^3$

Simulation results are shown in Table 3.2, which lists the propagation delays associated with the different models shown in Figure 3.7 and Figure 3.8, i.e., the transistor-based model and the parallel RC-based model. It shows that both configurations have very close propagation delay performances, which proves the accuracy of the parallel RC-based model. The two models are simulated using the parameters listed in Table 3.1.

Table 3.2 Propagation Delay Comparison of PRT and RC-VSRT Models

Model	Time Delay (nsec)
Transistor-based model	9.12
Parallel RC-based model	9.018

To check its accuracy, the parallel RC-based model was first compared to a transistor-based repeater VSRT using HSpice simulations with a 0.5 micron TSMC (Taiwan Semiconductor Manufacturing Company) fabrication technology. In the following chapter, we will develop the new an analytical model for the propagation delay starting from the transfer function of one segment and extending the model to N segments.

Chapter 4

An Analytical Parallel-Resistance RC-based Repeater Model for the Variable-Segment Regeneration Technique (VSRT)

4.1. Introduction

In the design of high speed systems, precise calculation of propagation delay in VLSI interconnects is crucial. With the development of VLSI technology, transmission wire effects now play a critical role in determining interconnect delays and system performance. A number of techniques have been presented for the simulation of interconnects. These techniques are based on either simulation techniques or analytical formulas (closed-form). Direct simulation tools such as SPICE give the most exact insight into arbitrary interconnect structures, but are computationally expensive. Thus, Elmore delay [9], which represents the first moment of the transfer function is the most commonly used delay model in the performance-driven routing of clock distribution and Steiner global routing topologies. The Elmore delay model can estimate the RC interconnect wires, in contrast, it cannot accurately estimate the delay for RLC interconnect wires. In this chapter, based on a transfer function calculation we are presenting a more accurate analytical model of the Variable-Segment Regeneration Technique (VSRT), which was introduced by Awwad and Nekili [34].

4.2. Previous Analytical Delay Models

Awwad and Nekili [34] used the work of Kahng and Muddu [24] to calculate an approximate analytical closed-form model for the VSRT. In both works, a serial resistance with a shunt capacitor was used to represent each inserted parallel repeater, as was discussed in Chapter 3. This model does not take into account the effect of complex interactions of inserted repeaters, and distributed driving capabilities of these repeaters beyond their local segments. Indeed, the approximated RC-modeled time constant of the parallel repeater does not reflect the driving capabilities of the inserted repeaters along the interconnect. In fact, with this model, the signal driving capability does not add with the distance from the interconnect input, but rather decreases, which does not properly reflect the operation of the repeater. Also, the usage of a serial resistance in the path of signal propagation would give false delay estimation because the repeater is supposed to pull-down the line and not load with more resistance.

4.3. A New Analytical Delay Model for the Variable-Segment Regeneration Technique (VSRT)

This section presents a new delay model, which gives a closed-form delay estimate that considers the effect of inductance. Taking into account the VSRT model introduced by Awwad and Nekili in [34], the analytical delay model for the parallel regeneration technique is based on the first and second moments which incorporate the effects of inductance of a distributed wire. In order to overcome some of the weaknesses of the mathematical model presented by Awwad and Nekili [34] for the VSRT, we rather model the pull-down resistance of the repeater in parallel with wire rather than in series. This

model is shown in Figure 4.1, where R is the segment resistance, L is the segment inductance and R_r is the drain-source repeater resistance, as we discussed in Chapter 3. C_i is the wire segment capacitance, C_r is the parasitic repeater capacitance, V_i is the input voltage of the wire segment, and V_o is the output voltage of the wire segment

Let us assume that $G_r = 1 / R_r$, and the total capacitance of the wire segment $C = C_i + C_r$

Therefore, $V_i = V_o(sC + G_r)(R + sL)$

Then, the transfer function of the interconnect model shown in Figure 4.1 can be written

$$\text{as } H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{(sC + G_r)(R + sL)} \tag{4.1}$$

$$= \frac{1}{s^2LC + s(RC + LG_r) + RG_r}$$

$$\text{Thus, the transfer function is } H(s) = \frac{1}{\beta s^2 + s\gamma + \alpha} \tag{4.2}$$

where, $\beta = LC, \gamma = RC + LG_r$ and, $\alpha = RG_r$

The resulting transfer function has two poles.

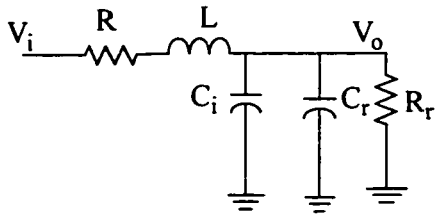

Figure 4.1 One-Segment VSRT with the repeater resistance modeled in parallel with the wire

Assuming the circuit of Figure 4.1 is driven with the step function shown in Figure 4.2. This input is a unit step function, and is represented in the time-domain as u(t-a). The

Laplace transfer function of such input is: $V_i(s) = \frac{e^{-as}}{s}$, where a is an arbitrary point on the time axis.

Figure 4.2 Step input function

Recalling Equation (4.1) and substituting the value of $V_i(s)$ as an input step function, H(s) becomes: $H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{\beta s^2 + \gamma s + \alpha}$

Thus, $V_o(s) = \frac{V_i(s)}{\beta s^2 + \gamma s + \alpha} = \frac{e^{-as}}{s(\beta s^2 + \gamma s + \alpha)}$

$$V_o(s) = \frac{e^{-as}}{s(\beta s^2 + \gamma s + \alpha)} = \frac{e^{-as}}{s(s - s_1)(s - s_2)}$$

where the two poles of the transfer function are:

$$s_{1,2} = \frac{-\gamma \pm \sqrt{\gamma^2 - 4\beta\alpha}}{2\beta}$$

Let us consider the intermediate variable $V_1 = \frac{1}{s(\beta s^2 + \gamma s + \alpha)}$

By using partial fractions:

$$V_1 = \frac{A}{s} + \frac{B}{(s - s_1)} + \frac{D}{(s - s_2)} \tag{4.3}$$

The values of A, B and D can be obtained from Equation (4.3) by changing the value of s such that:

$$A(s - s_1)(s - s_2) + B(s)(s - s_2) + D(s(s - s_1)) = 1$$

If s = s_1 then, $B(s)(s - s_2) = 1 \rightarrow B = \frac{1}{s_1(s - s_2)}$

If s = s_2 then, $D(s_2)(s_2 - s_1) = 1 \rightarrow D = \frac{1}{s_2(s_2 - s_1)}$

and, if s = 0 then, $A(-s_1)(-s_2) = 1 \rightarrow A = \frac{1}{s_1 s_2}$

Using Equation (4.3), and considering its Laplace inverse, we get the expression of the time-domain response. Therefore, Equation (4.3) becomes:

$$V_1(t) = [Au(t) + Be^{s_1 t}u(t) + De^{s_2 t}u(t)]$$

$$= [A + Be^{s_1 t} + De^{s_2 t}]u(t)$$

We used the unit step function as an input e^{-as} by using the basic rule which is shifting the time $t \rightarrow t-a$

$$e^{-as}F(s) \rightarrow f(t-a)u(t-a)$$

Since $V_o = V_i e^{-as}$, Equation (4.3) becomes:

$$V_o(t) = [A + Be^{s_1(t-a)} + De^{s_2(t-a)}]u(t-a) \tag{4.4}$$

Substituting A, B and D values in Equation (4.4) leads to:

$$V_o(t) = \left[\frac{1}{s_1 s_2} + \frac{1}{s_1(s-s_2)}e^{s_1(t-a)} + \frac{1}{s_2(s_2-s_1)}e^{s_2(t-a)}\right]u(t-a) \tag{4.5}$$

The poles of the transfer function can be either real, complex or double. We can now separately derive the delay model from the two-pole response for each of these three cases.

4.3.1. Real Poles

The two poles methodology yields the following response for the case of real poles where,

$$s_1 = \frac{-\gamma + \sqrt{\gamma^2 - 4\beta\alpha}}{2\beta}$$

$$s_2 = \frac{-\gamma - \sqrt{\gamma^2 - 4\beta\alpha}}{2\beta}$$

The condition for the poles to be real is $\sqrt{\gamma^2 - 4\alpha\beta} > 0$

$$V_o(t) = \left[\frac{1}{s_1 s_2} + \frac{1}{s_1(s_1-s_2)}e^{s_1(t-a)} + \frac{1}{s_2(s_2-s_1)}e^{s_2(t-a)}\right]u(t-a)$$

Since $|s_2| > |s_1|$, therefore the second term in the time-domain response decreases rapidly

compared to the first term. Hence, the two-pole response can be approximated by:

$$V_o(t) \approx \left[\frac{1}{s_1 s_2} + \frac{1}{s_1(s_1 - s_2)} e^{s_1(t-a)}\right] u(t-a) \text{ or } \frac{V_o(t)}{u(t-a)} = \frac{1}{s_1 s_2} + \frac{1}{s_1(s_1 - s_2)} e^{s_1(t-a)}$$

$\frac{1}{s_1(s_1 - s_2)} e^{s_1(t-a)} = \frac{1}{s_1 s_2} - \frac{V_o(t)}{u(t-a)}$ by keeping the exponential in the left side then multiplying the right side by the inverse of the exponential coefficient, which becomes:

$$e^{s_1(t-a)} = \frac{s_1(s_1 - s_2)}{s_1 s_2} - [s_1(s_2 - s_1)]\left[\frac{V_o(t)}{u(t-a)}\right]$$

$$\text{or, } s_1(t-a) = \ln\left(\frac{s_1(s_1 - s_2)}{s_1 s_2} - [s_1(s_2 - s_1)]\left[\frac{V_o(t)}{u(t-a)}\right]\right)$$

$$\text{letting, } X_r = \ln\left(\frac{s_1(s_1 - s_2)}{s_1 s_2} - [s_1(s_2 - s_1)]\left[\frac{V_o(t)}{u(t-a)}\right]\right)$$

$$\text{we have } t - a = \frac{X_r}{|s_1|}$$

$$t = \frac{X_r}{|s_1|} + a$$

Thus, the delay at voltage $\frac{V_o(t)}{u(t-a)}$ can be obtained as: $T_r = \frac{X_r}{|s_1|} + a$, where, T_r is the time domain of the real poles.

4.3.2. Complex Poles

The condition for complex poles is $\sqrt{\gamma^2 - 4\beta\alpha} < 0$

where the two poles of the transfer function are:

$$s_1 = \frac{-\gamma + \sqrt{\gamma^2 - 4\beta\alpha}}{2\beta} = -M + jN$$

$$s_2 = \frac{-\gamma - \sqrt{\gamma^2 - 4\beta\alpha}}{2\beta} = -M - jN$$

where, $M = \frac{\gamma}{2\beta}$

and, $N = \frac{\sqrt{|\gamma^2 - 4\beta\alpha|}}{2\beta}$

Substituting the value of M and N in Equation (4.4) leads to

$$V_o(t) = [A + Be^{-M(t-a)}e^{jN(t-a)} + De^{-M(t-a)}e^{-jN(t-a)}]u(t-a)$$

The time-domain response for complex poles is given by

$$V_o(t) = \sqrt{\frac{4\beta\alpha}{4\beta\alpha - \gamma^2}} e^{\frac{-\gamma}{\beta\alpha}} \times \sin\left[\frac{\sqrt{4\beta\alpha - \gamma^2}}{2\beta\alpha}(t-a) + \rho\right]$$

where, $\rho = \text{atan}\frac{\sqrt{4\beta\alpha - \gamma^2}}{\gamma}$

$$\therefore V_o(t) = [A + e^{-M(t-a)}B\cos N(t-a) + jB\sin N(t-a) + D\sin N(t-a) - jD\sin N(t-a)]$$

or,$[A + e^{-M(t-a)}(B + D)\cos N(t-a) + j(B - D)\sin N(t-a)]$

Substituting the M and N values in the above equation, we get:

$$V_o(t)= \left[A + \sqrt{\frac{4\beta\alpha}{4\beta\alpha-\gamma^2}}e^{\frac{-\gamma}{\beta\alpha}(t-a)} \times \sin\left(\frac{\sqrt{4\beta\alpha-\gamma^2}}{2\beta\alpha}(t-a)+\rho\right)\right]u(t-a)$$

Rearranging the terms would result in:

$$\frac{V_o(t)}{u(t-a)} - A = \sqrt{\frac{4\beta\alpha}{4\beta\alpha-\gamma^2}}e^{\frac{-\gamma}{\beta\alpha}(t-a)} \times \sin\left(\frac{\sqrt{4\beta\alpha-\gamma^2}}{2\beta\alpha}(t-a)+\rho\right)$$

$$e^{\frac{-\gamma}{\beta\alpha}(t-a)} \times \sin\left(\frac{\sqrt{4\beta\alpha-\gamma^2}}{2\beta\alpha}(t-a)+\rho\right) = \frac{\frac{V_o(t)}{u(t-a)} - A}{\sqrt{\frac{4\beta\alpha}{4\beta\alpha-\gamma^2}}} \tag{4.6}$$

The delay at a given voltage $\frac{V_o(t)}{u(t-a)}$ can be computed by solving the time in Equation(4.6) recursively. Elmore delay T_{ED} is defined as the first moment of the system impulse response, i.e, the coefficient of s in the system transfer function H(s). Following similar simplification performed by Kahng and Muddu [24] to solve the above recursive equation one can approximate the time variable in the exponential term by Elmore delay, i.e., substitute T_{ED} for a time t. Expanding sine in s Taylor series and considering only the first term yields:

$$e^{\frac{-\gamma}{\beta\alpha}(T_{ED}-a)}\left(\frac{\sqrt{4\beta\alpha-\gamma^2}}{2\beta\alpha}(T_c-a)+\rho\right) = \frac{\frac{V_o(t)}{u(t-a)} - A}{\sqrt{\frac{4\beta\alpha}{4\beta\alpha-\gamma^2}}}$$

where, T_c is the time domain of the complex poles.

$$(T_{ED}-a) = \frac{\frac{V_o(t)}{u(t-a)} - A}{e^{\frac{-\gamma}{\beta\alpha}(T_{ED}-a)}\frac{\sqrt{\beta\alpha}}{\beta\alpha}} - \frac{2\rho\beta\alpha}{\sqrt{4\beta\alpha-\gamma^2}}$$

$$T_c = \frac{\frac{V_o(t)}{u(t-a)} - A}{e^{\frac{-\gamma}{\beta\alpha}(T_{ED}-a)}\frac{\sqrt{\beta\alpha}}{\beta\alpha}} - \frac{2\rho\beta\alpha}{\sqrt{4\beta\alpha-\gamma^2}} + a$$

Letting $X_c = \frac{\frac{V_o(t)}{u(t-a)} - A}{e^{\frac{-\gamma}{\beta\alpha}(T_{ED}-a)}\frac{\sqrt{\beta\alpha}}{\beta\alpha}} - \frac{2\rho\beta\alpha}{\sqrt{4\beta\alpha-\gamma^2}} + a$

$$T_c = X_c + a$$

4.3.3. Double Poles

Referring to equation: $V_1 = \frac{1}{s(\beta s^2 + \gamma s + \alpha)}$

we have $s_1 = s_2$ therefore, $V_1 = \frac{1}{s(s-s_1)^2}$

$$V_1 = \frac{1}{s(s-s_1)^2} = \frac{E}{s} + \frac{F}{(s-s_1)^2}$$

By using partial fractions, we calculate the constant E and F as follows,

If $s = 0 \rightarrow 1 = Es_1^2 \rightarrow E = \frac{1}{s_1^2}$

and if $s = s_1 \rightarrow 1 = Fs_1 \rightarrow F = \frac{1}{s_1}$

Now, following the same method described for real poles, we express the time domain response: $V_o(t) = [E + F(t-a)e^{s_1(t-a)}]u(t-a)$

$$\text{at } t = t_0 \rightarrow \left(\frac{V_o(t_0)}{u(t-a)F} - \frac{E}{F} = (t-a)e^{s_2(t-a)}\right)$$

$$(t-a) = e^{-s_1 t} e^{as_1}\left[\frac{V_o(t_0)}{u(t_0-a)} - \frac{E}{F}\right]$$

Following the procedure outlined when dealing with the complex poles, we approximate the time variable in the exponential term by Elmore delay, i.e., substitute T_{Ed} for time t.

$$\text{Thus, } (t-a) = e^{-s_1 T_{ED}} e^{as_1}\left[\frac{V_o(t_0)}{u(t_0-a)} - \frac{E}{F}\right].$$

The condition for a double pole is $\gamma^2 = 4\beta\alpha$, where $s_1 = s_2 = \frac{\gamma}{2\beta}$. Substituting T_d for time t, where T_d is the time delay for the double poles. Then, the double-pole response is

$$T_d = e^{s_1(a-T_{ED})}\left[\frac{V_o(t_0)}{u(t_0-a)} - \frac{E}{F}\right] + a \tag{4.7}$$

$$\text{thus, } T_d = X_d + a$$

$$\text{where, } X_d = e^{s_1(a-T_{ED})}\left[\frac{V_o(t_0)}{u(t_0-a)} - \frac{E}{F}\right]$$

In the following subsection, we derive the expression for A_0, A_1 and A_2 which are respectively the coefficients of s^0, s^1 and s^2 terms, in terms of R, L, C and R_r circuit parameters shown in Figure 4.1. For the sake of simplicity, we start with only one segment.

4.4. Extending the Mathematical Model to N Segments

For the sake of completeness, the current section proposes a general analytical model for any number of segments. To calculate the delay at any segment along the wire, this can be done by extending the mathematical model based on the ABCD parameters. A theoretical delay model is needed to have a deeper understanding of the VSRT. In this section, we develop an analytical delay estimate for the parallel-resistance RC-based repeater VSRT, using first and second moments, which takes into account the effect of inductance.

A. Case of One Segment Only

Considering only one segment as shown in Figure (4.3)

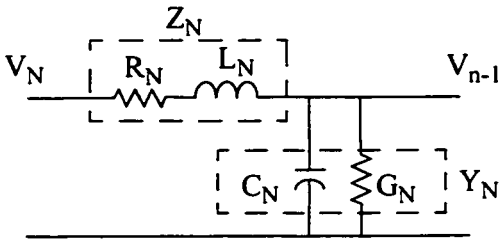

Figure 4.3: One segment only

the ABCD parameters are:

$$\begin{bmatrix} A_N & B_N \\ C_N & D_N \end{bmatrix}$$

where,

$A_N=1+Z_NY_N$,

$B_N=Z_N$,

$C_N=Y_N$,

and $D_N=1$ (4.8)

in addition,

$Z_N = R_N + s L_N$,

$Y_N = G_N + s C_N$

Therefore,

$A_N = 1 + (R_N + s L_N)(G_N + s C_N)$

$= (1 + R_N G_N) + s (L_N G_N + C_N R_N) + s^2 L_N C_N$

B. Case of Two Segments Only:

Considering two segments only, and following similar instructions than for the case of one segment, the ABCD parameters can be extracted for the circuit shown in Figure 4.4.

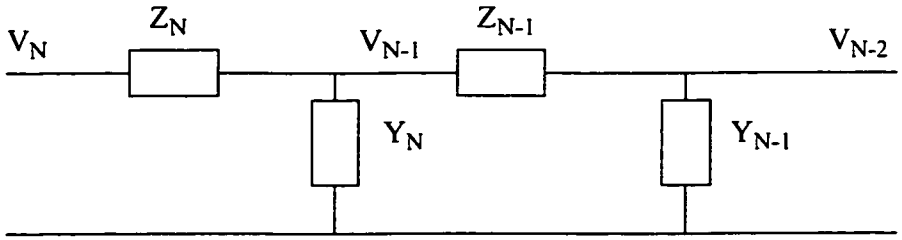

Figure 4.4 Two segments only

Overall ABCD parameters are given by following matrices:

$$\begin{bmatrix} A_{02} & B_{02} \\ C_{02} & D_{02} \end{bmatrix} = \begin{bmatrix} A_N & B_N \\ C_N & D_N \end{bmatrix} \begin{bmatrix} A_{N-1} & B_{N-1} \\ C_{N-1} & D_{N-1} \end{bmatrix} = \begin{bmatrix} A_N A_{N-1} + B_N C_{N-1} & A_N B_{N-1} + B_N D_{N-1} \\ C_N A_{N-1} + D_N C_{N-1} & C_N B_{N-1} + D_N D_{N-1} \end{bmatrix}$$

From the above matrices, we have:

$A_{02} = A_N A_{N-1} + B_N C_{N-1}$

Substituting the value of A, B, C, and D in Equation 4.8, we get:

$A_{02} = \{(1 + R_N G_N) + s (L_N G_N + C_N R_N) + s^2 (L_N C_N)\}\{(1 + R_{N-1} G_{N-1}) +$

$s (L_{N-1} G_{N-1} + C_{N-1} R_{N-1}) +$

$s^2 (L_{N-1}C_{N-1})+ (R_N+ s L_N)(G_{N-1}+ s C_{N-1})\}$

$A_{02}= \{(1+ R_N G_N) (1+ R_{N-1} G_{N-1})+(R_N G_{N-1})\}+$

$s\{(L_N G_N+C_N R_N) (1+ R_{N-1} G_{N-1})+(L_{N-1} G_{N-1}+C_{N-1} R_{N-1})(1+ R_N G_N)+$

$(L_N G_{N-1}+R_N C_{N-1})\} +s^2 \{(L_N C_N)(1+ R_{N-1} G_{N-1}) + (L_{N-1} G_{N-1})(1+ R_N G_N)+(L_N C_{N-1})\}$

From these equations, we get the coefficients of s^0, s^1 and s^2 are as follows

s^0 term: $\{1+ R_N (G_N+ G_{N-1})+ R_{N-1} (G_{N-1})+(R_N G_N)(R_{N-1} G_{N-1})\}$

s^1 term: $\{(L_N (G_N+G_{N-1})+ L_{N-1}G_{N-1}+ R_N (C_N+C_{N-1})+C_{N-1} R_{N-1} + (R_{N-1} G_{N-1})$

$(L_N G_N +C_N R_N)+ (R_N G_N)(L_N G_N+ C_N R_N)+R_N G_N(L_{N-1} G_{N-1}+C_{N-1} R_{N-1})\}$

s^2 term:$\{L_N (C_N+C_{N-1})+(L_{N-1}C_{N-1})+(L_N C_N R_{N-1}G_{N-1})+ (L_{N-1}C_{N-1}R_N G_N)\}$

$A_{02}= L_N C_N(1+ R_{N-1} G_{N-1})+ (R_{N-1} G_{N-1}) + L_{N-1}C_{N-1}(1+ R_N G_N)$

From the above equations, we find that, the coefficients of s^0 are in consistency which give us the general expression of the constant terms for all the segments and the formula can be expressed as shown letter.

The s^0 term is the A-parameter of the ladder network:

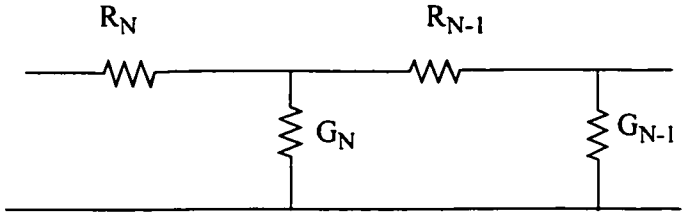

Figure 4.5 The constant terms along the wire

This can be readily expanded to any number of segments.

Also,

$A_{02} = \{(1+ R_N G_N) + s (L_N G_N+C_N R_N)+s^2 L_N C_N\}\{1+ R_{N-1} G_{N-1}) +$

$s (L_{N-1} G_{N-1}+C_{N-1} R_{N-1})+s^2 (L_{N-1}C_{N-1})+ (R_N+ s L_N)(G_{N-1}+ s C_{N-1})\}$

s^3 term: $\{(L_N C_N) (L_{N-1} G_{N-1} + C_{N-1} R_{N-1})+ L_{N-1} C_{N-1} (L_N G_N +C_N R_N)$

s^4 term: $L_N C_N L_{N-1} C_{N-1}$

s^{2N} term is: $L_N C_N L_{N-1} C_{N-1} L_{N-2} C_{N-2} L_{N-3} C_{N-3} L_{N-4} C_{N-4} \cdots L_N C_N$

By looking at these equations which give us the general expression of A_{02} for all the segments and the formula can be expressed as, $\left[\prod_{j=1}^{N} L_j\right]\left[\prod_{k=1}^{N} C_k\right]$.

Let us consider single RLC interconnect wire that is modeled by inserting a repeater with N segments. These RLC segments are connected as shown in Figure 4.4. For this structure, the input voltage V_{N+1} (s) can be written as:

$$V_{N-1}(s) = (R_N + sL_N)\sum_{j=1}^{N}[sC_j + G_j]V_j(s) + V_N(s) \tag{4.9}$$

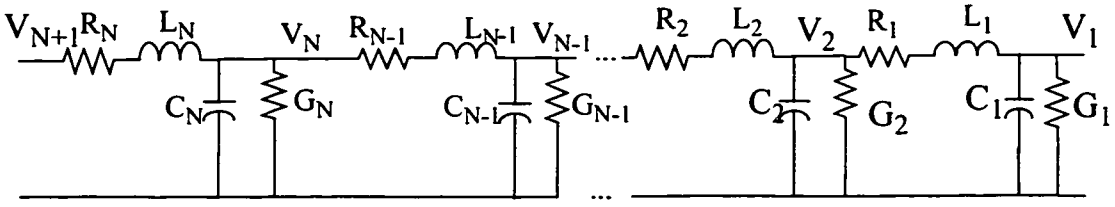

Figure 4.6: N-segment distributed RLC interconnect model

From Equation (4.9) the general expression of the constant terms for all segments are the coefficients of s^0, which are given by, $R_N\left[\sum_{j=1}^{N} G_j V_j(s)\right]$ + the constant values of V_N (s).

In other words, using the ABCD parameters, the general equation of the constant terms can be written as:

$$\begin{bmatrix} 1+R_N G_N & R_N \\ G_N & 1 \end{bmatrix}\begin{bmatrix} 1+R_{N-1} G_{N-1} & R_N \\ G_N & 1 \end{bmatrix}\cdots\begin{bmatrix} 1+R_2 G_2 & R_2 \\ G_2 & 1 \end{bmatrix}\begin{bmatrix} 1+R_1 G_1 & R_1 \\ G_1 & 1 \end{bmatrix}$$

This can be written as a matrix product of N segments for the constant terms which are R and G

$$\prod_{i=1}^{N-1}\begin{bmatrix} 1+R_{N-i} G_{N-i} & R_{N-i} \\ G_{N-i} & 1 \end{bmatrix} \tag{4.10}$$

Multiplying by the unit matrix, the matrices will not change. The first segment consists of s of the ABCD parameters can be written as

$$\begin{bmatrix} 1 & Z_N \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ Y_N & 1 \end{bmatrix}=\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}+\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ Y_N & 0 \end{bmatrix}+\begin{bmatrix} 0 & Z_N \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}+\begin{bmatrix} 0 & Z_N \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ Y_N & 0 \end{bmatrix}$$

Substituting the values of $Z_N = R_N + s L_N$, and $Y_N = G_N + s C_N$ in the above matrices gives:

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ G_N + sC_N & 0 \end{bmatrix}=\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ G_N & 0 \end{bmatrix}+\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ sC_N & 0 \end{bmatrix}$$

Similarly,

$$\begin{bmatrix} 0 & R_N + sL_N \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}=\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & R_N \\ 0 & 0 \end{bmatrix}+\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & sL_N \\ 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix} 0 & 0 \\ G_N + sC_N & 0 \end{bmatrix}\begin{bmatrix} 0 & R_N + sL_N \\ 0 & 0 \end{bmatrix}=\begin{bmatrix} 0 & R_N \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ G_N & 0 \end{bmatrix}+\begin{bmatrix} 0 & R_N \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ sC_N & 0 \end{bmatrix}$$

$$+\begin{bmatrix} 0 & sL_N \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ G_N & 0 \end{bmatrix}+\begin{bmatrix} 0 & sL_N \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ sC_N & 0 \end{bmatrix}$$

The first wire segments can be written as

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}+\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ G_N & 0 \end{bmatrix}+\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 & 0 \\ sC_N & 0 \end{bmatrix}$$

$$+\begin{bmatrix}0 & R_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}+\begin{bmatrix}0 & sL_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}+\begin{bmatrix}0 & R_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}0 & 0\\ G_N & 0\end{bmatrix}+\begin{bmatrix}0 & R_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}0 & 0\\ sC_N & 0\end{bmatrix}$$

$$+\begin{bmatrix}0 & sL_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}0 & 0\\ G_N & 0\end{bmatrix}+\begin{bmatrix}0 & sL_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}0 & 0\\ sC_N & 0\end{bmatrix}$$

By using the matrices algebra, the above matrices can be rearranged as,

$$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}+\begin{bmatrix}0 & 0\\ G_N & 0\end{bmatrix}+\begin{bmatrix}1 & 0\\ sC_N & 0\end{bmatrix}+\begin{bmatrix}0 & R_N\\ 0 & 0\end{bmatrix}+\begin{bmatrix}0 & sL_N\\ 0 & 0\end{bmatrix}+\begin{bmatrix}R_NG_N & 0\\ 0 & 0\end{bmatrix}$$

$$+\begin{bmatrix}0 & R_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}0 & 0\\ sC_N & 0\end{bmatrix}+\begin{bmatrix}0 & sL_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}0 & 0\\ G_N & 0\end{bmatrix}+\begin{bmatrix}0 & sL_N\\ 0 & 0\end{bmatrix}\begin{bmatrix}0 & 0\\ sC_N & 0\end{bmatrix}$$

$$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}+\begin{bmatrix}0 & 0\\ G_N & 0\end{bmatrix}+\begin{bmatrix}0 & R_N\\ 0 & 0\end{bmatrix}+\begin{bmatrix}R_NG_N & 0\\ 0 & 0\end{bmatrix}$$

$$+s\begin{bmatrix}1 & 0\\ C_N & 0\end{bmatrix}+\begin{bmatrix}0 & L_N\\ 0 & 0\end{bmatrix}+\begin{bmatrix}C_NR_N & 0\\ 0 & 0\end{bmatrix}+\begin{bmatrix}L_NG_N & 0\\ 0 & 0\end{bmatrix}+s^2\begin{bmatrix}L_NC_N & 0\\ 0 & 0\end{bmatrix}$$

Finally, the constant terms A_{0N} for all the segments can be expressed as:

$$\begin{bmatrix}1+R_NG_N & R_N\\ G_N & 1\end{bmatrix}+s\begin{bmatrix}1+C_NR_N+L_NG_N & L_N\\ C_N & 0\end{bmatrix}+s^2\begin{bmatrix}L_NC_N & 0\\ 0 & 0\end{bmatrix}$$

Defining A_{0N}, A_{1N} and A_{2N}, this matrix will be

$$[A_{0N}] + s[A_{1N}] + s^2[A_{2N}] \qquad (4.11)$$

where $[A_{0N}]$ is the constant term (coefficient of s^0). In order to get the constant term of N segments the general form can be written as:

$$\prod_{i=1}^{N-1}[A_{0,N-i}]$$

Multiplying the matrices $[A_0]$, $[A_1]$... $[A_{N-i}]$, applying Equation (4.10) and considering

the first and the second terms (coefficients of s^0 and s^1) for N-segment to generalize the equation.

In order to get the constant and the s terms, we have

$$\prod_{i=1}^{N-1}[(A_{0,N-i})+s(A_{1,N-i})]$$

Neglecting the higher-order terms. The formula for the constant term is given by Equation (4.10).

Based on the Equation (4.11), let us go forward to the next segments. Let's consider the first two segments:

a) Considering two segments N and N-1,

$$[A_{0,N}+A_{1,N}\,s][A_{0,N-1}+A_{1,N-1}s]$$

$$=\{(A_{0,N})(A_{0,N-1})+s[(A_{1,N})(A_{0,N-1})+(A_{0,N})(A_{1,N-1})]\} \qquad (a_1)$$

Neglecting s^2 term for an instance,

b) Considering the first three segments. Multiplying Equation (a_1) by $[A_{0,N-2}+A_{1,N-2}\,s]$, gives

$$[(A_{0,N})(A_{0,N-1})(A_{0,N-2})]+\{[(A_{0,N})(A_{0,N-1})(A_{1,N-2})]+[(A_{0,N})(A_{1,N-1})(A_{0,N-2})]+$$

$$[(A_{1,N})(A_{0,N-1})(A_{0,N-2})]\}s \qquad (b_1)$$

c) Considering four segments. Multiplying Equation (b_1) by $[A_{0,N-3}+A_{1,N-3}\,s]$, gives

$$[(A_{0,N})(A_{0,N-1})(A_{0,N-2})(A_{0,N-3})]+s\{[(A_{0,N})(A_{0,N-1})(A_{0,N-2})(A_{1,N-3})]+[(A_{0,N})(A_{0,N-1})$$

$$(A_{1,N-2})(A_{0,N-3})]+[(A_{0,N})(A_{1,N-1})(A_{0,N-2})(A_{0,N-3})]+[(A_{1,N})(A_{0,N-1})(A_{0,N-2})(A_{0,N-3})]\} \quad (c_1)$$

Expanding by induction

$$[(A_{0,N})(A_{0,N-1})(A_{0,N-2})\ldots(A_{0,1})]+$$

$$s\{[(A_{0,N})(A_{0,N-1})(A_{1,N-2})\ldots(A_{0,2})(A_{1,1})]+$$

$[(A_{0,N})(A_{0,N-1})(A_{0,N-2})...(A_{1,2})(A_{0,1})]+$

$[...]+$

$[(A_{0,N})(A_{0,N-1})\,(A_{0,N-2})...(A_{0,2})(A_{0,1})]+$

$[(A_{1,N})(A_{0,N-1})(A_{0,N-2})...(A_{0,2})(A_{0,1})]\}$ (4.12)

Recalling Equation (a_1),

$\{(A_{0,N})+s(A_{1,N})+s^2(A_{2,N})\}\{(A_{0,N-1})+s(A_{1,N-1})+s^2(A_{2,N-1})\}$, gives s terms:

s^0 term: $[(A_{0,N})(A_{0,N-1})]$ the first subscripts of A takes a single value "0"

s^1 term: $[(A_{0,N})(A_{1,N-1})+(A_{1,N})(A_{0,N-1})]$ the first subscripts of A takes the values "0, 1".

s^2 term: $[(A_{0,N})(A_{2,N-1})+(A_{1,N})(A_{1,N-1})+(A_{2,N})(A_{0,N-1})]$ the first subscripts of A takes the values "0,1,2".

s^3 term:$[(A_{1,N})(A_{2,N-1})+(A_{2,N})(A_{1,N-1})]$ the first subscripts of A takes the values "0,1,2,3".

s^4 term: $[(A_{2,N})(A_{2,N-1})]$ the first subscripts of A takes the values "0,1,2,3,4".

Recalling the Equation (b),

$[(A_{0,N-2})+s(A_{1,N-2})+s^2(A_{2,N-2})]$

Multiplying Equation (a_1) by the above matrix gives,

$\{[(A_{0,N-2})+s(A_{1,N-2})+s^2(A_{2,N-2})][(A_{0,N})+s(A_{1,N})+s^2(A_{2,N})\}\{(A_{0,N-1})+s(A_{1,N-1})+$

$s^2(A_{2,N-1})]\}$

So the s terms will be as follows:

s^0 term: $[(A_{0,N})(A_{0,N-1})(A_{0,N-2})]$

s^1 term: $[(A_{0,N})(A_{0,N-1})(A_{1,N-2})+(A_{0,N})\,(A_{1,N-1})(A_{0,N-2})+(A_{1,N})(A_{0,N-1})(A_{0,N-2})]$

s^2 term:$[(A_{0,N})(A_{0,N-1})(A_{2,N-2})+(A_{0,N})(A_{2,N-1})(A_{0,N-2})+(A_{2,N})(A_{0,N-1})(A_{0,N-2})+(A_{0,N})$

$(A_{1,N-1})(A_{1,N-2})+(A_{1,N})(A_{1,N-1})(A_{0,N-2})+(A_{1,N})(A_{0,N-1})+(A_{1,N-2})]$

The first subscripts of A takes the values "0,1,2".

s^3 term:$[(A_{0,N})(A_{1,N-1})(A_{2,N-2})]+[(A_{0,N})(A_{2,N-1})(A_{1,N-2})]+[(A_{1,N})(A_{0,N-1})$

$(A_{2,N-2})]+[(A_{1,N})(A_{1,N-1})(A_{1,N-2})]+[(A_{1,N})(A_{2,N-1})(A_{0,N-2})]+[(A_{2,N})(A_{0,N-1})$

$(A_{1,N-2})+(A_{2,N})(A_{1,N-1})(A_{0,N-2})]$

The first subscripts of A takes the values "0,1,2,3"

s^4 term:$[(A_{0,N})(A_{2,N-1})(A_{2,N-2})(A_{1,N})(A_{1,N-1})(A_{2,N-2})(A_{2,N})(A_{0,N-1})(A_{2,N-2})]+[(A_{1,N})$

$(A_{2,N-1})(A_{1,N-2})]+[(A_{2,N})(A_{1,N-1})(A_{1,N-2})+(A_{2,N})(A_{2,N-1})+(A_{0,N-2})]$

The first subscripts of A takes the values "0,1,2,3,4".

s^5 term:$[(A_{2,N})(A_{2,N-1})(A_{1,N-2})]+[(A_{2,N})(A_{1,N-1})(A_{2,N-2})]+[(A_{1,N})(A_{2,N-1})(A_{2,N-2})]$

s^6 term: $[(A_{2,N})(A_{2,N-1})(A_{2,N-2})]$

d) Considering five segments, and Multiplying Equation (c_1) by

$[(A_{0,N-4})+(A_{1,N4})s+s^2(A_{2,N-4})]$ gives,

s^2 term: $[(A_{0,N})(A_{0,N-1})(A_{0,N-2})(A_{0,N-3})(A_{0,N-4})+(A_{0,N})\ [(A_{0,N-1})(A_{0,N-2})(A_{0,N-3})$

$(A_{0,N-4})+(A_{0,N})(A_{0,N-1})(A_{1,N-2})(A_{0,N-3})(A_{1,N-4})+\ (A_{0,N})(A_{1,N-1})(A_{0,N-2})(A_{0,N-3})(A_{1,N4})+$

$(A_{1,N})(A_{0,N-1})(A_{0,N-2})(A_{0,N-3})(A_{1,N-4})+(A_{0,N})(A_{0,N-1})(A_{0,N-2})(A_{2,N-3})(A_{0,N-4})+$

$(A_{0,N})(A_{0,N-1})(A_{1,N-2})(A_{1,N-3})(A_{0,N-4})+(A_{0,N})(A_{0,N-1})(A_{0,N-2})(A_{1,N-3})(A_{0,N-4})+$

$(A_{1,N})(A_{0,N-1})(A_{0,N-2})(A_{1,N-3})(A_{0,N-4})+(A_{0,N})(A_{0,N-1})(A_{2,N-2})(A_{0,N-3})(A_{0,N-4})+$

$(A_{0,N})[(A_{1,N-1})(A_{1,N-2})(A_{0,N-3})(A_{0,N-4})+(A_{1,N})(A_{0,N-1})(A_{1,N-2})(A_{0,N-3})$

$(A_{0,N-4})+(A_{0,N})(A_{2,N-1})(A_{0,N-2})(A_{0,N-3})(A_{0,N-4})+(A_{1,N})(A_{1,N-1})(A_{0,N-2})(A_{0,N-3})(A_{0,N-4})+$

$(A_{2,N})(A_{0,N-1})(A_{0,N-2})(A_{0,N-3})(A_{0,N-4})]$ (d_1)

e) For N segments

s^2 term: $[(A_{0,N})(A_{0,N-1})(A_{0,N-2})...(A_{0,2})(A_{2,1})]$

$+[(A_{0,N})\ [(A_{0,N-1})(A_{0,N-2})...(A_{0,3})(A_{1,2})(A_{1,1})]$

$+[(A_{0,N})(A_{0,N-1})(A_{0,N-2})...(A_{0,4})(A_{1,3})(A_{0,2})(A_{1,1})]$

$+[(A_{0,N})(A_{0,N-1})...(A_{0,5})(A_{1,4})(A_{0,3})(A_{0,2})(A_{1,1})]$

...

...

...

$+[(A_{0,N})(A_{0,N-1})(A_{1,N-2})...(A_{0,3})(A_{0,2})(A_{1,1})]$

$+[(A_{0,N})(A_{1,N-1})(A_{0,N-2})...(A_{0,3})(A_{0,2})(A_{1,1})]$

$+[(A_{1,N})(A_{0,N-1})...(A_{0,3})(A_{0,2})(A_{1,1})]$

$+[(A_{0,N})(A_{0,N-1})(A_{0,N-2})...(A_{0,3})(A_{2,2})(A_{0,1})]$

$+[(A_{0,N})(A_{0,N-1})...(A_{0,4})(A_{1,3})(A_{1,2})(A_{0,1})]$

$+[(A_{0,N})(A_{0,N-1})...(A_{0,5})(A_{1,4})(A_{0,3})(A_{1,2})(A_{0,1})]$

...

...

...

$+[(A_{0,N})(A_{1,N-1})(A_{0,N-2})...(A_{0,5})(A_{0,4})(A_{0,3})(A_{1,2})(A_{0,1})]$

$+[(A_{1,N})(A_{0,N-1})(A_{0,N-2})...(A_{0,3})(A_{1,2})(A_{0,1})]$

...

...

...

$+[(A_{0,N})(A_{0,N-1})(A_{2,N-2})\ (A_{0,N-3})...(A_{0,2})(A_{0,1})]$

$$+[(A_{0,N})(A_{1,N-1})(A_{1,N-2})\ (A_{0,N-3})...(A_{0,2})(A_{0,1})]$$

$$+[(A_{1,N})(A_{0,N-1})(A_{1,N-2})\ (A_{0,N-3})...(A_{0,2})(A_{0,1})]$$

$$+[(A_{0,N})(A_{2,N-1})(A_{0,N-2})...(A_{0,2})(A_{0,1})]$$

$$+[(A_{1,N})(A_{1,N-1})(A_{0,N-2})...(A_{0,2})(A_{0,1})]$$

$$+[(A_{2,N})(A_{0,N-1})(A_{0,N-2})...(A_{0,2})(A_{0,1})] \quad (4.13)$$

4.5. Summary of the Different Cases in the Analytical Delay Model

Here, we summarize the description of the parallel-resistance RC-based repeater VSRT model for estimating delay in arbitrary interconnect trees. From the literature, we find that an RLC network is called an RLC tree if it does not contain a closed path of resistors and inductors, i.e., all resistors and inductors are floating with respect to ground and all capacitors are connected to ground. Consider an RLC interconnect tree with root (or source) S and a set of sinks (or leafs) $L = \{L_1, L_2,..., L_n\}$. The unique path from root S to the sink node i is denoted by p(i) and is referred as the main path. The edges/ nodes not on the main path are referred to as the off-path edges/nodes. Each edge on the main path of the tree can be modeled using a lumped RLC segment, e.g., an L, T or Π model. The off-path subtree rooted at node v can be replaced by the total subtree capacitance at node v. However, we add the drain-source conductance (G_r) of the parallel repeater in shunt with its drain-bulk capacitance and segment capacitance. Figure 4.5 shows the representation of the main path in the tree, where RLC segments are in parallel with C_r G_r-modeled inserted repeaters.

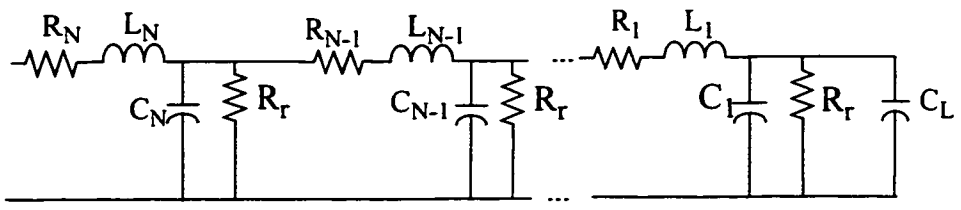

Figure 4.7: RLCG-modeled representation of the N-segment VSRT

The transfer function of this configuration is $H_N(s) = \prod_{i=1}^{N}\left[\frac{1}{\beta_i s^2 + \gamma_i s + \alpha_i}\right]$ (4.14)

where, $\beta_i = L_i C_i$, $\gamma_i = R_i C_i + L_i G_i$, and $\alpha_i = R_i G_i$. Using the analytical developments in previous sections, the 90% threshold delay at a given sink i, can be calculated as follows:

1. For real poles, where the condition is, $\sqrt{\gamma_i^2 - 4\alpha_i\beta_i} > 0$

the delay is: $T_{Nr} = \frac{X_{Nr}}{|s_{1N}|} + a$

where, $X_{Nr} = \ln\left(\frac{s_1(s_1 - s_2)}{s_1 s_2} - [s_1(s_2 - s_1)]\left[\frac{V_o(t)}{u(t-a)}\right]\right)$,

and where the two poles of the transfer function are:

$$s_{1N} = \frac{-\gamma_N + \sqrt{\gamma_N^2 - 4\beta_N\alpha_N}}{2\beta_N},$$

$$s_{2N} = \frac{-\gamma_N - \sqrt{\gamma_N^2 - 4\beta_N\alpha_N}}{2\beta_N}$$

s^0 coefficient: $\alpha_N = [A_{0,N}][A_{0,N-1}]\ldots[A_{0,1}]$

s^1 coefficient: γ_N given by Equation (4.12)

s^2 coefficient: β_N given by Equation(4.13)

where, $A_{0,i} = 1 + R_i G_i$

$A_{1,i} = L_i G_i + C_i R_i$

$A_{2,i} = L_i C_i$

2. For complex poles, where the condition is $\sqrt{\gamma_i^2 - 4\alpha_i\beta_i} < 0$

the delay is, $T_{NC} = X_{NC} + a$

where, $X_{NC} = \dfrac{\dfrac{V_o(t)}{u(t-a)} - A}{e^{\frac{-\gamma_N}{\beta_N\alpha_N}(T_{ED}-a)}\dfrac{\sqrt{\beta_N\alpha_N}}{\beta_N\alpha_N}} - \dfrac{2\rho_N\beta_N\alpha_N}{\sqrt{4\beta_N\alpha_N - \gamma_N^2}}$, and $\rho_N = \text{atan}\dfrac{\sqrt{4\beta_N\alpha_N - \gamma_N^2}}{\gamma_N}$,

when $t \to T_C$, then $\dfrac{V_o(t)}{u(t-a)} \to 1$, because, after T_c, the step input u(t-a) has finished propagating to the interconnect output.

Note, that the Elmore delay at the sink is equal to the first moment, or the first coefficient γ_N of the transfer function of the source-sink main path. We might use the result of Kahng and Muddu [24] to estimate the value of the delay $T_{ED}(i) = 2.3\gamma_i$, which is widely used although it is inaccurate, since it ignores inductance of the interconnect wires.

3. For double poles, where the condition is $\gamma_N^2 = 4\beta_N\alpha_N$

the delay is: $T_{ND} = X_{ND} + a$

where, $s_{1N} = s_{2N} = -\dfrac{\gamma_N}{2\beta_N}$, and $X_{ND} = e^{s_{1N}(a-T_{ED})}\left[\dfrac{V_o(t_0)}{u(t_0-a)} - \dfrac{E}{F}\right]$

The next step is to evaluate the effect of the parallel-resistance RC-based repeater VSRT model on the delay by considering a simple interconnect tree as shown in Figure 4.5. For a

specific value of the number of segments, N, we use the above described recursive coefficients and moments for computing RLCG circuit parameters of the main path.

4.6. Numerical Results and Conclusion

Nekili and Savaria [27] introduced the parallel repeater structure, that is inserted at regular intervals in the interconnect to be regenerated, thus dividing the interconnect into equal segments. To ensure a uniform driving capability for all segments of the interconnect, the size of the repeater was decreased as we move towards the interconnect end (see section 1.3). Another way to keep this uniformity is to divide the interconnect into variable segment lengths, while maintaining the size of the PRT repeater constant.

Let us first consider some assumptions used during simulation:

- the interconnect is divided into N different segments
- the first segment length (percentage of the total length) is l_1
- the uniform difference in segment lengths between any two successive segments is δ such that $l_{i+1} = l_i + \delta$, where i = [1,N-1]

We evaluate the effect of the parallel-resistance RC-based repeater VSRT model in the case of a 10 cm interconnect. A 0.9 μm interconnect width is used as it corresponds to the optimum propagation delay resulting from the simulation as shown in Table 3.2.

$R_i = [l_1 + (i-1)\delta]R_t$, where R_i is the wire resistance, of the i-th segment, and R_t is the total wire resistance,

$L_i = [l_1 + (1-i)\delta]L_t$, where L_i is the wire inductance of the i-th segment, and L_t is the total wire inductance.

$C_i = C_r + [l_1 + (1-i)\delta]C_t$, where C_i is the wire capacitance of the i-th segment, and C_t

is the total wire capacitance

$$\delta = 2\left\lceil \frac{1 - l_1 N}{N(N-1)} \right\rceil \tag{4.15}$$

where N is the number of segments. As δ is positive, this equation assumes that $N > 1$ and

$$l_1 < \frac{1}{N}$$

Considering the transfer function in Equation (4.14) for every specific number of segments, we have a different triplet α, γ ,and β. The algorithm mentioned in the appendix A requires two input variables (l_1 and N) and returns the results of Equations (4.16), (4.17), and (4.18), which are named w, y, and z values, respectively. The required input variables (design parameters) are: l_1, the first segment length (percentage of the total interconnect length), and N, the number of segments.

$$A_{0,i} = 1 + [l_1 + (i-1)\delta]\frac{R_t}{r_i} \tag{4.16}$$

$$A_{1,i} = [l_1 + (i-1)\delta]\frac{L_t}{r_i} + [C_r + (l_1(i-1)\delta)C_t][l_1 + (i-1)\delta]R_t \tag{4.17}$$

$$A_{2,i} = [l_1 + (i-1)\delta]L_t[C_r + (l_1(i-1)\delta)C_t] \tag{4.18}$$

where r_i and C_r are the resistance and the capacitance of the i-th repeater respectively.

Then, the next step is to calculate the poles s_1 and s_2. The calculation showed that complex poles are obtained when the previous simulation assumptions are considered. Using the complex time delay expression (T_c) obtained in section 4.5.2, we calculate the value of the propagation delay for different numbers of segments (different values of N). Table 4.1 shows the propagation delays associated with a 10 cm wire length and a 0.9 μm wire width for different numbers of segments N. For each value of N, the corresponding value

of l_l is extracted from Equation (4.15) considering δ as a constant. The parameter δ has been set to 0.007 in order to be able to compare to the serial-resistance RC-based VSRT in [34]. Then, l_l and N are both provided as inputs to the algorithm in Appendix A. Table 4.1 shows that, as the number of segments increases, the propagation delay decreases because of the increased signal driving capability when more repeaters (i.e., more segments) are added to the interconnect. Based on this result, we conclude that the analytical time delay of the parallel-resistance RC-based VSRT is very close to the simulation results shown in Table 3.2, which means that our analytical delay model is accurate. Moreover, the value of the propagation delay has been plotted in Figure 4.6, as a function of N using Matlab [38]. Figure 4.6 shows that the optimum delay is obtained for N = 21.

Table 4.1: Propagation delays associated with the parallel-resistance RC-based VSRT for a 10 cm wire length and a 0.9 μm wire Width

N	l_l (%)	t_{pd} (nsec)
3	3.29	14.92
5	1.92	14.78
7	1.3	14.57
9	0.9	14.29
13	0.52	13.36
15	0.38	12.66
17	0.26	11.8
20	0.12	10.65
21	0.07	9.10

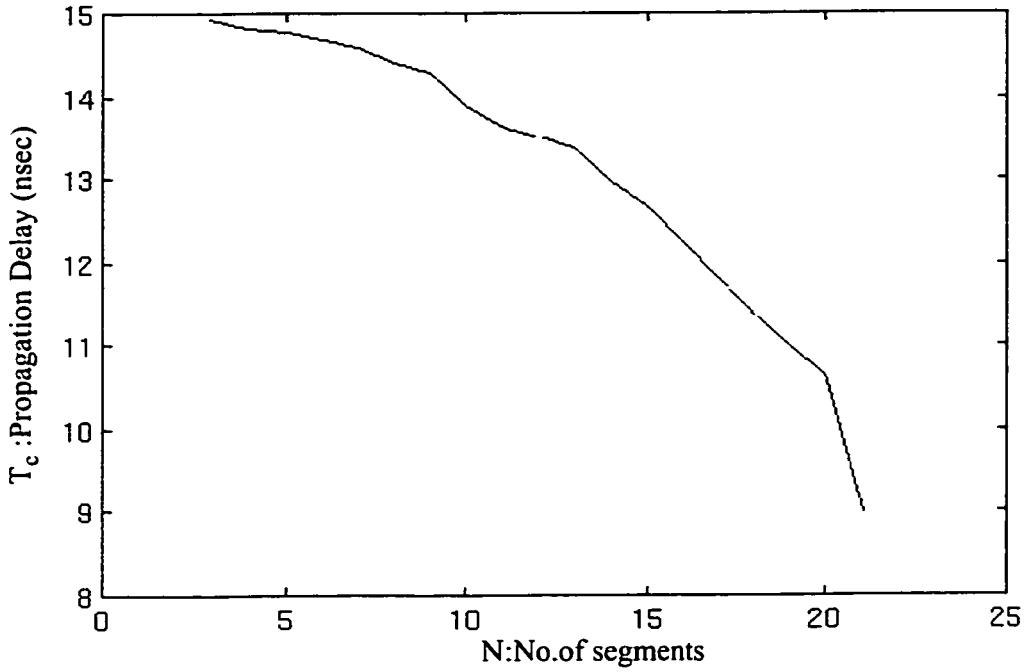

Figure 4.8 Plot of propagation delay of the VSRT analytical delay model with Delta = 0.007 versus No. of Segments

Increasing the number of segments N beyond 21 is expected to decrease the total delay at the expense of increased power dissipation and area.

Chapter 5

Conclusion and Future Work

Long interconnects remain one of the major bottlenecks for high-performance VLSI/SOC circuits. A conventional strategy to break the quadratic dependence of the delay with the interconnect length is to insert regularly spaced repeaters in the interconnect.

This thesis is one of the first attempts to build accurate models for regeneration techniques using parallel repeaters. Previous work in literature has modeled the repeaters as a gate capacitance loading the interconnect and a pull-down resistance in series with the interconnect. Unlike the conventional regeneration techniques which use serial repeaters, the usage of parallel repeaters to regenerate interconnects involves the interaction of all interconnect segments. Modeling the repeater resistance in series with the interconnect suffers some weaknesses. Indeed, in such a case, the signal driving capability decreases with the distance from the interconnect input while it is, in reality, increasing because of the additional driving capability added by inserting repeaters.

To overcome this kind of weaknesses, this thesis modeled the repeater resistance in parallel with the interconnect. Also, to ensure a uniform driving capability from interconnect input to interconnect output, the length of segments is increased when we move toward the interconnect output while the size of repeaters is kept constant. This technique was called the parallel-resistance RC-based repeater VSRT (Variable-Segment Regeneration Technique). To check its accuracy, this technique was first compared to a transistor-based repeater VSRT using HSpice simulations with a 0.5 micron TSMC (Taiwan Semiconduc-

tor Manufacturing Company) fabrication technology.

Then, an analytical model for the propagation delay was built starting from the transfer function of one segment and extending the model to N segments. Each segment is associated to a repeater. In order to account for the effect of interconnect inductance, two moments were used in the transfer function as opposed to previous Elmore delay models which use only one moment for RC interconnects.

Using Java, a software package successfully uses the analytical model to help the designer implement the optimal number of segments that minimizes the propagation delay.

The parallel-resistance RC-based repeater VSRT suffers however: from some limitations:

1. Modeling the repeaters as passive elements and the resistance in parallel with the interconnect put us in a situation where the repeaters attempt discharging the interconnect even in the absence of a logical '0" to propagate, thus eventually affecting the normal operation of the interconnect. However, there is no need to model the propagation of a logical '1' as the delay is known accurately to be zero.

2. Even in presence of a logical '0' to propagate, the repeaters do not wait until the local interconnect nodes reach their threshold but start discharging the local interconnect nodes before the signal even reaches them thus under-estimating the delay as compared to a transistor-based repeater VSRT.

Possible future work consists of the following:

1. The analytical model presented in this thesis involved intensive mathematical calculation in the s-domain. For some interconnect lengths and technologies, an RC model may be accurate enough. Therefore, it is interesting to explore the mathematical complexity of the analytical model for L=0 (no inductance) and to inves-

tigate which length and technology can make an RC model accurate enough.

2. The interconnect design parameters actually consist of the repeater size, the length of the 1^{st} segment, the constant length increase between two consecutive segments and the number of segments. Assuming the repeater size constant (because VSRT adopted), only the optimality of the number of segments has been considered in this thesis. However, for the sake of global optimality, the analytical model developed in this thesis is capable, as is, to plot a 2D propagation delay function with regard to the design parameters other than the repeater size.

3. The complexity of the coefficients in the s-domain made it difficult to calculate a closed-form solution. As an alternative to advise the designer on how to fix the design parameters, a numerical solution was adopted thus saving an immense number of electrical simulations.

4. Current Computer-Aided Design tools do not have modules to address the optimality of regenerating long interconnects. Therefore, the Matlab package developed at the end of this thesis can be fine-tuned, equipped with an interface and then to a CAD tool such as Cadence.

5. Obviously, if attached the designer is looking for a higher delay precision, more moments can be used to achieve a higher-order approximation.

References

[1] Tong. K. T and E. G. Friedman "Estimation of Transient Voltage Fluctuations in the CMOS-Based Power Distribution Networks" IEEE Vol.5, pp. 463-466, 2002.

[2] Ismail. Y. I, E. G. Friedman, and J. L. Neves "Equivalent Elmore Delay for RLC Trees" IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Vol.19, pp. 83-97, Januery 2000.

[3] Ismail. Y. I, and E. G. Friedman "Sensitivity of Interconnect Delay to On-Chip Inductance" Proceeding of the IEEE International Symposium on Circuits and Systems, Vol. III, pp. 403-406, May 28-31, 2000.

[4] Ismail.Y. I, E.G. Friedman, and J.L.Neves "Exploiting On-Chip Inductance in High Speed Clock Distribution Networks" Proceedings of the IEEE Workshop on Signal Processing Systems, pp. 643-652, Oct. 2000.

[5] Kahng. A. B, and S. Muddu "An Analytical Delay Model for RLC Interconnects" In Proceeding IEEE Interconnection Symposium Circuits and Systems, May 1996,Vol.IV, pp. 237-240; see also A. B. Khang and S. Muddu "Accurate Analytical Delay Models for VLSI Interconnection", Sept. 1995.

[6] Ismail. Y. I, and E. G. Friedman "DTT:Direct Truncation of the Transfer Function-An Alternative to Moment Matching for Tree Structured Interconnect" IEEE Transaction Computer-Aided Design of Integrated Circuits and Systems, Vol.21, pp 131-144, Feb. 2002.

[7] Masud. H, and Y. I. Ismail "Performance Analysis of Deep Submicron VLSI Circuits

in the Presence of Self and Mutual Inductance" IEEE, Vol. IV, pp. 197-200. 2002.

[8] Horowitz. H. A "Timing Models for MOS Circuits" PHD Thesis, Stanford University-Janury 1989.

[9] Rubinstein. J, P. Penfield and M. A. Horowitz "Signal Delay in RC Tree Networks" IEEE Transaction on CAD-2, July 1983, pp. 202-211.

[10] Zhou. D, S. Su, F. Tsui, D. S. Cong "Analysis of Tree of Transmission Lines". Computer Since Department, TR CSD-920010, UCLA, March 1992 (also to a paper, as "Simplified Synthesis of Transmission Lines with A Tree Structure". International Journal on Analog Integrated Circuits and Signal Processing (Special Issue on High-Speed Interconnects), 1993).

[11] MsCormick. S. P "Modeling and Simulation of VLSI Interconnects with Moments" Ph.D. Thesis,MIT,June 1989.

[12] Zhou. D, F. Tsui and D. S. Gao "High Performance Multichip Interconnection Design" Proceeding of the 4th ACM / SIGDA VLSI Physical Design Workshop, April 1993, pp. 32-43.

[13] Zhou. D, S. SU, F. Tsui, D. S. Gao, and J. S. Cong "A Simplified Synthesis of Transmission Lines with a Tree Structure" International Journal Analog Integrated Circuits Signal Process, Vol.5, pp. 19-30,January 1994.

[14] Elmore. W. C "The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifiers" Jouranl Application Physics, Vol.19, pp. 55-63, Jaunary 1948.

[15] Cong. J and L. He "Optimal Wire Sizing for Interconnects with Multiple Sources" Proceeding of the IEEE / ACM Design Automation Conference, pp. 568-574, Nov.1995.

[16] Nagel. L. W "SPICE2: A Computer Program to Simulate Semiconductor Circuits" University of California, Berkeley, CA, Technical Reptort ERLM520, May 1975.

[17] Boese. K. D, A. B. Kahng, B. A. McCoy, and G. Robins "Fidelity and Near-Optimality of Elmore-Based Routing Constructions" Proceeding of the IEEE International Conference Computer Design, pp. 81-84, Oct. 1993.

[18] Cong. J, A. B. Kahng, C. koh, and C. W. A. Taso "Bounded-Slew Clock and Steiner Routing under Elmore Delay" Proceeding of the IEEE International Conference Computer-Aided Design, pp. 66-71. Jan. 1995.

[19] Rubinstein. J, P. Penfield, and M. Horowitz "Signal Delay in RC Tree Networks" IEEE Transaction Computer-Aided design, Vol. CAD-2, pp. 202-211, July 1983.

[20] Ginneken. L. P. "Buffer Placement in Distributed RC-Tree Networks for Minimal Elmore Delay" In Proceeding IEEE Interconnection Symposium Circuits and Systems, pp. 865-868, May 1990.

[21] Kahng. A. B, and S. Muddu "An Analytical Delay Model for RLC Interconnects" IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Vol.16, no.12, Dec. 1997.

[22] Pillage. L. T, and R. A. Rohrer "Asymptotic waveform evaluation for timing analysis" IEEE Transaction Computer-Aided Design, Vol.9, pp. 352-366, April 1990.

[23] Krauter. B, R. Gupta, J. Willis, and L. T. Pileggi "Transmission Line Synthesis" International Proceedings 32nd ACM / IEEE Design Automation Conference, pp. 358-363, June 1995.

[24] kahng. A. B, and S. Muddu "An Analytical Delay Model for RLC Interconnects" In Proceeding IEEE Interconnection Symposium Circuits and Systems, Vol. IV, pp.237-240,

May 1996.

[25] Krauter. A. et al. "High-Speed Signal Propagation on Lossy Transmission Lines" IBM J. Res. Develop, Vol.34, no.4, pp.601-615, July 1990.

[26] Ismail. Y. I, and E. G. Friedman "Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits" Intnational Proceedings of the IEEE / ACM Design Automation Confernce, pp.721-724, June 1999.

[27] Nekili. M, and Y. Savaria "Parallel Regeneration of Interconnection in VLSI&ULSI Circuits" IEEE International Symposium on Circuits and Systems, Chicago, Illinois, May 3-6, 1993.

[28] Awwad. F. A, and M. Nekili "Regeneration Techniques for RLC VLSI Interconnect" Proceeding of the International Conference on Microelectronics, Morocco, pp.209-212, Oct. 2001.

[29] Secareanu. R. M, and E. G. Friedman "Transparent Repeaters" Proceedings of the IEEE Great Lakes Symposium on VLSI, pp.63-66, March 2000.

[30] Secareanu. R. M, and E. G. Friedman "Applying Analog Techniques in Digital CMOS Buffers to Improve Speed and Noise Immunity" Circuits and Systems II. Analog and Digital Signal Processing, Vol.48, no.5, pp.471-481, May 2001.

[31] Awwad. F. R, and M. Nekili "Variable-Segment &Variable-Driver Parallel Regeneration Technique for RLC VLSI Interconnects" Great Lakes Symposium on VLSI."GLSV-LSI", April 2002.

[32] Ron. Ho. et al. "Repeater Insertion in Deep Submicron CMOS: Ramp-Based Analytical Model and Placement Sensitivity Analysis " ISCAS 2000-IEEE International Symposium on Circuits and Systems, Vol III, pp 766-769, May 28-31,2001

[33] Ismail. Y. I, E. G. Friedman, and J. L. Neves "Repeater Insertion in Tree Structured Inductive Interconnects" IEEE Transaction on Circuits and Systems II: Analog and Digital Signal Processing, Vol.48, no.5, pp 471-481, May 2001.

[34] Awwad. F. R, and M. Nekili "Design Of High-Performance VLSI RLC Interconnects" Degree of Master of Applied Science. Concordia University, March 2002.

[35] Meindl. D. et al. "A Stochastic Wire-Length Distribution for Gigascale Integration(GSI)- PartI: Derivation and Validation" IEEE Transaction on Electron Device, vol.45,no.3, March 1998.

[36] Meindl. D. et al. "A Stochastic Wire-Length Distribution for Gigascale Integration(GSI)- Part II: Application to Clock Frequency, Power Dissipation, and Chip Size Estimation" IEEE Transaction on Electron Device, Vol.45, no.3, March 1998.

[37] Dally. W. J "A VLSI Architercture for Concurrent Data Structures" Kluwer Academeci Publishers, 1987.

[38] Matlab 6 from the Math Works Inc.

[39] Awwad. F. R, T. N. Lammoshi, and M. Nekili "Importance of On-Chip Inducatnce in Designing RLC VLSI Interconnects" Proceedings of the International Conference on Microlelectronics, Lebanon, Dec. 2002.

APPENDIX A

A.1. Introduction

This program is about calculating optimal design parameters for the parallel-resistance RC-based repeater VSRT. This is a stand alone program written entirely in Java. In order to run this program, please make sure that you have JDK1.2 or higher.

The main purpose of this program is to calculate three variables named w, y, and z. Considering the transfer function in Equation (4.14). Using this program, there are two functions for every variable to find its value. For example to find the value of z, the main function calls the ZArray( ); then, calculateZ ( ) function. Finally, the value of z will be in calculateZ ( ). Then, the next step is to calculate the poles s_1 and s_2.

A.2. Calculating Optimal Design Parameters

Given an interconnect length and width and a CMOS technology, the program calculates the optimum number of segments, N.

```
mport java.lang.Math;
/*
 * Tawfeeq.java
 *
 * Created on April 1, 2003, 1:27 AM
 */
```

```
/**
 *
 * @author Tawfeeq
 */
public class Tawfeeq
{

   static double δ = 0.007;
   static double l=0.0;
   static int size=0;
   static double Rt=4940;
   static double Ct=17.3 * Math.pow(10,-12);
   static double Lt=47.5 * Math.pow(10,-9);
   static double Cr=7.406 * Math.pow(10,-15);
   static double Y[]= new double[23];
   static double W[]= new double[23];
   static double Z[]= new double[23];
   static int r[]=
   {00000,18096,20517,20925,14188,16093,17376,16835,15974,15501,16972,17085,
    16319,15547,15603,15941,15911,15664,15591,16380,16445,15608,16787};


   /**
```

```
 * @param args the command line arguments
 */
public static void main(String[] args)
{

  if(args.length!=2)
    {
    System.out.println("PLEASE ENTER THE SIZE AND THE l");
  }
     else
     {
    size = new Integer(args[1]).intValue();
            if(size>23)
            {
              System.out.println("SIZE MUST BE LESS THAN OR EQUAL TO 23");
            }
            else
            {
                    δ = new Double(args[0]).doubleValue();
                    WArray();
            calculateW();
            YArray();
            calculateY();
            ZArray();
```

```
                calculateZ();
                }
        }
}
public static void calculateW()
{
   double w=W[1];
   for(int i=2; i<size;i++)
   {
    w = W[i]*w;
   }
   System.out.println("TOTAL w is = " + w);
}
public static void WArray()
{
    System.out.println(1 + "=" + W[1]);
      for(int i=1; i<size;i++)
   {

      W[i]=1+(l+(i-1)*δ)*Rt/r[i];
      System.out.println(i + "=" + W[i]);

   }
}
```

```
*****************************ZZZZZZZZZZZZZZZZZZ*********************
*********************************
   public static void ZArray()
   {
      System.out.println("ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ");
      for(int i=1; i<size;i++)
      {
         Z[i]=((1+(i-1)*δ)*Lt)*(Cr + (1+(i-1)*δ)*Ct);
      }
   }
   /*public static void calculateZ()
   {
      double z=Z[1];
         System.out.println(1 + "=" + Z[1]);
      for(int i=2; i<size;i++)
      {

            z = Z[i]*z;
            System.out.println(z);
         System.out.println(i + "=" + Z[i]);
      }
```

```
    System.out.println("TOTAL z is = " + z);
    System.out.println("ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ");
  }*/

**********YYYYYYYYYYYYYYYYYYY**********
**************************************

  public static void YArray()
  {

Sytem.out.println("YYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYY")
;
    for(int i=1; i<size;i++)
    {

      Y[i]=((l+(i-1)*δ)*Lt/r[i])+(Cr+(l+(i-1)*δ)*Ct)*(l+(i-1)*δ)*Rt;

    }
  }
  public static void calculateY()
  {
    double y=Y[1];
```

```
        System.out.println(1 + "=" + Y[1]);


      for(int i=2; i<size;i++)
      {
        y = Y[i]*y;
        System.out.println(i + "=" + Y[i]);
      }
      System.out.println("TOTAL y is = " + y);
                                                                                Sys-
tem.out.println("YYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYYY");


   }



   // Java Document



  public static void calculateZ()
  {
        double z = 0.0 ;
        for(int index =1; index <size; index++)
        {
          z = z + AddRows(index);
        }
```

```
        System.out.println("TOTAL z is = " + z);
    System.out.println("ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ");
}

public static  double AddRows(int zIndex)
{
        System.out.println("ZINDWEX IS " + zIndex);
        double total=calculateFirstWRow(zIndex) ;
        if(zIndex != size-1)
        {
         int y1 = zIndex;
         double y1Value= Y[y1];
         int y2 = y1+1;
         double y2Value = Y[y2];
         double result=0.0;
         System.out.println(" y1 = " + y1 + " y2 is " + y2);
         for(int index = zIndex; index <size; index++)
         {

          result = multipleWs( y1,  y1Value,  y2,  y2Value) ;
          if(y2!=size-1)
          {
           y2++;
           y2Value=Y[y2];
```

```
            }


            total = total + result;
           }
          }
    return total;
}
public static double multipleWs(int y1, double y1Value, int y2, double y2Value)
{
        double result = 1;
        for(int index = 1; index <size; index++)
        {
         if(y1==index)
       {
           result = result * y1Value;
         }
       else if(y2 == index)
       {
         result = result * y2Value;
       }
       else
       {
        result = result * W[index];
       }
```

```
    }
    return result;
  }

  public static double calculateFirstWRow(int zIndex)
  {
    double result =1;
    double zValue=Z[zIndex];
    for(int index =1; index <size; index++)
    {
     if(index==zIndex)
     {
      result = result * zValue;
     }
     else
     {
      result = result * W[index];
     }
    }
    return result;
  }
}
```