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Canada

AN ON-LINE UPS WITH IMPROVED INPUT-OUTPUT CHARACTERISTICS

Yu Lin

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

for the Degree of Master of Applied Science at

Concordia University

Montreal, Quebec, Canada

April 1993

ISBN 0-315-84703-4

ABSTRACT

AN ON-LINE UPS WITH IMPROVED INPUT-OUTPUT CHARACTERISTICS

Yu Lin

Standard uninterruptible power supply (UPS) systems are connected in series between the ac mains and the critical load. A phase controlled rectifier feeds a battery-supported dc bus and an inverter supplies the load. These systems require two conversion stages thus reducing operating efficiency. Moreover, input power factor is poor and large harmonic currents are injected into the ac mains. The proposed topology overcomes these drawbacks by placing the inverter-battery subsystem in shunt between the ac mains and the load. The battery is charged through the inverter dc bus. In normal operation, the ac mains feeds the load directly, and the inverter supplies only the amount of reactive power required to regulate the load voltage and to maintain the power factor very close to unity. When the ac mains fails, the solid state breakers, which connect ac mains to the load, open automatically, and the load is supplied by the battery, through the inverter. The proposed system has the following advantages : a near unity power factor, reduced line current harmonics and higher efficiency. Furthermore, unlike other proposed one conversion stage UPS systems, the proposed structure has the capability of automatic compensation for line or load unbalance. The thesis presents a complete analysis of both the steady state operations and the dynamic performances of the proposed system, with simulation and experimental verifications

ACKNOWLEDGMENTS

I wish to express my gratitude to my research supervisors Dr Géza Joos and Dr. James F. Lindsay for their friendship, valuable guidance and support during the course of this study.

I wish to thank Dr. Phoivos D. Ziogas for his advice of the paper published in APEC'92 that forms an essential part of this thesis work.

Special gratitude to Dr. Hua Jin for his suggestions and grammatical correction of the thesis.

I want to acknowledge the financial support provided by the National Science and Engineering Research Council of Canada through the NSERC grants and by the Government of Quebec through the FCAR grants.

Special thanks to Mr. Joseph Woods, Mr. Donato Vincenti, and Mr. Alexandre Campos for their laboratory assistance, Mr. Vassilios G. Agelidis and Mr Manish Pande for their assistance in written English, and Mr. José Espinoza for his word processing assistance.

Thanks are due to my friends and research colleagues, Atluri Ramaprasad, Lautaro Salazar, Navid Zargari, Ceasar Braz, Jean-Pierre Vandelac, Gerry Moschopoulos, Allen Insleay, Mohsen Jalali, Luiz Lopes and Ying Wang, in the Power Electronics Laboratory for the interesting discussions we shared.

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LIST OF PRINCIPAL SYMBOLS

C_2	load filter capacitor
C_{dc}	dc bus filter capacitor
d_a, d_b, d_c	three phase switching functions of the sine PWM voltage source inverter for the fundamental frequency
d_d, d_q	d axis and q axis components of the three phase switching functions
$\hat{d}_d$, $\hat{d}_q$	variations of the d axis and q axis components of switching functions
E	Battery voltage
f_o	fundamental frequency (60 Hz)
f_s	switching frequency
$G_C(s)$	transfer function of the lag / lead network
$G_{PI}(s)$	transfer function of the PI element
I_l	ac mains line current
i_{la}, i_{lb}, i_{lc}	three phase ac mains line currents
i_{ld}, i_{lq}	d axis and q axis components of the three phase ac mains line currents
I_{a2}, I_{b2}, I_{c2}	three phase negative sequence components of load currents
$\hat{i}_d$	variation of the d axis component of the ac mains currents
$\hat{i}_q$	variation of the q axis component of the ac mains currents
i_E	battery charging current
I_1	the fundamental component of the inverter output line current
I_L	load current
$I_{i,k}$	kth harmonic component of the inverter output line current
$I_{L,k}$	kth harmonic component of the load current

$I_{Ldc,k}$	kth harmonic component of the battery charging current
k	order of the harmonic component
k_i	ripple factor of the battery current
k_I	integral factor of the PI regulator
k_P	proportional factor of the PI regulator
k_v	ripple factor of the dc bus voltage
L_1	link reactor
L_2	load filter inductor
L_{dc}	dc bus filter inductor
M	modulation index
ΔM	modulation index variation
P	real power supplied by the ac mains
P_{INV}	inverter capacity
Q_{XC2}	power rating of the load filter capacitor
Q_{XCdc}	power rating of the dc bus filter capacitor
Q_{XL1}	power rating of the link reactor
Q_{L2}	power rating of the load filter inductor
Q_{XLdc}	power rating of the dc bus filter inductor
R_1	equivalent resistance for the link reactor losses
R_2	equivalent resistance for the load filter losses
R_{dc}	equivalent resistance for the losses of battery and dc bus filter
R_L	load equivalent resistance
s	Laplase calculator
T	d-q-o transformation matrix
THD_{il}	total harmonic distortion of the ac mains line current
THD_{iL}	total harmonic distortion of the load current
THD_{vL}	total harmonic distortion of the load voltage

V_1	ac mains line to neutral voltage
v_{1a}, v_{1b}, v_{1c}	ac mains three phase line to neutral voltages
v_{1d}, v_{1q}	d axis and q axis components of the ac mains line to neutral voltages
V_{a2}, V_{b2}, V_{c2}	three phase negative sequence components of ac mains voltages
v_{dc}	dc bus voltage
V_{dc}	dc component of the dc bus voltage
$\tilde{v}_{dc}$	dc bus voltage variation
ΔV_{dc}	dc bus voltage variation (in frequency domain)
$V_{dc,k}$	*k*th harmonic component of the dc bus voltage
V_i	the fundamental component of the inverter output line to neutral voltage
$V_{i,k}$	*k*th harmonic component of the fundamental component of the inverter output voltage
V_L	load voltage (line to neutral)
V_{Lab}	load voltage (line to line)
$V_{L,k}$	the *k*th harmonic component of the load voltage
X_{C2}	reactance of the load filter capacitor
X_{Cdc}	reactance of the dc bus filter capacitor
X_L	load equivalent reactance
X_{L1}	reactance of the link reactor
X_{L2}	reactance of the load filter inductor
X_{Ldc}	reactance of the dc bus filter inductor
Z_L	load impedance
α	a parameter of the lag / lead network
τ	a parameter of the lag / lead network
ω_o	fundamental frequency (ac mains frequency)
ω_b	break frequency of the system transient response

ω_{pI}	break frequency of the PI regulator
δ	phase shift angle between ac mains voltage and the fundamental component of the inverter output voltage
$\hat{\delta}$	phase shift angle variation
$\Delta\delta$	phase shift angle variation in frequency domain
ϕ	the angle between ac mains voltage and line current

CHAPTER 1

INTRODUCTION

1.1 Introduction

Today, critical equipments, such as computers and communication equipments, are playing more and more important role in the social economic activities Their malfunction or shutdown could result in considerable losses. For example, one interruption of a daily transfer of funds from a bank to the Federal Reserve (in U.S A.) because of a power disturbance to the bank's computer can cost the bank in loss of interest more than the uninterruptible power supply designed to prevent the problem Meanwhile, the critical equipments are considerably more sensitive to power quality than that of the past [1]. They require very clean and continuous power supply to guarantee their sound operation [2]. However, the commercial power sources are often polluted by many types of power disturbances that come from the load environment. For example, rectifier fed dc motors inject harmonic currents into the ac mains; the start or the stop of high power machines causes the temporary line undervoltage or line overvoltage. Moreover, ac mains interruption could happen at any time due to some unpredictable causes Therefore, the critical equipments require proper designed power conditioners to protect them [3] [4]

Although there are various power conditioners available, many of them address only certain types of power disturbances. They cannot satisfy the requirements of the critical equipments that are very sensitive to the power waveform Fortunately, uninterruptible power supplies (UPSs) have the capability of providing the load with clean and continuous power, and are therefore widely used.

The characteristics of the UPSs depend upon their topologies and their control

systems [5]. The increasingly stringent requirements of power quality have motivated the development of high performance UPSs.

1.2 Power quality problems and solutions

1.2.1 Power quality problems

A major study of U.S. commercial ac power by Bell Telephone laboratories has found that over 100 disturbances occurred per year on the average. A study by General Electricity suggests that a major disturbance occurs once per day on the average. Another major study by the Institute of Electrical and Electronic Engineers has also discovered that about 100 to 1000 spike/surges related disturbances are recorded each year [6].

Basically, power disturbances are classified into three types [6], Fig. 1.1.

Type I disturbances include spike and noise. Typically they come from lighting or power network switching.

Type II disturbances are momentary undervoltage or overvoltage. They occur in the events of power system failure, large load change and utility equipment malfunction.

Type III disturbances concern sustained undervoltage, brownout and blackout. The causes of them may be overload, power system failure, extreme unacceptable load change and severe equipment malfunction.

Depending on their severity, the disturbances may cause malfunction, shutdown, or damage on the equipments.

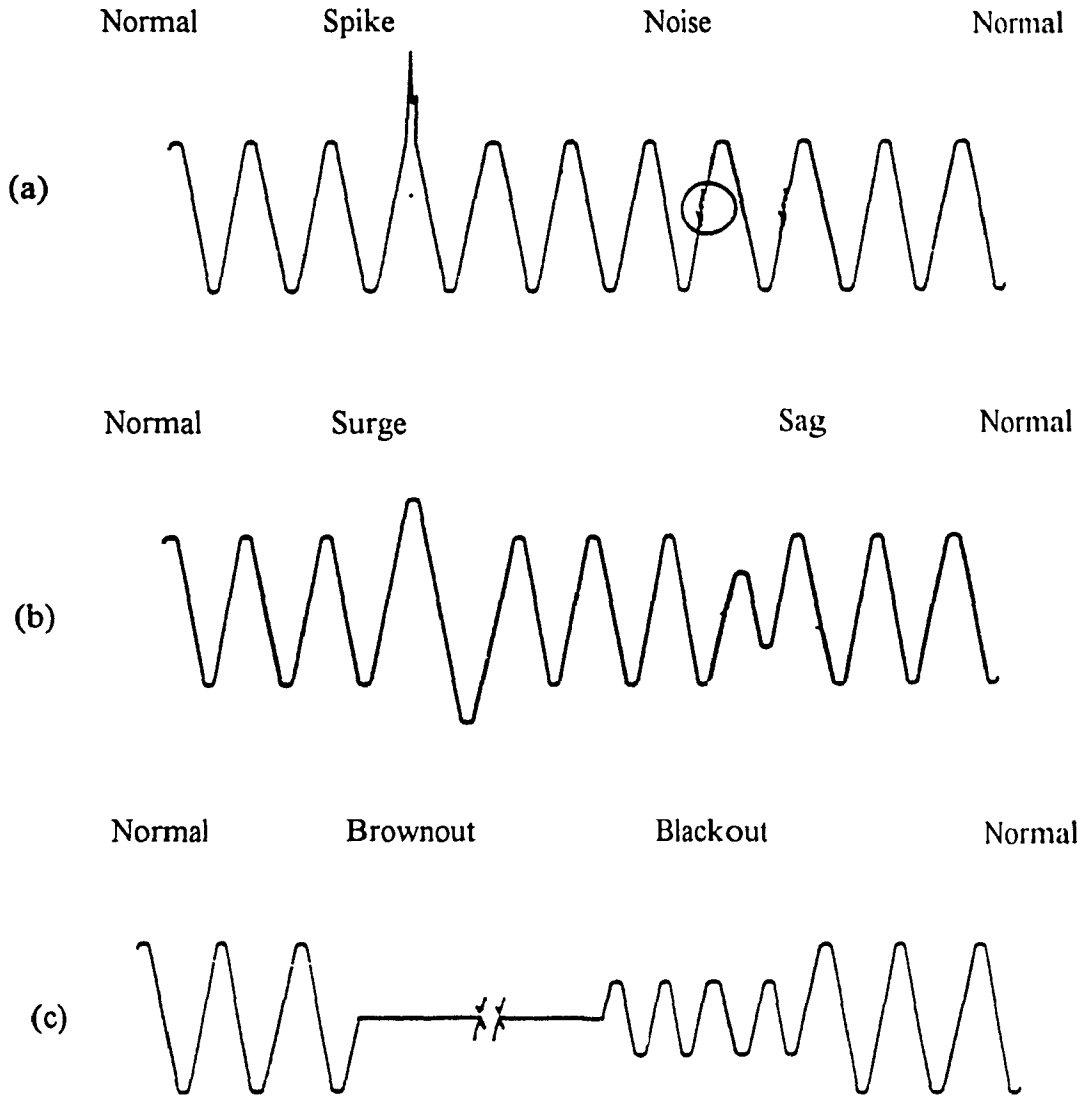


Fig. 1.1 Types of power disturbances

(a) Type I disturbances.

(b) Type II disturbances

(c) Type III disturbances.

1.2.2 Power conditioners

A range of power conditioning equipments has been used to overcome the problems associated with power disturbances. Most of the conditioners, however, have limited protection abilities. They can only protect the load from certain types of power disturbances A brief introduction to these equipments in the following illustrates the effectiveness of their solutions to the various potential power quality problems.

a) Transient suppressors

They are low cost, small size devices. They can absorb or clamp transient voltage spikes Some transient suppressors, like lightning arrestors, have also the function to lower the transient energy to an acceptable level. Most of the expensive power conditioners, such as line voltage regulators, static switches and UPSs, have these devices built in.

b) Filters

They are used to reduce electromagnetic interference (EMI) and/or radiofrequency interference (RFI). Because of the small size and low cost, they are built into a lot of electrical equipments and other expensive power conditioners .

c) Isolation transformers

They provide galvanic isolation between input circuit and output circuit. Because of the isolation, they have spike attenuation function. In addition, they are capable of eliminating the common-mode noise problem that is induced through the "ground loop" [6].

d) Voltage regulators

Voltage regulators have the ability to provide the load with a constant voltage regardless the variations of the source voltage. Several solid-state techniques have been developed in recent years to achieve a fast load voltage regulation responding to the input voltage variations. The abilities of voltage regulators to reduce spikes, noises and surges, however, are limited and to a large extent depend upon their design.

e) Motor generators

Motor generators had been widely used before the static power conversion equipments were introduced. They consist of an electric motor driving an ac generator so that the load is electrically isolated from the power line. However, because of the low efficiency, large weight/power ratio, and regular maintenance, they have been replaced by other types of conditioners.

f) Uniterruptible power supplies (UPSs)

Properly designed UPSs can protect the load completely from any type of power disturbances. Today, UPSs make full use of the advantages from the properties of the fast-speed solid-state semiconductors and modern control techniques to achieve high performances. For critical equipments, UPSs are the best solution.

1.3 Solid state UPS systems

1.3.1 Configurations

Basically, there are three general configurations of solid state UPS systems [6], Fig. 1.2, namely :

- -- line preferred UPS,
- -- inverter preferred UPS, and
- -- line interactive UPS.

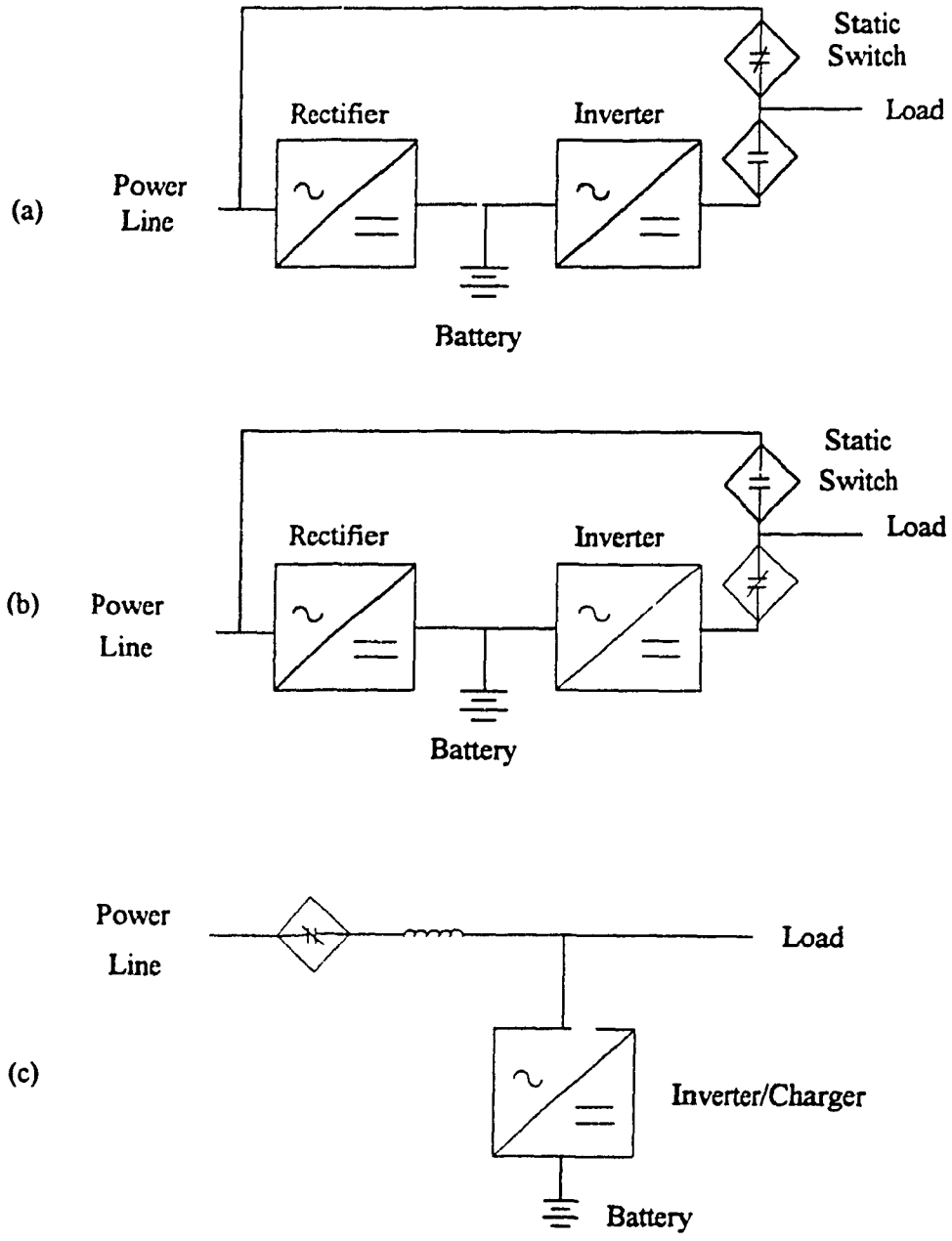


Fig. 1.2 Basic UPS configurations.

(a) Line preferred UPS.

(b) Inverter preferred UPS.

(c) Line interactive UPS.

a) Line preferred UPS

A line preferred UPS comprises a rectifier, an inverter, a battery and a static transfer switch, Fig 1.2(a). In the normal operating conditions, the load is powered by the incoming line directly through the transfer switch. The rectifier is floating - charging the battery and energizing the inverter. In the case of ac mains failure, the static switch transfers the load to the phase - synchronized static inverter, which continues powering with the energy stored in the battery. The transfer delay is so small that the phase distortion is avoided [7]. After ac mains resumes, the load is switched back to the line without phase discontinuity. The main advantage of line preferred UPS is the high operating efficiency due to the small rectifier charging current. However, a line preferred UPS can not isolate the load completely from the line disturbances and is therefore used mainly for the less waveform-sensitive load. Furthermore, without additional device, a line preferred UPS can attenuate neither the harmonic current generated by a nonlinear load nor the negative sequence current caused by an unbalanced load. For the sake of protecting utility environment, it is suitable only for the linear and balanced load

b) Inverter preferred UPS

An inverter preferred UPS is the same as a line preferred UPS in the electrical structure, Fig. 1.2(b). They differ in their operation modes. In the normal operating conditions, the inverter preferred UPS powers the load through the inverter. The rectifier continuously provides the sum of the real power required by the load and the battery recharge. In the case of maintenance or component failure, the load is transferred automatically by the static switch to the line without phase discontinuity. Since the inverter isolates the load from the ac mains completely, no power disturbances can affect the load. For this reason, the inverter preferred UPS is essentially the standard configuration for the critical and waveform sensitive equipment.

c) Line interactive UPS

A line interactive UPS uses only one converter to realize the functions of both rectification and inversion. Consequently, the size of the whole system is reduced, Fig. 1.2(c). In the normal operating conditions, the load is connected to the ac mains through the link reactor; and the converter functions as a rectifier floating - charging the battery. When ac mains fails, the solid state breaker cuts off the line and the converter operates as a voltage source inverter supplying the load with the energy from the battery.

Line interactive UPS is further classified into series processing inverter system and parallel processing inverter system depending on how the inverter is connected, Fig. 1.3.

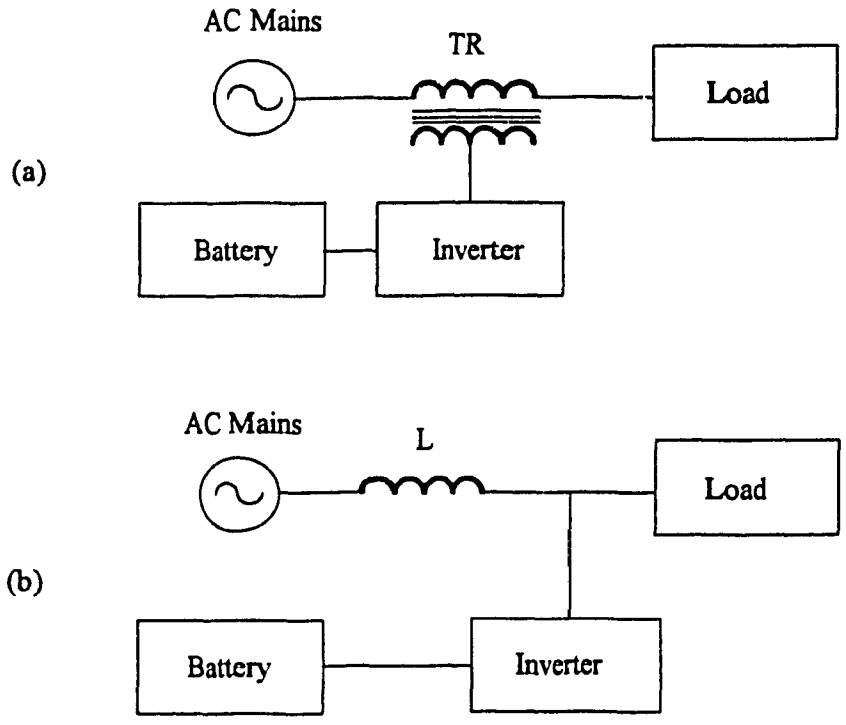


Fig. 1.3 Classification of the line interactive UPS.

(a) Series processing inverter system.

(b) Parallel processing inverter system.

1.3.2 Inverters

To a large extent, the characteristics of UPSs depend on their inverters. Four basic types of inverters are widely used today, namely,

-- square wave inverter;

-- quasi square wave inverter;

-- stepped wave inverter; and

-- pulse width modulated (PWM) inverter.

A square wave inverter comprises an elementary power stage and a ferro-resonant constant voltage transformer that accomplishes voltage regulation, current limitation and filtering, Fig. 1.4. The output voltage waveform is square wave. This type of inverter is the simplest one. However, because of its poor dynamic response, poor efficiency, short magnetic life and large output harmonics, at the present, the application of square wave inverter is generally limited to small power ratings (less than 2 kVA).

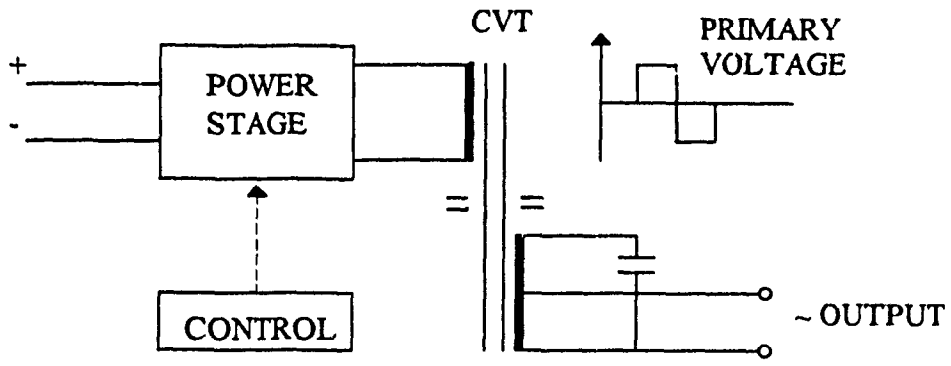


Fig. 1.4 Square wave inverter.

A quasi square wave inverter is essentially a pulse width controlled square wave (quasi) inverter, Fig. 1.5. A nonlinear control system regulates the phase width and an output filter filters out the unwanted harmonics to obtain a sine wave. Control simplicity is

its advantage. Its disadvantages include poor dynamic response and large magnetic components. It is hence used mainly for the loads that can tolerate harmonics (e.g. emergency lighting).

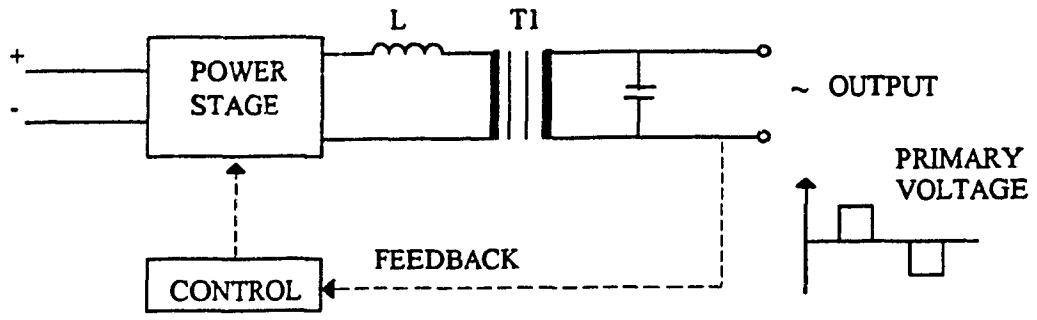


Fig. 1.5 Quasi square wave inverter.

A stepped wave inverter is similar to a quasi square wave inverter except that two or more power stages are combined to produce a primary waveform which approximates sine wave in steps, Fig. 1.6. This type of inverter gives a moderate dynamic response. However, it regulates the output voltage by means of a nonlinear control loop and its output wave shape is determined mainly by a sophisticated output filter. Today it is generally used for large kVA sizes (i.e. above 75 kVA).

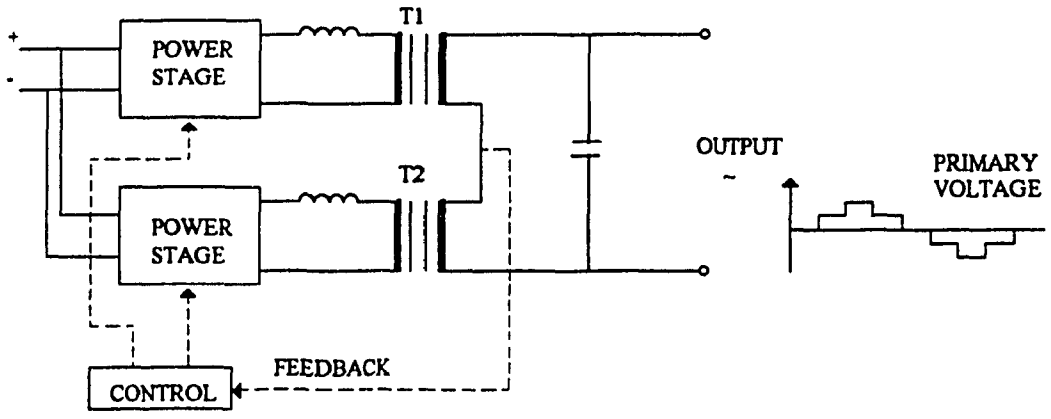


Fig. 1.6 Stepped wave inverter.

A pulse width modulation (PWM) inverter contains a modulation process performed on shaping the inverter ac voltage waveform, Fig. 1.7. It represents the most modern development in the inverter technology. It can provide the best voltage regulation and dynamic performance. Because of its unique capability, it has become the most common selection for various types of UPSs.

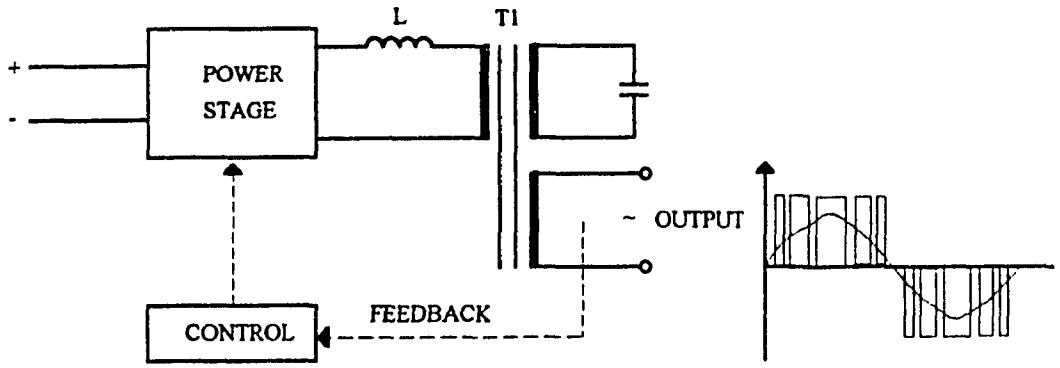


Fig. 1.7 PWM inverter.

Diverse PWM technologies have been developed, the most common one using the carrier type. With the carrier PWM technique, the low order harmonics of the output voltage are eliminated. The high frequency harmonics of the output voltage are lumped around the multiples of the carrier frequency and can be easily filtered out by a simple low pass filter. Moreover, such type of PWM technique allows the output wave shaping to be carried out through linear feedback loops.

1.4 Literature survey

1.4.1 Developments in UPS topologies

Traditional UPSs use the inverter preferred configuration. They provide full isolation and power conditioning. However, the rectifier of the system behaves as a nonlinear load to the ac mains It injects harmonics into ac mains, thus polluting the power system. Moreover, the power factor of the system is usually low because of the rectifier characteristics

One solution of reducing harmonic distortion is to use an additional ac filter. The design of the filter was discussed in [8]. However, the additional component of the ac filter increases not only the total price but also the weight / power ratio of the system.

With the development of high - speed semiconductor devices, diverse types of controlled rectifiers have been used to attenuate the harmonics and correct the power factor. A UPS system using a high - frequency switch mode rectifier was presented in [9]. Through the controlled rectifier, an ac line current with higher power factor and low harmonic distortion was obtained. Also, a three - phase 200 kVA UPS with insulated gate bipolar transistors (IGBT) was studied in [10]. In this system, a controlled charger is used. The charger uses IGBTs that operate at a switching frequency approximately ten times higher than that of the conventional converter. The experimental results show that the ac input current is almost distortion - free (wave distortion factor is 2.4%) and the power factor is high (0.99). However, since the controlled rectifier must supply the full load real current, the operating efficiency of the system is low. Furthermore, if there is no isolation transformer provided in the ac input of the charger, high level switching surges will appear between the inverter output lines and the neutral. Thus an isolation transformer is required between the inverter output and the load to avoid the surge interference, Fig. 1.8 [11].

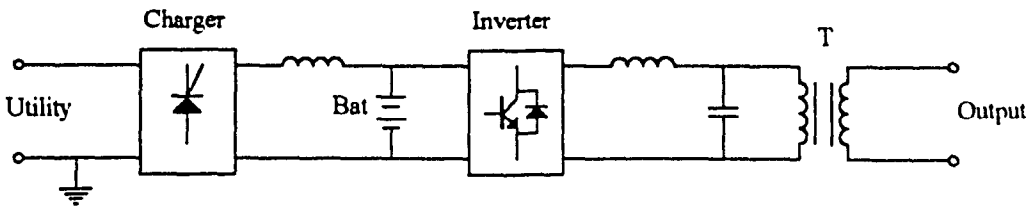


Fig. 1.8 Conventional UPS configuration (with isolation transformer).

In order to improve the system efficiency, a chargerless UPS using multi-functional inverter was proposed in [11]. An inverter is connected in shunt between the ac mains and the load through a L - C filter, Fig. 1.9. A solid state breaker is used to break the ac mains in the case of line failure. In the normal operating conditions, the ac mains supports the load directly and floating - charge the battery through the inverter. Since the converter doesn't provide the real power of the load in the normal operating conditions, the efficiency of the system is high. Furthermore, because the dc link is floating from the neutral, one line of the inverter output can be connected to the grounded line of the ac mains; and a clean output containing no switching surges can be obtained without additional isolation transformer. However, this topology could neither realize load voltage regulation nor isolate the load from the line disturbances.

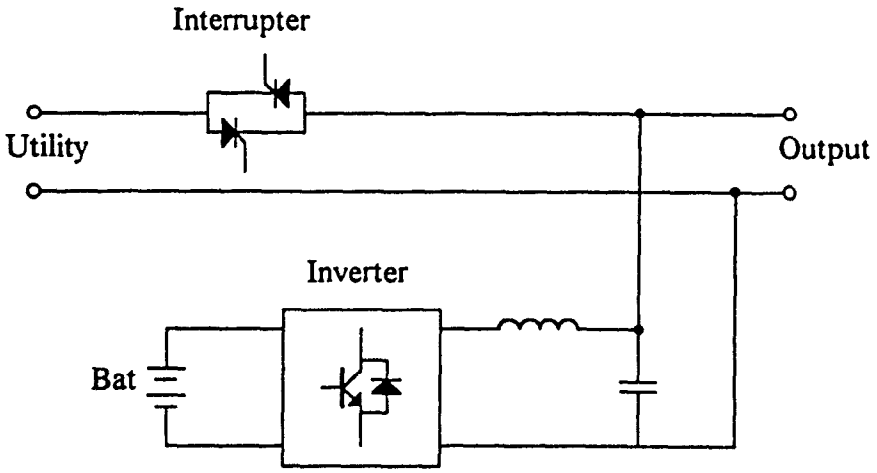


Fig. 1.9 A chargerless UPS configuration.

Another approach of improving the UPS efficiency was reported in [12], Fig. 1.10. A link reactor is added between the ac mains and the load. The load voltage can be regulated by means of the control of the reactive power supplied by the inverter. With a complicated control system, the inverter output instantaneous current and voltage are controlled, and a balanced sinusoidal line current is obtained even under the condition of nonlinear load, unbalanced load or sudden load change.

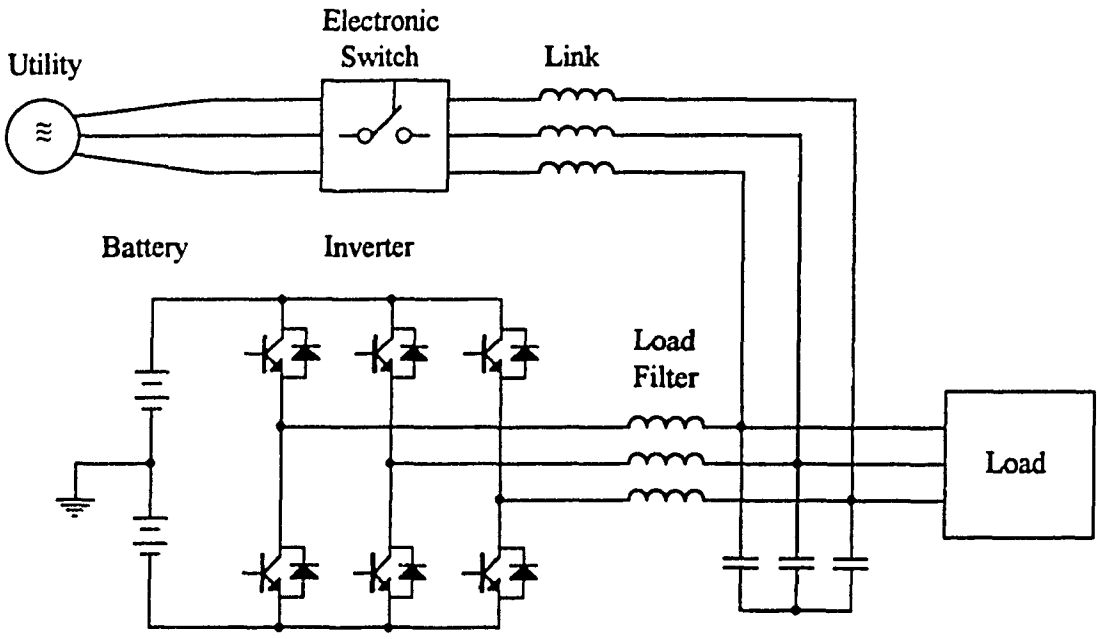


Fig. 1.10 The configuration of a parallel processing inverter system.

1.4.2 Improvements on the inverters

Since the inverter is the most important component of the UPS system, a great deal of studies has been focused on improving the inverter performance.

A paper describing optimum voltage and harmonic control PWM techniques for three phase static UPS was presented in [13]. In this paper, several PWM techniques suitable for three phase static UPSs are analyzed and evaluated. Optimum techniques are

subsequently selected on the basis of the low order harmonic attenuation capability associated with each technique.

State feedback output deadbeat control is an approach to achieve low total harmonic distortion (THD) in the output voltages of PWM inverters [14] [15] [16]. With the applications of microprocessor and digital control technique, the inverter output voltage waveform is shaped. An interesting work has been done in [14] where a modified algorithm of the PWM inverter deadbeat control suitable for UPS systems was presented The experimental results in the paper show that the inverter output voltages contain very small harmonic components.

Another interesting issue is the low output impedance UPS system for nonlinear critical loads [17] [18]. Theoretically, zero output impedance inverter stages provide balanced output voltage independent of the load condition. A qualitative classification of a variety of nonlinear and unbalanced loads was presented in [17]. A topology of a three phase high power inverter with low impedance output characteristic was also presented in the paper.

The previous work was conducted in the range of developing new topology and new control technique of the UPS system. Following the trend, this thesis proposes a topology of line interactive UPS system to improve the input - output characteristics.

1. 5 Scope and objectives

In existing line interactive UPS system [12], Fig 1.10, the compensation of unbalanced load and the elimination of harmonic injection can not be realized by the inverter itself and have to be accomplished through control loops. Therefore, the control system is complicated. Moreover, the capabilities to compensate unbalance and to reject harmonics are limited, especially for the large power rating systems

In order to overcome the main drawbacks of the existing line interactive UPS, a new topology, as shown in Fig. 1.11, is presented, analyzed and verified with simulation

and experimental results in this thesis. The proposed topology itself possesses the capabilities of unbalance compensation and harmonic absorption. The complicated control loops applied in [12] are replaced by simpler loops. The design considerations and the system modeling are also illustrated and verified. In particular, the main objectives of this thesis are :

I) To analyze and verify the feasibility of a parallel processing inverter topology with the characteristics of near unity power factor, low harmonic distortion, high efficiency, and line/load unbalance compensation.

II) To derive dynamic models, which can be used both to design regulators and to analyze the effect of the parameter variations on the system performance.

III) To present the design equations for both the power component ratings and the feedback loop parameters.

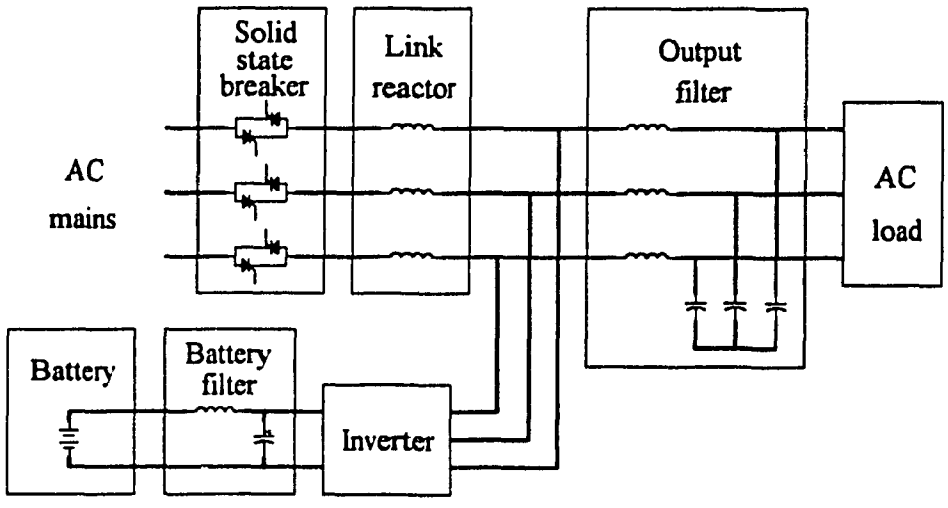


Fig. 1.11 Topology of the proposed UPS system.

1.6 Thesis outline

The content of the thesis is organized as follows:

In Chapter 2, a topology of line interactive UPS system is presented. The principles of the system steady state operation with the characteristics of load voltage regulation, power factor correction, harmonic elimination, and line / load unbalance compensation are described. Based on the predicted operating characteristics, design equations for the circuit component ratings are derived and a design example is given.

The steady state operations of the circuit designed in Chapter 2 are simulated with SPICE to validate the design equations. A 5 kVA, 208V prototype is set up to confirm the simulation results.

In Chapter 3, the control scheme employed in the proposed UPS system is introduced. An example of the control system design is carried out based on the predicted system performance.

Chapter 4 provides simulation and experimental results to confirm the system transient responses predicted in Chapter 3.

In Chapter 5, the summary and the conclusions of the thesis are made. The further works related to the thesis are suggested.

CHAPTER 2

OPERATION PRINCIPLES AND POWER CIRCUIT DESIGN

2.1 Introduction

A new topology of UPS system is presented in this chapter [20]. The new topology uses an inverter connected in shunt between the ac mains and the load, Fig. 1.11. The battery defines the inverter dc bus. Under normal operation, the ac mains feeds the load directly. The inverter supplies only the small amount of reactive power required to maintain the power factor close to unity and to regulate the load voltage. When the ac mains fails, transfer of power is automatic with the load being supplied from the battery fed inverter. The proposed system has the advantages of a near unity power factor, smaller line current harmonics and higher efficiency.

The proposed topology differs from the existing parallel processing inverter system (Fig. 1.10) in the position of the load filter so that the unbalance compensation and the harmonic absorption can be accomplished automatically by the inverter.

The single phase equivalent circuit for normal operation, the equivalent circuit for the negative sequence components, and the equivalent circuit for harmonic components are used in this chapter to illustrate the input - output characteristics of the proposed system. Based on the objectives of the operating characteristics, the power circuit design equations are derived and a design example is processed.

2.2 Power circuit components and connection

The power circuit of the proposed UPS system can be divided into three sections · the three-phase ac section, the three-phase voltage source inverter, and the dc section, Fig. 2.1.

In the three-phase ac section, the following components are used for each phase

-- two solid state breakers,

-- a link reactor, L_1, and

-- a second order load filter L_2, C_2.

In order to eliminate the triplen harmonics, the load filter capacitors are connected in Y.

The dc part consists of the following components :

-- a second order low pass filter L_{dc}, C_{dc}, and

-- a battery.

For each phase, two solid state breakers are connected back to back as a bidirectional switch between ac mains and the other part of the system. The ac terminals of the inverter are connected to the ac mains through the link reactors, and to the three phase load through the load filters. The dc terminals of the inverter are connected to the battery through a filter.

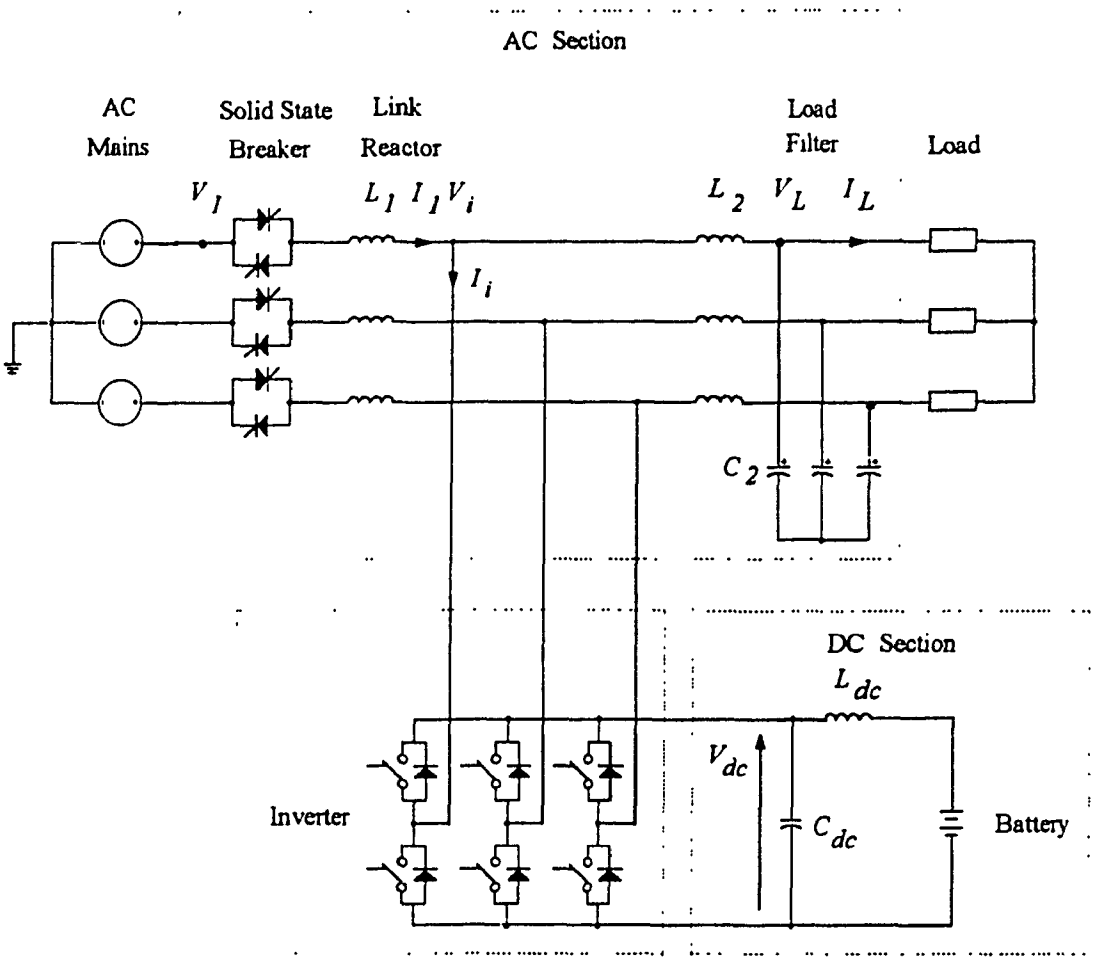


Fig. 2.1 Power circuit of the proposed UPS topology.

2.3 Principles of the steady state operation

Under normal conditions, the solid state line breakers are closed and the ac mains supplies the real power to the load directly (Mode I). The single phase equivalent circuit for the fundamental frequency is shown in Fig. 2.2. The amplitude of the inverter voltage V_i is determined by both the type of the PWM pattern used and the dc bus voltage defined by the battery. V_i can be adjusted independently of the ac mains voltage, which is assumed to vary over a typical range of 90% to 110% (± 10% [1]). Furthermore, the phase angle δ between the ac mains voltage V_1 and the inverter output voltage V_i is determined by the voltage drop across the link reactor. Thus, with the present of the link reactor, the inverter can be used to perform both load voltage regulation and load power factor correction.

The vector diagrams associated with steady state operations are shown in Fig. 2.3 with an assumption that the voltage drop in the load filter L_2 is neglected for the sake of simplification. The load voltage V_L is then equal to the fundamental component of the inverter output voltage V_i.

When ac mains fails, the solid state breakers are opened and the inverter continues to supply the load for a period of time defined by the battery capacity (Mode II).

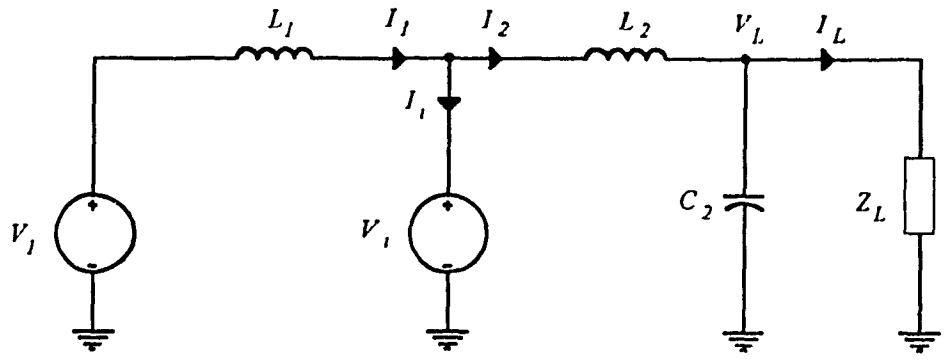


Fig. 2.2 Single phase equivalent circuit for normal operation.

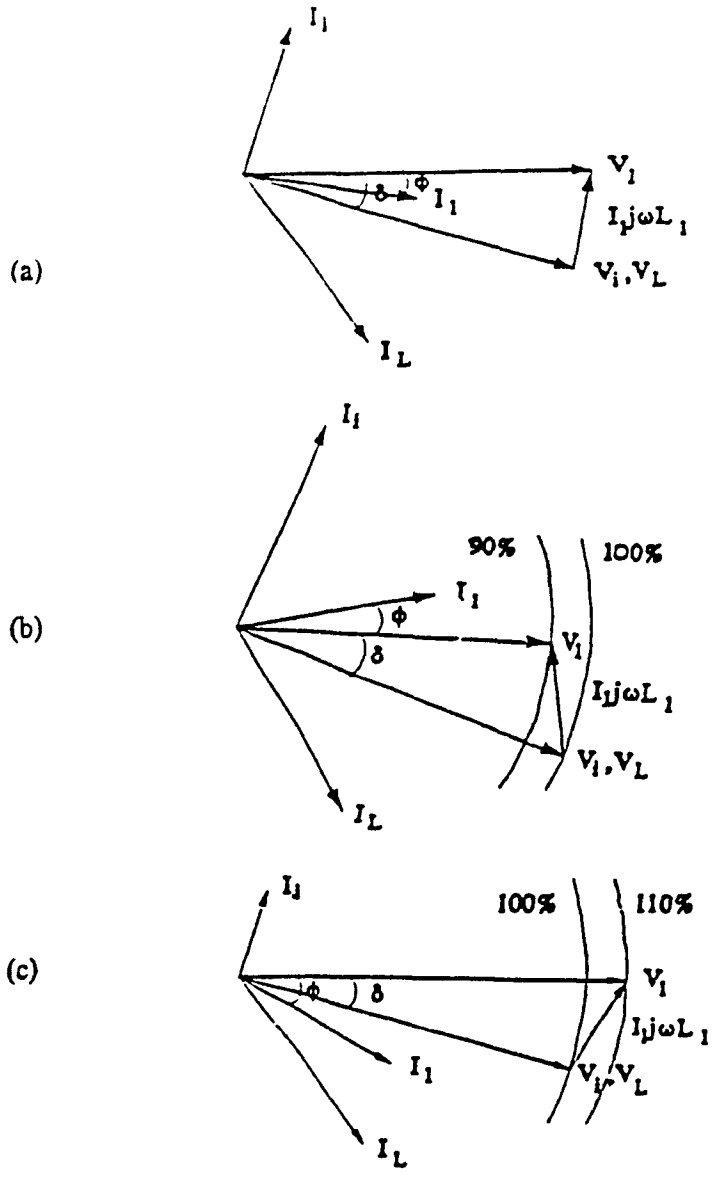


Fig. 2.3 Generalized phasor diagram for inductive load compensation.

(a) Rated ac mains voltage.

(b) 90% rated ac mains voltage.

(c) 110% rated ac mains voltage.

2.3.1 Power factor control

Since in steady state operation, the amplitude of the inverter output voltages are fixed by the battery voltage and the PWM patterns [21], the power transmission of the system from ac mains to the load can be represented by Fig. 2.4. The load angle δ is determined by the real power transferred to the load and is obtained from

$$P = \frac{V_l V_i}{X_{Ll}} \sin\delta \qquad (2.1)$$

Because the link reactor X_{Ll} is usually small (0.3 pu max.), the load angle δ is small under rated load conditions (in the range of 15^{o} or less). The ac mains is assumed to be at the rated value and the inverter voltage is adjusted to this value (Fig 2.3(a)) The power factor, given by cos(δ/2), is therefore very close to unity (0.98 or higher). Thus, adjusting the amplitude of the fundamental component of the inverter output voltage to that of the ac mains results in nearly unity overall power factor, the reactive power being supplied by the inverter.

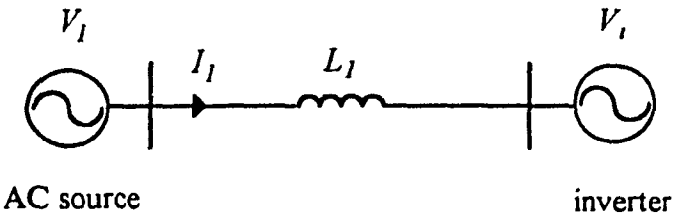


Fig. 2.4 Equivalent circuit, per phase, of UPS system, for power transmission analysis.

2.3.2 *Load voltage regulation*

It is assumed that the amplitude of the fundamental component of the inverter output voltage is kept close to the rated ac mains voltage, in order to regulate the load voltage. The consequences of variations in the ac mains voltage are illustrated in Figs. 2.3(b) and 2.3(c). The inverter supplies more reactive power (for undervoltage) or less reactive power (for overvoltage) required to regulate the load voltage [22]. However, power factor decreases as the ac mains variation increases.

The range of the inverter reactive current required to regulate the load voltage is illustrated in Fig. 2.5. This gives the inverter kVA requirement in the normal operating conditions.

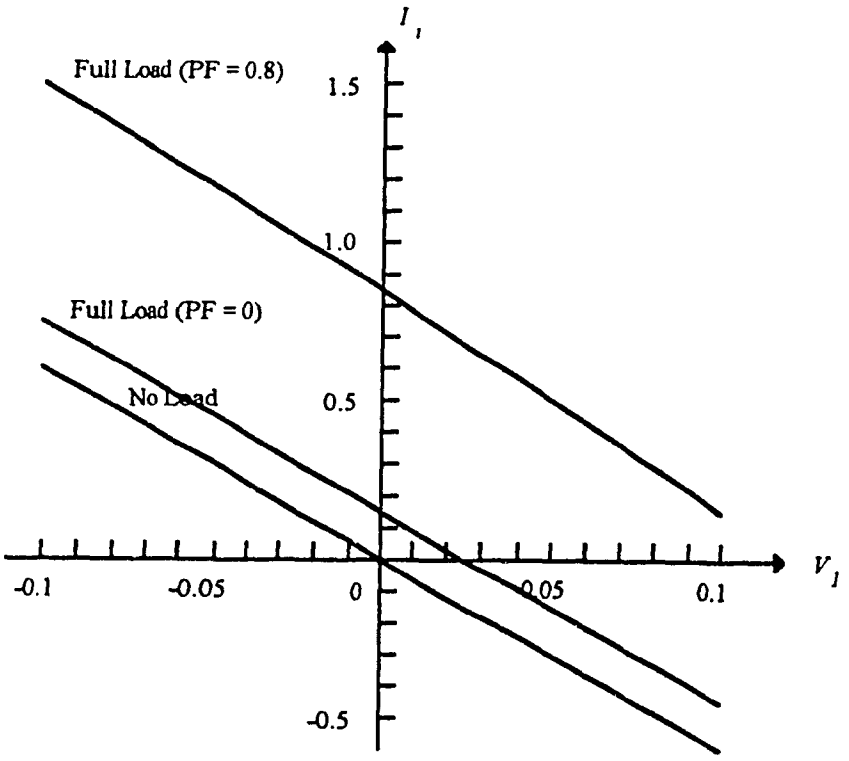


Fig. 2.5 Required reactive power against ac mains voltage variations.

2.3.3 Load and line harmonic absorption

For standard PWM patterns, the inverter output voltage presents a harmonic spectrum containing the fundamental frequency component and higher order harmonics, which are lumped around multiples of the inverter switching frequency [23]. For all other harmonics, it presents a short-circuit (Fig. 2.6). Therefore, all load harmonics, particularly low frequency components, are absorbed by the inverter and do not propagate into the ac mains. The same applies to line harmonics, if they exist.

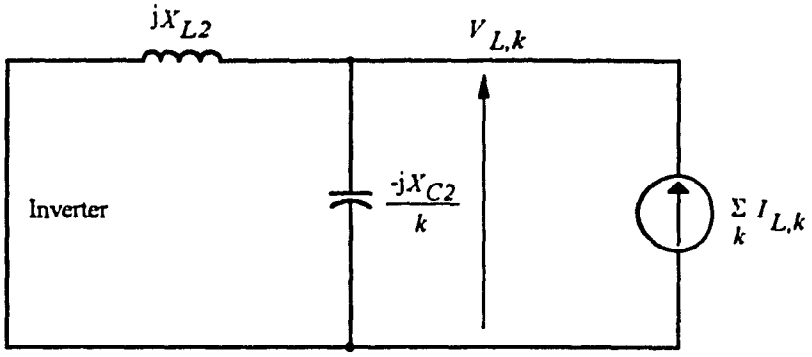


Fig. 2.6 Single phase equivalent circuit for load harmonic components.

Furthermore, since the PWM patterns of the three phase inverter are balanced, the inverter output voltages are sets of balanced three-phase voltages (positive sequence only). Therefore, the inverter behaves as a short circuit for all negative sequence voltage components appearing across its terminals, Fig. 2.7. As a consequence, the load voltages are balanced, even with an unbalanced ac mains. Conversely, an unbalanced load does not result, on the ac mains, in unbalanced line current.

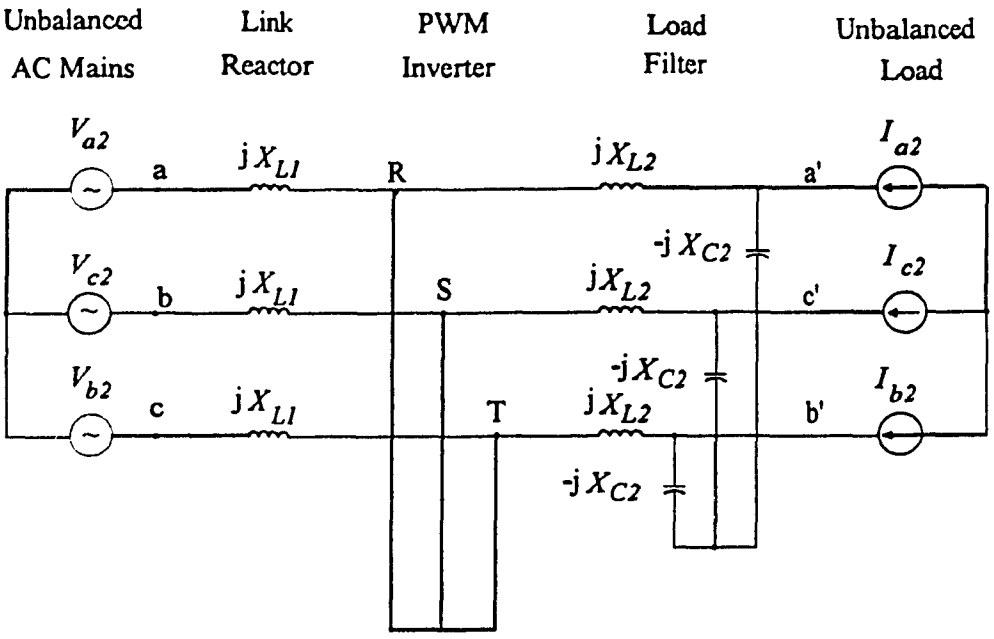


Fig. 2.7 The equivalent circuit for the negative sequence components of ac mains and load.

However, negative sequence voltage components appear entirely across the line reactor L_1 in the case of ac mains unbalance. Therefore, the design considerations for the reactor must include limiting the negative sequence currents, in addition to attenuating the harmonic currents injected into the ac mains [24]. In case of unbalance load condition, the capacity of bearing negative sequence currents should also be taken into consideration of designing the load L-C filter.

Finally, in all cases, negative sequence currents will pass through the inverter, and mainly through the dc filter capacitor. These additional second order harmonic components increase the dc bus ripple and must be taken into account in the design of the capacitor [24].

2.3.4 PWM pattern

Most PWM patterns for voltage source inverters are suitable for UPS applications Some offer advantages, due to the limited range of modulation index used These can be of the carrier or the programmed types.

The advantages of the PWM techniques include the following [25] :

a) No low order harmonic components are contained in the inverter ac voltages.

b) The inverter output voltages are balanced. The inverter appears as a short circuit for negative sequence currents.

The carrier type PWM, offers additional advantage in that all the high order harmonics are lumped around the multiples of the carrier frequency, which is usually much higher than the fundamental frequency, and can be filtered out by a small size filter

In this thesis, a standard sine PWM carrier technique is used

A standard sine PWM pattern is generated by comparing a modulation sine wave with a triangular carrier wave, Fig. 2.8(a). The peak to peak value of the triangular carrier wave is 2 pu. The amplitude of the modulation sine wave is defined as the modulation index, M, which determines the amplitude of the fundamental component of the PWM pattern, Fig. 2.8(a). The phase angle of the modulation sine wave is called the phase shift angle, δ, which determines the phase angle of the fundamental component of the PWM pattern, Fig. 2.8(a).

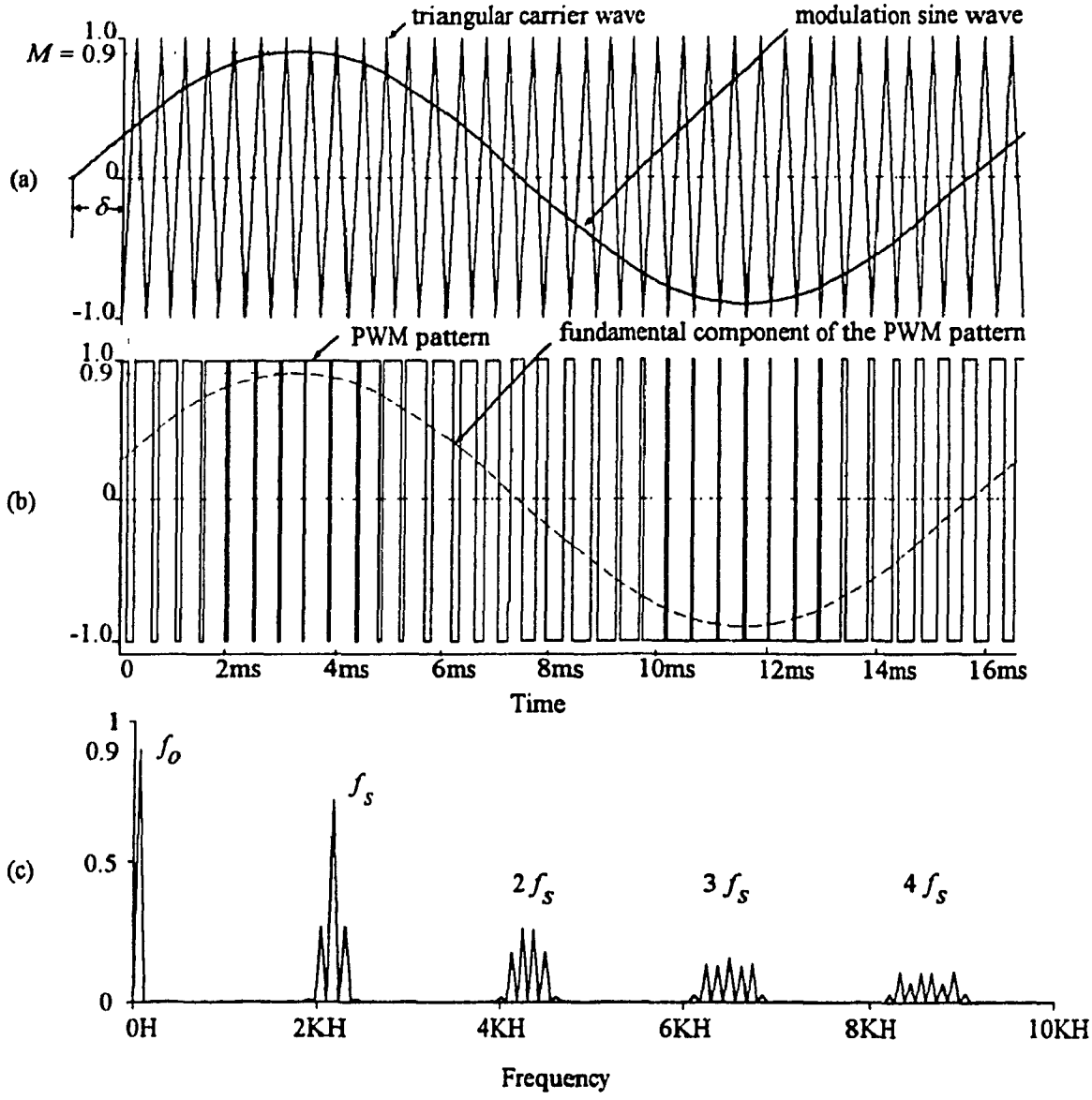


Fig. 2.8 Standard sine PWM pattern.

(a) Triangular carrier wave (f_S = 2160 Hz) and modulation sine wave (M = 0.9, $\delta = 30^o$).

(b) PWM pattern and its fundamental component.

(c) Frequency spectrum of the PWM pattern (f_O = fundamental frequency).

2.3.5 Filtering

The inverter output voltage contains high order harmonics that are filtered out by means of the following, Fig. 2.9 :

-- a first order filter, reactor L_1, on the line side,

-- a second order filter, L_2 - C_2, on the load side.

For a given total voltage or current harmonic distortion, the size of the reactive components, decreases as the inverter switching frequency increases.

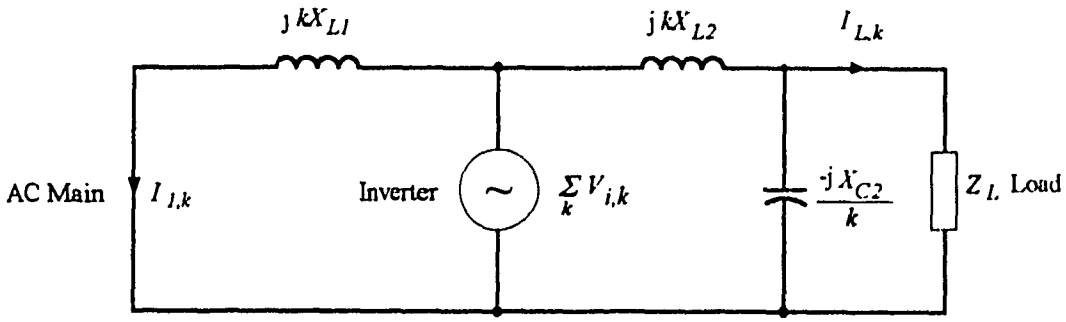


Fig. 2.9 Single phase equivalent circuit for inverter harmonic components.

2.4 Power circuit design

The design of the power circuit is based on the following assumptions :

a) the three ac mains voltages are balanced;

b) the three-phase load is balanced and linear;

c) the inverter switches are ideal;

d) the filter components are purely reactive and linear;

e) the dc bus voltage is ripple-free;

f) the inverter uses a sine PWM switching pattern.

Base values are as follows :

a) $V_{base} = V_{1r}$, the rated value of the ac mains line-to-neutral voltage;

b) $I_{base} = I_{1r}$, the rated value of the fundamental component of the ac mains line current.

c) $f_{base} = 60$ Hz.

The standard to evaluate the harmonics of a waveform is the total harmonic distortion [25], which is defined as the percentage ratio of the equivalent root mean square value (RMS) of all the harmonic components to the RMS value of the fundamental component. That is,

$$THD = \frac{1}{A_1}\sqrt{\sum_{k=2}^{\infty} A_k^2} \cdot 100\% \qquad (2.2)$$

where, k is the order of the harmonic, A_k is the amplitude of the kth harmonic component, and A_1 the amplitude of the fundamental component.

2.4.1 Line reactor design

The reactor is chosen on the basis of the total harmonic distortion of the current flowing through the ac mains : it has to be less than a value specified by documented codes and standards [32] [26]. Since no second or triplen order harmonics exist in the balanced sine PWM patterns, this distortion factor is given by,

$$THD_{i1} = \frac{1}{I_{i,1}}\sqrt{\sum_{k=5}^{\infty} I_{i,k}^2} \cdot 100\% \qquad (2.3)$$

where the current harmonics $I_{1,k}$ are the result of the inverter harmonic voltages $V_{i,k}$, as

shown in Fig. 2.9, and are given by

$$I_{1,k} = \frac{V_{i,k}}{kX_{L1}} \tag{2.4}$$

Therefore,

$$THD_{i1} = \frac{1}{I_{1,1}} \sqrt{\sum_{k=5}^{\infty} \left(\frac{V_{i,k}}{kX_{L1}} \right)^2} \cdot 100\% \tag{2.5}$$

The inverter voltage harmonics are defined by the PWM pattern and can be obtained, by simulation, from the frequency spectrum of the inverter ac voltage.

The negative sequence current component is considered in designing the reactive power rating of the reactor.

The reactive power rating of the reactor is given by

$$Q_{XL1} = X_{L1} I_{1,1}^2 (1 + THD_{i1})^2 \tag{2.6}$$

2.4.2 Load filter design

The purpose of the load filter is to reduce the harmonic content of the load voltage and current resulting from the inverter operation. The effect of the second order filter, L_2-C_2 (Fig. 2.9), depends upon the load impedance. The design criteria are to reduce the total harmonic distortion of the load current, THD_{iL} and of the voltage, THD_{vL}, below specified values (typically 1% and 5% respectively, [32]), under rated load conditions.

Assuming that the load can be represented by an equivalent (R_L, X_L) series circuit, the harmonic components of the current propagating the filter reactor are given by

$$I_{L,k} = \frac{V_{i,k} X_{C2}}{\left(X_{C2} R_L - k^2 X_{L2} R_L \right) + j\left(kX_{L2} X_{C2} - k^3 X_{L2} X_L + kX_L X_{C2} \right)} \tag{2.7}$$

where $V_{l,k}$ is defined by the PWM used.

The total harmonic distortion THD_{iL} is obtained from

$$THD_{iL} = \frac{1}{I_{L,1}} \sqrt{\sum_{k=5}^{\infty} I_{L,k}^2} \cdot 100\% \tag{2.8}$$

The harmonic components of the load voltage are given by

$$V_{L,k} = I_{L,k} \sqrt{R_L^2 + k^2 X_L^2} \tag{2.9}$$

and the total harmonic distortion is obtained from

$$THD_{vL} = \frac{1}{V_{L,1}} \sqrt{\sum_{k=5}^{\infty} V_{L,k}^2} \cdot 100\% \tag{2.10}$$

The kVA rating of the reactor is given by an equation similar to (2.6) and the kVA rating of the capacitor by

$$Q_{XC2} = \frac{V_{L,1}^2 (1 + THD_{vL}^2)}{X_{C2}} \tag{2.11}$$

2.4.3 DC bus filter design

The dc bus voltage consists of high frequency harmonics. In order to protect the battery, a second order low pass filter C_{dc} - L_{dc} (Fig. 2.10) is designed. Moreover, the capacitor C_{dc} also functions as a dc bus voltage regulator; and L_{dc} as a limiter to the

battery charging current.

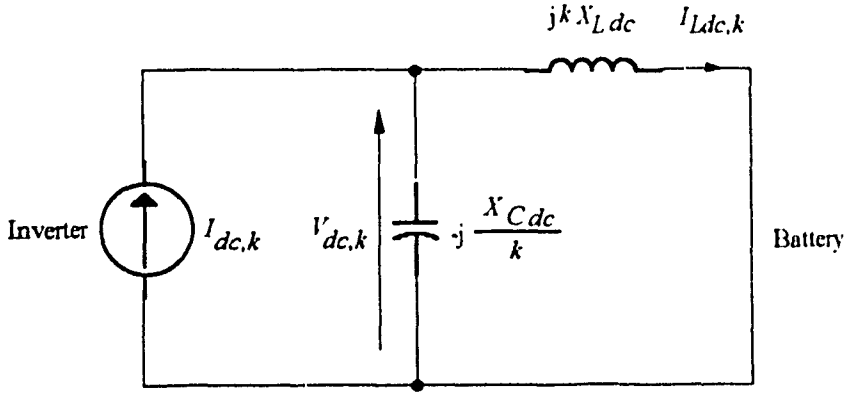


Fig. 2.10 Equivalent circuit of the dc bus for harmonic components.

The design of the dc bus filter is carried out based on the consideration of reducing the dc bus voltage ripple factor k_v and the battery current ripple factor k_i below specified limits (typically 1% and 5% respectively, [32]). The ripple factors are given by

$$k_v = \frac{1}{V_{dc}} \sqrt{\sum_{k=6}^{\infty} V_{dc,k}^2} \cdot 100\% \qquad (2.12)$$

$$k_i = \frac{1}{I_{dc}} \sqrt{\sum_{k=6}^{\infty} I_{Ldc,k}^2} \cdot 100\% \qquad (2.13)$$

where

$$V_{dc,k} = I_{dc,k} \frac{jkX_{Ldc}X_{Cdc}}{X_{Cdc} - k^2 X_{Ldc}} \qquad (2.14)$$

$$I_{Ldc,k} = I_{dc,k} \frac{k^2 X_{Ldc}}{k^2 X_{Ldc} - X_{Cdc}} \qquad (2.15)$$

with ω_o = system frequency

The dc current ripples $I_{Ldc,k}$ are determined by the voltage source inverter and can be obtained, by simulation, from frequency spectrum of the dc bus current.

2.4.4 Inverter rating

The inverter is rated for the worst operating conditions. This occurs when it supplies the load in the case of ac mains failure. Under normal conditions, the inverter only supplies reactive current that never exceed the rated load current (see Fig. 2.6). Standard inverter design principles therefore apply; that is, the inverter is rated for rated load [26].

2.4.5 Design example

The design equations derived above are applied to a 5 kVA, 208 V system. The load has a typical power factor of 0.8 (lagging). The battery voltage is 384 V [33]. The sine PWM with a carrier frequency of 2160 Hz and a modulation index of 0.9 is used in the example. The harmonic distortion factors THD_{vl}, THD_{iL}, and THD_{vL} are chosen as 5%, 1% and 5%, [32]. The ripple factors k_v and k_i are 1% and 5% respectively [32].

The harmonic components of the voltage waveform (line to line) associated with the switching pattern are listed in Table 2.1. The table can be used to calculate the inverter harmonic voltages $V_{l,k}$.

Table 2.1

Frequency Spectrum Of The Voltage (Line to Line)

Waveform Associated With The Switching Pattern

(Modulation Index $M = 0.9$, Switching Frequency = 36 pu)

Order k	Amplitude (percentage)	Order k	Amplitude (percentage)
1	100	110	14
34	29.7	112	14.7
38	29.7	139	12
71	28.3	143	12
73	28.3	145	12
104	14.7	149	12
106	14		

The link reactor data, which are listed in Table 2.2, are obtained from the design equations (2.3) to (2.6). In the normal operating conditions, the voltage drop across the reactor is 0.3 pu (equals X_{L1}). From Fig. 2.3(a), it is obviously that the angle δ is 0.3 radian and the system power factor 0.989.

Table. 2.2

Design Data Of The Link Reactor

X_{L1} (pu)	Q_{XL1} (pu)	THD_{I1}
0.3	0 33	4.4%

With equations (2.7) to (2.11), the second order load filter are designed, as the data listed in Table 2.3. In order to avoid the filter resonance, the resonant frequency of the filter (600 Hz) is designed much lower than that of the lowest order harmonic in Table 2.1, Fig. 2.11.

Table 2.3

Designed Data Of Load Filter

(For Rated Load Power (1 pu) And Rated Load Power Factor (0.8, lagging))

X_{L2} (pu)	Q_{XL2} (pu)	X_{C2} (pu)	Q_{XC2} (pu)	THD_{iL}	THD_{vL}
0 1	0.12	10	0.11	0.2%	4%

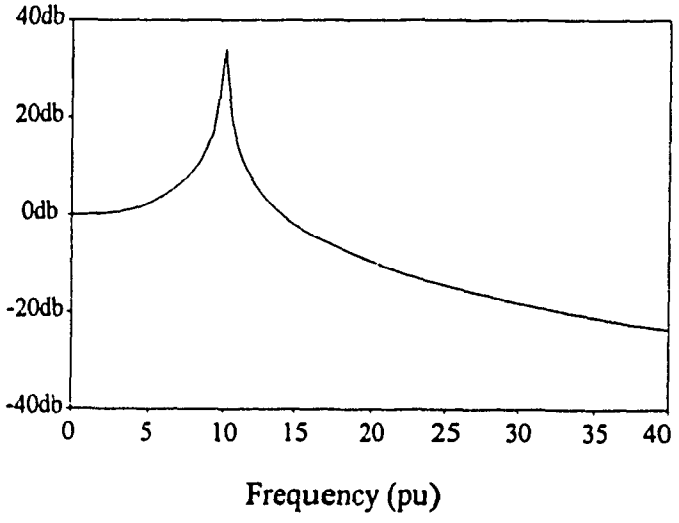


Fig. 2.11 Frequency response of the load filter.

Table 2.4 shows the harmonic amplitudes of the dc bus current associated with the switching pattern used. The table can be used to calculate $I_{Ldc,k}$.

Table 2.4

The Harmonic Amplitudes Of The DC Bus Current Associated With The PWM Pattern Used

Harmonic Order	Amplitude (percentage)	Harmonic Order	Amplitude (percentage)
DC	100	150	370
33	420	210	160
39	820	222	234
105	490	243	169
111	670	261	250
138	240		

Table 2.5 lists the design data of the dc bus filter, which are calculated from the equations (2.12) to (2.16). The resonant frequency of the filter (150 Hz) is designed far away from the harmonic frequency range in Table 2.4 to eliminate the resonant possibility.

Table 2.5

Designed Data Of The DC Bus Filter

Associated With The PWM Pattern Used

X_{Cdc} (pu)	Q_{XCdc} (pu)	X_{Ldc} (pu)	Q_{XLdc} (pu)	k_i	k_v
1.54	0.65	0.25	0.27	4.1%	0.2%

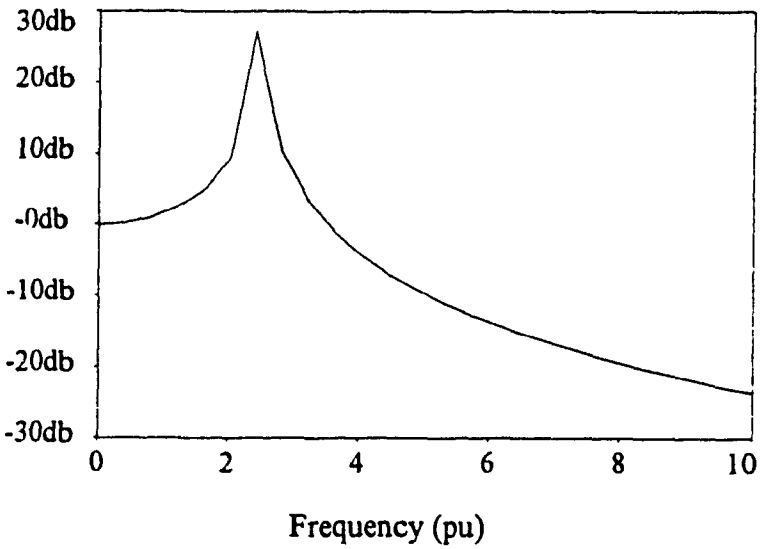


Fig. 2 12 Frequency response of the dc bus filter.

Table 2.6 lists the inverter ratings coming from the standard design principles.

Table 2.6

Voltage Source Inverter Switch Rating (pu)

Peak Current	RMS Current	Peak Forward Blocking Vol.	Peak Reverse Blocking Vol.
1.5	1.0	4.5	4.5

2.5 Conclusions

A new UPS configuration is proposed in this chapter. The general operating principles and the steady state input-output characteristics are discussed Also, the power component design considerations and a design example are given.

The theoretical analyses predict that the proposed topology (as illustrated in the design example) provides the load with a regulated load voltage containing very low harmonic components (THD_{iL} is less than 1% and THD_{vL} less than 5%). Because the inverter compensates the reactive power required by the load, the power factor of the system is high (0.989). The inverter can also absorb the harmonics generated by a nonlinear load so that the ac mains line current is harmonic-free (THD_{iI} is less than 5%) Moreover, the efficiency of the system is high since the inverter does not supply real power to the load. Because of this advantage, the battery energy does not change Consequently, the dc bus voltage and the battery charging current are ripple-free (k_v and k_i are less than 1% and 5% respectively).

CHAPTER 3

STEADY STATE OPERATION

3.1 Introduction

In order to confirm the predicted advantages of the proposed configurations, and to verify the derived power circuit design equations, the proposed UPS system using the data designed in Chapter 2, is simulated using SPICE [31]. The simulation results are provided for the system under the following conditions :

1) normal operating conditions,
2) fluctuations in the ac mains voltage,
3) nonlinear load or nonlinear ac mains,
4) unbalanced load or unbalanced ac mains, and
5) ac mains sudden failure.

The selected simulation results are verified with an experimental 5kVA, 208V prototype.

3.2 Normal operation

For the convenience of analysis, a simulation is carried out under the ac mains with the following assumptions :

1) the ac mains line to neutral voltage $V_1 = 1/\sqrt{2}$ pu;
2) the ac mains line current $I_1 = 1/\sqrt{2}$ pu.

With the assumptions, the amplitude of the ac mains voltage and line current is 1 and the comparison of waveforms becomes easy.

Under the normal operating conditions, the simulation results shown in Figs. 3.1 to

3.3 verify the main design considerations and equations; that is :

-- an inverter output line to line voltage with harmonics lumping around the multiple of the carrier frequency, Fig. 3.1.

-- a near unity power factor (0.989, Fig. 3.2(a));

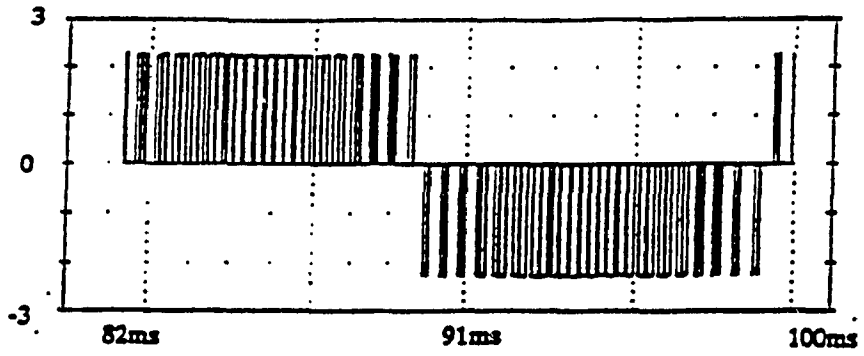
-- very low line current harmonic distortion (less than 5%, Fig. 3.2(b));

-- very low harmonic distortion in the load voltage and the load current (less than 5% and 1% respectively, Fig. 3.3(b) and Fig. 3.3(c));

-- very small dc bus voltage ripple factor and the battery current ripple factor (less than 1% and 5% respectively, Fig. 3.4(c) and Fig. 3.4(d)).

-- high operating efficiency since the battery charging current is very small, Fig.3.4(c).

(a)



(b)

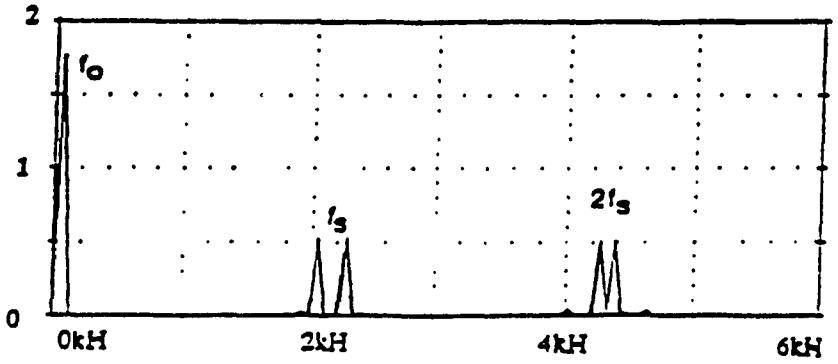
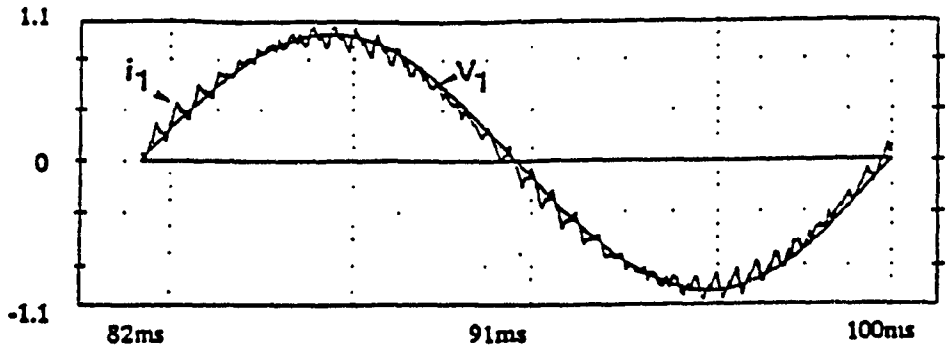


Fig. 3.1 Inverter output line to line voltage (simulation results).

(a) Inverter output line to line voltage (pu).

(b) Frequency spectrum of the inverter output voltage (pu).

(a)



(b)

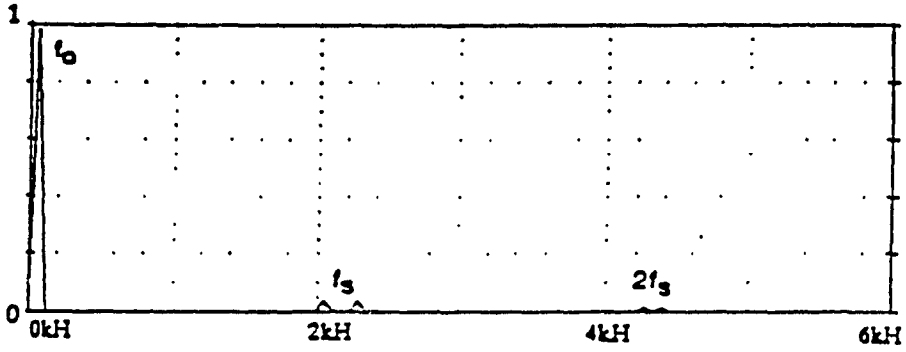


Fig. 3.2 AC mains line to neutral voltage and line current (simulation results, full load, load power factor = 0.8).

(a) AC mains line to neutral voltage and line current (pu).

(b) Frequency spectrum of ac mains line current (pu).

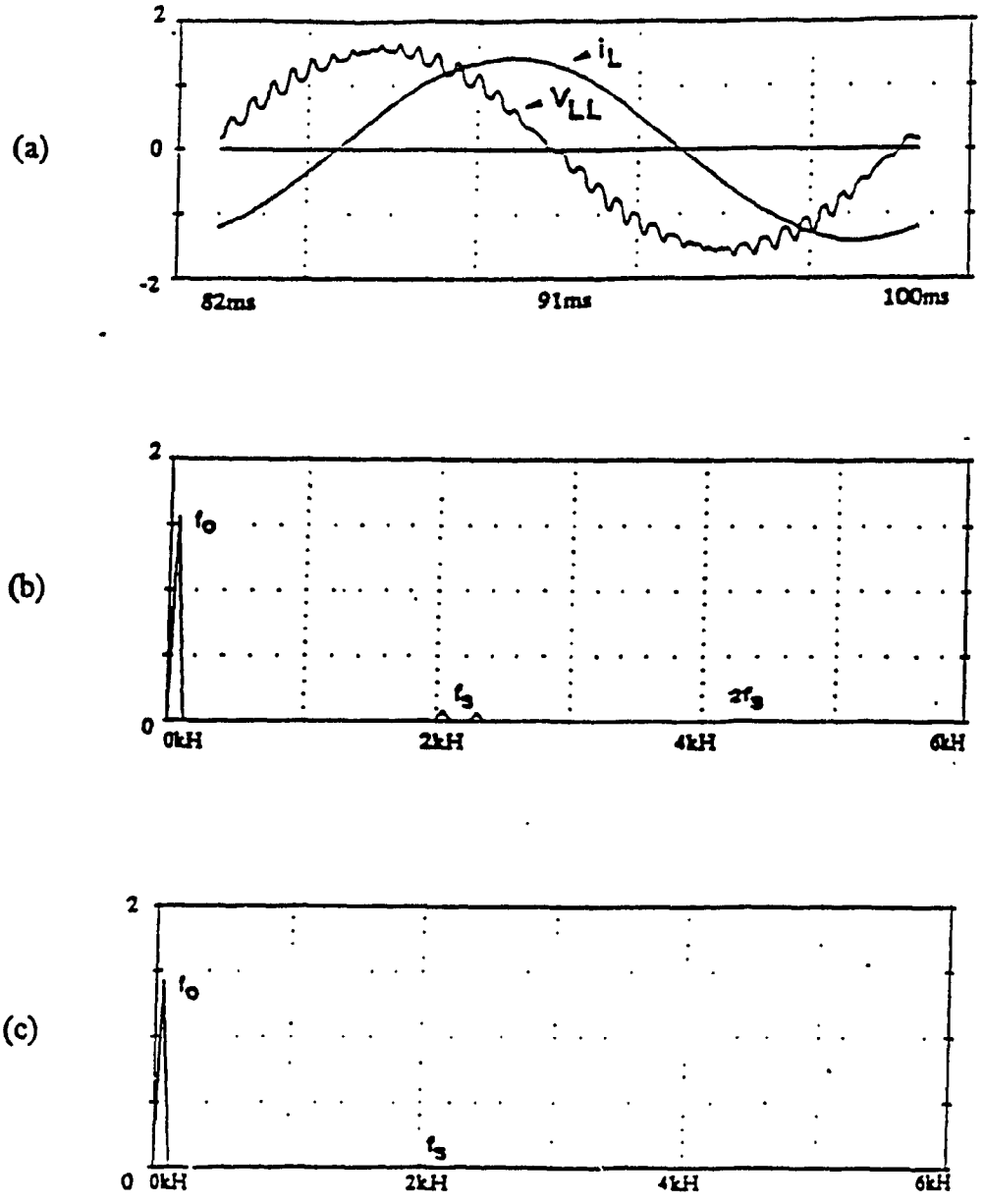


Fig. 3.3 Load voltage and current (simulation results, full load, load power factor = 0.8).

(a) Load voltage (line to line) and current (pu).

(b) Frequency spectrum of load voltage (pu).

(c) Frequency spectrum of load current (pu).

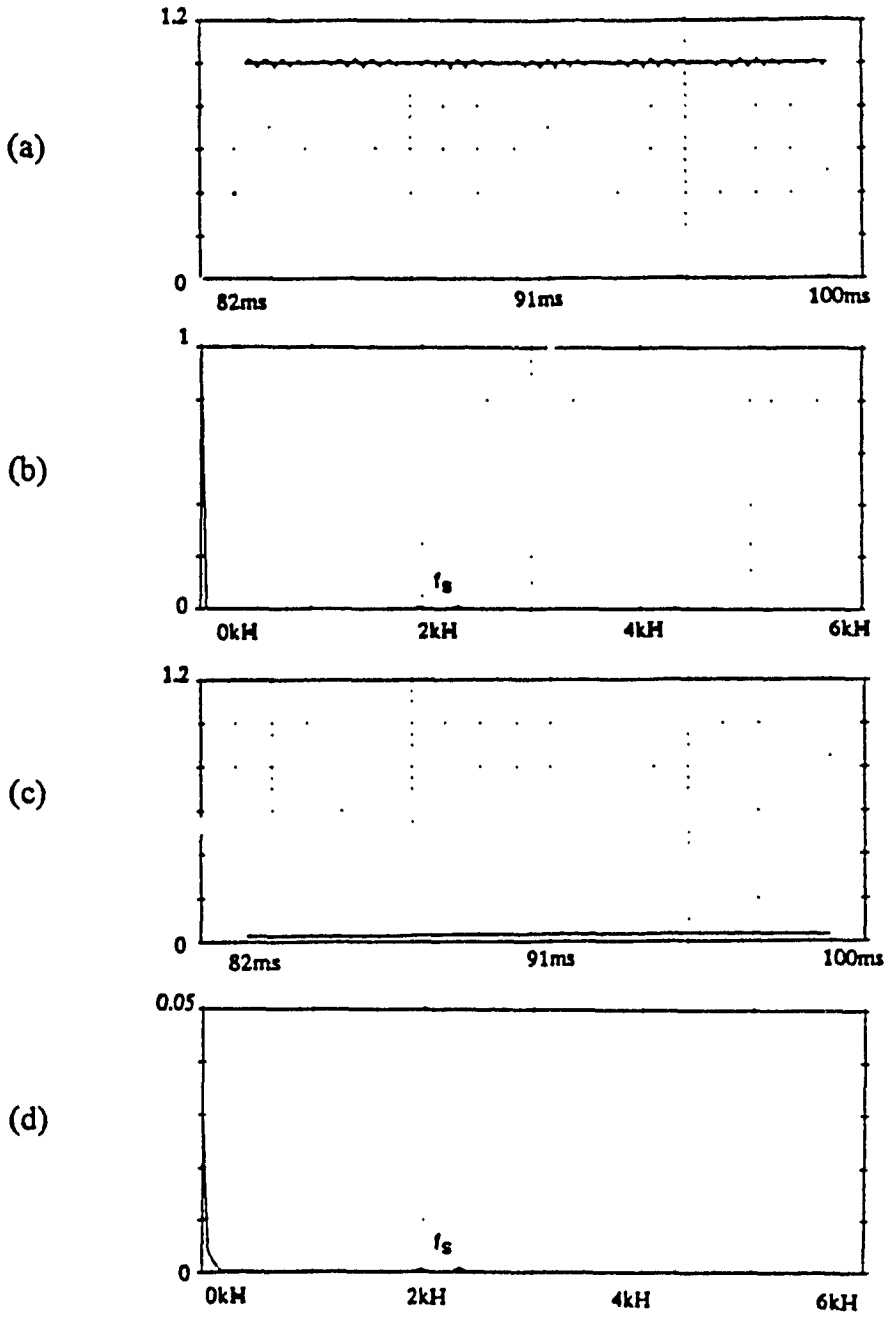


Fig. 3.4 DC bus voltage and battery current (simulation results).

(a) DC bus voltage (pu).

(b) Frequency spectrum of DC bus voltage (pu).

(c) Battery current (pu).

(d) Frequency spectrum of battery current (pu).

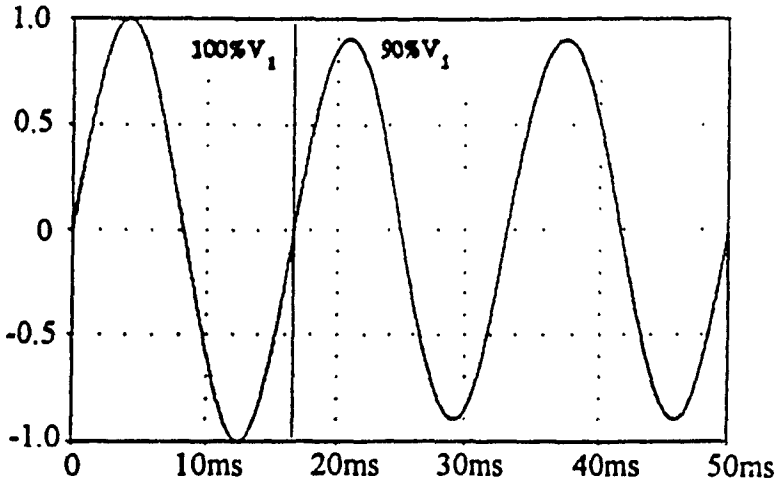
3.3 Fluctuations in the ac mains voltage

The ability of load voltage regulation of the system is verified by simulation with step changes of the ac mains voltage from 100% rated voltage to 90% rated voltage, and from 100% rated voltage to 110% rated voltage, respectively. The simulation results verify the generalized phasor diagram (Fig. 2.3), that is :

-- The inverter provides more reactive power to regulate the load voltage when the ac mains voltage is lower than the rated value, Fig. 3.5.

-- The inverter supplies less reactive power to regulate the load voltage when the ac mains voltage is higher than the rated value, Fig. 3.6.

(a)



(b)

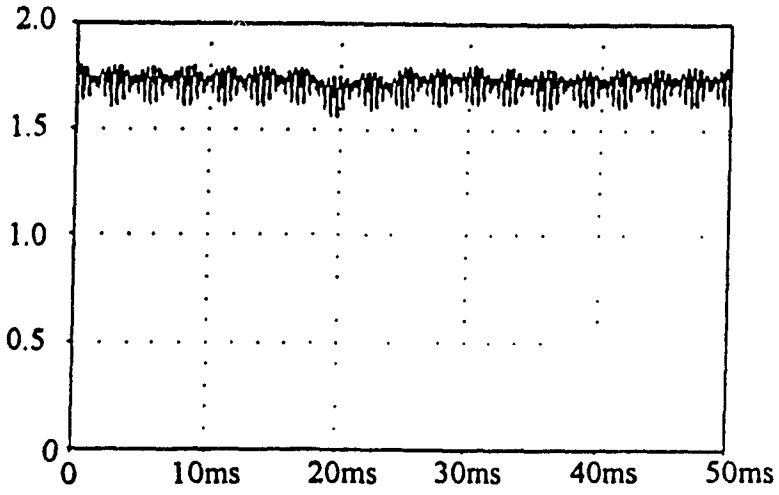
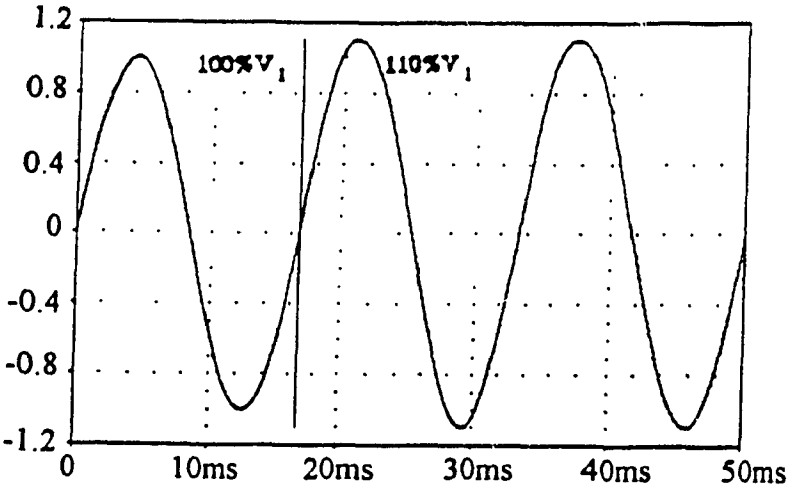


Fig. 3.5 Simulation results of the load voltage response to a step change in the ac mains voltage (from 100% rated voltage to 90% rated voltage at 16.67 ms)

(a) AC mains voltage (pu).

(b) Amplitude of the load voltage (line to line, pu).

(a)



(b)

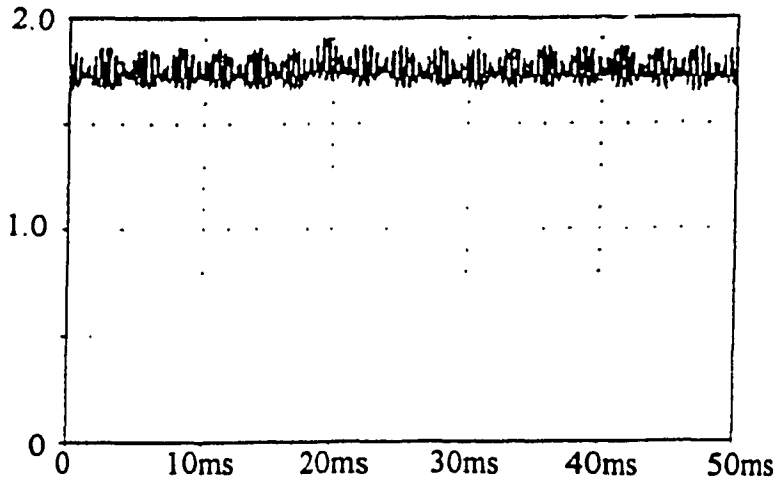


Fig 3 6 Simulation results of the load voltage response to a step change in the ac mains voltage (from 100% rated voltage to 110% rated voltage at 16.67 ms).

(a) AC mains voltage (pu).

(b) Amplitude of the load voltage (line to line, pu).

3.4 Nonlinear load or nonlinear ac mains

Simulations are carried out to confirm the harmonic absorption ability of the inverter. The simulation results validate the equivalent circuits for the load harmonic components (Fig. 2.6) and for the inverter harmonic components (Fig 2 9), specifically,

-- A nonlinear load, represented by a diode rectifier, does not result in low order harmonic distortion on the ac mains, Fig 3 7.

-- The harmonic component of the polluted ac mains (containing a fifth order harmonic with 1 pu amplitude) does not appear in the load current, Fig 3 8

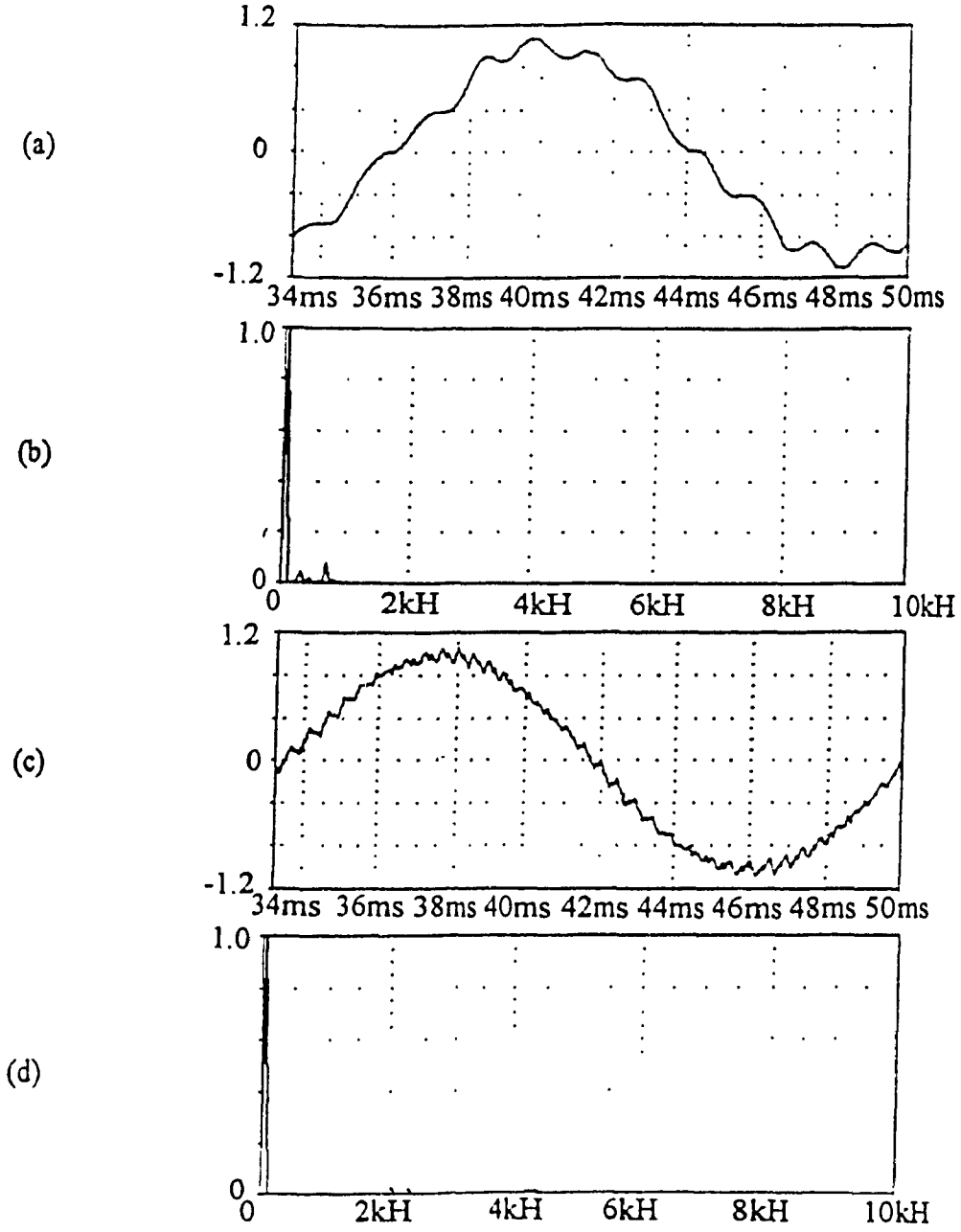


Fig. 3.7 Simulation results of the system under the conditions of a nonlinear load.

(a) Load current (pu).

(b) Frequency spectrum of the load current (pu).

(c) AC mains line current (pu).

(d) Frequency spectrum of the ac mains line current (pu).

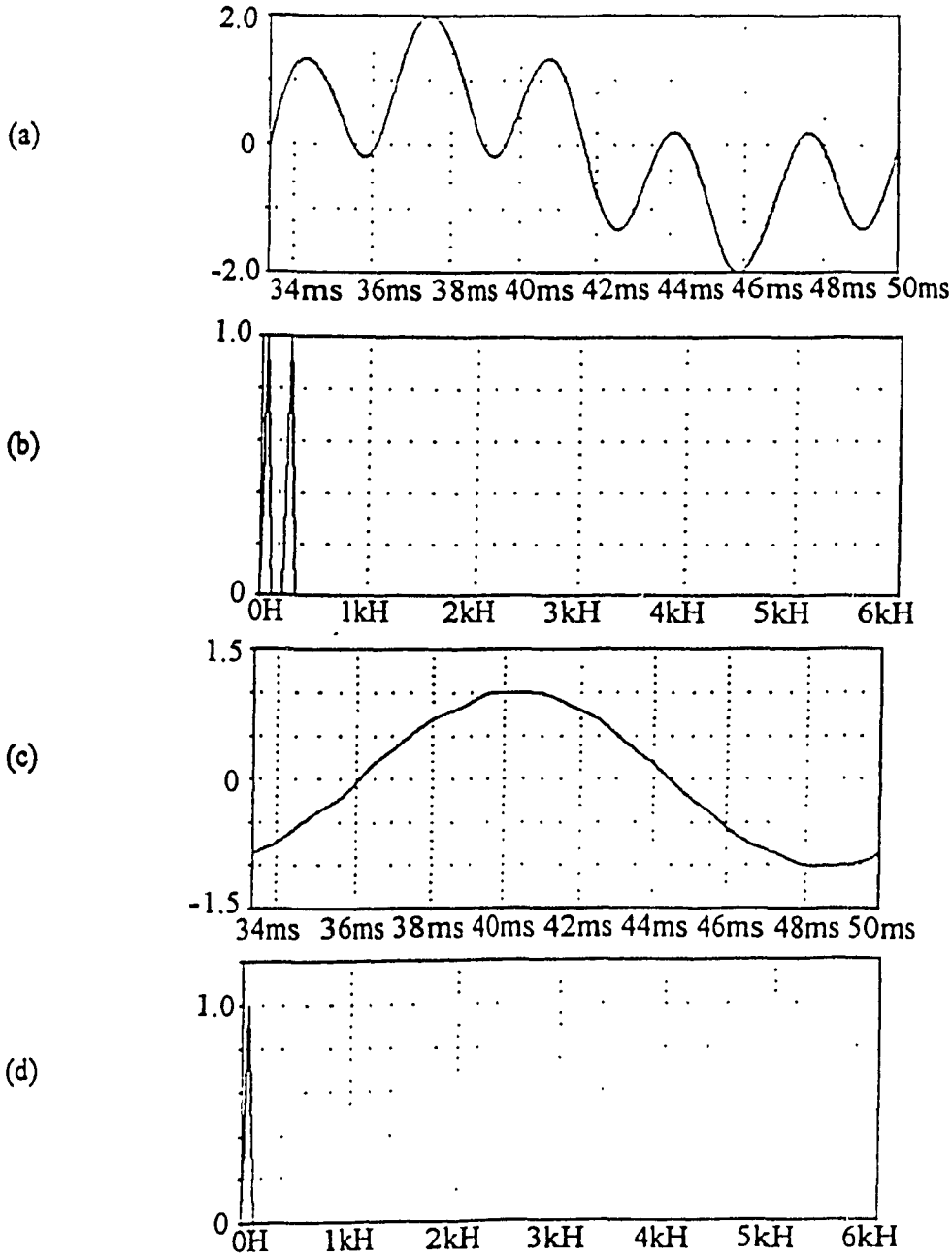


Fig. 3.8 Simulation results of the system under the conditions of a nonlinear ac mains

(a) AC mains line to neutral voltage (pu).

(b) Frequency spectrum of the ac mains voltage (line to neutral, pu)

(c) Load current (pu).

(d) Frequency spectrum of the load current (pu).

3.5 *Unbalanced load or unbalanced ac mains*

In order to observe the unbalance compensation ability of the inverter, two simulations are carried out respectively under the following conditions :

1) One phase (phase A) of the three phase load is opened (from practical point of view, one phase fault often happens in three phase systems), Fig. 3.9; and
2) One phase (phase A) of the ac mains voltage is opened, Fig. 3.10.

The results validate the equivalent circuit for the negative sequence components (Fig. 2.7), specifically,

-- A negative sequence current from an unbalanced load, does not appear on the ac mains, Fig. 3.9.

-- A negative sequence current on the ac mains does not flow through a balanced three phase load, Fig. 3.10.

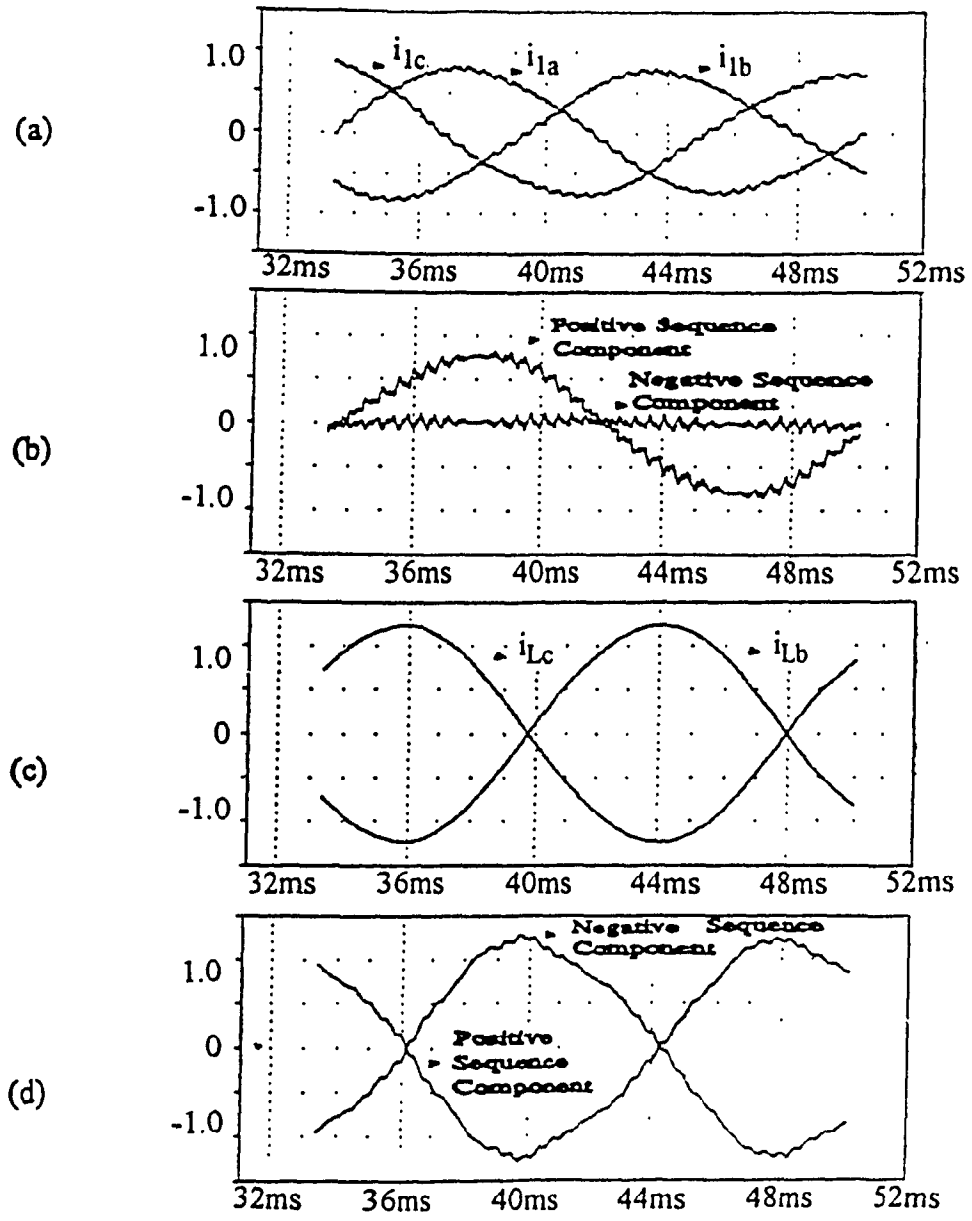


Fig. 3.9 Simulation results of the system under the conditions of an unbalanced load.

(a) AC mains line current (pu).

(b) Positive and negative components of the ac mains line current (pu)

(c) Load current (pu, phase A is opened).

(d) Positive and negative components of the load current (pu).

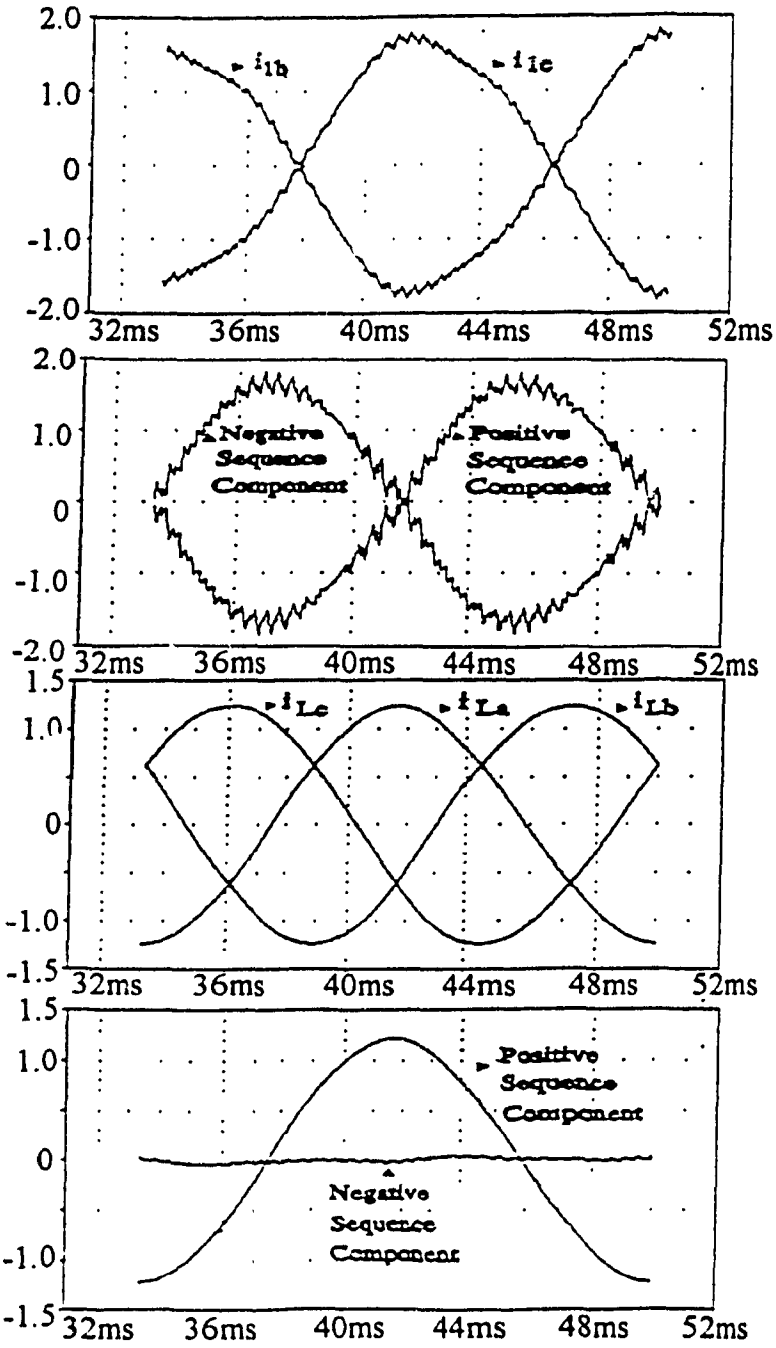


Fig. 3.10 Simulation results of the system under the conditions of an unbalanced ac mains.

(a) AC mains line current (pu, phase A is opened).

(b) Positive and negative components of the ac mains line current (pu).

(c) Load current (pu).

(d) Positive and negative components of the load current (pu).

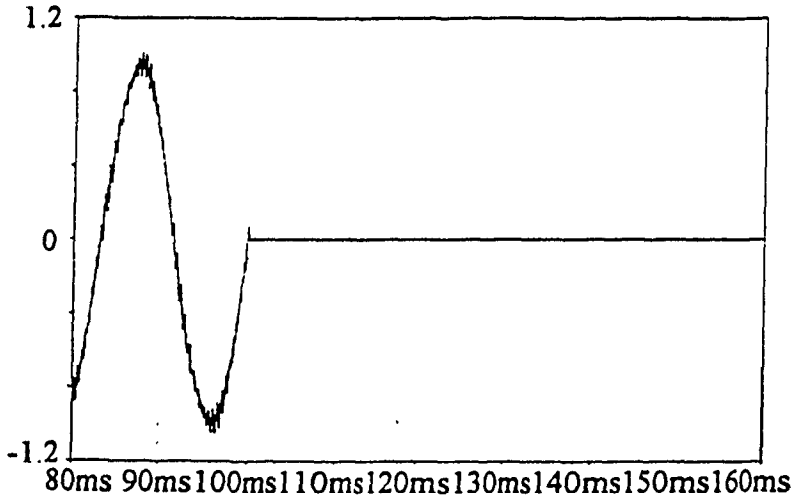
3.6 Sudden AC mains failure

The simulation results of the performance of the proposed system, when the ac mains fails suddenly, is shown in Fig. 3.11. Conclusions can be derived from Fig. 3.11 as followings :

(1) The transfer of the power supply from the ac mains to the inverter is automatic and with zero time delay.

(2) The variation of the load voltage is very small during the transient period.

(a)



(b)

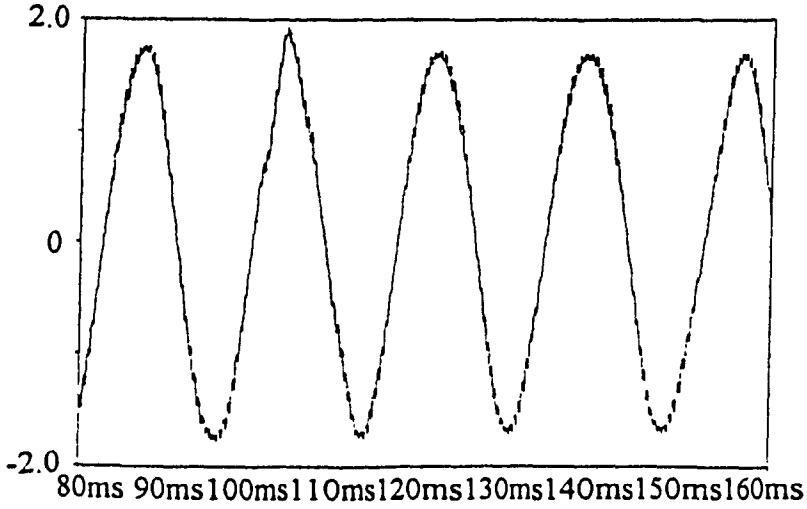


Fig. 3.11 Simulation results of the system under the conditions of a sudden block out (at 100 ms) of the ac mains.

(a) AC mains line current (pu).

(b) Load voltage (line to line, pu).

3.7 Experimental results

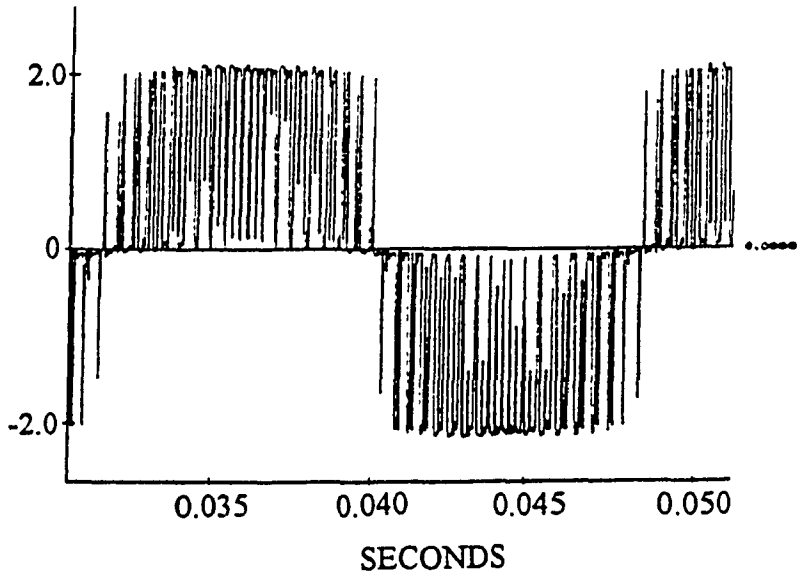
A 5kVA, 208V three phase UPS system using the per unit specifications designed in Chapter 2 was set up in the laboratory.

The system data are listed as following :

ac mains line to line voltage	: V_1 = 208 V
ac mains line current	: I_1 = 14 A
line reactance	: L_1 = 7 mH
Load filter	: L_2 = 2 mH
	C_2 = 30 uF
Inverter Capacity	: P_{VSI} = 5000 VA
Switching Frequency	: f_s = 2160 Hz
Battery Filter	: C_{dc} = 200 uF
	L_{dc} = 5 mH
Battery Voltage	: V_{dc} = 384 V

The experimental results under the normal operating conditions are shown in Figs. 3.12 to 3.15. They coincide with the simulation results, Figs. 3.1 to 3.4.

(a)



(b)

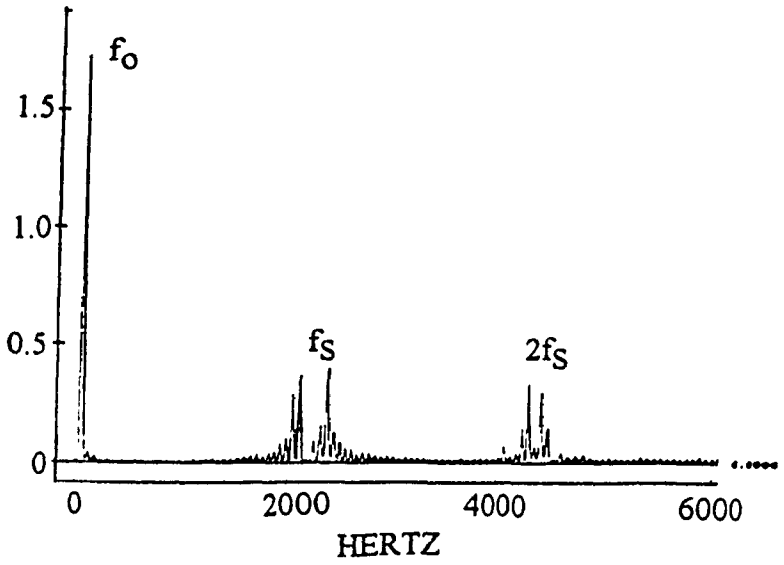
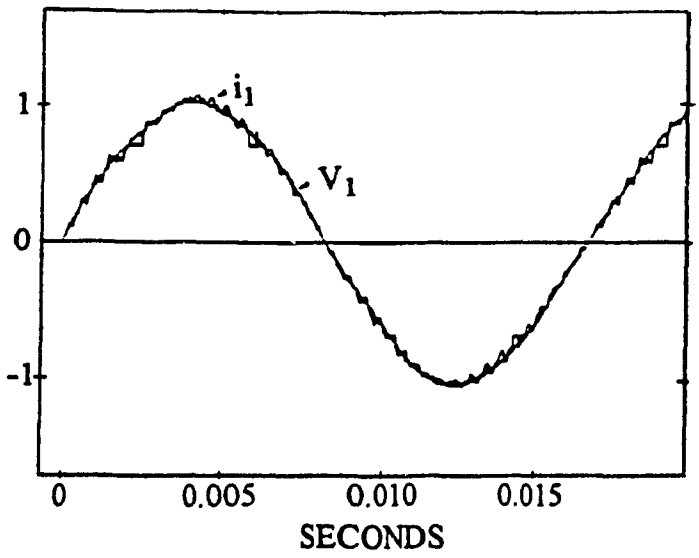


Fig. 3.12 Inverter output line to line voltage (experimental results).

(a) Inverter output line to line voltage (pu).

(b) Frequency spectrum of the inverter output voltage (pu).

(a)



(b)

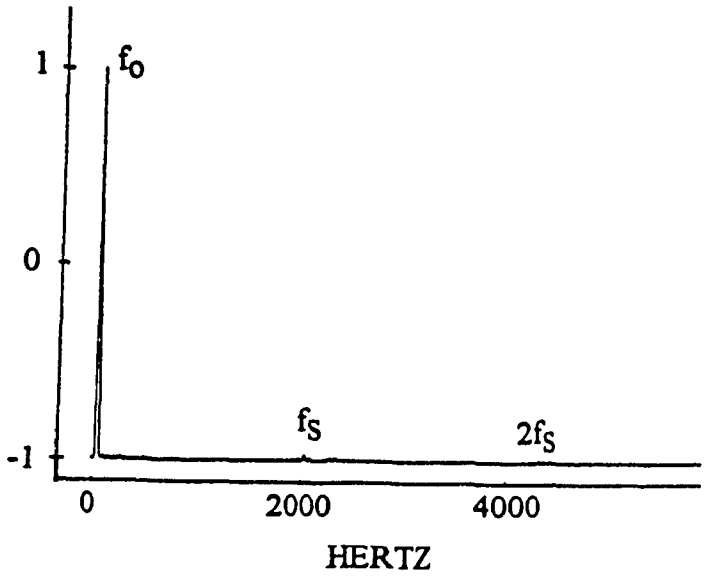


Fig. 3.13 AC mains line to neutral voltage and line current (experimental results, full load, load power factor = 0.8).

(a) AC mains line to neutral voltage and line current (pu).

(b) Frequency spectrum of ac mains line current (pu).

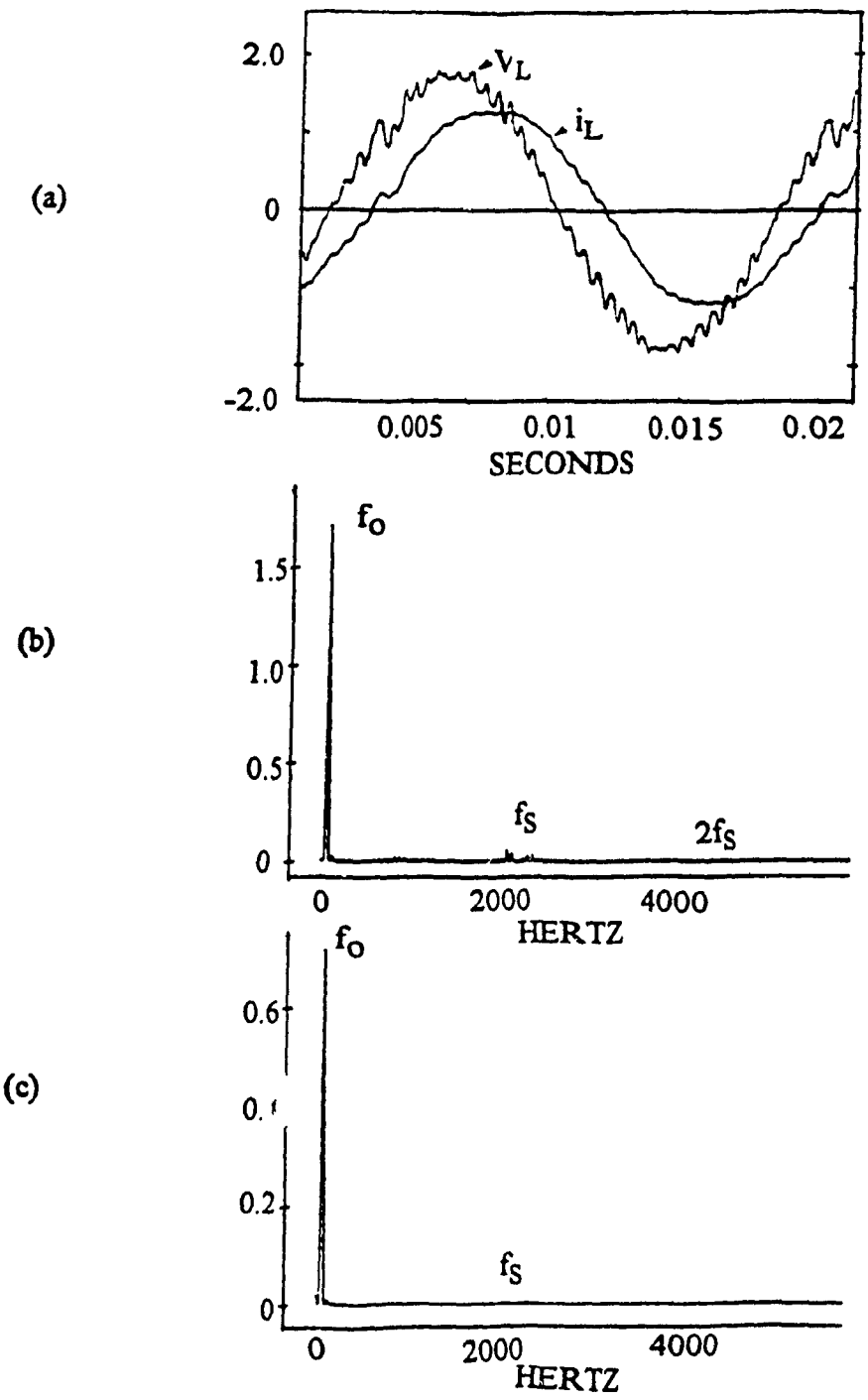


Fig. 3.14 Load voltage and current (experimental results, full load, load power factor = 0.8).

(a) Load voltage (line to line) and current (pu).

(b) Frequency spectrum of load voltage (pu).

(c) Frequency spectrum of load current (pu).

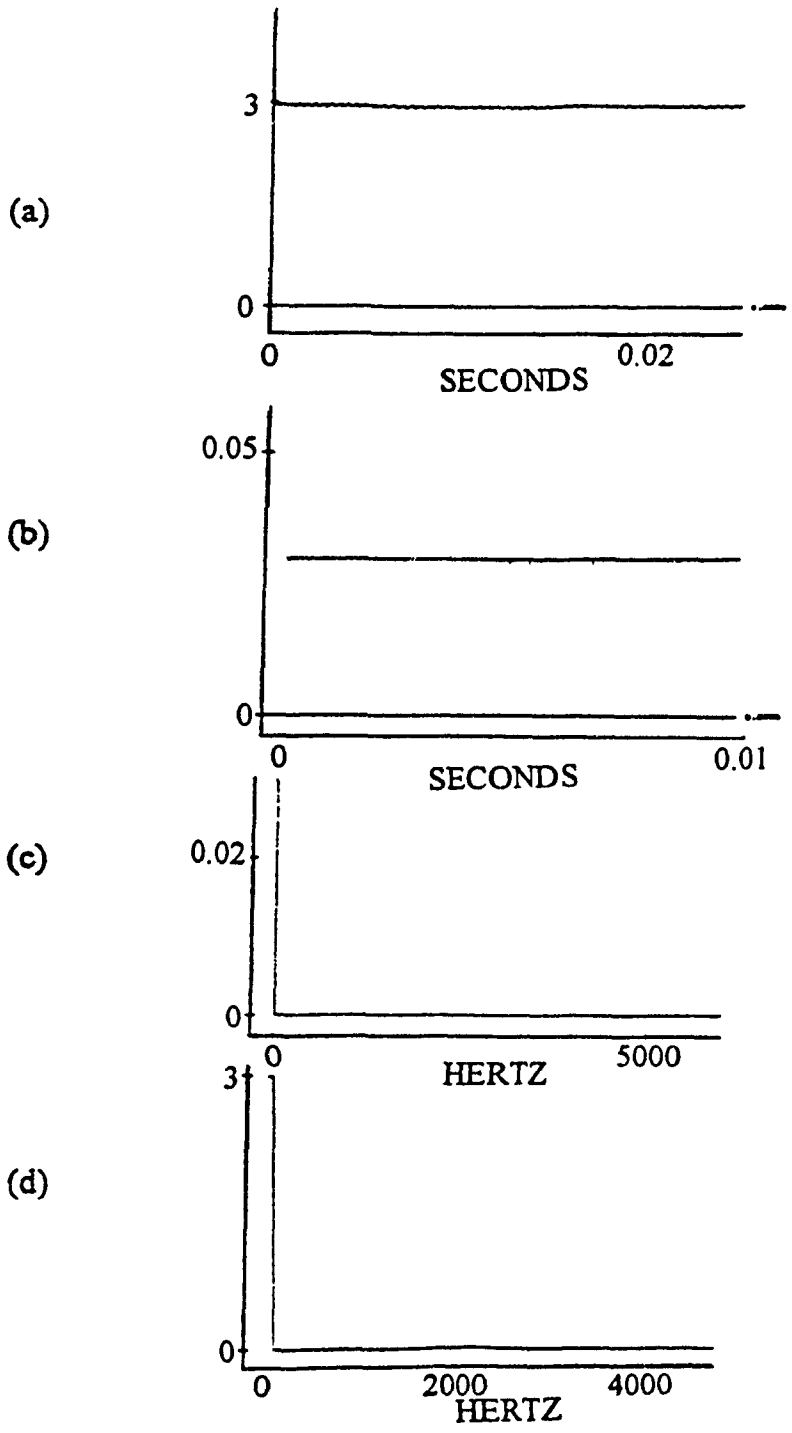


Fig. 3.15 DC bus voltage and battery current (experimental results).

(a) DC bus voltage (pu).

(b) Battery current (pu).

(c) Frequency spectrum of DC bus voltage (pu).

(d) Frequency spectrum of battery current (pu).

3.8 Conclusions

The simulation and the experimental results of the steady state operations of the proposed UPS system are provided to validate the power circuit design equations and the equivalent circuits. It can be concluded from the results that the proposed configuration provides:

-- Nearly unity power factor, Fig. 3.2(a).

-- Very low harmonic distortion in the ac mains current, Fig. 3.2(b).

-- Very low harmonic distortion in the load voltage and load current, Fig. 3.3.

-- High operating efficiency, Fig. 3.4(c).

-- Load voltage regulation, Figs. 3.5 and 3.6.

-- Automatic absorption of the load or line harmonic current, Figs. 3.7 and 3.8.

-- Automatic compensation for load or line unbalance, Figs. 3.9 and 3.10.

-- Continuous power supply, Fig. 3.11.

CHAPTER 4

CONTROL SYSTEM DESIGN

4.1 Introduction

The control loops of a UPS play a crucial role in the dynamic performance of the system. Many control principles have been practiced for different configurations [27] [28]. The two control loops employed in the proposed UPS system exploit fully the advantages of the proposed UPS system, Fig. 4.1. A slower loop (δ loop), acting on the angle between the ac mains voltage and the inverter voltage fundamental component, limits the battery charging current and regulates the dc bus voltage, Fig 4.2(a); and a fast loop (M loop), acting on the modulation index M, regulates the load voltage, Fig 4.2(b); Advantages include simplicity and reliability in implementation.

The design of the control loops of the parallel processing inverter systems is more complicated than that of the standard UPS systems. In order to design the regulators of the control loops, dynamic models for transient analyses are built, which also allow the influence of the system parameter variations on the system dynamic response to be analyzed.

Based on the system performance requirements, a design example is demonstrated, using the power circuit parameters designed in Chapter 2.

4.2 Requirements of the control loops

The voltage of the commercial power supply often fluctuates around its rated level The load supplied by the UPS system also changes with random characteristics These two external variations alter the amount of energy supplied to the battery and consequently

cause the fluctuations of the battery charging current. A control loop (δ loop) is therefore required to stabilize the dc bus voltage. This loop also ensures that under steady state conditions the inverter supplies no real power to the load. Moreover, this loop also has functions of (a) synchronizing the voltages between ac mains and the inverter, and (b) limiting the battery charging current.

The external variations also cause the fluctuations on the load voltage. In order to perform load voltage regulation, another loop (M loop) is required.

Under normal operating conditions, the regulation performed by the two control loops also guarantees nearly unity power factor, as illustrated in Fig. 2.3(a).

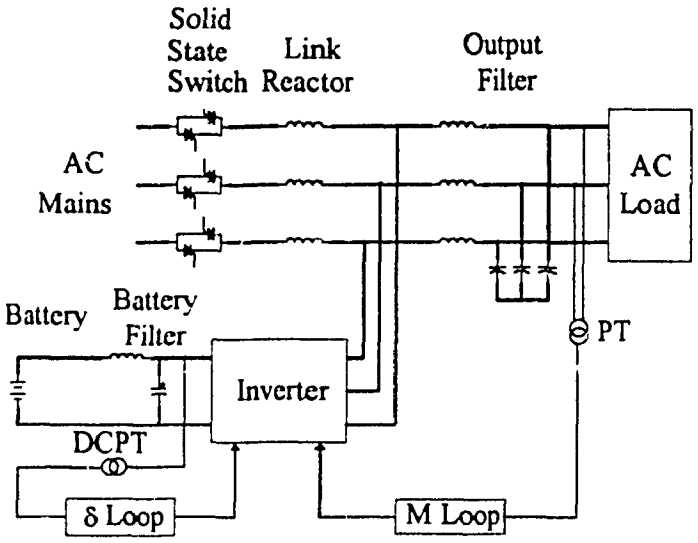
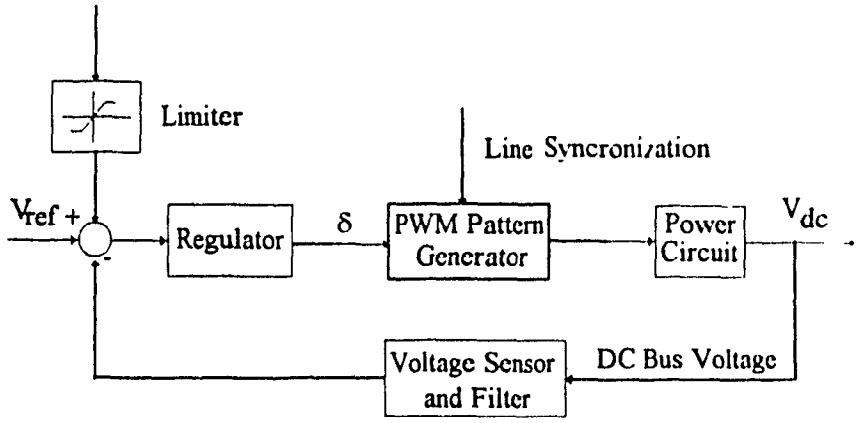


Fig 4.1 Control loops employed in the proposed UPS system.

(a)



(b)

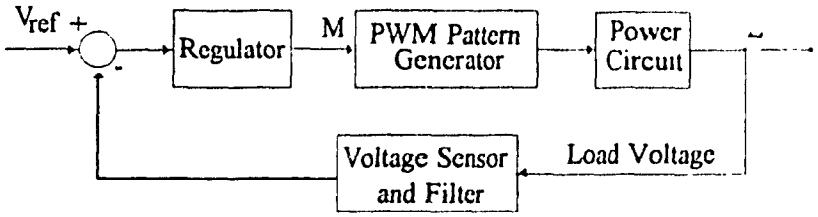


Fig. 4.2 Control loops of the proposed UPS system.

(a) DC bus voltage control loop (δ loop).

(b) Load voltage control loop (M loop)

4.3 Operating principles of the control loops

4.3.1 DC bus voltage regulation

In the normal operating conditions, the amount of real power delivered to the inverter alters the amount of energy stored in the battery, thus changing the battery charging current and varying the dc bus voltage. The real power, provided by the ac source, is proportional to the sine value of the angle δ between the ac mains voltage and the fundamental component of the inverter ac voltage. The angle δ is determined by the way the PWM pattern is generated. Since a standard sine PWM technique is applied in this thesis, the angle δ can be varied by phase shifting the sine modulation waveform [25]. Therefore, through a δ control loop, Fig. 4.2(a), the dc bus power is regulated, resulting in battery charging current limiting and dc bus voltage regulating. For a precise current limiting, an interventionist current loop or a cascaded inner current loop should be added.

4.3.2 Load voltage regulation

The amplitude of the fundamental component of the inverter ac voltage, V_1, is determined by the battery voltage and the amplitude of the fundamental component of the PWM pattern. With the sine PWM pattern, V_1 is proportional to the amplitude of the sine modulation waveform that is defined by the modulation index M. Therefore, the load voltage can be modulated by the second loop, the M loop, Fig. 4.2(b). This loop is designed to be much faster than the δ loop in order that the two loops do not interfere. This is describable and realizable since (a) instantaneous load voltage regulation is the priority, (b) the transient response of the battery voltage and current is not critical, and (c) the dynamics associated with δ control are slower than those of the M control.

4.4 Modeling of control loops

The single phase equivalent circuit for transient analysis, Fig 4.3, is used to build the dynamic models for the control loops.

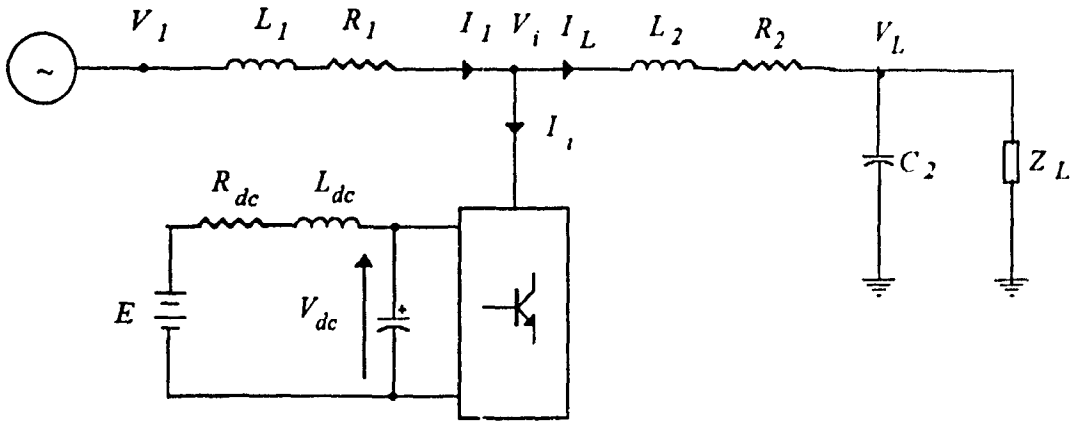


Fig. 4.3 Single phase equivalent circuit for modeling

The parameters and the variables shown in Fig. 4.3 are the same as Fig 2.1 Besides, R_1 represents the equivalent loss of the link reactor, R_2 is the equivalent resistance for the load filter, and R_{dc} for the sum of losses associated with the dc filter and the battery charging.

4.4.1 Modeling of the δ loop

The frequency response analysis of the δ loop is based on the dynamic model shown in Fig. 4.4. The dynamic model is obtained from a d-q transformation and is based on the following assumptions :

1) The three ac mains voltages are balanced and contain no harmonics

2) The dynamic model shown in Fig. 4 4 only takes into account the fundamental

components of currents and voltages. This is valid since the harmonic components do not affect the transient characteristics of the fundamental components because a) the amplitude of the harmonic currents are very small, and b) the frequency of the harmonic components are much higher than that of the fundamental components.

3) The system is linearized. This is valid since in practice, the variations of the phase shift angle δ are small [29].
4) The effect of the load current is neglected. This assumption is valid since the load current does not affect the dynamic characteristics of the system in the frequency range of interest (below 60 Hz) [22].

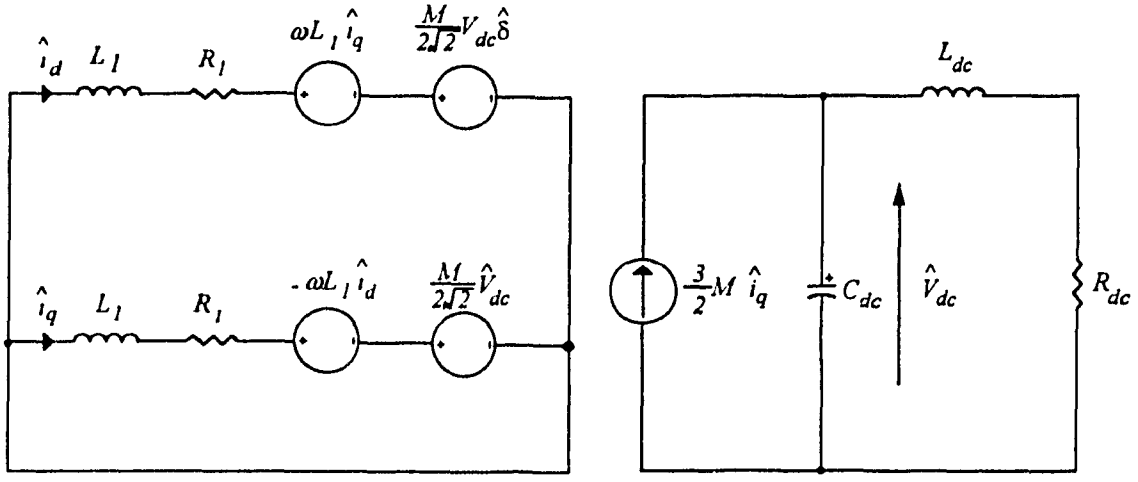


Fig. 4 4 Dynamic model for the transient analysis of the δ loop.

From Fig. 4.4, the derived transfer function of the open δ loop without compensation depends mainly on the values of the system damping, the link reactor L_1, and the dc bus filter,

$$\frac{\Delta V_{dc}}{\Delta \delta} = \frac{k_0(p_1 s + p_0)}{q_4 s^4 + q_3 s^3 + q_2 s^2 + q_1 s + q_0} \tag{4.1}$$

where

$$k_0 = \frac{3M^2}{4}\omega_0 L_1 V_{dc}$$

$$p_1 = L_{dc}$$

$$p_0 = R_{dc}$$

$$q_4 = L_{dc}C_{dc}L_1^2$$

$$q_3 = 2L_{dc}C_{dc}R_1L_1 + R_{dc}C_{dc}L_1^2$$

$$q_2 = L_{dc}C_{dc}\omega_0^2 L_1^2 + 2R_{dc}C_{dc}R_1L_1 + L_1^2 + \frac{3M^2}{4}L_{dc}L_1$$

$$q_1 = R_{dc}C_{dc}\omega_0^2 L_1^2 + 2R_1L_1 + \frac{3M^2}{4}(L_{dc}R_1 + R_{dc}L_1)$$

$$q_0 = \omega_0^2 L_1^2 + \frac{3M^2}{4}R_{dc}R_1$$

$\omega_0 = 2\pi \cdot$fundamental frequency

M = the modulation index of the sine PWM pattern.

The magnitude response of the open δ loop without compensation begins declining at ω_b with a speed of -60 db/dec.

A typical regulator is chosen comprising (a) a PI element to reduce the steady state error and improve transient response and tracking, and (b) a lag/lead network to adjust the transient response (phase/gain margin).

The transfer function of the PI element is equal to,

$$G_{PI}(s) = \frac{k_P s + k_I}{s}$$

$$= \frac{\frac{s}{\omega_{PI}} + 1}{\frac{s}{k_I}} \qquad (4.2)$$

with $\omega_{PI} = k_I/k_P$. For the sake of simplicity and straight perception, the break frequency of the PI element ω_{PI} is made equal to the open loop frequency ω_b, and the proportional factor k_P is chosen to satisfy the phase margin requirement.

The analog circuit of the PI element consists of an operational amplifier, two resistors R_1 and R_2, and a capacitor C, Fig. 4.5. The values of R_1, R_2 and C are chosen to meet Eq. (4.2),

$$k_P = \frac{R_2}{R_1}$$

$$k_I = \frac{1}{CR_1} \qquad (4.3)$$

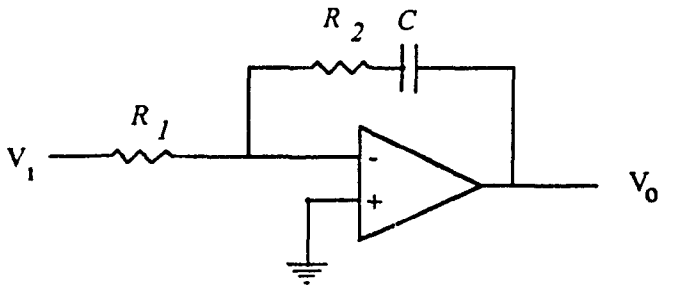


Fig. 4 5 Analog circuit of PI element.

The frequency response of the PI element is shown in Fig. 4.6. The magnitude response has an initial slope of -20 db/dec and an eventual value of $20 \cdot \log k_P$, Fig. 4.6(a). The phase response rises from -90° (phase lag) to 0°, Fig. 4.6(b).

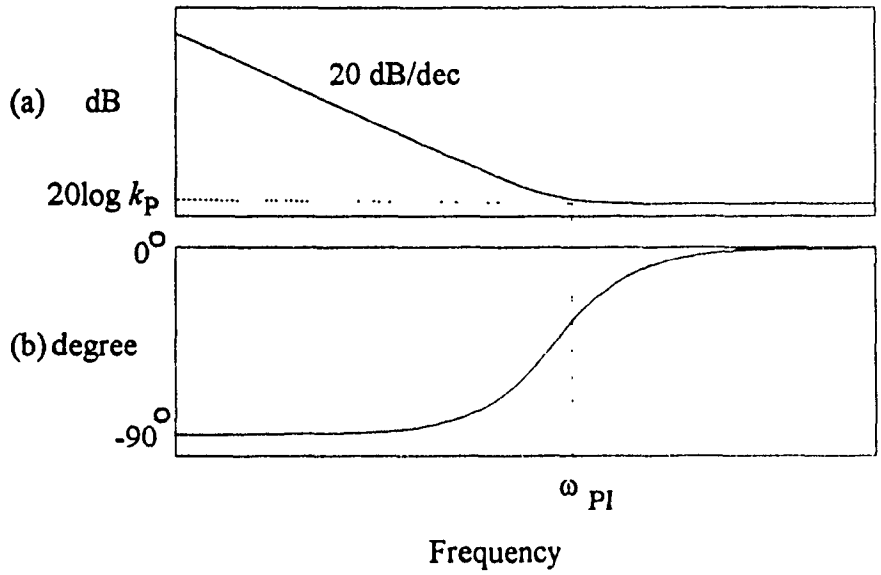


Fig. 4.6 Frequency response of the PI element.

(a) Magnitude response.

(b) Phase response.

The transfer function of the lag/lead network is,

$$G_C(s) = \frac{1 + \tau s}{1 + \alpha \tau s} \qquad (4\ 4)$$

The network contributes an additional gain to increase the response speed of the loop. The characteristics of the frequency response of the lag/lead network depends on the parameters α and τ, Fig. 4.7

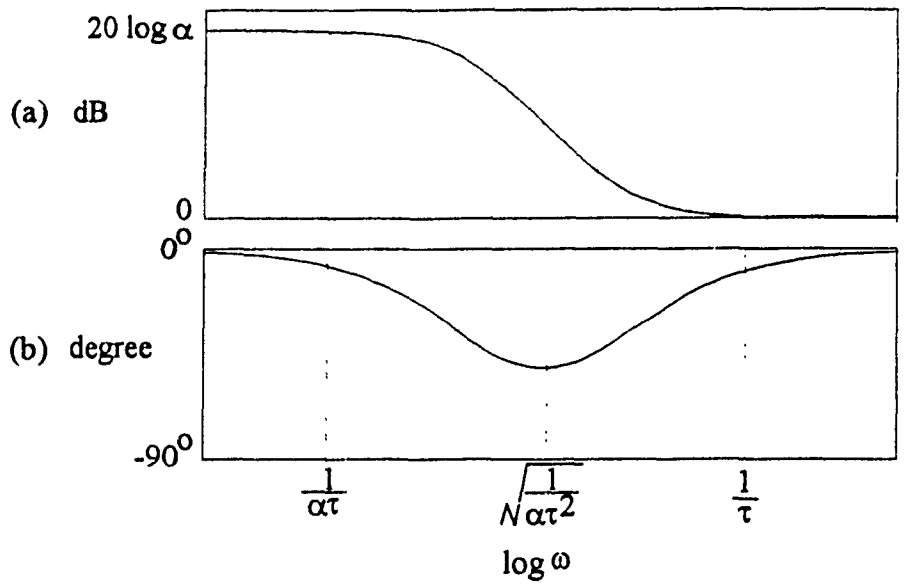


Fig. 4.7 Frequency response of the lag/lead network.

(a) Magnitude response.

(b) Phase response.

4.4.2 Modeling of the M loop

The design principles of the δ control loop can also be applied to the M loop design. The dynamic model for the M loop analysis is given in Fig. 4.8, based on the following assumptions :

(1) The three ac mains voltages are balanced and harmonic free.

(2) The dynamic model shown in Fig. 4.8 only takes into account the fundamental components of currents and voltages.

(3) The system is linearized.

(4) The effect of the load current and the ac mains line current are neglected.

(5) The load angle δ is constant.

(6) The dc bus voltage is ripple free.

The assumptions are valid due to the same reasons explained for modeling δ loop (for assumptions (1), (2), (3) and (4)) and the fact that the M loop is much faster than the

δ loop (for assumptions (5) and (6)).

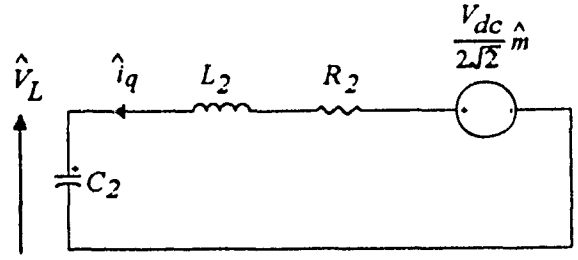


Fig. 4.8 Dynamic model for transient analysis of the M loop.

From Fig. 4.8, the derived transfer function of the open M loop without compensation depends mainly on the load filter values,

$$\frac{\Delta V_L}{\Delta m} = \frac{V_{dc}}{2\sqrt{2}} \frac{1}{L_2C_2s^2 + R_2C_2s + 1} \tag{4.5}$$

The same type of regulator is used and designed in the similar way as that for the δ loop.

4.5 Design example of control loops

The power circuit parameters of the proposed system are designed in Chapter 2 to satisfy the criteria pertaining to the load voltage ripple and the harmonic injection into the ac mains [20], specifically,

$L_1 = 0.3$ pu. $R_1 = 0.06$ pu.

$L_2 = 0.1$ pu. $R_2 = 0.02$ pu. $C_2 = 0.1$ pu

$L_{dc} = 0.25$ pu. $R_{dc} = 0.15$ pu. $C_{dc} = 0.65$ pu

and the per unit values are defined with respect to the following bases :

V_{base} = ac mains line to neutral voltage = 120 V

I_{base} = ac mains line current = 14 A

f_{base} = 60 Hz

4.5.1 Design example of δ loop

The predicted system frequency response of the open δ loop obtained from the transfer function given in Eq.(4.1) is plotted in Fig. 4.9.

The regulator is designed based on the following objectives [29] :

(1) The bandwidth of the closed δ loop is 10 Hz. This is based on the open loop characteristics (Fig. 4.9) and practical considerations, since he loop should be designed slower than the M loop.

(2) The percentage overshoot for an unit step reference is less than 5% (a standard specification [6]).

To satisfy the objectives, the regulator parameters are chosen from Eq.(4.2) and Eq.(4.4) as,

$$k_P = 0.111 \qquad k_I = 124 \qquad \tau = 0.0059 \qquad \alpha = 8.$$

The open loop frequency response of the δ control with compensation has 15 db gain margin and 45^{o} phase margin, Fig. 4.10. The corresponding closed loop frequency response has a bandwidth of 10 Hz, Fig. 4.11. Correspondingly, the predicted settling time is 100 ms, and the percentage overshoot 5% [30].

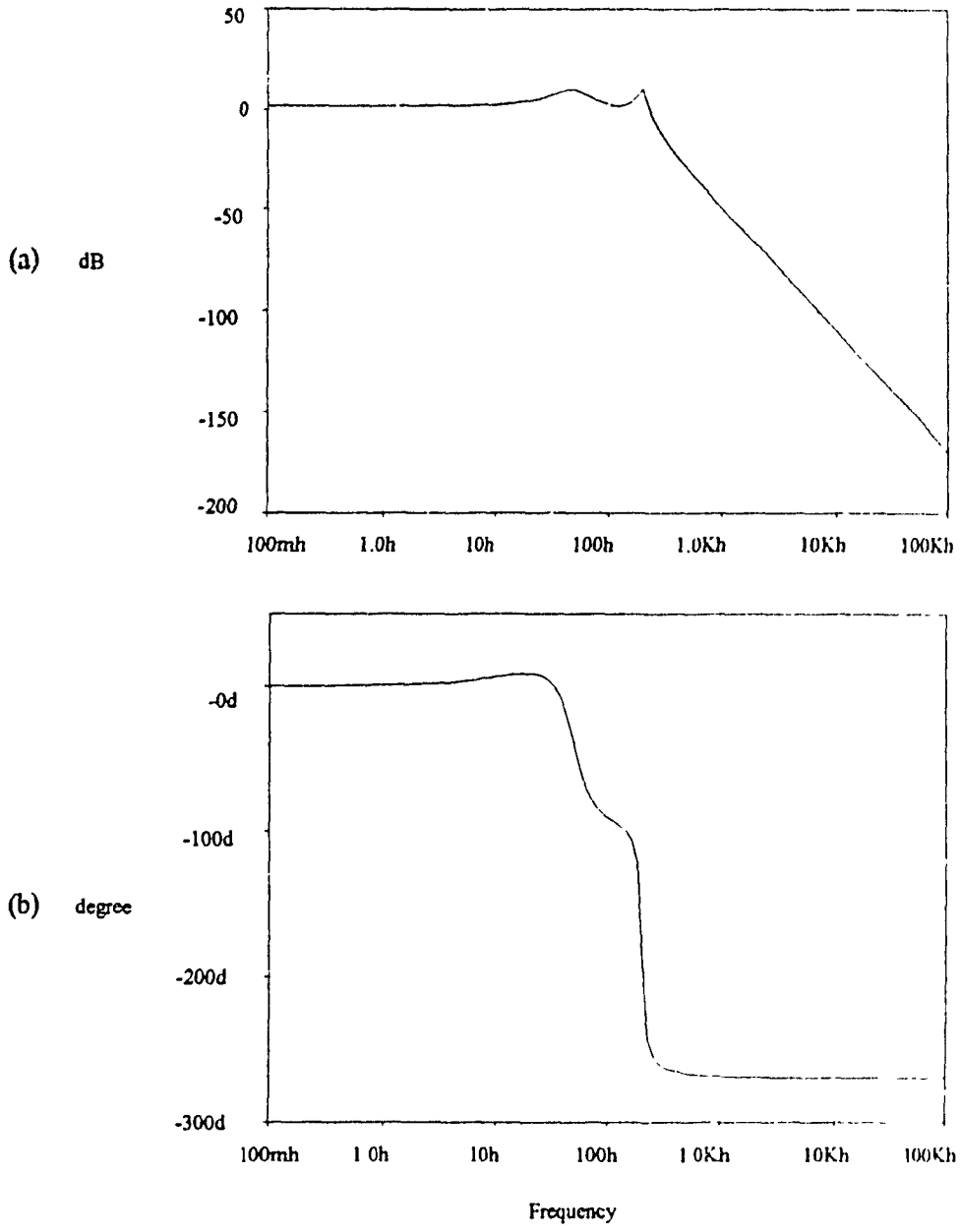


Fig. 4.9 Open loop frequency response of the uncompensated δ loop for no load operating conditions

(a) Magnitude response

(b) Phase response.

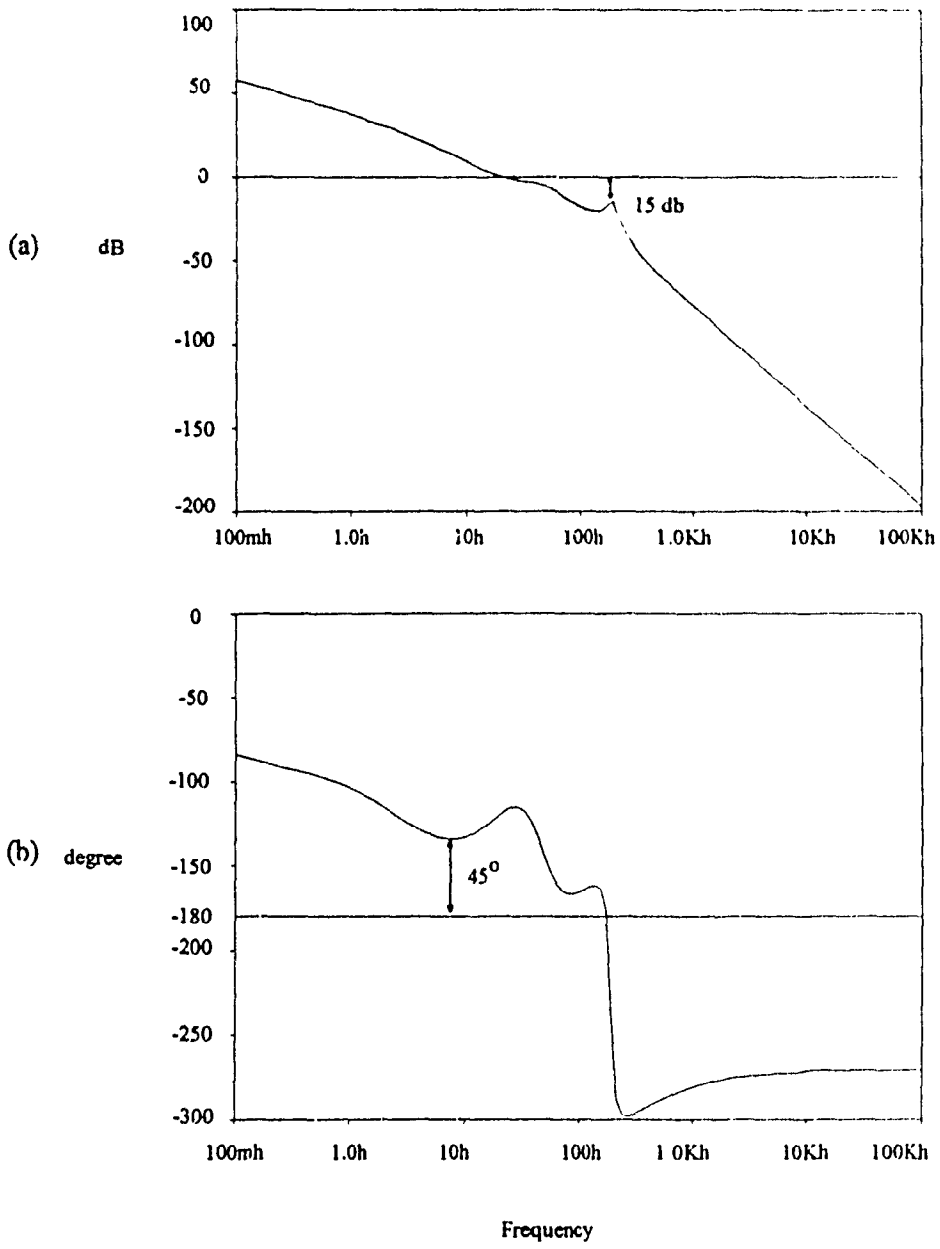


Fig. 4.10 Open loop frequency response of the compensated δ loop for no load operating conditions.

(a) Magnitude response.

(b) Phase response.

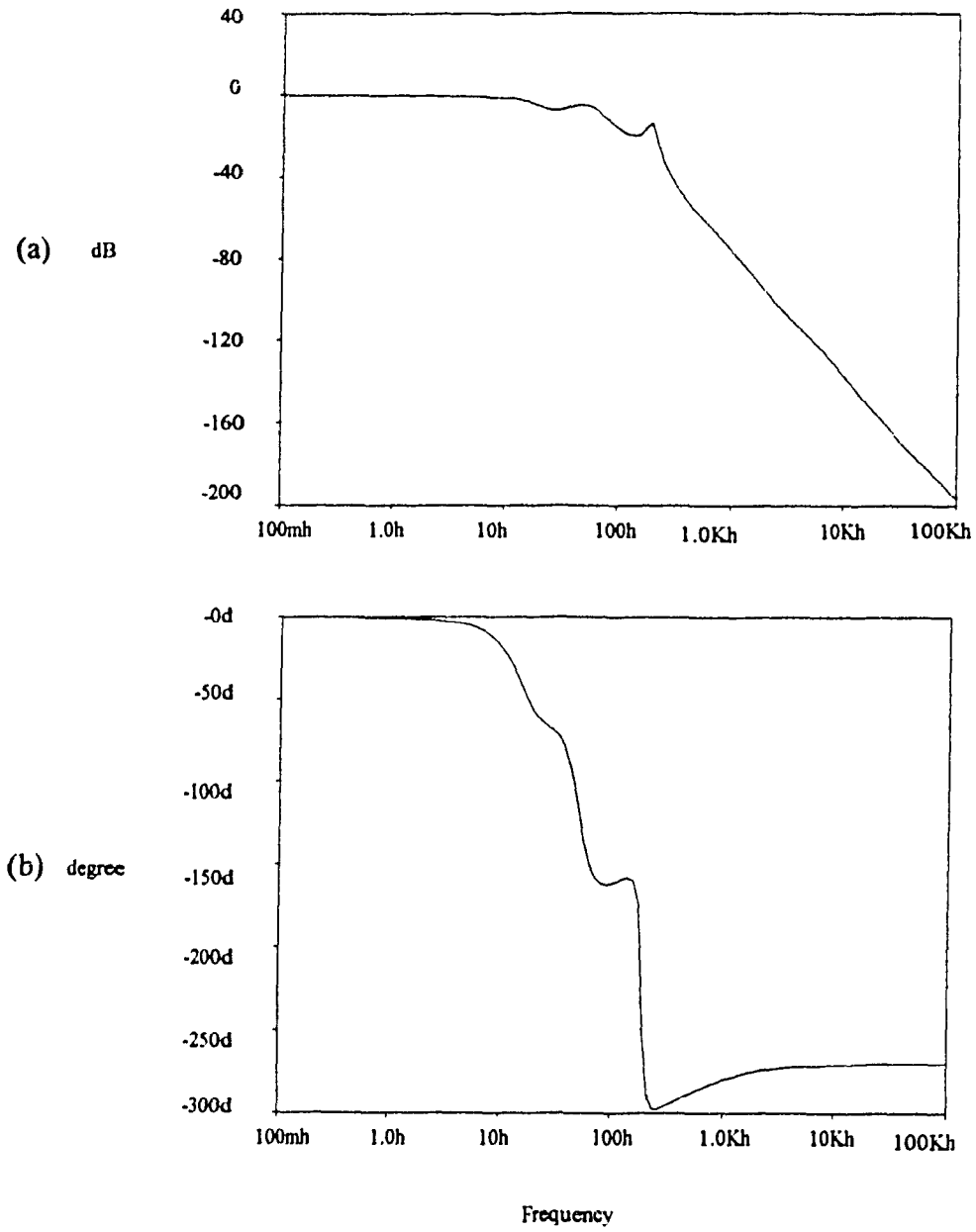


Fig. 4.11 Closed loop frequency response of the δ loop under no load operating conditions.

(a) Magnitude response.

(b) Phase response.

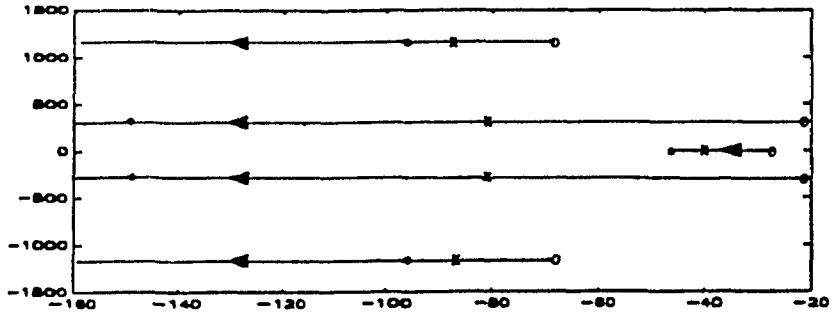
The influence of the important parameters on the system closed loop response is illustrated by means of the root loci, Fig. 4.12. Following conclusions can be drawn .

(1) The smaller the equivalent resistance for system losses, R_l, the slower the system responds, Fig. 4.12 (a).

(2) Decreasing the size of the line inductor, L_l, increases the speed of response, Fig. 4.12(b).

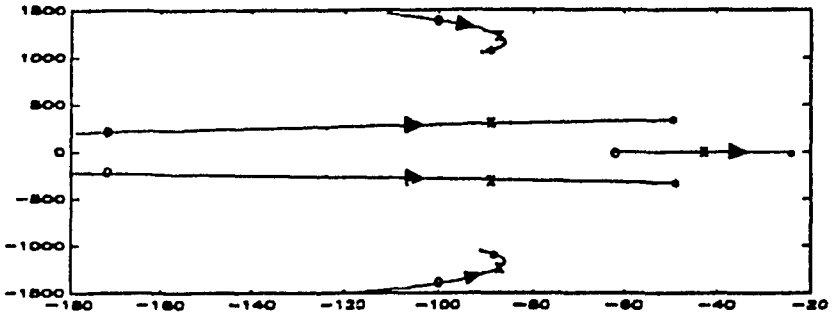
(3) A larger size of the dc bus capacitor, C_{dc}, causes a slower system response, Fig. 4.12(c).

(a)



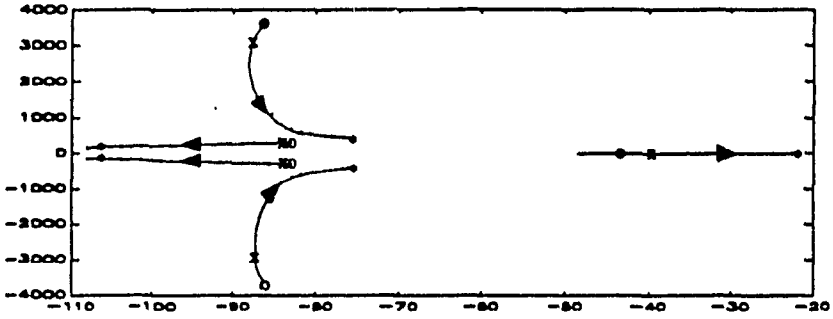
o : R_1 = 0.03 pu
x : R_1 = 0.06 pu (operating point)
* : R_1 = 0.12 pu

(b)



o : L_1 = 0.15 pu
x : L_1 = 0.3 pu (operating point)
* : L_1 = 0.6 pu

(c)



o : C_{dc} = 0.3 pu
x : C_{dc} = 0.65 pu (operating point)
* : C_{dc} = 1.3 pu

Fig. 4.12 Root loci of the closed δ loop for the variations of principal parameters.

(a) For increasing values of R_1.

(b) For increasing values of L_1.

(c) For increasing values of C_{dc}.

4.5.2 Design example of the M loop

The predicted open loop frequency response of the M control without compensation obtained from the transfer function given in Eq. (4 5) is plotted in Fig 4.13.

The design of the regulator is based on the following objectives [30] :

(1) The bandwidth of the closed loop is 100 Hz This is based on the open loop characteristics (Fig. 4.13) and practical considerations, since the M loop should be designed faster than the δ loop.

(2) The percentage overshoot for an unit step reference is less than 5% (a standard specification).

To satisfy the objectives, the regulator parameters are chosen from Eq.(4.2) and Eq.(4.4) as following :

$$k_P = 0.07 \qquad k_I = 457 \qquad \tau = 0.000258 \qquad \alpha = 12.$$

The open loop frequency response of the M control with regulator has 15 dB gain margin and 60^o phase margin, Fig. 4.14. The closed M loop frequency response has a much wider bandwidth (100 Hz) than that of the δ loop (10 Hz), Fig. 4.15. Correspondingly, the M loop is much faster than the δ loop. Moreover, from Fig 4.15, the predicted settling time is 10 ms, and percentage overshoot 5% [30].

The influence of the important parameters on the system closed loop response is illustrated in Fig. 4.16. Following conclusions can be drawn :

(1) Increasing the value of the equivalent resistance of the load filter, R_2, increases the system response, Fig. 4.16(a).

(2) Increasing the size of the inductor L_2, reduces the system response, Fig.4.16(b).

(3) Increasing the size of the capacitor C_2, reduces the system response, Fig.4.16(c).

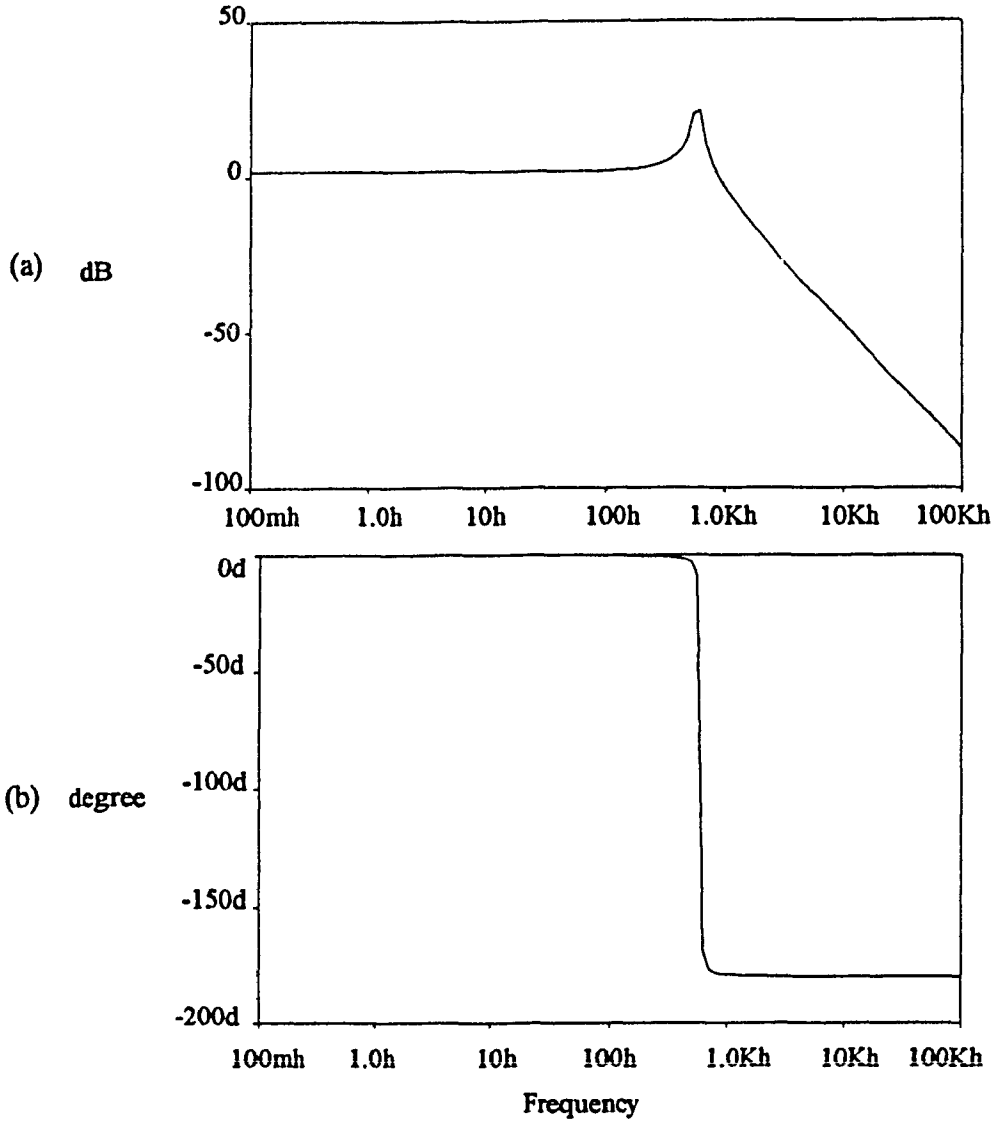


Fig. 4.13 Open loop frequency response of the uncompensated M loop under no load operating conditions.

(a) Magnitude response.

(b) Phase response.

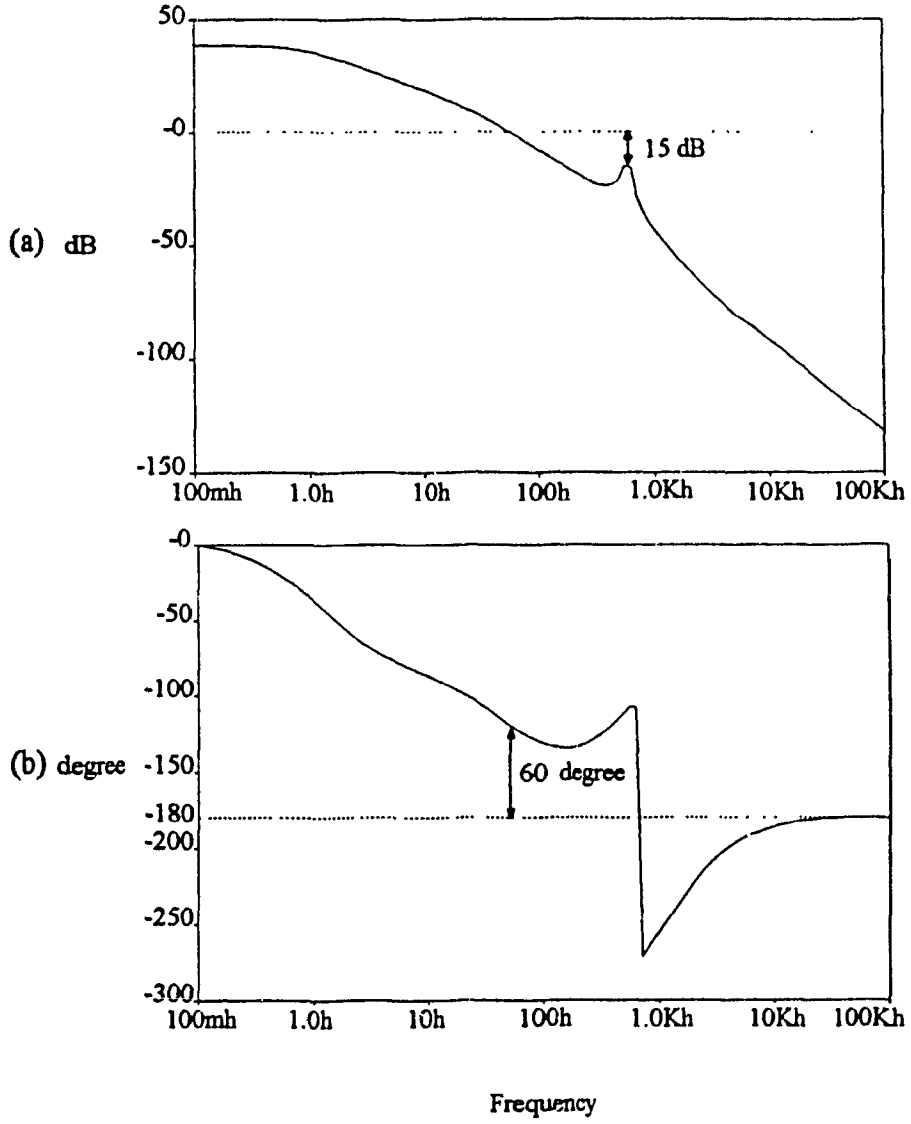


Fig. 4.14 Open loop frequency response of the compensated M loop under no load operating conditions.

(a) Magnitude response.

(b) Phase response.

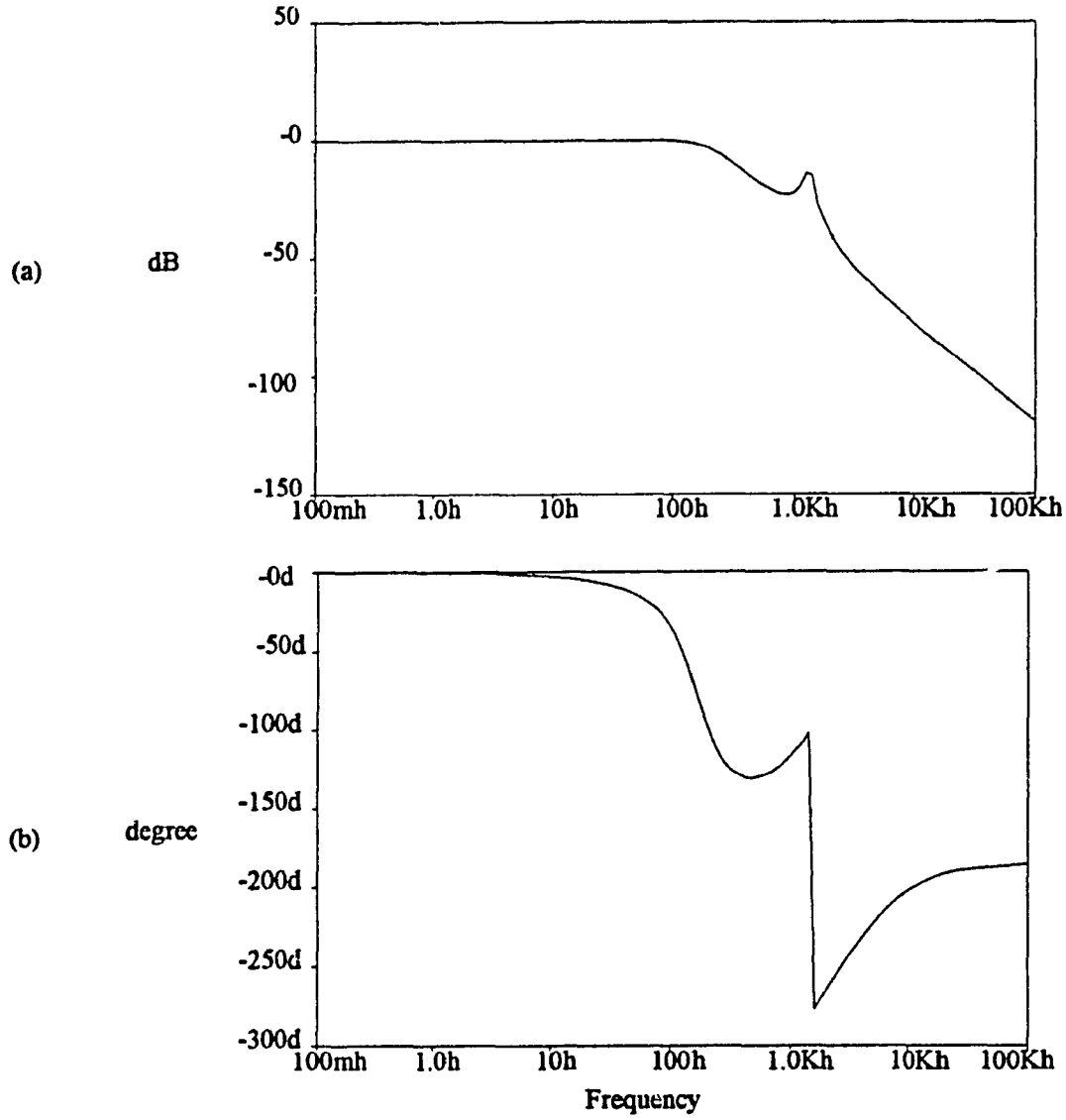
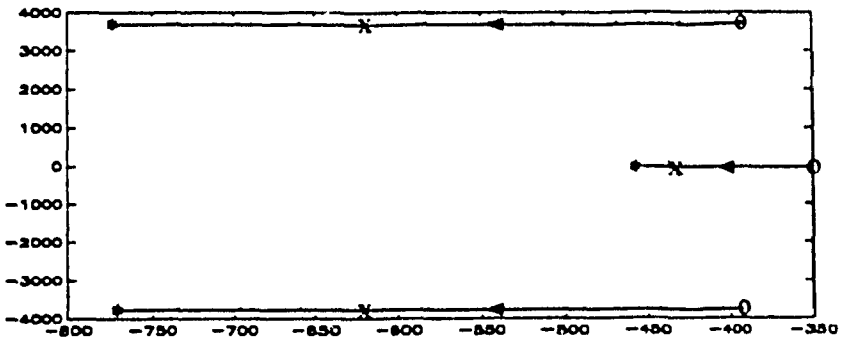


Fig. 4.15 Closed loop frequency response of the M loop under no load operating conditions.

(a) Magnitude response.

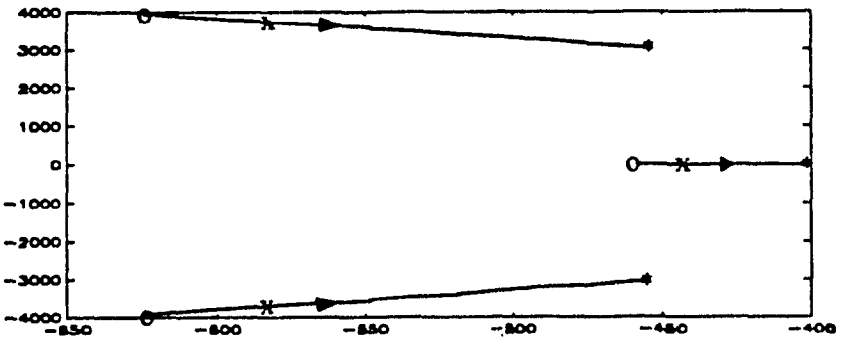
(b) Phase response.

(a)



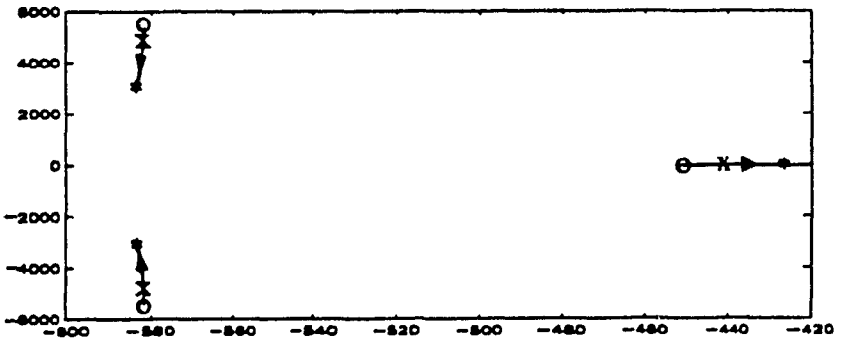
o : R_2 = 0.01 pu
* : R_2 = 0.03 pu
x : R_2 = 0.02 pu (operating point)

(b)



o : L_2 = 0.09 pu
* : L_2 = 0.15 pu
x : L_2 = 0.1 pu (operating point)

(c)



o : C_2 = 0.05 pu
* : C_2 = 0.15 pu
x : C_2 = 0.1 pu (operating point)

Fig. 4.16 Root loci of the closed M loop for the variations of principal parameters.

(a) For increasing values of R_2.

(b) For increasing values of L_2.

(c) For increasing values of C_{dc}.

4.6 Implementation of the control system

The block diagram of the control circuit is shown in Fig. 4.17.

A range of sine PWM patterns with a series of modulation index M is stored in an EPROM. The address of the EPROM consists of the most significant bits (MSBs) and the least significant bits (LSBs). The MSBs are used to select a pattern with a specific modulation index M, and the LSBs are used to address the waveform of the pattern.

A counter addresses the LSBs and a pattern is read at a fixed frequency that equals the ac supply frequency. A synchronization circuit resets the counter every cycle to synchronize the phase angle δ between the ac mains voltage and the inverter output voltage. The delay of the counter reset time determines the δ. Therefore, the implementation of the δ loop is acted on controlling the reset time of the counter.

An A/D converter converts the demanded modulation index M into a digital number which is used to address the MSBs of the EPROM. Hence, the M loop is realized by means of controlling the MSBs of the EPROM.

The design equations of the control loops are valid for Fig. 4.17 with the following assumptions :

a) The correction of the phase angle δ can only be carried out once the delay circuit resets the counter. The average time delay due to this fact is half cycle. However, this delay time is negligible compared to the system response (on average 6 cycles, [22]) and does not affect the validity of the design equations.

b) As long as the resolution of the modulation index of the patterns stored in the EPROM is high enough (12 patterns from M = 0.8 to 1.2 in the experimental set up), the effect of the quantization of the modulation index on the transient response of the system can also be neglected.

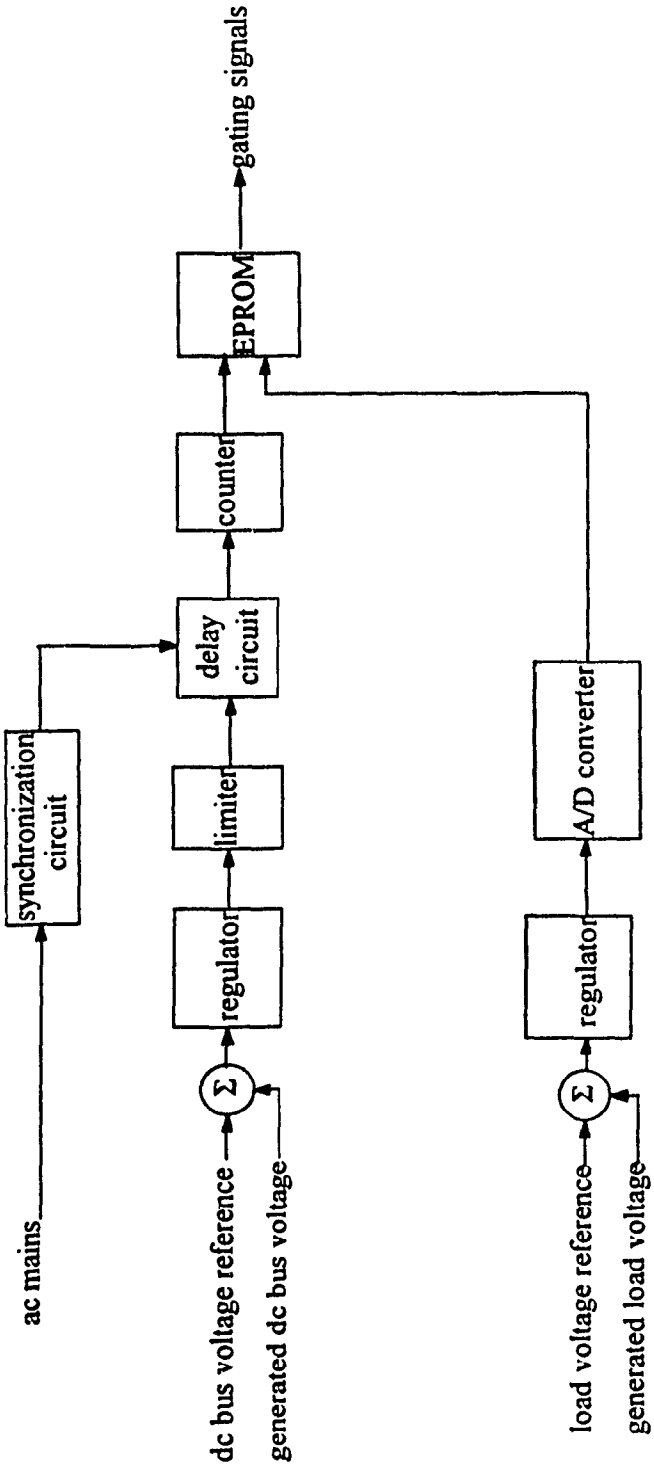


Fig. 4.17 Block diagram of the control circuit.

4.7 Conclusions

In this chapter, a dc bus voltage control loop (δ loop) and a load voltage control loop (M loop) are designed to fully exploit the advantages of the proposed UPS system. Dynamic models are derived. A design example is presented based on the power circuit parameters designed in Chapter 2. Conclusions can be made from the given example as following :

(1) The dynamic models can be used to design the regulators of the loops and to analyze the effect of the system transient response caused by the variations of the important system parameters.

(2) Through the δ loop control, the system transient response to a step change in the dc bus voltage reference is predicted to have a settling time less than 100 ms and an overshoot less than 5%.

(3) Through the M loop control, the system transient response to a step change in the load voltage reference is predicted to have a settling time less than 10 ms and an overshoot less than 5%.

Conclusions can also be made from the root loci (Fig. 4.12 and Fig. 4.16) of the closed control loops for the variations of the principal system parameters. Bigger values of R_1or R_2, or smaller values of L_1, L_2, or C_{dc}, increase the system transient response speed. Since a larger kVA of the UPS system results in the bigger values of R_1 and R_2, and a higher switching frequency results in the smaller L_1, L_2, and C_{dc}, in order to design a fast control system, a reasonable system damping ratio and a possible high switching frequency should be considered in designing the power circuit.

CHAPTER 5

DYNAMIC RESPONSES

5.1 Introduction

The simulation and the experiment are carried out to confirm the performance of the system predicted by the objectives of the control loops designed in chapter 4.

The dynamic responses of the system are obtained under the following conditions :

1) a step change in the dc bus voltage reference; and

2) a step change in the load voltage reference.

5.2 Response to a step change in the dc bus voltage reference

In order to verify the performance of the δ loop, a simulation is done with the system operating under the following conditions :

1) a step change in the dc bus voltage reference, and

2) a rated road.

The simulation results, as shown in Fig. 5.1, confirms the validity of the δ loop design based on the predicted closed loop response to a step change in the dc bus voltage reference, giving respectively,

-- a rise time that is 100 ms, and

-- a percentage overshoot that is less than 5%.

The simulation results are verified with the experimental prototype (introduced in Chapter 3) under the same conditions as that for the simulation. The experimental results, as shown in Fig. 5.2, coincide with the simulation results

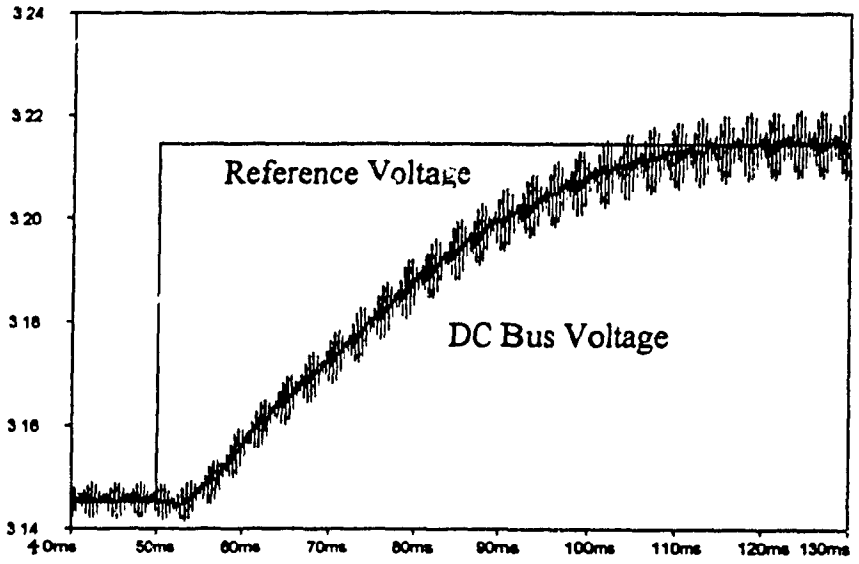


Fig. 5.1 Simulation results of the response of the dc bus voltage to a step change in the reference voltage (pu).

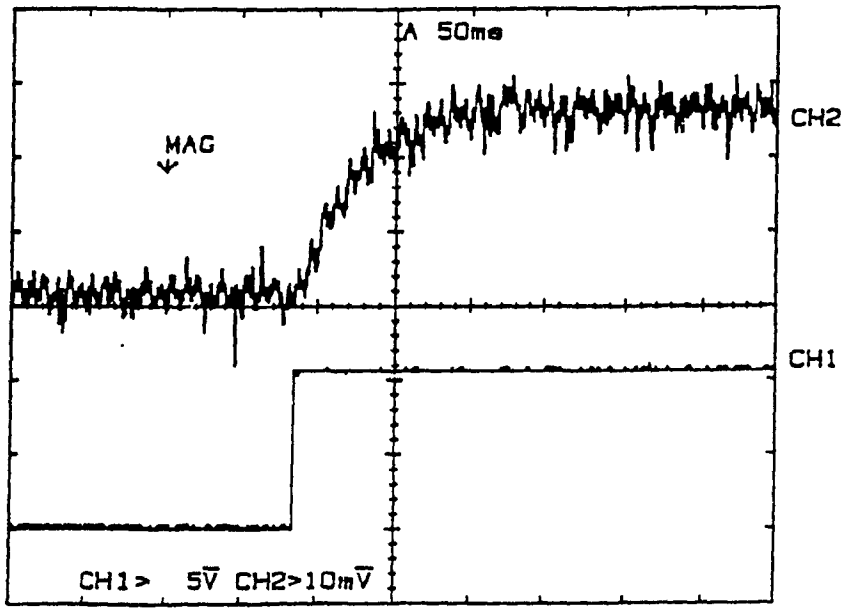


Fig. 5.2 experimental results of the response of the dc bus voltage to a step change in the reference voltage (pu).

5.3 Response to a step change in the load voltage reference

The performance of the M loop is simulated under the conditions of a step change in the load voltage reference from 0.9 pu to 1.1 pu (typical ±10% variation) and a rated load. The simulation results, Fig. 5.3, verify the predicted response of the closed M loop specified by the design objectives, giving respectively,

-- a rise time that is 10 ms, and

-- a percentage overshoot that is less than 5%.

Experimental results, as shown in Fig. 5.4, are obtained on the prototype under the same conditions as that for the simulation to confirm the simulation results.

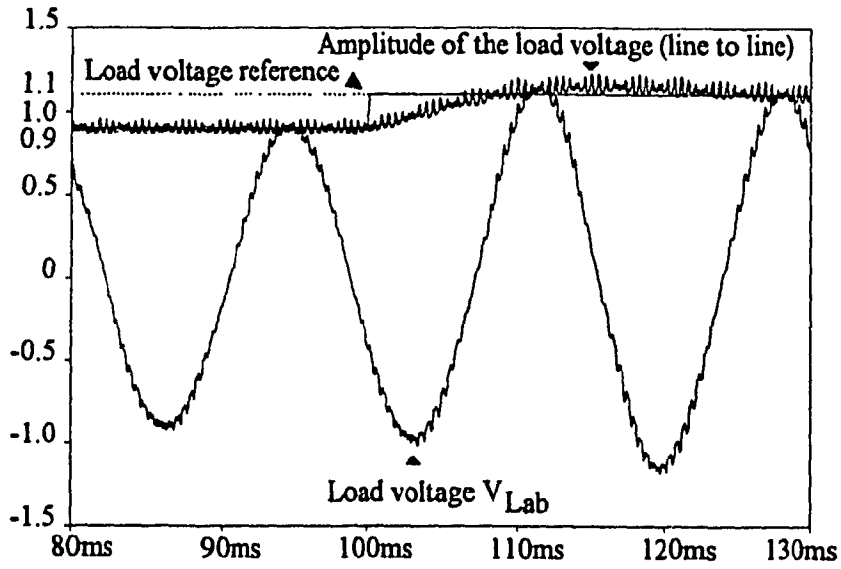


Fig. 5.3 Simulation results of the response of the load voltage to a step change in the reference (pu).

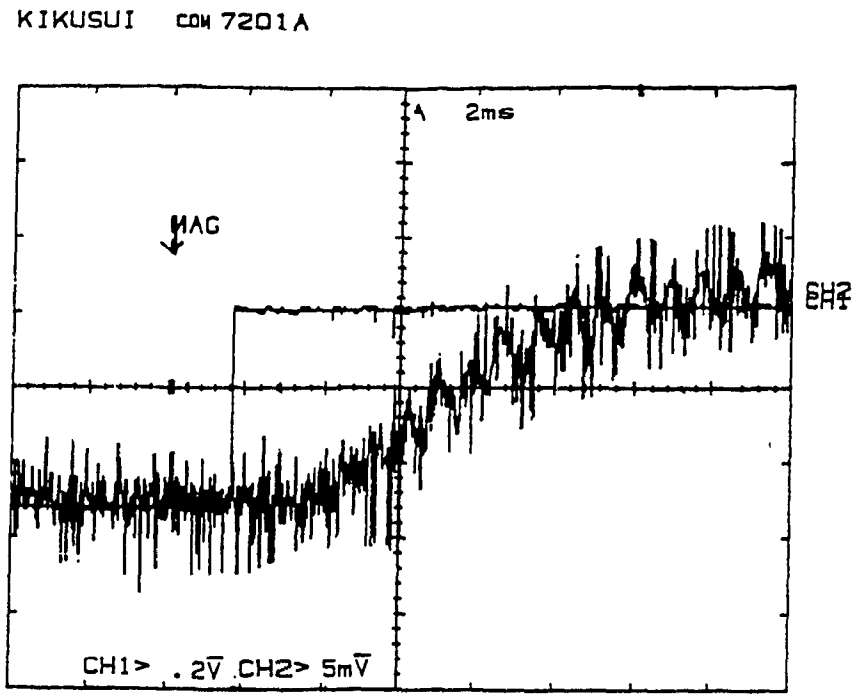


Fig. 5.4 Experimental results of the response of the load voltage to a step change in the reference voltage (pu).

5.4 Conclusions

The simulation and the experimental results validate the control loops design, which is based on the predicted closed loop responses to step changes in the references.

The results also confirm the following assumptions used for modeling :

-- The response of the M loop (100ms) is much faster than that of the δ loop (10ms). Therefore, the mutual effect between the two loops is negligible and the two loops can be designed separately.

-- Although the performance of the δ loop is carried out under the conditions of rated load, the results confirm the predicted response that is considered with neglect of the load current. Therefore, the load current does not affect the performance of the δ loop.

-- Similarly, the influence of the line current and the load current on the dynamic response of the M loop is confirmed negligible.

Moreover, the experimental results also confirm the following assumptions :

-- The delay time due to the reset cycle of the counter does not affect the validity of the design equations.

-- The effect of the quantization of the modulation index on the transient response of the system can be neglected as long as the resolution of the modulation index is high enough within the frequency range of interesting.

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 Summary of this thesis

The problems of the existing UPS systems and a proposed solution are addressed in this thesis.

In Chapter 1, potential power problems in the commercial ac supplies and the power quality requirements of the critical equipments are discussed. Various power conditioners and the general information on the solid state UPS systems are briefly introduced. The developing process of the UPS systems are reviewed. The problems associated with the input-output characteristics of the existing UPS systems are discussed.

A new UPS topology that overcomes the main drawbacks of existing UPS systems is proposed in Chapter 2. Its operating principles are illustrated in detail using equivalent circuits. A design procedure for the power circuit ratings is presented and a design example given.

Chapter 3 covers the steady state operation of the proposed UPS system. In order to validate the design procedure that is based on the predicted input-output characteristics of the system, the proposed UPS configuration using the data designed in Chapter 2, is simulated with SPICE. The simulation results are provided under the operating conditions that have been considered in the design. A 5kVA, 208V prototype is set up in the lab to confirm the simulation results.

Chapter 4 details the design of two control loops employed in the proposed UPS system. Dynamic models are constructed in order to design proper regulators. The control loops are designed in the frequency domain based on the predicted system response to

step changes in the references. The influence of the important system parameters on the performance of the control system is also studied.

The simulation and experimental results of the system dynamic responses are provided in Chapter 5 to verify the predicted performances of the two control loops designed in Chapter 4.

6.2 Conclusions of this thesis

The proposed UPS topology overcomes the two main drawbacks of the existing UPS systems : it has nearly unity power factor with very low harmonic distortion in the ac mains current, and it has high efficiency, since it uses a shunt topology. It has the other features of standard UPS systems, that is, load voltage regulation and battery charging capabilities. Further, unlike other proposed line interactive systems [12], it can compensate automatically for line or load unbalance.

The sine PWM technology eliminates all the low order voltage harmonics at the inverter ac terminals. Therefore, with a small size second order filter, a clean and continuous load current is obtained. Furthermore, a small size ac link reactor, not only contributes to correct the input power factor, but also reduces the line current harmonics below a specific value (specified by documented codes and standards [32]).

The two control loops employed in the proposed UPS system satisfy the system performance requirements. A slow loop, acting on the angle δ between line and inverter voltages, regulates the dc bus voltage to within the battery voltage variation specified by the manufacturer, thus guaranteeing that the inverter supplies no real power to the load under normal operating conditions. Furthermore, a current limit circuit ensures that the maximum battery charging current under discharged conditions does not exceed the manufacturer specified level. Another fast loop, acting on the modulation index M, regulates the load voltage. Compared with the control system employed in [12], the proposed control system is simpler.

Both the simulation and the experimental results confirm the predicted input-output characteristics and the dynamic performances of the proposed system designed in Chapter 2 and Chapter 4, thus validating the design equations.

6.3 Suggestions for future work

The implementation of the control system in this thesis uses an EPROM to store the PWM patterns. The correction of the δ error is done by resetting the counter every cycle. The time delay caused by this fact limits the response speed of the whole control system. In order to achieve faster transient response of the system, a microprocessor embedded control system could be a better alternative. With the application of the microprocessor, the PWM patterns can be generated in real time. The modulation index M and the phase angle δ associated with the patterns can be varied instantaneously, thus eliminating the time delay of the δ correction.

The synchronization of the ac mains and the inverter after ac mains' recovery has not studied yet in this thesis. The design of the synchronization circuit is complicated since the requirement of the load voltage overshoot is critical (typically less than 5% [32]). The performance of the system during the synchronization period could be an interesting topic.

The load voltage waveform is very important to critical equipments. In order to guarantee a clean and continuous load voltage under any operating conditions, the load current waveshaping control system could deserve being developed.

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APPENDIX A

SYSTEM TRANSFER FUNCTION FOR THE δ LOOP ANALYSIS

A.1 Introduction

The proposed UPS system transfer function for the performance analysis of the δ loop introduced in Chapter 4 is derived in detail in this appendix. First of all, d-q-o transformation is introduced, which is used to simplify the transient analysis of the three phase system. Secondly, system differential equations for the performance analysis of the δ loop are described. With the applications of the small signal analysis method and the Laplace transformation, the transfer function is derived from the differential equations The procedure can also be applied for the system transfer function for the M loop analysis.

A.2 D-q-o transformation

D-q-o transformation is widely used in the transient analysis of three phase system due to its unique property of converting three phase time-varying variables into time-invariant variables [33].

Three are several types of transformation matrixes available, depending on their mathematical expression forms. The matrix used in this appendix is given by,

$$\mathbf{T} = \frac{2}{3} \cdot \begin{bmatrix} \cos\omega \cdot t & \cos(\omega \cdot t - \frac{2\pi}{3}) & \cos\left(\omega \cdot t + \frac{2\pi}{3}\right) \\ \sin\omega \cdot t & \sin\left(\omega \cdot t - \frac{2\pi}{3}\right) & \sin\left(\omega \cdot t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \qquad (A.1)$$

where ω is the fundamental frequency and t the time variable.

The inversion of **T** equals to,

$$\mathbf{T}^{-1} = \begin{bmatrix} \cos\omega\cdot t & \sin\omega\cdot t & 1 \\ \cos\left(\omega\cdot t - \frac{2\pi}{3}\right) & \sin\left(\omega\cdot t - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\omega\cdot t + \frac{2\pi}{3}\right) & \sin\left(\omega\cdot t + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \tag{A.2}$$

For vectors of a three phase system,

$$\begin{aligned} v_a &= \sin(\omega\cdot t + \theta) \\ v_b &= \sin\left(\omega\cdot t + \theta - \frac{2\pi}{3}\right) \\ v_c &= \sin\left(\omega\cdot t + \theta + \frac{2\pi}{3}\right) \end{aligned} \tag{A.3}$$

where θ is the phase angle, the corresponding d-q-o components are obtained through the transformation,

$$\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} = \mathbf{T}\cdot\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \sin\theta \\ \cos\theta \\ 0 \end{bmatrix} \tag{A.4}$$

It is obviously that for a balanced three phase system, the zero axis component is zero.

A.3 System transfer function for the δ loop analysis

As mentioned in Chapter 4, the load current does not affect the system transient response within the interested frequency range. This assumption is verified by the simulation and the experimental results conducted in Chapter 5. Based on this fact and the

other assumptions made in Chapter 4 (assumptions for modeling), the system equivalent circuit for analyzing δ loop performance can be simplified, as shown in Fig. A.1 (only fundamental components are taken into account). In Fig. A.1, L_l and R_l represent the link reactor; L_{dc} and C_{dc} represent the dc bus filter; R_{dc} is the equivalent resistance for the losses associate with the filter and the battery charging; E is the battery voltage; v_{la}, v_{lb}, and v_{lc} are ac mains voltages; i_{la}, i_{lb}, and i_{lc} are ac mains line currents; d_a, d_b, and d_c are the switching functions for sine PWM voltage source inverter; and v_{dc} the dc bus voltage.

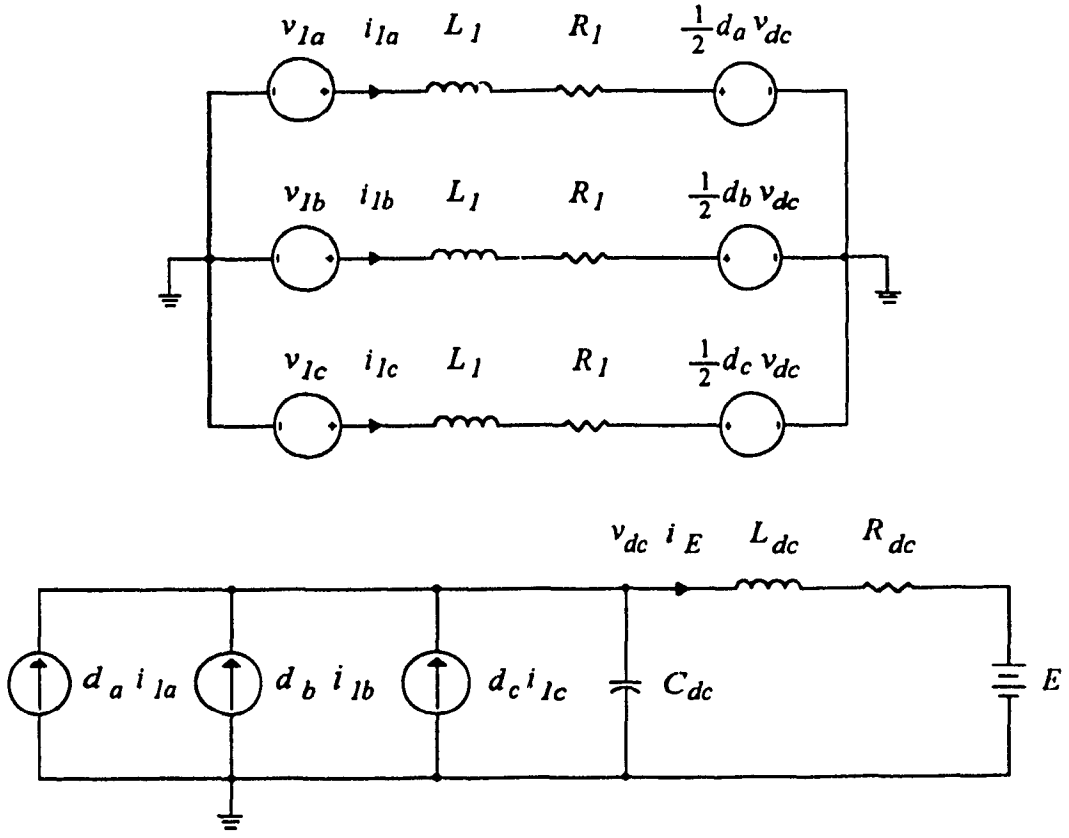

Fig. A.1 System equivalent circuit for δ loop transient analysis.

The switching functions for sine PWM patterns depend on the modulation index M and the phase angle δ,

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} M\sin(\omega \cdot t + \delta) \\ M\sin\left(\omega \cdot t + \delta - \frac{2\pi}{3}\right) \\ M\sin\left(\omega \cdot t + \delta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{A.5}$$

Based on Fig. A.1, the system performance is described by,

$$\begin{aligned} v_{1a} &= L_1 \tfrac{d}{dt} i_{1a} + i_{1a} R_1 + \tfrac{1}{2} d_a v_{dc} \\ v_{1b} &= L_1 \tfrac{d}{dt} i_{1b} + i_{1b} R_1 + \tfrac{1}{2} d_b v_{dc} \\ v_{1c} &= L_1 \tfrac{d}{dt} i_{1c} + i_{1c} R_1 + \tfrac{1}{2} d_c v_{dc} \\ d_a i_{1a} + d_b i_{1b} + d_c i_{1c} &= C_{dc} \tfrac{d}{dt} v_{dc} + i_E \\ v_{dc} &= L_{dc} \tfrac{d}{dt} i_E + i_E R_{dc} + E \end{aligned} \tag{A.6}$$

Performing d-q-o transformation on Eq. (A.6) yields,

$$\begin{aligned} &\begin{bmatrix} v_{1d} \\ v_{1q} \end{bmatrix} = R_1 \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} + L_1 \tfrac{d}{dt} \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} + \begin{bmatrix} 0 & \omega L_1 \\ -\omega L_1 & 0 \end{bmatrix} \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} + \tfrac{v_{dc}}{2} \begin{bmatrix} d_d \\ d_q \end{bmatrix} \\ &\tfrac{3}{2} \begin{bmatrix} i_{1q} & i_{1d} \end{bmatrix} \begin{bmatrix} d_q \\ d_d \end{bmatrix} = C_{dc} \tfrac{d}{dt} v_{dc} + i_E \\ &v_{dc} = L_{dc} \tfrac{d}{dt} i_E + i_E R_{dc} + E \end{aligned} \tag{A.7}$$

where v_{1d}, v_{1q} are the d axis and q axis components of ac mains voltages obtained by applying Eq. (A.4); similarly, i_{1d} and i_{1q} are d axis and q axis components of ac mains line currents; and d_d and d_q are d axis and q axis components of the switching functions.

When the δ loop is regulating the dc bus voltage, the system state variables and the control variables are fluctuating around their steady state values; that is,

$$\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} = \begin{bmatrix} I_{1d} \\ I_{1q} \end{bmatrix} + \begin{bmatrix} \hat{i}_{1d} \\ \hat{i}_{1q} \end{bmatrix}$$
$$\begin{bmatrix} d_d \\ d_q \end{bmatrix} = \begin{bmatrix} D_d \\ D_q \end{bmatrix} + \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} \qquad \text{(A.8)}$$
$$v_{dc} = V_{dc} + \hat{v}_{dc}$$
$$i_E = I_E + \hat{i}_E$$

where I_{1d}, I_{1q}, D_d, D_q, V_{dc} and I_E are the steady state values.

Substitute Eq. (A.5) and Eq. (A.8) into Eq. (A.7), and take the following assumptions into account,

a) $\sin\delta = 0$, since δ is small,

b) $\cos\delta = 1$,

c) the load voltage is constant because of the much faster M loop regulation; that is, $\frac{d}{dt}\left(mv_{dc}\right) = 0$;

the Eq. (A.7) becomes,

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = R_1 \begin{bmatrix} \hat{i}_{1d} \\ \hat{i}_{1q} \end{bmatrix} + L_1 \frac{d}{dt} \begin{bmatrix} \hat{i}_{1d} \\ \hat{i}_{1q} \end{bmatrix} + \begin{bmatrix} 0 & \omega L_1 \\ -\omega L_1 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{1d} \\ \hat{i}_{1q} \end{bmatrix} + \frac{V_{dc}}{2} \begin{bmatrix} M \\ 0 \end{bmatrix} \hat{\delta} + \begin{bmatrix} 0 \\ \frac{M}{2} \end{bmatrix} \hat{v}_{dc}$$
$$\frac{3}{2} M I_{1d} \cdot \hat{\delta} + \frac{3}{2} M \hat{i}_{1q} = C_{dc} \frac{d}{dt} \hat{v}_{dc} + \hat{i}_E \qquad \text{(A.9)}$$
$$\hat{v}_{dc} = L_{dc} \frac{d}{dt} \hat{i}_E + R_{dc} \hat{i}_E$$

Conducting Laplace transformation of Eq. (A.9) yields

$$\begin{bmatrix}0\\0\end{bmatrix}=\begin{bmatrix}L_1 s+R_1 & \omega L_1\\ -\omega L_1 & L_1 s+R_1\end{bmatrix}\begin{bmatrix}\hat{i}_{1d}\\ \hat{i}_{1q}\end{bmatrix}+\frac{V_{dc}}{2}\begin{bmatrix}M\\0\end{bmatrix}\hat{\delta}+\frac{1}{2}\begin{bmatrix}0\\M\end{bmatrix}\hat{v}_{dc}$$
$$\frac{3}{2}MI_{1d}\cdot\hat{\delta}+\frac{3}{2}M\cdot\hat{i}_{1q}=C_{dc}s\cdot\hat{v}_{dc}+\hat{i}_E \qquad (A.10)$$
$$\hat{v}_{dc}=(L_{dc}s+R_{dc})\cdot\hat{i}_E$$

where s is the Laplace operator.

Rearranging Eq. (A.10), the system transfer function for the δ loop performance analysis is given by,

$$\frac{\hat{v}_{dc}}{\hat{\delta}}=\frac{k_0(p_1 s+p_0)}{q_4 s^4+q_3 s^3+q_2 s^2+q_1 s+q_0} \qquad (A.11)$$

where

$$k_0=\frac{3M^2}{4}\omega_0 L_1 V_{dc}$$
$$p_1=L_{dc}$$
$$p_0=R_{dc}$$
$$q_4=L_{dc}C_{dc}L_1^2$$
$$q_3=2L_{dc}C_{dc}R_1L_1+R_{dc}C_{dc}L_1^2$$
$$q_2=L_{dc}C_{dc}\omega_0^2L_1^2+2R_{dc}C_{dc}R_1L_1+L_1^2+\frac{3M^2}{4}L_{dc}L_1$$
$$q_1=R_{dc}C_{dc}\omega_0^2L_1^2+2R_1L_1+\frac{3M^2}{4}(L_{dc}R_1+R_{dc}L_1)$$
$$q_0=\omega_0^2L_1^2+\frac{3M^2}{4}R_{dc}R_1$$
$$\omega_0=2\pi\cdot\text{fundamental frequency}$$

M = the modulation index of the sine PWM pattern.

APPENDIX B

POWER AND CONTROL CIRCUIT DIAGRAM

The power and control circuit diagram for the experimental prototype is provided in this appendix. The prototype was set up using the power circuit parameters designed in Chapter 2 and the control loops designed in Chapter 4.

The overall diagram is divided into several parts. In Fig. B.1, the structure of the power circuit is provided. Figs. B.2 and B.3 present the implementations of the feedback for the δ loop and the M loop respectively. Gating signal generation is described in Fig.B.4. A base drive circuit for bipolar junction transistor (BJT) is shown in Fig. B.5. The six base drives (for six switches) used in the prototype are identical in circuit. Finally, the data of BJTs used in this thesis are provided in Fig. B.6.

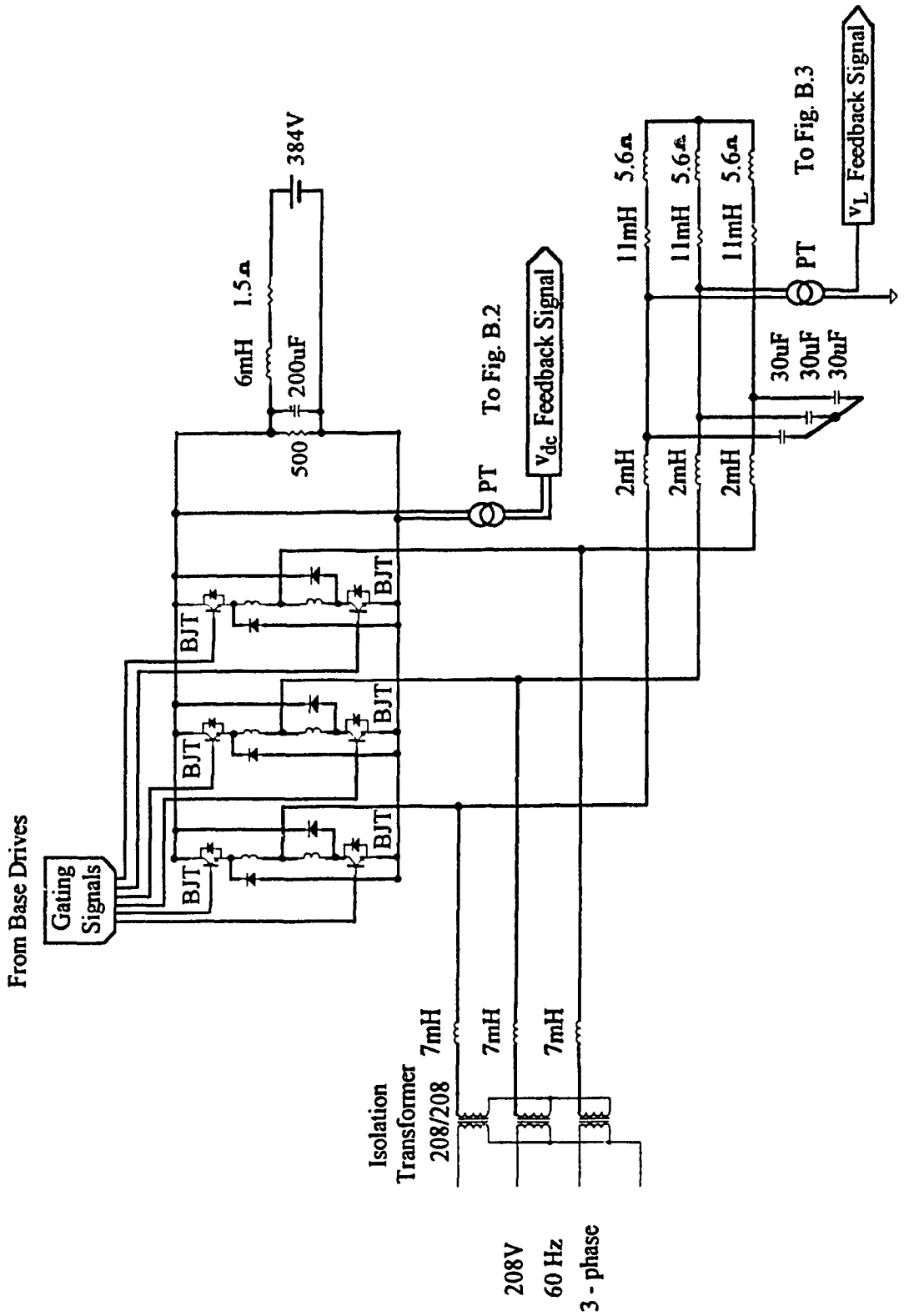

Fig. B.1 Power circuit of the prototype.

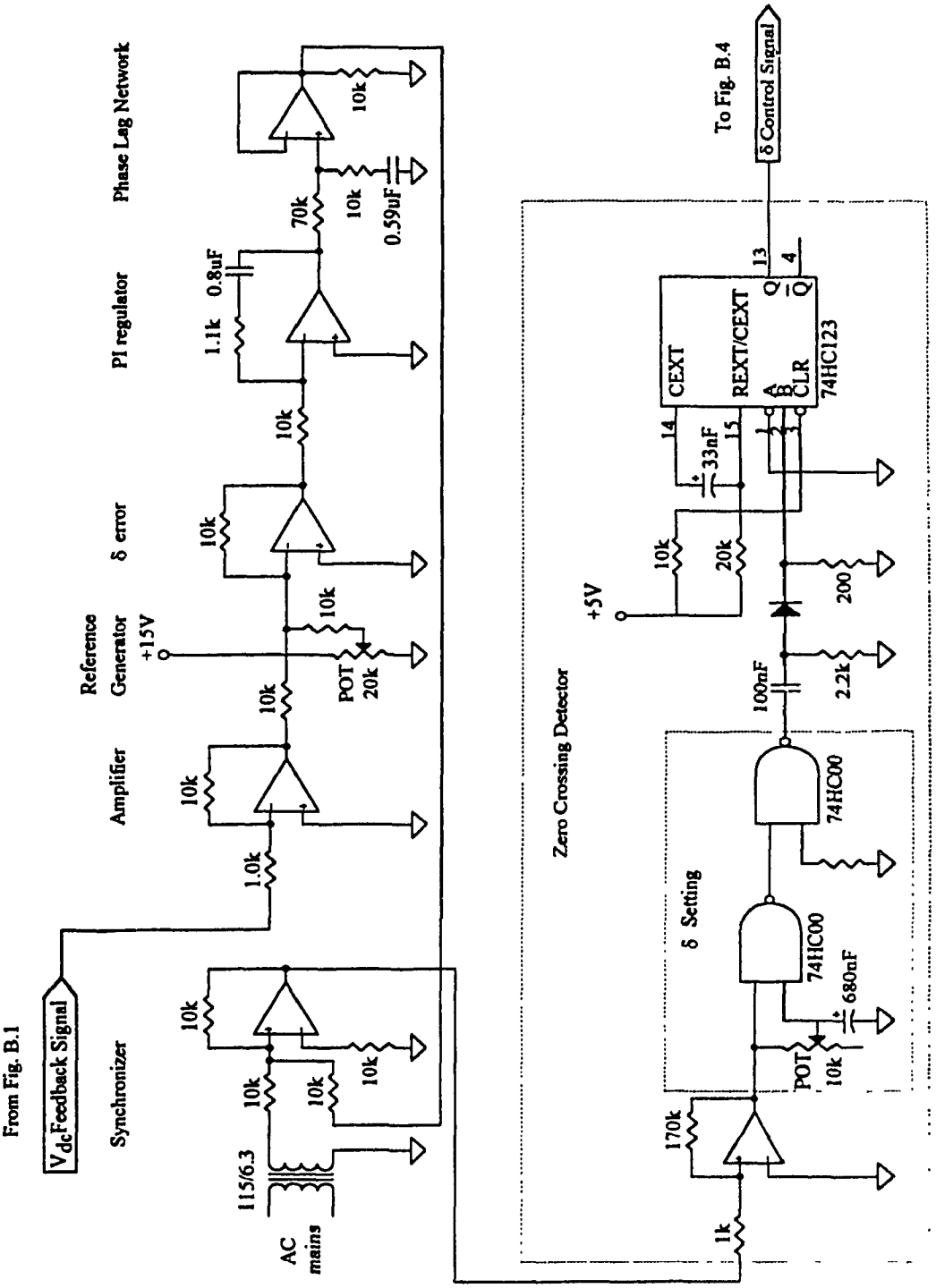

Fig. B.2 Implementation of the δ loop feedback.

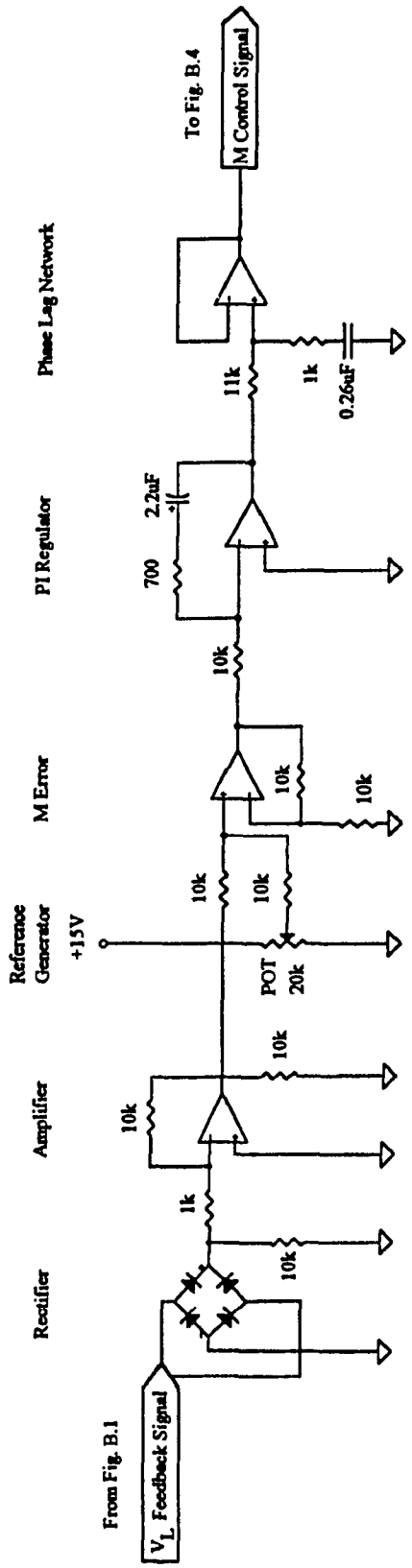

Fig. B.3 Implementation of the M loop feedback.

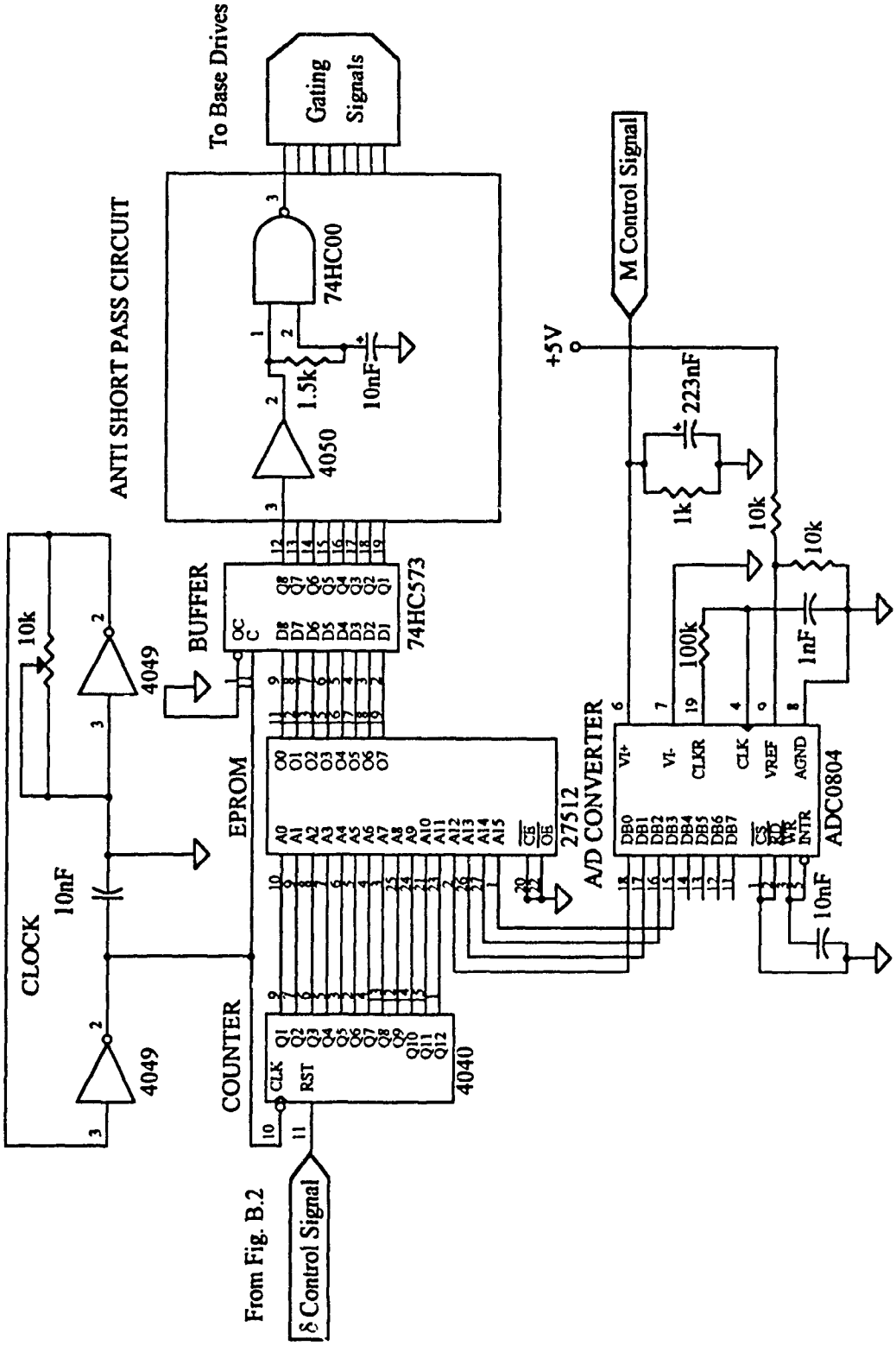

Fig. B.4 Gating signal generating circuit.

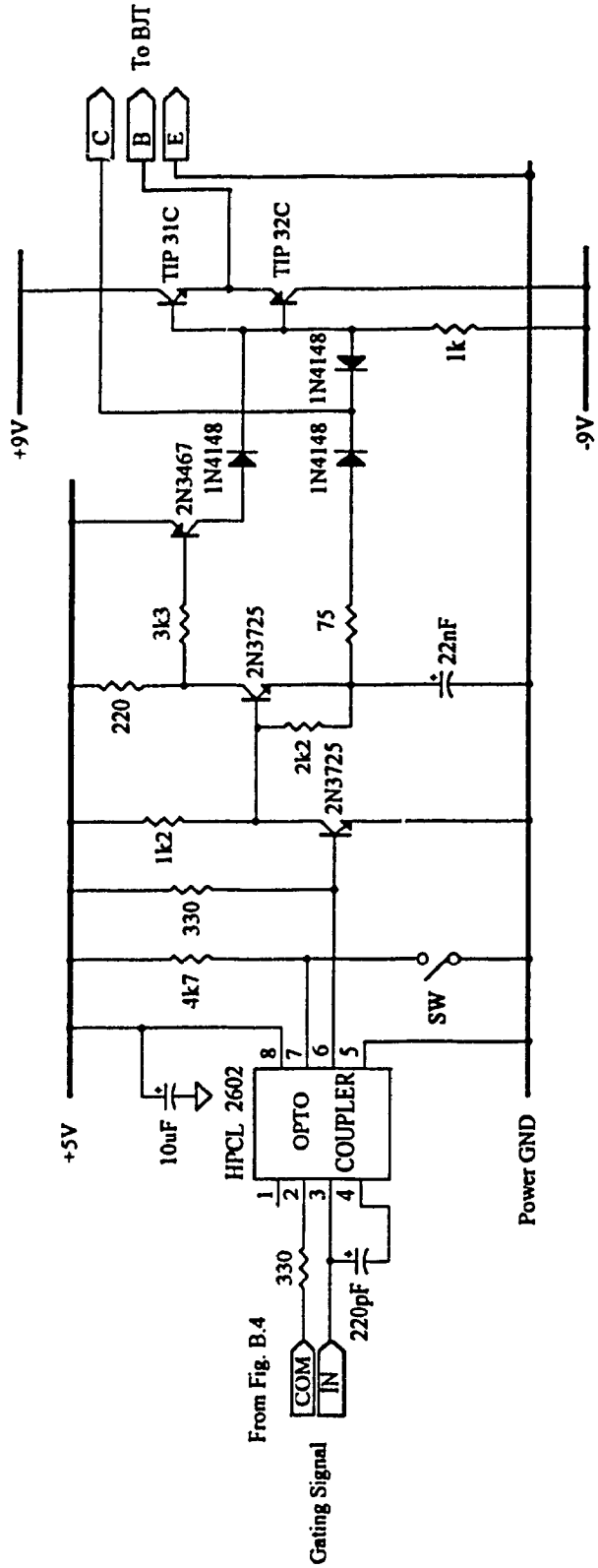

Fig. B.5 Base drive circuit for the bipolar junction transistor (BJT).

Type : *POWEREX* KT224512

Ratings : $V_{CEO(SUS)}$ = 450 V

V_{CEV} = 600 V

Current = 120 A

Equivalent Circuit :

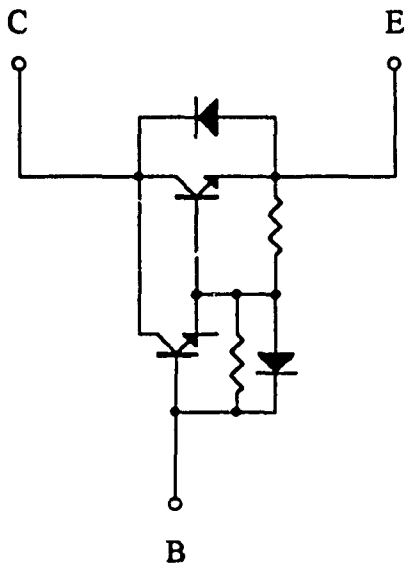

Fig. B6 Data of the BJT switch used in the prototype.