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HIGH PERFORMANCE ON-LINE CONTROL OF THREE-PHASE PWM CURRENT-SOURCE CONVERTERS

José R. Espinoza

A Thesis

in

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of

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Presented in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy at
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ABSTRACT

HIGH PERFORMANCE ON-LINE CONTROL OF THREE-PHASE PWM CURRENT-SOURCE CONVERTERS

José R. Espinoza, Ph.D.
Concordia University, 1996.

In medium and high power applications, two topologies have evolved for three-phase six-switch static power converters with an intermediate dc link, the voltage-source and the current-source. Despite the advantages of the current-source topology such as current limiting, higher reliability, and low ac-voltage harmonic distortion, voltage-source topologies are more widely used. This is in part due to the fact that current-source topologies present the following difficulties: (a) a lack of on-line modulating techniques that satisfy all the constraints of their gating signals and (b) the complexity of the control schemes for medium and high power applications. This thesis provides solutions to these problems. It proposes two enhanced on-line modulating techniques and three control schemes for three-phase six-switch current-source topologies, namely: (a) an on-line carrier-based PWM modulating technique, (b) an on-line PWM space-vector based modulating technique with reduced switching frequency, (c) an inner voltage control loop and an outer modulation index control loop for inverter topologies, and (d) a non-linear control scheme for rectifier topologies. The resulting power conversion schemes demonstrate the intrinsic advantages of the current-source topology and none of the disadvantages of the voltage-source topology. Moreover, they can be operated at reduced switching frequency, unity displacement power factor in the rectifier mode, minimum and constant load harmonic distortion, and allow the topology to provide high quality load waveforms and fast dynamic response. Simulated and experimental tests validate the theoretical considerations.

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Dedicated to the memory of my parents,

Víctor and María.

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Topologies

CS : Current-Source

VS : Voltage-Source

CSC : Current-Source Converter

VSC : Voltage-Source Converter

CSI : Current-Source Inverter

VSI : Voltage-Source Inverter

CSR : Current-Source Rectifier

VSR : Voltage-Source Rectifier

VC-CSI : Voltage-Controlled Current-Source Inverter

CC-VSI : Current-Controlled Voltage-Source Inverter

Power Switches

SCR : Silicon controlled rectifier

BJT : Bipolar junction transistor

MOSFET : Metal-oxide-semiconductor field effect transistor

GTO : Gate-turn-off thyristor

IGBT : Insulated-gate-bipolar transistor

MCT : MOS-controlled thyristor

General

HVDC : High Voltage dc

PWM : Pulse Width Modulation

ASD : Adjustable Speed Drive

THD : Total Harmonic Distortion

DF : Distortion Factor

SV : Space Vector

SVM : Space Vector Modulation

EPROM : Erasable Programable Read-Only Memory

LIST OF MAIN SYMBOLS

Voltage and Current Vectors

$[i_s]_{uvw}$: 3-ϕ supply currents, $uvw = abc$, $\alpha\beta\gamma$, or $dq0$ frame, $[i_s]_{uvw} = [i_{su}\ \ i_{sv}\ \ i_{sw}]^T$

$[i_r]_{uvw}$: 3-ϕ rectifier currents, $[i_r]_{uvw} = [i_{ru}\ \ i_{rv}\ \ i_{rw}]^T$

$[i_i]_{uvw}$: 3-ϕ inverter currents, $[i_i]_{uvw} = [i_{iu}\ \ i_{iv}\ \ i_{iw}]^T$

$[i_l]_{uvw}$: 3-ϕ load currents, $[i_l]_{uvw} = [i_{lu}\ \ i_{lv}\ \ i_{lw}]^T$

$[v_s]_{uvw}$: 3-ϕ supply voltages, $[v_s]_{uvw} = [v_{su}\ \ v_{sv}\ \ v_{sw}]^T$

$[v_r]_{uvw}$: 3-ϕ rectifier voltages, $[v_r]_{uvw} = [v_{ru}\ \ v_{rv}\ \ v_{rw}]^T$

$[v_i]_{uvw}$: 3-ϕ inverter voltages, $[v_i]_{uvw} = [v_{iu}\ \ v_{iv}\ \ v_{iw}]^T$

$[v_l]_{uvw}$: 3-ϕ load voltages, $[v_l]_{uvw} = [v_{lu}\ \ v_{lv}\ \ v_{lw}]^T$

$[m_r]_{uvw}$: 3-ϕ rectifier modulation indexes, $[m_r]_{uvw} = [m_{ru}\ \ m_{rv}\ \ m_{rw}]^T$

$[m_i]_{uvw}$: 3-ϕ rectifer modulation indexes, $[m_i]_{uvw} = [m_{iu}\ \ m_{iv}\ \ m_{iw}]^T$

Voltage, Current and Power

V : voltage space vector associated with $[v]_{abc}$

v_i : CSI dc link bus voltage

v_r : CSR dc link bus voltage

v_c : carrier voltage waveform

$V_{r,min}$: minimum dc link voltage in a VSR (peak line-to-line supply voltage)

$V_{r,max}$: maximum dc link voltage in a CSR ($0.866 \cdot V_{r,min}$)

$V_{i,max}$: maximum dc link voltage in a CSI (0.866 times the peak line load voltage)

I : current space vector associated with $[i]_{abc}$

i_{dc} : dc link current

$I_{r,min}$: minimum dc link current in a CSR for unity power factor

$I_{r,max}$: maximum dc link current in a VSR

$I_{i,max}$: maximum dc link current in a CSI

p : instantaneous real (active) power

q : instantaneous imaginary (reactive) power

Modulating Techniques

m_r : rectifier modulation index

m_i : inverter modulation index

M_r : rectifier modulation index SV

M_i : inverter modulation index SV

G_{ac} : modulating technique ac gain

G_{dc} : modulating technique dc gain

V_c : carrier waveform amplitude

Filter Parameters

L_r : rectifier filter inductance

L_{dc} : dc link filter inductance

C_{dc} : dc link filter capacitance

C_r : rectifier filter capacitance

C_i : inverter filter capacitance

Frequency and Period

f_s : utility frequency (60 Hz)

f_l : load frequency

f_c : carrier waveform frequency

ω_s : supply angular frequency ($\omega_s = 2\pi f_s$)

ω_l : load angular frequency ($\omega_l = 2\pi f_l$)

f_{cycle} : space vector frequency

f_{sw} : switching frequency

f_{rr} : rectifier filter resonance frequency

f_{ir} : inverter filter resonance frequency

t_c : carrier waveform period

t_{cycle} : space vector period

t_{sw} : switching period

Controller Parameters

k_{idc} : dc link current controller proportional gain

t_{idc} : dc link current controller integral gain

$t_{s,idc}$: dc link current controller settling time

b_{idc} : dc link current controller settling band

ξ_{idc} : dc link current controller damping ratio

k_{vl} : load voltage controller proportional gain

t_{vl} : load voltage controller integral gain

$t_{s,vl}$: load voltage controller settling time

b_{vl} : load voltage controller settling band

ξ_{vl} : load voltage controller damping ratio

k_{mi} : inverter modulation index controller proportional gain

t_{mi} : inverter modulation index controller integral gain

$t_{s,mi}$: inverter modulation index controller settling time

b_{mi} : inverter modulation index controller settling band

ξ_{mi} : inverter modulation index controller damping ratio

k_{mr} : rectifier modulation index controller proportional gain

t_{mr} : rectifier modulation index controller integral gain

$t_{s,mr}$: rectifier modulation index controller settling time

b_{mr} : rectifier modulation index controller settling band

ξ_{mr} : rectifier modulation index controller damping ratio

Induction Machine Parameters

R_a : armature resistance

R_r : rotor resistance

L_a : armature inductance

L_r : rotor inductance

L_M : magnetizing inductance

v_{emf} : back emf voltage

CHAPTER 1

INTRODUCTION

1.1 GENERAL INTRODUCTION

Electrical energy is primarily distributed as ac voltage at constant amplitude and frequency. However, the electrical requirements of most of the loads can assume different forms. For instance, in a modern adjustable speed drive (ASD), induction machines require a variable ac voltage and frequency supply as the speed requirements vary. Therefore, to interface a load to the ac mains, a power conversion system is required (Fig. 1.1(a)).

Electrical power conversion today is achieved by means of static power converters. This is mainly the result of their higher efficiency and their enhanced controllability, leading to an improvement in the overall efficiency of the system. However, practical power conversion systems based on static power converters do not behave in an ideal manner (Fig. 1.1(b)). Near unity input power factor operation is difficult to achieve and the static and dynamic requirements of the load are hard to meet. For example, ASDs, based on a voltage dc link, generate load voltages of the Pulse Width Modulated (PWM) type instead of the sinusoidal type, and inject pulsating line currents into the distribution system instead of sinusoidal shaped waveforms (Fig. 1.1(c)).

In general, the performance of a static power conversion scheme is dictated by the limitations inherent in the available power semiconductor switches, the power circuit topology, the modulating technique, and the control schemes. These general

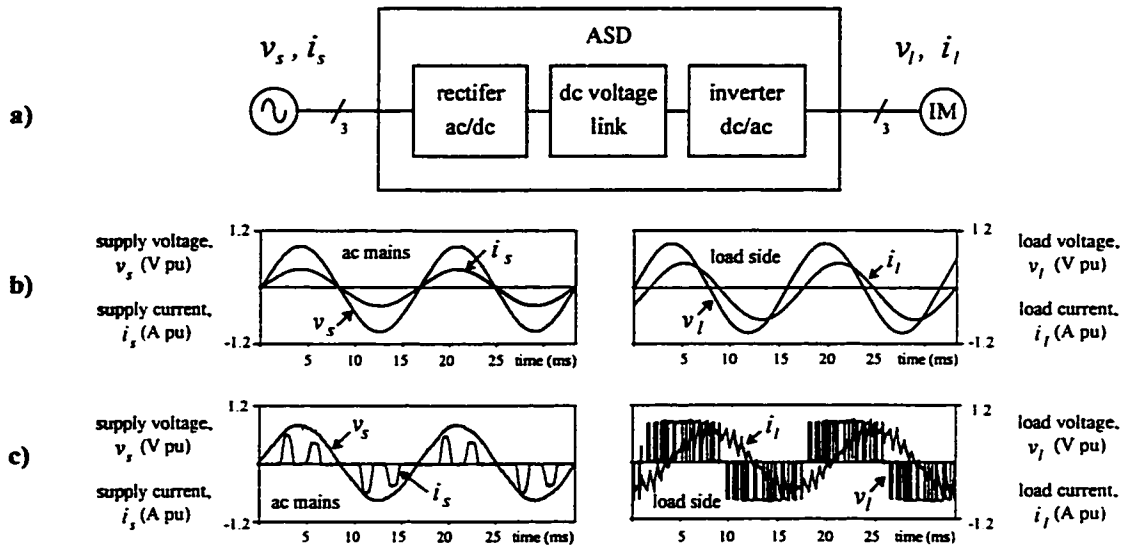

Fig. 1.1 A typical ASD scheme and associated waveforms.

a) The electrical power conversion topology. **b)** The ideal input (ac mains) and output (load) waveforms. **c)** The actual input (ac mains) and output (load) waveforms.

considerations are discussed in the next section.

1.1.1 Basic Three-Phase Power Conversion Structures

Static power converters are basically a network of power switches that are gated in a way to achieve the required power control objectives. The gating is generated by a modulation technique that is usually of the PWM type and the control objectives depend upon the load and supply requirements. These conversion schemes interface the ac mains with a specific load. The power circuit topology, modulating technique and control strategy used in these schemes define the overall advantages, drawbacks and limitations [1-3].

A. The Static Power Converter - Load Interaction

Voltage-source topologies are the preferred topologies on the load side, Fig.

1.2(b) and Fig. 1.2(c). This is mainly a result of the following: (a) they can operate under all output voltage/frequency ranges without any major restriction, (b) they can provide fast and accurate line current control, and (c) they are simple to modulate and control [4-6].

Current-source (CS) inverters are the dual topology of voltage-source inverters with voltage waveforms becoming current waveforms and vice versa [7-9] (Fig. 1.2(d)). Duality however implies three differences in favor of CS topologies: (a) the converter is more reliable due to the inherent load and converter short-circuit protection, (b) there is a very low load voltage *dv/dt* resulting from the filtering effect of the output capacitor, and (c) the system has instantaneous and continuous regenerative capabilities (Table 1.1).

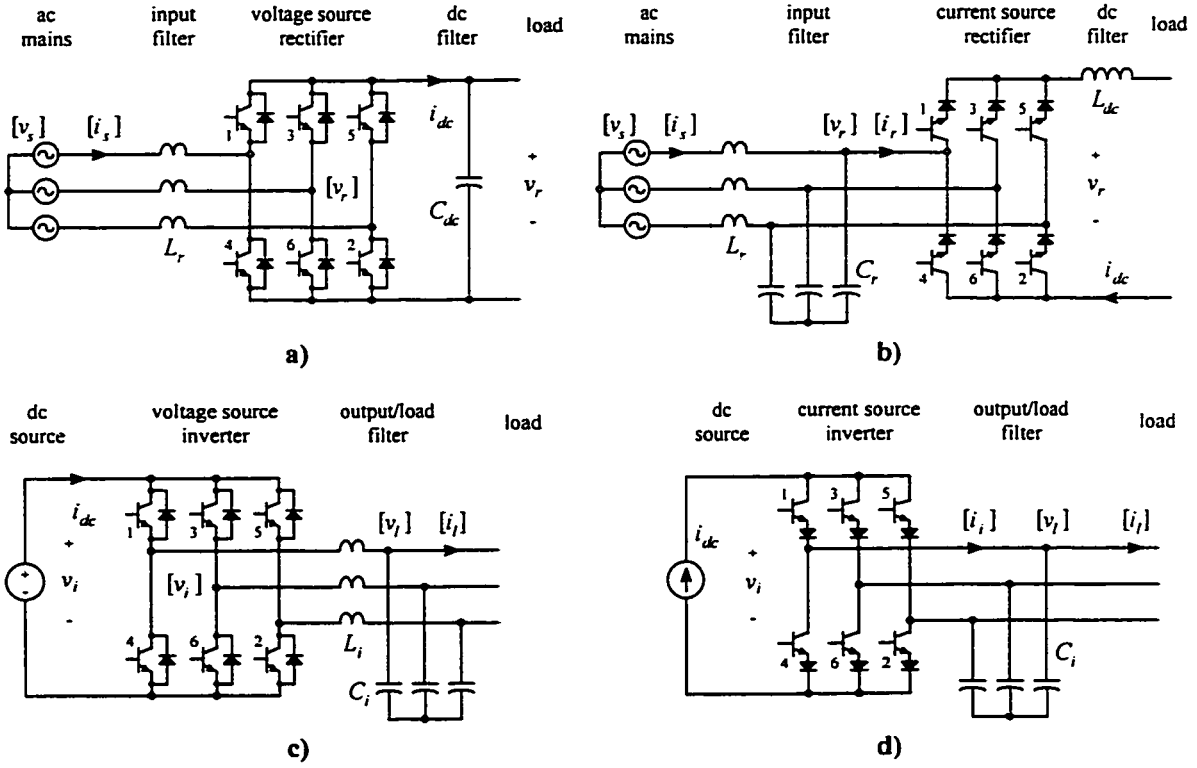

Fig. 1.2 Generalized three-phase six-switch voltage and current-source converters.

a) A voltage-source rectifier (VSR). **b)** A current-source rectifier (CSR). **c)** A voltage-source inverter (VSI). **d)** A current-source inverter (CSI).

These features make the structure attractive for medium and high power applications, where reliability is of main concern.

However, the implementation of PWM-CS topologies on the load side is complicated by a number of factors, among which, (a) lack of on-line modulation techniques due to the complexity of the gating requirements; this has resulted in the widespread use of selective harmonic elimination stored patterns, usually at a fixed modulation index, leading to slow dynamic response; (b) in those control schemes that use stored patterns and variable dc link current control, it is possible to have potential resonances between the output filter and load inductance; and (c) in those control schemes that use fixed nominal dc current and a variable inverter modulation index, there are additional losses in the dc link inductor and switches, the switches operating at rated current conditions at all times.

Table 1.1 Three-Phase Six-Switch Converter Comparison.

Converter Parameter	Converter			
	VS Rectifier	CS Rectifier	VS Inverter	CS Inverter
load filter	capacitive	inductive	inductive	capacitive
input filter order	first	second	unnecessary ♣	unnecessary ♣
output filter order	first	first	second *	first
possible resonance	no	yes (supply side)	yes (load side) *	yes (load side)
protected against	load open circuit	load short circuit	load open circuit	load short circuit
control modes	closed	closed/open	closed/open	closed/open
power flow control	dc current	dc voltage	dc current	dc voltage
dc volt. range (V_{dc})	$V_{dc} > V_{r,\min}$	$V_{r,\max} > V_{dc} > -V_{r,\max}$	$V_{dc} > 0$	$V_{i,\max} > V_{dc} > -V_{i,\max}$
dc curr. range (I_{dc})	$I_{r,\max} > I_{dc} > -I_{r,\max}$	$I_{dc} > I_{r,\min}$	$I_{i,\max} > I_{dc} > -I_{i,\max}$	$I_{dc} > 0$

* The second-order output filter (load side) is optional.
♣ An ideal dc supply is assumed.

B. The AC Mains - Static Power Converter Interaction

An important number of power conversion schemes use uncontrolled (diode-based) or controlled (thyristor-based) rectifiers as front-end converters to interface with the ac mains. These topologies feature reactive power (var) consumption and harmonic current injection into the distribution system. This results in low input power factor that increases the cost of operation and the losses in the line. Also, the current harmonics will distort the supply line current and through the line impedances, distorted voltages will appear on the ac system (Fig. 1.1(c)). These can interfere with other loads and converters resulting in resonances, malfunction of protections and control circuits, and interference with communication circuits [10-11].

An alternative to minimize harmonic pollution is to replace the thyristor and diode based front-end ac-dc rectifiers with PWM current-source (CS) rectifiers (Fig. 1.2(d)). These are fundamentally inverters synchronized to the ac mains. Appropriate control of these converters can provide unity displacement power factor and reduced input current harmonic distortion regardless of the load demand. However, the configuration has two significant drawbacks, which are not overcome with off-line pattern generators: (a) the input *LC* filter can easily resonate, and (b) the ac side of the topology behaves as a second-order non-linear system. Therefore, the topology requires an appropriate on-line gating scheme and a suitable control scheme typically based on either a stationary (*abc* or $\alpha\beta\gamma$) or a rotating frame (*dq0* frame).

1.1.2 Current Source Converter Implementation Issues

From the previous discussion, it can be concluded that existing current-source

inverters and rectifiers present intrinsic advantages such as high reliability and low ac voltage harmonic distortion. These advantages make attractive the CS topology in medium and high power applications. However, they have received less attention because of the difficulty of on-line PWM switching pattern generation and control.

Therefore, the main objectives is to provide high performance on-line PWM techniques and enhanced control schemes for both current-source inverters and rectifiers. The resulting power conversion schemes should feature, (a) unity input displacement power factor for rectifier applications, (b) high conversion efficiency, (c) high reliability, and (d) high quality load waveforms for inverter applications. These features should hold for steady state and during transient conditions of the load. This is the focus of the thesis.

1.2 PREVIOUS WORK

The review of previous work in this area is divided into three categories: (a) on-line PWM techniques, (b) control schemes on the inverter-load side, and (c) control schemes on the ac mains-rectifier side.

1.2.1 On-Line PWM Techniques

The CS converter have been the subject of a number of publications where the modulation is based on off-line pattern generation [12-17]. This has allowed the optimization of the pattern and simplified the compliance of the special requirements of the gating signals. Non-standard topologies on-line modulated have also been proposed; however, they require additional power switches beyond the requirements of the standard six-switch configuration [18-23]. This increases the cost and reduces the overall system

reliability, an important consideration in high power applications. Ooi, et al [24] developed an on-line carrier-based modulator for the six-switch topology. However, it must be modified as the carrier frequency is modified. Some studies in the VS converter have demonstrated that non-standard modulating signals can further improve the performance of the modulating technique by increasing the voltage/current utilization and reducing the switching frequency [25-27].

The availability of fast and inexpensive digital signal processors has lead to an increasing number of digital control schemes that require an on-line digital modulating technique [28-30]. A useful digital modulator is based on the Space Vector (SV) transformation which allows direct implementation of enhanced control schemes in the *dq0* and $\alpha\beta\gamma$ frames [31-35]. In order to optimize the SV technique, recent work has investigated the optimum switching sequence [36-39], operation under overmodulation [40-42], operation under unbalanced conditions [43], and minimization of uncharacteristic harmonics [44]. Although this modulating technique was initially developed for the VS converter, its application to the CS converter has also been successful [45]. However, in the case of the CS topology, studies related to switching sequence, harmonic distortion, and uncharacteristic harmonics have seldom been attempted [46].

1.2.2 Control Schemes for the Load Side Inverter

A refined three-phase variable voltage and frequency power supply is presented in [47]. Transient optimization issues of the topology are addressed in [48]. The topology is based on symmetrical VS converters and features (a) unity input power factor, (b)

regeneration capabilities, (c) acceptable input/output performance, and (d) fast and accurate line current control [29-30, 49]. Novel front-end rectifiers based on voltage source rectifiers are also introduced in [50-52]. However, these configurations only operate with a minimum dc link voltage which must be higher than the supply line peak voltage for unity power factor operation, even for light loads. Therefore, at low load voltages, the converter generates high harmonic distortion, which is load voltage dependent. Moreover, for fast fluctuating loads, refined control strategies are required [53-55].

The dual topology based on CS inverters presents low load voltage harmonic distortion due to the load filter [56]. Traditionally, the control scheme has been controlling the dc link current [57]. However, this scheme has a poor dynamic response. Moreover, if a thyristor front-end rectifier is used, the input power factor is low and load dependent [58]. Still, the intrinsic advantages of CS converters, such as low *dv/dt*, high reliability, and inherent current limiting capabilities make the topology attractive and hence recent work has been proposed to improve the standard configuration. This work includes, new topologies [22], PWM techniques applied to the CS inverter (CSI) [13, 23, 59], and PWM techniques applied to both the CS rectifier (CSR) and the CS inverter (CSI) [56, 60]. Moreover, to improve waveform quality and speed of response, new control schemes through dc link current control [61-62] and through modulation index control of the CSI [63-64] have been reported. Finally, integration of the dc link current and CSI modulation index control has also been reported [65]; however, this last work assumes a known load variation, this is not true in the general case.

AC adjustable-speed induction-motor drives based on either scalar or vector control employ mostly a VS inverter (VSI) to control the motor armature [67-69]. On the other hand, the implementation of a CSI based drive system [70-72] is complicated by a number of factors. First, the complexity of the CSI gating signals compared to the VSI gating signals, this has resulted in the widespread use of Selective Harmonic Elimination (SHE) stored patterns [15][64][73]. Second, in those control schemes that use stored patterns, such as SHE, and variable dc link current to control the output current, it is possible to have potential resonances between the output filter capacitor and the motor leakage inductance [62][74]. Finally, in those control schemes that use fixed dc current and a variable modulation index PWM generator at the CSI stage to control the output current, it is found that there are important losses in the switches and dc inductor, and stress to the power switches (they commutate at maximum current), and the harmonic distortion of the motor voltage varies with the CSI modulation index [23][75-76].

1.2.3 Control Schemes for the AC Mains Rectifier

PWM-CS rectifiers are gradually replacing line commutated thyristor rectifiers as front-end ac/dc converters since they can provide unity power factor. In conventional schemes, the PWM-CSR has operated with off-line patterns which result in a slow transient response. On the other hand, the presence of the *LC* input filter causes a load dependent input displacement power factor and may produce transient oscillations. Although oscillations can be attenuated by adding damping resistors, they reduce the overall conversion efficiency. Recently, attempts have been made to operate the rectifier by means of on-line current control [77-81]. The main goals have been to keep unity

displacement power factor, to eliminate the damping resistors, and to regulate either the dc voltage or the dc current. Solutions that meet the main requirements by using state variable feedback compensation have been proposed [77-78]. However, only unity power factor operation is allowed [77]. On the other hand, the use of a small signal model reduces the generality of the approach [78]. The input displacement power factor is compensated by using a linear approximation that is not accurate at light loads [79]. Finally, [80] achieves near unity power factor; however, drawbacks include low voltage utilization and low switch utilization; and [81] provides active damping; however, it is an approximated method.

The independent control of the supply reactive and active power components has also been proposed [82]. However, due to the non-linear and coupled behavior of the converter, both quantities are not independently controlled. Non-linear control based on state variable feedback linearization has already been introduced as a control alternative in power electronic systems [83-85]. This approach can be readily implemented in *dq0* coordinates [86]. Among its advantages are the system state variable linearization, and decoupling and dynamic specification.

Several publications have analyzed the non-linear and coupled model of the PWM-CSR feeding a passive load. Control schemes based on a state variable feedback strategy and a cascade structure have been proposed [45, 87]. However, both analyses are based on a small signal model and as the actual operating point moves away from the nominal one, the performance deteriorates, specially in terms of dynamic response. The analysis of the power configuration for a connection to an active load [88], and design

guidelines when a proportional controller is used are also provided [89]. However, since the dc side behaves as a first order system, this controller does not provide the fastest response. Thus, a higher order controller would be desirable; however, the method presented to identify the stable regions becomes involved. New control strategies which include the use of the instantaneous dc power demand as a feedforward variable have proved their superiority [90-91]. They can further minimize the size of passive components and allow the regenerative operation mode within safe stability margins. This control approach has not been used in CSR applications.

1.3 SCOPE OF THE THESIS

The objective of this thesis is to propose enhanced on-line PWM techniques and control schemes for three-phase six-switch CS topologies. The purpose is to make CS converters to achieve the same dynamic and static performance as VS converters.

The modulating techniques are developed in such a way that the CS converter becomes an ideal current amplifier with minimum switching frequency and thereby, enhanced control schemes can be applied. The proposed control schemes are analyzed and implemented to allow high performance operation of the power conversion system, including input displacement power factor control and high quality load waveforms. This thesis makes six specific and related contributions to the control of current source converters.

Modulating Techniques:

i) An on-line carrier-based PWM pattern generator is proposed [92].

ii) A dead-band carrier-based modulating technique is developed [93].

iii) The space vector modulation applied to CS converters is investigated [94-96].

Control Schemes:

iv) A variable voltage/frequency power supply based on a CSI is proposed [97].

v) A modulation index control loop for CS inverters is proposed [98-101].

vi) A non-linear control scheme for CS rectifiers is investigated [102-104].

1.3.1 Contributions to On-Line PWM Techniques

An analog on-line PWM carrier-based gating pattern generator for three-phase six-switch CS topologies is proposed. The circuit realization requires only three modulating signals and a carrier signal. It features, (a) reduced switching frequency, (b) smooth transition in and out of the overmodulation region, and (c) safe operation by integrating all the special requirements of the CS topology (such as shorting paths to generate zero line currents and over-laps to avoid interruptions of the dc link current).

An on-line modulating technique for CS converters, that uses three dead-band modulating signals, is proposed. However, instead of a triangular carrier, it uses a saw-tooth carrier signal. Thus, the switching frequency is further reduced to about 1/2 of the carrier without penalty on the harmonic distortion.

The digital on-line modulating technique based on space vector applied to CS converters is investigated. Three sequences of space vectors are further optimized to achieve minimum harmonic distortion and minimum switching frequency. Thus, switching frequencies at most 1/2 of the cycle frequency are obtained. Additional studies include minimization of uncharacteristic harmonics and delay compensation.

1.3.2 Contributions to Control Schemes

A three-phase variable ac voltage/frequency power supply based on a CSI is proposed. The converter is controlled by a load voltage feedback scheme. It features low *dv/dt* across the load and time responses of the order of either the carrier (for analog implementations) or cycle period (for digital implementations).

A modulation index control loop for CS inverters is proposed. It ensures near unity modulation index of the converter regardless of the load demand. The scheme leads to high switch utilization, minimum conduction losses, and fixed load harmonic distortion.

A non-linear control scheme for CS rectifiers is investigated. The approach allows independent control of the active (real) and reactive (imaginary) power components of the ac mains. The scheme features (a) a linearized state variable model, (b) decoupling of the real and imaginary line current components, (c) elimination of damping resistors, and (d) reduced current harmonic distortion.

The above modulating and control schemes are applied to standard and new applications of CS converters to probe their feasibility and improved performance. These are: (a) a fully functional variable voltage/frequency power supply based on symmetrical CS topologies for both front-end and load converters, (b) a CSI based induction motor drive and (c) a variable dc current-source based on a CS rectifier.

1.4 Outline and Methodology

The thesis is organized as follows.

Chapter 2 investigates an on-line carrier-based pattern generator and an improved

modulating technique. The pattern generator is best suited for analog control scheme implementations. A practical circuit realization of the proposed pattern generator is also included. The pattern generator extends the duality between VS converters and CS converters beyond the power circuit topology. In particular, all the carrier-based PWM techniques, such as Sinusoidal PWM (SPWM), can now be applied to CS converters. An improved modulating technique is obtained by replacing the standard sinusoidal signals by dead-band type of waveforms, and by replacing the standard triangular carrier signal by a saw-tooth type of signal. Simulation and experimental results on a 5 kVA prototype are included to verify the feasibility of the proposed circuit and modulating technique [92-93].

The space vector modulating technique applied to CS converters is investigated in Chapter 3. Specifically, three space vector sequences are analyzed. In order to ensure minimum switching frequency, an algorithm to choose the optimum zero space vector is proposed. The sequences are evaluated in terms of switching frequency, harmonic distortion, and current utilization. Simulated and experimental results on a 5 kVA CS inverter are presented. Additional studies include selection of the cycle period, minimization of uncharacteristic harmonics, and delay compensation [94-96].

Chapter 4 proposes a three-phase variable voltage and frequency voltage supply based on a CSI. A control strategy based on two loops is proposed. The inner loop makes the load voltage to track a given set of references with dynamic responses of the order of either the carrier or cycle period. The outer loop forces the CS inverter to operate at constant modulation index in steady state. This chapter also provides with the design

guidelines of all the filtering components and controller parameters. Simulated and experimental tests show the feasibility of the proposed strategy [97].

An improved CSI based ac induction machine drive is presented in Chapter 5. The scheme is based on a fully functional variable voltage/frequency power supply based on symmetrical CS topologies for both front-end and load converters. The control strategy is based on two control loops, the motor voltage and the CSI modulation index loops. The purpose is to preserve the inherent advantages of the CS topology (reliability, regeneration, and low *dv/dt*), as well as improve the overall efficiency through the internal dc link current control unlike standard CSI based drives. Experimental results on a 3 kVA laboratory unit are used to validate the proposed scheme [98-101].

Chapter 6 investigates a non-linear control technique based on state variable feedback linearization. The strategy is applied to a PWM-CS rectifier to obtain global linearization of the model, effective decoupling of the active (real) and reactive (imaginary) instantaneous powers, and elimination of the damping resistors. A systematic procedure to find the maximum and minimum setting points of the active and reactive powers is also included. Experimental results on a 2 kVA laboratory prototype are obtained. DSP hardware and software are used to simplify the realization of the proposed control strategy [102-103].

A dynamic analysis of a PWM-CS rectifier operating in regenerative mode is presented in Chapter 7. To avoid potential instability during the regeneration mode, a non-linear control strategy based on instantaneous load power feedforward is proposed. A systematic approach to controller design is also included. Simulated results on a 5 kVA

PWM rectifier are given [104].

APPENDIX A presents the set-ups used in the simulation and experimental verifications of the proposed modulating techniques and control schemes. APPENDIX B introduces a digital algorithm to reconstruct the ac line voltages in current source converters. The algorithm uses the dc link voltage and the gating signal information in order to reconstruct the ac voltages. This approach leads to a reduced number of voltage sensors. APPENDIX C provides with design guidelines for the passive components and controller parameters used in the simulation and experimental set-ups. Finally, APPENDIX D shows the induction machine small signal model in the *abc* frame used for dynamic analysis.

CHAPTER 2

ANALOG ON-LINE GATING PATTERN GENERATOR

2.1 INTRODUCTION

Current source converters are usually modulated using off-line pattern generators [12-17]. These generators obtain the gating signal, for instance, from EPROM memories. Storing units that have pre-loaded with all the possible sequences of the states of the switches and duration of them for one period of the line currents. This approach allows the optimization of the switching patterns to achieve high ac gain ($G_{ac} \approx 1$), low switching frequencies ($f_{sw} \approx 1/2 \cdot f_c$ of the equivalent carrier waveform), and low harmonic distortion. The ac (G_{ac}) and dc (G_{dc}) gains are defined by (2.1) and (2.2), respectively [4]. Also, it simplifies the compliance of the gating signals with the special requirements of forced commutated switches in CS converters (such as the shorting pulses to generate zero line currents).

As an alternative, and to overcome the gating difficulties, novel current-source power circuit topologies have been proposed for variable modulation index control, which consist in adding power switches to standard six-switch configuration [18-23]. In these modified configurations, it is possible to produce on-line the gating pulses for instantaneous line current control of CS converters. However, the addition of power switches reduces the overall system reliability, an important consideration in high power applications. In the on-line case, the gating signals are generated on a continuous basis as

function of the instantaneous value of a set of modulating signals and a carrier waveform.

$$G_{ac} = \begin{cases} \dfrac{\max\{\hat{i}_{r1}\}}{i_{dc}} & \text{in a CSR} \\ \dfrac{\max\{\hat{i}_{i1}\}}{i_{dc}} & \text{in a CSI} \end{cases} \tag{2.1}$$

where, $\hat{i}_{r1}$: peak of the fundamental component of the ac current in a CSR

$\hat{i}_{i1}$: peak of the fundamental component of the ac current in a CSI

i_{dc} : dc bus current

$$G_{dc} = \begin{cases} \dfrac{\max\{v_{r0}\}}{\hat{v}_r} & \text{in a CSR} \\ \dfrac{\max\{v_{i0}\}}{\hat{v}_i} & \text{in a CSI} \end{cases} \tag{2.2}$$

where, v_{r0} : dc component of the dc voltage in a CSR

$\hat{v}_r$: maximum amplitude of the dc voltage in a CSR

v_{i0} : dc component of the dc voltage in a CSI

$\hat{v}_i$: maximum amplitude of the dc voltage in a CSI

On-line PWM pattern generators nevertheless offer a number of control advantages over off-line optimized patterns: (a) faster dynamic response; (b) elimination of dc offsets under transient conditions; (c) continuous and precise control of the ac line current amplitude and phase. However, it has seldom been attempted for the six-switch CS configuration [24]. This chapter proposes a systematic analog approach to the on-line generation of gating patterns for such configurations. With such an approach, it is possible to extend the duality between VS and CS converters beyond the power circuit topology. In particular, all the carrier PWM techniques (such as sinusoidal, trapezoidal,

etc., ...) characterized by the possibility of on-line implementation and developed for VS converters can now be extended to CS rectifiers and inverters [4, 7-9]. Moreover, it is found that optimized gating patterns can also be obtained when non-standard modulating waveforms are used [25-27]. In fact, a gain equal to 1 and a switching frequency equal to 1/2 of the carrier waveform can easily be obtained.

2.2 PROPOSED ANALOG ON-LINE GATING PATTERN GENERATOR

The main purpose of a pattern generator is to produce gating signals, which applied to a CSC, generate line currents ($[i]_{abc}$) that track a given set of normalized references ($[i_n]_{abc}$, Fig. 2.1 (a)). The references are normally generated by an outer control loop (closed or open) according to a given static or dynamic objective. If the purpose of the pattern generator is attained, the converter becomes a current amplifier characterized by the following equation,

$$[i]_{abc} = G\,[i_n]_{abc}\,i_{dc} \quad \text{A} \tag{2.3}$$

where, G : gain that depends upon the modulating and carrier waveforms

$[i_n]_{abc}$: normalized current references

i_{dc} : dc bus current

Note that the line currents are PWM waveforms; however, the fundamental tracks the reference up to frequencies of about 1/2 the carrier waveform frequency. Also, the neutral is usually not connected; therefore, the line currents ($[i]_{abc}$) always add up to zero; therefore, the normalized line current references ($[i_n]_{abc}$) must also add up to zero.

2.2.1 CSC Gating Signals Constraints

In order to properly gate the power switches of a CSC, two main constraints must be meet at any time: (a) to properly define the load voltages at most one top (1, 3, or 5,) and one bottom switch (4, 6, or 2) should be closed at any time, and (b) the dc bus is of the current source type and thereby, it can not be opened; therefore, there must be at least one top (1, 3, or 5) and one bottom switch (4, 6, or 2) closed at all times (Fig. 1.2). Note that both constraints can be summarized by stating that at any time, only one top and one bottom switch must be closed.

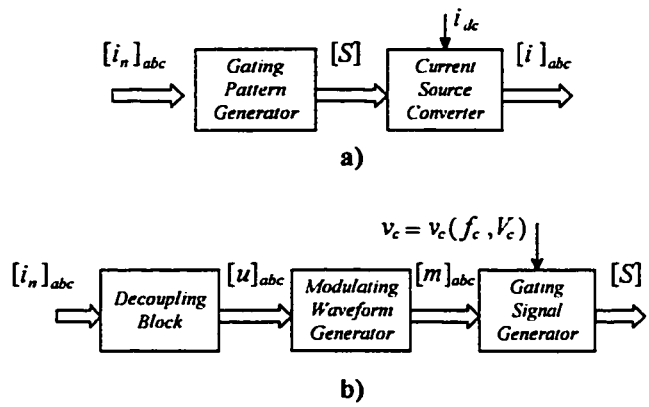

Fig. 2.1 Analog carrier-based on-line gating pattern generator scheme.

a) Generalized CSC and analog gating pattern generator schemes. **b)** Gating pattern generator stages.

2.2.2 Proposed Pattern Generator Circuit Realization

The proposed analog technique that permits on-line generation of gating patterns for a three-phase six-switch current-source configuration is implemented in the mixed analog/digital circuit given in Fig. 2.2. The circuit, as depicted in Fig. 2.1(b), is implemented in three stages: the *gating signal generator*, the *modulating waveform generator*, and the *decoupling block*.

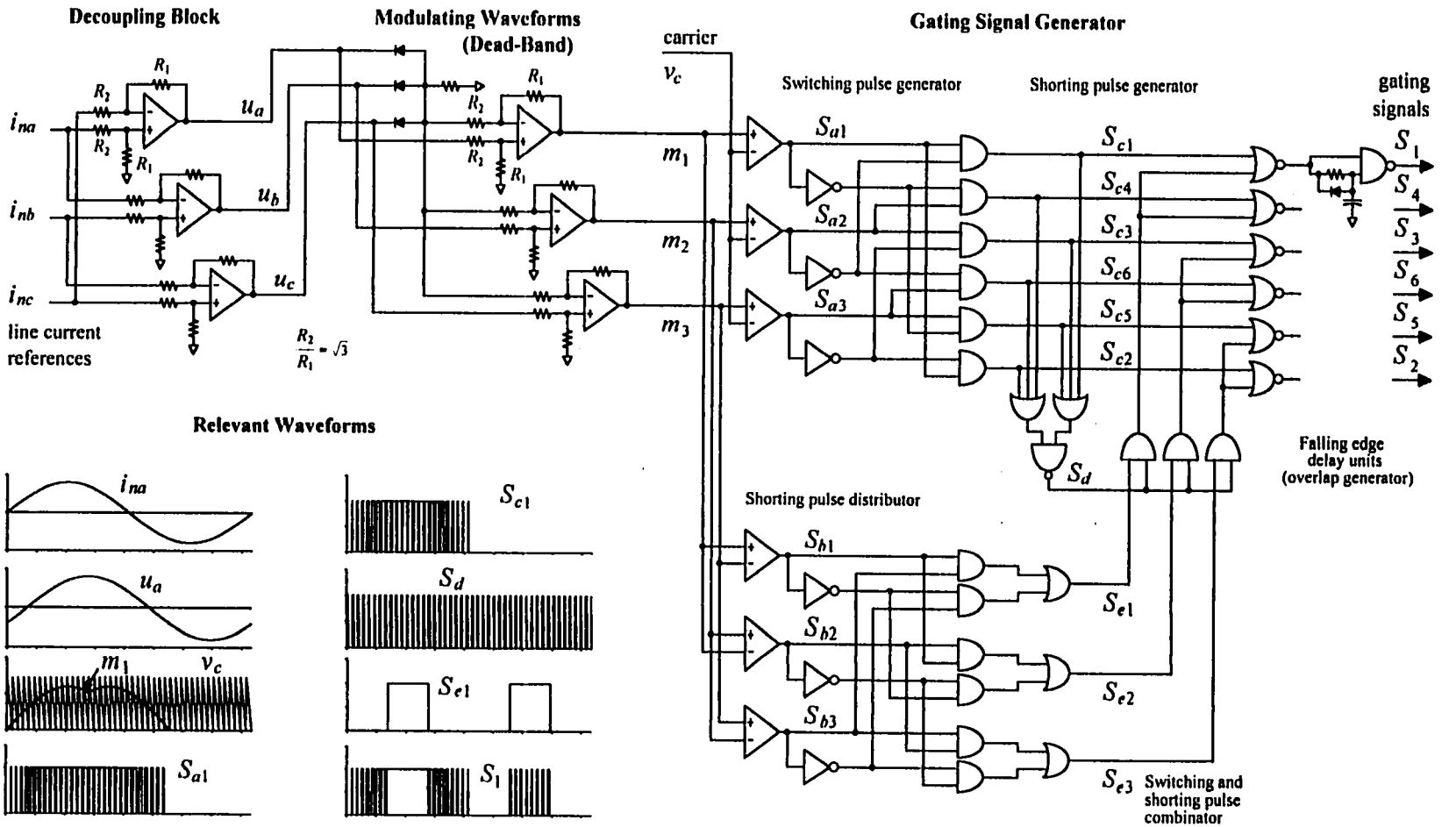

Fig. 2.2 Proposed analog on-line gating pattern circuit for CS converters.

A. The gating signal generator stage

This stage produces the gating signals ($[S] = [S_1 \ldots S_6]^T$) according to a carrier ($v_c = v_c(f_c, V_c)$) and three line-to-neutral modulating waveforms ($[m]_{abc} = [m_1 \ m_2 \ m_3]^T$). Therefore, any set of signals which, when combined, result in a sinusoidal line-to-line set of signals, will satisfy the requirement for a sinusoidal line current pattern. Examples of such modulating signals are the sinusoidal, sinusoidal with third harmonic injection [4], and dead-band [25] type of waveforms. Dead-band waveforms feature a band where no intersection between the carrier and the modulating signal is allowed, (i.e., m_1 in Fig. 2.2).

The first component of this stage (Fig. 2.2) is the *switching pulse generator*, where the signals S_{ai} ($i = 1, 2, 3$) are generated according to:

$$S_{ai} = \begin{cases} \text{HIGH} = 1 & \textit{if} \quad m_i > v_c \\ \text{LOW} = 0 & \textit{otherwise} \end{cases} \qquad i = 1, 2, 3 \qquad (2.4)$$

The outputs of the *switching pulse generator* are the signals S_{ci} ($i = 1,\ldots, 6$) which are basically the gating signals of the CSC without the shorting pulses. Table 2.1 shows the truth table of S_{ci} for all combinations of their inputs (S_{ai}, $i = 1, 2, 3$). It can be clearly seen that at most, one top and one bottom switch is ON. This satisfies the first constraint of CSC gating signals as stated before (Section 2.2.1). In order to satisfy the second constraint, the shorting pulse ($S_d = 1$) is generated (*shorting pulse generator*, Fig. 2.2) when none of the top switches ($S_{c1} = S_{c3} = S_{c5} = 0$) or none of the bottom switches ($S_{c4} = S_{c6} = S_{c2} = 0$) are gated. Then, this pulse is added (using OR gates) to only one leg of the CSC (either to the switches 1 and 4, 3 and 6, or 5 and 2) by means of the *switching and shorting pulse combinator* (Fig. 2.2). The signals S_{ei} ($i = 1, 2, 3$) ensure that (a) only

one leg of the CSC is shorted, since only one of the signals is HIGH at any time, and (b) an even distribution of the shorting pulse, since S_{ei} (i = 1, 2, 3) is high for 120° in each period (under balanced conditions). This ensures that the rms currents are equal in all the legs of the converter.

Finally, overlaps (< 5 μs for BJTs) are added as a final stage (*falling edge units*) to ensure proper commutation of the dc bus current among the top and bottom power switches. This overlap also provides a minimum on-time for the switches.

Table 2.1 Truth table for the *Switching Pulse Generator* stage.

			Top Switches			Bottom Switches		
S_{a1}	S_{a2}	S_{a3}	S_{c1}	S_{c3}	S_{c5}	S_{c4}	S_{c6}	S_{c2}
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0
0	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1	0
1	1	0	0	1	0	0	0	1
1	1	1	0	0	0	0	0	0

B. The modulating waveform generator stage

This stage generates the modulating signals ($[m]_{abc}$) out of the voltage signals ($[u]_{abc}$). In this thesis, a modified dead-band PWM technique is proposed, which unlike the regular dead-band technique proposed for VS inverters [25], uses a saw-tooth carrier instead of the standard triangular carrier. Fig. 2.2 shows one alternative to the generation of the dead-band modulating signals. Note that only this stage should be modified

according to the alternative modulating waveforms. For instance, for sinusoidal modulating waveforms, this stage could be replaced by voltage followers.

It has been shown that the line currents ($[i]_{abc}$) generated by the CSC and the phase waveforms ($[u]_{abc}$) are related by the following expression [24],

$$[i]_{abc} = \frac{G_{ac}}{\sqrt{3}V_c}[T][u]_{abc}\, i_{dc} \quad \text{A} \tag{2.5}$$

where, G_{ac} : ac gain of the PWM technique (e.g. $G_{ac} = 0.866$ for SPWM [4])

V_c : amplitude of the carrier waveform (Fig. 2.2)

$$[T] = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

Since $[T]$ in (2.5) is not diagonal, the line currents are coupled with respect to $[u]_{abc}$, this comes from the fact that each line current is generated from line-to-neutral signals. This feature is particularly undesirable when it comes to designing an external loop to generate the line current references. Therefore, a decoupling block is used to overcome this drawback.

C. The decoupling block stage

The decoupling block can be modeled as a linear transformation given by, $[u]_{abc} = [D]\cdot[i_n]_{abc}$ (where, $[D]$ is the decoupling matrix to be found, Fig. 2.1 (b)). Therefore,

$$[i]_{abc} = \frac{G_{ac}}{\sqrt{3}V_c}[T][D][i_n]_{abc}\, i_{dc} \quad \text{A} \tag{2.6}$$

If $[D]$ is chosen to be equal to $[T]^T$ and noting that $i_{na} + i_{nb} + i_{nc} = 0$, (2.6) yields,

$$[i]_{abc} = \frac{G_{ac}}{V_c}[i_{ref}]_{abc}\, i_{dc} \quad \text{A} \tag{2.7}$$

Eqn. (2.7) shows that the line currents can track the normalized references in a linear and decoupled fashion. An alternative to implement the *decoupling block* is given in Fig. 2.2. Additional features of the overall circuit over previous realizations are: (a) the *decoupling* and *gating signal generator* stages are general approaches and thereby, they can be used with any on-line carrier-based PWM technique, (b) the carrier waveform can be free-running, and (c) the circuit uses only binary logic to operate, which simplifies its design. Also, the proposed circuit realization (Fig. 2.2) can be used equally in CS Rectifiers and CS Inverters. In rectifiers, the current references must be synchronized with the ac mains.

2.3 SIMULATED AND EXPERIMENTAL RESULTS

To test the proposed circuit, a variety of standard modulating and carrier waveforms are used to generate the gating signals (such as sinusoidal modulating and triangular carrier waveforms). Since the proposed circuit is valid for any carrier-based PWM technique, some improved modulating and carrier waveforms which were initially developed for VS topologies are extended to CS topologies (such as dead-band modulating and triangular carrier waveforms). The simulated patterns are evaluated according to their switching frequency, ac and dc gain, harmonic spectrum, and harmonic distortion.

2.3.1 Modulating Techniques Performance Evaluation

Fig. 2.3 shows the simulated ac/dc waveforms of a CSC modulated by the modified dead-band technique. Table 2.2 summarizes a comparison of various analog

carrier-based PWM techniques implemented by using the proposed circuit. It is found that the proposed modified dead-band technique presents the lowest switching frequency and high ac gain.

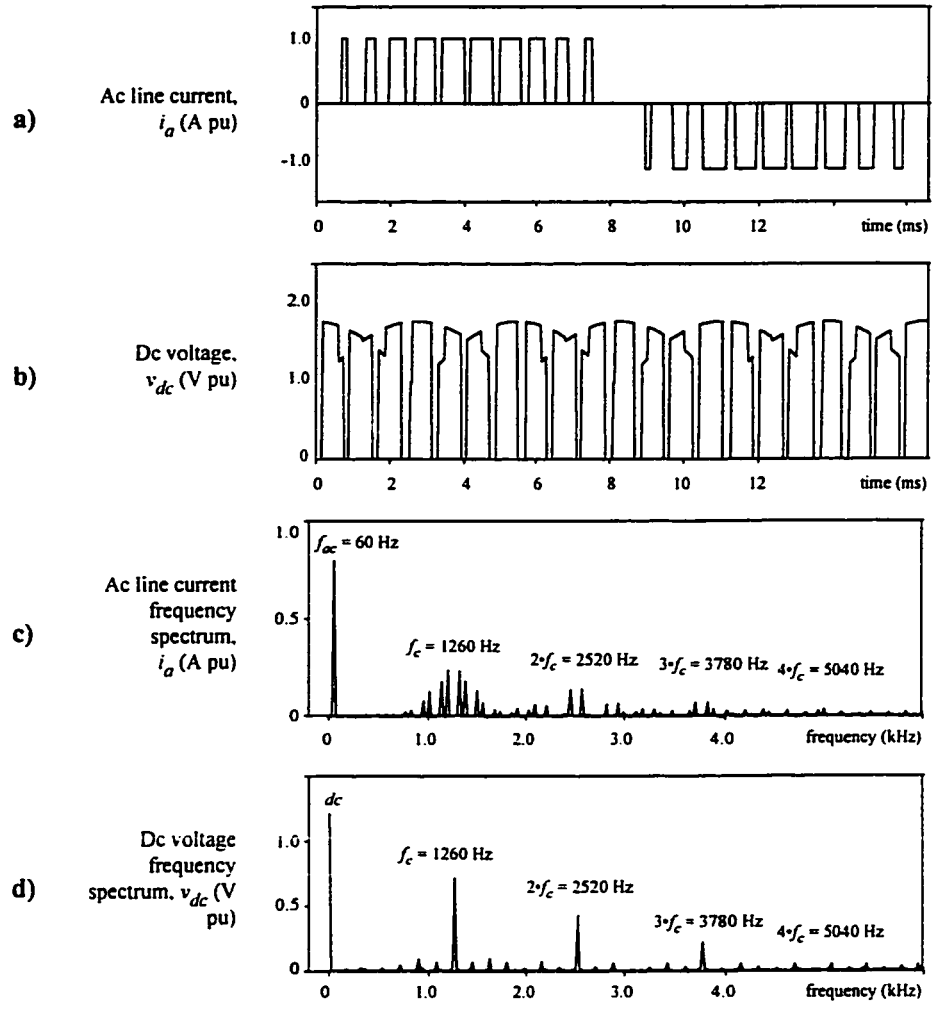

Fig. 2.3 Simulated CS converter ac/dc waveforms.

Modified dead-band technique, modulation index (m) = 0.8 pu; carrier frequency, f_c = 1260 Hz = 21 pu. **a)** Ac line current (i_a). **b)** Dc voltage (v_{dc}). **c)** Ac line current spectrum (i_a). **d)** Dc voltage spectrum (v_{dc}).

The ac and dc waveform harmonic spectra are evaluated using several harmonic distortion indexes. These are the distortion factors DF_1 (ac distortion factor for second-

order filtering), DF_2 (ac distortion factor for first-order filtering), and DF_3 (dc distortion factor for first-order filtering), that are defined by,

Table 2.2 Comparison of Analog Gating Patterns for CS Converters.

PWM Technique	switching freq. (f_{sw})	ac gain (G_{ac}) [4]	dc gain (G_{dc}) [4]
Sinusoidal PWM	f_c	0.866	0.750
Third Harmonic Injection	f_c	1.000	0.866
Trapezoidal PWM	f_c	1.053	0.911
Dead-Band PWM	$2/3 \cdot f_c - 1$	1.000	0.866
Modified Dead Band (Fig. 2.2)	$1/2 \cdot (f_c + 1)$	1.000	0.866

$$DF_1 = \frac{100}{h(1)}\sqrt{\sum_{n=2}^{\infty}\left(\frac{h(n)}{n^2}\right)^2} \quad \% \tag{2.8}$$

$$DF_2 = \frac{100}{h(1)}\sqrt{\sum_{n=2}^{\infty}\left(\frac{h(n)}{n}\right)^2} \quad \% \tag{2.9}$$

$$DF_3 = \frac{100}{h(0)}\sqrt{\sum_{n=1}^{\infty}\left(\frac{h(n)}{n}\right)^2} \quad \% \tag{2.10}$$

where, $h(n)$ is the rms value of the n^{th} harmonic.

Fig. 2.4 shows the variation of the distortion factors as a function of the modulation index (m) for some typical and the proposed PWM technique. Although it is given for one constant switching frequency (f_{sw} = 21 pu), their shape and relative position are independent of switching frequency [4]. In general, it is found that the proposed modified dead-band technique offers the lowest harmonic distortion.

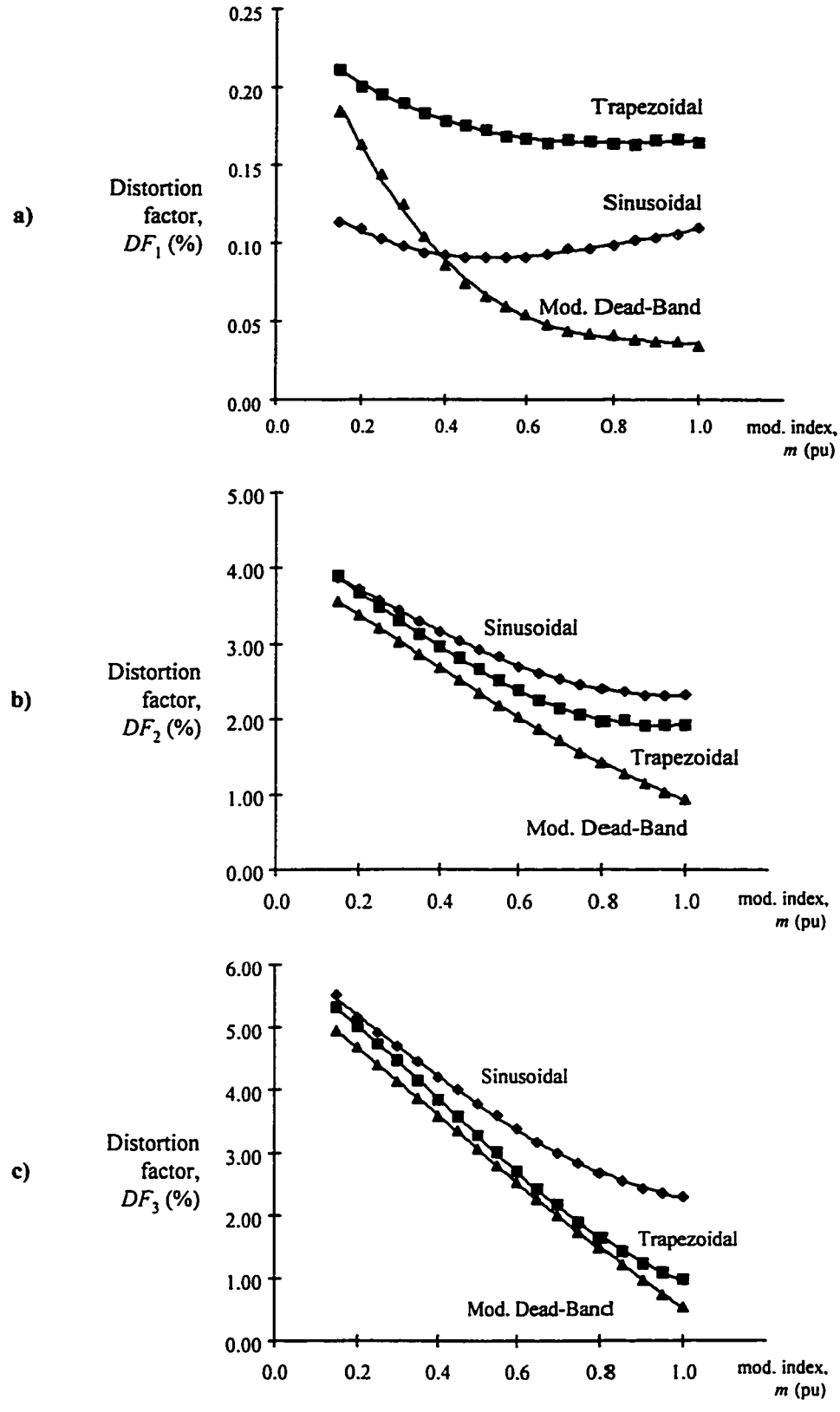

Fig. 2.4 Harmonic distortion factors for different carrier-based techniques.

Switching frequency, f_{sw} = 1260 Hz = 21 pu. **a)** DF_1 %. **b)** DF_2 %. **c)** DF_3 %.

2.3.2 Experimental Evaluation

The proposed gating pattern generator circuit (Fig. 2.2) is used to modulate a current source rectifier (APPENDIX A.1). In this case the line currents are synchronized with the ac mains by using the ac capacitor waveforms as normalized line current references. Fig. 2.5 shows the experimental waveforms for the proposed modified dead-band modulating technique. APPENDIX A.1 presents the set-up and test conditions.

2.3.3 Proposed Pattern Generator Under Overmodulation

Overmodulation in PWM current source converters is a transient condition that is mainly caused by the outer control loop. Under overmodulation, the modulating waveforms are higher than the carrier waveform ($m_k > V_c$, $k = 1$, 2, or 3 in Fig. 2.2). Fig. 2.6 shows the modulating waveforms and gating signals from $m = 0.8$ to overmodulation, $m = 2$. It is found that under overmodulation the proposed circuit satisfies naturally the gating signal requirements (Section 2.2.1). Moreover, under complete overmodulation, the circuit provides gating signals equivalent to six-step operation, which provides maximum voltage converter utilization.

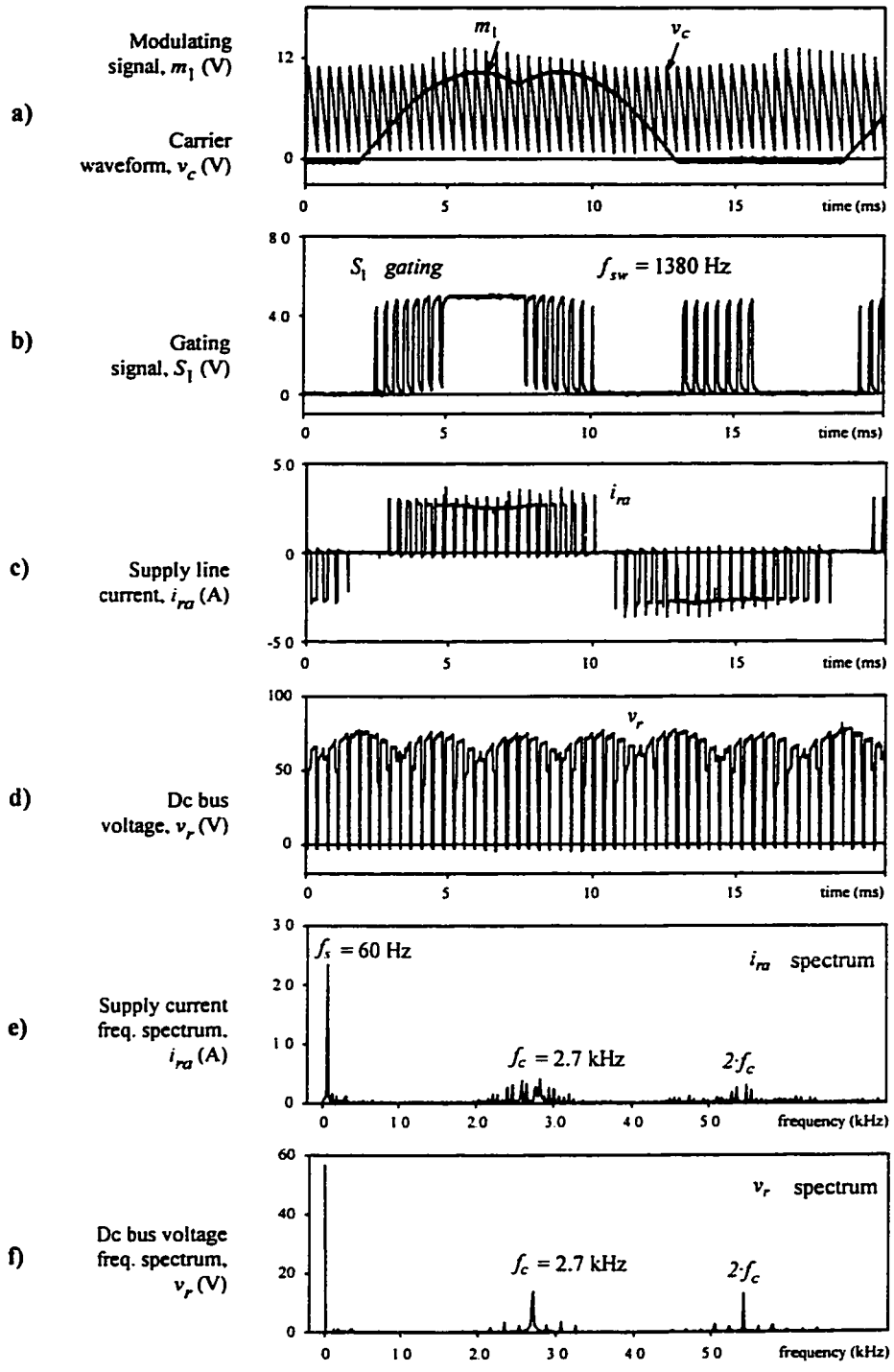

Fig. 2.5 Experimental results for the modified dead-band PWM scheme.

$m = 0.8, f_{sw} = 23$ pu = 1380 Hz, $f_c = 45$ pu = 2.7 kHz). **(a)** Modulating signal (m_1) and carrier waveform (v_c). **(b)** Gating signal for switch 1 (S_1). **(c)** Rectifier input current (i_{ra}). **(d)** Rectifier dc bus voltage (v_r). **(e)** Rectifier input current spectrum (i_{ra}). **(f)** Rectifier dc bus voltage spectrum (v_r).

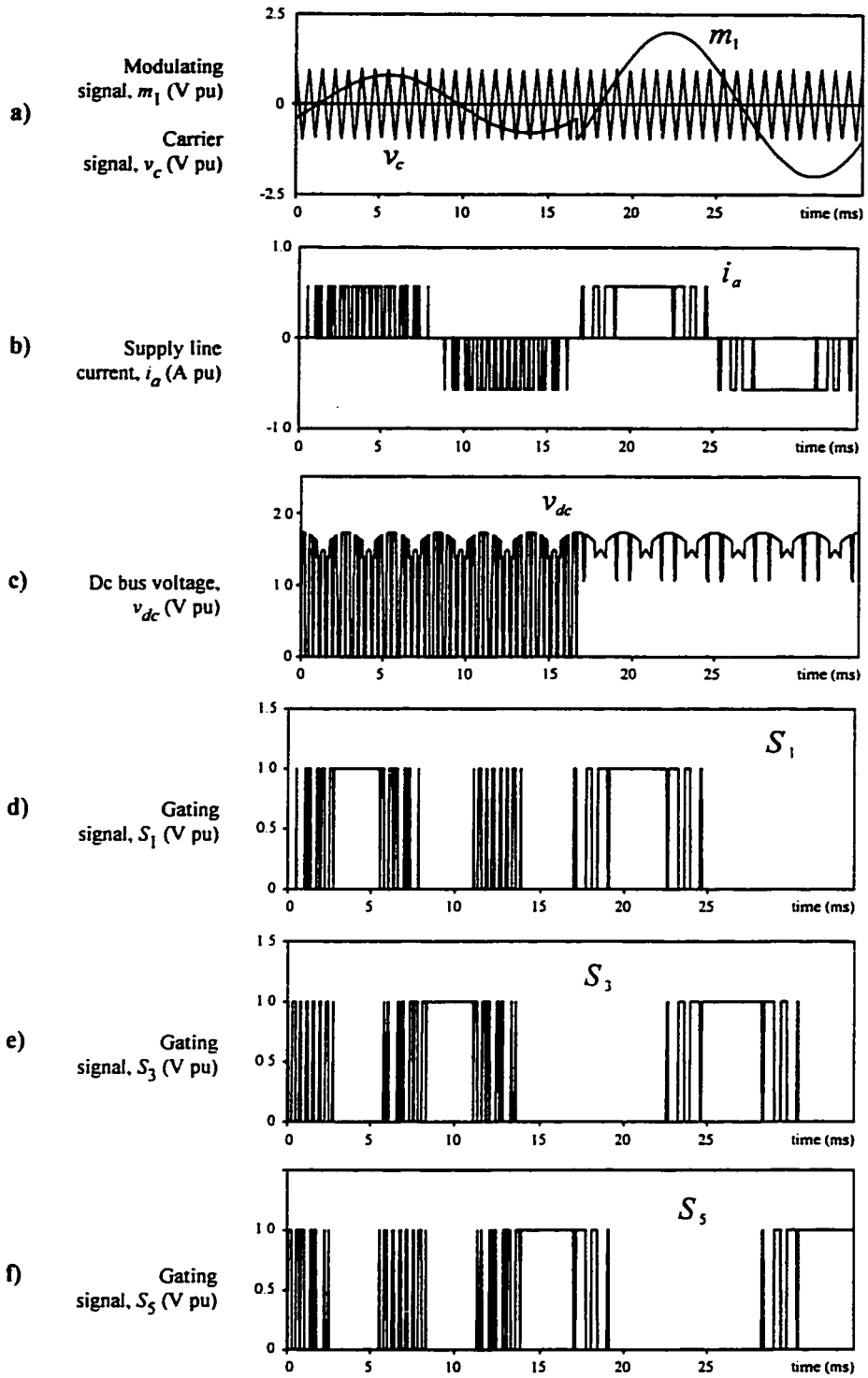

Fig. 2.6 Gating signals under overmodulation for the proposed circuit.

SPWM technique, $m = 0.8$ to $m = 2.0, f_c = 21$ pu = 1.26 kHz). **a)** Modulating signal (m_1) and carrier signal (v_c). **b)** Ac line current (i_a). **c)** Dc bus voltage (v_{dc}). **d)** Gating signal for switch 1 (S_1). **e)** Gating signal for switch 3 (S_3). **f)** Gating signal for switch 5 (S_5).

2.4 DISCUSSION AND CONCLUSIONS

A fully functional circuit implementation of an analog on-line gating pattern generator for three-phase six-switch current-source converter topologies has been proposed. Results show that: (a) the generation of appropriate gating patterns can be carried out on-line, (b) standard PWM techniques (sinusoidal, harmonic injection, trapezoidal, etc.) can be implemented and there is no penalty with respect to the ac/dc gains and harmonic quality, (c) enhanced modulating techniques, initially developed for VS topologies, can be extended to CS topologies, and (d) a proposed dead-band PWM technique has shown that the effective switching frequency can be reduced to one half of the carrier frequency, while keeping the high ac gain and lowest harmonic distortion.

The circuit also features over previous realizations the following improvements: (a) application, without major modifications, in any PWM carrier-based scheme, (b) operation with a free-running carrier waveform; however, optimum results are obtained if its frequency is an odd integer number multiple of 3 and it is synchronized with the line current reference, (c) only binary logic is required; thereby, its implementation is very simple, and (d) proper operation under transient and/or sustained overmodulation.

Thus, the proposed analog on-line pattern generator extends the duality between VS and CS converters beyond the power circuit topology. Enhanced control strategies can therefore be implemented. Specifically, Chapter 4 of this proposal shows a general purpose three-phase voltage supply based on a voltage-controlled CSI and Chapter 5 a high performance ac induction motor drive.

CHAPTER 3

DIGITAL ON-LINE GATING PATTERN REALIZATION

3.1 INTRODUCTION

Analog control of PWM converters can be readily implemented using analog on-line gating pattern generators (Chapter 2). Carrier based modulation techniques are the straight forward application for such strategies. However, there is an increasing number of digital control strategies that require a digital on-line gating pattern generator [29-30]. These emerging techniques are gaining popularity due to the development of more complex power topologies, such as three-phase converters, power factor correction units, active filters, etc., and the availability of fast and inexpensive digital signal processors (DSP), A/D and D/A converters, and other digital components.

Since its introduction [31-32], digital control methods based on Space Vectors (SV) are widely used [33-35]. Its main advantages include: (a) direct implementation of enhanced control strategies (in the rotating *dq* and stationary $\alpha\beta$ frames) and (b) straight forward implementation in digital systems (DSPs). Some studies have addressed crucial issues such as optimum switching sequence [36-39], operation under overmodulation [40-41], operation under unbalanced conditions [43], and minimization of uncharacteristic harmonics [44]. Although most of these techniques were initially developed for VS topologies, the introduction of space vector to CS converters has also been successful [45]. However, in the case of CS circuits, studies related to switching sequence, minimum

switching frequency, and uncharacteristic harmonics have seldom been attempted [46].

In this chapter, digital pattern generators for CS converters that are based on the space vector technique are investigated. Specifically, three sequences are analyzed and an algorithm to select the zero space vector is proposed. The resulting patterns feature reduced switching frequency (f_{sw}) while keeping a low harmonic distortion. Thus, minimum switching losses is assured.

3.2 PROPOSED DIGITAL GATING PATTERN REALIZATION

The instantaneous selection of the gating pattern, for a given line current reference, is done by a digital algorithm. The CS converter line current reference and gating pattern options are represented by Space Vectors. Thus, specific requirements of CS topology are readily incorporated in the pattern generation algorithm.

The overall performance of the SV-based techniques depend upon the use of the three degrees of freedoms available when implementing the SVM. These are: (a) sequence applied to the selected SV's, (b) selection of the zero SV, and (c) normalized cycle frequency (f_{cycle}: space vector sample frequency). In this chapter, three different sequences are studied, the selection of the zero SV is analyzed, and the influence of the normalized cycle frequency is established.

3.2.1 The Space Vector Transformation

The space vector is a complex number that can be associated to any three quantities of time (not necessarily sinusoidal) which add up to zero. For instance, the space vector associated with the ac line currents of a three-phase CS converter is given

by:

$$\mathrm{I} = \frac{2}{3}(i_a + i_b \cdot e^{\mathrm{j}\phi} + i_c \cdot e^{-\mathrm{j}\phi}) = \mathrm{I}_{\Re} + \mathrm{jI}_{\Im} \quad \mathrm{A} \tag{3.1}$$

where, $\phi = 2\pi/3$; and i_a, i_b, and i_c are the line current components.

A. Space Vectors of a CS Converter

Unlike a three-phase VS, a three-phase CS converter has nine valid switch combinations that are named *states*. Each state produces a specific set of ac line currents and thereby, a specific space vector can be associated to each one by using (3.1). Table 3.1 shows the different space vectors (I_k) associated with the nine states of a CS circuit. These are calculated using (3.1) and the states defined in Fig. 1.2.

B. Space Vector of the Line Current Reference

Like the nine states of a CS topology, the instantaneous ac line current reference ($[i_n]_{abc} = [i_{na}\ i_{nb}\ i_{nc}]^T$) can be represented by an equivalent space vector (I_n). Noting that this vector has a length proportional to the converter (rectifier or inverter) modulation index

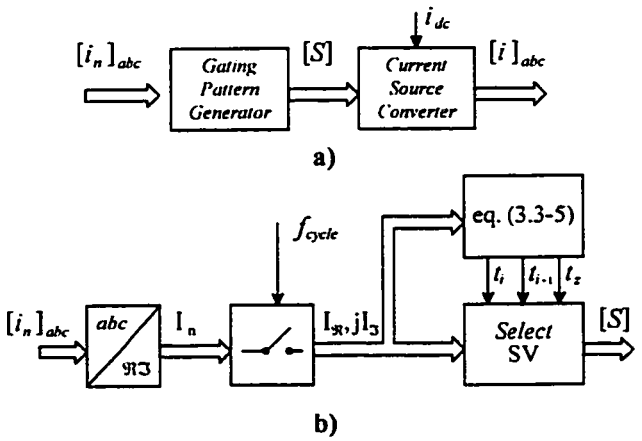

Fig. 3.1 Digital space vector-based on-line gating pattern generator scheme.

a) Generalized CSC and digital gating pattern generator schemes. **b)** Gating pattern generator stages.

(m) and a constant rotating angular frequency equal to ω for sinusoidal references. The CS converter space vectors (I_k, k =1,..., 9) and the line current reference (I_n) space vector are represented in a complex plane (Fig. 3.2).

Table 3.1 Space vectors of a three-phase six-switch CS topology.

State (k)	on Switches	i_a/i_{dc}	i_b/i_{dc}	i_c/i_{dc}	I_k/i_{dc}
1	1, 2	1	0	-1	1 + j 0.577
2	2, 3	0	1	-1	j 1.545
3	3, 4	-1	1	0	-1 + j 0.577
4	4, 5	-1	0	1	-1 - j 0.577
5	5, 6	0	-1	1	- j 1.545
6	6, 1	1	-1	0	1 - j 0.577
7	1, 4	0	0	0	0
8	3, 6	0	0	0	0
9	5, 2	0	0	0	0

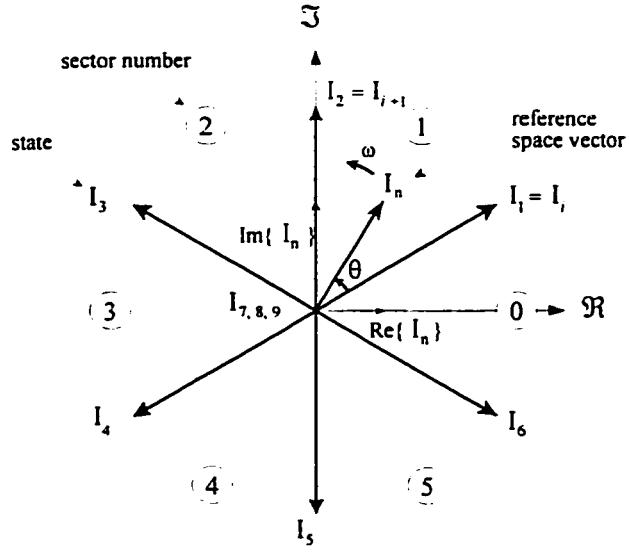

Fig. 3.2 CS converter and reference space vectors.

3.2.2 Space Vector Modulation (SVM)

The objective of the SVM technique is to approximate the current reference space vector (I_n) with the nine CS converter space vectors (I_k, k =1,..., 9). However, it has been reported that by approximating the reference space vector by only the nearest two non-zero (I_i and I_{i+1}) and only one of the three zero space vectors ($I_z = I_7$, I_8, or I_9, Fig. 3.2), the gain of the technique is maximized [36] and the switching frequency minimized. Thus, if the reference (I_n) is laying between the arbitrary vectors I_i and I_{i+1} (Fig. 3.2) the following expression can be derived,

$$I_n \cdot t_{cycle} = I_i \cdot t_i + I_{i+1} \cdot t_{i+1} + I_z \cdot t_z \quad \text{A·s} \tag{3.2}$$

where, t_i, t_{i+1}, t_z for $m \leq 1$ are given by,

$$t_i = t_{cycle} \cdot m \cdot \sin(\pi/3 - \theta) \quad \text{s} \tag{3.3}$$

$$t_{i+1} = t_{cycle} \cdot m \cdot \sin(\theta) \quad \text{s} \tag{3.4}$$

$$t_z = t_7 + t_8 + t_9 = t_{cycle} - t_i - t_{i+1} \quad \text{s} \tag{3.5}$$

where, t_{cycle} is the space vector interval, and $m = \| I_n \| / i_{dc}$.

A. SV Sequences

The SVM technique selects the vectors to be used and their respective on-times. However, the sequence in which they are used to gate the converter remains undetermined. In this Section, three sequences are studied (Seq_A, Seq_B, and Seq_C, Fig. 3.3) and their performance evaluated (Section 3.3) using three harmonic distortion factors (Section 2.3.1). Note that the evaluation can be done regardless of the selection of the zero SV due to the fact that the line current waveshape does not depend upon the selected

zero vector (I_7, I_8, or I_9, Table 3.1).

B. The Zero SV Selection

For a given SV sequence the selection of the zero SV defines the switching frequency [37]. In steady state, the normalized line current references are usually sinusoidal signals. Therefore, the line current SV reference (I_n) should describe a circular trajectory with constant angular speed (ω, Fig. 3.2). Thus, transitions only between adjacent SV's are expected.

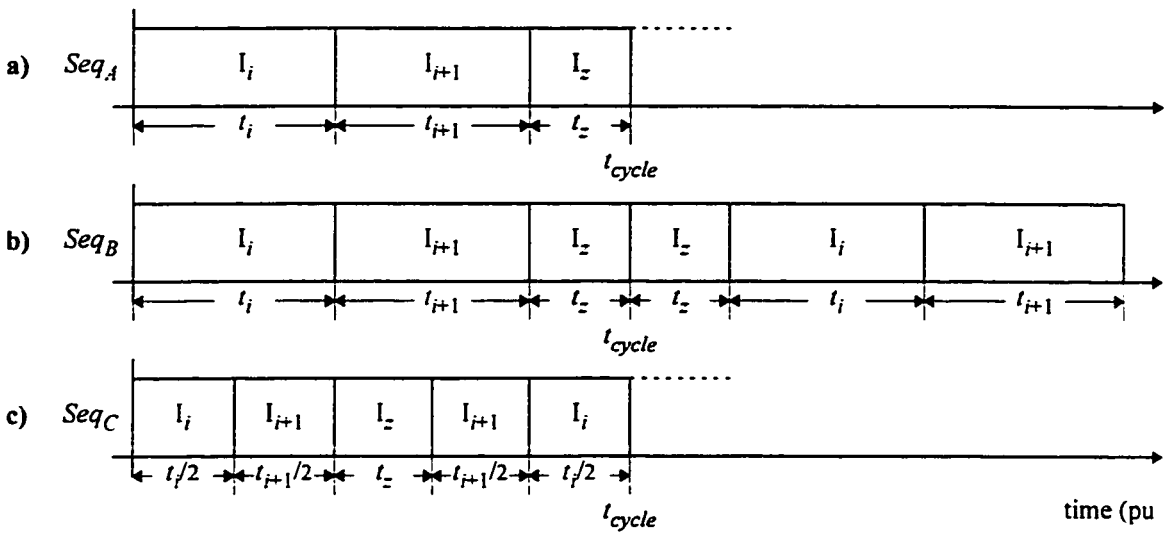

Fig. 3.3 CS converter SVM outstanding sequences.

a) Seq_A. b) Seq_B. c) Seq_C.

To illustrate the effect of the zero SV selection, Fig. 3.4 shows all possible transitions in Sector ① including the number of switch commutations from one state to another (the number on the branches). Specifically, Fig. 3.4(a) shows the transition from I_1 to I_2 or I_2 to I_1 (which is possible in all sequences), Fig. 3.4(b) from I_1 to I_1 (which is

possible in Seq_C), and Fig. 3.4(c) from I_2 to I_2 (which is possible in Seq_C). For instance, let's assume that the initial state is I_1, the final is I_2, and a zero SV is required in between. Fig. 3.4(a) shows that: if either I_7 or I_8 is used, a total of 3 commutations are required; however, if I_9 is used, only 2 commutations are required.

Fig. 3.4 shows that, for the proposed sequences, I_9 is the zero SV in Sector ① which provides the lowest switching frequency regardless of the initial and final state. As a generalization, Table 3.2 shows the zero vector (I_z) to be used in each sector in order to minimize the switching frequency.

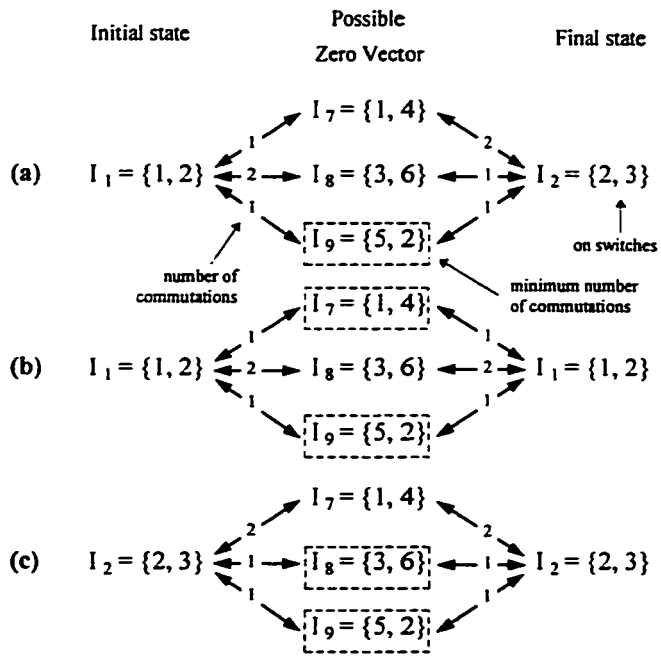

Fig. 3.4 Possible state transitions in Sector ① involving a zero SV.

a) Transition: $I_1 \Leftrightarrow I_z \Leftrightarrow I_2$ or $I_2 \Leftrightarrow I_z \Leftrightarrow I_1$, **b)** Transition: $I_1 \Leftrightarrow I_z \Leftrightarrow I_1$, **c)** Transition: $I_2 \Leftrightarrow I_z \Leftrightarrow I_2$.

Table 3.2 Zero SV for Minimum Switching Freq.

Sector	I_i	I_{i+1}	I_z
⓪	I_6	I_1	I_7
①	I_1	I_2	I_9
②	I_2	I_3	I_8
③	I_3	I_4	I_7
④	I_4	I_5	I_9
⑤	I_5	I_6	I_8

C. Normalized cycle frequency selection

The normalized carrier frequency in three-phase carrier-based PWM techniques is chosen to be an odd integer number multiple of 3 ($f_c = 3 \cdot k$, $k = 1, 3, 5,...$). Thus, it is possible to minimize parasitic or non-intrinsic harmonics in the PWM waveforms. A similar approach can be used in the SVM technique to minimize uncharacteristic harmonics. Hence, it is found that for the sequences Seq_A and Seq_C, the normalized cycle frequency (f_{cycle}) should be an integer multiple of 6, and 12 for the sequence Seq_B. This is due to the fact that in order to produce symmetrical line currents, all the sectors, a total of 6, should be equally used in one period. As an example, Fig. 3.5 shows the line current spectra for two values of f_{cycle} when employing the sequence Seq_A. It can be clearly seen that for $f_{cycle} = 45$ pu (Fig. 3.5(a)) additional harmonics are present (the dark areas on the plot), which are not present when $f_{cycle} = 42$ pu (multiple of 6, Fig. 3.5(b)).

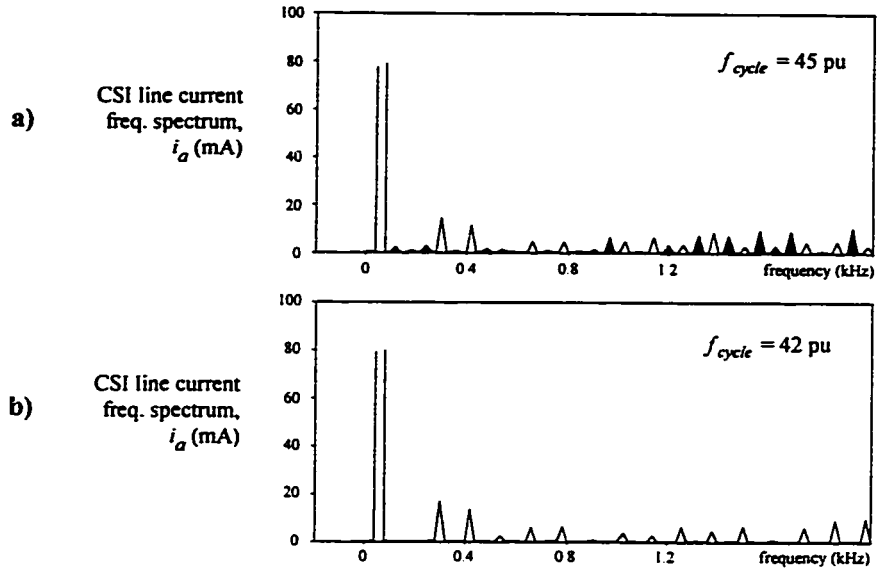

Fig. 3.5 Ac line current spectra for two normalized cycle frequencies.

$m = 0.8, f_{base} = 60$ Hz. **a)** $f_{cycle} = 45$ pu, **b)** $f_{cycle} = 42$ pu (multiple of 6).

3.3 SIMULATED AND EXPERIMENTAL RESULTS

The sequences Seq_A, Seq_B, and Seq_C are implemented on a TMS320C30 microprocessor based DSP board and used to modulate a CS inverter (APPENDIX A.2). The algorithm employs the zero SV for minimum switching frequency given in Table 3.2. Key experimental waveforms are depicted in Fig. 3.6 for Seq_A. APPENDIX A.2 shows the set-up and parameter values used in the implementation.

Table 3.3 summarizes a comparison of the SV-based modulating technique for the different sequences presented earlier in Section 3.2.2.A. The algorithms use the zero space vector given in Table 3.2. It can be observed that all the techniques present (a) high ac-dc gains ($G_{ac} = 1$, $G_{dc} = 0.866$) for unity modulation index and (b) switching frequencies at most one half of the cycle frequency ($f_{sw} \leq f_{cycle} / 2$) for modulation indexes lower than unity.

Their harmonic spectra are also evaluated using the distortion factor defined in Section 2.3.1 (DF_1, DF_2, and DF_3). Fig. 3.7 shows the distortion factors as a function of the modulation index for $m \leq 1$ and a fixed cycle frequency (f_{cycle} = 2520 Hz = 42 pu). From Fig. 3.7, it is noticed that the techniques based on sequences *A* and *B* present the lowest distortion for modulation indexes higher than 0.7.

Table 3.3 Comparison of Digital Gating Patterns for CS Converters.

Sequence (Fig. 3.3)	switching freq, f_{sw}	ac gain (G_{ac}) [4]	dc gain (G_{dc}) [4]
Seq_A	$3 \cdot (f_{cycle} / 6)$	1.000	0.866
Seq_B	$3 \cdot (f_{cycle} / 6) - 1$	1.000	0.866
Seq_C	$5 \cdot (f_{cycle} / 12) - 1$	1.000	0.866

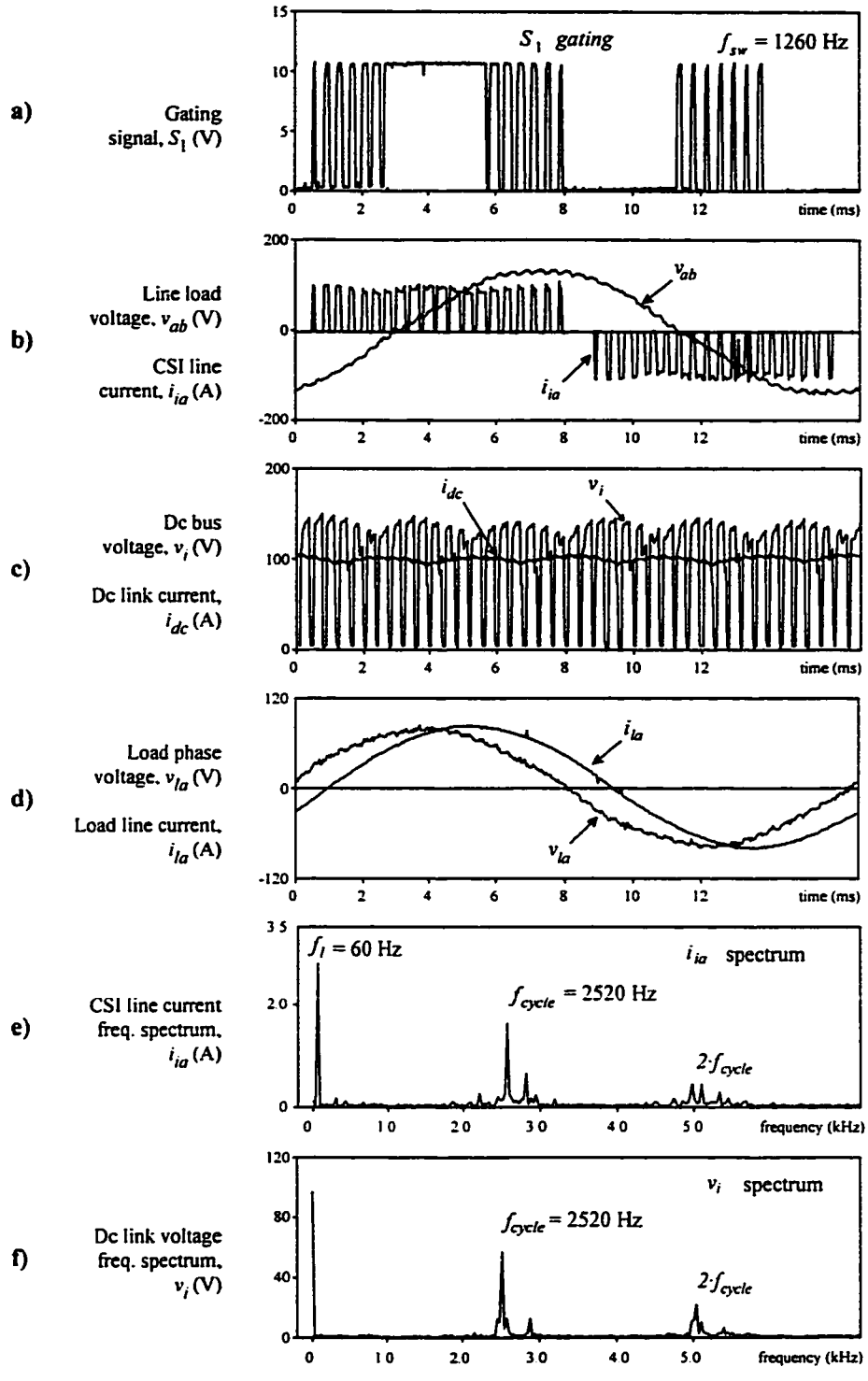

Fig. 3.6 Experimental results for the SV-based PWM based scheme.

$m = 0.8, f_{sw} = 21$ pu = 1260 Hz, $f_{cycle} = 2520$ Hz, Seq_A - Fig. 3.3. a) Gating signal for switch 1 (S_1). (b) CSI line current ($15 \cdot i_{ia}$) and line load voltage (v_{ab}). (c) Dc bus voltage (v_i) and current ($15 \cdot i_{dc}$). (d) Load phase current ($15 \cdot i_{la}$) and phase voltage (v_{la}). (e) CSI line current frequency spectrum (i_{la}). (f) Dc bus voltage frequency spectrum (v_i).

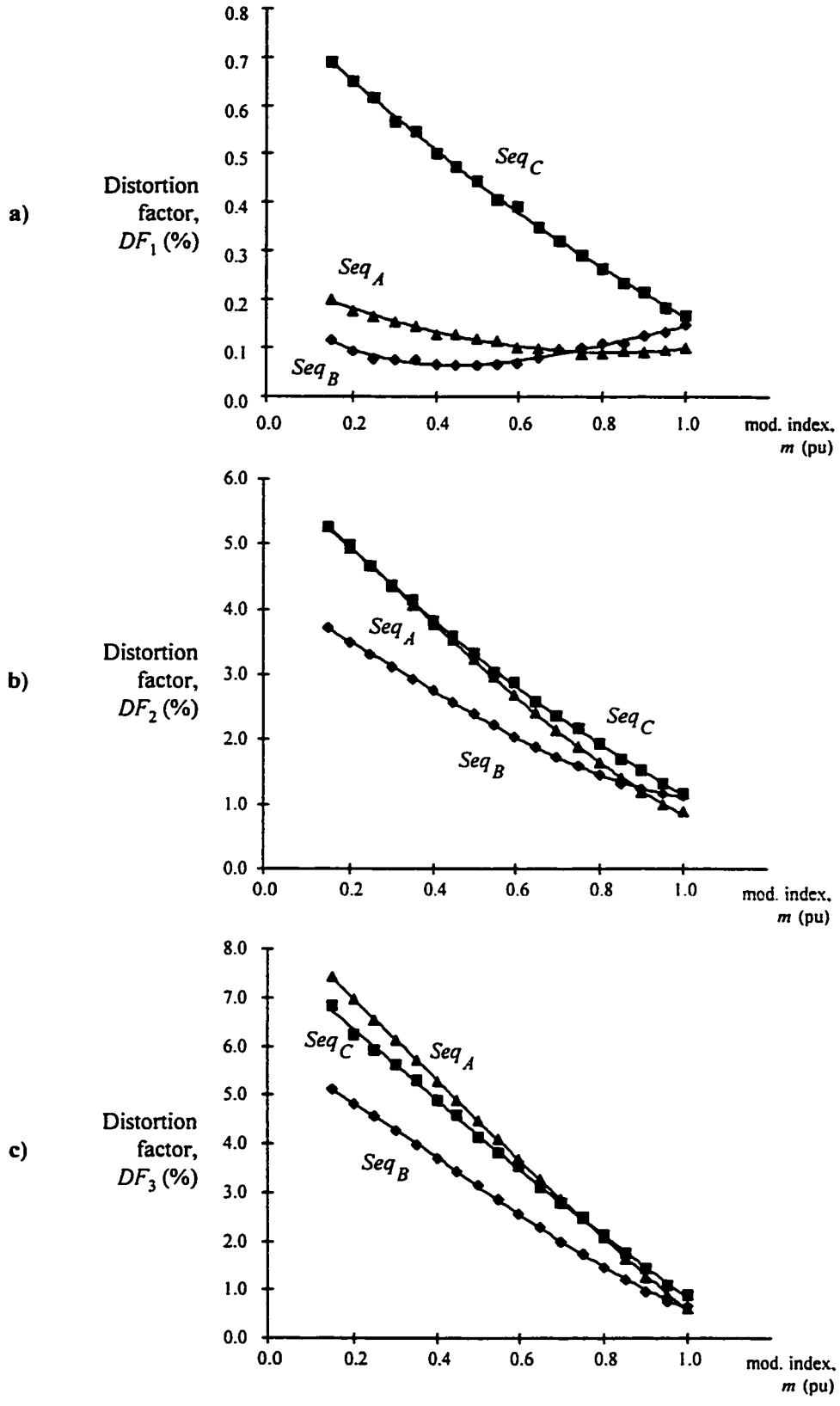

Fig. 3.7 Harmonic distortion factors for different SVM sequences.

Cycle frequency, f_{cycle} = 2520 Hz = 42 pu. **a)** DF_1 %. **b)** DF_2 %. **c)** DF_3 %.

3.4 DISCUSSION AND CONCLUSIONS

The space vector PWM technique, which has been already implemented in VS topologies, has been used to modulate three-phase current-source converters. The space vector modulation technique is a digital approach that can be implemented on-line in DSP systems to assemble modern control strategies. The technique requires the selection of the sequence of non-zero space vectors, the zero space vector, and the appropriate normalized cycle frequency.

Results show that: (a) the sequence of non-zero space vectors defines the harmonic distortion of the PWM waveforms, (b) the selection of the zero space vectors defines the resulting switching frequency, and (c) the appropriate selection of the normalized cycle frequency minimizes the uncharacteristic harmonics in the PWM waveforms.

In this chapter, three sequences, the optimum selection of the zero space vector and normalized cycle frequency are presented. The resulting algorithms offer the following improved advantages: (a) low harmonic distortion (< 0.2%) for modulation indexes lower than unity, (b) high ac-dc gains ($G_{ac} = 1$, $G_{dc} = 0.866$) for unity modulation index, and (c) switching frequencies at most one half of the cycle frequency ($f_{sw} \leq f_{cycle} / 2$) for modulation indexes lower than unity.

The algorithms are used to accomplish refined control schemes. Specifically, Chapter 6 shows a CSR operating under state variable decoupling and independent power flow control, and Chapter 7 a CSR operating in regenerative mode.

CHAPTER 4

AN INTEGRATED THREE-PHASE VC-CSI VOLTAGE SUPPLY

4.1 INTRODUCTION

The most commercial general purpose voltage-source power supply is based on a three-phase diode-rectifier - dc capacitor link - six-switch VSI configuration. This structure has been used because (a) it can operate in all the output frequency/voltage range without any major restriction, (b) it can produce acceptable input/output performance, and (c) it can provide fast and accurate on-line line current control [29-30, 34-35, 47-49].

The dual topology based on a CSI has been largely neglected due to the difficulties in controlling on-line the power switches. CS inverters are usually operated with a fixed pattern. Although the output current pattern is optimized, transient response of this current is slow, since it relies on changing the dc link current [57]. Moreover, if a thyristor front-end rectifier is used, the input power factor is low and load dependent [58]. However, CSI based topologies have intrinsic advantages, including: (a) the load voltages (and consequently the load currents for linear loads) are now sinusoidal. (b) inherent load short-circuit protection, the output current being limited by the dc bus current; (c) high converter reliability, due to unidirectional nature of the switches and the inherent short-circuit protection, and (d) instantaneous and sustained regeneration capabilities.

Due to these advantages, recent work has appeared in the literature, proposing

improvements to the standard structure; these include new structures [22], PWM techniques to applied at the CSI [13, 23, 59], and PWM techniques applied both rectifier and CSI [56, 60]. Moreover, new control strategies to improve waveform quality and speed of response have been reported, specifically through dc link current control [61-62] and through modulation index control of the CSI [22, 63-64]. Finally, integration of the dc link current and modulation index control has also been reported [65]. However, in this reported work, the dc link current control is based on the advance knowledge of the load variation. This assumption is not valid in the general case.

In this chapter a high performance three-phase voltage supply for fast fluctuating loads based on a PWM CSR - dc Link - PWM CSI topology is presented. The power circuit topology is symmetrical using identical input and output converters. Two control loops, to regulate the load voltage and the dc link current, are proposed. Thus, the fast load requirements are provided by the CSI, thus improving the transient performance, and the slower dc link current loop ensures high performance in steady state in terms of load harmonics and overall efficiency.

4.2 DESCRIPTION AND OPERATION

4.2.1 Power Circuit

The complete power circuit is shown in Fig. 4.1. The total configuration is composed of a three phase PWM CSR, a dc link reactor and a three phase PWM CSI. The main function of the PWM rectifier is to regulate the level of the dc link current (i_{dc}), by adjusting the dc PWM rectifier voltage (v_r). The implementation of PWM techniques requires gate turn-off switches devices such as BJTs, GTOs, or IGBTs, to be used as

unilateral rectifier switches.

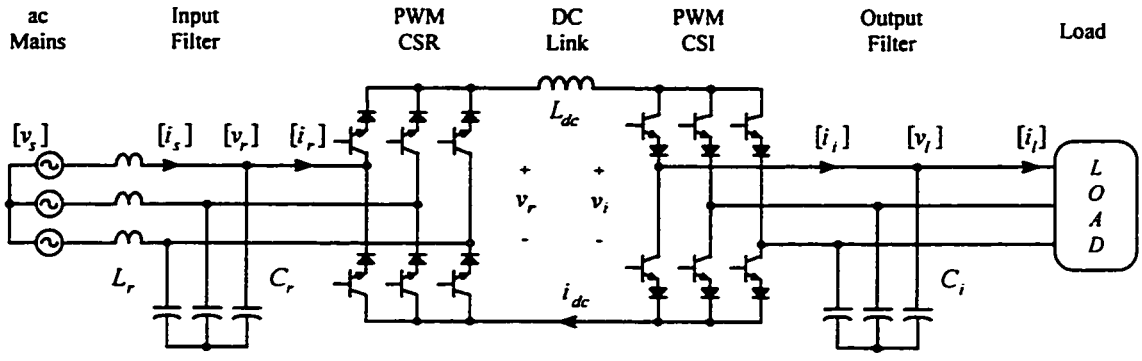

Fig. 4.1 Three-phase load voltage-regulated power supply topology.

The harmonics injected into the ac mains by the PWM rectifier operation are absorbed by the input filter (L_r, C_r); therefore, the input power factor is close to unity in its total operation range. The second system component is the dc link reactor (L_{dc}). Its function is to smooth the dc link current (i_{dc}) and therefore act as a current-source to the PWM-CSI. The magnitude of L_{dc} depends of the permissible dc link current ripple and the switching frequencies of the PWM CSR and PWM CSI. Finally, the main component is the CSI that produces three-phase PWM line currents ($[i_i]$) with minimum possible harmonic distortion. The output capacitive filter (C_i) absorbs the current harmonics generated by the CSI PWM action and defines the load voltage.

The proposed control diagram of the three phase voltage supply is shown in Fig. 4.2. The total control strategy is composed of two main control loops: the load voltage and the slower CSI modulation index loops. This last loop is actually a cascade structure where the inner loop is the dc link current loop.

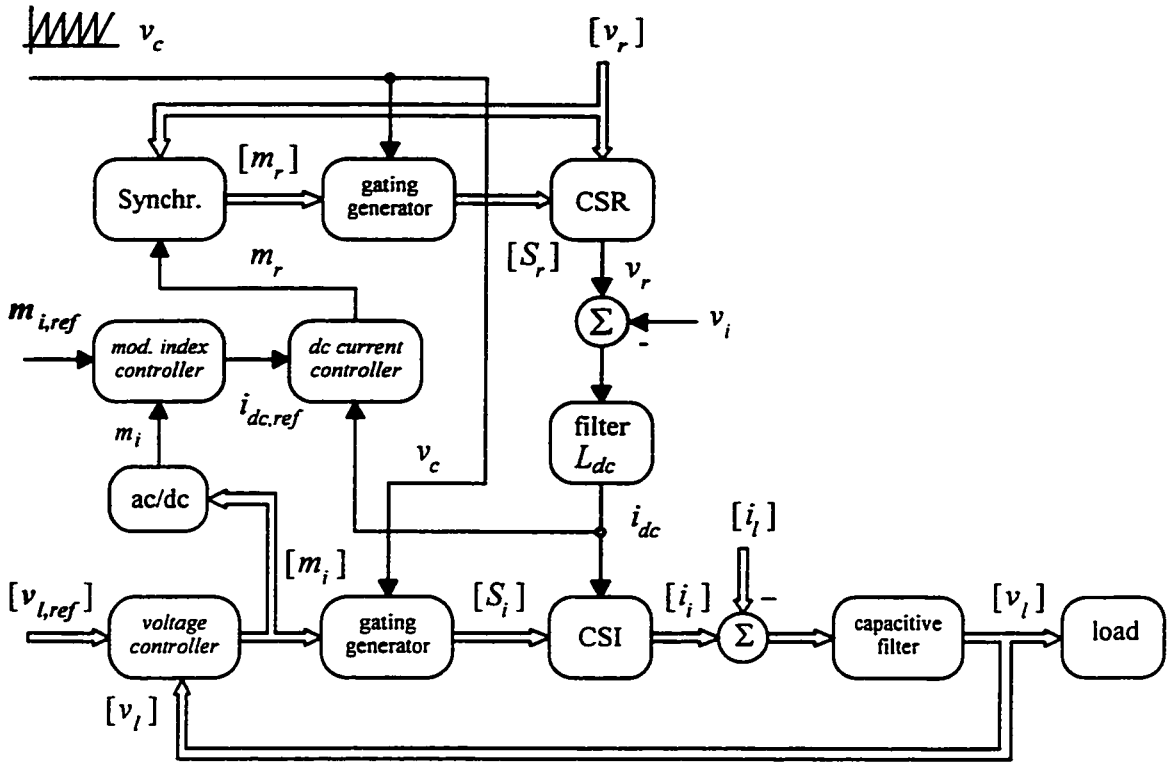

Fig. 4.2 Proposed control diagram of the voltage supply.

4.2.2 Load Voltage Control Loop

In order to provide a fast load voltage control, on-line modulation of the CSI is proposed. The loop is basically a feedback strategy, where the *voltage controller* block produces the modulating signals (m_{ik}, k = a, b, c) based on the difference between the load phase voltage reference vector ($[v_{l,ref}]$) and the actual load phase voltage vector ($[v_l]$). The modulating signals are used by the *gating generator* block to produce the gating signals (S_{ik}, k = 1,..., 6). This last block can be implemented using the analog or digital versions proposed in Chapters 2 and 3, respectively. Consequently, the *voltage controller* block can be implemented in an analog or digital version. This thesis reviews the *modified ramp comparison* (analog) and the *space vector* (digital) approaches.

A. Modified Ramp Comparison Controller

The *voltage controller* block can be implemented using a gain (P controller), or a gain and integrator (PI controller) in an analog fashion. The *gating generator* is the analog on-line pattern generator presented in Chapter 2, where the carrier (v_c) is a saw-tooth waveform. The maximum gain of the controller is adjusted such that the slope of the modulating signal never exceeds the triangular carrier slope. The CSI switching frequency is one half of the frequency of the carrier ($f_{sw} = 1/2 \cdot (f_c + 1)$) and the ac gain is equal to $G_{ac} = 1.0$. This approach produces well-defined harmonics in terms of magnitude and frequency, which simplifies the design of the filters. However, some disadvantages still remain: (a) there must be a steady state error between the reference and actual voltage for the system to operate properly and (b) the minimum error is limited by the maximum gain.

B. Space Vector Based Controller

This approach is entirely implemented on a microprocessor (DSP) and presents all the advantages of the above technique. In addition, since the *voltage controller* can be implemented in the *dq0* frame, zero steady state error can also be achieved. The *gating generator* is the digital on-line pattern generator presented in Chapter 3.

A reduction in the number of sensors can also be achieved in digital implementations. The load voltages are digitally reconstructed instead of measured. An additional algorithm uses the dc voltage and gating signal information to reconstruct the line load voltages. Experimental tests have shown that the totality of routines require a minimum sample time of approximately 120 μs on a TMS320C30 DSP chip and a

maximum sampling frequency of 8.33 kHz can therefore be achieved. APPENDIX B shows the algorithm used in experimental tests to on-line reconstruct the load voltages.

Table 4.1 presents a summary of the characteristics of the above strategies. The *hysteresis* (delta-modulated [66]) and SPWM *ramp comparison* approaches are also included as a base of comparison. Table 4.1 also shows that the *modified ramp comparison* and *space vector* based controllers exhibit excellent overall performance.

Table 4.1 Comparison of modulating techniques applied to VC-CSI.

Control Technique	switching frequency	ac gain	steady state error	spectrum
hysteresis	undefined	1.000	there may be	undefined
SPWM ramp comparison	f_c	0.866	there must be	well-defined
mod. ramp comp.	$1/2 \cdot (f_c + 1)$	1.000	there must be	well-defined
space vector (Seq_A)	$1/2 \cdot f_{cycle}$	1.000	zero	defined

4.2.3 CSI Modulation Index Control Loop

The second control loop is the PWM CSI modulation index control (m_i). The main function of this loop is to modify on-line the dc link current (i_{dc}) to the minimum possible to keep the steady state PWM CSI modulation index (m_i) equal to the reference ($m_{i,ref}$). The resulting modulation index strategy features: (a) minimum steady state stress in all the power switches due to the minimum dc link current operation, (b) constant harmonic load voltage distortion due to the fixed modulation operation, and (c) the potential to meet any load demand. Chapter 5 presents an application of the proposed voltage-regulated CSI based voltage supply, where the above features are quantified.

4.3 DESIGN CONSIDERATIONS

4.3.1 Filters Design

The design of the filtering components consists primarily in the choice of the C_i, L_{dc}, L_r, and C_r values (Fig. 4.1). The main criteria used to calculate them are (a) maximum peak-to-peak ripple and (b) a given resonance frequency. APPENDIX C.1 shows the derivation of the filter design guidelines.

A. Output Filter Design

The worst case corresponds when all the current harmonics generated by the PWM operation of CSI are absorbed by the output filter (C_i). This condition is the case of inductive loads and no load operation. Since the CSI ac currents [i_i] are PWM type, it is found that the capacitor reactance is given by,

$$X_{Ci} = X_l + \sqrt{(G_{ac}\, M_i\, f_c\, \Delta v_l)^2 + X_l^2 - 1} \quad \Omega \text{ pu} \tag{4.1}$$

where, Δv_l : maximum peak-to-peak voltage ripple in pu (usually 0.15 = 15 %)
M_i : nominal CSI modulation index (usually $M_i = 0.8$)
X_l : load reactance ($X_l = 0.6$ for a load with power factor = 0.8)
f_c : carrier frequency in pu

B. dc Link Filter Design

Both dc bus voltages (v_r and v_i in Fig. 4.1) are PWM type; therefore, the dc link inductor (L_{dc}) absorbs the instantaneous voltage differences and defines a dc current with minimum harmonic distortion. Considering that the worst condition is when both voltages are overlapped, the dc link reactance is given by,

$$X_{Ldc} = \frac{2\sqrt{6}}{\Delta i_{dc}\, f_c\, I_{dc}} \quad \Omega \text{ pu} \tag{4.2}$$

where, Δi_{dc} : maximum peak-to-peak dc current ripple (usually 0.1 pu = 10 %)
I_{dc} : nominal dc link current (pu)

C. Input Filter Design

The ac supply is naturally inductive (L_r) and therefore a capacitive component (C_r) must be inserted between the supply and the PWM CSR. Thus, C_r absorbs the current harmonics ($[i_r]$) injected by the PWM operation of the CSR and defines its input ac voltage ($[v_r]$). Since the CSR ac currents $[i_r]$ are PWM type, it is found that the capacitor reactance is given by,

$$X_{Cr} = \frac{\Delta v_r f_c}{I_{dc}} \quad \Omega \text{ pu} \tag{4.3}$$

where, Δv_r : maximum peak-to-peak voltage ripple (usually 0.10 pu = 10 %)

Usually, the ac supply inductance is adjusted to avoid any resonance phenomena by adding extra line reactance. Thus, if the normalized resonance frequency of the rectifier side filter is defined as f_{rr}, its value is chosen lower than half of the normalized carrier frequency (f_c) and higher than low frequency harmonics (5^{th}, 7^{th},... due to transient overmodulation of the CSR). Thus, the reactance is,

$$X_{Lr} = X_{Cr} / f_{rr}^2 \quad \Omega \text{ pu} \tag{4.4}$$

4.3.2 Controllers Design

The design guidelines are given for the load voltage, dc link current, and CSI modulation index controllers. The *modified ramp comparison* controller is used as the load voltage controller. APPENDIX C.2 shows the derivation of the following controller parameter design guidelines.

A. Load Voltage Controller

The *modified ramp comparison* controller is used. The *voltage controller* block in Fig. 4.2 is implemented using a PI analog controller to provide a satisfactory steady state performance. The gain is maximized to minimize the steady state error. However, in order to always ensure intersection between the modulating and the carrier waveform, there is a maximum possible proportional gain (K_{vl}) for a given integral gain (T_{vl}). A simplified expression of the maximum gain is given by,

$$K_{vl} = \frac{2 f_c T_{vl}}{\sqrt{1+(2\pi f_c T_{vl})^2}} \frac{V_c}{\Delta v_l} \quad 1/V \tag{4.5}$$

where, T_{vl} : normalized integral gain
V_c : normalized carrier amplitude

Fig. 4.3 shows the transfer function of the voltage close loop for various integral gains of the PI. The best transfer function is the one that is closer to unity and thereby, it presents minimum steady state error in a given operating region (10 to 180 Hz in this case). Thus, it is found that a suitable frequency response corresponds to $T_{vl} = 1.5\ t_c$.

B. dc Link Current Controller

The small signal model of the PWM rectifier is a first order type of system, where the dc link current (i_{dc}) versus the rectifier modulation index (m_r) transfer function is a pure integrator. A PI type controller is used to ensure zero steady state error and to obtain a desired overshoot (or damping ratio, ζ_{idc}) and settling time (t_{idc}). The expressions for the proportional gain (K_{idc}) and integral gain (T_{idc}) of the PI are given by,

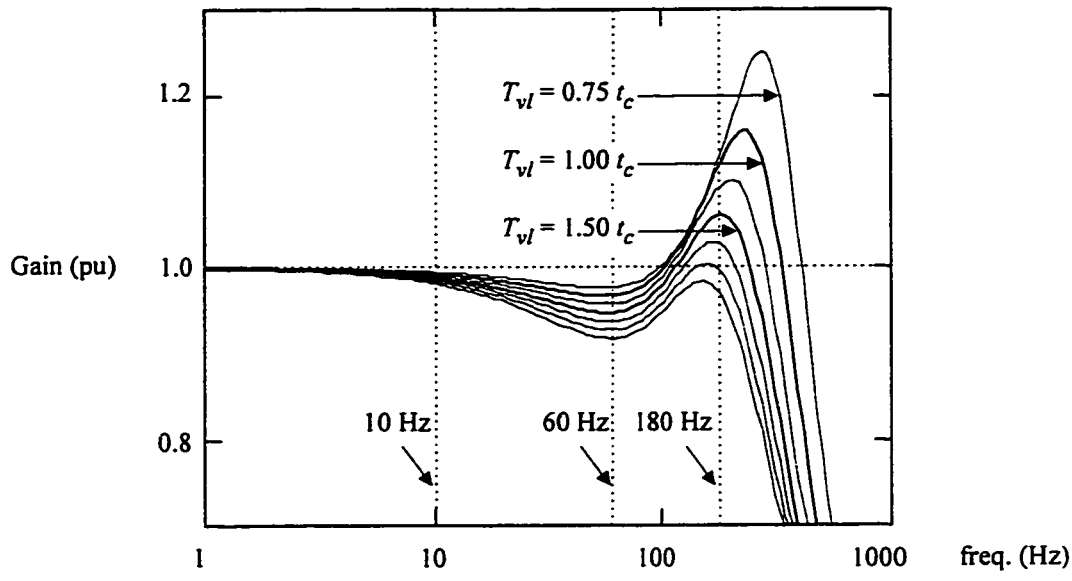

Fig. 4.3 VC-CSI voltage closed loop transfer function magnitude.
f_c = 33 pu, Δv_l = 0.15 pu, and M_i = 0.8

$$K_{idc} = \frac{V_c X_{Ldc} f_{cn} \ln(1/b_{idc})}{3\pi G_{ac} t_{idc}} \quad 1/\text{A} \tag{4.6}$$

where, t_{idc} : desired settling time in number of carrier periods (i.e. $= f_{cn}$ pu)
b_{idc} : settling time band (i.e. = 0.02 pu = 2 %)

$$T_{idc} = \frac{2\zeta_{idc}^2 t_{idc}}{\ln(1/b_{idc})} \quad \text{s} \tag{4.7}$$

where, ζ_{idc} : desired damping ratio (i.e. = 0.57 for 10 % overshoot)

Like the load voltage controller, the gains K_{idc} and T_{idc} of the PI controller should be limited in order to ensure intersection between the carrier and modulating waveforms. However, since the desired settling time is several times the carrier period, (4.6) and (4.7) are always within the safe range.

C. *CSI Modulation Index Controller*

The modulation index of the CSI (m_i) is adjusted by manipulating the dc link current (i_{dc}). The small signal model is a pure negative gain and thereby, a modified PI controller is used to ensure zero steady state error and to obtain a given overshoot (or damping ratio, ζ_{mi}) and settling time (t_{mi}). The proportional (K_{mi}) and integral (T_{mi}) gains are given by,

$$K_{mi} = \frac{I_{dc}}{4\zeta_{mi}^2 M_i} \quad \text{A} \tag{4.8}$$

$$T_{mi} = \frac{t_{mi}}{2\ln(1/b_{mi})} \quad \text{s} \tag{4.9}$$

where, I_{dc} : normalized dc link current (pu)
ζ_{mi} : desired damping ratio (i.e. = 0.57 for 10 % overshoot)
M_i : nominal CSI modulation index (i.e. = 0.8)
t_{mi} : desired settling time in pu (i.e. = 3 pu)
b_{mi} : settling time band (i.e. = 0.02 pu = 2 %)

4.4 SIMULATED AND EXPERIMENTAL RESULTS

Simulated results, on a pu basis and for a 50% step-down in the load current at t_o = 12 ms, are illustrated in Fig. 4.4 and Fig. 4.5. Specifically, Fig. 4.4 shows the power circuit relevant waveforms and Fig. 4.5 shows the control circuit relevant waveforms. The selection of the power circuit components and control parameters is done by following the design guidelines provided in Section 4.3. The integrated three-phase voltage-regulated CSI topology is implemented on an experimental 2 kVA set-up. The simulation and experimental conditions are given in APPENDIX A.3. From the simulated and experimental results (Fig. 4.6) it is possible to conclude that:

- The input current is PWM type, Fig. 4.4(a). This feature ensures minimum distortion factor and thereby, near unity input power factor. In the experimental set-up a power factor greater than 0.9 was always obtained.
- The step-down load current does not affect the output voltage, moreover, the load voltage tracks the reference in amplitude and phase, before, while and after the transient, Fig. 4.4(e).
- Both dc PWM rectifier (v_r) and dc PWM inverter voltages (v_i) have PWM waveshapes, Fig. 4.4(b), Fig. 4.4(c), and Fig. 4.6(d). These features reduce the magnitude of the dc link reactor (L_{dc}) and therefore improve the dynamic response of the dc current.
- The step-down load current is instantaneously absorbed by the modulation indexes ($[m_i]_{abc}$, Fig. 4.5(e)) on the voltage control loop, Fig. 4.2. The approximated delay time is 1/carrier frequency (= $1/f_c$).
- The steady state CSI modulation index (m_i, Fig. 4.5(a)) is achieved by modifying the dc link current(i_{dc}, Fig. 4.5(b)) through the modulation index and dc link current controllers, Fig. 4.2.
- The dc link current is modified by controlling the PWM rectifier modulation index (m_r, Fig. 4.5(c), $[m_r]_{abc}$, Fig. 4.5(d)).
- The variable dc link current operation mode (or fixed CSI modulation index) permits operation with constant load voltage harmonic distortion (< 5 %).

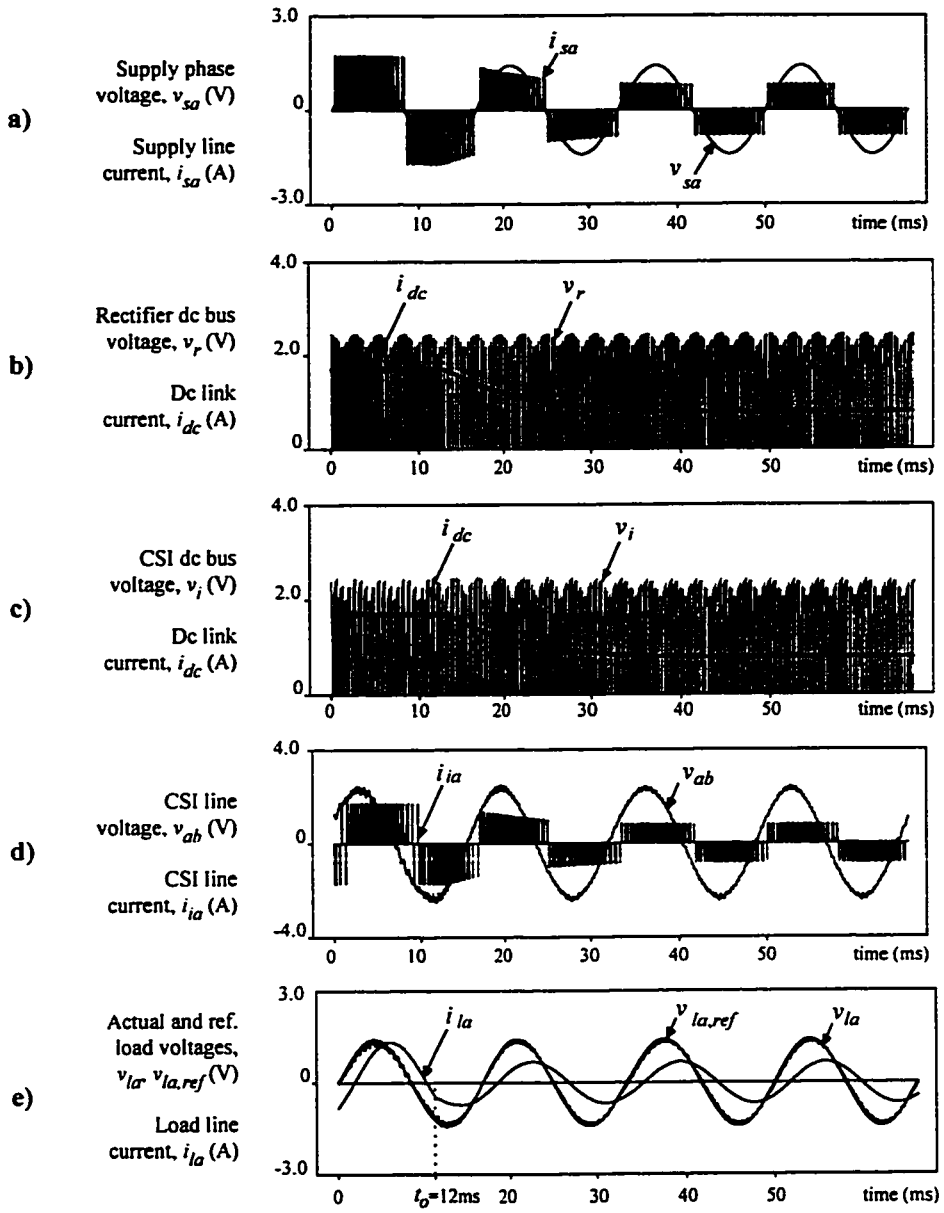

Fig. 4.4 VC-CSI power circuit simulated waveforms.

a) Ac supply volt. (v_{sa}) and current (i_{sa}). **b)** Rect. dc volt. (v_r) and dc current (i_{dc}). **c)** CSI dc volt. (v_i) and dc current (i_{dc}). **d)** Load line volt. (v_{ab}) and CSI ac current (i_{ia}). **e)** Load volt. (v_{la}), load ref. volt. ($v_{la,ref}$) and load current (i_{la}).

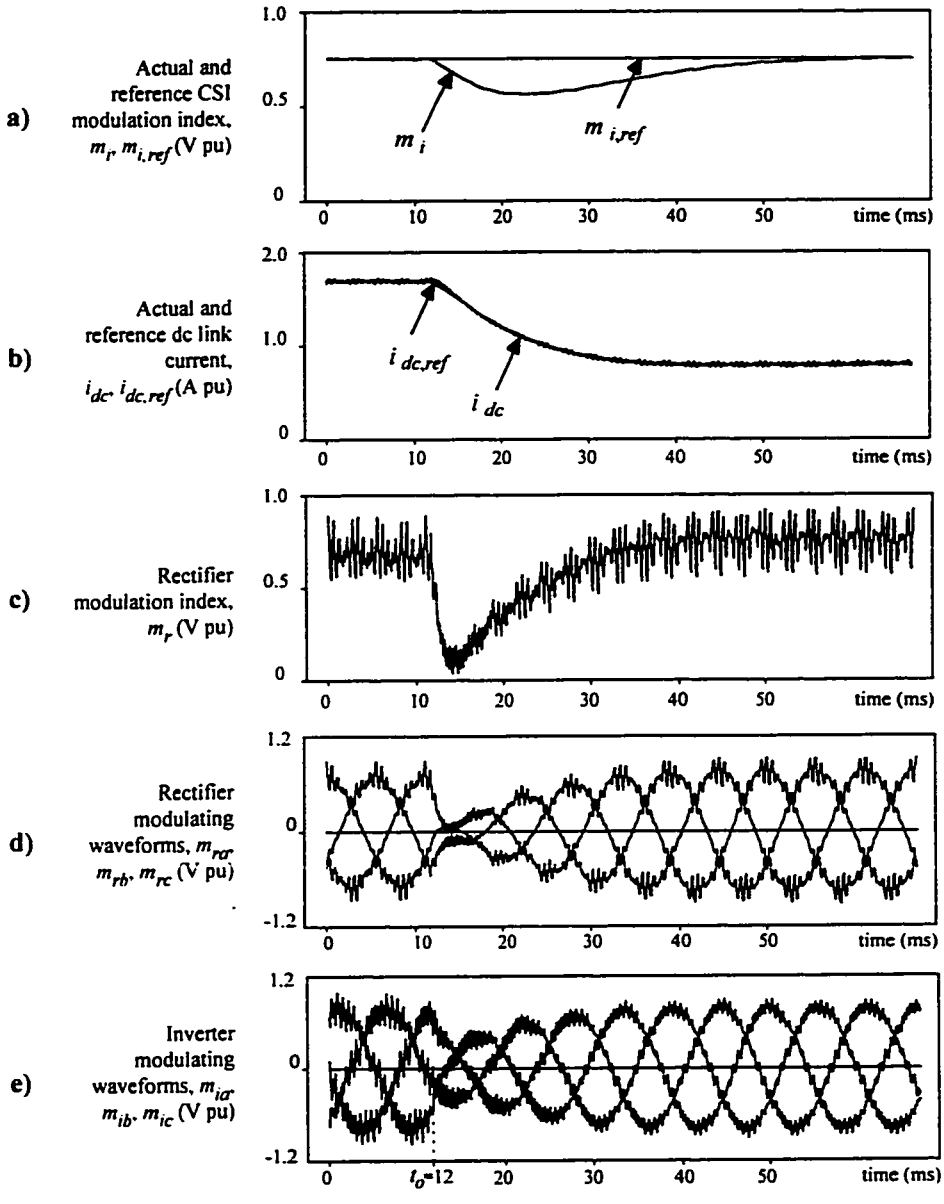

Fig. 4.5 VC-CSI control circuit simulated waveforms.

a) CSI modulation index ref. ($m_{i,ref}$) and actual mod. index (m_i). **b)** Dc current ref. ($i_{dc,ref}$) and actual dc current (i_{dc}). **c)** Rect. mod. index (m_r). **d)** Rect. modulation index vector ($[m_r]_{abc}$). **e)** CSI modulation index vector ($[m_i]_{abc}$).

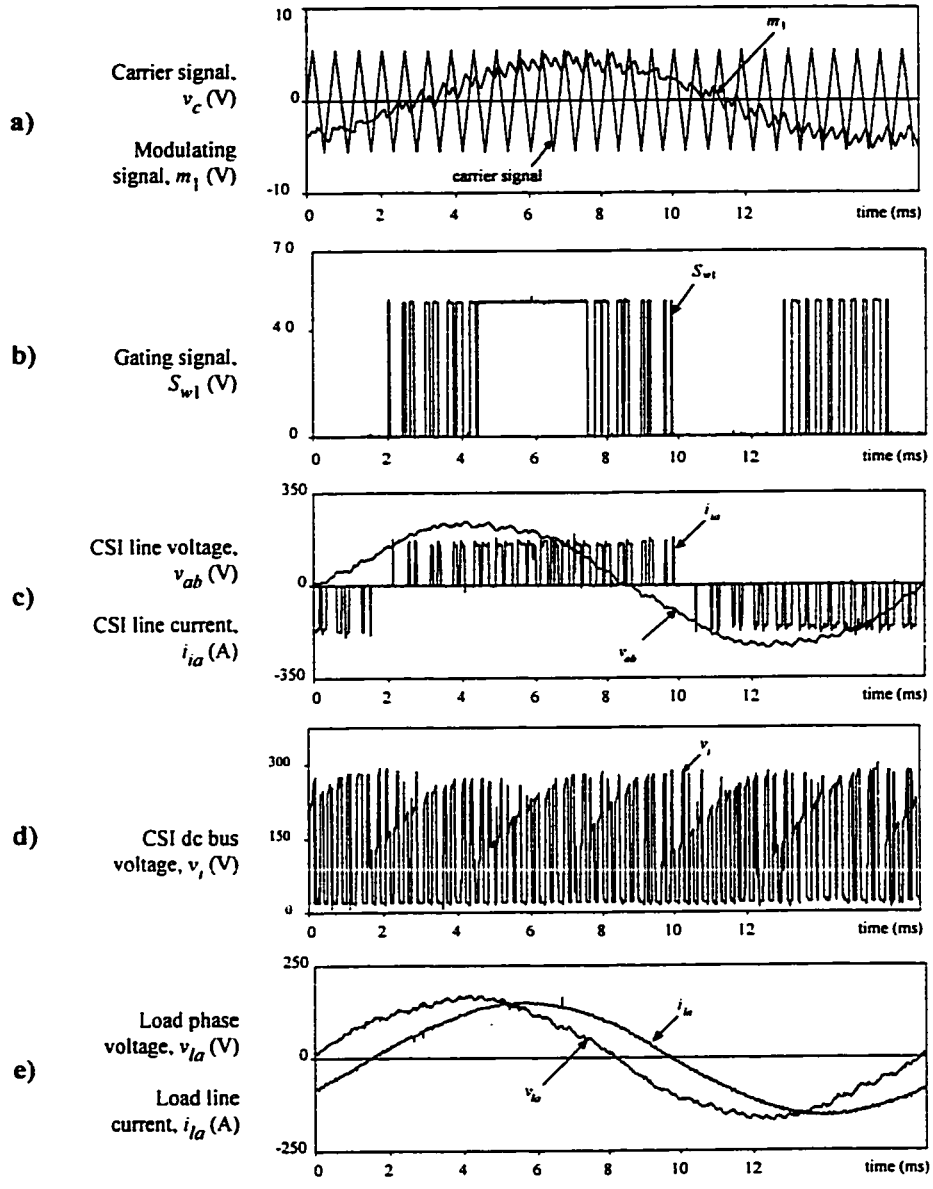

Fig. 4.6 VC-CSI experimental waveforms using ramp comparison.

Modulation index, $m = 0.8$, carrier frequency, $f_c = 1620$ Hz. **a)** Carrier and modulating signal (m_{ia}). **b)** Gating pattern, switch 1 (S_{i1}). **c)** Load line voltage (v_{ab}) and CSI output current ($10 \cdot i_{ia}$). **d)** CSI dc bus voltage (v_i). **e)** Load phase voltage (v_{la}), and load line current ($10 \cdot i_{la}$).

- Since the carrier frequency is constant, the switching frequency is therefore constant and independent of the load frequency operation.

4.5 Discussion and Conclusions

This chapter has demonstrated the feasibility of a variable voltage/frequency power supply based on an integrated current-source rectifier/inverter topology. The main features of the system include: (a) symmetrical current-source topologies for both front-end and load converters, (b) on-line analog generation of the gating signals for both PWM rectifier and inverter, (c) fast inner load voltage control loop, and (d) self-regulated dc link current loop that provides minimum dc link current operation and fixed CSI modulation index operation mode. Therefore, in addition to the inherent advantages of the CSI topology (short-circuit protection and regeneration capabilities), the above features lead to the following improved characteristics: (a) PWM waveforms with constant harmonic frequencies (which allows accurate design of filtering components), (b) near unity input power factor operation, (c) sinusoidal load voltages with fixed harmonic distortion regardless of the load magnitude and frequency operation, and (d) minimization of the power converter conduction losses and dc link inductor conduction losses.

CHAPTER 5

HIGH PERFORMANCE AC INDUCTION MOTOR DRIVE

5.1 INTRODUCTION

AC adjustable speed induction motor drives employ mostly a VSI topology to control the motor armature voltage [67-68]. Both scalar and vector control of induction motors are implemented using this approach, the latter requiring current control of the VSI [69]. On the other hand, the CSI topology offers inherent advantages (Chapter V), which make the structure best suitable for medium and high power applications [70]. Despite the advantages, the configuration when based on a thyristor front-end rectifier, still presents a poor input power factor. This due to the facts that the input line current is a six-step type of waveform and the control is based on phase control. To overcome these drawbacks, it has been proposed to replace the front-end thyristor rectifier by a PWM-CSR [71-72], allowing the operation with a near unity power factor.

However, the implementation of PWM-CS drive systems is complicated and may generate additional drawbacks. The difficulties are due to the complexity of the CSI gating signals compared to the VSI gating signals, this has resulted in the widespread use of Selective Harmonic Elimination (SHE) stored patterns [15][64][73]. In those control schemes that use stored patterns (such as SHE), and variable dc link current, it is possible to have a potential resonance between the output filter capacitor and the motor leakage inductance [62][74]. Finally, in those control schemes that use fixed dc current and a

variable modulation index PWM generator at the CSI stage, it is found that [23][75-76]: (a) there are important losses in the switches and dc inductor, (b) the power switches are under constant current stress (they commutate at maximum current), and (c) the harmonic distortion of the motor voltage varies with the CSI modulation index.

This chapter describes a CSI based ac induction machine drive with the following features: (a) the entire control strategy is implemented in a DSP system, based on the TMS320C30 chip, (b) the speed control strategy is based on a constant *V/f* scalar control technique, (c) both the rectifier and inverter topologies are Space Vector modulated. Furthermore: (a) the motor voltage is regulated on-line by using a feedback control technique and (b) the dc link current is regulated to the minimum value required to keep the inverter modulation index constant and independent of the speed reference and load torque. The above features lead to the following advantages over conventional CSI motor drive implementations: (a) the gating signals are directly generated by the Space Vector digital modulators (extra circuitry is only necessary to ensure overlaps), (b) the supply current harmonic distortion is constant and approximately equal to 3.5 % which leads to a input power factor always greater than 0.95, (c) the potential resonance is eliminated due to the feedback based voltage controller, (d) the stresses on power switches and the overall losses are always minimum due to the minimum dc link current operation, and (e) due to the constant inverter modulation index operation, the motor voltage harmonic distortion is constant, which minimizes the induction motor losses and allows an accurate output filter design. These features make the CSI drive an interesting alternative to the VSI based drives.

A complete comparison with conventional ac drives CSI based is also presented. Key performance indices such as harmonic distortion (*THD*), power factor (*pf*) and time response are evaluated and tabulated for both the conventional and the proposed schemes. Simulated and experimental results are given for a 3 kVA induction motor drive.

5.2 CONVENTIONAL CSI BASED AC DRIVES

In this chapter, drive classification is based upon the front end power converter type, which could be either a phase controlled or a PWM rectifier.

5.2.1 Phase controlled front end rectifiers

These drives use a thyristor front end rectifier (Fig. 5.1) and are operated at either variable or fixed dc current. The overall performance depends upon this feature.

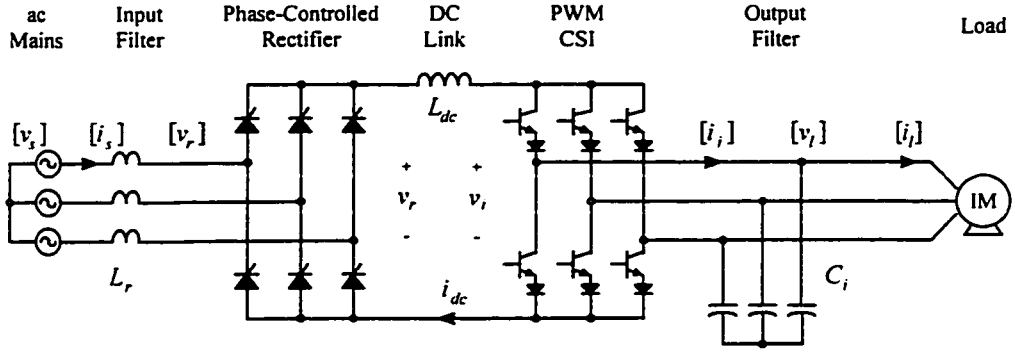

Fig. 5.1 Ac drive based on a phase controlled front end rectifier converter.

A. Variable dc Link Current Scheme.

The CSI is operated with a fixed pattern which is usually optimized in terms of harmonic spectrum and switching frequency. Thus, the load voltage harmonic distortion

(THD_{vl}) is minimum and constant (Table 5.1). In order to control the speed of the machine, the dc link current is continuously adjusted in such a way that the requirements of the load (speed and torque) are always meet. At a given speed, the dc current is continuously adjusted to meet the load torque requirements; therefore, independent of the load torque. Thus the input current displacement factor (or input power factor) is only speed dependent (Table 5.1). Also, since the dc link current is kept to a minimum value, the dc bus and switch conduction losses are also minimized. Usually, the dc link inductor is designed to have an acceptable dc link current ripple (5%). In order to achieve this value and due to the low order harmonics injected by the thyristor rectifier (6, 12, ...), the size of the dc inductor becomes quite bulky and thereby, the time response of the system is poor. Also, the supply current presents a high distortion factor (THD_{is} = 142%) due to the low order harmonics (5, 7, ...) injected by the thyristor rectifier (Fig. 5.2, APPENDIX A.4).

B. Fixed dc Link Current Scheme.

Unlike the above control scheme, the CSI is operated with a variable PWM pattern. Therefore, the load voltage harmonic distortion (THD_{vl}) is variable and depends upon the speed and load torque (Table 5.1). Since the dc link current is fixed, the different load power requirements are supplied by varying the dc link voltage. To achieve this, the input current displacement factor is continuously adjusted and, thereby, the input power factor becomes variable and close to zero for light loads (Fig. 5.3, APPENDIX A.4).

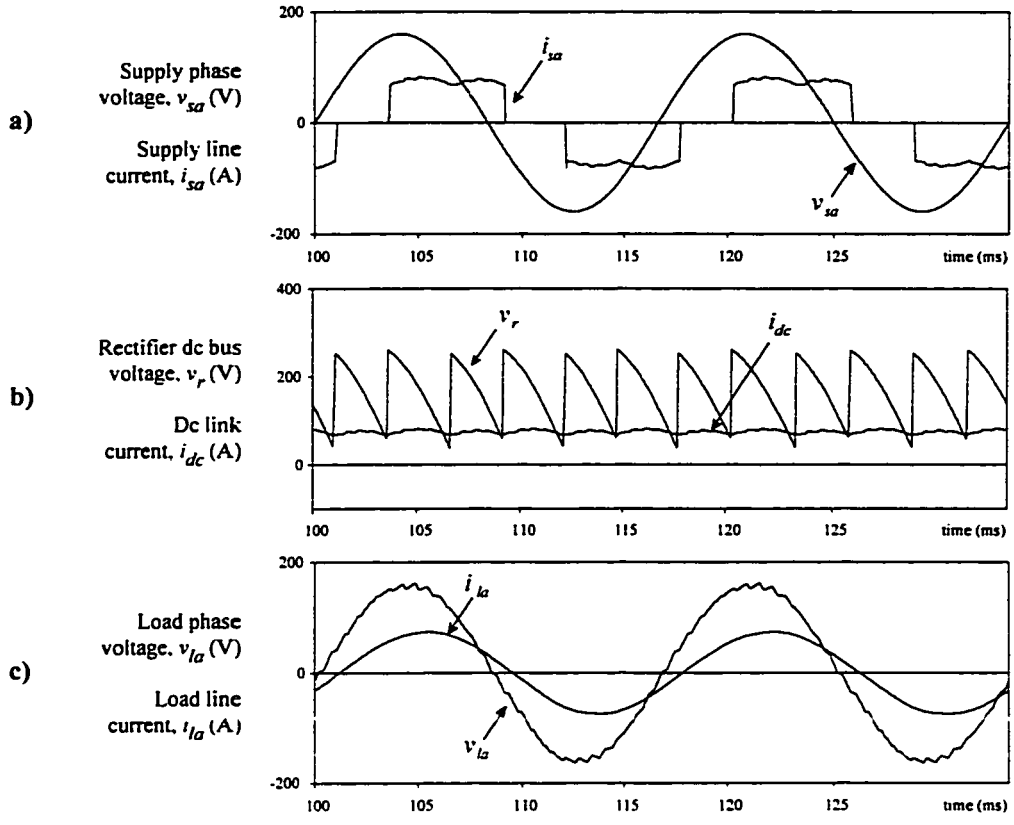

Fig. 5.2 Ac drive based on a phase controlled rectifier and variable dc current mode.

Simulated waveforms for 50% nominal load and 60 Hz output. **a)** Supply phase voltage (v_{sa}) and supply line current ($15 \cdot i_{sa}$). **b)** dc rectifier voltage (v_r) and dc link current ($15 \cdot i_{dc}$). **c)** Load phase voltage (v_{la}) and load line current ($15 \cdot i_{la}$).

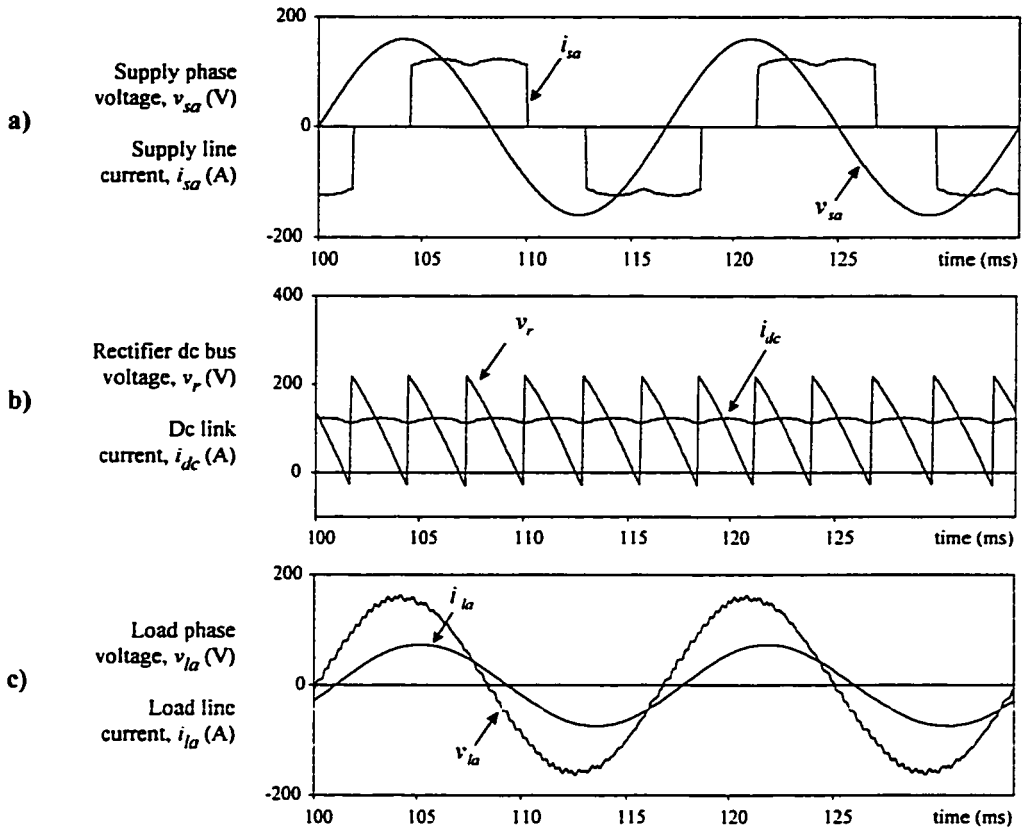

Fig. 5.3 Ac drive based on a phase controlled rectifier and fixed dc current mode.

Simulated waveforms for 50% nominal load and 60 Hz output. **a)** Supply phase voltage (v_{sa}) and supply line current ($15 \cdot i_{sa}$). **b)** dc rectifier voltage (v_r) and dc link current ($15 \cdot i_{dc}$). **c)** Load phase voltage (v_{la}) and load line current ($15 \cdot i_{la}$).

Table 5.1 CSI based ac drive schemes-comparison.

Parameter	Thyristor Front End Rectifier		PWM Front End Rectifier	
	Variable i_{dc} Fixed CSI Pattern	Fixed i_{dc} PWM CSI	Fixed i_{dc} PWM CSI	Variable i_{dc} PWM CSI ♣
THD_{vl}, motor voltage harmonic distortion	speed dependent $10 < THD_{vl} < 3.5\ \%$	speed dependent $10 < THD_{vl} < 3.5\ \%$	speed dependent $10 < THD_{vl} < 3.5\ \%$	constant $THD_{vl} = 3.5\%$
THD_{is}, supply current harmonic distortion	constant $THD_{is} = 142\%$	constant $THD_{is} = 142\%$	speed-torque dep. $10 < THD_{is} < 3.5\ \%$	constant $THD_{is} = 3.5\%$
ac supply power factor (pf_s)	speed dependent $0 < pf_s < 0.85$	speed-torque dep. $0 < pf_s < 0.85$	speed-torque dep. $0.8 < pf_s < 0.95$	constant $pf_s = 0.95$
transient response τ	slow $\tau \cong 1/L$	fast $\tau \cong 1/60$	very fast $\tau \cong 1/f_{cycle}$	very fast $\tau \cong 1/f_{cycle}$
dc bus and switch conduction losses	reduced	high	high	minimized

♣: Proposed CSI based ac drive control scheme.

where, $THD_{vl}\% = \dfrac{\sqrt{\sum_{k=2}^{\infty} V_{lk}^2}}{V_{l1}} \cdot 100$ and $THD_{is}\% = \dfrac{\sqrt{\sum_{k=2}^{\infty} I_{sk}^2}}{I_{s1}} \cdot 100$

Contrary to the variable dc link current scheme, the dc bus and switch conduction losses are always high due to the fact that the dc link current is always high (Table 5.1). Although the dc link inductor size is as big as the one used in the above scheme, the dynamic response is improved due to the variable PWM pattern approach and time responses are of the order of 1/60 s. This scheme also presents a high supply current harmonic distortion due to the thyristor rectifier operation (Table 5.1).

5.2.2 PWM front end rectifiers

Unlike phase controlled rectifier topologies, this topology uses a PWM rectifier (Fig. 5.4) and is operated with fixed dc link current. Therefore, in contrast to topologies based on thyristor front end rectifiers, the supply sees a overall system with enhanced performance indices. In fact, the overall drive input power factor is always greater than 0.95 and the total current harmonic distortion is always lower than 10% (Table 5.1). Also, since the CSI is PWM modulated, the system has time responses close to the switching period. However, the dc bus losses and switch conduction losses are very high due to the fixed dc link current operation mode (Fig. 5.5, APPENDIX A.4).

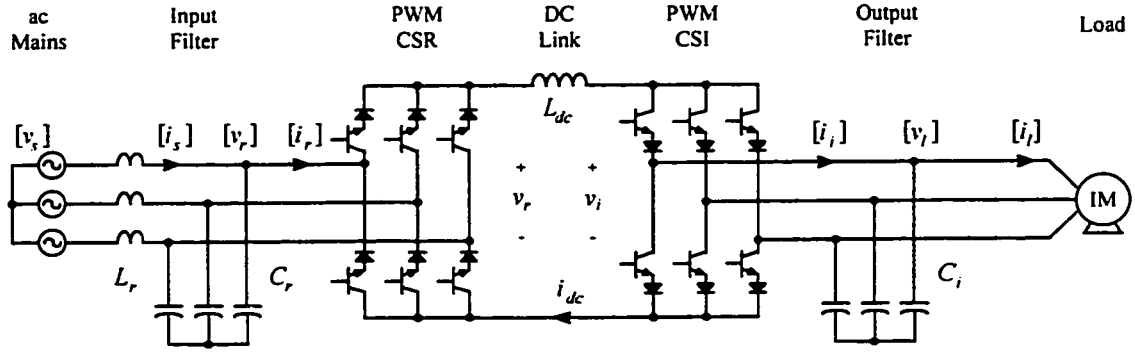

Fig. 5.4 Ac drive based on symmetrical PWM current-source converters.

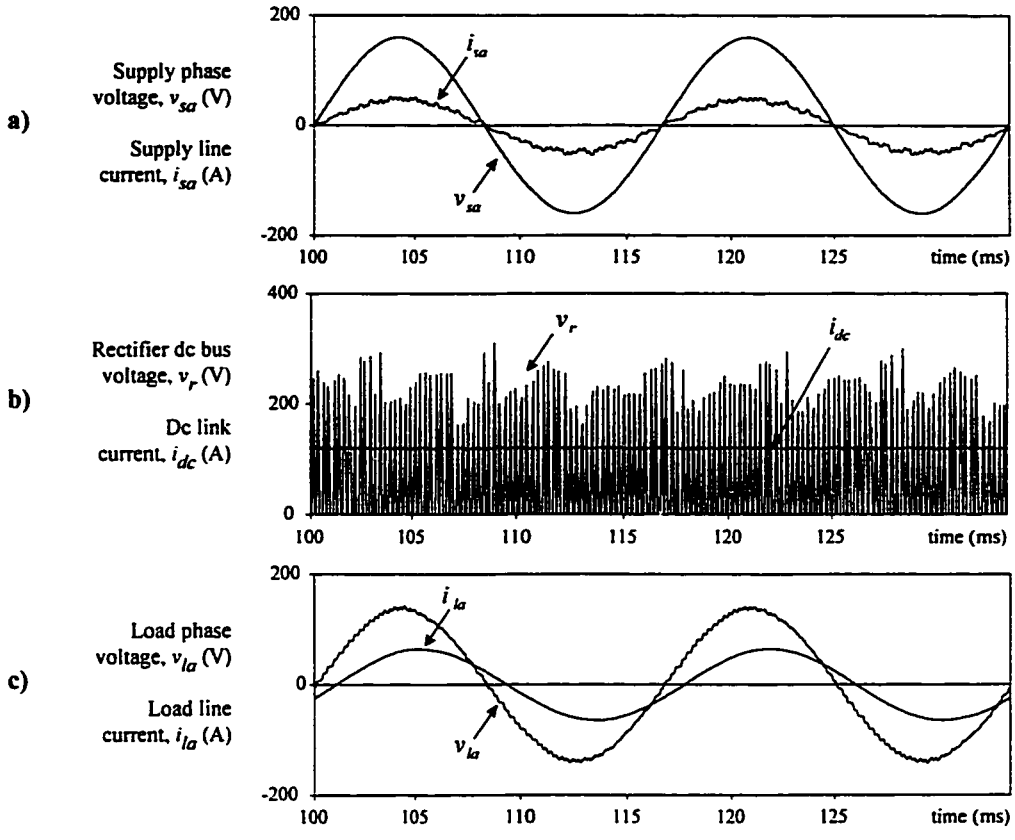

Fig. 5.5 Ac drive based on a PWM rectifier and fixed dc current mode.

Simulated waveforms for 50% nominal load and 60 Hz output. **a)** Supply phase voltage (v_{sa}) and supply line current ($15 \cdot i_{sa}$). **b)** dc rectifier voltage (v_r) and dc link current ($15 \cdot i_{dc}$). **c)** Load phase voltage (v_{la}) and load line current ($15 \cdot i_{la}$).

5.3 PROPOSED AC INDUCTION MOTOR DRIVE

5.3.1 Power Circuit

The complete power circuit is shown in Fig. 5.4. It is composed of a three phase PWM-CS rectifier, a dc link reactor and a three phase PWM-CSI. The main function of the rectifier is to regulate the dc link current (i_{dc}), by adjusting the rectifier dc voltage (v_r). The high frequency harmonics injected into the ac mains by the PWM rectifier operation are absorbed by the input filter (L_r, C_r). Therefore, the input distortion power factor and thereby, the overall input power factor is close to unity over the whole operating range.

The second system component is the dc link reactor (L_{dc}). Its function is to smooth the dc link current (i_{dc}) and therefore act as a current-source to the PWM-CSI. The magnitude of L_{dc} depends on the permissible dc link current ripple and the switching frequencies of the PWM-CSR and PWM-CSI (practical switching frequencies are of the order of kHz; therefore, the size of the dc link inductor is substantially smaller than for the thyristor rectifier case). Finally, the CSI produces three phase PWM line currents ($[i_l]$). The output capacitive filter (C_l) absorbs the high frequency current harmonics generated by the CSI PWM action and thereby, defines the sinusoidal output voltage.

5.3.2 Speed and CSI Modulation Index Loops

The proposed control diagram of the CSI based ac drive is shown in Fig. 5.6. The entire control scheme is digitally implemented on a DSP system based on the TMS320C30 chip. The control strategy is composed of two main control loops.

The first control loop is the motor speed control (ω_m) based on a slip speed regulator, which sets the slip speed reference (ω_{sl}) [68]. The synchronous speed (ω_{ms}), obtained by adding actual speed and slip speed, determines the inverter frequency (f_l). The motor voltage reference signal ($V_{l,ref}$) is generated from the frequency using a function generator, which ensures a nearly constant flux operation. Finally, the Voltage Controller and the Space Vector Modulator produce the switching pattern ($[S_l]$) based on the difference between the sine voltage reference waveforms ($v_{l,ref}$) and the sampled load voltage waveforms (v_l). This feedback scheme ensures that the CSI gating pattern ($[S_l]$), is modified on-line so as to force the load voltage v_l to track the reference $v_{l,ref}$ thereby resulting in a fast dynamic response (rise times in the range of the cycle period, t_{cycle}).

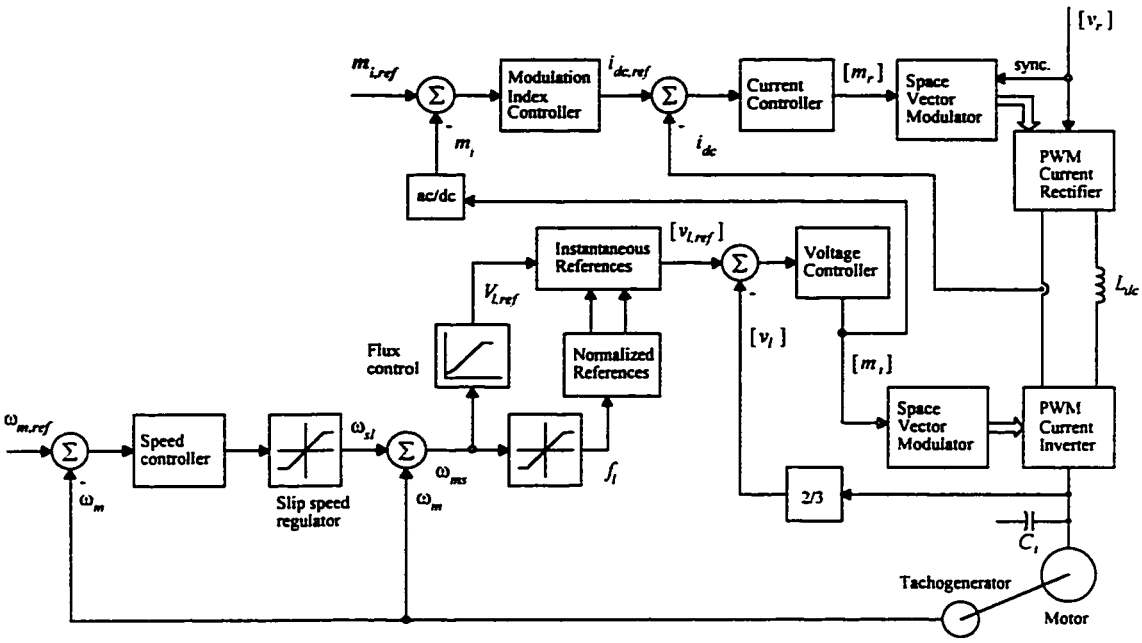

Fig. 5.6 Proposed control scheme for the ac drive based on CS converters.

The second control loop is the PWM-CSI modulation index control (m_i) based on Space Vector control of the front-end converter. The main function of this slower loop is to regulate on-line the dc link current (i_{dc}) to the minimum possible value required to keep the steady state PWM-CSI modulation index (m_i) equal to the reference ($m_{i,ref}$). The *load voltage*, *modulation index*, and *dc link current* controllers have been introduced and described in Chapter 4.

5.4 CONVERTER AND DRIVE PERFORMANCE

5.4.1 Voltage and Current Waveforms

The simulated voltage and current waveforms for the proposed control scheme are given in Fig. 5.7 for the nominal operating speed, and a half load operation. As expected,

the output (motor) voltage (Fig. 5.7(c)), presents a low ripple content (approximately 3.5%) (Fig. 5.8). Also, the input line current (Fig. 5.7(a)), has a minimum ripple content and is in phase with the phase voltage (these features ensure a nearly unity input power factor). The dc link current (Fig. 5.7(b)) is smaller than the value required to supply full load. Thus, it is guaranteed that the dc bus losses (Fig. 5.9) and switch conduction losses (Fig. 5.10) are also reduced as the required load power decreases. The simulated drive system and parameters values are given in APPENDIX A.4.

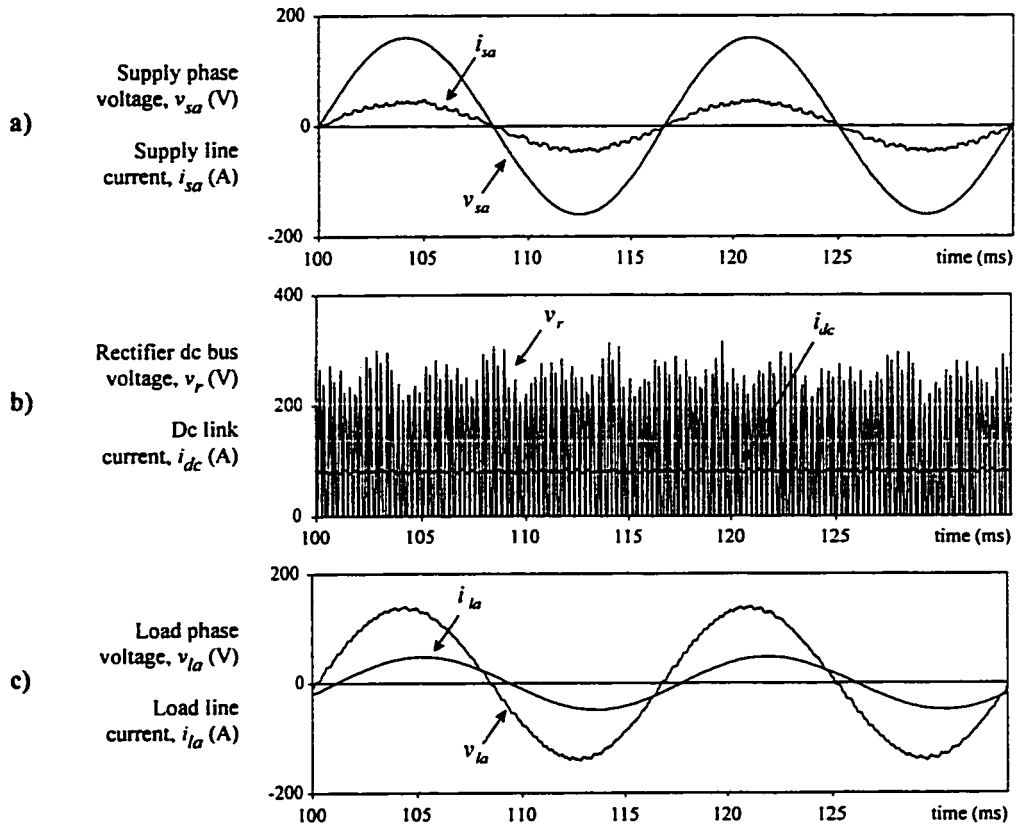

Fig. 5.7 Simulated waveforms for steady state operation.

50% nominal load and 60 Hz output. **a)** Supply phase voltage (v_{sa}) and supply line current ($15 \cdot i_{sa}$). **b)** Dc rectifier voltage (v_r) and dc link current ($15 \cdot i_{dc}$). **c)** Load phase voltage (v_{la}) and load line current ($15 \cdot i_{la}$).

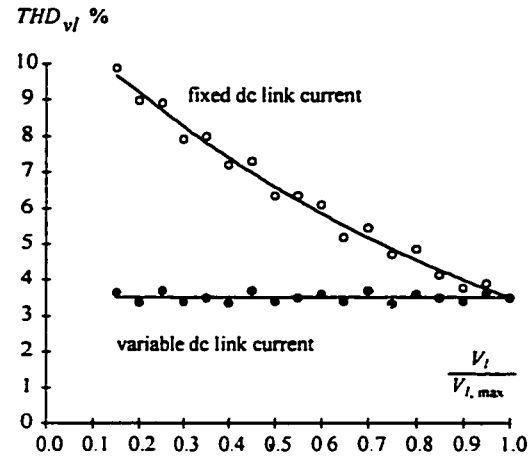

Fig. 5.8 Motor voltage harmonic distortion.

THD_{vl} as a function of the normalized load voltage or frequency (speed) (f_l = 48 pu, X_{Ci} = 4 pu)

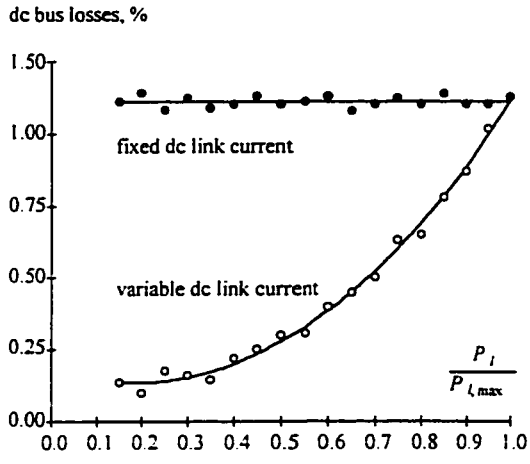

Fig. 5.9 dc bus conduction losses.

As a function of the normalized load power (torque) (f_l = 60 Hz, f_{cycle} = 48 pu, X_{Ci} = 4 pu, X_{Ldc} = 2 pu)

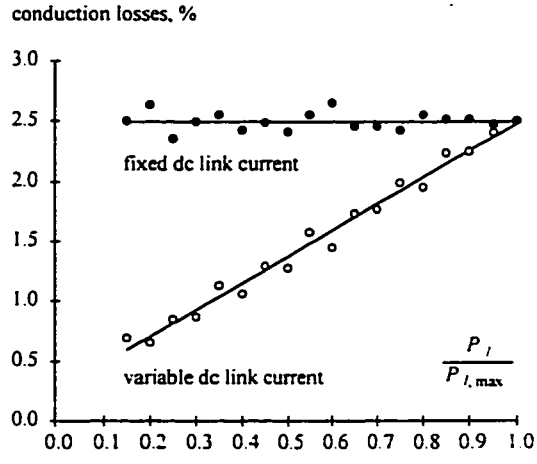

Fig. 5.10 CSI switch conduction losses.

As a function of the normalized load power (torque) (f_l = 60 Hz, f_{cycle} = 48 pu, X_{Ci} = 4 pu, X_{Ldc} = 2 pu)

5.4.2 Effect of Resonances on Drive Operation

The transfer function of inverter (motor) output voltage (v_l) to inverter modulating waveform (m_i) for the open loop case is given in Fig. 5.11(a). There is a resonance associated with the motor leakage reactances. Fig. 5.11(b), which plots the transfer

function of inverter (motor) output voltage (v_l) to motor voltage reference ($v_{l,ref}$), shows that the resonance is effectively attenuated through the action of the feedback voltage control loop. The implementation of this loop is possible due to the on-line gating of the CSI. APPENDIX D shows the transfer functions derivation.

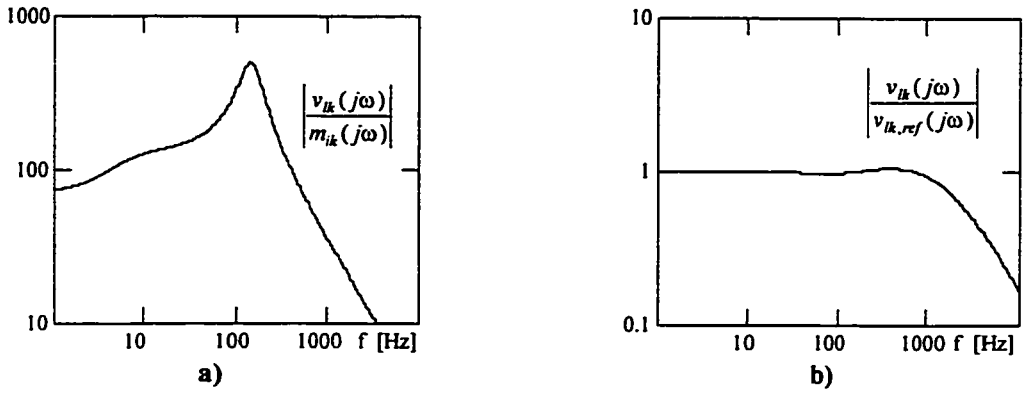

Fig. 5.11 Motor voltage transfer functions.

a) Motor voltage (v_{lk}) to modulating waveform (m_{ik}), open loop case. **b)** Motor voltage (v_{lk}) to motor voltage reference ($v_{lk,ref}$), close loop case. (k = a, b, c).

5.4.3 Efficient Improvement

Since in steady state the CSI modulation index control loop keeps the dc link current level to its minimum value (which depends upon the speed and load), it is possible to conclude that: (a) the input converter losses are reduced, (b) the losses in the dc link inductor (Fig. 5.9) and switches (Fig. 5.10) are minimized, (c) there is minimum steady state stress current in all the power switches, and (d) the CSI is operated under maximum current utilization. Also, since this loop keeps the CSI modulation index equal to the reference value as well, it is possible to conclude that: (a) the harmonic distortion of the motor voltage is kept constant and low (THD_{vl} = 3.5%) for any motor speed operation (Fig. 5.8) and (b) it has the potential to meet any load demand.

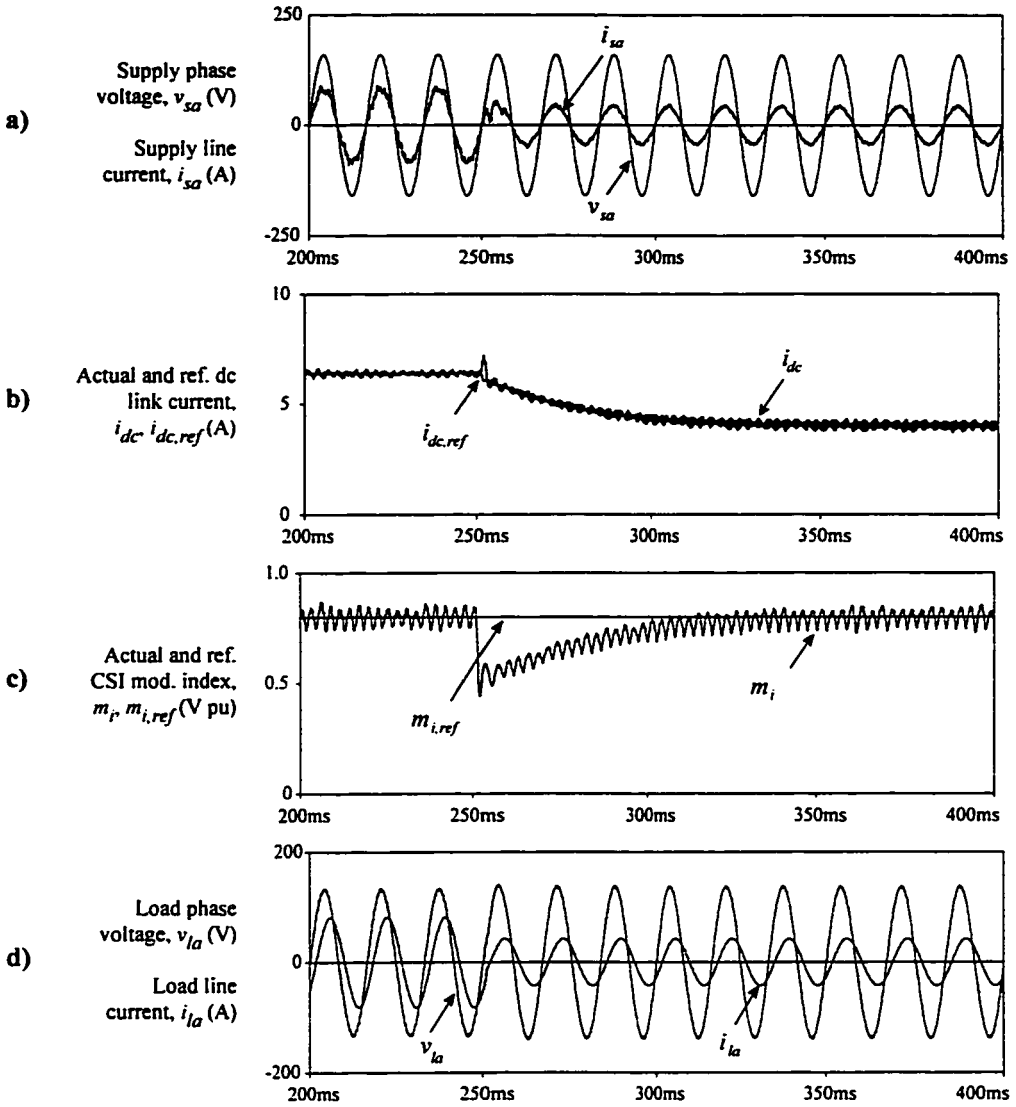

Fig. 5.12 Simulated transient response.

For 50% step-decrease in load torque (at t_o = 250 ms) and 60 Hz output. **a)** Supply phase voltage (v_{sa}) and supply line current ($15 \cdot i_{sa}$). **b)** Actual (i_{dc}) and reference ($i_{dc,ref}$) dc link current. **c)** CSI actual (m_i) and reference ($m_{i,ref}$) modulation index. **d)** Load phase voltage (v_{la}) and load line current ($15 \cdot i_{la}$).

5.4.4 Transient Response

To illustrate the dynamic response of the inner loops, a 50% step-decrease in the load torque is initiated at t_o = 250 ms. The simulated results are given in Fig. 5.12. Specifically, Fig. 5.12(d) shows how the motor voltage loop keeps the load voltage equal

to the reference before, during and after the load transient. Fig. 5.12(c) shows that the inverter modulation index (m_i) follows the reference under steady state conditions. Fig. 5.12(b) shows that the dc link current (i_{dc}) is minimized according to the load power requirements. Finally, Fig. 5.12(a) confirms the operation at near unity power factor.

5.4.5 Design Considerations

The design requires the choice of the input (L_r, C_r) and output (C_i) filters, the dc link inductor (L_{dc}), and the parameters of the controllers for the following loops: (a) speed (ω_m), (b) motor voltage ([v_l]), (c) inverter modulation index (m_i) and (d) dc link current (i_{dc}). The power topology and control strategy (except for the speed control loop) are similar to that presented in Chapter 4; therefore, their design is as presented in there. Finally, the speed controller is designed to be slower than the motor voltage controller (usually by a factor of 10) and according to the load requirements.

5.5 Experimental Results

The proposed control scheme was tested on a 3 kVA induction motor drive, with a phase controlled rectifier as a front end. Key waveforms are shown in Fig. 5.13 and Fig. 5.14 for two operating frequencies (30 and 60 Hz). Specifically, Fig. 5.13(a) & Fig. 5.14(a) show the motor line voltage (v_{ab}) and CSI line current (i_{oa}), Fig. 5.13(b) & Fig. 5.14(b) show the motor phase voltage (v_{pa}) and motor line current (i_{la}), Fig. 5.13(c) & Fig. 5.14(c) show the dc CSI voltage (v_i) and dc link current (i_{dc}), and Fig. 5.13(d) & Fig. 5.14(d) show the CSI line current spectrum (i_{ia}). Fig. 5.13(a) & Fig. 5.14 (a) show that the CSI line currents are PWM type and Fig. 5.13(d) & Fig. 5.14 (d) show that they have low

order harmonics at high frequencies (≅ 2.8 kHz). Therefore, the load voltages become almost sinusoidal waveforms (Fig. 5.13(a) & Fig. 5.14(a)) with the filtering action of the output capacitors. Fig. 5.13(d) & Fig. 5.14 (d) show that the SV technique produces the unwanted harmonics at fixed frequencies, which are independent of the motor frequency. Thus, there is no risk of resonances due to low frequency harmonics. Finally, Fig. 5.13(c) & Fig. 5.14(c) show that the dc current is minimized according to the load power (Fig. 5.13(c) shows a lower dc current level). The set-up and parameters values are given in APPENDIX A.4.

5.6 DISCUSSION AND CONCLUSIONS

The proposed CSI based ac induction motor drive topology exhibits the same high performance features as the corresponding VSI topology, both in terms of waveform quality and dynamic performance. In addition to the inherent advantages of the CSI topology (short-circuit protection, low output *dv/dt*, regeneration capabilities), the proposed supplemental CSI modulation index control highly improves the overall efficiency through the internal dc link current control, which minimizes the overall losses of the drive. The approach also achieves constant harmonic distortion of the motor voltage (5%); therefore, the motor efficiency is also improved. Moreover, the motor voltage loop provides an effective alternative to attenuate the load filter/motor resonances and the PWM-CSR ensures a high overall input power factor regardless of the load speed and torque.

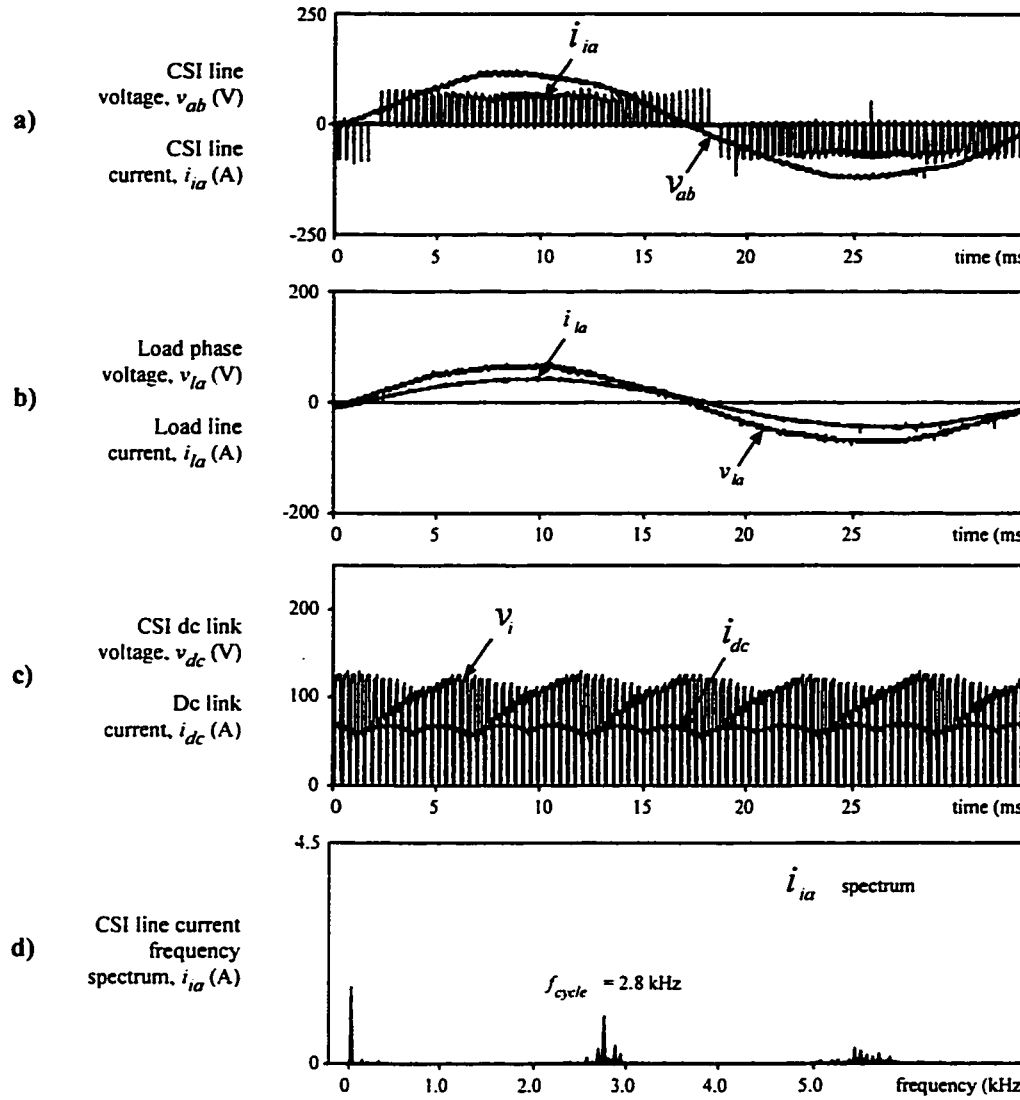

Fig. 5.13 Proposed CSI based ac drive, experimental waveforms at 30 Hz.

a) Motor line voltage (v_{ab}) and CSI current ($20 \cdot i_{ia}$). **b)** Motor phase voltage (v_{la}) and motor current ($20 \cdot i_{la}$). **c)** CSI dc voltage (v_i) and dc current ($20 \cdot i_{dc}$). **d)** Motor current spectrum (i_{la}).

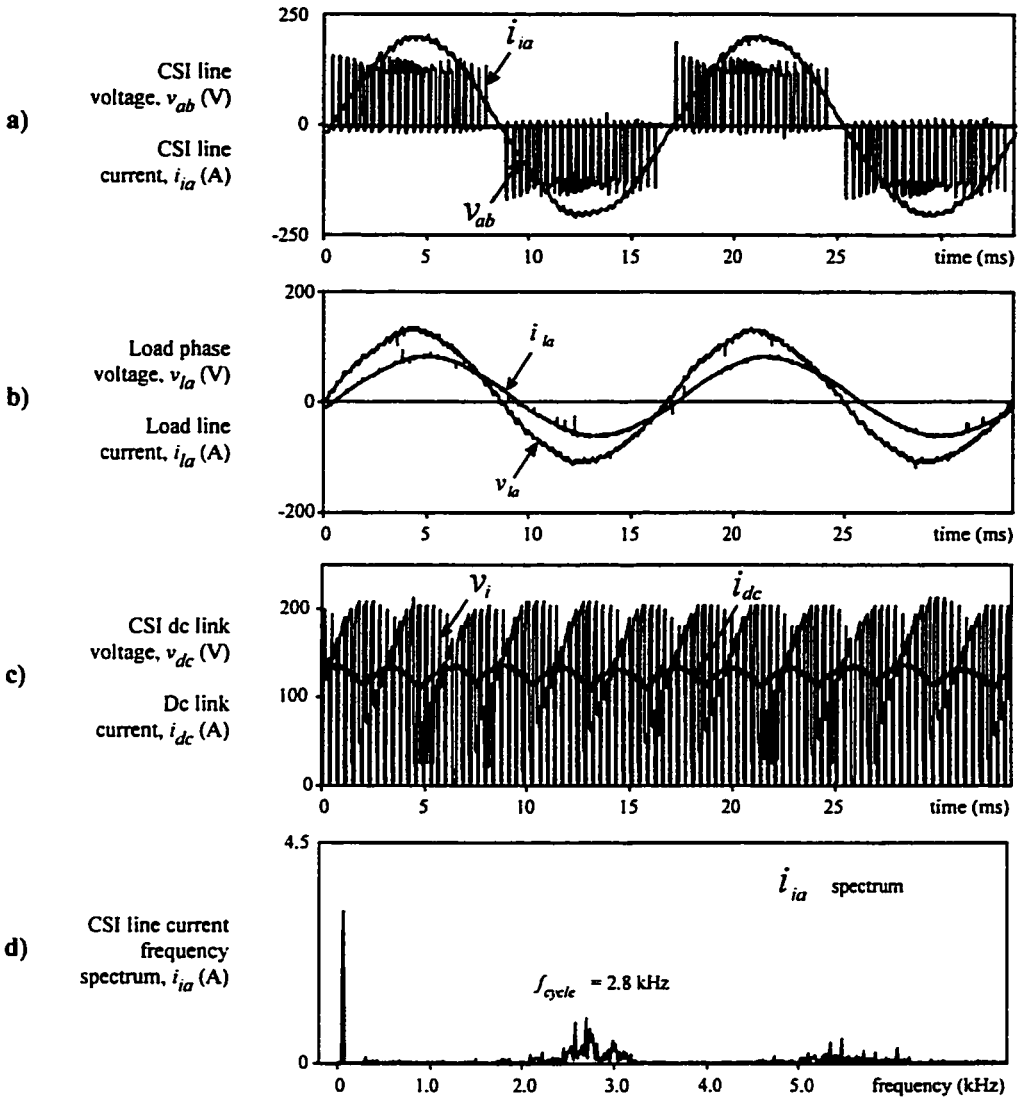

Fig. 5.14 Proposed CSI based ac drive, experimental waveforms at 60 Hz.

a) Motor line voltage (v_{ab}) and CSI current ($20 \cdot i_{ia}$). **b)** Motor phase voltage (v_{la}) and motor current ($20 \cdot i_{la}$). **c)** CSI dc voltage (v_i) and dc current ($20 \cdot i_{dc}$). **d)** Motor current spectrum (i_{la}).

CHAPTER 6

STATE VARIABLE DECOUPLING AND POWER FLOW CONTROL IN PWM-CSR

6.1 INTRODUCTION

PWM Current-Source Rectifiers (PWM-CSR) are gradually replacing the line commutated thyristor rectifiers as front-end ac/dc converter. In such rectifiers, a smoothing reactor is placed on the dc side and a *LC* filter has to be inserted on the ac side to provide a voltage bus and to reduce current harmonic injection into the distribution system resulting from the PWM operation. Direct interfacing with the ac mains often requires stringent specifications such as high input displacement factor (ideally ≈ 1) and low input current harmonic distortion (ideally ≈ 0).

In conventional schemes, the PWM-CSR has been operated with off-line patterns which result in a slow transient response, since the control strategies relies on changing the dc link current. On the other hand, the presence of the *LC* input filter causes a load dependent input displacement factor and may produce transient oscillations. Although oscillations can be attenuated by adding damping resistors, they reduce the overall conversion efficiency.

Recently, attempts have been made to operate the rectifier by means of on-line current control [77-81]. The main goals have been to keep a unity displacement factor, eliminate the damping resistors, regulate either the dc voltage or the dc current, and control independently the active and reactive power components. References [77-78]

propose solutions that meet the main requirements by using state variable feedback compensation in a static frame. However, [77] allows only unity power factor operation. On the other hand, [78] uses a small signal model that reduces the generality of the approach. Ref. [79] compensates the input displacement factor by using a linear approximation that is not accurate at light loads. Ref. [80] achieves near unity power factor; however, it presents low voltage utilization. Finally, [81] provides active damping; however, it is based on an approximation. The independent control on a continuous basis of the supply reactive and active powers has also been proposed [82]. However, due to the non-linear and coupled behavior of the converter, both quantities are not independently controlled.

A non-linear control strategy, based on state variable feedback linearization [83-85] is used in this chapter to introduce more flexibility in the control of the PWM-CSR and a more straight-forward approach to controller design. Specifically, it consists in linearizing the *dq* state variable model of the system, decoupling and controlling independently the direct (active power) and the quadrature (reactive power) line current components, and rejecting the effect of the supply voltage variations.

The strategy is entirely implemented on a digital system, hence, the SVM technique is used to generate the switching pattern. This results in the following improved features: (a) independent control of the active and reactive power, (b) inherent damping provided by the state variable feedback loop, (c) fast transient response (limited only by the sampling time), and (d) maximum supply voltage utilization of the rectifier.

The chapter includes the complete analysis and a design procedure of the

proposed control strategy. Experimental results on a 2 kVA DSP based laboratory prototype are also included to confirm the feasibility of the proposed control scheme.

6.2 DESCRIPTION OF THE POWER TOPOLOGY

The complete power circuit, shown in Fig. 6.1, is composed of a three phase PWM-CSR, a dc link reactor (L_{dc}), and a three phase second order input filter (L_r, C_r). The main function of the PWM-CSR is to regulate the level of the dc link current (i_{dc}), by adjusting the PWM-CSR dc link bus voltage (v_r). The harmonics injected into the ac mains by the PWM-CSR operation are absorbed by the *LC* input filter. The last component is the dc link reactor (L_{dc}), which smoothes the dc link current (i_{dc}) and therefore act as a current-source to the PWM-CSR. Fig. 6.1 also shows the set-up used to implement the control strategy.

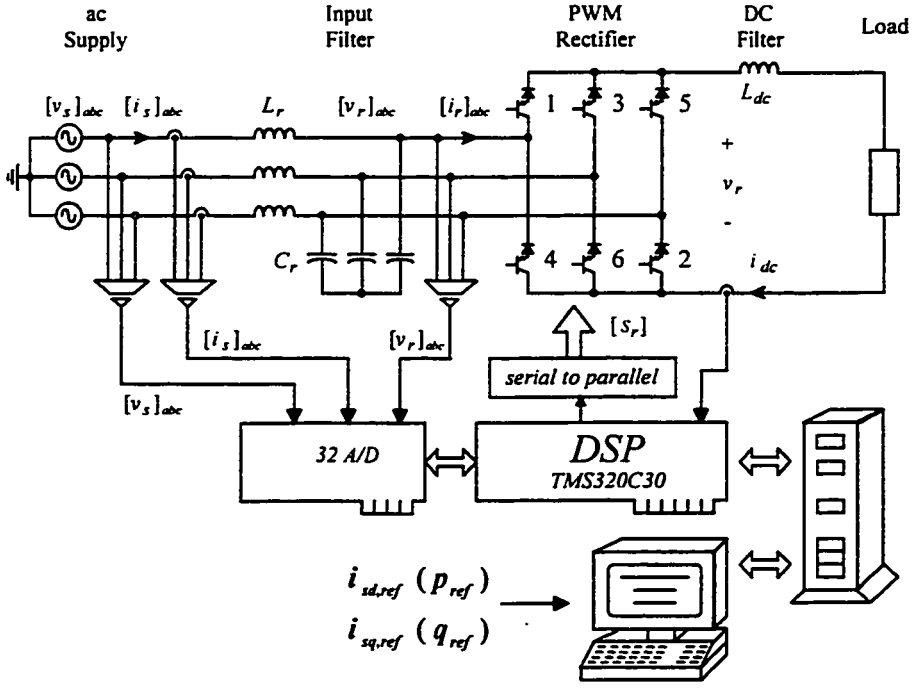

Fig. 6.1 PWM current-source rectifier power topology.

6.3 PROPOSED CONTROL STRATEGY

The gating signals are digitally generated using the Space Vector Modulating (SVM), technique presented in Chapter 3. This technique is preferred due to its high ac gain (equal to 1), reduced switching frequency (equal to one half of the cycle frequency) and straight-forward implementation in digital systems. Since the main objective is to control on a continuous basis the direct and quadrature line current for any load demand, it is necessary to on-line generate the modulating waveforms ($m_{r\beta}$, $m_{r\gamma}$), required by the SVM technique. To achieve this goal, the following control strategy is proposed.

6.3.1 Equivalent Model in the *abc* Frame

An equivalent single phase circuit for the ac supply, input filter and PWM-CSR, and the dc equivalent circuit are shown in Fig. 6.2. The dc voltage (v_r) and ac PWM-CSR line currents (i_{rk}, $k = a$, b, and phase c) are given by,

$$v_r = G_{ac} \sum_{k=a}^{c} m_{rk} \cdot v_{rk} \quad \text{V} \tag{6.1}$$

$$i_{rk} = G_{ac} \cdot m_{rk} \cdot i_{dc} \quad \text{A} \tag{6.2}$$

where, G_{ac} is ac gain of the PWM technique ($G_{ac} = 1$, for the SVM), and

m_{rk} are the modulating waveforms ($-1 \le m_{rk} \le 1$ to avoid overmodulation).

Each phase of the circuit is modeled by using the state variable approach and thereby, by using (6.1) and (6.2), the model of the system (Fig. 6.2) in the *abc* frame becomes.

$$\frac{d}{dt}[i_s]_{abc} = -\frac{1}{L_r}[v_r]_{abc} + \frac{1}{L_r}[v_s]_{abc} \quad \text{A/s} \tag{6.3}$$

$$\frac{d}{dt}[v_r]_{abc} = \frac{1}{C_r}[i_s]_{abc} - \frac{1}{C_r}G_{ac}[m_r]_{abc}\, i_{dc} \quad \text{V/s} \tag{6.4}$$

$$\frac{d}{dt}i_{dc} = \frac{1}{L_{dc}}G_{ac}[m_r]_{abc}^T[v_r]_{abc} - \frac{R_{dc}}{L_{dc}}i_{dc} \quad \text{A/s} \tag{6.5}$$

where, $[i_s]_{abc} = [i_{sa}\ i_{sb}\ i_{sc}]^T$, $[v_r]_{abc} = [v_{ra}\ v_{rb}\ v_{rc}]^T$, and i_{dc} are the state variables,

$[v_s]_{abc} = [v_{sa}\ v_{sb}\ v_{sc}]^T$ is the supply voltage vector (perturbation variables), and

$[m_r]_{abc} = [m_{ra}\ m_{rb}\ m_{rc}]^T$ is the modulating vector (input variables).

The *dq* transformation is valid during dynamic and steady state conditions [79]. In this work, the *dq* frame is preferred because all states variables become dc quantities in steady state. This feature will allow the use of standard controllers (such as PI and I type), to meet dynamic and steady state requirements (for instance, a given maximum overshoot and zero steady state error). It also facilitates the interface between the control outputs (*dq* rotating frame) and the SVM technique (α, β stationary frame).

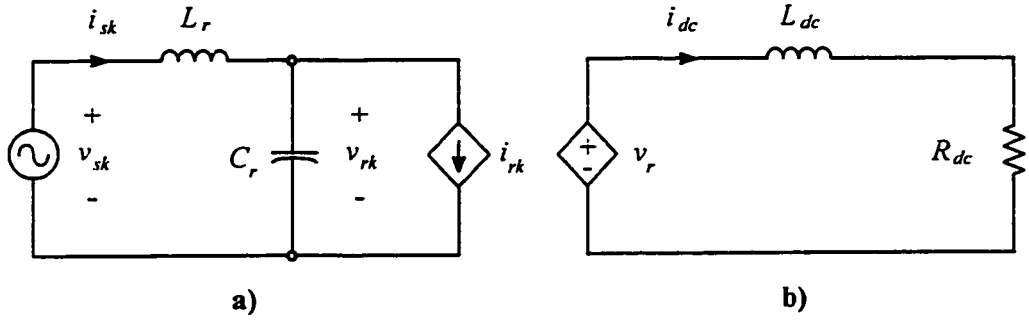

Fig. 6.2 PWM current-source rectifier model in the *abc* frame.

a) ac side (*k*: phase *a*, *b*, or *c*). **b)** dc side.

6.3.2 *dq* Frame Converter Model

In order to simplify the analysis, a balanced ac voltage supply is assumed;

therefore, the state variables have no zero sequence components. Thus, the *dq* transformation of the model in *abc* coordinates (6.3) to (6.5) yields,

$$\frac{d}{dt}[i_s]_{dq} + W[i_s]_{dq} = -\frac{1}{L_r}[v_r]_{dq} + \frac{1}{L_r}[v_s]_{dq} \quad \text{A/s} \tag{6.6}$$

$$\frac{d}{dt}[v_r]_{dq} + W[v_r]_{dq} = \frac{1}{C_r}[i_s]_{dq} - \frac{1}{C_r}G_{ac}[m_r]_{dq}\, i_{dc} \quad \text{V/s} \tag{6.7}$$

$$\frac{d}{dt}i_{dc} = \frac{3}{2}\frac{1}{L_{dc}}G_{ac}[m_r]_{dq}^T[v_r]_{dq} - \frac{R_{dc}}{L_{dc}}i_{dc} \quad \text{A/s} \tag{6.8}$$

where, $[v_s]_{dq} = [v_{sd}\ v_{sq}]^T$ (supply *dq* voltage vector)

$[i_s]_{dq} = [i_{sd}\ i_{sq}]^T$ (supply *dq* line current vector),

$[v_r]_{dq} = [v_{rd}\ v_{rq}]^T$ (capacitor *dq* voltage vector)

$[m_r]_{dq} = [m_{rd}\ m_{rq}]^T$ (input *dq* vector),

$W = \begin{bmatrix} 0 & -\omega_s \\ \omega_s & 0 \end{bmatrix}$, and ω_s : supply angular frequency ($\omega_s = 2\pi f_s$).

By expanding the *dq* model (6.6) to (6.8) into its components yields,

$$\frac{d}{dt}i_{sd} = \omega_s\, i_{sq} - \frac{1}{L_r}v_{rd} + \frac{1}{L_r}v_{sd} \quad \text{A/s} \tag{6.9}$$

$$\frac{d}{dt}i_{sq} = -\omega_s\, i_{sd} - \frac{1}{L_r}v_{rq} + \frac{1}{L_r}v_{sq} \quad \text{A/s} \tag{6.10}$$

$$\frac{d}{dt}v_{rd} = \omega_s\, v_{rq} + \frac{1}{C_r}i_{sd} - \frac{1}{C_r}G_{ac}\, i_{dc}\, m_{rd} \quad \text{V/s} \tag{6.11}$$

$$\frac{d}{dt}v_{rq} = -\omega_s\, v_{rd} + \frac{1}{C_r}i_{sq} - \frac{1}{C_r}G_{ac}\, i_{dc}\, m_{rq} \quad \text{V/s} \tag{6.12}$$

$$\frac{d}{dt}i_{dc} = \frac{3}{2}\frac{1}{L_{dc}}G_{ac}(m_{rd}v_{rd} + m_{rq}v_{rq}) - \frac{R_{dc}}{L_{dc}}i_{dc} \quad \text{A/s} \tag{6.13}$$

The resulting model (6.9) to (6.13) represents a multiple-input multiple-output (MIMO) type of system. The inputs are the modulating variables (m_{rd}, m_{rq}), and the outputs are the quadrature (i_{sq}, reactive power) and the direct (i_{sd}, active power) component of the supply current. Noting that unity displacement factor is a special case (when $i_{sq} = 0$, for a rotating frame synchronized with the ac supply voltage) and that the rectifier performs as a current-source with a value equal to i_{dc}.

Also, the *dq* model of the PWM-CSR (6.9) to (6.13) shows a non-linear system ((6.11)-(6.13) contain multiplications of the input variables and the state variables), and a coupled system (for instance, (6.13) shows that the dc current depends upon both input variables). Therefore, to achieve full linearization and decoupling, it is proposed to use an input-output linearization method [83].

6.3.3 Linearization and Decoupling of the *dq* Model

The method [83] establishes to differentiate the outputs variables as many times as necessary until one or more input variables appear explicitly. If i_{sd} is differentiated once, (6.9) is obtained, which does not contain any input, therefore, it is differentiated again, and by using (6.10) and (6.11) yields,

$$\frac{d^2}{dt^2} i_{sd} = -i_{sd}(\omega_s^2 + \omega_{rr}^2) - \frac{2\omega_s}{L_r} v_{rq} + \frac{\omega_s}{L_r} v_{sq} + \omega_{rr}^2 G_{ac} i_{dc} m_{rd} + \frac{1}{L_r} \frac{d}{dt} v_{sd} \quad \text{A/s}^2 \quad (6.14)$$

where, $\omega_{rr} = 1/\sqrt{C_r L_r}$ is the resonant angular frequency of the input filter.

Eq. (6.14) contains the input m_d, therefore the differentiation process applied to i_{sd} stops here. The same procedure is applied to i_{sq} which yields,

$$\frac{d^2}{dt^2}i_{sq} = -i_{sq}(\omega_s^2 + \omega_{rr}^2) + \frac{2\omega_s}{L_r}v_{rd} - \frac{\omega_s}{L_r}v_{sd} + \omega_{rr}^2 G_{ac} i_{dc} m_{rq} + \frac{1}{L_r}\frac{d}{dt}v_{sq} \quad \text{A/s}^2 \quad (6.15)$$

Eq. (6.14) and (6.15) can be written in a matrix format as:

$$\mathbf{X} = \mathbf{A} \cdot [m_r]_{dq} + \mathbf{B} \quad (6.16)$$

where, $\mathbf{X} = \begin{bmatrix} \frac{d^2}{dt^2}i_{sd} & \frac{d^2}{dt^2}i_{sq} \end{bmatrix}^T$

$$\mathbf{A} = G_{ac}\omega_{rr}^2 i_{dc}$$

$$\mathbf{B} = \begin{bmatrix} -i_{sd}(\omega_s^2 + \omega_{rr}^2) - \frac{2\omega_s}{L_r}v_{rq} + \frac{\omega_s}{L_r}v_{sq} + \frac{1}{L_r}\frac{d}{dt}v_{sd} \\ -i_{sq}(\omega_s^2 + \omega_{rr}^2) + \frac{2\omega_s}{L_r}v_{rd} - \frac{\omega_s}{L_r}v_{sd} + \frac{1}{L_r}\frac{d}{dt}v_{sq} \end{bmatrix}$$

The input-output linearization method proposes to restrict **X** to be of the linear and decoupled form:

$$\mathbf{X} = \mathbf{D} \cdot [u_r]_{dq} + \mathbf{F} \quad (6.17)$$

where, **D** and **F** are conveniently defined as:

$$\mathbf{D} = k_2, \quad \mathbf{F} = \begin{bmatrix} -k_1\frac{d}{dt}i_{sd} - k_2 i_{sd} \\ -k_1\frac{d}{dt}i_{sq} - k_2 i_{sq} \end{bmatrix} = \begin{bmatrix} -k_1\omega_s i_{sq} + \frac{k_1}{L_r}v_{rd} - \frac{k_1}{L_r}v_{sd} - k_2 i_{sd} \\ k_1\omega_s i_{sd} + \frac{k_1}{L_r}v_{rq} - \frac{k_1}{L_r}v_{sq} - k_2 i_{sq} \end{bmatrix}$$

also,

$[u_r]_{dq}$: new *dq* set of input variables, and

k_1, k_2: arbitrary positive gains used for pole placement.

The existence of the linear and decoupled form (6.17) is conditioned to the existence of the *input transformation* ($[m_r]_{dq}$ as function of $[u_r]_{dq}$, (6.18)). Thus, by replacing (6.16) in (6.17), the expression of the *input transformation* becomes,

$$[m_r]_{dq} = \mathbf{A}^{-1} \cdot (\mathbf{D}[u_r]_{dq} + \mathbf{F} - \mathbf{B})$$

$$= \underbrace{\frac{1}{G_{ac}\omega_{rr}^2 i_{dc}}}_{\text{linearization}} \left\{ \begin{array}{l} k_2 \begin{bmatrix} u_{rd} \\ u_{rq} \end{bmatrix} + \underbrace{\begin{bmatrix} -k_1 \frac{d}{dt} i_{sd} - k_2 i_{sd} \\ -k_1 \frac{d}{dt} i_{sq} - k_2 i_{sq} \end{bmatrix}}_{\text{damping}} - \\ \underbrace{\begin{bmatrix} -i_{sd}(\omega_s^2 + \omega_{rr}^2) - \frac{2\omega_s}{L_r} v_{rq} \\ -i_{sq}(\omega_s^2 + \omega_{rr}^2) + \frac{2\omega_s}{L_r} v_{rd} \end{bmatrix}}_{\text{decoupling}} \underbrace{\begin{bmatrix} +\frac{\omega}{L_r} v_{sq} + \frac{1}{L_r}\frac{d}{dt} v_{sd} \\ -\frac{\omega}{L_r} v_{sd} + \frac{1}{L_r}\frac{d}{dt} v_{sq} \end{bmatrix}}_{\text{voltage rejection}} \end{array} \right\} \quad (6.18)$$

The expression for the modulating vector (6.18) shows one possible singularity ($i_{dc} = 0$), where the *input transformation* is not defined and thereby, the method cannot be applied. However, although $i_{dc} = 0$ could be achieved during transient conditions, it is not a normal operation mode. In practical applications, when the sampled variable i_{dc} is lower than a given value, it is restricted to a minimum. Equation (6.18) also shows the different terms that contribute to the linearization, damping, decoupling, and rejection of supply voltage variations.

On the other hand, the actual implementation of (6.18) requires the differential of the *d* and *q* component of the supply voltages. In practice, the supply voltages are noisy, therefore, they are filtered by means of analog filters (cut-off frequency of about 10 kHz), then sampled, and finally numerically differentiated in the DSP. Note that **F** in (6.18) can be implemented using the sampled state variables (6.17) and thereby, the differential of the supply line currents are not required.

Thus, the direct and quadrature line current can be controlled independently by

means of u_{rd} and u_{rq} respectively and at fixed dynamic in the PWM-CSR operating region.

6.3.4 Dynamic Response Enhancement

Since (6.17) is linear, the Laplace Transform is used to continue the analysis and design. Thus, the model (6.17) can be expanded and written as follows,

$$\frac{i_{sd}(s)}{u_{rd}(s)} = \frac{i_{sq}(s)}{u_{rq}(s)} = \frac{k_2}{s^2 + s k_1 + k_2} \quad \text{A} \tag{6.19}$$

where, $i_{sd}(s)$, $i_{sq}(s)$, $i_{sd.ref}(s)$, and $i_{sq.ref}(s)$ are the Laplace Transforms of i_{sd}, i_{sq}, $i_{sd.ref}$, and $i_{sq.ref}$, respectively.

The Laplace Transform of the model (6.19) shows that zero steady state error in both current loops should be expected. This is valid as long as the *input transformation* (6.18), is computed accurately. However, since it assumes knowing the exact value L_r and C_r, which are usually only available as approximations, zero steady state error is not totally ensured. In order to achieve it, it is proposed to add two external integrators to force zero steady state error, even under inaccurate values of C_r and L_r.

Therefore, by adding a feedback loop with an integrator ($1/sT_{ac}$), the direct and quadrature line current closed loop transfer functions become (Fig. 6.3):

$$\frac{i_{sd}(s)}{i_{sd.ref}(s)} = \frac{i_{sq}(s)}{i_{sq.ref}(s)} = \frac{k_2 / t_{ac}}{s^3 + s^2 k_1 + s k_2 + k_2 / t_{ac}} \quad \text{A/A} \tag{6.20}$$

If (6.20) is restricted to be of the optimum third order transfer form, based on the ITAE criterion, the coefficients k_1, k_2, and t_{ac} can be found for a given settling time ($t_{s.ac}$).

Thus, for a 2% band,

$$k_1 = 1.75\frac{7.54}{t_{s,ac}}, \quad k_2 = 2.15\left(\frac{7.54}{t_{s,ac}}\right)^2, \quad t_{ac} = 2.15\frac{t_{s,ac}}{7.54} \tag{6.21}$$

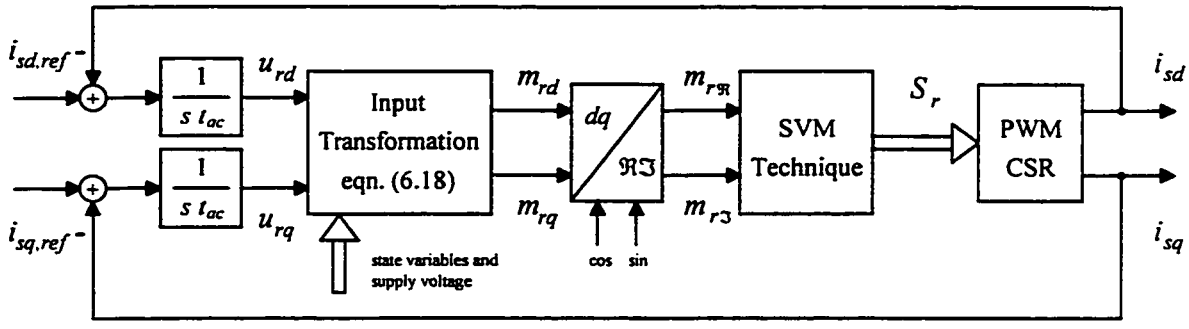

Fig. 6.3 Proposed control strategy scheme (linearization and decoupling).

6.4 PWM-CSR OPERATING REGION

The power topology and control strategy restrict the maximum and minimum steady state values of the state variables and thereby, the limits for the set-point references. For instance, due to the nature of the power circuit topology, the dc current (i_{dc}) is always positive; also, it will be shown that the quadrature line current (i_{sq}) range depends upon the actual dc current. Thus, to avoid setting the converter on an unachievable operating point, the operating region of the PWM-CSR is derived.

In order to find the operating region, the *dq* model of the converter (6.9) to (6.13) is set equal to zero and then solved systematically. The resulting set of variables are dc quantities and they are designated by capital letters. Assuming the *dq* transformation is synchronized with the supply voltage, the resulting normalized expressions as a function

of the inputs (M_{rd}, M_{rq}) are as follows,

$$I_{dc} = G_{ac} M_{rd} \frac{f_m^2}{f_m^2 - 1} \quad \text{A pu} \tag{6.22}$$

$$I_{sq} = \frac{(G_{ac} M_{rd} M_{rq} X_{Cr} f_m^2 + f_m^2 - 1) f_m^2}{X_{Cr} (f_m - 1)^2 (f_m + 1)^2} \quad \text{A pu} \tag{6.23}$$

$$I_{sd} = G_{ac}^2 \frac{f_m^4}{(f_m - 1)^2 (f_m + 1)^2} (M_{rd})^2 \quad \text{A pu} \tag{6.24}$$

$$V_{rq} = -G_{ac}^2 X_{Cr} \frac{f_m^2}{(f_m - 1)^2 (f_m + 1)^2} (M_{rd})^2 \quad \text{V pu} \tag{6.25}$$

$$V_{rd} = \frac{(G_{ac} M_{rd} M_{rq} X_{Cr} + f_m^2 - 1) f_m^2}{X_{Cr} (f_m - 1)^2 (f_m + 1)^2} \quad \text{V pu} \tag{6.26}$$

where, $f_m = \omega_r / \omega_s$, $V_{base} = V_{sd}$, $I_{base} = 3V_{sd} / (2R_{dc})$, and X_{Cr} is the pu capacitor reactance of the input filter

The inputs M_{rd} and M_{rq} are bounded. This comes from the fact that in order to inject line currents ($[i_r]_{abc}$, Fig. 6.1) without distortion, the modulating vector (m_{rq}, m_{rd}, Fig. 6.3) must have a magnitude lower than or equal to one. On the other hand, since the power topology can only provide positive dc currents, the operating region is defined by the following boundary conditions,

$$0 \le M_{rd} \le 1, \quad -1 \le M_{rq} \le 1 \tag{6.27}$$

A graphical interpretation for the operating region is given in Fig. 6.4. From Fig. 6.4, and (6.22) to (6.26) it can be concluded that,

- The range of the quadrature line current is restricted by the actual value of the dc current (Fig. 6.4).

- The maximum dc current (6.22) is proportional to the ac gain of the modulating technique (G_{ac}) and a function of the resonant frequency of the input filter (f_{ri}).
- The maximum range for the quadrature line current (Fig. 6.4) is given when M_{rd} = 0.707 (6.22).
- The maximum quadrature line current (6.23) is given when $M_{rd} = M_{rq} = 0.707$ (Fig. 6.4).

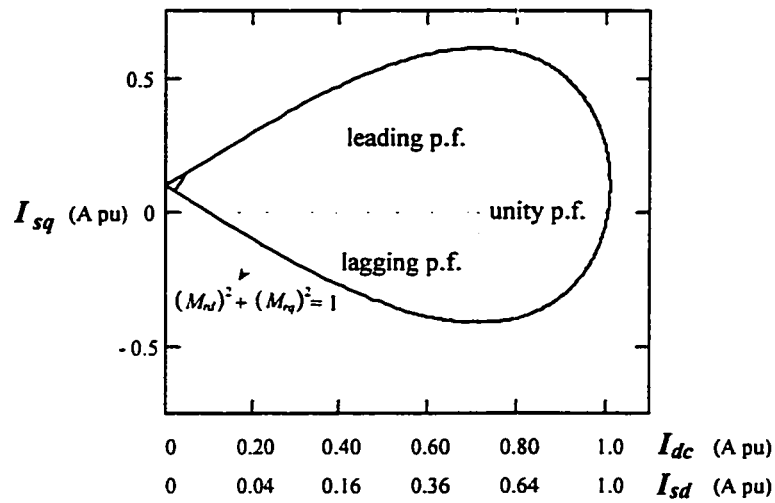

Fig. 6.4 Graphical representation of the operating region of the PWM-CSR.

C_r = 50 μF, L_r = 3 mH, R_{dc} = 20 Ω, and G_{ac} = 1, dc (I_{dc}) versus quadrature line current (I_{sq}).

6.5 EXPERIMENTAL RESULTS

6.5.1 Power Topology and Control Scheme Description

The power topology and proposed control strategy have been implemented on a 2 kVA laboratory prototype unit to verify feasibility (Fig. 6.1). A digital system based on the TMS320C30 DSP microprocessor has been used to implement the control strategy. The digital system uses a 32 A/D board to sample the required state variables. The main

board executes the control algorithm and also performs other tasks such as an on-line communication with an user interface, which runs on a PC platform. Thus, the references and controller parameters can be externally on-line entered and/or modified to perform transient and/or static tests. The gating signals are sent to the drivers through the serial port of the DSP microprocessor. Although the shorting paths of the gating signals are ensured by the SVM algorithm, overlaps (≈ 5 μs) are added at the serial to parallel stage.

6.5.2 Filter Components and Controller Parameters Design

The minimum sample time in this set-up is 185 μs. Therefore, a cycle frequency of 5040 Hz (cycle period of 198 μs) is chosen. Both d and q line current controllers are designed to achieve a 5 ms settling time ($t_{s,ac} = 5$ ms). Thus, by using (6.21), $k_1 = 2.639$ k, $k_2 = 4.892$ M, and $T_{ac} = 1.425$ ms.

The selection of L_{dc}, C_r, and L_r is done by following the design guidelines provided in APPENDIX C.3. APPENDIX A.5 shows the experimental set-up and parameter values, which are calculated following the design guidelines provided in APPENDIX C.3.

6.5.3 Experimental Waveforms

Unity displacement power factor is achieved by setting $i_{sq.ref} = 0$ and $i_{sd.ref} = 4$ A (Fig. 6.5). The supply line current (i_{sa}) is in phase with the phase voltage (Fig. 6.5(a)). However, a small distortion is observed in the line current (< 3%) which results in a input power factor equal to 0.972. The dc voltage (v_r) is of the PWM type (Fig. 6.5(b)) based on the SVM. Thus, the distortion introduced on the load and supply system is minimized. Both actual d and q current components are equal to the references; therefore, steady state

error is zero and unity displacement factor is achieved (Fig. 6.5(c)).

Leading displacement power factor is obtained by setting $i_{sq.ref} = 3$ A and $i_{sd.ref} = 4$ A (Fig. 6.6). The input line current (i_{sa}) is leading the supply phase voltage by approximately 36° (Fig. 6.6 (a)). The overall input power factor was 0.795 capacitive.

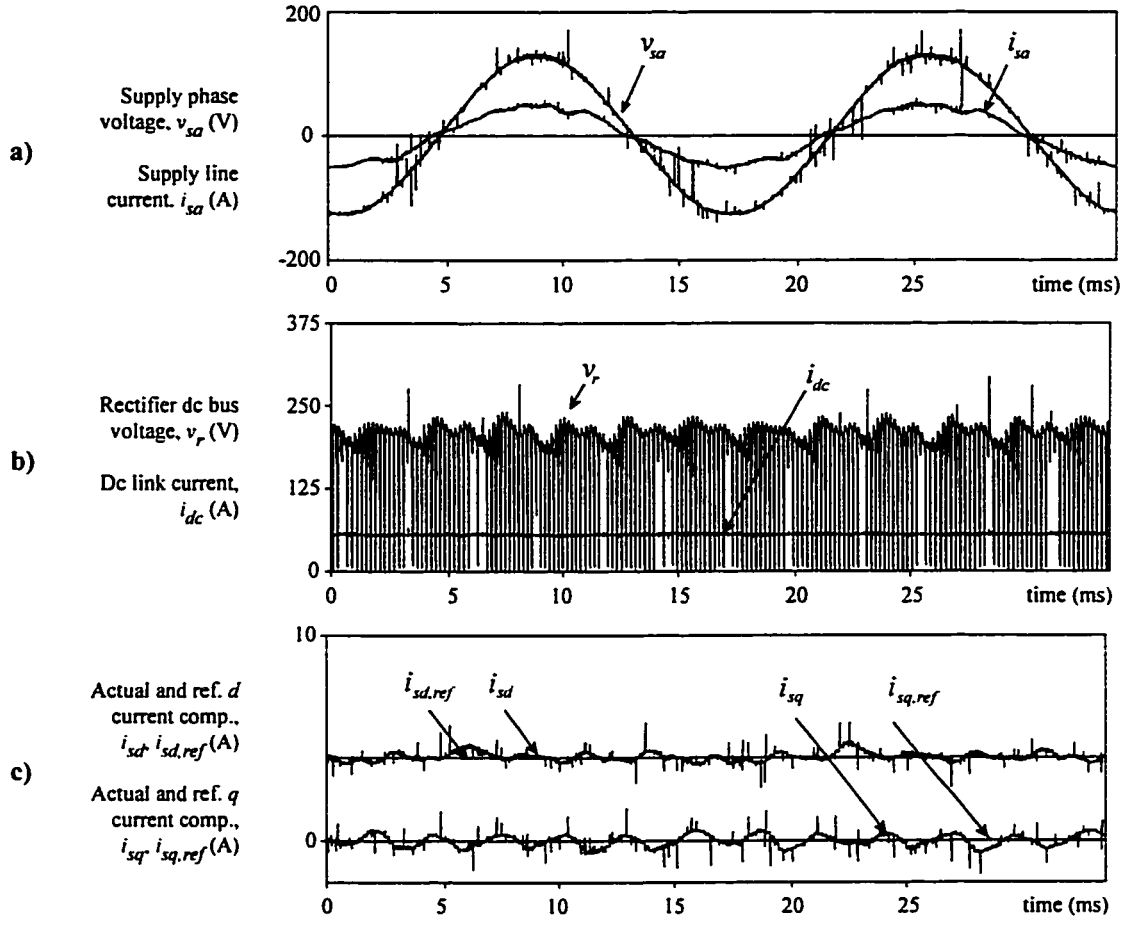

Fig. 6.5 Unity displacement power factor operating mode.

Experimental waveforms. (**a**) Supply voltage (v_{sa}) and current ($10 \cdot i_{sa}$). (**b**) CSR dc bus voltage (v_r) and dc link bus current ($10 \cdot i_{dc}$). (**c**) q and d line current references ($i_{sq.ref}$, $i_{sd.ref}$) and q and d actual currents (i_{sq}, i_{sd}).

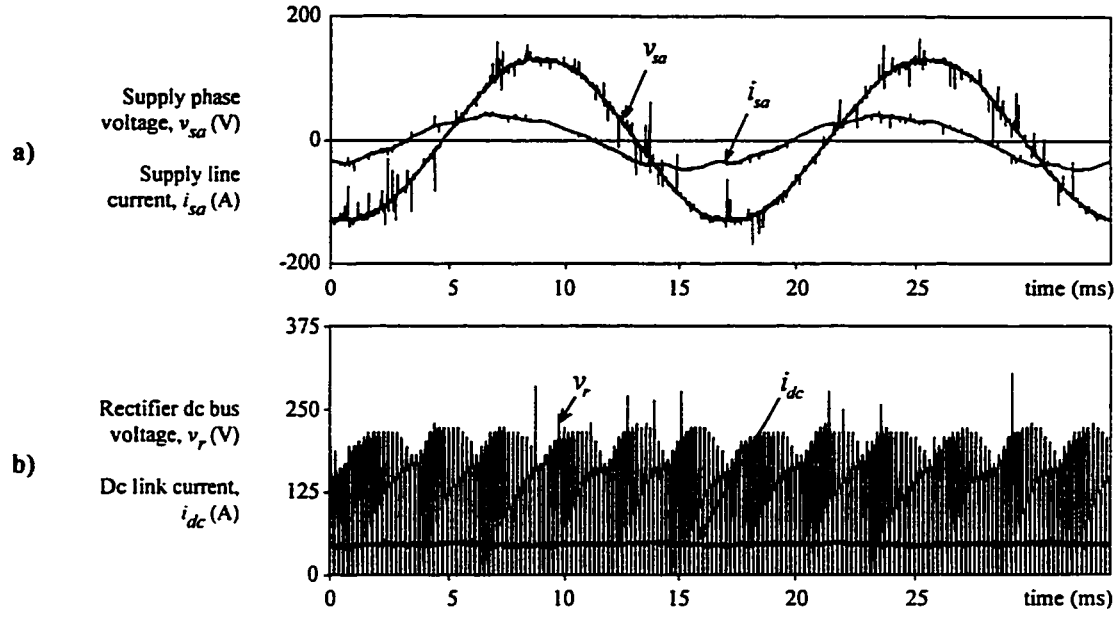

Fig. 6.6 Leading displacement power factor operating mode.

Experimental waveforms. (**a**) Supply phase voltage (v_{sa}) and supply current ($10 \cdot i_{sa}$). (**b**) CSR dc bus voltage (v_r) and dc link bus current ($10 \cdot i_{dc}$).

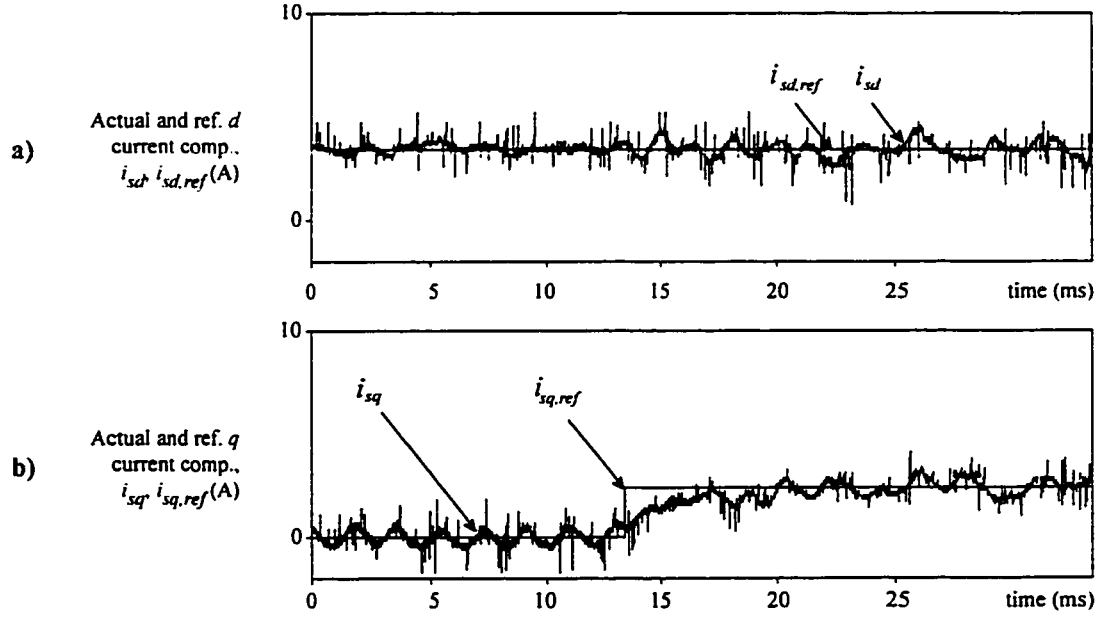

Fig. 6.7 Transient response, unity to leading displacement power factor.

Experimental waveforms. (**a**) d reference ($i_{sd,ref}$) and d actual line current (i_{sd}). (**b**) q reference ($i_{sq,ref}$) and q actual line current (i_{sq}).

Finally, a step increase in $i_{sq.ref}$ at t = 13 ms (from 0 to 3 A), while $i_{sd.ref}$ is set at 4 A, illustrates key dynamic features. Fig. 6.7 shows the d and q line current references and actual values. It can be seen that the d component is not modified during the transient (Fig. 6.7(a)). This confirms the decoupling and independent control of the active and reactive power. The settling time is found to be approximately 5 ms (Fig. 6.7(b)), which confirms the validity of the design guidelines of the line current component controllers. The results all indicate that the damping resistors on the input filter are no longer necessary. The required damping is supplied by the state variable feedback compensation. Similar tests were done for different operations point and all showed similar transient responses, which confirms fully linearization.

6.6 DISCUSSION AND CONCLUSIONS

The more straight-forward on-line control of a CSR is to regulate the ac line currents directly in the stationary *abc* frame. This chapter demonstrates the superiority of the proposed control technique which features: (a) control in a rotating *dq* frame; (b) a decoupling between d and q components, and (c) the use of a transformation to linearize the model. Furthermore, the use of DSP hardware and software greatly simplifies the realization of the proposed control technique. It also allows integration of control and PWM pattern generation. Results on a 2 kVA prototype indicate: (a) complete and accurate displacement power factor control; (b) fast, accurate and independent control of the d and q components; and (c) low input current harmonic distortion.

CHAPTER 7

CONTROL OF PWM-CSR IN THE REGENERATION MODE

7.1 INTRODUCTION

Several publications have analyzed the non-linear and coupled model of the PWM current-source rectifier (PWM-CSR) feeding a passive load. Ref. [45] applies a state variable feedback strategy to control independently the quadrature supply current component and the dc current. Ref. [87] proposes a scheme using a cascade structure where the inner loop is the d and q supply current components. However, both analysis and controller design are based on a small signal model and as the actual operating point moves away from the nominal one, the performance deteriorates, specially in terms of dynamic response.

Ref. [89] analyses the power configuration for a connection to an active load. It provides design guidelines when a P-type controller is used. The experimental results confirm the validity of the analysis; however, since the dc side behaves as a first order system, a P-type controller does not provide the fastest response. Thus, a higher order controller would be desirable; however, the method presented to identify the stable regions becomes involved.

Conversely, non-linear control techniques and specifically, *input-output linearization* based on *state variable feedback linearization*, have been successfully applied in power electronics topologies [84-85]. This technique has demonstrated the

main advantages of linearization and decoupling, characteristics highly desirable in systems including most of the power topologies. Ref. [84] applies this technique to a dc-dc buck-boost converter and clearly shows the importance of the appropriate selection of the controllable variables in order to ensure acceptable internal dynamics. Ref. [85] applies this technique to a three phase PWM voltage-source rectifier (PWM-VSR). Superiority over linear control is clearly demonstrated; however, the total dynamic response remains load dependent. Chapter 6 of this thesis applies the non-linear control technique to the three phase PWM current-source rectifier (PWM-CSR). Experimental results show that it is possible to control independently the d and q supply current components (decoupling feature), which allows operation with either unity, leading, or lagging displacement power factor without affecting the load power demand. Also, due to full linearization, it is possible to obtain an enhanced dynamic response and independence of the operating point.

A non-linear control strategy, based on the instantaneous load power demand feedforward, is used in this chapter to obtain a stable dc current link controller. This results in the following improved features: (a) a fast and stable dc current dynamic response independent of the operating point and operating mode (rectification or regeneration) and (b) a stable operating mode independent of the type of load (active or passive). The complete analysis and design procedure of the proposed control strategy are presented. Simulated results are also included to confirm the feasibility of the proposed control scheme.

7.2 POWER TOPOLOGY AND LOAD MODELING

The complete power circuit topology is shown in Fig. 7.1. A complete description of the function of each component is given in the previous chapter. The design guidelines of the dc link inductor (L_{dc}) and second order input filter (L_r, C_r), are included in the APPENDIX C.3.

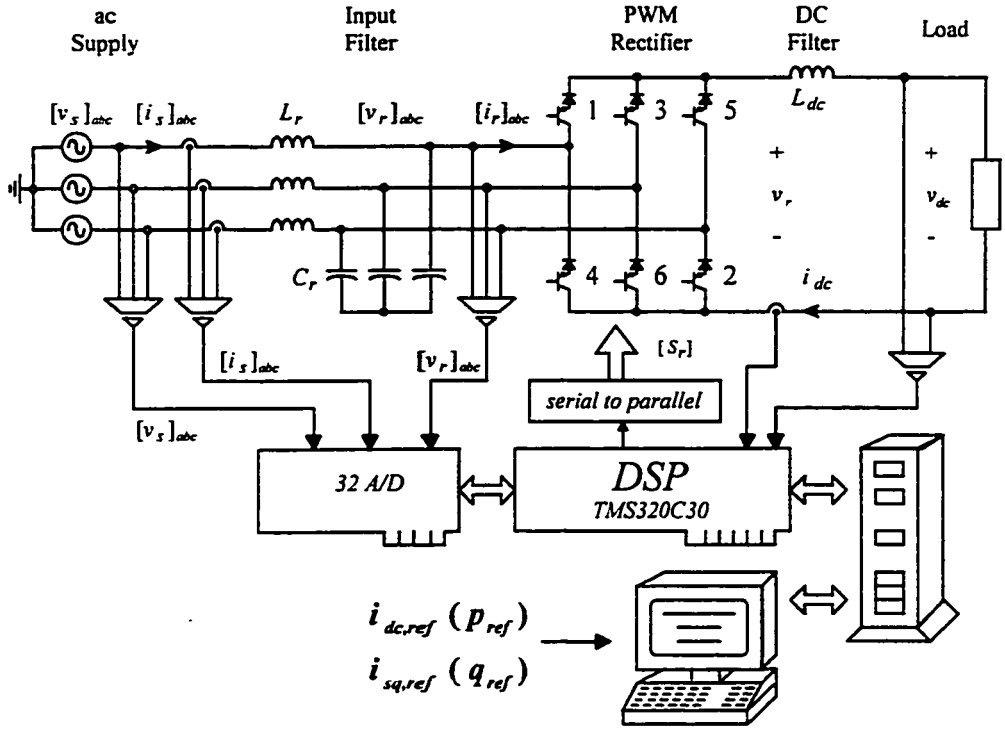

Fig. 7.1 PWM current-source rectifier power topology.

Two different load models are studied (Fig. 7.2): (a) a pure resistor (R_{dc}) to model passive loads and (b) a small resistor (R_{dc}) in series with a dc voltage supply (v_{dc}) to model active loads (i.e., a CSI fed induction motor drive [88] or a dc motor drive). Note that the regeneration mode can be modeled by reversing the polarity of the dc voltage supply, Fig. 7.2(b).

7.3 ANALYSIS OF STABILITY AS A FUNCTION OF THE LOAD TYPE

The stability of the dc link current loop is investigated by analyzing the small signal model of the converter. In order to get an expression that relates the output variable (dc link current, i_{dc}) with the input variables (supply line currents, $[i_s]_{abc}$), an instantaneous power balance is applied. The PWM rectifier (Fig. 7.1) is assumed lossless for analysis purposes; therefore, the instantaneous ac power equals the instantaneous dc power. Thus,

$$[v_r]_{abc}^T \left\{ [i_s]_{abc} - C_r \frac{d}{dt} [v_r]_{abc} \right\} = v_r i_{dc} \quad \text{W} \tag{7.1}$$

where, $[v_r]_{abc}$: input capacitor voltages (*abc* frame)

$[i_s]_{abc}$: supply line currents (*abc* frame)

v_r : dc bus rectifier voltage

i_{dc} : dc link current

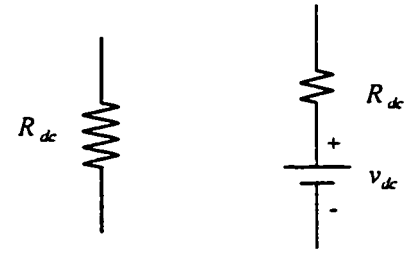

Fig. 7.2 PWM-CSR load models.

a) Passive load. **b)** Active load.

Simulated and experimental tests have shown that the variation of voltage across the input filter capacitor is negligible and therefore, the instantaneous power expression (7.1) in a *dq* frame [86] yields for a passive load (Fig. 7.2(a)),

$$\frac{3}{2}(v_{rd}i_{sd} + v_{rq}i_{sq}) = L_{dc}i_{dc}\frac{d}{dt}i_{dc} + R_{dc}i_{dc}^2 \quad \text{W} \tag{7.2}$$

and for an active load Fig. 7.2(b),

$$\frac{3}{2}(v_{rd}i_{sd} + v_{rq}i_{sq}) = L_{dc}i_{dc}\frac{d}{dt}i_{dc} + R_{dc}i_{dc}^2 + v_{dc}i_{dc} \quad \text{W} \tag{7.3}$$

where, $[v_r]_{dq} = [v_{rd}\ v_{rq}]$: input capacitor voltages (dq frame)

$[i_s]_{dq} = [i_{rd}\ i_{rq}]$: supply line currents (dq frame)

The internal ac line current controllers introduced in Chapter 6 are used as the inner loops of the dc link current loop. Thus, both d and q components of the line current (i_{sd} and i_{sq}) follow their respective references with zero steady state error and fast dynamic response. In practice the dc current loop is slower than the ac line current loops; therefore, they can be considered equal to their respective references ($i_{sd,ref}$ and $i_{sq,ref}$) for analysis purposes. Thus, the instantaneous power expressions (7.2) and (7.3) can be written as,

$$\frac{3}{2}(v_{rd}i_{sd,ref} + v_{rq}i_{sq,ref}) = L_{dc}i_{dc}\frac{d}{dt}i_{dc} + R_{dc}i_{dc}^2 \quad \text{W} \tag{7.4}$$

and,

$$\frac{3}{2}(v_{rd}i_{sd,ref} + v_{rq}i_{sq,ref}) = L_{dc}i_{dc}\frac{d}{dt}i_{dc} + R_{dc}i_{dc}^2 + v_{dc}i_{dc} \quad \text{W} \tag{7.5}$$

The above expressions clearly show that the dc link current can be controlled by manipulating $i_{sd,ref}$ and/or $i_{sq,ref}$. However, since unity displacement power factor ($i_{sq,ref} = 0$) is desirable for any load demand, the q component of the line currents cannot be used to control the dc current. Instead, $i_{sd,ref}$ becomes the input to control i_{dc}.

7.3.1 Small Signal Model for a Passive Load

The model for a passive load (7.4) is linearized around an operating point and $i_{sq,ref}$ = 0 is assumed. The resulting transfer function for $I_{dc} \neq 0$ is given by,

$$\frac{i_{dc}(s)}{i_{sd,ref}(s)} = \frac{3}{4}\frac{V_{rd}}{I_{dc}R_{dc}}\frac{1}{\frac{L_{dc}}{2R_{dc}}s+1} \quad \text{A/A} \tag{7.6}$$

where, V_{rd} : input capacitor voltage at a given operating point, *d* component

I_{dc} : dc link current at a given operating point

The open loop transfer function for a passive load (7.6) shows one pole located at $-L_{dc}/(2R_{dc})$ which is always in the left hand side of the *s* plane. Therefore, a standard P or PI controller in a feedback scheme will provide a stable closed loop operation. However, since the transfer function depends upon the dc link current, a variable dynamic performance can also be expected.

7.3.2 Small Signal Model for an Active Load

The model for an active load (7.5) is linearized around an operating point and $i_{sq,ref}$ = 0 is assumed. The resulting transfer function is given by,

$$\frac{i_{dc}(s)}{i_{sd,ref}(s)} = \frac{3}{2}\frac{V_{rd}}{2I_{dc}R_{dc}+V_{dc}}\frac{1}{\frac{L_{dc}I_{dc}}{2R_{dc}I_{dc}+V_{dc}}s+1} \quad \text{A/A} \tag{7.7}$$

where, V_{dc} : load dc voltage at a given operating point

The open loop transfer function for an active load (7.7) shows a first order system with the pole located at $-I_{dc}L_{dc}/(2R_{dc}I_{dc} + V_{dc})$. In most applications R_{dc} is negligible (for

instance, R_{dc} is the armature resistance in a dc drive). Thus, when V_{dc} is negative (regenerative power load mode) the open loop pole is located in the right hand side of the s plane. Therefore, if a standard P or PI controller is used to control the dc link, an unstable closed loop operation can be achieved. Moreover, and regardless of the stability issue, the overall dynamic performance becomes load dependent. The control scheme that uses the above approach (PI controller) is presented in Fig. 7.3 and simulation waveforms are depicted in Fig. 7.4.

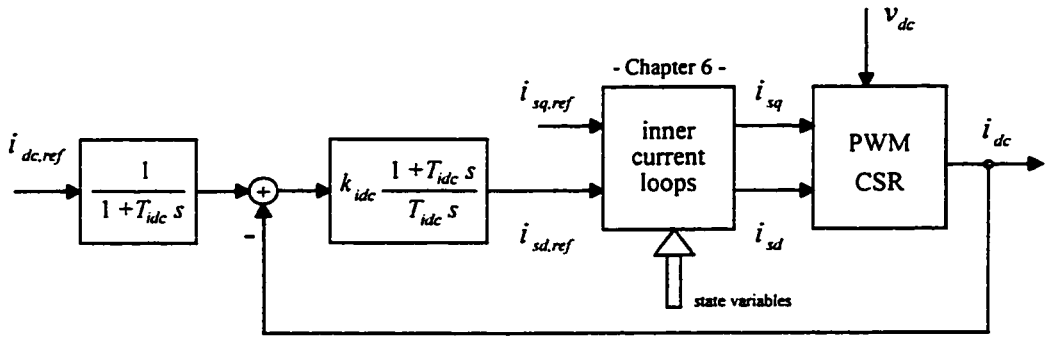

Fig. 7.3 dc link current control scheme using a standard PI controller.

Specifically, Fig. 7.4 shows the relevant waveforms for a step change in the dc link current reference at t = 30 ms and for a step change in the operating mode (from generation to regeneration) at t = 50 ms. It can be seen that the PI parameters can be designed to achieve an optimum dynamic response (overshoot, ξ_{idc}; and settling time, $t_{s,idc}$, for a given settling band, b_{idc}), for step changes in the dc link current reference (Fig. 7.4(c), t = 30 ms). However, the same parameters yield a highly oscillatory response for a load operating mode change (Fig. 7.4(c), t = 50 ms). This can also be noticed in the supply line current transient response (Fig. 7.4(a), t = 50 ms). The set-up is depicted in

Fig. 7.1 and the dc link current loop is shown in Fig. 7.3. The simulation conditions are given in APPENDIX A.6.

To overcome the non-linearities between i_{dc} and $i_{sd,ref}$, minimize the coupling effect of i_{sq}, and design a stable controller, the following control strategy is proposed.

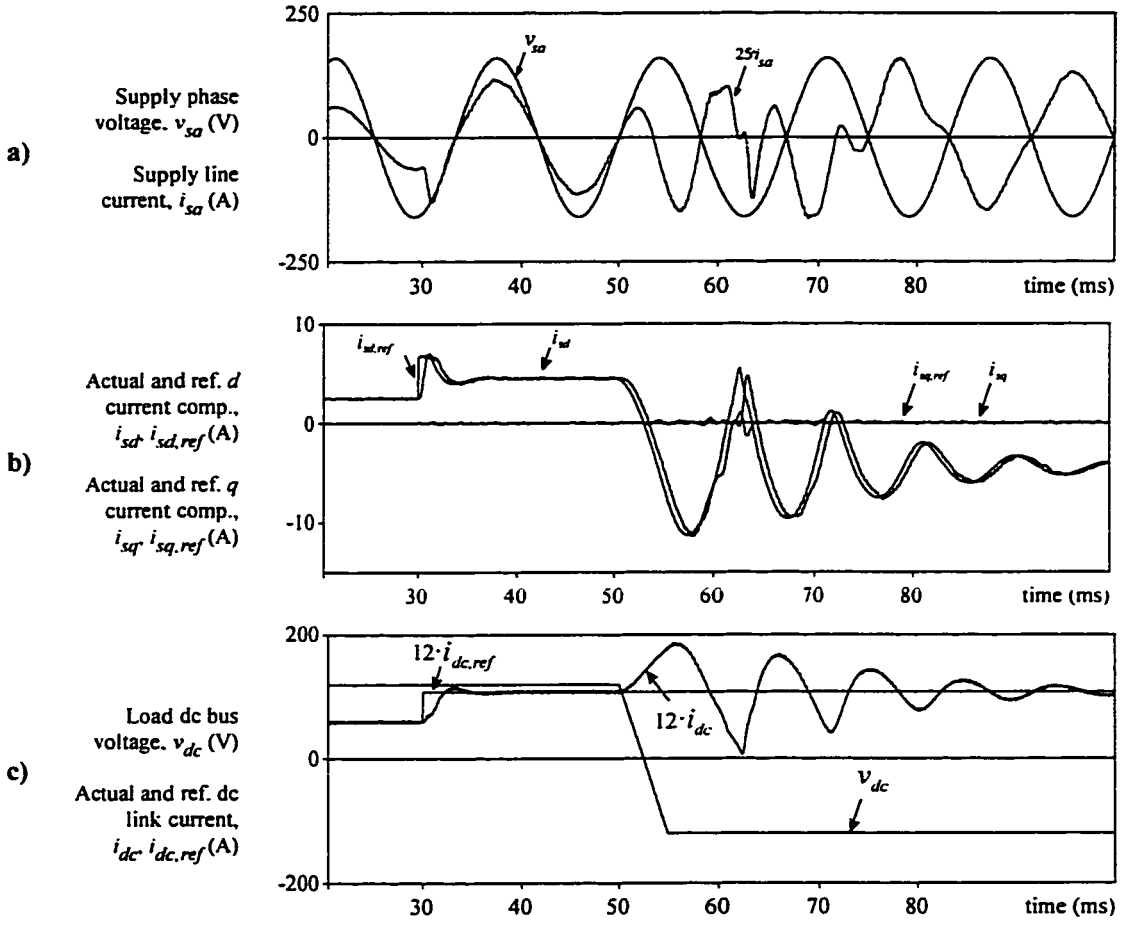

Fig. 7.4 Regenerative load mode simulation for a standard PI controller.

Simulated results. **a)** Supply voltage (v_{sa}) and current (i_{sa}). **b)** Actual supply current (i_{sd}, i_{sq}) and references ($i_{sd,ref}$, $i_{sq,ref}$). **c)** Actual dc current (i_{dc}), dc current reference ($i_{dc,ref}$), and load dc voltage (v_{dc}).

7.4 PROPOSED DC CURRENT LOOP STRATEGY

The internal loops (i_{sd} and i_{sq}) are designed to achieve fast settling times (less than 5 ms, Chapter 6). On the other hand, the dc current loop (outer loop) is designed to be slower than the line current loops; however, it should ensure optimum regulation and maintain the natural current-source operation. Therefore, the actual line current components can be considered equal to their references when designing the dc current loop. Although fast dynamic response is not required, stability is an important goal particularly under regenerative operation mode.

7.4.1 Generalized Load Model

Eq. (7.2) and (7.3) model the load as $R_{dc} \cdot i_{dc}^2$ for passive loads and $R_{dc} \cdot i_{dc}^2 + v_{dc}\, i_{dc}$ for active loads, respectively. By identifying terms, both expressions represent the instantaneous load power demand (p_{dc}) and thereby, both expressions can be written in a generalized form as,

$$L_{dc} i_{dc} \frac{d}{dt} i_{dc} = \frac{3}{2}(v_{rd} i_{sd,ref} + v_{rq} i_{sq,ref}) + p_{dc} \quad \text{W} \tag{7.8}$$

The load dc voltage (v_{dc}), combined with the dc link current information, is used to derive digitally the instantaneous load power demand and then used as a feedforward variable by the control strategy [90, 91].

7.4.2 dc Link Current Loop

If the right hand side of the generalized model (7.8) is chosen as an additional input u, the following control law is found,

$$i_{sd,ref} = \frac{2/3 \cdot (u - p_{dc}) - v_{rq} i_{sq,ref}}{v_{rd}} \quad \text{A} \tag{7.9}$$

and the generalized model (7.8) becomes,

$$L_{dc} i_{dc} \frac{d}{dt} i_{dc} = u \quad \text{W} \tag{7.10}$$

The resulting model (7.10) is independent of the load type (passive or active) and operation mode (generation or regeneration). Thus, a stable overall control strategy is expected. The resulting model (7.10) is a separable differential equation and if $i_{fb} = i_{dc}^2$, it is found that,

$$i_{fb} = \frac{2}{L_{dc}} \int_{-\infty}^{t} u \, d\tau \quad \text{A} \tag{7.11}$$

Eq. (7.11) represents a first order integrator; therefore, a first order filter in combination with a PI type controller ($k_{idc}(1+1/T_{idc}\, s)$ in a closed loop structure are used (Fig. 7.5). The total transfer function becomes,

$$\frac{i_{fb}(s)}{i_{fb,ref}(s)} = \frac{2k_{idc}}{T_{idc} L_{dc}} \frac{1}{s^2 + \frac{2k_{idc}}{L_{dc}} s + \frac{2k_{idc}}{T_{idc} L_{dc}}} \quad \text{A/A} \tag{7.12}$$

The gains k_{idc} and T_{idc} are designed to obtain a desired overshoot (i.e., 20%) and settling time (i.e., 10 ms). The total proposed control strategy is presented in Fig. 7.5.

7.4.3 Controller Design

Eq. (7.12) represents a standard second order transfer function; therefore, the controller parameters, are calculated to achieve a desired damping ratio (ξ_{idc}) and settling time ($t_{s,idc}$) for a given settling band (b_{idc}). Thus, by equalizing (7.12) with the standard

second order transfer function, the proportional and integral gains of the controllers are,

$$k_{idc} = \frac{L_{idc} \ln(1/b_{idc})}{T_s} \quad 1/A \tag{7.13}$$

$$T_{idc} = \frac{2\xi_{idc} t_{s,idc}}{\ln(1/b_{idc})} \quad s \tag{7.14}$$

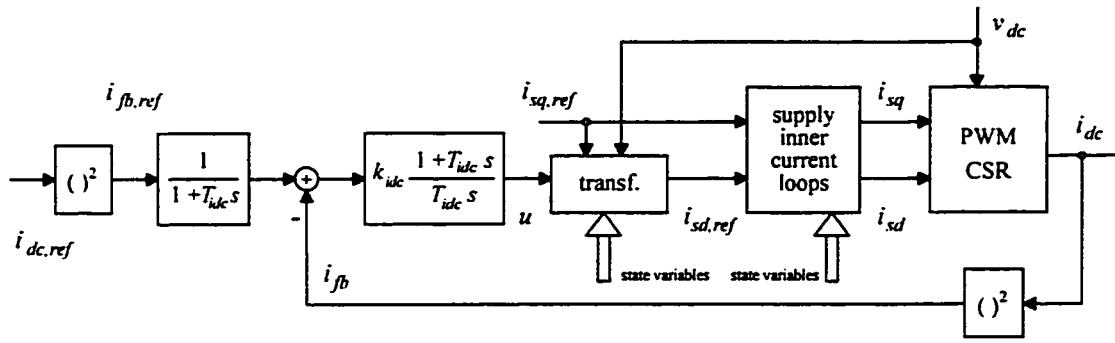

Fig. 7.5 Proposed dc link current control strategy.

Linearization, decoupling and dynamic optimization

7.5 SIMULATED RESULTS

The PWM-CSR (Fig. 7.1) supplying an active load was simulated using the proposed control strategy (Fig. 7.5). The set-up is depicted in Fig. 7.1 and the dc link current loop is shown in Fig. 7.5. The simulation conditions are given in APPENDIX A.6. Two different responses were studied. The dynamic response to step changes in the dc current reference (Fig. 7.6) and to a change from generation to regeneration mode (Fig. 7.7). From the results it is possible to conclude, (a) the reactive supply current component stays constant during the dc current transient (Fig. 7.6(b)), (b) the actual dc current loop follows the design parameters regardless of the operating point (Fig. 7.6(c)), (c) as the

load goes from generation to regeneration mode, the dc current stays practically constant, (Fig. 7.7(c)), and (d) the reactive supply current component stays constant before, while and after the load transient (Fig. 7.7(b)).

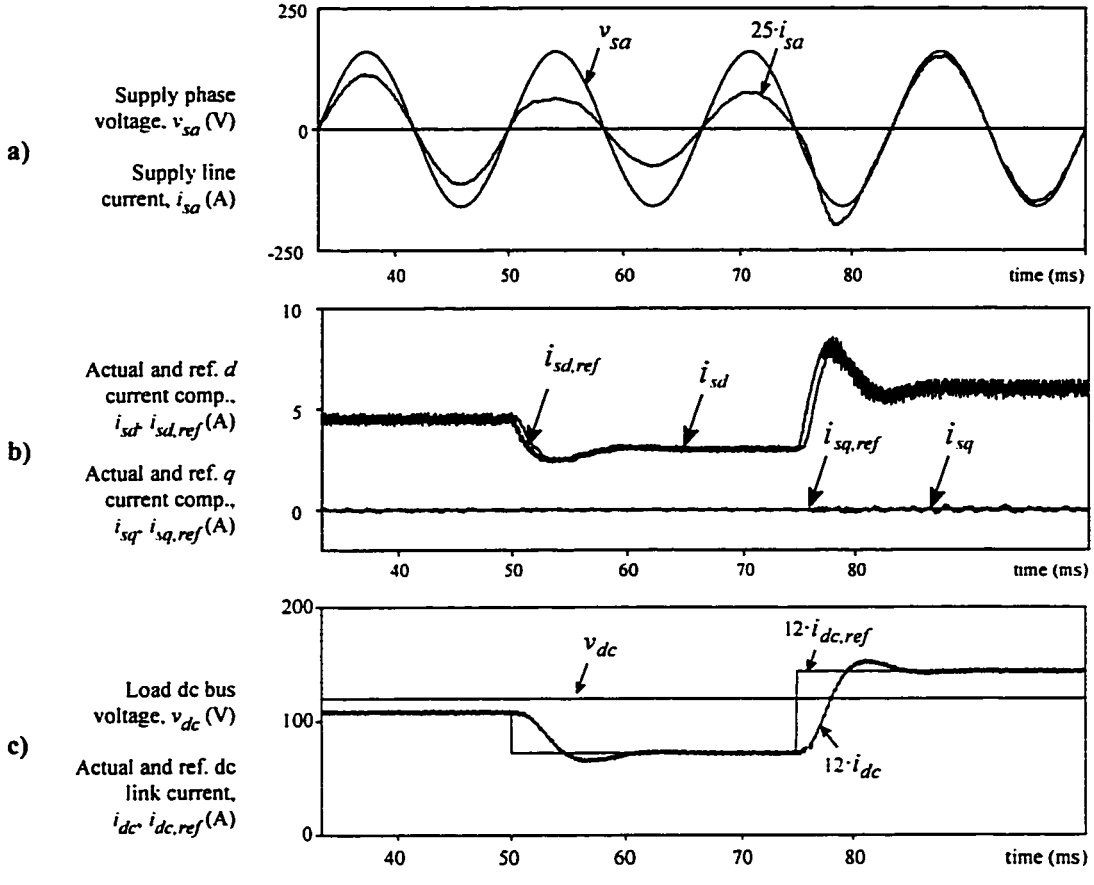

Fig. 7.6 PWM-CSR dynamic response under dc current reference step changes.

Simulated results. **a)** Supply voltage (v_{sa}) and current (i_{sa}). **b)** Actual supply current (i_{sd}, i_{sq}) and references ($i_{sd,ref}$, $i_{sq,ref}$). **c)** Actual dc current (i_{dc}), dc current reference ($i_{dc,ref}$), and load dc voltage (v_{dc}).

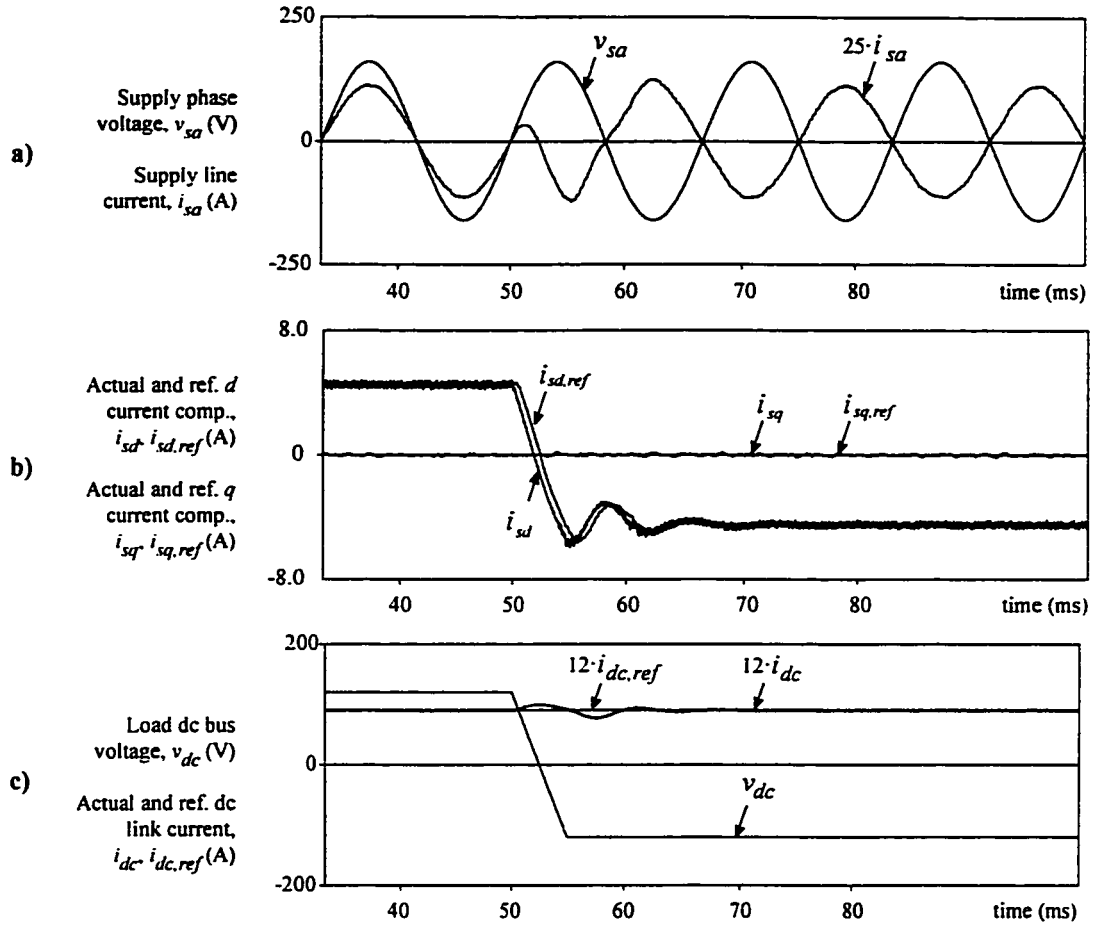

Fig. 7.7 PWM-CSR dynamic response from generation to regeneration mode.

Simulated results. **a)** Supply voltage (v_{sa}) and current (i_{sa}). **b)** Actual supply current (i_{sd}, i_{sq}) and references ($i_{sd.ref}$, $i_{sq.ref}$). **c)** Actual dc current (i_{dc}), dc current reference ($i_{dc.ref}$), and load dc voltage (v_{dc}).

7.6 Discussion and Conclusions

This chapter has introduced a dc current supply based on on-line control of the supply d and q current components of a PWM current source rectifier. The control strategy is based upon a cascade structure, where the inner loops are the supply d and q current component loops introduced in Chapter 6 of this thesis. Therefore, the control strategy features, (a) control in the dq frame, (b) independent control of the active and

reactive instantaneous supply power, (c) inherent supply current limiting capability, and (d) operation at unity, lagging or leading displacement factor.

In this chapter an outer dc link current loop based on instantaneous load power demand has been proposed. Thus, the overall control strategy is stable before, while, and after load transients (rectification to regeneration).

CHAPTER 8

SUMMARY AND CONCLUSIONS

8.1 SUMMARY

High performance on-line modulating techniques and control schemes for three-phase six-switch current-source topologies are investigated in this thesis. Specifically, the following aspects are studied:

1.- An on-line carrier-based PWM pattern generator is implemented. The circuit allows the direct implementation of any standard PWM carrier-based technique and thereby, the topology behaves as a current amplifier. An improved modulating technique is then derived that employs dead-band modulating signals and a saw-tooth carrier signal (Chapter 2). The pattern generator is implemented and the dead-band technique used to modulate a 5 kVA PWM current source rectifier prototype.

2.- Digital on-line PWM space-vector based modulating techniques minimizing the switching frequency are developed (Chapter 3). Unlike carrier-based techniques, these ones are readily implemented in digital systems. A generalized algorithm to select the zero space vector is derived. The sequences are tested by simulation and implemented on a TMS320C30 Real-Time System to modulate a 5 kVA current source inverter. The programming of the Real-Time System is done in real-time ANSI C.

3.- An inner load voltage and an outer modulation index control loop for current-source inverter topologies are investigated (Chapters 4 and 5). The inner loop ensures the operation of the topology as a variable voltage and frequency voltage supply. The outer

loop allows the operation at constant modulation index; therefore, at minimum dc link current. The loops are simulated and experimentally tested by means of a 5 kVA laboratory prototype.

4.- A non-linear control scheme for current-source rectifier topologies is proposed (Chapters 6 and 7). The approach allows the independent control of the active and reactive power drawn from the ac mains. Unity power factor operation becomes a special case. The rectifier mode is simulated and tested on a 5 kVA PWM current source converter. The regenerating mode is tested by means of simulation.

5.- To exploit the additional features available with digital control, an algorithm to reconstruct the ac voltages of a current source converter is developed and implemented (APPENDIX B). The technique allows the reduction of the number of voltage sensors. The algorithm is implemented on a TMS320C30 Real-Time System and used to reconstruct and control the output voltage of a 5 kVA current source inverter laboratory prototype.

For simulation purposes, two software programs are used: (a) the MicroSim PSPICE simulator versions 5.0 for DOS and 6.0 and 6.3 for WINDOWS, and (b) the PSIM (Power Electronic Circuit Simulation) simulator version 2.0 for DOS. For experimental purposes, three set-ups are employed (a) a forced commutated three-phase CS rectifier, (b) a forced commutated three-phase CS inverter, and (c) a phase-controlled three-phase thyristor rectifier. The design procedures are carried out by means of the MATHCAD software versions 5.0 and 5.0 Plus for WINDOWS.

8.2 CONCLUSIONS

The feasibility of the proposed on-line PWM techniques and control schemes for

three-phase six-switch current source converters is experimentally demonstrated. Laboratory prototypes in the 5 kVA range are used for experimental implementations. In addition, the experimental results validate the theoretical considerations, including the design guidelines for the passive components and the controller parameters. The following conclusions are reached regarding the proposed solutions to on-line modulation and control schemes:

1.- Current source converters can be on-line modulated using standard carrier-based (SPWM, trapezoidal,...) and space vector based techniques. Carrier-based techniques can be implemented using simple analog/digital electronics components. In this thesis, the proposed circuit realization also features: (a) operation with a free-running carrier waveform and (b) symmetric distribution of shorting and overlap pulses. Space vector techniques are directly implemented in digital systems, such as DSP based systems.

2.- The on-line modulation of current source topologies can be achieved at reduced switching frequency and maximum ac gain. For example, if three dead-band modulating waveforms and a saw-tooth carrier signal are used, the switching frequency is reduced to 1/2 of the carrier frequency and the ac gain is the maximum achievable. Both improvements are obtained without increasing the harmonic distortion.

3.- The analysis of digital pattern modulators based on the space vector technique shows that: (a) the sequence of non-zero space vectors defines the harmonic distortion of the PWM waveforms, (b) the selection of the zero space vector defines the resulting switching frequency, and (c) the appropriate selection of the normalized cycle frequency

minimizes the uncharacteristic harmonics in the PWM waveforms. It is found that regardless of the non-zero space vector sequence, there is only one zero space vector that provides minimum switching frequency in each cycle period. A switching frequency of at most 1/2 of the cycle frequency and the maximum achievable ac gain are achieved.

4.- Current source inverters can be operated as variable voltage power supplies. This is realized by using a closed loop with load voltage sensing that provides dynamic responses of the order of the carrier or cycle period. If an additional modulation index loop is used, the operation results in minimum dc link current operation. The integration of both loops feature: (a) very low and fixed *dv/dt* at the load side, (b) high efficiency due to minimum dc current operation, (c) attenuation of potential resonances due to the fast dynamic response of the inner voltage loop.

5.- Current source rectifiers can be operated at either leading, lagging, or unity displacement power factor. A non-linear control scheme allows the independent control of the reactive and active power components. The decoupling feature is achieved for both steady state and dynamic conditions. The technique also provides the necessary damping to ensure a stable operation in the rectification and regeneration modes.

8.3 SUGGESTIONS FOR FUTURE WORK

As an extension to this study of on-line modulating techniques and control schemes of three-phase six-switches current source converters, the following topics are suggested:

1.- Investigate and develop digital modulators based on the space vector technique to cover the overmodulation region.

2.- Optimize the sequence of non-zero space vectors and the selection of the zero space vector for minimum harmonic distortion at low cycle frequencies.

3.- Analyze and identify the effects of the overlaps required by the gating signal of current source converters.

4.- Extend and develop the proposed on-line modulating techniques to multi-level current source converters.

5.- Investigate the proposed non-linear control scheme for PWM current source rectifiers operated under unbalanced supply voltages.

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APPENDIX A

PARAMETER VALUES FOR THE VARIOUS EXPERIMENTAL SET-UPS

A.1 CS RECTIFIER MODULATED BY THE MOD. DEAD-BAND TECH. (SECTION 2.3)

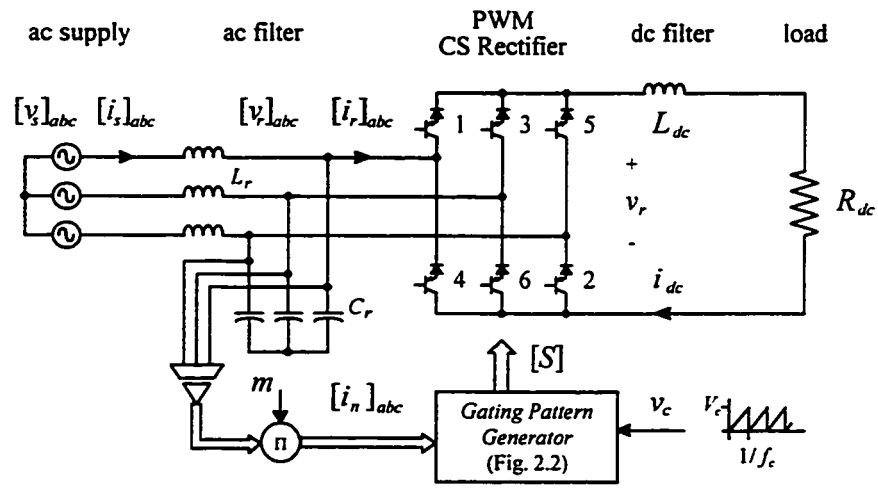


Fig. A.1 Experimental set-up, Section 2.3.

Table A.1 Components Values (set-up, Section 2.3)

Parameter	Value
m : nominal CSR modulation index	0.8 pu
f_c : carrier frequency	2.7 kHz
V_c : carrier amplitude	10 V
V_s : supply phase voltage	110 V
f_s : supply frequency	60 Hz
C_r : input filter capacitor	50 μF
L_r : input filter inductor	3 mH
L_{dc} : dc link inductor	30 mH
R_{dc} : load resistance	20 Ω

A.2 CS INVERTER MODULATED BY THE SPACE VECTOR TECH. SEQ_A (SECTION 3.3)

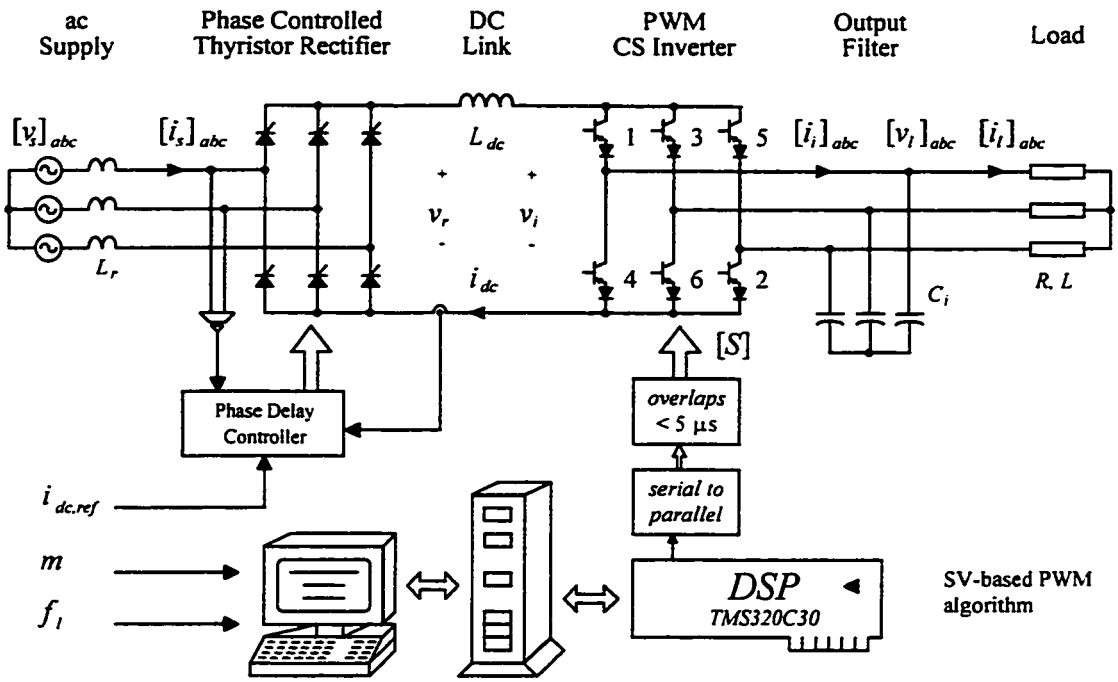


Fig. A.2 Experimental set-up, Section 3.3

Table A.2 Components Values (set-up, Section 3.3)

Parameter	Value
m : nominal CSI modulation index	0.8 pu
V_l : load phase voltage	110 V
f_l : load frequency	60 Hz
f_{cycle} : cycle frequency ♣	2.52 kHz
R : load resistance	17 Ω
L : load inductance	35 mH
$i_{dc,ref}$: dc link current reference	9 A
L_{dc} : dc link inductor	30 mH
C_i : load filter capacitor	35 µF

♣ : Experimental tests show that with a minimum sample period of 60 µs there is enough time to run the algorithm by the DSP system. Thus, the maximum cycle frequency is around 16.7 kHz.

A.3 VOLTAGE-CONTROLLED CSI GENERAL POWER SUPPLY (SECTION 4.4)

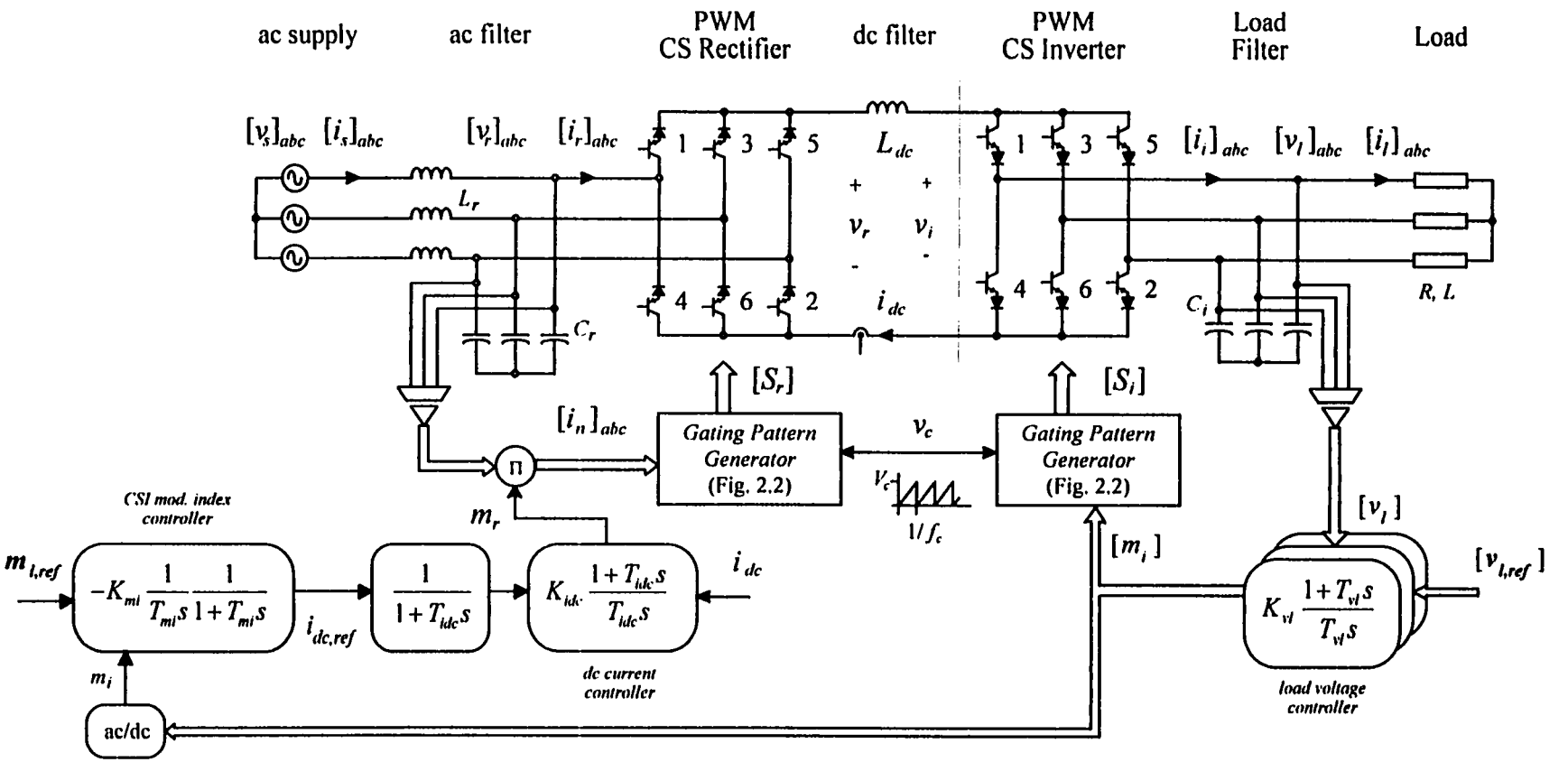


Fig. A.3 Experimental set-up, Section 4.4

Table A.3 Components Values (set-up, Section 4.4)

Parameter	Value
m_i : nominal CSI modulation index	0.8 pu
V_s : supply phase voltage	110 V
f_s : supply frequency	60 Hz
V_l : load line voltage	110 V
f_l : load frequency	60 Hz
f_c : carrier frequency	1.98 kHz
V_c : carrier amplitude	10 V
R : load resistance	19.36 Ω
L : load inductance	38.51 mH
i_{dc} : dc link current	5.25 A
Δv_l : load voltage peak-to-peak ripple	0.05 pu
Δi_{dc} : dc current peak-to-peak ripple	0.20 pu
Δv_r : input capacitor voltage ripple	0.10 pu
L_{dc} : dc link inductor	50 mH
C_i : load filter capacitor	66 μF
C_r : input filter capacitor	50 μF
L_r : input filter inductance	3 mH
K_{vl} : load voltage gain	0.49 pu
T_{vl} : load voltage integral gain	757 μs
K_{idc} : dc link current gain	1/230 pu
T_{idc} : dc link current integral gain	3.16 ms
ξ_{idc} : damping factor, dc link current loop	0.59 pu
t_{idc} : settling time, dc link current loop	16 ms
b_{idc} : settling band, dc link current loop	25 m
K_{mi} : CSI mod. index gain	-4.7 pu
T_{mi} : CSI mod. index integral gain	8.35 ms
ξ_{mi} : damping factor, mod. index loop	0.59 pu
t_{mi} : settling time, mod. index loop	50 ms
b_{mi} : settling band, mod. index. loop	50 m

A.4 CSI BASED AC DRIVE SET-UPS (SECTION 5)

A.4.1 ac Drive Based on a Thyristor Rectifier (Section 5.2.1)

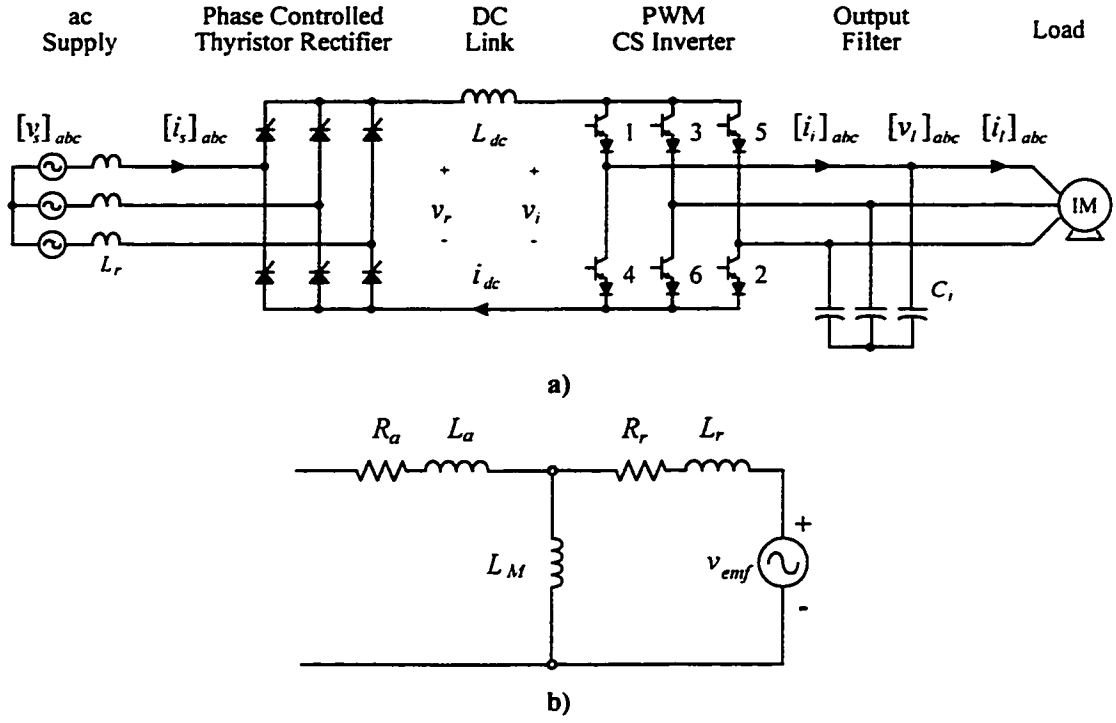


Fig. A.4 Simulated set-up, Section 5.2.1

a) Power topology, b) Induction machine per phase model.

Table A.4 Components Value (set-up, Section 5.2.1)

Parameter	Value
V_s : supply phase voltage	110 V
f_s : supply frequency	60 Hz
f_l : load frequency	60 Hz
L_r : supply inductance	1 mH
L_{dc} : dc link inductance	100 mH
C_i : load filter capacitor	30 μF
R_a, R_r : armature/rotor resistance	0.6 Ω
L_a, L_r: armature/rotor inductance	2.12 mH
L_M : magnetizing inductance	53 mH
V_{emf} : back emf voltage	110 V

A.4.2 ac Drive Based on a PWM Front End Rectifier (Section 5.2.2)

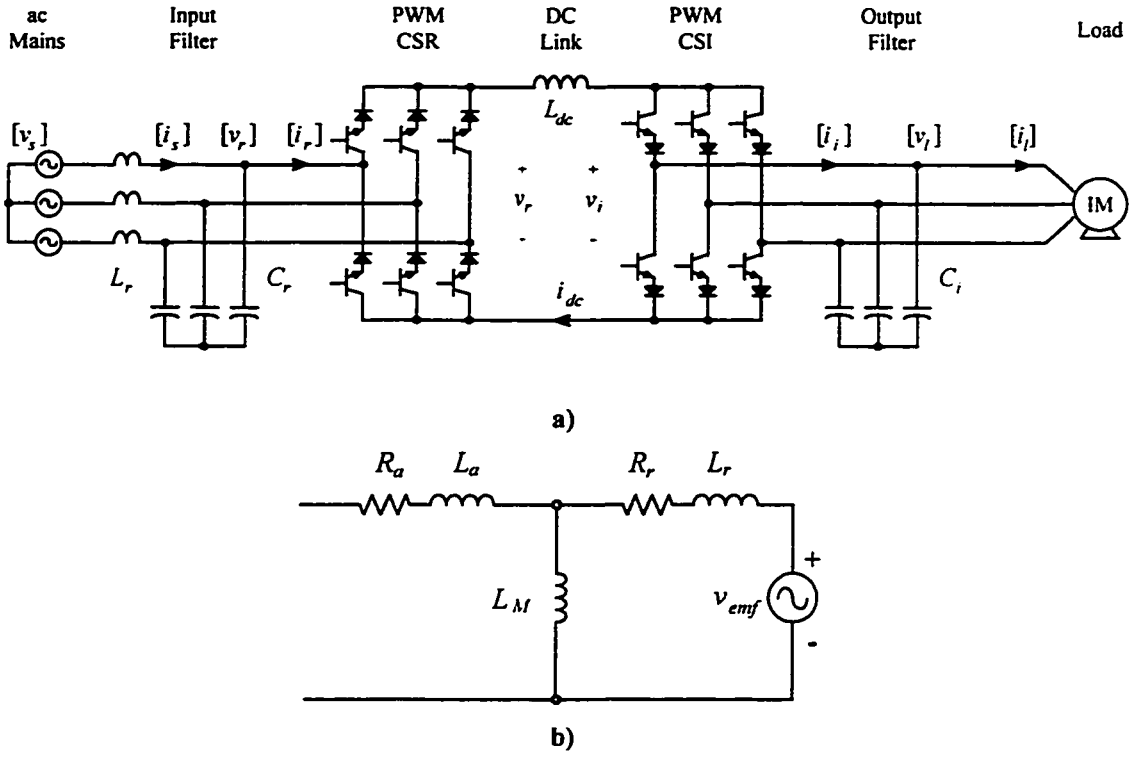


Fig. A.5 Simulated set-up, Section 5.2.2

a) Power topology, b) Induction machine per phase model.

Table A.5 Components Value (set-up, Section 5.2.2)

Parameter	Value
V_s : supply phase voltage	110 V
f_s : supply frequency	60 Hz
f_l : load frequency	60 Hz
L_r : supply filter inductance	3 mH
C_r : supply filter capacitance	50 μF
L_{dc} : dc link inductance	30 mH
C_i : load filter capacitor	30 μF
R_a, R_r : armature/rotor resistance	0.6 Ω
L_a, L_r: armature/rotor inductance	2.12 mH
L_M : magnetizing inductance	53 mH
V_{emf} : back emf voltage	110 V

A.4.3 Experimental Set-Up for the Proposed ac Drive (Section 5.5)

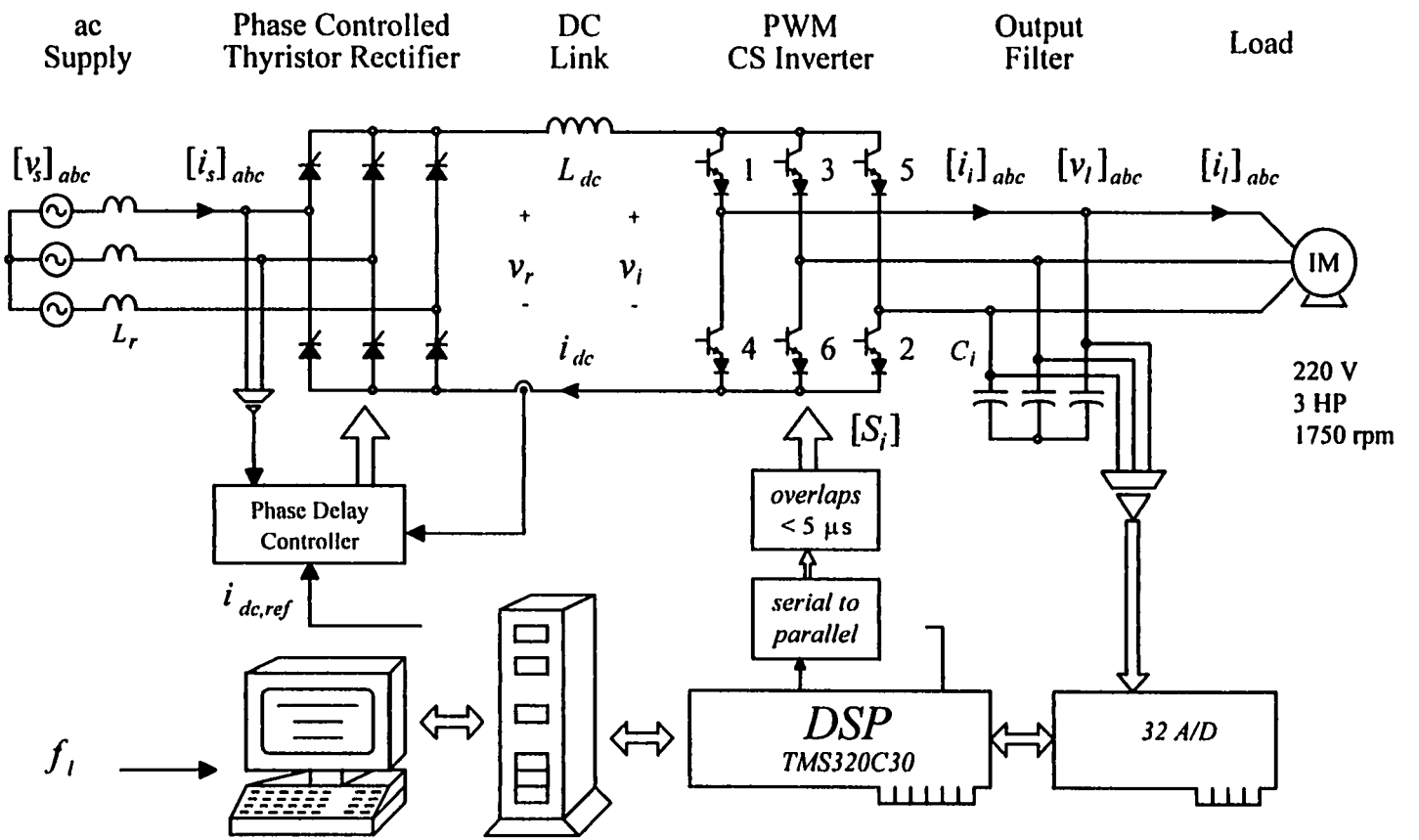


Fig. A.6 Experimental set-up, Section 5.5

A.5 POWER FLOW CONTROL IN PWM-CSR (SECTION 6.5)

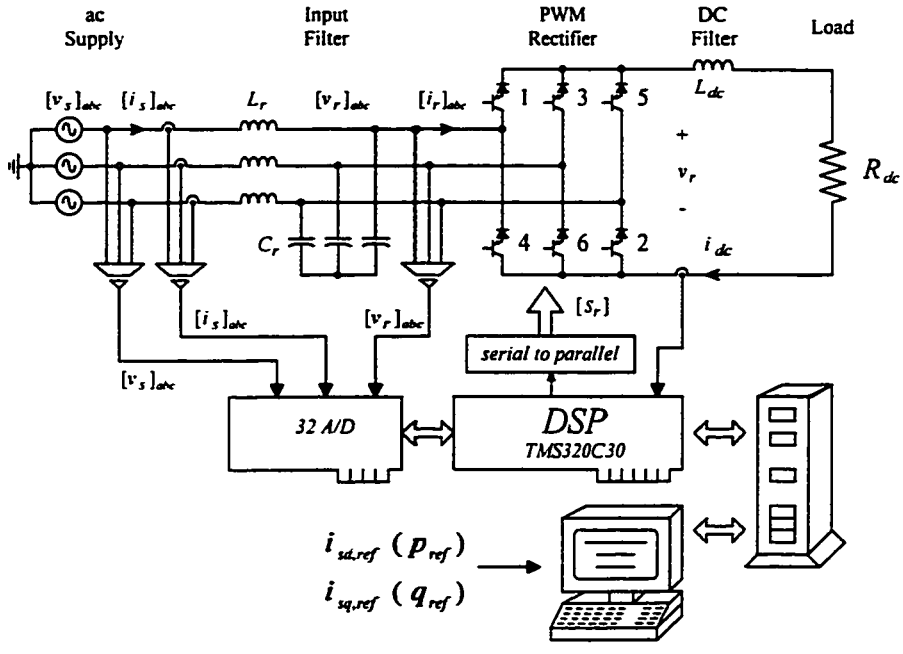


Fig. A.7 Experimental set-up, Section 6.5

Table A.6 Components Values (set-up, Section 6.5)

Parameter	Value
V_s : supply phase voltage	110 V
f_s : supply frequency	60 Hz
f_{cycle} : cycle frequency	5.04 kHz
f_{ri} : filter resonant frequency	9 pu
Δv_r : capacitor voltage peak-to-peak ripple	0.20 pu
Δi_{dc} : dc current peak-to-peak ripple	0.20 pu
L_r : input filter inductor	2 mH
C_r : input filter capacitor	40 μF
L_{dc} : dc link inductor	18 mH
R_{dc} : load resistance	20 Ω
$t_{s,ac}$: line current loop settling time	5 ms
k_1 : pole placement gain	2.64 k
k_2 : pole placement gain	4.89 M
t_{ac} : integral gain	1.43 ms

A.6 DC LINK CURRENT CONTROL IN PWM-CSR (SECTION 7)

Table A.7 Components Values (set-up, Section 7.3)

Parameter	Value
V_s : supply phase voltage	110 V
f_s : supply frequency	60 Hz
f_{cycle} : cycle frequency	5.04 kHz
f_m : filter resonant frequency	9 pu
Δv_r : capacitor voltage peak-to-peak ripple	0.20 pu
Δi_{dc} : dc current peak-to-peak ripple	0.20 pu
L_r : input filter inductor	2 mH
C_r : input filter capacitor	40 μF
L_{dc} : dc link inductor	18 mH
V_{dc} : load voltage	120 V
$t_{s,idc}$: dc link current loop settling time	10 ms
ξ_{idc} : dc link current loop damping ratio	0.71 pu
k_{idc} : PI proportional gain	100 m
T_{idc} : PI integral gain	1.0 ms

Table A.8 Components Values (set-up, Section 7.4)

Parameter	Value
V_s : supply phase voltage	110 V
f_s : supply frequency	60 Hz
f_{cycle} : cycle frequency	5.04 kHz
f_m : filter resonant frequency	9 pu
L_r : input filter inductor	2 mH
C_r : input filter capacitor	40 μF
L_{dc} : dc link inductor	18 mH
V_{dc} : load dc voltage	120 V
$t_{s,idc}$: dc link current loop settling time	10 ms
ξ_{idc} : dc current damping factor	0.71 pu
k_{idc} : PI proportional gain	7.04 pu
T_{idc} : PI integral gain	2.56 ms

APPENDIX B

LOAD VOLTAGE RECONSTRUCTION ALGORITHM

B.1 GENERAL FORMULATION

The following algorithm reconstructs the ac voltages of a three-phase six-switch current source converter. Although it is actually developed and implemented on a CS Inverter, it can also be implemented on a CS Rectifier. Since the algorithm is implemented on a digital system, the converter is consequently modulated by a digital approach. In the following, the space vector technique (Chapter 3) is used to modulate the converter. The algorithm manipulates the sampled voltage in the dc link CSI side (v_i), the already available switching pattern information (S_{ik}, k = 1,..., 6), and the space vector sinusoidal templates (Fig. B.1).

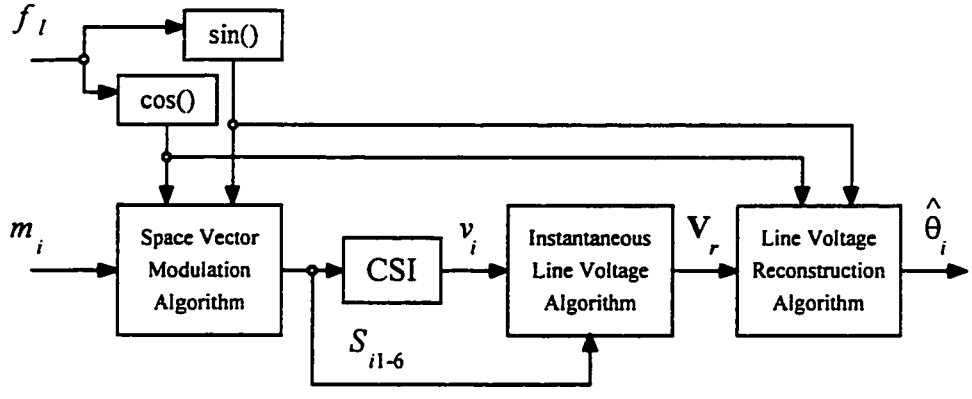


Fig. B.1 Load Voltage Reconstruction Scheme, Appendix A.2

Thus, the actual load voltages are assumed to be of the form:

$$\hat{y}_1(t_k) = \hat{v}_{ab}(t_k) = a_1 \cos(2\pi f_o t_k) + b_1 \sin(2\pi f_o t_k) \quad \text{(B.1)}$$

$$\hat{y}_2(t_k) = \hat{v}_{bc}(t_k) = a_2 \cos(2\pi f_o t_k) + b_2 \sin(2\pi f_o t_k) \quad \text{(B.2)}$$

$$\hat{y}_3(t_k) = \hat{v}_{ca}(t_k) = a_3 \cos(2\pi f_o t_k) + b_3 \sin(2\pi f_o t_k) \quad \text{(B.3)}$$

where, $\hat{y}_i(t_k)$: reconstructed load voltages (i = 1, 2, 3)

$\hat{\theta}_i = [a_i \quad b_i]^T$: coefficients to identify (i = 1, 2, 3)

$\sin(2\pi f_l t_k), \cos(2\pi f_l t_k)$: sinusoidal templates ($f_l$: load frequency)

In order to find the best coefficients $\hat{\theta}_i = [a_i \quad b_i]^T$ a LSE algorithm is used. Thus, if the sampled dc bus voltage at the time t_k is $v_i(t_k)$, the actual pieces of the load voltage are given by the following algorithm (*instantaneous line voltage algorithm* in Fig. B.1):

$v_{ab}(t_k) = 0$;
$v_{bc}(t_k) = 0$;
$v_{ca}(t_k) = 0$;
if ((S_{i1}==on) && (S_{i2}==on)) $v_{ca}(t_k) = -v_i(t_k)$;
if ((S_{i2}==on) && (S_{i3}==on)) $v_{bc}(t_k) = v_i(t_k)$;
if ((S_{i3}==on) && (S_{i4}==on)) $v_{ab}(t_k) = -v_i(t_k)$;
if ((S_{i4}==on) && (S_{i5}==on)) $v_{ca}(t_k) = v_i(t_k)$;
if ((S_{i5}==on) && (S_{i6}==on)) $v_{bc}(t_k) = -v_i(t_k)$;
if ((S_{i6}==on) && (S_{i1}==on)) $v_{ab}(t_k) = v_i(t_k)$;

The voltages $v_{ab}(t_k)$, $v_{bc}(t_k)$, and $v_{ca}(t_k)$ are the actual pieces of the load voltages, and they are conveniently represented by the vector $\mathbf{V}_r(t_k) = [v_{ab}(t_k) \quad v_{bc}(t_k) \quad v_{ca}(t_k)]^T$.

The reconstructed load voltages (B.1) to (B.3) can be rewritten as,

$$\hat{y}_i(t_k) = \mathbf{N}^T(t_k) \cdot \hat{\theta}_i \qquad i = 1, 2, 3 \quad \text{(B.4)}$$

where, $\mathbf{N}^T(t_k) = [\cos(2\pi f_o t_k) \quad \sin(2\pi f_o t_k)]$

Since $v_{ab}(t_k)$, $v_{bc}(t_k)$ and $v_{ca}(t_k)$ are the actual pieces of the line load voltages, the actual load voltage vector can be written as,

$$\mathbf{V}_o(t_k) = [y_1(t_k) \quad y_2(t_k) \quad y_3(t_k)]^T = [v_{ab}(t_k) \quad v_{bc}(t_k) \quad v_{ca}(t_k)]^T \tag{B.5}$$

After N samples, the reconstructed load voltages (B.4) can be written as,

$$\hat{\mathbf{Y}}_i(t_N) = \mathbf{M}(t_N) \cdot \hat{\theta}_i \tag{B.6}$$

where, $\hat{\mathbf{Y}}_i(t_N) = [\hat{y}_i(t_1) \quad \cdots \quad \hat{y}_i(t_N)]^T$, $i = 1, 2, 3$

$\mathbf{M}(t_N) = [\mathbf{N}(t_1) \quad \cdots \quad \mathbf{N}(t_N)]^T$

B.2 FORMULATION OF THE LSE ALGORITHM

The general LSE solution of (B.6) that includes a weighing matrix ($\mathbf{W}_i(t_N)$) is:

$$\hat{\theta}_i = (\mathbf{M}^T(t_N)\mathbf{W}_i(t_N)\mathbf{M}(t_N))^{-1}\mathbf{M}^T(t_N)\mathbf{W}_i(t_N)\mathbf{Y}_i(t_N) \tag{B.7}$$

where, $\mathbf{Y}_i(t_N) = [y_i(t_1) \quad \cdots y_i(t_N)]^T$, is the actual load voltage vector, $i = 1, 2, 3$.

The matrix $\mathbf{W}_i(t_N)$ should ensure fast dynamic response of the identification algorithm. Thus, it is chosen of the form,

$$\mathbf{W}_i(t_N) = \begin{bmatrix} \lambda_i^{N-1} & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & \lambda_i^1 & 0 \\ 0 & \cdots & 0 & 1 \end{bmatrix} \tag{B.8}$$

where, λ_i : forgetting factor ($0 < \lambda_i = \lambda \leq 1$, $i = 1, 2, 3$)

In real-time applications, the expression for the coefficients (B.7) can be further simplified if $\mathbf{M}(t_N)$ and $\mathbf{W}_i(t_N)$ are fixed. This is the case when the number of samples (N), the forgetting factor (λ) and the load frequency (f_l) are not time dependent. Under these

conditions, the factor $(\mathbf{M}^T(t_N)\mathbf{W}_i(t_N)\mathbf{M}(t_N))^{-1}\mathbf{M}^T(t_N)\mathbf{W}_i(t_N)$ becomes constant and therefore could be pre-calculated and stored off-line. Thus, (B.7) could be solved on-line with a minimum number of operations. However, the above conditions are not present in the proposed applications (i.e., when the number of samples (N) or the load frequency (f_l) need to be modified on-line). Therefore, a Recursive LSE (RLSE) algorithm is preferred that can solve (B.7) on-line with a minimum number of operations and without requiring pre-calculated and stored data.

B.3 FORMULATION OF THE RECURSIVE LSE ALGORITHM

The sequential RLSE algorithm derived from (B.6) and (B.7) is as follows,

$$e_i(t_k) = y_i(t_k) - \mathbf{N}^T(t_k)\cdot\hat{\theta}_i(t_{k-1}) \qquad i = 1, 2, 3 \tag{B.9}$$

$$\gamma(t_k) = \lambda + \mathbf{N}^T(t_k)\cdot\mathbf{P}(t_{k-1})\cdot\mathbf{N}(t_k) \tag{B.10}$$

$$\mathbf{K}(t_k) = \mathbf{P}(t_{k-1})\cdot\mathbf{N}(t_k) \tag{B.11}$$

$$\hat{\theta}_i(t_k) = \hat{\theta}_i(t_{k-1}) + \frac{\mathbf{K}(t_k)\cdot e_i(t_k)}{\gamma(t_k)} \qquad i = 1, 2, 3 \tag{B.12}$$

$$\mathbf{P}(t_k) = \left\{\mathbf{P}(t_{k-1}) - \frac{\mathbf{K}(t_k)\cdot\mathbf{K}^T(t_k)}{\gamma(t_k)}\right\}\cdot\frac{1}{\lambda} \tag{B.13}$$

where, $e_i(t_k)$: instantaneous error

$\gamma(t_k)$: correction factor

$\mathbf{K}(t_k)$: correction vector

$\mathbf{P}(t_k)$: propagation matrix

λ : forgetting factor ($0 < \lambda \leq 1$)

The value of λ defines the stability and the speed of the identification algorithm.

In fact, a high value ($\lambda \approx 1$) provides good stability; however, the algorithm presents an overall poor tracking capability. Experimental tests have shown that $\lambda = 0.8$ provides a good compromise between stability and tracking.

B.4 EXPERIMENTAL VERIFICATION

The above algorithm was experimentally tested on the set-up depicted in Fig. A.2 under the conditions presented in Table. A.2. Experimental waveforms are given in Fig. B.2 and confirm the feasibility of the proposed algorithm. The totality of routines needed to modulate the CSI and to reconstruct the load voltages require a minimum sample time of 120 μs, when a TMS320C30 DSP microprocessor is used. This allows a maximum switching frequency of 8.33 kHz.

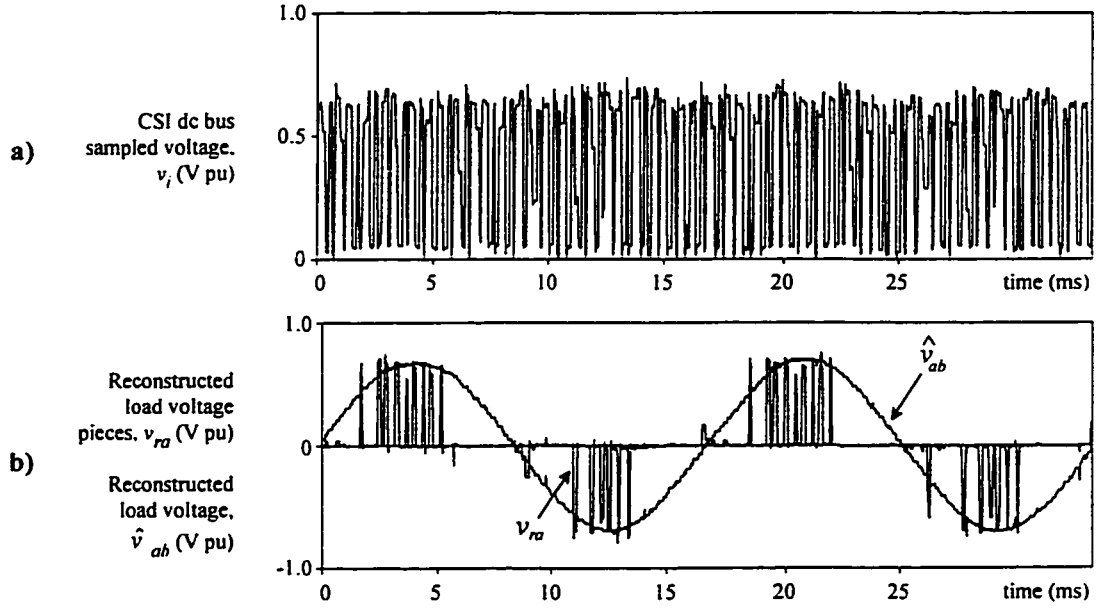


Fig. B.2 Experimental waveforms, Load Voltage Reconstruction, Appendix A.4

a) CSI input dc bus sampled voltage (v_i). **b)** Actual pieces of the reconstructed load voltage (v_{ra}) and reconstructed load voltage ($\hat{v}_{ab}$).

APPENDIX C

DESIGN GUIDELINES DERIVATION

C.1 PASSIVE COMPONENTS OF THE INTEGRATED VC-CSI (SECTION 4.3)

C.1.1 Load Capacitive Filter

The single phase equivalent circuit of the ac CSI line current (i_{ik}, k = 1,2, 3), RL load, and load filter (C_i) is depicted in Fig. C.1(b). Fig. C.2(b) shows the approximated ac CSI line current waveform. A wye connection of the load is assumed.

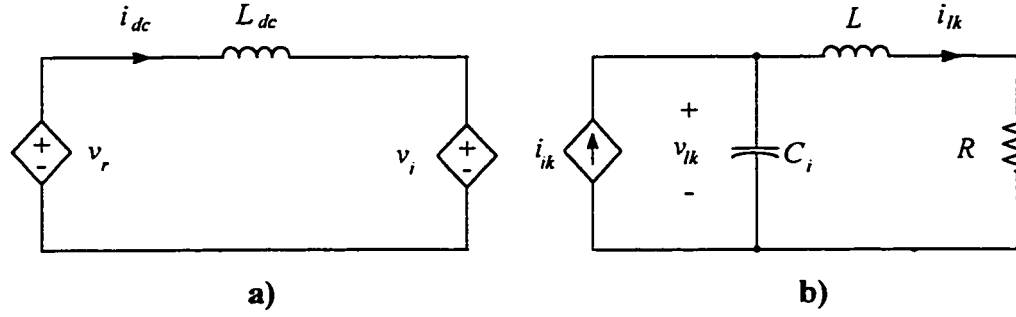


Fig. C.1 dc link and load equivalent circuits, Section 4.3

a) dc link equivalent circuit. **b)** per phase load equivalent circuit.

From Fig. C.2(b) can be concluded that the highest ac line current harmonic ($d(t)$ = 0.5) is around the cycle frequency and with an equivalent amplitude given by $i_{ik,fc} = I_{dc}$ / 2. At the carrier frequency the RL load can be considered as an open loop (worst case). Therefore, the voltage harmonic at the carrier frequency across C_i is given by,

$$v_{lk,fc} = \frac{I_{dc}}{2}\frac{X_{Ci}}{f_c} \quad \text{V} \tag{C.1}$$

If the peak-to-peak load voltage harmonic at the carrier frequency is limited to be

Δv_l V_l, (C.1) yields,

$$X_{Ci} = \frac{\Delta v_l f_c}{I_{dc}} \quad \Omega \text{ pu} \tag{C.2}$$

On the other hand, it can be seen from Fig. C.1(b) the fundamental load voltage is given by,

$$V_{l,1} = G_{ac} M_i I_{dc} \frac{X_{Ci}}{\sqrt{X_{Ci}^2 - 2X_{Ci}X_l + 1}} \quad \text{V} \tag{C.3}$$

By combining (C.2) and (C.3), the expression for the load filter capacitance is,

$$X_{Ci} = X_l + \sqrt{(G_{ac} M_i f_c \Delta v_l)^2 + X_l^2 - 1} \quad \Omega \text{ pu} \tag{C. 4}$$

C.1.2 dc Link Filter

The equivalent circuit of the dc link is depicted in Fig. C.1(a). Fig. C.2(a) shows the approximated CSI dc bus voltage waveform. The peak value is at most the peak line load voltage. Note that the approximated CSR dc bus voltage waveform looks as the CSI dc bus voltage waveform.

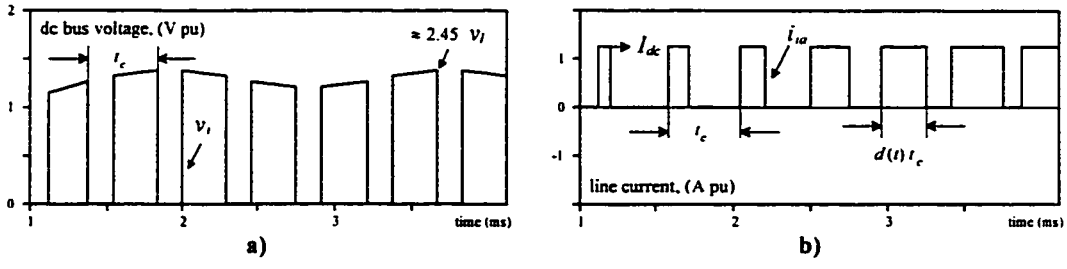


Fig. C.2 Approximated dc link voltage and ac CSI line current, Section 4.3

a) dc link voltage (v_r or v_i). **b)** ac CSI line current.

The worst case condition is when both the CSR and CSI dc bus voltages overlap

each other and therefore, the resulting voltage amplitude at the carrier frequency across the dc link inductor is $\sqrt{6}\,V_l$. Therefore, the dc link current harmonic amplitude at the carrier frequency is given by,

$$i_{dc,fc} = \frac{\sqrt{6}}{X_{Ldc}} \frac{V_l}{f_c} \quad \text{A} \tag{C.5}$$

If the peak-to-peak dc link current harmonic at the carrier frequency is limited to be $\Delta i_{dc}\, I_{dc}$, (C.5) yields,

$$X_{Ldc} = \frac{2\sqrt{6}}{\Delta i_{dc} I_{dc} f_c} \quad \Omega \text{ pu} \tag{C.6}$$

C.1.3 Input Filter

Due to the symmetry of the front-end and load power topologies. The input capacitor can be designed to meet the same requirements as the load capacitive filter. From, (C.2) one can write,

$$X_{Cr} = \frac{\Delta v_r f_c}{I_{dc}} \quad \Omega \text{ pu} \tag{C.7}$$

Since the input filter resonance (f_{rr}) must be within a given range, the input filter inductance is therefore calculated as,

$$X_{Lr} = X_{Cr} / f_{rr}^2 \quad \Omega \text{ pu} \tag{C.8}$$

C.2 Controller Parameters of the Integrated VC-CSI (Section 4.3)

C.2.1 Load Voltage Controller

The load voltages are controlled by on-line adjusting the modulating waveforms of the PWM inverter. The controllers are three identical PI type structure, where the gain

is maximized to enhance the dynamic response of the load voltage loop, Fig. A.3. In order to ensure intersections between the modulating signal ($[m_i]$) and the carrier waveform (v_c), the slope criterion is used to find the maximum gain. The PI controller transfer function is given by,

$$K_{vl}\frac{1+T_{vl}s}{T_{vl}s} \quad 1/V \tag{C.9}$$

The slope of the modulating signal is mainly produced by the load voltage component at the carrier frequency. This component is superimpose on the feedback variable, which is amplified by the PI controller. Therefore, the modulating signal slope (m_{i_slope}) is,

$$m_{i\_slope} = K_{vl}\frac{\sqrt{1+(2\pi f_c T_{vl})^2}}{2\pi f_c T_{vl}}\frac{2\pi f_c \Delta v_l V_l}{2} \quad 1/s \tag{C.10}$$

The maximum permissible slope of the modulating signal is the carrier slope, that is given by $V_c f_c$ for a saw tooth type of signal. Therefore, the maximum PI gain (K_{vl}) for a given integral gain (T_{vl}) is,

$$K_{vl} = \frac{2 f_c T_{vl}}{\sqrt{1+(2\pi f_c T_{vl})^2}}\frac{V_c}{\Delta v_l} \quad 1/V \tag{C.11}$$

C.2.2 dc Link Current Controller

The dc current is controlled by adjusting the modulation index of the front-end PWM rectifier (m_r). From Fig. A.3 and Fig. C.1(a) the model of the PWM CSR can be written as,

$$\frac{1}{V_c} m_r [v_r]^2 G_{ac} = L_{dc}\frac{d}{dt} i_{dc} + v_i \quad V \tag{C.12}$$

If the ac side rectifier voltage is considered constant and equal to the supply voltage ($[v_s] = [v_r]$), the Laplace transform of the small signal model representation of (C.12) becomes,

$$\frac{i_{dc}(s)}{m_r(s)} = \frac{3G_{ac}V_s^2}{V_c L_{dc}} \frac{1}{s} \quad \text{A} \tag{C.13}$$

In order to obtain a standard second order transfer function, a PI controller and a low pass filter are used, Fig. A.3. The resulting closed loop transfer function is,

$$\frac{i_{dc}(s)}{i_{dc,ref}(s)} = \frac{3G_{ac}V_s^2 K_{idc}}{V_c L_{dc} T_{idc}} \frac{1}{s^2 + \frac{3G_{ac}V_s^2}{V_c L_{dc}} s + \frac{3G_{ac}V_s^2 K_{idc}}{V_c L_{dc} T_{idc}}} \quad \text{A/A} \tag{C.14}$$

If the damping factor is ξ_{idc}, the settling time is t_{idc}, and the band for the settling time is b_{idc}, the gains are,

$$K_{idc} = \frac{V_c X_{Ldc} f_{cn} \ln(1/b_{idc})}{3\pi G_{ac} t_{idc}} \quad 1/\text{A} \tag{C.15}$$

$$T_{idc} = \frac{2\zeta_{idc}^2 t_{idc}}{\ln(1/b_{idc})} \quad \text{s} \tag{C.16}$$

C.2.3 CSI Modulation Index Controller

The CSI modulation index is controlled by regulating the dc link current. Thereby, this control loop generates the dc link current reference in a cascade structure, Fig. A.3. This loop is designed to be slower than the load voltage controller; therefore, the load voltages can be considered fixed an equal to the reference. Thus, the model can be expressed as,

$$V_l = \frac{LG_{ac}}{V_c}\frac{d}{dt}(m_i i_{dc}) + \frac{RG_{ac}}{V_c} m_i i_{dc} \quad \text{V} \tag{C.17}$$

Eq. (C.17) is non-linear; however, if the dynamic of the modulation index is forced to be slower than the dc link current dynamic, an analysis based on small signal model is found to provide good results. Thus, the small signal model obtained from (C.17) is,

$$\frac{m_i}{i_{dc}} = -\frac{M_i}{I_{dc}} \quad 1/\text{A} \tag{C.18}$$

In order to obtain a standard second order transfer function, a modified PI controller is used, Fig. A.3. The resulting closed loop transfer function is,

$$\frac{m_i(s)}{m_{i,ref}(s)} = \frac{M_i K_{mi}}{T_{mi}^2 I_{dc}} \frac{1}{s^2 + \frac{1}{T_{mi}} s + \frac{M_i K_{mi}}{T_{mi}^2 I_{dc}}} \quad \text{pu} \tag{C.19}$$

If the damping factor is ξ_{mi}, the settling time is t_{mi}, and the band for the settling time is b_{mi}, the gains are,

$$K_{mi} = \frac{I_{dc}}{4\xi_{mi}^2 M_i} \quad \text{A} \tag{C.20}$$

$$T_{mi} = \frac{t_{mi}}{2\ln(1/b_{mi})} \quad \text{s} \tag{C.21}$$

C.3 PASSIVE COMPONENTS OF THE PWM-CSR (SECTION 6.5 AND 7.2)

In order to simplify the design of L_{dc} and C_r, a maximum peak-to peak ripple criterion is used. On the other hand, L_r is designed to obtain a desired resonant frequency of the input ac filter. Thus, it is possible to avoid any resonance due to the PWM

operation of the CSR (harmonics around f_{cycle}, $2f_{cycle}$,...; with f_{cycle} = normalized cycle frequency), and non-characteristic harmonics (5^{th}, 7^{th},...) due to instantaneous saturation of the controllers, which yields overmodulation.

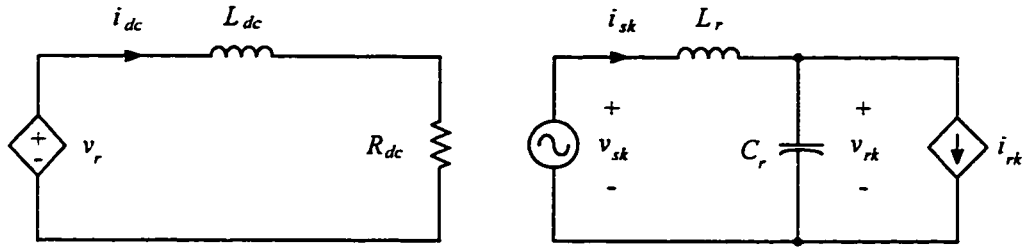


Fig. C.3 Equivalent circuits for the PWM-CSR, Section 6.5 and 7.2

a) dc link equivalent circuit. **b)** per phase load equivalent circuit ($k = a$, b, and phase c).

C.3.1 dc Link Inductor

The equivalent circuits for the PWM-CSR is shown in Fig. C.3. The approximated PWM-CSR dc bus voltage (v_{dc}) is depicted in Fig. C.4(a). If the voltage harmonics injected from the load side are neglected, it can be shown that the peak-to-peak dc current (Δi_{dc}) is given by,

$$\Delta i_{dc} = \frac{\sqrt{3} V_{sd}}{L_{dc} I_{dc}} G_{dc} M_d t_{cycle} \quad \text{A pu} \tag{C.22}$$

where, G_{dc} : dc gain of the mod. tech. ($G_{dc} = 0.866$, for the SVM),

t_{cycle} : cycle period of the SV (= 1 / (f_{cycle})),

By using (6.22), (C.22), and assuming $f_m^2 >> 1$, the normalized dc inductor reactance is given by,

$$X_{Ldc} = \frac{2\pi\sqrt{3}}{\Delta i_{dc} f_{cycle}} \frac{G_{dc}}{G_{ac}} \quad \Omega \text{ pu} \tag{C.23}$$

C.3.2 Input Filter Capacitor

The ac input capacitor (C_r) is designed to allow a given peak-to-peak voltage ripple across the input capacitor (Δv_r). If all current harmonics ($[i_r]_{abc}$) are absorbed by the ac capacitor (Fig. C.1(b)), the voltage ripple is given by,

$$\Delta v_r = \frac{I_{dc}}{C_r V_{sd}} d(t)\, t_{cycle} \quad \text{V pu} \tag{C.24}$$

Although $d(t)$ is a function of time (Fig. C.1(b)), the worst case corresponds to $d(t)$ = 0.5. Thus, by using (6.22) and (C.24), and assuming $f_{ri}^2 >> 1$, and maximum dc current (worst case), the normalized ac capacitor reactance is given by,

$$X_{Cr} = \frac{\Delta v_r f_{cycle}}{\pi} \quad \Omega \text{ pu} \tag{C.25}$$

C.3.3 Input Filter Inductance

Finally, the ac inductor (L_r) is calculated using a desired normalized resonant frequency for the input filter (f_{rr}). f_{rr} is usually chosen lower than a half of the normalized sample frequency (f_{cycle}) and higher than low frequencies due to transient overmodulation (5^{th}, 7^{th}). Thus, the reactance is given by,

$$X_{Lr} = X_{Cr} / f_{rr}^2 \quad \Omega \text{ pu} \tag{C.26}$$

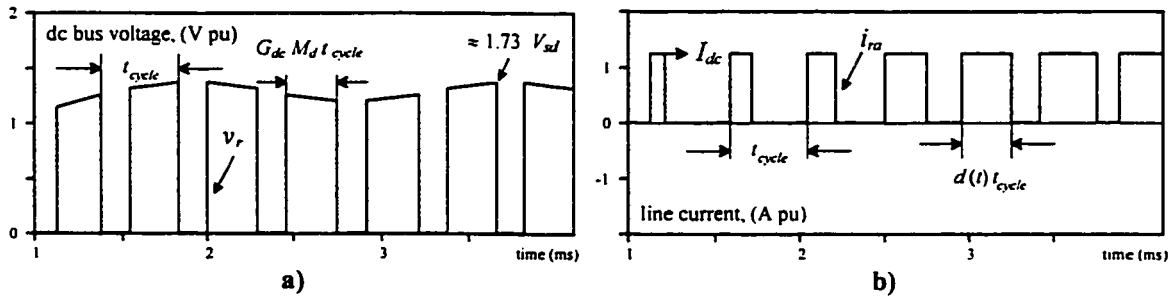


Fig. C.4 Approximated dc link voltage and ac CSR line current, Section 6.4 and 7.2

a) dc link voltage (v_r or v_i). **b)** ac CSI line current.

APPENDIX D

CSI BASED AC DRIVE TRANSFER FUNCTIONS

D.1 MOTOR VOLTAGE CONTROL DIAGRAM (SECTION 5)

The motor voltage control loop is shown in Fig. D.1. The *voltage controller* is a PI type controller, Chapter 4. The *gating signal generator* can be analog (Chapter 2) or digitally (Chapter 3) implemented. in an analog or digital Fig. D.1(b) shows the approximated ac CSI line current waveform. A wye connection of the load is assumed.

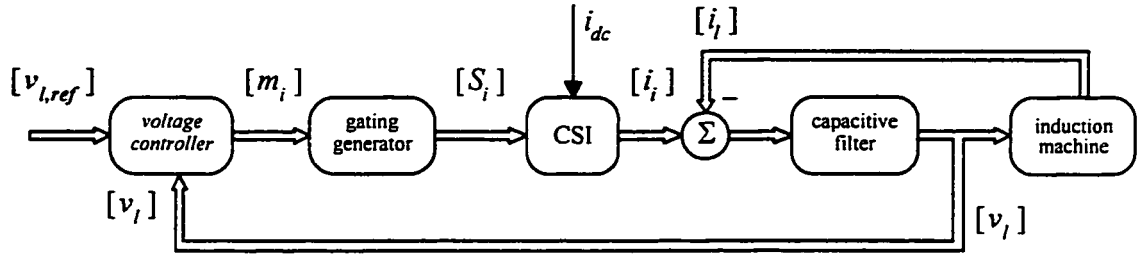


Fig. D.1 ac drive motor voltage control diagram, Section 5

D.2 EQUIVALENT CIRCUITS AND MODELS

An equivalent per phase circuit of the machine for small signal analysis is depicted in Fig. A.5(b). Therefore, the simplified transfer function becomes,

$$\frac{v_{lk}(s)}{i_{lk}(s)} = \frac{R_a R_r + s[R_r L_M + R_a(L_r + L_M) + R_r L_a] + s^2[L_r L_M + L_a(L_r + L_M)]}{R_r + s(L_r + L_M)} \quad \text{V/A (D.1)}$$

The capacitive filter behaves as an integrator ($1/C_f s$) and the current source inverter in combination with the gating generator acts as a current amplifier. Therefore, if the dc link current is considered constant (I_{dc}), $L_M >> L_r$, and $L_M >> L_a$, the open loop

transfer function becomes,

$$\frac{v_{lk}(s)}{m_{ik}(s)} = I_{dc}\frac{R_a R_r + sL_M(R_r+R_a)+s^2L_M(L_r+L_a)}{R_r+s(L_M+C_iR_rR_a)+s^2C_iL_M(R_r+R_a)+s^3C_iL_M(L_a+L_r)} \quad \text{V} \quad \text{(D.2)}$$

The above expression contains one resonance, which is given approximately by,

$$f_{ir} = \frac{1}{2\pi\sqrt{C_i(L_a+L_r)}} \quad \text{Hz} \quad \text{(D.3)}$$

Finally, the PI controller can be represented by,

$$\frac{m_{ik}(s)}{e_{ik}(s)} = k_{vl}\frac{1+sT_{vl}}{sT_{vl}} \quad \text{1/V} \quad \text{(D.4)}$$

The total open loop transfer function is given by the product of (D.2) and (D.4).

D.3 TRANSFER FUNCTION PLOTS

The different transfer functions are depicted in Fig. D.2. Specifically, Fig. D.2(a) shows the total open loop case and Fig. D.2(b) the closed loop case. It can be seen that the resonances are effectively attenuated by the feedback action.

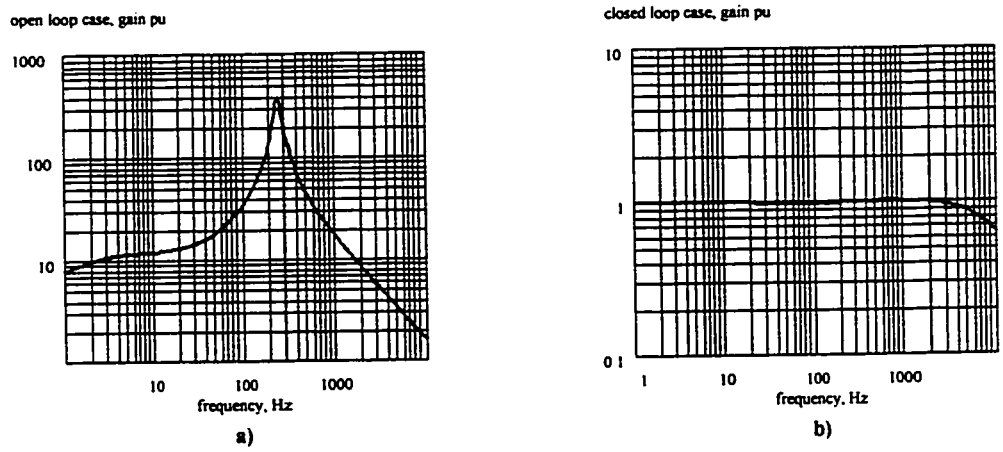
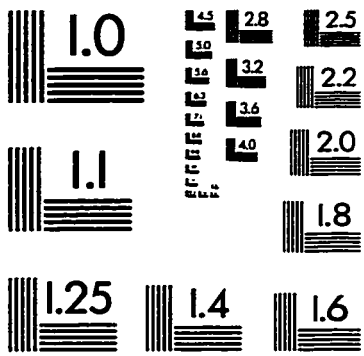
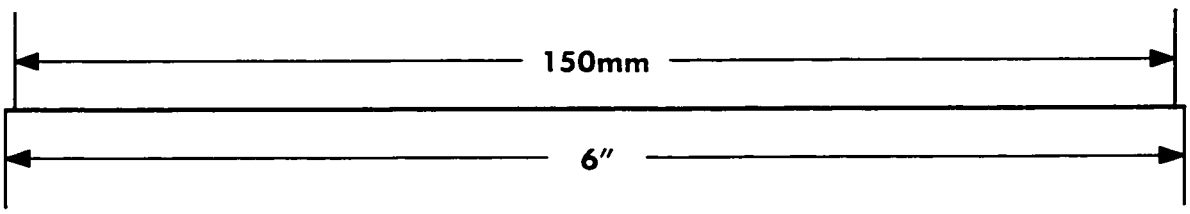


Fig. D.2 ac drive transfer functions, Section 5.

a) open loop case. **b)** closed loop case. $R_a = 0.6\ \Omega$, $R_r = 0.6\ \Omega$, $L_a = 2.12$ mH, $L_r = 2.12$ mH, $L_M = 53$ mH, $C_i = 100\ \mu$F, $I_{dc} = 10$ A, $k_{vl} = 0.5$, $T_{vl} = 1$ ms.

IMAGE EVALUATION
TEST TARGET (QA-3)





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