Design, Fabrication and Testing of Silicon Interdigitated Back Contact (IBC) Solar Cells

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ABSTRACT

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The Interdigitated Back Contact (IBC) solar cell relocates the classical cell's front p-n junction to its rear surface. In this manner, the device's optical and electrical characteristics are decoupled, thereby allowing their separate optimization. This thesis describes the work done in implementing a process sequence for IBC solar cell fabrication at Concordia's Microelectronics Laboratory.

In anticipation of the IBC design's more stringent infrastructure and process requirements, modifications were first made to the cleanroom facilities and to the silicon processing technology. Changes made to the latter included the adoption of more effective wafer cleaning, photolithography and p-n junction-formation procedures. A 4-mask IBC process sequence was subsequently developed which included Van der Pauw, Contact Resistance and Contact String test structures in its design to facilitate post-process testing procedures.

The sequence yielded devices with (dark) reverse saturation currents on the order of 2 nA, fill factors ranging from 72% to 74%, series resistances of approximately 8 ohms and efficiencies of 1% (AM2 spectrum). Photoconductive decay measurements revealed that the devices' photogenerated minority carriers had effective lifetimes of about 55 μs and therefore, diffusion lengths of approximately 260 μm. This is likely due to the high wafer cooling rates that were used subsequent to high temperature processing. The cells' low measured efficiency is therefore due to low minority carrier lifetime in the bulk since short diffusion lengths imply that only a small percentage of the generated carriers are collected by the rear-contacted junction.

ACKNOWLEDGEMENTS

I should begin by thanking Dr. B.A. Lombos for his enthusiasm and optimism during the early stages of this work.

Over the last two years, circumstances forced me at times to adopt a less than ideal attitude towards research and towards life in general. Dr. L.M. Landsberger and Dr. M. Kahrizi successfully pulled me through these moments by offering many helpful suggestions and much encouragement. This work could never have been completed without their unrelenting support.

In addition to providing me with the minority carrier lifetime data, Yacouba Diawara of Ecole Polytechnique (Montreal, Quebec) helped me with numerous experiments and offered many helpful insights into the inner workings of photovoltaic devices. For this I am deeply indebted to him.

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I owe most thanks to my family and friends who managed to put up with me over the last three years and who also managed to cheer me up when nothing seemed to be going right. Many thanks go to Grace for having encouraged me during the last year, especially during the last three months when I essentially transformed myself into an anti-social hermit.

DEDICATION

This work is dedicated to the memory of Dr. P.D. Ziogas and Dr. A.J. Saber.

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List of Symbols

A	Effective p-n junction area (cm^2)
α	Absorption coefficient (cm^{-1})
B	Parabolic oxidation rate constant ($\mu m^2/hr$)
c	Speed of light (2.998×10^8 m/sec)
D_B	Boron diffusion coefficient (cm^2/sec)
D_P	Phosphorus diffusion coefficient (cm^2/sec)
D_{it}	Density of interface states cm^{-2}
D_n	Electron diffusion constant (cm^2/sec)
D_p	Hole diffusion constant (cm^2/sec)
ΔR_p	Projected standard deviation (m)
Δp_n	Injected hole carrier density in n-type bulk (cm^{-3})
Δn_n	Injected electron carrier density in n-type bulk (cm^{-3})
E	Photon energy (eV)

E_F Fermi level (eV)

E_{Fn} Fermi level on n-side of p-n junction (eV)

E_{Fp} Fermi level on p-side of p-n junction (eV)

ϵ_o Permittivity of free space (8.8542×10^{-12} H/m)

$q\Phi$ Work function (eV)

$q\Phi_M$ Metal work function (eV)

$q\Phi_S$ Silicon work function (eV)

$q\chi$ Electron affinity (eV)

FF Fill factor

G Free carrier optical generation rate (carriers/$cm^3 \cdot$ sec)

Γ Photon flux (photons/$cm^2 \cdot$ sec)

I_L Resultant current due to optical excitation (A)

I_m Current at maximum power point (A)

I_s Diode reverse saturation current (A)

I_{sc} Short circuit current (A)

J Current density (A/cm^2)

J_p Hole current density (A/cm^2)

J_s Diode reverse saturation current density (A/cm^2)

k Boltzmann's constant (8.62×10^{-5} eV/°K)

λ Wavelength (μm)

L_p Hole diffusion length (m)

n_i Si intrinsic carrier concentration (1.5×10^{10} cm^{-3} @ 300 °K)

n_n Equilibrium majority carrier density (cm^{-3})

n_{po} Thermal equilibrium electron minority carrier density (cm^{-3})

N_a Acceptor doping level (cm^{-3})

N_B Boron doping concentration (cm^{-3})

N_{BG} Background doping concentration (cm^{-3})

N_d Donor doping level (cm^{-3})

N_D Doping concentration (cm^{-3})

N_{it} Interface states

N_o Surface doping concentration (cm^{-3})

N_P Phosphorus doping concentration (cm^{-3})

N_{st} Number of surface trapping centres/unit area (cm^{-2})

η Conversion efficiency

η_{air} Refractive index for air

η_{Si} Refractive index for silicon

η_{SiO_2} Refractive index for SiO_2

p_n Hole minority carrier density (cm^{-3})

p_{no} Thermal equilibrium hole minority carrier density (cm^{-3})

P_m Maximum developed power (W)

q Electron charge (1 eV)

Q_B Boron dose (cm^{-2})

Q_f Fixed oxide charge

Q_p Implanted dose that penetrates implant mask (cm^{-2})

Q_P Phosphorus dose (cm^{-2})

R Reflection coefficient

R_c Contact resistance (Ω)

R_p Projected ion implantation range (m)

R_s Sheet resistance ($\Omega/\square$)

R_{ser} Solar cell series resistance (Ω)

R_{sh} Solar cell shunt resistance (Ω)

σ Average conductivity $(\Omega \cdot cm)^{-1}$

σ_p Capture cross section of hole trapping centres (cm_2)

S Surface recombination velocity (cm/sec)

T Temperature (°K)

τ_{bulk} Bulk carrier lifetime (sec)

τ_o Average bulk carrier lifetime: $(\tau_p + \tau_n)/2$ (sec)

τ_{eff} Effective carrier lifetime (including τ_{bulk} and S) (sec)

τ_n Bulk electron minority carrier lifetime (sec)

τ_p Bulk hole minority carrier lifetime (sec)

μ_o Permeability of free space ($4\pi x10^{-7}$ H/m)

μ_p Hole mobility ($cm^2/v \cdot sec$)

U_p Excess hole recombination rate ($carriers/cm^3 \cdot sec$)

v_{th} Carrier thermal velocity (cm/sec)

V_m Voltage at maximum power point (V)

V_o Built-in potential (V)

V_{oc} Open circuit voltage (V)

W Transistion region width (cm)

x_j Junction depth (m)

Chapter 1
Introduction

Over the last decade, much work has gone into the development of more efficient photovoltaic energy conversion systems. Research groups across the world have been developing novel solar cell structures [1,2,3,4,5,6] that make use of new materials [7] and that have significantly improved solar cell conversion efficiency.

In 1984, the optimal conversion efficiency for conventional single crystal silicon solar cells was approximately 15 percent [8]. With the development of new process technologies and with the implementation of new designs, conversion efficiencies as high as 28 percent under concentrated sunlight have been reported [9]. The attainment of such high efficiencies is in large part due to the development of more elaborate, non-conventional cell configurations that allow for the optimization of the electrical and optical properties of these

devices. One such design is the Interdigitated Back Contact (IBC) silicon solar cell.

1.1 Conventional vs. IBC Solar Cell Design

Any device capable of photovoltaic action must be composed of essentially three components. These include:

- an **absorber material** in which light-induced transitions create mobile charge carriers that are free to move about in the material.

- an **electrostatic field** in the absorber that separates and sweeps out the photo-generated charge carriers, thus creating a current density, J, through the material.

- **ohmic contacts** to the absorber on either side of the field which allow the internally produced photocurrent to be introduced into an external circuit.

In addition to these components, an anti-reflection coating is also usually placed on the device's exposed surface so as to minimize the fraction of photons incident on the cell that are reflected rather than transmitted into the absorber.

Fig. 1.1 shows a conventional silicon homojunction cell design composed of a p(or n)-type silicon substrate acting as the absorber material [10, pp. 792-806]. An n(or p)-type diffusion made on the device's front surface forms a p-n

homojunction in the substrate which, due to the difference in doping, causes the creation of a space charge region at the junction. The space charge region establishes an electrostatic potential between the n and p regions and thus creates the required electrostatic field in the substrate.

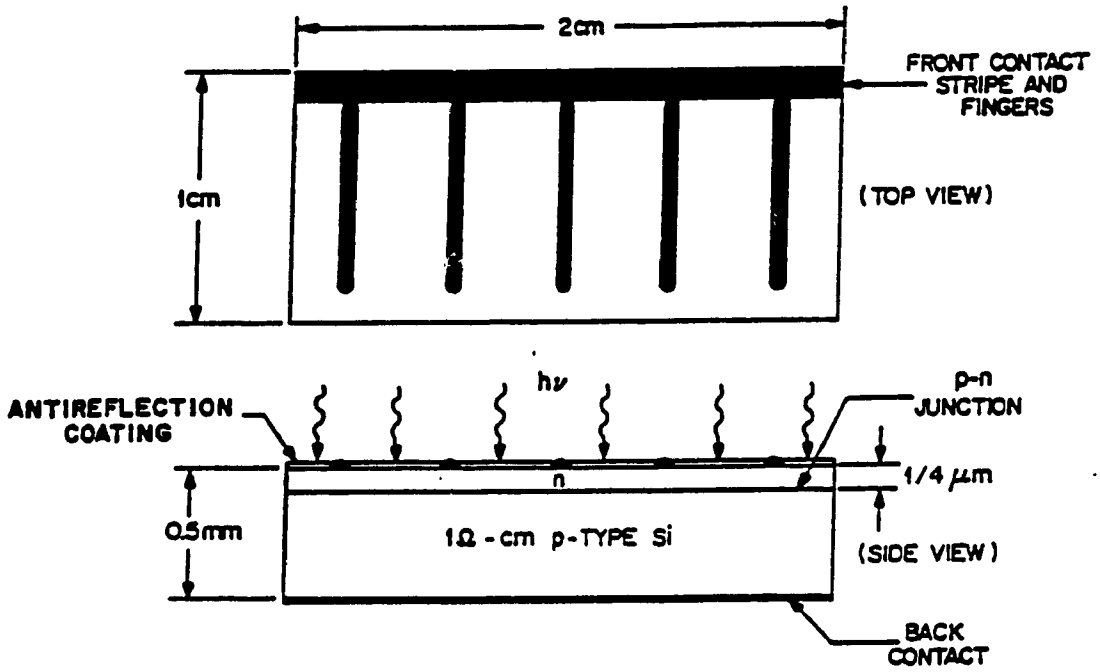


Figure 1.1: Conventional silicon solar cell design.

Photons of sufficient energy impinging on the cell's front surface create electron-hole pairs throughout the substrate. Some of these free carriers are swept across the junction and consequently give rise to the development of a photocurrent through the absorber. In order to introduce this current into the external circuit to which the device may be connected, ohmic contacts are

formed on the device's n and p-type regions. In the case of the device illustrated in Fig. 1.1, the p-type contact is made to the structure's backside and therefore covers its entire rear surface, while the n-type contact, in the form of a finger pattern, lies on the cell's front surface. The front contact is designed in this pattern such that there is sufficient area uncovered by metal to allow the incident photons to reach the silicon substrate.

The energy of a photon having a wavelength, λ, is given by [11, pp. 30-31]:

$$E = h\frac{c}{\lambda} \tag{1.1}$$

where

h = Planck's constant = 4.14×10^{-15} eV· sec
c = speed of light = 2.998×10^{8} m/sec

Since silicon has a bandgap of 1.11 eV, incident photons having a wavelength of 1.1 μm or less will have sufficient energy to create photo-generated carriers in the cell's bulk. Assuming for the moment that silicon has a maximum response over the spectral range from $\lambda = 0.35$ μm to 1.1 μm [12, p. 271], it can be shown that over this range, bare Si has a reflection coefficient ranging from approximately 30 to 55 percent [13, p. 198]. In an effort to reduce the device's front surface reflectivity to more reasonable values of 3 to 10 percent, anti-reflection (AR) coatings [1,2] are commonly used to couple light more efficiently into the cell structure. In the classical cell shown in Fig. 1.1,

the coating is formed at the cell's front surface, between the metal contact fingers.

From this discussion, it becomes apparent that a dilemma is reached when trying to minimize the front contact's shadowing effect by making the contact strings as thin as possible. In doing so, the front contact's electrical resistance is increased and any improvement offered by the minimization of the shadow losses is effectively negated. The main advantage offered by the Interdigitated Back Contact (IBC) cell is the decoupling of the electrical and optical properties of the conventional solar cell layout. Fig. 1.2 shows a typical IBC silicon solar cell structure [14].

In this design, the substrate is usually lightly doped and must have a high minority-carrier lifetime. Rather than creating a junction across the device's entire front surface, alternating p and n diffusions are made in a finger pattern at the rear surface, to which ohmic contacts are subsequently formed. In this configuration, charge carriers generated in the bulk by absorption of photons must diffuse to the back of the cell before they can be collected by the electrostatic field at the p-n junctions. Thus, the device's operation depends strongly on the properties of the silicon substrate, since the lifetime of the generated minority carriers must be kept high compared to the lifetime requirements of conventional cells [2,5].

The relocation of the front-grid contact to the device's rear surface offers two obvious advantages. Primarily, the ohmic contacts may be optimized to maximize their electrical performance and secondly, the cell's front surface may

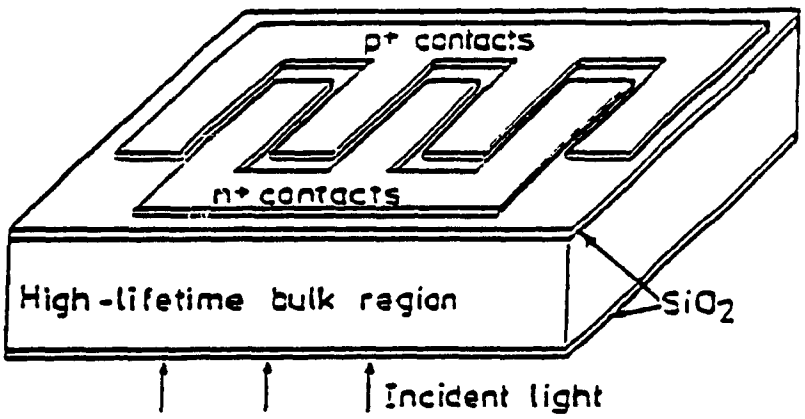


Figure 1.2: IBC solar cell structure.

be optimized to maximize photon capture over the spectral range of interest.

1.2 Organization

This thesis begins in chapter 2 with several theoretical considerations relevant to IBC solar cell design and performance. Topics that are discussed

include spectral response, static junction characteristics and current-voltage characteristics under dark and illuminated conditions.

Chapter 3 begins with a general description of the facilities needed for integrated circuit fabrication. Topics that are discussed include air quality, gowning practices, and water, gas and chemical requirements in the facility. This is followed with a presentation of the wafer cleaning, photolithography and boron diffusion processes that are in place in Concordia's Microelectronics lab.

Chapter 4 discusses the 4-level mask design and the process sequence that was developed for IBC cell fabrication. The mask layouts including test structures are presented. This is followed by a detailed description of the process schedules and conditions that were used to fabricate several functioning IBC solar cells.

Chapter 5 lists the experimental results that were obtained from one of the better devices. Preliminary data generated from measurements made with the on-chip test structures is first discussed, followed by a study of the cell's dark and illuminated I-V characteristics. The chapter concludes with a discussion of the effect of minority carrier lifetime on device performance.

The last chapter gives a summary of the work done in designing and fabricating IBC solar cells at Concordia. This is followed by a list of improvements that could be made to further improve device performance in the future.

Chapter 2
Fundamental Design Considerations

The physical layout of the IBC solar cell structure under consideration is shown in Fig. 2.1. As was discussed in chapter 1, the design's most salient feature is that it relocates the classical cell's front grid and junction to its rear surface, thereby allowing the separate optimization of its optical and electrical properties. In the discussion that follows, the structure's optical design criteria are discussed, followed by an analysis of its back-contacted p-n junctions' electrical characteristics.

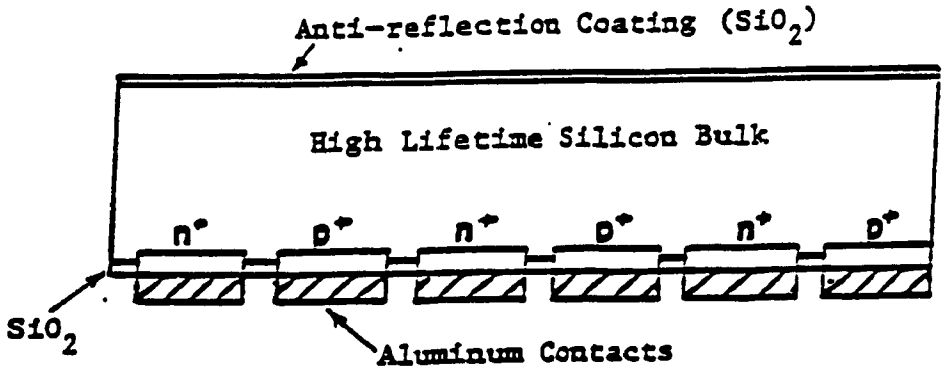


Figure 2.1: Detailed IBC solar cell structure.

2.1 Optical Design Considerations

Two parameters should be considered in designing the IBC structure's optical layout: (1) the bulk absorber material and (2) the anti-reflection coating. A bulk absorber material must be chosen and configured so that photons incident upon its surface will be absorbed by the bulk, generating free carriers within it.

An anti-reflection coating must be contrived which will reduce the number of photons that are reflected rather than transmitted into the bulk material.

2.1.1 Bulk Absorber Material

Fig. 2.2 shows the solar energy spectrum under air mass zero (AM0) and air mass two (AM2) conditions [15, p. 3]. The AM0 curve depicts the solar energy distribution outside the earth's atmosphere, whereas the AM2 curve describes the distribution at the earth's surface under average weather conditions. From this curve, it can be seen that the photon flux is maximum for wavelengths ranging from approximately $\lambda = 0.5\ \mu m$ to $\lambda = 0.9\ \mu m$.

If we designate the photon flux incident on a semiconductor absorbing medium as $\Gamma_o(\lambda)$ *(photons/cm^2·sec)*, the remaining flux at a distance x beneath its surface is given by [12, p. 48]:

$$\Gamma(\lambda,x) = \Gamma_o(\lambda)e^{-\alpha(\lambda)x} \tag{2.1}$$

where $\alpha(\lambda)$ is the absorption coefficient of the semiconductor as a function of wavelength.

Thus, at a depth $x = 1/\alpha(\lambda)$ in the semiconductor, 63 percent of the transmitted photon flux (incident photons that have not been reflected at the

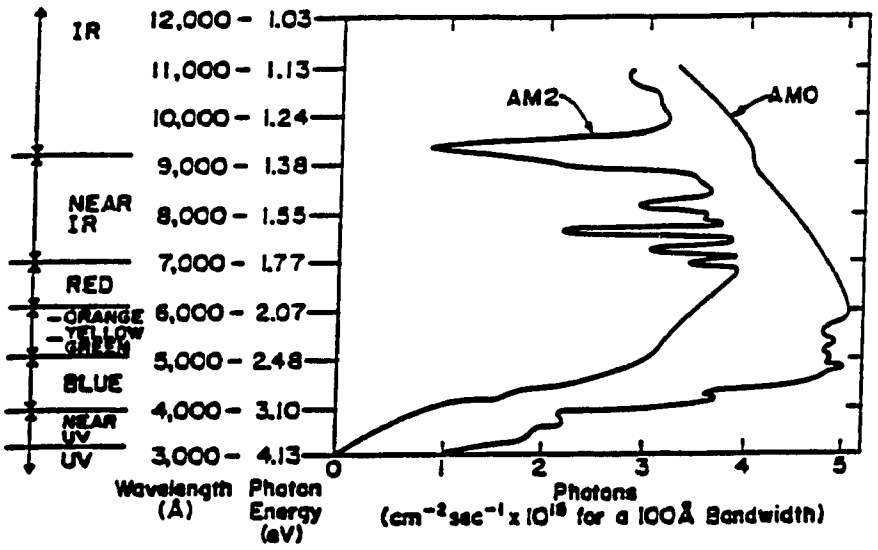


Figure 2.2: Solar energy spectrum for AM0 and AM2 conditions.

semiconductor surface) has been absorbed by the bulk and has generated free carriers within it. In the case of intrinsic absorption in which no traps lie within the semiconductor energy gap, the *free carrier generation rate*, $G(\lambda)$ *(carriers/cm³ · sec)*, due to a photon flux of a given frequency is [12, p. 48]:

$$G(\lambda,x) = \frac{-d\Gamma(\lambda)}{dx}$$

$$= \alpha(\lambda)\,\Gamma_o(\lambda)\,e^{-\alpha(\lambda)x}$$

$$= \alpha(\lambda)\,\Gamma(\lambda,x) \qquad (2.2)$$

Thus the number of carriers generated by photons of a given wavelength is very much dependent on the absorption coefficient at that wavelength for the bulk material in question. A plot of the room temperature absorption coefficient versus wavelength for silicon is shown in Fig. 2.3 [13, p. 187]. Using values from this plot and equation (2.1), the minimum absorber thickness needed to absorb most of the useful solar energy spectrum may be determined. Referring to the values listed in table 2.1 (which are obtained from figure 2.3), it can be concluded that to absorb at least 95% of the photons having a wavelength of $\lambda = 0.9\ \mu m$, the silicon substrate must be designed to have a minimum thickness, x_{min}, of:

$$\frac{\Gamma(\lambda = 0.9, x_{min})}{\Gamma_o(\lambda = 0.9)} = 0.05 = e^{-\alpha(\lambda = 0.9) \cdot x_{min}}$$

$$3 = 4x10^2 cm^{-1} \cdot x_{min}$$

$$x_{min} = 75\ \mu m$$

A greater percentage of the higher energy photons will obviously be absorbed by a silicon substrate of this thickness due to the photons' correspondingly larger absorption coefficients in the silicon.

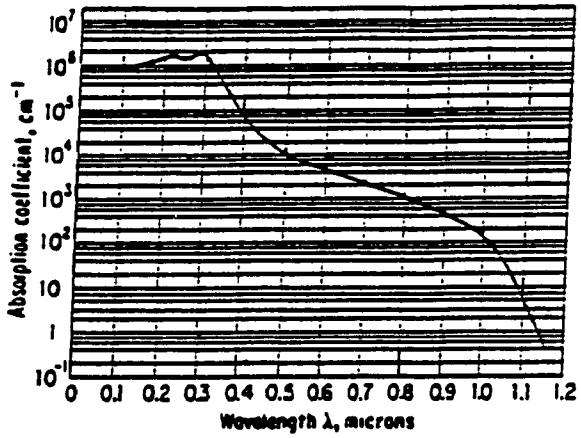


Figure 2.3: Room temperature absorption coefficient vs. wavelength for Si.

Table 2.1: Room temperature absorption coefficients for silicon.

λ [μm]	$\alpha(\lambda)$ [cm^{-1}]	absorption length $1/\alpha$ [μm]
1.1	4	2500
1.0	1.3×10^2	77
0.9	4.0×10^2	25
0.8	1.0×10^3	10
0.7	2.0×10^3	5
0.6	4.5×10^3	2.22
0.5	1.0×10^4	1.00
0.4	7.0×10^4	0.14
0.3	1.7×10^6	0.01
0.2	1.7×10^6	0.01
0.1	8.0×10^5	0.01

Having determined the minimum silicon substrate thickness needed to absorb a majority of the photons incident on its front surface, the average distance travelled by the photogenerated carriers within the bulk will now be determined. In doing so, we assume an n-type bulk and consequently, we consider the one-dimensional continuity equation for holes [10, pp. 51-57]:

$$\frac{\partial p_n}{\partial t} = G_p(\lambda,x) - U_p(x) - \frac{1}{q}\frac{\partial J_p}{\partial x} \tag{2.3}$$

where

$\frac{\partial p_n}{\partial t}$ = average rate of hole build-up in n-type bulk

$G_p(\lambda,x)$ = hole generation rate in the n-type bulk due to optical excitation

$U_p(x)$ = hole recombination rate in bulk

J_p = hole current density in bulk due to generated holes

The optical carrier generation rate, $G(\lambda,x)$, should not be confused with the thermal carrier generation rate, g, occurring naturally in silicon at temperatures above 0 °K. Under steady state conditions (with no external sources of excitation), thermal processes within the semiconductor bulk give rise to a carrier generation rate which is balanced by a carrier recombination rate, r. However, when photons are allowed to impinge upon the semiconductor surface, an optical generation rate, G, is established in the material in addition to the thermal rate. Relation (2.3) is concerned with the optical carrier

generation rate, G, and the recombination rate of these excess carriers, U, in the semiconductor bulk under illumination.

In one dimension, the hole current density in the bulk due to the generated holes is given by [10, pp. 51-57]:

$$J_p(x) = q\mu_p p_n(x)\mathscr{E}(x) - qD_p\frac{\partial p_n(x)}{\partial x} \tag{2.4}$$

where

D_p = hole diffusion constant = $kT\mu_p/q$ [cm^2/sec]
μ_p = hole mobility [$cm^2/V\cdot sec$]
T = temperature [°K]
q = electron charge [$1.6x10^{-19}$ C; 1eV]
k = Boltzmann's constant [$8.62x10^{-5}$ eV/°K]

From equation (2.4), it can be seen that the hole current density is composed of a drift component which arises from an externally applied electric field across the bulk, and a diffusion component caused by the excess carrier concentration gradient that exists between the device's front and rear surface.

For the system under consideration, it is assumed that the following conditions prevail:

1. The device is operated under one-sun conditions. Thus, the injected carrier density, $\Delta p_n \simeq \Delta n_n$ (= 10^{12} cm^{-3} under AM1.5 conditions [12, p. 70]), will be much less than the equilibrium majority carrier density, n_n (≃ substrate doping concentration ≃ $10^{14} \rightarrow 10^{15}$ cm^{-3}). Under these *low-injection* conditions, U_p can be approximated by:

$$U_p = \frac{p_n - p_{no}}{\tau_p} \tag{2.5}$$

where

p_n = hole minority carrier density [cm^{-3}]
p_{no} = thermal equilibrium hole minority carrier density [cm^{-3}]
τ_p = hole minority carrier lifetime [sec]

2. There is no established electric field between the structure's front and rear surface. The drift component of the hole current density may therefore be neglected and equation (2.4) may be simplified to:

$$J_p(x) = -qD_p \frac{\partial p_n(x)}{\partial x} \tag{2.6}$$

Under these conditions, relation (2.3) reduces to:

$$\frac{\partial p_n}{\partial t} = G_p(\lambda,x) - \frac{p_n - p_{no}}{\tau_p} + D_p \frac{\partial^2 p_n(x)}{\partial x^2} \tag{2.7}$$

It was shown earlier that a majority of the photons incident on a silicon substrate are absorbed within a depth of approximately 75 μm into the bulk. If it is assumed that the device's thickness, w, is much larger than this distance, then the hole optical generation rate in the n-type bulk, G_p, under steady state conditions may be set to zero in equation (2.7):

$$\frac{\partial p_n}{\partial t} = 0 = -\frac{p_n - p_{no}}{\tau_p} + D_p \frac{\partial^2 p_n(x)}{\partial x^2}$$

$$\frac{\partial^2 p_n(x)}{\partial x^2} = \frac{p_n - p_{no}}{D_p \tau_p} \qquad (2.8)$$

The boundary conditions that apply to the system under consideration are (refer to Fig. 2.4 [10, pp. 51-57]):

1. $p_n(x=0)$ = constant = Δp_n
2. $p_n(x=w) = p_{no}$ (assuming all carriers get collected at or very close to the device's rear surface)

and the solution to equation (2.8) is [10, pp. 51-57]:

$$p_n(x) = p_{no} + (\Delta p_n - p_{no}) \left[\frac{\sinh \frac{w-x}{L_p}}{\sinh \frac{w}{L_p}} \right] \qquad (2.9)$$

where

$$L_p = \textit{HOLE DIFFUSION LENGTH} = \sqrt{D_p \tau_p} \qquad (2.10)$$

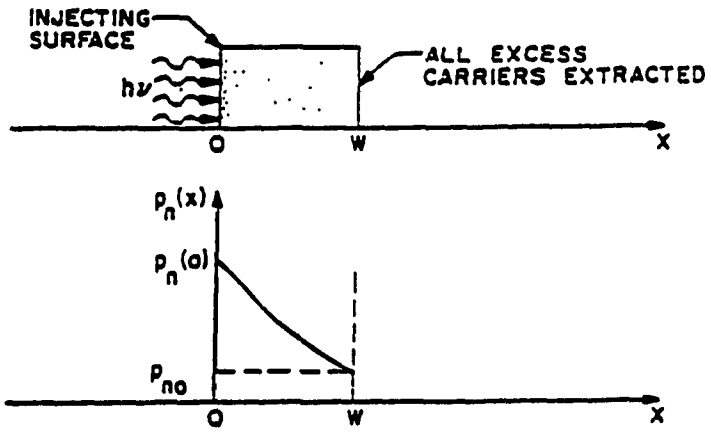


Figure 2.4: Steady state carrier injection from one side.

Diffusion length is defined as the average distance over which the original photogenerated carrier concentration decreases to 37% of its initial value. Thus, the hole diffusion length, L_p, can be used as an approximation of the average distance travelled by a generated hole before it recombines with an electron. Given the IBC design's structure, it is evident that L_p must be made as large as possible to maximize the number of carriers collected by the junctions located at the device's rear surface.

For a given substrate doping concentration, D_p, the diffusion constant for holes in the bulk silicon, can be approximated by a constant. An n-type silicon substrate having a resistivity of 10 $\Omega \cdot$ cm (doping concentration $\simeq 4.5 \times 10^{14}$

phosphorus atoms/cm^3) has a typical hole mobility of μ_p = 490 cm^2/V· sec [16]. Thus, from the *Einstein Relation*,

$$D_p = \frac{kT\mu_p}{q} \tag{2.11}$$

where

$k = 8.62 \times 10^{-5}$ eV/°K
T = 298 °K
q = 1 eV

we obtain that D_p = 12.59 cm^2/sec.

Table 2.2 lists typical values of hole lifetime and corresponding diffusion lengths given a diffusion constant of D_p = 12.59 cm^2/sec. These values illustrate that if the minority carriers in a sample have a lifetime of 20 μsec, for example, they will diffuse an average distance of about 160 μm in the material before recombining. This can be compared with a sample having a carrier lifetime of 1 msec in which the carriers travel an average distance of about 1.1 mm before recombining. From previous discussions, maximization of minority carrier diffusion length is desirable for the IBC solar cell due to the location of the p-n junctions by design. In practice, L_p is maximized by using substrates with high carrier lifetimes, and process schedules that maintain this high lifetime.

Table 2.2: Calculated values of L_p for several values of τ_p

τ_p (μsec)	L_p (μm)
1.0	36
20	159
100	355
200	502
500	793
1000	1122

Surface Recombination

In addition to carrier recombination occurring deep within the semiconductor bulk, recombination processes also occur at the semiconductor surface because of incompletely bonded surface atoms. Within the bulk, each Si atom forms a covalent bond with four of its nearest neighbours. At the surface however, the atoms can only make three of the four bonds and consequently, one of them is left "dangling". Dangling bonds act as minority carrier trapping centres [17] and give rise to a *surface recombination velocity*, S, that is directly proportional to the number of traps at the surface. This is evident from equation (2.12) which describes the hole surface recombination

velocity, S_p, in the case of an n-type substrate [18]:

$$S_p = \sigma_p v_{th} N_{st} \tag{2.12}$$

where

N_{st} = number of surface trapping centres/unit area
v_{th} = thermal velocity of the carriers $\cong 10^7$ cm/sec at room temperature [16]
σ_p = capture cross section of hole trap centres [cm^2]

Note that the capture cross section, σ_p, is a measure of how close a hole must come to the trap centre for it to be captured.

An excessive surface recombination velocity therefore tends to lower a substrate's effective carrier lifetime, τ_{eff}, even if its bulk lifetime is kept high. Equation (2.13) takes S into account in obtaining τ_{eff} for a silicon substrate having a thickness w [19]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2}{w}S \tag{2.13}$$

This equation was tested [19] by a contactless photoconductive decay method, and was found to be applicable for uniformly (lightly) doped substrates.

It has been demonstrated that an Al/Si interface has a surface recombination velocity that approaches the maximum (detrimental) attainable value for silicon (ie., 10^6 cm/sec) [20]. In the case of an oxidized silicon surface

in which an excess carrier density of 10^{12} cm^{-3} (AM1.5 conditions [12, p. 125]) is induced, however, S ranges from 10^2 to 10^4 cm/sec. Thus, if one considers the backside contact area of the IBC cell which includes both Al/Si and SiO_2/Si regions, an intermediate effective value of S would be applicable in equation (2.13).

The efficiency of modern silicon solar cells is limited by surface recombination. This is the case because process techniques have been developed which maintain the high bulk lifetime characteristics of certain absorber materials (such as float zone silicon - see chapter 4) [21]. Thus, in dealing with the problem of surface recombination, surface passivation techniques have also been developed that significantly reduce the number of carrier traps located at the wafer surface.

As was mentioned above, one method of surface passivation involves the growth of a high quality thermal oxide over the device's entire surface prior to metallization. Subsequent to this, holes are opened in the oxide where aluminum is permitted to come in contact with the diffused regions for the purpose of ohmic contact formation. By proceeding in this manner, the area of silicon in direct contact with aluminum is kept to a minimum, and therefore helps to reduce the effective recombination velocity at the surface.

This method of back-surface passivation presents yet another advantage in that the resulting Si-SiO_2-Al structure at the rear acts as a *back surface reflector* (BSR) which sends any unabsorbed photons back into the silicon bulk [1,27]. This increases the number of free carriers generated in the substrate by

increasing the probability of absorption of longer wavelength photons. Without the BSR, a significant proportion of these photons could pass through the substrate without ever being absorbed.

Two observations should be made concerning the passivating oxide grown on the silicon surface. Referring to the 2-D sketch of the Si-SiO_2 interface shown in Fig. 2.5 [22], it can be seen that even though the passivating oxide reduces the number of trapping centres at the Si surface, traps still remain because not all of the silicon atoms are fully bonded by the grown oxide. These atoms lie at the interface, or very near it in the oxide. Those lying at the interface itself are commonly referred to as interface states, N_{it}, while those lying near the interface in the oxide are referred to as fixed oxide charges, Q_f. In minimizing S, attempts are usually made to reduce the density of these traps even further through special processing techniques.

The density of fixed oxide charges is usually reduced by pulling the wafers from the oxidation furnace in an inert ambient (such as argon or nitrogen) subsequent to oxidation [22]. A more effective procedure leaves the wafers in the inert ambient after the oxidation for periods of up to one hour at the oxidation temperature [21]. This usually reduces the density of fixed charges to values ranging from $1x10^{11}$ to $2x10^{11}$ cm^{-2} while un-annealed wafers that are pulled in an O_2 ambient generally have charge densities of up to $9x10^{11}$ cm^{-2} [22].

Although the density of interface states, D_{it}, is also reduced by the post-

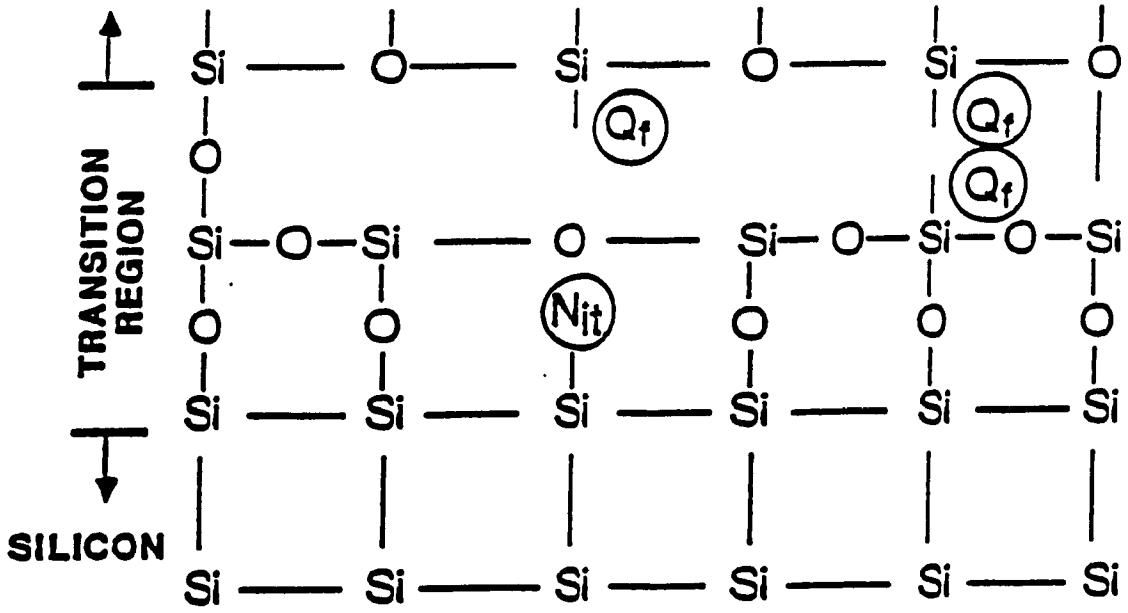


Figure 2.5: 2-D sketch of the Si-SiO_2 interface.

oxidation anneal, it is usually reduced even further by following the wafer metallization sequence with a post-metallization anneal. Anneal times vary from 10 to 30 minutes and are typically done at temperatures ranging from 400 to 450 °C in a forming gas ambient such as hydrogen [21]. The procedure introduces hydrogen atoms at the Si-SiO_2 interface which help to passivate the interface defects [21] and to therefore reduce D_{it}.

Post-oxidation and post-metallization anneals were performed when fabricating the devices for this work. Specific annealing parameters and conditions are described in greater detail in chapter 4.

2.1.2 Choice of Anti-Reflection Coating

Fig. 2.6 shows the room-temperature reflection coefficient versus wavelength for a bare silicon surface [13, p. 198]. In the range of wavelengths from $\lambda = 0.35$ to $1.1\ \mu$m, the reflection coefficient ranges from approximately 30 to 55 percent, indicating that many photons incident on a bare Si surface are reflected rather than transmitted into the bulk.

Anti-reflection (AR) coatings are usually placed at the front surface of photovoltaic devices in an attempt to minimize reflection losses. AR coatings must (1) couple light more efficiently into the absorber and must (2) passivate the device's front surface. Given the last criterion, the most obvious choice for a simple AR coat on silicon is SiO_2. Although more effective double-layer anti-reflection coatings composed of SiO_2/SiN layers have recently been developed [23,24], the design of a simple SiO_2 coat is considered in the following discussion.

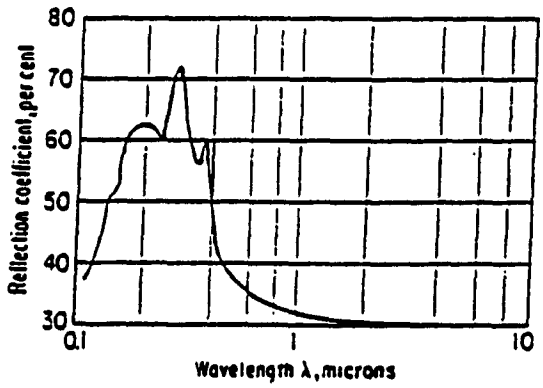


Figure 2.6: Reflection coefficient of Si vs. wavelength.

Equation (2.14) can be used to determine the reflection coefficient, R, at a given wavelength, λ, for an air-SiO_2-Si system having an SiO_2 thickness, d [13, pp. 200, 205, 206]:

$$R = \frac{(r_{12}+r_{23})^2 - 4r_{12}r_{23}\sin^2(2\pi d/\lambda)}{(1+r_{12}r_{23})^2 - 4r_{12}r_{23}\sin^2(2\pi d/\lambda)} \tag{2.14}$$

where

$$r_{12} = \frac{\eta_{air} - \eta_{SiO_2}}{\eta_{air} + \eta_{SiO_2}}$$

$$r_{23} = \frac{\eta_{SiO_2} - \eta_{Si}}{\eta_{SiO_2} + \eta_{Si}}$$

The refractive index for air, η_{air} is given by [25]:

$$\eta_{air} = c\sqrt{\mu_o \epsilon_o} \tag{2.15}$$

where

c = speed of light = 3×10^8 m/sec
μ_o = permeability of free space = $4\pi \times 10^{-7}$ H/m
ϵ_o = permittivity of free space = 8.8542×10^{-12} F/m

The refractive index of silicon dioxide, η_{SiO_2} is 1.46 [10, p. 852]. Silicon has a refractive index that varies significantly over the range of wavelengths from $\lambda = 0.2$ to 1.1 μm as is shown in Fig. 2.7 [13, pp. 200, 205, 206].

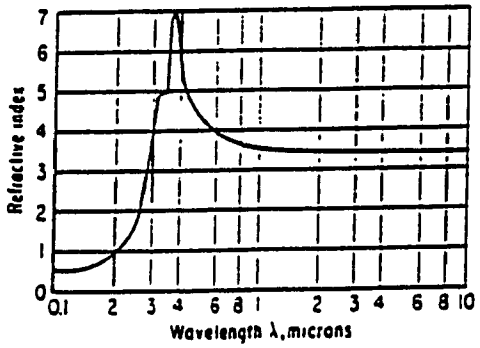


Figure 2.7: Room temperature refractive index of silicon.

Several research groups have used SiO_2 layer thicknesses of 0.1 to 0.12 μm as an AR coat [2,14,26,27]. Specifically, it has been demonstrated that an

SiO_2 thickness of 0.112 μm provides an average reflectance of approximately 20 percent over the spectral range of interest [26]. Using this oxide thickness and the silicon refractive index data plotted in Fig. 2.7, the average reflection coefficient for such a system may be calculated from equation (2.14). Table 2.3 lists several values of reflectance which were calculated using the following constants:

$$\eta_{air} = 1.00$$
$$\eta_{SiO2} = 1.46$$
$$d = 0.112\ \mu m$$

Thus, an SiO_2 thickness of 0.112 μm was used in implementing the front-surface AR coating of the IBC solar cells fabricated for this work.

Table 2.3: Reflectance vs. wavelength for a 0.112 μm SiO_2 AR coat.

λ (μm)	η_{Si}	R (%)
0.35	5.0	23.2
0.40	5.7	22.2
0.45	4.8	14.8
0.50	4.5	11.7
0.55	4.2	13.8
0.60	3.9	13.9
0.65	3.8	15.3
0.70	3.8	17.3
0.75	3.7	18.2
0.80	3.7	19.8
0.85	3.6	20.2
0.90	3.6	21.3
0.95	3.6	21.4
1.00	3.5	22.2
1.05	3.5	23.0
1.10	3.5	23.6

approximate average R = 18.9%

2.2 P-N Junction Characteristics

The following discussion of the IBC solar cell's p-n junction begins with an analysis of its characteristics under static conditions. In doing so, the width of the space charge region as a function f doping levels is derived by using the step-junction approximation.

The junction's I-V characteristics under dark and illuminated conditions are then discussed while considering the effect of reverse saturation current and series resistance on device performance.

The chapter concludes with a presentation of the equations approximating the cell's *maximum developed power*, P_m, its *fill factor*, *FF*, and its *conversion efficiency*, η.

2.2.1 Static characteristics

In creating the numerous finger-type p-n junctions at the IBC cell's rear surface, boron is usually introduced into an n-type bulk through solid-state diffusion. The physical location of the junctions reside at the point where the concentration of phosphorus atoms (for example) in the bulk equals the concentration of the p-type boron atoms in the diffused regions. The doping

difference at these locations causes holes to diffuse from the p to the n-side and electrons to diffuse from the n to the p-side. In addition to establishing a diffusion current in the bulk, this flow of majority carriers leaves behind uncompensated ions on either side of the junction (ie., positive ions on the n-side and negative ions on the p-side) that are fixed within the crystal lattice. The presence of these ions creates a *space charge region* (or *transition region*) in the bulk in which an electric field is established as shown in Fig. 2.8 [11, pp. 136-147].

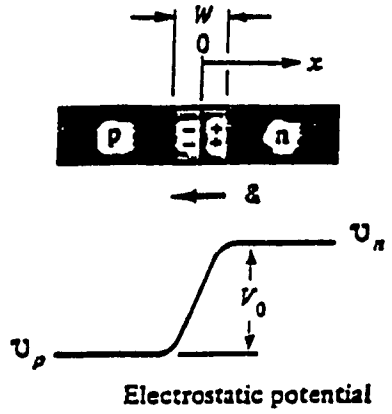


Figure 2.8: Space charge region at p-n junction.

In the presence of this field, minority carriers on either side of the junction are forced to flow across it into the other region. This flow of minority carriers creates a drift current component across the junction which is in a direction opposite to that of the diffusion current. Under equilibrium conditions

(ie, no thermal gradients, no optical excitation and no applied bias), the magnitude of the electric field (and therefore the number of exposed ions) grows until the drift current exactly equals the diffusion current.

It becomes apparent from this discussion that the width of the transition region is largely dependent on the doping levels on either side of the junction. In the case where the p-side doping is several orders of magnitude greater than the n-side doping, the depletion layer width on the n-side, x_{no}, will be many times larger than the layer width on the p-side, x_{po}. This must be the case because an equal number of charges must be uncovered on either side of the junction. Thus for a p^+-n junction, the total transition region width, W, can be approximated as [11, pp. 136-147]:

$$W \approx x_{no} = \left[\frac{2\epsilon V_o}{q}\left(\frac{N_a}{N_d(N_a + N_d)}\right)\right]^{1/2} \tag{2.16}$$

where

$\epsilon = \epsilon_r\epsilon_o$ = permittivity of silicon
$= (11.8)(8.85\text{x}10^{-14}\ \text{F/cm})$
$= 1.04\text{x}10^{-12}\ \text{F/cm}$

$q = 1.60\text{x}10^{-19}\ \text{C}$

N_a = doping on p side

N_d = doping on n side

V_o = built-in potential across the transition region

The built-in potential may be approximated as [11, pp. 136-147]:

$$V_o = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2} \tag{2.17}$$

where

$kT/q = 0.0259$ V

n_i = intrinsic carrier concentration for silicon

$= 1.5 \times 10^{10}$ cm^{-3} @ T = 300 °K

If the n-type doping concentration is assumed to be $N_d = 4.5 \times 10^{14}$ cm^{-3} and if the p-type doping is assumed to be approximately 10^{18} cm^{-3}, equations (2.17) and (2.16) predict a built-in potential of $V_o = 0.73$ V and a transition region width of W = 1.46 μm, respectively.

Thus, if an IBC solar cell is fabricated using a lightly doped n-type substrate with heavily doped p-type diffusions at the rear such that the step-junction approximation used above is valid, it may be concluded that the free carriers generated at the structure's front surface must travel a minimum distance of:

$$l_{min} = W_{cell} - x_j - x_{no} \tag{2.18}$$

where

W_{cell} = cell substrate thickness

X_j = p-n junction depth from rear surface

before they can be collected by the field in the transition region.

This analysis neglects minority carrier generation within the transition region, W, and therefore assumes that W does not change when the device is illuminated. Under highly injected conditions, however, such as when the device is operated under concentrated sunlight, the assumption no longer holds. Carrier generation within the region becomes important under these conditions and ultimately causes a small reduction in the transition layer width.

The devices fabricated for this work are tested under one-sun conditions. Thus, the assumption made above remains valid and it can be concluded that the transition layer width should not vary significantly from the predicted value of 1.46 μm. It should furthermore be noted that the built-in potential predicted by equation (2.17) gives only an upper limit to the device's maximum obtainable open-circuit voltage, V_{oc} (see next section) [15, pp. 182, 183].

2.2.2 I-V Characteristics

The ideal solar cell under illumination may be represented by an equivalent circuit composed of a constant current source, I_L, placed in parallel with the junction (ie., a diode) as shown in Fig. 2.9 [10, pp. 792-806].

The current through the load resistance, R_L, is therefore [28]:

$$I = I_s(e^{qV/kT} - 1) - I_L \tag{2.19}$$

where

I_s = reverse saturation current of ideal junction
I_L = current resulting from optical generation of excess carriers in the bulk
V = operating voltage

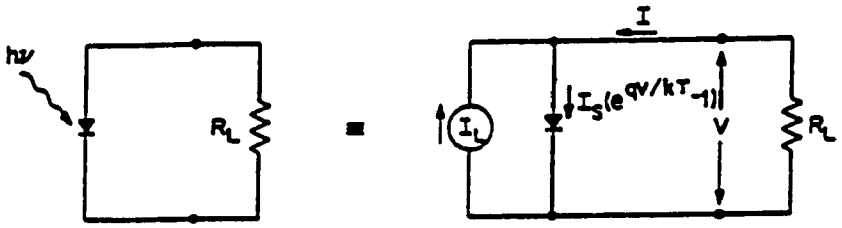


Figure 2.9: Equivalent circuit of ideal solar cell.

Fig. 2.10 plots the ideal I-V characteristics under both illuminated and dark conditions [12, p. 212]. The I-V curve under dark conditions assumes the shape of the classical diode characteristic. Under illuminated conditions however, the curve passes through the fourth quadrant since it is displaced downwards by an amount equal to the generated current, I_L. Hence, power can

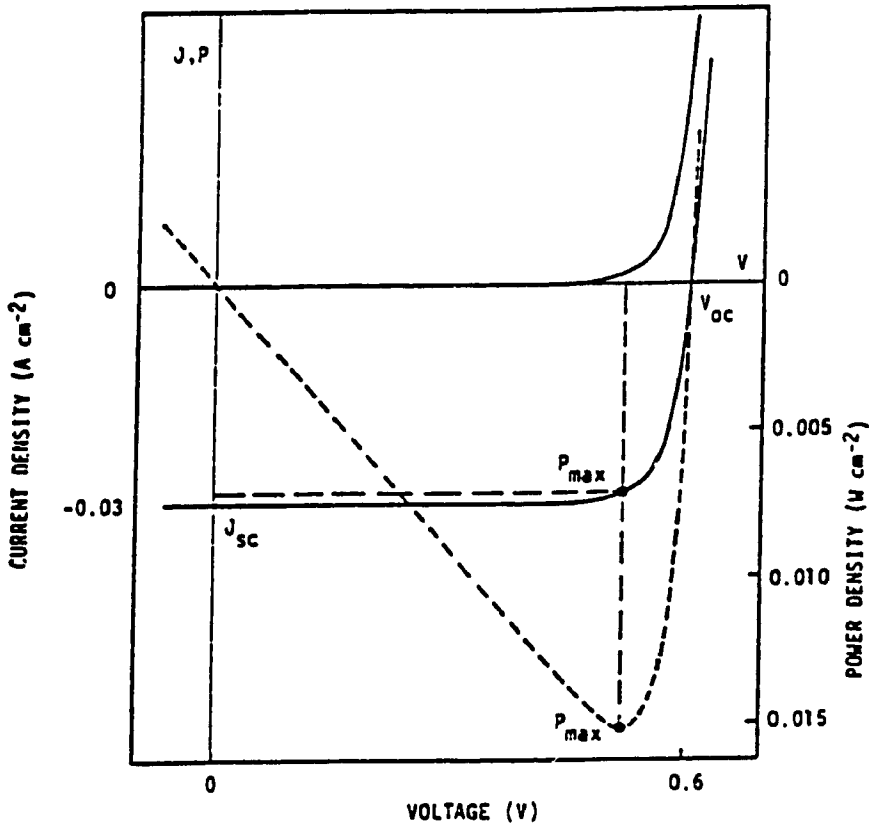


Figure 2.10: Ideal dark and illuminated I-V characteristics.

be extracted from the device when it is illuminated.

When the device is illuminated and its terminals are shorted, it develops a maximum current, I_{sc}. Likewise, when its terminals are left open and it is placed under illumination, the cell develops a maximum voltage, V_{oc}. The

magnitudes of V_{oc} and I_{sc} and the overall shape of the I-V characteristic are in general governed by the photogeneration, transport and loss properties of the solar cell structure as a whole [15, pp. 182, 183].

The magnitude of the open circuit voltage is largely dependent on the magnitude of the reverse saturation current, I_s, as is demonstrated by setting I = 0 in equation (2.19):

$$0 = I_s(e^{qV_{oc}/kT} - 1) - I_L$$

$$e^{qV_{oc}/kT} = \frac{I_L + I_s}{I_s}$$

$$e^{qV_{oc}/kT} \approx \frac{I_L}{I_s}$$

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{I_L}{I_s}\right) \qquad (2.20)$$

Relation (2.20) indicates that V_{oc} can be maximized by minimizing I_s. A simple calculation reveals that a device with an I_s of 10^{-9} A will have an open circuit voltage that is approximately 1.5x larger than a similar device with an I_s of 10^{-6} A.

Essentially two processes give rise to the saturation current across the junction under reverse bias conditions: (1) the thermal generation of electron-hole pairs, EHP's, in the neutral regions and (2) the generation of EHP's in the transition region. The carriers that are generated in the neutral regions and that

successfully diffuse to the space charge region get swept across it. This contributes a diffusion current component to the overall saturation current. The carriers generated within the transition region itself are also swept out of it and therefore contribute a generation current component to I_s. In deriving the magnitude of I_s, both these components should be considered [10, pp. 89-92] as is done in equation (2.21):

$$I_s = A\left(q p_{no}\sqrt{\frac{D_p}{\tau_p}} + q n_{po}\sqrt{\frac{D_n}{\tau_n}}\right) + \frac{q n_i W}{\tau_e} \tag{2.21}$$

where

p_{no} = equilibrium density of holes in n-region
n_{po} = equilibrium density of electrons in p-region
D_p = diffusion constant of holes in n-region
D_n = diffusion constant of electrons in p-region
τ_p = hole lifetime in n-type bulk region
τ_n = electron lifetime in p-type bulk region
A = effective junction area
W = transition region width
τ_e = average bulk carrier lifetime = $(\tau_p+\tau_n)/2$

In the case of the p^+-n junction considered earlier, p_{no} is much greater than n_{po} and equation (2.21) reduces to:

$$I_s \approx q A p_{no}\sqrt{\frac{D_p}{\tau_p}} + \frac{q n_i W}{\tau_e} \tag{2.22}$$

The equilibrium density of holes in the n-type region, p_{no}, may be determined from the *equilibrium condition* by setting n_n equal to N_{BG} where N_{BG} represents the background doping concentration of the n-type substrate [11, pp. 136-147]:

$$p_{no} = \frac{n_i^2}{n_n}$$

$$= \frac{n_i^2}{N_{BG}} \tag{2.23}$$

From equation (2.22), it can be concluded that I_s may be minimized by keeping the carrier lifetimes high. As is discussed further in chapters 4 and 6, this may usually be achieved by choosing a high quality starting material for the substrate and by using process sequences that maintain the high lifetime characteristics of such substrates.

Having discussed the importance of keeping the magnitude of the reverse saturation current to a minimum, the effect of series and shunt resistances on device performance is now considered. If the equivalent circuit of Fig. 2.9 is modified to include R_{ser} and R_{sh}, equation (2.19) becomes:

$$I = I_s[e^{q(V - IR_{ser})/kT} - 1] - I_L + \frac{V - IR_{ser}}{R_{sh}}$$

$$\ln\left[\frac{I + I_L}{I_s} + \frac{V - IR_{ser}}{I_s R_{sh}} + 1\right] = \frac{kT}{q}(V - IR_{ser}) \tag{2.24}$$

Any junction will have a certain amount of shunting current which is caused by, for example, tunnelling at the periphery of the junction plane [12, pp. 70, 125]. The shunt resistance is therefore representative of the sum of all sources of shunting current. For a good quality junction, R_{sh} is usually quite high. However, it can be seen from equation (2.24) that values of shunt resistance even as low as 100 ohms do not significantly change the device's power output [10, pp. 792-806] and therefore, the relevant term may be neglected in equation (2.24) to obtain:

$$I = I_s\left(\exp\left[\frac{q(V - IR_{ser})}{kT}\right] - 1\right) - I_L \tag{2.25}$$

Using equation (2.25), the solar cell output power may be derived as:

$$P = |VI| = I\left[\frac{kT}{q}\ln\left(\frac{I + I_L}{I_s} + 1\right) + IR_{ser}\right] \tag{2.26}$$

From equation (2.26), it can be deduced that, for example, a series resistance on the order of 5 ohms will reduce the relative maximum power developed by the cell to approximately 27% of its maximum achievable output when $R_{ser} = 0$. Fig. 2.11 shows the impact of R_{ser} on the illuminated I-V characteristics [28]. The plot in Fig. 2.12 uses equation (2.26) to plot the relative maximum available power as a function of series resistance [28].

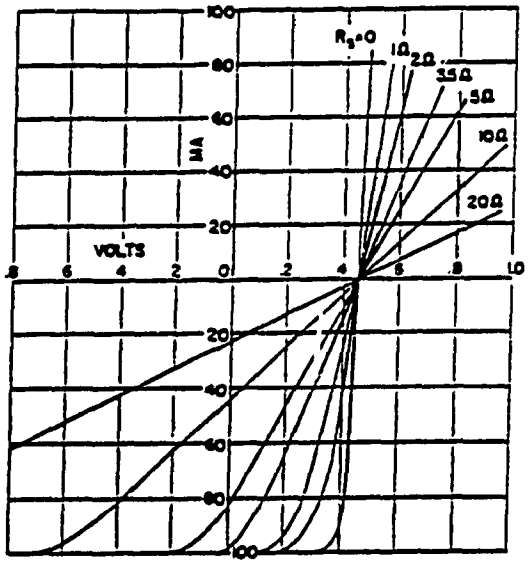


Figure 2.11: Impact of R_{ser} on illuminated I-V characteristics.

Referring once again to Fig. 2.10, we find that there exists a bias point on the illuminated I-V curve at which the cell develops a maximum power, P_{max}:

$$P_{max} = V_m I_m \tag{2.27}$$

where

V_m = voltage at maximum power point
I_m = current at maximum power point

Notice from Fig. 2.11 that an ideal curve will have an almost square shape, whereas the characteristic of a practical device having a finite series

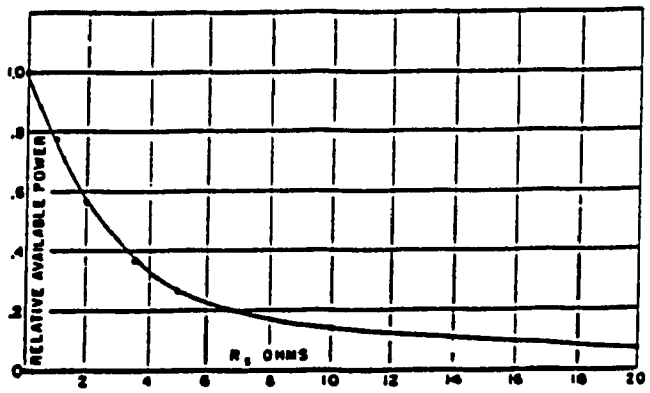


Figure 2.12: Relative maximum power available vs. R_{scr}.

resistance will have a more rounded shape. The maximum power point as defined by equation (2.27) is therefore very much dependent on the shape of the illuminated I-V characteristic. In describing the quality of the shape of the illuminated characteristic, the fill factor, FF, is commonly used [15, pp. 182, 183]:

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \tag{2.28}$$

Typical values for FF range from 0.6 to 0.8 [12, p. 13]. Thus, if a solar

cell's fill factor is maximized, its energy conversion efficiency, η, will also be maximized:

$$\eta = \frac{V_m I_m}{P_{input}} = \frac{FF \cdot I_{sc} V_{oc}}{P_{input}} \tag{2.29}$$

Summary

From the discussion presented above, it can be concluded that a solar cell must be designed to satisfy two criteria in order to maximize its conversion efficiency: (1) a good quality junction must be established within its bulk which maintains a low reverse saturation current, I_s, and (2) process parameters and materials used for its fabrication should keep the structure's series resistance, R_{ser}, to a minimum.

It should furthermore be noted that the magnitude of the current resulting from the optical generation of excess carriers in the bulk is in large part dependent on the number of carriers that "live long enough" and successfully reach the space charge region. If this number is low due to small minority carrier diffusion lengths, L_p (which are in turn due to short lifetimes), the magnitude of the resulting optical generation current, I_L, will also be diminished.

Chapter 3

Laboratory and Process Technology Development

Integrated circuit (IC) fabrication requires stringent control over process conditions and parameters. Hence, the establishment of adequate cleanroom facilities and the development of reproducible process technologies are essential pre-conditions for the fabrication of functional semiconductor devices.

Preliminary fabrication runs of large scale (300 - 400 micron) diodes and crude IBC cell structures in the Microelectronics Laboratory at Concordia University confirmed that problems existed in both of these areas. The frequent contamination of process wafers with visible dust particles and the inability to fabricate devices with acceptable electrical characteristics substantiated these concerns. These observations led to a complete overhaul of the laboratory and to the refinement of the silicon processing procedures prior to the commencement of subsequent IBC fabrication sequences. This chapter details

the results and conclusions drawn from this overhaul.

3.1 Laboratory Development

Contamination in a cleanroom will ultimately affect wafer yield and device performance. The major sources of cleanroom contamination include the following [29]:

1. Air
2. The Production Facility
3. Cleanroom Personnel
4. Process Water
5. Process Chemicals
6. Process Gases

All six of these areas were controlled as described in the following pages.

Air

The air in a busy city typically contains 5 million particles per cubic foot and is thus designated as having a class number of 5 million. In contrast, VLSI

fabrication areas which produce high density circuits with 1 micron linewidths can tolerate particle densities of 10 per cubic foot (class 10) and maximum particle sizes of 0.5 micron [29]. Cleanroom facilities are therefore equipped with dedicated ventilation systems and work stations that filter incoming air continuously and which keep particle densities to within tolerable limits.

The cleanrooms at Concordia University are estimated to be about class 5000 to class 10 000, a reasonable level [40, pp. 14-21] for fabricating devices with minimum linewidths of 10 to 20 microns. This level of air quality is maintained through the use of 99.99% efficient HEPA (high-efficiency particulate attenuation) filters that are installed at the duct outputs into each room. HEPA filters are constructed of a very fragile, porous material that is positioned in an accordion fashion within a sealed enclosure as shown in Fig. 3.1 [29]. Such units are capable of filtering large volumes of air at relatively low airflow velocities in the range of 90 to 100 ft/min [30].

In order to keep external contaminants from entering cleanroom work spaces, the air pressure in these areas must be maintained higher than that of the surrounding work areas. At Concordia, the air pressure in each of the three rooms is controlled by means of a calibration/monitoring unit located at the main entrance to the cleanrooms.

In calibrating the system, the pressure is made highest in the photolithography room where the dust-sensitive process of transferring circuit patterns onto process wafers is performed. The procedure involves the application of a thin layer of photoresist to the wafer and subsequently exposing

Figure 3.1: Internal HEPA filter design.

it to UV light through an appropriate mask. Any airborne particles falling onto the wafers while applying the resin or during exposure will likely cause device failure and will ultimately reduce product yield.

Photoresist application is therefore done in the photolithography room, inside a *horizontal laminar flowhood* (HLF) which is equipped with a separate blower motor/HEPA filter assembly. In this manner, a constant supply of clean, filtered air is ensured during photoresist application and therefore adds reproducibility to the procedure.

The Production Facility

Cleanrooms for semiconductor fabrication must be constructed to satisfy two important criteria: (1) they must keep out external contaminants and (2)

their exposed surfaces must be resistant to a large number of different chemicals. In addressing the first criterion, special attention is paid to the methods used in sealing wall joints, door seals and fixtures, and in satisfying the second criterion, special paints and floor covering materials are used. Thus, in order to achieve standards high enough for processing requirements, a basic room conditioning procedure must be followed. The following describes the procedure that was applied to Concordia's rooms.

Fine cracks in the photolithography room were sealed with plaster prior to the application of paintable, high quality caulking around piping holes, fixtures, wall-to-ceiling joints and wall-to-worktop joints. Before applying the final two coats of epoxy/enamel-based paint, a coat of primer was applied to all exposed surfaces in the two main rooms. Primer ensures adhesion between paint and various materials such as plaster, caulking and underlying paint which may not be compatible with the topcoat.

With the painting completed, the floor tiling was stripped and replaced with a more durable, epoxy-based cement. An appealing feature of this covering is that it eliminates any joints or crevices in which dust particles could become lodged and later become airborne. It also has a high tolerance to many chemicals and thus allows it to be cleaned with harsh solvents if necessary. Before relocating the cleaned equipment back into the rooms, all door seals were also replaced, and all surfaces were wiped with alcohol-soaked cleanroom wipers so as to remove any residues.

In re-installing process equipment, appropriate measures were taken to

ensure that their operation would not affect air quality in the future. For instance, the rotary vacuum pump which supplies vacuum to the mask aligner in the photolithography room did not originally have its exhaust connected to the venting system in the laboratory. The situation resulted in the frequent contamination of process wafers with fine droplets of vacuum pump oil that were apparent when a processed Si sample was viewed under a microscope. This problem was rectified by exhausting any machinery emissions to the lab's main venting system in the laboratory.

With the major pieces of equipment re-installed, the cleanrooms were once again cleaned, and entry into the rooms was subsequently restricted to properly gowned personnel.

Cleanroom Personnel

One of the most serious sources of contamination in a cleanroom environment is personnel. A human being moving at two miles per hour typically gives off up to 5 million particles [40, pp. 14-21] per minute through skin flaking, hair loss and through clothing [29]. People working in cleanrooms must therefore be covered with special clothing prior to entry into these sensitive areas.

Cleanroom garments are made of non-shedding material and are available

in a wide range of styles. For example, class 10 garments as shown in figure 3.2 [29] typically cover the entire body, and since the eyes are a major source of fluid particles, glasses with side shields are also usually worn.

Figure 3.2: Class 10 garments.

Ideally, any cleanroom should have a buffer zone between itself and the surrounding "dirty" environment where this clothing can be put on prior to entry into the main clean work areas. The zone consists of a separate, usually smaller room which is supplied with filtered air and which is also used as a storage area for the garments. In better installations, workers are blown clean with "air showers" located at the entrance to the main rooms.

At Concordia, garments consisting of hair nets, beard covers, overcoats, shoe covers and gloves are worn by all personnel entering the clean areas. The smaller of the three cleanrooms which is connected to the two main rooms is used as the gowning area. This gowning practice has been shown to have a dramatic impact on the cleanliness of the two main work areas.

Once proper facilities have been developed for IC fabrication, it is important that cleanliness in the laboratory be maintained by periodically cleaning the entire facility. Ideally, these cleaning sessions should be carried out on a continuous basis and should involve wiping *all* surfaces with alcohol-soaked cleanroom wipers.

If cleanliness is not maintained, a decrease in wafer yield can be expected due to particle contamination. Fig. 3.3 shows a photograph of an IBC finger pattern that had been fabricated in Concordia's laborartory after the renovations, but two weeks after the facilities had last been cleaned. Close examination of the photograph reveals that the p (wider fingers) and n (thinner fingers) diffusions were shorted out by a dust particle that happened to settle on the wafer sometime during processing. Problems such as these are now avoided by thoroughly cleaning the facilities at least once every week.

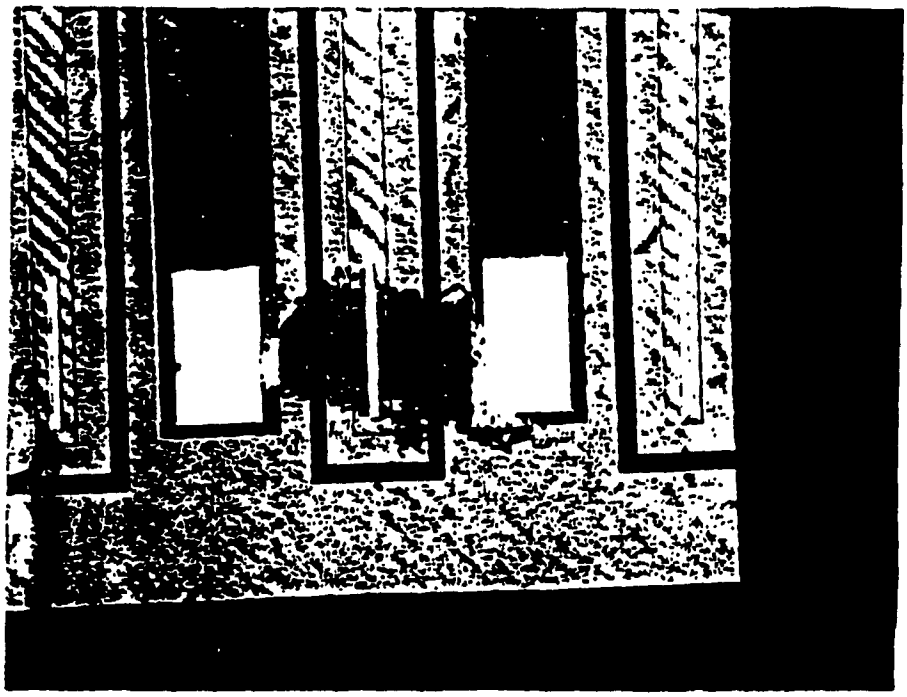


Figure 3.3: P-N junction short caused by dust particle.

Process Water

During the course of fabrication, semiconductor wafers go through many stages of etching, cleaning and photolithography which make use of many different types of acids, bases, and solvents. Each of these steps is usually

followed by several water rinses, and in cases where processing must be suspended for a period of time, the wafers are usually stored under water to minimize their exposure to contaminants. The purity requirements of water used for semiconductor processing therefore usually far exceed the water purity requirements of most other industries.

Water commonly contains contaminants such as sodium, chloride and calcium ions, as well as organic debris, bacteria, chlorine and carbon dioxide [30]. To properly remove these contaminants, water treatment usually begins with a reverse osmosis procedure which typically rejects 90 to 95 percent of the impurities found in most water systems [30]. This treatment is then followed by a deionization procedure which removes ionic contaminants from the water. The pre-treatment of the water via reverse osmosis is essential prior to deionization because the latter procedure does not effectively remove organics and bacteria from the water [30].

In measuring the ion content of the process water, an electrical current is passed through the water and a resistivity rating (in $\Omega \cdot$ cm) is deduced from the reading. Whereas water has a maximum achievable resistivity of 18.3 $M\Omega \cdot$ cm at 25 °C [30], the specification for VLSI processes usually calls for resistivity ratings of up to 18 $M\Omega \cdot$ cm [29].

The water purification system at Concordia is outfitted with a reverse osmosis unit whose output is followed by a deionization system capable of producing 18.3 $M\Omega \cdot$ cm water at a rate of 1.5 litres per minute [30]. A 100 litre storage tank is included in the installation.

Process Chemicals

The chemicals used for wafer processing must be of the highest purity. Industrial chemicals come in essentially four grades including *Commercial, Reagent, Electronic* and *Semiconductor* grade [29]. The first two grades are in general too contaminated, thus electronic or semiconductor grade chemicals are usually used by the semiconductor process industry. In the microelectronics laboratory at Concordia, electronic grade solutions are used throughout all stages of wafer processing.

Process Gases

Gases such as nitrogen, oxygen and hydrogen are used during diffusion, thermal oxidation and annealing procedures. Since these processes are usually carried out at high temperatures (450 - 1150°C), high purity gases must be used to again avoid wafer contamination. The gases used at Concordia are all of *Ultra High Purity Grade.*

3.2 Silicon Process Technology Development

In modifying the laboratory's established silicon process technology for the fabrication of IBC solar cells, close attention was paid to the following three areas:

1. Wafer Cleaning/Drying
2. Photolithography
3. P-N Junction Formation

3.2.1 Wafer Cleaning/Drying

Prior to any high temperature step such as oxidation or diffusion, silicon wafers must be properly cleaned and dried. A widely accepted cleaning procedure is the Reverse-RCA procedure [31]. It consists of the following steps:

1. Soak in boiling H_2SO_4:H_2O_2 (1:1) for 5 minutes
2. Rinse in running deionized (DI) H_2O for 2 minutes
3. Soak in boiling HCl:H_2O_2:H_2O (1:1:5) for 5 minutes
4. Rinse in running DI H_2O for 2 minutes
5. Dip in HF:H_2O (1:50) for 30 seconds
6. Rinse in running DI H_2O for 2 minutes

7. Soak in hot $NH_4OH:H_2O_2:H_2O$ (1:1:5) for 5 minutes
8. Rinse in running DI H_2O for 2 minutes
9. Blow dry with filtered N_2 gas

While other cleaning procedures, for example solvent-only procedures, are effective in removing contaminants found on wafers after lapping and polishing, they do not effectively remove organic films and heavy metals as does the Reverse-RCA procedure [32, p. 44].

3.2.2 Photolithography

Figure 3.4 shows how circuit patterns are transferred to a semiconductor surface through photolithography [33]. Prior to the diffusion of dopants in specific regions on the wafer surface, silicon dioxide (SiO_2) is grown on the sample's entire surface. The appropriate resin is then applied to the wafer, baked, and then exposed to ultraviolet light through a mask. After development, the exposed SiO_2 is etched away, leaving bare silicon wherever the diffusion is to be made. After the photoresist is stripped, the wafer is cleaned and the

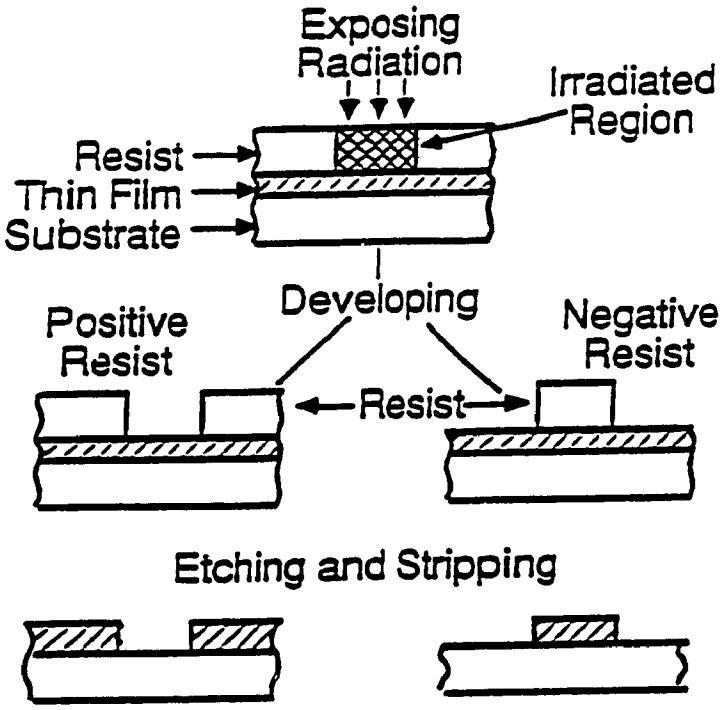


Figure 3.4: Delineating diffusion regions through lithography.

diffusion of p-type or n-type impurities is made at high temperature. P-type or n-type regions are thus formed in the silicon surface only in those areas that were not originally masked by silicon dioxide.

As is shown in Fig. 3.4, either negative or positive photolithography may be used for the process. When using negative photoresists, the UV-exposed

regions become polymerized by the light and resist dissolution by the developer. The unexposed regions are dissolved by the developer and a negative copy of the mask pattern is therefore created on the wafer surface. In the case of positive photoresists, the UV-exposed regions become soluble in the developer and a positive copy of the mask pattern is created on the wafer.

For a variety of reasons, the photolithographic processing described herein uses positive photoresist. Positive photoresists offer the following advantages [33]:

1. High resolution (<0.25 micron features possible)
2. Easily removed with acetone
3. High etch resistance

Unfortunately, positive resists also tend to be very sensitive to processing parameters such as exposure time/intensity, developing time/temperature and baking time/temperature. In fact, the applied films are likely to lift-off during developing or while etching if they are not properly processed.

The following discusses the measures that are taken at Concordia to ensure that (1) the applied films are consistently particle-free, and (2) the films are resistant to the developing and etching solutions used for processing

subsequent to exposure.

Microposit S1350J Photoresist which is manufactured by *Shipley Company Inc.* is used for all photolithography processes at Concordia. In applying the resin to the wafer surface, a syringe equipped with a *Minisart SRP-25* filter is used. These filters are solvent resistant and have a 0.45 micron pore size which help to keep any foreign particles found in the resin from reaching the wafer. Subsequent to exposure, the samples are developed in a solution of *Microposit 352 Developer* which is supplied as a ready to use solution by the manufacturer. The use of this solution which is kept stirred at moderate speed with a magnetic stirrer, ensures development uniformity and also renders the process very reproducible. Prior to exposure however, proper adhesion between the film and the wafer surface must be ensured by using the following sequence in applying the photoresist [34]:

1. Dry wafer in forced-air convection oven at 200°C for 30 minutes.

2. Let cool for 10 minutes.

3. Position wafer on spinner chuck and secure with vacuum.

4. Blow off dust particles with filtered N_2 gas.

5. Apply 4-5 drops of photoresist with filter-equipped syringe.

6. Spin at 3000 r.p.m for 30 seconds.

7. "Soft Bake" in forced-air convection oven for 30 minutes at 95°C.

8. Allow wafer to cool for 10 minutes.

9. Expose to UV light through appropriate mask.

10. Dip in stirred developer solution for 2 minutes.

If problems with photoresist adhesion are apparent during development (ie., the film lifts off), it is likely due to inadequate wafer surface preparation and to excessive humidity levels in the fab area. Under humid conditions, moisture absorbing surface layers such as phosphorus glass may keep the photoresist from adhering properly to the semiconductor surface. In dealing with this problem, the wafers are treated in the following manner to ensure that all surface oxides are hydrophilic and completely clean and dry [34]:

- Rinse off old photoresist with acetone.

- Boil wafers in acetone for 1 minute and allow to dry in air.

- Soak in warm *Microposit 1112A Remover* for 10 minutes.

- Rinse in running DI water for 2 minutes.

- Soak in warm H_2SO_4:H_2O (1:10) for 5 minutes.

- Rinse in running DI water for 2 minutes.

- Dip HF:H_2O (1:50) for 15 seconds.

- Rinse in running DI water for 2 minutes.

- Blow dry with nitrogen.

- Bake in forced-air convection oven at 200°C for 30 minutes.

- Allow to cool 10 minutes.

At this point, processing is resumed by repeating steps 1 to 10 from the previous page and then performing the following:

11. Rinse in DI H_2O for 1 minute.

12. Blow dry with compressed N_2.

13. "Hard Bake" for 30 minutes at 110°C.

14. Allow to cool for 10 minutes.

15. Proceed with etching procedure.

It should be mentioned that this process schedule repeatedly yields very uniform photoresist layers with well-defined features after exposure and development. In addition, the films are highly resistant to the HF:NH_4F (1:4) etching solution that is commonly used subsequent to the photolithography to etch away the exposed oxide on the wafer surface (see Fig. 3.4).

3.2.3 P-N Junction Formation

The following section describes a sequence of experiments that were performed to determine the viability of using *Borosilica* as a boron diffusion source for the fabrication of IBC solar cells. While the results are negative, the experiments have proven to be very instructive in clarifying the requirements for successful boron doping, eventually accomplished by ion implantation.

Borosilica spin-on sources are sometimes used to create junctions in n-type substrates [35]. Junctions formed with such a source at Concordia consistently had poor I-V characteristics and unusually high series resistances. The spin-on source in question is manufactured by *Emulsitone* and is composed of a boron-doped silica gel in an ethyl alcohol base. The concentration of boron in the fluid can be varied by diluting the solution with methanol, ethyl alcohol or isopropyl alcohol, and its application to a clean wafer surface is performed by spinning at 3000 rpm for approximately 15 to 30 seconds. The film is subsequently cured for 15 minutes in a forced-air convection oven set at a temperature of about 150 °C [35]. The latter step is done to ensure that all traces of solvent are driven out of the film prior to the high temperature pre-deposition of the boron atoms into the silicon substrate.

The procedure forms a 0.12 μm thick boron-doped SiO_2 film on the wafer surface which the manufacturer claims to act as a constant source for diffusion depths of up to 10 microns [35]. Processing subsequent to boron pre-deposition usually involves drive-in diffusion cycles at varying temperatures and, ultimately, the formation of contacts to the diffused regions through metallization procedures.

As is indicated above, many problems were encountered in using this solution. The following section describes these problems in greater detail and discusses the experimental procedures that were performed in trying to ameliorate the quality of the diffusions.

Experiment #1

The first problem that was addressed was the unusually high forward series resistance (1 to 5 kΩ, inconsistent) of diodes that were fabricated to test the junction characteristics. In order to ensure that the resistance was due to the Borosilica solution and not to the photolithography procedures that were in place at the time, the following process sequence was performed:

1. Clean n-type process wafers using boiling solutions of trichloroethane, acetone and methanol.

2. Etch off any native oxides by dipping wafers in a NH_4F:HF (4:1) solution for 30 seconds, then rinse in DI water.

3. Dry wafers under hot lamps.

4. Grow approximately 0.5 μm of SiO_2 on wafer using wet oxidation procedure (see Chp. 4).

5. Spin on and expose negative photoresist through boron diffusion mask and develop.

The wafers were at this point verified under a microscope to ensure that the diffusion windows had no trace of resin in them. Note that the photolithography procedures that were used then sometimes left traces of resin in the patterned windows after development. Thus, the photoresist was developed for longer periods of time in cases where traces were indeed found.

With the development completed, processing resumed as follows:

6. Dip wafers in a NH_4F:HF (4:1) solution until diffusion windows are hydrophobic, indicating that the oxide in the windows has been completely removed (NOTE: bare silicon is hydrophobic whereas silicon dioxide is hydrophillic).

7. Soften photoresist by soaking the wafers in hot nitric acid and subsequently scrubbing their surface with cotton swabs. The wafers are repeatedly verified under a microscope to ensure that no trace of resin remains on their surface.

8. Clean wafers using boiling solvents and then dry under hot lamps in preparation for the application of Borosilica.

9. Spin on Borosilica and proceed with the diffusion in an N_2 ambient at 1100 °C for 2 hours.

At this point in the processing, the wafers are covered with boron-doped glass over undoped glass (ie., SiO_2) in the non-diffusion areas and with boron-doped glass in the diffusion areas. The objective of the ensuing experiment was to determine whether some sort of film was created in the diffusion areas which perhaps was the source of the high resistance. The verification was done by soaking the wafers in a strong etching solution (ie., NH_4F:HF (2:1)) for approximately five minutes so as to remove all oxides from the wafers' surfaces.

If the diffusion proceeded as expected, the above oxide removal step should have produced a bare silicon surface on which the diffusion areas could no longer be discerned. This should have been the case since doping does not alter the structure of the silicon lattice itself. Fig. 3.5 shows a photograph of the

presumably bare wafer surface after completion of the etching procedure.

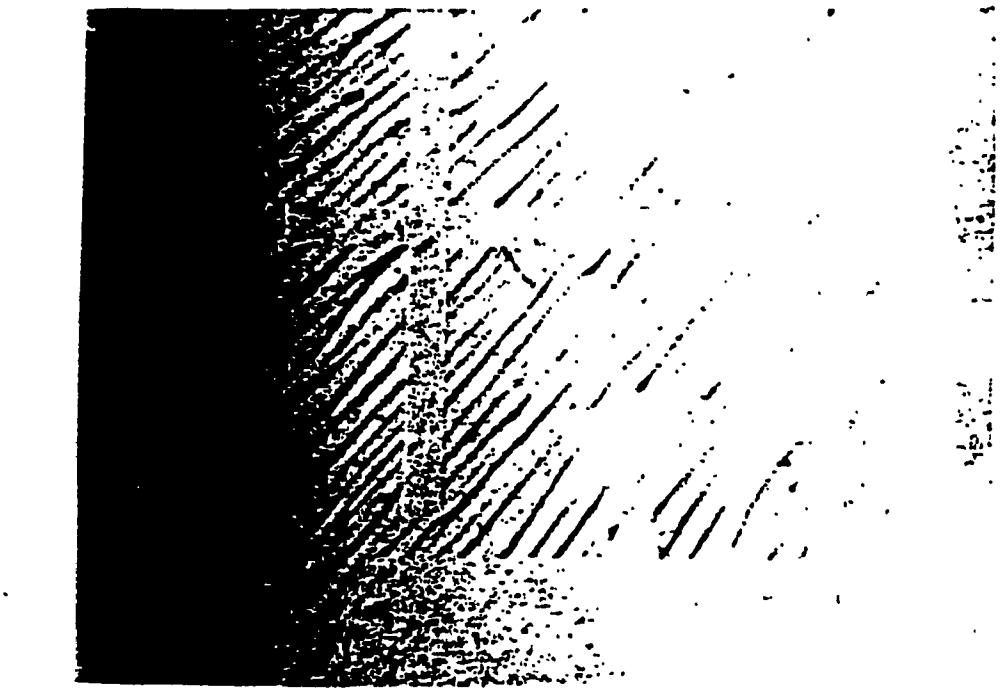


Figure 3.5: Presumably bare Si surface after diffusion.

Close examination of the photograph reveals that wherever it was in intimate contact with the silicon surface, the Borosilica caused the formation of a thin film that is barely visible to the naked eye. The film was also found to be somewhat inconsistently hydrophobic, making its detection very difficult.

Studies have shown that the film is in fact a silicon-boron phase (perhaps SiB_6) which is not soluble in HF and whose presence beneath the metal contact

to the diffused region is likely to cause an increase in contact resistance [36]. In an attempt to remove the phase, several experiments were carried out as outlined in the following discussions.

Experiment #2

The existence of the B-rich phase mentioned above is commonly referred to as a *brown stain* [35,36]. The product specifications from *Emulsitone* suggest that in order to avoid the formation of the stain whose removal is admittedly difficult, the diffusion should be carried out in an atmosphere of approximately 95% nitrogen and 5% oxygen [35]. It is claimed that such an ambient "will prevent staining and result in limited oxide growth to minimize boron gettering".

The above processing sequence was repeated therefore with approximately 5% O_2 in the N_2 flow during the diffusion. All other process parameters were left unchanged.

After etching the wafer down to bare silicon with an ammonium fluoride, hydrofluoric acid solution, the familiar problem was again observed. That is, the non-diffusion areas had a much more hydrophobic nature than the diffusion areas and the diffusion outlines were again visible when viewed under a microscope.

Some of the wafers were subsequently etched in a HNO_3:H_2O:HF

(100:100:1) solution for approximately 3 minutes in an attempt to remove the film [37]. This gave unsatisfactory results in that the staining problem remained and the silicon itself had been attacked, leaving the surface covered with pits and streaks.

Experiment #3

It has been reported that removal of the phase may be facilitated by following the diffusion with a low temperature oxidation (LTO) and subsequently etching the wafers in a dilute HF solution [38]. The oxidation is typically carried out at 600 °C in a flow of wet oxygen. Since the procedure is done at a relatively low temperature, the dopant diffusion profiles in the substrate are not significantly affected. The temperature should in theory be high enough however to support the chemical reaction of boron atoms in the phase with oxygen atoms in the gas flow, and the reaction of oxygen and silicon atoms at the interface. These reactions induce the growth of B_2O_3 and SiO_2 beneath the SiB_6 layer and should facilitate the subsequent removal of the phase. Although this procedure has apparently been successful in the removal of the boron phase created when using planar diffusion sources or gas-source diffusions [38,39], it was not successful in the case of the Borosilica spin-on diffusion source as is discussed in the following.

The wafers which had not yet been etched in the HNO_3 based solution described above (see experiment #2), were carefully etched in this solution to a point where the Borosilica was removed from the non-diffusion areas. That is, when the oxide in these regions appeared to be clear and no longer covered with Borosilica, the etching procedure was stopped so as to avoid damaging the silicon surface. The wafers were then rinsed in DI water, dried and oxidized in wet O_2 at 650 °C for 30 minutes. This was followed by an etch in H_2O:HF (10:1).

Again, the diffusion windows never became entirely hydrophobic, whereas the surrounding oxide layer became progressively thinner. Two more one-hour LTO sequences were carried out without much success. It was concluded at this point that efforts should no longer be concentrated on methods of removing the boron phase, but rather on ways of avoiding their formation altogether during diffusion.

Experiment #4

The silicon-boron phase is produced at the interface between the boron-doped glass and the underlying silicon if the number of boron atoms supplied to the interface is larger than the amount that can be dissolved in the substrate. More specifically, if the boron concentration in the Borosilica film is greater than the solid solubility of boron in silicon at the diffusion temperature, the

formation of the phase will be enhanced [36].

The solid solubility of boron in silicon at 1100 °C is approximately $3x10^{20}$ cm^{-3} [40, pp. 3-3, 5-1 to 5-11] which is greater than the concentration of boron in the *Emulsitone* solution (ie., $5x10^{20}$ cm^{-3}). Thus, in an effort to avoid phase formation, the solution was diluted to a concentration of $1x10^{20}$ cm^{-3} prior to processing. Note that the solid solubility of boron in silicon at 1000 °C is approximately $2x10^{20}$ cm^{-3} [40, pp. 3-3, 5-1 to 5-11] which is greater than the diluted solution's boron concentration. The details of the process sequence that was followed are given in the following section which discusses ohmic contact formation.

After the procedure, the samples were etched in NH_4F:HF (4:1) for approximately two minutes. The procedure was deemed successful in view of the fact that the diffusion windows were now completely hydrophobic, and no evidence of brown-staining was observed under the microscope.

Having solved the staining problem, questions still remained however as to whether the *Emulsitone* solution was a viable contender for the creation of the p-n junctions for IBC solar cell fabrication. More specifically, was Borosilica capable of producing diffusions having good junction characteristics with low reverse saturation currents, and could good quality ohmic contacts be made to the diffusions?

Although spin-on sources do not generally induce the formation of high quality junctions [40, pp. 3-3, 5-1 to 5-11], final tests made at Concordia

revealed that the creation of good quality ohmic contacts to the diffused regions was also quite difficult. The next section describes these tests and results.

Ohmic contact characteristics

An ohmic contact is defined as a low resistance metal-semiconductor contact capable of passing current linearly in either direction without affecting device performance [11, pp. 185-197]. Aluminum is commonly used when making contact with silicon, as is the case for the majority of the devices fabricated at Concordia University's Microelectronics Laboratory. In creating these contacts, problems are encountered in view of the fact that the metal and semiconductor *work functions*, Φ, are not equal.

Work function is defined as the energy needed to move an electron from the Fermi level, E_F, to vacuum. Aluminum has a work function of $q\Phi_M = 4.3$ eV, whereas the work function for silicon can be calculated using the following relation [10, pp. 245-250]:

$$q\,\phi_s = q(\chi + V_n) \tag{3.1}$$

where $q\chi$ (= 4.0 eV for silicon [11, pp. 185-197]) is the electron affinity measured from the vacuum level to the bottom of the conduction band, E_c, and qV_n is the difference in energy between the Fermi level, E_F, and the conduction band.

The majority carrier concentration, p_p, in a p-type sample is given by [11, pp. 136-147]:

$$p_p = n_i e^{(E_i - E_{Fp})/kT} \tag{3.2}$$

where

n_i = silicon intrinsic carrier concentration
= 1.5×10^{10} cm^{-3}
E_{Fp} = Fermi level on p-side

Since we are analyzing a heavily doped p-type region in silicon formed with *Borosilica*, we can approximate p_p in the diffused region by the acceptor concentration, N_a. Thus, the Fermi level of the boron-doped silicon can be calculated from equation (3.2) as:

$$N_a = n_i e^{(E_i - E_{Fp})/kT}$$

$$\frac{N_a}{n_i} = e^{(E_i - E_{Fp})/kT}$$

$$E_{Fp} = 0.0555\,eV - 0.0259 \ln (N_a/n_i)\,eV \tag{3.3}$$

The work function for p-type silicon as a function of its doping level can

subsequently be deduced as follows:

$$
\begin{aligned}
q\phi_S &= q\chi + qV_n \\
&= q\chi + E_{gSi} - E_{F_p} \\
&= 4.0\,eV + 1.11\,eV - 0.555\,eV + 0.0259\ln(N_a/n_i)\,eV \\
&= 4.555\,eV + 0.0259\ln(N_a/n_i)\,eV
\end{aligned}
\tag{3.4}
$$

From this information, it can be concluded that p-type silicon will always have a greater work function ($\Phi_s \geq 4.55$ eV) than aluminum ($\Phi_M = 4.3$ eV). Thus, considering the energy band diagram for the system before and after joining the two materials (see Fig. 3.6 [11, pp. 185-197]), it can also be concluded that a Schottky barrier will be created between the metal and the semiconductor when they are placed in contact.

Since Φ_S is greater than Φ_M, the semiconductor Fermi level, E_{FS}, is lower than the metal Fermi level, E_{FM}, and therefore when the two materials are placed in contact, charge transfer must occur to align the two levels at equilibrium. Specifically, the electron energies of the semiconductor must be raised by lowering the electrostatic potential of the semiconductor relative to the metal. This condition is satisfied by the transfer of majority carriers from the silicon to the aluminum. The transfer leaves behind uncompensated acceptor ions in the silicon and consequently leads to the creation of a depletion region

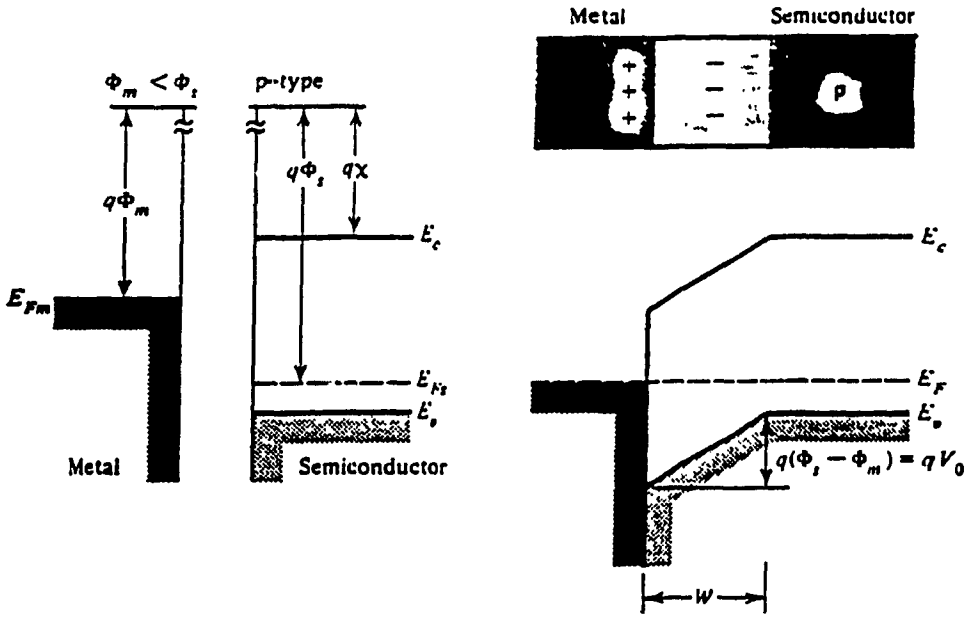


Figure 3.6: Schottky barrier formation between Al & p-type Si.

in the semiconductor near the interface. A potential barrier, $V_o = \Phi_S - \Phi_M$, is therefore established between the two materials which retards hole diffusion from the silicon to the aluminum and which keeps the junction from acting as a purely ohmic contact.

Recalling that the depletion layer width, W, in a semiconductor is a function of the doping level in the semiconductor (see Chp. 2), it can be concluded that W may be reduced to a point where the barrier becomes

transparent to holes by doping the semiconductor heavily at the metal-semiconductor interface. This results in a contact I-V characteristic that is not necessarily linear, but which has a very low resistance because holes have sufficient energy to tunnel through the barrier [42].

The aim of the following analysis is to verify whether the process sequence carried out during experiment #4 did in fact create a heavily boron-doped silicon surface below the aluminum layer. If the doping level was sufficiently high, a reasonably good ohmic contact should have been established between the two materials, and the resultant contact I-V characteristic should have demonstrated the fact.

The material used for the experiment was 10 $\Omega \cdot$ cm, phosphorus-doped, float-zone (FZ) silicon (see Chp. 4). In performing the experiment, a process schedule very similar to the one that had been developed for IBC cell fabrication (see Chp.4) was followed in an effort to emulate future processing conditions as closely as possible. The process schedule is summarized as follows (note that this is only a partial summary; complete process details and mask layouts are given in chapter 4):

1. Grow ~ 0.6 μm of SiO_2 to mask against boron diffusion.

2. Expose through boron mask, etch open boron diffusion windows, strip positive photoresist, clean wafers using Reverse-RCA procedure, dry wafers and apply *Borosilica* (diluted to $1x10^{20}$ cm^{-3}).

3. Pre-deposit Boron at 1000 °C for 2 hours in ~ 95% N_2 and 5% O_2 ambient.

4. Grow ~ 0.4 μm of SiO_2 at 1000 °C for 1 hour and 15 minutes in wet O_2 ambient to mask against subsequent phosphorus diffusion.

5. Expose through phosphorus mask, etch open phosphorus diffusion windows, strip positive photoresist, clean wafers using Reverse RCA procedure, dry wafers and apply *Phosphorosilica* (see Chp. 4).

6. Pre-deposit Phosphorus at 1000 °C for 1 hour in N_2 ambient.

7. Oxidize samples at 1000 °C for 13 minutes in wet O_2 ambient.

8. Anneal oxide at 1000 °C for 15 minutes in N_2 ambient.

9. Open contact windows through oxide (using photolithography), delinate metallization areas on wafer surface (using, again, photolithography), evaporate aluminum and anneal contacts at 450°C for 15 minutes in H_2 ambient.

During the boron predeposition, the boron surface concentration is held constant at $N_o = 1x10^{20}$ cm^{-3} and the diffusion therefore assumes a *complementary error function* profile (see Chp.5). The total number of boron atoms, Q_B, deposited during this initial diffusion (of duration $t_{p\text{-}dep} = 7200$ sec) may therefore be calculated as [41]:

$$Q_B = 2\sqrt{\left(\frac{D_B t_{p\text{-}dep}}{\pi}\right)} N_o \qquad (3.5)$$

where D_B is the diffusion coefficient of boron at T = 1000 °C and is given by [41]:

$$D_B = D_o e^{-E_A/kT}$$

$$= 0.76\, e^{-3.46/(8.62x10^{-5}\cdot 1273)}$$

$$= 1.54x10^{-14}\ cm^2/sec$$

Thus,

$$Q_B = 2\sqrt{\left(\frac{1.54x10^{-14}cm^2/sec \cdot 7200sec}{\pi}\right)}\ 1x10^{20}\ cm^{-3}$$

$$= 1.19x10^{15}\ cm^{-2}$$

In the analysis that follows, boron segregation into the silicon dioxide is neglected and it is assumed that pre-deposited boron atoms lie at or very near the semiconductor surface. Thus, the dopants assume a Gaussian distribution during the subsequent 2 hour and 43 minute drive in, and the resultant surface concentration can be estimated from equation (3.6) by replacing t with the total drive-in time of 9780 seconds and x with zero (ie., we want N_B at the surface) [41]:

$$N_B(x,t) = \frac{Q_B}{\sqrt{\pi D_B t}}\ e^{-\frac{x_j^2}{4D_B t}} \qquad (3.6)$$

Thus,

$$N_{B\text{-}surf} = \frac{1.19x10^{15}cm^{-2}}{\sqrt{\pi\,(1.54x10^{-14}cm^2/\text{sec})\cdot(9780\ \text{sec})}} \cdot 1$$

$$= 5.47x\,10^{19}\,cm^{-3}$$

To account for the segregation of the boron atoms into the SiO_2 during drive-in, the peak surface concentration calculated above should be multiplied by a factor of about 0.2 [40, pp. 3-3, 5-1 to 5-11]. Hence, the approximate final concentration of boron atoms at the silicon surface is roughly 10^{19} cm^{-3}. Given this result, the barrier height of the Al-Si interface under consideration may be found by setting N_a to 10^{19} cm^{-3} in equation (3.4) and proceeding as follows:

$$\phi_B = \phi_S - \phi_M$$

$$= 4.555 + 0.0259\ln(N_d/n_i) - \phi_M$$

$$= 4.555 + 0.0259\ln(10^{19}/1.5x10^{10}) - 4.3$$

$$\approx 0.8\,V$$

Figure 3.7 is a graph of the specific contact resistance, R_c, versus doping level, N_D, for various barrier heights [10, pp. 304-306]. Using this graph and the information presented above, it can be concluded that an Al-Si contact made to a p-type region fabricated according to the process schedule summarized above should have a specific contact resistance of approximately 10^{-1} $\Omega\cdot cm^2$.

Thus, for a contact area of about 0.012 cm^2, a contact resistance of about $10^{-1}/0.012 = 8.3\Omega$ would be expected.

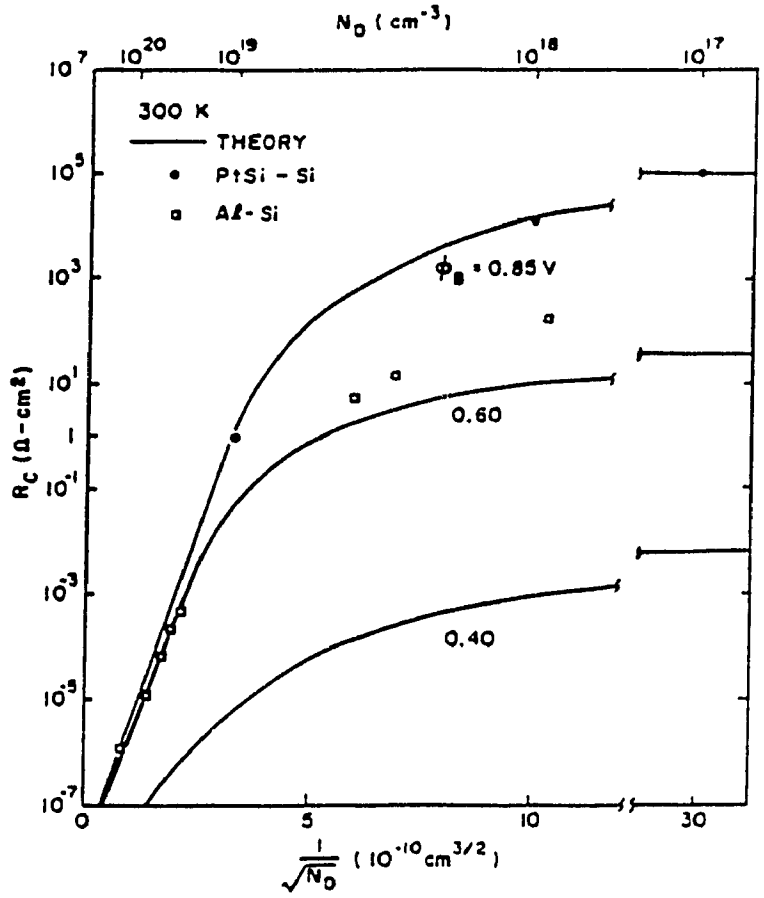


Figure 3.7: Specific contact resistance vs. doping level.

In testing the electrical characteristics of contacts made to the boron-doped silicon, two alluminum contacts were made to the diffused region. The contacts measured 1000 by 600 microns (thus total contact area = 2(0.1

cm)(0.06 cm) = 0.012 cm^2) and were separated by a distance of 80 microns (see chapter 4).

Figure 3.8 shows the device's measured I-V characteristic. The measurement was made with a *HP4145A Semiconductor Analyzer*, which had been programmed to sweep the voltage from -10 to +10 V between the two contacts and to measure the resultant current. It can be seen that the curve is not at all linear and that the series resistance is in excess of 15 kΩ in the linear regions. This resistance far exceeds the expected value on the order of 8 Ω, and the reasons for the discrepancy remain unclear.

Conclusions regarding the use of *Borosilica*

These final tests demonstrated that *Borosilica* should not be used as the source of boron dopant for the fabrication of solar cells. Devices fabricated with the product consistently suffered from unusually large contact resistances, unpredictable diode and contact I-V characteristics, and from non-uniform doping layers. The latter conclusion was reached after attempting to make sheet resistance measurements using Van Der Pauw test structures (see chapter 4) that had been included in the diffusion masks. These measurements were always erratic and failed to give reproducible results.

In view of these results, the IBC process schedules were re-structured to

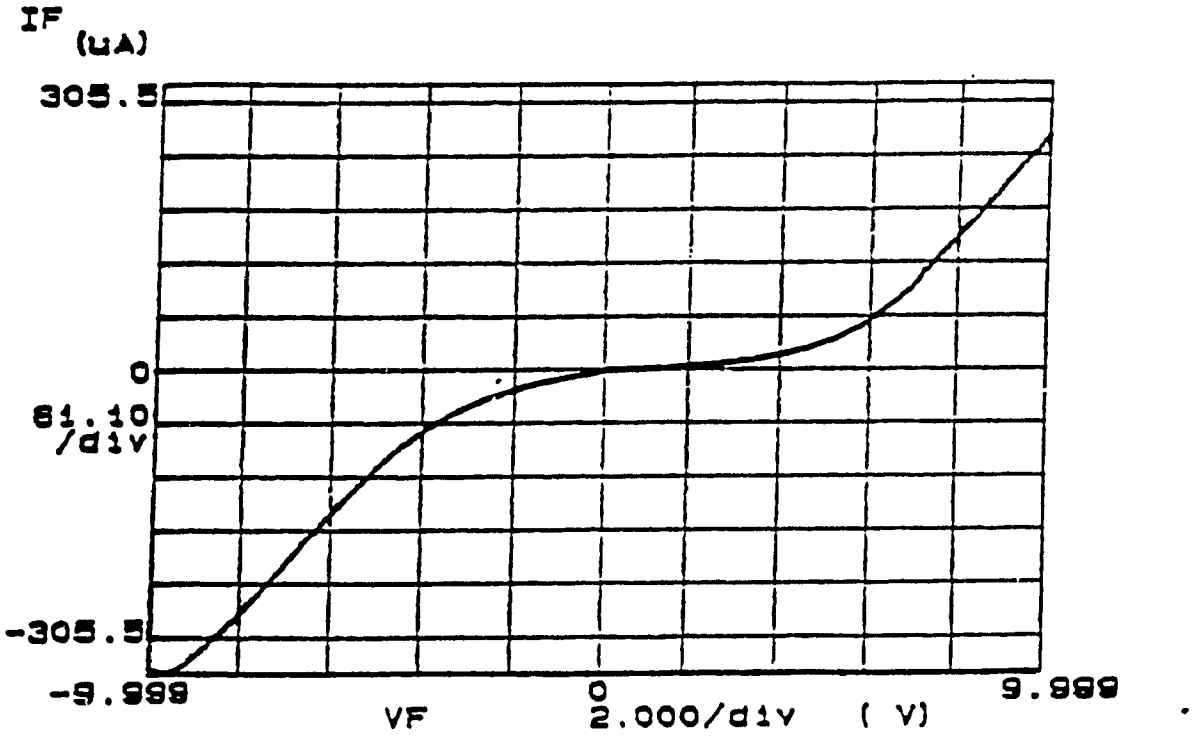


Figure 3.8: I-V curve of ohmic contact test structure.

accommodate an ion implantation sequence. As is discussed further in chapter 4, ion implantation was subsequently used rather than Borosilica in the formation of the IBC solar cell's rear-contacted p-n junctions.

Chapter 4
IBC Mask and Process Development

A total of six fabrication runs were performed in attempting to develop an IBC process sequence that would consistently yield devices with good electrical characteristics. Borosilica was used as the boron dopant for two of the runs while ion implanted wafers were used for the remaining four. As was discussed in chapter 3, Borosilica was dropped as the dopant source after tests proved conclusively that its use did not yield satisfactory junction and ohmic contact characteristics. Subsequent efforts were aimed at modifying the process used with the implanted wafers so as to obtain devices with tolerable values of sheet and contact resistance. The sequence that produced some of the better operational devices is described in the following pages.

The chapter begins with a brief summary of the process. This is followed with a description of the on-chip test structures that were included in the design

to allow for the verification of various process parameters and conditions. The layouts of the four masks used for fabrication are then considered, followed by a detailed description of the process schedules and conditions.

4.1 Process Summary

Certain variations of the interdigitated back contact solar cell design have been successfully realized with the use of a single photolithographic step [3,4]. In fabricating such devices, a self-aligning procedure is used which gives rise to the formation of *compensated regions* at the rear surface. In these regions, p and n-type dopants are allowed to interdiffuse, thereby establishing areas in which large concentrations of boron atoms cancel out large concentrations of phosphorus atoms. The existence of such regions introduce variables in the design that complicate its analysis [3,4] and that render less predictable performances than the conventional IBC cell.

In view of these observations, a conventional, four-mask implementation of the IBC solar cell was undertaken for this work. The fabrication sequence that yielded functioning devices consisted of the following steps:

1. Clean phosphorus-doped (n-type), 300 micron thick silicon wafer using Reverse-RCA cleaning procedure. (see Chp. 3) Wafers used for all fabrication runs are one-side polished (contact, or back-side)

and lapped on the other (sunward, or front-side).

2. Grow thermal oxide that will mask against subsequent boron implantation.

3. Using photolithography and mask level 1 (ie., **Boron Mask**), delineate boron implant/diffusion windows in the applied photoresist. Etch open windows in the oxide using a solution of $HF:NH_4F$.

4. Implant a dose of 10^{15} cm^{-2} boron atoms at an energy of 60 keV.

5. Strip photoresist.

6. Clean wafer using Reverse-RCA procedure while leaving original oxide layer intact.

7. Grow thermal oxide that will mask against subsequent phosphorus diffusion. Note that the substrate must be heavily-doped wherever contact is to be made to it so as to enhance the formation of good ohmic contacts. This was discussed in chapter 3 in the case of p-type contacts.

8. Using photolithography and mask level 2 (ie., **Phosphorus Mask**), delineate phosphorus diffusion windows in the applied photoresist. Etch open windows in the oxide and etch off the oxide from the wafer's front surface using a solution of $HF:NH_4F$.

9. Strip photoresist.

10. Clean wafer using Reverse-RCA procedure.

11. Perform phosphorus diffusion in an N_2 ambient using a Phosphorosilica spin-on diffusion source (this source does not exhibit the same problems as Borosilica).

12. Grow thermal oxide. This final oxide layer passivates all surfaces and acts as the anti-reflection coating on the cell's front-surface (recall that the front surface was bare Si prior to this step

due to step (8) above).

13. Using photolithography and mask level 3 (ie., **Contact Mask**), delineate contact windows to the p and n diffusions in preparation for the subsequent metallization sequence. Etch open windows in the oxide using a solution of HF:NH_4F (the front surface oxide is protected during the etch with a film of photoresist).

14. Using photolithography and mask level 4 (ie., **Metallization Mask**), delineate metallization windows in the applied photoresist.

15. Evaporate aluminum onto the wafer.

16. "Float-off" excess aluminum by soaking wafer in acetone.

17. Anneal wafer in H_2 ambient.

4.2 Mask Design

Several constraints had to be observed in designing the four masks needed for IBC solar cell fabrication at Concordia. Primarily, it was required that the masks be compatible with the mask aligner available in the laboratory. Specifically, the mask aligner which is manufactured by *COBILT Inc.*, could not be used to process wafers much larger than 1¼ inch in diameter. Thus, the total mask area was kept at approximately one square inch to ensure that problems would not be encountered in aligning the four-level design.

Secondly, masks that had in the past been used with the aligner did not

have feature sizes much smaller than 50 microns. Thus, since these early alignments had proven to be moderately difficult, the minimum feature size in the IBC masks was kept no smaller than 20 microns.

In addition to these constraints, the following design objectives were established prior to drawing the scaled layouts with *AUTOCAD*:

1. The solar cell active area should be kept to approximately $1 cm^2$.

2. Proper alignment marks should be used to facilitate alignment.

3. Sufficient area should be left in the design for the inclusion of contact pads to the cell's n and p fingers, respectively.

4. Test structures which could be used to verify various process parameters should be included in the design.

4.2.1 Test Structures

The following lists the test structures that were included in the layouts:

1. **Van der Pauw** sheet resistance structures for measuring diffusion and metallization sheet resistances.

2. **Contact Resistance** structures for measuring n and p contact resistances.

3. **Contact Strings** for verifying the probability of short or open circuits in the metallization.

Van der Pauw Structures

If the sheet resistance, R_s, ($\Omega/\square$) and the junction depth, x_j, of a diffused layer are known, the dopant surface concentration, N_{surf}, may be obtained from Irvin's Curves [41] for both Gaussian and erfc diffusion profiles. That is, a layer's average conductivity, σ, may be calculated from:

$$\sigma = \frac{1}{R_s \cdot x_j} \qquad (\Omega \cdot cm)^{-1} \tag{4.1}$$

Hence, given the layer's conductivity, its profile type (ie., erfc or Gaussian) and the substrate's background concentration, N_{BG}, the dopant surface concentration may be deduced from the curves.

The Van der Pauw technique is often used to obtain sheet resistances of diffused layers and of metallizations. When using the technique for diffused layers, a structure in the shape of a symmetrical four-leaf clover is first opened in the oxide layer covering the diffused region (see Fig. 4.1 [32, pp. 300-303]). Then by contacting the Si directly with 4 probes, current is forced between two adjacent contacts, and the voltage measured across the opposing pair. This is repeated around the structure's periphery until four sets of I-V data are obtained.

Using this data, the average sheet resistance may be calculated as [32, pp. 300-303]:

$$R_s = \frac{\pi}{ln2} \cdot \frac{1}{4}\left(\frac{V_{12}}{I_{34}} + \frac{V_{23}}{I_{41}} + \frac{V_{34}}{I_{12}} + \frac{V_{41}}{I_{23}}\right) \quad [\,\Omega/\square\,] \tag{4.2}$$

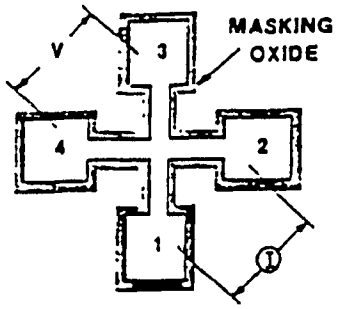


Figure 4.1: Van der Pauw test structure.

It should be noted that the structure's size does not affect the calculated value of sheet resistance since the voltage and current readings vary proportionately according to its size. Furthermore, the use of a high-input-impedance meter ensures that current is not passed while making the voltage measurement, thereby negating any contact resistance problems that may exist between the probe tips and the wafer surface. Note that the possibility of errors introduced by rounding of the corners at the structure's centre is minimized because the rounding is expected to be in the same order of magnitude of the

junction depth (less than 2 μm which is less than 1% of the width of the stripes)

When designing the IBC masks, two sets of three identical patterns were made for each diffusion type and one set of two identical patterns was made for the aluminum metallization. The inclusion of these redundant structures permit the verification of dopant uniformity and metallization thickness across the wafer surface.

Contact Resistance Structures

In determining the resistance introduced by metal-semiconductor contacts, a test pattern such as that shown in Fig. 4.2 is often used [43]. The pattern consists of differently spaced ohmic contacts made to a well-defined diffused region. Since current flow must be confined to this region, the doping level is made much higher than the substrate doping, as is usually the case when ohmic contacts are made to silicon (see chapter 3).

The resistance measured between two adjacent contacts is given by

$$R = 2R_c + \frac{R_s}{W} L \tag{4.3}$$

Thus, if the resistance between the different pairs of contacts is

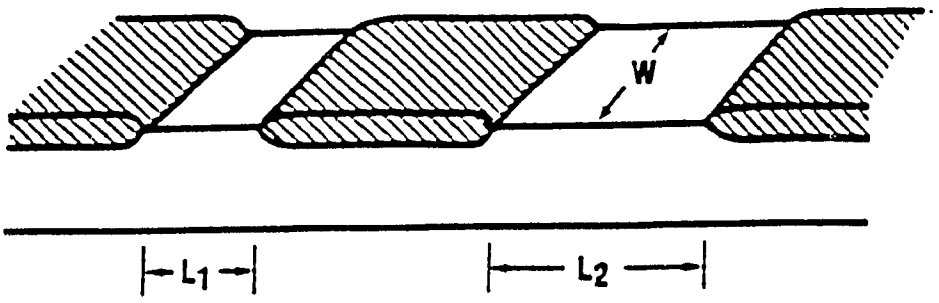


Figure 4.2: Basic contact resistance test pattern

measured, a plot can be made of resistance versus the distance between the contacts, L, as shown in Fig. 4.3 [43]. Hence, the contact resistance, R_c, can be found by locating the curve's y-intercept, while R_s (the sheet resistance of the diffused layer), can be deduced from its slope.

Figure 4.4 shows the layout and dimensions of the contact test structure incorporated in the IBC mask design. The contact width was made to be 1000 microns while the contact length was made 600 microns. A total of six contacts were delineated in a diffusion region having a total area of 1200 by 4400 microns. The contact spacings were made 80, 160, 240, 320 and 400 microns, respectively.

Four such structures were included to determine the resistance of the contacts made to the p and n-type diffusions. As a redundancy check, two patterns were made for each contact type.

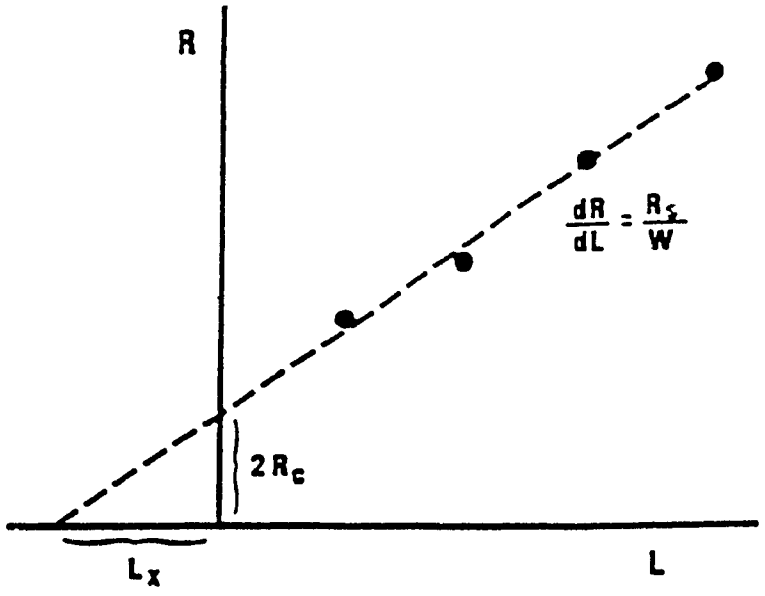


Figure 4.3: Plot of measured resistance vs contact separation.

Several points should be made about tests performed with these structures. Primarily, the probes used to make the measurements introduce a resistance that is added on to the measured resistance. Hence, this probe resistance should be determined and subtracted from the obtained readings. Secondly, the readings are extremely sensitive to contact spacing errors [43] and therefore, the spacing should be precisely measured prior to generating any curves. In our case, this problem was circumvented by photolithographically delineating the contact windows in the oxide covering the diffused region. Verifications made by microscope did in fact indicate that accurate, well-defined spacings between the contacts were in general obtained through this method.

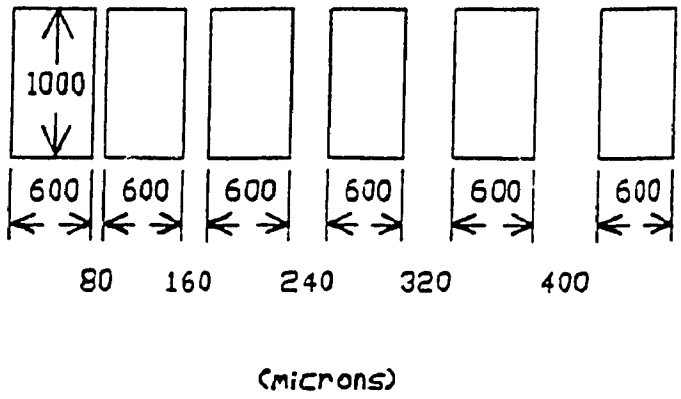


Figure 4.4: Contact test pattern dimensions used in the IBC mask layout.

Thirdly, patterns having irregular edges or defects should not be used as these will again introduce errors in the readings. In fact, it is suggested that data deviating significantly from the "norm" should be discarded when plotting the curves [43].

As a final note, it must be emphasized that most methods used to determine contact resistance give only a rough indication of true contact resistance. Problems discussed above such as irregular contact geometry, highly resistive metallizations (occurring when the aluminum layer is too thin) and spacing errors as small as 5 microns can give readings with errors in the range of 50 to 100% [43,44].

Contact Strings

Contact strings are often included in a mask design to check for the probability of open or short circuits in the metallization. The patterns used usually approximate the structure of the most sensitive (and therefore the most likely to fail) metallization patterns in the device. The string is delineated in the metallization mask, and is usually composed of two long parallel metal lines separated by a small distance. The distance is made to equal the smallest separation between any two metallized areas on the device's surface, and the length is usually chosen to approximate some of the longer metallized lines in the layout.

As is shown in the next few sections, the thinnest metal separation in the IBC masks is 40 microns, and the n and p finger lengths are on the order of 1 cm. Thus, the contact string devised for these masks is composed of two parallel, 260 micron thick metal lines, separated by a distance of 40 microns and having an effective overall length of approximately 4cm. As shown in figure 4.5, contact pads were located at the ends of each string to facilitate probing procedures.

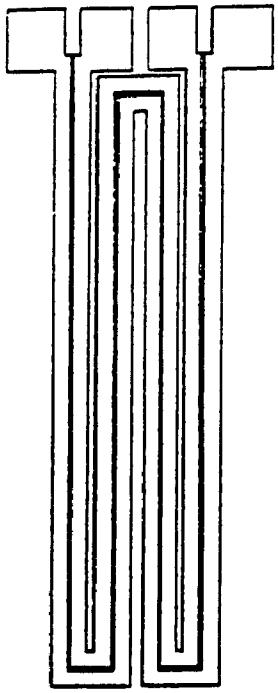


Figure 4.5: Contact string included in IBC mask design.

4.2.2 Mask #1: Boron Diffusion

Figure 4.6 shows the layout of the 2.04 cm^2 boron diffusion mask. It can be seen that five alignment marks were included in the design, the dimensions of which are shown in figure 4.7. Room for the eight Van der Pauw structures was made on the mask's bottom half, whereas space for the four contact resistance test patterns and the contact string was made on the layout's upper right-hand quadrant. The placement of the two resistance patterns and the three Van der Pauw's for the boron implant/diffusion is evident from Fig. 4.6.

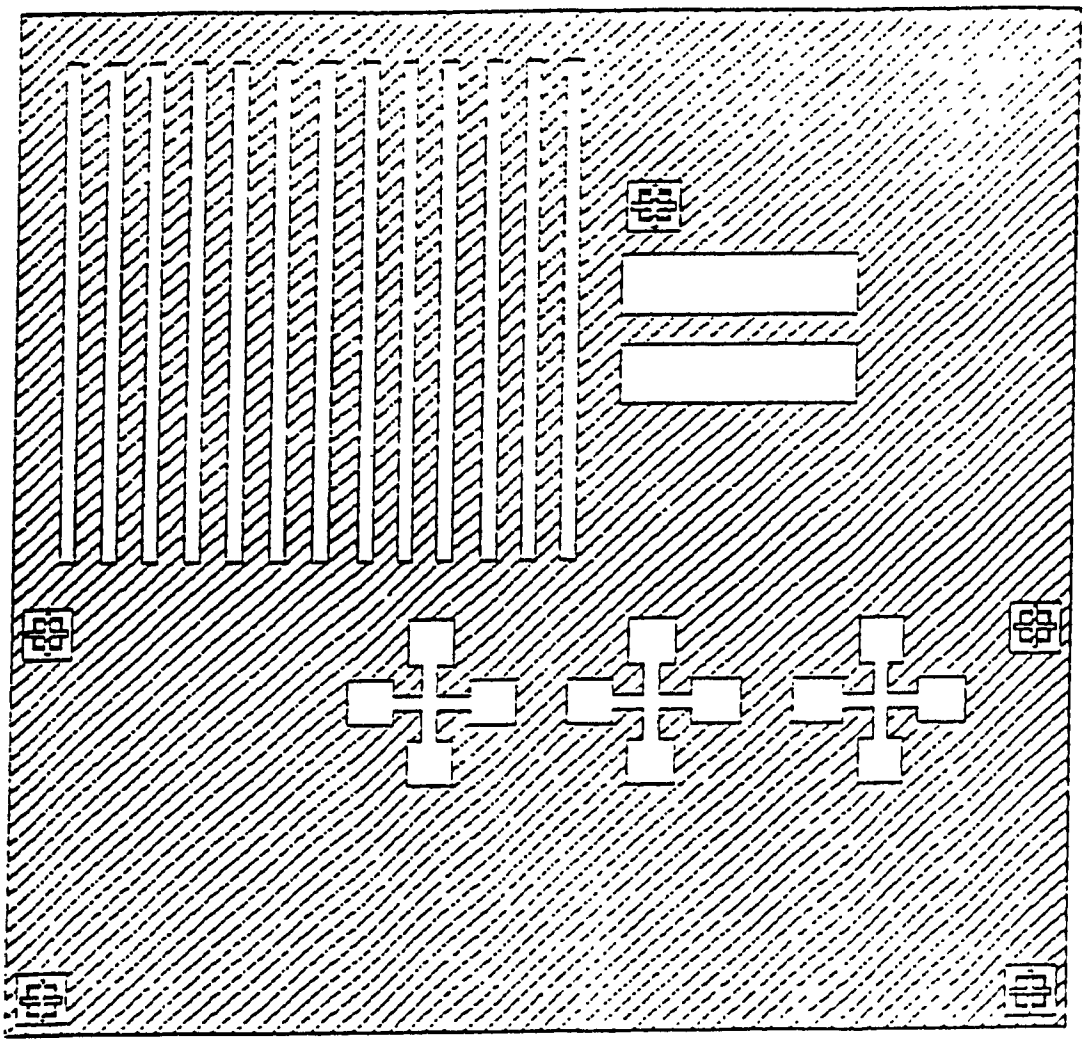


Figure 4.6: Mask #1: Boron Diffusion.

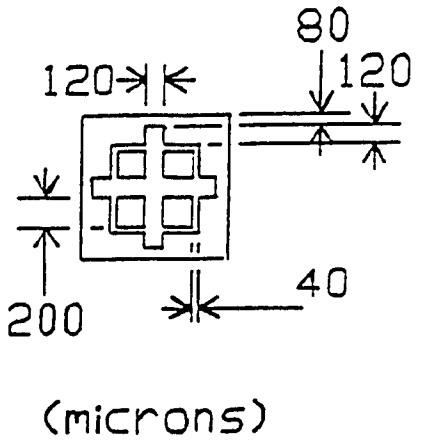


Figure 4.7: Alignment pattern dimensions.

The B implant areas for the solar cell are located in the mask's upper left-hand quadrant. The p-type diffusions consist of 13 fingers measuring 300 by 9980 microns, each separated by a distance of 500 microns. The total cell area is approximately one square centimetre and the emitter coverage fraction is roughly 39%. More specifically, the boron diffusion area (and hence the p-n junction area) makes up about 39 percent of the total cell area.

In laying out the solar cell portion of the IBC masks, it was decided that the emitter coverage fraction should be made to lie between 30 and 60 percent, which is a range commonly used for IBC cells operating under one-sun conditions [2,4,14].

4.2.3 Mask #2: Phosphorus Diffusion

Figure 4.8 shows the layout of the phosphorus diffusion mask. The two contact resistance structures are located below the equivalent structures for the boron diffusion, whereas the three Van der Pauw structures run along the layout's bottom edge. In this case, the 13 n-type diffusion fingers lying between the boron fingers measure 100 by 9980 microns and are separated by a distance of 700 microns.

It should be emphasized that the dimensions of the phosphorus diffusions are not as critical as those for the boron diffusions because they are needed strictly for the formation of good ohmic contacts to the n-type substrate (as opposed to emitter coverage). Thus, in designing the masks, it was decided that the p and n diffusions should be separated by the largest possible distance (200 microns in this case) while still allowing the formation of 20 micron contact holes to the diffused regions (see next section).

4.2.4 Mask #3: Contact

The contact mask is shown in figure 4.9. This mask is used to delineate those areas on the wafer surface where the oxide is to be removed prior to

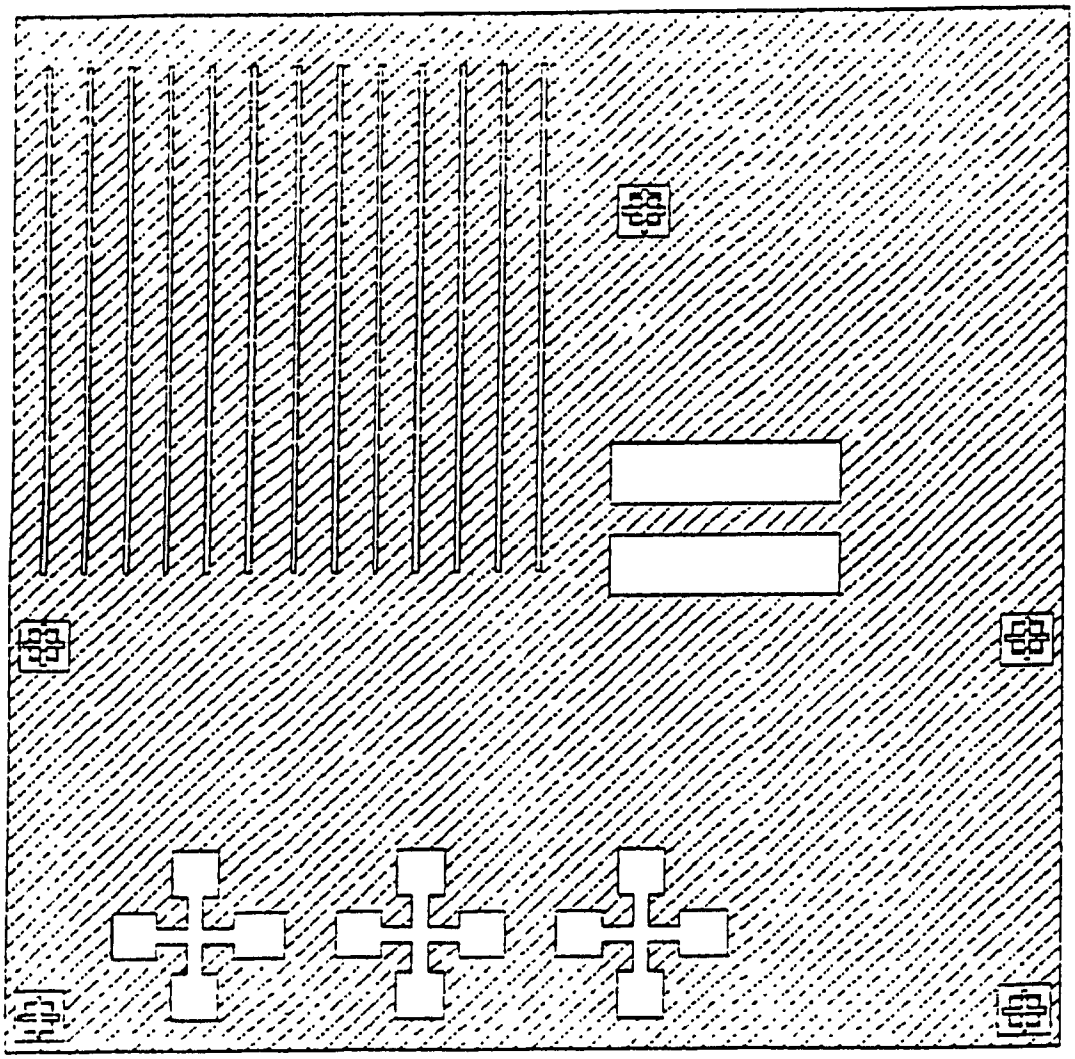


Figure 4.8: Mask #2: Phosphorus Diffusion.

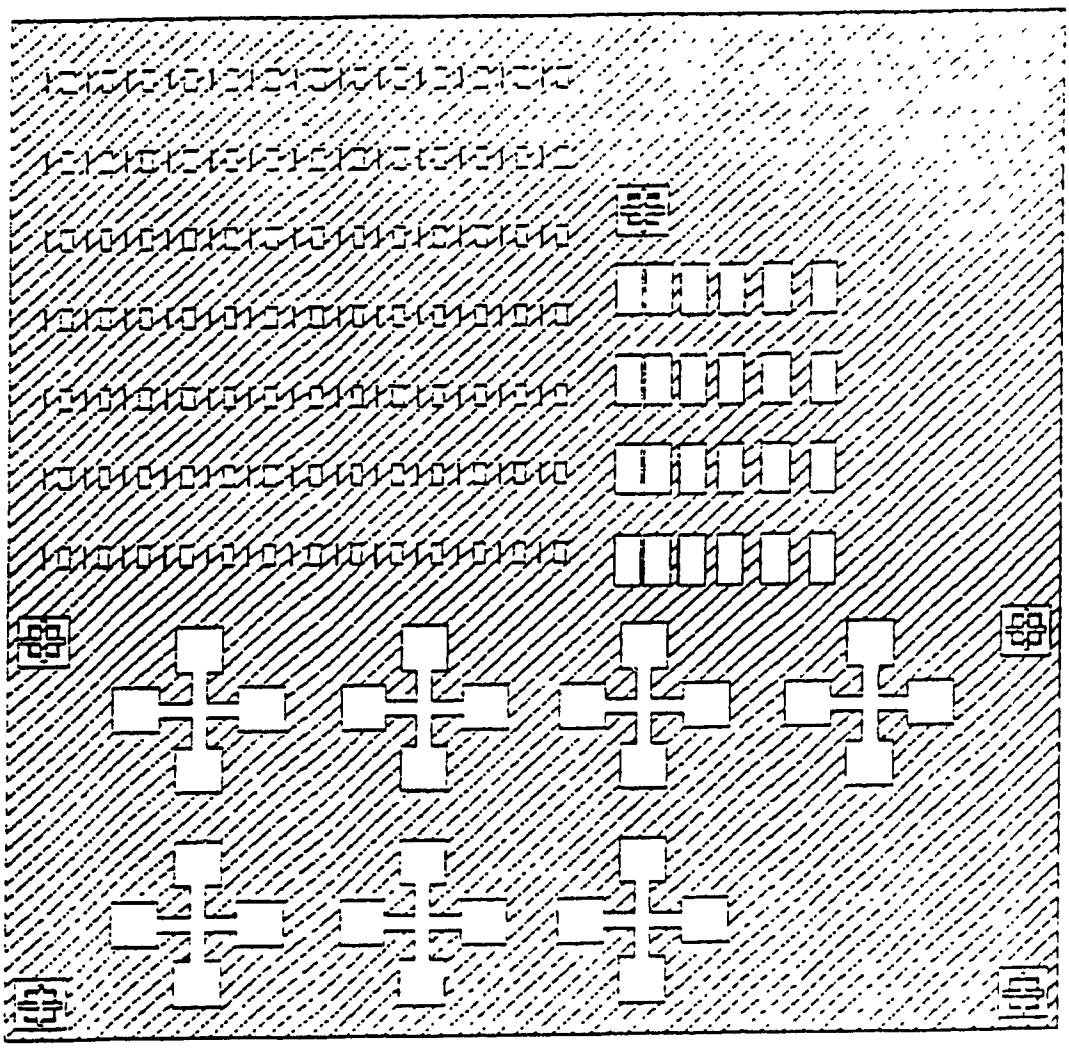


Figure 4.9: Mask #3: Contact.

metallization. Thus, the Van der Pauw windows as well as the previously discussed windows to the contact resistance patterns are opened with this mask, in addition to the contact holes to the diffused regions. Notice that a Van der Pauw pattern is also opened up in the oxide which covers an undoped region in the substrate. This pattern is eventually metallized (see next section) and may serve as a contact to the substrate should this be necessary for future testing procedures.

As was discussed in chapter 2, back surface recombination must be minimized by passivating as much of the cell's rear surface with silicon dioxide. Thus, rather than opening large contact holes running the entire length of the n and p-type diffusion fingers, smaller holes as shown in Fig. 4.9 are opened in the oxide covering the diffusions. The size of the holes was chosen so that the contact border was located 40 microns inside the diffusion border. Thus, in making contacts to the n-type diffusions, seven holes measuring 20 by 396 microns were made along the length of each finger, and each hole was vertically separated from the next one by a distance of 1188 microns. The contacts to the wider p-type fingers were made in the same manner, the only difference being that the lateral dimension of the holes was made 220 rather than 20 microns large.

4.2.5 Mask #4: Metallization

The metallization mask is shown in Fig. 4.10. Mask level 4 delineates those areas on the wafer surface where metal such as aluminum is to be deposited on the surface. Thus, the contacts to the contact resistance structures are covered with metal, as are the two Van der Pauw structures used to determine the metallization sheet resistance. In addition, the contact string pattern metallization is laid on the oxidized wafer surface, next to the contact resistance structures. The n and p-type finger metallizations are separated by a 40 micron distance, implying that approximately 89% of the cell's active back surface area is effectively covered with metal. Recall that in order to maximize the *back surface reflector* effect as is discussed in chapter 2, the metallization area should be made as large as possible.

Device testing is simplified by the inclusion of contact pads that are connected to the n and p bus bars, respectively. In designing the pads, their areas were maximized and they were kept away from the fingers so as to avoid damaging them while soldering wires to the pads. The area of the lower n-type pad measures 6.3mm^2 while the area of the upper p-type pad measures 8.4mm^2.

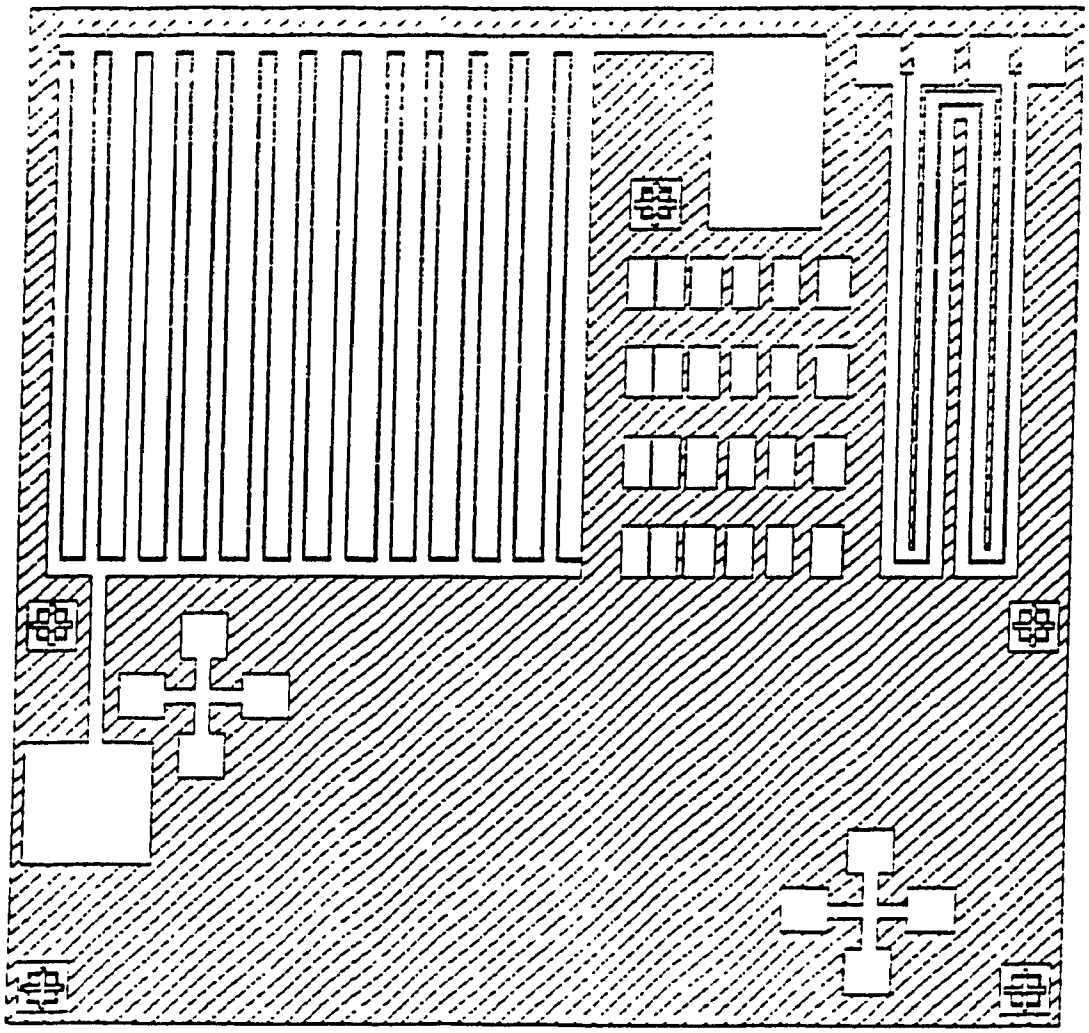


Figure 4.10: Mask #4: Metallization.

4.3 Detailed Processing Conditions and Parameters

It is a well known fact that lattice defects and impurities such as gold introduce levels in the silicon energy gap that act as carrier recombination centres [45]. Since the IBC solar cell configuration is very sensitive to carrier lifetime, careful attention is paid to the selection of the starting material prior to fabrication.

The production of pure, semiconductor grade materials is made possible through zone refining techniques that generate high purity silicon with very low dislocation densities [7,46 p. 101, 47]. Although float-zone (FZ) refined silicon is more expensive than the traditional Czochralski grown material, its use is usually mandated when high bulk carrier lifetimes are needed. Many research groups working with back-contact solar cell designs therefore make use of float-zone (FZ) silicon for their devices; such devices have in many cases yielded carrier lifetimes in excess of 2 msec [5,6,14,21].

Float zone silicon manufactured by *Wacker* is used in the fabrication of the interdigitated back contact cells for this work. The four-inch wafers have the following specifications:

- N-type, phosphorus-doped
- 10 $\Omega \cdot$ cm resistivity
- (100) orientation
- polished one side, lapped other side
- average thickness of 300 $\pm$ 15 μm

Wafers having a (100) orientation were selected so as to keep the density of surface atoms to a minimum. This minimizes the density of interface states, D_{it}, which in turn reduces the effective surface recombination velocity, S.

The process summary that was discussed briefly in section 4.1 is presented in greater detail in the pages that follow. Some numerical calculations such as post-implant and post-predeposition impurity profiles are presented in chapter 5 where they are compared with experimentally obtained values.

Note that prior to processing, the four-inch wafers are cut into one inch square slices which are subsequently cleaned using the Reverse-RCA procedure described in chapter 3. Note as well that the finger patterns are created on the polished side.

Oxide Growth for Masking Against Boron Implant

Ideally, the post-process boron surface concentration should be high enough to enhance the formation of good ohmic contacts to the diffused region. Thus, it was decided that the B implant should be done at a relatively low energy and at a very high dose.

A typical boron implant leaves most of the ions in electrically inactive interstitial rather than substitutional lattice sites. To activate these implanted ions, wafers are therefore usually annealed at high temperature.

It has been shown that a lattice that has been rendered amorphous or

nearly amorphous by an implant is more easily annealed than a partially damaged substrate [46, pp. 325-330]. Since boron is a "light" ion, it is stopped mostly by electronic rather than by nuclear interactions in the silicon lattice and therefore, very little damage is done to the crystal lattice at low doses. This problem is usually circumvented by using large implant doses which tend to increase damage and to consequently improve the characteristics of the annealed wafer.

An energy deposition of 10^{21} keV/cm^3 will usually render the substrate amorphous [48]. For a boron implant done at 60 keV, the projected range of the implanted ions is $R_p = 0.1903\ \mu m$. The dose needed to make the substrate amorphous is therefore at least [48]:

$$DOSE \approx \frac{(10^{21}\ keV/cm^3)(R_p)}{E}$$

$$\approx \frac{(10^{21}\ keV/cm^3)(1.903 \times 10^{-5} cm)}{60\ keV}$$

$$\approx 3.2 \times 10^{14}/cm^2$$

For the IBC cells fabricated, implant doses were at all times made higher than 10^{15}/cm^2.

Silicon dioxide is often used as a mask against ion implantation. Specifically, an oxide layer will effectively keep implanted ions from reaching the silicon surface beneath it provided that its thickness is made larger than a given minimum. The minimum thickness depends on the degree of masking that

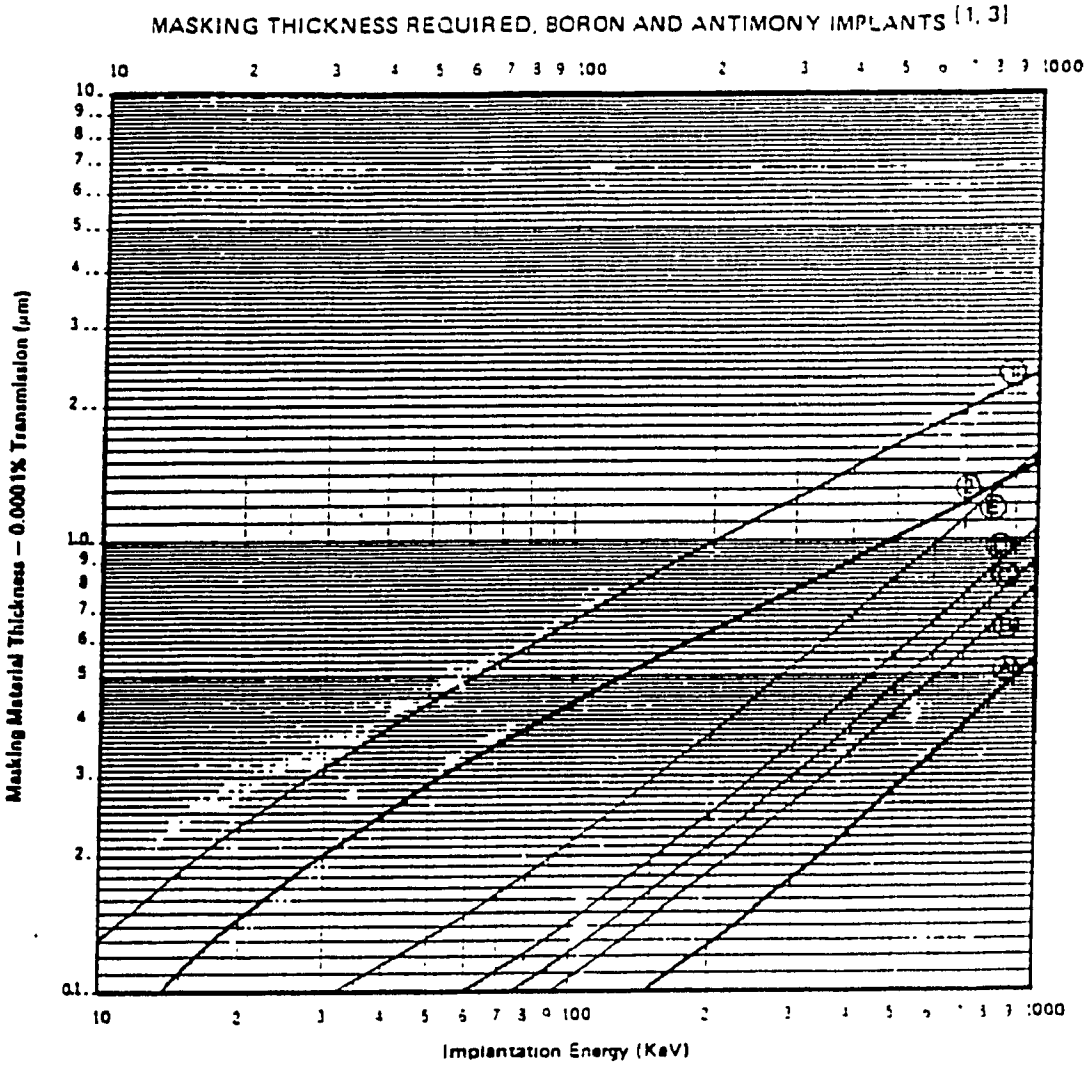
is required. For instance, to mask against a given fraction of the implanted ions (being of specific type, ie., boron, phosphorus, etc., and having a given energy), an oxide thickness, d, is needed which may be calculated from equation (4.4) [32, pp. 355-363]:

$$\frac{Q_p}{Q} = \frac{1}{2} erfc\left[\frac{d - R_p}{\sqrt{2}\Delta R_p}\right] \tag{4.4}$$

where

Q_p = dose that penetrates mask
Q = total implanted dose
d = masking oxide thickness
R_p = projected range of implanted ions (= 0.1903 μm @ 60 keV for boron [48])
ΔR_p = projected standard deviation of implanted ions (= 0.0556 μm @ 60 keV for boron [48])

In practice, graphs such as the one shown in Fig. 4.11 [40, pp. 6-1 to 6-10] are used to readily determine the oxide thickness needed to mask against B implants of varying energies. From curve #1 in this graph which corresponds to a boron implant masked by a thermally grown oxide, it can be seen that an oxide thickness of 0.49 μm will effectively mask 99.9999% of the boron atoms implanted at an energy of 60 keV.



ION	CURVE	MASKING MATERIAL	ION	CURVE	MASKING MATERIAL
Boron (Tool	1	Thermal SiO_2, Polysilicon Aluminum Negative Resist or Positive Resist	Antimony (Boron)	A	CVD Si_3N_4
				B	Thermal SiO_2 or Aluminum
				C	Polysilicon
	2	CVD Si_3N_4		D	Negative Resist
				E	Positive Resist

Figure 4.11: Oxide thickness for 99.9999% masking condition against boron implant (curve #1).

For this work, an oxide masking thickness of 0.6 microns was thermally grown prior to implantation. The growth parameters were:

- AMBIENT: wet oxygen, bubbler temp. ≃ 105 °C
- TEMP.: 1000 °C
- TIME: 2.01 hours

Sample calculation for oxidation time

Parabolic Rate Constant is given by [49]:

$$B = C_1 e^{-E_1/kT} \tag{4.5}$$

where

$C_1 = 2.14 \times 10^2\ \mu m^2/hr$ (wet O_2)
$E_1 = 0.71$ eV (wet O_2)
k = Boltzmann's constant = 8.62×10^{-5} eV/°K
T = 1273 °K (= 1000 °C)

Thus,

$$B = 2.14 \times 10^2\, e^{\frac{-0.71}{(8.62 \times 10^{-5})(1273)}}$$

$$= 0.331\ \mu m^2/hr$$

Linear Rate Constant is given by [49]:

$$B/A = C_2 e^{-E_2/kT} \tag{4.6}$$

where

$C_2 = 5.33\text{x}10^7$ μm/hr (wet O_2, (100) silicon)
$E_2 = 2.0$ eV (wet O_2)

Thus,

$$B/A = 5.33x10^7 e^{\frac{-2.0}{(8.62x10^{-5})(1273)}}$$

$$= 0.647\ \mu m/hr$$

Finally [49],

$$t_{oxid} = \frac{x_o^2}{B} + \frac{x_o}{B/A}$$

$$= \frac{(0.6\,\mu m)^2}{0.331\,\mu m^2/hr} + \frac{0.6\,\mu m}{0.647\mu m/hr}$$

$$= 2.01\ hr \tag{4.7}$$

Ideally, the wafers are oxidized immediately following the reverse-RCA cleaning procedure. In preparation for oxidation, the furnace is primed as follows:

1. Boil oxidation boat in acetone for 1 minute; blow-dry with compressed N_2 gas.

2. Turn ON water bubbler (it should be set for a temperature of about 105 °C).

3. Set N_2 flow in gas lines for furnace to approximately 1 SCFH.

4. Install clean oxidation tube in furnace and immediately connect gas hose. Note that when tubes are not in use, an N_2 ambient is maintained in them by keeping their tips sealed with *saran wrap*.

5. Turn ON furnace. Adjust its temperature setpoint to 1000 °C.

ASIDE: The oxidation reactor and boat may be cleansed at high temperature if deemed necessary by performing the following once the setpoint temperature has been reached:

- Push boat to centre of reactor (make sure that quartz rod used to do this is clean; ie., wipe it with acetone-soaked wiper).

- Increase furnace setpoint to approximately 1050 °C.

- Change ambient to wet O_2 at a flowrate of 1 SCFH.

- Wait 30 minutes.

- Change ambient to N_2, (flowrate = 1 SCFH) set furnace setpoint back to 1000 and pull boat back to mouth of reactor.

At this point, the system is ready for oxidation, and the cleaned wafers may be loaded onto the boat and oxidized as follows:

6. Push loaded boat to the centre of the reactor in 4-inch increments, waiting 2 minutes between each push.

7. Once boat has been at the centre for 2 minutes, change ambient to wet O_2 (flowrate = 1 SCFH) and begin oxidation timing.

8. At the end of the oxidation, change ambient to N_2 (flowrate = 0.5 SCFH), shut OFF furnace and slowly pull boat to the mouth of the reactor (this should take approximately 5 minutes).

9. Remove loaded boat from reactor and allow to cool for approximately 30-45 minutes.

Delineation of Boron Implant Areas

The *Boron Diffusion Mask (Mask #1)* is used to open the boron implant windows in the grown oxide. This is performed as follows:

1. Apply positive photoresist to wafer and bake as discussed in chapter 3.

2. Expose wafer for 15 sec. through Mask #1 using mask aligner.

3. Develop wafer in stirred developer, rinse in DI H_2O, dry with compressed N_2 gas and "hard-bake" wafers @ 115 °C (see Chp. 3).

4. Etch away exposed oxide in windows delineated in the photoresist

by dipping wafer in a solution of $HF:NH_4F$ (1:4) until windows become hydrophobic (1-3 minutes).

5. Rinse wafers in DI water and blow dry with compressed N_2.

Since photoresist does not affect the operation of the ion implanter, it is not removed prior to the boron implant.

Boron Implant

Three batches of wafers were implanted at 60 keV. Two batches were implanted with a dose of $1x10^{15}/cm^2$ (on two separate occasions) while the third was implanted with a dose of $2x10^{15}/cm^2$. Early tests performed on wafers from each lot revealed that the post-anneal impurity profile could not be controlled precisely by virtue of the fact that the implanted doses seemed to vary from run to run.

A test was performed to confirm these observations. It consisted of cutting a wafer from each implanted batch into several pieces and annealing them for different times at 1000 °C in wet O_2. After annealing, the sheet resistance of each piece was measured and compared with the others. In general, sheet resistances tended to vary by 5 to 15 percent for pieces that had gone through identical processing conditions, but which had been implanted at different times with the same dose. It should be mentioned that these variations

may be problematic for finely tuned process runs in the future which call for tight control over process conditions.

After implantation, the wafers are processed as follows:

1. Strip photoresist from wafers by boiling in acetone for 1 hour.

2. Swab with acetone and rinse clean with acetone.

3. Verify wafers under microscope. If traces of photoresist still remain on the wafer surface, repeat steps 1 and 2 until none can be found.

4. Clean wafers using Revers-RCA procedure (see Chp. 3).

The wafers are now ready to be oxidized in preparation for the phosphorus diffusion.

Oxide to Mask Against the Diffusion of Phosphorus Atoms

After several experimental runs, it was concluded that a one hour phosphorus pre-deposition at 1000 °C would yield a P surface concentration large enough to induce the formation of good ohmic contacts to the n-type substrate (see relevant discussion in chapter 5). The oxide thickness needed to

keep phosphorus atoms from reaching the silicon surface beneath the oxide may be determined by solving the diffusion equations (see Chp.5) in the case of diffusion into SiO_2. Note that P and B have diffusion coefficients in SiO_2 that are 0.1 to 0.01x smaller than their corresponding values in silicon [49].

As in the case of the oxide thickness needed to mask against a boron implant, graphs such as that shown in Fig. 4.12 [40, pp. 3-3, 5-1 to 5-11] are used to determine the oxide thickness needed to mask against a phosphorus pre-deposition. From this graph, it can be seen that an oxide thickness of 0.315 microns will effectively mask a phosphorus pre-deposition performed at 1000 °C for a duration of 1 hour.

Thus, an oxide thickness of approximately 0.4 microns is thermally grown on the implanted wafers in preparation for phosphorus diffusion. Oxide growth conditions are:

- AMBIENT: wet oxygen, bubbler temp. $\simeq$ 105 °C
- TEMP.: 1000 °C
- TIME: 1.00 hours

Note that the wafers are loaded and removed from the furnace using the same procedure that is described in the section discussing oxide growth against boron implantation. The oxidation is again performed with the oxidation reactor and boat.

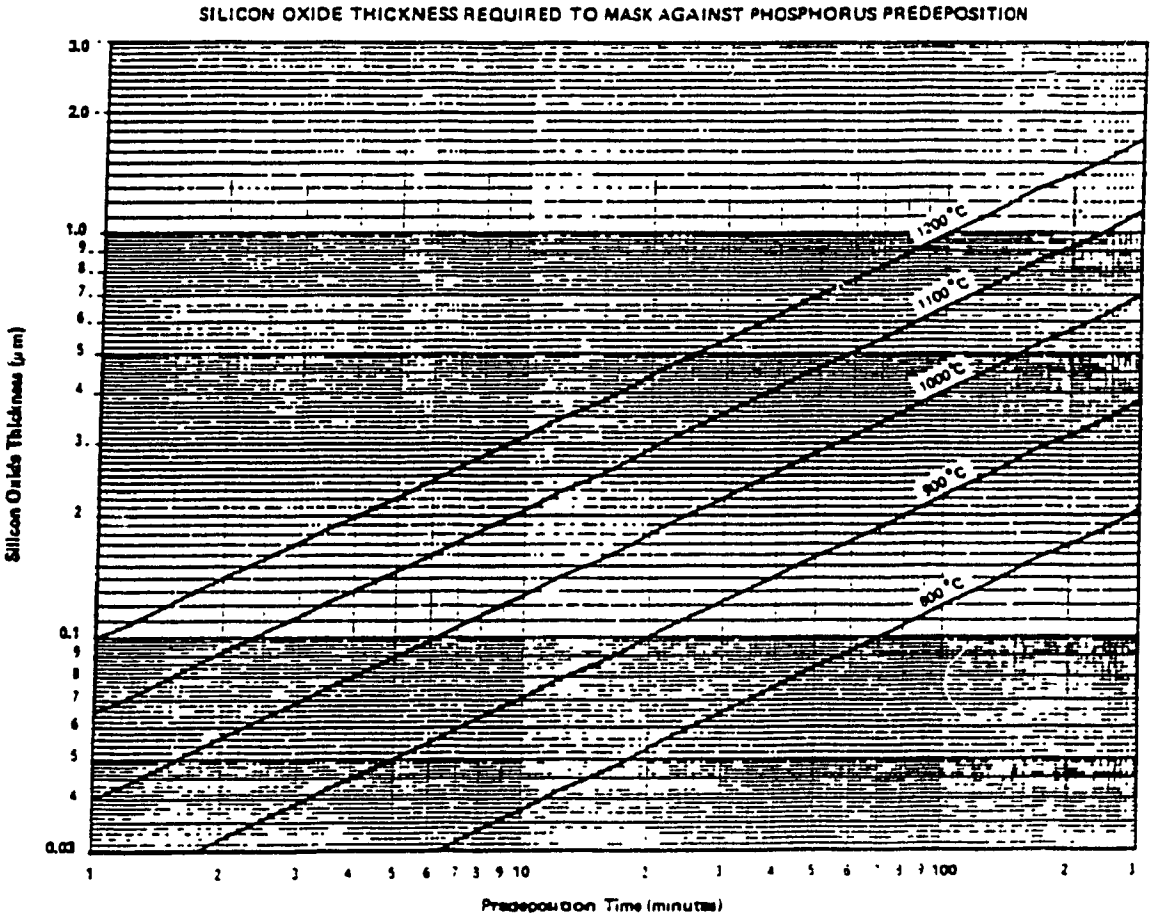


Figure 4.12: Oxide thickness needed to mask against P pre-dep.

Delineation of Phosphorus Diffusion Areas

The *Phosphorus Diffusion Mask (Mask #2)* is used to open the phosphorus diffusion areas in the masking oxide. The procedure is as follows:

1. Apply positive photoresist to wafer and bake again as discussed in chapter 3.

2. Expose wafer for 15 sec. through Mask #2 using mask aligner.

3. Develop, rinse, dry and bake wafers.

4. Etch away exposed oxide in windows delineated in the photoresist by dipping wafer in a solution of HF:NH_4F (1:4) until windows become hydrophobic (1-2 minutes).

5. Rinse wafers in DI water & blow dry with compressed N_2.

6. Remove photoresist by boiling wafers in two successive solutions of acetone, two minutes at a time.

7. Clean wafers using reverse-RCA procedure.

At this point, the wafers are ready for phosphorus pre-deposition.

Phosphorus Predeposition

Phosphorosilica does not exhibit the same problems as the Borosilica solution discussed in chapter 2 and therefore, it is used as the diffusion source

for P atoms. The solution has a phosphorus concentration of $5x10^{20}/cm^3$ and is processed in the same manner as Borosilica. A spun-on layer of Phosphorosilica acts as a constant source of phosphorus atoms for diffusion depths of up to 10 microns and therefore, its use ensures that the resultant dopant profile will have an erfc distribution.

Ideally, the diffusion itself is performed immediately following application of the Phosphorosilica to the wafers and in anticipation of this, the furnace is prepared as follows:

1. Boil diffusion boat in acetone for 1 minute; blow-dry with compressed N_2 gas.

2. Turn ON water bubbler (it should be set for a temperature of about 105 °C).

3. Set N_2 flow in gas lines for furnace to approximately 1 SCFH.

4. Install clean phosphorus tube in furnace and immediately connect gas hose.

5. Turn ON furnace. Adjust its temperature setpoint to 1000 °C.

ASIDE: The diffusion reactor and boat may be cleansed at high temperature if deemed necessary by repeating the procedure that was discussed earlier for the oxidation system.

The phosphorosilica is now applied to the wafers using the following procedure:

1. Ensure that wafers are dry by placing them in forced-air convection oven set to 150 °C for 30 minutes.

2. Let cool 10 minutes in ambient.

3. Using a syringe (dedicated for use with Phosphorosilica) equipped with a *Minisart*, 0.45 micron pore-size, solvent-resistant filter, apply 3-4 drops of the solution on the wafer surface and spin at 3000 r.p.m. for 30 seconds.

4. Dry wafers in forced-air convection oven set at 150 °C for 15 minutes.

5. Load wafer in diffusion boat and push to centre of reactor in 4-inch increments, waiting 2-minutes between each push. Once wafers have been at the centre for two minutes, the one-hour phosphorus pre-deposition timing is started.

Note that at the end of the pre-deposition, the wafers are not immediately pulled from the furnace. The ambient is instead changed to wet O_2 so that the final passivating oxide layer may be grown on the wafers.

Final Oxide Growth and Anneal

Recall that the final oxide layer is needed for three reasons. Primarily, a good quality oxide is required over the structure's entire surface so as to

properly passivate it (see chapter 2). Secondly, oxide is needed in the phosphorus diffusion windows so that contact holes may be selectively opened on these as well as on the boron diffusion windows. Finally, a 0.112 micron thick oxide layer is required on the device's front surface to act as an anti-reflection coating as was discussed in chapter 2.

The oxide is grown by keeping the wafers at the centre of the diffusion reactor at 1000 °C for another 13 minutes in a wet O_2 ambient set to a flowrate of approximately 1 SCFH. The oxide is subsequently annealed in a N_2 ambient (flowrate = 1 SCFH) for another 15 minutes at 1000 °C. This final oxide anneal improves the characteristics of the Si-SiO_2 interface as was discussed in chapter 2.

After the anneal, the loaded boat is slowly pulled to the mouth of the reactor (this should again take about 5 minutes). The loaded boat is then removed from the reactor mouth and the wafers are allowed to cool to room temperature (30-45 minutes) prior to further processing.

Delineation of Contact Windows Prior to Metallization

The *Contact Mask (Mask #3)* is used to open the contact windows in the diffusion fingers. This is once again performed with the use of positive photoresist:

1. Apply and bake positive photoresist to both sides of wafer (the front-side oxide must be protected during the final etching procedure).

2. Expose wafer backside through Mask #3 using mask aligner.

3. Develop, rinse, dry and bake wafers.

4. Etch away exposed oxide in contact windows in the photoresist by dipping wafer in a solution of HF:NH_4F (1:4) until windows become hydrophobic (1-2 minutes). Note that front-side oxide is protected during this procedure with the film of resin applied during step (1).

5. Rinse wafers in DI water & blow dry with compressed N_2.

6. Remove photoresist by boiling wafers in two successive solutions of acetone, two minutes at a time.

Delineation of Metallization Areas

The *Metallization Mask (Mask #4)* is used to delineate those areas where metal is to make contact with the wafer surface. This is again performed with the use of positive photoresist which is processed as described above. This time, the resin is not baked after it is exposed and developed. Rather, the resin-covered wafers are loaded into an aluminum evaporator in preparation for metallization.

Metallization

The metallization itself is performed in a vacuum chamber in which a 99.9999% pure aluminum pellet is placed on a tungsten heating element. The wafers are mounted face-down in the chamber, which is subsequently pumped down to approximately $1x10^{-3}$ Torr with a rotary pump. Vacuum is further improved with a diffusion pump that effectively evacuates the chamber down to a pressure of roughly $1x10^{-5}$ Torr.

When a satisfactory vacuum is attained, the pellet is heated until it begins to evaporate onto the loaded substrates. Using this technique, aluminum thicknesses of up to 1 micron may be obtained. With the evaporation completed, the devices are removed from their mount and subsequently soaked in acetone for approximately 2 to 3 hours so as to "float-off" the aluminum-covered photoresist. After the initial soaking period, the aluminum is rinsed off with a steady stream of pressurized acetone (such as that provided by a squeeze-bottle). The procedure is repeated until all traces of excess aluminum are removed.

The wafers are finally verified under a microscope to ensure that no shorts exist in the metallization pattern due to stray pieces of aluminum. The substrates are at this point ready for post-metallization annealing.

Post-Metallization Anneal

The final step in processing consists of heating the metallized samples at a temperature of approximately 450 °C in a "forming gas" ambient (typically composed of a mixture of H_2 and N_2 gas [20]) for about 15 minutes [21]. This procedure which is commonly performed in MOS Technology helps to further reduce the density of interface states at the Si-SiO_2 interface (see Chp.2).

At Concordia, the procedure is performed in a dedicated annealing furnace equipped with a sealed quartz reactor chamber. Devices are loaded into the reactor and the furnace temperature is subsequently controlled by means of a variac. Note that the reactor ambient is varied from N_2 to H_2, and the temperature at its centre is at all times monitored with the use of a type K thermocouple. Type K thermocouples are used because they allow the measurement of a wide range of temperatures [50]. The annealing procedure itself is performed as follows:

1. Load wafers in reactor chamber.
2. Purge reactor with N_2 gas for 5 minutes.
3. Light Bunsen burner located at the reactor output.
4. Blend-in H_2 gas in N_2 gas flow (about 50% H_2 & 50% N_2).
5. When gas at reactor output begins to burn, shut OFF N_2 gas flow.

6. Turn ON furnace. When temperature reaches 450 °C, stabilize reading by adjusting variac and then begin timing the 15 minute anneal cycle.

7. At the end of the cycle, shut OFF furnace and allow system to cool to about 80 °C in H_2 ambient.

8. Introduce N_2 in gas flow and shut OFF H_2 flow. The wafers are removed from the reactor after all traces of H_2 gas have been burned at the reactor output.

This final step completes IBC solar cell device fabrication. The test structures are now probed for verification of sheet resistance, contact resistance and for the probability of short or open circuits. Device performance is also characterized by means of test procedures that are discussed in chapter 5.

Chapter 5
Experimental Results

This chapter outlines the test procedures used in characterizing the solar cells obtained from the last fabrication run. This batch yielded 3 out of 6 working devices and was made using the process sequence described in chapter 4. In the pages that follow, the test results that were obtained from one of the better devices are discussed and in particular, its following parameters are presented:

1. n, p and metallization sheet resistances
2. n and p contact resistances
3. dark I-V characteristics
4. illuminated I-V characteristics
5. carrier lifetime

5.1 Sheet Resistance

The metallization and the p and n-type diffusion sheet resistances were obtained from the Van der Pauw test structures. The measurements were made with the use of a probe station equipped with four probe/chuck assemblies in which *Micromanipulator Model 7F* probe tips were installed.

The measurements themselves were made by placing a probe tip at the centre of each of the "pads" located around the Van der Pauw pattern's periphery. A constant DC current was then forced between a pair of adjacent pads and the resultant voltage was measured across the remaining two. As discussed in section 4.2.1, four separate I-V readings are obtained from each structure, from which the layer's average sheet resistance can be deduced through equation (4.2).

The measured I-V data for the metallization, phosphorus and boron diffusion structures is shown in tables 5.1 through 5.3, respectively (only two sets of data are shown for each diffusion). The corresponding average sheet resistance values are also indicated.

Table 5.1: Van der Pauw results (metallization).

	I (mA)	V (mV)	R_s (Ω/□)
	14.01	0.12	
	14.03	0.13	
	14.04	0.13	
Van der Pauw #1	14.04	0.13	0.041
	14.04	0.13	
	14.05	0.13	
	14.05	0.13	
Van der Pauw #2	14.05	0.13	0.042

average R_s for metallization = 0.042 Ω/□

Table 5.2: Van der Pauw results (phosphorus diffusion).

	I (mA)	V (mV)	R_s (Ω/□)
	19.95	34	
	19.92	34	
	19.85	32	
Van der Pauw #1	19.92	34	7.62
	19.97	35	
	19.97	35	
	19.98	35	
Van der Pauw #2	19.92	35	7.95

average R_s for phos diffusion = 7.79 Ω/□

Table 5.3: Van der Pauw results (boron diffusion).

	I (mA)	V (mV)	R_s (Ω/□)
	1.78	63.5	
	1.35	46.9	
	1.64	56.6	
Van der Pauw #1	1.28	44.4	158.20
	1.28	43.4	
	1.26	42.6	
	1.30	44.4	
Van der Pauw #2	1.27	42.6	153.43

average R_s for boron diffusion = 155.82 Ω/□

From these results, it can be concluded that both diffusions and the metallization thickness were relatively uniform across the wafer surface. Given the average values of sheet resistance, the metallization resistance and the dopant surface concentrations may be approximated as discussed in the following section.

Metallization Resistance

The typical thickness of an evaporated aluminum layer ranges from 0.4 to 0.6 μm. In this particular fabrication run, the metallization thickness was

made to be 0.9 μm in an effort to minimize metallization resistance. The contribution of the metallization resistance to the device's overall series resistance may be approximated by adding the resistance of the metal lines connecting the n and p pads to their respective bus bars and by adding to this result the resistance of the bus bars themselves. The dimensions of these structures are:

- line to n-pad: L = 2340 μm, W = 300 μm
- line to p-pad: L = 3380 μm, W = 300 μm
- n-bus bar: L = 9860 μm, W = 300 μm
- p-bus bar: L = 10060 μm, W = 300 μm

The metallization resistance may therefore be approximated as:

$$R_{Al} = R_{s\text{-}Al}\,[area(n\text{-}pad) + area(p\text{-}pad) + area(n\text{-}bus) + area(p\text{-}bus)]$$

$$= 0.042\,\Omega/\square \left[\frac{2340}{300}\square + \frac{3380}{300}\square + \frac{9860}{300}\square + \frac{10060}{300}\square\right]$$

$$= 0.042\,\Omega/\square \;(85.5\,\square)$$

$$= 3.590\,\Omega$$

This preliminary analysis indicates that the cell's series resistance will likely be quite high and that its conversion efficiency will be correspondingly lower than the expected value. Recall from chapter 2 that solar cell I-V characteristics are dramatically influenced by series resistances as low as 4 to 5 ohms.

Phosphorus Diffusion

In deriving the post-process phosphorus surface concentration from Irvin's curves, the diffused layer's junction depth, x_j, is needed in addition to its sheet resistance (see chapter 4). It should be noted that in the case of a phosphorus diffusion into an n-type substrate, "junction depth" refers to the point in the substrate at which the concentration of the diffused phosphorus atoms, N_P, equals the substrate background concentration, N_{BG}.

Although x_j is usually determined experimentally through junction staining techniques [40, p. 5-18 to 5-20], it may be approximated by using Fick's one-dimensional diffusion equation [41]. During the pre-deposition, the phosphorus surface concentration is kept constant and therefore, the boundary conditions become [41]:

a) $N(0,t) = N_o$ = constant
b) $N(\infty,t) = 0$
c) $N(x,0) = 0$
d) D_P = constant

Solving Fick's Law, ie.,

$$D_P \frac{\partial^2 N_P}{\partial x^2} = \frac{\partial N_P}{\partial t} \tag{5.1}$$

under these conditions, we obtain [41]:

$$N_P(x,t) = N_o \, erfc \frac{x}{2\sqrt{D_P t}} \tag{5.2}$$

Integrating equation (5.2) from x = 0 to x = ∞, the total number of phosphorus atoms, Q_P, deposited in the substrate during the 60 minute pre-deposition is [41]:

$$Q_P = 2\sqrt{\left(\frac{D_P t_{p\text{-}dep}}{\pi}\right)} N_o \tag{5.3}$$

where: N_o = constant P surface concentration
= $5 \times 10^{20}/cm^3$
D_P = P diffusion coefficient @ 1000 °C

Specifically [41],

$$D_P = D_o e^{-E_A/kT}$$

$$= 3.85\, e^{-3.66/(8.62x10^{-5}\cdot 1273)}$$

$$= 1.26x10^{-14}\ cm^2/\text{sec}$$

Thus:

$$Q_P = 2\sqrt{\left(\frac{1.26x10^{-14}\ cm^2/\text{sec}\cdot 3600\,\text{sec}}{\pi}\right)}\ 5x10^{20}\ cm^{-3}$$

$$= 3.80x10^{15}\ cm^{-2}$$

Now, during the subsequent 28 minute phosphorus drive-in at 1000°C (see chapter 4), the diffusion assumes a Gaussian profile [41]:

$$N_P(x,t) = \frac{Q_P}{\sqrt{\pi D_P t_{d-i}}}\ e^{-\frac{x^2}{4D_P t_{d-i}}} \qquad (5.4)$$

The junction depth may be calculated from (5.4) by replacing the phosphorus concentration, $N_P(x,t)$, with the background concentration, $N_{BG} = 4.5x10^{14}\ cm^{-3}$, and by replacing t_{d-i} with the drive-in time of 28 minutes (1680

seconds). Hence:

$$4.5x10^{14} = \frac{3.80x10^{15}}{\sqrt{\pi \cdot 1.26x10^{-14} \cdot 1680}} e^{-\frac{x_j^2}{4 \cdot 1.26x10^{-14} \cdot 1680}}$$

$$x_j = 3.42x10^{-5}\ cm$$

Now, given the diffused layer's measured sheet resistance, R_s, and its junction depth, x_j, its average conductivity may be calculated from equation (4.1):

$$\sigma = \frac{1}{R_s \cdot x_j}$$

$$= \frac{1}{7.79 \cdot 3.42x10^{-5}}$$

$$= 3742\ (\Omega \cdot cm)^{-1}$$

Finally, from Fig. 5.1 showing Irvin's curves for an n-type Gaussian diffusion profile [41], it can be deduced that an n-type layer having an average conductivity in excess of 1000 will also have an impurity surface concentration in excess of 10^{20}. Since a surface concentration of at least $5x10^{19}$ cm^{-3} is needed for the formation of good aluminum ohmic contacts to an n-type layer [40, p. 10-23], it is expected that for this fabrication run, the ohmic contacts were of high quality and therefore, low n-type contact resistances could be expected.

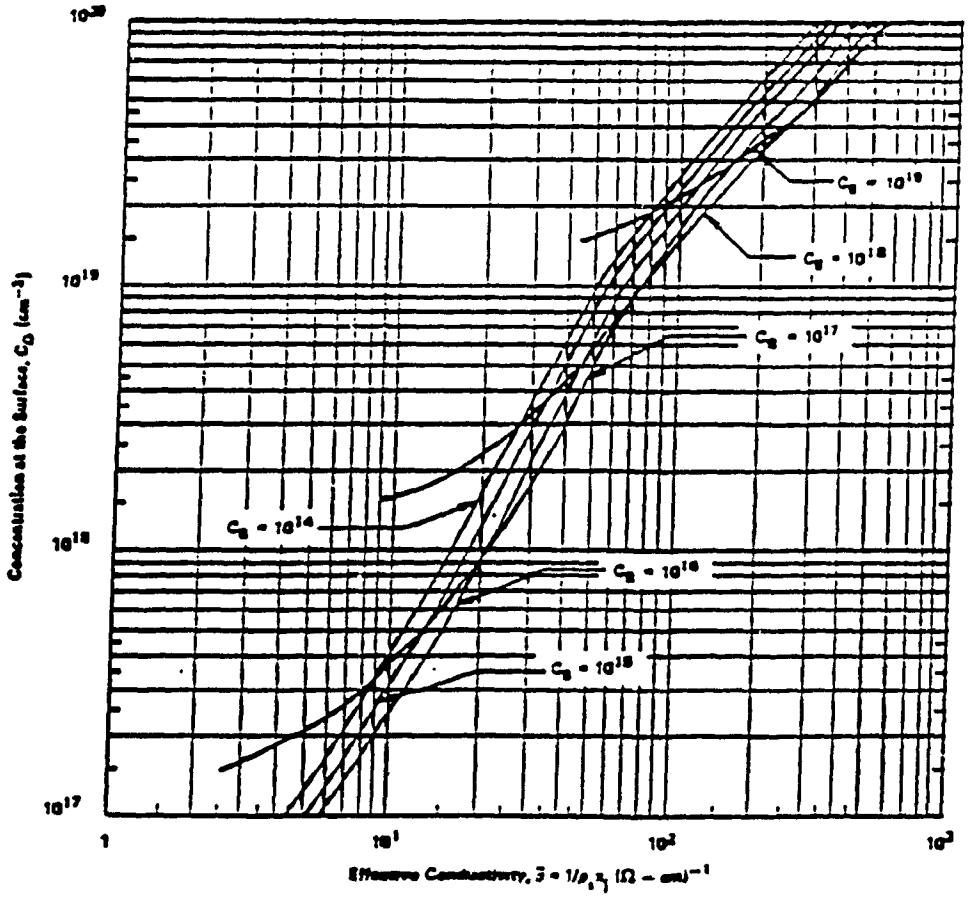


Figure 5.1: Irvin's curves for an n-type Gaussian impurity profile.

Boron Diffusion

The post-process boron surface concentration may be calculated from Irvin's curves in the same manner as was done for the phosphorus diffusion. In this case however, the junction depth is determined graphically since the boron dose is implanted rather than thermally pre-deposited into the substrate.

Impurities that have been annealed subsequent to implantation assume a Gaussian distribution that may be approximated as [40, p. 10-23]:

$$N_B(x,t) = \frac{Q_B}{\sqrt{2\pi}\sqrt{\Delta R_p^2 + 2Dt}} \exp\left(-\frac{1}{2}\frac{\Delta R_p}{R_p}\left[\frac{x - R_p}{\sqrt{\Delta R_p^2 + 2Dt}}\right]^2\right) +$$

$$\frac{Q_B}{\sqrt{2\pi}\sqrt{\Delta R_p^2 + 2Dt}} \exp\left(-\frac{1}{2}\frac{\Delta R_p}{R_p}\left[\frac{x + R_p}{\sqrt{\Delta R_p^2 + 2Dt}}\right]^2\right) \tag{5.5}$$

where:

t = post implant anneal time
D = diffusion coefficient of boron at the anneal temp
Q_B = implanted boron dose
N_B = boron concentration as a function of depth into the substrate and anneal time
R_p = projected range of implanted ions
ΔR_p = projected standard deviation of implanted ions

The implant and post-implant process parameters for the wafer under consideration are discussed in chapter 4 and are repeated here as follows:

implant energy	= 60 keV
implant dose (Q_B)	= 10^{15} cm^{-2}
R_p	= 0.1903×10^{-4} cm
ΔR_p	= 0.0556×10^{-4} cm
anneal temp	= 1000 °C
anneal time	= 60+60+13+15 = 148 min

By replacing these values and the diffusion coefficient of B in Si at 1000°C (=1.54x10^{-14} cm^2/sec, see section 3.2.3) in equation (5.5), we obtain an equation that describes the final boron impurity profile as a function of depth, x, in the substrate:

$$N_B(x,t=8880\text{sec}) = 2.29x10^{19}\, e^{-4.8x10^8(x - 1.9x10^{-5})^2} + 2.29x10^{19}\, e^{-4.8x10^8(x + 1.9x10^{-5})^2} \qquad (5.6)$$

If $N_B(x,t=8880$ sec) is plotted versus x, it is found that:

$$N_B(x_j,t=8880 \text{ sec}) = 4.5x10^{14} \text{ cm}^{-3} \text{ @ } x_j = 1.69\ \mu\text{m}$$

Given x_j and R_s for the boron impurity profile, the average conductivity of the diffused layer is again obtained from equation (4.1):

$$\sigma = \frac{1}{R_s \cdot x_j}$$

$$= \frac{1}{155.82 \cdot 1.69x10^{-4}}$$

$$= 37.97\ (\Omega \cdot cm)^{-1}$$

Using Irvin's curves for a p-type Gaussian diffusion profile [41] (see Fig. 5.2), the approximate boron surface concentration is found to be $N_B(x=0) \simeq 1.5x10^{19}$ cm^{-3} (recall that the theoretical calculations done in sect. 3.2.3 predict

a B surface concentration of 10^{19} cm^{-3}). Thus, referring to Fig. 3.7, it is again expected that good quality ohmic contacts were made to the p-type diffusions for

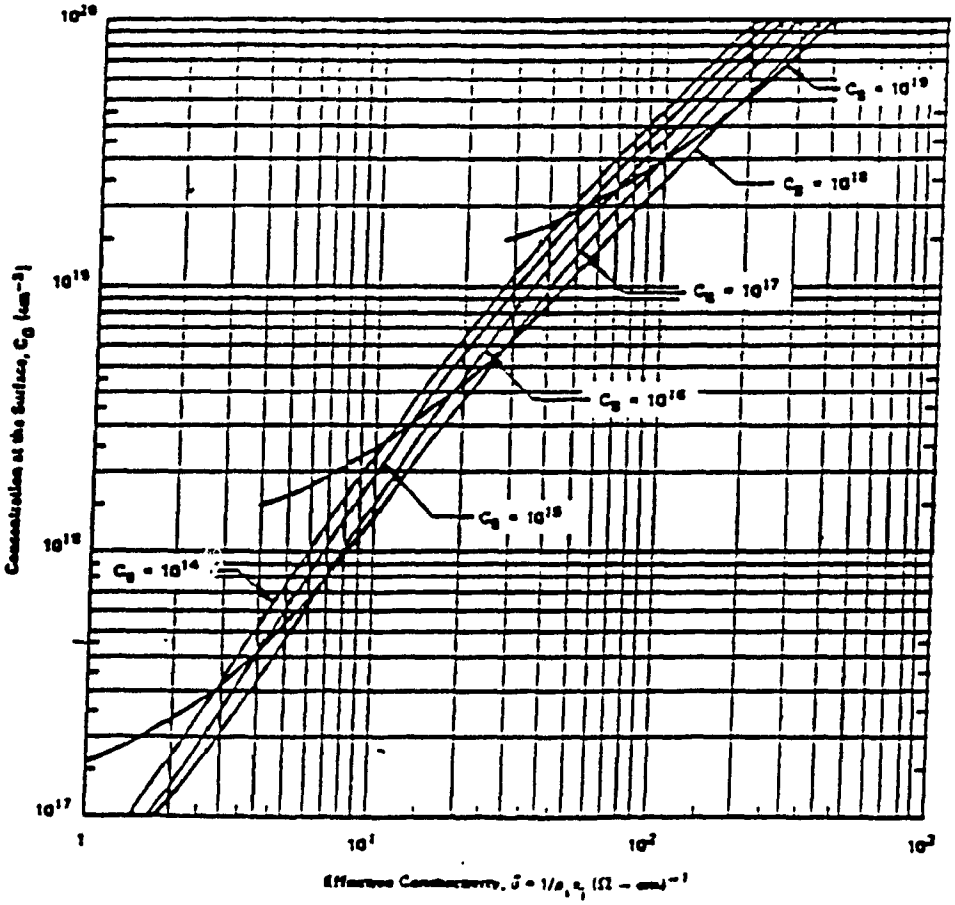


Figure 5.2: Irvin's curves for a p-type Gaussian impurity profile.

this fabrication run since the boron surface concentration is such that the specific contact resistance is expected to be less than 1 $\Omega \cdot cm^2$. These observations are further substantiated by the results presented in the next section.

5.2 Contact Resistance

The n and p ohmic contact I-V characteristics were verified prior to deriving their specific values of contact resistance. This was accomplished for each contact type (ie., n and p) by probing the two closest pads on their respective contact test structures and sweeping the applied voltage between the pads. The measurements were done with a *HP 4145 Semiconductor Parameter Analyzer* and the resultant I-V characteristics are shown in Figs. 5.3 and 5.4 for the n and p-contacts, respectively.

In the case of the n-contacts, the voltage was swept from -0.3 to +0.3 volts and the measured current at each of these voltages was found to equal:

$$I(V = +0.3V) = 48.81 \text{ mA}$$
$$I(V = -0.3V) = -48.83 \text{ mA}$$

In the case of the p-contacts, the voltage was swept from -1 to +1 volts and the measured currents were:

$$I(V = +1V) = 39.72 \text{ mA}$$
$$I(V = -1V) = -39.72 \text{ mA}$$

Since both contacts pass the same magnitude of current for a given positive or negative voltage bias and since the I-V curves are linear, it can be concluded that both the n and p-contacts approach the ohmic ideal. These curves also indicate however, that a significant voltage is dropped across the structures, in particular in the case of the p-contacts. These observations were verified by

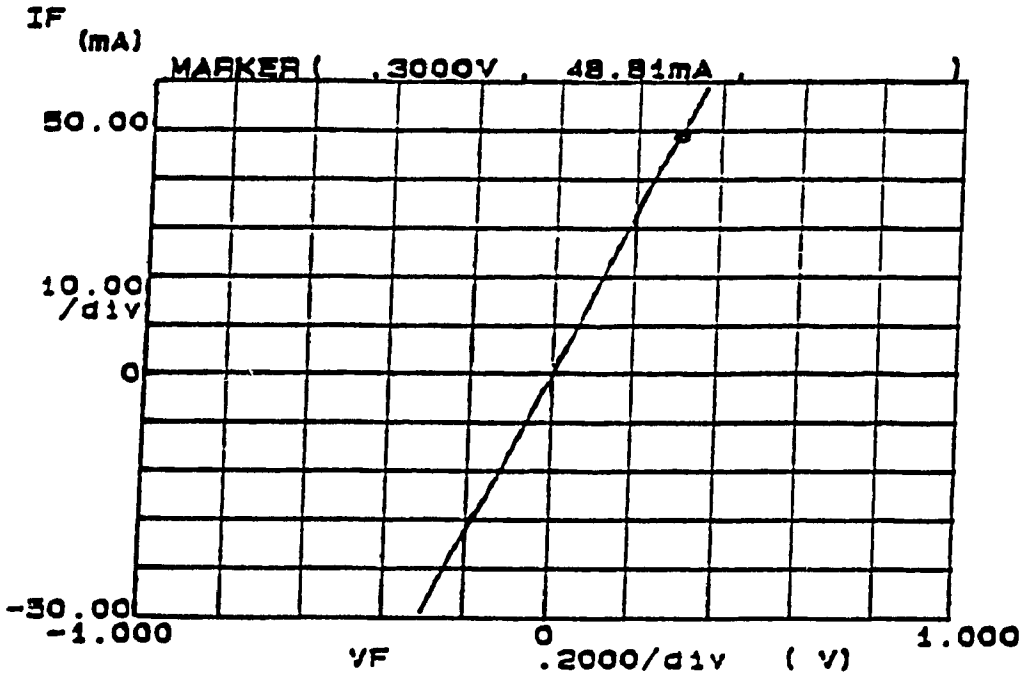


Figure 5.3: I-V plot for n-type ohmic contacts.

obtaining the n and p contact resistances from their respective test patterns using the procedure discussed in chapter 4.

The resistance of the probes that were used for the tests was determined prior to making any measurements. This was accomplished by placing their probe tips in contact with an aluminum layer and subsequently measuring the resistance between them. During these tests, the tip spacing was kept to within 1mm and the measured resistance was found to vary between 3.6 and 4.4 ohms.

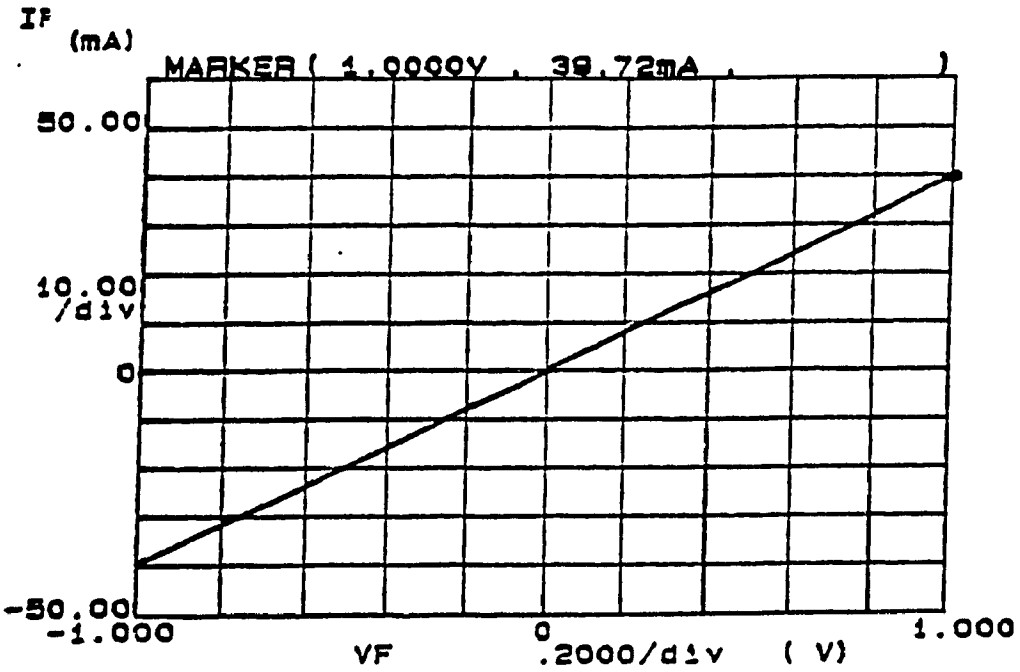


Figure 5.4: I-V plot for p-type ohmic contacts.

Consequently, all ensuing measurements were corrected by a factor of 4 ohms.

Recall that two patterns were included for each diffusion type in the mask design. Table 5.4 lists the corrected resistance readings that were obtained for the 5 pairs of measurements for each of the four patterns.

Table 5.4: Contact resistance test data.

	n_1	n_2	avg: n	p_1	p_2	avg: p
R_{12}(L=80μm) (Ω)	0.6	0.7	0.65	19.7	19.7	19.70
R_{23}(L=160μm) (Ω)	0.8	0.6	0.70	30.4	30.6	30.05
R_{34}(L=240μm) (Ω)	1.2	1.6	1.40	44.4	41.7	43.05
R_{45}(L=320μm) (Ω)	1.5	1.7	1.60	52.0	52.7	52.35
R_{56}(L=400μm) (Ω)	1.9	1.7	1.80	63.4	63.6	63.50

The non-linearity of the data for structure n_2 is likely due to irregular contact pad shapes for this particular test structure. That is, during the aluminum float-off procedure, it is possible that the break between the excess aluminum and the pads themselves was not very well defined. This may have produced some jagged edges around the periphery of the contact pads which in turn may have caused the discrepancy in the readings. Recall from chapter 4 that readings provided by contact resistance test structures are extremely sensitive to irregular pad shapes, causing at times differences of up to 100% between the measured and true values.

The resultant resistance versus contact spacing curves obtained from the n and p-contact patterns are shown in Figs. 5.5 and 5.6, respectively. The y-intercept of these curves is equal to twice the contact resistance, R_c, and their

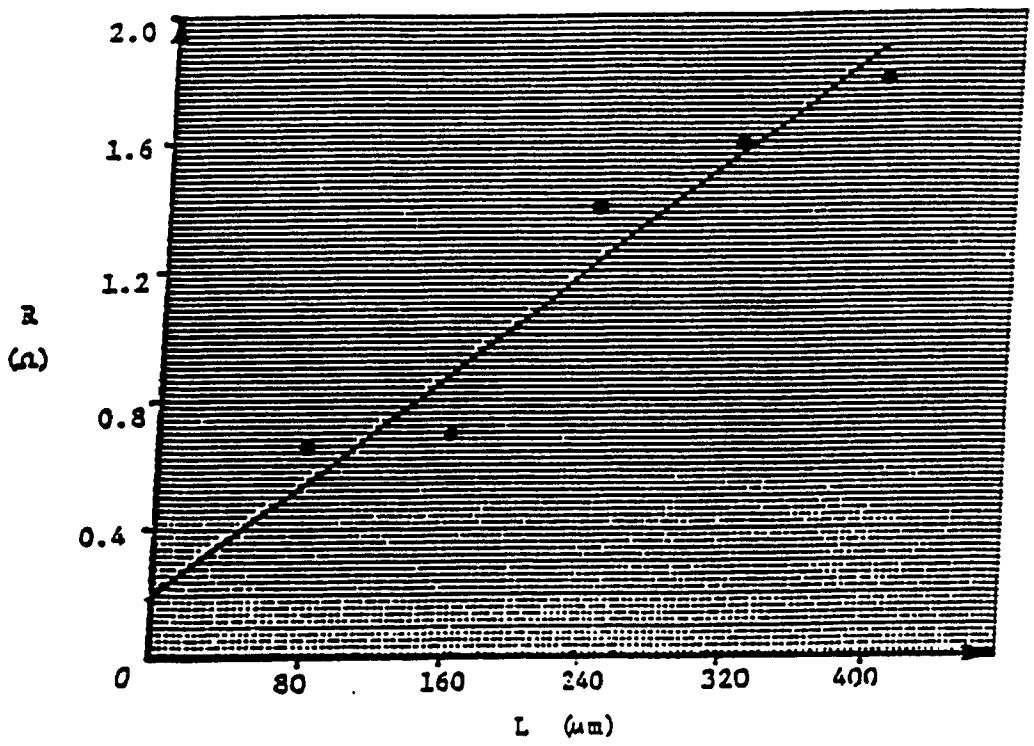


Figure 5.5: Resistance vs. contact spacing for n-type contacts.

slope is equal to:

$$SLOPE = \frac{R_s}{W}$$

where

W = width of the test pattern's diffused layer
= 1200 μm
R_s = sheet resistance of the diffused layer

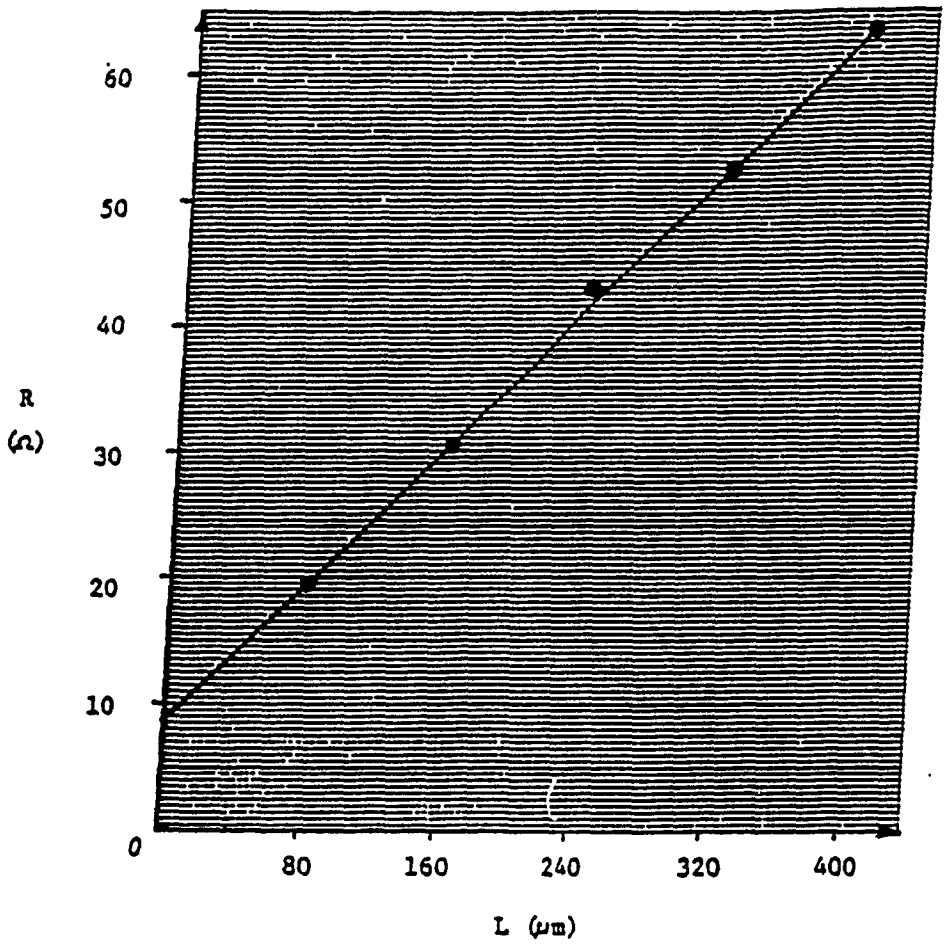


Figure 5.6 Resistance vs. contact spacing for p-type contacts.

The following data was deduced from the two plots:

p-type curve:

$$R_s = 165\ \Omega/\square$$
$$R_c = 4.25\ \Omega$$

n-type curve:

$$R_s = 5.16\ \Omega/\square$$
$$R_c = 0.1\ \Omega$$

Note that the sheet resistances calculated from these patterns are reasonably close to the values obtained from the Van der Pauw structures (ie., 155.82 Ω/□ and 7.79 Ω/□ for the p and n diffusions, respectively). The derived R_c results indicate that the contact resistance of the ion-implanted wafers is much less than the corresponding contact resistance of the wafers that had been processed with *Borosilica* (see chapter 2).

To calculate the cell's overall series resistance, R_{ser}, the bulk resistance, R_{bulk}, is needed in addition to the metallization and contact resistances calculated above. The bulk resistance may be approximated by considering that the total current output by the device under illumination is divided equally between the 13 sets of fingers at its rear. In passing from one n-finger to one p-finger, the current "sees" three different resistances which include (1) the resistance of the n-type diffusion, R_{n+}, (2) the resistance of the p-type diffusion, R_{p+}, and (3) the resistance of the lightly-doped bulk, R_n. These three resistances may be approximated by referring to the mask dimensions given in chapter 4 and by assuming that the current component in question flows from the centre of the n-finger to the centre of the p-finger:

$$R_{p+} = R_{sp+}\frac{150\,\mu m}{9980\,\mu m}$$

$$= (155.82\ \Omega/\square)(0.015\ \square)$$

$$= 2.337\,\Omega \qquad (5.7a)$$

$$R_{n+} = R_{s,n+}\frac{50\,\mu m}{9980\,\mu m}$$

$$= (7.79\ \Omega/\square)(5.010x10^{-3}\ \square)$$

$$= 0.039\,\Omega \tag{5.7b}$$

$$R_n = R_{s,n}\frac{200\,\mu m}{9980\,\mu m}$$

$$= \frac{\rho_n}{w_{cell}}0.02\ \square$$

$$= \frac{10\,\Omega\cdot cm}{300x10^{-4}cm}0.02\ \square$$

$$= (333.33\ \Omega/\square)(0.02\ \square)$$

$$= 6.667\,\Omega \tag{5.7c}$$

Thus, the total resistance seen by the current travelling from a p to a n-type finger is the sum of R_{p+}, R_{n+}, and R_n:

$$R_{p-n} = R_{p+} + R_{n+} + R_n$$

$$= 9.043\,\Omega \tag{5.8}$$

The total bulk resistance is therefore the parallel combination of 25 of these finger-to-finger resistances (see mask layout in Chp. 4):

$$R_{bulk} = \left[25\left(\frac{1}{R_{p\text{-}n}}\right)\right]^{-1}$$

$$= 0.362\ \Omega \tag{5.9}$$

Finally, the total cell series resistance, R_{ser}, is given by the sum of the two contact resistances, the metallization resistance and the bulk resistance:

$$R_{ser} = R_{Al} + R_{c,p\text{-}type} + R_{c,n\text{-}type} + R_{bulk}$$

$$= 3.590\ \Omega + 4.25\ \Omega + 0.10\ \Omega + 0.362\ \Omega$$

$$= 8.30\ \Omega \tag{5.10}$$

Referring to Fig. 2.12 in chapter 2, it can be concluded that this particular device's maximum developed power will be limited to less than 20 percent of its maximum achievable output. This approximate value of R_{ser} is compared in the next section with the value derived from the dark I-V curves.

5.3 Dark I-V Characteristics

Fig. 5.7 shows the device's dark I-V characteristic which was obtained with the *HP 4145 Analyzer*. Preliminary observations indicate that the device has good junction characteristics, but appears to have a high series resistance as is evidenced by the curve's slope in the forward linear region. In verifying these observations, the device's (1) forward series resistance, R_{scr}, and (2) its reverse saturation current, I_s, were obtained from the curve.

Series Resistance

The cell's series resistance is obtained from the inverse of the characteristic's slope in the forward linear region of operation. R_{scr} is found to be equal to approximately 8.3 ohms which is in agreement with the series resistance predicted in section 5.2.

The result further supports the observations made earlier that the device's optimal cell conversion efficiency will not be obtained. Referring to Fig. 2.12, it can be seen that a solar cell with an R_{scr} of 8.3 Ω will have its output power capability limited to about 17% of its maximum.

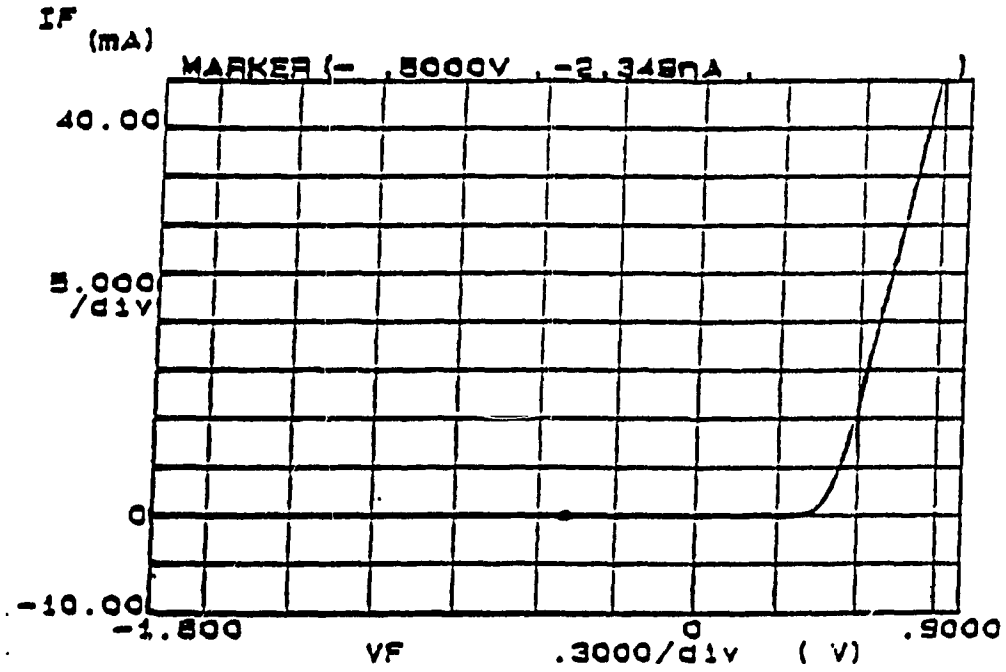


Figure 5.7: Dark I-V characteristic.

Reverse Saturation Current

The cell's reverse saturation current is obtained by measuring the current through the device at a biasing voltage of -0.5V in the dark. The resultant current was found to be I_s = -2.349x10^{-9}A (note that this is well above the HP4145 measurable minimum current), which can be compared with the theoretical value predicted by equation (2.22) by replacing the following parameter values:

$q = 1.6 \times 10^{-19}$ C
A = junction area = 0.39 cm^2 (see section 4.2.2)
$p_{no} = 500 \times 10^3$ cm^{-3} (from Eq. (2.23) with $N_{BO} = 4.5 \times 10^{14}$ cm^{-3})
$D_p = 12.59$ cm^2/sec (see section 2.1.1)
$\tau_p \simeq \tau_e \simeq \tau_{eff} = 55$ μsec (see section 5.5)
W = transition region width = 1.46 μm (see sect. 2.2.1)

Thus,

$$I_s = q A p_{no} \sqrt{\frac{D_p}{\tau_p}} + \frac{q n_i W}{\tau_e}$$

$$= (3.12 \times 10^{-14} C/cm) \sqrt{\frac{12.59\ cm^2/sec}{55 \mu\ sec}} + \frac{3.50 \times 10^{-13}}{55 \mu\ sec}$$

$$= 6.379 \times 10^{-9}\ A$$

The factor of 3 difference between the theoretical and experimental saturation currents can be explained by inaccuracies in the value estimated for average carrier lifetime, τ_e (see sect. 5.5) and the value derived for space charge region width, W.

5.4 Illuminated I-V Characteristics

Tests under illumination were performed on June 14, 1993 on the roof of Concordia University's Hall Building. This was a clear, sunny day and

therefore, it is assumed that the solar energy distribution available to the test sample at the time was that of the air mass 2 (AM2) spectrum. Recall that the AM2 spectrum is often used to represent the energy distribution at the earth's surface for average weather conditions [15, p. 3].

The device in question was mounted on a specially designed test rig that holds the wafer in place by means of a pivoting bracket assembly. The rig leaves the device's sunward side exposed while allowing contact to the wafer's n and p pads on its rear surface. The contacts are made by firmly pressing silver-plated copper wires to the pads and then coating the point of contact with a colloidal silver solution. The solution ensures the formation of good contacts between the dissimilar metals and is allowed to dry for approximately 15 minutes in air prior to testing.

The tests were carried out with the *HP 4145* which was programmed to vary the load seen by the solar cell. It was also programmed to simultaneously measure the device's terminal voltage and current. All experiments including those after removal of the front-side anti-reflection coating were made between 1:00 and 1:30 PM on the same day and the resultant illuminated I-V characteristics are shown in Figs. 5.8 and 5.9 (recall that the average cell active area is approximately 1 cm^2).

Once the characteristic for the device with the 0.112 μm AR oxide layer was obtained, the oxide was etched away by carefully placing the device's front surface in contact with a solution of NH_4F:HF (4:1) for 30 seconds. This was performed by grasping the wafer firmly and holding it horizontally with it's

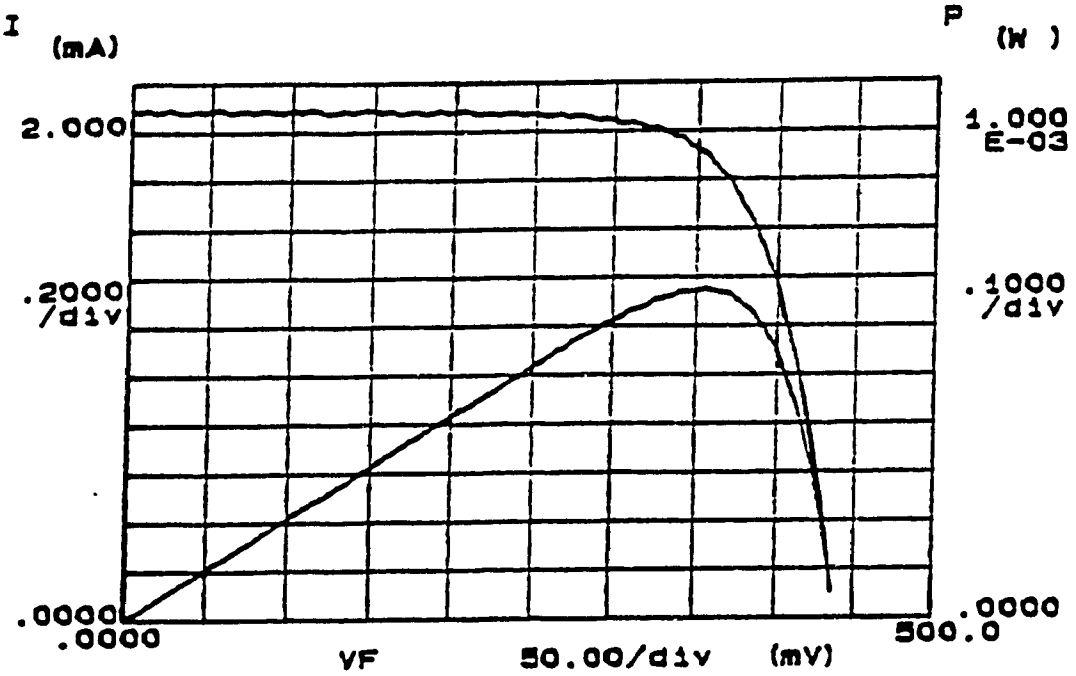


Figure 5.8: Illuminated I-V curve (with AR layer).

front-side facing downwards. It was then gently lowered to the surface of the solution where only its front face was permitted to touch it. No harm was done to the finger structure on the rear surface since the device was never completely submerged in the etchant. After the 30 second etch period, the wafer was thoroughly rinsed in DI water and dried. The hydrophobic nature of the device's front surface subsequent to the procedure indicated that all traces of SiO_2 had effectively been removed from it.

Power curves are also shown in addition to the I-V curves in Figs. 5.8 and 5.9. The curves were generated by the 4145 by programming it to multiply

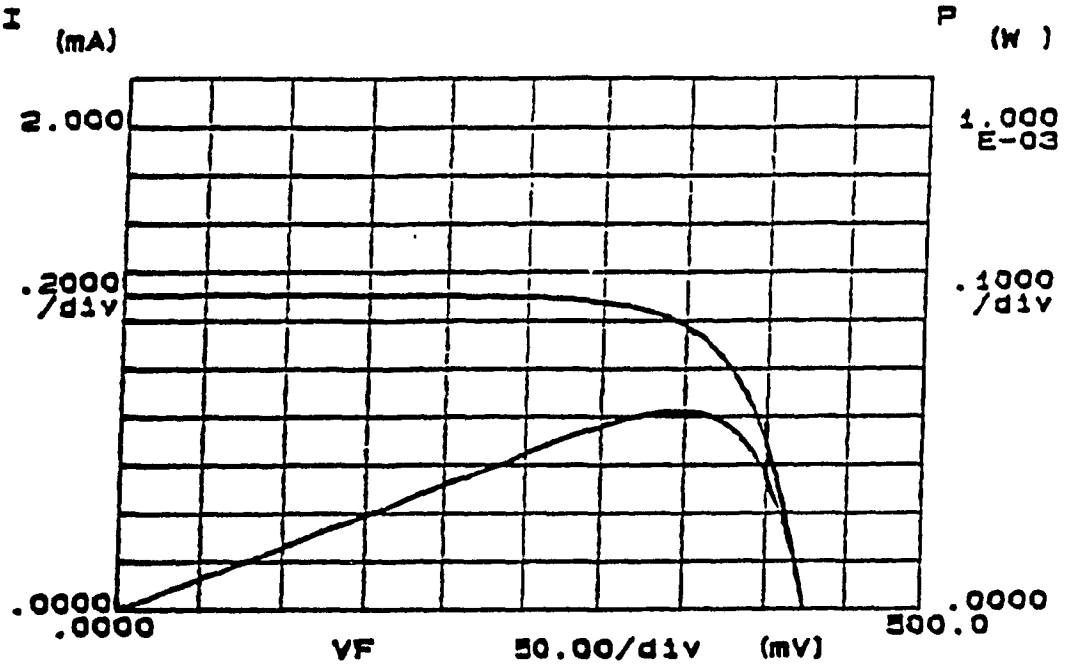


Figure 5.9: Illuminated I-V curve (without AR layer).

each sampled voltage with the corresponding current. The curve's peak indicates the location of the maximum power point on the I-V characteristic.

The following results were derived from these measurements:

with AR coat:

V_{oc} = 0.4374 V
I_{sc} = 2.092 mA
V_m = 0.3550 V
I_m = 1.905 mA

without AR coat:

$V_{oc} = 0.3742$ V
$I_{sc} = 119.7\ \mu$A
$V_m = 0.3000$ V
$I_m = 107.0\ \mu$A

The maximum power generated by the device is calculated from equation (2.27):

with AR coat:

$$p_m = V_m I_m$$
$$= (0.3550\ V)(1.905\ mA)$$
$$= 0.676\ mW$$

without AR coat:

$$p_m = V_m I_m$$
$$= (0.3000\ V)(107\ \mu A)$$
$$= 32.1\ \mu W$$

The magnitude of the maximum power output by the device without the SiO_2 front-side layer is roughly 21x smaller than its output with the layer. This is not surprising since a decrease in performance is expected for two reasons: (1) without the AR coat, approximately 30 to 50% of the incident photons on the bare silicon surface get reflected as compared with 10 to 20% with the SiO_2 layer (see chapter 2), and (2) it is expected that the device's surface recombination velocity is significantly increased by the removal of the

passivating oxide (see chapter 2). Since the AR coat would account for a 2 to 3x decrease in P_m, it can be concluded that the main reason for the significant decrease in power output is due to surface recombination. This supports the claims made in chapter 2 that SiO_2 remains one of the better materials for passivating silicon surfaces.

If it is assumed that the incident power density on the device under the given test conditions is roughly 0.0691 W/cm^2 [10, pp. 792-806] (AM2 conditions), the SiO_2-coated device's power conversion efficiency can be calculated from (2.27) as:

$$\eta = \frac{I_m V_m}{P_{input}}$$

$$= \frac{0.676\, mW/cm^2}{0.0691\, W/cm^2}$$

$$= 0.98\ \%$$

Normalizing this by a factor of 17% (see Fig. 2.12) to account for the cell's large series resistance, R_{ser}:

$$\eta_{norm} = \frac{1}{0.17}\ x\ \eta$$

$$= 5.76\ \%$$

Although this falls significantly short of the expected efficiency in excess

of 15%, the device's fill factor indicates that this result could be further improved. The fill factor may be calculated from equation (2.28):

with AR coat:

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}}$$

$$= \frac{(0.355\,V)(1.905\,mA)}{(0.4374\,V)(2.092\,mA)}$$

$$= 74\%$$

without AR coat:

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}}$$

$$= \frac{(0.3000\,V)(107\,\mu A)}{(0.3742\,V)(119.7\,\mu A)}$$

$$= 72\%$$

Note that the removal of the AR coat increases the surface recombination velocity, S (see Chp.2), but does not affect the bulk lifetime, τ_{bulk}. Hence, since I_s is a function of τ_{bulk} and not of S and since the device's series resistance, R_{ser}, is not a function of S, it can be concluded that FF, which is strongly dependent on I_s and R_{ser}, will not be influenced by the removal of the coat.

A fill factor of this magnitude indicates therefore that the device has very good junction characteristics (devices having efficiencies in the order of 22% typically have a FF of 80% under one-sun conditions [3,4]). Thus, since the

shape of the illuminated I-V curve is very sensitive to the device's series resistance (ie., as R_{scr} increases, the curve "rounds out" thereby reducing the FF), these results are particularly encouraging in that the device has a series resistance on the order of 8 ohms. Thus, if better process conditions in the future are successful in reducing this resistance, it is very likely that cells with fill factors approaching 80% will be obtained.

This result effectively indicates that the conditions under which the solar cell was fabricated were close to the ideal. Recall that an ideal junction is described by the ideal diode equation (c.f. Eq. (2.19)) [51]:

$$I = I_s(e^{qV/kT} - 1) \tag{5.11}$$

In reality, however, the I-V characteristic of a diode is largely dependent on process conditions, and therefore, its I-V characteristic is more accurately described by the following modified diode equation [51]:

$$I = I_s(e^{qV/nkT} - 1) \tag{5.12}$$

where "n" is the *ideality factor* and is a "measure of how close to the ideal were the conditions under which the physical device was fabricated" [51]. Considering the situation where the device's operating voltage approaches V_m, equation (5.12) reduces to:

$$I = I_o e^{qV/nkT}$$

$$\ln I = \ln I_o + \frac{qV}{nkT} \tag{5.13}$$

Plotting Eq. (5.13) on a semilog scale with the applied voltage, V, as the abscissa, a linear curve is obtained with a slope equal to

$$SLOPE = \frac{qV}{nkT}$$

Thus, as the device's ideality factor approaches unity, its I-V curve becomes much sharper (ie., the slope is maximized) and consequently, the cell's fill factor is maximized.

For comparison, tests were also performed on a commercial, single crystal silicon solar cell of conventional design. The device which had a total cell area of 8 cm^2, was purchased from *Radio Shack* and was tested under illumination using an *Oriel* solar simulator equipped with an AM1.5 filter. Tests revealed that the instrument was in need of calibration and therefore, its output level of illumination was not known. It could nonetheless be used for FF measurement, however, since the values of V_m, I_m, V_{oc} and I_{sc} could readily be obtained at that level of illumination, thereby permitting the calculation of fill

factor (ie., equation (2.28)):

$$FF = \frac{V_m I_m}{I_{sc} V_{oc}}$$

Several measurements made on the IBC device using this apparatus substantiated the assumption that FF is not dependent on insolation level (provided the device is being operating under low-level injection conditions). The measurements consistently yielded fill factors ranging from 72 to 74% which are in good agreement with the results obtained on Concordia's roof on June 14.

The following lists the commercial device's measured parameters under dark (ie., J_s and R_{scr}) and illuminated conditions (ie., FF):

$J_s = 32.1\ \mu A/cm^2$
$R_{scr} = 5.08\ \Omega$
$FF = 59\%$

The manufacturers claim a conversion efficiency of approximately 9.1% under AM2 conditions for this device. From these accumulated results, it can be concluded therefore that the IBC cell's low conversion efficiency is likely due to a low minority carrier lifetime in the substrate. The following section further discusses this possibility.

5.5 Minority Carrier Lifetime

The photoconductive decay method is commonly used to determine the effective minority carrier lifetime in a semiconductor sample [12, pp. 90-93]. In using the method, the sample's change in conductivity is monitored as a function of time after excess carriers are generated in the bulk. The carriers are usually generated by uniformly illuminating the sample's surface with a pulsed light source.

The conductivity of an n-type sample under dark, equilibrium conditions is given by:

$$\sigma = q\mu_n n_{no} + q\mu_p p_{no} \tag{5.13}$$

where: μ_n = electron mobility
μ_p = hole mobility
n_{no} = equil. concentration of electrons in n-sample
p_{no} = equil. concentration of holes in n-sample

When excess holes and electrons, Δp_n and Δn_n, are induced in the substrate, their concentrations decay exponentially and are given by:

$$\Delta p_n = p_n - p_{no} = \Delta p_{ni} e^{-t/\tau_p} \tag{5.14}$$

and

$$\Delta n_n = n_n - n_{no} = \Delta n_{ni} e^{-t/\tau_n} \tag{5.15}$$

where

Δp_{ni} = the excess hole concentration at t=0 (time at which pulsed light creates excess carriers)
Δn_{ni} = the excess electron concentration at t=0

Thus, under optical excitation, the change in conductivity, $\Delta\sigma$, due to the excess carriers is (from Eq. (5.10)):

$$\Delta\sigma = q\mu_n \Delta n_n + q\mu_p \Delta p_n \tag{5.16}$$

Now, if each photon impinging on the semiconductor surface creates an electron hole pair (EHP), then an equal number of excess holes and electrons will be created in the sample and consequently, $\Delta p_n = \Delta n_n$ [12, pp. 90-93] and equation (5.16) reduces to:

$$\Delta\sigma = q(\mu_n + \mu_p) \Delta p_{ni} e^{-t/\tau_p} \tag{5.17}$$

where it was assumed that the hole minority carrier lifetime, τ_p, is equal to the electron minority carrier lifetime, τ_n [12, pp. 90-93]. Thus, if $\Delta\sigma$ is monitored as a function of time after an excess carrier density is generated in the sample,

the effective carrier lifetime can be extracted from the exponential curve obtained [12, pp. 90-93].

Photoconductive decay measurements were made at l'Université de Montréal. A wafer from the same batch as the one considered in this chapter was used for the measurements and it was found that the effective minority carrier lifetime in the sample varied from approximately 50 to 60 μsec.

It was shown in the previous section that the removal of the SiO_2 passivating layer from the wafer surface causes an important increase in surface recombination velocity. Since the oxide on the test wafer's surface between the contact fingers was not removed prior to the lifetime tests, it is likely that the cause for the low effective lifetime is low bulk carrier lifetimes rather than high surface recombination velocities (see Eq. (2.13) in section 2.1.1).

Replacing $\tau_p = \tau_{eff} = 55$ μsec, equation (2.10) finds that the hole diffusion length in the sample is:

$$L_p = \sqrt{D_p \tau_p}$$

$$= \sqrt{(12.59\ cm^2/sec)(55 x 10^{-6}\ sec)}$$

$$= 263 \mu m$$

In section 2.1.1, it was found that in order to absorb most of the photons incident on a silicon substrate, its thickness had to be made at least 75 μm thick. Thus, most of the carriers are generated near the substrate's surface and in fact,

table 2.1 shows that a majority of the photons are absorbed at depths much smaller than 75 μm. It can be concluded therefore that with a diffusion length of only 263 μm, approximately $1\text{-}e^{-300/263} = 68\%$ of the photogenerated carriers never make it to the cell's rear surface which lies an average distance of 300 ± 15 μm away from the front surface (recall from chapter 4 that these devices use 300 micron-thick wafers). Hence, if 3x more carriers were successfully collected, we could expect a 3x improvement in efficiency (up to approximately 17% - see normalized efficiency calculation in section 5.4)

These observations indicate that low bulk minority carrier lifetimes are the likely cause for the device's unusually low energy conversion efficiency. This is discussed further in the following section.

5.6 Discussion

Equation (5.18) shows that a solar cell's energy conversion efficiency is strongly dependent on three factors including FF, I_{sc} and I_o:

$$\eta = \frac{FF \cdot I_{sc}(P_{input}) \cdot V_{oc}(P_{input})}{P_{input}}$$

$$= \frac{FF \cdot I_{sc}}{P_{input}} \cdot \frac{kT}{q} \ln \frac{I_{sc}}{I_s} \qquad (5.18)$$

Recall from section 5.4 that the device exhibited a fill factor of 74% which indicated good junction characteristics. Furthermore, the dark I-V measurements also indicated good junction characteristics in that reverse saturation currents in the nano-ampere range were measured. Since I_s is strongly dependent on bulk carrier lifetimes, (ie., from equation 2.22):

$$I_s = qAp_{no}\sqrt{\frac{D_p}{\tau_p}} + \frac{qn_iW}{\tau_e}$$

it is expected that future devices could have even smaller reverse saturation currents, provided that their bulk lifetimes could be increased to more typical values of 1 ms (see chapter 6).

Referring to equation (5.18), it can therefore be concluded that the device's low conversion efficiency is due to its small generated current density, $J_L = I_L/\text{area} = 2.092$ mA/cm^2 (AM2 spectrum). Fig. 5.9 plots (dotted curve) the maximum short circuit current density, J_{sc}, available from crystalline Si as a function of substrate thickness for AM0, AM1 and AM2 conditions [15, p.

71]. The calculation from the plot assumes that every photon absorbed by the substrate generates an electron-hole pair that ultimately gets collected and contributes to the overall generated photocurrent. From the curve for AM2 conditions, it can be seen that for a substrate thickness of 300 μm, the maximum achievable J_{sc} is about 33 mA/cm^2. This is 15x greater than the amount produced by the device under consideration.

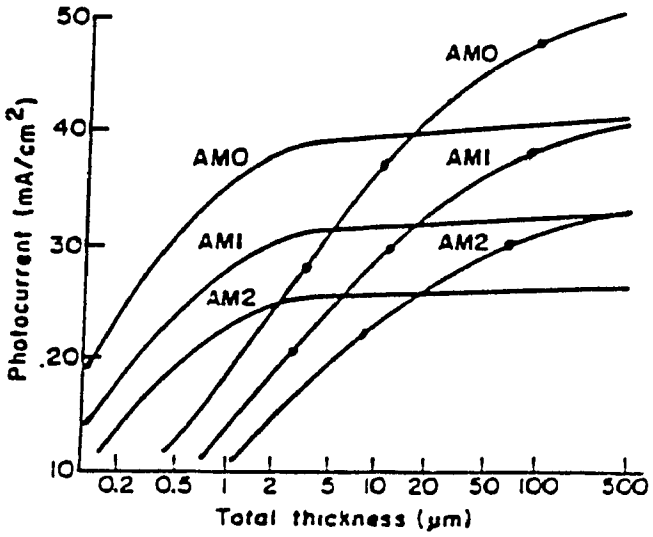


Figure 5.10: Maximum short circuit current density, J_{sc}, available from crystalline Si (dotted curve).

This analysis proves conclusively that not many generated carriers in the bulk reach the rear junction before recombining. Thus, I_{sc} is small and consequently, so is the device's conversion efficiency.

Assuming that improvements in the future (see chapter 6) produce the following results:

1. effective lifetime, τ_{eff}, increased to 1 ms
2. I_s decreased to 10^{-10} A due to increase in τ_{bulk}
3. J_{sc} increased to 30 mA/cm^2 due to increase in τ_{eff} and decrease in wafer thickness
4. FF increased to about 80% due to decrease in R_{scr}

equation (5.18) predicts that the cell's conversion efficiency under AM2 conditions will be:

$$\eta = \frac{FF \cdot I_{sc}}{P_{input}} \; 0.0259 \ln\left(\frac{I_{sc}}{I_s}\right)$$

$$= \frac{(0.80)(30\,mA)}{0.0691\,W} \; 0.0259 \ln\left(\frac{30\,mA}{10^{-10}A}\right)$$

$$= 17.6\ \%$$

This value much more closely approximates the expected efficiency of the IBC silicon solar cell design.

Chapter 6

Summary, Conclusions and Suggestions for Improvement

Interdigitated Back Contact silicon solar cells were fabricated at Concordia University's Microelectronics laboratory. In order to accommodate the more stringent process requirements of such devices, significant changes were made to the laboratory's silicon process technology prior to the development of a complete IBC fabrication sequence. In particular, it was demonstrated that the use of boron-doped spin-on sources should be avoided in the formation of p-n junctions since they give rise to diffusions with abnormally high contact resistances and excessive reverse saturation currents. Due to the design's sensitivity to process environment, a renovation procedure was also applied to the cleanroom facilities themselves so as to more closely match contamination standards established by the semiconductor processing industry.

Numerous experiments were made in fine-tuning the IBC solar cell

fabrication sequence developed for this work. After several attempts at using *Borosilica* as the boron doping source, the product was dropped due to problems encountered with doping uniformity, series resistance and junction quality. The source was replaced by an ion implantation sequence that yielded much better, reproducible results. Specifically, boron-implanted devices tended to have significantly lower reverse saturation currents, I_o, and p-type contact resistances, R_c (about 3 Ω vs. upwards of 1 kΩ), than equivalent devices fabricated with Borosilica as the doping source.

The final version of the IBC process sequence yielded devices with the following properties:

1. excellent junction characteristics with reverse saturation currents in the nano-ampere range and fill factors upwards of 70%.

2. excellent surface passivation characteristics as was evidenced by significant reductions in cell performance after removal of the front-surface SiO_2 passivating layer.

3. high series resistances on the order of 8 ohms due in large part to high metallization resistances and to (still) high p-type contact resistances.

4. low generated currents under illumination due to low minority carrier lifetimes in the bulk which keep their diffusion lengths well below the average cell thickness of 300 microns.

Due to #3 and #4, the devices' conversion efficiency remained well

below the expected value of 15 percent, even though the devices had very good junction characteristics. Changes that could be made to the established process sequence to improve upon the devices' performance are considered below.

In dealing with the high series resistance, two corrective measures could be taken. Primarily, the p-type contact resistance could be reduced by increasing the implanted dose of boron ions and by reducing the implant energy so as to diminish the projected range of the ions in the substrate. By proceeding in this manner, the boron surface concentration should be increased which should in turn cause a reduction in contact resistance.

Secondly, the metallization resistance could be reduced by using a better metallization process. This might involve evaporating a thicker layer of aluminum (greater than 0.9 μm as was done for these devices - note that the aluminum thickness was measured at Ecole Polytechnique using a quartz oscillator-based deposition monitoring system) [14], or the employment of a three-level metallization sequence such as Al-Ni-Au [1]. The latter sequence caps the original aluminum layer with a layer of nickel, which is itself covered with a layer of gold. These processes would reduce the device's metallization resistance to more acceptable values in the milli-ohm range.

The most obvious way of dealing with the devices' small minority carrier diffusion lengths on the order of 260 μm is by thinning the wafers down from 300 microns to about 150-200 microns. Such wafer thicknesses would not

appreciably diminish the maximum ideally obtainable short circuit current and they would not significantly complicate the fabrication process. The latter point was verified by tests made on the *COBILT* mask aligner with samples having an average thickness of about 150 microns.

The diffusion length itself can be significantly improved by increasing the lifetime of the minority carriers in the bulk. The use of float-zone silicon for fabrication should have resulted in lifetimes on the order of 1 ms [14] rather than those obtained on the order of 55 μs. It is likely that the bulk lifetimes were affected by the very high cooling rates utilized subsequent to high temperature processing (the wafers were pulled from the furnace centre in about 5 minutes).

Studies have shown that quenching after high temperature processing is very detrimental to carrier lifetime due to the fact that the procedure gives rise to recombination centres at E = 0.26 eV and at E = 0.49 eV within the silicon energy gap [52]. In avoiding the problem, cooling rates as low as 8°C/min are often used [14]. Thus, future process sequences could be modified so as to cool the wafers much more slowly subsequent to any high temperature step.

As a final observation, it should be mentioned that overall device performance may be further improved with the use of better AR coatings. For example, figure 6.1 plots the reflectance vs. wavelength for three different layers [22]. The double-layer SiO_2/SiN coating is formed through the use of sequential plasma-enhanced chemical vapor deposition (PECVD) techniques and

has an average reflectance of less than 8% over the range of wavelengths from $\lambda = 400$ nm to $\lambda = 1100$ nm. Recall that the 0.112 μm thick SiO_2 coating considered for this work has an average reflectance of about 18% over approximately the same range of wavelengths.

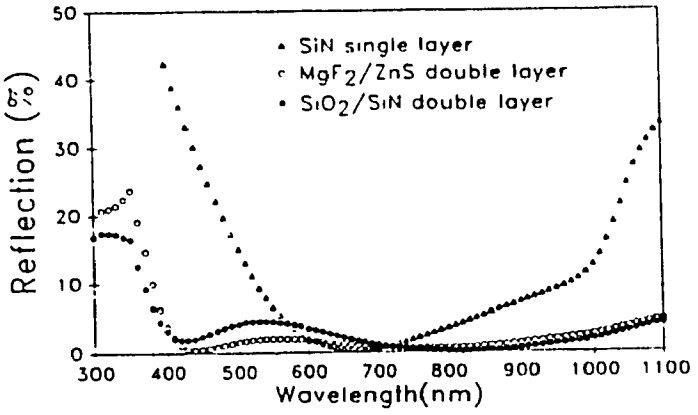


Figure 6.1: Reflectance as a function of wavelength for silicon cells with a) SiN coating, b) double-layer MgF_2/ZnS coating, and c) SiO_2/SiN AR coating.

In conclusion, the process sequence developed for this work allows the formation of very good quality junctions having excellent electrical characteristics. In addition to the requirement of good junction quality, however, the functioning of the IBC design depends critically on the lifetime of the photogenerated carriers in its absorber. Although the process sequence herein

yielded low carrier lifetimes on the order of 55 μs, it can be concluded that this value could be significantly improved. Future work could focus on ways of incorporating slow cool rates subsequent to any high temperature process steps such that impurity profiles are not dramatically affected by the new sequence and such that high carrier lifetimes are maintained in the bulk.

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