EMTP Simulation Of An HVDC System Operating With Weak AC Systems

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Abstract

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The study of the transient performance of an HVDC converter using EMTP requires detailed modelling of the controls and power system elements. Furthermore, due to the complexities associated with EMTP, considerable care has to be exercised during simulation. These requirements take on added importance particularly when the HVDC converter is operated with a weak ac system. In this thesis, modelling aspects of an HVDC system operating with weak ac systems are discussed.

Following a brief introduction to an HVDC system and its control characteristics, a CIGRE benchmark based HVDC system operating with a weak ac system is presented. A converter switch model is described along with the impact of the snubber circuit on the converter performance. Two gate firing units (GFU) are presented and their dynamic performance is assessed under fault conditions. A rectifier current controller, including a Voltage Dependent Current Limit (VDCL) circuit is presented. In addition, an inverter current controller and gamma controller are also presented.

To assess the transient performance achieved with the control schemes presented, results from EMTP based studies for this HVDC system under various ac-dc fault conditions are shown.

Acknowledgment

I sincerely express my gratitude to Dr. V. K. Sood and Dr. H. Jin for their financial support, valuable advice, time and patience during the course of this work.

The help offered by Computing Services, friends and colleagues at Concordia University is also acknowledged.

I would also like to thank my brothers Paresh, Janak and their families for giving me constant moral support.

Dedicated to my mother

Mrs. Lalitaben B. Khatri

and my late grandfather

Mr. Ranchordas C. Bhagat

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Chapter1
Introduction

The increasing use of high voltage dc (HVDC) transmission as a means of power transmission has created a need to assess its dynamic performance using digital simulators. The idea of digital simulation for HVDC systems was first proposed by [1] . The development of a general purpose Electromagnetic Transient Package (EMTP) [2] led to the possibility of a flexible digital simulator for modelling HVDC systems [3]. Since then, many authors have studied this problem with varying degrees of complexity [4,5,6,7,8]. One aspect of this problem which has not been well addressed is the operation of the HVDC system with weak ac systems.

This thesis deals primarily with the digital simulation of an HVDC system operating with weak ac systems. Different aspects of modelling and simulation such as generating gating signals, converter modelling, gamma measuring circuits etc., are discussed. An HVDC system based on the CIGRE benchmark system is studied in detail and results of the system under steady-state and fault conditions are presented.

1.1 Background on Digital Simulation of HVDC Systems

Traditionally, studies of HVDC systems have been carried out using analog simulators. With the increasing computation speed and power, digital simulators have been recently used for this purpose. The transient performance of an HVDC converter system is studied using computer packages like Electromagnetic Transient Package (EMTP) [2] and EMTDC. The simulation package used in this thesis is EMTP, developed in the late 1960's by Dr. Herman Dommel of University of British Columbia (UBC).

The modelling of a typical high voltage dc (HVDC) system incorporates the following elements:

1) thyristor converter bridges,

2) a converter transformers,

3) passive ac and dc side filters,

4) control units,

5) ac and dc side power systems.

In this study, a weak ac system is considered. The strength of an ac system connected to the terminals of a DC link is measured in terms of short circuit ratio (SCR) which is defined as

$$SCR = \frac{\text{Short Circuit level at the converter bus}}{\text{Rated dc power}} \qquad (1.1)$$

If the SCR is less than 3, the ac system is considered to be weak.

In a weak ac system, the harmonics of the commutation voltage at the converter ac side may lead to problems of harmonic instability. Hence, the commutation voltage cannot be used directly to derive gating signals for the converter valves. Gate Firing Units have to be used under these situations.

The weak ac system also causes other operational difficulties for the HVDC system. Digital simulation of these systems mount an additional challenge and thereby increasing the complexity of the problem in-terms of modelling the power system (converter model) and control systems (gate firing units).

1.2 Problem Definition

In most of the work previously done in the field of modelling HVDC system, a strong ac system has been assumed. For a strong ac system, the problem of using special synchronizing circuits like the gate firing units is eliminated. The process of deriving gating signals for the converter valves is hence relatively simple. Some authors have considered a weak system. However, many of the details required to model the HVDC system are not available. Hence as an educator or a utility planner, there is a need to model the HVDC converter system operating with a weak ac system in EMTP. The model developed here will provide details missing in other published work. In addition,the work presented here also gives detailed analysis of the model under various ac - dc fault conditions.

1.3 Literature Survey

Digital modelling of HVDC converter systems has been previously done with computer packages like EMTP, EMTDC, and special purpose programs.

In [3], modelling of an HVDC converter system was done using EMTP. This was the first attempt towards modelling an HVDC converter system using EMTP. The objective of [3] was to demonstrate the feasibility of EMTP to model an HVDC converter system and provide modelling details that would be useful to educators and researchers alike. In this work, the following assumptions were made:

1) An infinite (a strong) ac system was assumed. By assuming a strong ac system, the problems of generating gating signals for the converter valves is greatly simplified;
2) The dc transmission line was represented by a resistance, simplifying the dynamic behaviour of the system.

3) The inverter terminal was modelled simply by a back emf. Hence, the study of many problems like commutation failures, building a gamma measuring circuit and thereby implementing a gamma measuring circuit became less significant.

The paper introduced EMTP as a simulation tool for modelling HVDC converter systems and provided many useful details like transformer modelling, converter modelling, pulse generation for strong ac system, and the usefulness of TACS in EMTP to build the control circuitry. The authors also released EMTP data files that were very essential for educators. The authors, however, left many areas where the work could be further enhanced. For instance, models for special synchronizing units could be developed. This could pave a way for replacing the strong ac system with a weak ac system, building a gamma measuring circuit, and facilitating the implementation of a gamma controller. Consequently, the inverter model could be substituted by an inverter bridge. A Voltage Dependent Current Limit (VDCL) unit could be built making it possible to carry out tests like a dc line fault and a three phase fault on the existing model.

In [9], another attempt was made to demonstrate the effectiveness of EMTP to model power transmission systems like the HVDC converter system. In the proposed model, the author replaced the inverter model with an actual inverter bridge. A steady state operation of the entire model was demonstrated. The information provided was very useful as a starting point in modelling an HVDC converter system for educators. However, the author confined the operation of the system to one operating point and the problem of designing the controllers was not addressed. Furthermore, information required for modelling an HVDC converter system with a weak ac system in EMTP was still not available.

In [4], the first attempt was made towards modelling a realistic HVDC converter system. The authors modelled the Pacific Inter-tie HVDC system where they demonstrated

the effectiveness and capability of EMTP to model a realistic HVDC converter system. The authors in this model covered aspects of HVDC converter system modelling like weak ac systems and inverter control system absent in [3]. The authors replaced the inverter model by an inverter bridge, and added some protection units like the line protection unit, (VDCL). This work was used by Bonneville Power Administration (BPA) to study the Pacific Inter-tie HVDC system. Many details of this work like generation of firing pulses under weak ac systems, design of the rectifier and inverter control systems remained confined within BPA. Hence, from a user and educator stand point, many of the details required to model a realistic HVDC converter system in EMTP were still not available. Also, for the model presented, in addition to the faults studied, a dc line fault and a 3-phase fault cases were not included.

In [5], an EMTP based digital simulator was presented. This simulator used EMTP in parallel with a microcomputer containing a detailed converter model and extensive user inter active capability. This paper highlighted the versatility of using EMTP as a general purpose simulator. Since the objective of this paper was to present a simulator as a whole, many details necessary to build an HVDC converter system were not presented. A comprehensive fault analysis of the system using a digital simulator were not discussed.

In [6], modelling of digital controls for a Hydro-Quebec-New England HVDC system was done using the modified EMTP version. The results obtained were validated with actual field tests. Since the objective of this paper was to demonstrate implementation of digital controls using EMTP, again many details like the converter model, the method of generating gating signals, ac and dc side model of the system were not presented.

In [7,8], digital simulation of Manitoba Hydro's Nelson River HVDC system was carried out. The simulation was done using both EMTP and EMTDC. This paper made a use-

ful comparison between EMTP and EMTDC as simulation tools. Again, many of the details used to model the HVDC converter system were not presented. The fault analysis presented was not comprehensive. Many of the faults, like dc line fault and 3 phase ac faults, were not included.

In [10], a special purpose simulator was developed. The converter was modelled using graph theoretic approach. To facilitate this, the converter switch model was simplified and the valve was assumed to be ideal. Three converter control strategies were high lighted. They were :

a) Constant α control;

b) Individual phase control;

c) Equidistant pulse control.

The authors presented an interesting methodology to model an HVDC converter and some control strategies. However, the emphasis was still on a strong ac system. A lot of information that would be required to model a similar system in EMTP was not presented. Important information like a mathematical model of the converter which is required to design the PI controller, inverter control system of the HVDC converter system, were not revealed.

In [11], the authors took into account the effects of a weak ac system. They also presented algorithms for a gamma measuring circuit and a VDCL unit. The work also provided ac and dc side system models. It presented analysis for some of the faults like single phase and 3 phase fault at the inverter end. Again, the problem of generating gating signals for the converter in the presence of a weak ac system was not addressed. The details of the rectifier and inverter control system for implementation and the dc side fault analysis were not presented. Analysis of the system for dc side faults was not presented.

1.4 Proposed Approach

The objective of this thesis is to develop models and control schemes of an HVDC system operating with weak ac systems for EMTP simulation. In this thesis, the model developed in [3,9] is taken as the starting point. The strong ac system is replaced by a weak ac system. Existing switch models are modified by adding snubber circuits to protect against di/dt and dv/dt. Gate firing units are developed to produce gating signals in the presence of a weak ac system. The inverter model is replaced by a bridge and is equipped with a current controller. A gamma measuring circuit is built which facilitates the building of a gamma controller. In this model, protection circuits like the VDCL and ALPRET are added. A comprehensive fault analysis for various ac-dc fault conditions is carried out.

1.5 Thesis Outline

In Chapter 2, the CIGRE Benchmark based HVDC system is presented. Each building block of the system is briefly discussed. Control characteristics of the HVDC system are presented.

In Chapter 3, modelling details for control aspects of the HVDC system are presented.

In Chapter 4, results from the CIGRE benchmark HVDC system under various ac - dc fault/test conditions are presented. The transient performance of the HVDC system is assessed.

Finally, in Chapter 5, conclusions from this study, and recommendations for further work are provided.

Chapter 2
Structure and Control Characteristics of the HVDC Transmission System

2.1 Introduction

In this chapter, the CIGRE Benchmark based HVDC system operating with weak ac systems is presented. The system is divided into the following sub-systems, a) ac side of the power system, b) dc side of the power system, c) converter unit and d) control system. Each of the sub-systems will be discussed. An equivalent diagram of the HVDC system will be shown and control characteristics for this system will be discussed.

2.2 CIGRE Benchmark Based HVDC System

The HVDC system, shown in Figure 2.1, is based on the CIGRE Benchmark system [12] operating with a weak ac system having a Short Circuit Ratio of 2.5. In practice, a 12 pulse converter is used in the benchmark. To facilitate explanation of basic principles and reduce the computer simulation time and minimize memory requirements, a 6-pulse converter is modelled here. To reduce the 5th and 7th harmonics generated by a 6-pulse converter, a 5th and 7th harmonic filter is required and used. Note that the system modelled here is at 50Hz, and not 60Hz.

The HVDC system is divided into the following sub-units

a) Converter unit

b) AC side of the system

c) DC side of the system

d) Control system

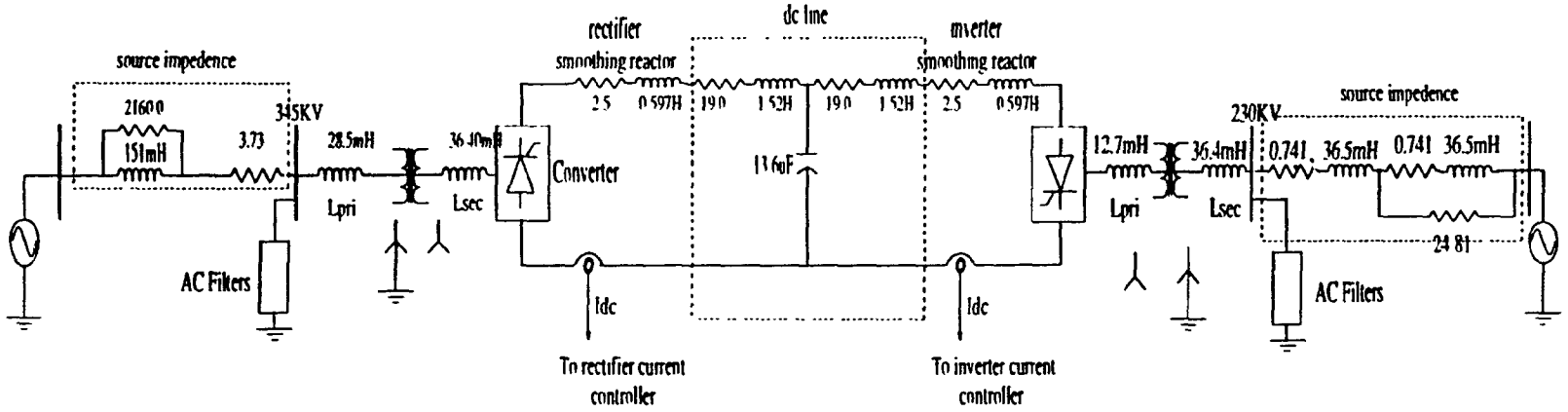


Figure 2.1: CIGRE benchmark model

a) Converter unit

A converter unit performs the conversion from ac to dc voltage or vice-versa. It can operate either as a rectifier or as an inverter by means of appropriate control units. The converter unit consists of two 3-phase bridges connected in series to form a 12-pulse converter unit (Figure 2.2). There are 12 valve units in each converter unit. To protect each valve against voltage and current surges, R-C snubber circuits are employed. Details of snubber circuits are presented in Chapter 4.

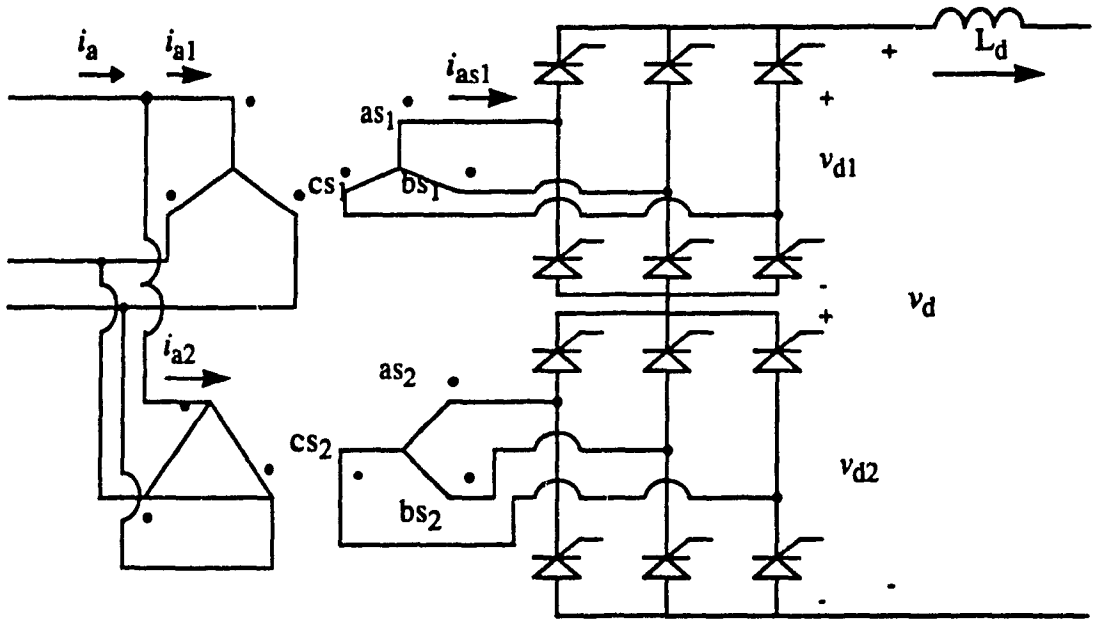


Figure 2.2: Twelve-pulse converter unit

The equivalent circuit of a rectifier, operating at constant ac voltage and constant firing angle is given in Figure 2.3 [13], while the equivalent circuit of an inverter is shown in Figure 2.4.

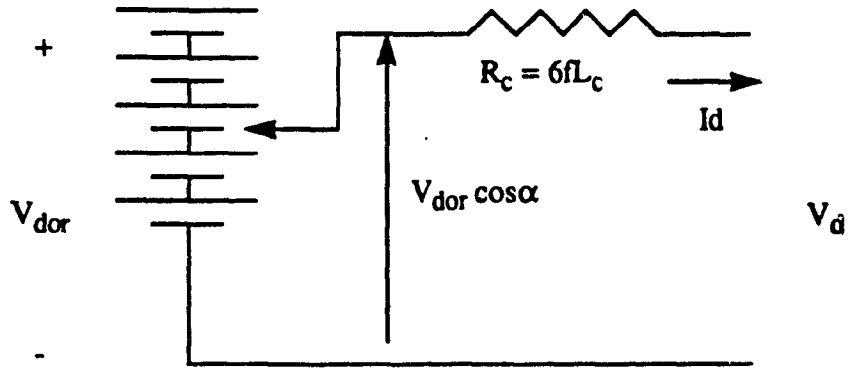


Figure 2.3: Equivalent circuit of bridge rectifier

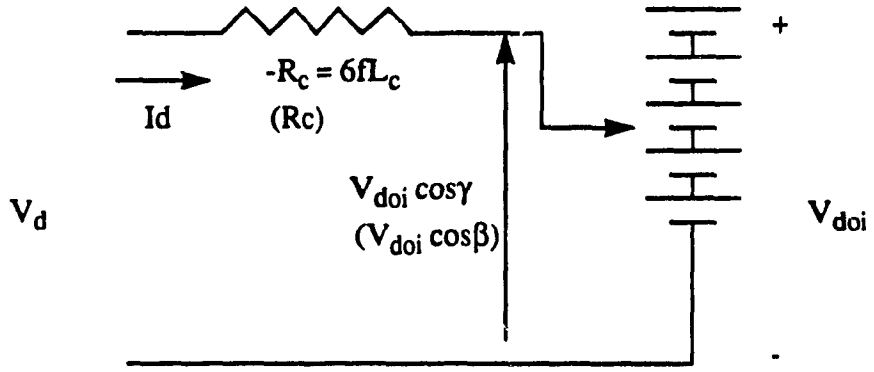


Figure 2.4: Equivalent circuit of inverter

b) AC side of the system

This sub-unit consists of an ac supply network, ac filters and transformers.

i) AC supply network: The ac supply network is represented by a Thevenin equivalent circuit. The Thevenin equivalent voltage represents the source voltage and the equivalent impedance represents the source impedance.

ii) AC filters: The ac filters are used to absorb the harmonics generated by the converter. In addition, they are also used to provide reactive power required by the converter unit.

The filters can be either tuned type or damped type or both (Figure 2.5).

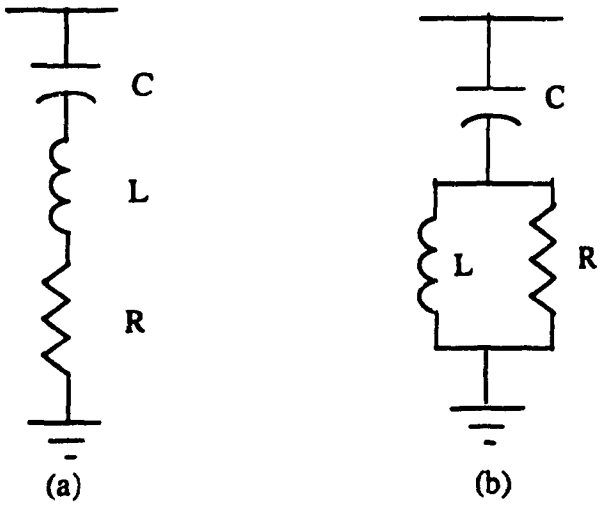


Figure 2.5 AC filters: (a) single tuned; (b) damped

The ac filter bank for this model is shown in Figure 2.6. This filter bank also includes filters for the 5th and 7th harmonics.

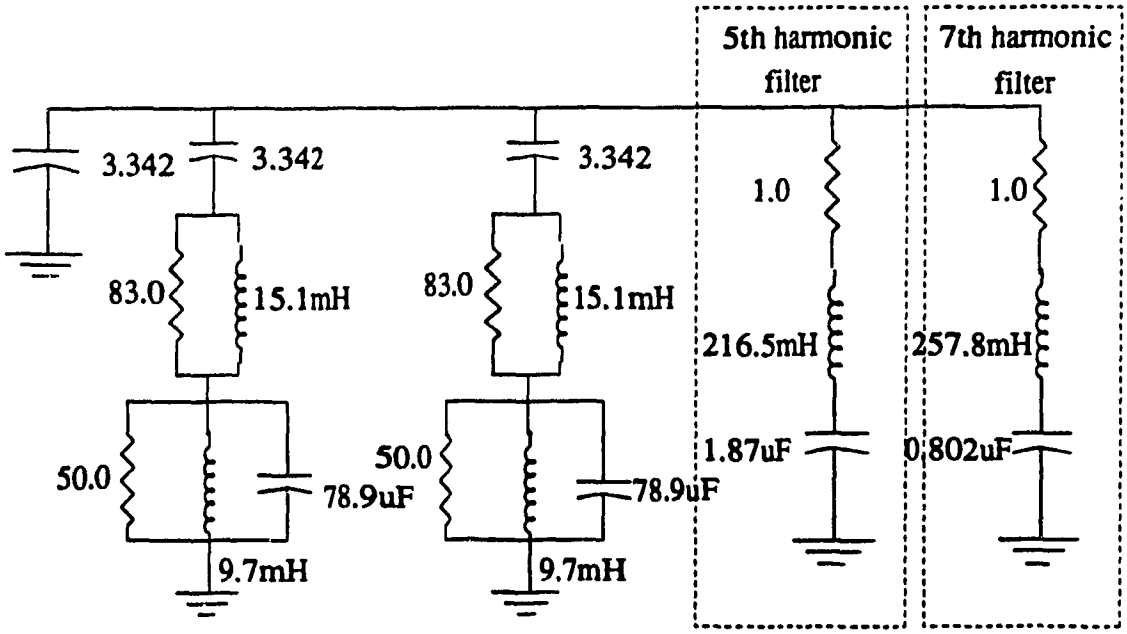


Figure 2.6: AC filter bank

iii) Converter transformer: The converter transformer can have the following configurations [14] a) three phase, two windings, b) single phase, three windings, c) single phase, two winding. The valve side (secondary) windings are connected in star and delta with neutral point ungrounded. On the ac side (primary), the transformers are connected in parallel with neutral grounded. Calculations for the primary and secondary impedances are shown in Appendix A.

c) DC side of the system

DC side of the system consists of a dc smoothing reactors, dc filters and dc transmission line.

i) DC filters: The harmonics in the dc current of the system can cause noise in communication systems. To eliminate these harmonics, a dc filter is used on the dc side of the system. This filter is a single-tuned filter tuned at the 6th harmonic.

ii) DC smoothing reactor: The dc smoothing reactor serves the following purposes:

1) To prevent consequent commutation failures in the inverter by limiting the rate of dc current increase during commutation in one bridge when the dc voltage of another bridge collapses.

2) To decrease the incidence of commutation failures in the inverter during dips in ac voltage.

3) To smooth the ripple in the dc current, and to prevent current from becoming discontinuous at light loads.

4) To limit the peak fault current in the rectifier due to a short circuit on the dc line.

The HVDC system under consideration consists of a rectifier side and an inverter side smoothing reactor, each having a value of 0.597H.

iii) DC transmission line: The dc transmission line is represented by an equivalent T-network shown in Figure 2.7. The dc line is tuned close to the fundamental frequency to intentionally increase the operational difficulties of the system. Higher order harmonics at the dc side of the converter are filtered out by the transmission line. From the equivalent circuit of the transmission line shown in Figure 2.7, the following transfer function can be derived.

$$T_{lc} = \frac{Z_3}{(Z_2+Z_3)Z_1+Z_2Z_3} \qquad (2.1)$$

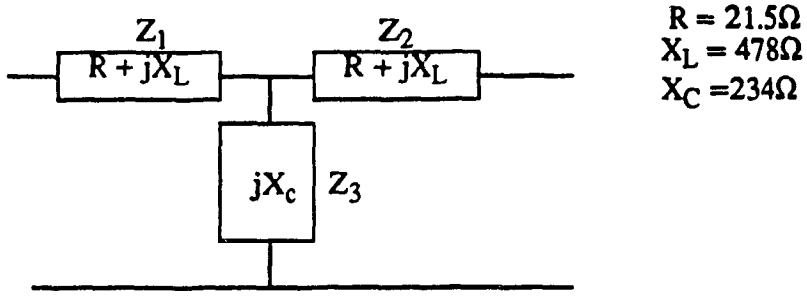


Figure 2.7: Equivalent circuit of dc transmission line

This equation is used while designing the controllers

d) Control System

The control system consists of the following elements:

i) Rectifier current controller

ii) Inverter current and gamma controller

iii) A Voltage Dependent Current Limit (VDCL) unit

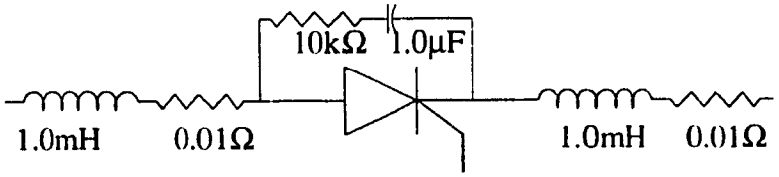
iv) A gate firing unit.

Details regarding the control system are presented in Chapter 3.

2.3 HVDC Converter Modelling

In an actual HVDC converter, each valve is constructed with many hundreds of thyristors in series. Each valve has a di/dt protection inductor usually with saturation characteristics. Furthermore, each thyristor in the valve has a parallel RC snubber and voltage-grading resistor. During switching and conduction periods, the thyristors have forward voltage drops and power losses.

In the simulated converter model, each of the 6 valves of the converter is modelled (Figure 2.8) as an ideal switch (Type 11 in EMTP). Using an ideal switch means that the device physics (i.e. turn-on and turn-off times, reverse recovery currents etc) are not represented. Never-the-less, even this limited switch model allows useful simulation studies for system-related phenomena.



Type 11 switch

Figure 2.8: Converter switch model

In the simulated EMTP model, the di/dt limiting inductors and RC snubber also serve relevant numerical purposes:

a) the di/dt inductors separate two ideal switches being connected to a common node, and

b) the RC snubber provides an alternative current flow path when the switch opens an inductive circuit.

A judicious choice of these parameters is therefore necessary to serve the twin objectives of numerical stability and circuit fiability. Data for these parameters is rarely specified by researchers who model HVDC converters (e.g. CIGRE Benchmark model does not specify these parameters). As an example, a test with values of R ranging from 0.2kΩ to 10.0kΩ and C from 0.0125μF to 1.0μF is shown in Figure 2.9. It is evident that inappropriate values of the RC snubber can lead to erroneous measurement of delay angles, overvoltages and even cause mal-operation of the circuit. In the case of a converter operating with weak ac systems, this can lead to particular difficulties.

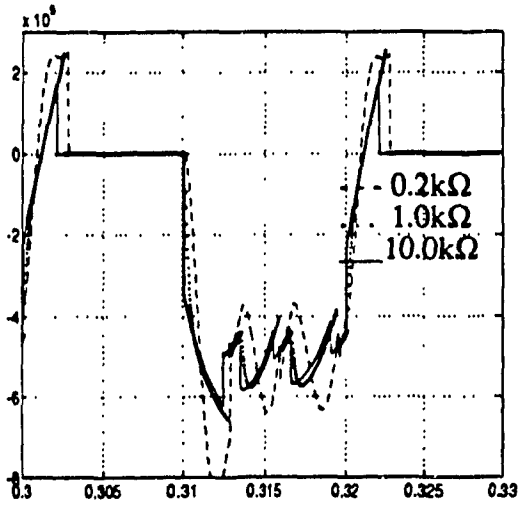


Figure 2.9 a: Valve voltage for different $R_{snubber}$

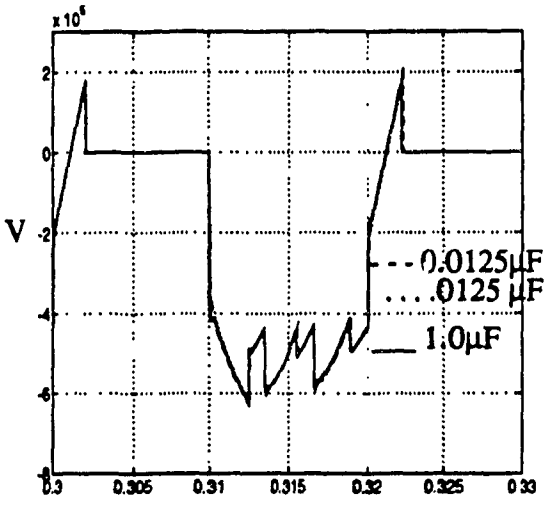


Figure 2.9 b: Valve voltage for different $C_{snubber}$

It is noted that the R values has a bigger impact than the C value within the range of snubber parameters tested. After optimization, R = 10kΩ and C = 1.0μF were selected for the snubber; it is pointed out that these values may not have any correlation with an actual snubber circuit used in practice. However, these values provide satisfactory commutation voltage for the switch used and the corresponding system model. The corresponding val-

ues for the di/dt limiting inductors are L = 1.0mH and R = 0.1Ω With these parameters, the measured values of dv/dt and di/dt are 0.152kV/ms and 2kA/ms respectively (Figure 2.10).

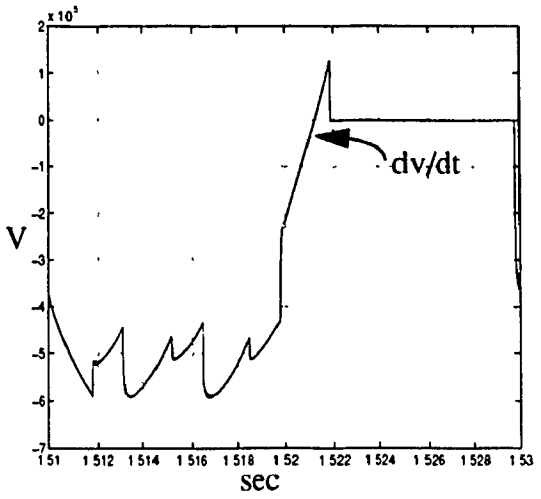


Figure 2.10 a: Valve voltage showing dv / dt

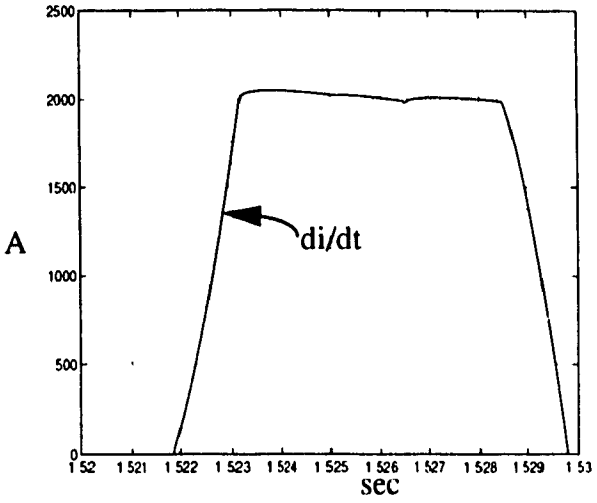


Figure 2.10 b: Valve current showing di / dt

2.4 Control Characteristics of an HVDC System

Using the equivalent circuits of the rectifier and inverter, an equivalent circuit for an HVDC converter system valid under steady state conditions is derived [13] and is shown in Figure 2.11

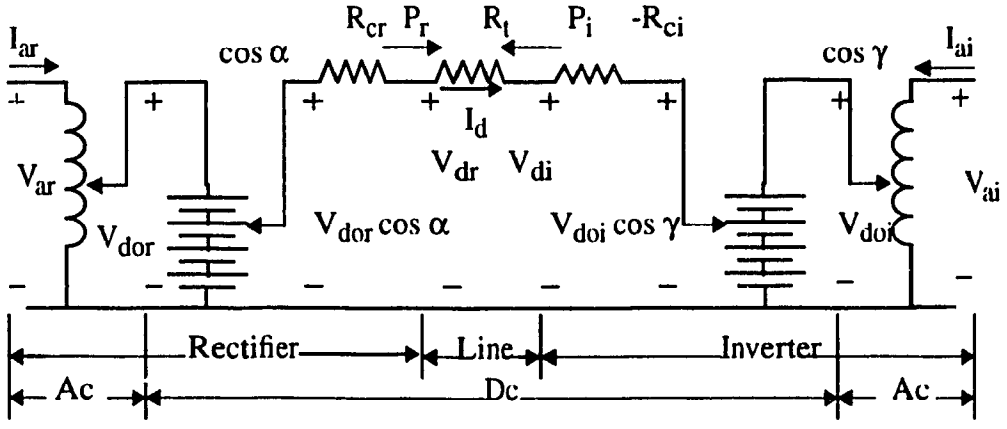


Figure 2.11: Equivalent circuit of an HVDC converter system

In Figure 2.4.1, the variables and parameters are

V_{dor} , V_{doi} : no load ideal dc voltages for rectifier and inverter respectively,

R_{cr} , R_{ci} : equivalent commutating resistance,

R_t : equivalent resistance of the line,

α : firing angle for the rectifier;

β : firing angle for the inverter,

γ : extinction angle.

The current I_d in the line is given by [13] as

$$I_d = \frac{V_{dor}\cos\alpha - V_{doi}\cos\gamma}{R_{cr} + R_t - R_{ci}} \qquad (2.2)$$

In (2.2), it is assumed that the inverter is operating with constant extinction angle. The dc link current, I_d is directly proportional to the difference of the two internal voltages, V_{dor} cosα and V_{doi} cosγ, and is controlled by these voltages. These internal voltages can be controlled through either the ac voltage or the firing angle. The ac voltage can be controlled by changing the tap settings of the converter transformers. In the gating unit control, the firing angle of the converter is adjusted to regulate the internal voltage. The method of controlling the gating unit is faster than changing the tap settings of the converter transformers.

Rectifier and inverter characteristics are plotted in rectangular coordinates (Figure 2.12), of direct current I_d and direct voltage V_d. If the rectifier current is controlled by the current controller, the rectifier characteristic is a vertical line (AB in Figure 2.12). If the inverter voltage is controlled by the gamma controller, the inverter characteristics is given by line CD (Figure 2.12). The slope of line CD is decided by R_{ci} and R_t. If R_{ci} is greater than R_t, the line CD has a negative slope. The operating point is given by the intersection of the lines AB and CD, point E in Figure 2.12. This operating points also confirms the fact that at any given point there can be only one voltage and current value.

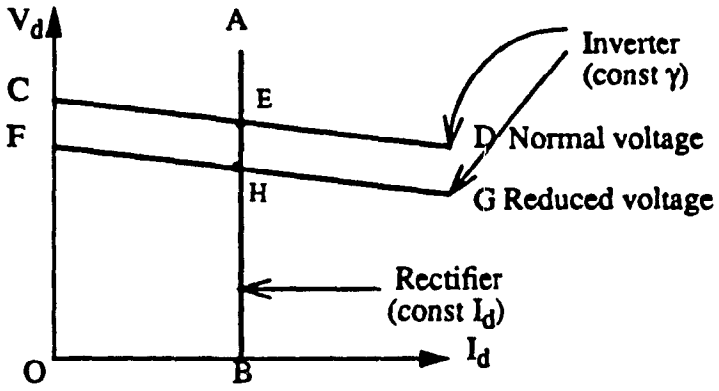


Figure 2.12: Rectifier and inverter characteristics

Lines AB and CD can be shifted by changing the appropriate references. To illustrate the shifting process, a rectifier case is considered. The rectifier characteristics can be shifted by changing the current reference, which is one of the inputs of the current controller, the other input being the measured current. If the measured current is less than the current reference, the controller advances the firing angle, raising the rectifier voltage in proportion to cosα and hence raising I_d. If the opposite is true, alpha is increased thereby reducing I_d.

At the inverter end, the inverter characteristics are raised or lowered by changing the tap settings of the transformer, or gamma controller is used. To study the behavior of the controllers for rapid changes in dc voltage which could be due to a short circuit on the ac system or collapse of the voltage of one valve group, a case is studied where there is a reduction in the inverter voltage. A reduction in the inverter voltage causes its characteristics to shift downwards from CD to FG (Figure 2.12). The new operating point is H. The power is reduced in the same proportion as the voltage since the current remains unchanged.

A decrease in the ac voltage at the rectifier end will cause a proportional decrease in

the dc voltage provided, cosα remains constant. The current controller will act towards maintaining a constant current by reducing alpha, causing the dc voltage to rise. This process will continue until alpha reaches alpha-min. The rectifier characteristics thus consists of two line segments, one is the minimum firing angle α_0 and other is constant current, as shown in Figure 2.13 by ABH.

A dip in the rectifier voltage shifts the rectifier characteristic down to A'B'H, which does not intersect with the inverter characteristic. This will cause the current and power to reach zero after a short delay due to the dc reactors. Thus a shift in the rectifier will cause a drastic change in the current and power. To avoid this drastic change, the inverter is also provided with a current controller. The reference current to the inverter current controller is set below the rectifier current reference by ΔI which is typically 10 - 15%. The inverter characteristic is now DFG, consisting of two segments, one is for gamma-min, and other for constant current. The operating point is now L.

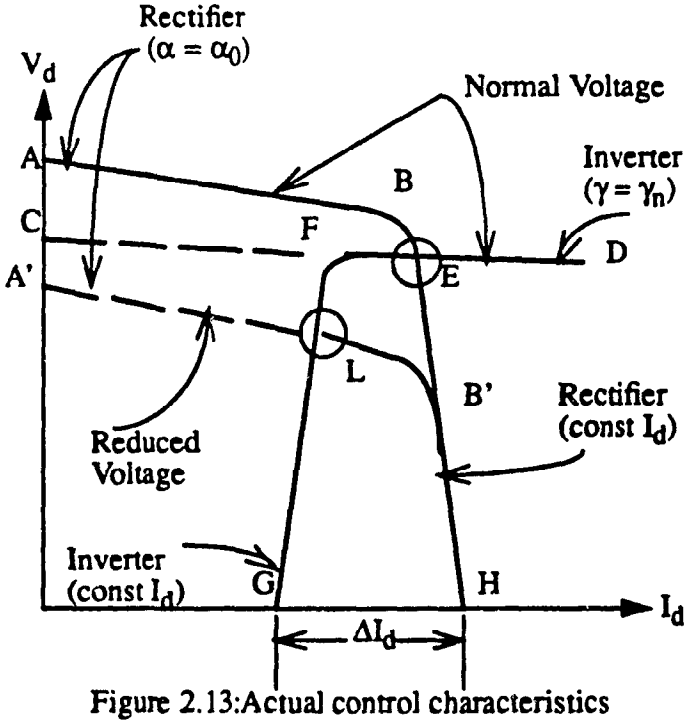


Figure 2.13:Actual control characteristics

2.5 Summary

The CIGRE Benchmark based HVDC system was presented. The structure of the system like the ac and dc sides of the power system were presented along with the control system and converter unit. An equivalent circuit of the system was presented. A converter model was presented which incorporates a di/dt and dv/dt protection circuits. The impact of the RC snubber circuit on the converter performance has been studied. Control characteristics for the HVDC system were also derived.

Chapter 3
Simulation of the HVDC Converter System - Control Circuits

3.1 Introduction

In this chapter, control circuits of the CIGRE benchmark based HVDC converter system operating with a weak ac system are presented. The control circuit consists of a gate firing unit, a current controller for the rectifier and inverter side, a gamma controller for the inverter side and a Voltage Dependent Current Limit (VDCL) for the rectifier.

Two types of gate firing units (GFUs) which use a voltage controlled oscillator (VCO) in conjunction with a phase locked loop are first presented. Their performance is studied under steady state and dynamic test conditions. A comparison between the performance of the two GFUs is made using a rectifier test system. In addition, a rectifier current controller along with a Voltage Dependent Current Limit (VDCL) is presented. Finally, an inverter with a current and a gamma controller is presented. A gamma measuring circuit necessary for the gamma controller is discussed. A design procedure for choosing the parameters of the PI controllers is presented.

3.2 Gate Firing Units (GFU)

The gate firing unit is an important element in the rectifier/inverter control circuit. It provides correct synchronization of the firing of thyristor switches under conditions such as distorted ac voltage signals, loss of commutation voltage and harmonic distortion. Two types of gate firing units are used in practice, a conventional GFU and a DQ-type GFU.

The conventional GFU uses a single ac signal. By contrast, the DQ-type GFU (also referred to as the Transvector type [15]), has a 3 phase ac to DQ (2 phase) transformation. This DQ-type has been used for motor drive applications for many years. Its first application to an HVDC system was made at Chateauguay, Quebec in the middle 1980's. One advantage claimed of the DQ-type GFU was its superior immunity to disturbances and harmonic distortion.

In the following, the operating characteristics and design of these two types of GFU are presented.

3.2.1 Conventional GFU

The block diagram of a conventional GFU is shown in Figure 3.1. In this circuit, the commutation voltage, assumed to be $V_{com} = \sin(\omega_1 t + \theta_1)$, is multiplied by a feedback signal which is $Vcos = \cos(\omega_2 t + \theta_2)$. The error voltage Verror is obtained according to eq 3.1

$$V_{error} = \sin(\omega_1 t + \theta_1)\cos(\omega_2 t + \theta_2)$$

$$= 0.5\sin([(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)]) + (0.5\sin[(\omega_1 + \omega_2)t + (\theta_1 + \theta_2)]) \quad (3.1)$$

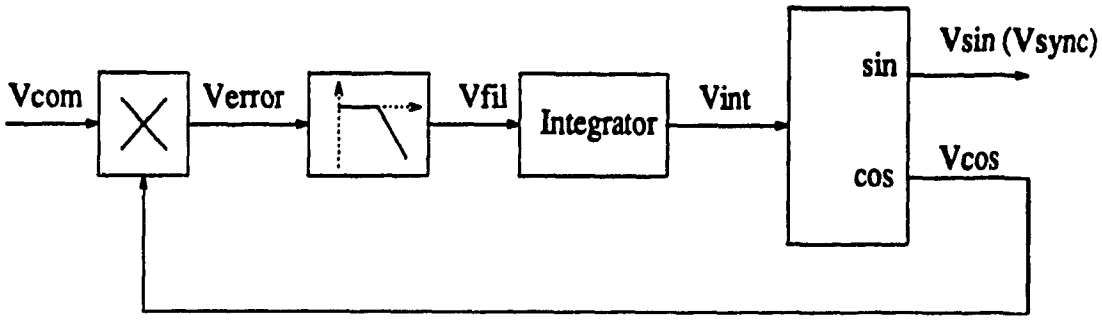


Figure 3.1: Block diagram of a conventional GFU

The first term in (3.1) represents the error between the synchronizing voltage and the commutation voltage due to the frequency and phase difference. In the feedback signal Vcos has the same frequency but different phase angle than that of the commutation voltage Vcom. This term becomes a dc component. Under steady state, the synchronizing voltage will be locked to the commutation voltage. In this case $\omega_1 = \omega_2$ and $\theta_1 = \theta_2$, and the first term will be zero. The second term is an unwanted ac component which has a frequency of $2\omega_1$ under steady state.

In order to extract the dc error signal, and filter out the unwanted ac component, a low-pass filter having the transfer function $\frac{\omega_c}{s+\omega_c}$ is used. The output is passed onto an integrator with a transfer function of 1/sTi. The integrator output, Vint, is used to modulate the frequency and phase of a free-running Sine-Cosine oscillator to generate the output signal Vsync. Under steady state conditions, the feedback signal Vsync will be in phase and have the same frequency as the commutation voltage, Vcom. Thus, Vsync can be used as a stable unpolluted signal to derive the voltage zero-crossover points to provide the timing reference points for the GFU.

Figure 3.2 shows the waveforms of the conventional GFU. It can be seen that the second harmonic ac component in the error signal is reduced by means of a low-pass filter, thus reducing its impact on the overall system operation. The bottom superimposed signals in Figure 3.2 show the commutation voltage, Vcom, and the synchronizing voltage, Vsync. Note that, in-order to clearly see the phasor relationship between Vcom and Vsync, the magnitude of Vsync has been deliberately increased by 20%.

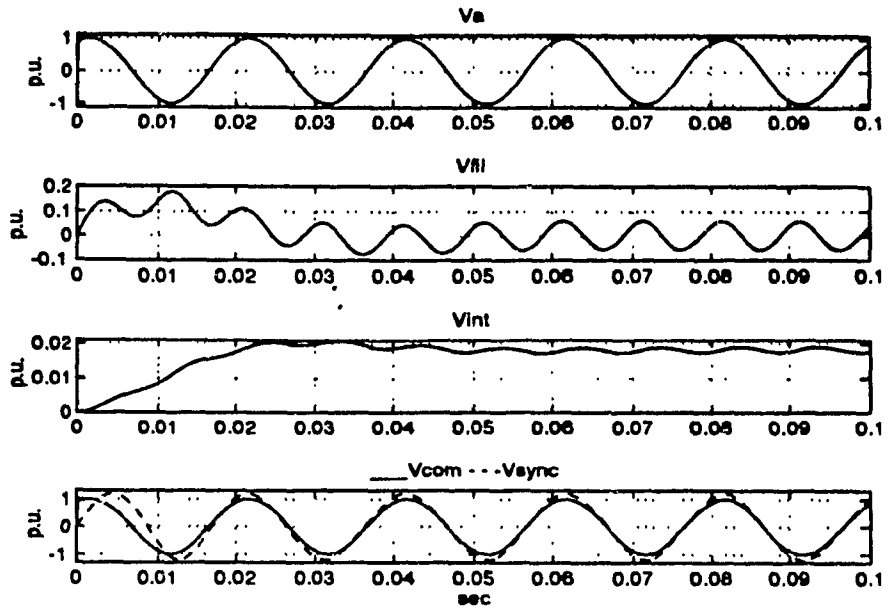


Figure 3.2: Waveforms of conventional GFU

3.2.1.1 Design of the Conventional GFU

The design criterion is to achieve the synchronization between Vcom and Vsync in the shortest possible time. One common design approach is to study the small signal model of the circuit and design the parameters in the frequency domain. The small signal model of a conventional gate firing unit is shown in Figure 3.3. The loop transfer function is given by equation 3.2 [16].

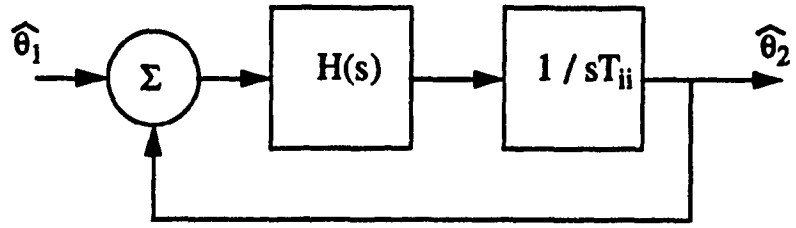


Figure 3.3: Small signal model for the conventional GFU

$$T_{12} = \left(\frac{\omega_c}{s+\omega_c}\right)\left(\frac{1}{sT_{ii}}\right) \qquad (3.2)$$

Figure 3.4 shows the Bode plot of the loop transfer function where the solid line represents the response of the loop transfer function T_{12}, dotted lines are for the low-pass filter function H(s) and the integrator transfer function $1/sT_{ii}$. This figure shows that in order to achieve the optimum phase margin of around 60^0, the integrator time constant should be selected such that the value of 1/Tii is smaller than ω_c, the cutoff frequency of the low-pass filter.

Figure 3.4 also shows that the loop response speed, represented by the gain cross-over frequency, is to a large extent limited by the cut-off frequency ω_c of the low-pass filter. There is a compromise in selecting ω_c. If ω_c is too high, the ac component in the error remains large and it will interfere with the system operation. On the other hand, if ω_c is too low, the overall system response of the system will be sluggish. Studies show that a cut-off frequency around one fifth of the ac component ($2\omega_c$) gives satisfactory results.

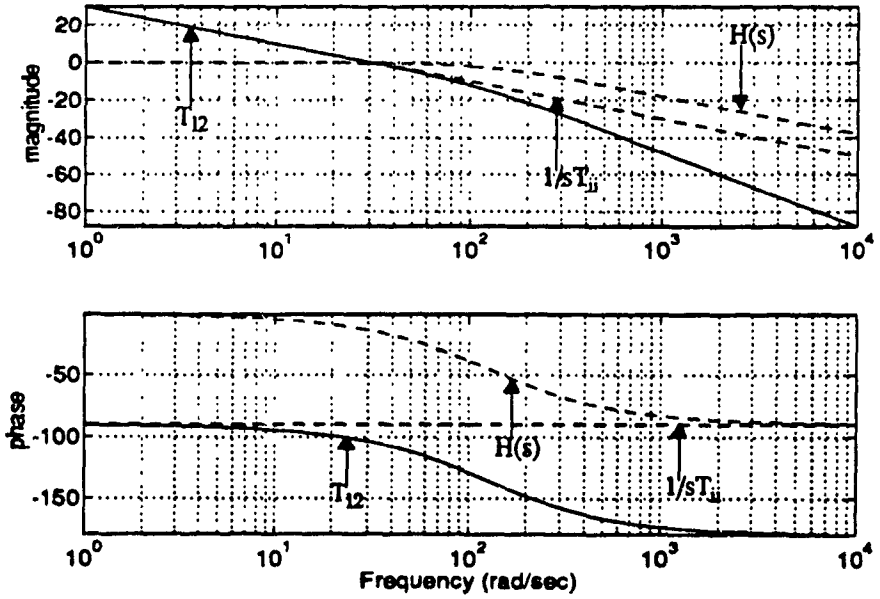


Figure 3.4: Bode plot for the loop transfer function of equation 3.2

3.2.1.2 Validation Tests for the Conventional GFU

In this section, behavior of the conventional GFU during (1) loss of commutation voltage and (2) presence of harmonics in the commutation voltage is discussed.

1) Loss of the Commutation Voltage

Figure 3.5 shows the internal signals from the conventional GFU during a temporary loss of commutation voltage caused by a fault on the ac commutation bus. The multiplier output Verror and the low-pass filter output Vfil are reduced to zero during the fault period. The Integrator output Vint shows only a small output voltage during the fault period which is used to modulate the frequency and phase of the Sine-Cosine oscillator stage following it. The post-fault synchronization dynamics of the conventional GFU show that the output voltage Vsync is able to synchronize with the commutation voltage Vcom within 1 cycle (20 ms at 50 Hz). The waveform of Vint also shows that the control loop is slightly underdamped and requires a settling time of about 3 cycles (50 ms).

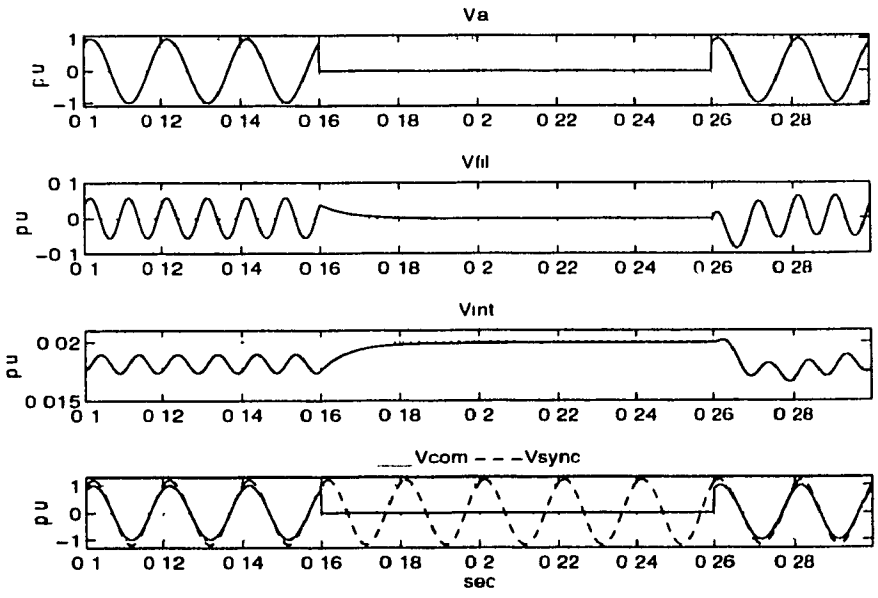


Figure 3.5: Loss of the commutation voltage

2) Harmonic Distortion Test

Figure 3.6 shows the internal signals from the conventional GFU for a 30% injection of a 3rd harmonic in the commutation bus, Vcom. The output voltage, Vsync, of the con-

ventional GFU contains no harmonics and is synchronized to the fundamental component of the commutation voltage. Tests with injections of other harmonics produced similar results.

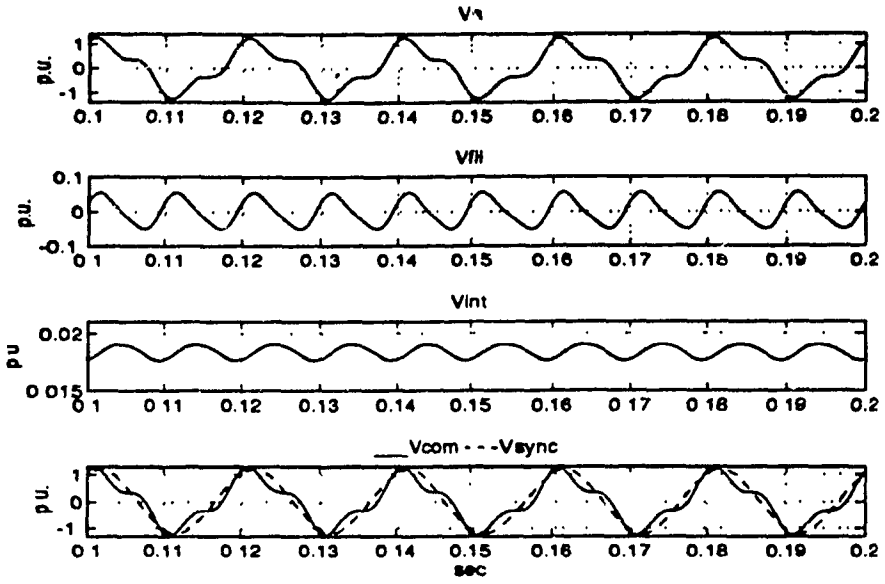


Figure 3.6: Harmonic distortion test for conventional GFU

3.2.2 DQ-type GFU

The block diagram of a DQ-type GFU and its corresponding signals are shown in Figures 3.7 and 3.8 respectively [17]. The three phase commutation voltages V_a, V_b and V_c are transformed into the DQ axis voltages V-alpha and V-beta using (3.3) and (3.4) respectively.

$$V_{alpha} = (\frac{2}{3})V_a - (\frac{1}{3})V_b - (\frac{1}{3})V_c \qquad (3.3)$$

$$V_{beta} = (\frac{1}{\sqrt{3}})(V_b - V_c) \qquad (3.4)$$

$$Error = (-V_{alpha} V \sin\theta + V_{beta} V \cos\theta) \qquad (3.5)$$

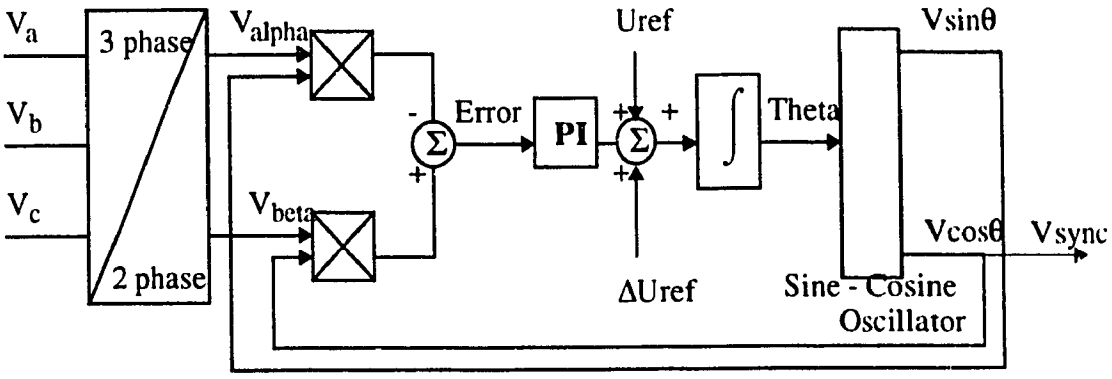


Figure 3.7: Block diagram of a DQ-type GFU

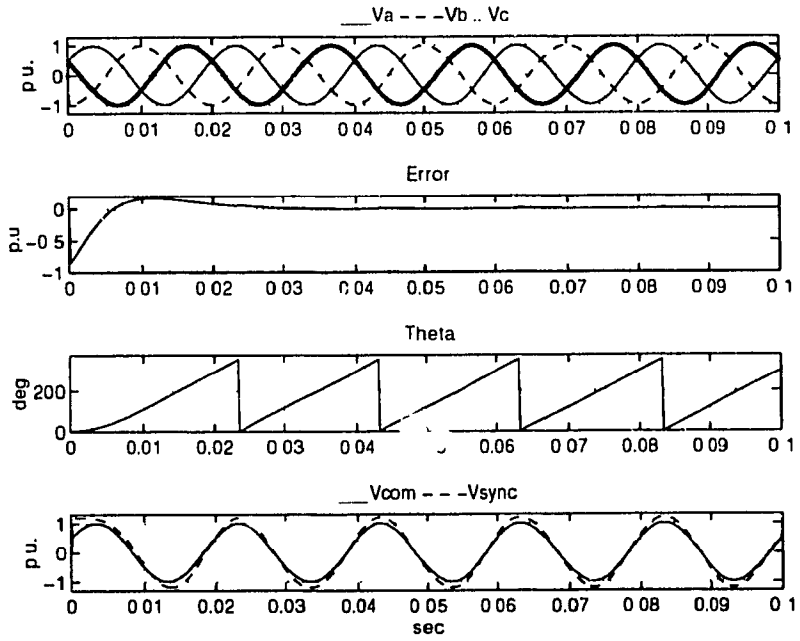


Figure 3.8: Waveforms for DQ-type GFU

An error signal, Error, is fed through a PI controller to generate a reference value for the VCO. This reference valve can be modulated by a signal ΔUref, and it has a fixed voltage bias Uref which sets the centre frequency (50Hz) of the VCO. The output of the VCO is a signal proportional to a sawtooth waveform (angle Theta). This waveform is used to

generate Sine-Cosine waveforms which are fed back to the multipliers to generate the error signal.

Under steady state this error is reduced to zero and the output of the Sine-Cosine oscillator will be in synchronism with the commutation voltages. In Figure 3.8, the output Vsync and Vcom are compared; note that the magnitude of Vsync has been deliberately increased by 20% to better illustrate the phasor relationship between the two signals. The loop transfer function of the DQ-type GFU is given by:

$$T_{l1}(s) = K_{pi}\left(\frac{1+sT_{pi}}{sT_{pi}}\right)\left(\frac{1}{sT_i}\right) \qquad (3.6)$$

where Kpi and Tpi are the gain and the time constant of the PI controller respectively.

3.2.2.1 Design of the DQ-type GFU

Similar to the conventional GFU, the design objective here is to achieve synchronization between Vsync and Vcom in the shortest possible time. The design approach is the same as the one used for designing a conventional GFU. The small signal block diagram of the DQ-type GFU is shown in Figure 3.9, where $G(s) = K_{pi}\left(\frac{1+sT_{pi}}{sTpi}\right)$ represents the PI controller transfer function.

The Bode plot of T_{l1} is shown in Figure 3.10. The solid lines are for the loop transfer function Tl1 and the dotted lines are for the PI controller and the integrator transfer function. From Figure 3.10, it can be concluded that, in order to achieve the optimum phase margin of around 60°, the value of 1/Ti' = Kpi/Ti should be larger than 1/Tpi. Also, since

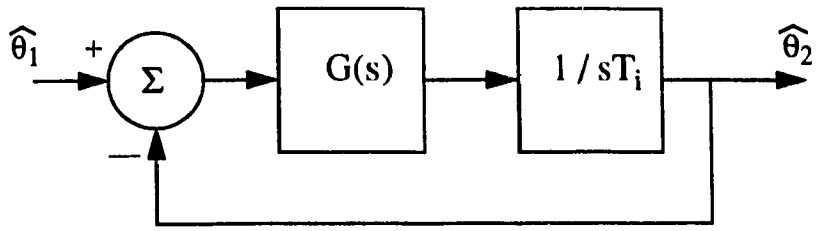


Figure 3.9: Small signal model for DQ-type GFU

the phase lag approaches 90^0 as the frequency increases, theoretically the gain cross-over frequency can be chosen as high as one wishes. Practically, this frequency will be limited in a realistic system. One of the limiting factors is the existence of a low-order harmonic component in the error signal when the 3-phase ac source contains harmonics. For example, with a third harmonic injection at the ac bus, the error signal contains a second harmonic ac component. Under such operating conditions, as the gain-cross-over frequency increases, the error signal between the synchronizing voltage (Vsync) and the fundamental component of the commutation voltage (Vcom) increases as well. Studies show that the-gain-cross over frequency of around 40 Hz provides a good compromise between a fast response and a small synchronizing error.

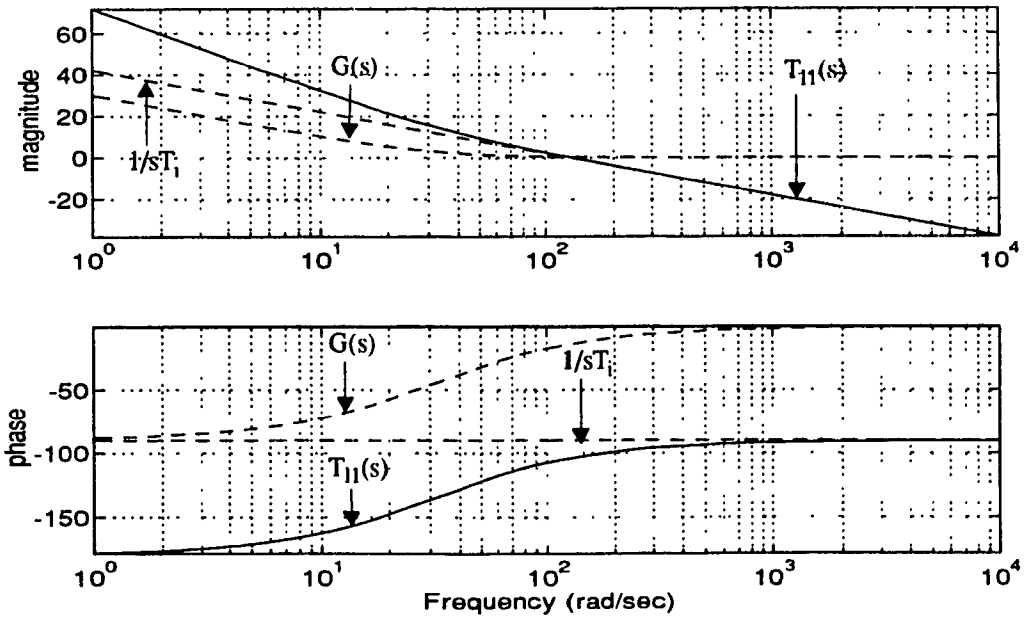


Figure 3.10: Bode plot for the loop transfer function of equation 3.6

3.2.2.2 Validation Test for the DQ-type GFU

In this section, behavior of the DQ-type GFU during (1) loss of commutation voltage and (2) presence of harmonics in the commutation voltage is discussed.

1) Loss of the Commutation Voltage:

Figure 3.11 shows the internal signals from the DQ-type gate firing unit during a temporary loss of commutation voltage caused by a 3-phase fault on the ac commutation bus. During the fault, the three phase commutation voltages Va, Vb and Vc are reduced to zero causing the Error input to PI controller to drop to zero. This results in the output of the saw-tooth waveform, Theta, to be at centre the frequency (50 Hz) of the VCO. After the fault, the error is reduced to zero within 1 cycle (20 ms at 50 Hz)

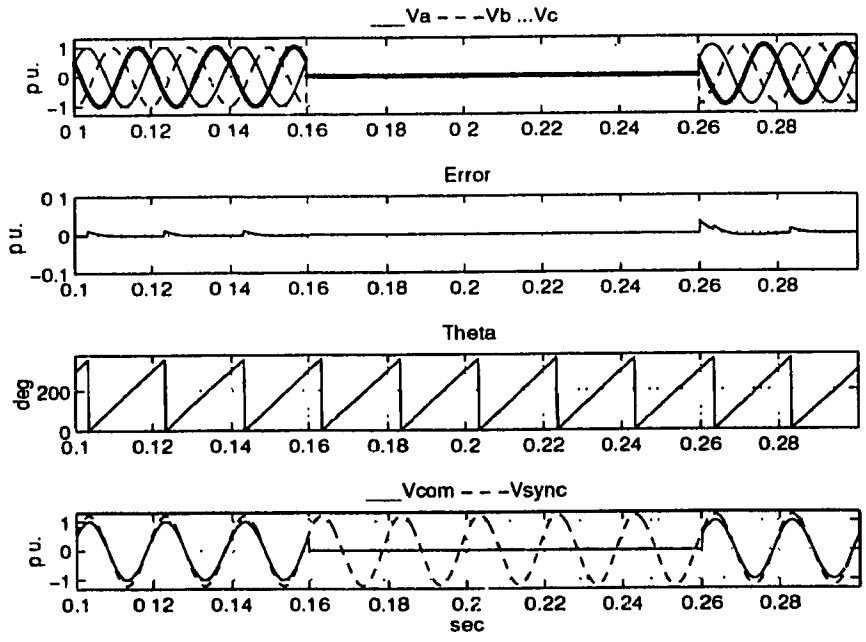


Figure 3.11: Loss of the commutation voltage

2) Harmonic Distortion Test

Figure 3.12 shows the internal signals for the DQ-type gate firing unit with a 30% third harmonic voltage on the commutation voltage. The Vsync output voltage of the DQ-type GFU contains no harmonics and is synchronized to the fundamental component of the commutation voltage.

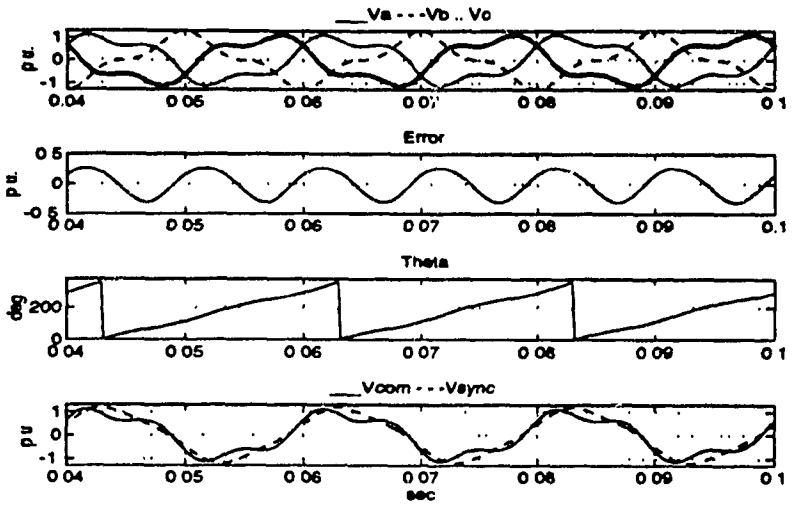


Figure 3.12: Harmonic distortion test for DQ-type GFU

3.2.3 Comparison Between the Conventional and DQ-type GFU's

The validation tests of gate firing units were open loop tests only. To assess the closed-loop performance of the GFUs when applied to a realistic system, gating pulses are derived using both GFU's, for a CIGRE benchmark HVDC rectifier system operating with a weak ac systems. The HVDC rectifier system is tested under ac-dc fault conditions and a comparison between the GFUs is made based on the results obtained here and the validation tests presented earlier.

3.2.3.1 Test System for Comparison

An HVDC rectifier system (Figure 3.13) based on the CIGRE Benchmark system [12] is used as a test system. Since a 6-pulse version of the converter is modelled, it is necessary to add 5th and 7th harmonic ac filters. The overall size of the filters is the same as that of the CIGRE converter system and will be presented later. A 6-pulse converter model is used here to minimize the simulation time. However, the same design principles and the operational characteristics for the GFUs can be extended to a 12-pulse unit.

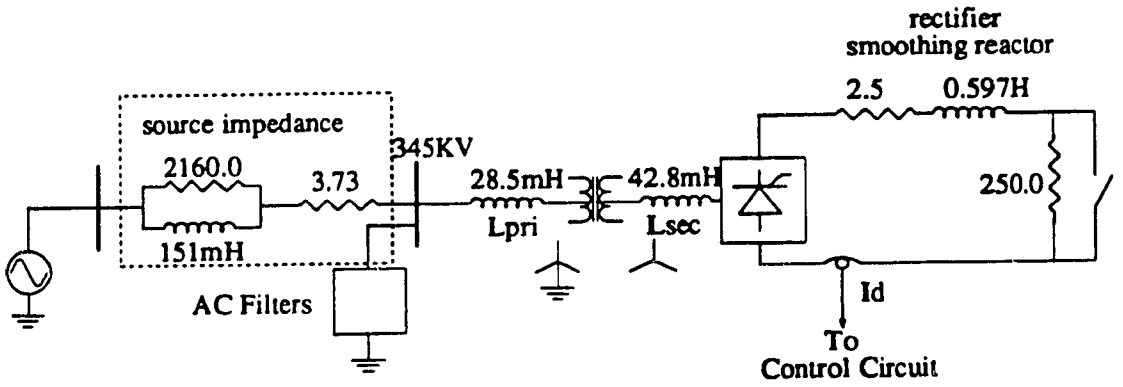


Figure 3.13: CIGRE benchmark based HVDC rectifier system

The block diagram of the current controller used with this system is showed in Figure 3.14. The measured dc current I_d is compared to a current order Iref, and a current error signal is generated. This current error is fed to a block, other input of which is a delayed step input FORAND. The delayed step input keeps the input to the PI controller zero for 0.02s; this effect contributes in reducing the initialization time of the simulation. The output of PI controller is limited between $\alpha_{min} = 5^o$ and $\alpha_{max} = 170^o$. Alpha-order, output of the PI controller is fed to a gating unit which uses the synchronized voltage Vsync to generate a firing pulse train. A ring counter is used to separate the firing pulses for the 6 valves of the rectifier.

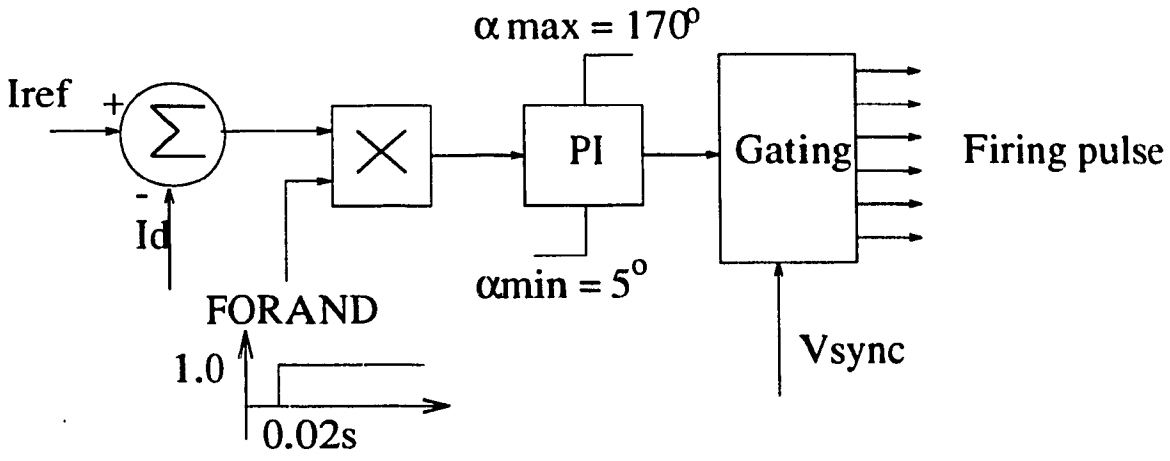


Figure 3.14: Block diagram of current controller

1) Initialization of Rectifier System Model

Figures 3.15a and 3.15b show the initialization of the rectifier system with the DQ-type and conventional GFUs respectively. The signals shown are the dc current I_d, alpha order and the superimposed values of the synchronizing voltage (1.2* Vsync) and the commutation voltage Vcom. In both cases startup is achieved rapidly and the GFUs are able to synchronize within 1 cycle. A detailed examination shows that DQ-type unit is marginally faster.

2) 10% Step Change in the Current Reference

Figures 3.16a and 3.16b show the case of a 10% step change in the current reference for a DQ-type and conventional gate firing unit respectively. The signals shown are the dc current I_d, alpha order and the superimposed values of the synchronizing voltage (1.2* Vsync) and the commutation voltage Vcom. For the DQ-type GFU and the conventional type, the step change is effected in 30 ms, the response is stable and well controlled. The GFU's are able to synchronize in the pre-fault, during the fault, and the post fault stages.

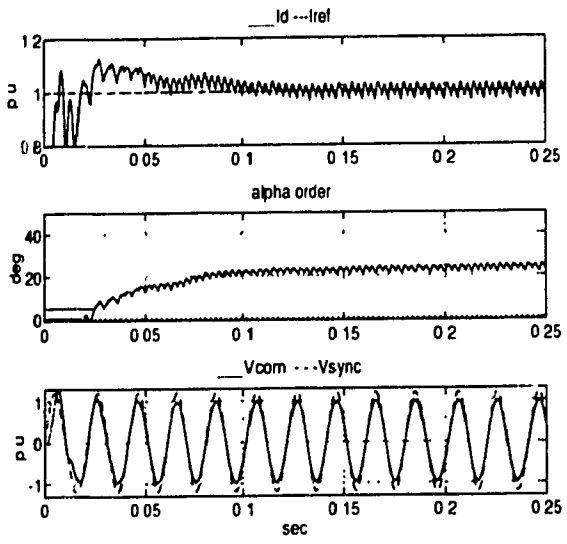


Figure 3.15a: Initialization with the conventional GFU

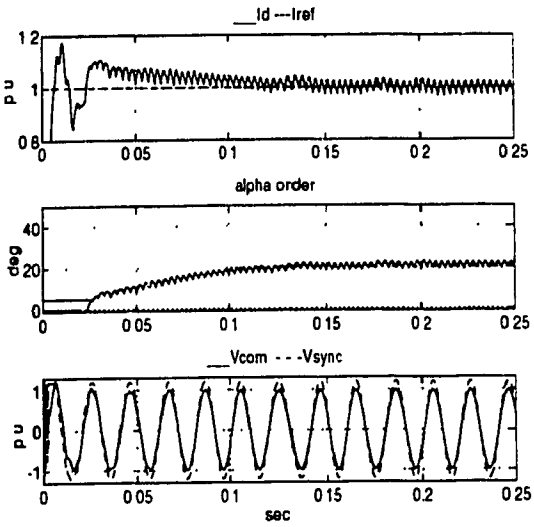


Figure 3.15b: Initialization with the DQ-type GFU

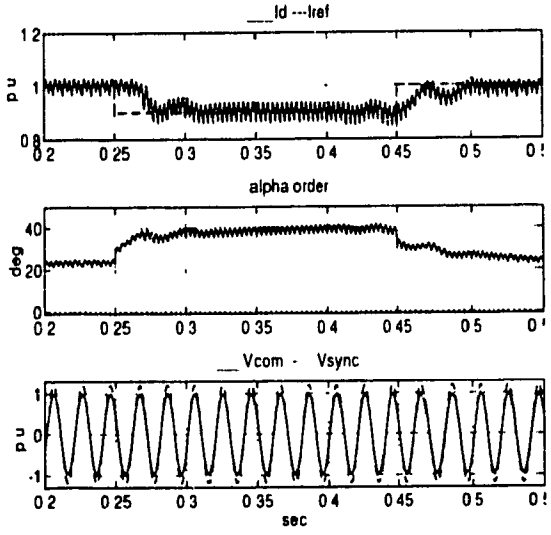


Figure 3.16a: 10% step change in the current reference with the conventional GFU

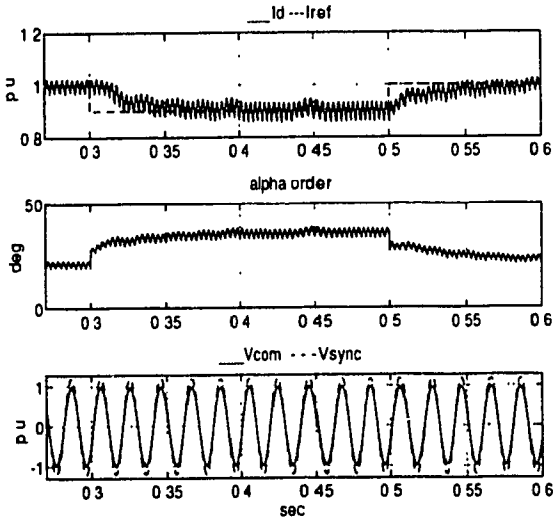


Figure 3.16b: 10% step change in the current reference with the DQ-type GFU

3) Single Phase Fault

Figures 3.17a and 3.17b show the case of a single phase fault for the rectifier system with the DQ-type and the conventional GFU. The signals shown are the dc current I_d, alpha order and the superimposed values of the synchronizing voltage (1.2* Vsync) and

the commutation voltage Vcom. For both cases a large second order component is seen in the dc current, a characteristic of the unbalanced fault in the system and the modulation effect of the converter. The presence of this second harmonic component does not affect the operation of the GFUs noticeably and they maintain synchronizm with the commutation voltage through out the fault period.

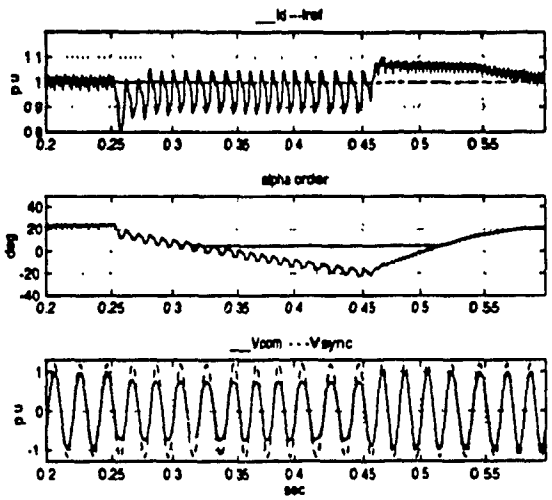


Figure 3.17a: Single phase fault with the conventional GFU

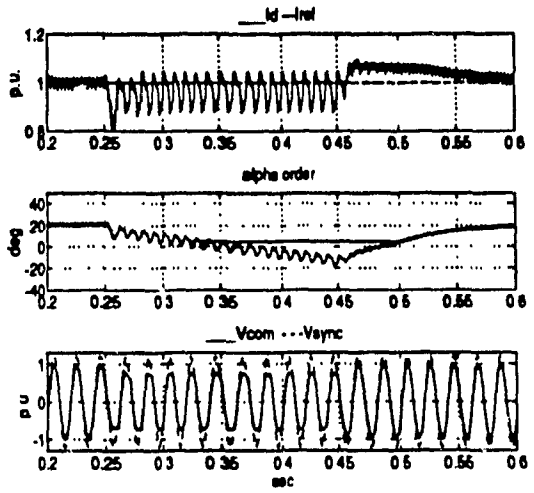


Figure 3.17a: Single phase fault with the DQ-type GFU

4) DC Line Fault

Figures 3.18a and 3.18b, show the case of a dc line fault for the rectifier system with a DQ-type and conventional gate firing units respectively. The signals shown are the dc current I_d, alpha order and the superimposed values of the synchronizing voltage (1.2 * Vsync) and the commutation voltage Vcom. Note that in these cases no voltage dependent current limits (VDCL) are utilised to reduce the current order since only the control response of the gate firing units is desired. In both cases the gate firing units are able to maintain synchronism within 1 - 2 cycles of the fault. The loss of the dc load causes the commutation voltage to rise and generate harmonics due to transformer saturation, but this does not cause persistent problems for the gate firing units. In case of weak ac systems,

this commutation voltage rise and the subsequent generation of harmonics is particularly important.

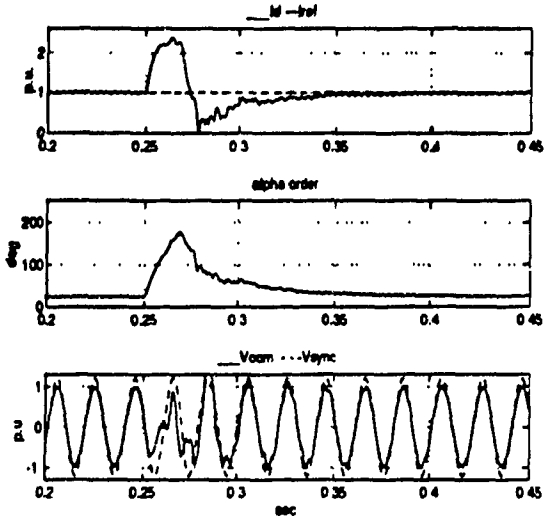


Figure 3.18a: DC line fault with the conventional GFU

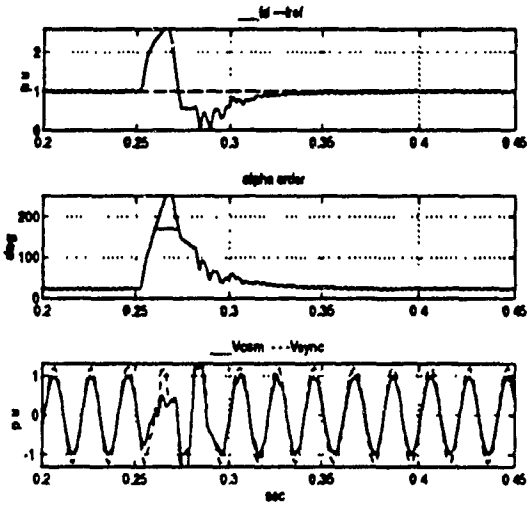


Figure 3.18b: DC line fault with the DQ-type GFU

3.2.3.2 Comparison

The major difference between the operational behavior of the DQ-type and the conventional GFU is the presence of a second harmonic component in the error signal under steady state for the conventional GFU. A low-pass filter is thus required in the conventional GFU to eliminate the second harmonic component. This low-pass filter is absent in the DQ-type GFU and hence a faster dynamic response can be achieved. Experience also shows that optimization of the low-pass filter requires additional effort when compared to the DQ-type GFU.

A performance comparison between the two GFUs show that both units are equally capable of operating with weak ac systems having high levels of pollution and harmonic distortion in the commutation voltage.

A DQ-type GFU is used for the remainder of this thesis to study the behaviour of the HVDC system.

3.3 Rectifier Controller

The rectifier controller includes the current controller and the Voltage Dependent Current Limit Circuit (VDCL).

3.3.1 Rectifier Current Controller

The objective of using a current controller on the rectifier is to maintain the current at a reference level decided by the VDCL. Similarly, a gamma controller is used to maintain certain dc voltage at the inverter end. The controller, which uses a PI controller, generates an alpha-order signal. This alpha order has to be utilized to change the firing angle of the converter valves and generates firing pulses that are in synchronism with the commutation bus. The gating control unit utilizes the alpha order signal and generates 6 pulses for the converter valves. The timing reference is provided by the GFU which generates a sinusoidal signal which is in synchronism with the commutation bus voltage.

The block diagram of the rectifier current controller is shown in Figure 3.19. The measured dc current, Idcr, is compared with the limited output, IOLIM, of the VDCL and an error signal is generated. This error signal is fed to the PI controller via a block, other input of which is a delayed step input FORAND. The delayed step input keeps the input to the PI controller zero for 0.1s; the effect of this delay is to reduce the initialization time. The PI controller generates an alpha-order signal which is limited between 1^{o} and 170^{o}. The output of the PI controller is used in conjunction with a protection signal ALPRET, for recovery from a dc line fault. The alpha order signal is fed to a gating unit which uses

the synchronized voltage Vsync to generate a firing pulse train. A ring counter is used to separate the firing pulses for the 6 valves of the rectifier.

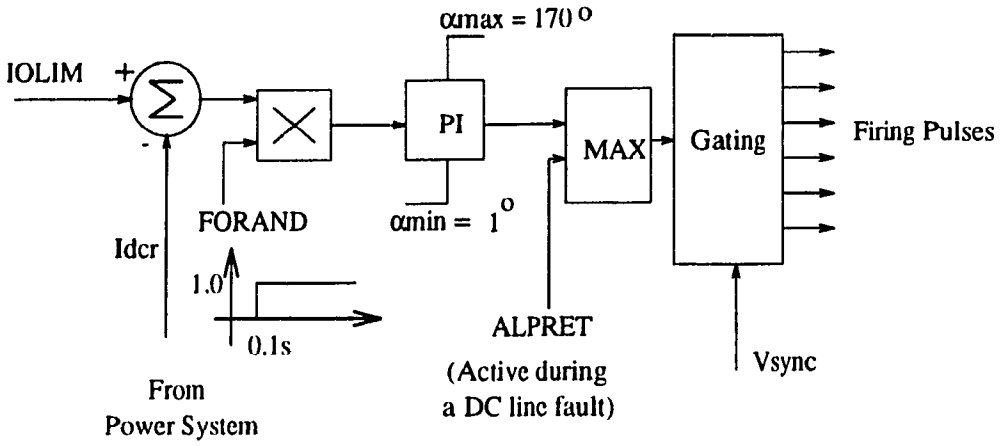


Figure 3.19: Rectifier current controller

3.3.2 Voltage Dependent Current Limit (VDCL) Unit

A dc line fault or an ac fault on the inverter end could dip the dc voltage to a value which could be zero or very low. The current under these conditions would be still maintained due to the rectifier current controller. The operation of the system with high dc current and low dc voltage could result in higher power losses and higher reactive power demand and could also lead to voltage instability. To avoid this problem, the current reference signal provided to the controllers should be a function of the dc voltage. A VDCL limits the current reference value for the rectifier controller based upon the level of the dc voltage.

The VDCL (Figure 3.20) consists of a static and dynamic sub-units which provide reference values during steady state and transient conditions respectively. The measured dc voltage is passed through a low-pass filter to eliminate higher order harmonics. The cut-off frequency (30 Hz) of the low-pass filter is chosen below the fundamental frequency to ensure the attenuation of high order harmonics being fed back from the dc voltage. The

combination of a low-pass filter and the pulse-shaping circuit removes spikes that may be present in the dc voltage. The output of the pulse shaping circuit is used by both the static and dynamic VDCL sub-units.

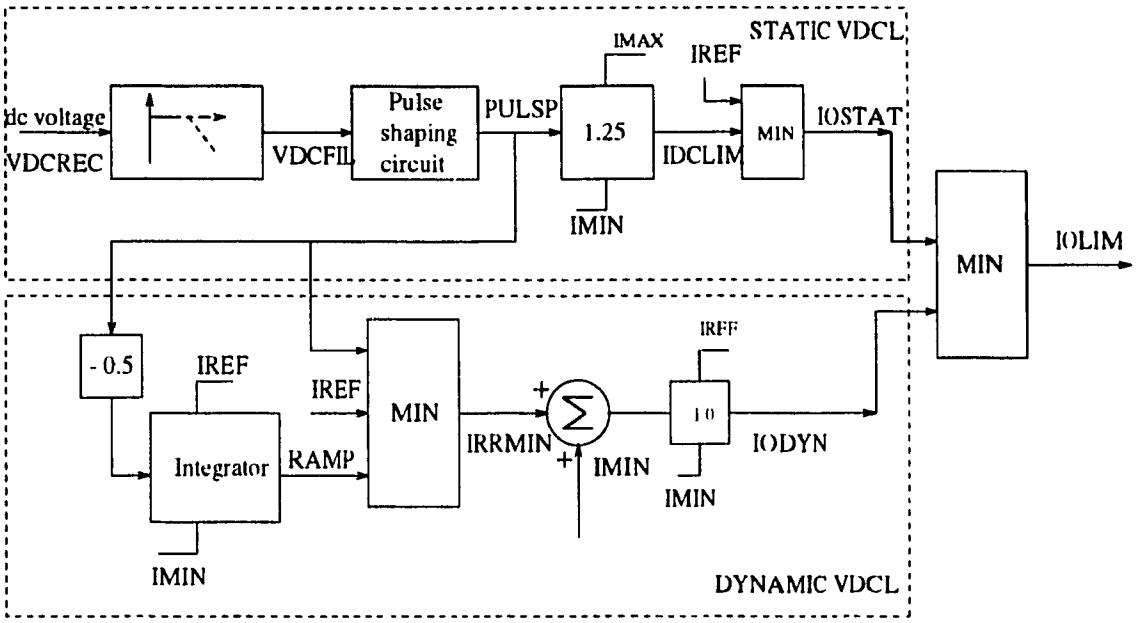


Figure 3.20: Block diagram of the VDCL unit

The static VDCL sub-unit consists of a voltage-to-current transducer with a gain of 1.25, the output of this block is limited between IMIN and IMAX. The output of the voltage-to-current transducer is fed to a MINIMUM-selector whose other input is the current reference, Iref. The output of the MINIMUM-selector is IOSTAT.

The dynamic VDCL sub-unit consists of an integrator (time constant 50 ms), which dictates the rise time of the dc current during the process of fault recovery. The output of the integrator is passed through a MINIMUM-selector which has the output of the pulse shaping circuit and Iref as its other inputs. The MINIMUM-selector ensures that in the worst case, the output of the follow ing blocks is IREF, which can be set externally. IMIN is added to the output of the MINIMUN- selector IRRMIN, through a summer. The output of the summer is then limited between IMIN and Iref. This is done to ensure that the out-

put of the dynamic VDCL sub-unit ramps up from IMIN to IREF during system start-up and also during recovery from faults such as a dc line fault.

To validate the operation of the VDCL the following simple test was done (Figure 3.21). The stepped VDCREC is the input to the unit as shown in Figure 3.3.21. During the recovery process, the output of the VDCL, IOLIM, is dictated by the dynamic VDCL. In contrast, during the normal operation the static VDCL sub-unit dictates the output.

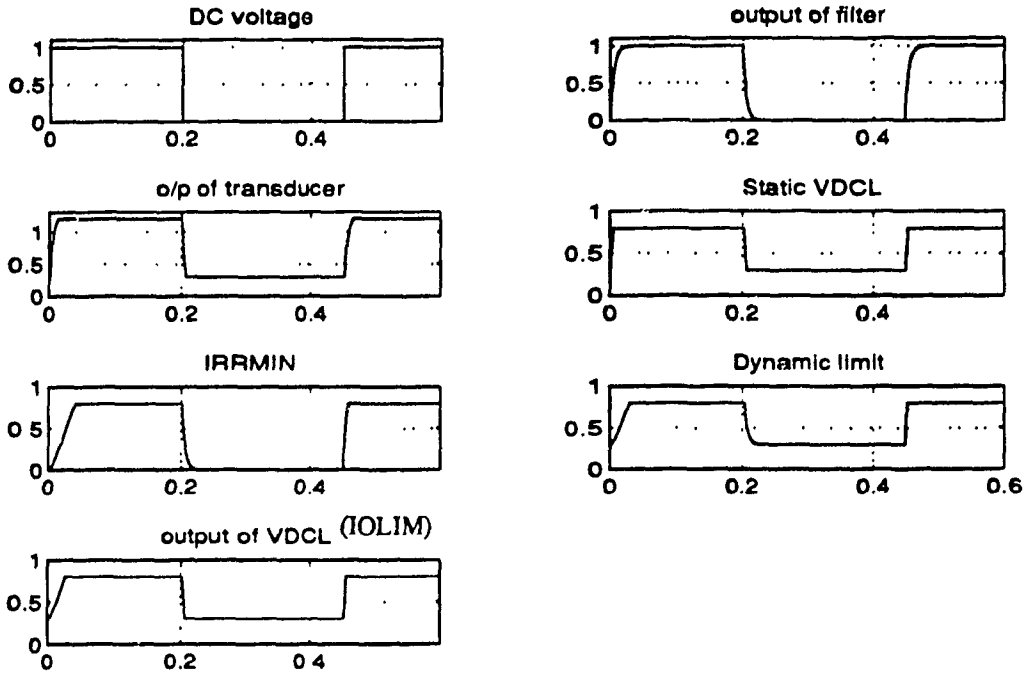


Figure 3.21: Validation test for VDCL

3.4 Inverter Control System

The inverter control circuit includes the curent controller and the gamma controller

3.4.1 Inverter Current Controller

The inverter current controller (Figure 3.22) is similar to the rectifier current controller.

The measured dc current is compared with IOLIM - 0.1, giving a current margin $\Delta I = 0.1$ p.u. The inverter PI controller generates an alpha-order signal A1 which is limited between 110^{o} and 150^{o}. The alpha order signal is then fed to a gating unit which uses the synchronized voltage Vsync to generate a firing pulse train. A ring counter is used to separate the firing pulses for 6 valves of the inverter.

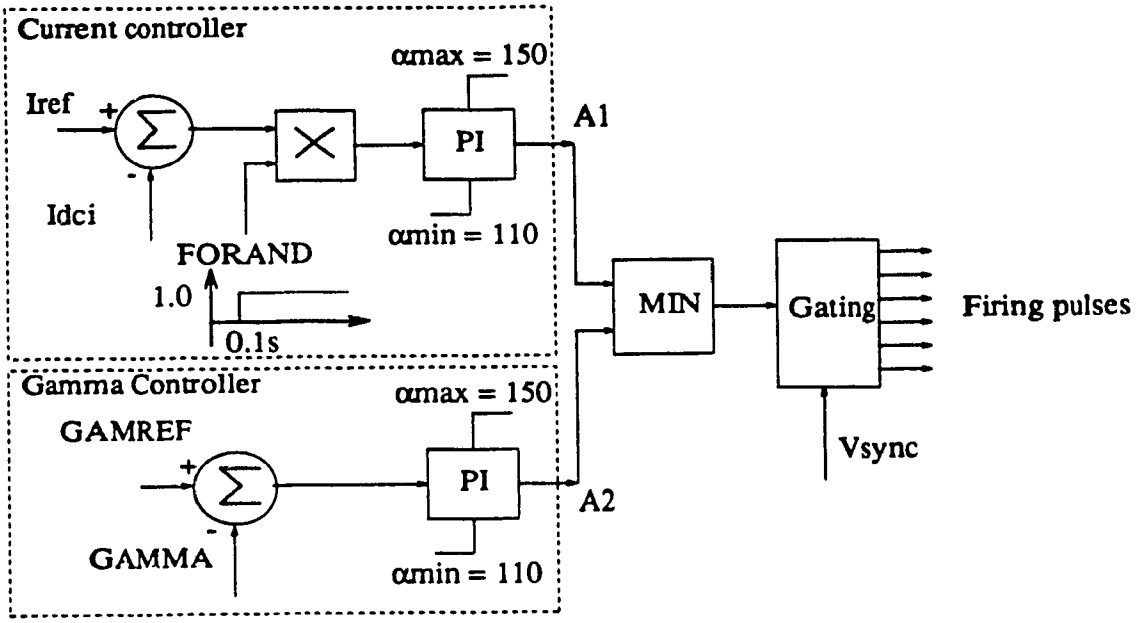


Figure 3.22: Inverter control system

3.4.2 Gamma Controller

To implement a gamma controller, a measure of the gamma is required (Figure 3.23) A typical voltage across an inverter valve is shown in Figure 3.23. The gamma measuring circuit is based on evaluating the time elapsed between the two zero-crossings a and b of the valve voltage.

The valve voltage provides the region a-b-c as a positive value. This voltage is used as a control voltage for a resettable integrator which integrates only when the control voltage

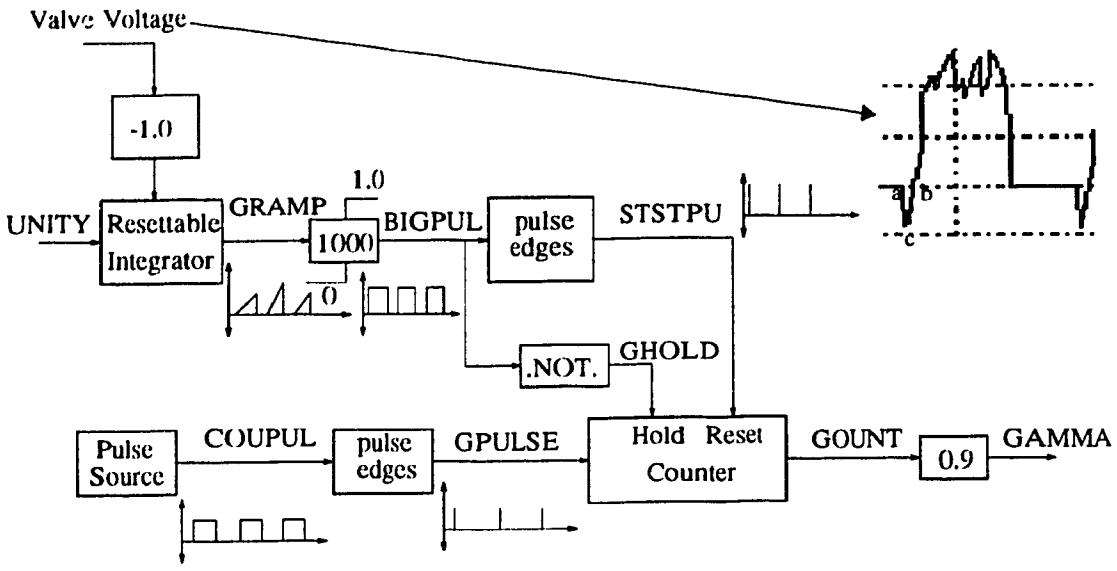


Figure 3.23: Gamma measuring circuit

is positive. The output of the resettable integrator is a ramp, the width of which is a function of the valve voltage. From this ramp voltage, rectangular pulses, BIGPUL, are obtained by using a zero-order block. A sharp pulse having a duration of one time step is derived at the rising edge of BIGPUL, these sharp pulses are used to reset the counter at the start of BIG PUL. When the duration of BIGPUL is over, another rectangular pulse, GHOLD, which is a complement of BIGPUL is used to hold the count of the counter. The pulse source for the counter has a pulse width of 25μs and a period of 50μs. So each count represents 0.9^{0}, hence to get the final output in degrees, a factor of 0.9^{0} is used. An average value of gamma using all six valves volt ages is obtained by using a low-pass filter.

To validate the operation of the gamma measuring circuit, a simple test is conducted. Gamma is set to 20^{0}, some key internal signals of the gamma measuring circuit for this test are shown in Figure 3.24. In Figure 3.24, the value of gamma is equal to the preset value of gamma, hence confirming the operation of the gamma measuring circuit.

The gamma controller is similar to the current controller except for the FORAND signal which is absent in the gamma controller. The measured value of gamma (output of the

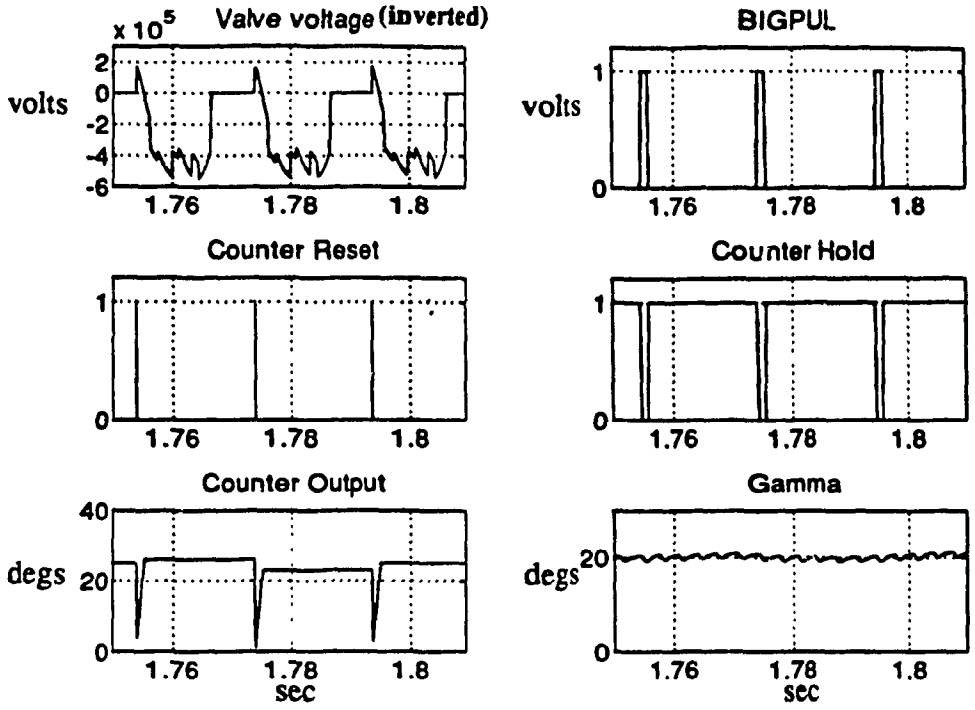


Figure 3.24: Validation of gamma measuring circuit

gamma measuring circuit) is compared with a reference value GAMREF. The error signal is fed to the PI controller which generates an alpha order signal A2, which is limited between 110^{o} to 150^{o}. A min selector is used to select the minimum of A1 and A2. The output of this min selector is used as an input by the gating unit which uses the synchronized voltage Vsync to generate a firing pulse train. A ring counter is used to separate the firing pulses for 6 valves of the inverter

3.5 Design of PI Controller Parameters

To design the parameters of the PI controller, the converter is represented by the following equation [18]

$$T_c = \frac{K}{(s + T_d)} \qquad (3.7)$$

where K = 1.35 VL-L, Td = the time delay = 120^0. The transfer function of the dc line can be represented by the following equation

$$T_{lc} = \frac{Z_3}{(Z_2 + Z_3) Z_1 + Z_2 Z_3} \qquad (3.8)$$

In the system, if we ignore the effect of the impedance of the ac sides, we get identical models for the rectifier and inverter. The Bode plot of the converter and the dc line is shown in Figure 3.25. The parameters are chosen such that an overall phase margin of about 60^0 is obtained. After some optimization tests, the following approximate PI controller parameters are obtained:

For the rectifier current controller, the phase margin is 43.66^0 and the gain cross-over frequency is 72.65 rads (Figure 3.25). For the inverter current controller, the phase margin is 37.56^0 and the gain cross-over frequency is 65.97 rads (Figure 3.26).

The gamma controller is designed using the same procedure described above.

These parameters are only approximate, but useful as starting values for the simulation. Optimized values for the controller parameters can then be obtained from detailed simulations.

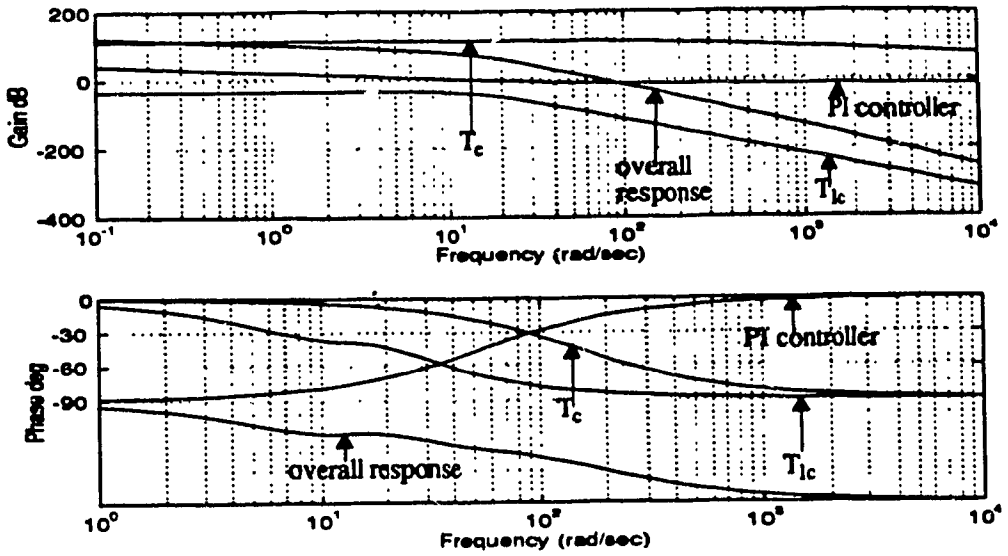


Figure 3.25: Bode plot of the rectifier control system

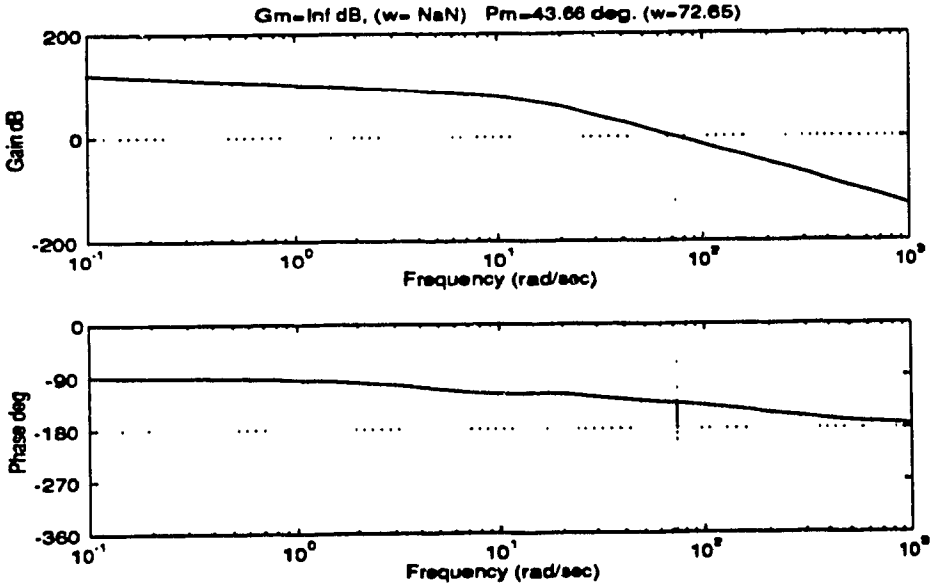


Figure 3.26: Gain margin and phase margin of the rectifier current controller

3.6 Summary

Control aspects of a CIGRE benchmark based HVDC converter system operating with weak ac systems were presented. Two GFUs are described and comparison is made between the two. The rectifier and the inverter control systems are presented. A design procedure for designing the parameters of the PI controller is outlined.

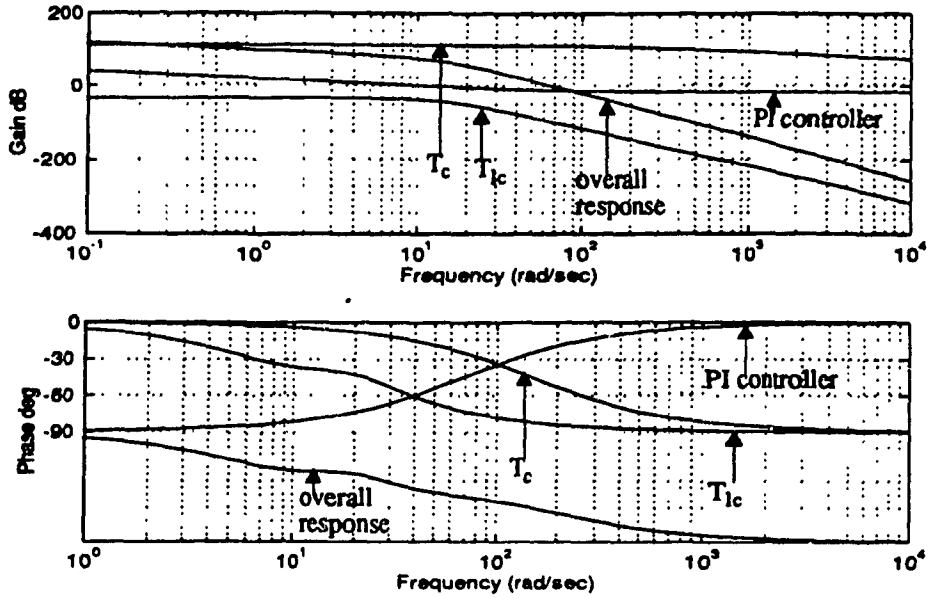


Figure 3.27: Bode plot of the inverter control system

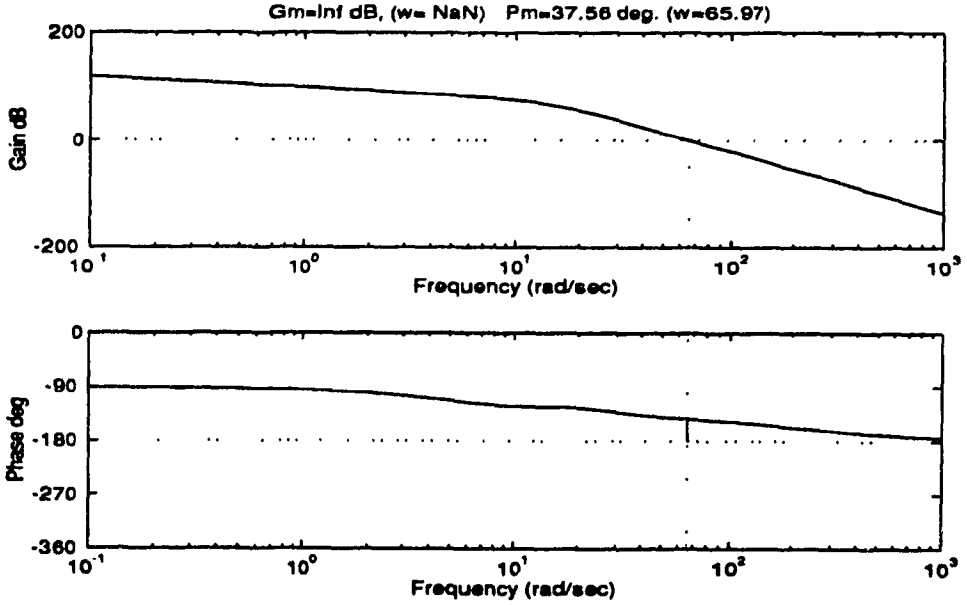


Figure 3.28: Gain and phase margin of the inverter control system

Chapter 4
Transient Behavior of the HVDC System

4.1 Introduction

The transient performance of an HVDC converter system operating with a weak ac system depends to a great extent on the control system utilized, besides other things. The details regarding the control system were presented in Chapter 3. To validate the operation of the current and gamma controllers, and protection circuits (i.e. VDCL), the HVDC converter system is tested under various ac-dc fault conditions. The results of these tests are presented in this chapter.

4.2 Initialization of the HVDC System

Care has to be taken to initialize the simulation to achieve the steady state operating point in a realistically short time. To do this, the firing pulses are blocked for a period of 0.1s, where-by releasing the controllers (in TACS portion of EMTP) to find their operating points. The blocking of the firing pulses is achieved by using a signal FORAND (Figure 3.19). The initialization process and system dynamics are shown in Figure 4.1. Right at the start, there is a commutation failure as seen from the ac voltage waveforms at both the rectifier and inverter sides. As a result of this, the dc voltage is equal to zero. The output of the gamma controller reaches a value of alpha-max (inverter) facilitating a gradual build up of the dc voltage. On the V_d-I_d control characteristics (Figure 4.2), the operating point follows line KA until it reaches the inverter current controller characteristic. A switch-over occurs at 0.9s as current control is taken over by the rectifier current controller. An overshoot is seen after the switch-over due to the transition from the inverter current controller to the rectifier current controller. When steady state is reached at 1.1s, the

dc current is controlled by the rectifier current controller and the voltage is controlled by the inverter gamma controller.

4.3 System Tests

To validate the operation of the control scheme for the CIGRE Benchmark HVDC system, the following tests were performed:

4.3.1 Controller Optimization Tests

Three controllers are in operation for the HVDC system:

1) Rectifier current controller

2) Inverter current controller

3) Gamma controller

All these controllers nned to be optimized individually. For optimization of these controller parameters, the following three tests were performed:

i) step change in the rectifier current reference

ii) step change in the inverter current reference

iii) step change in the inverter gamma reference

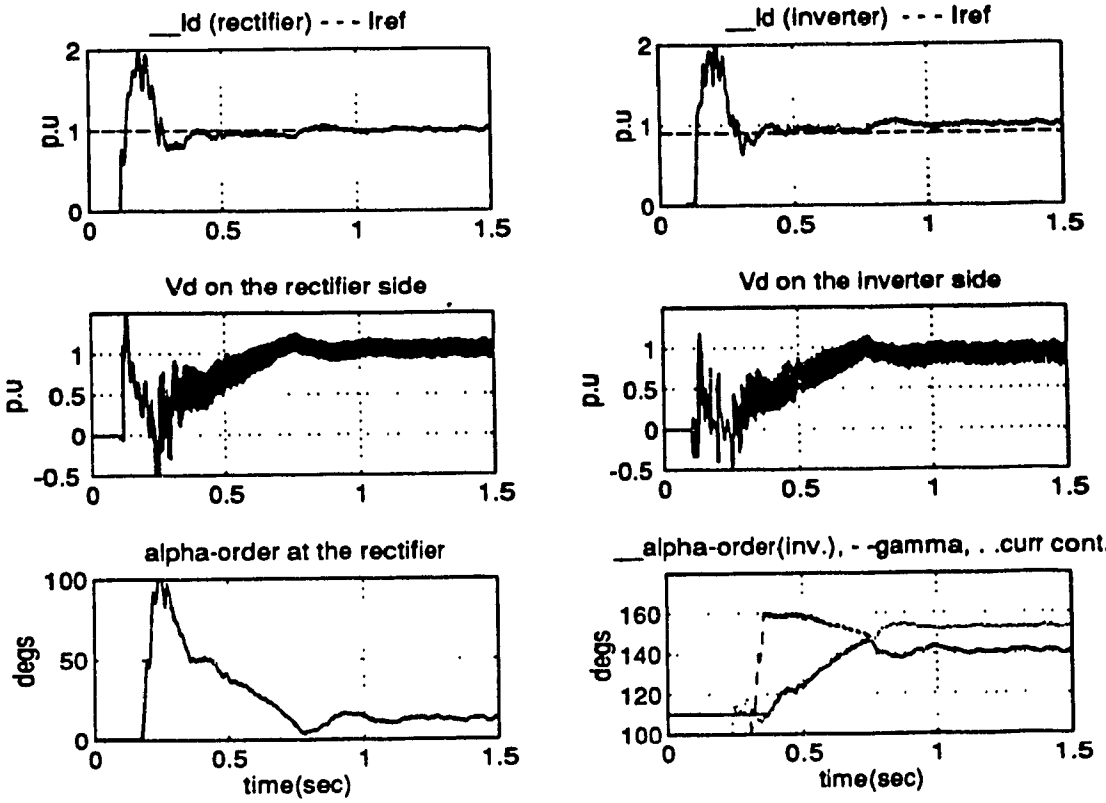


Figure 4.1a: Initialization of the HVDC converter system model

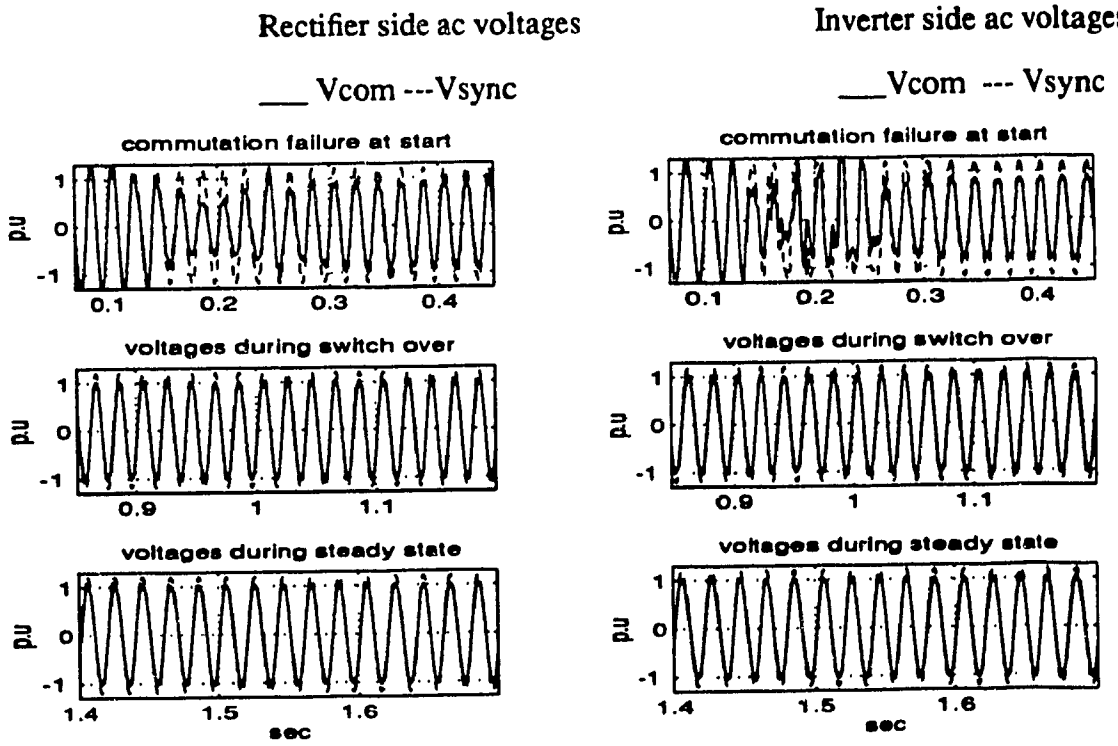


Figure 4.1b: The ac voltages for the initialization case

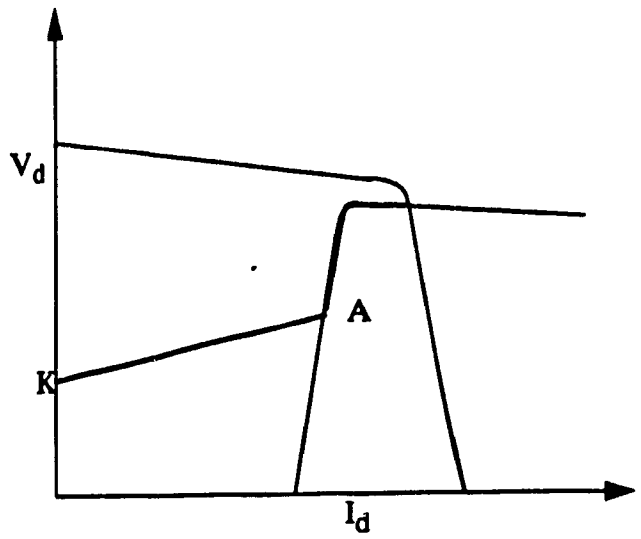


Figure 4.2: V_d - I_d control characteristics

4.3.1.1. 10% Step Change in the Rectifier Current Reference

To test the performance of the current controller at the rectifier end, a 10% step change is applied to its current reference (Figure 4.3). To effectively study the performance of the rectifier current controller and prevent any interference from the inverter current controller, the current margin ΔI is temporarily set to 20%. The step change is applied at 1.3s and the step change is effected in 100ms. The response is well controlled and stable. The results shows the dc current on the rectifier and the inverter sides along with their reference values. The dc voltages on the rectifier and the inverter sides are also shown. The rectifier alpha-order signal also shows the step change being effected. The inverter alpha-order signal shows that the inverter current controller plays no role in controlling the current. The gamma controller controls the inverter voltage.

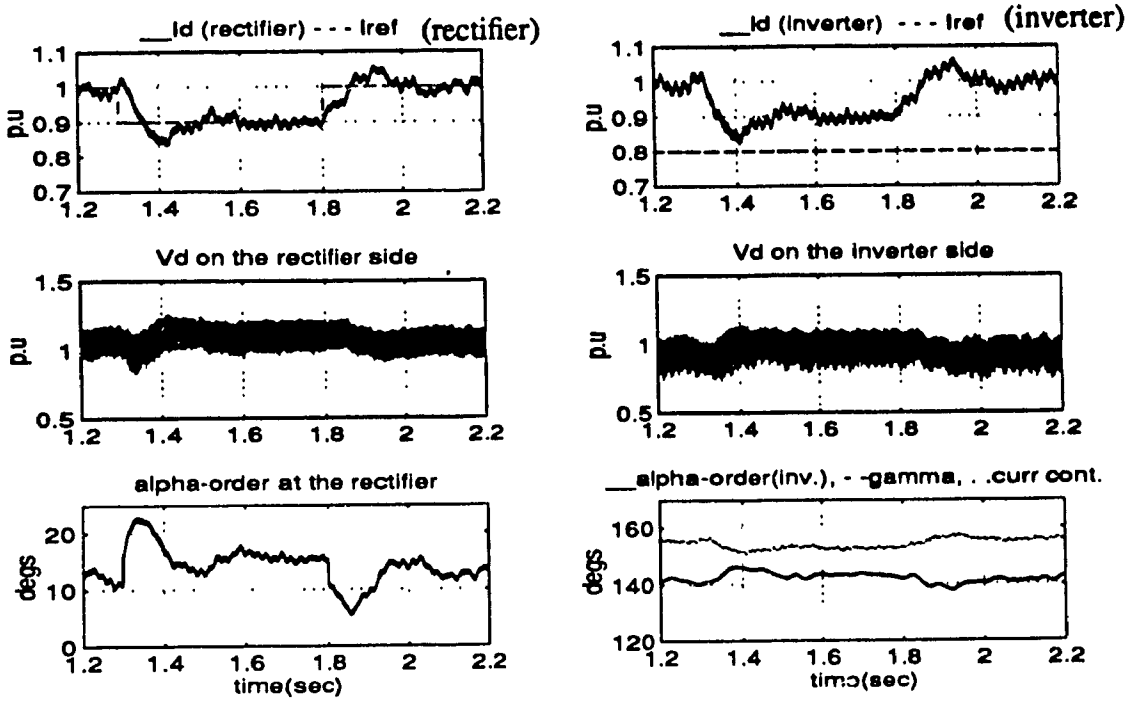


Figure 4.3a: 10% Step change in the rectifier current reference

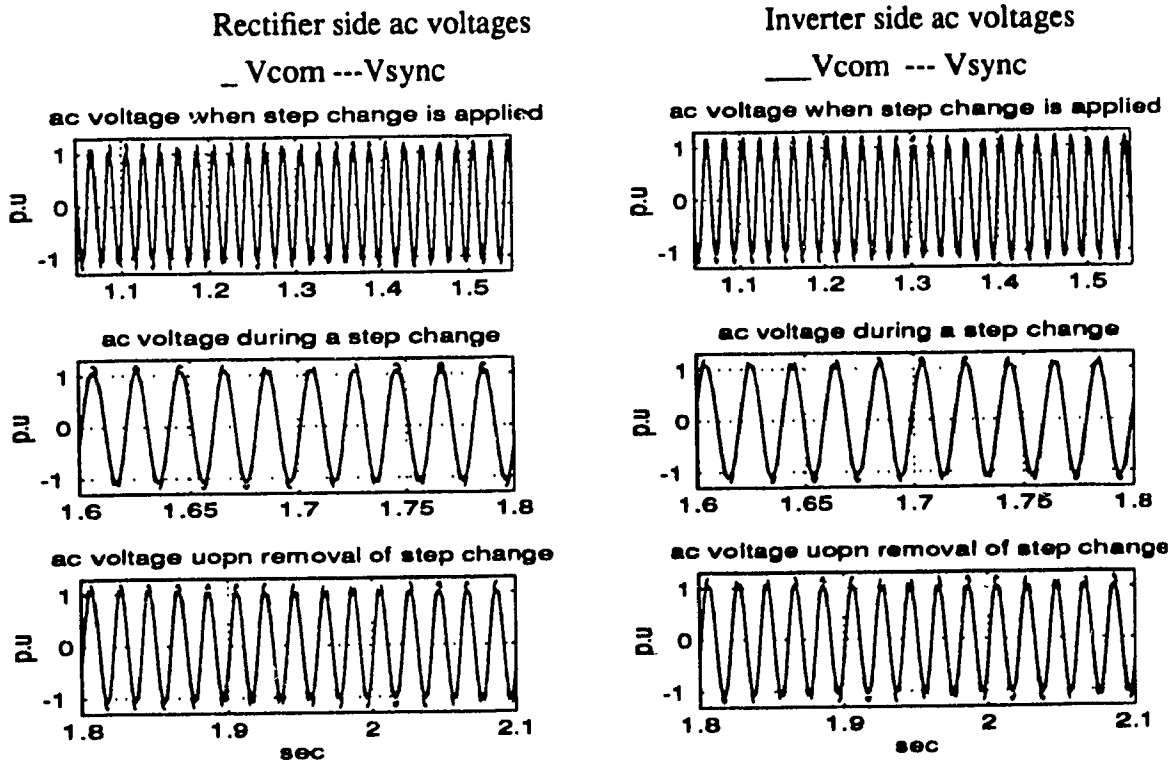


Figure 4.3b: The ac voltages for 10% step change in the rectifier current reference

4.3.1.2. 5% Step Change in the Inverter Current Reference

To test the performance of the inverter current controller, a 5% step change is applied to its current reference (Figure 4.4). To effectively study only the performance of the inverter current controller and prevent any interference from the rectifier current controller, the ac supply voltage at the rectifier end is reduced by 5% to force the rectifier current controller to its alpha-min limit. The response to the step change is stable and well controlled and is effected in 80ms. The results show the dc current at the rectifier and the inverter side along with their reference values. The dc voltages on the rectifier and the inverter sides are also shown. The rectifier alpha-order signal is at alpha-min so the inverter current controller controls the dc current of the system at a value of 0.9 p.u..

4.3.1.3. 2.5^{o} Step Change in Gamma Reference .

To test the performance of the inverter gamma controller, a 2.5 degs. step change is applied in the gamma reference (Figure 4.5). The response is well controlled and stable with a response time of 50ms. The dc voltages on the rectifier and inverter side dip due to the step gamma reduction. The alpha order signal at the rectifier end thus increases as seen in Figure 4.5

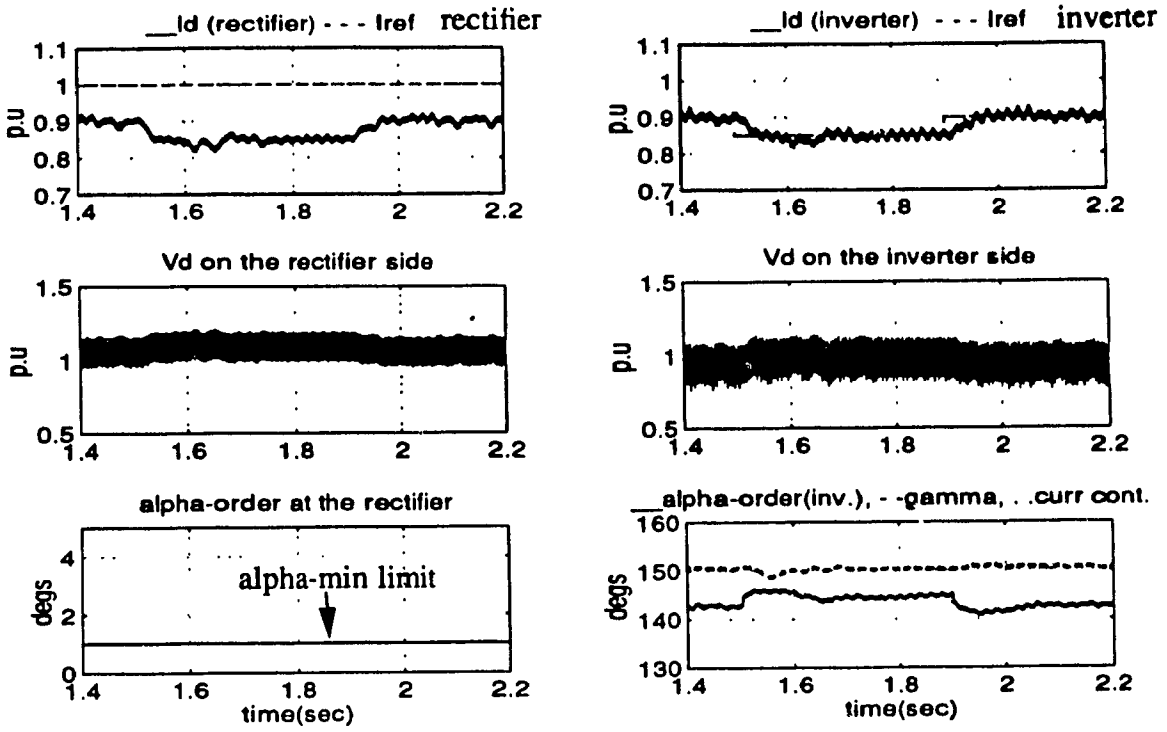


Figure 4.4a: 5% step change in the inverter curent reference

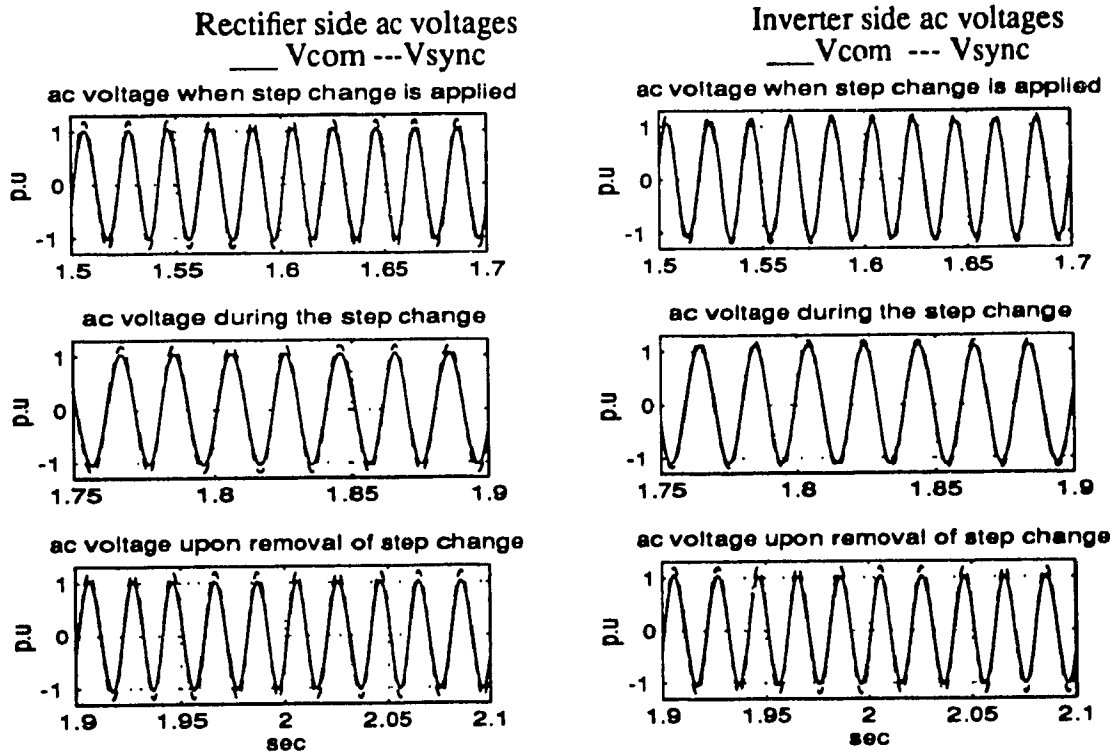


Figure 4.4b: The ac voltages for 5% step change in the inverter curent reference

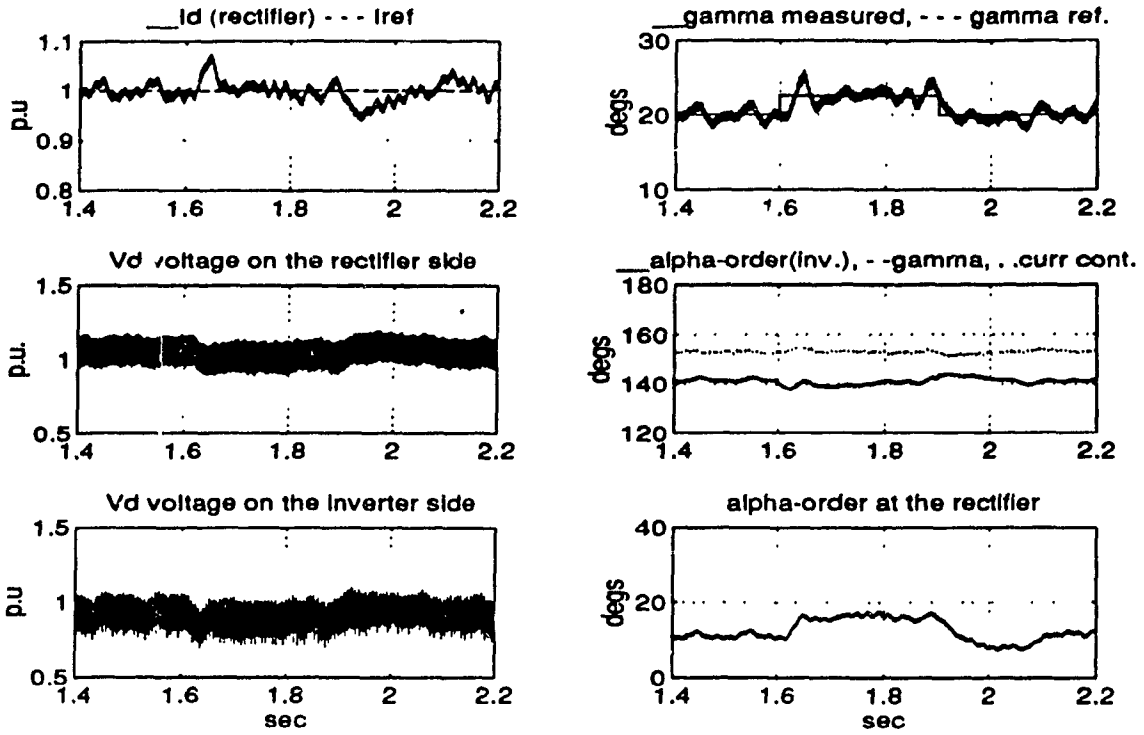


Figure 4.5a: 2.5^0 step change in the gamma reference

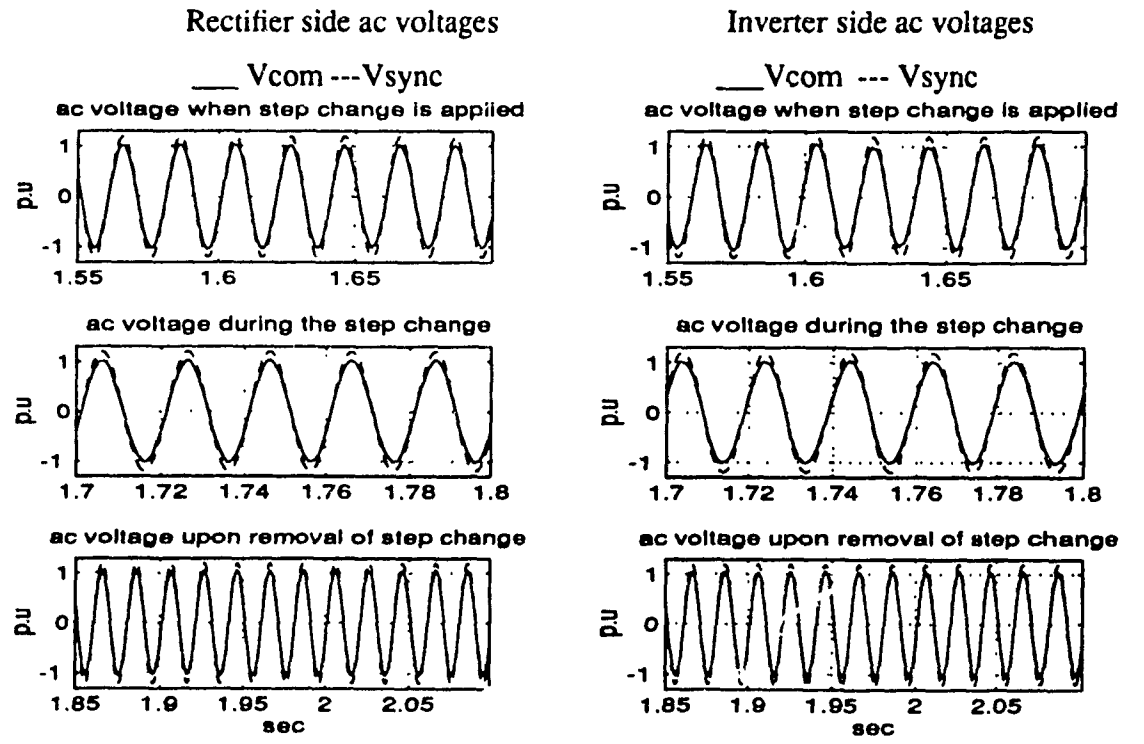


Figure 4.5b: The ac voltages for a 2.5^0 step change in gamma reference

4.3.2 Mode Shift Test

This test is performed to study the dynamics of the system when the control mode is shifted from the rectifier current controller to the inverter current controller, and back. The results are shown in Figure 4.6. Initially (at t=1.1s), the rectifier current controller is in control at the rectifier end and the gamma controller at the inverter end. At t = 1.1s, ac voltage at the rectifier is reduced by 5%, which causes the rectifier current controller to hit alpha-min, and it loses control over the current. The inverter current controller takes charge and the current is controlled to 0.9 p.u. At t = 1.5 sec, the ac voltages at the rectifier is returned to 1.0 p.u. and the rectifier current controller takes charge. However, there is a transition from one state to another. Also, the transition from rectifier current controller to inverter current controller is different from the transition which occurs from inverter current controller to rectifier current controller.

4.3.3 Fault Tests

In the following sections, results from a number of fault tests are presented and discussed.

4.3.3.1 Single-phase 1-cycle Fault at the Inverter Side(*commutation failure test*)

A commutation failure at the inverter is simulated by creating a single-phase 1-cycle fault at the inverter ac bus (at t=1.1s) which prevents the commutation occurring from one valve to another. The resulting commutation failure (Figure 4.7) causes the dc voltage to momentarily drop to zero. This causes the VDCL to operate and limit the dc current to IMIN. The ac voltage on the inverter side under these conditions collapse momentarily as seen in Figure 4.7. The valve voltage is thus distorted giving an incorrect value of gamma

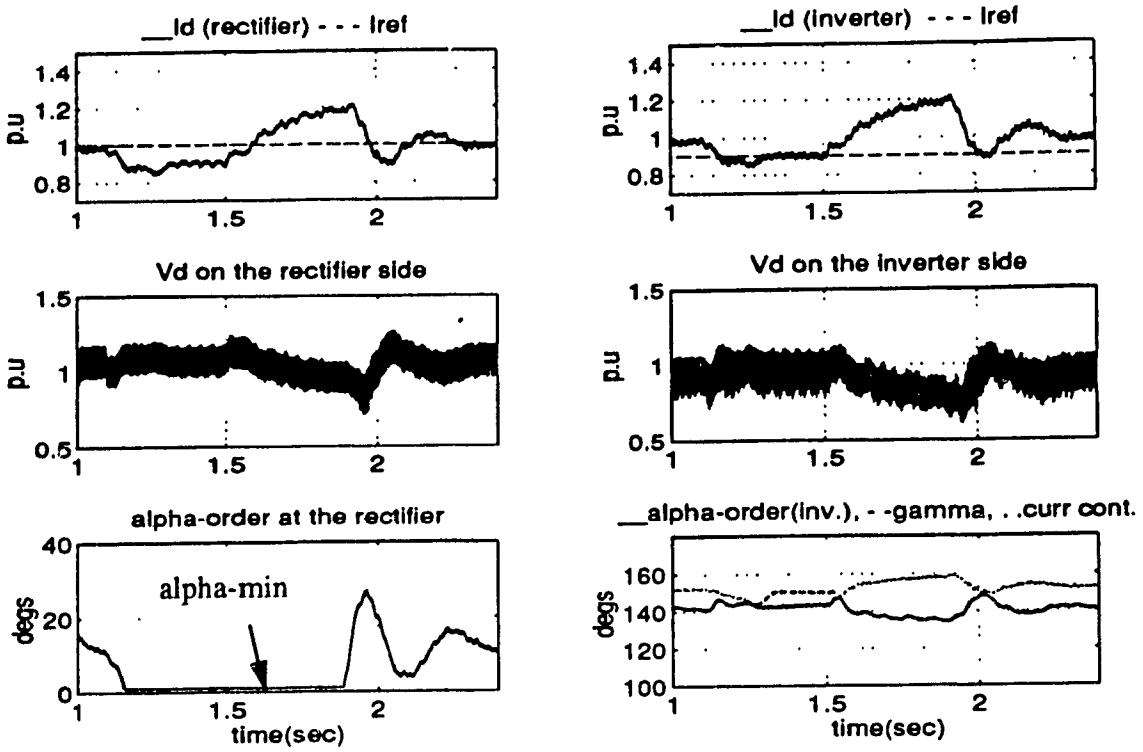


Figure 4.6a: Mode shift test

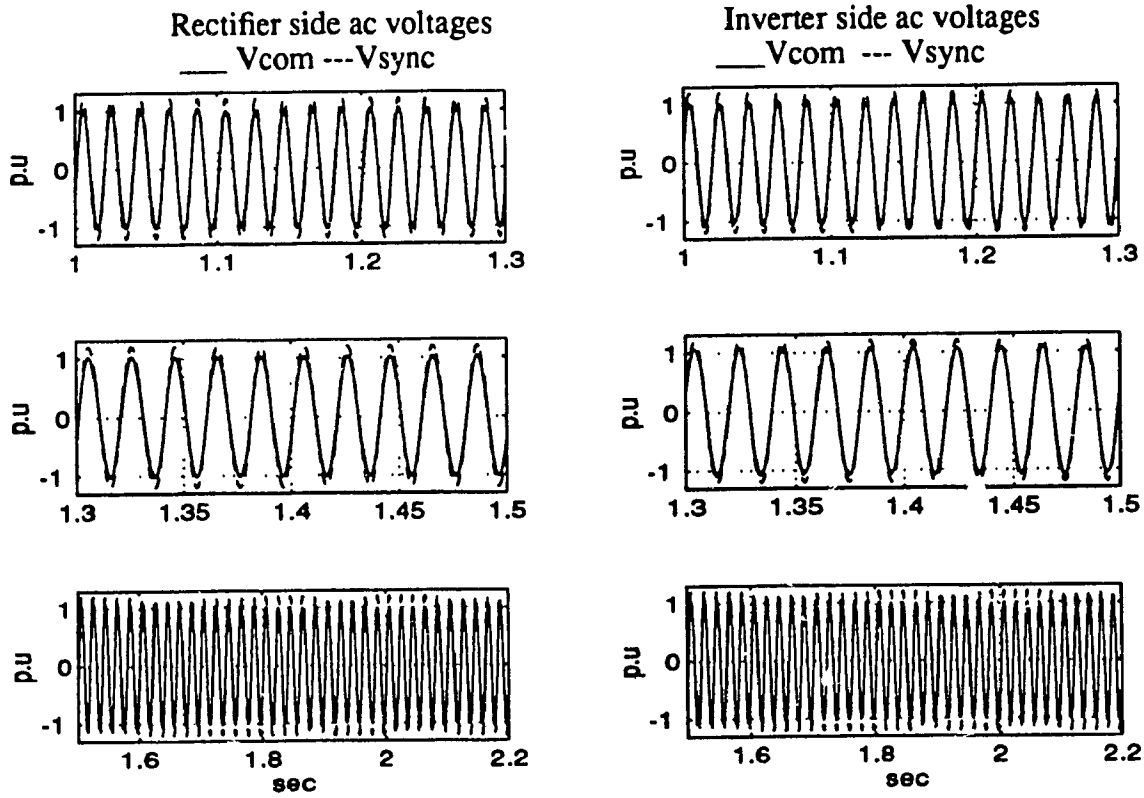


Figure 4.6b: The ac voltages for the mode shift test

measured. As a result, the PI controller output hits the alpha-max limit, as seen in Figure 4.7 The recovery process is initiated almost immediately resulting in the dc current to ramp up according to the VDCL. A transition from the inverter current controller to the rectifier current controller is also seen, similar to the one discussed previously in the initialization of the system.

4.3.3.2 Single-phase 5-cycle Fault at the Inverter Side

To study the response of the system for repetitive commutation failures at the inverter, a single-phase 5-cycle fault is applied at t=1.1s on the inverter ac bus (Figure 4.8). The initial fault causes the dc current to approach 2.0pu and collapses the dc voltage at the inverter end. The ac voltages at the inverter end are distorted as a result of this fault. The gamma controller hits alpha-max due to the reasons mentioned for the commutation failure test. Upon removal of the fault, the VDCL action insures the gradual ramp-up of dc current from zero to the prefault level in accordance with the limited current reference, IOLIM. Again, a transition is seen from the inverter current controller to the rectifier current controller during recovery.

4.3.3.3 Three-phase 5-cycle Fault at the Inverter Side

The response of the system under this fault is identical to the response obtained during a single-phase 5-cycle fault (Figure 4.9). The only obvious difference is seen at the inverter end dc voltage, where oscillations are seen due to the reflections on the transmission line.

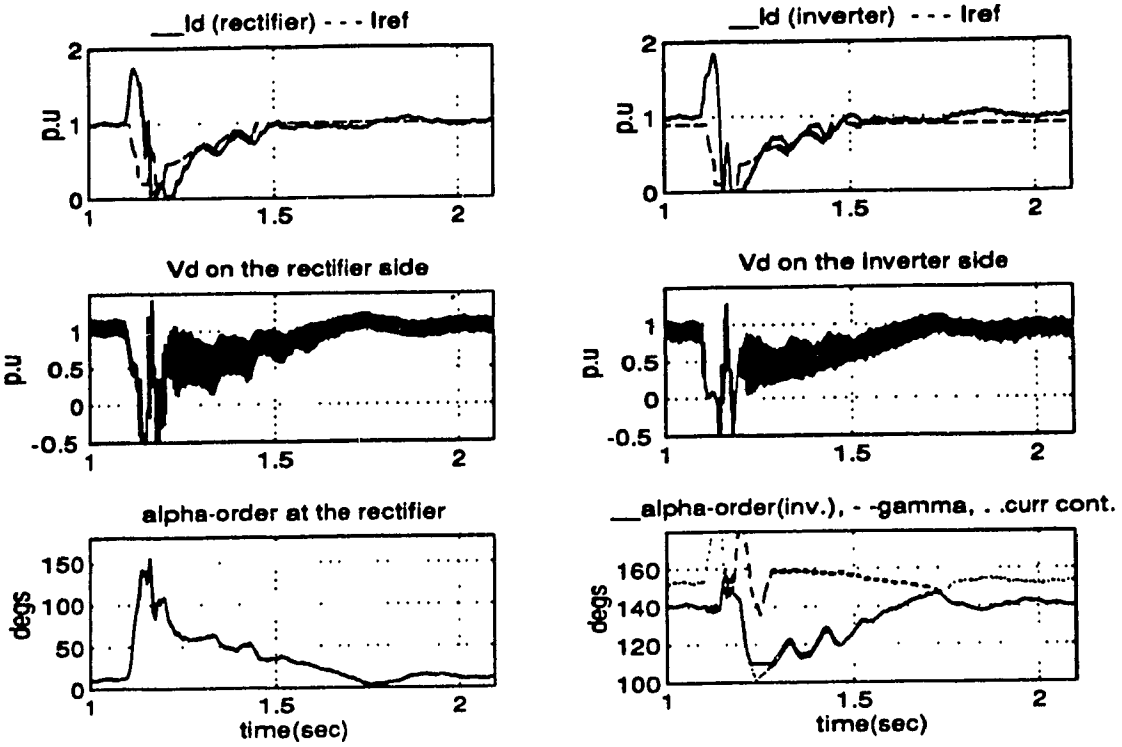


Figure 4.7a : Single-phase 1-cycle fault at the inverter

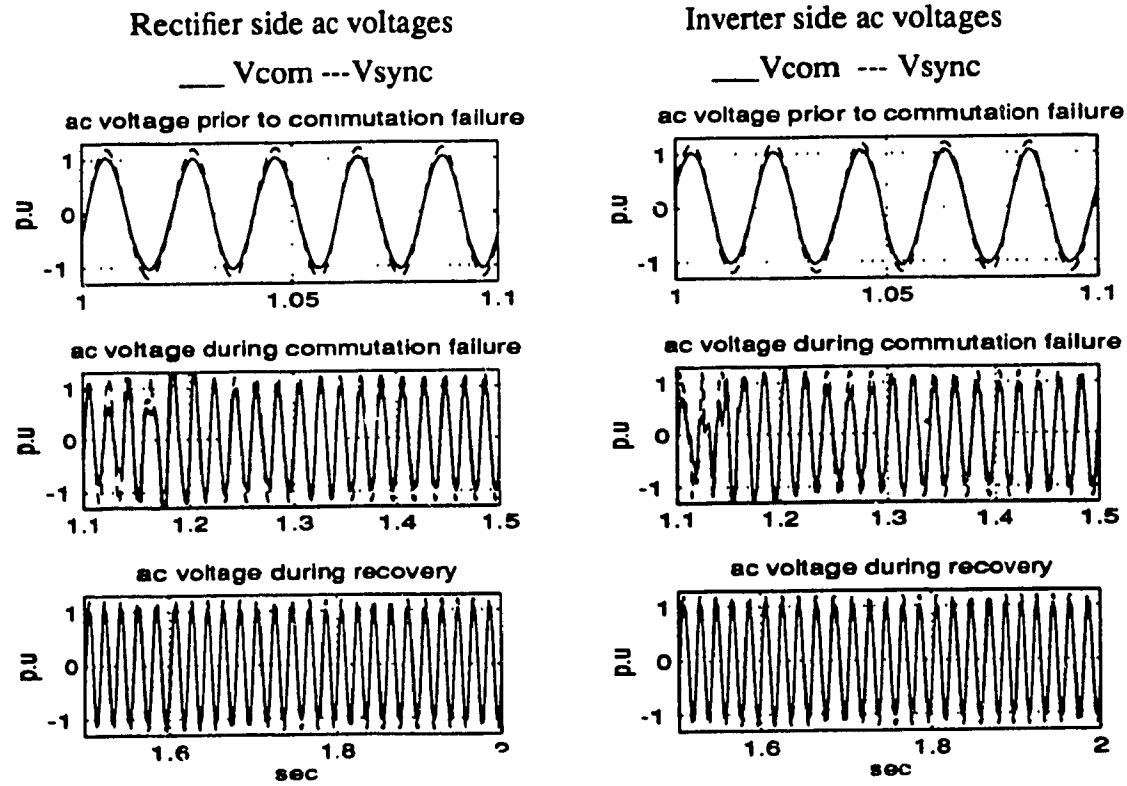


Figure 4.7b : The ac voltages for single-phase 1-cycle fault at the inverter

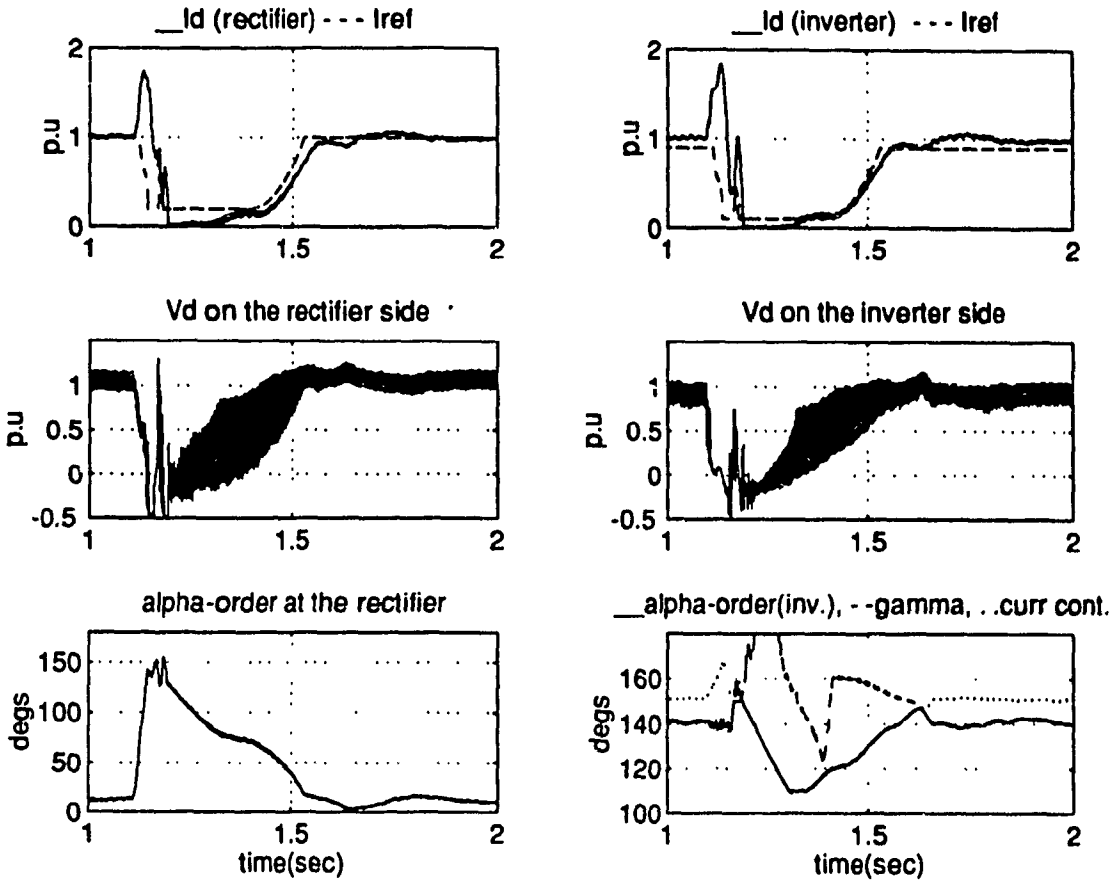


Figure 4.8a : Single-phase 5-cycle fault at the inverter

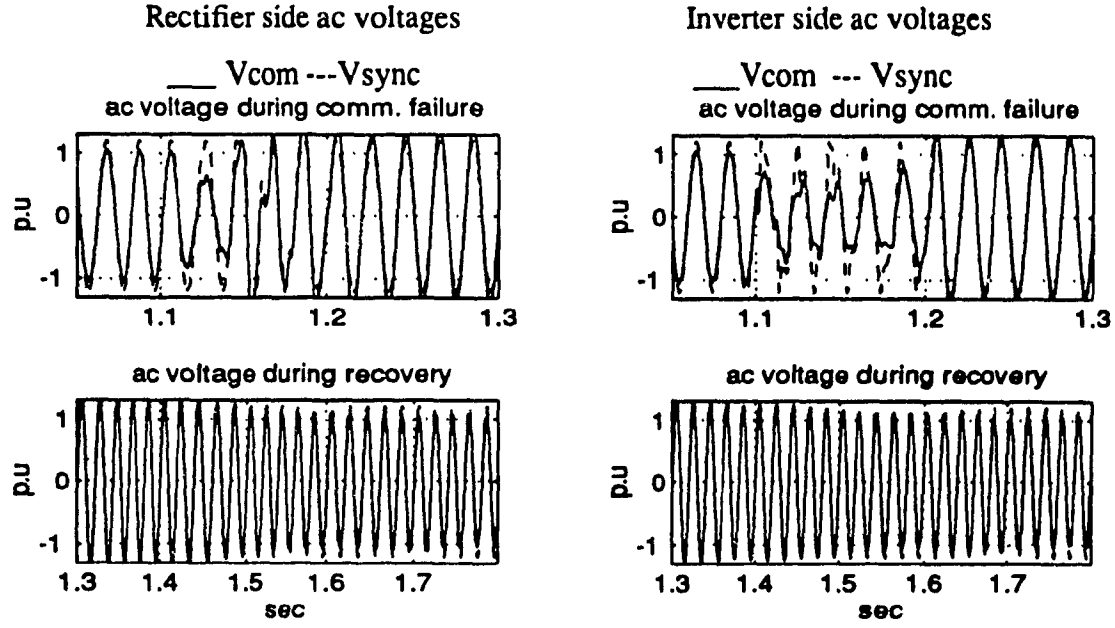


Figure 4.8 b : The ac voltages for single-phase 5-cycle fault at the inverter

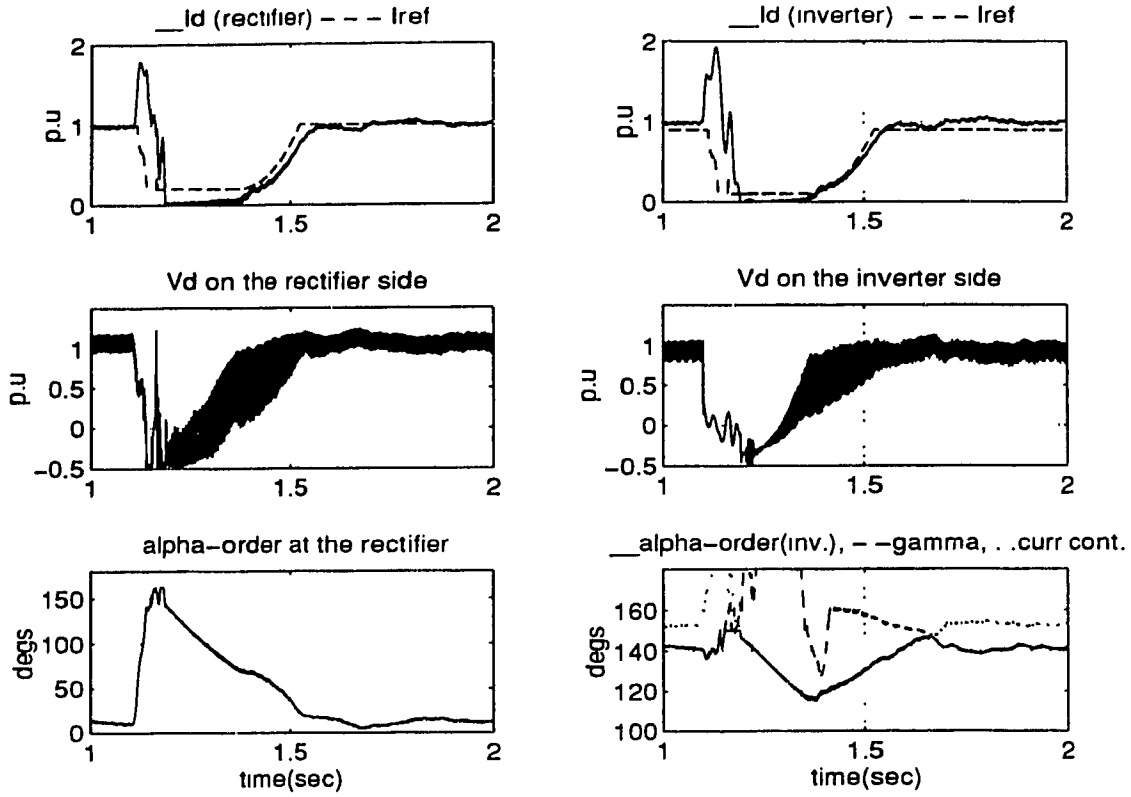


Figure 4.9a: Three-phase 5-cycle fault at the inverter

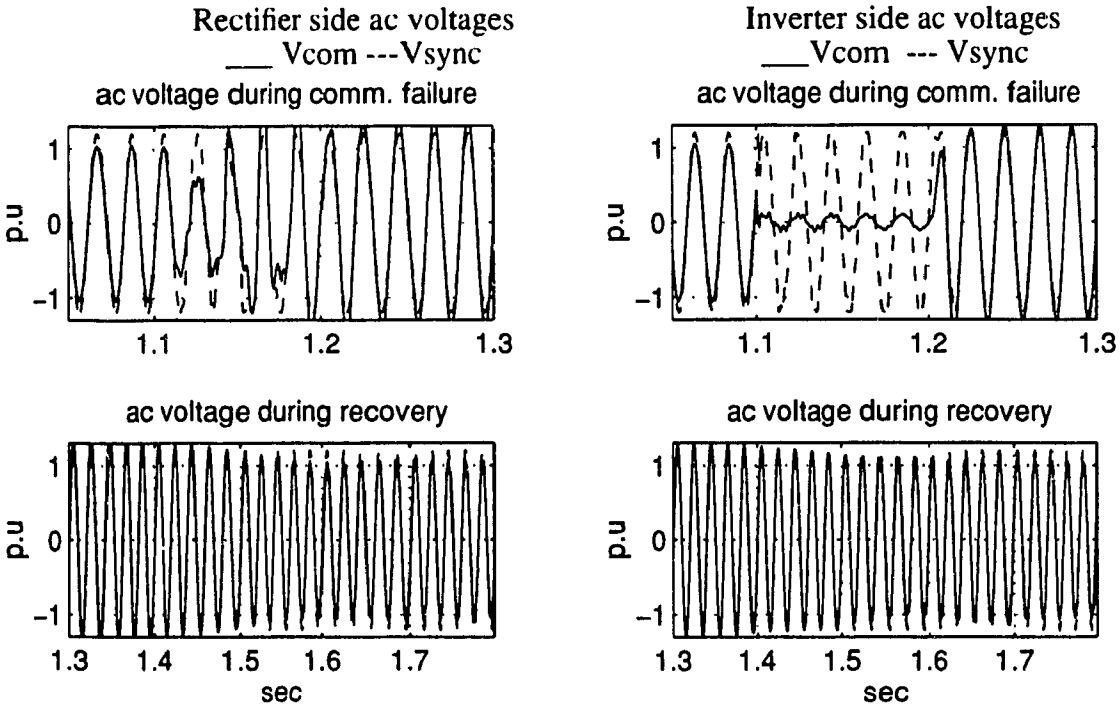


Figure 4.9b The ac voltages for three-phase 5-cycle fault at the inverter

4.3.3.4 Single-phase 5-cycle Fault at the Rectifier Side

A single-phase 5-cycle 30% fault is applied at the rectifier ac bus (Figure 4.10). The dc current during the fault contains a second harmonic component (100Hz) which is a characteristic of such a fault. Upon removal of the fault, there is a commutation failure (t=1.5s). The dc current then follows a pattern similar to the single-phase one-cycle fault at the inverter. For the results shown in the CIGRE benchmark, there is a commutation failure upon recovery, and also the level of harmonic content in the dc voltage during the fault is relatively low. The difference between the results shown here and the one presented in the CIGRE benchmark [12] could be attributed to the different types of VDCL and switch models used in the two systems.

4.3.3.5 Three-phase 5-cycle Fault at the Rectifier Side

The fault causes the dc voltage to collapse and hence reduces the current to zero due to lack of driving source voltage. The behaviour of the VDCL drops IOLIM to IMIN; however, the absence of the ac voltage at the rectifier prevents the current from recovering. Upon removal of the ac fault at the rectifier bus, the dc voltage reaches 1.0 p.u. and the current follows the same pattern (Figure 4.11) as during the initialization case.

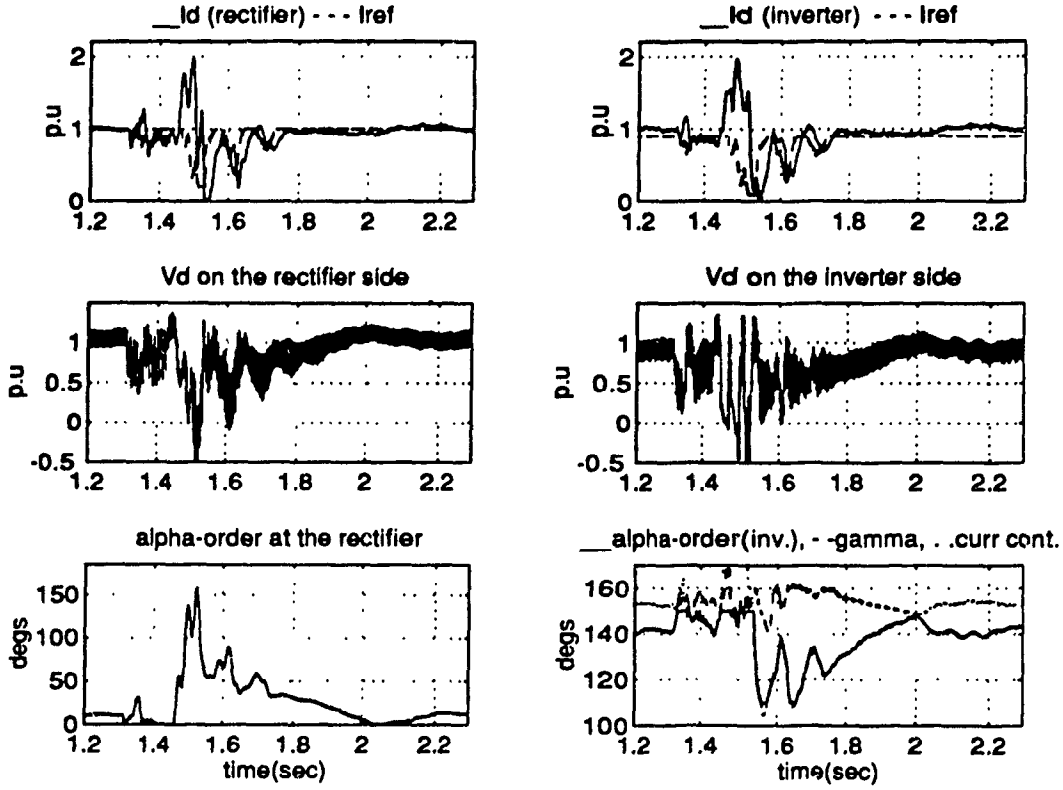


Figure 4.10a: Single-phase 5-cycle fault at the rectifier

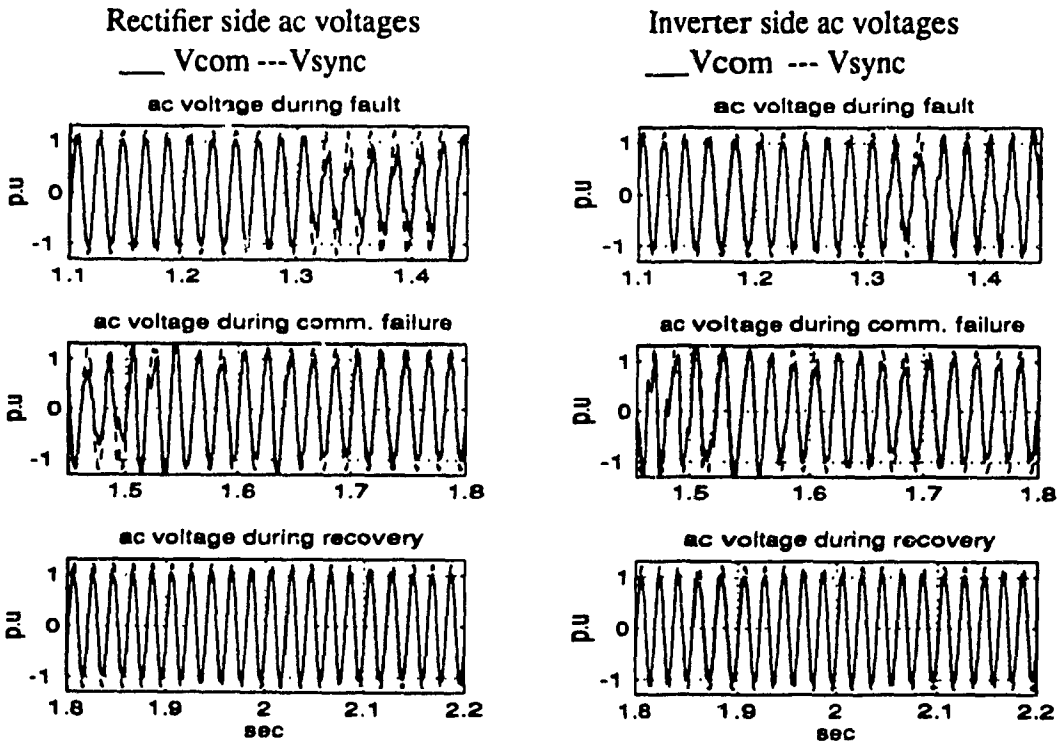


Figure 4.10b: The ac voltages for a single-phase 5-cycle fault at the rectifier

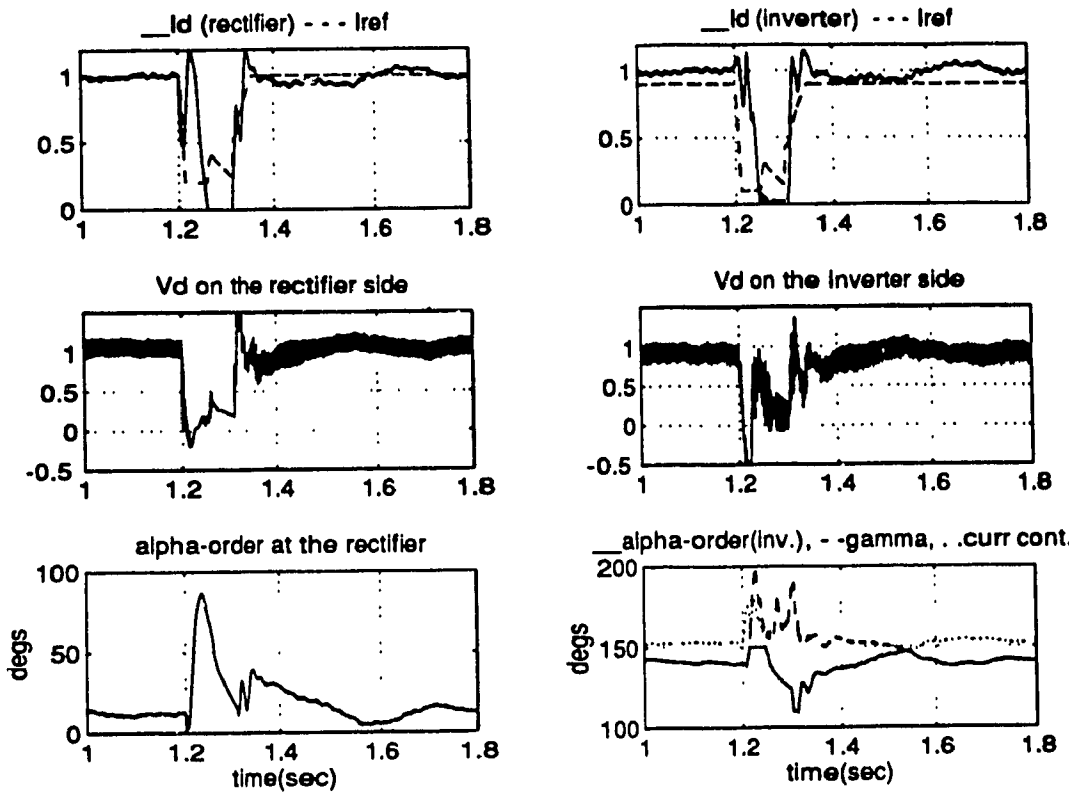


Figure 4.11a: Three-phase 5-cycle fault at the rectifier

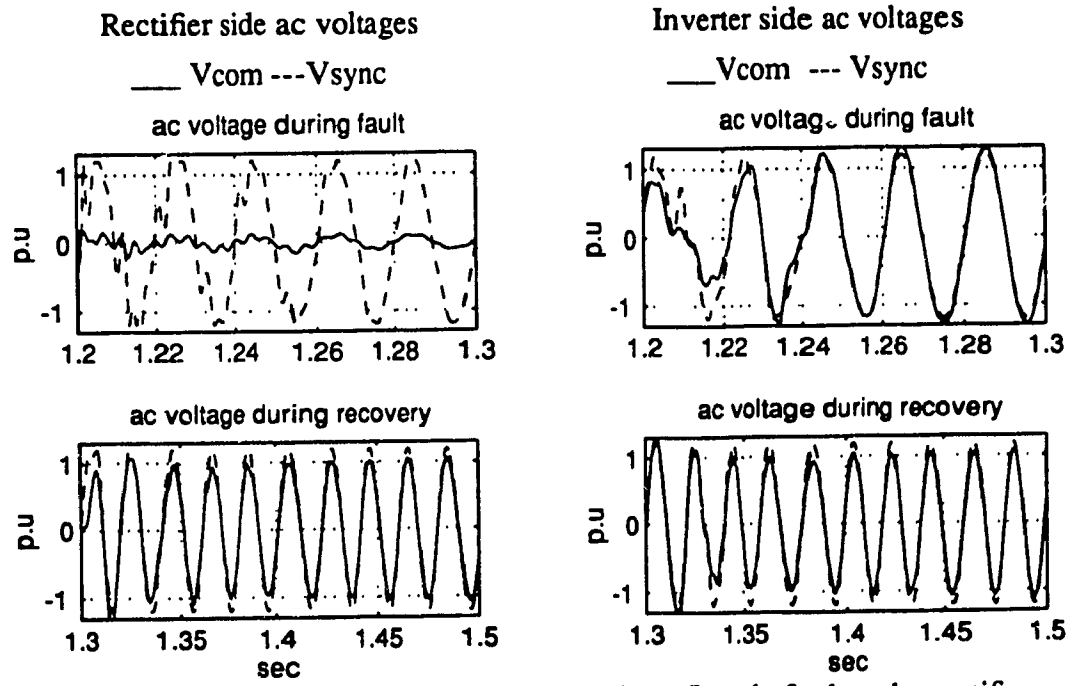


Figure 4.11b: ac voltages for three-phase 5-cycle fault at the rectifier

4.3.3.6 DC Line Fault at the Rectifier Side

A dc line fault is applied from 1.1s to 1.4s at the dc line side of the rectifier (Figure 4.12). The fault causes the dc voltage to collapse and the dc current to rise to a value greater than 2.0 p.u., a characteristic of this type of fault. The action of the VDCL causes the current to be limited to IMIN. From 1.3s to 1.4s a protection signal, ALPRET, is applied to deionize the fault arc. Upon removal of the fault, the dc current ramps up due to the action of the VDCL. The small delay observed between Idc and IOLIM is due to the use of a low-pass filter in the VDCL unit.

4.3.3.7 DC Line Fault at the Inverter Side

A dc line fault is applied from 1.1s to 1.4s at the dc line side of the inverter (Figure 4.13). The fault causes the dc voltage to collapse and the dc current to rise to a value greater than 2.0 p.u. The current in the inverter side is shorted out by the dc line fault, and hence during the fault duration the dc current at the inverter end is zero. The action of the VDCL causes the current to be limited to IMIN. From 1.3s to 1.4s a protection signal, ALPRET, is applied to deionize the fault arc. Upon removal of the fault, the dc current ramps up due to the action of the VDCL. The small delay observed between Idc and IOLIM is due to the use of a low-pass filter in the VDCL unit.

4.4 Summary

In this chapter, results of various ac-dc fault/tests conducted on the HVDC converter system operating with a weak ac system are presented. The results show the satisfactory performance of the system with the controllers used.

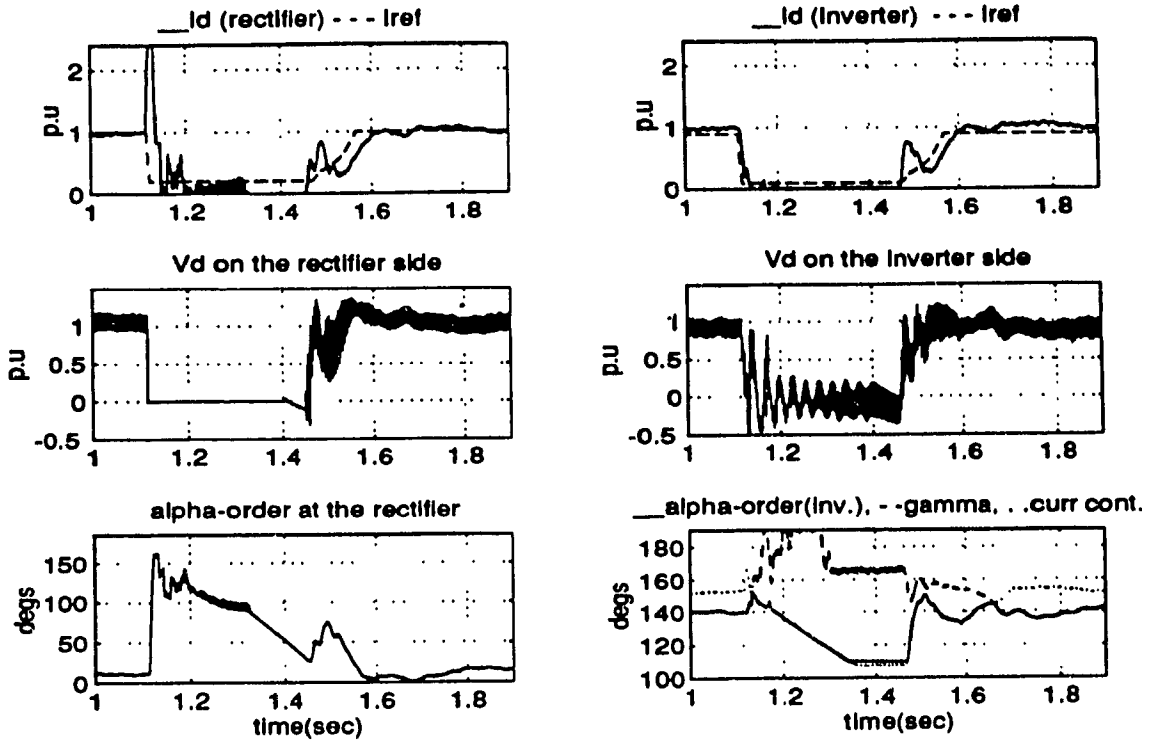


Figure 4.12a : dc line fault at the rectifier side

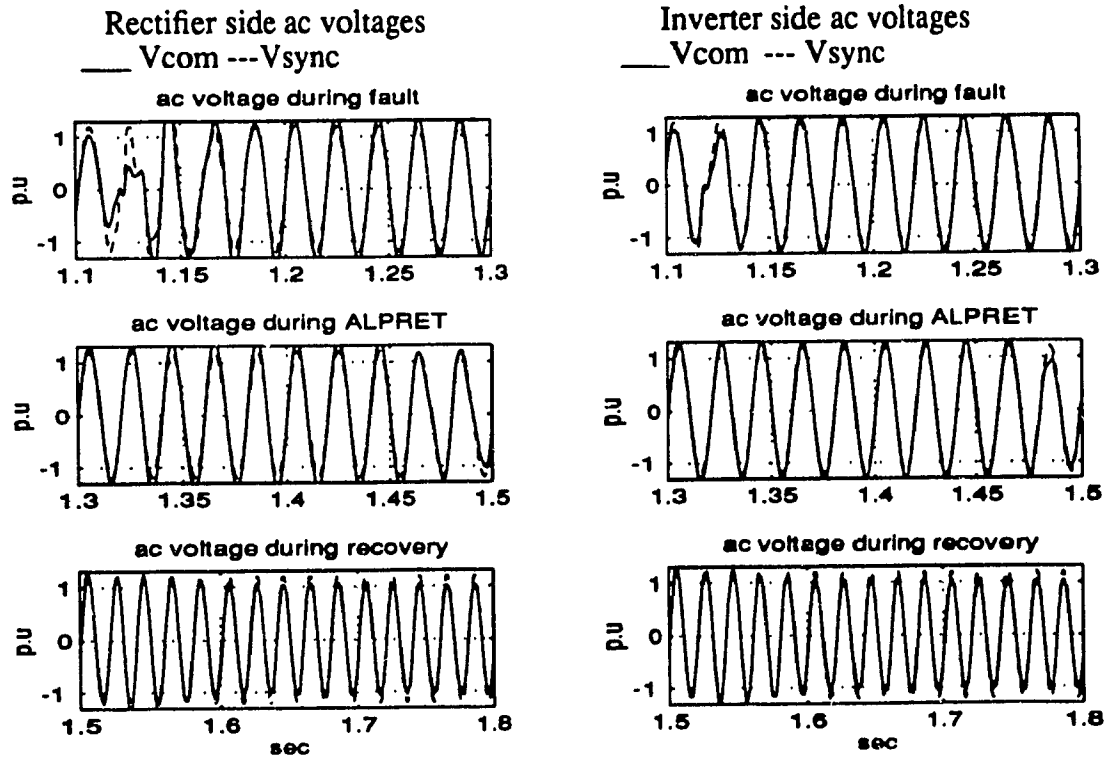


Figure 4.12b : The ac voltages for a dc line fault at the rectifier side

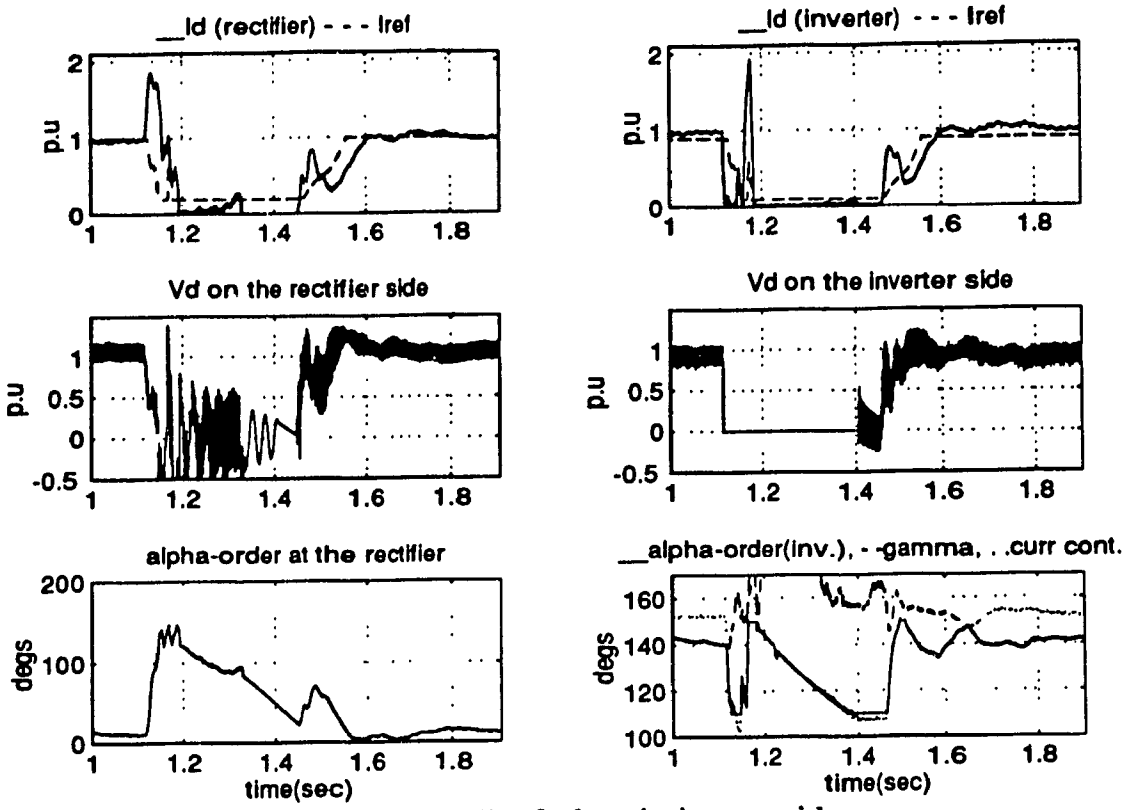


Figure 4.13a : dc line fault at the inverter side

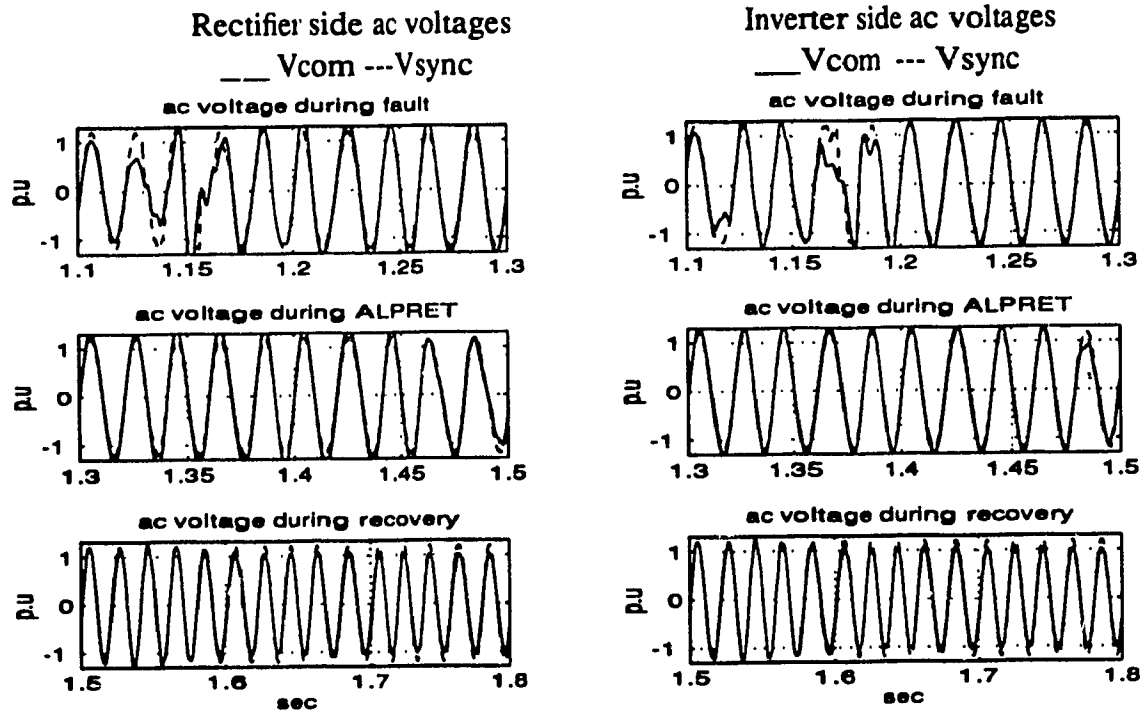


Figure 4.13b : ac voltages for a dc line fault at the inverter side

Chapter 5
Conclusions

In this thesis, the CIGRE benchmark based HVDC converter system operating with weak ac systems was studied using EMTP. The main contribution of this thesis is the derivation and implementation of models for different parts of the HVDC system in EMTP.

The specific contributions are :

1) Two types of GFU's, a conventional and a DQ-type, are analyzed and designed. Both GFU's use a phase locked loop in conjunction with a voltage controlled oscillator. A performance comparison between the two gate firing units showed that they are equally capable of operation in a weak ac system having high levels of pollution and harmonic distortion in the commutation voltage. On the other hand, due to the absence of a low-pass filter in its control loop, the DQ-type gate firing unit is relatively easier to design and is faster than the conventional type.

2) A Voltage Dependent Current Limit unit is developed which provides a reference to the current controller. The VDCL unit incorporates a static and a dynamic sub-unit which control the current reference during the steady state and transient conditions respectively.

3) A gamma measuring unit is developed. This unit is used in conjunction with the gamma controller at the inverter-end of the HVDC system.

4) A detailed model of the converter is presented which incorporates an ideal switch model with a parallel snubber circuit. Optimization tests for the snubber circuit

shows that for the selected range of R (200 Ω - 10kΩ) and C (1μF - 0.0125 μF), the value of R has a larger impact on the converter performance than C. A value of R = 10kΩ and C = 1.0μF were selected after optimization. These values may not have any co-relation with the values used in practice, however, they provide satisfactory commutation voltage for the switch used and the corresponding system model.

5) To study the dynamic behavior of the system, 11 tests are carried out on the HVDC system. The step changes in the rectifier and the inverter current controllers along with a step change in gamma controller are used to optimize the parameters of respective controllers. To study the response of the system under ac fault conditions, 1-phase and 3-phase faults are applied at the rectifier and the inverter ac systems. The ac faults were of either 1 or 5 cycle durations. These tests demonstrate the ability of the system to recover after removal of the fault. DC line faults at the dc side of the rectifier or inverter sides were also studied. These tests verify the operation of protection signals such as ALPRET in the rectifier current controller. The dc line faults also verify the operation of the VDCL. The detailed results from these tests prove the validity of the controllers and protection circuits used.

The work done here provides very detailed information, which is presently unavailable elsewhere, on aspects of modelling an HVDC system operating with weak ac systems. It is anticipated that these details will be helpful to educators and utility planners studying HVDC systems.

Recommendations for Future Work

In the modelled HVDC system, a 6-pulse model has been utilized for reasons of speed and minimization of cpu usage. In reality, the CIGRE benchmark system is a 12-pulse sys-

tem. It will, therefore, be more practical to update the converter model to a 12-pulse unit. Within EMTP, there is practically no limit as to the size and number of converter units that can be modeled.

The use of traditional PI controllers in the system restricts the operating point of the system. Moreover, the parameters of the PI controller can only be optimized over a small operating range. To overcome these problems, controllers which adapt to the circuit conditions may offer superior performance. Thus, the advantages offered by modern controllers based on Fuzzy Logic [19] or Neural Networks [20] can be explored.

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Appendix A

Transformer Calculations

In this Appendix, parameters of the transformers used in this simulation study are calculated.

Section I: Rectifier side

For the transformer at rectifier end, the following quantities are given:

$Z_{trans} = 0.18$ p.u.; $V_{prir} = V_{base} = 345$kV; $S_{base} = 1196$MVA; $V_{dr} = 500$kV

Step 1: To find the turns ratio at the rectifier side

In-order to find the turns ratio, we have to find the voltage V_{sec} (secondary voltage of the transformer), neglecting the voltage drop due to the commutation resistance ,

$$V_{dr} = 1.35\, V_{L\text{-}L} \cos \alpha_n \qquad (A.1)$$

where,

V_{dr} is the dc voltage at the rectifier end; and the value of α_n under steady state is 18^o.

From (A.1), $V_{L\text{-}L} = 389$kV.

$$\text{turns ratio} = n_r = \frac{V_{prir}}{V_{secr}} \qquad (A.2)$$

From (A.2), the turns ratio = 0.885.

Step 2: To find the primary and secondary impedances of the transformer

Using V_{base} and S_{base}, Z_{base} is given by the following equation,

$$Z_{base} = \frac{(\text{base kV}_{L\text{-}L})^2}{(\text{base MVA})_{3\phi}} \qquad \text{(A.3)}$$

Using (A.3), $Z_{base} = 99.52\Omega$

$$Z_{trans} = (Z_{base})\,(Z_{p.u.}) \qquad \text{(A.4)}$$

From (A.4), $Z_{transr} = 17.91\Omega$

Assuming $Z_{prir} = Z'_{secr} = Z_{transr} / 2$, where Z'_{sec} is the secondary impedance of the transformer referred to the primary side, $Z_{prir} = 8.956\Omega$. The inductance at the primary side of the transformer, L_{prir} is:

$$L_{prir} = \frac{Z_{pri}}{\omega} \qquad \text{(A.5)}$$

In (A.5), $\omega = 2 * \pi * 50$, therefore, $L_{prir} = 28.50\text{mH}$

$$L_{secr} = \frac{Z'_{sec}}{\omega\, n_r^2} \qquad \text{(A.6)}$$

From (A.6), $L_{secr} = 36.40\text{mH}$

Section II: Inverter side

For the transformer at the rectifier end, the following quantities are known:

$Z_{trans} = 0.18$ p.u., $V_{prii} = V_{base} = 230$kV, $S_{base} = 1196$MVA, $V_{di} = 500$kV

Step 1: To find the turns ratio at the inverter side

In-order to find the turns ratio, we have to find the voltage V_{sec} (secondary voltage of the transformer), neglecting the voltage drop due to commutation resistance [13],

$$V_{dr} = 1.35\, V_{L\text{-}L} \cos\gamma_n \qquad \text{(A.7)}$$

where, V_{di} is the dc voltage at the inverter end; and the value of γ under steady state is 18^o;

From (A.7), $V_{L\text{-}L} = 389$kV.

$$\text{turns ratio} = n_i = \frac{V_{prii}}{V_{seci}} \qquad \text{(A.8)}$$

From (A.8), the turns ratio = 0.591.

Step 2: To find the primary and secondary impedances of the transformer

Substituting V_{base} and S_{base} in equation A.3, $Z_{base} = 44.23\Omega$. Using (A.4), $Z_{trans} = 7.961\Omega$

Assuming $Z_{prii} = Z'_{seci} = Z_{transr} / 2$, where Z'_{seci} is the secondary impedance of the transformer referred to the primary side, $Z_{prii} = 3.980\Omega$

The inductance at the primary side of the transformer, L_{pri} is

$$L_{prii} = \frac{Z_{prii}}{\omega} \qquad \text{(A.9)}$$

In (A.9), $\omega = 2 * \pi * 50$. From (A.9), $L_{prii} = 12.67$mH.

$$L_{seci} = \frac{Z'_{seci}}{\omega \; n_r^2} \quad \text{(A.10)}$$

From (A.10), $L_{secr} = 36.40$mH.

Appendix B

Harmonic Filter Design

This appendix covers the design of filters for the 5^{th} and 7^{th} harmonics.

To design the hamonic filters at the rectifier side, the following assumptions are made:

1) the 5^{th} harmonic filter provides 70MVars

2) the 7^{th} harmonic filter provides 50MVars

The reactive power as a function of the capacitance is given by

$$Q(\text{MVars}) = (V_{l\text{-}l}\,(\text{kV}))^2\,\omega\,C \qquad \text{(B.1)}$$

where, Q is the reactive power; $V_{l\text{-}l}$ is the Line-Line commutation bus voltage; ω is the frequency of operation in rad/sec; and C is the filter capacitance.

A single tuned filter configuration is used to filter the 5^{th} and 7^{th} harmonic components in the commutation voltage. Equation B.1 is used to obtain the capacitances for the 5^{th} and 7^{th} harmonic filters.

For the 5^{th} harmonic filter

$$70\ \text{MVars} = (345\text{kV})^2 * 2*\pi * 50 * C_5 \qquad \text{(B.2)}$$

From (B.2), we can calculate C_5 as :$C_5 = 1.872\mu\text{F}$

The inductance L_5 is obtained using the following equation

$$f = \frac{1}{(2\pi\sqrt{LC})} \qquad \text{(B.3)}$$

Using (B.3) and f as 250Hz (5^{th} harmonic), L = 216.5mH.

Similarly, using Q = 30MVars, and f = 350Hz, the capacitance and inductance for a 7th harmonic filter are 0.802μF and 257.8mH respectively.

A resistance of 1Ω is added in series to 5th and 7th harmonic filters to provide damping.

Appendix C
List of Publications

1. Papers published on this research:

V. Khatri, V.K. Sood, H. Jin, "EMTP Simulation of an HVDC Rectifier Operating Under Weak AC System", 1994 IEEE PELS Workshop on Computers in Power Electronics, 7-10 Aug. 1994, Trois Rivieres, Quebec. Canada.

V. Khatri, V.K. Sood, H. Jin, "Analysis and EMTP Simulation of a Conventional Gate Firing Unit for HVDC Converters Operating with Weak AC System", 1994 Canadian Conference on Electrical and Computer Engineering, 25-28 Sept 1994, Halifax, NS, Canada.

2. Papers submitted on this research:

V. K. Sood, V. Khatri, H. Jin, "Performance Assessment using EMTP of two Gate Firing Units for HVDC Converters operating with a Weak AC Systems", submitted to International Conference on Power System Transients, Sept. 3-7 1995, Technical University of Lisbon, Portugal.

V. K. Sood, V. Khatri, H. Jin, "EMTP Modelling of CIGRE Benchmark Based HVDC Transmission System Operating with Weak AC Systems", submitted to International Conference on Power Electronics Drives and Energy Systems for Industrial Control, 8-11 Jan 1996, New Delhi, India.