Experimental Investigation of Interdigitated Back Contact Solar Cell Fabrication, and Porous Silicon as an Anti-Reflection Coating.

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Abstract

Experimental Investigation of Interdigitated Back Contact Solar Cell Fabrication, and Porous Silicon as an Anti-Reflection Coating

In this work experimental investigation on Interdigitated Back Contact (IBC) silicon solar cells and application of porous silicon as an anti-reflection (AR) coating have been considered. For this purpose, Interdigitated Back Contact solar cells with active areas of approximately one square centimeter were fabricated on both single- and double-side-polished silicon wafers. In order to investigate the effects of (a) impurity type and (b) the role of wafer thickness on the cell function, wafers of n- and p-type silicon (with resistivity of 11 and 5.6 ohm-cm, respectively) having 300 and 100 micron thickness were used in the cells fabrication. Two different diffusion techniques, spin-on sol-gel and ion-implantation were employed to do the boron diffusion process. The use of SiO_2 and porous silicon was investigated as anti-reflection coatings to cover the front surfaces of the cells.

The devices were characterized under dark and light conditions and the effects of parameters such as series and shunt resistances, reverse saturation current, ideality factor, open circuit voltage, short circuit current, fill factor, output power, and efficiency were measured and discussed in details.

(1) A technique for creating uniform porous silicon layers from back side point contacts is found.

(2) While porous silicon is found to have very low reflectivity, it does not enhance

solar cell performance.

(3) The failure of porous silicon as anti-reflection coating is discussed.

(4) The best cells formed were those having an 1100 Å SiO_2 layer as anti-reflection coating.

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CHAPTER 1

Introduction

1.1 Solar Cell

The solar cell, or photovoltaic (PV) device, is usually a solid-state (semiconductor) device that produces useful electricity in the form of DC voltage and current directly from the sun's radiation via the PV effect [1]. The PV effect can be described as follows [2]:

Light, which is pure energy, enters a PV cell and imparts enough energy to some bound electrons to create electron-hole pairs. A built-in-potential in the cell acts on these electrons and holes to produce a voltage (the so-called photo-voltage), which can be used to drive an external electrical load.

1.2 History of PV devices

The development of PV cells can be traced back 140 years to the discovery by Becquerel (1839) that a photovoltage resulted from the action of light on an electrode in an electrolyte solution. Some 40 years later, Adams and Day (1877) observed a similar effect in the solid material selenium. By 1914 solar conversion efficiencies of about 1% were achieved with selenium [3]. Selenium cells have never become practical as energy converters because their cost is too high relative to the

tiny amount of power they produce (1% efficiency) [2]. Research progressed on a variety of materials. Notably, in 1954 Reynolds et al.[1] observed the PV effect at a metal/single crystal CdS junction which led to the development of Cu_2S/CdS thin-film solar cell during the early 1960's. The modern era for photovoltaics began in 1954 when Chapin et al.[3] reported a solar conversion efficiency of 6% for a silicon single-crystal cell. With improved technology, silicon cell efficiency under terrestrial sunlight had reached 14% by 1958 [3]. By taking advantage of new technology, research has rapidly raised the efficiency of gallium arsenide-based cells reported by Jenny et al. (1956) with 4% efficiency up to efficiencies approaching 24% (1983) [3]. Tables 1 and 2, show the confirmed terrestrial cell and module efficiencies measured under the global AM1 spectrum (1000 W/m^2) at temperature 25 ^oC respectively [4].

	InP	GaAs	GaAs thin	Si	Si multicrystalline
Efficiency (%)	21.9	25.1	23.3	24	17.8
Date	4 / 1990	3 / 1990	4 / 1990	9 / 1994	3 / 1994

TABLE 1. Confirmed terrestrial cell efficiencies under AM1 spectrum

	CdTe	$CuInGaSe_2$	Si	Si (multicrystalline)
Efficiency (%)	7.8	9.7	21.6	15.3
Date	10 / 1993	5 / 1991	2 / 1994	10 / 1994

TABLE 2. Confirmed terrestrial modules under AM1 spectrum

Although GaAs solar cells have higher efficiencies, superior radiation resistance and better performance over a greater range of operating temperature than Si cells, and although GaAs technology is the best understood technology after Si, GaAs solar

cells have not been commercialized, essentially because of their cost [5]. In special PV applications, where highest possible performance is of paramount importance and cost is secondary, GaAs cells represent the best present option among the single junction cells. However, Si PV cells have become commercialized and in many countries around the world are being used to produce electricity [6,7,8,9]. In addition, power plants with capacities over 1 MW have been built, and are working successfully [9,10].

During 1994 the annual world-wide shipments of PV modules by manufacturers represented approximately 70 megawatts (MW). In comparison, roughly 23 MW were shipped in 1985, which means that the industry has grown over 300% in just 10 years [11]. On the other hand, the cost of Si cells has decreased from $15 per peak watt, W_p, (power provided by a solar cell at an insolation 1000 W/m^2 and cell junction temperature of 25 ^oC) in 1983 to about $4 W_p in 1993 [12]. The above facts imply that the Si single-crystal PV cell has become the prototype of all homojunction cells and has been the prime focus of research and development. At this point it should be mentioned that there is another area in PV technology in which many research groups around the world are working on it and seems to be very promising in terms of cost and this is thin film technology. CdTe, a-Si/a-Si, CIS (copper indium diselenide) are the materials which are the best in terms of stability, cost and performance [13] in this technology. Two U.S. Companies (Golden Photon Inc.[GPI] and Solar Cells Inc.) have publicly announced manufacturing plants and GPI facility is nearing completion at 2-MW annual production. In thin film technology also it seems that a-Si is the leading material [13].

1.3 Conventional solar cell design

A schematic representation of a conventional p-n homojunction Si solar cell is shown in Figure 1.1 [14].

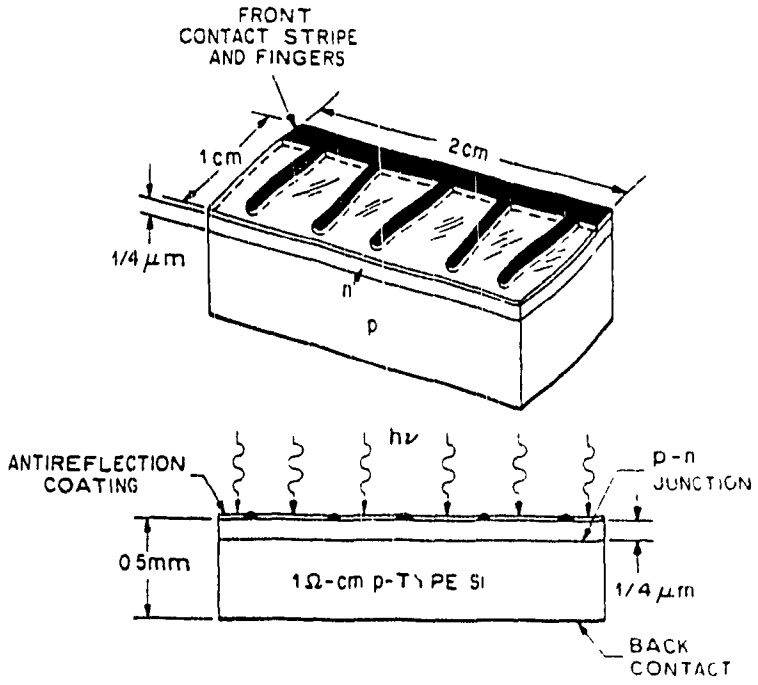


Figure 1.1: Schematic representation of a conventional Si solar cell design.

It consists of a shallow p-n junction on the surface, a front ohmic contact stripe and fingers, a back ohmic contact that covers the entire back surface, and an anti-reflection coating on the front surface [14]. Due to the difference in doping type from one side of the junction to the other, there will be creation of a space charge region at the junction. The space charge region establishes an electrostatic potential between the n- and p-region and thus creates an electrostatic field in the substrate [15].

Photons of sufficient energy (equal or greater than band gap energy, E_g) impinging on the cell's front surface create electron-hole pairs throughout the substrate [16]. Some of these free carriers are swept across the junction and consequently give rise to the development of a photocurrent through the substrate. This current will be introduced to the external circuit by means of ohmic contacts. The front contact is designed such that there is sufficient area not covered by metal, to allow the incident photons to reach the Si substrate. An anti-reflection coating is necessary since the high refractive index of silicon would otherwise result in substantial loss of power through reflection of the incident light [5].

1.4 Methods to increase the efficiency of PV solar cells

There are various methods to increase the PV cell efficiencies:

- anti-reflection (AR)coating. Deposition of an AR coating at the surface will minimize the surface reflectivity, allowing more incident photons to be captured [2].
- texturized surface. Another method for reducing reflection from a silicon surface is the use of a texturized surface, achieved by a crystallographic etch which results in surfaces with pyramidal topography. Multiple reflections at these surfaces will increase the possibility for light penetration into the silicon [17,18,19].
- porous silicon (PS). PS formed at the front surface of Si cells by electrochemical etching of Si in hydrofluoric (HF) acid can improve Si cell efficiency due to its highly texturized surface.
- back-surface field (BSF). Back surface fields are built-in fields at the back of a solar cell that reflect minority charge carriers back toward the junction and enhances the cell's carrier collection efficiency and thus its open circuit voltage and short cir-

cuit current [2].

• Interdigitated Back Contact (IBC) design. A major strategy for reducing the system cost and increasing efficiency of PV cells is to concentrate sunlight onto the surface of the solar cell [2]. The use of conventional Si solar cells with concentrators has been seriously limited by the low efficiencies obtained at high illumination intensities [20]. Efforts to improve the conventional Si solar cell's efficiency at high intensities have been directed toward reducing the device's internal resistance, which is mainly caused by the high resistivity of thin front surface diffused layer [20]. The series resistance can be lowered by addition of a metal grid pattern using narrow, closely spaced metal fingers, but this grid pattern will block a significant portion of the light. An alternate cell for use at high intensities is the interdigitated back contact solar cell (IBC), whose structure is shown in figure 1.2 [16,17,20]. The main advantage offered by the IBC cell is the decoupling of the electrical and optical properties of the conventional solar cell [16].

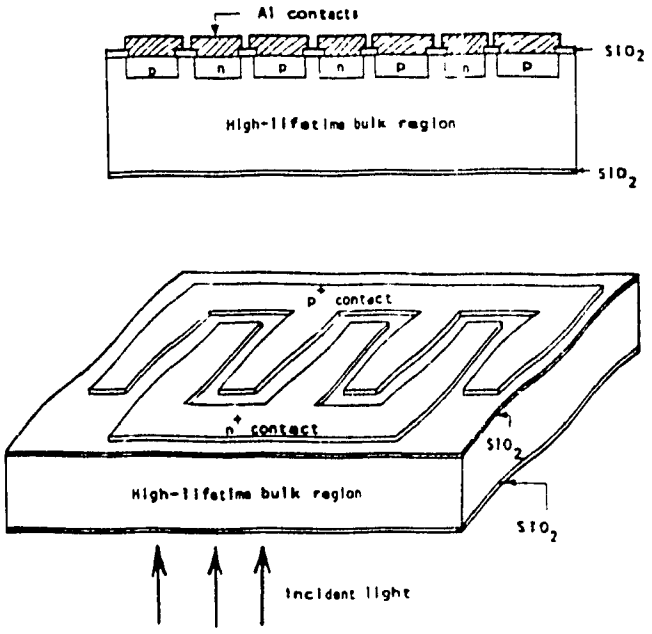


Figure 1.2: An IBC solar cell and its cross section.

In this device electrons and holes are generated in a high-lifetime bulk region and are collected at interdigitated diffused junctions on the back side of the cell. With both n^+ and p^+ junctions on the back side of the device, there is no metallization pattern on the front surface to shadow the incident photon flux. As a result, the main advantage offered by the IBC cell is the decoupling of the electrical and optical properties of the conventional solar cell [16]. In this design, the ohmic contacts may be optimized to maximize their electrical performance and the cell's front surface may be optimized to maximize photon capture over the special range of interest. However, it must be noted that, under these conditions, the performance of the cell depends upon sensitivity of the carrier lifetime through the bulk of the Si crystal and the surface recombination velocity at the surface of the wafer.

1.5 Objectives of the thesis

N-type, 300 micron-thick, IBC solar cells have been previously fabricated in the Microelectronics lab at Concordia University with efficiencies of about 1%, using a 4-mask process. The objectives of this thesis are:

a) To fabricate IBC cells using these masks and to optimize the cells performances by considering the following effects

- the electron mobility
- the hole mobility
- the substrate thickness
- sol-gel diffusion
- ion-implantation

b) To make porous silicon layers by the electrochemical etching on both n- and p-

type silicon wafers, and to optimize the conditions to minimize the reflectivity of the porous layer.

c) To investigate the use of porous silicon as an antireflection coating for solar cells.

1.6 Summary of the thesis

The principal findings and contributions of this thesis are in the areas of anti-reflection coatings, type and thickness of substrate and their effects on the IBC solar cell performance.

The contents of the thesis have been organized as follows:

Chapter 2 presents some theoretical considerations relevant to IBC cell design and performance. Other topics such as: spectral response, current-voltage characteristics under dark and illuminated conditions, and porous silicon formation techniques and properties will be discussed.

Chapter 3 presents the results of simulations done to optimize the parameters such as diffusion time and temperature under which the fabrication must be done. The four masks used in the cell fabrication, and a summary of the process sequence are described in this chapter.

The results for the basic device and dark I-V parameters such as sheet resistance, reverse saturation current, and ideality factor presented in chapter 4.

Chapter 5 discusses the creation of different antireflection (AR) coating layers such as silicon dioxide and porous silicon which are considered as AR coatings in this work. Furthermore, the problems associated with the formation of porous silicon on the front surface of the cells and the optimization of reflectivity of this layer, are discussed in detail.

Chapter 6 contains the illuminated results for the cells with different AR coatings at their front surfaces. The problems associated with the structure of the porous silicon layer, the experiments performed to eliminate the problem, and the results of the treatments are presented in this chapter.

Chapter 7 summarizes the conclusions and contributions of the thesis.

CHAPTER 2

Solar Cell and Porous Silicon Background

Fundamentally, a solar cell is a p-n junction with certain parameters optimized for efficient transformation of energy from the incident solar spectrum into electrical energy supplied to an external electrical load. As background for the experimental work to be described in subsequent chapters, this chapter will:

(1) introduce the basic p-n junction and the p-n junction solar cell;

(2) relate the p-n junction characteristics to the I-V characteristics, which are critical to a solar cell's function;

(3) outline the effect of certain important p-n junction parameter variations on solar cell performance;

(4) review the IBC solar cell structure as a more efficient alternative to standard solar cells;

(5) consider the reflectivity of the light at an air-semiconductor interface and demonstrate techniques to enhance the light trapping property at the interface;

(6) introduce the porous silicon, its optical properties, and its possible application as an antireflection coating for the silicon solar cells;

The ultimate solar cell performance will depend critically on several parameters such as: series and shunt resistances, reverse saturation current, open circuit voltage, short circuit current, and antireflection coating. Potential effects on each of these critical parameters will be highlighted throughout this chapter, since they will be the subject of critical measurements made in later chapters.

2.1 P-N JUNCTION FORMATION

Figure 2.1 shows the p-n junction in which one region of the single crystal semiconductor material is uniformly doped with acceptor impurity atoms to form a p-region and the adjacent region is uniformly doped with donor atoms to form an n-region. The interface separating the n- and p- regions is referred to as the metallurgical junction.

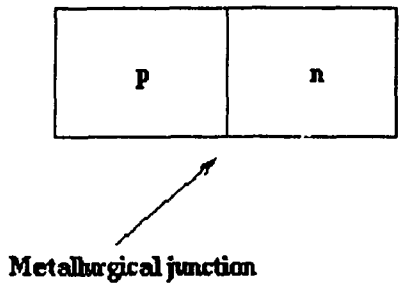


Figure 2.1: Simplified geometry of a p-n junction.

At any T >> 0 ^{o}K, at the metallurgical junction the large carrier concentration gradients at the junction cause carrier diffusion. The majority carrier holes in the p-region will begin diffusing into the n- region and majority carrier electrons in the n-region will begin diffusing into p-region causing a diffusion current in the bulk. As holes diffuse from the p- region, negatively charged acceptor ions will be left behind and similarly, as electrons diffuse from the n- region, positively charged donor ions will be left behind. Consequently, a negative space charge forms on the p-side of the metallurgical junction and a positive space charge forms on the n-side of the metallurgical junction. This space charge region creates an electric field that is directed from the positive charge toward the negative charge as illustrated in the figure 2.2.

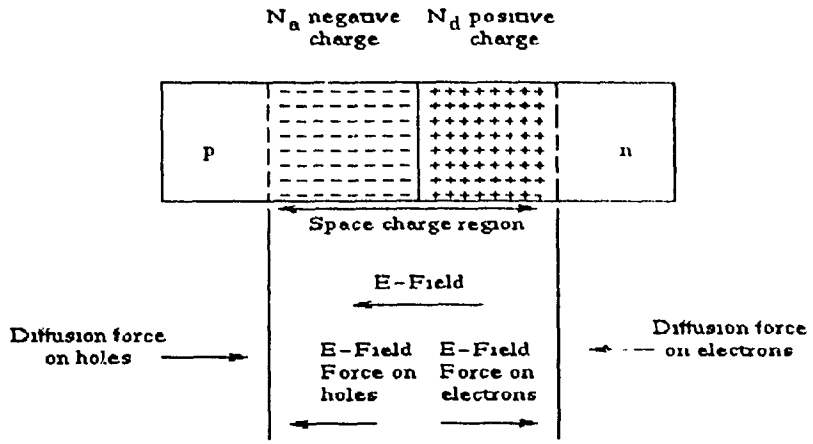


Figure 2.2: The space charge region, the electric field, and the forces acting on the charge carriers.

The electric field is in the direction opposite to the diffusion current for each type of charge carrier. In the presence of this field, minority carriers on either side of the junction are forced to flow across it into the other region. This flow of minority carriers creates a drift current component across the junction which is in a direction opposite to that of the diffusion current. Under equilibrium conditions (i.e., no thermal gradients and no applied bias), the magnitude of the electric field grows until the drift current exactly equals the diffusion current and the net current flow across the junction will become zero.

A solar cell is a pn junction with no voltage directly applied across the junction. The following figure shows a pn junction with a resistive load. Incident photons create electron-hole pairs in the space charge region. These photogenerated carriers are swept out by the electric field in this region and produce a photocurrent I_l in the reverse-bias direction and causes a voltage drop across the resistive load which forward biases the pn junction. Therefore, the net current in the reverse bias direction is $I=I_l-I_F$.

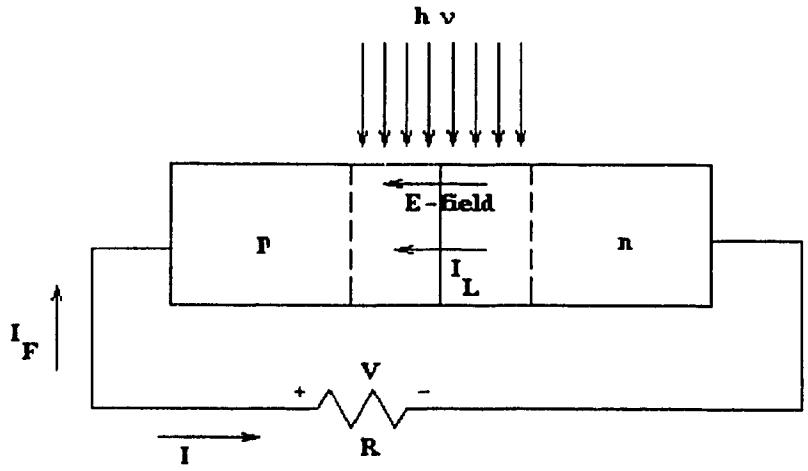


Figure 2.3: A pn junction solar cell with a resistive load.

2.2 I-V CHARACTERISTICS

The idealized equivalent circuit of a solar cell under solar irradiation is shown in figure 2.4 [14], where a constant current source, I_l, is in parallel with the junction.

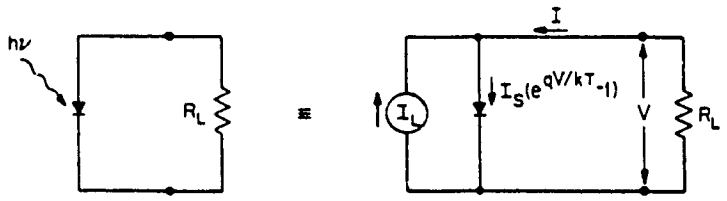


Figure 2.4: Idealized equivalent circuit of a solar cell.

The ideal I-V characteristic of solar cell is given by [14]

$$:I = I_s\left(e^{\frac{qV}{AkT}} - 1\right) + I_l \qquad (2.1)$$

where, I is current through load resistance, R_l, I_s is reverse saturation current of the junction, I_l is the source current resulting from the creation of excess carriers by the solar radiation, V is operating voltage, q is electron charge (1.6×10^{-19} C; 1 eV), k is Boltzmann's constant (8.62×10^{-5} eV/^{0}K), T is temperature [^{0}K], and A is junction quality factor. A is a function of applied voltage and recombination centres within the depletion region. As recombination rate within the depletion region increases due to the trap centres, the value of A becomes larger [3] and its value decreases as the applied voltage increases. The value of A is equal to 1 for an ideal p-n junction. For the non-ideal but still a good junction, the value of A will be between 1 and 2. The junction with an ideality factor greater than 2, has many trap centres within the depletion region.

Figure 2.5 [1] shows the light and the dark I-V curves for an ideal solar cell.

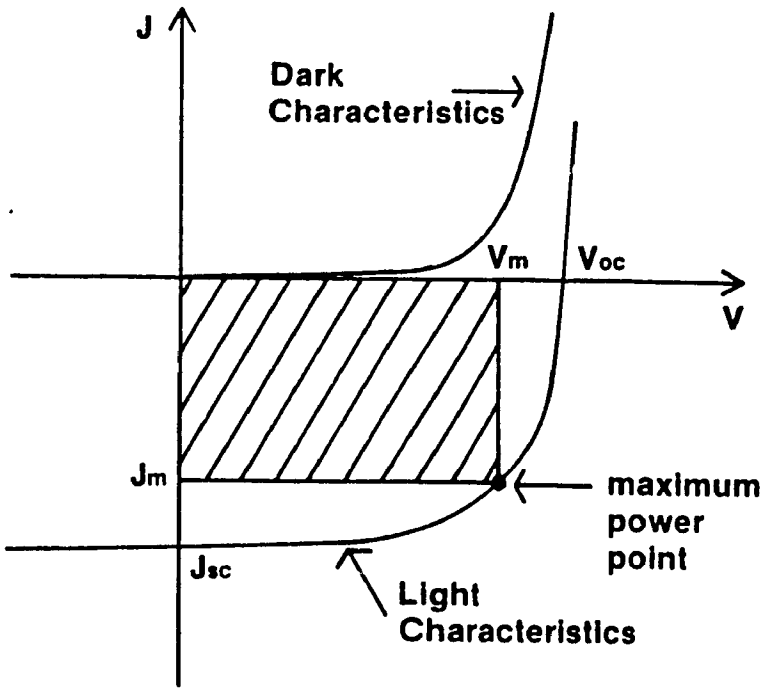


Figure 2.5: The dark and light I-V characteristics for an ideal solar cell.

The I-V curve under dark conditions assumes the shape of an ideal diode characteristic in the first quadrant of the I-V graph. Under illumination, the curve is translated downward by the magnitude of the light-generated current, $I_l=I_{sc}$, and passes through the fourth quadrant as shown in the figure 2.5. Hence, power can be extracted from the device under illumination. The intersection of the curve with the current and voltage axes correspond to the short-circuit current and open-circuit voltage respectively. Also, there exists a bias point on the illuminated I-V curve at which the cell develops a maximum power, P_{max}:

$$P_{max} = V_m I_m \tag{2.2}$$

where,V_m is voltage at maximum power point and I_m is current at maximum power point. The shaded region in the figure is the maximum power rectangle that represents the maximum power which can be delivered by a solar cell.

Mathematically, the short-circuit current and the open circuit voltage can be found by setting V and I equal to zero, respectively, in equation (2.1). The ideal I-V characteristic of the diode is as follows:

at V=0,

$$I = I_{sc} = -I_l \tag{2.3}$$

and at I=0,

$$V_{oc} = \frac{AkT}{q} Ln\left(\frac{I_l}{I_s} + 1\right) \tag{2.4}$$

Figures 2.6 [21] and 2.7 [21] show the effect of light intensity on the short circuit current and the open circuit voltage of a silicon solar cell. The typical value for the open circuit voltage is about 0.6 v for the silicon cell.

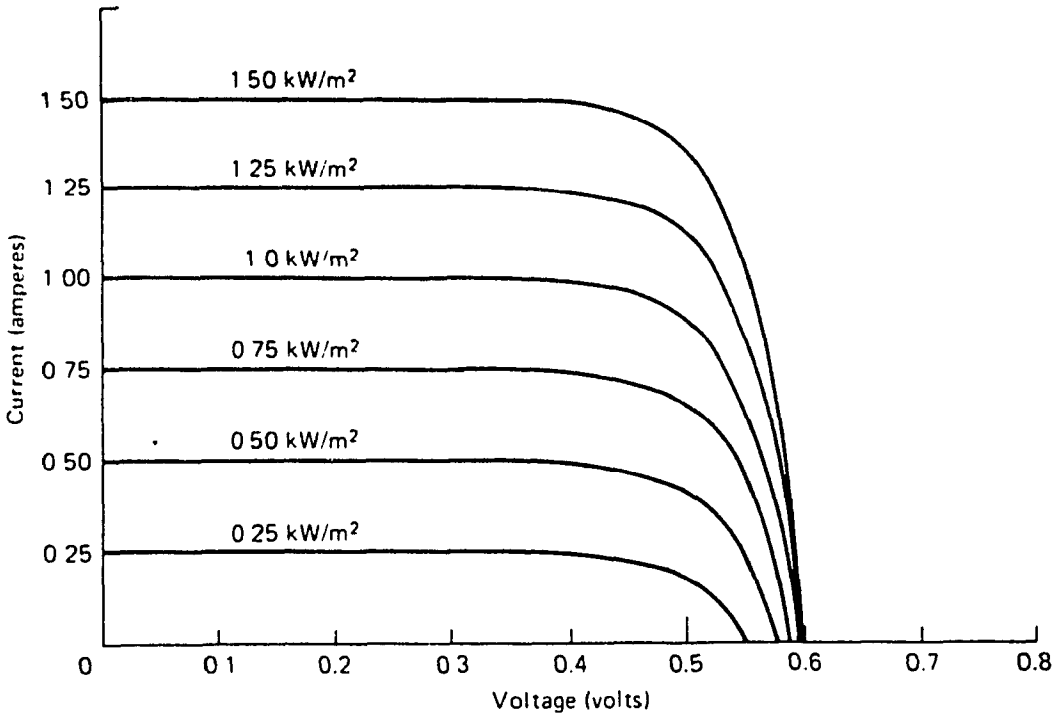


Figure 2.6: The effect of light intensity on the short circuit current and open circuit voltage.

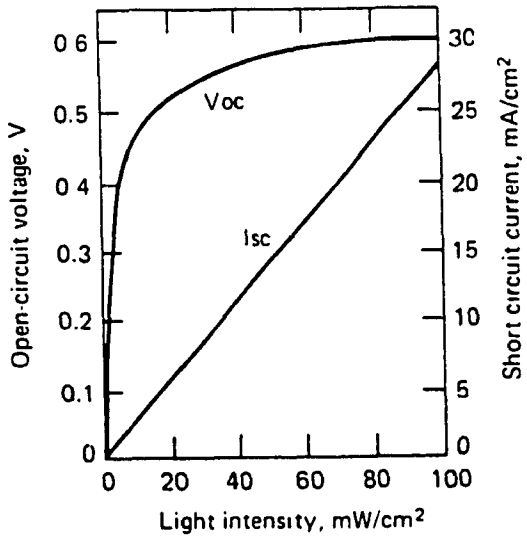


Figure 2.7: Open circuit voltage and short circuit current versus light intensity.

While equation (2.4) suggests at first that V_{oc} increases with the diode quality factor, A, this is actually not the case. Reverse saturation current, I_s, usually increases so rapidly as A increases, that a maximum V_{oc} for given I_l occurs only for A = 1 [5]. However, open circuit voltage,V_{oc}, can be maximized by minimizing I_s.

2.2.1 The origin of reverse saturation current

There are two processes responsible for generation of reverse saturation current across the junction under the reverse bias condition:

- thermal generation of electron-hole pairs in the neutral regions, within a diffusion length.
- thermal generation of electron-hole pairs within the depletion region

The first process contributes a diffusion current component and the second one contributes a generation current component. The magnitude of the reverse saturation current density J_s, is [22].

$$J_s = \left(qp_{no}\sqrt{\frac{D_p}{\tau_p}} + qn_{po}\sqrt{\frac{D_n}{\tau_n}} \right) + \frac{qn_i W}{\tau_e} \tag{2.5}$$

where, p_{no} is the equilibrium concentration of holes in the n-region [$=n^2_i/N_d$], n_{po} is equilibrium concentration of electrons in the p-region [$=n^2_i/N_a$], D_p is hole diffusion constant in the n-region, D_n is electron diffusion constant in the p-region, τ_p is hole life time in the n-type bulk region, τ_n is electron life time in the p-type bulk region, W is the depletion region width, N_d is the donor dopant concentration, N_a is the acceptor dopant concentration, n_i is intrinsic carrier concentration, and τ_e is average carrier life time which is equal to $(\tau_p+\tau_n)/2$.

Equation (2.5) is derived for an ideal diode. In the case of a real p-n junction where doping levels, N_a and N_d are not uniform with depth, or there are recombination processes taking place at the surface of semiconductor, then the above equation will change to [3,19]

$$:J_s = \left(qp_{no}\sqrt{\frac{D_p}{\tau_p}}X + qn_{po}\sqrt{\frac{D_n}{\tau_n}}Y\right) + \frac{qn_iW}{\tau_e} \tag{2.6}$$

where

$$X = \frac{S_p\cosh\frac{W_n}{L_p} + \frac{D_p}{L_p}\sinh\frac{W_n}{L_p}}{\frac{D_p}{L_p}\cosh\frac{W_n}{L_p} + S_p\sinh\frac{W_n}{L_p}}$$

and

$$Y = \frac{S_n\cosh\frac{W_p}{L_n} + \frac{D_n}{L_n}\sinh\frac{W_p}{L_n}}{\frac{D_n}{L_n}\cosh\frac{W_p}{L_n} + S_n\sinh\frac{W_p}{L_n}}$$

W_n is the distance from the surface to the edge of the depletion region in the n-region, W_p is the distance from the surface to the edge of the depletion region in the p-region, L_p is the hole diffusion length in the n-region, L_n is the electron diffusion length in the p-region, and S_p and S_n are minority carrier surface recombination velocities, corresponding to minority carrier recombinations at the surface in the n- and p-regions respectively and will be defined in the section 2.3.2.2. In the case of an

n^+-p junction, n_{po} is much greater than p_{no} and equation (2.6) reduces to

$$J_s = qn_{po}\sqrt{\frac{D_n}{\tau_n}}Y + \frac{qn_iW}{\tau_e} \tag{2.7}$$

Eventhough every p-n junction and diode has reverse saturation current, from the point of view of a solar cell this is an area of concern. To minimize the value of this parameter and thus, maximize the open circuit voltage, V_{oc}, the values of S_n, S_p, n_{po} and p_{no} in the equation (2.6) should be minimized. The values of p_{no} and n_{po} can be minimized by using initial materials with high concentration of donors and acceptors, respectively (~$10^{16}cm^{-3}$). The surface recombination velocities S_n and S_p will be minimized by making contact between the silicon and the aluminum through small areas, as will be discussed later in this chapter.

2.2.2 Effects of series and shunt resistances on the cell performance

The ideal diode circuit in figure 2.4 is modified to include the series resistance, R_{ser}, and shunt resistance, R_{sh}, in the circuit. Under this condition, the cell characteristic is given by [3]:

$$I = I_s\left(e^{\frac{q(V-IR_{ser})}{AkT}} - 1\right) - I_l + \frac{V-IR_{ser}}{R_{sh}} \tag{2.8}$$

The sources of shunt resistance, R_{sh}, are regions of reduced junction barrier height (due to presence of trap centres) and for a good quality junction, R_{sh} must be quite high [5,16]. The sources of series resistance, R_{ser}, are high contact resistance or

non-ohmic contacts, the bulk resistivity of the base layer, n- and p- layers, and finally the resistance of the metal path itself [1].

Figure 2.8 [21] shows the I-V characteristics of a solar cell under illumination, indicating the effects of changing series and shunt resistances.

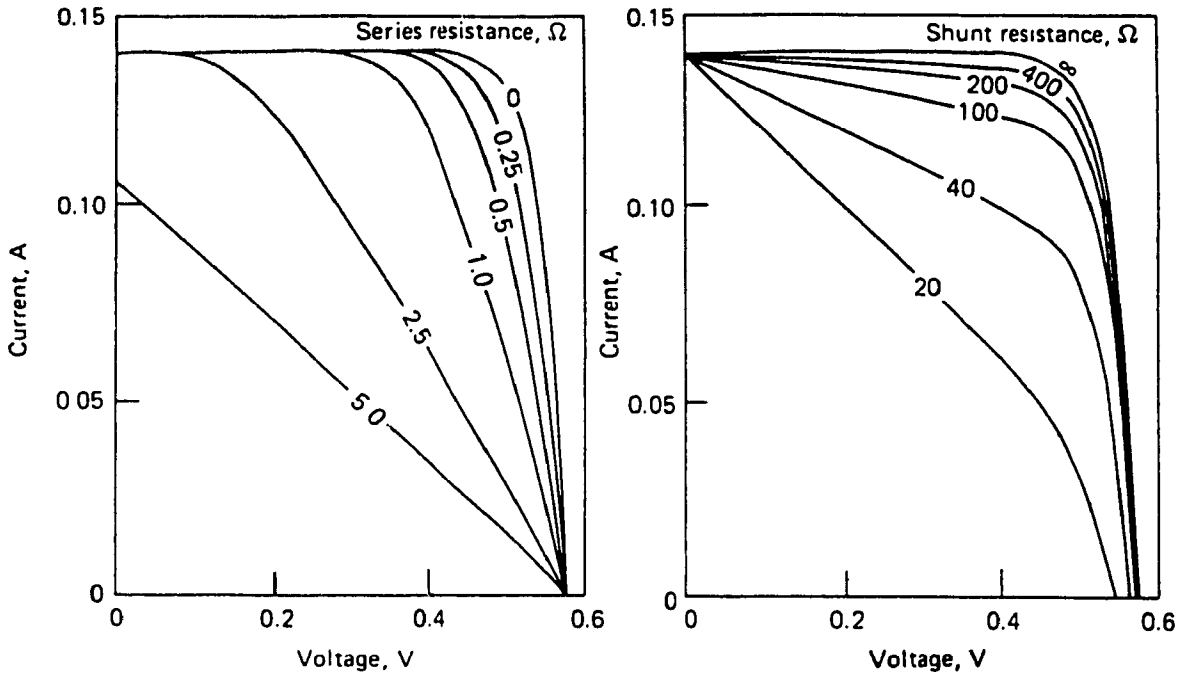


Figure 2.8: The I-V curve response to the changes in series and shunt resistances.

From figure 2.8 it can be deduced that the best case is obtained with the series resistance, R_{ser}, equal to zero and the shunt resistance, R_{sh}, equal to infinity. Non-ideal values of these resistances leads to the lowering of useful voltages and currents, and thus, the limiting of the overall device performance. The value of the series resistance can be minimized by using highly doped wafers, making ohmic contacts between the metal and semiconductor, and depositing a thick layer of metal. However, from figure 2.8 and also equation (2.8), it can be seen that the impact of shunt

resistance on device performance will be small for values of shunt resistance as low as 400 ohms [23,24]. Therefore, unless $R_{sh} < 400\ \Omega$, the last term in equation (2.8) can be neglected and the cell characteristic will become

$$I = I_s\left(e^{\frac{q(V-IR_{ser})}{AkT}} - 1\right) - I_l \tag{2.9}$$

or

$$V = \frac{AkT}{q} Ln\left(\frac{I+I_l}{I_s} + 1\right) + IR_{ser} \tag{2.10}$$

and the cell output power can be found from the following equation

$$:P = |IV| = I\left(\frac{AkT}{q} Ln\left(\frac{I+I_l}{I_s} + 1\right) + IR_{ser}\right) \tag{2.11}$$

From equation (2.11), one can realize that even small values of R_{ser} (~1 Ω) can reduce the value of out put power. Figure 2.9 [23] is a plot of equation (2.11) which shows the relative maximum available power as a function of R_{ser}.

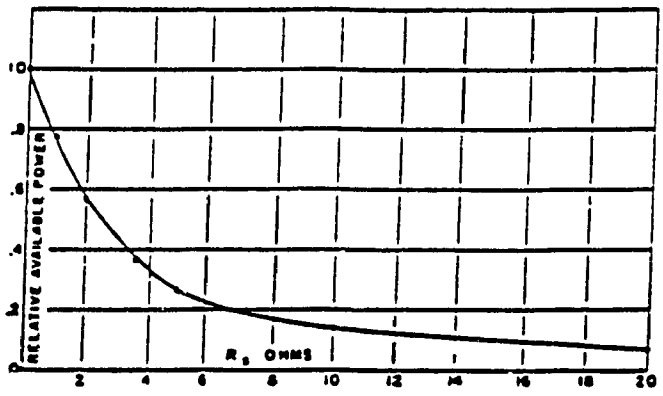


Figure 2.9: Relative maximum available power as a function of R_{ser}

By looking at the graph, one realizes that even series resistances with small values can reduce the relative power developed by a cell. Comparing figure 2.5, the light I-V curve for an ideal solar cell, with figure 2.8 which shows the light I-V curve for solar cells whose series resistances are not zero, one comes to the conclusion that the characteristic of a practical cell with a finite series resistance have a more rounded shape. Therefore, the maximum power point which is defined by the equation (2.2), is very much dependent on the shape of the illuminated I-V curve, in other words, the maximum power point is a function of both the series and the shunt resistances. Referring once again to figure 2.5. the product of V_m and I_m which give the maximum power point, is normalized to the product $V_{oc}I_{sc}$ and gives the fill factor, FF, which is a measure of "squareness" of the I-V curve. Considering figure 2.8, one realizes that the values of series and shunt resistances reduce the fill factor dramatically.

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \tag{2.12}$$

Fill factor is plotted in figure 2.10 [24] as a function of open circuit voltage, V_{oc}, for different values of A.

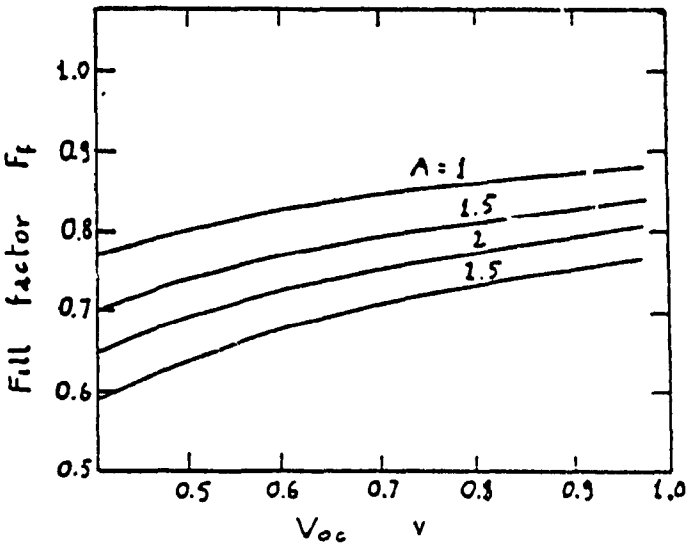


Figure 2.10: Fill factor versus open circuit voltage for different values of A.

Therefore, fill factor, FF, will be maximized if open circuit voltage is maximized. Typical values for fill factor range from 0.6 to 0.8 [3]. As it was discussed earlier, the fill factor is a measure of "squareness" of the I-V curve, on the other hand, it was shown that non-ideal values of shunt and series resistances would result in a rounded shape for the I-V characteristic of the solar cell under light. Therefore, the value of the fill factor will be very dependent on the value of series and shunt resistances and one should maximize the value of this parameter by optimizing the fabrication parameters for a low value of series resistance and a large value of shunt resistance.

The solar cell conversion efficiency at the maximum power point is defined by [19]

$$\eta = \frac{P_m}{P_{in}} \tag{2.13}$$

By substituting the value of P_m from equations (2.2) and (2.12), the conversion efficiency can be written as

$$\eta = \frac{FFV_{oc}I_{sc}}{P_{in}} \tag{2.14}$$

Therefore, efficiency of a cell is very much dependent on its fill factor and open circuit voltage and to maximize that, the reverse saturation current, I_s, which affects the open circuit voltage, the series and shunt resistances, R_{ser} and R_{sh}, which affect the fill factor must be optimized through proper processing.

This experimental work will in particular consider the process parameters such as surface concentration, junction depth, and surface recombination velocity which will result the optimized values for the reverse saturation current, series and shunt resistances.

2.2.3 Effect of temperature on the cell performance

The drop of solar cell efficiency with respect to temperature is shown in figure 2.11 [21]. Also figure 2.12 [21] shows that the open circuit voltage decreases as temperature of the cell increases.

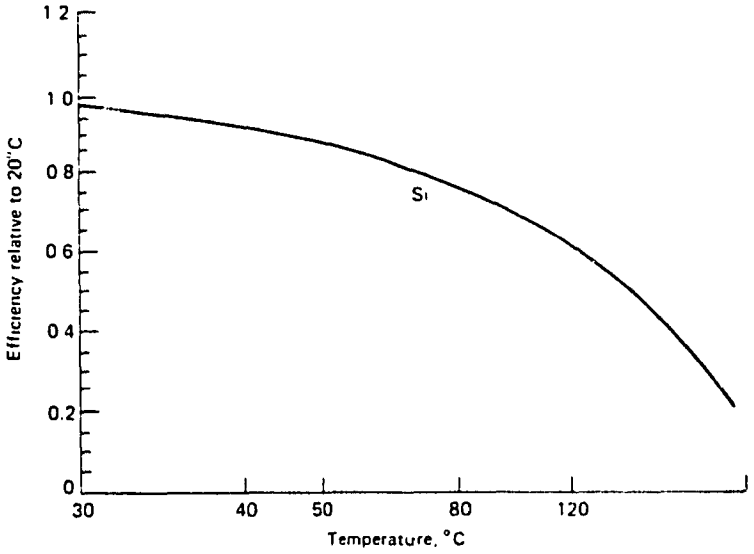


Figure 2.11: Si solar cell efficiency versus temperature.

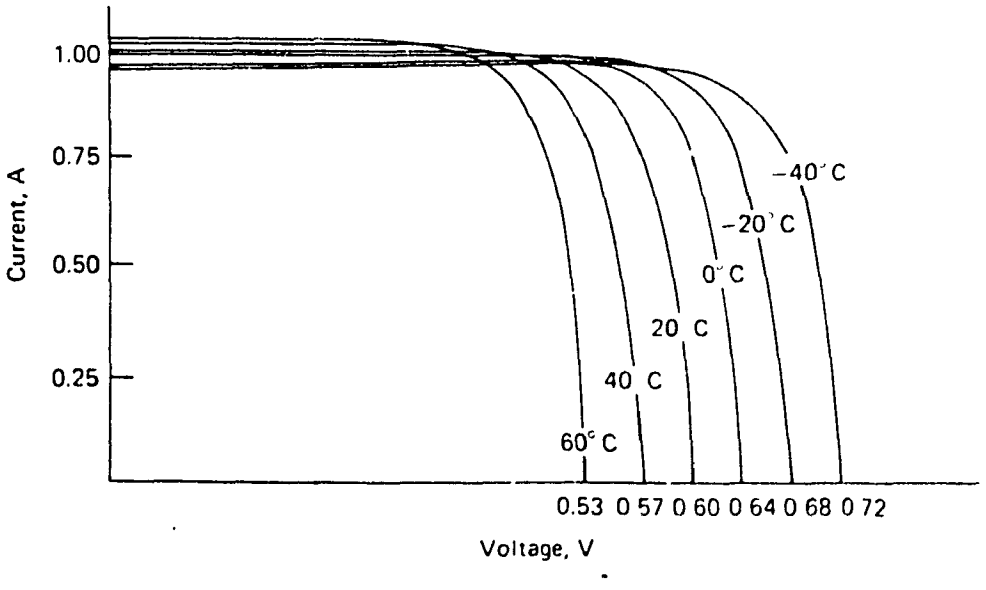


Figure 2.12: Change in open circuit voltage with variation in temperature.

Open circuit voltage is a function of reverse saturation current as shown in equation 2.4 and reverse saturation current itself is a function of the thermal equilibrium minority carrier concentration n_{po} and p_{no} in equation 2.6. Therefore, as temperature increases, the minority carrier concentrations will increase according to the following equations [15]

$$P_{no} = \frac{n_i^2}{N_d} = \frac{N_c N_v e^{\frac{-E_g}{kT}}}{N_d}, n_{po} = \frac{n_i^2}{N_a} = \frac{N_c N_v e^{\frac{-E_g}{kT}}}{N_a} \qquad (2.15)$$

where, N_c is the effective density of states in the conduction band in cm^{-3} and N_v is the effective density of states in the valence band in cm^{-3}. In case of silicon, N_c and N_v are equal to 2.8×10^{19} cm^{-3} and 1.04×10^{19} cm^{-3} respectively. Therefore, an increase in minority concentration causes an increase in reverse saturation current (equation 2.6) and consequently, open circuit voltage will decrease which results in lowering cell efficiency. Thus, to keep the values of the open circuit voltage and the efficiency unchanged, the heat must be taken away from the cell substrate.

2.3 Optical Considerations

2.3.1 Sunlight Reaching the Earth

Any discussion of solar energy and solar cells should begin with a look at the energy source, which in this case is the sun. The sun has a mass of 10^{24} tons, a diam-

eter of 865,400 miles and radiates energy at a rate of approximately $3.8x10^{20}$ mega watts (MW) [2]. Above the earth's atmosphere, sunlight carries over 1300 watts (W) of power per square meter, but not all of this reaches the earth's surface as it is shown in figure 2.13 [25].

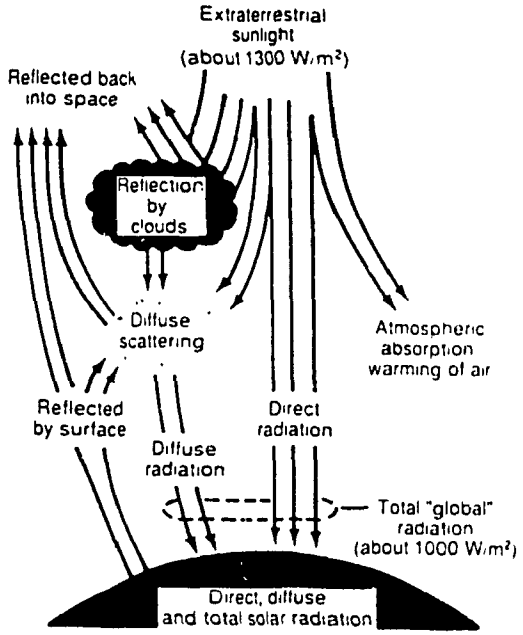


Figure 2.13: Part of the sunlight that reaches the earth's surface.

As it is shown in figure 2.13, the sunlight reaching the earth's surface has two components: (i) direct beam and (ii) a diffuse beam. The diffuse light is the portion of the sunlight that has been refracted or scattered in the atmosphere before it reaches the earth's surface. Under perfect, cloudless conditions, about 10% of sunlight is diffused and the rest is the direct beam. Passing through the atmosphere,

many parts of the sun's spectrum are attenuated. For example, X-rays are almost totally absorbed before reaching the ground, a good percentage of ultraviolet radiation is absorbed by the ozone, much infrared light is absorbed by water vapor and carbon dioxide. As a result of all these reflections, refractions, and absorptions, sun light loses 300 W during its passage through the atmosphere and at noon on a cloudless day, sunlight provides only 1000 W of power on each square meter of the earth's surface. Table 3 [26], illustrates the solar spectral irradiance under air-mass-zero and air-mass-one conditions as a function of wavelength.

Wavelength (μm)	Energy (eV)	Solar Spectral Irradiance AM0 (mw/cm^2)	Solar Spectral Irradiance AM1 (mw/cm^2)
- 1.15	0 - 1.08	31.77	25.24
1.15 - 1.00	1.09 - 1.24	9.51	8.41
1.00 - 0.90	1.25 - 1.38	8.29	6.02
0.90 - 0.80	1.39 - 1.55	9.93	8.35
0.80 - 0.70	1.56 - 1.78	12.37	8.05
0.70 - 0.60	1.79 - 2.07	15.15	13.25
0.60 - 0.50	2.08 - 2.49	17.70	14.30
0.50 - 0.40	2.50 - 3.11	18.77	15.10
0.40 - 0.30	3.12 - 4.14	10.17	7.91
0.30 - 0.20	4.15 - 6.22	1.63	0.37
0.20 - 0.00	6.22 - ∞	0.01	0.00
All Wavelengths	0 - ∞	135.30	107.00

TABLE 3. The solar spectral irradiance under air-mass-zero and air-mass-one conditions as a function of wavelength.

where the air-mass-zero and air-mass-one correspond to the energy received from the sun per unit time and per unit surface, outside and inside the atmosphere, respectively. The "air-mass-m" terminology is a common method of describing relative energy levels. It is the ratio of the actual length the solar beam traverses relative to the depth of the atmosphere with the sun in its zenith position. Referring to the figure 2.14 [27], the zenith path, zo is defined as unit air mass and the air mass, m, is defined as the ratio of so/zo, or reciprocal of cosine of angle z, where z is the sun zenith angle.

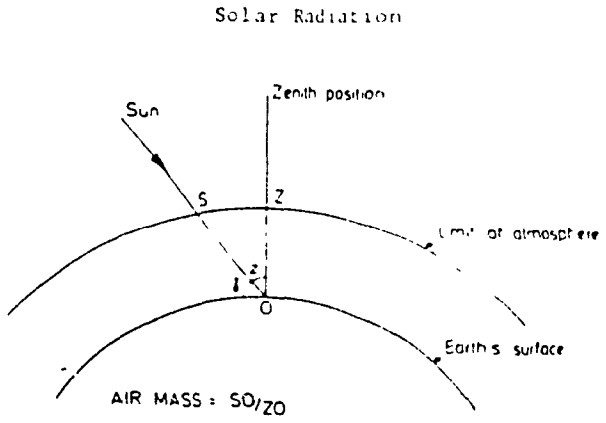


Figure 2.14: Definition of air mass.

2.3.2 Bulk absorber material

As photons strike the silicon surface, some are reflected back and the rest will continue into the silicon. Most of those will be absorbed and will interact with the bulk silicon atoms. The absorption of photons by the absorber material depends on the absorption coefficient of the material, α, which is a function of wavelength and of the material itself. Figure 2.15 [28], shows the room temperature absorption coefficient of silicon versus wavelength.

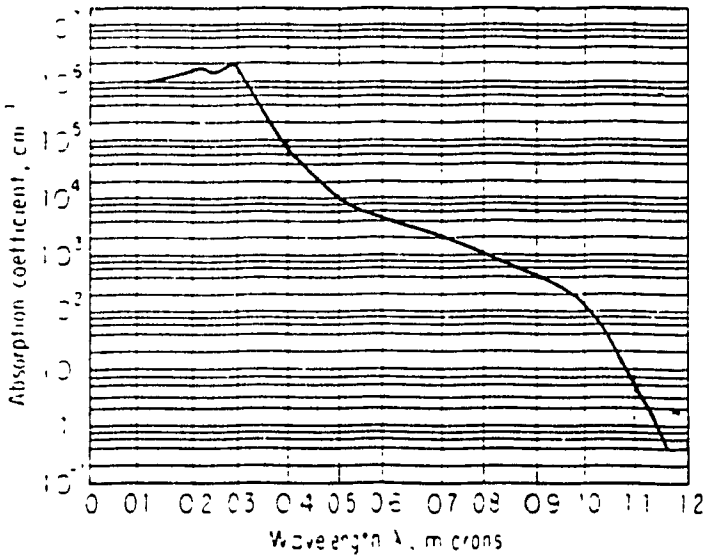


Figure 2.15: Room temperature absorption coefficient vs. wavelength for Si.

From this figure, it is clear that, as the wavelength of a photon decreases, the absorption coefficient of silicon increases. That is, photons with higher energies will be absorbed closer to the surface.

If the photon flux incident at the surface of semiconductor absorbing material is shown by $\Gamma_o(\lambda)$ (photons cm^{-2} sec^{-1}) and the reflection of some photons at the surface is neglected, then the remaining flux at the distance x beneath the surface is given by [3]

$$\Gamma(\lambda, x) = \Gamma_o(\lambda)\, e^{-\alpha(\lambda)x} \tag{2.16}$$

where $\Gamma(\lambda,x)$ is photon flux at distance x beneath the surface in cm^{-2} sec^{-1}, $\alpha(\lambda)$ is the absorption coefficient of the absorber material in cm^{-1}, and λ is wavelength of photon in cm. The following example gives a better understanding about the absorption coefficient of silicon at two wavelengths, 0.3 and 1 micron, and the thickness of substrate needed to absorb 99% of photons having those wavelengths, with the knowledge that the absorption coefficients of silicon at those wavelengths are available from Fig.2.16, can be calculated as follows:

$$\frac{\Gamma(\lambda_{0.3}, x)}{\Gamma_o(\lambda_{0.3})} = 0.01 = e^{-1.7 \times 10^6 x}, x = 0.027\mu m$$

$$\frac{\Gamma(\lambda_{1.0}, x)}{\Gamma_o(\lambda_{1.0})} = 0.01 = e^{-1.3 \times 10^2 x}, x = 354\mu m$$

Knowing that silicon has a bandgap energy of 1.11 eV, one can calculate the wavelength of the photon whose energy is just enough to create photo-carriers, using the following equation

$$E = h\frac{c}{\lambda} \tag{2.17}$$

where, E is photon energy, h is Planck's constant [= 4.14×10^{-15} eV.sec], and c is speed of light [= 3×10^{8} m/sec]. Therefore, photons with wavelength of 1.1 μm or less are useful for silicon solar cells. Figure 2.16 [29], illustrates the spectral response curve which is a typical plot of incremental current density generated by unit irradiance at a particular wavelength as a function of wavelength for a silicon solar cell.

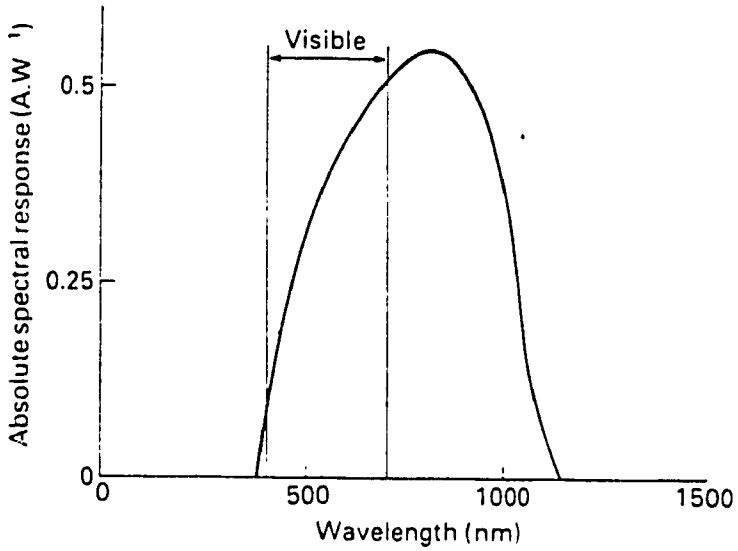


Figure 2.16: Spectral response curve.

Considering the results of the given example and the value of maximum wavelength needed to create photo-carriers, and the fact that photons with wavelengths longer than 1 micron have a very low probability to get absorbed by silicon due to its very low absorption, one comes to the conclusion that to absorb 99% of photons within the silicon substrate, a substrate thickness of 350 microns will be sufficient.

2.3.2.1 Photo-induced carriers inside the substrate

Once photo-carriers are generated within the substrate, they diffuse randomly and the following processes take place

- some of photocarriers will diffuse across the substrate and become separated by the electrostatic field inside the depletion region.
- some of the holes and electrons will directly recombine with each other or they will be trapped by the impurities and defect centres which are present within the substrate.
- finally, those photogenerated carriers which are close to the surface, will recombine with the dangling bonds present at the surface.

Among these processes, only the first process contributes to the output current. Therefore, for solar cells having the IBC structure, the use of high concentrated light is necessary to increase the concentration of photo-carriers and hence, increase the collection probabilities. Float zone, high lifetime wafers, which are very pure, may be used in the IBC structure to further enhance the collection probability. In a high lifetime wafer, the diffusion length (average length travelled by a minority carrier before it recombines with a majority carrier) of minority charge carriers will be longer and thus, the chance of being recombined before reaching the depletion region will be lower. In the case of an n-type substrate, the hole diffusion length is defined by the following equations [15]:

$$L_p = \sqrt{D_p \tau_p} \tag{2.18}$$

$$D_p = \frac{kT\mu_p}{q} \tag{2.19}$$

where L_p is minority carrier hole diffusion length in cm, D_p is minority carrier hole diffusion constant in cm^2/sec, τ_p is minority carrier hole lifetime in sec, k is Boltzmann's constant (=8.62×10^{-5} eV/°K), T is temperature in °K, μ_p is minority carrier hole mobility in $cm^2/V.sec$, and q is electron charge (=1.6×10^{-19} C).

Figure 2.17 [18] shows the physical layout of the IBC solar cell structure. In this design, for a good cell performance, the diffusion lengths (L_n and L_p) should be comparable with the substrate thickness. Any process to which the solar cell is submitted must not decrease the diffusion lengths. However, no matter how careful one is to maintain the diffusion lengths, The phenomenon of surface recombination is another limiting factor in the cell performance.

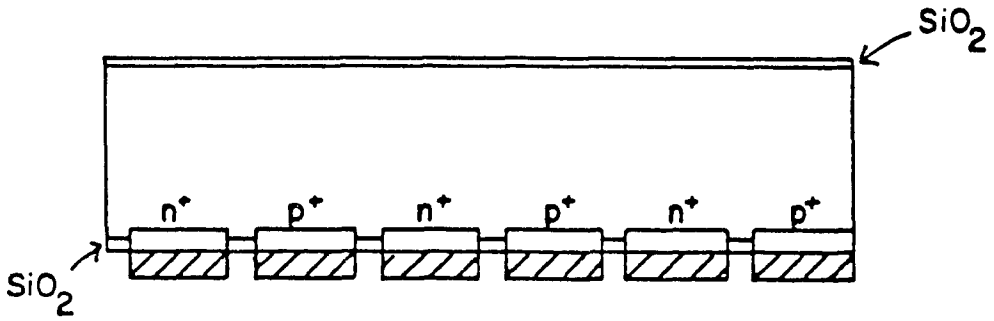


Figure 2.17: The physical layout of the IBC solar cell.

2.3.2.2 Surface recombination velocity (S)

Minority carrier recombination at the surface due to the presence of dangling bonds gives rise to a surface recombination velocity. Within the silicon substrate, each silicon atom forms a covalent bond with four of its nearest neighbors. However, at a free surface of an ideal silicon crystal structures, atoms can have only two or

three bonds satisfied, depending on the orientation of the silicon surface. Even if surface reconstruction changes the bonding configurations at the surface, there will remain strained and dangling bonds. These become trap centres for minority carriers [30]. The surface recombination velocity, (S), is defined by the following equation [31]:

$$S = \sigma v_{th} N_{st} \tag{2.20}$$

where σ is the capture cross section of trap centres in cm^2, v_{th} is thermal velocity of carriers [= 10^7 cm/sec] at room temperature, and N_{st} is number of surface trapping centres per unit area. In order to reduce the surface recombination velocity, the surface must be passivated and it has been shown that a silicon dioxide layer substantially decreases the number of trapping centres at the surface [32]. Figure 2.18 shows the Si/ SiO_2 interface [33]

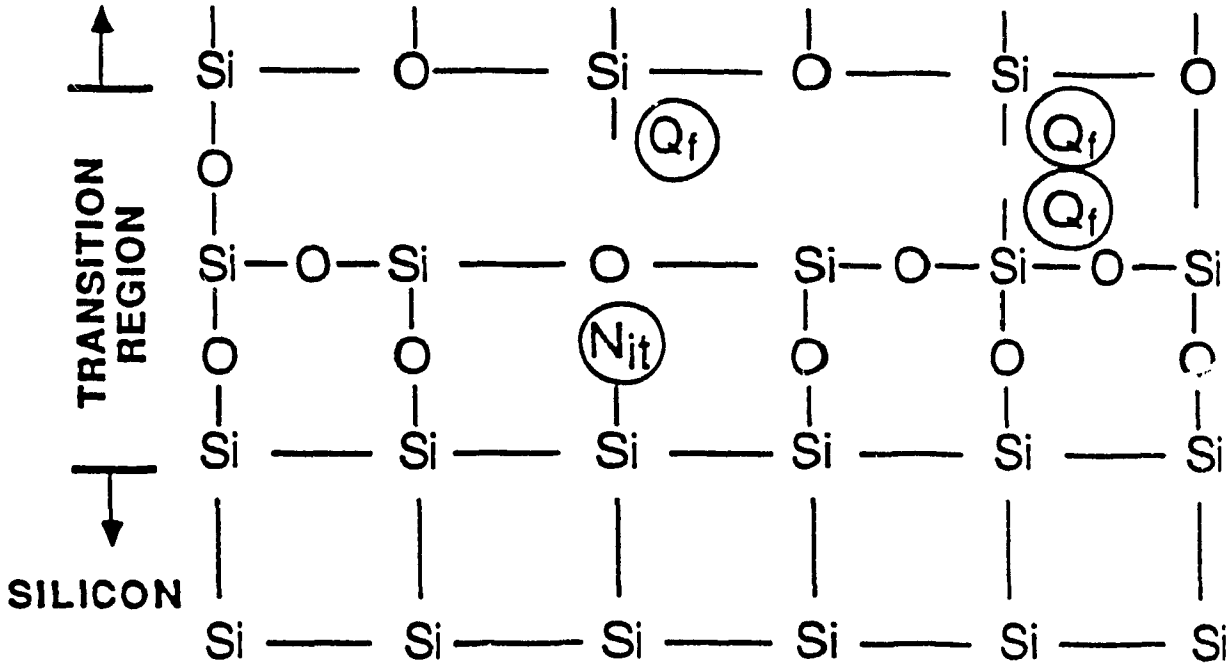


Figure 2.18: 2D sketch of the Si/SiO_2 interface.

It is shown that an Al/Si interface has a surface recombination velocity that approaches the maximum attainable value for silicon, 10^6 cm/sec [16]. On the other hand, a high-quality thermally-grown SiO_2/Si interface usually has a surface recombination velocity of 10^2 to 10^4 cm/sec [3]. Therefore, growth of a high quality thermal oxide over the entire surface of the device before metallization can reduce the surface recombination velocity. Reverse saturation current will therefore be decreased. However, some silicon atoms are not bonded by the oxide. Those Si atoms which lie at the Si/SiO_2 interface are referred to as interface states, N_{it}, and those which are located inside the oxide very close to interface, are called fixed oxide charges, Q_f [33]. The density of interface charges, N_{it}, can be reduced by a post metallization anneal in a mixture of hydrogen and nitrogen ambient at 450 ^oC for 30 minutes in which hydrogen atoms passivate the interface defects [16].

As discussed above, the Al/Si interface has the highest value of surface recombination velocity. In this work we will attempt to keep the value of the surface recombination velocity as low as possible by minimizing the silicon regions which are in direct contact with the aluminum.

2.3.3 Antireflection coatings

Silicon has a high ref active index for all the wavelengths as shown in figure 2.19 [28].

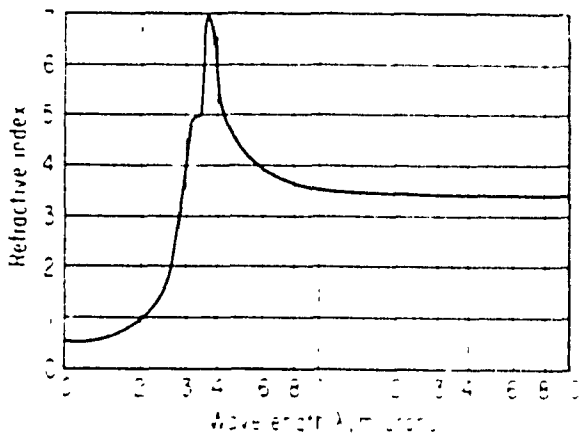


Figure 2.19: Refractive index of silicon at room temperature.

A considerable portion of light incident at the surface of Si will be reflected away rather than transmitted. The reflectivity at an air-semiconductor interface is given by [5,28]

$$R = \frac{(n_s - 1)^2}{(n_s + 1)^2} \tag{2.21}$$

where, n_s is refractive index of the semiconductor. As a result, an anti-reflection coating layer is necessary at the surface to minimize the reflectivity of the light. In this work porous silicon is chosen as an anti-reflection coating to be explored experimentally. The next section (2.5) is a complete description of formation and properties of porous silicon.

2.4 Criteria for an efficient solar cell

Based on the preceding discussions, here are a summary of criteria for a good solar cell, indicating the criteria for the required p-n junction.

- low reverse saturation current (I_s) in the range of microampere or lower, otherwise the open circuit voltage will become low.
- ideality factor (A) between 1 and 2 (the closer to 1, the better), it is acceptable up to 2 and the values higher than 2 will result in high reverse saturation current.
- series resistance (R_s) as low as possible (not higher than 1 Ω), series resistances higher 1 Ω will result in low fill factor.
- shunt resistance (R_{sh}) as high as possible (usually few KΩ or higher), the low value for this parameter, reduces the fill factor.
- fill factor (FF) as high as possible, its typical values are between 60% to 80%.
- surface reflectivity as low as possible, the average reflectivity of commercial solar cells is 10 to 15% (1100 Å SiO_2).

2.5 Porous Silicon

Porous silicon, a nanometer-scale structure of silicon has been known for more than 30 years and was discovered by Uhlir[34] by anodic etching of silicon in concentrated hydrofluoric acid(HF). Figure 2.20 shows a schematic for the apparatus for making porous silicon.

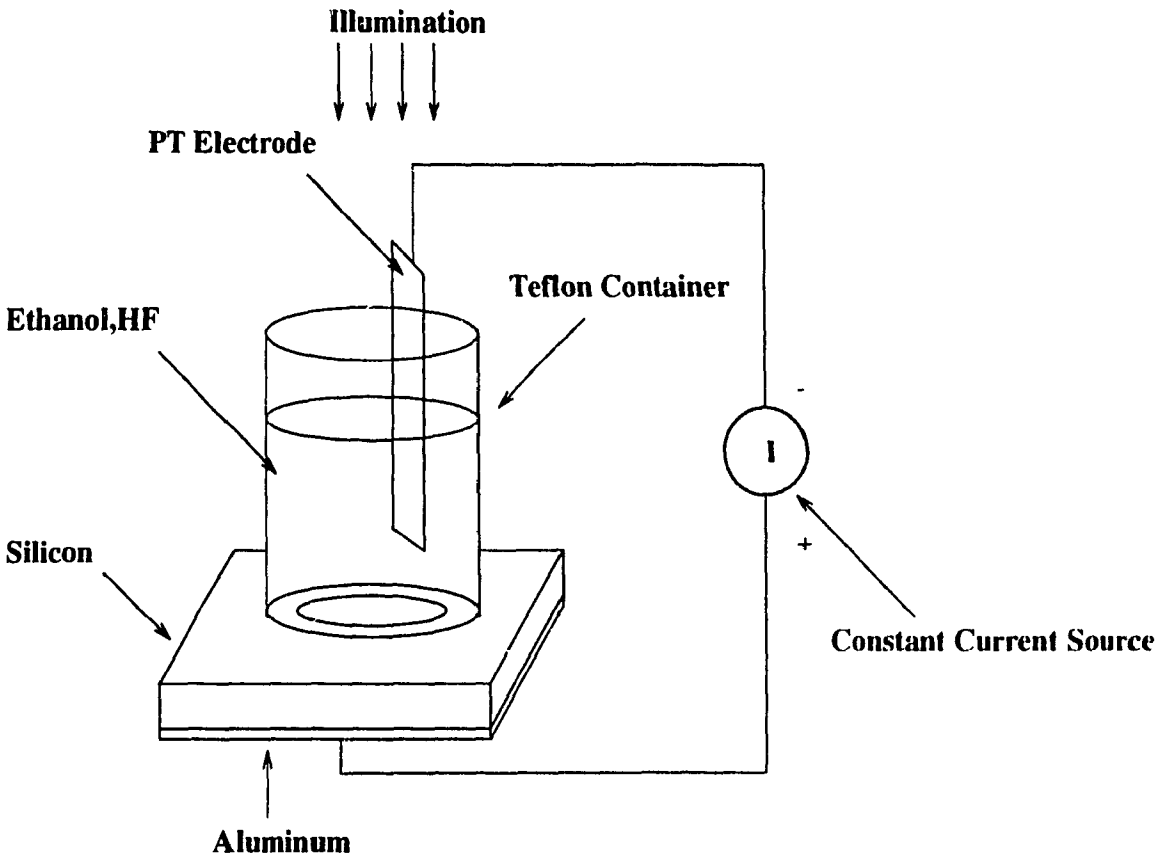


Figure 2.20: Formation of porous silicon layer.

Porous silicon was produced by exposing the surfaces of silicon wafers to the electrolyte solution (HF, Ethanol mixture) contained in a Teflon container and passing a constant current through the electrolyte with the silicon wafer as the anode and a Pt electrode as the cathode. Ohmic contacts were made to the other side of the wafer to facilitate good electrical contact for the electrochemical reaction. Anodic dissolution of silicon will take place in an acidic electrolyte which contains F^- ions[35,36]. This only happens in the presence of holes[36]. For p-type silicon under anodic bias, this condition is always fulfilled and experiments can be done under any light conditions. However, in the case of n-type silicon, because the hole concentration is low, the experiment must be done under light illumination in order to generate

enough holes to make the anodic dissolution of silicon possible [37,38]. Ethanol is added to the electrolyte to obtain porous layers of good crystalline quality[39]. Experiments show that porous silicon produced in an electrolyte solution consisting of only HF, has a non-uniform porous layer thickness and the interface between the silicon and the porous layer is uneven. These defects are due to the hydrogen bubbles formed on the surface of the silicon during the electrochemical reaction. By adding ethanol to the electrolyte, there would be considerable decrease in the size of the hydrogen bubbles and they will remove much easier. This leads to formation of porous silicon layer of good crystalline quality[39]. Fig.2.21 [39,40] shows cross section and top surface of porous silicon layer obtained by Transmission Electron Microscopy (TEM).

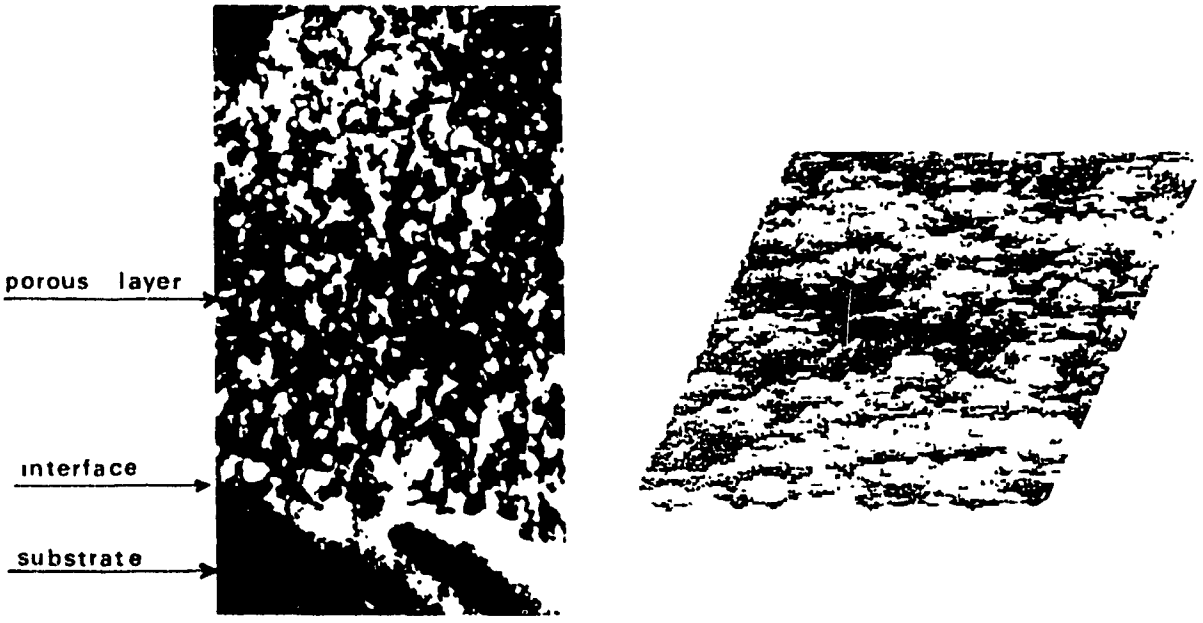


Figure 2.21: Top and cross-sectional TEM image of porous silicon.

As it is seen in these pictures, the surface of porous silicon layer has a highly textured morphology. The use of this material as an antireflection coating to enhance the performance of the silicon solar cells will be discussed later in section 2.5.2.

The porous structure of porous silicon sensitively depends on the doping type and doping level of silicon substrate, the HF concentration, and the anodization current densities used in the etching process [36,41].

The resulting microscopic structure of porous silicon is a topic of many researches since the formation process is still not well understood [42]. Significant attention has recently been directed toward porous silicon due to its visible photoluminescence (the emission of photons due to recombination of electrons and holes created by a photon absorption in a semiconductor). The first visible photoluminescence (PL) in porous silicon was reported by Pickering et al. in 1984 but it was not until 1990 that Canham [43] pointed out the importance of this phenomenon. The strong visible light emission in porous silicon is quite surprising, in view of the fact that bulk crystalline silicon has an indirect band gap at 1.1 eV at room temperature. This indirect band gap would normally result in a very inefficient radiative recombination producing light in the infrared. For crystalline silicon, both optical absorption and emission are very weak in comparison to materials having direct gaps [43]. Figure 2.22 (a) and (b)[37,44] show the PL spectra for porous silicon layer formed on a p- type silicon substrate in various HF concentrations, C_{HF}, at two fixed current densities J=50 and 20mA/cm^2 respectively for the forming time t=8 minutes. The effect of PL property of porous silicon on the silicon solar cells will be discussed later in section 2.5.2.

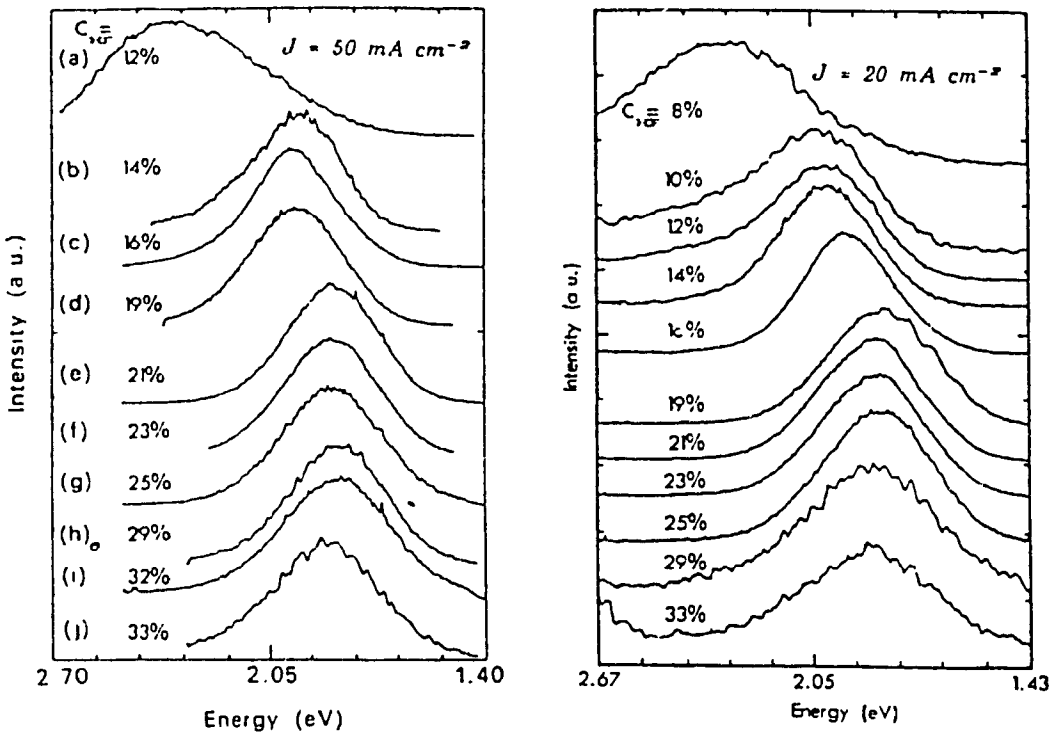


Figure 2.22: Photoluminescence spectra of p- type porous silicon samples formed in various HF concentration, C_{HF}, for t=8 minutes at fixed current densities J = 50 mA/cm^2 and J = 20 mA/ cm^2.

The results of figure 2.22 (a) and (b) are reorganized and illustrated in figure 2.23 (b) and (c) [37,44]. These figures show the photoluminescence peak energies as a function of HF concentration for p type porous silicon samples and figure 2.23 (a) shows the experimental results for n- type porous silicon samples, formed under the same conditions as those for samples in figure 2.22 (a).

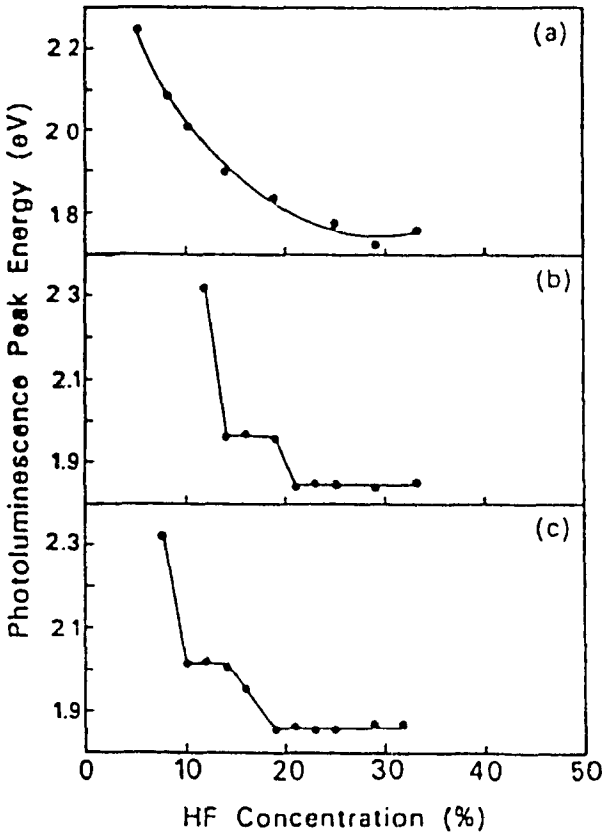


Figure 2.23: The HF concentration dependencies of photoluminescence peak energy for: (a) n- type porous silicon samples formed in the various HF concentration at a fixed current density J = 50 mA/cm^2 for t = 8 min, (b) p- type porous silicon samples made in various HF concentrations at a fixed current density J=50 mA/cm^2 for t=8 min, (c) p-type porous silicon samples formed in various HF concentrations for t=8 minutes at a fixed current density J=20mAcm^2.

From the above figures one can see that a decrease in HF concentration or an increase in current density will shift the photoluminescence peak toward the higher energies. The reason will be discussed in the next section.

2.5.1 Origin of PL in porous silicon

Until now different models have been developed to explain the origin of light emission in porous silicon[43] but no model has been able to explain all the experimental results obtained on porous silicon. These models are explained below.

2.5.1.1 Quantum confinement model

According to this model, in nanocrystalline size structure the band gap energy of crystalline silicon will be increased, also, the indirect band gap of crystalline silicon will be changed to a direct band gap [45]. This model indicates that the origin of the photoluminescence is a quantum size effect within crystalline silicon[36,37,45], i.e radiative recombination occurs in small silicon particles of diameter < 20 Å which are produced during the etching process [46]. The following experiments have shown evidence to support this theory.

a - The proof for the presence of a quantum size crystalline structure in porous silicon layers is obtained by gas adsorption experiments and Transmission Electron Microscopy (TEM) studies [46]. Si particles of diameters 1.86-2 nm are reported by gas adsorption experiments for porous silicon layers on degenerate silicon substrates and even smaller particles with diameters of 0.86 nm are reported for porous silicon layers grown on non-degenerate p-type silicon[36].

b - Quantum size effects have also been invoked to explain the observation of visible photoluminescence in various systems containing silicon nanocrystals, which have been produced by techniques other than etching [46].

c - Extensive etching studies reveal a strong dependence of peak position of the

PL on porosity (the ratio of pore volumes to the total volume of the porous silicon layer) [47]. Figures 2.24 and 2.25 show the PL spectrum variation and peak position shift with the anodization time at room temperature for a fixed current density of 25 mA/cm^2 [47].

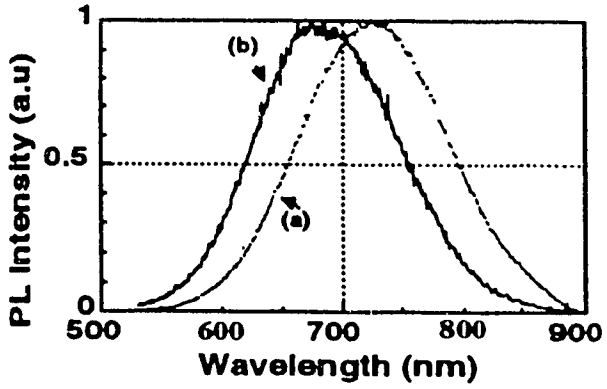


Figure 2.24: PL spectrum variation with the anodization time.a)t=30s b) t=600s.

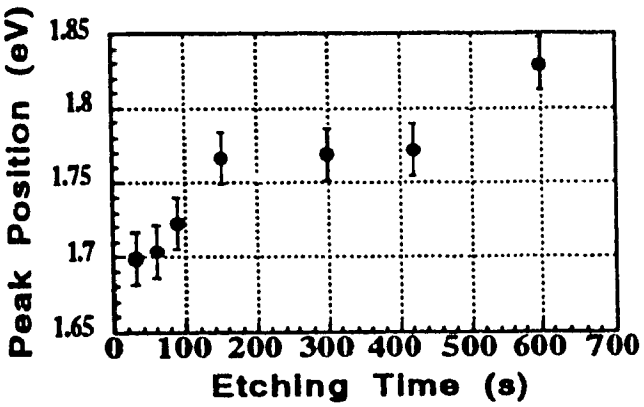


Figure 2.25: PL peak position shift with etching time.

The main feature of these spectra is the PL peak shift with etching time. Crystallites become smaller as the anodization time becomes longer. The peak is located at 730 nm after 30 seconds of etching and shifts continuously with time. After 10 minutes of etching, the peak is located at 678 nm [47]. The following explains the relation between the size of crystallites and the peak position of the PL spectrum:

According to the quantum confinement model, the silicon region between the etched pores can be considered as silicon quantum wires with a square cross section of side L, and their action on the photogenerated carriers can be further approximated as a square potential well with infinite depth[36,44]. Under these circumstances, the following energy barrier E_q can be obtained from the following equation

$$E_q = \frac{h^2}{4mL^2} \tag{2.22}$$

where, h is Plank's constant and m is given by

$$m = \frac{1}{m_h} + \frac{1}{m_e} \tag{2.23}$$

m_h and m_e are the effective hole and electron masses respectively. As a result, the band gap energy of quantum wires or nanocrystalline size silicon structures will be given by the following equation

$$E_g = E_{Crystalline\ Silicon} + E_q \tag{2.24}$$

Therefore, as size of silicon particles decreases(L), E_g will increase which causes a peak shift in the spectrum. This adjustable bandgap of porous silicon will again be discussed later with its connection to improvement of silicon solar cell efficiency.

Figure 2.26 shows the variation of silicon quantum wire energy gaps(Eg) with respect to the size of silicon quantum wires, L [37].

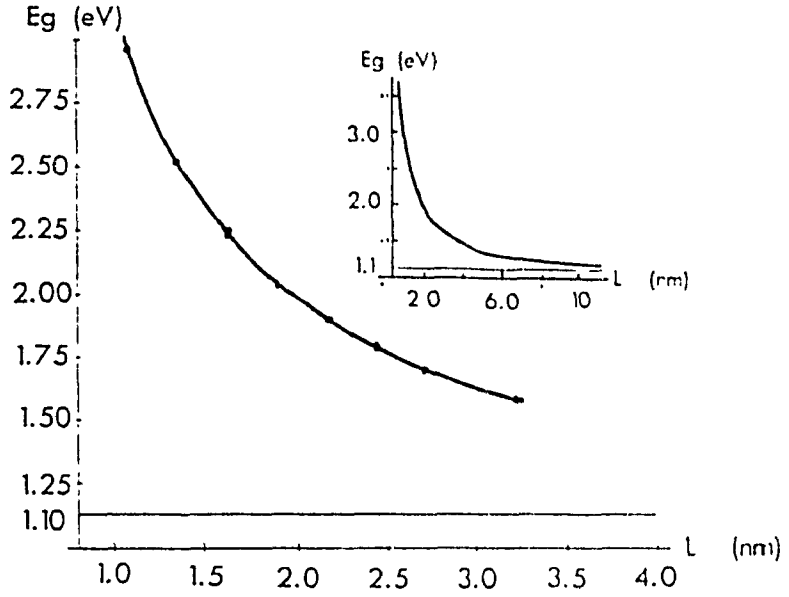


Figure 2.26: Silicon quantum wire energy gaps (Eg) as a function of size of silicon quantum wire(L).

2.5.1.2 Surface chemistry

Another model based on surface chemistry of porous silicon, suggests that the origin of photoluminescence is due to the complex compound of the porous silicon, and it is explained as follows.

(a) - Photoemission from Hydrides

Hydrogen complexes (SiH_x or $(SiH_2)_n$) emit visible light at room temperature [43]. By Fourier Transform Infrared Spectroscopy(FTIR) technique, it is shown that surface of as-prepared porous silicon contains SiH_x 0r $(SiH_2)_n$ structures. Therefore,

the origin of visible photoluminescence at room temperature in porous silicon could be due to the hydrides presenting at the surface.

(b) · Siloxene luminescence mechanism

There is visible photoluminescence from a specific molecular configuration of Si-O-H called siloxene ($Si_6O_3H_6$)[46]. It is suggested that the origin of visible PL in anodically oxidized silicon is due to siloxene ($Si_6O_3H_6$)[46]. Fig.2.27 shows the room temperature visible photoluminescence spectra of anodically oxidize porous silicon layers and of thermal annealed siloxene compounds which are chemically synthesized with two different preparation methods by Kautsky and Wohler[46].

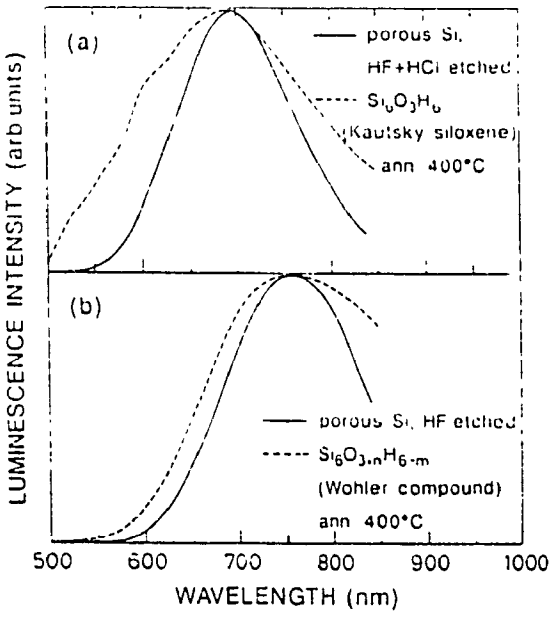


Figure 2.27: Room temperature PL spectra of anodically oxidized porous silicon layers and of thermally annealed siloxene compounds.

The agreement between the light emission from porous silicon layers and that from siloxene compounds strongly suggests a common structural origin of the PL in both cases[46].

2.5.2 Application of porous silicon in silicon solar cells

The following properties of porous silicon make this material potentially a good candidate as an absorbing layer on the surface of silicon solar cells.

2.5.2.1 Porous silicon as a UV convertor

Photoluminescence excitation (PLE) spectroscopy technique can be used to show that porous silicon is a UV convertor. This means that it absorbs UV light and converts it into visible light. In a PLE experiment [48], the wavelength of the excitation light, which is in the UV range, was varied while the change in the PL intensity at a fixed wavelength λ_0, was monitored (usually in the visible range). Figure 2.28 [48] shows the PLE spectra of 2 porous silicon samples with different thicknesses which is monitored at 800 nm. Sample B has a thicker porous silicon layer.

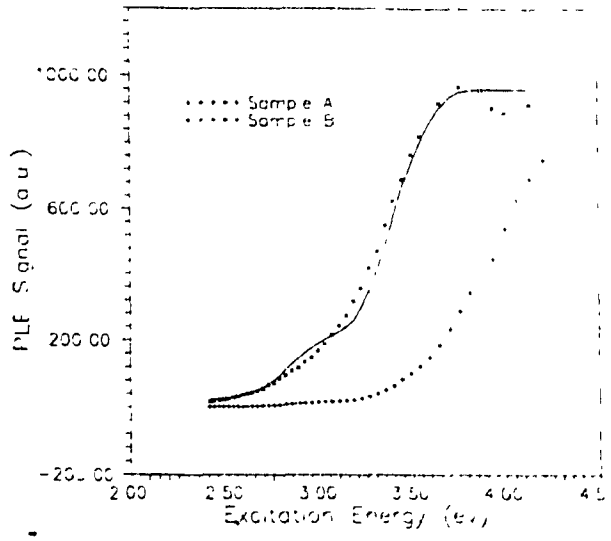


Figure 2.28: PLE spectra of two porous silicon samples monitored at 800 nm.

The PLE signal is the ratio between the photoluminescence intensity and excitation intensity which is proportional to the number of photons of wavelength λ_0 generated by one incident photon[48].

This property has the potential of being advantageous in a silicon solar cell. One would expect a higher efficiency for silicon solar cells with porous silicon layer on the top surface for the following reason.

As wavelength of light decreases the absorption coefficient of silicon increases, as shown in figure 2.15. This results in generation of electron-hole pairs near the surface of the silicon substrate which increases the possibility of photogenerated carriers being lost due to surface recombination.

However, the photoluminescence property of the porous silicon layer on the top surface of the cell can convert the UV and the blue light into longer wavelengths with higher intensity [48] (generation of photons with longer wavelength from photons with shorter wavelength). This can cause an increase in the number of electron-hole pairs inside the silicon substrate at distances far from the surface where the impact of surface recombination is lower. Therefore, photogenerated carriers would have a higher chance of being separated by the electric field inside the depletion region and this would increase the efficiency of silicon solar cells.

2.5.2.2 Porous silicon with Adjustable bandgap energy

Efficiency of solar cells is very dependent on the bandgap energy of the absorber material and it increases as the bandgap energy increases. On the other hand, by looking at figure 2.29 [15], which illustrates the solar spectral irradiance, one realizes that as the bandgap energy increases, the absorber material will become trans-

parent to more photons and this causes a decrease in the number of photogenerated carriers within the absorber material which results in lower efficiency for cells. Therefore an optimum value for the absorber-layer bandgap energy must be found

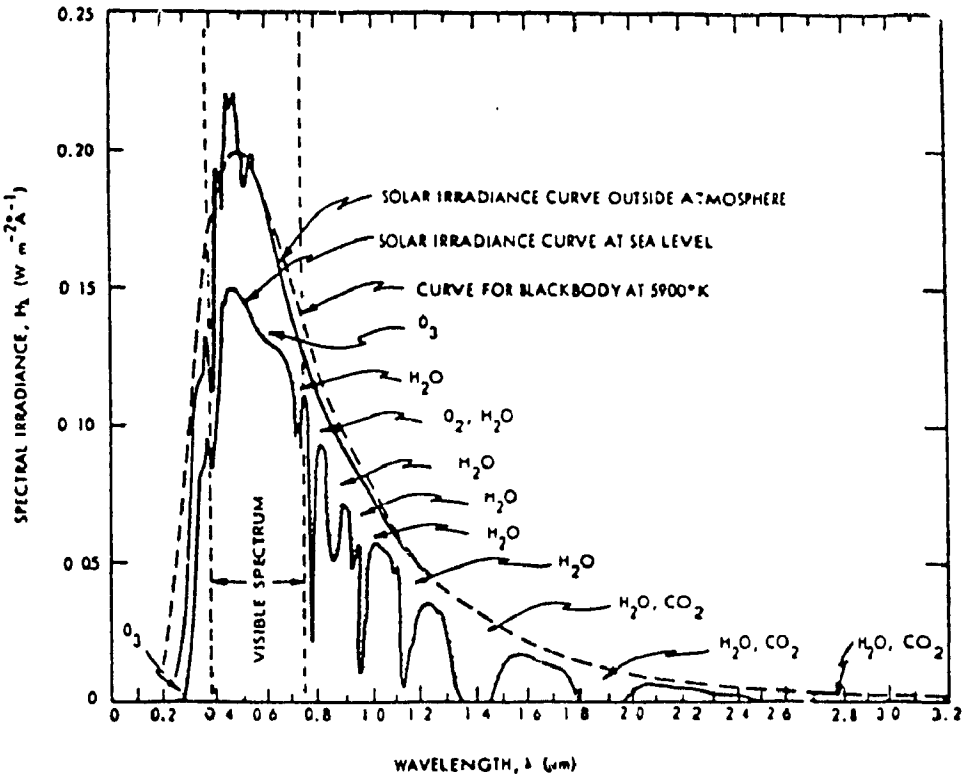


Figure 2.29: Solar spectral irradiance.

The challenge of matching of the bandgap energy to the solar spectra has led to a number of calculations whose results show that the optimum bandgap energy should be about 1.5 eV for maximum solar cell efficiency [1,15,24]. Figure 2.30 [15] shows the theoretical solar cell efficiency versus the band gap energy at room temperature.

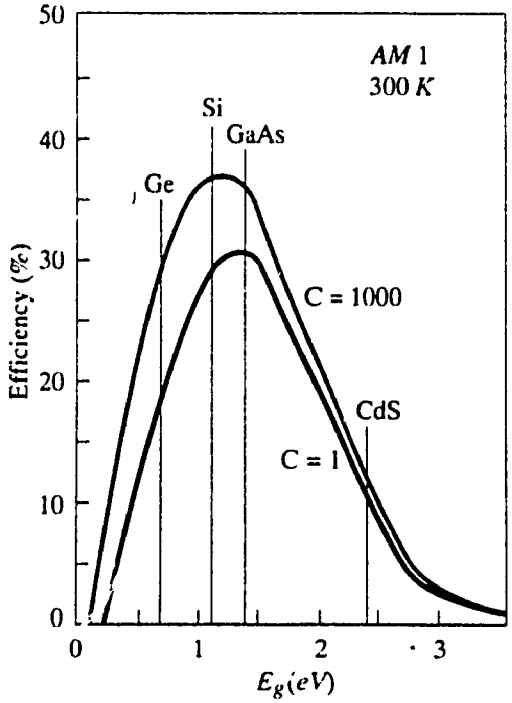


Figure 2.30: Ideal solar cell efficiency at room temperature for C=1 sun and C=1000 sun.

In the previous sections it is shown that the bandgap energy of porous silicon is a function of etching time, HF concentration and current density, consequently, this material can have an adjustable bandgap. As a result, by adjusting the porous silicon bandgap energy for optimum sunlight absorption, one could potentially increase the efficiency of silicon solar cells.

2.5.2.3 Porous silicon as an antireflection coating for silicon solar cells

A bare silicon surface has reflectivities ranging from approximately 55% at 0.35 μm to 30% at 1.1 μm, as shown in the figure 2.31 [28], indicating that a large portion of photons incident on a bare silicon surface will be reflected rather than transmitted into the bulk.

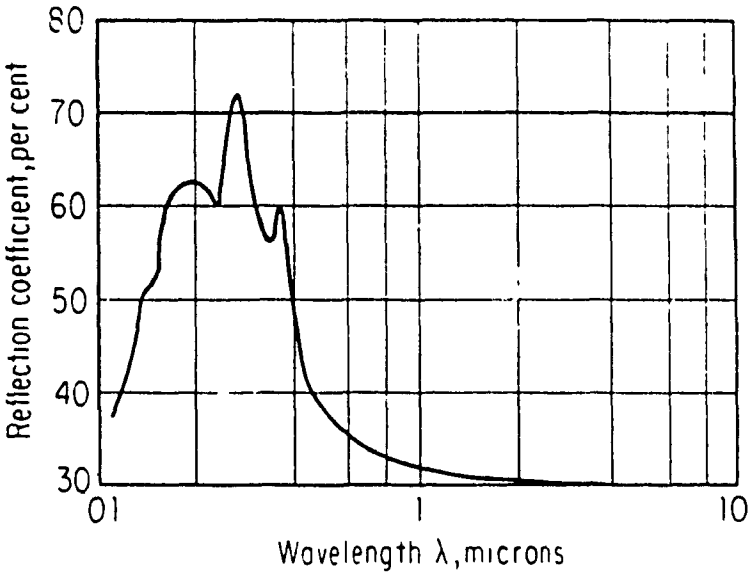


Figure 2.31: Reflection coefficient of silicon vs. wavelength.

This light reflectivity from bare silicon surface minimizes the photogeneration in the bulk and considerably degrades the silicon solar cell efficiency. In order to minimize surface reflectivity of these cells, different efforts have been made through studies of front surface texturization and implementation of antireflection coatings at the surface. Figure 2.32 [2], shows how surface texturization can reduce the reflectivity of light at the top surface by multiple reflections of the light.

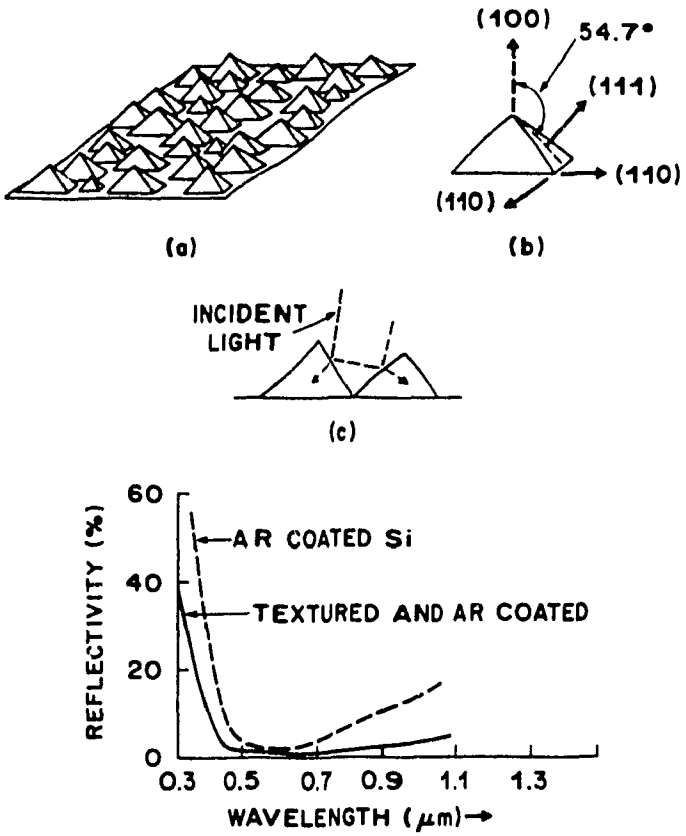


Figure 2.32: Effect of surface texturization on the reflectivity of light.

As it was shown in figure 2.21, porous silicon has a highly textured surface, as a result, this structure may be used to enhance light trapping at the surface of silicon solar cells.

Figure 2.33 [47] illustrates the reflectance curve of porous silicon obtained from UV to near infrared for a non-optimized thickness of porous silicon [47].

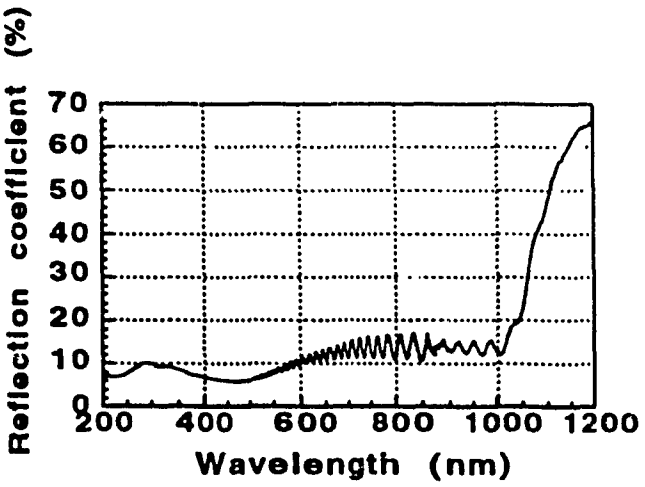


Figure 2.33: Reflectance spectrum of porous silicon prepared at current densities of 25 mA/cm^2.

Figure 2.34 [47] shows low reflectance (about 10 percent) over an extended spectral region which illustrates the antireflection performance of porous silicon.

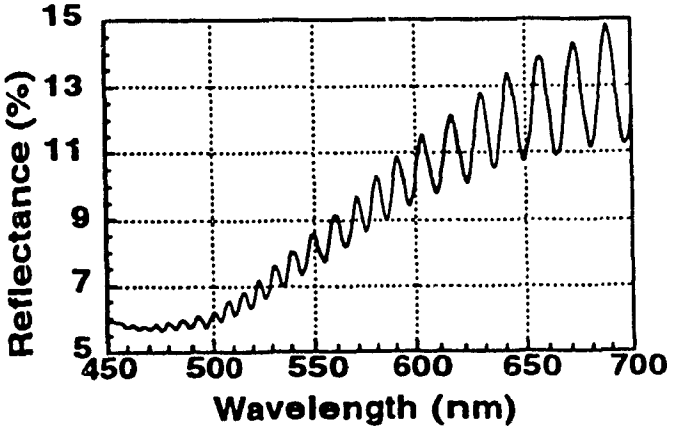


Figure 2.34: reflectance spectrum of porous silicon in the visible region.

The following materials have been used as antireflection coatings for silicon solar cells SiN, SiO_2, MgF_2, Si_3N_4, SiO, Tio_2, Ta_2O_5, Nd_2O_3, ZrO_2, CO_2, Al_2O_3, and ZnS [24]. In order to compare the reflectivity of porous silicon with other materials which are used as an antireflection coating in silicon solar cells, the performances of the best antireflection coatings in terms of their reflectivities are shown below.

Figure 2.35 [49] shows a comparison of the reflectance data for a single-layer SiN film with refractive index of 2 and thickness of 700 Å (n=2, T=700 Å), a double- layer SiO_2/SiN (n=1.45, T=950 Å)/(n=2.3, T=590 Å) and a double-layer MgF_2/ZnS (n=1.38, T=1100 Å)/(n=2.3, T=550 Å). Both double-layer coatings show about 8% reflection in the entire wavelength range of 400-1100 nm. Materials are deposited by plasma enhanced chemical vapor deposition (PECVD)[49].

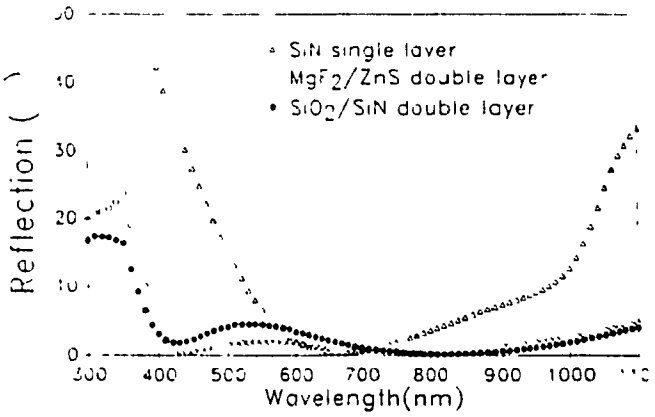


Figure 2.35: Reflectance as a function of wavelength for silicon cells with a) SiN AR coating, b) double-layer MgF_2/ZnS coating, c) SiO_2/SiN AR coating.

Figure 2.36 [50], shows the reflectivity of a double-layer titanium dioxide and silicon oxide with optimum thicknesses, deposited on a textured surface with inverted pyramids.

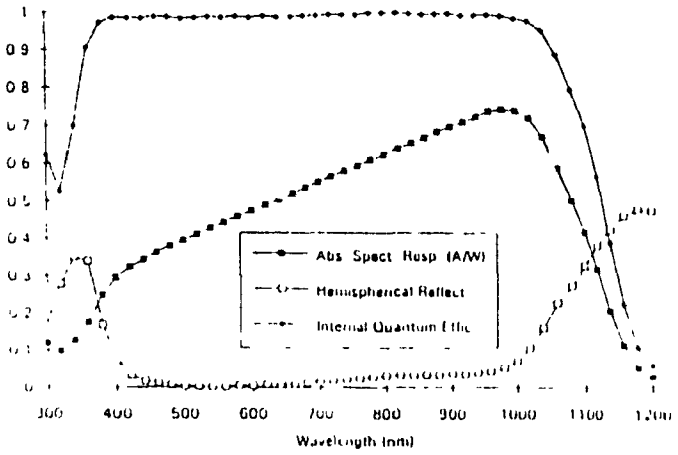


Figure 2.36: Reflectance spectrum for a double-layer titanium dioxide and silicon oxide AR coating deposited on a silicon textured surface with inverted pyramids.

The reflectance is less than 5% at all wavelengths between 420 to 980 nm. TiO_2 thin film is deposited by rf magnetron reactive sputtering of titanium under high vacuum (10^{-7}Torr).

Figure 2.37 [51], shows a comparison of reflectance data for 1) bare silicon, 2) a single- layer Nd_2O3 (n=1.5, T=500 Å), 3) a double- layer Nd_2O_3/ZnS (n=1.5, T=500 Å)/(n=2.3, T=700 Å).

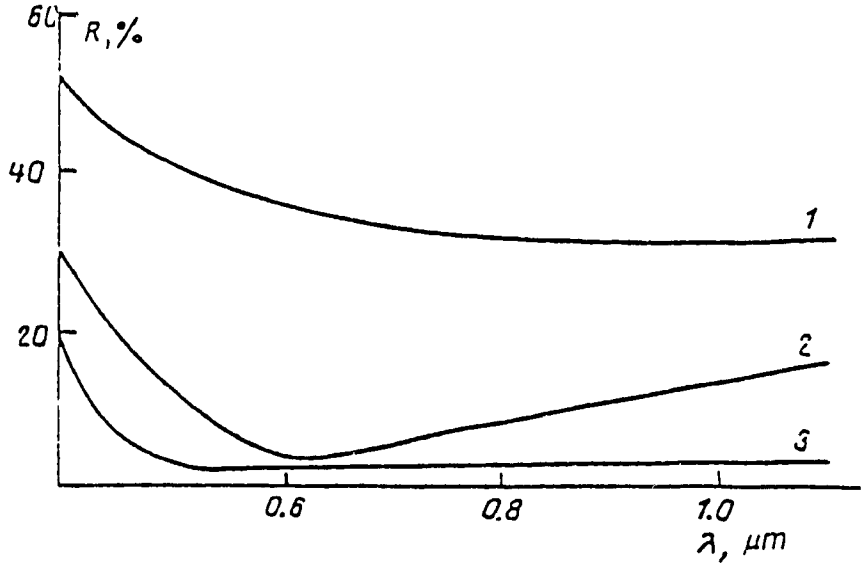


Figure 2.37: Reflectance spectrum for a double-layer Nd_2O_3/ZnS AR coating.

The double-layer coating shows lower than 5% reflectivity at wavelengths between 520 to 1100 nm. Nd_2O_3 is one of members in the rare-earth metal oxide family (REMO). REMO have refractive indexes ranging from 1.77 to 2.18 [52]. A film of the rare-earth metal is obtained by means of thermal deposition from a molybdenum tray in vacuum of about 10^{-5} Torr, then Nd_2O_3 film is obtained by thermal oxidation in the air at 450 ^{o}C [51].

However, in the industry none of above materials is used as an AR coating because they must be deposited either by plasma enhanced chemical vapor or by sputtering machines under vacuum, which are very critical and expensive pro-

cesses[24]. The most common antireflection coating used for silicon solar cells is one layer of SiO_2 with thickness of 1120 Å [18]. In the figure 2.38 [18], the upper curve shows the reflectance of a 1120 Å layer of SiO_2 deposited on the surface of a silicon solar cell and has an average reflectivity of about 18%. The lower curve is for a double-layer MgF_2/TiO_2 (n=1.38, T=1000 Å)/(n=01, T=360 Å).

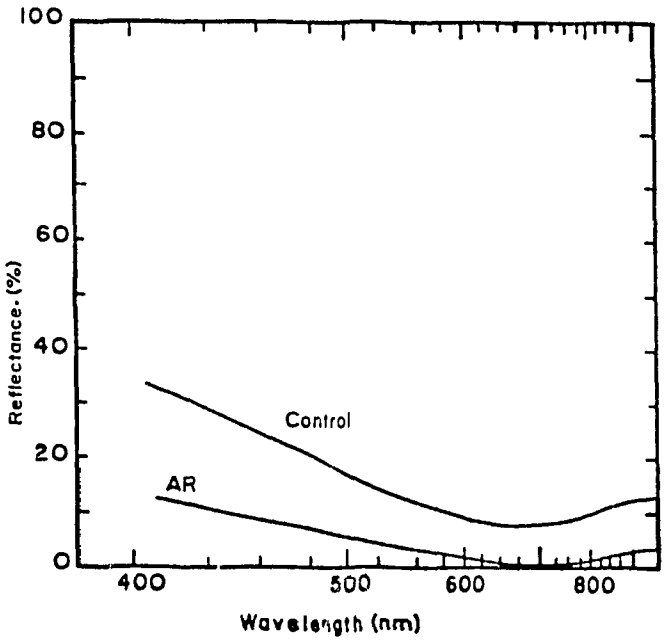


Figure 2.38: Reflectance spectrum for SiO_2 and a double-layer MgF_2/TiO_2 AR coating.

By considering the reflectance curves of all AR coating layers, one notices that reflectivity increases below wavelength 0.5 microns and from solar spectral irradiance for air mass one, figure 2.29, this increase in reflectivity causes loss of all high energy photons which have ability to generate charge carriers inside the bulk. However, in the case of porous silicon whose absorption and light emission properties can be adjusted over a wide range, not only might there not be any loss of high energy photons, the photoluminescence property of this material could convert those

photons to photons with longer wavelengths and higher intensities which could result in generation of more charge carriers in the bulk.

Compared with all of above antireflection coatings, porous silicon etching looks promising and might be able to produce equal results once the etching is fully optimized for minimum reflectance. Moreover, porous silicon is an extremely simple process and much cheaper than multi AR coating deposition. It is well suited for large-area, low-cost silicon solar cell process. The experiments in chapters 5 and 6 explore those possibilities.

CHAPTER 3

Fabrication Processes

Prior to initiating the fabrication process, the junction depth, impurity profiles, and surface concentration of solar cells were investigated, using SUPREM-IV. In this chapter the results of the simulations are described, then fabrication process summary and the mask layouts will be discussed.

3.1 SIMULATION RESULTS

Before cell fabrication, it was decided to do some simulations in order to optimize the impurity profiles within the silicon substrate in terms of surface concentration and junction depth. To do this, the SUPREM-IV which is a semiconductor fabrication process simulator program (written by M. E. Law, Stanford), was used. The program has the ability to simulate the following processing steps:
inert ambient, drive-in, oxidation of silicon and silicon nitride, ion-implantation, epitaxial growth of silicon, and etching of various materials.

For the simulation, a silicon substrate with background concentration of $4x10^{14}$ cm^{-3} was considered. The target parameters were: (i) highest surface concentration possible (~ 10^{20} cm^{-3}) and (ii) the junction depth in the range of 2 to 4 microns. For this, various initial conditions were considered in order to optimize the final results. Then the parameters which gave the optimal final results were chosen to fabricate the solar cells. The most sensitive step in this fabrication was the diffusion of impu-

rities into the silicon. The profiles of these diffusions determine the surface concentration, junction depth, ohmic contacts, and pn junction. Erroneous profiles would result in malfunction of the final device.

Initially, two techniques were considered for the diffusion process during the device fabrication. 1- spin-on silica-gel, 2- ion implantation. In the case of (1), the initial parameters such as silica-gel concentration, temperature, and time were varied and several simulation results were generated. For the case (2), also several simulation profiles were produced using various values for the implantation energy and implantation dose.

Figure 3.1 shows the profile of boron atoms in the silicon substrate, using spin-on silica-gel. In this graph, the solid curve corresponds to the profile of boron atoms in the silicon substrate after 2 hours predeposition at temperature 1100 ^{o}C in a nitrogen ambient. The surface concentration is $3x10^{20}cm^{-3}$ and the junction depth is located at 3.5 microns. The dotted curve shows the profile after 1 hour oxidation in a wet environment at 1000 ^{o}C. The new surface concentration is about $10^{20}cm^{-3}$ and the junction depth is at 4.2 microns. The dashed curve corresponds to the final profile of boron atoms in silicon after 1 hour phosphorous predeposition followed by 13 minutes oxidation and 15 minutes annealing at 1000 ^{o}C. The final profile shows a surface concentration of $10^{20}cm^{-3}$ and the junction depth is at 4.5 microns. The sharp decrease from $3x10^{20}$ to $10^{20}cm^{-3}$, which is represented by a dashed vertical line in the vicinity of original silicon surface (x=0), corresponds to the Si/SiO_2 interface and one can see that the concentration of boron atoms in the SiO_2 is higher than its concentration in silicon and this is due to back diffusion of boron atoms into the oxide layer. This is consistent with the segregation coefficient (M) of boron (which is defined as ratio of boron concentrations in the silicon and silicon dioxide) being less than 1 [33].

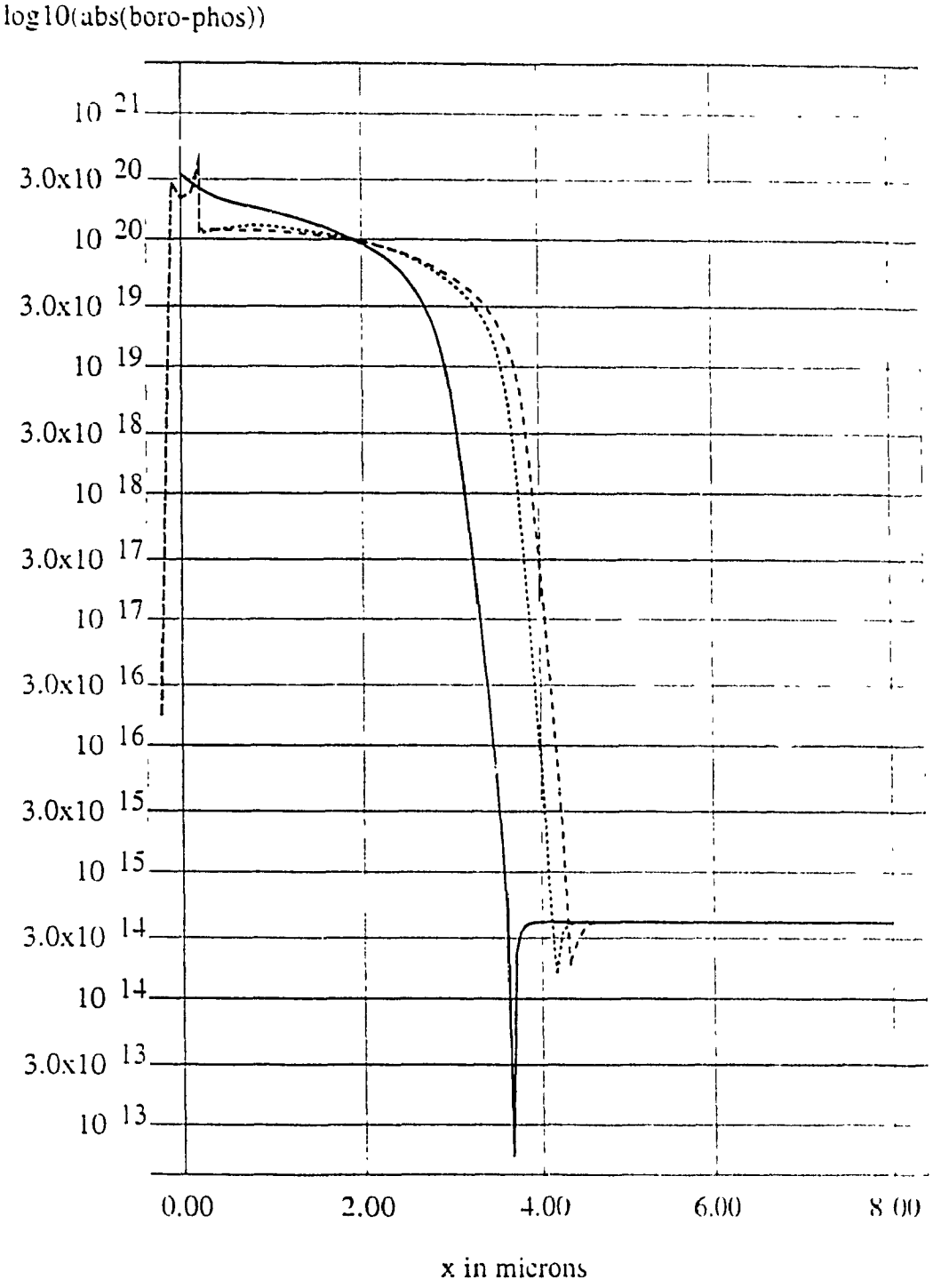


Figure 3.1: Profile of boron in silicon substrate after all high temperature steps (spin-on silica-gel technique was used to do the diffusion process).

Figure 3.2 shows the profile of phosphorus atoms in the same silicon substrate. The solid curve shows the profile of phosphorous atoms with a surface concentration of $5x10^{20}cm^{-3}$ and a junction depth at 1 micron after 1 hour phosphorous predeposition at 1000 °C in a nitrogen ambient. The dotted curve shows the profile after 13 minutes oxidation at 1000 °C with a surface concentration of $2x10^{20}cm^{-3}$ and junction depth at 2.1 microns. The final profile of phosphorous after 15 minutes annealing at 1000 °C is represented by the dashed curve in which, the surface concentration is at $2x10^{20}cm^{-3}$, high enough to make good ohmic contacts. In this case the sharp drop from $2x10^{20}$ to about $8x10^{18}cm^{-3}$ which is represented by a dashed vertical line, corresponds to the Si/SiO_2 interface. In this case the segregation coefficient (M) of phosphorus is greater than 1 which is in agreement with the values in the literature.

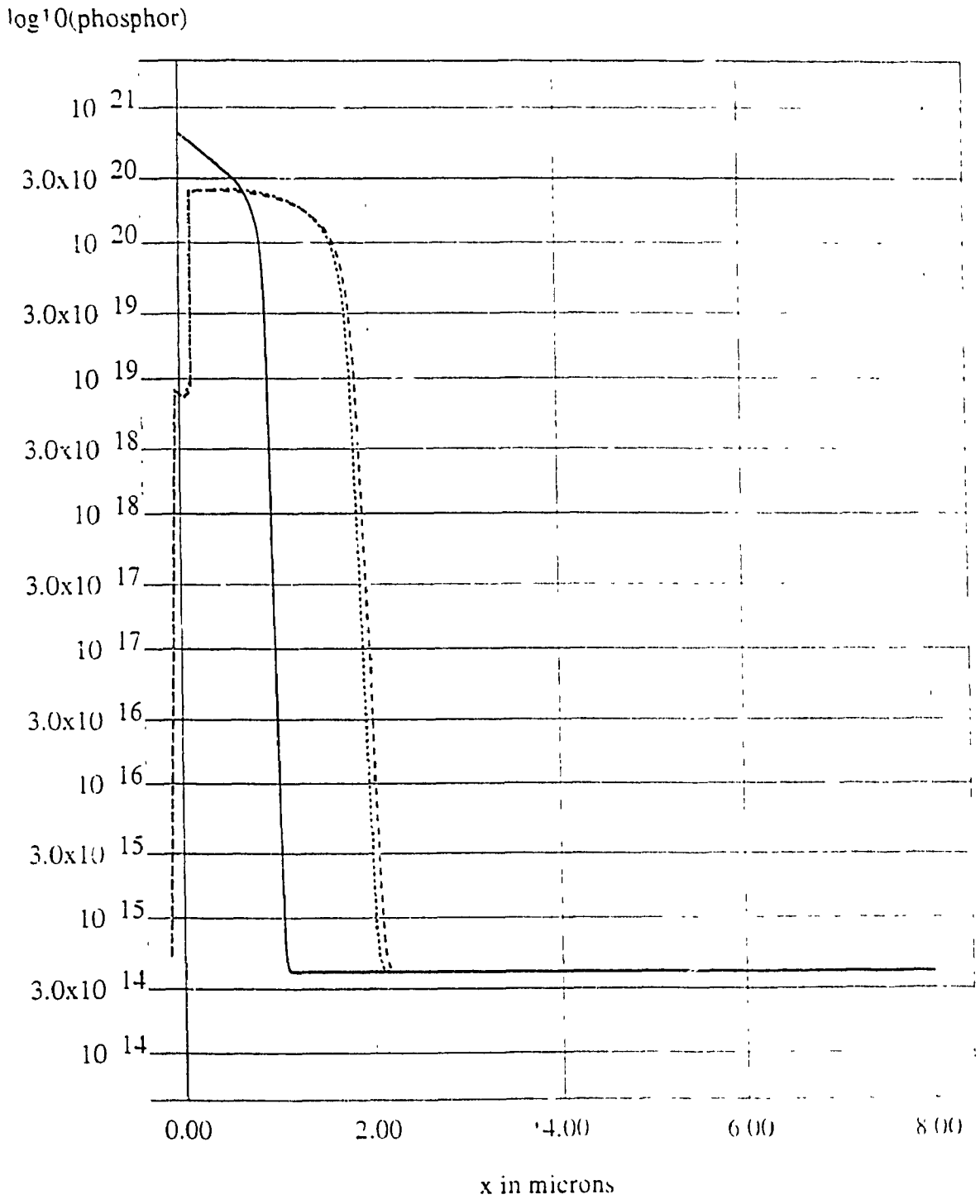


Figure 3.2: Profile of phosphorous atoms in the silicon substrate after all high temperature steps.

Figure 3.3 shows the profile of boron atoms in the silicon substrate, using the ion implantation technique. In this case the solid line corresponds to the profile of boron atoms after implantation of boron at an energy of 50 KeV and a dose of $10^{16}cm^{-2}$. After 1 hour oxidation at 1000 ^{o}C, the profile is changed and represented by the dotted curve with surface concentration at $3x10^{19}cm^{-3}$and the junction depth at 2.5 microns. The final profile is shown by the dashed curve after 1 hour phosphorous predeposition followed by 13 minutes oxidation and 15 minutes annealing all at the same temperature, 1000 ^{o}C. The final surface concentration is about $3x10^{19}cm^{-3}$ and the junction depth is at 2.7 microns. From the graph, the value of boron segregation coefficient (M) is less than 1, which is expected.

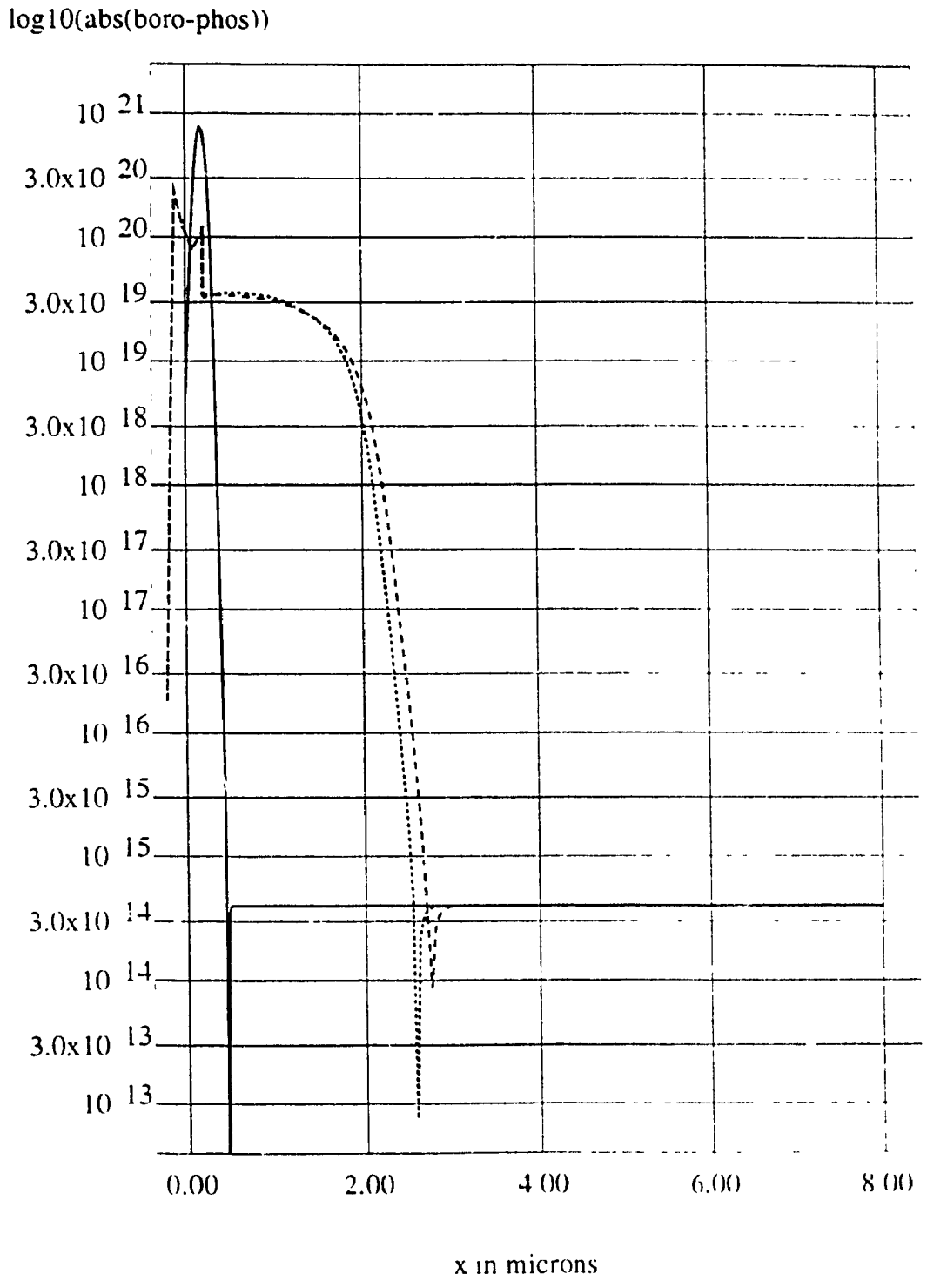


Figure 3.3: Profile of boron atoms in silicon substrate after all high temperature steps (ion implantation method is used to do the diffusion process).

3.2 Fabrication Process Summary

As described in the section 3.1, the most sensitive step in the fabrication is the diffusion of impurities into the silicon substrate which determines the surface concentration and the junction depth. The surface concentration is a crucial parameter and can degrade the ohmic contacts if its value is less than ~10^{20} cm^{-3}. Therefore, two different methods, sol-gel diffusion and ion implantation, were used to introduce boron atoms into the silicon substrate, to investigate the effects of these techniques on the device performance (it is believed that if sol-gel technique is used to diffuse boron atoms into the n-type silicon, there may be formation of a thin brownish glassy layer, so called "brown stain", which may cause a high resistance). In case of phosphorous atoms, the sol-gel diffusion technique was always used. Therefore, there are two different groups of solar cells with two slightly different fabrication sequences as will be explained below. For more details on each step, consult appendix A.

Starting materials:

n-type wafer

phosphorus doped, concentration~$4x10^{14}$ cm^{-3}

(100) orientation

average resistivity: 8 Ω-cm, 11 Ω-cm

thickness: 500 ±10 μm, 300 ±10 μm, 100 ±0.1 μm

p-type wafer

boron doped, concentration~$2x10^{15}$ cm^{-3}

(100) orientation

average resistivity: 5.4 Ω-cm

thickness: 300 ±10 μm, 100 ±0.1 μm

Initial Cleaning

Clean silicon samples using Reverse-RCA cleaning procedure (explained in appendix A).

Thermal Oxide

It was found that an oxide thickness greater than 0.45 μm is needed to mask 99.9999% of boron atoms which are implanted at an energy of 50 KeV, and in the case of boron pre-deposition at a temperature of 1100 °C for 2 hours, an oxide thickness greater than 0.25 μm will be required. Therefore it was decided to grow a layer of oxide with thickness of 0.6 μm.

Wet oxide (mask against boron)

Temperature = 1000 °C

Time = 120 min

Thickness = 0.6 μm

Mask #1

Deposit photoresist and use photolithography techniques and mask #1 to open boron implant/diffusion windows in the deposited photoresist. Etch oxide by a 1:4 solution of HF:NH_4F (BOE solution). Strip photoresist and clean the samples, using Reverse-RCA cleaning procedure.

At this point (for next step) samples are divided into two groups (a) and (b) which were processed differently.

a) Boron Implantation

Implant boron with a dose of $10^{16}cm^{-2}$ atoms at an energy of 50 KeV, strip photoresist, and clean wafers using Reverse-RCA cleaning procedure.

b) Boron Pre-deposition

Spin on borosilica, bake in the oven for 15 minutes at temperature 150 ^{o}C to dry the wafers and do the pre-deposition.

Boron pre-deposition

Temperature = 1100 ^{o}C

Time = 120 min

Ambient: N_2:O_2 (90%:10%) gas

Thermal oxide

It was found that an oxide thickness greater than 0.32 μm is needed to mask a phosphorus pre-deposition at 1000 ^{o}C for 1 hour. Therefore a layer of oxide with thickness of 0.35 μm was grown on both group of samples.

Wet oxide (mask against phosphorus)

Temperature = 1000 ^{o}C

Time = 60 min

Thickness = 0.35 μm

Mask #2

Deposit photoresist, apply mask #2, open phosphorous diffusion windows in the deposited photoresist. Etch the oxide in BOE solution.

Phosphorus Pre-deposition

Spin on phosphorosilica, bake in the oven for 15 minutes at temperature 150 ^{o}C to dry the wafers and do the pre-deposition.

Phosphorus pre-deposition

Temperature = 1000 ^{o}C

Time = 60 min

Ambient: N_2 gas

Passivating Oxide

Grow a thin layer of oxide (1100 Å) to passivate the whole surface and to form an anti-reflection coating on the cell's front surface.

Wet oxide (passivating layer)

Temperature = 1000 °C

Time = 13 min

Thickness = 1100 ±50 Å

Annealing

To reduce the density of fixed charges, Q_f, in the oxide layer, anneal wafers in the nitrogen ambient for 15 minutes.

Annealing

Temperature = 1000 °C

Time = 15 min

Ambient: N_2 gas

Mask #3

Deposit photoresist on both sides of the samples and by using photolithography, open contact windows (mask#3) in the n and p diffused fingers. Etch the oxide in BOE solution. The oxide on the front surface of the sample is protected by the photoresist. Strip photoresist and clean wafers.

Mask #4

Deposit photoresist and use mask #4 to open metallization windows. Metalize samples with the aluminum.

Lift-off

Float off the excess aluminum by soaking samples in the acetone.

Post metallization annealing

In order to make good contact between the silicon and metal and make further improvement at the interface of these two layers, anneal samples in the annealing furnace.

Post metallization annealing

Temperature = 450 ^{o}C

Time = 30 min

Ambient: H_2:N_2 (50%:50%)

Porous Silicon Formation

The schematic for porous silicon formation is shown in figure 3.4. This set up was used to prepare porous silicon layers on both n- and p-type cells at Ecole Polytechnique, MODFAB Lab.

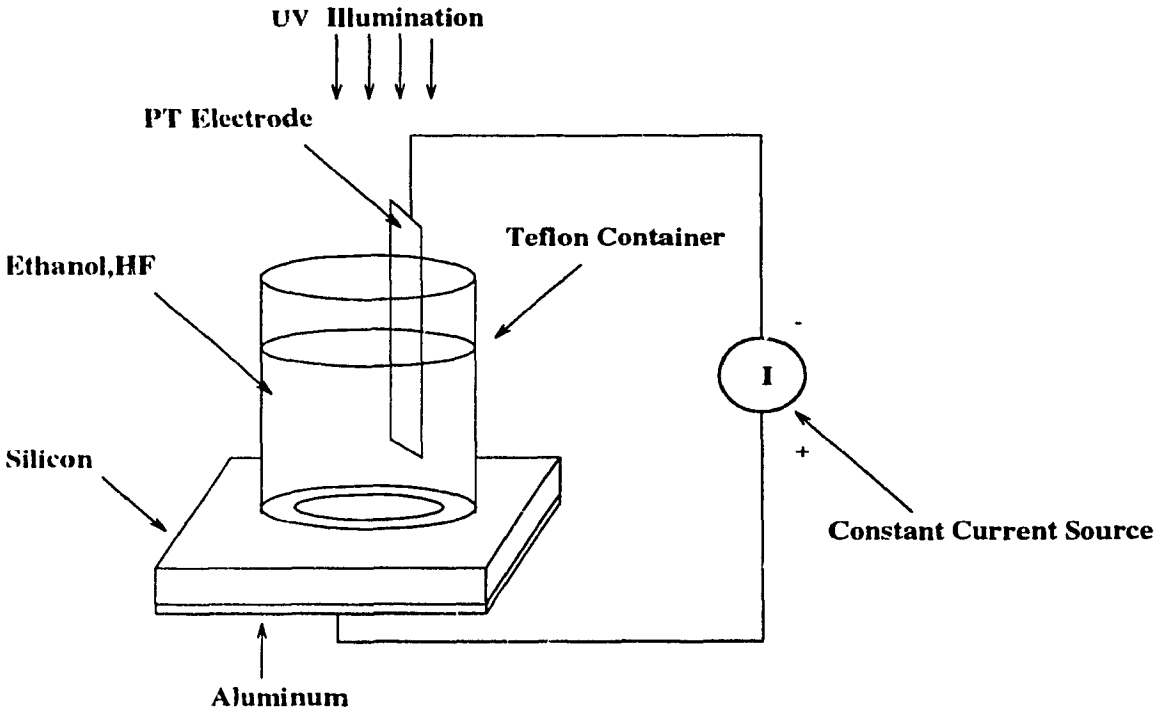


Figure 3.4: Formation of porous silicon under UV light.

Porous silicon formation conditions

N-type cell:	P-type cell:
1- cell thickness=300 μm	1- cell thickness=300 μm
Current density=8.88 mA/cm^2	Current density=4.44 mA/cm^2
Etching time = 180 sec	Etcing time = 120 sec
2- cell thickness=100 μm	2- cell thickness=100 μm
Current density=3.56 mA/cm^2	Current density=2.22 mA/cm^2
Etching time = 120 sec	Etching time = 120 sec

The experiment must be performed under the UV light

The following steps are taken to make porous silicon layers:

1. Remove the 1120 Å thick silicon dioxide on the front surface of the cells, using Q-tip and diluted HF.
2. Rinse in DI water and blow dry with nitrogen gas.
3. Clean the Teflon container with methanol and rinse in DI water.
4. Set the appropriate current and voltage values on a programmable constant current source.
5. Bring the front surface of the cell in contact with the hole present at the bottom of Teflon container and make sure that there is good contact.

Note: Electrolyte solution contains HF which can ruin aluminum in seconds, therefore, care must be taken to stop any leakage of HF that leads to a damage to aluminum paths on the other side of the cell.

6. Fill the container with a mixture of concentrated HF and ethanol (1:1).
7. Put the platinum electrode inside the electrolyte solution.

8. Connect the constant current source to the set up in a reverse biased form.

9. Turn on the 254 nm wavelength UV light.

10. Start the current source and at the same time start timing.

11. Stop the current source and turn the UV light off.

12. Disconnect the wires and remove the Platinum electrode.

13. Remove the electrolyte from the container in such a way to stop any leakage.

14. Fill the container with DI water for 30 seconds and then remove DI water.

15. Take the sample off the container bottom and rinse in DI water (for thin samples this should be done very carefully, otherwise, the sample will brake).

16. Blow and dry with nitrogen gas.

3.3 Layout

There were 4 masks with the following structures used in the fabrication of IBC solar cells, originally designed by V.Logiudice [16].

3.3.1 Mask #1: Boron diffusion

Figure 3.5 shows the layout of the 2.04 cm^2 boron diffusion mask. There are 13 p-type diffusion fingers on the mask's upper left-hand quadrant measuring 300 by 9980 microns each separated by a distance of 500 microns. There are also 5 alignment marks, 3 van der pauw structures, and 2 spaces (rectangles) for the four contact resistance test patterns. The Van der Pauw structures are used to measure the diffusion and metallization sheet resistances and the contact resistance structures are used

to measure the n and p contact resistances. The effective area of the cell is 1.12 cm^2.

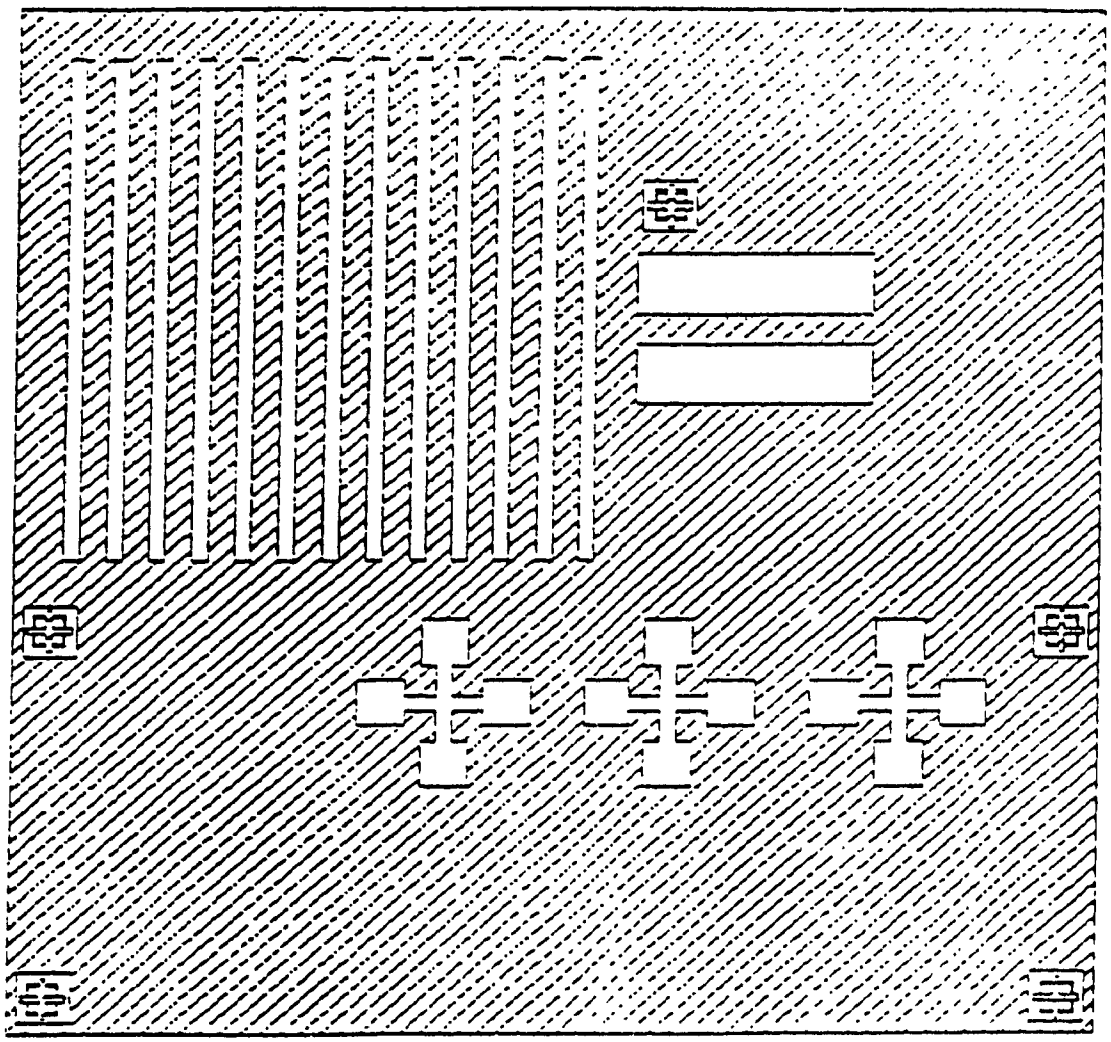


Figure 3.5: Boron diffusion mask (mask # 1).

3.3.2 Mask # 2: Phosphorous diffusion

Figure 3.6 shows the layout of the phosphorus diffusion mask. There are 13 n-type diffusion fingers measuring 100 by 9980 microns located between the boron fingers and separated by a distance of 700 microns from each other. There are alsc 3 Van der Pauw structures for measuring the sheet resistance of diffused phosphorus layer and 2 spaces for the four contact resistance test pattern.

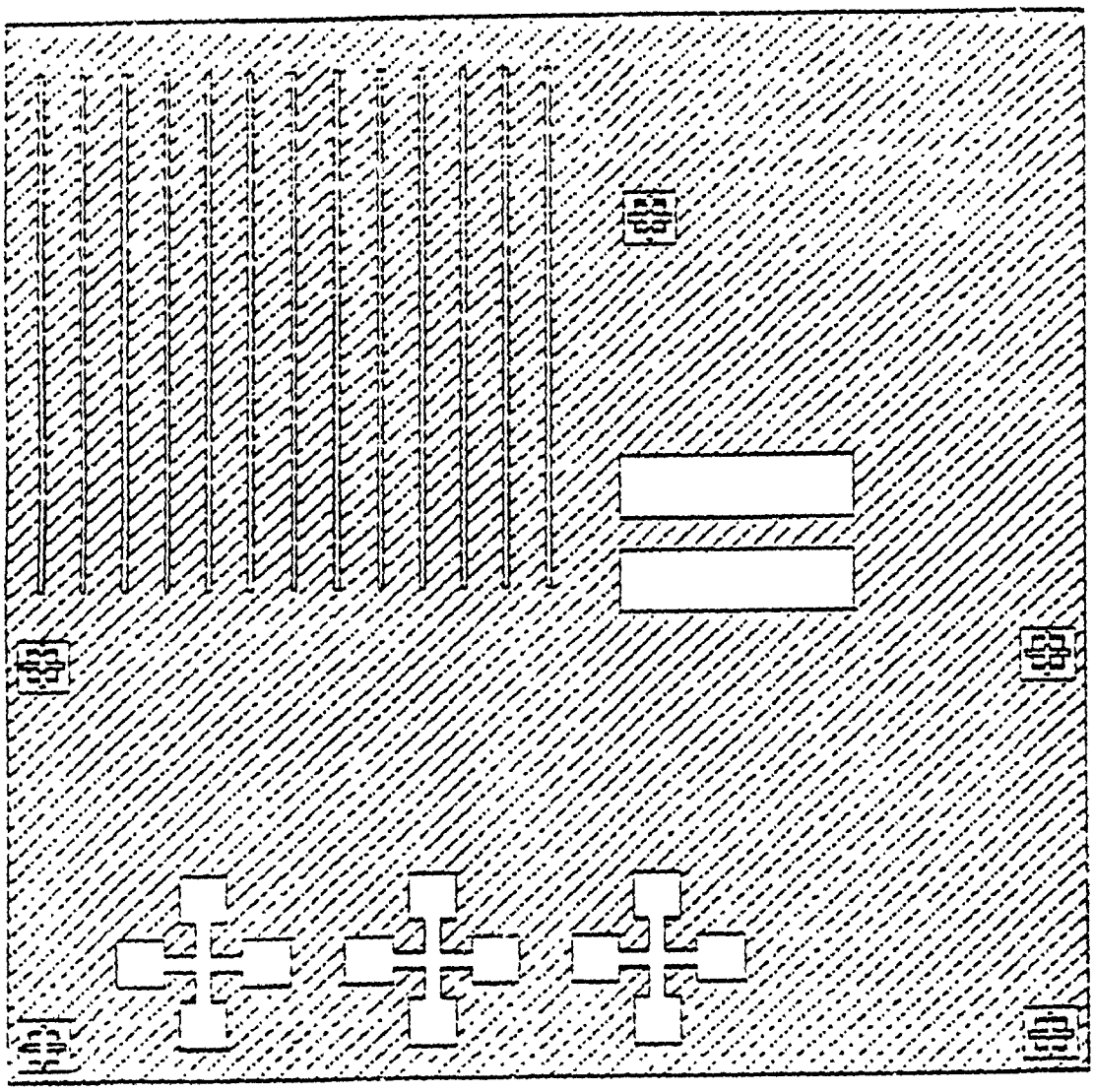


Figure 3.6: Phosphorus diffusion mask (mask # 2).

3.3.3 Mask # 3: Contact

Figure 3.7 shows the layout of the contact mask which is used to open areas on the wafer surface where the oxide must be removed prior to metallization. All Van der Pauw windows as well as the contact resistance patterns are opened with this mask.

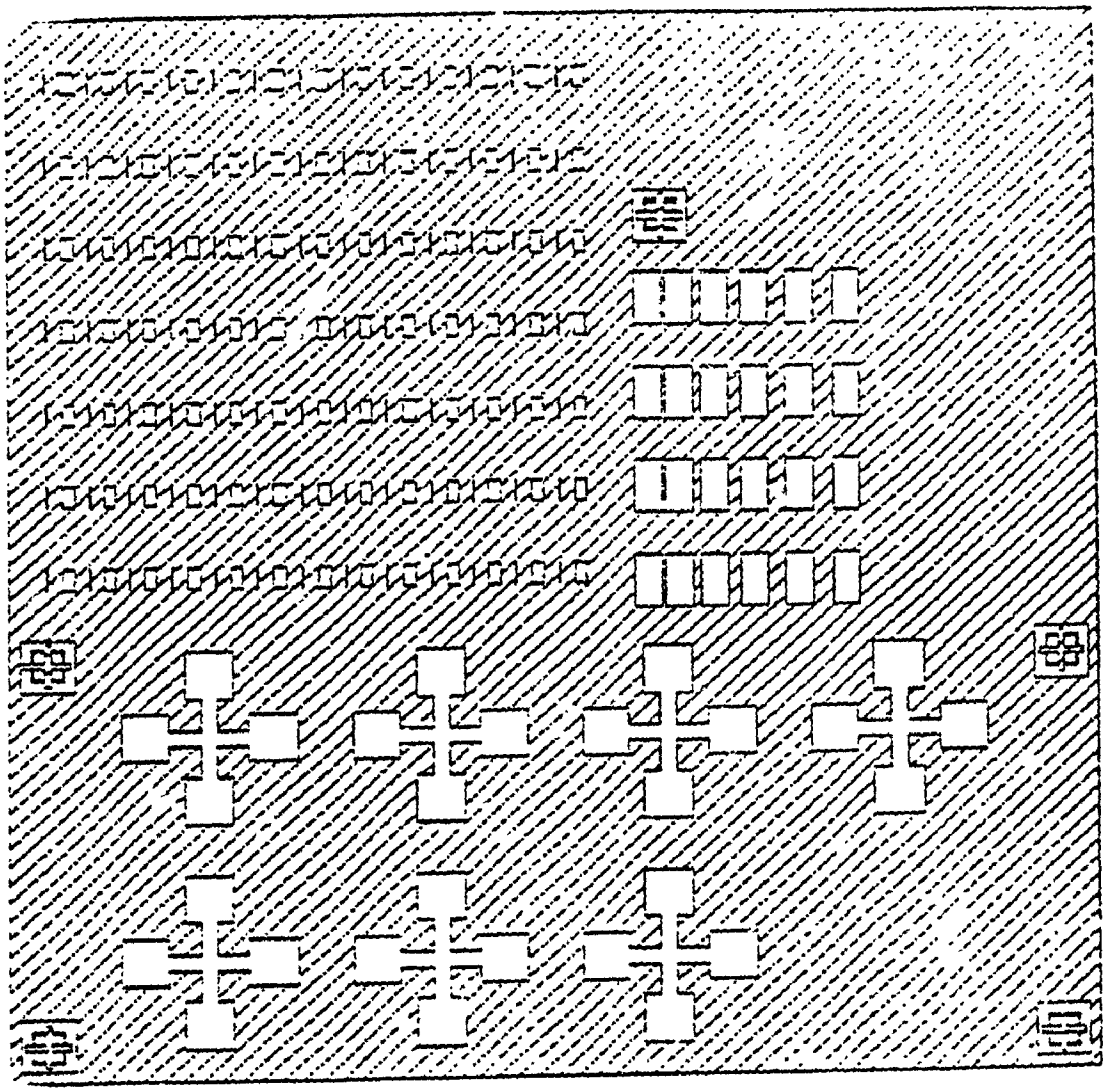


Figure 3.7: The contact mask (mask # 3).

There is also a Van der Pauw pattern opened in the oxide which covers the undoped region in the substrate and this can be used to measure the sheet resistance of the aluminum. To minimize the back surface recombination, the cell's rear surface must be passivated with the oxide, therefore, instead of opening large contact holes in the entire length of n- and p-type diffusion fingers, smaller holes are opened in this region. There are 7 holes measuring 20 by 396 microns along the length of each n-type diffusion finger and each hole is vertically separated from the next one by a distance of 1188 microns. For the p-type fingers, the contacts are made in the same manner except for the width of the holes which in this case is 220 μm rather than 20 μm.

3.3.4 Mask # 4: Metallization

Figure 3.8 shows the metallization mask which opens areas on the surface where metal is to be deposited. As it is shown in the figure, there are 2 Van der Pauw structures which are covered by the aluminum to measure the sheet resistance of the aluminum. There is a contact string pattern metallization to check for the probability of open or short circuits in the metallization. This structure is composed of two long parallel metal lines separated by a small distance which in this case is 40 microns, the distance between the n- and p-type finger metallization. Approximately 89% of

cell's active back surface is covered with aluminum and this will maximize the back surface reflector effect, that is, any unabsorbed photons will be reflected back to the substrate and this will increase the probability of absorption of longer wavelength photons. The contact pads have areas of 6.3 mm^2 and 8.4 mm^2.

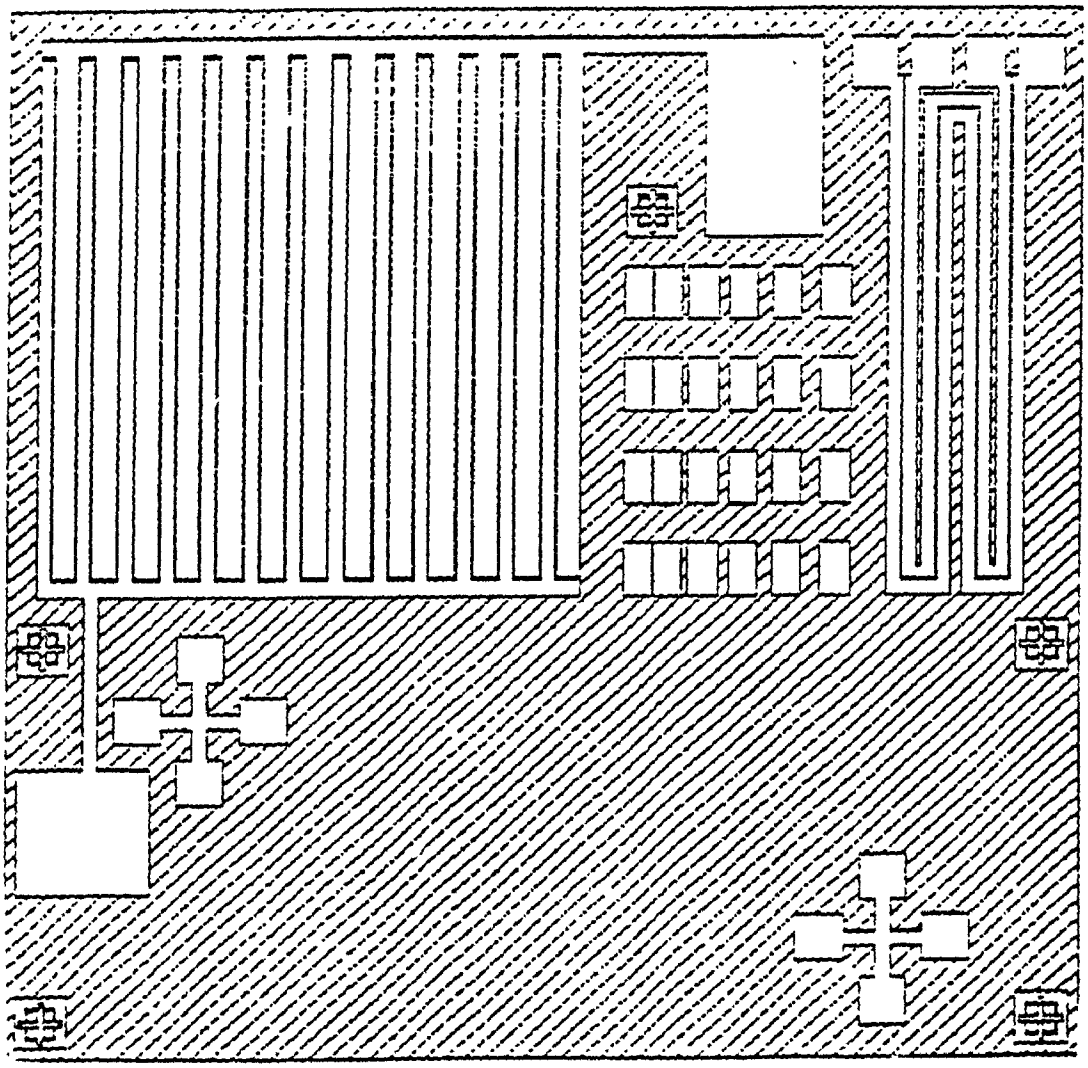


Figure 3.8: Metallization mask (mask # 4).

CHAPTER 4

Basic Device and Dark I-V Characterization

In this chapter, the sheet resistance results for the cells are presented and then the surface concentrations for the n- and p-type diffused layers are estimated using Irvin's curves for n- and p-type Gaussian diffusion profiles. The estimated surface concentrations are compared with the results obtained from simulations. The chapter continues with the I-V characteristics of n- and p-type contacts and an estimation of series resistance followed by the dark I-V characteristics of the cells. The methods to obtain the values of reverse saturation current, ideality factor, series, and shunt resistances from the dark I-V curves, are discussed and the corresponding results are tabulated.

4.1 Basic Device Characterization

4.1.1 Sheet Resistance

The sheet resistances for the aluminum, phosphorus, and boron diffused regions are obtained from Van der Pauw structures. The measurements were made on each sample using a probe station equipped with four probe/chuck assemblies. The average values for the sheet resistances are calculated as described in the Appendix B.

The average sheet resistances for the cells are shown in the tables 4 and 5.

Cell ID	Substrate type	Substrate thickness (μm.)	Boron technique	Al thickness (μm)	$R_{Ave,sht}$ Al (Ω/❑)	$R_{Ave,sht}$ boron (Ω/❑)	$R_{Ave,sht}$ phos. (Ω/❑)
N^1_{01}	**n**	**500**	**Sol-Gel**	**0.300**	**0.115**	**93**	**5.840**
N^1_{02}	n	300	Implant	0.500	0.058	26	4.900
N^1_{03}	n	300	Implant	0.300	0.128	25.110	5.270
N^2_{04}	n	300	Implant	0.400	0.094	24.800	5.480
N^2_{05}	n	300	Implant	0.400	0.091	24.660	4.580
N^2_{06}	n	300	Implant	0.300	0.115	25.800	5.150
N^1_{07}	n	300	Sol-Gel	0.400	0.086	490	5.820
N^1_{08}	n	300	Sol-Gel	0.400	0.087	558	5.200
N^2_{09}	n	300	Sol-Gel	0.300	0.112	224	6.600
N^2_{10}	n	300	Sol-Gel	0.300	0.115	260	5.020
N^2_{11}	n	300	Sol-Gel	0.300	0.111	110.400	7.780
P^2_{12}	p	300	Implant	0.300	0.123	39	4.900
P^2_{13}	p	300	Implant	0.300	0.146	34.050	3.750
P^2_{14}	p	300	Implant	0.300	0.137	33.200	4.300
P^2_{15}	p	300	Sol-Gel	0.300	0.129	86.820	4.330
P^2_{16}	p	300	Sol-Gel	0.400	0.090	81.200	4.020

TABLE 4. Average sheet resistances for Al, and Phosphorous and Boron diffusions for the 500 and 300 micron cells.

cell ID	Substrate type	Substrate thickness (μm)	Boron technique	Al thickness (μm)	$R_{Ave,sht}$ Al (Ω/❑)	$R_{Ave,sht}$ boron (Ω/❑)	$R_{Ave,sht}$ phos. (Ω/❑)
N_{17}	n	100	Implant	0.60	0.06	25	6.70
N_{18}	n	100	Implant	0.60	0.06	36.74	11.60
N_{19}	n	100	Implant	0.60	0.06	23.77	6.30
N_{20}	n	100	Sol-Gel	0.60	0.06	44.20	8.52
N_{21}	n	100	Sol-Gel	0.60	0.06	248.50	6.30
N_{22}	n	100	Sol-Gel	0.60	0.06	122	5.80
N_{23}	n	100	Sol-Gel	0.60	0.06	323	6.10
P_{24}	n	100	Implant	0.60	0.06	37.60	7.30
P_{25}	p	100	Implant	0.60	0.06	50.80	6.90
P_{26}	p	100	Sol-Gel	0.60	0.06	191.40	5.80
P_{27}	p	100	Sol-Gel	0.60	0.06	120.30	5.87

TABLE 5. Average sheet resistances for the Al, and phosphorous and boron diffusions for the 100 micron cells.

The first row in the table 4 is in bold to distinguish between the only 500 micron cell, N^1_{01}, and the remaining cells. In the subsequent tables, measurements for this cell are always in bold. In the first column of the tables, cells names are shown. the base corresponds to the type of the cell, the subscript indicates the cell number and the superscript indicates the surface condition of the wafer (1=one-side polished wafer, 2=double-side polished wafer). Names without superscript correspond to 100 micron double-side polished cells.

Considering the results in the above tables, one can observe the following trends: (1) as aluminum thickness increases, its sheet resistance decreases. This will result in lower series resistance associated with metallization in the dark I-V measurements.

(2) The average sheet resistance of ion-implanted boron layers in n-type substrates is lower than that of the ion-implanted layers in p-type substrates. This is most probably due to a different value of diffusivity of boron in an n-type substrate from that in p-type substrates.

(3) among the boron sol-gel diffused cells, the values of average sheet resistances for n-type cells are often higher than for p-type cells and this could be due to the brown stain problem in case of n-type cells as discussed in the chapter 3, section 3.2.

(4) in the case of phosphorous, the average sheet resistance values in p-type cells are lower than in n-type cells and this is again due to different values for diffusivity of phosphorus in n- and p-type substrates.

5- The average sheet resistance of ion-implanted boron layers is usually much lower than that of sol-gel diffused boron layers.

The average conductivities of these diffused layers can be found using the measured sheet resistance and then their corresponding surface concentrations can be estimated, using Irvin's curves for n-and p-type Gaussian diffusion profiles, shown in the Appendix A [33]. The average conductivity of diffused layers is obtained from the following equation [33]

$$\sigma = \frac{1}{R_{Ave,sht} x_j} \tag{4.1}$$

where, σ is average conductivity of the diffused layer in $(\Omega cm)^{-1}$, $R_{Ave,sht}$ is average sheet resistance of the diffused layer in [$\Omega/\square$), and x_j is the junction depth of the diffused layer in [cm].

The values for the average sheet resistance, junction depth, average conductivity, and surface concentration are summarized in Table 6.

Diffused layer in n-type substrate	$R_{Ave.sht}$ ($\Omega/\square$)	X_j (cm)	σ_{Ave} $(\Omega/\square)^{-1}$	Estimated surface concentration from Irvin's curves	Estimated surface concentration form simulation
Phosphorus	7	2.2×10^{-4}	650	$> 10^{20}$	2×10^{20}
Boron (implant)	25	2.8×10^{-4}	142	6×10^{19}	3.5×10^{19}.
Boron (sol-gel)	270	3.6×10^{-4}	10.30	2×10^{18}	1×10^{20}

TABLE 6. The estimated surface concentration for phosphorus and boron diffused layers in the n-type substrate.

In this table, the values for the junction depth are extracted from figures 3.2, 3.3, 3.1, respectively. Except for the case of boron diffused regions (using sol-gel technique), the estimated surface concentrations from the Irvin's curves and simulations are in good agreement. The discrepancy between the values of surface concentrations in the case of boron sol-gel diffusion could be due to the brown stain problem which increases the resistivity of the diffused layer and thus reduces the average conductivity and the surface concentration of this diffused layer.

It should be mentioned that surface concentrations are important in case of making ohmic contacts between aluminum and n-and p-type silicon wafers. A minimum surface concentration of 5×10^{19} cm^{-3} is required to make good ohmic contact between aluminum and n-type silicon wafer and in case of p-type silicon wafers, the surface concentration should be about 10^{19}.

4.1.2 N- and P Contacts

Figure 4.1 shows a typical I-V characteristic of n-type contacts. This measurement is done with HP 4145 Semiconductor Parameter Analyzer by probing the two closest pads on their respective contact test structures and sweeping the applied voltage between the pads.

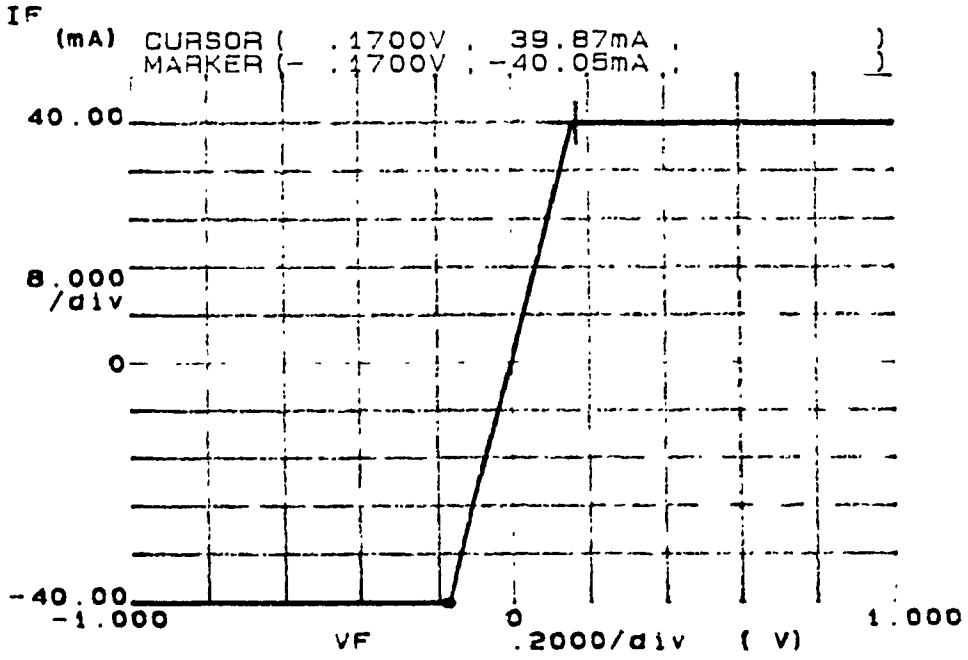


Figure 4.1: I-V plot for n-type ohmic contacts.

The voltage is swept from -0.17 to 0.17 volts and the corresponding currents at each point are -40.05 and 39.87 mA. Since the I-V curve is linear and the magnitude of current for a given positive and negative voltage bias is the same, it can be con-

cluded that n contacts are ohmic contacts.

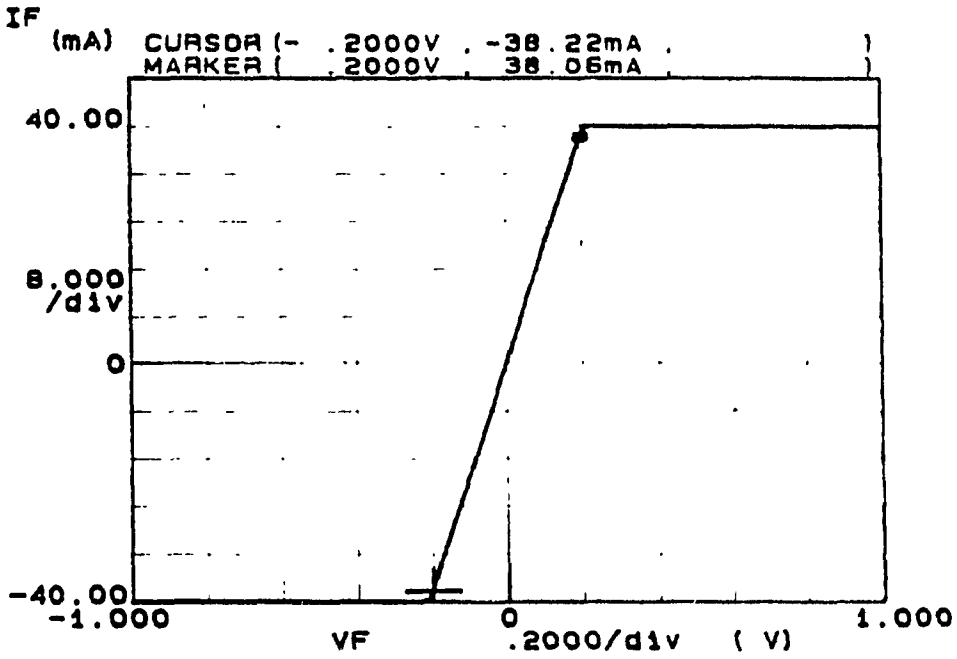


Figure 4.2: I-V plot for p-type ohmic contacts in the case of a boron implanted cell.

Similarly, figure 4.2 shows the same measurements for implanted p-type contacts. The voltage is swept from -0.2 to 0.2 volts and the corresponding currents at each point are -38.22 and 38.06 mA. Results demonstrate that boron-implanted p contacts are also good ohmic contacts.

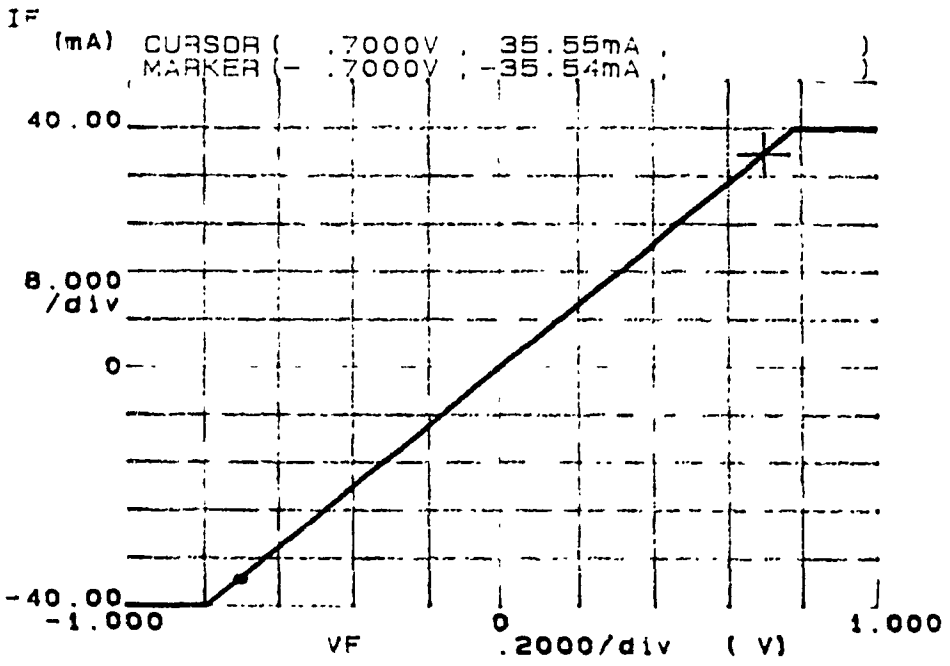


Figure 4.3: I-V plot for p-type ohmic contacts in case of boron sol-gel diffused cell.

Figure 4.3 shows the I-V plot for sol-gel diffused p-type contacts. Although the contact resistance is higher than that of implanted cells, it is still an ohmic contact.

Having found the values for the sheet resistances of the metallized and diffused layers, in the following pages the values for the n and p contact resistances and the resistance of the metallized layer are estimated. These results are used to find an estimated value for the overall series resistance of the cells.

4.1.3 Bulk and Contact Resistances

The p and n contact structures shown on mask#4 are used to measure the values of the corresponding ohmic contacts. The value of the bulk resistance is calculated using the sheet resistances of the diffused layers. The procedures are shown in the Appendix B. The following table shows the values of the bulk and contact resistances for different groups of 100 micron cells..

Cell ID	Boron technique	R_{cn} (Ω)	R_{cp} (Ω)	R_{bulk} (Ω)
N_{17}	Implant	0.05	0.05	0.90
N_{18}	Implant	0.05	0.05	0.90
N_{19}	Implant	0.04	0.05	0.89
N_{20}	Sol-Gel	0.04	0.05	0.91
N_{21}	Sol-Gel	0.05	0.07	1.03
P_{24}	Implant	0.05	0.06	0.48
P_{27}	Sol-Gel	0.04	0.09	0.52

TABLE 7. The bulk and contact resistances.

As discussed earlier in this chapter, the n and p contacts are ohmic contacts and according to the results shown in table 7, the contact resistances are very low and almost negligible. However, the bulk resistances for both n- and p-type substrates are high due to the high resistivities of the initial materials. The bulk resistance for the p-type cells is lower than that of n-type cells and this is due to lower resistivity for the p-type wafers.

4.1.4 Metallization Resistance

The thickness of aluminum deposited on the all 100 micron thick cells, is about 0.6 microns as shown in the table 5. The contribution of metallization resistance to the device's overall series resistance can be approximated by adding the resistance of the metal lines connecting the n and p pads to their respective bus bars and by adding to this result the resistance of the bus bars themselves [16]. The metallization resistance may be approximated as:

$$R_{Al} = R_{Ave,sht}Al\ [area(n\text{-}pad)+area(p\text{-}pad)+area(n\text{-}bus)+area(p\text{-}bus)]$$

where the value for the average sheet resistance for the aluminum with 0.6 micron is shown in the table 5 (~0.06 Ω/❑) and the dimensions of the structures are as follows:

line to n-pad: L=2340 μm, n-bus bar: L=9860 μm
W=300 μm, W=300 μm

line to p-pad: L=3380 μm, p-bus bar: L=10060 μm
W=300 μm, W=300 μm

R_{Al}=0.06 Ω/❑ [2340/300 ❑+3380/300 ❑+9860/300 ❑+10060/300 ❑]=5.12 Ω

As discussed in the chapter 2 section 2.2.2, the total series resistance of a cell is due to the contact resistances, the resistance of the bulk, and the resistance of the

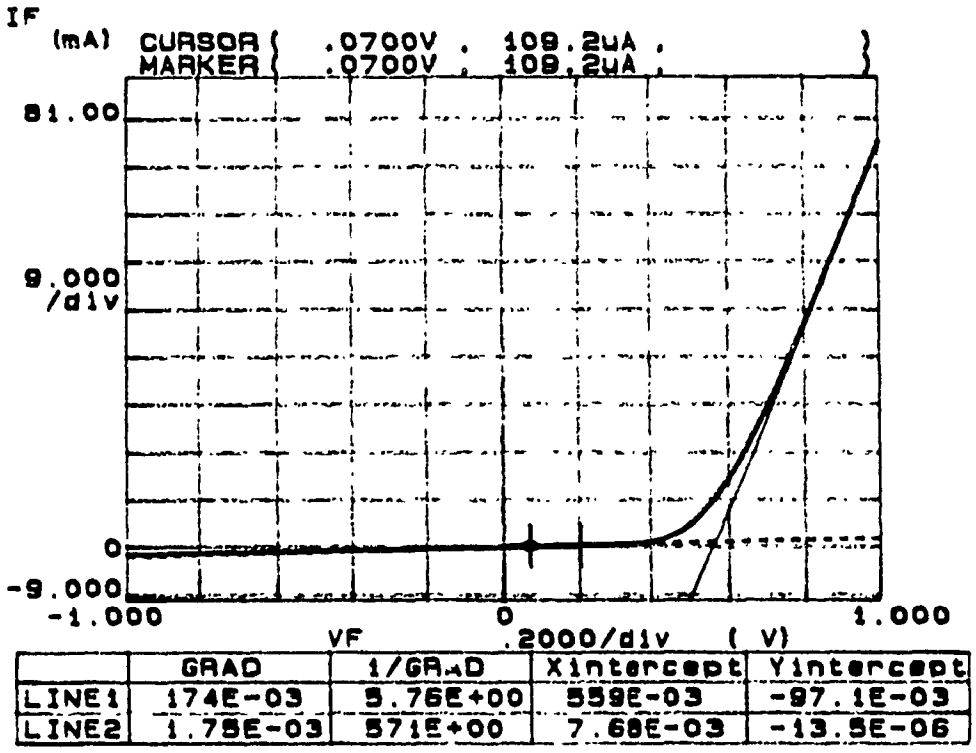
metal itself. Therefore, the estimated overall series resistance of the 100 micron cells would be in the range of 6 to 7 ohms. So, the overall series resistance in these cells is not as low as it should be (lower than 1 Ω would be desirable, see section 2.4 in Chapter 2). Series resistances this high will have substantial detrimental impact on solar cell fill factor, and thus on the cell efficiency as will be discussed later in Chapter 6. However, it is encouraging that the high series resistance is found to be not due to the surface concentration or ohmic contacts but due to the metal thickness.

In view of the "proof of concept" nature of this study, this is encouraging, since this problem could be straightforwardly solved if such solar cells were to be mass-produced.

4.2 Dark I-V Characteristics

All the cells were characterized under dark conditions with HP 4145 Semiconductor Analyzer. The following figure shows the dark I-V characteristics for the cell P_{24} and illustrates the methods by which the values of series and shunt resistances

are obtained.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	174E-03	5.76E+00	559E-03	-97.1E-03
LINE2	1.75E-03	571E+00	7.68E-03	-13.5E-06

Figure 4.4: The dark I-V characteristics for the cell P_{24}.

The cell's series resistance is obtained from the slope of the I-V characteristic in the forward linear region of operation where the series resistance dominates. The shunt resistance value is obtained from the slope of the I-V characteristic in the forward region in the vicinity of the origin. The table in the caption of figure 4.4 represents various parameters. In this table, LINE1 corresponds to the solid line which is tangent to the I-V curve in the linear region, LINE2 corresponds to the dashed line which is tangent to the I-V curve near the origin, the second column shows the value

of slopes for these two lines and the third column illustrates the reciprocal of these slopes which are the values of series and shunt resistances. These values for the sample P_{24} are R_s=5.76 Ω and R_{sh}=571 Ω respectively. Finally, the fourth and fifth columns correspond to the intercepts of the slopes with the x and y axes.

4.2.1 Reverse Saturation Current, I_s, Ideality Factor, A

To measure the reverse saturation current and the ideality factor of the cells, the following technique is used:

The I-V characteristic of a diode is described by the following equation:

$$I = I_s\left(e^{\frac{qV}{AkT}} - 1\right) \tag{4.2}$$

where, I_s and A, are reverse saturation current and diode ideality factor respectively. When the applied voltage approaches the values greater than few kT/q, then the equation can be approximated as:

$$I = I_s\left(e^{\frac{qV}{AkT}}\right) \tag{4.3}$$

or

$$Ln(I) = \frac{qV}{AkT} + Ln(I_s) \tag{4.4}$$

This equation indicates that Ln (I) is a linear function of the applied voltage, V, and

that the slope of the curve in the linear region is q/AkT, in which the value of q/kT at a given temperature is known. Thus, the value of the ideality factor, *A*, can be calculated. Moreover, this equation indicates that when the applied voltage is zero, Ln(I_s)will be equal to Ln(I) or, in other words, I_s will be equal to I. Thus in the Ln(I) vs. V curve, the intercept of the curve (for large value of V) with Ln(I) axis gives the reverse saturation current.

Figure 4.5 demonstrates the Ln(I)-V plot for the cell P_{24} from which the values of reverse saturation current and the ideality factor may be determined.

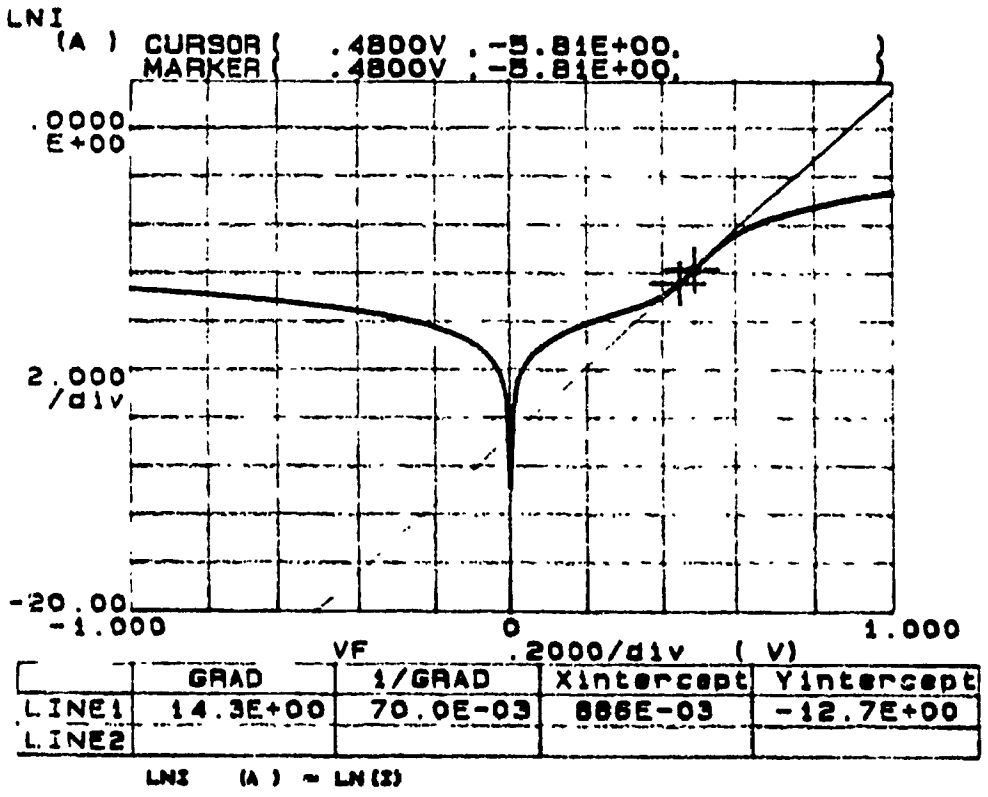


Figure 4.5: The Ln current-voltage plot for the cell P_{24}.

In the figure 4.5, the left part of the curve between 0 and -1 volts corresponds to the generation current within the depletion region when the device is in the reverse biased mode. In the right part of the curve between 0 and +1 volts, the different components of the current for the forward bias regime are shown. Considering figure 4.5, in the forward bias mode there are three different regions as follows:

(1) the region between 0 and 0.2 volts in which the value of the current is low due to the low value of the applied voltage. The current component in this region is due to the recombination of the carriers within the depletion region and it is referred to as the recombination current.

(2) the next current component is the diffusion current for the applied voltages between 0.2 and ~ 0.6 volts. This is the region where the Ln(I) is a linear function of the applied voltage and the line in the figure 4.5 is tangent to the curve in this region of the curve.

(3) the last current component is the injection current for the applied voltages higher than 0.6 volts. Referring to the equation 2.8, it is clear that, as the value of the applied voltage increases, the effect of the series resistance on the current starts and this effect can be seen in the figure 4.5 in part of the curve with voltages higher than 0.6 volts. The values for the reverse saturation current and the ideality factor obtained from the above curve, are $3x10^{-6}$ and 2.7 respectively.

Tables 8 and 9 summarize the estimated parameters from the I-V characteristics of various samples. Corresponding measured resistivity, series resistance, and shunt resistance of the samples are also included in these tables.

CELL	TYPE	ρ Ω-cm	BORON	Al μm	R_S Al Ω/❑	I_S(A)	*A*	R_S (Ω)	R_{sh} KΩ
N^1_{01}	**n**	**8**	**Sol-Gel**	**0.30**	**0.12**	**$8.58x10^{-10}$**	**1.25**	**10.50**	**13.50**
N^1_{02}	n	8	Implant	0.50	0.06	$4.50x10^{-8}$	1.70	7.75	7.20
N^1_{03}	n	8	Implant	0.30	0.13	$6x10^{-10}$	1.23	10.40	14.50
N^2_{04}	n	11	Implant	0.40	0.10	$3.70x10^{-6}$	2.85	8.4	1.20
N^2_{05}	n	11	Implant	0.40	0.10	$3.05x10^{-7}$	2.14	8.15	7.5
N^2_{06}	n	11	Implant	0.30	0.12	$1.50x10^{-8}$	1.60	10	10
N^1_{07}	n	8	Sol-Gel	0.40	0.09	$1.24x10^{-7}$	1.60	8.30	8
N^1_{08}	n	8	Sol-Gel	0.40	0.09	$3.70x10^{-5}$	2.36	9.20	0.60
N^2_{09}	n	11	Sol-Gel	0.30	0.11	$3.73x10^{-7}$	1.98	10.70	7.4
N^2_{10}	n	11	Sol-Gel	0.30	0.11	$3x10^{-9}$	1.40	10	13.20
N^2_{11}	n	11	Sol-Gel	0.30	0.11	$6x10^{-10}$	1.12	8.30	15.60
P^2_{12}	p	5.40	Implant	0.30	0.12	$1.50x10^{-5}$	3.54	12.80	0.30
P^2_{13}	p	5.40	Implant	0.30	0.15	$1.12x10^{-7}$	2	11.30	2
P^2_{14}	p	5.40	Implant	0.30	0.14	$1.03x10^{-4}$	5.14	12.20	0.40
P^2_{15}	p	5.40	Sol-Gel	0.30	0.13	$1.13x10^{-4}$	4.82	12.80	0.39
P^2_{16}	p	5.40	Sol-Gel	0.40	0.10	$6.10x10^{-5}$	4.45	8.20	0.43

TABLE 8. Dark I-V characteristics of 500 and 300 micron solar cells.

CELL	TYPE	ρ Ω-cm	BORON	Al μm	R_S Al Ω/❑	I_s(A)	*A*	R_s (Ω)	R_{sh} KΩ
N_{17}	n	11	implant	0.60	0.06	$3x10^{-5}$	3.33	6.09	1.22
N_{18}	n	11	implant	0.60	0.06	$5.40x10^{-5}$	3.90	6.75	0.50
N_{19}	n	11	implant	0.60	0.06	$5x10^{-6}$	3	6.11	3.28
N_{20}	n	11	sol-gel	0.60	0.06	$4.90x10^{-5}$	4.10	6.26	0.53
N_{21}	n	11	sol-gel	0.60	0.06	$6.80x10^{-6}$	2.90	6.61	2.80
N_{22}	n	11	sol-gel	0.60	0.06	$3.70x10^{-5}$	3.42	6.51	0.94
N_{23}	n	11	sol-gel	0.60	0.06	$1.80x10^{-5}$	2.70	6.82	1.25
P_{24}	p	5.6	implant	0.60	0.06	$3x10^{-6}$	2.7	5.76	0.57
P_{25}	p	5.6	implant	0.60	0.06	$1x10^{-4}$	4.10	6.50	0.21
P_{26}	p	5.6	sol-gel	0.60	0.06	$1.56x10^{-4}$	4.90	6.28	0.26
P_{27}	p	5.6	sol-gel	0.60	0.06	$2.61x10^{-4}$	4.68	6.11	0.21

TABLE 9. Dark I-V characteristics of 100 micron solar cells.

There are many features which can be observed in Tables 8 and 9, summarized below, and subsequently explained. The judgements here are based on the discussion of p-n junction and solar cell quality outlined in chapter 2, section 2.4. The ideality factor, *A*, needs to be as near to 1 as possible, and is acceptable up to about 2, the reverse saturation current, I_s, is acceptable in the range of microampere or lower, the series resistance, R_s, has to be less than 1 Ω, and the shunt resistance, R_{sh}, as high as possible (few KΩ or higher).

The best dark I-V parameters for different groups of cells (with 300 micron thickness) shown in table 8, are summarized as follows:

N-type one-side polished cells having the best dark I-V characteristics:

N^1_{03} (Implant): has an excellent I_s ($6x10^{-10}$ A), very good *A* (1.23), very good R_{sh} (14.50 KΩ), but R_s is too high (10.40 Ω).

N^1_{01} (sol-gel): has an excellent I_s ($8.58x10^{-10}$ A), very good *A* (1.25), very good R_{sh} (13.5 KΩ), but R_s is too high (10.50 Ω).

N-type double-side polished cells having the best dark I-V characteristics:

N^2_{06} (Implant): has an excellent I_s ($1.5x10^{-8}$ A), good *A* (1.60), very good R_{sh} (10 KΩ), but R_s is too high (10 Ω).

N^2_{11} (sol-gel): has an excellent I_s ($6x10^{-10}$ A), excellent *A* (1.12), very good R_{sh} (15.60 KΩ), but R_s is too high (8.30 Ω).

P-type double-side polished cells having the best dark I-V characteristics:

P^2_{13} (Implant): has a good I_s ($1.12x10^{-7}$ A), satisfactory *A* (2), low R_{sh} (2 KΩ), R_s is too high (11.30 Ω).

P^2_{16} (sol-gel): has high I_s ($6.10x10^{-5}$ A), very bad *A* (4.45), very low R_{sh} (0.43 KΩ), R_s is too high (8.20 Ω).

In the following, the average dark I-V characteristics are summarized for different groups of cells (with 300 micron thickness) shown in table 8.

Implanted one-side polished n-type cells:

excellent I_s ($5x10^{-9}$ A) very good A (1.50) very high R_s (9.10 Ω)

very good R_{sh} (10.85) KΩ

Implanted double-side polished n-type cells:

good I_s ($3.7x10^{-7}$ A) high A (2.2) very high R_s (8.85 Ω)

good R_{sh} (6.23 KΩ)

Sol-gel diffused one-side polished n-type cells:

good I_s ($3.4x10^{-6}$ A) satisfactory A (1.74) very high R_s (9.40 Ω)

good R_{sh} (7.4 KΩ)

Sol-gel diffused double-side polished n-type cells:

excellent I_s ($3.3x10^{-8}$ A) very good A (1.5) very high R_s (10.0 Ω)

very good R_{sh} (12 KΩ)

Implanted double-side polished p-type cells:

high I_s ($5x10^{-5}$ A) very high A (3.57) very high R_s (11.75 Ω)

low R_{sh} (1.2 KΩ)

Sol-gel diffused double-side polished p-type cells:

high I_s ($5.5x10^{-5}$ A) very high A (4.63) very high R_s (10.50 Ω)

very low R_{sh} (0.41 KΩ)

The best dark I-V parameters for different groups of cells (with 100 micron thickness) shown in table 9, are summarized as follows:

N-type double-side polished cells with the best dark I-V characteristics:

N_{19} (Implant): satisfactory I_s ($5x10^{-6}$A) very high A (3) low R_{sh} (3.28 KΩ) very high R_s (6.11 Ω)

N_{21} (sol-gel): satisfactory I_s ($6.8x10^{-6}$A) very high A (2.9) low R_{sh} (2.80 KΩ) very high R_s (6.61 Ω)

P-type double-side polished cells with the best dark I-V characteristics:

P_{24} (Implant): very low I_s ($3x10^{-6}$ A) very high A (2.70) very low R_{sh} (0.57 KΩ) very high R_s (5.76 Ω)

P_{26} (sol-gel): very low I_s (1.5610^{-4} A) very high A (4.90) very low R_{sh} (0.26 KΩ) very high R_s (6.28 Ω)

In the following, the average dark I-V characteristics are summarized for different groups of cells (with 100 micron thickness) shown in table 9.

Implanted double-side polished n-type cells:

high I_s (2.8×10^{-5} A) very high A (3.41) very high R_s (6.32 Ω)

low R_{sh} (1.7 KΩ)

Sol-gel diffused double-side polished n-type cells:

high I_s (4.5×10^{-5} A) very high A (3.28) very high R_s (6.60 Ω)

low R_{sh} (1.4 KΩ)

Implanted double-side polished p-type cells:

very high I_s (10^{-4} A) very high A (4.10) very high R_s (6.50 Ω)

very low R_{sh} (0.21 KΩ)

Sol-gel diffused double-side polished p-type cells:

very high I_s (2×10^{-4} A) very high A (4.80) very high R_s (6.20 Ω)

very low R_{sh} (0.24 KΩ)

Considering the values of the parameters in the tables 8 and 9, one can reach the following conclusions:

(1) In the case of n-type, 300 micron-thick cells, with few exceptions, most of the ideality factors, reverse saturation currents, and shunt resistances are excellent, for both sol-gel diffused and implanted cells. This indicates that the conditions under which the cells are fabricated was satisfactory (for a good diode the value of the ideality factor should be close to 1 as discussed in section 2.4, and the value of reverse saturation current should be in the range of 1 microampere or lower). This is true for both implanted and sol-gel diffused boron. However, in the case of 100 micron cells (both n- and p-type) and 300 micron p-type cells, the values of the ideality factors are much higher. This indicates that there are many trap centers available within the p-n junction depletion region. The increase in the values of ideality factors has caused a very fast increase for the values of the reverse saturation currents in these cells. Knowing that both groups of cells are processed under the same conditions, one may relate the origin of the problem to the original wafers. It is likely that in the original wafers there is a high concentration of trap centers which act as recombination centers and thus increases the reverse saturation current.

(2) As the value of reverse saturation current increases, the value of the shunt resistance decreases. This is due to the reduced junction barrier height as discussed in the section 2.2.2.

(3) The values of series resistance vary from 5.7 Ω to 12.8 Ω for all cells. Earlier in the chapter 2, it was discussed that a value of series resistance greater than 1 Ω will result in more rounded I-V curve for the cell under illumination and thus reduces the fill factor. Therefore, one expects a rather low fill factor for these cells and particularly in the case of 100 micron thick cells, the value of this parameter should be even lower, compared with the 300 micron cells, due to the lower value for the shunt

resistances for these cells.

(4) In the case of 100 micron cells, the values of the series resistances are in the ranges between 6 to 7 ohms and as discussed in the section 4.1.4, the reason for high series resistance for these cells is the high resistance of the metal path itself.

As a summary, the dark I-V parameters of the cells indicate that (1) the p-n junction process was satisfactory. (2) 300 micron p-type and 100 micron wafers were not as pure as 300 micron n-type wafers (3). The high series resistance for these cells is due to the metal thickness. (4) Due to high values for series resistances (for all cells) and low values for shunt resistances (for 100 micron cells), one expects a low fill factor for these cells under illumination.

CHAPTER 5

Creation and Characterization of Anti-Reflection Coatings

As a part of this work, two different anti-reflection (AR) coatings are created on the front surface of the cells and their corresponding reflectivities are investigated. The two coatings investigated are silicon dioxide and porous silicon. This chapter explains the experimental procedures for the formation of each layer in detail and discusses their corresponding reflectivities. The reflectivities of these layers were measured at Ecole Polytechnique, using the light spectrometer, Perkin Elmer λ_{19}.

5.1 Silicon Dioxide as an AR Coating

An SiO_2 layer having thickness ~1100 Å on the front surface of the cells acts as an AR coating. Immediately after the 1-hour phosphorus pre-deposition at 1000 °C in a nitrogen ambient (see step A.4.2 in Appendix A), the ambient was changed to oxygen for 13 minutes to grow a layer of oxide with thickness of ~1100 Å. Figure 5.1 compares the reflectivities of the bare silicon and a ~1100 Å-thick oxide layer on

one of the cells, as a function of illuminated light wavelength. As it is obvious from the curves, the bare silicon reflects between 50% and 30% of photons having wavelengths between 400 nm and 1000 nm respectively. The silicon dioxide, on the other hand, reflects on average only 15% of the photons in the same range of wavelengths.

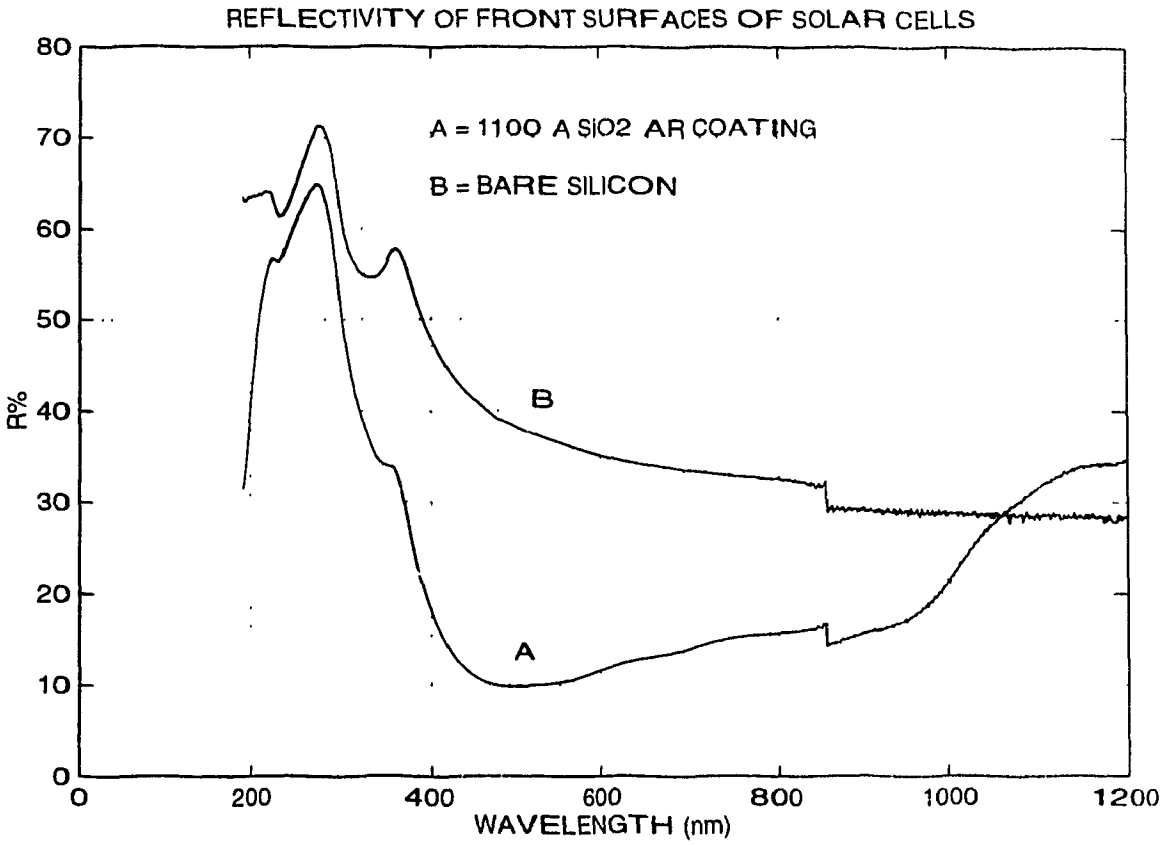


Figure 5.1: Reflectance curves for bare and SiO_2 coated silicon.

5.2 Porous Silicon as an AR Coating

The experimental setup for the formation of porous silicon on the front surface of the cells was schematically shown in figure 3.4. All the experiments regarding porous silicon formation were done at the Ecole Polytechnique, in the MODFAB

Lab. Before optimizing the reflectivity of the porous silicon, some preliminary experiments were done and the results are shown in Figure 5.2.

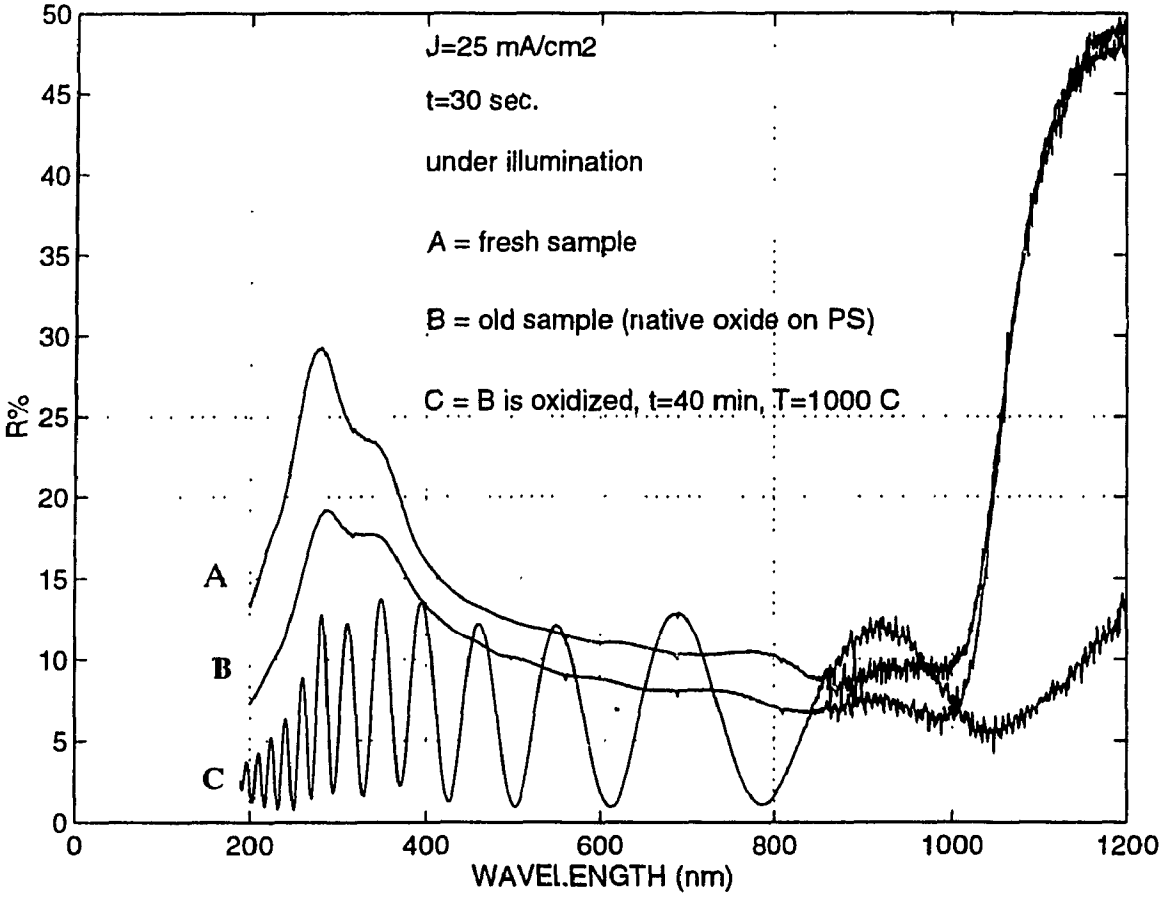


Figure 5.2: Reflectivity of porous silicon, A-as prepared, B- after a few weeks, C-after subsequent high-temperature oxidation.

Figure 5.2 shows the reflectivities of porous silicon layers formed on an n-type silicon wafer as a function of light wavelength. Different measurements were done on the sample right after porous silicon formation (fresh sample), after few weeks (old sample), and also after high temperature oxidation. The porous layer was formed by current density of 25 mA/cm^2 for 30 seconds, under a 100 watt light bulb. As was explained in Chapter 2, for the formation of porous silicon layer on the n-

type silicon wafers, the presence of light is necessary in order to provide minority hole carriers.

The curve A in the figure corresponds to the reflectivity of a fresh porous silicon layer formed on an n-type silicon wafer. It shows an average reflectivity of ~ 12% in the range between 400 and 1000 nm. The reflectivity of the sample was re-measured after few weeks (the curve B), and its value had decreased by about 25% for the whole wavelength range. This is due to the formation of a layer of thin native oxide (~ 30 Å) on the top of the porous layer. In this case both the porous silicon layer and the thin oxide layer on top of it act as a double AR coating and therefore the reflectivity drops further. This phenomena indicates that the aging effect not only does not deteriorate the reflectivity of the porous layer formed on the front surface of the cell, but may improve the performance of the cell due to lowering of reflectivity at its front surface. The effect of a layer of thick oxide (~ 2500 Å) on the reflectivity of the porous layer is shown by the curve C in Figure 5.2. A layer of thick oxide reduces the reflectivity even further. The appearance of fringes in the reflectance curve is due to the constructive and destructive interferences between the reflected light beams from the top and the bottom of the thick oxide layer.

5.2.1 Porous Silicon on the Front Surface of an IBC Cell

To make a porous silicon layer on the front surfaces of the cells, some problems arose associated with the metal structure on the rear surface of the cells. The porous layers formed on the front surfaces of both n- and p-type cells, were considerably non-homogeneous with high reflectivities (about 12% in the visible range). In an attempt to obtain a homogeneous porous layer with low reflectivity, experiments at different current densities and etching times were performed. No satisfactory result was achieved.

It was observed that the porous layer did not form at low current densities (≤ 5 mA/cm^2). As the value of current density was increased, the porous layer started to form in some specific points at the surface. By inspection, it was found that the porous layer was formed only in the area directly facing the metal contacts on the back side of the cell. An increase in the value of current density did not improve the uniformity of the features formed on the front surface of the cell.

The electrochemical etching time was varied as well. Increasing the time of electrochemical etching caused some improvements. However, the porous layer still was non-homogeneous and its reflectivity was about 10% at wavelengths between 200 and 1200 nm.

Figure 5.3 shows the layout of the backside of the solar cell in which the areas with the gray color are covered with the aluminum. The square region on the upper left corner of the figure corresponds to the cell's active area in which p- and n-diffused fingers are located, and where the porous layer on the front surface of the cell will be formed (facing this structure).

As discussed in Appendix A, during the fabrication of cells, prior to metallization, windows were opened in the oxide covered n- and p-type fingers to make the

contacts between the aluminum and silicon. These contacts are small areas, in order to decrease the concentration of trap centers usually present at the interface between these two materials. The areas in which the aluminum is in direct contact with the silicon are shown in figure 5.4. In this figure, the small squares on the upper left corner correspond to the areas through which the aluminum is in contact with the bare silicon.

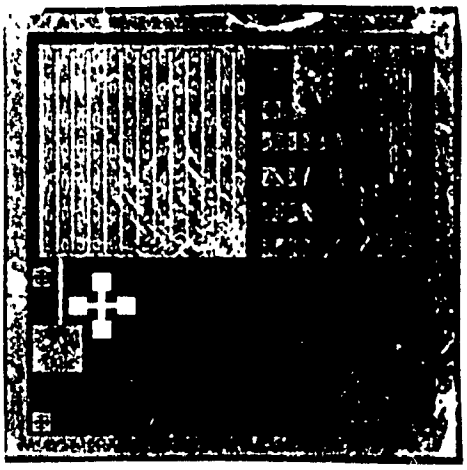


Figure 5.3: The layout of the IBC solar cell.

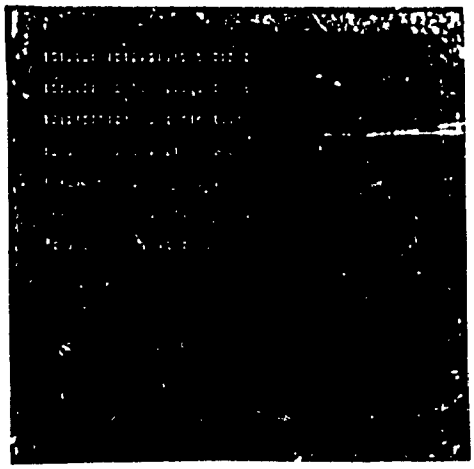


Figure 5.4: The areas through which the aluminum is in contact with the bare silicon in the back side of the solar cell.

During the formation of a porous silicon layer, current passes through these contact areas. The porous layer forms on the front surface of the cell, only at the locations where the current reaches the front surface. Therefore, the porous layer on the front surface of the cell will be created in a pattern similar to the one on the back side of the cell. Figure 5.5 shows the pattern of a porous layer formed on the front surface of one of the cells under the following conditions: current density (J) = 40 mA/cm^2, etching time (t) = 30 sec., and the experiment was done under a 100 watt light bulb.

Figure 5.5: The structure of the porous silicon layer formed on the front surface of an IBC solar cell under the following conditions: J=40 mA/cm^2 t=30 sec., under a 100 watt light bulb.

In this figure, the dotted brown pattern on the upper right corner corresponds to the regions where the porous silicon layer was formed on the front surface of a cell. This dotted pattern is the same as the pattern of Al/Si contacts shown in the upper left corner of figure 5.4. Therefore, it is obvious that the patterned nature of the back

contacts is an important cause of the inhomogeneity of the porous layer on the front surface of the IBC solar cell.

To eliminate this problem, more experiments were performed in which the value of the current density was kept the same but the etching time was varied. Not much improvement was observed. The above experiments were repeated for lower values of current densities and it was observed that, as the value of current density decreased and the time of electrochemical etching increased, the more area became porous on the front surface. Each backside contact point became a source for a larger porous area on the front side. The optimal (most uniform) porous silicon pattern obtained by varying the current and time is shown figure 5.6. These optimal values for the current density and the etching time were 25 mA/cm^2 and 300 sec. respectively and the experiment was performed under a 100 watt light bulb.

Figure 5.6: The optimized structure for the porous silicon layer formed on the front surface of an IBC solar cell under the following conditions: J=25 mA/cm^2, t=300 sec., under a 100 watt light bulb.

By comparing the structures shown for the porous silicon layers in figures 5.5 and 5.6, and also the conditions under which these layers are formed, one can discern to the following tendencies: a current density of 40 mA/cm^2 creates a strong electrostatic field across the wafer which accelerates the holes in a relatively straight path toward the front surface of the cell regardless of the etching time. Therefore, on the other side of the cell, the porous silicon forms only in the small areas facing the windows through which the current enters the cell (figure 5.5). However, when the current density is decreased (to 25 mA/cm^2), the applied electrostatic field is lowered and the holes will not be confined in a straight path and can spread laterally to the neighboring regions. As a result, larger area will be etched as shown in figure 5.6. The experiments were repeated for the longer etching time and for the various values of current densities under a 100 watt light bulb, No improvement in the uniformity of the porous silicon layer was observed over the optimum found in figure 5.6.

The reflectivities of these inhomogeneous porous silicon layers was measured to be high (~10%) as compared to uniform porous silicon.

In order to make the above discussion more clear and provide a better understanding about the origin of the problem, the idealized schematics of the porous silicon patterns formed on the front surfaces of the cells are shown in figures 5.7 and 5.8.

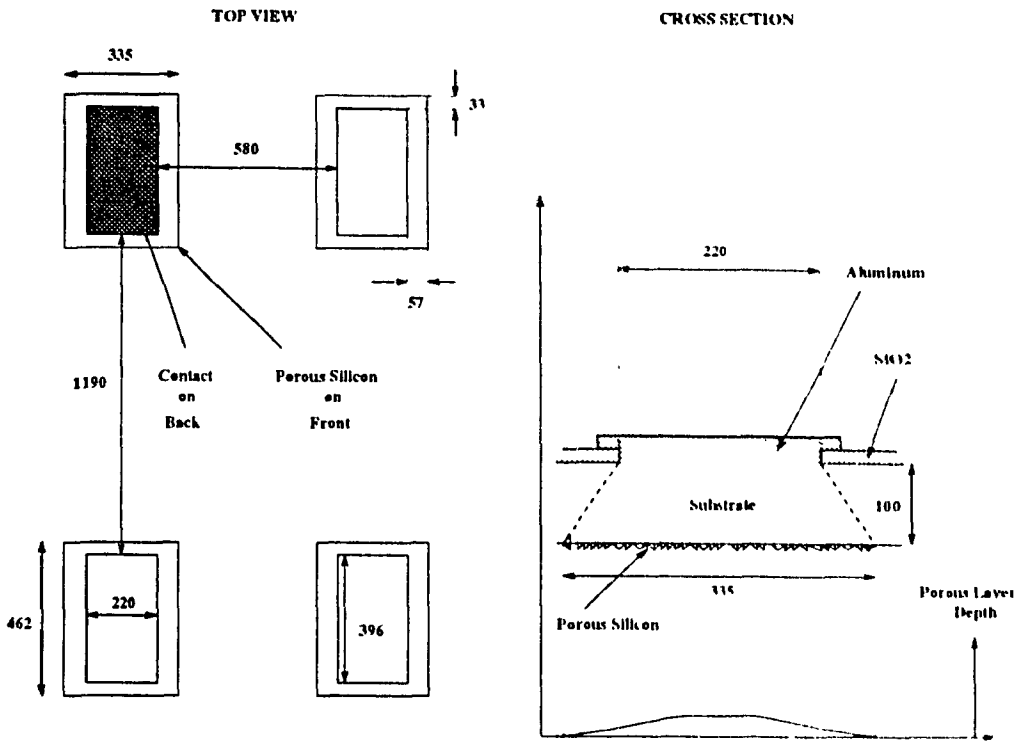


Figure 5.7: Idealized schematics of porous silicon patterns formed on the front surface of the p-type 100 micron thick cell (J=40 mA/cm^2, t=30 sec., under a 100 watt light bulb).

Figure 5.7 shows the idealized schematics of the porous silicon (outer rectangles) formed on the front surface of the IBC cell (units are in micron) under the following conditions: J=40 mA/cm^2, etching time of 30 sec. and under a 100 watt light bulb. The inner rectangles correspond to the contacts on the back side of the cell. As discussed earlier, a current density of 40 mA/cm^2 will create a strong electrostatic field across the cell which confines the holes and does not let them spread as much in their path towards the front surface of the cell. Therefore, the structure of the porous layer on the front side of the cell becomes similar to the contact structures on the back side of the cell and as shown in the above figure, the dimensions of the porous layers are comparable with the dimensions of the contacts.

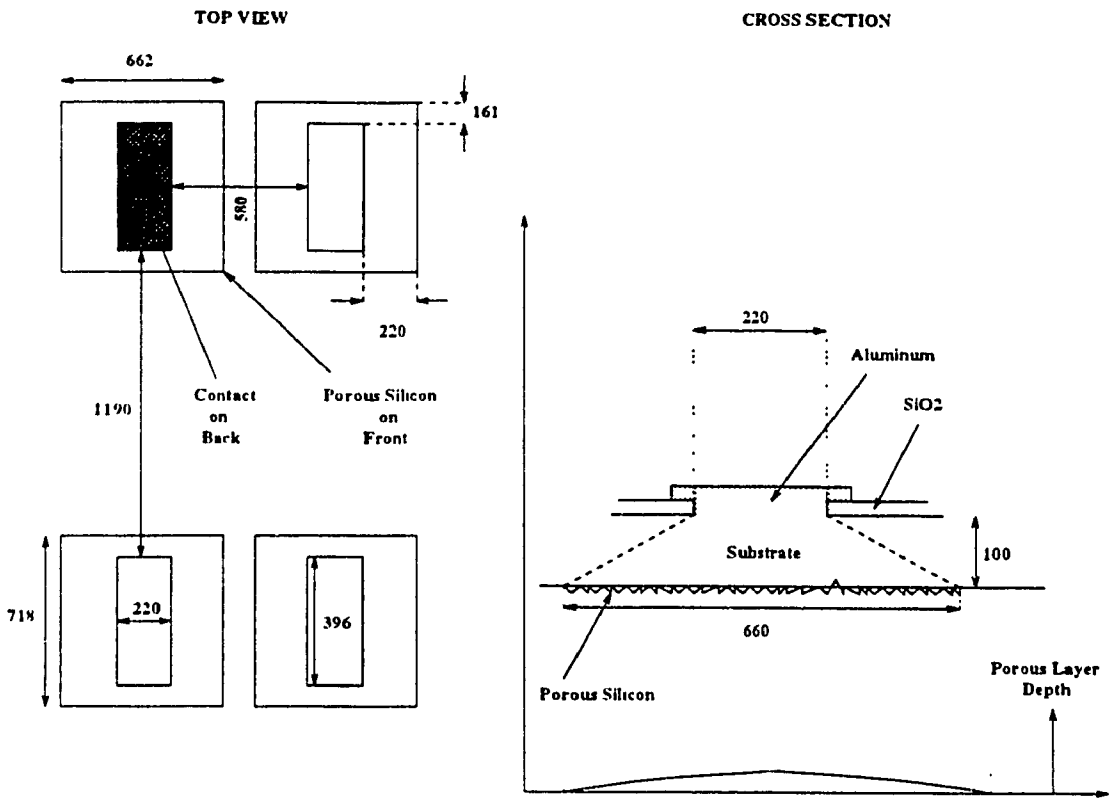


Figure 5.8: Idealized schematics of porous silicon patterns formed on the front surface of the p-type 100 micron thick cell (J=25 mA/cm^2, t=300 sec., under a 100 watt light bulb).

Figure 5.8 shows the idealized schematics of porous silicon formed on the front surface of a p-type 100 micron thick IBC cell. Both top and cross section views of the porous layers formed, indicate larger spread for the porous regions, compared to the structures shown in figure 5.7. This is due to the lower current density and longer etching time. As the applied current density decreases, the holes will be less confined by the electrostatic field and the longer etching time will let them spread more in their paths towards the front surface of the cell. Therefore, the regions of the porous silicon become larger.

Figures 5.9 and 5.10, show the optimized reflectivities for the porous layers formed on the front surfaces of both p- and n-type cells under a 100 watt light bulb.

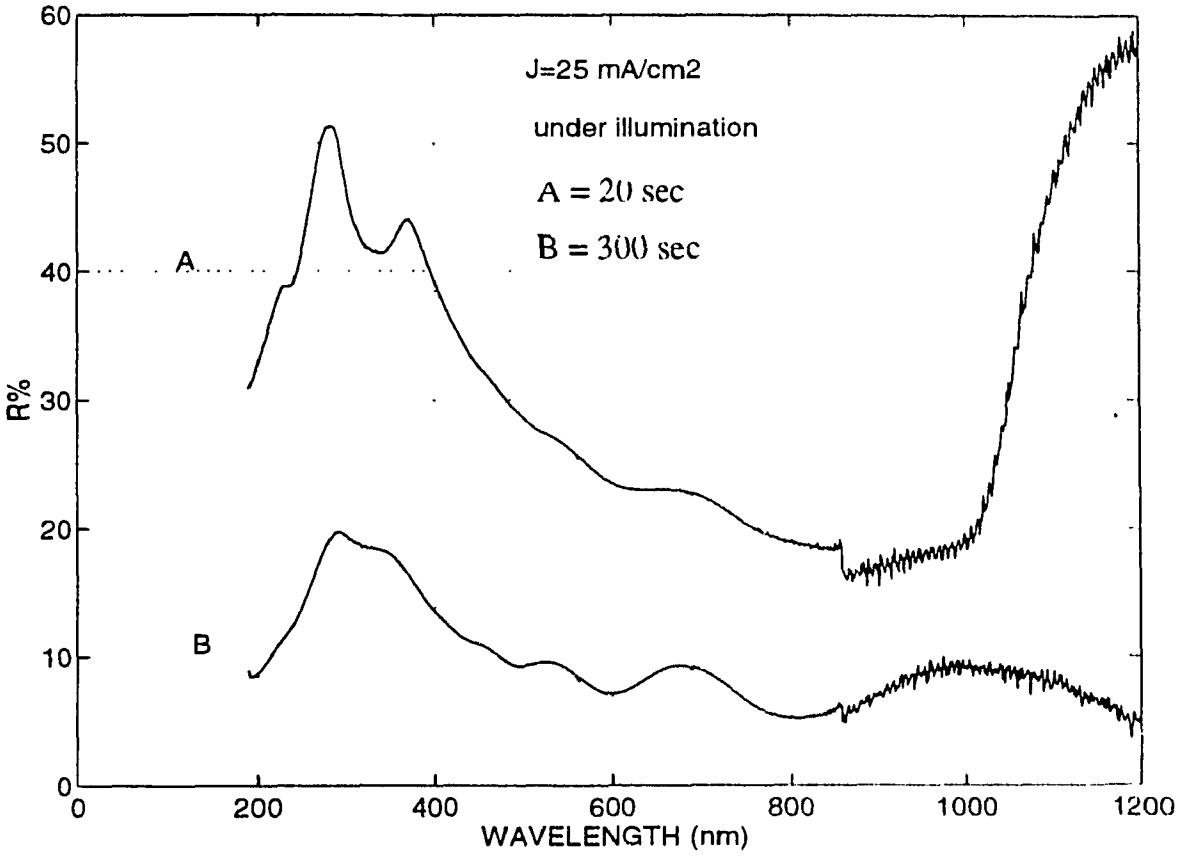


Figure 5.9: The effect of etching time on the reflectivities of the non-uniform porous silicon layers formed on the front surfaces of p-type cells with 300 micron thicknesses.

In figure 5.9, the curve B illustrates the reflectivity of the porous layer shown in the figure 5.6. As it is shown in this figure, the both porous layers are formed for the same current density of 25 mA/cm^2 and under illumination of a 100 watt light bulb. Only the etching time is different. The porous layer with the longer etching time, has lower reflectivity. Neither of these reflectivities is good. The high reflectivities are

due to the high non-uniform porous silicon formation, where much of the surface is not covered with the porous silicon.

Figure 5.10, shows the reflectivities of the porous silicon layers formed on the front surfaces of n-type cells.

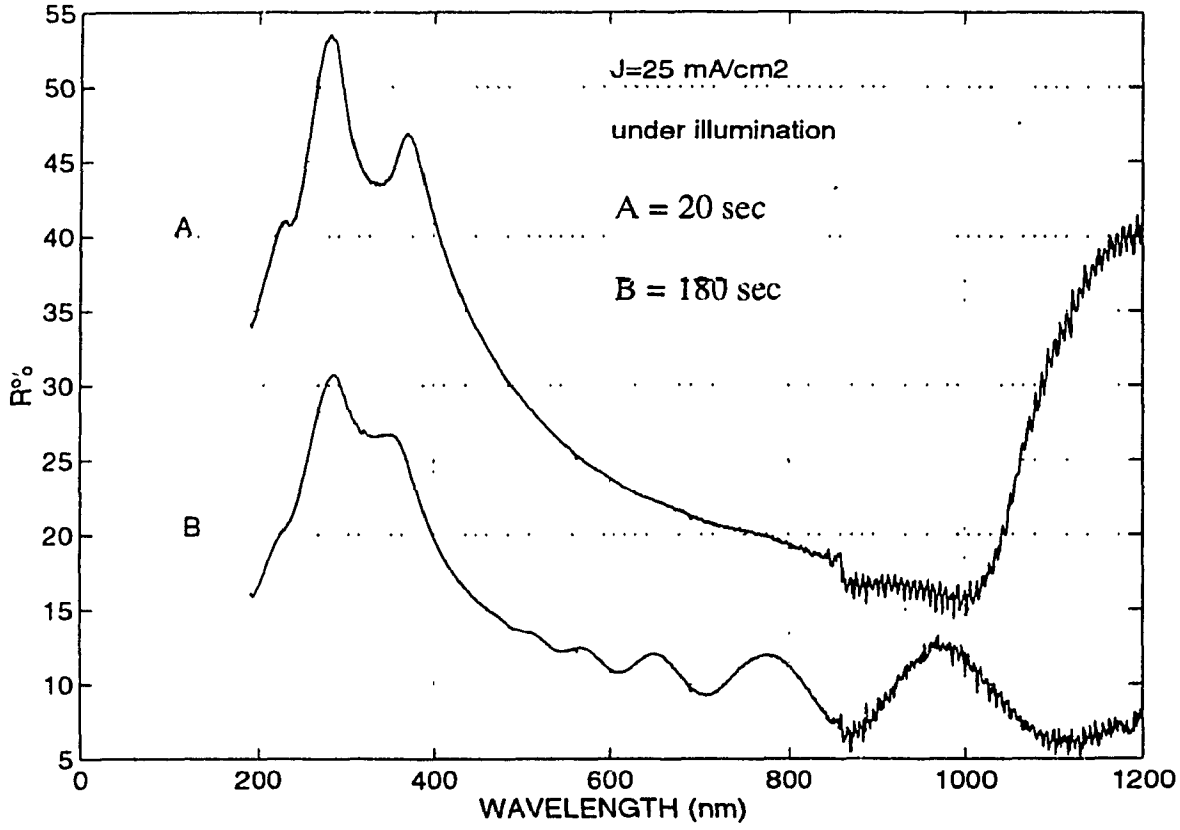


Figure 5.10: The effect of etching time on the reflectivities of the porous silicon layers formed on the n-type cells with 300 micron thicknesses.

The curves in figure 5.10 correspond to the reflectivities of the porous layers formed on n-type cells under the same conditions, except for different etching time for curve B. Like the p-type cells, the reflectivity of the porous layer also decreases as the etching time increases. It should be mentioned that the curves B in the both figures 5.9 and 5.10, correspond to the optimized reflectivities of the porous layers

formed on the front surfaces of p- and n-type cells under a 100 watt light bulb.

The results suggest that as the holes spread more at the front surface, a larger area will be etched which results in lower reflectivities for both n- and p-type cells. Therefore if one can supply holes uniformly to the front surface, a better pattern will be etched and the reflectivity of the surface will be reduced.

5.2.2 More Uniform Porous Silicon by UV Light

As discussed in the Chapter 2 section 2.3.2, the absorption coefficient of silicon increases with decreasing the photon wavelength and this results in generation of photo-carriers near the surface for high energy (short wavelength) photons. Therefore, in order to increase the concentration of holes near the surface, it was decided to perform the next experiments under ultra violet (UV) light instead of a 100 watt light bulb. By repeating the experiments under the UV light, the conditions for the formation of the porous layers on the front surfaces of both n- and p-type cells with 300 and 100 micron thicknesses were optimized. Considerably lower reflectivities were obtained.

It was observed that the porous silicon layers formed on the samples under UV light illumination would have a non-uniform thickness, if the current densities exceeded certain values. Some porous silicon particles were broken off the samples in this condition. As an example this value was found to be bigger than 10 mA /cm^2 for the case of n-type, 300 micron substrates. The current density was lowered in several steps until a uniform layer was obtained. A current density of 8.88 mA/cm^2 was obtained to give uniform layers for the above substrate. This procedure was repeated for the other types of substrates to obtain uniform porous silicon layers.

Figures 5.11 - 5.14 show the reflectivities of these layers formed on the surfaces of the IBC cells. It should be noted that when the experiments are done under the UV light, there is no need for passing a large current through the wafer. A small current-density (9 $mA/cm^2 > J > 2\ mA/cm^2$) would be sufficient. This is due to the formation of holes with high concentration at the surface due to UV light.

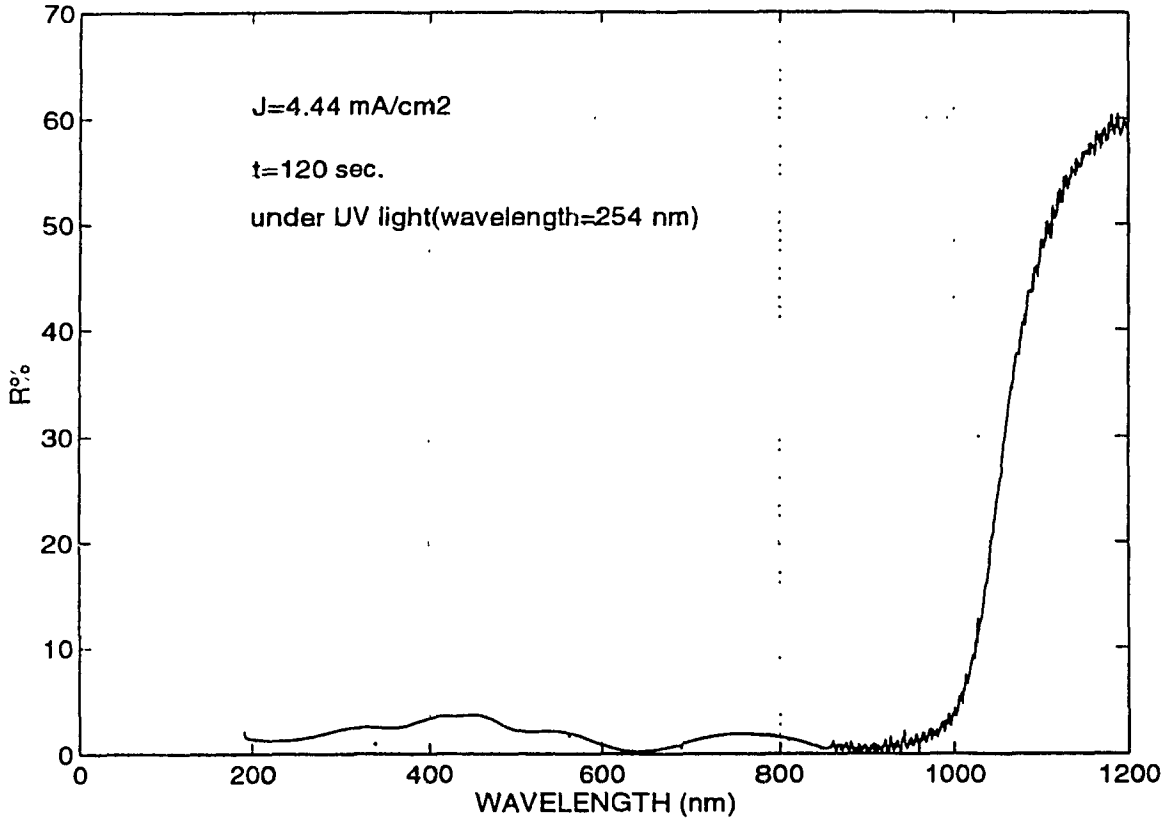


Figure 5.11: The optimized reflectivity for the porous silicon layer formed on the surface of a p-type, 300 micron cell.

Figure 5.11, shows the reflectivity of a porous silicon layer formed on the front surface of a p-type 300 micron thick cell (P^2_{12}) by applying a current density of (J)=4.44 mA/cm^2, under 254 nm UV light, for 120 sec. As it is clear from the figure, the average reflectivity of this layer for the range of 200 to 1000 nm, is less than 5%.

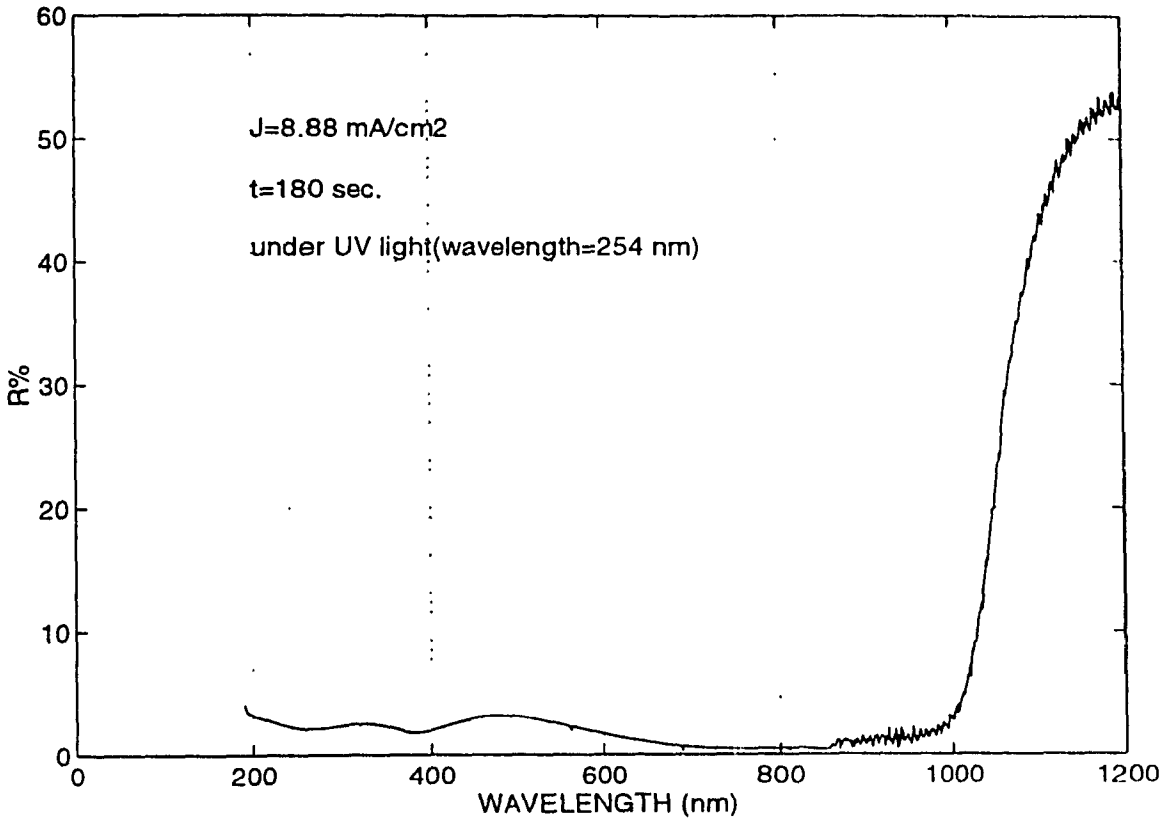


Figure 5.12: The optimized reflectivity for the porous silicon layer formed on the surface of an n-type, 300 micron cell.

Figure 5.12 shows the reflectivity of a porous silicon layer formed on the front surface of a 300 micron thick, n-type IBC cell (N^2_{04}). The porous silicon was formed under a current density of 8.88 mA/cm^2 for 180 sec. and under a UV light (λ=254 nm). The average reflectivity of the layer between the light wavelength range of 200 to 1000 nm, is below 5%.

Comparison of figures 5.11 and 5.12 shows that in the case of n-type cell, higher values of current density and longer etching time is required to produce a porous layer with the same properties of that produced on the p-type cell. This is due to the low concentration of holes in the n-type cell.

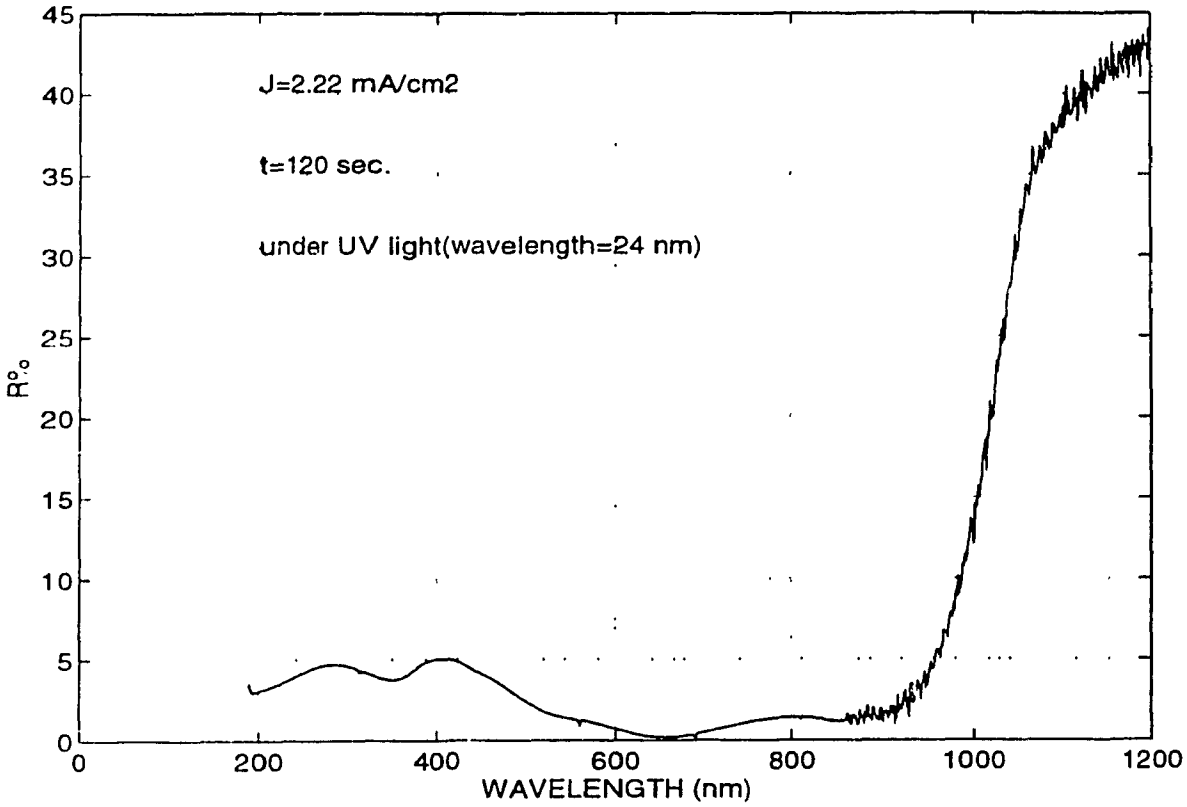


Figure 5.13: The optimized reflectivity for the porous silicon layer formed on the surface of a p-type, 100 micron cell.

Figure 5.13, illustrates the reflectivity of the porous layer formed on the front surface of a 100 micron thick, p-type cell (P_{25}), under the following conditions: the current density (J)=2.22 mA/cm^2, the etching time (t)=120 sec., under a UV light (λ=254 nm).

Comparing figures 5.11 and 5.13 in which the reflectivities of the porous layers formed on the p-type cells are shown, it is revealed that the thickness of the cell plays an important role in forming the porous layer. In the case of a 300 micron cell, the value of the required current density is two times larger than the value required for a 100 micron cell. This is due to the fact that in the case of 300 micron cell, more holes will be recombined before reaching the surface of the cell. Therefore, the

thicker the cell, the larger the current that is needed.

Figure 5.14, shows the optimized porous silicon reflectivity formed on the front surface of a 100 micron thick, n-type cell (N_{23}).

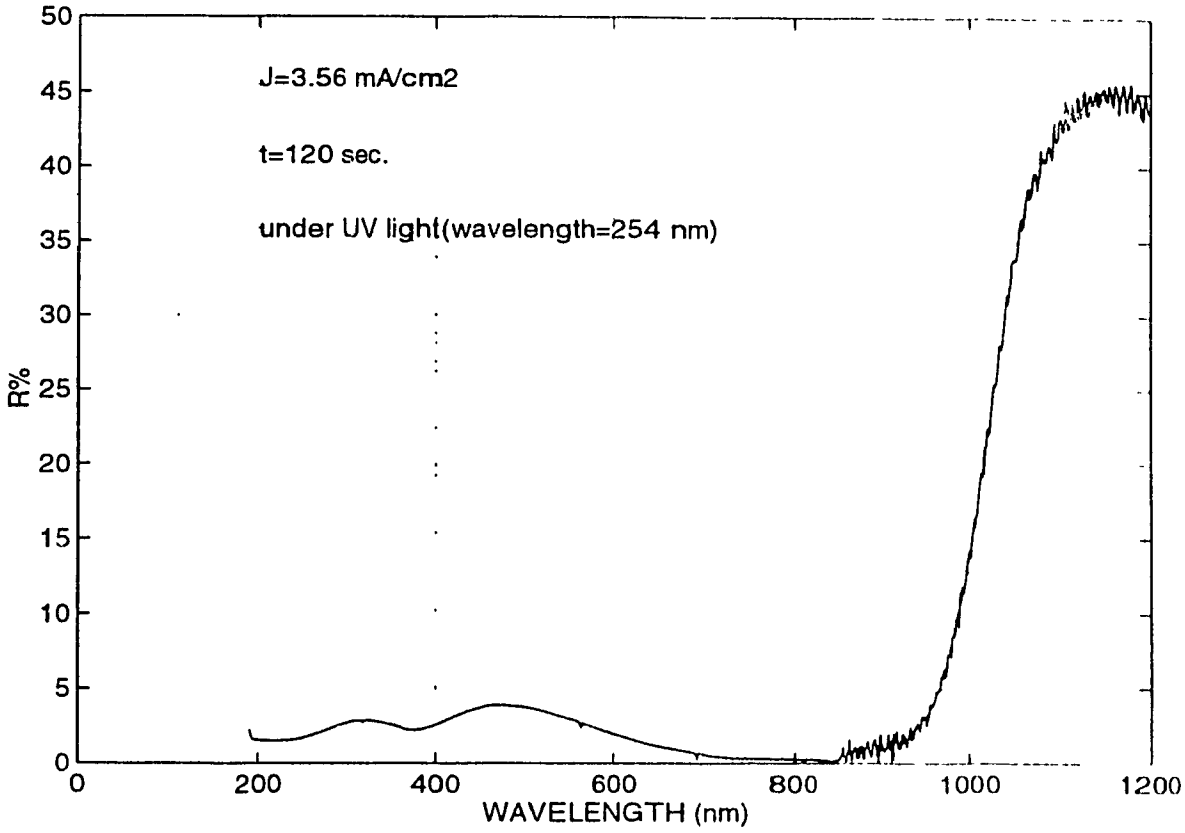


Figure 5.14: The optimized reflectivity for the porous silicon layer formed on the surface of an n-type, 100 micron cell.

As in the case of 300 micron cells, for 100 micron n-type cells more current is required to produce a porous layer comparable with one on a p-type cell.

Figure 5.15 shows the optimal current density vs. thickness for the optimized porous silicon layers formed on the front surfaces of the cells.

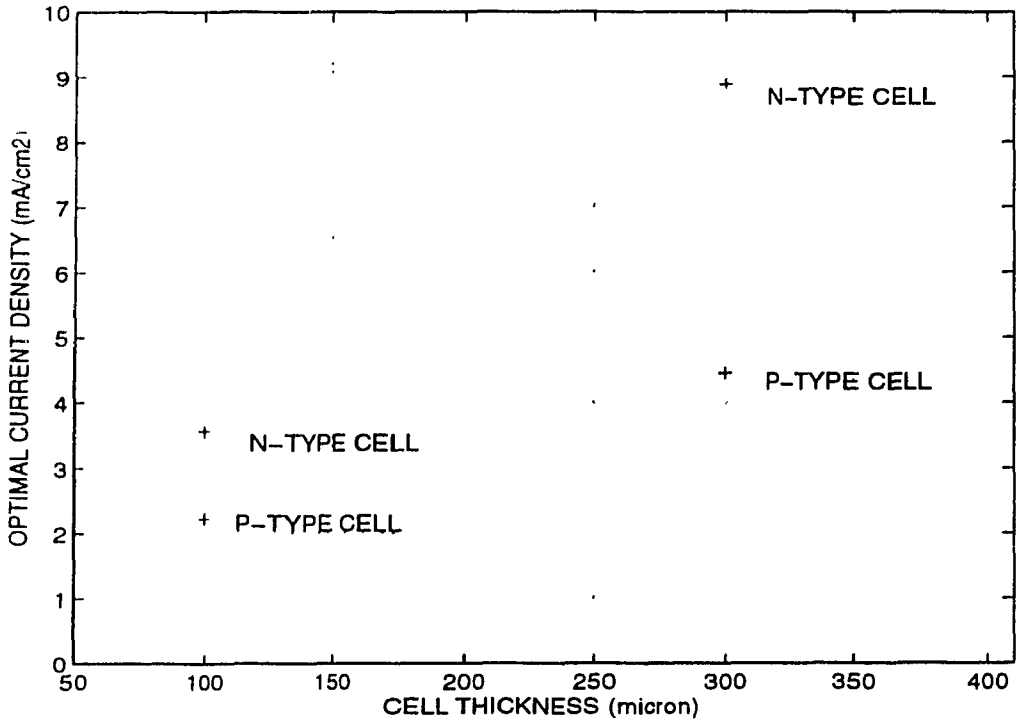


Figure 5.15: The optimal current density vs. cell thickness for the porous silicon formed on the front sides of IBC cells.

As it is clear from the figure, for the n type cells, higher current density is required to produce a porous layer with the same properties of that produced on the p-type cell. This is true for both 100 micron and 300 micron cells. It is also clear that for cells of the same type, higher current density is required for the 300 micron cell to produce a porous layer with the same properties of that produced on the 100 micron cell. In the case of n-type substrates, this difference is larger than that of p-type substrates. These results confirm the discussion on "effect of current density and impurity type on the structure of porous silicon" presented in Chapter 2 section 2.5.

Figure 5.16 compares the effect of a polished front side surface prior to porous silicon layer formation.

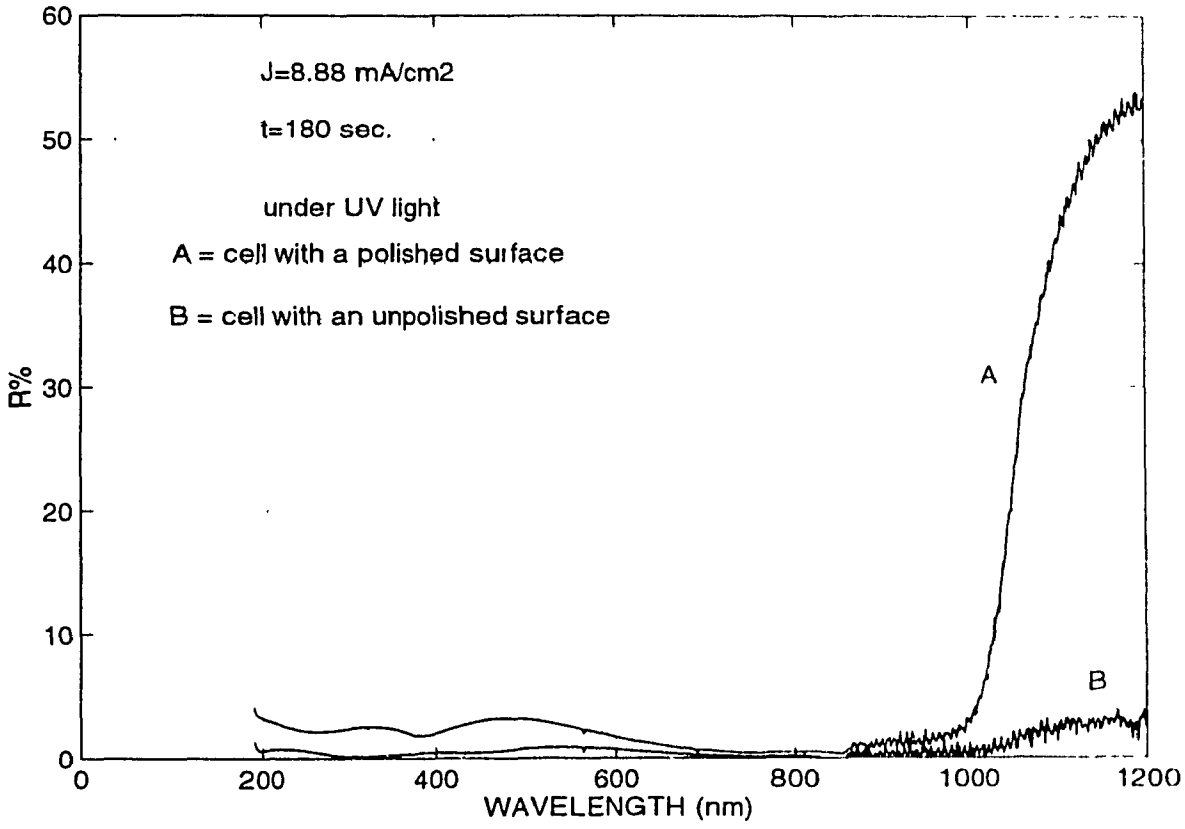


Figure 5.16: The effect of the surface condition on the reflectivity of the porous silicon layers formed on the front surfaces of n-type, 300 thick cells.

As it is shown in the figure, the formation conditions under which both porous layers are formed are exactly the same and the types and the thicknesses of both cells are also the same (both cells are 300 micron thick and are n-type). However, their reflectivities are not the same. The curve A shows the reflectivity of the porous layer formed on a cell (N^2_{04}) having a polished surface. Its average reflectivity is about 3% for the wavelengths between 200 and 1000 nm. The curve B corresponds to the

reflectivity of the porous layer formed on the surface of a cell (N^1_{08}) which is unpolished. Its average reflectivity is 0.5% for wavelengths between 200 to 1200 nm.

The reason for a lower reflectivity for a porous layer on an unpolished surface, is the initial surface roughness. By making the porous layer on a rough surface, the surface of the porous layer becomes highly texturized and thus enhances the light trapping effect at its surface. As a result, one-sided polished wafers are more suitable for fabrication of IBC cells with porous silicon as AR coating.

By considering the optimized reflectivities of the porous silicon layers formed on the polished or unpolished silicon surfaces and comparing these results with the reflectivities of the other AR coatings which were considered in Section 2.5.2.3, one realizes that the optimized reflectivity of a porous silicon layer is even lower than the best double AR coating layer which has ever been deposited on a texturized surface.

As a summary, in this chapter the formation of silicon dioxide and porous silicon as AR coatings for the IBC solar cells are discussed and their reflectivities are measured.

It was shown that the porous layers formed on the front surface of the IBC solar cells under an ordinary light bulb were highly inhomogeneous and their reflectivities were high. It was found that the contacts on the rear surface of the cells were responsible for this inhomogeneity. The problem was eliminated by making the porous silicon under UV light. The reflectivity of the porous silicon for different types of cells was optimized. The results showed that the structure of the porous silicon is very sensitive to the type and thickness of the substrate. The average reflectivity of the porous silicon formed on the polished front side surface was measured to be ~3% for wavelengths between 200 to 900 nm. For the same range of wavelengths, the average reflectivity of a 1100 Å thick-silicon dioxide layer was measured to be ~15%.

CHAPTER 6

Illuminated I-V Characteristics

In this chapter, the procedures used to characterize the solar cells under illuminated conditions are explained and the results presented.

First, the chapter will present a detailed explanation of these procedures and analysis applied to one of the cells (P_{24}), and then will tabulate the corresponding results for all of the cells. The I-V and P-V curves for this cell with different AR coatings (a layer of SiO_2 with ~1100 Å thickness, and a porous silicon layer) are presented. Then, the chapter continues with a discussion of the effects of these AR coatings on the cells' performances. Finally, the problems associated with the porous silicon and the steps taken to alleviate them are discussed.

6.1 1100 Å-Thick Oxide as AR Coating

Figure 6.1, shows the illuminated I-V characteristic for cell P_{24} with 1100 Å SiO_2 as an AR coating on the front surface of the cell.

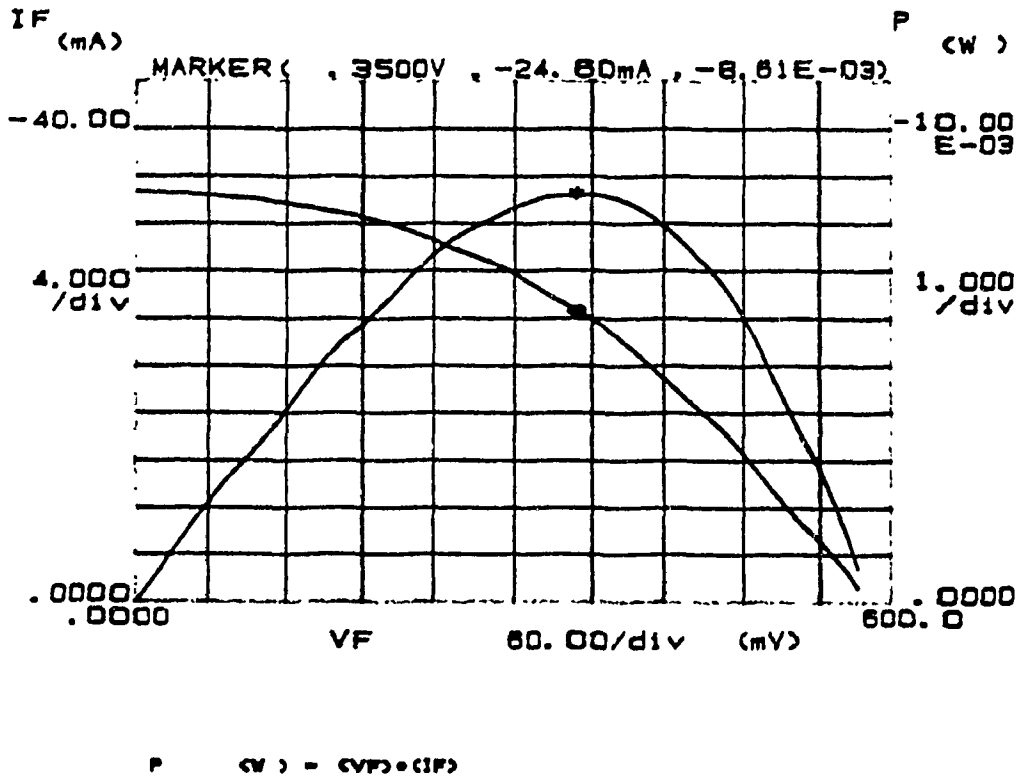


Figure 6.1: Illuminated I-V characteristic for the cell P_{24} with SiO_2 as an AR coating.

In figure 6.1, the y-axis on the left corresponds to the output current, the x-axis corresponds to the voltage developed across the cell due to the different loads seen by the cell, and the y-axis on the right shows the value of output power for each load. In this figure, both I-V and power curves for cell P_{24} are illustrated in which the values of maximum output power and the corresponding voltage and current are shown by markers on each curve. The value of maximum output power, P_m, is 8.61 mW. The maximum voltage, V_m, and current, I_m, are 0.35 V and 24.60 mA respectively. It should be mentioned that by knowing the value of maximum output power, one can obtain the values of voltage and current at that point by just dropping perpendiculars

from that point to the I and V axes. Two other parameters, short-circuit current, I_{sc}, and open-circuit voltage, V_{oc}, can be extracted from the I-V curve by finding the intercepts of this curve with the I and V axes respectively. The corresponding values for the I_{sc} and V_{oc} are 34.68 mA and 0.57 V. Knowing the values of the above parameters, one can calculate the cell's fill factor, FF, using equation 2.12 in chapter 2:

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} x100 = \frac{0.35 \times 24.6}{0.57 \times 34.68} x100 = 44$$

As it was predicted in section 4.2, the high value of series resistance (=5.76 Ω) and the low value of shunt resistance (=571 Ω), resulted a low fill factor for this cell.

Finally, the power conversion efficiency (η) for this cell can be found from Equation 2.13 in Chapter 2. The effective area of the cell is 1.12 cm^2, and the output power per unit area will be 8.61/1.12=7.7 mW/cm^2, and the power conversion efficiency will be:

$$\eta = \frac{P_m}{P_{in}} x100 = \frac{7.7}{100} x100 = 7.7$$

The I-V characteristic of the cell under one sun conditions was repeated after the oxide on the front face was etched away. Then porous silicon was formed at the surface of the cell and the measurement was repeated. The results of these measurements are presented in the following pages.

It should be mentioned that cells are characterized under one-sun conditions (P_{in} = 100 mW/cm^2) at CANMET with the HP 4145 Semiconductor Parameter Analyzer which was programmed to vary the load seen by the solar cell. It was also programmed to simultaneously measure the cell's terminal voltage, current and output power.

Figure 6.2 shows the I-V characteristic for the cell P_{24} without AR coating.

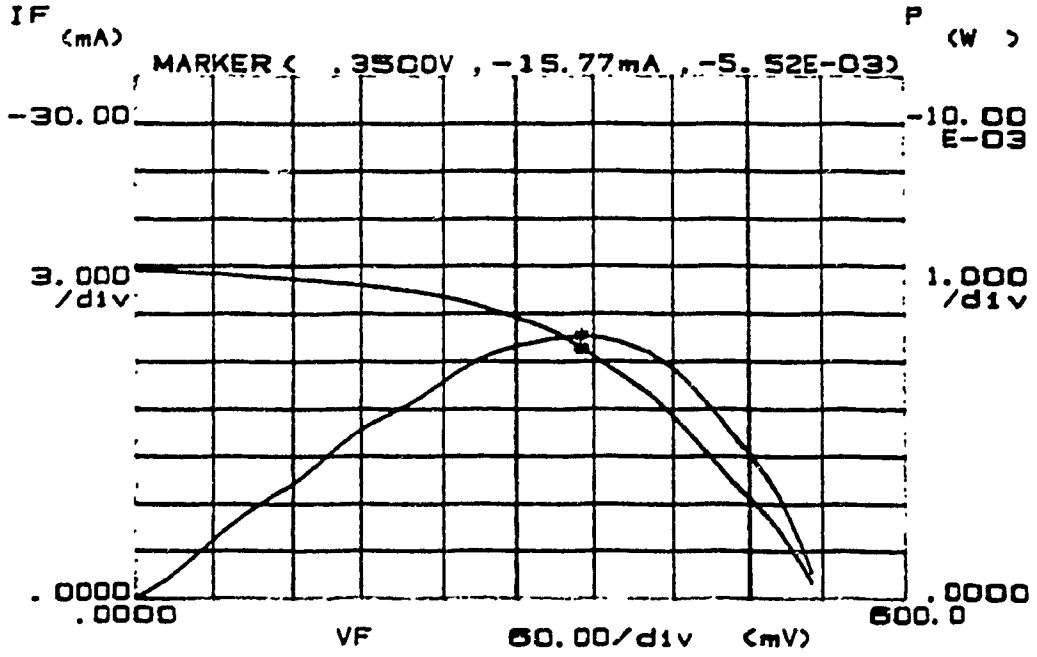


Figure 6.2: Illuminated I-V characteristic for cell P_{24} without AR coating.

The parameters extracted from the curve in figure 6.2, are shown in the table 10. Parameters related to I-V characteristic of the cell with AR coating are also included for comparison. The second column in this table corresponds to the average reflectivities of silicon and silicon dioxide between wavelengths 400 to 800 nm.

cell P_{24}	Ave. Ref. 400-800 nm %	P_m (mW)	V_m (V)	I_m (mA)	V_{oc} (V)	I_{sc} (mA)	FF%	η%
with SiO_2	~15	8.61	0.35	24.60	0.57	34.68	44	7.7
without SiO_2	~40	5.52	0.35	15.77	0.53	20.69	50	4.93
% decreased	-	36	0	36	7	40	-	36

TABLE 10. The performances of the cell P_{24} with and without SiO_2.

The results indicate that except for the fill factor, FF, which is increased, the remaining parameters are decreased when SiO_2 is etched away from the front surface of the cell. The reasons for these considerable changes are as follows.

(1) the bare silicon reflectivity is much higher than the reflectivity of a layer of 1100 Å thick SiO_2 layer as shown in figure 5.1. Therefore, when the SiO_2 is removed from the front surface of the cell, more photons will be reflected back from the cell's surface and this causes a lower concentration of photo-generated carriers within the substrate. A reduction in concentration of photo-generated carriers results in lower values for open circuit voltage and short circuit current as shown in figures 2.6 and 2.7. Finally, due to all above factors, the conversion efficiency of the cell decreases. The reduction in the short circuit current is much higher than that of the open circuit voltage. This is due to the fact that the short circuit current is a linear function of absorbed light intensity, whereas the open circuit voltage is a logarithmic function of absorbed light intensity as described by the equations 2.3 and 2.4, and shown in figures 2.6 and 2.7.

(2) As it was discussed in section 2.3.2.2, a layer of SiO_2 at the surface of silicon reduces considerably the concentration of dangling bonds present at the surface. These dangling bonds have a role of trap centers for the minority photo-generated carriers. Therefore, after removing the oxide from the front surface of the cell, the concentration of trap centers at the surface increases and consequently reduces the concentration of minority carriers within the substrate. This results in lower value for the output current.

The parameters representing all cells' performances with and without the SiO_2 AR coating are tabulated in the tables 11, 12, 13, and 14.

CELL	BORON	P_{in} mW/cm^2	P_m (mW)	V_m (V)	I_m (mA)	V_{oc} (V)	I_{sc} (mA)	FF %	η%
N^1_{01}	**sol-gel**	**100**	**0.03**	**0.30**	**0.08**	**0.37**	**0.10**	**67**	**0.02**
N^1_{02}	implant	100	0.70	0.35	2	0.45	2.23	70	0.62
N^1_{03}	implant	100	1.21	0.37	3.30	0.48	3.23	78	1.10
N^2_{04}	implant	100	5.75	0.34	16.90	0.55	21.07	50	5.11
N^2_{05}	implant	100	1.32	0.31	4.26	0.55	9.56	25	1.17
N^1_{07}	sol-gel	100	0.07	0.23	0.28	0.32	0.34	60	0.06
N^1_{08}	sol-gel	100	0.03	0.10	0.31	0.15	0.45	46	0.03
N^2_{11}	sol-gel	100	0.06	0.29	0.19	0.36	0.22	70	0.05
P^2_{12}	implant	100	1.34	0.38	1.34	0.48	4.65	60	1.20
P^2_{13}	implant	100	2.97	0.35	8.49	0.52	10.24	56	2.64
P^2_{14}	implant	100	0.35	0.24	1.44	0.43	2.71	30	0.31

TABLE 11. Illuminated I-V characteristics of 500 and 300 micron solar cells under one-sun conditions with 1100 Å SiO_2 as an AR coating at front surface having an average reflectivity of 15% in visible region.

Table 11, shows the illuminated parameters for 500 and 300 micron cells with a layer of SiO_2 with thickness of 1100 Å at the front surface. As it was explained before, N^1_{01} is the only cell with the thickness of 500 microns and it is highlighted.

Table 12, shows the illuminated parameters for the 500 and 300 micron cells without SiO_2 at the front surface.

CELL	BORON	P_{in} mW/cm^2	P_m (mW)	V_m (V)	I_m (mA)	V_{oc} (V)	I_{sc} (mA)	FF %	η%
N^1_{01}	**sol-gel**	**100**	**0.02**	**0.30**	**0.08**	**0.37**	**0.09**	**68**	**0.02**
N^1_{02}	implant	100	0.38	0.34	1.11	0.43	1.27	69	0.34
N^1_{03}	implant	100	0.64	0.38	1.69	0.46	1.85	75	0.57
N^2_{04}	implant	100	3.58	0.37	9.68	0.52	11.74	58	3.20
N^2_{05}	implant	100	0.37	0.31	1.20	0.42	1.40	63	0.33
N^2_{06}	implant	100	1.35	0.39	3.47	0.49	3.89	70	1.20
N^1_{07}	sol-gel	100	0.04	0.23	0.18	0.31	0.24	58	0.04
N^1_{08}	sol-gel	100	0.02	0.08	0.21	0.13	0.29	45	0.02
N^2_{09}	sol-gel	100	3.68	0.37	9.94	0.53	11.53	60	3.27
N^2_{10}	sol-gel	100	0.12	0.22	0.56	0.32	0.74	53	0.11
N^2_{11}	sol-gel	100	0.04	0.28	0.13	0.36	0.16	68	0.03
P^2_{12}	implant	100	1.01	0.37	2.72	0.48	3.63	58	0.90
P^2_{13}	implant	100	2.09	0.37	5.66	0.51	6.75	60	1.86
P^2_{14}	implant	100	0.46	0.24	1.90	0.40	3.42	33	0.40
P^2_{15}	sol-gel	100	0.20	0.19	1.03	0.29	1.81	37	0.17
P^2_{16}	sol-gel	100	0.17	0.19	0.88	0.31	1.41	38	0.15

TABLE 12. Illuminated I-V characteristics of 500 and 300 micron solar cells under one-sun conditions without AR coating, average reflectivity of 40% in the visible region for the cells.

Tables 13 and 14, show the parameters for illuminated cells under one sun condi-

tions for the 100 micron cells with and without SiO_2 on their surfaces, respectively.

CELL	BORON	P_{in} mW/cm^2	P_m (mW)	V_m (V)	I_m (mA)	V_{oc} (V)	I_{sc} (mA)	FF%	η%
N_{17}	implant	100	7.84	0.33	23.75	0.55	32.86	43	7
N_{18}	implant	100	0.46	0.14	3.324	0.22	5.028	42	0.41
N_{20}	sol-gel	100	6.17	0.36	17.13	0.54	21.86	52	5.48
N_{21}	sol-gel	100	3.98	0.34	11.72	0.50	14.48	55	3.54
P_{24}	implant	100	8.61	0.35	24.60	0.57	34.68	44	7.70
P_{27}	sol-gel	100	4.47	0.29	15.44	0.52	26.90	32	4

TABLE 13. Illuminated I-V characteristics of 100 micron solar cells under one-sun conditions with 1100 Å SiO_2 as an AR coating having average reflectivity of 15% in the visible region.

CELL	BORON	P_{in} mW/cm^2	P_m (mW)	V_m (V)	I_m (mA)	V_{oc} (V)	I_{sc} (mA)	FF%	η%
N_{17}	implant	100	4.64	0.32	14.48	0.51	19.33	47	4.13
N_{18}	implant	100	0.28	0.13	2.15	0.2	3.27	43	0.43
N_{19}	implant	100	5.48	0.36	15.22	0.53	19.19	54	4.90
N_{20}	sol-gel	100	3.02	0.35	8.64	0.5	11.35	53	2.70
N_{21}	sol-gel	100	2.61	0.34	7.67	0.48	9.30	58	2.10
N_{22}	sol-gel	100	3.23	0.33	9.78	0.49	13.49	49	2.90
N_{23}	sol-gel	100	1.82	0.29	6.26	0.43	8.291	51	1.62
P_{24}	implant	100	5.52	0.35	15.77	0.53	20.69	50	4.93
P_{25}	implant	100	0.53	0.23	2.31	0.34	3.75	41.50	0.47
P_{26}	sol-gel	100	3.38	0.31	10.91	0.48	15.83	44	3
P_{27}	sol-gel	100	3.04	0.28	10.86	0.47	16.94	38	2.70

TABLE 14. Illuminated I-V characteristics of 100 micron solar cells under one-sun conditions without AR coating, average reflectivity of 40% in the visible region for the cells.

Comparing the values of short circuit currents and efficiencies for the cells in tables 11, 12, 13, and 14, one notices that an AR coating has a big impact on the performance of the cells with 100 and 300 micron thicknesses. However, for the cell N^1_{01} whose thickness is 500 microns, no difference was observed when AR layer was removed from the surface of the cell. It can be concluded that the thickness of the cell is very crucial to the cell performance. As the thickness of the cell increases, the probability that photo-generated carriers reach the junction near the back surface of the cell decreases, and if the thickness is greater than the average diffusion length of photo-generated minority carriers, then the light intensity will not have much effect on the cell short circuit current. This is the case which was observed for the 500-micron cell.

Figures 6.3 and 6.4, show the relative quantum efficiencies (quantum efficiency is defined as ratio of the short circuit current to the total flux of the absorbed photons at a particular wavelength) versus wavelength for two cells with 500 micron and 300 micron thicknesses. These measurements were done at NREL (National Renewable Energy Laboratory) by sending cells to the Colorado in the United States. These results also confirm the above reasoning about the effect of the cell thickness on its performance.

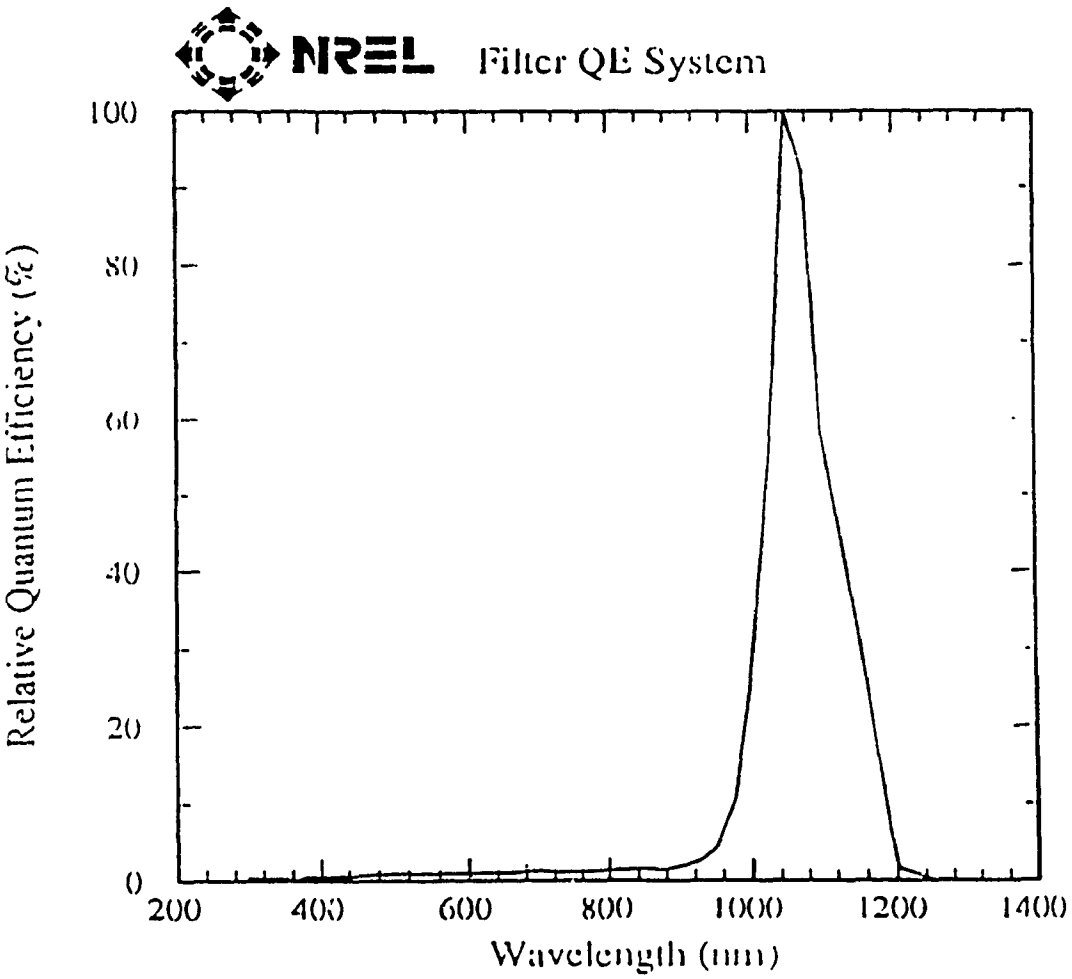


Figure 6.3: Relative quantum efficiency for a 500 micron IBC cell (A_6).

It is clear from the figure 6.3 that the quantum efficiency for the photons with wavelengths lower than 1000 nm, is very low. This indicates that the charge carriers produced by these photons, are all recombined before reaching the junctions at the rear side of the cell. It was also discussed in the chapter 2 section 2.3.2, that a silicon wafer with a thickness of ~350 micron will absorb all the photons with wavelengths equal or lower than 1 micron. Therefore, these 500 micron thick wafers are not suitable for the fabrication of IBC solar cells.

Figure 6.4, shows the relative quantum efficiency versus wavelength for a 300 micron thick cell.

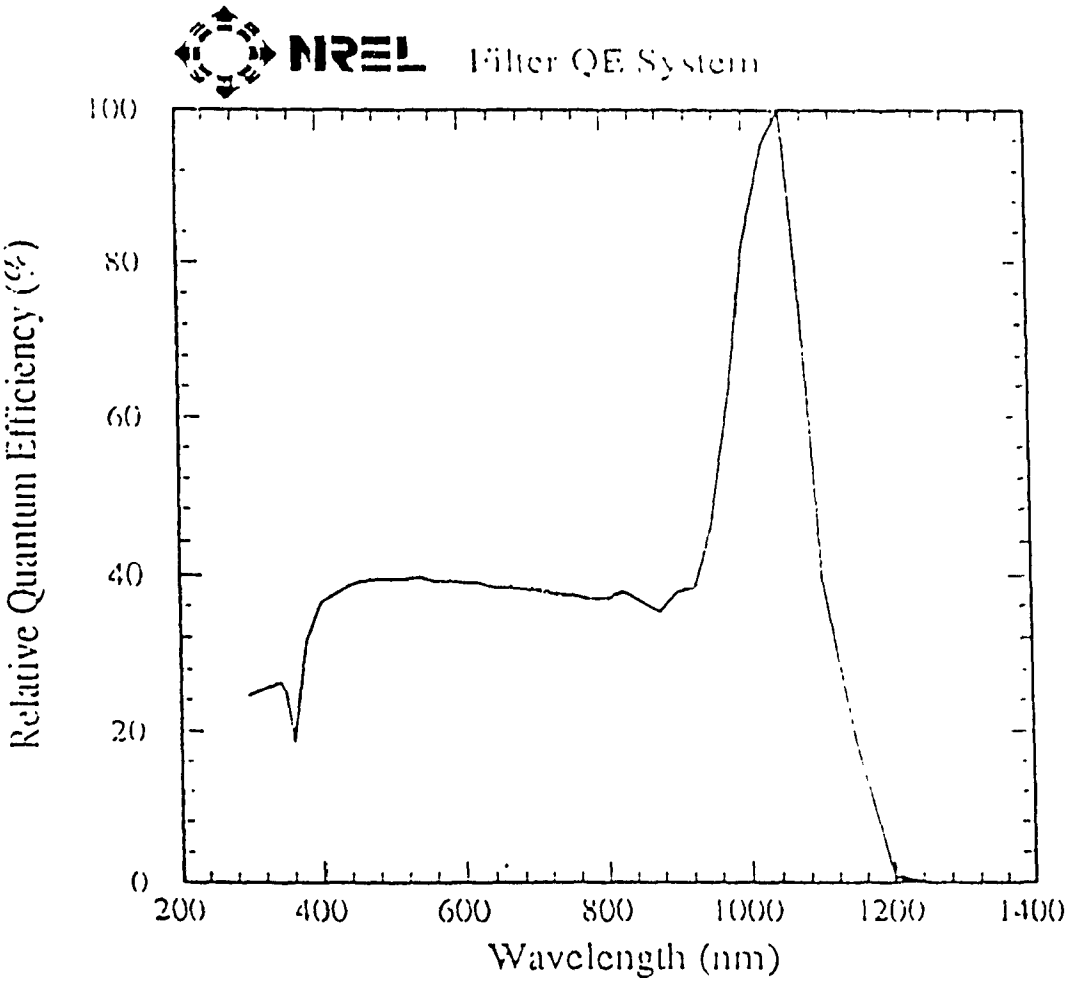


Figure 6.4: Relative quantum efficiency for a 300 micron IBC cell.

As it is shown in the figure, when the cell thickness is reduced from 500 microns to 300 microns, the relative quantum efficiencies for the wavelengths between 400 nm to 960 nm are ~38%. That is, in the case of 300 micron cells, more photo-generated carriers can reach the junctions at the rear side of the cell.

The following conclusions may be drawn by comparing the values of different parameters shown in above tables:

(1) Considering the open circuit voltages for 300 micron cells (table 12), one realizes that there are considerable variations from one cell to another. The open circuit voltage is a function of illumination intensity and reverse saturation current (discussed in Chapter 2). These variations exist even for the cells having comparable short circuit currents. Therefore, the origin of these variations must be related to the variations in the reverse saturation currents for these cells. This is true, considering the dark I-V parameters for these cells (Table 8, Chapter 4), we realize that there are big variations among the reverse saturation currents and this results in different values for the open circuit voltages. However, in the case of 100 micron cells, the variation in the value of open circuit voltage is much lower and this is due to the lower variations among the reverse saturation current for these cells.

(2) In Chapter 4, the best cells (in terms of reverse saturation current and the ideality factor) from each groups were identified and shown. In the following, the names of those cells are repeated:

<u>300 micron cells with lowest I_s and A from each group</u>

P-type (Implant) -----> P^2_{13} P-type (sol-gel) -----> P^2_{16}

N-type (Implant) -----> N^2_{06} N-type (sol-gel) -----> N^2_{11}

N-type (Implant, one-side polished)-----> N^1_{03}

<u>100 micron cells with lowest I_s and A from each group</u>

P-type (Implant) -----> P_{24} P-type (sol-gel) -----> P_{26}

N-type (Implant) -----> N_{19} N-type (sol-gel) -----> N_{21}

Considering the values of the open circuit voltages in the Tables 12 and 14, one realizes that the above mentioned cells have the highest open circuit voltages or their open circuit voltages are comparable with that of best cells in their corresponding

groups. This means that the prediction in Chapter 4 (cells with the lowest reverse saturation currents are the best cells) was correct.

(3) As discussed in chapter 2, the typical value of the fill factor is 60% to 80% and this parameter is very dependent on the values of series and shunt resistances. Considering the values of this parameter for 300 micron cells (Table 12), although the cells suffer from high series resistances (Table 8, dark I-V parameters for 300 micron cells), they have relatively good fill factors due to their high shunt resistances. It is also clear that as the value of shunt resistance decreases, the fill factor decreases too. However, in the case of 100 micron cells as predicted in chapter 4, the values of fill factors are not satisfactory (shown in Table 14) due to their very low shunt resistances for these cells.

Figure 6.5 shows the effect of shunt resistance on the fill factor for different groups of cells having 100 and 300 micron thicknesses.

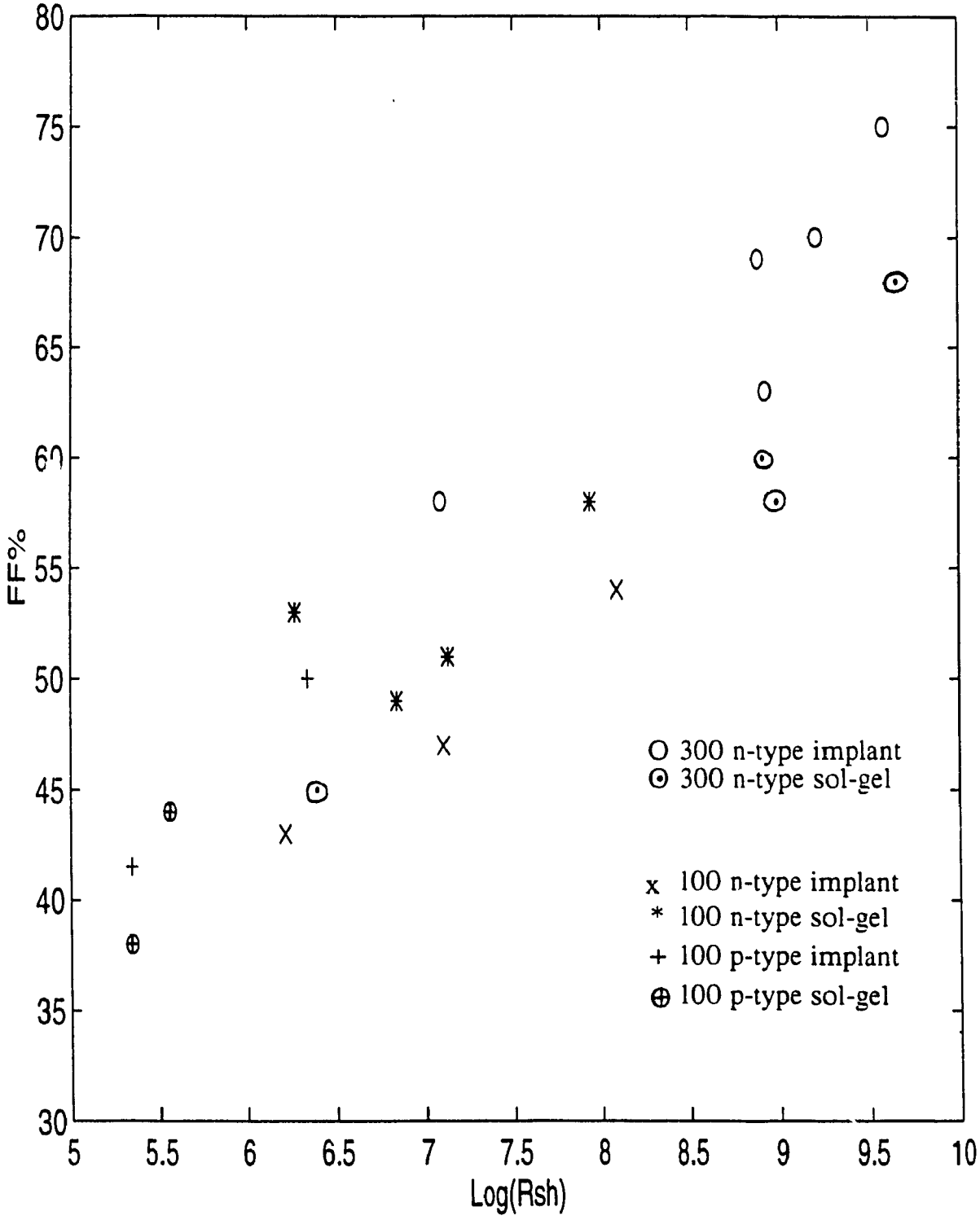


Figure 6.5: Fill factor vs. shunt resistance.

Figure 6.5 indicates that the fill factor increases as the shunt resistance increases. It is also clear that in the case of 100 micron p-type cells, the low shunt resistance resulted in lower fill factor for these cells compared to 100 micron n-type cells. As discussed earlier in chapter 4, the low shunt resistance is a consequence of high reverse saturation current. This means that the 100 micron p-type cells have higher reverse saturation currents, compared to 100 micron n-type cell. This indicates that the concentration of trap centres in these cells is even higher than that of n-type cells. However, 300 micron cells except for the case of p-type sol-gel diffused cells, have higher fill factors compared to 100 micron cells.

(4) Although the 100 micron thick solar cells have higher reverse saturation currents, lower shunt resistances, and lower fill factors, compared to 300 micron cells, they show better performances in terms of short circuit currents and efficiencies due to having thinner substrate (the probability that photo-generated carriers get collected by the rear junction and contribute to the short circuit current is higher).

Figure 6.6 shows the effect of the cell thickness on the short circuit current (for the n-type sol-gel diffused cells).

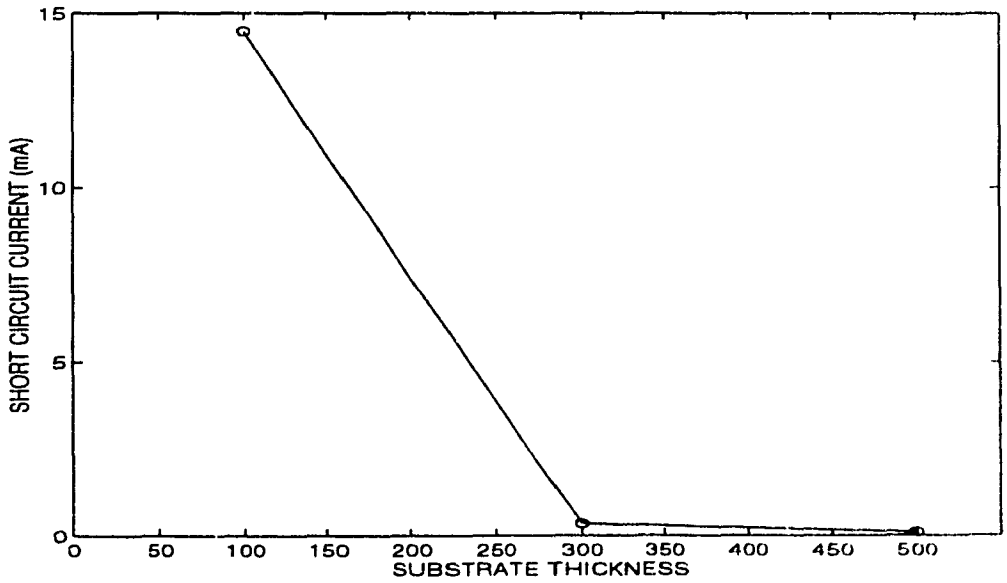


Figure 6.6: The effect of substrate thickness on the short circuit current.

Figure 6.6 indicates that for the IBC solar cell, the substrate thickness is a crucial parameter and that the 500 and 300 micron substrates should not be used.

(5) Under one-sun conditions the values of open circuit voltages for 100 micron cells with n-type substrates indicate that in the case of boron implantation, cells have higher open circuit voltage, compared to sol-gel boron diffused cells. It is believed that if cells were characterized under the concentrated light, then the values of open circuit voltages for sol-gel diffused cells most probably would be comparable to that of implanted cells. The n-type sol-gel diffused cells have relatively higher fill factors, compared to implanted cells and this indicates that sol-gel diffused cells can be operated under the higher concentrated light. Therefore, under the optimized illumination, these cells should show better performance. This means that the sol-gel diffusion technique should be sufficient for the process.

(6) Although, p-type cells have higher reverse saturation currents (see table 9 in Chapter 4), compared to n-type cells, their open circuit voltages and short circuit currents are comparable with those of n-type cells. This indicates that p-type substrates should be more suitable for fabrication of IBC cells.

(7) For both the 300 micron and the 100 micron cells, removal of SiO_2 from their surfaces, decreases both the short circuit currents and the efficiencies of n-type cells by ~ 41% and in the case of p-type cells, these parameters are decreased by ~ 32%. The larger decrease in the values of these parameters in the n-type cells is most probably due to lower mobility of minority holes in these cells, compared to mobility of electrons in the p-type cells. The low mobility of holes in the n-type cells, makes them more susceptible of being trapped by the trap centers usually exist at the surface of a bare silicon.

Figure 6.7 shows the effect of SiO_2 on the cell conversion efficiency for two 100 micron thick cells (with n-and p-type substrates).

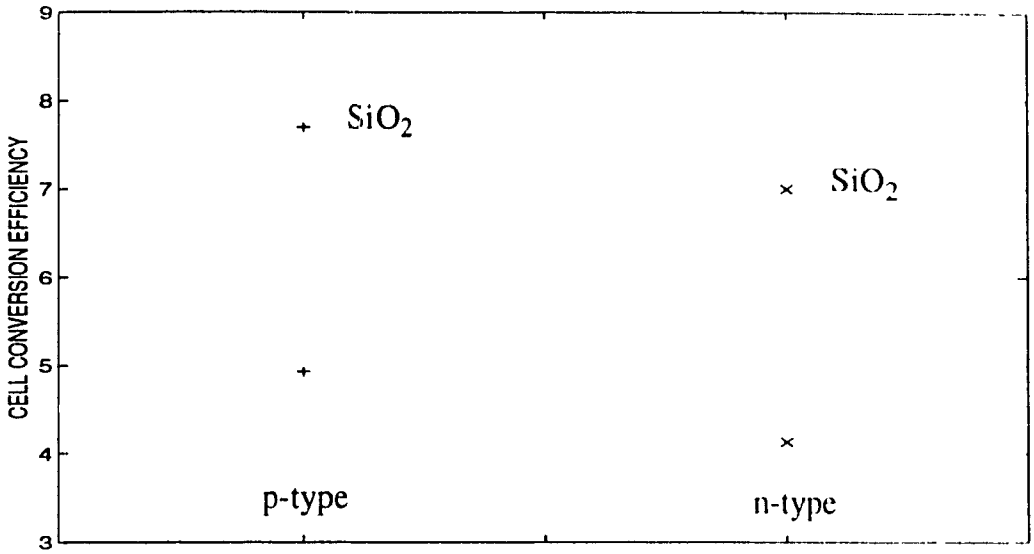


Figure 6.7: The effect of SiO_2 on the cell conversion efficiency.

6.2 Porous Silicon as AR coating

The illuminated I-V curve for the cell P_{24} with the porous silicon as an AR coating on the front surface of the cell, is shown in the figure 6.8 and the results for the remaining cells are summarized in tables 15 and 16.

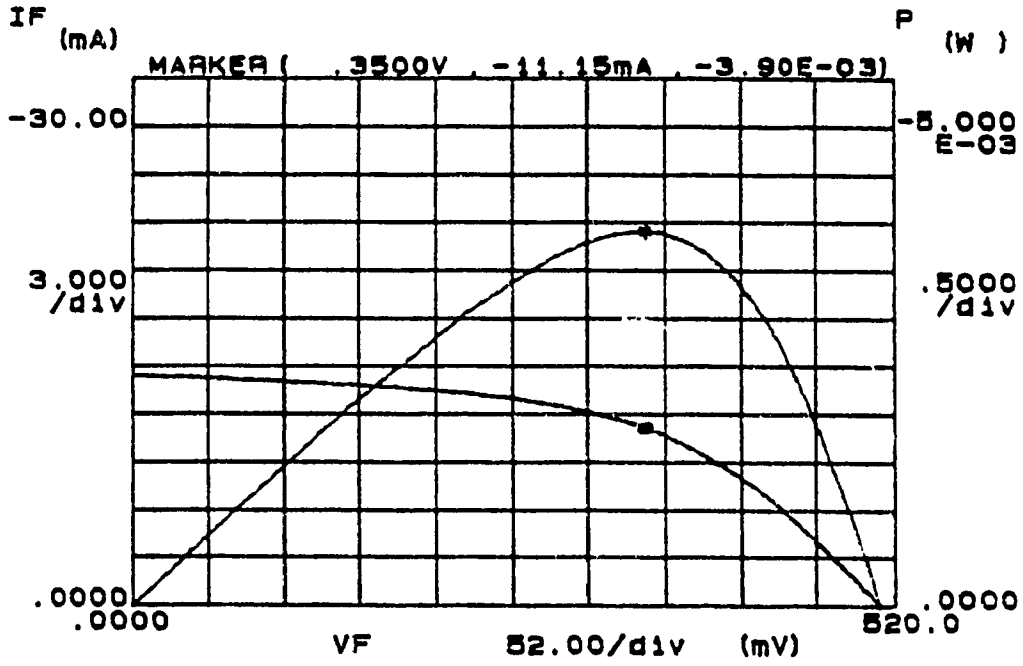


Figure 6.8: The illuminated I-V characteristic of cell P_{24} with the porous silicon as an AR coating on its front surface.

The parameters extracted from the curve in figure 6.8 for the cell P_{24} with the porous silicon as an AR coating on its front surface are shown in table 15. The results for the remaining cells are shown in table 16.

cell P_{24}	P_m(mW)	V_m(V)	I_m(mA)	V_{oc}(V)	I_{sc}(mA)	FF%	η%
with SiO_2	8.61	0.35	24.60	0.57	34.68	44	7.70
without SiO_2	5.52	0.35	15.77	0.53	20.69	50	4.93
with PS layer	3.90	0.36	11.15	0.51	14.40	54	3.51

TABLE 15. The illuminated parameters for the cell P_{24} under one sun conditions with and without AR coating on its front surface.

The results indicate that with porous silicon layer on the top of the cell, the corresponding values for the parameters such as open circuit voltage, short circuit current, and efficiency are lowered by 4%, 30%, and 29% respectively, compared with the case when the front surface of the cell is not covered with the AR coating.

ID	thick μm	boron	reflectivity max/min % 400-800 nm	P_m (mW)	V_m (V)	I_m (mA)	V_{oc} (V)	I_{sc} (mA)	FF%	η%
P_{24}	100	implant	6 - <1	3.90	0.36	11.15	0.51	14.40	53	3.51
P_{26}	100	sol-gel	4 - 1	3.07	0.30	10.24	0.48	15.46	41	2.77
P_{27}	100	sol-gel	7 - <1	1.86	0.26	7.16	0.42	11.59	38	1.67
N_{19}	100	implant	3.5 - <1	0.75	0.30	2.50	0.43	3.13	56	0.67
N_{21}	100	sol-gel	5 - <1	0.64	0.30	2.14	0.42	2.66	57	0.58
N_{17}	100	implant	5 - <1	0.46	0.24	1.92	0.36	2.55	50	0.42
N_{22}	100	sol-gel	4 - <1	0.43	0.24	1.78	0.36	2.44	49	0.39
N_{20}	100	sol-gel	5 - <1	0.32	0.23	1.38	0.36	2.00	44	0.29
P^2_{13}	300	implant	3 - 1	1.81	0.37	4.90	0.51	5.82	61	1.63
P^2_{12}	300	implant	3 - 1	0.83	0.35	2.38	0.47	3.14	56	0.75
N^2_{04}	300	implant	4 - 1	0.22	0.27	0.80	0.39	0.90	62	0.2
N^2_{09}	300	sol-gel	4 - 1	0.08	0.26	0.29	0.35	0.35	62	0.07

TABLE 16. The illuminated parameters for the 100 and 300 micron cells under one sun conditions with the porous silicon as AR coating.

By comparing the results shown in table 16, with the results shown in the tables 12 and 14, one notices that the porous silicon on the front surfaces of the n-type cells decreases the short circuit currents and the efficiencies of these cells by about 90% and for the p-type cells, these values are reduced by 22%.

6.3 Discussion

As it was discussed earlier in section 2.5.2, for a porous silicon layer with the following properties

- as a UV convertor
- with an adjustable bandgap
- with a highly texturized surface
- with an extremely simple process, well suited for large area, and cost effective

one expects to be an excellent candidate for the photovoltaic industry. However, the results of the experiments reveal that there are problems associated with this material that make the application of this layer in the photovoltaic area less likely.

6.3.1 Difficulties with the Porous Silicon

The reduction in the value of the short circuit current is likely to be due to one or the combination of the following reasons:

a) **high surface recombination at the surface**

when the porous silicon layer is formed on the surface of the cell, then the surface area will become much larger compared with the surface area of the bare silicon

and this results in a higher concentration of dangling bonds due to the absence of a passivating layer. Therefore, the recombination of photo-generated minority carriers at the surface increases and thus, the short circuit current decreases.

b) **heterojunction formation**

As it was mentioned before, the bandgap energy of the porous silicon is larger than that of the silicon. As a result, there will be a heterojunction formed at the interface of the silicon and the porous silicon. Knowing that there will be an associated electric field for every heterojunction structure, only one type of charge carriers can pass through each heterojunction. Therefore, only one type of carriers generated within the porous layer, can pass through the junction between silicon and the porous silicon. This would result in lower short circuit current for the cells.

Furthermore, referring to the figure 2.24, which shows the photoluminescence spectrum of the porous silicon, and using the relation $\lambda=1.24/E$ (μm), which relates the wavelength of the photon to its energy, one realizes that within the porous layer itself there are distribution of silicon crystallites having bandgap energies ranging from about 1.3 to 2.3 eV. These crystallites of randomly varying size are all adjacent to each other in the porous silicon layer. Figure 6.9 plausibly depicts the porous silicon as being composed of this random assembly of crystallites.

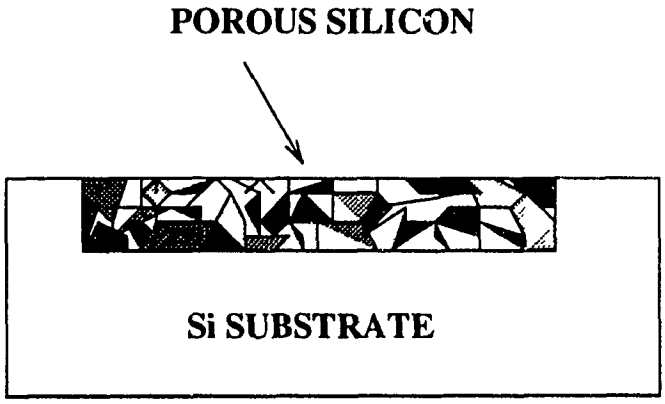


Figure 6.9: The assumed structure for the porous silicon.

If this is true, it is likely that there may be also heterojunctions within the porous layer itself. There may be an associated electrostatic field for each heterojunction which lets only one type of charge carrier pass through the junction. Since the size and therefore bandgap of each crystallite will vary from one crystallite to the next, one can expect that carriers will not have a clear path, and may recombine before leaving the porous silicon. Therefore, the concentration of carriers photo-generated in the porous silicon reaching the silicon substrate will be considerably decreased, and the value of the short circuit current drops as well.

6.3.2 Attempted Solutions

To understand the electrical properties of the porous silicon and phenomenon causing the low efficiency of IBC cells covered by porous silicon, more investigations are conducted as follow:

1- To investigate the effect of the surface passivation on the porous layer, two different experiments were performed as follows:

1.a) cells were annealed in hydrogen gas under the following conditions:

cell N_{19} was annealed in the hydrogen at T=380 ^{o}C for 2:15 hours,

cell N^{2}_{04} was annealed in the hydrogen at T=380 ^{o}C for 3:15 hours,

The table 17 shows the results for the cell N_{19}, annealed in hydrogen for 2:15 hours at temperature 380 °C.

N_{19} with PS	V_{oc}(V)	I_{sc}(mA)
before annealing	0.43	3.13
annealed in H_2	0.43	2.84
decreased%	0	9.5

TABLE 17. The illuminated parameters for one 100 micron cell under one sun conditions with the porous silicon before and after annealing in H_2 for 2:15 hours at 380 °C.

The table 18 shows the results for the cell N^2_{04} annealed in hydrogen for 3:15 hours at temperature 380 °C.

N^2_{04} with PS	V_{oc}(V)	I_{sc}(mA)
before annealing	0.39	0.90
annealed in H_2	0.41	1.15
decreased%	-	-
increased%	5	27.50

TABLE 18. The illuminated parameters for one 300 micron cell under one sun conditions with the porous silicon before and after annealing in H_2 for 3:15 hours at 380 °C.

The results shown in the table 17, indicate that the annealing process suppresses the cells performances, but the results in the table 18 reveal the fact that the annealing time is a very crucial parameter which can suppress or improve the cells performances. As it is clear from the results in these two tables, if the annealing time is not long enough, the value of the short circuit current for the cell decreases, but as the

annealing time increases, there will be an improvement in the value of the parameters. Therefore, the hydrogen annealing can improve the cells performances. It is likely that the dangling bonds present at the surface of the porous silicon will be passivated and thus, the concentration of the trap centers at the surface decreases and results in higher concentration for the photo-generated minority carriers and higher short circuit current. The result of this experiment confirms that one of the problems associated with the porous silicon, is the high surface recombination at its surface as predicted before in section 6.3.1(a).

1.b) Porous silicon oxidized at high temperature

New cells were fabricated on p-type wafers. The fabrication procedure was the same as before except that in the previous fabrication, the porous layer was formed on the surface of the cell at the last step right after metallization (in this case, it was not possible to make a high temperature oxide layer due to the presence of the aluminum at the rear surface), but in the new fabrication, the porous layer was formed at the front surface of the cells after the phosphorus diffusion and before growing the passivating oxide on both sides of the cells. Therefore, the porous layers on the front surfaces of the new cells are covered with a layer of oxide (~1000 Å thick) thick enough to passivate the trap centers present at the surface of the layers.

Table 19, shows the dark I-V parameters for a new cell, P_{28}, and in order to compare these parameters with the previously fabricated cells, the dark I-V parameters for some of the cells are also included in this table. As it is clear from the table, the values of all the dark parameters for the three cells are close and comparable.

CELL	TYPE	ρ (Ω-cm)	BORON	Al (μm)	I_s(A)	A	R_s (Ω)	R_{sh} (KΩ)
P_{28}	**p**	**5.6**	**sol-gel**	**0.60**	**$1.1x10^{-4}$**	**4.45**	**5.61**	**0.20**
P_{26}	p	5.6	sol-gel	0.60	$1.56x10^{-4}$	4.90	6.28	0.26
P_{27}	p	5.6	sol-gel	0.60	$2.61x10^{-4}$	4.68	6.11	0.21

TABLE 19. The dark I-V characteristics of the 100 micron cells in which the cell P_{28} is a new cell and its dark parameters are compared with previously fabricated cells.

In the following table the illuminated parameters for the three cells are shown:

CELL	V_{oc}(v)	I_{sc}(mA)
P_{28}	**0.35**	**4.026**
P_{26}	0.48	15.46
P_{27}	0.42	11.59

TABLE 20. The illuminated parameters for the cells with different condition for the porous layer surfaces formed on the top of the cells

By comparing the values of these parameters, the open circuit voltage and the short circuit current, for the cell P_{28}, vs. the two previous cells, one notices a sharp decrease in the values of these parameters for the new cell, P_{28}. As discussed earlier, improvement was observed for the values of the open circuit voltage and the short circuit current of cells, by passivating the surfaces of the porous layers on the cells, in a hydrogen ambient. However, in the case of oxide passivation, although a layer of thick oxide passivates the trap centers at the surface of the porous layer and decreases the porous layer reflectivity (shown in figure 5.2), it drastically suppresses

the performance of the cell.

There are some possible explanations for this. (a) as the oxide grows on the surface of the porous layer, the width of the crystalline porous silicon decreases (to grow 1 micron oxide at the surface of the silicon, 0.45 microns silicon will be consumed) and referring to the equation 2.22, which describes the relation between the width of the crystallite and its bandgap, the bandgap of the crystallite increases. This increase in the value of the bandgap energies for the crystallites is likely to increase the value of the electrostatic field associated with the heterojunctions formed between the tiny porous silicon crystals and thus reduce the probability that one type of carriers pass through the junctions. As a result, the values of the short circuit current and the open circuit voltage drop. The result of this experiment confirms that another problem associated with the porous silicon, is the formation of the heterojunctions within the porous layer between the different small crystals of porous silicon. (b) there might be formation of the oxide between some small crystallites and isolate them from each other. This will block both types of carriers passing from one crystallite to the next and thus, decreases the short circuit current.

As a summary to the chapter, the following may be stated:

(1) It was shown that the illuminated I-V characteristics of the cells are directly related to their dark I-V parameters and that the judgements about the cells dark I-V parameters presented in chapter 4 were correct.

(2) It is believed that under the concentrated light, the performances of both boron sol-gel diffused and boron implanted cells would be possibly comparable. Knowing that the implantation technique is quite expensive, the sol-gel diffusion technique would be appropriate for the fabrication of solar cells.

(3) it was found that a layer of oxide with ~1100 Å thickness will improve the cells

performances.

(4) The effects of mobilities of holes and electrons on the cells performances were observed.

(5) The effect of porous silicon on the cells performances was shown and it was found that a layer of porous silicon at the surface of the cell, will decrease both open circuit voltage and short circuit current.

(6) It was discussed that the possible reason for the failure of porous silicon as an AR coating was possibly due to the heterojunctions formed between the porous layer and silicon substrate and between the small crystallites within the porous layer itself.

CHAPTER 7

Conclusions, Contributions and Suggestions

A series of Interdigitated Back Contact solar cells on p-type and n-type wafers having thicknesses of 100, 300 and 500 microns, were fabricated using sol-gel and ion-implantation techniques. A full set of physical properties, including the I-V characteristics of the fabricated devices were measured under dark and light illumination conditions. Two different antireflection coatings were applied to the front surface of the cells and the characterizations were repeated. The results were compared and the following conclusions were determined.

7.1 Conclusions

A- Dark Conditions

- Reverse saturation currents in the range of nanoamperes were achieved in the case of dark I-V characteristics of n-type 500 and 300 micron solar cells. The obtained ideality factors were between 1 to 2. These results indicate an excellent junction formation for the cells. The results obtained by the relatively less-expensive sol-get technique were quite comparable with those obtained for the case of ion-implantation technique.
- In the case of 300 micron p-type and 100 micron cells for both p-type and n-type,

higher reverse currents and ideality factors (undesirable) were obtained. This could be due to the lower quality (high concentration of trap centers) of the original wafers.

• The series resistances in all the cells were high. Due to the thin layer of aluminum deposited on the cells, the sheet resistances of the metallized regions were high.

B- Under Illuminated Conditions

The devices were also characterized under one sun light and the following results were obtained.

• Characterization of the cells under illumination showed that the performance of the Interdigitated Back Contact solar cells was very dependant on the cell thickness. The short circuit current was highest for 100 micron cells and lowest for 500 micron cells.

• The average value of fill factor for n-type 300 and also for the case of 500 micron cells was about 68%. The shunt resistances for these cells were very high (good). However, in the case of 300 micron p-type and for all 100 micron cells, the fill factor was quite low, about 50%, due to very low shunt resistances and high series resistances for these cells

• Comparing p-type cells with n-type cells, with comparable observed reverse saturation current values, higher short circuit currents and higher open circuit voltages were observed for the p-type cells. This is due to the higher value of mobility for the electrons in the p-type substrate than that of the holes in the n-type substrate.

• Comparing the illuminated parameters for the cells with different thicknesses, it was observed that the efficiency was highest for the 100 micron cells and lowest for the 500 micron cells.

(C) Anti-Reflection Coatings

In order to increase the efficiencies of the solar cells, anti-reflection coatings were used. This would enhance the amount of light absorbed by the cells' front surfaces. In this work two different anti-reflection coatings, silicon dioxide and porous silicon were used.

- It was found that a layer of SiO_2 with ~1100 Å thickness is an excellent passivation and anti-reflection coating. There was significant reduction in the cell performance after removal of the SiO_2 layer (~40% and 30% in the values of short circuit currents for n- and p-type cells, respectively).
- The porous silicon layers with very low reflectivities in the wavelength range between 200 to 900 nm (reflectivities of about 3% for cells with polished surfaces and 0.5% for cells with unpolished surfaces), were formed on the front surfaces of all cells. The results revealed that the porous silicon layer not only does not enhance the cell performance, but reduces both short circuit current and open circuit voltage of the cell. The failure of porous silicon as an anti-reflection coating is most probably due to formation of heterojunction structures formed within the porous layer between small silicon crystallites having different bandgaps and between the porous silicon layer and the silicon substrate as well. Due to the presence of these structures, the photo-generated carriers can not reach the silicon substrate and thus, both short circuit current and open circuit voltage decreases.

7.2 Main Contributions:

There are several original contributions which have arisen from this work. They may be summarized as follows:

On the fabrication of silicon solar cells:

- P-n junctions were fabricated using sol-gel boron and phosphorus diffusion, at a high enough quality for use in solar cells. The sol-gel technique was proven to be successful when diffusing into n-type substrates, and is expected to be also useful when diffusing into p-type substrates.
- Porous silicon is unlikely to be useful as an anti-reflection coating for silicon solar cells. This is hypothesized to be because of the complex crystallite structure which prevents carriers absorbed in the porous silicon from diffusing into the bulk silicon.
- This thesis serves as a substantial collection of measurements on the IBC solar cell structure, relating most common parameters and measures of solar cell performance.

On the creation of porous silicon:

- Under the usual conditions of illumination by visible light, the uniformity of a porous silicon layer on one surface of a Si wafer depends sensitively on the geometry of the contacts used to inject current from the other side, and depends sensitively on the applied current density.
- However, porous silicon can be made to be highly uniform, in spite of highly variant backside contact geometry, by illuminating the front surface by UV light.

7.3 Suggestions For Future Work

To improve the cell performance, the following modifications are suggested:

- High-quality 100 micron Float-zone wafers in which the concentration of trap centers is very low, must be used to fabricate Interdigitated Back Contact solar cells.
- A thick layer of aluminum (~1 micron) should be deposited at the surface to lower the metallization resistance.
- A new design should have more of the back surface covered by p- and n-fingers. In the present design, the back side has substantial areas where the surface is just near-intrinsic silicon in between the junction depletion regions. This provides unwelcome additional sites for surface recombination for the carriers diffusing from the front side, and increases the average distance which the carriers must travel. A redesigned mask set would have the same effective area, but more p- and n-type diffused fingers.

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Appendix A

Detailed Description of the Fabrication Process

In the following, the fabrication process is explained in details:

Four inch wafers (n- and p-type), with 500, 300, and 100 micron thicknesses, were cut into one inch square samples. Reverse-RCA cleaning procedure, a standard cleaning procedure in microelectronics fabrication lab, described as follows, used to clean the samples:

A.1 Reverse-RCA Cleaning procedure

1. Boil samples in H_2So_4:H_2O_2 (1:1) for 5 minutes.
2. Rinse in running deionized (DI) water for 2 minutes.
3. Boil in HCl:H_2O_2:H_2O (1:1:5) for 5 minutes.
4. Rinse in DI water for 2 minutes.
5. Dip in HF:H_2O (1:20) for 30 seconds.
6. Rinse in DI water for 2 minutes.
7. Soak in hot NH_4OH:H_2O_2:H_2O (1:1:5) for 5 minutes.
8. Rinse in DI water for 2 minutes.
9. Blow dry with N_2 gas.

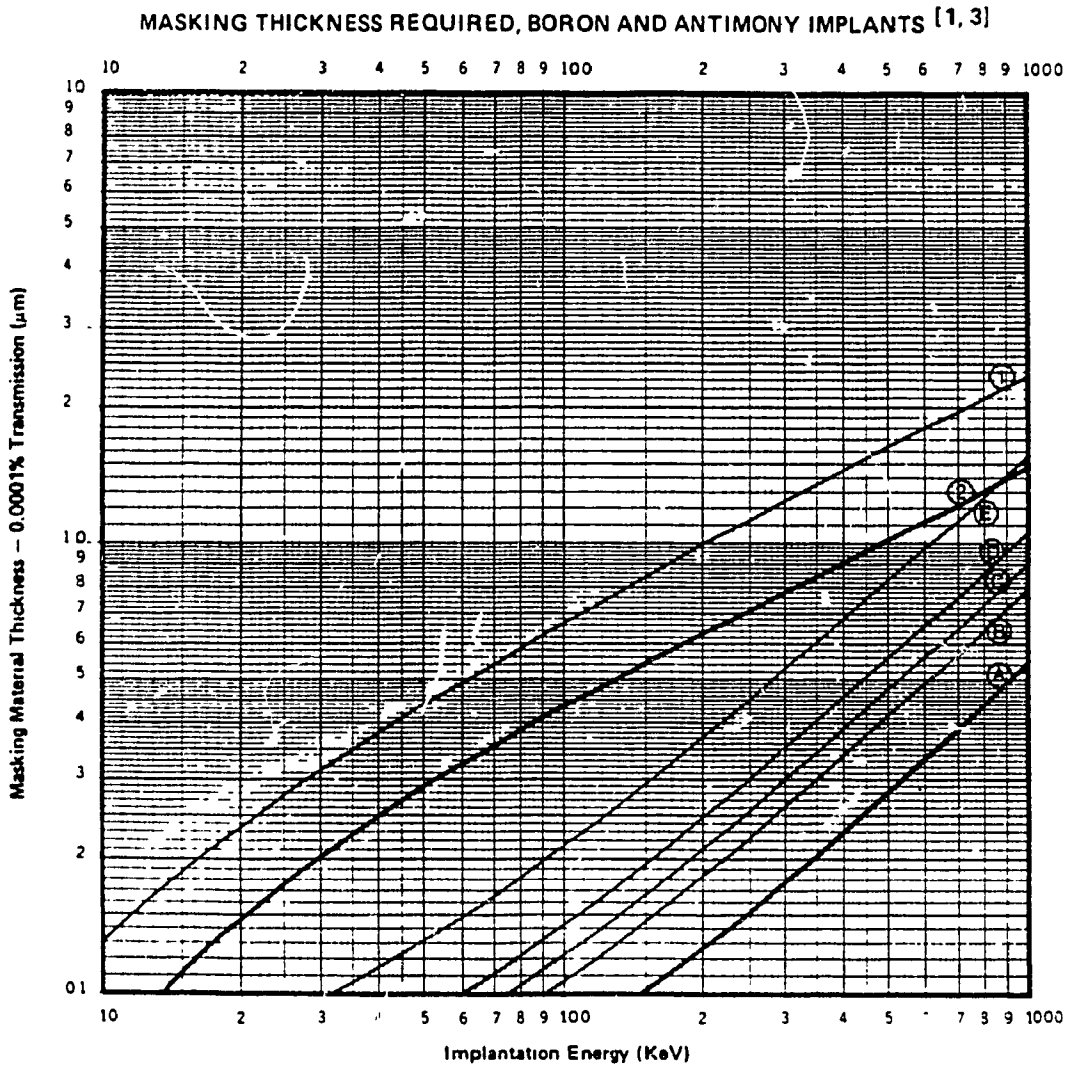
In the above cleaning procedure, the steps 1 and 3 are used to remove all the metallic contaminants and step 7 is used to remove the organic contaminants.

A.2 Silicon Oxide as a Passivating Mask

Silicon dioxide with a certain thickness can be used to mask against impurities from reaching the silicon substrate. In case of ion implantation, the following equation can be used to calculate the thickness of oxide [34],d

$$\frac{Q_p}{Q} = \frac{1}{2} erfc\left(\frac{d - R_p}{\sqrt{2}\Delta R_p}\right) \tag{A.1}$$

where, Q_p is fraction of dose which penetrates the mask, Q is the total implanted dose, d is the thickness of required oxide, R_p is projected range of implanted ions which depends on implantation energy and the impurity material, ΔR_p is projected standard deviation of implanted ions which is a function of implantation energy and impurity materials. Usually, in practice, experimentally determined curves are used to determine the thickness of oxide needed to mask against different impurities[34]. Fig.A.1, shows the masking material thickness versus the implantation energy [16]. Curve #1 is used to find the oxide thickness in order to mask 99.9999% of implanted borons at different energies.



ION	CURVE	MASKING MATERIAL	ION	CURVE	MASKING MATERIAL
Boron (Top)	1	Thermal SiO_2, Polysilicon, Aluminum, Negative Resist, or Positive Resist	Antimony (Bottom)	A	CVD Si_3N_4
				B	Thermal SiO_2 or Aluminum
				C	Polysilicon
	2	CVD Si_3N_4		D	Negative Resist
				E	Positive Resist

Figure A.1: Oxide thickness required to mask 99.9999% of implanted borons at different implanted energies (curve #1).

From this curve, it can be seen that an oxide thickness greater than 0.45 μm is needed to mask 99.9999% of the boron atoms which are implanted at an energy of 50 Kev. For the case of phosphorous and boron diffusions, using the sol-gel diffusion technique, graphs A.2 and A.3 [16] can be used to determine the thickness of oxide required to mask against phosphorous and boron predepositions respectively.

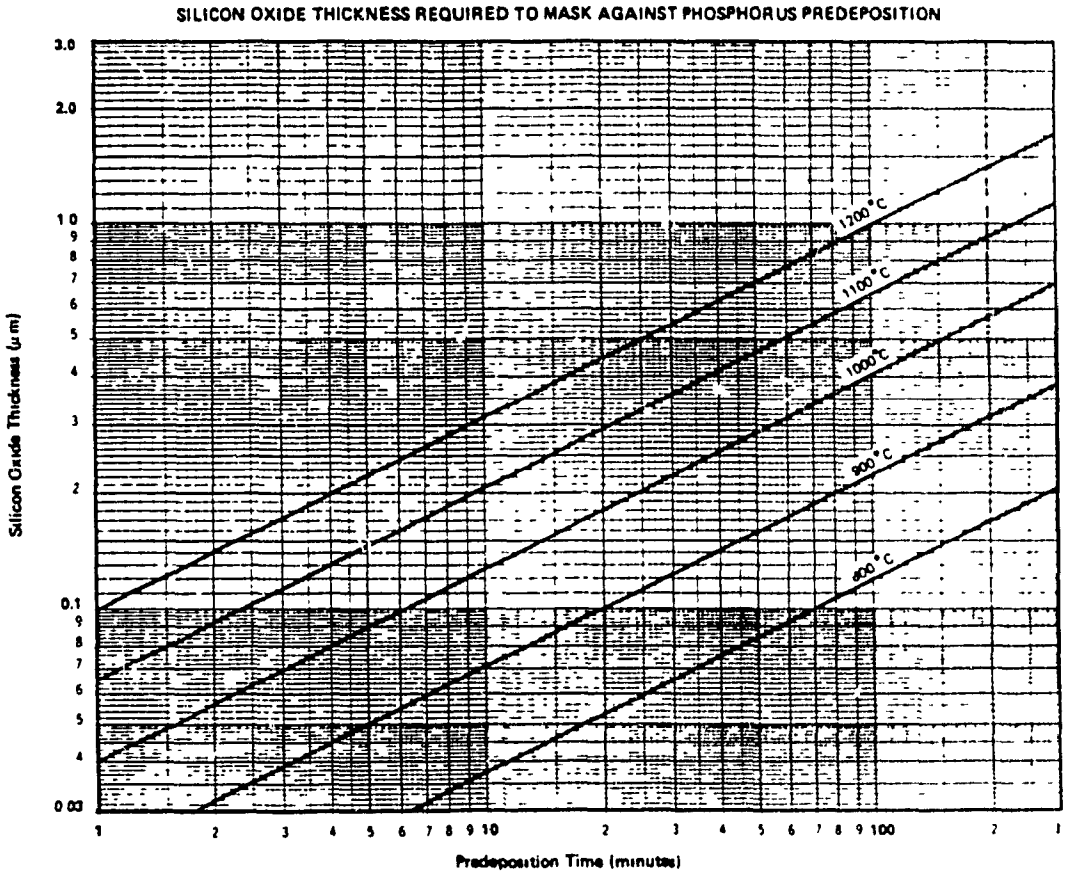


Figure A.2: Silicon oxide thickness required to mask against phosphorous predeposition.

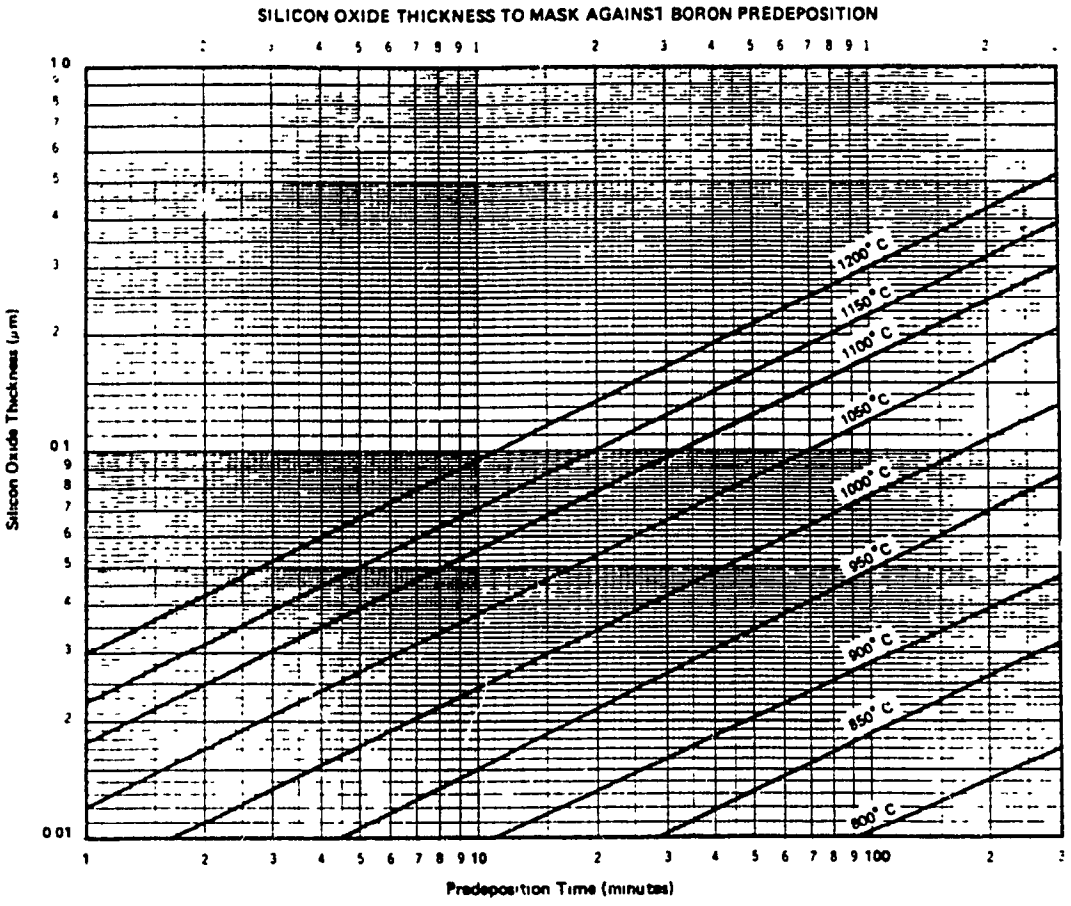


Figure A.3: Silicon oxide thickness to mask against boron predeposition.

A.2.1 Oxide Growth

To grow silicon oxide with any specific thickness a wet oxidation technique was employed. In this technique, the pure oxygen gas runs through water vapor before reaching the oxidation chamber. The oxide thickness is related to the oxida-

tion time as follows [33]:

$$t_{ox} = \frac{x_o^2}{B} + \frac{x_o}{B/A} \qquad \text{(A.2)}$$

where, t_{ox} is the oxidation time in hours, x_o is the required oxide thickness in microns, B is parabolic rate constant in $\mu m^2/hr$, and B/A is the linear rate constant in $\mu m/hr$. Both, B and B/A can be found from the following equations

$$B=C_1\exp(-E_1/kT), \quad B/A=C_2\exp(-E_2/kT) \qquad \text{(A.3)}$$

where, C_1 and C_2 are constants and for wet oxidations their values are $2.14\times10^2 \mu m^2/hr$ and $5.33\times10^7 \mu m/hr$ respectively. E_1 and E_2 are activation energies and for wet oxidation their values are 0.71 eV and 2 eV respectively. k is Boltzmann's constant ($=8.62\times10^{-5}$ eV/ ^oK). Accordingly, the values of B and B/A are 0.331 $\mu m^2/hr$ and 0.649 $\mu m/hr$ respectively.

To grow a layer of wet oxide to mask against the boron predeposition and implantation with thickness of 0.6 μm at 1000 ^oC (using wet oxidation techniques), it was found from equation A.2 that the oxidation time should be 2 hours. Fig A.4 [33] can also be used to find the oxidation time at different temperatures for a desired thickness of wet oxidation on a (100) silicon.

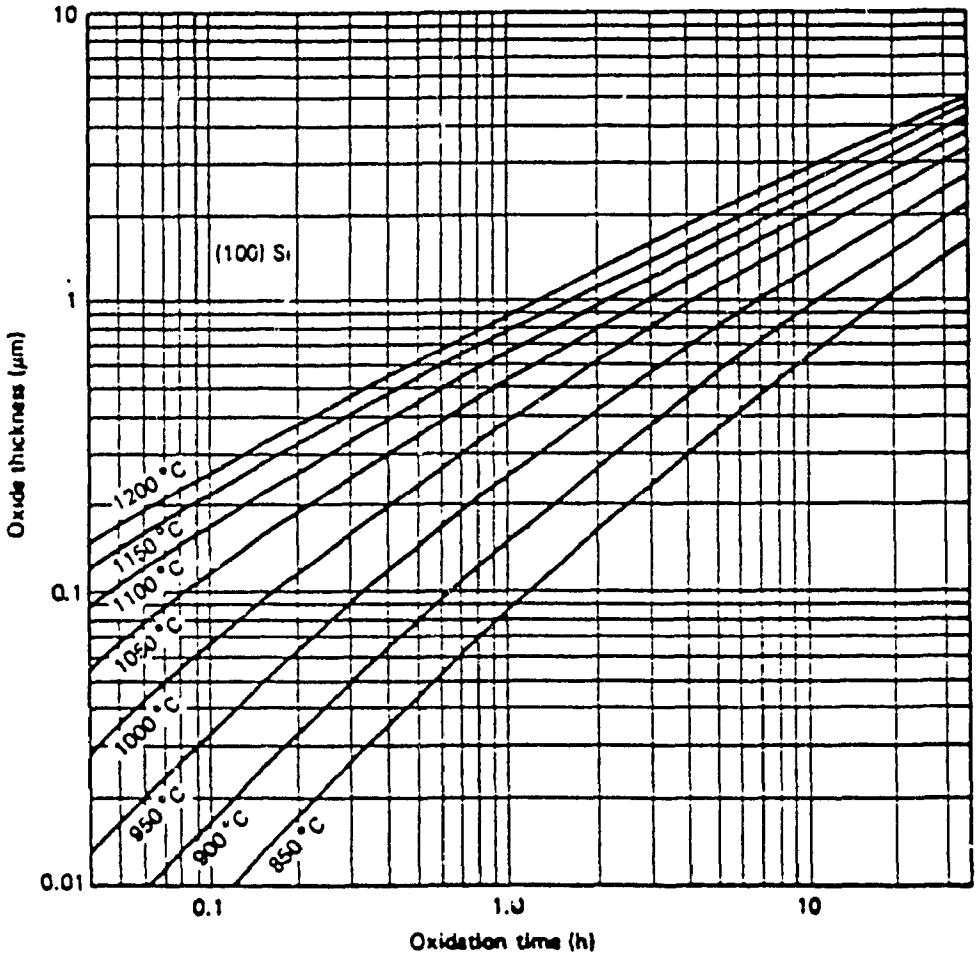


Figure A.4: The oxide thickness versus oxidation time for wet oxidation and (100) silicon.

From the figure, it is also clear that for an oxide thickness of 0.6 μm, the oxidation time is about 2 hours.

A.2.2 Oxidation Procedure

1. Boil the oxidation boat in acetone and methanol consecutively and dry it with N_2 gas.
2. Turn the water bubbler on and set the temperature at 100 ^{o}C.
3. Place the oxidation tube in the furnace.
4. Turn the furnace on and set the temperature at 1000 ^{o}C and let the nitrogen gas run in the tube at a flow rate of 2 lit/min.
5. Load the samples on the oxidation boat and put the boat at the tube mouth.
6. Insert the boat to the centre of tube very slowly. This procedure should take about 15 minutes.
7. Once the boat is in the middle, change the ambient to wet oxygen at the flow rate of 1 SCFH and start timing.
8. Once the oxidation is done, turn the furnace off and change the ambient to nitrogen at flow rate of 2 lit/min.
9. Gradually pull the boat to the mouth of the tube and leave it there until it cools down.
10. Remove the boat and store the samples in the DI water.

A.3 Applying First Mask (Boron Diffusion)

The following steps were taken to open windows in the oxide to make the samples ready for boron diffusion

1. Place the sample on the spinner chuck and turn the vacuum on.
2. Blow the samples with nitrogen gas to remove the dust particles.

3. Apply 5-6 drops of photoresist with the filter-equipped syringe on each sample.

4. Spin at 3000 r.p.m for 30 seconds.

5. Soft bake in forced-air convection oven for 30 minutes at 95 °C.

6. Let sample cool down.

7. Expose the samples to UV light through mask #1 using lithography and aligner machine.

8. Dip in stirred developer solution for 1 minute.

9. Rinse in the DI water and dry the samples with nitrogen gas.

10. Check samples under the microscope to make sure that the pattern is developed completely.

11. Hard-bake in forced-air convection oven for 30 minutes at 115 °C.

12. Etch the patterned oxide in a solution of HF:NH_4F (1:4) until the pattern on each sample becomes hydrophobic (indicating that all oxide is etched away).

At this point, the samples are divided into two groups, group (a) in which the boron will be introduced into substrate by ion implantation technique and group (b) in which sol-gel diffusion technique is used to introduce boron into the substrate.

13. Remove the photoresist from the surface of samples in group (b) by boiling them in acetone.

14. Clean samples in group (b) using Reverse-RCA cleaning procedure.

15. Store group (b) samples in DI water.

A.3.1 Boron Implantation

Samples in group (a) were implanted at the Sherbrook university at an energy of 50 Kev and a dose of $1x10^{16}cm^{-2}$according to the simulation results, figure 3.3. To

remove the photoresist from the surface of samples, they were soaked in hot acetone which is always used to remove the photoresist, but photoresist did not come off. Different chemical solutions such as hot H_2SO_4, HCl, and NH_4OH which are strong remover of photoresist, were used to remove the photoresist, but there were no success. Hot acetone and ultrasonic bath did not work either. It was concluded that when samples were implanted with boron ions, some of photoresist molecules were driven into the SiO_2 layer with the boron ions. Therefore, it was decided to etch part of the SiO_2 layer on the top of 300 micron samples in such a way to remove the photoresist molecules in the oxide layer near the surface, without losing the pattern on the samples. To do this, the samples were etched one at the time, in a solution of $HF:H_2O$ (1:50) for 2-3 minutes, and in this way photoresist was removed. After Reverse-RCA cleaning procedure, sample were stored in DI water. This procedure was not applicable to 100 micron thick samples because they were extremely fragile and would possibly brake during the above procedure. It was decided to use oxygen enhanced plasma etching technique to remove the photoresist. This technique was used at Polytechnique, Lisa lab, and was able to remove the photoresist. Then samples were cleaned and stored in DI water.

A.3.2 Pre-deposition of Borosilica on Samples group (b)

Borosilica manufactured by Emulsitone, was used as a diffusion source with a boron concentration of $5x10^{20}$ cm^{-3}.The following steps were taken to prepare the furnace and apply borosilica on the samples

1. Boil the boron diffusion boat in acetone and methanol consecutively.
2. Turn the bubbler on and set the temperature to 100 ^{o}C.

3. Install the boron diffusion tube in the furnace.

4. Turn the furnace on and set the temperature to 1100 °C.

5. Run the nitrogen gas in the tube with the flow rate of 2 lit/min.

6. Take the samples out of DI water and blow dry with nitrogen gas.

7. Put the samples on the spinner chuck and turn the vacuum on.

8. Blow with nitrogen to remove the dusts.

9. Apply 5-6 drops of borosilica with the filter-equipped syringe.

10. Spin at 3000 r.p.m for 30 second.

11. Bake in forced-air convection oven for 15 minutes at 150 °C.

12. Load the samples on boron diffusion boat and push the boat to the middle of tube very gradually.

13. Once the samples are in the middle of tube, change the ambient to 20% oxygen and 80% nitrogen (adding oxygen to ambient is to avoid the brown stain problem which causes high resistance), and start timing.

After 2 hours diffusion, turn the furnace off and change the ambient to nitrogen gas and slowly pull the boat to the mouth of tube.

A.3.3 Oxide Growth to Mask Against the Phosphorus pre-deposition

From the results of simulation, fig.3.2, it was found that 1 hour phosphorus pre-deposition at 1000 °C would yield high surface concentration, therefore, by knowing the pre-deposition condition, the oxide thickness to mask the phosphorus atoms can be determined from the Fig.A.2 [16]. The figure shows that an oxide thickness

greater than 0.32 microns can mask a phosphorus pre-deposition performed at 1000 ^{o}C for 1 hour. Therefore all the samples were oxidized at 1000 ^{o}C for 1 hour using the procedure described in the section 3.4.3.2.

A.4 Applying Second Mask (Phosphorous Diffusion)

Following the described steps in the section 3.4.3, windows were open in the oxide to make samples ready for phosphorous diffusion.

A4.1 Phosphorus Pre-desposition

Phosphorosilica manufactured by Emulsitone, is used as a diffusion source with a phosphorus concentration of $1x10^{21}$ cm^{-3}. Following the steps described in the section 3.4.3.2, phosphorosilica was deposited on the samples at 1000 ^{o}C for 1 hour in a nitrogen ambient.

A.4.2 Final Oxide Growth and Annealing

After 1 hour phosphorus pre-deposition at 1000 ^{o}C, the ambient was changed to oxygen for 13 minutes to grow a layer of oxide with thickness of 1120 Å. This final oxide is necessary for the following reasons

1. At the surface of silicon there are many dangling bonds and an oxide with thickness greater than 400 Å will passivate the surface [32].
2. As it was discussed in the section 2.3.2.2, the surface recombination velocity has its maximum value at Si/Al interface, therefore, aluminum should be in contact with

silicon in small regions. This thin oxide layer will cover the n-and p-type fingers and then by photolithography techniques, holes can be selectively opened in this regions.
3. An oxide thickness of 1120 Å acts as an antireflection coating as it was discussed in chapter 2.

Finally, after 13 minutes wet oxidation, the ambient is changed to nitrogen and there will be a 15 minutes annealing at the same temperature to reduce the density of fixed charges, Q_f, as discussed in the section 2.3.2.2. After annealing, furnace was turned off and samples were pulled to the mouth of tube very slowly.

A.5 Opening Contact Windows before Metallization (Mask #3)

Mask #3 was used to open contact windows in both p- and n-type diffusion fingers. Following the steps described in the section 3.4.3, the contact windows were opened in the oxide on the p- and n-type diffusion fingers. It should be mentioned that in order to keep the oxide on the front surface of the samples, the front surface must be covered with the photoresist as well to protect the oxide.

A.6 Metallization Mask (Mask #4)

Mask #4 was applied to define the windows where metal has to be deposited on the samples. In this part of the process some difficulties regarding photoresist lift-off, arose due to the very long and narrow structures present on the mask #4 (patterns with about 10000 microns length and 40 microns width). After developing the exposed photoresist on the samples, the pattern was partly removed and it was

impossible to keep the pattern on its place. In order to remove this problem, it was tried to change the photoresist thickness, the exposure time, the photoresist and developer solution types, but there were no success. It was found that chlorobenzene can harden the chemical structure of photoresist. Therefore, it was decided to use this chemical in order to remove the problem. Different combinations of baking temperature, exposure time, chlorobenzene dip time, Photoresist thickness, and baking time were tried and the following procedure was able to remove the problem:

1. Spin photoresist at 3000 r.p.m for 30 seconds.
2. Soft bake at 95 ^{o}C for 30 minutes.
3. Chlorobenzene dip for 4 minutes and 30 seconds.
4. Bake at 92 ^{o}C for 5 minutes.
5. Expose to UV light for 40 seconds.
6. Develop for 6 seconds.

Notice that this recipe is developed only for the following combination

1. 1350 J Photoresist Shipley
2. 354 Developer Shipley
3. Cobilt Mask Aligner (Old Mask Aligner)

and if anyone of above components is changed then the recipe will not work. Samples were metalized at Polytechnique, Lisa lab with aluminum thickness of 0.6 microns.

A.6.1 Post Metallization Anneal

In order to improve ohmic contact between semiconductor and aluminum and also decrease the density of interface charges, Q_{it}, present at the interface of Si/

SiO_2,the final step in processing is to anneal samples in an annealing furnace in an ambient, mixed of nitrogen and hydrogen gas. The following explains the annealing procedure:

Load the samples into the furnace tube and turn the furnace on. Let the nitrogen gas flow in the tube and monitor the temperature of the furnace carefully. When temperature is about 300 ^{o}C, turn on the Bunsen burner located at the furnace output and then turn the hydrogen gas on. At temperature 450 ^{o}C, start timing for 30 minutes. Once the annealing is completed, turn off both the furnace and hydrogen gas but let the nitrogen flow until samples cool off. Turn off the Bunsen burner and take the samples out of the furnace.

Figures.A.5 and A.6, show the Irvin's curves for the n- and p-type Gaussia diffusion profiles respectively.

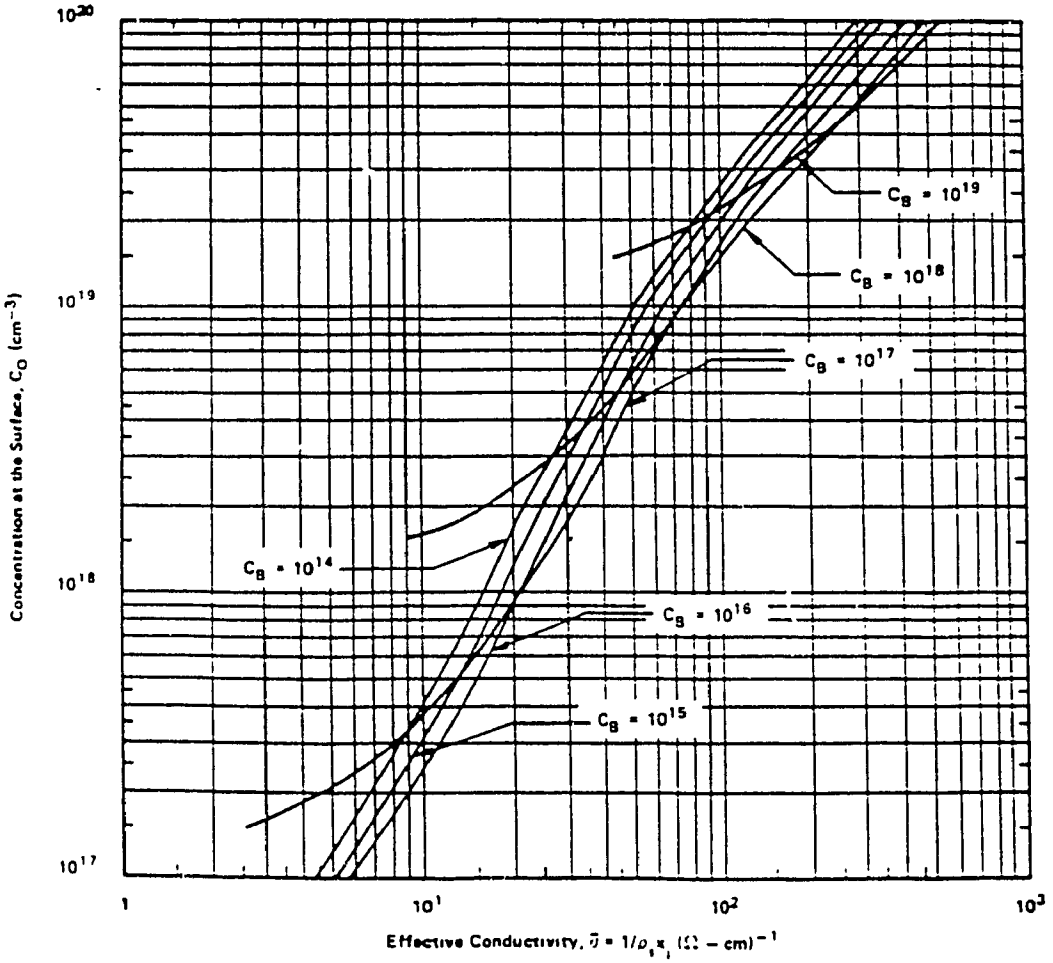


Figure A.5: Irvin curves for an n-type Gaussian impurity profile.

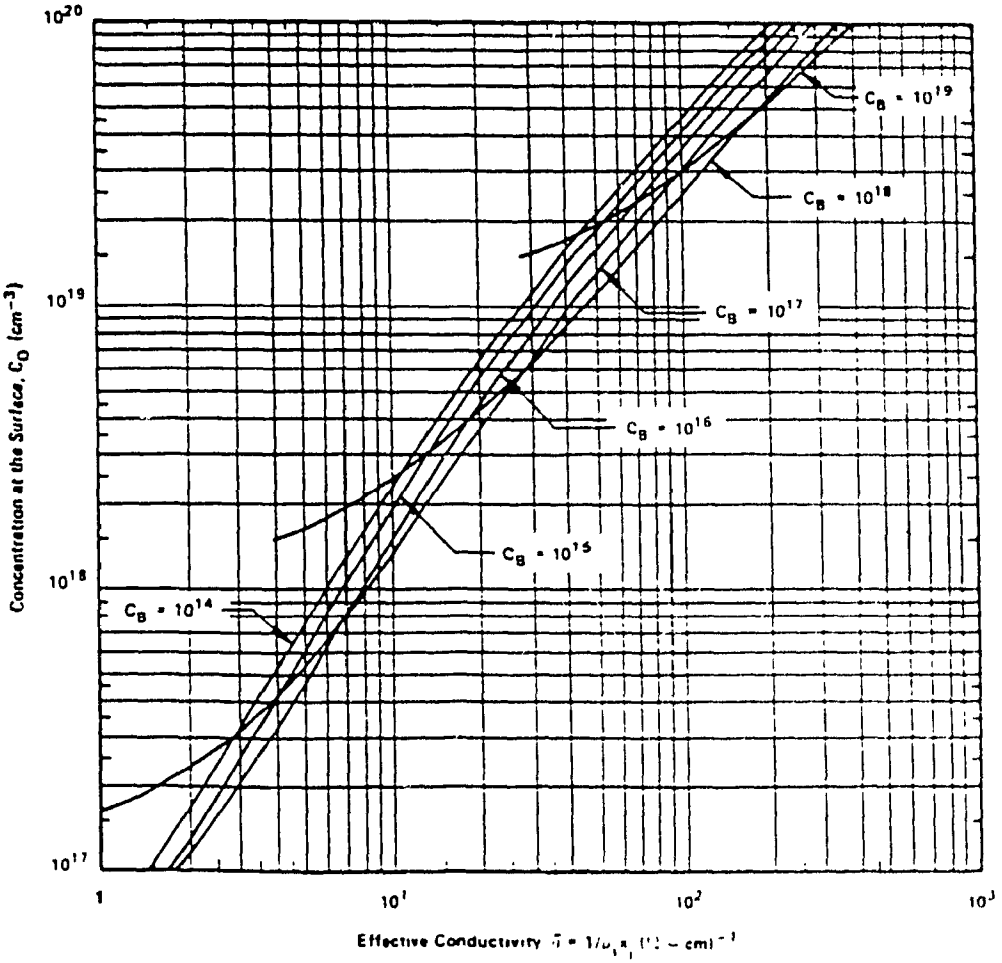


Figure A.6: Irvin curves for a p-type Gaussian impurity profile.

Appendix B

Sheet Resistance, The Bulk Resistance, and Ohmic contacts Measurement Procedures

B-1 Sheet Resistance

In the following, a Van der Pauw structure is shown and the procedures to measure the sheet resistances of the metallized and the diffused layers, using this structure, are described.

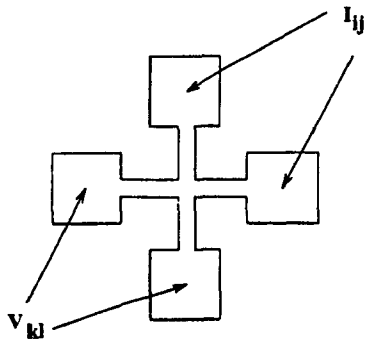


Figure B.1: Vander Pauw Structure.

place a probe tip at the center of each of the pads located around the Van der Pauw patteren's periphery and force a constant current between a pair of adjacent pads and measure the voltage across the remaining two. For each structure, there will be four separate I-V readings from which the layer's average sheet resistance can be

calculated from the following equation [16]:

$$R_{Ave \cdot sht} = \frac{\pi}{Ln2}\frac{1}{4}\left(\frac{V_{12}}{I_{34}} + \frac{V_{23}}{I_{41}} + \frac{V_{34}}{I_{12}} + \frac{V_{41}}{I_{23}}\right)$$

where $R_{Ave.sht}$ is the average sheet resistance of the diffused layer, I_{ij} is the current forced between a pair of adjacent pads, and V_{kl} is the measured voltage across the remaining two pads.

The tables 3, 4, and 5 show the measured I-V data for the metallization, phosphorous, and boron diffusion structures for the cell P_{24},respectively. In each table the corresponding average sheet resistance for each structure is shown.

	I (mA)	V (mV)	R_{sht} (Ω/❑)
	21.42	0.30	
	21.42	0.30	
	21.42	0.30	
Van der Pauw # 1	21.42	0.30	0.06
	21.35	0.30	
	21.35	0.30	
	21.35	0.30	
Van der Pauw # 2	21.35	0.30	0.06

TABLE 21. Van der Pauw results for cell P_{24} (metallization)

For each layer, the measurements were done for two independent Van der Pauw structure. The average sheet resistance for this specific sample, for layer of metallization, phosphorus, and boron was found to be 0.06 Ω/❑, 7.3 Ω/❑, and 37.6 Ω/❑ respectively. In these tables, the second column illustrate the values of applied cur-

rents forced between a pair of adjacent pads and the third column show the values of voltages appeared across the remaining two pads. The values in the fourth columns correspond to the sheet resistances for each of Van der Pauw structures.

	I (mA)	V (mV)	R_{sht} (Ω/❑)
	7.63	12.80	
	7.27	12.40	
	7.36	11.90	
Van der Pauw # 1	8.29	13.80	7.54
	8.03	12.60	
	8.12	12.60	
	8.5	13.20	
Van der Pauw # 2	8.36	12.90	7.04

TABLE 22. Van der Pauw results for cell P_{24} (phosphorous diffusion)

	I (mA)	V (mV)	R_{sht} (Ω/❑)
	1.53	12.50	
	3.7	31	
	4.84	40	
Van der Pauw # 1	3.76	30	37.14
	1.68	14.30	
	1.89	15	
	2.29	19.70	
Van der Pauw # 2	4.58	39.50	38.13

TABLE 23. Van der Pauw results for cell P_{24} (boron implantation)

B-2 Bulk Resistance

The bulk resistance, can be approximated by considering that the output current is divided equally between 13 sets of fingers at the rear side of the cell. The current passing from n finger to the p finger, will experience 3 different resistances due to the a) n finger, b) undoped bulk, and c) p finger. Knowing the values of the sheet resistances for the n finger and p finger, as well as the value of the bulk resistivity and the dimensions of the fingers, the value of the resistance from the middle of n finger to the middle of p finger can be calculated as follows:

$$R_n = R_{sht,n}(150/9980)$$

$$R_p = R_{sht,p}(50/9980)$$

$$R = R_{sht}\ (200/9980)$$

where R_n, R_p, and R, correspond to the resistances of the n and p diffused fingers, and the undoped region between the two fingers, respectively. The $R_{sht,n}$, $R_{sht,p}$, and R_{sht}, corresponds to the sheet resistances of those regions, respectively. The value of the R_{sht} can be found from the resistivity (ρ) and the thickness (W) of the wafer ($R_{sht}=\rho/W$).

Therefore, the resistance between n and p finger will be:

$$R_{n\text{-}p} = R_n + R_p + R$$

and the total bulk resistance will be

$$R_{bulk} = (R_{n\text{-}p})/25$$

B-3 N and P Contact Resistances

The basic technique used to measure contact resistance of ohmic contacts, employs a test structure composed of differently spaced ohmic contacts as illustrated in the following figure. The contacts have a width, W, and the pattern is isolated to restrict the current flow along the distance, L. The resistance between two contacts consists of the two contact resistance plus the resistance of the semiconductor layer between the two contacts. Therefore, the total resistance is

$$R = 2 \times R_c + (R_{sht}/W) \times L$$

where R_c is the contact resistance and R_{sht} is the sheet resistance of the region between the contacts.

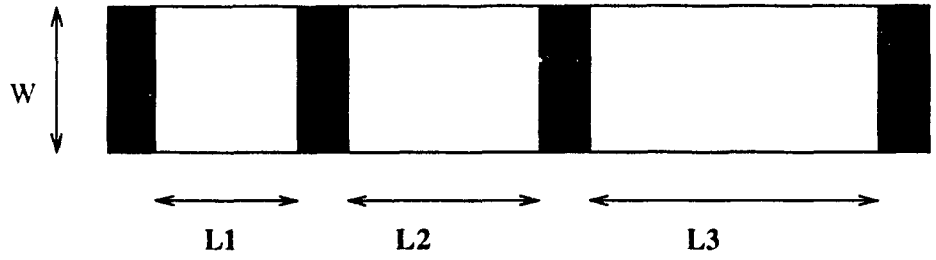


Figure B.2: Basic pattern used to experimentally determine the contact resistance.

Assuming the sheet resistance is constant, a plot of measured resistance as a function of spacing, L, will yield a straight line whose intercept with the R axis gives the value 2 x R_c. The figure B3, shows the plot of resistance versus spacing.

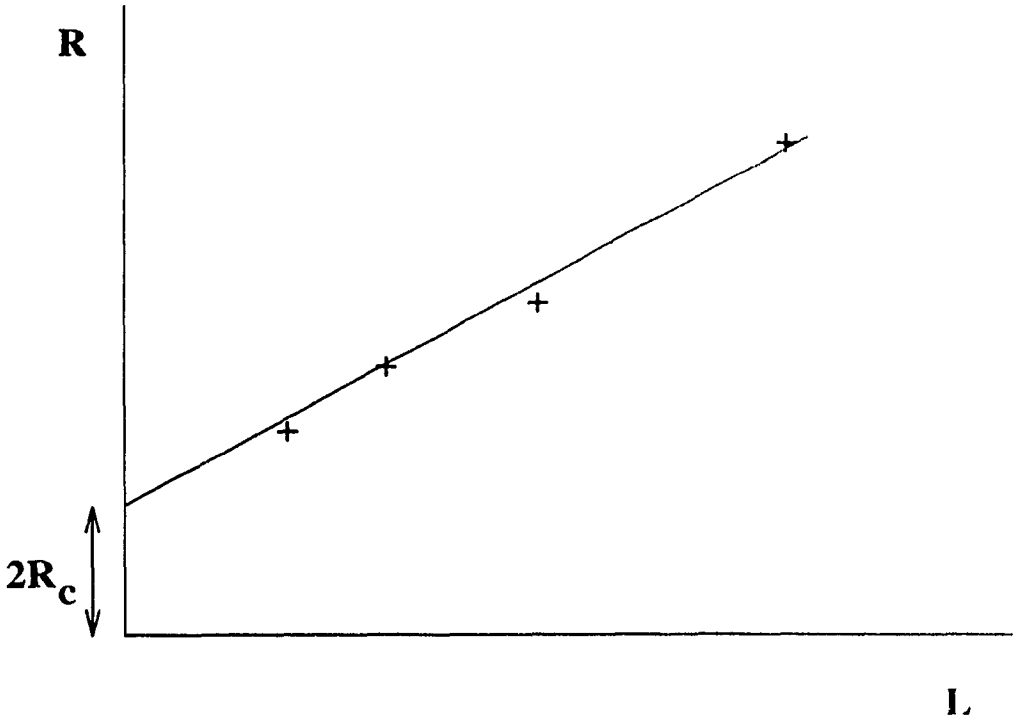


Figure B.3: Plot of measured resistance as a function of contact separation.

This method was used to measure the contact resistances of both n- and p-type contact structures shown on the mask #4. Then these values are used to estimate the values for the cell overall contact resistances. Recall that there are 13 n-type fingers and 7 contact structures on each finger, the overall contact resistance of the cell due to the n-type fingers, was obtained by parallel combinations of these structures. The same calculation was done in the case of p-type fingers.

Appendix C

Simulations

In the following, the programs written to simulate the p-n junction structures (the impurity profiles, the junction depth, and the surface concentration) using the SUPREM-IV, are shown.

C.1 Program # 1

This program simulates the boron profile within the n-type silicon substrate using sol-gel diffusion technique.

```
# some set stuff
set echo
option quiet
mode one.dim

# vertical definition
line x loc=0          spacing=0.02   tag=top
line x loc=1.5        spacing=0.02
line x loc=3.0        spacing=0.05
line x loc=4.0        spacing=0.05
line x loc=8.0        spacing=0.5    tag=bottom
```

```
# the silicon wafer
region silicon   xlo=top   xhi=bottom

# set the exposed surfaces
bound exposed xlo=top   xhi=top

#calculate the mesh
init phos conc=4.0 e14

# the boron diffusion card
diffuse time=120     temp=1100     boron gas.conc=5e20

# plot the initial profile
sel z=log10(abs(boron-phos))
plot.1d     x.max=8.0      y.min=13.0      y.max=21.0

pause

# the diffusion card
method init=1.0e-3 two.d
diffuse time=60 temp=1000 wet

# plot the next profile
sel z=log10(abs(bor-phos))
plot.1d cle=f axi=f
```

```
pause

# the annealing card
diffuse time=88 temp=1000

# save the data
structure out=boron.str

# plot the final profile
sel z=log10(abs(boro-phos))
plot.1d cle=f axi=f

pause
```

****----------****

C.2 Program # 2

This program simulates the phosphorus profile within the n-type silicon substrate using sol-gel diffusion technique.

```
# some set stuff
set echo
option quiet
mode one.dim
# vertical diffusion
```

```
line x loc=0          spacing=0.02        tag=top
line x loc=1.5        spacing=0.02
line x loc=3.0        spacing=0.05
line x loc=5.0        spacing=0.5
line x loc=8.0                            tag=bottom

# the silicon wafer
region silicon   xlo=top   xhi=bottom

# set the exposed surfaces
bound exposed   xlo=top   xhi=top

# calculate the mesh
init phos conc=4.0e14

# phos diffusion
diffuse time=60 temp=1000 phos gas.conc=5e20

# plot the initial profile
sel z=log10(phos)
plot.1d   x.max=8.0   y.min=14.0   y.max=21.0

pause

# the diffusion card
method init=1.0e-3 two.d
```

```
diffuse time=13 temp=1000 wet

# plot the second profile
sel z=log10(phosp)
plot.1d cle=f axi=f

pause

# the diffusion card
diffuse time=15 temp=1000

# save the data
structure out=phos.str

# plot the final profile
sel z=log10(phosphor)
plot.1d cle=f axi=f
pause
```

****----------****

C.3 Program # 3

This program simulates the boron profile within the n-type silicon substrate using ion-implantation technique.

```
# some set stuff
```

```
set echo
option quiet
mode one.dim

# vertical diffusion
line x loc=0          spacing=0.02          tag=top
line x loc=1.5        spacing=0.02
line x loc=3.0        spacing=0.05
line x loc=4.0        spacing=0.05
line x loc=8.0        spacing=0.5           tag=bottom

# the silicon wafer
region silicon   xlo=top   xhi=bottom

# set the exposed surfaces
bound exposed   xlo=top   xhi=top

# calculate the mesh
init phos conc=4.0e14

# the uniform boron implant
implant boron dose=1.0e16 energy=50 gauss

# plot the initial profile
sel z=log10(abs(boron-phos))
plot.1d   x.max=8.0   y.min=13.0   y.max=21.0
```

```
pause

# the diffusion card
method init=1.0e-3 two.d
diffuse time=60 temp=1000 wet

# plot the next profile
sel z=log10(abs(bor-phos))
plot.1d cle=f axi=f

pause

# the annealing card
diffuse time=88 temp=1000

# save the data
structure out=boron.str

# plot the final profile
sel z=log10(abs(boro-phos))
plot.1d cle=f axi=f

pause
```

****----------****