Generation, Design and Optimization of Stray Insensitive SC Networks

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ABSTRACT

Generation, Design and Optimization of Stray Insensitive SC Networks

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A systematic and comprehensive approach for the generation, design and optimization of stray insensitive switched capacitor networks is proposed in this thesis. Special emphasis is given to circuits employing one and two operational amplifiers (OAs). Towards this end, the parasitic insensitivity conditions reported earlier in the literature are exploited in developing the generation procedure. The study of single OA networks leads to a step-by-step generation and design procedure which allows, many times, considerable improvements in already existing designs. The investigation of second order networks (two OAs) yields 23 new biquads, some of which allow designs with minimum number of capacitors. The five parasitic insensitive general biquads reported so far in the literature are also derived in the process. Finally, a computer-aided procedure to reduce the integrated circuit area required to realize a given discrete transfer function by a switched capacitor network is proposed. The method minimizes the total capacitance of the final network implementation. Tradeoffs between total capacitance and

network sensitivities are discussed. Examples are given to demonstrate the possibility of design improvement by using the techniques introduced in this thesis. Extensive laboratory tests confirm the validity of the techniques presented in this thesis.

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TO MY MOTHER AND MY FATHER

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CHAPTER I

INTRODUCTION

1.1 PRELIMINARY CONSIDERATIONS

Metal-Oxide-Semiconductor (MOS) integrated circuit technology is unique in its ability to store signal carrying charge packages for relatively long periods of time, to move such packages under clock control and to continuously sense the charge without destroying the information (high input impedances). This inherent analog memory capability has been widely exploited in the design of dynamic logic circuits and dynamic random access memories. Another attraction of MOS technologies is the fact that its transistor structure is much simpler than the bipolar structure, allowing higher integrated circuit densities. Furthermore, MOS circuits consume much less power than their bipolar counterparts.

As a result of continuous advances in MOS technology, increasingly powerful digital signal processors have replaced analog circuitry in many application areas. However, the electrical signals on which these processors operate are usually continuous-time analog quantities, such as speech, to quote one example. Consequently, interface circuits are required to interconnect the analog and digital environments. Typical interface functions are

amplification, filtering and analog to digital as well as digital to analog conversions. It is highly desirable from economic standpoint to have these interfaces incorporated with the digital circuitry in a single large scale integration (LSI) chip. It has also been shown that, by slightly modifying the MOS technology to include precision MOS capacitors, the same inherent technological capabilities of the original MOS processes can be used to realize analog functions in a form compatible with the high density, low-cost digital LSI circuitry.

About a decade ago, analog to digital conversion was first implemented by all-MOS circuits using charge redistribution techniques [1,2]. It was found that with proper design, the monolithic MOS capacitor possessed remarkably stable characteristics in terms of its voltage and temperature coefficients (typically 10-50 ppm/^{o}C and 20-200 ppm/V, respectively [3]). The absolute value of the capacitance, however, exhibited random processing variations of the order of 10 to 20 percent. This limitation was soon overcome by the development of design techniques in which the precision analog quantities were defined by ratios of MOS capacitors, instead of by their absolute values. With proper layout techniques ratios of monolithic MOS capacitors are reproducible with accuracies of 0.1% [3,4,5]. Also, by the same time, an internally compensated MOS operational amplifier (OA) was developed [6].

One of the areas of application which has benefited most from the development of MOS technology for the implementation of analog circuits is telephony, through the utilization of switched capacitor (SC) filters.

SC circuits are sampled-data analog systems, and as such they occupy an intermediate position between fully analog (continuous time/continuous amplitude) and fully digital (discrete time/discrete amplitude) systems. For filtering applications, in particular, they offer several advantages over fully analog circuits. They can be completely integrated yielding compact, reliable and inexpensive (for large volume applications) filters. Their frequency responses are controlled by clock signals. Hence, these filters can be easily synchronized, multiplexed and programmed.

Compared to an equivalent digital filter, the SC realization usually requires a less complicated structure and often much less chip area on an integrated circuit. On the other hand, its accuracy is limited to the equivalent of about 10 bits (0.1% accuracy in the capacitance ratios). This may prevent the use of SC filters in applications where very high accuracy is critically important. Therefore, SC and digital fiters tend to have complementary applications and are usually not directly competitive in any situation.

1.1.1 Introduction to SC Filters

High quality analog filters had been historically realized as passive RLC circuits. However, inductors are physically large, electrically lossy and noisy, and unsuitable for miniaturization. Consequently, an effort to replace them by active elements began in the sixties with the appearance of the RC-active filters. This type of filter has gained wide acceptance since then, specially for applications in the voice frequency range (0 - 4kHz). In order to reduce their physical size, RC-active filters are often implemented in a hybrid form, by using thick-film or thin-film technologies. Thick film circuits consist of resistive inks fused onto the surface of a ceramic substrate and monolithic operational amplifiers (OAs) bonded onto the substrate. Since good quality thick-film capacitors are not easily obtained, usually discrete capacitors are externally soldered to the circuit. Thin-film circuits consist of resistors "and" capacitors deposited on a ceramic or alumina substrate. The film thickness used is considerably less than in the thick-film process. As in thick film circuits, monolithic OAs are soldered onto the substrate.

The next step towards miniaturization is to realize fully integrated (monolithic) filters. For the advantages previously discussed, MOS technology is usually preferred over the bipolar technology for filtering applications. The integration of RC-active filters, however, presents some

difficulties. Due to the area they occupy in the chip, MOS capacitors are seldom made larger than about 100pF (a 1pF capacitor occupies an area of about $200\mu m^2$). Since for filtering applications in the voice frequency range time constants of the order of $RC \cong 10^{-4}$s are required, a reasonably large capacitor (say, C=10pF) would require a resistor R of the order of $10^7\Omega$. Such a resistor would occupy an area around $10^6\mu m^2$, which is approximately 10% of the average chip area of an entire analog MOS integrated circuit [7]. Furthermore, MOS resistors tend to be nonlinear. Also, since both capacitors and resistors have, at present, absolute accuracies of only 5 to 10 percent, and their errors are not correlated, the overall error of a RC time constant can be as high as 20%. This error will also vary with the temperature and the signal level.

Switched capacitor techniques offer an elegant solution to this problem in MOS technology. The basic principle of operation is very simple. Early researchers in the area of SC filters visualized the possibility of simulating the characteristics of a resistor by switching a capacitor between two circuit nodes using a high frequency clock signal. Consider, for example, the circuit of Fig. 1.1(a). This circuit is composed by a capacitor C and two analog switches. The switches are closed (short circuited) and open (open circuited) alternately, according to the clock signal represented in Fig. 1.2.

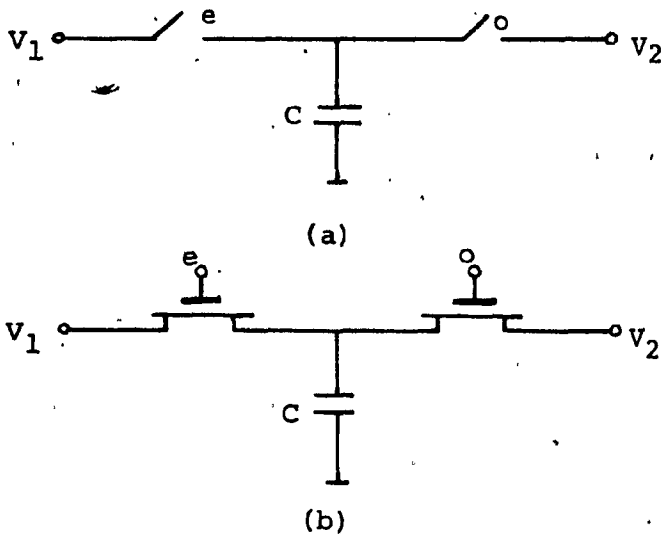


Figure 1.1: Resistor equivalent

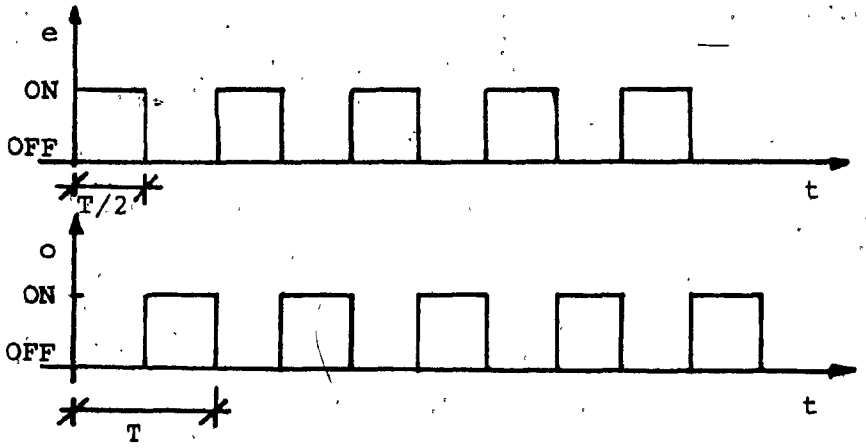


Figure 1.2: Biphase non-overlapping clock signal

e : even phase

o : odd phase

When the even phase of the clock signal is "ON" (high voltage level), the even switch is closed and, because of the non-overlapping nature of the two clock phases, the odd switch (o) is open (odd phase is "OFF"). In the next clock phase (odd), the positions are reversed - The even switch is open and the odd switch is closed. This operation is repeated at the clock rate $f_s=1/T$, T being the entire clock period, as shown in Fig. 1.2. The clock rate f_s is also often referred as the sampling rate or the sampling frequency in the SC literature.

During the even phase, capacitor C is charged to the voltage v_1 and, during the odd phase, C is charged to the voltage v_2. The amount of charge that is transferred between the two nodes is then given by

$$\Delta Q = C(v_1 - v_2) \tag{1.1}$$

Since the switching operation is repeated at frequency f_s, the average current passing from v_1 to v_2 can be calculated as

$$I = \Delta Q f_s = C f_s (v_1 - v_2) \tag{1.2}$$

If the switching rate is much higher than the signal

frequencies of interest, the time sampling effect can be ignored in a first-order analysis and the switched capacitor C can be considered as a direct replacement of a conventional resistor R with the value

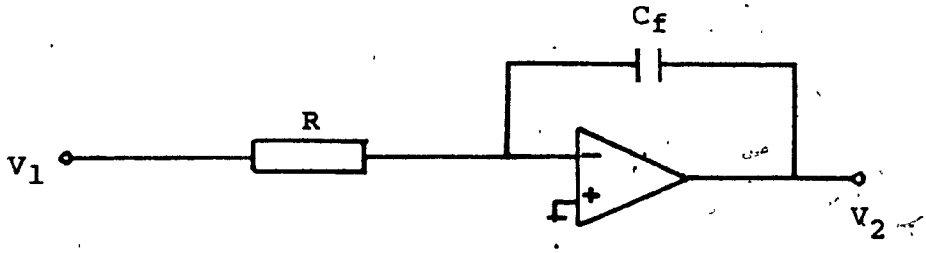
$$R = \frac{1}{Cf_s} \tag{1.3}$$

For example, a resistance of 1MΩ can be obtained by switching a 10pF capacitor at 100kHz.

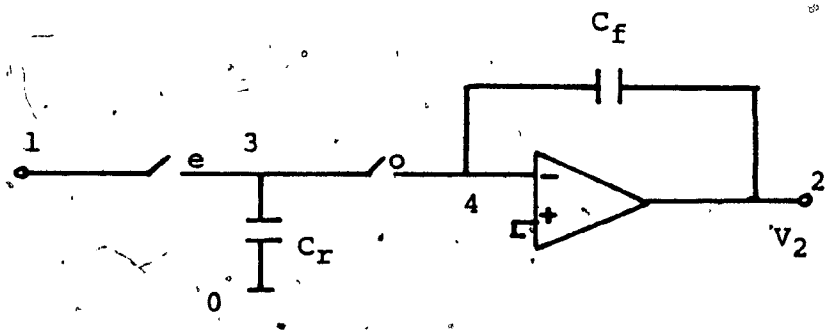
The switches are implemented by two MOS transistors, as shown in Fig. 1.1(b). Note that now very little silicon area is needed to implement significant resistance values. As a matter of fact, the area (which is proportional to the capacitance value) decreases as the required resistance increases.

This resistor equivalence arrangement was used in the early stages of the development of SC filters. The idea was to replace directly the resistors used in the well known RC-active structures [7,8,9]. Consider, for example, the integrator circuit shown in Fig. 1.3(a). The s-domain voltage transfer function of this network, considering ideal elements, is given by

$$\frac{V_2}{V_1} = -\frac{1}{sRC} \tag{1.4}$$



(a)



(b)

Figure 1.3: Resistor equivalence applied to an integrator circuit.

Now, consider the arrangement in Fig. 1.3(b). Here the resistor has been replaced by the switched capacitor $C_r=1/(Rf_s)$, according to (1.3). Then, by the resistance equivalence concept, the switched capacitor integrator has the same transfer function with the new time constant

$$RC = \frac{C_f}{C_r} \cdot \frac{1}{f_s} \tag{1.5}$$

Hence, the integrator response is now determined by the capacitor ratio C_f/C_r. This result is vital for the success of the SC technique. It implies that the frequency responses of filters composed by such integrators are determined solely as functions of capacitance ratios. Since capacitance ratios can be obtained with high precision in the MOS fabrication process, very compact and highly reliable circuits can be realized.

It soon became clear, however, that the time delay through the switched capacitor integrators, when employed in a larger network, could lead to significant errors (even compromising the circuit stability) in predicting the network behaviour [10,11]. Thus, the idea of direct resistor equivalences has been gradually abandoned. Nevertheless, the potential ability of the SC networks in realizing high-precision monolithic integrated analog MOS

circuits was, in the process, revealed.

At present, SC networks are regarded as a distinct class of discrete-time networks and not as an alternative implementation for continuous-time counterparts. Exact analysis methods employing the z-Transform have been developed in order to predict correctly the network behaviour [12,13]. Thus, with proper z-domain based designs, SC techniques allow precision filters to be produced in monolithic form without the need for trimming or recalibration. They represent the latest design techniques for filter networks over the RC-active techniques of the sixties and seventies.

Since the late seventies, various design procedures and new structures have been proposed for the synthesis of SC filters. The development of these design methodologies followed very closely the paths used for the design of RC-active networks. Large majority of the designs proposed so far are based on component simulations (resistances and inductances), operational simulation of passive RLC ladder networks or on the interconnection (mainly in cascade form) of first and second order (biquads) building blocks. Again, as in the RC-active case, while the ladder network designs tend to yield realizations with very low sensitivities at the cost of more complicated synthesis procedures, the building blocks approach offer high modularity and easy to design networks at the expense of a degradation on the

sensitivity performance. However, for SC networks, the inherent capacitance ratio accuracy reduces considerably the effects of the increased sensitivities to element variations on the realized transfer function. This fact allows the designer of SC networks to be more tolerant with respect to acceptable sensitivity performances in the design process. Sensitivity values which would be considered unacceptable for a RC-active network are, many times, routinely tolerable in a SC network. Consequently, as it should be expected, the simpler and modular approach of filter design using first and second order building blocks has enjoyed large popularity on the synthesis of high order SC filters.

Any technology, no matter how good it might be, has its own inherent drawbacks for a specific type of implementation. These drawbacks have to be overcome by improving the fabrication process and/or by using special circuit theory techniques in the generation of the network topologies to be employed. Switched capacitor networks are no exception to this rule. Technological problems such as noise generated by the different components, leakage currents of the MOS transistors, low open-loop gain and poor power supply noise rejection of the MOS OAs, among others, must be considered in the design of the final chip layout in order to guarantee a good filter performance [3,5]. Among the problems inherent to the SC technology which should be considered during the network topology generation step, one

of the most important ones is, undoubtedly, the influence of the various parasitic capacitances created in the fabrication process on the frequency performance of the filter. Their effects and the solution to the problem are the subject of the next section.

1.2 STRAY INSENSITIVITY CONDITIONS

In the analysis of an actual SC network, parasitic capacitances to the substrate (ac ground) from the various switch terminals (specially drain and source), from the routing lines interconnecting the network elements and from the capacitor plates will provide an error in the definition of the transfer function coefficients if not properly considered [4,5]. Since capacitances of the order of 1pF (often as small as 0.1pF) are currently employed in integrated SC circuits, the parasitic capacitances from the various nodes of the circuit to the ground node cannot be neglected or even considered to be small. Furthermore, the values of the parasitic capacitances in a MOS circuit are strongly dependent on the specifics of the fabrication technology employed and, many times, on the operating points of the different MOS devices within the same circuit [3]. Moreover, the stray capacitance associated with a given node is typically nonlinear in nature [3,4,5] and its value will depend on the number and types of the circuit elements connected to that node. Therefore, the values of the various parasitic capacitors of a SC circuit should be

regarded as completely independent of each other.

In order to illustrate better the influence of the stray capacitances on the electrical behaviour of the network, consider again the SC integrator of Fig. 1.3(b). The analysis of this network (analysis procedures are reviewed in the next section) reveals that the ratio of the output voltage V_2 to the input voltage V_1, both sampled in the even phase of the clock signal, is given by

$$\frac{V_2^e}{V_1^e} = -\frac{C_r}{C_f}\frac{z^{-1}}{1 - z^{-1}} \tag{1.6}$$

Now, if the parasitic capacitance, say C_p, existing from node 3 to ground is considered, it would be always in parallel with C_r. Consequently, the actual voltage transfer function of the integrator is given by

$$\frac{V_2^e}{V_1^e} = -\frac{C_r + C_p}{C_f}\frac{z^{-1}}{1 - z^{-1}} \tag{1.7}$$

Since typical values for C_p, which includes all the stray capacitances from that node to ground, can be considered to reach around 5% of the value of C_r, a corresponding error will exist for each gain constant within any network containing the integrators if they are designed according to equation (1.6). Such design inaccuracies may

lead to intolerable errors in the network frequency response. Fortunately, the errors due to parasitic capacitances may be eliminated through proper circuit design techniques.

In what follows, we will be dealing with the most popular type of SC networks, namely the biphase SC networks, in which the clock signal is provided by two non-overlapping phases (here termed even and odd) with a 50% duty cycle [4,5], as per Fig. 1.2. The 50% duty cycle condition can be relaxed most of the times and is used only for the sake of simplicity of expressions. Moreover, for all purposes, capacitors, switches and OAs will be considered ideal, except for their parasitic capacitances which cannot be disregarded for any operating frequency range or signal amplitude levels. Ideal capacitors are lossless elements, with no leakage current associated with them. Ideal switches are considered to be perfect short-circuits when closed (zero "ON" resistance) and perfect open circuits when open (infinite "OFF" resistance). Ideal OAs are differential amplifiers with infinite DC open-loop gain, infinite input impedance, zero output impedance and infinite bandwidth. As a consequence of these considerations, the main application of the circuits studied in this thesis will be in the area of voice band signal filtering. However, the majority of SC filters are, at present, used in this area.

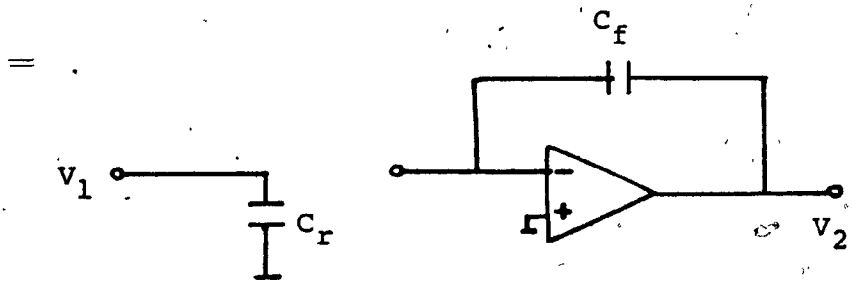
A set of conditions which guarantees the stray insensitivity of a biphase SC network for applications in this frequency range has been proposed by Hasler in [14]. Since these conditions are extensively used in this thesis, they are reviewed here for the sake of continuity.

A parasitic insensitive network is defined as a network whose any z-domain voltage transfer function, regardless of which are the input and output variables, is independent of the parasitic capacitances of the network elements. The network formed when all "even switches" are closed (open) and all "odd switches" are open (closed) will be called "even (odd) circuit". As an example, Fig. 1.4 shows the even and odd circuits corresponding to the integrators of Fig. 1.3(b).

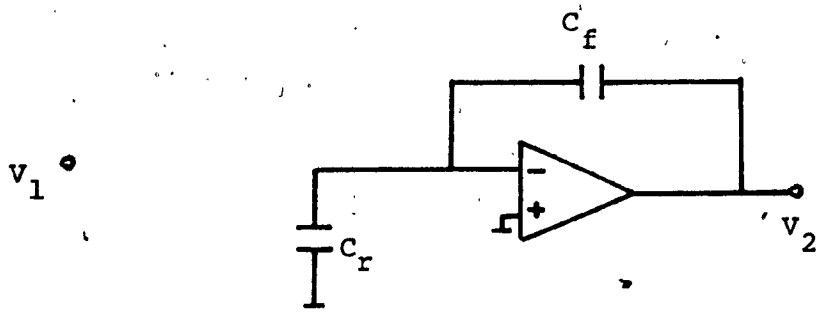
The parasitic insensitivity conditions formulated in [14] for a typical node, say n, of a biphase SC network are:

Condition 1 - Every node in both the even and odd circuits of a SC network must be a V-node (input voltage source or an OA output), a virtual ground (I-node) or the ground node.

Condition 2 - The switching of any node n between a V-node and an I-node in consecutive phases is permitted only if the voltage of the V-node is set to zero during the phase in which it is connected to node n.



(a)



(b)

Figure 1.4: (a) Even circuit associated with the integrator in Fig. 1.3(b).
(b) Corresponding odd circuit.

Clearly, the integrator of Fig. 1.3(b) is not stray insensitive since node 3 violates condition 2 above.

Due to wide applicability of the first and second order SC building blocks, it appears desirable to have a systematic and efficient method to generate such networks. It is also interesting to generate them in such a way that their parasitic insensitivity is guaranteed. The usual approach to such generation procedures has been to build the networks as interconnections of simpler blocks which are already known to be stray insensitive [15,16,17,18,19]. Even though this kind of approach has led to networks with good performance, it clearly does not exploit the full potential of the available technology. Recently [20], the parasitic insensitivity conditions just discussed have been used to obtain general building blocks for first and second order networks. Unfortunately, however, the method proposed in [20] leads to oversized general networks containing redundant elements which have to be deleted by inspection, an extremely laborious process, specially in the case of second order networks. Moreover, no practical procedure has been proposed in order to reduce the universal biquad to structures of manageable sizes. Further, the simplest possible connection of a capacitive terminal to any network node, namely by a short-circuit, has to be implied by the parallel combination of an even switch and an odd switch. Finally, the possibility of a switch placed across the OA in

single OA networks (commonly used in the designs of amplifiers and delay networks) [21,22,23] can be obtained from the proposed formulation only as a limiting case, where a capacitance value is made infinitely large.

It therefore appears desirable to investigate further the generation of parasitic insensitive networks in order to explore the possibilities of obtaining systematic procedures that yield practical and simple networks. Such a method should lead directly to the minimum size of the most general parasitic insensitive structure for a given number of OAs. At this stage, it is worthwhile to review briefly some analysis techniques which are used extensively in this thesis.

1.3 ANALYSIS OF SC NETWORKS

The available literature in the analysis of SC networks is very extensive. However, in order to understand and reproduce all the network analyses performed in this thesis, only very simple techniques are necessary. Therefore, in what follows, a summary of the analysis concepts used in this work is presented.

1.3.1 Analysis of SC Networks by Inspection

All networks discussed in this thesis (and most of the SC networks available in the literature) can be viewed as a combination of first order circuits. Thus, by means of

an example, we illustrate here how these circuits can be analyzed by inspection. Once the analysis of each building block is performed, the analysis of the complete network is merely a question of solving a system of equations.

Consider the network in Fig. 1.5. The charges q_1 and q_2 stored in the capacitors C_1 and C_2, respectively, have been assigned arbitrary polarities. In order to determine the z-domain voltage transfer functions of this network, it is enough to determine the Charge Conservation Equations (CCEs) at the virtual ground (node 3) for both clock phases. The CCEs associated with a given node are nothing but the charge equivalents of the Kirchoff Current Law (KCL) equations or, in other words, they express the same principle of energy conservation in terms of the charges stored in the capacitors. Since SC networks operate with discrete charge transfers (and not with continuous current flows), the solution of the network CCEs represents the natural analysis approach to this type of networks. The CCEs state that, for every network node and for each clock phase, the sum of the charge variations of all capacitances connected to that node equals zero.

The general equation for the variation of the charge stored in a capacitor C between two time instants t_1 and t_2 $(t_2>t_1)$ is given by

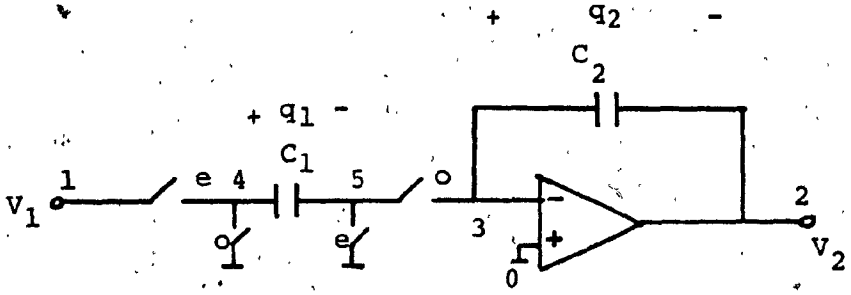


Figure 1.5: Switched capacitor integrator.

$$\Delta q = q(t_2) - q(t_1) = C[v_c(t_2) - v_c(t_1)] \qquad (1.8)$$

where v_c stands for the voltage across capacitor C. Thus, considering t=nT the sampling instants of the even phase and t=nT+kT/2 the sampling instants of the odd phase, the CCE relative to node 3 in the even phase (t=nT) can be written as

$$C_2[-v_2(nT) + v_2(nT-T/2)] = 0 \qquad (1.9)$$

since only C_2 is connected to node 3 in the even phase and the voltage at node 3 (virtual ground) is always equal to zero. The CCE for the odd phase (t=nT+T/2) yields

$$C_1[0 + v_1(nT)] + C_2[-v_2(nT+T/2) + v_2(nT)] = 0 \qquad (1.10)$$

Note that the final voltage across C_1 is zero because the capacitor is short-circuited by the virtual ground in the odd phase. Equation (1.9) leads to the conclusion that

$$v_2(nT) = v_2(nT-T/2) \qquad (1.11)$$

and, consequently, from (1.10) and (1.11)

$$C_2[v_2(nT+T/2) - v_2(nT-T/2)] = C_1 v_1(nT) \tag{1.12}$$

Applying the z-Transform [24,25] to (1.12) yields, in the z-domain,

$$C_2[z^{1/2}V_2^o(z) - z^{-1/2}V_2^o(z)] = C_1 V_1^e(z) \tag{1.13}$$

where the superscripts e and o are used to identify the specific phase in which the voltage signal is being taken. Equation (1.13) can be re-arranged as

$$C_2 V_2^o(z)(1 - z^{-1}) = C_1 z^{-1/2} V_1^e(z) \tag{1.14}$$

Similarly, the application of the z-Transform to (1.11) yields

$$V_2^e(z) = z^{-1/2} V_2^o(z) \tag{1.15}$$

meaning that $v_2(t)$ changes its amplitude only during the odd phase. Such amplitude is then held constant for the even phase. Equations (1.14) and (1.15) combined lead to

$$\frac{V_2^o(z)}{V_1^e(z)} = \frac{C_1}{C_2} \frac{z^{-1/2}}{1 - z^{-1}} \qquad (1.16)$$

and

$$\frac{V_2^e(z)}{V_1^e(z)} = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \qquad (1.17)$$

Note that, in general, a biphase SC network with one input and one output will have four possible voltage transfer functions, depending on the sampling instants chosen for the input and output voltages.

1.3.2 Switching Matrices

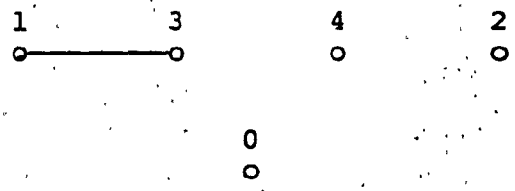
The "switching scheme" of a SC network is defined as the circuit obtained from the original network when all the capacitors are removed. Consequently, the switching scheme determines how each of the network nodes, independently of any capacitive connection, is switched to the other existing nodes during both the even and the odd phases. According to the conditions discussed in the last section, the ways in which a given node is switched determine the parasitic insensitivity of the network. Hence it is important to have a way of mathematically representing the switching scheme of a SC network. To this end, the switching matrices S_e (even phase) and S_o (odd phase) defined in [12] are used in this work. The definition of

their entries for a biphase circuit is given here for convenience.

Consider the "even (odd) closed switch network" as the network resulting from the original one when all the elements, excepting the closed even (odd) switches are removed. The entries of S_e (S_o) are defined as follows:

$$S_{ij} = \begin{cases} 1, \text{ if } i \text{ is the lowest numbered node of a separate part of the even (odd) closed switch network and } j \text{ belongs to that separate part.} \\ 0, \text{ otherwise.} \end{cases}$$

Even though this definition may be hard to understand, it turns out to be very easy to apply. Two examples are presented here in order to clarify the definition of the switching matrices since they are of major importance in the development of the present work. Consider, as a first example, the network in Fig. 1.3. Note that the ground node is numbered zero. This is usually done because a row in S_e (S_o) correponding to the reference node is not necessary. Fig. 1.6 shows the two graphs termed even closed and odd closed switch networks corresponding to this circuit. Note that the graphs are obtained by placing all network nodes and then simply connecting, by means of branches, the nodes which are connected by the even or odd switches in the original network, depending on the case. The separate parts



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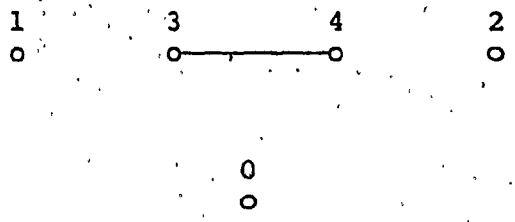


(b)

Figure 1.6: Graphs used to determine S_e and S_o (Ex. 1).
(a) Even closed switch network.
(b) Odd closed switch network.

mentioned in the definition are then readily available.

Now, the lowest numbered node of each separate part is identified, namely 0, 1, 2 and 4 for the even closed switch network and 0, 1, 2 and 3 for the odd closed switch network. Thus, only those rows of S_e (S_o) corresponding to these numbers (excepting the zero) will have nonzero elements. These 1's will appear in the position of a given row corresponding to the main diagonal of the matrix (position (i,i)) and in the positions corresponding to the other nodes connected to the same separate part. Then, from Fig. 1.6 one obtains

$$S_e = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \end{array} \begin{array}{c} \begin{array}{cccc} 1 & 2 & 3 & 4 \end{array} \\ \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \end{array}$$

and

$$S_o = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \end{array} \begin{array}{c} \begin{array}{cccc} 1 & 2 & 3 & 4 \end{array} \\ \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \end{array}$$

As a second example, let us consider the integrator in Fig. 1.5. The even closed and odd closed switch networks are shown in Fig. 1.7, where the different separate parts can be easily identified. The use of the definition of the switching matrices yields

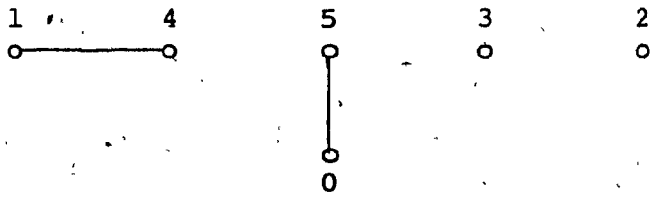
$$S_e = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array} \begin{array}{c} \begin{array}{ccccc} 1 & 2 & 3 & 4 & 5 \end{array} \\ \begin{bmatrix} 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{array}$$

and

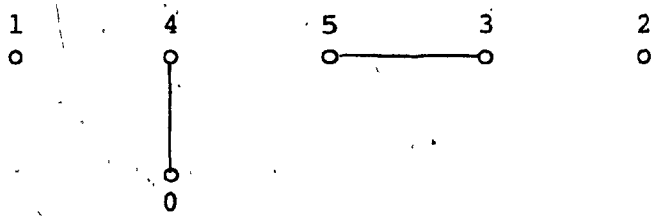
$$S_o = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array} \begin{array}{c} \begin{array}{ccccc} 1 & 2 & 3 & 4 & 5 \end{array} \\ \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{array}$$

Note that a node switched to ground gives rise to a row and a column of zeros in the switching matrix of the corresponding phase (e.g., node 5 in the even phase and node 4 in the odd phase).

A very important feature of these switching matrices is that they uniquely determine the switching



(a)



(b)

Figure 1.7: Graphs used to determine S_e and S_o (Ex. 2).

(a) Even closed switch network.

(b) Odd closed switch network.

scheme of the network. It is this property that makes such matrices attractive for use in a synthesis procedure.

1.3.3 Pole Placements

Whenever a new network topology is devised for the implementation of a given type of transfer function, it is appropriate to consider the stability and realizability of the proposed circuit. If the new topology is intended to be useful in any application, it is expected to be able to realize all stable pole positions. For sampled-data networks this means the realization of poles anywhere within the unit circle in the z-domain [24,25]. Since in this thesis the design of biquadratic transfer functions is emphasized, the study of the realizable pole positions by a given second order network is reviewed here. A similar study for the cases of first order transfer functions, which are also studied in this thesis, is trivial and can be done by inspection.

The stability conditions for a biquad whose transfer function H(z) is written in the form

$$H(z) = \frac{\gamma + \varepsilon z^{-1} + \delta z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}} \qquad (1.18)$$

can be conveniently expressed [26] in the α, β parameter space by means of the area within the triangle shown in

Fig. 1.8. The upper parabolic area of the triangle represents the values of α and β for stable, complex poles. The remainder of the upper triangular area, where $\beta>0$, corresponds to pairs of real poles which lie either to the left or to the right of $z=0$. The lower portion of the triangle, where $\beta<0$, corresponds to real poles which lie on alternate sides of $z=0$. Clearly, the upper portion of the triangle ($\beta>0$) represents the most useful pole locations for frequency selective filters.

Therefore, in order for a biquad to be considered as a general structure in terms of pole placement realizations it should, at least, be able to realize any pole positions within the upper parabolic area of the triangle in Fig. 1.8 (complex poles). The inequalities describing the stability triangle are given by

$$\beta \leq 1 \tag{1.19}$$

$$\alpha + \beta \geq -1 \tag{1.20}$$

$$\alpha - \beta \leq 1 \tag{1.21}$$

These inequalities can be used to easily determine the pole placement capabilities of a given structure.

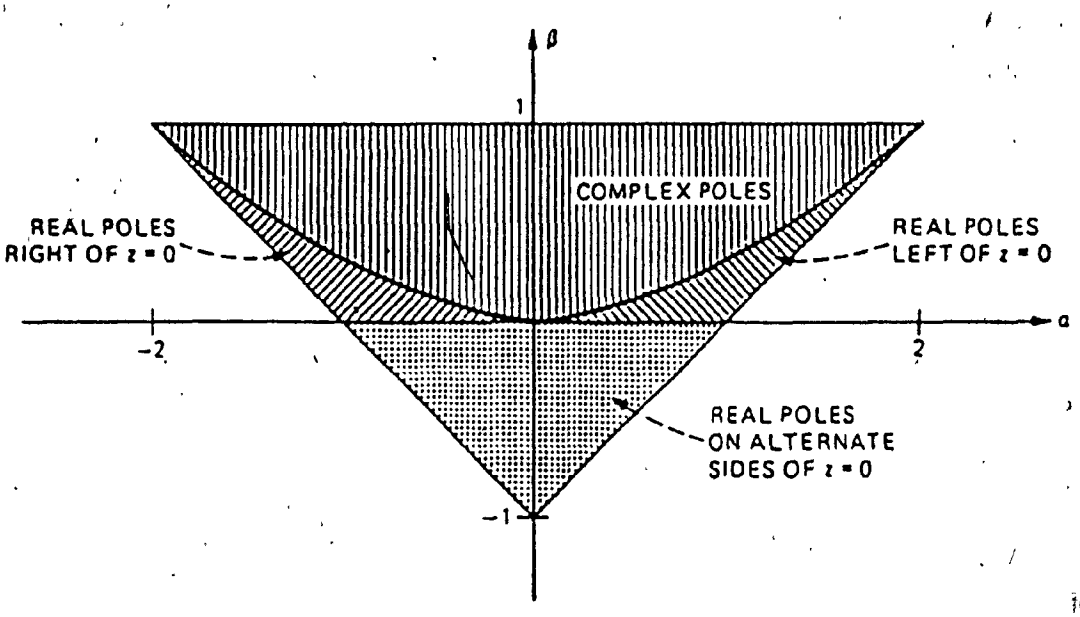


Figure 1.8: Stability region in the α, β plane for a biquadratic transfer function.

1.4 SCOPE OF THE THESIS

The aim of this thesis is to develop systematic and comprehensive procedures for the generation of stray insensitive biphase SC networks. Single OA and biquadratic (second order) networks are given special attention due to their wide applicability. Further, a method is proposed for the optimization of SC networks. The method aims at the minimization of the total silicon chip area required in the realization of a given transfer function.

Towards this end, the parasitic insensitivity conditions presented in [14], in conjunction with the definition of the switching matrices for biphase SC networks [12], are employed in order to obtain the most general switching scheme of a stray insensitive SC network with a given number of OAs.

The method is introduced in Chapter II for the generation of single OA networks. Then, the obtainable networks are classified and, for each class, a complete study is performed in order to determine all possibly realizable transfer functions along with the necessary conditions for their realizability. Then, the application of the different types of input signal waveforms and the ways to guarantee the desired voltage waveform at the output are studied. The possible ways to realize the various transfer functions without any matching conditions on the

network elements are then determined.

In Chapter III, the network generation procedure is extended to the case of second order networks. Then, the concept of "capacitor switching networks" (CSNs) is introduced. This concept allows the generation of canonic (minimum number of elements) or quasi-canonic biquad building blocks by manipulating only small subnetworks of the most general biquad without, however, losing any generality on the generation process. A total of 28 networks is derived. The complete set includes the 5 stray insensitive biquads presented so far in the literature. The remaining 23 networks are completely new. Design equations are provided and dynamic range scaling as well as spread and total capacitance minimization are discussed.

In Chapter IV, a new optimization algorithm is proposed to minimize the chip area necessary for the realization of a discrete transfer function. By allowing a controlled increase in the number of elements, the total capacitance is minimized by an algorithm which is partly numerical and partly analytical. The proposed method allows the optimization to be performed with a variable network topology without the need for a large computational effort. The network sensitivities and dynamic range are accounted for during the optimization process.

The possibility of design improvement by using the newly obtained networks is demonstrated in all the appropriate chapters by means of detailed examples. In order to test the validity of the theory presented, various SC filters were designed and tested in laboratory. Due to the lack of proper MOS fabrication facilities, the filters were implemented using discrete components.

Chapter V summarizes the various theoretical and experimental results presented in this thesis. The chapter concludes with suggestions for further research work.

CHAPTER II

SINGLE OA SC NETWORKS

2.1 INTRODUCTION

This chapter deals with the generation, classification and design of single OA SC networks. Most of the SC network implementations make use of certain basic building blocks or cells. These are combined in many different ways to generate a final structure that satisfies the prescribed specifications. Literature survey reveals that single OA building blocks are the most used of these basic cells. They are widely employed in filtering as well as in nonfiltering applications. In SC filters these cells have been extensively used in the realization of first as well as second order and even higher order filters [3,7,15,21,27]. In nonfiltering applications they have been exploited to perform a wide variety of functions such as in A/D and D/A conversions [1,2,21,28,29], sample-and-hold circuits [23,29,30], amplifiers [21,22], unit delays [21,31], modulators [21,32], analog multipliers [23,33], oscillators [34] and amplitude detectors [35].

It thus appears desirable to have a systematic and efficient method to generate single OA SC networks. It is also of interest to generate them in such a fashion that they are suitable for given applications starting from the desired input/output relationships.

A new approach is presented here which exploits the stray insensitivity conditions discussed in Chapter I in the generation of SC networks. The proposed procedure is systematic and comprehensive. It is based on the determination of the most general switching scheme which will guarantee the stray insensitivity of the final network. Then, only those capacitors that contribute to the transfer function are employed along with the derived switching scheme. This automatically leads to the minimum size of the most general parasitic insensitive SC structure for a given number of operational amplifiers (OAs). Although the proposed network generation method can be applied to systems of any order, this chapter deals exclusively with single OA networks [36,37]. In Chapter III the method is extended for the generation of SC biquads. After the generation procedure, a comprehensive study on the reduction of the general network to a practical (and most of the times canonical) structure is presented.

Towards this end, the most general switching matrix for a single OA SC network satisfying the stray insensitivity conditions is first determined. Then the existing networks are separated in two distinct classes. For each of these classes the most general switching scheme is established and the appropriate capacitor locations are discussed. This study leads to the general single OA SC networks for the two classes. Then, for both classes the

investigation proceeds in the following steps:

step 1: Analysis of the general network and the determination of the general output equations.

step 2: Determination of all transfer functions realizable by the general network, along with the sets of necessary conditions for their realizability. In this study different types of input signal waveforms are considered.

step 3: Determination of additional sets of restrictions which should be imposed on the general structures if sampled and held output or a delay from input to output are required.

step 4: Study of the possible ways to realize the transfer functions determined in step 2 without the requirement of any matching conditions for the network elements. The concluding results are tabulated.

Finally, a comprehensive section on how to apply the results obtained in this chapter to generate practical structures is presented. Some techniques to improve the final design are also discussed. A detailed example of an all-pass filter design is given in order to illustrate the usefulness of the proposed method. The resulting circuits are compared with previously reported realizations. A second example on the generation of biquad building blocks

is also presented.

2.2 GENERAL SWITCHING MATRIX

We now apply the parasitic insensitivity conditions discussed in Chapter I to a general network using one OA. It can be easily verified by inspection that, in order to satisfy Condition 1 without compromising the circuit stability, the general network must assume, during each of the phases, a topology of the type shown in Fig. 2.1 where the white blocks represent either capacitors or open circuits and the shaded feedback block may represent a capacitor, an open circuit or a short circuit. The possibility of a voltage follower from input to output is not considered (even though a buffer alone would be stray insensitive) for the reasons explained below. Two options are possible here:

(1) The even and odd circuits are equal (voltage follower). This is a trivial case.

(2) The network assumes the buffer configuration during one phase, say even, and a topology derived from Fig. 2.1 during the next phase (odd). Hence, for the odd phase the noninverting input of the OA must be disconnected from the input signal (where it was connected in the buffer configuration) and switched to ground. Therefore, the inverting input of the OA is connected to a V-node (output of the OA) in one phase (even) and becomes an I-node in the next phase (odd). This situation clearly violates Condition

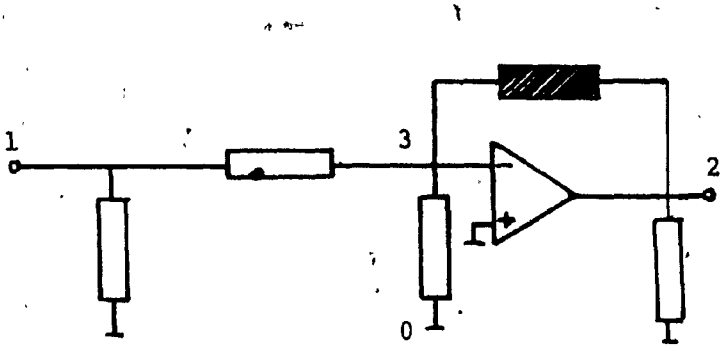


Figure 2.1: Topology assumed by single OA networks during each clock phase.

2 for stray insensitivity unless the output is made zero during both phases. This, of course, is not a useful case.

Consequently, in what follows, the set of networks which assume, for each of the phases, the topology shown in Fig. 2.1 is studied. Such networks have some topological properties which will be used in the derivations that follow. In these networks the noninverting OA input terminal is always grounded and the inverting one is an I-node for both phases. Also, since I-nodes must be OA input terminals and V-nodes must be either input voltage sources or OA output terminals, both the even and odd circuits will have always the same four nodes (and only them), namely, the input node, the output and inverting input terminals of the OA and the ground node. All other nodes must be connected to one of these in each phase such that Condition 1 for parasitic insensitivity is satisfied. In the remainder of this chapter, the following node numbering scheme is always used:

node 0: ground node.
node 1: input voltage source.
node 2: output of the OA.
node 3: virtual ground of the OA.

The remaining network nodes are numbered from 4 to n.

To represent the network switching scheme, the switching matrices S_e (even phase) and S_o (odd phase)

defined in [12] and briefly discussed in Chapter I are used.

Using this definition and the proposed node numbering scheme, the matrices S_e and S_o assume the form

$$S_{e,o} = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ \vdots \\ n \end{array} \begin{array}{c} \begin{array}{cccccc} 1 & 2 & 3 & 4 & \cdots & n \end{array} \\ \left[\begin{array}{cccc:ccc} 1 & 0 & 0 & S_{14}^{e,o} & \cdots & S_{1n}^{e,o} \\ 0 & 1 & S_{23}^{e,o} & S_{24}^{e,o} & \cdots & S_{2n}^{e,o} \\ 0 & 0 & S_{33}^{e,o} & S_{34}^{e,o} & \cdots & S_{3n}^{e,o} \\ \hdashline & & & & & \\ & 0 & & & 0 & \\ & & & & & \end{array}\right] \end{array}$$

where 0 is the matrix whose entries are all zero. If a node is grounded during a given phase, all the entries in the corresponding column will be zero. Here it is assumed that a connection between the input node (independent voltage source) and the output or the virtual ground of the OA cannot be made. Also, it should be clear that only one of the entries S_{23} and S_{33} corresponding to a given phase can be equal to 1. More specifically, two cases may happen:

(1) Nodes 2 and 3 are never connected together. In this case $S_{33}=1$ and $S_{23}=0$ for both S_e and S_o.

(2) Nodes 2 and 3 are connected through a switch during

one of the phases (say the even phase). In this case $S^e_{23}=1$, $S^e_{33}=0$, and because the connection cannot be permanent (voltage follower cases), $S^o_{33}=1$ and $S^o_{23}=0$.

In order to facilitate subsequent derivations, the complete set of networks will, from now on, be classified into two distinct classes, namely:

Class I- Networks included in case 1 above.

Class II- Networks included in case 2 above.

Obviously, these two classes are mutually exclusive. Class I, which includes most of the useful structures, will be studied first.

2.3 GENERAL SINGLE OA NETWORK (CLASS I)

Considering the form of the switching matrices S_e and S_o as well as the conditions to be satisfied by the networks in this class ($S^{e,o}_{33}=1$ and $S^{e,o}_{23}=0$), the first three rows of both S_e and S_o can be combined in a single switching matrix S_I (6xn) which contains all the informations about the switching scheme of a biphase network belonging to Class I. The matrix S_I will have the following form:

$$
S_I = \begin{array}{c} \\ 1^e \\ 2^e \\ 3^e \\ 1^o \\ 2^o \\ 3^o \end{array}
\begin{array}{c}
\begin{array}{cccccccc} 1 & 2 & 3 & 4 & \cdots & k & \cdots & n \end{array} \\
\left[\begin{array}{cccccccc}
 & & & s^e_{14} & \cdots & s^e_{1k} & \cdots & s^e_{1n} \\
 & I & & s^e_{24} & \cdots & s^e_{2k} & \cdots & s^e_{2n} \\
 & & & s^e_{34} & \cdots & s^e_{3k} & \cdots & s^e_{3n} \\
\hline
 & & & s^o_{14} & \cdots & s^o_{1k} & \cdots & s^o_{1n} \\
 & I & & s^o_{24} & \cdots & s^o_{2k} & \cdots & s^o_{2n} \\
 & & & s^o_{34} & \cdots & s^o_{3k} & \cdots & s^o_{3n}
\end{array}\right]
\end{array}
$$

where I stands for the (3x3) identity matrix.

It is interesting to note that there is a one-to-one correspondence between a given matrix S_I and the network switching scheme associated with it. Each column of S_I ($j>3$) determines how a given node is connected to the four basic ones in both the even and the odd phases. Therefore, the study of all possible patterns for a typical column (say kth column) will determine the ways in which an internal node k can be connected during each one of the two phases. Also, by considering some theoretical and practical restrictions which can be imposed on the switching scheme

without any loss of generality, many redundancies and impractical cases can be avoided. These restrictions are the following:

(1) Each node can be connected to at most one of the V, I and ground nodes during each phase. Otherwise, two voltage sources or a voltage source and a zero-valued-voltage node will be connected in parallel during a phase. Consequently, only one nonzero element may appear in each portion (even and odd) of a column of S_I.

(2) Each node must be connected to at least one of the V-nodes or I-nodes during at least one phase. Otherwise, this node will remain either permanently disconnected or permanently grounded. This eliminates the possibility of a column of zeros in S_I.

(3) No node can be connnected to another node in both phases. In such a case, the nodes would be coincident. Hence, the even and the odd portions of a column of S_I can never be equal.

(4) Two nodes with exactly the same switching scheme for both phases are not allowed. It would characterize a redundancy. This eliminates the possibility of two identical columns in S_I.

Note also that for this class of networks, Condition 2 for parasitic insensitivity requires that $s_{ik}^{e,o} x s_{jk}^{o,e} = 0$ for $i=1,2$ and $j=3$ because none of the voltage sources V_1 or V_2 is set to zero in any one of the clock

phases (no switch across the OA and V_1 is an independent source).

The application of these restrictions to a typical column of the switching matrix S_I leads to the 8 distinct switching patterns shown in Fig. 2.2. Due to restriction 4 above, we can state that any SC network belonging to Class I will have at most 11 nodes, excepting the ground node. In Fig. 2.2 each possible pattern has been assigned a number from 4 to 11 that refers to a specific node in the general SC network for Class I. Fig. 2.3 shows the most general switching scheme for the networks of this class with its 11 nodes numbered according to the table in Fig. 2.2. In Fig. 2.3, capacitors can be connected between any pair of nodes without affecting the parasitic insensitivity of the network. Once, however, the switching scheme is fixed, the capacitor placements will determine the contributions of each voltage source to the network CCEs.

In principle, a capacitor can be placed between any two of the 12 nodes (including the ground node). However, depending on its location, it does or does not affect the network behaviour. The CCEs (in terms of the node voltages) written for the even and odd circuits at node 3 will completely determine all voltage transfer functions for any network in this class, for this is the only node for which the CCEs form a linearly independent set. It can be easily verified by inspection that in the following cases these

		4	5	6	7	8	9	10	11
even	(1,k)	1	0	0	0	0	0	0	1
	(2,k)	0	1	0	0	0	0	1	0
	(3,k)	0	0	1	0	0	0	0	0
odd	(1,k)	0	0	0	1	0	0	1	0
	(2,k)	0	0	0	0	1	0	0	1
	(3,k)	0	0	0	0	0	1	0	0

Figure 2.2: Possible switching patterns (Class I).

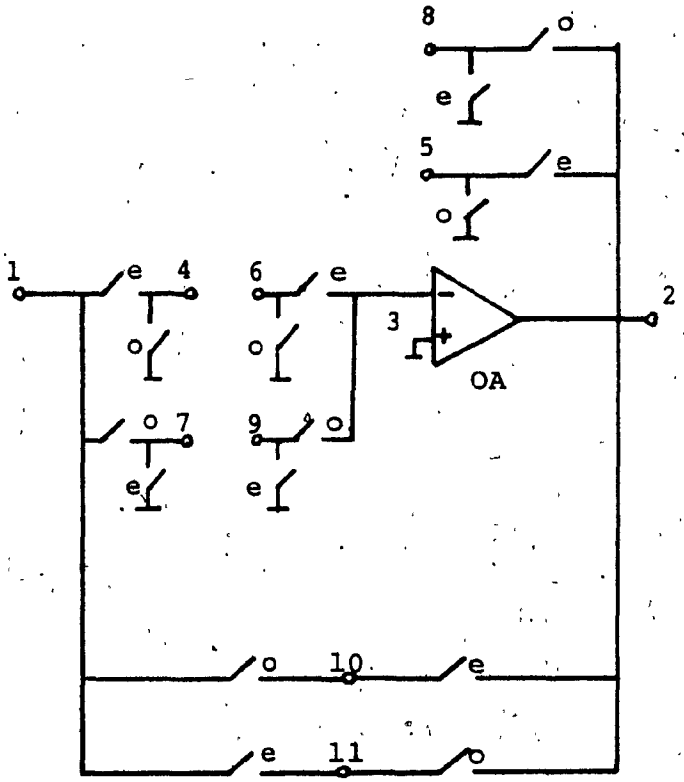


Figure 2.3: General switching scheme (Class I).

CCEs will not depend on the corresponding capacitors:

(a) A capacitor permanently connected from any node to ground.

(b) A capacitor placed between two nodes which are connected to V-nodes in both phases.

(c) A capacitor placed between two nodes which are connected to zero-valued-voltage nodes (I-node or ground) in both phases.

The remainder are capacitors linking a node which is switched at least once to a V-node, to another node which is switched at least once to an I-node. All these cases are shown in Fig. 2.4 where an asterisk at position (i,j) characterizes a possible capacitive connection from node i to node j. Consequently, a maximum of 24 capacitors will be necessary to realize any possible transfer function realizable by a network in Class I. The most general network for this class is shown in Fig. 2.5. It should be observed that the number of switches in this figure is excessively large. This is because each node switching scheme of Fig. 2.3 is repeated several times in Fig. 2.5. This is done in order to allow the effect of each one of the 24 capacitors in the final transfer function to be easily determined. Actually, in any implementation no more than 16 switches (Fig. 2.3) are necessary since each node switching scheme is used only once and all capacitor terminals connected to the same type of node are placed together.

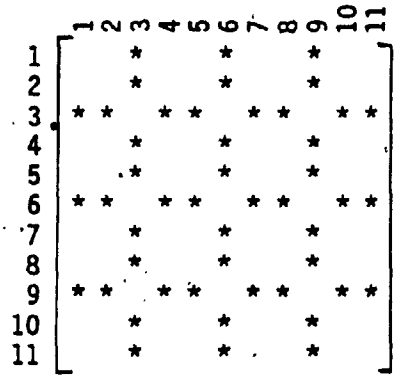


Figure 2.4: Useful capacitor locations (Class I).

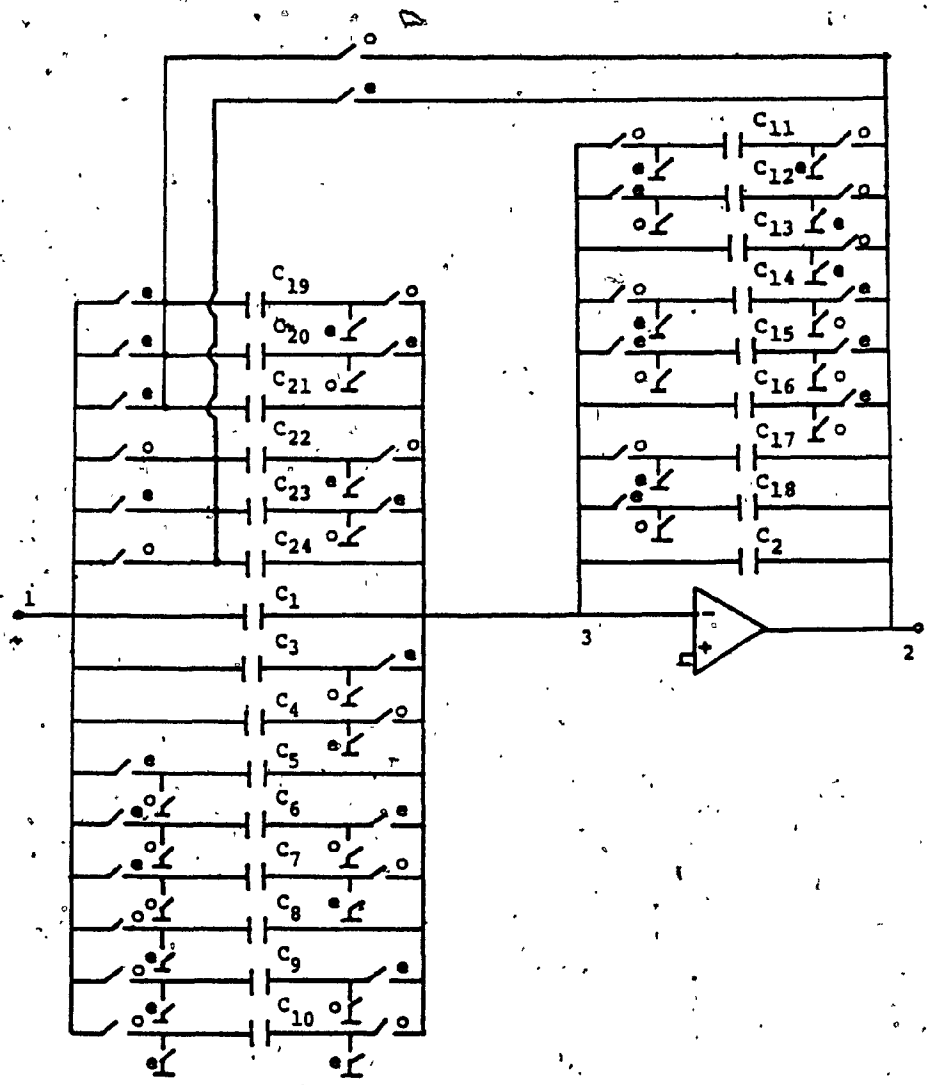


Figure 2.5: General network (Class I).

This point will be more clearly illustrated by an example later on.

The analysis of the general block in Fig. 2,5, assuming ideal elements, leads to the following CCEs:

Even phase:

$$\alpha_5 V_2^e = -\alpha_1 V_1^e + z^{-1/2}\alpha_3 V_1^o + z^{-1/2}\alpha_7 V_2^o \qquad (2.1)$$

Odd phase:

$$\alpha_6 V_2^o = -\alpha_2 V_1^o + z^{-1/2}\alpha_4 V_1^e + z^{-1/2}\alpha_8 V_2^e \qquad (2.2)$$

where $z=\exp(j\omega T)$, T being the sampling period and

$$\alpha_1 = C_1 + C_3 + C_5 + C_6 + C_{20} + C_{21} \qquad (2.3a)$$

$$\alpha_2 = C_1 + C_4 + C_8 + C_{10} + C_{22} + C_{24} \qquad (2.3b)$$

$$\alpha_3 = C_1 + C_3 + C_8 + C_9 + C_{23} + C_{24} \qquad (2.3c)$$

$$\alpha_4 = C_1 + C_4 + C_5 + C_7 + C_{19} + C_{21} \qquad (2.3d)$$

$$\alpha_5 = C_2 + C_{15} + C_{16} + C_{18} + C_{23} + C_{24} \qquad (2.3e)$$

$$\alpha_6 = C_2 + C_{11} + C_{13} + C_{17} + C_{19} + C_{21} \qquad (2.3f)$$

$$\alpha_7 = C_2 + C_{12} + C_{13} + C_{18} + C_{20} + C_{21} \qquad (2.3g)$$

$$\alpha_8 = C_2 + C_{14} + C_{16} + C_{17} + C_{22} + C_{24} \qquad (2.3h)$$

At this stage some remarks about the values of α_i, i=1,...,8 are in order:

(a) The values of α_i, i=1,...,8 are always greater or equal to zero.

(b) In order to guarantee the stability of the network,

a negative feedback path must exist across the OA during both the phases. Looking at equations (2.1) and (2.2) this fact can be translated into the necessity for the presence of α_5 in (2.1) and α_6 in (2.2). The existence of nonzero α_5 and α_6 guarantees that some charge is flowing from the output node to the virtual ground of the OA during each phase since these are the frequency independent coefficients of V_2^e and V_2^o for the even and odd CCEs at node 3, respectively. Therefore, in what follows α_5 and α_6 are not allowed to be zero. This is, most of the times, accomplished by the use of capacitor C_2. Whenever possible, the presence of C_2 is advisable for stability reasons, due to the non-overlapping nature of the clock signal [4,7,38].

Solving the CCEs (2.1) and (2.2) for V_2^e and V_2^o as functions of the input signal yields

$$V_2^e = -\frac{\alpha_1\alpha_6 - z^{-1}\alpha_4\alpha_7}{\alpha_5\alpha_6 - z^{-1}\alpha_7\alpha_8} V_1^e + \frac{z^{-1/2}(\alpha_3\alpha_6 - \alpha_2\alpha_7)}{\alpha_5\alpha_6 - z^{-1}\alpha_7\alpha_8} V_1^o \qquad (2.4)$$

and

$$V_2^o = -\frac{\alpha_2\alpha_5 - z^{-1}\alpha_3\alpha_8}{\alpha_5\alpha_6 - z^{-1}\alpha_7\alpha_8} V_1^o + \frac{z^{-1/2}(\alpha_4\alpha_5 - \alpha_1\alpha_8)}{\alpha_5\alpha_6 - z^{-1}\alpha_7\alpha_8} V_1^e \qquad (2.5)$$

Considering the four possible transfer functions of a biphase SC network, equations (2.4) and (2.5) can be rewritten as

$$V_2^e(z)=H^{ee}(z)V_1^e(z)+H^{oe}(z)V_1^o(z) \tag{2.6}$$

$$V_2^o(z)=H^{oo}(z)V_1^o(z)+H^{eo}(z)V_1^e(z) \tag{2.7}$$

where

$$H^{ee}(z) = -\frac{\alpha_1\alpha_6-z^{-1}\alpha_4\alpha_7}{\alpha_5\alpha_6-z^{-1}\alpha_7\alpha_8} \tag{2.8a}$$

$$H^{oe}(z) = \frac{z^{-1/2}(\alpha_3\alpha_6-\alpha_2\alpha_7)}{\alpha_5\alpha_6-z^{-1}\alpha_7\alpha_8} \tag{2.8b}$$

$$H^{eo}(z) = \frac{z^{-1/2}(\alpha_4\alpha_5-\alpha_1\alpha_8)}{\alpha_5\alpha_6-z^{-1}\alpha_7\alpha_8} \tag{2.8c}$$

$$H^{oo}(z) = -\frac{\alpha_2\alpha_5-z^{-1}\alpha_3\alpha_8}{\alpha_5\alpha_6-z^{-1}\alpha_7\alpha_8} \tag{2.8d}$$

2.4 REALIZABLE TRANSFER FUNCTIONS (CLASS I)

In this section, all the voltage transfer functions realizable by a network of Class I as well as the necessary conditions for their realizability are determined as functions of the α_i's, i=1,...8, defined in the last section. The various possibilities of choosing the different α_i's in order to satisfy these realizability conditions are also determined. The possible ways of

practical implementation of the transfer functions are discussed in section 2.6.

From equations (2.4) and (2.5) one can easily verify that the general form of the obtainable transfer functions will be completely modified if the input signal is sampled and held for a full clock period (e.g., $V_1^o = z^{-1/2} V_1^e$). Hence, in what follows, this possibility will be treated as a special case. We start with the case of a general input signal waveform.

2.4.1 General Input

In this case, the input voltage $v_1(t)$ can be either a continuously time-varying signal (e.g., a sinewave) or a sampled-data signal with a staircase waveform whose amplitude is not kept constant for the entire sampling period (both phases). Consequently, for staircase input waveform the amplitudes of $v_1(t)$ for the even and odd phases will be considered independent of each other. As far as continuously time-varying input waveforms are concerned, it must be emphasized that, due to the discrete-time nature of the z-domain analysis employed, the transfer functions obtained will relate the input and output amplitudes only at the sampling instants $t=nT/2$. Also, in order to guarantee the accuracy of the results, these sampling instants should be considered to occur at the end of each phase. The capacitor voltages at these instants of time are the initial

conditions for the next phase. If, however, one is interested in determining z-domain transfer functions that describe the network behaviour between two sampling instants due to a continuously time varying input signal, the network analysis should be carried out using the Modified z-Transform [24] instead of the conventional z-Transform. In this work, the SC networks are treated as discrete-time networks and the conventional z-Transform is employed. Consequently, we are interested in the network voltages at the sampling instants and the equations (2.4) and (2.5) are valid for any type of input signal.

The detailed study of equations (2.6), (2.7) and (2.8) leads to all realizable voltage transfer functions. The final results are presented in Table 2.1 using the four basic transfer functions (eqs. 2.8). The four transfer functions in Table 2.1 are the only possible ways to relate the input and output voltages in the different phases. Here, whenever the input signal is sampled only once per period, the sampling is assumed, without any loss of generality, to be done during the even phase. The output, however, is always considered for both phases, according to equations (2.6) and (2.7). By doing so, all possible transfer functions can be obtained. The entries in column 2 are obtained by determining the necessary conditions to eliminate the terms in (2.6) and (2.7) which are not part of the desired transfer function. Column 3 lists all the

Table 2.1: Realizable transfer functions (general input).

Transfer Function	Necessary Conditions	Different Possibilities
1.1 $\frac{V_2^e}{V_1^e} = H^{ee}$	$H^{oe} \equiv 0$ $\alpha_3\alpha_6 - \alpha_2\alpha_7 = 0$	1.1.1- $\alpha_2 = \alpha_3 = 0$ 1.1.2- $\alpha_3 = \alpha_7 = 0$ 1.1.3- $\alpha_2 \neq 0, \alpha_3 \neq 0, \alpha_7 \neq 0$ $\alpha_3\alpha_6 = \alpha_2\alpha_7$
1.2 $\frac{V_2^o}{V_1^e} = H^{eo}$	$H^{oo} \equiv 0$ $\alpha_2\alpha_5 - z^{-1}\alpha_3\alpha_8 = 0$	1.2.1- $\alpha_2 = \alpha_3 = 0$ 1.2.2- $\alpha_2 = \alpha_8 = 0$
1.3 $\frac{V_2}{V_1^e} = H^{ee} + H^{eo}$	$H^{oe} = H^{oo} \equiv 0$ $\alpha_3\alpha_6 - \alpha_2\alpha_7 = 0$ $\alpha_2\alpha_5 = 0$ $\alpha_3\alpha_8 = 0$	$\alpha_2 = \alpha_3 = 0$
1.4 $\frac{V_2}{V_1} = H^{ee} + H^{eo}$	$H^{ee} = H^{oo}$ $H^{eo} = H^{oe}$ $\alpha_1\alpha_6 = \alpha_2\alpha_5$ $\alpha_4\alpha_7 = \alpha_3\alpha_8$ $\alpha_3\alpha_6 - \alpha_2\alpha_7 = \alpha_4\alpha_5 - \alpha_1\alpha_8$	———

possible ways to achieve such eliminations. The complete study is extensive but straightforward. Consequently, it is not presented here in detail.

The transfer functions V_2^e/V_1 and V_2^o/V_1 are not obtainable since for their realization it is required that $H^{ee}=H^{oe}$ and $H^{eo}=H^{oo}$, leading to identically zero numerators (see eqs. 2.6 to 2.8).

2.4.2 Sampled and Held Input

We now study the case where $v_1(t)$ is a sampled-data signal with a staircase waveform, and with the special feature of being kept constant over the entire sampling period.

Again without loss of any generality, it can be assumed that the input signal changes its amplitude only in the even phase. Hence, the sample and hold condition can be expressed, in the z-domain, by the equality

$$V_1^o = z^{-1/2}V_1^e \tag{2.9}$$

Substituting (2.9) into (2.6) and (2.7), the following new set of network equations can be obtained:

$$V_2^e = (H^{ee} + z^{-1/2}H^{oe})V_1^e \tag{2.10a}$$

$$V_2^o = (H^{eo} + z^{-1/2}H^{oo})V_1^e \tag{2.10b}$$

This system of equations leads to the voltage transfer functions shown in Table 2.2. The transfer functions V_2^e/V_1, V_2^o/V_1 and V_2^{ℓ}/V_1 do not apply in this case since V_1^e and V_1^o are no longer independent.

It is interesting to observe that the condition of sampled and held input not only leads to transfer functions not realizable otherwise (check the signs of the numerator coefficients) but also eliminates the need for any extra realizability conditions, allowing a greater design flexibility.

2.5 SPECIAL RESTRICTIONS

The two cases (Tables 2.1 and 2.2) discussed in the last section account for all possibly realizable z-domain transfer functions using a network from Class I. Nevertheless, sometimes it may be necessary to impose further restrictions on the network behaviour due to external conditions. The two most commonly imposed restrictions are the avoidance of a continuous path from the input to the output (specially if the input signal does not have a staircase waveform) and/or the requirement for an output sampled and held over a full clock period. These conditions are sometimes necessary (or convenient) to allow the interconnection of distinct blocks in a large system (e.g., a high order filter). They can also be applied in order to avoid the need for sample and hold circuits at the

Table 2.2: Realizable transfer functions ($V_1^o = z^{-1/2} V_1^e$).

Transfer Function	necessary conditions
2.1 $\frac{V_2^e}{V_1^e} = H^{ee} + z^{-1/2} H^{oe}$	NONE
2.2 $\frac{V_2^o}{V_1^e} = H^{eo} + z^{-1/2} H^{oo}$	NONE
2.3 $\frac{V_2}{V_1^e} = \frac{V_2^e + V_2^o}{V_1^e} =$ $= (H^{ee} + H^{eo}) + z^{-1/2}(H^{oe} + H^{oo})$	NONE

input and/or at the output of the system. Therefore, it is worthwhile to determine the necessary conditions to be imposed on the general network in order to guarantee each of these properties. Such study is the objective of this section.

2.5.1 No Continuous Path from Input to Output

Consider equations (2.4) and (2.5). In the time domain, these equations can be written, respectively, in the following forms:

$$\alpha_5\alpha_6 v_2(nT) = -\alpha_1\alpha_6 v_1(nT)+H_1 v_1(nT-T)+H_2 v_1(nT-T/2)+ H_3 v_2(nT-T) \quad (2.11)$$

and

$$\alpha_5\alpha_6 v_2(nT-T/2) = -\alpha_2\alpha_5 v_1(nT-T/2)+H_4 v_1(nT-3T/2)+ H_5 v_1(nT-T)+H_6 v_2(nT-3T/2) \quad (2.12)$$

where H_i, i=1,..,6 are time independent constants (functions of the various α_i's).

If a continuous path cannot exist from the input (v_1) to the output (v_2) during any phase, $v_2(nT)$ must be independent of $v_1(nT)$ in (2.11) and, likewise, $v_2(nT-T/2)$ should not be a function of $v_1(nT-T/2)$ in (2.12). Since α_5 and α_6 cannot be zero for stability reasons (see section 2.3), one can readily verify from equations (2.11) and (2.12) that the necessary conditions for a "broken" path

from input to output in both phases are given by

$$\alpha_1 = \alpha_2 = 0 \tag{2.13}$$

With these conditions satisfied, only delayed versions of the input signal can influence the output voltage at any time.

We now determine the necessary conditions for a fully held output. It is important to note that the following study is completely independent of the one in this subsection. Condition (2.13) and the ones to be derived next constitute independent sets.

The sampled and held output property can be accomplished (for biphase networks) in two different ways, namely, $V_2^e = z^{-1/2}V_2^o$ or $V_2^o = z^{-1/2}V_2^e$. These two options are investigated in what follows.

2.5.2 Sampled and Held Output ($V_2^e = z^{-1/2}V_2^o$)

Whenever some output condition is imposed, the two different cases of input voltage waveform discussed in section 2.4 should be considered separately since they lead to distinct z-domain equations. We first deal with the case of a general input signal.

General Input (V_1^e and V_1^o independent)

In order to guarantee $V_2^e = z^{-1/2}V_2^o$ we must have, from equations (2.6) and (2.7)

$$H^{ee}(z)V_1^e(z) + H^{oe}(z)V_1^o(z) = z^{-1/2}H^{oo}(z)V_1^o(z) + z^{-1/2}H^{eo}(z)V_1^e(z)$$

or, more specifically, from (2.8)

$$(-\alpha_1\alpha_6+z^{-1}\alpha_4\alpha_7)V_1^e(z)+z^{-1/2}(\alpha_3\alpha_6-\alpha_2\alpha_7)V_1^o(z) = z^{-1/2}(-\alpha_2\alpha_5+z^{-1}\alpha_3\alpha_8)V_1^o(z)+z^{-1}(\alpha_4\alpha_5-\alpha_1\alpha_8)V_1^e(z) \qquad (2.14)$$

Since this equation must hold for any frequency, the coefficients of equal powers of $z^{-1/2}$ must be equal for any values of V_1^e and V_1^o. Therefore, the following conditions must be satisfied:

$$\alpha_1 = 0$$
$$\alpha_4\alpha_5 = \alpha_4\alpha_7$$
$$\alpha_3\alpha_8 = 0$$
$$\alpha_2(\alpha_7-\alpha_5) = \alpha_3\alpha_6$$

The study of all possible ways of satisfying these equalities (for α_5 and α_6 not zero) yields the conditions shown in Table 2.3 (top left). We now consider the case of sampled and held inputs.

Table 2.3: Conditions for S/H output.

	$V_1^o \neq z^{-\frac{1}{2}} V_1^e$	$V_1^o = z^{-\frac{1}{2}} V_1^e$
$V_2^e = z^{-\frac{1}{2}} V_2^o$	(i) $\alpha_1 = \alpha_3 = 0$ $\alpha_5 = \alpha_7$ (ii) $\alpha_1 = \alpha_4 = \alpha_8 = 0$ $\alpha_3 \neq 0$ $\alpha_2(\alpha_7 - \alpha_5) = \alpha_3\alpha_6$	(i) $\alpha_1 = \alpha_3 = 0$ $\alpha_2 = \alpha_4$ (ii) $\alpha_1 = \alpha_3 = 0$ $\alpha_5 = \alpha_7$ (iii) $\alpha_1 = \alpha_8 = 0$ $\alpha_3 \neq 0$ $(\alpha_4 - \alpha_2)(\alpha_5 - \alpha_7) = \alpha_3\alpha_6$
$V_2^o = z^{-\frac{1}{2}} V_2^e$	(i) $\alpha_2 = \alpha_4 = 0$ $\alpha_6 = \alpha_8$ (ii) $\alpha_2 = \alpha_3 = \alpha_7 = 0$ $\alpha_4 \neq 0$ $\alpha_1(\alpha_8 - \alpha_6) = \alpha_4\alpha_5$	(i) $\alpha_2 = \alpha_4$ $\alpha_6 = \alpha_8$ (ii) $\alpha_2 \neq \alpha_4$ $\alpha_6 \neq \alpha_8$ $\alpha_1 \neq 0$ $\alpha_1\alpha_7 = \alpha_3\alpha_5$ $\alpha_1(\alpha_8 - \alpha_6) = \alpha_5(\alpha_4 - \alpha_2)$

Sampled and Held Input ($V_1^o = z^{-1/2}V_1^e$)

For this case, the set of equations (2.10) must be considered. From these equations, in order to guarantee $V_2^e = z^{-1/2}V_2^o$, we should have

$$H^{ee} + z^{-1/2}H^{oe} = z^{-1/2}H^{eo} + z^{-1}H^{oo}$$

or substituting here the expressions in (2.8)

$$-\alpha_1\alpha_6+z^{-1}(\alpha_4\alpha_7+\alpha_3\alpha_6-\alpha_2\alpha_7) =$$
$$z^{-1}(\alpha_4\alpha_5-\alpha_2\alpha_5-\alpha_1\alpha_8)+z^{-2}\alpha_3\alpha_8 \qquad (2.15)$$

Equating the coefficients of the same powers of $z^{-1/2}$ yields

$$\alpha_1 = 0$$
$$\alpha_3\alpha_8 = 0$$
$$(\alpha_4-\alpha_2)(\alpha_5-\alpha_7) = \alpha_3\alpha_6$$

The possible ways of satisfying these equalities are also presented in Table 2.3 (top right). Next, we consider the second possibility for a sampled and held output.

2.5.3 Sampled and Held Output ($V_2^o = z^{-1/2}V_2^e$)

Using the same procedure presented in the last subsection (for $V_2^e = z^{-1/2}V_2^o$), the sets of necessary conditions to guarantee $V_2^o = z^{-1/2}V_2^e$ for both types of input signal can be determined. The results of this investigation

are shown in Table 2.3 (bottom).

It should be noted at this point that any one of the conditions (i), (ii), etc. in each section of Table 2.3 will guarantee the desired results at the output. It is not necessary that all conditions be satisfied simultaneously.

2.6 NETWORK REALIZATIONS (CLASS I)

So far, we have determined all types of voltage transfer functions which can be realized by a network from Class I. Also, the necessary conditions for these realizations were determined as functions of the various α_i's. We now study the possible ways of satisfying these conditions such that the resulting networks can realize the desired transfer functions without the requirement of any matching condition (tracking) for the capacitors employed. For each set of necessary conditions, the realizable transfer functions (avoiding the necessity of capacitor tracking) as well as the network constraints are determined. The special cases of sampled and held output voltages and networks without a continuous path from input to output are also studied.

In order to save space, only one case will be studied in detail. The particular case to be presented here was chosen in order to illustrate the complete development. The remaining cases can be studied following the same procedure in a straightforward manner.

Let us consider the transfer function V_2^e/V_1^e for a general input signal (case 1.1 in Table 2.1). From the three possible ways to guarantee the realizability we choose, for instance, the first one, subcase (1.1.1) in Table 2.1. Therefore, the necessary conditions are given by

$$\alpha_2 = \alpha_3 = 0 \tag{2.16}$$

Since α_2 and α_3 are sums of nonegative entriest (capacitor values) the only solution for this equation, according to (2.3b) and (2.3c) is

$$C_1 = C_3 = C_4 = C_8 = C_9 = C_{10} = C_{22} = C_{23} = C_{24} = 0 \tag{2.17}$$

and the realizable transfer function H^{ee} will be

$$H^{ee} = \frac{V_2^e}{V_1^e} = -\frac{\alpha_4\alpha_6 - z^{-1}\alpha_4\alpha_7}{\alpha_5\alpha_6 - z^{-1}\alpha_7\alpha_8} \tag{2.18}$$

where the new values for the nonzero α_i's are given by

$$\alpha_1 = C_5 + C_6 + C_{20} + C_{21} \tag{2.19a}$$

$$\alpha_4 = C_5 + C_7 + C_{19} + C_{21} \tag{2.19b}$$

$$\alpha_5 = C_2 + C_{15} + C_{16} + C_{18} \tag{2.19c}$$

$$\alpha_6 = C_2 + C_{11} + C_{13} + C_{17} + C_{19} + C_{21} \tag{2.19d}$$

$$\alpha_7 = C_2 + C_{12} + C_{13} + C_{18} + C_{20} + C_{21} \tag{2.19e}$$

$$\alpha_8 = C_2 + C_{14} + C_{16} + C_{17} \tag{2.19f}$$

The general network has been reduced to 15 capacitors. Now, let us consider the other possible

restrictions which might be necessary in a given application:

(a) No Direct Path from Input to Output

If this condition is required, equation (2.13) must be satisfied, i.e., $\alpha_1 = \alpha_2 = 0$. The value of α_2 is already zero from (2.16). For $\alpha_1 = 0$, we add the constraints

$$C_5 = C_6 = C_{20} = C_{21} = 0 \tag{2.20}$$

As expected, the realizable transfer function is modified to

$$\frac{V_2^e}{V_1^e} = \frac{z^{-1}\alpha_4\alpha_7}{\alpha_5\alpha_6 - z^{-1}\alpha_7\alpha_8} \tag{2.21}$$

where the α_i's are modified to satisfy (2.20).

(b) Sampled and Held Output

Since the transfer function being realized is V_2^e/V_1^e (the output is sampled at the even phase) a sampled and held output is characterized by the condition $V_2^o(z) = z^{-1/2}V_2^e(z)$. Therefore, we now investigate the two possible ways to satisfy this condition, according to Table 2.3 (botton left).

(i) **First Option**

$$\alpha_2 = \alpha_4 = 0 \qquad (2.22)$$

and

$$\alpha_6 = \alpha_8 \qquad (2.23)$$

In order to satisfy (2.22) we should have (α_2 is already zero by eq.(2.16) from (2.19b)

$$C_5 = C_7 = C_{19} = C_{21} \qquad (2.24)$$

and for $\alpha_6 = \alpha_8$, expressions (19d), (19f) and (2.24) yield

$$C_2 + C_{11} + C_{13} + C_{17} = C_2 + C_{14} + C_{16} + C_{17} \qquad (2.25)$$

If this equality is to be guaranteed independently of matching conditions, we must have

$$C_{11} = C_{13} = C_{14} = C_{16} = 0 \qquad (2.26)$$

and the realizable transfer function is given by

$$\frac{V_2^e}{V_1^e} = \frac{-\alpha_1}{\alpha_5 - z^{-1}\alpha_7} \quad \text{for } \alpha_6 \neq 0 \qquad (2.27)$$

where

$$\alpha_1 = C_6 + C_{20}$$
$$\alpha_5 = C_2 + C_{15} + C_{18}$$
$$\alpha_6 = C_2 + C_{17}$$
$$\alpha_7 = C_2 + C_{12} + C_{18} + C_{20}$$
$$\alpha_8 = C_2 + C_{17}$$

The general network is then reduced to a circuit employing at most 6 capacitors.

(ii) Second option

$$\alpha_2 = \alpha_3 = \alpha_7 = 0 \tag{2.28}$$

and $$\alpha_1(\alpha_8-\alpha_6) = \alpha_4\alpha_5 \quad \text{for} \quad \alpha_4 \neq 0 \tag{2.29}$$

From (2.28) and (19c) we have

$$C_2 = C_{12} = C_{13} = C_{18} = C_{20} = C_{21} = 0 \tag{2.30}$$

and from (2.19), (2.29) and (2.30), after some simple algebraic manipulations, the following equation must hold

$$(C_5+C_6)(C_{14}-C_{11}-C_{19})+C_6C_{16}=(C_7+C_{19})(C_{15}+C_{16})+C_5C_{15} \tag{2.31}$$

In order to satisfy this equation without matching conditions, one of the following restrictions should be applied to the general network:

(a) $$C_5 = C_7 = C_{11} = C_{14} = C_{16} = C_{19} = 0 \tag{2.32}$$

or

(b) $$C_6 = C_7 = C_{11} = C_{14} = C_{15} = C_{19} = 0 \tag{2.33}$$

and, for any of these cases, the realizable transfer function is

$$\frac{V_2^e}{V_1^e} = -\frac{\alpha_1}{\alpha_5} \quad \text{for} \quad \alpha_6 = C_{17} \neq 0 \tag{2.34}$$

The network in this case employs at most 3 capacitors.

This concludes the investigation of this specific case. All the other possibilities were studied following the same procedure and the results are presented in Table 2.4. In this table, the sets of capacitors which are made zero in order to realize a transfer function or to satisfy a given restriction were initially determined by the necessary conditions obtained previously. Then, those capacitors which would not affect, regardless of their values, the stability of the network or any of the transfer function coefficients were deleted. By doing so, the general structure for a specific case will not include unnecessary elements.

For an effective use of Table 2.4, some observations are in order, namely:

(a) The transfer function V_2/V_1^e is implicitly included in Table 2.4. Since

$$\frac{V_2}{V_1^e} = \frac{V_2^e}{V_1^e} + \frac{V_2^o}{V_1^e} \tag{2.35}$$

the referred transfer function can be readily obtained by adding the other two. The necessary conditions are then derived as the union of the sets available for V_2^e/V_1^e and V_2^o/V_1^e.

(b) The transfer V_2/V_1 is not included in Table 2.4 since the only network that can be obtained is an unswitched

Table 2.4: Transfer functions (Class I).

Transfer Function			necessary conditions $C_1=0$	$V_2^e=z^{-\frac{1}{2}}V_2^o$ (*)	extra conditions $C_1=0$	$V_2^o=z^{-\frac{1}{2}}V_2^e$ (*)	extra conditions $C_1=0$
$H_1(z)=\frac{-a_0+z^{-1}a_2}{b_0-z^{-1}b_2}=$ $\frac{-a_1a_6+z^{-1}a_4a_7}{a_5a_5-z^{-1}a_7a_8}$		$\frac{V_2^e}{V_1^e}$	1=1,3,4,8,9, 10,22,23,24	———	———	$\frac{-a_1}{a_5-z^{-1}a_7}$	1=5,7,11,13, 14,16,19,21.
						$\frac{-a_1}{a_5}$	1=2,6(5),7,11, 12,13,14,15 (16),18,19,20, 21.
		$\frac{V_2^e}{V_1^e}$	1=3,4,9,10,11, 12,17,18,19, 20,22,23.	———	———	———	———
$H_2(z)=$	$=\frac{(a_4a_5-a_1a_8)z^{-\frac{1}{2}}}{a_5a_6-z^{-1}a_7a_8}$	$\frac{V_2^o}{V_1^e}$	1=1,3,4,8,9, 10,22,23,24.	$\frac{a_4z^{-\frac{1}{2}}}{a_6-z^{-1}a_8}$	1=5,6,12,13, 15,16,20,21.	———	———
$=\frac{\pm a_1z^{-\frac{1}{2}}}{b_0-z^{-1}b_2}$	$=\frac{a_4}{a_6}z^{-\frac{1}{2}}$	$\frac{V_2^o}{V_1^e}$	1=1,2,3,4,6,8, 9,10,12,14,16, 17,20,22,24.	$\frac{a_4}{a_6}z^{-\frac{1}{2}}$	1=5,13,15,21, 23.	———	———
$H_3(z)=\frac{-a_0\pm z^{-1}a_2}{b_0-z^{-1}b_2}=$ $\frac{-a_1a_6+z^{-1}((a_4-a_2)a_7+a_3a_6)}{a_5a_6-z^{-1}a_7a_8}$ for $V_1^o=z^{-\frac{1}{2}}V_1^e$		$\frac{V_2^e}{V_1^e}$	———	———	———	$\frac{-a_1+z^{-1}a_3}{a_5-z^{-1}a_7}$	1=4,5,7,8,10, 11,13,14,16, 19,21,22,24.
						$\frac{-a_1}{a_5}$	1=(1-4),5(6), (7-14),16(15), (18-24).

Table 2.4: Continued.

Transfer Function		necessary conditions $C_i=0$	$V_2^e=z^{-\frac{1}{2}}V_2^o$ (*)	extra conditions $C_i=0$	$V_2^o=z^{-\frac{1}{2}}V_2^e$ (*)	extra conditions $C_i=0$
$H_4(z)=\dfrac{\pm a_1 z^{-\frac{1}{2}}+a_3 z^{-\frac{1}{2}}}{b_0-z^{-1}b_2}$	$\dfrac{V_2^o}{V_1^e}$	———	$\dfrac{(a_4-a_2)z^{-\frac{1}{2}}}{a_6-z^{-1}a_8}$	i=1,3,5,6,8,9, 12,13,15,16, 20,21,23,24.	———	———
$=\dfrac{((a_4-a_2)a_5-a_1a_8)z^{-\frac{1}{2}}+a_3a_8z^{-\frac{1}{2}}}{a_5a_6-z^{-1}a_7a_8}$			$z^{-\frac{1}{2}}$	$C_i\neq 0$ only for i=19,23.		
for $V_1^o=z^{-\frac{1}{2}}V_1^e$			$\dfrac{a_2}{a_6}z^{-\frac{1}{2}}$	$C_i\neq 0$ only for i=4,8,13,18		

(*) These conditions are meaningful only if V_1 has a staircase waveform or if $a_1=a_2=0$.

OBS: In order to avoid any continuous path from input to output, $a_1=a_2=0$ must hold, or equivalently, $C_i=0$ for i=1,3,4,5,6,8,10,20,21,22 and 24.

capacitive amplifier, which constitutes a trivial case.

(c) In order to determine a transfer function for which the input is sampled during the odd phase (V_2^e/V_1^o for instance) one has only to interchange the names of the even and odd phases. In terms of the various α_i's, i=1,...,8, this interchange can be accomplished by performing the following variable substitutions:

$$\alpha_1 \leftrightarrow \alpha_2$$
$$\alpha_3 \leftrightarrow \alpha_4$$
$$\alpha_5 \leftrightarrow \alpha_6$$
$$\alpha_7 \leftrightarrow \alpha_8$$

A simpler solution would be to realize the transfer function with the original clock phases interchanged (V_2^o/V_1^e in the above example) and, after the whole design is performed, exchange the names of the even and odd phases.

2.7 GENERAL SINGLE OA NETWORK (CLASS II)

In this section we study the class of networks which have a switch placed across the OA input and output terminals during one phase, say even. We start from the general form of the switching matrices discussed in section 2.2, considering this time the case 2. In this case (which characterizes the networks in Class II) the general form of the combined switching matrix S_{II} is:

$$
S_{II} = \begin{array}{c} \\ 1^e \\ 2^e \\ 3^e \\ \hline 1^o \\ 2^o \\ 3^o \end{array}
\begin{array}{c}
\begin{array}{ccc|ccccc} 1 & 2 & 3 & 4 & \cdots & k & \cdots & n \end{array} \\
\left[\begin{array}{ccc|ccccc}
1 & 0 & 0 & S^e_{14} & \cdots & S^e_{1k} & \cdots & S^e_{1n} \\
0 & 1 & 1 & S^e_{24} & \cdots & S^e_{2k} & \cdots & S^e_{2n} \\
0 & 0 & 0 & 0 & \cdots & 0 & \cdots & 0 \\ \hline
1 & 0 & 0 & S^o_{14} & \cdots & S^o_{1k} & \cdots & S^o_{1n} \\
0 & 1 & 0 & S^o_{24} & \cdots & S^o_{2k} & \cdots & S^o_{2n} \\
0 & 0 & 1 & S^o_{34} & \cdots & S^o_{3k} & \cdots & S^o_{3n}
\end{array}\right]
\end{array}
$$

Some particular properties of S_{II} should be emphasized, namely:

(1) $S^e_{22}=S^e_{23}=1$. This characterizes the connection (through a switch) between nodes 2 and 3 during the even phase. Note that this connection is not allowed for the odd phase since it would lead to the case of the voltage follower, already discussed in section 2.2.

(2) The choice of the even phase for the connection of nodes 2 and 3 was arbitrary and without any loss of generality, since for this class of networks, the sampling of the input and output voltages will be considered for both

phases.

(3) The third row of S_{II} is always zero. This happens because, during the even phase, node 3 belongs to a separate part including node 2 which is, of course, the lowest numbered node in that subgraph.

The next step is to investigate all possible patterns for a column of S_{II} corresponding to an internal node, say k. Like in the case of Class I, the redundancies and impractical cases can be avoided by the consideration of the four restrictions discussed in section 2.3. The study of all possibilities leads to the 8 distinct switching patterns shown in Fig. 2.6. In this figure, each pattern has been assigned a number which will correspond to a given node in the general network of Class II. It can be verified from Fig. 2.6 that the maximum number of nodes for a network in Class II will be 11. Nevertheless, in order to maintain an one-to-one correspondence with the node numbering of the general switching scheme for the networks in Class I, we have introduced the node number 12 to realize the 8th possible pattern. Comparing Fig. 2.2 and Fig. 2.6 one can readily verify that the node 6 (Class I) has been suppressed and the new possible switching scheme has been added as node 12. Such new node switching pattern is possible because, for this class of networks, $V_2^e=V_3^e=0$. Therefore, according to Condition 2 for parasitic insensitivity, a node can be switched to V_2 (V-node) in the even phase and then to V_3

even	(1,k)	1	0	0	0	0	0	1	0
	(2,k)	0	1	0	0	0	1	0	1
	(3,k)	0	0	0	0	0	0	0	0
odd	(1,k)	0	0	1	0	0	1	0	0
	(2,k)	0	0	0	1	0	0	1	0
	(3,k)	0	0	0	0	1	0	0	1
node		4	5	7	8	9	10	11	12

Figure 2.6: Possible switching patterns (Class II).

(I-node) in the odd phase.

Fig. 2.7 shows the most general switching scheme for the networks of Class II with its nodes numbered according to the table in Fig. 2.6.

The capacitor placements within this structure were investigated using the same procedure described in section 2.3 and the useful cases are shown in Fig. 2.8 where an asterisk at the position (i,j) means a possible capacitive connection between nodes i and j. It is interesting to observe that node 5 in Fig. 2.7 is completely useless. Any capacitor with a terminal connected to it will not affect any of the network CCEs. This fact should be expected since node 5 behaves exactly as the already eliminated node 6 (see Fig. 2.3) as the switch across the OA transforms node 2 into a virtual ground during the even phase. Fig. 2.9 shows the most general SC network of Class II. Here again the one-to-one correspondence with the capacitors of Fig. 2.5 was maintained for convenience. Therefore, even though the capacitors are numbered up to C_{31} in Fig. 2.9, only 21 capacitors are actually employed. The number of switches shown in this figure is not the minimum so that the contributions of each capacitor can be readily visualized. From Fig. 2.7 it can be verified that at most 15 switches are needed for such networks (node 5 is already disregarded).

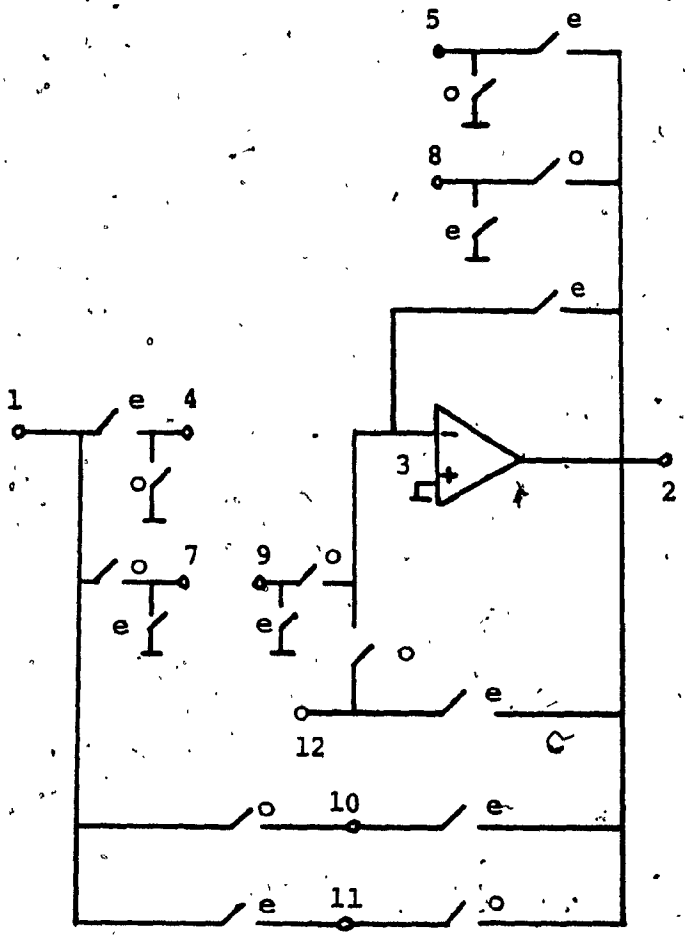


Figure 2.7: General switching scheme (Class II).

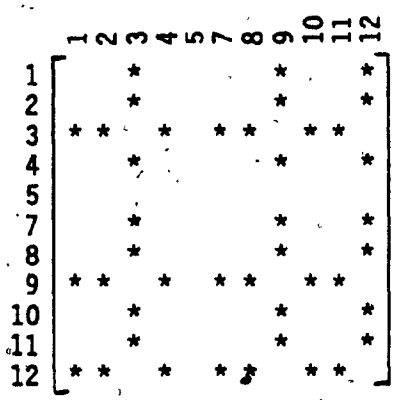


Figure 2.8: Useful capacitor locations (Class II).

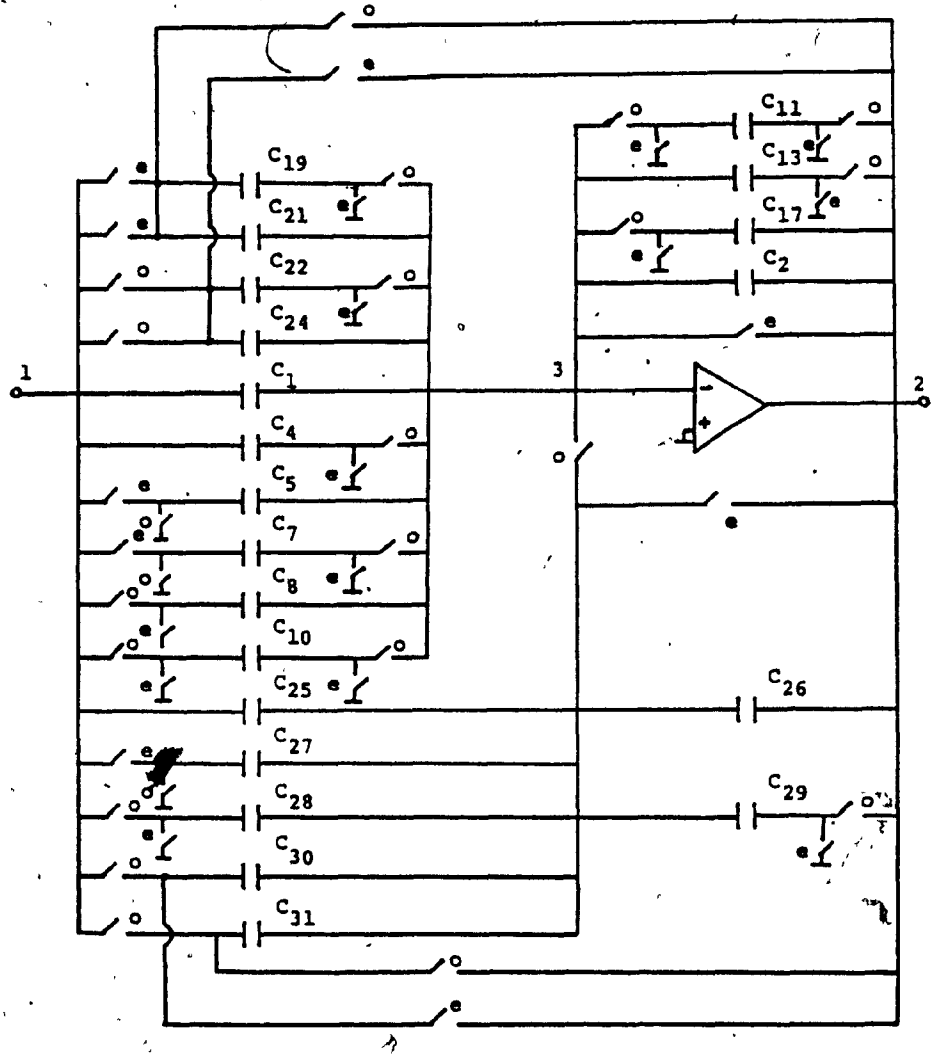


Figure 2.9: General network (Class II).

The analysis of the general network in Fig. 2.9 consists of the determination of the CCE at node 3 for the odd phase, with the previous knowledge that $V_2^e=0$. By doing so, the following charge equation is obtained:

$$V_2^o = -\frac{\hat{\alpha}_1}{\hat{\alpha}_3} V_1^o + z^{-1/2} \frac{\hat{\alpha}_2}{\hat{\alpha}_3} V_1^e \qquad (2.36)$$

where

$$\hat{\alpha}_1 = C_1+C_4+C_8+C_{10}+C_{22}+C_{24}+C_{25}+C_{28}+C_{30} \qquad (2.37a)$$

$$\hat{\alpha}_2 = C_1+C_4+C_5+C_7+C_{19}+C_{21}+C_{25}+C_{27}+C_{31} \qquad (2.37b)$$

$$\hat{\alpha}_3 = C_2+C_{11}+C_{13}+C_{17}+C_{19}+C_{21}+C_{29}+C_{31} \qquad (2.37c)$$

Since a continuous feedback path must always exist from the output to the input of the OA to guarantee network stability, the coefficient of $V_2^o(z)$ in (2.36), namely $\hat{\alpha}_3$, can never be equal to zero if the network is not embedded in a larger negative feedback loop.

A very interesting property can be visualized if the terms in (2.36) are grouped in a particular way. Let us write (2.36) as

$$(C_8+C_{10}+C_{22}+C_{24}+C_{28}+C_{30})V_1^o + (C_2+C_{11}+C_{13}+C_{17}+C_{26}+C_{29})V_2^o + (C_1+C_4+C_{25})(V_1^o-z^{-1/2}V_1^e) + (C_{19}+C_{21}+C_{31})(V_2^o-z^{-1/2}V_1^e) - (C_5+C_7+C_{27})z^{-1/2}V_1^e=0 \qquad (2.38)$$

With the CCE written in this form, the contributions of each

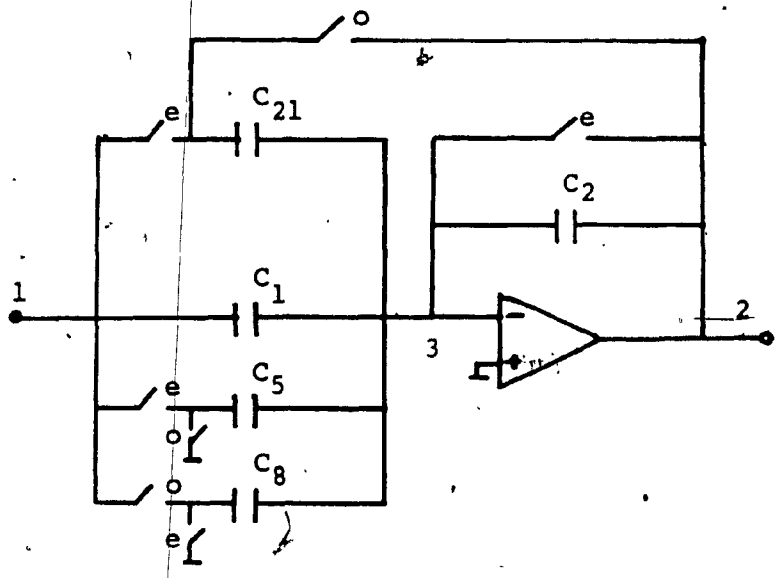
capacitor as functions of the voltage sources are clearly shown. Note that each capacitor appears only once in (2.38). Consider now the following capacitor sets:

set 1: C_8, C_{10}, C_{22}, C_{24}, C_{28}, C_{30}
set 2: C_2, C_{11}, C_{13}, C_{17}, C_{26}, C_{29}
set 3: C_1, C_4, C_{25}
set 4: C_{19}, C_{21}, C_{31}
set 5: C_5, C_7, C_{27}

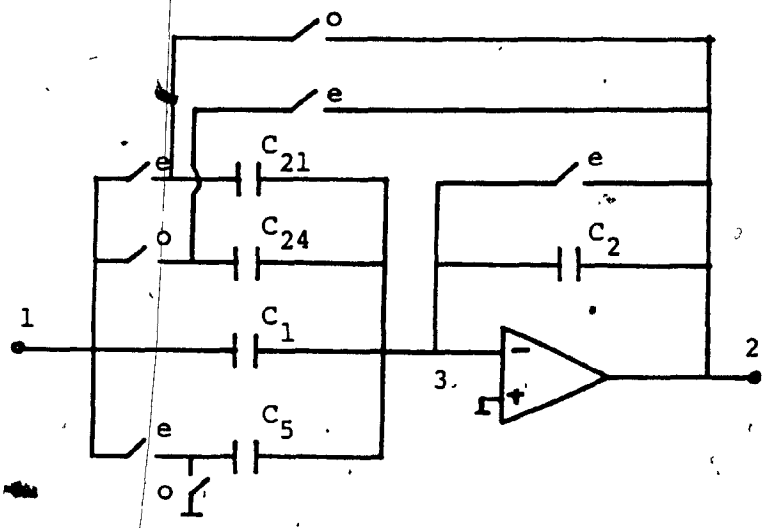
Each of these sets is composed of exactly the capacitances which are within each of the five parenthesis in (2.38). Furthermore, the sets are mutually exclusive. Consequently, only one capacitor from each set is necessary to realize any possible transfer function, since all capacitors within the same set perform exactly the same function in the network. The choice of which capacitor will be used from each set is irrelevant in terms of the realizable transfer functions and therefore a reasonable approach is to to choose the one(s) which would employ less switches to perform a given function. By doing so, the 5 sets are reduced to

set 1: C_8 or C_{24}
set 2: C_2
set 3: C_1
set 4: C_{21}
set 5: C_5

This choice leads to the 2 general building blocks shown in



(a)



(b)

Figure 2.10: Reduced general networks (Class II).

Fig. 2.10 for Class II. For the circuit in Fig. 2.10a ($C_{24}=0$)

$$V_2^o = - \frac{C_1+C_8}{C_2+C_{21}} V_1^o + z^{-1/2} \frac{C_1+C_5+C_{21}}{C_2+C_{21}} V_1^e \qquad (2.39)$$

and for Fig. 2.10b ($C_8=0$)

$$V_2^o = - \frac{C_1+C_{24}}{C_2+C_{21}} V_1^o + z^{-1/2} \frac{C_1+C_5+C_{21}}{C_2+C_{21}} V_1^e \qquad (2.40)$$

Therefore, at most 5 capacitors and 7 switches are required to implement any transfer function realizable by a network of Class II.

The study of sampled and held input signal can be performed as done for Class I. The study is quite simple and is omitted here. Sampled and held outputs, however, cannot be obtained from a network of this class since the output voltage is always made equal to zero during one of the phases. In order to avoid a continuous path from input to output, C_1, C_8 and C_{24} should be made zero in Fig. 2.10.

If the output is desired at the even phase, one can (as suggested in section 2.6) perform the design with the phases interchanged and, afterwards, substitute the even switches by odd switches and vice-versa in the final network.

2.8 DESIGN CONSIDERATIONS

A look at the values of α_i, i=1,...,8, reveals that each of these coefficients has a single capacitor which does not appear in any other α_i. The list of exclusive capacitors is as follows:

$$\begin{aligned} \alpha_1 &\rightarrow C_6 & \alpha_5 &\rightarrow C_{15} \\ \alpha_2 &\rightarrow C_{10} & \alpha_6 &\rightarrow C_{11} \\ \alpha_3 &\rightarrow C_9 & \alpha_7 &\rightarrow C_{12} \\ \alpha_4 &\rightarrow C_7 & \alpha_8 &\rightarrow C_{14} \end{aligned} \qquad (2.41)$$

Each of the remaining 16 capacitors are shared by 2 or more of the α coefficients. Therefore, if we consider each of the α_i's realized only by its exclusive capacitor, it is clear that any realizable transfer function can be obtained. Nevertheless, the price paid by this simplification will be, most of the times, the use of more capacitors than the minimum necessary, leading to an increase in the total capacitance and many times to an increase in the capacitance spread of the final network.

Consequently, it would be very useful to have a procedure that takes advantage of the extra 16 capacitors in obtaining better designs. We propose here a method to explore this possibility without increasing the complexity of the networks.

The idea is to use, at the begining, only the 8 basic elements plus unswitched capacitors to obtain the general transfer function for a given case, i.e., to substitute each α_i in Table 2.4 by the values of their exclusive capacitors plus C_1 or C_2 depending on the case. In this way, the expression of the general transfer function becomes much simpler to deal with and, as explained before, no generality is lost in the realizability of the various coefficients. From this simplified transfer function one can easily determine, by inspection, the possible ways to implement the final network employing a relatively small number of capacitors (in general 4 or 5). Then, we try to employ the remaining capacitors in order to improve the design. This can be accomplished in two basic ways:

(a) Reduction of the Number of Capacitors with the Same Spread and Less Total Capacitance

By studying the general expressions for the various α_i's in (2.3) one can easily verify that some sets of 2 or 4 of the basic capacitors, whenever equal in value, can be replaced by a single capacitor. All these substitutions are listed in Table 2.5. For instance, if in a given design, capacitors C_7 and C_{11} (case 6 in Table 2.5) are employed and their values happen to be equal (or can be forced to be), a single capacitor C_{19} of the same value could be used to substitute both C_7 and C_{11}. This procedure maintains the spread of the initial design and decreases the

Table 2.5: Capacitor equivalences.

	numerically equal capacitors	equivalent capacitor
1.	C_6, C_9	C_3
2.	C_6, C_7	C_5
3.	C_6, C_{12}	C_{20}
4.	C_6, C_7, C_{11}, C_{12}	C_{21}
5.	C_7, C_{10}	C_4
6.	C_7, C_{11}	C_{19}
7.	C_9, C_{10}	C_8
8.	C_9, C_{15}	C_{23}
9.	C_9, C_{10}, C_{14}, C_{15}	C_{24}
10.	C_{10}, C_{14}	C_{22}
11.	C_{11}, C_{12}	C_{13}
12.	C_{11}, C_{14}	C_{17}
13.	C_{12}, C_{15}	C_{18}
14.	C_{14}, C_{15}	C_{16}

total capacitance by the value of C_7.

(b) Reduction of the Total Capacitance with the Same Number of Capacitors

In this case, Table 2.5 is used in an alternative way. Let us take the same example with the difference that now C_7 and C_{11} are not equal in order to satisfy the design equations. Again from expressions (2.3) and Table 2.5 we see that, whatever function can be performed by C_7 and C_{11} may be likewise performed by C_7 and C_{19} or by C_{11} and C_{19}, as follows:

(i) If $C_7 > C_{11}$, use $C_{19} = C_{11}$ and $\hat{C}_7 = C_7 - C_{11}$ where C_7 is the value of the initial design and $\hat{C}_7$ is the new value to be employed in the network.

(ii) If $C_{11} > C_7$, use $C_{19} = C_7$ and $\hat{C}_{11} = C_{11} - C_7$.

It is clear that these substitutions reduce the total capacitance of the final network if $\hat{C}_7$ ($\hat{C}_{11}$) is greater than the smallest capacitance value of the original network. The component spread is increased only if the capacitance value generated by a difference becomes smaller than the least valued element of the initial design. Then the ratio of maximum to minimum capacitance values within the network is increased.

The use of these design techniques is better illustrated by means of examples.

2.9 EXAMPLES

Example 1

We take as an example a first order bilinearly transformed all pass filter used in [39] as a building block in a spectral line enhancer. The s-domain transfer function is given by

$$H(s) = \frac{\Omega - s}{\Omega + s} \tag{2.42}$$

which bilinearly transformed yields

$$H(z) = \frac{-(\frac{1-\Omega}{1+\Omega}) + z^{-1}}{1 - z^{-1}(\frac{1-\Omega}{1+\Omega})} \tag{2.43}$$

According to the specifications in [39], the transfer function H(z) is to be realized as

$$H(z) = \frac{V_2^o}{V_1^o} \quad \text{where} \quad V_1^o = z^{-1/2} V_1^e \tag{2.44}$$

In order to use Table 2.4 we rewrite (2.43) and (2.44) as

$$H(z) = \frac{V_2^o}{V_1^e} = \frac{-(\frac{1-\Omega}{1+\Omega})z^{-1/2}+z^{-3/2}}{1-z^{-1}(\frac{1-\Omega}{1+\Omega})}, \quad V_1^o = z^{-1/2}V_1^e \tag{2.45}$$

Now, according to Table 2.4, we want to realize

$$H_4(z) = \frac{[(\alpha_4-\alpha_2)\alpha_5-\alpha_1\alpha_8]z^{-1/2}+\alpha_3\alpha_8 z^{-3/2}}{\alpha_5\alpha_6-z^{-1}\alpha_7\alpha_8} \tag{2.46}$$

Considering the simplified forms of α_i, i=1,...,8 as

$$\alpha_1 = C_1+C_6 \qquad \alpha_5 = C_2+C_{15}$$
$$\alpha_2 = C_1+C_{10} \qquad \alpha_6 = C_2+C_{11}$$
$$\alpha_3 = C_1+C_9 \qquad \alpha_7 = C_2+C_{12}$$
$$\alpha_4 = C_1+C_7 \qquad \alpha_8 = C_2+C_{14}$$

and normalizing all capacitors with respect to C_2 yields

$$H_4(z) = \frac{[(C_7-C_{10})(1+C_{15})-(C_1+C_6)(1+C_{14})]z^{-1/2}+(C_1+C_9)(1+C_{14})z^{-3/2}}{(1+C_{11})(1+C_{15})-z^{-1}(1+C_{12})(1+C_{14})} \tag{2.47}$$

We now eliminate, arbitrarily, C_{12} and C_{14} since they only provide positive feedback. Also, from (2.47) we see that

C_{11} and C_{15} are not necessary at the same time in the same design. Equivalent reasoning eliminates the simultaneous use of C_1 and C_9.

Let us consider a first possibility where $C_9=C_{15}=0$. Then

$$H_4(z) = \frac{(C_7-C_1-C_6-C_{10})z^{-1/2}+C_1z^{-3/2}}{(1+C_{11})-z^{-1}} \qquad (2.48)$$

Comparing coefficients with (2.43) yields

$$C_{11} = \frac{2\Omega}{1-\Omega}$$

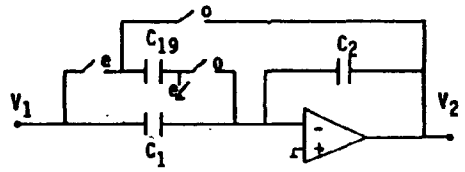
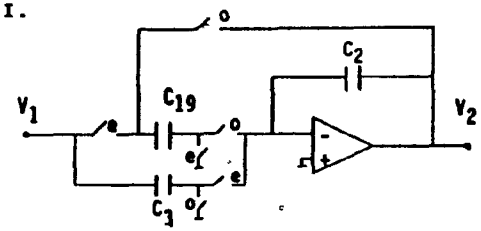
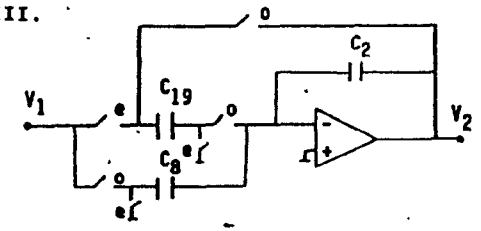
$$C_1 = \frac{1+\Omega}{1-\Omega}$$

$$C_7 = \frac{2\Omega}{1-\Omega}$$

and $$C_6 = C_{10} = 0$$

The network obtained is exactly the one proposed in [39]. We now apply the simplification procedures. Since $C_7=C_{11}$ in the final design, the improvement technique (a) can be employed. We use case 6 in Table 2.5 and substitute both capacitors by $C_{19}=2\Omega/(1-\Omega)$. The final network (which is canonic) is presented as network I in Table 2.6. Proceeding

Table 2.6: All-pass networks.

Networks	original capacitances	final capacitances
I. 	$C_1 = \frac{1+\Omega}{1-\Omega}$ $C_7 = C_{11} = \frac{2\Omega}{1-\Omega}$ $C_2 = 1$	$C_1 = \frac{1+\Omega}{1-\Omega}$ $C_{19} = \frac{2\Omega}{1-\Omega}$ $C_2 = 1$
II. 	$C_6 = C_9 = \frac{1+\Omega}{1-\Omega}$ $C_7 = C_{11} = \frac{2\Omega}{1-\Omega}$ $C_2 = 1$	$C_3 = \frac{1+\Omega}{1-\Omega}$ $C_{19} = \frac{2\Omega}{1-\Omega}$ $C_2 = 1$
III. 	$C_9 = C_{10} = \frac{1+\Omega}{1-\Omega}$ $C_7 = C_{11} = \frac{2\Omega}{1-\Omega}$ $C_2 = 1$	$C_8 = \frac{1+\Omega}{1-\Omega}$ $C_{19} = \frac{2\Omega}{1-\Omega}$ $C_2 = 1$

in the same way for the other possible choices of C_1, C_9, C_{11} and C_{15} the remaining canonic networks in Table 2.6 can be easily obtained.

The application of the improvement technique (b) is not shown here since it can be carried out in the same way and because the final results will depend on the numerical values of the transfer function coefficients.

At this point one can easily verify the advantages of using a systematic generation and design procedure. Three new distinct networks were derived from the application of the proposed method which realize the desired transfer function with the following advantages over the version reported earlier [39]:

(i) The capacitance spread is maintained.

(ii) The number of components is brought to a canonic count.

(iii) The total capacitance is reduced by $2\Omega/(1-\Omega)$.

(iv) No one of the three new designs requires capacitor tracking (equal values) in order to realize the desired transfer function.

(v) The three networks employ at most 6 switches, which is the number used in the original one. Furthermore, one of the new structures (I) employs only 4 switches.

Example 2

Another important application for the first order blocks is in the generation of second order networks. Suppose we are interested in the realization of a biquad for which both outputs are held for a full clock period ($V^o_{out}=z^{-1/2}V^e_{out}$). A flow graph capable of realizing a general second order denominator is shown in Fig. 2.11 where the input is considered to be sampled only during the even phase. The transfer functions of the two first order blocks are then determined, compared with the transfer functions in Table 2.4 and realized by following the generation and design procedure just described. Furthermore, from the general expression of the denominator polynomial it can be verified that if $K_2=K_4$ the final network will still be able to realize any pole location within the unit circle. This observation allows the use of case 8 in Table 2.5 and design improvement technique (a), resulting in the reduction of the final network to the form shown in Fig. 2.12 (this is already the minimum switch realization). The input capacitors were chosen arbitrarily so that a general numerator could also be realized. For any application at most 3 of these capacitors are necessary. The transfer functions for the general biquad in Fig. 2.12 are

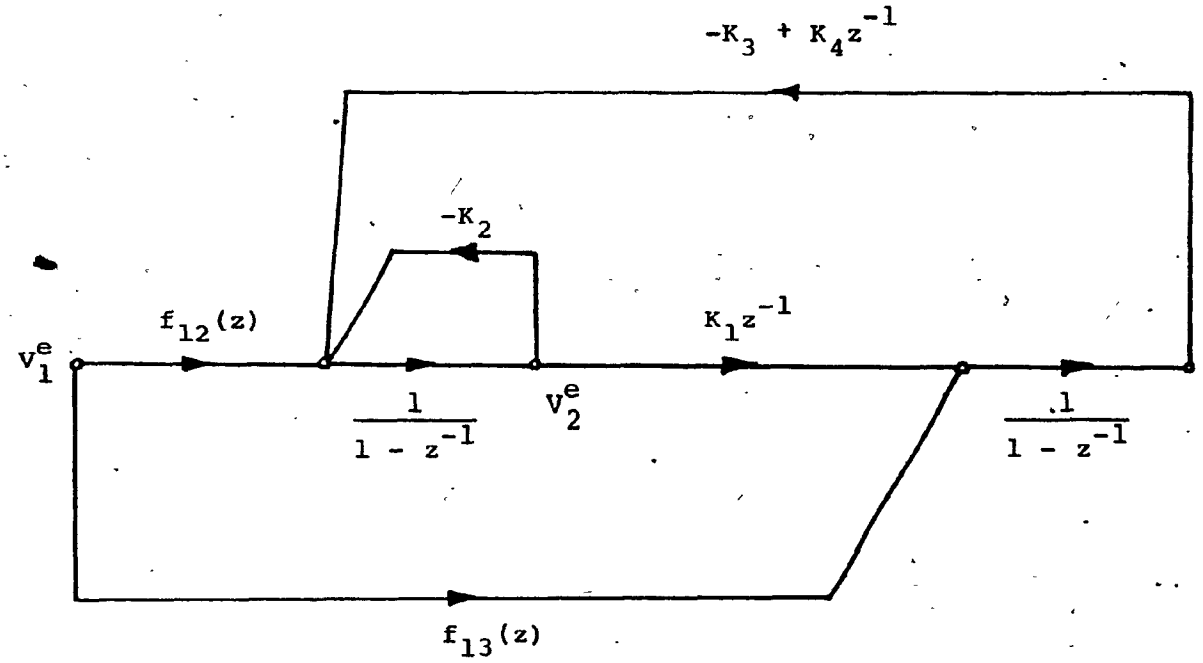


Figure 2.11: Flow graph representation of a general biquad.

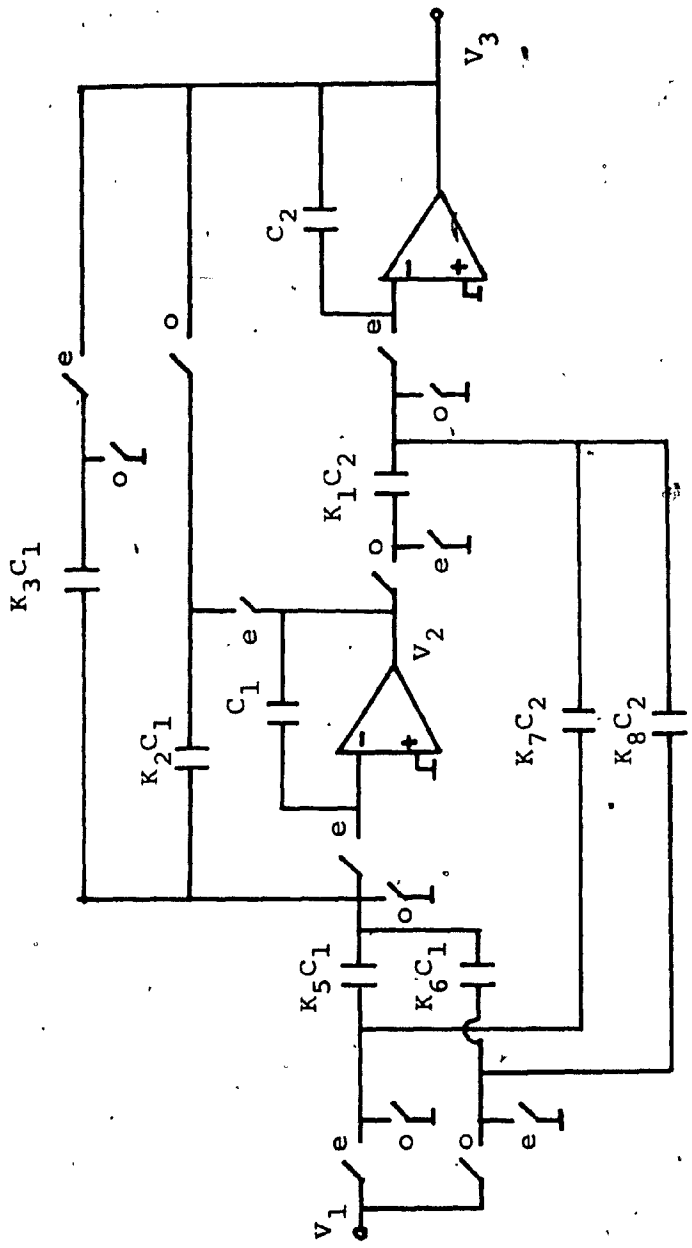


Figure 2.12: General biquad.

$$\frac{V_3^e}{V_1^e} = \frac{-K_7(1+K_2) + z^{-1}[K_8(1+K_2)+K_7-K_1K_5] + z^{-2}(K_1K_6-K_8)}{(1+K_2) + z^{-1}(K_1K_3-K_2-2) + z^{-2}(1-K_1K_2)}$$

$$\frac{V_2^e}{V_1^e} = \frac{(K_3K_7-K_5) + z^{-1}(K_5+K_6-K_2K_7-K_3K_8) + z^{-2}(K_2K_8-K_6)}{D(z)}$$

Depending on the design values for the input capacitors some further structural simplification or design improvement can be obtained by using the capacitor sets in Table 2.5 to combine feedforward and feedback capacitors.

2.10. SUMMARY

A systematic study of the generation and design of stray insensitive single OA SC networks has been presented. Towards this end, the parasitic insensitivity conditions reported earlier in the literature are exploited in such a way that redundant elements are automatically excluded from the resulting general networks. The networks thus obtained are separated in two classes. For each class, all realizable transfer functions are determined along with the necessary conditions for their realizability. Then all the possible ways to implement such transfer functions without the requirement of any matching conditions on the network elements are studied. The final results are tabulated in a ready-to-use format. The different types of input and

output voltage waveforms are considered. Finally, a comprehensive section on how to apply the derived results to generate practical structures is presented. Some techniques to improve the final results for smaller total capacitance and element spread are discussed.

A detailed example of an all-pass filter design is presented to illustrate the application of the proposed method. The results obtained compare very favorably with a previously reported structure. A second example on the generation of a general biquadratic building block is also presented.

In this chapter, we have considered systematic generation and design procedures for parasitic insensitive, single OA networks. The resulting networks are at most of the first order. In the next chapter, we extend the developments of this chapter for systematic generation and design of parasitic insensitive second order networks.

CHAPTER III

SECOND ORDER SC NETWORKS

3.1 INTRODUCTION

A great deal of effort has been spent in the past decade in the generation of good building blocks that can be used to implement high order filters, one of the most important blocks being the biquad. This chapter deals with the generation and design of such networks.

In order for a biquad to be generally useful as a building block, it should possess the following properties:

(1) Should be parasitic insensitive.

(2) Should be capable of realizing any stable z-domain transfer function.

(3) Should have low sensitivity with respect to the capacitance values.

(4) Should provide an area efficient realization.

Some structures satisfying the above mentioned properties have been presented [15,18,26] and extensively applied in the synthesis of SC networks. Usually the final decision in the selection of a structure to implement a given set of specifications is based on performance measures such as the total capacitance, capacitance spread, sensitivity, etc. Even though several SC structures may realize the same frequency response, they can vary widely

with respect to such figures of merit. Therefore, it is not uncommon to synthesize different networks from a pre-stablished library and then compare them for a final decision [40]. Consequently, it would be desirable to expand the existing set of good performance biquads in order to provide a wider design choice.

This chapter presents a systematic and comprehensive approach to exploit the stray insensitivity conditions proposed earlier in the literature [14] (see Chapter I) in the generation of SC biquads. The steps to obtain the most general stray insensitive second order network follow closely the development used in Chapter II for the single OA networks. As a consequence, many properties and definitions are borrowed directly from that chapter. Nevertheless, whenever the comprehension and/or the natural continuation of the text appear likely to be compromised by their omission, some of these properties and definitions are repeated for clarity of presentation. However, after the general second order SC network is obtained, this chapter takes on a completely different approach in comparison with the one followed in the previous chapter [42,43].

In order to provide easy to design building blocks, only canonic or quasi-canonic realizations are derived in this chapter. A total of 28 networks is obtained. The complete set includes the five parasitic insensitive biquad

building blocks presented so far in the literature [15,18,26]. The remaining 23 networks are completely new. The canonic structures obtained allow the realization of biquads with fewer capacitors than the ones presented in the literature. Sensitivity values are determined as functions of the parameters of a bilinearly transformed transfer function. Design equations are provided for all networks. Algorithms are given for dynamic range scaling. Also, spread and total capacitance minimization techniques are dicussed. Detailed examples are given along with experimental results in order to illustrate the possibility of design improvement using the new structures.

3.2 SOME DESIGN CONSIDERATIONS

The results of Chapter II show (see Table 2.4) that biquads satisfying the parasitic insensitivity conditions 1 and 2 cannot be realized using only one OA. Thus, henceforth only 2 OA realizations will be considered.

At this stage, some practical considerations are in order. Due to their periodic time-varying nature, SC filters are better analyzed by using the z-transform (z-domain) instead of the Laplace transform (s-domain). However, during each clock phase the network is a time-invariant analog circuit and as such must be stable so that the outputs of the OAs will not saturate. Consequently, in what follows a reliable SC biquad will be

required to have its overall feedback loop "broken" for both phases [41]. If such a loop occurs, the biquad would behave, within that phase, as an active-C circuit with an overall feedback and therefore would have its stability dependent on the frequency responses of the OAs. Of course, due to the broken feedback loop condition, a local negative feedback path must exist for both OAs during each phase.

It can be verified by inspection that a 2 OA biquad which satisfies the foregoing stability requirements along with the stray insensitivity conditions 1 and 2 discussed in Chapter I must assume in any phase, even or odd, the topology shown in Fig. 3.1. The boxes shown between various nodes may be open-circuits or capacitors.

3.3 GENERAL BIQUAD

The next step in the generation process is the application of the parasitic insensitivity conditions to the class of networks which assume, for each of the even and odd phases, a topology of the type shown in Fig. 3.1.

The networks in this class have some topological properties which will be useful for the derivations that follow. The noninverting OA input terminals are always grounded and the inverting ones are I-nodes (virtual gounds) for both phases. Also, both the even and the odd circuits, as defined in Chapter I, will always reduce to a network containing only the following six nodes:

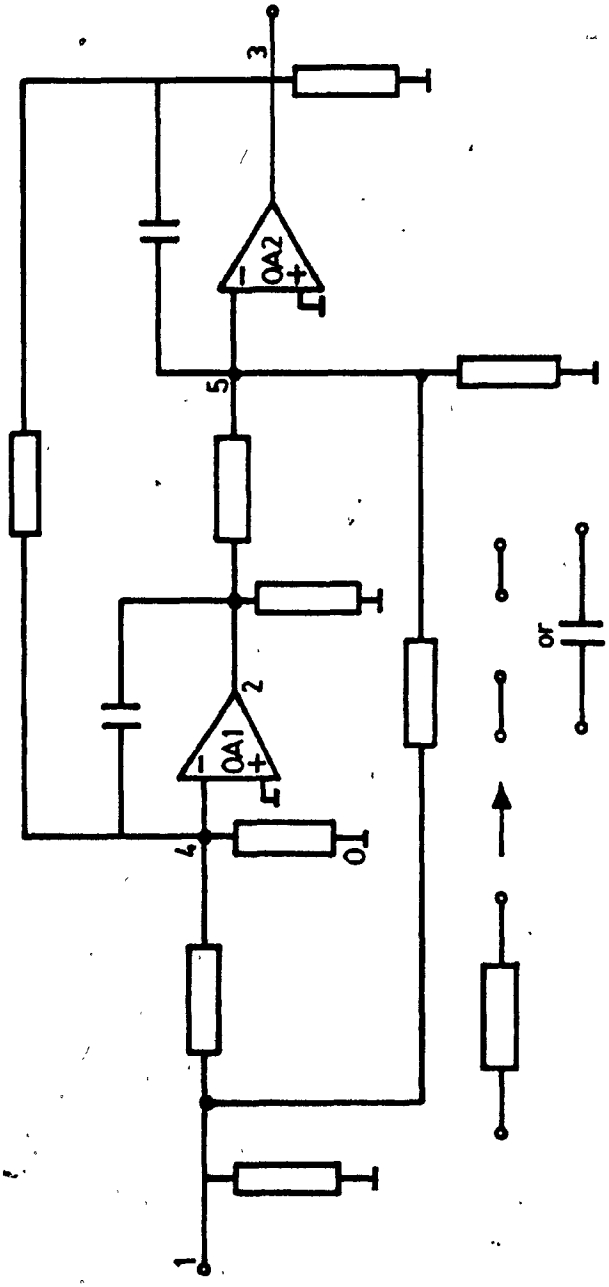


Figure 3.1: OA input connections (even and odd circuits).

node 0: Ground node.

node 1: Input voltage source.

node 2: Output of the OA#1 (OA1).

node 3: Output of the OA#2 (OA2).

node 4: Virtual ground of the OA1.

node 5: Virtual ground of the OA2.

Consequently, all other nodes must be switched to one of these six nodes in each phase to satisfy the parasitic insensitivity conditions. Henceforth, this node numbering assignment is always used. The remaining network nodes are numbered from 6 to n. Note from Fig. 3.1 that any two of the six basic nodes can never be connected together.

3.3.1 General Switching Scheme

As done in Chapter II, the network switching scheme will be represented by the switching matrices S_e (even phase) and S_o (odd phase) defined in [12]. With this definition and the proposed node numbering scheme, the (nxn) matrices S_e and S_o assume the form

$$S_{e,o} = \begin{array}{c} \\ 1^{e,o} \\ \vdots \\ 5^{e,o} \\ 6^{e,o} \\ \vdots \\ n^{e,o} \end{array} \begin{array}{c} \begin{array}{cccccc} 1 & \cdots & 5 & 6 & \cdots k \cdots & n \end{array} \\ \left[\begin{array}{cc|ccc} & & s_{16}^{e,o} & \cdots s_{1k}^{e,o} \cdots & s_{1n}^{e,o} \\ & I & \vdots & \vdots & \vdots \\ & & s_{56}^{e,o} & \cdots s_{5k}^{e,o} \cdots & s_{5n}^{e,o} \\ \hline & & & & \\ & 0 & & 0 & \end{array}\right] \end{array}$$

where I stands for the (5x5) identity matrix and 0 for the matrix whose entries are all zero. The term S^e_{ik} (S^o_{ik}) denotes the (i,k)th element of S_e (S_o). If a node is grounded in the even (odd) phase, all the entries in the correspnnding column of S_e (S_o) will be zero.

The first five rows of both S_e and S_o can be combined in a single switching matrix S (10xn) which contains all the informations about the switching scheme of the biphase SC network. The matrix S will have the following form

$$
S = \begin{array}{c} \\ 1^e \\ \\ 5^e \\ 1^o \\ \\ 5^o \end{array}
\begin{array}{c}
\begin{array}{cccc} 1 & \ldots & 5 & \end{array} \\
\left[\begin{array}{c|ccc}
 & s^e_{16} & s^e_{1k} & s^e_{1n} \\
I & \vdots & \vdots & \vdots \\
 & s^e_{56} & s^e_{5k} & s^e_{5n} \\
\hline
 & s^o_{16} & s^o_{1k} & s^o_{1n} \\
I & \vdots & \vdots & \vdots \\
 & s^o_{56} & s^o_{5k} & s^o_{5n}
\end{array}\right]
\end{array}
\begin{array}{c}
\begin{array}{ccc} 6 & \ldots & k \ldots n \end{array}
\end{array}
$$

Each column of S determines uniquely how a given node is connected to the six basic nodes in both the even and odd phases. Therefore, the study of all possible patterns for a typical column (say kth column) will determine in which ways an internal node k can be connected during each one of the two phases. The number of possibilities for a given column

is, however, excessively large. Nevertheless, by considering for S the four restrictions on the switching scheme discussed in section 2.3 for S_I, many redundancies and impractical cases can be avoided.

Note also that the switching of a V-node to an I-node or vice-versa in consecutive phases is not allowed (Condition 2 for stray insensitivity). The only way to allow such a switching would be by making V_2 or V_3 (V_1 is an independent source) equal to zero in one of the phases. Such voltage setting could only be accomplished by placing a switch across one of the OAs during that phase (voltage follower). However, this would eliminate the "memory" capacity of one of the integrators by discharging the continuous feedback capacitor and, as a consequence, no second order transfer function denominator could be obtained from the network. This is, in fact, the reason why such a switch does not appear in Fig. 3.1. Hence, for any column k of S it is required that

$$s_{ik}^{e,o} \times s_{jk}^{o,e} = 0 \quad \text{for } i=1,2,3 \text{ and } j=4,5$$

The application of these restrictions to a typical column of S leads to the 18 possible distinct switching patterns shown in Fig. 3.2. Due to restriction 4 above we can state that any SC network belonging to this class will have at most 23 nodes, plus the ground node. Fig. 3.3 shows

	node no.	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
even ph.	(1,k)	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
	(2,k)	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
	(3,k)	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
	(4,k)	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	(5,k)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0
odd ph.	(1,k)	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0
	(2,k)	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0
	(3,k)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0
	(4,k)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	(5,k)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 3.2: Possible node switching patterns.

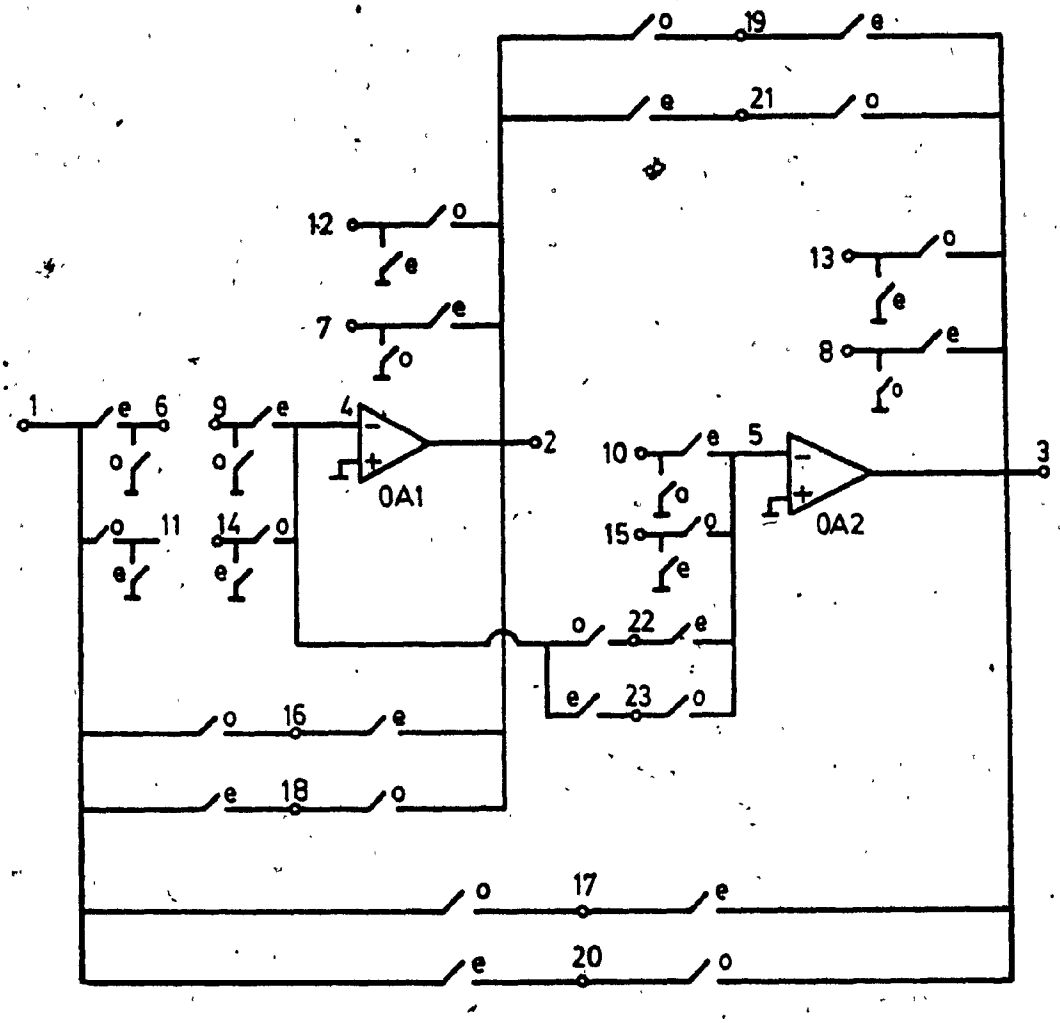


Figure 3.3: General switching scheme.

the resulting most general switching scheme for this class of SC biquads with its 23 nodes numbered according to the table in Fig. 3.2.

3.3.2 Capacitor Locations

In principle, a capacitor can be placed between any two of the 24 nodes of Fig. 3.3 without affecting the stray insensitivity of the resulting network. However, as already discussed in section 2.3, it can be easily verified that the network transfer functions will not be dependent on the following capacitors: (a) a capacitor permanently connected from any node to ground, (b) a capacitor placed between two nodes which are connected to V-nodes (voltage sources) in both phases, (c) a capacitor placed between two nodes which are connected to zero-valued-voltage nodes (I-nodes or ground) in both phases.

The remaining 120 capacitor locations are shown in Fig 3.4 where an asterisk at position (i,j) characterizes a possible capacitive connection from node i to node j.

A circuit with 120 elements, however, is still too complex to be handled in a useful manner for design purposes. Fortunately, further reduction is possible without restricting in any way the degrees of freedom desired in a design process. To proceed further, we need the following definition.

Definition: The "capacitor switching network" (CSN) of a

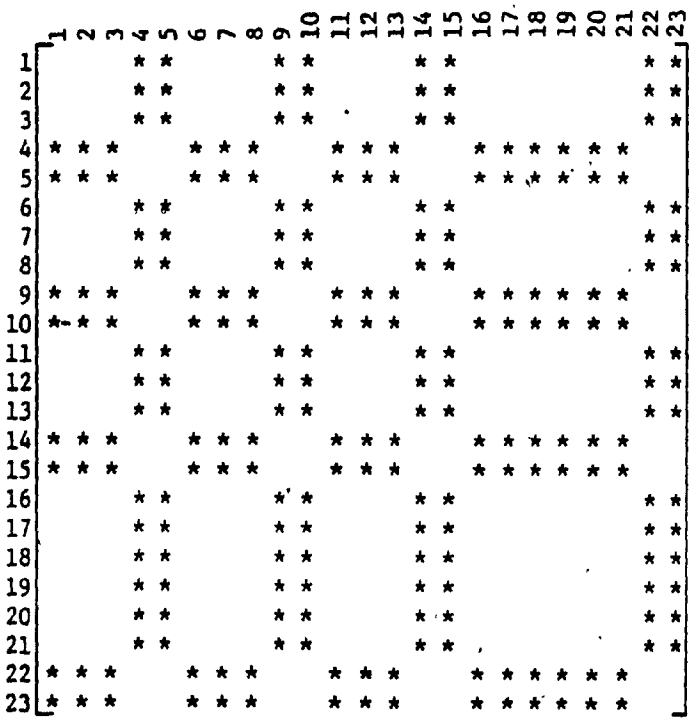


Figure 3.4: Useful capacitor locations.

given capacitor C is the subnetwork formed by C and all the switches and nodes which are connected to C during at least one phase. An allowable external node of a CSN is one of the following three types: V-node, I-node or ground. Hence, hereafter such a node will be referred only by its type.

The CSN is then the minimum subnetwork required to determine the contribution of a given capacitor C to the charge conservation equations (CCEs) of the network. Since the CSNs are dependent only on the switching patterns of the nodes connected to each of the capacitor terminals, different capacitors may have the same CSN. They can be differentiated only by the identification of the V-nodes and I-nodes of the CSN with the network nodes for each case.

The CSNs of the capacitors in Fig 3.4 were obtained by inserting them (one at a time) in the switching scheme of Fig 3.3 and then applying the definition given above. Any one of these CSNs belongs to the set of 16 distinct categories shown in Table 3.1 if the network nodes are referred only by their types. In Table 3.1, V stands for the voltage of a V-node and I represents a virtual ground. The contributions of the corresponding capacitors to the CCEs evaluated at the virtual grounds are presented. The particular case of a voltage signal sampled and held (S/H) over a full clock period is also considered.

Table 3.1: Different possible capacitor switch networks.

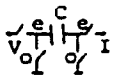
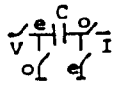
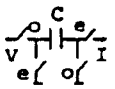
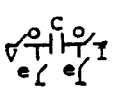
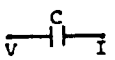
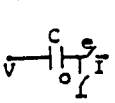
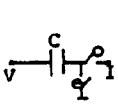
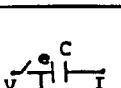
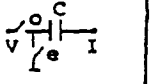
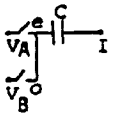
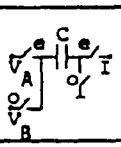
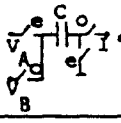
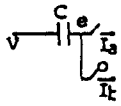
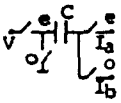
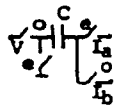
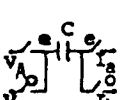
	$V^o \neq z^{-\frac{1}{2}}V^e$		$V^o = z^{-\frac{1}{2}}V^e$	
CSN	EVEN PHASE	ODD PHASE	EVEN PHASE	ODD PHASE
1. 	$C(V^e)$	0	$C(V^e)$	0
2. 	0	$C(-z^{-\frac{1}{2}}V^e)$	0	$C(-z^{-\frac{1}{2}}V^e)$
3. 	$C(-z^{-\frac{1}{2}}V^o)$	0	$C(-z^{-1}V^e)$	0
4. 	0	$C(V^o)$	0	$C(z^{-\frac{1}{2}}V^e)$
5. 	$C(V^e-z^{-\frac{1}{2}}V^o)$	$C(V^o-z^{-\frac{1}{2}}V^e)$	$C(1-z^{-1})V^e$	0
6. 	$C(V^e-z^{-\frac{1}{2}}V^o)$	0	$C(1-z^{-1})V^e$	0
7. 	0	$C(V^o-z^{-\frac{1}{2}}V^e)$	0	0
8. 	$C(V^e)$	$C(-z^{-\frac{1}{2}}V^e)$	$C(V^e)$	$C(-z^{-\frac{1}{2}}V^e)$

Table 3.1: continued.

	$V^o \neq z^{-\frac{1}{2}}V^e$		$V^o = z^{-\frac{1}{2}}V^e$	
CSN	EVEN PHASE	ODD PHASE	EVEN PHASE	ODD PHASE
9. 	$C(-z^{-\frac{1}{2}}V^o)$	$C(V^o)$	$C(-z^{-1}V^e)$	$C(z^{-\frac{1}{2}}V^e)$
10. 	$C(V_A^e - z^{-\frac{1}{2}}V_B^o)$	$C(V_B^o - z^{-\frac{1}{2}}V_A^e)$	$C(V_A^e - z^{-1}V_B^e)$	$C(V_B^e - V_A^e)z^{-\frac{1}{2}}$
11. 	$C(V_A^e - z^{-\frac{1}{2}}V_B^o)$	0	$C(V_A^e - z^{-1}V_B^e)$	0
12. 	0	$C(V_B^o - z^{-\frac{1}{2}}V_A^e)$	0	$C(V_B^e - V_A^e)z^{-\frac{1}{2}}$
13. 	$C(V^e - z^{-\frac{1}{2}}V^o) \to I_a$ $0 \to I_b$	$0 \to I_a$ $C(V^o - z^{-\frac{1}{2}}V^e) \to I_b$	$C(1-z^{-1})V^e \to I_a$ $0 \to I_b$	$0 \to I_a$ $0 \to I_b$
14. 	$C(V^e) \to I_a$ $0 \to I_b$	$0 \to I_a$ $C(-z^{-\frac{1}{2}}V^e) \to I_b$	$C(V^e) \to I_a$ $0 \to I_b$	$0 \to I_a$ $C(-z^{-\frac{1}{2}}V^e) \to I_b$
15. 	$C(-z^{-\frac{1}{2}}V^o) \to I_a$ $0 \to I_b$	$0 \to I_a$ $C(V^o) \to I_b$	$C(-z^{-1}V^e) \to I_a$ $0 \to I_b$	$0 \to I_a$ $C(z^{-\frac{1}{2}}V^e) \to I_b$
16. 	$C(V_A^e - z^{-\frac{1}{2}}V_B^o) \to I_a$ $0 \to I_b$	$0 \to I_a$ $C(V_B^o - z^{-\frac{1}{2}}V_A^e) \to I_b$	$C(V_A^e - z^{-1}V_B^e) \to I_a$ $0 \to I_b$	$0 \to I_a$ $C(V_B^e - V_A^e)z^{-\frac{1}{2}} \to I_b$

By inspection of Table 3.1 it can be verified that all possible contributions can be obtained from the following 4 basic ones: CV^e, and $-z^{-1/2}CV^o$ for the even phase, and CV^o and $-z^{-1/2}CV^e$ for the odd phase.

Note that each of these basic contributions can be independently provided by (and only by) a capacitor among those with CSNs of the types 1, 2, 3, and 4. Consequently, the remaining CSNs can be viewed as combinations of two or more of the basic CSNs. Of course, this observation is also valid for the case of S/H voltage sources. Therefore, the subnetwork formed by the capacitors whose CSNs are among the four basic ones is able to realize any voltage tranfer function realizable by the general network. Also, since each distinct contribution is provided by a different capacitor, every coefficient of the resulting CCEs can be independently controlled, yielding maximum design flexibility.

The network shown in Fig. 3.5 is the subnetwork mentioned above with four additional unswitched capacitors. Capacitors B and D are necessary to guarantee the linear operation of the network due to the non-overlapping nature of the clock signals [38]. With such clock signal, a period of time will always exist, after the end of one phase and the begining of the next one, during which all the switches will be open. Consequently, during these periods of time the OAs will operate without feedback if capacitors B and D

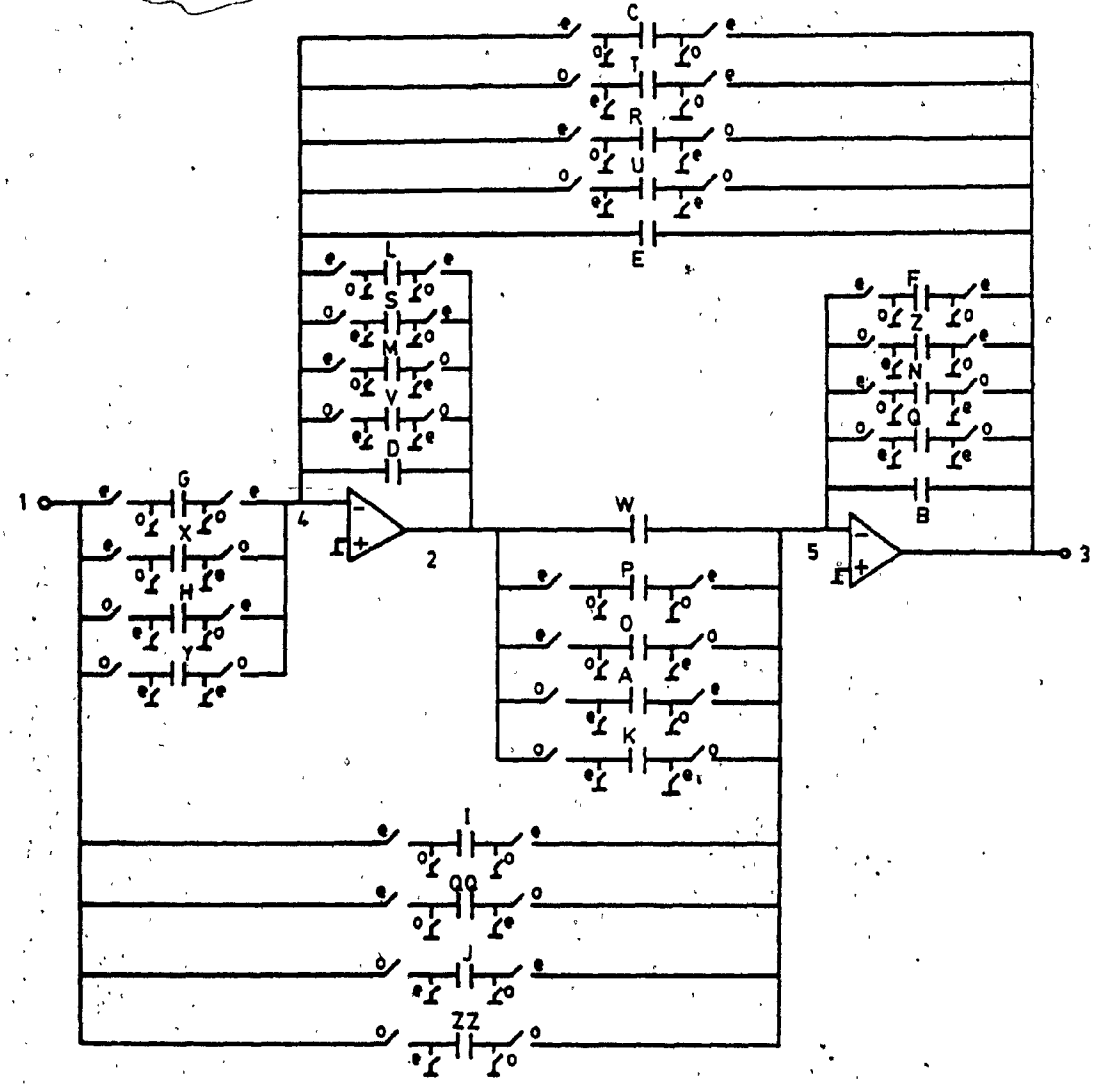


Figure 3.5: Simplified general biquad.

are not employed. Capacitors E and W have been included for the following reasons. They belong to the set of useful capacitive connections in Fig 3.4. Also, they are attractive from the design point of view since they represent the simplest form of connection between two nodes and are equivalent to the use of all four basic CSNs at the same time (see Table 3.1). Since we will be mostly concerned with the realizations of the poles of the transfer function, unswitched capacitors from node 1 to nodes 4 and 5 will not be included at this point. Their use as well as the use of the other CSNs will be considered later on.

In what follows, the network of Fig. 3.5 will be studied in detail. Clearly, this network has many redundant switches. However, they are retained so that one can readily identify the different CSNs. Besides, as discussed in Chapter II, the realization with the minimum number of switches can be easily derived from this one by identifying each node with the corresponding node type in Fig. 3.3 and then substituting all nodes of the same type by a single one.

3.3.3 Input and Output Conditions

In order to ensure automatic input-output compatibility of the different blocks in an interconnected network, the outputs of the biquads will be required to be S/H over a full clock period for inputs of the same type.

Hence, $V_3^o = z^{-1/2}V_3^e$ for $V_1^o = z^{-1/2}V_1^e$. The output at node 3 and the even phase were chosen arbitrarily without any loss of generality. Consequently, the transfer function V_3^e/V_1^e provides all the necessary information about the voltage V_3.

With these input and output conditions satisfied, all the biquads generated in this chapter can be easily interconnected since the output of one block will be automatically compatible with the input conditions of any other. Furthermore, at most one sample and hold circuit will be required (at the input), independently of which biquad output is chosen as the network output since all of them will automatically have a fully held sampled data voltage waveform.

The necessary and sufficient conditions to guarantee such output waveform are determined, by analysis, to be (i) W=O=K=0, (ii) Z=Q, and (iii) ZZ=QQ. No assumption was made on the waveform of V_2. Also, it can be shown that if conditions (ii) and (iii) are fulfilled, $V_3(z)$ is no longer dependent on the values of Z, Q, ZZ or QQ. Therefore, in an actual circuit these capacitors can be set equal to zero. When this is done, Fig. 3.5 yields the transfer functions:

$$\frac{V_3^e}{V_1^e} = \frac{\begin{array}{l}(1+V)\,[PG-I(1+L)\,]+z^{-1}\{J(1+L)\,(1+V)+\\ I(1+M)\,(1+S)+(X-Y)\,[A(1+L)-P(1+M)\,]-AG(1+S)-PH(1+V)\,\}+z^{-2}\{[AH-J(1+M)\,](1+S)\,\}\end{array}}{\begin{array}{l}(1+V)\,[(1+F)\,(1+L)-P(E+C)\,]+z^{-1}\{(T-U)\,[P(1+M)-A(1+L)\,]+P(E+R)\,(1+V)+A(E+C)\,(1+S)-\\ (1+F)\,(1+M)\,(1+S)-(1+N)\,(1+L)\,(1+V)\,\}+z^{-2}\{[(1+M)\,(1+N)-A(E+R)\,](1+S)\,\}\end{array}} \qquad (3.1)$$

$$\frac{V_2^e}{V_1^e} = \frac{\begin{array}{l}(1+V)\,[I(E+C)-G(1+F)\,]+z^{-1}\{(T-U)\,[AG-I(1+M)\,]+\\ (X-Y)\,[(1+F)\,(1+M)-A(E+C)\,]+[H(1+F)+G(1+N)-I(E+R)-J(E+C)\,](1+V)\,\}+\\ z^{-2}\{(T-U)\,[J(1+M)-AH]+(X-Y)\,[A(E+R)-(1+M)\,(1+N)\,]+(1+V)\,[J(E+R)-H(1+N)\,]\}\end{array}}{D(z)} \qquad (3.2)$$

$$\frac{V_2^o}{V_1^e} = z^{-1/2}\left\{\frac{\begin{array}{l}\{(T-U)\,[PG-I(1+L)\,]+(X-Y)\,[(1+F)\,(1+L)-P(E+C)\,]+\\ (1+S)\,[I(E+C)-G(1+F)\,]\}+z^{-1}\{(T-U)\,[J(1+L)-PH]+(X-Y)\,[P(E+R)-\\ (1+N)\,(1+L)\,]+(1+S)\,[H(1+F)+G(1+N)-J(E+C)-I(E+R)\,]\}+z^{-2}\{(1+S)\,[J(E+R)-H(1+N)\,]\}\end{array}}{D(z)}\right\} \qquad (3.3)$$

Capacitors B and D have been normalized to unity without any loss of generality [26]. This can be done because they belong to distinct groups, namely (A, B, P, F, N, I, J) and (G, H, X, Y, D, L, S, M, V, C, T, R, U, E), which can be independently scaled without affecting the network transfer functions. These groups are identified by the virtual ground to which their capacitors are connected in at least one phase [5]. If B and D are not normalized, then each element value in (3.1), (3.2) and (3.3) must be substituted by the ratio of that capacitance to the value of the feedback capacitor (B or D) which is connected to the same virtual ground.

3.4 BIQUAD BUILDING BLOCKS

Even though the network in Fig. 3.5 is able to realize any second order discrete transfer function, it is clear that it contains an unnecessarily large number of capacitors. Too many elements in a network tend to complicate the design procedure. Consequently, it is natural to look for canonical or quasi-canonical realizations. If these realizations cannot satisfy some design requirements such as low total capacitance, spread or sensitivity, then a configuration employing an increased number of elements should be tried. However, if the final objective is the reduction of the area required for integration, this increase in the number of elements should be exercised with care. The consequent increase in the

number of interconnections will require extra area in the chip and may overcome the advantages obtained in terms of total capacitance.

A general biquad employing 2 OAs will require at least seven capacitors (including the reference capacitors B and D) since the transfer function coefficients yield a system of five equations in terms of the network capacitance ratios. Since the number of elements necessary to implement the numerator will depend on the specific transfer function realized, we seek to minimize only the number of capacitors employed to realize a general denominator.

A biquadratic transfer function can be written in the form

$$H(z) = \frac{\gamma + \epsilon z^{-1} + \delta z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}} \qquad (3.4)$$

The coefficients α and β in (3.4) are completely determined by the capacitances in the feedback loop and, theoretically, four of these capacitors (including B and D) should be sufficient. However, it can be verified by inspection that a general and stable biquadratic transfer function cannot be obtained from the network in Fig. 3.5 using less than five capacitors in the feedback loop. Since at least one capacitor from each of the sets (C, T, R, U, E) and (P, A) must be present to guarantee the realizability of complex poles, the five capacitors are to be chosen in the following

way:

(a) capacitors B and D.

(b) one or two capacitors from (P,A).

(c) one or two capacitors from (C,T,R,U,E).

(d) none or one capacitor from (L,S,M,V,N,F).

Besides, P and E as well as P and C are not allowed to appear in the same network since they would close the feedback loop in the even phase and the network could become unstable in the corresponding configuration. Also, any two networks with identical feedback loops except for the interchange of the OAs are considered the same. After this first step in the generation process, the networks obtained must have their denominators derived from (3.1) and analyzed. This procedure eliminates those which are unstable or do not realize all possible complex pole pairs inside the unit circle. The study of stability and possible pole locations may be carried out as explained in Chapter I [26].

Following this procedure, the first 14 biquads in Table 3.2 are obtained, where the boxes represent the feedforward CSNs in Fig. 3.5. The name of each network is given by the capacitors employed in the feedback loop. Only networks PTL [26], PTF [15], ACF [15,26], AUE [18] and ACE [26] from Table 3.2 have been previously reported in the literature. The transfer functions are provided for the outputs which are fully held over a clock period. If only

Table 3.2: Biquad building blocks.

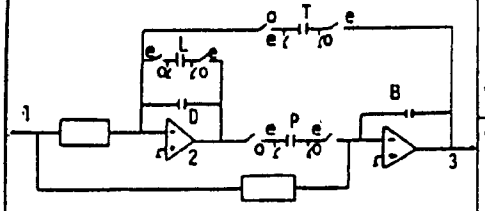
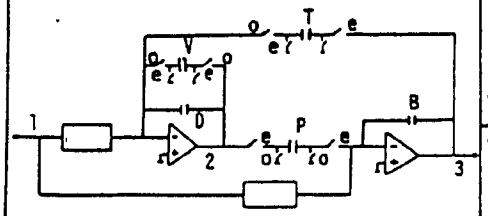
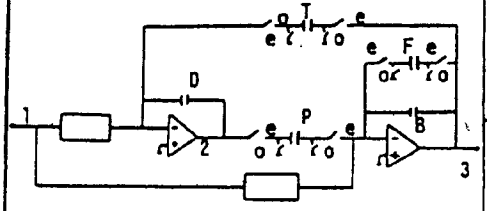
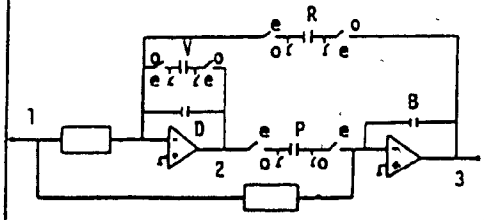
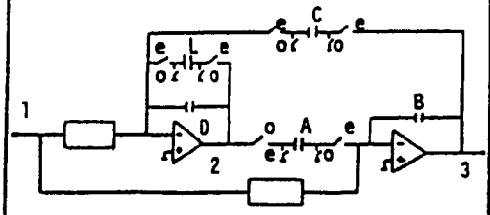
	NETWORK	TRANSFER FUNCTIONS
1 PTL		$\frac{V_3^e}{V_1^e} = \frac{[PG-I(1+L)]+z^{-1}[J(1+L)+I-(X-Y)P-PH]+z^{-2}(-J)}{(1+L)+z^{-1}(PT-L-2)+z^{-2}}$
2 PTV		$\frac{V_3^e}{V_1^e} = \frac{(1+V)(PG-I)+z^{-1}[J(1+V)+I-(X-Y)P-PH(1+V)]+z^{-2}(-J)}{(1+V)+z^{-1}(PT-V-2)+z^{-2}}$
3 PTF		$\frac{V_3^e}{V_1^e} = \frac{(PG-I)+z^{-1}[J+I-(X-Y)P-PH]+z^{-2}(-J)}{(1+F)+z^{-1}(PT-F-2)+z^{-2}}$
4 PRV		$\frac{V_3^e}{V_1^e} = \frac{(1+V)(PG-I)+z^{-1}[J(1+V)+I-(X-Y)P-PH(1+V)]+z^{-2}(-J)}{(1+V)+z^{-1}[PR(1+V)-V-2]+z^{-2}}$
5 ACL		$\frac{V_3^e}{V_1^e} = \frac{-I(1+L)+z^{-1}[J(1+L)+I+(X-Y)(1+L)A-AG]+z^{-2}(AH-J)}{(1+L)+z^{-1}(AC-L-2)+z^{-2}}$ $\frac{V_2^e}{V_1^e} = \frac{(IC-G)+z^{-1}[G+H-JC-(QQ-ZZ)C]+z^{-2}(-H)}{(1+L)+z^{-1}(AC-L-2)+z^{-2}}$

Table 3.2: Continued.

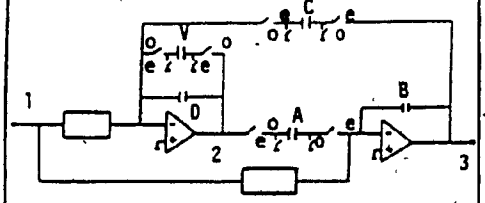
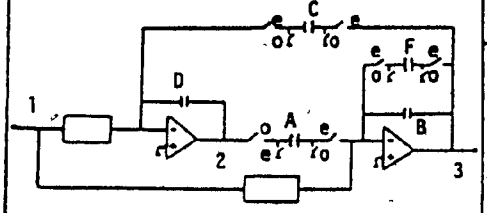
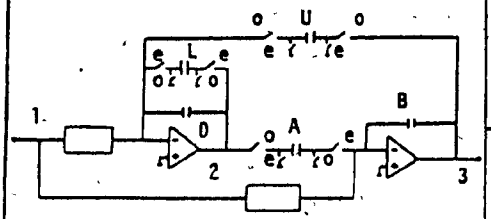
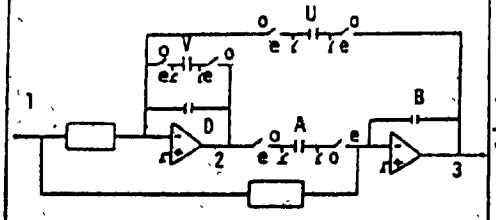
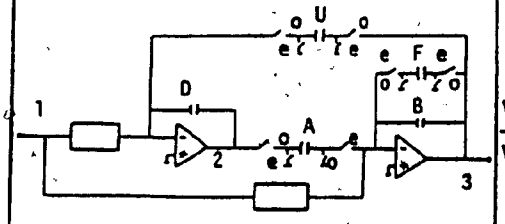
	NETWORK	TRANSFER FUNCTIONS
6 ACV		$\frac{V_3^e}{V_1^e} = \frac{-(1+V)I+z^{-1}[J(1+V)+I+(X-Y)A-AG] +z^{-2}(AH-J)}{(1+V) + z^{-1}(AC-V-2) + z^{-2}}$
7 ACF		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG] + z^{-2}(AH-J)}{(1+F) + z^{-1}(AC-F-2) + z^{-2}}$ $\frac{V_2^e}{V_1^e} = \frac{[IC-(1+F)G]+z^{-1}[G+H(1+F)-JC -(QQ-ZZ)C]+z^{-2}(-H)}{(1+F) + z^{-1}(AC-F-2) + z^{-2}}$
8 AUL		$\frac{V_3^e}{V_1^e} = \frac{-I(1+L)+z^{-1}[J(1+L)+I+(X-Y)(1+L)A -AG]+z^{-2}(AH-J)}{(1+L) + z^{-1}[AU(1+L)-L-2] + z^{-2}}$
9 AUY		$\frac{V_3^e}{V_1^e} = \frac{-(1+V)I+z^{-1}[J(1+V)+I+(X-Y)A-AG] +z^{-2}(AH-J)}{(1+V) + z^{-1}(AU-V-2) + z^{-2}}$
10 AUF		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG]+z^{-2}(AH-J)}{(1+F) + z^{-1}(AU-F-2) + z^{-2}}$

Table 3.2: Continued.

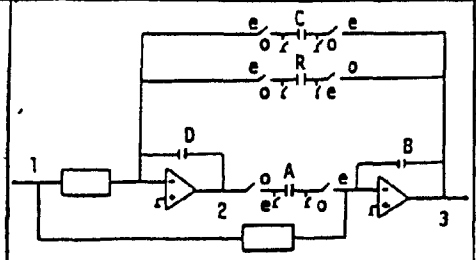
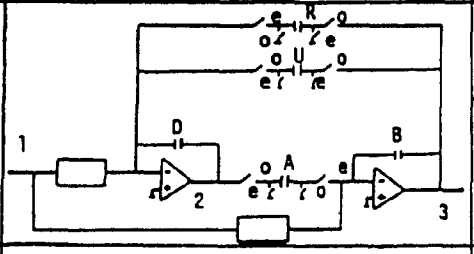
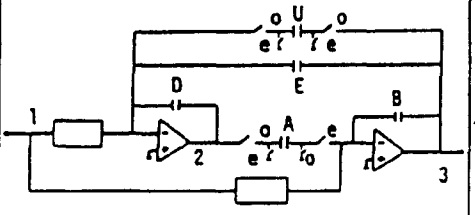
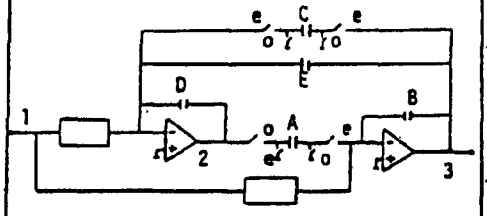
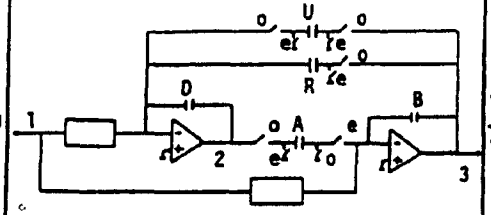
	NETWORK	TRANSFER FUNCTIONS
11 ACR		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG]+z^{-2}(AH-J)}{1+z^{-1}(AC-2)+z^{-2}(1-AR)}$ $\frac{V_2^e}{V_1^e} = \frac{(IC-G)+z^{-1}[G+H-JC-IR+(QQ-ZZ)(R-C)]+z^{-2}(JR-H)}{1+z^{-1}(AC-2)+z^{-2}(1-AR)}$
12 ARU		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG]+z^{-2}(AH-J)}{1+z^{-1}(AU-2)+z^{-2}(1-AR)}$
13 AUE		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG]+z^{-2}(AH-J)}{1+z^{-1}(AU+AE-2)+z^{-2}(1-AE)}$
14 ACE		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG]+z^{-2}(AH-J)}{1+z^{-1}(AE+AC-2)+z^{-2}(1-AE)}$ $\frac{V_2^e}{V_1^e} = \frac{[I(E+C)-G]+z^{-1}[G+H-J(E+C)-IE-(QQ-ZZ)C]+z^{-2}(JE-H)}{1+z^{-1}(AE+AC-2)+z^{-2}(1-AE)}$
15 ARRU		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG]+z^{-2}(AH-J)}{1+z^{-1}(AR+AU-2)+z^{-2}(1-AR)}$

Table 3.2: Continued.

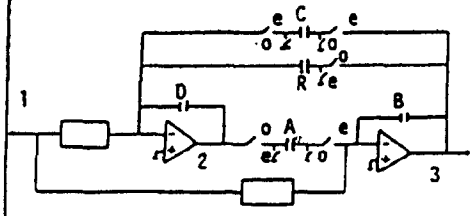
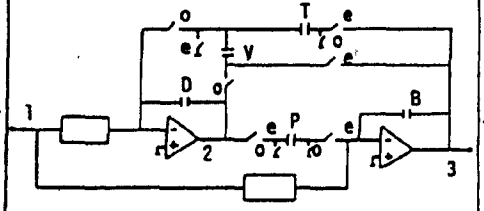
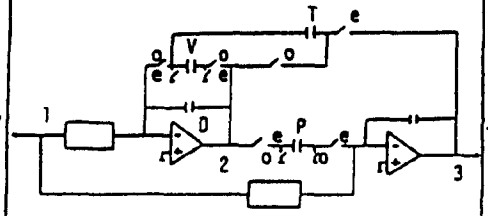
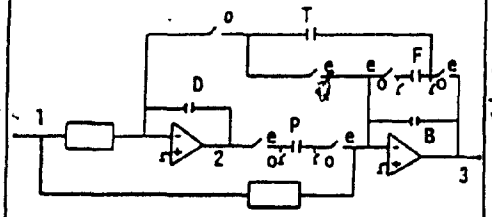
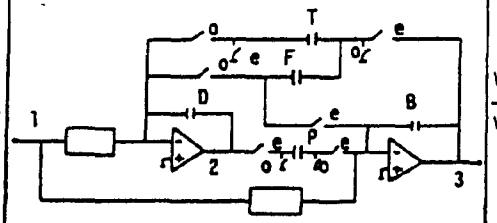
	NETWORK	TRANSFER FUNCTIONS
16 ARRC		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG)]+z^{-2}(AH-J)}{1+z^{-1}(AC+AR-2)+z^{-2}(1-AR)}$
17 PTVV		$\frac{V_3^e}{V_1^e} = \frac{(1+V)(PG-I)+z^{-1}[J(1+V)+I-(X-Y)P -(1+V)PH]+z^{-2}(-J)}{(1+V)+z^{-1}(PT+PV-V-2)+z^{-2}}$
18 PTTV		$\frac{V_3^e}{V_1^e} = \frac{(1+V+T)(PG-I)+z^{-1}[(J-PH)(1+V+T) +I-(X-Y)P]+z^{-2}(-J)}{(1+V+T)+z^{-1}(PT-V-T-2)+z^{-2}}$
19 PTTF (*)		$\frac{V_3^e}{V_1^e} = \frac{(PG-I)+z^{-1}[J+I-(X-Y)P-PH]+z^{-2}(-J)}{(1+F+\tilde{T})+z^{-1}(P\tilde{T}-F-\tilde{T}-2)+z^{-2}}$ $\tilde{T} = \frac{T}{D} \quad \hat{T} = \frac{T}{B}$
20 PTFF (*)		$\frac{V_3^e}{V_1^e} = \frac{(PG-I)+z^{-1}[J+I-(X-Y)P-PH]+z^{-2}(-J)}{(1+\tilde{F})+z^{-1}(PT+P\hat{F}-\tilde{F}-2)+z^{-2}}$ $\tilde{F} = \frac{F}{B} \quad \hat{F} = \frac{F}{D}$

Table 3.2: Continued.

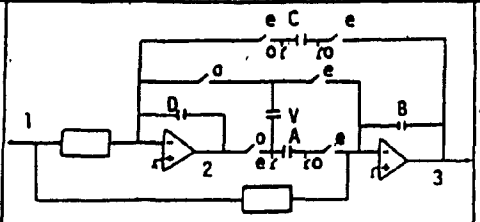
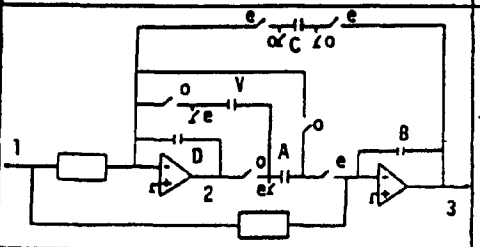
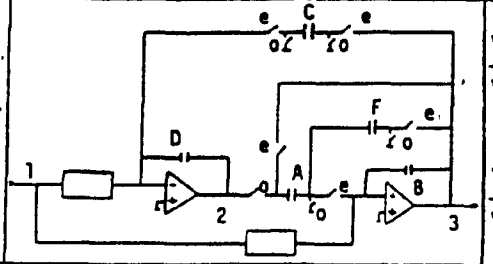
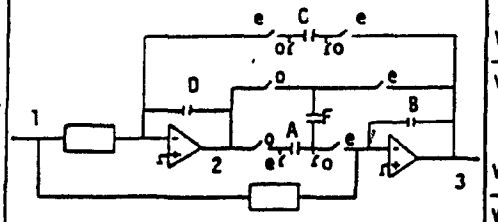
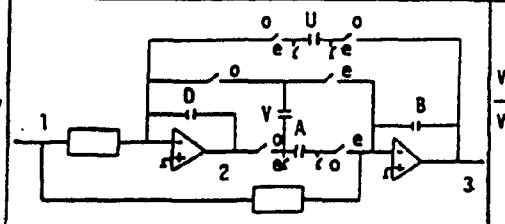
	NETWORK	TRANSFER FUNCTIONS
21 ACVV (*)		$\frac{V_3^e}{V_1^e} = \frac{-(1+\tilde{V})I+z^{-1}[J(1+\tilde{V})+I+(X-Y-G)(A+\hat{V})]+z^{-2}[(A+\hat{V})H-J]}{(1+\tilde{V})+z^{-1}(AC+C\tilde{V}-\tilde{V}-2)+z^{-2}}$ $\tilde{V}=\frac{V}{D} \quad \hat{V}=\frac{V}{B}$
22 AACV (*)		$\frac{V_3^e}{V_1^e} = \frac{-(1+\tilde{A}+\hat{V})I+z^{-1}[J(1+\tilde{A}+\hat{V})+I+(X-Y)\tilde{A}-\tilde{A}G]+z^{-2}(\tilde{A}H-J)}{(1+\tilde{A}+\hat{V})+z^{-1}(\tilde{A}C-\tilde{A}-\hat{V}-2)+z^{-2}}$ $\tilde{A}=\frac{A}{B} \quad \hat{A}=\frac{A}{D}$
23 AACF		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)A-AG]+z^{-2}(AH-J)}{(1+F+A)+z^{-1}(AC-A-F-2)+z^{-2}}$ $\frac{V_2^e}{V_1^e} = \frac{[IC-G(1+F+A)]+z^{-1}[G+H(1+F+A)-C(J+QQ-ZZ)]+z^{-2}(-H)}{(1+F+A)+z^{-1}(AC-A-F-2)+z^{-2}}$
24 ACFF		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y-G)(A+F)]+z^{-2}[(A+F)H-J]}{(1+F)+z^{-1}(AC+FC-F-2)+z^{-2}}$ $\frac{V_2^e}{V_1^e} = \frac{[IC-G(1+F)]+z^{-1}[G+H(1+F)-C(J+QQ-ZZ)]+z^{-2}(-H)}{(1+F)+z^{-1}(AC+FC-F-2)+z^{-2}}$
25 AUVV (*)		$\frac{V_3^e}{V_1^e} = \frac{-(1+\tilde{V})I+z^{-1}[J(1+\tilde{V})+I+(X-Y-G)(A+\hat{V})]+z^{-2}[(A+\hat{V})H-J]}{(1+\tilde{V})+z^{-1}(AU+\tilde{V}U-\tilde{V}-2)+z^{-2}}$ $\tilde{V}=\frac{V}{D} \quad \hat{V}=\frac{V}{B}$

Table 3.2: Continued.

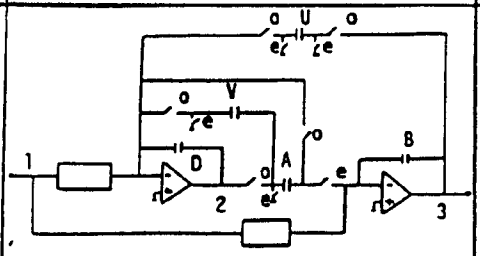
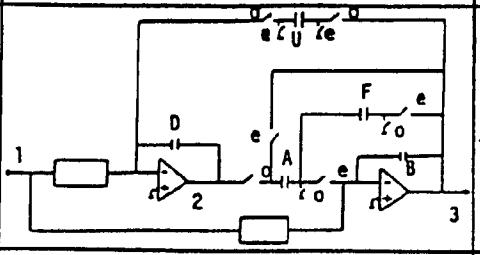
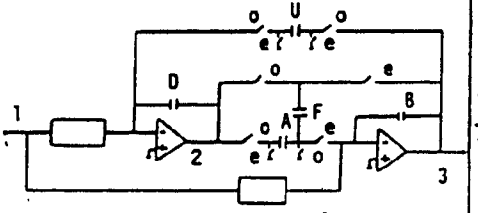
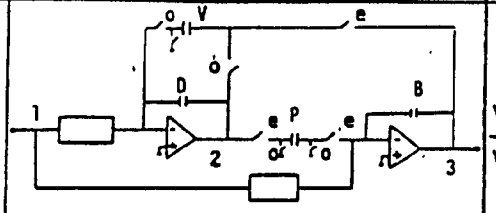
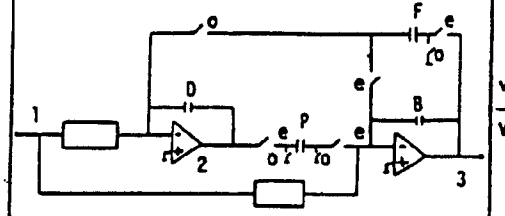
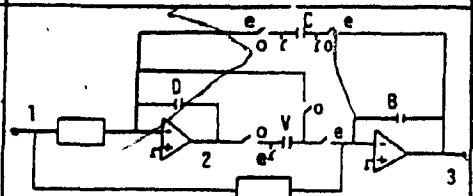
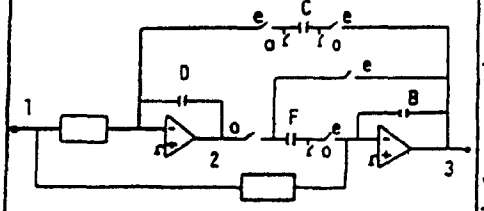
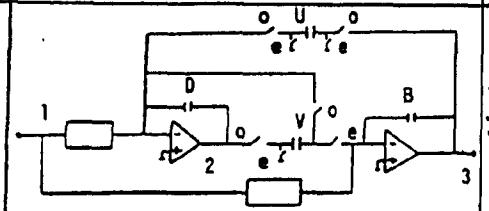
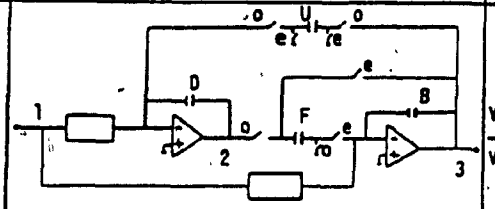
	NETWORK	TRANSFER FUNCTIONS
26 AAUV (*)		$\frac{V_3^e}{V_1^e} = \frac{-(1+\hat{A}+V)I+z^{-1}[J(1+\hat{A}+V)+I+(X-Y-G)\tilde{A}]+z^{-2}(\tilde{A}H-J)}{(1+\hat{A}+V)+z^{-1}(\tilde{A}U-\hat{A}-V-2)+z^{-2}}$ $\tilde{A}=\frac{A}{B} \quad \hat{A}=\frac{A}{D}$
27 AAUF		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y-G)A]+z^{-2}(AH-J)}{(1+F+A)+z^{-1}(AU-F-A-2)+z^{-2}}$
28 AUFF		$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y-G)(A+F)]+z^{-2}[(A+F)H-J]}{(1+F)+z^{-1}(AU+FU-F-2)+z^{-2}}$
29 PVV	 PTVV (T = 0) or PTTV (V = 0)	$\frac{V_3^e}{V_1^e} = \frac{(1+V)(PG-I)+z^{-1}[J(1+V)+I-(X-Y)P-PH(1+V)]+z^{-2}(-J)}{(1+V)+z^{-1}(PV-V-2)+z^{-2}}$
30 PFF (*)	 PTFF (T = 0) or PTTF (F = 0)	$\frac{V_3^e}{V_1^e} = \frac{(PG-I)+z^{-1}[J+I-(X-Y)P-PH]+z^{-2}(-J)}{(1+\tilde{F})+z^{-1}(P\hat{F}-\tilde{F}-2)+z^{-2}}$ $\tilde{F}=\frac{F}{B} \quad \hat{F}=\frac{F}{D}$

Table 3.2: Continued.

	NETWORK	TRANSFER FUNCTION
31 CVV (*) 6	 AACV (V = 0) or ACVV (A = 0)	$\frac{V_3^e}{V_1^e} = \frac{-(1+\tilde{V})I+z^{-1}[J(1+\tilde{V})+I+(X-Y)\tilde{V}-\tilde{V}G]+z^{-2}(\tilde{V}H-J)}{(1+\tilde{V})+z^{-1}(C\tilde{V}-\tilde{V}-2)+z^{-2}}$ $\tilde{V}=\frac{V}{D} \quad \hat{V}=\frac{V}{B}$
32 CFF	 ACFF (A = 0) or AACF (F = 0)	$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)F-FG]+z^{-2}(FH-J)}{(1+F)+z^{-1}(CF-F-2)+z^{-2}}$ $\frac{V_2^e}{V_1^e} = \frac{[IC-G(1+F)]+z^{-1}[G+H(1+F)-(J+QQ-ZZ)C]+z^{-2}(-H)}{(1+F)+z^{-1}(CF-F-2)+z^{-2}}$
33 UVV (*)	 AUVV (A = 0) or AAUV (V = 0)	$\frac{V_3^e}{V_1^e} = \frac{-(1+\tilde{V})I+z^{-1}[J(1+\tilde{V})+I+(X-Y-G)\hat{V}]+z^{-2}(\tilde{V}H-J)}{(1+\tilde{V})+z^{-1}(U\hat{V}-\tilde{V}-2)+z^{-2}}$ $\tilde{V}=\frac{V}{D} \quad \hat{V}=\frac{V}{B}$
34 UFF	 AUFF (A = 0) or AAUF (F = 0)	$\frac{V_3^e}{V_1^e} = \frac{-I+z^{-1}[J+I+(X-Y)F-FG]+z^{-2}(FH-J)}{(1+F)+z^{-1}(UF-F-2)+z^{-2}}$

V_2 is desired as output, capacitors QQ and ZZ in Fig. 3.5 can be restored without affecting the fully held character of the output. The only exception is the network ACE. In this case the capacitor E would transfer an amount of charge proportional to V_3^o to capacitor D, making $V_2^o \neq z^{-1/2} V_2^e$ if $V_3^o \neq z^{-1/2} V_3^e$. Hence, for the network ACE, QQ=ZZ is an absolutely necessary condition for a S/H V_2. Otherwise, the presence of these two capacitors can be exploited in realizing the zeros of the transfer function. Therefore, their contributions are considered in the transfer functions V_2^e/V_1^e.

Looking at certain pairs of networks in Table 3.2, (networks PTF and AUV, for instance) the reader might be tempted to identify them as the same network except for the interchange of the even and odd phases. However, one should keep in mind that, by hypothesis, the input voltage is always changing its value at the even sampling instants and that, with this condition fixed, even and odd switches cannot have their names simply exchanged without modifying the network characteristics. Therefore, such networks are, in fact, distinct. Also, it can be verified that some sets of networks in Table 3.2 have very similar transfer functions (ACF and AUF for instance). However, despite of the transfer function similarities, their feedback loop capacitors are switched in different phases. Since the switching scheme (CSN) can affect considerably the ways in

which the various CSNs from the feedforward or feedback loop capacitors can interact, all networks are presented separately. This point will become more evident on the examples at the end of this chapter.

We now turn our attention to the remaining CSNs in Table 3.1. Though it has been shown that the CSNs of types 5 to 16 are not necessary for realizing any pole-zero pattern, they can be used to generate new network topologies with very interesting properties. Since each of these CSNs may be thought as a combination of 2 or more CSNs among types 1 to 4, we can substitute some sets of CSNs from the feedback loops of the 14 already generated biquads by other sets employing the new CSNs such that the same kind of contributions from each voltage to each of the CCEs can be obtained (qualitatively speaking) without increasing the number of capacitors. The procedure is better illustrated by an example. Consider, for instance, the network PTV. The virtual ground of OA1 has the two feedback loop switched capacitors T and V connected to it. These capacitors have CSNs of types 2 and 4 respectively. Therefore, their contributions to the corresponding CCEs can be summarized as follows:

	even phase	odd phase
T	0	$-z^{-1/2}V_3^e$
V	0	V_2^o

total 0 $V_2^o - z^{-1/2}V_3^e$ (3.5)

From Table 3.1, we collect all CSNs which contribute to the CCEs of a single virtual ground with the terms V_2^o or $-z^{-1/2}V_3^e$ in the odd phase and zero in the even phase, for a voltage V_3 held over a full clock period. Here we are not interested in cancellation of the contributions since this would lead to the use of redundant elements. This search yields

0 for even phase: C_2, C_4, C_7 and C_{12}.

V_2^o for odd phase: C_4, C_5, C_7, C_9, C_{10} and C_{12}.

$-z^{-1/2}V_3^e$ for odd phase: C_2, C_8, C_{10} and C_{12}.

where C_i stands for a capacitor with CSN of type i. We then determine by inspection how the types of contribution in (3.5) can be obtained by using at most two of these capacitors. The following sets satisfy this condition:

	CCE in odd phase	
(a) (C_2, C_4):	$C_4V_2^o - z^{-1/2}C_2V_3^e$	(3.6)
(b) C_{12}:	$C_{12}(V_2^o - z^{-1/2}V_3^e)$	(3.7)
(c) (C_2, C_{12}):	$C_{12}V_2^o - z^{-1/2}(C_2 + C_{12})V_3^e$	(3.8)
(d) (C_4, C_{12}):	$(C_4 + C_{12})V_2^o - z^{-1/2}C_{12}V_3^e$	(3.9)

Option (a) leads to the same network PTV. The others will give us the networks PVV, PTVV and PTTV, respectively, in Table 3.2.

The transfer functions of the networks generated in this way must be checked for stability and realization of second order transfer functions with arbitrary complex pole locations since the contributions to the CCEs were guaranteed only qualitatively, not quantitatively. Also, it is useful to note that even though these networks are not directly derived from the biquad in Fig. 3.5, their transfer functions can be easily determined without the need of a new analysis. Let us return to our example. The transfer function of the network PVV (case b) can be directly derived from the transfer function of PTV (case a) by making $C_2=C_4=C_{12}$ or, equivalently, T=V. In order to obtain the transfer function for the network PTVV (case c), on the other hand, one must substitute C_4 (capacitor V) by C_{12} (new CSN) and C_2 (capacitor T) by C_2+C_{12} in the original function. Now, renaming $C_{12}=V$ this is equivalent to the simple substitution of T by T+V in the transfer function of PTV. Likewise, for case d (PTTV) one must substitute V by T+V. Indeed, a closer look at these biquads reveals that network PVV, for instance, could have been obtained from PTV with T=V by application of the superposition principle. If V_2 and V_3 are alternately considered zero in PVV, the original CSNs for T and V can be immediately visualized.

The same reasoning is valid for networks PTVV and PTTV. Nevertheless, the formal approach just presented is advisable in order to avoid missing any case.

Repeating this process for all 14 networks from PTL to ACE the remaining biquads in Table 3.2 can be obtained. All the transfer functions listed are normalized for B=D=1. Special care must be taken, however, in evaluating the coefficients of the denormalized transfer function for the networks marked with an asterisk (*). In these cases the same capacitor is connected to both virtual grounds and its value has to be divided by B or D depending on its position in the transfer function. To avoid mistakes, the notation $(\tilde{C},\hat{C})$ has been introduced in Table 3.2. Of course, if B=D then $\tilde{C}=\hat{C}$. The last 6 biquads in Table 3.2 are canonic networks since they employ only 4 capacitors in their feedback loops. These canonic networks are, in fact, subnetworks of some of the others (see Table 3.2), where one capacitor has been made zero. Nevertheless, they are presented here separately because they constitute the only existing particular cases of these 28 biquads in which a general second order transfer function can be obtained employing the minimum possible number of capacitors in the feedback loop. Consequently, for comparable dynamic ranges, spreads and total capacitances, these designs should be preferred over the others since they employ less components.

The CSN equivalences just discussed can also be applied after synthesis procedure to combine the feed-forward and feedback loop capacitors. It should be mentioned that the CSN equivalence technique was first suggested in [26]. However, in [26] this was done only for a particular case - the combination of CSNs of types 1 and 3 for a fully held voltage source. The procedure proposed here is general.

8.5 SENSITIVITIES

In evaluating the pole frequency (ω_o) and Q-factor sensitivities with respect to capacitor variations for a biquad, conditions such as high sampling rates and high Q-factors are usually imposed [17,26]. However, in designing SC filters, the z-domain transfer function is, most of the times, obtained from the desired analog specification via the bilinear transformation [4,5] so that lower clock to cutoff frequency ratios can be used. Also, although it is usually believed that the sensitivity is proportional to the Q-factor by analogy to the continuous case, this does not always happens in SC filters [44]. Furthermore, low Q sections are quite often necessary in the synthesis of high order cascade filters [4,40].

In this chapter we make the only assumption that the z-domain transfer function H(z) has been obtained by the bilinear transformation of a s-domain specification H(s).

Since the bilinear transformation is the most frequently used technique in synthesis of biquads, this assumption is clearly a reasonable one.

For simplicity, we shall evaluate the bandwidth (ω_b) sensitivities. The Q sensitivities can always be obtained by noting that $Q=\omega_o/\omega_b$. Hence

$$S_x^Q = S_x^{\omega_o} - S_x^{\omega_b} \quad \text{for} \quad S_x^F = \frac{x}{F}(\partial F/\partial x)$$

Since we use the bilinear transformation in obtaining H(z) from H(s), the inverse transformation must be used to recover the original design parameters as functions of the SC network elements. Applying the inverse bilinear transformation

$$z^{-1} = \frac{1 - (sT/2)}{1 + (sT/2)} \tag{3.10}$$

to a H(z) as in (3.4) and comparing the resulting denominator with

$$D(s) = s^2 + \omega_b s + \omega_o^2$$

yields

$$\omega_o T = 2\left[\frac{1 + \alpha + \beta}{1 - \alpha + \beta}\right]^{1/2} \tag{3.11}$$

$$\omega_b T = \frac{4(1-\beta)}{1 - \alpha + \beta} \tag{3.12}$$

where T is considered invariant because, in general, the clock signal is taken from a very stable source. Also, ω_o and ω_b can be evaluated taking into account the warping effects of the bilinear transformation [4,5,25]. Determining and from Table 3.2 for each biquad as functions of the capacitance values, the evaluation of the sensitivities is straightforward. Here it is important to include explicitly the capacitors B and D in the analytical expressions of the transfer function coefficients.

In order to clarify the results, the 28 biquads were grouped in 6 subclasses. A subclass is defined by the property that the denominator in the transfer function of a network within the given subclass can be obtained from that of another one in the same subclass simply by substituting one set of variables by another.

The values obtained for the sensitivities can be expressed as functions of ω_o and ω_b by back substituting the values of α and β and using the expressions (3.11) and (3.12). Table 3.3 shows the sensitivities for the different classes where the nature of the variable substitutions within each class are clearly indicated. Note that the sensitivities are presented in a very convenient form. Having these expressions and the desired s-domain transfer function one can discard the high sensitivity networks even before the design starts. Only for subclasses E and F some capacitor values are required to determine the weighting

Table 3.3: Sensitivities.

NETWORKS								SUBCLASS A	
PTL	PTV	ACL	ACV	AUV	ACF	PTF	AUF	$S_{\omega_o^T}$	$S_{\omega_b^T}$
P	P	A	A	A	A	P	A	$\frac{1}{2}\left[1 + (\frac{\omega_o^T}{2})^2\right]$	$(\frac{\omega_o^T}{2})^2$
T	T	C	C	U	C	T	U	$\frac{1}{2}\left[1 + (\frac{\omega_o^T}{2})^2\right]$	$(\frac{\omega_o^T}{2})^2$
L	V	L	V	V	F	F	F	$-\frac{1}{2}(\frac{\omega_b^T}{2})$	$1 - \frac{\omega_b^T}{2}$
B	B	B	B	B	D	D	D	$-\frac{1}{2}\left[1 + (\frac{\omega_o^T}{2})^2\right]$	$-(\frac{\omega_o^T}{2})^2$
D	D	D	D	D	B	B	B	$-\frac{1}{2}\left[1 - \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2\right]$	$-\left[1 - \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2\right]$
SUBCLASS B									
PRV	AUL							$S_{\omega_o^T}$	$S_{\omega_b^T}$
P	A							$\frac{1}{2}\left[1 + (\frac{\omega_o^T}{2})^2\right]$	$(\frac{\omega_o^T}{2})^2$
R	U							$\frac{1}{2}\left[1 + (\frac{\omega_o^T}{2})^2\right]$	$(\frac{\omega_o^T}{2})^2$
V	L							$\frac{\omega_b^T}{4}\left[\frac{1 - \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2}{1 + \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2}\right]$	$1 + \frac{\omega_b^T}{2}\left[\frac{2(\frac{\omega_o^T}{2})^2}{1 + \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2} - 1\right]$
B	B							$-\frac{1}{2}\left[1 + (\frac{\omega_o^T}{2})^2\right]$	$-(\frac{\omega_o^T}{2})^2$
D	D							$-\frac{1}{2}\left\{1 + (\frac{\omega_o^T}{2})^2 + \frac{\omega_b^T}{2}\left[\frac{1 - \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2}{1 + \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2}\right]\right\}$	$-1 + \frac{\omega_b^T}{2} - (\frac{\omega_o^T}{2})^2\left[2 - \frac{1 - \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2}{1 + \frac{\omega_b^T}{2} + (\frac{\omega_o^T}{2})^2}\right]$

Table 3.3: Continued.

NETWORKS								SUBCLASS C	
ACR	ARU							$S_x^{\omega_o T}$	$S_x^{\omega_b T}$
A	A							$\frac{1}{2}\left[1 + \frac{\omega_b T}{2} - \left(\frac{\omega_o T}{2}\right)^2\right]$	$1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2$
C	U							$\frac{1}{2}\left\{1+\left(\frac{\omega_o T}{2}\right)^2 + \frac{\omega_b T}{4}\left[1+\frac{1}{\left(\frac{\omega_o T}{2}\right)^2}\right]\right\}$	$\frac{\omega_b T}{4} + \left(\frac{\omega_o T}{2}\right)^2$
R	R							$\frac{\omega_b T}{8}\left[1 - \frac{1}{\left(\frac{\omega_o T}{2}\right)^2}\right]$	$1 + \frac{\omega_b T}{4}$
B	B							$-\frac{1}{2}\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$	$-\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$
D	D							$-\frac{1}{2}\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$	$-\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$
SUBCLASS D									
AUE	ACE	ARRU	ARRC					$S_x^{\omega_o T}$	$S_x^{\omega_b T}$
A	A	A	A					$\frac{1}{2}\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$	$1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2$
U	C	U	C					$\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2\right]$	$\left(\frac{\omega_o T}{2}\right)^2$
E	E	R	R					$\frac{\omega_b T}{4}$	$1 + \frac{\omega_b T}{2}$
B	B	B	B					$-\frac{1}{2}\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$	$-\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$
D	D	D	D					$-\frac{1}{2}\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$	$-\left[1 + \frac{\omega_b T}{2} + \left(\frac{\omega_o T}{2}\right)^2\right]$

Table 3.3: Continued.

NETWORKS								SUBCLASS E	
PTVV	PTFF	ACVV	ACFF	AUVV	AUFF			$S_x^{\omega_o T}$	$S_x^{\omega_b T}$
P	P	C	C	U	U			$\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2\right]$	$\left(\frac{\omega_o T}{2}\right)^2$
T	T	A	A	A	A			$\frac{1}{2}\left\{\frac{T}{T+V}\left[1 + \left(\frac{\omega_o T}{2}\right)^2\right]\right\}$	$\frac{T}{T+V}\left(\frac{\omega_o T}{2}\right)^2$
V	F	V	F	V	F			$\frac{1}{2}\frac{V}{T+V}\left\{\left[1+\left(\frac{\omega_o T}{2}\right)^2\right] - \frac{\omega_b T}{2}\right\}$	$1 + \frac{V}{T+V}\left(\frac{\omega_o T}{2}\right)^2 - \frac{\omega_b T}{2}$
B	D	B	D	B	D			$-\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2\right]$	$-\left(\frac{\omega_o T}{2}\right)^2$
D	B	D	B	D	B			$-\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2 - \frac{\omega_b T}{2}\right]$	$-\left[1 + \left(\frac{\omega_o T}{2}\right)^2 - \frac{\omega_b T}{2}\right]$
SUBCLASS F									
PTTV	PTTF	AACV	AACF	AAUV	AAUF			$S_x^{\omega_o T}$	$S_x^{\omega_b T}$
P	P	C	C	U	U			$\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2\right]$	$\left(\frac{\omega_o T}{2}\right)^2$
T	T	A	A	A	A			$\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2 - \frac{T}{V+T}\left(\frac{\omega_b T}{2}\right)\right]$	$\frac{T}{T+V}\left(1 - \frac{\omega_b T}{2}\right) + \left(\frac{\omega_o T}{2}\right)^2$
V	F	V	F	V	F			$-\frac{1}{2}\left(\frac{V}{V+T}\right)(\omega_b T)$	$\frac{V}{V+T}\left[1 - \frac{\omega_b T}{2}\right]$
B	D	B	D	B	D			$-\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2\right]$	$-\left(\frac{\omega_o T}{2}\right)^2$
D	B	D	B	D	B			$-\frac{1}{2}\left[1 + \left(\frac{\omega_o T}{2}\right)^2 - \frac{\omega_b T}{2}\right]$	$-\left[1 + \left(\frac{\omega_o T}{2}\right)^2 - \frac{\omega_b T}{2}\right]$

factors T/(T+V) and V/(V+T). However, these factors are bounded between 0 and 1 and hence a worst case analysis can give a reasonable idea about the final sensitivities. Note that, in these terms, T represents a capacitance value and should not be confused with the T in $\omega_o T$ and $\omega_b T$ which stands for the sampling period. Also, note that T and V in such factors should be replaced by other variables if a network other than PTVV or PTTV is being analyzed. From this table it can also be verified that by increasing the Q-factor and the sampling rate ($\omega_o T \to 0$ and $\omega_b T \to 0$) one may in fact decrease the network sensitivities.

3.6 SYNTHESIS PROCEDURE

Tables 3.4, 3.5 and 3.6 provide the necessary information for the synthesis of the 34 networks in Table 3.2 which allow 41 different designs since 7 of these biquads may have both outputs fully held over a sampling period.

In order to condense the design equations, the denominator and numerator polynomials of the transfer functions were grouped into 7 (Table 3.4) and 10 (Table 3.5) different types respectively. All 41 transfer functions can be realized by combining these polynomials and by applying some elementary variable transformations. The step by step synthesis procedure can be outlined as follows:

(a) Table 3.2- Choose the network to be synthesized.

Table 3.4: Design equations - denominators.

(*) B = D = 1

$D(z) = 1 + \alpha z^{-1} + \beta z^{-2}$	CAPACITANCE VALUES(*)
$D_1(z) = 1 + \frac{PT-L-2}{1+L} z^{-1} + \frac{1}{1+L} z^{-2}$	$P = 1$, $L = \frac{1-\beta}{\beta}$, $T = \frac{1+\alpha+\beta}{\beta}$
$D_2(z) = 1 + \frac{PR(1+V)-V-2}{1+V} z^{-1} + \frac{1}{1+V} z^{-2}$	$P = 1$, $V = \frac{1-\beta}{\beta}$, $R = 1+\alpha+\beta$
$D_3(z) = 1 + (AC-2)z^{-1} + (1-AR)z^{-2}$	$A = 1$, $R = 1-\beta$, $C = \alpha+2$
$D_4(z) = 1 + (AU+AE-2)z^{-1} + (1-AE)z^{-2}$	$A = 1$, $E = 1-\beta$, $U = 1+\alpha+\beta$
$D_5(z) = 1 + \frac{PV-V-2}{1+V} z^{-1} + \frac{1}{1+V} z^{-2}$	$V = \frac{1-\beta}{\beta}$, $P = \frac{1+\alpha+\beta}{1-\beta}$
$D_6(z) = 1 + \frac{PT+PV-V-2}{1+V} z^{-1} + \frac{1}{1+V} z^{-2}$	$P = \frac{1+\alpha+\beta}{2(1-\beta)}$, $T = \frac{1-\beta}{\beta}$, $V = \frac{1-\beta}{\beta}$
$D_7(z) = 1 + \frac{PT-V-T-2}{1+V+T} z^{-1} + \frac{1}{1+V+T} z^{-2}$	$P = \frac{2(1+\alpha+\beta)}{1-\beta}$, $T = \frac{1-\beta}{2\beta}$, $V = \frac{1-\beta}{2\beta}$

Table 3.5: Design equations - numerators.

$N(z) = \gamma + \epsilon z^{-1} + \delta z^{-2}$		
$N_1(z) = \frac{PG-I(1+L)}{1+L} + \frac{[J(1+L)+I-(X-Y)P-PH]}{1+L} z^{-1} + \frac{(-J)}{1+L} z^{-2}$	$\gamma \leq 0$ $\quad I = -\gamma \quad G = 0$ $J = -\delta(1+L) \quad H+X-Y = \frac{-\delta(1+L)^2-\gamma-\epsilon(1+L)}{P}$	$\gamma > 0$ $\quad I = 0 \quad G = \gamma(1+L)/P$ $J = -\delta(1+L) \quad H+X-Y = \frac{-\delta(1+L)^2-\epsilon(1+L)}{P}$
$N_2(z) = (PG-I) + \frac{[J(1+V)+I-(X-Y)P-PH(1+V)]}{1+V} z^{-1} + \frac{(-J)}{1+V} z^{-2}$	$\gamma < 0 \quad I = -\gamma \quad G = 0$ $J = -\delta(1+V)$ $H(1+V)+X-Y = \frac{-\delta(1+V)^2-\gamma-\epsilon(1+V)}{P}$	$\gamma > 0 \quad G = \gamma/P \quad I = 0$ $J = -\delta(1+V)$ $H(1+V)+X-Y = \frac{-\delta(1+V)^2-\epsilon(1+V)}{P}$
$N_3(z) = \frac{(PG-I)}{1+F} + \frac{[J+I-(X-Y)P-PH]}{1+F} z^{-1} + \frac{(-J)}{1+F} z^{-2}$	$\gamma < 0 \quad I = -\gamma(1+F) \quad G = 0$ $J = -\delta(1+F)$ $H+X-Y = \frac{-(\delta+\gamma+\epsilon)(1+F)}{P}$	$\gamma > 0 \quad G = \gamma(1+F)/P \quad I = 0$ $J = -\delta(1+F)$ $H+X-Y = \frac{-(\delta+\epsilon)(1+F)}{P}$
$N_4(z) = -I + \frac{[J(1+L)+I+(X-Y)(1+L)A-AG]}{1+L} z^{-1} + \frac{(AH-J)}{1+L} z^{-2}$	$\delta < 0 \quad I = -\gamma \quad H = 0$ $J = -\delta(1+L)$ $(X-Y)(1+L)-G = \frac{\delta(1+L)^2+\gamma+\epsilon(1+L)}{A}$	$\delta \geq 0 \quad I = -\gamma \quad J = 0$ $H = \delta(1+L)/A$ $(X-Y)(1+L)-G = \frac{\gamma+\epsilon(1+L)}{A}$
$N_5(z) = \frac{IC-G}{1+L} + \frac{[G+H-JC-(QQ-ZZ)C]}{1+L} z^{-1} + \frac{(-H)}{1+L} z^{-2}$	$\gamma < 0 \quad I = 0 \quad G = -\gamma(1+L)$ $H = -\delta(1+L)$ $J+QQ-ZZ = -(\gamma+\delta+\epsilon)(1+L)/C$	$\gamma > 0 \quad G = 0 \quad I = \gamma(1+L)/C$ $H = -\delta(1+L)$ $J+QQ-ZZ = -(\delta+\epsilon)(1+L)/C$
$N_6(z) = -I + \frac{[J(1+V)+I+(X-Y)A-AG]}{1+V} z^{-1} + \frac{(AH-J)}{1+V} z^{-2}$	$\delta < 0 \quad I = -\gamma \quad H = 0$ $J = -\delta(1+V)$ $X-Y-G = [\delta(1+V)^2+\gamma+\epsilon(1+V)]/A$	$\delta > 0 \quad I = -\gamma \quad J = 0$ $H = [\delta(1+V)]/A$ $X-Y-G = [\gamma+\epsilon(1+V)]/A$
$N_7(z) = \frac{(-I)}{1+F} + \frac{[J+I+(X-Y)A-AG]}{1+F} z^{-1} + \frac{AH-J}{1+F} z^{-2}$	$\delta < 0 \quad I = -\gamma(1+F) \quad H = 0$ $J = -\delta(1+F)$ $X-Y-G = [(\gamma+\epsilon+\delta)(1+F)]/A$	$\delta > 0 \quad I = -\gamma(1+F) \quad J = 0$ $H = [\delta(1+F)]/A$ $X-Y-G = [(\gamma+\epsilon)(1+F)]/A$
$N_8(z) = \frac{[IC-G(1+F)]}{1+F} + \frac{[G+H(1+F)-JC-(QQ-ZZ)C]}{1+F} z^{-1} + \frac{(-H)}{1+F} z^{-2}$	$\gamma < 0 \quad G = -\gamma \quad I = 0$ $H = -\delta(1+F)$ $J+QQ-ZZ = [-\gamma-\epsilon(1+F)-\delta(1+F)^2]/C$	$\gamma > 0 \quad H = -\delta(1+F) \quad G = 0$ $I = [\gamma(1+F)]/C$ $J+QQ-ZZ = [-\epsilon(1+F)-\delta(1+F)^2]/C$

Table 3.5: Continued.

$N(z) = \gamma + \varepsilon z^{-2} + \delta z^{-4}$		
$N_9(z) = (IC-G)+[G+H-JC-IR+(QQ-ZZ)(R-C)]z^{-1} + (JR-H)z^{-2}$	$\gamma < 0$ $I=QQ=ZZ=0$ $G = -\gamma$ $J = [-(\delta+\gamma+\varepsilon)]/(C-R)$ $H = JR-\delta$	$\gamma > 0$ $G=QQ=ZZ=0$ $I = \gamma/C$ $J = I - (\gamma+\delta+\varepsilon)/(C-R)$ $H = JR-\delta$
	$\delta < 0$ $J=QQ=ZZ=0$ $H = -\delta$ $I = (\gamma+\varepsilon+\delta)/(C-R)$ $G = IC-\gamma$	$\delta > 0$ $H=QQ=ZZ=0$ $J = \delta/R$ $I = J + (\gamma+\varepsilon+\delta)/(C-R)$ $G = IC-\gamma$
$N_{10}(z) = [I(E+C)-G]+[G+H-J(E+C)-IE-(QQ-ZZ)C]z^{-1}+(JE-H)z^{-2}$	$\gamma < 0$ $I=QQ=ZZ=0$ $G = -\gamma$ $J = -(\gamma+\varepsilon+\delta)/C$ $H = JE-\delta$	$\gamma > 0$ $G=QQ=ZZ=0$ $I = \gamma/(C+E)$ $J = I - (\gamma+\delta+\varepsilon)/C$ $H = JE-\delta$
	$\delta < 0$ $J=QQ=ZZ=0$ $H = -\delta$ $I = (\gamma+\varepsilon+\delta)/C$ $G = I(E+C)-\gamma$	$\delta > 0$ $H=QQ=ZZ=0$ $J = \delta/E$ $I = J + (\gamma+\varepsilon+\delta)/C$ $G = I(E+C)-\gamma$

Table 3.6: Initial design procedure.

NETWORK	DENOMINATOR $D_f(z)$	VARIABLE TRANSF. FOR $D_f(z)$	NUMERATOR $N_k(z)$	VARIABLE TRANS. FOR $N_k(z)$
	f		k	
PTL	1	—	1	—
PTV	1	V=L	2	—
PTF	1	F=L	3	—
PRV	2	—	2	—
ACL	1	C=T , A=P	4	—
ACV	1	V=L , A=P , C=T	6	—
ACF	1	F=L , A=P , C=T	7	—
AUL	2	L=V , A=P , U=R	4	—
AUV	1	V=L , A=P , U=T	6	—
AUF	1	F=L , A=P , U=T	7	—
ACR	3	—	7	F=0
ARU	3	U=C	7	F=0
AUE	4	—	7	F=0
ACE	4	C=U	7	F=0
ARRU	4	R=E	7	F=0
ARRC	4	C=U , R=E	7	F=0
PTVV	6	—	2	—
PTTV	7	—	2	V=V+T
PTTF	7	F=V	3	F=F+T
PTFF	6	F=V	3	—
ACVV	6	A=T , C=P	6	A=A+V
AACV	7	A=T , C=P	6	V=V+A
AACF	7	A=T , C=P , F=V	7	F=F+A
ACFF	6	A=T , C=P , F=V	7	A=A+F
AUVV	6	A=T , U=P	6	A=A+V
AAUV	7	A=T , U=P	6	V=V+A
AAUF	7	A=T , U=P , F=V	7	F=F+A
AUFF	6	A=T , U=P , F=V	7	A=A+F
PVV	5	—	2	—
PFF	5	F=V	3	—
CVV	5	C=P	6	A=V
CFF	5	C=P , F=V	7	A=F
UVV	5	U=P	6	A=V
UFF	5	U=P , F=V	7	A=F
ACL/2	1	C=T , A=P	5	—
ACF/2	1	F=L , A=P , C=T	8	—
ACR/2	3	—	9	—
ACE/2	4	C=U	10	—
AACF/2	7	A=T , C=P , F=V	8	F=F+A
ACFF/2	6	A=T , C=P , F=V	8	—
CFF/2	5	C=P , F=V	8	—

(b) Table 3.6 (1st column)- With the name of the network, obtain the subindex i corresponding to the respective denominator $D_i(z)$.

(c) Table 3.4- Determine the values of the feedback loop capacitors to realize $D_i(z)$ using the coefficients α and β of the transfer function $H(z)$ written as in (3.4).

(d) Table 3.6 (3rd column)- Apply the variable transformations in order to obtain the values of the capacitors actually employed in the network.

(e) Table 3.6 (4th column)- With the name of the network, obtain the subindex k corresponding to the respective numerator $N_k(z)$.

(f) Table 3.6 (5th column)- Perform the necessary modifications in the capacitor values for this network.

(g) Table 3.5- Determine the values of the feedforward capacitors for the case in hand.

At this stage, some observations are in order:

(1) If the output at V_2 is desired, the network's name followed by "/2" (for instance, ACL/2) must be used in Table 3.6. Also, in these cases X=Y=0 has been assumed in Table 3.5 to guarantee a fully held output.

(2) Network designs ACR/2 and ACE/2 allow both positive and negative gain constants. The others have this property only for some transfer functions. However, in most of the cases the sign of the gain constant is a trivial constraint.

(3) The design equations presented are not unique but a

set of feasible solutions. It can be readily verified that at most 3 feedforward capacitors are necessary to realize any biquadratic transfer function with any of these networks.

3.6.1 Dynamic Range Scaling

The synthesis equations presented so far result in unscaled capacitor values. After this initial design, capacitor scaling can be used to improve the network performance without affecting the final transfer function. An important factor to be considered in this regard is the dynamic range of the network. The voltage level of the main output is usually controlled in the approximation step by scaling the original transfer function. However, the secondary output voltage level cannot be easily controlled during the approximation or initial design steps. If such output voltage level is too high, overloads may occur. On the other hand, if it is very low, additional noise might be involved. Therefore, it is desirable to have a procedure which allows the scaling of this output for a synthesized network. In Table 3.7 two distinct methods which were derived from simple flow graph techniques are given for the networks in Table 3.2.

Out of the 41 possible designs, 29 can always be scaled. From the remaining 12, 8 can be scaled if certain conditions are satisfied. If, however, such conditions are

Table 3.7: Dynamic range scaling.

NETWORK	METHOD 1 $V_{2,3} \rightarrow kV_{2,3}$	METHOD 2 $V_{2,3} \rightarrow kV_{2,3}$	CONDITIONS
PTL to ARRC, PFF, CVV, UVV SCALING V_2	(A,D,L,M,P,S,Y) → ÷ k	(G,X,H,Y,C,T,R,U,E) → × k (P,A) → ÷ k (NOT POSSIBLE FOR PFF, CVV, UVV)	—
PTL to ARRC SCALING V_3	(B,F,N,C,T,R,U,E) → ÷ k	(I,J,QQ,ZZ,P,A) → × k (C,T,R,U,E) → ÷ k	—
PTVV	(D,P) → ÷ k T → T+V(1-1/k) V → V/k	(G,H,X,Y) → × k T → k[T+V(1-1/k)] P → P/k	$k > \frac{1}{1+\frac{I}{V}}$
PTTV	(D,P) → ÷ k $V \rightarrow \frac{1}{k}[V+T(1-k)]$	(G,H,X,Y) → × k V → V+T(1-k) T → kT P → P/k	$k < 1+\frac{V}{T}$
PTTF	(D,P) → ÷ k	(G,H,X,Y) → × k F → F+T(1-k) T → kT P → P/k	$k < 1+\frac{F}{T}$ FOR METHOD 2
PTFF	(D,P) → ÷ k	(G,H,X,Y) → × k T → k[T+F(1-1/k)] P → P/k	$k > \frac{1}{1+\frac{I}{F}}$ FOR METHOD 2
ACVV	(D,V,A) → ÷ k	(G,H,X,Y) → × k $A \rightarrow \frac{1}{k}[A+V(1-k)]$ C → kC	$k < 1+\frac{A}{V}$ FOR METHOD 2
AACV	(D,V,A) → ÷ k	(G,H,X,Y) → × k V → V+A(1-1/k) A → A/k C → kC	$k > \frac{1}{1+\frac{V}{A}}$ FOR METHOD 2

Table 3.7: Continued.

NETWORK	METHOD 1	METHOD 2	CONDITIONS
AACF	$F \leftarrow F+A(1-1/k)$ $(D,A) \leftarrow + k$	$(G,H,X,Y,C) \leftarrow \times k$ $F \leftarrow F+A(1-1/k)$ $A \leftarrow A/k$	$k > \frac{1}{1+\frac{F}{A}}$
ACFF	$D \leftarrow D/k$ $A \leftarrow \frac{1}{k}[A+F(1-k)]$	$(G,H,X,Y,C) \leftarrow \times k$ $A \leftarrow \frac{1}{k}[A+F(1-k)]$	$k < 1+\frac{A}{F}$
AUVV	$(D,V,A) \leftarrow + k$	$(G,H,X,Y,U) \leftarrow \times k$ $A \leftarrow \frac{1}{k}[A+V(1-k)]$	$k < 1+\frac{A}{V}$ FOR METHOD 2
AAUV	$(D,V,A) \leftarrow + k$	$(G,H,X,Y,U) \leftarrow \times k$ $V \leftarrow V+A(1-1/k)$ $A \leftarrow A/k$	$k > \frac{1}{1+\frac{V}{A}}$ FOR METHOD 2
AAUF	$F \leftarrow F+A(1-1/k)$ $(D,A) \leftarrow + k$	$(G,H,X,Y,U) \leftarrow \times k$ $F \leftarrow F+A(1-1/k)$ $A \leftarrow A/k$	$k > \frac{1}{1+\frac{F}{A}}$
AUFF	$D \leftarrow D/k$ $A \leftarrow \frac{1}{k}[A+F(1-k)]$	$(G,H,X,Y,U) \leftarrow \times k$ $A \leftarrow \frac{1}{k}[A+F(1-k)]$	$k < 1+\frac{A}{F}$
AACF/2	$F \leftarrow \frac{1}{k}[F+A(1-k)]$ $(B,C) \leftarrow + k$	$(I,J,QQ,ZZ) \leftarrow \times k$ $F \leftarrow F+A(1-k)$ $C \leftarrow C/k$ $A \leftarrow kA$	$k < 1+\frac{F}{A}$
ACFF/2	$A \leftarrow A+F(1-1/k)$ $(B,C,F) \leftarrow + k$	$(I,J,QQ,ZZ) \leftarrow \times k$ $C \leftarrow C/k$ $A \leftarrow k[A+F(1-1/k)]$	$k > \frac{1}{1+\frac{A}{F}}$

not fulfilled, they can still be scaled to a closer-to-desired condition. Only the remaining 4 (PVV, CFF, CFF/2 and UFF) cannot be scaled at all.

Since a very popular method of scaling for optimum dynamic range is to equalize the maximum OA output voltage values for a fixed input level [17,18,26], we present here the analytical expressions to determine the maximum magnitude of a second order z-domain transfer function.

Given an H(z) expressed as in (3.4), it can be shown that the maximum value of its magnitude occurs at one of the following frequencies:

(a) $\omega T = 0 \quad (z=1)$.

(b) $\omega T = \pi \quad (z=-1)$.

(c) $$\omega_m T = \cos^{-1}\left\{\frac{-4(af-cd) \pm \sqrt{16(af-cd)^2 - 8(bf-ec)\left[(a-c)e+(f-d)b\right]}}{4(bf-ec)}\right\}$$

where

$$a=\gamma^2+\varepsilon^2+\delta^2$$

$$b=2\varepsilon(\gamma+\delta)$$

$$c=2\gamma\delta$$

$$d=1+\alpha^2+\beta^2$$

$$e=2\alpha(1+\beta)$$

$$f=2\beta$$

hence

$$|H(e^{j\omega T})|_{max} = \max\{|H(1)|, |H(-1)|, |H(e^{j\omega_m T})|\}$$

These formulas in conjunction with (3.1), (3.2), (3.3) and Table 3.7 provide an analytical and straightforward dynamic range scaling procedure.

3.6.2 Spread and Total Capacitance Scaling

Typically, the capacitance scaling discussed in the last subsection is going to modify the total capacitance and the capacitance spread needed for a given realization. The next step in the design process in then to adjust these two quantities to their minimum values without affecting the already established network characteristics. There are basically two procedures to perform this last element scaling. The first approach is simply to scale all the network elements so that the minimum capacitance value in the network becomes unity. We assume here, for normalization purposes, the unit capacitance as the minimum capacitance value that can be implemented using a given technology.

The second approach is to scale separately different groups of capacitors. The capacitors in each group are identified, as discussed in section 3.4 by the virtual ground to which they are connected. Since these groups can be independently scaled, a minimum capacitance (with unity value) can be defined for each group.

In general, the second approach is optimal (leads to minimum spread and total capacitance) whenever it is

possible to identify the different groups of capacitors. It is important to note, however, that this approach cannot be applied if a given capacitor terminal is switched to virtual grounds of two distinct OAs in different phases (e.g. capacitor F in PTFF). From Table 3.2 one can readily verify that the nine networks marked with an asterisk cannot be scaled by following the second approach. Nevertheless, such networks should not be diregarded since they still may result in the best design for a given case.

3.7 APPLICATIONS

All networks proposed so far can realize any biquadratic z-domain voltage transfer function. Therefore, performance criteria such as total capacitance, capacitance spread and sensitivity among others will determine the recommended circuit for a given application. In practice, these values depend on factors such as the type of transfer function, the pole Q, the gain constant and the sampling rate employed. In order to illustrate the possibility of design improvement using the new networks proposed, we give here two examples where a reduction in the area required for integration may be achieved. The examples are presented in Table 3.8 where the best design obtained from all networks in Table 3.2 is compared with the best result among the structures previously reported. The figure of merit used for this comparison was the sum of the normalized total capacitance and the component spread (C_{max}/C_{min}). Maximum

Table 3.8: Examples of design improvement.

	NETWORK	C_T	SPREAD	NUMBER OF CAPACITORS
Ex.1 - HPN f_p = 2.5kHz Q_p = 2 f_z = 2.0kHz f_s = 250kHz high freq. gain = 1	ACR/2	33.3	21.7	8
	AUE	72.5	28.1	7
Ex.2 - LPN f_p = 2.0kHz Q_p = 10 f_z = 2.5kHz f_s = 12.5kHz DC gain = 1	PFF	33.9	11.5	6
	ACF	34.9	11.5	7

dynamic range was also considered as a requirement.

Example 1 is a highpass notch (HPN) section. The final network is shown in Fig. 3.6. In this design, the CSN of type 11 (Table 3.1) has been employed twice to combine elements from the feedback loop (capacitors C and R) with the feedforward capacitors G and H, as anticipated in section 3.4. The use of such combination has led to a reduction in the total capacitance necessary for the realization. Also, it is clear that this final network could not have been obtained by starting with network ARU. As a matter of fact, in ARU the output voltage V_2 is not even S/H. Substantial improvements in the total capacitance (53%) and in the capacitance spread (21.8%) are obtained at the expense of an increase in the network sensitivity (Table 3.3). However, due to the high capacitance ratio accuracy obtainable in MOS circuits, this is not a major drawback. In fact, a Monte Carlo simulation, considering capacitance ratio tolerances of $\pm 0.1\%$ (Gaussian distribution) shows maximum variations of 0.62% (σ = standard deviation = 5.14Hz) in ω_o and 0.69% ($\sigma = 0.0064$) in Q. Therefore, the frequency performance of the filter should lie within practically acceptable limits. Clearly, in this case, the use of one more capacitor will not overcome the advantages obtained by the total capacitance minimization.

In example 2 we illustrate the use of canonical structures. Since both realizations present about the same

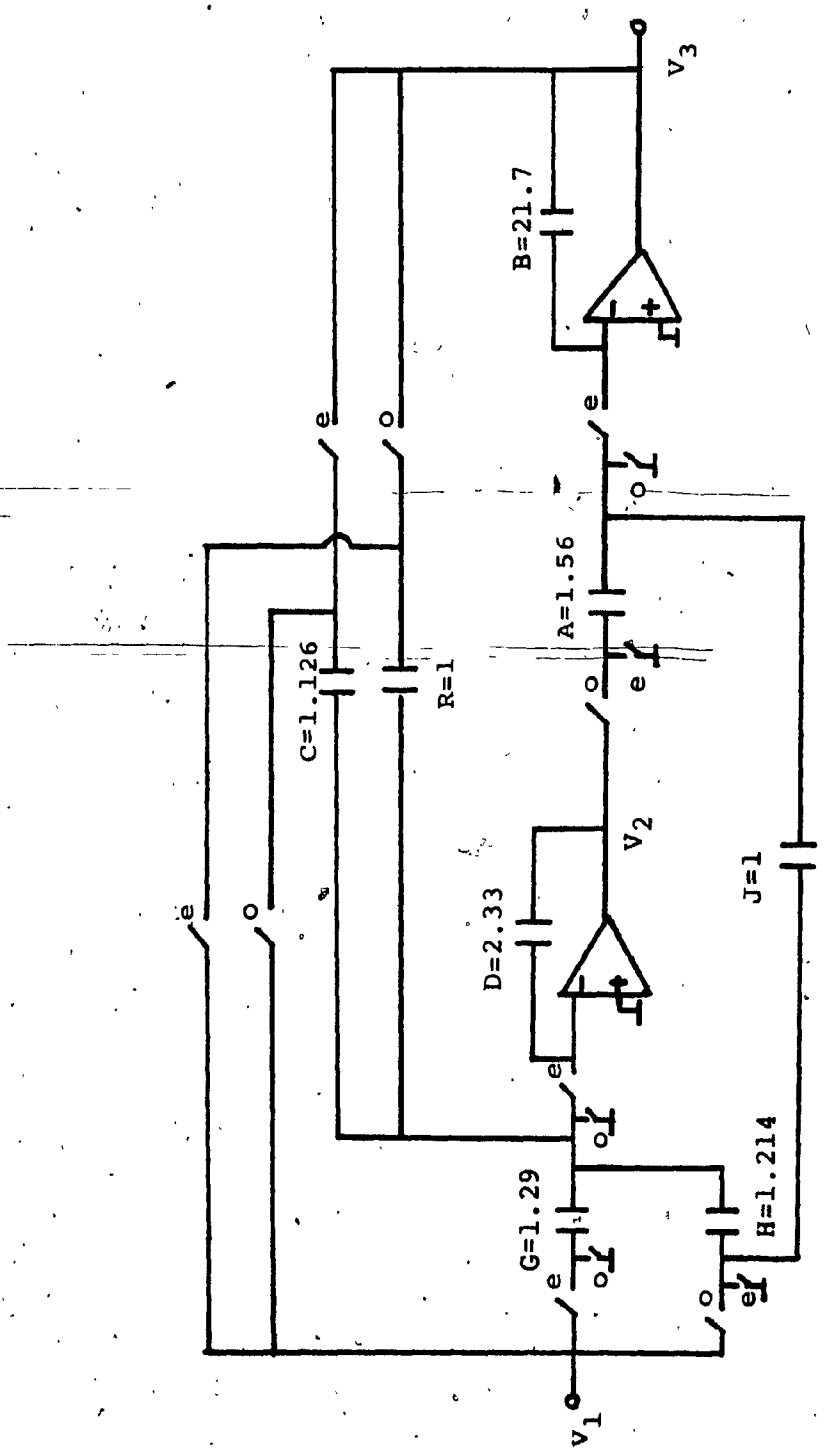


Figure 3.6: Example 1 (HPN)

total capacitance, spread and sensitivity, the implementation employing fewer capacitors should be preferred. This choice would decrease the area required for interconnections within the chip. Example 2 is discussed in more details in the next section.

3.8 EXPERIMENTAL RESULTS

In order to verify the theoretical results, most of the networks proposed in this chapter were constructed in discrete form to realize several different transfer functions. In all cases the experimental results agree closely with the theoretical predictions. However, in order to preserve space, only one example is presented in detail.

The lowpass notch filter (LPN) of example 2 has the prewarped bilinearly transformed z-domain transfer function

$$H(z) = \frac{0.6445473083905(1 - 0.6180339885z^{-1} + z^{-2})}{1 - 1.028244799797z^{-1} + 0.91898727228363z^{-2}}$$

The final realization of the network PFF (biquad no.30 in Table 3.2) is shown in Fig. 3.7.

Also, it should be noted that since capacitors I and J are equal, they can be substituted by an unswitched capacitor. This simplification is equivalent to the replacement of CSNs of types 1 and 3 by a CSN of type 5 (see Table 3.1). Consequently, the LPN filter can be realized

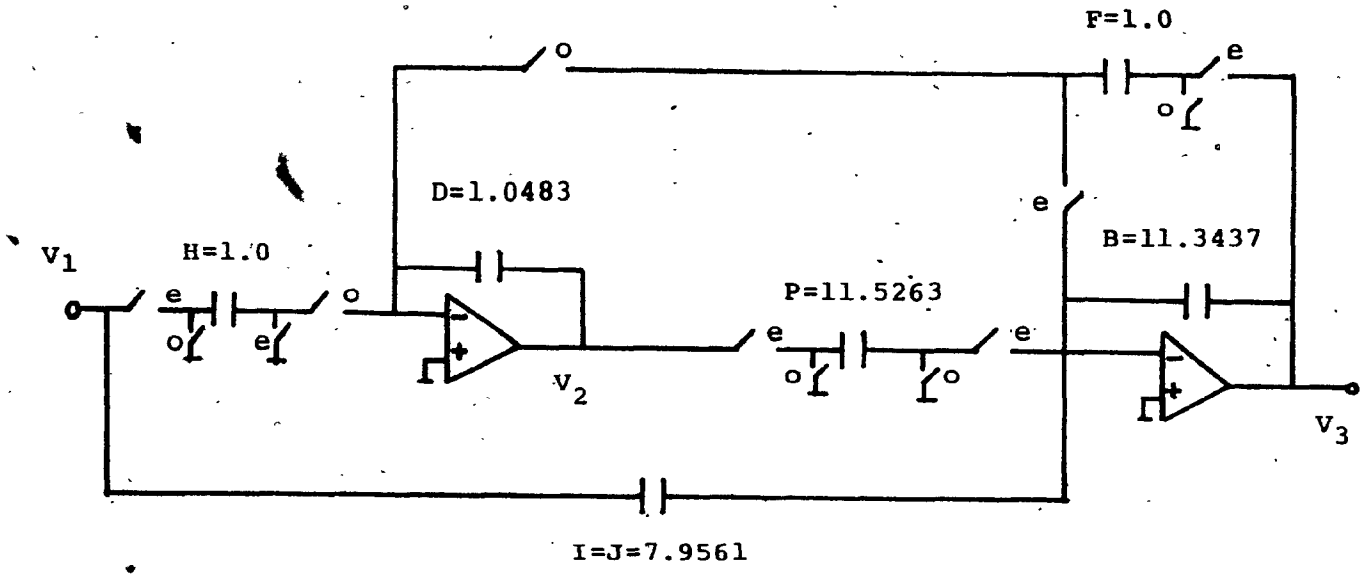


Figure 3.7: Lowpass notch filter (PFF). Capacitance values in nanofarads. Transfer function $H(z)=V_3^e/V_1^e$.

using only 6 capacitors and with better performance than the 7 capacitor version since now the transfer function coefficients γ and δ are exactly equal due to the perfect matching of capacitors I and J. As mentioned in subsection 3.6.2, even though network PFF cannot be scaled for minimum total capacitance by independently scaling different groups of capacitors, it has yielded the design with the smallest total capacitance. The theoretical frequency response and the experimental measurements are presented in Fig. 3.8 which shows a close agreement between theory and practical results.

The laboratory tests were performed using LF347 OAs and MC14066B MOS analog switches. Capacitors of 2% tolerance with respect to their nominal values were chosen and no tuning was used. The clock was generated by a TTL circuitry and the sample and hold input circuit was the same employed in [45- Fig 3.4(a)].

3.9 SUMMARY

A systematic method of generating stray insensitive biquadratic SC networks has been presented. Towards this end, the conditions for parasitic insensitivity reported earlier in the literature are exploited. The proposed method is employed to generate biquads with about the lowest necessary number of capacitors (at most 8) for general transfer function realizations. As a consequence, 23 new

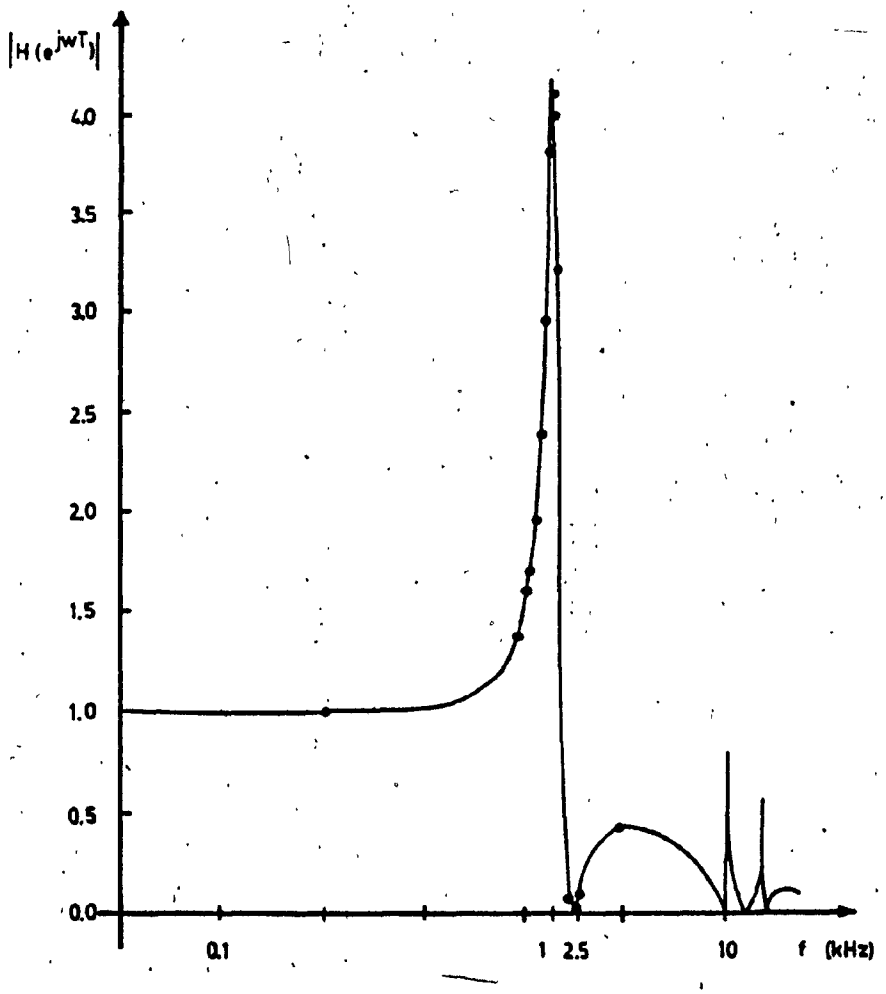


Figure 3.8: Experimental results.

(—) Theoretical.

(●) Measured.

general biquads as well as the five presented so far in the literature have been obtained. Some of the new structures have subnetworks which are canonic with respect to the number of capacitors and are, themselves, general biquads. This permits, in some cases where dynamic range, total capacitance and/or capacitance spread properties are acceptable, further reduction in the number of capacitors necessary to realize a biquadratic transfer function. The biquads obtained are completely interchangeable and input-output compatible. These properties make them a valuable tool, attractive for use as a network library in a general computer-aided design and optimization package [40].

Detailed analysis and design procedures for the biquads have been provided.

The possibility of design improvement by using the novel structures has been illustrated by means of examples. Extensive experimental tests have been conducted on most of the proposed networks. In all cases, the test results agree closely with the theoretical predictions.

So far, the number of elements allowed in the network has been limited so that easy to design structures could be obtained. It would be interesting, however, to investigate the possibilities of design improvement if the number of capacitors is no longer limited by considerations of design complexity. In the next chapter, an optimization

algorithm is developed which allows the designer to rationally use the degrees of freedom available in the most general stray insensitive SC network with a given number of OAs leading to structures with reduced total capacitance and component spread.

CHAPTER IV

OPTIMIZATION OF SC BIQUADS

4.1 INTRODUCTION

In the last two chapters, canonic or quasi-canonic networks were sought for the realization of SC networks. This is a natural approach if one is looking for a design procedure which can be carried out with pencil and paper. Canonic structures usually lead to economical and practical realizations. However, in MOS integrated circuit implementations the total capacitance is more directly associated with the area needed for integration than the number of capacitors employed. Therefore, it is desirable to investigate the possibility of improving the final realization in some sense by allowing more capacitors in the network. Since increasing the number of network elements will increase the number of degrees of freedom in the design, most probably some performance measure can be improved if more elements are used. However, the price paid for such improvement is the necessity of more complex design tools, usually involving optimization techniques [46,47,58].

In this chapter a new technique is proposed to optimize the design of SC networks. The technique seeks to minimize the total capacitance and spread necessary, for a given transfer function, in the resulting SC network. Even though the proposed method can be extended to structures of

any order, its development is presented here for the particular case of second order networks. The technique can also be applied, in a straightforward manner, to the design of single OA networks. Since any transfer function can be realized by combining first and second order building blocks, the method, in its present form, can be regarded as quite general.

4.2 OPTIMIZATION OF SC BIQUADS

In optimizing the design of SC biquads, the main objective will be the minimization of the total capacitance required for a given realization (transfer function). Such objective has been chosen due to the close relationship between total capacitance and the area needed for integration.

Some methods using numerical optimization techniques and/or tradeoff curves have recently been proposed in the literature [46,47,58]. Most of them consider a previously established structure with a fixed number of components. Others start from a large network and seek to minimize the number of elements by numerically generating a series of continuously equivalent networks [47]. Each newly obtained structure has one component less than the previous one. Then, for each element elimination, a complete numerical optimization procedure is applied.

It would be interesting to have a method which to avoids the necessity of a fixed structure while, at the same time, possessing the capability of generating networks of a manageable size without requiring excessive computer time. It also appears desirable that the degrees of freedom inherent to the most general stray insensitive biquad (120 capacitors) determined in Chapter III be available to the designer.

However, any attempt at optimizing this general biquad directly, by numerical methods, will lead to several difficulties, such as:

(a) an excessively large number of variables. It is not practical to use 120 variables in the process of optimizing a single second order network.

(b) since for SC networks all the transfer function coefficients are dependent only upon capacitance ratios, any realization could be arbitrarily scaled down to decrease the total capacitance. Therefore, the technological limit for the minimum capacitance value (say $C_{min}=1$) has to be included in the optimization process. This consideration introduces a major difficulty in numerical optimizations if one does not want to fix the network topology a priori. A condition such as

$$C_i \geq 1 \text{ or } C_i = 0$$

cannot be easily implemented in a continuous optimization process. Therefore, a numerical optimization applied directly to the general biquad (with $C_i \geq 1$) would lead to full networks [46] since it will not be possible to eliminate any element. Then, if a 120 capacitor network is used, the optimized network will employ all the 120 capacitors.

In the optimization of RC-active networks, the theory of equivalence transformations such as the Howitt transformation has been successfully used to reduce the number of variables [48]. However, in order to keep the number of elements at a reasonable count, some optimization variables are usually forced to be zero. This is done either in an arbitrary manner or by evaluating analytically the transformed network matrix in order to determine a new set of equality constraints to be incorporated into the optimization problem. Furthermore, a necessary step in the generation of equivalent networks is to determine the new element values for the transformed network from a given, say, nodal admittance matrix. However, in the case of SC networks, such determination of the element values from the entries of the admittance matrix is not unique due to the time-varying nature of the circuit. In the analysis process, a switch closed in a given phase results in the contraction (addition) of two rows and two columns of the network admittance matrix [13]. The interpretation of such

a contraction in the reverse direction (design) is not, however, unique [47,49].

On the other hand, the concepts of CSN and CSN equivalences introduced in the previous chapters allow the optimization to be performed by parts. By doing so, at each optimization step a reduced number of variables is required and, at the end, the number of elements in the optimized network has an upper bound which is ususally quite acceptable for practical purposes.

In what follows it is assumed for convenience (as done in Chapter III) that the output signal of the biquad is required to be sampled and held (S/H) over a full clock period.

The optimization method proposed here [60] is subdivided into two independent steps, namely:

(1) Start with the network consisting of only the capacitors whose CSNs are among the four basic ones (types 1, 2, 3 and 4 in Table 3.1). Also, the S/H output requirement is imposed. Hence, the starting network is the one in Fig. 3.5 with K=O=W=Q=Z=QQ=ZZ=0, as shown in Fig. 4.1. Recall that by using only these four basic CSNs, one has the maximum degree of freedom in choosing the numerical values of the coefficients of the network CCEs. The total capacitance of such a network is then minimized with the transfer function coefficients used as equality

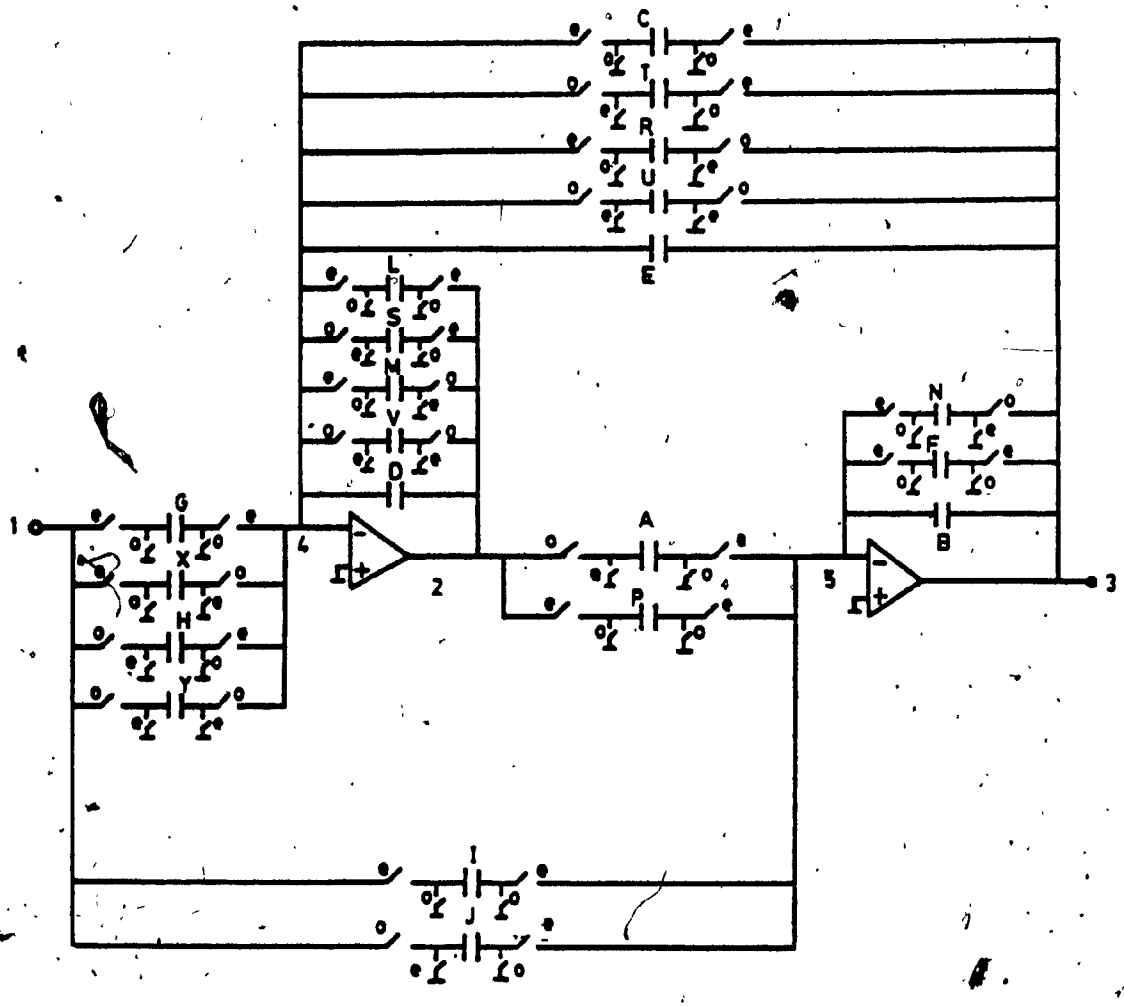


Figure 4.1: General biquad with sampled and held output at node 3.

constraints [50]. This step will determine the best way to distribute numerically the coefficients of the CCEs in order to obtain a reduced total capacitance.

(2) Apply the remaining CSNs to the optimized biquad. The new CSNs are employed in order to decrease the total capacitance (and most of the times the spread and the number of capacitors) necessary to realize the numerical values determined in step (1) for the coefficients of the CCEs.

This method has been found to have the following features:

(i) Leads to networks with reasonably few components.
(ii) Few and easy to handle constraints in the numerical optimization.
(iii) Few optimization variables (≤ 20).
(iv) Reasonable computational times for optimizations with a variable structure.
(v) The designer always deals with a network of manageable size.

4.3 STEP I - NUMERICAL OPTIMIZATION

Using the network in Fig. 4.1, for a given set of transfer function coefficients γ, ε, δ, α and β, the problem can be stated as follows:

minimize

$$\sum_{i=1}^{20} x_i, \quad x_i = \text{value of the ith capacitance} \qquad (4.1)$$

subject to:

(a) Equality constraints given by the analytical expressions for the transfer function coefficients.

(b) inequality constraints*:

$$x_i \geq 1 \qquad i=1,\ldots,20,\ i \neq p,c \tag{4.2}$$

$$\text{if } C=x_c=0, \text{ make } 0 \leq x_c \leq 10^{-8} \text{ and } x_p \geq 1 \tag{4.3}$$

$$\text{if } P=x_p=0, \text{ make } 0 \leq x_p \leq 10^{-8} \text{ and } x_c \geq 1 \tag{4.4}$$

This optimization procedure leads to a network with reduced total capacitance and employing at most 19 capacitors.

4.3.1 Modifications on the Basic Algorithm

So far, we have been solely concerned with the minimization of the total capacitance required to realize a given second order transfer function. Though this will be always our main objective, it is desirable, if possible, to take into account some other network performance measures during the optimization process.

It is known that, in general, total capacitance and network sensitivity minimizations are competing objectives [58]. If some improvement is obtained in the total capacitance required for a given realization, the price that

(*)Here, as previously, capacitors P and C are not allowed to appear in the same network for stability reasons.

is usually paid is a corresponding increase in the network sensitivities to element variations. Consequently, any realistic design should, somehow, take into account these sensitivities. Another aspect which is not as crucial as the sensitivity but should not be completely diregarded is the dynamic range of the network. Usually, for practical purposes (specially in signal filtering applications), maximum dynamic range is not absolutely necessary. However, if the maximum signal levels at the outputs of the different OAs in a SC network are severely mismatched, the usefulness of the network might be affected. Hence, the basic algorithm proposed in the last section should be modified to account for the network sensitivities as well as dynamic range control. The modifications are included as follows:

(a) The Sensitivity Measure

Following the approach used in Chapter III, the ω_o and Q sensitivities are used as figures of merit to determine the network sensitivity performance. Also, the bilinear transformation is used to obtain the discrete transfer function H(z) from the analog counterpart. The reasons for using the bilinear transformation were mentioned in Chapter III.

Recall that, for a H(z) of the form

$$H(z) = \frac{\gamma + \varepsilon z^{-1} + \delta z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}} \qquad (4.5)$$

the application of the inverse bilinear transformation yields

$$f_o = \left(\frac{\omega_o T}{2}\right)^2 = \frac{1 + \alpha + \beta}{1 - \alpha + \beta} \tag{4.6}$$

and

$$f_b = \frac{\omega_b T}{4} = \frac{1 - \beta}{1 - \alpha + \beta} \tag{4.7}$$

Consequently,

$$S_x^{\omega_o} = \frac{1}{2} S_x^{f_o} \text{ and } S_x^{\omega_b} = S_x^{f_b} \tag{4.8}$$

where x stands for any network element.

These sensitivities can be written as [51].

$$S_x^{f_o} = S_\alpha^{f_o} S_x^\alpha + S_\beta^{f_o} S_x^\beta \tag{4.9}$$

$$S_x^{f_b} = S_\alpha^{f_b} S_x^\alpha + S_\beta^{f_b} S_x^\beta \tag{4.10}$$

which, after some algebraic manipulation yield

$$S_x^{f_o} = \frac{2x}{(1-\alpha+\beta)(1+\alpha+\beta)} \left[(1+\beta) \frac{\partial \alpha}{\partial x} - \alpha \frac{\partial \beta}{\partial x}\right] \tag{4.11}$$

$$S_x^{f_b} = \frac{x}{(1-\beta)(1-\alpha+\beta)} \left[(1-\beta) \frac{\partial \alpha}{\partial x} + (\alpha-2) \frac{\partial \beta}{\partial x}\right] \tag{4.12}$$

Since the values of α and β are constants determined by the desired transfer function, the sensitivity function

$$f_{sens} = \sum_{k\ 1}^{20} \{ |(1+\alpha+\beta)(1-\alpha+\beta) S_{x_k}^{\omega_o}| + |(1-\beta)(1-\alpha+\beta) S_{x_k}^{\omega_b}| \} \tag{4.13}$$

or, equivalently,

$$f_{sens} = \sum_{k\ 1}^{20} \{ |x_k| [|(1+\beta) \frac{\partial \alpha}{\partial x_k} - \alpha \frac{\partial \beta}{\partial x_k}| + |(1-\beta) \frac{\partial \alpha}{\partial x_k} + (\alpha-2) \frac{\partial \beta}{\partial x_k}|] \} \tag{4.14}$$

should provide a good measure for the sensitivity performance of the network.

(b) Dynamic Range Scaling

In the general biquad of Fig. 4.1, the voltage at node 2 is not guaranteed to have a sampled and held waveform. Therefore, in general, the maximum amplitudes for V_2^e and V_2^o should be assumed independent of each other. This assumption makes the dynamic range scaling a very difficult task. However, it has been verified by various examples that most of the times, (and independently of the sampling rate employed), these maxima are reasonably close to each other. Hence, in this optimization a technique is employed which usually leads to good practical results in dynamic range scaling.

Let us compare the peak amplitude of V_2^e with the peak amplitude of V_3^e. The transfer functions from the input to both outputs can be written as

$$H_1(z) = \frac{N_1(z)}{D(z)} = \frac{V_3^e(z)}{V_1^e(z)} = \frac{\gamma_1 + \varepsilon_1 z^{-1} + \delta_1 z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}} \qquad (4.15)$$

and

$$H_2(z) = \frac{N_2(z)}{D(z)} = \frac{V_2^e(z)}{V_1^e(z)} = \frac{\gamma_2 + \varepsilon_2 z^{-1} + \delta_2 z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}} \qquad (4.16)$$

Then

$$\left|\frac{V_2^e}{V_3^e}\right|^2 = \left|\frac{\gamma_2 + \varepsilon_2 z^{-1} + \delta_2 z^{-2}}{\gamma_1 + \varepsilon_1 z^{-1} + \delta_1 z^{-2}}\right|^2 \qquad (4.17)$$

For most second order transfer functions, if the pole's Q-factor is larger or equal to 5, the maximum value of the magnitude function occurs at a frequency close to the pole frequency* [52]. This is not true only in the case of a frequency rejection network (with finite Q for the zero). In this case the maximum will be given by the magnitude at DC and the algorithm can be easily adapted. Hence, for

(*)In practice, such assumption usually leads to good results even for Q factors close to one.

practical purposes, it is reasonable to compare the amplitudes at the pole frequency. We therefore include two more inequality constraints in the optimization problem (4.1) in order to guarantee the conditions

$$K_2 \leq \left| \frac{V_2^e(e^{j\omega_o T})}{V_3^e(e^{j\omega_o T})} \right|^2 \leq K_1 \tag{4.18}$$

where K_1 and K_2 are parameters chosen by the designer. For designs using the bilinear transformation, the value of ω_o is the actually desired value (not prewarped) in the analog transfer function if prewarping was employed to obtain $H(z)$. Otherwise, one should use the modified value $(2/T)\tan^{-1}(\omega_o T/2)$ for ω_o [25,26]. The two constraints are then given by

$$|N_2^e(\omega_o)|^2 \leq K_1 |N_1^e(\omega_o)|^2 \tag{4.19}$$

and

$$|N_2^e(\omega_o)|^2 \geq K_2 |N_1^e(\omega_o)|^2 \tag{4.20}$$

where

$$|N_i^e(\omega_o)|^2 = (\gamma_i^2+\varepsilon_i^2+\delta_i^2) + 2\varepsilon_i(\gamma_i+\delta_i)\cos\omega_o T + 2\gamma_i\delta_i\cos(2\omega_o T) \quad (4.21)$$

for i=1,2 and T=sampling period.

4.3.2 Multiple Criteria Optimization (MCO)

We now describe the modified algorithm which is actually used in the numerical optimization procedure. The complete expressions for the constraints and their derivatives are presented in the appendix at the end of the chapter. The basic algorithm dicussed in section 4.3.1 has been modified as follows:

(a) Objective Function: The new objective function is given by

$$f_{opt} = w_1 f_{cap} + w_2 f_{sens} \quad (4.22)$$

where w_1 and w_2 are arbitrary weigths, f_{cap} is given by (4.1) and f_{sens} by (4.14).

(b) New Constraints: The constraints given by (4.19) and (4.20), as per eq. (4.21), are added to control the network's dynamic range.

The modified objective function transforms the simple initial optimization problem into a Multiple Criteria Optimization (MCO) problem. This is because total capacitance and network sensitivity are competing

minimization objectives.

The minimization of f_{opt} as in (4.22) subject to equality and inequality constraints characterizes a weigthed sum MCO problem. To proceed further, it is useful to recall some definitions commonly used in the MCO literature [53,54]. Henceforth, a bar is used below letters representing vectors in order to indicate their multidimensional nature. Our MCO problem can be stated as

minimize

$$\underline{f}(\underline{x}) = (f_{cap}(\underline{x}),\ f_{sens}(\underline{x})) \qquad (4.23)$$

subject to $\underline{g}(\underline{x}) \geq 0$ (inequality constraints)

and $\underline{h}(\underline{x}) = 0$ (equality constraints)

where $\underline{x}=(x_1, x_2, \ldots, x_{20})$ is the vector of designable parameters (capacitance values). The following definitions then apply [53]:

Definition 1: The "feasible region", Ω, in the parameter space is the set of all designable parameters that satisfy the constraints.

Definition 2: The "feasible region" in the objective function space is the image by $\underline{f}$ of the feasible region in the parameter space.

Definition 3: A point $\underline{x}^* \in \Omega$ is a local noninferior point if and only if for some neighborhood of $\underline{x}^*$ there does not exist a $\Delta\underline{x}$ such as $(\underline{x}^*+\Delta\underline{x}) \in \Omega$ and

$$f_i(\underline{x}^* + \Delta\underline{x}) \leq f_i(\underline{x}^*) \quad , \quad i=\text{cap, sens}$$

and

$$f_j(\underline{x}^* + \Delta\underline{x}) < f_j(\underline{x}^*) \quad , \quad \text{for some } j$$

In general, there are an infinite number of noninferior points for a given MCO problem. The collection of noninferior points is the noninferior set. The image of the noninferior set by $\underline{f}$ is called the noninferior solution set or the tradeoff surface. Note that a noninferior point is the same as an optimum tradeoff solution. A design is noninferior if an improvement in any objective function requires a degradation in at least one of the other objectives.

As mentioned before, we have chosen to use the weighted sum method to convert the MCO problem (4.23) into the scalar objective function problem (4.22). The next problem is how to choose the weights w_1 and w_2 in order to achieve good tradeoff points in an efficient manner. Since in our case there are only two competing objective functions, a very simple weight selection heuristic can be chosen [53,54].

We first minimize each objective function separately in order to find the boundaries of the noninferior surface in the objective function space (points $\underline{f}_1^*$ and $\underline{f}_2^*$ in Fig. 4.2). Then, these points are used to define a straight line (in general a plane) in the objective function space by solving the following set of equations in w_1 and w_2 [53,54]:

$$w_1 f_{cap}^1 + w_2 f_{sens}^1 = 1$$

$$w_1 f_{cap}^2 + w_2 f_{sens}^2 = 1 \qquad (4.24)$$

The straight line determined by this set of equations and the noninferior solution $\underline{f}_3^*$ found by using these weights, are shown in Fig. 4.2. Such a solution is found by numerically optimizing (4.22) with the values of w_1 and w_2 given by the solution of (4.24).

Now if one wishes, for instance, to determine another noninferior solution with smaller f_{cap}, the set of equations given by $\underline{f}_3^*$ and $\underline{f}_2^*$ is solved to determine the new set of weights. On the other hand $\underline{f}_1^*$ and $\underline{f}_3^*$ should be used to further decrease f_{sens}. This process continues until a tradeoff point is obtained which is satisfactory from the designer's point of view.

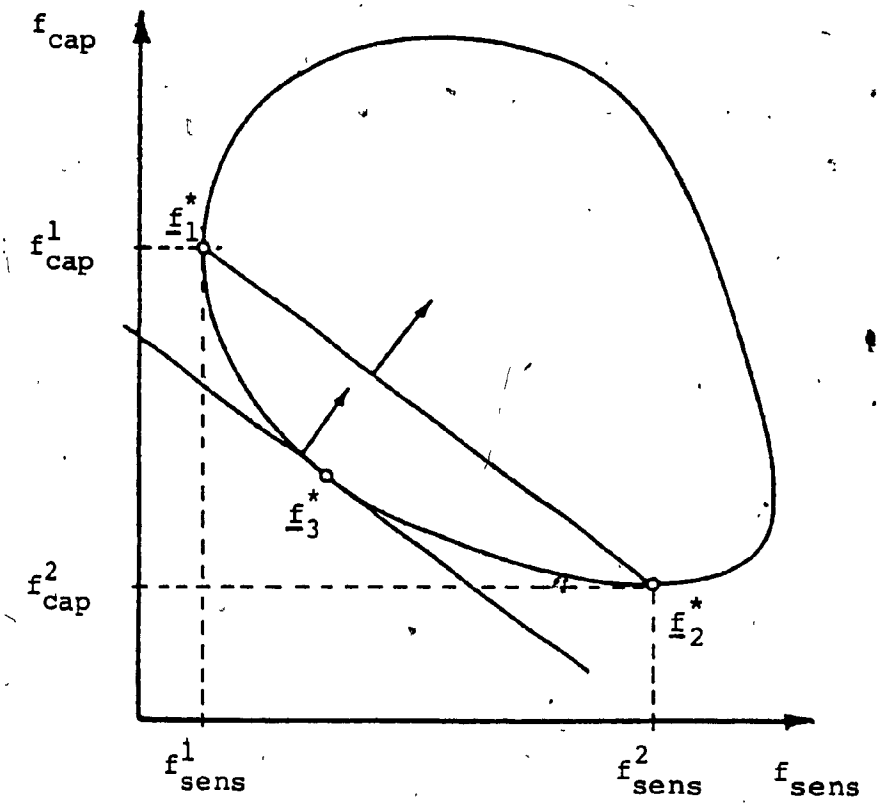


Figure 4.2: Multiple criteria optimization strategy.

4.4 STEP II - USE OF THE REMAINING CSNs

At this point of the optimization process we have a SC biquad with 19 capacitors (Fig. 4.1), reduced total capacitance and acceptable sensitivity and dynamic range. The next step is to use the extra degrees of freedom given by the remaining elements of the general biquad (120 capacitors) in order to further improve the present design. This can be done by using the CSNs of types 5 to 16 in Table 3.1. Such a procedure was briefly discussed in Chapters II and III. In this chapter the idea is going to be used in the same way it was presented in Chapter II. However, single OA networks employ only part of the CSNs in Table 3.1 and the natural simplicity of the resulting networks required no further formalization of the method. In Chapter III, on the other hand, the CSN equivalences were used only analytically in order to obtain new structures for the realization of a general second order transfer function. It was of no concern at that time if the use of these equivalences would lead to a reduced total capacitance or component spread. Also, only one or two equivalences could be used in each network due to the reduced number of components and no generalization was necessary. Only in the examples at the end of the chapter, the use of equivalent CSNs to improve the final implementation was hinted. Now, since the complete network in Fig. 4.1 is being used, all possible CSN combinations must be determined. Also, one

should know a priori how much can be gained in total capacitance by the application of a particular CSN equivalence and what is happening with the network sensitivities when the modifications in the structure are performed.

Hence, in what follows, a generalization of the use of the CSN equivalences and their application to reduce the total capacitance of the network is presented. The method can be applied to any network derived from the general parasitic insensitive biquad with 120 capacitors.

4.4.1 Generalization of the CSN Equivalences

Consider the CSNs shown in Table 3.1. This is the complete set of possible CSNs in a stray insensitive SC biquad according to the parasitic insensitivity conditions discussed in Chapter I [14].

Suppose that we have a network (such as in Fig. 4.1) which contains only switched capacitors with CSNs of types 1, 2, 3 and 4. We wish to determine how the CSNs 5 through 16 in Table 3.1 can be employed to substitute combinations of these four basic CSNs. By inspection of the contributions of such CSNs to the network CCEs in Table 3.1 one can easily determine the equivalent sets shown in Table 4.1, where C_i stands for a capacitor with CSN of type i. Each of these sets can be substituted by a single CSN as listed in the first column of Table 4.1 if the values of all

Table 4.1: Equivalent sets of CSNs for a general biquad.

		EQUIVALENT SETS	
	CSN	not S/H V-node	S/H
same V-node, same I-node	C_5	C_1, C_2, C_3, C_4	C_1, C_3
	C_6	C_1, C_3	C_1, C_3
	C_7	C_2, C_4	---(*)
	C_8	C_1, C_2	same
	C_9	C_3, C_4	same
diff V-nodes, same I-node	C_{10}	C_1, C_2 (V-node A) C_3, C_4 (V-node B)	same
	C_{11}	C_1 (V-node A) C_3 (V-node B)	same
	C_{12}	C_2 (V-node A) C_4 (V-node B)	same
same V-node, diff I-nodes	C_{13}	C_1, C_3 (I-node a) C_2, C_4 (I-node b).	same
	C_{14}	C_1 (I-node a) C_2 (I-node b).	same
	C_{15}	C_3 (I-node a) C_4 (I-node b)	same
diff V-nodes, diff I-nodes	C_{16}	V_A -[ ]- I_a → C_1 V_A -[ ]- I_b → C_2 V_B -[ ]- I_a → C_3 V_B -[ ]- I_b → C_4	same

(*) If the capacitors are not equal in value, drop the smallest one and make the other equal to the difference.

capacitances in the set are equal. If this is not the case, still the capacitor set may be substituted by another set with at most the same number of elements but with reduced total capacitance, as explained below.

Suppose that C_a has an equivalent set composed by C_b and C_c. Then, whenever C_b and C_c appear in the network they can be substituted by equivalent CSNs in one of the following ways:

(a) if $C_b=C_c$, substitute the set by $C_a=C_b=C_c$.
(b) if $C_b>C_c$, substitute the set by $C_a=C_c$ and $\hat{C}_b=C_b-C_c$.
(c) if $C_c>C_b$, substitute the set by $C_a=C_b$ and $\hat{C}_c=C_c-C_b$.

At this point an illustrative example would be instructive. Consider the SC network shown in Fig. 4.3(a). Capacitor C_b has CSN of type 1 and capacitor C_c has CSN of type 2. According to Table 4.1, they form a set which would be exactly equivalent to a CSN of type 8 if they were numerically equal. Even though C_b and C_c are numerically distinct, the CSN of type 8 can still be used to reduce both the spread and the total capacitance of the network. Since $C_c>C_b$ (option c above) we substitute C_b by a capacitance C_a of the same value but with CSN of type 8 (see Table 3.1). Also, C_c is replaced by $\hat{C}_c$ with the same CSN but with a numerical value equal to the difference C_c-C_b (Fig. 4.3(b)). Note that now C_a is equivalent to a CSN of type 1 and a CSN of type 2, both with unity capacitances. Therefore, $\hat{C}_c$ is

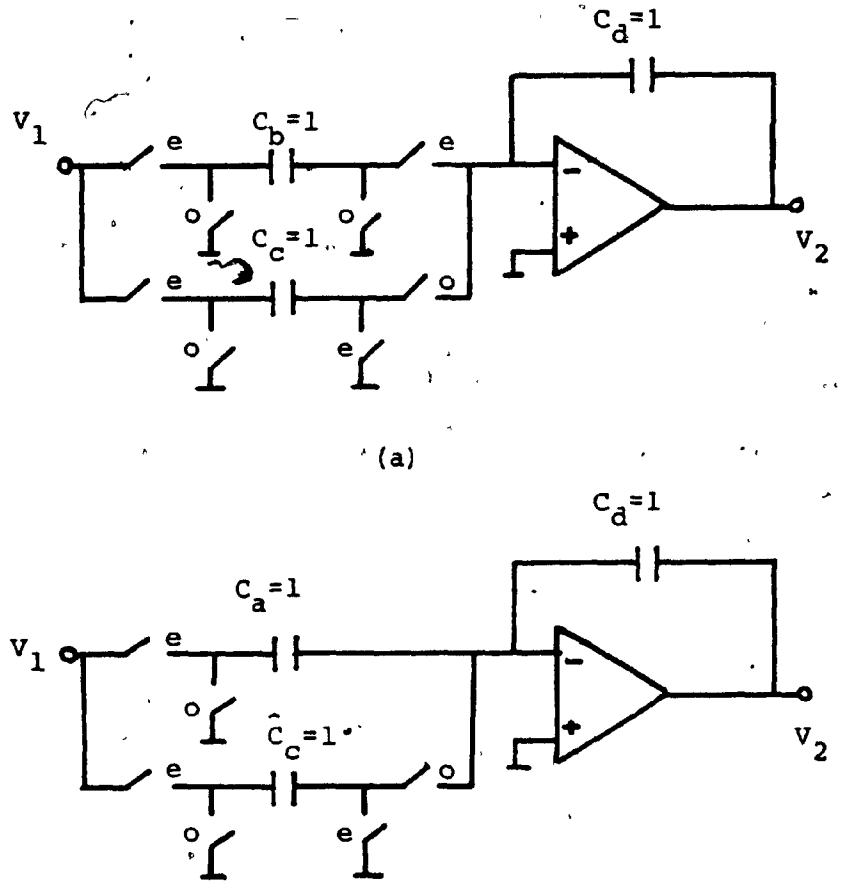


Figure 4.3: Illustrative example.

(a) Initial network.

(b) Network modified by CSN equivalences.

necessary only to complete the contribution given by C_c in Fig. 4.3(a) to the CCE evaluated at the virtual ground. Both networks can be easily verified to have exactly the same CCEs. However, network (b) is clearly a better design in terms of total capacitance and element spread.

The procedure just presented guarantees that:

(i) The network equations (CCEs) remain unchanged.
(ii) All capacitance values remain greater or equal to zero after the modification is performed.

Nevertheless, in order to improve the final design according to our main objective function (total capacitance), we must guarantee that the total sum of capacitor values is reduced after the new capacitors have been scaled so that $C_{min}=1$, i.e., the normalized value of the minimum capacitance allowed by the technology. Since the CSNs can be combined either 2 at a time or 4 at a time, only these two cases have to be studied, as follows.

(1) Case 1 - Combination of 2 CSNs

Let $C_1,C_2,C_3,\ldots,C_n$, $C_i \geq 1$ for all i, be the capacitors of one stage of the biquad if the 2 stages can be scaled separately or, otherwise, the capacitors of the complete network. Let (C_1,C_2) be a set of capacitors whose CSNs can be combined. Also, suppose without any loss of generality, that $C_1>C_2$. The total capacitance C_T of the

initial network is given by

$$C_T = C_1 + C_2 + C_3 + \ldots + C_n \tag{4.25}$$

After the network transformation, the new values for C_1 and C_2 will be

$$\hat{C}_1 = C_1 - C_2 \quad \text{(with the same CSN)}$$

$$\hat{C}_2 = C_2 \quad \text{(with a different CSN)} \tag{4.26}$$

Then, depending on the numerical values of C_1 and C_2, three distinct types of transformation may be performed, namely:

Transformation type 1: If $C_1=C_2$.
Then the new total capacitance $\hat{C}_T$ will be given by

$$\hat{C}_T = C_2 + C_3 + \ldots + C_n = C_T - C_1 \tag{4.27}$$

and the total capacitance is reduced as well as the number of capacitors in the network ($\hat{C}_1=0$).

Transformation type 2: If $C_1-C_2 \geq 1$.
Then

$$\hat{C}_T = (C_1 - C_2) + C_2 + C_3 + \ldots + C_n = C_T - C_2 \qquad (4.28)$$

and again the total capacitance is reduced. The number of elements, however, remains unchanged.

Transformation type 3: If $0<C_1-C_2<1$.

In this case all capacitor values must be scaled so that $C_{min}=1$. Then

$$\hat{C}_T = \frac{1}{C_1-C_2}(C_1 - C_2 + C_2 + C_3 + \ldots + C_n) \qquad (4.29)$$

or

$$\hat{C}_T = \frac{C_T - C_2}{C_1 - C_2} \qquad (4.30)$$

Hence, the total capacitance will be reduced only if

$$C_1 - C_2 > 1 - \frac{C_2}{C_T} \qquad (4.31)$$

The transformations of types 1 and 2 are usually preferable over the transformations of type 3 for the following two reasons reasons:

(i) They allow more reduction in total capacitance.

(ii) Each transformation of types 1 and 2 is completely independent of any other circuit modification. On the other hand, if a transformation of type 3 is performed, it modifies at least all capacitance values within the same stage (connected to the same virtual ground). Consequently, the effect (total capacitance reduction) of a subsequent transformation can only be determined after the first one is performed and the network elements re-scaled. Hence, if a given capacitor is involved in any one of the three types of transformation, types 1 and 2 should be given preference.

(2) Case 2 - Combination of 4 CSNs

Let (C_1,C_2,C_3,C_4) be a set of capacitors whose CSNs can be combined. Remember that $C_i \geq 1$, for all i, by hipothesis. Suppose, without any loss of generality, that $C_1 \geq C_2 \geq C_3 \geq C_4$. Then

$$C_T = C_1 + C_2 + C_3 + C_4 + C_5 + \ldots + C_n \tag{4.32}$$

and the new values of the four capacitors after the transformation will be

$$\begin{aligned} \hat{C}_1 &= C_1 - C_4 \\ \hat{C}_2 &= C_2 - C_4 \\ \hat{C}_3 &= C_3 - C_4 \\ \hat{C}_4 &= C_4 \end{aligned} \tag{4.33}$$

Again, depending on their numerical values, three types of

transformation are possible, namely:

Transformation type 1: If $C_1=C_2=C_3=C_4$.
Then

$$\hat{C}_T = C_4 + C_5 + \ldots + C_n = C_T - 3C_4 \qquad (4.34)$$

and the total capacitance as well as the number of capacitors are reduced ($\hat{C}_1=\hat{C}_2=\hat{C}_3=0$).

Transformation type 2: If $C_i-C_4\geq 1$ for some i=1, 2 or 3 and $C_i=C_4$ for the remaining capacitors in the set.
Then

$$\hat{C}_T = C_1 + C_2 + C_3 - 2C_4 + C_5 + \ldots + C_n = C_T-3C_4 \qquad (4.35)$$

and the total capacitance is reduced. The element count will be reduced by the number of capacitors among C_1, C_2 and C_3 which are equal to C_4.

Transformation type 3: If $0<C_i-C_4<1$ for some i=1,2 or 3.
Then, suppose that

$$C_1 - C_4 = \min\{C_1 - C_4, C_2 - C_4, C_3 - C_4\}$$

The new value of the total capacitance (after scaling) will be

$$\hat{C}_T = \frac{1}{C_1 - C_4} (C_1 - C_4 + C_2 - C_4 + C_3 - C_4 + C_4 + C_5 + \ldots + C_n) =$$

$$\frac{C_T - 3C_4}{C_1 - C_4} \qquad (4.36)$$

Hence, a reduction in the total capacitance will be obtained only if

$$C_1 - C_4 > 1 - \frac{3C_4}{C_T} \qquad (4.37)$$

Looking at expressions (4.34) through (4.37) one can reach the same conclusions as in case 1.

4.4.2 Analytical Optimization

We are now in the position to suggest an optimization strategy for the analytical part of the total capacitance minimization of a SC biquad. Recall that we start this step of the optimization with a network which contains 19 capacitors (Fig 4.1), all of them greater or equal to unity in value. In order to facilitate the design, all possible CSN combinations within the network of Fig. 4.1 were determined and are presented in Table 4.2. In this table, C_i again stands for a capacitor with CSN of type i. The optimization procedure can then be summarized by the following steps:

Table 4.2: Equivalent sets of CSNs for the biquad of Fig. 4.1.

C_5	C_6	C_7	C_8	C_9	C_{10}
(C,R)	(P,A)	(S,V)[3]	(C,T)	(R,U)	(G,X,M,V)
(G,H)	(L,M)	(T,U)[4]	(G,X)	(H,Y)	(G,X,R,U)
(P,A)[2]		(X,Y)[4]	(L,S)	(M,V)	(L,S,H,Y)
(I,J)					(L,S,R,U)
(F,N)					(C,T,H,Y)
(L,S,M,V)					(C,T,M,V)
(L,M)[2]					

[1] Note that V_1 and V_3 are S/H over a full clock period.
[2] If $V_2^o = z^{-1/2} V_2^e$.
[3] If S=V and V_2 is S/H ($V_2^o = z^{-1/2} V_2^e$), drop the combination.
[4] If the capacitors are equal, drop the combination.

Table 4.2: Continued.

C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}
(G,M)	(X,V)	(I,J,X,Y)	(I,X)	(J,Y)	(I,X,A,V)
(G,R)	(X,U)	(P,A,S,V)	(P,S)	(A,V)	(P,S,J,Y)
(L,H)	(S,Y)	(F,N,T,U)	(F,T)	(N,U)	(I,X,N,U)
(L,R)	(S,U)				(F,T,J,Y)
(C,M)	(T,V)				(P,S,N,U)
(C,H)	(T,Y)				(F,T,A,V)
(P,N)					
(P,J)					
(I,A)					
(I,N)					
(F,A)					
(F,J)					

Step 1: Look for transformations of type 1. These are the most preferable ones since they not only reduce the total capacitance as much as the type 2 transformations but they also eliminate capacitors, simplifying the final design.

Step 2: After the transformations of type 1 are realized, look for transformations of type 2. Here as well as in step 1, the largest set of transformations simultaneously realizable should be sought.

Step 3: Verify if there are still any capacitors whose values exceed 2 ($2C_{min}$). If this is the case, such capacitors may still be re-utilized for transformations of types 1 and 2. Then, return to step 1 and look for combinations involving these capacitors. Otherwise, proceed to step 4.

Step 4: After all transformations of types 1 and 2 have been realized, look for transformations of type 3. Note that these transformations must be realized sequentially. Therefore, start with the most profitable ones.

It should be understood that the optimization procedure proposed here does not yield (at least not always) a single option for the final realization. Particularly in steps 1 and 2 some subjective decision making is usually required. The designer will isolate all possible sets of transformations which are simultaneously realizable. Then, one of such sets must be chosen, and this choice will be, in general, based on criteria established for each specific

design. For example, suppose one is trying to minimize the total capacitance as well as the number of capacitors required for a given realization. It is possible that more than one set of transformations may yield exactly the same values for these parameters. Then, the designer should either choose any one of the available networks or introduce a new decision factor. One of such factors which may turn out to be of major importance is the network sensitivity. Recall that the analytical optimization starts with a fixed network which has, by the numerical optimization, acceptable sensitivity performance. However, one should know what happens with the network sensitivities when the structural transformations discussed in this section are performed. Even though different sets of transformations may lead to networks with the same total capacitance and number of capacitors, such networks will have different topologies and, consequently, different sensitivity performances. Such differences may, at last, decide which network should be preferred for a practical realization.

In what follows, the effects of the CSN combinations on the network sensitivities are analytically determined. With these results one can determine the sensitivities of the modified networks simply by using the sensitivity values obtained for the initial 19 capacitor configuration. Such sensitivities, on the other hand, can be obtained as a natural outcome of the numerical

optimization previously performed.

4.5 EFFECTS OF THE CSN COMBINATIONS ON THE NETWORK SENSITIVITIES

In order to avoid redundant explanations, we discuss only the case of the combination of 4 CSNs. The results for the particular case of 2 CSNs combined can then be readily derived.

Suppose that four capacitors C_1, C_2, C_3 and C_4 ($C_i \geq 1$ for all i) are combined by CSN equivalences. Also, consider without any loss of generality, that the value of C_4 is the lowest of these capacitors. Then, the new capacitance values will be given by

$$\begin{aligned} \hat{C}_1 &= C_1 - C_4 \\ \hat{C}_2 &= C_2 - C_4 \\ \hat{C}_3 &= C_3 - C_4 \\ \hat{C}_4 &= C_4 \end{aligned} \tag{4.38}$$

Now, let f be the function whose sensitivities are to be determined. The values of the sensitivities of f with respect to C_i, i=1,2,3,4, are known from the numerical optimization step. Considering the fact that the numerical value of f is not modified by the transformation (same CCEs) as, for example, is the case when f is equal to ω_o and Q, we have

$$f(C_1,C_2,C_3,C_4) = \hat{f}(\hat{C}_1,\hat{C}_2,\hat{C}_3,\hat{C}_4) = f(\hat{C}_1+\hat{C}_4,\hat{C}_2+\hat{C}_4,\hat{C}_3+\hat{C}_4,\hat{C}_4)$$

where $\hat{f}$ is the expression obtained when the variable transformations (4.38) are substituted in f. We are interested in determining the sensitivities of $\hat{f}$ with respect to $\hat{C}_i$, i=1,2,3,4. The sensitivity expressions are given by

$$S^{\hat{f}}_{\hat{C}_i} = \frac{\hat{C}_i}{\hat{f}} \frac{\partial \hat{f}}{\partial \hat{C}_i} = \frac{\hat{C}_i}{f} \frac{\partial f}{\partial C_i} \frac{\partial C_i}{\partial \hat{C}_i} \quad \text{for } i=1,2,3 \tag{4.39}$$

$$S^{\hat{f}}_{\hat{C}_4} = \frac{\hat{C}_4}{\hat{f}} \frac{\partial \hat{f}}{\partial \hat{C}_4} = \frac{\hat{C}_4}{f}\left[\frac{\partial f}{\partial C_1} \frac{\partial C_1}{\partial \hat{C}_4} + \frac{\partial f}{\partial C_2} \frac{\partial C_2}{\partial \hat{C}_4} + \frac{\partial f}{\partial C_3} \frac{\partial C_3}{\partial \hat{C}_4} + \frac{\partial f}{\partial C_4} \frac{\partial C_4}{\partial \hat{C}_4}\right] \tag{4.40}$$

but

$$\frac{\partial C_1}{\partial \hat{C}_1} = \frac{\partial C_2}{\partial \hat{C}_2} = \frac{\partial C_3}{\partial \hat{C}_3} = \frac{\partial C_1}{\partial \hat{C}_4} = \frac{\partial C_2}{\partial \hat{C}_4} = \frac{\partial C_3}{\partial \hat{C}_4} = \frac{\partial C_4}{\partial \hat{C}_4} = 1 \tag{4.41}$$

Then, from (4.38) through (4.41)

$$S^{\hat{f}}_{\hat{C}_i} = \frac{C_i - C_4}{f} \frac{\partial f}{\partial C_i} \quad \text{for } i=1,2,3 \tag{4.42}$$

and

$$S^{\hat{f}}_{\hat{C}_4} = \frac{C_4}{f}\left[\frac{\partial f}{\partial C_1} + \frac{\partial f}{\partial C_2} + \frac{\partial f}{\partial C_3} + \frac{\partial f}{\partial C_4}\right] \qquad (4.43)$$

By noting that

$$C_4 = C_i(C_4/C_i) \qquad \text{for any } i$$

and by using the definition of normalized sensitivity [51], the following sensitivity values are obtained:

$$S^{\hat{f}}_{\hat{C}_i} = (1 - \frac{C_4}{C_i})\, S^f_{C_i} \qquad \text{for} \quad i=1,2,3 \qquad (4.44)$$

$$S^{\hat{f}}_{\hat{C}_4} = S^f_{C_4} + (\frac{C_4}{C_1})S^f_{C_1} + (\frac{C_4}{C_2})S^f_{C_2} + (\frac{C_4}{C_3})S^f_{C_3} \qquad (4.45)$$

From these equalities we conclude that whenever the CSN equivalences are employed, all capacitors involved, except the least valued one (here C_4) have their sensitivitites reduced. The sensitivity of the least valued capacitor, however, may increase or decrease, depending on the relative values of the sensitivities with respect to the other capacitors involved in the combination. Another interesting property is that, even though the individual sensitivities may vary considerably, the total sum remains unchanged. This is because any parameter of the transfer function of a SC network is homogeneous of order zero [59] with respect to

the capacitance values (not capacitance ratios) [4,5].

It should be clear at this point that the derivations for the case of a combination of 2 capacitors would lead to the same conclusions as in (4.44) and (4.45) without the terms corresponding to, say, C_2 and C_3.

4.6 OPTIMIZATION ALGORITHM

In this section a flow chart is presented which summarizes the optimization algorithm discussed so far. The numerical optimization (Step I) is not shown in detail because the algorithm employed is very simple and was implemented using the subroutine VF02AD of the Harwell Library [55]. More details about the objective function and the constraints can be found in the appendix at the end of this chapter. The flow chart is presented in Fig. 4.4, where the box labelled MCO refers to the numerical Multiple Criteria Optimization. In the next section, two detailed examples are presented in order to illustrate the application of this algorithm.

It is interesting to note that the analytical optimization algorithm of Fig. 4.4 could be implemented by a computer program. However, such an implementation may bring more problems than benefits. One of the major problems would be the decision points of the type "is the present value of this figure of merit acceptable?". Usually these decisions are quite subjective and the acceptable values

Figure 4.4: Optimization Algorithm.

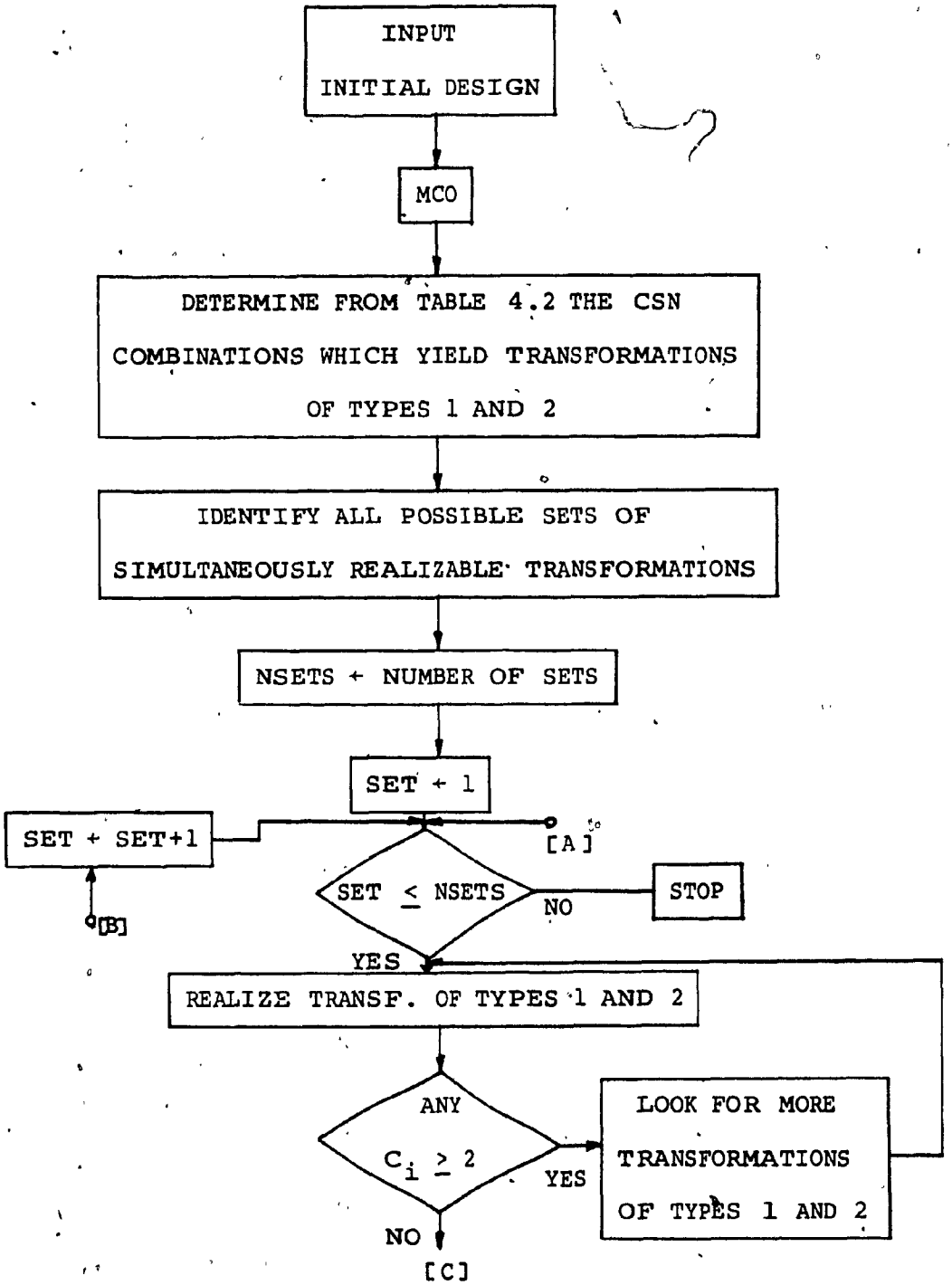
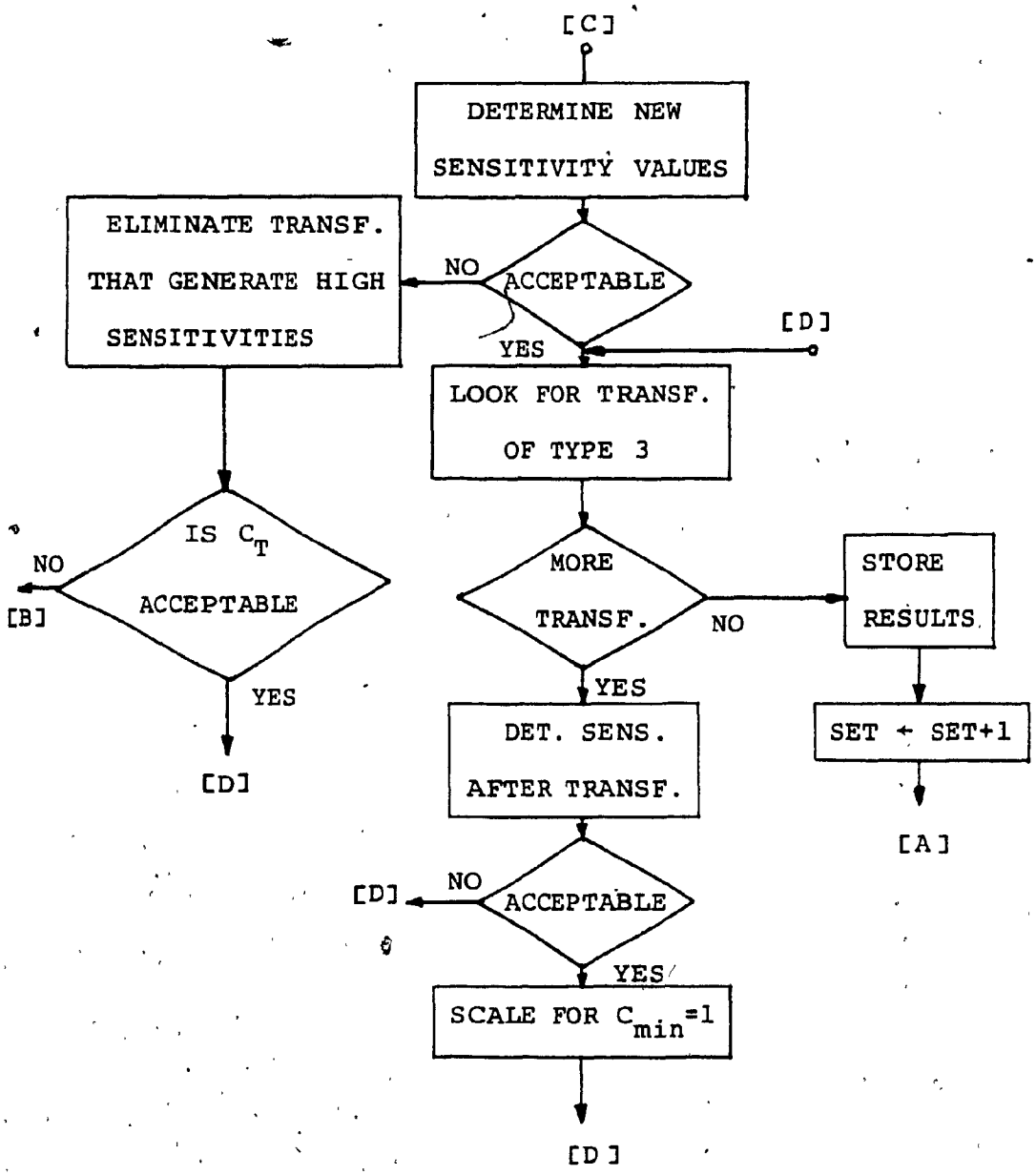


Figure 4.4: Continued.



vary from one designer to the other. A possible solution would be the implementation of an interactive program. However, in all the examples tried so far the execution of the algorithm proved to be so simple as to be carried out by using pencil and paper, and the need for a probably time consumming program was not felt at all. As a matter of fact, the MCO step is the most time consumming part of the design procedure in its present form. This is probably due to the fact that no special effort was made to minimize the computing time in this step.

4.7 EXAMPLES

4.7.1 Lowpass notch filter

As a first example, consider a lowpass notch section with the following specifications:

f_p (pole frequency) = 2 kHz

Q_p (pole Q) = 30

f_z (zero frequency) = 2.5 kHz

DC gain = 1.

f_s (sampling frequency) = 25 kHz

To control the dynamic range we use, in (4.18)

$K_1 = 1.1$

$K_2 = 1/K_1$

Two brief initial runs for C=0 and P=0 indicate that the optimization considering P=0 leads to better results in this case. Then, the initial network used for all steps of the MCO was the network ACR in Table 3.2, where

A=1.

B=2.01249

C=16.405406

D=31.1915

G=15.405389

I=1.29304

J=1.29304

R=1.

The MCO steps are shown in Table 4.3. The output of the fourth run represents a good compromise between total capacitance and network sensitivity. The capacitance values for this network as well as the ω_o and Q sensitivities are shown in Table 4.4. It can be verified that the ω_o sensitivities are quite small, whereas some of the Q sensitivities have increased considerably. However, considering that for high Q networks the ω_o sensitivities are of major importance [4,5,51,52] and that capacitance ratios can be implemented within 0.1% of tolerance [3,4,5], such Q sensitivity values are quite acceptable [56]. Nevertheless, the design is not concluded yet. Up to this point though, the total capacitance required has been

Table 4.3: MCO steps - lowpass notch filter.

RUN	w_1	w_2	f_{cap}	f_{sens}	system solved
1	1	0	21.9646	19.7541	-----
2	0	1	2301.3832	2.2489	-----
3	0.00038547	0.050194	144.9863	3.1351	(1,2)
4	0.005946	0.04401	46.5865	6.052	(1,3)
5	0.017403	0.03127	29.2408	10.1923	(1,4)

Table 4.4: Capacitance values and sensitivities of the numerically optimized lowpass notch filter.

Capacitors	Cap. values	ω_o sensitivity	Q sensitivity
A	2.165	0.545	-2.396
B	3.7209	-0.430	1.888
C	5.6699	0.599	0.490
D	9.3941	-0.498	0.548
F	1.0	-0.071	-13.252
G	6.3871	-	-
H	1.0	-	-
I	3.0332	-	-
J	3.1546	-	-
L	1.0	-0.0189	-6.007
M	1.0015	-0.0266	6.252
N	1.0	-0.045	13.760
P	0.0	-	-
R	1.0	-0.086	-2.949
S	1.3049	0.0239	7.616
T	1.0	-0.0958	-0.0839
U	1.7554	0.168	0.147
V	1.0	-0.0258	-6.014
X	1.0	-	-
Y	1.0	-	-

reduced by 33% and the capacitance spread by 69.9%. It is worthwhile to note that such improvement in component spread allows an easier implementation of accurate capacitance ratios [5], minimizing the consequences of the higher Q sensitivities.

We now proceed to the next step of the design procedure, i.e., the analytical optimization according to the algorithm of Fig. 4.4. Table 4.5 shows the list of all possible transformations of types 1 and 2. This list is obtained by determining the capacitor sets in Table 4.2 which satisfy the necessary conditions for such transformations. Then, the possible independent sets of transformations are identified. In this search, preference in given to those transformations which lead to greater reductions on the total capacitance and/or the number of capacitors. It should be remembered that, whenever possible, it is interesting to reduce the number of elements in the network, since this number is associated with the amount of connections to be implemented in the chip and connections occupy die area.

By this search, it is found that the set of transformations (among five possibilities) shown in Table 4.6 yields the maximum reduction in total capacitance. The new capacitance and sensitivity values obtained after performing such transformations are presented in Table 4.7. It can be verified from this table that approximately one

Table 4.5: Possible CSN equivalence transformations of types 1 and 2 (lowpass notch).

CAPACITOR SET	REDUCTION IN	
	No. OF CAPACITORS	TOTAL CAPACITANCE
(C,R)	-	1.0
(G,H)	-	1.0
(F,N)	2	1.0
(X,Y)	2	2.0
(C,T)	-	1.0
(G,X)	-	1.0
(H,Y)	1	1.0
(C,T,H,Y)	2	3.0
(G,M)	-	1.0015
(G,R)	-	1.0
(L,H)	1	1.0
(L,R)	1	1.0
(C,M)	-	1.0015
(C,H)	-	1.0
(I,N)	-	1.0
(F,A)	-	1.0
(F,J)	-	1.0
(X,V)	1	1.0
(T,V)	1	1.0
(T,Y)	1	1.0
(I,X)	-	1.0
(F,T)	1	1.0
(J,Y)	-	1.0
(A,V)	-	1.0
(I,X,A,V)	1	3.0
(F,T,J,Y)	2	3.0
(F,T,A,V)	2	3.0

Table 4.6: Set of transformations which leads to maximum reduction in total capacitance (lowpass notch filter).

CAPACITOR SET	REDUCTION IN	
	No. OF CAPACITORS	TOTAL CAPACITANCE
(F,N)	2	1.0
(C,T,H,Y)	2	3.0
(I,X,A,V)	1	3.0
(L,R)	1	1.0
(G,M)	-	1.0015

Table 4.7: Values of the transformed elements, their sensitivities and the structural modifications performed in the network (lowpass notch filter).

CAPACITOR SET	CAPACITORS	INITIAL VALUES	NEW VALUES	ω_o SENSITIVITIES	Q SENSITIVITIES	NETWORK MODIFICATIONS
(F,N)	F	1.0	F=N=0	-	-	-
	N	1.0	B=B+1	-	-	-
(L,R)	L	1.0	1.0	-0.1049	-8.9560	$L = C_{11}$
	R	1.0	-	-	-	
(I,X,A,V)	I	3.0332	2.0332	-	-	$I = C_1$
	X	1.0	-	-	-	
	A	2.1650	1.1650	0.293	-1.289	$A = C_3$
	V	1.0	1.0	0.226	-7.120	$V = C_{16}$
(C,T,H,Y)	C	5.6699	4.6699	0.460	0.404	$C = C_1$
	T	1.0	1.0	0.0028	0.0025	$T = C_{10}$
	H	1.0	-	-	-	
	Y	1.0	-	-	-	
(G,M)	G	6.3871	5.3856	-	-	$G = C_1$
	M	1.0015	1.0015	-0.0266	6.252	$M = C_{11}$

half of the sensitivities have decreased and one half have increased. The final values, however, are quite acceptable and the maximum magnitude of the Q sensitivities has dropped from 13.76 to 8.96 due to the elimination of capacitors F and N from the network. Their sensitivities are now incorporated into the sensitivities with respect to capacitor B. However, only variations on the capacitance ratios will affect the network performance. Therefore, one should be concerned only about the sensitivitites with respect to the elements other than B and D since these two are the reference capacitors (appear in the denominator) for all the capacitance ratios. Table 4.7 also lists the network modifications required. For each capacitor set, the modifications are performed as explained in the following for the case of the combination (I,X,V,A). Firstly, drop all capacitors involved in the combination. Then use the new values for I, A and V (X=0) in capacitors with the associated CSNs, namely C_1, C_3 and C_{16} respectively. Of course this has to be done so that the voltage sources and virtual grounds initially switched to a given capacitor remain the same. Also, the switching phases must be maintained. A good way to verify whether the transformations were performed correctly is by applying the supperposition theorem to the voltage sources involved. By doing so, one should be able to identify all the switching schemes used in the original configuration.

The next step is to verify if more transformations of types 1 and 2 can be performed. To this end we take all capacitors whose values are over 2 and look for possible combinations involving them. Such study shows that capacitors I and J can be recombined. Capacitor I is then substituted by an unswitched capacitor (CSN type 5) of the same value and J has its value modified to J-I=1.1214 (with the same CSN). This step reduces even further the total capacitance.

The final network is shown in Fig. 4.5 and employs 13 capacitors. No transformation of type 3 is possible here which would lead to a reduction in the total capacitance. A comment is in order at this point. Usually, the transformations of type 3 lead to marginal improvements only. This happens because, according to equation (4.30), the reduction in total capacitance for combinations of 2 capacitors (the most common one) is always less than the value of the smallest capacitance value of the set which is, after the numerical optimization, usually close or equal to unity. For combinations of 4 capacitors, eq. (4.36), the improvement may be more significant, but only in the cases where there are two or more capacitors which are equal and are, at the same time, the least valued elements in the set. Therefore, the designer should, at this point of the optimization, decide about the convenience of looking for transformations of type 3. Our experience has demonstrated

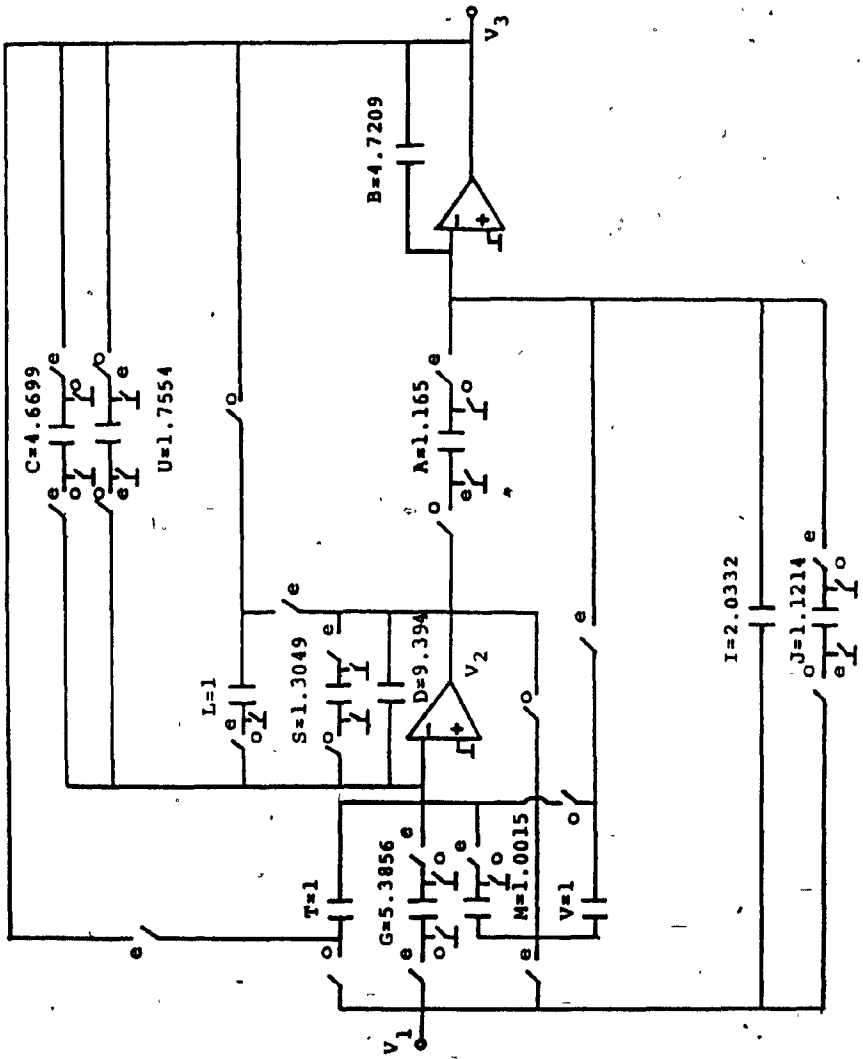


Figure 4.5: Lowpass notch filter - optimized network.

that, most of the times, the economy obtained (if any) does not pay for the time spent in the search and calculations involved. Nevertheless, after a few examples any designer should be able to develop a "feeling" of when such transformations are worth trying.

Table 4.8 presents a comparison of the networks corresponding to the initial design, the numerically optimized design and the final design obtained after the analytical optimization. It can be readily verified from this table that almost 50% of improvement in total capacitance and 70% improvement in component spread have been obtained over the initial design. Also, the number of elements is not excessively large. In any case, the application of this method yields realizations with at most 19 capacitors, the final number depending on the element reduction obtained in the analytical optimization.

An analysis of the final network shows that a good dynamic range has resulted. The ratios of the maximum amplitude values of V_2^e and V_2^o over the maximum magnitude value of V_3^e for a unity input signal are verified to be 1.046 and 1.088 respectively.

As expected, this improvement in the network design comes at the expense of an increase in sensitivity, compared with the initial realization. However, the high capacitance ratio accuracy obtainable in MOS circuits and the

Table 4.8: Comparisons (lowpass notch).

	INITIAL DESIGN	AFTER NUMERICAL OPTIM.	IMPROVEMENT ON THE INITIAL DESIGN	AFTER ANALYTICAL OPTIM.	IMPROVEMENT ON THE INITIAL DESIGN	IMPROVEMENT ON THE NUMERICAL OPTIM.
TOTAL CAPACITANCE	69.9	46.6	33%	35.55	48.9%	15.9%
SPREAD	31.19	9.4	69.9%	9.4	69.9%	-
No. OF CAPACITORS	8	19	-	13	-	31.6%

improvement achieved in capacitance spread serve to mitigate the effects of the increased sensitivities. In fact, a Monte Carlo simulation, considering capacitance ratio tolerances of $\pm 0.1\%$ (Gaussian distribution) shows maximum variations of 0.063% (σ=0.43 Hz) in ω_o and 1.48% (σ=0.148) in Q. Consequently, the frequency performance of the filter should lie within acceptable limits in practice.

4.7.2 Bandpass filter

As a second example, consider a bandpass network with the following specifications:

f_p (pole frequency) = 2 kHz
Q_p (pole Q) = 30
Peak gain = 1
f_s (sampling frequency) = 20 kHz

The same values of K_1=1.1 and K_2=1/K_1 are used. An initial run reveals that better results can be obtained by using a network with C=0.

The initial design used is then the network APR (ACR/2 in Table 3.2), where

A=1.
B=31.6936
C=0
D=3.25233
G=1.

H=1.

I=6.60916

P=20.4952

R=2.0

The MCO steps are shown in Table 4.9. The output of the fifth run is then chosen to proceed with the analytical optimization. The capacitance values and the corresponding sensitivities for this design are presented in Table 4.10.

For this network, the ratios of the maximum amplitudes for the outputs V_2^e and V_2^o over the maximum amplitude for V_3^e, all for a unitary input, are found to be 1.01 and 1.48, respectively. Such dynamic range is usually acceptable for signal filtering purposes.

The analytical optimization proceeds as follows. Table 4.11 shows all possible network transformations of types 1 and 2. The two sets of transformations shown in Table 4.12 are the ones which yield maximum reduction of total capacitance and element count. Since these two options are found to yield approximately the same total capacitance, number of capacitors and sensitiviy performance, let us pick option 1 to proceed further with the example. The new capacitance and sensitivity values obtained after the transformations are presented in Table 4.13, along with the corresponding network modifications.

Table 4.9: MCO steps - bandpass filter.

RUN	w_1	w_2	f_{cap}	f_{sens}	system solved
1	1	0	22.9352	22.1245	-----
2	0	1	24349.5125	3.33195	-----
3	3.48886×10^{-5}	0.045163	367.78426	3.699997	(1,2)
4	2.28814×10^{-3}	0.042827	70.3777	5.54421	(1,3)
5	0.0115953	0.0331786	36.0542	9.6061	(1,4)

Table 4.10: Capacitance values and sensitivities of the numerically optimized bandpass filter.

Capacitors	Cap. values	ω_o sensitivity	Q sensitivity
A	1.2923	-0.216	-3.026
B	4.4159	-0.463	1.901
C	-	-	-
D	3.4959	-0.434	0.545
F	1.0	-0.608	-10.019
G	1.0	-	-
H	3.6630	-	-
I	1.0367	-	-
J	1.0	-	-
L	1.0	-0.096	-11.429
M	1.0091	0.052	12.113
N	1.0060	-0.044	9.963
P	4.4246	0.784	0.634
R	1.0	0.201	-2.688
S	1.1445	-0.087	12.516
T	2.9478	0.556	0.450
U	1.0	-0.189	-0.153
V	1.0	-0.003	11.354
X	1.0	-	-
Y	3.6184	-	-

Table 4.11: Possible CSN equivalence transformations of types 1 and 2 (bandpass).

CAPACITOR SET	REDUCTION IN	
	No. OF CAPACITORS	TOTAL CAPACITANCE
(G,H)	-	1.0
(P,A)	-	1.29
(G,X)	1	1.0
(R,U)	1	1.0
(G,X,R,U)	3	3.0
(T,U)	1	1.0
(X,Y)	1	1.0
(G,R)	1	1.0
(L,H)	-	1.0
(L,R)	1	1.0
(P,N)	-	1.006
(P,J)	-	1.0
(F,J)	1	1.0
(X,V)	1	1.0
(X,U)	1	1.0
(S,Y)	-	1.44
(T,V)	-	1.0
(P,S)	-	1.44
(F,T)	-	1.0
(J,Y)	-	1.0
(F,T,J,Y)	1	3.0

Table 4.12: Sets of transformations which lead to maximum reduction in total capacitance (bandpass filter).

	CAPACITOR SET	REDUCTION IN	
		No. OF CAPACITORS	TOTAL CAPACITANCE
option 1	(G,X,R,U)	3	3.0
	(F,J)	1	1.0
	(P,A)	-	1.29
	(P,N)	-	1.006
	(L,H)	-	1.0
	(S,Y)	-	1.44
	(T,V)	-	1.0
option 2	(G,X,R,U)	3	3.0
	(F,T,J,Y)	1	3.0
	(P,A)	-	1.29
	(P,S)	-	1.44
	(L,H)	-	1.0

Table 4.13: Values of the transformed elements, their sensitivities and the structural modifications performed in the network (bandpass filter).

CAPACITOR SET	CAPACITORS	INITIAL VALUES	NEW VALUES	ω_o SENSITIVITIES	Q SENSITIVITIES	NETWORK MODIFICATIONS
(G,X,R,U)	G	1.0	-	-	-	
	X	1.0	-	-	-	
	R	1.0	1.0	0.120	-2.535	$R = C_{10}$
	U	1.0	-	-	-	
(F,J)	F	1.0	1.0	-0.608	-10.019	
	J	1.0	-	-	-	$F = C_{11}$
(P,A)	P	4.4246	3.1323	0.555	0.449	$P = C_1$
	A	1.2923	1.2923	0.013	-2.840	$A = C_6$
(P,N)	P	3.1323	2.126	0.292	0.237	$P = C_1$
	N	1.0060	1.0060	0.134	10.107	$N = C_{11}$
(L,H)	L	1.0	1.0	-0.096	-11.429	$L = C_{11}$
	H	3.6630	2.6630	-	-	$H = C_3$
(S,Y)	S	1.1445	1.1445	-0.087	12.516	$S = C_{12}$
	Y	3.6184	2.4739	-	-	$Y = C_4$
(T,V)	T	2.9478	1.9478	0.367	0.297	$T = C_2$
	V	1.0	1.0	0.185	11.507	$V = C_{12}$

Note that in this example, the possibility of using the capacitor P in more than one combination has been identified from the beginning. Hence, both network transformations were executed in the same step. Note, however, that they are executed sequentially since the capacitance and sensitivity values resulting from the first combination are employed as initial values for the second transformation. Furthermore, transformations of type 3 were not sought for the reasons given in example 1.

The final network is shown in Fig. 4.6 and the corresponding comparisons are presented in Table 4.14.

A Monte Carlo simulation, with $\pm 0.1\%$ tolerance for the capacitance ratios (Gaussian distribution) shows maximum variations of 0.062% (σ=0.425 Hz) in ω_o and 2.77% (σ=0.277) in Q, which is usually acceptable in practice [56].

It should be mentioned that in the examples presented here, the main goal was the reduction in the total capacitance required for a given realization, keeping the sensitivity performance of the network as well as its dynamic range within practically acceptable limits. If, for a given application, such limits are more demanding, the choice of the tradeoff point in the numerical optimization and the transformations to be used in the analytical optimization should be more carefully exercised.

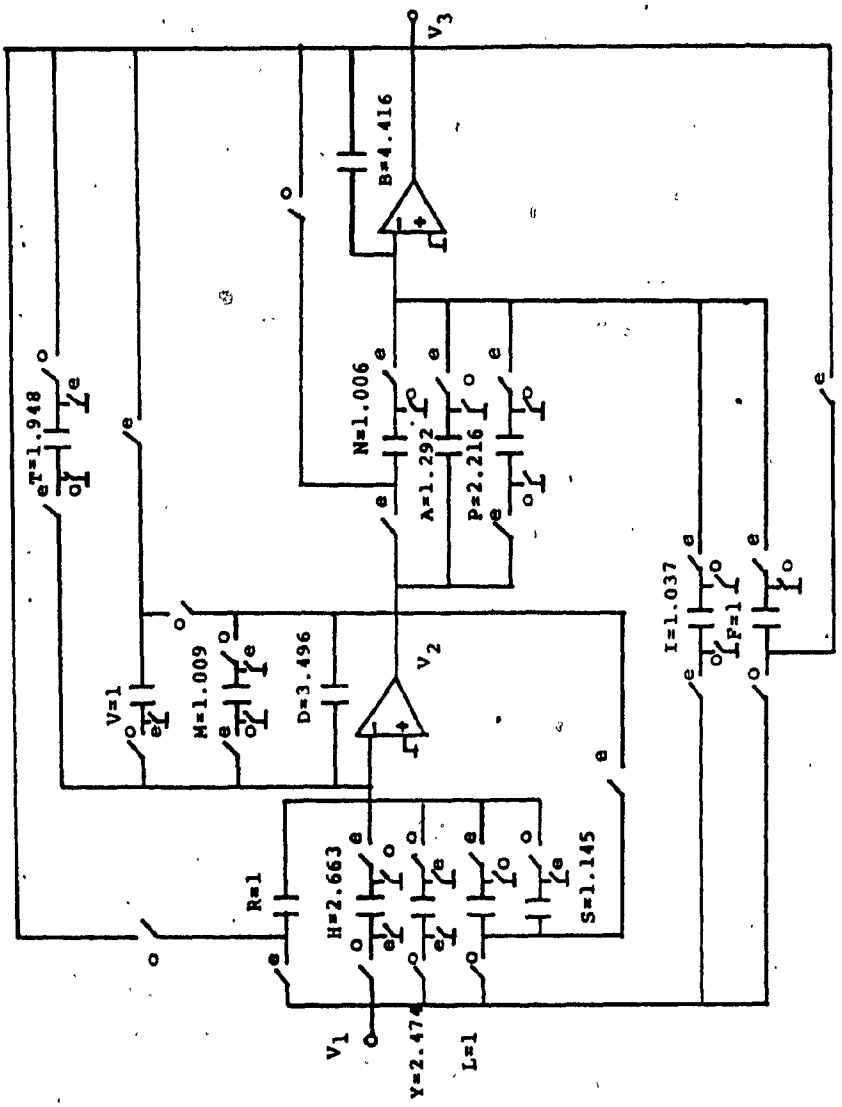


Figure 4.6: Bandpass filter - optimized network.

Table 4.14: Comparisons (bandpass).

	INITIAL DESIGN	AFTER NUMERICAL OPTIM.	IMPROVEMENT ON THE INITIAL DESIGN	AFTER ANALYTICAL OPTIM.	IMPROVEMENT ON THE INITIAL DESIGN	IMPROVEMENT ON THE NUMERICAL OPTIM.
TOTAL CAPACITANCE	67.05	36.05	46.2%	26.6	60.3%	26.2%
SPREAD	31.69	4.43	86.02%	4.42	86.05%	0.2%
No. OF CAPACITORS	8	19	-	15	-	21.05%

The examples presented here, however, illustrate the possibility of considerable design improvement by applying the proposed technique.

4.8 SUMMARY

In this chapter a new technique is proposed for the optimization of stray insensitive SC networks. The proposed algorithm makes use of the CSN equivalences presented in Chapter III. This allows the design to be carried out with a small number of variables and without the need of large computational times.

By using techniques of Multiple Criteria Optimization, a tradeoff between the total capacitance necessary to realize a given transfer function and the network sensitivities is achieved in the numerical part of the optimization algorithm. In this step, only a reduced general biquad with 19 capacitors is used. This is done, however, without any loss in the design flexibility regarding the realization of the transfer function coefficients. In the subsequent step, the CSN equivalences are employed to further reduce the total capacitance, the capacitance spread and the number of elements in the network. Analytical formulas are provided to determine the effects of the application of any given CSN equivalence on the total capacitance as well as on the network sensitivities. The control of the dynamic range is also

discussed and a technique is proposed which has led to good practical results. Two examples are presented in detail to illustrate the application of the algorithm. These examples show the possibility of considerable design improvement by using the new method.

The optimization procedure proposed in this chapter has been applied to the most general stray insensitive biquad, according to the stray insensitivity conditions presented in [14] and briefly discussed in Chapter I. However, it is important to note that the method can be equaly applied to any subnetwork of this general biquad. A typical example would be its application to optmize single OA networks. Even in the case of biquads, the initial network does not have to contain necessarily 19 capacitors. Of course, the smaller the size of the initial structure the lesser are the chances to reduce the total capacitance by any optimization procedure. However, depending on the particulars of the technology employed, sometimes the use of more elements could overcome the advantages obtained by the reduction of the total capacitance in terms of the integration area due to the need for more interconnections. In the examples presented in this chapter we have used the most general network in order to illustrate the generality of the method. In practice, it may not be always necessary to start from the most general network. One can start from any useful intermediate network.

4.9 APPENDIX

In this appendix we present a detailed description of the numerical optimization step (MCO) of the algorithm in Fig. 4.4. The objective function, the equality and inequality constraints, as well as their respective derivatives are presented. The specific order of presentation has been chosen for the sake of neatness.

4.9.1 Equality Constraints

As explained in section 4.3, the equality constraints are given by the coefficients of the transfer function $H(z)$ written as in (4.5). From (4.5) and (3.1) the transfer function coefficients for the network in Fig. 4.1 are given by

$$\gamma = \frac{PG-I(1+L)}{(1+F)(1+L)}$$

$$\epsilon = \frac{\begin{array}{l}J(1+V)(1+L)+I(1+M)(1+S)+\\(X-Y)[A(1+L)-P(1+M)]-AG(1+S)-PH(1+V)\end{array}}{(1+F)(1+L)(1+V)}$$

$$\delta = \frac{[AH-J(1+M)](1+S)}{(1+F)(1+L)(1+V)} \qquad \text{(A.1)}$$

$$\alpha = \frac{\begin{array}{l}(T-U)[P(1+M)-A(1+L)]+PR(1+V)+\\AC(1+S)-(1+F)(1+M)(1+S)-(1+N)(1+L)(1+V)\end{array}}{(1+F)(1+L)(1+V)}$$

$$\beta = \frac{[(1+M)(1+N)-AR](1+S)}{(1+F)(1+L)(1+V)}$$

Recall that, in obtaining these equations, B=D=1 has been assumed. Therefore, the variables in the above equalities are capacitance ratios and not absolute capacitance values.

Let us now define the vector $\underline{x}$ of the optimization variables as function of the capacitances in Fig. 4.1 in the following way:

$$\underline{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \\ x_{10} \\ x_{11} \\ x_{12} \\ x_{13} \\ x_{14} \\ x_{15} \\ x_{16} \\ x_{17} \\ x_{18} \\ x_{19} \\ x_{20} \end{bmatrix} = \begin{bmatrix} A \\ B \\ C \\ D \\ F \\ G \\ H \\ I \\ J \\ L \\ M \\ N \\ P \\ R \\ S \\ T \\ U \\ V \\ X \\ Y \end{bmatrix}$$

and the elements y_i of the vector $\underline{y}$ of the capacitance ratios in equations (A.1) as

$$y_i = \frac{x_i}{x_2} \text{ for } i=1,2,5,8,9,12,13$$

and $$y_i = \frac{x_i}{x_4} \text{ otherwise.}$$

The substitution of these definitions in (A.1) yields, for the equality constraints h_i, i=1 to 5, the following expressions:

$$h_1 : [\gamma(1+y_5)+y_8](1+y_{10})$$

$$h_2 : \{[\varepsilon(1+y_5)-y_9](1+y_{10})+y_7y_{13}\}(1+y_{18})+ [y_1y_6-y_8(1+y_{11})](1+y_{15})-(y_{19}-y_{20})[y_1(1+y_{10})- y_{13}(1+y_{11})]$$

$$h_3 : \delta(1+y_5)(1+y_{10})(1+y_{18})-[y_1y_7-y_9(1+y_{11})](1+y_{15})$$

$$h_4 : \{[\alpha(1+y_5)+(1+y_{12})](1+y_{10})-y_{13}y_{14}\}(1+y_{18})+ [(1+y_5)(1+y_{11})-y_1y_3](1+y_{15})- (y_{16}-y_{17})[y_{13}(1+y_{11})-y_1(1+y_{10})]$$

$$h_5 : \beta(1+y_5)(1+y_{10})(1+y_{18})-[(1+y_{11})(1+y_{12})-y_1y_{14}](1+y_{15})$$

The derivatives of these constraints, which are required by the Harwell optimization subroutine VF02AD are given by:

$$\frac{\partial h_1}{\partial x_2} = \frac{1}{x_2^2}\left[y_6 x_{13} - (1+y_{10})(\gamma x_5 + x_8)\right]$$

$$\frac{\partial h_1}{\partial x_4} = \frac{1}{x_4^2}\left\{x_6 y_{13} - x_{10}\left[\gamma(1+y_5)+y_8\right]\right\}$$

$$\frac{\partial h_1}{\partial x_5} = \frac{1}{x_2}\left[\gamma(1+y_{10})\right]$$

$$\frac{\partial h_1}{\partial x_6} = -\frac{y_{13}}{x_4}$$

$$\frac{\partial h_1}{\partial x_8} = \frac{(1+y_{10})}{x_2}$$

$$\frac{\partial h_1}{\partial x_{10}} = \frac{\gamma(1+y_5)+y_8}{x_4}$$

$$\frac{\partial h_1}{\partial x_{13}} = \frac{-y_6}{x_2}$$

$$\frac{\partial h_2}{\partial x_1} = \frac{y_6(1+y_{15}) - (y_{19}-y_{20})(1+y_{10})}{x_{10}}$$

$$\frac{\partial h_2}{\partial x_2} = \frac{-1}{x_2^2}\{[y_6(1+y_{15})-(y_{19}-y_{20})(1+y_{10})]x_1+$$
$$(\varepsilon x_5-x_9)(1+y_{10})(1+y_{18})-(1+y_{11})(1+y_{15})x_8+$$
$$[y_7(1+y_{18})+(y_{19}-y_{20})(1+y_{11})]x_{13}\}$$

$$\frac{\partial h_2}{\partial x_4} = \frac{-1}{x_4^2}\{(y_1x_6-y_8x_{11})(1+y_{15})+(y_{19}-y_{20})(y_{13}x_{11}-y_1x_{10})+$$
$$[\varepsilon(1+y_5)-y_9][(1+y_{18})x_{10}+(1+y_{10})x_{18}]+$$
$$y_{13}x_7(1+y_{18})+[y_1y_6-y_8(1+y_{11})]x_{15}+$$
$$[y_1(1+y_{10})-y_{13}(1+y_{11})](x_{20}-x_{19})+y_7y_{13}x_{18}\}+$$
$$y_{13}[x_7(1+y_{18})+x_{18}y_7]$$

$$\frac{\partial h_2}{\partial x_5} = \frac{\varepsilon(1+y_{10})(1+y_{18})}{x_2}$$

$$\frac{\partial h_2}{\partial x_6} = \frac{y_1(1+y_{15})}{x_4}$$

$$\frac{\partial h_2}{\partial x_7} = \frac{y_{13}(1+y_{18})}{x_4}$$

$$\frac{\partial h_2}{\partial x_8} = \frac{-(1+y_{11})(1+y_{15})}{x_2}$$

$$\frac{\partial h_2}{\partial x_9} = \frac{-(1+y_{10})(1+y_{18})}{x_2}$$

$$\frac{\partial h_2}{\partial x_{10}} = \frac{[\varepsilon(1+y_5)-y_9](1+y_{18})-y_1(y_{19}-y_{20})}{x_4}$$

$$\frac{\partial h_2}{\partial x_{11}} = \frac{(y_{19}-y_{20})y_{13}-(1+y_{15})y_8}{x_4}$$

$$\frac{\partial h_2}{\partial x_{13}} = \frac{y_7(1+y_{18})+(y_{19}-y_{20})(1+y_{11})}{x_2}$$

$$\frac{\partial h_2}{\partial x_{15}} = \frac{y_1 y_6 - y_8(1+y_{11})}{x_4}$$

$$\frac{\partial h_2}{\partial x_{18}} = \frac{\{\varepsilon[(1+y_5)-y_9](1+y_{10})+y_7 y_{13}\}}{x_4}$$

$$\frac{\partial h_2}{\partial x_{19}} = \frac{-[y_1(1+y_{10})-y_{13}(1+y_{11})]}{x_4}$$

$$\frac{\partial h_2}{\partial x_{20}} = \frac{y_1(1+y_{10})-y_{13}(1+y_{11})}{x_4}$$

$$\frac{\partial h_3}{\partial x_1} = \frac{-y_7(1+y_{15})}{x_2}$$

$$\frac{\partial h_3}{\partial x_2} = \frac{-1}{x_2^2}\{[x_9(1+y_{11})-x_1 y_7](1+y_{15})+\delta x_5(1+y_{10})(1+y_{18})\}$$

$$\frac{\partial h_3}{\partial x_4} = \frac{-1}{x_4^2}\{(x_{11}y_9-x_7y_1)(1+y_{15})+\delta(1+y_5)[x_{10}(1+y_{18})+ x_{18}(1+y_{10})]-[y_1y_7-y_9(1+y_{11})]x_{15}\}$$

$$\frac{\partial h_3}{\partial x_5} = \frac{\delta(1+y_{10})(1+y_{18})}{x_2}$$

$$\frac{\partial h_3}{\partial x_7} = \frac{-y_1(1+y_{15})}{x_4}$$

$$\frac{\partial h_3}{\partial x_9} = \frac{(1+y_{11})(1+y_{15})}{x_2}$$

$$\frac{\partial h_3}{\partial x_{10}} = \frac{\delta(1+y_5)(1+y_{18})}{x_4}$$

$$\frac{\partial h_3}{\partial x_{11}} = \frac{y_9(1+y_{15})}{x_4}$$

$$\frac{\partial h_3}{\partial x_{15}} = \frac{-[y_1 y_7 - y_9(1+y_{11})]}{x_4}$$

$$\frac{\partial h_3}{\partial x_{18}} = \frac{\delta(1+y_5)(1+y_{10})}{x_4}$$

$$\frac{\partial h_4}{\partial x_1} = \frac{(y_{16}-y_{17})(1+y_{10}) - y_3(1+y_{15})}{x_2}$$

$$\frac{\partial h_4}{\partial x_2} = \frac{-1}{x_2^2}\{(\alpha x_5 + x_{12})(1+y_{10})(1+y_{18}) +$$
$$(y_{16}-y_{17})[x_1(1+y_{10}) - x_{13}(1+y_{11})] +$$
$$(1+y_{15})[x_5(1+y_{11}) - x_1 y_3] - x_{13} y_{14}(1+y_{18})\}$$

$$\frac{\partial h_4}{\partial x_3} = \frac{-y_1(1+y_{15})}{x_4}$$

$$\frac{\partial h_4}{\partial x_4} = \frac{-1}{x_4^2}\{[\alpha(1+y_5) + (1+y_{12})][x_{10}(1+y_{18}) + x_{18}(1+y_{10})] +$$
$$(y_{16}-y_{17})(x_{10}y_{17} - x_{11}y_{13}) + [x_{11}(1+y_5) - x_3 y_1](1+y_{15}) +$$
$$[(1+y_5)(1+y_{11}) - y_1 y_3]x_{15} + [y_{13}(1+y_{11}) -$$
$$y_1(1+y_{10})](x_{17}-x_{16}) - y_{13}[x_{14}(1+y_{18}) + x_{18}y_{14}]\}$$

$$\frac{\partial h_4}{\partial x_5} = \frac{\alpha(1+y_{10})(1+y_{18}) + (1+y_{11})(1+y_{15})}{x_2}$$

$$\frac{\partial h_4}{\partial x_{10}} = \frac{[\alpha(1+y_5) + (1+y_{12})](1+y_{18}) + (y_{16}-y_{17})y_1}{x_4}$$

$$\frac{\partial h_4}{\partial x_{11}} = \frac{(1+y_5)(1+y_{15}) - y_{13}(y_{16}-y_{17})}{x_4}$$

$$\frac{\partial h_4}{\partial x_{12}} = \frac{(1+y_{10})(1+y_{18})}{x_2}$$

$$\frac{\partial h_4}{\partial x_{13}} = \frac{-[y_{14}(1+y_{18})+(y_{16}-y_{17})(1+y_{11})]}{x_2}$$

$$\frac{\partial h_4}{\partial x_{14}} = \frac{-y_{13}(1+y_{18})}{x_4}$$

$$\frac{\partial h_4}{\partial x_{15}} = \frac{(1+y_5)(1+y_{11})-y_1y_3}{x_4}$$

$$\frac{\partial h_4}{\partial x_{16}} = \frac{-[y_{13}(1+y_{11})-y_1(1+y_{10})]}{x_4}$$

$$\frac{\partial h_4}{\partial x_{17}} = \frac{y_{13}(1+y_{11})-y_1(1+y_{10})}{x_4}$$

$$\frac{\partial h_4}{\partial x_{18}} = \frac{[\alpha(1+y_5)+(1+y_{12})](1+y_{10})-y_{13}y_{14}}{x_4}$$

$$\frac{\partial h_5}{\partial x_1} = \frac{y_{14}(1+y_{15})}{x_2}$$

$$\frac{\partial h_5}{\partial x_2} = \frac{-\{[x_1y_{14}-x_{12}(1+y_{11})](1+y_{15})+\beta x_5(1+y_{10})(1+y_{18})\}}{x_2^2}$$

$$\frac{\partial h_5}{\partial x_4} = \frac{-1}{x_4^2}\{\beta(1+y_5)-[x_{10}(1+y_{18})+x_{18}(1+y_{10})]+ (1+y_{15})[x_{14}y_1-x_{11}(1+y_{12})]- [(1+y_{11})(1+y_{12})-y_1y_{14}]x_{15}\}$$

$$\frac{\partial h_5}{\partial x_5} = \frac{\beta(1+y_{10})(1+y_{18})}{x_2}$$

$$\frac{\partial h_5}{\partial x_{10}} = \frac{\beta(1+y_5)(1+y_{18})}{x_4}$$

$$\frac{\partial h_5}{\partial x_{11}} = \frac{-(1+y_{12})(1+y_{15})}{x_4}$$

$$\frac{\partial h_5}{\partial x_{12}} = \frac{-(1+y_{11})(1+y_{15})}{x_2}$$

$$\frac{\partial h_5}{\partial x_{14}} = \frac{y_1(1+y_{15})}{x_4}$$

$$\frac{\partial h_5}{\partial x_{15}} = \frac{-[(1+y_{11})(1+y_{12})-y_1y_{14}]}{x_4}$$

$$\frac{\partial h_5}{\partial x_{18}} = \frac{\beta(1+y_5)(1+y_{10})}{x_4}$$

4.9.2 Inequality Constraints

The inequality constraints can be divided into two distinct groups. The first group guarantees the nonexistence of negative elements in the network. The constraints are given by the inequalities (4.2) and (4.3) or (4.4). Their derivatives can be obtained readily and are not presented here. The second group of inequality constraints is used for dynamic range control, as per inequalities (4.19) and (4.20). The derivatives of these two constraints, if analytically evaluated, would be very complex and, therefore, would require large amounts of memory and computing time in the execution of the program. Consequently, these derivatives were evaluated by numerical methods.

For the numerical determination of derivatives, the two-point difference formula (forward difference) has been

employed [57]. According to this formula, the derivative of a multivariable function $f(\underline{x})$ with respect to a variable x_i of $\underline{x}$ is given by

$$\frac{\partial f}{\partial x_i} = \frac{f(x_i+\Delta x_i)-f(x_i)}{\Delta x_i} \qquad (A.2)$$

where $\Delta x_i = 10^{-13} x_i$ has been used. This formula has been preferred over the three point formula [57] to economize computing time since the accuracy obtained has been verified to be sufficient.

4.9.3 Objective Function

Since the objective function (4.22), is a linear combination of f_{cap} and f_{sens}, the derivatives can be evaluated separately for each of these functions and then weighted and added as per equation (4.22).

The derivatives of f_{cap} with respect to the variables x_i are all equal to one. The derivatives of f_{sens}, on the other hand, are quite complex. Due to the fact that the sensitivity expressions themselves already contain the derivatives of α and β with respect to the optimization parameters, the evaluation of the derivatives of f_{sens} involves the determination of the second derivatives of α and β.

The derivative of f_{sens} with respect to a given x_i can be written as

$$\frac{\partial f_{sens}}{\partial x_i} = \sum_{i\ 1}^{20} |x_k| \left[\frac{\partial}{\partial x_i} |f_3(x_k)| + \frac{\partial}{\partial x_i} |f_4(x_k)|\right] + \frac{\partial |x_k|}{\partial x_i} \left[|f_3(x_k)| + |f_4(x_k)|\right] \quad (A.3)$$

where

$$f_3(x_k) = (1+\beta) \frac{\partial \alpha}{\partial x_k} - \alpha \frac{\partial \beta}{\partial x_k} \quad (A.4)$$

$$f_4(x_k) = (1-\beta) \frac{\partial \alpha}{\partial x_k} + (\alpha-2) \frac{\partial \beta}{\partial x_k} \quad (A.5)$$

$$\frac{\partial f_3(x_k)}{\partial x_i} = (1+\beta) \frac{\partial^2 \alpha}{\partial x_k \partial x_i} - \alpha \frac{\partial^2 \beta}{\partial x_k \partial x_i} + \frac{\partial \beta}{\partial x_i} \frac{\partial \alpha}{\partial x_k} - \frac{\partial \alpha}{\partial x_i} \frac{\partial \beta}{\partial x_k} \quad (A.6)$$

$$\frac{\partial f_4(x_k)}{\partial x_i} = (1-\beta) \frac{\partial^2 \alpha}{\partial x_k \partial x_i} + (\alpha-2) \frac{\partial^2 \beta}{\partial x_k \partial x_i} + \frac{\partial \alpha}{\partial x_i} \frac{\partial \beta}{\partial x_k} - \frac{\partial \beta}{\partial x_i} \frac{\partial \alpha}{\partial x_k} \quad (A.7)$$

Now, a look at the expressions of the equality constraints h_4 and h_5 reveals that, for $\alpha = N_\alpha / D_\alpha$ and $\beta = N_\beta / D_\beta$

$$h_4 = \alpha_n D_\alpha - N_\alpha$$

and

$$h_5 = \beta_n D_\beta - N_\beta$$

where α_n and β_n are nominal values of α and β, respectively, obtained from the given transfer function. Then, with a little algebraic manipulation, one concludes that

$$\frac{\partial \alpha}{\partial x_k} = \frac{-1}{D_\alpha}\left[\alpha \frac{\partial D_\alpha}{\partial x_k} - \frac{\partial N_\alpha}{\partial x_k}\right] = \frac{-1}{D_\alpha}\frac{\partial h_4}{\partial x_k} \tag{A.8}$$

and, likewise

$$\frac{\partial \beta}{\partial x_k} = \frac{-1}{D_\beta}\frac{\partial h_5}{\partial x_k} \tag{A.9}$$

where $D_\alpha = D_\beta = (1 + y_5)(1 + y_{10})(1 + y_{18})$

Since the expressions for the derivatives of h_4 and h_5 have been already determined, the following procedure can be employed to evaluate the second partial derivatives of α and β. These derivatives can be written as

$$\frac{\partial^2 \alpha}{\partial x_k \partial x_i} = \frac{\partial}{\partial x_i}\left(\frac{\partial \alpha}{\partial x_k}\right)$$

$$\frac{\partial^2 \beta}{\partial x_k \partial x_i} = \frac{\partial}{\partial x_i}\left(\frac{\partial \beta}{\partial x_k}\right)$$

Then:

(1) Evaluate $\frac{\partial \alpha}{\partial x_k}(x_i)$ and $\frac{\partial \beta}{\partial x_k}(x_i)$. These values are easily obtainable from (A.8) and (A.9). They are also employed to evaluate f_{sens}.

(2) Transform x_i into $x_i+\Delta x_i$ ($\Delta x_i=10^{-13}x_i$ has been used).

(3) Evaluate $\frac{\partial \alpha}{\partial x_k}(x_i+\Delta x_i)$ and $\frac{\partial \beta}{\partial x_k}(x_i+\Delta x_i)$. This is equivalent to repeat step (1) with x_i replaced by $x_i+\Delta x_i$.

(4) Evaluate

$$\frac{\partial^2 \alpha}{\partial x_k \partial x_i} = \frac{1}{\Delta x_i}\left[\frac{\partial \alpha}{\partial x_k}(x_i+\Delta x_i) - \frac{\partial \alpha}{\partial x_k}(x_i)\right]$$

and

$$\frac{\partial^2 \beta}{\partial x_k \partial x_i} = \frac{1}{\Delta x_i}\left[\frac{\partial \alpha}{\partial x_k}(x_i+\Delta x_i) - \frac{\partial \alpha}{\partial x_k}(x_i)\right]$$

With these values in hand, the evaluation of f_{sens} and its derivatives is straightforward.

CHAPTER V

CONCLUSIONS

5.1 SUMMARY

Switched capacitor filters have been extensively researched in the past decade. These filters are very attractive since they are completely MOS realizable. This feature minimizes the final cost, improves the reliability and facilitates the reproduction in large scale. Considerable effort has been spent in the generation of good SC networks, specially for filtering applications. Among the existing design methodologies, one that has enjoyed a great deal of popularity is the synthesis of SC filters by an interconnection of building blocks (usually in cascade form) such as amplifiers, delay circuits, first order and second order networks. This approach offers some advantages over the direct design of high order filters, such as modularity, simpler design equations and easier scaling.

In this thesis a new method has been proposed for the generation of SC networks in such a way that the circuits obtained are automatically insensitive to the parasitic capacitances inherent to the fabrication process. The network generation method is simple, easy to apply and leads directly to the minimum size of the most general stray insensitive SC network for a given number of OAs. Special attention has been given to the particular cases of single

OA and second order networks due to their wide applicability. Techniques have also been proposed to reduce the general networks obtained to structures of manageable size without losing flexibility in the design process. Further, an optimization algorithm has been presented which allows the reduction of the chip area necessary for the realization of a given transfer function.

Towards this end, a new systematic approach is presented, using the parasitic insensitivity conditions previously reported, to determine the most general switching scheme which guarantees the stray insensitivity of a SC network with a given number of OAs. Then, only those capacitors which contribute to the network transfer function are employed along with the derived switching scheme. This approach automatically avoids the use of redundant elements. The method is introduced in Chapter II to determine the most general stray insensitive single OA SC network. Subsequently, all possible z-domain transfer functions obtainable from this general single OA network are derived, along with the necessary conditions for their realizability without any matching conditions being imposed on the capacitors employed. Techniques are then proposed to reduce the general structure to circuits of practically acceptable complexity. Also, procedures to improve the final design by reducing the total capacitance, the number of elements and/or the component spread are discussed.

In Chapter III, the network generation technique is extended for the case of second order networks (two OAs). After the derivation of the most general stray insensitive biquad, the concept of "capacitor switching network" (CSN) is introduced. This concept allows the determination of a reduced general biquad which is able to realize any transfer function realizable by the original network with maximum flexibility in choosing the coefficients of the various CCEs. The reduced network employs only capacitors that are switched according to a limited set of four basic types of CSNs. Quasi-canonic (8 capacitors) building blocks capable of realizing any second order transfer function are derived from the reduced general biquad. Then, the remaining CSNs are employed, along with the already derived biquads, to obtain a new set of general second order networks. Some of the new networks have subnetworks which are canonic in terms of the number of capacitors and are, themselves, general biquads. A total of 28 biquad building blocks is obtained. The complete set contains the five stray insensitive general biquads presented so far in the literature. The remaining 23 networks are completely new. Design equations are provided for all networks, along with sensitivity values for a bilinearly transformed transfer function. Dynamic range maximization as well as spread and total capacitance minimizations are discussed.

Chapter IV deals with the optimization of SC networks. An algorithm is proposed to reduce the chip area necessary for the implementation of a given transfer function. This is done through the minimization of the required total capacitance. The new method allows the optimization to be carried out with a network of variable topology without, however, requiring the computational effort usually necessary in these cases. Even though the proposed algorithm can be applied to networks of any order, the design of second order networks is emphasized since those are the most used building blocks in the synthesis of SC filters. The design flexibility of the most general stray insensitive biquad, which employs 120 capacitors, is maintained without the need of more than 19 variables during any phase of the optimization process. Such reduction in the system complexity is obtained by using the concept of CSN equivalences, which is generalized in this chapter. In the proposed method, multiple criteria optimization techniques are employed so that a tradeoff between total capacitance and network sensitivity is obtained. Dynamic range scaling is also considered.

In all the relevant chapters, detailed examples are presented which demonstrate the possibility of design improvement by the use of the new techniques proposed. Many SC filters have been built and tested in laboratory to verify the validity of the theoretical results presented.

Due to the lack of proper MOS integration facilities, however, these filters have been implemented using discrete components. The experimental results agree closely with the theoretical predictions.

5.2 SUGGESTIONS FOR FURTHER WORK

Some of the possible directions for further research on the results obtained in this thesis are discussed in what follows:

(i) So far, the technique for generation of parasitic insensitive SC networks has been applied to structures employing at most two OAs. Since the method is general, its extension to produce good network topologies for the realization of higher order filters (such as ladder networks, for instance) is certainly an appropriate topic for future investigation.

(ii) The networks obtained in this thesis are known to perform well in the voice-band frequency range. Their capabilities for applications at higher frequencies, however, are still to be determined. Since many of the new networks employ novel capacitor switching schemes, an investigation in this direction could lead to interesting results.

(iii) The biquad building blocks obtained in Chapter III have been derived to realize general second order transfer functions. An alternative approach would be to determine sets of networks to realize specific

transfer functions, such as bandpass, lowpass, etc. Generating the biquads in this way, the design flexibility given by the general building blocks is lost. On the other hand, some properties like sensitivity or total capacitance, for example, may be improved because the new structures would be specifically generated to realize the desired transfer function.

In conclusion, it is hoped that the results reported in this thesis will be useful to others interested in the area of design and implementation of switched capacitor networks.

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