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HIGH PERFORMANCE STATIC CONVERTERS FOR SERIES COMPENSATION OF INDUSTRIAL POWER SYSTEMS

Alexandre Campos

A Thesis

in

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ABSTRACT

HIGH PERFORMANCE STATIC CONVERTERS FOR SERIES COMPENSATION OF INDUSTRIAL POWER SYSTEMS

Alexandre Campos, Ph.D.
Concordia University, 1994.

Increased loading on installed resources and the proliferation of non-ideal loads are turning power systems into weak networks, for which the assumption of an ideal infinite bus is no longer applicable. This results in the presence of undesirable system characteristics such as harmonic contamination, increased reactive power flow, voltage and current unbalance, and voltage instability. This thesis proposes a number of high performance single and three-phase series compensators capable of eliminating or reducing some of these negative impacts of weak systems on the power supply quality at the user level. It deals specifically with voltage unbalance compensation, ac voltage regulation, and load power factor compensation in industrial power systems. PWM voltage source inverters connected in series with the ac supply through transformers form the core of the proposed compensators. Their operation is based on the control of the amplitude and phase of the output voltage of the PWM inverters. Voltage unbalance compensation in three-phase systems is performed by controlling three single-phase inverters independently, cancelling the negative sequence voltage component; the positive sequence component can then be adjusted to regulate the voltage. Voltage regulation is achieved by controlling the amplitude of the compensating voltage to reduce source voltage variations. Input power factor correction is obtained by phase-shifting the compensating voltage with respect to the source voltage when operating with reactive loads. The principles of operation, design equations, design examples and implementation procedures are included to demonstrate the validity of the proposed compensation methods. Simulation and experimental results on 5 kVA laboratory prototypes confirm the validity of the theoretical considerations and feasibility of the proposed compensators.

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Dedicated to my wife Neuza and
my parents Guinarte and Ivone.

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LIST OF MAIN SYMBOLS

$\mathbf{A}$	Symmetrical sequence components transformation matrix.
$\mathbf{F}_{abc1}$	Switching function fundamental component - positive sequence component.
$\mathbf{F}_{abc2}$	Switching function fundamental component - negative sequence component.
ϕ_L	Load phase angle.
ϕ_s	Phase angle at the source.
G_i	Gain of the PWM technique - modulation index to rms value.
I_{BASE}	Base current.
Ii_{BASE}	Base current - inverter side.
$\mathbf{I}_{abc}$	Line currents.
$\vec{I}_L$	Load current.
I_i	Inverter output current.
K_i	Ripple of the dc bus current.
K_v	Ripple of the dc bus voltage.
$\vec{MF}$	Magnitude factor.
ME	Magnitude error.
$\vec{P}_C$	Compensator real power.

P_{dc} DC bus rated real power.

$\vec{Q}_C$ Compensator reactive power.

R_{abc} Reference signals for the inverter.

R_{abc1} Reference signals for the inverter - positive sequence component.

R_{abc2} Reference signals for the inverter - negative sequence component.

S_{BASE} Base power.

$\vec{S}_C$ Compensator apparent power.

$\vec{S}_L$ Load apparent power.

S_R Rectifier rated power.

θ Phase angle between the source and the load voltages.

S_I Inverter rated power.

SL_f Rated power of L_f.

SC_f Rated power of C_f.

THD_i Current THD.

THD_v Voltage THD.

$\vec{UF}$ Unbalance factor.

$\vec{V}_L$ Load terminal voltage.

$\mathbf{VL}_{abc}$ Load line-to-line voltages.

$\mathbf{VL}_{abc1}$ Load line-to-line voltages - positive sequence component.

$\mathbf{VL}_{abc2}$ Load line-to-line voltages - negative sequence component.

$\mathbf{Vi}_{BASE}$ Base voltage - inverter side.

$\mathbf{V}_{BASE}$ Base voltage.

$\vec{V}_C$ Compensator terminal voltage.

$\mathbf{Vc}_{abc}$ Compensator line-to-line voltages.

$\mathbf{Vc}_{abc1}$ Compensator line-to-line voltages - positive sequence component.

$\mathbf{Vc}_{abc2}$ Compensator line-to-line voltages - negative sequence component.

$\vec{V}_S$ Source terminal voltage.

$\mathbf{Vs}_{abc}$ Source line-to-line voltages.

$\mathbf{Vs}_{012}$ Symmetrical components of the source line-to-line voltages.

$\mathbf{Vs}_{abc1}$ Source line-to-line voltages - positive sequence component.

$\mathbf{Vs}_{abc2}$ Source line-to-line voltages - negative sequence component.

$\mathbf{V}_{I_{abc}}$ Inverter line-to-line voltages.

$\mathbf{V}_{I_{abc1}}$ Inverter line-to-line voltages - positive sequence component.

$\mathbf{V}_{I_{abc2}}$ Inverter line-to-line voltages - negative sequence component.

V_{dc} DC bus rated voltage.

V_I Inverter output voltage.

$\underline{v}(t)_{abc}$ Space-vectors of the line-to-line voltages.

$\underline{v}(t)_{012}$ Space-vectors of the line-to-line voltages symmetrical sequence components.

$\underline{v}_1(t)_{odq}$ Space-vectors of the odq components of the positive sequence component.

$\underline{v}_2(t)_{odq}$ Space-vectors of the odq components of the negative sequence component.

$v_1(t)_{odq}$ odq components of the positive sequence component.

$v_2(t)_{odq}$ odq components of the negative sequence component.

XL_f Reactance of the inductor of the inverter output filter.

XC_f Reactance of the capacitor of the inverter output filter.

XL_{dc} Reactance of the inductor of the dc bus filter.

XC_{dc} Reactance of the capacitor of the dc bus filter.

Z_{BASE} Base impedance.

Zi_{BASE} Base impedance - inverter side.

LIST OF ACRONYMS

THD	Total Harmonic Distortion
IEC	International Electrotechnical Commission
VAR	Volt-Ampere-Reactive
CS-VAR	Current Source VAR
VS-VAR	Voltage Source VAR
PWM	Pulse Width Modulation
SPWM	Sine PWM
PCC	Point-of-Commom-Connection
TCR	Thyristor Controlled Reactor
TSC	Thyristor Switched Capacitor
FC-TCR	Fixed-Capacitor TCR
HVDC	High Voltage DC
VSI	Voltage Source Inverter

CHAPTER 1

INTRODUCTION

1.1 General

In standard power systems analysis it is assumed, in most applications, that the source can be represented as an ideal three-phase source. A source is considered ideal if it produces balanced three-phase voltages with constant amplitude and frequency, for any load condition. This defines what is known as an infinite bus. This assumption is less and less valid as power systems reach their loading limits and non ideal loads proliferate. These include nonlinear loads (static power converters) and large single-phase loads [1-2].

This exploitation of the system closer to its limits, which results in a reduction of the operational safety margin, is the consequence of a variety of problems. The oil crisis during the seventies created economic conditions for a major shift toward the use of electricity as the primary energy source. Also, the fast industrialization, urbanization and population growth, particularly in developing countries, has increased the demand for electrical energy. Added to these problems is the fact that new electrical energy sources are becoming scarce and more expensive. The immediate consequence is the added load on the existing power system, resulting in a weaker power system, for which the infinite bus assumption is no longer valid. The high equivalent impedance that characterizes weak power systems creates an ideal

environment for harmonic propagation, and the presence of reactive power flow, voltage unbalances, current unbalances, and voltage instabilities [4-8].

Traditionally these problems have been solved at two levels: (a) the utility level, by the addition of new resources such as power stations, shunt and series capacitor compensation, and new transmission lines, and (b) at the user level, by adding voltage regulation equipment, load power factor correction devices, passive harmonic filters and unbalance compensators. The first solution, the addition of new resources, is becoming less attainable due to the following: (a) the available sites for hydroelectric plants are farther and farther removed from major loads; (b) the society exercises pressures against the installation of new nuclear or thermoelectric power plants; (c) obtaining right-of-way allied with concerns of health safety are making the construction of new transmission lines an almost unmanageable task [4-8]. At the user level the traditional techniques are no longer capable of solving the problems they were designed to solve. Examples of these are: (a) the use of tapped transformers to regulate the load voltage are becaming insufficient mostly due to the fast voltage variations experienced by industrial power system; (b) the presence of harmonics in the line currents and voltages are turning the use of capacitors in power factor compensation into a very expensive and complex scheme due to the potential of low frequency resonance.

The origin of the problem, for both utility and user levels, resides in the fact that power systems are mostly controlled by mechanical devices, and cannot act fast enough to reduce the effects of the switching of large loads, the penetration of harmonics, and fast unbalance and reactive power variations.

1.2 Effects of Power Quality on Industrial Loads

The above mentioned problems result in the industrial customers seeing more and more a low quality power supply, deviating from the ideal infinite bus concept, and having a variety of effects on the load. Two of the main effects are (a) the appearance of voltage unbalances due to the presence of single phase loads, and (b) voltage variations due to the increase in the power supply equivalent impedance. Furthermore, the customer is still constrained to reflect back onto the ac system a high power factor load.

The quality of ac voltage sources is an important, if not critical, aspect for most of the loads present in today's power systems. The specialization and selectiveness of the loads are increasing their vulnerability to power quality problems. This reflects into a restricted range of acceptable input characteristics, such as input voltage variation and maximum voltage unbalance. These restrictions are forcing the sources to be constrained to very narrow margins of operation. As an example, large voltage variations are not generally tolerable in power systems, and most utilities define a maximum acceptable margin of ± 20% of voltage variation. Undervoltage causes degradation in the performance of electrical motors by increasing their line currents, and overvoltages can drive motors and transformers into saturation, which causes harmonic generation.

Unbalance is usually classified in two categories, voltage (or source) unbalance, and current (or load) unbalance, despite the fact they do not occur separately. An uncompensated unbalanced load, when supplied by a balanced voltage source, will create an unbalanced set of currents, which can appear throughout the power system causing unbalanced voltage drops. The magnitude of such unbalances in the power system increases as the system

equivalent impedance becomes larger, which is one of the main characteristics of a power system exploited closer to its limits.

Voltage unbalance has not yet been standardized at the power system level, and the only mention to voltage unbalance limits is the NEMA standard MG-1 for ac sources, which specifies a maximum of 1% of voltage unbalance when supplying ac motors [2]. The consequences on ac motors of an unbalanced source are severe. For example, a 3.5% voltage unbalance can result in a 25% increase in the operating temperature, and a shortening by half of the insulation life span of induction motors [2]. Synchronous machines are generally more sensitive to voltage unbalance. Very large generators can tolerate very little sustained unbalance, and they are usually equipped with negative sequence alarms set for 5% of current unbalance.

These three constraints at the customer supply level, which are voltage unbalances, voltage regulation, and load power factor, leave the customer with the following choices: (a) design his equipment to take into account these deviations from the ideal source, which usually translates into a much higher installation and maintenance cost, or (b) take corrective actions to guarantee a high quality ac source. This last solution can be met either through series connected control devices or through VAR injection [8-11].

The main objective of the thesis is to address the problem of voltage regulation and unbalance compensation at the industrial load level. Although VAR injection is used to achieve these goals, power factor correction remains a secondary issue, and VAR compensation to achieve unity power factor is therefore not analyzed in depth in this work.

1.3 Literature review

1.3.1 AC Controllers

The simplest and most common method of obtaining a regulated and balanced ac voltage source uses phase-controlled thyristor ac-ac controllers, as shown in Fig.1.1. The line voltage is first increased by means of a transformer and its output voltage is then reduced by modifying the ac waveform to obtain the required load voltage [12,13]. The chopping procedure is done by line-commutated thyristors. By controlling symmetrically the firing angle of both switches, as shown in Fig. 1.2.(a), it is possible to vary the rms value of the output voltage V_o (Fig. 1.2.(b)). This line-commutated approach produces a large amount of harmonics (Fig. 1.2.(c)), which might require a large output filtering stage. Due to the current harmonics and the phase-shift of the fundamental current component, the input power factor

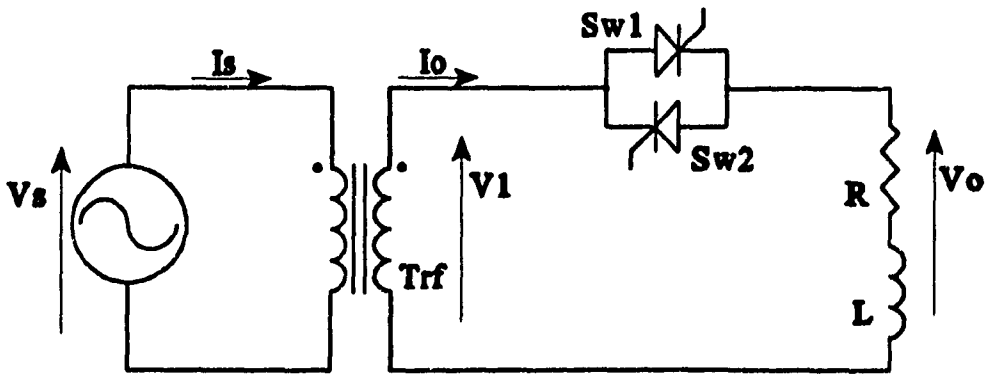

Fig. 1.1 - Typical single-phase ac-ac converter.

is very low, and a power factor correction network might be required to increase it. Because all the load power is controlled by the converter, its power rating is always higher than 1 pu. Also, the cycle by cycle control scheme gives the converter a small bandwidth, and poor dynamic response.

Three phase versions of these ac controllers have also been proposed. Voltage regulation is achieved by the same procedure as described for the single phase converter.

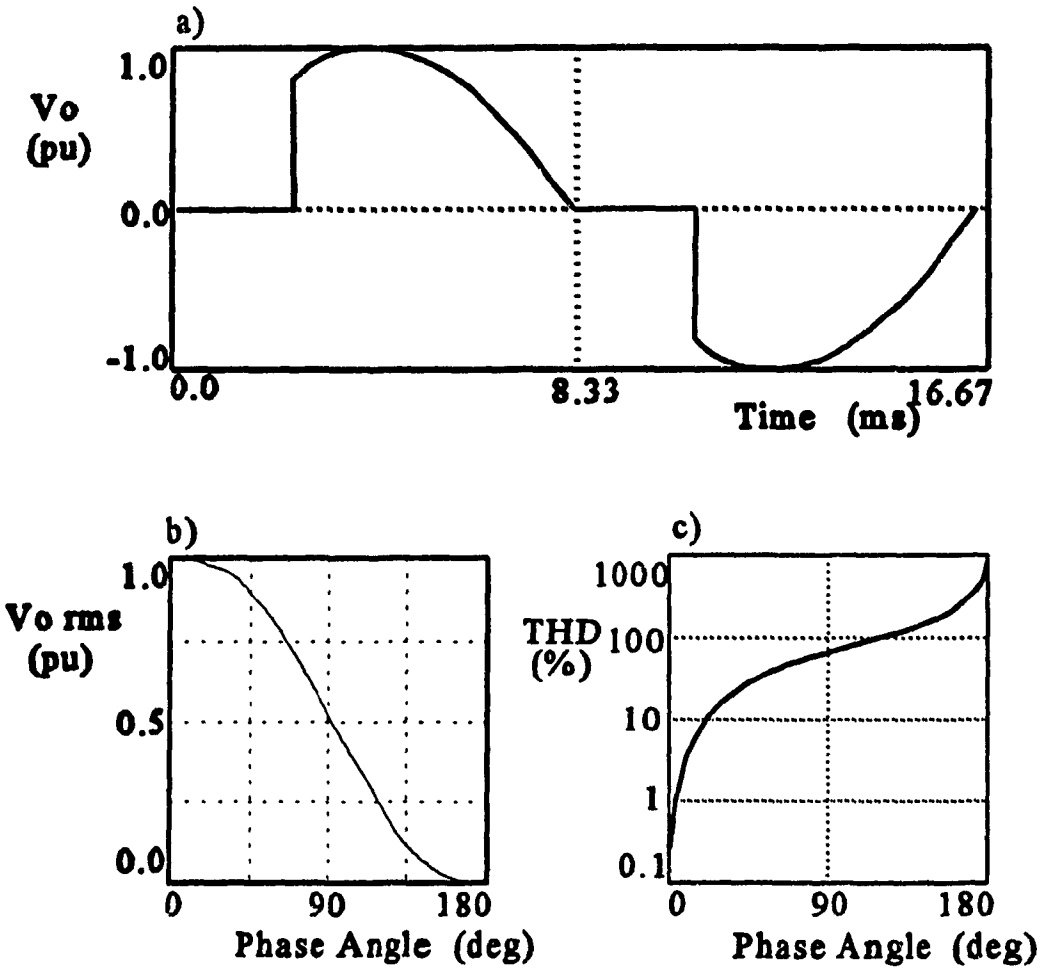

Fig. 1.2 - a) Output voltage waveform, b) rms value of the load voltage, and c) total harmonic distortion for a single phase line-commutated ac-ac converters.

Besides voltage regulation features, Muljadi *et al* presented a static compensator for unbalanced sources using this scheme, Fig 1.1 [14]. The unbalance compensation of the source voltage is achieved by using unsymmetrical control of each phase. The drawbacks presented for the single phase configuration are all applicable to this case.

With the appearance of high power controllable switches such as bipolar transistors, GTO's and MOSfets, it became possible to improve the performance of ac controllers by using pulse width modulation (PWM) techniques. Fig. 1.3.a shows the output voltage waveform of a typical PWM controlled single phase ac-ac converter. By controlling the duty-cycle of the gating signals it is possible to vary the rms value of the output voltage (Fig. 1.3.b). The spectrum of the load voltage contains the desired fundamental and harmonic components of the same order as the switching frequency. This results in a reduction in the low frequency harmonics injected into the power system and in the size of the required input/output filters, as shown in Fig. 1.3.c. The dynamic performance of the system is improved when compared to line-commutated schemes. Most of applications do require a transformer in order to regulate output voltage with low input voltages. Furthermore, these ac choppers require bidirectional switches, in which high reliability is difficult to achieve. The total power rating for the system is still larger than 1 pu [15,16].

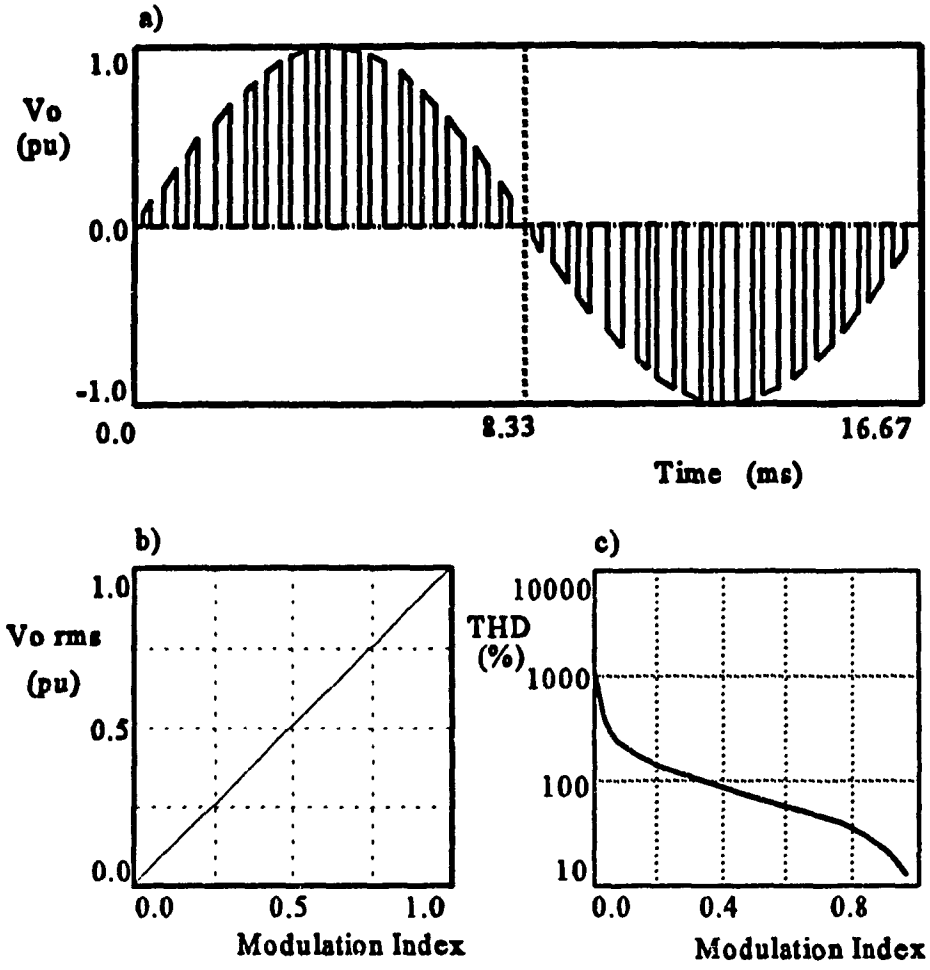

Fig. 1.3 - a) Output voltage waveform, b) rms value of the load voltage, and c) total harmonic distortion for a single phase PWM controlled ac-ac converters.

1.3.2 VAR Compensators

Voltage regulation in unconstraint buses by shunt VAR compensation has been commercially used mostly in power transmission systems. The reactive energy required for

the operation of the power system is supplied by compensators placed at specific points in the system, allowing the regulation of the bus voltage. The utility is required to supply mostly real power, which improves the utilization of the systems' resources, and reduces the risks of instability. There are three basic approaches to VAR compensation based on: (a) passive components; (b) thyristor-switched reactors combined with capacitors, if required; and (c) the solid-state PWM converters.

1.3.2.1 Series Passive Devices

VAR compensation by means of passive devices has been used for a long time. The method consists in connecting in series with the ac line a bank of capacitors to compensate the equivalent inductive reactance of the source [3,4,6]. A typical configuration of a series capacitive compensator is shown in Fig. 1.4. The capacitors can be inserted or removed by the bypass switches. With a proper adjustment of the degree of compensation (the number

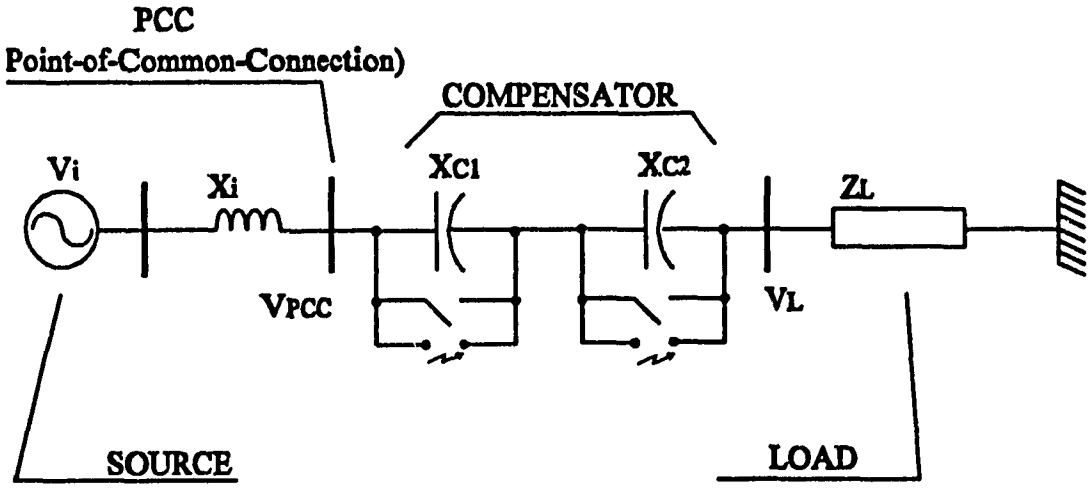

Fig. 1.4 - Simplified diagram of a passive capacitive compensation.

of capacitors) it is possible to maintain the load voltage in a required value. This technique is basically a steady state solution due to the intrinsic low speed of the switching approach, which is usually a mechanical one. When high power thyristors are used in this function, a slightly faster switching action can be achieved. The main disadvantages of this technique are (a) the minimum switching interval is half cycle, giving to the system a poor dynamic response, (b) there is the risk of series resonances between the capacitors and the system inductances, which requires special protective devices, (c) the variation of the degree of compensation is not continuous but discrete and fixed by the number of capacitors used, and (d) voltage unbalance compensation cannot be achieved.

1.3.2.2 Shunt Passive Devices

The most common approach for voltage regulation with VAR compensation is by means of shunt connected devices, such as thyristor switched reactances. It is a well-known technique, and has been widely used since the appearance of high-power SCR's [17-21]. At the user level, it has mostly been used in power factor control. These devices act as a variable shunt impedance by synchronously inserting or removing shunt capacitors and controlling the effective value of inductors connected across the network. Using an appropriate control approach, the VAR injection can be controlled to achieve the voltage regulation.

Fig. 1.5 shows the three main topologies of thyristor switched reactances, which are (a) the thyristor-controlled reactor (TCR), (b) the thyristor-switched capacitor (TSC), usually employed with TCR, and (c) the fixed capacitor TCR (FC-TCR).

The first topology (Fig. 1.5.a), the thyristor-controlled reactor (TCR) consists in a fixed reactor in series with a bidirectional switch (two back-to-back connected thyristors). Variable inductance can be achieved by delaying the firing angles of the switches. This configuration can only provide a variable inductive reactance, thus it is limited to applications where only voltage reduction is needed. Due to the fact that in most cases a voltage boost is the required corrective action, a variable capacitive reactance is the only possible solution to achieve voltage regulation[18-20].

The topology shown in Fig. 1.5.b, the thyristor-switched capacitor (TSC), can provide a switched capacitive reactance. It consists in a fixed capacitor that can be inserted or removed from the network by switching the thyristors at appropriate angles. A small

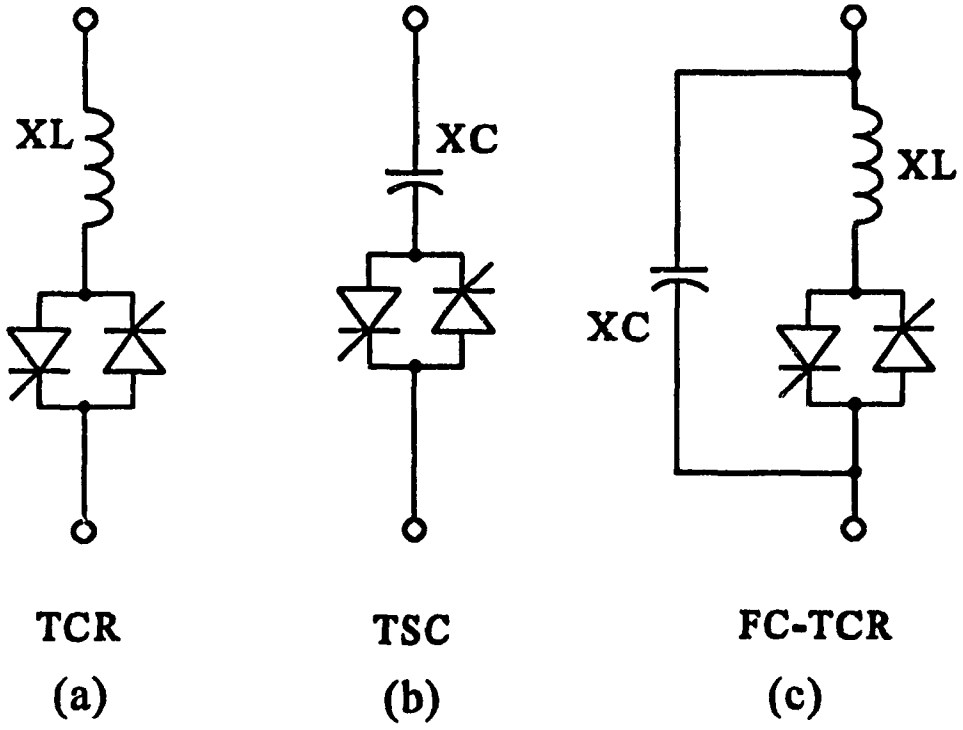

Fig. 1.5 - Common topologies for thyristor-controlled reactive elements used in power system compensators.

inductor is usually used in series with the capacitor to limit overcurrents during turn-on transients. The switches are fired when the difference between the capacitor and the line voltages is minimum, in this way reducing potentially harmful current surges in the TSC. This restriction eliminates the possibility of controlling the TSC by delaying the firing angle, as used in the TCR case. Therefore, the TSC can only provide a discrete control given by its total insertion or total removal of the network. An approximate continuous variation of the reactance can be achieved by grouping in parallel a number of units identical to the one shown in Fig. 1.5.b, and the smoothness of the control is solely limited by the number of units in the bank [19,20].

The FC-TCR shown in Fig. 1.5.c can provide a continuous variable capacitive/inductive reactance, therefore combining the advantages of both the TCR and the TSC. The equivalent reactance can vary from the maximum capacitive value of X_C when the TCR is off, to the maximum inductive reactance given by $X_L - X_C$ when the TCR in fully inserted.

The main drawbacks of switched reactance compensators are the large size of the reactive elements, the large amounts of harmonics injected in the line (TCR and FC-TCR), and the unavailability of a smooth control (TSC). Also, due to the cycle-by-cycle switching approach they do not provide a good dynamic response.

Voltage unbalance compensation can be achieved by means of switched reactances by controlling independently the injection in each phase. These compensators however have been used only in load unbalance compensator. For example, a dynamic compensation of the load unbalance by means of a static converter was proposed by Grandpierre et al in 1977 [21].

A shunt line-commutated thyristor controlled reactor (TCR's) was used to balance the line current of an unbalanced load. The control technique was based on a detection of the symmetrical components of the line current and their use to generate the appropriate firing angles to the converter.

1.3.2.3 Static VAR Compensators

With the advent of high-power/high-speed semiconductor controllable switches, several high-performance shunt connected static VAR compensators have been proposed, achieving a much better performance than their predecessors, the switched reactors and capacitors. By using a high-frequency high-performance modulation technique with an appropriate control strategy these compensators can provide high efficiency, very fast dynamical response, and a considerable reduction in number and volume of the magnetic elements [10,22-25].

Fig. 1.6 shows the two main topologies used in static VAR compensators, the voltage source (VS-VAR) and the current source VAR (CS-VAR) compensators. The VS-VAR type is implemented with a voltage source inverter or a current source inverter with a voltage control loop, which gives to the compensator the voltage-source characteristics. The CS-VAR type is implemented with a current source inverter or a voltage source inverter with a current control loop, which gives to the compensator the current-source characteristics. Voltage regulation can be achieved with either type of VAR compensator. However due to the shunt connection, they require careful control and protection when operating with an

unbalance source. Moran *et al.* presented a series of high performance CS-VAR compensators and a detailed analysis of their operation under unbalanced voltage conditions [22-24]. The negative sequence impedance to the ground is normally very low, unless a large reactance is placed in series with the converter or with the source.

Moran *et al.* show that a VS-VAR compensator, in addition to performing power factor correction and harmonic suppression, can intrinsically compensate for voltage unbalances [25]. This can be seen in Fig. 1.6.b: the voltage in the load is clamped by the

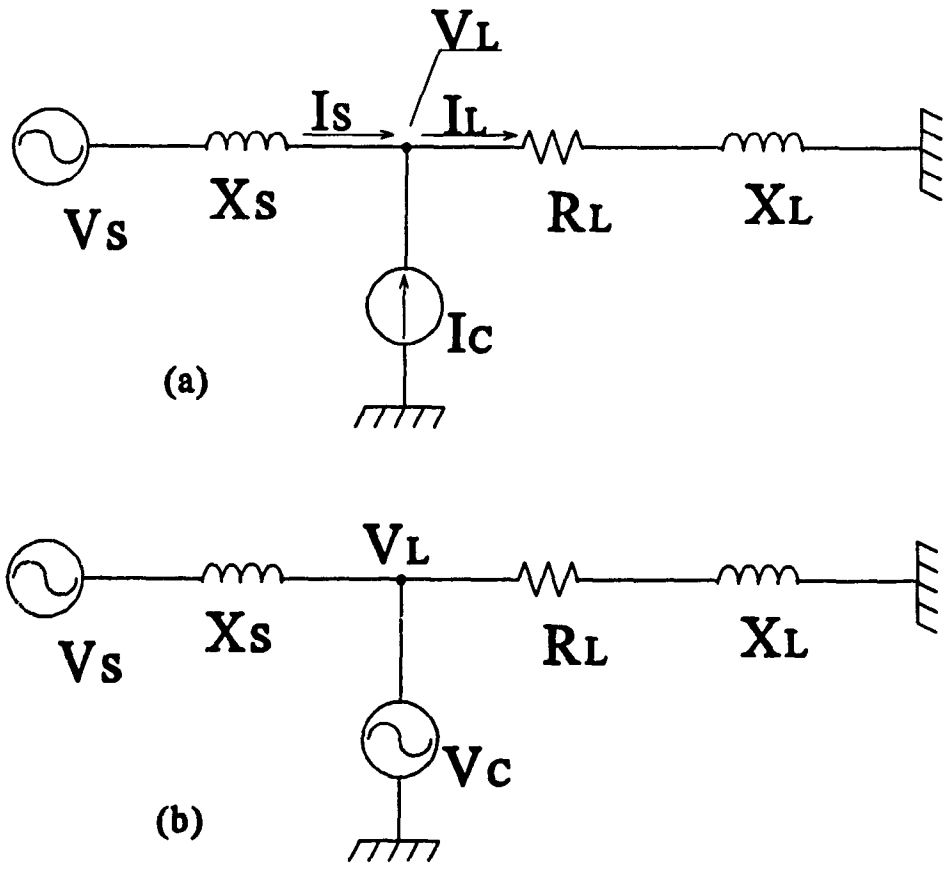

Fig. 1.6 - Main topologies of shunt VAR compensators. a) Current source, and b) voltage source types.

compensator's output voltage, and if the compensator generates only positive sequence voltages, it will act as a short-circuit for negative sequence components, buffering the load from the source unbalance. This feature however imposes penalties on the compensator, because it requires ratings capable of supporting the extra current generated by the negative sequence component of the source, which is only limited by the line reactance X_S. For example, for an unbalance of 0.1 pu and a source reactance of 0.1 pu, the additional current passing through the compensator is a negative sequence component of 1 pu.

1.3.3 Active series devices

Arrillaga *et al.* proposed a series connected converter for voltage control in transmission lines of three phase power systems. It is based on line-commutated thyristor-controlled ac-ac converters [26]. The converter is connected to the line by means of a series transformer, as shown in the Fig. 1.7. The amplitude and phase of the voltage across the secondary of the series transformer T1 is controlled by combining two voltage sources, one in-phase (V_d) and the other in quadrature (V_q) with the line voltage. The disadvantages of such a system are the high levels of harmonic injection and the high cost of the quadrature source, which has to be obtained from the power system through a costly and complex transformer configuration, shown in the Fig. 1.7 as T2. The same authors suggested, in more recent papers, a simplification to this scheme for cases where only one of the voltage components is required. As an example, they have shown that the use of a in-phase voltage boosting in substitution to the transformer on-load tap-changer, improves the operation of

HVDC links. The regulation of the dc link voltage is done in the ac side, and the ac/dc converter can be replaced by a diode rectifier.

High performance PWM-based series connected compensators have also been proposed in recent papers. In particularly Ooi *et al.* have presented series VAR compensators for power systems transmission lines. These compensators are based on a voltage source or current source inverter topology. Their principal aim is power system transmission and stability enhancement.

However these schemes have not been applied at the industrial level, for voltage unbalance compensation and voltage regulation. These applications, as presented in this

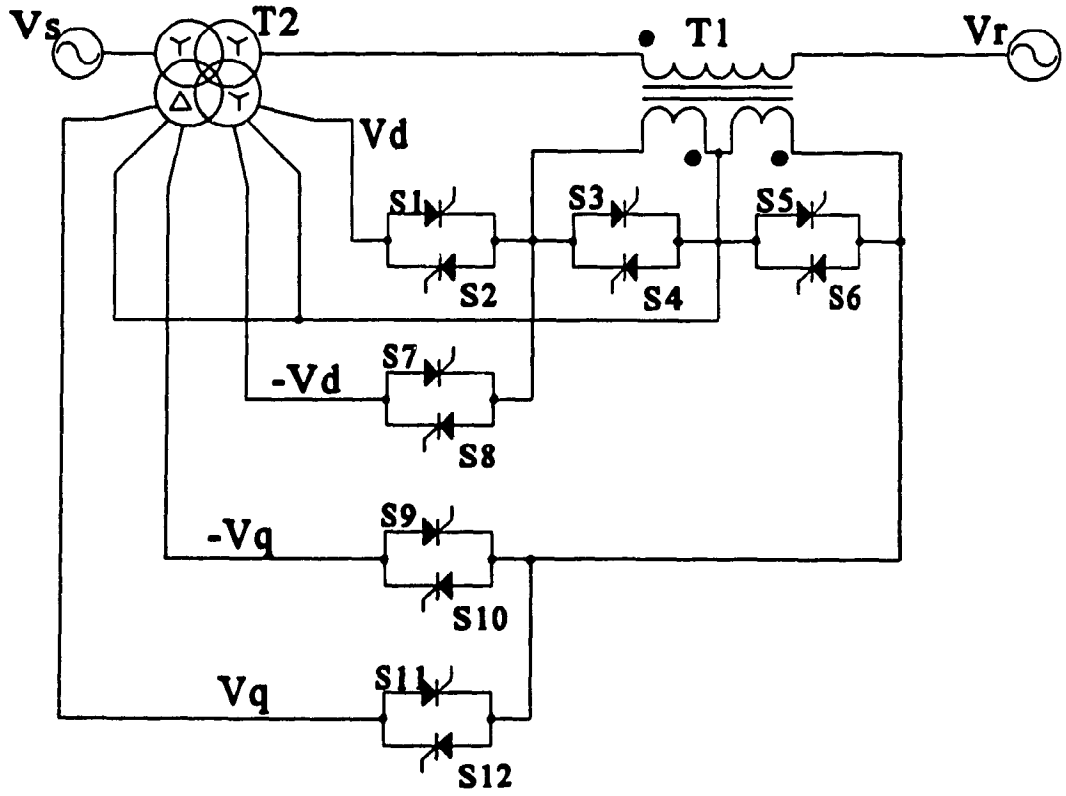

Fig. 1.7 - Circuit diagram of a four-quadrant voltage injector.

thesis are therefore new applications of series connected PWM converters.

The table 1.1 shows a qualitative comparison of the compensation techniques presented above, where their main characteristics are summarized.

1.4 Contributions

The scope of this thesis is to present, analyze, design, and verify by simulation and experimentally high-performance series-connected compensators for single and three-phase power systems. The compensators are based on voltage source inverter topology. Specific contributions are the following:

(a) The concept of ac voltage regulation using high-performance PWM-controlled static converters connected in series is introduced (chapter 2).

(b) The use of series compensators to obtain an easy and fast control of the power factor of reactive loads is demonstrated. This is a by-product of voltage regulation (chapter 2).

(c) An unbalance compensation technique using three single-phase series compensators with independent controls is introduced. It is shown that the load voltage can be regulated as well as balanced (chapter 3).

(d) A three-phase series compensator is shown to perform voltage unbalance compensation, by means of unbalanced switching function (chapter 4).

(e) A closed-form approach to calculate the required gating signals for unbalance operation of voltage source inverters is presented, and it is shown to be implementable with any carrier-based PWM technique (chapter 4).

Table 1.1 - Comparison of Basic Types of Compensation Techniques

Type *	ac-ac SCR	ac-ac PWM	Passive VAR	TCR	TSC	SVC
Voltage Regulation Capability	Yes	Yes	(Yes)	(Yes)	(Yes)	(Yes)
Voltage Unbalance Capability	Yes	Yes	No	(Yes)	(Yes)	(Yes)
Current Unbalance Capability	No	No	(Yes)	Yes	Yes	Yes
Input Power Factor	Poor	Medium	Good	Poor	Good	Good
Dynamic Response	Poor	Medium	Very poor	Poor	Poor	Very good
Input Current Harmonic Distortion	Poor	Medium	None	High	None	Low
Input filter	(Needed)	Needed	None	(Needed)	None	Small
Continuous Control	Yes	Yes	No	Yes	No	Yes
Output Voltage Harmonic Distortion	High	Medium	None	Poor	None	Good
Cost	Medium	High	Low	Medium	Medium	High
kVA	> 1 pu	> 1 pu	*	*	*	*

( ) - Indirect effect * - Application dependent.

(f) A method to control a three-phase compensator is described, with a mathematical analysis and implementation techniques based on a high performance digital signal processor (chapter 5).

(g) The concept of an instantaneous symmetrical components transformation is introduced, and used in the controller design in the unbalance compensators (chapter 5).

(h) The dynamic analysis of unbalanced three-phase systems is described, based on the instantaneous symmetrical transformation (chapter 5).

1.5 Summary of the thesis

This thesis is organized as follows.

Chapter 2 presents an alternative to the series ac voltage controller consisting of a low power series connected controlled auxiliary voltage source. It is implemented using a voltage source inverter connected in series with the ac supply through a transformer. A pulse-width modulation technique is used to provide a high quality output voltage, to reduce the size of the required filter, and to achieve a fast dynamic response. The proposed method is applicable when output voltage control over a wide range is not required, but rather voltage stabilization, and when a range for the input voltage can be specified. The use of a series connection allows a considerable reduction in the total power required to perform the regulation. However, four quadrant operation is necessary. The total kVA rating of the system is dependent on the maximum range allowed for the input voltage variations. When

the maximum compensation voltage is not required, and the system is supplying a reactive load, the remaining voltage regulation capacity can be used to improve the input power factor. This is achieved by injecting a voltage component in quadrature with the source voltage. This chapter includes a description of the principles of operation of two modes of operation, as a voltage regulator, and as a voltage regulator with power factor improvement. Simulation and experimental results of a 1.2 kVA prototype are presented to demonstrate the feasibility of the proposed system.

Chapter 3 proposes a series connected voltage compensator, for unbalanced three phase sources, consisting of three single phase voltage source inverters. The inverters are connected to the power system through a transformer. The negative sequence component of the supply line voltage is extracted and eliminated from the source. The amplitude of the positive sequence is then adjusted to obtain a regulated output. The use of pulse-width modulation (PWM) results in a system with faster dynamic response than the ac controllers. Also because of the high switching frequency used, the system allows a considerable reduction in the power rating of the required filter. Another advantage of the proposed method is the low power rating of the inverters.

Chapter 4 presents an alternative topology for the unbalance compensator of Chapter 3. It is based on series connected force commutated three phase converter. It overcomes the disadvantages of conventional thyristor compensators, and at the same time it reduces the number of switches and the magnetic volume, compared to the compensator presented in Chapter 3. The voltage unbalance present in three phase ac supplies is eliminated with a low kVA series connected compensator, consisting of one three-phase voltage source inverter

connected to the power system through a transformer. The negative sequence component of the supply line-to-line voltage is extracted and eliminated from the input voltage, reducing the load voltage to a balanced system with amplitude given by the positive sequence. It is shown that by having the inverter operate with unbalanced switching functions it is also possible to control the amplitude of the positive sequence component. This allows the system to also perform load voltage regulation. The use of pulse-width modulation (PWM) results in a system with fast dynamic response, and the possibility of using a high switching frequency allows a considerable reduction in the power rating of the required filter.

Chapter 5 describes a method for the dynamic analysis of unbalanced networks and the design of controllers working in such conditions. The first step consists in partitioning the system under analysis in its symmetrical sequence equivalents. The result is a set of balanced networks corresponding to the zero, the positive and the negative sequence components, which are then analyzed using a dq transformation. In order to implement this technique, it is necessary to define of a time-domain (instantaneous) symmetrical sequence transformation, which is based in the concept of space-vectors used for some time in the ac machines control. The method is applied to the analysis of the dynamic response of a series-connected voltage unbalance compensator, and to the design of its control loops.

Appendix A describes a digital calculator capable of extracting the positive and the negative sequence components of the line-to-line voltages of ac systems in real-time. The calculator's hardware implementation consists of a fast Digital Signal Processor connected to a 16 bits A/D, both using one PC as a development station. The software responsible to the calculation procedure implements a reduced radix-2 DIF FFT algorithm to extract the

fundamental time-varying phasors related to the line-to-line voltages. These values are used to calculate the symmetrical sequence components. Enough processing free time is left to allow the implementation of almost any control procedure. The algorithm, allied with some special implementation techniques, give the system a faster transient response than techniques mentioned in the literature. The transient response time is within one cycle of the ac supply. The standard FFT algorithm is simplified in order to reduce the processing time, requiring only one complex multiplication per sample.

CHAPTER 2

SERIES CONNECTED PWM VOLTAGE REGULATOR FOR SINGLE PHASE AC SOURCES

2.1. Introduction

This chapter presents an alternative to the series ac voltage controller, combining some advantages of the methods mentioned in the introduction. The system consists of a low power series connected controlled auxiliary voltage source, which is implemented by using a voltage source inverter (VSI) connected in series to the ac supply through a transformer. A pulse-width modulation (PWM) technique is used to provide a high quality output voltage, to reduce the size of the required filter, and to achieve a fast dynamic response.

The proposed method is applicable when output voltage control over a wide range is not required, but rather voltage stabilization is important and the range of the input voltage can be specified. This is not a limitation in a wide range of applications like ac stabilizers for computer systems, sensitive laboratory instruments, and biomedical equipment, where the main concern is voltage stabilization and not voltage control. This constraint and the use of a series connection allow a considerable reduction in the total power required to perform the regulation. Thus, the total kVA rating of the system is dependent on the maximum range allowed for the input voltage variations where 20% is a commonly accepted range.

When the maximum compensation voltage is not required, and the system is supplying a reactive load, the remaining voltage can be used to improve the input power factor. This is

achieved by injecting a voltage component in quadrature with the source voltage.

This chapter describes two modes of operation of the proposed circuit: as a voltage regulator, and as a voltage regulator with power factor improvement. Also presented are design curves, design equations, and a design example. Simulation and experimental results of a 1.2 kVA prototype are presented to demonstrate the feasibility of the proposed system.

2.2. Principle of Operation

In order to describe the principle of operation of the proposed compensator, its topology is simplified to an ideal single-phase ac voltage source, that allows independent control of its amplitude and phase. The compensator is placed in series with the systems, between the ac mains and the load, as shown in Fig. 2.1.

With the compensator placed as shown, and with total control over its amplitude and phase, it is possible to make it perform a variety of tasks, among them load voltage control for both active and reactive voltage drops, input power factor control (source side), VAR

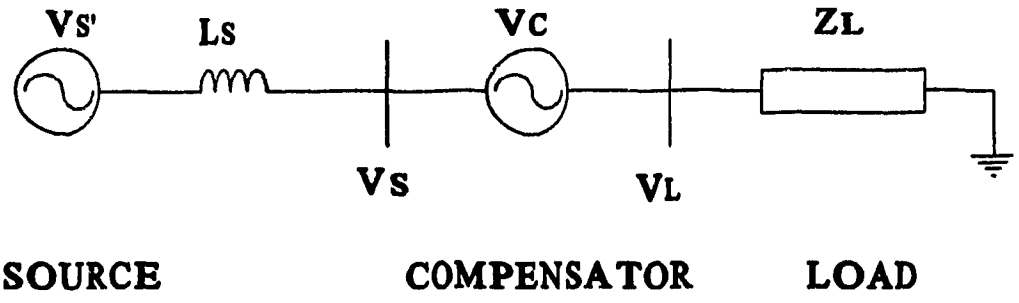

Fig. 2.1 - Simplified diagram of a series compensator.

compensation, inrush current limitation in reactive loads, and buffering transients for electrical machines. As an example, by synchronizing the compensator with the source voltage V_S, and maintaining its phase zero, it is possible to regulate the load voltage V_L to a required reference value.

2.2.1 Voltage Regulation

The basic concept of the proposed system is illustrated by means of a simplified model where the series connected compensation voltage source is assumed ideal, without harmonics and null impedance, as shown in Fig. 2.1.The compensation voltage source V_C is placed in series with the ac supply, between the source and the load. With this procedure, voltage regulation in the load can be achieved by controlling the amplitude and the phase of the voltage of the auxiliary source V_C.

For a given source voltage $\vec{V}_S$ and a required load voltage $\vec{V}_L$, a correction voltage $\vec{V}_C$ can be obtained by,

$$\vec{V}_C = \vec{V}_L - \vec{V}_S = (1 - \vec{MF}) * \vec{V}_L \qquad (2.1)$$

where MF is the magnitude factor. given by,

$$\vec{MF} = \frac{\vec{V}_S}{\vec{V}_L} = (1 - ME)\angle\theta \quad \text{pu} \qquad (2.2)$$

and ME is the magnitude error in voltage.

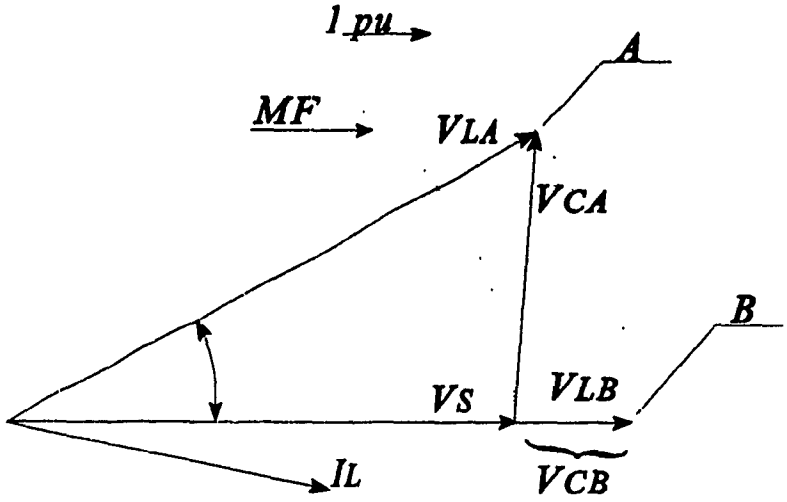

Fig. 2.2 - Principles of voltage regulation.

A phasor diagram for this technique is shown in Fig. 2.2. For a given source voltage, it is required a load voltage of one pu. The locus of solutions for this compensation is the circle of one pu, where two of the infinite solutions are shown as A and B. The solution B requires a minimum of voltage injection, which is translated in to a minimal apparent power from the compensator. This solution requires the synchronization of the compensator to the ac source, by maintaining the compensation voltage $\vec{V}_c$ in-phase with the line voltage $\vec{V}_s$.

This approach simplifies the control of the system by reducing the equation (2.1) to the following scalar expression.

$$V_c = (1 - |\vec{MF}|) = ME \qquad \text{pu} \qquad \textbf{(2.3)}$$

2.2.2 Power Factor Improvement

The use of a voltage source inverter to implement the auxiliary source V_C gives full control over the amplitude of the correction voltage as well as its phase with respect to a given reference. As shown in the previous section, voltage regulation requires a controlled amplitude of $\vec{V}_C$, which means that any point over the circle of one pu, in Fig. 2.2, is a solution for the regulation problem. Thus the input voltage phasor $\vec{V}_S$ can be phase-shifted with respect to $\vec{V}_L$ to any value, respecting the limitations in power. This procedure can be used to correct or at least to improve the system's input power factor. When supplying a reactive load and the full correction voltage is not used by the regulation procedure, it is possible to use the remaining margin of $\vec{V}_C$ to perform input power factor improvement.

There are two possible operating conditions, depending on the load power factor $\cos(\phi_L)$ and on the maximum value of the angle between the source and the load voltages θ_{max}. If $\cos(\phi_L) \geq \cos(\theta_{max})$, it is possible to achieve total power factor correction, and if $\cos(\phi_L) \leq \cos(\theta_{max})$ only power factor improvement can be achieved. The angle θ_{max} is calculated by the following expression.

$$\cos(\theta_{max}) = \frac{1 + |\vec{MF}|^2 - ME_{max}^2}{2 \cdot |\vec{MF}|} \qquad (2.4)$$

Where ME_{max} is the maximum error in voltage the compensator can accept. Both cases are shown in Figs. 2.3 and 2.4 with ME_{max}=20% and MF=0.85.

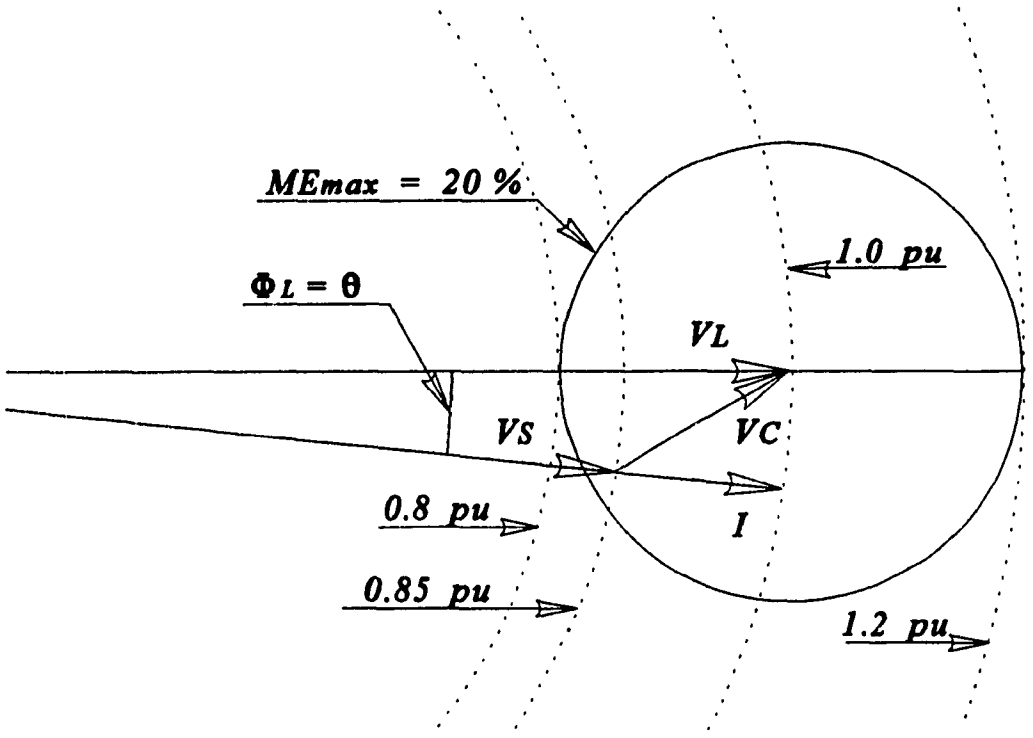

Fig. 2.3 -Voltage regulation & power factor correction (MEmax = 20%, ME = 15%).

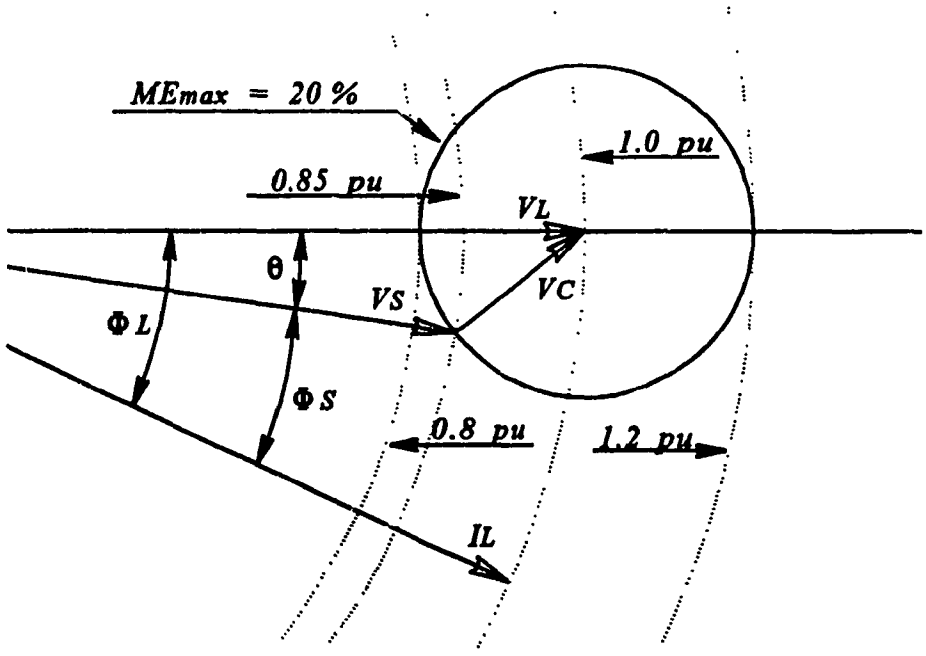

Fig. 2.4 - Voltage regulation with power factor improvement (MEmax = 20% and ME = 15%).

The phase angle between the source and the load voltages is defined by,

$$\theta = \min(\theta_{max} ; \phi_L) \tag{2.5}$$

With the position of $\vec{V}_s$ defined it is possible to calculate the components of the required correction voltage with respect to the source voltage (used reference phasor).

$$V_{CX} = \cos(\theta) - |\vec{MF}| \qquad \text{pu} \tag{2.6}$$

$$V_{CY} = \sin(\theta) \qquad \text{pu} \tag{2.7}$$

Finally, the input power factor is given by the following expression.

$$\cos(\phi_S) = \cos(\phi_L - \theta) \tag{2.8}$$

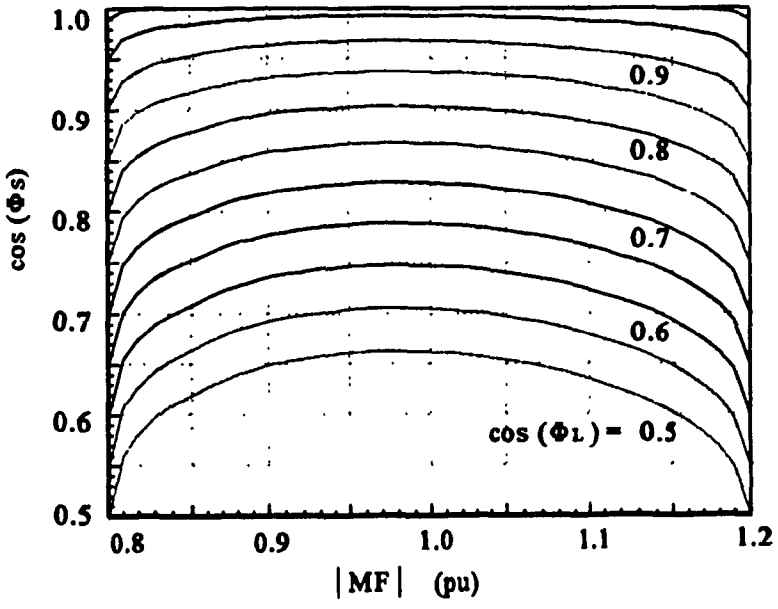

Fig. 2.5 - Source power factor as function of $|MF|$ and the load power factor (for $ME_{max} = 0.2$).

Fig. 2.5 shows the relation between the input power factor cos (ϕ_S) and the magnitude factor MF for some values of the load power factor cos (ϕ_L), and for $ME_{max} = \pm 20\%$.

2.3. Power requirements

In order to understand the boundaries of the compensation scheme, consider the system presented in Fig. 2.6, where a typical case of industrial power system is shown. The source V_i is assumed ideal (infinite bus) and the reactance of transmission lines, transformers, etc, are represented by X_i.

The PCC (point-of-commom-connection) bus supports two loads, the one given by I_{LO}, and the compensator branch. Between the PCC bus and the compensator a reactance (X_S) is used to model transformers, transmission lines, etc. The compensator is required to maintain the voltage at the load (V_L) constant and equal to one pu.

There are basically two control approaches to achieve this goal, through VAR

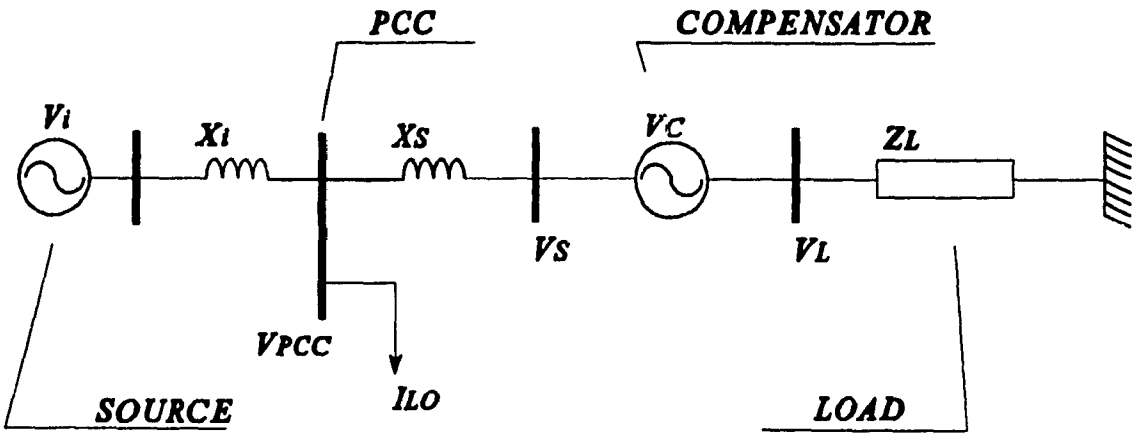

Fig. 2.6 - Simplified diagram of a series compensator.

compensation and by using minimum apparent power, and both cases can be analyzed by calculating the power requirements for the compensator. The apparent power required by the regulator is calculated by,

$$\vec{S}_C = \vec{V}_C \cdot \vec{I}_L^{\,*} = \vec{V}_L \cdot \vec{I}_L^{\,*} \cdot (1 - \vec{MF}) \tag{2.9}$$

$$\vec{S}_C = \vec{S}_L \cdot (1 - \vec{MF}) \tag{2.10}$$

where $\vec{S}_C$ is the compensator power and $\vec{S}_L$ is the load power. This equation can be separated into real and reactive power as follows.

$$P_C = S_L * [\cos(\phi_L) - |\vec{MF}| * \cos(\phi_S)] \tag{2.11}$$

$$Q_C = S_L * [\sin(\phi_L) - |\vec{MF}| * \sin(\phi_S)] \tag{2.12}$$

where cos (ϕ_L) is the load power factor and cos (ϕ_S) is the ac source power factor.

By maintaining P_C approximately zero the regulator can work as a self-controlled dc bus reactive power compensator, which is an attractive setup since the regulator does not require a dc supply. Fig. 2.7 presents an example of voltage regulation by reactive power compensation for a load power factor equal to 0.8, lagging, and for two cases of source voltage, 0.9 pu (point B) and 1.2 pu (point A).

The condition for reactive compensation is satisfied when, from (2.11),

$$\cos(\phi_S) = \frac{\cos(\phi_L)}{|\vec{MF}|} \tag{2.13}$$

which has solutions in the real domain only for $|\vec{MF}| \geq \cos(\phi_L)$. This means that for undervoltage conditions the range of voltage regulation is limited by the load power factor. In the example shown in Fig. 2.7 any voltage reduction to a value lower than 0.8 cannot be corrected by means of reactive power only. This is the case of voltage drops caused by the parallel current I_{LO} over the reactance X_i in Fig. 2.6. Another major drawback of this technique is the power rating of the regulator. Despite the fact the regulator has to supply

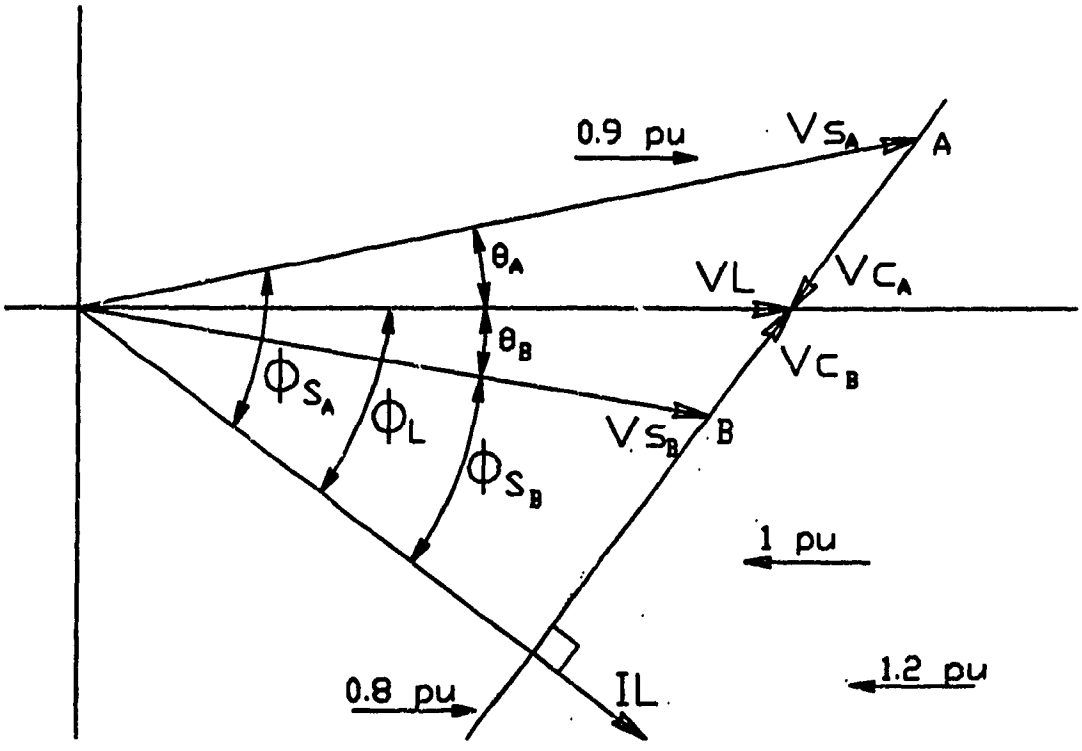

Fig. 2.7 - Voltage regulation by reactive compensation.

only reactive power, its power rating can be large. For example, for ME_{max} = 20% the regulator power rating is 0.66 pu, for a unity load power factor and a source overvoltage of 20% ($|\vec{MF}|$ = 1.2). Due to these limitations, voltage regulation by means of a series reactive power compensator alone is feasible only for reactive voltage drops in the line leading directly to the load (the compensator branch in Fig. 2.6); in general it cannot compensate for reactive drops created in the line by currents drawn by loads connected in parallel with the load/compensator system (I_{LO} in Fig. 2.6), unless this current is in phase with the compensator's current, which is not the most probable situation. In this case real power becomes necessary.

Thus when using the compensator with parallel paths, as in the case of an industrial plant shown in Fig. 2.6, it will not be able to regulate the load voltage for any condition, if the voltage at the point of common coupling (PCC) is not already regulated.

Because of these constraints, it is suggested a method that minimizes the total power (both real and reactive) instead of zeroing only the real power. This procedure minimizes the regulator power ratings and provides a way to regulate the load voltage for any condition of voltage drop, provided it is inside the specified limits. This is obtained by maintaining the phase of $\vec{MF}$ equal to zero, meaning that the load and the source voltages are in phase, requiring a regulator capable of supplying reactive as well as real power. The advantage of the method is that the rated power can be reduced to values in the range of the reactance X_s (in pu), which is usually around 0.2 pu.

Also, because most of the voltage drop is reactive, it is possible to define different

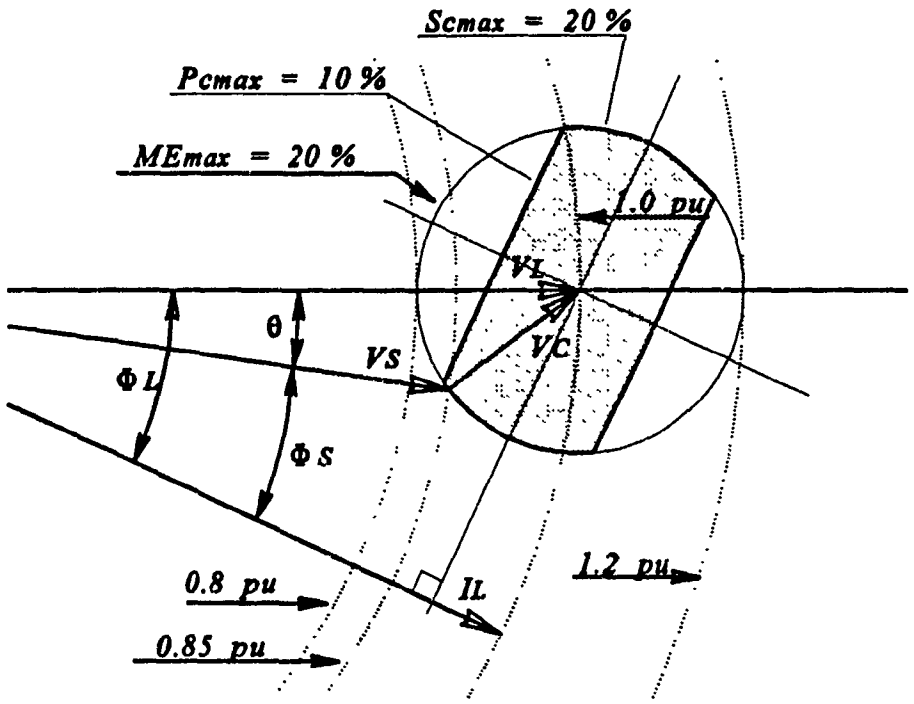

Fig. 2.8 - Voltage regulation with power minimization.

ratings for the reactive power and the real power the compensator can supply/absorb. The minimization of the real power is an interesting approach , since this parameter defines the size and the cost of the dc power supply (see item 2.5.4).

Fig. 2.8 shows the phasor diagram of a compensator with ME_{max} = 0.2 and ME = 0.15, supplying a load with a power factor of 0.8, lagging. This diagram is similar to the one in Fig. 2.4, but with one difference: the limit for real power (Pc_{max}) is now reduced to 0.1 pu, reducing the size and cost of the dc source. The shaded area in Fig. 2.8 is the locus of operation of the compensator. Any voltage phasor inside this area can be compensated to reach 1 pu.

2.4. Circuit Description

Fig. 2.9 shows the power circuit of the proposed regulator. The main element is a single phase voltage source inverter (VSI) with outputs connected to the ac supply through a transformer. The inverter is built using a single-phase bridge configuration with bipolar power transistors and anti-parallel diodes as main switches. The inverter is controlled using a carrier-based sine PWM, but any modulation technique can be used. The output harmonics generated by the inverter are attenuated by a second order LC filter, providing a low THD voltage (less than 5%) to the series transformer. When voltage regulation alone is required,

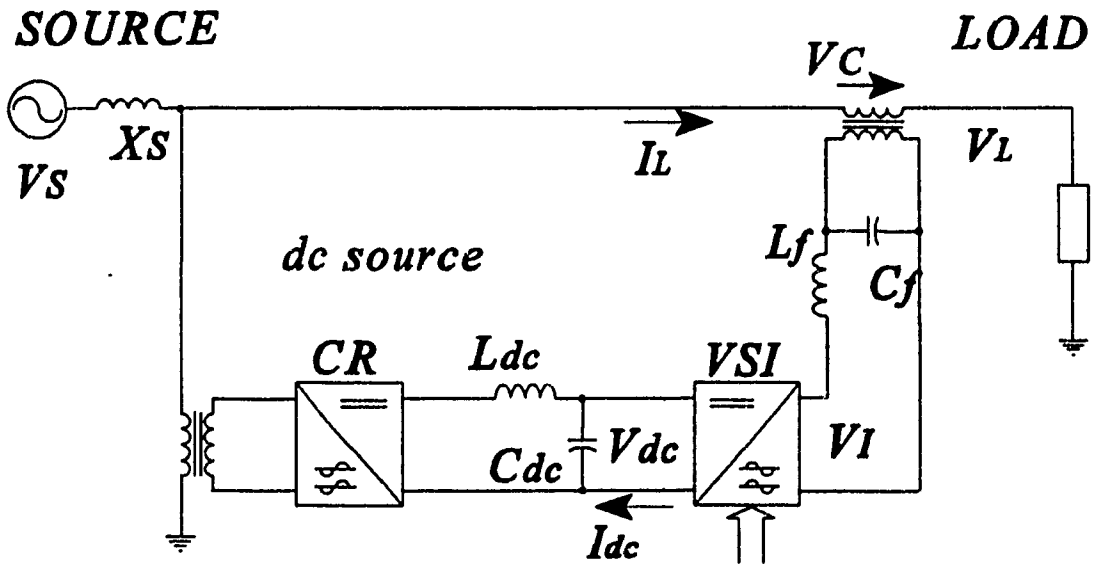

Fig. 2.9 - Circuit diagram of the proposed ac regulator.

the inverter is controlled by the modulation index, with the PWM pattern of the inverter output being in phase with the ac source. In the case of power factor improvement, phase control of V_C is also necessary. The control subsystem (not shown) should provide the required set of references to the modulator, according to (2.3) or (2.6) and (2.7), to maintain the load voltage equal to a specified reference.

The dc power supply shown in Fig. 2.9 is only necessary when the compensator is required to supply real power. It consists on a single-phase transformer, a rectifier, and a dc bus filter. The ratings of this supply are defined in accord with the application requirements for real power. The general case, to provide the required V_C at any load power factor, the compensator requires a dc source with current regeneration capabilities, which can be implemented using a PWM rectifier. In the circuit presented as example, only one quadrant operation was used, which simplifies the dc source to a diode rectifier. The dc bus second order filter is designed to reduce the ripple in the voltage to less than 5%.

2.5. Circuit Design

The starting point for designing the compensator is the establishment of a maximum source voltage variation (ME_{max}) which the regulator will be capable to compensate, and the maximum real power it should be allowed to supply/absorb. The maximum voltage variation ME_{max} is defined by the utility standards, and by the application requirements. A common value is ±20%, which means the regulator can be designed to be capable of compensating for undervoltages from 80% to overvoltages up to 120%. The maximum real power is defined

by the application, as shown in the item 2.3. For design purposes it is considered the general case of four quadrants operation (supply/absorb real and reactive power).

The following assumptions are used in this design.

i) The switches are assumed ideal.

ii) The filter components are ideal.

iii) The base value for the power (S_{BASE}) is the rated load power.

iv) The base value for the voltage (V_{BASE}) is the infinite bus line-to-neutral voltage.

v) The base voltage in the inverter side (Vi_{BASE}) is calculated using the series transformer turns ratio.

2.5.1. Series Transformer Design

The basis for designing the main transformer is the maximum source voltage variation (ME_{max}). With this parameter defined, the transformer power rating, primary and secondary voltage are given in pu by,

$$S_T = V_{T_{prim}} = V_{T_{sec}} = ME_{max} \quad \text{pu} \qquad (2.14)$$

The actual value of the primary voltage is given by the dc bus voltage (V_{dc}) and by the gain of the PWM technique (G_i) being used in the VSI. Using the actual value for V_{dc}, the transformer turns ratio is calculated by,

$$a = \frac{N_2}{N_1} = \frac{ME_{max} * V_{base}}{V_{dc} * G_i} \qquad (2.15)$$

The rated transformer current is 1 pu.

2.5.2. Inverter's Design

The design of the inverter consists in the specification of the topology to be used, the modulation technique, the type and parameters of the switches.

With respect to the topology, a single-phase full-wave bridge voltage source inverter was chosen, basically due to its simplicity and reasonable performance. The inverter is controlled using a sine pulse-width modulation technique (SPWM). This is an arbitrary choice because any modulation technique can be applied to this compensator.

Assuming the filter is properly designed no current harmonics will pass through the inverter, thus the current in any switch is very close to sinusoidal. The current ratings for the switches are then,

$$\left\{ \begin{array}{l} I_{SW_{rms}} = \frac{1}{\sqrt{2}} \\ I_{SW_{pk}} = \sqrt{2} \\ I_{SW_{avg}} = \frac{1}{\pi} \end{array} \right\} \quad \text{pu} \qquad (2.16)$$

The voltage rating is given by the dc bus voltage as follows.

$$\begin{Bmatrix} V_{SW_{rms}} = \frac{1}{\sqrt{2}} \cdot \sqrt{\sum_{n=1}^{\infty} (V_{L_n})^2} \\ V_{SW_{pk}} = V_{dc} \end{Bmatrix} \quad \text{pu} \quad (2.17)$$

The apparent power required from the inverter is higher than the one in the transformer due to the presence of harmonics in the output voltage, and it is given by,

$$S_I = \sqrt{\sum_{n=1}^{\infty} (V_{L_n})^2} \quad \text{pu} \quad (2.18)$$

2.5.3. Inverter's Filter Design

The inverter's output filter is designed taking as constraints the total harmonic distortion for the current in the inductor and the voltage in the load, defined as follows.

$$THD_i = \frac{I_H}{I_1} = \frac{\sqrt{\sum_{n=2}^{\infty} [I_n]^2}}{I_1} \quad (2.19)$$

Where I_1 is the rms value of the fundamental component, I_H is the rms value of the harmonics, and I_n is the rms value of the n-th harmonic of the line current.

$$THD_v = \frac{V_H}{V_1} = \frac{\sqrt{\sum_{n=2}^{\infty} [V_n]^2}}{V_1} \quad (2.20)$$

Where V_1 is the rms value of the fundamental component, V_H is the rms value of the

harmonics, and V_n is the rms value of the n-th harmonic of the line-to-neutral voltage.

In order to design the filter, the system shown in Fig. 2.9 is simplified to the equivalent shown in Fig. 2.10. The inverter's output voltage and the load current are modelled by their harmonic component, specified by the index *n*.

Using the Norton equivalent for the inverter and inductor L_f, the equivalent current harmonic is given by,

$$I_{L_n} = \frac{V_{L_n}}{n \cdot XL_f} \qquad n = 2,..,\infty \tag{2.21}$$

Taking into consideration that most of the voltage harmonics generated in the inverter (V_{In}) will appear across the inductor L_f, the total rms of the harmonics components of I_1 is,

$$I_{L_H} = \frac{1}{XL_f} \cdot \sqrt{\sum_{n=2}^{\infty} \left(\frac{V_{L_n}}{n}\right)^2} \tag{2.22}$$

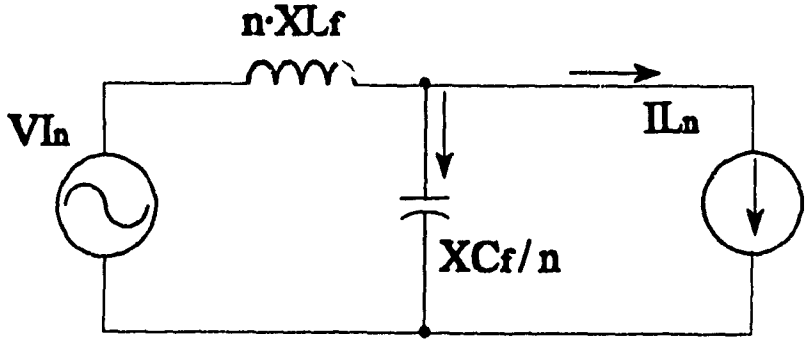

Fig. 2.10 - Equivalent circuit used for designing the inverter's output filter.

Substituting in (2.22) the definition of THD_i, it is possible to get the expression for the reactance of L_f, as follows.

$$XL_f = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n}\right)^2}}{THD_i} \quad \text{pu} \qquad (2.23)$$

In order to calculate XC_f it is assumed that all current harmonics pass through C_f. The harmonics of the voltage across the capacitor are then,

$$V_{C_n} = I_{I_n} * \frac{XC_f}{n} = \frac{XC_f}{XL_f} * \frac{V_{I_n}}{n^2} \qquad n=2,..,\infty \qquad (2.24)$$

Using this expression it is possible to calculate the total rms value for these harmonics.

$$V_{C_H} = \frac{XC_f}{XL_f} * \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n^2}\right)^2} \qquad (2.25)$$

Substituting this expression in the definition of THD and using the relation between THD_{VC} and THD_{VL} given by (2.26), an expression for XC_f is obtained, as shown in (2.27).

$$THD_{VC} = \frac{V_{C_{harm}}}{V_{C_1}} = \frac{V_{C_{harm}}}{ME_{max}} = \frac{THD_{VL}}{ME_{max}} \qquad (2.26)$$

$$XC_f = \frac{XL_f * THD_{VL}}{\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n^2}\right)^2}} \quad \text{pu} \qquad (2.27)$$

Figs. 2.11and 2.12 present the design relations for XL_f and XC_f (equations (2.23) and

(2.27)) obtained for ME_{max}= 20% and for a SPWM bridge voltage source inverter at unity modulation index.

The kVA ratings for both C_f and L_f are calculated from (2.28) and (2.29), respectively.

$$SC_f = \frac{ME_{max}}{XL_f}\sqrt{(1 + THD_{VL}^2)\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n}\right)^2} \quad pu \qquad (2.28)$$

$$SL_f = \sqrt{(1 + THD_i^2)\sum_{n=2}^{\infty}(V_{I_n})^2} \quad pu \qquad (2.29)$$

Fig. 2.13 shows (2.28), for the same conditions given for Fig. 2.11. For low values of THD_i and THD_{VL} (2.29) is approximately constant, and for the same conditions, is equal to 0.096 pu.

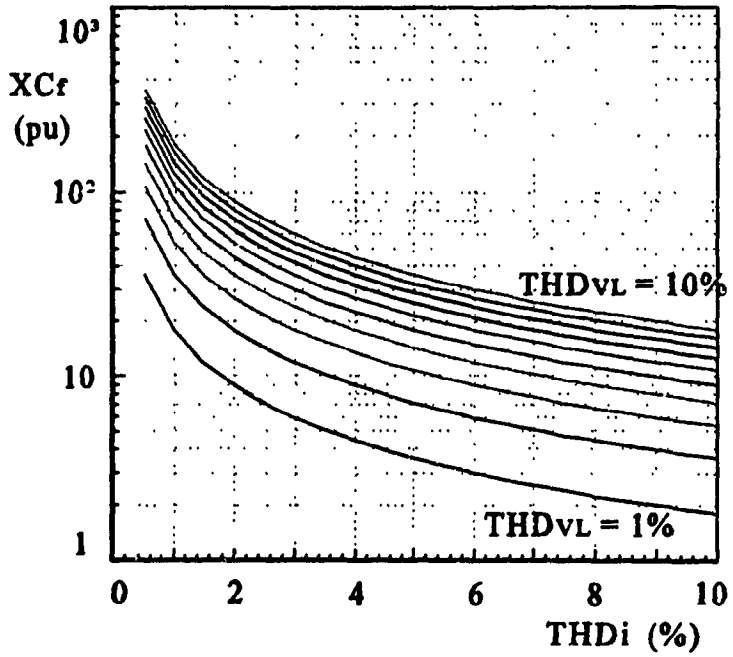

Fig. 2.11 - Inverter's filter design - Capacitor reactance

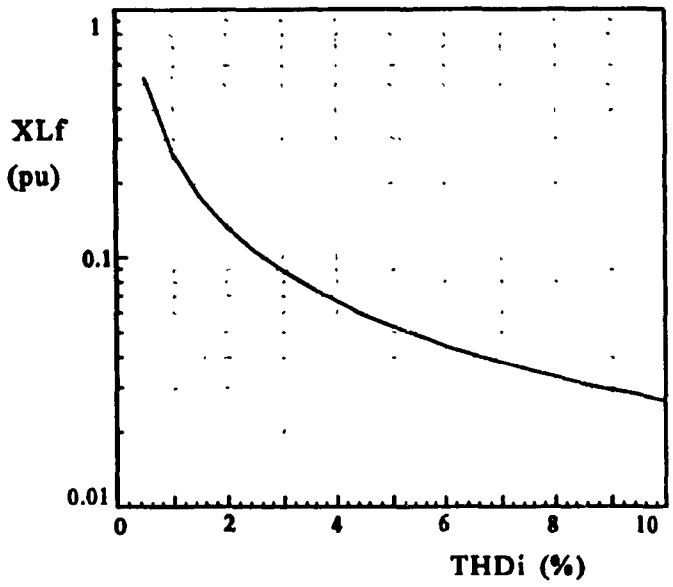

Fig. 2.12 - Inverter's filter design - Inductor reactance.

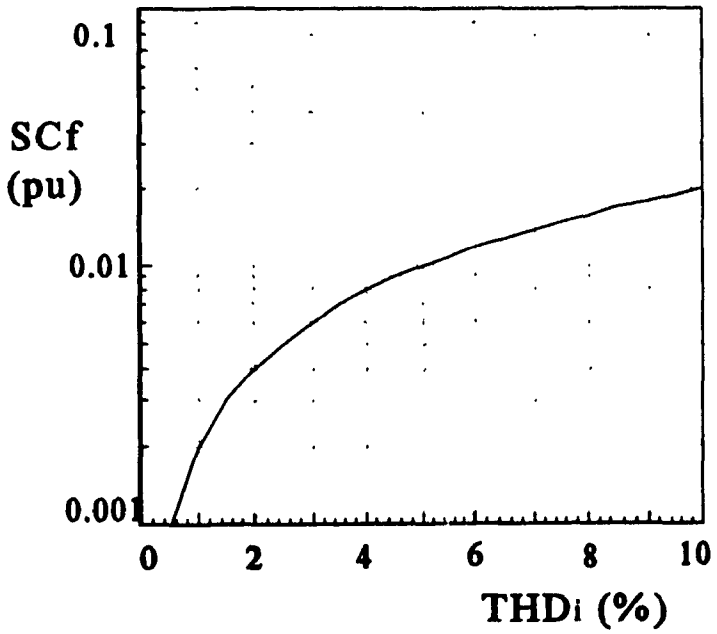

Fig. 2.13 - Inverter's filter design - Capacitor power ratings.

2.5.4. Dc Source Design

The dc source consists of a transformer, a rectifier and a filter, conected as shown in Fig. 2.14.

The design of the dc source depends on the desired mode of operation of the compensator. The general case, operating in four quadrants (supply/absorb real and reactive power), the compensator requires a dc source capable of operate in two quadrants.

The starting point for the design of such a circuit is the definition of the amount of real power the compensator will be allowed to provide to the system (Pc_{max}). As already mentioned in the item 2.3, if the real power is made zero, the compensator becomes a series var compensator, and the dc source is not necessary. In this case the dc bus can be supported by the inverter using slight phase-shifts of the voltage with respect to the load current. The real power necessary to maintain the dc bus is supplied/absorbed from the ac mains.

When real power is required to perform the compensation, the dc source becomes

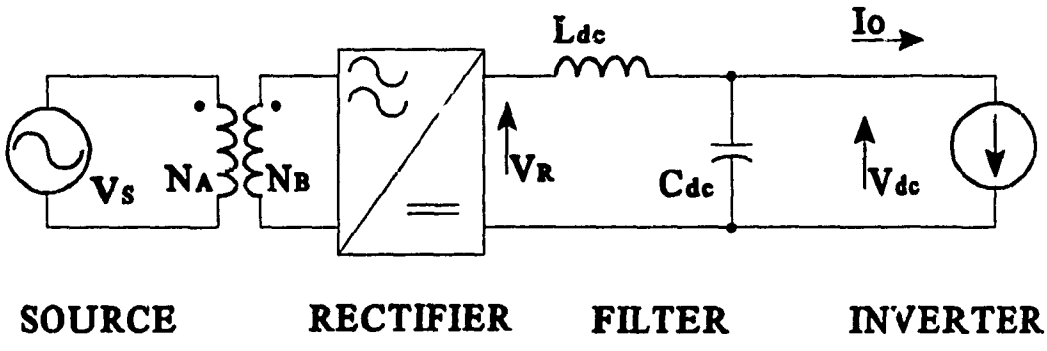

Fig. 2.14 - Equivalent circuit used for designing the dc source.

necessary, and its power ratings is defined by the value and the phase with respect to the line current of the error voltage the compensator should eliminate. For the worst case, the maximum real power is given by the kVA ratings of the compensator (eqn. (2.14)).

If the compensator is required only to **supply** real power, as in the proposed example, the dc source does not need to regenerate current, thus a diode rectifier can be used to implement it. In this case the ratings for the rectifier are,

$$\left\{ \begin{array}{l} V_{SW_{rms}} = \frac{\pi}{4} V_{dc} \\ V_{SW_{pk}} = \frac{\pi}{2} V_{dc} \\ V_{SW_{avg}} = \frac{V_{dc}}{2} \end{array} \right\} \quad \text{pu} \qquad (2.30)$$

$$\left\{ \begin{array}{l} I_{SW_{rms}} = \frac{\sqrt{K_i^2 + 1}}{\sqrt{2}} \cdot \frac{P_{dc}}{V_{dc}} \\ I_{SW_{pk}} = \sqrt{2} \cdot \sqrt{K_i^2 + 1} \cdot \frac{P_{dc}}{V_{dc}} \\ I_{SW_{avg}} = \frac{P_{dc}}{2\ V_{dc}} \end{array} \right\} \quad \text{pu} \qquad (2.31)$$

Where P_{dc} is the required real power (equal to Pc_{max}), V_{dc} is the rated dc bus voltage, and K_i is the maximum current ripple in the inductor L_{dc}.

The apparent power required from the rectifier is,

$$S_R = \frac{\pi \cdot \sqrt{K_i^2 + 1}}{2\sqrt{2}} \cdot P_{dc} \qquad (2.32)$$

The transformer ratings are,

$$\begin{cases} S_T = S_R = \dfrac{\pi \cdot \sqrt{K_i^2 + 1}}{2\sqrt{2}} \cdot P_{dc} \\ V_{T_B} = V_m = \dfrac{\pi}{2\sqrt{2}} \cdot V_{dc} \\ V_{T_A} = V_S \\ \dfrac{N_B}{N_A} = \dfrac{\pi}{2\sqrt{2}} \cdot \dfrac{V_{dc}}{V_S} \end{cases} \tag{2.33}$$

2.5.5. Dc bus Filter Design

The design of the dc bus filter is similar of the inverter's output filter. The major difference is that the parameters used as basis for are the ripple factor in the dc bus voltage and the break frequency of the filter. The ripple factor is defined as,

$$K_v = \frac{V_H}{V_{dc}} \tag{2.34}$$

Where V_H is the rms value of the harmonics of the dc bus voltage, and V_{dc} is the dc bus average voltage.

First, using the Norton theorem on the rectifier and the inductor, the equivalent current source can be calculated as,

$$I_{L_n} = \frac{V_{R_n}}{n * XL_{dc}} \qquad n = 2,..,\infty \tag{2.35}$$

Where I_{Ln} is the rms value of the n-th harmonic of the current passing through the inductor L_{dc}, V_{Rn} is the rms value of the n-th harmonic of the output voltage of the rectifier, and XL_{dc} is the value of the inductor reactance.

Assuming that the capacitor acts as an ideal short circuit for all harmonics, most of the current harmonics pass through it. The effect of this current harmonics in the voltage across the capacitor is given by,

$$V_{dc_n} = I_{C_n} * \frac{XC_{dc}}{n} = \frac{XC_{dc}}{XL_{dc}} * \frac{V_{R_n}}{n^2} \qquad n=2,..,\infty \tag{2.36}$$

Where I_{Cn} is the rms value of the n-th harmonic of the current passing through the capacitor C_{dc} (the sum of the inverter plus the rectifier currents), V_{Rn} is the rms value of the n-th harmonic of the output voltage of the rectifier, XC_{dc} and XL_{dc} are the values of the capacitor and the inductor reactances.

From this expression it is possible to obtain the rms value of the harmonics of the capacitor's voltage (dc bus voltage) as,

$$V_{dc_H} = XC_{dc} \cdot \sqrt{\sum_{n=2}^{\infty} \left(\frac{Io_n}{n} + \frac{V_{R_n}}{n^2 XL_{dc}} \right)^2} \tag{2.37}$$

$$XC_{dc} = \frac{K_v \cdot V_{do}}{\sqrt{\sum_{n=2}^{\infty} \left(\frac{Io_n}{n} + \frac{V_{R_n}}{n^2 XL_{dc}} \right)^2}} \qquad \text{pu} \qquad (2.38)$$

This expression is independent of the type of rectifier and modulation technique being used. The value of V_{dc} is given by the item 2.5.1.

In order to calculate both reactances, a second parameter is required. The most useful one in this case is the natural frequency of the filter, which is given by,

$$f_o = \sqrt{\frac{XC_{dc}}{XL_{dc}}} \qquad \text{pu} \qquad (2.39)$$

In order to exemplify the use of these equations, they are applied to a system with a single-phase full-wave diode rectifier and a single phase SPWM voltage source inverter, and the result is shown graphically in Fig. 2.15.

2.6. Design Example

In order to illustrate the use of these equations an example is presented with the following requirements: the maximum variation of the source voltage that the system is required to correct is $ME_{max} = 20\%$; the compensator is required to supply real power up to the full rated power ($Pc_{max} = Sc_{max}$); a sine PWM with switching frequency of 31 pu is used to control the single phase full bridge VSI ($G_i = 0.707$); the transformer has a turns ratio a = 1:4.25; the total harmonic distortion for both current and voltage should be $\leq 5\%$; the load power factor is equal to 0.75, lagging.

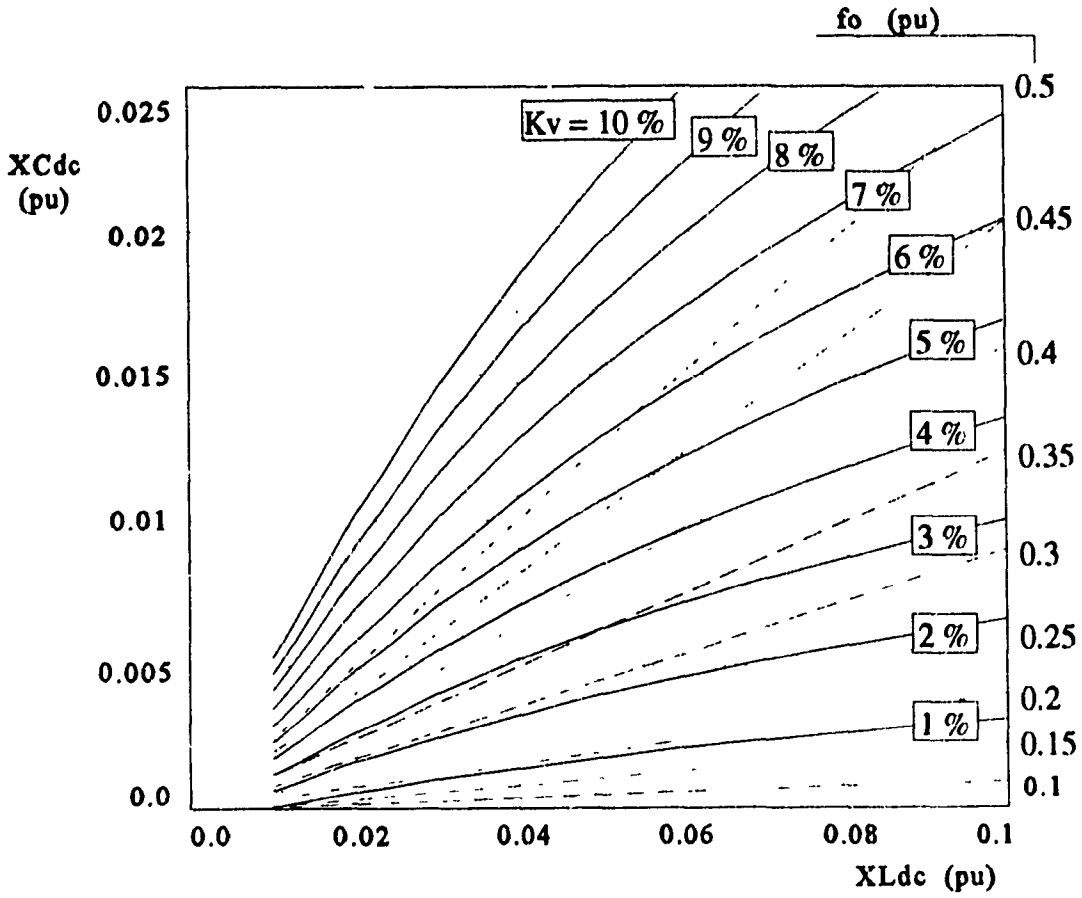

Fig. 2.15 - Dc bus filter design. Capacitor and inductor reactance as functions of the dc bus voltage ripple and the filter's break frequency.

The base values are S_{base} = 1.2 kVA, on the ac source side V_{base}= 110 V and on the inverter side V_{base}= 467.5 V.

The tables 2.1 to 2.6 summarize the results.

Table 2.1 - Transformer Ratings

Parameter	Equation	Value (pu)	Value (actual)
S_T	2.14	0.2	240 VA
V_{Tprim}	2.14	0.2	93.5 V
I_{Tprim}	2.14	1	2.57 A
V_{Tsec}	2.14	0.2	22 V
I_{Tsec}	2.14	1	10.9 A
N_2/N_1	2.15	1 : 4.25	

Table 2.2 - Filter Ratings

Parameter	Equation	Value (pu)	Value (actual)
S_{Lf}	2.29	0.096	115.2 VA
X_{Lf}	2.23	0.027	4.36 Ω
S_{Cf}	2.28	0.01	12 VA
X_{Cf}	2.27	8.95	1443.9 Ω

Table 2.3 - Inverter Ratings (Switches Ratings)

Parameter	Equation	Value (pu)	Value (actual)
S_I	2.18	0.2	240 VA
V_{dc}		0.283	132.23 V
f_{SW}		31	1.86 kHz
V_{SWpk}	2.17	0.283	132.23 V
V_{SWrms}	2.17	0.157	73.4 V
I_{SWpk}	2.16	1.41	3.64 A
I_{SWavg}	2.16	0.318	0.82 A
I_{SWrms}	2.16	0.707	1.82 A

Table 2.4 - Dc Source - Filter Ratings

Parameter	Equation	Value (pu)	Value (actual)
X_{Ldc}	2.37	0.02	3.65 Ω
X_{Cdc}	2.41	0.002	0.91 Ω

Table 2.5 - DC Source - Rectifier Ratings

Parameter	Equation	Value (pu)	Value (actual)
S_{dc}	2.32	0.223	267.24 VA
V_{SWpk}	2.3	0.445	207.82 V
V_{SWrms}	2.3	0.222	103.91 V
V_{SWavg}	2.3	0.142	66.15 V
I_{SWpk}	2.31	1	2.57 A
I_{SWrms}	2.31	0.5	1.285 A
I_{SWavg}	2.31	0.353	0.908 A

Table 2.6 - Dc Source - Transformer Ratings

Parameter	Equation	Value (pu)	Value (actual)
S_T	2.33	0.223	267.24 VA
V_{TA}	2.33	1	110 V
V_{TB}	2.33	0.314	146.95 V
N_A/N_B	2.33		1:1.336

2.7. Simulated and Experimental Results

To confirm feasibility, this method was applied to the system shown in Fig. 2.9 with parameters described in the tables I to VI. Simulation of the complete system has been performed to verify and confirm the operating principles and characteristics. An 1.2 kVA experimental unit has than been built. The results of both simulation and experimentation indicate that the proposed method performs as expected. In particular:

- Figs. 2.16, 2.18 and 2.20 show the source voltage, the load voltage and the load current from both simulation and experimental results, respectively. The comparison between the simulated and the experimental results confirms that the power factor is improved: the

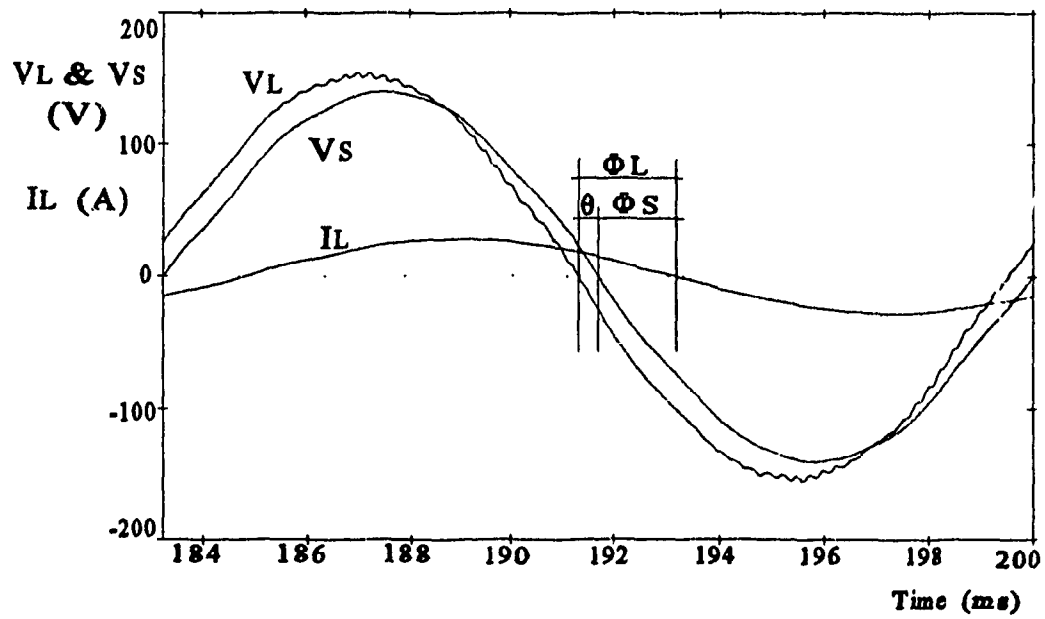

Fig. 2.16 - Simulation results. Voltage regulation with power factor improvement.

angle between the source voltage and the current is reduced.

- Figs. 2.17, 2.19, 2.21 and 2.22 present the simulated and the experimental spectra, respectively, of the source and the load voltages. These figures indicate that the harmonic content is very low, and that the load voltage has been increased to the required value (110 V).

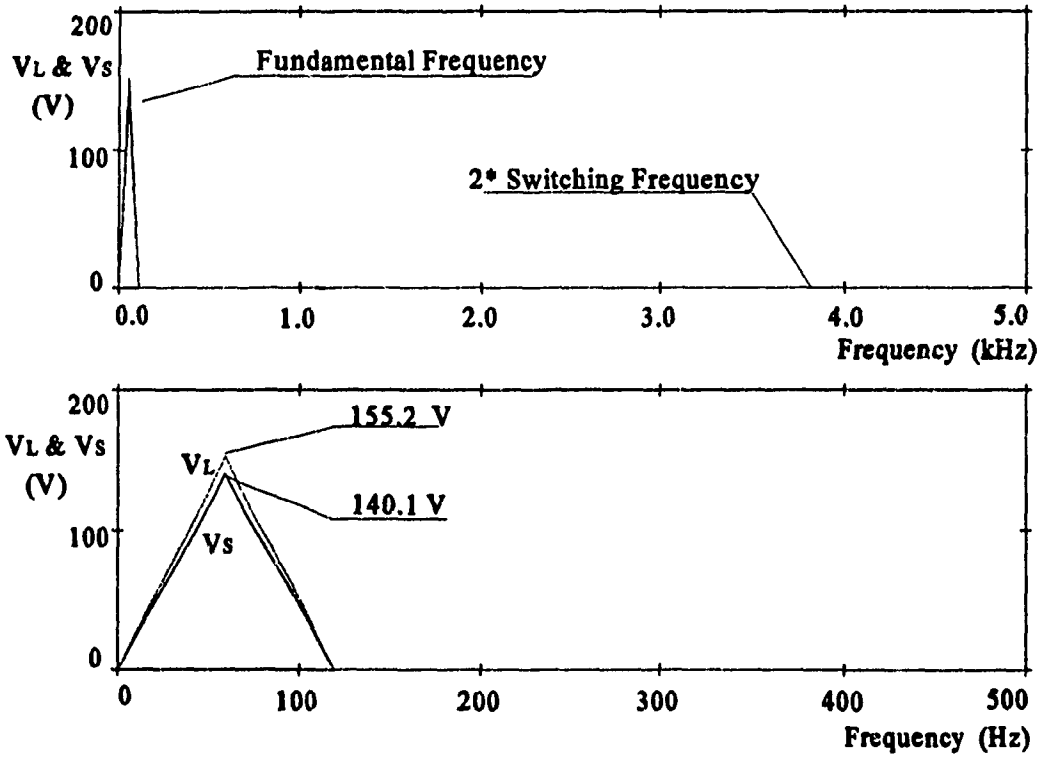

Fig. 2.17 - Simulation results - Spectra of the source and load voltages.

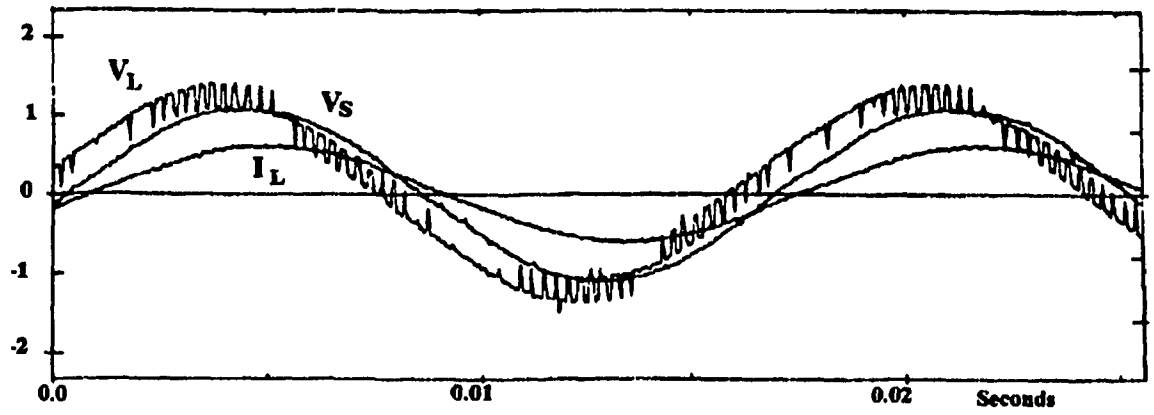

Fig. 2.18- Experimental results
Source voltage, load voltage (100 V/div) and load current (20 A/div)

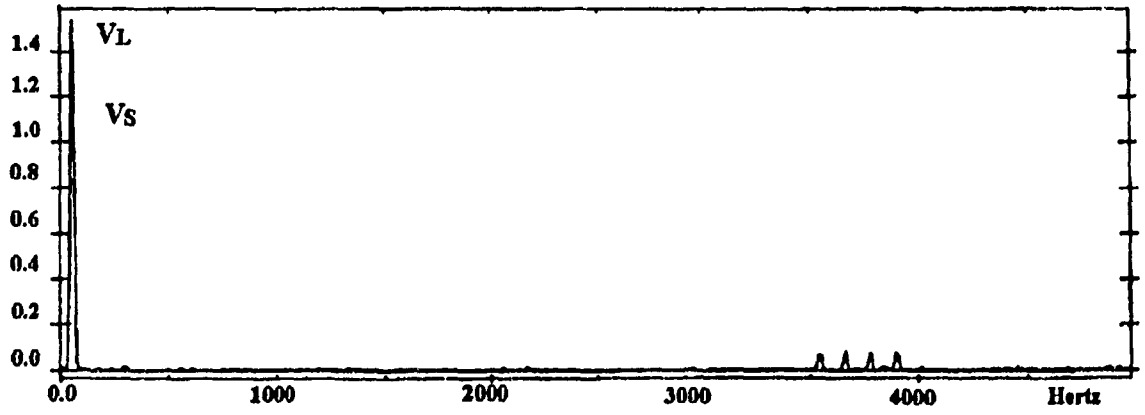

Fig. 2.19 - Experimental results. Source and load voltage spectra (100 V/div).

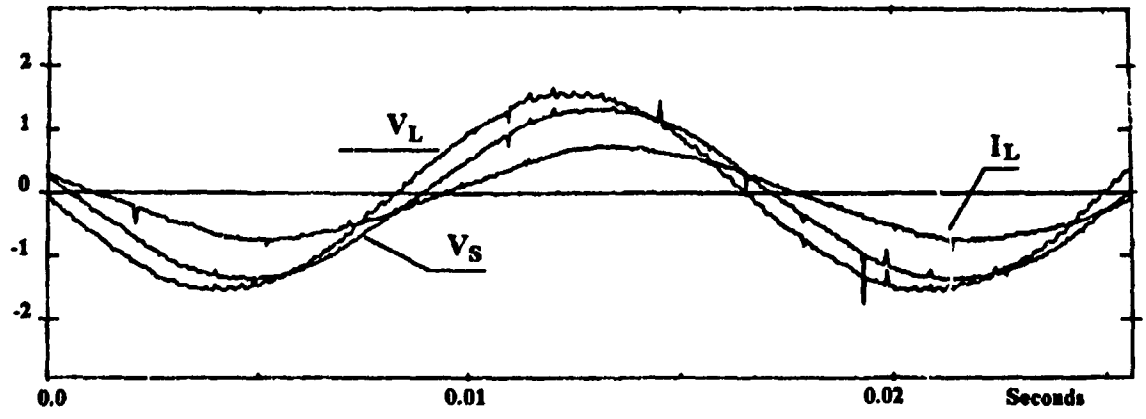

Fig. 2.20 - Experimental results with filter
Source voltage, load voltage (100 V/div) and load current (20 A/div).

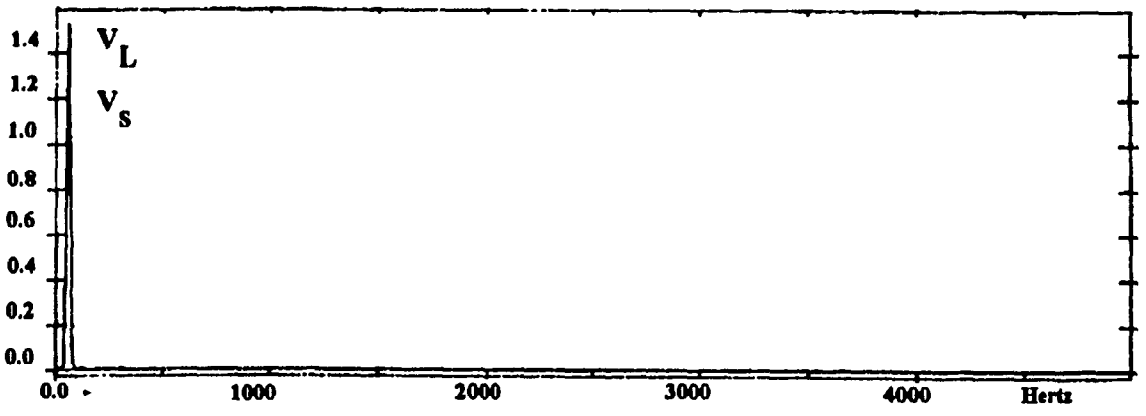

Fig. 2.21- Experimental results with filter. Source voltage and load voltage spectra (100 V/div)

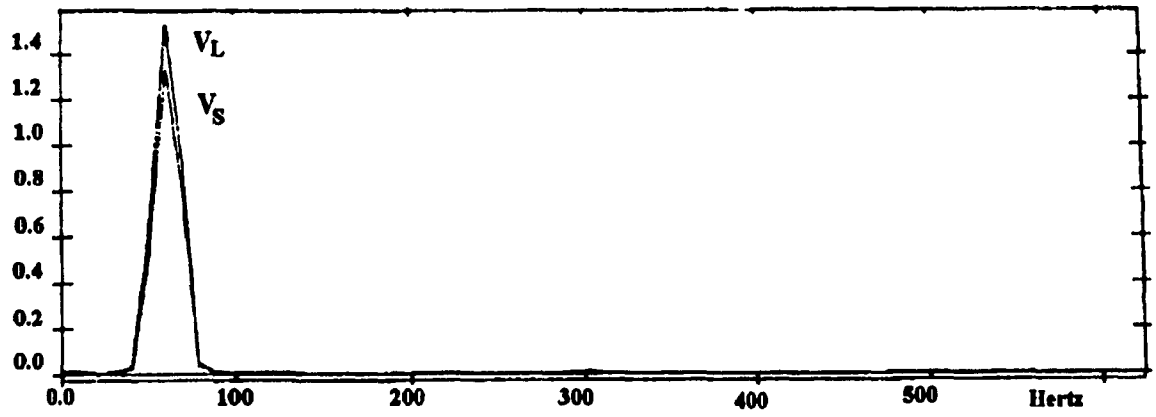

Fig. 2.22- Experimental results with filter. Source voltage and load voltage spectra (100 V/div)

2.8. Conclusions

The feasibility of a series voltage regulator for single phase ac voltage sources was demonstrated in this chapter. The use of a series transformed coupled voltage source inverter is shown to perform load voltage regulation and input power factor correction in single phase ac system. The use of a PWM voltage source inverter results in only very low harmonic injection in the ac system. Furthermore only a low kVA rating is required, that can however be either real or reactive, or both, depending upon the load power factor and ac line voltage level. Typically, a low kVA (0.2 pu) was required to perform voltage regulation in an ac source with a maximum of 10% of undervoltage. The power factor for the ac source was improved ($\cos(\Phi_L) = 0.75$ and $\cos(\Phi_S)=0.84$) by phase-shifting the regulator voltage.

CHAPTER 3

A SERIES VOLTAGE COMPENSATOR FOR THREE-PHASE UNBALANCED SOURCES

3.1. Introduction

This chapter proposes a method to eliminate the voltage unbalance present in three phase ac supplies using a series connected compensator with a low kVA rating. The compensator consists of three single phase voltage source inverters connected to the power system through a transformer. The negative sequence component of the line-to-line supply voltage is extracted and eliminated from the source, thus reducing the voltages to a balanced system with an amplitude dictated by the positive sequence. This component can then be adjusted in order to obtain a regulated load voltage. The use of pulse-width modulation (PWM) results in a system with fast dynamic response, and the possibility of using a high switching frequency allows a considerable reduction in the power rating of the required filter.

3.2. Principle of Unbalance Compensation

A three phase unbalanced delta connected voltage source shown in Fig. 3.1, with line voltages given by (3.1), can be decomposed into two balanced three phase systems using the symmetrical components transformation shown in (3.2).

$$Vs_{abc} = \begin{bmatrix} \hat{V}s_{ab} \\ \hat{V}s_{bc} \\ \hat{V}s_{ca} \end{bmatrix} \tag{3.1}$$

$$Vs_{012} = \begin{bmatrix} \hat{V}s_0 \\ \hat{V}s_1 \\ \hat{V}s_2 \end{bmatrix} = A^{-1} * Vs_{abc} \tag{3.2}$$

Where A is the transformation matrix, given by:

$$A^{-1} = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix}$$

$$A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \tag{3.3}$$

and $\alpha = e^{j120}$.

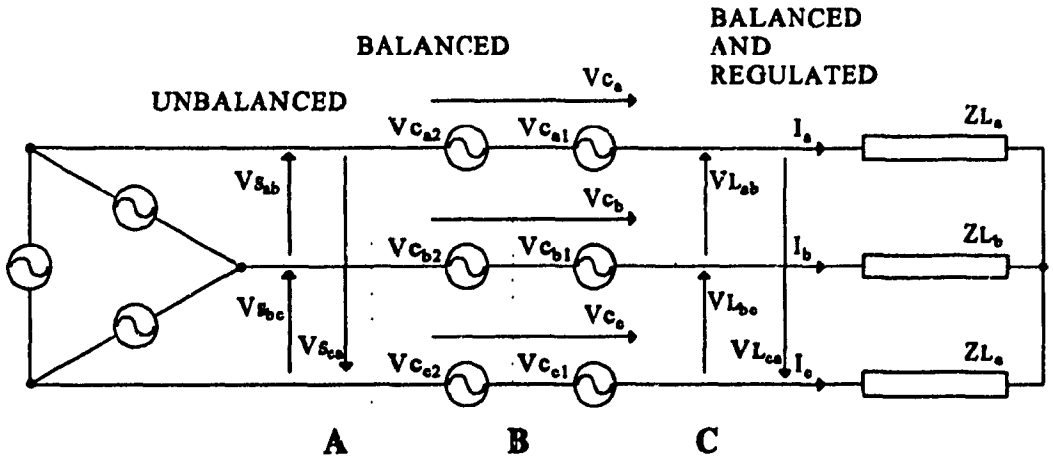

Fig. 3.1 - Simplified representation for an unbalance compensator.

If line-to-line voltages are used as in (3.1) or assuming there is no neutral path in the system, the zero sequence component $\hat{V}s_0$ is zero. The positive and the negative sequence components ($\hat{V}s_1$ and $\hat{V}s_2$) define two sets of balanced line-to-line voltages. Only the positive sequence component is desired while the presence of the negative sequence component is due to the unbalanced source. Therefore with the elimination of the negative sequence component a balanced three phase source is obtained.

In order to quantify the unbalance in the system a parameter must be defined. Among the several parameters that have been proposed to this date, the most common is the NEMA unbalance factor, defined in the MG1-14.34 standard (1980) as: the maximum deviation of the line voltages from their average divided by this average, as show in (3.4).

$$\text{NEMA UF} = \frac{\max(Vs_{abc}) - \text{avg}(Vs_{abc})}{\text{avg}(Vs_{abc})} * 100\% \qquad (3.4)$$

Despite the fact that this is the preferred practical parameter, its usefulness is limited due to its nonlinearity. The International Electrotechnical Commission defines another and more usable unbalance factor, as the ratio between the negative and the positive sequence components [33]:

$$\hat{UF} = \frac{\hat{V}s_2}{\hat{V}s_1} = |\hat{UF}|\angle\phi_{UF} \qquad (3.5)$$

The relation between this and the NEMA factor is given by the following equation:

$$\text{NEMA UF} = \left(\frac{3}{1 + \frac{|\alpha + \vec{UF}| + |1 + \alpha * \vec{UF}|}{|1 + \vec{UF}|}} - 1 \right) \tag{3.6}$$

When voltage control is required, it becomes necessary to define a second parameter to quantify the error between the load voltage and the required reference. This is defined as the magnitude factor MF, and is the ratio between the positive sequence of the line-to-line voltage and the required load line-to-line voltage ($\hat{V}_{REF}$):

$$\vec{MF} = \frac{\hat{V}s_1}{\hat{V}_{REF}} = |\vec{MF}| \angle \phi_{MF} = (1 - ME) \angle \phi_{MF} \qquad \text{pu} \tag{3.7}$$

Once these two parameters are defined, the required set of line-to-line voltages necessary to perform the unbalance compensation can be obtained by:

$$\mathbf{Vc}_{abc2} = \begin{bmatrix} \hat{V}c_{ab2} \\ \hat{V}c_{bc2} \\ \hat{V}c_{ca2} \end{bmatrix} = - \hat{V}s_2 * \mathbf{T}_2 \qquad \text{pu} \tag{3.8}$$

where

$$\mathbf{T}_2 = \begin{bmatrix} 1 \\ \alpha \\ \alpha^2 \end{bmatrix} \tag{3.9}$$

Substituting $\hat{V}s_2$ from (3.5) and (3.7) into (3.8), we have:

$$\mathbf{Vc}_{abc2} = - \hat{UF} * \hat{MF} * \mathbf{T}_2 \qquad \text{pu} \qquad (3.10)$$

The direct subtraction of the negative sequence from the source line voltages is performed by the first set of series voltage sources shown in Fig. 3.1 by the line-to-neutral voltages $\hat{V}c_{a2}$, $\hat{V}c_{b2}$ and $\hat{V}c_{c2}$, leaving a balanced system of line-to-line voltages at the coupling point B. The value of the line-to-neutral voltages are given by the following equation.

$$\begin{bmatrix} \hat{V}c_{a2} \\ \hat{V}c_{b2} \\ \hat{V}c_{c2} \end{bmatrix} = \frac{\mathbf{Vc}_{abc2}}{1 - \alpha} = - \hat{UF} \cdot \hat{MF} \cdot \frac{\mathbf{T}_2}{1 - \alpha} \qquad \text{pu} \qquad (3.11)$$

The second set of voltage sources in Fig. 3.1, $\hat{V}c_{a1}$, $\hat{V}c_{b1}$ and $\hat{V}c_{c1}$, is used to perform the load voltage control. The required line-to-line voltage to be added to $\mathbf{Vs}_{abc}$ to obtain $\hat{V}_{REF}$ is given by:

$$\mathbf{Vc}_{abc1} = (1 - \hat{V}s_1) \cdot \mathbf{T}_1 \qquad \text{pu} \qquad (3.12)$$

where

$$\mathbf{T}_1 = \begin{bmatrix} 1 \\ \alpha^2 \\ \alpha \end{bmatrix} \qquad (3.13)$$

Substituting (3.7) in (3.12),

$$\mathbf{Vc}_{abc1} = (1 - \hat{M}F) * \mathbf{T}_1 \qquad \text{pu} \qquad \textbf{(3.14)}$$

The necessary line-to-neutral voltages to perform the voltage control are given by:

$$\begin{bmatrix} \hat{V}c_{a1} \\ \hat{V}c_{b1} \\ \hat{V}c_{c1} \end{bmatrix} = \frac{\mathbf{Vc}_{abc1}}{1 - \alpha^2} = (1 - \hat{M}F) \cdot \frac{\mathbf{T}_1}{1 - \alpha^2} \qquad \text{pu} \qquad \textbf{(3.15)}$$

From (3.11) and (3.15) it is possible to calculate the total required set of phase voltages to perform the unbalance compensation and voltage control, as follows:

$$\begin{bmatrix} \hat{V}c_a \\ \hat{V}c_b \\ \hat{V}c_c \end{bmatrix} = \begin{bmatrix} \hat{V}c_{a1} \\ \hat{V}c_{b1} \\ \hat{V}c_{c1} \end{bmatrix} + \begin{bmatrix} \hat{V}c_{a2} \\ \hat{V}c_{b2} \\ \hat{V}c_{c2} \end{bmatrix} \qquad \textbf{(3.16)}$$

$$\begin{bmatrix} \hat{V}c_a \\ \hat{V}c_b \\ \hat{V}c_c \end{bmatrix} = \frac{\mathbf{T}_1}{1 - \alpha^2} - \hat{M}F \cdot \left(\frac{\mathbf{T}_1}{1 - \alpha^2} + \hat{U}F \cdot \frac{\mathbf{T}_2}{1 - \alpha} \right) \text{pu} \qquad \textbf{(3.17)}$$

3.3. System Description

Fig. 3.2 shows the circuit used to implement the proposed method. It consists of three single phase PWM voltage source inverters connected in series with the line through three single phase transformers. Second order filters are connected between the inverters and the transformers to reduce the harmonic content of the injected voltage.

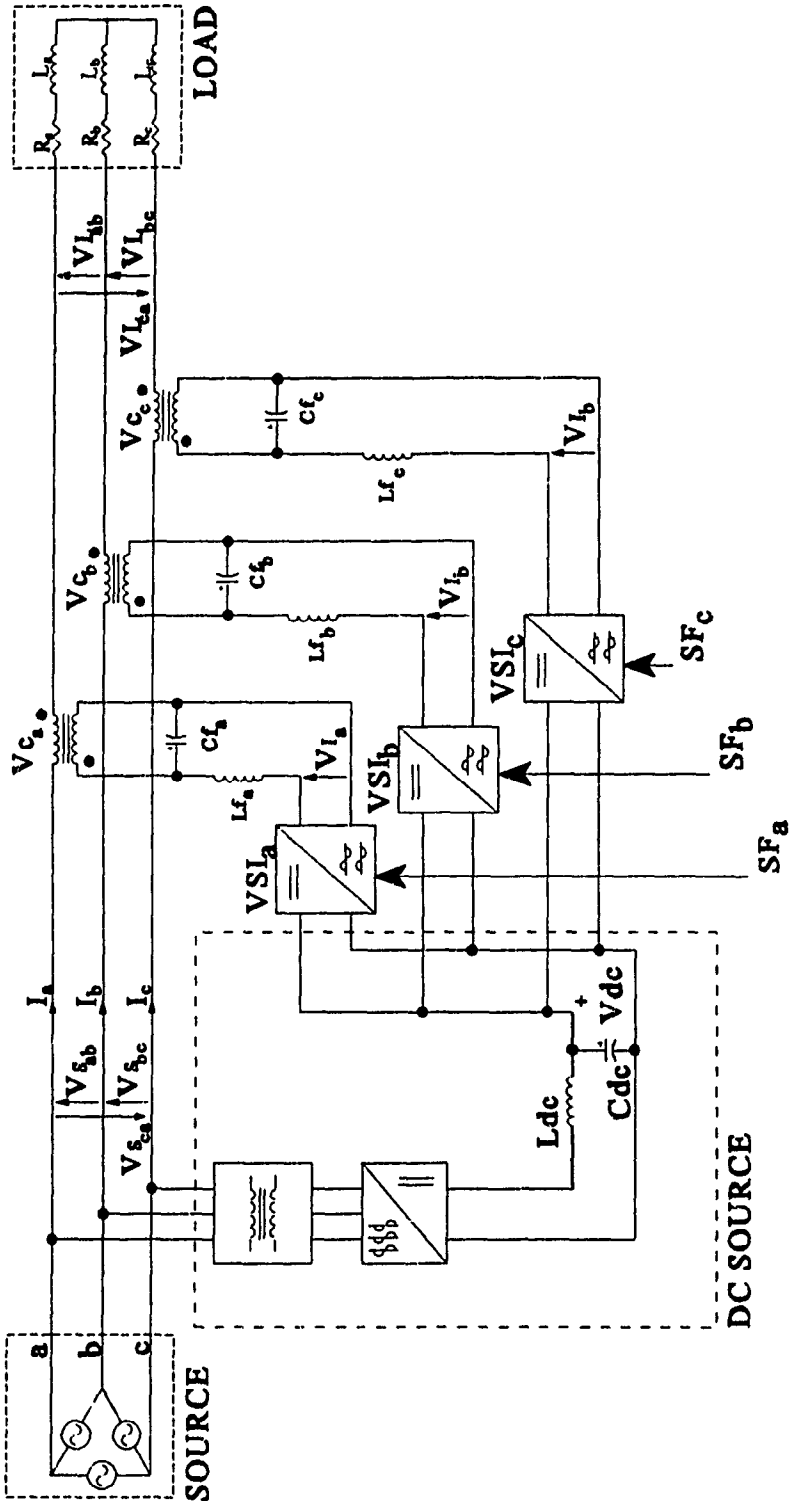

Fig. 3.2 - Block diagram of the proposed unbalance compensator.

The line-to-line load voltages are decomposed into their symmetrical components by a filtering stage. These values are used by the controller to generate the appropriate gating signals for the inverters in order to achieve the set of voltages given by (3.17).

3.4. System Design

The main parameters for designing the proposed compensator are the maximum unbalance factor $|\hat{UF}|_{max}$, and the minimum magnitude factor $|\hat{MF}|_{min}$ of the source. They are both defined by the utility standards and by application requirements. A common minimum value for the magnitude factor is 80%, which means the compensator is capable of adjusting voltage errors from undervoltages of 80% to overvoltages up to 120%. The maximum unbalance allowed in the utility line has not been standardized. The only reference in the literature to unbalance constraints is the one from NEMA, where a maximum of 5% of unbalance (NEMA UF) is recommended when supplying induction motors. Whe designing AC systems, a maximum of 20% unbalance in the supply voltages is generally assumed.

The magnitude of the maximum allowed unbalance factor ($|\hat{UF}|_{max}$) can be chosen based on the NEMA factor (more commonly used and known) as a starting point and then determining $\hat{UF}$ from (3.6) or Fig. 3.3. The phase of $\hat{UF}$ should be assumed 60 degrees (worst case - gives the largest $|\hat{UF}|$).

The use of transformers in both sides of the compensator gives complete freedom to choosing the value of the dc bus voltage V_{dc}, which can be specified by a cost evaluation of the switches and filter capacitors.

The following assumptions are used in this design.

i) The switches are ideal.

ii) The filter components are ideal.

iii) The base value for the power (S_{BASE}) is the rated load power.

iv) The base value for the voltage (V_{BASE}) is the infinite bus line-to-line voltage.

v) The base voltage in the inverter side ($V_{I_{BASE}}$) is calculated using the series transformer turns ratio.

3.4.1. Power Requirements

The power required to perform the compensation is defined in pu by the maximum compensation voltage Vc_{max} , which occurs when the negative sequence component to be eliminated is in phase with the positive sequence to be corrected. The magnitude of this apparent power is calculated by (3.18). Fig. 3.3 shows the relationship between these parameters ($|\vec{UF}|_{max}$, $|\vec{MF}|_{min}$) and the NEMA unbalance factor in the calculation of the compensator rated power (in pu), which is expressed by:

$$S_C = \sqrt{3} \cdot Vc_{max} = \sqrt{3} \cdot (1 - |\vec{MF}|_{min} * (1 - |\vec{UF}|_{max})) \text{ pu} \qquad \textbf{(3.18)}$$

The real power supplied or absorbed at any moment by the compensator is determined by the load power factor and by the value of the positive sequence component of the compensation voltage (Vc_{abc1}). If voltage regulation is not needed for a particular application (i.e. if only unbalance compensation is desired), then no real power is required and the dc source can be eliminated. In this case the dc bus can be supported by the inverter using slight phase-shifts of the voltage with respect to the load current. The real power necessary to maintain the dc bus is absorbed from the ac mains. Under the worst case, for unity load power factor and maximum positive sequence component (full voltage regulation), the compensator's real power is given by,

$$P_C = S_C = \sqrt{3} \cdot Vc_{max} \qquad \text{pu} \qquad (3.19)$$

This expression establishes the extreme situation where it is assumed that the voltage error is solely due to drops on resistive elements. This case almost never occurs because most of the voltage drops, as shown in Chapter 2, are due to reactive elements such as transformer leakage reactances, inductances of filters, etc. In applications where a limit for the voltage drop on resistive elements can be specified, the rated real power can be reduced to a minimum value, which minimizes the size and cost of the dc source.

3.4.2. Series Transformer Design

With the maximum unbalance factor and the minimum magnitude factor defined, the maximum secondary voltage of the transformer is given, by the following equation.

$$Vc_{max} = \frac{1 - |\vec{MF}|_{min} * (1 - |\vec{UF}|_{max})}{\sqrt{3}} \quad pu \quad (3.20)$$

The transformer turns ratio and primary voltage depend on the maximum output voltage of the inverter, which is defined by the dc bus voltage and the modulation technique used to control the inverter. Assuming that the inverter gain for the fundamental component of the line-to-line voltage is G_i and the dc bus voltage is V_{dc}, the transformer turns ratio is:

$$N_T = \frac{Vc_{max}}{Gi \cdot V_{dc}} \quad pu \quad (3.21)$$

Because of the series connection, the rated current in the transformer is one pu, and the total apparent power is given in pu by the maximum secondary voltage, as follows.

$$S_{T_{max}} = \frac{1}{3} Sc_{max} = \frac{Vc_{max}}{\sqrt{3}} \quad pu \quad (3.22)$$

3.4.3. Design of the Voltage Source Inverters.

The use of three independent single-phase voltage source inverters allows a complete freedom in the choice of configuration and modulation technique. A high performance compensation system can therefore be easily achieved. Designing the inverters involves the specification of the topology to be used, the modulation technique, and the switches to be used and their ratings.

Single-phase half-bridge voltage source inverters, with bipolar transistors as switches are used. The inverters are controlled using a carrier-based sine pulse-width modulation technique (SPWM), which is an arbitrary choice since any modulation technique could be applied to this compensator.

$$\left\{ \begin{array}{l} I_{SW_{rms}} = \dfrac{1}{\sqrt{2}} \\ I_{SW_{pk}} = \sqrt{2} \\ I_{SW_{avg}} = \dfrac{1}{\pi} \end{array} \right\} \qquad \text{pu} \qquad (3.23)$$

Assuming the filter is properly designed, no current harmonics will pass through the inverter, thus the current in any switch will be very close to sinusoidal. The current ratings for the switches are then given by: The voltage rating is given by the following equations.

$$\left\{ \begin{array}{l} V_{SW_{rms}} = \dfrac{1}{\sqrt{2}} \cdot \sqrt{\sum_{n=1}^{\infty} (V_{I_n})^2} \\ V_{SW_{pk}} = V_{dc} \end{array} \right\} \qquad \text{pu} \qquad (3.24)$$

The apparent power required from the inverter is higher then that of in the transformer due to the presence of harmonics in the output voltage, and it is given by:

$$S_I = \frac{1}{3} \cdot \sqrt{\sum_{n=1}^{\infty} (V_{I_n})^2} \qquad \text{pu} \qquad (3.25)$$

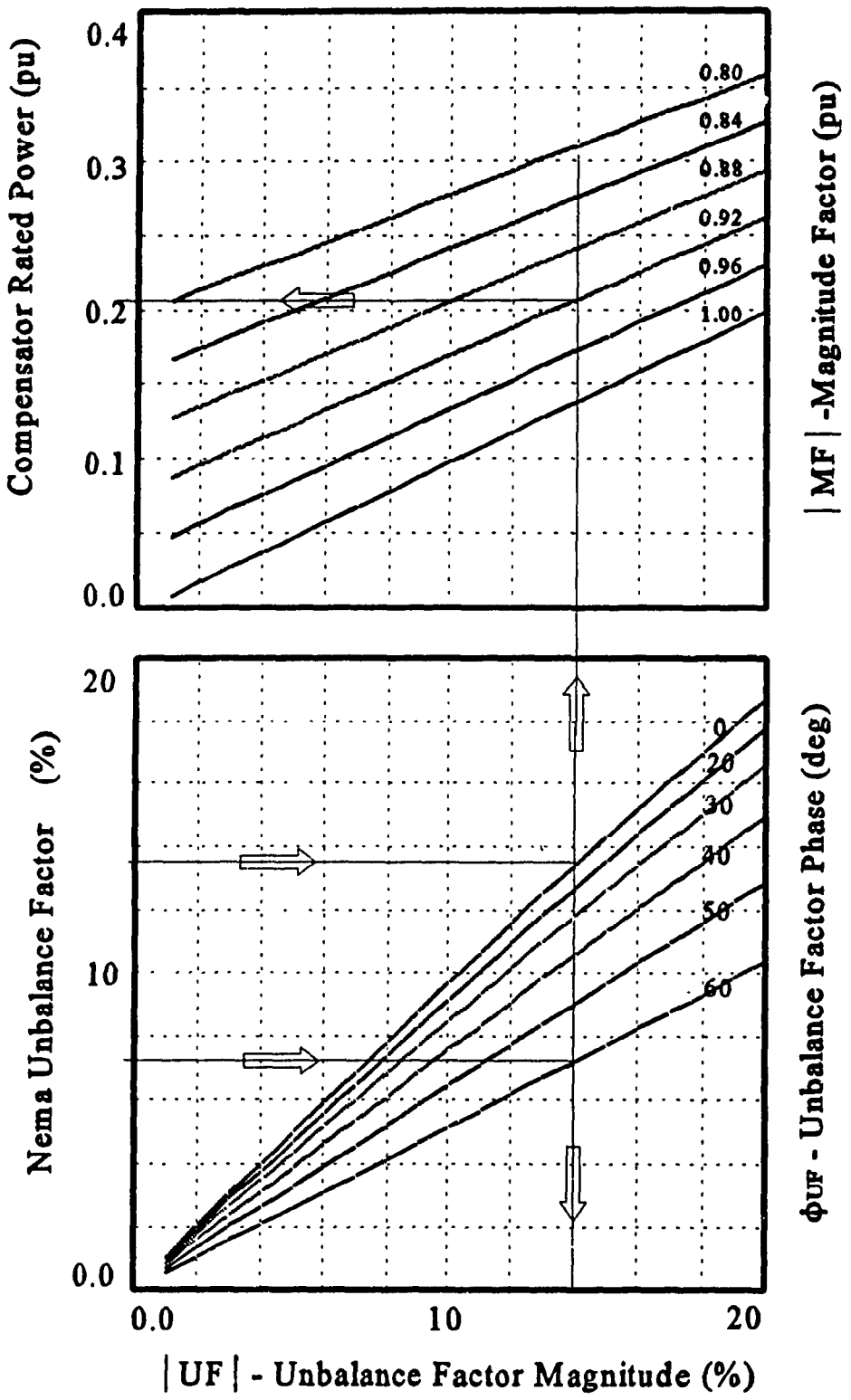

Fig. 3.3 - Unbalance factors and compensator power rating.

3.4.4. Design of the Inverter Output Filter.

The method used to design the filters for the output of each inverter is approximately the same as the one already presented in Chapter 2, except for the fact that the voltage harmonics injected by the inverters in the present case are higher than the previous. Analysis of such a system can be done on a per phase basis due to the use of independent inverters. The equivalent circuit is shown in Fig. 3.4, where the inverter output voltage and the load current are modelled by their harmonic component, specified by the index *n*.

Using the method described in the previous chapter, the value of the inductor reactance is calculated as follows.

$$XL_f = \frac{K_i}{THD_i} \quad \text{pu} \qquad (3.26)$$

where

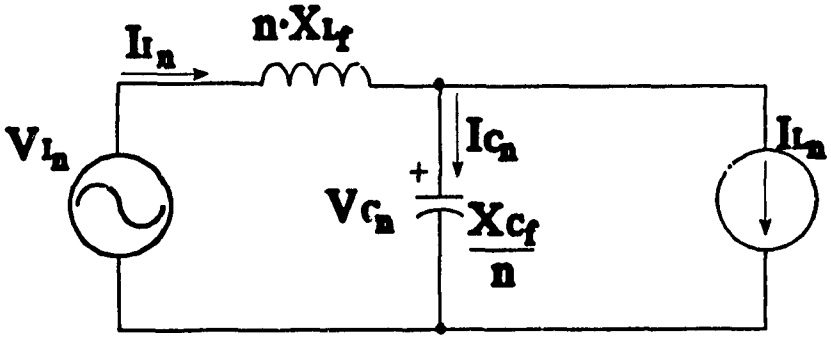

Fig. 3.4 - Equivalent circuit used for designing the inverter output filter.

$$K_1 = \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n}\right)^2} \quad \text{pu} \qquad (3.27)$$

The rms value of the voltage across the capacitor due to the harmonics is:

$$Vc_H = \frac{XC_f}{XL_f} \cdot \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n^2}\right)^2} \quad \text{pu} \qquad (3.28)$$

Thus, the capacitor reactance is calculated by taking into account that the relationship between the total harmonic distortion of the load voltage and the capacitor voltage is given by:

$$THD_{Vc} = \frac{V_{C_H}}{V_{C_1}} = \frac{V_{C_H}}{Vc_{max}} = \frac{THD_{VL}}{2\ Vc_{max}} \qquad (3.29)$$

Substituting (3.28) in this last equation, XC_f can be obtained, as shown in the following equation.

$$XC_f = \frac{XL_f \cdot THD_{VL}}{2 \cdot K_2} \quad \text{pu} \qquad (3.30)$$

where

$$K_2 = \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n^2}\right)^2} \quad \text{pu} \qquad (3.31)$$

Figs. 3.5 and 3.6 present the relationship between XC_f and XL_f ((3.30 and (3.26)) obtained for a SPWM half bridge voltage source inverter at unity modulation index with $|\hat{U}F|_{max} = 20\%$, $|\hat{M}F|_{min} = 80\%$.

The kVA ratings for C_f and L_f are calculated from (3.32) and (3.33), respectively.

$$SC_f = \frac{Vc_{max}}{XL_f} \cdot \frac{K_1}{\sqrt{3}} \cdot \sqrt{(1 + THD_{Vc}^2)} \approx \frac{Vc_{max} \cdot THD_i}{\sqrt{3}} \quad pu \qquad (3.32)$$

$$SL_f = \frac{K_0}{\sqrt{3}} \cdot \sqrt{(1 + THD_i^2)} \approx \frac{K_0}{\sqrt{3}} \quad pu \qquad (3.33)$$

where K_0 is defined as,

$$K_0 = \sqrt{\sum_{n=2}^{\infty} (V_{I_n})^2} \quad pu \qquad (3.34)$$

For the case of a sine PWM half bridge voltage source inverter, the value of K_1 is 0.009. Also, for low values of THD_i and THD_{VL} the approximations shown in (3.32) and (3.33) are valid, which makes the kVA ratings of the inductor equal to 0.207 pu.

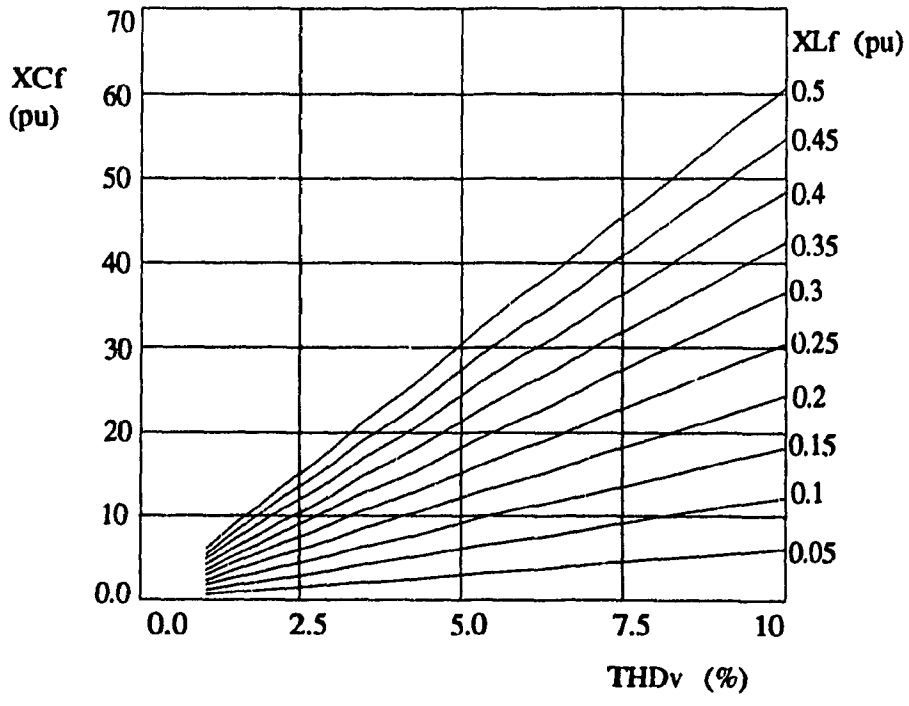

Fig. 3.5 - Inverter filter design - Capacitor reactance.

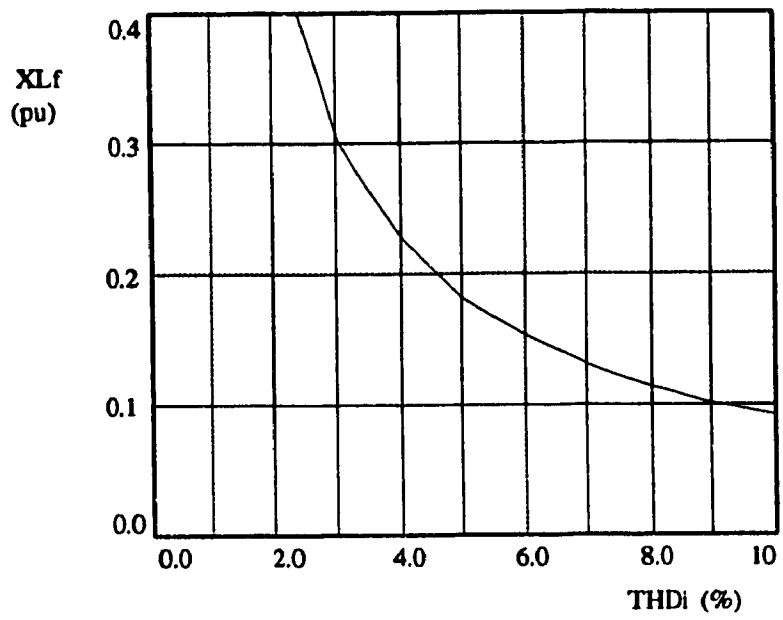

Fig. 3.6 - Inverter filter design - Inductor reactance.

3.4.5. Design of the dc Source.

The dc source consists of a transformer, a rectifier and a filter, connected as shown in Fig. 3.7.

The design of the dc source depends on the desired mode of operation of the compensator. For the general case, operating in four quadrants (supply or absorb real and

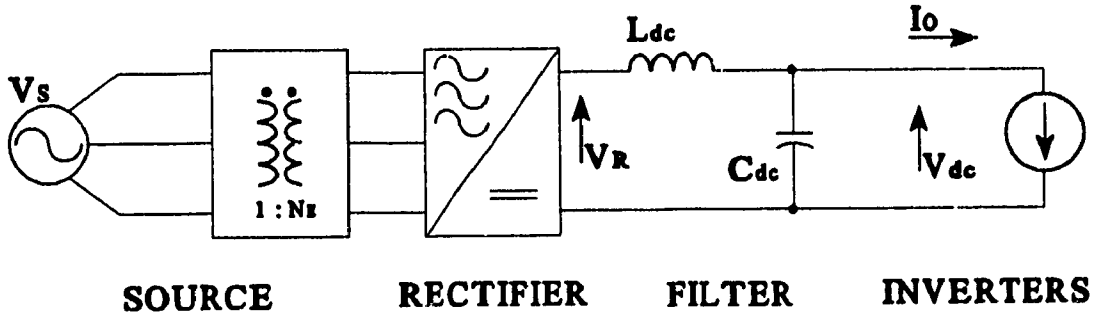

Fig. 3.7 - Equivalent circuit used for designing the dc source.

reactive power), the compensator requires a dc source capable of operate in two quadrants.

The starting point for the design of such a circuit is the definition of the amount of real power that the compensator is allowed to provide to the system (Pc_{max}). As already mentioned in the section 3.4.1, if the real power is made zero, the compensator becomes a series var compensator, and the dc source is not necessary.

When real power is required to perform the compensation, the dc source becomes necessary, and its power ratings are defined by the value and the phase of the compensator voltage ($\mathbf{Vc}_{abc}$) with respect to the line current. Also, if the compensator is required only to **supply** real power, as in the proposed example, the dc source does not need to regenerate current, thus a diode rectifier can be used to implement it. In this case the ratings for the rectifier are,

$$\left\{ \begin{array}{l} V_{SW\,rms} = \dfrac{V_{dc}}{\sqrt{3}} \cdot \sqrt{\dfrac{\pi^2}{9} + \dfrac{\pi}{2\sqrt{3}}} \\ V_{SW\,pk} = \dfrac{\pi}{3} V_{dc} \\ V_{SW\,avg} = \dfrac{2}{3} V_{dc} \end{array} \right\} \quad \text{pu} \qquad (3.35)$$

$$\left\{ \begin{array}{l} I_{SW\,rms} = \dfrac{1}{\sqrt{3}} \dfrac{P_{dc}}{V_{dc}} \\ I_{SW\,pk} = \dfrac{\pi}{3} \dfrac{P_{dc}}{V_{dc}} \\ I_{SW\,avg} = \dfrac{1}{3} \dfrac{P_{dc}}{V_{dc}} \end{array} \right\} \quad \text{pu} \qquad (3.36)$$

Where P_{dc} is the required real power (equal to Pc_{max}), $V_{.}$ the rated dc bus voltage, and Ki is the maximum current ripple in the inductor L_{dc}.

The apparent power required from the rectifier is,

$$S_R = 1.178 \cdot P_{dc} \qquad \text{pu} \qquad \textbf{(3.37)}$$

The transformer ratings are,

$$\left\{ \begin{array}{l} S_T = 1.178 \cdot P_{dc} \\ V_{T_B} = \dfrac{\pi}{3\sqrt{6}} \cdot V_{dc} \\ V_{T_A} = V_S \\ \dfrac{N_S}{N_P} = \dfrac{\pi}{3\sqrt{6}} \cdot \dfrac{V_{dc}}{V_S} \end{array} \right\} \qquad \text{pu} \qquad \textbf{(3.38)}$$

3.4.6. Design of the dc Bus Filter.

The design of the dc bus filter for the proposed compensator is similar to the one in Chapter 2. Some diffferences are of notice: (a) the dc source is now implemented by using a three-phase bridge rectifier; and (b) the harmonics injected by the inverters in the dc bus current are increased.

The expression obtained in Chapter 2 for the capacitor reactance is still valid for the present case. Only the harmonics of the rectifier output voltage and inverter input current have a different value. The capacitor reactance is then,

$$XC_{dc} = \frac{K_V \cdot V_{dc}}{\sqrt{\sum_{n=2}^{\infty}\left(\frac{Io_n}{n} + \frac{V_{R_n}}{n^2\, XL_{dc}}\right)^2}} \quad \text{pu} \qquad (3.39)$$

where K_V is the ripple of the dc bus voltage V_{dc}, Io_n is the n-th harmonic of the sum of the input currents of all three inverters, VRn is the n-th harmonic of the output voltage of therectifier, XL_{dc} and XC_{dc} are the inductor and the capacitor reactances (in pu).

In order to calculate both reactances a second parameter is required, and in this case the natural frequency of the filter, given by,

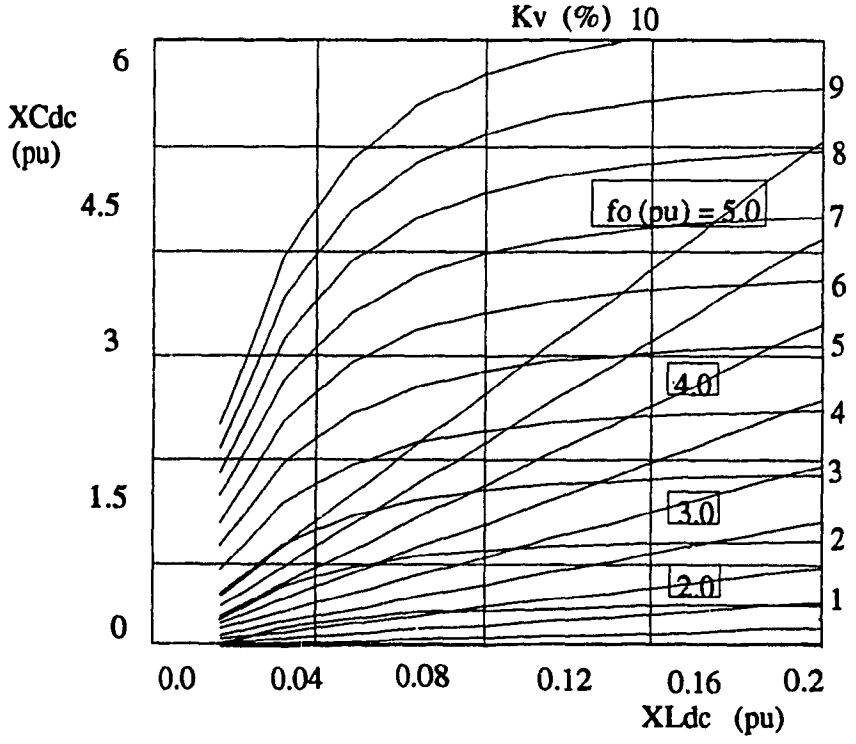

Fig. 3.8 - Dc bus filter capacitor and inductor reactances as functions of the dc bus voltage ripple and the filter break frequency.

$$f_o = \sqrt{\frac{XC_{dc}}{XL_{dc}}} \qquad \text{pu} \qquad (3.40)$$

is used. These equations are applied to a system with a a three-phase bridge diode rectifier and three single phase half bridge SPWM voltage source inverter, and the result is shown graphically in the Fig. 3.8.

3.5. Design Example

In order to illustrate the use of the design equations, the following example is presented. The requirements are: the rated power of the system is 2.2 kVA; the maximum unbalance factor is 20%; the maximum magnitude error is 20% (|MF| = 0.8) ; the line-to-line load voltage is $\sqrt{3}\cdot 110$ volts ; a half-bridge voltage source inverter is used ; the inverters are controlled with sine PWM modulation with switching frequency of 31 pu; the compensator is required only to supply real power up to the full rated power (Pdc = Sc); the transformer has a turns ratio of 1:4; the total harmonic distortion for both current and voltage should be $\leq$ 5%; the load power factor is equal to 0.75, lagging. The base values and the result of the design are presented in the following tables.

Table 3.1 - Base Values

Parameter	Value (actual)
S_{BASE}	2.2 kVA
V_{BASE}	190.53 V
Vi_{BASE}	440 V
I_{BASE}	6.67 A
Ii_{BASE}	1.67 A
Z_{BASE}	16.5 Ω
Zi_{BASE}	264 Ω
Gi	0.354

Table 3.2 - Transformer Ratings.

Parameter	Equation	Value (pu)	Value (actual)
Power	3.22	0.12	264 VA
Primary voltage	3.2	0.208	39.6 V
Secondary voltage	---	0.36	158.4 V
Primary current	---	1	1.67 A
Secondary current	---	1	6.67 A
Turns ratio	3.21	0.25	---

Table 3.3 - Inverter Ratings (Switches Ratings) - Each inverter

Parameter	Equation	Value (pu)	Value (actual)
S_I	3.25	0.17	373.2 VA
V_{dc}		1.017	448 V
f_{SW}		31	1.86 kHz
V_{SWpk}	3.24	1.017	448 V
V_{SWrms}	3.24	0.36	158.2 V
I_{SWpk}	3.23	1.41	2.36 A
I_{SWavg}	3.23	0.318	0.531 A
I_{SWrms}	3.23	0.707	1.18 A

Table 3.4 - Filter Ratings.

Parameter	Equation	Value (pu)	Value (actual)
S_{Lf}	3.33	0.207	456 VA
X_{Lf}	3.26	0.18	47.5 Ω
S_{Cf}	3.32	0.006	13.2 VA
X_{Cf}	3.30	10.9	2877 Ω

Table 3.5 - DC Source - Rectifier Ratings.

Parameter	Equation	Value (pu)	Value (actual)
S_R	3.37	0.424	932.97 VA
V_{SWpk}	3.35	1.047	460.8 V
V_{SWrms}	3.35	0.831	365.6 V
V_{SWavg}	3.35	0.678	298.3 V
I_{SWpk}	3.36	0.371	0.619 A
I_{SWrms}	3.36	0.204	0.341 A
I_{SWavg}	3.36	0.118	0.197 A

Table 3.6 - Dc Source - Filter Ratings.

Parameter	Equation	Value (pu)	Value (actual)
f_o	3.40	3.5	212 Hz
X_{Ldc}	3.39	0.02	5.28 Ω
X_{Cdc}	3.39	0.25	66 Ω

Table 3.7 - Dc Source - Transformer Ratings.

Parameter	Equation	Value (pu)	Value (actual)
S_T	3.38	0.424	932.97 VA
V_{TA}	3.38	1	110 V
V_{TB}	3.38	0.435	191.3 V
N_A/N_B	3.38		1:1.336

3.6. Experimental Results

In order to confirm the proposed voltage compensation method, it was applied to the following system:

Total apparent load power - 2.2 KVA Required line voltage -√3*110 Volts

Load impedance - 16.9 Ω Load power factor - 0.78

Unbalance factor - 13.8% Magnitude error - 7.7% (MF=0.923)

Tables 3.8 to 3.10 summarize the main results, and the principal steady-state waveforms are presented in the Figs. 3.4 to 3.11.

Figs. 3.9 and 3.10 show the supply line-to-line voltages with their respective spectrum. The voltage unbalance is quite clear in both figures.

Figs. 3.11 and 3.12 show the instantaneous load line-to-line voltages and their respective spectrum. The spectra demonstrate that the balancing of the fundamental component is achieved and the harmonics injected are reasonable low.

The same system was also tested with a filtering stage in order to reduce the THD of the load voltages. Figs. 3.13 and 3.14 present the results obtained. The line-to-line load voltages (Fig. 3.13) have a low THD, as can be seen in their spectra (Fig. 3.14).

Figs. 3.15 and 3.16 show the instantaneous load line current and its spectrum without and with filter. Due to the filtering effect of the load (Power Factor = 0.79) the harmonic content in the current is negligible, as shown by its spectrum.

Table 3.8 - Experimental results summary - source .

Vs_{ab}	165 V ∠0°	Vs_0	0 V ∠0°
Vs_{bc}	200 V ∠-127.3°	Vs_1	175.8 V ∠-7.3°
Vs_{ca}	165 V ∠105.4°	Vs_2	24.23 V ∠112.7°
UF	0.138 pu ∠120°	MF	0.923 pu ∠-7.3°

Table 3.9 - Experimental results summary - load - no filter .

Variable	Total	Fundamental	THD
VL_{ab}	195.31 V	190.71 V	0.221
VL_{bc}	195.83 V	190.23 V	0.244
VL_{ca}	194.39 V	190.71 V	0.1975
I_a	6.66 V	6.62 V	0.1197
SOURCE APPARENT POWER		2.05 kVA	
COMPENSATOR APPARENT POWER		0.317 kVA	
LOAD APPARENT POWER		2.25 kVA	

Table 3.10 - Experimental results summary - load - with filter.

Variable	Total	Fundamental	THD
VL_{ab}	191.92 V	190.73 V	0.112
VL_{bc}	192.07 V	190.49 V	0.129
VL_{ca}	191.49 V	190.59 V	0.097
I_a	6.63 V	6.62 V	0.055
SOURCE APPARENT POWER		2.04 kVA	
COMPENSATOR APPARENT POWER		0.316 kVA	
LOAD APPARENT POWER		2.20 kVA	

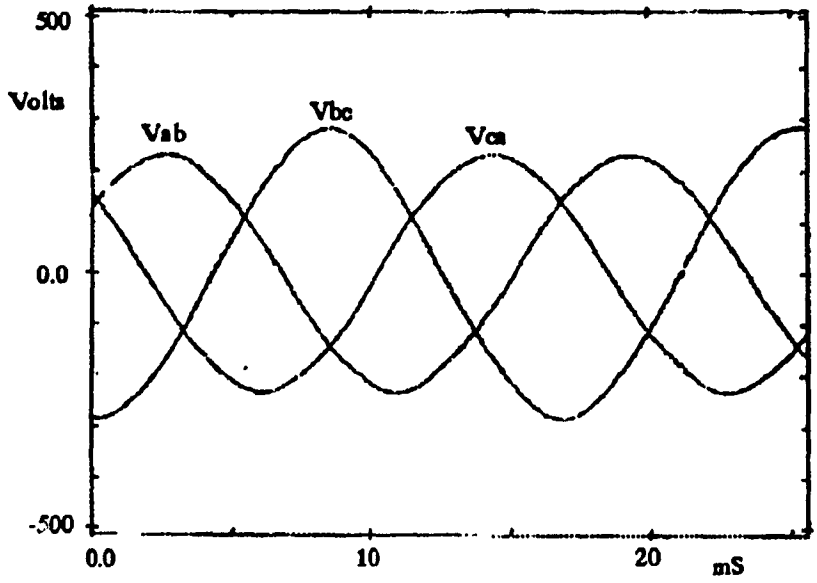

Fig. 3.9 - Experimental Results. Supply line-to-line voltages - VS_{ab}, VS_{bc} and VS_{ca}

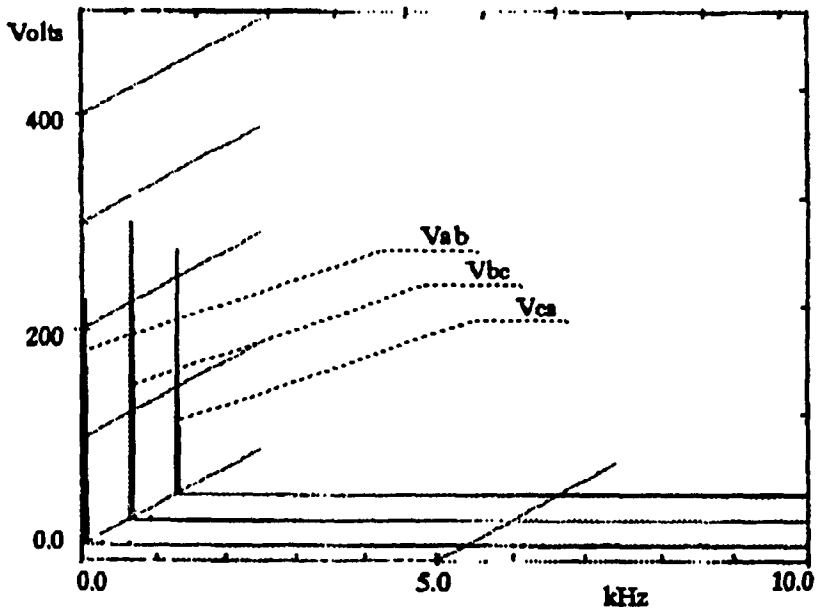

Fig. 3.10 - Experimental Results. Spectrum of the supply line-to-line voltages - VS_{ab}, VS_{bc} and VS_{ca}

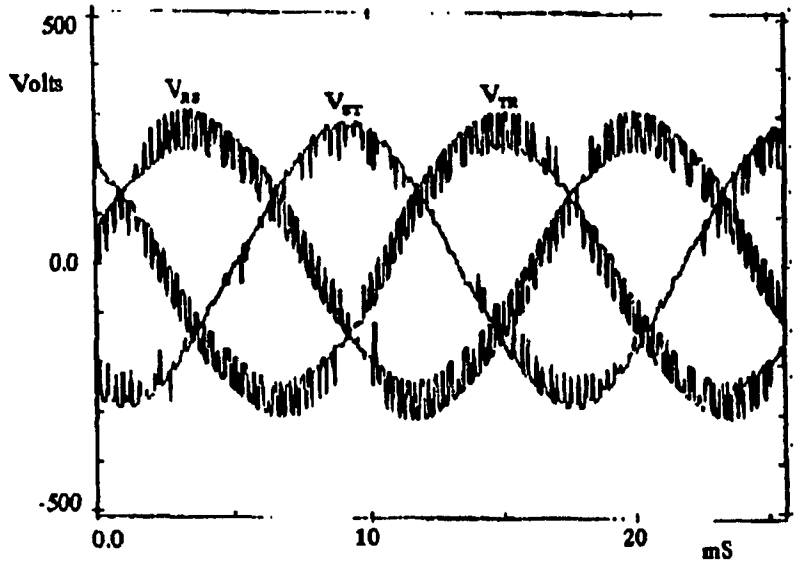

Fig. 3.11 - Experimental Results. Load line-to-line voltages without filter - VL_{ab}, VL_{bc} and VL_{ca}

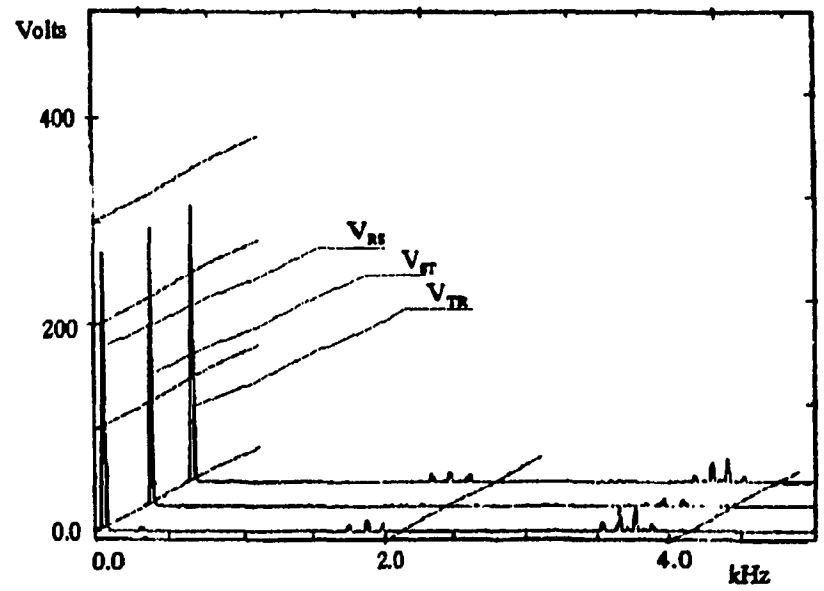

Fig. 3.12 - Experimental Results. Spectrum of the load line-to-line voltages without filter- VL_{ab}, VL_{bc} and VL_{ca}

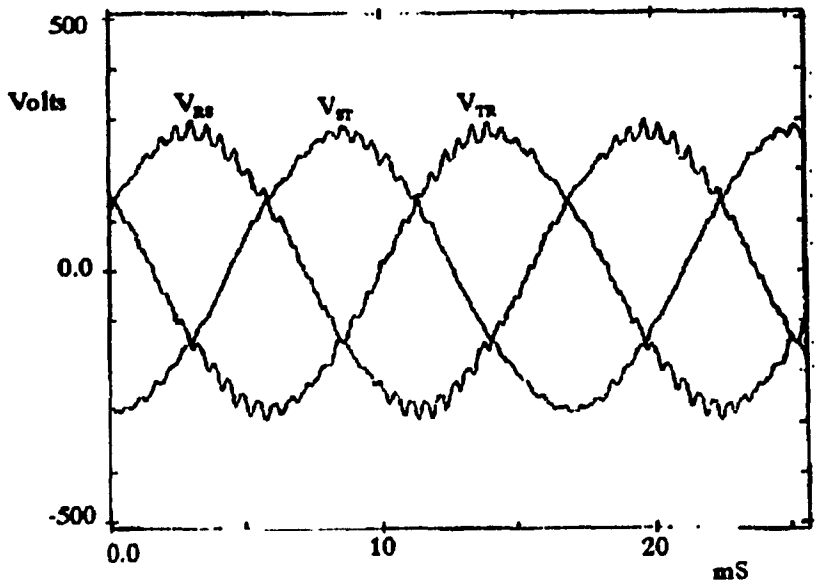

Fig. 3.13 - Experimental Results. Load line-to-line voltages with filter - VL_{ab}, VL_{bc} and VL_{ca}

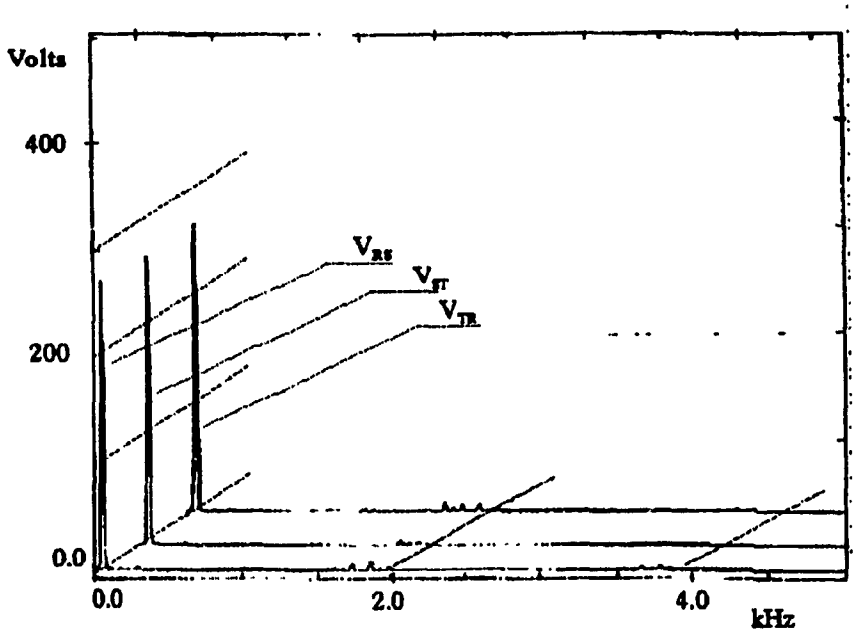

Fig. 3.14 - Experimental Results. Spectrum of the load line-to-line voltages with filter- VL_{ab}, VL_{bc} and VL_{ca}

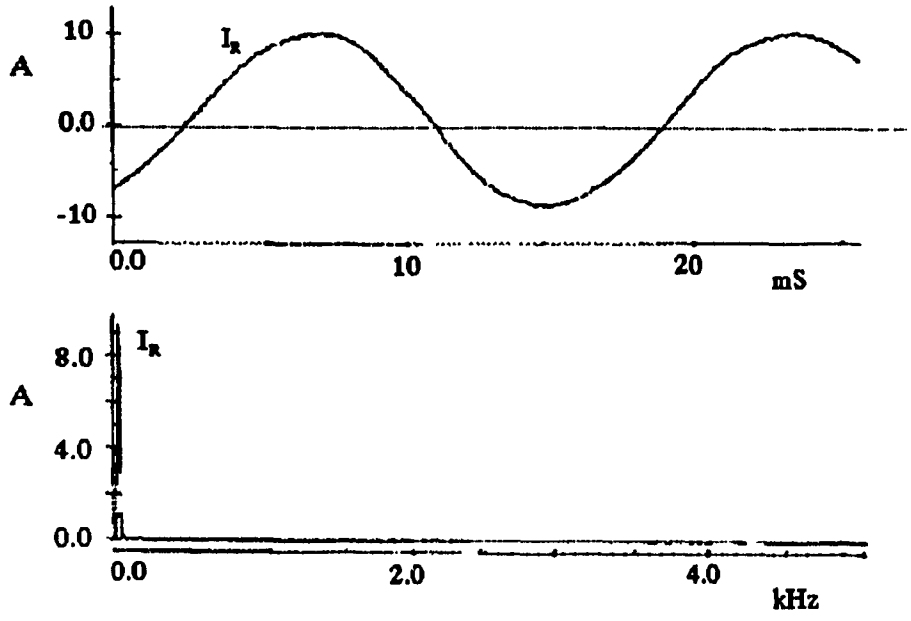

Fig. 3.15 - Experimental Results Without Filter. Top - Load line current.Bottom - Spectrum of the load line current

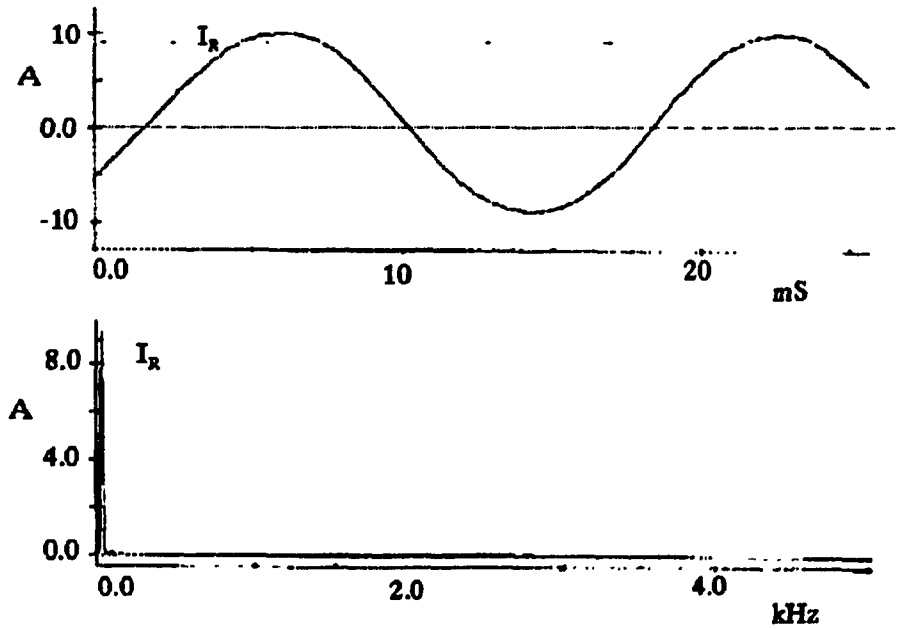

Fig. 3.16 - Experimental Results. Top - Load line current with filter .Bottom - Spectrum of the load line current with filter

3.7. Conclusions

A series voltage compensator for three-phase unbalanced sources has been presented and analyzed. The system, based on three single-phase voltage source inverters connected in series with the supply using transformers, proved to be feasible and performed as expected. A 2.2 kVA prototype was built and used to compensate a source with 13.8% (UF=0.138) unbalance and 7.7% magnitude error (MF=0.923). Simulation and experimental results showed a very good correlation with the expected performance, balanced line-to-line load voltages with low THD being produced. The total power required by the compensator was reasonably low (0.14 pu).

CHAPTER 4

VOLTAGE UNBALANCE COMPENSATOR BASED ON A THREE PHASE VSI OPERATING WITH UNBALANCED SWITCHING FUNCTIONS

4.1 Introduction

An alternative to the series unbalance compensator presented in chapter 3, also based on series connected force commutated converters, is proposed in this chapter. The proposed compensator overcomes disadvantages of conventional ac controllers, such as high kVA ratings and high harmonic injection. At the same time the number of switches and the volume of the magnetic parts are reduced, when compared to the compensator presented in the previous chapter.

The voltage unbalance present in three-phase ac supply is eliminated using a low kVA rating series connected compensator. It consists of a three-phase voltage source inverter connected to the power system through a transformer. The negative sequence component of the supply line-to-line voltage is extracted and eliminated from the input voltage, reducing the load voltage to a balanced system with amplitude given by the positive sequence. It is shown that by having the inverter operate with unbalanced switching functions it is also possible to control the amplitude of the positive sequence component. This allows the system to also perform load voltage regulation. The use of pulse-width modulation (PWM) results in a system with fast dynamic response, and the possibility of

using a high switching frequency allows a considerable reduction in the power rating of the required filter.

4.2. Principle of Operation

The structure of the proposed system is introduced by the simplified diagram presented in Fig. 4.1. The line-to-line voltages of the three-phase voltage source are assumed unbalanced and are given by (4.1).

$$Vs_{abc} = \begin{bmatrix} \hat{V}s_{ab} \\ \hat{V}s_{bc} \\ \hat{V}s_{ca} \end{bmatrix} \tag{4.1}$$

These voltages can be decomposed in two balanced three-phase systems using symmetrical components transformation, as shown in (4.2).

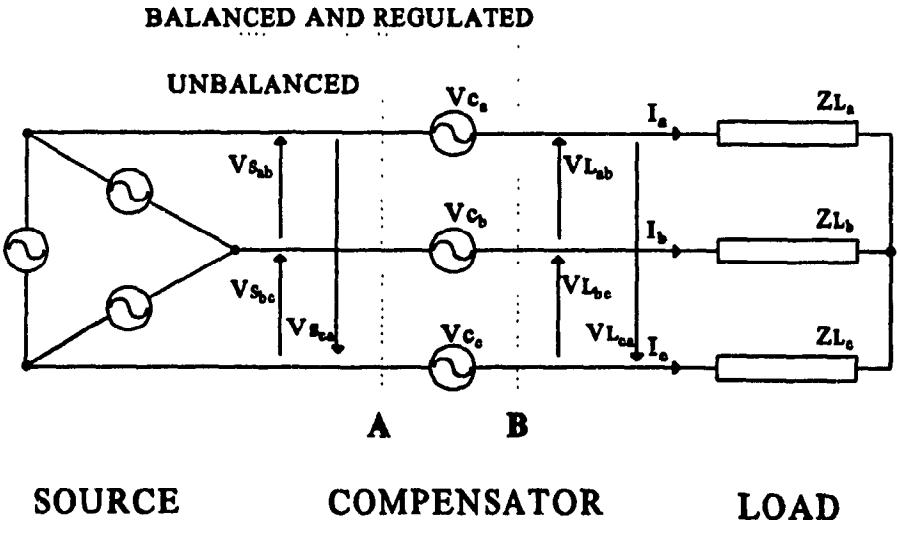

Fig. 4.1 - Simplified representation for an unbalance compensator.

$$\mathbf{Vs}_{012} = \begin{bmatrix} \hat{V}s_0 \\ \hat{V}s_1 \\ \hat{V}s_2 \end{bmatrix} = \mathbf{A}^{-1} \cdot \mathbf{Vs}_{abc} \tag{4.2}$$

Where **A** is the transformation matrix, given by:

$$\mathbf{A}^{-1} = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix}$$

$$\mathbf{A} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ i & \alpha & \alpha^2 \end{bmatrix} \tag{4.3}$$

and $\alpha = e^{j120}$

Assuming there is no neutral path in the system, the zero sequence component $\hat{V}s_0$ must be zero. The system shown in Fig. 4.1 is then reduced to the positive and the negative sequence ($\hat{V}s_1$ and $\hat{V}s_2$) equivalents shown in the unipolar diagrams in Fig. 4.2. The compensator line-to-line voltages ($\mathbf{Vc}_{abc}$) are expressed by (4.4), where the indexes *1* and *2* refer to the positive and negative sequence components, respectively.

$$\left\{ \begin{array}{l} \mathbf{Vc}_{abc1} = \begin{bmatrix} \hat{V}c_{ab1} \\ \hat{V}c_{bc1} \\ \hat{V}c_{ca1} \end{bmatrix} = \begin{bmatrix} \hat{V}L_{ab1} \\ \hat{V}L_{bc1} \\ \hat{V}L_{ca1} \end{bmatrix} - \begin{bmatrix} \hat{V}s_{ab1} \\ \hat{V}s_{bc1} \\ \hat{V}s_{ca1} \end{bmatrix} \\ \\ \mathbf{Vc}_{abc2} = \begin{bmatrix} \hat{V}c_{ab2} \\ \hat{V}c_{bc2} \\ \hat{V}c_{ca2} \end{bmatrix} = \begin{bmatrix} \hat{V}L_{ab2} \\ \hat{V}L_{bc2} \\ \hat{V}L_{ca2} \end{bmatrix} - \begin{bmatrix} \hat{V}s_{ab2} \\ \hat{V}s_{bc2} \\ \hat{V}s_{ca2} \end{bmatrix} \end{array} \right\} \tag{4.4}$$

The unbalance compensation is achieved by forcing the negative sequence of the load voltage ($\mathbf{VL}_{abc2}$) to be zero (voltages at the section B in Fig. 4.2), which can be implemented by making the negative sequence component of the compensator voltages ($\mathbf{Vc}_{abc2}$) equal to the source negative sequence component.

In order to perform voltage regulation the positive sequence component of the load voltage (section A in Fig. 4.2) has to be adjusted to a given voltage reference $\mathbf{V}_{ref}$. This is done by adding to the source a voltage proportional to its positive sequence component.

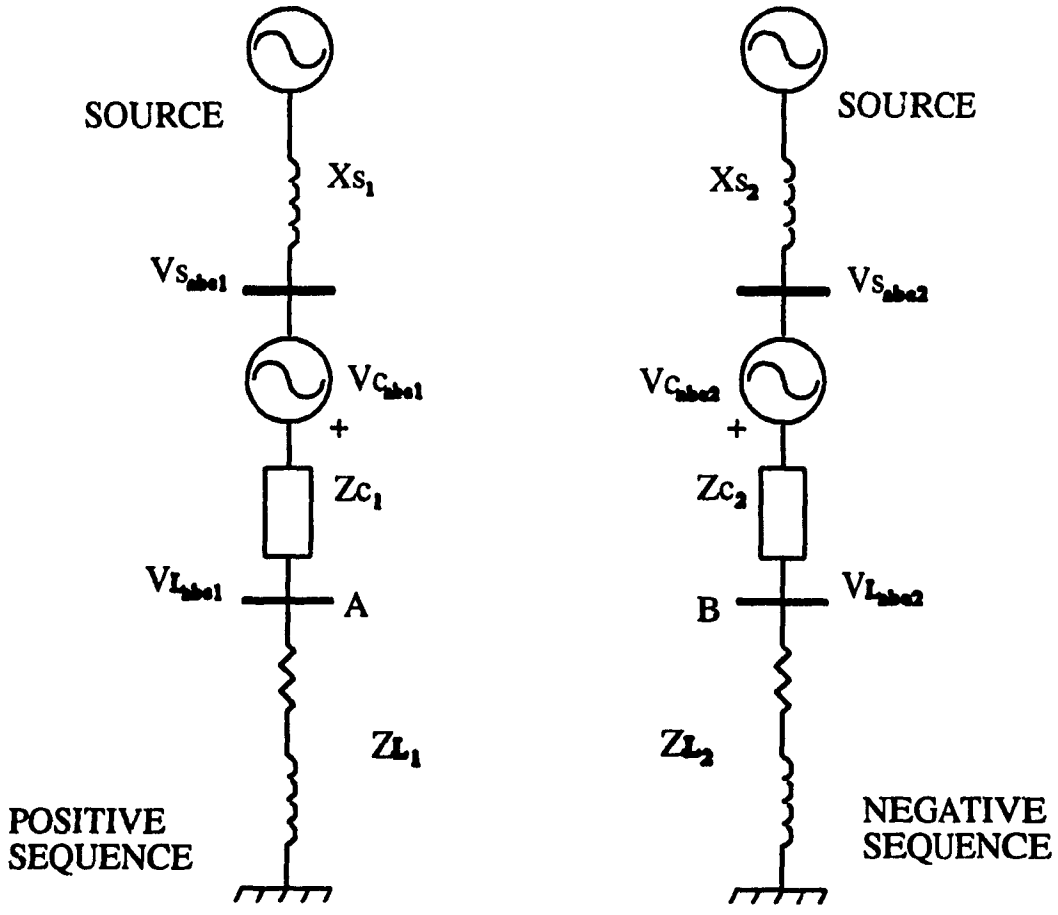

Fig. 4.2 - Simplified representation of the compensation scheme by its symmetrical components equivalent.

Fig. 4.3 shows the correspondent set of phasors of the ab line-to-line voltage, where $\hat{V}s_{ab1}$ and $\hat{V}s_{ab2}$ are the positive and the negative sequences, $\hat{V}c_{ab}$ is the compensator ab line-to-line voltage and $\hat{V}L_{ab}$ is the load line-to-line voltage.

Using the vector operators T_1 and T_2 as shown and the reference voltage V_{ref} as a base voltage, (4.3) can be reduced to,

$$\left\{ \begin{array}{l} Vc_{abc1} = T_1 \cdot (1 - \dfrac{\hat{V}s_{ab1}}{\hat{V}_{ref}}) = T_1 \cdot (1 - \dfrac{\hat{V}s_1}{\hat{V}_{ref}}) \\ \\ Vc_{abc2} = - T_2 \cdot \dfrac{\hat{V}s_{ab2}}{\hat{V}_{ref}} = - T_2 \cdot \dfrac{\hat{V}s_2}{\hat{V}_{ref}} \end{array} \right\} \quad \text{pu} \qquad (4.5)$$

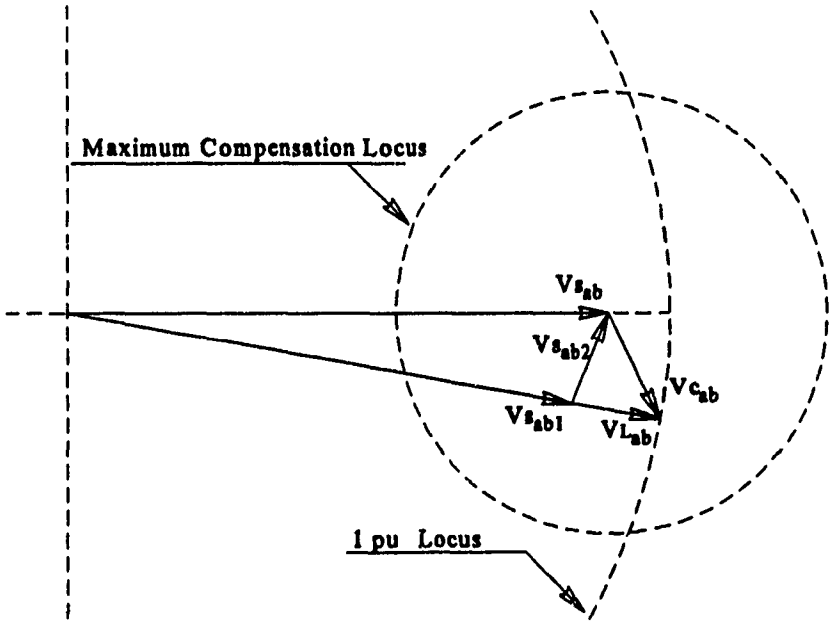

Fig. 4.3 - Compensation procedure for the ab line-to-line voltage.

where

$$\mathbf{T}_1 = \begin{bmatrix} 1 \\ \alpha^2 \\ \alpha \end{bmatrix} \tag{4.6}$$

$$\mathbf{T}_2 = \begin{bmatrix} 1 \\ \alpha \\ \alpha^2 \end{bmatrix} \tag{4.7}$$

The unbalance factor, defining as per IEC [33], is the ratio between the negative and the positive sequence components, and defining the magnitude factor as the ratio between the positive sequence component and the reference voltage:

$$\vec{UF} = \frac{\vec{V}_{S_2}}{\vec{V}_{S_1}} = |\vec{UF}|\angle\phi_{UF} \qquad \text{pu} \tag{4.8}$$

$$\vec{MF} = \frac{\vec{V}_{S_1}}{\vec{V}_{REF}} = |\vec{MF}|\angle\phi_{MF} \qquad \text{pu} \tag{4.9}$$

Using these definitions (4.5) is simplified to (4.10).

$$\left\{ \begin{array}{l} \mathbf{Vc}_{abc1} = \mathbf{T}_1 \cdot (1 - \vec{MF}) \\ \mathbf{Vc}_{abc2} = -\mathbf{T}_2 \cdot \vec{UF} \cdot \vec{MF} \end{array} \right\} \qquad \text{pu} \tag{4.10}$$

This set of equations defines the required line-to-line voltages that performs the unbalance compensation and load voltage control.

On a pu basis, the primary and the secondary transformer voltages are equal and can be calculated by wye-delta transformations for positive and negative sequence components, as follows.

$$\left\{ \begin{bmatrix} \hat{V}c_{a1} \\ \hat{V}c_{b1} \\ \hat{V}c_{c1} \end{bmatrix} = (1 - \bar{M}F) \cdot \frac{T_1}{1-\alpha^2} \right\} \quad \text{pu} \qquad (4.11)$$

$$\left\{ \begin{bmatrix} \hat{V}c_{a2} \\ \hat{V}c_{b2} \\ \hat{V}c_{c2} \end{bmatrix} = -\bar{U}F \cdot \bar{M}F \cdot \frac{T_2}{1-\alpha} \right\}$$

With a proper design the filter stage does not affect the fundamental component. Thus the fundamental component of the line-to-line voltages at the output of the inverter are defined by (4.11) and by the primary connection of the transformer. For a delta connected primary,

$$\left\{ \begin{array}{l} V_{l_{abc1}} = \begin{bmatrix} \hat{V}c_{a1} \\ \hat{V}c_{b1} \\ \hat{V}c_{c1} \end{bmatrix} \\ \\ V_{l_{abc2}} = \begin{bmatrix} \hat{V}c_{a2} \\ \hat{V}c_{b2} \\ \hat{V}c_{c2} \end{bmatrix} \end{array} \right\} \quad \text{pu} \qquad (4.12)$$

Total value can be obtained by adding both sequence components:

$$V_{l_{abc}} = \frac{T_1}{(1-\alpha^2)} - \bar{M}F \cdot \left(\frac{T_1}{(1-\alpha^2)} + \frac{T_2}{(1-\alpha)} \cdot \bar{U}F \right) \quad \text{pu} \qquad (4.13)$$

4.3. Derivation of the Switching Functions and Gating Signals

The implementation of both unbalance elimination and load voltage regulation requires a compensator providing an unbalanced set of voltages, with fundamental components given by (4.12). Under these conditions the inverter operates with unbalanced switching functions, and the determination of these functions, i.e. the reference signals and the gating signals (or modulation index) does not follows the standard procedure.

The fundamental components of the inverter switching functions, defined as the inverter line-to-line output voltages normalized to the dc-bus voltage, are as follows:

$$\left\{ \begin{aligned} \mathbf{F}_{abc1} &= \begin{bmatrix} \hat{F}_{ab1} \\ \hat{F}_{bc1} \\ \hat{F}_{ca1} \end{bmatrix} = \frac{T_1}{V_{dc}\cdot(1-\alpha^2)} \cdot (1-\hat{MF}) \\ \mathbf{F}_{abc2} &= \begin{bmatrix} \hat{F}_{ab2} \\ \hat{F}_{bc2} \\ \hat{F}_{ca2} \end{bmatrix} = -\frac{T_2}{V_{dc}\cdot(1-\alpha)} \cdot \hat{UF}\cdot\hat{MF} \end{aligned} \right\} \quad \text{pu} \qquad (4.14)$$

These expressions are independent on the modulation scheme used, and can be used as a starting point to design the modulator. When using a carrier-based PWM technique, the determination of the reference signals (or modulation index) is facilitated by the linear transfer characteristic of the inverter, which implies a linear relationship between the fundamental component of the output voltage and the modulation index (overmodulation excluded). In this case the superposition theorem holds and the fundamental components of the reference signals can be determined by dividing the line-to-capacitor mid-point voltages (fictitious central point between the filter capacitors in Fig. 4.4) by the gain of the

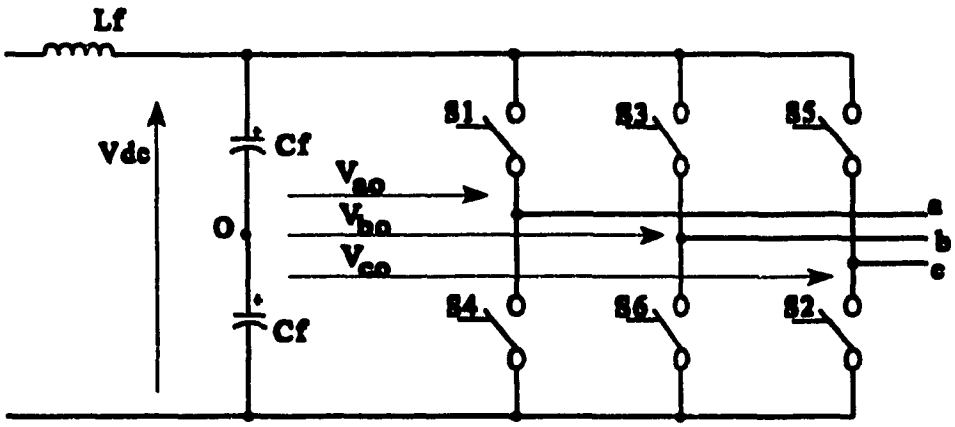

Fig. 4.4 - Simplified structure of the voltage source inverter used.

fundamental component of the PWM scheme being used (G_i).

For the inverter shown in Fig. 4.4, the fundamental component of the line-to-capacitor mid-point voltages can be obtained by a delta-wye transformation on (4.12) as follows:

$$\left\{ \begin{bmatrix} \hat{V}_{ao1} \\ \hat{V}_{bo1} \\ \hat{V}_{co1} \end{bmatrix} = \frac{F_{abc1}}{(1-\alpha^2)} \right\} \qquad \text{pu} \qquad \textbf{(4.15)}$$

$$\left\{ \begin{bmatrix} \hat{V}_{ao2} \\ \hat{V}_{bo2} \\ \hat{V}_{co2} \end{bmatrix} = -\frac{F_{abc2}}{(1-\alpha)} \right\}$$

Therefore the total value of the reference signals are:

$$\left\{ \begin{aligned} \mathbf{R}_{abc1} &= \begin{bmatrix} R_{a1} \\ R_{b1} \\ R_{c1} \end{bmatrix} = \frac{T_1 \cdot (1 - \vec{MF})}{Gi \cdot V_{dc} \cdot (1-\alpha^2)^2} \\ \mathbf{R}_{abc2} &= \begin{bmatrix} R_{a2} \\ R_{b2} \\ R_{c2} \end{bmatrix} = \frac{-T_2 \cdot \vec{UF} \cdot \vec{MF}}{Gi \cdot V_{dc} \cdot (1-\alpha)^2} \end{aligned} \right\} \quad \text{pu} \qquad (4.16)$$

and the final value is given by adding the positive and the negative sequence components:

$$\mathbf{R}_{abc} = K_1 - \vec{MF} \cdot (K_1 + \vec{UF} \cdot K_2) \qquad \text{pu} \qquad (4.17)$$

where,

$$\left\{ \begin{aligned} K_1 &= \frac{T_1}{Gi \cdot V_{dc} \cdot (1-\alpha^2)^2} \\ K_2 &= \frac{T_2}{Gi \cdot V_{dc} \cdot (1-\alpha)^2} \end{aligned} \right\} \quad \text{pu} \qquad (4.18)$$

For implementation purposes any carrier-based PWM can be used. The only restriction is the linearity between reference (modulation index) and output voltage. For example, Figs. 4.5 and 4.6 show the waveforms for a sine pulse-width modulator with an unbalance factor of 15% (UF=0.15) and a magnitude error of 10% (MF=0.9). The transformer is assumed with a delta connection in the primary, and the reference voltages were obtained from (4.17).

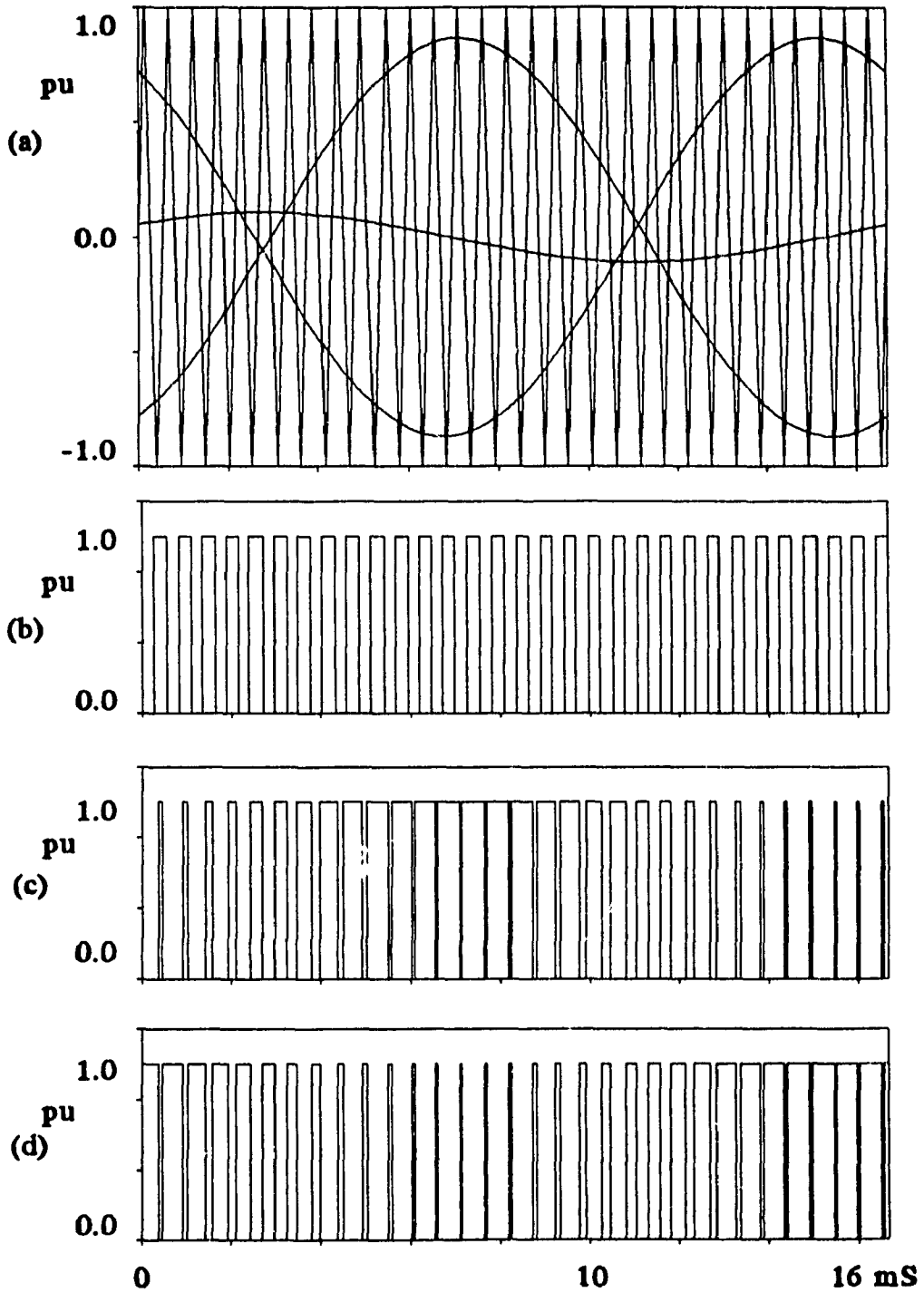

Fig. 4.5 - Unbalanced sine PWM. a) References and carrier signals. Gating signals: b) G1 ; c) G3 ; d) G5

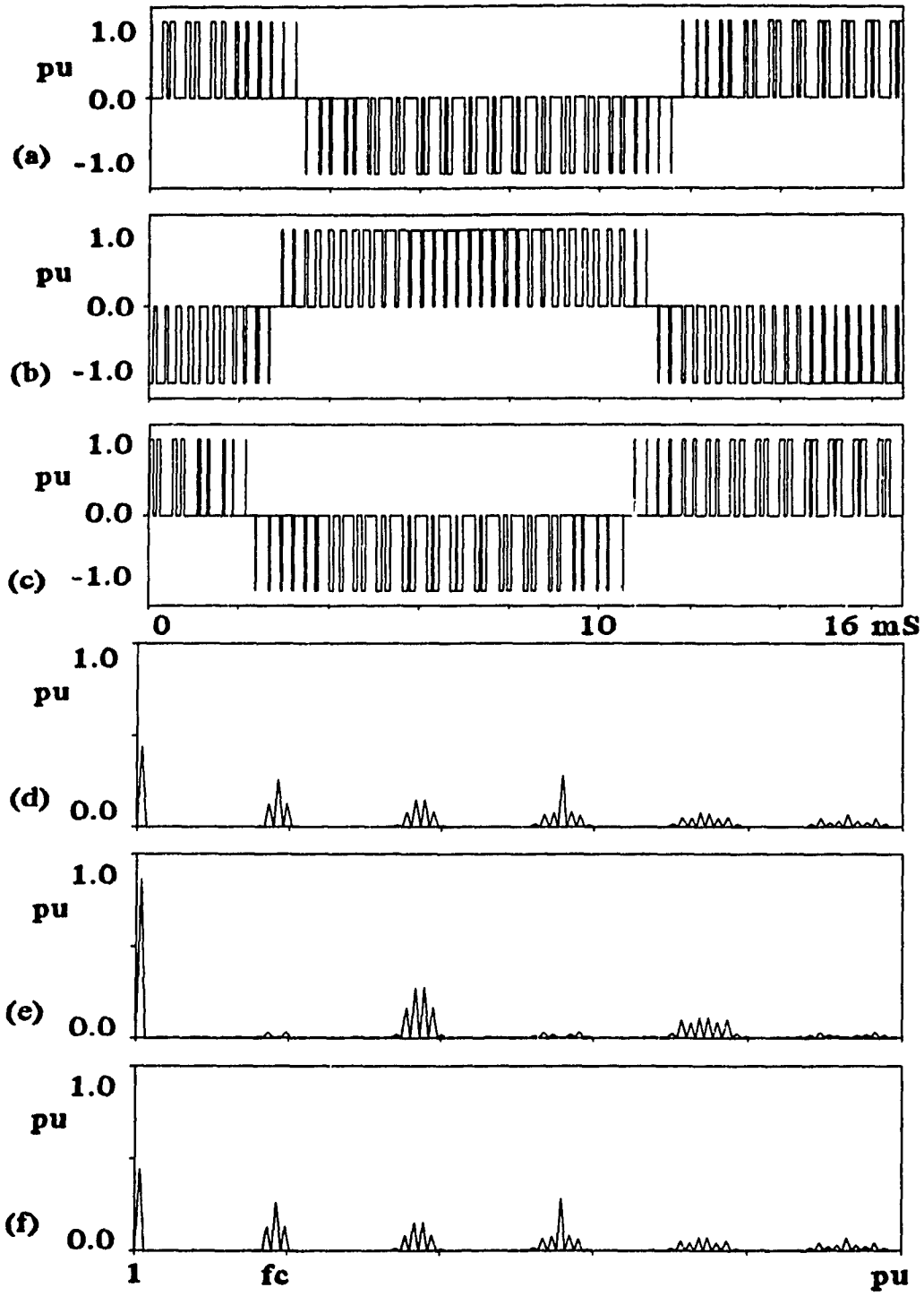

Fig. 4.6 - Unbalanced sine PWM. a, b and c) Inverter line-to-line voltages. d, e and f) Spectra.

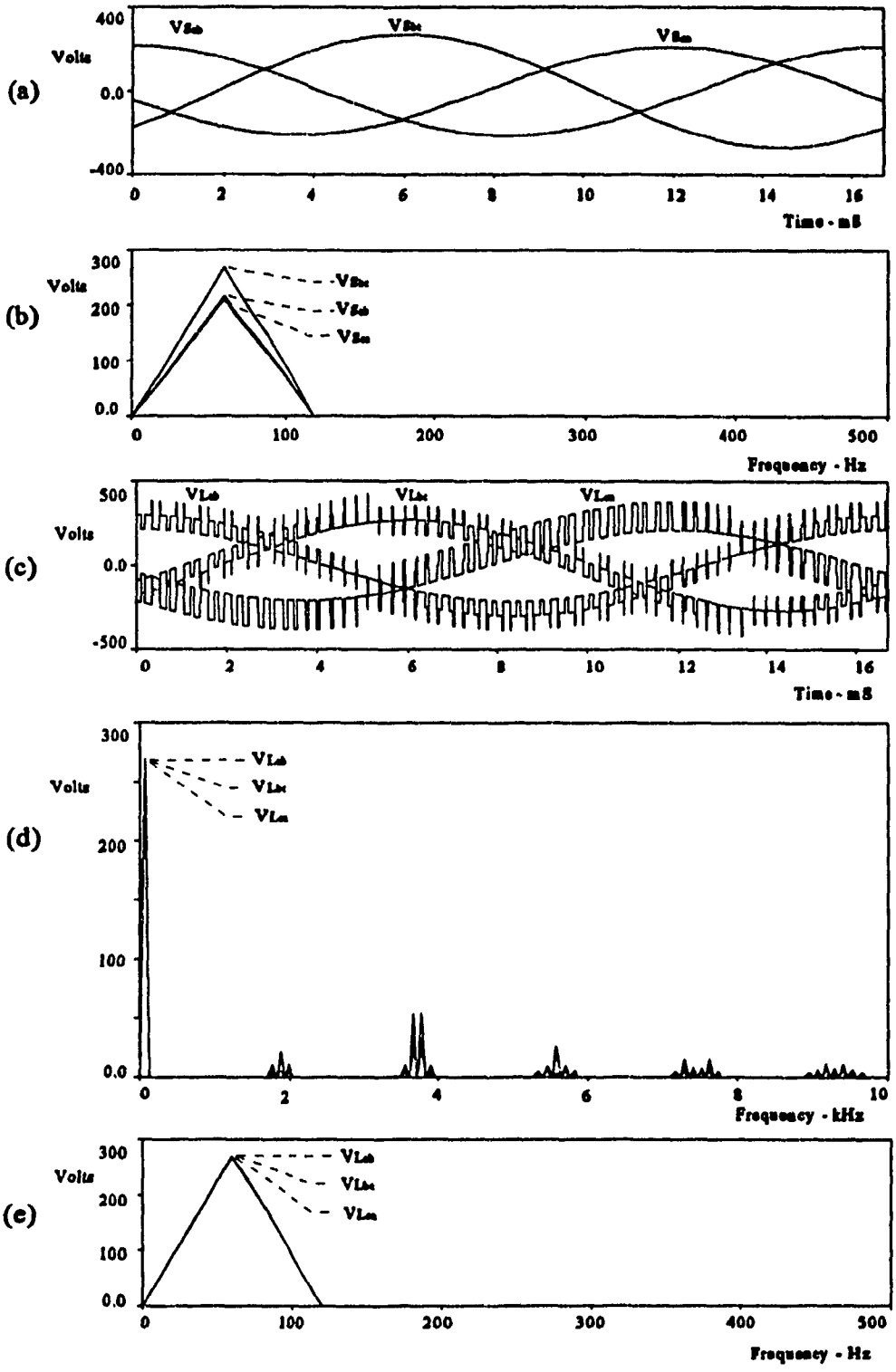

Fig. 4.7 - Simulation results. a) Source voltages; b) Source voltages - spectra; c) Load voltages; d) and e) Load voltages - spectra.

These reference signals were used in a simulation of the compensation scheme, and the results are presented in Fig.4.7. The compensation is achieved and demonstrated by Figs. 4.7.d and 4.7.e, where the spectra of the fundamental component of both source and load voltages are presented.

4.4 System Description

Fig. 4.8 shows the circuit used to implement the proposed compensator. It consists basically on a three-phase PWM voltage source inverter connected in series with the line through a delta-wye three-phase transformer. A dc source is required to provide four quadrant operation to the compensator, allowing it to perform the compensation under any condition of voltage drop in the source.

Unbalance compensation and load voltage regulation are achieved by controlling the amplitude and the phase of the reference voltages R_a, R_b and R_c of the modulator. This set of voltages, for a given condition of unbalance and voltage error, can be obtained by (4.17), where all parameters but UF and MF are constants.

The calculation of both the unbalance and magnitude factors and the solution of (4.17) require a reasonable large number of vector operations, making the analog implementation of the control subsystem and the filter for symmetrical components a non practical approach. A fast digital signal processor is suggested to extract the symmetrical components from the load line-to-line voltages, as shown in Appendix A.

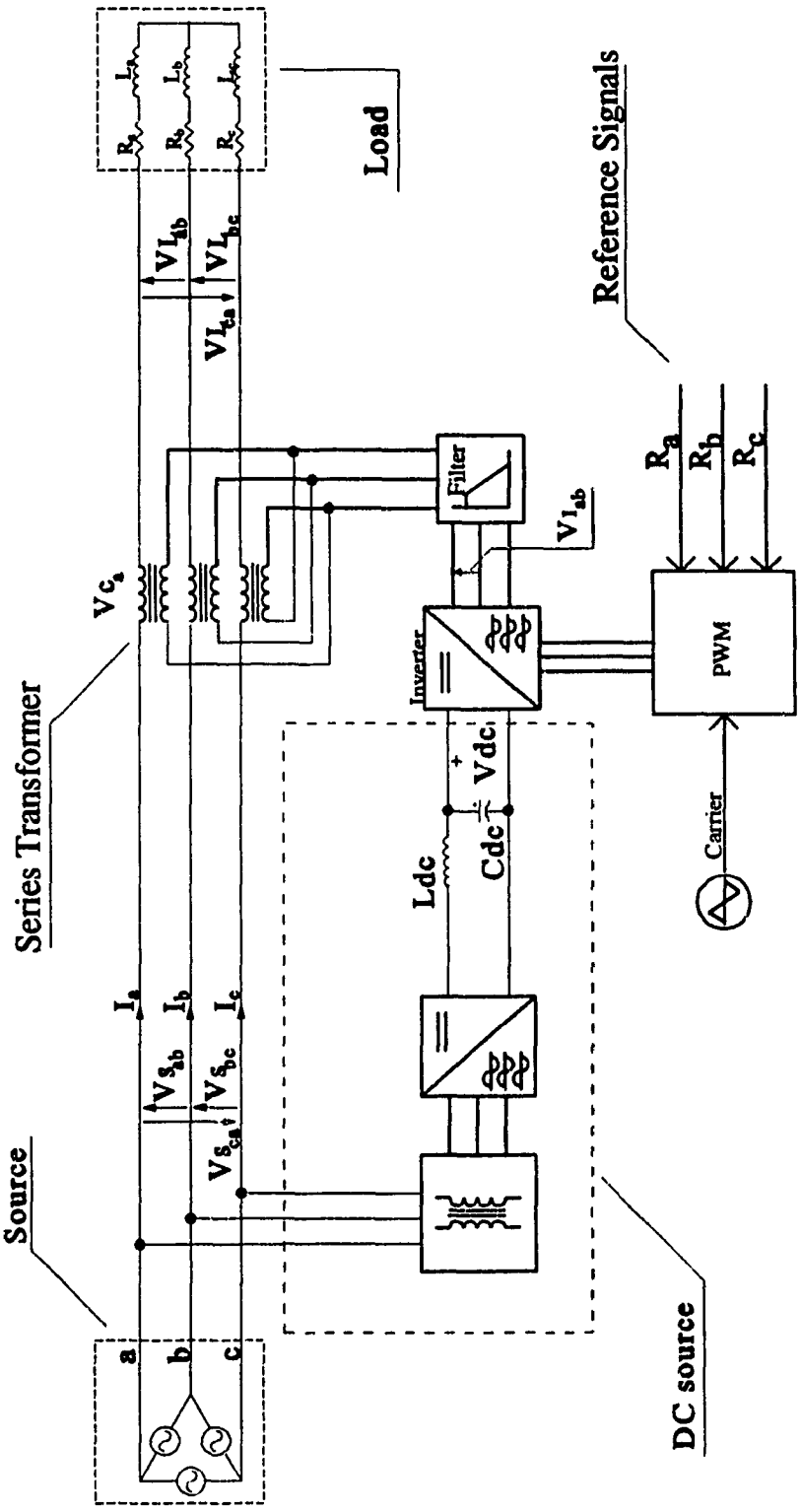

Fig. 4.8 - Diagram of the proposed series unbalance compensator.

The DSP should also be used to solve (4.17), generating the appropriate reference signals for the modulator.

Eventhough the harmonics injected by the compensator is reasonably low, a small second-order filter can be connected between the inverter and the transformer to reduce the harmonic content of the injected voltage, which reduces the load voltage THD. The design of this filter is presented in the section 4.

4.5. System Design

The design of the proposed system follows the same procedure described in Chapter 3. The starting point is the definition of the magnitude of the maximum allowed unbalance factor ($|\vec{UF}|_{max}$), and the maximum error in the magnitude of the positive sequence component, which is given by $1 - |\vec{MF}|_{min}$. The unbalance factor can be chosen based on the NEMA factor as shown in Chapter 3, equation (3.6) or Fig. 3.3.

The value of the dc bus voltage Vdc is specified by a cost evaluation of the switches and filter capacitors.

The following assumptions are used in this design.

i) The switches are ideal.

ii) The filter components are ideal.

iii) The base value for the power (S_{BASE}) is the rated load power.

iv) The base value for the voltage (V_{BASE}) is the infinite bus line-to-line voltage.

v) The base voltage in the inverter side (VI_{BASE}) is calculated using the series transformer turns ratio.

4.5.1. Power requirements

The power required to perform the compensation is defined in pu by the maximum compensation voltage V_{Cmax}. Fig. 3.3 is still valid to the present design, thus it can be used to calculate S_C, which magnitude is expressed by:

$$S_C = \sqrt{3} \cdot Vc_{max} = \sqrt{3} \cdot (1 - |\vec{MF}|_{min} * (1 - |\vec{UF}|_{max})) \quad pu \qquad (4.19)$$

The real power supplied or absorbed at any moment by the compensator is defined by the load power factor and by the value of the positive sequence component of the compensation voltage (Vcabc1). If voltage regulation is not needed for a particular application (i.e. if only unbalance compensation is desired), then no real power is required and the dc source can be eliminated. The worst case, for unity load power factor and maximum positive sequence component (full voltage regulation), the compensator real power is given by,

$$P_C = S_C = \sqrt{3} \cdot Vc_{max} \qquad pu \qquad (4.20)$$

This value can be reduced in some cases using the considerations presented in Chapter 2. For these applications, where a limit for the voltage drop on resistive elements

can be specified, the rated real power can be reduced to a minimum value, which minimizes the size and cost of the dc source.

4.5.2. Series transformer design

With the maximum unbalance factor and the minimum magnitude factor defined, the maximum secondary voltage of the transformer is given, by the following equation.

$$Vc_{max} = \frac{1 - |\vec{M}F|_{min} * (1 - |\vec{U}F|_{max})}{\sqrt{3}} \quad pu \quad (4.21)$$

The transformer turns ratio and primary voltage depend on the maximum output voltage of the inverter and on the transformer configuration. Assuming that the inverter gain for the fundamental component of the line-to-line voltage is G_i, the dc bus voltage is V_{dc}, and the transformer has its primary connected in delta, its turns ratio is:

$$N_T = \frac{Vc_{max}}{Gi \cdot V_{dc}} \quad pu \quad (4.22)$$

Due to the series connection, the rated current in the transformer is one pu, and the total apparent power is given in pu by the maximum secondary voltage, as follows.

$$S_{T_{max}} = Sc_{max} = \sqrt{3} \cdot Vc_{max} \quad pu \quad (4.23)$$

4.5.3 Design of the Voltage Source Inverter.

The design of the inverter involves the specification of the topology to be used, the modulation technique, and the switches to be used and their ratings.

A three-phase bridge voltage source inverter, with bipolar transistors as switches is used. The inverter can be controlled by any carrier-based PWM technique. In this case it is chosen a sine pulse-width modulation technique (SPWM).

Assuming the filter is properly designed, no current harmonics will pass through the inverter, thus the current in any switch will be very close to sinusoidal. The current ratings for the switches are then given by:

$$\left\{ \begin{array}{l} I_{SW_{rms}} = \dfrac{1}{\sqrt{2}} \\ I_{SW_{pk}} = \sqrt{2} \\ I_{SW_{avg}} = \dfrac{1}{\pi} \end{array} \right\} \quad \text{pu} \qquad (4.24)$$

The voltage rating is given by the following equations.

$$\left\{ \begin{array}{l} V_{SW_{rms}} = \dfrac{1}{\sqrt{6}} \cdot \sqrt{\sum_{n=1}^{\infty} \left(V_{I_n}\right)^2} \\ V_{SW_{pk}} = V_{dc} \end{array} \right\} \quad \text{pu} \qquad (4.25)$$

The apparent power required from the inverter is higher than that of in the transformer due to the presence of harmonics in the output voltage, and it is given by:

$$S_I = \sqrt{\sum_{n=1}^{\infty} (V_{I_n})^2} \quad \text{pu} \qquad (4.26)$$

4.5.4. Design of the Inverter Output Filter.

The method used to design the filter for the output of the inverter is the same as the one used in Chapter 3. The voltage harmonics injected by the inverter in the present case are smaller than the previous (Chap.3). Analysis of such a system can be done on a per phase basis due to the fact the worst case occurs either with balanced or unbalanced voltages. The equivalent circuit is shown in Fig. 4.9, where the inverter output voltage and the load current are modelled by their harmonic component, specified by the index *n*.

Using the method described in the previous chapter, the value of the inductor

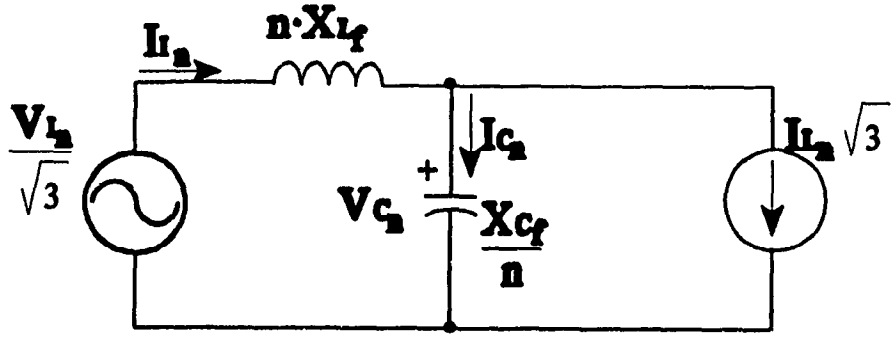

Fig. 4.9 - Equivalent circuit used for designing the inverter output filter.

reactance is calculated as follows.

$$XL_f = \frac{K_1}{THD_i} \qquad \text{pu} \qquad \textbf{(4.27)}$$

where

$$K_1 = \frac{1}{\sqrt{3}} \cdot \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n}\right)^2} \qquad \text{pu} \qquad \textbf{(4.28)}$$

The rms value of the voltage across the capacitor due to the harmonics is:

$$Vc_H = \frac{1}{\sqrt{3}} \cdot \frac{XC_f}{XL_f} \cdot \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n^2}\right)^2} \qquad \text{pu} \qquad \textbf{(4.29)}$$

Thus, the capacitor reactance is calculated by taking into account that the relationship between the total harmonic distortion of the load voltage and the capacitor voltage is given by:

$$THD_{Vc} = \frac{V_{C_H}}{V_{C_1}} = \frac{V_{C_H}}{Vc_{max}} = \frac{THD_{VL}}{2\ Vc_{max}} \qquad \textbf{(4.30)}$$

Substituting (4.29) in this last equation, XC_f can be obtained, as shown in the following equation.

$$XC_f = \frac{XL_f \cdot THD_{VL}}{2 \cdot K_2} \qquad \text{pu} \qquad \textbf{(4.31)}$$

where

$$K_2 = \frac{1}{\sqrt{3}} \cdot \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_{I_n}}{n^2}\right)^2} \qquad \text{pu} \qquad \textbf{(4.32)}$$

Figs. 4.10 and 4.11 present the relationship between XC_f and XL_f ((4.31 and (4.27)) obtained for a three-phase SPWM bridge voltage source inverter at unity modulation index with $|\vec{UF}|_{max} = 20\%$, $|\vec{MF}|_{min} = 80\%$.

The kVA ratings for C_f and L_f are calculated from (4.33) and (4.34), respectively.

$$SC_f = \frac{Vc_{max}}{XL_f} \cdot \frac{K_1}{\sqrt{3}} \cdot \sqrt{(1 + THD_{Vc}^2)} \approx \frac{Vc_{max} \cdot THD_i}{\sqrt{3}} \quad pu \qquad (4.33)$$

$$SL_f = \frac{K_0}{\sqrt{3}} \cdot \sqrt{(1 + THD_i^2)} \approx \frac{K_0}{\sqrt{3}} \quad pu \qquad (4.34)$$

where K0 is defined as,

$$K_0 = \frac{1}{\sqrt{3}} \cdot \sqrt{\sum_{n=2}^{\infty} (V_{I_n})^2} \quad pu \qquad (4.35)$$

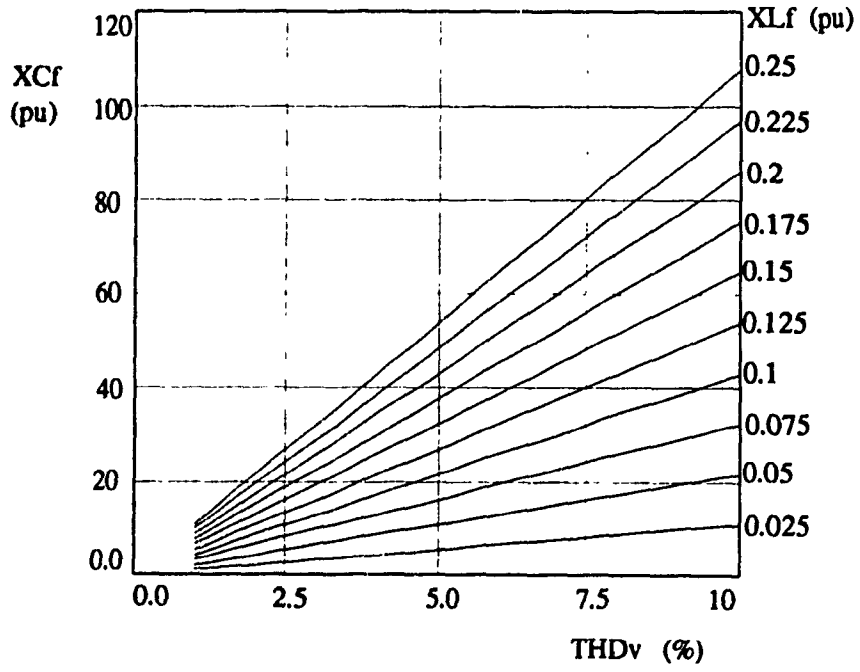

Fig. 4.10 - Inverter filter design - Capacitor reactance.

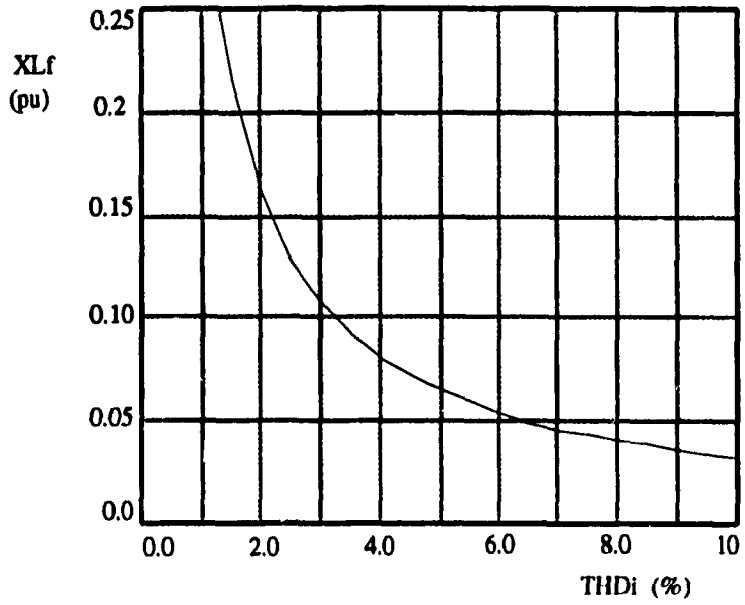

Fig. 4.11 - Inverter filter design - Inductor reactance.

For the case of a sine PWM bridge voltage source inverter, the value of K_i is 0.003. Also, for low values of THDi and THDVL the approximations shown in (4.33) and (4.34) are valid, which makes the kVA ratings of the inductor constant and equal to 0.072 pu.

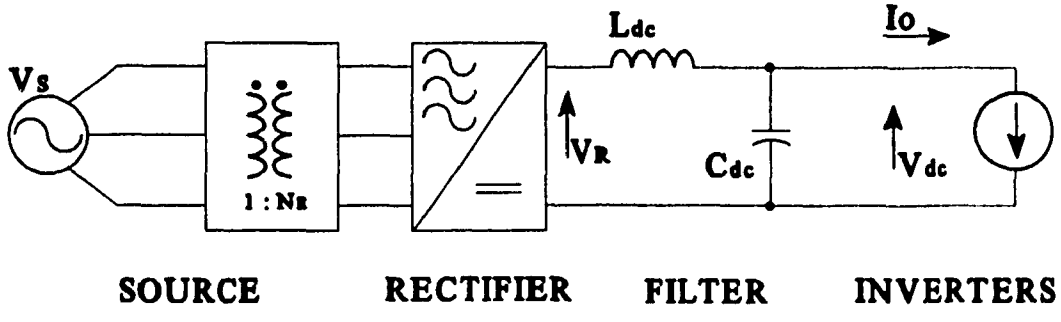

Fig. 4.12 - Equivalent circuit used for designing the dc source.

4.5.5. Design of the dc source.

The dc source consists of a transformer, a rectifier and a filter, connected as shown in Fig. 4.12. Its design depends on the desired mode of operation of the compensator. For the general case, operating in four quadrants (supply or absorb real and reactive power), the compensator requires a dc source capable of operate in two quadrants.

The starting point for the design of such a circuit is the definition of the amount of real power that the compensator is allowed to provide to the system (Pc_{max}). As already mentioned in the sections 3.4.1 and 4.5.1, if the real power is made zero, the compensator becomes a series var compensator, and the dc source is not necessary. For design purposes it is assumed that the compensator is required only to supply real power, thus the dc source does not need to regenerate current, and a diode rectifier can be used to implement it. In this case the ratings for the rectifier are,

$$\left\{ \begin{array}{l} V_{SW\,rms} = \dfrac{V_{dc}}{\sqrt{3}} \cdot \sqrt{\dfrac{\pi^2}{9} + \dfrac{\pi}{2\sqrt{3}}} \\ V_{SW\,pk} = \dfrac{\pi}{3} V_{dc} \\ V_{SW\,avg} = \dfrac{2}{3} V_{dc} \end{array} \right\} \quad \text{pu} \qquad (4.36)$$

$$\left\{ \begin{array}{l} I_{SW\,rms} = \dfrac{1}{\sqrt{3}} \dfrac{P_{dc}}{V_{dc}} \\ I_{SW\,pk} = \dfrac{\pi}{3} \dfrac{P_{dc}}{V_{dc}} \\ I_{SW\,avg} = \dfrac{1}{3} \dfrac{P_{dc}}{V_{dc}} \end{array} \right\} \quad \text{pu} \qquad (4.37)$$

Where Pdc is the required real power (equal to Pcmax), Vdc is the rated dc bus voltage, and Ki is the maximum current ripple in the inductor Ldc.

The apparent power required from the rectifier is,

$$S_R = 1.178 \cdot P_{dc} \qquad \text{pu} \qquad (4.38)$$

The transformer ratings are,

$$\left\{ \begin{array}{l} S_T = 1.178 \cdot P_{dc} \\ V_{T_B} = \dfrac{\pi}{3\sqrt{6}} \cdot V_{dc} \\ V_{T_A} = V_S \\ \dfrac{N_S}{N_P} = \dfrac{\pi}{3\sqrt{6}} \cdot \dfrac{V_{dc}}{V_S} \end{array} \right\} \qquad \text{pu} \qquad (4.39)$$

4.5.6 Design of the dc bus Filter.

Designing the dc bus filter for the proposed compensator follows the same method presented in Chapter 3, with exception for the current harmonics injected by the inverter into the dc bus, which now are due to the operation of a three-phase SPWM inverter.

The expression used in Chapter 3 for the capacitor reactance is still valid for the present case, which is

$$XC_{dc} = \frac{K_V \cdot V_{dc}}{\sqrt{\sum_{n=2}^{\infty} \left(\frac{Io_n}{n} + \frac{V_{R_n}}{n^2 \, XL_{dc}} \right)^2}} \qquad \text{pu} \qquad (4.40)$$

where KV is the ripple of the dc bus voltage Vdc, Ion is the n-th harmonic of the sum of the input currents of all three inverters, VRn is the n-th harmonic of the output voltage of the rectifier, XLdc and XCdc are the inductor and the capacitor reactances (in pu).

In order to calculate both reactances a second parameter is required, and in this case the natural frequency of the filter, given by,

$$f_o = \sqrt{\frac{XC_{dc}}{XL_{dc}}} \qquad \text{pu} \qquad \textbf{(4.41)}$$

is used. These equations are applied to a system with a a three-phase bridge diode rectifier

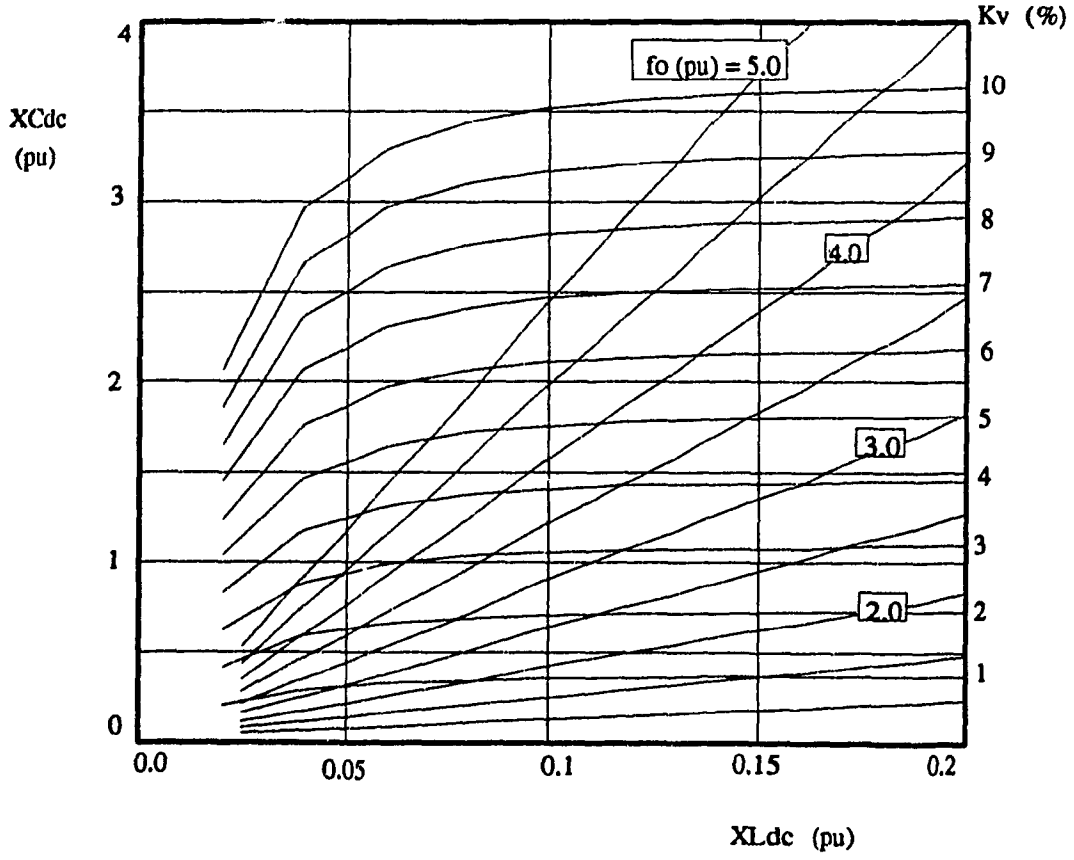

Fig. 4.13 - Dc bus filter capacitor and inductor reactances as functions of the dc bus voltage ripple and the filter break frequency.

and a three-phase bridge SPWM voltage source inverter, and the result is shown graphically in the Fig. 4.13.

4.6. Design Example

In order to illustrate the use of these design equations, the following example is presented. The requirements are: the rated power of the system is 1.3 kVA; the maximum unbalance factor is 20%; the maximum magnitude error is 20% ($|MF| = 0.8$) ; the line-to-line load voltage is $\sqrt{3} \cdot 110$ volts ; a three-phase bridge voltage source inverter is used ; the inverter is controlled with sine PWM modulation with switching frequency of 31 pu; the compensator is required only to supply real power up to the full rated power ($P_{dc} = S_c$); the transformer has a turns ratio of 1:4; the total harmonic distortion for both current and voltage should be $\leq 5\%$; the load power factor is equal to 0.75, lagging. The base values and the result of the design are presented in the following tables.

Table 4.1 - Base Values

Parameter	Value (actual)
S_{BASE}	1.3 kVA
V_{BASE}	190.53 V
Vi_{BASE}	440 V
I_{BASE}	3.94 A
Ii_{BASE}	1.71 A
Z_{BASE}	27.9 Ω
Zi_{BASE}	148.6 Ω
Gi	0.613

Table 4.2 - Transformer Ratings.

Parameter	Equation	Value (pu)	Value (actual)
Power	4.23	0.36	468.4 VA
Primary voltage	---	0.36	158.4 V
Secondary voltage	4.21	0.208	39.6 V
Primary current	---	1	1.71 A
Secondary current	---	1	3.94 A
Turns ratio	4.22	0.25	---

Table 4.3 - Inverter Ratings (Switches Ratings) - Each inverter

Parameter	Equation	Value (pu)	Value (actual)
S_I	4.26	0.387	503.1 VA
V_{dc}		0.587	258.4 V
f_{SW}		31	1.86 kHz
V_{SWpk}	4.25	0.587	258.4 V
V_{SWrms}	4.25	0.158	69.5 V
I_{SWpk}	4.24	1.41	2.48 A
I_{SWavg}	4.24	0.318	0.544 A
I_{SWrms}	4.24	0.707	1.209 A

Table 4.4 - Filter Ratings.

Parameter	Equation	Value (pu)	Value (actual)
S_{Lf}	4.34	0.072	93.9 VA
X_{Lf}	4.27	0.07	10.4 Ω
S_{Cf}	4.33	0.005	6.7 VA
X_{Cf}	4.31	18	2674 Ω

Table 4.5 - DC Source - Rectifier Ratings.

Parameter	Equation	Value (pu)	Value (actual)
S_R	4.38	0.424	551.3 VA
V_{SWpk}	4.36	0.615	270.5 V
V_{SWrms}	4.36	0.48	211.1 V
V_{SWavg}	4.36	0.391	172.2 V
I_{SWpk}	4.37	0.642	1.1 A
I_{SWrms}	4.37	0.354	0.61 A
I_{SWavg}	4.37	0.204	0.35 A

Table 4.6 - Dc Source - Filter Ratings.

Parameter	Equation	Value (pu)	Value (actual)
f_o	4.41	3.5	212 Hz
X_{Ldc}	4.40	0.15	22.3 Ω
X_{Cdc}	4.40	1.8	267.4 Ω

Table 4.7 - Dc Source - Transformer Ratings.

Parameter	Equation	Value (pu)	Value (actual)
S_T	4.39	0.424	551.3 VA
V_{TA}	4.39	1	190.53 V
V_{TB}	4.39	0.251	110.4 V
N_A/N_B	4.39		1:0.58

4.7 Experimental Results

In order to confirm the proposed method a 1.3 kVA prototype, without the filter stage, of the system shown in Fig. 4.8 was built and tested. An unbalance factor of 10.75% and the magnitude error of 9.01% (MF = 0.909) was produced in the source, as shown in the Figs. 4.14 and 4.15.

The results of the compensation are presented in Figs. 4.16 to 4.20 and show a very good correlation with the expected performance.

Particularly, comparing fundamental components of the source line-to-line voltages shown in Fig. 4.15 with the load line-to-line voltages shown in Fig. 4.19, confirm the compensation procedure. Fig. 4.16 to Fig.4.18 show that even without the filter, harmonic content of the load line-to-line voltages is reasonably low (average THD of 20%). The source and the transformer leakage inductances are also factors that contribute to reduce the harmonic content in the load.

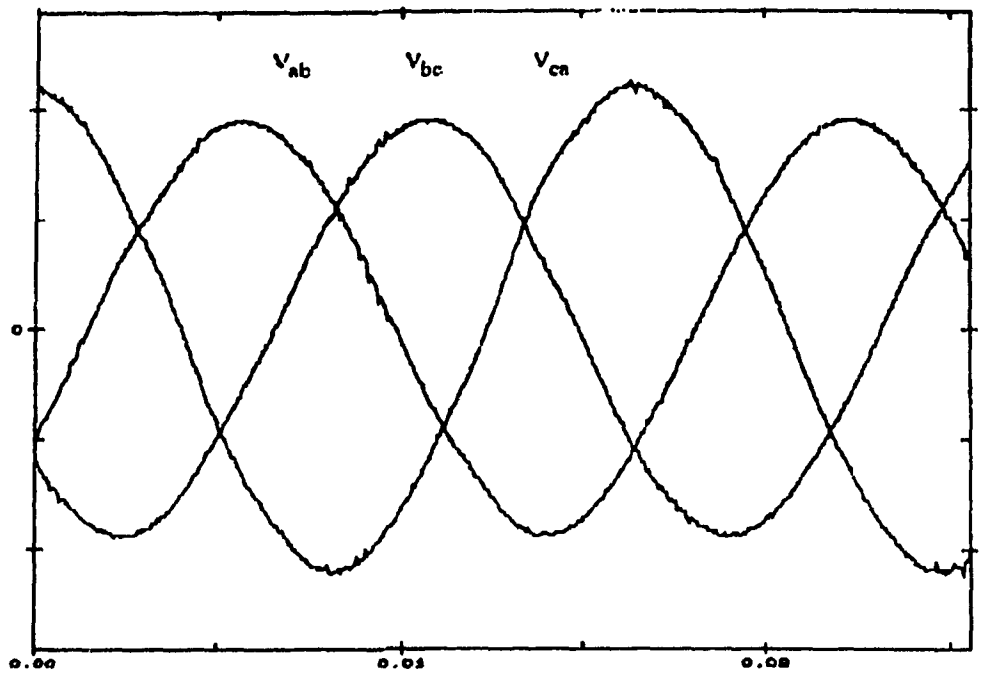

Fig. 4.14 - Source line-to-line voltages - VS_{ab}, VS_{bc} and VS_{ca}. Vertical scale: 125 V/div - Horizontal scale: seconds

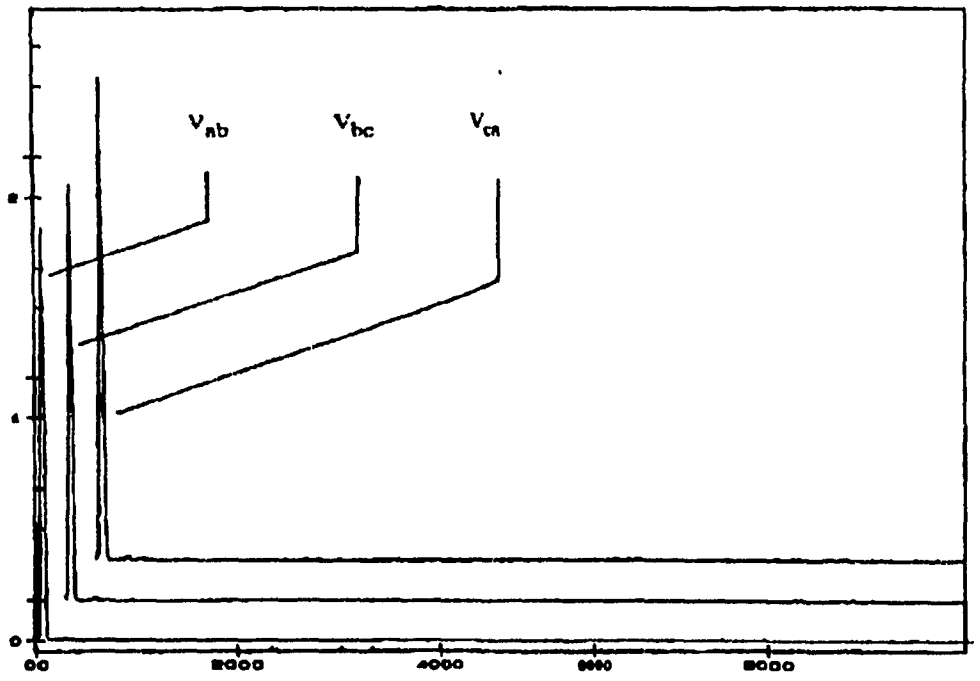

Fig. 4.15 - Spectra of the source line-to-line voltages. Vertical scale : 125 V/div - Horizontal scale : hertz

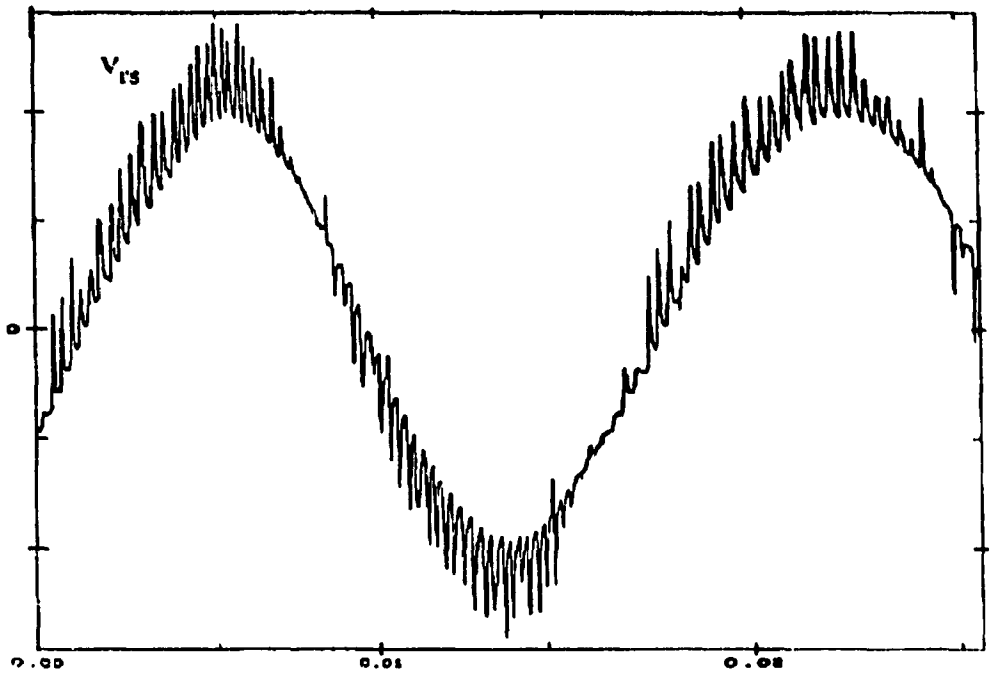

Fig. 4.16 - Load line-to-line voltage - VL_{ab}.Vertical scale : 125 V/div - Horizontal scale : seconds

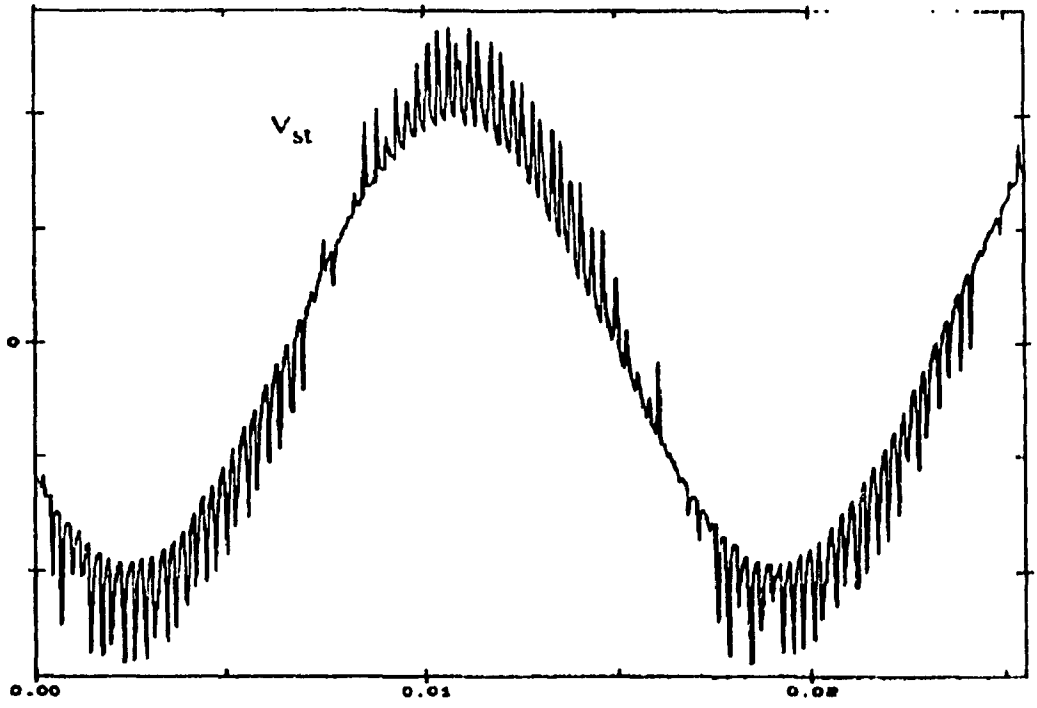

Fig. 4.17 - Load line-to-line voltage - VL_{bc}.Vertical scale : 125 V/div - Horizontal scale : seconds

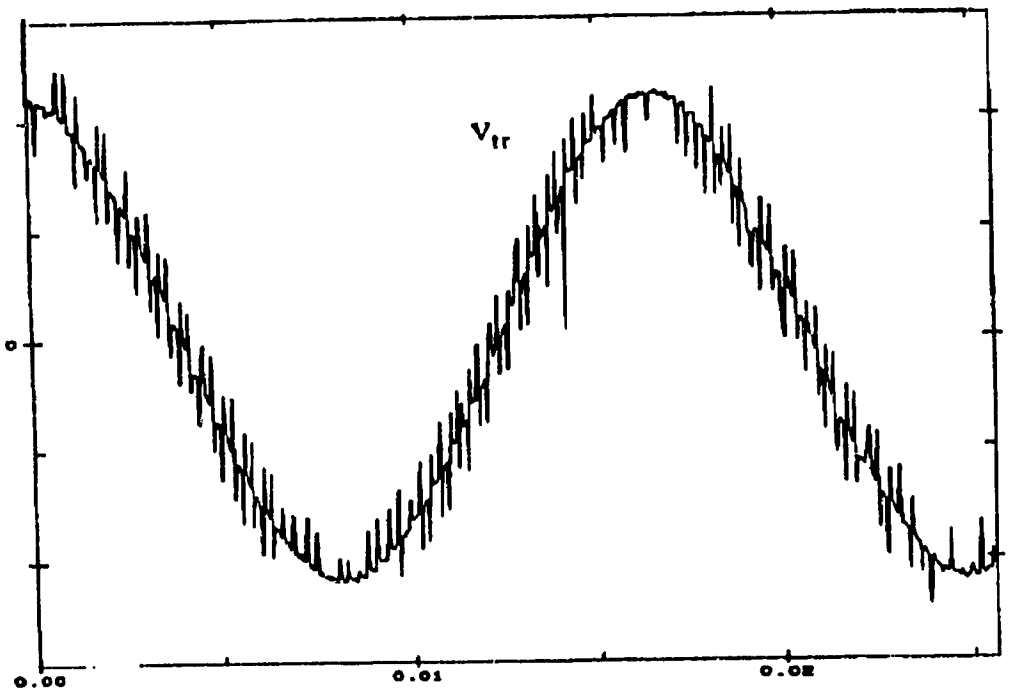

Fig. 4.18 - Load line-to-line voltage - VL_{ca} Vertical scale : 125 V/div - Horizontal scale : seconds

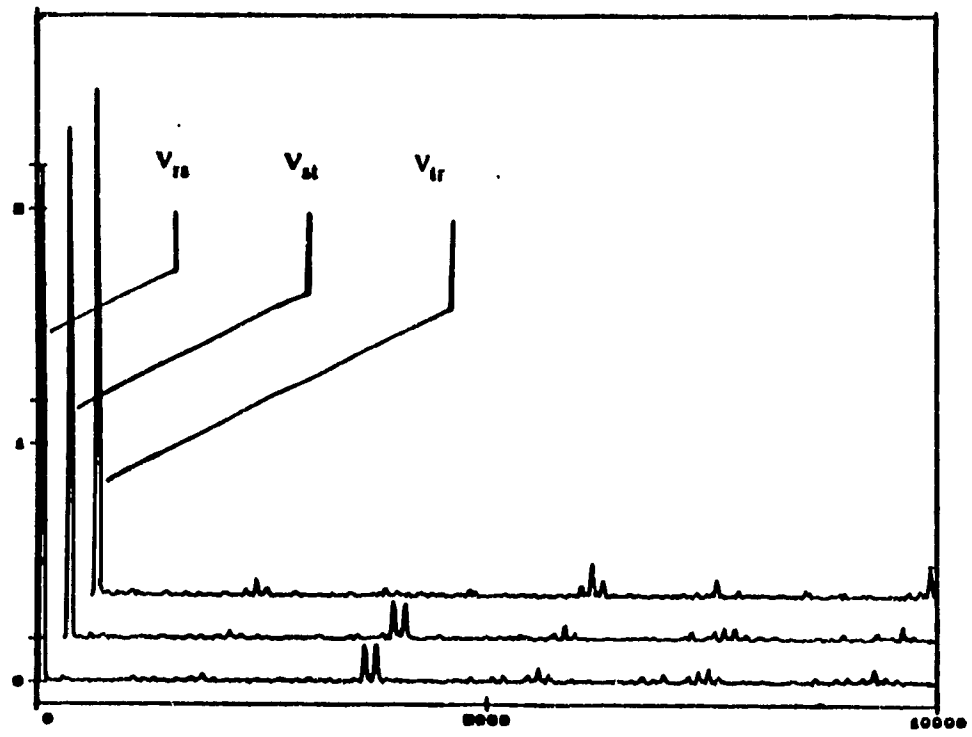

Fig. 4.19 - Spectra of the load line-to-line voltages. Vertical scale : 125 V/div - Horizontal scale : hertz

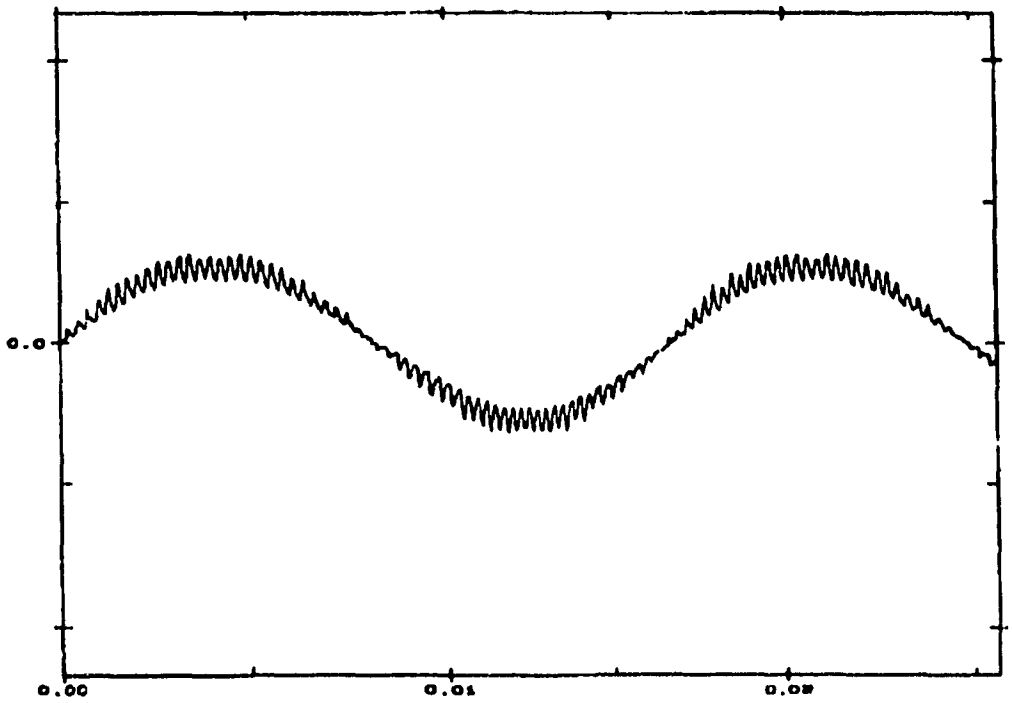

Fig. 4.20 - Line current - I_b.
Vertical scale : 10 A/div - Horizontal scale : seconds

4.8 Conclusions

A series voltage compensator for three-phase unbalanced sources with a low kVA rating as compared to shunt compensators, has been presented and analyzed in this chapter. The system, based on a three-phase voltage source inverter with unbalanced gating patterns and connected in series with the supply through a three-phase delta-wye transformer, proved to be feasible and performed as expected. A 1.3 kVA prototype was built and tested with an 11% unbalance and 9% magnitude error. The results showed a very good correlation with the expected performance, producing a balanced line-to-line load voltage with a low harmonic distortion, even without a filter. The compensator required an active power of only 0.11 pu, which confirms one of the main advantages of the compensation scheme proposed.

CHAPTER 5

DYNAMIC ANALYSIS AND DESIGN OF COMPENSATORS FOR UNBALANCED AC VOLTAGES

5.1. Introduction

Today a wide range of apparatus, based on power electronics, is commercially available or in development, among them, shunt static VAR compensators, and high speed phase-shifters. Power system unbalance control is one of the areas in which this technology was only recently introduced, as shown in the previous chapters [40,41].

There are two types of unbalances in a power system: voltage unbalance (source unbalance) and current unbalance (load unbalance), depending upon its origin. The usual solution for load unbalance is to balance its impedance with a passive reactive-only network, or to balance the line currents with shunt-connected var compensators working under unbalance conditions[21]. In the case of voltage unbalance, the use of a series-connected voltage source inverter allows the regulation and the balancing of the voltage on the load side with a low rating power compensator [40,41]. In the cases of series and shunt compensators, the operation of the converter under unbalanced switching functions requires a control approach that takes in account this non ideal operating condition. Such an approach has not yet been fully developed.

This chapter describes a method for the dynamic analysis of unbalanced networks and

the design of controllers working under such conditions.

The first step consists in partitioning the system under analysis into its symmetrical sequence equivalents. The result is a set of balanced networks corresponding to the zero, the positive and the negative sequence components, which are then analyzed using a dq transformation.

In order to implement this technique, it is necessary to define a time-domain (instantaneous) symmetrical sequence transformation , which is based in the concept of space-vectors, which have been used for some time in modeling and control of the ac machines.

The proposed method is applied in the analysis of the dynamic response of a series-connected voltage unbalance compensator, and in the design of its control loops.

5.2. Description of the Technique

5.2.1. Symmetrical Components Transformation

The symmetrical sequence components transformation is a linear, power invariant transformation originally defined for steady-state analysis of three-phase unbalanced systems, and largely used in power systems fault analysis and protection. The transformation states that any unbalanced three-phase system can be decomposed into two components, named *positive and negative sequence components*, and into a neutral point offset, named *zero sequence component*. The transformation is defined by the matrices,

$$A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \qquad A^{-1} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \tag{5.1}$$

Where $\alpha = e^{j120}$

The positive and the negative sequence components define two linearly independent balanced three-phase systems, which can be analyzed separately using the superposition theorem.

Given a vector formed by the phasors of three-phase voltages, the symmetrical components transformation gives the values of the zero sequence component (V_0), the positive sequence component (V_1) and the negative sequence component(V_2) for the system's line *a*.

$$V_{012} = A \cdot V_{abc} \tag{5.2}$$

Because this transformation is based on the phasors of the voltages, which is a steady-state representation of the amplitude and the phase of the instantaneous voltage functions, it is limited to steady-state applications.

5.2.2. Instantaneous Symmetrical Components

The limitation of steady-state application for the above technique, the use of voltage phasors in the transformation, can be eliminated by using the concept of space-vectors, a widely used tool in field-oriented control of ac machines, which was developed in mid-

seventies [34,35]. A space-vector $\underline{w}(t)$ with an amplitude W, which can be a scalar function of the time (a step as example), and with a variable angular position $\beta(t)$, is defined as,

$$\underline{w}(t) = W \cdot e^{j(\beta(t))} = W \cdot (\cos(\beta(t)) + j\sin(\beta(t)) \tag{5.3}$$

This can be used to represent a sinusoidal voltage source as follows.

$$v(t) = V \cdot \cos(\beta(t)) = Re(\underline{v}(\beta(t))) \tag{5.4}$$

Taking a set of three-phase unbalanced voltage sources the correspondent set of space-vectors is,

$$\underline{v}(t)_{abc} = \begin{bmatrix} V_a \cdot e^{j(\omega t + \phi_a)} \\ V_b \cdot e^{j(\omega t + \phi_b - 120)} \\ V_c \cdot e^{j(\omega t + \phi_c + 120)} \end{bmatrix} = e^{j\omega t} \cdot \begin{bmatrix} V_a \cdot e^{j(\phi_a)} \\ V_b \cdot e^{j(\phi_b - 120)} \\ V_c \cdot e^{j(\phi_c + 120)} \end{bmatrix} \tag{5.5}$$

Multiplying (5.5) by the symmetrical components transformation matrix we obtain the space-vectors of the symmetrical sequence components as shown in the equation (5.6).

$$\underline{v}(t)_{012} = \frac{e^{j\omega t}}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \cdot \begin{bmatrix} V_a \cdot e^{j(\phi_a)} \\ V_b \cdot e^{j(\phi_b - 120)} \\ V_c \cdot e^{j(\phi_c + 120)} \end{bmatrix} \tag{5.6}$$

Thus, the instantaneous values of the symmetrical components of the voltages are obtained by extracting the real part of these space-vectors.

$$v(t)_{012} = Re\left(\frac{e^{j\omega t}}{3}\cdot\begin{bmatrix} V_a\, e^{j(\phi_a)} + V_b\, e^{j(\phi_b-120)} + V_c\, e^{j(\phi_c+120)} \\ V_a\, e^{j(\phi_a)} + V_b\, e^{j(\phi_b)} + V_c\, e^{j(\phi_c)} \\ V_a\, e^{j(\phi_a)} + V_b\, e^{j(\phi_b+120)} + V_c\, e^{j(\phi_c-120)} \end{bmatrix}\right) \qquad (5.7)$$

Eqn. (5.7) gives the time-domain (instantaneous) symmetrical components of the voltages provided. It shows that the concept of symmetrical components, given originally only for steady-state analysis, can be used for dynamic analysis once the time dependency is maintained during the transformation.

The behavior of the transformation during transients is exemplified in Fig. 5.1. A set of initially balanced line-to-neutral voltages are provided. At the instant t_1 a step is applied in the line A, increasing its voltage by 50%. And at the instant t_2 a phase failure is experienced.

The concept of instantaneous symmetrical components transformation can be used in combination with the superposition theorem to perform dynamical analysis of unbalanced networks. The system is separated in its instantaneous model for zero, positive and negative sequence components, and then analyzed separated using any known technique such as the following dq transformation.

5.2.3. dq0 Model for Instantaneous Symmetrical Sequence Components

Once the unbalanced system is separated in two balanced ones, it's possible to apply dq transformation. This will allow the analysis and the design of any application using dc dynamical models. A typical example is the design of an unbalance compensator.

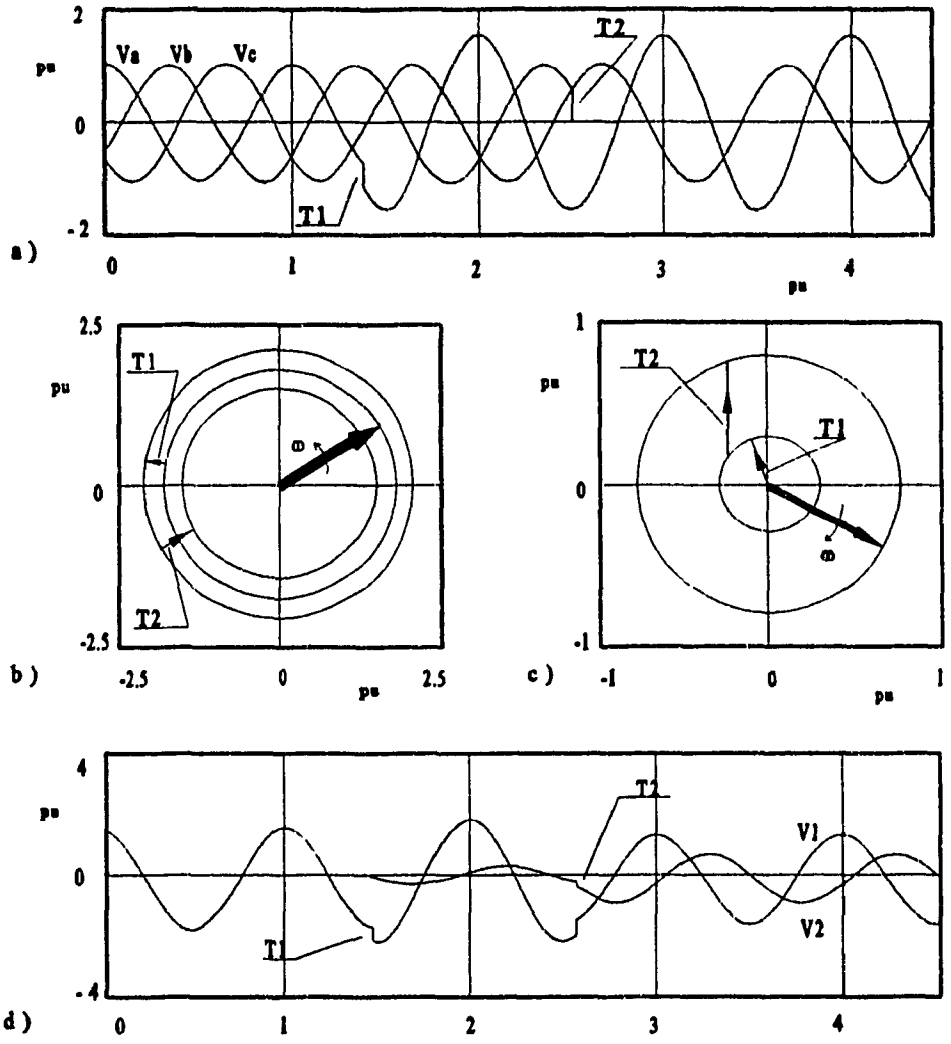

Fig. 5.1 - a) Instantaneous voltages ; b) Positive sequence trajectory
c) Negative sequence trajectory ; d) Instantaneous positive and negative sequence

5.2.3.1 Positive Sequence Component

The dq transformation of a set of balanced three-phase voltages is defined by its

transformation matrix **P**, as follows.

$$P = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \sin(\theta) & \sin(\theta-120) & \sin(\theta+120) \\ \cos(\theta) & \cos(\theta-120) & \cos(\theta+120) \end{bmatrix} \tag{5.8}$$

Rewriting this transformation matrix using the space-vector concept,

$$P = \frac{(\underline{P} + \underline{P}^*)}{2} \tag{5.9}$$

where $\underline{P}$ is,

$$\underline{P} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ e^{j\theta} & e^{j(\theta-120)} & e^{j(\theta+120)} \\ e^{j(\theta-90)} & e^{j(\theta-210)} & e^{j(\theta+30)} \end{bmatrix} \tag{5.10}$$

The 0dq components for the positive sequence instantaneous voltages are obtained by applying this transformation in a set of voltages as in (5.5).

$$v_1(t)_{odq} = P \cdot Re(\underline{v}_1(t)_{abc}) = P \cdot \frac{\underline{v}_1(t)_{abc} + \underline{v}_1^*(t)_{abc}}{2} \tag{5.11}$$

where the space vectors are given as follows.

$$\underline{v}_1^*(t)_{abc} = \begin{bmatrix} 1 \\ \alpha \\ \alpha^2 \end{bmatrix} \cdot \underline{v}_1^*(t) = T_2 \cdot \underline{v}_1^*(t) \tag{5.12}$$

$$\underline{v}_1(t)_{abc} = T_1 \cdot \underline{v}_1(t) = \begin{bmatrix} 1 \\ \alpha^2 \\ \alpha \end{bmatrix} \cdot \underline{v}_1(t) \tag{5.13}$$

Substituting (5.9), (5.12) and (5.13) in (5.11) results,

$$v_1(t)_{0dq} = \frac{1}{2} \cdot \sqrt{\frac{3}{2}} \left(\begin{bmatrix} 0 \\ e^{-j\theta} \\ e^{-j(\theta-90)} \end{bmatrix} \cdot \underline{v}_1(t) + \begin{bmatrix} 0 \\ e^{j\theta} \\ e^{j(\theta-90)} \end{bmatrix} \cdot \underline{v}_1^*(t) \right) \tag{5.14}$$

Using the definition of positive sequence space-vector given by,

$$\underline{v}_1(t) = V_1 \cdot e^{j\omega t} \cdot e^{j\phi_1} \tag{5.15}$$

we obtain the final equation for the 0dq components of the positive sequence component as,

$$v_1(t)_{0dq} = \sqrt{\frac{3}{2}} \cdot V_1 \cdot \begin{bmatrix} 0 \\ \cos(\omega t + \phi_1 - \theta) \\ \sin(\omega t + \phi_1 - \theta) \end{bmatrix} \tag{5.16}$$

Where V_1 and ϕ_1 are the magnitude and the phase of the positive sequence component space-vector, and θ is the position of the d-q frame for the positive sequence component.

5.2.3.2 Negative Sequence Component

The dq transformation of the negative sequence component can be obtained by using the same procedure, and results in,

$$v_2(t)_{0dq} = \sqrt{\frac{3}{2}} \cdot V_2 \cdot \begin{bmatrix} 0 \\ \cos(\omega t+\phi_2+\theta) \\ \sin(\omega t+\phi_2+\theta) \end{bmatrix} \tag{5.17}$$

5.2.4. Positioning the d-q Frames

The final step in the dq transformation is to establish the observer's position, the reference axis, which defines the angle θ in the (5.16) and (5.17). In a single sequence dq model θ is used to eliminate the time dependency by choosing the reference axis to be rotation with a constant speed, equal to the source angular speed ω, and with an angular displacement δ. This can still be used for multiple sequence dq models, but due to the intrinsic opposite rotation directions of the positive and the negative sequences, two references have to be established, defined by,

$$\theta_1 = \omega t + \delta \qquad\qquad \theta_2 = -\omega t - \delta \tag{5.18}$$

Substituting these values in (5.16) and (5.17) results,

$$v_1(t)_{0dq} = \sqrt{\frac{3}{2}} \cdot V_1 \cdot \begin{bmatrix} 0 \\ \cos(\phi_1-\delta) \\ \sin(\phi_1-\delta) \end{bmatrix} \tag{5.19}$$

$$v_2(t)_{0dq} = \sqrt{\frac{3}{2}} \cdot V_2 \cdot \begin{bmatrix} 0 \\ \cos(\phi_2-\delta) \\ \sin(\phi_2-\delta) \end{bmatrix} \tag{5.20}$$

The technique presented above reduces an unbalanced three-phase system (ac) into a dynamical model containing four dc (in steady-state) circuits, which are suitable to control design, as shown in the next section.

5.3. Series-Connected Unbalance Compensator

5.3.1. System Description

The technique above presented can be used with any unbalanced ac network, but it is particularly helpful in the dynamic analysis and design of static converters working under unbalanced conditions. This is the case of the systems presented in the chapters 3 and 4, where static converters, connected in series to the ac line, were used to eliminate the negative sequence component, and to regulate the positive sequence component of the line [40,41]. Fig. 5.2 shows a diagram of such a compensator, as presented in the chapter 4.

The goal of the compensator is to maintain the load voltage constant and balanced. The compensator is formed by the following blocks: the inverter, the symmetrical sequence components calculators, the controller, the dc source, the inverter output filter, and the series transformer. The symmetrical components calculators are responsible for extracting the positive and the negative sequence components of the load and source line-to-line voltages and feed them to the controller. Based on this information and on the reference required, the controller should provide the necessary reference voltages for the modulator (carrier-type) in order to generate the compensating voltages at the output of the inverter. The complete steady-state analysis is presented in the chapter 4.

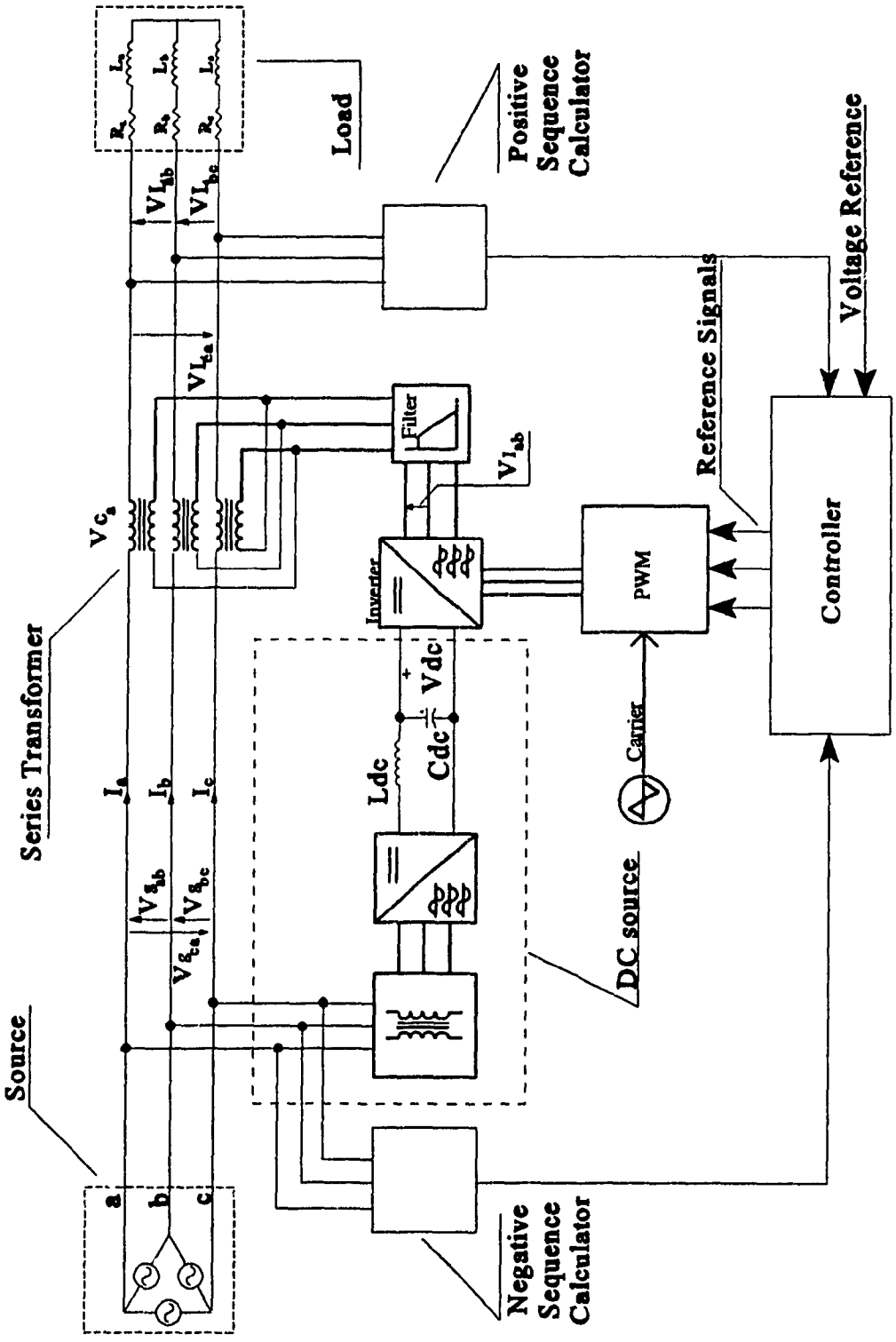

Fig. 5.2- Diagram of the proposed series unbalance compensator.

5.3.2. Modeling in d-q Frame

The following assumptions were used for simplification purposes in the coming analysis:

- the break frequency of the inverter output filter is placed far from the required bandwidth of the compensator, thus the filter can be eliminated from the control analysis;

- the switching frequency used in the modulator is much larger than the break frequency of the inverter output filter (at least twice), which allows modeling of the inverter by a gain;

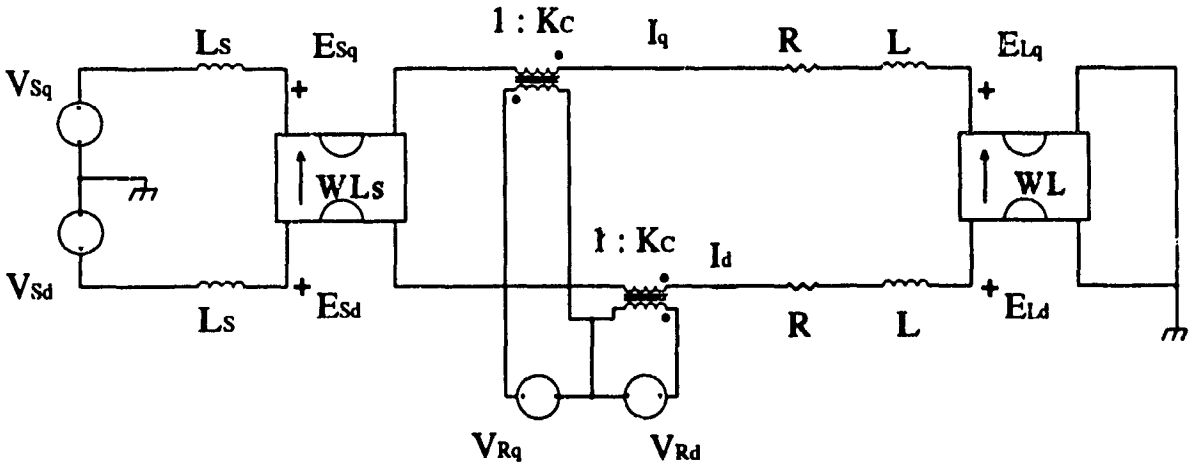

Fig. 5.3 - Model for one of the sequences of the compensator in the d-q frame.

- the analysis is made on a line-to-line basis, thus the zero sequence can be eliminated from the models.

Using these assumptions, and the technique for graphical dq transformation described in [36-39], the compensator can be reduced to a d-q frame model as shown in Fig. 5.3.

The d and the q sequence components of the source voltage (V_{sd} and V_{sq}) and the

compensator voltage (V_{Rd} and V_{Rq}) are given by the (5.19) and (5.20). The elements E_{Sd}, E_{Sq}, E_{Ld}, and E_{Lq} are defined by the gyrators created by L and L_S in the dq transformation as shown in [36].

Defining the position of the dq frame is the main tool for reducing the size of the model and the controller. The source voltage is not directly available for this purpose. If the dq frame is placed in phase with the compensator voltage (V_{Rd} and V_{Rq}), it became necessary the use of four control loops in order to regulate the load voltage and to eliminate the unbalance, the d and the q axis of each symmetrical sequence component. A much better solution is achieved if the dq frame is aligned with the load voltage by synchronization, allowing the elimination of one of the dq components.

Aligning the d-axis with the load voltage, its q-axis components are eliminated, for both symmetrical sequence components, which turns the q-axis component of the compensator voltage unnecessary. The current gyrators are eliminated by calculating the equivalent impedance in their d-axis terminals. The circuit is reduced to the one in Fig. 5.4.

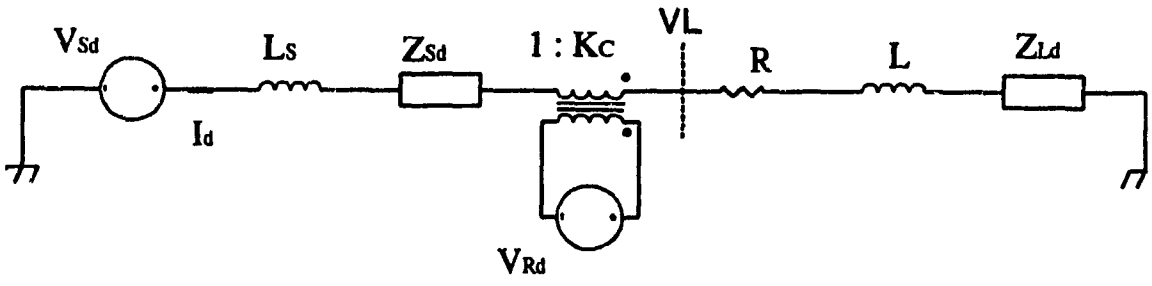

Fig. 5.4 - Resultant model after the dq frame synchronization with the load voltage.

From the circuit presented in Fig. 5.4 it is possible to obtain the transfer functions for

the load voltage as shown in blocks in Fig. 5.5.

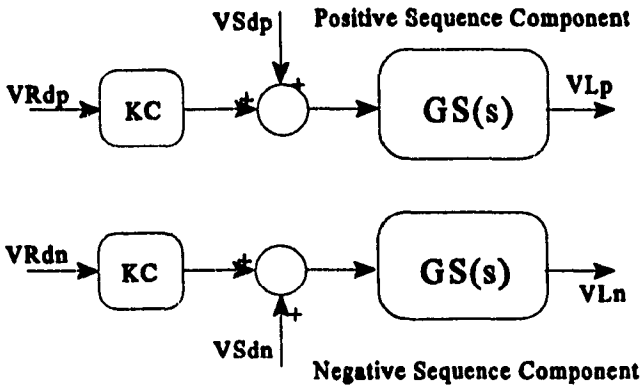

Fig. 5.5 - Block diagram of the compensator for both symmetrical components.

The blocks of Fig. 5.5 are defined as,

$$K_C = G_i \cdot V_{DC} \cdot \frac{N_2}{N_1} \tag{5.21}$$

Where K_C is the gain of the inverter reflected to the secondary side of the transformer, G_i is the gain of the PWM technique being used, V_{DC} is the dc-bus voltage and N_2/N_1 is the turns-ratio of the series transformer.

$$G_S(s) = \gamma \cdot \frac{s^2 + s \cdot 2\omega_L + \omega_L^2 + \omega_B^2}{s^2 + s \cdot (1+\gamma)\omega_L + \omega_L \omega_T + \omega_B^2} \tag{5.22}$$

Where

$$\omega_L = \frac{R}{L}$$

$$\omega_T = \frac{R}{(L + L_S)} \qquad (5.23)$$

$$\gamma = \frac{L}{(L + L_S)}$$

Using as example the compensator given in Chap. 4, whose data are:

$R = 22.3\ \Omega$ $\qquad$ $X_L = 16.8\ \Omega$

$X_S = 4.2\ \Omega$ $\qquad$ $V_{DC} = 258.3\ V$

$G_t = 0.613\ pu$ $\qquad$ $\frac{N_2}{N_1} = 0.25$

Substituting these values in (5.21), (5.22) and (5.23), the system transfer function results in a $K_C = 39.6$ V and:

$$G_S(s) = 0.8 \cdot \frac{s^2 + s \cdot 1006 + 395131}{s^2 + s \cdot 402.4 + 344328} \qquad (5.25)$$

With the system model established, it is possible to apply any of the classic dynamic analysis and design tools, such as root-locus, bode, nyquist, to obtain its performance and to design a controller for the compensator.

5.4 Control Loop Design

The analysis presented in the previous sections reduces the unbalance compensator

to a set of two independent networks, defined in terms of the negative and the positive sequence components of the system. This allows the design of the control subsystem with two independent dc loops, one to eliminate the negative sequence and the other to regulate the load voltage (positive sequence).

The elimination of the negative sequence component of the load voltage, as shown in the previous sections, requires the knowledge of the position of the negative sequence space-vector. A procedure to extract the symmetrical sequence components from an unbalanced set of voltages is presented in [53].

Because the goal of the negative sequence control loop is to eliminate the negative sequence component from the load voltage, a feedback loop for this purpose would require monitoring the position of the negative sequence space-vector in the source side, and the magnitude of the same variable in the load side of the compensator. In order to reduce the complexity of the control subsystem, it is suggested the use of a feedforward loop. This approach does provide a very fast dynamic response, however it has the disadvantage of not allowing the reduction of the static error to zero.

The proposed loop for the negative sequence is shown in Fig. 5.6, where this quantity is extracted and reinjected into the line with reversed polarity. The negative sequence component of the load voltage is then reduced to a value close to zero (for ideal conditions it is zero).

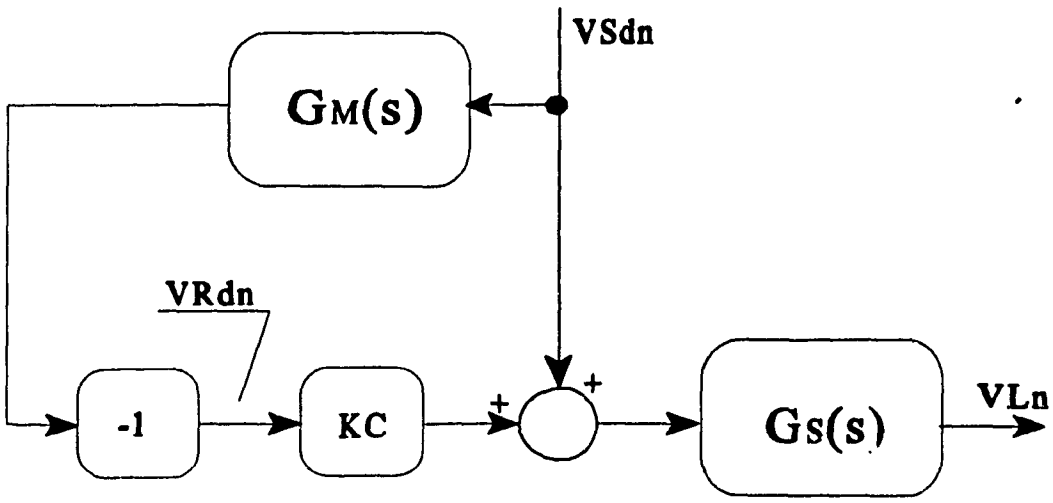

Fig. 5.6 - Block diagram of the negative sequence elimination feedforward loop.

The block defined by G_M models the sensor unit, which is a symmetrical sequence components calculator implemented as presented in Chap. 6 [53]. The transfer function for this unit is modeled by:

$$G_M(s) = K_M \cdot \frac{1}{1 + s\tau_M} \tag{5.26}$$

where K_M is the total gain of the measurement process and τ_M is its time constant. For the calculator described in [53], and for the compensator in Chap.4, these values are:

$$G_M(s) = 0.00437 \cdot \frac{1}{1 + s \cdot 0.011} \tag{5.27}$$

The regulation of the load voltage can be achieved by a feedback loop. In order to do so it is required the measurement of its positive sequence component, which can be done by

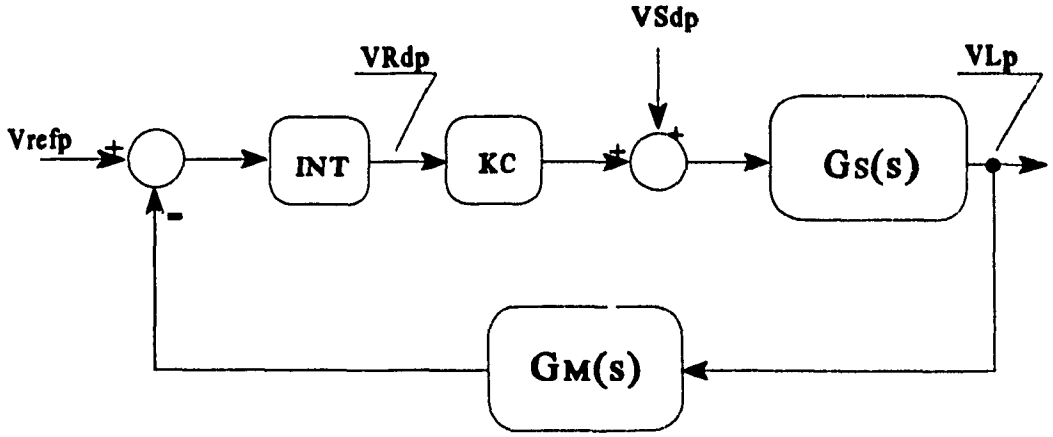

Fig. 5.7 - Block diagram of the load voltage regulator feedback loop.

the measurement approach described in [53].

The proposed feedback loop for load voltage regulation is shown in Fig. 5.7.

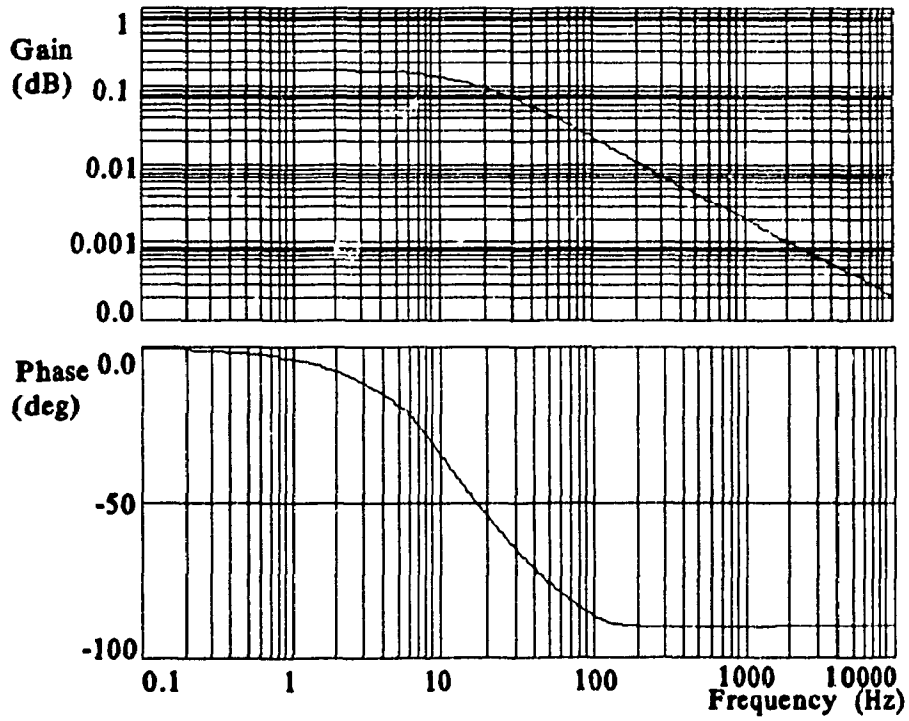

Fig. 5.8 - Open loop Bode diagrams (gain and phase) for the proposed control system.

The frequency response for the open loop transfer function of this system is shown in Fig. 5.8.

The design parameter to be used is the required bandwidth for the compensator. This value is specified by the slower element in the overall loop, which in the present case is the measurement unit with a bandwidth of 30 Hz.

An integrator is designed to reduce the static error to zero, and to match the above mentioned constraint. Its transfer function is:

$$G_I(s) = \frac{1}{s \cdot 0.004} \tag{5.28}$$

The inclusion of this regulator in the system permits the determination of the final closed loop frequency response, as shown in Fig. 5.9.

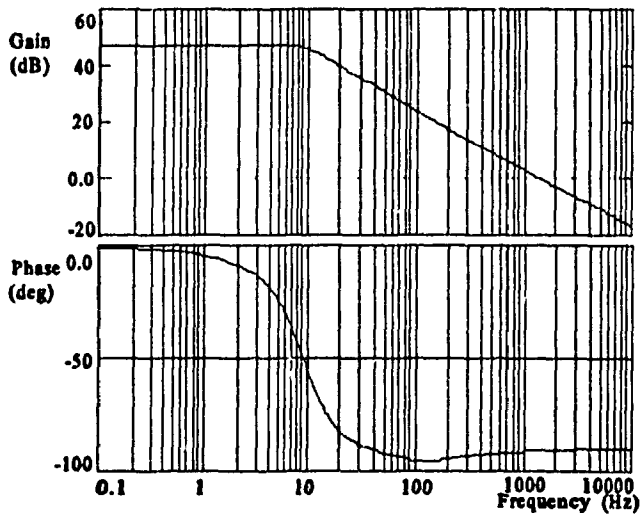

Fig. 5.9 - Closed loop Bode diagrams (gain and phase) for the proposed control system.

5.5. Simulation Results

The proposed system was tested by simulation in order to validate the design procedure and to confirm its feasibility. It has shown to perform according to the expected, i.e., the system regulates the load voltage and compensates the voltage unbalance. Particularly, it shows that:

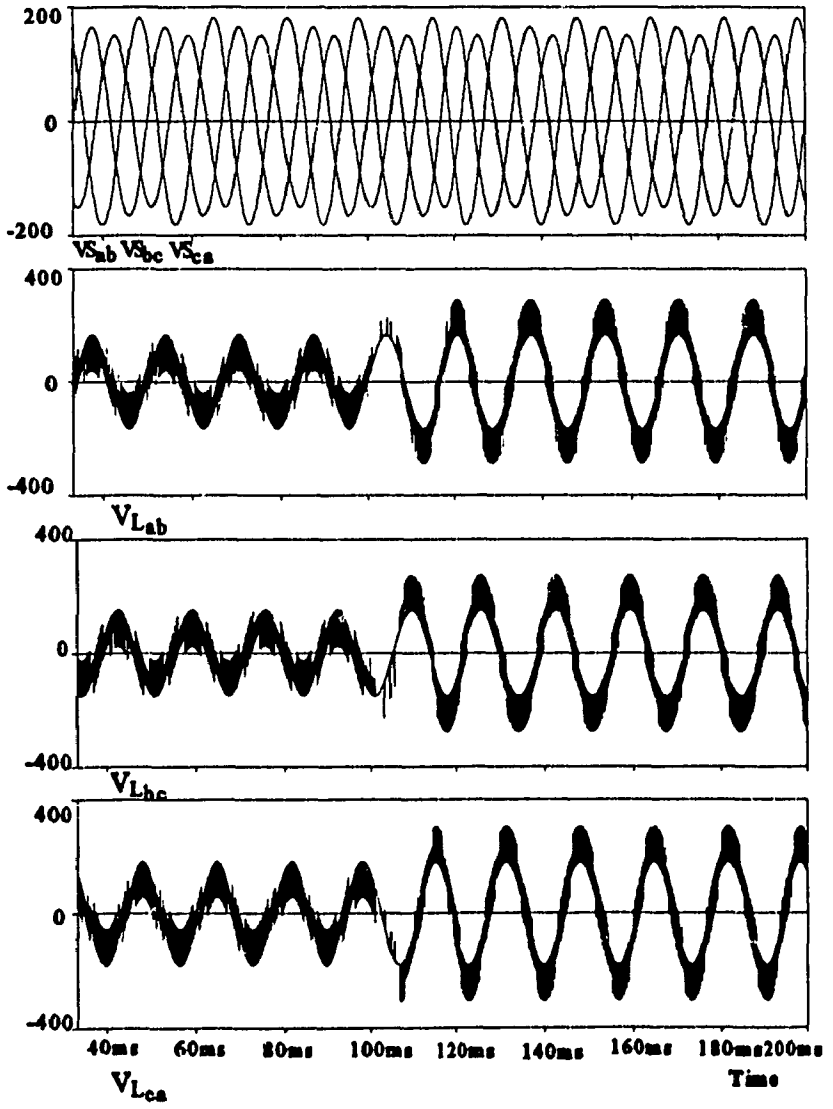

Fig. 5.10 - Simulation results. Source voltages, and load voltages.

(a) The unbalance is reduced from 21% to 1.5%. Total elimination is not achieved due to the use of a feedforward loop, as shown in Figs. 5.11.a and 5.11.b.

(b) The system exhibits a good speed response. For a step change in the positive sequence reference voltage from 0.5 to 1pu, the measured settling time (2%) is of 13.5ms.

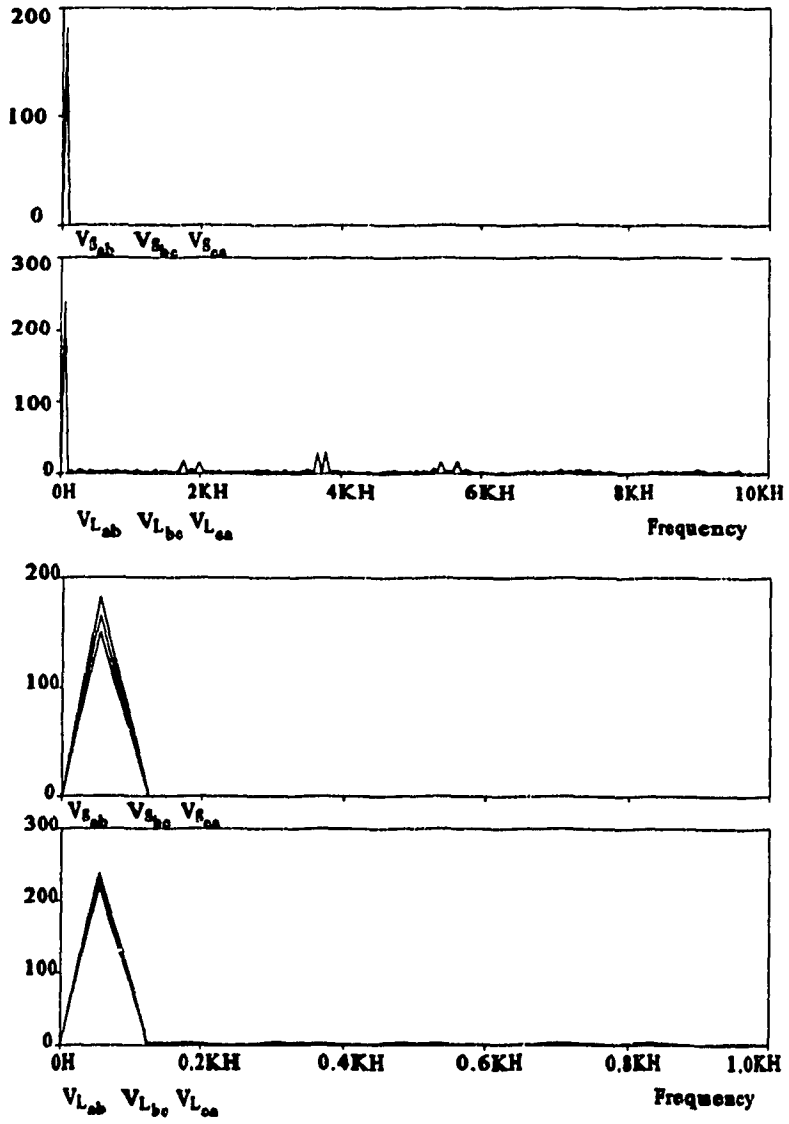

Fig. 5.11 - Simulation results. Spectra of the source voltages, and of the load voltages..

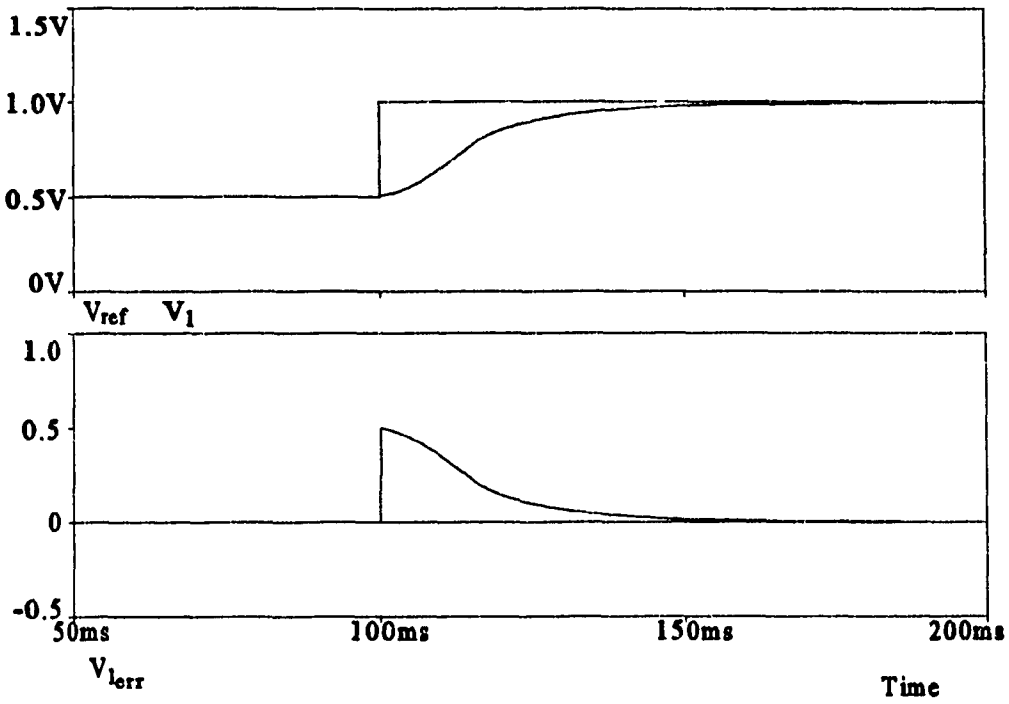

Fig. 5.12 - Simulation results under a reference transient. a) Reference step and positive sequence response, and b) error in the positive sequence.

5.6. Conclusions

A method to analyze the dynamics of the proposed voltage unbalance compensator, and to design its control loops was presented. The method has proven to be a very useful tool for modeling passive networks with or without static power converters connected to them. It was shown that the use of the dq components with unbalanced systems requires the measurement of the instantaneous values of the symmetrical sequence components, and can

be achieved by using the instantaneous symmetrical sequence transformation, which is also described in this chapter. The technique was applied to the compensator presented in Chap. 4, and simulation results demonstrate its feasibility.

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1. Summary

High performance static converters used for series compensation in industrial power systems have been investigated in this thesis. The following topologies and application aspects have been studied:

(a) An ac voltage regulator for single phase loads consisting of a low power series connected auxiliary voltage source. It is implemented using a single-phase voltage source inverter connected in series with the ac supply through a transformer. The control of the inverter is done using a sine pulse-width modulation (SPWM) pattern. The power rating of the compensator is obtained for two possible situations: (a) injecting reactive power only, and (b) injecting real and reactive power. The study includes a description of two modes of operation, as a voltage regulator, and as a voltage regulator with power factor improvement. The system was analyzed under steady-state conditions and for an open loop operation by simulation, and tested on a 1.2 kVA experimental prototype, in order to prove its feasibility.

(b) A series connected voltage compensator for unbalanced three phase sources is proposed. It consists of three single-phase voltage source inverters, connected to the power system through three single-phase transformers. The unbalanced voltages are resolved in their symmetrical sequence components for balancing and regulation purposes. The measured negative sequence of the source voltages is reinjected in the line with an opposite phase, while the positive sequence component is used for regulation of the load voltage. A SPWM

technique is used to control the inverters. The proposed system was tested by simulation and by means of a laboratory prototype of 2.2 kVA rating.

(c) An alternative topology for unbalance compensators is proposed employing only one three-phase voltage source inverter, instead of the three single-phase VSI option used in the previous case. The inverter is controlled with a SPWM pattern with unbalanced switching functions, which allows the elimination of the unbalance and also the control the magnitude of the positive sequence component of the load voltage. The procedure for calculating the required reference signals to generate these unbalanced switching functions is presented. The system was tested for an open loop operation under steady-state conditions by simulation and by means of a 1.3 kVA prototype to verify its feasibility.

In addition to these topics, the following related aspects were investigated:

(a) A method for the dynamic analysis of unbalanced networks and for the design and control of unbalance voltage compensators working under such conditions is proposed. It consists of the partitioning of the system under analysis to its symmetrical sequence equivalents. The result is a set of two independent balanced networks corresponding to the positive and the negative sequence components. In order to implement this technique, a time-domain (instantaneous) symmetrical sequence transformation is defined, which is based on the concept of space-vectors. A dq transformation is used to reduce the two symmetrical component networks to a set of dc equivalent circuits (in steady-state). The method is applied to the analysis of the dynamic response and to the design of control loops for the voltage unbalance compensator based on the three-phase voltage source inverter.

(b) A digital calculator capable of extracting the positive and the negative sequence components of the line-to-line voltages of ac systems in real-time is developed. The calculator hardware implementation consists of a Digital Signal Processor (TMS320C25) connected to a 16 bits A/D, both using one PC as a development station. The software used for the calculation procedure implements a reduced radix-2 DIF FFT algorithm to extract the fundamental time-varying phasors related to the line-to-line voltages (space-vectors). These values are used to calculate the symmetrical sequence components. Some special implementation techniques are introduced to improve the calculator dynamic response.

6.2 Conclusions

Experimental implementation of the proposed compensators on laboratory prototypes of the 2 kVA range has proven the feasibility of the proposed compensators and their control schemes. In addition, these prototypes have validated the proposed tools for the analysis of the instantaneous unbalances and the method of resolving the symmetrical components defining the voltage unbalance. The following conclusions were reached regarding the proposed solutions to power supply quality problems related to voltage regulation and voltage unbalance:

(a) Voltage regulation for single-phase loads can be achieved through series compensation. For the case using only reactive power injection, a voltage source inverter connected to a self-controlled dc bus is sufficient. However, when real power is also supplied, the rated power of the compensator can be reduced, compared to the system using only

reactive power. For example, to correct for a 20% voltage error using only reactive power, the rated power of the compensator is 0.66 pu. However, using the combined real and reactive power approach results in a reduction to 0.2 pu of the required power rating. In this case, despite the fact that a rectifier is required to supply the real power, its power rating for the worst case is 0.2 pu. The reduction in the power rating also results in a reduction of the voltage distortion injected into the supply system. When the maximum compensation voltage is not used in the regulation procedure, and the system is supplying a reactive load, the remaining voltage can be used to improve the input power factor.

(b) Two topologies of voltage unbalance compensators are proposed, the first based on three single-phase voltage source inverters, and the other on a three-phase voltage source inverter. They are both equally effective in balancing and regulating the load voltage. The single-phase topology imposes less constraints on the control scheme and PWM pattern generation. However, this topology does require larger passive filter components to meet the required distortion limits. Also, the overall power rating of the compensator is larger for the single phase topology mostly due to the difference in the voltage gain of the inverters.

6.3 Suggestions for Future Work

As an extension to this study of series compensation of industrial supply systems, the following topic are suggested:

(a) An investigation of the effects of this type of series compensation on the magnitude and control of short circuit currents.

(b) The investigation of current source inverter topologies rather than the voltage source inverter topology used in this work.

(c) The investigation of the use of this type of series compensation on the control of inrush currents of large transformer units.

(d) The use of the proposed compensator topologies as active power filters to suppress harmonics generated by nonlinear loads.

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APPENDIX A

A DSP-BASED REAL-TIME DIGITAL CALCULATOR FOR SYMMETRICAL COMPONENTS

A.1 Introduction

Until recently, the symmetrical sequence component transformatio: was a technique used basically in the analysis of unbalanced polyphase ac circuits, and in some cases of system protection. With the improvement in the speed of mechanical switches and with the arrival of fast high-power semiconductor switches, fast measurement of the symmetrical sequence components of voltages and currents in power systems is becoming a necessity. Several new applications, such as high-speed relays, unbalance compensators, generator protection against faults, require the symmetrical sequences as a basis for defining operating conditions. Also the fast measurement of symmetrical sequence components of voltages and/or currents can be used in the monitoring of power systems status for analysis, operation, protection, compensation, etc.

This chapter investigates a DSP implementation of a real-time calculator for symmetrical components.

A.2 Background Information

The detection of symmetrical sequence components has in the past been done basically

by means of passive and active analog filters. These have a fundamental problem: they do not perform well under the presence of dc and/or harmonics. Also analog filters characteristics may drift with temperature and aging, requiring sophisticated compensation circuits and a continuous calibration. Digital filters however do not exhibit these problems, and are becoming increasingly powerful, fast and inexpensive. This topic has become an active area in the last decade, and several papers have appeared [42-50].

Dash *et al.* have presented a protection scheme for asymmetrical faults in generators based on the detection of the negative sequence component at the machine terminals [42].

A power systems protection scheme using a digital algorithm to obtain the symmetrical sequence components was presented by Phadke *et al.* [43]. It uses a DFT algorithm to extract the symmetrical sequence components from the line voltages of the system. In a more recent paper Phadke *et al.* [45] expanded this approach by dealing with many practical problems such as sampling frequency, processing time of some mathematical operations, etc. They also suggest the use of this technique for measuring frequency variation.

A computationally viable method for symmetrical sequence components measurement was presented by Degens [44]. It consisted in solving the equation that defines the symmetrical components transformation on an instantaneous basis. The drawback of such approach is that it requires a delay of 240° (11.1 ms @ 60 Hz) for two of the voltages to obtain the instantaneous values of the symmetrical components and an extra delay of 240° to calculate their correspondent phasors. These intrinsic delays are responsible for a total transient response time of 33 ms @ 60 Hz.

In this chapter, a filter capable of extracting the positive and the negative sequence components of the line-to-line voltages of ac systems in real-time is described. The hardware implementation consists of a fast Digital Signal Processor connected to a 16 bit A/D, both using one PC as a development station. The software responsible for the filtering procedure implements a reduced radix-2 DIF FFT algorithm to extract the fundamental time-varying phasors related to the line-to-line voltages. These values are used to calculate the symmetrical sequence components and leaving enough processing free time to allow the implementation of almost any control procedure. The algorithm used allied with some implementation techniques give the system a faster transient response than the above mentioned techniques. The transient response time is only one cycle. The standard FFT algorithm is simplified in order to reduce the processing time, requiring only one complex multiplication per sample.

A.3 System Description

A.3.1 Hardware

Fig. A.1 shows the block diagram of the hardware used to implement the proposed filter. The line-to-line voltages are isolated and scaled to fit in the A/D input range with a transformer and an attenuation amplifier. A high speed 16 bits A/D, capable of sampling at 200 kHz, provides a complement-of-two digital equivalent for the line-to-line voltages. These values are passed through interruption to the DSP board. The processor responsible for the calculation of the symmetrical sequence components is a high performance Texas Instruments

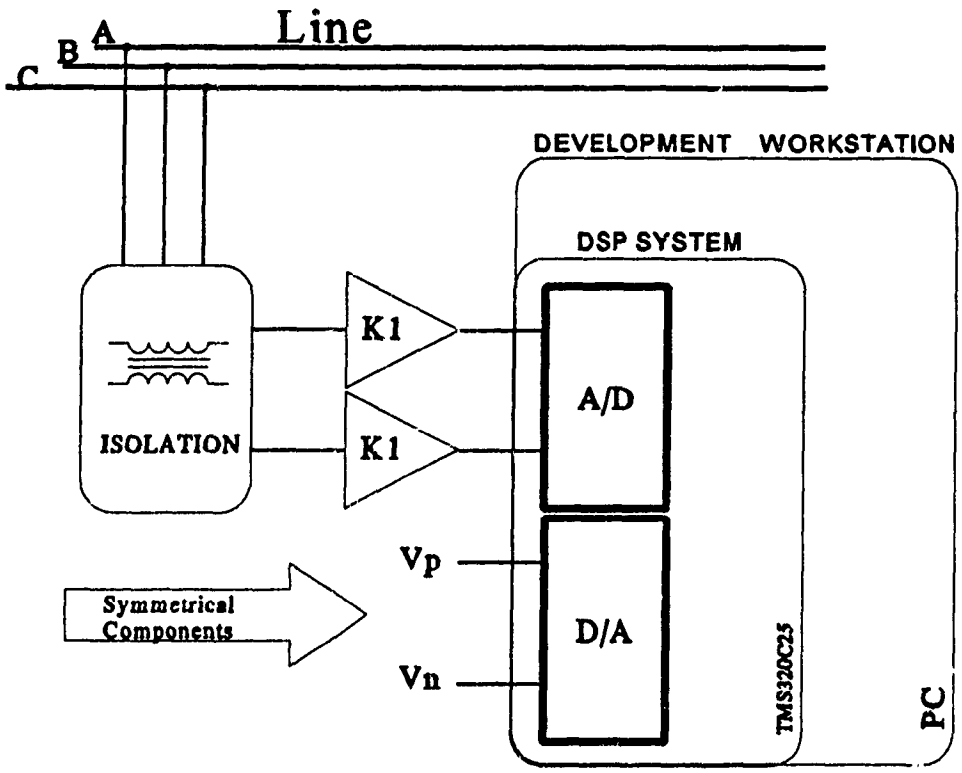

Fig. A.1 - Block diagram of the hardware of the proposed system.

TMS320C25 integer DSP, running at 40 MHz. The results of the processing stage are sent out through a 16 bits D/A. Depending on the application, this result can be the instantaneous values of the positive and negative symmetrical sequence components, the magnitude of these components, or the resultant signal of an internal control block. All these systems were connected to a PC compatible that was used as a development workstation for the DSP.

A.3.2 Software

The program used to implement the proposed filter consists in three blocks: the FFT, the rotation and the transformation block, as shown in Fig. A.2. The data sampled through

the A/D is processed by a radix-2 decimation-in-frequency reduced FFT algorithm to ob in the phasor correspondent to the fundamental component of the input voltage. Despite the fact phasor has appeared as a steady-state definition, it also works for transients, as shown in the appendix A. Here its amplitude and phase are not constant but varying with time, unless the voltages are in steady-state.

Because no hardware synchronization is used, a rotation stage is required to establish a reference in time. This is done by rotating one of the voltage phasors to the origin, eliminating its imaginary part. The other is rotated by the same angle, maintaining the same relative position to the reference. This eliminates any requirement of zero-crossing detection at the controller level. Depending on the application it may be necessary, but only externally to the digital subsystem. These values are then used as inputs to a symmetrical sequence component's transformation, providing the required positive and negative sequence as outputs.

These procedures can be processed in a short time by the DSP, leaving enough time

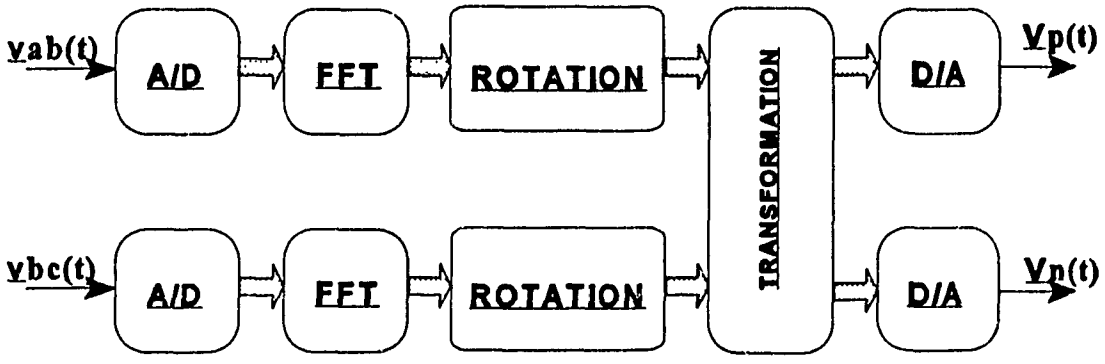

Fig. A.2 - Block diagram of the proposed system - Software.

for any extra application. Up to this point this technique does not refer to a specific application, and can be used to control and compensate the unbalance in the power system, to regulate the positive sequence voltage in the generator, or to start a fault protection system, as examples.

A.4 Mathematical Analysis

The mathematical approach to implement the proposed filter consists in three main blocks: the phasor extraction, the software synchronization, and the symmetrical components' transformation itself.

A.4.1 Extraction of the Time-Dependent Phasors

There are many possible techniques to extract the phasors of the line-to-line voltages [47-50]. Taking in account the simplicity of the algorithm and the available tools for implementation, it was chosen a Discrete Fourier Transform (DFT) [52], and among the various algorithms available we have chosen a radix-2 decimation-in-frequency reduced FFT [51], due to its simplicity and possibility to gain speed by reducing its calculation requirements further more. This algorithm is defined as:

$$X_1 = \frac{2}{N} \cdot \sum_{n=0}^{n=\frac{N}{2}-1} \left(\left[x(n) - x(n+\frac{N}{2}) \right] \cdot W_N^n \right) \qquad \text{(A.1)}$$

where $W_N^n = e^{j\frac{2\pi}{N} \cdot n}$ is the twiddle factor, N is the number of samples per period,

$\mathbf{x(n)}$ is the value of the input function at the n-th sample, and $\mathbf{X_1}$ is the fundamental value of the input function.

The choice of sampling frequency is a critical point for the overall speed of the filter. Some authors suggest the use of a sampling rate multiple of 3 times the line frequency [44] to eliminate the effect of some harmonics of the fundamental, and to simplify the calculation. With today's powerful and specialized DSP's it become much more suitable a sampling frequency multiple of two allowing the use of an FFT algorithm as the one in (A.1), which can simplify the indexing of variables when programming.

Fig. A.3 shows a graphical representation of the algorithm in (42) with a sampling frequency of 1.92 kHz (32 sampling per period @ 60 Hz).

This figure shows that the actual implementation of this algorithm can be further improved by storing all the intermediate results thus, when a new sample is done ($\mathbf{x_4}$ in Fig. A.3), only one complex multiplication is necessary. This gives a reasonable reduction in the processing time, allowing a new output result per sample.

Applying this algorithm to a set of two line-to-line voltages gives as result,

$$\begin{bmatrix} \underline{v}_{ab}(t) \\ \underline{v}_{bc}(t) \end{bmatrix} = \frac{2}{N} \cdot \sum_{n=0}^{n=\frac{N}{2}-1} \left(\begin{bmatrix} v_{ab}(n,t) \\ v_{bc}(n,t) \end{bmatrix} - \begin{bmatrix} v_{ab}(n+\frac{N}{2},t) \\ v_{bc}(n+\frac{N}{2},t) \end{bmatrix} \right) \cdot W_N^n \qquad \text{(A.2)}$$

Where the underlined terms $\underline{\mathbf{v}}_{ab}$ and $\underline{\mathbf{v}}_{bc}$ are time-dependent vectors on the complex plane, representing the time-dependent amplitudes and phases of the line-to-line voltages.

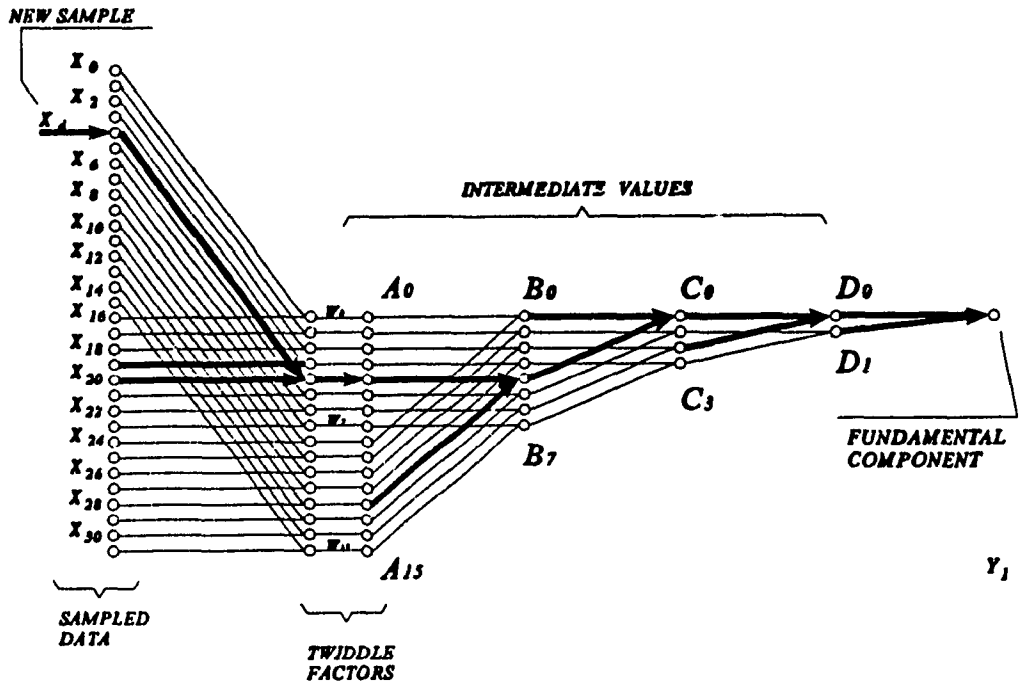

Fig. A.3 - Radix-2 DIF reduced FFT.

A.4.2 Software Synchronization

In order to avoid any hardware synchronization between the set of voltages being measured and the processor, a software substitute is implemented.

The free-running characteristic of the phasor extraction gives as result a pair of rotating vectors in the complex plane. At any instant, the phase of these two vectors to the internal (DSP) frame is due to the lack of synchronization and to differences between the internal clock frequency (crystal-based) and the line frequency, which usually vary slightly around the rated value. The synchronization procedure consists in a rotation of the external frame (the two phasors) to superimpose it on the internal frame. For the phasor chosen as

reference, it is required the calculation of its magnitude. The second phasor requires a rotation by an angle equal to the phase of the reference ϕ_{ab}.

A.4.3 Symmetrical Components Transformation

If there is no interest in the line-to-neutral symmetrical components or there is no neutral path in the system, the zero sequence does not affect the analysis or is not present. This assumption allows a considerable simplification to the standard symmetrical transformation definition, reducing it to two independent variables' matrix equation, defined by:

$$\begin{bmatrix} \underline{v}_1(t) \\ \underline{v}_2(t) \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & -\alpha^2 & \alpha - \alpha^2 \\ 1 - \alpha & \alpha^2 - \alpha \end{bmatrix} \cdot \begin{bmatrix} \underline{v}_{ab}(t) \\ \underline{v}_{bc}(t) \end{bmatrix} = B \cdot \begin{bmatrix} \underline{v}_{ab}(t) \\ \underline{v}_{bc}(t) \end{bmatrix} \qquad \text{(A.3)}$$

where $\alpha = e^{j120}$

The variables $\underline{v}_{ab}(t)$ and $\underline{v}_{bc}(t)$ are the time-dependent phasors correspondent to the input line-to-line voltages given by (43), and $\underline{v}_1$, and $\underline{v}_2$ are the time-dependent positive and negative sequence components of these voltages, which are dc quantities when in steady-state.

A.5 Frequency Response

Detecting symmetrical sequence components in an actual power system requires a careful analysis of its response for numerous non ideal conditions, such as the presence of noise and harmonics in the signal being measured. Ideally the filter should be capable of rejecting any frequency component different from the fundamental. Fig. A.4 shows the frequency response of the proposed algorithm. It shows that the harmonics of the fundamental are eliminated, as required.

Despite the fact the harmonic should be eliminated, the filter has to be insensitive to small frequency oscillations around the fundamental. This guarantees that frequency variations normally present in the ac mains, will not affect the filter operation. Fig. A.5 shows the error in the measurement expected for a maximum variation of ± 5% of the rated value.

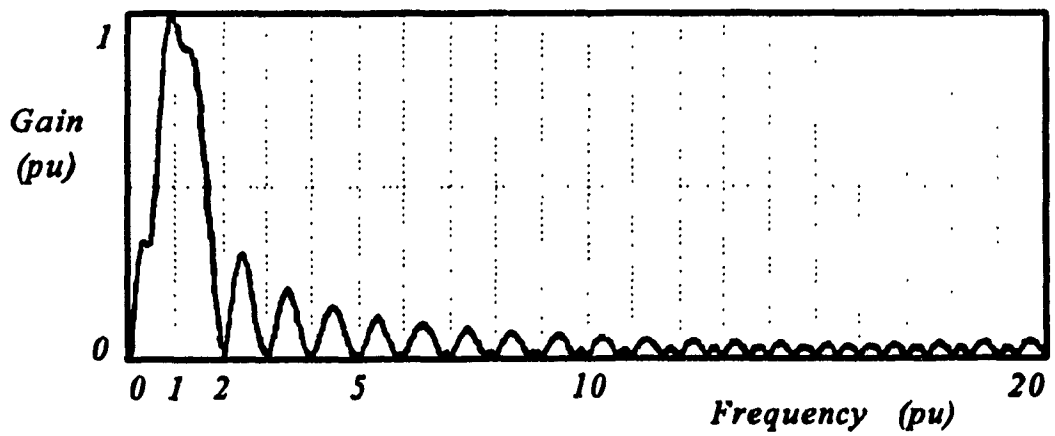

Fig. A.4 - Frequency response of the proposed algorithm.

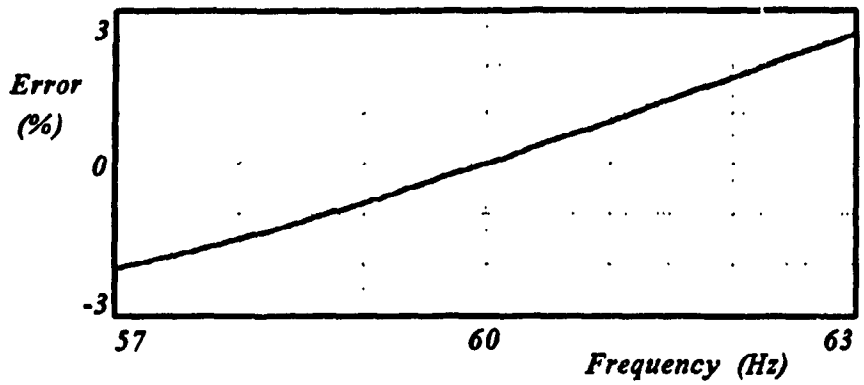

Fig. A.5 - Error due to the frequency variation (±5%).

A.6 Experimental Results

In order to confirm the feasibility of the proposed filter the A/D inputs were redirected to the PC I/O ports, which allowed the test of the actual filter under a variety of conditions. To illustrated the performance of the proposed filter, Figs. A.6, A.7 and A.8 present its response for various common situations.

Fig. A.6 shows the transient response of the filter for three states. The section **A** shows a balanced system with a positive sequence component of 1 pu. The section **B** shows the system with a positive sequence component reduced to 0.8 pu and a negative sequence component of 0.16 pu (unbalance factor of 20 %). It is interesting to note the time necessary to reach steady-state, which is one cycle (32 samples @ 60 Hz), given a *time constant* of approximately 11 ms, which reasonably smaller than the methods presented in the references [42-50]. The section **C** maintains the same positive sequence component of **B** and reduces

the unbalance factor to 10% (negative sequence component is 0.08 pu).

Fig. A.7 presents the response of the filter to two very common occurrences in the ac mains, the presence of third order harmonics, and dc offset, which are both major problems for analog filters. The filter shows a very good performance under these conditions. The steady-state result with and without these condition is practically the same.

Another very common occurrence in the ac mains is the frequency variation. In most power systems it is acceptable frequency variations of ±5%. Fig. A.8 shows the operation of the filter with the frequency varying from 57 Hz (-5%) to 63 Hz (+5%), with 0.8 pu of positive sequence and 0.16 pu of negative sequence components. It demonstrates no effect on the positive sequence component, and a slight increase in the ripple of the negative

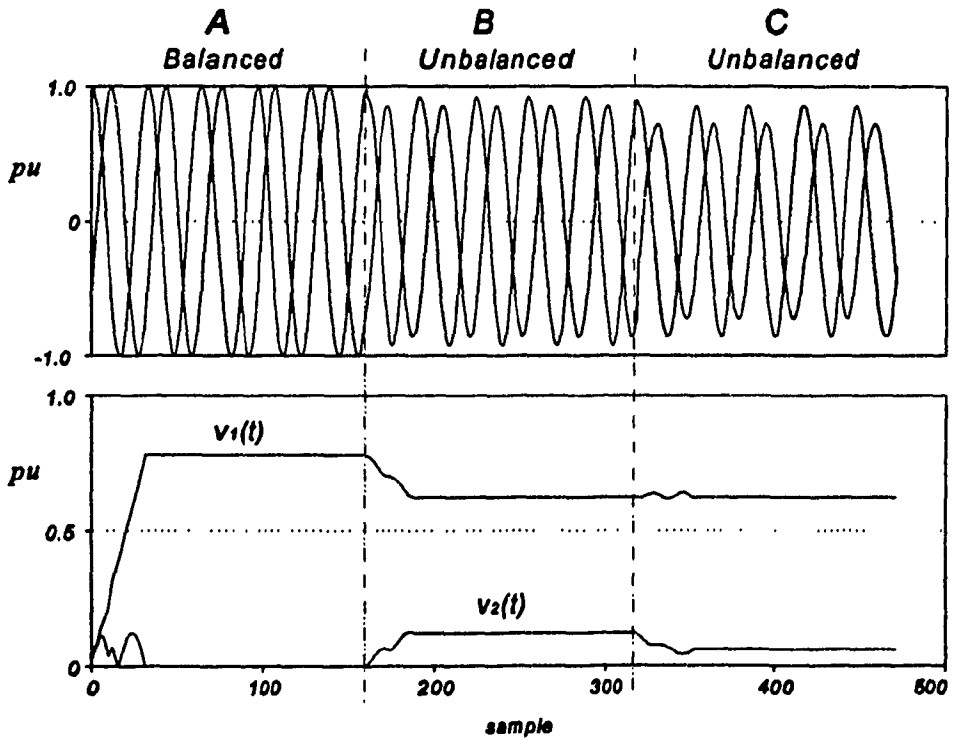

Fig. A.6 - Transient response. A) Balanced; B) 20% unbalanced ; C) 10% unbalanced

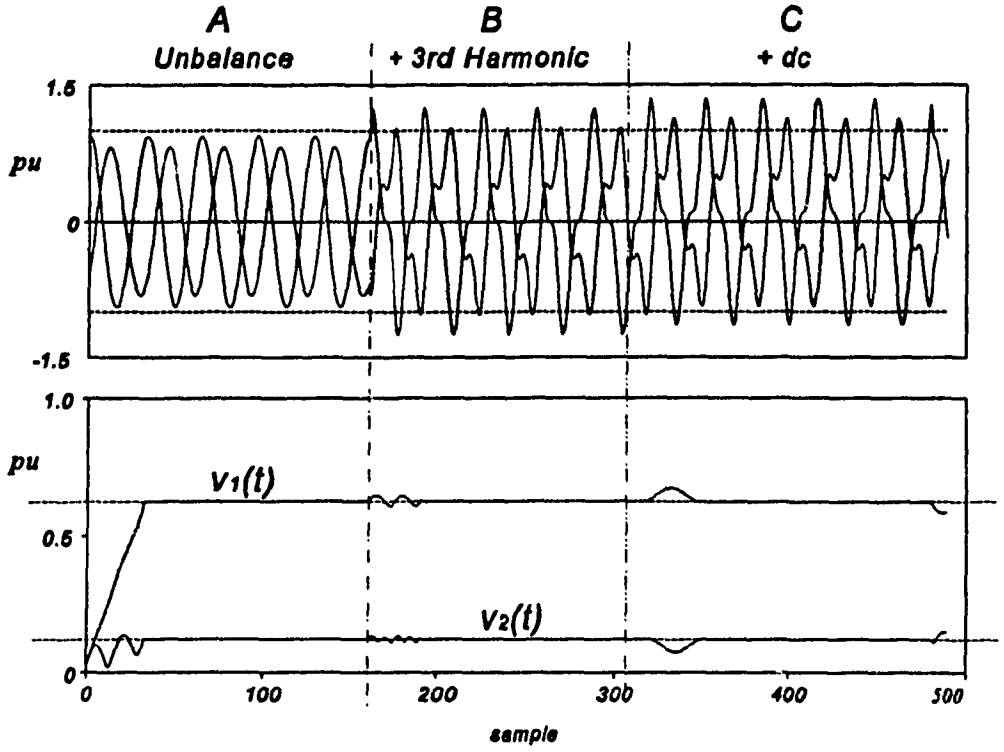

Fig. A.7 - Effect of the third harmonic and of dc offset.

sequence component when it is off the rated value (60 Hz).

A.7 Conclusions

A DSP-based digital filter was presented and analyzed in this chapter. It proved to perform as expected, extracting the symmetrical sequence components of the line-to-line voltages in real-time. A time constant of approximately 11 ms was achieved, and it is defined only by the phasor extraction algorithm. The speed of the processor does not affect the time constant, thus once improved algorithms become a requirement, they can yet be implemented

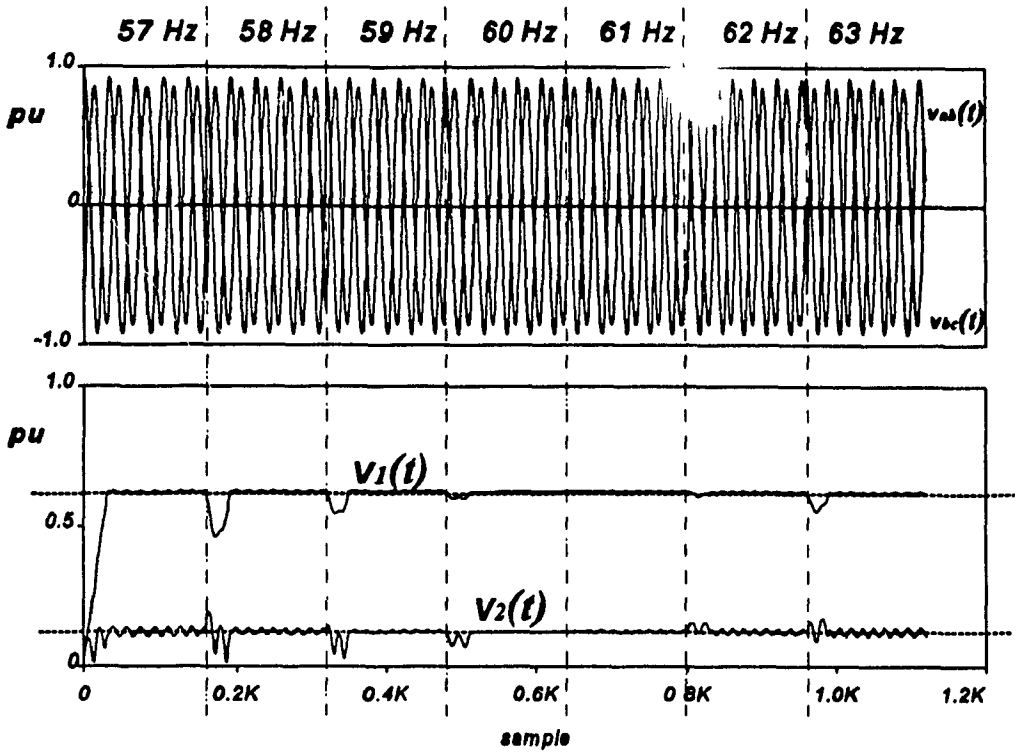

Fig. A.8 - Effect of ±5% frequency variation.

on the same hardware and with the same symmetrical components' calculation algorithm. The processing time for each functional block is reasonably short: the FFT algorithm requires only 255 instruction cycles (26 us with the TMS320C25-40); to process the result of the FFT requires most of the time, 1119 instruction cycles (112 us); and to perform the i/o functions it is necessary 34 instruction cycles (3.4 us). All the processing requires a total of 141 us, which is only 27 % of the sampling period, leaving the rest of the time (73%) to be dedicated to control procedure or to increase the sampling frequency (if required). Also since only two line-to-line voltages are required, the cost of the sampling hardware is reduced.

It is also shown that the filter performs well even under non ideal conditions such as third-harmonic, dc offset, and frequency variations. There are almost no variations of the expected result.

APPENDIX B

COMPUTATIONAL ASPECTS

Various standard or specific software packages are exploited in this thesis. No simulator was designed and no programming in advanced languages such as C or BASIC was required, except for the designing of specific models used in the design and simulation of the proposed compensators.

Most of the mathematical design procedures, such as the design of the circuits, was done using MATHCAD versions 2.5 for DOS, versions 3.1 and 4.0 for WINDOWS, and version 3.1 for UNIX. The cases of analysis and design that required a more specialized study, such as the dynamic modeling presented in Chapter 5, the choice was the use of MATLAB, versions 3.5 for DOS, and 4.0 for WINDOWS and UNIX. With respect to simulation procedures, two software programs were used: (a) the MicroSim PSPICE versions 4.0 to 5.3 for DOS, WINDOWS and version 5.3 for SUNOS, and (b) the PSIM (power electronic circuit simulation) program version 1.0 for DOS and for SUNOS.

The simulation was done by means of a switching function approach on PSPICE. Here the converters are modeled as ideal multiplication blocks. The input variable (dc bus voltage) is multiplied by the switching function of the inverter in order to obtain the output function (line-to-line voltages). The same procedure is used in the output line current. All the remainder of the system (transformers, load, filters, etc) is considered ideal. In all the chapters

but the last (Chapter 5), this was the methodology used for simulation. In Chapter 5 all the blocks of the power and control circuits were modeled specifically for the compensator in study. For example, the digital filter used to extract the symmetrical sequence components from the line-to-line voltages is implemented in detail.