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HIGH PERFORMANCE MEDIUM POWER UNINTERRUPTIBLE POWER SUPPLY

Mike Boost

A Thesis

in

The Department

of

Electrical & Computer

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ABSTRACT

The concept of an ideal uninterruptible power supply (UPS) has evolved within the last ten years. In the past, solid state UPS carried performance specifications slightly better than those for an equivalent motor generator set. Todays medium power UPS is expected to power a wider variety of critical loads rendering it virtually as sophisticated as the equipment it powers. Traditional UPS balanced, linear loads such as motors and transformers are being displaced by unbalanced and nonlinear loads such as computers. Furthermore, UPS are now expected to operate within the human working environment in densely populated areas where the minimization of space and weight is increasingly important Unfortunately the widening UPS operating environment and load spectrum often handicaps the current generation of UPS In view of this, this thesis is directed towards the theoretical design and experimental verification of a UPS power train more compatible to modern loads and environments with streamlined space and weight requirements

In order to achieve the high performance UPS a new topology is proposed that includes a fully controlled rectification stage, high frequency link isolation stage and a low output impedance inverter stage

Advanced pulse width modulation (PWM) techniques are critically evaluated allowing application of the most suitable technique for both the controlled rectification stage and the inverter stage The results yield filter components of reduced size and weight.

The proposed high frequency link stage is used to provide isolation and

regulate the inverter input voltage. Evaluation of several feasible topologies yields a suitable power conversion stage that allows a dramatic reduction of transformer size and weight.

The low output impedance inverter stage contains a strategically selected output filter and a novel PWM technique to allow clean power delivery to most single and three phase nonlinear loads as well as unbalanced loads.

The thesis includes the evaluation of the switch and drive as well as the controller design for each of the three stages. The Evaluation of several suitable semiconductors yields a single common switching device and drive for the UPS. Further, three different controllers are used respectively for each stage. In particular a new, completely digital controller without a microprocessor is developed for the rectification stage allowing for increased ruggedness.

Two sophisticated software programs are developed to aid the analysis. A worst case ratings program to quickly solve converter ratings based on load and applied PWM technique and a simulation program to quickly analyze power electronic circuits which employ PWM are presented.

Finally in order to establish the feasibility of the new UPS topology, and to validate the analytical techniques predicted, key results are simulated and experimentally verified on a 10kVA laboratory prototype. Details of practical importance not typically found in the literature, such as lead inductance limitations, electromagnetic interference (EMI), snubbers, layout requirements, switching deadtimes/overlaps and transformer saturation are included.

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LIST OF ACRONYMS

THD	Total Harmonic Distortion
NEMA	National Electric Manufacturers Association
UPS	Uninterruptible Power Supply
PWM	Pulse Width Modulation
HF	High Frequency
CR	Controlled Rectifier
VSI	Voltage Sourced Inverter
CSI	Current Sourced Inverter
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse Width Modulation
MSPWM	Modified Sinusoidal Pulse Width Modulation
HIPWM	Harmonic Injection Pulse Width Modulation
PF/pf	Power Factor
MTBF	Mean Time Between Failures
EMI	Electromagnetic Interference
TIPF	Total Input Power Factor
EPROM	Erasable Programmable Read Only Memory
SMPS	Switch Mode Power Supply
IC	Integrated Circuit
ZTO	Zero turn off thyristor

LIST OF SYMBOLS

VRMS	Rectifier input rms voltage
VDC	Rectifier output dc voltage
α	Controlled rectifier phase delay firing angle
VDROP	Rectifier combined line and source impedance drop
VDCFLOAT	Battery Float Voltage
Bd	Battery discharge ratio
αMIN	Minimum phase delay firing angle
HAR_N	Amplitude of harmonic N
N	Harmonic order
$HARA_N$	Fourier series odd harmonic frequency term amplitude
$HARB_N$	Fourier series even harmonic frequency term amplitude
VIN	Input converter voltage
FBK	Filter Break Frequency
FBASE	Rectifier input voltage frequency
RK	Harmonic reduction factor
HAR_{FUND}	Fundamental harmonic amplitude
HAR_{DOM}	Dominant harmonic amplitude
FO	Filter order
ORDER	Dominant Harmonic Order
IIN_N	Converter input current amplitude of harmonic N
IODC	Rectifier output dc current
GAC	Converter ac gain
GDC	Converter dc gain
DF_1, DF_2, DF_3	Distortion factor quality index

GACMAX	Maximum converter ac gain
GDCMAX	Maximum converter dc gain
ICII	Inverter dc link capacitor rms current quality factor
ICR	CR rms input capacitor current quality factor
SW_F	Converter SHE switching frequency
M	Converter modulation index
CI1,CI2,LI,CI,LO,CO	Converter filter component values
XLI,XCI,XLO,XCO	Converter filter component impedance values
ILIRMS, ICIRMS	Converter filter component rms current rating
ILORMS, ICORMS	Converter filter component rms current rating
VLIRMS, VCIRMS	Converter filter component rms voltage rating
VLORMS, VCORMS	Converter filter component rms voltage rating
LIVA,CIVA,LOVA,COVA	Converter filter component power rating
ISWAVE	Converter average switch current rating
ISWRMS	Converter rms switch current rating
ISWPK, ISW1PK	Converter peak switch current rating
ISW2PK, ISW3PK	Converter peak switch current rating
ISW4PK	Converter peak switch current rating
VSWPK	Converter peak switch voltage
VDCBUSMAX	Inverter maximum dc bus voltage
VDCCBUSMIN	Inverter minimum dc bus voltage
VL-N	Inverter output line to neutral fundamental voltage
ZL-N	Inverter output line to neutral load
PTOTAL	Total inverter output apparent power
ISCALE, VSCALE,	Worst case inverter ratings program current voltage
ZSCALE	and impedance scaling factors
QL	Fundamental cut set matrix

$Q_{EC}, Q_{ER}, Q_{EL}, Q_{ES}, Q_{CC}$	Sub divisional cut set matrices
Q_{CR}, Q_{CL}, Q_{CJ}, Q_{RR}	Sub divisional cut set matrices
Q_{RL}, Q_{RJ}, Q_{LL}, Q_{LJ}	Sub divisional cut set matrices
C_t	Capacitor twig diagonal matrix
C_l	Capacitor link diagonal matrix
L_t	Inductor twig matrix
L_l	Inductor link matrix
G_t	Conductance twig diagonal matrix
G_l	Conductance link diagonal matrix
R_t	Resistive twig diagonal matrix
R_l	Resistive link diagonal matrix
V_{DCBUS}	Inverter input supply voltage
K_{MAX}	Total # of intersections below 90°
INTER(X)	Converter transition or voltage swing angle
ϕ_N	Phase shift of harmonic N
Z_L	Inverter load impedance
R_L	Inverter load impedance, resistive portion
X_{CL}	Inverter load impedance, capacitive portion
X_{LL}	Inverter load impedance, inductive portion
I_{DCBUS_RIP}	Inverter input inductor current ripple
V_{IN_RIP}	Inverter input capacitor voltage ripple
I_{DCBUS}	Inverter input supply current
$RX_{N,M}$	Normalized rectifier output voltage amplitude of harmonic N and modulation index M
$\mathcal{TF}$	Converter transfer function
$\mathcal{TF}_M$	Converter transfer function at modulation index M
$\mathcal{TF}_{MAX}$	Maximum converter transfer function

$\mathcal{TF}_{MIN}$	Minimum converter transfer function
V_{BATMIN}	Minimum battery voltage
V_{BATMAX}	Maximum battery voltage
X	State space analysis state vector
U	State space analysis supply vector
G_{SW1}, G_{SW2}, G_{SW3}	Inverter switch gating signals
G_{SW4}, G_{SW5}, G_{SW6}	Inverter switch gating signals
V_{AN}, V_{BN}, V_{CN}	Inverter leg center point to fictitious neutral voltage
V_{OUT}	Converter output voltage
V_{LOAD}	Converter load line to neutral voltage
I_{OUT}	Inverter output line current
I_{SW1}, I_{SW2}, I_{SW3}	Converter switch current
I_{SW4}, I_{SW5}, I_{SW6}	Converter switch current
I_{SW}	Converter switch current
$I_{OUT\_TD}(\omega\tau)$	Time domain representation of I_{OUT}
$I_{OUT\_TDP}(\omega\tau)$	Positive section of $I_{OUT\_TD}(\omega\tau)$ X $G_{SW1\_TD}(\omega\tau)$
$G_{SW1\_TD}(\omega\tau)$	Time domain representation of G_{SW1}
P_{OUT}	Converter output power
P_{IN}	Converter input power
I_{LOAD}	Inverter load current
V_{XN}, V_{YN}, V_{ZN}	Rectifier input source line - neutral voltage
I_{INA}	Rectifier input bridge current
F1, F2	PWM control signals for rectifier gating derivation
V_{BAT}	Battery voltage
V	Input rectifier peak source voltage
V_{MAX}	Input rectifier peak source voltage at high line
V_{MIN}	Input rectifier peak source voltage at low line

IDCMAX	Maximum rectifier output dc current level
ILO	Converter output inductor current
$ILO_{N,M}$	Rectifier output inductor current amplitude of harmonic N at modulation index M
ILOMAX	Maximum dc output current of rectifier
ILORIP	Rectifier output current ripple factor
$VLO_{N,M}$	Rectifier output inductor voltage amplitude of harmonic N at modulation index M
IA	Rectifier source line current
ICI	Rectifier input filter capacitor current (single phase)
VLI	Rectifier input filter inductor voltage
e	Displacement angle between VXN and IINI
IINA	Rectifier bridge input current
eIA_1	Displacement angle of IA_1
$eVXN_1$	Displacement angle of VXN_1
VINATHD	Rectifier input voltage THD
ICI, ICI1, ICI2	Converter input capacitor filter current
ICO	Converter output capacitor filter current
ILI	Converter input inductor filter current
VD1R, VD2R, VDR	Reverse diode voltages
Vo	HF link output load voltage
Io	HF link output load current
NN	Transformer turns ratio
D	Duty cycle
DMAX	Maximum duty cycle
DMIN	Minimum duty cycle
VINMIN	Minimum HF link input voltage

V_{INMAX}	Maximum HF link input voltage
V_{OMAX}	Maximum HF link output voltage
V_{OMIN}	Minimum HF link output voltage
I_{D1}, I_{D2}, I_D	HF link diode current
I_{D1AVE}, I_{D2AVE}	HF link diode ave current
A_P	Transformer area product
A_W	Transformer core window area
A_E	Transformer magnetic core cross section area
K_U, K_T, K_P, K_B	Transformer sizing factors
F_{SW}	HF link switching frequency
ΔB	Transformer core flux swing
A_P^*	Relative transformer area product
V_{LO}	Output inductor voltage
V_{CI}, V_{C1}, V_{C2}	Input capacitor voltage
I_T	Transformer current
F_{CK}	Clock frequency
L_{S1}, L_{S2}	Saturable reactors
I_1, I_2, I_3	Inverter output line currents
Z_1, Z_2, Z_3	Inverter output leg impedances including filter capacitor and load
V_{PWM}	Inverter output line to line PWM waveform
I_{U1}, I_{U2}, I_{U3}	Inverter mesh analysis loop currents
Z_a, Z_b, Z_c	Inverter unbalanced load impedances
Z_{FILTER}	Equivalent LC filter impedance
V_{LOADLL_N}	Inverter output line to line voltage amplitude of harmonic N
kVA	Kilo volt-amp

1.0 INTRODUCTION

1.1 General

Electric power utilities have strived to keep ac power at high availability. However, by virtue of its complex network structure (exceeding on occasion thousands of miles) power distribution equipment is prone to abnormalities and failure. Although numerous power line disturbance phenomena may occur, power blackouts are typically considered the prime problem. The mean time between failures (MTBF) of a high quality power utility is roughly 200 hours [6]. If uncompensated, outages may lead to a life threatening situation in medical facilities and air traffic control centers.

This problem gave rise to the concept of utilizing an intermediate or auxiliary energy stage between the ac mains and the critical load which could process and provide power during a utility failure. The uninterruptible power supply [UPS] is such an intermediate stage providing variable amounts of battery powered, auxiliary energy. Its use is now virtually standard practice in the traditional life threatening, critical power environments.

The history of the UPS reveals several distinct evolutionary phases leading to the present generation termed "4th generation UPS" characterized by PWM control. Recent developments include a thrust towards the production of a UPS, with more extensive applications beyond those of the traditional life threatening type. New installations in close proximity to manpower as well as in expanded industrial environments have led to the imposition of stricter UPS specifications which have handicapped the present "4th generation". Two of the main factors contributing to the increasing use of UPS systems were the introduction of modern sophisticated electronics equipment into virtually

every facet of engineering, and the optimization of manufacturing flow concepts. Each of these two factors are are discussed in more detail.

1) Modern office complexes and many manufacturing divisions now utilize high technology equipment in the form of telecommunications apparatus, robotics, data acquisition tools, main frames and personal computers. On a broader scale, many small business outfits are also stepping up their employment of similar technologically intensive yet less complex equipment [7]. The majority of equipment in this category contain microprocessors which have branched out from their computer roots into many diverse applications such as cash register control, telephone operation, security systems supervision, process control and instrumentation. Such equipment may provide the industrial leading edge and/or enhanced competitiveness at all levels, yet are often highly sensitive to mains disturbances. A power outage in the millisecond range can cause excessive costs and delays due to loss of services and/or data. Moreover, of equal importance, a substantial part of equipment damage or inexplicable shut downs are due to ac mains over voltages and high voltage spikes which typically occur at a rate of 5/month [6]. Reasonable hydro specifications guarantee a steady state window of +/-10% nominal voltage. However, a significant portion of modern technology based equipment (ie. computers) are only guaranteed to operate properly up to and including 6% above nominal line voltage [8]. Consequently the MTBF of the system is influenced to a greater extent by the ac mains quality rather than the MTBF of the actual equipment. As more institutions demand higher amounts of ac energy in many areas a negative quality factor is created. Some experts insist that in certain areas the

escalating demand for ac power has highly burdened hydro facilities leading to an actual diminishing of quality [9]. This leads to a higher risk of ac line abnormalities. In an effort to alleviate the quality problem many businesses are beginning to accept the need for a UPS system.

2) Secondly, an on going industrial trend towards reduced maintenance and increased quality has led to flow manufacturing concepts such as the *Can Ban Line* and *push* methods. These involve strict interaction between machines and operators in a production line format that are highly vulnerable to interruptions. Reinstating flow may involve resetting machinery, electronic robots or re-booting software control. This often results in costly setbacks. With the expanding awareness of these new manufacturing techniques many industries are becoming more heavily dependant on the quality of ac power supplied to them. A detailed study revealing the magnitude of operating losses attributed to ac failures dictates that on the average day an average sized Canadian industrial facility will lose $3000.00 due to a power outage of less than one minute [10]. An Inco representative recently reported at a conference that a power outage of 100ms forced the reprocessing of $250,000 worth of nickel [7]. It is clear that the effect of ac shutdown must today be considered more damaging and costly to businesses and industries than in previous years. Consequently to reduce expenses, an increasing demand for medium power UPS has been generated by manufacturing departments to reduce costly, unexpected shutdowns.

1.2 Evolving UPS Requirements

The widening spectrum of applications for medium power UPS has necessitated the establishment of a new set of power supply requirements both physically and electrically.

1.2.1 Physical UPS Requirements

Physical requirements stem from the office environment where floor space prices are at a premium and consequently raise concerns about supply power density. Most present medium power UPS have power densities in the range of .1->.4 w/in^3 [11],[12],[13],[14],[15],[16] without batteries. Combining this low power density with added space (approximately 25 inches for rear access leads to the typical floor space requirement of 21 ft^2 for a 10kVA UPS. This renders it expensive to utilize especially in down town locations where floor space rental is in the order of \$30.00/ft^2 to \$190.00/ft^2 per month.

Secondly, from the standpoint of floor loading, many office structures can handle approximately 70kg/ft^2. With a typical weight of.06->.1 kg/w (without batteries) a medium power UPS could weigh 1000kg [14],[16]. This is often too heavy for non concrete floors consequently the range of application may be limited by weight constraints.

Finally, many UPS utilize Pulse Width Modulation (PWM) techniques in order to improve the waveforms and benefit from the resulting components size, weight and cost reduction. For medium power semiconductors, the maximum switching frequency is relatively low creating in many instances unbearable audible noise in the range of 1 to 18 Khz. This often forces added consideration and expense for the utilization of such a converter in the office or working environment.

In summary, the three major physical challenges are weight reduction,

size reduction and audible noise reduction.

1.2.2 Electrical UPS Requirements

Traditionally UPS are designed to deliver power to linear and balanced loads which in the past were in the majority. However, modern high technology equipment is not necessarily balanced or linear. In fact, by the year 2000 it is estimated that over 50% of the utility's power grid will consist of computers or similar equipment [18]. UPS loads are expected to dramatically increase accordingly. These loads can create conditions where the typical UPS inverter stage can no longer guarantee clean power nor abide by the specifications for the output waveform. This may lead to load failure as well as a reduction of UPS MTBF and battery life.

Secondly, with expensive shutdown costs, system reliability requirements are escalating. Surveys have shown that large (32%) UPS downtime is attributed directly to failures initiated at the control components level primarily due to IC failure [17]. Consequently the need has arisen to alleviate this condition in order to improve reliability and general ruggedness of the supply.

Finally, most UPS are equipped to handle loads of limited power factor typically in the range of .8 lagging to unity [11]. Limiting the power factor range typically reduces the voltage transfer function window of the UPS inverter stage allowing for a more efficient design. This is no longer sufficient as many nonlinear loads exhibit capacitive characteristics in the leading range and many inductive linear loads have power factors less than .8. In summary, the main electrical challenges include the capability to deliver quality power to nonlinear and unbalanced loads, increased power factor range and improvement in supply ruggedness.

1.3 Scope of this Thesis

Todays modern UPS are static, employing semiconductors combined with battery backed power. Although various configurations are now available the UPS structure most commonly encountered is termed *"4th generation UPS"* [11],[16].

Being geared essentially for traditional applications the typical UPS cannot meet many of the new challenges in modern industrial and office complex applications without added expense and/or complexity. In an attempt to compensate for this, many UPS manufacturers have invested heavily in adapters which when combined with the present generation UPS provide partial solutions in limited areas. However some physical requirements are often impossible to meet with the present system. Consequently, a significant amount of research is being directed towards medium power UPS to complete the present *"5th Generation"* evolutionary stage and thus eliminating the need for various adapters, reducing space and weight requirements and permitting less expensive operation in the widening spectrum of office and industrial applications.

This thesis contributes to this research trend by presenting the theory and design of a UPS tailored to new applications meeting many of the challenges required by todays typical UPS customers. Solutions to the major setbacks presently encountered are derived, implemented and tested leading to a high performance UPS.

Chapter two initially outlines a framework of specifications for a UPS which is expected to complement the new, more specification stringent environment. Since focus is given on overcoming the modern electrical and physical challenges previously presented, attention is focused primarily on the power train. A number of secondary items (which are clearly important

during actual design) have virtually no significance on the results presented. For this reason items such as the transfer switch, transient response, battery storage facilities, low voltage disconnects, overload conditions, electromagnetic interference, loop compensation and circuitry surveillance are given little consideration.

The chapter then presents an improved topology which is expected to satisfy the needs of the modern requirements by reducing weight and size. The topology highlights a high frequency link stage to provide electrical isolation.

Thirdly a critical evaluation of pulse width modulation techniques is presented leading to the selection of the most compatible ones for the UPS topology selected. This leads to further size and weight reduction.

Finally, chapter two presents developed software tools essential to accurate UPS design and evaluation. The software routines include a worst case inverter ratings program and an analysis/simulation program.

Chapter three focuses on the UPS power systematic power train design. The power train is segregated into three stages; the rectifier stage, the high frequency link stage and the inverter stage. Each is analyzed and optimized separately, worst case component ratings are evaluated and selected sections are simulated and/or experimentally proven. Three possible options for a high frequency link stage are evaluated. The most appropriate one is selected based on practical limitations. However, not to exclude future improved component availability, all component stresses and ratings are done in a per unit system thus simplifying future pro rating. Attention is also focused on items which are of practical importance such as semiconductor drive and switch evaluation, controllers for each stage, snubbers, gating requirements such as delays/overlaps, transformer saturation and cost considerations. This ensures

that practical limitations are not simply ignored during the design and evaluation process.

Chapter four focuses on special UPS load considerations which are not typically addressed in present UPS designs. The load effects are evaluated and utilized to make design and strategy adjustments to the UPS topology. After optimally designing the output filter and applying a novel high performance PWM technique the improved inverter stage is simulated and experimentally verified under various harsh loading conditions.

Chapter five summarizes all conclusions and extrapolates the extent to which the design goals were achieved. Moreover further areas of continuing research are presented.

2.0 UPS DESIGN CRITERIA

2.1 Introduction

An overview of a wide variety of UPS manufactures data sheets will reveal that specifications can be subdivided into two classes. The first class encompasses a majority of requirements which have been developed and accepted over decades rendering them as virtual industry wide standards. These include specifications such as

-Total Harmonic Distortion (THD) < 5%

-Maximum harmonic amplitude < 3%

-Input power factor at rated load > .9

In contrast, the second class contains several specifications which have not solidified and remain relatively inconsistent. Although many manufacturers of UPS now list their respective specifications, a uniform standard is often lacking. Specifications in this category typically include

-Allowable unbalanced load

-Output Power Factor

-Power Density

-Allowable Nonlinear Load

Using typical applications, publications and surveys, a modern specifications table is constructed encompassing both classes. A comparison between present typical UPS specifications and the modern specifications table reveals critical performance characteristics which are in need of being upgrading to meet the requirements of modern consumer applications.

Given incomplete specifications, the presently existing popular *4th generation UPS topology* is segregated into smaller sections in order to

evaluate areas where alterations or restructuring would enhance performance. In order to meet the stringent requirements the overall power train topology is modified. This includes the application of a high frequency link stage yielding a high performance type UPS.

Accompanying the high performance topology is the requirement for an equally high performance PWM technique. The selection of an advanced PWM technique is not a simplistic procedure. With the wide acceptance of gate turn off power devices (eg bipolars, power FETs, GTOs etc) significant research effort has recently been focused on improving converter performance by improved PWM techniques. With still higher performance power semiconductors on the horizon (ie ZTO), PWM is envisioned to carry even greater significance. In response to this a number of "improved" PWM schemes have been proposed to increase converter gain and/or reduce output distortion. However little or conflicting data is available about their merits relative to each other. Further, most PWM schemes are judged by their output voltage spectrum when applied to an inverter stage while numerous other criteria as well as applications should be considered. Since UPS typically contain a controlled rectifier stage as well as an inverter stage it may be erroneous to select the rectifier PWM scheme based on its application to an inverter stage. Consequently, selection of the best PWM technique for UPS applications is accompanied by uncertainty which can lead to less than optimum results. Recognizing this problem, this chapter compares the most prominent PWM schemes, providing the framework for selection of the most compatible PWM technique for the rectifier as well as inverter stages of the proposed high performance UPS power train.

Finally, the void in available software directed towards power electronics necessitates the development of preliminary analysis and design

software tools specially tailored to three phase power converters. This chapter develops two programs capable of evaluating UPS performance characteristics leading to correct component selection. The deve oped programs include an Analysis/Simulation routine [3] and A Worst Case Components ratings routine.

2.2 Modern Medium Power UPS Specifications

2.2.1 Input Specifications

Medium power, when referred to UPS driven critical loads typically falls within the 10-20 kVA range. At this power level three phase 208 volt nominal lines are by, far the most widely used supply rails in North America. Hydro systems offer a typical window of +6%,-10% of nominal voltage [8] and although some power supplies offer brownout handling capabilities until -15% [16], this is often considered to be too conservative since such occurrences are rare. Moreover, batteries make such a step unnecessary and costly.

Frequency variation by hydro is typically +/-1% [8] indicating that the UPS should be conservatively rated at +/-3% to ensure problem free input operation when a heavy load steps on line transiently slowing down hydro generators.

Input power factor is often given little weight by UPS manufacturers yet since total input apparent power is used by electrical utilities as a pricing parameter, a poor power factor becomes costly. Moreover, since most UPS are used at 64% of rated load [6], power factor should be relatively high even at half load. This translates into a modern input power factor requirement of pf >.9 for 50% to 100% load. Other input criteria such as surge protection, electromagnetic interference (EMI) and walk-in are important parameters yet

have no influence within the scope of this thesis and are thus neglected. A summary of the input specifications are given in table T2.1

2.2.2 Output Specifications

The vast majority of linear and nonlinear loads are capable of operating properly with a steady state supply voltage of up to 5% total harmonic distortion (THD) as long as no individual harmonic exceeds 3% in amplitude. The typical modern UPS is designed to deliver these specifications while accommodating balanced and linear loads, which in the past were the majority. However, newer types of loads are not necessarily balanced or linear and can create conditions where the typical UPS inverter stage can no longer maintain waveform specifications possibly leading to load failures. In fact many consumers are now requiring that UPS manufacturers give specifications under nonlinear load conditions as well as linear in order to guarantee performance after purchase [8]. Further, many manufacturers are outlining testing standards for nonlinear applications such as three to one crest to rms single phase load current waveforms at 70% to 85% rated power [8]. This is in anticipation of nonlinear switch mode power supply (SMPS) current demands which are now found in a wide variety of equipment. A second standard often used is a test circuit simulating computer power supplies shown in figure F2.1 [19]. In order to accommodate such loads, the UPS THD requirement should be held to <5% for linear as well as nonlinear loads.

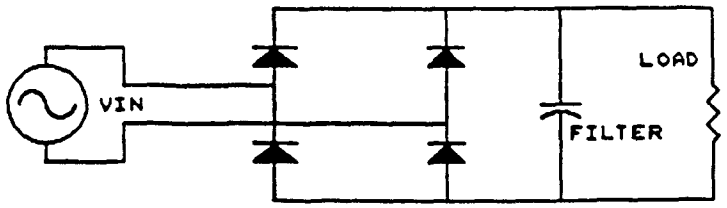


Figure F2.1 Typical SMPS equivalent circuit C=2.8μF/W 1/R=8.7μmhos/W

Unbalanced loads often induce unbalanced load voltages. For some types of loads connected to the same voltage lines the existence of unbalanced voltage may be damaging. Ac motors for instance, may experience dramatic overheating and life reduction due to short circuit, negative sequence rotor currents. The National Electric Manufacturers Association (NEMA) has recommended heavy motor deratings for unbalanced supply voltages greater than 2.5% while operation of motors with greater than 5% supply unbalance is not recommended [20]. By unbalancing loads on the three phase inverter this limit is easily exceeded. Since modern loads are not expected to be balanced, the UPS should keep voltage unbalance to less than 1.5% even under worst case unbalanced load.

Although no standard for acceptable load power factor range has been widely adopted, many manufacturers design to meet loads with limited range of .8 lagging to unity [11]. This avoids larger inverter modulation range and trims down UPS design requirements. However many modern loads such as computers and SMPS do not fall into this range. This dictates that modern UPS should be able to deliver power to a wider range of loads typically varying from .7 lagging to .7 leading.

2.2.3 Physical Specifications

Traditionally size and weight of the UPS has not been a critical

parameter since battery backup size and weight dominated. However many industries and office complexes are reducing battery reserve requirements to the level where only an orderly shutdown procedure need be powered from backup. This has re-focused attention towards UPS physical specifications. Typical medium power 4th generation UPS have a power to weight ratio of roughly (10-15) w/kg without batteries [11],[12],[15]. Modern UPS in the same power range should approach weights that virtually permit wall mounting eliminating the requirement for occupied floor space. This translates into a weight ratio of better than 25w/kg.

In general, size is proportional to weight. A typical UPS has a density of .1-.5w/in^3. This should be increased to 1w/in^3 resulting in office volume cost savings. Further size reduction in the order of 40% can be realized by exploiting forced air cooling with little cost impact. Moreover, MTBF figures of 800,000 hours for fans will not effect the overall UPS system MTBF. Since UPS are now expected to operate in human working environments where normal conversations are to be held, power supply audible noise is a concern. Todays typical 4th generation UPS utilize relatively high semiconductor switching speeds when implementing PWM strategies. For medium power semiconductors the maximum switching frequency is relatively low creating in many instances unbearable noise in the range of 1 to 18Khz. This often forces added considerations and expense for utilization of such a converter in the working environment. Further, the use of forced cooling rather than convection will create additional noise. Summing all elements contributing to noise, the modern office environment will have audible noise of less than 55 - 65dba at 1 meter distance with a 45dba ambient noise [21].

Operating temperature in controlled environments seldom exceeds 30^0 C, however the UPS is expected to operate when environmental control is

temporarily disabled. The size of the UPS is related to the maximum ambient temperature and the allowable components temperature rise. The UPS should be fully operational in a 40^0 ambient. This gives a baseline for heatsink size. Efficiency of the power supply is also a critical parameter influencing cost directly and MTBF indirectly. Todays UPS efficiency ratings fall in the 72% to 85% range depending on operating conditions. Design of a modern UPS should allow for no lower than 80% efficiency at nominal load to keep user costs low and MTBF high.

A summary of the specifications is listed in table T2.1

INPUT:	Voltage 3-ϕ 208 +10% -10%
	Freq 60 ±3hz
	Power Factor >.9 from 50% to 100% load
OUTPUT:	Voltage 208
	Power 5-15Kva
	THD <5%
	Maximum harmonic <3%
	100% nonlinear load capacity
	typical 120° pulse for 3-ϕ
	typical 3-1 peak to rms ratio for 1-ϕ
	Full unbalanced load capabilities
	Including open loads
	100% combination of unbalanced and nonlinear loads
	Power factor: .7 lag to .7 lead
PHYSICAL:	Temperature operation 0°-40°
	Forced air cooling
	Weight ratio >25W/kg
	Density >1W/in^3
	Audible noise <65 dba
	Efficiency: >80%

Table T2.1 Modern UPS Specifications

2.3 UPS Topology Evaluation

Numerous UPS topologies exist for medium power applications with respective advantages and drawbacks. Included in the list of topologies is the Ferroresonant version which is either "on line" and inefficient, or "off line" increasing risk of unavailability . The triport UPS which has the battery charger and inverter stages merged also has handicaps since during its standby stage the complex inverter design delivers charging power to the batteries. Should supply failure occur, the inverter must reverse the power flow to supply the starved load. The low voltage transfer time interval may be to severe for some loads. Square wave UPS,s have limited application as they do not produce a sine wave output. The most common UPS structure available today and possibly the most reliable one is shown in block form in figure F2.2. Classified as a 4th generation UPS, this configuration will be referred to throughout this thesis as the benchmark topology.

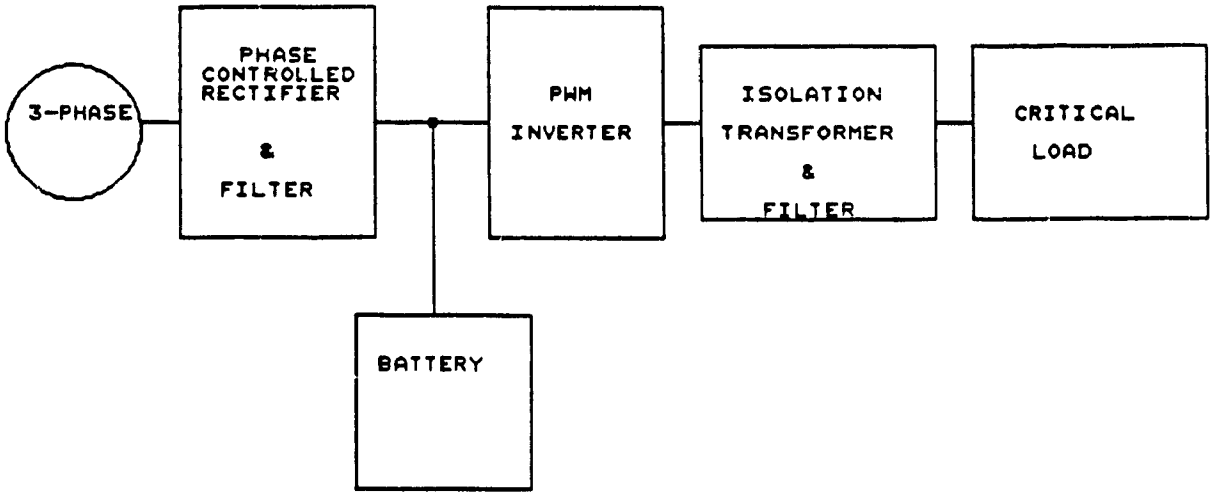


Figure F2.2 4th generation UPS power train topology

The phase controlled rectifier typically consists of thyristor semiconductors and a single order inductive filter. This stage is shown in

expanded form in figure F2.3. The rectifier output voltage swing is given by

$$V_{DC} = \sqrt{2}\,\frac{3\cdot(V_{RMS}-V_{DROP})}{\Pi}\cdot COS(\alpha) \qquad (2.1)$$

where V_{drop} = typical combined line and thyristor drop at at medium power levels

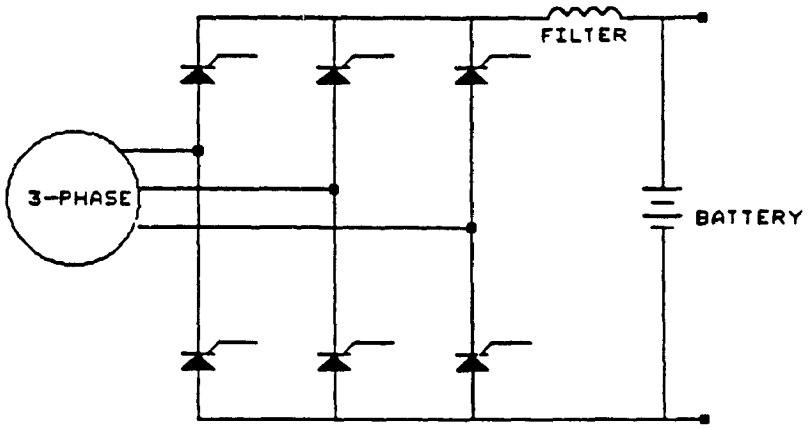


Figure F2.3 Phase controlled rectifier/battery charger stage

The batteries must be kept at "float" voltage potential continuously in anticipation of a power failure. This voltage is roughly 2.25 volts per battery cell. During a power failure the battery terminal voltage is permitted to diminish to 1.75 volts per cell before permanent damage due to deep discharge will occur. At low ac line

$$V_{RMS} = 183V$$

At this voltage the rectifier will be at full conduction angle (ie $\alpha=0^{\circ}$ = diode bridge action) giving the rated "float" voltage of the batteries as

$$V_{DCFLOAT} = \sqrt{2}X\frac{3(183-5)}{\Pi}COS(0^{\circ}) = 240V \qquad (2.2)$$

The maximum firing angle corresponds to maximum input line voltage

capabilities after an ac failure at which point in time the battery pack voltage has depleted to virtual low voltage disconnect point. The angle can be determined from the ratio of minimum to maximum battery voltage given by

$$Bd = \frac{1.75}{2.25} = .78$$

Therefore at high ac line

$$V_{RMS} = 229V \qquad V_{DROP} = 0V$$

and the minimum battery voltage firing angle is given by

$$\alpha = \text{ARCCOS}\left[\frac{V_{DCFLOAT} \cdot Bd \cdot \Pi}{\sqrt{2} \cdot 3(V_{RMS} - V_{DROP})}\right] \tag{2.3}$$

or

$$\alpha_{min} = \text{ARCCOS}\left[\frac{240 \cdot .78 \cdot \Pi}{\sqrt{2} \cdot 3(229-0)}\right] = 52^{\circ}$$

The harmonic voltages present at the rectifier output terminals are derived using fourier series and are given by

$$HAR_N = \sqrt{HARA_N^2 + HARB_N^2} \tag{2.4}$$

where

$$HARA_N = \frac{6}{\Pi}\int_{\alpha+(\pi/3)}^{\alpha+(2\pi/3)} V_{IN} \sin(N \cdot \omega\tau)\, d\omega\tau$$

$$HARB_N = \frac{6}{\Pi}\int_{\alpha+(\pi/3)}^{\alpha+(2\pi/3)} V_{IN} \cos(N \cdot \omega\tau)\, d\omega\tau$$

$$V_{IN} = \sqrt{2}\, V_{RMS} \sin(N \cdot \omega\tau) \tag{2.5}$$

$$N = 6, 12, 18, \ldots\ldots, \infty$$

The dominant harmonic to be filtered will be the sixth for which at

$$\alpha = 52^{\circ}$$

results in

$$HAR_N = 84V$$

or 44% of the dc level voltage. Since battery manufacturers recommend less than <5% ripple for full battery life span [22], this harmonic would have to be reduced to roughly 2% indicating a bulky filter requirement. The filter would typically be at a break frequency of

$$FBK = \left[\frac{HAR_{FUND} \cdot RK}{HAR_{DOM}}\right]^{1/Fo} \cdot ORDER \cdot FBASE \qquad (2.6)$$

Where

FBK	=	Filter break frequency required to reduce the dominant harmonic to RK times the fundamental
RK	=	Reduction factor=.02
HAR_{FUND}	=	186V
HAR_{DOM}	=	84
FBASE	=	Input supply frequency=60hz
Fo	=	Filter order=1 (choke only)
ORDER	=	dominant harmonic order =6

Evaluation of equation 2.6 gives

$$FBK = 16hz$$

These result translates into the requirement of a large output filter reactor going against the desired weight and size reduction. Moreover, reflected back on the input ac side, the power converter contributes to a poor power factor and an input line current with low order harmonics. The input line current harmonic ratios at full conduction are given by

$$\left|\frac{I_{IN_N}}{I_{IN_1}}\right| = \frac{1}{N} \qquad (2.7)$$

$$N = 1,5,7,11,13,\ldots,\infty$$

A 20% fifth, 14% seventh, etc. as equation 2.7 indicates, may lead not only to poor power factor, but input voltage distortion and power line overheating. To overcome these problems, and the ongoing expense of poor power factor, shunt capacitors are often used [23]. These components are also large and bulky once again going against the weight and size reduction requirements.

The battery stage is generally independent of the power electronics design. Weight and size are directly related to charge required and battery type. The cells are considered to be external to the UPS electronics and may not necessarily be located in its vicinity.

The PWM inverter stage generally employs gate controlled semiconductors such as GTO's or darlingtons. An expanded version of the inverter stage represented in figure F2.2 is shown in figure F2.4.

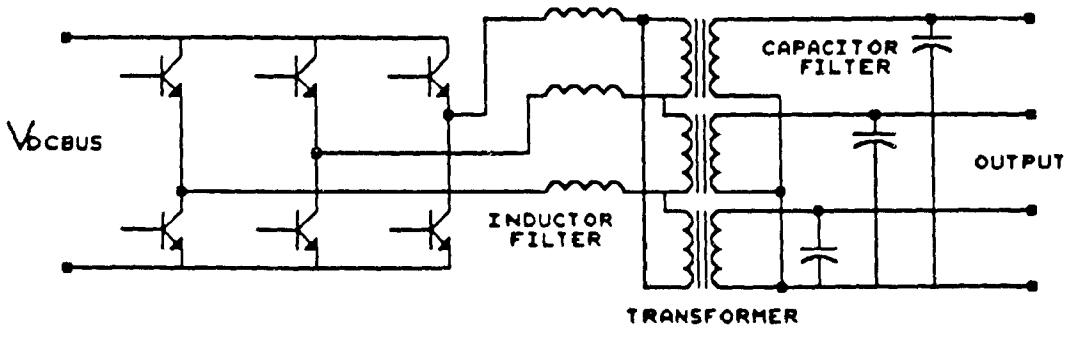


Figure F2.4 3-ϕ UPS inverter stage

By increasing switching frequency the output filter is generally reduced in

size. However, typical PWM inverters in the medium power class have limited switching speed due to associated switching stresses. The required filter design to reduce the harmonic content typically contains poles in low frequency ranges which pose a high risk of increasing THD when the UPS is supplying power to a nonlinear load. Further, the relatively high impedance of the filter causes unbalanced voltages when power is supplied to unbalanced loads which may cause undesirable effects. Finally, PWM reduces the inverter voltage gain. This implies higher component currents, higher temperature operation and lower reliability.

The isolation transformer is used for voltage matching, isolation and to create a ground reference for single phase loads (delta-wye windings). At 60hz rated frequency, the three phase transformer may weigh hundreds of pounds. The transformer stage is generally the largest and heaviest item (excluding batteries) in the UPS. Therefore a major concern of an improved design is the reduction in the size and weight of the output transformer.

2.3.1 Proposed UPS Topology

The new topology shown in figure F2.5 would address the requirements associated with the specifications outlined earlier.

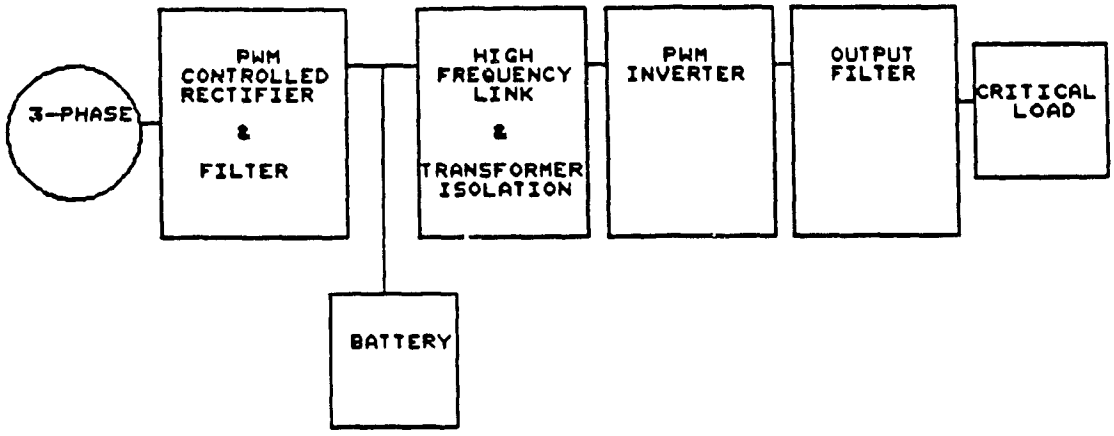


Figure F2.5 Proposed 60hz UPS topology

The novelties of this topology can be categorized as follows:

1) Input stage;

A PWM controlled rectifier replaces the previous 4th generation style phase controlled bridge. The associated advantages are;

-A reduction of input and output harmonic distortion. This implies reduction of filter size, weight and cost.

-Linear modulation control rather than "COS(α)" control previously encountered in the phase controlled rectifier. This should simplify control.

-Improved input power factor which further reduces required filtering and user ongoing cost penalties.

-Improved dynamic response. A line or battery transient could be compensated with higher speed resulting in a larger bandwidth.

2) Inverter stage;

The PWM inverter and transformer are replaced with a

high frequency link stage (HF link) and a regulated input PWM inverter. The associated advantages are;

-Isolation is now provided by a 2 Kg high frequency transformer rather than 300 Kg low frequency version. This dramatically reduces weight and size.

-Since the inverter input is regulated, high performance fixed pattern PWM techniques can now be applied to the inverter. This results in higher voltage gain and lower switching frequencies thus reducing switching stresses and improving the input and output harmonic distortion. This translates into further filter size and weight reduction.

-The gating and control of the 3-ϕ inverter is simplified thus improving its reliability.

3) Output filter stage;

The output filter stage is strategically designed to permit passive compensation for the application of a wide range of modern loads. The associated advantages are:

-Ability to supply power to fully nonlinear loads.

-Ability to supply power to fully unbalanced loads.

-Ability to supply full rated power to single phase loads.

-Improved dynamic response for accommodation of special switch mode power supply loads.

-Lower filter cost, size and weight.

4) General topology advantages;

Further indirect topology advantages include;

-The use of forced air cooling to further shrink heatsink size and weight. The fans provide for little reliability downgrade or maintenance increase. Fan filters are not required because air flow is solely through the confined heat sink apparatus.

-Common power semiconductors throughout the power stages and as a result a single style of base drive. This drives cost down because of increased quantities. It also tends to increase quality due to increased simplicity.

The overall objective of the UPS topology is to substantially reduce size and weight over the present 4th generation UPS while at the same time exceeding previous performance capabilities to reach the high performance specifications outlined in chapter 2.2.1.

2.4 PWM For Improving Power Converter Performance

In power electronics, (PWM) is an operation performed on "raw" voltage and current waveforms to shape their spectra in a way beneficial to the application under consideration. Spectra shaping typically means the creation of a 'deadband' between wanted and unwanted spectral components to ease post PWM filtering requirements. For a given switching frequency it is desirable that the deadband be as wide as possible. To illustrate this point figures F2.6A,B,D and E show a typical inverter line to line output voltage before and after it has been pulse width modulated. Figure F2.6C and F show the resulting line current waveforms obtained with a load power factor of .8 lagging. In particular, figure F2.6F shows that PWM allows static inverters to generate close to ideal output waveforms while providing variable voltage and variable frequency operation. In addition to the importance of spectral shaping, the

main advantage of PWM is that it allows linear amplitude control of the output voltages/currents by varying a linear signal.

Further investigation of the results shown in figure F2.6 also reveals that PWM has several disadvantages, which include:

1-Attenuation of the wanted fundamental component, in this case from 1.1pu to .866pu.

2-Drastically increased switching frequencies (in this case from 1pu to 21pu). This means greater stresses on the associated switching devices and therefore derating of those devices.

3-Generation of high frequency harmonic components not previously present.

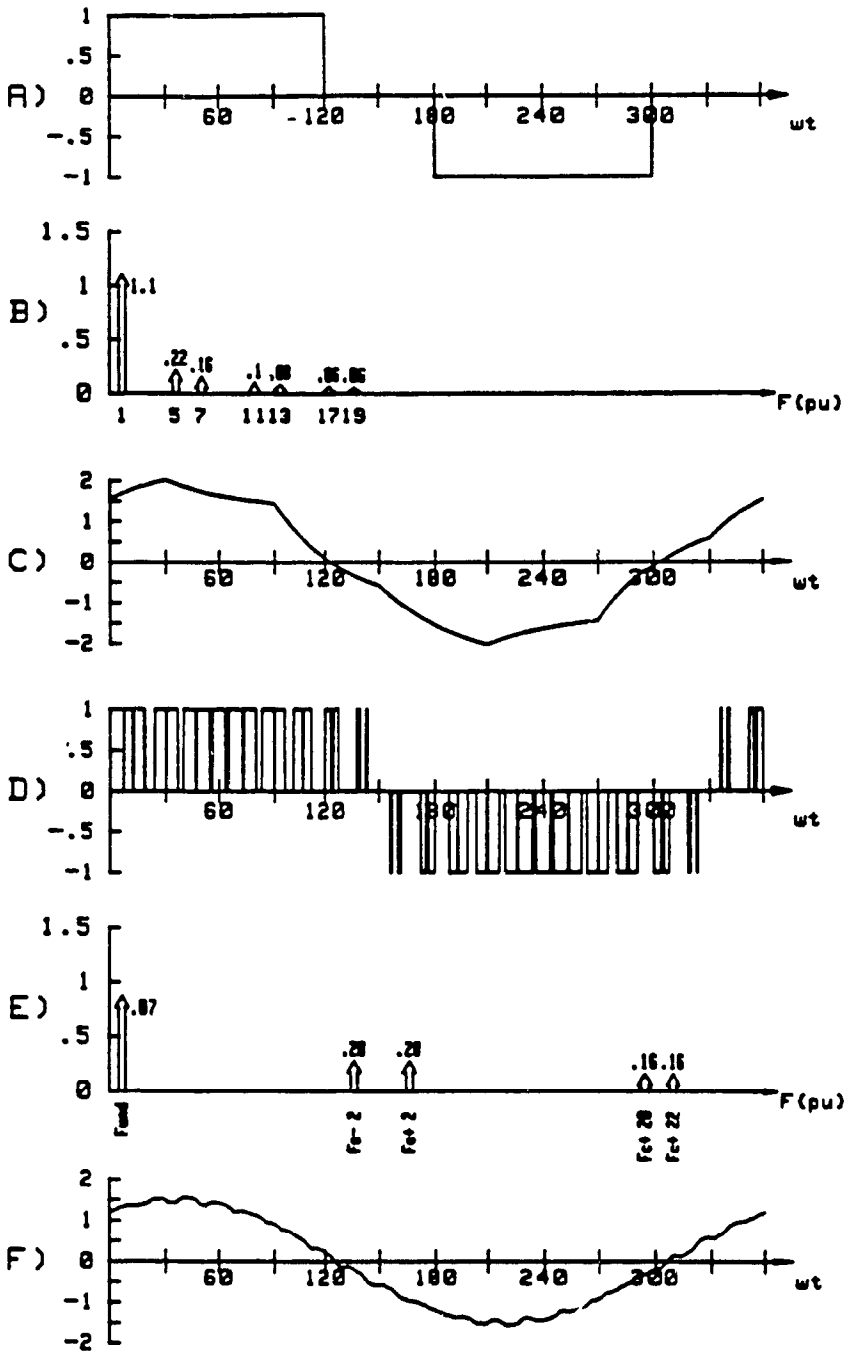


Figure F2.6 Inverter voltage and current waveforms with six step and sinusoidal(SPWM) operation.
A) Square wave output line to line voltage
B) Line to line voltage spectrum (square wave)
C) Output line current (square wave)
D) SPWM output line to line voltage
E) Line to line voltage spectrum (SPWM)
F) Output line current (SPWM)

Since the advantages of PWM outweigh the respective disadvantages, a considerable research effort has gone into minimizing the PWM disadvantages mentioned earlier. As a result numerous PWM schemes have been introduced over the past decade offering specific advantages in specific applications. Since dramatic UPS improvements can be obtained with PWM it is imperative to select the appropriate technique for both the controlled rectifier stage and the inverter stage. To date only a handful of techniques have proven to be widely used and are so called '*improved*' PWM techniques [25],[26],[27],[28],[29]. However, previous work related to these improved techniques has been focused on converter output spectra neglecting other important criteria such as input spectra, input/output distortion factor, switching frequencies and hardware implementation considerations. Furthermore, another focus of previous work has been inverter applications neglecting in the process some other equally important areas such as controlled rectifiers. Consequently a clearer picture should be developed before selecting a PWM technique for UPS avoiding less than optimum results.

Since there are several PWM techniques and two types of converters involved in this evaluation, care must be taken to present relevant results with clarity. For this purpose, a generalized bridge converter (figure F2.7 comprised of six ideal four quadrant switches has been employed. The main advantage of this converter is that because of the nature of its switches it can function either as an inverter (voltage or current sourced) or as a rectifier by simply applying the proper gating signals. The generalized converter thus permits the ac terminal waveforms (AC TERM) to represent either;

A) The line to line voltage of a voltage source inverter(VSI),

B) The input line current of a controlled rectifier(CR),

and the dc terminal waveforms (DC TERM) to represent;

A) The input current of a VSI,

B) The output voltage of a CR.

Also in the evaluation that follows, the switching frequency of the bridge is kept constant to provide a common basis for comparison of each technique under rectifying and inverting operation.

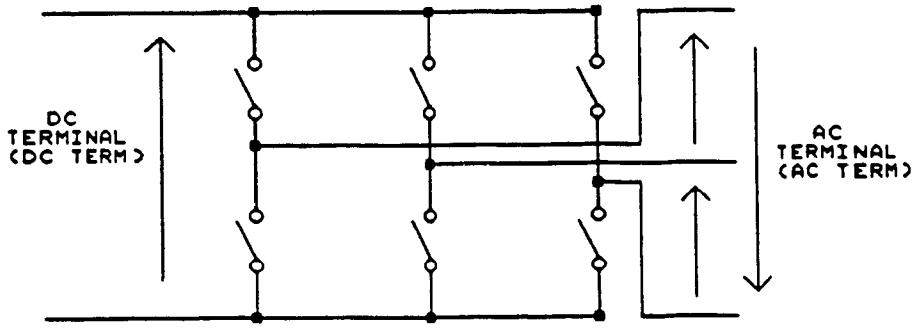


Figure F2.7 Generalized bridge configuration

2.4.1 Carrier PWM Techniques

Carrier PWM techniques represent any firing pattern whose angles are derived by the intersection of two waveforms namely the carrier and reference. A vast number of schemes fall into this category. The more prominent ones include;

1) Sinusoidal PWM (Figure F2.8) [24]

2) Modified Sine PWM (Figure F2.9) [25]

3) Third Harmonic Injection PWM (Figure F2.10) [26],[27]

4) Harmonic Injection PWM (Figure F2.11)

2.4.1.1 The Original Sine PWM Technique [24]

This original technique has been included for the purpose of using it as a 'benchmark' to evaluate respective improved techniques. Its main intrinsic features are shown in figure F2.8. The largest disadvantage with this technique is that the maximum possible AC TERM and DC TERM gain values are only

$$G_{AC} = .866 \qquad \text{and} \qquad G_{DC} = .75$$

respectively. Where;

1) AC TERM gain (G_{AC}) is the ratio of maximum value (peak) of the fundamental component of the ac terminal waveform to the amplitude of the unfiltered switched dc pulses comprising the same terminal waveform.

2) DC TERM gain (G_{DC}) is the ratio of the maximum value of the dc component of the dc terminal waveform to the maximum amplitude of the unfiltered pulses comprising the same terminal waveform.

The main advantage of this technique is that it generates line to neutral ac spectra with no third order harmonics. This allows the use of neutral to neutral connections (if required) and decoupled (individual) control of each one of the three inverter phases.

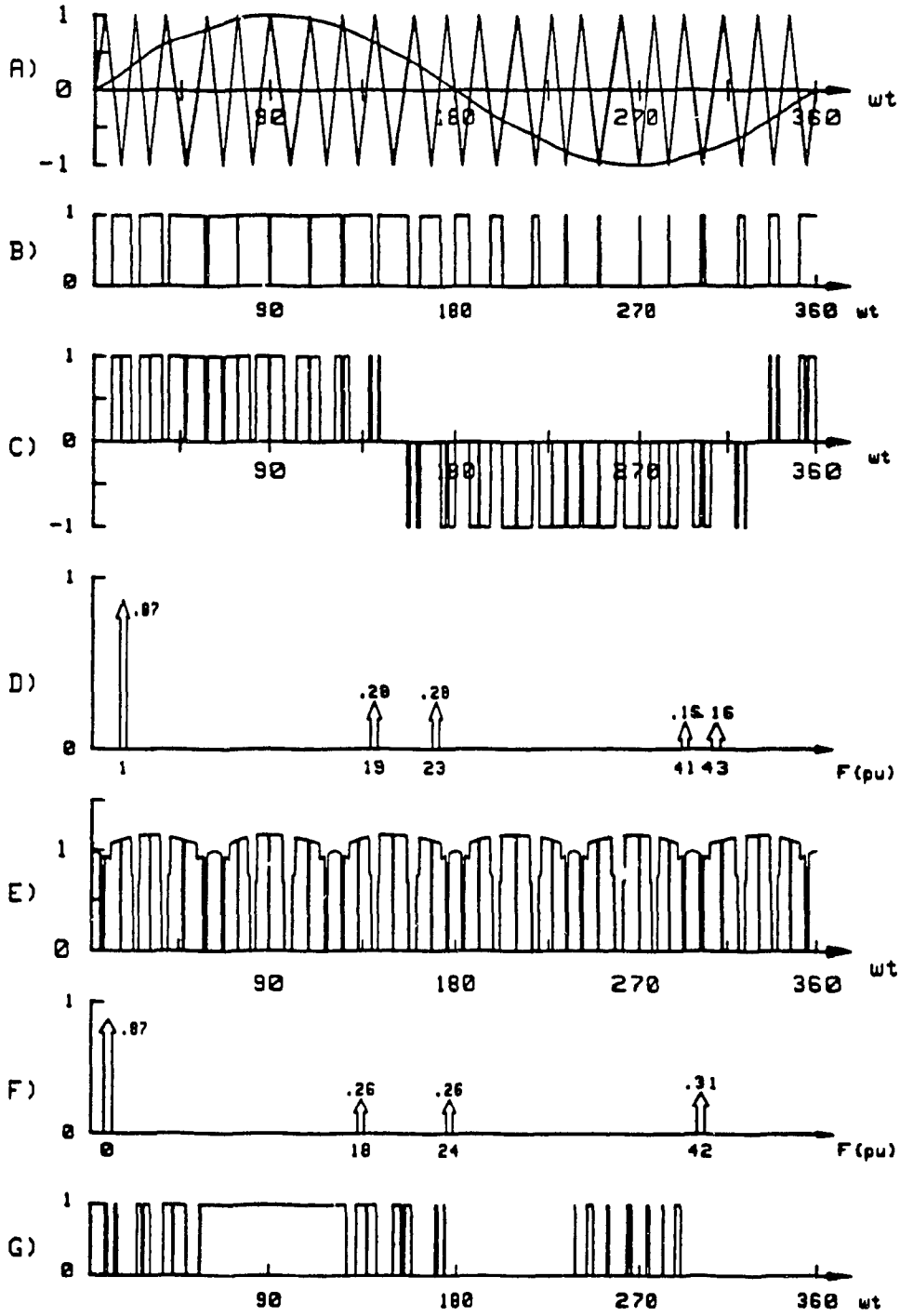


Figure F2.8 Sinusoidal PWM (SPWM)

A) SPWM scheme
B) VSI switch#1 gating signal (GSW1)
C) AC TERM
D) AC TERM spectrum
E) DC TERM
F) DC TERM spectrum
G) CR switch#1 gating signal

2.4.1.2 The Modified Sine PWM Technique [25]

The main intrinsic features of this technique are shown in figure F2.9. Separate spectra are shown for VSI and CR operation respectively in order to maintain the same switching frequency. In particular;

A) This technique defines the AC TERM (figure F2.9C on a line to line basis for VSI's and on a line basis for CR's.

B) As shown in figure F2.9A and B only the first and last 60° intervals (per half cycle) of the AC TERM waveform are directly defined through intersections of respective sine(reference) and triangular(carrier) waveforms. The 60° to 120° intervals are obtained by folding the first and last 60° intervals around the 60° and 120° points respectively.

C) As shown in figure F2.9D, this technique provides a substantially higher AC TERM gain as compared with the original sine PWM technique (Figure F2.8). However, from part (B) above it follows that hardware implementation for this technique is rather complex. Also, this technique generates a substantial (21%) AC TERM third harmonic component on a line to neutral basis. Under balanced and open neutral operating conditions however, third harmonic currents cannot flow and thus the third order voltage harmonics are neutralized.

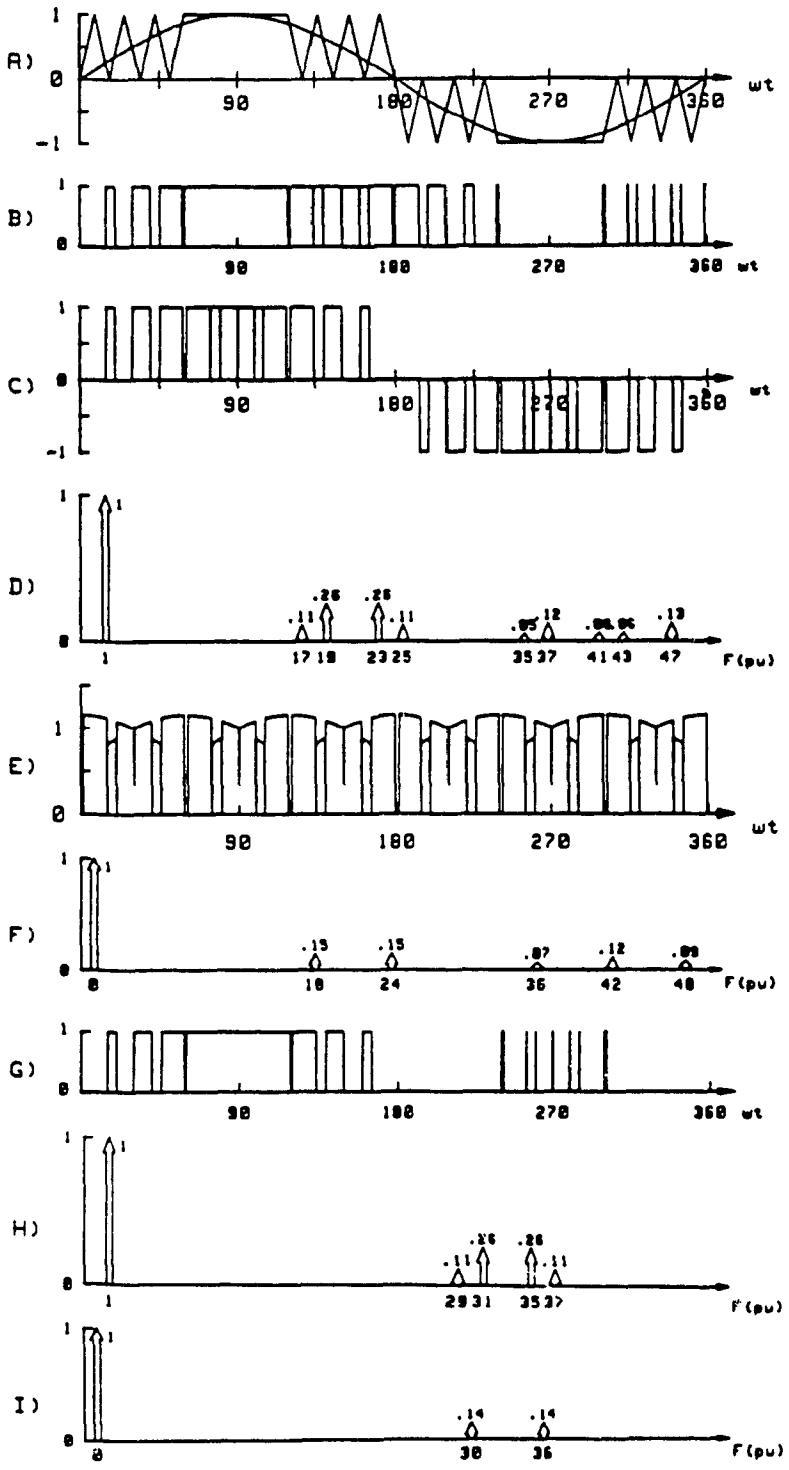


Figure F2.9 Modified Sinusoidal PWM (MSPWM)

A) MSPWM Scheme
B) VSI switch#1 gating signal (GSW1)
C) VSI output voltage
D) VSI output voltage spectrum
E) VSI input current
F) VSI input current spectrum
G) CR switch#1 gating signal
H) CR line current spectrum
I) CR output voltage spectrum

2.4.1.3 The Third Harmonic Injection PWM Technique [26] [27]

This improved technique has been derived from the original sine PWM technique (Figure F2.8) through the addition of a 17% third harmonic component to the original sine reference waveform. The resulting flat topped waveform shown in figure F2.10 allows over modulation (with respect to the original sine PWM technique) while maintaining excellent AC TERM and DC TERM spectra. In particular:

A) The analytical expression for the reference waveform is

$$Y=1.15\cdot\sin(\omega\tau)+.19\cdot\sin(3\omega\tau).$$

B) The AC TERM gain (Figure F2.10D) is equal to the respective gain obtained with the modified sine PWM (Figure F2.9D) and substantially higher than the gain obtained with the original sine PWM technique (Figure F2.8D).

C) Furthermore, from figure F2.10A it can be deduced that the hardware implementation of this technique is quite simple. However, this technique also generates a substantial AC TERM third harmonic component (17%) on a line to neutral basis.

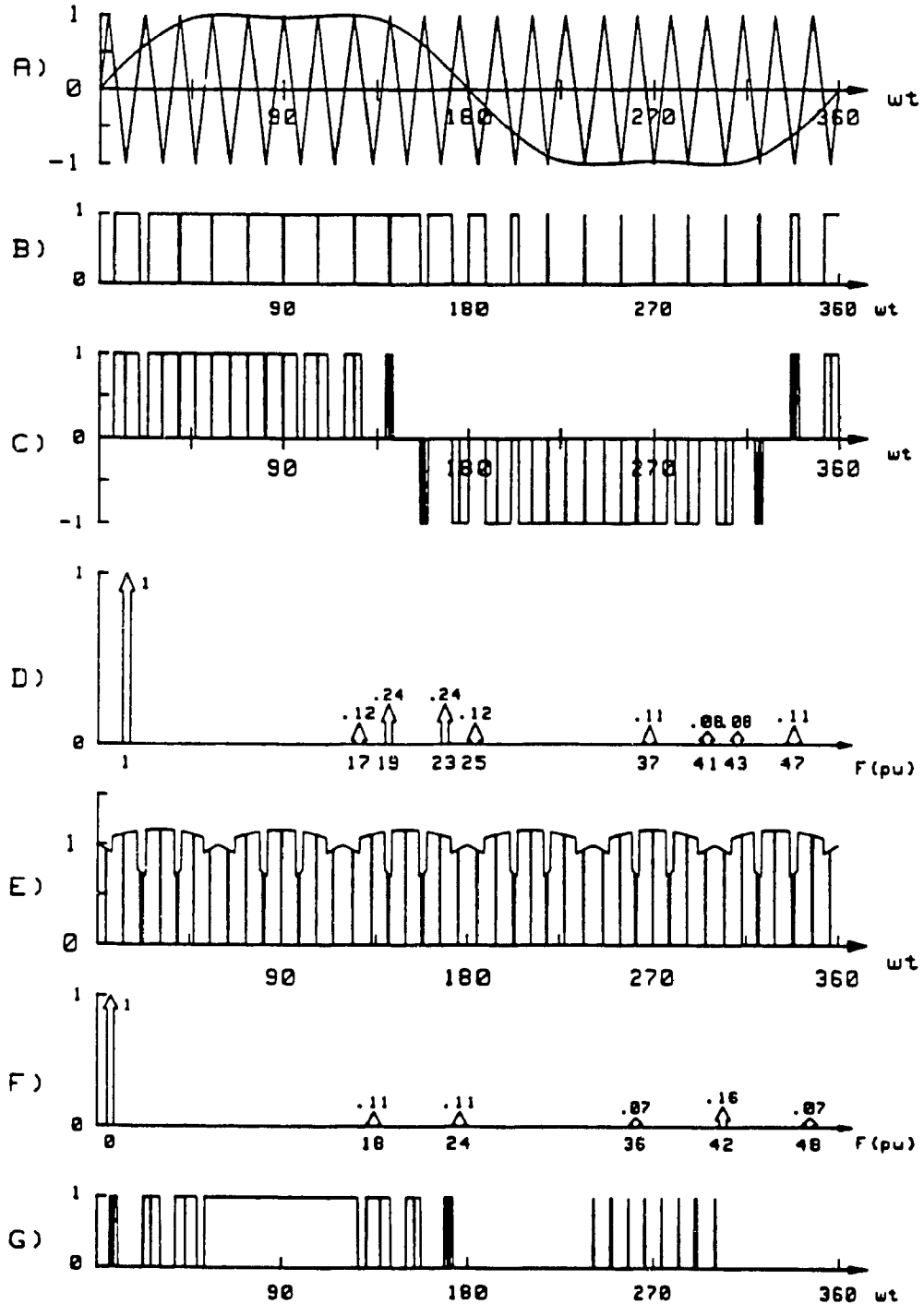


Figure F2.10 Harmonic Injection PWM (HIPWM) (1st & 3rd)

A) HIPWM scheme
B) VSI switch#1 gating signal (GSW1)
C) AC TERM
D) AC TERM spectrum
E) DC TERM
F) DC TERM spectrum
G) CR switch#1 gating signal

2.4.1.4 The Harmonic Injection PWM Technique

This technique shown in figure F2.11 is a variation of the previously discussed third harmonic injection technique. The variation is obtained by injecting additional harmonics in the respective reference waveform. The resulting waveform (Figure F2.11A) again allows over modulation while improving even further the resulting frequency spectra of the AC TERM and DC TERM waveforms. In particular;

A) The analytical expression for the reference waveform is now

$$Y = 1.15 \cdot \sin(\omega\tau) + .27 \cdot \sin(3\omega\tau) - .029 \cdot \sin(9\omega\tau).$$

B) The AC TERM gain (Figure F2.11D) is equal to the gain obtained with the previous two improved PWM techniques, while the harmonic spectra of AC and DC TERM waveforms are clearly better.

C) Again as deduced from figure F2.11A, the hardware implementation of this technique is as simple as with the SPWM and the third harmonic injection techniques.

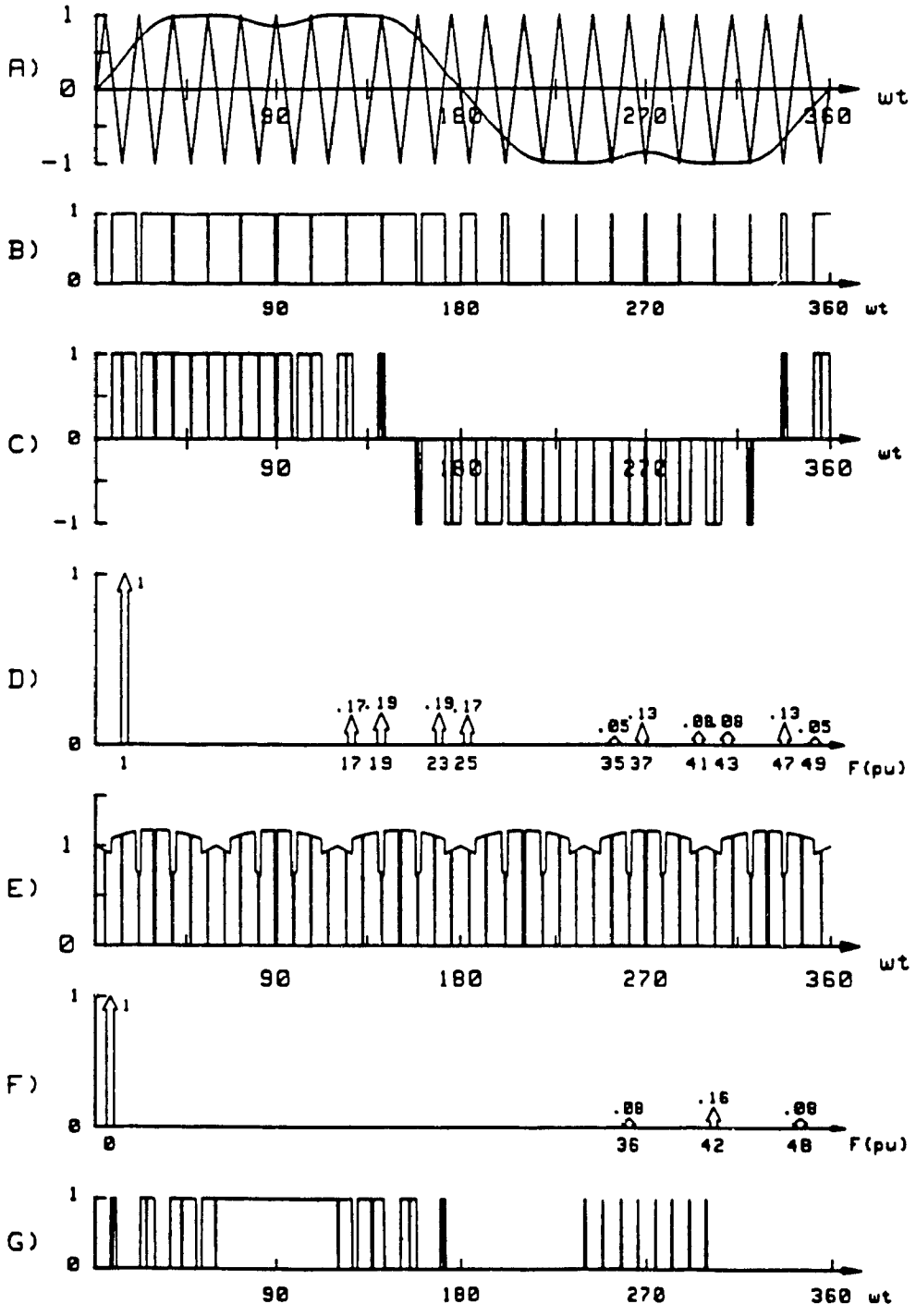


Figure F2.11 Harmonic Injection PWM (HIPWM) (1st & 3rd & 9th)
A) HIPWM scheme
B) VSI switch#1 gating signal (GSW1)
C) AC TERM
D) AC TERM spectrum
E) DC TERM
F) DC TERM spectrum
G) CR switch#1 gating signal

2.4.1.5 Waveform Quality Under Variable Modulation Index Conditions

Although the waveforms shown in figures F2.8 through F2.11 provide an accurate characterization of the evaluated PWM techniques, they also have the disadvantage of showing respective harmonic spectra at only one modulation index value. (ie M=1). However in most applications, output converter power is controlled by varying the modulation index value. It therefore becomes necessary to investigate the quality of the various converter waveforms obtained with each of the techniques for all modulation index values. Three quality indexes used to evaluate these waveforms are defined as follows;

$$DF_1 = \frac{100}{G_{ACMAX}} \sqrt{\sum_{n=5,7..}^{\infty} \left[\frac{HAR_N}{N^2} \right]^2} \qquad (2.8)$$

$$DF_2 = \frac{100}{G_{ACMAX}} \sqrt{\sum_{n=5,7..}^{\infty} \left[\frac{HAR_N}{N} \right]^2} \qquad (2.9)$$

$$DF_3 = \frac{100}{G_{DCMAX}} \sqrt{\sum_{n=6,12..}^{\infty} \left[\frac{HAR_N}{N} \right]^2} \qquad (2.10)$$

Where: DF_1 = ac terminal distortion factor for second order ac side filtering

DF_2 = ac terminal distortion factor for first order ac side filtering

DF_3 = dc terminal distortion factor for first order dc side filtering

The variations of these three quality indexes as a function of M are shown in figures F2.12, F2.13 and F2.14 respectively.

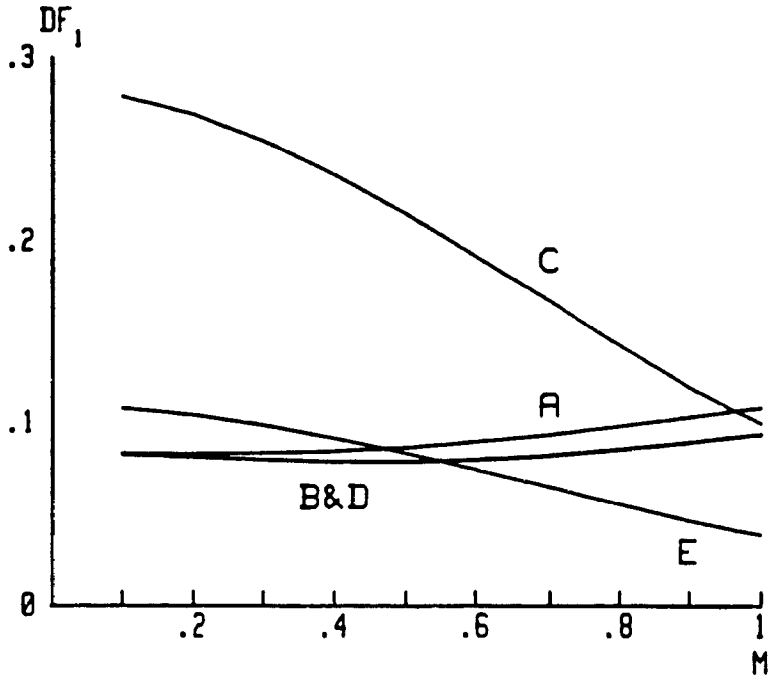


Figure F2.12 2nd order filter distortion factor (AC TERM)
A) SPWM
B) HIPWM (1st & 3rd)
C) MSPWM VSI operation
D) HIPWM (1st & 3rd & 9th)
E) MSPWM CR operation

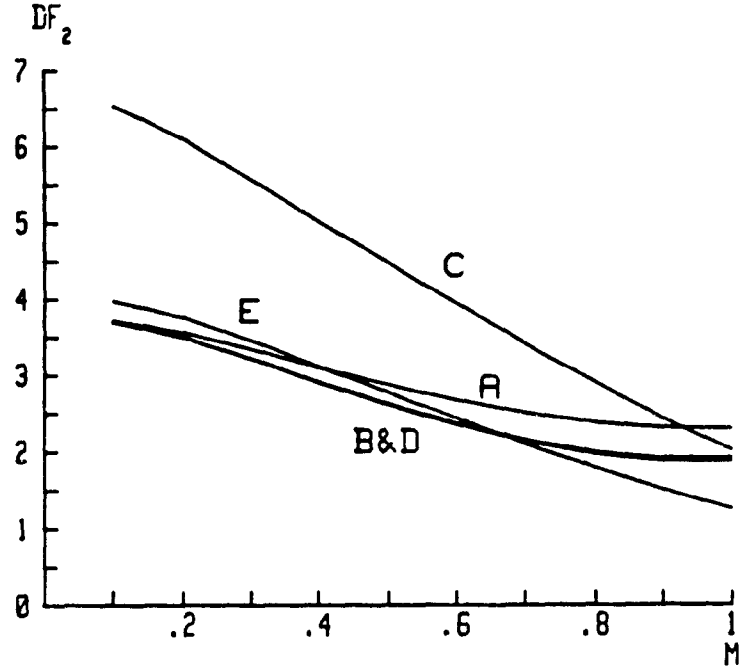


Figure F2.13 1st order filter distortion factor (AC TERM)

A) SPWM
B) HIPWM (1st & 3rd)
C) MSPWM VSI operation
D) HIPWM (1st & 3rd & 9th)
E) MSPWM CR operation

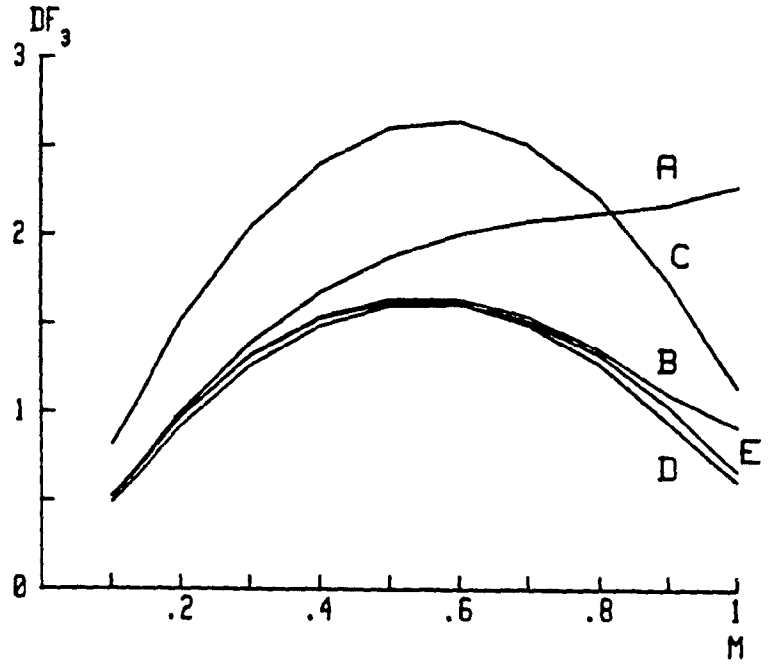


Figure F2.14 1st order filter distortion factor (DC TERM)
A) SPWM
B) HIPWM (1st & 3rd)
C) MSPWM VSI operation
D) HIPWM (1st & 3rd & 9th)
E) MSPWM CR operation

It is noted that DF_1, DF_2 and DF_3 have been defined in ways that reflect actual levels of harmonic distortion experienced in actual applications. For example, static UPS employ a second order L-C filter between inverter and loads. Such filters provide harmonic attenuation which is approximately inversely proportional to the square of the order (N) of the harmonic. Therefore the DF_1 data shown in figure F2.12 are relevant to UPS inverter stages and any other static ac power supply that employs a second order filter. Similarly, ac and dc motors supplied from PWM static converters utilize their respective leakage and armature inductances to produce quasi sinusoidal and quasi dc input current waveforms. These inductances provide first order attenuation to voltage harmonics which is equivalent to dividing the amplitude of each harmonic by its respective order. Therefore the DF_2 and

DF_3 data shown in figures F2.13 and F2.14 are applicable to ac and dc motor drives. Controlled rectifiers supplying UPS power also falls in this category as any other similar application utilizing a first order filter.

To stress emphasis on the input spectral content of each technique, a quality index is defined for the rms ripple value that the input filter must tolerate or support. The rms current rating I_{CII} of the dc link capacitor for VSI operation is shown in figure F2.15 as a function of modulation index M. The rms current of the input capacitor I_{CR} for controlled rectification is shown in figure F2.16. The analytical expressions for I_{CII} and I_{CR} are;

$$I_{CII} = \sqrt{\sum_{n=6,12..}^{\infty} I_{IN_N}^2} \qquad (2.11)$$

$$I_{CR} = \sqrt{\sum_{n=5,7..}^{\infty} I_{IN_N}^2} \qquad (2.11a)$$

It is finally noted that although the exact DF_1 , DF_2, DF_3 , I_{CII} and I_{CR} values shown in the figures are valid for only one particular common carrier frequency (shown in figures F2.8A, F2.9A, F2.10A and F2.11A), their shapes and relative position are independent of carrier frequency. Consequently, these data can be used for the general evaluation of the PWM techniques which follow in section 2.4.3.

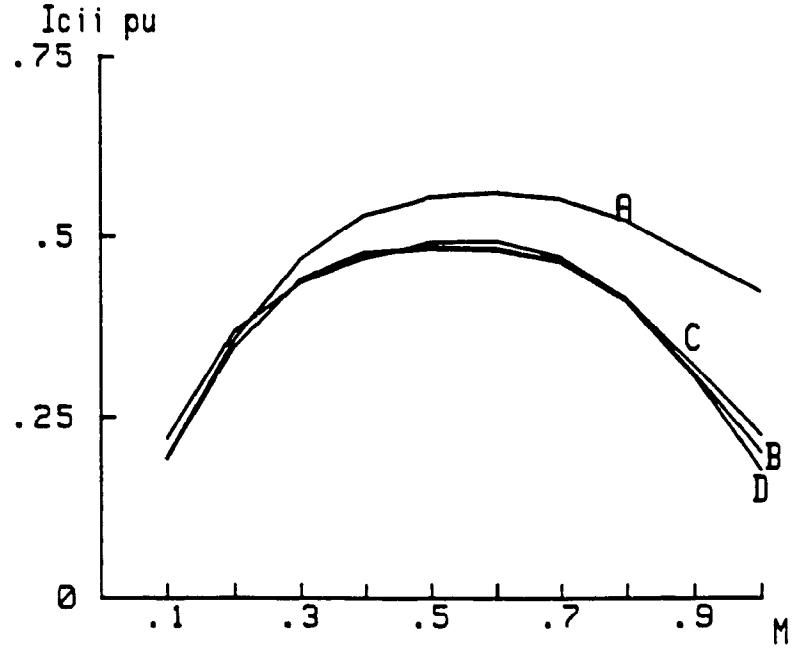


Figure F2.15 Inverter dc terminal rms ripple
A) SPWM
B) HIPWM (1st & 3rd)
C) MSPWM
D) HIPWM (1st & 3rd & 9th)

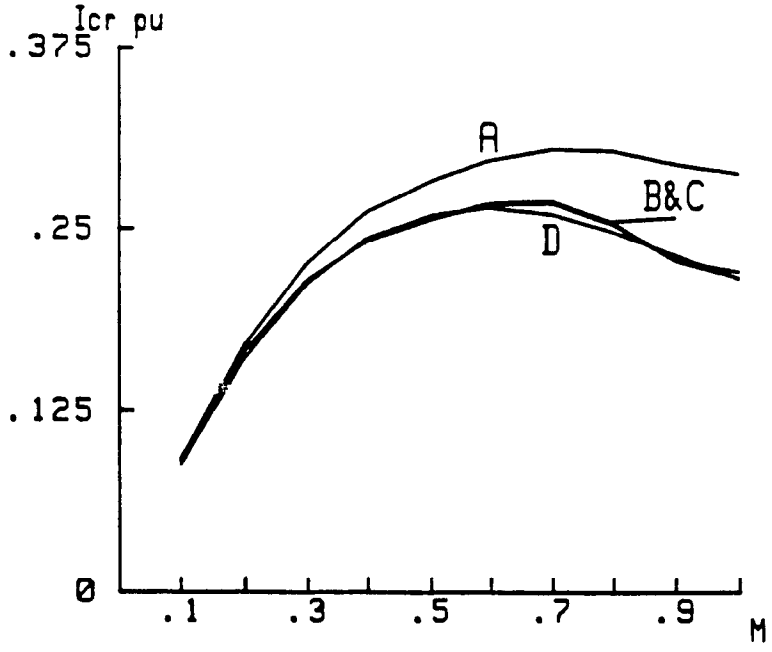


Figure F2.16 Rectifier input capacitor rms ripple current
A) SPWM
B) HIPWM (1st & 3rd)
C)HIPWM (1st & 3rd & 9th)
D)MSPWM

2.4.2 Programmed PWM Techniques [28],[29],[30]

Programmed PWM schemes define firing patterns that are created through computer optimization routines. The computer program may be geared toward minimization of certain criteria such as low order harmonics, THD and/or distortion factor, or may be directed towards the maximization of fundamental component amplitude. Computation time is directly related to the number of harmonics to be controlled. The relatively complex minimization routines typically involve nonlinear matrix manipulations. Good initial approximations are generally required and convergence is not always guaranteed. Due to the nonlinear nature of the problem, the angles reaching the final objective may not be a unique solution. Discrimination by use of distortion factor is then typically used to aid in the selection.

Programmed techniques often offer better voltage utilization and lower switching frequencies than carrier techniques when employed with converters supplied from independently regulated voltage or current sources. However drawbacks also exist with the programmed techniques. These include;

1) The switching angles are occasionally sensitive to fluctuation in exact timing. In actual applications, deadtimes for voltage source inverters and overlaps for rectifiers introduce shifted switching angles which lead to a dramatic alteration of output spectra. Figure F2.17 shows a popular programmed PWM technique derived to eliminate the 5th and 7th harmonics. Table T2.2 shows the actual harmonics measured in a 1 kVA 3-ϕ inverter lab model employing transistors with 20μsec dead times incorporated. The delays have introduced a 5% fifth and seventh defeating the purpose of the PWM technique.

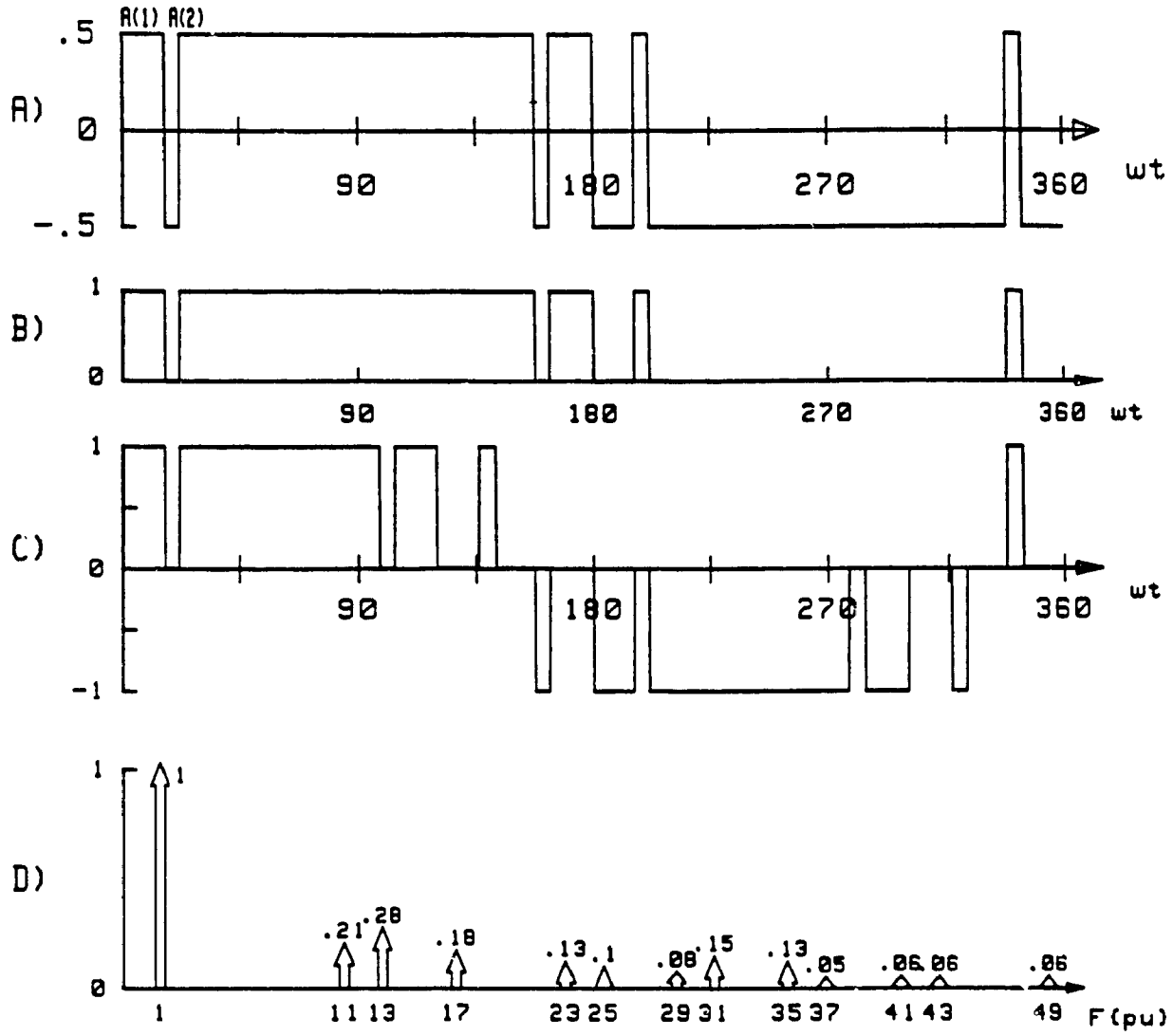


Figure F2.17 Programmed PWM sensitive to angle distortion
A) SHE line to neutral voltage waveform
B) Switch #1 gating signal GSW1
C) Line to line output voltage
D) Expected output line to line voltage spectrum

angle 1	=16.2 deg
angle 2	=22 deg
frequency	=400 hz
magnitude of 5th	= 5%
magnitude of 7th	= 5.3%
magnitude of 11th	= 27%
magnitude of 13th	= 30.7%

Table T2.2 Harmonic spectrum with 20usec deadtimes

2) When used in a variable input voltage situation;

A) Sophisticated control hardware is required to store and access the required large number of switching patterns;

B) Associated hardware becomes practical and cost effective only through VLSI implementation. The expertise required to design such hardware is not available to most small companies. Further, the number of units produced must be large enough to justify initial development costs.

Despite selected application drawbacks programmed techniques typically yield low THD. This has led to its wide spread use in many applications including fixed and variable supply converters. By far the most prominent of these techniques is Selective Harmonic Elimination (SHE).

2.4.2.1 Selective Harmonic Elimination (SHE)[28],[29]

SHE focuses on the direct elimination of undesired harmonics. The approach may not result in minimal THD as other programmed techniques do [30] yet it carries the added advantage of eliminating rather than minimizing unwanted low order harmonics. This feature is helpful in reducing the likelihood of harmonic amplification as a result of transient behavior. The technique essentially defines the AC TERM spectra based on a selected number

of switching angles. Figure F2.17C shows the general AC TERM waveform. The waveform is prescribed as having quarter wave symmetry requiring only the switching angles below 90° to completely describe the waveform. Fourier analysis of the waveform reveals a harmonic content of;

$$HAR_N = \frac{4}{N \cdot \Pi} \left[1 + 2 \sum_{K=1}^{KMAX} (-1)^k \, COS(N \cdot INTER(K)) \right] \qquad (2.12)$$

where KMAX = total # of angles from 0° to 90°

SHE can essentially be split into two categories; SHE converter operation with a regulated input supply and SHE converter operation with a non regulated supply.

2.4.2.1.1 SHE With Regulated Converter Input [28]

For regulated inputs the converter is free of modulation control. Consequently, only one PWM pattern need be established resulting in constant output ripple to be filtered. The required number of angles is directly proportional to the number of harmonics to be set to zero (plus an offset) by using equation 2.12. This in turn leads to the expression for converter switching frequency (turn off/switch) as;

$$SW_F = \left[2 \cdot KMAX + 1 \right] X \text{ base frequency} \qquad (2.13)$$

where base frequency = Converter AC TERM fundamental frequency

Therefore for a 3-ϕ inverter eliminating 5th, 7th, 11th and 13th harmonics the switching frequency would be 540hz and each switch turns off 9 times per

cycle. Figure F2.18 was developed to show the characteristics of the PWM scheme (for elimination of 5th, 7th, 11th, 13th and 17th) while table T2.3 lists the associated angles.

The nature of solving the simultaneous equations for this application is such that a good initial guess is required to ensure convergence. Consequently as the desired number of eliminated harmonics increases convergence is more difficult. Further, at some point convergence may occur yet the magnitude of the fundamental component may be substantially lower than required. Moreover when the order approaches 21 pu the computational time cost to solve the angles will be lengthy even for a mainframe. For these reasons no angles were solved for comparison with the carrier techniques. However when the switching frequency approaches 21 pu, an extra angle may be introduced which controls the magnitude of the fundamental. The switching frequency only marginally rises while the optimized angles are more easily extracted by the software. This approach is typically used for non regulated converter inputs and is described in chapter 2.4.2.i.2.

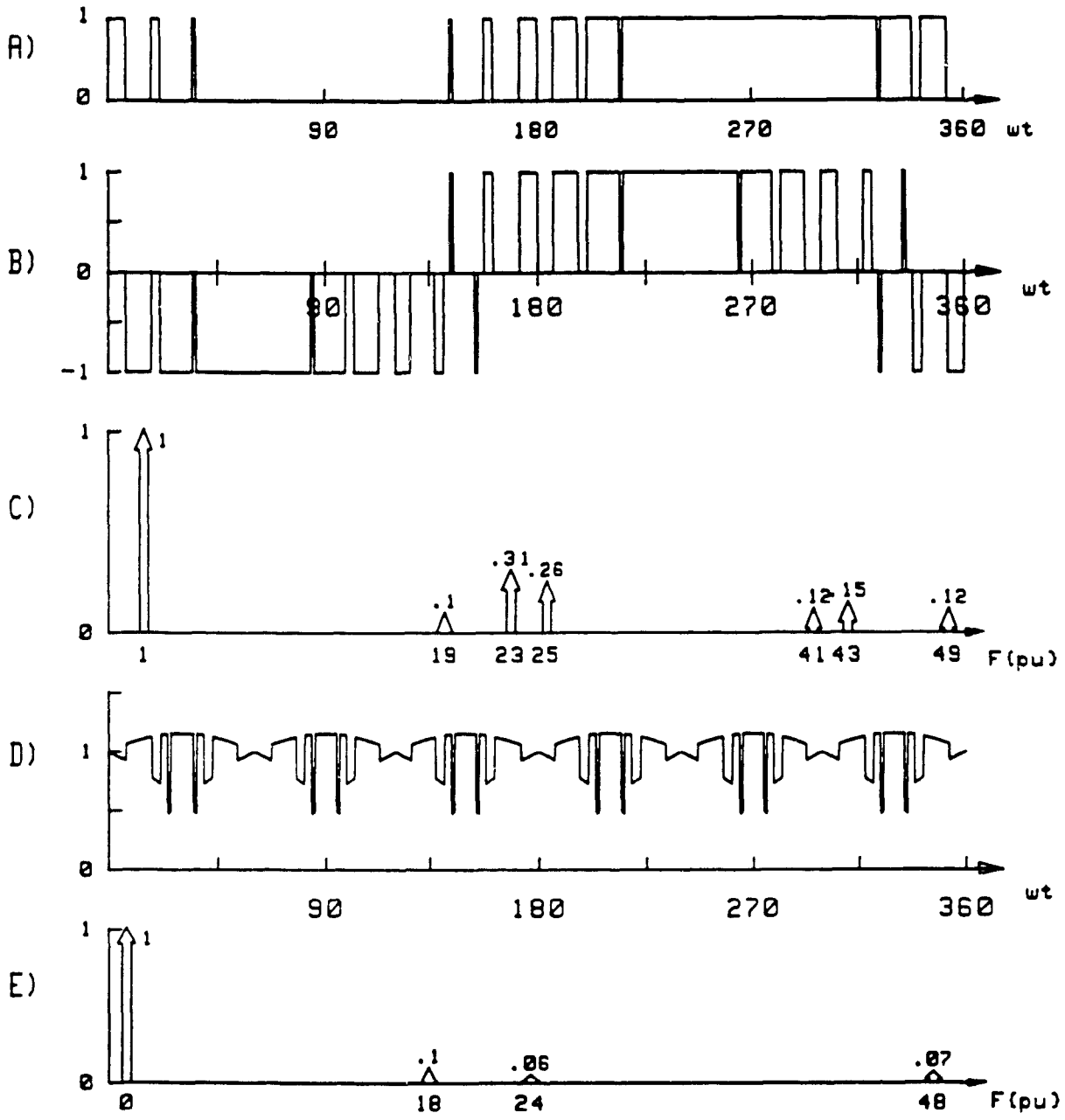


Figure F2.18 SHE PWM

A) SHE inverter switch #1 gating signal (GSW1)
B) AC TERM
C) AC TERM spectrum
D) DC TERM
E) DC TERM spectrum

INTER(1)	=	6.7952
INTER(2)	=	17.2962
INTER(3)	=	21.0252
INTER(4)	=	34.6566
INTER(5)	=	35.9840

Table T2.3 Five harmonic elimination angles

2.4.2.1.2 SHE with Unregulated Converter Input [29]

For unregulated supply applications the SHE scheme must control fundamental amplitude as well as suppress the prescribed harmonics. This requires an extra degree of freedom in the nonlinear matrix resulting in an added switching angle. As the number of suppressed harmonics increases the added degree of freedom becomes less significant. The expression added to the nonlinear matrix is of the form

$$HAR_1 = \frac{4}{\Pi}\left[1 + 2\sum_{K=1}^{KMAX}(-1)^K \cos(INTER(K))\right] \qquad (2.14)$$

The new expression for switching frequency is thus;

$$SW_F = \left[2 \cdot KMAX + 3\right] X \text{ base frequency} \qquad (2.15)$$

A 3-ϕ inverter with variable modulation control, eliminating the 5th, 7th, 11th, and 13th harmonics, operating at 60 hz would have a switching frequency of 660 hz. Each switch commutates 11 times/cycle.

Figure F2.19 shows the characteristics of SHE with switching stresses equal to that of the carrier techniques.

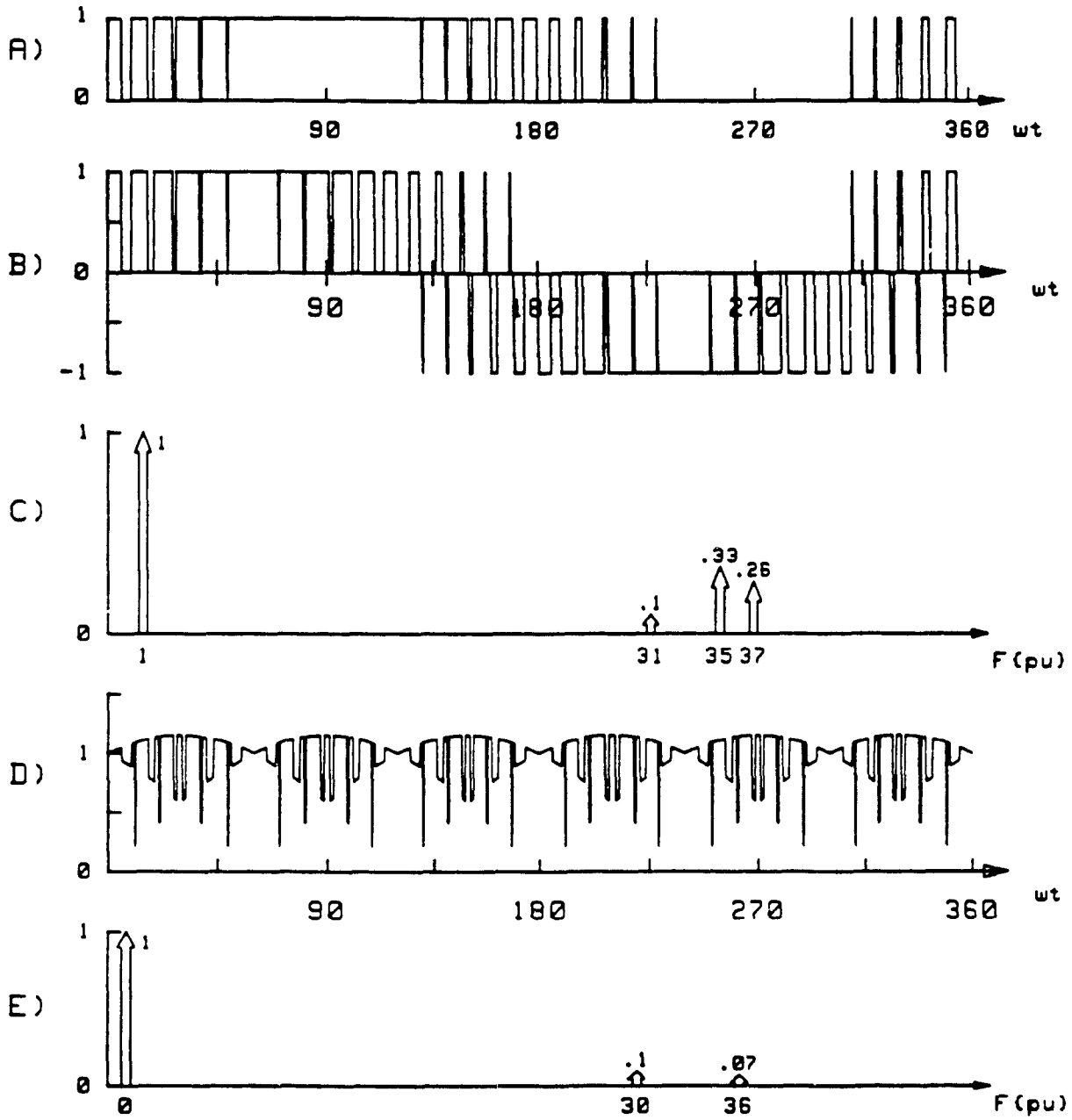


Figure F2.19 SHE characteristics

A) SHE switch #1 gating signal (GSW1)
B) AC TERM
C) AC TERM spectrum
D) DC TERM
E) DC TERM spectrum

Figure F2.20 shows the distortion factor values DF_1 , DF_2 and DF_3 as defined in chapter 2.4.1.5 for SHE with a switching frequency of 21pu as the modulation index is varied. Moreover, to emphasize input spectral content of this technique the quality indices used in chapter 2.4.1.5 are once again used here. The results are shown in figure F2.21.

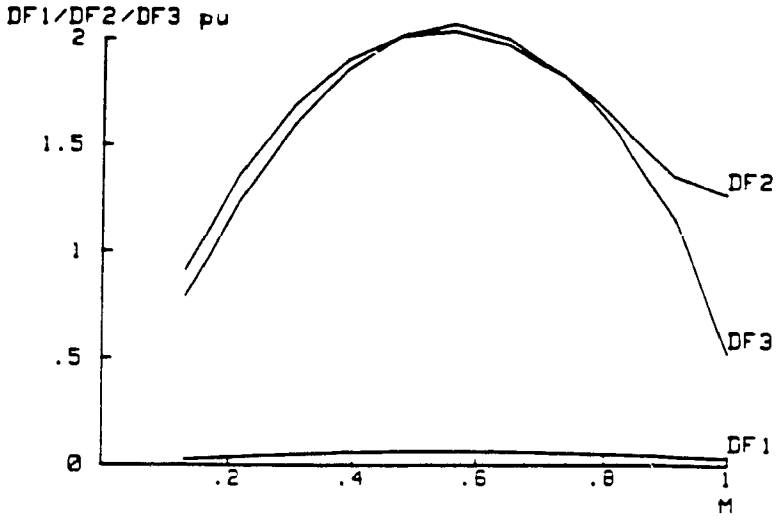


Figure F2.20 SHE distortion factor indices

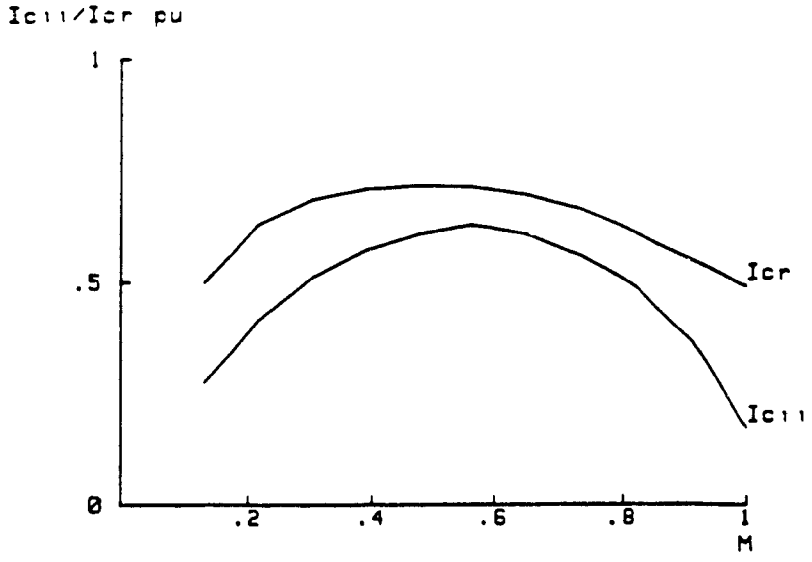


Figure F2.21 SHE input current quality factors

2.4.3 PWM Classification and Selection

For the meaningful interpretation of evaluation data, the switching frequency variable has been eliminated by using the same switching frequency for all PWM techniques. However, careful investigation of the MSPWM technique shows that for the same AC TERM and DC TERM waveforms, controlled rectifiers require lower switching frequencies than voltage source inverters. Because of this asymmetry this technique has been represented twice in figure F2.12, F2.13 and F2.14.

2.4.3.1 AC TERM and DC TERM Gain

Respective AC TERM and DC TERM gains for all 5 PWM techniques are summarized in Table T2.4. It is noted that these gain values are relatively independent of switching frequency and are directly proportional to the respective modulation index values M.

From Table T2.4 it is obvious with regards to AC/DC GAINS all improved PWM techniques are

A) better than the original sine technique

B) equivalent amongst themselves

TECHNIQUE	G_{AC}	G_{DC}
SPWM	.866	.750
MSPWM	1	.866
HIPWM(1st & 3rd)	1	.866
HIPWM(1st & 3rd & 9th)	1	.866
SHE	1	.866

Table T2.4 Maximum AC and DC TERM gain values (M =1)

2.4.3.2 Quality Factors

The variation of DF_1, DF_2, DF_3, I_{CII} and I_{CR} as a function of M show that;

A) For Voltage source inverter applications the SHE technique offers the best quality AC TERM waveforms.

B) For controlled rectification the MSPWM technique offers the combined best quality AC TERM and DC TERM waveforms.

C) For voltage sourced inverters that cover the entire modulation range, all advanced carrier techniques offer equal quality and superior input capacitor current ratings.

D) For VSI operating at unity modulation index, all advanced schemes are roughly equivalent for input capacitor rms current rating.

E) For controlled rectification, all advanced carrier PWM techniques offer equally improved input rms capacitor ratings vs. SPWM and SHE.

2.4.3.3 UPS Controlled Rectifier PWM Selection

The input supply to the controlled rectifier is unregulated. The expected modulation swing will be in the area of (from chapter 3.3)

$$.63 \leq M \leq 1$$

From this modulation swing figures F2.12, F2.13, F2.14, F2.15, F2.16, F2.20 and F2.21 reveal that the best PWM technique for the controlled rectification stage is MSPWM. If only output DC TERM waveforms were considered, then from figure F2.14 HIPWM would appear to be the optimum choice. However overall examination of the figures (in particular F2.12) shows a dramatic AC TERM advantage of MSPWM and consequently its overall selection.

2.4.3.4 Voltage Source Inverter PWM Selection

The VSI stage is supplied by a regulated input thus simplifying the output voltage control. The SHE PWM scheme requires simple logic to apply in this application. Moreover it offers better output distortion factor and lower quality factors. It is therefore justifiable that for VSI UPS applications with a pre regulated input, Selective Harmonic Elimination is the best choice.

2.5 Software Development

In order to facilitate research in the area of PWM converters two dedicated software routines were developed to speed up repeated data runs. The first routine is a worst case component ratings evaluation program while the second is an analysis/simulation program. The programs were written in Basic and operate on a HP desk top computer. Thorough documentation has been prepared to allow extension or modification of the programs at a later date.

2.5.1 UPS Inverter Worst Case Ratings Program

A program to evaluate component stresses is essential for proper converter investigation not only for implementation purposes but for comparative evaluation as well. The components must include input and output filters as well as semiconductors. Current, voltage, power and $\mu F/\mu H$ ratings should all be derived. The developed program was designed specifically for UPS regulated input inverter stages. Worst case operating points are derived over the range of load conditions. The program proves valuable for PWM comparison on the basis of converter stresses. Results are given in per unit ratings and in actual units based on a selected converter kVA rating. A complete program listing is provided in Appendix A.

2.5.1.1 Program Methodology

The methodology is based on the assumption that the generalized 3ϕ UPS inverter stage configuration of figure F2.22 is employed. This topology is chosen to reflect the proposed UPS inverter stage of chapter 2.3.1. Since the input is assumed regulated, its variation with respect to load changes poses no direct concern in terms of inverter modulation changes.

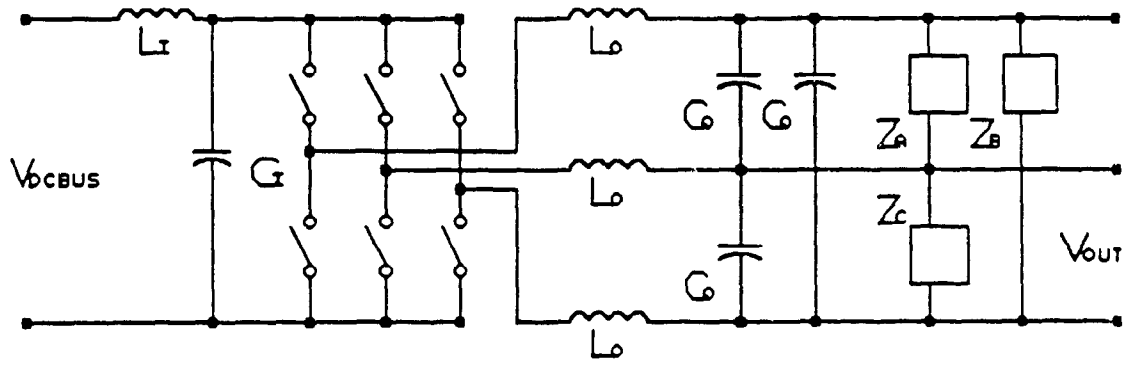


Figure F2.22 Worst case ratings inverter stage generalized structure

The software uses frequency domain and time domain analysis to return the component ratings based on the user defined switching conditions of the inverter semiconductors and load power factor range. The switching strategy may be selected from a menu of PWM techniques or user defined before program operation. The program can be segregated into three distinct stages;

A) Derivation of worst case per unit component ratings based on user selected PWM.

B) Actual component ratings based on user selected converter power rating.

C) Example set of waveforms based on user selected load power factor.

2.5.1.2 Derivation of Worst Case Per Unit Component Ratings

Based on the desired PWM technique the program evaluates the following ratings;

Output filter;	inductance impedance	XLO
	inductance current	ILORMS
	inductance voltage	VLORMS
	inductance power	LOVA
	capacitance impedance	XCO
	capacitive current	ICORMS
	capacitive voltage	VCORMS
	capacitive power	COVA
Switching bridge;	average switch current	ISWAVE
	rms switch current	ISWRMS
Input filter;	inductance impedance	XLI
	inductance current	ILIRMS
	inductance voltage	VLIRMS
	inductance power	LIVA
	capacitance impedance	XCI
	capacitive current	ICIRMS
	capacitive voltage	VCIRMS
	capacitive power	CIVA
DC bulk voltage swing	maximum bus voltage	VDCBUSMAX
	minimum bus voltage	VDCBUSMIN

The equations and derivations of each of these variables are detailed in chapter 3.1 and will not be duplicated here. However the results are based on the following preset data which the user may wish to alter should the occasion be called for;

-Output power factor	.7 lag to .7 lead
-Output filter THD	≤5%
-Max. individual harmonic	≤2% @ pf=1
-Output filter damping factor	=.707 @ pf=1
-Input filter inductor current THD	≤10%
-Input filter capacitor voltage THD	≤5%

A flowchart summarizing the software stages is shown in figure F2.23.

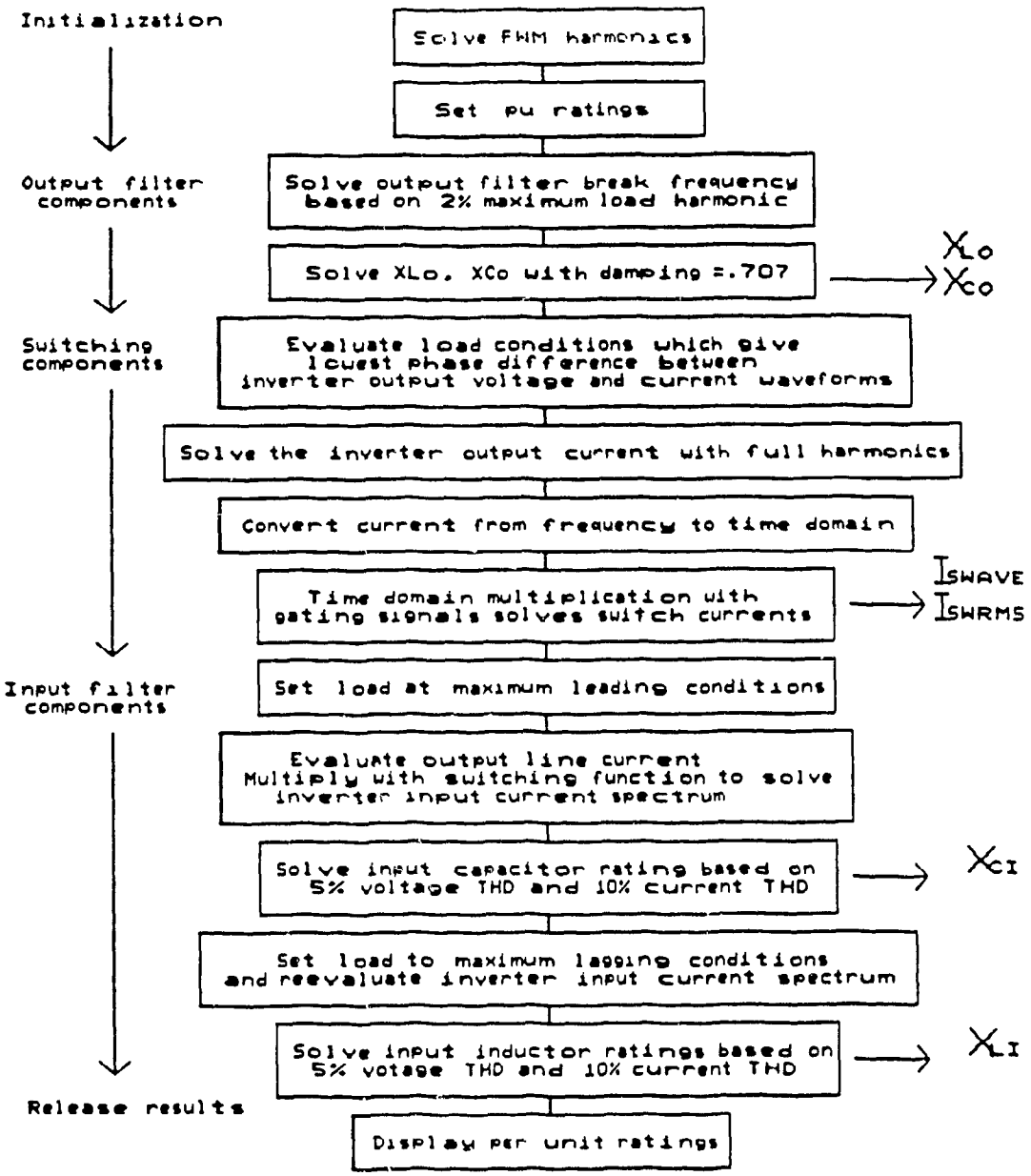


Figure F2.23 Inverter worst case per unit ratings flowchart

After converting the PWM gating signals into its frequency domain and time domain representative transfer function characteristics, the per unit

references are set. These include;

Output V_{L-N} =1pu peak

Load Z_{L-N} =1pu

Power P_{TOTAL} =1.5pu

To solve the output filter requirements, the software sifts through the frequency components of the output voltage locating the dominant harmonic and setting the output filter break frequency accordingly. Using an industry standard load damping factor of .707, X_{LO} and Xco are solved.

The worst case switch current ratings are found when the inverter output line current and the line to fictitious load neutral voltage are in phase. With the derivedoutput filter components inserted, the load is numerically filtered until the fundamental components of these waveforms are either in phase or as close as possible due to load swing and output filter limits. Inverter output current is solved with this load and filter condition in the frequency domain and then converted to the time domain by harmonic summation. This time domain representation is finally multiplied with the time domain representation of the inverter switching PWM function leading to the average and rms switch currents.

The worst case input filter ratings require two basic loop passes since the worst case for each filter component is at different load power factors. First the load is adjusted to ./ leading, line currents are solved and reflected via the inverter transfer function to the primary where the worst case capacitor rating X_{CI} can be solved using a nonlinear optimization subroutine. Finally, resetting the load to .7 lagging the process is repeated for input filter inductor X_{LI}.

2.5.1.3 Actual Component Ratings

With the completion of worst case per unit ratings, the program displays the resulting data and prompts the user with a *'PRINTOUT AND/OR PROCEED'* INSTRUCTION. After a data printout (if desired) is obtained the user is prompted for an inverter power rating. Actual component ratings are then deduced by the programs scaling as;

$$V_{L-N} = 115\sqrt{2}$$

$$kVA = kVA \text{ (user input)} \tag{2.16}$$

$$I_{SCALE} = kVA \cdot 6.66/V_{L-N} \tag{2.17}$$

$$V_{SCALE} = V_{L-N} \tag{2.18}$$

$$Z_{SCALE} = \frac{3 \cdot 4^2}{2000 \cdot kV_A} \tag{2.19}$$

2.5.1.4 Test Point Data and Waveforms

As a final stage the program prompts the user for a test point load condition and solves selected resulting waveforms and data such as component currents and THD. This allows visual inspection and comparison with worst case results confirming the software calculations.

2.5.1.5 Example Operation

The underlying complexity of the system of equations (theoretical derivations of section 3.1) vanishes upon use of the program. Table T2.5 shows the resulting program printout of per unit calculations for Selective Harmonic Elimination of 5th and 7th harmonics.

Inverter worst case pu ratings

OUTPUT VOLTAGE=1pu PEAK
OUTPUT VA =1.5pu
OUTPUT CURRENT=1pu PEAK
LOAD IMPEDENCE=1pu/phase Y connection

DC BUS VOLTAGE SWINGS FROM 1.53 pu TO 1.93 pu
AVERAGE SWITCH CURRENT= .301 pu

INPUT FILTER		
IND= .039 pu	Irms= .871 pu	Vrms= .046 pu
CAP= 6.146 pu	Irms= .265 pu	Vrms= 1.93 pu
OUTPUT FILTER		
IND= .164 pu	Irms= .751 pu	Vrms= .434 pu
CAP= 12.194 pu	Irms= .087 pu	Vrms= .707 pu

Table T2.5 Worst case inverter per unit ratings for SHE example

To scale the inverter stage for 115 V_{L-N} output as proposed (figure F2.5 section 2.3.1) a power rating input is required. After the test point load power factor is entered the operational waveforms are drawn. In figure F2.24 the software derived waveforms for the example of table T2.5 are shown with a converter power rating of 10 kVA and a load power factor of .7 lagging. The results clearly and quickly show the quality of a PWM technique when operating on the proposed inverter stage.

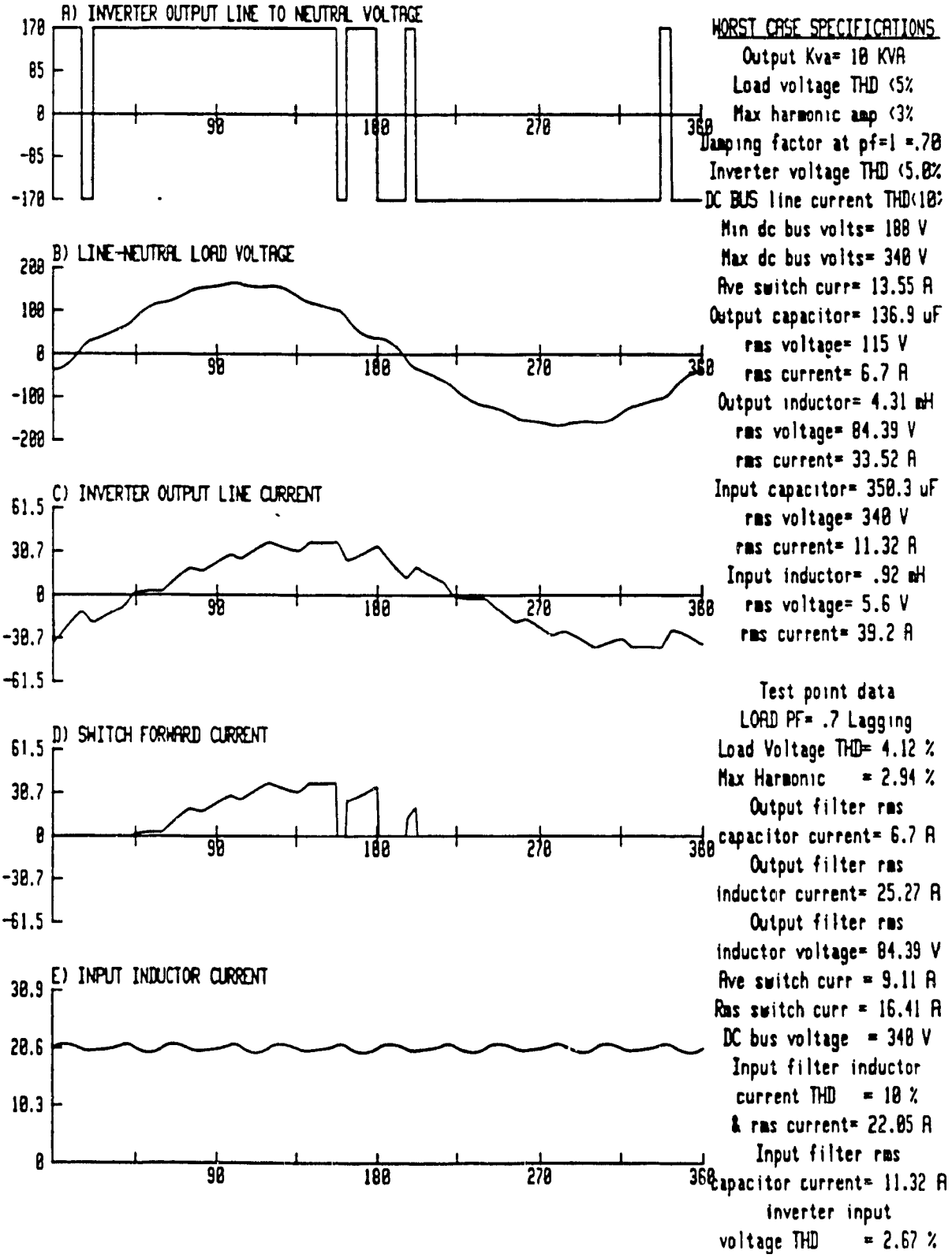


Figure F2.24 Worst case inverter ratings waveforms for SHE example

2.5.2 An Analysis/Simulation Program For Power Electronic Circuits [3]

Modern power converters typically featurePWM techniques and nonlinear region semiconductor operation. Although numerous general circuit analysis programs are available [31], [32], [33], [34], [35], [36], [37], [38], [39] only one has been developed with both of these characteristics taken in to consideration [36]. References [31],[32],[33],[34],[35],[39] all either use SPICE for simulation or are SPICE clones. Although ideal switches may usually be modeled, spice based programs have several drawbacks including the lack of simplified PWM facilities. Since fully controlled rectifiers and inverters utilize PWM, these software packages are either inappropriate or involve substantial time to employ.

Reference [36] (AUTOSEC 5) alleviates this problem by allowing for a simple user interface with a variety of voltage supply waveforms. However the introduction of simplified PWM facilities here is associated with the following further shortcomings;

A) All ideal switches must be accompanied by a resistor/capacitor snubber circuit. Since fully controlled UPS similar to the one proposed in chapter 2.3.1 have at least 13 controlled semiconductors the circuit complexity substantially increases.

B) No capacitor loop or inductor cutset can successfully be analyzed until further components are added to eliminate the loop or cutset. This further increases complexity of the UPS since such loops exist in standard filtering arrangements.

C) Downgrade of user friendliness.

In contrast to existing programs, the program developed by the author overcomes these disadvantages and is also extremely user friendly. The user

simply constructs the power converter on the screen, inputs component values, creates or selects a PWM scheme from a menu and allows the program to solve the output waveforms. The switching function concept [40] is used to convert the nonlinear system into a linear system. Results are obtained using state space analysis.

2.5.2.1 Program Methodology

The program can be roughly divided into three sections; input, processing and output.

The input section utilizes a schematic capture type data entry section that is extremely user friendly. The circuit under simulation is entered and displayed on the CRT (as shown in figure F2.25) by using a rotary knob or pre defined function keys. The circuit elements represented by softkeys include; dc/ac voltage and current sources, resistors, capacitors, inductors, switches, single and three phase converter structures, and connecting lines. Additional graphic features designed to enhance circuit illustrations and labelling include; arrows, loops, circles, squares, etc. The circuit values are entered interactively. The program searches through the drawn circuit and prompts for the respective component values. Pre-programmed customized voltage and/or current sources are entered by using their binary file names. This includes a variety of preprogrammed PWM techniques or user entered techniques. A complete analysis of the user friendly input section is presented by the author in [62].

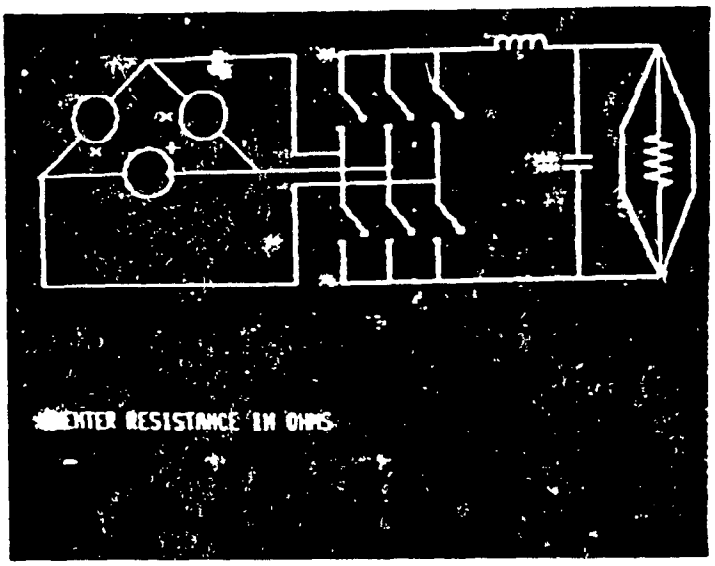


Figure F2.25 Typical screen display of entered circuit

The processing section incorporates a number of powerful subroutines. The objective is to employ time domain state space analysis techniques because of its compatibility with digital computers to simulate power electronic circuits.

Assuming ideal switching conditions, switch configurations typically found in UPS and other power electronic circuits are often described as a single block element that offers a particular transfer function. This essentially combines a linear source with nonlinear elements resulting in a linear time domain representation of a linear voltage or current source. PWM techniques define switch configuration transfer functions [41]. Figure F2.26 shows the piecewise linear voltage source modeled from the full bridge switch configuration. In this fashion nonlinear switch configurations can be eliminated from the analysis thus simplifying and hastening the output results. In fact, the resulting state matrix will have its order reduced by

roughly 66% over PSPICE. Consequently the execution speed of the program is increased.

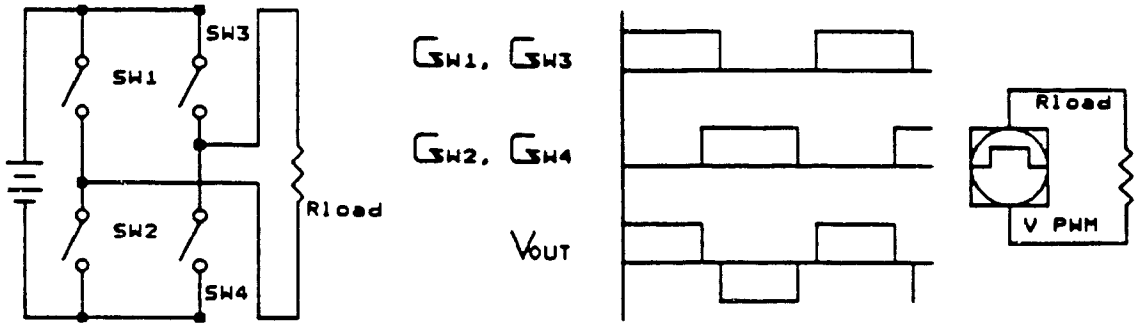


Figure F2.26 Modeling of a Single Phase PWM Inverter

From the circuit diagram drawn on CRT the program constructs the respective circuit 'tree' by using established principles of linear graph and circuit analysis theory [42]. Accordingly all voltage sources and as many capacitors as possible become 'twigs' while current sources and as many inductors as possible become 'links'. Resistors may be either 'links' of 'twigs'.

From the circuit tree, the fundamental cut-set matrix is formed and subdivided as

$$
Q_L = \begin{array}{c} \\ \text{twigs} \end{array}
\begin{array}{c}
\begin{array}{cccc} \multicolumn{4}{c}{\text{links}} \\ C & R & L & J \end{array} \\
\begin{array}{c} E \\ C \\ R \\ L \end{array}
\begin{bmatrix}
Q_{EC} & Q_{ER} & Q_{EL} & Q_{EJ} \\
Q_{CC} & Q_{CR} & Q_{CL} & Q_{CJ} \\
0 & Q_{RR} & Q_{RL} & Q_{RJ} \\
0 & 0 & Q_{LL} & Q_{LJ}
\end{bmatrix}
\end{array}
\qquad (2.20)
$$

Also matrices Ct, Cl, Lt, Ll, Gt, Gl, Rt, Rl, $\mathcal{Y}$, $\hat{\mathcal{Y}}$, $\mathcal{F}$, $\hat{\mathcal{F}}$, $\mathcal{H}$, $\hat{\mathcal{H}}$, $\mathcal{G}$, $\hat{\mathcal{G}}$, $\mathcal{C}$, $\hat{\mathcal{C}}$, $\mathcal{L}$, $\hat{\mathcal{L}}$, R and G are formed where;

Ct = Capacitor twig diagonal matrix

Cl = Capacitor link diagonal matrix

Lt = Inductor twig matrix

Ll = Inductor link matrix

Gt = Conductance twig diagonal matrix

Gl = Conductance link diagonal matrix

Rt = Resistive twig diagonal matrix

Rl = Resistive link diagonal matrix

$$\mathcal{Y} = Q_{CR}R^{-1}Q_{CR}^{T} \tag{2.21}$$

$$\hat{\mathcal{Y}} = Q_{CR}R^{-1}Q_{ER}^{T} \tag{2.22}$$

$$\mathcal{F} = Q_{RL}^{T}G^{-1}Q_{RL} \tag{2.23}$$

$$\hat{\mathcal{F}} = Q_{RL}^{T}G^{-1}Q_{RJ} \tag{2.24}$$

$$\mathcal{H} = -Q_{CL}+Q_{CR}R^{-1}Q_{RR}^{T}RtQ_{RL} \tag{2.25}$$

$$\hat{\mathcal{H}} = -Q_{CJ}+Q_{CR}R^{-1}Q_{RR}^{T}RtQ_{RJ} \tag{2.26}$$

$$\mathcal{G} = Q_{CL}^{T}-Q_{RL}^{T}G^{-1}Q_{RR}GlQ_{CR}^{T} \tag{2.27}$$

$$\hat{\mathcal{G}} = Q_{EL}^{T}-Q_{RL}^{T}G^{-1}Q_{RR}GlQ_{ER}^{T} \tag{2.28}$$

$$\mathcal{C} = Ct+Q_{CC}ClQ_{CC}^{T} \tag{2.29}$$

$$\hat{\mathcal{C}} = -Q_{CC}ClQ_{EC}^{T} \tag{2.30}$$

$$\mathcal{L} = Lll+Q_{LL}^{T}LttQ_{LL} \tag{2.31}$$

$$\hat{\mathcal{L}} = -Q_{LL}^{T}LttQ_{LJ} \tag{2.32}$$

$$R = Rl+Q_{RR}^{T}RtQ_{RR} \tag{2.33}$$

$$G = Gt+Q_{RR}GlQ_{RR}^{T} \tag{2.34}$$

From these matrices data manipulation is used to formulate the standard continuous time state space matrix

$$\frac{dx}{dt} = \mathcal{A}x + \mathcal{B}_1 u + \mathcal{B}_2 \frac{du}{dt} \tag{2.35}$$

where;

$$\mathcal{A} = \begin{bmatrix} \mathcal{C}^{-1} & 0 \\ 0 & \mathcal{L}^{-1} \end{bmatrix} \begin{bmatrix} -\mathcal{Y} & \mathcal{H} \\ \mathcal{G} & -\mathcal{F} \end{bmatrix} \tag{2.36}$$

$$\mathcal{B}_1 = \begin{bmatrix} \mathcal{C}^{-1} & 0 \\ 0 & \mathcal{L}^{-1} \end{bmatrix} \begin{bmatrix} -\hat{\mathcal{Y}} & \hat{\mathcal{H}} \\ \hat{\mathcal{G}} & -\hat{\mathcal{F}} \end{bmatrix} \tag{2.37}$$

$$\mathcal{B}_2 = \begin{bmatrix} \mathcal{C}^{-1} & 0 \\ 0 & \mathcal{L}^{-1} \end{bmatrix} \begin{bmatrix} \hat{\mathcal{C}} & 0 \\ 0 & \hat{\mathcal{L}} \end{bmatrix} \tag{2.38}$$

Equation 2.38 suggests that $\mathcal{B}_2 = [0]$ if $\hat{\mathcal{C}} = [0]$ and $\hat{\mathcal{L}} = [0]$. Such is the case when the system is causal and no capacitor loop or inductor cut set exists. In such a case equation 2.35 becomes

$$\frac{dx}{dt} = \mathcal{A}x + \mathcal{B}_1 u \tag{2.39}$$

and the output equation is given as

$$\mathcal{W} = Cx + Du \tag{2.40}$$

The outputs are obtained by implementing in the circuit, transparent to the user, voltage and current sources of zero value. Without affecting the circuit electrically these sources can be used to monitor currents and voltages respectively. These sources labelled

$$\left[Eo\right] \;\&\; \left[Jo\right]$$

respectively are merged with the existing sources

$$\left[E\right] \;\&\; \left[J\right]$$

in the fundamental cut set link matrix. The output vector $\mathcal{W}$ is then defined as

$$\mathcal{W} = \begin{bmatrix} I_{Eo} \\ V_{Jo} \end{bmatrix} \tag{2.41}$$

Utilizing standard linear graph theory [42] the following equation can be obtained;

$$I_E = -Q_{EC}I_{C1} - Q_{ER}I_{R1} - Q_{EL}I_{L1} - Q_{EJ}I_J \tag{2.42}$$

Since

$$I_{C1} = C1\frac{d}{dt}V_{C1} = C1Q_{EC}^T\frac{d}{dt}V_E + C1Q_{CC}^T\frac{d}{dt}V_{Ct} \tag{2.43}$$

and

$$I_{R1} = R^{-1}(Q_{CR}^T V_{CT} + Q_{ER}^T V_E - Q_{RR}^T Rt(Q_{RL}I_{L1} + Q_{RJ}I_J)) \tag{2.44}$$

we have by substituting 2.43 and 2.44 into 2.42

$$I_E = -Q_{EC}C1Q_{EC}^T\frac{d}{dt}V_E - Q_{EC}C1Q_{CC}^T\frac{d}{dt}V_{Ct} - Q_{ER}R^{-1}Q_{CR}^T V_{CT} -$$

$$Q_{ER}R^{-1}Q_{ER}^T V_E + Q_{ER}R^{-1}Q_{RR}^T RtQ_{R1}I_{L1} + Q_{ER}R^{-1}Q_{RR}^T RtQ_{RJ}I_J - Q_{EL}I_{L1} - Q_{EJ}I_J \tag{2.45}$$

Assuming no source derivatives will exist. (ie $\frac{d}{dt}V_E = 0$)
Sifting only the zero value voltage sources out we have

$$I_{Fo} = -Q_{EoC}C1Q_{CC}^T\frac{d}{dt}V_{Ct} - Q_{EoR}R^{-1}Q_{CR}^T V_{CT} -$$

$$Q_{EoR}R^{-1}Q_{EoR}^T V_E + Q_{EoR}R^{-1}Q_{RR}^T RtQ_{R1}I_{L1} + Q_{EoR}R^{-1}Q_{RR}^T RtQ_{RJ}I_J - Q_{EoL}I_{L1} - Q_{EoJ}I_J \tag{2.46}$$

Similarly we can derive the output expression for V_{Jo} as;

$$V_J = Q_{EJ}^T V_E + Q_{CJ}^T V_{Ct} + Q_{RJ}^T V_{Rt} + Q_{LJ}^T V_{Lt} \tag{2.47}$$

Since $V_{Lt} = Lt\frac{d}{dt}I_{Lt} = -LtQ_{LL}\frac{d}{dt}I_{L1} - LtQ_{LJ}\frac{d}{dt}I_J$ (2.48)

and $$V_{Rt} = -G^{-1}(Q_{RL}I_{L1} + Q_{RJ}I_J + Q_{RR}G1(Q_{CR}^T V_{Ct} + Q_{ER}^T V_E)) \quad (2.49)$$

we have by substituting 2.48 and 2.49 into 2.47

$$V_J = Q_{EJ}^T V_E + Q_{CJ}^T V_{Ct} - Q_{RJ}^T G^{-1} Q_{RL} I_{L1} - Q_{RJ}^T G^{-1} Q_{RJ} I_J - Q_{RJ}^T G^{-1} Q_{RR} G1 Q_{CR}^T V_{Ct} -$$

$$Q_{RJ}^T G^{-1} Q_{RR} G1 Q_{ER}^T V_E - Q_{LJ}^T Lt Q_{LL} \frac{d}{dt} I_{L1} - Q_{LJ}^T Lt Q_{LJ} \frac{d}{dt} I_J \quad (2.50)$$

Finally V_{Jo} can be sifted from all voltage sources as;

$$V_{Jo} = Q_{EJo}^T V_E + Q_{CJo}^T V_{Ct} - Q_{RJo}^T G^{-1} Q_{RL} I_{L1} - Q_{RJo}^T G^{-1} Q_{RJo} I_J - Q_{RJo}^T G^{-1} Q_{RR} G1 Q_{CR}^T V_{Ct} -$$

$$Q_{RJo}^T G^{-1} Q_{RR} G1 Q_{ER}^T V_E - Q_{LJo}^T Lt Q_{LL} \frac{d}{dt} I_{L1} \quad (2.51)$$

Equations 2.51 and 2.45 can be combined into matrix form as

$$\begin{bmatrix} I_{Eo} \\ V_{Jo} \end{bmatrix} = \begin{bmatrix} -Q_{EoC} C1 Q_{CC}^T & 0 \\ 0 & -Q_{LJo}^T Lt Q_{LL} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} V_{Ct} \\ I_{L1} \end{bmatrix} +$$

$$\begin{bmatrix} -Q_{EoR} R^{-1} Q_{CR}^T & Q_{EoR} R^{-1} Q_{RR}^T Rt Q_{RL} - Q_{EoL} \\ Q_{CJo}^T - Q_{RJo}^T G^{-1} Q_{RR} G1 Q_{CR}^T & -Q_{RJo}^T G^{-1} Q_{RL} \end{bmatrix} \begin{bmatrix} V_{Ct} \\ I_{L1} \end{bmatrix} +$$

$$\begin{bmatrix} -Q_{EoR} R^{-1} Q_{ER}^T & Q_{EoR} R^{-1} Q_{RR}^T Rt Q_{RJ} - Q_{EoJ} \\ Q_{EJo}^T - Q_{RJo}^T G^{-1} Q_{RR} G1 Q_{ER}^T & -Q_{RJo}^T G^{-1} Q_{RJo} \end{bmatrix} \begin{bmatrix} V_E \\ I_J \end{bmatrix} \quad (2.52)$$

After substitution of equation 2.39 where

$$X = \begin{bmatrix} V_{Ct} \\ I_{Ct} \end{bmatrix} \quad (2.53)$$

we obtain

$$\begin{bmatrix} I_{Eo} \\ V_{Jo} \end{bmatrix} = \left[\begin{bmatrix} -Q_{EoC} C_1 Q_{CC}^T & 0 \\ 0 & -Q_{LJo}^T L_t Q_{LL} \end{bmatrix} \begin{bmatrix} \mathcal{A} \end{bmatrix} + \begin{bmatrix} -Q_{EoR} R^{-1} Q_{CR}^T & Q_{EoR} R^{-1} Q_{RR}^T R_t Q_{RL} - Q_{EoL} \\ Q_{CJo}^T - Q_{RJo}^T G^{-1} Q_{RR} G_1 Q_{CR}^T & -Q_{RJo}^T G^{-1} Q_{RL} \end{bmatrix} \right] \begin{bmatrix} V_{Ct} \\ I_{L1} \end{bmatrix} +$$

$$\left[\begin{bmatrix} -Q_{EoC} C_1 Q_{CC}^T & 0 \\ 0 & -Q_{LJo}^T L_t Q_{LL} \end{bmatrix} \begin{bmatrix} \mathcal{B}_1 \end{bmatrix} + \begin{bmatrix} -Q_{EoR} R^{-1} Q_{EoR}^T & Q_{EoR} R^{-1} Q_{RR}^T R_t Q_{RJ} - Q_{EoJ} \\ Q_{EJo}^T - Q_{RJo}^T G^{-1} Q_{RR} G_1 Q_{ER}^T & -Q_{RJo}^T G^{-1} Q_{RJo} \end{bmatrix} \right] \begin{bmatrix} V_E \\ I_J \end{bmatrix} \tag{2.54}$$

Substituting into equation 2.41 we obtain

$$\mathcal{W} = Cx + Du \quad \text{where}$$

$$C = \left[\begin{bmatrix} \alpha & 0 \\ 0 & \beta \end{bmatrix} \begin{bmatrix} \mathcal{A} \end{bmatrix} + \begin{bmatrix} -X_1 & X_2 \\ X_3 & -X_4 \end{bmatrix} \right] \tag{2.55}$$

$$D = \left[\begin{bmatrix} \alpha & 0 \\ 0 & \beta \end{bmatrix} \begin{bmatrix} \mathcal{B}_1 \end{bmatrix} + \begin{bmatrix} -X_5 & X_6 \\ X_7 & -X_8 \end{bmatrix} \right] \tag{2.56}$$

$$\alpha = -Q_{EoC} C_1 Q_{CC}^T \tag{2.57}$$

$$\beta = -Q_{LJo}^T L_t Q_{LL} \tag{2.58}$$

$$X_1 = Q_{EoR} R^{-1} Q_{CR}^T \tag{2.59}$$

$$X_2 = Q_{EoR} R^{-1} Q_{RR}^T R_t Q_{RL} - Q_{EoL} \tag{2.60}$$

$$X_3 = Q_{CJo}^T - Q_{RJo}^T G^{-1} Q_{RR} G_1 Q_{CR}^T \tag{2.61}$$

$$X_4 = Q_{RJo}^T G^{-1} Q_{RL} \tag{2.62}$$

$$X_5 = Q_{EoR} R^{-1} Q_{EoR}^T \tag{2.63}$$

$$X_6 = Q_{EoR} R^{-1} Q_{RR}^T R_t Q_{RJ} - Q_{EoJ} \tag{2.64}$$

$$X_7 = Q_{EJo}^T - Q_{RJo}^T G^{-1} Q_{RR} G_1 Q_{ER}^T \tag{2.65}$$

$$X_8 = Q_{RJo}^T G^{-1} Q_{RJo} \tag{2.66}$$

A unique feature of this program is that it can handle capacitor loops and/or inductor cut sets. This feature frees the user from requiring additional components (such as series and shunt resistors) to eliminate unavoidable loops and cut sets. The restriction resulting from the presence of such circuit conditions is that only the readily available state variables (i.e. capacitor twig voltages and inductor link currents) are used as outputs. Equation 2.35 keeps its expanded form and a coordinate transformation is used to simplify computation. Letting

$$x' = x - \mathcal{B}_2 u \tag{2.67}$$

we also obtain $$\frac{d}{dt} x' = \frac{d}{dt} x - \mathcal{B}_2 \frac{d}{dt} u \tag{2.68}$$

which after substitution into 2.35 leaves

$$\frac{d}{dt} x' = \mathcal{A}(x' + \mathcal{B}_2 u) + \mathcal{B}_1 u \tag{2.69}$$

or

$$\frac{d}{dt} x' = \mathcal{A}' x' + \mathcal{B}' u \tag{2.70}$$

where $$\mathcal{A}' = \mathcal{A} \tag{2.71}$$

$$\mathcal{B}' = (\mathcal{A}\mathcal{B}_2 + \mathcal{B}_1) \tag{2.72}$$

The traditional output equation for this state space equation is

$$W = Cx + D_1 u + D_2 \frac{d}{dt} u \tag{2.73}$$

however by allowing only the state variables as obtainable outputs

$D_1 = 0$ and $D_2 = 0$ leaving

$$W = Cx \tag{2.74}$$

or after coordinate transformation

$$W = C(x' + \mathcal{B}_2 u) \tag{2.75}$$

or

$$W = C'x' + D'u \tag{2.76}$$

where

$$C' = C \tag{2.77}$$

$$D' = C\mathcal{B}_2 \tag{2.78}$$

The state space equation is solved through the discretization of the continuous time system as detailed in reference [43]. This reference dictates that a continuous time system represented by equation 2.35 can be converted to an equivalent discrete time system represented as;

$$x[(k+1)T] = F(T)x(kT) + G(T)u(KT) \tag{2.79}$$

where

k =Discrete time instance

T =Sampling rate

$F(T) = \exp(\mathcal{A}T)$

$G(T) = \int_0^T \exp(\mathcal{A}\tau)\mathcal{B}_z d\tau$

$\mathcal{B}_z$ =Representative $\mathcal{B}'$or $\mathcal{B}_1$ (whichever applies)

To simplify computation of $\exp(\mathcal{A}T)$ and avoid complex, time consuming diagonalization, a simplistic truncated power series is used. Since

$$\exp(x) = \sum_{m=0}^{\infty} \frac{x^m}{m!} \tag{2.80}$$

we have

$$F(T)=\exp(\mathcal{A}T) = \sum_{m=0}^{\infty} \frac{(\mathcal{A}T)^m}{m!} \tag{2.81}$$

and

$$G(T)=\mathcal{A}^{-1}\exp(\mathcal{A}\tau)\mathcal{B}_Z\Big|_0^T=\mathcal{A}^{-1}\exp(\mathcal{A}T)\mathcal{B}_Z-\mathcal{A}^{-1}\mathcal{B}_Z$$

$$= \mathcal{A}^{-1}\left[\sum_{m=0}^{\infty}\frac{(\mathcal{A}T)^m}{m!}-1\right]\mathcal{B} \qquad (2.82)$$

The possibility of catastrophic cancellation or truncation is not a significant problem since the HP computer used has 64 bit floating point operation offering roughly 15 bits of accuracy. The number used limiting the expansion is "6" which proved sufficient in most examples tested.

At this stage point by point iteration is used on the state space output equation yielding a time domain waveform of the desired voltages and currents. The results are stored in pre-defined arrays.

The output section is designed to be no less user friendly than the input section. Multiple waveforms can be displayed on the screen with user specified magnifications, offsets and numerous mathematical manipulation facilities. Zoom features allow precise visualization of quick transient behavior and circuit design or PWM quality. Hard copies and waveform disk storage is also a necessary and implemented feature. Figure F2.27 displays typical output waveforms showing the programs effectiveness.

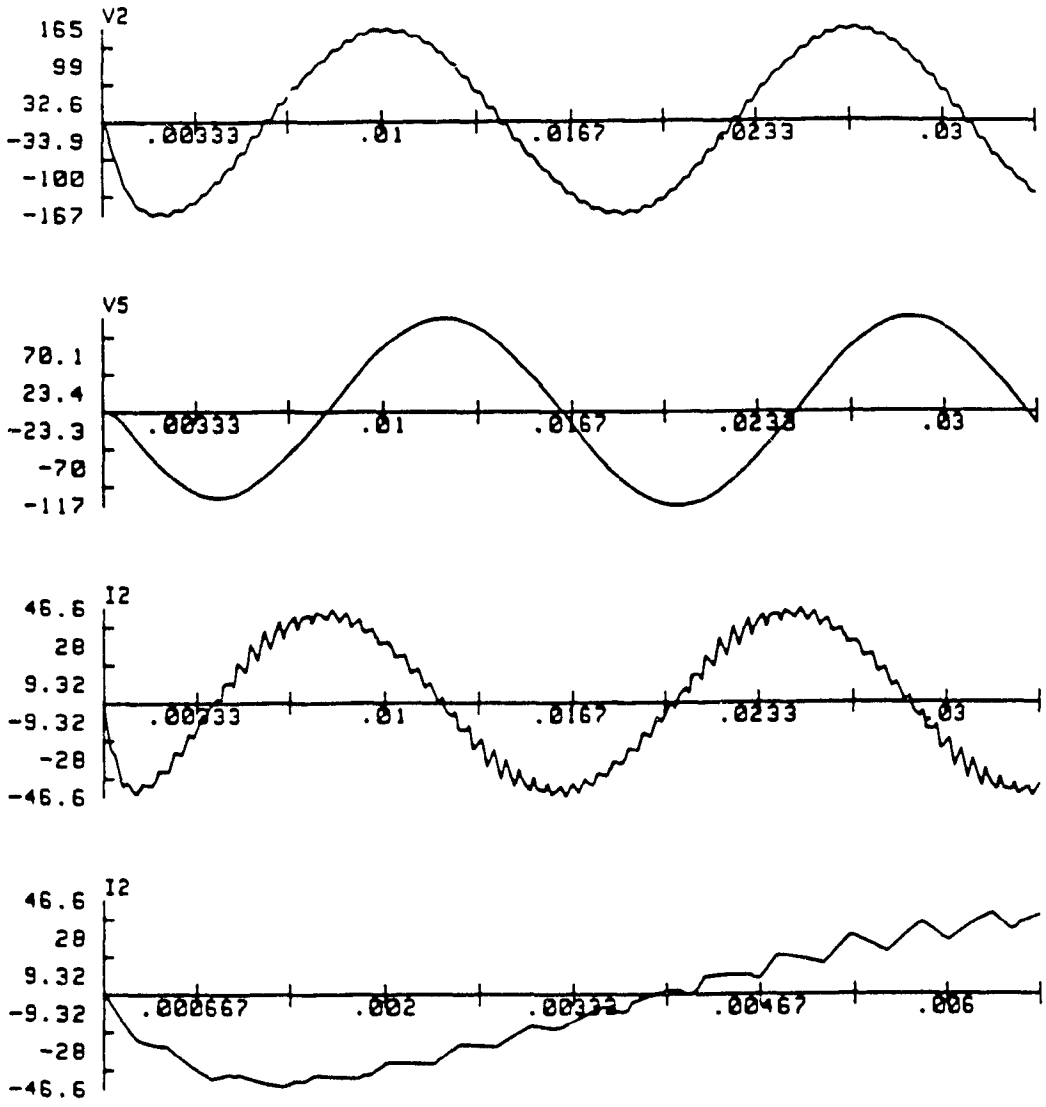


Figure F2.27 Analysis/Simulation program typical output waveforms

2.6 Conclusion

Typical medium power UPS systems have been shown to only partially solve the concerns of modern consumer. Expansion of sophisticated electronics into all faucets of commercial enterprise, combined with power critical manufacturing processes have handicapped the typical 4th generation UPS. The construction of a modern specifications table not only confirms this but leads to the derivation of a novel high performance topology to meet the high

standards.

The topology is less than optimal without its most compatible PWM technique. Arbitrary application of a PWM technique may lead to unoptimalresults. Based on the evaluation presented, the PWM technique most suitable to each power stage of the UPS was;

1) SHE for the inverter stage, and

2) MSPWM for the controlled rectifier stage.

This will lead to the optimal combination of size reduction, weight reduction, and cost savings.

The software developed is relatively essential to simply and effectively analyze 3-ϕ static converters under various conditions. The routines were partially shown through brief examples, to be useful tools in a UPS research environment.

In particular, the analysis/simulation package emphasizes three main ingredients; user friendliness via direct schematic capture, low memory requirements, and faster execution time via a 3:1 reduction in the state matrix order when compared with PSPICE.[62]

The worst case ratings program quickly derives required components. When size and weight are of prime importance as in the applications considered, the software provides rapid comparison of component values versus switching frequency, load swing and PWM technique.

Further examples of the software results are presented in subsequent chapters 3 and 4.

3.0 DESIGN FOR 60 HZ UPS APPLICATIONS

From mains input to three phase output the 60 hz UPS topology proposed in chapter 2.3.1 can be segregated into three distinct stages for purposes of analysis; the input rectification and battery charging stage; the high frequency link and isolation stage; and the output inverter stage. These stages are each subdivided into input filter, switching bridge, and output filter sections to further simplify the analysis. To apply the resulting data to any input/output power, voltage, etc, all relevant equations and results are in per unit format. The base values selected for each stage reflect values which simplify assimilation and utilization. For instance;

1) For the inverter stage, all expressions are derived using the load voltage and output power as base values. This allows pro-rating of results based on known load voltage conditions such as 208 volt or 480 volt. Manipulation of this data then defines the inverter input requirements.

2) For the rectifier stage, all expressions and results are derived using the input voltage and power as base values. This enables pro-rating to known electrical mains inputs such as 208Vac or 600Vac. Manipulation of this data then defines the output voltage of the rectifier stage.

3) The high frequency link stage expressions are derived via both the input and output voltage ranges since both are required to identify the isolation stage turns ratio.

Although modern UPS specifications outlined in chapter 2.2 dictate that unbalanced and nonlinear loads should present little problem to the UPS

topology, the inverter stage analysis presented here assumes completely balanced and linear load conditions. This serves as a reference point for an in depth study into the topology alterations required for more complex nonlinear and unbalanced loads presented in chapter 4.0.

Since the application of a high frequency link in the UPS power train is relatively new, it is debatable as to which topology is an optimal choice. The actual high frequency link power conversion topology is more heavily dependant on power level than the inverter or rectifier power stages. In light of this an evaluation of several topologies is presented in chapter 3.3 giving insight into the proper selection for the medium power range of 10kVA.

Later parts of this chapter focus on a design example which includes extensive simulation and selected experimental verification. Frequently encountered experimental problems which are dealt with in this chapter include:

1) Proper power semiconductor selection. When ideal theoretical switches are replaced by non ideal practical switches, additional details and problems may exist.

2) Base drive selection. Gating any semiconductor is not a trivial problem and substantial time must be given to a suitable drive based on switch selection. This is especially true at medium to high power ranges.

3) Snubbers and switch protection. Numerous capacitors and saturable inductors are usually present in actual power train implementations and should therefore be considered.

4) PWM generation, control and protection. In actual implementations dead times or overlaps are required which on occasion may alter waveform spectral content. Sturdy digital controllers are

presented to reliably perform the requ ed control features.

3.1 Balanced Load Worst Case Inverter Ratings

The analysis of a 3-ϕ inverter power train as shown in figure F3.1 can be segregated into three discrete sections; the output filter stage; the power conversion stage and the input filter stage. Since the proposed inverter topology carries no isolation requirements, the usual output transformer evaluation is not present. Moreover since the isolation stage has been accommodated via a high frequency link preceding the inverter, the inverter power stage has its input voltage fully regulated.

Topology component ratings are solved from output to input

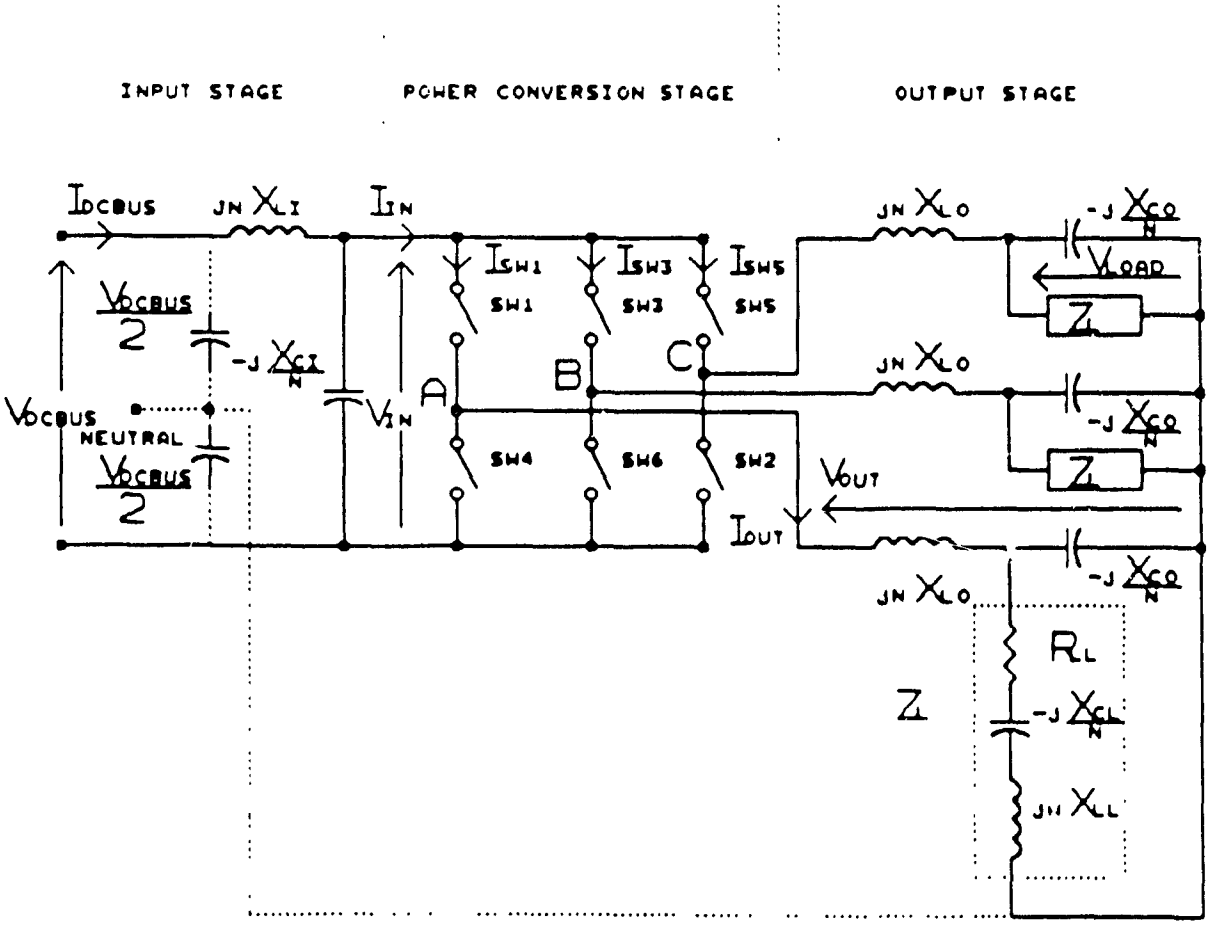


Figure F3.1 UPS inverter power train schematic

The analysis is based on the voltage and current transfer characteristics of the power conversion stage which in turn depend heavily on the PWM scheme applied. Figure F3.2 shows a typical PWM gating signal which may be applied to switch SW1 of figure F3.1.

Figure F3.2 Inverter switch#1 (SW1) gating signal (GSW1)

All analysis is done assuming ideal semiconductor switches. This simplifies the task and is relatively accurate since in practical applications non ideal switches alter the power train component evaluation only slightly. To fully comprehend an ideal switch operation suggests the visualization of an infinite impedance component when given a gating signal of level "0" and an infinite conductance when given a gating signal of level "1" as shown in figure F3.2.

Classical rules of voltage source inverter operation dictate that the voltage at points A, B and C of Figure F3.1 must be defined at all times. This rule immediately defines the gating signal of SW4 (G_{SW4}) as the inverse of Gsw1. (ie when Gsw1=0 -> Gsw4=1, when Gsw1=1 -> Gsw4=0). As a consequence of this, voltage V_{AN} can be defined directly by the PWM scheme and the dc bus voltage (V_{DCBUS}). Further, a second classical rule defines that V_{BN} and V_{CN} be at 120° and 240° phase difference with respect to V_{AN} leading to immediate definitions of V_{AB}, V_{BC} and V_{CA}. The voltage V_{AN} can be defined as

$$V_{AN} = \left[\sum_{N=1,3,5..}^{\infty} HAR_N \, SIN\, N(\omega\tau + \phi N) \right] \frac{V_{DCBUS}}{2} \; pu \qquad (3.1)$$

where HAR_N is the amplitude of each harmonic generated by the PWM scheme on a two level, ±1 swing or

$$HAR_N = \frac{4}{N\pi} \left[1 + 2 \sum_{K=1}^{KMAX} (-1)^K \, COS(N \cdot inter(K)) \right] \qquad (3.2)$$

It should be noted that the PWM harmonics generated in chapter 2.4 as AC TERM quantities are 3-ϕ, line to line values. Equation 3.2 is only valid for quarter wave symmetry pwm which is assumed here This leads to the transfer function of the inverter power stage;

$$\mathcal{TF} = \frac{V_{OUT}}{V_{DCBUS}} = \frac{1}{2} \sum_{N=1,3,5.}^{\infty} HAR_N \, SIN\, N(\omega\tau + \phi N) \qquad (3.3)$$

where $V_{OUT} = V_{AN}$

Setting $\phi N = 0$ as a reference point we have

$$\mathcal{TF} = \frac{V_{OUT}}{V_{DCBUS}} = \frac{1}{2} \sum_{N=1,5,7..}^{\infty} HAR_N \, SIN\, N\omega\tau \qquad (3.4)$$

Since the input stage is completely regulated, the PWM routine need not be changed to alter the gain of the converter as pointed out in chapter 2.4.2.1.1. This keeps HAR_N constant throughout the analysis Further assumptions made throughout the inverter analysis include;

-the existence of balanced load conditions

-the presence of a ripple free inverter input voltage

-the use of ideal power switching devices

-the use of ideal reactive components

-a PWM scheme which has quarter wave symmetry and is uniformly applied.

Selection of the PWM technique to be utilized was accomplished in chapter 2.4 and defined as SHE. The switching frequency however cannot be defined until the power level is considered. To deliver 10 kVA, a 3-ϕ inverter of the type shown in figure F3.1 can handle a switching frequency of roughly 25 pu with a 60 hz base frequency. Moreover it is estimated that the high frequency link stage powering the inverter will have a switching frequency of roughly 18 Khz. To prevent large magnitude, low order beat frequencies from disrupting the system the nonlinear power inverter will switch at roughly one tenth of the speed as the high frequency link supplying its power. This frequency falls roughly at 1.8 Khz. As derived in chapter 2.4, with SHE, the inverter requires a switching frequency or number of turn-offs/(switch·cycle) of

$$SW_F = (2 \cdot \#\text{ eliminated harmonics} + 3)\text{pu} \quad (3.5)$$

By setting the switching frequency at SW_F=21pu equation 3.5 yields

$$\#\text{ eliminated harmonics} = 9.$$

Using the nonlinear equations as described in section 2.4.2.1.1, elimination of 9 low order harmonics (ie 5, 7, 11, 13, 17, 19, 23, 25, and 29) results in the angles of table T3.1.

ANGLE #	ANGLE (DEGREES)
1	0.0000
2	5.4931
3	9.5486
4	16.6050
5	19.3359
6	27.7902
7	29.3928
8	39.0637
9	39.8068
10	50.8458
11	51.0535
12	128.9465
13	129.1452
14	140.1932
15	140.9363
16	150.6072
17	152.2098
18	160.6641
19	163.3935
20	170.4514
21	174.5069
22	180.0000
23	185.4931
24	189.5486
25	196.6065
26	199.3359
27	207.7902
28	209.3928
29	219.0637
30	219.8068
31	230.8458
32	231.0535
33	308.9465
34	309.1542
35	320.1932
36	320.9363
37	330.6072
38	332.2098
39	340.6641
40	343.3935
41	350.4514
42	354 5068
43	360.0000

Table T3.1 Inverter PWM transition angles

Moreover the actual spectral content is shown in figure F2.19C on a line to line basis with V_{DCBUS}=1pu.

3.1.1 Output Filter Ratings

The output filter required to reduce the THD below 5% is solved based on the following assumptions;

1) No voltage triplens exist,
2) The load is balanced resistive and equal to 1pu
3) Reducing the dominant harmonic below 2% virtually guaranteesthat the THD will be below 5% and the dominant harmonic will be below 3% during balanced loads of power factor swings from .7 leading to .7 lagging.

Since the PWM scheme is constant and the load is resistive, the dominant harmonic to fundamental component is a fixed ratio. Consequently the per unit break frequency of the output filter can be solved from

$$W_N = ORDER \cdot \left[\frac{(.02)HAR_{FUND}}{HAR_{DOM}} \right]^{1/Fo} \text{ pu} \qquad (3.6)$$

where W_N = pu filter break frequency (radians)

F_o = filter order= 2 for proposed UPS

Allowing the industry standard damping factor of .707, the pu capacitive and inductive impedances can be expressed as

$$X_{CO} = 2(.707)W_N \text{ pu} \qquad (3.7)$$

$$X_{LO} = 2(.707)/W_N \text{ pu} \qquad (3.8)$$

With reference to figure F2.19C one notes that the dominant harmonic which results in the lowest pu filter break frequency is the 35th. When

substituted into equation 3.6

$$W_N = 8.623 \text{ pu}$$

This further results in (from 3.7 and 3.8)

$$X_{CO} = 12.194 \text{ pu}$$

$$X_{LO} = .164 \text{ pu}$$

The current, voltage and power ratings of the output filter components requires derivation of the load voltage (V_{LOAD}) and the output current (I_{OUT}). To accommodate a generalized load varying in power factor, a series R-L-C network is used and represented as

$$Z_L = R_L + jNX_{LL} - jX_{CL}/N \text{ pu} \quad (3.9)$$

Therefore

$$I_{OUT} = \frac{V_{OUT}}{Z_{EQUIVALENT1}} \quad (3.10)$$

$$\text{Where} = Z_{EQUIVALENT1} = jNX_{LO} + \frac{Z_L(-jX_{CO}/N)}{Z_L - jX_{CO}/N} \text{ pu} \quad (3.11)$$

or using 3.4;

$$I_{OUT} = \sum_{N=1,5,7..}^{\infty} HAR_N \, SIN(N\omega\tau) \, \frac{V_{DCBUS}}{Z_{EQUIVALENT1}} \cdot \frac{1}{2} \text{ pu} \quad (3.12)$$

Treating the expression as a phasor quantity

$$I_{OUT} = \sum_{N=1,5,7.}^{\infty} \frac{HAR_N \, V_{DCBUS}}{jNX_{LO} + \frac{Z_L(-jX_{CO}/N)}{Z_L - jX_{CO}/N}} \cdot \frac{1}{2} \text{ pu} \quad (3.13)$$

$$= \sum_{N=1,5,7..}^{\infty} \frac{HAR_N \; VDCBUS}{jNXLO + \dfrac{-jXCORL/N + XCO/N(NXLL-XCL/N)}{RL + j(NXLL - XCL/N - XCO/N)}} \cdot \frac{1}{2} \text{ pu} \qquad (3.14)$$

$$= \sum_{N=1,5,7..}^{\infty} \frac{HAR_N \; VDCBUS}{jNXLO + \dfrac{(XCO/N(NXLL-XCL/N) - jXCORL/N)(RL-j(NXLL-XCL/N-XCO/N))}{RL^2 + (NXLL - XCL/N - XCO/N)^2}} \cdot \frac{1}{2} \qquad (3.15)$$

$$= \sum_{N=1,5,7..}^{\infty} \frac{1}{2} \cdot \frac{HAR_N \; VDCBUS}{jNXLO + \dfrac{RLXCO/N(NXLL-XCL/N) - jXCORL^2/N - \dfrac{jXCO/N(NXLL-XCL/N-XCO/N)(NXLL-XLO/N) - XCORL/N(NXLL-XCL/N-XCO/N)}{RL^2 + (NXLL - XCL/N - XCO/N)^2}}{}} \qquad (3.16)$$

Letting $A1 = \dfrac{\frac{RLXCO}{N}(NXLL - \frac{XCL}{N}) - \frac{XCORL}{N}(NXLL - \frac{XCL}{N} - \frac{XCO}{N})}{RL^2 + (NXLL - XCL/N - XCO/N)^2}$ (3.17)

$$= \frac{XCO^2 RL/N^2}{RL^2 + (NXLL - XCL/N - XCO/N)^2} \qquad (3.18)$$

$$B1 = \left[j\,NXLO - \left[\frac{\frac{XCORL^2}{N} + \frac{XCO}{N}(NXLL - \frac{XCL}{N} - \frac{XCO}{N})(NXLL - \frac{XCL}{N})}{RL^2 + (NXLL - XCL/N - XCO/N)^2} \right] \right] \qquad (3.19)$$

we obtain

$$I_{OUT} = \sum_{N=1,5,7..}^{\infty} \frac{1}{2} \cdot \frac{HAR_N \; V_{DCBUS}}{\sqrt{A_1^2 + B_1^2}} \; \angle -ARCTAN(B_1/A_1) \; pu \qquad (3.20)$$

Where HAR_N = eqn 3.2

A_1 = eqn 3.18

B_1 = eqn 3.19

From figure F3.1 it can be seen that the output filter combined with the load, act as a voltage divider for V_{OUT}. Since the PWM pattern is fixed this action tends to force V_{DCBUS} through a wide voltage swing trying to keep load voltage (V_{LOAD_1}) constant at 1 p.u. during load variations in power factor.

Mathematically,

$$V_{LOAD} = \frac{V_{OUT}}{Z_{EQUIVALENT}} \qquad (3.21)$$

$$\text{Where} \quad Z_{EQUIVALENT} = 1 + jNX_{LO}\left[\frac{jN}{X_{CO}} \cdot \frac{1}{R_L + j(NX_{LL} - X_{CL}/N)} \right] pu \qquad (3.22)$$

Using eqn 3.3, and treating the expression as a phasor

$$V_{LOAD} = \sum_{N=1,5,7..}^{\infty} \frac{HAR_N \; V_{DCBUS}}{1 + jNX_{LO}\left[\frac{jN}{X_{CO}} + \frac{1}{R_L + j(NX_{LL} - X_{CL}/N)} \right]} \cdot \frac{1}{2} \; pu \qquad (3.23)$$

$$= \sum_{N=1,5,7..}^{\infty} \frac{HAR_N \; V_{DCBUS}}{1 - \frac{N^2 X_{LO}}{X_{CO}} + \frac{jNX_{LO}R_L}{R_L^2 + (NX_{LL} - X_{CL}/N)^2} + \frac{NX_{LO}(NX_{LL} - X_{CL}/N)}{R_L^2 + (NX_{LL} - X_{CL}/N)^2}} \cdot \frac{1}{2} \qquad (3.24)$$

$$\text{Letting} \quad A_2 = 1 - \frac{N^2 X_{LO}}{X_{CO}} + \frac{NX_{LO}(NX_{LL} - X_{CL}/N)}{R_L^2 + (NX_{LL} - X_{CL}/N)^2} \qquad (3.25)$$

$$B_2 = j\left[\frac{jNX_{LO}R_L}{R_L^2 + (NX_{LL} - X_{CL}/N)^2} \right] \tag{3.26}$$

we obtain

$$V_{LOAD} = \sum_{N=1,5,7..}^{\infty} \frac{HAR_N \; V_{DCBUS}}{\sqrt{A_2^2 + B_2^2}} \cdot \frac{1}{2} \text{ pu} \tag{3.27}$$

Where HAR_N = eqn 3.2

A_2 = eqn 3.25

B_2 = eqn 3.26

By letting N=1 and substituting known values of Z_L ,X_{CO} and X_{LO} the required dc bus voltage (V_{DCBUS}) can be derived in order to deliver a 1 pu load voltage (V_{LOAD_1}=1).

$$V_{DCBUS} = \sqrt{\frac{A_2^2 + B_2^2}{HAR_1 \left[\frac{1}{2}\right]}} \text{ pu} \tag{3.28}$$

The worst case output capacitor current rating is tied to the worst case voltage ripple it experiences. This will typically occur when the load is at the lowest lagging power factor. The inductive load tends to cancel some of the capacitive filtering effect thus increasing the ripple. For the UPS application here, .7 is the worst case load lagging power factor. Setting the load power factor to .7 lagging, utilizing the output filter earlier designed and setting N=1, equations 3.25 and 3.26 yields

A_2 = 1.103 pu

$$B_2 = .1148 \text{ pu}$$

By inserting HAR_1, equation 3.28 yields

$$V_{DCBUS} = 1.93 \text{ pu}$$

Concerned only with harmonic amplitudes I_{CORMS} may be defined as;

$$I_{CORMS} = \frac{V_{CORMS}}{Z_{CO}} \text{ pu} \tag{3.29}$$

$$= \frac{1}{2}\sqrt{\sum_{N=1,5,7..}^{\infty}\left[\frac{HAR_N \; V_{DCBUS}}{\sqrt{A_2^2 + B_2^2}} \cdot \frac{N}{\sqrt{2}\,X_{CO}}\right]^2} \text{ pu} \tag{3.30}$$

and

$$V_{CORMS} = \frac{1}{2}\sqrt{\sum_{N=1,5,7..}^{\infty}\left[\frac{HAR_N \; V_{DCBUS}}{\sqrt{A_2^2 + B_2^2}} \cdot \frac{1}{\sqrt{2}}\right]^2} \text{ pu} \tag{3.31}$$

Where HAR_N = from figure F2.19

A_2 = equation 3.25 with Z_L =.7 lag

B_2 = equation 3.26 with Z_L =.7 lag

V_{DCBUS} = equation 3.28 with Z_L =.7 lag

Finally

$$Cov_A = V_{CORMS} \cdot I_{CORMS} \text{ pu} \tag{3.32}$$

Table T3.2 shows the evaluation of equation 3.27

N	V_{LOAD_N}
1	1.0000
5	0.0000
7	0.0000
11	0.0000
13	0.0000
17	0.0000
19	0.0000
23	0.0000
25	0.0000
29	0.0000
31	0.0000
35	0.0240
37	0.0145
41	0.0017
43	0.0005
47	0.0002
49	0.0000
53	0.0002
55	0.0000
59	0.0004
61	0.0003
65	0.0033
67	0.0026
71	0.0016
73	0.0017
77	0.0005
79	0.0002
83	0.0001
85	0.0001
89	0.0001
91	0.0001
95	0.0004
97	0.0010

Table T3.2 Load voltage harmonics with .7 lagging power factor

Using figure F2.19C for HAR_N and substituting in equations 3.30, 3.31 and 3.32, we obtain

I_{CORMS} = .087 pu

V_{CORMS} = .707 pu

C_{OVA} = .0615 pu

The worst case output inductor current rating occurs when the load is at its lowest capacitive power factor. In contrast and of slightly lower priority, the worst case voltage rating will occur when the power factor is at its lowest lagging value. This can be explained by the load/filter voltage divider action creating the highest required dc bus voltage under fully inductive loads. Since the fundamental load voltage is constant at 1pu, the difference between V_{DCBUS} and V_{LOAD_1} appears across the output filter inductance. The inductor current can be solved using equation 3.20 where the phase term can be neglected.

$$I_{LORMS} = \sqrt{\sum_{N=1,5,7..}^{\infty} \left[\frac{1}{2} \cdot \frac{HAR_N \, V_{DCBUS}}{\sqrt{A_1^2 + B_1^2}} \cdot \frac{1}{\sqrt{2}} \right]^2} \quad pu \qquad (3.33)$$

where A_1 = equation 3.18 with pf=.7 leading

B_1 = equation 3.19 with pf=.7 leading

At .7 leading power factor equation 3.28 yields

V_{DCBUS}= 1.53 pu

Further, equation 3.20 results in table T3.3 which represents the spectral content of I_{OUT}.

N	I_{OUT_N}
1	1.0601
5	0.0000
7	0.0000
11	0.0000
13	0.0000
17	0.0000
19	0.0000
23	0.0000
25	0.0000
29	0.0000
31	0.0236
35	0.0529
37	0.0340
41	0.0044
43	0.0014
47	0.0006
49	0.0000
53	0.0006
55	0.0000
59	0.0015
61	0.0013
65	0.0136
67	0.0112
71	0.0072
73	0.0082
77	0.0025
79	0.0009
83	0.0004
85	0.0003
89	0.0006
91	0.0009
95	0.0024
97	0.0062

Table T3.3 Output line current harmonic content for .7 leading pf

Utilizing table T3.3, equation 3.33 gives,

$$I_{LORMS} = 0.751 \text{ pu}$$

The worst case inductor voltage can also be solved from equation 3.20 but with lagging power factor as opposed to leading.

$$V_{LORMS} = I_{OUT} \cdot Z_{LO} \qquad (3.34)$$

$$V_{LORMS} = \sqrt{\sum_{N=1,5,7..}^{\infty}\left[\frac{1}{2}\cdot\frac{HAR_N\ V_{DCBUS}}{\sqrt{A_1^2 + B_1^2}}\cdot\frac{nX_{LO}}{\sqrt{2}}\right]^2} \quad pu \qquad (3.35)$$

where A_1 = equation 3.18 with pf=.7 lagging

B_1 = equation 3,19 with pf=.7 lagging.

Finally

$$L_{OVA} = V_{LORMS} \cdot I_{LORMS} \qquad (3.36)$$

V_{DCBUS} has previously been solved for lagging power factor of .7 as

V_{DCBUS}= 1.93 pu

Solution of equation 3.35 results in

V_{LORMS}= .434 pu

and finally

L_{OVA}=.3259 pu

3.1.2 Inverter Switch Ratings

In practical application only the forward current passing through the power switching device is considered when solving rated current. This is due to the addition of an anti-parallel diode used to pass the regenerative current. Based on this, the maximum current will occur when I_{OUT} is in phase with V_{OUT} resulting in full switch conduction interval. The current rating is found by combining the output filter solved in chapter 3.1.1 with an appropriately selected load such that the inverter sees a resistive output impedance. The generalized load was given in chapter 3.1.1. as

$$Z_L = R_L + jnX_{LL} - jX_{CL}/n \qquad (3.37)$$

producing an output current solved via equation 3.20 rewritten here for convenience.

$$I_{OUT} = \sum_{N=1,5,7..}^{\infty} \frac{1}{2} \cdot \frac{HAR_N \; V_{DCBUS}}{\sqrt{A_1^2 + B_1^2}} \; \angle -ARCTAN(B_1/A_1) \text{ pu} \qquad (3.38)$$

where $\angle -ARCTAN(B_1/A_1)$ =phase between V_{OUT} and I_{OUT}

From this expression it can be seen that to keep the fundamental component of I_{OUT} in phase with V_{OUT}

$$\angle -ARCTAN(B_1/A_1) = 0 \qquad (3.39)$$

Substituting the filter components derived in chapter 3.1.1, letting N=1 in equation 3.39 and fixing $|Z_L|$=1pu, X_{LL} or X_{LC} is a function of R_L and the equation (3.39) essentially reduces to a single variable transcendental form. At this point a single variable root finder routine such as the Secant method may be used to solve the load components R_L, X_{LL} and X_{CL}.

Applying the root finder results in

R_L = .99635 pu

X_{CL} = .08535 pu

X_{LL} = .00000 pu

These values place the fundamental components of V_{OUT} and I_{OUT} in phase.

Once the load conditions are known only V_{DCBUS}, which is directly dependent on load conditions remains to be evaluated before solving the magnitude of I_{OUT}. V_{DCBUS} can be solved using equation 3.28 resulting in

V_{DCBUS} = 1.7151 pu

The solution of V_{DCBUS} can be substituted in equation 3.20 to solve for

IOUT. It is feasible to multiply the spectral content of IOUT with the spectral content of a modified version of the transfer function $\mathcal{TF}$ (equation 3.4) to obtain the harmonic content of the switch current Iswl. This in turn could be used to solve for average and rms switch current. However, the process is extremely tedious and time consuming. The alternate approach used here is to convert IOUT into its time domain representation and multiply with the time domain representation of the switch gating signal Gswl [41]. The time domain representation of IOUT is given by an array solved from the instantaneous amplitude calculations of IOUT as

$$IOUT\_TD(\omega\tau) = \sum_{N=1,5,7..}^{\infty} \frac{1}{2} \cdot \frac{HAR_N \; VDCBUS}{\sqrt{A1^2 + B1^2}} \cdot SIN\left[N\omega\tau - \angle ARCTAN(B1/A1) \right] pu \qquad (3.40)$$

where $\omega\tau$ = 0,1,2....360 (deg)

$A1$ = equation 3.18

$B1$ = equation 3.19

The resulting time domain waveform shape is shown in figure F3.3A

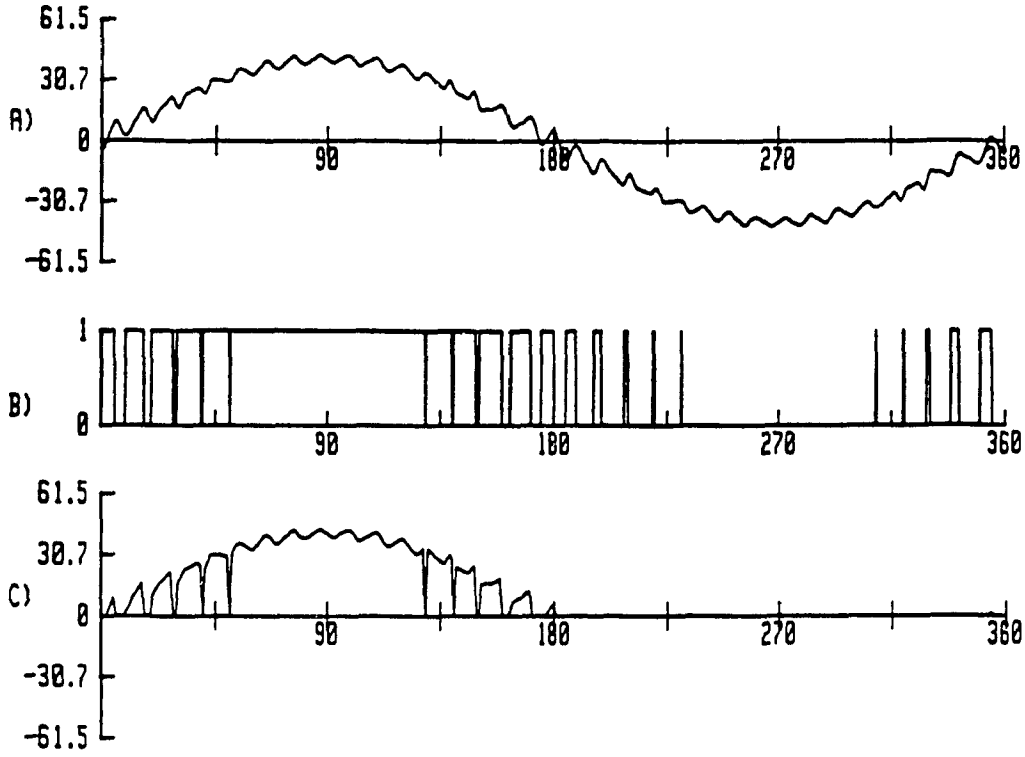


Figure F3.3 Theoretical switch waveforms

A) Inverter output line current
B) Switch gating signal Gsw1
C) Switch current

The gating signed of switch SW1 (Gsw1) is likewise stored in an array as

$$Gsw1\_TD(\omega\tau) = \begin{cases} 1 \text{ when SW1 is infinite conductance} \\ 0 \text{ when SW1 is infinite impedence} \end{cases}$$

$$\text{where} \quad \omega\tau = 0, 1, 2, \ldots, 360 \tag{3.41}$$

The waveform is shown in figure F3.3B. It can be seen that the angles or transition states correspond to table T3.1.

Since the power semiconductor is typically rated based only on its forward current $I_{OUT\_TD}(wt)$ must be screened for its positive portions.

$$I_{OUT\_TDP}(\omega\tau) = \begin{cases} I_{OUT\_TD}(\omega\tau) \cdot G_{SW1\_TD}(\omega\tau) & \text{when } I_{OUT\_TD}(\omega\tau) > 0 \\ 0 & \text{when } I_{OUT\_TD}(\omega\tau) \leq 0 \end{cases}$$

where $\omega\tau = 0,1,2,\ldots,360$ (3.42)

The screening and multiplication process results in the waveform shown in figure F3.3C. The average as well as the rms current ratings of each switch can be found respectively as

$$I_{SWAVE} = \frac{1}{360} \sum_{\omega\tau=0}^{360} I_{OUT\_TDP}(\omega\tau) \quad pu \tag{3.43}$$

$$I_{SWRMS} = \sqrt{\frac{1}{360} \sum_{\omega\tau=0}^{360} \left[I_{OUT\_TDP}(\omega\tau) \right]^2} \quad pu \tag{3.44}$$

Solving equation 3.43 results in an average switch current of

$$I_{SWAVE} = .301 \text{ pu}$$

3.1.3 Input Filter Ratings

Figure F3.4 shows the input stage of figure F3.1 with a current sink that accurately models the combined power converter and output stage.

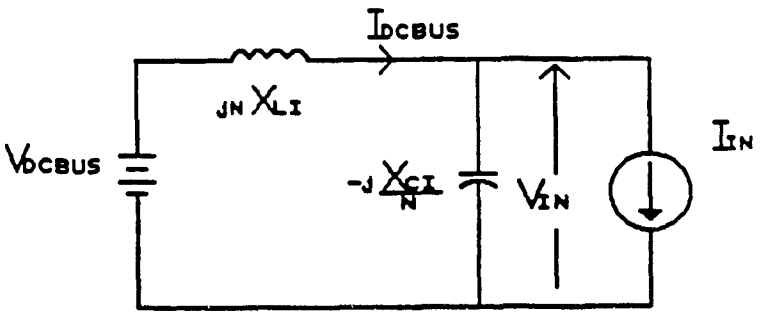


Figure F3.4 Input stage analysis model

The components LI and CI are selected to simultaneously limit the voltage supply current ripple (IDCBUS_RIP) and to keep a steady inverter input voltage (VIN). Typically allowable inductor current ripple (IDCBUS_RIP) is 10%, where

$$I_{DCBUS\_RIP} = \frac{100}{I_{DCBUS_0}} \sqrt{\sum_{N=6,12,18}^{\infty} I_{DCBUS_N}^2} \qquad (3.45)$$

where I_{DCBUS_N} = Magnitude of the N'th component of IDCBUS current.

Similarly the allowable capacitor voltage ripple (VIN_RIP) is 5% , where

$$V_{IN\_RIP} = \frac{100}{V_{IN_0}} \sqrt{\sum_{N=6,12,18}^{\infty} V_{IN_N}^2} \qquad (3.46)$$

where V_{IN_N} = Magnitude of the N'th component of inverter input voltage VIN.

Letting

$$I_{IN} = \sum_{N=0,6,12}^{\infty} I_{IN_N} \cos(N\omega\tau) \qquad (3.47)$$

we obtain

$$I_{DCBUS} = \sum_{N=0,6,12}^{\infty} \frac{I_{IN_N} \cos(N\omega\tau)}{1-N^2 X_{LI}/X_{CI}} \tag{3.48}$$

Therefore extracting only the magnitudes for ripple calculation;

$$I_{DCBUS\_RIP} = \frac{100}{I_{DCBUS_0}} \sqrt{\sum_{N=6,12,18}^{\infty} \left[\frac{I_{IN_N}}{1-N^2 X_{LI}/X_{CI}} \right]^2} \tag{3.49}$$

With N=0 in equation 3.48 $I_{DCBUS} = I_{IN_0}$. Further, let

$$X_F = X_{LI}/X_{CI} \tag{3.50}$$

and equation 3.49 becomes

$$I_{DCBUS\_RIP} = \frac{100}{I_{IN_0}} \sqrt{\sum_{N=6,12,18}^{\infty} \left[\frac{I_{IN_N}}{1-N^2 X_F} \right]^2} \tag{3.51}$$

By setting I_{DCBUS_RIP} to 10% we can solve X_F using a single variable root finder routine such as the secant method.

Using superposition and once again dealing only with magnitudes

$$V_{IN} = V_{DCBUS} + \sum_{N=0,6,12}^{\infty} \frac{I_{IN_N} \cdot N X_{LI}}{1-N^2 X_{LI}/X_{CI}} \tag{3.52}$$

leading to

$$V_{IN\_RIP} = \frac{100}{V_{DCBUS}} \sqrt{\sum_{N=6,12,18}^{\infty} \left[\frac{I_{IN_N} \cdot N X_{CI} \cdot X_F}{1-N^2 X_F} \right]^2} \tag{3.53}$$

By setting V_{IN_RIP} to 5% and using the X_F found from 3.51, a single variable numerical routine can be used to solve X_{CI}. Since

$$X_F = X_{LI}/X_{CI} \tag{3.54}$$

we have

$$X_{LI} = X_F \cdot X_{CI} \tag{3.55}$$

which is used to solve for X_{LI}.

The spectral content of I_{IN} required to complete equation 3.51 and 3.53 can be solved with the aid of figure F3.5.

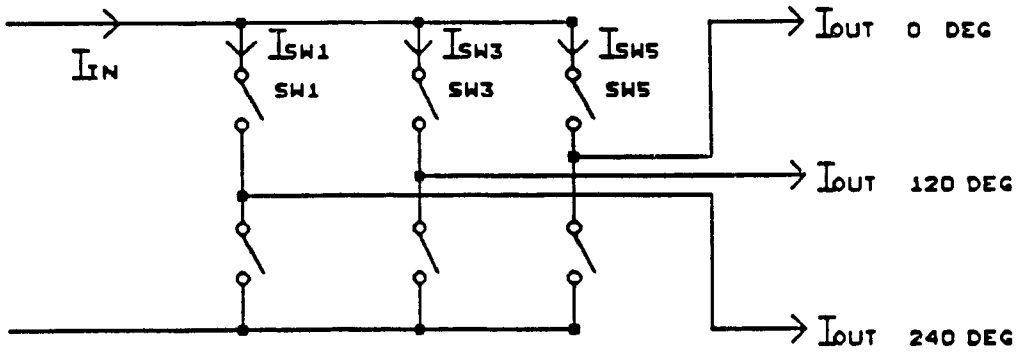


Figure F3.5 Summation of switch currents

From figure F3.5 current I_{IN} can be solved as

$$I_{IN} = I_{SW1} + I_{SW3} + I_{SW5} \tag{3.56}$$

With interest only in harmonic magnitude level, due to 120° and 240° phase shifts between the three switch currents,

$$I_{IN} = \sum_{N=0,6,12}^{\infty} 3 \cdot I_{SW1_N} \tag{3.57}$$

This can be seen by the phasor representation of figure F3.6.

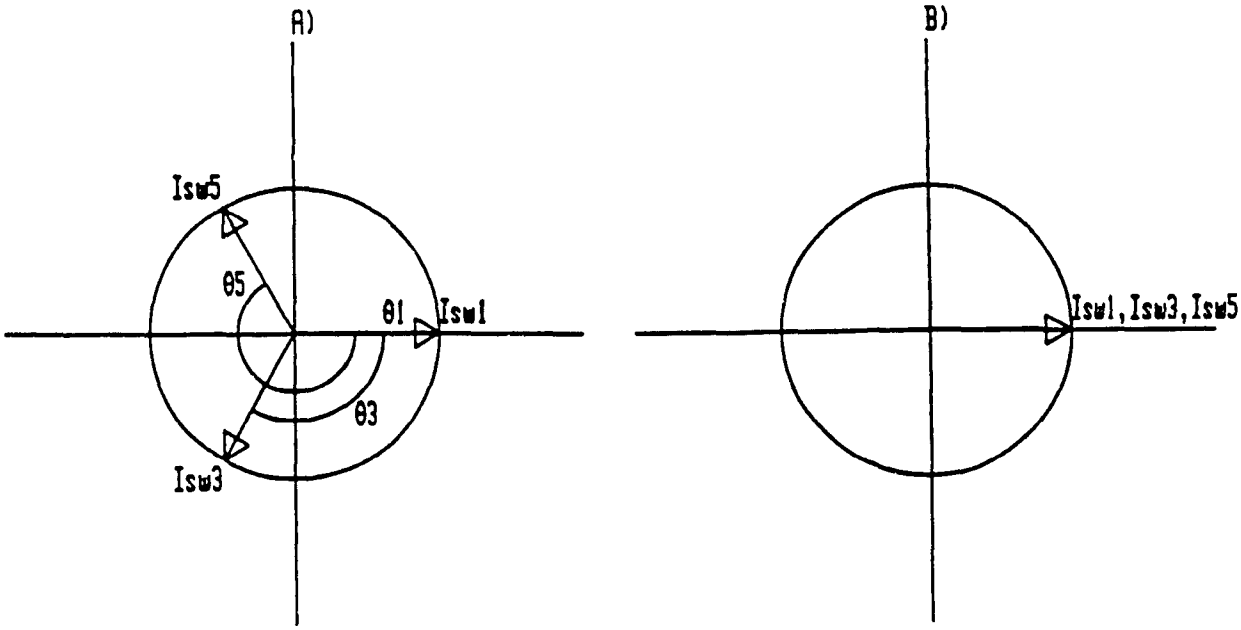


Figure F3.6 Phasor diagram of input current

A) Representation of harmonics of non 6 multiples
B) Representation of even harmponics of multiples of 6

In particular figure F3.6A shows that the phasors for all three currents will be equally phase shifted for any harmonic in the series

$$N = 2,\ 4,\ 8,\ 10,\ 14,\ 16,\ldots.\infty$$

on the basis of

$$\begin{aligned} \theta_1 &= 0.0^\circ = \text{ref} \\ \theta_2 &= 120 \cdot N \\ \theta_3 &= 240 \cdot N \end{aligned} \qquad (3.58)$$

Thus when summed

$$I_{IN_N} = Isw1_N + Isw3_N + Isw5_N = 0 \quad \text{for } N = 2,\ 4,\ 8,\ 10\ldots\infty$$

In contrast however for N = 0, 6, 12, 18...∞ figure F3.6B and equation 3.58 reveals that the harmonics are in phase and sum up thus leading to equation 3.57.

Iswl is solved in the frequency domain by

$$I_{SWl} = G_{SWl} \cdot I_{OUT} \tag{3.59}$$

where

$$G_{SWl} = \sum_{K=1,3,5..}^{\infty} \frac{HAR_K}{2} \cdot SIN(K\omega\tau) + \frac{1}{2} \tag{3.60}$$

Further an alteration of equation 3.20 results in

$$I_{OUT} = \sum_{N=1,5,7..}^{\infty} I_{OUTMAG_N} \cdot SIN(N\omega\tau + I_{OUTPHASE_N}) \tag{3.61}$$

where $$I_{OUTMAG_N} = \frac{1}{2} \cdot \frac{HAR_N \, V_{DCBUS}}{\sqrt{A_1^2 + B_1^2}}$$

$$I_{OUTPHASE_N} = \angle -ARCTAN(B_1/A_1)$$

A_1 = equation 3.18

B_1 = equation 3.19

Therefore,

$$I_{SWl} = \frac{1}{2} \sum_{N=1,5,7}^{\infty} I_{OUTMAG_N} \cdot SIN(N\omega\tau + I_{OUTPHASE_N}) + \sum_{N=1,5,7..}^{\infty} \sum_{K=1,3,5..}^{\infty} I_{OUTMAG_N} \cdot SIN(N\omega\tau + I_{OUTPHASE_N}) \cdot \frac{HAR_K}{2} \cdot SIN(K\omega\tau) \tag{3.62}$$

The first term on the right of the equal sign will eventually be canceled by Isw3 and Isw5 due to phenomena explained earlier. The final term on the right of the equation can be solved with the help of the trigonometric identity;

$$\mathrm{SIN(A)\cdot SIN(B)} = \frac{\mathrm{COS(A-B)-COS(A+B)}}{2} \tag{3.63}$$

Leading to

$$\mathrm{Isw1}^{*} = \sum_{N=1,5,7}^{\infty} \sum_{K=1,3,5}^{\infty} \frac{\mathrm{IOUTMAG_N\ HAR_K}}{4} \left[\mathrm{COS}(N\omega\tau + \mathrm{IOUTPHASE_N} - K\omega\tau) - \mathrm{COS}(N\omega\tau + \mathrm{IOUTPHASE_N} + K\omega\tau)\right] \tag{3.64}$$

$$= \sum_{N=1,5,7}^{\infty} \sum_{K=1,3,5}^{\infty} \frac{\mathrm{IOUTMAG_N\ HAR_K}}{4} \left[\mathrm{COS}((N-K)\omega\tau + \mathrm{IOUTPHASE_N}) - \mathrm{COS}((N+K)\omega\tau + \mathrm{IOUTPHASE_N}\right] \tag{3.65}$$

Using $\mathrm{COS(A-B)} = \mathrm{COS(A)\cdot COS(B)} + \mathrm{SIN(A)\cdot SIN(B)}$ (3.66)

and

$\mathrm{COS(A+B)} = \mathrm{COS(A)\cdot COS(B)} - \mathrm{SIN(A)\cdot SIN(B)}$ (3.67)

we obtain

$$\mathrm{Isw1}^{*} = \sum_{N=1,5,7}^{\infty} \sum_{K=1,3,5}^{\infty} \frac{\mathrm{IOUTMAG_N\ HAR_K}}{4} \left[\mathrm{COS\ (IOUTPHASE_N)\cdot COS}(N-K)\omega\tau - \mathrm{SIN(IOUTPHASE_N)\cdot SIN}(N-K)\omega\tau - \mathrm{COS(IOUTPHASE_N)\cdot COS}(N+K)\omega\tau + \mathrm{SIN(IOUTPHASE_N)\cdot SIN}(N+K)\omega\tau\right] \tag{3.68}$$

Equation 3.68 can be further simplified resulting in

$$I_{SW1}^{*} = \sum_{N=1,5,7}^{\infty} \sum_{K=1,3,5}^{\infty} \left[\cos\left(I_{OUTPHASE_N}\right) \cdot \left[\cos(N-K)\omega\tau - \cos(N+K)\omega\tau \right] + \right.$$

$$\left. \sin\left(I_{OUTPHASE_N}\right) \cdot \left[\sin(N+K)\omega\tau - \sin(N-K)\omega\tau \right] \right] \frac{I_{OUTMAG_N} \, HAR_K}{4} \qquad (3.69)$$

Since only harmonic components of N=0,6,12,18...∞ will exist, with the multiplication factor of three, equation 3.69 yields

$$I_{IN} = 3 \cdot \sum_{N=1,5,7}^{\infty} \sum_{K=1,3,5}^{\infty} \left[\cos\left(I_{OUTPHASE_N}\right) \cdot \left[\cos(N-K)\omega\tau - \cos(N+K)\omega\tau \right] + \right.$$

$$\left. \sin\left(I_{OUTPHASE_N}\right) \cdot \left[\sin(N+K)\omega\tau - \sin(N-K)\omega\tau \right] \right] \frac{I_{OUTMAG_N} \, HAR_K}{4} \qquad (3.70)$$

where $|N-K|, |N+K| = 0,6,12,\ldots,$

In μF's, the worst case inpu capacitor rating will exist when the output load is .7 power factor leading. With these conditions, equation 3.70 yields the inverter input current harmonic content shown in table T3.4

N	$I_{I N_N}$
0	.6900
6	.0009
12	.0001
18	.0001
24	.0005
30	.1366
36	.3231
42	.0258
48	.0045
54	.0053
60	.0126
66	.1336
72	.1057
78	.0131
84	.0051
90	.0138

Table T3.4 Inverter input current spectrum at .7 pf leading

Insertion of this spectrum to equation 3.51 and 3.53 results in

X_{LI} = .0317 pu

X_{CI} = 6.146 pu

X_{CI} will be a worst case desired rating, however X_{LI} will be discarded as it is not a worst case rating. The worst case rating for X_{LI} occurs at load power factor of .7 lagging which is in contrast to the worst case for X_{CI}.

Re-calculation of 3.70 using a lagging power factor of .7 results in an input current spectral content shown in table T3.5.

N	I_{IN_N}
0	.5400
6	.0012
12	.0001
18	.0002
24	.0006
30	.0831
36	.3639
42	.0350
48	.0053
54	.0057
60	.0142
66	.1019
72	.0833
78	.0105
84	.0041
90	.0112

Table T3.5 Inverter input current spectrum at .7 pf lagging

Re-evaluation of equation 3.51 with a fixed value of X_{CI} solved earlier results in the worst case input filter inductor rating

$$X_{LI} = .039 \text{ pu.}$$

The input filter capacitor may be a unipolar device since only dc voltage plus ripple will be expected across its terminals. The maximum dc bus voltage ($V_{DCBUSMAX}$) will occur during lowest inductive load power factor giving

$$V_{CIRMS} = V_{DCBUS} \tag{3.71}$$

Where V_{DCBUS} =equation 3.28 with PF = .7 lagging

The result is

$$V_{CIRMS} = 1.93 \text{ pu.}$$

Further, the current ripple supplied by the capacitor can be solved with the assumption that all harmonic currents demanded by the power conversion stage are delivered from the capacitor. Simplifying equation 3.70 to

$$I_{IN} = \sum_{N=0,6,12..}^{\infty} I_{INMAG_N} \quad pu \tag{3.72}$$

Where I_{INMAG_N} = amplitudes of each harmonic yielded by processing equation 3.70

The worst case current will prevail during the lowest power factor inductive load yielding

$$I_{CIRMS} = \sqrt{\sum_{N=6,12,18..}^{\infty} \frac{I_{INMAG_N}^2}{2}} \quad pu \tag{3.73}$$

Evaluation of equation 3.73 results in (truncated to 60pu)

$$I_{CIRMS} = .265 \text{ pu}$$

In contrast to Switch Mode Rectifiers, the input filter inductor current is not at highest level when the dc bus voltage (V_{DCBUS}) is at its minimum level. Worst case input inductor current (I_{LIRMS}) exists when I_{OUT} and V_{OUT} are in phase as during the worst case switch current ratings of chapter 3.1.2. Therefore,

$$I_{LIRMS} = \frac{P_{OUT}}{V_{DCBUS}} = \frac{P_{IN}}{V_{DCBUS}} = \frac{V_{LOAD_1} \cdot I_{LOAD_1} \cdot PF \cdot 3}{2\ V_{DCBUS}} \tag{3.74}$$

Since V_{LOAD_1} = 1 pu peak

I_{LOAD_1} = 1 pu peak

PF = R_L

$$I_{LIRMS} = \frac{3 \cdot R_L}{2 \cdot V_{DCBUS}} \text{ pu} \qquad (3.75)$$

where R_L was previously solved via equation 3.39

V_{DCBUS} is solved using equation 3.28

Evaluation of equation 3.75 results in

$R_L = .99635$ pu

$V_{DCBUS} = 1.7151$ pu

and finally $I_{LIRMS} = .871$ pu

The worst case input filter inductor voltage occurs when the load is at its lowest lagging power factor. This power factor implies worst case input filter capacitor voltage resulting in worst case inductor ripple voltage if the dc bus voltage is assumed constant.

Therefore,

$$V_{LIRMS} = \sqrt{\sum_{n=6,12,18}^{\infty} \left[\frac{I_{INMAG_N} \cdot X_{CI}}{\sqrt{2}_N} \right]^2} \text{ pu} \qquad (3.76)$$

Where I_{INMAG_N} is solved from 3.70 with a load power factor of lowest lagging value.

Utilizing the lagging power factor input current spectrum previously solved and shown in table T3.5 equation 3.76 yields

$V_{LRIMS} = .046$ pu.

In practice this voltage is so low that it is negligible. For this reason it is not taken into account during the input filter inductor current calculations (equation 3.75) or the capacitor terminal voltage calculation

(equation 3.71).

In order to derive all worst case ratings it becomes evident that several basic equations are utilized many times with different load conditions. The main equations referred to are 3.20, 3.27, 3.28 and 3.70. This repetition requirement combined with the complex and tedious summations virtually necessitate a computer algorithm to quickly and accurately yield results. For this reason specialized software was developed. It's full description is featured in chapter 2.5.1

3.2 3 Phase Controlled Rectifier Ratings

The output power of a 3-ϕ controlled rectifier can be adjusted by either phase shifting the semiconductor gating signals with respect to the input line voltages, or by using a PWM technique with modulation control. The former technique allows an optimized, fixed PWM pattern that can offer significant gain and/or harmonic reduction at nominal loads. Phase shifting to control output voltage however, results in dramatic power factor deterioration typically equal in value to the normalized output voltage [23]. [i.e. reducing the rectifier output voltage to 50% results in an input power factor of .5]. Even with the addition of large input filter components to compensate, power factor cannot be raised to the required specification given in chapter 2. In contrast, the use of a variable modulation PWM technique can keep power factor significantly higher while still linearly controlling the output voltage. This feature is accompanied however by an increase in switching frequency and usually a reduction in gain over the programmed PWM option. Never the less, a variable modulation index PWM technique is employed here since, for practical applications, the correction of power factor to meet the specifications is envisioned to be more complex than increasing switch and component ratings to compensate for increased switching stresses.

The rectifier stage is shown in figure F3.7.

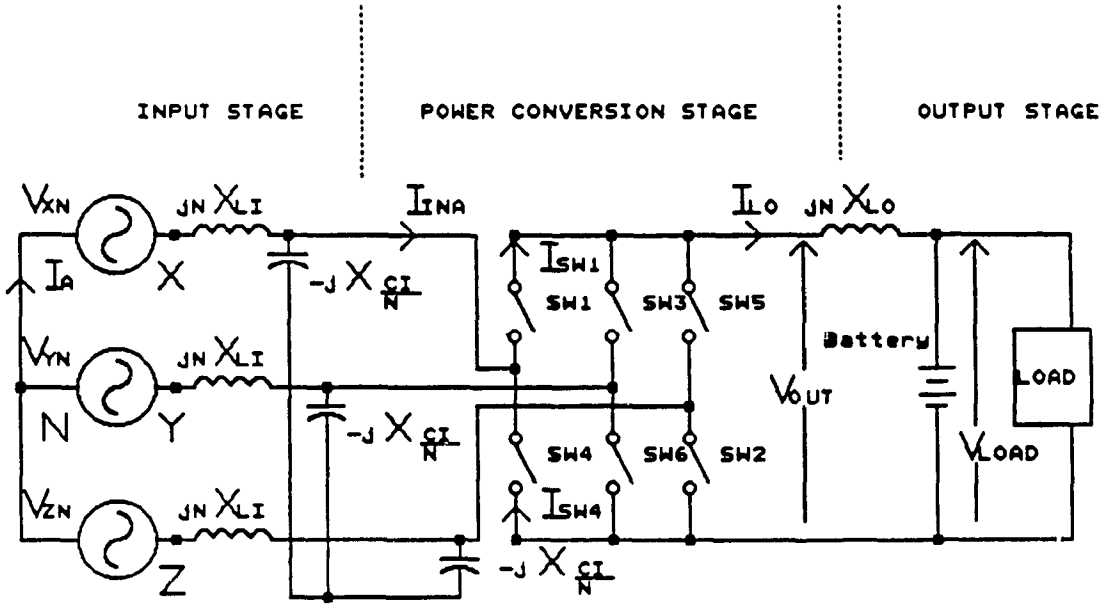


Figure F3.7 Controlled rectifier power train topology

The assumptions made during the analysis are;

1) ideal switches and components

2) balanced input voltage supply

3) rectifier load is essentially resistive

The rectifier can effectively be segregated into the output stage, power conversion stage, and the input stage. As in the inverter analysis the bridge transfer function $\mathcal{TF}$ is a significant variable during analysis. As a starting point, figure F3.8 shows a basic 3-ϕ rectifier model which simplifies analysis. Initially, the effects of the input filter are ignored.

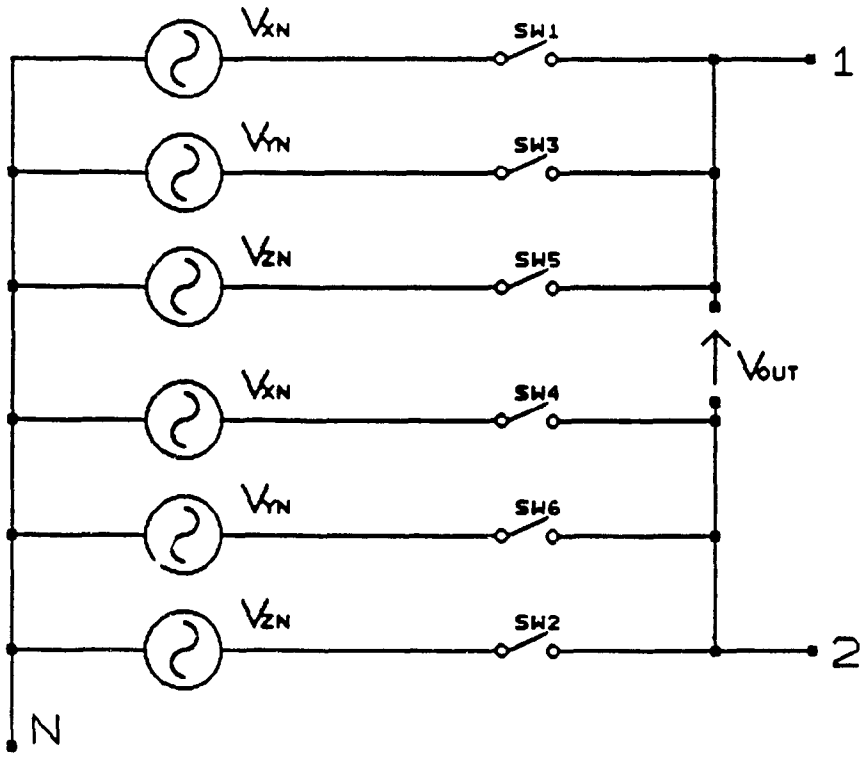


Figure F3.8 Simplified model for transfer function realization

V_{IN} can be written as

$$V_{IN} = V_{XN} \cdot G_{SW1} + V_{YN} \cdot G_{SW3} + V_{ZN} \cdot G_{SW5} \quad (3.77)$$

Similarly

$$V_{2N} = V_{XN} \cdot G_{SW4} + V_{YN} \cdot G_{SW6} + V_{ZN} \cdot G_{SW2} \quad (3.78)$$

Combining equations 3.77 and 3.78

$$V_{OUT} = V_{12} = V_{IN} - V_{2N} \quad (3.79)$$

$$= V_{XN}(G_{SW1}-G_{SW4}) + V_{YN}(G_{SW3}-G_{SW6}) + V_{ZN}(G_{SW5}-G_{SW2}) \quad (3.80)$$

During gating signal derivations (Gsw1-Gsw4) is chosen to reflect the desired input line current 'I_{INA}' wave shape with a constant of multiplication for scaling. This shape corresponds directly to the intersections evaluated with the PWM technique chosen. Figure 3.9 shows a typical gating signal

derivation to clarify the aforementioned discussion by example. Similarly (Gsw3-Gsw6) and (Gsw5-Gsw2) are phase shifted with respect to (Gsw1-Gsw4).

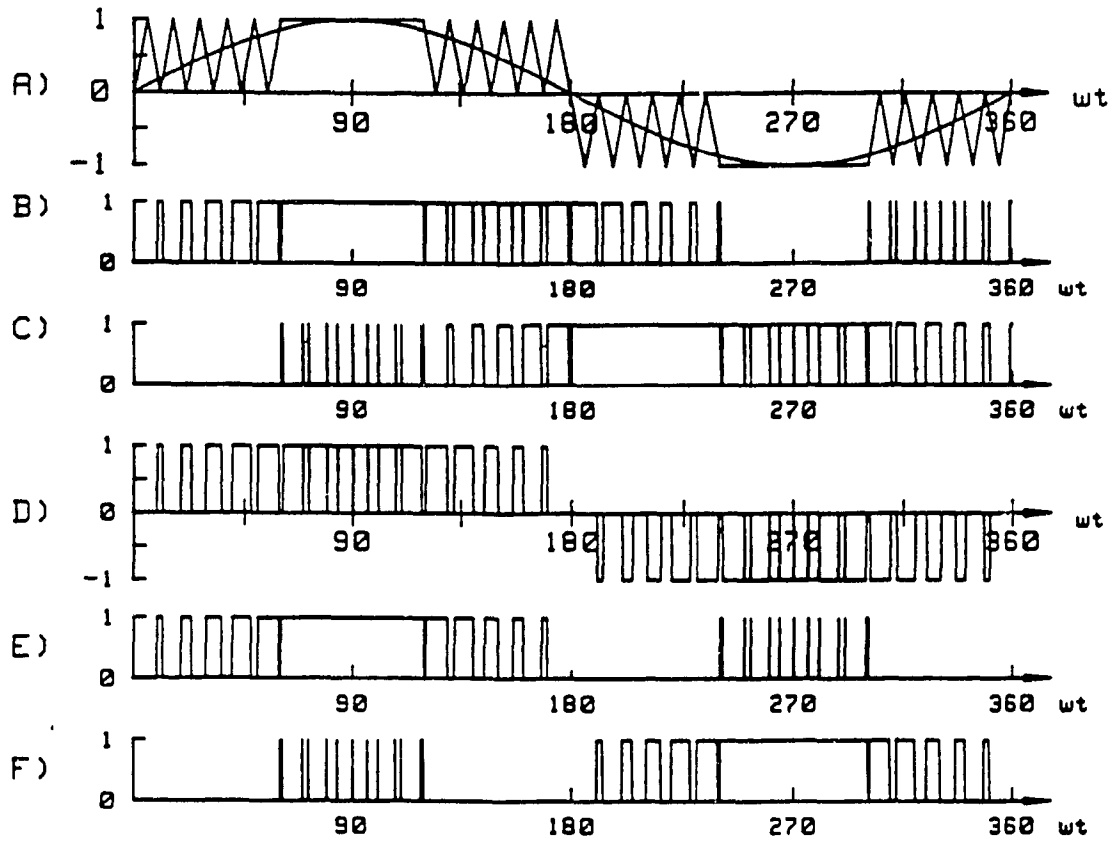


Figure F3.9 Controlled rectifier gating signal derivation

A) PWM Scheme
B) Control signal F1
C) Control signal F2
D) Desired input current shape (F1-F2)
E) Gating signal for SW1 (GSW1)
F) Gating signal for SW4 (GSW4)

Gsw1-Gsw4 can be represented in the frequency domain form as

$$(\text{Gsw1-Gsw4}) = \sum_{N=1,5,7}^{\infty} \text{HAR}_N \text{ SIN } N(\omega\tau+\phi N) \qquad (3.81)$$

Where HAR_N are the AC TERM quantities derived in chapter 2.4 on a line to line output basis. (The inverter analysis previously presented utilized the

respective line to neutral AC TERM quantities) Similarly, yet phase shifted we obtain

$$(Gsw3\text{-}Gsw6) = \sum_{N=1,5,7..}^{\infty} HAR_N \text{ SIN } N(\omega\tau+\phi N-120) \tag{3.82}$$

$$(Gsw5\text{-}Gsw2) = \sum_{N=1,5,7..}^{\infty} HAR_N \text{ SIN } N(\omega\tau+\phi N-240) \tag{3.83}$$

The input voltages may be set to

$$V_{XN} = V\cdot SIN(\omega\tau) \tag{3.84}$$

$$V_{YN} = V\cdot SIN(\omega\tau-120) \tag{3.85}$$

$$V_{ZN} = V\cdot SIN(\omega\tau-240) \tag{3.86}$$

Combining 3.81 to 3.86 and letting $\phi N=0$ for reference we obtain

$$V_{OUT}=V\cdot SIN(\omega\tau)\sum_{N=1,5,7..}^{\infty} HAR_N\cdot SIN(N\omega\tau) + V\cdot SIN(\omega\tau-120)\sum_{N=1,5,7..}^{\infty} HAR_N\cdot SIN\ N(\omega\tau-120+$$

$$V\cdot SIN(\omega\tau-240)\sum_{N=1,5,7..}^{\infty} HAR_N\cdot SIN(N\omega\tau-240) \tag{3.87}$$

Using the trigonometric expression of equation 3.63 we obtain

$$V_{OUT}= \sum_{N=1,5,7..}^{\infty} \frac{V\cdot HAR_N}{2}\left[\left[COS(N-1)\omega\tau - COS(N+1)\omega\tau\right] + \left[COS(N-1)(\omega\tau-120 - \right.\right.$$

$$\left.\left.COS(N+1)(\omega\tau-120)\right] + \left[COS(N-1)(\omega\tau-240) - COS(N+1)(\omega\tau-240)\right]\right] \tag{3.88}$$

From this expression it can be observed that for

(N-1) or (N+1) = 2, 4, 8, 10, 14.....∞,

the expression reduces to zero. As derived in chapter 3.1.3 this phenomenon is due to the summation of three phasor quantities at 0, 120, and 240 degree displacements. However if

(N-1) or (N+1) = 0, 6, 12.....∞,

the three resulting phasors coincide leading to

$$\mathcal{TF} = \frac{V_{OUT}}{V} = \frac{3}{2}\sum_{(N+1),(N-1)=0,6,12..}^{\infty} HAR_N\left[COS(N-1)\omega\tau - COS(N+1)\omega\tau\right] \quad (3.89)$$

Letting

$$\frac{V_{OUT}}{V} = \sum_{(N+1),(N-1)=0,6,12..}^{\infty} \frac{3}{2} HAR_N\left[COS(N-1)\omega\tau - COS(N+1)\omega\tau\right] = \sum_{N=0,6,12,18}^{\infty} RX_N\, S(N\omega\tau)$$

we obtain

$$\mathcal{TF} = \frac{V_{OUT}}{V} = \sum_{N=0,6,12,18}^{\infty} RX_N\, COS(N\omega\tau) \quad (3.90)$$

The per unit ratings used for the analysis are

V_{XN} = 1 pu peak

P_{IN} = .5 pu/phase = 1.5 pu total

3.2.1 Output Filter Rating

Only a single order inductive filter is required since the application of batteries implies a second order filter overall effect. The per unit battery voltage can be defined by known parameters. The rectifier must supply full

battery voltage at low line. Therefore

$$V_{BATMIN} = V_{MIN} \cdot \mathcal{TF}_{MAX} \text{ pu} \tag{3.91}$$

where V_{MIN} = Low input line voltage =.9 pu

$\mathcal{TF}_{MAX}$ = Maximum dc component converter gain

Altering 3.90 to accommodate for modulation index swing we have

$$\mathcal{TF}_{M} = \frac{V_{OUT}}{V} = \sum_{N=0,6,12,18}^{\infty} Rx_{N,M} \cos(N\omega\tau)$$

Therefore, the maximum converter gain can be found by letting

$N = 0$ & $M = 1$ as

$$V_{BATMAX} = V \cdot Rx_{0,1} = .9 \cdot Rx_{0,1} \tag{3.92}$$

To avoid battery damage maximum discharge is limited to 78% of maximum charge or

$$V_{BATMIN} = .78 \cdot .9 \cdot Rx_{0,1} \tag{3.93}$$

This leads to the minimum $\mathcal{TF}$ required ($\mathcal{TF}_{MIN}$) (assuming linear gain PWM) of

$$\mathcal{TF}_{MIN} = V_{BATMIN}/V_{MAX} \text{ pu} \tag{3.94}$$

where V_{MAX} = High input line voltage =1.1 pu

$\mathcal{TF}_{min}$ = minimum required converter gain

Evaluating equation 3.94 results in

$$\mathcal{TF}_{MIN} = .638 \cdot Rx_{0,1} \tag{3.95}$$

leading to

$$\frac{\mathcal{TF}_{MIN}}{Rx_{0,1}} = .638 \tag{3.96}$$

or

$$\mathcal{TF}_{MIN} = Rx_{0,.638}$$

Equations 3.92 and 3.93 immediately define the rectifiers output voltage swing as

$$.702 \cdot Rx_{0,1} \leq V_{OUT} \leq .9 \cdot Rx_{0,1} \tag{3.97}$$

Assuming only dc current through the inductor, the maximum output current results during lowest battery voltage or

$$I_{LOMAX} = \frac{P_{IN}}{V_{BATMIN}} = \frac{2.137}{Rx_{0,1}} \text{ pu} \tag{3.98}$$

It is generally desired to keep the current ripple in the output choke to below 5.5% of the maximum output current I_{DCMAX} where the ripple is defined as

$$I_{LO\_RIP} = \frac{100}{I_{LOMAX}} \sqrt{\sum_{N=6,12,18..}^{\infty} I_{LO_{N,M}}^2} \tag{3.99}$$

$$\text{where } I_{LO_{N,M}} = \frac{V_{LO_{N,M}}}{NX_{LO}}$$

Assuming only dc voltage appears across the battery terminals;

$$V_{LO_{N,M}} = Rx_{N,M} \text{ pu} \tag{3.100}$$

and

$$I_{LO\_RIP} = \frac{100}{\left[\frac{2.137}{Rx_{0,1}}\right]} \sqrt{\sum_{N=6,12,18..}^{\infty} \left[\frac{Rx_{N,M}}{NX_{LO}}\right]^2} \tag{3.101}$$

or

$$X_{LO} = \frac{100}{5.5\left[\frac{2.137}{Rx_{0,1}}\right]} \sqrt{\sum_{N=6,12,18..}^{\infty} \left[\frac{Rx_{N,M}}{N}\right]^2} \qquad (3.102)$$

The required worst case or largest filter inductor can be found by scanning through the modulation indexes (M) of the optimum PWM technique.

The most compatible PWM technique for controlled rectification has been identified in chapter 2.4 as MSPWM. As in the inverter stage analyses of chapter 3.1, switching stresses dictate that the switching frequency remain within the 21pu area at 60hz base frequency. Table T3.6 shows the derived harmonics content of the input line current pu harmonics as a function of modulation index for MSPWM with a switching frequency of 22 pu. The harmonics at full modulation index can be seen in fig F2.9 as the AC TERM spectrum.

	M				
N	.6	.7	.8	.9	1.0
1	.60	.70	.80	.90	1.0
5	0	0	0	0	0
7	0	0	0	0	0
11	0	0	0	0	0
13	0	0	0	0	0
17	0	0	0	0	0
19	0	0	0	0	0
23	.01	.01	.01	0	0
25	.01	.01	.01	.01	.01
29	.02	0	.03	.07	.11
31	.32	.33	.32	.29	.26
35	.32	.33	.32	.30	.26
37	.02	0	.03	.07	.11
41	.01	.01	.01	.01	.01
43	.01	.01	.01	.01	0
47	.01	.01	.01	.01	0
49	.01	.01	.01	.01	0
53	.01	.01	.01	.01	.01
55	.01	.02	.01	.01	.01
59	.03	.03	.01	.02	.05
61	.12	.14	.16	.15	.12
65	.17	.10	.03	.02	.05
67	.17	.10	.03	.02	.05
71	.12	.15	.16	.15	.12
73	.03	.03	.01	.01	.05
77	.01	.02	.02	.01	.01
79	.01	.01	.01	.01	.01
83	.01	.01	.01	.01	.01
85	.01	.01	.02	.02	.01
89	.02	.02	.02	0	.03
91	.04	.07	.10	.01	.08
95	0	0	0	0	0
97	0	0	0	0	0

Table T3.6 Input current harmonic content as a function of M

Figure F3.10 shows the harmonic content of the converter transfer function as the modulation index is varied. The figure is derived from equation 3.89 where HAR_N is altered with modulation index.

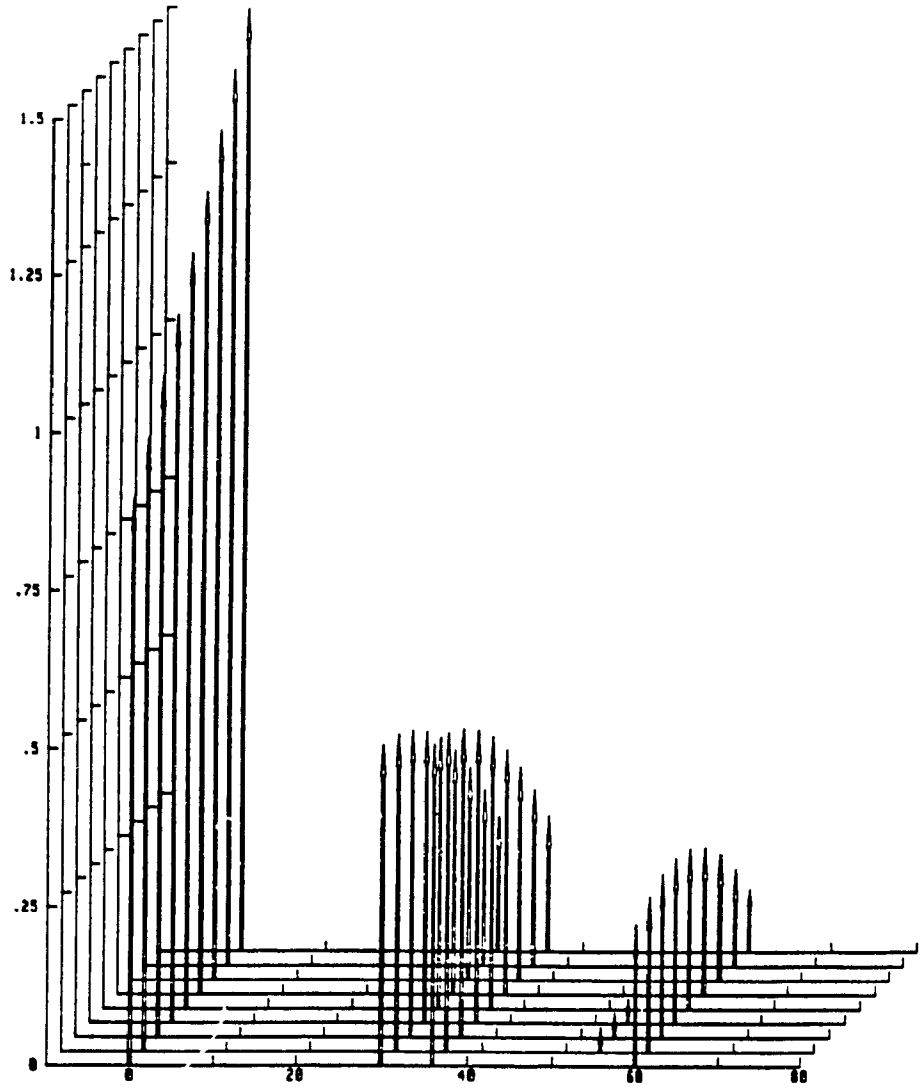


Figure F3.10 Controlled rectifier harmonic gains as a function of M

Figure F3.11 shows the required output filter 'X_{LO}' as a function of modulation index "M" based on equation 3.102. Worst case is observed at modulation index M = .638 or minimum modulation index, which defines the output filter.

$$X_{LO} = .294 \text{ pu}$$

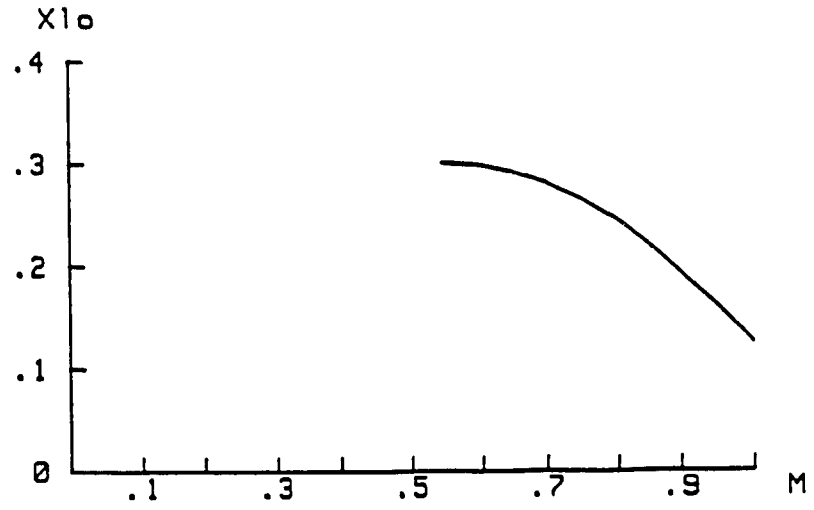


Figure F3.11 Required Output Inductor Impedance vs modulation index M

The rated current of the choke can be found from equation 3.98 and figure F3.10 resulting in

$$I_{LOMAX} = 1.425 \text{ pu.}$$

The rated voltage of the choke can be found from the worst case voltage harmonic across it used in equation 3.102.

$$V_{LORMS} = \sqrt{\sum_{N=6,12,18\ldots}^{\infty} \left[\frac{Rx_{N,M}}{\sqrt{2}} \right]^2} \qquad (3.103)$$

Where M = worst case found during X_{LO} search in equation 3.102

Figure F3.11 shows the worst case modulation index "M" to be .638 which results in

$$V_{LORMS} = .65 \text{ pu}$$

Further from figure F3.10

$$Rx_{0,1} = 1.5 \text{ pu}$$

which is confirmed by the dc gain specified in chapter 2.4.3.1 as

$$\text{DC gain} = .866 \text{ w.r.t. peak L-L input voltage}$$

translating into

$$.866 \cdot \sqrt{3} = 1.5 \text{ w.r.t peak L-N input voltage}$$

This further leads to the battery voltage swing defined by equation 3.97 as

$$1.053 \leq V_{OUT} \leq 1.350 \quad \text{pu}$$

3.2.2 Rectifier Switch Ratings

The rectifier output current I_{LO} can effectively be assumed harmonic free and continuous to simplify the power converter switch ratings while retaining accurate results.

Basic rectifier switching laws dictate that in figure F3.7 only one of the upper switches (SW1, SW3, SW5) and one of the lower switches (SW4, SW6, SW2) is conducting at any given instance. This implies that if the output current is continuous, then a switch is active and must conduct current. As in the inverter analysis the PWM scheme used defines the switch gating signals which may be represented in an array as

$$G_{SW1\_TD}(\omega\tau) = \begin{cases} 1 \text{ when SW1 is infinite conductance} \\ 0 \text{ when SW1 is infinite impedence} \end{cases} \qquad (3.104)$$

$$\text{where} \quad \omega\tau = 0,1,2,\ldots,360$$

Worst case switch currents will occur at maximum load current and relatively independent of the input line voltage. Since at all times one upper switch must conduct and the PWM technique is equally distributed, the average switch

current rating is

$$I_{SWAVE} = I_{LOMAX}/3 \tag{3.105}$$

Since

I_{DCMAX} =1.425 pu

I_{SWAVE} = .475 pu

Furthermore,

$$I_{SWRMS} = \sqrt{\frac{1}{3}}\, I_{LOMAX} \tag{3.106}$$

=.823 pu

The maximum switch voltage is computed directly from the input voltage swing as

$$V_{SWPK} = \sqrt{3}\, V_{XN} = \sqrt{3}\cdot 1.1 = 1.905 \text{ pu} \tag{3.107}$$

3.2.3 Input Filter Ratings

The input filter is added to improve the input power factor. The total input power factor can be segregated into two parameters;

1) Displacement power factor, which is the real part of the fundamental supply current in phase with the supply voltage and
2) Distortion power factor which is defined by the supply current harmonics which contribute no real power yet burden the lines.

If no input filter were used the displacement power factor would always be unity for the PWM control used here. Moreover, if the source impedance was low, virtually no input voltage THD would exist and all current harmonics could be supplied by the ac mains. The source impedance is expected to be low since the medium power level usually indicates a main hydro feed. [44] However, at high input lines and low battery voltage the distortion power

factor will force the total input power factor to be as low as .5 which is well below the requirements of chapter 2.2.

Placing a filter to compensate the power factor involves a capacitance which could deliver the harmonics and an inductance to isolate the capacitance from the stiff voltage supply. While alleviating the distortion power factor this process degrades the displacement power factor. Moreover, while the capacitors provide a low impedance path for the current harmonics, voltage distortion will be generated across its terminals presenting a non ideal 60hz supply to the rectifier bridge. A further drawback as a result of adding the filter is the voltage drop experienced. This is typically below 5% and is neglected during the component evaluation.

Many different parameters may be used as criteria for selecting actual filter component values including PF optimization, source current distortion, rectifier input voltage distortion, cost, [23], kVA, and weight among others. Power factor and rectifier input voltage distortion are used here because of their direct influence on the specifications given in chapter 2.2.

Figure F3.12 shows a simplified form of figure F3.7 suitable for input filter design analysis.

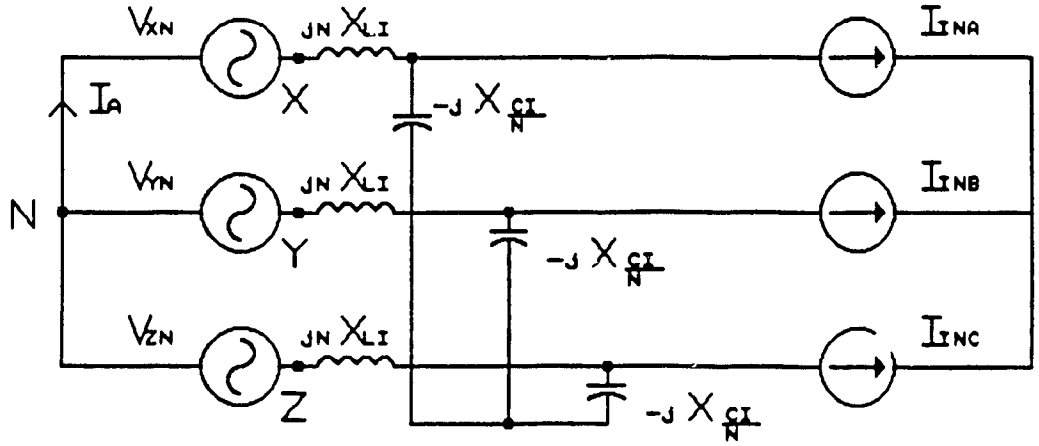


Figure F3.12 Simplified input stage for controlled rectifier

Under balanced conditions each of the three phases can be analyzed by an identical, equivalent circuit shown in figure F3.13 where

I_A =Total input current of source V_{XN}

I_{A_1} =Peak fundamental input current of source V_{XN}

I_{INA} =Total inverter input current of line A

I_{INA_1} =Peak fundamental inverter input current of line A

I_{CI} =Total capacitor current

V_{INA} =Inverter input voltage using neutral point

V_{LI} =Input inductor filter voltage

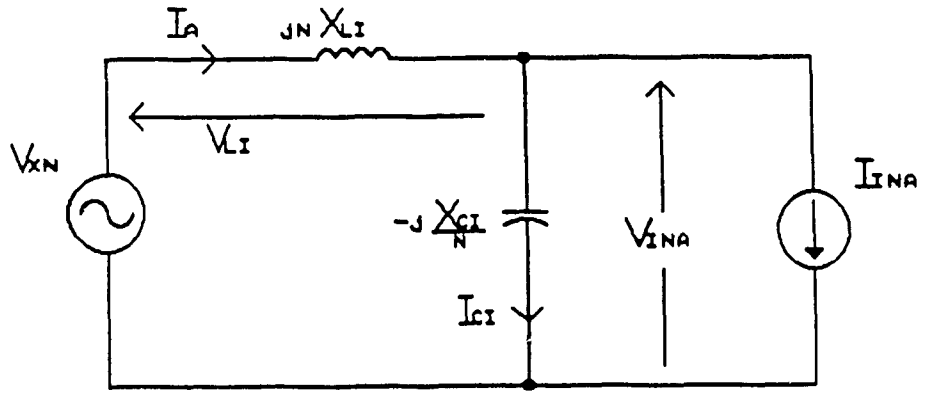


Figure F3.13 Single phase equivalent input circuit

Optimizing the two element filter for two different objectives involves two independent equations. The first criteria involves setting the input power factor to .9 under worst case conditions. Total input power factor can be expressed as,

$$TIPF = \frac{I_{A_1} \cdot COS(\theta)}{I_A} \qquad (3.108)$$

where θ =displacement angle between V_{XN} and I_{A_1}

The input current I_A is given by

$$I_A = \sqrt{I_{A_1}^2 + \sum_{N=5,7,11..}^{\infty} I_{A_N}^2} \quad pu \tag{3.109}$$

$$= \sqrt{(I_{CI_1} + I_{INA_1})^2 + \sum_{N=5,7,11..}^{\infty} I_{A_N}^2} \quad pu \tag{3.110}$$

where I_{CI_1} =peak fundamental current of capacitor C_I

I_{A_N} =peak amplitude of N'th component of current I_A

Since

$$I_{CI_1} = j \frac{V_{INA_1}}{X_{CI}} \quad pu \tag{3.111}$$

where

V_{INA_1} = peak fundamental inverter input voltage

and

$$I_{INA_1} = \frac{2\ P_{IN}}{3\ V_{INA_1}} = \frac{2\ P_{OUT}}{3\ V_{INA_1}} \tag{3.112}$$

we have

$$I_{A_1} = \frac{2\ P_{OUT}}{3\ V_{INA_1}} + j \frac{V_{INA_1}}{X_{CI}} \tag{3.113}$$

The magnitude is given by

$$|I_{A_1}| = \sqrt{\left[\frac{2\ P_{OUT}}{3\ V_{INA_1}}\right]^2 + \left[\frac{V_{INA_1}}{X_{CI}}\right]^2} \tag{3.114}$$

Further, since

$$I_{A_N} = \sum_{N=5,7,11..}^{\infty} I_{INA_N} \cdot \frac{1}{1-N^2 X_{LI}/X_{CI}} \tag{3.115}$$

where I_{INA_N} peak amplitude of N'th component of I_{INA}

we have

$$I_A = \sqrt{\left[\frac{2 \cdot P_{OUT}}{3 \cdot V_{INA_1}}\right]^2 + \left[\frac{V_{INA_1}}{X_{CI}}\right]^2 + \sum_{N=5,7,11..}^{\infty} \left[I_{INA_N} \frac{1}{1-N^2 X_{LI}/X_{CI}}\right]^2} \tag{3.116}$$

Solving angle θ, requires only the fundamental component phases for V_{XN} and I_A. Using V_{INA} as the adopted reference phase "zero" we set

$$V_{INA} \Rightarrow \quad V_{INA} \angle 0 \tag{3.117}$$

and from equation 3.113 we may obtain

$$\theta I_{A_1} = \text{ARCTAN}\left[\frac{3 \cdot V_{INA_1}^2}{2 \cdot X_{CI} \cdot P_{OUT}}\right] \tag{3.118}$$

Solving the fundamental inductor voltage we have

$$V_{LI_1} = jI_{A_1} \cdot X_{LI} \tag{3.119}$$

$$= j\frac{2 \cdot P_{OUT} \cdot X_{LI}}{3 \cdot V_{INA_1}} - \frac{V_{INA_1} \cdot X_{LI}}{X_{CI}} \tag{3.120}$$

where V_{LI_1} =peak fundamental voltage across inductor LI

The supply voltage required to combine the equations is

$$V_{XN} = V_{LI_1} + V_{INA_1} \tag{3.121}$$

$$= V_{INA_1}\left[1 - \frac{X_{LI}}{X_{CI}}\right] + j\left[\frac{2 \cdot P_{OUT} \cdot X_{LI}}{3 \cdot V_{INA_1}}\right] \tag{3.122}$$

giving the phasor angle of supply voltage as

$$\theta V_{XN} = \text{ARCTAN}\left[\frac{2 \cdot P_{OUT} \cdot X_{LI}}{3 \cdot V_{INA_1}^{2} \cdot (1 - X_{LI}/X_{CI})}\right] \tag{3.123}$$

Substituting equations 3.123, 3.118, 3.113 and 3.116 into 3.108 we obtain

$$TIPF = \frac{\sqrt{\left[\frac{2\ P_{OUT}}{3\ V_{INA_1}}\right]^2 + \left[\frac{V_{INA_1}}{X_{CI}}\right]^2}}{\sqrt{\left[\frac{2 \cdot P_{OUT}}{3 \cdot V_{INA_1}}\right]^2 + \left[\frac{V_{INA_1}}{X_{CI}}\right]^2 + \sum_{N=5,7,11..}^{\infty}\left[I_{INA_N}\frac{1}{1 - N^2 X_{LI}/X_{CI}}\right]^2}} \cdot$$

$$\frac{\cos\left[\text{ARCTAN}\left[\frac{2 \cdot P_{OUT} \cdot X_{LI}}{3 \cdot V_{INA_1}^{2} \cdot (1 - X_{LI}/X_{CI})}\right] - \text{ARCTAN}\left[\frac{3 \cdot V_{INA_1}^{2}}{2 \cdot X_{CI} \cdot P_{OUT}}\right]\right]}{\sqrt{\left[\frac{2 \cdot P_{OUT}}{3 \cdot V_{INA_1}}\right]^2 + \left[\frac{V_{INA_1}}{X_{CI}}\right]^2 + \sum_{N=5,7,11..}^{\infty}\left[I_{INA_N}\frac{1}{1 - N^2 X_{LI}/X_{CI}}\right]^2}} \tag{3.124}$$

As previously mentioned, the addition of a filter creates inverter input

voltage distortion. The distortion is minimized by proper selection of LI and CI given by the total harmonic distortion (THD) expression;

$$V_{INATHD} = \frac{100}{V_{INA_1}} \sqrt{\sum_{N=5,7,11..}^{\infty} \left[I_{INA_N} \left[\frac{X_{LI} \cdot X_{CI}}{NX_{LI} - X_{CI}/N} \right] \right]^2} \qquad (3.125)$$

The typically accepted safe valve for rectifier input voltage THD is 5%.

Equations 3.124 and 3.125 represent two nonlinear equations with two variables. XLI and XCI can be solved given worst case values of V_{INA_1}, Pout and I_{INA_N}. The current IINA is solved by multiplying in the frequency domain, the rectifier output current ILO by the power converter transfer characteristic [41] or

$$I_{INA} = (G_{SW1} - G_{SW4}) \cdot I_{LO} \qquad (3.126)$$

where (Gsw1 - Gsw4) is given as equation 3.81

Safely assuming that ILO is only a DC level current greatly simplifies equation 3.126 and stabilizes the relative harmonic content with respect to the fundamental of IINA. In this fashion the worst harmonic current should lead to the lowest input distortion power factor. The worst harmonic content occurs at lowest modulation index which occurs at maximum input voltage V_{INA_1} and lowest battery voltage. Furthermore since input power factor tends to decrease as output power decreases, worst case POUT will exist at the lowest power in which the specifications dictate power factor criteria to be kept.

It is safe to assume that V_{INA_1} will not excessively exceed VXN. At V_{INA_1} equal to high line or 1.1 pu, battery voltage is at its minimum level of (from equation 3.93)

$$V_{BATMIN} = .78 \times .9 \times 1.5 = 1.053 \text{ pu}$$

The rectifier minimum output power level while still maintaining .9 power

factor is

$$P_{OUT} = .75 \text{ pu.}$$

Using these two parameters Table T3.7 was constructed listing the rectifier input line current spectrum.

N	I_{INA_N}
1	.45
5	0
7	0
11	0
13	0
17	0
19	0
23	.01
25	.01
29	.01
31	.23
35	.23
37	.01
41	.01
43	.01
47	.01
49	.01
53	.01
55	.01
59	.02
61	.09
65	.10
67	.10
71	.09
73	.02
77	.01
79	.01
83	.01
85	.01
89	.01
91	.04

Table T3.7 Rectifier input current spectrum for worst case input filter calculations

Substituting these values into equations 3.124 and 3.125 results in

$$TIPF = \frac{\sqrt{.2066 + \frac{1.21}{X_{CI}^2}} \cdot \cos\left[\arctan\left[\frac{.4132 \cdot X_{LI}}{1 - X_{LI}/X_{CI}}\right] - \arctan\left[\frac{2.42}{X_{CI}}\right]\right]}{\sqrt{.2066 + \frac{1.21}{X_{CI}^2} + \sum_{N=5,7,11..}^{\infty} \left[\frac{I_{INA_N}}{1 - N^2 X_{LI}/X_{CI}}\right]^2}} \tag{3.127}$$

$$V_{INATHD} = 5 = \frac{100}{V_{INA_1}} \sqrt{\sum_{N=5,7,11..}^{\infty} \left[I_{INA_N}\left[\frac{X_{LI} \cdot X_{CI}}{NX_{LI} - X_{CI}/N}\right]\right]^2} \tag{3.128}$$

Evaluation of these equations simultaneously results in

$$X_{LI} = .05 \text{ pu}$$

and

$$X_{CI} = 4.8 \text{ pu}$$

Worst case capacitive current ratings will occur at maximum output power and minimum modulation index which gives the highest amount of ripple currents as well as fundamental current due to high line input voltage V_{IN_1}. The expression for rms capacitor current is;

$$I_{CIRMS} = \frac{1}{\sqrt{2}} \sqrt{I_{CI_1}^2 + \sum_{N=5,7,11..}^{\infty} I_{CI_N}^2} \tag{3.129}$$

where $$I_{CI_1} = V_{INA_1}/X_{CI} \tag{3.130}$$

$$I_{CI_N} = \frac{I_{IN_N}}{1 - X_{CI}/X_{LIN}^2} \tag{3.131}$$

I_{IN_N} = N'th harmonic component of I_{IN}

I_{IN} = worst case rectifier input line current harmonics at lowest modulation index and rated load

Table T3.7 shows that the rectifier harmonic input currents at high line and minimum battery voltage are applicable for worst case capacitor current ratings also. Since

$$V_{INA_1} = 1.1 \text{ pu}$$

and

$$X_{CI} = 4.8 \text{ pu}$$

we obtain

$$I_{CI_1} = .229 \text{ pu}$$

Moreover, I_{CI_N} can be simplified to

$$I_{CI_N} = \frac{I_{IN_N}}{1-96N^2} \tag{3.132}$$

resulting in (from equation 3.129)

$$I_{CIRMS} = \frac{1}{\sqrt{2}} \sqrt{.052 + \sum_{N=5,7,11..}^{\infty} \left[\frac{I_{IN_N}}{1-96/N^2} \right]^2} \tag{3.133}$$

After evaluation, equation 3.133 results in

$$I_{CIRMS} = .34 \text{ pu}$$

The worst case inductor current occurs when the highest expected fundamental current component supplied by the source is present. This is found from

$$I_{LIRMS} = \frac{\sqrt{2} \cdot P_{IN}}{3V_{XN} \cdot \cos(\theta I_{A_1} - \theta V_{XN})} \qquad (3.134)$$

where V_{XN} = minimum input peak voltage

θI_{A_1} = solved from equation 3.118

θV_{AN} = solved from equation 3.123

P_{IN} = rated output power

Evaluation of 3.134 leads to

I_{LIRMS} =.788 pu

3.3 High Frequency Link Evaluation

High frequency link converters are not new and an enormous amount of topologies exist [45]. This mandates a screening stage to limit the possible options for analysis. An appropriate basis for categorizing the converter is by the number of power semiconductors employed. It is generally accepted that for reliability, simplicity and cost purposes, the converter topology employing the lowest number of power semiconductors capable of doing the task will be chosen. Proceeding from this basis the topology with most potential in each category (1, 2, 4 switches) is evaluated leading to the most suitable choice for the application. The preceding chapters (3.1 and 3.2) have revealed distinct terminal per unit voltage quantities required for proper operation. The rectifier will supply voltage of

$$1.053 \text{ pu} < V_{BAT} < 1.35 \text{ pu}$$

and the inverter requires an input voltage of

$$1.53 \text{ pu} < V_{DCBUS} < 1.93 \text{ pu}$$

These values must therefore be processed by the high frequency link. Based on topology, the knowledge of the terminal quantities results in immediate selection of required transformer turns ratio which simplifies further per unit ratings of components. Moreover, per unit component stresses (voltage, current and power) are evaluated assuming reactive components much larger than actually required to further simplify comparison. (ie inductances and capacitances are assumed to be infinite for voltage and current ratings). This is followed by actual component value derivations.

3.3.1 Single Switch Evaluation

The simplified forward converter is shown in figure F3.14

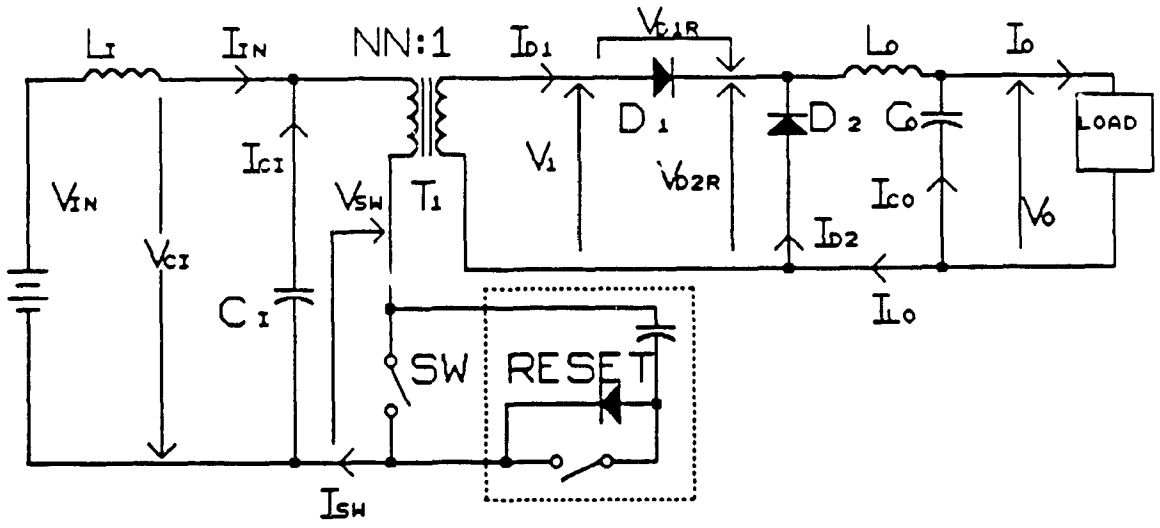


Figure F3.14 Single switch forward converter

This is the simplest topology of High Frequency (HF) Links evaluated in this sub-chapter. The lack of complexity is a distinct advantage and the topology is commonly used for relatively lower power applications mainly due

to high current ripple and semiconductor stresses. However with the recent emergence of higher performance semiconductor devices and capacitors recently, the topology may make a viable yet simple HF link option. Of major concern, and as shown in figure F3.14 is the means by which the power transformer can be reset. Several techniques similar to the one shown here exist [46] [47] and have proven themselves to be suitable in industrial SMR applications. Specializedresetting techniques allow a duty cycle higher than the traditional maximum of 50% while at the same time permit bidirectional magnetizing current flow. This advantage usually results in higher semiconductor voltages and in practical applications limit the duty cycle to approximately 70% for a rectified 208 volt input line voltage. Not to underestimate this topology; the evaluation here assumes a good resulting technique is applied and duty cycle can swing as high as 75%. This would limit the switching power semiconductor reverse voltage to roughly 650 volts as shown in the following discussion. The limit is used since it approaches the limit for practical MOSFET semiconductors. Moreover, the following assumptions are also utilized;

1) The switch and diodes are ideal
2) Capacitors and inductors are lossless
3) The transformer is ideal
4) The source is ideal
5) The load is purely resistive
6) The effect of any di/dt or dv/dt limiting is neglected
7) Stray parasitics are neglected

Component stress values can be derived with the aid of typical waveforms shown in figure F3.15.

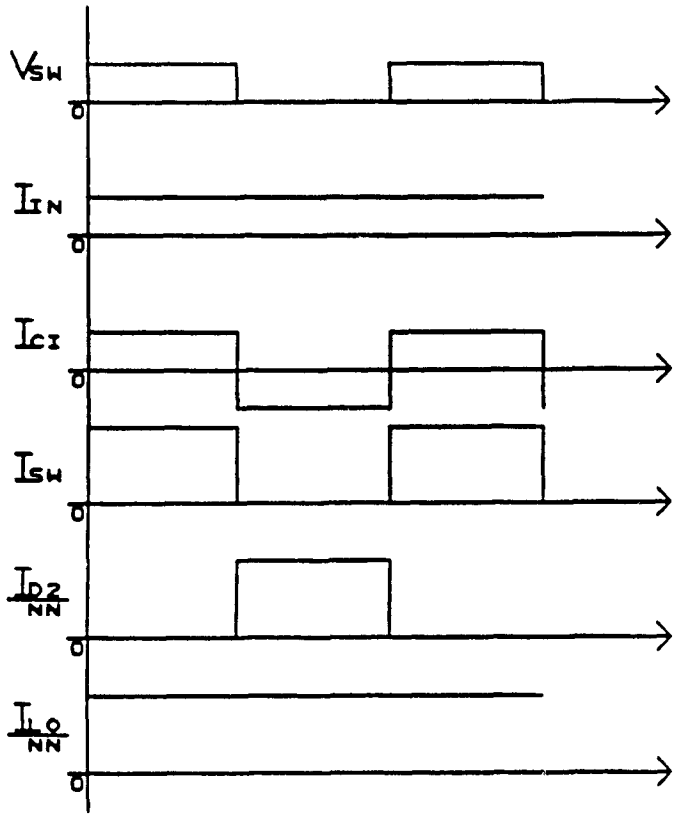


Figure F3.15 Forward converter typical waveforms

The duty cycle "D" relates the terminal voltages by

$$D = \frac{V_O \cdot NN}{V_{IN}} \tag{3.135}$$

Setting the maximum duty cycle to .75 we have

$$D_{MAX} = .75$$

which allows setting of the transformer turns ratio as

$$NN = \frac{D_{MAX} \cdot V_{INMIN}}{V_{OMAX}} \tag{3.136}$$

$$D = \frac{V_O \cdot NN}{V_{IN}}$$

Evaluation of 3.136 results in

$$NN = .409$$

Further, the minimum duty cycle "DMIN" is

$$DMIN = \frac{VOMIN \cdot NN}{VINMAX} = .4635 \tag{3.137}$$

Capacitor CI will have an rms current

$$ICIRMS = \sqrt{\frac{1}{T}\int_0^T ICI^2 dT}$$

$$= \sqrt{\frac{1}{T}\int_0^{DT} IIN^2\left[\frac{1}{D} - 1\right]^2 dT + \frac{1}{T}\int_{DT}^{T} -IIN^2\, dT}$$

$$= IIN\sqrt{D\left[\frac{1}{D} - 1\right]^2 + \left[1 - D\right]} = IIN\sqrt{\frac{1}{D} + D - 2 + 1 - D}$$

$$= IIN\sqrt{\frac{1}{D} - 1} = IIN\sqrt{\frac{VIN}{VO \cdot NN} - 1} = \frac{PIN}{VIN}\sqrt{\frac{VIN}{VO \cdot NN} - 1}$$

$$= \frac{1.5}{VIN}\sqrt{\frac{VIN}{VO \cdot .409} - 1} \tag{3.138}$$

The worst case occurs when the duty cycle (D=.5) is associated with a minimum possible input voltage.

Therefore when

$$VIN = 1.25 \text{ pu}$$

and $$VO = 1.53 \text{ pu},$$

$$ICIRMS = 1.2 \text{ pu}$$

The critical ratings for the power switch are ISWAVE, ISWRMS, ISWPK and

VSWPK.

The switch current is given by

$$I_{SW} = I_{CI} + I_{IN} = \begin{cases} I_{IN}/D & 0 \le t \le DT \\ 0 & DT \le t \le T \end{cases} \tag{3.139}$$

The average switch current can be derived as

$$I_{SWAVE} = \frac{1}{T}\int_0^{DT} \frac{I_{IN}}{D}\, dT = I_{IN} = \frac{P_{IN}}{V_{IN}} \tag{3.140}$$

Worst case will occur at low input voltage where

$$I_{SWAVE} = 1.5/1.053 = 1.4245 \text{ pu}$$

Similarly the rms switch current is given by

$$I_{SWRMS} = \sqrt{\frac{1}{T}\int_0^{DT} \left[\frac{I_{IN}}{D}\right]^2 dT} \tag{3.141}$$

$$= I_{IN}\sqrt{\frac{1}{D}} \quad = I_{IN}\sqrt{\frac{V_{IN}}{V_O \cdot NN}} \quad = P_{IN}\sqrt{\frac{1}{V_{IN} \cdot V_O \cdot NN}}$$

$$= 1.5\sqrt{\frac{1}{V_{IN} \cdot V_O(.409)}} \tag{3.142}$$

Worst case occurs at minimum input and output voltages or

$$V_{IN} = 1.05 \text{ pu} \qquad \text{and} \qquad V_O = 1.53 \text{ pu}$$

resulting in

$$I_{SWRMS} = 1.85 \text{ pu.}$$

The volt seconds balance of the transformer shows that

$$V_{IN} \cdot D = V^{\bullet}(1-D) \tag{3.143}$$

where $V^{\bullet}$ = reverse voltage across the transformer

Rearranging we have

$$V^{\bullet} = \frac{V_{IN} \cdot D}{1-D} \tag{3.144}$$

The switch voltage can be found from

$$V_{SWPK} = V^{\bullet} + V_{IN} \tag{3.145}$$

$$= \frac{V_{IN}}{1-D} = \frac{V_{IN}}{1-V_O \cdot NN/V_{IN}} = \frac{V_{IN}^2}{V_{IN} - V_O(.409)} \tag{3.146}$$

Worst case occurs at maximum duty cycle and yields

$$V_{SWPK} = 4.21 \text{ pu}$$

The peak switch current is found from

$$I_{SWPK} = (I_{IN} + I_{CI})_{t=DT} \tag{3.147}$$

$$= \frac{I_{IN}}{D} = \frac{I_{IN} \cdot V_{IN}}{V_O \cdot NN} = \frac{P_{IN}}{V_O \cdot NN} = \frac{1.5}{V_O \cdot (.409)} \tag{3.148}$$

Therefore at worst case when the minimum output voltage is present resulting in

$$I_{SWPK} = 2.397 \text{ pu}$$

Significant diode ratings include I_{DAVE} and V_{DR}

where I_{DAVE} =average diode current

V_{DR} =peak reverse diode voltage

For diode D_1

$$I_{D1AVE} = I_{SWAVE} \cdot NN \tag{3.149}$$

$$= 1.425 \times .409 = .5828 \text{ pu}$$

V_{D1R} can be found by altering equation 3.143 as

$$V_{D1R} = \frac{V_{IN} \cdot D}{(1-D) \cdot NN} = \frac{V_O \cdot NN}{(1-D) \cdot NN} = \frac{V_O}{(1-D)} \tag{3.150}$$

Worst case for V_{D1R} will exist at maximum duty cycle resulting in

$$V_{D1R} = 7.72 \text{ pu}$$

For diode D_2 the average current is

$$I_{D2AVE} = I_{SWPK} \cdot (1-D) \cdot NN \tag{3.151}$$

At worst case which occurs at minimum duty cycle

$$I_{D2AVE} = 2.397 \cdot (1-.4635) \cdot .409 = .53 \text{ pu}$$

Further

$$V_{D2R} = \frac{V_{IN}}{NN} \tag{3.152}$$

which at worst case yields

$$V_{D2R} = 3.3 \text{ pu}$$

The output filter inductor carries an rms current of

$$I_{LORMS} = \frac{P_{IN}}{V_O} \tag{3.153}$$

Therefore at worst case or minimum output voltage

$$I_{LORMS} = 1.5/1.53 = .98 \text{ pu}$$

The output filter capacitor has ideally zero ripple current or

$$I_{CORMS} = 0.0 \text{ pu}$$

Another parameter that offers significant insight into topology evaluation is the isolation power transformer size. Transformer size when

dealing with ferrite materials is limited by two parameters; flux swing and losses. At 10 kVA and expected operating frequencies of 20khz-40khz both parameters are expected to be equally dominant in limiting the core size. This allows the size of the transformer to be approximated by either parameter. The flux swing limitation is used here to approximate a relative size. The parameter most often used for ferrite transformer sizing is the core area product 'Ap' [48].

$$A_P = A_W A_E = \left[\frac{P_{IN} \cdot 10^4}{K_T \cdot K_U \cdot K_P \cdot 420 \cdot K_B \cdot \Delta B \cdot 2F_{SW}} \right]^{1.31} \qquad (3.154)$$

where A_P = area product

A_W = core window area

A_E = magnetic core cross section area

P_{IN} = power transfer

K_U = window utilization factor

K_T = topology factor

K_P = primary area factor

F_{SW} = switching frequency

ΔB = core flux swing

K_B = allowable flux swing

In a forward topology;

$$K_U = .4$$

This is a standard level which is not surprisingly low when considering insulation and creepage requirements required by regulatory agencies. Moreover from empirical equations [48] $K_T = .71$ and $K_P = .5$

Because of the nonlinear nature of equation 3.154, the equation can be

normalized to simplify the relative comparison between topologies. This results in

$$A_P^* = \frac{A_P}{\left[\frac{P_{IN}}{\Delta B \cdot F_{SW}}\right]^{1.31}} = \left[\frac{10^4}{K_T \cdot K_U \cdot K_P \cdot 420 \cdot K_B \cdot 2}\right]^{1.31} \qquad (3.155)$$

Typical forward converters allow $K_B = .25$ however with core resetting and duty cycle excursion until D = .75 as assumed here

$$K_B = .375$$

Therefore,

$$A_P^* = \left[\frac{10^4}{2(.71)(.4)(.5)(420)(.375)}\right]^{1.31} = 1196$$

The derived current and voltage per unit stresses as well as transformer relative size help to provide a semi-complete set of component ratings leading to topology segregation. The parameters however were derived with infinite reactive component values. To further complete the data, actual values of inductors and capacitors are required.

The output filter is a second order type in which the inductance and capacitance values can be solved separately. The values solved in this section assume only a resistive load. However, in the final design when the high frequency link provides energy to the inverter stage, the actual filter required will not only depend on the HF link design, but also on the inverter stage design. Nevertheless, the topology design influences the harmonics the filter will have to attenuate from the front end. In this context the size of Lo and Co based solely on the link topology is a good estimate of the design's effectiveness. The typical waveforms are shown in figure F3.16.

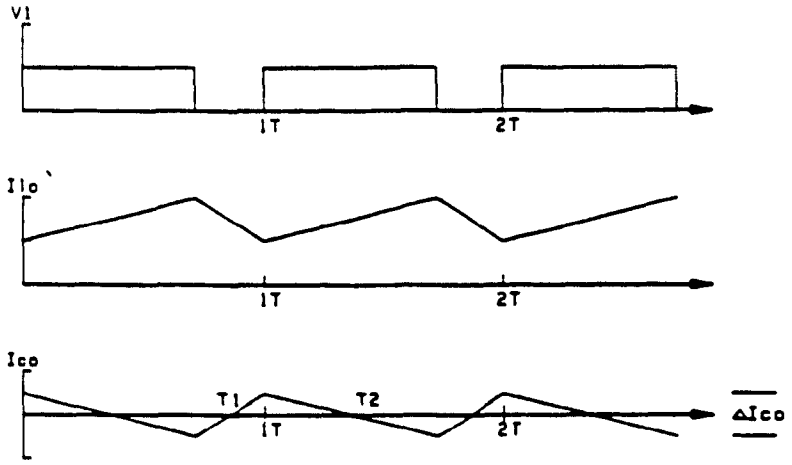


Figure F3.16 Forward converter typical output waveforms

Lo can be calculated from the equation

$$V_{LO} = L_O \frac{d}{dt} I_{LO} \tag{3.156}$$

During the off time

$$V_{LO} = V_O \tag{3.157}$$

Further, the off time during application of Vo can be calculated from

$$dt = T_{OFF} = (1-D)\cdot T = \left[\frac{1 - V_O \cdot NN/V_{IN}}{F_{SW}} \right] \tag{3.158}$$

In order to keep relatively low output ripple and low peak switch current it is sufficient that the ripple "ΔIo" superimposed on the dc output current be

$$\Delta I_{LO} \leq .25\ I_O \tag{3.159}$$

Substituting equations 3.159, 3.158 and 3.157 into 3.156 leaves

$$L_O = \frac{V_O \cdot T_{OFF}}{.25 \cdot I_O} \tag{3.160}$$

In a per unit basis analysis where

$$X_{LO} = \omega L_O = 2\pi \cdot F_{SW} \cdot L_O \tag{3.161}$$

we obtain

$$X_{LO} = \frac{V_O \cdot T_{OFF} \cdot 2\pi \cdot F_{SW}}{.25 \cdot I_O}$$

$$= \frac{V_O^2}{.25 \cdot P_{OUT}} \left[\frac{1 - V_O \cdot NN/V_{IN}}{F_{SW}} \right] \cdot 2\pi \cdot F_{SW}$$

$$= \frac{8\pi \cdot V_O^2}{P_{OUT}} \left[1 - \frac{V_O \cdot NN}{V_{IN}} \right] \tag{3.162}$$

At worst case, when Maximum V_O and V_{IN} exists

$$X_{LO} = 25.92 \text{ pu}$$

Using figure F3.16 the current passing through the capacitor will create a ripple voltage across it and the output according to

$$\Delta V_O = \frac{1}{C_O} \int_{T1}^{T2} I_{CO} \, dT \tag{3.163}$$

Based on a geometrical law, the integration of Ico will result in the area above the zero level from T1 to T2 being

$$\int_{T1}^{T2} I_{CO} \, dT = \text{ average height X length } = \frac{\Delta I_{CO}}{4} \cdot \frac{T}{2} \tag{3.164}$$

Therefore

$$\Delta Vo = \frac{\Delta Ico}{4} \cdot \frac{1}{2Fsw} \cdot \frac{1}{Co} \tag{3.165}$$

and since

$$\Delta Ico = \Delta I_{LO} = .25 \cdot Io$$

we have

$$\Delta Vo = \frac{Io}{32 \cdot Co \cdot Fsw}$$

or

$$Co = \frac{Io}{32 \cdot Fsw \cdot \Delta Vo} \tag{3.166}$$

Since this application dictates a low ripple voltage of

$$\Delta Vo = .05 \cdot Vo \tag{3.167}$$

$$Co = \frac{Io}{Vo \cdot 1.6 \cdot Fsw} \tag{3.168}$$

When altered into a frequency independent format for per unit levels

$$Xco = \frac{1}{\omega Co} = \frac{1}{2\pi \cdot Fsw \cdot Co} \tag{3.169}$$

Substitution of equation 3.168 into 3.169 yields

$$Xco = \frac{Vo^2 \cdot 1.6}{2\pi \cdot P_{OUT}} \tag{3.170}$$

The worst case for Xco is evident when Vo is minimum and equation 3.170 yields

$$Xco = \frac{1.53^2 \cdot 1.6}{2\pi \cdot 1.5} = .397 \text{ pu} \tag{3.171}$$

The input filter parameters are solved in a similar fashion starting with the equivalent circuit of figure F3.17. and waveforms of figure F3.18.

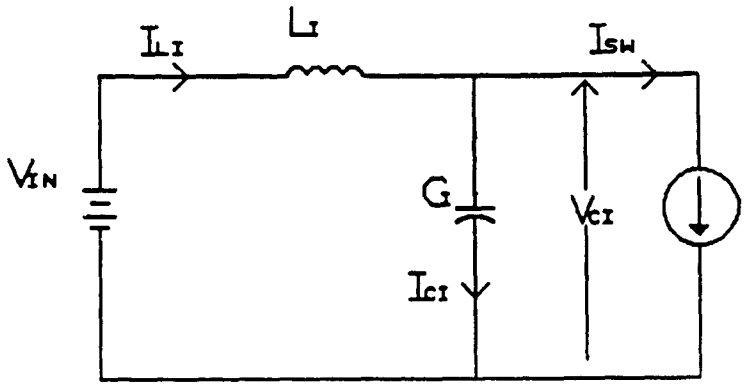


Figure F3.17 HF link equivalent input circuit

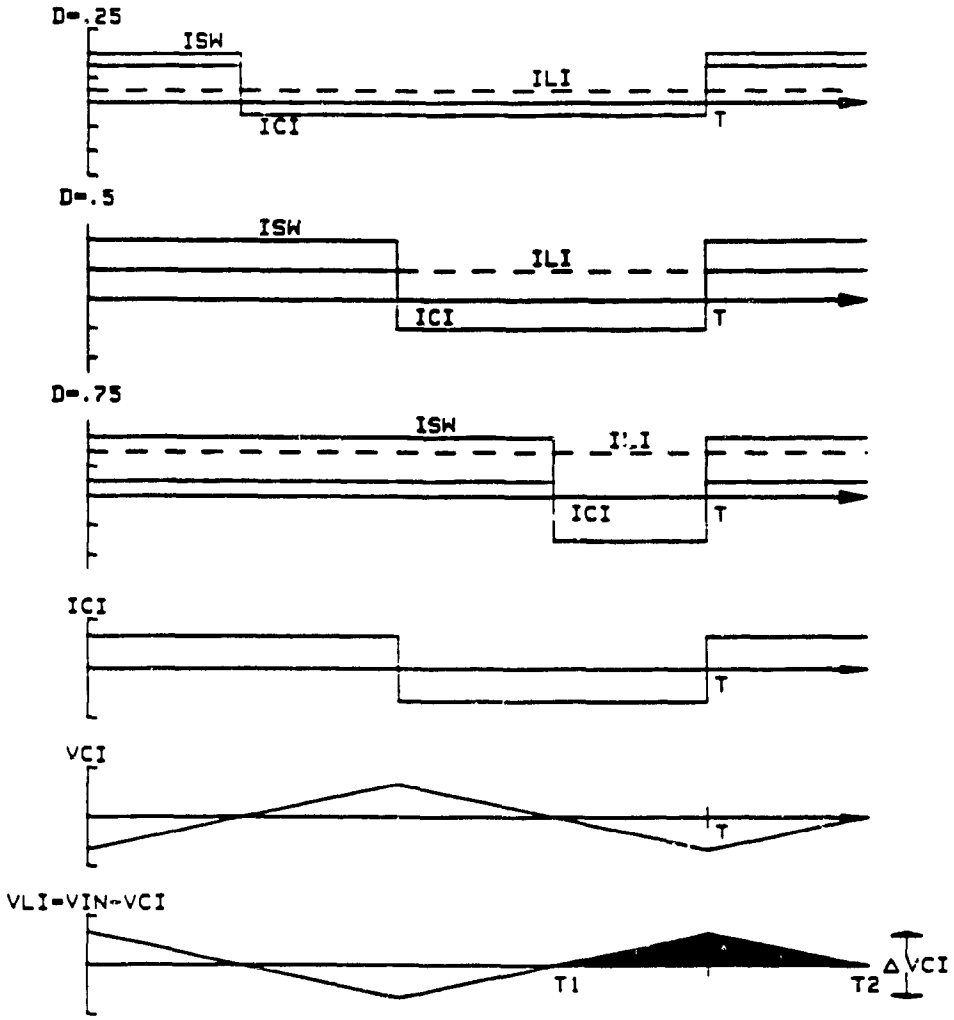


Figure F3.18 HF link equivalent input circuit waveforms

As in many power supply applications this equivalent circuit delivers constant power to its load. This indicates that duty cycle is relatively independent of load and heavily dependant on input voltage fluctuations. Moreover, it dictates that the peak current level is constant throughout duty cycle variation. Figure F3.18 shows that the normalized "Ic·t" product for a positive excursion is largest for duty cycle = 50%. Further since

$$\Delta Q_{CI} = I_{CI} \cdot \Delta t \quad \text{or} \quad \Delta V_{CI} \propto (I_{CI} \cdot t) \tag{3.172}$$

implying that the greatest ripple voltage will occur when

1) the load is full (max current) and

2) the duty cycle is 50%.

Current through the input capacitor is given by

$$I_{CI} = C_I \frac{d}{dt} V_{CI} \tag{3.173}$$

The positive peak level of I_{CI} is given as

$$I_{CPOS} = \left[\frac{1-D}{D} \right] \cdot I_{IN} \tag{3.174}$$

Further we also have

$$I_{IN} = \frac{P_{IN}}{V_{IN}} \tag{3.175}$$

and $D = .5$

equation 3.173 becomes after rearranging terms

$$\Delta V_{CI} = \frac{P_{IN}}{V_{IN} \cdot C_I} \cdot \Delta t \tag{3.176}$$

Further

$$\Delta t = .5 \cdot T \tag{3.177}$$

Since a widely accepted ripple voltage at the input capacitor is 15%

$$\Delta V_{CI} = .15 \cdot V_{IN} \tag{3.178}$$

we have after rearranging terms of equation 3.176

$$C_I = \frac{3.334 \cdot P_{IN}}{F_{SW} \cdot V_{IN}^2} \tag{3.179}$$

or in frequency independent form

$$X_{CI} = \frac{V_{IN}^2}{2\pi \cdot (3.334) \cdot P_{IN}} \tag{3.180}$$

V_{IN} at its lowest value represents the worst case where equation 3.180 yields

$$X_{CI} = \frac{1.053^2}{2\pi \cdot (3.334) \cdot 1.5} = .0353pu$$

It can further be extrapolated that as the ripple voltage across the capacitor worsens, the ripple current through the filter choke also increases because

$$I_{LI} = \frac{1}{L_I} \int_{T1}^{T2} V_{LI}\, dT \tag{3.181}$$

Using the waveforms of figure F3.18 and geometric rules the shaded sections area is

$$\text{shaded area} = .25 \cdot \Delta V_{CI} \cdot T/2 \tag{3.182}$$

implying that

$$\Delta I_{LI} = \frac{1}{L_I} \cdot \frac{.25 \cdot \Delta V_{CI}}{2 \cdot F_{SW}} \tag{3.183}$$

Using equation 3.178 and nominally accepted battery ripple current of 5% or

$$\Delta I_{LI} = .05 \cdot I_{IN} = \frac{.05 \cdot P_{IN}}{V_{IN}} \tag{3.184}$$

we obtain

$$L_I = \frac{.25 \cdot .15 \cdot V_{IN}^2}{.05 \cdot P_{IN} \cdot F_{SW} \cdot 2} \tag{3.185}$$

Conversion to frequency independent base yields

$$X_{LI} = \frac{2\pi \cdot .375 \cdot V_{IN}^2}{P_{IN}} \tag{3.186}$$

In contrast to the earlier derived input capacitor rating, worst case for the reactor results at maximum input voltage yielding

$$X_{LI} = \frac{2\pi \cdot (.375) \cdot 1.35^2}{1.5} = 2.86 \text{ pu}$$

The equations derived in this section are utilized in a critical comparative scenario in chapter 3.4.

3.3.2 Half Bridge Evaluation

The simplified half bridge converter is shown in figure F3.19.

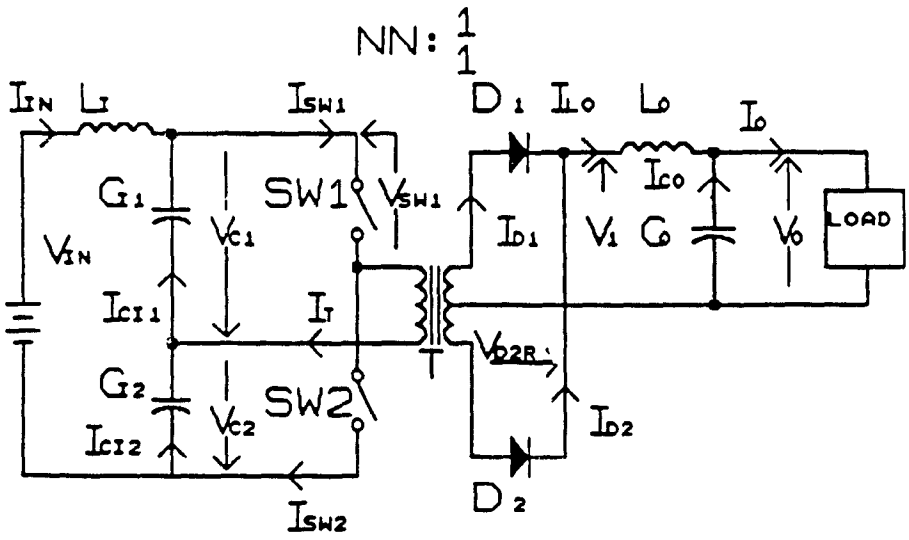


Figure F3.19 Simplified half bridge inverter power train

The two major distinctions of this bridge with reference to the forward converter presented earlier are;

1) Power is transferred in both directions through the transformer.

2) The switch peak voltage is reduced to input voltage V_{IN}.

A disadvantage of this topology is the possibility of transformer

saturation and consequently failure. Current mode control which is used in many applications to remedy this disadvantage, is not effective by itself in the half bridge[48]. Options available to safeguard against saturation include a flux balancing cap, magnetically coupled energy return [48] or logic to compensate duty cycle so that current mode control does not completely discharge one bus capacitor. (i.e. C_{11} or C_{12}). These methods are not shown in the figure, yet must be considered if the half bridge is used as a HF link. All the assumptions laid out for the forward converter apply here as well.

Waveforms for the topology are shown in figure F3.20. As in the forward converter component stress analysis,reactive components are assumed to be infinite in value. Because of several inherent similarities between the half bridge and the forward converter a number of derivations are identical and therefore only final results will be shown.

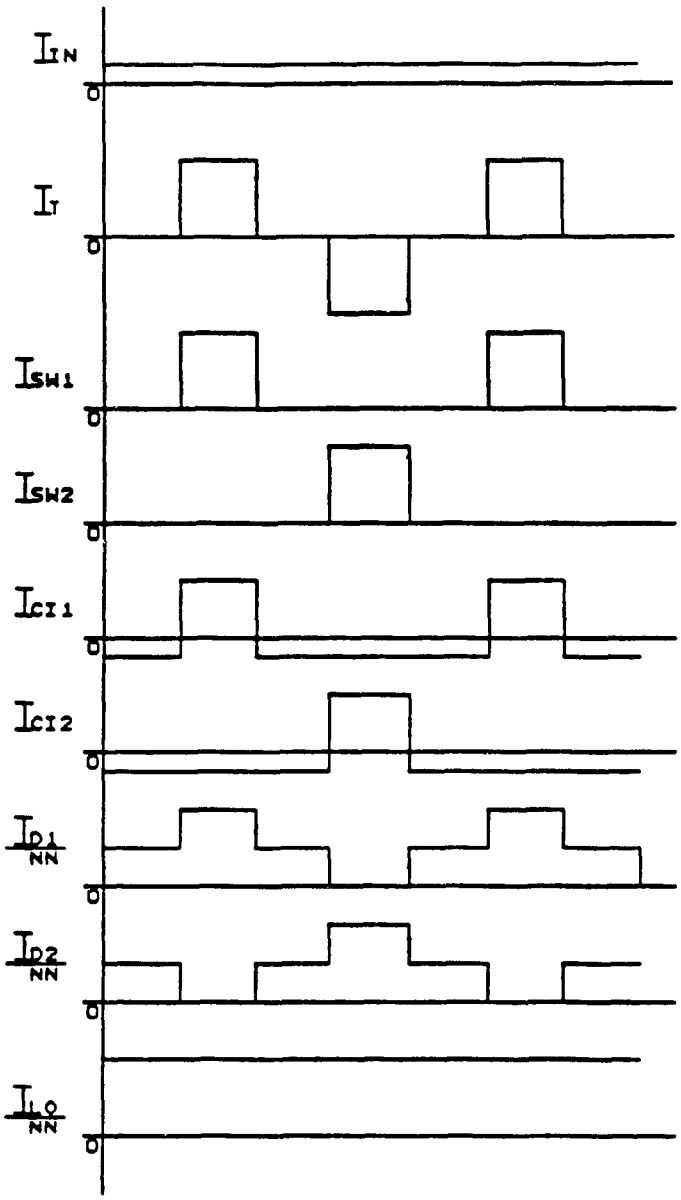


Figure F3.20 Waveforms for the half bridge inverter

Duty cycle varies according to

$$D = \frac{V_{O} \cdot NN}{V_{IN}} \qquad D \leq .5 \tag{3.187}$$

At a maximum duty cycle of 50%

$$D_{MAX} = .5$$

and low line we obtain

$$N_N = \frac{D_{MAX} \cdot V_{INMIN}}{V_{OMAX}} \tag{3.188}$$

or

$$N_N = \frac{.5 \cdot 1.053}{1.93} = .273 \tag{3.189}$$

Further

$$D_{MIN} = \frac{V_{OMIN} \cdot N_N}{V_{INMAX}} = \frac{1.53 \cdot .273}{1.35} = .309 \tag{3.190}$$

Capacitors C_{I1} and C_{I2} will have input rms currents of

$$I_{CIIRMS} = I_{CI2RMS} = \sqrt{\frac{1}{T}\int_0^T I_{CI1}^2 \, dT}$$

Using equation 3.138 we have

$$I_{CI1RMS} = I_{CI2RMS} = \frac{P_{IN}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_O \cdot N_N} - 1}$$

Since P_{IN} = 1.5 pu this yields the per unit rms current as

$$I_{CIIRMS} = I_{CI2RMS} = \frac{1.5}{V_{IN}} \sqrt{\frac{V_{IN}}{V_O \cdot .273} - 1} = 1.76 \text{ pu} \tag{3.191}$$

under worst case conditions.

For all comparative purposes, the two switching devices will face equal stresses.

$$\text{Since} \quad I_{SW1} = I_{CI1} + I_{IN} = \begin{cases} I_{IN}/D & 0 \le t \le DT \\ 0 & DT \le t \le T \end{cases} \tag{3.192}$$

the rms, average and peak current expressions of the power semiconductor devices will be identical to the forward converters. The equations (from section 3.3.1) are;

$$I_{SW1AVE} = I_{SW2AVE} = \frac{P_{IN}}{V_{IN}} = \frac{1.5}{1.053} = 1.4245 \text{ pu} \tag{3.193}$$

$$I_{SW1RMS} = I_{SW2RMS} = P_{IN}\sqrt{\frac{1}{V_{IN}\cdot V_O \cdot NN}} = 1.5\sqrt{\frac{1}{V_{IN}\cdot V_O \cdot .273}}$$

$$= 2.262 \text{ pu} \tag{3.194}$$

$$I_{SW1PK} = I_{SW2PK} = \frac{P_{IN}}{V_O \cdot NN} = \frac{1.5}{V_O \cdot .273} = 3.591 \text{ pu} \tag{3.195}$$

The peak inverse voltage across the power semiconductors is defined as the bus voltage. This can be quickly seen by the three modes of operation.

1) top switch on/lower switch off

$V_{SW1} = 0$

$V_{SW2} = V_{IN}$

2) top switch off/lower switch off

$V_{SW1} = V_{IN}/2$

$V_{SW2} = V_{IN}/2$

This is based on continuous load current that forces both output diodes to conduct which in turn impose zero volts on the primary of the transformer.

3) top switch off/lower switch on

$$V_{SW1} = V_{IN}$$

$$V_{SW2} = 0$$

Therefore,

$$V_{SWPK} = V_{IN} = 1.35 \text{ pu} \tag{3.196}$$

As the two power switching devices carry equal stress, the two output diode rectifiers also experience equal stresses. The current through diode D_1 is given by the expression

$$I_{D1} = \begin{cases} I_{SW1PK} \cdot NN & 0 \le t \le DT \\ I_{SW1PK} \cdot NN/2 & DT \le t \le T/2 \\ 0 & T/2 \le t \le T/2 + DT \\ I_{SW1PK} \cdot NN/2 & DT + T/2 \le t \le T \end{cases} \tag{3.197}$$

The average diode currents are equal and is given by

$$I_{D1AVE} = I_{D2AVE} = \int_0^D I_{SW1PK} \cdot NN \, dT + \int_0^{1-2D} \frac{I_{SW1PK} \cdot NN}{2} \, dT \tag{3.198}$$

$$= I_{SW1PK} \cdot NN \cdot \left[D + \frac{1-2D}{2} \right] = I_{SW1PK} \cdot NN/2$$

Since

$$I_{SW1PK} = \frac{P_{IN}}{V_O \cdot NN} \tag{3.199}$$

we have

$$I_{D1AVE} = I_{D2AVE} = \frac{P_{IN}}{2V_O} = \frac{1.5}{2V_O} = .49 \text{ pu} \tag{3.200}$$

The reverse voltage is solved by using the transformer turns ratio as

$$V_{D1R} = V_{D2R} = \frac{2}{NN} \cdot \frac{V_{IN}}{2} = \frac{V_{IN}}{NN} = \frac{V_{IN}}{.273} = 4.94 \text{ pu} \quad (3.201)$$

The output filter components carry equivalent rms currents as in the forward converter due to the infinite values assumption. Worst case output inductor current is given at lowest output voltage by

$$I_{LORMS} = \frac{P_{IN}}{Vo} = \frac{1.5}{Vo} = .98 \text{ pu} \quad (3.202)$$

Further, as in the forward converter

$$I_{CORMS} = 0 \text{ pu} \quad (3.203)$$

Equation 3.155 (chapter 3.3.1) given for relative transformer power transfer ratio is a general empirical equation applicable in the half bridge topology as well. Therefore, we have

$$A_P^* = \left[\frac{10^4}{K_T \cdot K_U \cdot K_P \cdot 420 \cdot K_B \cdot 2} \right]^{1.31}$$

However for the half bridge inverter

$K_T = 1$

$K_U = .4$

$K_P = .41$

$K_B = .5$

yielding

$$A_P^* = \left[\frac{10^4}{2 \cdot K_T \cdot K_W \cdot K_P \cdot 420 \cdot K_B} \right]^{1.31} = 679.4 \quad (3.204)$$

As in the forward converter analysis of reactive component values provide further insight into the effectiveness of the power conversion topology.

Derivation of the output filter components for the half bridge is virtually identical to the derivation for the forward converter with only minor alterations. From equation 3.160

$$L_O = \frac{V_O \cdot T_{OFF}}{.25 \cdot I_O}$$

where

$$T_{OFF} = \left[\frac{1-2D}{2} \right] \cdot T = \left[\frac{1 - 2V_O \cdot NN/V_{IN}}{2F_{SW}} \right] \qquad (3.205)$$

The duty cycle multiplication factor of "2" and the overall division factor of "2" is a result of double the inductor charging frequency when compared to a forward converter with equal switching frequency. This is shown in figure F3.21.

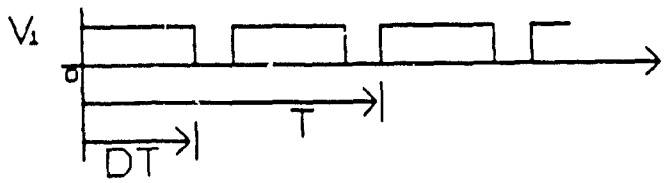


Figure F3.21 Half bridge inverter output inductor charging

The per unit equivalent in the frequency domain is given by

$$X_{LO} = \frac{V_O \cdot T_{OFF}}{.25 \cdot I_O} \cdot 2\pi \cdot F_{SW} \quad pu \qquad (3.206)$$

$$= 4\pi \cdot \frac{V_O}{I_O} \left[1 - \frac{2 \cdot V_O \cdot NN}{V_{IN}} \right] = 4\pi \cdot \frac{V_O^2}{P_{OUT}} \left[1 - \frac{2 \cdot V_O \cdot NN}{V_{IN}} \right] \quad pu \qquad (3.207)$$

At worst case, when

$$V_O = 1.65 \text{ pu}$$

$$V_{IN} = 1.35 \text{ pu}$$

equation 3.207 yields

$$X_{LO} = 7.59 \text{ pu}$$

The value of output capacitance is given by a modified form of equation 3.168 as

$$C_O = \frac{I_O}{V_O \cdot 1.6 \cdot F_{SW}} \cdot \frac{1}{2} \qquad (3.208)$$

Again the division factor of "2" is a result of double filter energy charging per switching period. When altered to the frequency independent per unit format

$$X_{CO} = \frac{V_O^2 \cdot 1.6}{\pi \cdot P_{OUT}} \text{ pu} \qquad (3.209)$$

The worst case arises when "Vo " is at its minimum value yielding

$$X_{CO} = \frac{(1.53)^2 \cdot 1.6}{\pi \cdot (1.5)} = .794 \text{ pu}$$

The input filter values are calculated based on similar assumptions used for the forward converter input filter design. The worst case input capacitor voltage ripple occurs when duty cycle D = .5 resulting in a relatively square wave current extraction from capacitors C_{I1} and C_{I2}. This results in the same expression as used for the forward converter (equation 3.179).

$$C_{I1} = C_{I2} = \frac{3.334 \cdot P_{IN}}{F_{SW} \cdot V_{IN}^2}$$

This yields a worst case impedance equivalent to the forward converter of

$$X_{CI} = .0353 \text{ pu}$$

At 50% duty cycle however, the input inductor sees zero current ripple because

$$\Delta V_{CI1} + \Delta V_{CI2} = 0 \qquad (3.210)$$

This is due to the exact 180° phase shift of gating signals drawing constant current from the filter choke. The inductor actually delivers current ripple to two capacitors 180° out of phase resulting in ripple current at two times the switching frequency. Since the worst case ripple for the inductor still occurs at 50% up and 50% down excursion time the duty cycle to provide that ripple would be 25%. Figure F3.22 shows the waveform representation.

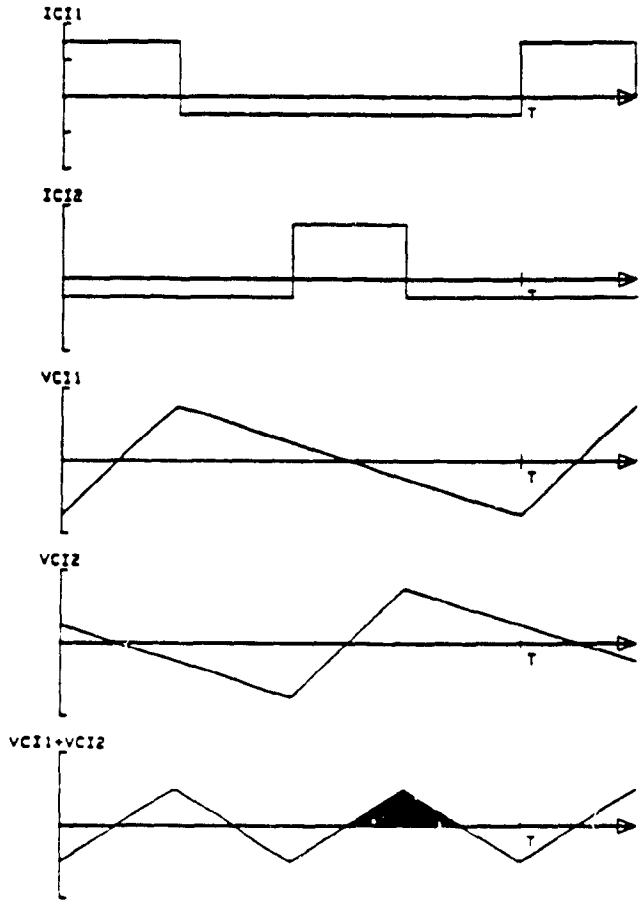


Figure F3.22 Half bridge inverter input waveforms

From the figure,

$$\frac{\Delta(V_{CI1} + V_{CI2})}{\Delta V_{CI1}} = \frac{2}{3} \qquad (3.211)$$

The shaded section of (V_{CI1} + V_{CI2}) represents the area of V_L contributing to the rising current ripple of L_1. The average is given by

$$\frac{\Delta V_{LI}}{4} = \frac{\Delta V_{CI}}{4} \cdot \frac{2}{3} = \frac{\Delta V_{CI1}}{6} \qquad (3.212)$$

The area is given by

$$\frac{\Delta V_{C11}}{6} \cdot \frac{T}{4} \tag{3.213}$$

Combining yields

$$\Delta I_{LI} = \frac{1}{L_I} \cdot \frac{\Delta V_{C11} \cdot T}{24} \tag{3.214}$$

As in the forward converter, input ripple current is limited to 5% resulting in

$$\Delta I_{LI} = .05 \cdot I_{IN} = .05 \cdot P_{IN}/V_{IN}. \tag{3.215}$$

Moreover,

$$\Delta V_{C11} = .15 \cdot V_{IN} \tag{3.216}$$

and

$$T = 1/F_{SW} \tag{3.217}$$

Inserting and rearranging equation 3.214 we obtain

$$L_I = \frac{.125 \cdot V_{IN}^2}{P_{IN} \cdot F_{SW}} \tag{3.218}$$

Solving for the equivalent frequency independent per unit expression results in

$$X_{LI} = \frac{2\pi \cdot (.125) \cdot V_{IN}^2}{P_{IN}} \text{ pu} \tag{3.219}$$

At worst case, when maximum input voltage exists equation 3.219 yields

$$X_{LI} = \frac{2\pi \cdot (.125) \cdot (1.35)^2}{1.5} = .955 \text{ pu}$$

3.3 Full Bridge Evaluation

The simplified full bridge converter is shown in figure F3.23.

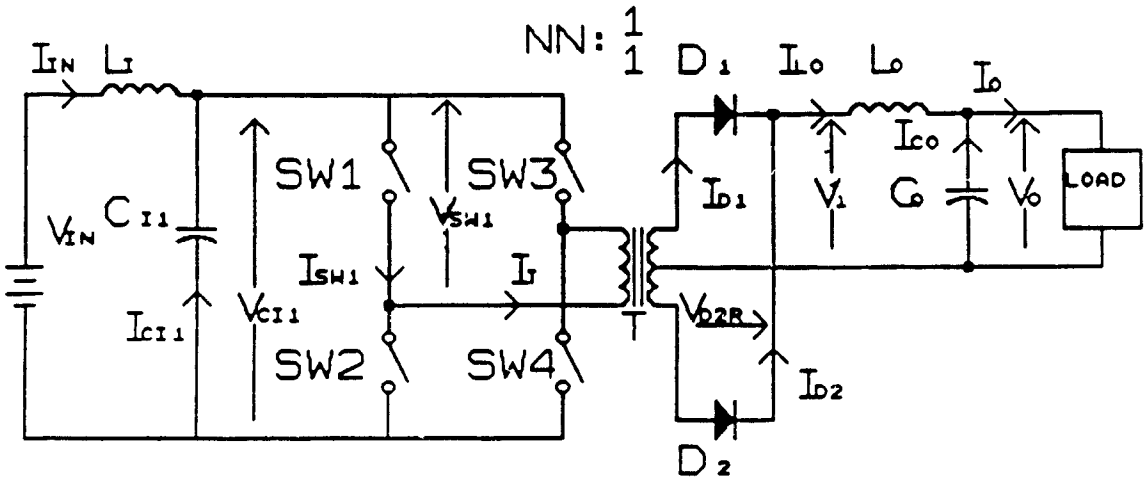


Figure F3.23 Full bridge inverter power train topology

The main differences of the full bridge with respect to the half bridge are:

1) The transformer primary voltage is no longer $V_{IN}/2$ indicating that for equal power transfer, the switches of the full bridge carry half the current.

2) There is no need to provide special circuitry to equalize the voltage across the input capacitors as was needed in the half bridge.

3) The problem of transformer saturation can be alleviated by current mode control without bulk capacitor discharge as was noticed in half bridge.

Waveforms for this topology are shown in figure F3.24.

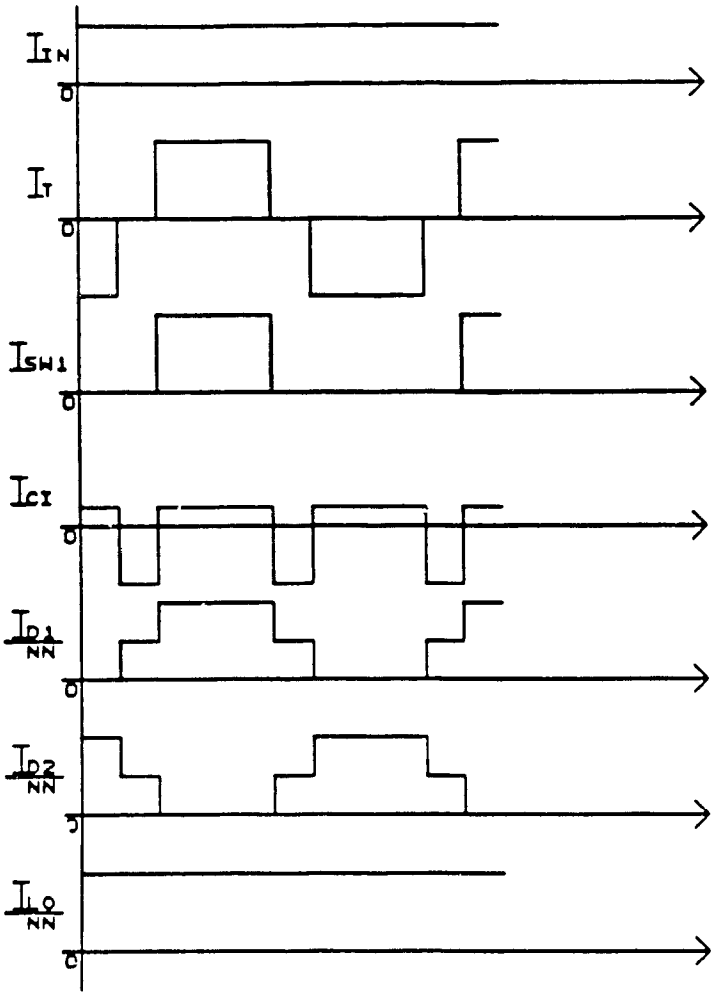


Figure F3.24 Full bridge inverter topology waveforms

It should be noted that all component ratings that requiring identical derivations as in the half bridge or the forward converter will not be duplicated, yet will be shown in final form. Moreover, the assumptions previously outlined for the forward and half bridge prevail here. Letting

$$D = \frac{Vo \cdot NN}{2 \cdot VIN} \qquad \text{Where } D \leq .5 \tag{3.220}$$

we have

$$NN = \frac{2 \cdot DMAX \cdot VINMIN}{VOMAX} = \frac{2 \cdot (.5) \cdot (1.053)}{1.93} = .546$$

Further

$$DMIN = \frac{VOMIN \cdot NN}{2 \cdot VINMAX} = \frac{1.53 \cdot (.546)}{2 \cdot (1.35)} = .309$$

Capacitor CI will have an rms current rating derived in a similar fashion as the forward converter. Equation 3.138 is rewritten with emphasis on the duty cycle of current in the capacitor.

$$ICIRMS = IIN \cdot \sqrt{\frac{1}{DCAP} - 1} \quad pu \tag{3.221}$$

where $DCAP = 2D = = \frac{VO \cdot NN}{VIN}$

After substitution we have

$$ICIRMS = \frac{1.5}{VIN} \sqrt{\frac{VIN}{VO \cdot NN} - 1} = \frac{1.5}{VIN} \sqrt{\frac{VIN}{VO \cdot (.54)} - 1} \quad pu \tag{3.222}$$

At worst case, when VIN=1.35 pu and Vo=1.53 equation 3.222 yields

$$ICIRMS = .87 \text{ pu}$$

The important switch parameters are evaluated from;

$$ISW1 = ICI + IIN = \begin{cases} IIN/2D & 0 \le t \le DT \\ 0 & DT \le t \le T \end{cases} \tag{3.223}$$

The average switch current is equal for each switch and is given by

$$I_{SWAVE} = \frac{1}{T}\int_{0}^{DT} \frac{I_{IN}}{2\cdot D}\, dT = \frac{I_{IN}}{2} = \frac{P_{IN}}{2\cdot V_{IN}} \qquad (3.224)$$

At lowest input voltage this results in

$$I_{SW1AVE} = I_{SW2AVE} = I_{SW3AVE} = I_{SW4AVE} = \frac{1.5}{2\cdot(1.053)} = .712 \text{ pu}$$

The rms switch current is given by

$$I_{SW1RMS} = \sqrt{\frac{1}{T}\int_{0}^{DT} \left[\frac{I_{IN}}{2D}\right]^2 dT} = I_{IN}\sqrt{\frac{1}{4\cdot D}} \qquad (3.225)$$

Since

$$D = \frac{V_O\cdot NN}{2\cdot V_{IN}}$$

$$I_{SW1RMS} = I_{IN}\cdot\sqrt{\frac{V_{IN}}{2\cdot V_O\cdot NN}} = P_{IN}\cdot\sqrt{\frac{1}{2\cdot V_O\cdot V_{IN}\cdot NN}} \qquad (3.226)$$

At worst case (ie minimum V_O and V_{In})

$$I_{SW1RMS} = I_{SW2RMS} = I_{SW3RMS} = I_{SW4RMS} = 1.5\cdot\sqrt{\frac{1}{2\cdot(1.053)\cdot(1.53)\cdot(.546)}}$$

$$= 1.131 \text{ pu}$$

The full bridge peak switch current is given by

$$I_{SW1PK} = (I_{IN} + I_{CI})_{t=DT} = \frac{I_{IN}}{2 \cdot D} = \frac{I_{IN} \cdot V_{IN}}{V_O \cdot NN} = \frac{P_{IN}}{V_O \cdot NN} \qquad (3.227)$$

at worst case or minimum output voltage equation 3.227 results in

$$I_{SW1PK} = I_{SW2PK} = I_{SW3FK} = I_{SW4PK} = \frac{1.5}{1.53 \cdot (.546)} = 1.796 \text{ pu}$$

To solve the maximum reverse voltage across each power switching device, equations derived for the half bridge hold here as well.

$$V_{SW1PK} = V_{SW2PK} = V_{SW3PK} = V_{SW4PK} = V_{IN} = 1.35 \text{ pu}$$

The output stage of the full bridge has nearly identical stresses as the half bridge. The output diodes carry a worst case average current at lowest output voltage of

$$I_{D1AVE} = I_{D2AVE} = \frac{P_{IN}}{2 \cdot V_O} = \frac{1.5}{2 \cdot (1.53)} = .490 \text{ pu}$$

Further,

$$V_{D1R} = V_{D2R} = \frac{2 \cdot V_{IN}}{NN} = \frac{2 \cdot (1.35)}{.546} = 4.945 \text{ pu}$$

at worst case. Moreover, as derived in the forward and half bridge application;

$$I_{LORMS} = \frac{P_{IN}}{V_O} = \frac{1.5}{1.53} = .98 \text{ pu}$$

and

$$I_{CORMS} = 0 \text{ pu}$$

The derivation for relative transformer size (equation 3.155 of chapter 3.3.1) is applicable for the full bridge topology as well. Further, due to the similar nature of the forward and half bridge configurations the transformer will be roughly the same size.

$$A_P^{\bullet} = \left[\frac{10^4}{2 \cdot K_T \cdot K_U \cdot K_P \cdot 420 \cdot K_B} \right]^{1.31} \qquad (3.228)$$

In the full bridge application

$K_T = 1.0$

$K_U = .4$

$K_P = .41$

$K_B = .5$

Evaluation 3.228 yields

$$A_P^{\bullet} = 679.4 \text{ pu}$$

Eliminating the assumption of infinite inductance and capacitance, the required impedance values of the filter components can be solved.

From the forward topology evaluation

$$L_O = \frac{V_O \cdot T_{OFF}}{.25 \cdot I_{OUT}} \text{ pu} \qquad (3.229)$$

where

$$T_{OFF} = \left[\frac{1-2D}{2} \right] \cdot T \tag{3.230}$$

Since

$$D = \frac{V_O \cdot NN}{2 \cdot V_{IN}}$$

equation 3.230 becomes after rearranging

$$T_{OFF} = \left[\frac{1 - V_O \cdot NN/V_{IN}}{2 \cdot F_{SW}} \right] \tag{3.231}$$

After substitution of equation 3.231 into equation 2.229 and solving for impedance

$$X_{LO} = \frac{V_O \cdot T_{OFF} \cdot 2\pi \cdot F_{SW}}{.25 \cdot I_{OUT}} \text{ pu} \tag{3.232}$$

$$= \frac{4\pi V_O}{I_{OUT}} \left[1 - \frac{V_O \cdot NN}{V_{IN}} \right] = \frac{4\pi \cdot V_O^2}{P_{OUT}} \left[1 - \frac{V_O \cdot NN}{V_{IN}} \right] \text{ pu} \tag{3.233}$$

When V_O = 1.65 pu and V_{IN} = 1.35 pu equation 3.232 yields its worst case impedance

$$X_{LO} = 7.59 \text{ pu}$$

Also from chapter 3.? ? equation 3.208,

$$C_O = \frac{.5 \cdot I_{OUT}}{V_O \cdot 1.6 \cdot F_{SW}} = \frac{.5 \cdot P_{OUT}}{V_O^2 \cdot 1.6 \cdot F_{SW}} \text{ pu} \tag{3.234}$$

This can be represented in impedance form as

$$Xco = \frac{Vo^2 \cdot 1.6}{\pi \cdot POUT} \text{ pu} \tag{3.235}$$

When Vo is at its minimum (ie Vo = 1.53 pu), Xco is at its worst case of

$$Xco = .795 \text{ pu.}$$

The input filter capacitive positive level current is

$$ICPOS = \left[\frac{1-2D}{2D} \right] \cdot IIN \tag{3.236}$$

The worst case voltage ripple will occur when the capacitor current has a square wave form which parallels the worst case scenario of the forward and half bridge input capacitors. However, for the full bridge this occurs when duty cycle D = .25 since the capacitor sees twice the current sink frequency as each power semiconductor. Using

$$ICI = CI \frac{d}{dt} VCI \tag{3.237}$$

combined with the assumption that the capacitor delivers all the ripple current yields

$$\left[\frac{1-2D}{2D} \right] \cdot IIN = CI \cdot \frac{\Delta VCI}{\Delta t} \tag{3.238}$$

Letting

$$D = .25$$

and

$$\Delta t = TOFF = \left[\frac{1 - 2D}{2} \right] \cdot T \tag{3.239}$$

and

$$\Delta V_{CI} = .15 \cdot V_{IN} \tag{3.240}$$

equation 3.238 becomes after isolating for C_I

$$C_I = 1.6667 \cdot \frac{I_{IN} \cdot T}{V_{IN}} \text{ pu} \tag{3.241}$$

Since

$$P_{IN} = I_{IN} \cdot V_{IN} \tag{3.242}$$

and

$$T = 1/F_{SW} \tag{3.243}$$

equation 3.241 becomes

$$C_I = 1.667 \cdot \frac{P_{IN}}{F_{SW} \cdot V_{IN}^2} \text{ pu} \tag{3.244}$$

After conversion to the frequency independent per unit basis we obtain

$$X_{CI} = \frac{V_{IN}^2}{1.667 \cdot P_{in} \cdot 2\pi} \text{ pu} \tag{3.245}$$

Equation 3.245 has a worst case value when V_{IN} is at its minimum value (ie V_{IN} = 1.053 pu) yielding

$$X_{CI} = .071 \text{ pu}$$

The input filter inductor will see the worst case ripple at D = .25 just as the capacitance. In fact, the required value of inductance can be derived from equation 3.185 yet with double the switching frequency due to the nature of the full bridge.

Therefore,

$$L_I = \frac{.1875 \cdot V_{IN}^2}{P_{IN} \cdot F_{SW}} \text{ pu} \qquad (3.246)$$

or as an impedance

$$X_{LI} = \frac{.1875 \cdot V_{IN}^2 \cdot 2\pi}{P_{IN}} \text{ pu} \qquad (3.247)$$

Equation 3.247 has a worst case value when V_{IN} = 1.35 pu of

$$X_{LI} = 1.431 \text{ pu}$$

3.3.4 High Frequency Link Selection

A tabulated list of the required per unit ratings for each of the HF link options is shown in Table T3.8.

ITEM	SINGLE SWITCH	HALF BRIDGE	FULL BRIDGE
I_{CIRMS}	1.200	1.760	0.870
I_{SWAVE}	1.425	1.425	0.712
I_{SWRMS}	1.850	2.262	1.131
I_{SWPK}	2.397	3.591	1.796
Vswpk	4.210	1.350	1.350
I_{D1AVE}	0.583	0.490	0.490
V_{D1R}	7.720	4.945	4.945
I_{D2AVE}	0.530	0.490	0.490
V_{D2R}	3.300	4.945	4.945
I_{LORMS}	0.980	0.980	0.980
I_{C0RMS}	0.000	0.000	0.000
A_P	1196.	679.4	679.4
X_{LO}	25.92	7.590	7.590
X_{CO}	0.397	0.794	0.794
X_{CI}	0.035	0.035	0.071
X_{LI}	2.860	0.955	1.431

Table T3.8 Summary of high frequency link ratings

Observation of the data in Table T3.8 reveals that;

1- The single switch converter is simple and rugged. It requires only one main switch base drive. However, the configuration is associated with several significant drawbacks including:

A) All magnetic components are equal to or larger than the remaining two topologies. In particular the power transformer will be roughly twice the volume of the half bridge or full bridge equivalent circuit. Moreover inductors are also at least double the size. This drawback contradicts the design objective of reduced weight and size.

B) The semiconductor reverse voltages are extremely high. For typical line applications of 115 V_{L-N}, the reverse voltage on the switching device will be 688 volts immediately hampering the application of popular MOSFET switches. Further a secondary diode will face reverse voltages of 1265 volts eliminating the use of ultra fast secondary diodes unless series diodes are used. If fast recovery diodes are used, duty cycle time will be eroded because of the longer recovery time which may require larger current handling capability of the power switching devices.

2- The attractive feature of the half bridge is its dramatic reduction in semiconductor voltage requirements over the single switch converter, enabling easy use of MOSFET's and ultra fast diodes. Moreover, transformer volume and reactive component size are significantly reduced over the single switch equivalent. However, the power switching device will face increased RMS and peak currents. In a 10KW power transfer, the peak current which directly effects the thermal stress commutated by the switch, is in the range of 150 amps. Once again virtually elimination MOSFET application unless a significant number of parallel semiconductors are used. Even with bipolar semiconductors,

large drive currents are required for proper operation which is not a trivial matter.

3- The full bridge significantly reduces the component stresses across the board when compared with the single switch converter, and many parameters when compared with the half bridge converter. This topology however requires four independent isolated drives which will extend the cost and complexity.

Based on Table T3.8 and the observations expressed, the most suitable high frequency link topology for the medium power UPS system proposed would be the full bridge topology. This configuration offers minimal total volume and weight while maintaining minimal component stresses at the expense of added complexity.

3.4 Design Example

All of the per unit ratings can be upgraded to exact component values for any power level with the exception of the transformer relative size parameter (A_P^*). Since the ferrite core transformer size is a nonlinear function, it must be derived at point of use.

The design example outlined here adheres closely to the summary of specifications listed in chapter 2.2.1 with the note that unbalanced and nonlinear loads are not yet addressed. The base parameters are

V_{IN} = 115V_{RMS} L-N ±10% 60Hz

P_{IN} = 10kVA

V_{OUT} = 115V_{RMS} L-N

Fsw(Inverter) = 60Hz

Fsw(HF link) = 20KHz

Fsw(Rectifier) = 60Hz

These parameters translate into the following scaling factors

$$V_{ACTUAL} = V_{pu} \cdot V_{IN(PEAK)} = 115\sqrt{2} \cdot V_{pu} = 162.6 \cdot V_{pu} \qquad 3.248$$

$$Z_{ACTUAL} = \left[\frac{3 \cdot V_{IN(PEAK)}^2}{2 \cdot P_{IN}}\right] \cdot Z_{pu} = \left[\frac{3 \cdot (115\sqrt{2})^2}{2 \cdot 10000}\right] \cdot Z_{pu} = 3.967 \cdot Z_{pu} \qquad (3.249)$$

$$I_{ACTUAL} = \left[\frac{2 \cdot P_{IN}}{3 \cdot V_{IN(PEAK)}}\right] \cdot I_{pu} = \left[\frac{2 \cdot 10000}{3 \cdot 115\sqrt{2}}\right] \cdot I_{pu} = 40.99 \cdot I_{pu} \qquad (3.250)$$

$$P_{ACTUAL} = \frac{P_{IN}}{1.5} \cdot P_{pu} = \frac{10000}{1.5} \cdot P_{pu} = 6667 \cdot P_{pu} \qquad (3.251)$$

3.4.1 Circuit Values

Figure F3.25 shows the complete power UPS power train configuration.

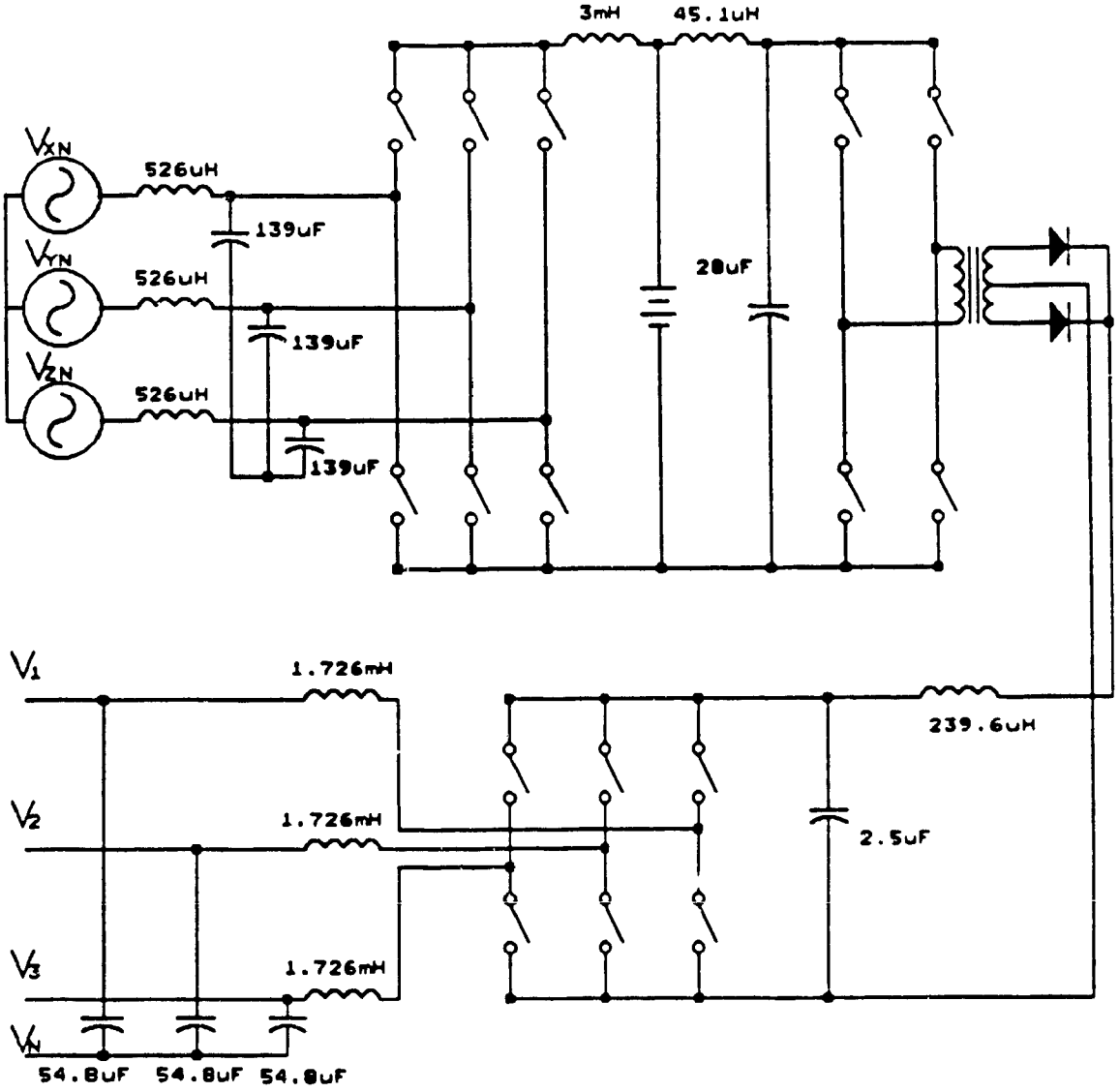


Figure F3.25 UPS power train with components

3.4.1.1 Inverter Stage

Z_{co}	=	48.37Ω
C_o	=	54.8μF
I_{co}	=	3.566A_{RMS}
V_{co}	=	115V_{RMS}
Co_{VA}	=	410VA

Z_{LO}	=	.65Ω
L_O	=	1.726mH
I_{LO}	=	30.74A_{RMS}
V_{LO}	=	70.58V_{RMS}
L_{OVA}	=	2.173kVA
I_{SWAVE}	=	12.34A
V_{SWPK}	=	313.9V
Z_{LI}	=	.155Ω
L_I	=	410μH
I_{LI}	=	35.7A_{RMS}
V_{LI}	=	7.48V_{RMS}
L_{IVA}	=	267 1VA
Z_{CI}	=	24.28Ω
C_I	=	108 8μF
I_{CI}	=	10 86A_{RMS}
V_{CI}	=	313 9V
C_{IVA}	=	3 409kVA
$V_{DCBUSMAX}$	=	313 9V
$V_{DCBUSMIN}$	=	248 8V

3.4.1.2 Rectifier Stage

Z_{LO}	=	1.166Ω
L_O	=	3 09mH
I_{LO}	=	58 4A
V_{LO}	=	105 7V_{RMS}
L_{OVA}	=	161 2VA
I_{SWAVE}	=	19 47A

I_{SWRMS} = 33.73A_{RMS}

V_{SWPK} = 309.9V

Z_{LI} = .198Ω

L_I = 526μH

I_{LI} = 32.3A_{RMS}

Z_{CI} = 19.04Ω

C_I = 139μF

I_{CI} = 13.94A_{RMS}

V_{BATMIN} = 171.3V

V_{BATMAX} = 219.6V

3.4.1.3 High Frequency Link Stage

Z_{CI} = .281Ω

C_I = 28μF

I_{CI} = 35.66A_{RMS}

V_{CI} = 219.6V

Z_{LI} = 5.677Ω

L_I = 45.1μH

I_{LI} = 58.56A

I_{SWAVE} = 29.18A

I_{SWRMS} = 46.36A_{RMS}

I_{SWPK} = 73.62A

V_{SWPK} = 219.6V

I_{DAVE} = 20.09A

V_{DPK} = 804.2V

Z_{LO} = 30.11Ω

L_O = 239.6μH

I_{LO} = 40.17A_{RMS}

Z_{CO} = 3.154Ω

C_O = 2.5μF

Transformer area product

$$A_P = A_P^{\bullet}\left[\frac{P_{IN}}{\Delta B \cdot F_{SW}}\right]^{1.31}$$

P_{IN} = 10KW

ΔB = 3000 Gauss or .3 Teslas

F_{SW} = 20KHz

Therefore A_P = 1327cm^4

3.4.2 Simulation Results

To strengthen confidence in the analytical derivations, various sections of the power train were simulated using rated values

3.4.2.1 Inverter Simulation

The worst case ratings program derived from the analytical expressions of chapter 3 1 and outlined in chapter 2 5 1 was used to generate component waveforms resulting from the inverter data derived in chapter 3.4.1 1 Selected waveforms are shown in figure F3.26 for operating conditions of

V_{DCBUS} = 314 V

Load PF = .7 lagging

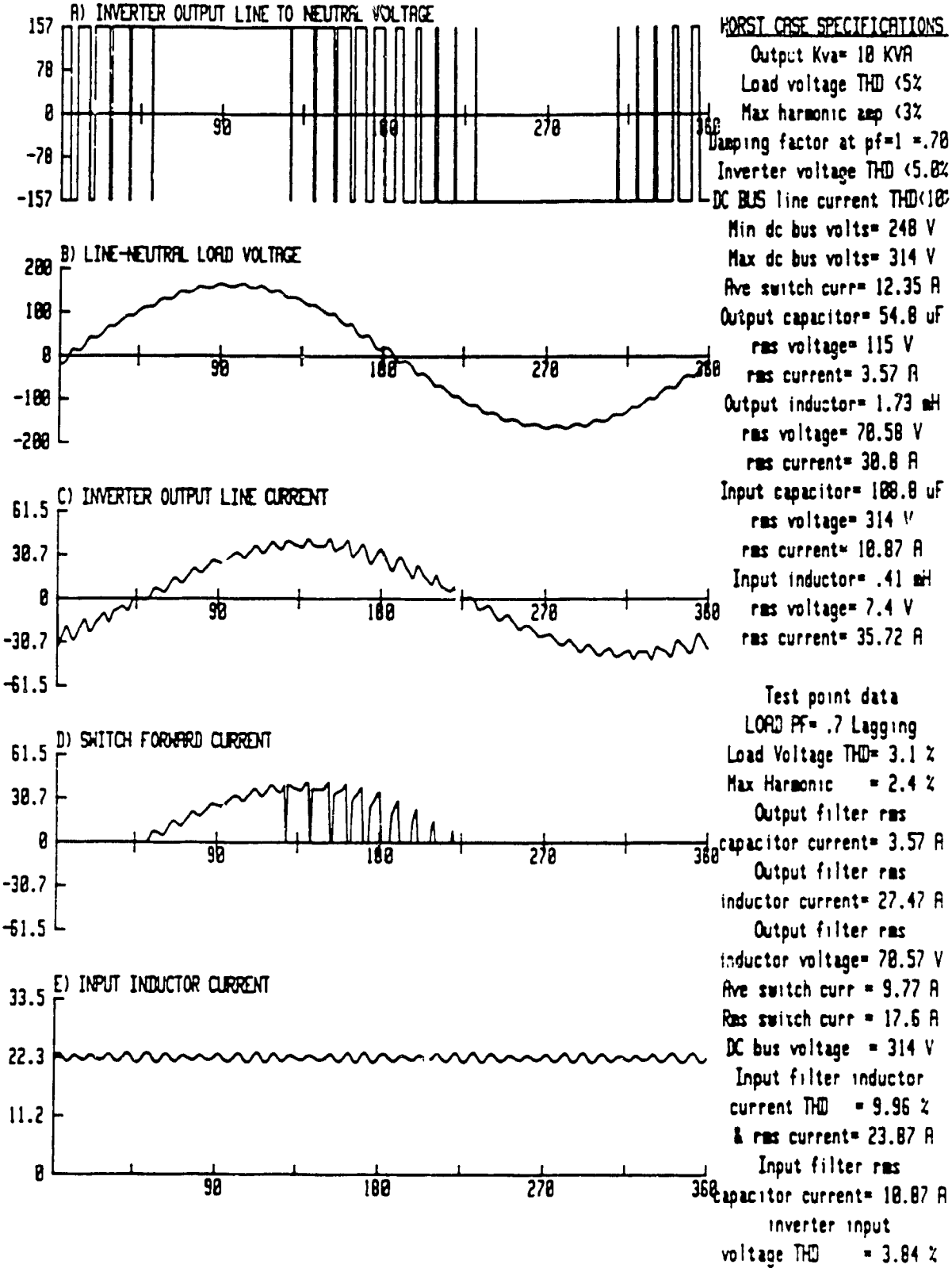


Figure F3.26 Worst case inverter ratings program waveform results with lagging PF

Since these waveforms are derived almost entirely in the frequency domain using fourier series, true simulation was done using the software program outlined in chapter 2.5.2. The circuit simulated is shown in figure F3.27.

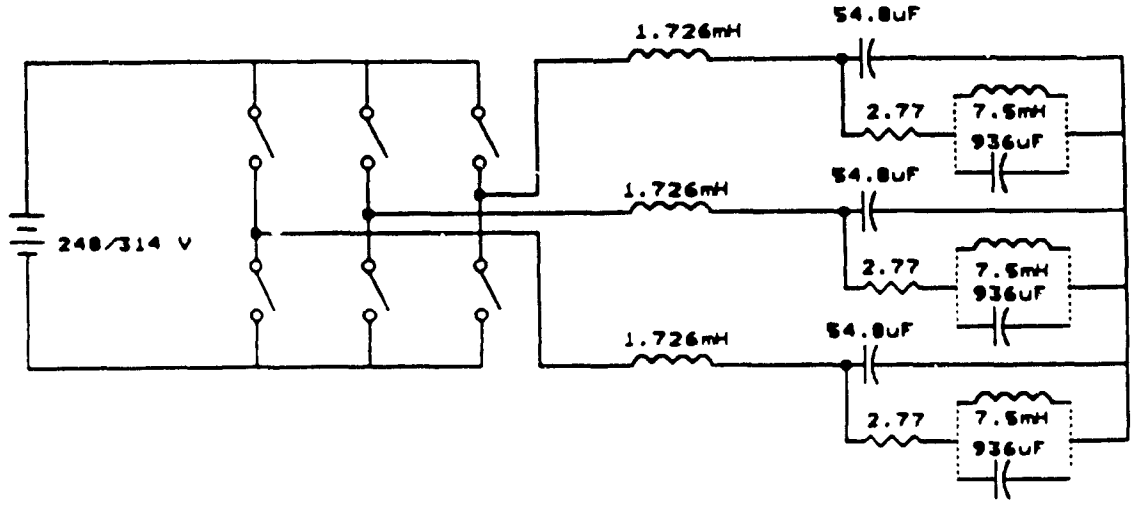


Figure F3.27 Simulated inverter circuit topology

The resulting simulated steady state waveforms are shown in figure F3.28. The waveforms show complete agreement with results derived from the worst case ratings program results Further, all waveforms are within derived worst case ratings.

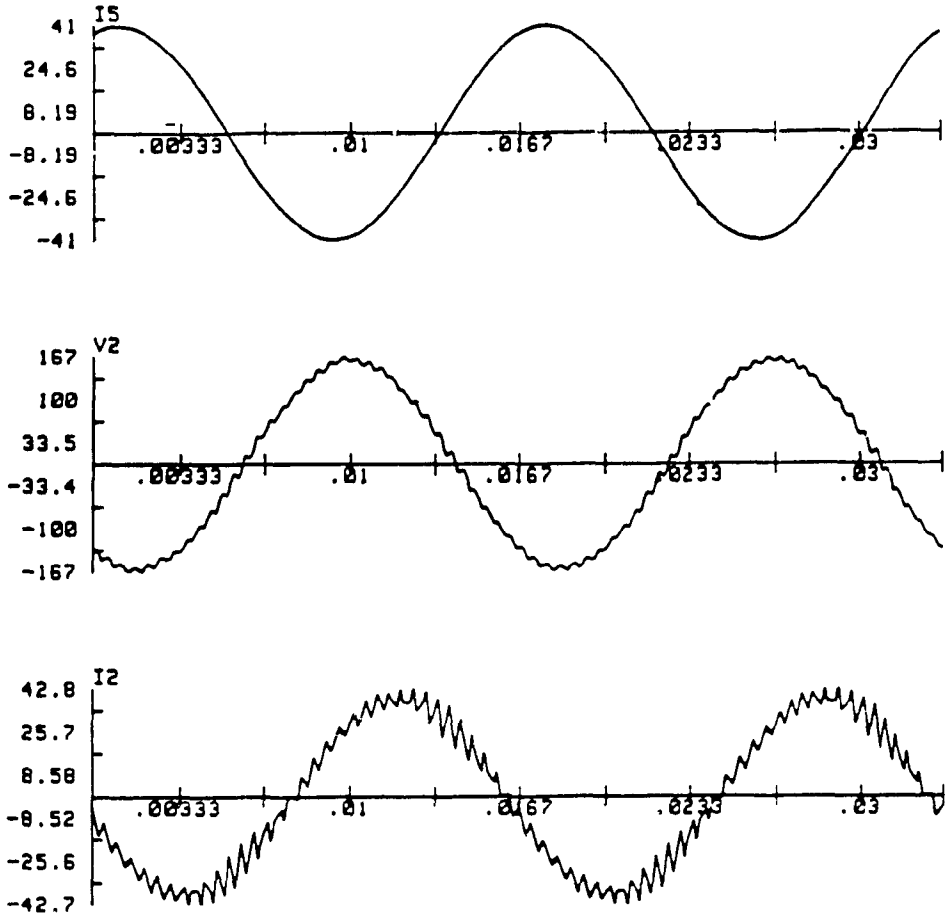


Figure F3.28 Inverter lagging PF simulation results

I5-> Load current
V2-> Inverter load L-N voltage
I2-> Inverter output line current

A second pass of the worst case analysis test point data for

V_{DCBUS} = 248.8

Load PF = .7 leading

results in the waveforms shown in figure F3.29.

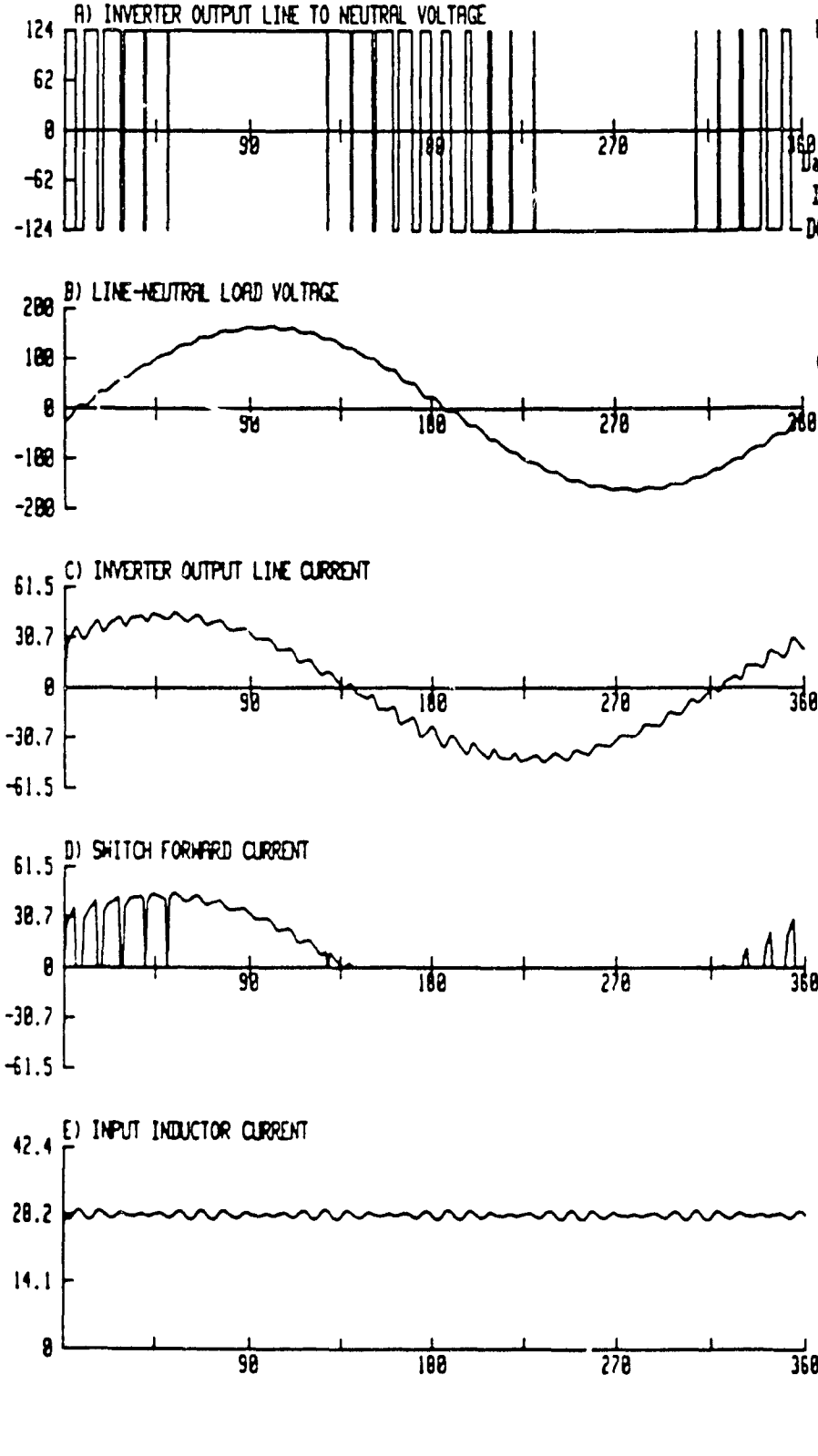


Figure F3.29 Worst case inverter ratings program waveform results with leading PF

This worst case capacitive load effect was also simulated with the results shown in figure F3.30

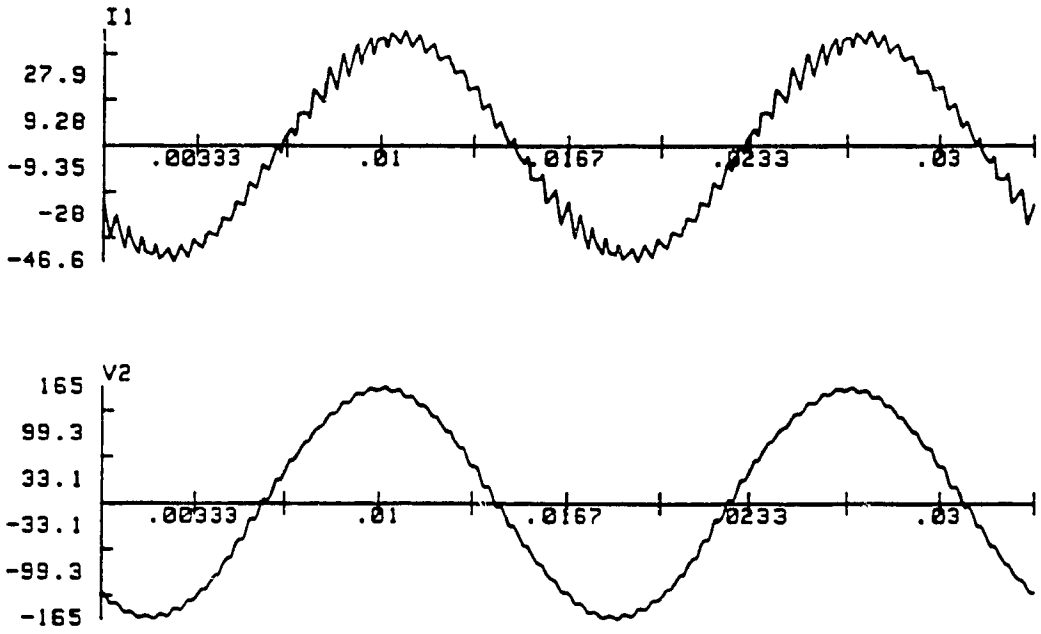


Figure F3.30 Inverter leading PF simulation results

I1-> Inverter Output line Current
V2-> Inverter load L-N voltage

Comparison of respective waveforms and test data reveal complete agreement. Further, component stresses are within respective worst case expectations.

A final run of the worst case ratings program yields the waveforms of figure F3.31 under unity power factor loading. These results are used for experimental verification in forthcoming sections.

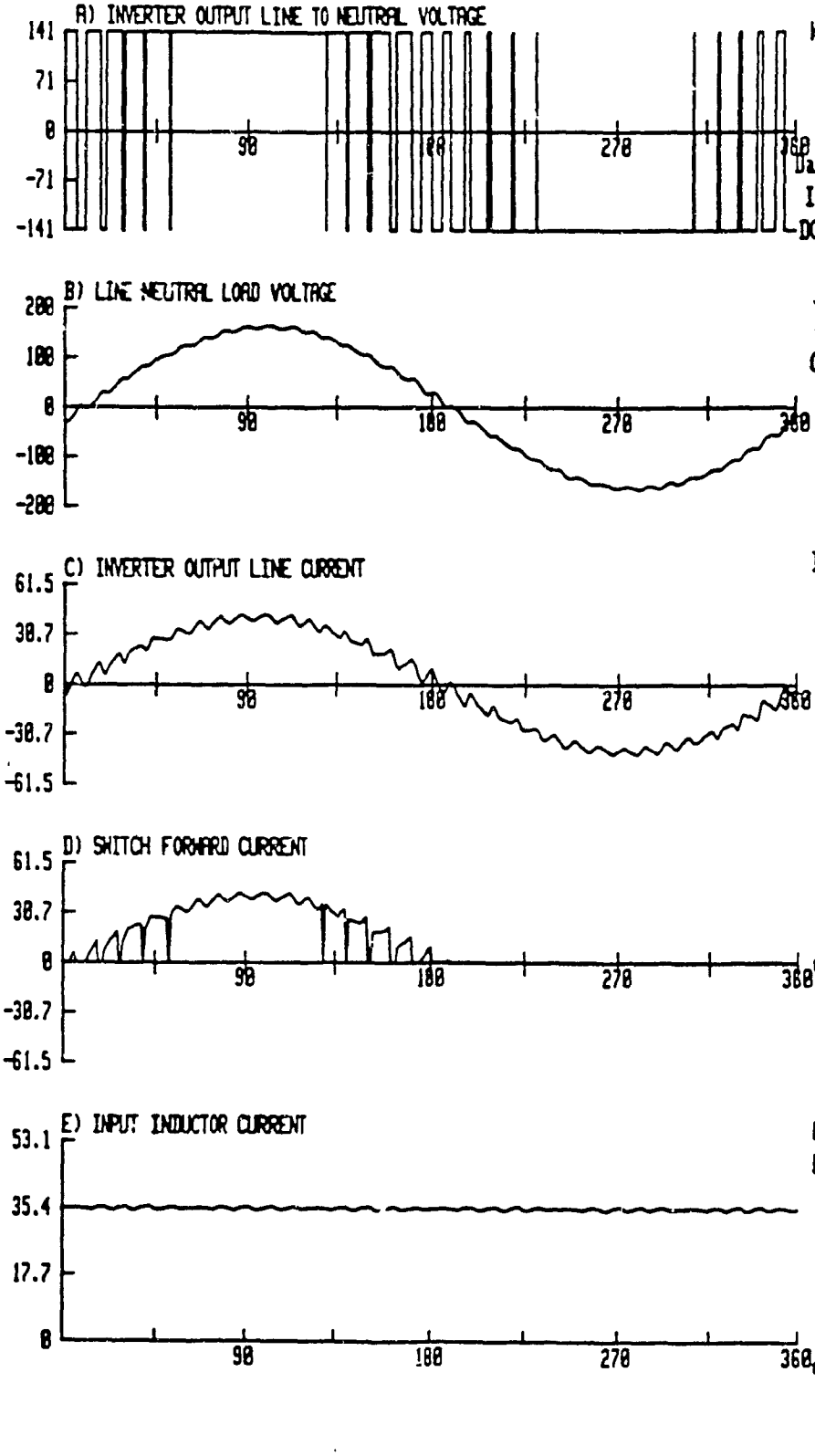


Figure F3.31 Worst case inverter ratings program results with unity power factor

3.4.2.2 Rectifier Simulation

The simulation analysis software developed was further used to simulate the rectifier shown in figure F3.32

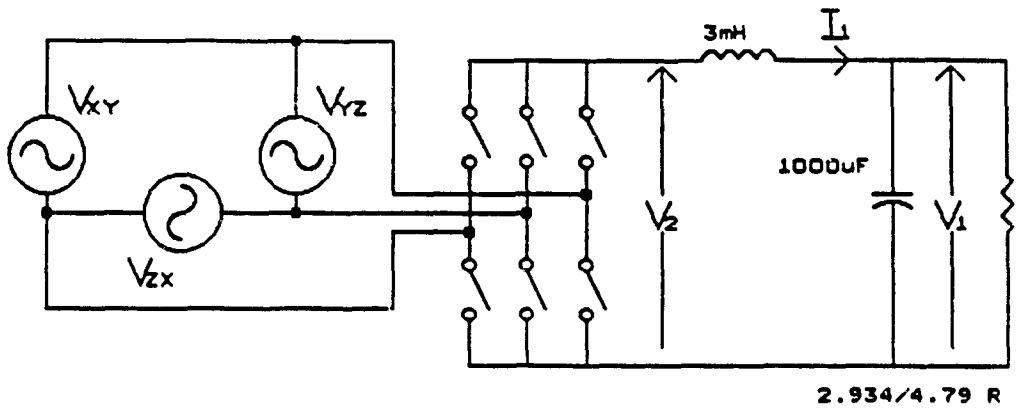


Figure F3.32 Rectifier simulation topology

The rectifier assumes a battery capacitance of at least 1000uF exists and the conditions are worst case in terms of ripple content ie

V_{XN} = high line = 126.5 $V_{RMS\ L\text{-}N}$

M = .638

Load = 10KW

The simulation results are shown in figure F3.33 and represent start up conditions.

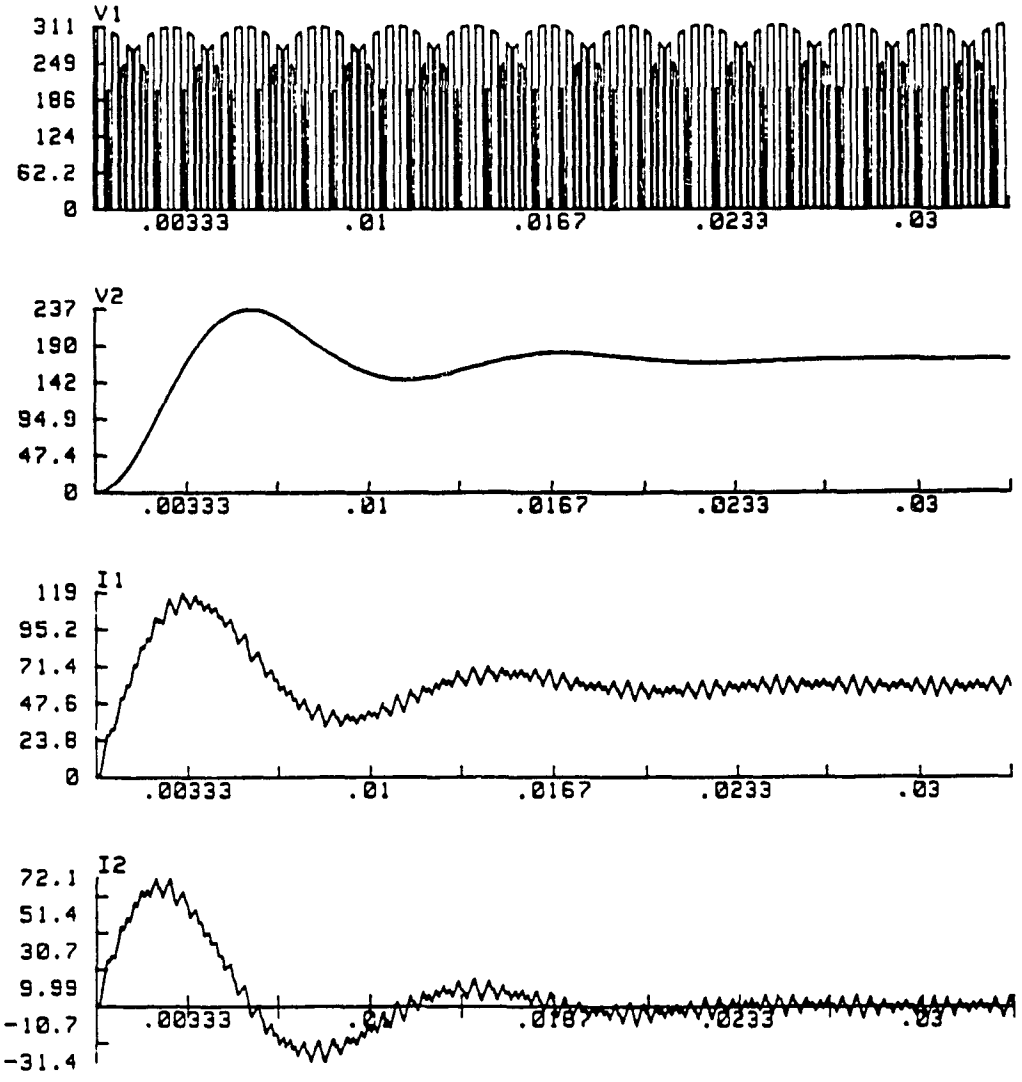


Figure F3.33 **Rectifier simulation at high line**

V1-> Rectifier output voltage
V2-> Load voltage
I1-> Output inductor current
I2-> Battery current

Figure F3.34 displays the simulation programs versatility. Expanding the latter time section of figure F3.33, steady state conditions are observed. Once again the results are within the worst case ratings specified (ie $V_{BAT} \cong V_{BATmin}$ and $I_{L1} \cong 55A_{RMS}$).

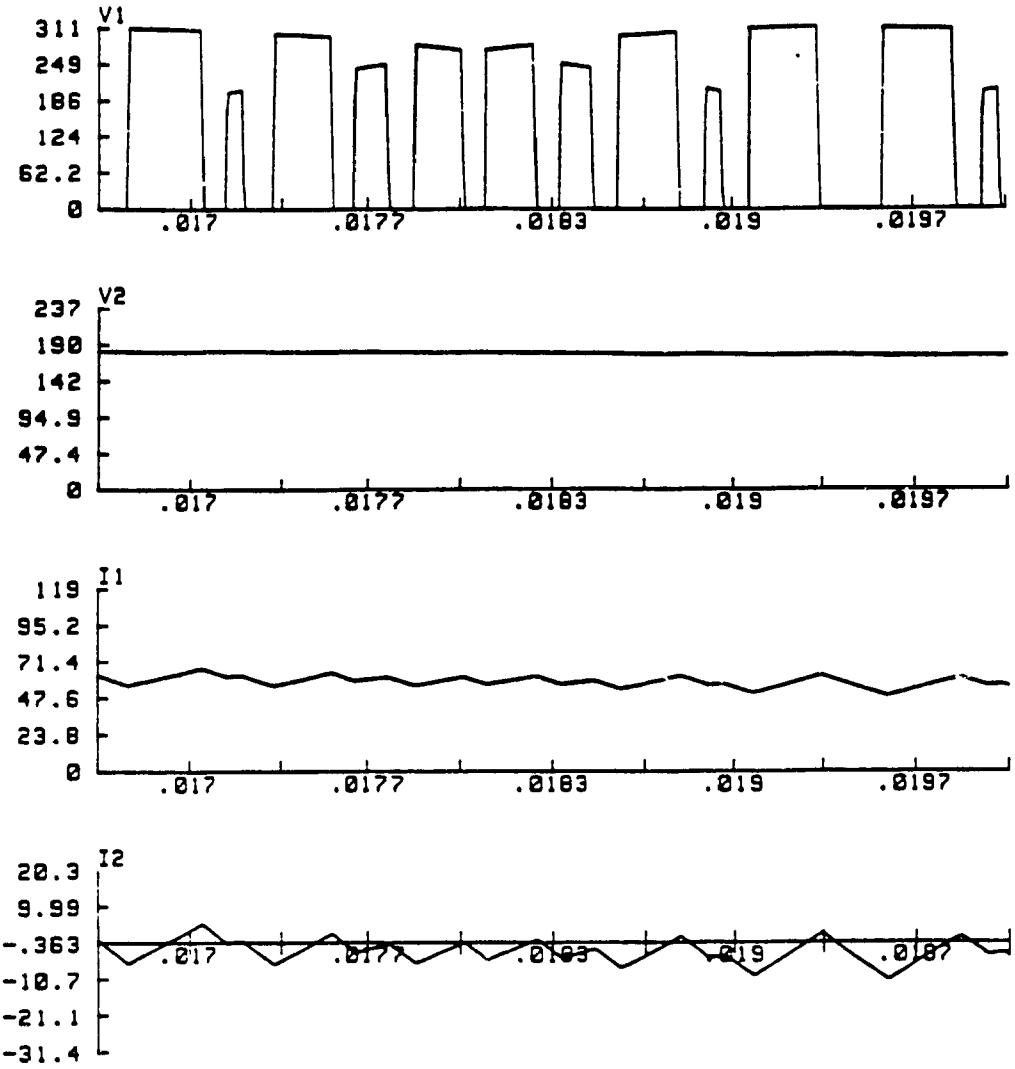


Figure F3.34 Rectifier simulation at high line (expanded time)

V1-> Rectifier output voltage
V2-> Load voltage
I1-> Output inductor current
I2-> Battery current

A second simulation was done to validate operation at full float battery voltage. The circuit conditions for the simulation are

V_{XN} = low line = 103.5 $V_{RMS\ L\text{-}N}$

M = 1

The resulting simulated waveforms are shown in figure F3.35 which reveal that the float voltage of 219 is identical with the analytical results. This indicated that even at low line and maximum battery voltage, the rectifier is

able to charge the batteries. Moreover, all results are within the worst case conditions dictated in chapter 3.3.2.

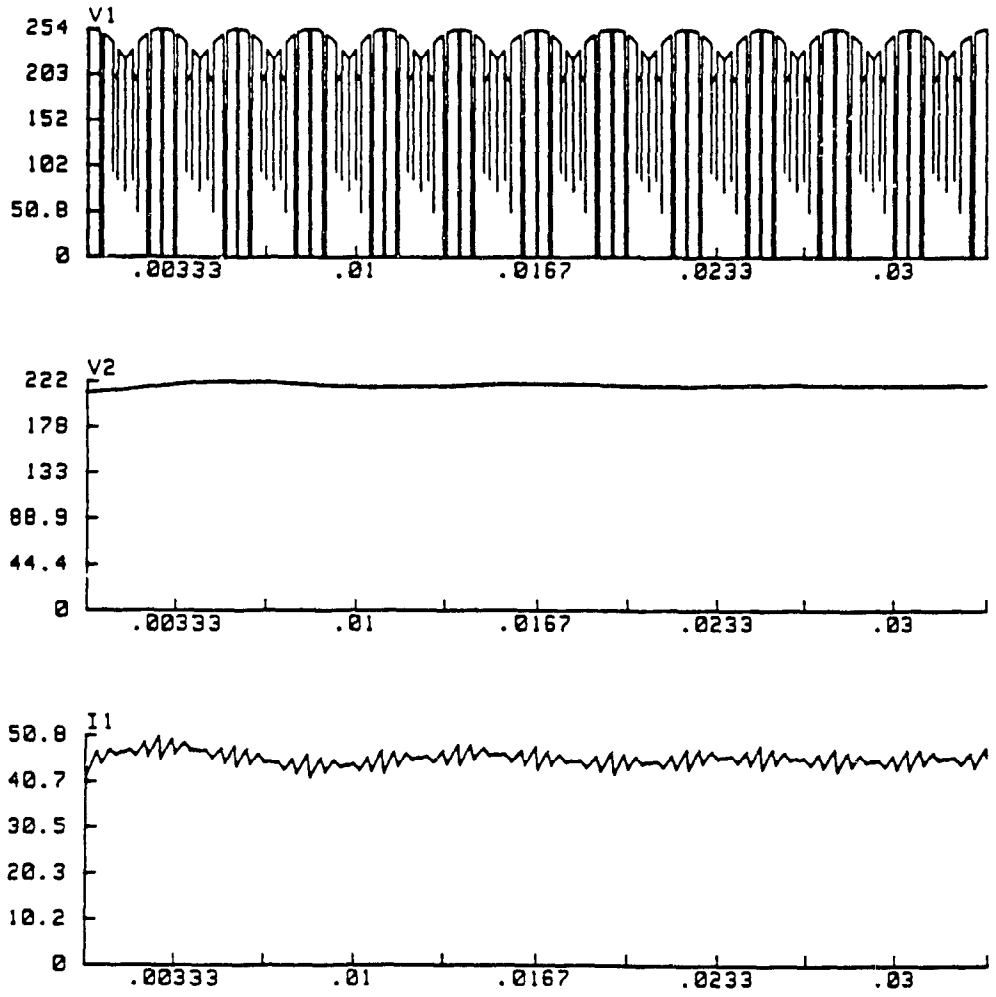


Figure F3.35 Rectifier simulation (expanded time at low line)

V1-> Rectifier output voltage
V2-> Load voltage
I1-> Output inductor current

3.4.2.3 High Frequency Link Simulation

At best, most simulation routines including the program (ASPEC) developed here, have difficulties performing accurate simulation of a power conversion stage incorporating a transformer. Removal of the transformer dramatically

simplifies the circuit to the point where simulation is a formality. Based on this only true experimental results will be used to check the validity of the HF link stage derivations.

3.4.3 Switch and Drive Selection

Proper power semiconductors cannot be chosen without consideration for their required base drives. The semiconductors considered for each stage were the GTO, MOSFET, darlington, and IGBT.

Although it is not unreasonable to mix and match alternate varieties of semiconductors in a single power unit, it is seen as a negative step towards simplification. Further, for a particular power range different semiconductors do not have a dramatic price variation. Due to these reasons the semiconductor evaluation is appendix A2 yields a single semiconductor type which can be used throughout the UPS. This will undoubtedly bring advantages in

1) design simplicity - single type drive required
2) quality testing/trouble shooting - options reduced
3) design price - through increased quantities

The high frequency link is seen as the critical power conversion stage for semiconductor evaluation since it has the highest thermal loss due both to higher switching frequencies and greater levels of current. It can be safely assumed (as far as current capabilities are concerned) that if a power semiconductor device satisfies the high frequency link environment it can be used in the inverter and rectifier stages also. The inverter stage will dictate the switch voltage blocking capabilities since it is the maximum of the three power stages. (Chapter 3.4.1) Appendix A2 evaluates the four applicable semiconductors with respect to drive considerations applied to the HF link stage. Table T3.9 shows a critical item evaluation of the

semiconductor.

SWITCH	Speed	Ruggedness	Voltage	Drive complexity	Losses
IGBT	good	good	good	good	poor
MOSFET	good	border	good	good	good
GTO	poor	good	good	poor	poor
Darling	border	good	good	border	good

LEGEND: good = acceptable for the HF link presented
border = tollerable for the HF link presented
poor = not acceptable for the HF link presented

Table T3.9 Switch evaluation criteria table summary

Via Appendix A2 and Table T3.9 it can be concluded that the MOSFET would provide the best power switching semiconductor for overall use in the proposed UPS. Using MOSFET's, good snubber and transient protection is required to avoid stresses ensuring the MOSFETS proper operation. This is detailed among the items described in practical limitations (Chapter 3.4.5).

3.4.4 Controller Circuits

Digital circuitry is often preferred over analog circuitry signals to increase noise immunity. This is especially true in locations where EMI and other similar phenomena exist. PWM is applied creating so-called 'switching noise' thereby forcing added stress on any analog small signal control circuitry. These analog components are already inherently sensitive in order to quickly provide a comparison between a sine wave reference and a high frequency triangular carrier [24]. The switching environment may inadvertently trigger a false comparison causing a possible failure. Surveys have shown that a large number [32%] of UPS down time is attributed directly to failures at the control component level specifically due to linear IC failure [17].

In view of this two of the gating control circuits in this thesis are

entirely digital. It is expected to enhance the ruggedness of the UPS by increasing its noise immunity. Furthermore, no microprocessor and associated support hardware is used.

Since the UPS contains three distinct power stages, each with its own power conversion section the controller for each is unequal and therefore presented separately.

3.4.4.1 Inverter Controller

Since the inverter stage is free from UPS output voltage control its power semiconductor devices can be gated in a consistent predetermined fashion. The PWM scheme with firing angles described in Section 3.1 can be programmed into an EPROM. As shown in figure F3.36 the EPROM is then addressed via a counter and driven by a free running clock.

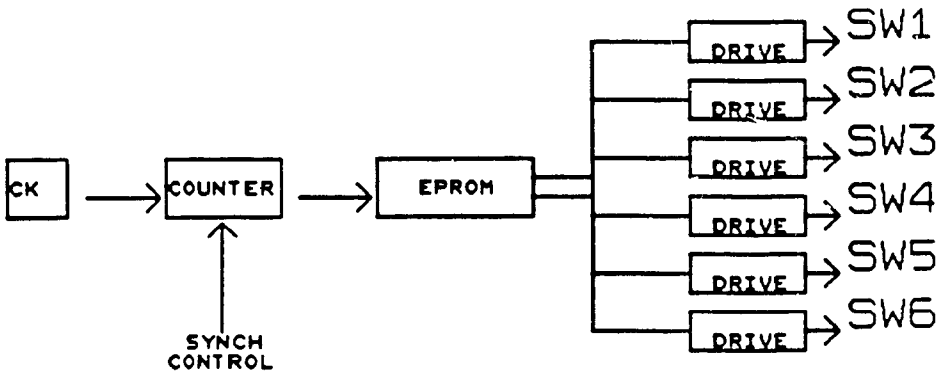


Figure F3.36 Inverter gating signal derivation

The outputs of the EPROM are steered to the six drives and activate therespective semiconductors during an EPROM output high and deactivate during an EPROM low.

A 64K (8K x 8 output) bit eprom results in a resolution of .044° which is satisfactory considering the smallest pulse to be reproduced is .21° (Table

T3.1 chapter 3.1). The counter stepping through the EPROM is a cascade connection of 4 X 4 stage counters. The clock runs at a base frequency of

$$F_{CK} = 60 \cdot 8192 = 491.5 \text{ KHz} \tag{3.252}$$

which can be accommodated by a standard CMOS clock. The final hardware configuration is shown in figure F3.37.

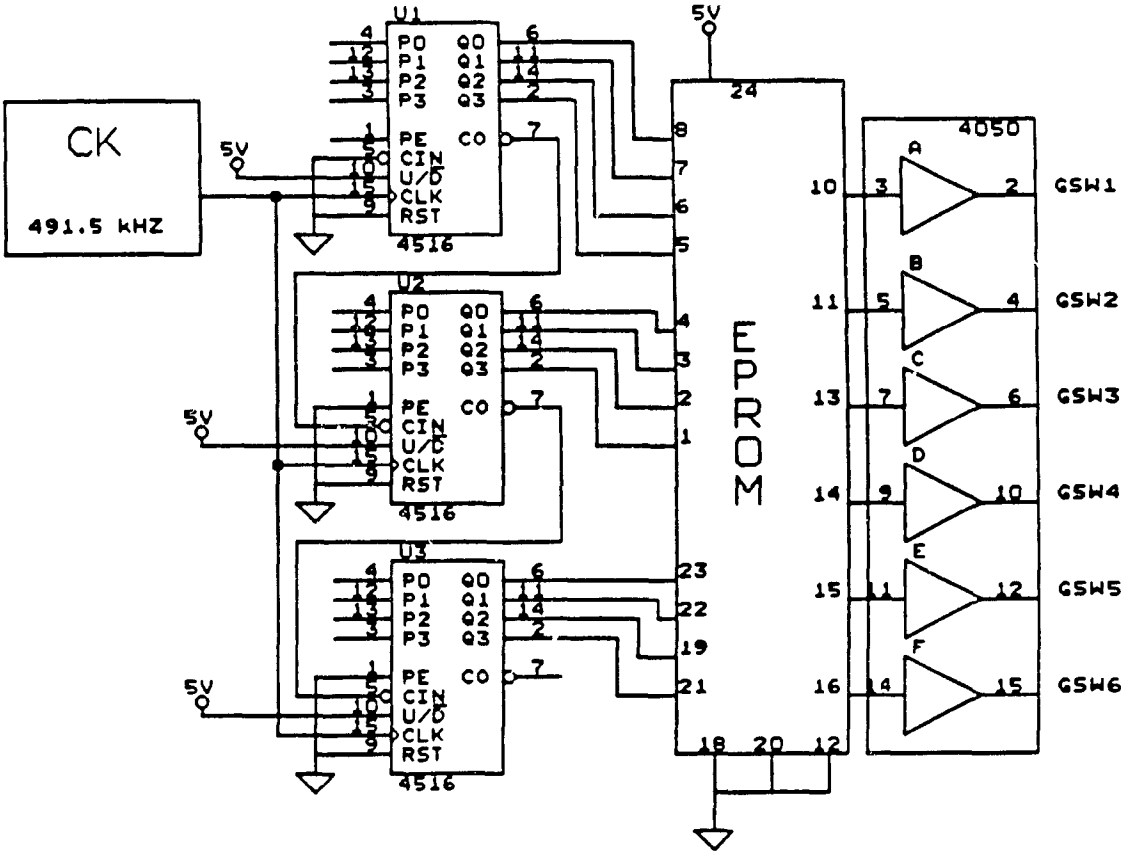


Figure F3.37 Inverter gating signal hardware

3.4.4.2 Rectifier Controller [5]

Figure F3.38 displays the first 90° of MSPWM operating on the standard controlled rectifier of figure F3.7.

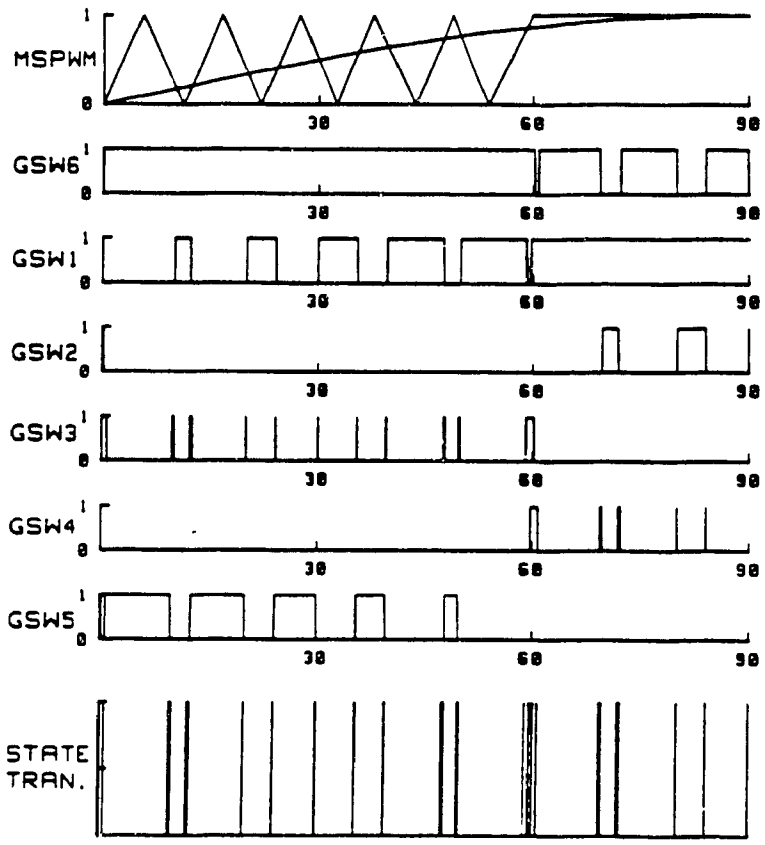


Figure F3.38 Expanded MSPWM gating signals for control derivation

A) MSPWM scheme
B) GSW6
C) GSW1
D) GSW2
E) GSW3
F) GSW4
G) GSW5
H) State Transition

Figure F3.38B shows the gating signal for switch #6 Similarly, figure F3.38C,D,E,F and G correspond to the remaining five gating signals of the rectifier respectively. Figure F3.38H shows each occurrence of a switch transition represented as a state change. The key point to observe is that the order of state changes as they occur in time is rigidly fixed and is thus independent of the modulation index. [i.e. State change #2 always appears before state change #3 and always after state change #1]. All PWM techniques which exhibits this feature is can be executed by the control circuit presented. This feature ensures that there is no dramatic load current change

due to pulse inconsistencies or 'wandering' as modulation index changes. Each of these state changes (corresponding to a particular angle) is stored as a 12 bit binary number in a standard EPROM. (See figure F3.39). When a particular address is presented to the input of EPROM, its associated 12 bit binary angle is placed on the output along with three multiplexed control signals representing the state of the rectifiers six switches (on or off) after the binary angle is reached.

Figure F3.39 shows a block diagram of the control schematic. In particular, counter 'B' is a 12 stage (4096 count) counter.

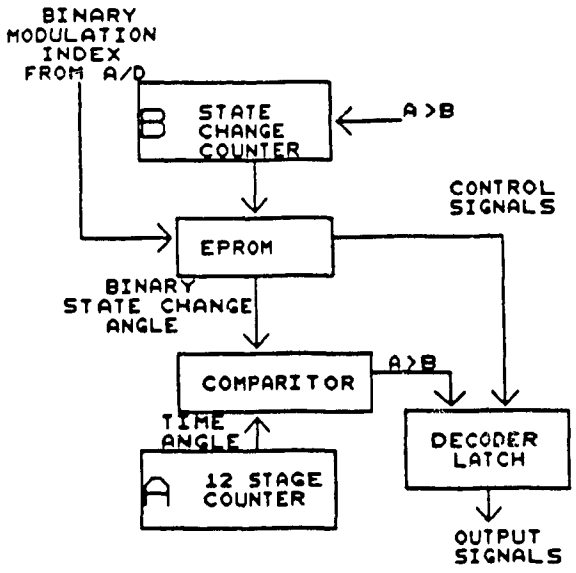


Figure F3.39 Control block diagram

The counter may be externally reset and synchronized to input hydro frequency, locking the gating signals with the input line voltage. Each count places a binary 12 bit angle on its output. (i.e. 0000/0000/0000=0^0 1111/1111/1111=360^0). This binary angle is fed into a 12 bit magnitude comparator which compares this signal with the 12 bit angle existing on the output of the EPROM. Assuming momentarily that the modulation index is held

constant, the output of the EPROM is held until the angle output by the counter 'A' exceeds the angle output of the EPROM. At this instant the comparator releases a pulse followed by the latching of the three switch control signals. Further, the pulse enables counter 'B' which increments the EPROM output to the next higher angle at which a state change exists. Eventually, the free running counter 'A' will again exceed this angle producing again a pulse changing the switch signals and EPROM output.

Changing modulation index is accommodated by simply using a different EPROM section containing those angles associated with the new modulation index. The comparator output allows the master clock to pulse through to counter 'B' providing a catch up action should the new modulation index angle be smaller than the output of counter 'A'. This rapidly increments counter 'B' until its output exceeds once again counter 'A' allowing the comparator output to fall inactive again. Since the pulse cannot 'wander', the switch signals merely change width. This smooth change can be seen in figure F3.40.

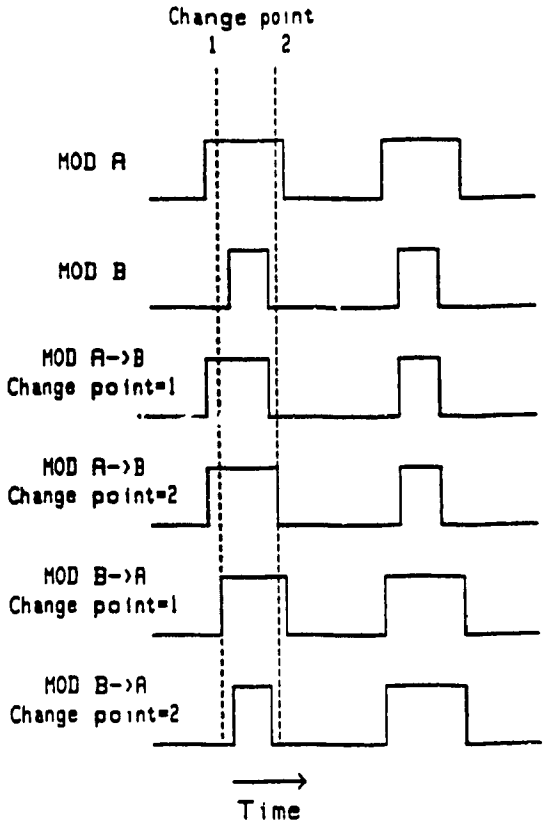


Figure F3.40 Digital modulation change

In particular figure F3.40 shows two different modulation index's and the resulting switch signals when the modulation index is changed to either points 1 or 2. Note that modulation corrective action can only be taken at the upcoming intersection and the switch signals cannot be altered until such time. The result is a smooth crossover from one modulation index to another.

As stated earlier the main qualifying requirement for a PWM technique employed by this control is that the state changes occur in a pre-defined, consistent order independent of modulation index. A number of schemes fill this prerequisite including the Modified pulse Width Modulation technique derived as most compatible in section 2.4.

The full circuit schematic is shown in Appendix A3. All parts including the EPROM'S are readily available. The main clock is simply composed of two

series inverters with an R-C charge/discharge type arrangement. The modulation index adjustment is accomplished by an A/D converter. Since the total number of state changes is not an integral binary number, a reset is provided for the EPROM counter consisting of simply an 'AND' gate. The comparator output is buffered using a 4050 Buffer/Driver and then latched. Simple CMOS D type flip-flops are used as latches and provide the multiplexed control signals for all six rectifier switches. All logic is powered from a single 5 volt supply.

3.4.4.3 High Frequency Link Controller

Current mode control has been widely accepted as a high performance converter controller. Pulse by pulse current limiting ensures overcurrent protection, transformer saturation protection, and enhanced loop response. The enhanced loop response is due to a reduction of open loop transfer function order from 2 to 1. Moreover, a large number of integrated circuits [IC] dedicated to current mode control are available. Figure F3.41 shows a typical current mode control IC [49]. After voltage and current feedbacks are applied and the gating signals are digitally processed.

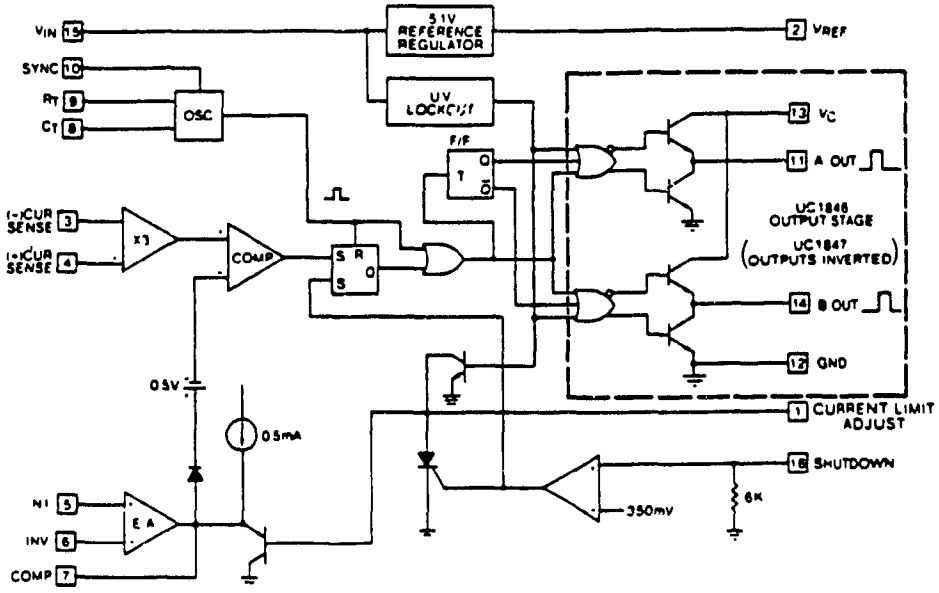


Figure F3.41 Current mode control chip 3846

Figure F3.42 shows the circuit schematic used for the high frequency link stage. Since this thesis does not address loop optimization the feedback compensation components are unoptimized.

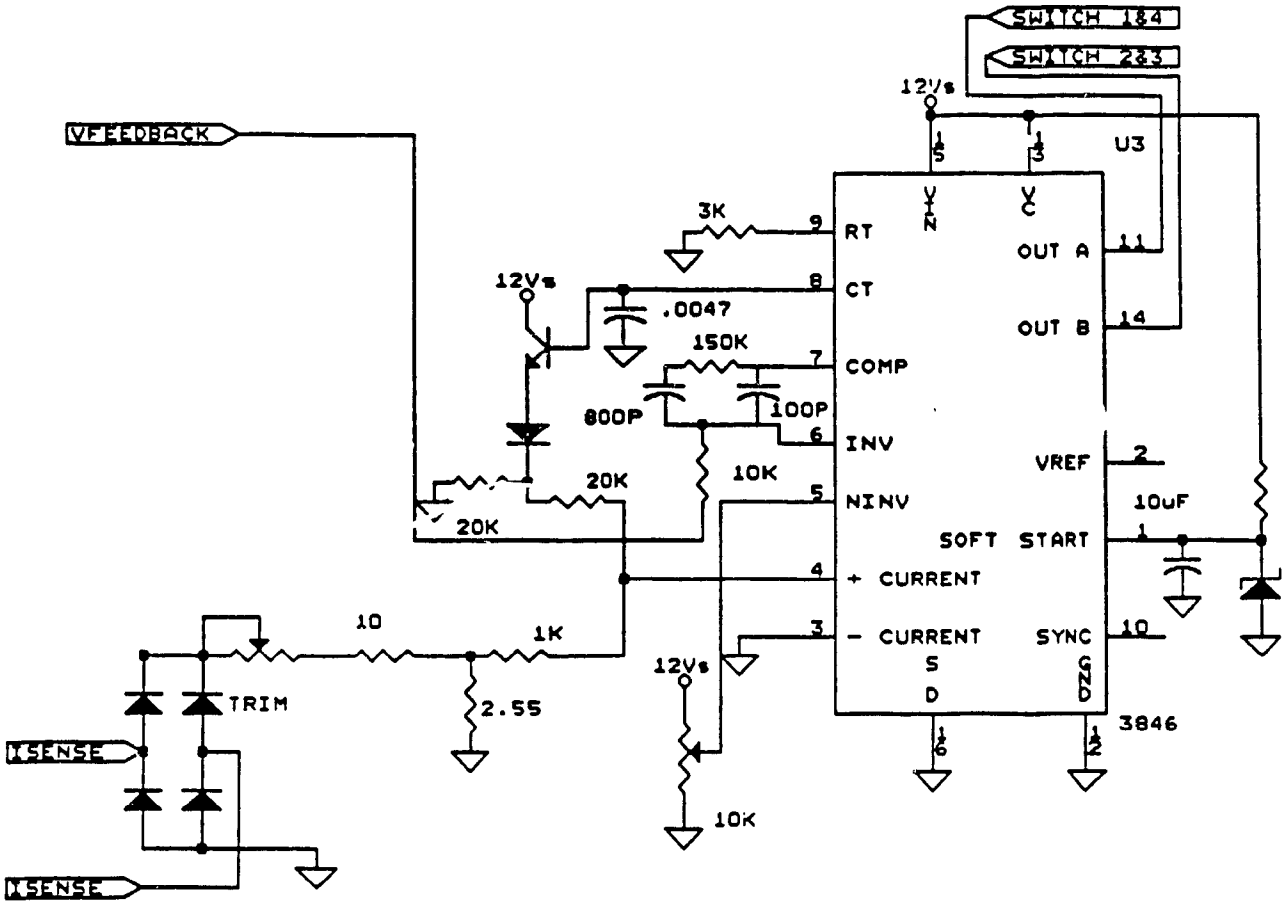


Figure F3.42 HF link control using the 3846

3.4.5 Practical Limitations

Although theoretical analysis can often provide sufficient results, once practical hardware is utilized a number of real world phenomena play a significant part in the design. To the knowledge of the author no modern power (10KW) super sonic high frequency link has to date been developed. Since no previously published data is available on the "hidden" characteristic problems of such a converter, several prominent phenomena experienced are discussed in this section.

3.4.5.1 Snubbers

Unlike ideal semiconductors practical devices dissipate heat and will experience voltage overshoot. Snubbers, whether lossy or lossless are essentially required for all semiconductors in the UPS.

The MOSFET snubbers used in the inverter and high frequency link stage are identical and are shown in figure F3.43.

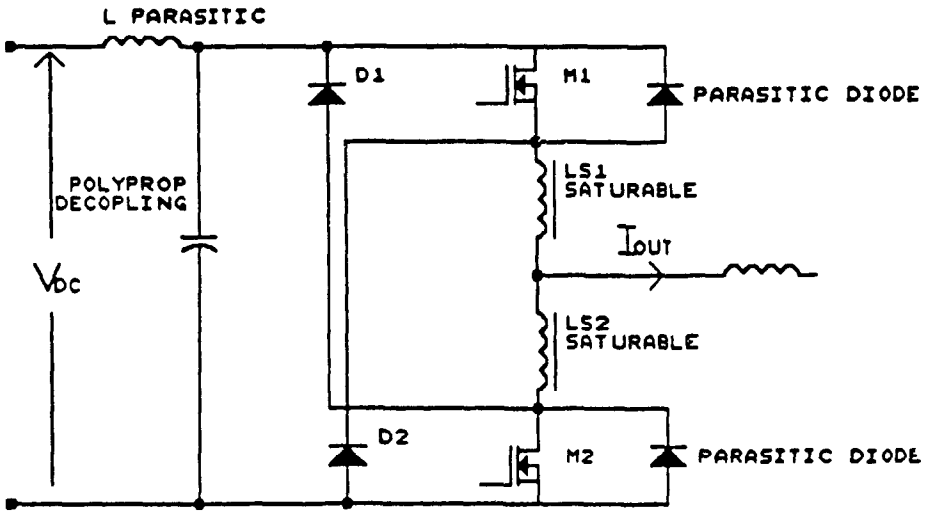


Figure F3.43 HF link and inverter MOSFET snubber

This snubber performs three essential functions for MOSFET utilization.

1) The saturable reactors L_{s1}, and L_{s2} tend to isolate the power MOSFETS so that when one is enabled the semiconductors parasitic capacitance (gate to drain and gate to source) cannot conduct current to the alternate MOSFET. This helps to prevent unintentional MOSFET conduction.

2) The disabling of the parasitic MOSFET body diodes is accomplished by the ultra fast diodes D_1 and D_2 as well as the saturable inductors L_{s1} and L_{s2}. Consider MOSFET M_1 conducting forward current and MOSFET M_2 inactive. Saturable L_{s1} is saturated and L_{s2} is at worst case at its residual flux level. Turning off MOSFET M_1

with inductive output current would tend to cause diode D2 to conduct rather than the parasitic diode of M2 which would first require the saturation of Ls2. This effectively disables the parasitic diodes.

3) The ultra fast diodes in combination with the decoupling capacitor prevent significant voltage overshoot across the MOSFETS.

The transformer secondary diodes require snubbing or protection from reverse recovery problems. Since current is exchanged between these two diodes abruptly, as one goes into reverse recovery it essentially provides a short circuit to the second diode resulting in tremendous current spikes. Figure F3.44 shows a commonly used solution which is also used in this thesis. The saturable reactors are rated to hold diode reverse voltage for roughly two times the reverse recovery times before saturating. This guarantees safe commutation.

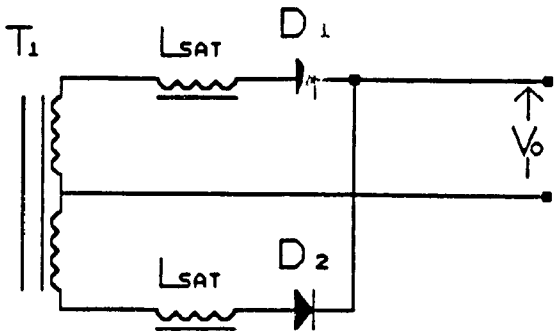


Figure F3.44 Output diode reverse recovery snubbing

The saturables used are an amorphous type from Toshiba having an area of .10 cm^2. The secondary peak voltage is roughly

$$V_{DR} = \frac{2 \cdot V_{INMAX}}{NN} = 4.945pu = 804.4 \text{ Volts} \qquad (3.253)$$

Ultra fast diodes typically take 50NSEC to recover. Therefore

$$Ns = \frac{V_{DR} \cdot (2 \cdot T_{RR})}{\phi_s} \qquad (3.254)$$

Letting ϕ_S $=390 \cdot 10^{8}$ Webers (from Toshiba)

T_{RR} =50NSEC (Reverse recovery time)

V_{DR} =804.4 V

Ns =Number of turns on core

we obtain

Ns =8.688 Turns

This implies that nine turns around this saturable reactor are required to hold off reverse recovery.

The controlled rectifier semiconductor snubbers are typically diode-resistor-capacitor snubbers as shown in figure F3.45.

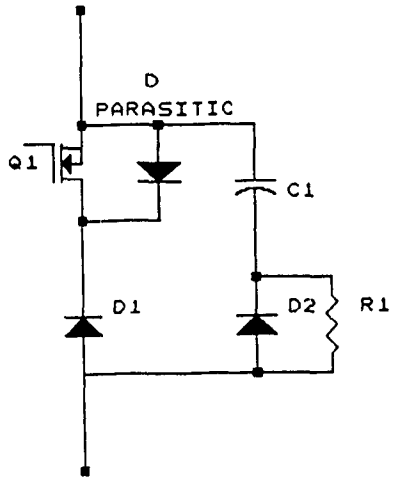


Figure F3.45 Rectifier MOSFET snubber

Diode D1 is required to prevent the MOSFET parasitive diode from conducting

which would destroy the bridge. Diode D_2 simply provides a path for parasitic inductive energy to flow when the semiconductor is turned off. Capacitor C_1 charges with this energy preventing voltage overshoot. The energy is then dissipated at the next switch turn on via R_1. C_1, can be selected based on a realistic measure of 100nH. By equating energy

$$CV^2 = LI^2 \tag{3.255}$$

for a voltage overshoot of 50V

$$C_1 = \frac{100\text{nH} \cdot (58.4)^2}{50^2} = 136\text{nF}$$

The resister R_1, must bleed this energy roughly four times faster than the switching frequency or using the time constant

$$R_1 \leq \frac{\frac{1}{60\text{Hz}} \cdot \frac{1}{(\text{Fsw pu})}}{4 \cdot C_1} \tag{3.256}$$

where Fsw pu = 22pu

Evaluation results in

$$R1 \leq 1.39\ \text{K}\Omega$$

The power loss is the energy of the capacitors or

$$P_{LOSS} = F_{SW} \cdot 60 \cdot .5 \cdot C_1 \cdot (V_{SWPK} + V_{OVER})^2 \tag{3.257}$$

where $V_{OVER} = 50\text{V}$

$$= 22 \cdot 60 \cdot .5 \cdot 136\text{N} \cdot 359.9^2$$

$$= 11.6 \text{ Watts}$$

3.4.5.2 Layout Requirements

The major problem at the layout level is lead inductance. At this power level and switching frequency, the minimization of track length is not sufficient. The internal wire leads of components themselves are occasionally enough to create problems. The high frequency link power semiconductors are of particular interest. Even if a snubber is located simply one inch away, the combined component-lead inductance may be 100nH. Since the drive designed is expected to turn the semiconductor off in roughly 100nsec, the voltage overshoot across the semiconductor may be

$$V = L \cdot \frac{\Delta I_{LP}}{\Delta T} = 100_N \cdot \frac{73.62}{100_N} = 73\ V \qquad (3.258)$$

This is already 35% of the nominal switch voltage (V_{SWPK}) and forces over sizing the switch even with a careful snubber design. In fact for all switching semiconductors used here, the snubber components were connected terminal to terminal with no intermittent leads in order to minimize inductance loop length.

If any leads were necessary, their cross sectional areas were selected on the basis of inductance as well as current carrying capacity. Figure F3.46 shows the loop length to be minimized.

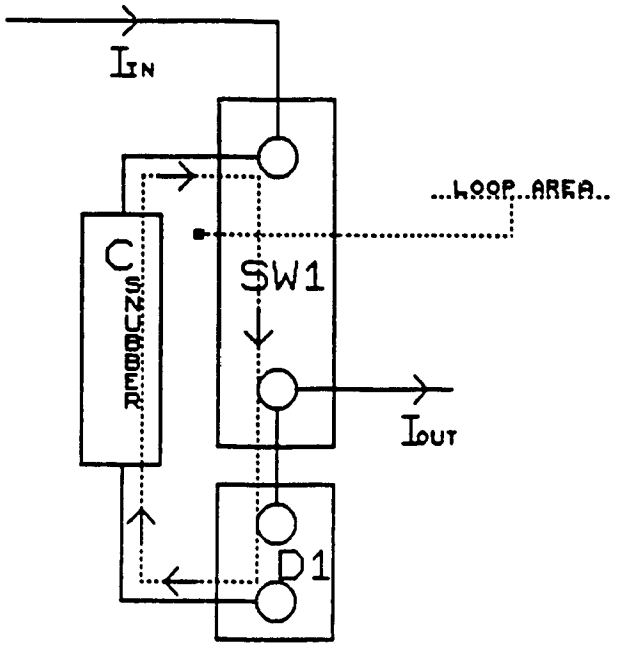


Figure F3.46 Critical current loop of MOSFET semiconductors

A second area of concern is the transformer primary power loop area. The UPS radiated Electromagnetic Interference (EMI) will be directly related to the loop area of the pulsed power current. Consequently minimal loop area must be maintained. Figure F3.47 shows a typical full bridge configuration with power loop area enclosed by the dashed line.

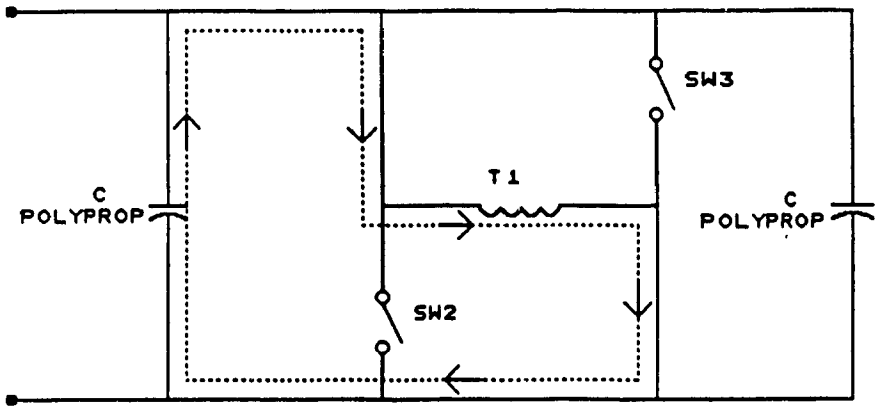


Figure F3.47 Typical inverter pulsed current loop area

Figure F3.48 shows an alternate circuit layout used in this thesis to minimize the loop area [4].

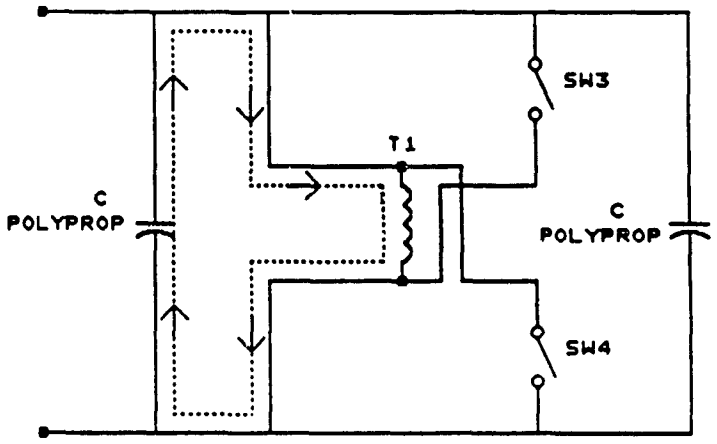


Figure F3.48 Improved inverter pulsed current loop area

3.4.5.3 Switching Deadtimes/Overlaps

Power bridge configurations such as the high frequency link and inverter used here are known to experience dramatic failure if cross conduction occurs. The bus short circuit via semiconductors can be avoided by the application of deadtimes between alternate gating of the semiconductors of the same leg. A detailed gating sequence is shown in figure F3.49. This deadtime guarantees that SW1 and SW2 are never on simultaneously.

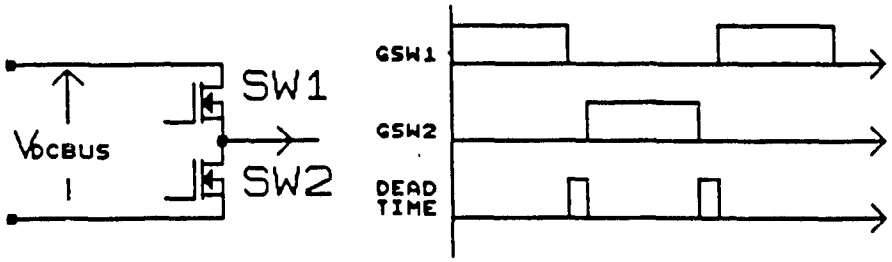


Figure F3.49 HF link and Inverter switch deadtime

The controlled rectifier however experiences the dual problem. Figure

F3.50 shows this in detail.

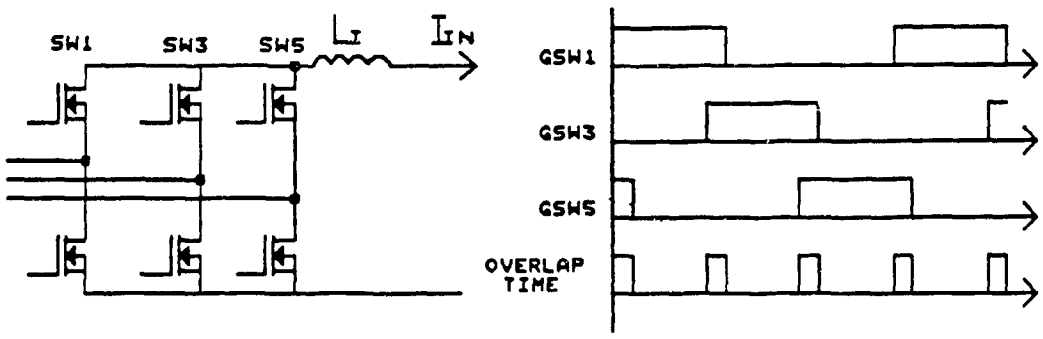


Figure F3.50 Rectifier switch overlap

Smoothing inductor LI tends to draw continuous dc current. If neither SW1, SW3 or SW5 are conducting then the interruption of current will generate a large voltage spike across the semiconductors. To ensure this does not happen, overlaps are given to the semiconductor gating signals which tend to guarantee a current path for IIN.

3.4.5.4 Transformer Saturation

A problem associated with a voltage driven inverter stage coupled to a load through anisolation transformer, such as the high frequency link, is the possibility of transformer saturation. This occurs if any unbalance of gating signals or semiconductor conduction voltage drop occurs. A dc voltage will be present across the transformer which will saturate the core.

Saturation can be prevented with suitable control logic such as Current Mode Control. This control method monitors the transformer primary current and thereby adjust the duty cycle of the semiconductors to offset any transformer current unbalance.

3.4.6 Experimental Results

To verify the theoretical derivations and concepts, selected experimental results were obtained on a full scale 10kVA engineering model. All the practical considerations were fully utilized.

3.4.6.1 Inverter Stage

The inverter section of figure F3.25 was constructed. Figure F3.51 shows the resulting output line-line voltage waveform. The waveform shape is similar to that of figure F2.19B. Switching delays have eliminated the inner pulses. To confirm the integrity of the waveform a spectrum analysis was performed resulting in figure F3.52B. The spectral content clearly matches that of figure F2.19C indicating that the eliminated pulses have no detrimental effects. The peak voltage of figure F3.51 is seen to be similar that of figure F3.31. (A factor of $\sqrt{3}$ is required in order to convert from line to line to line to neutral). From figure F3.51 the peak voltage is roughly 258 volts. From figure F3.31 the peak line to line voltage is 244 volts. This difference is reasonably attributed to circuit losses with were neglected in the simulation.

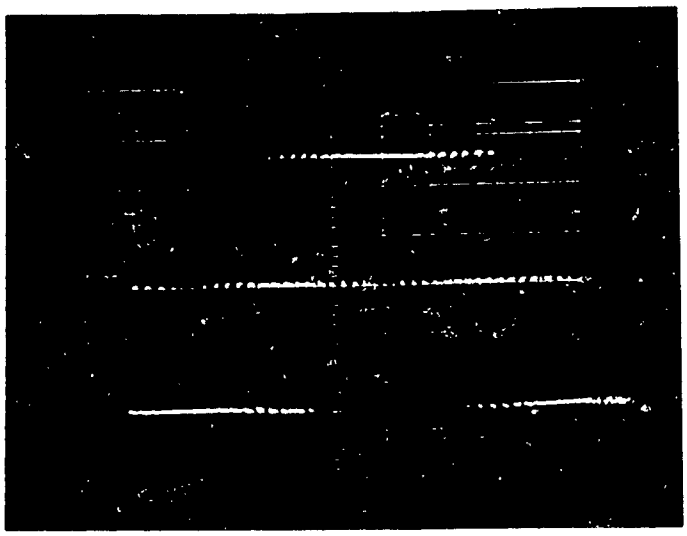


Figure F3.51 Experimental inverter line to line voltage 100V/div

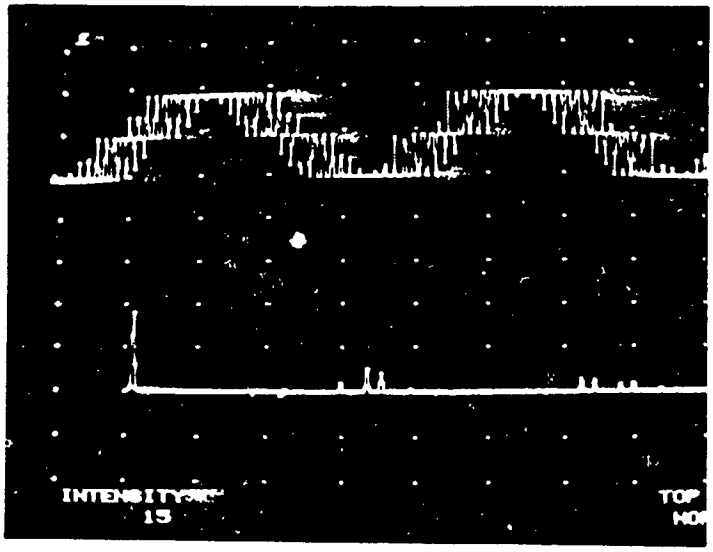


Figure F3.52 Experimental inverter line to line spectrum

A) line to line voltage

B) line to line voltage spectrum.

Figure F3.53 shows the output line current and the switch current for unity power factor load. The results show complete agreement with the worst case ratings program waveform results. Even the slightly lagging current between the output line current and switch current as predicted is evident. The only dissimilarity is noticed when comparing the dips of switch current to zero value in figure F3.31 which do not exist in figure F3.53. This is knowingly attributed to the disadvantage of having the catch diode in such close proximity to the MOSFETS (minimizing inductance) that the experimental switch current shown includes the catch diode current.

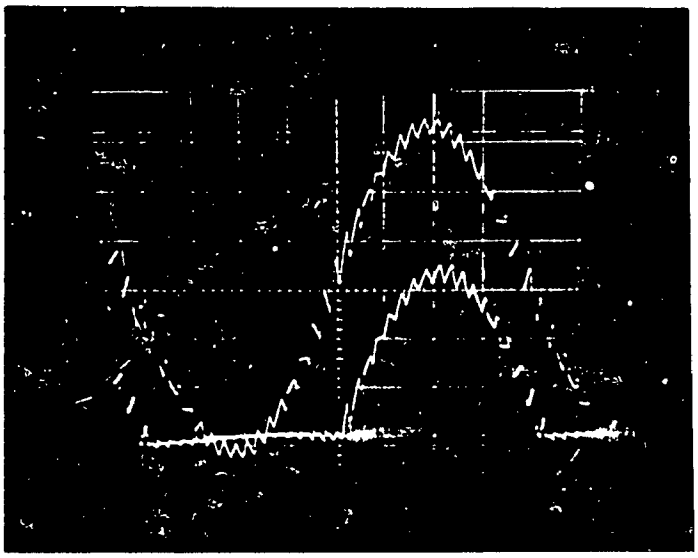


Figure F3.53 Inverter switch and output line current

A) Output line current 10A/div

B) Switch current 10A/div

Figure F3.54 shows the output line to neutral load voltage and the inverter output line current as a phase reference. The waveform shapes and

quantities again agree with figure F3.31. Figure F3.55B displays the spectrum of the output load voltage and has a THD in the area of 1.5%.

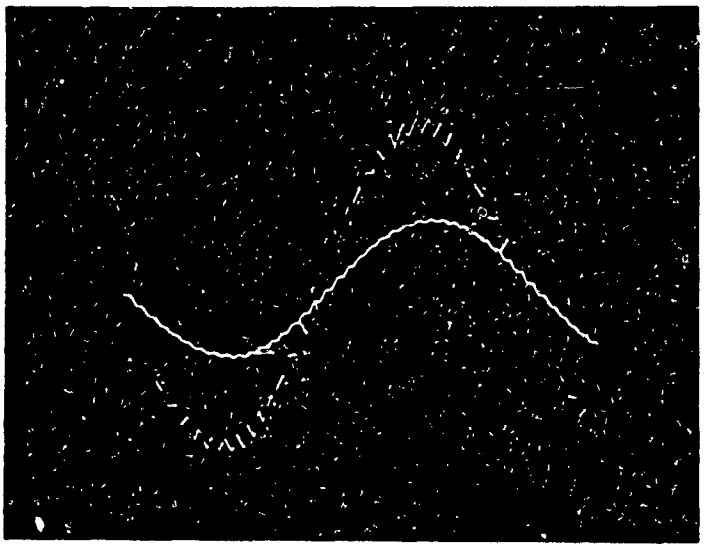


Figure F3.54 Experimental inverter load voltage

A) Inverter output line current 10A/div

B) Inverter output line to neutral voltage 100V/div

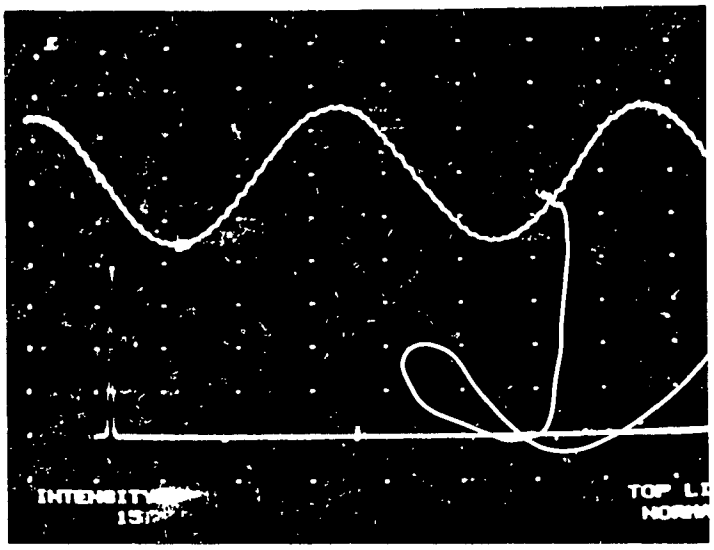


Figure F3.55 Experimental inverter output voltage spectrum

A) Inverter output line to neutral voltage

B) Inverter output line to neutral voltage spectrum

3.4.6.2 High Frequency Link Stage

The full bridge inverter of figure F3.23 was constructed. Due to limited components at high power and high frequency applications the transformer turns ratio was .533:1 rather than the required .546:1 (chapter 3.3.3). Further, the output filter utilized was 85μH rather than the required 240μH (chapter 2.4.1.3). This however should only affect the output current ripple and consequently the output voltage ripple. To compensate for this a larger output filter capacitor is used. The larger value of capacitance is necessary since the high output current ripple (5 amps rms) and high voltage require a relatively large electrolytic. Full two loop current mode control was employed as shown in figure F3.42.

Experimental results were taken at a typical operating point of

V_{BAT} = 200V

V_{DCBUS} = 300V

resulting in a required switch duty cycle of D=.4. Operating at full power of 10kw, the load was set to 9Ω. Switch voltage and switch current are shown in figure F3.56 and figure F3.57 respectively.

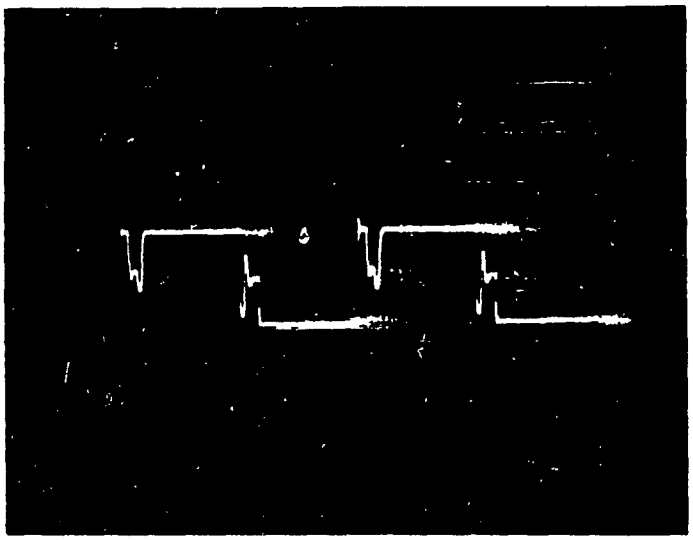


Figure F3.56 HF Link MOSFET drain source voltage. 100V/div 10μs/div

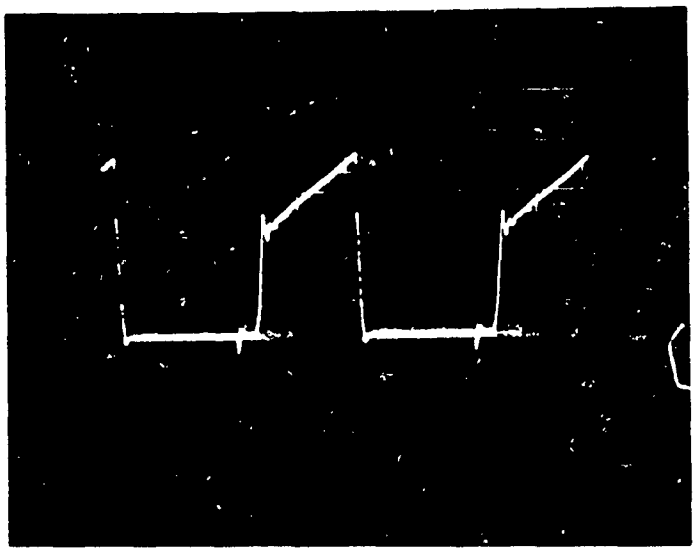


Figure F3.57 HF link MOSFET current. 20A/div 10μs/div

In particular, figure F3.57 shows the current mode control limiting the switch current to 72 amps peak. Further, the initial spike of current is the result of the reverse recovery of the output diodes. Without the saturable reactors (equation 3.254) the spike would be substantially higher and would falsely trigger the current mode control loop. Figure F3.56 shows the effective snubbering of the switching MOSFET's. The voltage overshoot is limited to roughly 20%. The oscillations during the deadtime can be attributed to the effective LC combination of the primary transformer leakage and the parasitic MOSFET capacitance.

Figure F3.58 shows the Transformer primary current. The figure reveals that unless the output choke is reasonably sized, the peak current that the switch must commutate will rise thus leading to increased switching losses.

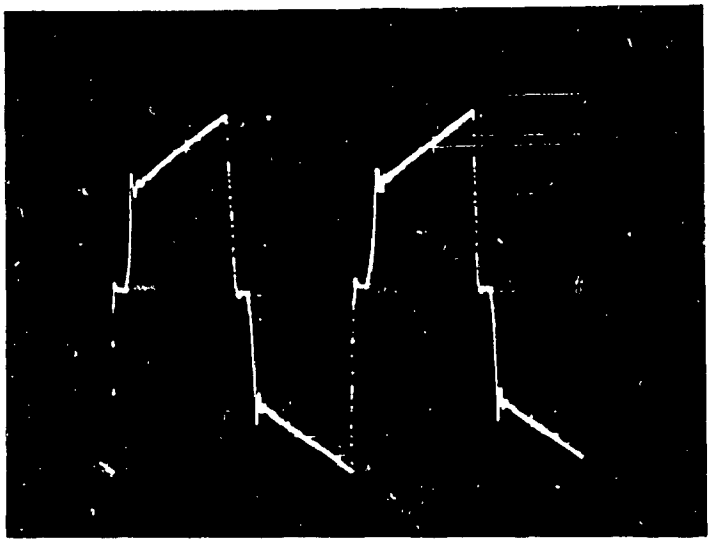


Figure F3.58 HF link transformer primary current. 20A/div 10μs/div

Figure F3.59 shows the output diode voltage. The substantial overshoot of 33% is a clear handicap. At maximum input voltage of 220V the peak diode reverse voltage will be in the order of 1075V. The maximum ultra fast diode presently available is rated at 1000V. Figure F3.59 shows this limit to be reached with further increase resulting in possible destruction. Snubbing this with an RC configuration would reduce the overshoot at the expense of higher power loss.

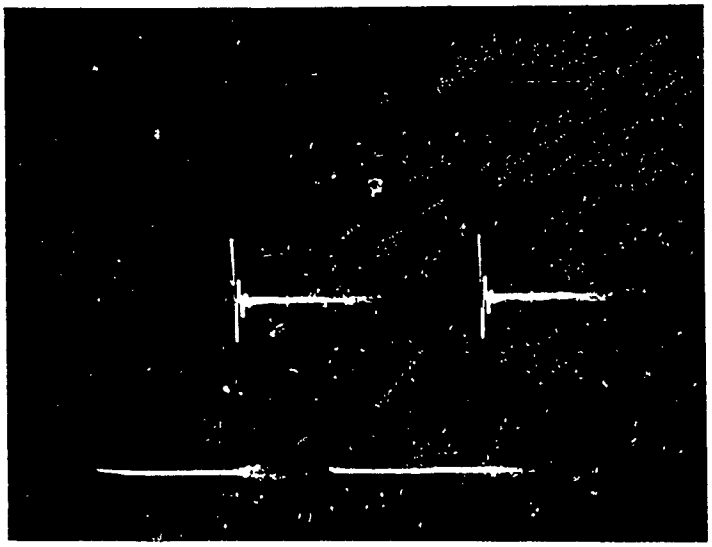


Figure F3.59 HF link output diode reverse voltage 200V/div 10μs/div

The output choke current is shown in figure F3.60. With an output voltage of 300V, the expected peak to peak ripple current should be 18A. The experimental current waveform verifies this result.

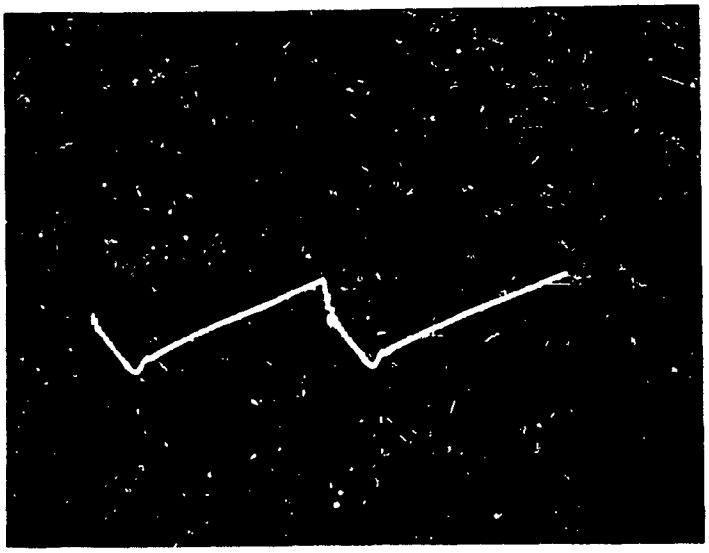


Figure F3.60 HF link output inductor current 10A/div 5μs/div

3.4.6.3 Rectifier Stage

The rectification stage was not experimentally verified, however it is felt that experimental verification of the inverter simulation results yield full credibility to the simulation results for the rectification stage.

3.5 Conclusion

The advanced high performance UPS topology designed was intended to address the specifications of chapter 2.2. In particular, the input controlled rectification stage accommodates input supply variations of +/-10%, output battery float/discharge levels, output power factor ranges of .7 leading to .7 lagging and input power factor of .9 as low as 50% rated load. Via simulated and experimental results, the three stage UPS topology has been shown to follow analytical derivations and adhere to the required technical specifications with the exception of unbalanced and nonlinear loads which are

dealt with in chapter four.

Efficiency of the inverter stage was 94% for a balanced, resistive, rated load. The efficiency of the high frequency link was measured to be 94% at nominal conditions. The expected efficiency of the rectifier is 92%. The overall UPS system efficiency is 81%.

By eliminating the low frequency transformer from the high performance topology, a weight reduction of 100kg is expected. Application of highly compatible PWM techniques for the rectification and inversion stages has further reduced reactive component size. These efforts are directed towards the physical specifications of light weight and small size.

Evaluating several high frequency link topologies yielded the full bridge as the best suited for the power range of 10kVA. The forward converter although simple, was ruled out due to the lack of available components. The half bridge was not suitable due to excessive semiconductor stresses.

The expected UPS volume and density is based on the high frequency link and inverter prototype as well as estimated rectifier parameters. Table T3.10 provides a summary of the data.

ITEM	VOLUME	BASIS
Inverter	2500 IN^3	prototype
Rectifier	2500 IN^3	estimate
HF link	2000 IN^3	prototype
Miscl./trans. sw.	1000 IN^3	estimate
SUB TOTAL	8000 IN^3	N/A
Contingency	800 IN^3	10%
TOTAL	8800 IN^3	N/A

Table T3.10 UPS volume summary

The power density based on the volume results in a value of 1.136w/in^3

which is 14% higher than the specifications outlined in chapter 2.2 and roughly 100% higher than typically existing UPS.

A rudimentary itemized weight list for the UPS is presented in table T3.11.

STAGE	ITEM	BASIS	WEIGHT
Inverter	Heatsink & fan	prototype	23 lbs
	Semiconductors, busbars & snubbers	prototype	8 lbs
	Output filter	prototype	40 lbs
	Drive & logic	prototype	4 lbs
Rectifier	Heatsink & fan	estimate	23 lbs
	Semiconductors, busbars & snubbers	estimate	10 lbs
	Output Filter	estimate	20 lbs
	Drive & logic	estimate	4 lbs
HF link	Heatsink & Fan	prototype	27 lbs
	Semiconductors, busbars & snubbers	prototype	10 lbs
	Input filter	prototype	5 lbs
	Output filter	prototype	15 lbs
	Transformer	prototype	12 lbs
	Drive & logic	prototype	4 lbs
Miscl.	Enclosure, supports & clamps	estimate	205 lbs
	Transfer Switch	estimate	30 lbs
SUB TOTAL	N/A	N/A	440 lbs
Contingency	N/A	N/A	40 lbs
TOTAL	N/A	N/A	480 lbs

Table T3.11 UPS weight summary

The total weight results in a weight ratio of 45 w/kg which exceeds the outline's specifications and surpasses typical market UPS by 300%.

To reduce switching semiconductor application complexity, a single semiconductor type and drive circuit were employed throughout the three power stages. Evaluation of several suitable semiconductors yielded the MOSFET as a

preferred semiconductor.

To ensure limited susceptibility to radiated and conducted noise, digital gating signal controls were designed for two of the three stages. Although no quantitative measurements were taken, experimental results proved complete EMI immunity.

Experimental verification with a 10kw prototype revealed practical limitations not typically addressed in the literature. Layout requirements, lead inductance, radiated magnetic EMI, snubber design, switching deadtimes/overlaps and diode reverse recovery were determined to be of critical value to the experimental setup. These issues were outlined in chapter 3.5.

Finally, although simulated and experimental results were completed at 10kw, the component values and stresses are evaluated in per unit format permitting scaling to other power levels.

4.0 SPECIAL LOAD CONSIDERATIONS

With the drive towards low maintenance and complete automation, an increasing number of newly-developed equipment, highly sensitive to mains disturbances have emerged including:

1) Telecommunications equipment (PBAXs).

2) Main-frame computers.

3) System Monitoring devices.

4) Robots for automation.

5) Data acquisition systems.

6) Traction rectifier sets.

Since equipment of this kind provides value added performance, their employment is becoming widespread. The typical modern UPS is designed to accommodate balanced linear loads, which in the past were the majority. However, the new types of loads are not necessarily balanced or linear and can create conditions where the typical UPS inverter stage can no longer maintain waveform specifications, possibly leading to load failures as well as a reduction of inverter MTBF.

Since the primary cause of self-induced unfavorable operation conditions is the output impedance of the inverter filter, a zero output impedance inverter stage would provide balanced output voltages independent of the load conditions.

As a result, several proposals have emerged including 3-ϕ voltage coupling, transformers [50], [51], filter resonant traps [52], [53], and unbalanced inverter switching functions [54], [55]. These techniques have attained relative success in making the UPS more load compatible. However,

they fail to be a substantial step towards a universal, low impedance, high power UPS inverter stage.

This chapter provides a qualitative categorization of a variety of nonlinear and unbalanced loads encompassing their origin and effects on the UPS inverter including the severe irregularities induced on the DC link waveforms. Further, the aforementioned techniques of handling nonlinear and unbalanced loads are briefly evaluated clearly showing their attributes and drawbacks. These results lead to the derivation of a low impedance UPS inverter design with a strategically selected output filter in combination with an advanced PWM technique enabling clean power delivery to a wide variety of unbalanced and nonlinear loads. Other advantages include the following:

1) With a low impedance inverter only average voltage needs be sampled thus simplifying the control.
2) Utilization of advanced PWM techniques allows reduction in switching losses permitting higher power operation.
3) Fast transient response due to small reactive components.

4.1 Categorization of Loads

Modern static UPS inverters of all power ranges typically employ PWM techniques which inherently generate unwanted voltage harmonics along with the required fundamental. The application of a second-order LC-type low-pass filter is commonly implemented to attenuate these harmonics. However, the fundamental will experience a magnitude change and a phase shift induced primarily by the filter in conjunction with the load applied. The application of 3-ϕ balanced loads such as AC motors produces, by symmetry, equal magnitude and phase displacements. Consequently, the load experiences no self-induced terminal voltage distortion. Furthermore, since the line currents are

inherently balanced, the inverter input filter need be designed only for traditionally existing input current harmonics which are present at multiples of six times the fundamental frequency. Excluding fault conditions, potentially damaging load situations can be broadly divided into two categories.

1) Unbalanced loads which include a number of combinations of 1-ϕ and 3-ϕ phase linear loads leading to unequal individual inverter leg power factors. Moreover, utilization of only one or two phases of a three-phase system constitutes an unbalanced load from the battery point of view because of its reflected effects on the DC link current.
2) Nonlinear loads which induce voltage harmonics at the output of an inverter because of their harmonic current demand. A number of such loads exist, including:

a) Switching regulators with capacitive input power supplies.

b) Phase-controlled rectifiers.

c) Highly capacitive saturated magnetic transformers.

d) Main-frame computers (especially during start-up).

e) Traction rectifier sets.

f) Metering devices.

g) Gaseous discharge lamps, including fluorescent lights.

h) Arc furnaces.

i) Switching power supplies without primary transformers.

j) Ferro-resonant transformers.

Figure F4.1 shows a generalized categorization of the various types of loads modern UPS must handle including some typical examples.

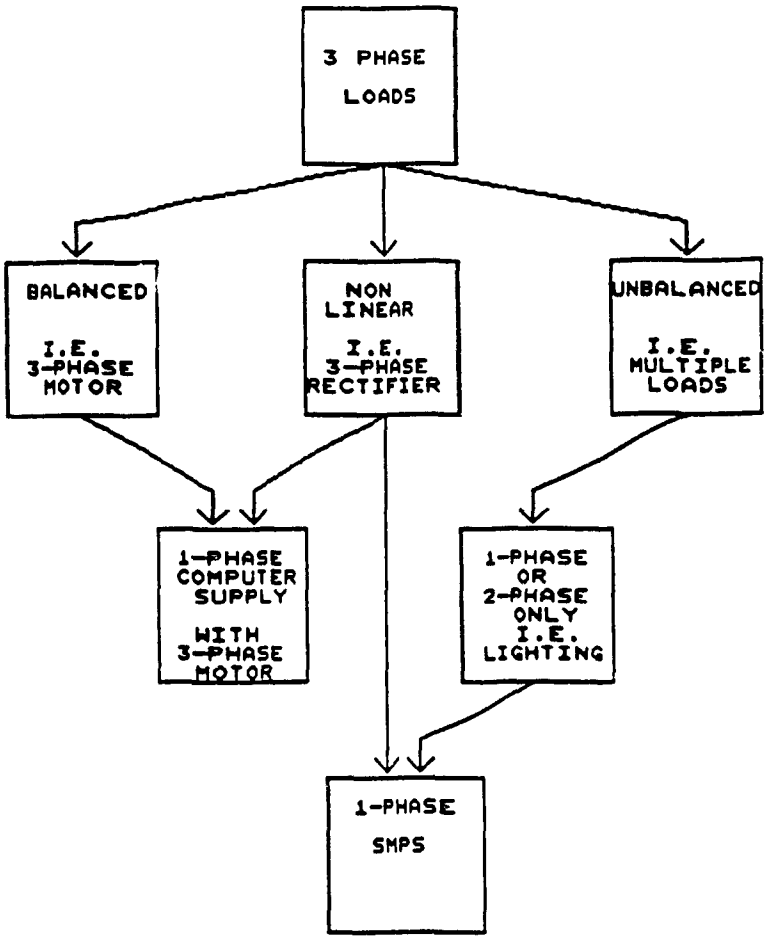


Figure F4.1 3-ϕ load tree with examples

To illustrate the effects adverse load conditions create on the typical inverter, a modern medium power transistor UPS inverter stage is employed as a benchmark and shown in figure F4.2. Assuming the transformer is well designed (i.e. negligible leakage inductance), all impedances may be transferred to the primary as shown in figure F4.3 to simplify analysis. It is also assumed that Sine PWM [24] is employed with a 21 pu carrier frequency creating a switching frequency of 1260 Hz/switch for a North American UPS. The filter break frequency is such that the dominant harmonic is reduced to below 2% under balanced load resistive conditions using the equation

$$W_N = \text{ORDER} \cdot \left[\frac{.02 \cdot HAR_{FUND}}{HAR_{DOM}} \right]^{1/Fo} \qquad (4.1)$$

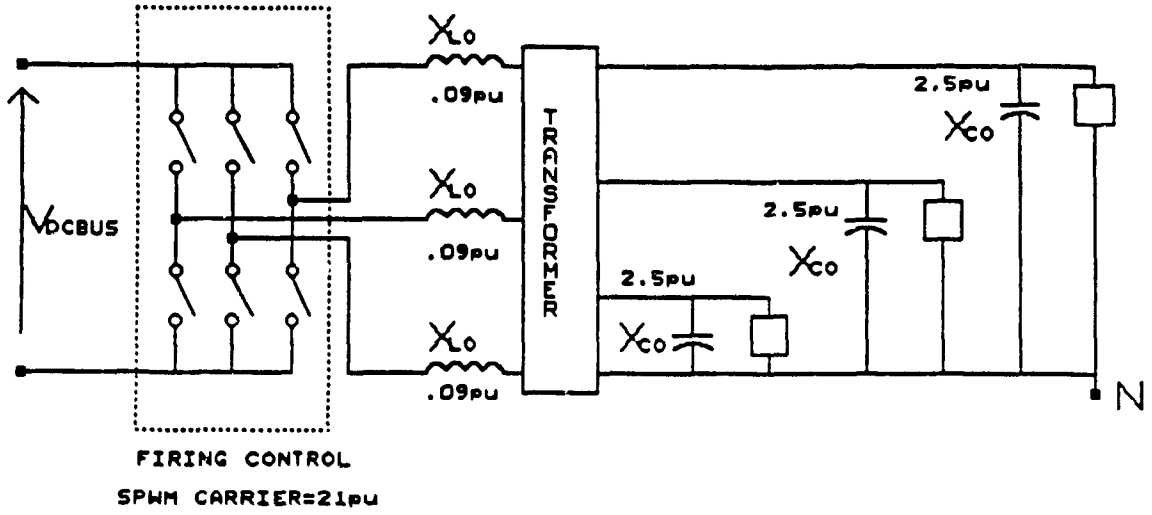


Figure F4.2 Typical UPS inverter configuration

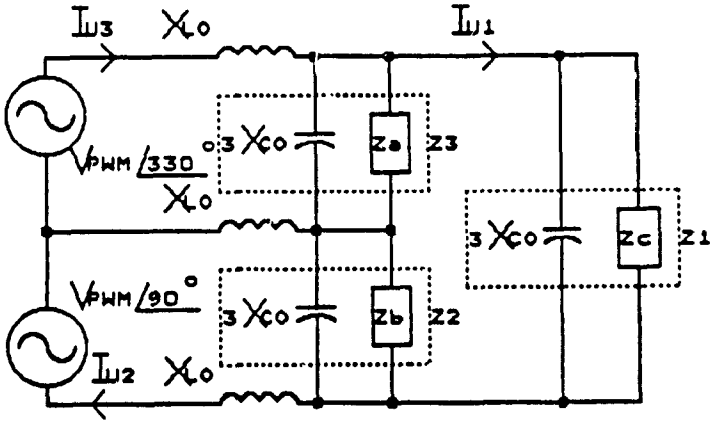


Figure F4.3 Simplifier inverter circuit

With X_{LO} =.09 pu and Xco =2.5pu, THD can be kept below 5% while supplying power to a balanced load at power factors from .7 lagging to .7 leading as given by the specifications table T2.1.

4.1.1 Unbalanced Load Application

The unbalanced application under consideration consists of an industrial complex where a single medium power UPS supports a 3-ϕ basement production line motor as well as office equipment and building lighting [59]. While combining 1-ϕ and 3-ϕ loads, it is not uncommon for the UPS to see different leg impedances and power factors. This creates different magnitude drops and phase shifts across each filter resulting in a large line-to-line voltage unbalance. Because of the detrimental effects this creates on particular loads, (NEMA) has set standard limits of unbalance for certain applications to below 1%-5% [20], using line-to-line voltages to reflect unequal phase displacement

$$\%\text{Unbalance} = \frac{\text{Max deviation from average voltage}}{\text{Average Voltage}} \tag{4.2}$$

By standard mesh analysis and a assuming purely sinusoidal supply, the following matrix can be derived from the UPS filter load stage of figure F4.3.

$$\begin{bmatrix} Z_1 + Z_2 + Z_3 & -Z_2 & -Z_3 \\ -Z_2 & Z_2 + 2jX_{LO} & -jX_{LO} \\ -Z_3 & -jX_{LO} & Z_3 + 2jX_{LO} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 \\ V_{PWM} \angle 90^\circ \\ V_{PWM} \angle 330^\circ \end{bmatrix} \tag{4.3}$$

Figure F4.4 shows the resulting voltage unbalance as a function of the load impedances and indicates potentially damaging results for a typical motor connected to the terminals including 75% insulation life reduction and 50% increase in losses. Further, for typical office computer apparatus tied on the same line survival is ensured for input voltages which are not 6% in excess of nominal [8]. From the curves, we can see this boundary is violated on occasion

possibly leading to equipment malfunction.

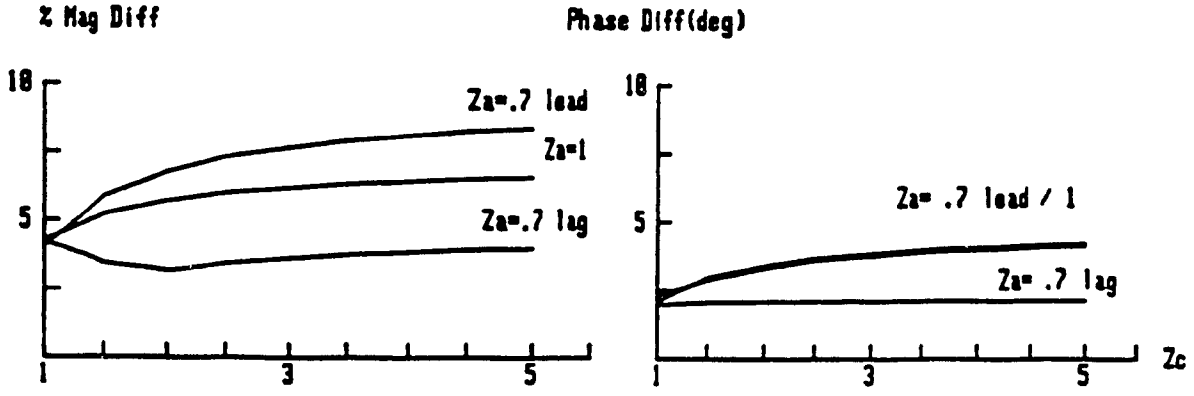


Figure F4.4 Resulting NEMA %voltage and phase unbalance (Z_b=.7 pu lag)

$$\%\text{unbalance} = \frac{\text{maximum deviation from the average voltage}}{\text{average voltage}}$$

A second common UPS adverse operation condition occurs during periods where portions of its three phase load are not in use leaving only one or two phases delivering power to the load. Figure F4.5 was constructed showing the resulting magnitude of the second harmonic DC link current under 1-ϕ operation of a 3-ϕ UPS. The amplitude of the harmonic is solved using equation 4.3 to find line currents and then utilizing the switching function concept (outlined in chapter 3.1) to generate the input spectrum (inverter switching harmonics are neglected). The input filter must now be designed to attenuate a second harmonic of significant amplitude (in contrast to standard sixth) or face the possibility of inverter input voltage distortion.

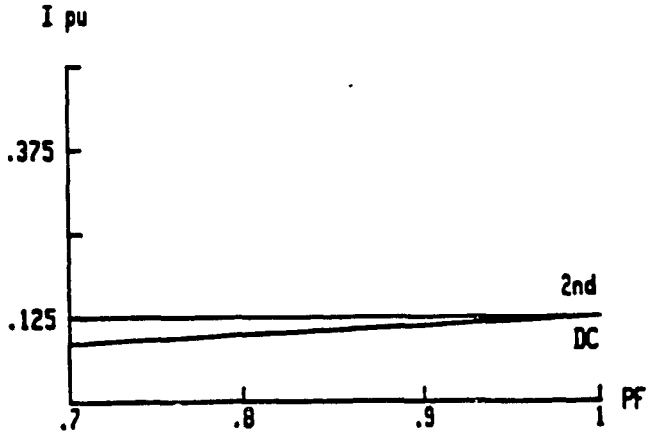


Figure F4.5 DC link current during 1-ϕ operation of 3-ϕ UPS.

4.1.2 Nonlinear Load Application

Since most of the load induced nonlinear distortion is independent of the inverter output harmonics, the inverter output voltage is assumed to consist only of it's fundamental component. The impedance of the output LC-filter as seen by a current drawn from the inverter by the nonlinear load is given by

$$Z_{FILTER} = \frac{X_{LO} \cdot X_{CO}}{j(NX_{LO} - X_{CO}/N)} \qquad (4.4)$$

Figure F4.6 shows the filter impedance for various harmonics demanded by the nonlinear load and shows where its pole lies. This pole, or infinite impedance point, exists for any second order filter and indicates that any harmonic current demanded by the nonlinear load in the vicinity of the pole will be reflected as a substantial voltage harmonic superimposed on the fundamental. By applying Fourier series analysis, Table T4.1 shows the per unit harmonic currents present on the input lines of a typical 6-pulse power converter.

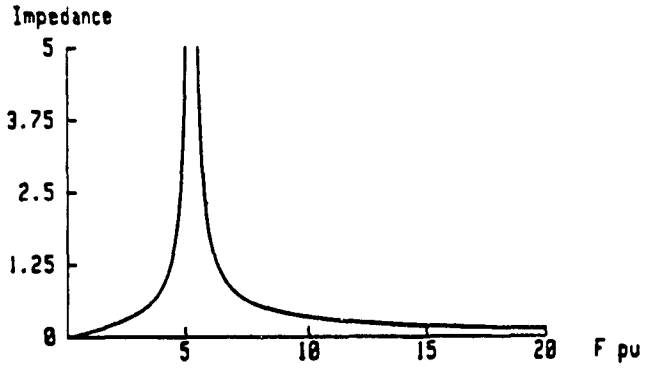


Figure F4.6 Typical LC filter impedance

N	Current pu
5th	.175
7th	.110
11th	.045
13th	.029
17th	.015
21th	.010
23rd	.009

Table T4.1 Per unit rectifier current harmonics

In reality these values are smaller than the ones corresponding to the standard square wave because of the effects of various line inductances [57]. Attempting to supply power to such a nonlinear load using the typical benchmark inverter results in an output voltage THD of greater than 50%. Shifting of the pole slightly would not seriously affect the THD level. A major pole shift to a higher frequency would seriously hamper THD requirements whereas a major shift to a lower frequency not only increases filter size, but would seriously increase voltage unbalance during unbalanced load conditions.

A second type of common nonlinear UPS loads found in a modern office complex are 1-ϕ SMPS incorporated in most data processing machines. Since SMPS typically demand a large third harmonic, serious waveform distortion may occur

because typical 3-ϕ inverters are not generally designed to accommodate such large harmonic demands. The THD for nonlinear applications requiring a 50% third or fifth harmonic can become substantially large as shown in figure F4.7. This type of distortion is clearly unacceptable.

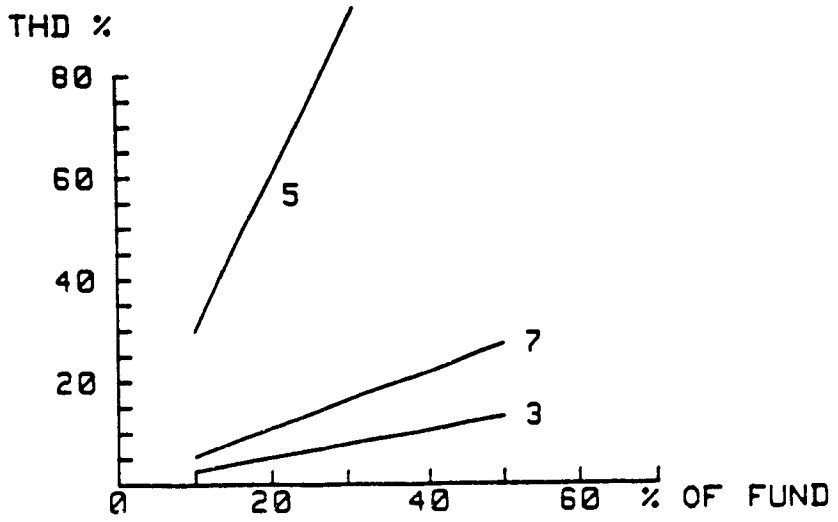


Figure F4.7 THD under nonlinear load with various harmonics

4.2 Existing Alternatives

Because the placement of the pole during filter design is a direct function of the inverter switching frequency, an apparent solution to the problem of unbalanced/nonlinear loads would be to decrease the filter impedance by increasing the switching frequency. Low power 1-ϕ inverters having the capability of high switching frequency generally place the pole at a high frequency. Consequently, these supplies are compatible with many standard nonlinear loads. In contrast, this solution is unacceptable beyond certain output power levels since switching losses and stresses must be kept low thereby imposing a maximum switching frequency constraint.

4.2.1 Combining 1-ϕ Inverters

A typical solution to the unbalance problem without increasing switching frequency is to utilize three separate 1-ϕ bridges independently controlled and combined into a 3-ϕ output via a complex transformer arrangement. The method is shown in figure F4.8 and enables independent leg voltage and phase control, compensating for load unbalance. However, the scheme carries several disadvantages including:

1) Multiple voltage feed backs are required because of independent control rather than a single average value of all three phases.
2) Double the number of semiconductors, increasing switching losses, cost and decreasing reliability.
3) Inefficient utilization of magnetic transformer material.
4) Large DC link current harmonics.
5) Inability to handle nonlinear loads without addition measures.

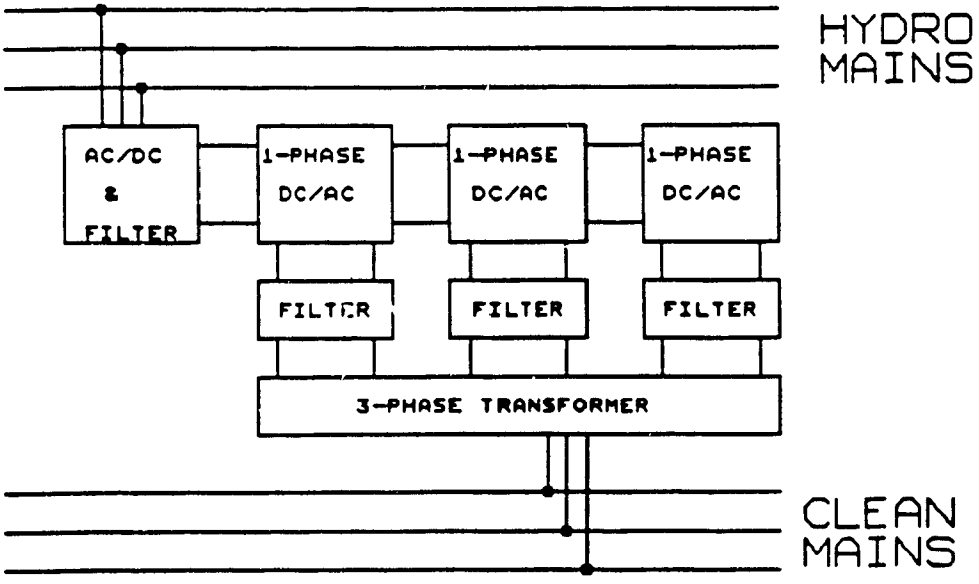


Figure F4.8 Unbalanced solution with three single phase bridges

4.2.2 Harmonic Traps

A widely used technique enabling the inverter to accommodate nonlinear loads is the employment of harmonic traps [52], [53]. These effectively provide a circulating path for harmonic currents demanded by the load. Figure F4.9 shows a typical example of a harmonic trap where

$$X_{LT} = \frac{X_{CT}}{N^2} \qquad (4.5)$$

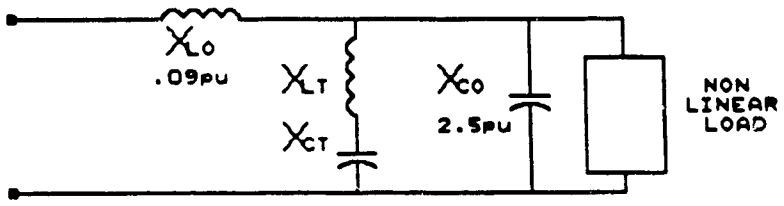


Figure F4.9 Single harmonic trap

Initial investigation of this equation suggests that low order harmonics would require large values of inductance or capacitance. However, this is slightly offset by a higher impedance to the fundamental current resulting in a drop of overall current ratings of the trap components (providing that the trapped harmonic current is relatively low in magnitude to begin with). Further, a strong advantage of this technique is that the traps can be added to the system in the field of operation, permitting customization of the inverter to nonlinear load demands. This advantage has prompted UPS manufacturers to produce special interfaces which can be employed to actually clean up nonlinear load induced distortion [58]. However, since the interface is not entirely universal an alternate interface may be required to offset unbalanced load distortions. This leads to added expense and space requirements as well as a non-universal solution to enabling UPS management of

the adverse loads. Further, more serious drawbacks exist including:

1) Filter traps at low frequencies and high currents are bulky and costly, especially so for the 75% 3rd harmonic present in many 1-ϕ computer supplies.

2) Numerous traps may be necessary for loads such as 3-ϕ diode rectifiers in which many harmonics must be supplied.

3) Each zero introduced by a trap also introduces a pole in the filter transfer characteristic increasing the chance of instability.

4) Tuning the traps can be difficult even with good component tolerances.

5) Traps are not effective and may be detrimental when dealing with unbalanced loads possibly forcing their continuous application and removal depending on load conditions.

4.2.3 Unbalanced Switching Function

Sophisticated inverter control is another area in which some success has been attained. The instantaneous feedback method [54], [55]. in which the control scheme forces the inverter output voltage to stay within a pre-defined window independent of load conditions, is a good example of such schemes. This bang-bang type of control often has a non-fixed inverter switching frequency which depends on load conditions complicating prediction of operating characteristics under adverse load conditions. Further, the technique is effective only for high frequency applications due to the rapid response requirements.

Finally, several control techniques have been proposed recently [59], [60] that are relatively effective for alleviating distortion caused by triac type nonlinear loads. However since the filter inductance impedance is

typically .09pu, operation under 3-ϕ unbalanced loads may not conform to minimum phase displacement requirements. Moreover, these schemes are generally geared for 1-ϕ operation and have not been thoroughly proven for 3-ϕ operation. The techniques generally focus on a contingency style of problem solution rather than a preventative style which would stop the problem at the source.

4.3 UPS System Modifications

The solution proposed focuses on the minimization of inverter output impedance. By substantially reducing the output filter size the inverter can be driven towards a low output impedance source permitting clean, balanced power delivery to unbalanced loads. Further, effective filter pole placement in combination with low filter impedance ensures the ability to keep relatively clean power under nonlinear load condition as well.

4.3.1 UPS Output Filter Derivation

As shown previously, the major portion of magnitude and phase alteration during unbalanced load conditions is primarily due to the filter reactor. To alleviate this problem the reactor impedance is reduced. Using equation 4.3 and figure F4.3, figure F4.10 was created showing the effects that varying X_{LO} has on the magnitude and phase of the unbalanced load supply. The input voltages are assumed to be purely sinusoidal and since the value of X_{CO} plays a relatively small role in this instance its value has been kept constant at the benchmark level of 2.5 pu.

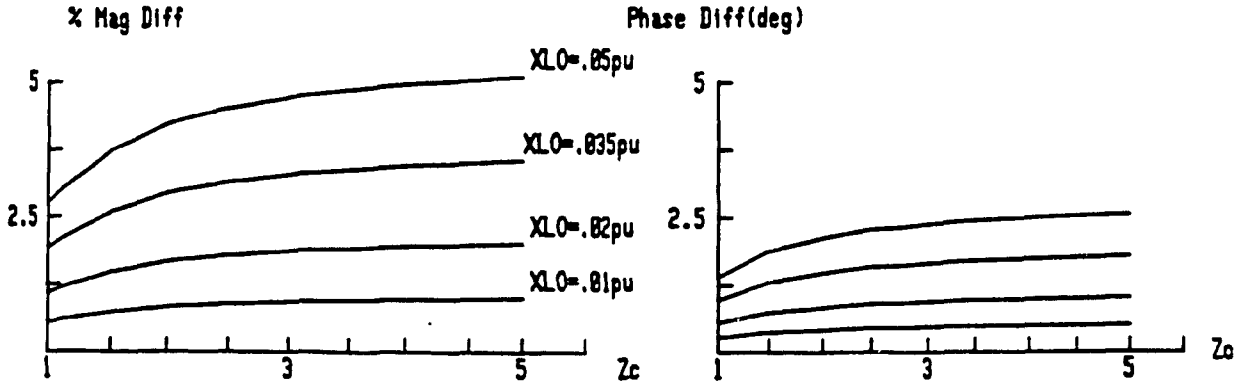


Figure F4.10 Unbalanced effect as X_{LO} is varied (Z_A=.7 lag, Z_B=.7 lead)

From the figure it can be seen that X_{LO} should be as low as .015 pu to virtually eliminate unbalance problems, remain within NEMA standards, and maintain computer apparatus requirements.

Adjustments of X_{LO} from .09 pu to .015 pu creates a new filter transfer function in which a pole (infinite impedance) exists at

$$\sqrt{\frac{X_{CO}}{X_{LO}}} = \sqrt{\frac{2.5}{.015}} = 12.9 \text{ pu frequency} \qquad (4.6)$$

This indicates that any voltage harmonic created from the inverter or current harmonic demanded by a particular load at 13 pu will cause severe distortion due to amplification. Since any LC filter will contain at least one pole, it is theoretically impossible to create a trouble free inverter-filter combination able to handle any conceivable type of load. However, by properly placing the pole, most realistic, presently available nonlinear loads may be tolerated. The known frequencies to avoid include:

1) All odd harmonics excluding triplens ensuring no large filter impedances for 3-ϕ balanced nonlinear loads (i.e.

1,5,7,11,13,17,19.....).

2) All odd harmonics below approximately 13 pu. 1-ϕ nonlinear loads whose current harmonics typically fall steeply in magnitude after the 7th (i.e. 1,3,5,7,9,11) would induce voltage harmonics at low frequencies.

Based on these factors, a pole frequency of approximately 15 pu is reasonable. A value of 15.3pu is chosen to guarantee that if a minuscule 15pu voltage or current harmonic exists from switching delays or load conditions, its amplification will not be infinite. Xco can therefore be derived as

$$X_{CO} = X_{LO} \cdot (\text{pole frequency})^2 = 3.5 \text{ pu} \qquad (4.7)$$

4.3.2 Special PWM

Shifting of the filter break frequency to 15.3 pu from the benchmark frequency of 5.27 must be accompanied by a substantial rise in switching frequency to adhere to the THD requirements. If SPWM were used, the switching frequency would dictate an increase from 21 pu to 57 pu or 170%. This may become too large for medium power inverters. Consequently, a more advanced PWM scheme must be used.

An approach at higher powers is to use an optimized fixed-pattern inverter firing scheme in conjunction with the regulated front-end stage to vary the DC link voltage. The PWM scheme employed is a derivative of the harmonic injection technique [27] where a triangular carrier is compared with a reference containing fundamental and third components. The third allows for overmodulation and better harmonic content. On the other hand, the third harmonic component virtually disappears in the 3-ϕ system (Figure F4.11A). This scheme, as most other PWM schemes, typically has its dominant harmonic

present at the carrier frequency (Figure F4.11C). The modification utilized here is to increase the carrier frequency to 57 pu and eliminate any comparison of the triangle with the reference in between 33° and 147° (Figure F4.11D). This reduces the switching frequency to approximately 2/5 of the carrier frequency while leaving the dominant harmonic at the carrier frequency as shown in figure F4.11F. Numerically, the inverter switching frequency is kept at 23pu while the dominant harmonic has shifted to 57 pu thus allowing for the needed reduction in output filter size and consequently impedance.

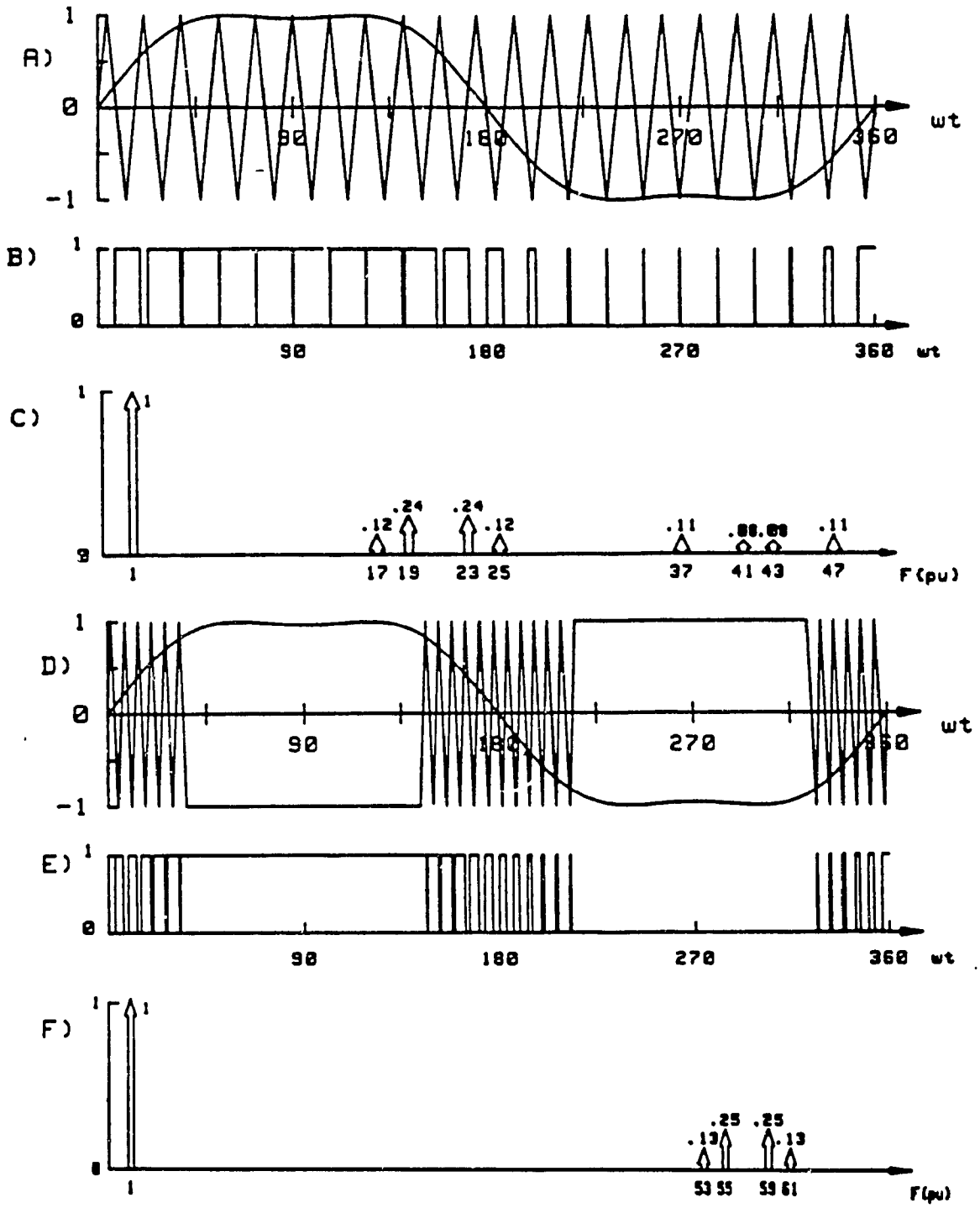


Figure 4.11 Advanced Harmonic Injection PWM

A) Typical utilization
B) Switch #1 gating of (A) (21 pu switching frequency)
C) Spectrum of (A)
D) Altered version of (A)
E) Switch #1 gating of (D) (23 pu switching frequency)
F) Spectrum of (D)

The proposed circuit topology is shown in figure F4.12A and is compatible with the UPS topology proposed in chapter 2.3.1.

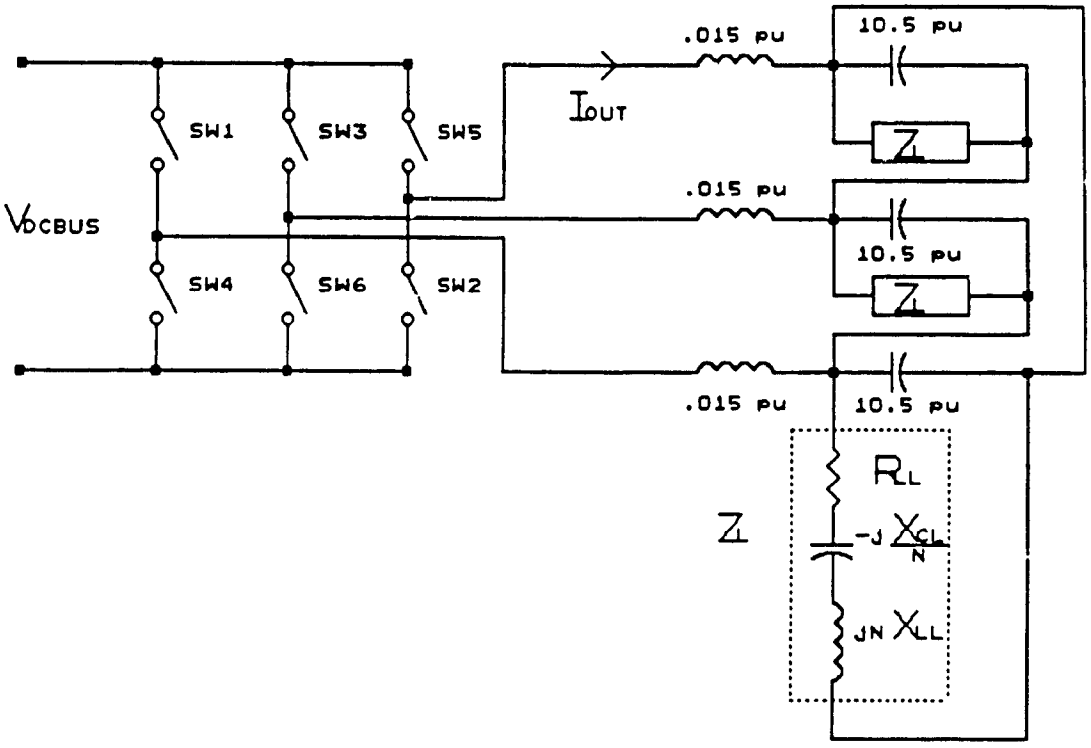


Figure F4.12A Proposed UPS inverter topology

The attribute of this topology is its ability to maintain clean quality power for any delta connected 3-ϕ load, linear or nonlinear. Although this may blanket 90% of the typical applications, if a neutral lead is required for line to neutral loads the topology may not appropriately solve unbalanced conditions. For these extreme cases the topology of figure F4.12B may be used.

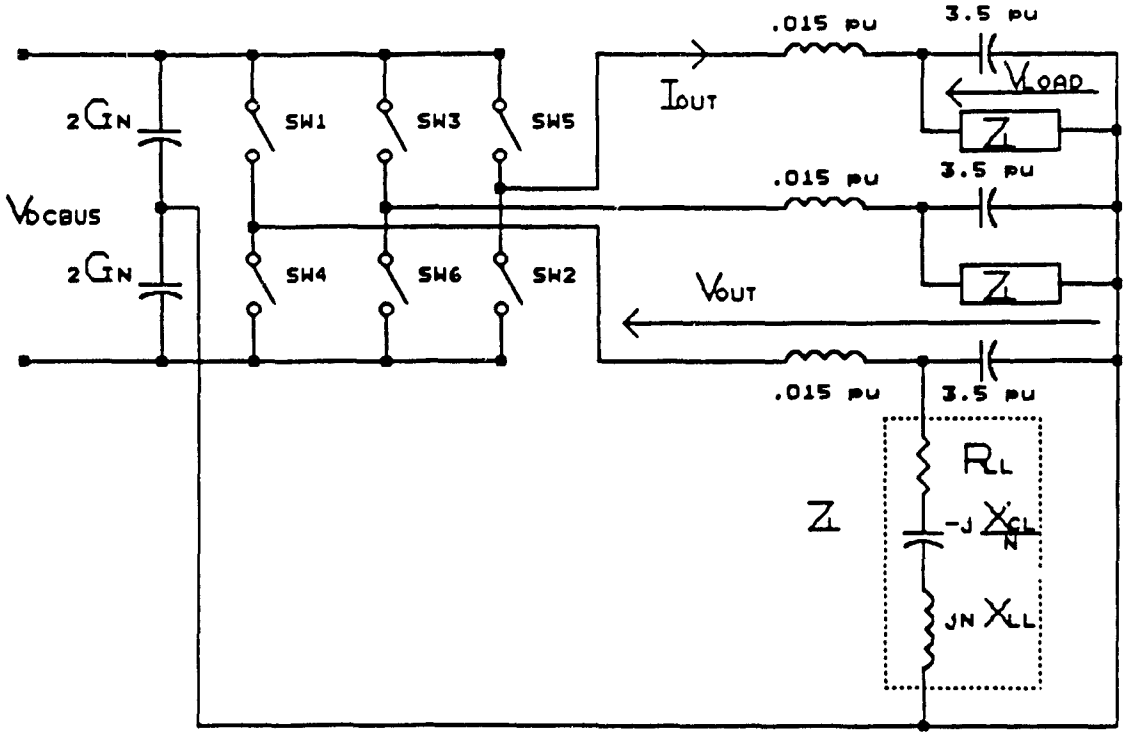


Figure F4.12B UPS inverter topology proposed for special case 1-ϕ line to neutral loads.

The main differences with this topology are:

1) The input filter capacitor is now split to present a stiff neutral to the output 3-ϕ lines.

2) Since the advanced PWM scheme employed uses a 3rd harmonic component in its reference waveform the line to neutral output voltage will contain this harmonic which flows freely with the closed neutral connection. An alternate advanced PWM scheme must be employed. SHE with its dominant harmonic at roughly 57 pu and suppression of triplens would require a switching frequency of 28 pu. This is generally acceptable in medium power inverters and limits the switching frequency increase over our bench mark inverter to 33%.

4.4 Topology Performance

Since results for the proposed topologies are expected to differ only in switching losses and input capacitor filter division the former topology (Figure F4.12A) will be used for experimental evaluation due to its relatively simpler form.

4.4.1 Predicted Topoiogy Performance

4.4.1.1 Balanced Linear Load

For a balanced resistive load of 1pu/phase load voltage harmonics and THD are given by

$$V_{LOAD_N} = \frac{V_{OUT_N}}{\left[\left[1 - \frac{N^2 X_{LO}}{X_{CO}}\right]^2 + \left[\frac{N X_{LO}}{R_L}\right]^2\right]^{.5}} \qquad (4.8)$$

where V_{OUT_N} and V_{LOAD_N} are respective line to neutral variables

$$\%THD = \frac{100}{V_{LOAD_1}}\sqrt{\sum_{N=3,5..}^{\infty}\left[V_{LOAD_N}\right]^2} \qquad (4.9)$$

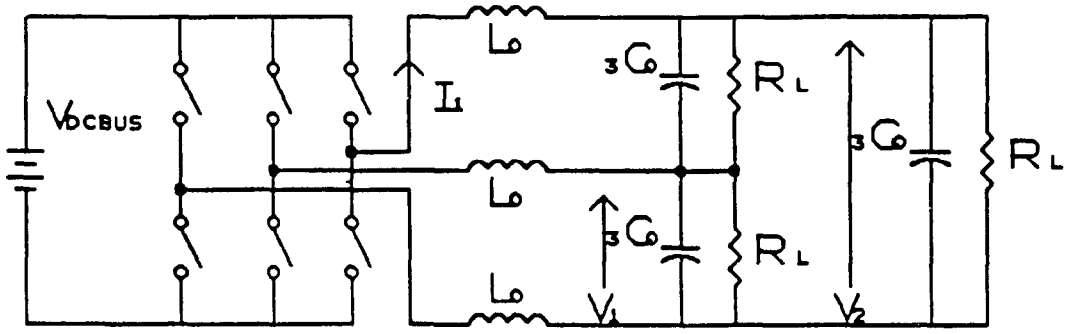
where R_L = load resistor/phase =1pu

X_{LO} = filter reactance =.015pu

X_{CO} = filter capacitance =3.5pu

Totaling these harmonics reveals an expected THD of 4.8%. To further display the schemes performance under balanced load conditions the inverter circuit of figure F4.13A was simulated using ASPEC under balanced resistive load

conditions. Full input PWM voltage was applied and all components were transferred to the primary thus simplifying the analysis. The resulting steady state line-to-line voltage and line current are shown in figure F4.13B.



LOAD CONDITIONS	
Z	=1PU

SPECIFICATIONS	
V_{DCBUS}	=2.449V
L_o	=40uH
$3C_o$	=252uF
R_L	=3R

Figure F4.13A Simulation test circuit

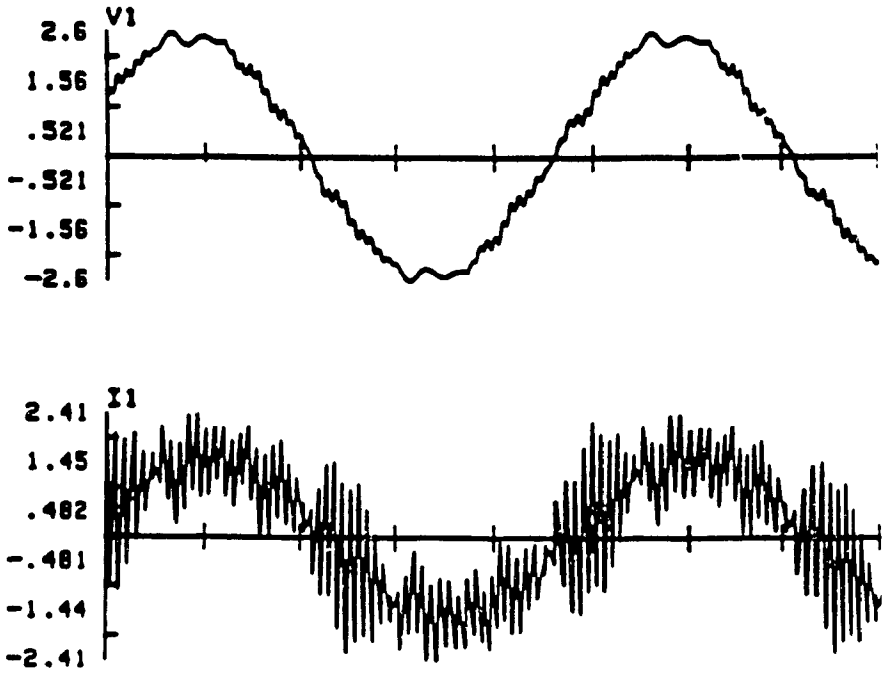


Figure F4.13B Simulated waveforms under balanced load conditions

Observation of the simulated results reveals that:

1) The voltage has an acceptable THD.

2) The peak line current or switch current is roughly 2.4 pu which is an increase over the benchmark inverter by 14%. From a switch ratings point of view this is not a critical drawback since semiconductors can easily maintain peak currents higher than average current ratings.

3) Because of the low line inductance, interrupt shutdown loops must be reasonably fast. Since load shorts must pass through two reactors the rate of rise of current will be

$$\frac{\sqrt{3}}{(.03/2\pi 60)} = \frac{\Delta I}{\Delta t} = .022 \text{ pu}/\mu s \qquad (4.10)$$

Since good control shutdown loops can react and turn off transistor

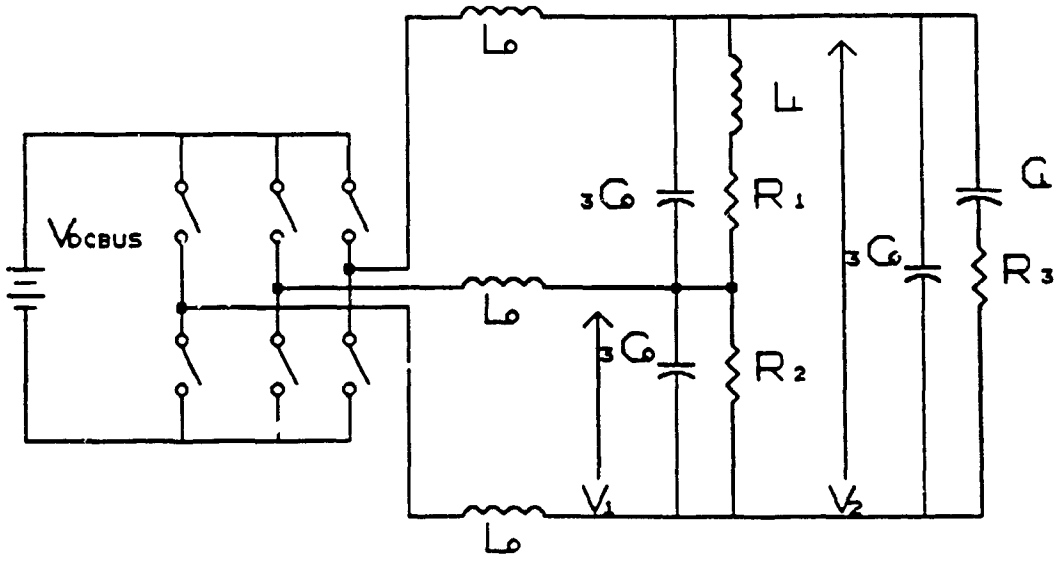
switches within 10μs the switch current will be shut down before a rise of .2pu. Moreover, sophisticated base drives are available with self-protection features [61] enabling fast shutdown virtually independent of the series inductance.

4.4.1.2 Unbalanced Load Test

To seriously test the scheme's ability to handle unbalanced loads the circuit of figure F14A, loaded with individual leg power factors of 1, .7 lagging and .7 leading has been simulated. Figure F14B shows two of the three resulting line-to-line voltages. After spectra examination the results of table T4.2 were tabulated.

LEG	Vrms	PHASE
1	1.73	0°
2	1.74	119.6°
3	1.75	240°

Table T4.2 Unbalanced output voltages



LOAD CONDITIONS
Z_A=.7 LAG
Z_B=1
Z_C=.7LEAD

SPECIFICATIONS	
V_{DCBUS}	=2.449V
L_o	=40uH
$3C_o$	=252uF
F	=5.68mH
C	=1238uF
R_1	=2.1R
R_2	=3R
R_3	=2.1R

Figure F4.14A Unbalanced simulation test circuit

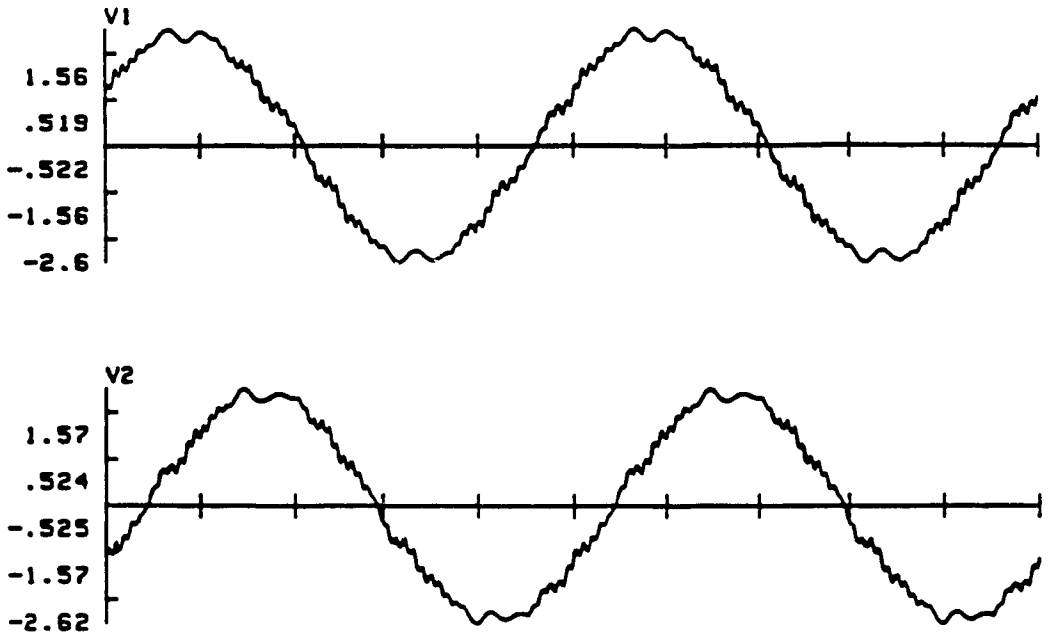


Figure F4.14B Simulated waveforms under unbalanced load conditions

4.4.1.3 Nonlinear Load Application

The equivalent model for load induced current harmonics is shown in figure F4.15. Since the load is balanced an equivalent 1-ϕ model can be obtained and the harmonics solved from

$$\%V_{LOADLL_N} = I_{LOAD_N}\left[\frac{X_{CO}\cdot X_{LO}}{j(nX_{LO} - X_{CO}/n)}\right] X\ 100 \qquad (4.11)$$

The table of expected voltage harmonics generated solely from a 3-ϕ nonlinear load are listed in table T4.3.

N	I_{LOAD_N}	V_{LOADLL_N}
5	.175	1.47%
7	.110	1.46%
11	.045	1.54%
13	.029	2.05%
17	.015	1.60%
19	0	0.00%
23	.009	0.25%

Table T4.3 Expected voltage harmonics

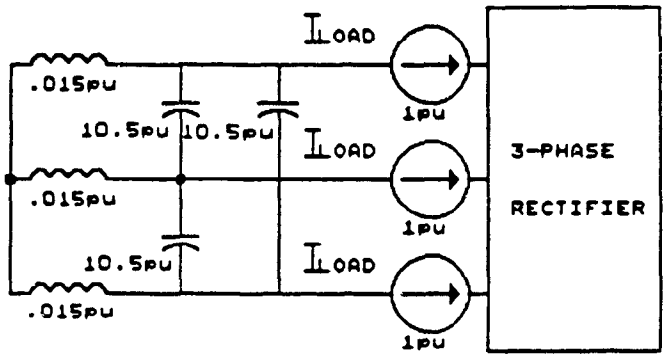


Figure F4.15 Equivalent circuit of load induced harmonics

4.4.1.4 1-ϕ Nonlinear Load

1-ϕ nonlinear loads may draw numerous low order harmonics at various amplitudes. It is not abnormal to expect a 75% 3rd harmonic current demand along with 5th and 7th harmonics. The equivalent circuit for a 1-ϕ 100% rectifier load under test is shown in figure F4.16 and the expression solving the predicted voltage harmonics is given by equation 4.11 with a multiplying factor of 2/3 accounting for parallel filter components. Figure F4.17 shows, using equation 4.11, the expected rise in THD of each low order harmonic as a function of amplitude.

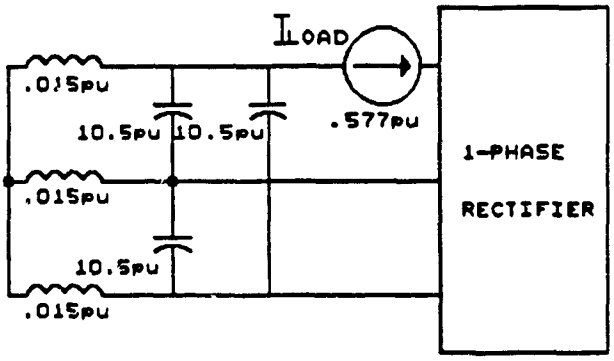


Figure F4.16 Equivalent circuit of single phase load induced harmonics

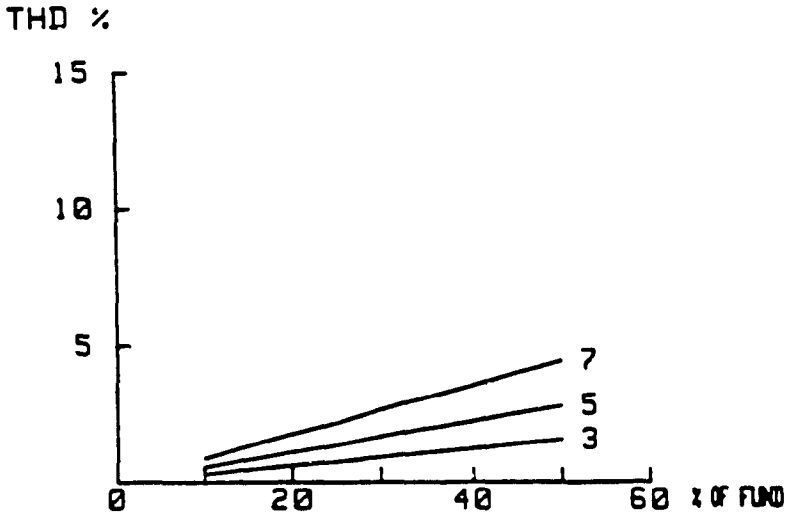


Figure F4.17 THD under adverse load condition

Consequently theoretical results dictate that voltage distortion would be kept at a minimum despite the application of many unbalanced and/or nonlinear loads presently existing.

4.4.2 Experimental Results

To verify the effectiveness of the proposed topology design experimentally, a 3 kVA laboratory MOSFET inverter stage was utilized and subjected to the various loads at full rated operating conditions. The load free circuit contains the components shown in table T4.4.

V_{LOADLL_1}	1.73pu	$150V_{rms}$
I_{LOAD_1}	1.00pu	$10.33A_{rms}$
Z_L	1.00pu	8.42 Ω
P_{OUT}	3.00pu	2.7 Kw
X_{LO}	.015pu	330 μH
X_{CO}	10.5pu	30.0 μF
F_{BASE}	1.00pu	60.0 Hz

Table T4.4 Experimental component values

The schematic of figure F4.13A was implemented using these base values and a balanced resistive load. Figure F4.18A, and F4.18B shows the line-to-line voltage and line current respectively under these conditions. Figure F4.18C shows the resulting voltage spectrum.

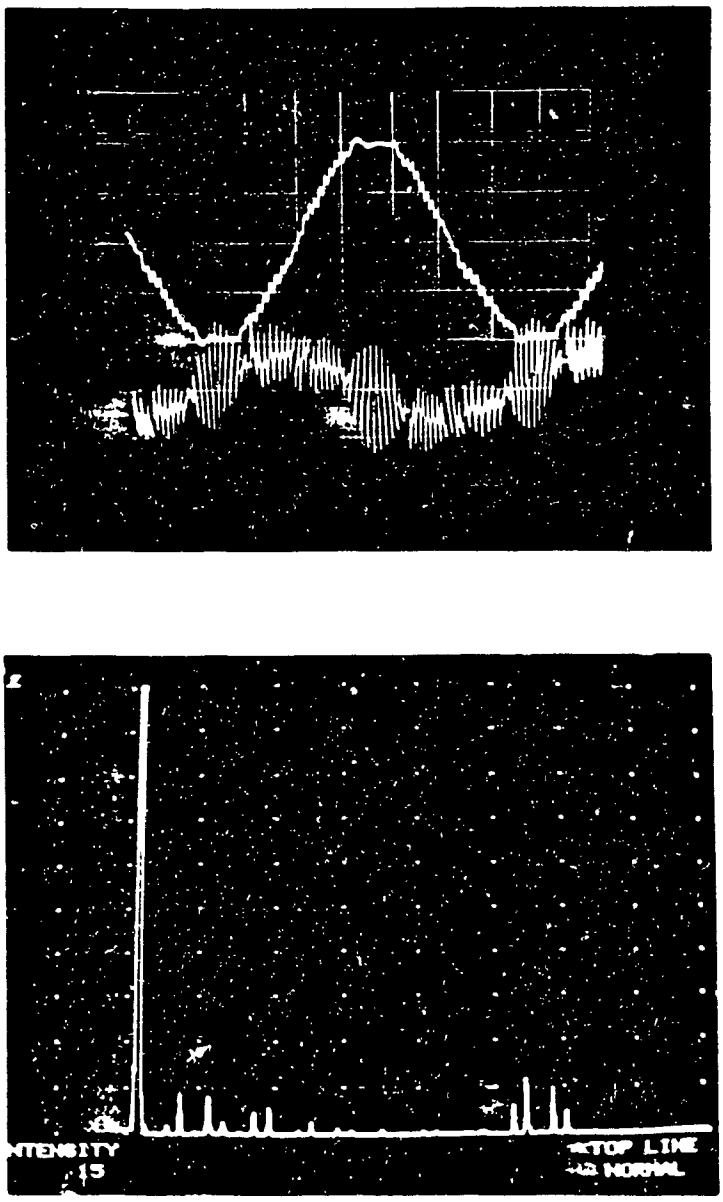


Figure F4.18 Waveforms under balanced load conditions
Power Factor = 1, R = 8.42 Ω (L-N)/phase
A) Line to line voltage 100V/div
B) Line current 20A/div
C) Spectrum of (A) 2%/div 614Hz/div. Dominant is at 5Spu freq.

Comparison with simulated predicted results reveals insignificant differences. The THD measured was 4.4% which is within most industrial standards.

To test under unbalanced load conditions the schematic of figure F4.14A

was implemented. Figure F4.19 shows the three line-to-line voltages and their associated spectra. By observation, all spectra have similar THD levels and are below the required 5% and have a maximum harmonic amplitude of 2.7%. Further measured line to line load voltage results are shown in table T4.5.

Voltage of Z_A	$= 151\angle 0^\circ$ Vrms
Voltage of Z_B	$= 152\angle 118^\circ$ Vrms
Voltage of Z_C	$= 152.1\angle 240.5^\circ$ Vrms

Table T4.5 Unbalanced load line to line voltages

These waveforms compare favorably with the simulated results shown in Figure F4.14 and theoretical data of Table T4.2. The results show virtually balanced voltages which conform with NEMA specifications and computer apparatus requirements.

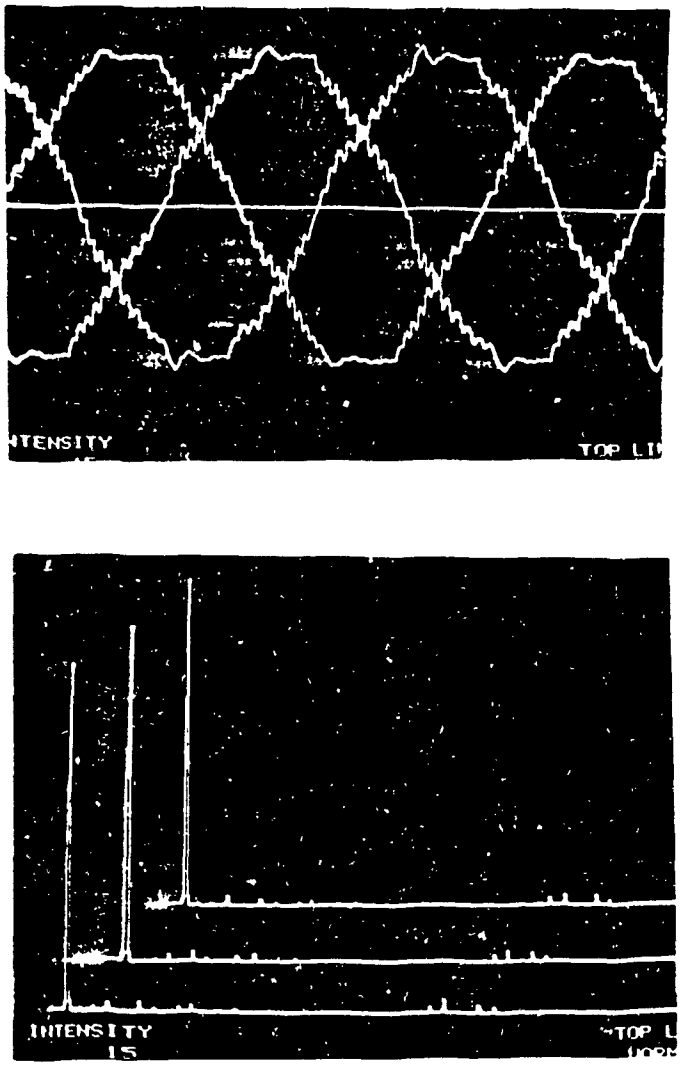


Figure F4.19 Waveforms under unbalanced load conditions
Leg 1-> PF=.7 lag R=17.67 L=48uH
Leg 2-> PF=.7 lead R=17.67 C=147uF
Leg 3-> PF=1 R=25.26
A) Three line to line voltages
B) Spectra of (A). Maximum harmonic = 2.7%

Waveform results under full current 3-ϕ nonlinear rectifier load applications are shown in figure F4.20. In particular, figure F4.20A shows the resulting line-to-line voltage waveform while figure F4.20C shows it's associated spectrum. Figure F4.20B shows the harmonic demand of the load or

output line current spectrum. The harmonics are slightly larger than expected because of the greater than expected load current harmonics (low smoothing reactance) and the addition of the small low order inverter injected harmonics. This resulted in an experimental THD to 5.8% which is still an improvement over typical mains distortion observed if a 100%, 3-ϕ nonlinear load is applied.

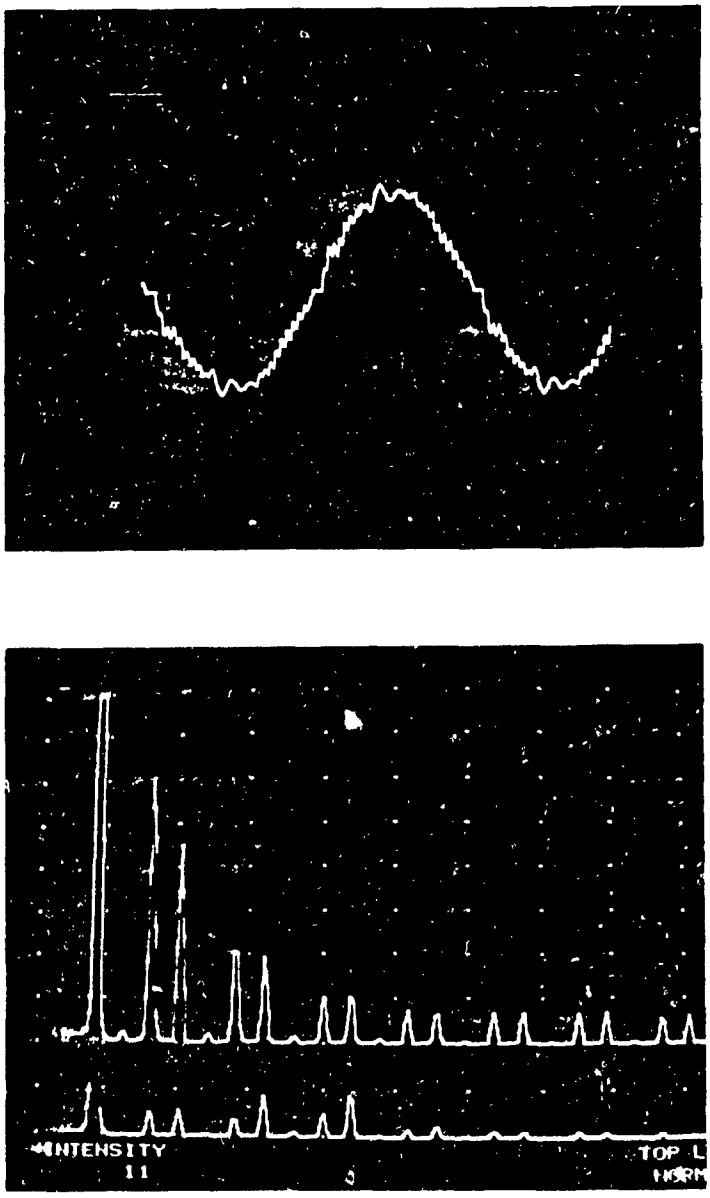


Figure F4.20 Waveforms under 3-ϕ nonlinear load conditions
Line current = 10.28 A V_{LOADLL} = 150 V
A) Line to line Voltage 100V/div
B) Spectrum of line current 3%/div
C) Spectrum of line to line voltage 3%/div

The experimental results for a 1-ϕ rectifier type load are shown in figure F4.21A-D. The inverter is delivering a peak to rms current ratio of 2.5 at 100% 1-ϕ rated conditions. In particular figure F4.21A shows the output

line-to-line voltage while its spectrum is shown in figure F4.21D. The current demanded by the load is shown in figure F4.21B with its associated spectrum in figure F4.21C. The low distortion (THD=5.2%) shows that the proposed low impedance 3-ϕ filter can supply 1-ϕ computer type loads without a drastic reduction in voltage waveform quality.

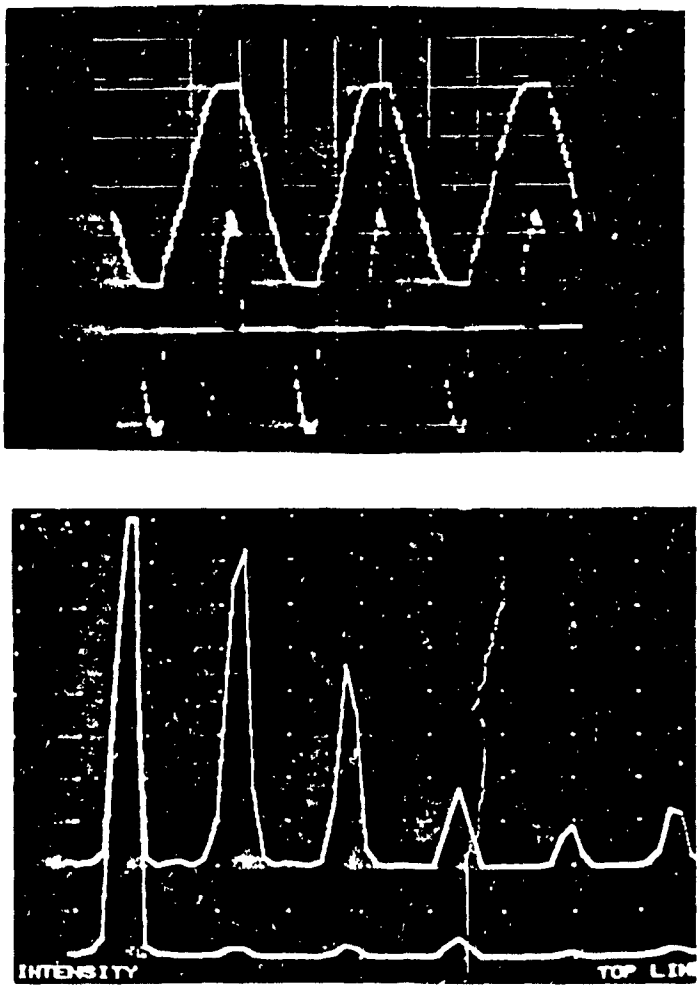


Figure F4.21 Waveforms under 1-ϕ nonlinear load conditions
Line current = 5.9 A V_{LOAD} = 150 V

A) Line to line voltage 100V/div
B) Line current delivered to load 5A/div
C) Spectrum of line current 10%/div
D) Spectrum of line to line voltage 10%/div

4.5 Conclusion

A large number of modern loads requiring clean uninterrupted power are nonlinear and/or unbalanced. Consequently modern 3-ϕ UPS should be designed to power such loads without serious compromise and without added interfacing. Results show that typical PWM 4th generation UPS cannot meet these requirements. This has forced many UPS manufacturers into contingency type corrective measures to minimize the effects of the problem.

The solution presented in this chapter focused on preventive type corrective action that substantially reduces the problem at its source. The adaptive measures outlined allowing the UPS design to meet harsher, modern loads using a selected PWM technique and special output filter selection. Based on theoretical and extensive experimental results the low output impedance 3-ϕ UPS presented in this chapter performs well under unbalanced as well as nonlinear load applications.

5.0 CONCLUSIONS SUMMARY

The last decade has seen the emergence of a rapid expansion of medium power UPS applications. The main factors leading to the growth stem from two sources; the reliability of electric utility energy and the increasing number of complex loads which are dependent on the reliability of ac power.

Many ac power generating institutions are operating at or approaching full capacity. Further, future customer demands of power are expected to substantially increase. Continuous operation at full level rather than a fraction of full tends to decrease reliability. Utility expansion difficulties arising as a result of environmental concerns and future use of nuclear reactors tend to slow down power upgrading required for consumers. Moreover, by the year 2000, 50% of ac mains loads are expected to be nonlinear. The unwanted harmonics, heavy neutral line currents and associated anomalies introduced by nonlinear loads is expected to further reduce ac line reliability. To magnify the problem, the increasing customer dependence on electric energy is increasing the cost of associated power failures. This is reflected in studies which show a heavy cost to the average Canadian institution when a power failure is encountered.

Two substantial increases in UPS applications have come from newly developed high technology equipment and optimized manufacturing processes. Modern equipment containing microprocessor hardware have branched out to every area of business. The cost of corrupt or lost data to an institution relying on the equipment is often intolerable. Similarly, in the production facilities of many businesses, streamlined manufacturing costs has resulted in highly optimized processes sensitive to ac power availability. The resetting of

machinery and /or rebooting of software can be time consuming and costly.

The increasing spectrum of applications has tested the suitability of current, traditional, medium power UPS. The typical *"4th Generation UPS"* cannot meet the decreasing size and weight requirements in a number of downtown locations. The UPS occupies costly excessive floor space and often cannot be supported by office complexes built without concrete floors. The UPS cannot maintain output terminal specifications when supplying power to the two most common nonlinear loads. Further, unbalanced loading creates unbalanced output voltages which may exceed acceptable tolerances for motors and computers.

The proposed UPS affectively alleviate these problems. A substantial size reduction was obtained enabling costly floor space to be reduced. Significant weight reductions were also achieved allowing not only general floor loading applications but providing the first step towards the envisioned wall mounted medium power UPS. The proposed UPS allows full single and three phase diode bridge nonlinear loading capabilities. Further, fully unbalanced loads spanning the load power factor spectrum including open phases have been compensated for to prevent intolerable unbalanced voltages. Moreover, the proposed UPS design permits output load power factor from .7 leading to .7 lagging. In order not to overburden the ac distribution panel the proposed UPS maintains input power factor above .9 even as low as 50% loading. This feature is in anticipation of typical over rating of the UPS (64% loading). Recognizing the increased awareness for system ruggedness, (transients outside specification tolerances) a new, fully digital controller is used for the controlled rectifier stage. Finally, to enhance future design and analysis, two software routines were created. First, the extensive UPS design equations are combined methodically to form a worst case ratings program which promptly

returns component ratings and stresses. Secondly, the need for extensive simulation of PWM based power converters lead to the fabrication of a simulation program specially tailored to power electronic circuits.

To address UPS size and weight a new topology was presented. After harmonic analysis a fully controlled, MOSFET, PWM rectifier/battery charger stage was proposed. In order to obtain maximum benefits from the rectifier, a number of high performance PWM techniques both carrier and programmed were evaluated and compared. The evaluation criteria included many figures of merit such as; output spectrum quality, input spectrum quality, input capacitor ripple current, bridge gain, and implementation difficulties. The PWM scheme that proved most compatible for the charger was the MSPWM technique. The PWM technique allows the minimization of input and output filter components. Worst case component ratings for the rectifier were evaluated using derived design equations. The extensive equations are formulated with methodology compatible to computer processing using optimization routines. The derivations, based on harmonic analysis yielded required switch ratings and filter values. The input power factor of greater than 90% at 50% loading under the worst case line and battery conditions for the prescribed PWM was used to solve the input filter components. The validity of the equations and PWM effectiveness were checked with a simulation program for various rectifier conditions.

The largest weight and size reductions are obtained via the proposed HF link stage. This intermediate stage successfully eliminated the bulky output low frequency transformer, replacing it with a 2 kg high frequency version. Since the application of a HF link stage in UPS is relatively new several promising topologies were evaluated yielding the most suitable for implementation with modern components. A per unit component value and stress table revealed the full bridge operating at super sonic frequencies to be the

most suitable. Rather than simulation to verify design equations, full experimental data from a 10kW laboratory prototype complete with current mode control were obtained. Results show complete agreement.

Further size and weight gains were obtained with the proposed, transformer free inverter stage. By once again comparing selected carrier and programmed PWM techniques as in the controlled rectifier stage, the most compatible PWM technique was selected. Under balanced, linear load conditions with regulated input SHE provided the best quality terminal waveforms leading to the smallest possible filter. Based on the load power factor range of .7 leading to .7 lagging, extensive design equations were detailed. A worst case ratings program based on the formulated equations yielded all component values and stresses. As in the controlled rectifier evaluation, the inverter stage was simulated under various conditions to prove the generalized worst case ratings program results. Further to verify the design methodology and simulation results, an experimental 10kVA prototype inverter stage was implemented. The experimental results showed complete agreement with both the simulated results and the worst case ratings harmonic analysis results.

Harsh loading conditions such as nonlinear and unbalanced loads are alleviated by design strategies particular to the proposed UPS inverter stage. Evaluating several existing alternatives such as harmonic traps, revealed that only partial solutions could be obtained. The proposed solution commences by reducing the impedance of the output filter inductor. The inverter then approaches an ideal source with only minor unbalancing of the output voltages even under extremely unbalanced loading conditions. To compensate the substantial rise in THD when the filter reactor is reduced, a new PWM technique is introduced that effectively maintains the switching frequency low, yet spreads the deadband between the fundamental output and first family

of harmonics by 170%.

Delivery of power while maintaining output waveform specifications under nonlinear loads is achieved by strategic filter pole placement. By placing the pole at 15.3 pu the inverter delivers the low order, large amplitude current harmonics. The filter experiences little load induced harmonic voltages thus maintaining low load THD even under 100% nonlinear loads of three phase or single phase.

To confirm the new PWM technique and filter selection strategies, extensive simulation and experimental data were obtained. The results confirmed the design and derivations.

The large number of mathematical computations undergone to yield suitable components for any stage of the UPS, left a large exposure to error. To increase design speed and reliability, the design equations for the UPS inverter stage were combined in a software package. Based on PWM and output load power factor variation, worst case component ratings and stresses are evaluated rapidly and without error. After worst case ratings are solved, actual component values are solved based on user input data of processed power. Moreover operating point waveforms and component stresses are solved at a user selected load power factor. The program is not only a general design tool, but can be used as an analysis and evaluation tool for PWM techniques. The standardization of component ratings can effectively reduce first cut design time as well as increase reliability.

For power electronics circuits, simulation has always been a relatively tedious and time consuming process. So much so that for PWM inverters with a large number of pulses per period, simulation was often neglected. Moreover, commonly used simulation programs often require over night computation time which is not practical. With three individual, active power processing stages

in the proposed UPS a simulation program dedicated to power electronic circuits with PWM was developed to substantially reduce simulation time. The mathematic tool of computation is state space analysis. Further, capacitor loops and inductor cut sets which are common in three phase converter filters present no computational handicaps. The extensive use of the simulation routine provided an internal look at converter waveforms. Moreover, the program can be used not only as a first cut towards design, but as a teaching aid as well.

5.1 Further Work

Each stage of the UPS was designed relatively independently with separate filtering and control. It is however envisioned that with synchronized gating of the HF link and inverter stages, and a strategic PWM approach, the intermediate filtering stage may be substantially reduced or even eliminated. Further work could be done to investigate this concept.

By increasing rectifier complexity it is possible to merge the high frequency link with the rectifier stage. The result envisioned is a 3ϕ to 1ϕ high frequency cyclo conversion stage that when rectified would not only provide dc battery voltage but light weight, high frequency isolation as well. The inverter would also need modification since its input would no longer be regulated. The result would reduce the two stage losses to single stage losses during ac failure ultimately reducing reserve battery requirements.

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1   !  APPENDIX A1
2   !
3   !  Worst Case Inverter Ratings Program
5   !  ----------------------------------
6   !
7   !
8   !
9   !
11     DEG
20     OPTION BASE 1
30     PRINT " SELECT PWM SCHEME BY SELECTING SOFTKEY"
40     DIM Inter(100),Har(100),Sw1(1440),Vload(100),Vloadphase(100),Vout(100)
50     DIM Ioutmag(100),Ioutphase(100),Iout(1000),Cos1(100),Sin1(100),Iin(100),Is
w(1000)
60     DIM Hfhar(100),Iinhf(100)
70     ON KEY 0 LABEL "P&H 5" GOTO Ph5
80     ON KEY 1 LABEL "P&H 2" GOTO Ph2
90     ON KEY 3 LABEL "PESC87" GOTO Pesc87_pro_pwm
100!   ON KEY 2 LABEL "SQUARE" GOTO Square
110    ON KEY 4 LABEL "PH2_7" GOTO Ph2_7
120    ON KEY 5 LABEL "P&H_31" GOTO Ph_31
130    GOTO 70
140 Square:  !
150          Angles=1
160          Intersections=6
170          Inter(1)=90
180          Inter(2)=90
190          Inter(3)=180
200          Inter(4)=270
210          Inter(5)=270
220          Inter(6)=360
230          GOTO Start
240 Ph2_7:        !
250       Angles=3
260       Intersections=14
270       Inter(1)=7.107788
280       Inter(2)=70.8794
290       Inter(3)=81.40777
300       Inter(4)=180-Inter(3)
310       Inter(5)=180-Inter(2)
320       Inter(6)=180-Inter(1)
330       Inter(7)=180
340       Inter(8)=180+Inter(1)
350       Inter(9)=180+Inter(2)
360       Inter(10)=180+Inter(3)
370       Inter(11)=360-Inter(3)
380       Inter(12)=360-Inter(2)
390       Inter(13)=360-Inter(1)
400       Inter(14)=360
410       GOTO Start
420 Ph2:  !
430       Angles=2
440       Intersections=10
450       Inter(1)=16.2448
460       Inter(2)=22.0630
470       Inter(3)=180-Inter(2)
480       Inter(4)=180-Inter(1)
490       Inter(5)=180
```

```
500         Inter(6)=180+Inter(1)
510         Inter(7)=180+Inter(2)
520         Inter(8)=360-Inter(2)
530         Inter(9)=360-Inter(1)
540         Inter(10)=360
550         GOTO Start
560 Ph5:        !
570             Angles=5
580             Intersections=22
590             Inter(1)=6.7952
600             Inter(2)=17.2962
610             Inter(3)=21.0252
620             Inter(4)=34.6566
630             Inter(5)=35.9840
640             Inter(6)=180-Inter(5)
650             Inter(7)=180-Inter(4)
660             Inter(8)=180-Inter(3)
670             Inter(9)=180-Inter(2)
680             Inter(10)=180-Inter(1)
690             Inter(11)=180
700             Inter(12)=180+Inter(1)
710             Inter(13)=180+Inter(2)
720             Inter(14)=180+Inter(3)
730             Inter(15)=180+Inter(4)
740             Inter(16)=180+Inter(5)
750             Inter(17)=360-Inter(5)
760             Inter(18)=360-Inter(4)
770             Inter(19)=360-Inter(3)
780             Inter(20)=360-Inter(2)
790             Inter(21)=360-Inter(1)
800             Inter(22)=360
810             GOTO Start
820 Pesc87_pro_pwm:             !
830                             Angles=11
840                             Intersections=46
850                             Inter(1)=3.01482
860                             Inter(2)=6.628317
870                             Inter(3)=9.04997
880                             Inter(4)=13.24088
890                             Inter(5)=15.101288
900                             Inter(6)=19.82383
910                             Inter(7)=21.17835
920                             Inter(8)=26.36674
930                             Inter(9)=27.28896
940                             Inter(10)=32.8635
950                             Inter(11)=33.4385
960                             Inter(12)=180-Inter(11)
970                             Inter(13)=180-Inter(10)
980                             Inter(14)=180-Inter(9)
990                             Inter(15)=180-Inter(8)
1000                            Inter(16)=180-Inter(7)
1010                            Inter(17)=180-Inter(6)
1020                            Inter(18)=180-Inter(5)
1030                            Inter(19)=180-Inter(4)
1040                            Inter(20)=180-Inter(3)
1050                            Inter(21)=180-Inter(2)
1060                            Inter(22)=180-Inter(1)
1070                            Inter(23)=180
```

```
1080                            Inter(24)=180+Inter(1)
1090                            Inter(25)=180+Inter(2)
1100                            Inter(26)=180+Inter(3)
1110                            Inter(27)=180+Inter(4)
1120                            Inter(28)=180+Inter(5)
1130                            Inter(29)=180+Inter(6)
1140                            Inter(30)=180+Inter(7)
1150                            Inter(31)=180+Inter(8)
1160                            Inter(32)=180+Inter(9)
1170                            Inter(33)=180+Inter(10)
1180                            Inter(34)=180+Inter(11)
1190                            Inter(35)=360-Inter(11)
1200                            Inter(36)=360-Inter(10)
1210                            Inter(37)=360-Inter(9)
1220                            Inter(38)=360-Inter(8)
1230                            Inter(39)=360-Inter(7)
1240                            Inter(40)=360-Inter(6)
1250                            Inter(41)=360-Inter(5)
1260                            Inter(42)=360-Inter(4)
1270                            Inter(43)=360-Inter(3)
1280                            Inter(44)=360-Inter(2)
1290                            Inter(45)=360-Inter(1)
1300                            Inter(46)=360
1310                            GOTO Start
1320 Ph_31:!
1330                            Angles=10
1340                            Intersections=42
1350                            Inter(1)=5.4931
1360                            Inter(2)=9.5486
1370                            Inter(3)=16.6065
1380                            Inter(4)=19.3359
1390                            Inter(5)=27.7902
1400                            Inter(6)=29.3928
1410                            Inter(7)=39.0637
1420                            Inter(8)=39.8068
1430                            Inter(9)=50.8458
1440                            Inter(10)=51.0535
1450                            Inter(11)=180-Inter(10)
1460                            Inter(12)=180-Inter(9)
1470                            Inter(13)=180-Inter(8)
1480                            Inter(14)=180-Inter(7)
1490                            Inter(15)=180-Inter(6)
1500                            Inter(16)=180-Inter(5)
1510                            Inter(17)=180-Inter(4)
1520                            Inter(18)=180-Inter(3)
1530                            Inter(19)=180-Inter(2)
1540                            Inter(20)=180-Inter(1)
1550                            Inter(21)=180
1560                            Inter(22)=180+Inter(1)
1570                            Inter(23)=180+Inter(2)
1580                            Inter(24)=180+Inter(3)
1590                            Inter(25)=180+Inter(4)
1600                            Inter(26)=180+Inter(5)
1610                            Inter(27)=180+Inter(6)
1620                            Inter(28)=180+Inter(7)
1630                            Inter(29)=180+Inter(8)
1640                            Inter(30)=180+Inter(9)
1650                            Inter(31)=180+Inter(10)
```

```
1660                        Inter(32)=360-Inter(10)
1670                        Inter(33)=360-Inter(9)
1680                        Inter(34)=360-Inter(8)
1690                        Inter(35)=360-Inter(7)
1700                        Inter(36)=360-Inter(6)
1710                        Inter(37)=360-Inter(5)
1720                        Inter(38)=360-Inter(4)
1730                        Inter(39)=360-Inter(3)
1740                        Inter(40)=360-Inter(2)
1750                        Inter(41)=360-Inter(1)
1760                        Inter(42)=360
1770                        GOTO Start
1780 Start:          !
1790                 PRINT CHR$(12)
1800                 PRINT "Solving the System Per Unit ratings"
1810                 PRINT "      ————————PLEASE WAIT————————"
1820                 OFF KEY
1830                 !
1840 !*****************************************************************************
1850 !***********                    INVERTER STAGE       **********************
1860 !*****************************************************************************
1870 !
1880                 !
1890 ! INVERTER TRANSFER FUNCTION LINE TO NEUTRAL
1900! ————————————————————————————————————————————————————————————————————————
1910                 !
1920                 FOR N=1 TO 100 STEP 2              ! USING FOURIER SERIES
1930                 IF N MOD (3)=0 THEN GOTO 2000      ! TO SOLVE HARMONIC
1940                 Dummy=0                            ' COMPONENTS
1950                 FOR K=1 TO Angles
1960                 Dummy=Dummy+(-1)^K*COS(N*Inter(K))
1970                 NEXT K
1980                 Har(N)=(Dummy*2+1)*4/PI/N/2
1990            !    PRINT N,Har(N),ABS(Har(N)/Har(1))*100
2000                 NEXT N
2010                 !
2020   ! INVERTER LINE TO NEUTRAL SWITCHING FUNCTION (TIMEDOMAIN)
2030  !————————————————————————————————————————————————————
2040                 !
2050                 K=1
2060                 J=1
2070                 FOR I=1 TO 360
2080                 IF Inter(K)<I THEN
2090                 IF J=1 THEN
2100                 J=0
2110                 ELSE
2120                 J=1
2130                 END IF
2140                 K=K+1
2150                 END IF
2160                 Sw1(I)=J
2170                 NEXT I
2180       !
2190       !         FINDING THE OUTPUT FILTER BREAK  FREQUENCY
2200   !*************************************************************************
2210   !
2220       !         UNDER RESISTIVE LOAD CONDITIONS OF 1PU
2230       !         DOMINANT IS REDUCED TO 2% BY PROPERLY PLACING WN
```

```
2240        !
2250        Wh=100                                          ! STEP THROUGH ALL
2260        FOR N=5 TO 100 STEP 2                           ! HARMONICS TO FIND
2270        IF N MOD (3)=0 THEN GOTO 2320                   ! DOMINANT HARMONIC
2280        IF ABS(Har(N)/Har(1))<.02 THEN GOTO 2320
2290        Dummy=N*(ABS(Har(1))*.020/ABS(Har(N)))^.5
2300        IF Dummy<Wh THEN Wh=Dummy
2310     !  PRINT N,Wh
2320        NEXT N
2330        !
2340        !                   FILTER IMPEDENCES
2350        Xcc=2*.707*Wh       ! INDUSTRIAL TYPICALLY ACCEPTED DAMPING
2360        Xlo=2*.707/Wh       ! FACTOR IS .707
2370     !  Xcc=1
2380    !   Xlo=.1
2390        !
2400                ! SOLVING WORST CASE SWITCH RATINGS
2410      !*****************************************************
2420      !
2430      ! WORST CASE  IS WHEN INVERTER OUTPUT LINE VOLTAGE IS IN PHASE WITH THE
2440      ! OUTPUT CURRENT. USING THE FILTER COMPONENTS ALREADY SOLVED WE USE
2450      ! THE SECANT ITERATIVE METHOD TO SOLVE FOR THE LOAD CONDITIONS
2460      ! WHERE IOUT AND VOUT ARE IN PHASE
2470    !
2480    Count=0
2490        A1=.5   ! INITIAL POWER FACTOR GUESS
2500        A2=1
2510        R1=A1
2520        Count=Count+1
2530        IF A1>=1 THEN
2540        R1=.99
2550        A1=.99
2560        END IF
2570        IF A1<0 THEN
2580        R1=.01
2590        A1=.01
2600        END IF
2610        Xc1=SQR(1-R1^2)
2620        IF Inductive=1 THEN Xc1=-Xc1
2630        A=R1*Xcc^2/(R1^2+(-Xc1-Xcc)^2)
2640        B=Xlo-(Xcc*R1^2+Xcc*(-Xc1)*(-Xc1-Xcc))/(R1^2+(-Xc1-Xcc)^2)
2650        Sol1=-ATN(B/A)
2660        IF A<0 THEN Sol1=Sol1+180
2670        R1=A2
2680        IF A2>1 THEN
2690        R1=1
2700        A2=1
2710        END IF
2720        IF A2<0 THEN
2730        A2=0
2740        R1=0
2750        END IF
2760        Xc1=SQR(1-R1^2)
2770        IF Inductive=1 THEN Xc1=-Xc1
2780        A=R1*Xcc^2/(R1^2+(-Xc1-Xcc)^2)
2790        B=Xlo-(Xcc*R1^2+Xcc*(-Xc1)*(-Xc1-Xcc))/(R1^2+\-Xc1-Xcc)^2)
2800        Sol2=-ATN(B/A)
2810        IF A<0 THEN Sol2=Sol2+180
```

```
2820        Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
2830        IF ABS(Sol3-A2)<.0001 THEN GOTO Solved1
2840        A1=A2
2850        A2=Sol3
2860        IF Count>200 THEN
2870        Count=0
2880        Inductive=1
2890        END IF
2900        GOTO 2510
2910        !
2920 Solved1:       !  SOLUTION TO RL IS GIVEN IN Sol3
2930                !-------------------------------------------------------
2940                !
2950        Rl=Sol3
2960        IF Sol3<.7 THEN Rl=.7
2970        Xcl=SQR(1-Rl^2)
2980        Xll=0
2990        IF Inductive=1 THEN
3000        Xcl=0
3010        Xll=SQR(1-Rl^2)
3020        END IF
3030                Rl_temp=Rl      .     FOR USE LATER (KVA RATINGS)
3040        !
3050        ! SINCE THE OUTPUT VOLTAGE OF A UPS IS FIXED AT 1pu,THE DC BUS
3060        ! VOLTAGE MUST BE ADJUSTED TO THE GAIN OF THE PWM SCHEME AT THE
3070        ! SOLVED LOAD CONDITIONS. THIS
3080        ! IN TURN GIVES THE CORRECT pu CURRENT RATINGS OF THE DEVICES
3090        ! UNDER CONSIDERATION.
3100        !
3110        ! ADJUSTING THE DC BUS VOLTAGE LEVEL AND THE HARMONICS
3120        ! TO OBTAIN 1 PU OUTPUT VOLTAGE PEAK
3130        !
3140        N=1
3150        A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
3160        B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
3170        Dcbus=ABS(SQR(A^2+B^2)/Har(1))
3180        Dcbus_temp=Dcbus  ! FOR LATER USE DURING HF LINK CALCULATIONS
3190        FOR N=1 TO 100 STEP 2     ! USING THE DC BUS AND LOAD CONDITIONS
3200        Vout(N)=Har(N)*Dcbus      ! ADJUST THE INVERTER OUTPUT VOLTAGE
3210        NEXT N                    ! HARMONICS
3220        !
3230        !                    INVERTER OUTPUT LINE CURRENT
3240        !-------------------------------------------------------
3250        !
3260        FOR N=1 TO 100 STEP 2
3270        IF N MOD (3)=0 THEN GOTO 3330          ! HRMONIC  COMPONENTS
3280        A=Rl*Xco^2/N^2/(Rl^2+(N*Xll-Xcl/N-Xco/N)^2)
3290        B=N*Xlo-(Xco*Rl^2/N+Xco/N*(N*Xll-Xcl/N)*(N*Xll-Xcl/N-Xco/N))/(Rl^2+(N
*Xll-Xcl/N-Xco/N)^2)
3300        Ioutmag(N)=Vout(N)/SQR(A^2+B^2)
3310        Ioutphase(N)=-ATN(B/A)
3320        IF A<0 THEN Ioutphase(N)=Ioutphase(N)+180
3330        NEXT N
3340        !
3350        ! FINDING THE INVERTER OUTPUT CURRENT IN THE TIME DOMAIN FROM THE
3360        ! SUM OF ITS HARMONICS.
3370        ! ------------------------------------------------------------
3380        FOR Wt=1 TO 360 STEP 1
```

```
3390        Dummy=0
3400        FOR N=1 TO 100 STEP 2
3410        IF N MOD (3)=0 THEN GOTO 3430
3420        Dummy=Dummy+Ioutmag(N)*SIN(N*Wt+Ioutphase(N))
3430        NEXT N
3440        Iout(Wt)=Dummy
3450        NEXT Wt
3460        !
3470  !                          SWITCH CURRENT AND RATINGS
3480  !   (MULTIPYING THE LINE CURRENT BY THE SWITCHING FUNCTION IN TIME DOMAIN)
3490        !-------------------------------------------------------------------
3500        !
3510        Dummy=0
3520        FOR Wt=1 TO 360 STEP 1
3530        IF (Iout(Wt)>0) AND Sw1(Wt)>0 THEN
3540                          Dummy=Dummy+Sw1(Wt)*Iout(Wt)
3550        END IF
3560        NEXT Wt
3570        Iswave=Dummy/360
3580        !
3590        !
3600        !                SOLVING THE INPUT FILTER COMPONENTS
3610        !*****************************************************************
3620        !
3630        ! WORST CASE micro farad condition FOR THE CAPACITOR
3640        !  AT THE INPUT OCCURS WHEN THE LOAD
3650        !    IS MAXIMUM LEAD THEREFORE INPUT CURRENT IS FIRST SOLVED
3660        !    USING A LOAD OF .7 LEADING AND THE OUTPUT FILTER
3670        !    DESIGNED EARLIER
3680        !    THIS GIVES US THE WORST CASE FOR THE CAPACITOR
3690        !
3700        !
3710        ! FIRST PASS
3720        !
3730        Rl=.7
3740        Xll=0
3750        Xcl=SQR(1-Rl^2)
3760        !
3770        ! ADJUSTING THE DC BUS VOLTAGE LEVEL AND THE HARMONICS
3780        ! TO OBTAIN 1 PU OUTPUT VOLTAGE PEAK
3790        !
3800        N=1
3810        A=(1-N^2*Xlo/Xoo+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
3820        B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
3830        Dcbus=ABS(SQR(A^2+B^2)/Har(N))
3840        Dcbus_lead=Dcbus ! FOR USE DURING THE HF LINK ROUTINE
3850        FOR N=1 TO 100 STEP 2
3860        Vout(N)=Har(N)*Dcbus
3870        NEXT N
3880        !
3890        !                       INVERTER OUTPUT LINE CURRENT
3900        !-------------------------------------------------------------------
3910        !
3920        FOR N=1 TO 100 STEP 2
3930        IF N MOD (3)=0 THEN GOTO 3990
3940        A=Rl*Xoo^2/N^2/(Rl^2+(N*Xll-Xcl/N-Xoo/N)^2)
3950        B=N*Xlo-(Xoo*Rl^2/N+Xoo/N*(N*Xll-Xcl/N)*(N*Xll-Xcl/N-Xoo/N))/(Rl^2+(N
*Xll-Xcl/N-Xoo/N)^2)
```

```
3960        Ioutmag(N)=Vout(N)/SQR(A^2+B^2)
3970        Ioutphase(N)=-ATN(B/A)
3980        IF A<0 THEN Ioutphase(N)=Ioutphase(N)+180
3990        NEXT N
4000        !
4010        !              SOLVING THE INPUT CURRENT SPECTRUM
4020        !-------------------------------------------------------------
4030        !
4040        FOR N=1 TO 100 STEP 2     ! OUTPUT LINE CURRENT HARMONICS
4050        FOR K=1 TO 100 STEP 2     ! INVERTER IN VOLTAGE SWITCHING FUNCTION
4060        !
4070        IF (N-K)=0 THEN
4080        Dc_input=Dc_input+COS(Ioutphase(N))*Ioutmag(N)*Har(K)/2
4090        GOTO 4220
4100        END IF
4110        !
4120        IF ((N-K)<0) AND ((N-K) MOD (6)=0) THEN
4130        Cos1(ABS(N-K))=Cos1(ABS(N-K))+COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
4140        Sin1(ABS(N-K))=Sin1(ABS(N-K))+SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
4150        GOTO 4220
4160        END IF
4170        !
4180        IF ((N-K)>0) AND ((N-K) MOD (6)=0) THEN
4190        Cos1(N-K)=Cos1(N-K)+COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
4200        Sin1(N-K)=Sin1(N-K)-SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
4210        END IF
4220        IF ((N+K) MOD (6)=0) AND ((N+K)<55) THEN
4230        Cos1(N+K)=Cos1(N+K)-COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
4240        Sin1(N+K)=Sin1(N+K)+SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
4250        END IF
4260        NEXT K
4270        NEXT N
4280 Solved2:       !
4290                FOR I=6 TO 100 STEP 6
4300                Iin(I)=SQR(Cos1(I)^2+Sin1(I)^2)*3  ! CALCULATION OF
4310                NEXT I                             ! HARMONICS
4320                Dc_input=Dc_input*3
4330        !
4340        !  THE SECANT METHOD IS USED AS A LINEAR SEARCH TECHNIQUE (2 TIMES)
4350        !  IN ORDER TO FIND THE INPUT FILTER COMPONENTS
4360        !  INPUT VOLTAGE THD IS LIMITD TO   5%
4370        !  INPUT CURRENT THD IS LIMITED TO 10%
4380        !-------------------------------------------------------------
4390        !
4400        A1in=.1
4410        A2in=.2
4420        A1=A1in
4430        A2=A2in
4440        ON ERROR GOTO 4590
4450        Dummy=0
4460        Dummy1=0
4470        FOR N=6 TO 100 STEP 6
4480        Dummy=Dummy+(Iin(N)/(1-N^2*A1))^2
4490        Dummy1=Dummy1+(Iin(N)/(1-N^2*A2))^2
4500        NEXT N
4510        Sol1=100*SQR(Dummy)/Dc_input-10
4520        Sol2=100*SQR(Dummy1)/Dc_input-10
4530        Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
```

```
4550        IF ABS(Sol3-A2)<.00001 THEN GOTO Solution3
4560        A1=A2
4570        A2=Sol3
4580        GOTO 4450
4590        A1in=A1in/10
4600        A2in=A2in/10
4610        GOTO 4420
4620 Solution3: !
4630            OFF ERROR
4640            Xf=Sol3
4650            IF Xf<0 THEN GOTO 4590
4660        !
4670        A1=1
4680        A2=5
4690        Dummy=0
4700        Dummy1=0
4710        FOR N=6 TO 100 STEP 6
4720        Dummy=Dummy+(Iin(N)*N*A1*Xf/(1-N^2*Xf))^2
4730        Dummy1=Dummy1+(Iin(N)*N*A2*Xf/(1-N^2*Xf))^2
4740        NEXT N
4750        Sol1=100*SQR(Dummy)/Dcbus-5
4760        Sol2=100*SQR(Dummy1)/Dcbus-5
4770        Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
4780        IF ABS(Sol3-A2)<.00001 THEN GOTO Solution4
4790        A1=A2
4800        A2=Sol3
4810        GOTO 4690
4820 Solution4:      !
4830                 Xci_temp=Sol3   ! TEMPORARY STORAGE OF THE INPUT FILTER
4840                 !                 CAPACITOR
4860                 !
4870                 !-------------------------------------------------
4880                   !
4890                   !
4900        !   2ND PASS
4910        !
4920        !   WORST CASE CONDITIONS FOR THE INPUT FILTER INDUCTOR
4930        !   micro henry size
4940        !   OCCURS AT A LAGGING  LOAD POWER FACTOR OF .7
4950        !   USING THE OUTPUT FILTER DESIGNED EARLIER
4960        !   THIS GIVES US THE WORST CASE FOR THE INDUCTOR
4970        !-------------------------------------------------
4980        !
4990        R1=.7
5000        Xc1=0
5010        X11=SQR(1-R1^2)
5020        !
5030        ! ADJUSTING THE DC BUS VOLTAGE LEVEL AND THE HARMONICS
5040        ! TO OBTAIN 1 PU OUTPUT VOLTAGE PEAK
5050        !
5060        N=1
5070        A=(1-N^2*X1o/Xco+N*X1o*(N*X11-Xc1/N)/(R1^2+(N*X11-Xc1/N)^2))
5080        B=(N*X1o*R1/(R1^2+(N*X11-Xc1/N)^2))
5090        Dcbus=ABS(SQR(A^2+B^2)/Har(N))
5100        Dcbus_lag=Dcbus ! FOR USE LATER DURING HF LINK ROUTINE
5110        FOR N=1 TO 100 STEP 2
5120        Vout(N)=Har(N)*Dcbus
5130        NEXT N
```

```
5140        !
5150        !                    INVERTER OUTPUT LINE CURRENT
5160        !-------------------------------------------------------------
5170        !
5180        FOR N=1 TO 100 STEP 2
5190        IF N MOD (3)=0 THEN GOTO 5250
5200        A=R1*Xcc^2/N^2/(R1^2+(N*X11-Xc1/N-Xcc/N)^2)
5210        B=N*Xlo-(Xcc*R1^2/N+Xcc/N*(N*X11-Xc1/N)*(N*X11-Xc1/N-Xcc/N))/(R1^2+(N
*X11-Xc1/N-Xcc/N)^2)
5220        Ioutmag(N)=Vout(N)/SQR(A^2+B^2)
5230        Ioutphase(N)=-ATN(B/A)
5240        IF A<0 THEN Ioutphase(N)=Ioutphase(N)+180
5250        NEXT N
5260        !
5270        !            SOLVING THE INPUT CURRENT SPECTRUM
5280        !-------------------------------------------------------------
5290        !
5300        MAT Cos1= (0)     ! RESET ALL ARRAYS
5310        MAT Sin1= (0)
5320        Dc_input=0
5330        !
5340        FOR N=1 TO 100 STEP 2     ! OUTPUT LINE CURRENT HARMONICS
5350        FOR K=1 TO 100 STEP 2    ! INVERTER IN VOLTAGE SWITCHING FUNCTION
5360        !
5370        IF (N-K)=0 THEN
5380        Dc_input=Dc_input+COS(Ioutphase(N))*Ioutmag(N)*Har(K)/2
5390        GOTO 5520
5400        END IF
5410        !
5420        IF ((N-K)<0) AND ((N-K) MOD (6)=0) THEN
5430        Cos1(ABS(N-K))=Cos1(ABS(N-K))+COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
5440        Sin1(ABS(N-K))=Sin1(ABS(N-K))+SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
5450        GOTO 55^^
5460        END IF
5470        !
5480        IF ((N-K)>0) AND ((N-K) MOD (6)=0) THEN
5490        Cos1(N-K)=Cos1(N-K)+COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
5500        Sin1(N-K)=Sin1(N-K)-SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
5510        END IF
5520        IF ((N+K) MOD (6)=0) AND ((N+K)<55) THEN
5530        Cos1(N+K)=Cos1(N+K)-COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
5540        Sin1(N+K)=Sin1(N+K)+SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
5550        END IF
5560        NEXT K
5570        NEXT N
5580 Solved7:      !
5590               Dummy=0
5600               FOR I=6 TO 100 STEP 6
5610               Iin(I)=SQR(Cos1(I)^2+Sin1(I)^2)*3
5620               Dummy=Dummy+Iin(I)
5630               NEXT I
5640               Dc_input=Dc_input*3
5650        !
5660        !  THE SECANT METHOD IS USED AS A LINEAR SEARCH TECHNIQUE (2 TIMES)
5670        !  IN ORDER TO FIND THE INPUT FILTER COMPONENTS
5680        !  INPUT VOLTAGE THD IS LIMITED TO  5.0%
5690        !  INPUT CURRENT THD IS LIMITED TO 10.0%
5700        !-------------------------------------------------------------
```

```
5710        !
5720        A1in=.1
5730        A2in=.2
5740        A1=A1in
5750        A2=A2in
5760        Dummy=0
5770        Dummy1=0
5780        ON ERROR GOTO 5900
5790        FOR N=6 TO 100 STEP 6
5800        Dummy=Dummy+(Iin(N)/(1-N^2*A1))^2
5810        Dummy1=Dummy1+(Iin(N)/(1-N^2*A2))^2
5820        NEXT N
5830        Sol1=100*SQR(Dummy)/Dc_input-10.0
5840        Sol2=100*SQR(Dummy1)/Dc_input-10.0
5850        Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
5860        IF ABS(Sol3-A2)<.000001 THEN GOTO Solution5
5870        A1=A2
5880        A2=Sol3
5890        GOTO 5760
5900        A1in=A1in/10
5910        A2in=A2in/10
5920        GOTO 5740
5930 Solution5: !
5940              OFF ERROR
5950              Xf=Sol3
5960              IF Xf<0. THEN GOTO 5900
5961              GOTO Solution6
5970        !
5980        A1=1
5990        A2=5
6000        Dummy=0
6010        Dummy1=0
6020        FOR N=6 TO 100 STEP 6
6030        Dummy=Dummy+(Iin(N)*N*A1*Xf/(1-N^2*Xf))^2
6040        Dummy1=Dummy1+(Iin(N)*N*A2*Xf/(1-N^2*Xf))^2
6050        NEXT N
6060        Sol1=100*SQR(Dummy)/Dcbus-5.0
6070        Sol2=100*SQR(Dummy1)/Dcbus-5.0
6080        Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
6090        IF ABS(Sol3-A2)<.00001 THEN GOTO Solution6
6100        A1=A2
6110        A2=Sol3
6120        GOTO 6000
6130 Solution6:       !
6140                  Xli=Xf*Xci_temp ! INPUT FILTER SIZE
6150                  Xci=Xci_temp
6160        !
6170        !
6180                  !    SOLVING THE CAPACITOR KVA
6190     !-------------------------------------------------------------
6200                  !
6210     ! THE WORST CASE RIPPLE CURRENT FOR THE CAPACITOR IS WHEN LOAD IS .7 LAG
6220     ! ASSUME XCI DELIVERS ALL INVERTER RIPPLE CURRENT
6230     ! THE WORST CASE VOLTAGE RIPPLE ACROSS THE INDUCTOR IS PRODUCED BY THE
6240     ! WORST CASE CURRENT RIPPLE THROUGH THE CAPACITOR. IT IS CALCULATED BY
6250     ! THE CAPACITOR IMPEDENCE * CAPACITOR WORST CASE CURRENT RIPPLE
6260     !
6270                  Dummy=0
```

```
6280              Dummy1=0
6290                FOR N=6 TO 54 STEP 6
6300                Dummy=Dummy+(Iin(N)/SQR(2))^2
6310                Dummy1=Dummy1+(Iin(N)*Xci_temp/N/SQR(2))^2
6320                NEXT N
6330                Xciirms=SQR(Dummy)
6340                Xlivrms=SQR(Dummy1)
6350        !-------------------------------------------
6360              Xcivrms=Dcbus
6370              !
6380        Rl=Rl_temp
6390        Xll=0
6400        Xcl=SQR(1-Rl^2)
6410        IF Inductive=1 THEN
6420        Xcl=0
6430        Xll=SQR(1-Rl^2)
6440        END IF
6450        N=1
6460        A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
6470        B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
6480        Dcbus=ABS(SQR(A^2+B^2)/Har(N))
6490        Preal_temp=Rl_temp*.5*3
6500        Xliirms=Preal_temp/Dcbus
6510        !-------------------------------------------
6520        !
6530        !       FINDING THE DC BUS VOLTAGE SWING
6540        !*********************************************
6550        Rl=.7
6560        Xll=.714
6570        Xcl=0
6580        N=1
6590        A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
6600        B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
6610        Dcbusmax=ABS(SQR(A^2+B^2)/Har(N))
6620        Rl=.7
6630        Xll=0
6640        Xcl=.714
6650        N=1
6660        A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
6670        B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
6680        Dcbusmin=ABS(SQR(A^2+B^2)/Har(N))
6690        !
6700        !                   OUTPUT FILTER
6710        !  (WORST CASE FOR CAPACITOR IS AT LOAD POWER FACTOR .7 LAG)
6720        !  (WORST CASE FOR INDUCTOR IS AT LOAD POWER FACTOR .7 LEAD)
6730        !*************************************************************************
6740        !
6750        !
6760        !             OUTPUT FILTER CAPACITOR
6770        !-------------------------------------------
6780        Rl=.7
6790        Xll=SQR(1-Rl^2)
6800        Xcl=0
6810        FOR N=1 TO 100 STEP 2
6820        IF N MOD 3=0 THEN GOTO 6860
6830        A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
6840        B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
6850        Vload(N)=Har(N)*Dcbusmax/SQR(A^2+B^2)
```

```
6860        NEXT N
6870        !
6880        Dummy=0
6890        Dummy1=0
6900          FOR N=1 TO 100 STEP 2
6910          IF N MOD (3)=0 THEN GOTO 6940
6920          Dummy=Dummy+(Vload(N)/SQR(2))^2
6930          Dummy1=Dummy1+(Vload(N)*N/Xco/SQR(2))^2
6940          NEXT N
6950          Xcovrms=SQR(Dummy)
6960          Xcoirms=SQR(Dummy1)
6970          Xcova=Xcoirms*Xcovrms
6980          !
6990          !                OUTPUT FILTER INDUCTOR
7000          !-------------------------------------------
7010          !
7020          !   WORST CASE FOR VOLTAGE IS WHEN LOAD PF=.7 LAGGING
7030          Xcl=0
7040          Rl=.7
7050          Xll=SQR(1-Rl^2)
7060        FOR N=1 TO 100 STEP 2
7070        IF N MOD (3)=0 THEN GOTO 7110
7080        A=Rl*Xco^2/N^2/(Rl^2+(N*Xll-Xcl/N-Xco/N)^2)
7090        B=N*Xlo-(Xco*Rl^2/N+Xco/N*(N*Xll-Xcl/N)*(N*Xll-Xcl/N-Xco/N))/(Rl^2+(N
*Xll-Xcl/N-Xco/N)^2)
7100        Ioutmag(N)=Dcbusmax*Har(N)/SQR(A^2+B^2)
7110        NEXT N
7120        !
7130        Dummy1=0
7140          FOR N=1 TO 100 STEP 2
7150          IF N MOD (3)=0 THEN GOTO 7170
7160          Dummy1=Dummy1+(Ioutmag(N)*N*Xlo/SQR(2))^2
7170          NEXT N
7180          Xlovrms=SQR(Dummy1)
7190          !
7200          !   WORST CASE FOR CURRENT IS WHEN PF=.7 LEADING
7210          !
7220          Xll=0
7230          Rl=.7
7240          Xcl=SQR(1-Rl^2)
7250        FOR N=1 TO 100 STEP 2
7260        IF N MOD (3)=0 THEN GOTO 7300
7270        A=Rl*Xco^2/N^2/(Rl^2+(N*Xll-Xcl/N-Xco/N)^2)
7280        B=N*Xlo-(Xco*Rl^2/N+Xco/N*(N*Xll-Xcl/N)*(N*Xll-Xcl/N-Xco/N))/(Rl^2+(N
*Xll-Xcl/N-Xco/N)^2)
7290        Ioutmag(N)=Dcbusmin*Har(N)/SQR(A^2+B^2)
7300        NEXT N
7310        !
7320        Dummy=0
7330        Dummy1=0
7340          FOR N=1 TO 100 STEP 2
7350          IF N MOD (3)=0 THEN GOTO 7370
7360          Dummy=Dummy+(Ioutmag(N)/SQR(2))^2
7370          NEXT N
7380          Xloirms=SQR(Dummy)
7390          Xlova=Xloirms*Xlovrms
7400          !*******************************************************
7410          !*******************************************************
```

```
7420          !           INVERTER PU RATINGS HAVE BEEN DERIVED
7430          !*****************************************************
7440          !*****************************************************
7450          PRINT CHR$(12)
7460          PRINT "Inverter worst case pu ratings"
7470          PRINT "-----------------------------"
7480        PRINT "OUTPUT VOLTAGE=1pu PEAK"
7490        PRINT "OUTPUT  VA    =1.5pu      "
7500        PRINT "OUTPUT CURRENT=1pu PEAK"
7510        PRINT "LOAD IMPEDENCE=1pu/phase Y connection"
7520        PRINT
7530        PRINT "DC BUS VOLTAGE SWINGS FROM";PROUND(Dcbusmin,-2);"pu TO ";PROUN
D(Dcbusmax,-2);"pu"
7540        PRINT "AVERAGE SWITCH CURRENT=";PROUND(Iswave,-3);"pu"
7550        PRINT
7560        PRINT "INPUT FILTER       "
7570        PRINT "IND=";PROUND(Xli,-3);"pu","  Irms=";PROUND(Xliirms,-3);"pu","  V
rms=";PROUND(Xlivrms,-3);"pu"
7580        PRINT "CAP=";PROUND(Xci,-3);"pu","  Irms=";PROUND(Xciirms,-3);"pu","  V
rms=";PROUND(Xcivrms,-3);"pu"
7590        PRINT
7600        PRINT "OUTPUT FILTER"
7610        PRINT "IND=";PROUND(Xlo,-3);"pu","  Irms=";PROUND(Xloirms,-3);"pu","  V
rms=";PROUND(Xlovrms,-3);"pu"
7620        PRINT "CAP=";PROUND(Xco,-3);"pu","  Irms=";PROUND(Xcoirms,-3);"pu","  V
rms=";PROUND(Xcovrms,-3);"pu"
7630        PRINT
7640        IF Flag=1 THEN GOTO 9860
7650                    !*****************************************************
7660                    !   HIGH FREQUENCY LINK STAGE WORST CASE PU CALCULATIONS
7670                    !*****************************************************
7680                    !
7690                    !
7700            !
7710            High_freq=20000 !SWITCHING FREQUENCY OF HIGH FREQUENCY INVERTER
7720            Tran_ratio=1    ! TRANSFORMER RATIO (TRAN_RATIO : 1)
7730            Enom=Tran_ratio*Dcbusmax/.8 ! NOMINAL BATTERY VOLTAGE
7740            Dutymin=.8/1.1*Dcbusmax/Dcbusmin
7750            !
7760            !
7770            !   WORST CASE RATINGS
7780  !*****************************************************
7790  !
7800  !           DIODES
7810  !           -------
7820    Diodevmax=1.1*Enom/Tran_ratio
7830    Diodeiave=Xliirms/2   !Xliirms=WORST CASE INVERTER INPUT DC CURRENT
7840  !
7850  !           TRANSFORMER
7860  !           -----------
7870  ! FOR THE RMS CURRENT THE
7880  ! WORST CASE EXISTS WHEN E=1.1*Enom ie. MIN DUTY CYCLE & WHEN LOAD  IS
7890  ! CAPACITIVE. HOWEVER THIS POINT VARIES WITH FILTER AND IS THEREFORE
7900  ! FOUND BY ROUTINE LOOP SAMPLING.
7910        FOR Rl=1 TO .85 STEP -.01
7920        Xcl=SQR(1-Rl^2)
7930        Xll=0
7940        N=1
```

```
7950        A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
7960        B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
7970        Dcbus=ABS(SQR(A^2+B^2)/Har(N))
7980     Dc_input=3*Rl/2/Dcbus      !USING EQUAL REAL POWER TO SOLVE DC COMPONENT
7990                                ! OF INVERTER INPUT CURRENT
8000     Duty=Dcbus*.8/1.1/Dcbusmax ! FINDING THE DUTY CYCLE FOR THE WORST CASE
8010            Up=(180-(180*Duty))/2
8020            Down=180-Up
8030             ! FROM PRIMARY SIDE
8040            Dummy=0
8050            Dummy1=0
8060               FOR N=1 TO 100 STEP 2
8070               Hfhar(N)=2/N/PI*(-COS(Down*N)+COS(Up*N))
8080               Dummy1=Dummy1+(Dc_input/Duty/Tran_ratio*Hfhar(N)/SQR(2))^2
8090               NEXT N
8100               IF SQR(Dummy1)>Tranirms THEN Tranirms=SQR(Dummy1)
8110               NEXT Rl
8120               !
8130  ! FOR THE RMS VOLTAGE THE
8140  ! WORST CASE EXISTS WHEN E=1.1*Enom ie. MIN DUTY CYCLE & WHEN THE LOAD
8150  ! IS LAGGING PF=.7
8160     Dcbus=Dcbus_lag! VALUES OF DC BUS VOLTAGE WHEN INVERTER OUTPUT =.7 LAG
8170     Dc_input=3*.7/2/Dcbus!USING EQUAL REAL POWER TO SOLVE DC COMPONENT
8180                                ! OF INVERTER INPUT CURRENT
8190     Duty=Dcbus*.8/1.1/Dcbusmax ! FINDING THE DUTY CYCLE FOR THE WORST CASE
8200            Up=(180-(180*Duty))/2
8210            Down=180-Up
8220             ! FROM PRIMARY SIDE
8230            Dummy=0
8240            Dummy1=0
8250               FOR N=1 TO 100 STEP 2
8260               Hfhar(N)=2/N/PI*(-COS(Down*N)+COS(Up*N))
8270               Dummy=Dummy+(1.1*Enom*Hfhar(N)/SQR(2))^2
8280            !  Dummy1=Dummy1+(Dc_input/Duty/Tran_ratio*Hfhar(N)/SQR(2))^2
8290               NEXT N
8300               Tranvrms=SQR(Dummy)
8310               Tranva=Tranvrms*Tranirms
8320  !
8330  !             HF SWITCH RATINGS
8340  !             ---------------
8350  ! AVERAGE CURRENT IS CALCULATED ASSUMING XLI IS INFINITE->ONLY DC CURRENT
8360  ! THIS IS LEGAL SINCE HF LINK IS OPERATING AT >20Khz
8370  !
8380           Swhfv=1.1*Enom
8390  !  Swhfiave=(MAX REAL OUTPUT POWER*.5)/(.8*Enom)
8400           Swhfiave=1.5*.5/.8/Enom
8410  !
8420  !             INPUT FILTER COMPONENTS
8430  !             -----------------------
8440  !  WORST CASE FOR INDUCTOR MICRO HENRY SIZE OCCURS AT LOAD PF=.7 LEADING
8450  !  AND WHEN E=1.1*Enom (MIN DUTY CYCLE)
8460     Dcbus=Dcbus_lead! VALUES OF DC BUS VOLTAGE WHEN INVERTER OUTPUT VOLTAGE
8470                     !  AND CURRENT ARE IN PHASE FROM ABOVE
8480     Dc_input=3*.7/2/Dcbus!USING EQUAL REAL POWER TO SOLVE DC COMPONENT
8490                                ! OF INVERTER INPUT CURRENT
8500     Duty=Dcbus*.8/1.1/Dcbusmax ! FINDING THE DUTY CYCLE FOR THE WORST CASE
8510     Idc_bat=Dc_input/Tran_ratio*Duty
8520     RAD
```

```
8530        FOR N=1 TO 100 STEP 1
8540        An=Dc_input/N/PI*(1-COS(2*PI*Duty*N))
8550        Bn=Dc_input/N/PI*(SIN(2*PI*Duty*N))
8560        Iinhf(N)=SQR(An^2+Bn^2)
8570        NEXT N
8580        !
8590              !
8600        DEG
8610        !  THE SECANT METHOD IS USED AS A LINEAR SEARCH TECHNIQUE (2 TIMES)
8620        !  IN ORDER TO FIND THE INPUT FILTER COMPONENTS
8630        !  INPUT VOLTAGE THD IS LIMITED TO 2.5%
8640        !  INPUT CURRENT THD IS LIMITED TO 5%
8650        !-------------------------------------------------------------------
8660        !
8670        A1=1.1
8680        A2=2.1
8690        Dummy=0
8700        Dummy1=0
8710        FOR N=1 TO 100 STEP 1
8720        Dummy=Dummy+(Iinhf(N)/(1-N^2*A1))^2
8730        Dummy1=Dummy1+(Iinhf(N)/(1-N^2*A2))^2
8740        NEXT N
8750        Sol1=100*SQR(Dummy)/Idc_bat-5
8760        Sol2=100*SQR(Dummy1)/Idc_bat-5
8770        Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
8780        IF ABS(Sol3-A2)<.00001 THEN GOTO Solution11
8790        A1=A2
8800        A2=Sol3
8810        GOTO 8690
8820 Solution11: !
8830              Xf=Sol3
8840        !
8850        A1=.1
8860        A2=.2
8870        Dummy=0
8880        Dummy1=0
8890        FOR N=1 TO 100 STEP 1
8900        Dummy=Dummy+(Iinhf(N)*N*A1*Xf/(1-N^2*Xf))^2
8910        Dummy1=Dummy1+(Iinhf(N)*N*A2*Xf/(1-N^2*Xf))^2
8920        NEXT N
8930        Sol1=100*SQR(Dummy)/(1.1*Enom)-2.5
8940        Sol2=100*SQR(Dummy1)/(1.1*Enom)-2.5
8950        Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
8960        IF ABS(Sol3-A2)<.00001 THEN GOTO Solution12
8970        A1=A2
8980        A2=Sol3
8990        GOTO 8870
9000 Solution12:     !
9010        Xlhf=Sol3*Xf/(High_freq*2/60) ! WORST CASE HIGH FREQUENCY INDUCTOR
9020         !
9030    ! WORST CASE FOR CAPACITOR MICRO FARAD SIZE OCCURS WHEN 60hz INVERTER
9040    ! OUTPUT VOLTAGE AND CURRENT ARE IN PHASE
9050    !  AND WHEN E=1.1*Enom (MAX DUTY CYCLE)
9060     Dcbus=Dcbus_temp! VALUES OF DC BUS VOLTAGE WHEN INVERTER OUTPUT VOLTAGE
9070                     !  AND CURRENT ARE IN PHASE FROM ABOVE
9080     Dc_input=3*Rl_temp/2/Dcbus!USING EQUAL REAL POWER TO SOLVE DC COMPONENT
9090                               ! OF INVERTER INPUT CURRENT
9100     Duty=Dcbus*.8/1.1/Dcbusmax  ! FINDING THE DUTY CYCLE FOR THE WORST CASE
```

```
9110    Idc_bat=Dc_input/Tran_ratio*Duty
9120    RAD
9130       FOR N=1 TO 100 STEP 1
9140       An=Dc_input/N/PI*(1-COS(2*PI*Duty*N))
9150       Bn=Dc_input/N/PI*(SIN(2*PI*Duty*N))
9160       Iinhf(N)=SQR(An^2+Bn^2)
9170       NEXT N
9180       DEG
9190       !  THE SECANT METHOD IS USED AS A LINEAR SEARCH TECHNIQUE (2 TIMES)
9200       !  IN ORDER TO FIND THE INPUT FILTER COMPONENTS
9210       !  INPUT VOLTAGE THD IS LIMITED TO 2.5%
9220       !  INPUT CURRENT THD IS LIMITED TO 5%
9230       !-------------------------------------------------------------------
9240       !
9250       A1=1.1
9260       A2=2.1
9270       Dummy=0
9280       Dummy1=0
9290       FOR N=1 TO 100 STEP 1
9300       Dummy=Dummy+(Iinhf(N)/(1-N^2*A1))^2
9310       Dummy1=Dummy1+(Iinhf(N)/(1-N^2*A2))^2
9320       NEXT N
9330       Sol1=100*SQR(Dummy)/Idc_bat-5
9340       Sol2=100*SQR(Dummy1)/Idc_bat-5
9350       Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
9360       IF ABS(Sol3-A2)<.00001 THEN GOTO Solution13
9370       A1=A2
9380       A2=Sol3
9390       GOTO 9270
9400 Solution13: !
9410             Xf=Sol3
9420       !
9430       A1=.1
9440       A2=.2
9450       Dummy=0
9460       Dummy1=0
9470       FOR N=1 TO 100 STEP 1
9480       Dummy=Dummy+(Iinhf(N)*N*A1*Xf/(1-N^2*Xf))^2
9490       Dummy1=Dummy1+(Iinhf(N)*N*A2*Xf/(1-N^2*Xf))^2
9500       NEXT N
9510       Sol1=100*SQR(Dummy)/(.8*Enom)-2.5
9520       Sol2=100*SQR(Dummy1)/(.8*Enom)-2.5
9530       Sol3=A2-(Sol2*(A2-A1)/(Sol2-Sol1))
9540       IF ABS(Sol3-A2)<.00001 THEN GOTO Solution14
9550       A1=A2
9560       A2=Sol3
9570       GOTO 9450
9580 Solution14:     !
9590                 Xchf=Sol3*High_freq*2/60     ! HIGH FREQUENCY CAPACITOR
9600              !
9610                 ! FILTER RATINGS
9620      !-------------------------------------
9630     ! SOLVED AT E= 1.1Enom AND INVERTER IOUT AND VOUT ARE IN PHASE
9640    Dcbus=Dcbus_temp! VALUES OF DC BUS VOLTAGE WHEN INVERTER OUTPUT VOLTAGE
9650                    !  AND CURRENT ARE IN PHASE FROM ABOVE
9660    Dc_input=3*Rl_temp/2/Dcbus!USING EQUAL REAL POWER TO SOLVE DC COMPONENT
9670                              ! OF INVERTER INPUT CURRENT
9680    Duty=Dcbus*.8/1.1/Dcbusmax ! FINDING THE DUTY CYCLE FOR THE WORST CASE
```

```
9690    Idc_bat=Dc_input/Tran_ratio*Duty
9700                RAD
9710                Dummy=0
9720                Dummy1=0
9730                FOR N=1 TO 100 STEP 1
9740          An=Dc_input/N/PI*(1-COS(2*PI*Duty*N))
9750          Bn=Dc_input/N/PI*(SIN(2*PI*Duty*N))
9760               Dummy=Dummy+(SQR(An^2+Bn^2)/SQR(2))^2
9770          Dummy1=Dummy1+(SQR((An^2+Bn^2))/SQR(2)*Xchf/(N*High_freq*2/60))^2
9780               NEXT N
9790               DEG
9800               Xchfirms=SQR(Dummy)
9810               Xlhfvrms=SQR(Dummy1)
9820               Xlhfirms=Swhfiave*2
9830               Xchfvrms=1.1*Enom
9840               !
9850        PRINT
9860        PRINT "HF Link worst case pu ratings"
9870        PRINT "-----------------------------"
9880        PRINT "TRANSFORMER RATIO=1:1"
9890        PRINT "HF INVERTER SWITCHING FREQUENCY=";High_freq
9900        PRINT "MAX DIODE VOLTAGE=";PROUND(Diodevmax,-2);"pu"
9910        PRINT "AVE DIODE CURRENT=";PROUND(Diodeiave,-2);"pu"
9920        PRINT "RMS PRIMARY TRANSFORMER VOLTAGE=";PROUND(Tranvrms,-2);"pu"
9930        PRINT "RMS PRIMARY TRANSFORMER CURRENT=";PROUND(Tranirms,-2);"pu"
9940        PRINT "PEAK HF INVERTER SWITCH VOLTAGE=";PROUND(Swhfv,-2);"pu"
9950        PRINT "AVE HF INVERTER SWITCH CURRENT =";PROUND(Swhfiave,-2);"pu"
9960        PRINT
9970        PRINT "INPUT FILTER RATINGS"
9980        PRINT "INDUCTOR=";PROUND(Xlhf,-4);"pu","Irms=";PROUND(Xlhfirms,-2);"p
u","  Vrms=";PROUND(Xlhfvrms,-2);"pu"
9990        PRINT "CAPACITOR=";PROUND(Xchf,-1);"pu","Irms=";PROUND(Xchfirms,-2);"
pu","  Vrms=";PROUND(Xchfvrms,-2);"pu"
10000       Flag=0
10010       ON KEY 1 LABEL "PRINTOUT" GOTO Printout
10020       ON KEY 2 LABEL "PROCEED" GOTO Proceed
10030       GOTO 10010
10040 Printout:     !
10050               Flag=1
10060               PRINTER IS 701
10070               GOTO 7460
10080 Proceed:!
10090         PRINTER IS 1
10100      !
10110       !*************************************************************************
10120       !
10130       !   USER INPUT OF LOAD AND OUTPUT POWER FOR SAMPLE OPERATING POINT
10140       !
10150       !*************************************************************************
10160       !
10170       OFF KEY
10180       PRINT CHR$(12)
10190       V=115*SQR(2) ! THIS IS THE STANDARD NA HYDRO OUTPUT
10200       INPUT "OUTPUT POWER IN KVA",Kva
10210       INPUT "OUTPUT POWER FACTOR .7 -1",Pf
10220       Dummy=0
10230       Lead$lag$="        "
10240       IF Pf=1 THEN
```

```
10250     Xcl=0
10260     Xll=0
10270     GOTO 10300
10280     END IF
10290     INPUT "LEADING(1) OR LAGGING(2)  POWER FACTOR",Dummy
10300     !   SCALING FACTORS
10310       V_scale=V
10320       I_scale=Kva*666.66666/V
10330       Z_scale=3*V^2/2000/Kva
10340       Kva_scale=2*Kva/3*1000
10350       Rl=Pf*Z_scale
10360       IF Dummy=0 THEN GOTO 10460
10370     IF Dummy=1 THEN
10380                     Xcl=SQR(1-Pf^2)*Z_scale
10390                     Xll=0
10400                     Leadlag$="Leading"
10410     ELSE
10420                     Xll=SQR(1-Pf^2)*Z_scale
10430                     Xcl=0
10440                     Leadlag$="Lagging"
10450                     END IF
10460      IF Flag=1 THEN GOTO 10510
10470     Xco=Xco*Z_scale
10480     Xlo=Xlo*Z_scale
10490     Xci=Xci*Z_scale
10500     Xli=Xli*Z_scale
10510     GINIT
10520     GRAPHICS ON
10530     !
10540     N=1
10550     A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
10560     B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
10570     Dcbus=ABS(SQR(A^2+B^2)/Har(N)*V_scale)
10580     Dcbus_t=Dcbus
10590     FOR N=1 TO 100 STEP 2
10600     Vout(N)=Har(N)*Dcbus
10610     NEXT N
10620     !
10630     !         THE SWITCHING FUNCTION
10640     !
10650     LDIR 90
10660     CSIZE 2.8,.32
10670     VIEWPORT 5,23,8,75
10680     WINDOW Dcbus/2,-Dcbus/2,0,360
10690     AXES Dcbus/4,45,0,0
10700     CLIP OFF
10710     FOR I=-Dcbus/2 TO Dcbus/2 STEP Dcbus/4
10720     MOVE I,0
10730     LORG 8
10740     LABEL PROUND(I,0)
10750     NEXT I
10760     FOR I=90 TO 360 STEP 90
10770     MOVE 0,I
10780     LORG 6
10790     LABEL I
10800     NEXT I
10810     LORG 1
10820     MOVE Dcbus/2,5
```

```
10830       LABEL "A) INVERTER OUTPUT LINE TO NEUTRAL VOLTAGE"
10840       MOVE 0,0
10850                   K=1
10860                   J=Dcbus/2
10870                   FOR I=1 TO 1440
10880                   IF Inter(K)<I/4 THEN
10890                   J=-J
10900                   K=K+1
10910                   END IF
10920                   DRAW J,I/4
10930                   NEXT I
10940       !
10950       !           TEST POINT  OUTPUT LOAD VOLTAGE
10960       !
10970       Dummy=0
10980       Dummy1=0
10990       Max_har=0
11000       FOR N=1 TO 100 STEP 2
11010       IF N MOD (3)=0 THEN GOTO 11110
11020       A=(1-N^2*Xlo/Xco+N*Xlo*(N*Xll-Xcl/N)/(Rl^2+(N*Xll-Xcl/N)^2))
11030       B=(N*Xlo*Rl/(Rl^2+(N*Xll-Xcl/N)^2))
11040       Vload(N)=Vout(N)/SQR(A^2+B^2)
11050       Dummy1=Dummy1+(Vload(N)/SQR(2)*N/Xco)^2
11060       IF N=1 THEN GOTO 11090
11070       Dummy=Dummy+Vload(N)^2
11080       IF Vload(N)>Max_har THEN Max_har=Vload(N)
11090       Vloadphase(N)=-ATN(B/A)
11100       IF A<0 THEN Vloadphase(N)=Vloadphase(N)+180
11110   NEXT N
11120       Thd_lv=ABS(SQR(Dummy)*100/Vload(1))
11130       Iccrms=SQR(Dummy1)
11140       Max_har=ABS(Max_har/Vload(1))*100
11150       !
11160       VIEWPORT 30,48,8,75
11170       WINDOW 200,-200,0,360
11180       CLIP ON
11190       AXES 100,45,0,0
11200       CLIP OFF
11210       FOR I=-200 TO 200 STEP 100
11220       MOVE I,0
11230       LORG 8
11240       LABEL PROUND(I,0)
11250       NEXT I
11260       FOR I=90 TO 360 STEP 90
11270       MOVE 0,I
11280       LORG 6
11290       LABEL I
11300       NEXT I
11310       LORG 1
11320       MOVE 200,0
11330       LABEL "B) LINE-NEUTRAL LOAD VOLTAGE"
11340       MOVE 0,0
11350       FOR Wt=0 TO 360 STEP 1
11360       Dummy=0
11370       FOR I=1 TO 100 STEP 2
11380       IF I MOD (3)=0 THEN GOTO 11390
11390       Dummy=Dummy+Vload(I)*SIN(I*Wt+Vloadphase(I))
11400       NEXT I
```

```
11410       DRAW Dummy,Wt
11420       NEXT Wt
11430       !
11440       !              TEST POINT INVERTER OUTPUT CURRENT
11450       !
11460       Dummy=0
11470       Dummy1=0
11480       FOR N=1 TO 100 STEP 2
11490       IF N MOD (3)=0 THEN GOTO 11570
11500       A=R1*Xco^2/N^2/(R1^2+(N*X11-Xc1/N-Xco/N)^2)
11510       B=N*X1o-(Xco*R1^2/N+Xco/N*(N*X11-Xc1/N)*(N*X11-Xc1/N-Xco/N))/(R1^2+(N
*X11-Xc1/N-Xco/N)^2)
11520       Ioutmag(N)=Vout(N)/SQR(A^2+B^2)
11530       Dummy=Dummy+(Ioutmag(N)/SQR(2))^2
11540       Dummy1=Dummy1+(Ioutmag(N)/SQR(2)*X1o*N)^2
11550       Ioutphase(N)=-ATN(B/A)
11560       IF A<0 THEN Ioutphase(N)=Ioutphase(N)+180
11570       NEXT N
11580       Ilorms=SQR(Dummy)
11590       V_input+COS(Ioutphase(N))*Ioutmag(N)*Har(K)/2
12450       GOTO 12580
12460       END IF
12470       !
12480       IF ((N-K)<0) AND ((N-K) MOD (6)=0) THEN
12490       Cos1(ABS(N-K))=Cos1(ABS(N-K))+COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
12500       Sin1(ABS(N-K))=Sin1(ABS(N-K))+SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
12510       GOTO 12580
12520       END IF
12530       !
12540       IF ((N-K)>0) AND ((N-K) MOD (6)=0) THEN
12550       Cos1(N-K)=Cos1(N-K)+COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
12560       Sin1(N-K)=Sin1(N-K)-SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
12570       END IF
12580       IF ((N+K) MOD (6)=0) AND ((N+K)<55) THEN
12590       Cos1(N+K)=Cos1(N+K)-COS(Ioutphase(N))*Har(K)*Ioutmag(N)/2
12600       Sin1(N+K)=Sin1(N+K)+SIN(Ioutphase(N))*Har(K)*Ioutmag(N)/2
12610       END IF
12620       NEXT K
12630       NEXT N
12640             Dummy=0
12650             Dummy1=0
12660             Dummy2=0
12670             Dummy3=0
12680             FOR N=6 TO 54 STEP 6
12690             Iin(N)=SQR(Cos1(N)^2+Sin1(N)^2)*3
12700             Dummy1=Dummy1+(Iin(N)/SQR(2))^2
12710             Dummy=Dummy+(Iin(N)/(1-N^2*Xli/Xci))^2
12720             Dummy3=Dummy3+(Iin(N)/SQR(2)*Xci/N)^2
12730             Dummy2=Dummy2+(Iin(N)*N*Xli/(1-N^2*Xli/Xci))^2
12740             NEXT N
12750             Dc_input=Dc_input*3
12760             Thd_ddbusi=SQR(Dummy)*100/Dc_input
12770             Xliirms_test=SQR(Dummy/2)+Dc_input
12780             Icirms=SQR(Dummy1)
12790             Thd_inv_inpv=SQR(Dummy2)*100/Ddbus
12800             !
12810       VIEWPORT 105,123,8,75
12820       WINDOW Dc_input*1.5,0,0,360
```

```
12830       CLIP ON
12840       AXES Dc_input*1.5/3,45,0,0
12850       CLIP OFF
12860       FOR I=0 TO Dc_input*1.5 STEP Dc_input*1.5/3
12870       MOVE I,0
12880       LORG 8
12890       LABEL PROUND(I,-1)
12900       NEXT I
12910       FOR I=90 TO 360 STEP 90
12920       MOVE 0,I
12930       LORG 6
12940       LABEL I
12950       NEXT I
12960       LORG 1
12970       MOVE Dc_input*1.5,0
12980       LABEL "E) INPUT INDUCTOR CURRENT"
12990       MOVE 0,0
13000       FOR Wt=0 TO 360 STEP 1
13010       Dummy=0
13020       FOR N=6 TO 100 STEP 6
13030       Dummy=Dummy+Cos1(N)/(1-N^2*Xli/Xci)*COS(N*Wt)+Sin1(N)/(1-N^2*Xli/Xci)
*SIN(N*Wt)
13040       NEXT N                                          ! GIVING BATTERY CURRENT
13050       DRAW Dummy+Dc_input,Wt
13060       NEXT Wt
13070       !
13080       Li=Xli/2/PI/60
13090       Lo=Xlo/2/PI/60
13100       Ci=1/Xci/2/PI/60
13110       Co=1/Xco/2/PI/60
13120       VIEWPORT 0,100,0,130
13130       WINDOW 0,100,0,100
13140       CLIP OFF
13150       MOVE 5,88
13160       LORG 5
13170       CSIZE 3.0,.31
13180       LABEL "WORST CASE SPECIFICATIONS"
13190       MOVE 6,77
13200       DRAW 6,100
13210       MOVE 8,88
13220       LABEL "Output Kva=";PROUND(Kva,-2);"KVA"
13230       LABEL "Load voltage THD <5%"
13240       LABEL "Max harmonic amp <3%"
13250       LABEL "Damping factor at pf=1 =.707"
13260       LABEL "Inverter voltage THD <5.0%"
13270       LABEL "DC BUS line current THD<10%"
13280       LABEL "Min dc bus volts=";PROUND(Dcbusmin*V_scale,0);"V"
13290       LABEL "Max dc bus volts=";PROUND(Dcbusmax*V_scale,0);"V"
13300       LABEL "Ave switch curr=";PROUND(Iswave*I_scale,-2);"A"
13310       LABEL "Output capacitor=";PROUND(Co*1000000,-1);"uF"
13320       LABEL "rms voltage=";PROUND(Xcovrms*V_scale,0);"V"
13330       LABEL "rms current=";PROUND(Xcoirms*I_scale,-2);"A"
13340       LABEL "Output inductor=";PROUND(Lo*1000,-2);"mH"
13350       LABEL "rms voltage=";PROUND(Xlovrms*V_scale,-2);"V"
13360       LABEL "rms current=";PROUND(Xloirms*I_scale,-2);"A"
13370       LABEL "Input capacitor=";PROUND(Ci*1000000,-1);"uF"
13380       LABEL "rms voltage=";PROUND(Xcivrms*V_scale,0);"V"
13390       LABEL "rms current=";PROUND(Xciirms*I_scale,-2);"A"
```

```
13400       LABEL "Input inductor=";PROUND(Li*1000,-2);"mH"
13410       LABEL "rms voltage=";PROUND(Xlivrms*V_scale,-1);"V"
13420       LABEL "rms current=";PROUND(Xliirms*I_scale,-2);"A"
13430       LABEL
13440       LABEL "Test point data"
13450       LABEL "LOAD PF=";PROUND(Pf,-2);Leadlag$
13460       LABEL "Load Voltage THD=";PROUND(Thd_lv,-2);"%"
13470       LABEL "Max Harmonic    =";PROUND(Max_har,-2);"%"
13480       LABEL "Output filter rms"
13490       LABEL "capacitor current=";PROUND(Icorms,-2);"A"
13500       LABEL "Output filter rms"
13510       LABEL "inductor current=";PROUND(Ilorms,-2);"A"
13520       LABEL "Output filter rms"
13530       LABEL "inductor voltage=";PROUND(Vlorms,-2);"V"
13540       LABEL "Ave switch curr =";PROUND(Iswavet,-2);"A"
13550       LABEL "Rms switch curr =";PROUND(Iswrmst,-2);"A"
13560       LABEL "DC bus voltage  =";PROUND(Dcbus,0);"V"
13570       LABEL "Input filter inductor"
13580       LABEL "current THD   =";PROUND(Thd_dcbusi,-2);"%"
13590       LABEL " & rms current=";PROUND(Xliirms_test,-2);"A"
13600       LABEL "Input filter rms"
13610       LABEL "capacitor current=";PROUND(Icirms,-2);"A"
13620       LABEL "inverter input"
13630       LABEL "voltage THD     =";PROUND(Thd_inv_inpv,-2);"%"
13640       ON KEY 4 LABEL "HARDCOPY" GOTO Hard
13650       ON KEY 3 LABEL "HF LINK RATINGS" GOTO Hflink
13660       GOTO 13640
13670 Hard:     !
13680           GINIT
13690           GRAPHICS ON
13700           PLOTTER IS 705,"HPGL"
13710           OUTPUT 705;"VS5"
13720           GOTO 13630
13730 Hflink:       !
13740               !
13750               !*********************************************************
13760               GRAPHICS OFF
13770               OFF KEY
13780           INPUT "PLEASE INPUT THE NOMINAL BATTERY VOLTAGE",Enom
13790           Dcbus=Dcbus_t ! SAVED FROM INVERTER SECTION USER SPECIFIED LOAD
13800           Tran_ratio=.8*Enom/(Dcbusmax*V_scale)  !  TRANSFORMER RATIO AS ?
:1
13810           IF Hfpass=1 THEN GOTO 13960
13820           Xchf=Xchf*Z_scale*Tran_ratio^2
13830           Xlhf=Xlhf*Z_scale*Tran_ratio^2
13840           Chf=1/Xchf/2/60/PI
13850           Lhf=Xlhf/2/PI/60
13860           Diodeiave=Diodeiave*I_scale
13870           Diodevmax=Diodevmax*V_scale
13880           Swhfiave=Swhfiave*I_scale/Tran_ratio
13890           Xlhfirms=Xlhfirms*I_scale/Tran_ratio
13900           Xlhfvrms=Xlhfvrms*V_scale*Tran_ratio
13910           Xchfvrms=Xchfvrms*V_scale*Tran_ratio
13920           Xchfirms=Xchfirms*I_scale/Tran_ratio
13930           Tranirms=Tranirms*I_scale/Tran_ratio
13940           Tranvrms=Tranvrms*V_scale*Tran_ratio
13950           Hfpass=1
13960           INPUT "INPUT THE BATTERY TEST VOLTAGE SCALING FACTOR.8Enom<E<1.1
```

```
Enom",Fac
13970           E_test=Fac*Enom
13980  Dc_input=KVa*1000*Pf/Dcbus  !USING EQUAL REAL POWER TO SOLVE DC COMPONENT
13990           Duty=Dcbus/(E_test/Enom)/(Dcbusmax*V_scale)*.8
14000           Up=(180-(180*Duty))/2
14010           Down=180-Up
14020           !
14030           ! DIODES
14040           !
14050            Diodevmax_t=E_test/Tran_ratio
14060            Diodeiave_t=Xliirms_test/2
14070            !
14080            ! TRANSFORMER RATINGS
14090            !
14100            ! FROM PRIMARY SIDE
14110            Dummy=0
14120            Dummy1=0
14130               FOR N=1 TO 100 STEP 2
14140               Hfhar(N)=2/N/PI*(-COS(Down*N)+COS(Up*N))
14150               Dummy=Dummy+(E_test*Hfhar(N)/SQR(2))^2
14160               Dummy1=Dummy1+(Dc_input/Duty/Tran_ratio*Hfhar(N)/SQR(2))^2
14170               NEXT N
14180               Tranvrms_t=SQR(Dummy)
14190               Traniirms_t=SQR(Dummy1)
14200               Tranva_t=Tranvrms_t*Traniirms_t
14210               !
14220               !
14230               !  SWITCH RATINGS
14240               !
14250                Swhfiave_t=Dc_input*.5/Tran_ratio*Duty
14260                !
14270                ! FILTER RATINGS
14280                !
14290             Dummy=0
14300             Dummy1=0
14310             Dummy2=0
14320             FOR N=1 TO 100 STEP 1
14330             RAD
14340          An=(Dc_input/Tran_ratio)/N/PI*(1-COS(2*PI*Duty*N))
14350          Bn=(Dc_input/Tran_ratio)/N/PI*(SIN(2*PI*Duty*N))
14360              DEG
14370              Dummy=Dummy+(SQR((An^2+Bn^2))/SQR(2))^2
14380          Dummy1=Dummy1+(SQR((An^2+Bn^2))/SQR(2)*Xchf/(N*High_freq*2/60))^2
14390          Dummy2=Dummy2+(SQR(An^2+Bn^2)/(1-(N*High_freq*2/60)^2*Xlhf/Xchf))^2
14400              NEXT N
14410              Xchfirms_t=SQR(Dummy)
14420              Xlhfvrms_t=SQR(Dummy1)
14430              Ibat_thd=SQR(Dummy2)*100/(Swhfiave_t*2)
14440              Xlhfirms_t=Swhfiave_t*2
14450              Xchfvrms_t=E_test
14460              !
14470         PRINT " HF Link Worst Case Ratings"
14480         PRINT "-------------------------------"
14490         PRINT "BATTERY CURRENT THD<5%"
14500         PRINT "HF INVERTER INPUT VOLTAGE THD<2.5%"
14510         PRINT "TRANSFORMER RATIO=";PROUND(Tran_ratio,-2);":1"
14520         PRINT "HF INVERTER SWITCHING FREQUENCY=";High_freq;"hz"
14530         PRINT "MAX DIODE VOLTAGE=";PROUND(Diodevmax,-2);"V"
```

```
14540       PRINT "AVE DIODE CURRENT=";PROUND(Diodeiave,-2);"A"
14550       PRINT "RMS PRIMARY TRANSFORMER VOLTAGE=";PROUND(Tranvrms,-2);"V"
14560       PRINT "RMS PRIMARY TRANSFORMER CURRENT=";PROUND(Tranirms,-2);"A"
14570       PRINT "HF INVERTER SWITCH VOLTAGE=";PROUND(Enom*1.1,-2);"V"
14580       PRINT "AVE HF INVERTER SWITCH CURRENT =";PROUND(Swhfiave,-2);"A"
14590       PRINT
14600       PRINT "INPUT FILTER RATINGS"
14610       PRINT "INDUCTOR=",PROUND(Ihf*1000000,-2);"uH    Irms=";PROUND(Xlhfirms
,-2);"A   Vrms=";PROUND(Xlhfvrms,-2);"V"
14620       PRINT "CAPACITOR",PROUND(Chf*1000000,-2);"uF    Irms=";PROUND(Xchfirms
,-2);"A   Vrms=";PROUND(Xchfvrms,-2);"V"
14630       PRINT
14640       PRINT "HF Link Ratings at test point"
14650       PRINT "-- ----------------------------"
14660       PRINT "TEST VOLTAGE=";PROUND(E_test,-1);"/";PROUND(Enom,-1);"->";"RAT
IO=";PROUND(E_test/Enom,-3)
14670       PRINT "PEAK DIODE VOLTAGE=";PROUND(Diodevmax_t,-2);"V"
14680       PRINT "AVE DIODE CURRENT=";PROUND(Diodeiave_t,-2);"A"
14690       PRINT "RMS PRIMARY TRANSFORMER VOLTAGE=";PROUND(Tranvrms_t,-2);"V"
14700       PRINT "RMS PRIMARY TRANSFORMER CURRENT=";PROUND(Tranirms_t,-2);"A"
14710       PRINT "AVE HF INVERTER SWITCH CURRENT =";PROUND(Swhfiave_t,-2);"A"
14720       PRINT "BATTERY CURRENT THD=";PROUND(Ibat_thd,-2);"%"
14730       PRINT
14740       PRINT "INPUT FILTER RATINGS"
14750       PRINT "INDUCTOR=","Irms=";PROUND(Xlhfirms_t,-2);"A","   Vrms=";PROUND
(Xlhfvrms_t,-2);"V"
14760       PRINT "CAPACITOR=","Irms=";PROUND(Xchfirms_t,-2);"A","   Vrms=";PROUN
D(Xchfvrms_t,-2);"V"
14770       PRINTER IS 1
14780       ON KEY 1 LABEL "CHANGE BAT V" GOTO Change_test
14790       ON KEY 2 LABEL "PRINTOUT" GOTO Printout_1
14800       ON KEY 3 LABEL "CHANGE PF" GOTO Change_pf
14810       GOTO 14780
14820 Change_test:      !
14830       OFF KEY
14840       PRINT CHR$(12)
14850       PRINT "BAT TEST VOLTAGE IS NOW";E_test;". THIS IS ";Fac;"*NOMINAL VOL
TAGE"
14860       GOTO 13960
14870 Printout_1:       !
14880                   PRINTER IS 701
14890                   GOTO 14470
14900 Change_pf:!
14910             PLOTTER IS 3,"INTERNAL"
14920             Flag=1
14930             OFF KEY
14940             PRINT CHR$(12)
14950             GOTO 10210
14960                  END
```

APPENDIX A2

SEMICONDUCTOR EVALUATION

1) Darlington

The darlington power semiconductor has traditionally been accepted as a rugged, fully controlled (on/off) electronic valve. Although darlingtons are available well into the required voltage and current range of the proposed UPS design, a significant drawback was seen in the storage time. Approaching 12 μsec in a 25 μsec pulse, [20khz switching environment] storage time reflected the undesirable feature of duty cycle based on load. Moreover, if a short circuit should be experienced the storage time may be extended causing overlap and cross conduction. The general solution is to provide dead times (see chapter 3.4.5.3) compensating for the maximum estimated storage times. This is unacceptable since 12 μsec of a 25 μsec pulse eliminated for storage would double switch currents for equivalent though-put power.

The storage time problem can be alleviated with special drive strategies. In particular, an anti saturation diode or 'Bakers clamp' can be used. This diodc effectively connected from the base to collector (anode and cathode respectively) of the power darlington prevents the base voltage from exceeding a diode voltage drop above the collector voltage. This holds the darlington in the quasi saturation region. Without deep saturation before turn off, the darlington attains its blocking state more rapidly resulting in less storage time.

Several iterations of drive design were pursued until a satisfactory result was achieved.

Figure FA2.1 shows the drive circuit utilized. The features of the circuit include

1) The required on/off power of the darlington is difficult to pass through a pulse transformer, therefore secondary side split rail power is used.

2) Opto isolation is obtained via the HP2602.

3) Anti saturation diode acting as a 'bakers clamp'.

4) Active turn off and passive turn on of the main power semiconductor emphasizing turn off speed.

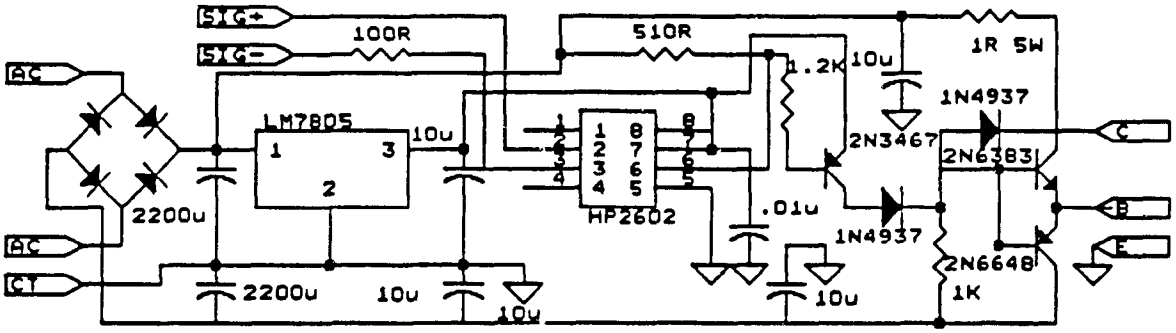

Figure FA2.1 Darlington base drive circuit

Experimental verification of storage time reduction were obtained for Power Transistor (Toshiba 100 & 300 amp 500 V) QM100DY-H and QM300HA-24. These are shown in table TA2.1 and table TA2.2.

Amps	Without antisaturation diode ±10V		+10V -20V		With antisaturation diode ±10V		+10V -20V	
	Tμs	Amps	Tμs	Amps	Tμs	Amps	Tμs	Amps
20	3.2	-6	2.2	-11	1.0	-5.0	.9	-9
40	4.0	-6	2.4	-11.2	1.2	-5.2	1.0	-9
60	4.3	-6	2.7	-11.5	1.7	-5.9	1.2	-10.5
80	4.4	-6	3.0	-11.5	2.1	-6.0	1.6	-11.2
100	4.5	-6	3.1	-11.5	2.5	-6.0	1.8	-11.8

Table TA2.1 Storage time switching characteristics of QM 100DY-H

Amps	Without antisaturation diode ±10V		+10V -20V		With antisaturation diode ±10V		+10V -20V	
	Tμs	Amps	Tμs	Amps	Tμs	Amps	Tμs	Amps
40	6.0	-6.5	4.0	-12.5	3.0	-7.0	2.0	-13.0
80	8.0	-6.5	5.6	-13.0	4.7	-7.0	3.4	-13.2
120	9.5	-6.5	6.6	-13.5	7.0	-7.0	5.2	-13.5
160	10.0	-6.5	7.0	-13.5	7.8	-7.0	6.2	-13.5
180	10.3	-6.5	7.4	-13.5	8.4	-7.0	7.0	-13.5

Table TA2.2 Storage time switching characteristics of QM 300HA-24

Figure FA2.2 shows the test circuit configuration.

Finally, figure FA2.3 shows base drive current modification required to safely accommodate the -20 volt reverse bias gate voltage.

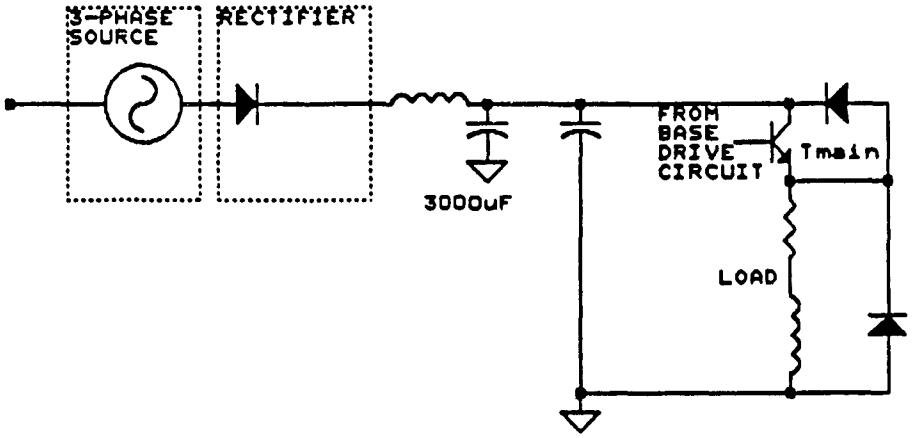

Figure FA2.2 Storage time test circuit

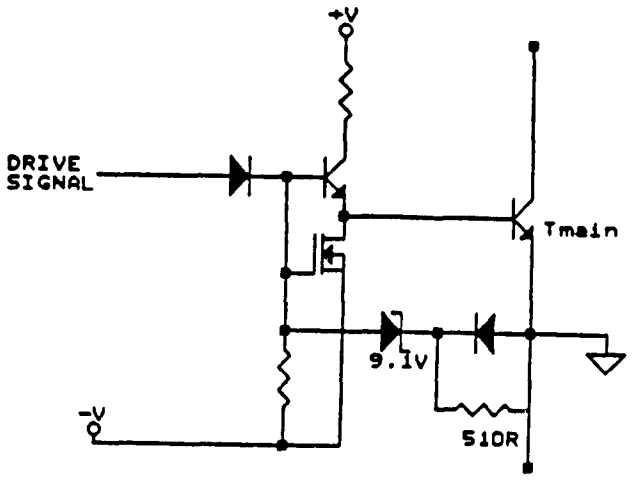

Figure FA2.3 Base drive modification accommodating a -20 V reverse potential voltage

From table TA2.1 and TA2.2, the minimum storage time values are obtained under maximum reverse bias conditions and with antisaturation diode present. It is also noted that storage times were found to be independent of transistor blocking voltage levels.

Minimal storage time at 100 Amp was found to be approximately 2μsec. With safety margin this transpires into a 3μsec deadtime which at 20 khz operating frequency reduces maximum duty cycle by 12%. This is seen as a highly undesirable feature. A second drawback is the relatively large base drive power consumption.

2) MOSFET

Although MOSFETS have traditionally dominated at low power levels recent parallel dies in appropriate packages have enabled their competitive use at medium powers. Their main drawback is the conduction losses at high blocking voltages in excess of 500 volts. For the UPS power train proposed here voltages remain below this level and consequently conduction power loss is not

serious. However, the high current ratings of the HF link cannot be handled by a standard single package module. With present technology and standard low cost parts, two MOSFETS in parallel for each high frequency link switch are required.

The drive required for MOSFET activation is simplified over the darlington and is shown in figure FA2.4.

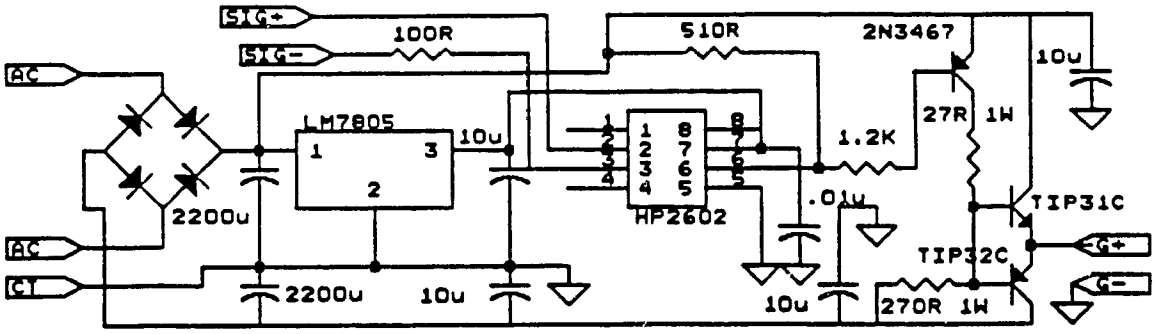

Figure F2.4 MOSFET base drive circuit

In general, other than requiring parallel power devices the MOSFETS showed no detrimental effects. Turn off time was roughly 200 times faster than the darlingtons eliminating the large deadtimes required. Further effective losses (conduction and switching) were equivalent to the darlingtons (in conjunction with the antisaturation diodes).

Current fall times were in the order of 100 nsec resulting in a turn off power loss of

$$P_{LOSS} = .5 \cdot (V_{DCBUS} \cdot I_{COM} \cdot T_{OFF} \cdot F_{SW}) \qquad \text{A2.1}$$

where V_{DCBUS} = blocking voltage

I_{COM} = turn off current level

T_{OFF} = current fall time

F_{SW} = switching frequency

Using the data of chapter 3.4 equation A2.1 yields

$$P_{LOSS} = .5 \cdot (219.6 \cdot 73.62 \cdot 10^{-7} \cdot 20000)$$

$$= 16.16 \text{ WATT/SWITCH}$$

Since each switch contains two packages

$$P_{LOSS} = 8.08 \text{ WATT/MODULE}$$

3) IGBT

The insulated gate bipolar transistor (IGBT) has emerged recently to address a medium voltage (500-1000V), medium current (30-300A) market. The semiconductor retains the ruggedness of high voltage darlingtons yet is accompanied with lower storage time. Reducing the storage time of the darlington to .5μsec is a very attractive feature. Moreover, the IGBT input appears as a MOSFET to its driver which is another desirable feature. This implies that the same drive utilized for MOSFET semiconductors can be used for IGBTs as well (figure FA2.4).

Although storage times were significantly reduced the current fall time during turn off was approximately .5μsec. When compared to the MOSFET or darlington this created a significantly larger amount of switching loss. The IGBT losses due only to switching characteristics are given by equation A2.1. With a 1μsec fall time the equation yields

$$P_{LOSS} = 80 \text{ WATT/SWITCH}$$

This is a tremendous burden on efficiency, cooling and semiconductor reliability. It should be noted that the switching power loss of the IGBT is roughly five times that of MOSFETS evaluated earlier.

4) Gate turn off thyristor (GTO)

The GTO is the most rugged of the semiconductors evaluated withstanding

large current surges. Two distinct problems were expected with the GTO. Firstly, typical combined turn off and turn on time is in the range of 12μsec. Secondly, a large reverse base current of typically 50% anode current is required to extinguish the semiconductor current flow.

A relatively complex base drive was developed to alleviate these problems. The test circuit is shown in figure FA2.5 while the drive schematic is shown in figure FA2.6.

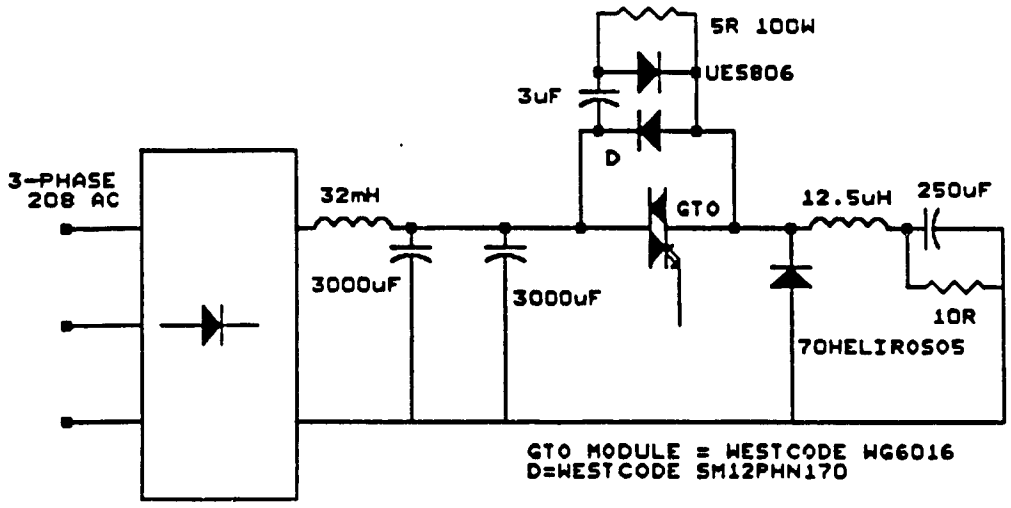

Figure FA2.5 GTO test circuit

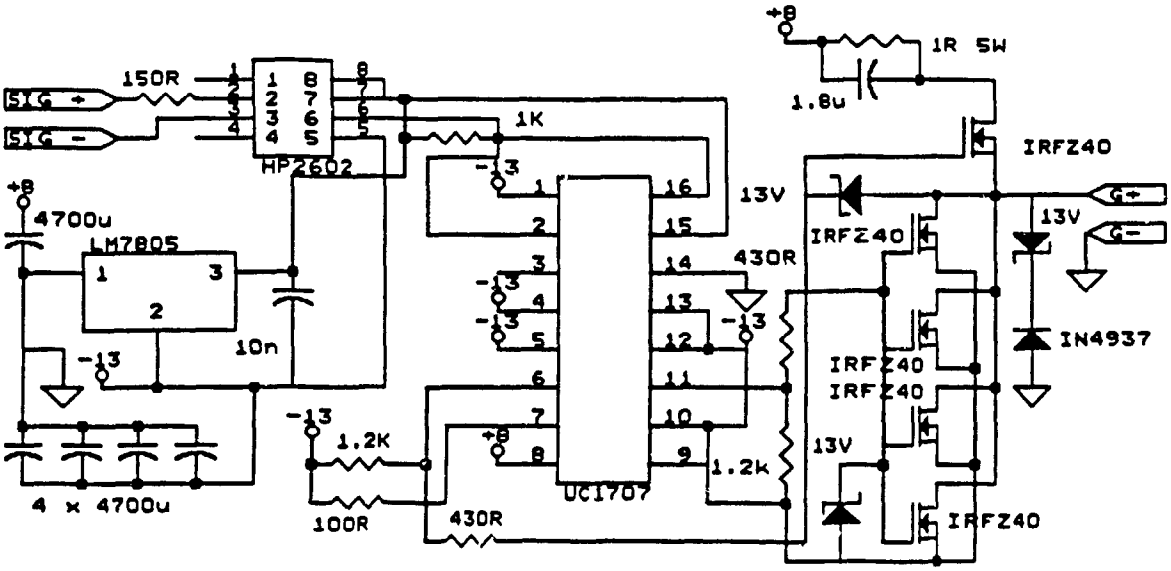

Figure FA2.6 GTO Base drive

The central component of the drive is IC UC1707 which has excellent driving capabilities and built in protection functions. Further, the drive incorporates an extremely fast turn off circuitry with large gain and low resistance. 4 x IRFZ40 MOSFETs are paralleled providing a theoretical current capacity of 2000 amps. Experimental results shown in figure FA2.7 reveals that the drive successfully commutates 200 amps of anode current in a total time of 4μsec. Further, figure FA2.8 shows V_{SWPK} of the GTO during turn off revealing safe dv/dt operation.

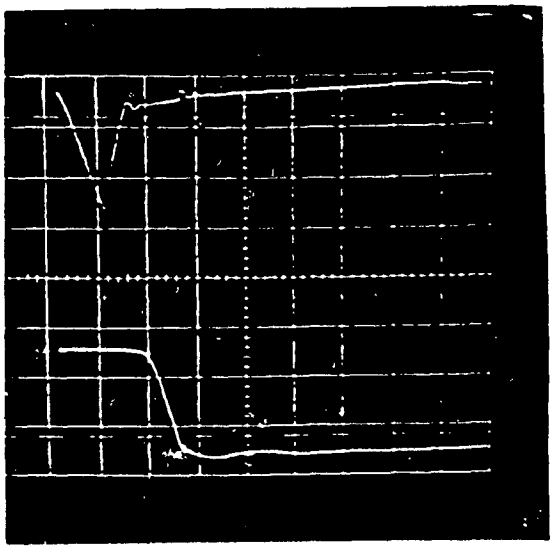

Figure FA2.7 Experimental GTO turn off base and anode current
TOP: GTO base current (25 amps/div 2μs/div)
BOTTOM: GTO anode current (100 amps/div 2μs/div)

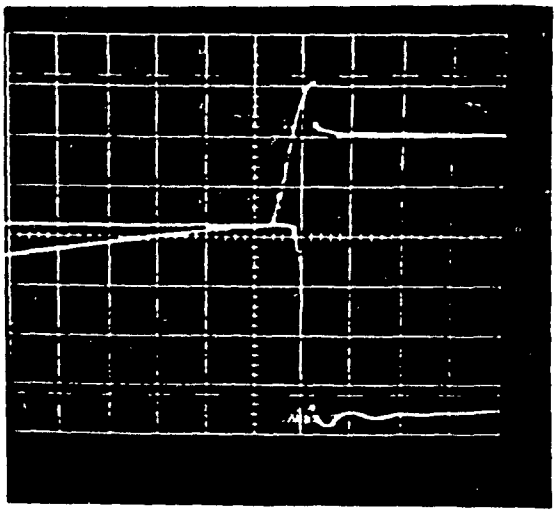

Figure FA2.8 Experimental GTO turn off anode current and V_{AK}
TOP: GTO V_{AK} voltage (100 volts/div 4μs/div)
BOTTOM: GTO anode current (100 amps/div 4μs/div)

Although the drive designed has sufficient strength to successfully commutate the GTO, attempts to speed up the 4μsec turn off time resulted in

GTO destruction. This dictated that the switching speeds cannot be dramatically improved to meet the high frequency link requirements. Moreover, the ruggedness of the GTO is partially overshadowed by the complex base drive requirement.