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HIGH PERFORMANCE SOLID-STATE VAR COMPENSATORS

Luis Morán

A Thesis
in
The Department
of
Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy at
Concordia University
Montréal, Québec, Canada

January 1990

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ABSTRACT

HIGH PERFORMANCE SOLID-STATE VAR COMPENSATORS

Luis Morán T.
Concordia University, 1990

With the continuous proliferation of nonlinear types of load, the requirements imposed by utilities on power factor and harmonic pollution are becoming more rigorous. These requirements involve precise and continuous reactive power control with fast response times, avoidance of line current harmonic generation and avoidance of resonances created by peripheral low frequency current sources. To satisfy the above criteria, solid-state var compensators using force-commutated converters have been developed and are gradually gaining recognition from the static converter industry and the users of electric power.

High performance solid-state var compensators using three-phase PWM current-source and voltage-source inverters are proposed, analyzed and experimentally verified in this thesis. The proposed var compensator topologies present improved performance characteristics in terms of the size of the reactive components, generated current harmonic distortion, and control simplicity and flexibility. The described configurations are based on PWM current-source inverters connected to a dc reactor and PWM voltage-source inverters connected to a dc capacitor.

There are four main features of the proposed topologies. First, by applying properly selected PWM techniques it is shown that the size of the var compensators reactive components can be reduced significantly. Secondly, to improve system transient response, a current regulated synchronous
compensator which operates at a constant switching frequency is presented. The advantages of this scheme include fast response time and reduced switching stresses. Third, control system simplifications are achieved in a power factor compensator that requires minimum sensing (line and converter voltages only) and no reactive power calculations. Finally, this system also reduces any line current harmonics generated by nonlinear loads and compensates for voltage unbalance in the ac source. Further, a systematic and comprehensive design method for the power circuit and the control system is developed for each of the proposed schemes. Design and implementation are confirmed by simulation. The feasibility of each scheme, and the performance evaluation during steady-state and transient operating conditions is verified experimentally.
ACKNOWLEDGEMENTS

I wish to express my gratitude to Dr. P. D. Ziogas and Dr. G. Joos for their valuable advice and support during the course of this study.

I want to thank "Odeplan" of Chile for the financial assistance which enable me to undertake this research.

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Special gratitude to my wife Marisa for her understanding and encouragement during the preparation of this thesis.
# TABLE OF CONTENTS

Abstract ......................................................... iii
Acknowledgements ........................................... v
Table of Contents ............................................ vi
List of Figures ............................................... xi
List of Tables ................................................. xviii
List of Acronyms ............................................. xix
List of Principal Symbols ................................. xx

## CHAPTER 1. INTRODUCTION

1.1 Introduction ............................................. 1

1.2 General Information on var Compensators ................... 2
  1.2.1 Fixed or mechanically switched capacitors ............... 3
  1.2.2 Synchronous condensers ................................ 4
  1.2.3 Static var compensators ................................ 4
    1.2.3.1 Saturated reactors .................................. 5
    1.2.3.2 Thyristor-switched capacitors ...................... 7
    1.2.3.3 Thyristor-controlled reactor ....................... 8
    1.2.3.4 Combined TSC and TCR system ...................... 9
  1.2.4 Solid-state var compensators .......................... 10

1.3 Review of Previous Work ................................ 13
  1.3.1 Solid-State var compensators .......................... 15
  1.3.2 Active power filters .................................. 18

1.4 Scope and Contributions ................................ 20
1.5 Summary ................................................................................. 21

CHAPTER 2 CURRENT SOURCE SOLID-STATE VAR COMPENSATORS
2.1 Introduction ............................................................................. 24
2.2 Principles of Operation .......................................................... 25
2.3 System Description ................................................................. 26
  2.3.1 Power circuit description .................................................. 28
  2.3.2 Reactive power control circuit description ....................... 28
  2.3.3 PWM switching pattern description .................................. 30
2.4 Power Circuit Design ............................................................. 31
  2.4.1 Input filter design ........................................................... 33
  2.4.2 Semiconductor switch ratings .......................................... 37
  2.4.3 DC Reactor design ......................................................... 39
2.5 Reactive Power Control Unit Design ......................................... 42
  2.5.1 DC current control circuit design ..................................... 42
  2.5.2 Gating signals generator design ....................................... 43
2.6 Simulated PWM Inverter results ............................................. 44
2.7 Design Example ....................................................................... 45
  2.7.1 Power circuit ................................................................. 45
  2.7.2 DC current control ......................................................... 48
  2.7.3 $\alpha$ phase-shift control circuit ....................................... 49
2.8 Experimental Results ........................................................... 49
  2.8.1 Steady-state response ..................................................... 49
  2.8.2 Dynamic response ......................................................... 50
2.9 Conclusion ............................................................................. 50
CHAPTER 3 SYNCHRONOUS SOLID-STATE VAR COMPENSATORS

3.1 Introduction ........................................... 54

3.2 Principles of Operation .................................. 55

3.3 System Description ...................................... 58
  3.3.1 Power circuit description ............................. 58
  3.3.2 Control circuit description ........................... 58
  3.3.3 PWM switching pattern description .................. 60

3.4 Power Circuit Design .................................... 62
  3.4.1 Design of the synchronous link reactor ............... 64
  3.4.2 Semiconductor switch ratings .......................... 67
  3.4.3 DC capacitor design .................................. 69

3.5 Design of the δ Control Unit ............................ 71

3.6 Influence of the Compensator Parameters ................. 76

3.7 Analysis for Unbalance Voltage Source Condition .......... 77
  3.7.1 Input and output waveforms analysis .................. 77
  3.7.2 System design considerations .......................... 85

3.8 Simulated PWM Inverter Results ......................... 87
  3.8.1 Simulated waveforms for balanced ac mains voltages .... 87
  3.8.2 Simulated waveforms for unbalanced ac mains voltages .... 90

3.9 Design Example ......................................... 90
  3.9.1 Power Circuit ....................................... 90
  3.9.2 δ Control Unit ...................................... 93

3.10 Experimental Results ................................... 94
  3.10.1 Experimental results for balanced ac mains voltages .... 94
  3.10.2 Experimental results for unbalanced ac mains voltages .... 96
  3.10.3 Dynamic response .................................. 96
CHAPTER 4 CURRENT CONTROLLED SYNCHRONOUS VAR COMPENSATORS

4.1 Introduction .......................................... 102
4.2 Principles of Operation .................................. 103
  4.2.1 Current control unit ................................ 103
  4.2.2 Voltage control unit ................................ 103
  4.2.3 Gating signal generator ............................. 105
4.3 Power Circuit Design ..................................... 108
  4.3.1 Design of the synchronous link reactor .......... 109
  4.3.2 Design of the dc capacitor ........................ 111
4.4 Control Circuit Design ................................... 113
  4.4.1 Voltage control loop ............................... 113
  4.4.2 Current control loop ............................... 113
  4.4.3 Gating signal generator ............................ 114
4.5 Design Example ......................................... 114
  4.5.1 Power circuit ..................................... 114
  4.5.2 Control circuit ................................... 115
4.6 Simulated Results ....................................... 116
  4.6.1 Steady-state simulated waveforms ................. 116
  4.6.2 Simulated transient waveforms .................... 117
4.7 Conclusions ........................................... 123

CHAPTER 5 A POWER FACTOR COMPENSATOR AND HARMONIC SUPPRESSOR SYSTEM

5.1 Introduction ........................................... 124
5.2 Principles of Operation ................................ 125
5.2.1 Power factor compensation ........................................ 126
5.2.2 Voltage regulation .................................................. 129
5.2.3 Harmonic compensation ........................................... 130
5.2.4 Unbalanced voltage compensation ......................... 130
5.3 System Design Criteria ................................................ 131
5.4 Simulated Results ...................................................... 135
  5.4.1 Simulated waveforms for linear load compensation ....... 135
  5.4.2 Simulated waveforms for nonlinear load compensation ... 135
5.5 Experimental results .................................................. 138
  5.5.1 Experimental results for linear load compensation ....... 140
  5.5.2 Experimental results for nonlinear load compensation ... 140
  5.5.3 Experimental results for voltage compensation ............. 142
5.6 Conclusion .............................................................. 146

CHAPTER 6 CONCLUSIONS
6.1 Conclusions ........................................................... 147
6.2 Suggestions for Future Work ........................................ 149

REFERENCES .................................................................. 151

APPENDIX A TRANSFER FUNCTION OF THE SYNCHRONOUS SOLID-STATE
COMPENSATOR ................................................................ 158
APPENDIX B THE CHARACTERISTIC [A]-MATRIX OF THE SSVC SYSTEM 168
APPENDIX C LOAD FILTER DESIGN ....................................... 170
<table>
<thead>
<tr>
<th>Fig.</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>The saturated reactor compensator configuration</td>
<td>6</td>
</tr>
<tr>
<td>1.2</td>
<td>The thyristor-switched capacitor configuration</td>
<td>8</td>
</tr>
<tr>
<td>1.3</td>
<td>The thyristor-controlled reactor configuration</td>
<td>9</td>
</tr>
<tr>
<td>1.4</td>
<td>The solid-state current-source var compensator configuration</td>
<td>12</td>
</tr>
<tr>
<td>1.5</td>
<td>The solid-state voltage-source var compensator configuration</td>
<td>12</td>
</tr>
<tr>
<td>2.1</td>
<td>Principle of reactive current compensation</td>
<td>27</td>
</tr>
<tr>
<td>2.2</td>
<td>The current-source var compensator configuration</td>
<td></td>
</tr>
<tr>
<td>2.3</td>
<td>Closed loop control of compensating current</td>
<td>29</td>
</tr>
<tr>
<td>2.4</td>
<td>The reactive power control circuit</td>
<td>29</td>
</tr>
<tr>
<td>2.5</td>
<td>Inverter switching pattern and associated switching angles</td>
<td>32</td>
</tr>
<tr>
<td>2.6</td>
<td>Analytical model for the LC filter. (a) Single-phase equivalent LC filter circuit</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>(b) Single-phase equivalent circuit at fundamental frequency. (c) Phasor diagram for leading power factor</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>(d) Phasor diagram for lagging power factor</td>
<td></td>
</tr>
<tr>
<td>2.7</td>
<td>Single-phase equivalent LC filter circuit for the harmonics</td>
<td>36</td>
</tr>
<tr>
<td>2.8</td>
<td>The frequency response of the LC filter</td>
<td>38</td>
</tr>
<tr>
<td>2.9</td>
<td>The block-diagram of dc current closed loop control</td>
<td>43</td>
</tr>
<tr>
<td>2.10</td>
<td>Inverter simulated waveforms for capacitive mode operation with PWM scheme (Xc=7.27 pu and Xi=0.068)</td>
<td>46</td>
</tr>
</tbody>
</table>
Fig. 2.11 Inverter simulated waveforms for inductive mode of operation with PWM scheme (Xc=7.27 pu and Xi=0.068 pu)

Fig. 2.12 The proportional controller

Fig. 2.13 Experimental voltage and current waveforms for capacitive var compensation

Fig. 2.14 Experimental voltage and current waveforms for inductive var compensation

Fig. 2.15 Response of current-source var compensator to biased sinusoidal-wave var reference. (a) Var reference. (b) DC current \( I_{dc} \)

Fig. 3.1 (a) Single phase equivalent circuit of SSVC at fundamental frequency. (b) Phasor diagram for leading power factor. (c) Phasor diagram for lagging power factor

Fig. 3.2 Synchronous solid-state var compensator configuration

Fig. 3.3 Closed loop control of compensating current for SSVC

Fig. 3.4 Block diagram of the \( \delta \) phase-shift control

Fig. 3.5 Xi versus Np plots with various THDI values for modulation index of 1.12

Fig. 3.6 Voltage-source inverter PWM switching pattern for modulation index 1.12 and associated switching angles
Fig. 3.7 Voltage-source inverter switching pattern with different modulation index values (Np = 11) 63

Fig. 3.8 Analytical model of output filter for leading var compensation. (a) Single phase equivalent output filter circuit at fundamental frequency. (b) Single phase equivalent output filter circuit for harmonics 64

Fig. 3.9 Bode diagram of the SSVC open loop frequency response. (a) Magnitude response. (b) Phase response 74

Fig. 3.10 The block diagram of the SSVC control system 75

Fig. 3.11 The PI controller 76

Fig. 3.12 Root locus for increasing values of the dc capacitor 78

Fig. 3.13 Root locus for increasing values of the synchronous link inductor 79

Fig. 3.14 Root locus for increasing values of the damping resistance 80

Fig. 3.15 Three-phase equivalent circuit for voltage unbalanced analysis 82

Fig. 3.16 Three-phase equivalent circuit for negative sequence components 82

Fig. 3.17 DC capacitor reactance Xc versus synchronous reactor Xi plots 86

Fig. 3.18 THDi versus synchronous reactor (Xi) plots 86

Fig. 3.19 PWM voltage-source inverter simulated waveforms for 88
leading var compensation (\(X_l = 0.38\) pu and \(X_c = 5.41\) pu)

Fig. 3.20 PWM voltage-source inverter simulated waveforms for lagging var compensation (\(X_l = 0.38\) pu and \(X_c = 5.41\) pu)

Fig. 3.21 PWM voltage-source inverter simulated waveforms for leading var compensation (\(X_l = 0.38\) pu and \(X_c = 5.41\) pu)

Fig. 3.22 PWM voltage-source inverter simulated waveforms for leading var compensation and 5% unbalanced ac source voltage (\(X_l = 0.43\) pu and \(X_c = 3.6\) pu)

Fig. 3.23 Bode plot of the SSVC open loop frequency response

Fig. 3.24 Experimental SSVC open loop frequency response

Fig. 3.25 Experimental inverter voltage and current waveforms for leading var compensation and balanced ac source voltages

Fig. 3.26 Experimental inverter voltage and current waveforms for lagging var compensation and balanced ac source voltages

Fig. 3.27 Experimental inverter voltage and current waveforms for leading var compensation and 5% unbalanced ac source voltage (\(X_l = 0.38\) pu and \(X_c = 5.4\) pu)

Fig. 3.28 Experimental inverter voltage and current waveforms for leading var compensation and 5% unbalanced ac source voltage (\(X_l = 0.43\) pu and \(X_c = 3.6\) pu)

Fig. 3.29 Experimental open loop system response for step
change in the phase-shift angle $\delta$. (a) DC voltage response. (b) Inverter ac current response

Fig. 3.30 Experimental dc voltage closed loop response for a step change in the load power factor. (a) DC voltage response for a step change from leading to lagging. (b) DC voltage response for a step change from lagging to leading.

Fig. 4.1 The current controlled synchronous solid-state var compensation configuration

Fig. 4.2 Block diagram of the current regulated SSVC control system

Fig. 4.3 Principles of operation of the proposed current control technique

Fig. 4.4 Design values for the synchronous link reactor

Fig. 4.5 Simulated current and voltage waveforms for steady-state operating conditions and leading var compensation

Fig. 4.6 Simulated current and voltage waveforms for steady-state operating conditions and lagging var compensation

Fig. 4.7 Simulated current and voltage waveforms for transient operating conditions (step change from 1 pu leading to 1 pu lagging)

Fig. 4.8 Simulated current and voltage waveforms for transient operating conditions (step change from 1 pu leading to 1 pu lagging)
Fig. 5.1 Reactive power compensator and harmonic suppressor configuration

Fig. 5.2 Single phase equivalent circuit of the power factor compensator and harmonic suppressor system at fundamental frequency

Fig. 5.3 Phasor diagram for inductive load and lagging input power factor ($V_{ao1} = V_{an}$ to achieve nearly unity power factor lagging)

Fig. 5.4 Phasor diagram for inductive load and leading input power factor

Fig. 5.5 The $\delta$ phase-shift control unit

Fig. 5.6 Single phase equivalent circuit for harmonic components of power factor compensator and harmonic suppressor system connected to nonlinear load. (a) Equivalent circuit for ac mains. (b) Equivalent circuit for nonlinear load

Fig. 5.7 Three-phase equivalent circuit for negative sequence components

Fig. 5.8 Voltage-source inverter switching pattern with modulation index of 1.12 and associated switching angles

Fig. 5.9 (a) Simulated phase to neutral source voltage $V_{an}$. (b) Simulated source line current $I_l$

Fig. 5.10 Simulated load voltage $V_L$ and respective simulated load current $I_L$

Fig. 5.11 Simulated inverter output current $I_l$ for linear
load compensation.

Fig. 5.12 Simulated PWM voltage-source inverter waveforms for linear load compensation

Fig. 5.13 Simulated waveforms for nonlinear load compensation

Fig. 5.14 Experimental results for linear load compensation

Fig. 5.15 Experimental results for nonlinear load compensation.

Fig. 5.16 Experimental results for 10% undervoltage compensation

Fig. 5.17 Experimental results for 10% overvoltage compensation

Fig. 5.18 Experimental results for 20% unbalance in ac source voltages

Fig. A.1 The equivalent circuit of the SSVC system

Fig. A.2 The generalized phasor diagram of the perturbed system

Fig. A.3 Open loop frequency response of the SSVC for rated operating condition \( i_{q0} = 1 \text{ pu} \). (a) Magnitude diagram

Fig. A.4 Open loop frequency response of the SSVC for no load operating conditions \( i_{q0} = 0 \text{ pu} \). (a) Magnitude diagram. (b) Phase diagram

Fig. C.1 Single phase equivalent load filter circuit at mains frequency

Fig. C.2 Single phase equivalent load filter circuit for harmonic components
## LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 1.1</td>
<td>Comparison of basic types of compensators</td>
<td>14</td>
</tr>
<tr>
<td>Table 2.1</td>
<td>Frequency spectrum of current waveform associated with the switching pattern</td>
<td>32</td>
</tr>
<tr>
<td>Table 2.2</td>
<td>Design data for ac filter (pu)</td>
<td>41</td>
</tr>
<tr>
<td>Table 2.3</td>
<td>Current-source inverter switch ratings (pu)</td>
<td>41</td>
</tr>
<tr>
<td>Table 2.4</td>
<td>Design data for the dc reactor</td>
<td>41</td>
</tr>
<tr>
<td>Table 3.1</td>
<td>Frequency spectrum of voltage waveform associated with the switching pattern</td>
<td>62</td>
</tr>
<tr>
<td>Table 3.2</td>
<td>Design data for the reactor $X_1$ (pu)</td>
<td>68</td>
</tr>
<tr>
<td>Table 3.3</td>
<td>Voltage-source inverter switch ratings (pu)</td>
<td>68</td>
</tr>
<tr>
<td>Table 3.4</td>
<td>Design data associated with the dc capacitor (pu)</td>
<td>72</td>
</tr>
<tr>
<td>Table 4.1</td>
<td>Frequency spectrum of the voltage waveform</td>
<td>110</td>
</tr>
<tr>
<td>Table 4.2</td>
<td>Design data for the dc capacitor (pu)</td>
<td>112</td>
</tr>
<tr>
<td>Table 5.1</td>
<td>Design data for ac output filters (pu)</td>
<td>134</td>
</tr>
<tr>
<td>Table 5.2</td>
<td>Inverter switch ratings (pu)</td>
<td>134</td>
</tr>
<tr>
<td>Table 5.3</td>
<td>Design data for the dc capacitor (pu)</td>
<td>134</td>
</tr>
<tr>
<td>Acronym</td>
<td>Definition</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>------------</td>
<td></td>
</tr>
<tr>
<td>EPROM</td>
<td>erasable programmable read only memory</td>
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<tr>
<td>FET</td>
<td>field effect transistor</td>
<td></td>
</tr>
<tr>
<td>GTO</td>
<td>gate turn off thyristor</td>
<td></td>
</tr>
<tr>
<td>HVDC</td>
<td>high voltage direct current</td>
<td></td>
</tr>
<tr>
<td>MVA</td>
<td>mega Volt-Ampères</td>
<td></td>
</tr>
<tr>
<td>PI</td>
<td>proportional integral</td>
<td></td>
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<tr>
<td>PWM</td>
<td>pulse width modulation</td>
<td></td>
</tr>
<tr>
<td>Rc</td>
<td>ripple current factor</td>
<td></td>
</tr>
<tr>
<td>Rv</td>
<td>ripple voltage factor</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>saturated reactor</td>
<td></td>
</tr>
<tr>
<td>SSVC</td>
<td>synchronous solid-state var compensator</td>
<td></td>
</tr>
<tr>
<td>SVC</td>
<td>static var compensator</td>
<td></td>
</tr>
<tr>
<td>TCR</td>
<td>thyristor-controlled reactor</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>total harmonic distortion</td>
<td></td>
</tr>
<tr>
<td>THDi</td>
<td>total harmonic distortion of the ac current</td>
<td></td>
</tr>
<tr>
<td>THDv</td>
<td>total harmonic distortion of the ac voltage</td>
<td></td>
</tr>
<tr>
<td>TSC</td>
<td>thyristor-switched capacitor</td>
<td></td>
</tr>
<tr>
<td>VCO</td>
<td>voltage-controlled oscillator</td>
<td></td>
</tr>
</tbody>
</table>
**LIST OF PRINCIPAL SYMBOLS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_o$</td>
<td>inverter open loop gain</td>
</tr>
<tr>
<td>$A_{1}$</td>
<td>fundamental component of the inverter switching function</td>
</tr>
<tr>
<td>$A_k$</td>
<td>$k^{th}$ harmonic component of the inverter switching function</td>
</tr>
<tr>
<td>$A_{min}$</td>
<td>minimum amplitude of the triangular waveform</td>
</tr>
<tr>
<td>$C$</td>
<td>capacitor</td>
</tr>
<tr>
<td>$C_s$</td>
<td>series capacitor for slope compensation</td>
</tr>
<tr>
<td>$f_{clock}$</td>
<td>frequency of the address counter</td>
</tr>
<tr>
<td>$f_{o}$</td>
<td>ac supply frequency</td>
</tr>
<tr>
<td>$f_{t}$</td>
<td>frequency of the triangular waveform</td>
</tr>
<tr>
<td>$G_c(s)$</td>
<td>transfer function of the PI controller</td>
</tr>
<tr>
<td>$H(s)$</td>
<td>inverter closed loop transfer function</td>
</tr>
<tr>
<td>$I_a$</td>
<td>rated rms value of the inverter line current</td>
</tr>
<tr>
<td>$I_{a1}$</td>
<td>rated rms value of the fundamental component of the inverter ac current</td>
</tr>
<tr>
<td>$I_{a_k}$</td>
<td>rms value of the $k^{th}$ harmonic component of the ac current source</td>
</tr>
<tr>
<td>$i_c$</td>
<td>instantaneous capacitor current</td>
</tr>
<tr>
<td>$I_{dc}$</td>
<td>dc current</td>
</tr>
<tr>
<td>$I_{dc,L}$</td>
<td>average value of the current through the dc reactor</td>
</tr>
<tr>
<td>$I_{dc,rms}$</td>
<td>rms value of the current through the dc reactor</td>
</tr>
<tr>
<td>$I_{d2}$</td>
<td>second harmonic component of the inverter dc current</td>
</tr>
<tr>
<td>$I_{l}$</td>
<td>rated rms value of the line current</td>
</tr>
<tr>
<td>$I_{l1}$</td>
<td>rated rms value of the line current fundamental component</td>
</tr>
<tr>
<td>$I_{lk}$</td>
<td>rms value of the $k^{th}$ line current harmonic component</td>
</tr>
<tr>
<td>$I_r$</td>
<td>controllable current source output current</td>
</tr>
<tr>
<td>$I_{r}$</td>
<td>rms value of the dc reactor current</td>
</tr>
</tbody>
</table>
Irk \quad \text{rms value of the dc reactor } k^{th} \text{ current harmonic}

I_{ref} \quad \text{inverter reference current}

I_{gen} \quad \text{inverter generated current}

I_{a2}, I_{b2}, I_{c2} \quad \text{negative sequence components of the inverter line currents}

I_{a2} \quad \text{line currents}

k \quad \text{order of the harmonic component}

K_{conv} \quad \text{gain of the current-source inverter for small variations around the } 90^\circ \text{ operating point}

K_I \quad \text{gain of the integral controller}

K_m \quad \text{gain of the feedback loop}

K_P \quad \text{gain of the proportional controller}

L_s \quad \text{inductance of the saturated reactor}

L_1 \quad \text{inductance of the synchronous link reactor}

L_2 \quad \text{inductance of the load filter}

M \quad \text{modulation index}

N \quad \text{total number of memory locations}

N_p \quad \text{number of chops per half-cycle of the PWM switching pattern}

P_{ac} \quad \text{real power provided by the ac source}

Q_c \quad \text{SSVC generated or absorbed reactive power}

Q \quad \text{reactive power require to maintain constant voltage}

s \quad \text{Laplace operator}

S_c \quad \text{apparent power transferred between the ac source and the SSVC}

S_{cl} \quad \text{apparent power of the LC filter capacitor}

S_{c_{dc}} \quad \text{apparent power of the dc capacitor}
SL apparent power of the LC filter inductor
SLdc apparent power of the dc reactor
SL1 apparent power of the reactor X1
Sw semiconductor switch
Van, Vbn rms value of phase to neutral source voltages
Vcn
Va rms value of the current-source inverter line to neutral output voltage
Val rms value of the current-source inverter line to neutral output voltage fundamental component
Vak rms value of the k\textsuperscript{th} harmonic component current-source inverter line to neutral output voltage
Vao rms value of the phase to neutral inverter output voltage
Vao1 rms value of the phase to neutral inverter output voltage fundamental component
Vabo rms value of the line to line inverter output voltage
Vak rms value of the k\textsuperscript{th} harmonic component inverter phase to neutral output voltage
Vck k\textsuperscript{th} harmonic component of the voltage across the dc capacitor
Vdc dc voltage
Vdcrms rms value of the voltage across the dc capacitor
Vcmax maximum voltage across the dc capacitor
Vrk rms value of the k\textsuperscript{th} voltage harmonic across the dc reactor
Vab2, Vbc2, negative sequence components of the source line to line voltage
Vca2
Vref\textsuperscript{max} maximum reference voltage value
$V_{refmin}$  minimum reference voltage value

$X_c$  capacitive reactance of the LC filter

$X_i$  inductive reactance of the LC filter

$X_1$  synchronous reactor

$X_c$  dc capacitor impedance at mains frequency

$X_2$  load filter reactor

$X_{ef}$  load filter capacitive reactance

$X_t$  total system equivalent reactance

$\alpha$  power factor angle

$\alpha_k$  switching function angles

$\delta$  phase-shift between the ac mains voltage and the inverter output voltage

$\gamma$  storage resolution of the PWM switching patterns in degrees

$\kappa$  an appropriate integer number

$\omega_L$  impedance of the dc reactor at mains frequency

$\omega_b$  closed loop breaking frequency of the current-source var compensator

$\omega_{bc}$  closed loop breaking frequency of the voltage-source var compensator

$\omega_c$  inverter open loop break frequency

$\theta/\omega$  limits of integration

$\Delta V$  voltage fluctuation

$\lambda$  maximum slope of the inverter output current
CHAPTER 1
INTRODUCTION

1.1. Introduction

Var compensation is defined as the management of reactive power to improve the quality of the power supply in an ac power system [1]. In general, the problem of reactive power compensation is viewed from two aspects, load compensation and voltage support [2].

In load compensation the objectives are to increase the value of the load power factor, to balance the real power drawn from the ac supply, and to eliminate current harmonic components produced by large, fluctuating, nonlinear industrial loads [3]. These types of loads normally interphase with the ac system at specific points or network terminals, and can be handled best by local compensators connected to these same terminals. The main benefit provided by power factor improvement is the reduction in the reactive power flow supplied by the ac system. This results in lower cost for the purchased real power (if the utility enforces a power factor clause), increase in the ac system electrical power capacity, voltage regulation improvement, and lower power losses. Although reducing the cost of power is still the primary reason for improving the power factor, the increase in the ability of the system to transport real power can, at times, be of greater importance [4].

Voltage support is generally required to reduce voltage fluctuation at a given terminal of a transmission line. Here the load need not be localized. For example, several loads and generating units may be tied by a transmission network and the objective is to reinforce transmission capability by voltage support at the compensated terminal. This voltage support is achieved by
controlling the reactive current component that flows in the transmission lines. Var compensation in transmission systems also improves the stability of the ac system by increasing the maximum power that can be transmitted. It also helps to produce a substantially flat voltage profile at all levels of power transmission, it improves HVDC conversion terminal performance, it increases transmission efficiency, and it controls steady-state and temporary overvoltages [2].

Reactive power control is closely related to the problem of harmonic control because reactive power compensation is often associated with loads which generate harmonics. Also reactive power compensators almost always influence the resonant frequency of the power system, at least locally, and it is important that capacitors, reactors, and compensators be deployed in such a way as to avoid problems with harmonic resonances. Moreover, many types of var compensators inherently generate harmonics which must be either suppressed internally or filtered externally.

1.2 General Information on Var Compensators

Traditionally, rotating synchronous condensers and fixed or mechanically switched capacitor and inductor banks have been used for reactive power compensation. In recent years, however, there has been a greatly increased demand for controllable var sources to regulate and stabilize transmission lines and to compensate large, fluctuating, nonlinear industrial loads [5], [6], [7], [8]. Recent advances in high-power semiconductor technology and in electronic circuitry have resulted in the development of controllable static var compensators with fast response times. Conventional static var compensators employ thyristor-switched capacitors (TSC) and thyristor
phase-controlled reactors (TCR) to provide or absorb the required reactive power [9]. Force-commutated converters are also used to realize controllable current and voltage sources for reactive power and harmonic compensation [10], [11]. In particular, the use of force-commutated PWM converters with an appropriate control system permits the construction of solid-state compensators capable of generating or absorbing reactive current waveforms with a time response faster than the fundamental power network cycle. The evolution of the technology is briefly described in the following sections.

1.2.1 Fixed or mechanically switched capacitors

Shunt capacitors were first employed for power factor correction in the year 1914 [12]. The leading current drawn by the shunt capacitors compensates the lagging current drawn by the load. The selection of shunt capacitors depends on many factors the most important of which is the amount of lagging reactive power taken by the load. In the case of widely fluctuating loads, the reactive power of the load also varies over a wide range. Thus, a fixed capacitor bank may often lead to either over-compensation or under-compensation. Variable var compensation is achieved using switched capacitors. Depending on the total var requirement, capacitor banks are switched into or switched out of the system. The smoothness of control is solely dependent on the number of capacitor switching units used. The switching is usually accomplished using relays and circuit breakers. However, these methods based on mechanical switches and relays invariably have the disadvantage of being sluggish and unreliable. Also they generate high inrush currents, and require frequent maintenance [12].
1.2.2 Synchronous Condensers

Synchronous condensers have played a major role in voltage and reactive power control for more than 50 years. Functionally, a synchronous condenser is simply a synchronous machine connected to the power system. After the unit is synchronized, the field current is adjusted to either generate or absorb reactive power as required by the ac system. The machine can provide continuous reactive power control when used with the proper automatic exciter system. Synchronous condensers have been used at both distribution and transmission voltage levels to improve stability and to maintain voltages within desired limits under varying load conditions and contingency situations. However, synchronous condensers are rarely used today because they require substantial foundations and a significant amount of starting and protective equipment. They also contribute to the short circuit current and they cannot be controlled fast enough to compensate for rapid load changes. Moreover, their losses are much higher than those associated with the static compensators. Their advantages lies in their high temporary overload capacity [1].

1.2.3 Static Var Compensators

As in the case of the synchronous condenser, the aim of achieving fine control over the entire var range, has been fulfilled with the development of static compensators but with the advantage of faster response times [13]. Static var compensators (SVC) consist of standard reactive power shunt elements (reactors and capacitors) which are controlled to provide rapid and variable reactive power [1], [2], [9], [14], [15], [16]. They can be grouped into three basic categories, the saturated reactor, the thyristor-switched
capacitor and the thyristor-controlled reactor. These and their variants account for the majority of static compensators used today in both transmission and distribution systems.

1.2.3.1 Saturated Reactors

The saturated reactor (SR) compensator was the first of the modern fast-response compensators to be widely used. With field test initially reported by Friedlander in 1964 [17], this compensator is unique in that it does not employ any solid state switches or active control. A typical configuration of a SR compensator is shown in Fig. 1.1. The SR is a self regulating device that responds only to changes in its terminal voltage. The voltage regulation characteristic of the SR compensator depends on the natural saturation characteristics of the iron-core reactor, \( L_s \), the series capacitor used for saturation slope compensation, \( C_s \), and the presence of shunt capacitors, \( C \), which provide filtering and leading var generation. Without series slope-correction capacitors, the SR type compensator has a faster response time than any thyristor-controlled var compensator. Slope-correction capacitors slow this response slightly so that the SR response time is roughly identical to the 0.5 - 2 cycles settling time of thyristor-controlled var compensators.

The usual harmonics associated with saturation in iron-core devices are internally compensated by specially designed multiple coupled core twin and treble-tripler reactors [9]. The twin-tripler has six cores and the characteristic current harmonics generated are of order \( 12k \pm 1 \) \((k = 1, 2, 3,...)\). The treble-tripler has nine cores and its characteristic current harmonics are of order \( 18k \pm 1 \) \((k = 1, 2, 3,...)\). Because of its additional
harmonic canceling capability, which results in an overall harmonic generation of less than 2%, the treble-tripler is the type of saturated reactor most often used for reactive power compensation.

![Diagram of saturated reactor compensator configuration]

Fig. 1.1. The saturated reactor compensator configuration

The SR compensator has its share of technical and economic deficiencies. Slope-correction capacitors in series with the SR provide a means of modifying the voltage regulation characteristic of the compensator system. However, the potential of subharmonic resonance resulting from these capacitors must be thoroughly studied, and subharmonic filtering across these capacitors may be required. This compensator has limited flexibility with regard to modifications of its characteristics and is thus less adaptable to changing system conditions than the more flexible thyristor-controlled
compensator. However, as far as maintenance is concerned, this compensator does not require any particular care. Finally, saturated reactors have more losses than the thyristor-controlled compensators and this can be a major concern where the cost of losses is appreciable [15].

1.2.3.2 Thyristor-Switched Capacitors

Figure 1.2 shows the basic scheme of a static compensator of the thyristor-switched capacitor type. First introduced by ASEA in 1971 [18], the shunt capacitor bank is split up into appropriately small steps, which are individually switched in and out using bidirectional thyristor switches. Each single-phase branch consists of two major parts, the capacitor C and the thyristor switches Sw1 and Sw2. In addition, there is a minor component, the inductor L, whose purpose is to limit the rate of rise of the current through the thyristors and to prevent resonance with the network. The capacitor may be switched with a minimum of transients if the thyristor is turned on at the instant when the capacitor voltage and the network voltage are the same. Static compensators of the TSC type have the following properties: stepwise control, average delay of one half-cycle (maximum one cycle), and no generation of harmonics [16].

Despite the attractive theoretical simplicity of the switched capacitor scheme, its popularity has been hindered by a number of practical disadvantages [14], [15], [16]: the var compensation is not continuous, each capacitor bank requires a separate thyristor switch and therefore the construction is not economical, the steady state voltage across the non-conducting thyristor switch is twice the peak supply voltage, and the thyristor must be rated for or protected by external means against line
voltage transients and fault currents.

![Diagram of thyristor-switched capacitor configuration]

Fig 1.2. The thyristor-switched capacitor configuration.

1.2.3.3 Thyristor-controlled reactor

Figure 1.3 shows the scheme of a static compensator of the thyristor controlled reactor type. In most cases, the compensator also includes a fixed capacitor. Each of the three phase branches includes an inductor, L, and the thyristor switches Sw1 and Sw2. Reactors may be both switched and phase-angle controlled.

When phase-angle control is used, a continuous range of reactive power consumption is obtained. It results, however, in the generation of odd harmonic current components during the control process. Full conduction is obtained with a gating angle of 90°. Partial conduction is obtained with gating angles between 90° and 180°. The effect of increasing the gating angle is to reduce the fundamental component of the current. This is equivalent to an increase in the inductance of the reactor, reducing the reactive power
absorbed as well as the reactor current. However, it should be pointed out that the change in the reactor current may only take place at discrete points of time, which means that adjustments cannot be made more frequently than once per half-cycle. Static compensators of the TCR type are characterized by: the ability to effect continuous control, maximum delay of one half cycle and practically no transients. The principal disadvantages of this configuration are the generation of low frequency harmonic current components, and increased losses when working in the inductive region (i.e. absorbing reactive power) [15].

![Diagram](image)

Fig. 1.3. The thyristor-controlled reactor configuration.

1.2.3.4 Combined TSC and TCR system

Irrespective of the reactive power control range required, any static compensator can be built up from one or both of the above mentioned schemes (i.e., TSC and TCR). In those cases where the system with switched capacitors is used, the reactive power is divided into a suitable number of steps and
the variation will therefore take place stepwise. Stepless control may be obtained by incorporating a thyristor-controlled reactor, which introduces continuous control between steps. If at the same time it is desired to absorb reactive power, the entire capacitor bank is disconnected and the equalizing reactor becomes responsible for the absorption. By coordinating the control between the reactor and the capacitor steps, it is possible to obtain fully stepless control. Static compensators of the combined TSC and TCR type are characterized by a continuous control, practically no transients, low generation of harmonics (because the controlled reactor rating is small compared to the total controlled power), and flexibility in control and operation. An obvious disadvantage of the TSC-TCR as compared with TCR and TSC type compensators is the capital cost. A smaller TCR rating results in some savings, but these savings are more than absorbed by the cost of the capacitor switches and the more complex control system. A premium of 15 to 20% is typical for TSC-TCR as compared to fixed capacitor and TCR compensators [6], [15].

1.2.4 Solid-State Var Compensators

The use of force-commutated converters as a means of compensating reactive power has been shown to have considerable promise [10], [19], [20], [21]. With the remarkable progress of gate commutated semiconductor devices, attention has been focused on solid-state var compensators capable of generating or absorbing reactive power without requiring large banks of capacitors or reactors. Several approaches are possible including current-source and voltage-source inverters. The current-source approach uses a reactor supplied with a regulated dc current (see Fig. 1.4), while the
voltage-source inverter uses a capacitor with a regulated dc voltage (see Fig. 1.5).

The major advantages of solid-state var compensators are the significant reduction in size, and the potential reduction in cost achieved from the elimination of a large number of passive components and lower relative capacity requirement for the semiconductor switches [19], [20]. Because of its smaller size, solid-state var compensators are well suited for applications where space is at premium. As compared with thyristor-controlled capacitor and reactor banks, solid-state var compensators have the following advantages:

i) They can provide both leading and lagging reactive power, thus enabling a considerable saving in capacitors and reactors. This in turn reduces the possibility of resonances at some critical operating conditions.

ii) Since the time response of force-commutated converter can be faster than the fundamental power network cycle, reactive power can be controlled continuously and precisely.

iii) High frequency modulation of the force-commutated converter results in a low harmonic content of the supply current, thus reducing the size of filter components.

iv) They don't generate inrush current.

v) The dynamic performance under voltage variations and transients is improved.

vi) Solid-state var compensators are capable of generating 1 pu reactive current even when the line voltages are very low. This ability to support the line is better than that obtained with conventional var
Fig. 1.4. The solid-state current-source var compensator configuration.

Fig. 1.5. The solid-state voltage-source var compensator configuration.
compensators because the current in shunt capacitors and reactors is proportional to the voltage.

vii) Solid-state compensators with appropriate control can also act as active line harmonic filters.

An active power filter can eliminate current harmonic components by injecting its compensating current directly into the ac lines. The complete cancellation of the harmonics will be achieved if the compensator generates the exact current harmonic component required by the load. Active power filters present better harmonic compensation characteristics than conventional LC passive power filters, especially in the case of impedance fluctuation of the ac power system and frequency variation of harmonic currents [24] - [37].

Table 1.1 summarizes the comparative merits of the main types of compensators. The significant advantages of solid-state var compensators make them an interesting subject for further research. In this thesis high-performance solid-state var compensators using current-source and voltage-source PWM inverters are investigated and fully analyzed. The proposed schemes are suitable for three-phase balanced cyclic loads of moderate ratings. These include motors, drives, rectifiers, and most industrial processes, with the specific exception of arc furnaces, which are not balanced loads. Suitable design procedures for the power converter and associated control system are also discussed.

1.3 Review of Previous Work

Depending on the application solid-state compensators can be classified as either var compensators or as active filters. As var compensators,
<table>
<thead>
<tr>
<th></th>
<th>SYNCHRONOUS CONDENSER</th>
<th>STATIC COMPENSATOR</th>
<th>SOLID-STATE COMPENSATOR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TCR(with shunt capacitors if necessary)</td>
<td>TSC(with TCR if necessary)</td>
<td>Polyphase Saturated Reactor</td>
</tr>
<tr>
<td>Accuracy of</td>
<td>Good</td>
<td>Very good</td>
<td>Good</td>
</tr>
<tr>
<td>compensation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control flexibility</td>
<td>Good</td>
<td>Very good</td>
<td>Good, very good with TCR</td>
</tr>
<tr>
<td>Reactive power</td>
<td>Leading/Lagging</td>
<td>Lagging/Leading-indirect</td>
<td>Leading/Lagging-indirect</td>
</tr>
<tr>
<td>capability</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control</td>
<td>Continuous</td>
<td>Continuous</td>
<td>Discontinuous (continuous with TCR)</td>
</tr>
<tr>
<td>Response time</td>
<td>Slow</td>
<td>Fast, 0.5 to 2 cycles</td>
<td>Fast, 0.5 to 2 cycles</td>
</tr>
<tr>
<td>Harmonics</td>
<td>Very good</td>
<td>Filters may be necessary</td>
<td>Good, filters may be necessary with TCR</td>
</tr>
<tr>
<td>Losses</td>
<td>Moderate</td>
<td>Good, but increase in lagging mode</td>
<td>Good, but increase in leading mode</td>
</tr>
<tr>
<td>Phase balancing</td>
<td>Limited</td>
<td>Good</td>
<td>Limited</td>
</tr>
<tr>
<td>ability</td>
<td></td>
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</table>
solid-state converters can compensate only for displacement power factor. On the other hand, active filters can compensate for both current harmonics and the reactive power required by nonlinear loads. In this section, previous work related to both solid-state var compensators and active power filters is reviewed.

1.3.1 Solid-state Var Compensators

Gyugyi has presented a general description of different types of var compensators [10]. The principles of operation of var generators using current-source and voltage-source converters are described. Also the author investigated var generators using voltage-source and hybrid (i.e., voltage and current-source) ac/ac frequency changers. In the voltage-source ac/ac frequency changer approach, a high frequency LC resonant circuit is connected to the frequency changer, which converts the resonant high frequency to the system frequency. The output terminals of the frequency changer are connected to the ac system via small inductors. Reactive power is controlled by changing the amplitude of the frequency changer output voltage. This scheme has the potential advantage of reduced size and possibly reduced cost because the reactive elements operate at high frequency. Also, the output currents have little distortion and thus require little or no filtering. The major disadvantage of this approach is the relative complexity which makes it impractical for medium and high power applications. In the hybrid or "power doubling" arrangement the input and output sides are both connected to the ac system, and thus both the input and output frequencies are equal to the system frequency. The output terminals of the frequency changer are connected to the power system through a small inductor. As in the voltage-source scheme
reactive power control is achieved by varying the amplitude of the frequency changer output voltage. The main function of the frequency changer is to phase-shift input and output currents by 180°. This operating mode makes it possible to provide twice as much reactive power for the ac system as the actual VA rating of the frequency changer. Thus, a 0.5 pu rating can supply 1 pu reactive power to the system. Another advantage of this scheme is that, in principle, it requires no reactive storage components. The major disadvantages of this scheme are that it generates large unwanted input current and output voltage low frequency harmonics, it requires a step up transformer for leading var compensation, and as in the voltage-source ac/ac frequency changer approach, the converter topology is complex and requires a large number of gate commutated switches with a symmetrical bidirectional blocking capability which limits its application in high power systems.

Schmid proposed a var compensator that uses two controlled rectifiers, one of which is force-commutated [11]. The two converters are connected in parallel and loaded by a smoothing reactor which is common to both rectifiers. The line-commutated rectifier always draws a purely inductive current from the power system while the force-commutated rectifier generates a purely capacitive current. Therefore, the phase displacement between the supply voltage and the total input current of the rectifier can be set to leading or lagging 90° depending on which rectifier carries the larger current. The principal advantage of this configuration is that transient response is independent of the value of the reactor since fast changes in the input current are supplied from the circulating current. However, this scheme has the following disadvantages: it requires another reactor to limit the circulating current, circulating current can cause discontinuity in the dc
output current of the rectifiers with a result that full reactive power output can no longer be attained, and it generates low frequency input current harmonics. Moreover, the presence of two rectifiers involves additional cost and complexity.

Alexander et al. proposed a design procedure for a var compensator using a single-phase force-commutated current-source inverter [22], [23]. Reference [22] presented the design procedure for the dc reactor and in [23] the design of the power converter including the commutation circuit is reported. However, the design criteria on the dc inductor is based on the reactor losses, and no consideration of the inductance value to reduce harmonic distortion is discussed. Moreover, no analysis of dynamic response and control design is reported.

Walker described a 2.5 MVA compensator consisting of shunt capacitor banks and two force-commutated current-source inverters rated at 1.25 MVA each [21]. The dc terminals of the bridges are shorted through a dc inductor. The dc voltage across the inductor is near zero, and the current is regulated by controlling small deviations from the ±90° gating angle. The proposed control method is suited to provide either a unity power factor, a constant power factor other than unity, or an undisturbed voltage. The converter ac currents contain low frequency harmonics which force the use of passive filters. Moreover, the work presented in [21] does not include any data on the power circuit components, nor any analysis of the control system design.

Sumi et al. developed a 20 MVA compensator using six force-commutated three-phase voltage-source inverters connected in parallel and phase-shifted by 10° [19]. Edwards et al. implemented a 1 MVA compensator employing a twelve pulse three-phase voltage-source inverter composed of two six pulse
bridges phase-shifted by 30° [20]. The outputs of the twelve pulse inverter are connected to LC filters. In both cases ([19], [20]) the inverters are fed from a common dc capacitor and are connected to the power system through a reactor. Reactive power is controlled by adjusting the amplitude of the inverter output voltage. Any value of reactive power can be supplied by controlling the difference of the phase angle between the inverters and the line voltage. However, no design data on the power circuit components, no analysis of the control system design was reported.

1.3.2 Active Power Filters

In the last decade, active power filters have been researched and developed to suppress harmonics generated by static power converters and large nonlinear loads. Active power filters can absorb harmonic currents with variable frequencies effectively, because they can control their output current according to the harmonic current variation. Various power circuit configurations of the active power filter have been proposed [24]-[37]. Notably, attention has been paid to active power filters using current-source or voltage-source PWM converters. Although the voltage-source converter is better with regard to losses and filter capacity in the elimination of PWM carrier harmonics, the current-source type is more reliable and offers more protection.

There have been numerous papers presented and articles written about active power filters. Gyugyi and Strycula proposed a family of active power filters functioning as ideal current or voltage generators [24]. The realization of these generators is accomplished by using modulated solid-state switching circuits which operate in a self-sufficient manner from
passive reactive storage elements. Only single-phase active filters are reported.

Takahashi and Nabae presented an universal power distortion compensator [25]. The system compensates not only the active and reactive power in a step like fashion but also deals with unbalanced currents and low order harmonics. A rapid current control method is proposed using a thyristor converter which is triggered asymmetrically. However, the proposed system requires a complex control system and can compensate only for distortional components lower than the 7th harmonic.

Harashima et al. presented a closed loop control system for instantaneous reactive power compensation [26]. The proposed control system consists of a measuring circuit of reactive power and a closed-loop control with a bandwidth of 0-800 Hz. The main disadvantage of the proposed system is that to obtain the reactive power value, a half-cycle of the line frequency is required. In order to attain faster response times, the concept of instantaneous reactive power in three-phase circuits was introduced by Akagi et al. [27], [28]. The instantaneous reactive power is defined for arbitrary three-phase voltage and current waveforms without any restriction. It is defined using only the instantaneous values of the voltages and currents.

Based on the instantaneous reactive power theory, a number of active power filters capable of eliminating not only the fundamental reactive power in transient states but also some current harmonic components have been developed [28]-[38]. These active filters, however, have the following problems in terms of their practical applications:

i) It is difficult to realize a large capacity static power converter with good frequency response.
ii) The initial and long-term costs of active power filters are high compared to those of LC filters.

iii) They require a high switching frequency and a complex control system for instantaneous harmonic calculation and compensation.

Moreover, most of the active power filters that have been presented in the technical literature use hysteresis current control which has the disadvantage of generating uneven and random switching patterns.

1.4 Scope and Contributions

The scope and objective of this thesis is to present, analyze, and verify experimentally high performance solid-state var compensators using force-commutated PWM current-source and voltage-source inverters. The proposed var compensators provide improved performance characteristics in terms of smaller component ratings, lower harmonic distortion in the generated voltage and current waveforms, and continuous and accurate reactive power control. In particular, the principal contributions of this thesis are:

i) The analysis, design, and demonstration of the feasibility of three-phase solid-state var compensators that present significant reductions in reactive components. PWM techniques are used to eliminate low frequency harmonics thus reducing the size of filter elements.

ii) An analytical procedure to determine the mathematical model of a synchronous solid-state var compensator operating with the δ phase-shifted angle control method is presented (Chapter 3). The mathematical model permits the derivation of the system transfer function and the design of the compensator controller. A detailed
description of the analysis is provided in appendix A.

iii) A novel current regulated var compensator is proposed, analyzed, and designed with a time response smaller than half a cycle of the power supply and with constant switching frequency. Constant switching frequency generates a uniform switching pattern resulting in fixed current harmonic components. These harmonic components are filtered easily (Chapter 4).

iv) A novel power factor compensation technique that can maintain a near-unity ac source power factor without sensing and computing the reactive power required by the load is presented in Chapter 5.

v) A compensator topology that can substantially reduce the amplitude of any line current harmonics generated by nonlinear types of load is presented. Moreover, this topology also compensates for unbalance in the ac source voltages (Chapter 5).

1.5 Summary

The contents of this thesis have been organized as follows:

In Chapter 2 a reactive power compensator which employs a three-phase PWM current-source inverter is presented and analyzed. The proposed system can compensate for leading or lagging displacement power factor. Relevant input and output current and voltage waveforms, and component ratings are derived, and predicted results are verified experimentally. However, this topology suffers from the need for an LC ac filter to eliminate line current harmonics and a bulky reactor - disadvantages which are overcome by the approach proposed and presented in the succeeding chapter.

In Chapter 3 a three-phase synchronous solid-state var compensator which
employs a PWM voltage-source inverter is presented and analyzed. The proposed system can also compensate for leading or lagging displacement power factor with a slow response time. The proposed scheme is discussed in terms of principles of operation, power circuit and control system design, and analysis under unbalanced voltage source operating conditions. Also, a mathematical model for the compensator connected across a variable power factor load is derived. This allows the design of the controller and the study of the influence of compensator parameters in the system response. Again, predicted results are verified experimentally for both open and closed loop responses. It is also found that the system transient response can be improved with the implementation of a current control loop which is presented in the next chapter.

In Chapter 4 a current regulated var compensator that uses a three-phase PWM voltage-source inverter is proposed. Reactive power compensation is achieved by forcing the inverter output ac current to follow a reactive sinusoidal reference waveform at a constant switching frequency. The design of the power converter and the associated control system as well as the transient performance of a dynamic var compensation are presented.

In Chapter 5 a novel three-phase solid-state power factor compensator and harmonic suppressor system is proposed and analyzed. The proposed system has also the ability to work as a voltage regulator. As a voltage regulator, the system can correct for undervoltage, overvoltage, and voltage unbalances produced by the ac mains. As a power factor compensator, it can maintain a near-unity mains input power factor without sensing and computing the associated reactive power component. Also, the proposed system can substantially reduce any line current harmonics generated by nonlinear types
of load. The proposed scheme is discussed in terms of principles of operation and design criteria. A laboratory prototype has been built and used to verify the analytically predicted results.
CHAPTER 2

CURRENT SOURCE SOLID-STATE VAR COMPENSATORS

2.1 Introduction

According to the primary objective of this thesis, which is the performance improvement of solid-state var compensators, this chapter presents the analysis of a current-source var compensator which shows a significant reduction in the size of the reactive components and uses a simple control scheme. The proposed system uses a current-source PWM inverter and can compensate for displacement power factor in a three-phase balanced system. It can also provide leading or lagging reactive power which results in a considerable reduction in the passive storage element ratings as compared with other static var compensator approaches [9]. Although single-phase and three-phase versions of current source var compensators have already been presented in the technical literature [10], [21], [22], [23], the solid-state var compensator scheme used in this chapter differs from previously discussed approaches in the following ways.

i) It is designed for applications which require displacement power factor compensation (harmonics excluded) with a slow response time.

ii) Slow response times allow the use of PWM current waveshaping switching patterns that minimize the generation of unwanted harmonics.

iii) These patterns can be easily stored in a EPROM, thus simplifying logic software and hardware requirements.

iv) The use of an optimized PWM current waveshaping patterns allows significant reduction in the filter component values and sizes. They
also require lower switching frequencies, which contribute to lower switching stresses of converter components.

v) Finally, lower component stresses allow higher levels of output power from the same converter topology.

The treatment presented in this chapter includes the principles of operation, the input and output filter component design, the analysis of current and voltage stresses of components, and a method of closing the reactive power demand loop. Finally, experimental results from a prototype unit are compared and verified with the analytically predicted results.

2.2 Principles of Operation

The solid-state var compensator used in this chapter can be explained by considering a controllable current source connected in parallel with the load as shown in Fig. 2.1. The controllable current source generates a sinusoidal current waveform \( I_R \), leading or lagging by \( 90^\circ \) with respect to the corresponding phase to neutral source voltage \( V_{an} \). This implies that only reactive power flows in bilateral form going from the controllable current source to the ac system for leading \( 90^\circ \) and vice-versa for lagging \( 90^\circ \). The amount of reactive power generated or absorbed by the controllable current source can be easily controlled by adjusting the amplitude of the current \( I_R \). The expression becomes

\[
\text{var} = V_{an} I_R
\]  \hspace{1cm} (2.1)

However, \( I_R \) must be made to lag or lead \( V_{an} \) by an angle \( \alpha \) approximately equal to \( 90^\circ \) so that the controllable current source absorbs adequate real power from the ac system. This real power coincides with the current source losses.

Figure 2.2 illustrates a practical version of the controllable current
source shown in Fig. 2.1. The PWM current-source inverter is set to operate at a phase shift angle \( \alpha \) which is close to 90° (leading or lagging). At this point, the current-source inverter is capable of compensating for system losses while maintaining the desired reactive power level. The required value of the reactive power can be regulated by adjusting the amplitude of the ac current \( I_a \) through a gating control of the inverter switches. It is noted that the magnitude of the ac current \( I_a \) is dependent on the magnitude of the dc current \( I_{dc} \). To increase the amplitude of \( I_a \), a small positive dc voltage must be applied to the reactor so that \( I_{dc} \) will increase until it reaches the required value. The expression becomes

\[
I_{dc}(t) = \frac{V_{dc} t}{L} + I_{dc}(O^-)
\]  

(2.2)

In the same way, if it is necessary to decrease the amplitude of \( I_a \), then a small negative dc voltage must be applied to the reactor. The expression is given by

\[
I_{dc}(t) = I_{dc}(O^-) - \frac{V_{dc} t}{L}
\]  

(2.3)

The required levels of positive or negative \( V_{dc} \) voltages are obtained through the closed-loop control shown in Fig. 2.3.

2.3 System Description

The topology of the three-phase current-source var compensator is shown in Fig. 2.2. It consists of a three-phase mains, a second-order ac filter, a PWM current-source inverter, and a dc reactor. The nature and functions performed by each major system component are described as follows.
Fig. 2.1. Principle of reactive current compensation.

Fig. 2.2. The current-source var compensator configuration.
2.3.1 Power Circuit Description

The first major system component is a three-phase PWM current-source inverter. The ac terminals of the inverter are connected to the ac mains through an LC filter. The inverter LC filter acts as an interface between the three-phase PWM current-source inverter and the ac mains. As such, its function is to minimize the dumping of current and voltage harmonics on utility lines. The dc side of the current-source inverter is connected to a reactor which carries a unidirectional current Iac and is the main reactive energy storage element. The clamping circuit connected to the dc side is designed to absorb, in case of fault, the whole energy of the dc reactor while keeping the resulting voltage stresses on system components within safe limits.

2.3.2 Reactive Power Control Circuit Description

The block diagram of the reactive power control circuit shown in Fig. 2.3. is expanded in Fig. 2.4. This circuit consists of a controller, a voltage-controlled oscillator (VCO), a counter, and a stored switching pattern. An optimized stored PWM current waveform switching pattern which minimizes the generation of unwanted harmonics is continuously applied to the six gate-commutated converter switches. Reactive power control is achieved by adjusting the amplitude of the dc current Iac. To avoid jittering problems caused by harmonic components in the ac mains voltages, the proposed control scheme does not require a zero crossing detector for gating signal synchronism. The average voltage, Vac, applied across the dc reactor is controlled by changing the frequency of the switching pattern. The principles of operation are as follows.

Under steady-state operating conditions (i.e., \( \alpha \approx 90^\circ \) leading or
Fig. 2.3. Closed loop control of compensating current.

Fig. 2.4. The reactive power control circuit.
lagging) the var demand signal is zero and the stored switching pattern is read at a fixed frequency close to \( f_0 \) (the ac supply frequency). At this operating point the inverter absorbs the real power necessary to compensate for system losses while it maintains the required reactive power level. If the var reference changes, the controller adjusts the input voltage of the VCO to read the stored pattern at a different frequency thus generating a positive or negative average voltage value across the dc reactor. The variation in the reactor voltage in turn changes the amplitude of the dc current. Note that the frequency of the VCO is changed only until the dc current reaches the new value. For leading var compensation, if the pattern is read at a frequency lower than \( f_0 \) (\( V_{dc} < 0 \)) then the value of the reactive power generated will increase, and for lagging var compensation, the reactive power generated will increase if the pattern is read at a frequency higher than \( f_0 \) (\( V_{dc} < 0 \)).

2.3.3 PWM Switching Pattern

The performance characteristics of the static power converter largely depends on the choice of the particular PWM strategy employed. The PWM schemes available today can be broadly classified as carrier modulated sine PWM [39], and programmed PWM schemes [40]. Programmed PWM techniques optimize a particular switching function so as to obtain minimum losses [41], reduced torque pulsation [42], or selective elimination of harmonics [43], and therefore are the most effective means of obtaining high performance results. Since in this application the objective is to minimize the size of the ac filter and the dc reactor, the switching function should result in the selective elimination of low frequency harmonics. The main disadvantage of
the programmed PWM technique is the difficulty of computing the specific PWM switching angles to optimize a particular switching function. Despite this difficulty, as compared with the conventional carrier modulated sine PWM schemes, programmed PWM techniques have the advantages of presenting about 50% reduction in the inverter switching frequency, and higher voltage gain due to the possibility of overmodulation [40]. Moreover, the use of a precalculated optimized programmed PWM switching pattern avoids on line computations and provides a straightforward implementation of a high performance technique.

The optimized stored PWM current waveshaping pattern is shown in Fig. 2.5. Table 2.1 shows the frequency spectrum of the ac current waveform $I_a$ generated with this pattern [44]. Inspection of this frequency spectrum shows that the selected PWM scheme attenuates the low-order harmonics of the current $I_a$ effectively. The amplitude of the fundamental component of $I_a$ has been taken as 100%.

2.4 Power Circuit Design

The power circuit data presented in this section have been obtained with the following assumptions.

i) The three ac mains voltages are balanced.

ii) The inverter switching elements are ideal.

iii) The filter components are ideal.

iv) The direct current $I_d$ is ripple-free.

v) The ac filter delivers rated reactive power.

vi) The current-source inverter is delivering rated leading reactive power.
Fig. 2.5. Inverter switching pattern and associated switching angles (a₁=2.1, a₂=13.8, a₃=17.5, a₄=25.2, a₅=30, a₆=34.8, a₇=42.5, a₈=46.2, a₉=57.9).

<table>
<thead>
<tr>
<th>Order</th>
<th>Amplitude (percent)</th>
<th>Order</th>
<th>Amplitude (percent)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>23</td>
<td>4.603</td>
</tr>
<tr>
<td>5</td>
<td>0.113</td>
<td>25</td>
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</tr>
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<td>11</td>
<td>2.121</td>
<td>31</td>
<td>21.473</td>
</tr>
<tr>
<td>13</td>
<td>1.273</td>
<td>35</td>
<td>9.176</td>
</tr>
<tr>
<td>17</td>
<td>1.641</td>
<td>37</td>
<td>9.337</td>
</tr>
<tr>
<td>19</td>
<td>8.511</td>
<td>41</td>
<td>6.927</td>
</tr>
</tbody>
</table>
vii) The inverter switching pattern is as shown in Fig. 2.5.

Design data are expressed in per unit with respect to the following base:

\[ V_{\text{base}} = V_{a1} \], rated value of the fundamental component of the PWM current-source inverter line to neutral voltage,

\[ I_{\text{base}} = I_{a1} \], rated value of the fundamental component of the PWM current-source inverter ac current.

2.4.1 AC Filter Design

The size, cost, and complexity of the ac filter is determined by the specified total harmonic distortion in the ac source current (THDi) and in the ac voltage (THDv). By definition, THDv and THDi are

\[
\text{THDv} = \frac{100}{V_{a1}} \left[ V_a^2 - V_{a1}^2 \right]^{1/2}
\]

(2.4)

where \( V_a \) is the rms value of the PWM current-source inverter phase to neutral voltage and \( V_{a1} \) is the rated rms value of the fundamental component of \( V_a(t) \); and

\[
\text{THDi} = \frac{100}{I_{i1}} \left[ I_i^2 - I_{i1}^2 \right]^{1/2}
\]

(2.5)

where \( I_i \) is the rms value of the line current and \( I_{i1} \) is the rated rms value of the fundamental component of \( I_i(t) \). Since the current \( I_i(t) \) contains an infinite number of harmonic components, for a leading power factor it is analytically defined by
\[ I(t) = \sum_{k=1}^{\infty} I_{1k} \sin \left( k(\omega t + 90^\circ) \right) \]  

(2.6)

Similarly, the inverter line current is analytically defined by

\[ I_a(t) = \sum_{k=1}^{\infty} I_{ak} \sin \left( k(\omega t + 90^\circ) \right) \]

(2.7)

As the switching pattern has quarter wave symmetry only odd harmonics exists (Fig. 2.5) and its Fourier coefficients, \( I_{ak} \), are given by, [43]

\[ I_{ak} = \frac{4I_{dc}}{k\pi} \sum_{j=1}^{N_p} (-1)^{j+1} \cos (k\alpha_j) \]

(2.8)

where \( N_p \) is the number of chops per half-cycle in the current \( I_a(t) \) \( (N_p = 11) \).

With the assumption that all the harmonics \( I_{ak} \) circulate through the capacitor, from Fig. 2.7

\[ V_{ak} = -j \frac{X_c}{k} I_{ak} \]

(2.9)

then the total rms value of the voltage across the capacitor is given by

\[ \left[ \sum_{k=5}^{\infty} V_{ak}^2 \right]^{1/2} = X_c \left[ \sum_{k=5}^{\infty} \left( \frac{I_{ak}}{k^2} \right)^2 \right]^{1/2} \]

(2.10)

and from (2.4)
\[ X_c = \frac{V_{a1} \text{THD}_{v}}{\left[ \sum_{k=5}^{\infty} \left[ \frac{I_{ak}}{k^2} \right] \right]^{1/2}} \]  \hspace{1cm} (2.11)

Figure 2.7 shows that in magnitude

\[ \left[ \sum_{k=5}^{\infty} I_{1k}^2 \right]^{1/2} = \frac{X_c}{X_1} \left[ \sum_{k=5}^{\infty} \left[ \frac{I_{ak}}{k^2} \right]^2 \right]^{1/2} \]  \hspace{1cm} (2.12)

and from (2.5)

\[ X_1 = \frac{X_c}{I_{11} \text{THD}_{i}} \left[ \sum_{k=5}^{\infty} \left[ \frac{I_{ak}}{k^2} \right]^2 \right]^{1/2} \]  \hspace{1cm} (2.13)

From Fig. 2.6

\[ I_{11} = j \left[ I_{a1} + \frac{V_{a1}}{X_c} \right] \]  \hspace{1cm} (2.14)

or

\[ I_{11} = -j \left[ I_{a1} - \frac{V_{a1}}{X_c} \right] \]  \hspace{1cm} (2.15)

for leading or lagging power factor.

The apparent power required by the ac filter components is given by (2.16) and (2.17):

\[ S_L = X_1 I_{11}^2 + \frac{X_c^2}{X_1} \sum_{k=5}^{\infty} \frac{I_{ak}^2}{k^2} \]  \hspace{1cm} (2.16)

is the apparent power required by the reactor, and
Fig. 2.6. Analytical model for the LC filter. (a) Single phase equivalent LC filter circuit. (b) Single phase equivalent circuit at fundamental frequency. (c) Phasor diagram for leading power factor. (d) Phasor diagram for lagging power factor.

Fig. 2.7. Single phase equivalent LC filter circuit for harmonics.
\[ S_{ci} = \frac{V_{s1}^2}{X_c} + X_c \sum_{k=5}^{\infty} \frac{I_{s1}^2}{k} \]  \hspace{1cm} (2.17)

is the apparent power required by the capacitor.

Solving (2.8), (2.11), (2.13)-(2.17), with the constraints that under rated operating conditions THDi \leq 5\% and THDv \leq 10\%, for a leading power factor, it is found that \( X_c = 7.27 \) pu and \( X_l = 0.0684 \) pu. The apparent power required by the capacitor and by the reactor is 0.1767 pu and 0.0939 pu.

The ac filter design data associated with the PWM current-source inverter and with a structure which utilizes a six-step inverter are summarized in Table 2.2. Table 2.2 shows that the proposed PWM scheme yields significant reductions in the ac filter components values (approximately 70\%) and in the filter kVA (approximately 74\%) as compared with structures which utilizes a six-step inverter.

Figure 2.8 shows the frequency response of the LC filter. The resonant frequency is located at \( f/f_o = 10.3 \). Since the selected PWM switching pattern effectively eliminates low frequency components (see Table 2.1) the LC filter does not create low frequency resonances. However, the filter amplifies some low frequency current components.

### 2.4.2 Semiconductor Switch Ratings

For rated operating conditions the design data presented in Table 2.3 include the rms, and peak current rating for each switch, as well as the peak forward and reverse blocking voltages. The switching frequency for the PWM inverter is 660 Hz, and for the six step inverter is 60 Hz. The type of gate commutated switch (i.e., power fets, bipolars, GTO's etc.) is not specified,
Fig. 2.8. The frequency response of the LC filter.
because the choice of switches depends on the respective voltage and current levels. All relevant data are presented in summary form, in pu with respect to ac base values, in Table 2.3.

2.4.3 DC Reactor Design

For symmetrical and sinusoidal ac waveforms, reactive power is compensated by interchanging energy among the phases. In this case the dc reactor only serves to provide a dc current for the inverter. For this reason, the design of the dc reactor is performed with the constraint that under rated operating conditions the ripple factor for the direct current $I_{dc}$ is less than five percent and the ac line to line voltages are balanced and sinusoidal. Hence

$$R_c = \frac{\sum_{k=6}^{\infty} I_{rk}^2}{I_{dcL}}$$

(2.18)

where

$$I_{rk} = \frac{V_{rk}}{k\omega L}$$

(2.19)

and

- $R_c$ ripple current factor,
- $I_{rk}$ rms value of the $k^{th}$ current harmonic through the dc reactor,
- $I_{dcL}$ average value of the current through the reactor,
- $V_{rk}$ rms value of the $k^{th}$ voltage harmonic across the dc reactor,
- $\omega L$ impedance of the dc reactor at mains frequency (i.e., $\omega L = 120\pi L \Omega$),
\[ \omega_L = \frac{1}{Rc Ldc} \left[ \sum_{k=0}^{\infty} \frac{V_{rk}^2}{k^2} \right]^{1/2} \] 

(2.20)

The voltage across the reactor \( V_{dc}(t) \) is given by

\[ V_{dc}(t) = \sum_{k=1}^{\infty} V_{an}(t) A_k \sin(k\omega t) + \sum_{k=1}^{\infty} V_{bn}(t) A_k \sin(k\omega t - 120k) + \sum_{k=1}^{\infty} V_{cn}(t) A_k \sin(k\omega t + 120k) \] 

(2.21)

where (a), (b), and (c) are the switching functions of the PWM current-source inverter obtained with the PWM scheme (Fig. 2.5), and \( V_{an}(t), V_{bn}(t), V_{cn}(t) \) are the ac mains phase to neutral voltages. Developing (2.21) for balanced ac voltages

\[ V_{dc}(t) = \frac{3}{\sqrt{2}} V_{an} \left\{ \sum_{k=1,2}^{\infty} (-1)^{k+1} \left[ A_{6k+1} + A_{6k-1} \right] \cos(6k\omega t) \right\} \] 

(2.22)

where \( V_{an} \) is the rms value of the ac mains voltage.

The maximum apparent power allowed in the reactor is limited by inductor saturation and is given by

\[ S_{Ldc} = V_r I_r \] 

(2.23)

where \( V_r \) and \( I_r \) are the rms value of the voltage across and the current through the dc reactor. Table 2.4 summarizes the design data for the dc reactor associated with the PWM scheme and with a typical six-step approach.
### TABLE 2.2
DESIGN DATA FOR AC FILTER (pu)

<table>
<thead>
<tr>
<th></th>
<th>X&lt;sub&gt;i&lt;/sub&gt;</th>
<th>I&lt;sub&gt;i&lt;/sub&gt; (rms)</th>
<th>S&lt;sub&gt;L&lt;/sub&gt;</th>
<th>X&lt;sub&gt;c&lt;/sub&gt;</th>
<th>S&lt;sub&gt;c&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM Inverter</td>
<td>0.068</td>
<td>1.139</td>
<td>0.094</td>
<td>7.27</td>
<td>0.177</td>
</tr>
<tr>
<td>Six step Inverter</td>
<td>0.252</td>
<td>1.466</td>
<td>0.548</td>
<td>2.16</td>
<td>0.491</td>
</tr>
</tbody>
</table>

### TABLE 2.3
CURRENT-SOURCE INVERTER SWITCH RATINGS (pu)

<table>
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<tr>
<th></th>
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<tbody>
<tr>
<td>PWM Inverter</td>
<td>1.386</td>
<td>0.8</td>
<td>2.45</td>
<td>2.45</td>
</tr>
<tr>
<td>Six step Inverter</td>
<td>2.565</td>
<td>1.481</td>
<td>2.45</td>
<td>2.45</td>
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</table>

### TABLE 2.4
DESIGN DATA FOR DC REACTOR (pu)

<table>
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<th></th>
<th>ωL</th>
<th>S&lt;sub&gt;Ldc&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM Inverter</td>
<td>0.278</td>
<td>2.15</td>
</tr>
<tr>
<td>Six step Inverter</td>
<td>1.08</td>
<td>4.3</td>
</tr>
</tbody>
</table>
Table 2.4 shows that the proposed structure yields significant reduction in
the dc reactor value and size.

2.5 Reactive Power Control Unit Design

The reactive power control unit consists of a dc current control circuit
and a gating signal generator. The dc current, \( I_{dc} \), is controlled against the
reactive power reference signal (Fig. 2.2), so that the dc voltage becomes
the value which will produce the reactive power demanded. The gating signal
generator provides the switching pattern to the six gate-commutated switches
of the inverter continuously.

2.5.1 DC Current Control Circuit Design

The block diagram of the closed loop control is shown in Fig. 2.9. It
consists of a proportional controller, \( K_P \), the inverter, the dc reactor, and
the feedback loop with gain \( K_m \). The parameters of the dc reactor are \( L \) and \( R \),
where \( R \) represents the losses of the reactor, the switches, and the ac
filter. The ratio between the controller output voltage and the mean value of
the inverter dc voltage, \( V_{dc} \), is nonlinear. However, for small variations,
this ratio is linearized and equal to the constant \( K_{conv} \). The closed loop
transfer function of the system is equal to

\[
\frac{\Delta I_{dc}}{\Delta I_{ref}} = \frac{K_P K_{conv}}{R + sL} = \frac{K_P K_{conv}}{s + \frac{Km}{R + sL}}
\]

(2.24)

The closed loop break frequency of the var compensator, \( \omega_b \), is
\[ \omega_b = \frac{R + K_m K_P K_{conv}}{L} \quad (2.25) \]

From (2.25) the gain of the proportional controller is found to be

\[ K_P = \frac{\omega_b L - R}{K_m K_{conv}} \quad (2.26) \]

Fig. 2.9. The block diagram of the dc current control loop.

2.5.2 Gating Signals Generator Design

The main parameters for the design of the gating signal generator circuit are

i) the ac mains frequency \( f_0 \),

ii) the storage resolution \( \gamma \) of the PWM switching pattern in degrees.

Assuming a storage resolution of \( \gamma \) degrees per memory location, it follows that the total number of memory locations, \( N \), becomes

\[ N = \frac{360}{\gamma} \quad (2.27) \]
Furthermore, for better compatibility with existing memory devices, $\gamma$ should be chosen such that

$$\frac{360}{\gamma} = 2^\kappa$$  \hspace{1cm} (2.28)

where $\kappa$ is an appropriate integer number.

Consequently, the number of stages, $a$, of the counter required to address sequentially the aforementioned memory locations must satisfy (2.28). Also, since the switching pattern has to be read $f_o$ times per second the corresponding frequency of the address counter clock becomes

$$f_{\text{clock}} = f_o N = f_o \frac{360}{\gamma}$$  \hspace{1cm} (2.29)

2.6 Simulated PWM Inverter Results

To verify analytical key results, the aforementioned compensator structure as specified in Tables 2.2-2.4 was tested by simulation on a HP 9836 microcomputer. A dedicated computer program was employed to generate the switching functions and the steady-state voltage and current waveforms shown in Figs. 2.10(a)-(d), 2.11(a)-(d).

Figures 2.10(a) and 2.11(a) show the switching function for the phase A for leading and lagging modes of operation. Figures 2.10(b) and 2.11(b) show the ac line current $I_l$ and the corresponding phase to neutral voltage, $V_{an}$, obtained with the operating conditions depicted in Figs. 2.10 and 2.11. Figures 2.10(c) and 2.11(c) show the phase to neutral voltage of the PWM current-source inverter $V_{ak}$ with the corresponding ac current $I_a$. Figures 2.10(d) and 2.11(d) show the dc voltage applied across the dc reactor for leading and lagging reactive power compensation. Table 2.1 shows that the
amplitude of the 7th and 11th harmonic component of the switching pattern are effectively reduced. However, because of the frequency response of the LC filter (see Fig. 2.8), the amplitude of these harmonic components are amplified. Nevertheless, this result is acceptable because the THDi of the ac current is below 5%.

2.7 Design Example

To illustrate the significance and facilitate the use of the theoretical results obtained in section 2.5, the following example is given.

2.7.1 Power Circuit

The compensator has the following specifications:

\[ V_{\text{an}} \quad \text{ac supply,} \quad 117 \text{ V}, \]
\[ S \quad \text{compensator input apparent power,} \quad 1.1 \text{ kVA}, \]
\[ f_0 \quad \text{supply frequency} \quad 60 \text{ Hz}. \]

From these values the following base values are defined,

1 pu voltage \( V = 117 \text{ V} \)
1 pu apparent power \( S = 375 \text{ VA} \)
1 pu current \( I = 3.2 \text{ A} \)
1 pu impedance \( Z = 36.5 \Omega \)
1 pu frequency \( f = 60 \text{ Hz} \).

Therefore, using Tables 2.2-2.4 the specifications of the components of the reactive power compensator system are given by

i) AC filter:

\[ X_1 = 2.5 \Omega \quad L = 6.6 \text{ mH} \quad S_L = 35.2 \text{ VA} \]
\[ X_c = 265 \Omega \quad C_1 = 10 \mu\text{F} \quad S_{C1} = 66.3 \text{ VA} \]
Fig. 2.10. Inverter simulated waveforms for capacitive mode of operation with the PWM scheme ($X_C = 7.27$ pu, $X_I = 0.068$ pu). (a) Switching function phase A. (b) AC line current $I_l$, phase to neutral source voltage $V_{an}$. (d) Inverter ac current $I_a$ with inverter phase to neutral voltage $V_{ak}$. (d) Inverter dc voltage $V_{dc}$. 
Fig. 2.11. Inverter simulated waveforms for inductive mode of operation with PWM scheme ($X_c = 7.27\text{ pu}, X_l = 0.068\text{ pu}$). (a) Switching function phase A. (b) AC line current $I_l$ with the phase to neutral source voltage $V_{an}$. (c) Inverter ac current $I_a$ with inverter phase to neutral voltage $V_{ak}$. (d) Inverter dc voltage $V_{dc}$. 
ii) Semiconductors:
Peak Current = 4.4 A    Average Current = 1.5 A    RMS Current = 2.6 A
Peak Forward Voltage = 287 V    Peak Reverse Voltage = 287 V.
Switching Frequency = 660 Hz.

iii) DC Reactor:
\[ \omega L = 10.14 \, \Omega \quad L = 27 \, \text{mH} \quad S_{Ldc} = 682 \, \text{VA}. \]

2.7.2 DC Voltage Control

The required closed loop bandwidth of the var compensator is 10 Hz. Using (2.26) with
\[ \omega_b = 20\pi \, \text{rad/s} \quad R = 0.5 \, \Omega \]
\[ L = 27 \, \text{mH} \quad K_m = 0.01 \]
\[ K_{conv} = 35 \]

\( K_P \) is equal to 3.42.

The practical implementation of the proportional controller is shown in Fig. 2.12. The absolute value of its transfer function is given by

\[ K_P = \left| \frac{V_o}{V_1} \right| = \frac{R_2}{R_1} = 3.42 \]  \hspace{1cm} (2.30)

![Diagram](image)

Fig. 2.12. The proportional controller.
2.7.3 Phase shift Control Circuit

Theoretical investigation of the switching pattern employed in this chapter has shown that a resolution of $0.1^\circ$ per memory location maintains accurately the harmonic spectrum shown in Table 2.1 [45]. Consequently, the minimum number of memory locations chosen for the experimental investigation of the compensator system becomes $N = 360/0.1 = 3600$ memory locations. In order to use standard devices a 4 Kb EPROM is selected. The frequency of the address counter clock is given by

$$f_{clock} = 60 \times 4096 = 245.76 \text{ kHz}.$$  

2.8 Experimental Results

To check the validity of the proposed analysis and design method, selected theoretical results were verified with an experimental 1.1 kVA unit.

2.8.1 Steady-State Response

Steady-state results obtained with this reactive power compensator experimental unit are shown in Figs. 2.13 and 2.14. Figures 2.13(a) and 2.14(a) show the line current $I_l(\omega t)$ with the phase to neutral source voltage $V_{an}(\omega t)$ for leading and lagging var compensation. Figures 2.13(b) and 2.14(b) show the line current $I_l(\omega t)$ and its frequency spectrum. From these figures it is apparent that $I_l(\omega t)$ has a low total harmonic distortion (THDi). This result is in close agreement with the THDi specification that has been included in the design of the compensator structure (THDi < 5%). The presence of low frequency components in the line currents is due to the frequency response of the LC filter. Figures 2.13(c) and 2.14(c) illustrate the
experimental inverter line to line voltage $V_{ab}(\omega t)$ and line current $I_a(\omega t)$. Finally, Figs. 2.13(d) and 2.14(d) show the dc voltage applied across the dc reactor for leading and lagging modes of operation.

Comparison with the simulated waveforms shown in Figs. 2.10 and 2.11 reveals a close agreement between predicted and experimental current and voltage waveforms values. Moreover, agreement between the waveforms implies agreement in the respective peak, average, and rms current and voltage values.

2.8.2 Dynamic Response

The current-source var compensator was tested for dynamic response using a biased sinusoidal-wave reference. The amplitude of the reference was adjusted to cause the var compensator to swing to its rated limits. The frequency of the sinusoidal reference var was increased until the current generated by the inverter could no longer track the reference. The performance evaluation of the subject model has revealed excellent system response under dynamic conditions with maximum bandwidth of 10 Hz as shown in Fig. 2.15.

2.9 Conclusion

In this chapter a reactive power compensator which employs a three-phase current-source PWM inverter has been presented and analyzed. The proposed scheme is designed for applications in three-phase balanced systems which mainly require displacement power factor compensation (leading or lagging) with a slow response time (i.e., harmonics excluded). PWM is used as a means of reducing the size of the reactive components. Performance evaluation and
Fig. 2.13. Experimental voltage and current waveforms for capacitive var compensation. (a) AC line current $I_1$ (2 A/div) with the phase to neutral source voltage $V_{an}$ (50 V/div), $f_0 = 60$ Hz. (b) Line current $I_1$ and its frequency spectrum. (c) Inverter line to line voltage $V_{ab}$ (100 V/div) with the inverter ac current $I_a$ (2 A/div), $f_0 = 60$ Hz. (d) Voltage across the dc reactor $V_{dc}$ (100 V/div), $f_0 = 60$ Hz.
Fig. 2.10. Experimental voltage and current waveforms for inductive var compensation. (a) AC line current $I_l$ (2 A/div) with the phase to neutral source voltage $V_{an}$ (50 V/div), $f_0 = 60$ Hz. (b) Line current $I_l$ and its frequency spectrum. (c) Inverter line to line voltage $V_{ab}$ (100 V/div) with the inverter ac current $I_a$ (2 A/div), $f_0 = 60$ Hz. (d) Voltage across the dc reactor $V_{dc}$ (100 V/div), $f_0 = 60$ Hz.
related design equations are provided for the implementation of the converter and the associated control circuits. Detailed ac current harmonic analysis has shown that the proposed configuration yields effective suppression of low order harmonic components allowing significant reduction in reactive filter components. A method for controlling the generated reactive power has also been discussed. The closed agreement between analytical and experimental results proves the validity of the analysis and the feasibility of the proposed reactive power compensator.

Fig. 2.15. Response of the current-source var compensator to a biased sinusoidal-wave var reference. (a) Var reference. (b) DC current Idc.
CHAPTER 3
SYNCHRONOUS SOLID-STATE VAR COMPENSATORS

3.1 Introduction

Although the current source var compensator discussed in chapter 2 has the advantages of being reliable and easy to protect, it also has several disadvantages including the requirements of power semiconductors with symmetrical bidirectional voltage blocking capability, the use of an LC filter to eliminate current harmonic components, and the use of a bulky reactor. These disadvantages can be eliminated with the use of a voltage-source inverter. Voltage-source inverters require semiconductors with only unidirectional voltage blocking capabilities, also they generate an ac output voltage with a relatively low harmonic content so that current harmonic components can be attenuated with a simple reactor.

In this chapter a synchronous solid-state var compensator (SSVC) system which employs a three-phase PWM voltage-source inverter is presented and analyzed. The proposed SSVC can compensate for leading and lagging displacement power factor with a slow response time. A slow response time allows the use of PWM voltage waveshaping switching patterns that minimize the generation of unwanted harmonics which, in turn, allows significant reduction in the size of filter components and switching stresses.

The contents of this chapter, also include the principles of operation, the power and control circuit design, and the analysis of unbalanced ac mains voltage conditions. Based on the synchronous machine theory [48], the SSVC mathematical model is derived. The mathematical model allows the design of the system controller and the transient analysis. Finally, predicted results
for transient and steady-state conditions are verified experimentally for both open and closed loop responses.

3.2 Principles of Operation

The operating principles of the SSVC can be explained, with reference to the synchronous machine theory, by considering a variable voltage source connected to the ac mains through an inductor, as shown in Fig. 3.1 [19]. The general expression for the apparent power flowing between the ac mains and the SSVC is given by

$$ S = \frac{V_{an}}{X_1} \sin(\delta) - j \left[ \frac{V_{an}}{X_1} \cos(\delta) - \frac{V_{an}^2}{X_1} \right] $$

where $\delta$ is the phase-shift between the phase to neutral ac mains voltage, $V_{an}$, and the phase to neutral SSVC output voltage, $V_{ao1}$.

![Diagram](image)

(a)

(b)

(c)

Fig. 3.1. The principles of operation of the SSVC system. (a) Single phase equivalent circuit of the SSVC at fundamental frequency. (b) Phasor diagram for leading power factor. (c) Phasor diagram for lagging power factor.
Figure 3.1 and equation (3.1) illustrate the following system characteristics:

i) Real power flow is bilateral going from \(V_{an}\) to \(V_{a01}\) for lagging \(\delta\) and vice-versa for leading \(\delta\).

ii) For the limited case of \(\delta = 0^\circ\) and the power factor angle \(\alpha = \pm 90^\circ\) only reactive power flows.

iii) For \(\delta = 0^\circ\) and \(V_{a01} > V_{an}\) the SSVC supplies only leading reactive power.

iv) For \(\delta = 0^\circ\) and \(V_{a01} < V_{an}\) the SSVC absorbs only lagging reactive power.

v) For \(\delta = 0^\circ\), \(I_{al}\) is directly proportional to \(V_{an}-V_{a01}\). Consequently the required reactive power can be controlled from full leading (capacitive) to full lagging (inductive) by adjusting the amplitude of the var compensator output voltage, \(V_{a01}\). For \(\delta = 0^\circ\) the expression for the reactive power becomes, from (3.1)

\[
Q_c = \frac{\frac{V_{an}(V_{an}-V_{a01})}{X_1}}
\]

(3.2)

Figure 3.2 illustrates a practical implementation of the variable voltage source, \(V_{a01}\), shown in Fig. 3.1. It consists of a pulse-width modulated voltage-source inverter connected to a dc capacitor. The inverter output voltages are connected to the ac mains through an inductor and are kept in phase with the ac mains voltages.

Since the PWM voltage-source inverter operates without an external dc supply, using a self controlled dc bus, the amplitude of \(V_{a00}\) is controlled by adjusting the small amount of real power absorbed by the inverter through the \(\delta\) closed-loop control circuit shown in Fig. 3.3. Under steady-state
operating conditions the PWM voltage-source inverter absorbs the real power necessary to compensate for the capacitor, inductors, and switching losses, while maintaining the required output voltage value. To increase the amplitude of $V_{abo}$ a small positive average value of current must circulate through the dc capacitor so that $V_{dc}$ will increase until $V_{abo}$ reaches the required value. In the same way, if it is necessary to decrease the amplitude of $V_{abo}$ then a small negative average value of current must flow through the dc capacitor. The inverter output line to line voltage, $V_{abo}$, is equal to the dc capacitor voltage, $V_{dc}$, multiplied by the modulation index (M) of the inverter switching function, that is

$$V_{abo,\text{peak}} = M V_{dc}$$

(3.3)

![Diagram](image)

Fig. 3.2. Synchronous solid-state var compensator configuration.
3.3 System Description

Figure 3.2 shows the circuit diagram of the synchronous solid-state var compensator studied. It consists of a three-phase ac supply, a synchronous link, a PWM voltage-source inverter, and a dc capacitor. The nature and function performed by each major system component are described as follows.

3.3.1 Power Circuit Description

The principal power system component of the SSVC shown in Fig. 3.2 is a three-phase PWM voltage-source inverter. The ac terminals of the inverter are connected to the ac mains through a synchronous link, $X_1$, which also serves as first order low-pass filter. The dc side of the PWM voltage-source inverter is connected to a dc capacitor which carries the input ripple current of the inverter and is the main reactive storage element.

3.3.2 Control Circuit Description

Figure 3.4 depicts the block diagram of the $\delta$ phase-shift control system shown in Fig. 3.3. It contains the $\delta$ control unit and the gating signal generator unit. The $\delta$ control unit generates the reset pulse to the counter thus providing the correct value for the phase-shift angle $\delta$. This control unit has a proportional-integral (PI) controller, a comparator, a ramp generator (in synchronism with the ac mains voltage), and a positive edge differentiator. The gating signal generator consists of a VCO, a counter, and a stored switching pattern.

The control of the $\delta$ phase-shift angle is achieved by varying the reset pulse of the counter that addresses the EPROM (Fig. 3.4). Under steady-state operating conditions, the phase-shift angle $\delta$ is adjusted to allow the flow
Fig. 3.3. Closed loop control of compensating current for SSVC.

Fig. 3.4. Block diagram of the $\delta$ phase shift control.
of the small amount of real power necessary to compensate for system losses. If the var demand signal changes, the PI controller adjusts one of the inputs of the comparator providing the required δ. Note that the other input of the comparator is a ramp waveform which is synchronized with the ac mains voltage.

3.3.3 PWM Switching Pattern Description

For the application described in this chapter, reactive power compensation, programmed PWM techniques are recommended because they offer better voltage utilization and lower switching frequencies and allow the elimination of a selected number of harmonics [40]. Thus the size of the reactor, Xi, is minimized, which becomes important especially when the SSVC is working in the capacitive compensation mode.

The switching frequency depends upon harmonic content restrictions and, in practice, by the turn-off time requirements of the devices used. The commutation losses also play an important role at higher switching frequencies. Although increasing the number of pulses per half-cycle, Np, in the ac output voltages, Vab0, reduces the size of the reactor Xi, Fig. 3.5 shows that only small improvements are possible past the value of 11 pulses (i.e., 11 turn-off times per half-cycle and ten harmonics eliminated) [46]. Therefore, the Np = 11 value has been chosen for the system treated in this chapter.

The optimized stored PWM voltage waveshaping pattern shown in Fig. 3.6 is continuously applied to the six controlled switches of the PWM voltage-source inverter. Table 3.1 shows the frequency spectrum generated with this switching pattern. Inspection of this frequency spectrum confirms that the
Fig. 3.5. $X_1$ versus $N_p$ plots with various THDi values for modulation index of 1.12

Fig. 3.6. Voltage-source inverter PWM switching pattern for modulation index 1.12 and associated switching angles ($a_1=4.4$, $a_2=10.8$, $a_3=14.1$, $a_4=21.1$, $a_5=23.4$, $a_6=31.6$, $a_7=33$, $a_8=42.3$, $a_9=43.1$, $a_{10}=65.9$, $a_{11}=66.3$).
PWM scheme selected (Fig. 3.6) attenuates the low-order harmonics of the output voltage, \( V_{\text{ab}} \). Figure 3.7 shows programmed PWM switching patterns for different values of modulation index.

<table>
<thead>
<tr>
<th>Order</th>
<th>Amplitude</th>
<th>Order</th>
<th>Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>29</td>
<td>0.177</td>
</tr>
<tr>
<td>5</td>
<td>0.11</td>
<td>31</td>
<td>0.044</td>
</tr>
<tr>
<td>7</td>
<td>0.56</td>
<td>35</td>
<td>34.07</td>
</tr>
<tr>
<td>11</td>
<td>0.35</td>
<td>37</td>
<td>32.4</td>
</tr>
<tr>
<td>13</td>
<td>0.11</td>
<td>41</td>
<td>4.29</td>
</tr>
<tr>
<td>17</td>
<td>0.146</td>
<td>43</td>
<td>1.79</td>
</tr>
<tr>
<td>19</td>
<td>0.225</td>
<td>47</td>
<td>1.85</td>
</tr>
<tr>
<td>23</td>
<td>0.72</td>
<td>49</td>
<td>0.5</td>
</tr>
<tr>
<td>25</td>
<td>0.1</td>
<td>53</td>
<td>0.233</td>
</tr>
</tbody>
</table>

### TABLE 3.1
FREQUENCY SPECTRUM OF VOLTAGE WAVEFORM ASSOCIATED WITH THE SWITCHING PATTERN

3.4 Power Circuit Design

The design data presented in this section have been obtained for the SSVC worst-case operating conditions. This worst-case operating point occurs while supplying rated leading reactive power. Thus the dc voltage, \( V_{\text{dc}} \), and the ac output currents are at a maximum value. Moreover, the design is carried out under the following assumptions:

i) The three ac mains voltages are balanced and distortion-free.

ii) The inverter switching elements are ideal.

iii) The filter components are ideal.

iv) The force-commutated voltage-source inverter is delivering rated leading reactive power.

v) The inverter switching patterns are as shown in Fig. 3.6.
Fig. 3.7. Voltage-source inverter switching pattern with different modulation index values (Np = 11). (a) M = 0.6 (b) M = 0.8 (c) M = 1 (d) M = 1.1 (e) M = 1.12 (f) M = 1.14.
Design data are expressed in per unit with respect to the following base:

\[ V_{\text{base}} = V_{\text{an}}, \quad \text{the rated value of the ac mains line to neutral voltage,} \]

\[ I_{\text{base}} = I_{\text{al}}, \quad \text{the rated value of the fundamental component of the force-commutated voltage-source inverter output line current} \, I_{\text{a}(t)}. \]

### 3.4.1 Design of the Synchronous Link Reactor

The design of the synchronous link reactor, \( X_{\text{i}} \), is performed with the constraint that under rated leading var compensation the THDi of the ac current is less than 5%. Also, it is assumed that the dc voltage, \( V_{\text{dc}} \), is ripple free.

The minimization of the reactor, \( X_{\text{i}} \), for a given THDi is important—especially for leading var compensation. For this operating condition, the smaller the size of \( X_{\text{i}} \) the larger the amount of reactive power that can be transferred from the SSVC system to the load. Thus, the compensator’s effectiveness is increased and since the dc voltage is reduced, the voltage stresses across the switches and the dc capacitor are lower.

Figure 3.8 shows the single phase equivalent circuit for the inverter at mains frequency and for harmonic components.

![Diagram](image)

**Fig. 3.8.** Analytical model of output filter for leading var compensation. (a) Single phase equivalent output filter circuit at fundamental frequency. (b) Single phase equivalent output filter circuit for harmonics.
From Fig. 3.8(a)

\[ V_{ao1} = V_{an} + jI_{a1}X_1 \]  \hspace{1cm} (3.4)

with

\[ V_{ao1} = \frac{4V_{dc}}{\sqrt{2}} \left[ 2 \sum_{j=1}^{n+1} (-1)^{j+1} \cos(\alpha_j) - 1 \right] \]  \hspace{1cm} (3.5)

where \( n \) is the number of harmonics to be eliminated and \( \alpha_j \) the switching angle values shown in Fig. 3.6. From Fig. 3.8(b)

\[ V_{aok} = jkX_1I_{ak} \]  \hspace{1cm} (3.6)

The total harmonic distortion of the ac mains current is given by

\[ \text{THDi} = \frac{100}{I_{a1}} \left\{ \sum_{k=1}^{\infty} I_{aok}^2 - I_{a1}^2 \right\}^{1/2} \]  \hspace{1cm} (3.7)

then from (3.6) and (3.7)

\[ \text{THDi} = \frac{1}{I_{a1}X_1} \left\{ \sum_{k=5}^{\infty} \left( \frac{V_{aok}}{k} \right)^2 \right\}^{1/2} \]  \hspace{1cm} (3.8)

with

\[ \frac{V_{aok}}{k} = \frac{4V_{dc}}{\sqrt{2}} \left[ 2 \sum_{j=1}^{n+1} (-1)^{j+1} \cos(k\alpha_j) - 1 \right] \]  \hspace{1cm} (3.9)

Replacing (3.9) in (3.8) gives
\[
\text{THDi} = \frac{4V_{dc}}{2 \sqrt{\frac{2}{\pi X_{1a1}}}} \left\{ \sum_{k=5}^{\infty} \frac{1}{k^4} \left( 2 \sum_{j=1}^{n+1} (-1)^{j+1} \cos(k\alpha_j) - 1 \right)^2 \right\}^{1/2}
\] (3.10)

From (3.3), and considering the inverter phase to neutral voltage \(V_{an1}\), the dc voltage, \(V_{dc}\), is given by

\[
V_{dc} = 2 \sqrt{\frac{2}{M}} V_{an1}
\] (3.11)

Taking \(V_{an}\) and \(I_{a1}\) equal to 1 pu (according to the base values already defined), and replacing (3.11) in (3.4) gives:

\[
V_{dc} = 2 \sqrt{\frac{2}{M}} (1+X_1)
\] (3.12)

and replacing (3.12) in (3.10)

\[
\text{THDi} = \frac{4(1+X_1)}{\pi X_1 M} \left\{ \sum_{k=5}^{\infty} \frac{1}{k^4} \left( 2 \sum_{j=1}^{n+1} (-1)^{j+1} \cos(k\alpha_j) - 1 \right)^2 \right\}^{1/2}
\] (3.13)

Finally, solving (3.13) for \(X_1\)

\[
X_1 = \frac{4 \left\{ \sum_{k=5}^{\infty} \frac{1}{k^4} \left( 2 \sum_{j=1}^{n+1} (-1)^{j+1} \cos(k\alpha_j) - 1 \right)^2 \right\}^{1/2}}{\pi(M)\text{THDi}-4 \left\{ \sum_{k=5}^{\infty} \frac{1}{k^4} \left( 2 \sum_{j=1}^{n+1} (-1)^{j+1} \cos(k\alpha_j) - 1 \right)^2 \right\}^{1/2}}
\] (3.14)

The apparent power required by the ac output filter is given by

\[
S_{li} = X_{il\text{rms}}^2
\] (3.15)
with

\[ l_{\text{rms}}^2 = \sum_{k=1}^{\infty} l_{\text{sk}}^2 \]  

(3.16)

From (3.7)

\[ \sum_{k=1}^{\infty} l_{\text{sk}}^2 = l_{\text{d1}}^2 \left( 1 + \text{THDi}^2 \right) \]  

(3.17)

Finally,

\[ S_{\text{Li}} = X_{\text{Lia}}^2 \left( 1 + \text{THDi}^2 \right) \]  

(3.18)

Table 3.2 summarizes the reactor design data associated with the SSVC system for different values of modulation index and different values of THDi. Table 3.2 also presents the reactor design data for an SSVC system using a six step voltage-source inverter. Table 3.2 shows that the proposed SSVC structure yields significant reduction in the output reactor as compared to structures that utilize a six step inverter. It is noted that for the same THDi, the lower the modulation index used for the switching pattern, the higher are the values required for the ac output filter and for the inverter ac output voltage. This becomes clear as soon as one examines the base values and the definition of the modulation indexes used in this design.

3.4.2. Semiconductor Switch Ratings

For rated capacitive operating conditions, THDi = 5% and different modulation index values, the design data presented in Table 3.3 includes rms and peak current ratings for each gate commutated switch as well as peak
### TABLE 3.2
DESIGN DATA FOR THE REACTOR X₁ (pu)

<table>
<thead>
<tr>
<th>THDi</th>
<th>X₁</th>
<th>SI₁</th>
<th>Va₀, rms</th>
<th>Va₀₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.03</td>
<td>4.59</td>
<td>4.59</td>
<td>7.82</td>
<td>5.59</td>
</tr>
<tr>
<td>0.05</td>
<td>0.97</td>
<td>0.97</td>
<td>2.76</td>
<td>1.97</td>
</tr>
<tr>
<td>0.07</td>
<td>0.54</td>
<td>0.54</td>
<td>2.16</td>
<td>1.54</td>
</tr>
</tbody>
</table>

**PWM INVERTER**

- Modulation Index = 0.8
- Modulation Index = 1.0
- Modulation Index = 1.12
- Modulation Index = 1.14

<table>
<thead>
<tr>
<th>THDi</th>
<th>X₁</th>
<th>SI₁</th>
<th>Va₀, rms</th>
<th>Va₀₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.03</td>
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<td>1.65</td>
<td>3.38</td>
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</tr>
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<td>0.61</td>
<td>2.04</td>
<td>1.59</td>
</tr>
<tr>
<td>0.07</td>
<td>0.37</td>
<td>0.37</td>
<td>1.74</td>
<td>1.37</td>
</tr>
<tr>
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<td>0.86</td>
<td>0.86</td>
<td>2.51</td>
<td>1.86</td>
</tr>
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<td>0.05</td>
<td>0.38</td>
<td>0.38</td>
<td>1.60</td>
<td>1.38</td>
</tr>
<tr>
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<td>0.25</td>
<td>0.25</td>
<td>1.45</td>
<td>1.25</td>
</tr>
<tr>
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<td>0.75</td>
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<td>0.35</td>
<td>0.35</td>
<td>1.54</td>
<td>1.35</td>
</tr>
<tr>
<td>0.07</td>
<td>0.23</td>
<td>0.23</td>
<td>1.40</td>
<td>1.23</td>
</tr>
<tr>
<td>SIX STEP INVERTER</td>
<td>0.05</td>
<td>12.8</td>
<td>12.9</td>
<td>14.4</td>
</tr>
</tbody>
</table>

### TABLE 3.3
VOLTAGE-SOURCE INVERTER SWITCH RATINGS (pu)

<table>
<thead>
<tr>
<th>Modulation Index</th>
<th>Peak Current</th>
<th>rms Current</th>
<th>Peak Forward Blocking Volt.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM INVERTER</td>
<td>0.8</td>
<td>1.414</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>1.0</td>
<td>1.414</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>1.12</td>
<td>1.414</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>1.14</td>
<td>1.414</td>
<td>0.5</td>
</tr>
<tr>
<td>SIX STEP INVERTER</td>
<td>1.0</td>
<td>1.414</td>
<td>0.5</td>
</tr>
</tbody>
</table>
reverse blocking voltages. The type of gate commutated switch (i.e. power fet, bipolar, GTO, etc.) is not specified, because the choice of the switches depends on the voltage and current levels.

All the relevant data is presented in summary form (in pu with respect to the ac base values) in Table 3.3. Table 3.3 shows that the modulation index of the switching pattern only affects the voltage stresses on the switches.

3.4.3 DC Capacitor Design

The dc capacitor is designed with the constraint that with rated leading var compensation, the ripple factor for the direct voltage, $V_{ac}$, is less than 5%. Also, it is assumed that the ac line output currents are balanced and sinusoidal. Hence

$$R_v = \frac{\left\{ \sum_{k=0}^{\infty} V_{ck}^2 \right\}^{1/2}}{V_{dc}} \tag{3.19}$$

where

$$V_{ck} = \frac{X_c}{k} I_{ck} \tag{3.20}$$

and

$R_v$ is the ripple factor,

$V_{ck}$ is the rms value of the $k^{th}$ voltage harmonic across the dc capacitor,

$V_{ac}$ is the average value of the direct voltage across the dc capacitor,

$I_{ck}$ is the rms value of the $k^{th}$ current harmonic through the dc
capacitor,

\[ X_c \] is the impedance of the dc capacitor at mains frequency (i.e., \( X_c = 1/(120\pi C) \ Ω \)),

and replacing (3.20) in (3.19) gives

\[
X_c = \frac{R_v V_{dc}}{\left[ \sum_{k=6, 12}^\infty \frac{I^2_{ek}}{k^2} \right]^{1/2}} \tag{3.21}
\]

The current across the dc capacitor, \( I_{dc} \), is given by the equation

\[
I_{dc}(t) = \sum_{k=1}^\infty A_k \sin(kt) I_a(t) + \sum_{k=1}^\infty A_k \sin(kt-120k) I_b(t) + \sum_{k=1}^\infty A_k \sin(kt+120k) I_c(t) \tag{3.22}
\]

where (a), (b), and (c) are the switching functions of the force-commutated voltage-source inverter obtained with the PWM switching pattern shown in Fig. 3.6, and \( I_a(t) \), \( I_b(t) \), and \( I_c(t) \) are the inverter ac output line currents. The Fourier coefficients of the switching function are given by

\[
A_k = \frac{4}{k\pi} \left[ 2 \sum_{j=1}^{n+1} (-1)^{k+1} \cos(k\alpha_j) - 1 \right] \tag{3.23}
\]

Using the trigonometric identity
\[
\sin(\alpha)\sin(\beta) = \frac{1}{2} \left[ \cos(\alpha-\beta) - \cos(\alpha+\beta) \right]
\]  
(3.24)

for each term in (3.22) and then developing for different values of \( k \)

\[
I_{ck}(t) = \frac{3}{\sqrt{2}} \left\{ \sum_{k=5,12}^{\infty} (A_{k-1} + A_{k+1}) \sin(kt) \right\}
\]  
(3.25)

Finally,

\[
X_c = \frac{2 R v \cdot V_{dc}}{3 \left\{ \sum_{k=5,12}^{\infty} \frac{1}{k^2} (A_{k-1} + A_{k+1})^2 \right\}^{1/2}}
\]  
(3.26)

The apparent power allowed in the capacitor is given by

\[
S_{dc} = V_{dc, \text{rms}} I_{dc, \text{rms}}
\]  
(3.27)

Table 3.4 summarizes the design data for the dc capacitor for different values of modulation index and THDI and for the SSVC using a PWM voltage-source inverter and a SSVC scheme using a six step inverter.

3.5 Design of the \( \delta \) Control Unit

Reactive power control is achieved by varying the voltage across the dc capacitor through the \( \delta \) control scheme shown in Fig. 3.3. The derivation of the SSVC transfer function relating the phase-shift angle \( \delta \) with the voltage across the dc capacitor is presented in Appendix A, [47]. The analysis presented in Appendix A is based on the synchronous machine theory [48]. Equation (3.28) gives the normalized SSVC open loop transfer function and
<table>
<thead>
<tr>
<th>PWM INVERTER</th>
<th>THDi</th>
<th>Xc</th>
<th>Sc dc</th>
<th>Vdc</th>
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<tr>
<td>Modulation Index = 0.8</td>
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<td>32.89</td>
<td>8.22</td>
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<td></td>
<td>0.05</td>
<td>11.60</td>
<td>2.90</td>
<td>6.97</td>
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<td></td>
<td>0.07</td>
<td>9.08</td>
<td>2.27</td>
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<tr>
<td>Modulation Index = 1.0</td>
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<td>3.12</td>
<td>7.50</td>
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<tr>
<td></td>
<td>0.05</td>
<td>6.24</td>
<td>1.88</td>
<td>4.52</td>
</tr>
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<td></td>
<td>0.07</td>
<td>5.33</td>
<td>1.61</td>
<td>3.86</td>
</tr>
<tr>
<td>Modulation Index = 1.12</td>
<td>0.03</td>
<td>7.26</td>
<td>1.95</td>
<td>4.69</td>
</tr>
<tr>
<td></td>
<td>0.05</td>
<td>5.41</td>
<td>1.45</td>
<td>3.49</td>
</tr>
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<td></td>
<td>0.07</td>
<td>4.87</td>
<td>1.31</td>
<td>3.15</td>
</tr>
<tr>
<td>Modulation Index = 1.14</td>
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<td>7.08</td>
<td>1.81</td>
<td>4.35</td>
</tr>
<tr>
<td></td>
<td>0.05</td>
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<td></td>
<td>0.07</td>
<td>4.95</td>
<td>1.26</td>
<td>3.04</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SIX STEP INVERTER</th>
<th>THDi</th>
<th>Xc</th>
<th>Sc dc</th>
<th>Vdc</th>
</tr>
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<td>25.8</td>
<td>12.7</td>
<td>30.6</td>
<td></td>
</tr>
</tbody>
</table>
Fig. 3.9 shows the corresponding SSVC open loop frequency response.

\[
\frac{\Delta V_{dc}}{\Delta \delta} = \frac{3(M)^2 \omega L}{X_C s^3 + 2 r X_1 X_C s^2 + \left[ \frac{X_1}{X_C} + \frac{r^2}{X_C} + 3 M^2 X_1 \right] s + 2(M)^2 r} \quad (3.28)
\]

The controller required for the compensation of the dc voltage or equivalent reactive power loop can be deduced from the SSVC open loop frequency response shown in Fig. 3.9. This figure shows that the compensator response can be approximated by a first order response in the frequency range of interest (i.e., below 377 rad/s). Using a standard design technique, the PI controller parameters are chosen as follows:

i) The integral term I, of gain Ki, and the transfer function Ki/s, is required to obtain steady-state accuracy, since the system has a finite dc gain resulting from the losses.

ii) The proportional term P, of gain KP, allows the required closed loop bandwidth to be achieved.

The block diagram of the closed loop system is shown in Fig. 3.10. The corresponding approximate transfer function obtained from (3.28) can be written as:

\[
G(s) = \frac{\Delta V_{dc}}{\Delta \delta} = \frac{A_o}{s \omega_b + 1} \quad (3.29)
\]

where Ao is the inverter open loop gain. The open loop break frequency \( \omega_b \) results from the combined effect of R, L, and C (i.e., time constants RC, L/R, and period \( \sqrt{LC} \)). The transfer function of the PI controller is given by
Fig. 3.9. Bode diagram of the SSVC open loop frequency response. (a) Magnitude response. (b) Phase response.
\[ G_c(s) = K_P + \frac{K_I}{s} = \frac{s}{\omega_c} \frac{1}{\frac{s}{K_I}} \]  

(3.30)

with \( \omega_c = K_I/K_P \). The break frequency \( \omega_c \) is made equal to the open loop break frequency \( \omega_b \). The closed loop transfer function of the system is given by

\[ H(s) = \frac{K_d G_c(s) G(s)}{1 + K_m K_d G_c(s) G(s)} = \frac{K_I K_d A_o}{s + K_m K_d K_I A_o} \]  

(3.31)

![Block diagram](image)

**Fig. 3.10.** The block diagram of the SSVC closed loop control system

The required closed loop breaking frequency, \( \omega_{bc} \), is equal to

\[ \omega_{bc} = K_m K_d K_I A_o \]  

(3.32)

From (3.32)

\[ K_I = \frac{\omega_{bc}}{K_m K_d A_o} \]  

(3.33)

and from (3.30)

\[ K_P = \frac{K_I}{\omega_c} \]  

(3.34)

The practical implementation of the PI controller is shown in Fig. 3.11
and its transfer function is given by

\[
\left| \frac{V_2}{V_1} \right| = \frac{R_2}{R_1} + \frac{1}{sC R_1} \quad (3.35)
\]

Equation (3.35) has to be equal to the transfer function of the PI controller given in (3.30), so

\[ R_2 \quad \text{and} \quad K_I = \frac{1}{C R_1} \quad (3.36) \]

![Fig. 3.11. The PI controller.](image)

3.6 Influence of Compensator Parameters

The influence on system response of the dc bus capacitor value \( C \), the inductor \( L \), and the system damping represented by the equivalent resistance \( R \) are illustrated by means of the root locus shown in Figs. 3.12, 3.13, and 3.14. The characteristic \([A]\)-matrix of the SSVC system is derived from the mathematical model obtained in Appendix A and is equal to:
\[
[A] = \begin{bmatrix}
\frac{-R}{L} & \omega & \frac{-M}{L} \\
-\omega & \frac{R}{L} & 0 \\
\frac{3M}{C} & 0 & 0
\end{bmatrix}
\] (3.37)

The derivation of the SSVC characteristic [A]-matrix is presented in Appendix B. The root locus of the system is evaluated numerically by the Matlab subroutines [49]. Figures 3.12, 3.13, and 3.14 show that the open loop system is stable for all values of C, L, and R.

Conclusions concerning the influence of the compensator parameters on open loop system response and bandwidth are also drawn from these figures:

i) Decreasing the size of the dc capacitor (increasing the impedance) results in a faster response, Fig. 3.12.

ii) Decreasing the size of the ac inductor increases the system speed response, Fig. 3.13.

3.7 Analysis for Unbalanced Voltage Source Condition

The analysis presented in this section shows how unbalanced voltages in the ac mains affect the SSVC input and output current and voltage waveforms. Also, analytical results are used to obtain system design curves as a function of ac source voltage unbalance for the reactor, \(X_1\), and the dc capacitor.

3.7.1 Input and Output Waveforms Analysis

Figure 3.15 shows the equivalent circuit used in this analysis. The PWM voltage-source inverter is represented by the lossless sinusoidal voltage
Fig. 3.12. Root locus for increasing values of dc capacitor.
Fig. 3.13. Root locus for increasing values of the synchronous link reactor.
Fig. 3.14. Root locus for increasing values of the damping resistance.
sources \(v_{ao}, v_{bo}, \text{ and } v_{co}\). The voltage sources \(v_{ao}, v_{bo}, \text{ and } v_{co}\) supply only reactive power - the active power required by the load is supplied by the ac mains. Since the sum of the line to line voltages in a three-phase system is always zero, zero sequence components are never present in the line to line voltage.

The fundamental components of the inverter ac output voltages are equal to

\[
\begin{align*}
V_{ao1}(\omega t) &= V_{dc}A_1 \sin(\omega t) \\
V_{bo1}(\omega t) &= V_{dc}A_1 \sin(\omega t - 120^\circ) \\
V_{co1}(\omega t) &= V_{dc}A_1 \sin(\omega t + 120^\circ)
\end{align*}
\] (3.38)

where \(V_{dc}\) is the average value of the dc capacitor voltage and \(A_1\) is the fundamental component of the inverter switching function (see (3.23)). Equation (3.38) shows that the inverter output voltages are always balanced. For this reason no negative sequence voltage components are present at its terminals. The equivalent circuit of the SSVC for negative sequence components at fundamental frequency is shown in Fig. 3.16. The negative sequence components of the ac mains line to line voltages are given by

\[
\begin{align*}
V_{ab2} &= \frac{1}{3} \left( V_{ab} + V_{bc} + V_{ca} \right) \\
V_{bc2} &= a V_{ab2} \\
V_{ca2} &= a^2 V_{ab2}
\end{align*}
\] (3.39)

and

\[
a = 1 / 120^\circ
\] (3.40)

Figure 3.16 shows that the negative sequence components of the line currents are limited only by \(X_l\). The negative sequence components of the
Fig. 3.15. Three-phase equivalent circuit for voltage unbalanced analysis.

Fig. 3.16. Three phase equivalent circuit for negative sequence components
output currents are equal to

\[ I_{ad2} = \frac{V_{a02}}{jX_1} \]
\[ I_{be2} = \frac{V_{b02}}{jX_1} \]
\[ I_{cf2} = \frac{V_{c02}}{jX_1} \]  

(3.41)

The fundamental component of the inverter output currents are given by

\[
\begin{bmatrix}
I_{ad} \\
I_{be} \\
I_{cf}
\end{bmatrix} =
\begin{bmatrix}
1 & 1 & 1 \\
1 & a^2 & a \\
1 & a & a^2
\end{bmatrix}
\begin{bmatrix}
I_{ado} \\
I_{اد1} \\
I_{ad2}
\end{bmatrix}
\]  

(3.42)

where \( I_{ado} \), \( I_{اد1} \), \( I_{ad2} \), are the zero, positive, and negative sequence components of the inverter output currents, with \( I_{اد1} = I_{ fas} / 1^\circ \). The inverter dc current is obtained by multiplying the ac output currents by the respective switching functions (see (3.22)). For unbalanced ac output currents the expression for the dc currents becomes

\[ I_{dc}(\omega t) = I_{dc} + \sum_{k=2}^{\infty} I_{dck} \cos(k\omega t + \theta_k) \]  

(3.43)

Equation (3.43) shows that ac current unbalance generates a second order harmonic in the dc current and dc voltage frequency spectra. The second order dc current harmonic generated by the ac mains voltage unbalance results from the interaction of the fundamental component of the switching functions with the fundamental component of the unbalanced ac output currents. Thus, the magnitude of the dc current second harmonic depends on the degree of the
ac current unbalance and on the modulation index of the switching function. The general expression is

$$I_{dc2}(\omega t) = \frac{-A_1}{2} \left\{ I_{a2}\cos(\omega t-\phi_a) + I_{b2}\cos(2\omega t+120-\phi_b) + I_{c2}\cos(2\omega t-120-\phi_c) \right\}$$  \hspace{1cm} (3.44)$$

The presence of $I_{dc2}$ in the dc side of the inverter is of concern because its low frequency and relative large amplitude can increase considerably the dc ripple voltage. This in turn influences the size of the dc capacitor required to maintain the dc ripple voltage within acceptable limits. A second order harmonic in the dc voltage also generates uncharacteristic low frequency harmonics in the inverter ac output voltages. The inverter output voltage is given by

$$V_{ao}(\omega t) = \frac{1}{2} V_{dc}(t) \sum_{j=1}^{\infty} A_j\sin(j\omega t)$$ \hspace{1cm} (3.45)$$

where

$$V_{dc}(t) = V_{dc} + \sum_{k=2}^{\infty} V_{dc(k)}\cos(k\omega t+\theta_k)$$ \hspace{1cm} (3.46)$$

Replacing (3.46) in (3.45) and then using the trigonometric identities yields

$$V_{ao}(\omega t) = \frac{1}{2} V_{dc} \sum_{j=1}^{\infty} A_j\sin(j\omega t) +$$

$$\frac{1}{4} \sum_{k=2}^{\infty} V_{dc(k)} \left\{ \sum_{j=1}^{\infty} A_j\sin[\omega t(k+j)+\theta_k] - \sum_{j=1}^{\infty} A_j\sin[\omega t(k-j)+\theta_k] \right\}$$ \hspace{1cm} (3.47)$$
The average value, \( V_{ac} \), defines the fundamental component of the ac output voltage, \( V_{ao} (\omega t) \), and the unwanted high frequency harmonics. These high frequency harmonics can be easily minimized by the selection of an appropriate PWM technique. However, the interaction between the second order harmonic of the dc voltage and the fundamental component of the switching function creates a third order harmonic in the inverter ac output voltages which increases the total harmonic distortion of the input current significantly. From (3.47)

\[
V_{ao} (\omega t) = \frac{1}{4} V_{dc2} A_1 \sin(3\omega t + \Theta_1)
\]  

(3.48)

### 3.7.2 System Design Considerations

The use of PWM techniques yields a significant reduction in the value of the ac reactor and in the dc capacitor as compared to the six-step inverter configurations [50]. However, the smaller the values of \( L \) and \( C \), the more sensitive the system becomes to input voltage unbalances. Further, the smaller the value of \( X_l \), the larger the negative sequence component of the ac output current thus increasing the value of the second harmonic component of the dc voltage. Also, a small dc capacitor (i.e., large value of \( X_c \)) will generate a large second harmonic in the dc voltage.

With appropriate values for \( X_l \) and \( X_c \), significant improvements can be achieved in the THDi and \( R_v \) for unbalanced ac mains voltage conditions. Figure 3.17 and 3.1f show system design curves as a function of the ac mains voltage unbalance for the ac reactor, \( X_l \), and the dc capacitor reactance, \( X_c \). Figure 3.17 gives the value of \( X_l \) and \( X_c \) that will keep \( R_v \) equal to 5\% for ac voltage unbalances of 5\% and 10\%. Figure 3.18 shows the THDi of the inverter
Fig. 3.17. DC capacitor reactance ($X_c$) versus synchronous link reactor ($X_l$).

Fig. 3.18. THDi versus synchronous link reactor ($X_l$) plots.
ac current for the given values of Xi and Xc obtained from Fig. 3.17. These
curves are valid for a programmed PWM technique, with a modulation index
equal to 1.12, and 10 harmonics eliminated (see Fig. 3.6).

3.8 Simulated PWM Inverter Results

To verify key analytical results, the aforementioned SSVC system
specified in section 3.4 was tested by simulation on an HP-9836
microcomputer. A dedicated computer program was employed to generate the
switching functions and the steady-state voltage and current waveforms.
Simulated results are presented next for the case of balanced and unbalanced
ac mains voltages.

3.8.1 Simulated waveforms for balanced ac mains voltages

Figures 3.19 and 3.20 show the current and voltage waveforms for the SSVC
system for rated leading and lagging var compensation. In particular, Figs.
3.19(a) and 3.20(a) show the inverter phase to neutral output voltage and the
corresponding inverter line to line output voltages are shown in Fig. 3.19(b)
and 3.20(b). Figure 3.19(c) and 3.20(c) depict the ac line current. From
these figures it is apparent that the ac mains current has very low total
harmonic distortion. This result is in close agreement with the specified THD
limits. Figures 3.19(d) and 3.20(d) illustrate the current through the dc
capacitor. Finally, Figs. 3.19(e) and 3.20(e) show the phase to neutral
source voltage, the fundamental component of the inverter output phase to
neutral voltage, and the fundamental component of the ac output current for
leading and lagging var compensation.
Fig. 3.19. PWM voltage-source inverter simulated waveforms for leading var compensation ($X_l = 0.38$ pu, $X_c = 5.41$ pu) and balanced source voltages. (a) Inverter phase to neutral output voltage $V_{ao}$. (b) Inverter line to line output voltage $V_{abo}$. (c) AC line current $I_a$. (d) Inverter input dc current $I_{dc}$. (e) Phase to neutral source voltage, $V_{an}$, fundamental component of inverter output voltage $V_{ao}$, and ac output line current, $I_a$. 
Fig. 3.20. PWM voltage-source inverter simulated waveforms for lagging var compensation ($X_l = 0.38 \text{ pu}$, $X_c = 5.41 \text{ pu}$) and balanced source voltages. (a) Inverter phase to neutral output voltage $V_{ao}$. (b) Inverter line to line output voltage $V_{abo}$. (c) AC line current $I_a$. (d) Inverter input dc current $I_{dc}$. (e) Phase to neutral source voltage, $V_{an}$, fundamental component of inverter output voltage $V_{ao}$, and ac output line current, $I_a$. 
3.8.2 Simulated waveforms for unbalanced ac mains voltage

Figure 3.21 shows the simulated results for 5% unbalanced ac source voltages applied to the SSVC designed for balanced source voltage conditions (i.e., \( X_l = 0.383 \) pu and \( X_c = 5.4 \) pu). Figures 3.21(a) and 3.21(b) show the effect of a 5% voltage unbalance in the inverter ac output voltage and current. Figure 3.21(b) shows that the ac current has a significant third order order harmonic. Figure 3.21(c) shows that the dc voltage waveform contains a second order harmonic component which leads to the third harmonic in the output voltages and currents. Finally, Fig. 3.22 shows the effects of the ac source voltage unbalance (5%) on a SSVC system which has been designed using Figs. 3.17 and 3.18 (i.e., \( X_l = 0.43 \) pu and \( X_c = 3.6 \) pu). In this case the distortion in the dc voltage and output current and voltage waveforms is lower (\( R_v=0.05 \) and THDi=4.6%).

3.9 Design Example

To illustrate the significance and facilitate the use of the theoretical results obtained in sections 3.4 and 3.5 the following example is given.

3.9.1 Power Circuit

The SSVC system has the following specifications

\[
\begin{align*}
V_{an} \text{ (rms)} & \quad \text{ac supply} \quad (60 \text{ V}) \\
S & \quad \text{SSVC output apparent power} \quad (800 \text{ VA}) \\
f_{ac} & \quad \text{ac mains frequency} \quad (60 \text{ Hz})
\end{align*}
\]

From these data the following base values are defined

- 1 pu voltage \( V = 60 \text{ V} \).
- 1 pu apparent power \( S = 267 \text{ VA} \).
Fig. 3.21. PWM voltage-source inverter simulated waveforms for leading var compensation and 5% unbalanced ac source voltage ($X_l = 0.383 \text{ pu}$ and $X_c = 5.4 \text{ pu}$). (a) Inverter output line to line voltage $V_{ab}$. (b) AC line output current $I_a$. (c) Line current frequency spectrum. (d) Inverter dc voltage $V_{dc}$. (e) DC voltage frequency spectrum.
Fig. 3.22. PWM voltage-source inverter simulated waveforms for leading var compensation and 5% unbalanced ac source voltage ($X_i = 0.43$ pu and $X_c = 3.6$ pu). (a) Inverter output line to line voltage $V_{ab,c}$. (b) AC line output current $I_a$. (c) Line current frequency spectrum. (d) Inverter dc voltage $V_{dc}$. (e) DC voltage frequency spectrum.
1 pu current \( I = 4.4 \text{ A.} \)
1 pu impedance \( Z = 13.5 \text{ Ω.} \)
1 pu frequency \( f = 60 \text{ Hz.} \)

Therefore, using tables 3.2, 3.3 and 3.4 for \( M = 1.12 \) and \( \text{THDi} = 0.05 \), the specifications of the components of the SSVC system are given by:

i) ac filter

\[ X_l = 5.171 \text{ Ω} \quad L_1 = 13.7 \text{ mH} \quad S_L = 103 \text{ VA} \]

ii) semiconductors

peak current = 6.2 A  
rms current = 2.2 A  
peak reverse blocking = 210 V
voltage

iii) dc capacitor

\[ X_c = 73 \text{ Ω} \quad C = 36 \text{ μF} \quad S_{Sc} = 388 \text{ VA} \]

### 3.9.2 δ Control Unit

The SSVC system transfer function obtained with the values calculated in section 3.6.1 is equal to

\[
\frac{\Delta V_{dc}}{\Delta \delta} = \frac{1468}{(j\omega \tau_1 + 1) \left[ 1 + \frac{2\xi}{\omega_n} j\omega + \left( \frac{j\omega}{\omega_n} \right)^2 \right]} \tag{3.49}
\]

where \( \tau_1 = 0.03226 \text{ s} \), \( \xi = 0.0223 \), and \( \omega_n = 967.29 \text{ rad/s} \). Figure 3.23 shows that the break frequency corresponding to a 3 db drop is equal to \( f_b = 5 \text{ Hz.} \)

The value of the dynamic resistance parameter \( R \) was estimated from the measurements of the inductors, wires, capacitor resistances, and the dynamic resistance of the switches at the steady-state operating point. The equivalent dynamic resistance value referred to the ac side was found to be
\( R = 0.3 \ \Omega \) (0.022 pu). Since at low frequency the var compensator behaves as a first order system, the transfer function is reduced to

\[
\frac{\Delta V_d}{\Delta \delta} \approx \frac{A_0}{s/\omega_b + 1}
\]  

(3.50)

Figure 3.24 shows the experimental open loop transfer function obtained with the SSVC prototype unit as specified in section 3.9.1. From Fig. 3.24

\[ A_0 = 1200 \ \text{V/rad} \quad \text{and} \quad \omega_c = 35 \ \text{rad/s} \]

The required SSVC closed loop breaking frequency is selected at 10 Hz. From (3.33) with \( K_m = 0.01 \) and \( K_d = 0.032 \), \( K_l \) is equal to

\[ K_l = 163.62 \ \text{rad/s} \]

and from (3.34)

\[ K_p = 4.34 \]

3.10 Experimental Results

To verify key predicted results, an experimental 2 kVA unit has been implemented. Steady state waveforms obtained for balanced and unbalanced ac mains voltage conditions are displayed in Figs. 3.25, 3.26, 3.27, and 3.28. Transient results are shown in Fig. 3.28.

3.10.1 Experimental Results for Balanced AC Mains Voltages

Steady state results obtained with this SSVC experimental unit are depicted in Figs. 3.25 and 3.26. Figures 3.25(a) and 3.26(a) show the inverter ac output line current \( I_a(\omega t) \) with the phase to neutral source voltage \( V_{an}(\omega t) \) for leading and lagging var compensation. Figures 3.25(b) and 3.26(b) show the inverter output current \( I_a(\omega t) \) and its frequency spectrum.
Fig. 3.23. Bode plot of the theoretical SSVC open loop frequency response

Fig. 3.24. Experimental SSVC open loop frequency response.
From these figures it is apparent that $I_a(\omega t)$ has a low THD. This result is in close agreement with the THDi $\leq 5\%$ specification that has been included in the design of the SSVC structure. Also, Figs. 3.25(a) and 3.26(a) show that the inverter generates or absorbs mainly reactive power. Figures 3.25(c) and 3.26(c) illustrate the experimental output line to line voltage, $V_{ab}(\omega t)$. Finally, Figs. 3.25(d) and 3.26(d) show the voltage and current across and through a bidirectional switch for leading and lagging mode of operation. Comparison between simulated results (Figs. 3.19 and 3.20) and experimental waveforms shows that they are in close agreement.

3.10.2 Experimental Results for Unbalanced AC Mains Voltages

The effects of a 5% ac mains voltage unbalance in the experimental SSVC unit are shown in Figs. 3.27 and 3.28. Figure 3.27(a) shows the inverter ac output current with its frequency spectrum. The frequency spectrum shows that the third order harmonic generated by the second harmonic component of the dc voltage. Figure 3.27(b) shows the dc voltage and its frequency spectrum. It is noted that the amplitude of the second order harmonic is significant.

Figure 3.28 shows the SSVC system waveforms again for 5% ac mains voltage unbalance but with $X_i = 0.43$ pu and $X_c = 3.6$ pu. Figure 3.28(a) and 3.28(b) show that the effect of the unbalance on output current and dc voltage is negligible. Comparison of figures 3.27, 3.28 and 3.21, 3.22 shows that the analysis and simulation of the SSVC system is supported by the results obtained from the prototype.

3.10.3 Dynamic Response

Figures 3.29(a) and 3.29(b) show the open loop step response to change in
Fig. 3.25. Experimental inverter voltage and current waveforms for leading var compensation and balanced ac source voltages. (a) Output line current $I_a$ (2 A/div), phase to neutral source voltage $V_{an}$ (50 V/div), $f_o =60$ Hz. (b) Inverter output current $I_a$ and its frequency spectrum. (c) Inverter output line to line voltage $V_{ab}$ (100 V/div). (d) Inverter switch current $I_s$ (2 A/div), inverter switch voltage $V_s$ (100 V/div).
Fig. 3.26. Experimental inverter voltage and current waveforms for lagging var compensation and balanced ac source voltages. (a) Output line current $I_a$ (2 A/div), phase to neutral source voltage $V_{an}$ (50 V/div), $f_0$ =60 Hz. (b) Inverter output current $I_a$ and its frequency spectrum. (c) Inverter output line to line voltage $V_{ab}$ (100 V/div). (d) Inverter switch current $I_s$ (2 A/div), inverter switch voltage $V_s$ (100 V/div).
Fig. 3.27. Experimental inverter voltage and current waveforms for leading var compensation and 5% unbalanced ac source voltage. ($X_l = 0.38$ pu and $X_c = 5.4$ pu). (a) Inverter ac output current $I_a$ and respective frequency spectrum. (b) Inverter dc voltage $V_{dc}$ and its respective frequency spectrum.

Fig. 3.28. Experimental inverter voltage and current waveforms for leading var compensation and 5% unbalanced ac source voltage. ($X_l = 0.43$ pu and $X_c = 3.6$ pu). Inverter ac output current $I_a$ and its respective frequency spectrum. (b) Inverter dc voltage $V_{dc}$ and its respective frequency spectrum.
Fig. 3.29. Experimental open loop system response for step change in the phase-shift angle $\delta$. a) DC voltage response. b) Inverter ac current response.

Fig. 3.30. Experimental dc voltage closed loop response for step change in the load power factor. (a) DC voltage response for a step change from a leading to lagging load power factor. (b) DC voltage response for a step change from a lagging to a leading load power factor.
the angle $\delta$ and the load power factor. The response time from 0 to 95% of the steady-state value is $T_r = 100$ms. This corresponds to a system bandwidth of 5 Hz if a first order system is assumed. These figures agree with the result of the frequency response test (Fig. 3.24). Furthermore, these results are in agreement with these derived from the theoretical model and confirm the validity of the approach. Based on the use of the model, a PI controller was designed to achieve a closed loop bandwidth of 10 Hz. Figures 3.30(a) and 3.30(b) show the dc voltage closed loop response for a step change in the var command signal. The experimental results confirm the theoretical design. Good overall performance is obtained.

3.11 Conclusion

This chapter provides a comprehensive analysis of a synchronous solid-state var compensator. The proposed system is designed for applications that require displacement power factor correction leading or lagging with a slow response time (i.e., harmonics excluded). The design problem has been approached considering balanced and unbalanced ac mains voltage conditions. Pulse width modulation is used as a means of reducing the size of reactive components. A model was derived for the analysis of the solid-state var compensator operating with the $\delta$ phase-shift angle control method. The model allows the effect of the system parameters on the open loop performance to be analyzed. Predicted results are compared to experimental results for a laboratory set-up and show good agreement. They confirm the validity of the proposed model. The model is also used for the design of a var controller for closed loop operation. The close agreement between analytical and experimental results proves the feasibility of the proposed SSVC system.
CHAPTER 4
CURRENT CONTROLLED SYNCHRONOUS VAR COMPENSATORS

4.1 Introduction

Chapter 3 shows that the transient response of the synchronous solid-state var compensator, when working with the $\delta$ control loop, depends on the values of the dc capacitor, C, and the output reactor, $X_l$. By decreasing the values of $X_l$ and C the time response of the SSVC is reduced (see Figs. 3.12 and 3.13). However, harmonic restrictions on the line currents and the dc voltage determine the values required for $X_l$ and C thus fixing the minimum time response of the system. The transient response of the SSVC can be improved with the addition of a current control loop. Moreover, a current control loop provides inherent overcurrent protection for the system.

This chapter presents and analyzes the current controlled synchronous solid-state var compensator. The scheme shown in Fig. 4.1 differs from previously discussed approaches [19], [20], [51]-[53] in the following ways:

i) It uses a current control technique which allows leading or lagging reactive power compensation with a fast response time (below half a cycle of the ac supply).

ii) Current control is achieved with a constant switching frequency which produces a uniform switching pattern resulting in fixed current harmonic components.

iii) Direct overcurrent protection is provided increasing the system reliability.

The treatment of the compensator includes the principles of operation and the design of the power and the control circuits. The transient and
steady-state performance of the proposed var compensator is simulated using a standard electronics circuit simulation package.

4.2 Principles of Operation

The operating principles of the current controlled var compensator proposed in this chapter are described with the help of the control system block diagram shown in Fig. 4.2. The control system consists of a current control unit, a dc voltage control circuit, and a gating signal generator. A brief functional description of each of these units is given in the next 3 subsections.

4.2.1 Current Control Unit

The current control unit forces the line current of the inverter to follow a sinusoidal reference waveform which is phase-shifted by almost 90° (leading or lagging) with respect to the corresponding phase-to-neutral voltage. Any value of reactive power can be supplied or absorbed by changing the amplitude and the sign of the inverter current reference waveform. The required line current is generated by changing the inverter output voltage through a modulation index control.

4.2.2 Voltage Control Unit

The dc voltage control unit keeps the voltage across the dc capacitor equal to a constant reference voltage. Keeping the dc voltage constant simplifies the voltage control scheme, but it increases the switching stresses, especially for lagging var compensation (low modulation index). The higher stresses occur because the narrow pulses generated in the gating
Fig. 4.1. The current controlled synchronous solid-state var compensator.

Fig. 4.2. Block diagram of the control system.
signals require the switches to turn on and turn off at a faster rate. However, this problem can be solved by using two reference signals. For leading var compensation the reference voltage is equal to a maximum value, \( V_{\text{ref max}} \), while for lagging var compensation the reference voltage is changed to a minimum value, \( V_{\text{ref min}} \). By introducing two different voltages across the dc capacitor the need for narrow switching pulses (low modulation index) is reduced. Thus, a general switching function composed of wider pulses and having a modulation index close to one is used and the resulting switching stresses are lower.

The voltage across the dc capacitor is controlled by adjusting the small amount of real power absorbed by the inverter. The real power required by the inverter is controlled by phase-shifting the reference current waveform by plus or minus \( \alpha \) degrees with respect to the 90° (leading or lagging) steady-state operating point. The real power absorbed by the inverter is given by

\[
P = 3V_{\text{ao}} I_1 \sin(\alpha)
\]  

(4.1)

4.2.3 Gating Signal Generator

A constant switching frequency is achieved by comparing the current error signal with a triangular reference waveform. The purpose of introducing the triangular waveform is to stabilize the inverter switching frequency by forcing it to be constant and equal to the frequency of the triangular reference. The proposed method can be explained by considering the hysteresis technique plus the addition of a fixed frequency triangular waveform inside the imaginary hysteresis window (Fig. 4.3). If the reference current, \( I_{\text{ref}} \),
is higher than the generated current, $I_{gen}$, the error waveform is positive and when compared with the triangular waveform it results in a positive pulse. This pulse will then turn on an inverter bottom switch that will increase the corresponding output line current. In the same way, if $I_{ref} < I_{gen}$, the error waveform is negative and the gating signals are adjusted so that the line current decreases (a top switch is turned on). The slope of the error signal is chosen to be always smaller than the slope of the triangular waveform in order to ensure that an intersection between the two signals exists. Thus, the current error signal is forced to remain between the maximum and the minimum of the triangular waveform and as a result the line current follows the reference closely. Moreover, since the error between $I_{ref}$ and $I_{gen}$ is always kept within the positive and negative peaks of the triangular waveform, the system has an inherent overcurrent protection. However, a large variation in the reference current will generate a large error signal which can be higher than the amplitude of the triangular waveform. In this case there will not be an intersection between the error and the triangular waveform, thus the switching pattern will not change until the error is reduced and a new intersection occurs.

The minimum amplitude of the triangular waveform is determined by the maximum slope of the error which is in turn fixed by the maximum slope of the line current. The maximum slope of the line current is determined by the maximum instantaneous voltage drop across the inductor and the value of the inductance. Reducing the amplitude of the triangular waveform below this value will generate multiple crossing between the current error and the triangular signals thus disturbing the operation of the inverter [54].

The harmonic content of the inverter output voltage, $V_{so}$, is nearly
Fig. 4.3. Principles of operation of the proposed current control technique
independent of the amplitude of the modulating triangular wave. However, the dominant harmonic frequency of \( V_{ao} \) is determined by the frequency of the triangular waveform. As a result, lower order harmonics in \( V_{ao} \) are negligible. Also, since the switching frequency is usually higher than the line frequency, the effect of any phase or frequency drift in the triangular waveform is negligible, thus, in practice, no synchronization is needed for the triangular waveform with respect to the current reference. Moreover, the switching frequency does not need to be an integer multiple of the line frequency [55].

Table 4.1 shows the frequency spectrum of the inverter output voltage, \( V_{ao} \). Since the gating signals are generated from the intersection of a triangular carrier waveform superimposed on a sinusoidal wave, the frequency spectrum of \( V_{ao} \) is similar to the frequency spectrum obtained with the sinusoidal PWM technique [56].

4.3 Power Circuit Design

The inclusion of the current control loop alters the stresses on the system components as compared with the SSVC scheme presented in Chapter 3. Although the current control loop improves the compensator time response, it generates an output voltage with a frequency spectrum worse than that of selective harmonic elimination PWM technique used in the previous chapter. It also results in transient overvoltages across the dc capacitor. The design procedure presented in this section takes these considerations into account so that the system components can be rated appropriately.

The component ratings presented here have been obtained with the following assumptions.
i) The ac source voltages are balanced and distortion-free.

ii) The inverter switches and the filter components are ideal.

iii) The inverter is delivering rated leading reactive power (i.e., the inverter output voltage is maximum).

iv) The dc voltage reference is constant and equal to \( V_{r_{\text{max}}} \).

The design data are expressed in pu with respect to the following base:

\[ V_{\text{base}} = V_{\text{an}}, \text{ the rated rms value of the ac mains line to neutral voltage,} \]

\[ I_{\text{base}} = I_{\text{a1}}, \text{ the rated rms value of the fundamental component of the inverter output current.} \]

4.3.1 Design of the synchronous link reactor

The design of the synchronous reactor, \( X_1 \), is performed with the constraint that under rated leading var compensation the THDi is less than 5%. Also, it is assumed that the dc voltage is ripple-free and the modulation index is one.

The large THD of the inverter output voltage, \( V_{ao} \), requires an increased value of \( X_1 \) in order to keep the line current distortion below 5%. However, a large value of \( X_1 \) increases the dc voltage and reduces the range of compensation. This problem can be solved by increasing the inverter switching frequency. Figure 4.4 shows the reactor design curve for different switching frequencies. The value of \( X_1 \) obtained from Fig. 4.4 ensures a THDi below 5%.

The value of \( X_1 \) is calculated from the following equation

\[
X_1 = \frac{V_{dc}}{2 \sqrt{2} \cdot \text{THDi}} \left[ \sum_{k}^\infty \left( \frac{V_{aok}}{k} \right)^2 \right]^{1/2}
\]  \hspace{1cm} (4.2)

where \( V_{dc} \) is the dc voltage, \( V_{aok} \) is the peak value of the \( k^{\text{th}} \) inverter
TABLE 4.1
FREQUENCY SPECTRUM OF THE VOLTAGE WAVEFORM

<table>
<thead>
<tr>
<th>Order k</th>
<th>Amplitude (pu)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.0</td>
</tr>
<tr>
<td>ft-2</td>
<td>0.32</td>
</tr>
<tr>
<td>ft+2</td>
<td>0.32</td>
</tr>
<tr>
<td>2ft-b</td>
<td>0.18</td>
</tr>
<tr>
<td>2ft+b</td>
<td>0.18</td>
</tr>
<tr>
<td>3ft-4</td>
<td>0.16</td>
</tr>
<tr>
<td>3ft+4</td>
<td>0.16</td>
</tr>
</tbody>
</table>

\[ b = \begin{cases} 
1 & \text{if } ft \text{ is an odd number} \\
2 & \text{if } ft \text{ is an even number} 
\end{cases} \]

Fig. 4.4. Design values for the synchronous link reactor.
output voltage harmonic component, and \( k \) is the order of the harmonic component.

4.3.2 Design of the dc capacitor

Under steady-state operating conditions the dc voltage control loop keeps the dc voltage constant. However, transient changes in the reactive power command signal (i.e., changes in the inverter line current amplitude) generate voltage fluctuations across the dc capacitor. The amplitude of these voltage fluctuations can be controlled effectively with an appropriate dc capacitor value.

An overvoltage is created when the inverter line currents are forced to reduce their amplitude, or when they are forced to change from a 90° leading to a 90° lagging phase-shift. On the other hand, an undervoltage is generated when the line currents are forced to increase their amplitude, or when they are forced to change from a 90° lagging to 90° leading phase-shift. These dc voltage fluctuations are created because transiently the dc capacitor supplies (or absorb) the extra power required (or delivered) by the load and \( X_i \), and results in a current being drawn by or supplied to the dc capacitor. The amplitude of this voltage fluctuation depends on the instant at which the transient occurs and on the amount of change in the line current amplitude. The maximum overvoltage is generated when one of the line currents is forced to change from 1 pu leading to 1 pu lagging. The maximum overvoltage value is given by

\[
V_{\text{cmax}} = \frac{1}{C} \int_{\theta/\omega}^{\theta} ic(t)dt + V_{\text{dc}}
\]

where
$V_{c_{\text{max}}}$ is the maximum overvoltage across the dc capacitor,

$V_{dc}$ is the steady-state dc voltage,

$i_c$ is the instantaneous capacitor current,

$\theta_1/\omega$ are the limits of integration.

Since the dc current is defined by the product of the inverter line currents with the respective switching functions (see equation 3.22), the mean value of the dc current that generates the maximum overvoltage can be estimated by

$$\int_{t_1}^{t_2} i_c(t) dt = l_{\text{line}} \int_{\theta_1/\omega}^{\theta_2/\omega} \left[ \sin(\omega t) + \sin(\omega t + 120^\circ) \right] dt$$

(4.4)

where $\theta_1/\omega$ and $\theta_2/\omega$ are the limits of integration ($90^\circ$ and $120^\circ$) and $l_{\text{line}}$ is the peak value of the inverter line current. From (4.3)

$$C = \frac{1}{\Delta V} \int_{t_1}^{t_2} i_c(t) dt$$

(4.5)

Equation (4.5) gives the value of the dc capacitor, $C$, that will maintain the dc voltage fluctuation below $\Delta V$ pu.

Table 4.2 summarizes the capacitor design data, in pu with respect to the ac base values already defined. The design data have been evaluated considering $X_l = 0.35$ pu, $V_{dc} = 2.7$ pu, and $\Delta V_{dc} = 0.1$ pu.

**TABLE 4.2**

DESIGN DATA FOR THE DC CAPACITOR (pu)

<table>
<thead>
<tr>
<th>$X_c$</th>
<th>$V_{dc}$</th>
<th>$S_{dc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.7</td>
<td>3.82</td>
<td>1.59</td>
</tr>
</tbody>
</table>
4.4 Control Circuit Design

The design procedure for the current and voltage loops is based on the respective time response requirements. Since the transient response of the var compensator is determined by the current control loop, its time response has to be fast enough to follow the current reference waveform closely. On the other hand, the time response of the dc voltage control need not be fast and is selected to be at least 10 times slower than current loop time response. Thus, these units can be designed as two independent systems.

4.4.1 Voltage control loop

The dc voltage control is achieved by adjusting the small amount of real power absorbed by the inverter. This power is controlled by phase-shifting the inverter line current around the ±90° operating point. It should be noted that this corresponds to phase-shifting the inverter output voltage with respect to the corresponding ac source voltage. Moreover, this approach is equivalent to the δ control method presented in Chapter 3. Thus, the design of the voltage control loop can be realized following the procedure presented in section 3.5.

4.4.2 Current control loop

A PI controller is selected for the current control loop since it contributes to zero steady-state error in tracking the reference current signal [57]. Simulated results have shown that the compensator transient response is improved by adjusting the gain of the proportional part (Kp) equal to one and the gain of the integrator (Ki) equal to the frequency of the triangular waveform. From (3.36)
\[
K_P = \frac{R_2}{R_1} = 1 \quad \text{and} \quad K_I = \frac{1}{R_1 C} = f_t
\]

where \( f_t \) is the frequency of the triangular waveform.

4.4.3 Gating Signal Generator

The switching patterns are generated from the intersection between the current error signal and the triangular waveform. The minimum value for the amplitude of the triangular waveform can be readily found from the maximum instantaneous voltage drop across the reactor, \( X_1 \) (\( X_1 = \omega L_1 \)), and the value of \( L_1 \). The maximum slope of the inductor current is:

\[
\lambda = \frac{V_{an} + 0.5V_{dc}}{L_1}
\]

where \( V_{an} \) is the peak value of the ac source phase voltage and \( V_{dc} \) is the steady-state dc voltage. Therefore, the following relation gives the minimum peak amplitude of the triangular waveform for this slope.

\[
A_{min} = \frac{\lambda}{4f_t}
\]

where \( f_t \) is the frequency of the triangular waveform.

4.5 Design Example

To illustrate and facilitate the use of the theoretical results obtained in previous sections, the following example is given.

4.5.1 Power Circuit

The current controlled synchronous var compensator has the following
specifications:

\[
\begin{align*}
V_{an} & \quad \text{ac supply (rms)} \quad 120 \text{ V} \\
S & \quad \text{compensator output apparent power} \quad 12 \text{ kVA} \\
f_{ac} & \quad \text{mains frequency} \quad 60 \text{ Hz}
\end{align*}
\]

From these data the following base values are defined

1 pu voltage \( V = 120 \text{ V} \)
1 pu apparent power \( S = 4 \text{ kVA} \)
1 pu current \( I = 33.33 \text{ A} \)
1 pu impedance \( Z = 3.6 \text{ } \Omega \)
1 pu frequency \( f = 60 \text{ Hz} \)

Therefore using the design data obtained in section 4.3, the specification of the compensator power components are given by:

i) Synchronous reactor

\[
\begin{align*}
X_1 & = 1.26 \text{ } \Omega \\
L_1 & = 3.342 \text{ mH} \\
S_{L1} & = 1.4 \text{ kVA}
\end{align*}
\]

ii) dc capacitor

\[
\begin{align*}
X_c & = 6.12 \text{ } \Omega \\
C & = 433 \text{ } \mu \text{F} \\
V_{dc} & = 505 \text{ V} \\
S_{CdC} & = 6.4 \text{ kVA}
\end{align*}
\]

iii) semiconductors

\[
\begin{align*}
\text{peak current} & = 47 \text{ A} \\
\text{rms current} & = 16.7 \text{ A} \\
\text{peak reverse blocking voltage} & = 505 \text{ V} \\
\text{switching frequency} & = 2.16 \text{ kHZ}
\end{align*}
\]

4.5.2 Control circuit

The switching frequency is obtained from the design of the synchronous reactor, \( X_1 \). Also the switching frequency defines the frequency of the triangular waveform which, in turn, determines the time response of the current control loop. From (4.6) the gains of the PI controller of the
current loop are found to be:

\[ K_I = 13572 \text{ rad/s} \quad \text{and} \quad K_P = 1 \]

The minimum amplitude of the triangular waveform is obtained from (4.8) and (4.7). From (4.7)

\[ \lambda = \frac{170 + 0.5 \times 458}{3.342 \times 10^{-3}} = 119390 \text{ A/s} \]

and from (4.8)

\[ A_{\min} = \frac{119390}{4 \times 2160} = 13.82 \text{ A or 0.416 pu} \]

The design of the voltage control loop is presented in section 3.9.2.

4.6 Simulated results

The performance of the current controlled synchronous var compensator, as specified in section 4.5, was simulated using a standard electronic circuit simulation package (PSpice) [58]. The system was simulated for a steady-state and transient operating conditions.

4.6.1 Steady-state simulated waveforms

Figures 4.5(a) and 4.6(a) show the simulated inverter line current and voltage source waveforms for leading and lagging var compensation. These figures indicate that only leading and lagging reactive power is produced by the inverter. Also, from these figures it is apparent that the inverter line currents have a low THD. These results agree with the specified THD limits. The inverter line to line output voltage for leading and lagging var
compensation are shown in Figs. 4.5(b) and 4.6(b). In this case, lagging var compensation was obtained by reducing the modulation index of the inverter output voltage (i.e., the reference dc voltage signal was kept constant). Figures 4.5(c) and 4.6(c) show the current flowing through the dc capacitor for leading and lagging var compensation. The voltage across the dc capacitor for leading var compensation is shown in Fig. 4.5(d).

4.6.2 Simulated transient response

The transient performance of the proposed var compensator was tested by simulating a step change in the current reference signals while keeping the reference signal of the dc voltage constant. The step change is applied when the current reference of phase A is at its maximum value. Figures 4.7 and 4.8 show simulated results for the case in which the inverter line current (phase A) is forced to change from 1 pu leading to 1 pu lagging. In particular Figs. 4.7(a), 4.7(b) and 4.7(c) illustrate the line currents of the inverter with the respective phase to neutral source voltages. These figures proves that the compensator time response is very fast ($\tau \approx 0.3$ ms). The inverter line to line output voltage is shown in Fig. 4.8(a). Figure 4.8(b) shows the voltage across the dc capacitor at the instant the transient occurs. Figure 4.8(b) illustrates that the overvoltage generated across the dc capacitor is below 10% of $V_{dc}$. This results proves the validity of the dc capacitor design criteria. Finally, Fig. 4.8(c) shows the dc capacitor current. It is noted that the mean value of the dc current at the instant the step change occurs is not zero.
Fig. 4.5. Simulated current and voltage waveforms for steady-state operating conditions and leading var compensation. (a) Inverter line current $I_a$, and respective phase to neutral voltage. (b) Inverter output voltage $V_{ab0}$. (c) Inverter dc current $I_d$. (d) Inverter dc voltage $V_{dc}$. 
Fig. 4.6. Simulated current and voltage waveforms for steady-state operating conditions and lagging var compensation. (a) Inverter line current $I_a$, and respective phase to neutral voltage. (b) Inverter output voltage $V_{ab0}$. (c) Inverter dc current $I_{d}$. 
Fig. 4.7. Simulated current and voltage waveforms for transient operating conditions (step change from 1 pu leading to 1 pu lagging). (a) Inverter line current $I_a$, with phase to neutral source voltage $V_{an}$. (b) Inverter line current $I_b$ with phase to neutral source voltage $V_{bn}$. (c) Inverter line current $I_c$ with phase to neutral source voltage $V_{cn}$.
Fig. 4.8. Simulated current and voltage waveforms for transient operating conditions (step change from 1 pu leading to 1 pu lagging). (a) Inverter line to line output voltage $V_{ab}$. (b) Inverter dc voltage $V_{dc}$. (c) Inverter dc current $I_{dc}$. 
4.7 Conclusions

In this chapter a synchronous solid-state reactive power compensator with current control has been presented and analyzed. The proposed system is designed for applications that require power factor correction, leading or lagging with a fast response time (below half a cycle of the ac supply). A method for generating a reactive current with a constant switching frequency has been presented. The design procedures for the power and the control circuit have also been discussed. Finally, steady-state and transient simulated results obtained with the PSpice simulation package proved the feasibility of the proposed scheme.
CHAPTER 5

A POWER FACTOR COMPENSATOR AND HARMONIC SUPPRESSOR SYSTEM

5.1 Introduction

Nonlinear loads require not only power factor correction but also the elimination of the current harmonic components. Active power filters are used to compensate for distortion power factor in systems supplying nonlinear loads. However, active power filters have the disadvantages of requiring high switching frequency, a complex control system, and a special circuit to calculate, in real time, the harmonic components generated by the load. In this chapter, a novel power factor and harmonic suppressor system is presented and analyzed. This scheme employs a PWM voltage-source inverter (Fig. 5.1) and has two important features. First, it can maintain a near-unity mains input power factor without sensing and computing the associated reactive power, and second, it can substantially reduce any line current harmonics generated by nonlinear types of load.

Also, by changing the reference signal in the voltage control unit, the proposed scheme can operate as a voltage regulator. As a voltage regulator, the system maintains a constant and balanced voltage across the load independently of the voltage fluctuations generated by the ac mains. Moreover, as compared with the synchronous solid-state approach, the proposed topology has the following advantages:

i) It can compensate for voltage unbalance generated by the ac source.

ii) It reduces the load short-circuit current.

iii) It presents smaller voltage stresses across the switches and the dc
capacitor — especially for inductive load compensation.

In particular, this chapter discusses the proposed scheme in terms of principles of operation and power system design. Finally, predicted results are verified experimentally.

![Diagram](image)

Fig. 5.1 The power factor and harmonic suppressor configuration

5.2 Principles of Operation

The principles of operation of the proposed solid state compensator, Fig. 5.1, are discussed next with the help of Figs. 5.2, 5.3, and 5.4. In the equivalent circuit shown in Fig. 5.2, \( V_{an} \) represents one of the three balanced phase to neutral voltages of the ac source and \( V_{an1} \) the fundamental component of the PWM voltage-source inverter. To minimize the dumping of current and voltage harmonics on the utility lines and on the three-phase load, the ac terminals of the inverter are connected to the ac source through a reactor, \( X_1 \), and to the load through a second order low pass filter, \( X_2 \) and
Figures 5.3 and 5.4 depict the generalized phasor diagram at the fundamental frequency for a lagging and a leading ac mains power factor. At the fundamental frequency the current flowing through the filter capacitor is very small, and it is assumed that \( I_2 = I_L \).

### 5.2.1 Power Factor Compensation

Figures 5.2, 5.3, and 5.4 illustrate the following system characteristics:

1. The inverter output voltage \( V_{a0i} \) lags the ac mains voltage \( V_{an} \) by the voltage displacement angle, \( \delta \). The ac mains current, \( I_i \), lags the voltage drop \( V_i \) by 90° (assuming ideal reactor, \( X_i \)).

2. For any type of load, the ac mains power factor angle \( \alpha \), can be controlled by adjusting the amplitude of the voltage \( V_{a0i} \).

3. For a small voltage drop across the reactor, \( X_i \), the power factor of the ac mains is nearly unity and lagging if \( V_{a0i} \) is slightly lower or equal to \( V_{an} \). If \( V_{a0i} \) is slightly higher than \( V_{an} \) then the ac mains power factor value will be almost one, leading.

4. The ac mains supplies the real power required by the load and by the inverter. The reactive power is provided mainly by the voltage-source inverter.

As a result of the above characteristics, the input power factor of the ac source can be maintained at near unity leading or lagging without sensing and computing the associated reactive power component required by the load. This is done by forcing the amplitude of the voltage \( V_{a0i} \) to be slightly lower or equal to the amplitude of the voltage \( V_{an} \). The amplitude of the
Fig. 5.2. Single-phase equivalent circuit of the power factor compensator and harmonic suppressor system at fundamental frequency.

Fig. 5.3. Phasor diagram for inductive load and lagging input power factor. 
(V_{ao1} = V_{an} to achieve nearly unity power factor lagging)

Fig. 5.4. Phasor diagram for inductive load and leading input power factor 
(V_{ao1} > V_{an}).
inverter ac voltage is controlled by adjusting the dc bus voltage through small changes in the amount of real power absorbed by the inverter through a δ closed loop control. The real power absorbed by the inverter is the difference between the real power delivered by the ac source and the real power consumed by the load. The real power provided by the ac source is given by

\[ P_{ac} = \frac{V_a V_{ao1}}{X_l} \sin(\delta) \]  

(5.1)

where δ is the phase-shift between the source voltage, \( V_a \), and the fundamental component of the inverter ac voltage, \( V_{ao1} \). The control of δ is achieved by varying the reset pulse of the counter that addresses the EPROM (Fig. 5.5). Under no-load operating conditions the ac source supplies the real power corresponding to the losses of the inverter and the reactor.

![Diagram of the control unit](image)

**Fig. 5.5.** The δ phase-shift control unit

Under a load power factor fluctuation the inverter will transiently supply or absorb the extra real and reactive power required or delivered by the load [59]. If the load power factor increases, the inverter will transiently supply the extra apparent power required by the load, thereby
discharging the dc capacitor. In order to keep both the amplitude of the inverter output voltage equal to the amplitude of the corresponding ac voltage and the ac mains power factor close to unity, δ is increased and the inverter will draw more real power from the ac source restoring the dc voltage. If the load power factor decreases, the inverter will transiently absorb the extra apparent power delivered by the load thus increasing the dc voltage. To restore \( V_{ac} \) the dc capacitor is discharged by decreasing δ.

5.2.2. Voltage Regulation

Figure 5.2 shows that voltage compensation can be achieved by keeping the inverter output voltage, \( V_{ao1} \), constant. However, voltage fluctuations in the ac mains alter the amount of real power that flows into the inverter changing the value of \( V_{ac} \) [60]. For an undervoltage fluctuation in the ac source, the inverter will transiently supply the difference in the real power required by the load thereby discharging the dc capacitor. In order to keep the voltage \( V_{ao1} \) constant, δ is increased and the inverter will draw more real power from the ac source. Further, an overvoltage variation will increase the real power flowing to the inverter and charge the dc capacitor. Thus, to keep \( V_{ao1} \) constant δ is decreased.

The transient response of the converter, while working in the voltage compensation mode, depends mainly on the value of the dc capacitor. For a large dc capacitor (i.e., slow system response) the voltage compensator system will not react to fast voltage variations in the ac source thus keeping the voltage across the load constant. For slow voltage fluctuation in the ac source the δ closed loop control system shown in Fig. 5.5 will react keeping \( V_{ao1} \) constant.
5.2.3. Harmonic Compensation

Figure 5.6 shows the equivalent circuit of the solid-state compensator system connected to a nonlinear load. It is noted that the current harmonic components generated by the nonlinear load circulate mainly through the voltage source inverter. The amplitude of the current harmonic flowing through the ac source depends on the PWM switching pattern applied to the inverter and the value of the reactor $X_i$.

![Diagram of equivalent circuits](image)

(a)  (b)

Fig. 5.6. Single-phase equivalent circuit for harmonic components of the power factor and harmonic suppressor system connected to a nonlinear load. (a) Equivalent circuit for ac mains. (b) Equivalent circuit for nonlinear load.

5.2.4. Unbalanced Voltage Compensation

The proposed solid-state compensator system also compensates for voltage unbalance in the ac source since its line to line ac output voltages are by definition balanced (see 3.38). For this reason no negative sequence voltage components are present at its terminals. The equivalent circuit of the proposed voltage compensator system for negative sequence components is shown in Fig. 5.7. From this figure it is evident that the negative sequence currents generated by the unbalanced ac source voltage circulate through the inverter. The unbalanced ac output currents of the inverter generate a second
order harmonic component in the dc current. The second order harmonic component flowing through the dc capacitor increases the ripple factor of the dc voltage. This problem can be solved by selecting an appropriate dc capacitor (see Section 3.7.2). Also, the rated power of the source reactors must be increased in order to stand the overcurrent generated by the source unbalance. The overcurrent value is a function of the amount of unbalance in the source voltages.

![Fig. 5.7. Three-phase equivalent circuit for negative sequence components](image)

5.3 System Design Criteria

The design procedure for this scheme is the same as with the synchronous solid-state var compensator presented in Chapter 3. However, the ratings of the components (i.e., filters, switches, and dc capacitor) are smaller since the inverter ac output voltage in this case has to be equal to the ac mains voltage. The control logic requirement is also the same except for the fact
that it becomes simpler than the synchronous case as the reactive power
calculator unit is not required in this scheme.

The power circuit design data presented in this section have been
obtained with the following assumptions:

i) The three ac mains voltages are balanced.

ii) The three-phase load is balanced and linear.

iii) The inverter switches and filter components are ideal.

iv) The voltage-source inverter is delivering rated leading reactive
power.

v) The inverter switching pattern is as shown in Fig. 5.8. This pattern
correspond to the programmed PWM technique [40], [43]. The dominant
harmonics are the 35\textsuperscript{th} and 37\textsuperscript{th} with a switching frequency of 1.38 kHz
and amplitude equal to 0.34 pu and 0.32 pu respectively. The
fundamental component is considered as 1 pu (see Table 3.1).

Design data are expressed in pu with respect to the following base:

\[ V_{\text{base}} = V_{\text{an}}, \] the rated rms value of the ac mains line to neutral voltage.

\[ I_{\text{base}} = I_{\text{a1}}, \] the rated rms value of the fundamental component of the
inverter output line current \( I_{\text{a}}(t) \).

Fig. 5.8. Voltage-source inverter switching pattern with modulation index of
1.12 and associated switching angles in degrees (\( a_1=4.4, a_2=10.8, a_3=14.1, 
\),
\( a_4=21.1, a_5=23.4, a_6=31.6, a_7=33, a_8=42.3, a_9=43.1, a_{10}=65.9, a_{11}=66.3 \)).
Tables 5.1, 5.2 and 5.3 summarize the relevant design data for the source and load filters, the inverter switches, and the dc capacitor. The design procedure for the load filter is presented in Appendix C. A comparison with the synchronous solid-state var compensator presented in Tables 3.2, 3.3, and 3.4 reveals that the proposed scheme yields significant reduction in the voltage switches ratings (28%), ac filters (26% for X1), and dc capacitor values and sizes (28% for Xc). The reduction in the compensator components is a consequence of forcing the inverter ac output voltage to be almost equal to the ac mains voltage. Therefore, the inverter dc voltage is reduced which in turns decreases the voltage stresses across the switches and also allows the use of a smaller reactor X1 and a smaller dc capacitor.

The rated power of the proposed compensator has to be specified according with its mode of operation. If it is required to operate as a power factor compensator the converter must be capable of supplying the reactive power required by the load and by the filter reactors X1 and X2. On the other hand, if working as a voltage compensator, the reactive power required to maintain a constant voltage at the point of connection to the system is given by

\[
Q = \frac{V_{ab} \Delta V}{X_t}
\]  

(5.2)

provided that the system line to line voltage, \(V_{ab}\), does not change by more than \(\Delta V\%). Here, \(X_t\) represents the total system equivalent reactance referred to the point of connection (i.e., \(X_1\) plus any line reactance supply), and \(Q\) corresponds to the rated reactive power of the compensator system.
### Table 5.1
**Design Data for AC Output Filters (pu)**

<table>
<thead>
<tr>
<th>Source Filter</th>
<th>Load Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_1$</td>
<td>$S_{L1}$ ($L_1$)</td>
</tr>
<tr>
<td>$0.2766$</td>
<td>$0.2773$</td>
</tr>
<tr>
<td></td>
<td>$X_2$</td>
</tr>
<tr>
<td></td>
<td>$0.043$</td>
</tr>
<tr>
<td></td>
<td>$S_{L2}$ ($L_2$)</td>
</tr>
<tr>
<td></td>
<td>$0.249$</td>
</tr>
<tr>
<td></td>
<td>$X_{c_f}$</td>
</tr>
<tr>
<td></td>
<td>$10$</td>
</tr>
<tr>
<td></td>
<td>$S_{c_f}$ ($C_r$)</td>
</tr>
<tr>
<td></td>
<td>$0.1318$</td>
</tr>
</tbody>
</table>

### Table 5.2
**Inverter Switch Ratings (pu)**

<table>
<thead>
<tr>
<th>Peak Current</th>
<th>rms Current</th>
<th>Peak reverse Blocking Vol.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1.414$</td>
<td>$0.5$</td>
<td>$2.53$</td>
</tr>
</tbody>
</table>

### Table 5.3
**Design Data for DC Capacitor (pu)**

<table>
<thead>
<tr>
<th>$X_c$</th>
<th>$S_{dc}$</th>
<th>$V_{dc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$3.91$</td>
<td>$1.05$</td>
<td>$2.53$</td>
</tr>
</tbody>
</table>
5.4 Simulated Results

To verify key analytical results, the solid-state compensator specified in Tables 5.1, 5.2, and 5.3, was tested by simulation on a HP-9836 microcomputer. Simulated waveforms are presented next for the case of power factor compensation for linear and nonlinear loads connected to the system.

5.4.1 Simulated Waveforms for Linear Load Compensation

Simulated waveforms for the compensation of a 0.7 power factor inductive load are shown in Figs. 5.9, 5.10, 5.11, and 5.12. Figure 5.9 shows the phase to neutral source voltage waveform, $V_{an}$, and the respective input line current waveform, $I_l$. From this figure it is apparent that the input power factor of the ac mains is near unity. Figure 5.10 shows the load voltage waveform, $V_L$, and the load current waveform, $I_L$. It is noted that the load filter attenuates the harmonic components of $I_L$ and $V_L$ effectively. This result is in close agreement with the specification that has been included in the design of the load filter (THDi < 5% and THDv < 10%). Figure 5.11 shows the output current of the inverter, $I_{inv}$, waveform. Finally, simulated voltages and currents waveforms of the PWM voltage-source inverter are shown in Fig. 5.12.

5.4.2 Simulated Waveforms for Nonlinear Load Compensation

The nonlinear load is simulated by a current source with a THDi equal to 21%. Figures 5.13(a) and 5.13(b) show the phase to neutral source voltage waveform, $V_{an}$, and the respective line current waveform, $I_l$. The simulated waveform of the load current, $I_L$, is shown in Fig. 5.13(c). These results prove the effectiveness of the proposed power factor compensator and harmonic
Fig. 5.9. Simulated current and voltage ac source waveforms for linear load compensation. (a) Phase to neutral voltage $V_{an}$. (b) Line current $I_l$.

Fig. 5.10. Simulated load voltage $V_l$ and load current $I_l$ waveforms.

Fig. 5.11. Simulated inverter output current, $I_i$, for linear load compensation.
Fig. 5.12. Simulated PWM voltage-source inverter waveforms for linear load compensation. (a) Inverter phase to neutral output voltage $V_{ao}$. (b) Inverter line to line output voltage $V_{ab}$. (c) Diode current $I_d$. (d) Controlled switch current $I_t$. (e) Inverter input current $I_{dc}$. 
suppressor system. Figure 5.13(d) shows the output current of the inverter waveform, \(I_{\text{inv}}\), and finally the dc current waveform of the inverter, \(I_{\text{dc}}\), is shown in Fig. 5.13(e).

Figures 5.13(d) and 5.13(e) show that nonlinear loads contribute to higher values of harmonic components in the output and input currents of the inverter. Low frequency harmonics generated by nonlinear loads are reflected to the dc side of the inverter. These harmonics increase the ripple factor of the dc voltage. However, they can be easily attenuated with the selection of an appropriate dc capacitor.

### 5.5 Experimental Results

In this section, the validity of the theoretical results obtained in the previous sections is verified experimentally on a 1 kVA laboratory unity with the following example.

\[
\begin{align*}
V_{\text{an}} & \quad \text{ac supply phase voltage} & \quad (60 \, \text{V}) \\
S & \quad \text{compensator output apparent power} & \quad (800 \, \text{VA}) \\
f_{\text{ac}} & \quad \text{ac source frequency} & \quad (60 \, \text{Hz})
\end{align*}
\]

Thus, from the above specifications the following base values are defined

1 pu voltage \(V = 60\, \text{V}\).

1 pu apparent power \(S = 267\, \text{VA}\).

1 pu current \(I = 4.4\, \text{A}\).

1 pu impedance \(Z = 13.5\, \Omega\).

1 pu frequency \(f = 60\, \text{Hz}\).

Therefore, using tables 5.1, 5.2, and 5.3, the specifications of the compensator components are given by:

i) ac source filter
Fig. 5.13. Simulated waveforms for nonlinear load compensation. (a) Phase to neutral source voltage $V_{an}$. (b) Source line current $i_l$. (c) Load current $i_l$. (d) Inverter output current $i_a$. (e) Inverter input current $i_{dc}$. 
\[ X_1 = 3.73 \, \Omega \quad L_1 = 9.9 \, \text{mH} \quad S_{L1} = 74 \, \text{VA} \]

ii) load filter
\[ X_2 = 0.58 \, \Omega \quad L_2 = 1.5 \, \text{mH} \quad S_{L2} = 12.6 \, \text{VA} \]
\[ X_{cr} = 135 \, \Omega \quad C_r = 20.4 \, \mu\text{F} \quad S_{cr} = 35.2 \, \text{VA} \]

iii) semiconductors
peak current = 6.2 A \quad \text{rms current} = 2.2 A
peak reverse = 152 V
blocking voltage

iv) dc capacitor
\[ X_c = 52.8 \, \Omega \quad C = 50 \, \mu\text{F} \quad V_{ac} = 152 \, \text{V} \quad S_c = 388 \, \text{VA} \]

The design of the \( \delta \) control loop is presented in section 3.9.2. Experimental results obtained with the component values derived above are shown in Figs. 5.14 - 5.18.

5.5.1 Experimental Results for Linear Load Compensation

Figure 5.14 illustrates the steady-state experimental results obtained for a 0.7 power factor inductive linear load compensation. In particular Fig. 5.14(a) shows the ac source line current with the phase to neutral source voltage. It is noted that the ac source power factor is nearly unity. Figure 5.14(b) indicates the respective frequency spectrum of the line current. Figure 5.14(c) shows the load phase to neutral voltage with the respective load current. Figure 5.14(d) illustrates the inverter output current and output voltage. Finally, Fig. 5.14(e) shows the dc input current of the inverter.

5.5.2 Experimental Results for Nonlinear Load Compensation

Figure 5.15(a) shows the ac source line current with the phase to
Fig. 5.14. Experimental results for linear load compensation. (a) Phase to neutral voltage $V_{an}$ (100 V/div), with the respective source line current $I_s$ (2 A/div). (b) Frequency spectrum of the source line current. (c) Phase to neutral load voltage $V_l$ (50 V/div), load current $I_l$ (5 A/div). (d) Inverter output current $I_i$ (5 A/div), inverter output line to line voltage $V_{ab-o}$ (100 V/div). (e) Inverter input current $I_{ac}$ (5 A/div).
neutral source voltage. Figure 5.15(b) depicts the respective frequency spectrum of the line current. Figure 5.15(c) shows the nonlinear load current with the respective frequency spectrum (Fig. 5.15(d)). Finally, Fig. 5.15(e) shows the inverter output current and the respective frequency spectrum (Fig. 5.15(f)). These figures illustrate the effectiveness of the proposed compensator system in eliminating low frequency current harmonics generated by nonlinear types of load.

5.5.3 Experimental Results for Voltage Compensation

In order to further reduce the total harmonic distortion of the load voltage, the value of the load filter capacitor was increased to 50 µF ($X_c = 4$ pu). Figure 5.16(a) shows the ac source line current with the respective phase to neutral source voltage for a 10% undervoltage compensation and a load with 0.7 lagging power factor. Figure 5.16(b) depicts the load current with the respective phase to neutral load voltage. Figure 5.17(a) shows the ac source line current with the respective phase to neutral source voltage for a 10% overvoltage compensation and a load with a 0.7 lagging power factor. Figure 5.17(b) depicts the load current with the respective phase to neutral voltages. Figure 5.16 and 5.17 illustrate that the proposed compensator maintains a constant steady state load voltage independent of the supply voltage fluctuations.

Finally, Fig. 5.18 shows the voltage waveforms for a 20% unbalance in the ac source voltage. Figure 5.18(a) shows the balanced line to line inverter output voltages. Figure 5.18(b) illustrates the unbalanced phase to neutral source voltages. These figures indicate the good performance of the compensator under unbalances in the ac supply.
Fig. 5.15. Experimental results for nonlinear load compensation. (a) Source line current $I_L$ (2 A/div) with the phase to neutral source voltage $V_{an}$ (100 V/div). (b) Frequency spectrum of the line current. (c) Load current $I_L$ (5 A/div). (d) Load current frequency spectrum. (e) Inverter output current $I_i$ (2 A/div). (f) Inverter output current frequency spectrum.
Fig. 5.16. Experimental results for 10% undervoltage compensation. (a) Source line current $I_l$ (2 A/div), phase to neutral voltage source $V_{an}$ (50 V/div). (b) Load current $I_L$ (2 A/div), phase to neutral voltage $V_L$ (50 V/div).

Fig. 5.17. Experimental results for 10% overvoltage compensation. (a) Source line current $I_l$ (5 A/div), phase to neutral voltage source $V_{an}$ (50 V/div). (b) Load current $I_L$ (2 A/div), phase to neutral voltage $V_L$ (50 V/div).
Fig. 5.18. Experimental results for 20% unbalance in ac source voltage. (a) Line to line inverter output voltages (100 V/div). (b) Phase to neutral source voltages (50 V/div).
5.6 Conclusion

In this chapter a power factor compensator and harmonic suppressor system has been presented and analyzed. The proposed scheme can also work as a voltage regulator. As a power factor compensator it can maintain a near-unity mains power factor without sensing and computing the associated reactive power component. As a voltage regulator it can maintain a constant and balanced voltage across the load independently of the voltage fluctuations generated by the ac mains. It can also substantially reduce any line current harmonics generated by nonlinear types of load. The close agreement between the analytical and the experimental results proves the validity of the analysis and the feasibility of the proposed system.
CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 Conclusions

High performance var compensators based on three-phase current-source and voltage-source PWM inverters have been described and analyzed. The proposed schemes result in more compact, flexible and more simple structures than those produced by existing var compensator topologies, while maintaining high quality ac line current waveforms. The main results of the study on high performance solid-state var compensators can be summarized as follows.

In Chapter 2 it has been shown that the proposed current-source var compensator yields significant reduction in the size of the reactive components and provides effective suppression of low order harmonics. Jittering problems caused by harmonic components in the voltage ac supply have been eliminated with the design of a control circuit that does not need a zero crossing detector for gating signal synchronism. The proposed scheme has been designed for applications in three-phase balanced systems which mainly require displacement power factor compensation (leading or lagging) with a slow response time. Performance evaluation and related design equations have been provided for the implementation of the converter and the associated control system. Finally, selected results have been verified experimentally.

In Chapter 3, three-phase synchronous solid-state var compensators have been investigated. It has been shown that they generate ac output voltages with low harmonic content so that line current harmonic components can be attenuated with a reactor. The proposed var compensator has been designed for
applications that require displacement power factor correction leading or lagging with a slow response time. The power circuit design has been approached by considering both balanced and unbalanced ac mains voltage conditions. Simulated and experimental results have shown that with an appropriate design of the synchronous link and dc capacitor the proposed SSVC system can operate under unbalanced ac mains voltage without distorting the generated line current and the dc voltage waveforms significantly. Also, a good agreement between experimental and theoretical results has been obtained proving that the derived mathematical model used for the design of the var controller for closed loop operation is valid.

A current regulated synchronous var compensator has been proposed in Chapter 4. Compared to the synchronous var compensator discussed in Chapter 3, the current regulated approach exhibits a faster transient response (below half a cycle of the ac supply) with an inherent system overcurrent protection. Current control has been obtained with constant switching frequency thus reducing switching stresses. The design procedures for the power and the control circuit have been presented. Steady-state and transient simulated results obtained with the PSpice simulation package have confirmed the feasibility of the proposed scheme.

Finally, the search for a simple var control loop has led to a novel power factor compensator structure whose principles of operation have been described in Chapter 5. The proposed scheme is able to maintain a near-unity ac source power factor without sensing and computing the associated reactive power component. It can also substantially reduce any line current harmonics generated by nonlinear types of load. Moreover, the system was able to compensate for voltage unbalances generated by the ac source. By changing the
reference signal in the voltage control unit it is shown that the system can maintain a constant and balanced voltage across the load independently of the voltage fluctuations generated by the ac mains. The different modes of operation have been discussed in detail. Theoretical and experimental results have confirmed the validity of the analysis and the feasibility of the proposed system.

In summary all the solid-state var compensator structures proposed and treated in this thesis exhibit significantly improved performance over existing var compensators. They are compact since no bulky reactive power components are necessary and they can provide leading or lagging reactive power. Also, they do not require large output filters since low frequency harmonics are effectively attenuated. Moreover, they use simple, flexible and reliable control mechanisms. Some key results have been verified experimentally in order to prove their validity.

6.2 Suggestions for Future Work

Future work could be performed in four main areas:

i) With the use of a superconducting magnetic energy storage system instead of the reactor, the PWM current-source scheme presented in Chapter 2 can be applied for active and reactive power compensation. Fast real and reactive power compensators can be used for power system stabilization or for leveling load fluctuations. Real power can be controlled by phase-shifting the inverter line currents while reactive power can be adjusted by changing the converter switching pattern modulation index.

ii) The synchronous solid-state var compensator presented in Chapter 2 was
discussed using a self controlled dc bus (i.e., a dc capacitor). The same topology can be analyzed with an independently controlled dc bus. In this case the inverter output voltages are synchronized with the ac source and the inverter losses are supplied from the dc bus. Potential advantages of this scheme include a faster transient response through a modulation index control and better reliability since the dc bus voltage is fixed.

iii) The current regulated method used with the synchronous var compensator presented in Chapter 4 can be extended for active power filter applications. Further improvements in the time response must be achieved to compensate for line current harmonic components.

iv) Also, the current regulated method presented in Chapter 4 can be used as a front-end inverter in ac/ac or ac/dc converters. In this case the reference current is kept in phase with the source voltage and the real power is controlled with the $\delta$ loop. The advantages of such a system include the elimination of the dc reactor, the capability for an instantaneous reversal of power, low harmonic distortion in the line currents, constant switching frequency, and excellent input power factor.

v) With the addition of an extra voltage control loop the transient response of the power factor compensator presented in Chapter 5 can be improved significantly. Faster transient response can be achieved by including a control loop that changes the modulation index of the switching pattern while the $\delta$ control loop maintains the dc voltage constant.
REFERENCES


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May/June 1984.


APPENDIX A

TRANSFER FUNCTION OF THE SYNCHRONOUS SOLID-STATE VAR COMPENSATOR

A.1 Mathematical Model

The mathematical model of the SSVC system is derived considering the equivalent circuit shown in Fig. A1 and based on the following assumptions:

i) The three ac source voltages are balanced and contain no harmonics.

ii) The equivalent circuit shown in Fig. A1 only takes into account the fundamental components of currents and voltages. The harmonics generated by the PWM voltage-source inverter are neglected. They do not affect the results when they are small enough, as is the case for most of the practical PWM systems [51].

iii) The system is linearized. This assumption is valid since in practice the variation of the phase-shift, \( \delta \), is small.

iv) All the losses of the system are lumped and represented by an equivalent resistance connected in series with the reactor (Fig. A1).

v) The delay introduced by the reset pulse of the EPROM (maximum one cycle) is negligible compared to the estimated system response time (on average 10 cycles).

\[ \begin{align*}
\text{AC SOURCE} & \quad R \quad L
\end{align*} \]

\[ \begin{align*}
\text{V} \quad \text{I} \quad \text{E} \quad \text{INVERTER}
\end{align*} \]

Fig. A.1. The equivalent circuit of the SSVC system.
To derive the SSVC system transfer function, the inverter output voltage is assumed to oscillate around a mean value \( \delta_0 \) between \( \delta_0 - \Delta \delta \) and \( \delta_0 + \Delta \delta \) with a frequency \( \omega_\delta \) [48]. That is

\[
\delta(t) = \delta_{\text{max}} \cos(\omega_\delta t) = \text{Re} \left[ \delta_{\text{max}} e^{j\omega_\delta t} \right] \tag{A.1}
\]

The voltage drop between the ac source voltage \( V \) and the inverter voltage \( E \) is

\[
v(t) - e(t) = L \frac{di(t)}{dt} + Ri(t) \tag{A.2}
\]

Taking the inverter voltage oscillations into account, the voltages and currents in the d-q axis are given by

\[
v(t) = \text{Re} \left[ (v_d + jv_q) e^{j(\omega_0 t + \Delta \delta)} \right]
\]

\[
i(t) = \text{Re} \left[ (i_d + ji_q) e^{j(\omega_0 t + \Delta \delta)} \right] \tag{A.3}
\]

\[
e(t) = \text{Re} \left[ (e_d + je_q) e^{j(\omega_0 t + \Delta \delta)} \right]
\]

where \( \omega_0 = 2\pi f_0 \) and \( f_0 \) is the ac source frequency. Using (A.3) in (A.2)

\[
\left[ (v_d + jv_q) - (e_d + je_q) \right] e^{j(\omega_0 t + \Delta \delta)} = R(i_d + ji_q)e^{j(\omega_0 t + \Delta \delta)} + \]

\[
L \frac{d}{dt} (i_d + ji_q)e^{j(\omega_0 t + \Delta \delta)}
\]

but
\[ L \frac{d}{dt}(i_{d} + j_{iq})e^{j(\omega_{d}t + \Delta\delta)} = L \left[ \frac{d}{dt} i_{d} + j \frac{d}{dt} i_{iq} \right] e^{j(\omega_{d}t + \Delta\delta)} + j(\omega_{o} + \frac{d}{dt} \Delta\delta) L (i_{d} + j_{iq}) e^{j(\omega_{d}t + \Delta\delta)} \]  

Replacing (A.5) in (A.4) and canceling the exponential term

\[ (v_{d} + jv_{q}) - (ed + jeq) = R(i_{d} + j_{iq}) + jL(\omega_{o} + \frac{d}{dt} \Delta\delta)(i_{d} + j_{iq}) \]

\[ + L \left[ \frac{d}{dt} i_{d} + j \frac{d}{dt} i_{iq} \right] \]  

(A.6)

Grouping the real and imaginary part of (A.6)

\[ v_{d} - ed = R i_{d} + L \frac{d}{dt} i_{d} - \omega_{o} L i_{iq} - L i_{iq} \frac{d}{dt} \Delta\delta \]  

(A.7)

\[ v_{q} - eq = R i_{q} + L \frac{d}{dt} i_{iq} + \omega_{o} L i_{id} + L i_{id} \frac{d}{dt} \Delta\delta \]  

(A.8)

The steady state equations of the system are

\[ v_{d0} - edo = R i_{d0} + L \frac{d}{dt} i_{d0} - \omega_{o} L i_{q0} \]  

(A.9)

\[ v_{q0} - eqo = R i_{q0} + L \frac{d}{dt} i_{q0} + \omega_{o} L i_{d0} \]  

(A.10)

Applying small perturbations to the variables in (A.7) and (A.8) around the operating point yields

\[ v_{d} = v_{d0} + \Delta v_{d} ; \quad ed = edo + \Delta ed ; \quad id = i_{d0} + \Delta id \]  

(A.11)

\[ v_{q} = v_{q0} + \Delta v_{q} ; \quad eq = eqo + \Delta eq ; \quad iq = i_{q0} + \Delta iq \]

Replacing (A.11) in (A.7) and (A.8) and then subtracting the corresponding
steady state equations (A.9) and (A.10)

\[
\Delta v_d - \Delta e_d = R \Delta i_d + L \frac{d \Delta i_d}{dt} - \omega L \Delta i_q - L_{i_q o} \frac{d \Delta \delta}{dt} - L \Delta i_q \frac{d \Delta \delta}{dt}
\] (A.12)

\[
\Delta v_q - \Delta e_q = R \Delta i_q + L \frac{d \Delta i_q}{dt} + \omega L \Delta i_d + L_{i_d o} \frac{d \Delta \delta}{dt} + L \Delta i_d \frac{d \Delta \delta}{dt}
\] (A.13)

Neglecting the second order terms (products of variations)

\[
\Delta v_d - \Delta e_d = R \Delta i_d + L \frac{d \Delta i_d}{dt} - \omega L \Delta i_q - L_{i_q o} \frac{d \Delta \delta}{dt}
\] (A.14)

\[
\Delta v_q - \Delta e_q = R \Delta i_q + L \frac{d \Delta i_q}{dt} + \omega L \Delta i_d + L_{i_d o} \frac{d \Delta \delta}{dt}
\] (A.15)

Subtracting (A.10) multiplied by \( \Delta \delta \) from (A.14)

\[
\Delta v_d - \Delta e_d - v_{q o} \Delta \delta + e_{q o} \Delta \delta = R \Delta i_d + L \frac{d \Delta i_d}{dt} - \omega L \Delta i_q - L_{i_q o} \frac{d \Delta \delta}{dt} - R_{i_q o} \Delta \delta - L \Delta \delta \frac{d i_{q o}}{dt} - \omega L_{i_d o} \Delta \delta
\] (A.16)

However,

\[
- L_{i_q o} \frac{d \Delta \delta}{dt} - L \Delta \delta \frac{d i_{q o}}{dt} = - L \frac{d (i_{q o} \Delta \delta)}{dt}
\] (A.17)

Repeating the same procedure for (A.15) and (A.9) and then applying the Laplace transform gives the final equations for the system

\[
\begin{bmatrix}
\Delta v_d - v_{q o} \Delta \delta \\
\Delta v_q + v_{q o} \Delta \delta
\end{bmatrix}
- \begin{bmatrix}
\Delta e_d - e_{q o} \Delta \delta \\
\Delta e_q + e_{q o} \Delta \delta
\end{bmatrix}
= \begin{bmatrix}
R + sL & -\omega L \\
\omega L & R + sL
\end{bmatrix}
\times \begin{bmatrix}
\Delta i_d - i_{q o} \Delta \delta \\
\Delta i_q + i_{q o} \Delta \delta
\end{bmatrix}
\] (A.18)
A.2 Transfer Function of the Inverter

In order to simplify the analysis, the inverter ac output voltage is considered as the reference phasor, so that the d-q components of the ac source would now seem to oscillate about their constant values \(v_{do}\) and \(v_{qo}\), with amplitudes \(\Delta v_d\), \(\Delta v_q\) and frequency \(\omega_\delta\). The phasor diagram of the perturbed system is drawn showing all the voltages in Fig. A.2.

Fig. A.2. The generalized phasor diagram of the perturbed system.

From Fig. A.2

\[
\begin{align*}
v_{do} &= V \cos(\delta) ; & \Delta v_q &= V \Delta \delta \sin(90 - \delta) = -V \Delta \delta \cos \delta \\
v_{qo} &= V \sin(\delta) ; & \Delta v_d &= V \Delta \delta \sin(90 - \delta) = V \Delta \delta \sin \delta
\end{align*}
\]  

(A.19)

Replacing (A.19) in (A.18)

\[
\begin{align*}
\Delta v_d - v_{do} \Delta \delta &= V \Delta \delta \sin \delta - V \Delta \delta \sin \delta = 0 \\
\Delta v_q + v_{qo} \Delta \delta &= -V \Delta \delta \cos \delta + V \Delta \delta \cos \delta = 0
\end{align*}
\]  

(A.20)

Also from Fig. A.2
\[ e_{d0} = E \quad \Delta e_d = \Delta E \]
\[ e_{q0} = 0 \quad \Delta e_q = 0 \]  

(A.21)

The inverter ac output voltage \( E \) is related to the dc voltage by the switching function modulation index, \( M \), so

\[ e_{d0} = (M)V_{dco} \]
\[ \Delta e_d = (M)\Delta V_{dc} \]  

(A.22)

Replacing (A.21), (A.20), and (A.19) in (A.18) yields

\[
\begin{bmatrix}
\Delta i_d - i_{q0}\Delta \delta \\
\Delta i_q + i_{d0}\Delta \delta
\end{bmatrix} =
\begin{bmatrix}
R + sL & -\omega_0L \\
\omega_0L & R + sL
\end{bmatrix}^{-1} \begin{bmatrix}
-M\Delta V_{dc} \\
MV_{dco}\Delta \delta
\end{bmatrix}
\]  

(A.23)

From (A.23)

\[
\Delta i_d = \frac{-M\Delta V_{dc}(R+SL) + \omega_0LMV_{dco}\Delta \delta + i_{q0}\Delta \delta}{L^2s^2 + 2RLs + (\omega_0L)^2 + R^2}
\]  

(A.24)

This gives the line current variations due to oscillations of the phase-shift angle \( \delta \). The power balance equation of the inverter in the time domain is

\[ 3(e_{d0} + e_{q0}) = V_{dc} I_{dc} \]  

(A.25)

Applying small perturbations around the steady state operating point

\[ 3(e_{d0} \Delta e_d)(i_{d0} + \Delta i_d) = (V_{dco} + \Delta V_{dc})(I_{dco} + \Delta I_{dc}) \]  

(A.26)
Subtracting the steady-state equation and neglecting second order terms

\[ 3(e_{dc}\Delta i_d + \Delta e_{dc}) = V_{dc0}\Delta i_{dc} + \Delta V_{acc} \Delta i_{dc} \quad (A.27) \]

\( i_{dc} \) correspond to the steady-state current component that provides the losses of the var compensator and \( i_{dc0} \) is the average value of the current through the dc capacitor (\( i_{dc0} = 0 \)). Since the losses of the SSVC are small, the product \( \Delta e_{dc} \Delta i_{dc} \) can be neglected. Replacing \( i_{dc} \) in (A.27) yields

\[ 3e_{dc}\Delta i_d = V_{dc0}C \frac{d}{dt} \Delta V_{dc} \quad (A.28) \]

and applying Laplace transform gives

\[ \Delta i_d = \frac{sC}{3M} \Delta V_{dc} \quad (A.29) \]

Combining (A.24) and (A.29) yields

\[ \frac{\Delta V_{dc}}{\Delta \delta} = \frac{3M\omega_0(L^2s^2 + 2RLs + R^2 + \omega^2L^2) + 3M^2\omega_0LV_{dc0}}{CL^2s^3 + 2RLCs^2 + (\omega^2L^2C + R^2C + 3M^2L)s + 3M^2R} \quad (A.30) \]

Using normalized values for \( R, L, C, i_{q0}, \) and \( V_{dc0} \) with respect to the base values defined in section 3.4 the transfer function becomes

\[ \frac{\Delta V_{dc}}{\Delta \delta} = \frac{3M i_{q0}(X_1s^2 + 2rX_1s + r^2 + X_1^2) + 3M^2X_1i_{dc}}{\frac{X_1^2}{X_C}s^3 + \frac{2rX_1}{X_C}s^2 + \left[ \frac{X_1}{X_C} + \frac{r}{X_C} + 3M^2X_1 \right]s + 3M^2r} \quad (A.31) \]

Figures A.3 and A.4 show the open loop frequency response of the SSVC for rated operating condition (\( i_{q0} = 1 \) pu) and for no load operating conditions.
(i_qo = 0). The steady-state current, i_qo, generates two zeros in the SSVC system transfer function. However, Figs. A.3 and A.4 show that these zeros do not affect the compensator response in the frequency range of interest (below 60 Hz). Thus, the compensator transfer function is simplified (i_qo = 0) and is equal to:

\[
\frac{ΔV_{dc}}{Δ\delta} = \frac{3M^2X_iV_{dc0}}{\frac{X_i}{X_c} s^3 + \frac{2rX_i}{X_c} s^2 + \left[ \frac{X_i}{X_c} + \frac{r^2}{X_c} + 3M^2X_i \right] s + 3M^2r}
\]

Equation (A.31) in the normalized form, is used in Chapter 3 to:

i) Analyze the effect of parameters such as C, L, and system damping R on the open loop response.

ii) Design the appropriate controller to achieve a desired closed loop step response or system bandwidth.
Fig. A3. Open loop frequency response of the SSVC for rated operating condition (l_{q0} = 1 pu). (a) Magnitude diagram. (b) Phase diagram.
Fig. A4. Open loop frequency response of the SSVC for no load operating condition ($i_q = 0$ pu). (a) Magnitude diagram. (b) Phase diagram.
APPENDIX B

THE CHARACTERISTIC [A]-MATRIX OF THE SSVC SYSTEM

The equations of the system derived in Appendix A are:

\[
\begin{bmatrix}
\Delta i_d \\
\Delta i_q \\
\end{bmatrix} = \begin{bmatrix}
R + sL & -\omega_0 L \\
\omega_0 L & R + sL \\
\end{bmatrix}^{-1} \begin{bmatrix}
-(M)\Delta V_{dc} \\
(M)\Delta V_{dco} \\
\end{bmatrix}
\]  

(B.1)

and

\[
\Delta id = \frac{sC}{3M} \Delta V_{dc}
\]  

(B.2)

From (B.1)

\[
-(M)\Delta V_{dc} = R\Delta i_d + L \frac{d\Delta i_d}{dt} - \omega_0 L \Delta i_q
\]  

(B.3)

\[
(M)\Delta V_{dco} = \omega_0 L \Delta i_d + R\Delta i_q + L \frac{d\Delta i_q}{dt}
\]  

(B.4)

or

\[
\frac{d\Delta i_d}{dt} = -\frac{R}{L} \Delta i_d + \frac{\omega_0 L}{L} \Delta i_q - \frac{M}{L} \Delta V_{dc}
\]  

(B.5)

\[
\frac{d\Delta i_q}{dt} = -\frac{\omega_0 L}{L} \Delta i_d - \frac{R}{L} \Delta i_q + \frac{M}{L} V_{dco}\delta
\]  

(B.6)

and

\[
\Delta i_d = \frac{C}{3M} \frac{d\Delta V_{dc}}{dt} \rightarrow \frac{d\Delta V_{dc}}{dt} = \frac{3M}{C} \Delta i_d
\]  

(B.7)

Finally, the SSVC equations in state space variables are
\[
\begin{align*}
\frac{d}{dt} \begin{bmatrix}
    \Delta i_d \\
    \Delta i_q \\
    \Delta V_{dc}
\end{bmatrix} &= \begin{bmatrix}
    -R/L & \omega & -M/L \\
    -\omega & -R/L & 0 \\
    3M/C & 0 & 0
\end{bmatrix} \begin{bmatrix}
    \Delta i_d \\
    \Delta i_q \\
    \Delta V_{dc}
\end{bmatrix} + MV_{dco}/L \\
\end{align*}
\] (B.8)

The characteristic \([A]-matrix\) of the SSVC is equal to

\[
\begin{align*}
\begin{bmatrix}
    -R/L & \omega & -M/L \\
    -\omega & -R/L & 0 \\
    3M/C & 0 & 0
\end{bmatrix}
\end{align*}
\] (B.9)
APPENDIX C

Load Filter Design

The function of this filter is to minimize the dumping on the load of current and voltage harmonic components generated by the inverter. The design of the LC load filter is realized with the constraints that under rated operating conditions the total harmonic distortion of the current flowing through the load is less than or equal to 5%, and the total harmonic distortion of voltage applied to the load (THDv) is less than or equal to 5%. A 0.9 power factor inductive load is considered for this design.

Figure C1 shows the single-phase equivalent load filter circuit at mains frequency. Figure C2 shows the single-phase equivalent load filter circuit for harmonic components.

Fig. C1. Single-phase equivalent load filter circuit at mains frequency.

Fig. C2. Single-phase equivalent load filter circuit for harmonic components.
From Fig. C2

\[ V_{a0k} = jkX_2I_{2k} + (RL + jkXL)I_{Lk} \]  \hspace{1cm} (C.1)

\[ -j\frac{X_c}{k} I_{ck} = (RL + jkXL)I_{Lk} \]  \hspace{1cm} (C.2)

\[ I_{2k} = I_{ck} + I_{Lk} \]  \hspace{1cm} (C.3)

From equations (C.1), (C.2), (C.3)

\[ I_{Lk} = \frac{V_{a0k} X_{cf}}{(X_{cf}RL-k^2X_2R_L) + j(kX_2X_{cf}-k^3X_2XL+kXLX_{cf})} \]  \hspace{1cm} (C.4)

and from the THDi

\[ THD_i^2 = \sum_{k=5}^{\infty} \frac{X_{cf}^2V_{a0k}^2}{(X_{cf}RL-k^2X_2R_L)^2 + (kX_{cf}X_2-k^3XLX_2+kXLX_{cf})^2} \]  \hspace{1cm} (C.5)

The values of \( X_2 \) and \( X_c \) are found by solving (C.5) for \( THD_i = 0.05 \) pu, \( RL = 0.9 \) pu and \( XL = 0.46 \) pu.

Changes in the load impedance modify the harmonic content of the load currents and voltages. However, if the load power factor decreases, the total harmonic distortion of the load current improves since the load reactance for harmonic components is larger.

The voltage drop across the filter reactance \( X_2 \) affects the load voltage regulation. This problem can be avoided by reducing the values of \( X_2 \) and \( X_c \) (i.e. bigger capacitance), or by selecting a switching pattern with a dominant component at higher frequency.