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**NEW DC BUS COMMUTATED PWM CONVERTERS**

**Essam Morad**

**A Thesis**

**in**

**The Department**

**of**

**Electrical and Computer Engineering**

**Presented in Partial Fulfillment of the Requirements**

**for the Degree of Master of Engineering**

**Concordia University**

**Montréal, Québec, Canada**

**January 1992**

**Copy Wright, Essam Morad**



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ISBN 0-315-73639-9

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## ABSTRACT

### NEW TYPES OF DC BUS COMMUTATED PWM CONVERTERS

Essam Morad

High switching frequencies are inevitable trends in the area of power converters. In addition to higher power density, they yield low acoustic noise and better control of current and voltage spectral characteristics. These high switching frequencies introduce several problems in PWM converters such as high switching losses (i.e. high  $dv/dt$  and  $di/dt$ ), and high electromagnetic interference (EMI). Resonant converter topologies operate at soft switching conditions. However, these topologies have their own inherent problems. These problems stem from the need to overrate the inverter semiconductor devices with respect to the output power, increasing the overall system cost as well as the component count.

Pulse width modulated (PWM) topologies are conceptually simpler, but they yield higher switching losses. As a result, snubber circuits have been developed to minimize the switching losses, and to improve the pwm converter's operating conditions. Considerable problems still exist such as circuit complexity, increased part count, snubber losses in the case of dissipative topologies, and required minimum circuit duty cycles because of snubber reset time.

This thesis shows that some of these problems can be solved by using dc bus commutated topologies. Dc bus commutating topologies have low circuit complexity resulting in more reliable operating conditions. However, the existing dc bus commutating topologies create some problems in PWM inverters, such as high voltage stress across the switching devices, and high subharmonics at the output.

Whereas this thesis proposes a new technique of dc bus commutated PWM converter. This innovative technique operates PWM converter at soft switching condition. Two dc bus commutating topologies are proposed and implemented in three PWM converters. The proposed dc bus commutating topologies do not cause the problems created by the existing ones. Moreover, nearly zero switching losses and low switch stresses, with relatively low circuit complexity, are achieved. Complete analysis and appropriate design examples are presented. Finally, simulation results for each of the resulting converter topologies, and experimental verification of two topologies are provided.

### ACKNOWLEDGEMENTS

I wish to express my thanks and gratitude to Dr. P. D Ziogas and Dr. G. Joos for their valuable advice and support during the course of this study.

I wish to thank all my friends and research colleagues in the power electronics lab at Concordia University for their help during the preparation of this thesis.

The financial assistance received from Concordia University is also gratefully acknowledged.

Special gratitude to my family for their support and encouragement.

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## LIST OF ACRONYMS

DC	direct current
AC	alternative current
PWM	pulse width modulation
SPWM	sine pulse width modulation
EMI	electromagnetic interference
FET	field effect transistor
MOSFET	metal oxide field effect transistor
GTO	gate turn off thyristor
IGBT	insulated gate bipolar transistor
ZCS	zero-current switching
ZVS	zero-voltage switching
VS	voltage source inverter
ZVSO	zero-voltage switching off
PLRI	parallel-loaded resonant inverter
$\Omega$	ohm
A	ampere
V	Volt
W	watt
s	second
Hz	hertz

## LIST OF PRINCIPAL SYMBOLS

$S_1, S_2, \dots$	inverter switches
$S_o$	dc bus switch
$TH_1, TH_2, \dots$	thyristors
$D_1, D_2, \dots$	diodes
$Dr_1, Dr_2, \dots$	rectifier diodes
$T$	transformer
$C_1, C_2, C_o$	dc bus capacitors
$C_c$	current commutating capacitor
$R_l$	load resistor
$L_l$	load inductor
$L_f$	output filter
$L_m$	transformer magnetizing inductor
$L_o, L_s$	$di/dt$ limiting inductors
$L_c$	current commutating inductor
$V, v$	voltages
$V_{dc}$	dc voltage
$V_{in}, V_s, V_{co}$	input dc voltages
$V_{so}, V_{s1}, \dots$	switch reverse voltages
$V_{TH1}$	thyristor reverse voltage
$V_l, V_{Lf}, \dots$	inductors voltages
$V_R, V_{RL}, \dots$	loads voltages
$V_{c1}, V_{c2}, \dots$	capacitors voltages
$V_{ca}$	ramp carrier phase A voltage



$V_{cb}$	ramp carrier phase B voltage
$V_{cc}$	ramp carrier phase C voltage
$V_{ra}$	reference phase A voltage
$V_{rb}$	reference phase B voltage
$V_{rc}$	reference phase C voltage
$V_{Ra}$	resistive load phase A voltage
$V_{La}$	inductive load phase A voltage
$I, i$	currents
$I_{dc}$	dc current
$I_{S1}, I_{S0}, \dots$	switches currents
$I_{TH1}, I_{TH2}, \dots$	thyristors currents
$I_{D1}, I_{D2}, \dots$	diodes currents
$I_{Co}, I_{C1}, \dots$	capacitors currents
$I_{Lo}, I_{Lf}, \dots$	inductors currents
$I_R, I_{RL}, \dots$	loads currents
$I_{Ra}$	resistive load phase A current
$I_{La}$	inductive load phase A current
$I_{RL(min)}$	minimum load current
$I_{RL(max)}$	maximum load current
$I_{RL(ave)}$	average load current
$\Delta I_{RL}$	ripple load current
$P$	power
$P_o, P_{out}$	output power
$S_o$	apparent output power
$\cos(\alpha)$	power factor

$W$	Energy
$f$	frequency
$\omega$	radian frequency
$f_r$	ringing frequency
$\omega_r$	radian ringing frequency
$f_o$	inverter output frequency
$f_s$	switching frequency
$F_{inv}$	inverter switching frequency
$F_{so}$	dc bus switching frequency
$D$	duty cycle
$D_{inv}$	inverter switches duty cycle
$D_{so}$	dc bus switch duty cycle
$t$	time
$A_1, A_2$	constants
$\alpha_1, \alpha_2$	phase shifts

## CHAPTER 1

### INTRODUCTION

#### 1.1 Trends in High Frequency Power Conversion

The two major application areas for power converter technology using thyristors or transistors as switching devices are:

- i) Dc/dc or ac/dc converters targeted towards general purposes such as power supply systems, and
- ii) Ac/ac or dc/ac inverters used for variable speed drives, UPS system etc.

In all areas of power electronics, the basic objectives of high frequency power conversion are to increase the performance and power density of manufactured equipment. Performance improvement can be characterized by factors such as ripple current, spectral characteristics, acoustic noise and size of the power converter. Typical applications of power supply systems using high frequency converters can be found in many areas, such as:

i) Communications:

- Telephone substations.
- Robotics and mainframe computers.
- Airborne and mobile equipment.

ii) Space industry:

- Artificial satellites.
- Space stations and vehicles.

iii) Marine industry:

- Ships and submarines.

In all the above mentioned fields high power density of the power supply systems is very important issue.

### 1.2 Problems in High Frequency Power Conversion

Converters can be mainly divided into two types, resonant converters and pulse width modulation (PWM) converters. The problems which limit the use of PWM converters, at high frequencies operation are:

- High switching losses.
- High electromagnetic interference (EMI).
- Increased copper loss due to skin effect, and
- Increased magnetic loss due to eddy current.

The problems of switching losses and EMI do not exist in resonant converters. However, additional problems exist in both types of converters when operating at high frequencies. They are:

- i) The stored charge in the converter components such as:  
Diodes, thyristors, transistors, and others.
- ii) The stray inductances of wiring connections, and stray capacitances associated with the circuit elements.

The main objectives of this thesis are to analyze the above mentioned problems in various types of converters, and to provide a new method to avoid the problems existing in PWM converters at high switching frequencies. Specifically, the following subjects are provided:

- i) A study of the switching losses in high frequency PWM converters.
- ii) A Description of the switching behavior of high frequency resonant converters, and a complete analysis and simulation results of one example of

these converters, and

iii) A propose of a new technique to provide soft switching condition, for high frequencies PWM converters. The proposed technique uses dc bus commutating subcircuits, to achieve Zero-voltage dc bus switching condition. This condition, results in the ability to operate PWM converters at high switching frequencies. The proposed dc bus commutating subcircuits are applied to three high frequency PWM inverter topologies. These topologies are comprehensively treated in this thesis.

In order to make a link between the topics treated in this presentation and to provide a brief review of soft switching converters, the next section is provided. It describes in detail the existing methods of providing soft switching conditions for the PWM converters, and shows the switching behaviors in various types of resonant converters.

### 1.3 Soft Switching Converters

As mentioned above, in order to achieve power conversion at high frequencies one must find ways to minimize switching losses and protect the switching devices. Two ways could be:

i) At high power demands, where PWM switching modes are used, soft switching conditions can be achieved by:

1) Snubber circuits, or by

2) Ac or dc bus commutating subcircuits.

ii) At low power demands soft switching can be achieved by using resonant converter topologies.

### 1.3.1 Soft Switching PWM Converters Using Snubber Subcircuits

In this section the classification of snubber networks and their principle of operation are described. The advantages and disadvantages in each type of snubber network, when applied in PWM converters, are pointed out. Snubber subcircuits can be classified as:

- a) Conventional dissipative, and
- b) Nondissipative.

Conventional dissipative snubber networks described in references [1,2,3,4,5], are shown in Fig. 1.1. The load can be connected to either the collector or emitter terminals shown. These snubbers can be divided into:

- i) Turn-on snubber and its polarized derivative form.
- ii) Turn-off snubber and its polarized derivative form, and
- iii) Combined turn-on and turn-off snubber.

The turn-on snubber uses an inductor  $L$  to limit the current stress  $di/dt$  through the switching device. For example, it limits the current through the transistor  $Q$ , which is used as a switch in Fig. 1.1. While the turn-off snubber uses a capacitor  $C$  to reduce the voltage stress  $dv/dt$  on the switch. The resistor  $R$  is used by the turn-off snubber to dissipate the capacitor  $C$  stored energy. Applying these snubbers to the PWM converter switches achieve the following:

- a) Switching loss transfer.
- b) Overvoltage suppression.
- c) Rate of rise control of voltage and current.
- d) Reduction of noise and electromagnetic interference (EMI), and
- e) Avoidance of secondary breakdown.

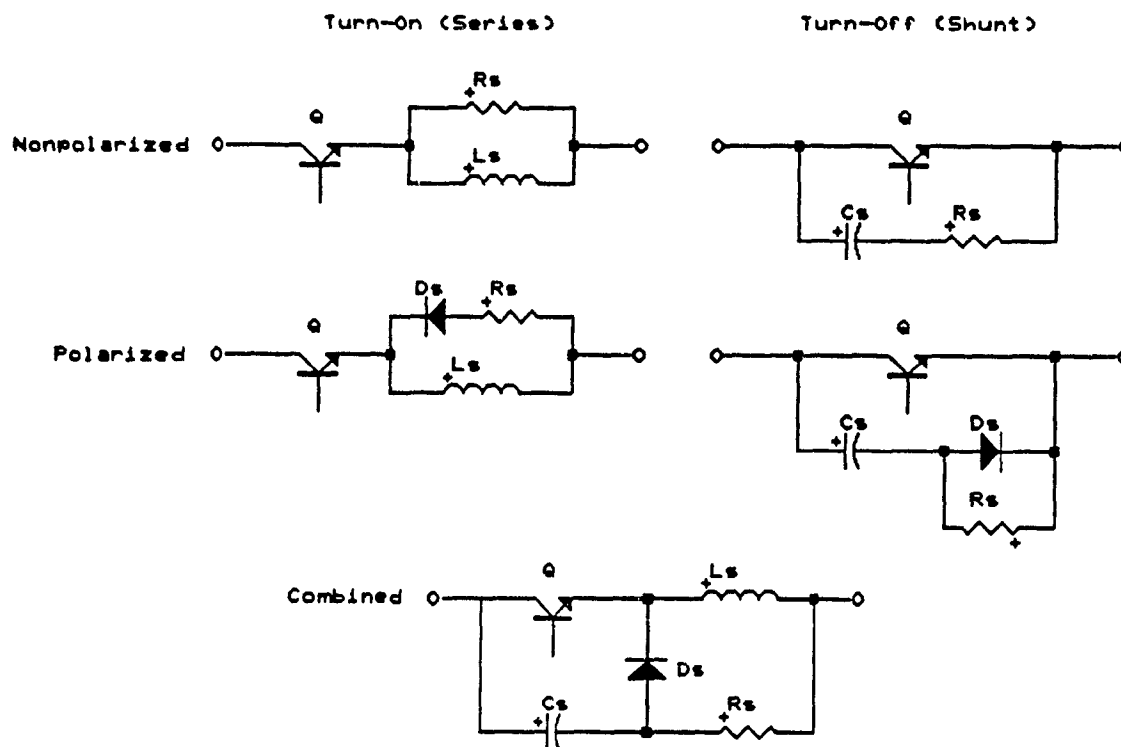


Fig. 1.1 Conventional Dissipative Snubbers

However, the system efficiencies when using these snubbers are still low. Moreover, the overall system capability is limited due to snubber reset time.

Nondissipative snubber networks have been proposed in references [6,7]. These snubbers do not use resistors to dissipate the energy stored in their storage elements (the inductors and capacitors). However, this energy can be recovered and transferred to the input source or to the load of the PWM converter topologies. Nondissipative snubbers have the same advantages as conventional ones. In addition, they improve the overall system efficiency. However, they have their own inherent problems. These problems are:

- High peak current through and voltage across the switching devices.
- High circuit complexity, and

-Minimum required duty cycle due to snubber reset time.

### 1.3.2 Soft Switching PWM Converters Using Ac or Dc Bus Commutation

This section describes in detail the various types of ac and dc bus commutation topologies proposed to provide soft switching conditions for PWM converter switches. The first subsection 1.3.2.1 introduces the most popular PWM three-phase voltage source inverter (VSI). The advantages and the limitations of this topology under high frequency hard switching operation are given. The second subsection 1.3.2.2 explains the principle of ac bus commutation approaches to provide soft switching condition for high frequency PWM three-phase VSI. The third subsection 1.3.2.3 explains the principle of dc bus commutation in high frequency PWM three-phase VSI.

#### 1.3.2.1 Introduction

The use of a PWM technique in the voltage source inverter, shown in Fig. 1.2, results in the ability to control the inverter output voltage and frequency simultaneously. In addition, harmonic minimization and increased power factor for rectifier topologies can be achieved by using PWM techniques. This topology is implemented with a wide range of power devices including MOSFETs, BJTs, IGBTs and GTOs, and is generally used in high power application up to 2 megawatts. The reasons for its popularity are:

- a) Simple power circuit structure.
- b) Minimum VA ratings of devices.
- c) Easy control, and
- d) Low cost.



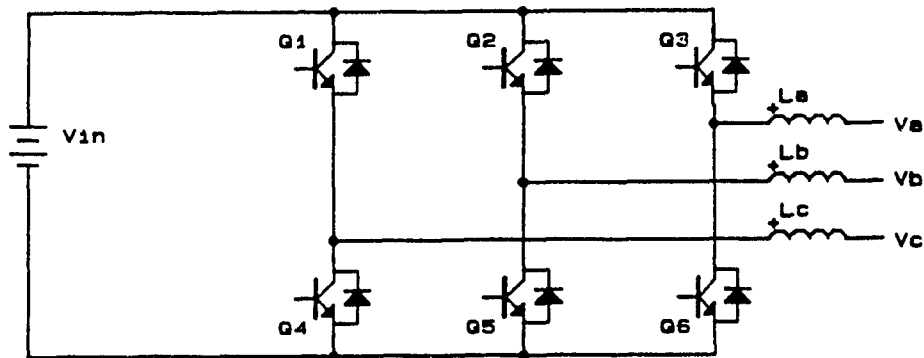


Fig. 1.2 Hard Switched Voltage Source Inverter

Continuing developments in power devices technology, especially in device switching characteristics have contributed significantly to the improvement of inverter performance. In spite of these improvements, state of art inverter technology faces substantial design problems which limit PWM inverters at high frequency operation. These limitations are:

- a) High  $dv/dt$  and  $di/dt$  stresses resulting in high switching losses and high EMI.
- b) High peak stresses in devices as a result of:
  - 1) Inductive switching, and
  - 2) Diode reverse recovery.
- c) Destructive failure modes are possible.

As in the case of dc/dc converter, the dominant problems originated from the diode stored charge and associated reverse recovery phenomena, device switching losses and the stray inductances and capacitances. Therefore, the operating frequencies of hard switching PWM VSI Fig. 1.2 are limited.

Soft switching strategies can be formulated to ease device stresses and alleviate switching losses in PWM three-phase VSI. These strategies allow a

substantial increase in the inverter switching frequencies resulting in low acoustic noise, high power density and better control of the overall system.

Ac or dc bus commutation techniques provide zero-current or zero-voltage switching condition for high frequency PWM VSI. These techniques prove to have significant advantages over snubber networks. The following two subsections explore these techniques further.

#### 1.3.2.2 Ac Bus Commutated PWM Converters

The concept of using a high frequency link as an intermediate stage in the power converter, as opposed to a dc link, was reported in the literature by Espelage and Bose in reference [8]. In these topologies there is an unrestricted relationship between the input and output frequencies.

The motivation for these types of topologies was the use of a single commutation circuit for the entire three-phase inverter. The basic elements of a high frequency resonant link operate at a frequency substantially higher than either the input or output frequency. Typical link frequencies may range from 20-to-30 KHz for multi-kilowatt applications.

Fig. 1.3 shows a series resonant high frequency ac bus commutated PWM inverter proposed by Schwarz in reference [9]. This topology works under zero-current switching condition. Fig. 1.4 illustrates the parallel resonant high frequency ac bus commutated PWM inverter. This topology accomplishes zero-voltage switching operation. Synchronizing the turn-off instants with these zero-voltage times yields the desired soft switching effect. However, the disadvantages of the series or parallel resonant high frequency ac bus commutated PWM inverter are:

- High control circuit complexity, and
- High losses in the oscillation circuits.

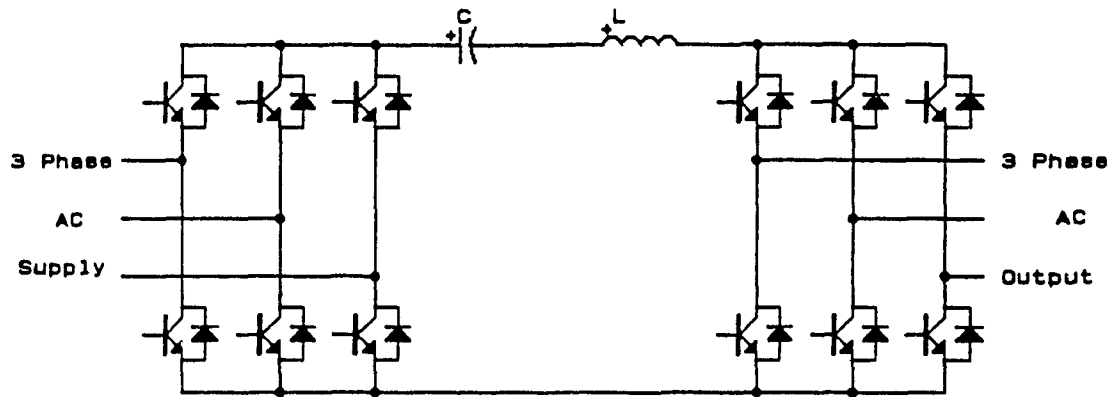


Fig. 1.3 Series Resonant High Frequency AC Bus Commutated PWM Inverter

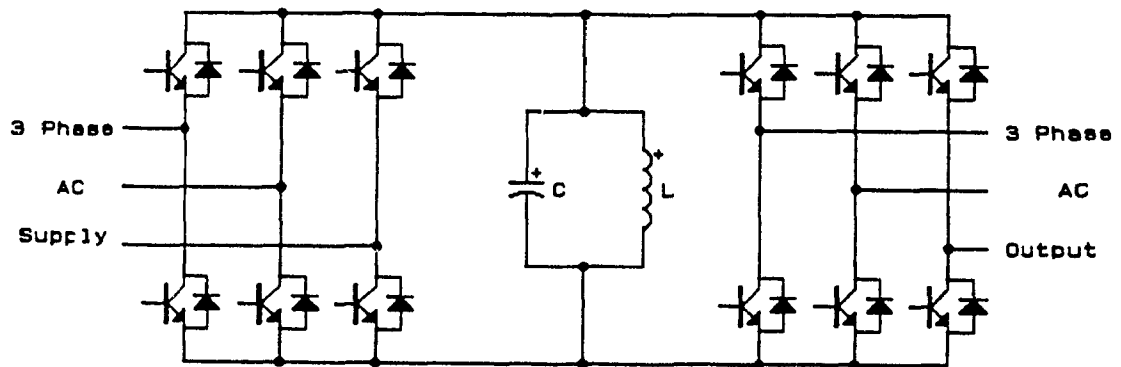


Fig. 1.4 Parallel Resonant High Frequency AC Bus Commutated PWM Inverter

### 1.3.2.3 Dc Bus Commutated PWM Converters

The resonant dc link voltage source inverter (VSI) shown in Fig. 1.5 was proposed by Divan in reference [10]. The circuit can be considered as a conventional VSI with additional LC elements. The resonant elements set up an oscillation of the dc link centered around the supply voltage ( $V_{in}$ ). The link voltage waveform oscillates between zero and  $2.5 V_{in}$ . When the link voltage waveform is at zero volts, all the devices across the dc bus may be switched with no switching losses. Maintaining the dc bus at zero volts for a finite duration ensures that the system losses will be restored through an energy storage inductor.

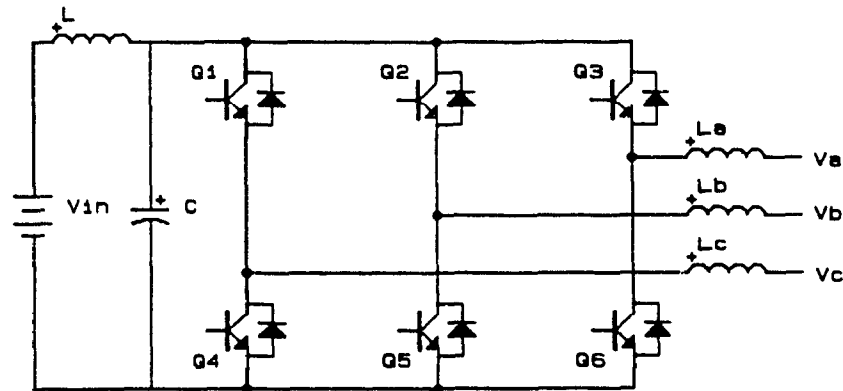


Fig. 1.5 Resonant Dc Bus Commutated Inverter

This topology is not practical especially in high power applications, since the switching devices have to be oversized. However, Alternative topologies maintaining zero-voltage switching condition have solved the above problem, but created others. A complete discussion about the existing dc bus commutation topologies is presented in chapter 2.

### 1.3.3 Soft Switching Resonant DC/DC Power Converters

This section illustrates the switching behaviors in dc/dc resonant converters. It indicates the advantages of these converters at high frequency operation and points out its limitations. Whenever high frequency power conversion is mentioned, one automatically thinks of resonant power converters. Much of the pioneering effort on this type of power converters was due to Schwarz in references [15,16]. In these topologies thyristors are used as switching devices. The advantages in adopting resonant power conversion are:

- i) Zero current switching (ZCS) when operating below the LC tank resonant frequency.
- ii) Zero voltage switching (ZVS) when operating above the frequency of the LC tank.

The above two features significantly lower the switching losses, thus permitting high frequency operation.

- iii) Low  $di/dt$  stress on components due to the non-rectangular power waveforms.
- iv) Parasitic elements can be made useful in parts of the power processing circuit.
- v) Low EMI, since the parasitic elements are generating less noise, and
- vi) Ability to control high power (but with its own set of problems).

The disadvantages or problems in the operation of these topologies include:

- a) High complexity in control circuitry, since the switching must be done at zero current or zero voltage.
- b) High peak current and/or voltage in power switches, and

c) Inefficient usage of device capabilities.

Additionally, resonant power converters confront some similar limiting elements existing in PWM power converters. They are the eddy current losses in transformer cores, and the skin effect losses in conductors.

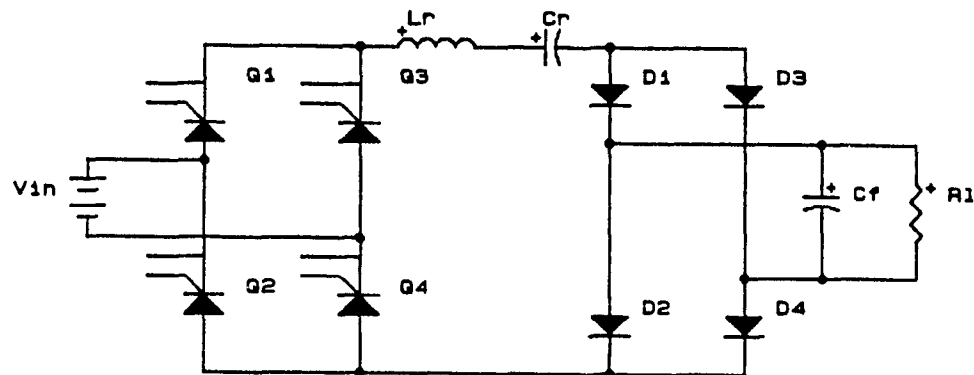


Fig. 1.6 Full-Bridge Series Resonant Dc-Dc Converter

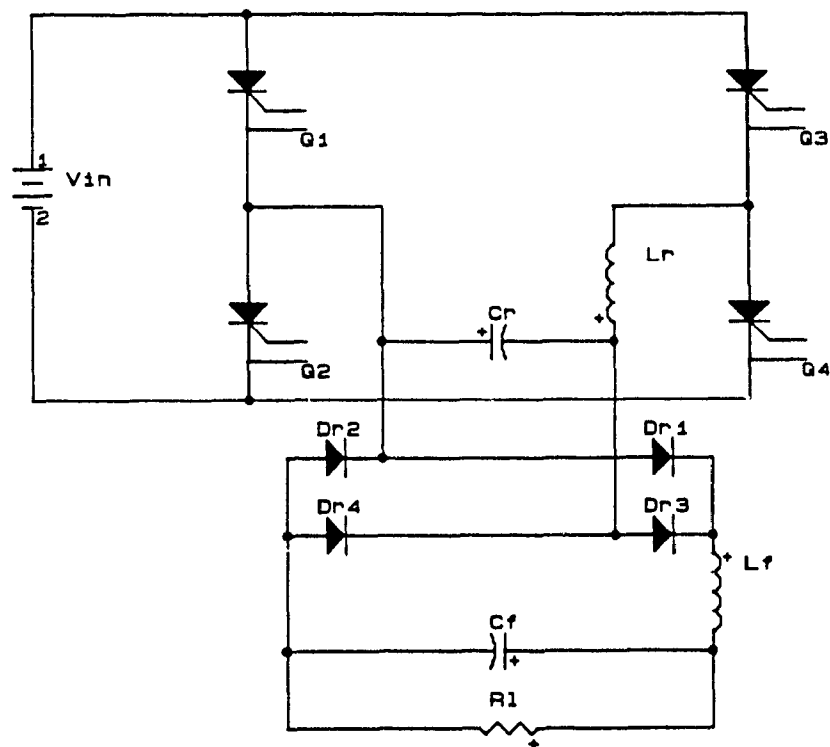


Fig. 1.7 Full-Bridge Parallel Resonant Dc-Dc Converter

Mainly, the resonant dc/dc converters can be separated into parallel and series resonant types, Figs. 1.6 and 1.7. In general terms, the series resonant dc/dc converter behaves very much like a current source and is therefore short-circuit proof and parallelable for current-sharing functions. Whereas the parallel resonant converter behaves more like a voltage source with low output short circuit capability. The series and parallel resonant types can further be classified into fixed and variable frequency types.

Although higher frequencies can now be obtained without switching loss limitations, the resonant dc/dc converter technologies did not make a major impact on the commercial scene. Since at high power demands the switching devices have to be overrated with respect to the output power. Moreover, the circuit complexity of resonant converter is high, and the overall system reliability is low.

#### 1.3.4 Soft Switching Quasi-Resonant Converters

This section illustrates the operation of quasi-resonant converters and its switching environment. It points out the circuit advantages and its limitations. The principle of the resonant-switch PWM converter, called also quasi-resonant converter, has been proposed by Liu and Lee in reference [18] and is shown in Fig. 1.8.

Replacing the power switches in the PWM converters with resonant switches a new family of converters named "quasi-resonant converters", were introduced. The LC tank circuit is always present near the power switch. It is used not only to shape the current and voltage waveforms of the power switch but also to store and transfer energy from input to output, in a manner similar to the

conventional resonant converters. The effective use of the LC elements in these topologies achieves zero-current and zero-voltage switching condition.

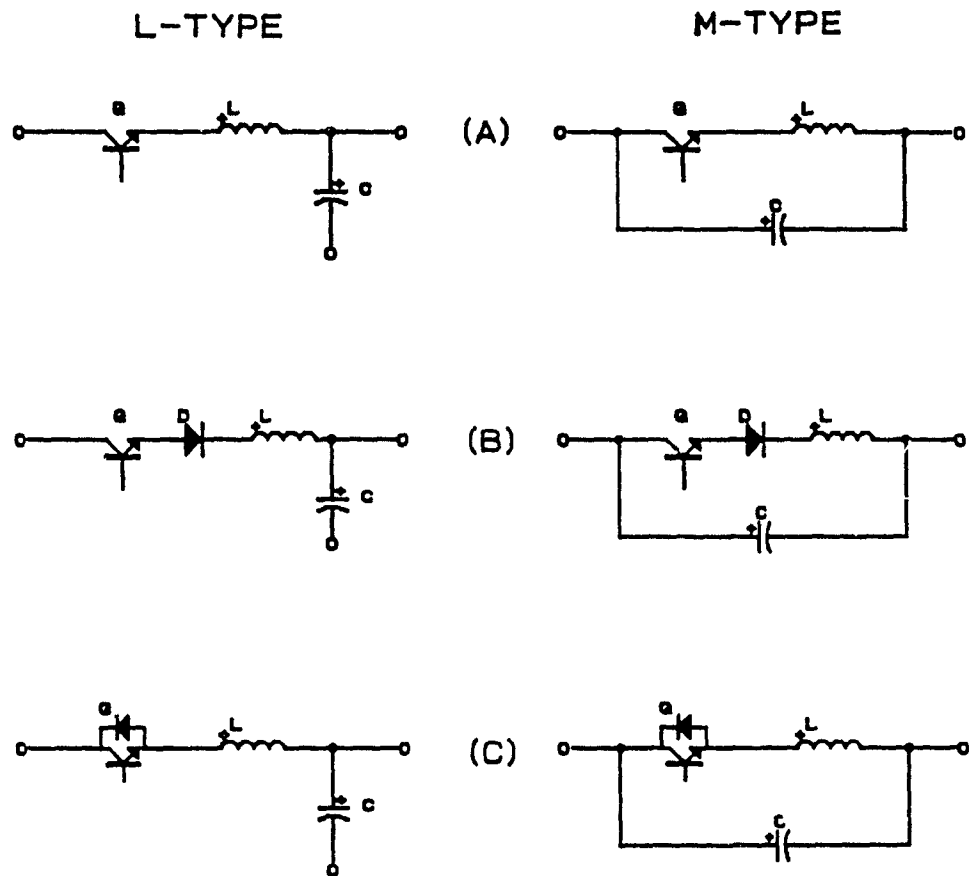
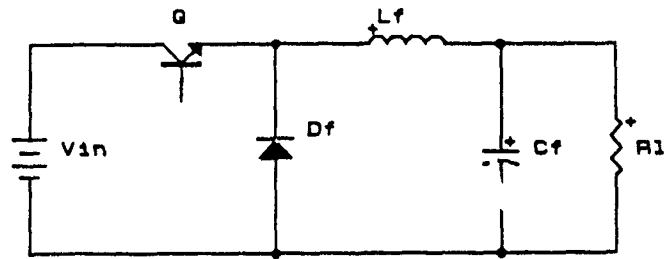


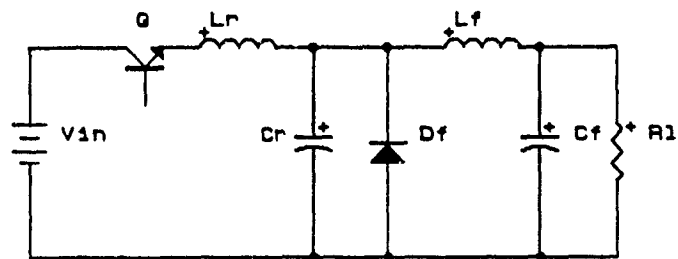
Fig. 1.8 Resonant Switch Configurations

a) General Topologies. b) Half-Wave. c) Full-Wave.

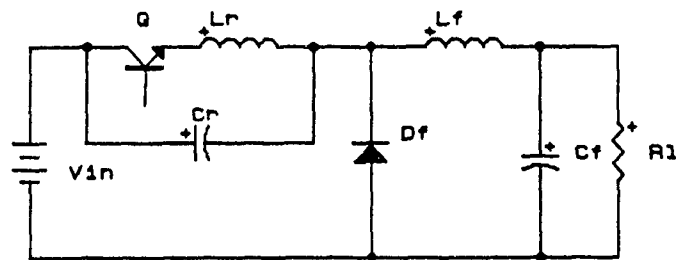




(A)



(B)



(C)

Fig. 1.9 Buck Converter

a) Conventional. b) With L-Type Resonant Switch.

c) With M-Type Resonant Switch.

The implementation of the resonant-switch approach for buck converter is shown in Fig. 1.9. The Figure indicates that two types of resonant-switch topologies are possible. These types can be specified as L-type and M-type.

Although these circuits represent a step in the right direction, various problems can be identified with each of these topologies. In particular, the peak voltage stress and the diode reverse recovery are the limitations. The need to limit voltage stresses restricts the operating range of the converter especially under light load conditions. Further, reverse recovery of the free-wheeling diode causes voltage spikes and trapped energy which needs to be handled. The conclusions which can be drawn thus far from the presented materials are:

- a) High frequency power conversion is necessary.
- b) Resonant converters, can be used in high frequency low power applications,  
and
- c) PWM converters, aided by soft switching techniques, can be utilized in high  
frequency high power applications.

#### 1.4 Advantages of Proposed Topologies

The scope and objective of this thesis is to present a new and improved alternative to the hard-switching problem associated with PWM converters. For this purpose three high frequency PWM dc/dc original converter topologies, their complete analysis, design, simulation, and experimental verification for two of them, are provided. The proposed topologies utilize dc bus commutating subcircuits. They are designed to provide a zero-voltage dc bus condition to commutate the semiconductor devices, thus minimizing switching stresses and losses.

In addition and due to the presence of the dc bus commutation subcircuit, the inverter switches of the proposed topologies can be protected and isolated from the dc bus under adverse system operation conditions.

#### 1.5 Thesis Organization

The contents of this thesis have been organized as follows:

In Chapter 2, an overview of the switching losses in PWM converter, and switching environment in resonant converters are presented. An example including analysis and simulation results is provided. In addition, methods of improving switching conditions in PWM converters are discussed with special emphasis on dc bus commutating techniques.

In Chapter 3, the analysis and design of a half-bridge dc bus commutated high frequency PWM dc/dc converter employing a dc bus commutating subcircuit is presented. The subcircuit consists of a dc bus interrupt switch with a capacitor connected across the dc bus. It commutates the inverter switches under zero-voltage condition. Proof of concept, simulation, and experimental

results are provided.

In Chapter 4, the analysis and design of a full-bridge dc bus commutated high frequency PWM dc/dc converter is presented. The topology uses a lossless snubber subcircuit associated with a dc bus switch, and an L-C commutating subcircuit to achieve zero-voltage and zero-current commutating conditions. Again, proof of concept, simulation and experimental results are also provided.

In Chapter 5, the application of the concept of dc bus commutation used in chapter three is extended to three-phase PWM VSI. The analysis and design of a dc bus commutated full-bridge high frequency three-phase PWM VSI is treated in detail. A design example and simulation results verifying the associated principles of operation are also presented.

In Chapter 6, conclusions and suggestions of work in the near future are provided.

## CHAPTER 2

### AN OVERVIEW OF THE SWITCHING LOSSES IN VARIOUS TYPES OF CONVERTERS

This chapter includes the following:

In section 2.1, the introduction describing the classification of device power losses is presented.

In section 2.2, switching characteristics of ideal switches using a resistive or an inductive load circuit are provided.

In section 2.3, the introduction of sine pulse width modulation (SPWM) technique and SPWM-inverter power losses are briefly discussed.

In section 2.4, description of switching environment in resonant dc/dc converters, and an example of Parallel-Loaded Resonant Inverter (PLRI) are given. This example includes a power circuit analysis, switching behavior, and simulation results. Thyristors with antiparallel diodes as switching devices are used in the topology of PLRI. The commutation of these devices takes place under zero-current and zero-voltage conditions resulting in zero switching losses and low EMI.

In section 2.5, methods of improving switching conditions in PWM converters are treated. Special emphasis is given to the existing dc bus commutation techniques which are used to minimize the switching losses. Finally, two innovative dc bus commutating subcircuits are proposed. These two subcircuits can be applied in high frequency PWM dc/dc converters to eliminate the switching losses.

In section 2.6, conclusions of this chapter are provided.

## 2.1 Introduction

The applications of transistors as switching devices have been increasing due to recent developments in their switching characteristics. These applications can be found in fields such as:

- Motor speed control.
- PWM converter for power supply systems.
- Induction heating, and
- High frequency welding and others.

In order to use these devices properly, designers must be able to keep device junction temperatures within rated values. The device power losses are generally grouped into three categories:

- 1) Switching losses.
  - a) Turn-on loss, and
  - b) Turn-off loss.
- 2) Conduction loss, and
- 3) Off-state losses.

The off-state losses in high-power electronic circuits contribute a very small portion to the total losses. Therefore, they are considered negligible. Whereas the relative magnitudes of the switching and conduction losses are greatly dependent on the type of load circuit in which the transistors are used. They also depend on operating frequency, the turn-on and turn-off snubbers used and certain inherent characteristics of the transistor itself.

## 2.2 Switching Characteristics of Ideal Switches

Switching characteristics of ideal switches will be shown in each type of

the following load circuits:

- 1) Resistive load circuit, and
- 2) Inductive load circuit.

### 2.2.1 Resistive Load Switching Characteristics

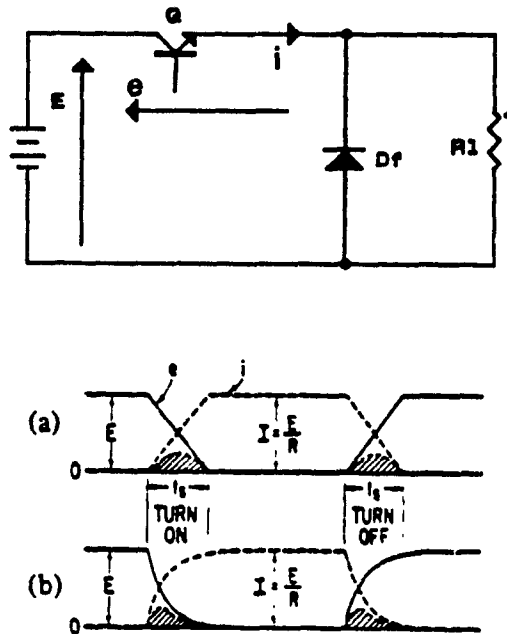


Fig. 2.1 Transistor Switching A Resistive Load.

a) Linear Rise and Fall. b) Exponential Rise and Fall.

In this section, the calculation of a switch's switching losses in a resistive load circuit is presented. It will show that these switching losses are proportional to the switched power, the switching frequency and the effective switching times (turn-off and turn-on times). These switching times depend on the switch-switching characteristics and the base drives used. Therefore, in order to have low switching losses the designer has to ensure the following:

- i) Select fast switching switches, and
- ii) Design proper base drives to commutate the switches fast.

The circuit and switching waveforms of a resistive load are shown in Fig. 2.1 with two alternative ideal switching characteristics, using the transistor as switching device. This simple case is described in reference [19] and is reviewed here to establish a baseline for further analysis of switching behavior.

In Fig. 2.1 (a) the voltage is assumed to fall linearly during turn-on, and the current is assumed to fall similarly during turn-off. The circuit equations in the turn-on interval are as follows:

Transistor voltage:

$$e = E \left(1 - \frac{t}{t_s}\right) \quad [\text{V}] \quad \text{for } 0 < t < t_s \quad (2.1)$$

Transistor current (assumed):

$$i = \frac{E - e}{R} = I \frac{t}{t_s} \quad [\text{A}] \quad \text{for } 0 < t < t_s \quad (2.2)$$

where,

$$I = \frac{E}{R} \quad [\text{A}] \quad (2.3)$$

Transistor power dissipation:

$$P = e i = E I \frac{t}{t_s} \left(1 - \frac{t}{t_s}\right) \quad [\text{W/pulse}] \quad (2.4)$$

Total turn-on switching loss:

$$W = \int_0^{t_s} P dt = \frac{1}{6} E I t_s \quad [\text{W} \cdot \text{s/pulse}] \quad (2.5)$$

During turn-off the time-dependent factors in the voltage and current equations are interchanged. The same expressions are valid for the power dissipation and total turn-off loss although switching time  $t_s$  will generally



be different. If the transistor is assumed to switch exponentially with a time constant  $\tau$ , as shown in Fig. 2.1 (b), then the turn-on equations become as follows:

Transistor voltage (assumed):

$$e = E \exp \left( - \frac{t}{\tau} \right) \quad [V] \quad (2.6)$$

Transistor current:

$$i = I \left[ 1 - \exp \left( - \frac{t}{\tau} \right) \right] \quad [A] \quad (2.7)$$

Total turn-on switching loss:

$$W = \int_0^{\infty} e i dt = \frac{1}{2} E I \tau \quad [W \cdot s / \text{pulse}] \quad (2.8)$$

Again, the turn-off loss calculation will result in the same function as in (2.8), but the value of the time constant will generally be different. In order to reduce the turn-on and turn-off losses,  $t_s$  or  $\tau$  should be as small as possible. Reducing  $t_s$  and  $\tau$  can be achieved by using fast switching switches and designing proper base drives.

### 2.2.2 Inductive Load Switching Characteristics

The circuit and waveforms for transistor switching an inductive load are sketched in Fig. 2.2. At low duty cycle and during turn-on, current rises slowly in the transistor. Initially, the inductance supports the supply voltage while the voltage across the transistor falls very quickly and the instantaneous product of voltage and current is negligible.

On the other hand, during turn-off, the voltage across the transistor starts to rise and reaches a maximum value before the collector current starts

to fall. This condition generates a larger peak power than for the resistive load. Switching turn-off loss for an inductive load with no snubber is:

$$W_{off} = \frac{1}{2} (V_c I_c t_{cf}) \quad [W . s/pulse] \quad (2.9)$$

where,

$V_c$  maximum voltage across transistor at turn-off (supply + spike),

$I_c$  maximum load current, and

$t_{cf}$  turn-off crossover time.

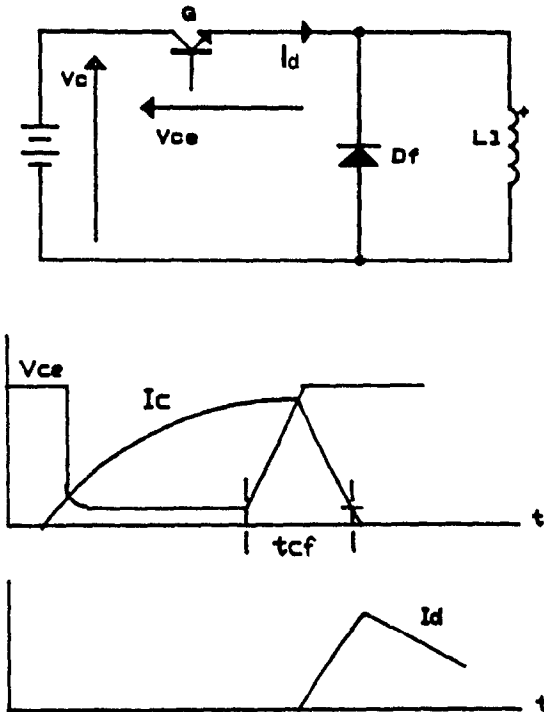


Fig. 2.2 Inductive Switching Waveforms (low duty cycle)

When the transistor is turned off, current that was flowing in the inductor continues to flow through the diode placed across the inductor. This condition will keep the induced voltage from creating a voltage spike that can destroy the transistor. Diode current rises to the maximum value of load

### 2.4.2 Switching conditions of Parallel-Loaded Resonant Inverter (PLRI)

In this subsection switching condition, detailed analysis and simulation results of a parallel-loaded resonant inverter (PLRI) Fig. 2.6 are given. This example will show that, zero-current and zero-voltage switching condition, can be obtained by using this type of resonant inverter.

#### 2.4.2.1 Circuit Description

The dc-to-ac full-bridge PLRI, shown in Fig. 2.6, consists of:

- 1) The input dc voltage  $V_{in}$ .
- 2) Self turn-off switches (thyristors, SCRs)  $TH_1$ ,  $TH_2$ ,  $TH_3$ , and  $TH_4$ , with the antiparallel diodes  $D_1$ ,  $D_2$ ,  $D_3$ , and  $D_4$ , and
- 3) Underdamped resonant tank L-C ( $L=L_1+L_2$ ) with the load represented by  $R_1$ .

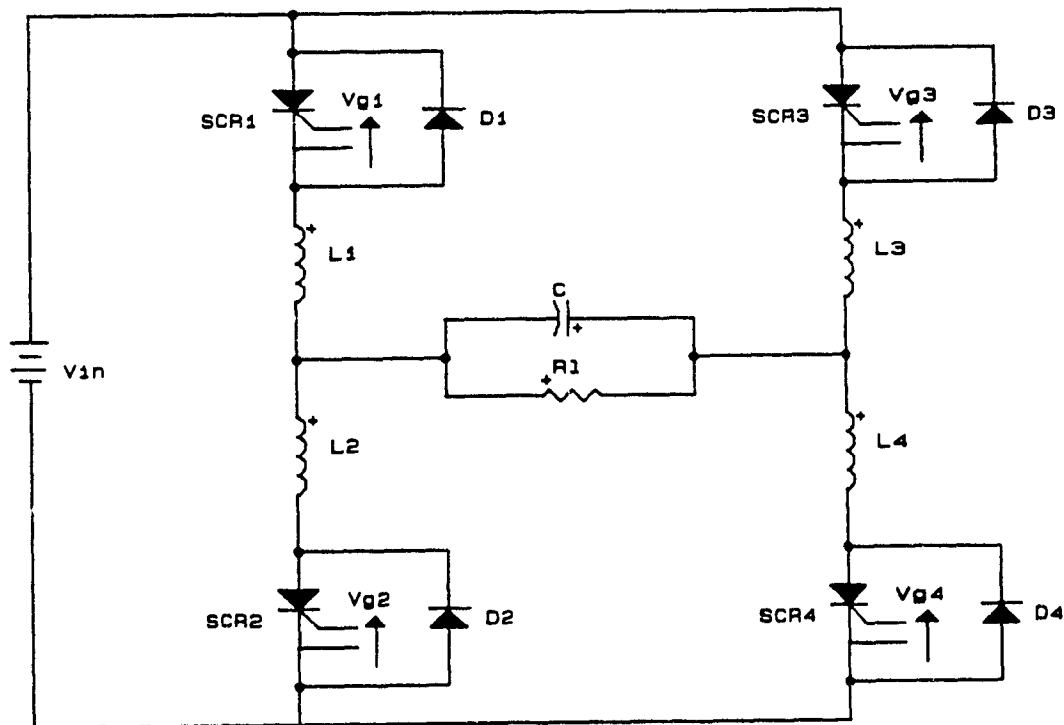


Fig. 2.6 DC-to-AC Full-Bridge Parallel-Loaded Resonant Inverter

#### 2.4.2.2 Topology Switching Environment

Initially the capacitor  $C$  has a negative voltage value. Thyristors  $TH_1$  and  $TH_4$  are fired simultaneously at low  $di/dt$ . Current stress  $di/dt$  and turn-on losses are limited by the inductors  $L_1$  and  $L_4$ . The current  $i_{th1,4}$  through the thyristors  $TH_1$  and  $TH_4$  is underdamped resonant. When this current reaches zero, the thyristors  $TH_1$  and  $TH_4$  are turned off at zero current and zero voltage condition. This switching condition can be explained as follows:

When thyristors  $TH_1$  and  $TH_4$  are turned off, the voltage across the capacitor  $C$  has reached a maximum positive value which is larger than the value of the input dc voltage  $V_{in}$ . Therefore, the capacitor  $C$  is forced to discharge into the dc source, through  $TH_1$  and  $TH_2$  antiparallel diodes  $D_1$  and  $D_4$ . This current-flow, creates zero-voltage in addition to zero-current switching condition. The inverter turn-off process is now complete, and the next period of operation can be started at any moment by firing the thyristors  $TH_2$  and  $TH_3$ .

#### 2.4.2.3 Analysis and Modes of Operation

The PLRI topology discussed in this section has three distinct modes of operation during a switching cycle. These modes, (a), (b), and (c) are next explained in detail.

Mode (a):

The equivalent circuit during interval  $t_1=0$  to  $t_2$ , is shown in Fig. 2.7. At  $t_1$ , the switches  $TH_1$  and  $TH_4$  are fired simultaneously. Initially the capacitor has a negative value  $V_{c(0)}$ . The components  $C$  and  $L$  form an underdamped resonant circuit with the resistive load  $R_l$ . The capacitor  $C$  is

being charged with the polarity as shown. This mode ends at  $t_2$  when the thyristors  $TH_{1,4}$ 's current  $I_{th1,4}$  becomes zero and they turn off. At the same moment the voltage across  $C$  has reached the maximum positive value  $V_{c(02)}$ , which is greater than the supply voltage  $V_{in}$ . The current through the switches through the time interval  $t_1 \rightarrow t_2$ , as a function of time, is given by:

$$I_{th1,4} = \frac{V_{in}}{R_1} + A_1 e^{\left(\frac{-1}{2R_1 C}\right)} \sin(\omega_r t + \alpha_1) \quad [A] \quad (2.12)$$

Where  $A_1$  and  $\alpha_1$  can be calculated using initial values.

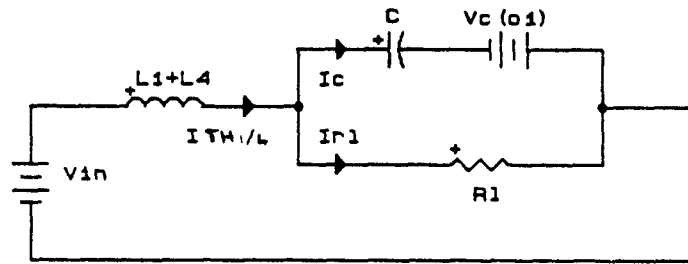


Fig. 2.7 The Equivalent Circuit of Mode (a) of Topology Fig. 2.6,  $t_1 \rightarrow t_2$

The ringing frequency is given by:

$$\omega_r = \sqrt{\frac{1}{L C} - \frac{1}{4 R_1^2 C^2}} \quad [\text{rad/s}] \quad (2.13)$$

Mode (b):

The equivalent circuit during interval  $t_2$  to  $t_3$ , is shown in Fig. 2.8. At  $t_2$  since  $V_{c(02)} > V_{in}$ , the capacitor  $C$  begins discharging into the dc supply source through the feedback diodes  $D_1$  and  $D_4$ . This current-flow creates zero voltage across the thyristors  $TH_1$  and  $TH_4$ . When  $V_c = V_{in}$ , the feedback current reaches its maximum value and begins decreasing toward zero. At  $t_3$ , the feedback current reaches zero and the voltage across  $C$  is  $V_{c(03)}$ . The feedback

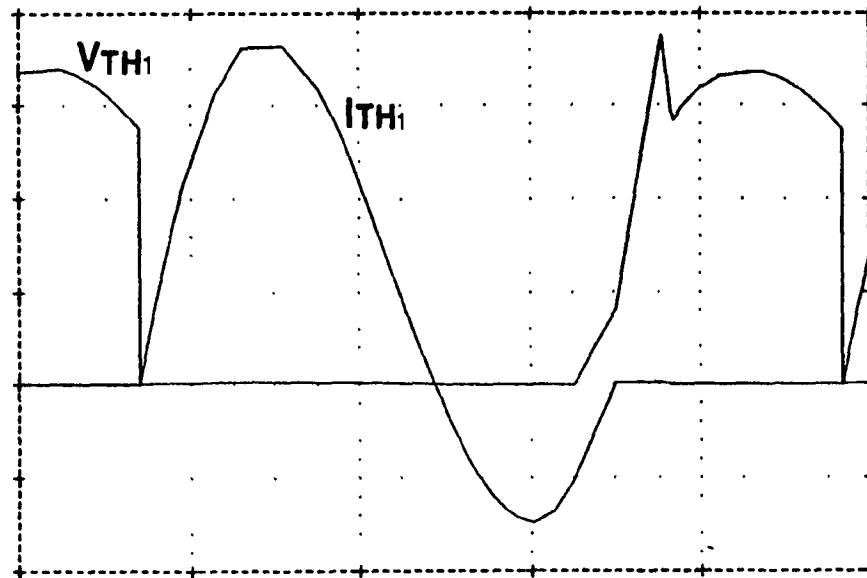


Fig. 2.10 Current and Voltage Through the Thyristor  $TH_1$  of Topology Fig 2.6

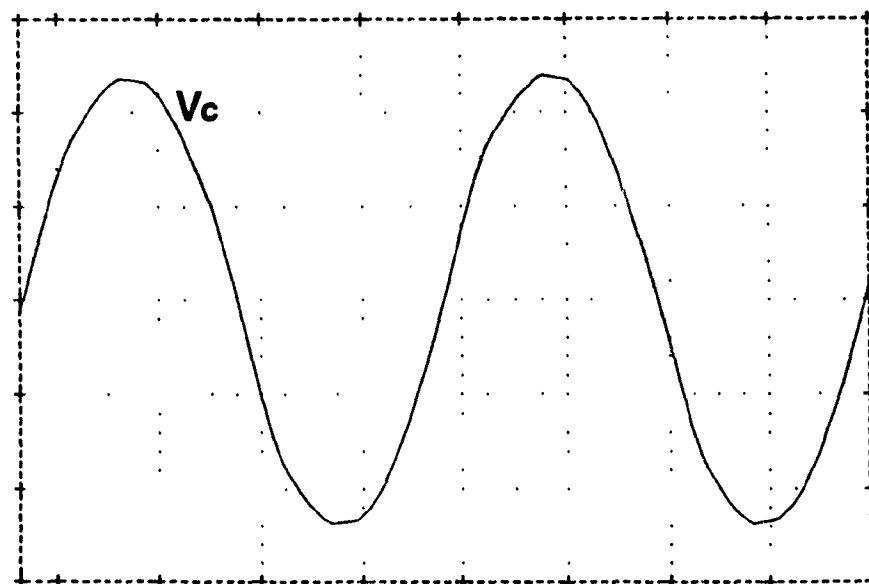


Fig. 2.11 The Voltage Across the Capacitor  $C$  of Topology Fig. 2.6

switches. This converter topology functions at high frequencies with no switching losses. However, the topology suffers from high voltage stress of up to  $2.5 V_{in}$  across its switching devices.

The actively clamped resonant dc link inverter shown Fig. 2.12 and proposed in reference [11] is an alternative topology. It reduces the voltage stresses to near  $1.5 V_{in}$ , while maintaining zero-voltage dc bus switching condition. However, due to the discrete width modulation used high sub-harmonics exist in the inverter output ac voltages.

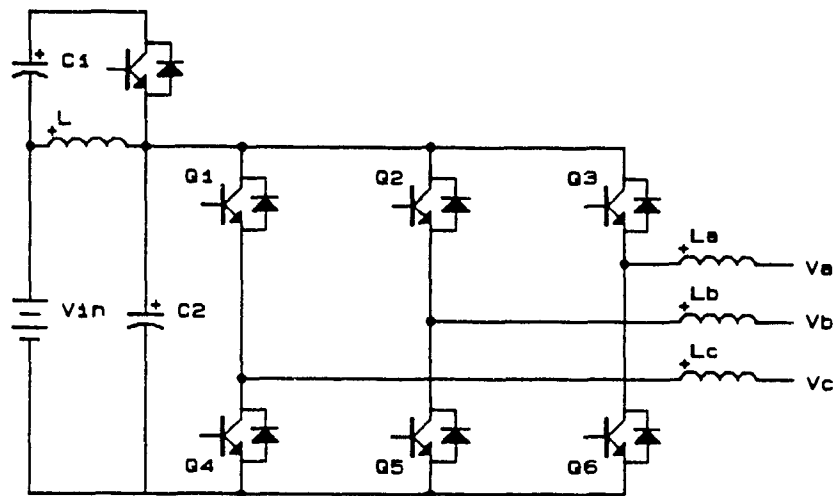


Fig. 2.12 The Actively Clamped Resonant DC Link Inverter

A new technique of PWM with resonant dc link converters has also been proposed lately in reference [12]. This technique results in reduced levels of sub-harmonics. Whereas the PWM switching capability is obtained with significantly higher losses and device stresses.

Pulse-commutation subcircuits known from the thyristor inverters and proposed in references [13,14], also generate zero-voltage dc bus switching conditions. These topologies are in the right direction of reducing switching

losses. However, the main disadvantage of these topologies is high circuit complexity which increases the size, weight and cost of the system.

### 2.5.3 The Proposed Family of Dc Bus Commutated Subcircuits

Two dc bus commutating subcircuits are proposed in this section. The first subcircuit is depicted in Fig. 2.13. It consists of only a dc bus interrupt switch and a capacitor connected across the dc bus. The second proposed dc bus commutating subcircuit is illustrated in Fig. 2.14. It consists of an interrupt dc bus switch, three diodes, two capacitors and an inductor.

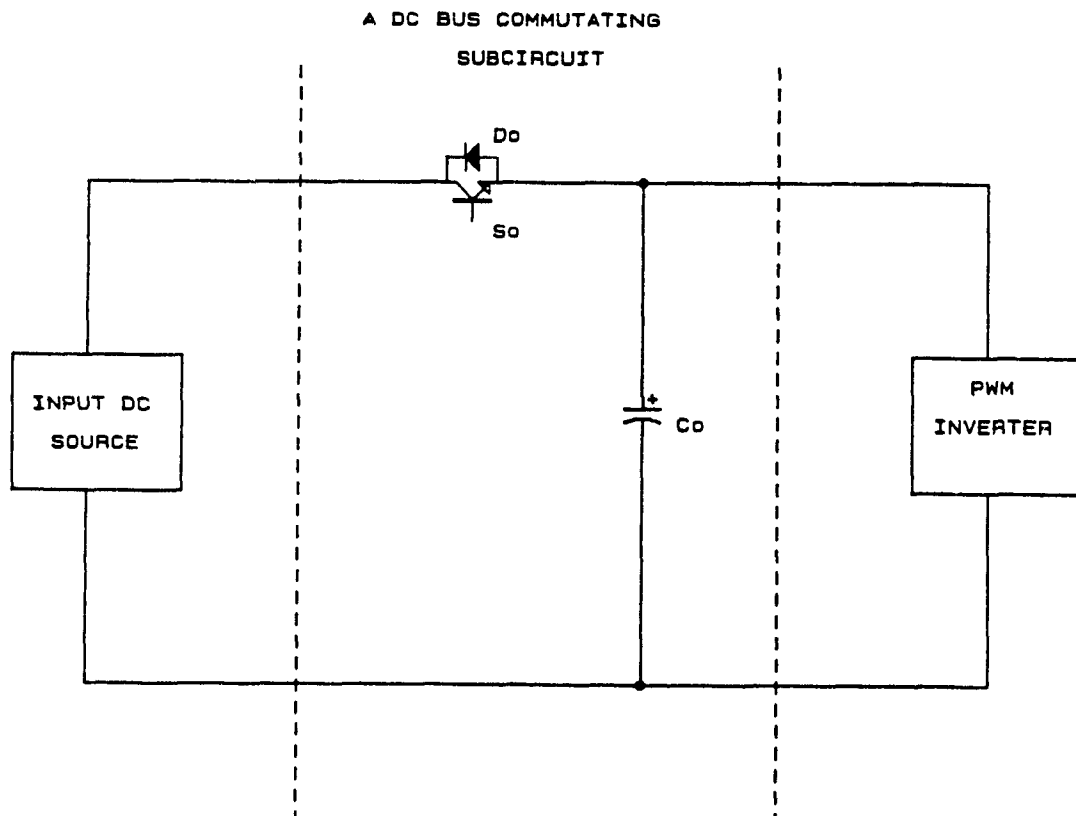


Fig. 2.13 The Proposed Dc Bus Commutating Subcircuit, Topology No.(1)



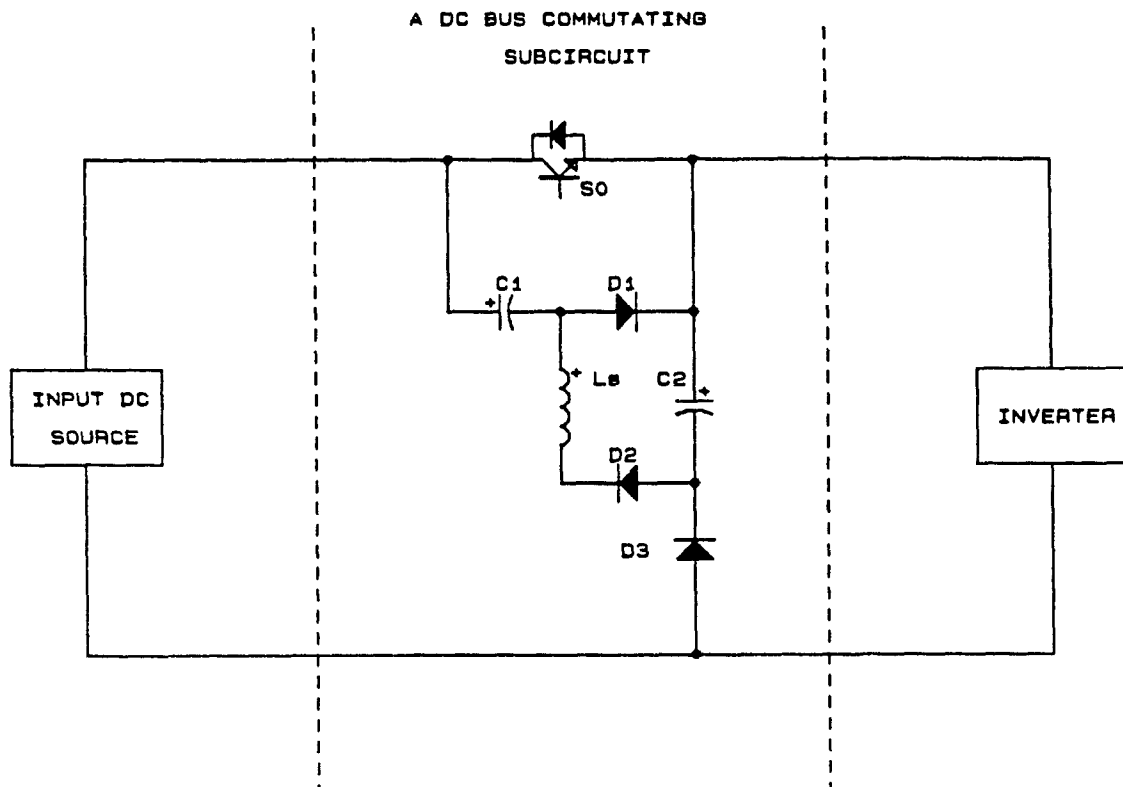


Fig. 2.14 The Proposed Dc Bus Commutating Subcircuit, Topology No. (2)

The main feature of these subcircuits is that they also provide zero dc bus voltage switching conditions at the cost of moderate additional circuit complexity. As a result, the associated converters operate with zero switching losses, minimum switch stresses and low EMI. Also the desired high switching frequency PWM converters, can now be realized without excessive circuit complexity.

The implementation of the proposed dc bus commutating subcircuits shown in Figs. 2.13 and 2.14 for half-bridge, full-bridge, and three-phase full-bridge high frequency PWM dc/dc converters will be explained in the following three chapters.

## 2.6 Conclusions

Thus far, the problems associated with converter operation at high frequency and power levels have been summarized. Switching conditions in resonant and PWM converters, have been also discussed. Soft switching techniques were proposed to improve the switching condition in PWM converters. The advantages and disadvantages of each of these techniques have been pointed out. Finally, a new dc bus commutation technique has been proposed. This technique applies innovative types of dc bus commutating subcircuits to reduce the switching losses in PWM converters.

The conclusions which can be drawn from the information provided thus far are:

- Converting power at high frequency operation is necessary in terms of improving performance, and reducing size and costs.

- At low power levels resonant converters fulfill the requirement of high frequency operation without introducing serious operating difficulties.

- At high power levels high frequency PWM converters, aided by soft switching techniques, are the alternative to the resonant ones.

- Soft switching techniques can be obtained by:

- a) Applying snubber subcircuits, or preferably by
- b) Using proper dc bus commutating subcircuits.

## CHAPTER 3

### ANALYSIS AND DESIGN OF A HALF-BRIDGE DC BUS SOFT COMMUTATED PWM DC/DC CONVERTER

In this chapter, the implementation of the proposed dc bus commutating subcircuit topology No. (1) shown in Fig. 2.13, for half-bridge PWM dc/dc converter is discussed in detail. In particular, the following sections are devoted to explore the operation and performance of the resulting dc bus commutated half-bridge converter shown in Fig. 3.1.

In section 3.1, an introduction about the advantages obtained by the implementation of the proposed commutating subcircuit is provided.

In section 3.2, the zero-voltage switching conditions for the dc bus switch and the inverter switches are presented.

In section 3.3, a complete identification of all modes of operation is provided.

In section 3.4, a complete mathematical analysis of all modes of operation is presented.

In section 3.5, design guidelines to select the component values are provided.

In section 3.6, a design example uses the equations obtained in the previous section is outlined.

In section 3.6, simulation results of the key currents and voltages are obtained. In particular, the switching behaviors of the converter switches are shown.

In section 3.7, experimental results are provided to prove that the predicted zero-voltage switching conditions are achieved.

In section 3.8, conclusions are drawn from this chapter's contents.

### 3.1 Introduction

The proposed dc bus commutating subcircuit shown in Fig. 2.13 is applied for half-bridge PWM dc/dc converter, which can be used in low power applications. The resulting topology is shown in Fig. 3.1. It is noted that with this topology zero switching losses for the inverter switches and for the dc bus switch, are achieved under rated to no load condition. As compared to the topologies which implement other dc bus commutation approaches [13,14], the proposed topology has the following advantages:

- i) It converts power at high switching frequencies with relatively slow switches (e.g. IGBTs, Bipolars, and GTOs).
- ii) The power and control circuits are very simple, and
- iii) The dc bus switch can be used to isolate the inverter from the dc bus under adverse system operating conditions.

The resulting dc-to-dc half bridge forward pwm topology shown in Fig. 3.1, consists of three sections:

- 1) The dc bus which includes the input dc voltage  $V_s$ , the series dc bus switch  $S_0$  and a parallel dc bus snubber capacitor  $C_0$ .
- 2) The half bridge forward PWM inverter including the switches  $S_1$  and  $S_2$ , the diodes  $D_1$  and  $D_2$ , the  $di/dt$  limiting inductor  $L_0$  and the parallel inductor  $L_m$ . The inductor  $L_m$  represents the magnetizing inductance of the high frequency isolating transformer  $T$ .
- 3) The half bridge rectifier consisting of the diodes  $D_{r1}$  and  $D_{r2}$  and filter inductor  $L_f$  connected to the load represented by resistor  $R_L$ .

The operating conditions of the discussed dc/dc converter Fig. 3.1 are described in the following section. In particular, switching sequence and behavior are explained.

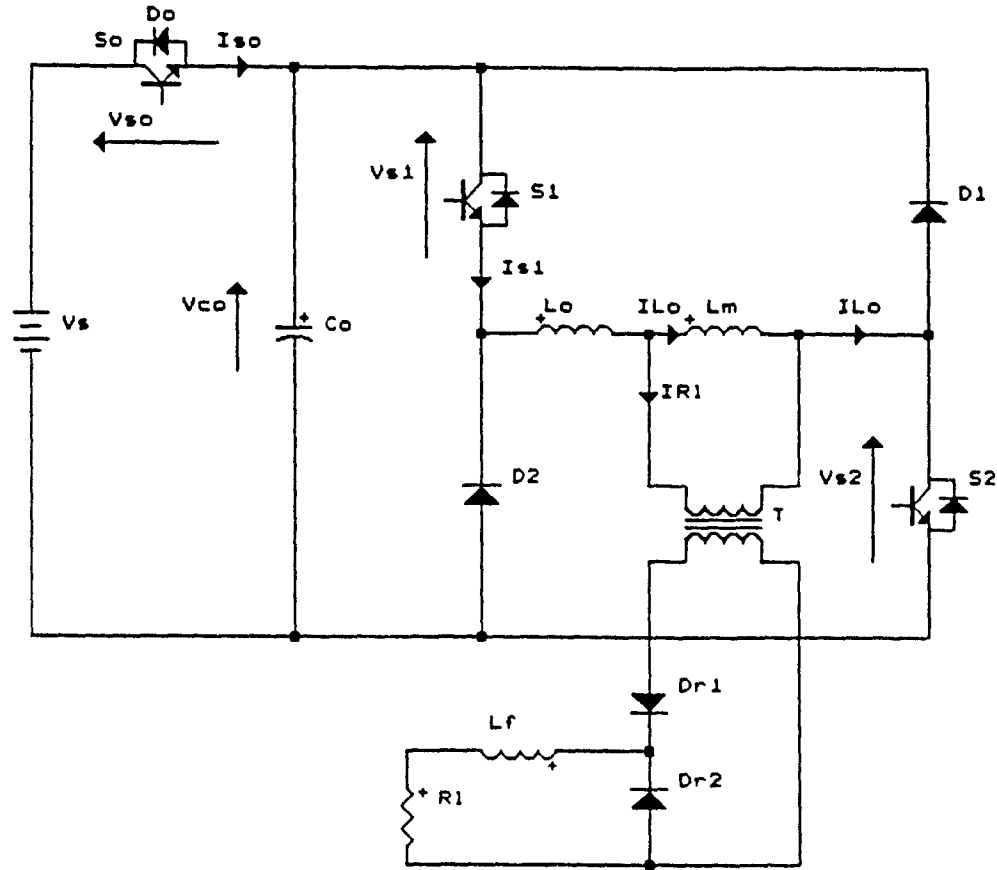


Fig. 3.1 A Dc Bus Commutated Half-Bridge PWM Dc/Dc Converter

### 3.2 Zero-Voltage Switching Environment

The converter achieves soft current switching as follows: Initially, all three switches are on and the voltage across  $C_o$  is equal to the input dc voltage  $V_s$ . The current  $I_{so}$  through the switches  $S_o$ ,  $S_1$  and  $S_2$  is flowing from the dc source  $V_s$  through the load  $R_1$  and increases at a constant rate. Shortly before the end of the switching period, the dc bus switch  $S_o$  is first turned off under zero  $V_{so}$  condition since  $V_s = V_{co}$ . Immediately,  $C_o$  begins to discharge at the rate of  $C_o/I_{Lo}$  (V/ $\mu$ s). When  $V_{co}=0$  (V),  $D_1$  and  $D_2$  become

forward biased and the current  $I_{Lo}$  begins to freewheel through the upper and lower halves of the forward converter.

Next, switches  $S_1$  and  $S_2$  are turned off under zero  $V_{s1,2}$  voltage conditions. With switches  $S_1$  and  $S_2$  off, the current  $I_{Lo}$  is forced by  $L_o$  to flow back into  $C_o$  through diodes  $D_1$  and  $D_2$ . Eventually,  $V_{Co}$  exceeds  $V_s$  and  $D_o$  begins to conduct. At this moment,  $S_o$  can be turned on under zero volt condition. The converter turn-off process is now complete and the next period of operation begins at the appropriate moment by turning on  $S_1$  and  $S_2$ . All modes of operation of the examined topology of Fig. 3.1 are further explained in the following sections.

### 3.3 Modes of Operation

The circuit under study which is illustrated in Fig. 3.1, has six distinct modes of operation during a switching cycle. The time-intervals identifying the modes a, b, c, d, e and f are shown in Fig. 3.2. The performance of the circuit in each mode is described below.

Mode (a): The equivalent circuit of this mode for interval  $t_1 \rightarrow t_2$  Fig. 3.2, is shown in Fig. 3.3. Initially at  $t_1$ , the switches  $S_o$ ,  $S_1$  and  $S_2$  are on and the voltage across  $C_o$  equals  $V_s$ . The current  $I_{s0}$  through the switches  $S_o$ ,  $S_1$  and  $S_2$  is the sum of the load current  $I_{R1}$ , which increases from a minimum value and the magnetizing inductor  $L_m$  current  $I_{lm}$  which increases from zero. The surging inductor  $L_o$  limits  $di/dt$  through the switches. Under steady state conditions and by neglecting  $L_o$  ( $L_o \ll L_m$  and  $L_o \ll L_r$ ) the voltage across  $L_m$  equals  $V_s$ .

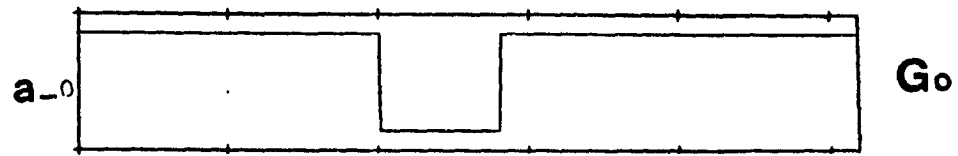


Fig. 3.2 (a) The Gating Signal of the Dc Bus Switch  $S_o$ , Topology Fig. 3.1



Fig. 3.2 (b) The Gating Signals of the Switches  $S_1$  and  $S_2$ , Topology Fig. 3.1

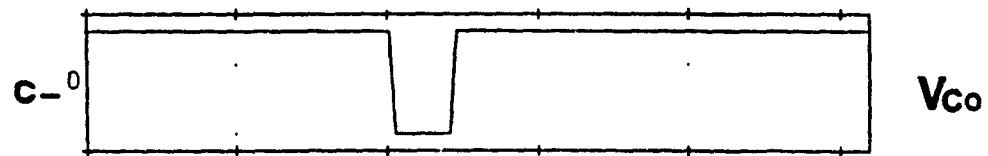


Fig. 3.2 (c) The Dc Bus Voltage  $V_{co}$ , Topology Fig. 3.1

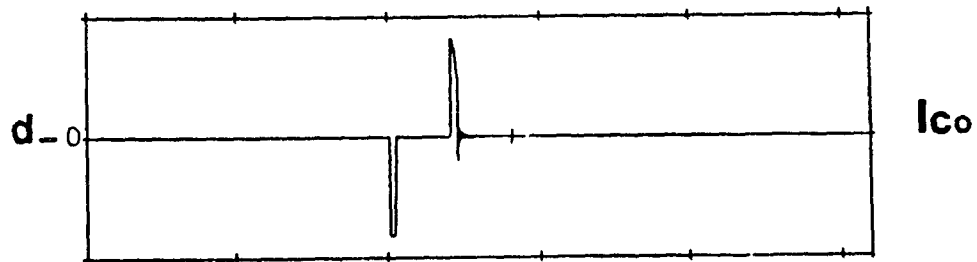


Fig. 3.2 (d) The Current Through the Capacitor  $C_o$ , Topology Fig. 3.1

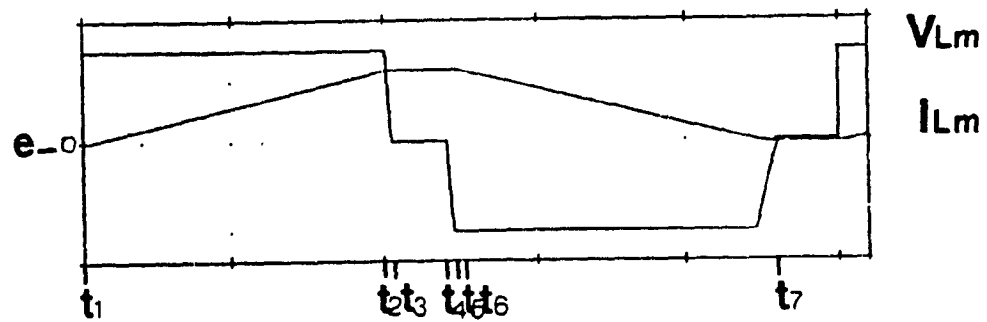


Fig. 3.2 (e) The Voltage and the Current Through  $L_m$ , Topology Fig. 3.1

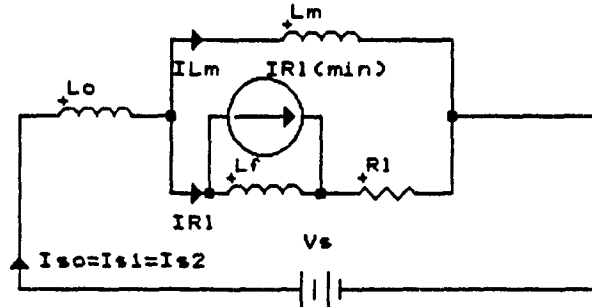


Fig. 3.3 The Equivalent Circuit of Mode (a) of Topology Fig. 3.1,  $t_1 \rightarrow t_2$

Mode (b): The equivalent circuit of this mode, for interval  $t_2 \rightarrow t_3$  in Fig. 3.2, is illustrated in Fig. 3.4. At  $t_2$ ,  $S_0$  is gated off at zero voltage since  $V_s = V_{Co}(o_2)$ , and  $S_1$  and  $S_2$  are kept on. At the same moment, the capacitor  $C_0$  begins discharging by sourcing the current  $I_{Lo}(o_2)$ , which reaches a maximum value until  $t_3$ .

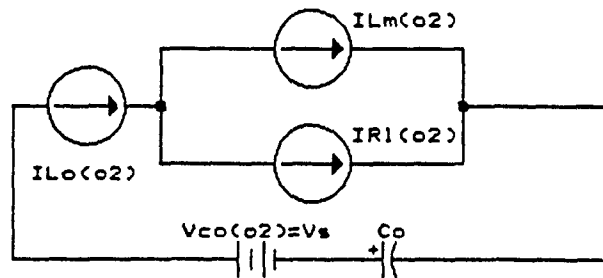


Fig. 3.4 The Equivalent Circuit of Mode (b), Topology Fig. 3.1,  $t_2 \rightarrow t_3$

Mode (c): The equivalent circuit for this mode, during interval  $t_3 \rightarrow t_4$  in Fig. 3.2, is depicted in Fig. 3.5. At  $t_3$ , the capacitor  $C_0$  is completely discharged to zero. Therefore, the dc bus is short circuited and a freewheeling period exists. The current through  $L_0$   $I_{Lo} = I_{R1} + I_{Lm}$ , is clamped at its maximum value, half of which freewheels through  $L_0$ ,  $D_1$  and  $S_1$  and the



remainder through  $L_o$ ,  $S_2$  and  $D_2$ . In the rectifier circuit,  $I_{R1}$  begins freewheeling through  $D_{r1}$ ,  $L_r$  and  $R_l$ . At any moment of this time interval,  $S_1$  and  $S_2$  could be gated off at zero voltage resulting in zero turn-off losses.

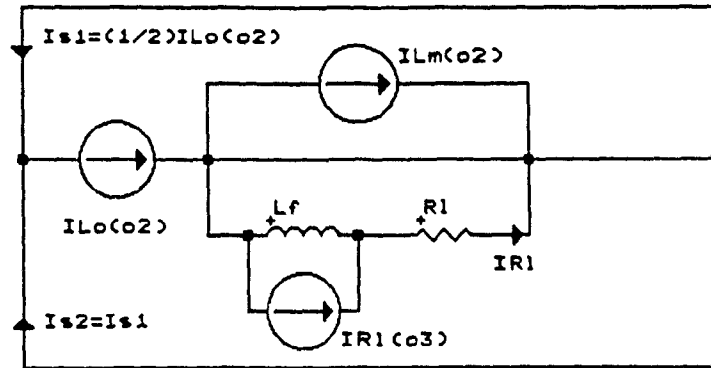


Fig. 3.5 The Equivalent Circuit of Mode (c) of Topology Fig. 3.1,  $t_3 \rightarrow t_4$

Mode (d): The equivalent circuit of this mode, for interval  $t_4 \rightarrow t_5$  in Fig. 3.2, is depicted in Fig. 3.6. At  $t_4$ , the switches  $S_o$ ,  $S_1$  and  $S_2$  are off and the inductor  $L_o$  current  $I_{L_o}$ , forced by the stored energy of  $L_o$ , is sent back to the dc bus passing through  $D_1$  and  $D_2$ . Immediately, this current  $I_{L_o} = I_{R1} + I_{L_m}$  begins charging the capacitor  $C_o$  until  $t_5$ , at which time  $I_{L_o} = I_{L_m}$ . In the rectifier circuit at  $t_4$ , the load current  $I_{R1}$  begins commutating from  $D_{r1}$  to  $D_{r2}$ . At  $t_5$ , the current through  $D_{r1}$  reaches zero and the current through  $D_{r2}$  reaches the load current  $I_{RL}$ .

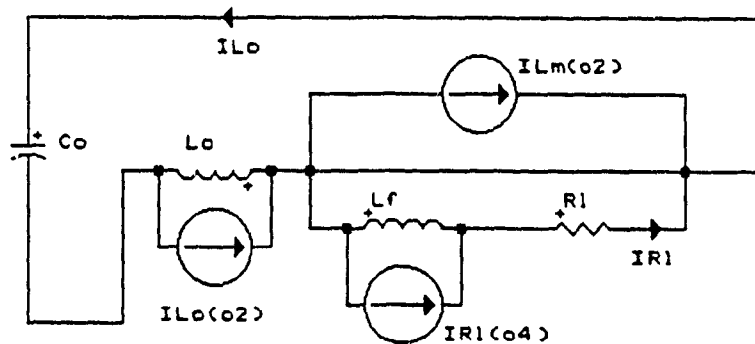


Fig. 3.6 The Equivalent Circuit of Mode (d) of Topology Fig. 3.1,  $t_4 \rightarrow t_5$

Mode (e): The equivalent circuit of this mode, in the interval  $t_5 \rightarrow t_6$  in Fig. 3.2, is shown in Fig. 3.7. At  $t_5$ , the switches  $S_0$ ,  $S_1$  and  $S_2$  are still off. The load current  $I_{R1}$  freewheels through  $D_{r2}$ , while the current  $I_{L0}=I_{Lm}$  continues charging the capacitor  $C_0$ . This charging current flows through  $L_0$ ,  $L_m$ ,  $D_1$  and  $D_2$ , until  $t=t_6$  when  $V_{C0}=V_s$  and  $V_{Lm}=-V_s$ .

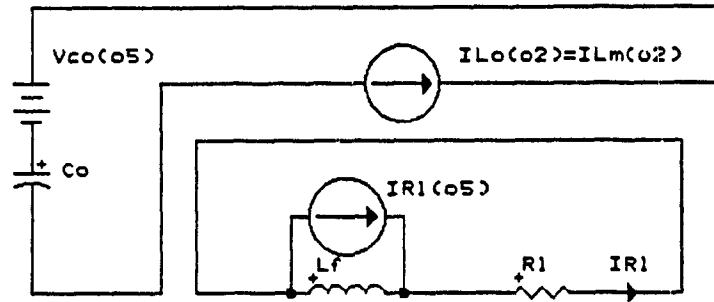


Fig. 3.7 The Equivalent Circuit of Mode (e) Topology of Fig. 1.3,  $t_5 \rightarrow t_6$

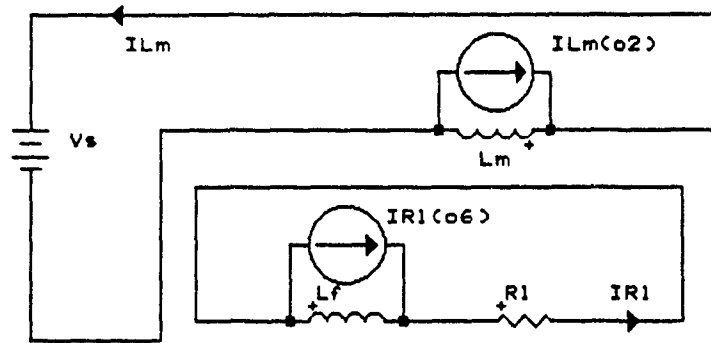


Fig. 3.8 The Equivalent Circuit of mode (f) of Topology Fig. 3.1,  $t_6 \rightarrow t_7$

Mode (f): The equivalent circuit of this mode, for the interval  $t_6 \rightarrow t_7$  in Fig. 2.3, is shown in Fig. 3.8. At  $t_6$ , the capacitor  $C_0$  is completely charged to the input dc voltage value  $V_s$ . The dc bus switch  $S_0$  can now be gated on at zero voltage condition. The load current  $I_{R1}$  keeps freewheeling through  $D_{r2}$

and decreasing toward a minimum value dictated by  $L_r$  and  $R_l$ . While the current  $I_{lm}$  is now transferred to the dc bus switch antiparallel diode  $D_o$ . This current also transfers the rest energy of  $L_m$  to the dc source until  $I_{lm}$  reaches zero. By now, all modes of operation have been defined.

### 3.4 Circuit Analysis

In this section, the analytical expressions describing all modes of operation of the examined converter topology Fig. 3.1 are presented. Expressions for the currents and the voltages during all subsequent modes of operation are obtained by assuming the following:

- i) All the converter components are ideal.
- ii) The input voltage is a stiff dc, and
- iii) The turns ratio of the high frequency isolating transformer is one.

Mode (a): The equivalent circuit is shown in Fig. 3.3. The current through the dc bus switch and the inverter switches, as a function of time, is given by:

$$I_{s0}(t) = I_{s1}(t) = I_{s2}(t) = I_{Lm}(t) + I_{Rl}(t) \quad (3.1)$$

Under steady state operation conditions and by neglecting  $L_o$  since ( $L_o \ll L_m$  and  $L_o \ll L_r$ ), the currents  $I_{Lm}(t)$  and  $I_{Rl}(t)$  are given by:

$$I_{Lm}(t) = \frac{V_s}{L_m} t \quad (3.2)$$

$$I_{Rl}(t) = \frac{V_s}{R_l} + \left( I_{Rl}(min) - \frac{V_s}{R_l} \right) e^{-\frac{R_l}{L_r} t} \quad (3.3)$$

The voltages across  $C_o$ ,  $L_m$ ,  $R_l$  and  $L_r$  in this mode are given by:

$$V_{C0(01)} = V_s \quad (3.4)$$

$$V_{Lm} = V_s \quad (3.5)$$

$$V_{RI(t)} = I_{RI(t)} R_l \quad (3.6)$$

$$V_{Lf(t)} = L_f \frac{dI_{RI(t)}}{dt} \quad (3.7)$$

where  $I_{RI(min)}$  is the minimum load current, and can be calculated as follows:

$$I_{RI(min)} = I_{RI(ave)} - \frac{1}{2} \Delta I_{RI} \quad (3.8)$$

where  $I_{RI(ave)}$  and  $\Delta I_{RI}$  are the average load current, and the ripple load current. They are given by:

$$I_{RI(ave)} = \frac{t_2 F_{inv} V_s}{R_l} \quad (3.9)$$

$$\Delta I_{RI} = \frac{(V_s - t_2 F_{inv} V_s)}{L_f} t_2 \quad (3.10)$$

where  $F_{inv}$  is the switching frequency of the inverter switches  $S_1$  and  $S_2$ . The time  $t_2$  can be computed from:

$$t_2 = \frac{D_{s0}}{F_{s0}} \quad (3.11)$$

where  $F_{s0}$  and  $D_{s0}$  are the switching frequency and the duty cycle of the dc bus switch  $S_0$ . At  $t_2$ , the voltage across  $C_0$  is given by:

$$V_{C0(02)} = V_s \quad (3.12)$$

at the same moment  $t_2$ , the current through the switches  $S_1$  and  $S_2$ , has already reached a maximum value and is given by:

$$I_{S1(max)} = I_{S2(max)} = (I_{Lm} + I_{RI}) \big|_{t_2} \quad (3.13)$$

Mode (b): The equivalent circuit is given in Fig. 3.4. At  $t=t_2$ , the switch  $S_0$  is gated off, whereas the capacitor  $C_0$  sources the dc bus switch current  $I_{S0}$ . In this mode the current  $I_{S0}$  can be considered as a constant current source. The voltage across  $C_0$  as a function of time is given by:

$$V_{C0}(t) = - \frac{I_{S0}(t) \big|_{t_2} t}{C_0} + V_{C0}(t_2) \quad (3.14)$$

This mode ends at  $t_3$ , when the capacitor  $C_0$  is discharged to zero:

$$V_{C0}(t_3) = 0 \quad (3.15)$$

whereas the voltage across  $L_m$  is also equal to zero:

$$V_{Lm}(t_3) = 0 \quad (3.16)$$

this moment  $t_3$  can be calculated as follows:

$$t_3 = \frac{C_0 V_s}{I_{S0} \big|_{t_2}} + t_2 \quad (3.17)$$

Mode (c): The equivalent circuit of this mode is illustrated in Fig. 3.5. The voltages across  $C_0$  or  $L_m$  is zero. The currents through the inverter switches are clamped at the maximum values of:

$$I_{S1} = I_{S2} = \frac{1}{2} ( I_{Lm} + I_{R1} ) \big|_{t_2} \quad (3.18)$$

whereas the currents through  $D_1$  and  $D_2$  are given by:

$$I_{D1} = I_{D2} = \frac{1}{2} ( I_{Lm} + I_{R1} ) \big|_{t_2} \quad (3.19)$$

In the load circuit, the current  $I_{R1}$  begins decreasing and freewheeling through  $D_{r1}$  and is given by:

$$I_{R1}(t) = I_{R1} \Big|_{t_2} e^{-\frac{R_1}{L_f} t} \quad (2.20)$$

This mode ends at  $t=t_4$ , when the inverter switches  $S_1$  and  $S_2$  are turned off at zero voltage condition having zero turn-off losses. The time  $t_4$  can be calculated as follows:

$$t_4 = \frac{D_{S1/2}}{F_{S1/2}} \quad (3.21)$$

where  $D_{S1/2}$  and  $F_{S1/2}$  are the duty cycle and the switching frequency of the inverter switches.

Mode (d): The equivalent circuit of this mode is depicted in Fig. 3.6. At  $t_4$ , all the switches  $S_0$ ,  $S_1$  and  $S_2$  are off. The voltage across  $L_m$  equals zero. The current through  $L_o$ , which has the initial maximum value of  $(I_{Lm} + I_{R1}) \Big|_{t_2}$ , begins charging  $C_o$ . This current flows through  $D_1$  and  $D_2$  back to the dc bus. As a function of time, this current is given by:

$$I_{L0}(t) = I_{L0}(\max) \cos(\omega_r t) \quad (3.22)$$

where,

$$I_{L0}(\max) = (I_{Lm} + I_{R1}) \Big|_{t_2} \quad (3.23)$$

$$\omega_r = \frac{1}{\sqrt{L_o C_o}} \quad (3.24)$$

In the load circuit, the current  $I_{R1}$  undergoes a commutating period from  $D_{r1}$  to  $D_{r2}$ . The currents  $I_{D_{r1}}$  and  $I_{D_{r2}}$  as function of time are given by:

$$I_{Dr1}(t) = \frac{-I_{R1}|_{t_4} t}{t_5 - t_4} + I_{R1}|_{t_4} \quad (3.25)$$

$$I_{Dr2}(t) = \frac{I_{R1}|_{t_4} t}{t_5 - t_4} \quad (3.26)$$

where,

$$I_{R1}|_{t_4} = I_{R1}|_{t_2} e^{-\frac{R_1}{L_f} t_4}$$

The voltage across  $C_0$  as a function of time is given by:

$$V_{C0}(t) = \frac{1}{C_0} \int_0^t I_{L0}(t) dt \quad (3.27)$$

This time interval ends at  $t=t_5$ , at which time  $I_{L0} = I_{Lm}|_{t_2}$ . The time  $t_5$  can be calculated as follows:

$$t_5 = \frac{\pi}{\omega_r 180} \cos^{-1} \left( \frac{I_{Lm}|_{t_3}}{(I_{Lm} + I_{R1})|_{t_3}} \right) + t_4 \quad (3.28)$$

at this time,

$$I_{Dr1} = 0 \quad \text{and} \quad I_{Dr2} = I_{R1}|_{t_4} = I_{R1}|_{t_5}$$

at the same time, the voltage across  $C_0$  is given by:

$$V_{C0}(t_5) = \frac{1}{C_0} \int_{t_4}^{t_5} I_{L0}(t) dt \quad (3.29)$$

Mode (e): The equivalent circuit is shown in Fig. 3.7: At  $t_5$ , the current  $I_{Lm}$ , which can be considered constant continues charging  $C_0$ . The voltage across  $C_0$  is given by:

$$V_{C0}(t) = \frac{I_{Lm}|_{t_2} t}{C_0} + V_{C0(05)} \quad (3.30)$$

whereas the voltage across  $L_m$  is given by:

$$V_{Lm}(t) = - V_{C0}(t) \quad (3.31)$$

This time interval ends at  $t=t_6$ , when the voltages across  $C_0$  and  $L_m$  are:

$$V_{C0(06)} = V_s \quad (3.32)$$

$$V_{Lm(06)} = - V_s \quad (3.33)$$

The time  $t_6$ , can be calculated as follows:

$$t_6 = \frac{C_0 (V_s - V_{C0(05)})}{I_{Lm}|_{t_2}} + t_5 \quad (3.34)$$

Mode (f): The equivalent circuit is presented in Fig. 3.8. The dc bus switch  $S_0$  is gated on at zero voltage. The current  $I_{Lm}$  is shifted to the antiparallel diode  $D_0$  of the dc bus switch  $S_0$ . Thus the rest energy of  $L_m$  is transferred to the source until  $t=t_7$ , at which time  $I_{Lm}=0$ . In the load circuit,  $I_{R1}$  keeps freewheeling through  $D_{r2}$ , and decreasing towards the minimum value  $I_{R1(min)}$  which is given by Equation (3.8).

At  $t=t_7$  the end of the switching cycle, the voltage and the current through  $L_m$  reach zero. In order to simplify the calculation of the time  $t_7$ , the current  $I_{Lm}|_{t_2}$  is considered constant during the time interval  $t_2 \rightarrow t_6$ . In other words, the energy transferred from  $L_m$  to  $C_0$  is considered negligible. Hence the time  $t_7$  can be computed from:



$$t_7 = \frac{L_m I_{Lm} |_{t_2}}{V_s} + t_6 \quad (3.35)$$

### 3.5 Design GuideLines

In this section, design guidelines for selecting the converter component values will be provided. In particular,  $L_o$  and  $C_o$  will be designed to yield soft switching condition for the inverter switches. The output power  $P_o$ , the input voltage  $V_s$ , the switching frequency of the inverter switches  $F_{inv}$ , and the switching frequency of the dc bus switch  $F_{so}$ , are the key converter design parameters.

-The maximum achievable duty cycles of the dc bus switch, and for the inverter switches are given by:

$$D_{so(max)} = 1 - \left[ (t_6 - t_2) - (t_4 - t_3) \right] F_{inv} \quad (3.36)$$

$$D_{inv(max)} = \frac{t_4}{t_7 - (t_4 - t_3)} \quad (3.37)$$

-The output filter  $L_r$  is chosen according to the acceptable ripple current  $\Delta I_{r1}$ . From (3.10)  $L_r$  can be given by:

$$L_r = \frac{(1 - t_2 F_{inv})}{\Delta I_{r1}} V_s t_2 \quad (3.38)$$

where  $t_2$  is given by (3.11).

-The magnetizing inductor of the transformer  $L_m$  is selected from (3.2):

$$L_m = \frac{V_s}{\frac{\Delta I_{Lm}}{\Delta t}} \quad (3.39)$$

where,

$$\Delta t = t_7 - t_4 \leq \frac{T_{inv}}{2} \quad \text{and} \quad T_{inv} = \frac{1}{F_{inv}}$$

-The  $dI_{Lo}/dt$  limiting inductor  $L_o$  is selected to produce smooth current rise through the inverter switches. If  $dI_{Lo}/dt$  is chosen in the range 60-100 (A/ $\mu$ s), the turn-on losses are nearly zero. The switch  $dI_{Lo}/dt$  is given by:

$$\frac{dI_{Lo}}{dt} = \frac{V_s}{L_o} \quad (3.40)$$

An additional variable in choosing  $L_o$  and  $C_o$  is the time interval  $(t_5-t_4)$  Equation (3.28), during which the charging current through  $C_o$  goes from the value of  $(I_{Lm} + I_{R1})|_{t_2}$  to the value of  $I_{Lm}|_{t_2}$ .

-The dc bus parallel capacitor  $C_o$  is designed to provide a soft turn-off switch condition assisted by the dc bus switch  $S_o$ . At the worst case, when the load current equals zero,  $C_o$  is designed as follows:

$$C_o = \frac{I_{Lm}|_{t_2}}{\frac{dv}{dt}} \quad (3.41)$$

where,

$$I_{Lm}|_{t_2} = \frac{V_s}{L_m} t_2 = \frac{V_s}{L_m} \frac{D_{s_o}}{F_{s_o}}$$

and at rated load condition  $C_o$  will be:

$$C_o = \frac{I_{s_o}|_{t_2}}{\frac{dv}{dt}} \quad (3.42)$$

where,

$$I_{so}|_{t_2} = (I_{Lm} + I_{R1})|_{t_2} = (I_{Lm})|_{t_2} + \frac{D_{so}}{F_{so}} F_{in} \frac{V_s}{R1}$$

and,

$$R1 = \frac{V_o^2}{P_o} = \frac{\left( \frac{D_{so}}{F_{so}} F_{inv} V_s \right)^2}{P_o}$$

### 3.6 Design Example

The design example presented in this section will use the equations in section 3.5 to provide guidelines for component selection. It will present the calculated values for the dc bus capacitor Co, the di/dt limiting inductor Lo, the magnetizing inductance of the high frequency isolating transformer Lm and the output filter Lr of the converter shown in Fig. 3.1. The design is performed with the following assumptions:

output power	Po= 5 (Kw)
input voltage	Vs= 300 (V)
maximum dc bus switch duty cycle	Dso= 0.84
maximum inverter switches duty cycle	Dinv= 0.48
dc bus switching frequency	Fso= 40 (KHz)
inverter switching frequency	Finv= 20 (KHz)
ripple output current	ΔIR1= 3.75 % IR1(ave)
current-increase rate through Lm	ΔILm/Δt= 1 (A/μs)
current-increase rate through Lo	dILO/dt= 75 (A/μs)
charging rate of Co, at no load	dv/dt= 400 (V/μs)

The equations given in section 3.5 and the above assumptions have been used to calculate the converter component values. The results are given bellow:

output filter	Lr= 1 (mH)
magnetizing inductance	Lm= 0.3 (mH)

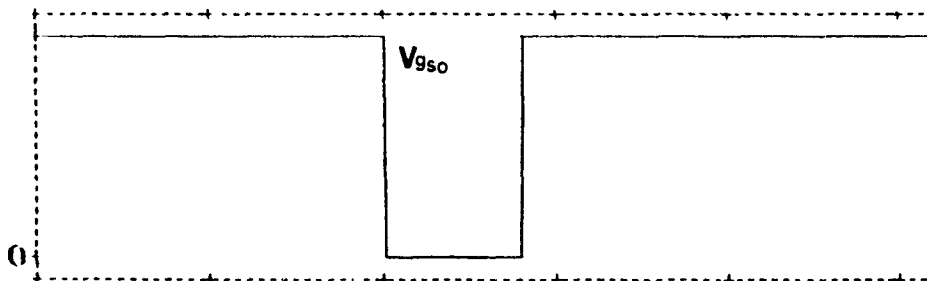
di $L_o$ /dt limiting inductance  $L_o = 4 \text{ } (\mu\text{H})$

dc bus capacitor  $C_o = 0.05 \text{ } (\mu\text{F})$

The value of  $C_o$  computed above is selected according to no load condition, where  $dv/dt = 400 \text{ (V}/\mu\text{s)}$ . At rated load condition,  $dv/dt$  will be increased to the value of  $1300 \text{ (V}/\mu\text{s)}$  which is still acceptable. Thus, the selected  $C_o$  value designed by using Equation (3.41), results in nearly zero turn-off losses of the inverter switches from no load to full load Conditions.

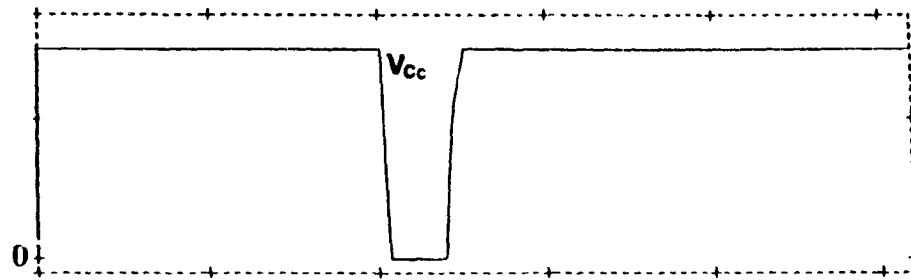
### 3.7 Simulation Results

In this section, the converter parameters and the converter component values obtained in the previous section, have been used and tested at different duty cycles. Pspice package described in reference [18] was utilized to simulate the performance of the examined dc-dc topology shown in Fig. 3.1 and to prove the results predicted thus far in this chapter. In particular, Figs. 3.9 (a) to 3.9 (h) show part of the simulation results. The obtained modes of operation are as theoretically predicted, especially the zero losses switching behaviors of the dc bus switch and of the inverter switches.



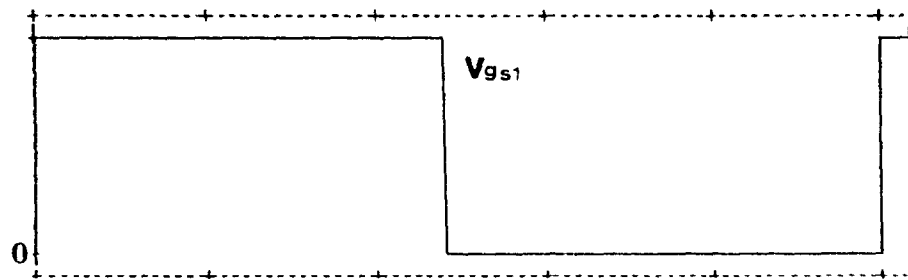
$V_{gso} = 5 \text{ (V)/div}$ ,  $t = 10 \text{ } (\mu\text{s)/div}$

Fig. 3.9 (a) The Gating Signal of Switch  $S_o$



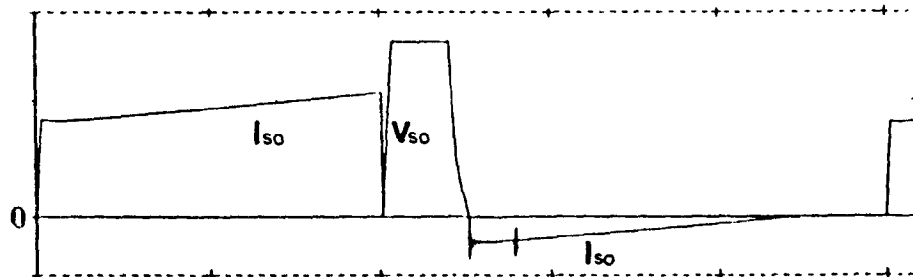
$V_{co} = 200$  (V/div),  $t = 10$  ( $\mu$ s/div)

Fig. 3.9 (b) The Voltage Across  $C_o$



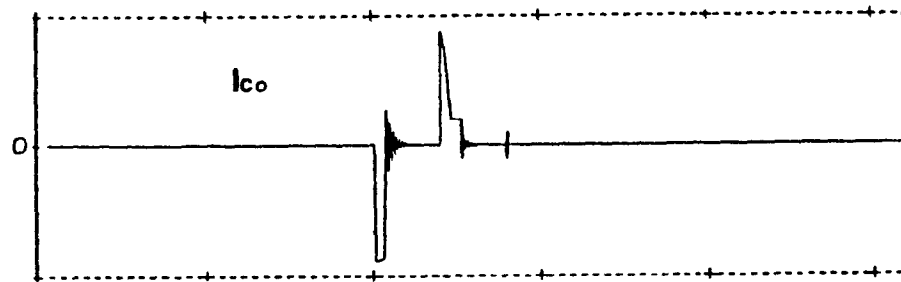
$V_{gs1/2} = 5$  (V/div),  $t = 10$  ( $\mu$ s/div)

Fig. 3.9 (c) The Gating Signals of the Switches  $S_1$  and  $S_2$



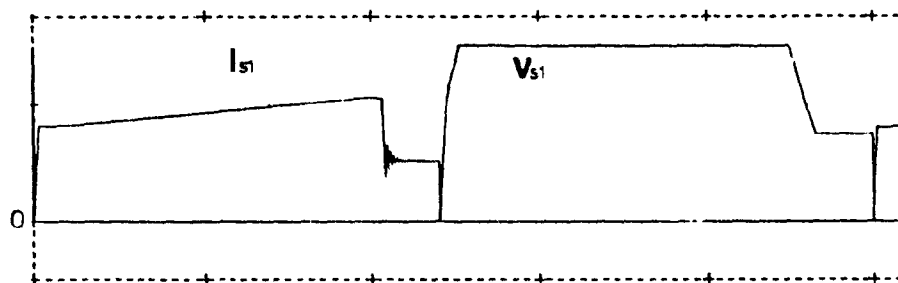
$V_{so} = 50$  (V)/div,  $I_{so} = 13.8$  (A)/div,  $t = 10$  ( $\mu$ s)/div

Fig. 3.9 (d) The Voltage and the Current Through  $S_o$



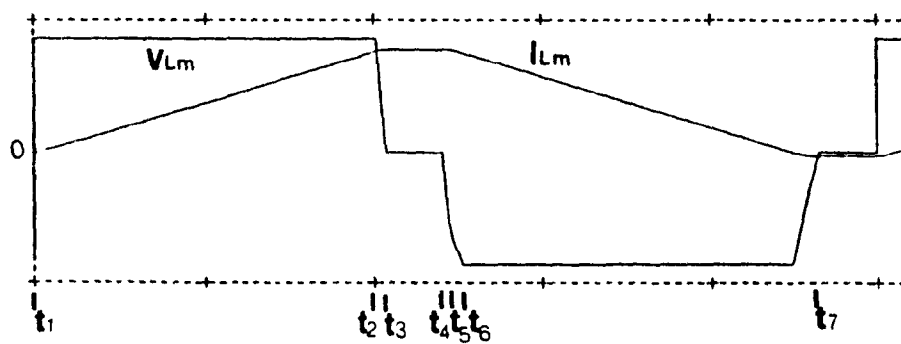
$I_{co} = 10 \text{ (A)/div}$ ,  $t = 10 \text{ (}\mu\text{s)/div}$

Fig. 3.9 (e) The Current Through the Capacitor  $C_o$



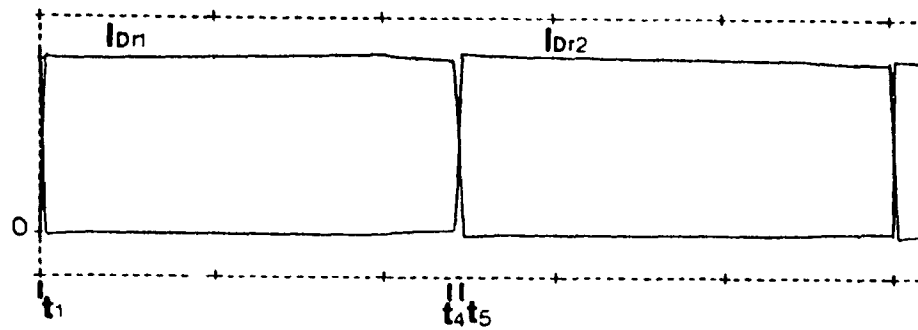
$V_{s1/2} = 50 \text{ (V)/div}$ ,  $I_{s1/2} = 13.8 \text{ (A)/div}$ ,  $t = 10 \text{ (}\mu\text{s)/div}$

Fig. 3.9 (f) The Current and the Voltage Through  $S_1/S_2$



$V_{lm} = 100 \text{ (V)/div}$ ,  $I_{lm} = 8.4 \text{ (A)/div}$ ,  $t = 10 \text{ (}\mu\text{s)/div}$

Fig. 3.9 (g) The Current and the Voltage Through  $L_m$



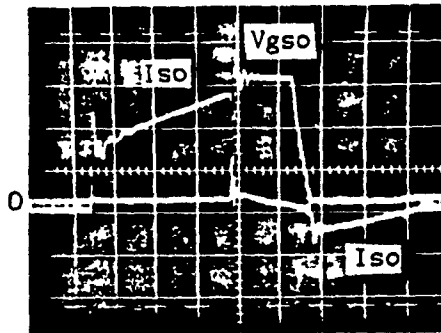
$$I_{Dr1} = I_{Dr2} = 9.3 \text{ (A)/div, } t = 10 \text{ (}\mu\text{s)/div}$$

Fig. 3.9 (h) The Currents Through  $D_{r1}$  and  $D_{r2}$

### 3.8 Experimental Results

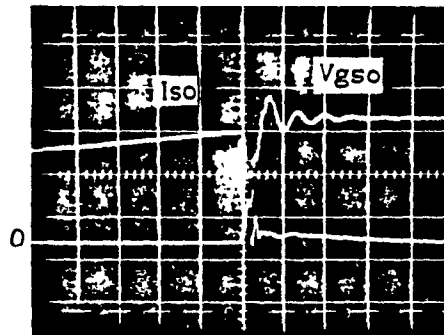
This section is provided to establish the feasibility of the improved PWM dc-dc converter Fig. 3.1 and to verify the analytical and simulated results. A 1 Kw laboratory unit operating at 20 KHz switching frequency was built and tested successfully. This unit has used the same converter parameters and component values obtained in section 3.6.

Key experimental results corresponding to the predicted and simulated ones are shown in Fig. 3.10. In particular, Figs. 3.10 (a) and 3.10 (b) show that as predicted the actual switching losses for the dc bus switch  $S_0$  are nearly zero. The same conclusion applies to Figs. 3.10 (c), 3.10 (d) and 3.10 (e), which show the voltage and current for one of the inverter switches (e.g. switch  $S_1$ ).



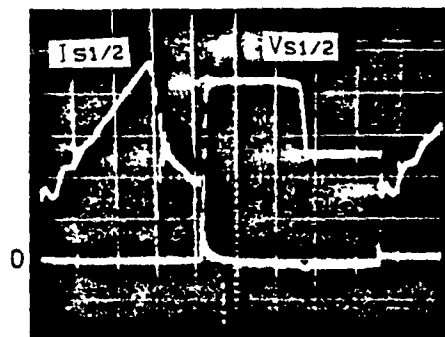
$V_{so} = 66 \text{ (V/div)}$ ,  $I_{so} = 8 \text{ (A/div)}$ ,  $t = 5 \text{ (}\mu\text{s/div)}$

Fig. 3.10 (a) The Voltage and the Current Through  $S_o$



$V_{so} = 66 \text{ (V/div)}$ ,  $I_{so} = 8 \text{ (A/div)}$ ,  $t = 1 \text{ (}\mu\text{s/div)}$

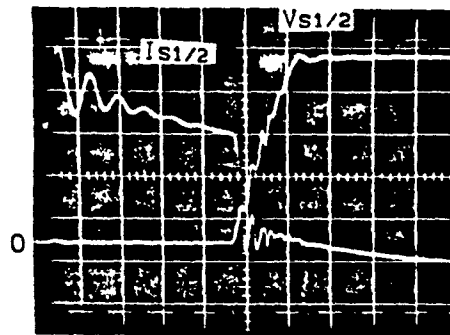
Fig. 3.10 (b) The Turn-off Period of the Switch  $S_o$



$V_{s1/2} = 50 \text{ (V/div)}$ ,  $I_{s1/2} = 4.76 \text{ (A/div)}$ ,  $t = 5 \text{ (}\mu\text{s/div)}$

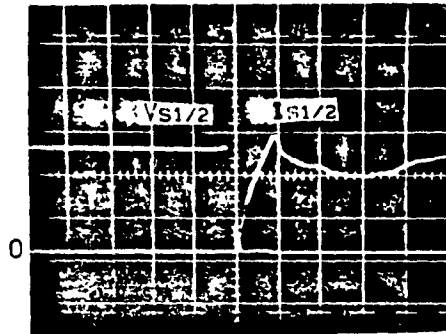
Fig. 3.10 (c) The Voltage and the Current Through  $S_1$





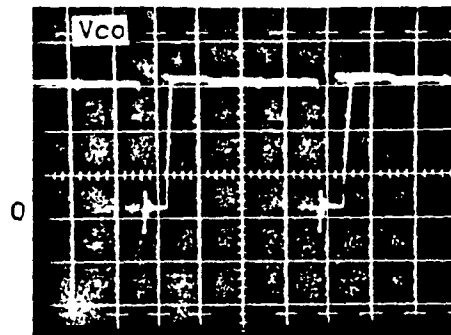
$V_{s1/2} = 50 \text{ (V)/div}$ ,  $I_{s1/2} = 4.76 \text{ (A)/div}$ ,  $t = 1 \text{ (}\mu\text{s)/div}$

Fig. 3.10 (d) The Turn-off Period of the Switch  $S_1$



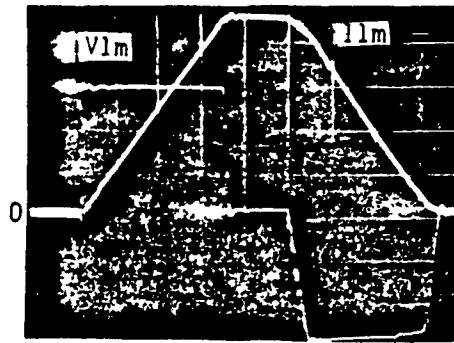
$V_{s1/2} = 50 \text{ (V)/div}$ ,  $I_{s1/2} = 4.76 \text{ (A)/div}$ ,  $t = 1 \text{ (}\mu\text{s)/div}$

Fig. 3.10 (e) The Turn-on Period of the Switch  $S_1$



$V_{co} = 66 \text{ (V)/div}$ ,  $t = 5 \text{ (}\mu\text{s)/div}$

Fig. 3.10 (f) The Voltage Across the Capacitor  $C_o$



$V_{lm} = 66 \text{ (V)/div}$ ,  $I_{lm} = 2.26 \text{ (A)/div}$ ,  $t = 5 \text{ (}\mu\text{s)/div}$

Fig. 3.10 (g) The Voltage and the Current Through  $L_m$

### 3.9 Conclusions

A detailed analysis and design procedure for the dc bus commutated half-bridge forward PWM, dc-dc converter Fig. 3.1 have been provided in this chapter. The effective use of the dc bus commutating subcircuit topology No. (1) Fig. 2.13, implemented in the analyzed topology Fig. 3.1, has yielded zero-voltage switching condition for the inverter switches as well as for the dc bus switch.

Thus, the resulting half-bridge topology Fig. 3.1 can be used to convert low power at high switching frequency with nearly zero switching losses. Theoretical results have been verified experimentally on a 1 Kw 20 KHz laboratory prototype. The next chapter will be devoted to study the implementation of the second proposed dc bus commutating topology shown in Fig. 2.14, for a full-bridge dc/dc converter.

## CHAPTER 4

### ANALYSIS AND DESIGN OF A FULL-BRIDGE DC BUS SOFT COMMUTATED PWM DC/DC CONVERTER

In this chapter, the implementation of the proposed dc bus commutating subcircuit topology No. (2) shown in Fig. 2.14, with additional load current commutation subcircuit in a full-bridge PWM dc/dc converter topology is treated in detail. In particular, the following sections are devoted to explore the operation and performance of the resulting dc bus commutated full-bridge converter shown in Fig. 4.1.

In section 4.1, an introduction about the advantages obtained by the implementation of the proposed commutating subcircuit is provided.

In section 4.2, a complete identification of all modes of operation, including the inverter switching conditions are addressed.

In section 4.3, a complete mathematical analysis of all modes of operation is presented.

In section 4.4, design guidelines to select the component values are provided.

In section 4.5, a design example using the equations obtained in the previous section is presented.

In section 4.6, simulation results of the key currents and voltages are obtained. In particular, the switching behavior of converter switches is examined.

In section 4.7, experimental results are provided to prove that operation under zero-voltage zero-current switching conditions is indeed achieved.

In section 3.8, conclusions of this chapter are provided.

#### 4.1 Introduction

A full-bridge PWM dc/dc converter topology using the proposed dc bus commutating subcircuit shown in Fig. 2.14 to accomplish zero-voltage switching condition. In addition, the converter utilizes a load current commutating subcircuit consisting of L and C elements to yield zero-current switching condition. The resulting full-bridge pwm dc/dc converter is shown in Fig. 4.1.

The above mentioned topology can be used in medium power applications, and at high switching frequencies. Zero switching losses for the inverter switches, and for the dc bus switch are achieved under rated to nearly no load operating conditions. As compared to other topologies which incorporate the dc bus commutation approaches described in [13,14], the proposed topology has the following advantages:

- i) Only one subcircuit is required to commute all inverter switches at zero-voltage.
- ii) Increased reliability due to lower switching stresses.
- iii) Decreased circuit complexity resulting from reduced parts count, and
- iv) The dc bus switch can be used to isolate and protect the inverter from the dc bus under adverse system operating conditions.

The proposed full-bridge pwm dc/dc converter topology shown in Fig. 4.1 consists of three sections:

- 1) The dc bus which includes the input dc voltage  $V_s$ , the dc bus commutating subcircuit which in turn consists of a switch  $S_0$ , capacitors  $C_1$  and  $C_2$ , an inductor  $L_s$  and diodes  $D_1$ ,  $D_2$  and  $D_3$ .
- 2) The inverter section including switches  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$ , the load current commutation section which in turn includes capacitor  $C_c$  and inductor  $L_c$ , which represents the leakage inductance of the high frequency transformer T.

- 3) The rectifier section consisting of the diodes  $D_{r1}$ ,  $D_{r2}$ ,  $D_{r3}$  and  $D_{r4}$ , and filter inductor  $L_f$  connected to the Load represented by resistor  $R_l$ .

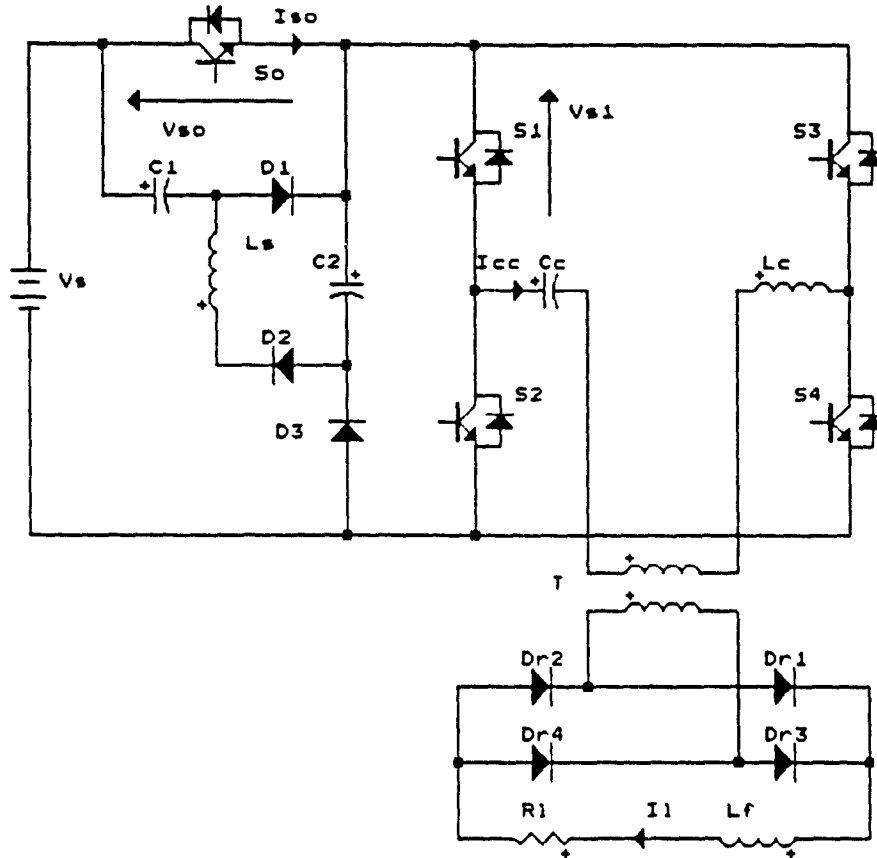


Fig 4.1 A Full-Bridge Dc Bus Commutated PWM Dc/Dc Converter

#### 4.2 Modes of Operation

In this section all modes of operation of the proposed topology shown in Fig. 4.1 are defined. It is shown that the system operates in six distinct modes during a switching cycle. These modes are a, b, c, d, e and f. The performance of the circuit in each mode is next explained.



current passes through  $S_0$ ,  $S_1$ ,  $C_c$ ,  $D_{r1}$ ,  $R_l$ ,  $L_f$ ,  $D_{r4}$ ,  $L_c$ ,  $S_4$  and the voltage source  $V_s$ . It keeps increasing linearly until  $t_3$  the end of this mode. The voltage across the capacitor  $C_c$  also keeps increasing linearly from the negative value  $V_{C_c(02)}$  to the positive value  $V_{C_c(03)}$ .

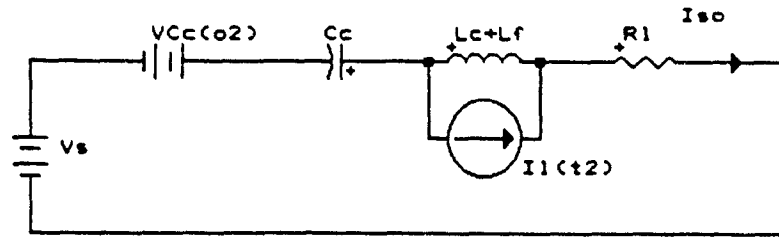


Fig. 4.3 The Equivalent Circuit of Mode (b), Topology Fig. 4.1,  $t_2 \rightarrow t_3$

Mode (c): The equivalent circuit of this mode is depicted in Fig. 4.4. At  $t_3$ , the dc bus switch  $S_0$  is turned off and the capacitor  $C_1$  begins sourcing the load current  $I_l$  which can be considered constant. This current passes through  $D_{r1}$ ,  $S_1$ ,  $C_c$ ,  $D_{r1}$ ,  $R_l$ ,  $L_f$ ,  $D_{r4}$ ,  $L_c$ ,  $S_4$  and  $V_s$ . The charging rate of  $C_1$  controls  $dv/dt$  across  $S_0$  resulting in zero-voltage  $S_0$  turn-off condition. This mode ends at  $t_4$ , at which moment the input dc voltage  $V_s$  minus the capacitor  $C_1$  voltage equals the voltage across  $C_2$ ,  $V_s - V_{C_1(04)} = V_{C_2(02)}$ .

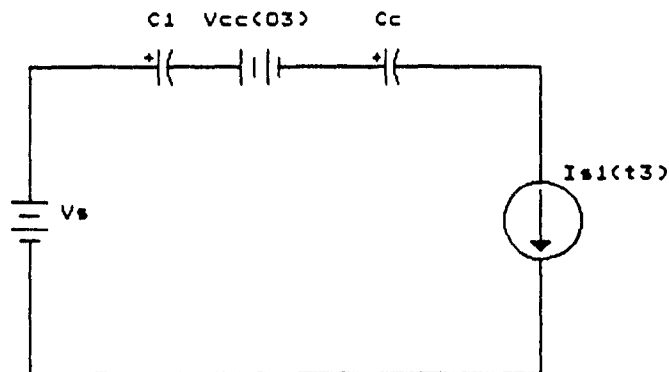


Fig. 4.4 The Equivalent Circuit of Mode (c), Topology Fig. 4.1,  $t_3 \rightarrow t_4$

Mode (d): The equivalent circuit is illustrated in Fig. 4.5. At  $t_4$ , the  $C_1$  voltage equals  $C_2$  voltage. This condition forces  $C_1$  and  $C_2$  to temporarily share the load current  $I_1$  which can be considered constant. This current  $I_1$  keeps charging the capacitor  $C_c$  until  $t_5$ . At this moment, the voltage across  $C_c$  reaches  $V_{c(05)}$  which is equal to  $C_2$  capacitor voltage or to the input dc voltage  $V_s$  minus  $C_1$  voltage,  $V_{c(05)} = V_{c2} = V_s - V_{c1}$ . While the currents through  $C_1$  and  $C_2$  as well as the inverter output voltage fall to zero.

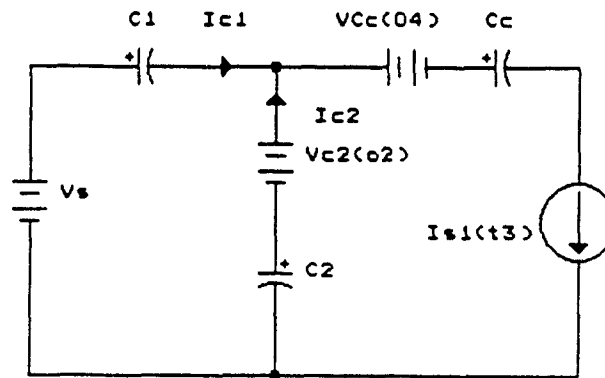


Fig. 4.5 The Equivalent Circuit of Mode (d), Topology Fig. 4.1,  $t_4 \rightarrow t_5$

Mode (e): The equivalent circuit of this mode is shown in Fig. 4.6. At  $t_5$ ,  $I_{c1} = I_{c2} = 0$ , while the current in the inverter circuit  $I_{cc}$  begins freewheeling. Half of  $I_{cc}$  freewheels through  $S_1$ ,  $C_c$ ,  $L_c$  and the  $S_3$  antiparallel diode. Whereas, the other half freewheels through  $S_4$ ,  $C_c$ ,  $L_c$  and the  $S_2$  antiparallel diode. While this current freewheels it decreases toward zero at a rate dictated by  $V_{c(05)}/L_c$ . At  $t_6$ , the current  $I_{cc}$  becomes zero and the voltage across  $C_c$  reaches the maximum positive value  $V_{c(06)}$ .

Mode (f): The equivalent circuit of this mode is shown in Fig. 4.7. At  $t_6$ , the  $C_c$  Voltage,  $V_{c(06)}$  is slightly larger than the  $C_2$  voltage  $V_{c2(05)}$  or than the input dc voltage  $V_s$  minus  $C_1$  voltage,  $V_{c1(05)}$ :  $V_{c(06)} > V_{c2(05)}$  or  $V_{c(06)} > V_s - V_{c1(05)}$ .



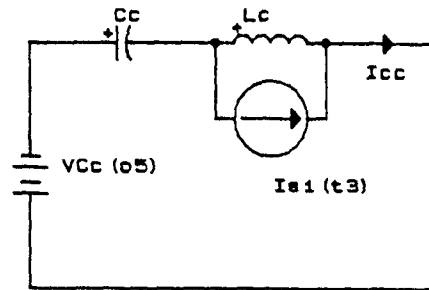


Fig. 4.6 The Equivalent Circuit of Mode (e), Topology Fig. 4.1,  $t_5 \rightarrow t_6$

This condition forces  $C_c$  to discharge via  $L_c$  and the antiparallel diodes of  $S_1$  and  $S_4$  to the value of  $V_{c1}(07)$ , sending current back to the dc bus. This current will charge  $C_2$  to  $V_{c2}(07)$  and discharge  $C_1$  to  $V_s - V_{c1}(07)$ .

It should be noted that the value  $V_{c1}(07)$  will be the initial voltage of  $C_c$  at the beginning of the negative half cycle. Therefore, it is equal to the absolute initial value  $V_{c1}(01)$ . Since the  $C_c$  discharging current passes through the  $S_1$  and  $S_4$  antiparallel diodes, the switches  $S_1$  and  $S_4$  can now be turned off at zero-voltage zero-current condition, thus yielding zero turn-off switching losses.

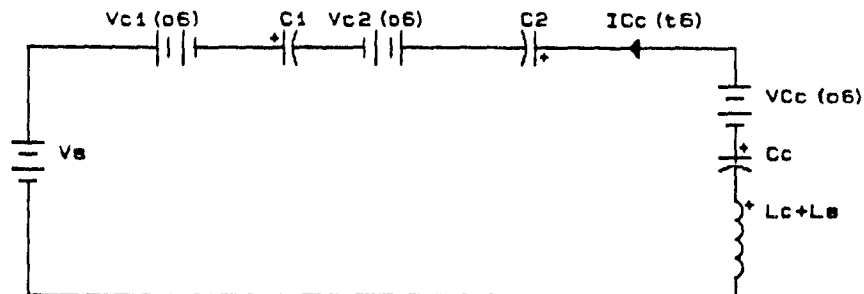


Fig. 4.7 The Equivalent Circuit of Mode (f), Topology Fig. 4.1,  $t_6 \rightarrow t_7$

In the rectifier circuit and during the time interval  $t_3 \rightarrow t_7$ , the load

current begins freewheeling and decreasing toward its minimum value which is dictated by  $R_1$  and  $L_f$ . This current flows through  $R_1$ ,  $L_f$ ,  $D_{r1}$ ,  $D_{r2}$ ,  $D_{r3}$  and  $D_{r4}$ . The equivalent load circuit in this time interval is shown in Fig. 4.8. By now, all modes of operation through the positive half cycle have been defined and the modes in the negative half cycle can be defined and analyzed in similar manner.

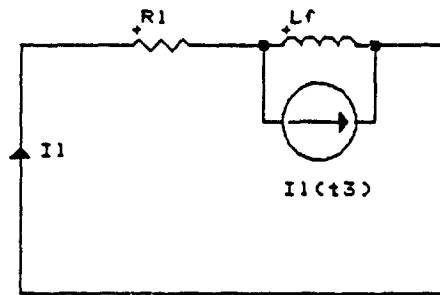


Fig. 4.8 The Equivalent Load Circuit, Topology Fig. 4.1,  $t_3 \rightarrow t_7$

#### 4.3 Circuit Analysis

Here, the analytical expressions describing all modes of operation of the proposed converter topology Fig. 4.1 are presented. The expressions for currents and voltages, during all subsequent modes of operation, are obtained by assuming the following:

- i) All the converter components are ideal.
- ii) The input voltage is a stiff dc.
- iii) The commutating subcircuit inductor  $L_s$  is air cored, and
- iv) The turns ratio of the high frequency isolating transformer is one.

Mode (a): The equivalent circuit is shown in Fig. 4.2. The current through  $S_0$ , as a function of time,  $I_{s0}(t)$  is given by:

$$I_{s0}(t) = I_{s1}(t) + I_{sn}(t) \quad (4.1)$$

where,

$$I_{s1}(t) = I_{s4}(t) = I_1(t) = I_{c2}(t) \quad (4.2)$$

$$= e^{-t} [B_1 \cos(\omega_1 t) + B_2 \sin(\omega_1 t)]$$

and,

$$I_{sn}(t) = \frac{V_s + 2 V_{C2(01)}}{L_s \omega_s} \sin(\omega_s t) \quad (4.3)$$

and where,

$$\omega_1 = \sqrt{\omega_0^2 - \xi^2}$$

$$B_1 = I_1(\min) \quad \text{and} \quad B_2 = \frac{\left. \frac{dI_{s1}}{dt} \right|_{t_1} + \xi B_1}{\omega_1}$$

$$\xi = \frac{R_1}{2(L_f + L_c)} \quad \text{and} \quad \omega_0 = \frac{\left. \frac{dI_{s1}}{dt} \right|_{t_1} + \xi B_1}{\omega_1}$$

$$\left. \frac{dI_{s1}}{dt} \right|_{t_1} = V_s - V_{C2(01)} - I_1(\min) R_1$$

$$\omega_s = \frac{1}{\sqrt{L_s C_{eq1}}} \quad \text{and} \quad C_{eq1} = \frac{C_1 C_2}{C_1 + C_2}$$

$V_{C2(01)}$  and  $I_1(\min)$  will be calculated at the end of this section. At  $t_1=0$ , the voltages across  $C_1$  and  $C_2$  are given by:

$$V_{C1(01)} = V_s + V_{C2(01)} \quad (4.4)$$

$$V_{C2(01)} = V_{C2(01)} \quad (4.5)$$

The capacitor  $C_1$  could be considered as a voltage source since it begins to transfer its stored charge to  $C_2$ . The transferred charge can be calculated as follows:

$$Q = C_1 V_{C1} = C_2 V_{C2} \quad (4.6)$$

whereas the  $C_1$  and  $C_2$  voltages as functions of time can be given by:

$$V_{C1}(t) = -\frac{1}{C_1} \int_0^t I_{Sn}(t) dt + V_{C1}(01) \quad (4.7)$$

$$V_{C2}(t) = \frac{1}{C_2} \int_0^t I_{Sn}(t) dt + V_{C2}(01) \quad (4.8)$$

and the voltage across  $C_c$  is given by:

$$V_{Cc}(t) = \frac{1}{C_c} \int_0^t I_{S1}(t) dt + V_{Cc}(01) \quad (4.9)$$

At the end of this mode, when  $t=t_2=(\pi/\omega_s)$  and  $I_{Sn}=0$  the voltages across  $C_1$ ,  $C_2$  and  $C_c$  are:

$$V_{C1}(02) = 0 \quad (4.10)$$

$$V_{C2}(02) = \frac{C_1}{C_2} (V_s + V_{Cc}(01)) - V_{Cc}(01) \quad (4.11)$$

$$V_{Cc}(02) = \frac{1}{C_c} \int_{t1}^{t2} I_{S1}(t) dt + V_{Cc}(01) \quad (4.12)$$

Mode (b): The equivalent circuit is illustrated in Fig. 4.3. The dc bus switch current  $I_{S0}$  as a function of time is given by:

$$I_{S0}(t) = e^{-\xi t} [ B_1 \cos(\omega_1 t) + B_2 \sin(\omega_1 t) ] \quad (4.13)$$

It is also given by:

$$I_{S0}(t) = I_{S1}(t) = I_{S4}(t) = I_{Cc}(t) = I_l(t) \quad (4.14)$$

This current reaches the maximum value at  $t_3$ , the end of this mode. The time

$t_3$  is given by:

$$t_3 = \frac{D_{s0}}{F_{s0}} \quad (4.15)$$

where  $D_{s0}$  and  $F_{s0}$  are the duty cycle and the switching frequency of the dc bus switch  $S_0$ . The voltage across  $C_c$  at  $t_3$  will be:

$$V_{Cc(03)} = \frac{1}{C_c} \int_{t_2}^{t_3} I_{Cc(t)} dt + V_{Cc(02)} \quad (4.16)$$

The voltages across  $C_1$  and  $C_2$  keep their previous values which are:

$$V_{C1(03)} = V_{C1(02)} = 0 \quad (4.17)$$

$$V_{C2(03)} = V_{C2(02)} = \frac{C_1}{C_2} (V_s + V_{Cc(01)}) - V_{Cc(01)} \quad (4.18)$$

Mode (c): The equivalent circuit is depicted in Fig. 4.4. At  $t_3$ , the dc bus switch is gated off and  $C_1$  carries the load current  $I_1|_{t_3}$  which is considered a constant current source. This current is given by:

$$\begin{aligned} I_1|_{t_3} &= I_{s1}(t_3) = I_{s4}(t_3) = I_{Cc}(t_3) \\ &= e^{-\xi t_3} [ B_1 \cos(\omega_1 t_3) + B_2 \sin(\omega_1 t_3) ] \end{aligned} \quad (4.19)$$

At  $t_4$ , the voltage across  $C_c$  is:

$$V_{Cc(04)} = \frac{1}{C_c} I_1|_{t_3} (t_4 - t_3) \quad (4.20)$$

and the voltages across  $C_1$  and  $C_2$  are:

$$V_{C1(04)} = \frac{I_1|_{t_3}}{C_1} (t_4 - t_3) = V_s - V_{Cc(04)} = V_{C2(02)} \quad (4.21)$$

$$V_{C2(04)} = V_{C2(02)} \quad (4.22)$$

The time  $t_4$  can be calculated by using the following expression:

$$\begin{aligned} t_4 &= \frac{C_1 V_{C2(02)}}{I_1|_{t_3}} + t_3 \\ &= \frac{C_1}{I_1|_{t_3}} \left( \frac{C_1}{C_2} (V_s + V_{Cc(01)}) - V_{Cc(0)} \right) + t_3 \end{aligned} \quad (4.23)$$

Mode (d): The equivalent circuit is given in Fig. 4.5. At  $t_4$ ,  $C_2$  begins discharging and sharing the load current with capacitor  $C_1$ . The currents through  $C_1$  and  $C_2$  can be calculated from the following two expressions:

$$I_{C1} = I_1|_{t_3} \frac{\frac{1}{C_2}}{\frac{1}{C_1} + \frac{1}{C_2}} = I_1|_{t_3} \frac{C_1}{C_1 + C_2} \quad (4.24)$$

$$I_{C2} = I_1|_{t_3} \frac{\frac{1}{C_1}}{\frac{1}{C_1} + \frac{1}{C_2}} = I_1|_{t_3} \frac{C_2}{C_1 + C_2} \quad (4.25)$$

The voltages across  $C_1$  and  $C_2$  as functions of time are:

$$V_{C1}(t) = \frac{I_1|_{t_3} t}{C_1 + C_2} + V_{C1(04)} \quad (4.26)$$

$$V_{C2}(t) = \frac{-I_1|_{t_3} t}{C_1 + C_2} + V_{C2(02)} \quad (4.27)$$

At  $t_5$ , the current  $I_{C1}=I_{C2}=0$ , whereas the voltage across  $C_c$  is given by the integral equation:

$$V_{Cc(05)} = \frac{1}{C_c} \int_{t_4}^{t_5} I_{Cc}(t) dt + V_{Cc(04)} \quad (4.28)$$

whereas the voltages across  $C_1$  and  $C_2$  are given by:

$$V_{C1(05)} = \frac{I_1|_{t_3} (t_5 - t_4)}{C_1 + C_2} + V_{C1(04)} = V_s - V_{Cc(05)} \quad (4.29)$$

$$V_{C2(05)} = \frac{-I_1|_{t_3} (t_5 - t_4)}{C_1 + C_2} + V_{C2(02)} = V_{Cc(05)} \quad (4.30)$$

The instant  $t_5$  can be calculated by:

$$t_5 = \frac{\pi}{\omega_2} + t_4 \quad (4.31)$$

where,

$$\omega_2 = \frac{1}{\sqrt{C_{eq2} L_c}} \quad \text{and} \quad C_{eq2} = \frac{(C_1 + C_2) C_c}{(C_1 + C_2) + C_c}$$

Mode (e): The equivalent circuit is shown in Fig. 4.6. At  $t_5$ ,  $I_{C1} = I_{C2} = 0$  and the current through the  $C_c$  and  $L_c$  is given by:

$$I_{Cc}(t) = I_1(\max) \cos(\omega_c t) - \frac{V_{Cc(05)}}{\omega_c L_c} \sin(\omega_c t) \quad (4.32)$$

where,

$$\omega_c = \frac{1}{\sqrt{C_c L_c}} \quad \text{and} \quad I_1(\max) = I_1(t)|_{t_3}$$

The current through  $S_1$  or  $S_4$  is:

$$I_{S1}(t) = I_{S4}(t) = \frac{1}{2} I_{Cc}(t) \quad (4.33)$$

$I_{Cc}$  reaches zero at  $t_6$ , which can be calculated by:

$$t_6 = \left[ \frac{\pi}{180 \omega_c} \operatorname{tg}^{-1} \left( \frac{I_1(\max) \omega_c L_c}{V_{Cc(05)}} \right) \right] + t_5 \quad (4.34)$$

whereas the voltage across  $C_c$  at  $t_6$  is given by:

$$V_{Cc(06)} = \frac{1}{C_c} \int_{t_5}^{t_6} I_{Cc}(t) dt + V_{Cc(05)} = V_{Cc(\max)} \quad (4.35)$$

While the voltages across  $C_1$  and  $C_2$  are keeping their previous mode values:

$$V_{C1(06)} = V_{C1(05)} \quad (4.36)$$

$$V_{C2(06)} = V_{C2(05)} \quad (4.37)$$

Mode (f): The equivalent circuit is illustrated in Fig. 4.7. At  $t_6$ , and since the following condition exists,  $V_{Cc(06)} > V_{C2(05)}$  or  $V_{Cc(06)} > V_s - V_{C1(05)}$ . The capacitor  $C_c$  begins to slightly discharge through  $L_c$  and the  $S_1$  and  $S_4$  antiparallel diodes back to the dc bus. This current  $I_{Cc(t)}$  will charge the capacitor  $C_2$  and discharge the capacitor  $C_1$ . As a function of time  $I_{Cc(t)}$  is given by:

$$I_{Cc(t)} = \left( \frac{V_{Cc(05)} - V_{Cc(06)}}{\omega_3 (L_c + L_s)} \right) \sin(\omega_3 t) \quad (4.38)$$

At  $t_7$ , the end of this mode and the end of the first half switching, the current  $I_{Cc(t)}$  becomes zero. The time  $t_7$ , can be calculated from:

$$t_7 = \frac{\pi}{\omega_3} + t_6 \quad (4.39)$$

where,

$$\omega_3 = \frac{1}{\sqrt{L_{eq} C_{eq3}}} \quad \text{and} \quad L_{eq} = L_s + L_c$$

$$C_{eq3} = \frac{C_{eq1} C_c}{C_{eq1} + C_c} \quad \text{and} \quad C_{eq1} = \frac{C_1 C_2}{C_1 + C_2}$$

At the instant  $t_7$ , the voltages across  $C_c$ ,  $C_1$  and  $C_2$  are clamped at the values of:

$$V_{Cc(07)} = \frac{1}{C_c} \int_{t_6}^{t_7} I_{Cc(t)} dt + V_{Cc(06)} = |V_{Cc(01)}| \quad (4.40)$$



$$V_{C1(07)} = \frac{-1}{C_1} \int_{t_6}^{t_7} I_{Cc(t)} dt + V_{C1(06)} = V_s - V_{Cc(07)} \quad (4.41)$$

$$V_{C2(07)} = \frac{1}{C_2} \int_{t_6}^{t_7} I_{Cc(t)} dt + V_{C2(06)} = V_{Cc(07)} \quad (4.42)$$

In order to determine the voltages and the currents through the converter topology, in all modes of operation the initial values  $V_{Cc(01)}$  and  $I_{l(min)}$  have to be calculated. These two initial values will be calculated as follows:

- $V_{Cc(01)}$  calculation: In order to facilitate the calculation of  $V_{Cc(01)}$ , the load current  $I_l$ , in the time interval of  $t_1$  to  $t_6$  can be considered constant and is given by:

$$I_l = \frac{V_s D_{s0}}{R_l} \quad (4.43)$$

where  $D_{s0}$  is the duty cycle of the dc bus switch  $S_0$ . The voltages across  $C_c$  through all modes of operation will be:

$$V_{Cc(02)} = \frac{1}{C_c} I_l \frac{\pi}{\omega_s} + V_{Cc(01)} \quad (4.44)$$

$$V_{Cc(03)} = \frac{1}{C_c} I_l F_{s0} D_{s0} + V_{Cc(01)} \quad (4.45)$$

where  $F_{s0}$  is the switching frequency of the dc bus switch  $S_0$ .

$$V_{Cc(04)} = \frac{1}{C_c} I_l (t_4 - t_3) + V_{Cc(03)} \quad (4.46)$$

$$= \frac{I_l}{C_c} \left[ \frac{C_1}{I_l} \left( \frac{C_1}{C_2} (V_s + V_{Cc(01)}) - V_{Cc(01)} \right) \right] + V_{Cc(03)}$$

$$V_{Cc(05)} = \frac{I_1}{C_c} \frac{\pi}{\omega_2} + V_{Cc(04)} \quad (4.47)$$

$$V_{Cc(06)} = \frac{I_1}{C_c} \frac{\pi}{180 \omega_c} \operatorname{tg}^{-1} \left( \frac{I_1 \omega_c L_c}{V_{Cc(05)}} \right) + V_{Cc(05)} \quad (4.48)$$

$$V_{Cc(07)} = \frac{1}{C_c} \frac{\pi}{\omega_3} \frac{V_{Cc(05)} - V_{Cc(06)}}{\sqrt{2} \omega_3 (L_c + L_s)} + V_{Cc(06)} \quad (4.49)$$

$$= - V_{Cc(01)}$$

The capacitor  $C_c$  initial voltage  $V_{Cc(01)}$  and all the other voltages across  $C_c$ , through all modes of operation can be determined from (4.44) to (4.49).

- $I_{l(\min)}$  calculation: The minimum load current  $I_{l(\min)}$  can be calculated from:

$$I_{l(\min)} = I_l - \frac{1}{2} \Delta I_l \quad (4.50)$$

where  $I_l$  has been given in (4.43).  $\Delta I_l$  is the ripple of the load current and is given by:

$$\Delta I_l = \frac{V_{Lf}}{L_f} \Delta t \quad (4.51)$$

where  $\Delta t$  is the on-time of the dc bus switch  $S_0$  and is given by:

$$\Delta t = \frac{D_{S0}}{F_{S0}} \quad (4.52)$$

and  $V_{Lf}$  is the voltage drop on the output filter  $L_f$  during the on-time of the dc bus switch, and is given by:

$$V_{Lf} = V_s - V_{Rl} = V_s - D_{S0} V_s = (1 - D_{S0}) V_s \quad (4.53)$$

where  $V_{Rl}$  is the voltage drop on the load  $R_l$  during the on-time of the dc bus switch. Using (4.50) to (4.53),  $I_{l(\min)}$  will be:

$$I_{l(min)} = \frac{V_s D_{so}}{R_l} - \frac{D_{so} (1 - D_{so}) V_s}{2 L_f F_{so}} \quad (4.54)$$

#### 4.4 Design Guidelines

In this section, guidelines for selecting the converter component values will be provided. In particular, the components of the dc bus commutating subcircuit  $C_1$ ,  $C_2$  and  $L_s$  will be designed to yield zero-voltage inverter switching condition. While the components of the load current commutating subcircuit,  $C_c$  and  $L_c$  will be designed to yield zero-current inverter switching condition.

The output power  $P_{out}$ , the input voltage  $V_s$  and the inverter switching frequency  $F_{inv}$  are the key converter design parameters. In addition, the switching frequency of the dc bus switch should be equal to twice the operating frequency of the inverter switches. This condition should be satisfied since the dc bus switch should be on during most of the positive and the negative half cycles of the inverter output.

-The design of the output filter  $L_f$ :  $L_f$  is chosen according to the acceptable ripple current  $\Delta I_l$ .  $L_f$  can be calculated from Equations (4.51) to (4.53):

$$L_f = \frac{(1-D_{so}) D_{so} V_s}{\Delta I_l F_{so}} \quad (4.55)$$

The load current  $I_l$  can be considered constant by selecting  $L_f$  large enough. This condition simplifies the analysis and the design procedures.

-The design of the load current commutating subcircuit,  $C_c$  and  $L_c$ : The capacitor  $C_c$  value should be selected as large as possible. A large  $C_c$  value decreases the voltage drop  $V_{cc}$  across  $C_c$  Equation (4.56), during  $S_o$  turn-on time.

$$V_{Cc} = \frac{1}{C_c} I_l t_3 = \frac{1}{C_c} \frac{D_{so} V_{so}}{R_l} \frac{D_{so}}{F_{so}} \quad (4.56)$$

A small value of  $V_{Cc}$  is necessary to achieve zero turn-off loss through the dc bus switch  $S_o$ . For example;  $V_{Cc} = (10 \rightarrow 20) \% V_s$  forces  $C_1$  to charge to  $V_s - \frac{V_{Cc}}{2} = V_s - (5 \rightarrow 10) \% V_s$  and  $C_2$  to discharge to  $\frac{V_{Cc}}{2} = (5 \rightarrow 10) \% V_s$  resulting in nearly zero turn-off loss through the dc bus switch  $S_o$ .

The inductor  $L_c$  value is selected to produce smooth current rise through the inverter switches. The switch  $dI/dt$  is given by:

$$\frac{dI}{dt} = \frac{V_{Cc(05)}}{L_c} \quad (4.57)$$

If  $dI/dt$  is chosen in the range  $20 \rightarrow 30$  (A/ $\mu$ s), the turn-on losses are nearly zero. An additional variable in choosing the  $L_c$  and  $C_c$  values is the time interval  $(t_6 - t_5)$ , in Figs. 4.9 and 4.10, during which the current in the inverter circuit decreases from its maximum value to zero according to Equation (4.34).

-The design of the dc bus commutating subcircuit  $C_1$ ,  $C_2$  and  $L_s$ : The capacitor  $C_1$  is designed to provide a smooth turn-off process through the dc bus switch. A  $dv/dt = 150 \rightarrow 300$  (v/ $\mu$ s) results in nearly zero turn-off loss. Since the capacitor  $C_2$  returns the energy from  $C_1$  to the load through the commutating circuit, its value should be at least equal to that of  $C_1$  or larger. The values of  $C_1$  and  $C_2$  can be selected from Equations (4.29) and (4.30) by using the following expressions:

$$C_1 + C_2 = \frac{I_l(\max) (t_5 - t_4)}{V_{C1(05)} - V_{C1(04)}} \quad (4.58)$$

$$C_1 + C_2 = \left| \frac{- I_l(\max) (t_5 - t_4)}{V_{C2(05)} - V_{C2(04)}} \right| \quad (4.59)$$

taking into consideration that:  $t_5 - t_4 < \frac{D_{so}}{F_{so}}$ .

The inductor  $L_s$  is designed to limit the slope of the current  $I_{sn}$ . A  $dI_{sn}/dt$  between 20-30 (A/ $\mu$ s) satisfies the requirement of nearly zero turn-on loss through the dc bus switch  $S_o$ . The inductor  $L_s$  can be selected from:

$$L_s = \frac{V_s + 2 V_{C_c(01)}}{\sqrt{2} \frac{dI_{sn}}{dt}} \quad (4.60)$$

It is also noted that the dc bus switch  $S_o$  and each diagonal pair of the inverter switches are turned on simultaneously. Moreover, each pair of inverter switches should be turned off after the dc bus switch  $S_o$ . The delay time should be at least equal ( $t_6 - t_3$ ), as illustrated in Fig. 4.9. This time is necessary to allow the capacitor  $C_1$  to charge to  $V_s - V_{C_c(05)}$ ,  $C_2$  to discharge to  $V_{C_c(05)}$  and the inverter current in the capacitor  $C_c$  to fall to zero. As a result, the maximum duty cycle of the dc bus switch  $S_o$  that can be achieved is given by:

$$D_{S0(max)} = 1 - F_{S0} (t_6 - t_3) \quad (4.61)$$

#### 4.5 Design Example

The design example presented in this section will use the equations in section 4.4. It will provide guidelines for determining the component values of the dc bus commutating subcircuit, the load current commutating subcircuit and the output filter for the converter shown in Fig. 4.1. The design is performed with the following assumptions:

output power	$P_o = 5$ (kW)
input voltage	$V_s = 250$ (V)
inverter switching frequency	$F_{Inv} = 20$ (KHz)
dc bus switching frequency	$F_{S0} = 40$ (KHz)
dc bus switch duty cycle	$D_{S0} = 0.75$

ripple output current	$\Delta I_1 = 4.5 \% I_1$
The maximum $C_c$ voltage	$V_{Cc} = 10 \% V_s$
current-increase rate through $L_c$	$dI_1/dt = 25 \text{ (A/}\mu\text{s)}$
current-increase rate through $L_s$	$dI_{sn}/dt = 29.4 \text{ (A/}\mu\text{s)}$
charging rate of $C_1$	$dv/dt = 89 \text{ (V/}\mu\text{s)}$

The equations given in section 4.5 and the above assumptions were used to calculate the converter component values. The results are given below:

output filter	$L_r = 0.001 \text{ (H)}$
current commutating capacitor	$C_c = 5 \text{ (}\mu\text{F)}$
current commutating inductor	$L_c = 2 \text{ (}\mu\text{H)}$
dc bus commutating capacitor	$C_1 = 0.1 \text{ (}\mu\text{F)}$
dc bus commutating capacitor	$C_2 = 0.2 \text{ (}\mu\text{F)}$
dc bus commutating inductor	$L_s = 6.8 \text{ (}\mu\text{H)}$

#### 4.6 Simulation Results

In this section, the converter parameters and the component values obtained in the previous section, have been used and tested at different duty cycles. Spice package described in reference [18] was used to simulate the performance of the examined dc-dc topology shown in Fig. 4.1 and to prove the results predicted thus far in this chapter. Figs. 4.9 (a) to 4.9 (e) show the simulation results. The modes of operation obtained are as theoretically predicted especially the nearly zero losses switching behavior of the dc bus switch and of the inverter switches.

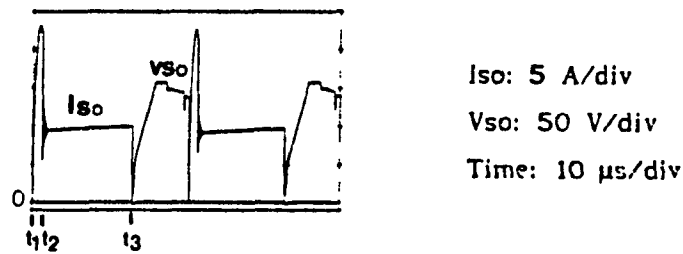


Fig. 4.9 (a) The Current and the Voltage Across Switch  $S_0$ , Topology Fig. 4.1

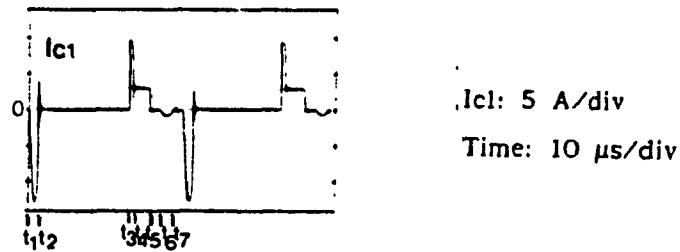


Fig. 4.9 (b) The Current Through the Dc Bus Capacitor  $C_1$ , Topology Fig. 4.1

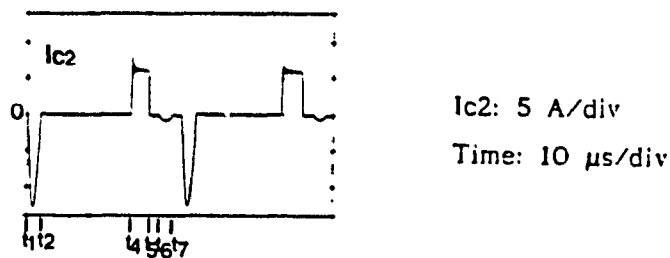


Fig. 4.9 (c) The Current Through the Dc Bus Capacitor  $C_2$ , Topology Fig. 4.1

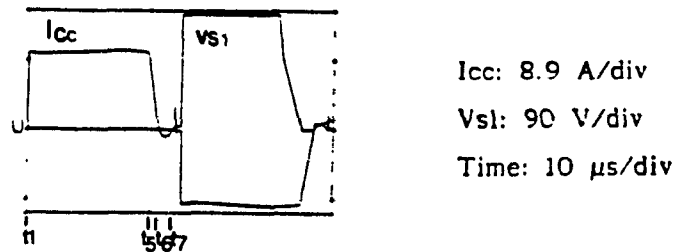


Fig. 5.9 (d) The Current and the Voltage Through  $S_{1,4}$ , Topology Fig. 4.1

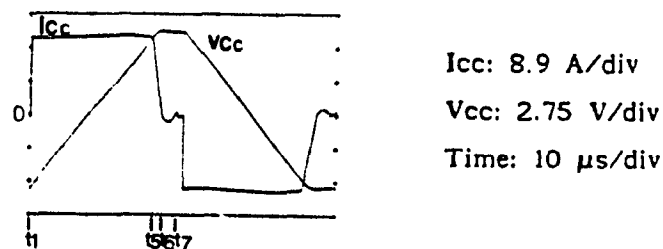
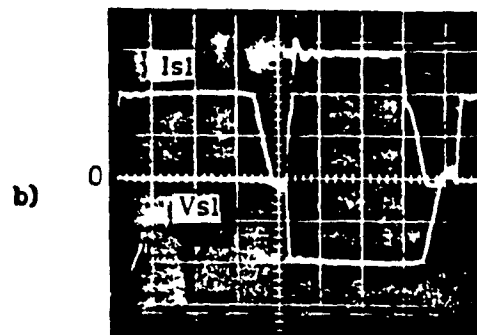
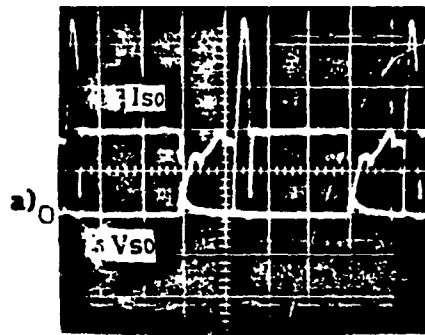


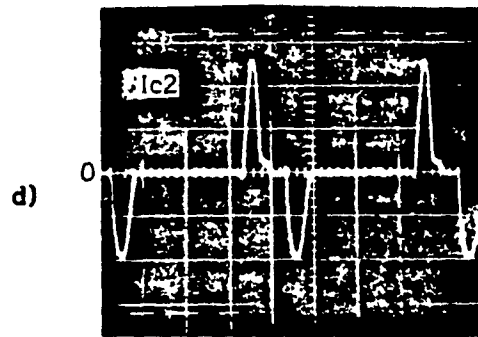
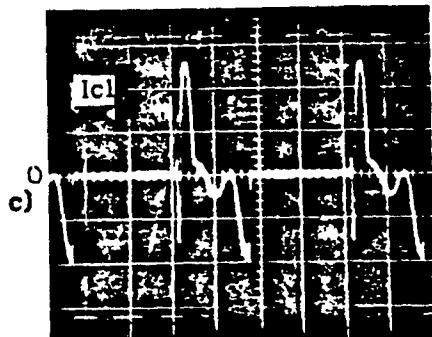
Fig. 4.9 (e) The Current and the Voltage Through  $C_c$ , Topology Fig. 4.1



$V_{s0}=V_{s1}=50$  (V/div),  $I_{s0}=I_{s1}=5$  (A/div), Time= 6.25 ( $\mu$ s/div)

Fig. 4.10 (a) The Current and the Voltage Through  $S_0$ , Topology Fig. 4.1

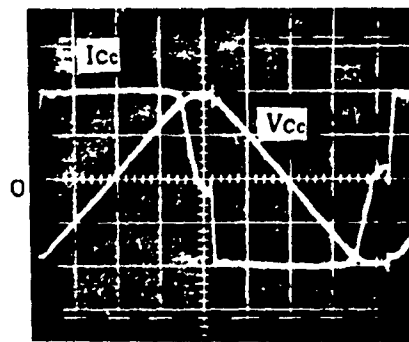
Fig. 4.10 (b) The Current and the Voltage Through  $S_{1,4}$ , Topology Fig. 4.1



$I_{c1}=I_{c2}=5$  (A/div), time=6.25 ( $\mu$ s/div)

Fig. 4.10 (c) The Current Through the Capacitor  $C_1$ , Topology Fig. 4.1

Fig. 4.10 (d) The Current Through the Capacitor  $C_2$ , Topology Fig. 4.1



$V_{cc}=3.25$  (V/ $\mu$ s),  $I_{cc}=5$  (A/div), time=6.25 ( $\mu$ s/div)

Fig. 4.10 (e) The Current and the Voltage Through  $C_c$ , Topology Fig. 4.1



#### 4.7 Experimental Results

This section is provided to establish the feasibility of the discussed full-bridge PWM dc-dc converter Fig. 4.1 and to verify the theoretical and simulation results. The same converter parameters and component values obtained in section 4.5 have been used. A 1 kw laboratory unit operating at 20 kHz switching frequency was built and tested successfully.

Key experimental results corresponding to the predicted and simulated ones are shown in Figs. 4.10 (a), (b), (c), (d), and (e). Particularly, Fig. 4.10 (a) shows that as predicted, the actual switching losses for the dc bus switch  $S_0$  are zero. The same conclusion applies to Fig. 4.10 (b), which shows the respective switching losses for one of the inverter switches (e.g.  $S_1$ ).

#### 4.8 Conclusions

A detailed analysis and design procedure for the full-bridge PWM dc-dc converter, shown in Fig. 4.1 has been provided in this chapter. The effective use of the proposed dc bus commutating subcircuit topology No. (2) and the load current commutating subcircuit consisting of L and C elements has yielded zero-voltage zero-current switching conditions. Theoretical results have been verified experimentally on a 1 kw 20 kHz laboratory prototype.

Thus, the resulting full-bridge topology Fig 4.1 can be used to convert medium power at high switching frequencies with minimum switching losses. However, it has been found that the circuit complexity of the dc bus commutating subcircuit topology No. (2) implemented in the converter shown in Fig. 4.1, is relatively high. Therefore, the dc bus commutating subcircuit topology No. (1) implemented in chapter 3, will be applied for three-phase topology and will be treated in the following chapter.

## CHAPTER 5

### ANALYSIS AND DESIGN OF A FULL-BRIDGE 3-PHASE DC BUS COMMUTATED PWM VOLTAGE SOURCE INVERTER

In this chapter, the implementation of the proposed dc bus commutating subcircuit topology No. (1) shown in Fig. 2.13, for three-phase full-bridge PWM VSI is treated in detail. In particular, the following sections are devoted to explore the operation and performance of the resulting dc bus commutated PWM VSI topology, shown in Fig. 3.1.

In section 5.1, an introduction of the advantages obtained by the implementation of the proposed commutating subcircuit is provided.

In section 5.2, a PWM scheme utilized for the proposed inverter topology is described.

In section 5.3, a complete identification of all modes of operation with emphasis on the switching behavior of the dc bus switch and the inverter switches are presented.

In section 5.4, a complete mathematical analysis of all modes of operation is obtained.

In section 5.5, design guidelines to select the topology component values are provided.

In section 5.6, a design example using the equations obtained in the section 5.5 is presented.

In section 5.7, simulation results of the key currents and voltages are obtained. In particular, the switching behavior of the dc bus switch and the inverter switches is shown.

In section 5.8, conclusions are drawn pertaining to the subject matter discussed in this chapter.

### 5.1 Introduction

The purpose of this chapter is to present a new and simple method of realizing zero-voltage switching (ZVS) PWM three-Phase VSI. The proposed topology, shown in Fig. 5.1, applies the principle of zero-voltage dc bus commutation to achieve soft switching condition. This condition is achieved by the dc bus commutating subcircuit topology No. (1) Fig. 2.13, which consists of an interrupt dc bus auxiliary switch  $S_0$  and a dc bus parallel capacitor  $C_0$ . Moreover, the proposed subcircuit when implemented for three-phase PWM VSI has the following direct advantages:

- i) It does not affect the operating conditions which are dictated by the pwm used. Therefore, minimum switch stresses and low switching losses are achieved while the advantages of the pwm scheme are maintained.
- ii) The power and control circuits are very simple, and
- iii) The commutation circuit can be used to isolate the inverter under adverse system operating conditions.

The proposed topology of zero-voltage dc bus commutated PWM three-phase VSI shown in Figure 5.1, consists of the following sections:

- 1) The dc bus commutation subcircuit includes the dc supply voltage  $V_{in}$ , the auxiliary switch  $S_0$  with the antiparallel diode  $D_0$  and the dc bus parallel capacitor  $C_0$ .
- 2) The inverter three phase circuit consisting of the six main inverter switches ( $S_1 \rightarrow S_6$ ) with the antiparallel diodes ( $D_1 \rightarrow D_6$ ).
- 3) The load circuit including the three-phase symmetrical inductive load represented by  $R_L$  and  $L_L$ .

It is finally noted that proper operation of the inverter shown in Fig. 5.1 requires that the load has some finite line inductance and that all six

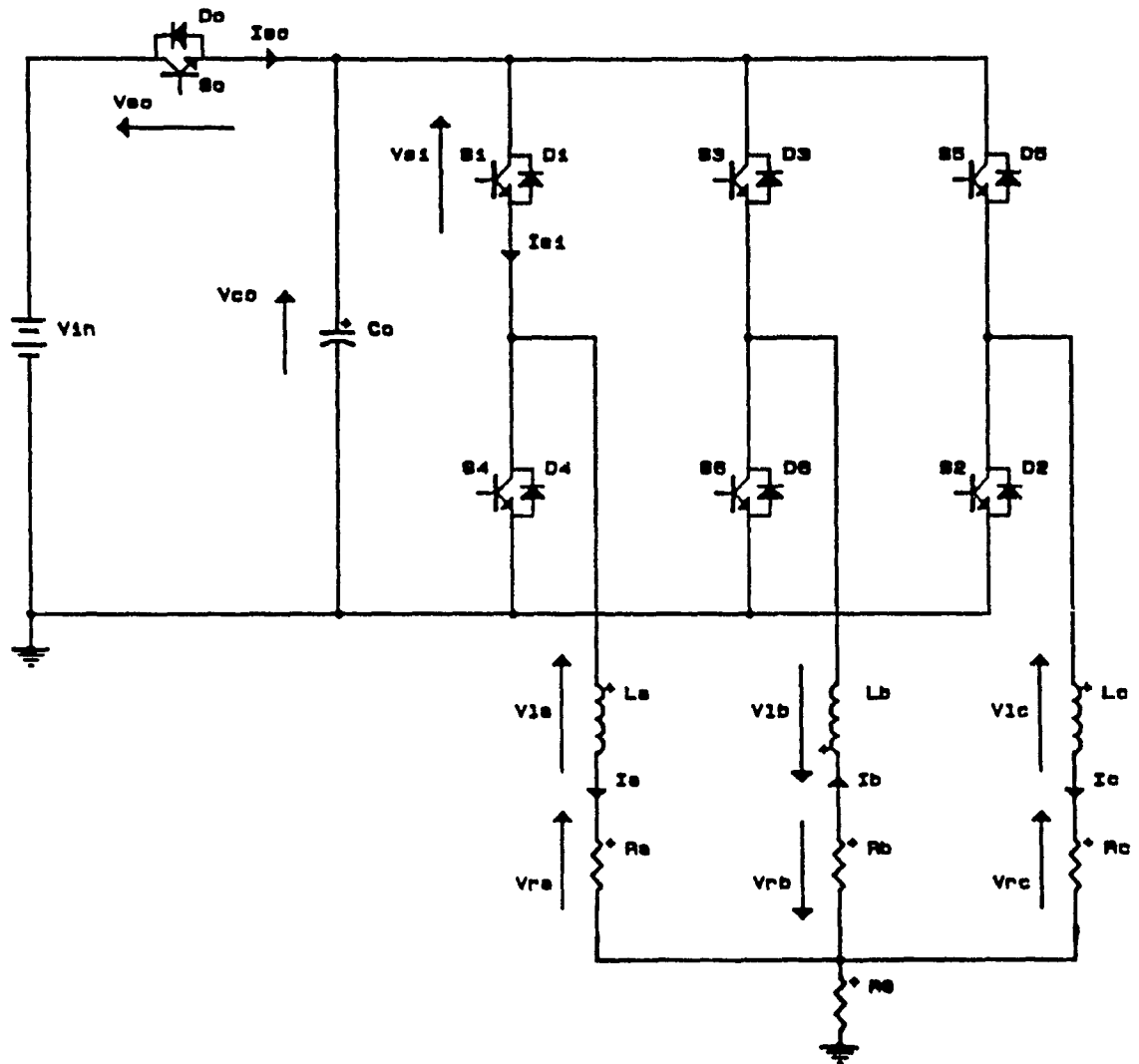


Fig. 5.1 A ZVS Dc Bus Commutated High-Frequency High-Power PWM VSI

inverter switches commutate at the same time (in order to charge up  $C_o$ ). This last requirement can be easily met by selecting the carrier ramp waveform (of the modulation scheme) as shown in Fig. 5.2 (a). For this reason the inverter PWM scheme is described next in greater detail.

### 5.2 Description of the PWM Scheme

The third harmonic injection SPWM technique proposed in reference [17] Fig. 5.2 (a), with modulation index near 1 has been applied in the proposed topology. The inverter pole switching functions for each phase of the inverter are shown in Figs. 5. 2 (b), (c), and (d) respectively. They are generated by comparing the reference voltages  $V_{ra}$ ,  $V_{rb}$  and  $V_{rc}$ , with common ramp carriers  $V_{ca}$ ,  $V_{cb}$  and  $V_{cc}$ . The gating signal for the dc bus interrupt switch  $S_o$  is depicted in Fig. 5.2 (e). This Figure demonstrates that the beginning of the turn-off intervals of the dc bus switch  $S_o$  are defined by the vertical edges of the ramp carrier waveforms.

In other words, immediately before the three phase inverter switches commutate simultaneously the dc bus switch turns off first. Consequently, the capacitor  $C_o$  discharges to zero volts setting up the required zero-voltage turn-off condition for the inverter switches. When all six inverter switches are off, the load currents (aided by the line inductances) momentarily return to the dc bus thus charging  $C_o$  up to dc bus voltage  $V_{in}$ .

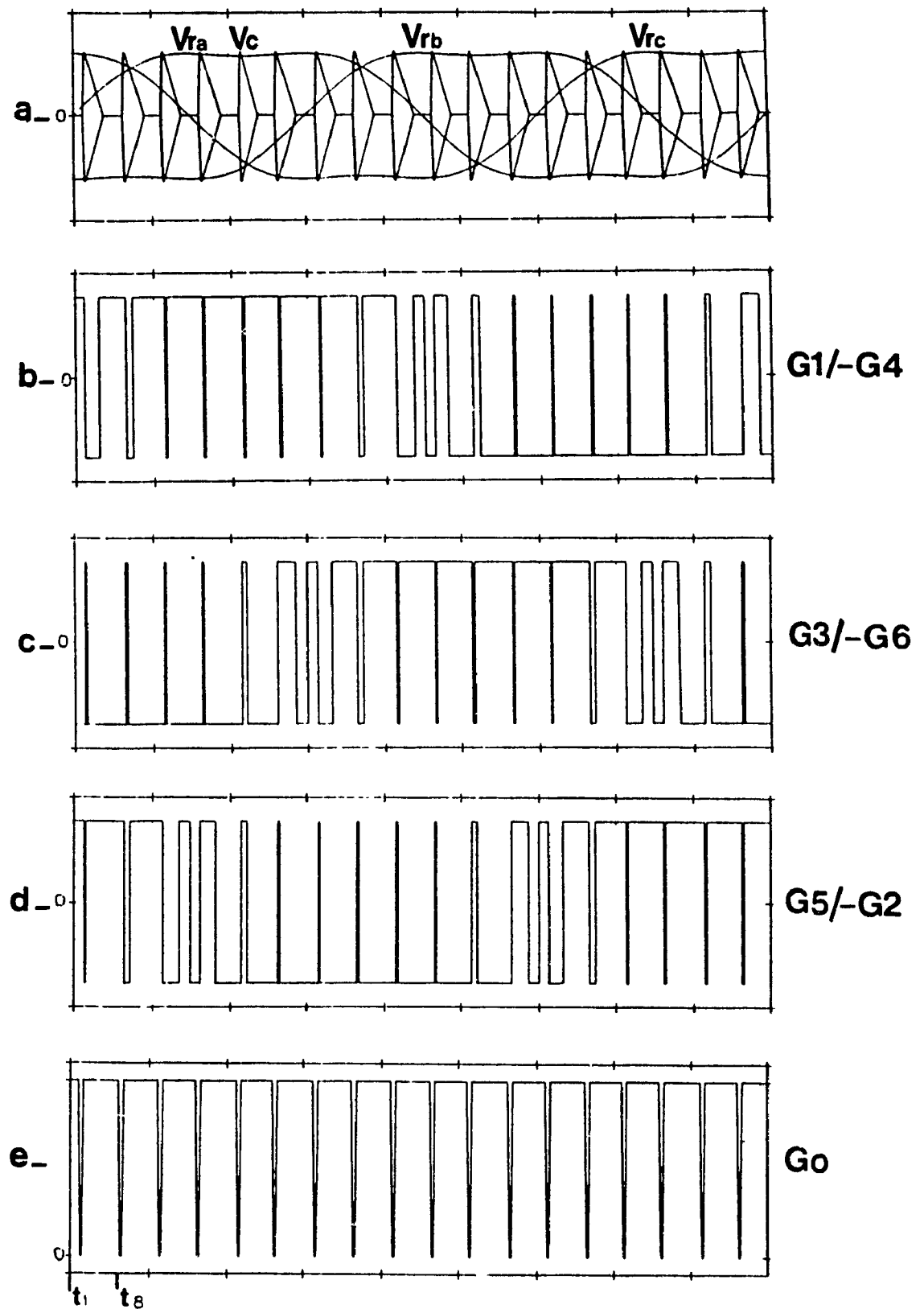


Fig. 5.2 PWM Schemes and the Respective Switching Functions, Topology Fig. 5.1

### 5.3 Principles of Operation

In this section, the performance of the proposed dc bus commutation circuit is described. The ZVS environment for the inverter switches ( $S_1 \rightarrow S_6$ ), and for the dc bus interrupt switch  $S_0$  is explained. All modes of operation of the proposed topology are defined. The three phase PWM inverter presented here operates in a similar manner during each switching period. To facilitate the description of modes of operation, Figs. 5.3 and 5.4 are shown. They demonstrate for a random switching period the switching times, voltages, and currents through the inverter switches. For each switching period, the topology has seven modes of operation with corresponding time intervals. These modes a, b, c, d, e, f and g will be defined and explained in detail aided by Figs. 5.3 and 5.4.

Mode (a): Initially, at  $t_1=0$  in Figs. 5.3 and 5.4, the switches  $S_1$ ,  $S_5$  and  $S_6$  are on and the switches  $S_3$ ,  $S_2$  and  $S_4$  are off. The voltage across the capacitor  $C_0$  is equal to the dc supply voltage  $V_{in}$ . The load current  $I_a$  passes through the switch  $S_1$ .  $I_c$  flows through  $S_5$ .  $I_b$ , which is equal to the sum of  $I_a$  and  $I_c$ , goes through  $S_6$  and  $S_0$ . These currents increase linearly until  $t_2$ .

Mode (b): At  $t_2$  in Figs. 5.3 and 5.4, the switch  $S_0$  is turned off at zero voltage condition since  $V_c(t_2)=V_{in}$ . The capacitor  $C_0$  begins discharging toward zero by sourcing the current  $I_{s0}$ , while the switches  $S_1$ ,  $S_5$  and  $S_6$  are kept on and the switches  $S_4$ ,  $S_2$  and  $S_3$  are kept off until  $t_3$ .

Mode (c): At  $t_3$  in Figs. 5.3 and 5.4, the capacitor  $C_0$  is completely discharged and the dc bus voltage is equal to zero, hence a freewheeling period exists. The load is shortcircuited by the switches  $S_1$ ,  $S_5$  and  $S_6$  and by the switches  $S_2$ ,  $S_4$ , and  $S_3$  antiparallel diodes  $D_2$ ,  $D_4$  and  $D_3$ .  $S_1$  and  $D_4$  share the load phase current  $I_a$ , while  $S_5$  and  $D_2$  share the current  $I_c$  and  $S_6$  and  $D_3$

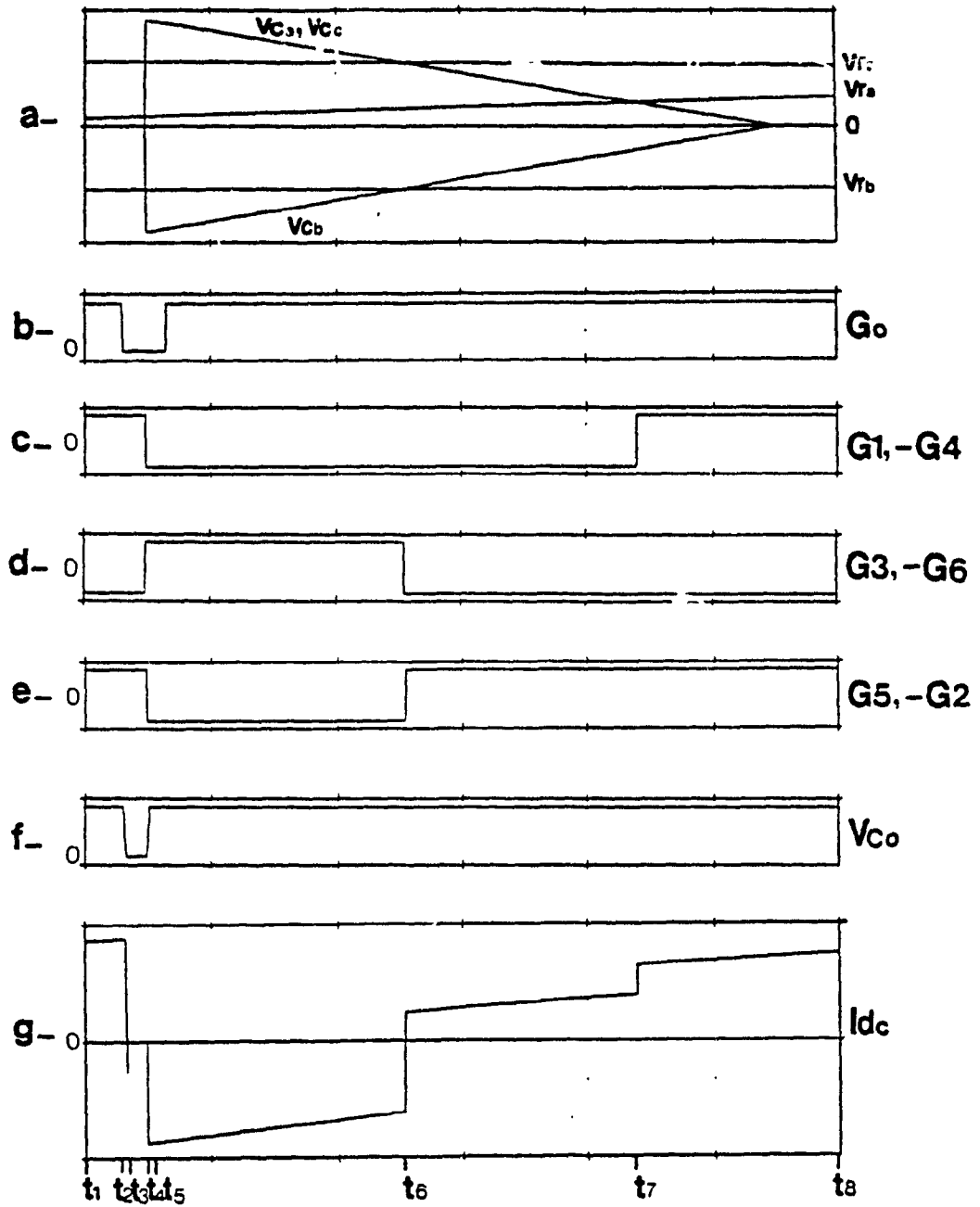


Fig. 5.3 The Switching Times during a Switching Period Topology, Fig. 5.1

- a) Shows the used PWM scheme.
- b) Depicts the gating signal for the dc bus switch  $S_o$ .
- c), (d), and (e) Illustrate the inverter switching functions.
- f) Depicts the dc bus voltage  $V_{Co}$ .
- g) Shows the dc bus current  $I_{dc}$ .



share the current  $I_b$ , which is equal to  $I_a + I_c$ . At any moment of this time interval the switches  $S_1$ ,  $S_5$  and  $S_6$  can be turned off and be commutated by  $S_3$ ,  $S_4$  and  $S_2$  at zero voltage condition, resulting in zero turn-off and turn-on losses.

Mode (d): At  $t_4$  in Figs. 5.3 and 5.4, the switches  $S_1$ ,  $S_5$  and  $S_6$  are turned off and  $S_4$ ,  $S_2$  and  $S_3$  are turned on at zero voltage condition. Since the three phase load is inductive, the load phase currents do not change their directions in the load circuit at this stage. Therefore,  $I_a$  passes through  $S_4$  antiparallel diode  $D_4$  and  $I_c$  flows through  $S_2$  antiparallel diode  $D_2$ . The current  $I_b$  which is still equal to  $I_a + I_b$ , passes through  $S_3$  antiparallel diode  $D_3$  and immediately goes back to the dc bus and begins recharging the capacitor  $C_o$ .

Mode (e): At  $t_5$  in Figs. 5.3 and 5.4, the capacitor  $C_o$  voltage reaches the dc supply voltage  $V_{in}$ . At this moment, the dc bus switch  $S_o$  can be turned on at zero voltage, yielding a zero turn-on loss. At the same moment, the current  $I_b$  continues passing through the dc bus in the negative direction through the switch  $S_o$  antiparallel diode  $D_o$ , to the dc supply voltage source until  $t=t_6$ .

Mode (f): At  $t_6$  in Figs. 5.3 and 5.4, the switches  $S_3$  and  $S_2$  are turned off and  $S_6$  and  $S_5$  are turned on, whereas switch  $S_1$  is kept off and  $S_4$  is kept on. This commutation is lossless since it takes place at zero voltage condition. This condition exists, because the commutated currents  $I_b$  and  $I_c$  were in negative direction passing through  $S_3$  and  $S_2$  antiparallel diodes  $D_3$  and  $D_2$ . At the moment of this commutation,  $I_a$  still passes through  $S_4$  antiparallel diode  $D_4$  and  $I_b$  flows through the switch  $S_6$ . The current  $I_c$  which is now equal to the dc bus switch current  $I_{s_o}$ , passes through the switch  $S_5$ .

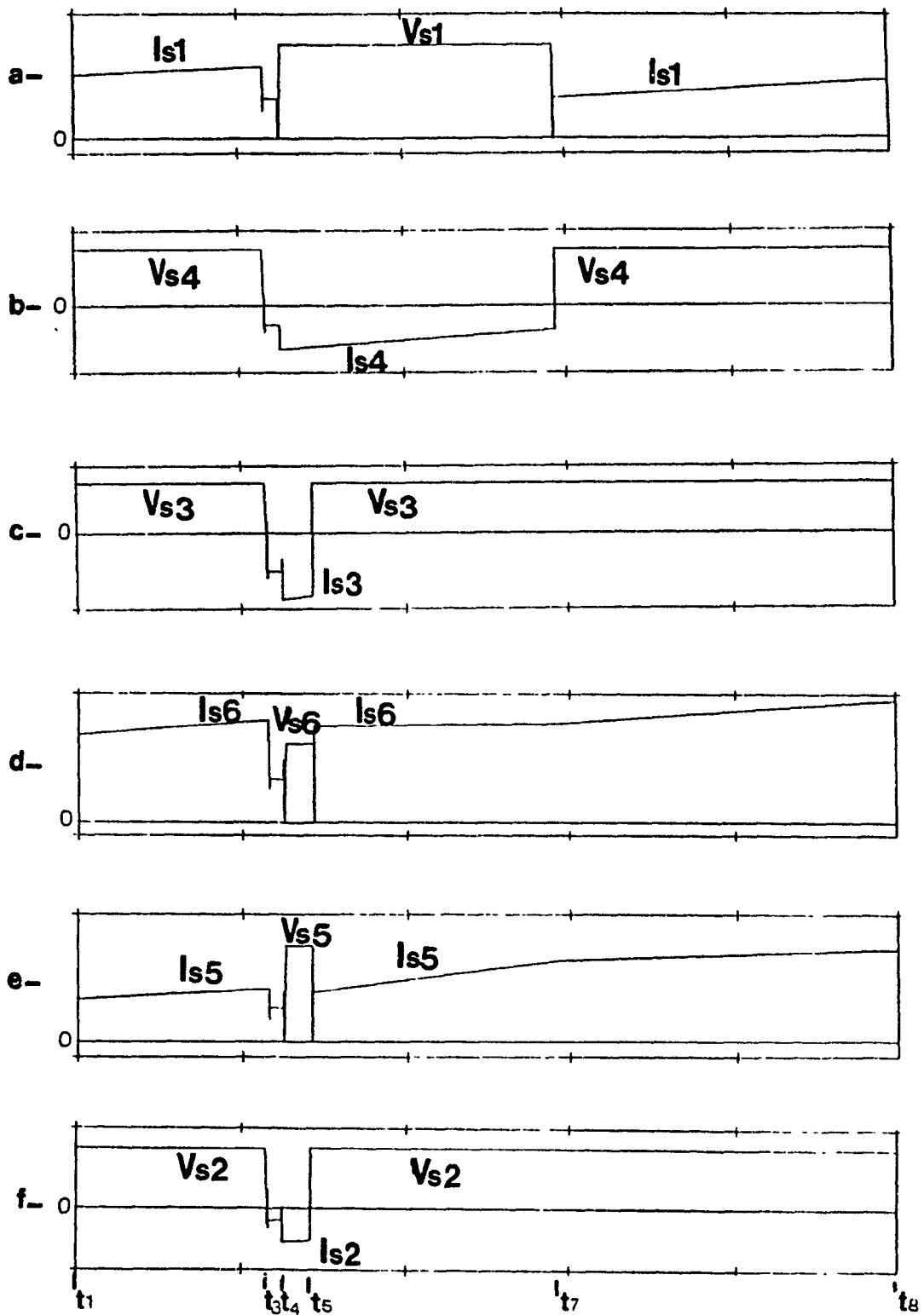


Fig. 5.4 Switch Currents and Voltages in a Switching Period Topology, Fig. 5.1

Mode (g): At  $t_7$  in Figs. 5.3 and 5.4, the switches  $S_5$  and  $S_6$  are kept on and  $S_2$  and  $S_3$  are kept off, while the switch  $S_4$  is turned off and switch  $S_1$  is turned on. Again, this commutation is lossless because the commutated current  $I_a$  was passing through  $S_4$  antiparallel diode  $D_4$ , creating zero voltage turn-off condition. At the moment of this commutation,  $I_a$  passes through the switch  $S_1$ ,  $I_b$  and  $I_c$  still flow through the switches  $S_6$  and  $S_5$  respectively. By now, all modes of operation through one switching period have been defined. The other switching periods can be defined and analyzed in a similar manner.

#### 5.4 Circuit Analysis

Here, the analytical expressions describing all modes of operation of the examined inverter topology Fig. 5.1 are presented. Expressions for the currents and the voltages during all subsequent modes of operation are obtained by assuming the following:

- i) All the circuit components are ideal.
- ii) The supply voltage  $V_{in}$  is a stiff dc type, and
- iii) The three-phase load is balanced.

Mode (a): At  $t_1$  in Figs. 5.3 and 5.4, the current through the dc bus switch  $S_0$  and through  $S_6$  as a function of time is given by:

$$I_{S0}(t) = I_{dc}(t) = I_{S6}(t) = \frac{V_{in}}{r} (1 - e^{-\frac{r}{l} t}) \quad (5.1)$$

where,

$$r = \frac{3}{2} R_l \quad \text{and} \quad l = \frac{3}{2} L_l$$

and the currents through  $S_1$  and  $S_5$  are:

$$I_{S1}(t) = I_{S5}(t) = \frac{1}{2} I_{S0}(t) = I_{R1a}(t) = I_{R1c}(t) \quad (5.2)$$

The resistive phase (A) or (C) voltage can be obtained from:

$$V_{R(a,c)}(t) = \frac{1}{3} V_{in} (1 - e^{-\frac{r}{L} t}) \quad (5.3)$$

and the inductive phase (A) or (C) voltage is given by:

$$V_{L(a,c)}(t) = \frac{1}{3} V_{in} e^{-\frac{r}{L} t} \quad (5.4)$$

While the resistive phase (B) voltage can be calculated from:

$$V_{Rb}(t) = \frac{2}{3} V_{in} (1 - e^{-\frac{r}{L} t}) \quad (5.5)$$

and the inductive phase (B) voltage is obtained from:

$$V_{Lb}(t) = \frac{2}{3} V_{in} e^{-\frac{r}{L} t} \quad (5.6)$$

Mode (b): At  $t_2$  in Figs. 5.3 and 5.4, the dc bus switch  $S_0$  is turned off and the capacitor  $C_0$  begins sourcing the Current  $I_{S0}$ . In this mode the current  $I_{S0}$  can be considered constant. The voltage across  $C_0$  as a function of time is given by:

$$V_{Co}(t) = - \frac{I_{S0}(t) \big|_{t_2} t}{C_0} + V_{Co(2)} \quad (5.7)$$

where,

$$V_{Co(2)} = V_{Co(1)} = V_{in}$$

This mode ends at time  $t_3$  when the capacitor  $C_0$  is completely discharged to zero. The time  $t_3$  can be calculated from:

$$t_3 = \frac{C_o}{I_{s_o}|_{t_2}} V_{in} + t_2$$

where  $t_2$  is the turn-off moment of the switch  $S_o$ .

Mode (c): At  $t_3$  in Figs. 5.3 and 5.4, the dc bus voltage equals zero and a freewheeling period exists. The currents through the inverter circuit are given by:

$$I_{s1}(t) = I_{d4}(t) = \frac{1}{2} I_a(t_3) \quad (5.9)$$

$$I_{s5}(t) = I_{d2}(t) = \frac{1}{2} I_c(t_3) \quad (5.10)$$

$$I_{s6}(t) = I_{d3}(t) = \frac{1}{2} I_b(t_3) = \frac{1}{2} (I_a(t_3) + I_c(t_3)) \quad (5.11)$$

Mode (d): At  $t_4$  in Figs. 5.3 and 5.4, the switches  $S_1$ ,  $S_5$  and  $S_6$  are turned off and the switches  $S_4$ ,  $S_2$  and  $S_3$  are turned on at zero-voltage condition. The currents through the inverter circuit are given by:

$$I_{s1} = 0 \quad \text{and} \quad I_{d4} = I_a \quad (5.12)$$

$$I_{s5} = 0 \quad \text{and} \quad I_{d5} = I_c \quad (5.13)$$

$$I_{s6} = 0 \quad \text{and} \quad I_{dc} = I_{d3} = I_b = I_a + I_c \quad (5.14)$$

At  $t_4$ , immediately  $I_b|_{t_3}$  given by Equation (5.11) begins recharging the dc bus capacitor  $C_o$ . In this mode, the currents  $I_a$ ,  $I_b$ , and  $I_c$  can be considered constant. The voltage across  $C_o$ , as a function of time, is given by:

$$V_{co} = \frac{I_b|_{t_3}}{C_o} t \quad (5.15)$$

This mode ends at  $t_5$ , when the capacitor  $C_o$  is charged to the input dc voltage

value  $V_{in}$ . The time  $t_5$  can be calculated from:

$$t_5 = \frac{C_o}{I_b|_{t_3}} V_{in} + t_4 \quad (5.16)$$

where  $t_4$  is the time when all the inverter switches are commutating.

Mode (e): At  $t_5$  in Figs. 5.3 and 5.4, the current  $I_b$  passes through  $S_o$  antiparallel diode  $D_o$  to the dc supply voltage  $V_{in}$ , whereas:

$$I_a(t) = I_{d4}(t) \quad (5.17)$$

$$I_c(t) = I_{d2}(t) \quad (5.18)$$

where,

$$I_b(t) = I_a(t) + I_c(t) = I_{d3}(t) = I_{dc}(t) \quad (5.19)$$

Mode (f): At  $t_6$  in Figs. 3.5 and 4.5, the switches  $S_3$  and  $S_2$  are turned off and  $S_6$  and  $S_5$  are turned on. The dc bus current  $I_{dc}$  increases toward the positive value of  $I_c$  and is given by:

$$I_{dc}(t) = I_{s5}(t) = I_c(t) \quad (5.20)$$

whereas,

$$I_{d4}(t) = I_a(t) \quad (5.21)$$

and

$$I_{s6}(t) = I_b(t) \quad (5.22)$$

Mode (g): At  $t_7$  in Figs. 3.5 and 4.5, the switches  $S_5$  and  $S_6$  are kept on and  $S_2$  and  $S_3$  are kept off, while the switch  $S_1$  is turned on and  $S_4$  is turned off. The dc bus switch current  $I_{s0}$  increases to the value of  $I_b$  and is given by:

$$I_{s0}(t) = I_{dc}(t) = I_{s6}(t) = I_b(t) = I_a(t) + I_c(t) \quad (5.23)$$

whereas,

$$I_a(t) = I_{s1}(t) \quad (5.24)$$

and,

$$I_c(t) = I_{s5}(t) \quad (5.25)$$

until  $t=t_s$  the end of the switching period.

### 5.5 Design Guidelines

In this section, design guidelines for selecting the circuit component values will be provided. In particular, the  $C_o$  value and the dc bus switch switching frequency will be calculated to yield soft switching condition for the inverter switches as well as for the dc bus switch.

It should be noted that in order to recharge the dc bus capacitor  $C_o$ , a minimum output power should be maintained and the three-phase load must be inductive. Therefore, the modulation scheme applied Fig. 5.2 the output power  $P_o$  and the load power factor  $\cos(\alpha)$  are the key inverter design parameters.

-The determination of the switching frequency  $F_{so}$  of the dc bus switch  $S_o$ : The turn-off times of the switch  $S_o$  are always defined by the vertical edges of the three-phase ramp carrier waveforms Fig. 5.2. Therefore, the switching frequency of the dc bus switch  $F_{so}$  can be given from the following:

$$F_{so} = F_c = 18 F_o \quad (5.26)$$

where  $F_c$  is the carrier wave frequency and  $F_o$  is inverter output frequency. It is obvious from Figs. 3.5 and 3.4, that the duty cycle of the dc bus switch  $S_o$  is near one.  $S_o$  is turned off for a short time in a switching period. This time should be at least equal to the following time intervals:

- 1) Turn-off time of the dc bus switch  $S_o$ .
- 2) Discharging and recharging times of the capacitor  $C_o$ , at minimum applied output power, which will be assumed:  $P_{o(min)} = 20 \% P_o$ , and
- 3) The commutating period of switches  $S_1$ ,  $S_5$ , and  $S_6$ , by the switches  $S_3$ ,  $S_2$ , and  $S_4$ .

-The design of the dc bus parallel capacitor  $C_o$ :  $C_o$  is designed to provide soft turn-off switching conditions for the inverter switches whenever needed and dictated by the modulation scheme. The capacitor  $C_o$  value can be obtained from:

$$C_o = \frac{I_{dc}}{\frac{dv}{dt}} \quad (5.27)$$

The current  $I_{dc}$  (the maximum fundamental component of the line current  $I_L$ ) can be calculated as follows:

$$I_{dc} = I_L = I_b = I_a + I_c = \frac{2 P_{o(min)}}{\sqrt{3} V_L \cos(\alpha)} \quad (5.28)$$

where  $V_L$  is the maximum fundamental component of line-to-line voltage. At modulation index  $M.I. = 1$ ,  $V_L$  is given by:

$$V_L = \sqrt{3} \frac{V_{in}}{2} \quad (5.29)$$

The capacitor  $C_o$  value will be selected according to the output power between the range of  $0.2 P_o$  to  $P_o$ , which results in  $A dv/dt$  in a range values between 100 to 600 V/  $\mu s$ . The resulting range values of  $dv/dt$  yields low switch stresses and zero turn-off losses through the inverter switches.

-The resistive phase load represented by  $R_l$  is given by:

$$R_l = \frac{P_o}{3 I_L^2(rms)} \quad (5.30)$$



-The inductive phase load represented by  $L_1$  is given by:

$$L_1 = \frac{\sqrt{S_o^2 - P_o^2}}{2 \pi F_o (3 I_{L(rms)}^2)} \quad (5.31)$$

where  $S_o$  is the apparent output power and  $F_o$  is the output fundamental frequency.

### 5.6 Design Example

The design example presented in this section will use the equations in the previous section to provide guidelines for component selection. In particular, a switching frequency of the dc bus switch and a value for the dc bus capacitor  $C_o$  will be determined. The design of the three-phase PWM VSI topology shown in Fig 5.1 is performed with the following assumptions:

output power	$P_o = 10 \text{ (Kw)}$
inverter output frequency	$F_o = 55 \text{ (Hz)}$
input dc voltage	$V_{in} = 300 \text{ (V)}$
minimum output load	$P_{o(min)} = 20 \% P_o$
load power factor	$\cos(\alpha) = 0.8 \text{ lagging}$
$C_o$ charging rate	$dv/dt = 111,1 \text{ to } 555.5 \text{ (V/}\mu\text{s)}$

The equations given in section 5.5, and the above assumption have been used to calculate the following values:

dc bus capacitor	$C_o = 0.1 \text{ (}\mu\text{F)}$
dc bus switching frequency	$F_{so} = 990 \text{ (Hz)}$
resistive phase load	$R_1 = 2.16 \text{ (}\Omega\text{)}$
inductive phase load	$L_1 = 2.34 \text{ (mH)}$

### 5.7 Simulation Results

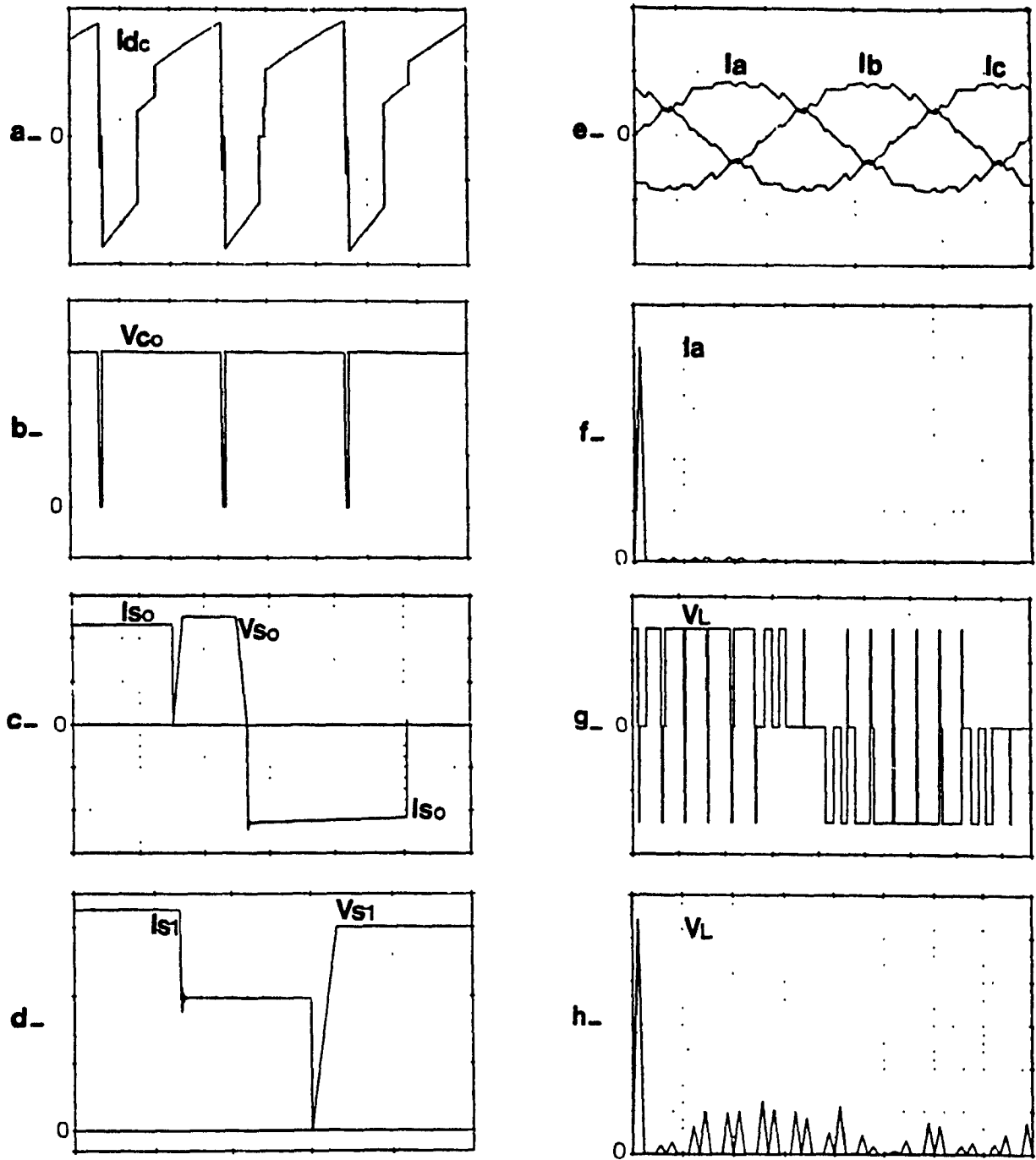


Fig. 5.5 The Simulation Results Topology, Fig. 5.1.

- a) Dc bus current. b) Dc bus voltage. c) Current and voltage of  $S_o$ . d) Current and voltage of  $S_i$ . e) 3-Phase load current. f) Frequency spectrum of  $I_a$ . g) Output inverter line-to-line voltage  $V_L$ . h) Frequency spectrum of  $V_L$ .

In this section, the PWM scheme, the inverter parameters and the component values obtained in sections 5.2 and 5.6 were used. Pspice package described in reference [18] was utilized to simulate the performance of the examined ZVS three-Phase PWM VSI topology shown in Fig. 5.1. The key currents and voltages through the topology are shown. Specifically:

Fig. 5.5 (a) demonstrates the dc bus current. As previously explained, the dc bus current becomes negative, whenever the inverter six-switches are commutating, recharging the capacitor  $C_o$ , and setting up ideal condition (zero-voltage switching) for the dc bus switch to be turned on.

Fig. 5.5 (b) depicts the dc bus voltage. As shown, the dc bus voltage is reduced towards zero after auxiliary switch  $S_o$  turns off, thus providing zero-voltage periods for the inverter switches main commutations.

Fig. 5.5 (c) shows the current and the voltage through the dc bus auxiliary switch  $S_o$ . Clearly, it displays zero switching losses.

Fig. 5.5 (d) illustrates the current and the voltage through one of the inverter switches. Obviously, it demonstrates zero switching losses.

Fig. 5.5 (e) shows the three phase output load currents.

Fig. 5.5 (f) points out the respective harmonic spectrum of one phase of the load currents.

Fig. 5.5 (g) depicts the output inverter line-to-line voltage  $V_L$ .

Fig. 5.5 (h) illustrates the respective harmonic spectrum of  $V_L$ .

## 5.8 Conclusions

A detailed analysis, design procedure and simulation results for the three-phase PWM VSI topology shown in Fig. 5.1, were presented in this chapter. The effective use of the dc bus commutating subcircuit topology No.

(1) Fig. 2.13 implemented in the analyzed system Fig. 5.1, has yielded zero-voltage switching condition for the inverter switches as well as for the dc bus switch. In addition to low circuit complexity, the dc bus commutating subcircuit implemented here does not affect the operating condition of the PWM scheme used. Therefore, minimum switching losses are achieved, while the advantages of the PWM scheme are maintained. Thus, the resulting topology can be used in high-power high-frequency applications with minimum switching losses.

The next chapter will be devoted to provide conclusions regarding the contents of this thesis. In addition, suggestions for further research in the field of soft switching conditions for PWM converters are provided.

### CONCLUSION AND SUGGESTIONS

#### 6.1 Conclusions

The advantages of converting power at high frequencies were described in chapter one. It was agreed that high frequency operating conditions for dc/dc converters yields high power density, low acoustic noise and better input and output converter spectrum characteristics.

As shown in chapter 2, the resonant dc/dc converters are suitable to operate at high frequencies since the switching losses and the EMI are low. However, these topologies are not practical in high power applications, since the switching devices have to be overrated as compared to the output power.

The PWM dc/dc converters aided by soft switching techniques in high power applications are the alternative to the resonant ones. In particular, dc bus commutation techniques can be considered as the best approach proposed thus far to provide a soft switching condition for PWM converters. However, the existing dc bus commutating subcircuits have some problems such as high circuit complexity and part counts.

This thesis presents two dc bus commutating subcircuits, which do not have the above mentioned problems while they create a zero-voltage switching condition for the inverter switches as well as for the dc bus switch. These two subcircuits can be implemented in low, medium and high power high frequency dc-to-dc PWM single and three-phase converters. The resulting converter topologies have nearly zero switching losses.

In particular, the dc bus commutating subcircuit proposed in chapter 3 topology No. (1) Fig. 2.13 for half-bridge PWM dc/dc converter yields zero

power switching losses. Moreover, the circuit complexity and part counts are very low. The resulting converter topology Fig. 3.1 can be used in low-power high-frequency applications.

Moreover, the dc bus commutating subcircuit proposed in chapter 4 topology No. (2) Fig. 2.14 , for full-bridge PWM dc/dc converter, yields significant reduction of the switching losses. However, the circuit complexity is relatively high. The resulting converter topology Fig. 4.1 can be used in medium-power high-frequency applications.

In chapter 5, the implementation of the dc bus commutating subcircuit, topology No. (1) Fig. 2.13 for three-phase PWM VSI yields zero switching losses. In addition, the dc bus commutating subcircuit does not affect the PWM operating condition. Therefore, minimum switching losses and switch stresses are obtained, while the advantages of the PWM used are maintained. The resulting topology Fig. 5.1 can be used in high-power high-frequency applications.

Finally, due to the presence of the dc bus commutating subcircuits the inverter switches of the topologies Fig. 3.1 Fig. 4.1, and Fig. 5.1 can be protected under adverse operating conditions. The protection could be done as follows: Since the inverter output voltage or current is always sampled, a signal could be sent to a the dc bus switch base drive. This signal could turn-off the dc bus switch, thus shutting the system off under abnormal inverter operating conditions.

## 6.2 Suggestions

The continuing demand for product size reduction, less acoustic noise and better control of output current and voltage of the power supply systems,

forces power supply designers to strive for a greater degree of perfection. PWM converters will continue to fulfill the above requirements for some years to come. However, there is still a lot of work to be done to perfect the PWM conversion process resulting in higher efficiencies and more reliable operation conditions. Specifically, eliminating the switching losses will contribute in improving the overall system efficiency and reliability by decreasing switch stresses.

The trend to achieve these objectives is by using dc or ac bus commutated subcircuits. In fact, these subcircuits reduce the switching losses and the stresses through the inverter switches. Moreover, the circuit complexity and part counts of the converter topology when using these subcircuits are relatively low.

In near future, the parasitic elements of the converter devices such as mosfet drain-source capacitance, transformer leakage inductance and others could possibly be used in an advantageous manner to reduce the switching losses at high frequencies operation. Successful approaches in this area may eliminate the need of any external subcircuits to provide soft switching conditions. Thus, more compact and lighter power supplies operating at high switching frequencies with minimum switching losses can be achieved.

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