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**ZERO VOLTAGE SWITCHING
FLYBACK AND FORWARD CONVERTER TOPOLOGIES**

Youhao Xi

A Thesis

in

The Department

of

Electrical and Computer Engineering

**Presented in Partial Fulfillment of the Requirements
for the Degree of Master of Applied Science at
Concordia University
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ABSTRACT

Zero voltage switching flyback and forward converter topologies

Youhao Xi

Advanced telecommunication and computer systems demand high efficiency and high power density, distributed power supplies. Both the flyback and forward converter topologies are good candidates for these applications, owing to their simple circuitry. These topologies, however, require practical performance improvements.

Improved zero voltage switching (ZVS) flyback and forward dc/dc converter topologies are developed in this thesis. They employ an auxiliary circuit, with only a few small components and switching devices, to achieve ZVS of the main switch. Steady state analyses are performed and show that the proposed topologies have the following merits: lossless switching of the main switch independent of the line and load conditions, no increase in conduction losses, simple power and control circuitry, and capability of operating in either voltage or current mode control.

The small signal analysis and closed loop stability of the proposed topologies are also derived. The resulting compensation required for stable operation is obtained and shown to be straightforward.

The steady state and small signal analyses are verified on a 50W prototype flyback converter switching at 200 kHz, and on a 100 W prototype forward converter

switching at 300 kHz, respectively. Experimental results show that both the flyback and forward converters have about 5 to 7% higher efficiencies than the conventional hard switching converters for typical efficiencies of 70% and 85%, respectively. These topologies can therefore advantageously replace existing power supplies in advanced telecommunications and computer applications.

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LIST OF ACRONYMS

AC	Alternative Current
CA	error Current Amplifier
DC	Direct Current
EMI	Electromagnetic Interference
IC	Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PI	Proportional-Integral network
PWM	Pulse Width Modulation
rms	Root Mean Square value
VA	error Voltage Amplifier
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

LIST OF PRINCIPAL SYMBOLS

ω_o	angular frequency given by $1/\sqrt{L_m C_{snb}}$
ω_n	angular frequency given by $1/\sqrt{L_{op} C_{snb}}$ for the flyback topology, and by $\sqrt{2 / (L_{op} C_{snb})}$ for the forward topology
ω_r	angular frequency given by $n/\sqrt{L_s C_{snb}}$
C_m	input capacitor of a dc/dc converter
C_o	output capacitor
C_{snb}	snubber capacitor
D_1	primary side blocking diode of the auxiliary circuit
D_2	secondary side blocking diode of the auxiliary circuit
D_{o1}	rectifier diode in the output stage
D_{o2}	freewheeling diode in the output stage
D	nominal duty cycle of the main switch
D_{aux}	duty cycle of the auxiliary switch
D_{max}	maximum duty cycle of the main switch
D_{min}	minimum duty cycle of the main switch
D_e	effective duty cycle of the main switch in the forward topology
D_x	reduction in duty cycle of the main switch by L_x in the forward topology
\hat{d}	small signal deviation of D in Laplace transformation
\hat{d}_x	small signal deviation of D_x in Laplace transformation

f_c	cross over frequency of an open loop system
f_p	a pole of a transfer function
f_z	a zero of a transfer function
f_s	switching frequency
$G_{CA}(s)$	transfer function of the error current amplifier compensation network
$G_m(s)$	closed loop transfer function of the current loop
$G_{pw}(s)$	transfer function of the voltage loop power circuit
$G_{VA}(s)$	transfer function of the error voltage amplifier compensation network
$H_1(s)$	transfer function of current loop power circuit
$H_2(s)$	transfer function of the output stage of voltage loop
I_{ap}	primary peak current of the auxiliary circuit
I_{as}	secondary peak current of the auxiliary circuit
I_o	nominal output current
I_{peak}	peak switch current of the flyback topology
i_m	instantaneous magnetizing current in the forward topology
i_s	instantaneous secondary current of the power transformer
\hat{i}_{Lo}	small signal deviation of the output inductor current in Laplace transformation
\hat{i}_o	small signal deviation of the output current in Laplace transformation
K	turns ratio of the current sensor transformer
k	deviation factor of V_0 from V_{in}
L_{ap}	primary of the coupled inductors of the auxiliary circuit
L_{as}	secondary of the coupled inductors of the auxiliary circuit

L_m	magnetizing inductor of T_r
L_o	output inductor
L_s	additional secondary inductor in the forward topology
L_T	effective inductance seeing into primary winding of T_r in the forward topology
L_l	reflected inductance of L_s into the primary side of T_r
N_r	number of turns of the core resetting winding of T_r
N_p	number of turns of the primary winding of T_r
N_s	number of turns of the secondary winding of T_r
n	reciprocal of the turns ratio of the power transformer, equal to N_s/N_p
$Q1$	main switch power MOSFET
$Q2$	auxiliary switch power MOSFET
Q_C	clamp switch power MOSFET in the active clamp topology
Q_M	main switch power MOSFET in the active clamp topology
R_o	load resistor
R_D	on resistance of a power MOSFET
R_s	current sensor resistor
S	power switch
s	Laplace transformation variable
T_r	power transformer
T_s	switching cycle of the converter
u_{Q1}	instantaneous drain-to-source voltage of $Q1$
u_s	instantaneous secondary voltage of T_r

V_0	drain-to-source voltage of $Q1$ at the beginning of each switching cycle
V_{in}	input voltage of the DC/DC converter
V_o	nominal output voltage
V_{ref}	reference voltage
V_s	peak value of the secondary voltage of T_r
V_{sw}	peak-to-peak voltage of the saw-tooth signal in the PWM control unit
\hat{v}_{CA}	small signal deviation of the output voltage of CA in Laplace transformation
\hat{v}_o	small signal deviation of V_o in Laplace transformation
\hat{v}_{Rs}	small signal deviation of the voltage resulted from the sensed current in Laplace transformation
\hat{v}_{VA}	small signal deviation of the output voltage of VA in Laplace transformation

CHAPTER 1

INTRODUCTION

1.1 POWER SUPPLIES FOR TELECOMMUNICATION AND COMPUTER SYSTEMS

In recent years, telecommunication and computer systems have experienced fast growth. These advanced systems require distributed power supplies. The principal features of the supplies are constant operating frequency, high efficiency and high power density. The power levels are usually ranged from hundreds of watts down to thirty watts or lower.

To meet the requirements of these applications, a number of pulse width modulation (PWM) MOSFET topologies are commonly used to implement the distributed power supplies. These topologies include the full bridge, half bridge, push-pull, double switch forward, single switch forward and flyback topologies, which are listed in the sequence from high power level down to low power level. Each topology has unique properties which makes it best suited for a certain power level.

This thesis limits the discussion within applications with power level below 150

watts, where the single switch MOSFET forward and flyback topologies are best suited.

1.2 FLYBACK AND FORWARD TOPOLOGIES

Figs. 1.1 and 1.2 show the standard topologies of the single switch MOSFET flyback and forward converters, which are best suited for applications at power level below 150 W and dc line voltages below 200 V. Their operating principles are briefed below. Each topology has advantages and drawbacks, which are compared in Table 1.1.

The transformer of the flyback is operated in the indirect power transfer mode. When the switch is turned on, a rising current flows through the primary winding (an inductor), thus an amount of energy is stored in the core of the transformer. When the switch is turned off, the dotted end of the secondary winding (another inductor) reverses the voltage polarity. Thus, the rectifier diode is forward biased and the stored energy is transferred to the output via the secondary winding and the rectifier. Periodical switching of the switch will keep the power continuously flowing from the input to the output. By modulating the pulse width of each switching signal, the output voltage is regulated.

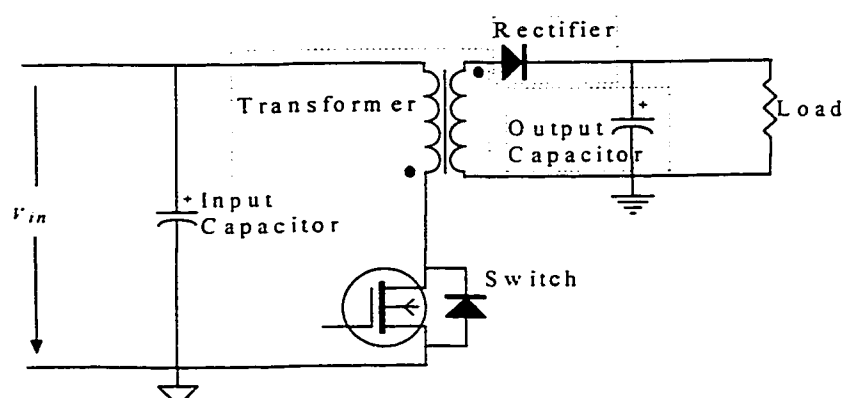


Fig. 1.1 A flyback converter topology.

The transformer of the forward is operated in the direct power transfer mode. When the switch is turned on, an amount of energy is transferred to the output via the transformer and the rectifier. When the switch is turned off, the core of the transformer is reset by a tertiary winding. Periodical switching of the switch will keep the power flowing from the input to the output. By modulating the pulse width of each switching signal, the output voltage is regulated.

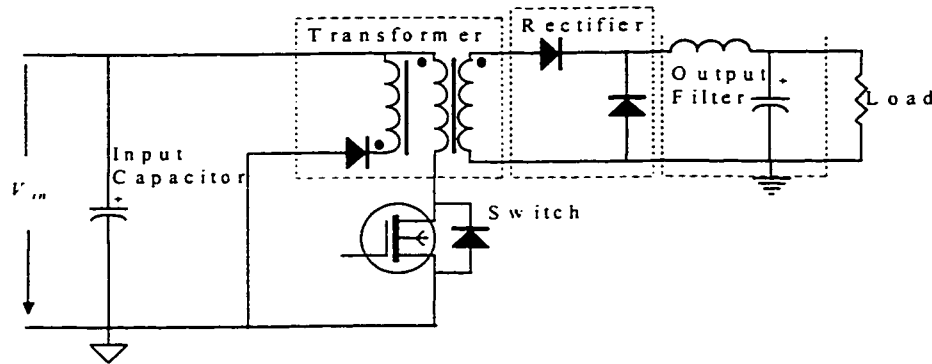


Fig. 1.2 A forward converter topology.

Table 1.1 Comparison between the two topologies based on the same power level and operating frequency

	The flyback topology	The forward topology
Advantages	<ol style="list-style-type: none"> 1. Simpler circuitry: no output inductor, only one rectification diode in the output stage, 2. Simpler transformer structure, 3. Better regulating of slave outputs against the load variations in multi-outputs applications. 	<ol style="list-style-type: none"> 1. Less rms and peak currents, 2. Less ripple in the output voltage, 3. Smaller output capacitor needed.
Disadvantages	<ol style="list-style-type: none"> 1. Higher RMS and peak currents, 2. Larger ripples in the output voltage, 3. Bigger output capacitor needed. 	<ol style="list-style-type: none"> 1. Output inductor and two more diodes are needed, 2. One more set of winding of the power transformer is needed to reset the core, 3. Poor regulation of slave outputs against the load variations.
Applications	<ol style="list-style-type: none"> 1. Low output current, 2. Relatively lower power level, 3. Multiple outputs. 	<ol style="list-style-type: none"> 1. High output current, 2. Relatively higher power level, 3. Better for single output.

1.3 PROBLEMS WITH THE STANDARD TOPOLOGIES AND SOLUTIONS

Unfortunately, the standard flyback and forward topologies are operated with hard switching, that is, there are significant overlaps between the switch current and voltage during the turn-on and turn-off transients. These overlaps causes the so called switching losses. Thus, it is difficult to achieve high power density and high efficiency with the standard topologies.

In order to achieve high power densities, the power supplies are operated at increasingly higher frequencies. However, when the switching frequency increases, the losses associated with the turn-on and turn-off of the power switching devices in the hard switching MOSFET converters also increase. These losses are so significant that operation of the converters above 50 kHz is prohibitive, because of the low conversion efficiency and high cooling requirements.

Over the years, the resistor-capacitor-diode snubber (RCD) has been employed to reduce the turn-off voltage stress and switching losses in the switches of converters. However, the power removed from the switching losses due to RCD dissipates completely in RCD itself. Thus, RCD has no contributions to achieve high efficiency nor to reduce the size of the cooling devices. Hence, RCD is not an solution to the applications concerned herein.

Normally, the solution is to employ the soft switching techniques. There are two

types of soft switching techniques, namely zero voltage switching (ZVS) and zero current switching (ZCS). Both can eliminate or greatly reduce the switching losses. But it has been shown in [1] that ZVS is a better scheme than ZCS in the MOSFET converter topologies. Owing to this reason, a lot of work has been done to develop ZVS flyback/forward topologies.

1.4 REVIEW OF EXISTING ZVS FLYBACK/FORWARD TOPOLOGIES

Several ZVS flyback /forward converter topologies have been proposed, including the active clamp converters [2-13], the “mirror-structured” converters [14], and the non-dissipative snubber [15-17]. Although ZVS is achieved in these converter topologies, they have at least one of the following drawbacks: complicated control schemes, increased conduction losses, loss of ZVS under the light load conditions, under utilization of power transformer, and restrictions on use due to patents.

1.4.1 Active Clamp Topology

Fig. 1.3 shows an active clamp forward converter topology, where a clamp circuit consisting of a switch and a capacitor is added to the standard forward circuit. With the clamp circuit, ZVS is achieved in the main switch. The clamp circuit of Fig. 1.3 can also be employed in the flyback topology, forming an active clamp flyback converter.

The drawbacks of these topologies include:

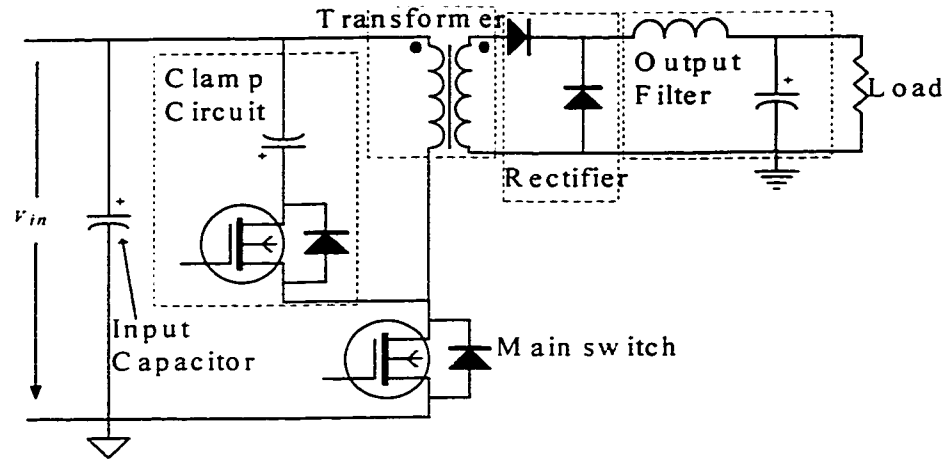


Fig. 1.3 An active clamp forward converter topology.

- (i) They need an isolated, variable duty cycle gate drive for the clamp switch,
- (ii) They require a modified PWM control technique to properly program the associated delays between gate drives of the main and clamp switches, so as to achieve ZVS,
- (iii) ZVS is lost under light load conditions.
- (iv) ZVS is achieved at the cost of increased conduction losses,
- (v) The current mode control can not be used,
- (vi) The patent related legal issues make it difficult to use, because it is a patented technique.

1.4.2 'Mirrored structure' Topology

Fig. 1.4 shows a ZVS flyback converter topology which has a mirrored structure on both sides of the power transformer [14], where a MOSFET switch replaces the rectifier diode of the standard flyback circuit. Other topologies like the forward can be converted into a ZVS operation in the same manner.

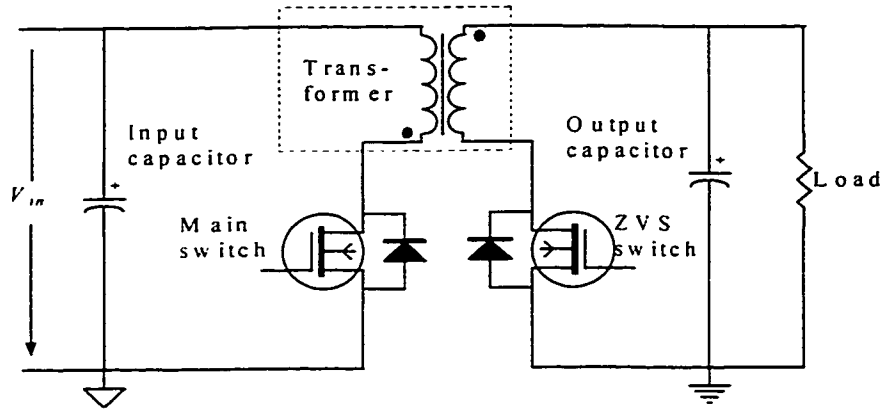


Fig. 1.4 The 'mirrored-structure' ZVS flyback converter.

The mirrored structure circuit employs fewer components than the active clamp converter. As the output voltage is usually low ($<24\text{ V}$) for the telecommunication and computer systems applications, a low voltage rating MOSFET can be selected for the ZVS switch. The drawbacks of this topology include:

- (i) It needs an isolated gate drive for the ZVS switch,
- (ii) The utilization of the power transformer is poorer,
- (iii) The conduction losses are increased,
- (iv) Larger ripples are resulted on the output capacitor.

1.4.3 Passive Non-dissipative Snubber Flyback/Forward Topologies

Fig. 1.5 shows a forward converter topology employing a non-dissipative snubber [15-17]. Two diodes and a capacitor and an inductor forms the snubber. No additional switch is required. This snubber can also be applied to a flyback converter topology.

The drawbacks of the non-dissipative snubber include: (i) The switch has a hard switching at turn-on, and (ii) The topology is not suitable for applications when the input

voltage varies in a wide range.

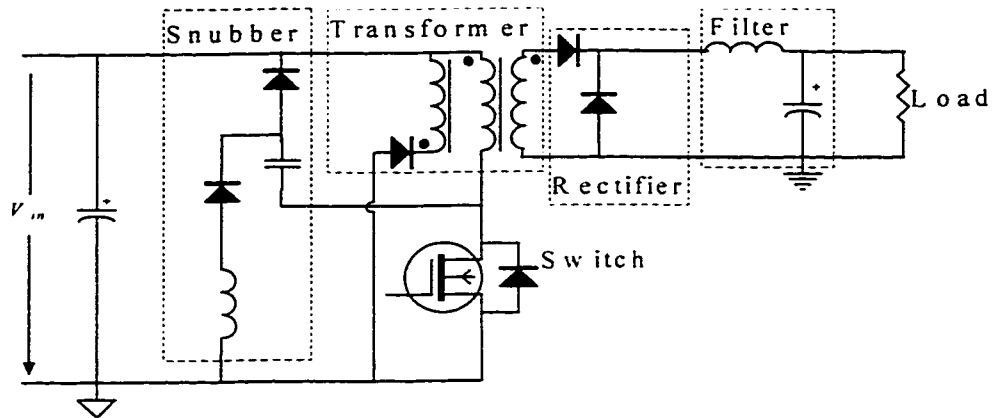


Fig. 1.5 A forward converter with a non-dissipative snubber.

1.5 SCOPE AND CONTRIBUTIONS OF THIS THESIS

The objective of this thesis is to propose and analyze ZVS flyback and forward topologies that can overcome the following drawbacks of the existing topologies:

- (i) complicated gate drive schemes,
- (ii) loss of ZVS under light load,
- (iii) no ability to employ current mode control,
- (iv) increase in conduction losses,

and to compare performance of the proposed topologies with that of the standard (conventional hard switching) flyback and forward converters.

The scope of this thesis is limited to the steady state analyses, small signal analyses, experimental verifications, and design of the proposed topologies for applications at the power level below 150 W, switching frequency between 200 kHz and

300 kHz, dc line voltage below 200V. Average current mode control is selected as the control scheme.

The principle contributions of this thesis are as follows:

(i) ZVS flyback and forward converter topologies are proposed and analyzed. It is shown that the proposed topologies have several advantages over the existing ZVS and conventional flyback and forward topologies, including no increase in conduction losses, simplicity in both power and control circuitry, lossless switching independent of line/load conditions.

(ii) Prototype flyback and forward converters of the proposed topologies are built, which are operated at 200 kHz and powering 50 W, and at 300 kHz and powering 100W, respectively. Experimental verifications of the theoretical analyses are performed with these prototypes. Comparisons of efficiencies between the proposed converters and the conventional hard switching converters are made, which show that the proposed converters have about 5% to 7% higher efficiency.

(iii) The design procedures for the proposed converter topologies are presented.

1.6 THESIS OUTLINE

The contents of each chapter in this thesis are summarized below.

In Chapter 2, a ZVS flyback converter topology is presented. The principles of operation are illustrated and modes of operation are detailed. The steady state operation in each mode is analyzed. Parameters evaluating the steady state performance of the

converter are derived. Experimental results of the prototype flyback converter are presented and are compared with the theoretical predictions.

In Chapter 3, a ZVS forward converter topology is presented. The principle of operation is illustrated and modes of operation are detailed. The steady state operation in each mode is analyzed. Some parameters evaluating the steady state performance of the converter are derived. Experimental results of the prototype forward converter are presented and are compared with the theoretical predictions.

In Chapter 4, small signal models are discussed, based on the average current mode control. The flyback converter can utilize the same small signal model as a conventional flyback converter. The small signal model of the forward converter is derived. The compensation for both the current and voltage loops is discussed and the small signal analysis of the forward converter is verified experimentally.

In Chapter 5, design procedures are presented. Design examples are given for both the flyback and forward topologies. A simple implementation of generating of the gating drive signals for the auxiliary switch is presented.

In Chapter 6, research and development in the thesis are summarized. Advantages and disadvantages of the proposed topologies are discussed. Suggestions for future work are made.

CHAPTER 2

A ZVS FLYBACK CONVERTER TOPOLOGY

2.1 INTRODUCTION

Among the conventional dc/dc converters, the flyback topology employs the fewest power components and devices. It is best suited for multiple output applications at total power levels below 150 W and dc line voltages above 100 V. However, as mentioned previously, the standard flyback is unable to meet the requirements for high power density and high efficiency, and the existing ZVS flyback converters have several previously mentioned drawbacks. Research for better solutions is hence required.

This chapter presents a ZVS flyback converter topology which is able to overcome some of the drawbacks of the existing topologies. The topology employs an auxiliary circuit that helps to achieve ZVS in the main switch, with addition of only a few number of small power rating components and devices.

The converter operates in the discontinuous mode. The continuous mode operation is not recommended here since it is not easy to stabilize the converter. A steady state analysis of the converter is presented in this chapter to understand the behavior and to develop performance characteristics.

The circuit description is made in Section 2.2. The modes of operation are detailed in Section 2.3. The steady state analysis is performed in Section 2.4. Performance is discussed in Section 2.5 and experimental verifications are made in Section 2.6.

2.2 CIRCUIT DESCRIPTION

Fig. 2.1 shows a ZVS flyback converter topology employing an auxiliary circuit drawn inside the dashed line block. Outside the block is a standard flyback topology shown in Fig. 1.1.

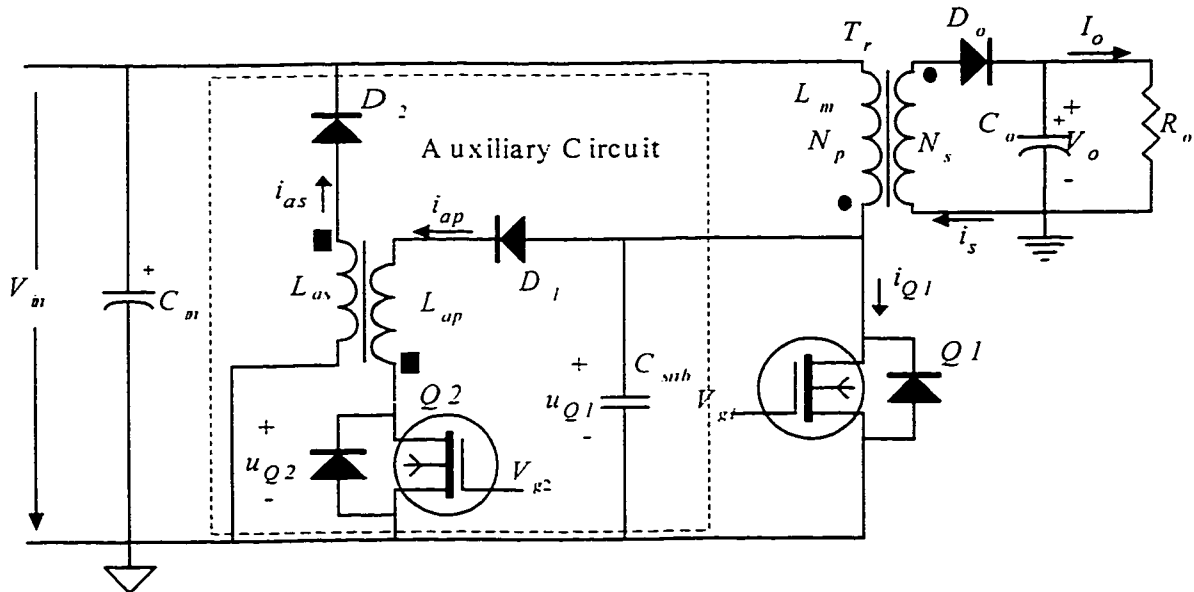


Fig. 2.1 The proposed ZVS flyback converter topology.

In Fig. 2.1, C_m is the input capacitor, T_r is the power transformer with windings N_p (primary) and N_s (secondary), L_m is the magnetizing inductance of T_r , D_o is the output rectifier diode, C_o is the output capacitor, R_o is the load and $Q1$ is the main switch.

The auxiliary circuit consists of (i) a snubber capacitor C_{snb} , which is connected in parallel with the main switch $Q1$, (ii) two coupled inductors L_{ap} (primary) and L_{as} (secondary), (iii) two blocking diodes D_1 and D_2 , and (iv) an auxiliary switch $Q2$.

2.3 MODES OF OPERATION

Fig. 2.2 shows key waveforms of the proposed converter. For each switching cycle, T_s , the converter operates in the following five intervals. In the operation of a standard flyback, there are no Intervals 1 and 3. These two intervals are fulfilled by the auxiliary circuit and are introduced here to achieve ZVS in the main switch, $Q1$, during both its turn-on and turn-off transients.

2.3.1 Interval 1 ($t_1 < t \leq t_2$)

Fig. 2.3(a) shows the circuit operation during this interval. At the beginning of this interval, $Q2$ is turned ON. It has a zero current turn-on, because L_{ap} is in series with it. Its drain-to-source voltage falls rapidly to zero, and a resonant loop consisting of C_{snb} , L_{ap} and L_m , as shown in Fig. 2.4, is formed. C_{snb} starts to discharge through L_{ap} . The discharging current builds up a magnetic field in the core of the coupled inductors, transferring the stored energy in C_{snb} in the previous cycle to the core of L_{ap} .

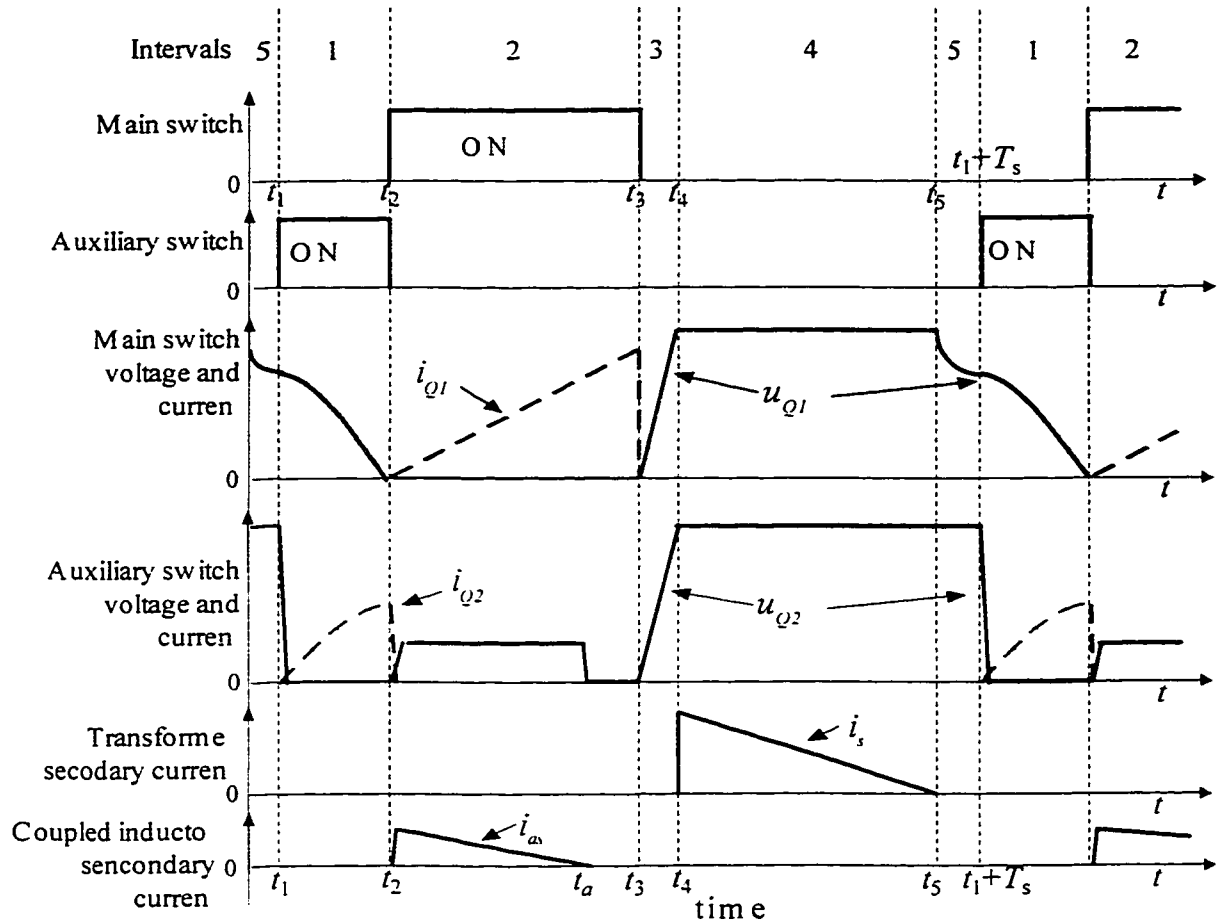


Fig. 2.2 Key waveforms of the converter of Fig. 2.1. The converter operates in five modes per switching cycle. Variables are defined in Fig. 2.1

At the end of this interval, $t = t_2$, C_{sub} is depleted. As a consequence, the drain of $Q1$ is pulled down to zero voltage, providing the ZVS condition for $Q1$ at its turn-on. During this interval, C_o supplies the output current.

2.3.2 Interval 2 ($t_2 < t \leq t_4$)

Fig. 2.3(b) shows the circuit operation during this interval. At the beginning of this interval, $Q1$ is turned ON under the zero voltage condition. Hence it has no turn-on losses. At the same moment, $Q2$ is turned OFF, stopping the current in L_{ap} rapidly. The

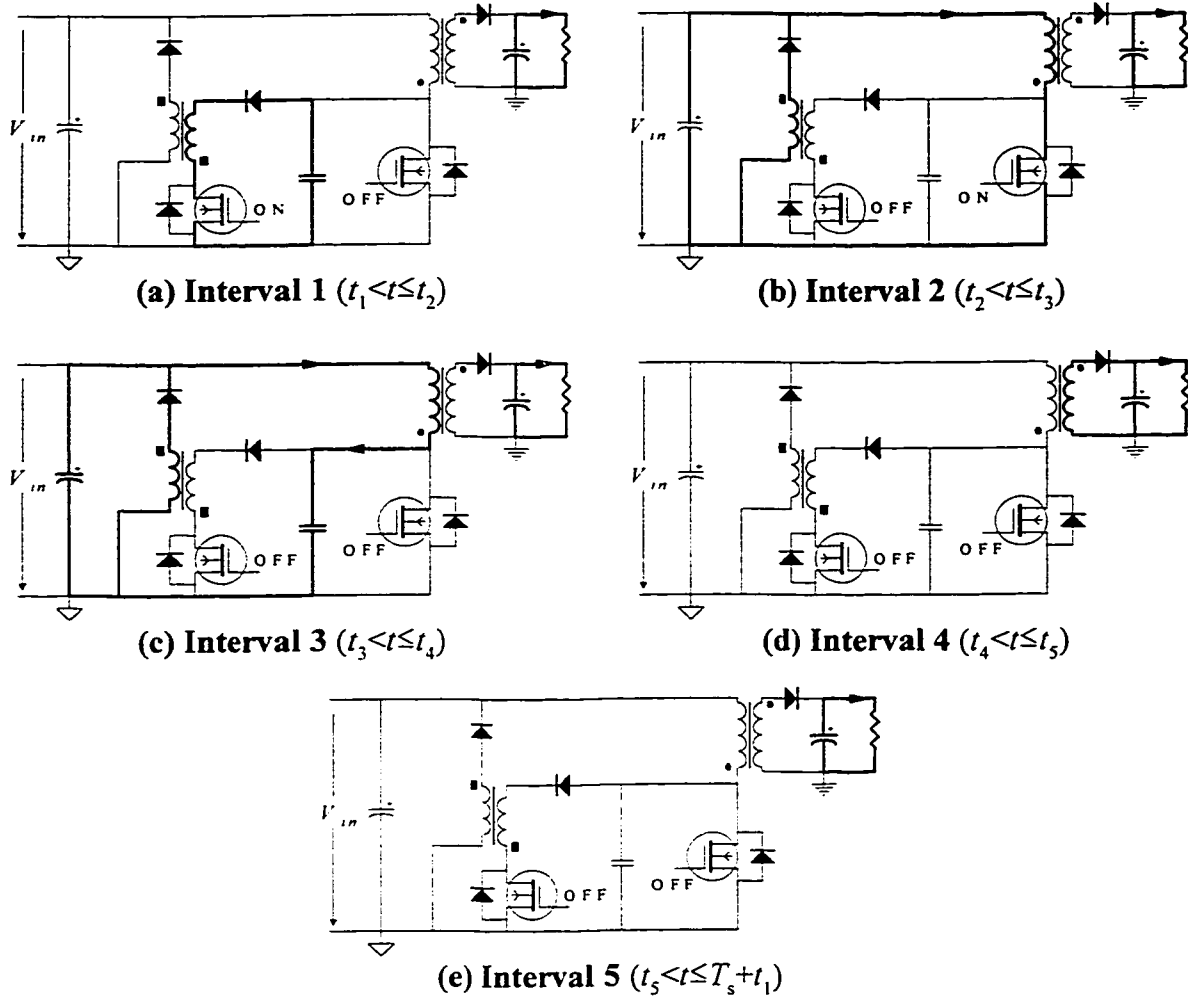


Fig. 2.3 Modes of operation of the converter of Fig. 2.1. The operation is divided into five modes per switching cycle. The key waveforms are shown in Fig. 2.2.

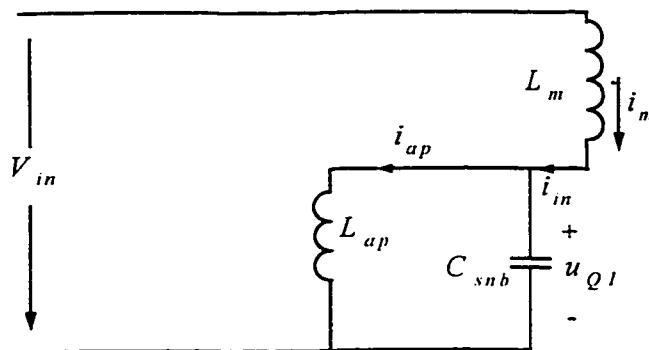


Fig. 2.4 The equivalent circuit of the discharging resonant loop in Interval 1. Variables are defined in Fig. 2.1.

rapidly falling current in L_{ap} reverses the voltage polarity on the dotted ends of the coupled inductors. Thus D_2 becomes forward biased and is forced to conduct.

When D_2 is conducting, L_{as} sees a constant voltage V_m . Through coupling, L_{ap} sees a reflected voltage. This voltage is the stress voltage on $Q2$. By increasing the ratio of L_{as} to L_{ap} , the stress will be lower. This in turn reduces the turnoff switching losses in $Q2$. On the other hand, the current in L_{as} is decreasing linearly. In this way the stored energy in the core of the coupled inductors is gradually fed back into the input line. At $t = t_a$, the process completes and D_2 becomes reverse biased again.

When $Q1$ is ON, the magnetizing inductor of T_r sees a constant voltage V_m . Thus, the current in $Q1$ rises linearly. In this way the energy is stored in the core of T_r in the same fashion as in a standard flyback converter. During this interval, C_o supplies the output current.

2.3.3 Interval 3 ($t_3 < t \leq t_4$)

Fig. 2.3(c) shows the circuit operation during this interval. At the beginning of this interval, $Q1$ is turned OFF. C_{snb} is in the process of charging and it slows down the rise of the drain voltage of $Q1$. A sufficient value of capacitance of C_{snb} will guarantee a ZVS turnoff. The current in the primary side is decreasing in a resonant mode, with an angular frequency determined by L_m and C_{snb} . The decreasing of the primary current reverses the polarity on the dotted ends of T_r . But before the voltage of the secondary side of T_r reaches the output voltage V_o , D_o maintains reverse biased. C_o supplies the output

current during this interval.

2.3.4 Interval 4 ($t_4 < t \leq t_5$)

Fig. 2.3(d) shows the circuit operation during this interval. At the beginning of this interval, the voltage of the secondary side reaches V_o . Then D_o is forward biased and begins to conduct. The secondary current refills C_o , and also supplies the output current. In this way the stored energy in T_r is now transferred to the output.

The conduction of D_o causes N_s to see a constant voltage V_o . This in turn clamps the voltages on both primary and secondary windings, and consequently, it clamps the voltage across the main switch QI .

2.3.5 Interval 5 ($t_5 < t \leq t_1+T_s$)

Fig. 2.3(e) shows the circuit operation during this interval. At the beginning of this interval, the stored energy in T_r is completely transferred to the load. Then D_o is reversed biased again and C_o supplies all the output current. The difference between the drain voltage of QI and the dc line voltage V_m causes a resonance in the network consisting of L_m and C_{sub} .

At the end of Interval 5, a new cycle begins and Intervals 1 through 5 repeat.

2.4 STEADY STATE ANALYSIS

The operating principle has been described in last section. In this section the

steady state analysis is performed with the assumptions made below. In the analysis, the time varying variables such as the current and voltage of the principal components and devices are determined. Based on these variables, the performance of the converter is illustrated, and the resultant quantities such as the rms, average or peak current and voltage of the principal components and devices are obtained in Section 2.5. These quantities are used in designing the converter as presented in Chapter 5.

In the analysis presented below, a closed form solution is obtained by solving a set of differential equations in each interval and by matching the boundary conditions at the boundary of each interval. The initial conditions are a function of the operating frequency f_s , the input dc line voltage V_m and the output power P_o . These initial conditions can be obtained by the iterative process such as the Newton-Raphson method.

2.4.1 Assumptions, Definitions and Initial Conditions

For convenience, following assumptions are made:

- (i) The steady state conditions have been established, and the converter is running at the nominal output voltage V_o and the static load condition: P_o ,
- (ii) Each component and device has ideal properties, that is
 - (1) T_r : the leakage inductance is ignored, and the core does not saturate,
 - (2) L_{ap}, L_{as} : the coupling factor is 1.0, and the core does not saturate,
 - (3) C_o, C_{snb} : pure capacitors, and the capacitance of C_o is infinite,
 - (4) D_1, D_2, D_o : the forward voltage drop is 0 V, the recovery time is 0 s,
 - (5) $Q1, Q2$: the on resistances are 0 Ω , the inherent capacitances are 0 F.

The effects of the non-ideal properties of the components and devices are investigated in Section 2.5.1.

(iii) The magnetizing inductance of the transformer, L_m , is much larger than L_{ap} .

Following parameters are defined:

ω_n --angular frequency of the resonant tank of C_{sub} and L_{ap} ,

ω_0 --angular frequency of the resonant tank of C_{sub} and L_m ,

i_{ap} --instantaneous current in $Q2$,

I_{ap} --peak current in $Q2$,

i_{as} --instantaneous current in L_{as} ,

I_{as} --peak current in L_{as} ,

I_{mpeak} --peak magnetizing current in T_r ,

i_{Q1} --instantaneous current in $Q1$,

i_s --instantaneous secondary current,

I_s --peak secondary current,

n --reciprocal of turns ratio of T_r , or N_s/N_p ,

u_{Q1} --instantaneous drain voltage of $Q1$, or voltage across C_{sub} ,

u_{Q2} --instantaneous drain voltage of $Q2$,

V_0 --initial drain voltage of $Q1$ per switching cycle,

$V_{p,Q1}$ --clamped voltage stress of $Q1$ when it is OFF.

The analysis begins by stating the initial conditions of Interval 1:

(i) $Q1$ and $Q2$ are both OFF, and the drain voltage of the paralleled switches is V_0 ,

$$u_{Q1}(t_1) = u_{Q2}(t_1) = V_0 \quad (2-1)$$

$$i_{Q1}(t_1) = i_{ap}(t_1) = 0 \quad (2-2)$$

(ii) The magnetizing inductor L_m and C_{snb} undergoes a resonance, but the resonant current in L_m is negligible,

$$i_m(t_1) = 0 \quad (2-3)$$

(iii) Both D_2 and D_o are reverse biased, and C_o supplies the total output current,

$$i_{as}(t_1) = i_s(t_1) = 0 \quad (2-4)$$

2.4.2 Interval 1 ($t_1 < t \leq t_2$)

This interval starts at $t = t_1$. $Q2$ is turned on and C_{snb} and L_m forms a resonant tank as shown in Fig. 2.4. Hence the following equations govern the resonant process in this tank.

$$L_m \frac{di_m}{dt} + u_{Q1} = V_m \quad (2-5)$$

$$u_{Q1} = L_{ap} \frac{di_{ap}}{dt} \quad (2-6)$$

$$i_{ap} + C_{snb} \frac{du_{Q1}}{dt} = i_m \quad (2-7)$$

Combining Eqs. (2-5) through (2-7),

$$C_{snb} \frac{L_{ap} L_m}{L_{ap} + L_m} \frac{d^2 u_{Q1}}{dt^2} + u_{Q1} = \frac{L_{ap}}{L_{ap} + L_m} V_m \quad (2-8)$$

According to the assumption (iii), $L_{ap} \ll L_m$. Hence, Eq. (2-8) can be approximated as,

$$C_{snb} L_{ap} \frac{d^2 u_{Q1}}{dt^2} + u_{Q1} = 0 \quad (2-9)$$

By the definition made above,

$$\omega_n = 1/\sqrt{L_{ap}C_{snb}} \quad (2-10)$$

Giving the initial conditions expressed in Eqs. (2-1) through (2-4), Eqs. (2-9) and (2-6) yield, respectively

$$u_{Q1}(t) = V_0 \cos[\omega_n(t - t_1)] \quad (2-11)$$

$$i_{ap}(t) = V_0 \sqrt{C_{snb}/L_{ap}} \sin[\omega_n(t - t_1)] \quad (2-12)$$

Because D_2 and D_o are reverse biased and $Q1$ is OFF and $Q2$ is ON, the following equations are found to govern the respective variables in this interval.

$$i_{as}(t) = i_s(t) = i_{Q1}(t) = i_m(t) = 0 \quad (2-13)$$

$$u_{Q2}(t) = 0 \quad (2-14)$$

At the end of this interval, the resonance completes a quarter of its period, i.e., $\omega_n(t_2 - t_1)$ equals $\pi/2$. Thus, u_{Q1} always reaches zero regardless of V_0 which is determined by f_s , V_m and P_o ,

$$u_{Q1}(t_2) = 0 \quad (2-15)$$

and i_{ap} reaches the peak value given by

$$I_{ap} = i_{ap}(t_2) = V_0 \sqrt{C_{snb}/L_{ap}} \quad (2-16)$$

The final value of each variable in Interval 1 defines the initial conditions of Interval 2.

2.4.3 Interval 2 ($t_2 < t \leq t_3$)

This interval starts at $t = t_2$. $Q2$ is turned OFF and i_{ap} falls immediately to zero. A current is forced to flow through L_{as} and D_2 and into the input dc line, with an initial current I_{as} determined by the energy conservative equation,

$$\frac{1}{2} L_{as} I_{as}^2 = \frac{1}{2} L_{ap} I_{ap}^2 \quad (2-17)$$

which yields

$$I_{as} = I_{ap} \sqrt{L_{ap} / L_{as}} \quad (2-18)$$

Substituting Eq.(2-16) into (2-18),

$$I_{as} = V_0 \sqrt{C_{snb} / L_{as}} \quad (2-19)$$

L_{as} sees a constant voltage V_m . As $Q1$ is ON, L_m also sees a constant voltage V_m . Thus,

$$i_{as}(t) = I_{as} - \frac{V_m}{L_{as}}(t - t_2) \quad (2-20)$$

$$i_{Q1}(t) = i_m(t) = \frac{V_m}{L_m}(t - t_2) \quad (2-21)$$

As $Q1$ is ON and $Q2$ is OFF and D_o is reverse biased, therefore

$$i_s(t) = i_{ap}(t) = 0 \quad (2-22)$$

$$u_{Q1}(t) = 0 \quad (2-23)$$

At $t = t_a$, i_{as} reaches zero. Thus, by letting i_{as} be zero in Eqs. (2-20), t_a can be found,

$$t_a = \frac{I_{as} L_{as}}{V_m} + t_2 \quad (2-24)$$

Hence the voltage stress on $Q2$ is governed by

$$u_{Q2}(t) = \begin{cases} V_m \sqrt{L_{ap} / L_{as}} & t_2 < t \leq t_a \\ 0 & t_a < t \leq t_4 \\ u_{Q1}(t) & t_4 < t \leq t_1 + T_s \end{cases} \quad (2-25)$$

At the end of this interval, $t = t_3$, i_{Q1} reaches its peak value, as given by

$$I_{mpeak} = i_m(t_3) = \frac{V_m}{f_s L_m} D \quad (2-26)$$

where, f_s is the switching frequency, and

D is the switching duty cycle of $Q1$, which is required to regulate the output voltage at the static load conditions (discussed in Section 2.5.2) and is here equal to $(t_3-t_2)/T_s$.

The final value of each variable in Interval 2 defines the initial conditions of Interval 3.

2.4.4 Interval 3 ($t_3 < t \leq t_4$)

This interval starts at $t = t_3$. $Q2$ is turned OFF and C_{snb} is charged by i_m . Referring to Fig. 2.4, the drain voltage of $Q1$ in this interval satisfies the following equation

$$u_{Q1} + L_m C_{snb} \frac{d^2 u_{Q1}}{dt^2} = V_m \quad (2-27)$$

Giving the initial conditions determined by Eqs. (2-21) and (2-23), the solution of Eq. (2-27) can be obtained as

$$u_{Q1}(t) = V_m \left\{ 1 + \frac{\omega_0 D}{f_s} \sin[\omega_0(t - t_3)] - \cos[\omega_0(t - t_3)] \right\} \quad (2-28)$$

where, by the definition made previously,

$$\omega_0 = 1/\sqrt{L_m C_{snb}} \quad (2-29)$$

As both $Q1$ and $Q2$ are OFF and D_o is reverse biased, other variables in this interval are found to be governed by the following equations, respectively,

$$i_{Q1}(t) = i_{as}(t) = i_{Q2}(t) = i_s(t) = 0 \quad (2-30)$$

Investigating the rising speed of u_{Q1} by differentiating Eq. (2-28) and substituting Eq. (2-29) into the result:

$$\frac{du_{Q1}(t)}{dt} = V_m \left[\frac{D}{f_s L_m C_{snb}} \cos\left(\frac{t-t_3}{\sqrt{L_m C_{snb}}}\right) + \frac{1}{\sqrt{L_m C_{snb}}} \sin\left(\frac{t-t_3}{\sqrt{L_m C_{snb}}}\right) \right] \quad (2-31)$$

Eq. (2-31) reveals that the rising speed of u_{Q1} is controlled by C_{snb} . Giving the proper value of C_{snb} will sufficiently slow down the rise of u_{Q1} and hence achieve ZVS in $Q1$ at the turn-off transient.

The magnetizing current is given by

$$i_m(t) = C_{snb} \frac{du_{Q1}(t)}{dt} \quad (2-32)$$

At the end of this interval, $t = t_4$, u_{Q1} reaches the clamped voltage as given by

$$V_{p-Q1} = u_{Q1}(t_4) = V_m + \frac{1}{n} V_o \quad (2-33)$$

Thus, the duration of this interval can be determined by substituting Eq. (2-33) into (2-28) and solving the resultant equation for (t_4-t_3) . The final value of each variable in Interval 3 defines the initial conditions of Interval 4.

2.4.5 Interval 4 ($t_4 < t \leq t_5$)

This interval starts at $t = t_4$. D_o is forward biased and a current flows through N_s and D_o into the output end. As N_s has an inductance equal to $n^2 L_m$, the initial value of the secondary current, I_{sp} , can be obtained from the energy conservative equation,

$$\frac{1}{2} L_m I_{mpeak}^2 = \frac{1}{2} n^2 L_m I_{sp}^2 + \frac{1}{2} C_{snb} V_{p-Q1}^2 \quad (2-34)$$

which gives

$$I_{sp} = \frac{1}{n} \sqrt{I_{mpeak}^2 - L_m V_{p-Q1}^2} \quad (2-35)$$

N_s sees a constant voltage V_o , therefore

$$i_s(t) = I_{sp} - \frac{V_o}{n^2 L_m} (t - t_4) \quad (2-36)$$

As $Q1$ and $Q2$ are OFF and u_{Q1} is clamped, thus, the following equations are obtained

$$u_{Q1}(t) = V_{p-Q1} \quad (2-37)$$

$$i_{as}(t) = i_{Q1}(t) = i_{ap}(t) = i_m(t) = 0 \quad (2-38)$$

Because the converter is operated in the discontinuous conduction mode, the secondary current i_s will reach zero within one switching cycle. Thus, the relation between the peak value of the secondary current and the output power P_o is found to be

$$P_o = \frac{1}{2} n^2 L_m I_{sp}^2 f_s \quad (2-39)$$

Hence, at the end of this interval, $t = t_5$,

$$i_s(t_5) = I_{sp} - \frac{V_o}{n^2 f_s L_m} D' = 0 \quad (2-40)$$

where, D' is the equivalent duty cycle of rectifier D_o and is equal to $(t_5 - t_4)f_s$.

The duration of this interval can be determined by combining Eqs. (2-39) and (2-40) and solving the resultant equation for D' . The final value of each variable in Interval 4 defines the initial conditions of Interval 5.

2.4.6 Interval 5 ($t_5 < t \leq T_s + t_1$)

This interval starts at $t = t_5$. D_o is reverse biased again. $Q1$ and $Q2$ are OFF. C_{snb} and L_m undergo a resonance and this resonance obeys Eq. (2-27). Giving the initial conditions as determined by last interval, and solving the equation for u_{Q1} ,

$$u_{Q1}(t) = V_m + \frac{1}{n}V_o \cos[\omega_0(t - t_5)] \quad (2-41)$$

$$i_m(t) = C_{\text{sub}} \frac{du_{Q1}}{dt} = -\frac{V_o}{n} \sqrt{\frac{C_{\text{sub}}}{L_m}} \sin[\omega_0(t - t_5)] \quad (2-42)$$

As D_o and D_2 are reverse biased and $Q1$ and $Q2$ are OFF, thus,

$$i_s(t) = i_{Q1}(t) = i_{as}(t) = i_{ap}(t) = 0 \quad (2-43)$$

At the end of this interval, $t = T_s + t_1$, u_{Q1} reaches a voltage V_o , which is the steady state initial voltage of Interval 1 of each cycle. From Eq. (2-41), it is found that

$$V_o = u_{Q1}(T_s + t_1) = V_m + \frac{1}{n}V_o \cos[\omega_0(T_s + t_1 - t_5)] \quad (2-44)$$

Since L_m is much larger than L_{ap} , by comparing Eqs (2-42) to (2-12), i_m is negligible and hence ignored in the analysis of Interval 1, that is.

$$i_m(T_s + t_1) \approx 0 \quad (2-45)$$

The final value of each variable in Interval 5 defines the initial conditions of Interval 1 in the next switching cycle, which just repeats the same process as analyzed above..

2.5 PERFORMANCE

2.5.1 Effects of the Non-Ideal Components

The above analysis has been made under the assumptions of ideal components and devices. In fact, each component and device of the circuit has some non-ideal properties. For example, the leakage of the transformer, the ON resistance and the inherent capacitance of switches, and so on. It is important to determine whether they make a

remarkable deviation.

It can be explained as follows. The ON resistance of switch causes the so called conduction losses. The inherent capacitors indeed have some effects on the performance of the switch. But the output capacitor of the switches can be combined with C_{snb} , and the effects of input capacitor of the switches can be made negligible by employing strong gate drives. The blocking diodes in Fig. 2.1 can be chosen as nearly ideal ones, like the Schottky diode or the ultra-fast diode. However, the effect of the leakage inductances of the circuit are detectable on key waveforms.

The effects of the leakage inductance of the transformer become apparent in Interval 4. It is because in other intervals they can be combined with magnetizing inductance L_m . However, in Interval 4, the flux linked inductance (L_m) is clamped at a constant voltage (V_o/n), but the leakage inductance is not affected by this clamp action. The leakage, called L_{leak} in the following discussion, undergoes a resonance governed by

$$L_{leak} C_{snb} \frac{d^2 u_{Q1_leak}}{dt^2} + R_{ESR} C_{snb} \frac{du_{Q1_leak}}{dt} + u_{Q1_leak} = 0 \quad (2-46)$$

where u_{Q1_leak} is the voltage component of u_{Q1} caused by the leakage, and

R_{ESR} is the equivalent series resistance of the resonant loop.

The initial conditions of Eq. (2-46) are given by Eqs. (2-21) and (2-23). Thus, the solution of Eq. (2-46) is

$$u_{Q1_leak}(t) \approx I_{mpeak} \sqrt{\frac{L_{leak}}{C_{snb}}} e^{-\rho(t-t_4)} \sin[\omega_{leak}(t-t_4)] \quad (2-47)$$

where,

$$\rho = \frac{R_{ESR}}{2 L_{leak}} \quad (2-48)$$

$$\omega_{leak} \approx 1/\sqrt{L_{leak} C_{snb}} \quad (2-49)$$

Superimposing $u_{Q1_leak}(t)$ onto u_{Q1} will give the total voltage of C_{snb} .

Similarly, the leakage of L_{ap} and the inherent drain-to-source capacitor of $Q2$ undergo another resonance between the turnoff of $Q2$ and t_o , as given by

$$u_{Q2_leak}(t) \approx I_{ap} \sqrt{\frac{L_{a_leak}}{C_{oss_Q2}}} e^{-\lambda(t-t_2)} \sin[\omega_{a_leak}(t-t_2)] \quad (2-50)$$

where L_{a_leak} is the leakage of L_{ap} ,

C_{oss_Q2} is the inherent capacitance of $Q2$,

ω_{a_leak} is given by

$$\omega_{a_leak} \approx 1/\sqrt{L_{a_leak} C_{oss_Q2}} \quad (2-51)$$

λ is given by

$$\lambda = \frac{R_{a_ESR}}{2 L_{a_leak}} \quad (2-52)$$

where R_{a_ESR} is the equivalent series resistance of the resonant tank.

Hence, superimposing $u_{Q2_leak}(t)$ onto u_{Q2} will give the total drain voltage of $Q2$.

2.5.2 Determination of Duty Cycle for the Output Regulation

Combining Eqs. (2-39) and (2-40),

$$P_o = \frac{1}{2} n^2 L_m \left(\frac{V_o}{n^2 L_m} D' T_s \right)^2 f_s = \frac{V_o}{2 n^2 f_s L_m} D'^2 \quad (2-53)$$

Combining Eqs. (2-26), (2-33), (2-34), (2-40) and (2-53), the duty cycle required at the

input and load conditions is found to be

$$D = \frac{1}{V_{in}} \sqrt{f_s L_m \left[2P_o + f_s C_{sub} \left(V_{in} + \frac{V_o}{n} \right)^2 \right]} \quad (2-54)$$

When P_o is so large that the second term in the bracket of right side of Eq. (2-54) is negligible, Eq. (2-54) can be approximated as

$$D \approx \frac{1}{V_{in}} \sqrt{2f_s L_m P_o} \quad (2-55)$$

Then, substituting Eq. (2-55) into (2-54), and ignoring the second term, yield

$$nV_{in}D \approx V_o D' \quad (2-56)$$

2.5.3 Advantages and Disadvantages of the Proposed Converter

The following major advantages of the proposed converter can be identified.

(i) No need of an isolated gate drive for the auxiliary switch, because $Q2$ and $Q1$ have common source connection as shown in Fig. 2.1.

(ii) Generating of the gate drive signals is simple, because the on time of $Q2$, unlike in the case of the active clamp topology, is fixed at a quarter of the resonance period of the L_{ap} - C_{sub} tank.

(iii) The ZVS conditions, provided by Intervals 1 and 3, are not affected by the line and load conditions (refer to Eqs. (2-15) and (2-31)). Hence ZVS can always be achieved regardless of the line/load conditions.

(iv) Less EMI is generated. Substituting Eq. (2-31) into (2-32) and differentiating the equation with respect to time,

$$\frac{di_m}{dt} = V_{in} \left[\frac{-D}{f_s L_m \sqrt{L_m C_{snb}}} \cos\left(\frac{t-t_3}{\sqrt{L_m C_{snb}}}\right) + \frac{1}{L_m} \sin\left(\frac{t-t_3}{\sqrt{L_m C_{snb}}}\right) \right] \quad (2-57)$$

The first term in the bracket on the right hand of Eq. (2-57) principally governs the falling current in L_m . It indicates clearly that the snubber capacitor C_{snb} slows down the falling speed of the current, and hence lowering the EMI generated.

(v) Simple in circuitry, and all components of the auxiliary circuit require small power ratings, since they only handle the stored energy in C_{snb} .

(vi) Conduction losses are not increased. Unlike in the active clamp topology, where extra circulating power is required to flow in and out of the clamp capacitor, the proposed topology does not involve the extra circulating power. Hence the conduction losses are not increased.

The disadvantage of the proposed topology is that the auxiliary switch has a hard switching turn-off. But the switching losses in $Q2$ can be reduced to a very low level by selecting a MOSFET through trading off between the least ON resistance and the least inherent capacitance, and also by increasing the ratio of L_{as} to L_{ap} , which lowers the voltage stress on $Q2$ at turn-off as given by Eq. (2-25).

2.5.4 RMS, Average, Peak Current and Voltage Values

In the design, the rms, average or peak current and voltage are required to determine the rating requirements in selecting the components. Some of these values have been obtained in the analysis. Other values are calculated below.

(1) Rms current in $Q1$

The current in $Q1$ has a triangle waveform. Hence the rms current is

$$I_{RMS_Q1} = \sqrt{\frac{D}{3}} I_{mpeak} \quad (2-58)$$

Substituting Eqs. (2-26) and (2-54) into (2-58),

$$I_{RMS_Q1} = \frac{V_m}{\sqrt{3} f_s L_m} D^{\frac{3}{4}} = \sqrt[4]{\frac{[2P_o + f_s C_{snb} (V_m + \frac{1}{n} V_o)^2]^3}{9 f_s L_m V_m^2}} \quad (2-59)$$

Correcting Eq. (2-59) for a conversion efficiency less than 1, say η , the rms current becomes

$$I_{RMS_Q1} = \sqrt[4]{\frac{[2 \frac{P_o}{\eta} + f_s C_{snb} (V_m + \frac{1}{n} V_o)^2]^3}{9 f_s L_m V_m^2}} \quad (2-60)$$

(2) Rms current in $Q2$

The current in $Q2$ is one quarter of a sine wave, as given by Eq. (2-12). Hence, it is found that

$$I_{RMS_Q2} = \sqrt{\frac{1}{2\pi} \int_0^{\frac{\pi}{4}} (V_o \sqrt{C_{snb}/L_{ap}} \sin \theta)^2 d\theta} = \frac{1}{4} V_o \sqrt{\frac{\pi - 2}{\pi} \cdot \frac{C_{snb}}{L_{ap}}} \quad (2-61)$$

The average current is found to be

$$I_{av_Q2} = \frac{1}{2\pi} \int_0^{\frac{\pi}{4}} V_o \sqrt{C_{snb}/L_{ap}} \sin \theta d\theta = \frac{2 - \sqrt{2}}{4\pi} V_o \sqrt{C_{snb}/L_{ap}} \quad (2-62)$$

(3) Average current in D_2

The current in D_2 is triangular. From Eqs. (2-19) and (2-24), it is found that the average current in D_2 is given by

$$I_{av_D2} = \frac{1}{2} I_{as} \frac{t_a - t_1}{T_s} = \frac{C_{sub} V_0^2}{2V_m} f_s \quad (2-63)$$

(4) Average current in D_o

The current in D_o is triangular. From Eqs. (2-39) and (2-40), the average current in D_o is given by

$$I_{av_Do} = \frac{D'}{2} I_{sp} = \sqrt{\frac{2P_o}{f_s n^2 L_m}} = \frac{P_o}{V_o} \quad (2-64)$$

2.5.5 Losses Caused by the Auxiliary Circuit

(1) Switching losses in $Q2$: P_{s_Q2}

It is estimated that

$$P_{s_Q2} = \frac{1}{2} C_{oss_Q2} V_0^2 f_s + \frac{1}{3} I_{ap} V_m \sqrt{L_{ap}/L_{as}} t_{off_Q2} f_s \quad (2-65)$$

where C_{oss_Q2} is the output capacitance of $Q2$, and

t_{off_Q2} is the OFF transient time of $Q2$.

(2) Conduction losses in $Q2$: P_{c_Q2}

The losses are found to be

$$P_{c_Q2} = I_{RMS_Q2}^2 R_{D_Q2} \quad (2-66)$$

where R_{D_Q2} is the ON resistance of $Q2$.

(3) Conduction losses in D_1 and D_2 : $P_{c_D1\&2}$

The conduction losses in D_1 and D_2 are found to be

$$P_{c_D1\&2} = V_{F_D1} I_{av_Q2} + V_{F_D2} I_{av_D2} \quad (2-67)$$

where V_{F_D1} is the forward voltage drop of D_1 , and

$V_{F,D2}$ is the forward voltage drop of D_2 .

(4) Total losses by the auxiliary circuit

$$P_{l_a} = P_{s_Q2} + P_{c_Q2} + P_{c_{D1\&2}} \quad (2-68)$$

2.5.6 Losses Removed by ZVS Operation

(1) Switching losses in $Q1$ in a hard switching operation: $P_{s_{Q1}}$

The hard switching will cause switching losses in $Q1$ as estimated by

$$P_{s_{Q1}} = \frac{1}{2} C_{oss_{Q1}} V_o^2 f_s + \frac{1}{3} I_{mpeak} \left(V_{in} + \frac{1}{n} V_o \right) t_{off_{Q1}} f_s \quad (2-69)$$

where $t_{off_{Q1}}$ is the OFF transient time of $Q1$, and

$C_{oss_{Q1}}$ is the output capacitance of $Q1$.

(2) Net saving of power due to ZVS operation

The net saving of the power due to the ZVS operation of the proposed converter is approximately

$$\Delta P = P_{s_{Q1}} - P_{l_{Q2}} \quad (2-70)$$

2.6 EXPERIMENTAL RESULTS

2.6.1 Experiment Setup

A prototype ZVS flyback converter is built based on the design presented in Chapter 5. The circuit operates under an input dc line varying from 90 V to 160 V. The dc line voltage is obtained directly from a diode bridge rectifying an ac line voltage in a range of 75 V to 135 V. UC3855 is used as the PWM control chip. The schematic of the

circuit is shown in Fig. II.1 in Appendix II.

The operating conditions of the circuit are summarized as follows: (i) the dc line voltage range is 90 V to 160V (corresponding to a dc line voltage range 75 V to 135 V), (ii) the full load is 50 W, with two outputs, of which the master output is 10 W at 5 V and the slave output is 40 W at 20V, and (iii) the switching frequency is 200 kHz.

2.6.2 Key Waveforms

Fig. 2.5 shows the theoretical waveforms of u_{Q1} and i_{Q1} , which are drawn in MathCAD based on the equations which are found to govern u_{Q1} and i_{Q1} in the analysis presented in the previous sections. Fig. 2.6 shows the experimental results of the drain voltage and current of $Q1$ in the prototype converter. Comparison between the theoretical and experimental results are made in Table 2.1. It is seen that they are in good agreement.

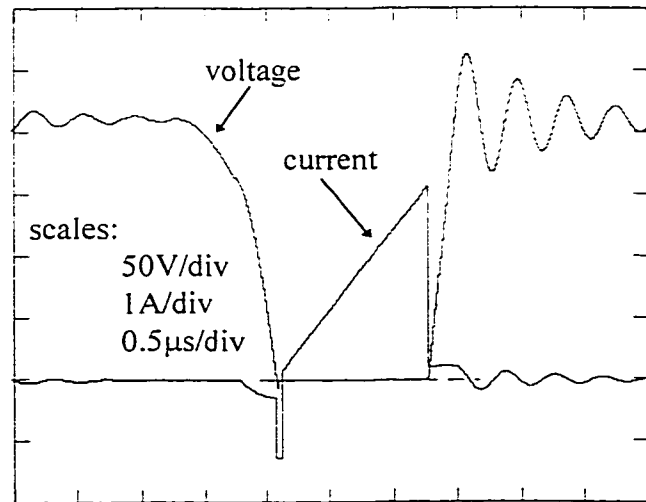


Fig. 2.5 Theoretical results: the drain voltage and current waveforms of $Q1$ in Fig. 2.1, which are predicted by the steady state analyses made in Section 2.4 and 2.5. The negative drain current is due to the latching of the body diode of $Q1$ before it is turned on.

Operating conditions: $V_{in}=130V$, $P_o=50W$, $f_s=200kHz$

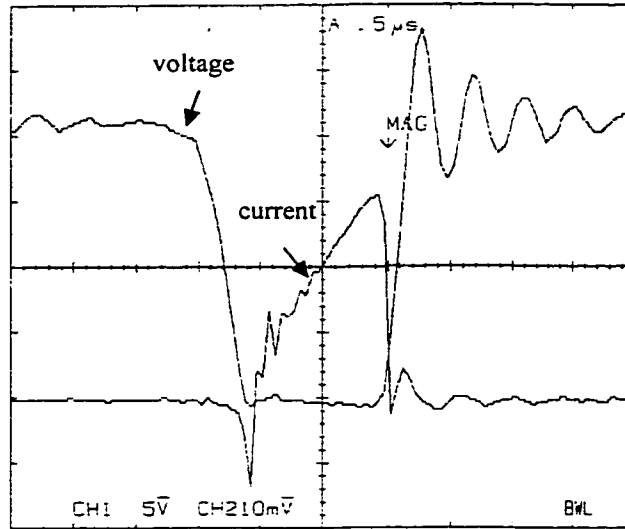


Fig. 2.6 The experimental results: the drain voltage and current waveforms of $Q1$ in the prototype ZVS converter of Fig. 2.1. The theoretical waveforms are shown in Fig. 2.5.
 Scales: vertical--50V/div., 1A/div.; horizontal--0.5 μ s/div.
 Operating conditions: $V_m=130$ V, $P_o=50$ W, $f_s=200$ kHz

Table 2.1 Comparison between the theoretical and experimental results of the current, voltage and duty cycle of the main switch.
 ($V_m=130$ V, $P_o=50$ W, $f_s=200$ kHz)

	D	V_{peak}	V_{off}	I_{peak}
Theoretical	0.23	273V	210V	3.16A
Experimental	0.22	280V	220V	3.22A

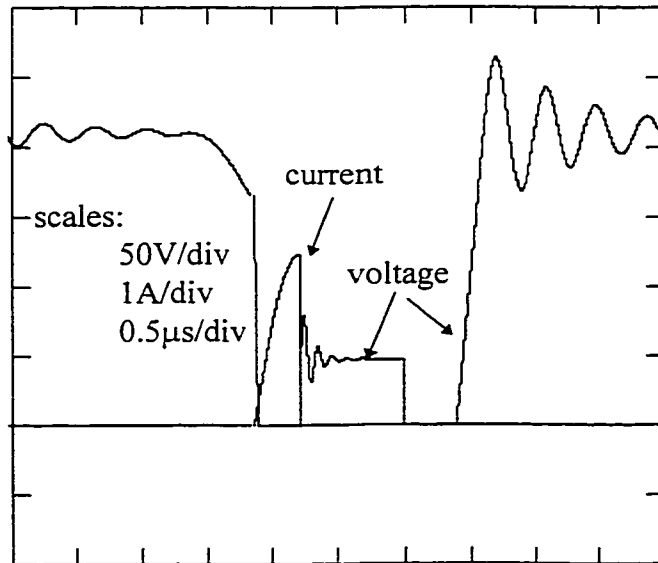


Fig. 2.7 The drain voltage and current waveforms of $Q2$ in Fig. 2.1, which are predicted by the steady state analyses in Sections 2.4 and 2.5.
 Operating conditions: $V_m=130$ V, $P_o=50$ W, $f_s=200$ kHz.

Fig. 2.7 shows the theoretical waveforms of u_{Q2} and i_{ap} , which are drawn in MathCAD based on the equations which are found to govern u_{Q2} and i_{ap} in the analysis presented in the previous sections.

Fig. 2.8 shows the experimental results of the drain voltage and current of $Q2$ in the prototype converter. Comparison between the theoretical and experimental results are made in Table 2.2. It is seen that they are in good agreement.

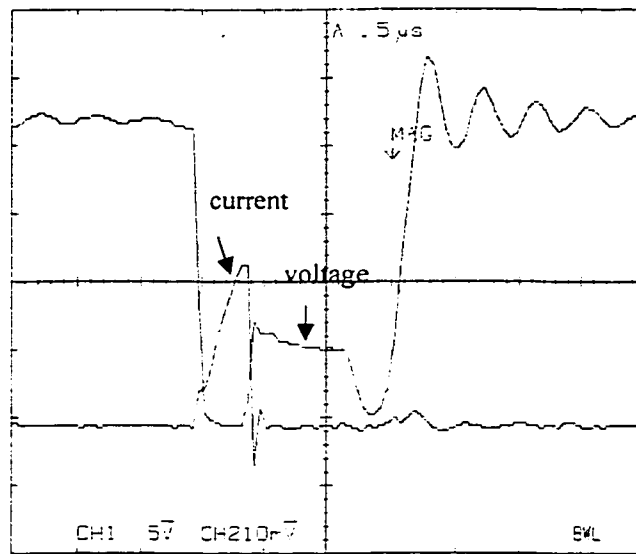


Fig. 2.8 The experimental results of the drain voltage and current waveforms of $Q2$ in the prototype ZVS converter of Fig. 2.1. The theoretical waveforms are shown in Fig. 2.7. Scales: vertical-50V/div. 1A/div.; horizontal-0.5 μ s/div. Operating conditions: $V_m=130V$, $P_o=50W$, $f_s=200kHz$

Table 2.2 Comparison between the theoretical and experimental results of the current, voltage and duty cycle of the auxiliary switch.

($V_m=130V$, $P_o=50W$, $f_s=200kHz$)

	D	t_a-t_2	V_{off}	I_{peak}
Theoretical	0.23	1.69 μ s	47.3V	2.69A
Experimental	0.22	1.60 μ s	52.0V	2.40A

Figs. 2.9 and 2.10 show the experimental key waveforms of the main switch $Q1$ and the auxiliary switch $Q2$, respectively, under light load condition. It is seen that ZVS is not lost at light load.

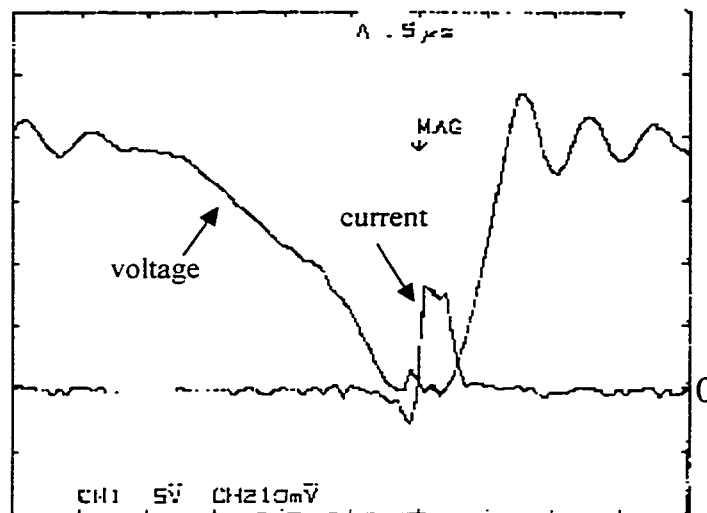


Fig. 2.9 Experimental results: the current and voltage waveforms of the main switch $Q1$ in ZVS operation under light load condition: $V_m=120V$, $P_o=10W$, $f_s=200kHz$.
Scales: vertical-50V/div. 1A/div.; horizontal-0.5 μ s/div.

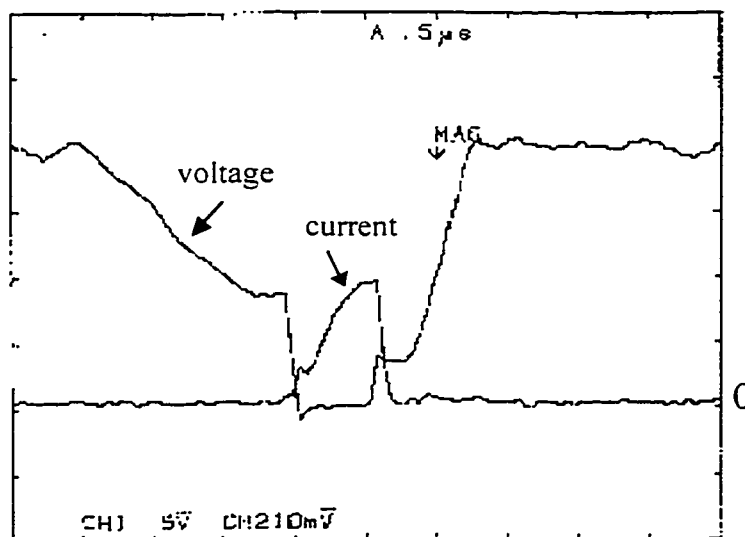


Fig. 2.10 The current and voltage waveforms of the auxiliary switch $Q2$ under light load condition: $V_m=120V$, $P_o=10W$, $f_s=200kHz$.
Scales: vertical-50V/div. 1A/div.; horizontal-0.5 μ s/div.

2.6.3 Efficiency

Experimental results of the efficiency from the prototype converter are obtained. The input dc voltage is obtained from a diode bridge rectifier which rectifies the ac line voltage varying between 75 V to 135 V (ac). For convenience, the experimental results of efficiency include the effect of this input rectifier stage.

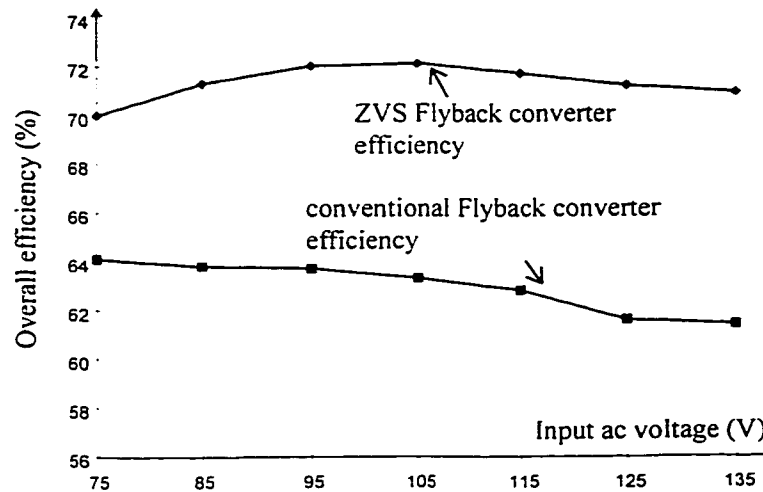


Fig. 2.11 The overall efficiency of the converter vs. input AC voltage (the range of AC voltage corresponds to a dc input voltage range of 90 to 160V). The efficiency of hard switching operation of the converter is made in comparison here. The output power is $P_o=50W$, and $f_s=200kHz$.

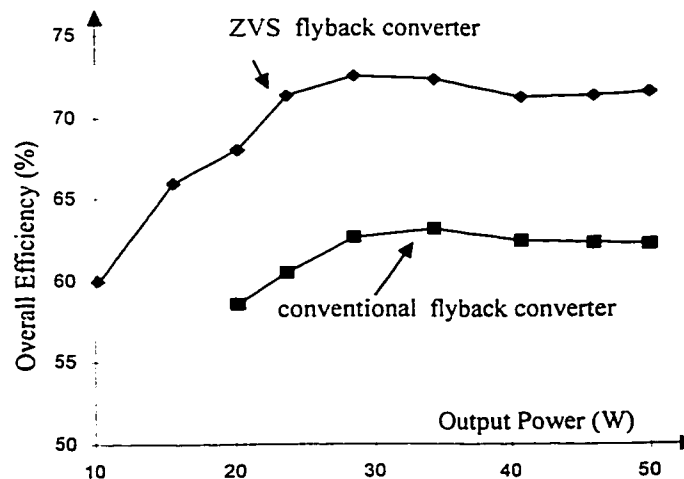


Fig. 2.12 The overall efficiency vs. load under given input voltage for both the proposed and conventional circuits. The efficiency measured includes the efficiency of the input ac-to-dc bridge rectifier stage. $V_{in}=120V$, $f_s=200kHz$.

Fig. 2.11 shows the efficiency of the converter vs. input voltage under the full load condition (50W). The comparison between the efficiencies of the ZVS and the hard switching flyback converters is also made in Fig. 2.11. The comparison shows that ZVS indeed makes a remarkable increase in efficiency: an increase of about 7% is obtained.

Fig. 2.12 shows the overall efficiency of the converter vs. load under given input voltage for both the proposed and conventional circuits. The proposed circuit always has higher efficiency than the conventional hard switching flyback converter.

2.7 CONCLUSIONS

In this chapter a ZVS flyback converter topology has been presented and analyzed. The steady state operation of the circuit can be divided into five distinct intervals. The steady state analysis of the circuit is performed and verified experimentally.

Analysis and experiments show that the performance of the proposed converter is enhanced with the auxiliary circuit. 7% higher efficiency has been achieved on the prototype circuit as compared with the conventional hard switching converter. Other major merits of the proposed ZVS flyback topology include:

- (i) Lossless switching of the main switch, independent of the line and load conditions,
- (ii) Simple power and control circuitry,
- (iii) No increase in conduction losses.

(iv) Ability to operate in either voltage or current mode control.

Therefore, the proposed converter topology provides an attractive alternative to the existing ZVS flyback topologies and it is promising in wide applications in telecommunication and computer systems in the future.

CHAPTER 3

A ZVS FORWARD CONVERTER TOPOLOGY

3.1 INTRODUCTION

The single switch forward converter topology is extremely popular in telecommunication and distributed dc bus applications. This topology offers a cost effective solution to fill the void created between the low power flyback topology and the more complex high power bridge types. Operating in continuous inductor current mode, the forward converter utilizes a much lower peak current than its flyback counterpart. This is advantageous with low voltage inputs.

As reviewed in Chapter 1, the conventional forward is not able to achieve high power density and high efficiency, and the existing ZVS forward converters have several previously mentioned drawbacks. Better solutions should be searched for.

This chapter presents a ZVS forward converter topology employs a similar auxiliary circuit to that in chapter 2, with a little modification. The auxiliary circuit helps to achieve ZVS in the main switch of the converter.

The converter operates in continuous mode in order to reduce the peak current in

the switch. A steady state analysis of the converter is presented in this chapter to understand the behavior and to develop performance characteristics.

The organization of this chapter is as follows. In section 2.2, the circuit description is presented. In Section 2.3, the modes of operation are detailed. In Section 2.4, the steady state analysis is performed. In Section 2.5 performance is discussed and in Section 2.6 experimental verifications are made.

3.2 CIRCUIT DESCRIPTION

Fig. 3.1 shows a ZVS forward converter topology employing the similar auxiliary circuit to that in Fig. 2.1, drawn in the dashed line block. A modification on the auxiliary circuit is that there is an additional small inductor L_s in series with the secondary winding. The reason of this modification is revealed by the analysis in Section 3.4.2.

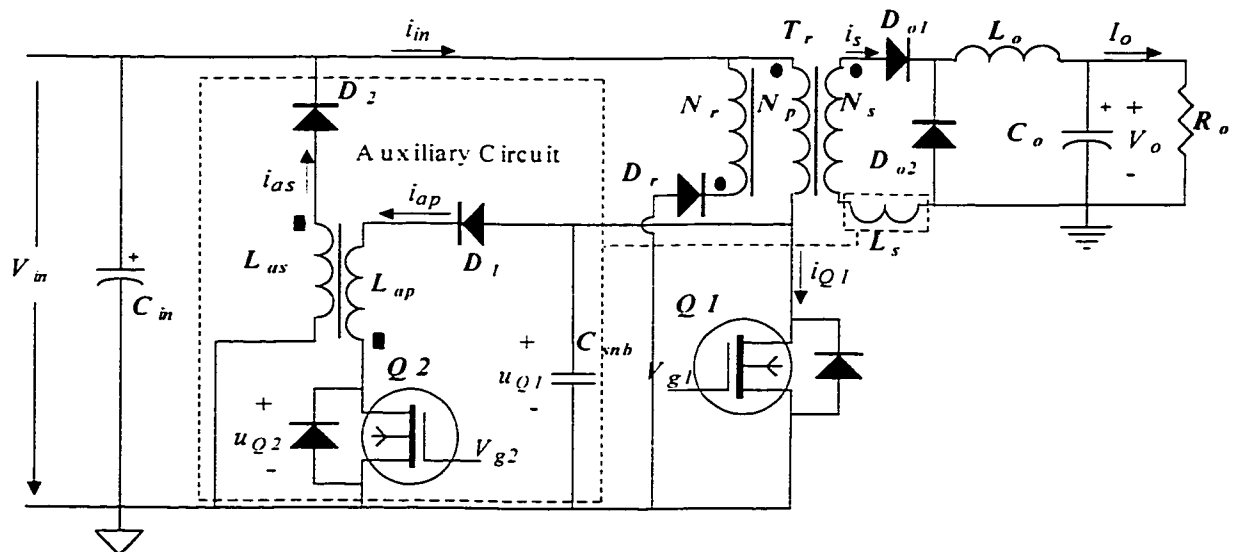


Fig. 3.1 The proposed ZVS forward converter topology.

In Fig. 3.1, the basic forward circuit is comprised of (i) the input capacitor C_{in} , (ii) the power transform T_r , which has three windings, the primary N_p , the secondary N_s , and the tertiary N_r that helps to reset the core, (iii) the main switch $Q1$, (iv) the rectifier D_{o1} and the freewheeling diode D_{o2} , (v) the output inductor L_o , (vi) the output capacitor C_o , (vii) the blocking diode D_r , and (viii) the load R_o .

The auxiliary circuit consists of (i) a snubber capacitor C_{snb} , which is in parallel with $Q1$, (ii) two coupled inductors L_{ap} and L_{as} , (iii) two blocking diodes D_1 and D_2 , (iv) an auxiliary switch $Q2$, and (v) a small inductor L_s , which is inserted into the secondary side of the power circuit.

3.3 MODES OF OPERATION

Fig. 3.2 shows key waveforms of the proposed converter of Fig. 3.1. The operation of the circuit can be divided into the following seven intervals. In a standard forward converter, there are no Intervals 1, 2 and 4. These intervals are fulfilled by the auxiliary circuit in order to achieve ZVS in $Q1$.

3.3.1 Interval 1 ($t_1 < t \leq t_2$)

Fig. 3.3(a). At the beginning of this interval, $Q2$ is switched ON. Thus C_{snb} , L_{ap} and L_s form a resonant tank, as show in Fig. 3.4. C_{snb} begins to discharge through L_{ap} and $Q2$. The discharging current rises resonantly and builds up a magnetic field in the core of L_{ap} . In this way the discharged energy from C_{snb} is transferred to the core. The voltage of C_{snb} drops to zero within this interval.

3.3.2 Interval 2 ($t_2 < t \leq t_3$)

Fig. 3.3(b). At the beginning of this interval, $Q1$ is switched ON under the zero voltage condition. At the same moment, $Q2$ is switched OFF, which stops the current in L_{ap} rapidly. The rapidly falling current reverses the voltage polarity at the dotted ends of the coupled inductors. Thus, D_{as} becomes forward biased and is forced to conduct, releasing the stored energy in the core of L_s .

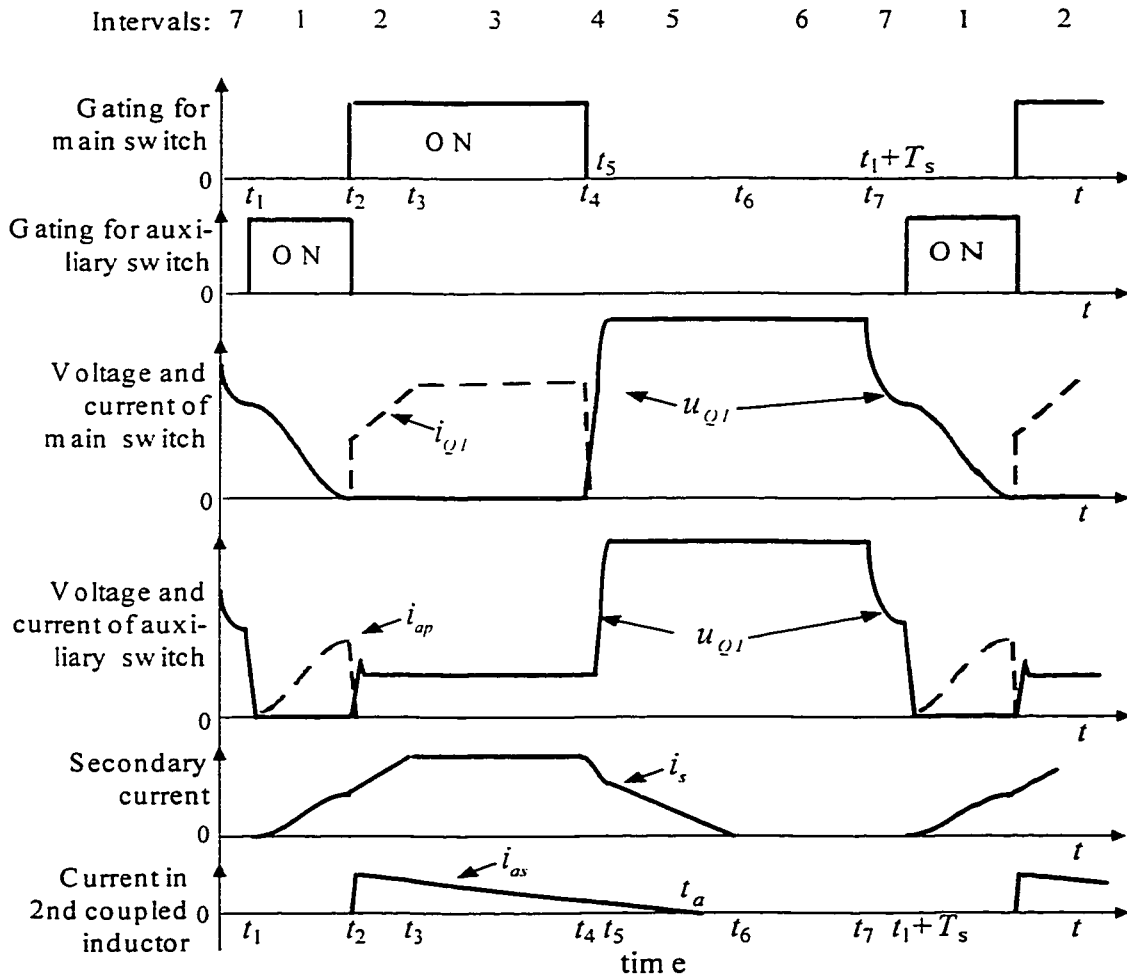


Fig. 3.2 Key waveforms of the proposed converter of Fig. 3.1. The converter operates in seven modes each switching cycle. Variables are defined in Fig. 3.1

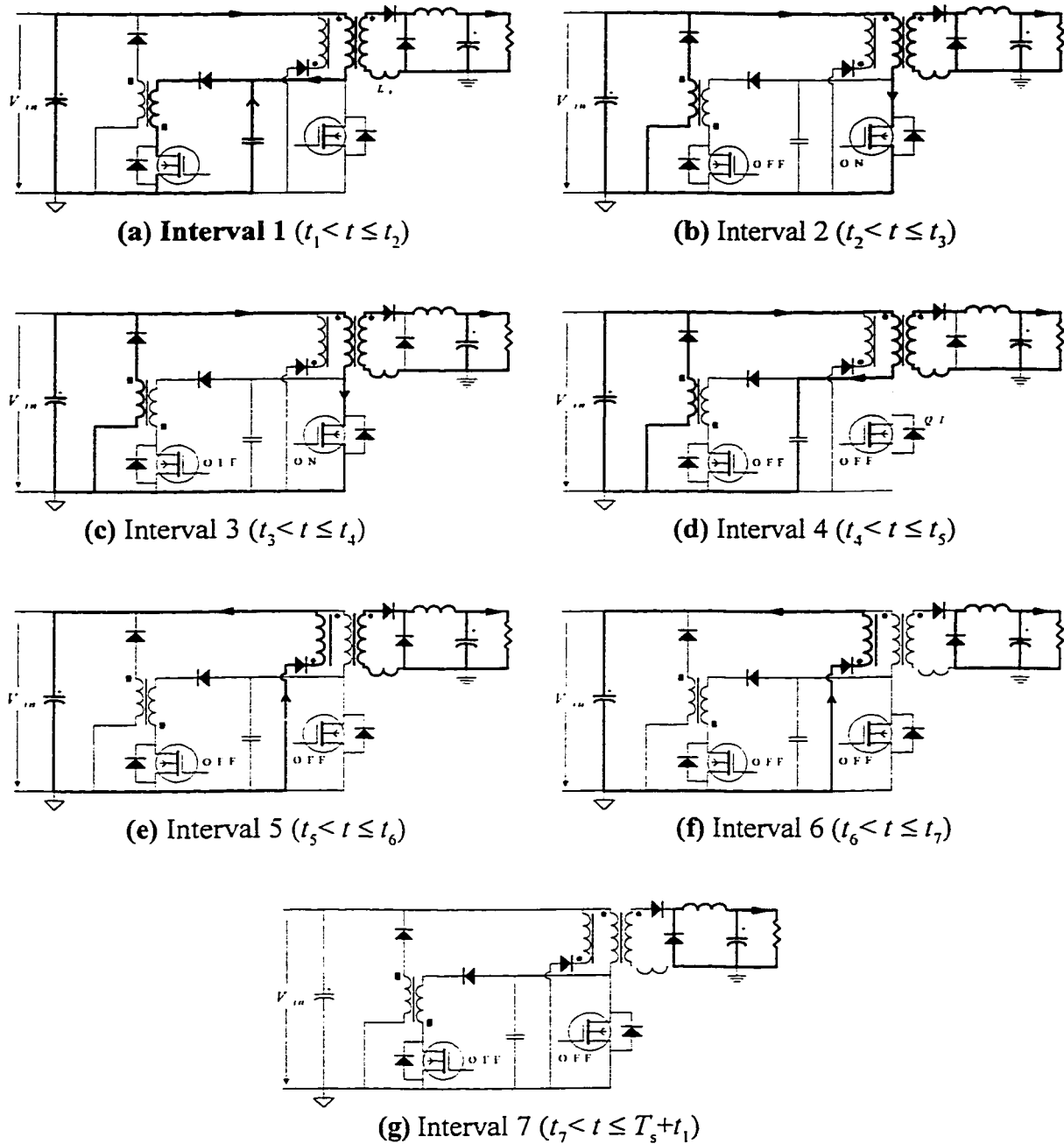


Fig. 3.3 Modes of operation of the converter of Fig. 3.1. The operation is divided into seven modes per switching cycle. The key waveforms are shown in Fig. 3.2.

The current in $Q1$ reflects the secondary current, which rises slowly owing to the existence of L_s . Both D_{o1} and D_{o2} are conducting to give the total current in L_o , with the current in D_{o1} rising and that in D_{o2} falling linearly.

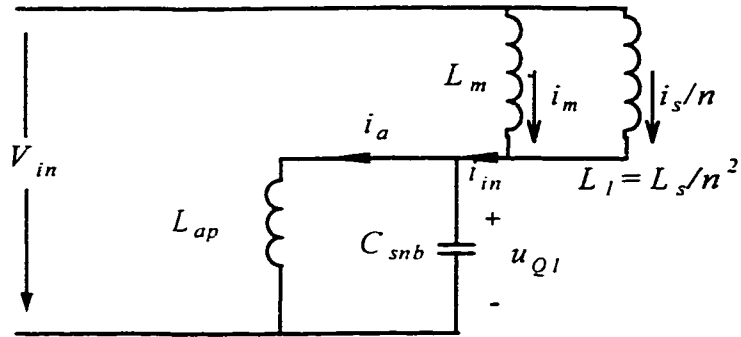


Fig. 3.4 The equivalent circuit of the discharging process in Interval 1. Variables are defined in Fig. 3.1.

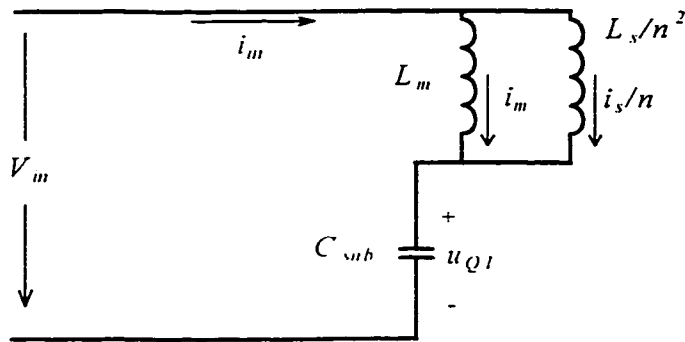


Fig. 3.5 The equivalent circuit of the charging process in Interval 5. The variables are defined in Fig. 3.1.

3.3.3 Interval 3 ($t_3 < t \leq t_4$)

Fig. 3.3(c). At the beginning of this interval, current in D_{o1} reaches the value of the current in L_{o1} , and current in D_{o2} falls to zero. Power is delivered to the load in the same manner as in the standard forward converter.

3.3.4 Interval 4 ($t_4 < t \leq t_5$)

Fig. 3.3(d). At the beginning of this interval, $Q1$ is switched OFF. The primary current charges C_{snb} . With a sufficient value of capacitance, C_{snb} can satisfactorily slow down the speed of rise of the drain voltage of $Q1$ so as to facilitate a ZVS turnoff in $Q1$.

Starting at the beginning of this interval, the current in D_{o1} decreases and D_{o2} is forced to conduct by L_o . L_s and C_{snb} forms a resonant tank shown in Fig. 3.5. The current in D_{o1} and that flowing into C_{snb} fall resonantly, and the drain voltage of $Q1$ rises resonantly. The current in D_{o2} rises accordingly.

3.3.5 Interval 5 ($t_5 < t \leq t_6$)

Fig. 3.3(e) shows the circuit operation during this interval. At the beginning of this interval, the drain of $Q1$ reaches a voltage of $2V_m$. D_r is forced to conduct. Thus, the voltage of the primary winding of T_r is clamped to a voltage of $-V_m$, and the drain voltage of $Q1$ is clamped to $2V_m$. In this way the core of T_r is reset. During this interval, L_s sees a clamped voltage and the current in D_{o1} falls linearly.

3.3.6 Interval 6 ($t_6 < t \leq t_7$)

Fig. 3.3(f) shows the circuit operation during this interval. At the beginning of this interval, the current in L_s exhaust, D_{o1} is reverse biased and D_{o2} freewheels the total inductor current in L_o . The voltage clamp action lasts until the current in D_r fall to zero at the end of this interval.

3.3.7 Interval 7 ($t_7 < t \leq T_s+t_1$)

Fig. 3.3(g) shows the circuit operation during this interval. At the beginning of this interval, the clamp action stops. C_{snb} and the magnetizing inductance L_m of T_r form a resonant loop. The drain voltage of $Q1$ starts to oscillate about the input dc line voltage V_m , starting from $2V_m$.

Following Interval 7, the process repeats from Intervals 1 through 7.

3.4 STEADY STATE ANALYSIS

The operating principle has been described in last section. In this section, the steady state analysis is performed with the assumptions made below. Based on the analysis, the time varying variables such as the current and voltage of the principal components and devices are determined, the performance of the converter is illustrated, and the resultant quantities such as the rms, average, or peak current and voltage of the components/devices are obtained. These quantities are used in designing the converter as presented in Chapter 5.

The analysis below uses a similar approach to that in analyzing the flyback converter in Section 2.4. Similarly, the initial conditions can be obtained by the previously mentioned iterative process.

3.4.1 Assumptions, Definitions and Initial Conditions

For convenience, the following assumptions are made:

(i) The steady state conditions have been established, and the converter is running at the nominal output voltage V_o and the static load conditions: P_o ,

(ii) Each component and device has ideal properties, that is,

(1) T_r : the leakage inductance is ignored, and the core does not saturate,

(2) L_{op}, L_{as} : the coupling factor is 1.0, and the core does not saturate,

(3) C_o, C_{sub} : pure capacitors, and the capacitance of C_o is infinitive,

(4) L_o : the inductance of L_o is infinitive,

(5) $D_1, D_2, D_{o1}, D_{o2}, D_r$: the forward voltage drop is 0 V, the recovery time is 0 s,

(6) $Q1, Q2$: the on resistances are 0 Ω , the inherent capacitances are 0 F.

The effects of the non-ideal properties of the components and devices are investigated in Section 2.5.1.

(iii) The magnetizing inductance of the transformer, L_m , is much larger than L_{ap} .

The following parameters are defined:

ω_n --angular frequency of the resonant tank of C_{snb} , L_{ap} and L_s (Interval 1),

ω_0 --angular frequency of the resonant tank of C_{snb} and L_m (Interval 7),

ω_r --angular frequency of the resonant tank of C_{snb} and L_s (Interval 4),

i_{ap} --instantaneous current in $Q2$,

I_{ap} --peak current in $Q2$,

i_{as} --instantaneous current in L_{as} ,

I_{as} --peak current in L_{as} ,

i_{in} --instantaneous input current,

I_{mpeak} --peak magnetizing current in T_r ,

I_o --output current,

i_{Q1} --instantaneous current in $Q1$,

i_s --instantaneous secondary current,

I_s --peak secondary current,

k --factor by which V_o deviates from V_m ,

L_1 --reflected value of L_s seen from the primary side of T_r ,

L_m --magnetizing inductance of T_r ,

L_r --effective inductance of paralleling L_1 and L_m ,

n --reciprocal of turns ratio of T_r , equal to N_s/N_p ,

V_o --output voltage,

$V_{p,Q1}$ --clamped voltage stress of $Q1$ when it is OFF,

$V_{p,Q2}$ --clamped OFF voltage of $Q2$ when it is OFF,

u_{Q1} --instantaneous drain voltage of $Q1$, or voltage across C_{sub} ,

V_0 --initial drain voltage of $Q1$ per switching cycle.

According to the definitions and basic circuit theory,

$$L_1 = \frac{1}{n^2} L_{v1} \quad (3-1)$$

$$L_r = \frac{L_m L_1}{L_m + L_1} \approx L_1 \quad (3-2)$$

$$\omega_n = \sqrt{\frac{1}{C_{sub}} \cdot \frac{L_{ap} + L_r}{L_{ap} L_r}} \quad (3-3)$$

$$\omega_r = 1/\sqrt{L_r C_{sub}} \quad (3-4)$$

$$\omega_0 = 1/\sqrt{L_m C_{sub}} \quad (3-5)$$

The analysis begins by stating the initial conditions of Interval 1:

(i) Both $Q1$ and $Q2$ are OFF, and the drain voltage of the paralleled switches $Q1$ and $Q2$ is V_0 ,

$$u_{Q1}(t_1) = u_{Q2}(t_1) = V_0 = (1+k)V_m \quad (3-6)$$

where k is the factor by which V_0 deviates from V_m , and

$$i_{Q1}(t_1) = i_{ap}(t_1) = 0 \quad (3-7)$$

(ii) The magnetizing inductor L_m and C_{snb} undergoes a resonance in the end of last switching cycle, but the resonant current in L_m is negligible,

$$i_m(t_1) = 0 \quad (3-8)$$

(iii) D_2 , D_{o1} and D_r are reverse biased, and D_{o2} freewheels the total output current,

$$i_{as}(t_1) = i_s(t_1) = 0 \quad (3-9)$$

3.4.2 Interval 1 ($t_1 < t \leq t_2$)

This interval starts at $t = t_1$. $Q2$ is turned on and a resonant tank shown in Fig. 3.4 is formed. The resonance process obeys the following equations:

$$L_r \frac{di_m}{dt} + u_{Q1} = V_m \quad (3-10)$$

$$u_{Q1} = L_{ap} \frac{di_{ap}}{dt} \quad (3-11)$$

$$i_{ap} + C_{snb} \frac{du_{Q1}}{dt} = i_m \quad (3-12)$$

Combining Eqs. (3-10) through (3-12),

$$\frac{d^2 u_{Q1}}{dt^2} + \frac{1}{C_{snb}} \cdot \frac{L_{ap} + L_r}{L_{ap} L_r} u_{Q1} = \frac{1}{C_{snb} L_r} V_m \quad (3-13)$$

Giving the initial conditions determined by Eqs. (3-6) through (3-8), the solution of Eq. (3-13) is

$$u_{Q1}(t) = \frac{L_{ap}}{L_{ap} + L_r} V_m + \left(\frac{L_r}{L_{ap} + L_r} + k \right) V_m \cos[\omega_n(t - t_1)] \quad (3-14)$$

Eq. (3-14) indicates that, if L_s were absent from the circuit of Fig. 3.1, namely $L_r = 0$, u_{Q1} could never reach zero. Under this condition, no ZVS would be achieved. To solve this problem, L_s is hence introduced.

It can be extended from Eq. (3-14) that, if there exists a relation

$$L_r = \frac{1-k}{1+k} L_{ap} \quad (3-15)$$

u_{Q1} will always reach zero when the first half of the resonant process finishes. But it is impossible to satisfy Eq. (3-15) over all the operating range, because k is not a fixed parameter and it is determined by the line and load conditions. For simplicity in design, let

$$L_r = L_{ap} \quad (3-16)$$

and set the duration of this interval to be a half of the resonant period. Thus, if the condition $k > 0$ is always valid, u_{Q1} will always reach zero within this duration and is automatically clamped at zero by latching in of the body diode of $Q1$ in the rest of this interval. It will be shown in Section 3.4.8 that this condition can be reached by selecting a large L_m .

Referring to Eqs. (3-1) and (3-2), Eq. (3-16) can be satisfied by selecting the value of L_s as given by

$$L_s = n^2 \frac{L_m L_{ap}}{L_m - L_{ap}} \approx n^2 L_{ap} \quad (3-17)$$

Thus, Eq. (3-14) can be rewritten as

$$u_{Q1}(t) = \frac{1}{2}V_m + \left(\frac{1}{2} + k\right)V_m \cos[\omega_n(t - t_1)] \quad (3-18)$$

From Eqs. (3-11), (3-10), (3-18) and the initial conditions (3-7) and (3-8), the following variables can be determined as

$$i_{ap}(t) = \frac{V_m}{2L_{ap}}(t - t_1) + \left(\frac{1}{2} + k\right)\frac{V_m}{\omega_n L_{ap}} \sin[\omega_n(t - t_1)] \quad (3-19)$$

$$i_m(t) = \frac{V_m}{2L_{ap}}(t - t_1) + \left(\frac{1}{2} + k\right)\left(\frac{1}{\omega_n L_{ap}} - \omega_n C_{sub}\right)V_m \sin[\omega_n(t - t_1)] \quad (3-20)$$

Refer to Fig. 3.4, the magnetizing and the secondary currents of the transformer can be determined, respectively, by

$$i_s(t) = \frac{1}{n} \cdot \frac{L_m}{L_m + L_1} i_m(t) \quad (3-21)$$

$$i_m(t) = \frac{L_1}{L_m + L_1} i_m(t) \quad (3-22)$$

Since D_2 is reverse biased and $Q1$ is OFF,

$$i_{as}(t) = i_{Q1}(t) = 0 \quad (3-23)$$

As explained previously, at the end of this interval,

$$u_{Q1}(t_2) = 0 \quad (3-24)$$

Thus, the ZVS condition for turning on of $Q1$ is established.

The final value of each variable in Interval 1 defines the initial conditions of Interval 2. For convenience in the following analysis, let

$$I_{ap} = i_{ap}(t_2) = \frac{V_m}{2L_{ap}}(t_2 - t_1) \quad (3-25)$$

$$I_{s1} = i_s(t_2) = \frac{1}{n} \cdot \frac{L_m}{L_m + L_{ap}} \cdot \frac{V_m}{2L_{ap}} (t_2 - t_1) \approx \frac{1}{n} \cdot \frac{V_m}{2L_{ap}} (t_2 - t_1) \quad (3-26)$$

$$I_1 = i_m(t_2) \quad (3-27)$$

$$I_{m1} = i_m(t_2) \quad (3-28)$$

3.4.3 Interval 2 ($t_2 < t \leq t_3$)

This interval starts at $t = t_2$. Similarly to Section 2.4.3, it can be determined that

$$I_{as} = I_{ap} \sqrt{L_{ap} / L_{as}} \quad (3-29)$$

$$i_{as}(t) = I_{as} - \frac{V_m}{L_{as}} (t - t_2) \quad (3-30)$$

From Eq. (3-30), the duration when i_{as} flows is determined by

$$t_a - t_2 = \frac{L_{as}}{V_m} I_{as} \quad (3-31)$$

During $(t_a - t_2)$, u_{Q2} will be clamped at a voltage the same as given by Eq. (2-25).

As L_s sees a constant voltage nV_m , the secondary current rises linearly

$$i_s(t) = \frac{nV_m}{L_s} (t - t_2) + I_{s1} \quad (3-32)$$

As L_m sees a constant voltage V_m , thus,

$$i_m(t) = \frac{V_m}{L_m} (t - t_2) + I_{m1} \quad (3-33)$$

Hence the primary current is

$$i_m(t) = i_{Q1}(t) = i_m(t) + ni_s(t) \approx \frac{n^2 V_m}{L_s} (t - t_2) + I_{s1} \quad (3-34)$$

As $Q2$ is off and $Q1$ is on,

$$i_{op}(t) = 0 \quad (3-35)$$

$$u_{Q1}(t) = 0 \quad (3-36)$$

At the end of this interval, the secondary current reaches the value of the output current I_o

$$i_s(t_3) = I_o \quad (3-37)$$

Hence, from Eqs. (3-32) and (2-37), the duration of this interval can be determined as

$$t_3 - t_2 = (I_o - I_{s1}) \frac{L_s}{nV_m} \quad (3-38)$$

If $I_o < I_{s1}$, which is a case under the light load conditions, Interval 2 will not exist. It is because the secondary current has reached I_o in Interval 1. Thus, D_{o2} is reverse biased and the total output current flows through D_{o1} . Under such conditions, the operation directly enters Interval 3 from Interval 1.

The final value of each variable in Interval 2 defines the initial conditions of Interval 3.

3.4.4 Interval 3 ($t_3 < t \leq t_4$)

This interval starts at $t = t_3$. In this interval, the operation of the circuit is the same as the standard forward converter: L_m sees a constant voltage V_m , i_s is commanded by L_o to be constant at I_o , and the total input current flows through $Q1$. Therefore, the following equations govern the respective variables during this interval.

$$i_m(t) = \frac{V_m}{L_m}(t - t_2) + I_{m1} \quad (3-39)$$

$$i_s(t) = I_o \quad (3-40)$$

$$i_{Q1}(t) = i_m(t) = ni_s(t) + i_m(t) \approx nI_o \quad (3-41)$$

$$i_{ap}(t) = 0 \quad (3-42)$$

$$u_{Q1}(t) = 0 \quad (3-43)$$

The final value of each variable in Interval 3 defines the initial conditions of Interval 4. For convenience in the following analysis, let

$$I_{m2} = i_m(t_4) \quad (3-44)$$

3.4.5 Interval 4 ($t_4 < t \leq t_5$)

This interval starts at $t = t_4$. $Q1$ is turned OFF at the beginning of this interval. C_{sub} is charged and the equivalent circuit is shown in Fig. 3.5. Thus, u_{Q1} is governed by the following differential equation,

$$\frac{d^2 u_{Q1}}{dt^2} + \frac{1}{C_{sub} L_r} u_{Q1} = \frac{1}{C_{sub} L_r} V_m \quad (3-45)$$

Giving the initial conditions determined by Eqs. (3-41) and (3-43), it is found that

$$u_{Q1}(t) = V_m - V_m \cos[\omega_r(t - t_4)] + \frac{nI_o}{\omega_r C_{sub}} \sin[\omega_r(t - t_4)] \quad (3-46)$$

As L_m sees a voltage $(V_m - u_{Q1})$ and L_s sees a voltage $n(V_m - u_{Q1})$, thus,

$$i_m(t) = \frac{L_1}{L_m + L_1} \left\{ \omega_r C_{sub} V_m \sin[\omega_r(t - t_4)] + nI_o \cos[\omega_r(t - t_4)] \right\} \quad (3-47)$$

$$i_s(t) = \frac{1}{n} \cdot \frac{L_m}{L_m + L_1} \left\{ \omega_r C_{sub} V_m \sin[\omega_r(t - t_4)] + nI_o \cos[\omega_r(t - t_4)] \right\} \quad (3-48)$$

And the input current is

$$i_m(t) = C_{sub} \frac{du_{Q1}(t)}{dt} = \omega_r C_{sub} V_m \sin[\omega_r(t - t_4)] + nI_o \cos[\omega_r(t - t_4)] \quad (3-49)$$

As both $Q1$ and $Q2$ are OFF,

$$i_{Q1}(t) = i_{op}(t) = 0 \quad (3-50)$$

At the end of this interval, u_{Q1} reaches $2V_m$, i.e.,

$$u_{Q1}(t_5) = 2V_m \quad (3-51)$$

Then L_m sees a negative voltage $-V_m$ and D_r becomes forward biased and starts to conduct, clamping u_{Q1} at $2V_m$.

The final value of each variable in Interval 4 defines the initial conditions of Interval 5. For convenience in the following analysis, let

$$I_{s2} = i_s(t_5) \quad (3-52)$$

$$I_{m3} = i_m(t_5) \quad (3-53)$$

3.4.6 Interval 5 ($t_5 < t \leq t_6$)

This interval starts at $t = t_5$. The core of T_r is reset as D_r conducts. L_m sees a constant voltage $-V_m$, and L_s sees a constant voltage $-nV_m$. Thus,

$$i_m(t) = I_{m3} - \frac{V_m}{L_m}(t - t_5) \quad (3-54)$$

$$i_s(t) = I_{s2} - \frac{nV_m}{L_s}(t - t_5) \quad (3-55)$$

As D_r conducts, the tertiary current which consists of i_m and the reflected secondary

current flows into the dc line,

$$i_m(t) = -i_m(t) - ni_s(t) \quad (3-56)$$

As both $Q1$ and $Q2$ are OFF and u_{Q1} is clamped, therefore

$$i_{Q1}(t) = i_{op}(t) = 0 \quad (3-57)$$

$$u_{Q1}(t) = 2V_m \quad (3-58)$$

At the end of this interval, i_s reaches zero

$$i_s(t_6) = 0 \quad (3-59)$$

Thus, D_{o1} becomes reverse biased again and D_{o2} freewheels the total output current I_o .

From Eqs. (3-55) and (3-59), the duration of this interval is determined by

$$(t_6 - t_5) = \frac{I_{s2}L_s}{nV_m} \quad (3-60)$$

The final value of each variable in Interval 5 defines the initial conditions of Interval 6.

3.4.7 Interval 6 ($t_6 < t \leq t_7$)

This interval starts at $t = t_6$. The resetting of the core continues. If the resetting finishes in Interval 5, this interval will be skipped and the operation enters directly into Interval 7 from Interval 5.

As L_m sees a constant voltage $-V_m$, and u_{Q1} is still clamped,

$$i_m(t) = I_{m3} - \frac{V_m}{L_m}(t - t_5) \quad (3-61)$$

$$u_{Q1}(t) = 2V_m \quad (3-62)$$

The tertiary current consisting of i_m flows into the dc line,

$$i_m(t) = -i_m(t) \quad (3-63)$$

As D_{o1} is reverse biased and $Q1$ and $Q2$ are both OFF,

$$i_s(t) = i_{Q1}(t) = i_{ap}(t) = 0 \quad (3-64)$$

At the end of this interval, i_m falls to zero, finishing the resetting

$$i_m(t_7) = 0 \quad (3-65)$$

D_r becomes reverse biased again. From Eqs. (3-61) and (3-65), the duration of this interval is determined by

$$t_7 - t_6 = (t_7 - t_5) - (t_6 - t_5) = \frac{I_{m3}L_m}{V_m} - \frac{I_{s2}L_s}{nV_m} \quad (3-66)$$

The final value of each variable in Interval 6 defines the initial conditions of Interval 7.

3.4.8 Interval 7 ($t_7 < t \leq t_8$)

This interval starts at $t = t_7$. C_{snb} and L_m undergo a resonance owing to the difference between u_{Q1} and the input dc line voltage V_m . Similarly to Section 2.4.6,

$$u_{Q1}(t) = V_m \{1 + \cos[\omega_0(t - t_7)]\} \quad (3-67)$$

$$i_m(t) = i_m(t) = C_{snb} \frac{du_{Q1}}{dt} = -\omega_0 C_{snb} V_m \sin[\omega_0(t - t_7)] \quad (3-68)$$

Substituting Eq. (3-5) into (3-68),

$$i_m(t) = i_m(t) = -\sqrt{\frac{C_{snb}}{L_m}} V_m \sin[\omega_0(t - t_7)] \quad (3-69)$$

Owing to the large value of L_m , i_m can be ignored and regarded as 0. This is consistent with assumption (ii) in Section 3.4.1 (Eq. (3-8)). As D_{o1} is reverse biased and both $Q1$ and $Q2$ are OFF, thus

$$i_{ap}(t) = i_{Q1}(t) = i_s(t) = 0 \quad (3-70)$$

$$i_m(t) = i_m(t) \approx 0 \quad (3-71)$$

At the end of this interval, one switching cycle finishes. As in the steady state operation, u_{Q1} reaches V_0 . Referring to Eqs. (3-6) and (3-67), the factor by which the steady state initial drain voltage of $Q1$ deviates from V_m is determined by

$$k = \cos[\omega_0(T_s + t_1 - t_7)] \quad (3-72)$$

Selecting a large L_m will result in a small ω_0 (for example, let $\omega_0 T_s < \pi$) and hence $k > 0$ so as to achieve ZVS over all the line/load range (refer to Section 3.4.2).

The final value of each variable in Interval 7 defines the initial conditions of Interval 1 in the next switching cycle, which repeats the same process as in this cycle.

3.5 PERFORMANCE

3.5.1 Effects of the Non-Ideal Components/Devices

Each realistic component and devices has some non-ideal properties as mentioned in Section 2.5.1. For the same reasons as explained in Section 2.5.1, the non-ideal properties will not make a significant deviation from the operation of the circuit discussed above.

A similar process to that in Section 2.5.1 can be followed to determine the effects of the leakage inductances, and it will not be repeated here.

3.5.2 Determination of Duty Cycle as to Regulate the Output Voltage

Refer to Fig. 3.3. In one switching cycle, L_o sees a constant voltage $nV_m - V_o$ for a duration of $(D - D_x)T_s$, where D is the duty cycle of the main switch $Q1$ and D_x is the reduction of the effectual duty cycle owing to L_s , which is given by

$$D_x = (t_3 - t_2) f_s \quad (3-73)$$

and L_o sees another constant voltage $-V_o$ for the rest of the cycle, thus, the volt-second balance of L_o gives the following equation:

$$(D - D_x)(nV_m - V_o) - (1 - D - D_x)V_o = 0 \quad (3-74)$$

which yields

$$(D - D_x)nV_m = V_o \quad (3-75)$$

Assuming the output power is P_o , thus

$$I_o = \frac{P_o}{V_o} \quad (3-76)$$

Substituting Eq. (3-38) into (3-37), and substituting (3-26) and (3-76) into the result

$$D_x = (I_o - I_{s1}) \frac{L_s}{nV_m} f_s = \left[\frac{P_o}{V_o} - \frac{V_m}{2nL_{ap}}(t_2 - t_1) \right] \frac{L_s}{nV_m} f_s \quad (3-77)$$

Let D_{aux} represent the duty cycle of the auxiliary switch $Q2$,

$$D_{aux} = (t_2 - t_1) f_s \quad (3-78)$$

Getting $(t_2 - t_1)$ from Eq. (3-78) and substituting the result and Eq. (3-17) into (3-77), it yields

$$D_x = \left(I_o - \frac{V_{in}}{2nf_s L_{ap}} D_{aux} \right) \frac{L_s}{nV_{in}} f_s = \frac{f_s L_s P_o}{nV_{in} V_o} - \frac{1}{2} D_{aux} \quad (3-79)$$

Eq. (3-75) indicates that, in order to regulate the output voltage at certain line/load conditions, the duty cycle of the main switch should be

$$D = \frac{V_o}{nV_{in}} + D_x = \frac{V_o}{nV_{in}} + \frac{f_s L_s P_o}{nV_{in} V_o} - \frac{1}{2} D_{aux} \quad (3-80)$$

3.5.3 Advantages and Disadvantages of the Proposed Converter

The following major advantages of the proposed converter can be identified from the above analysis.

- (i) No need for an isolated gate drive for the auxiliary switch, because $Q2$ and $Q1$ have a common source connection (refer to Fig. 3.1).
- (ii) Generating the gate drive signal is simple, because the on time of $Q2$, unlike in the case of the active clamp topology, is fixed at a half of the resonance period of the L_T - L_{ap} - C_{snb} tank (refer to Section 3.4.2)
- (iii) The ZVS turn-on transient of $Q1$, facilitated by Intervals 1, is not affected by the line and load conditions. The turn-off transient of $Q1$ is affected by the load current I_o as shown in Eq. (3-47). With a sufficient value of capacitance, C_{snb} will guarantee a ZVS turnoff in $Q1$ under the full load condition. Under light load, the rise of u_{Q1} will be slower. Hence, ZVS will always be achieved regardless of the line/load conditions.

- (iv) Less EMI is generated owing to that C_{snb} slows down speed of change of the inductor current and capacitor voltage, as indicated by Eqs. (3-46) and (3-47).
- (v) It is simple in circuitry, and all components of the auxiliary circuit require small power ratings.
- (vi) Conduction losses are not increased. Because C_{snb} is always there to slow down the voltage rise speed and to lower $Q1$'s voltage stress. Unlike in the existing techniques where extra circulating power is need by the clamp circuit, the auxiliary circuit does not draw extra power.

The disadvantage of the proposed topology is that the auxiliary switch has a hard switching turnoff. But the switching losses in $Q2$ can be minimized by selecting a MOSFET through trading off between the least ON resistance and the least inherent capacitance, and also by increasing the ratio of L_{an} to L_{ap} , which lowers the voltage stress on $Q2$ at turnoff.

3.5.4 RMS or Average Current Values

In the design, the rms, average or peak current and voltage are required to determine the rating requirements in selecting the components. Some of these values have been obtained in the analysis. Other values are calculated below.

(1) RMS current in $Q1$

The current in $Q1$ can be approximated with a square waveform (Fig. 3.2), thus,

$$I_{RMS_Q1} = \sqrt{f \int_{t_1}^{t_1+T} i_{Q1}^2(t) dt} \approx \sqrt{Dn} I_o = \sqrt{D} \frac{nP_o}{V_o} \quad (3-85)$$

For a conversion efficiency less than 1, say η , the RMS current becomes

$$I_{RMS_Q1} = \sqrt{D} \frac{nP_o}{\eta V_o} \quad (3-86)$$

(2) RMS current in $Q2$

The current in $Q2$ consists of two components, one is in a triangle waveform, the other is a half period of a sinusoidal waveform, as given by Eq. (3-19). Thus,

$$I_{RMS_Q2} = \sqrt{f_s \int_{t_1}^{t_1+T_s} i_{ap}^2(t) dt} = \frac{V_m}{L_{ap}} \sqrt{\frac{D_{aux}^3}{12 f_s^2} + \frac{9 D_{aux}}{16 \omega_n^2}} \quad (3-87)$$

The average current is found to be

$$I_{av_Q2} = \frac{V_m}{4 f_s L_{ap}} D_{aux}^2 + \frac{3V_m}{\sqrt{2} \pi \omega_n L_{ap}} D_{aux} \quad (3-88)$$

(3) Average current in D_2

The current in D_2 is triangular. From Eqs. (3-22), (3-26) and (3-28), it is found that the average current in D_2 is given by

$$I_{av_D2} = \frac{V_m}{8 f_s L_{ap}} \cdot D_{aux}^2 \quad (3-89)$$

(4) Average currents in D_{o1} and D_{o2}

The current in D_{o1} is of a complex waveform. The average current in D_o can be calculated as

$$I_{av_Do1} = \sqrt{f_s \int_{t_1}^{t_1+T_s} i_s^2(t) dt} \approx \frac{P_o}{V_o} D \quad (3-90)$$

and the average current in D_{o2} is determined by

$$I_{av_Do2} = I_o - I_{av_Do1} \approx \frac{P_o}{V_o} (1 - D) \quad (3-91)$$

3.5.5 Losses Caused by the Auxiliary Circuit

(1) Switching losses in $Q2$: P_{s_Q2}

It is found that

$$P_{s_Q2} = \frac{1}{2} C_{oss_Q2} V_0^2 f_s + \frac{1}{3} I_{ap} V_{in} \sqrt{L_{ap}/L_{as}} t_{off_Q2} f_s \quad (3-92)$$

where C_{oss_Q2} is the output capacitance of $Q2$, and

t_{off_Q2} is the OFF transient time of $Q2$.

(2) Conduction losses in $Q2$: P_{C_Q2}

The losses is found to be

$$P_{C_Q2} = I_{RMS_Q2}^2 R_{D_Q2} \quad (3-93)$$

where R_{D_Q2} is the ON resistance of $Q2$.

(3) Conduction losses in D_1 and D_2 : $P_{C_D1\&2}$

The conduction losses in D_1 and D_2 are found to be

$$P_{C_D1\&2} = V_{F_D1} I_{av_Q2} + V_{F_D2} I_{av_D2} \quad (3-94)$$

where V_{F_D1} is the forward voltage drop of D_1 , and

V_{F_D2} is the forward voltage drop of D_2 .

(4) Total losses by the auxiliary circuit

$$P_{I_a} = P_{s_Q2} + P_{C_Q2} + P_{C_D1\&2} \quad (3-95)$$

3.5.6 Losses Removed due to ZVS Operation

(1) Switching losses in $Q1$ in a hard switching operation: P_{s_Q1}

The hard switching will cause a switching losses in $Q1$ as given by

$$P_{s_Q1} = \frac{1}{2} C_{oss_Q1} V_0^2 f_s + \frac{2}{3} n I_o V_{in} t_{off_Q1} f_s \quad (3-96)$$

where t_{off_Q1} is the OFF transient time of $Q1$, and

C_{oss_Q1} is the output capacitance of $Q1$.

(2) Net saving of power due to the ZVS operation

The net saving of the power due to the ZVS operation of the proposed converter is approximately

$$\Delta P = P_{s_Q1} - P_{l_Q2} \quad (3-97)$$

3.6 EXPERIMENTAL RESULTS

3.6.1 Experiment Setup

A prototype ZVS forward converter is built based on the design presented in Chapter 5. Since the circuit outputs a power of 100 W at an output voltage of 5 V, synchronous rectifiers are chosen in the output rectification stage of the circuit so as to reduce the losses in the stage. An improved self-driven gate drive technique for synchronous rectifier in the forward converter [18] is used to optimize the performance of the synchronous rectifiers. The schematic of the prototype converter is shown in Fig. II.2 in Appendix II.

The operating conditions of the circuit are summarized as follows: (i) the input dc line voltage varies from 40 V to 60 V, (ii) the full load is 100 W at a output voltage of 5 V, and (iii) the switching frequency is 300 kHz.

3.6.2 Key Waveforms

Fig. 3.6 shows the theoretical waveforms, which are drawn in MathCAD based on the equations of u_{Q1} and i_{Q1} obtained in the steady state analysis in Section 3.5. Fig. 3.7 shows experimental results of the waveforms of drain voltage and current of $Q1$ in the prototype converter. These two figures are under the same operating conditions: $V_{in}=50V$, $P_o=100W$. The comparison between the theoretical and experimental results is made in Table 3.1. It is seen that they are in good agreement.

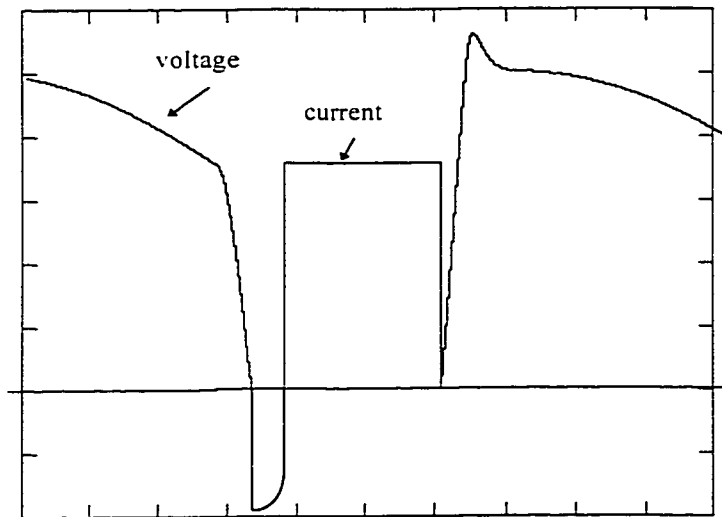


Fig. 3.6 The drain voltage and current waveforms of $Q1$ in Fig. 3.1, which are predicted by the steady state analysis made above. The negative drain current is due to the latching of the body diode of $Q1$ before it is turned on
Vertical: 2A/div., 20V/div., Horizontal: 0.5 μ s/div.

Table 3.1 Comparison between the theoretical and experimental results of the current, voltage and duty cycle of the main switch
($V_{in}=50V$, $P_o=100W$, $f_s=300kHz$)

	D	Vpeak	V0	Ipeak
Theoretical	0.29	115V	71.0V	6.67A
Experimental	0.31	118V	77.0V	6.80A

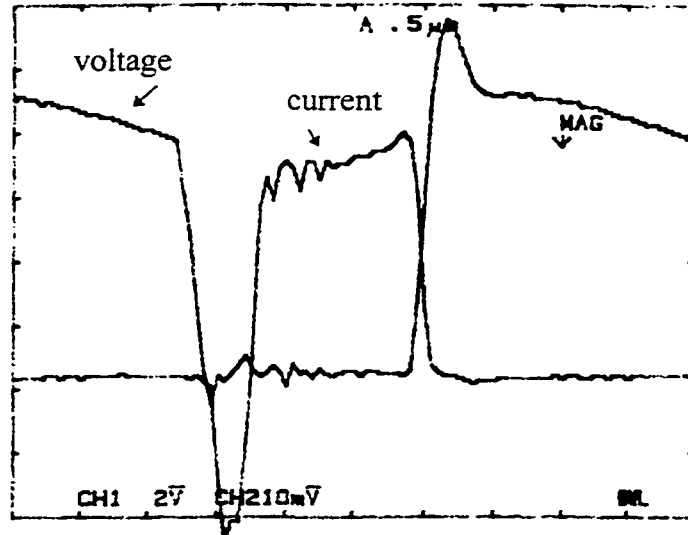


Fig. 3.7 The experimental results of the drain voltage and current of $Q1$ in a prototype ZVS converter of Fig. 3.1. The theoretical waveform is shown in Fig. 3.6
Vertical: 2A/div., 20V/div., Horizontal: 0.5 μ s/div.

Fig. 3.8 shows the theoretical waveforms of u_{Q2} and i_{Q1} based on the steady state analysis in Section 3.4 and 3.5. Fig. 3.8 is drawn with the software MathCAD. Fig. 3.9 shows experimental results of the waveforms of drain voltage and current of $Q2$ in the prototype ZVS converter of Fig. 3.2. These two figures are under the same operating conditions: $V_{in}=50V$, $P_o=100W$. The comparison between the theoretical and experimental results is made in Table 3.2. It is seen that they are in good agreement.

Table 3.2 Comparison between the theoretical and experimental results of the current, voltage and duty cycle of the auxiliary switch
($V_{in}=50V$, $P_o=100W$, $f_s=300kHz$)

	V_{peak}	V_{off}	I_{peak}
Theoretical	115V	9.12V	3.56A
Experimental	118V	8.80V	3.30A

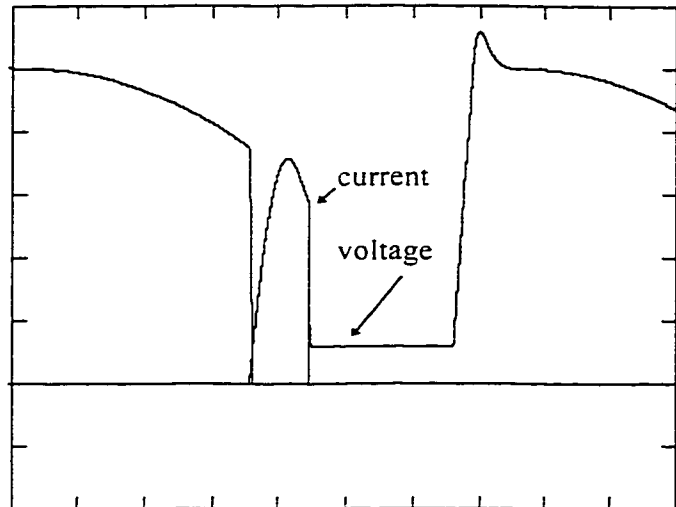


Fig. 3.8 The drain voltage and current waveforms of Q_2 in Fig. 3.1, which are predicted by the steady state analysis made above.
Vertical: 1A/div., 20V/div., Horizontal: 0.5 μ s/div.

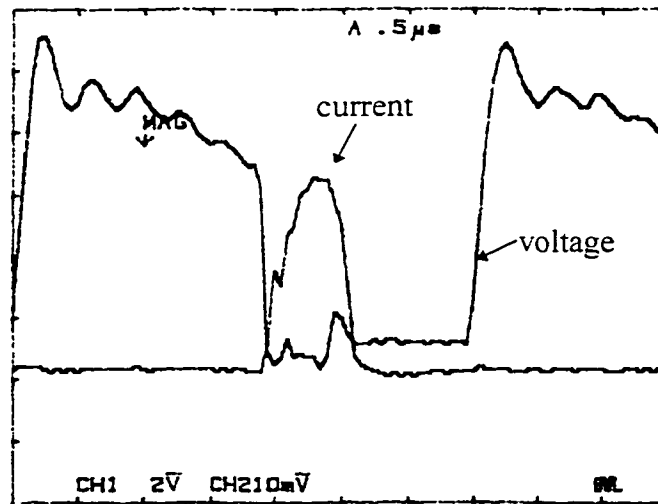


Fig. 3.9 The Experimental results of the drain voltage and current waveforms of Q_2 in Fig. 3.1. The theoretical waveform is shown in Fig. 3.8.
Vertical: 1A/div., 20V/div., Horizontal: 0.5 μ s/div.

Figs. 3.10 through 3.16 show the current and voltage waveforms of the main and auxiliary switches at different line/load conditions, verifying the analysis in that ZVS is always achieved in the main switch.

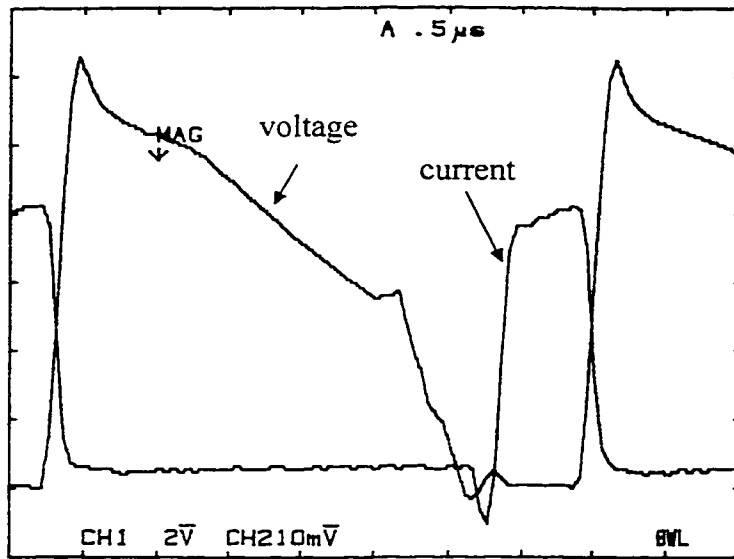


Fig. 3.10 Experimental results: the current and voltage of $Q1$ at high line full load. $P_o=100\text{W}$, $V_m=60\text{V}$, $f_s=300\text{kHz}$. Scales: vertical-- 20V/div. , 2A/div. ; horizontal-- $0.5\mu\text{s/div.}$

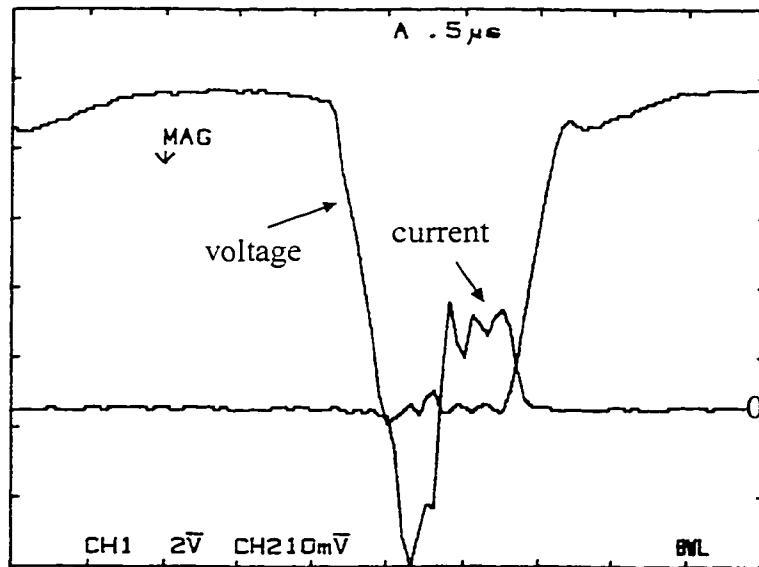


Fig. 3.11 Experimental results: the current and voltage of $Q1$ at high line light load. $P_o=20\text{W}$, $V_m=60\text{V}$, $f_s=300\text{kHz}$. Scales: vertical-- 20V/div. , 2A/div. ; horizontal-- $0.5\mu\text{s/div.}$

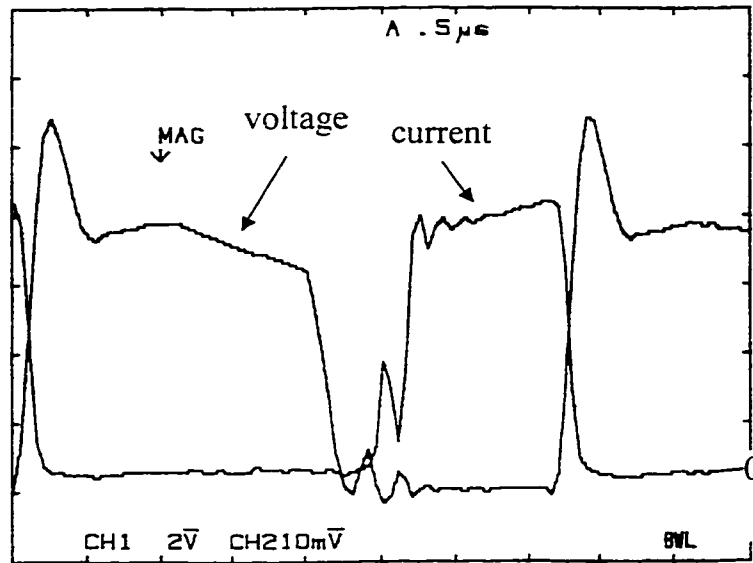


Fig. 3.12 Experimental results: the current and voltage of QI at low line full load.
 $P_o=100\text{W}$, $V_m=40\text{V}$, $f_s=300\text{kHz}$.
 Scales: vertical-- 20V/div. , 2A/div. ; horizontal-- $0.5\mu\text{s/div.}$

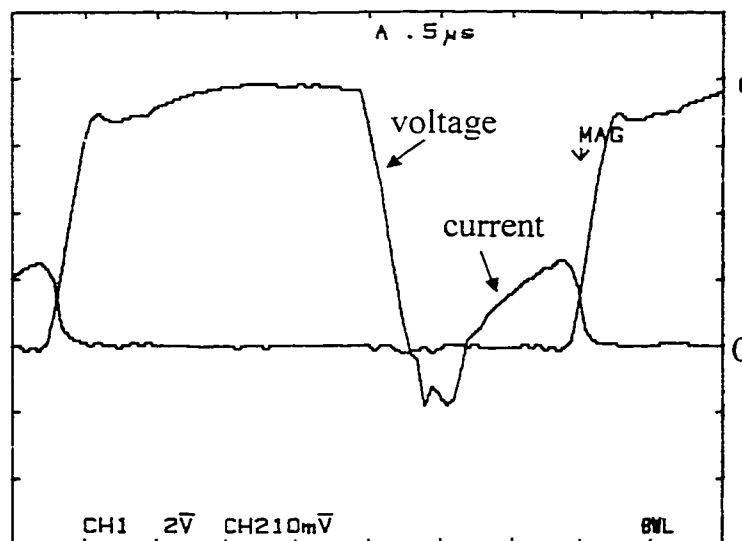


Fig. 3.13 Experimental results: the current and voltage of QI at low line light load.
 $P_o=20\text{W}$, $V_m=40\text{V}$, $f_s=300\text{kHz}$.
 Scales: vertical-- 20V/div. , 2A/div. ; horizontal-- $0.5\mu\text{s/div.}$

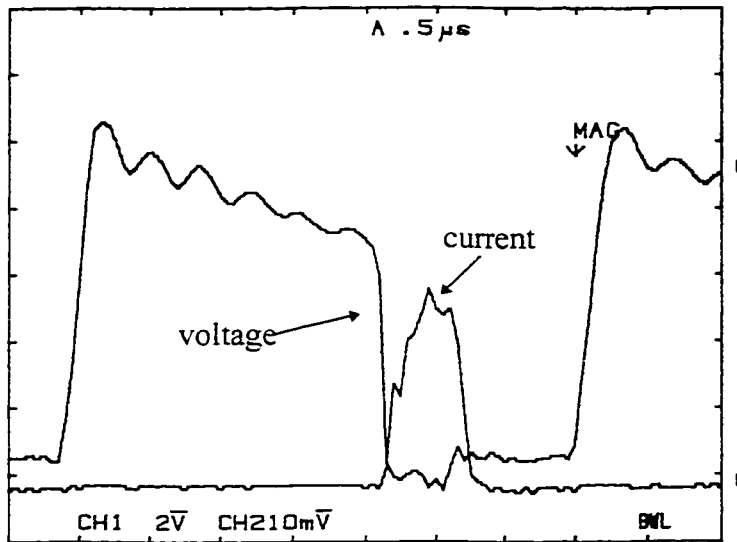


Fig. 3.14 Experimental results: the current and voltage of $Q2$ at medium line half load.
 $P_o=50\text{W}$. $V_{in}=50\text{V}$. $f_s=300\text{kHz}$.
 Scales: vertical-- 20V/div. , 1A/div. ; horizontal-- $0.5\mu\text{s/div.}$

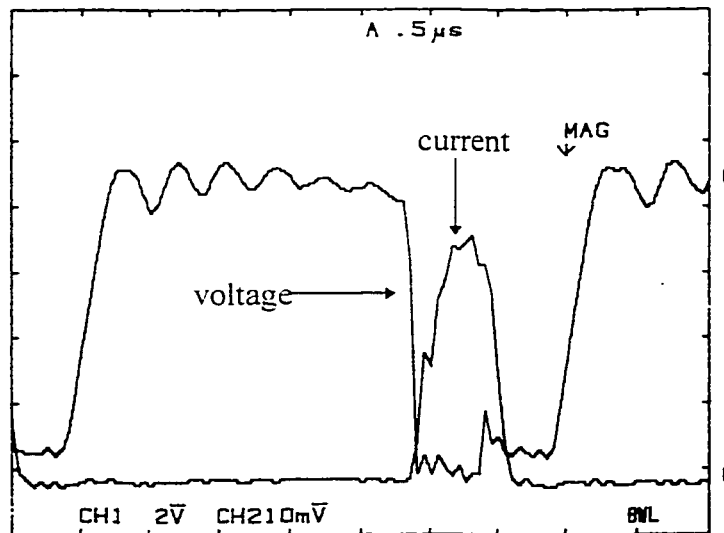


Fig. 3.15 Experimental results: the current and voltage of $Q2$ at high line light load.
 $P_o=20\text{W}$. $V_{in}=60\text{V}$. $f_s=300\text{kHz}$.
 Scales: vertical-- 20V/div. , 1A/div. ; horizontal-- $0.5\mu\text{s/div.}$

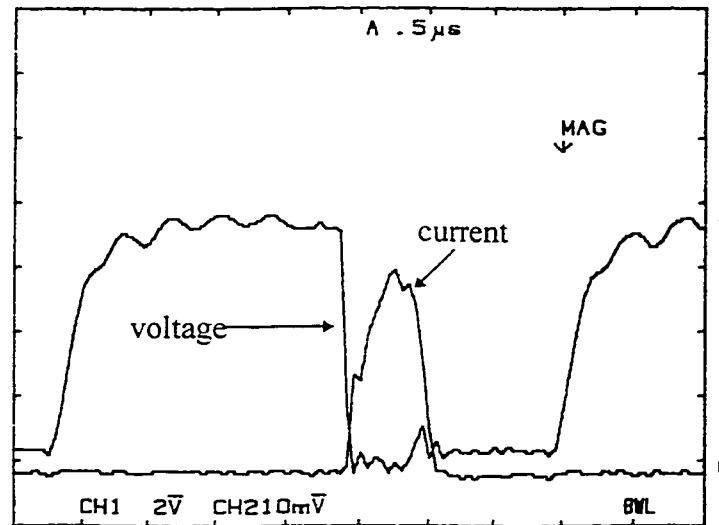


Fig. 3.16 Experimental results: the current and voltage of $Q2$ at low line light load.
 $P_o=20\text{W}$, $V_m=40\text{V}$, $f_s=300\text{kHz}$.
 Scales: vertical-- 20V/div ., 1A/div .; horizontal-- $0.5\mu\text{s/div}$.

3.6.3 Efficiency

Experimental results of the efficiency from the prototype converter are obtained. The input dc voltage varies from 40 to 60 V. The full load power is 100 W. Synchronous rectification is used in the circuit output rectifying stage.

Fig. 3.17 shows the experimental results the efficiency vs. input voltage under full the load condition (100W). The comparison between the efficiencies of the ZVS and the hard switching operation of the forward converter is made in Fig. 3.17. The hard switching forward also employs synchronous rectifiers. The comparison shows that ZVS indeed makes a significant increase (about 5%) in efficiency. ZVS operation at frequency of 200 kHz is also tested, where the snubber capacitor and the primary of the coupled inductor are adjusted to suit for this frequency.

The efficiency is about 1% higher than that at 300kHz. The gain in efficiency is due to the reduced switching losses in the auxiliary switch, and the gate drives of the synchronous rectifiers.

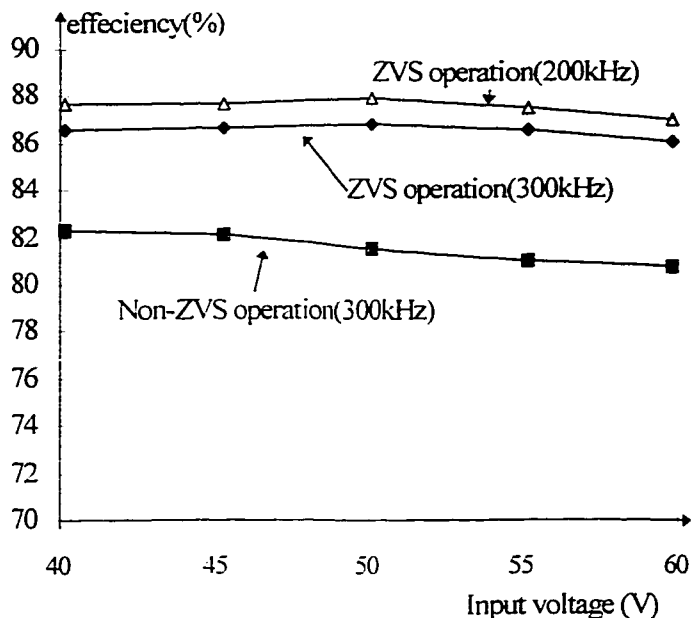


Fig. 3.17 The efficiencies vs. input voltage of the prototype converter in ZVS operation and non-ZVS operation of the forward converter (conditions: $P_o=100\text{W}$, $V_o=5\text{V}$).

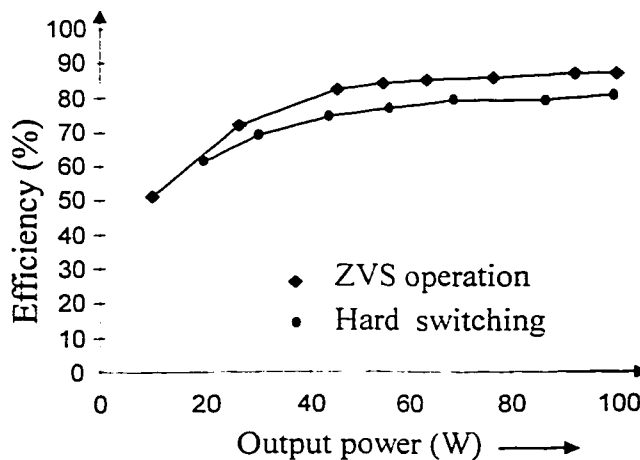


Fig. 3.18 The efficiencies vs. load of the prototype converter in ZVS operation and non-ZVS operation. Conditions: $V_{in}=50\text{V}$, $f_s=300\text{kHz}$.

Fig. 3.18 shows the efficiency vs. load under given input voltage for both the proposed and conventional circuits. The proposed circuit always has better efficiency than the conventional hard switching forward converter.

The efficiency is expected to be higher if optimized magnetics are used, and if a PCB circuit is built. That means, using the proposed forward topology, a 90% forward converter outputting 20A at 5V is possible.

3.7 CONCLUSIONS

In this chapter a ZVS forward converter topology has been presented and analyzed. The steady state operation of the circuit can be divided into seven intervals. The steady state analysis of the circuit is performed and verified experimentally.

Analysis and experimental results show that the performance of the proposed converter is enhanced with the auxiliary circuit. About 5% higher efficiency has been achieved on the prototype circuit as compared with the conventional hard switching converter. Higher efficiency is expected on PCB circuit with optimal magnetics. Other major merits of the proposed ZVS forward topology include

- (i) Lossless switching of the main switch, independent of the line and load conditions,
- (ii) Simple power and control circuit,
- (iii) No increase in conduction losses,
- (iv) Ability to operate in either voltage or current mode control.

Therefore, the proposed converter topology will hopefully be widely used in industrial application in the future.

CHAPTER 4

SMALL SIGNAL MODELS AND CLOSED LOOP STABILITY

4.1 INTRODUCTION

The steady state analyses of the proposed converters have been performed in the previous chapters, which have shown the advantages of the converters over the conventional hard switching and existing ZVS circuits. However, only the steady state analysis is not enough. The circuits should tolerate the line and load variations, and they should regulate the output against these variations by means of closed loop control. In order to study the behavior of converters under these conditions, the small signal analyses for both the converters are presented in this chapter. These analyses are also used to optimize the closed loop response.

This chapter presents the small signal models and the closed loop stability of the converters. The small signal model of a circuit differs with the loop structure, or the control technique used. Normally, there are three types of control technique developed for the dc/dc converters, namely, the voltage mode control, the peak current mode control,

and the average current mode control. It has been shown in [19,20] that the average current mode control brings in the best dynamic performance, hence, it is discussed in this chapter. As the flyback converter can utilize a model previously developed in [20], only the small signal model of the forward converter is derived below. During the discussion, the equivalent series resistance (ESR) of the capacitors is ignored because the effects of ESR can be reduced with high quality capacitors and these effects is negligible in the frequency range of our concern (<100 kHz).

The structure of this chapter is as follows. Section 4.2 reviews the basic criteria of a stable closed loop system. Section 4.3 discusses the stabilization of the flyback converter. Section 4.4 presents the derivation of the small signal model of the forward converter, and discusses the stabilization issues. Section 4.5 presents the experimental verifications of the model derived.

4.2 CRITERIA OF A DYNAMICALLY STABLE SYSTEM

According to the Nyquist stability criteria, the closed loop stability of a switch mode converter is optimal, if (i) the open loop gain has a slope of -20 dB/dec. in the vicinity of the crossover frequency f_c , and (ii) the open loop transfer function has a phase margin of about 45° to 63° [19-21]. Proper compensation should be made around the loop to meet these two criteria. Hence the loop should be tailored such that the above two conditions are satisfied.

4.3 SMALL SIGNAL MODELS OF THE ZVS FLYBACK CONVERTER

To simplify the discussion, it is assumed that the auxiliary circuit works for a very short time compared to the main circuit, which is the practical case when UC3855 (shown in Appendix I) is employed as the PWM control chip. The duty cycle of the auxiliary circuit D_{aux} is about 0.07 to 0.1. Also, it is assumed that the converter operates in the discontinuous conduction mode. Under such conditions, as analyzed in Section 2.4.2, the effect of the auxiliary circuit on the transformer current is negligible, and hence it is undetectable on the secondary side of the power transformer. In other words, it has little dynamic effect on the operation of the converter. Therefore, from the control point of view, the auxiliary circuit can be excluded from the closed loop, and importantly, the analysis is that of a basic flyback converter.

Fig. 4.1 shows the block diagram of a conventional feedback control loops of the standard flyback in the average current mode control. Fig. 4.2 shows a typical implementation of the feedback loops of Fig. 4.1 [20]. The current loop is formed by the following elements: (i) a current sensor resistor R_s , (ii) an error current amplifier CA, (iii) a PWM comparator and the gate drive, and (iv) the power switch S . Current in the switch is sensed. Because the control chip has a current synthesizer inside UC3855, the sensed current is transformed to reconstruct the inductor current in L_m .

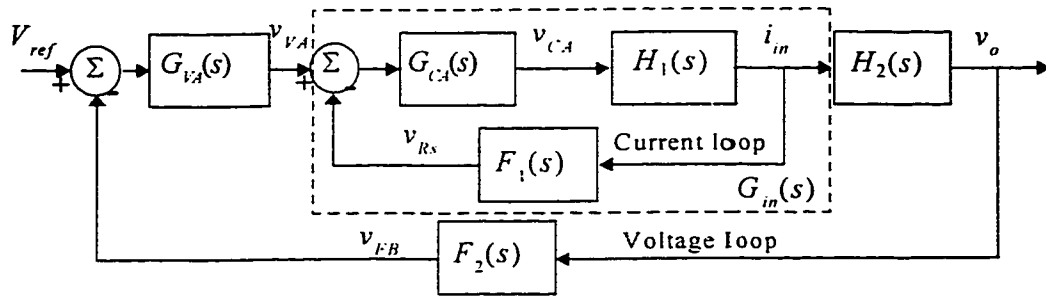


Fig. 4.1 The Block diagram of the control loops.

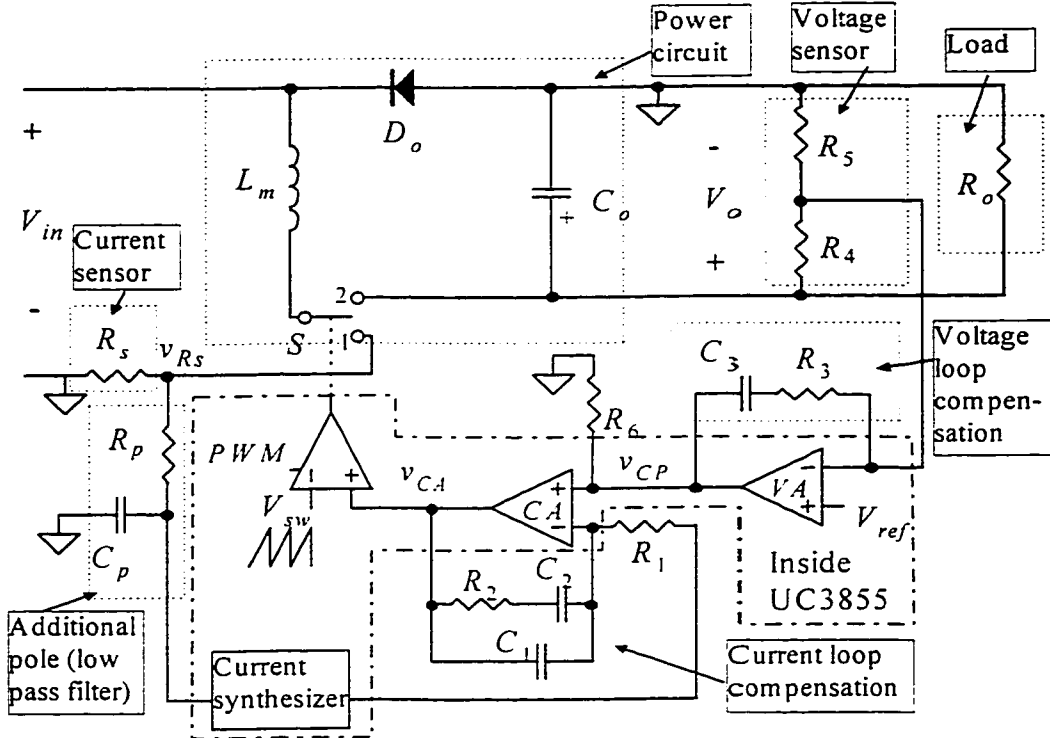


Fig. 4.2 A typical implementation of the feedback loops of Fig. 4.1. The elements enclosed by the dot-dash line are inside the UC3855 chip. Through the current synthesizer, R_1 reflects the actual current signal in L_m .

The voltage loop is comprised of (i) the closed current loop, (ii) the voltage sensor (R_4 and R_5), (iii) an error voltage amplifier VA , and (iv) the power circuit. The compensation elements are selected below.

4.3.1 Small Signal Model of the Current Loop of the Flyback Converter

(1) Transfer function of the power circuit

From the previous work [20], the small-signal control-to-input gain of the flyback current loop power circuit of Fig. 4.1 (from v_{CA} at the CA output, to v_{R_s} , the voltage across R_s) is given by

$$\frac{\hat{v}_{R_s}}{\hat{v}_{CA}} = \frac{R_s}{V_{sw}} \left(I_L + \frac{V_o}{sL_m} \right) \quad (4-1)$$

where, I_L is the averaged inductor current in L_m .

Incorporating this model into the isolated flyback topology shown in Fig. 1.1, where the turns ratio of the power transformer is $1/n$, and that of the current sensor transformer is K , the gain becomes

$$\frac{\hat{v}_{R_s}}{\hat{v}_{CA}} = H_1(s)F_1(s) = \frac{KR_s}{V_{sw}} \left(I_L + \frac{V_o}{nsL_m} \right) \quad (4-2)$$

where $F_1(s)$ is the current sensor transfer function given by

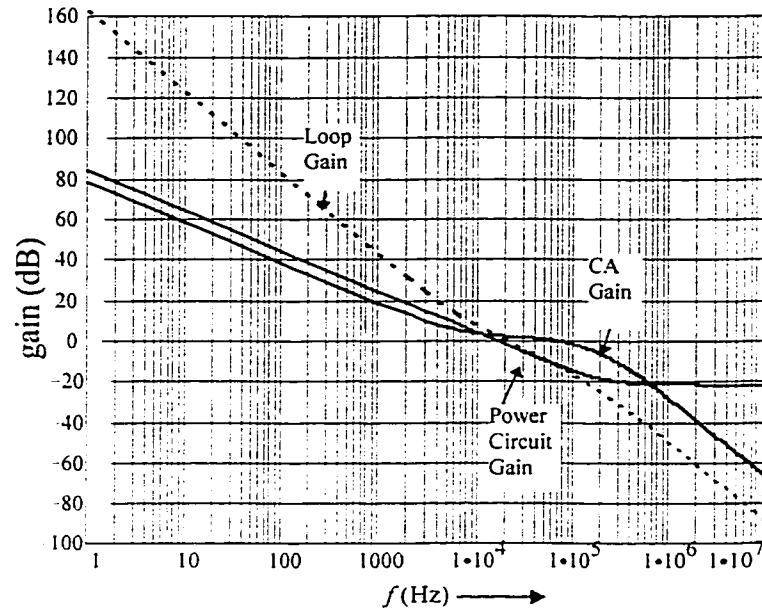
$$F_1(s) = KR_s \quad (4-3)$$

Eq. (4-2) has a pole at 0 Hz and a zero at

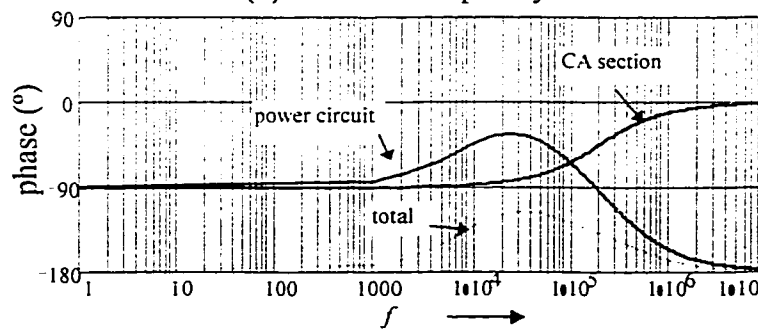
$$f_z = \frac{V_o}{2\pi n I_L L_m} \quad (4-4)$$

This zero moves with I_L , which corresponds to certain line and load conditions. In order to maintain the stability under all line/load conditions, the crossover frequency of the current loop gain should be selected lower than the lowest zero given by Eq. (4.4).

Fig. 4.3 shows the bode plot of the current loop of the prototype flyback converter (refer to the design example in Chapter 5), where $K=1/100$, $n=1/18$, $V_o=5$ V, $V_{sw}=5.5$ V, $R_s=30$ Ω , and $L_m=50$ μ H, and $f_s=200$ kHz. In this case it is found that the lowest value of f_z , which corresponds to the full load and lowest input voltage, is about 190 kHz.



(a) Gain vs. frequency



(b) Phase shift vs. frequency

Fig. 4.3 The Bode Plot of the opened current loop of the prototype flyback converter.

(2) Compensation for the closed loop stabilization

Concepts of the compensation for the closed loop stabilization can be illustrated

with the example of the prototype converter.

The crossover frequency f_c should not go higher than the lowest zero frequency of the power circuit transfer function. Also, it should be selected below one sixth of the switching frequency [20]. In the example, if $f_s=200$ kHz and $f_z=190$ kHz, then f_c is set at 20 kHz.

The result of the compensation is shown in Fig. 4.3(a), and has two poles and one zero to give a proper loop gain. The implementation is shown in Fig. 4.2. Thus the transfer function of CA is determined by

$$G_{CA}(s) = \frac{sR_2C_2 + 1}{sR_1[sR_2C_1C_2 + (C_1 + C_2)]} \quad (4-5)$$

where the poles and zero are found to be

$$f_{p1} = 0 \quad (4-6)$$

$$f_{p2} = \frac{C_1 + C_2}{2\pi R_2 C_1 C_2} \quad (4-7)$$

$$f_{z1} = \frac{1}{2\pi R_2 C_2} \quad (4-8)$$

In order to suppress the high frequency noise caused by switching, it requires additional pole around f_{p2} by adding the network R_p - C_p , which gives

$$f_{p2} = \frac{1}{2\pi R_p C_p} \quad (4-9)$$

The value of each component is determined as [20]

$$C_1 = K \frac{R_s}{R_1 V_{sw} f_s} I_{L_max} \quad (4-10)$$

$$R_2 = \left[\frac{\hat{v}_{Rs}}{\hat{v}_{C.A}} \bigg|_{f=f_c} \right]^{-1} R_1 \quad (4-11)$$

$$C_2 = \frac{1}{2\pi R_2 f_{z1}} \quad (4-12)$$

$$R_p = \frac{1}{2\pi f_{p2} C_p} \quad (4-13)$$

In the example of the prototype converter, by selecting $R_1=3.9 \text{ k}\Omega$ it is found that $C_1=100 \text{ pF}$ and $R_2=4.7 \text{ k}\Omega$. By putting a zero at $f_{z1}=6 \text{ kHz}$, there are $C_2=4700 \text{ pF}$ and $f_{p2}=100 \text{ kHz}$. By letting $C_p=1000 \text{ pF}$, it yields $R_p=1.5 \text{ k}\Omega$.

The compensation is shown in Fig. 4.3(a). Fig. 4.3(b) shows the Bode plot of the total open loop phase shift. The open loop phase margin at f_c is found to be 61.5° .

The equivalent transfer function of the closed current loop is

$$G_m(s) = \frac{G_{C.A}(s)H_1(s)}{1 + G_{C.A}(s)H_1(s)F_1(s)} \quad (4-14)$$

$G_m(s)$, is an element of the voltage loop.

4.3.2 Small Signal Model of the Voltage Loop of the Flyback Converter

The stability criteria for the voltage loop is the same as that for the current loop. The compensation is needed to tailor the total voltage loop gain to fit the stability criteria.

(1) Transfer function of the power circuit

For the flyback converter output stage shown in Fig. 4.1, the small signal model is

$$\hat{v}_o = \frac{R_o}{1 + sR_o C_o} \hat{i}_o \quad (4-15)$$

By the power balance equation,

$$(I_o + \Delta I_o)(V_o + \Delta V_o) = (I_m + \Delta I_m)(V_m + \Delta V_m) \quad (4-16)$$

where ΔI_o , ΔV_o , ΔI_m , and ΔV_m are the small signal perturbations in the related signals.

Ignoring the second order terms and assuming a constant V_m and applying the Laplace transformation, Eq. (4-16) yields the small signal model for the output stage:

$$I_o \hat{v}_o + V_o \hat{i}_o = V_m \hat{i}_m \quad (4-17)$$

where

$$I_o = V_o / R_o \quad (4-18)$$

From Eqs.(4-14) and (4-16), the transfer function of the output stage is

$$H_2(s) = \frac{\hat{v}_o}{\hat{i}_m} = \frac{V_m}{V_o} \frac{R_o}{2 + sR_o C_o} \quad (4-19)$$

Then the power circuit transfer function. from the output of VA to the output end of the converter, is

$$G_{pw}(s) = \frac{\hat{v}_o}{\hat{v}_{CP}} = G_m(s) H_2(s) \quad (4-20)$$

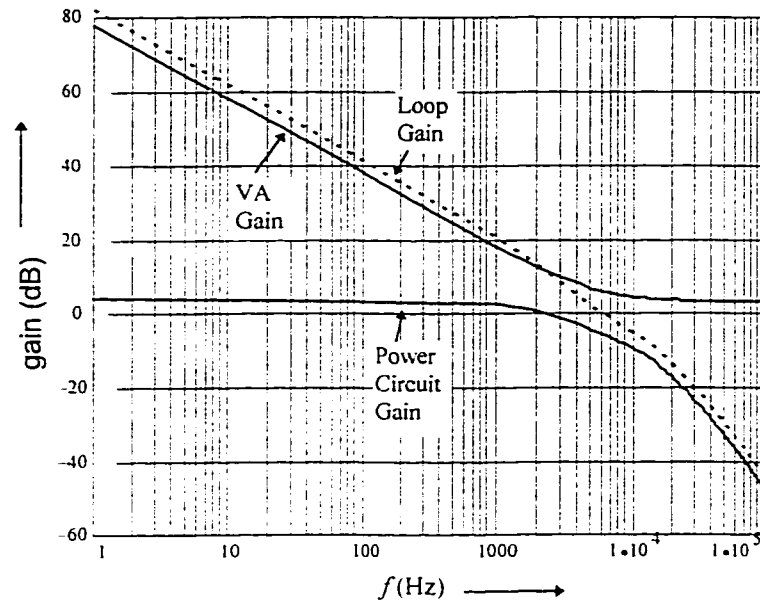
Fig. 4.4 shows the Bode plot of the voltage loop gain of the prototype flyback.

(2) Compensation for the closed loop stabilization

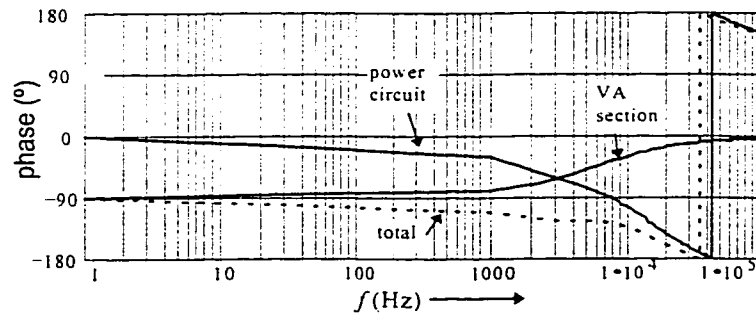
Referring to Fig. 4.4(a), the compensation for the voltage loop can be achieved by a PI controller. The implementation is shown in Fig. 4.2. Thus the transfer function of the VA compensation network and the voltage sensor is

$$G_{VA}(s) F_2(s) = \frac{\hat{v}_{CP}}{\hat{v}_o} = \left(\frac{R_3}{R_4} + \frac{1}{sR_4 C_3} \right) \quad (4-21)$$

In the example of the prototype flyback converter, it is found that, by selecting the crossover frequency at 10 kHz, and choosing $R_4=3\text{ k}\Omega$ and $R_5=4.5\text{ k}\Omega$, the needed compensation requires $R_3=4.9\text{ k}\Omega$ and $C_3=7.8\text{ nF}$. The phase margin is thus found to be 63.2° .



(a) Gain vs. frequency



(b) Phase shift vs. frequency

Fig. 4.4 The Bode plot of the gain of open voltage loop of the prototype flyback converter.

4.4 SMALL SIGNAL MODEL OF THE ZVS FORWARD CONVERTER

Fig. 4.5 shows the block diagram of the typical control loops of a forward topology, where the inductor current i_{L_o} is controlled.

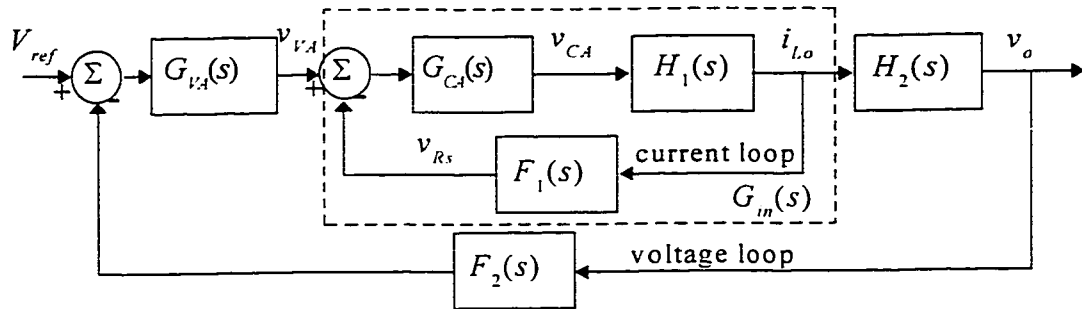


Fig. 4.5 A typical block diagram of the control loops of forward converter.

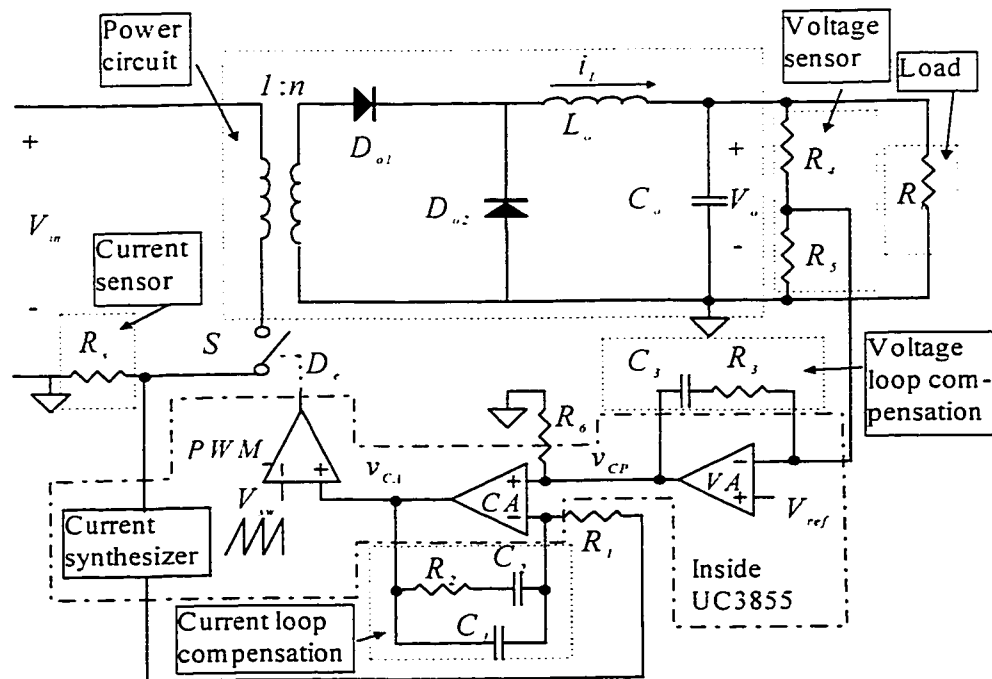


Fig. 4.6 A typical implementation of the feedback loops of Fig. 4.5. The elements enclosed by the dot-dash line are inside the UC3855 chip. Through the current synthesizer, R_s reflects the actual current signal in L_o .

Fig. 4.6 shows a typical implementation of the feedback loops of Fig. 4.5 in the case of the forward topology. The current loop is formed by the following elements: (i) a current sensor resistor R_s , (ii) an error current amplifier CA , (iii) a PWM comparator and the drive, and (iv) the power switch S .

4.4.1 Small Signal Models of the Current Loop of the Forward Converter

(1) Transfer function of the power circuit

Current in the switch is sensed. But, owing to the current reconstruction element, which is called the ‘current synthesizer’ in the PWM chip UC3855, the current in L_o , namely i_L , is virtually sensed and hence controlled.

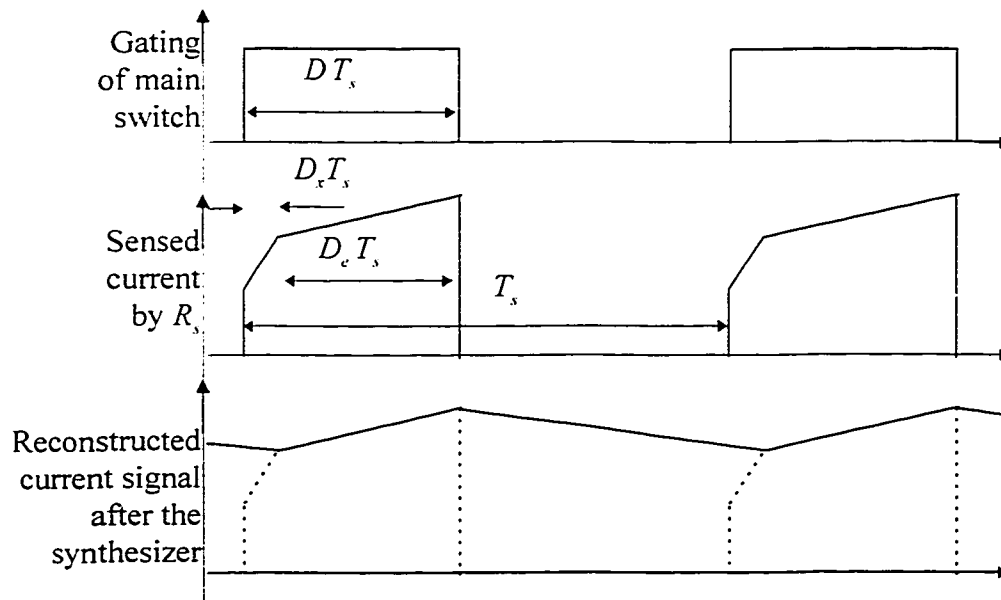


Fig. 4.7 The reconstruction of the sensed current in the proposed ZVS forward converter. The sensed switch current shown in Fig. 3.2, is reconstructed by the synthesizer inside UC3855 to reflect the waveshape of the output inductor current. D is the main duty cycle, D_c is the effective duty cycle, and D_x is the difference between them.

Fig. 4.7 shows the current reconstructing function in the proposed ZVS forward converter. The sensed switch current shown in Fig. 3.2, is reconstructed by the synthesizer inside UC3855 to reflect the waveshape of the output inductor current. D is the main duty cycle, D_e is the effective duty cycle, and D_x is the difference between them. D_x is due to the effects of L_s in Fig. 3.1 and is determined by Eq. (3-79). From the loop point of view, such a reconstruction function simply hides the effects of the auxiliary circuit, making it look like a conventional forward converter. The only exception here is that the effectual duty cycle is no longer D , but is

$$D_e = (D - D_x) \quad (4-22)$$

Therefore, the state space average equation of the converter is,

$$(nV_m - V_o)(D - D_x) - V_o(1 - D - D_x) = L_o \frac{di_{L_o}}{dt} \quad (4-23)$$

where, $n = N_s/N_p$.

Then the DC model of the converter is

$$nV_m(D - D_x) - V_o = 0 \quad (4-24)$$

which is confirmed by Eq. (3-75). With assumption of constant V_m and V_o , the small signal AC model is represented as

$$nV_m(\hat{d} - \hat{d}_x) = sL_o \hat{i}_{L_o} \quad (4-25)$$

According to Eqs.(3-25), (3-26), (3-32), (3-34), (3-37) and (3-78), it can be obtained

$$I_o = \frac{nV_m}{L_s} D_x T_s + \frac{V_m}{2nL_{op}} D_{aux} T_s \quad (4-26)$$

Substituting Eq. (3-17) into (4-26), and substituting $I_o + \Delta I_o$, $V_m + \Delta V_m$ and $D_x + \Delta D_x$ for their respective variables, and ignoring the second order terms, gives

$$\Delta I_o = \frac{nV_m}{L_s f_s} \Delta D_x + \frac{n\Delta V_m}{L_s f_s} \left(D_x + \frac{D_{aux}}{2} \right) \quad (4-27)$$

Hence,

$$\Delta D_x = \frac{L_s f_s}{nV_m} \Delta I_o - \frac{D_x + 0.5D_{aux}}{V_m} \Delta V_m \quad (4-28)$$

By the assumption $\Delta I_o = \Delta I_{lo}$ and $\Delta V_m = 0$,

$$\Delta D_x = \frac{L_s f_s}{nV_m} \Delta I_{Lo} \quad (4-29)$$

In the Laplace transformation, Eq. (4-29) can be written as:

$$\hat{d}_x = \frac{L_s f_s}{nV_m} \hat{i}_{Lo} \quad (4-30)$$

Substituting it into Eq.(4-25), and rearranging the terms,

$$\hat{i}_{Lo} = \frac{nV_m}{sL_o + f_s L_s} \hat{d} \quad (4-31)$$

Then the sensed voltage on the sensor resistor, on the secondary of the sensor transformer, is

$$\hat{v}_{Rs} = nKR_s \hat{i}_{Lo} \quad (4-32)$$

where K is the turns ratio of the current sensor transformer, R_s the sensor resistor.

Let V_{sw} represent the peak to peak voltage of the saw tooth waveform, then

$$\hat{d} = \frac{1}{V_{sw}} \hat{v}_{CA} \quad (4-33)$$

where v_{CA} is the output of the current amplifier of the current loop.

Therefore, from Eqs. (4-31) through (4-33), the control-to-output gain of the forward current loop power circuit (from v_{CA} at CA output, to v_{Rs} , the voltage across the sensor

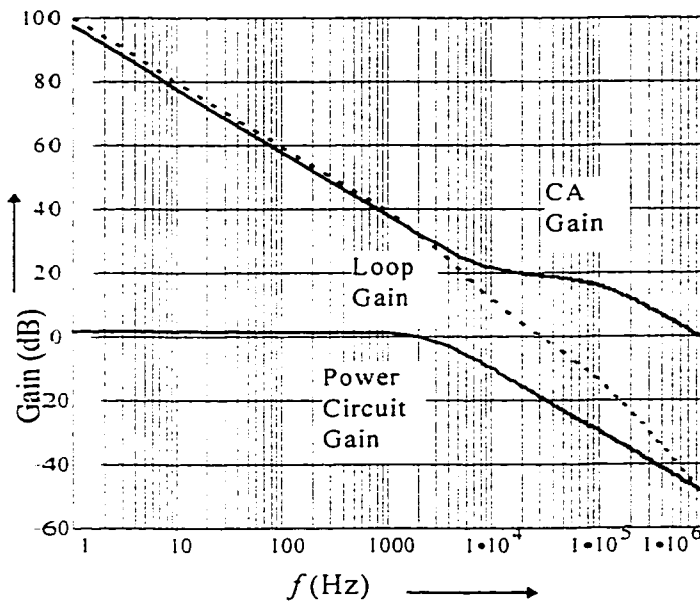
resistor R_s) is given by

$$H_1(s)F_1(s) = \frac{\hat{v}_{R_s}}{\hat{v}_{CA}} = \frac{n^2 KR_s V_{in}}{V_{sw}} \cdot \frac{1}{sL_o + f_s L_s} \quad (4-34)$$

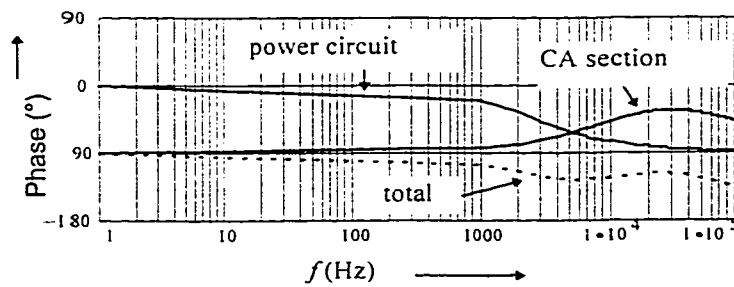
There is a pole at

$$f_p = \frac{f_s L_s}{2\pi L_o} \quad (4-35)$$

Hence the power circuit open loop gain is flat at low frequencies and rolls off at f_p with a -20dB/Dec. slope.



(a) Gain vs. frequency



(b) Phase shift vs. frequency

Fig. 4.8 The Bode plot of the current loop of the prototype forward converter.

Fig. 4.8 shows the Bode plot of the open loop gain of the current loop of the prototype forward converter (refer to the design example in Chapter 5 and Appendix II), where $n=1/3$, $L_o=6 \mu\text{H}$, $L_s=0.3 \mu\text{H}$, $f_s=300 \text{ kHz}$, $R_s=12.5 \Omega$, $K=1/100$, $V_m=50 \text{ V}$ and $V_{sw}=5.5 \text{ V}$. Then the pole of the power circuit is found to be at 2.6 kHz.

(2) Compensation for the closed loop stabilization

The needed compensation network is similar to that in the flyback circuit, i.e., two pole and one zero compensation. The implementation of the compensation is shown in Fig. 4.6. Similar process to that in the case of flyback topology is followed.

Eqs. (4-5) through (4-9) define the transfer function of the compensator and the poles and zero. Eqs. (4-11) and (4-12) determine the values of R_2 and C_2 . C_1 is determined from Eq. (4-7) by setting the second pole, f_{p2} . In the example of the prototype forward converter, selecting $f_c=30 \text{ kHz}$, $R_1=3.3 \text{ k}\Omega$, $f_z=8.0 \text{ kHz}$ and $f_{p2}=100 \text{ kHz}$, it is found that, $R_2=33 \text{ k}\Omega$, $C_1=56 \text{ pF}$ and $C_2=560 \text{ pF}$.

Fig. 4.8 (b) shows the Bode plot of the open loop phase shift of the current loop of the prototype forward converter. The phase margin is about 61.5° .

The equivalent transfer function of the closed current loop has the same definition as in Eq. (4-14).

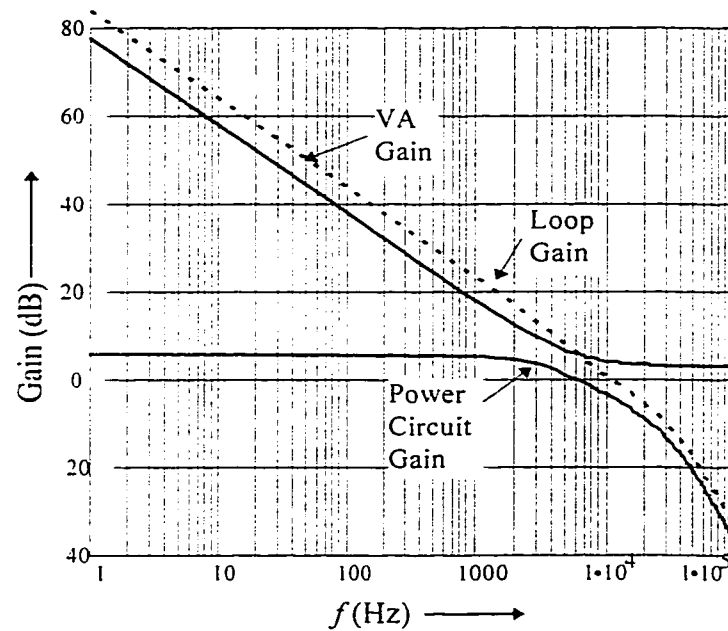
4.4.2 Voltage Loop of the Forward Converter

(1) The characteristic of the power circuit gain

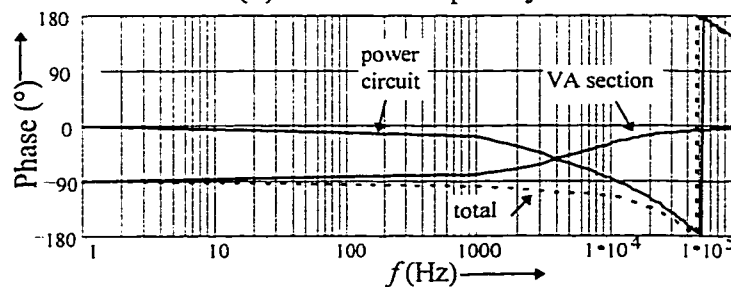
The closed inner loop is an element of the voltage loop. Referring to Fig. 4.6, the output stage of the circuit has a transfer function as given by

$$H_2(s) = \frac{\hat{v}_o}{\hat{i}_o} = \frac{R_o}{1 + s \cdot R_o \cdot C_o} \quad (4-36)$$

Then the power circuit, from the output of VA to the output of the converter, has a transfer function as defined in Eq. (4-20).



(a) Gain vs. frequency



(b) Phase shift vs. frequency

Fig. 4.9 The Bode Plot of the open voltage loop gain and phase-shift of the prototype forward converter.

Fig. 4.9 shows the Bode plot of the open voltage loop of the prototype forward converter.

(2) Compensation for the closed loop stabilization

With reference to Fig. 4.9(a), the compensation can be performed by a PI controller. The implementation is shown in Fig. 4.6. The transfer function of the VA compensation network and the voltage sensor is defined by Eq. (4-21). In the case of the prototype forward converter, if selecting the crossover frequency around 10 kHz, $R_4=3$ k Ω and $R_5=4.5$ k Ω , the components for the PI are found to be $R_3=4.3$ k Ω and $C_3=6.8$ nF. The open voltage loop gain is show in Fig. 4.11. The phase margin is 64.8°.

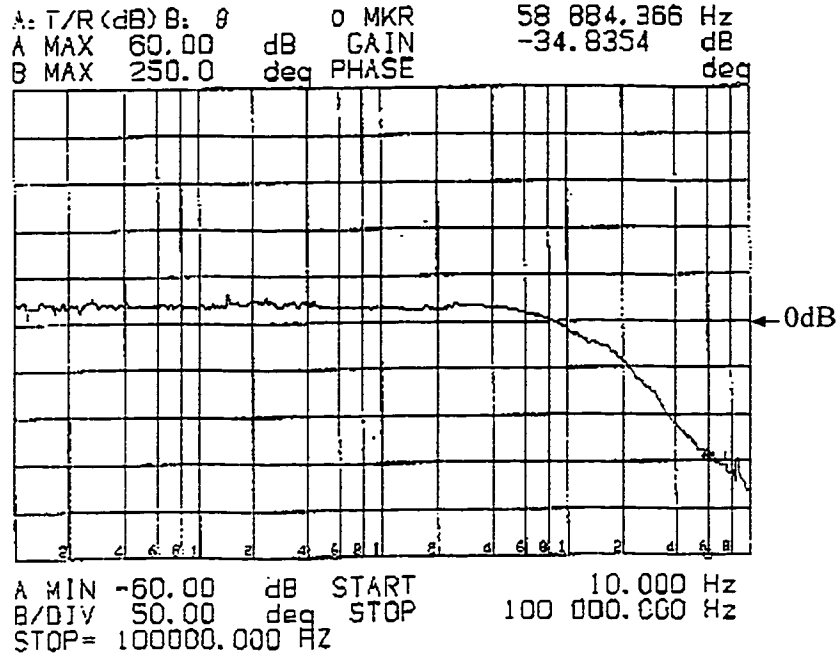
4.5 Experimental Results

Experimental verification of the small signal models discussed above is made on the prototype forward converter. For convenience, the transfer function of the voltage loop power circuit, $G_{pw}(s)$, is tested.

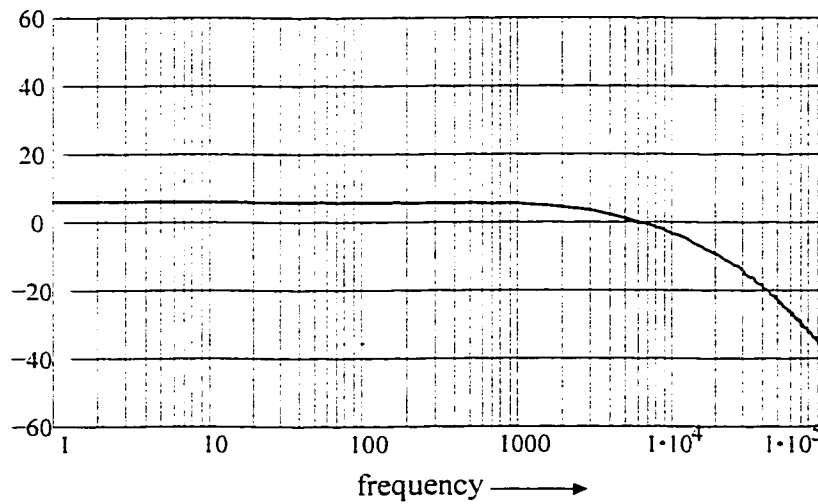
Figs. 4.10(a) and 4.11(a) show the experimental results of the Bode plots of $G_{pw}(s)$. Figs. 4.10(b) and 4.11(b) shows the theoretical predictions of $G_{pw}(s)$ in the same scale as Fig. 4.10(a).

Table 4.1 The theoretical and experimental results of the power circuit transfer function.

	gain in low freq. range	phase in low freq. range	gain at 10 kHz	phase at 10 kHz	gain at 100 kHz	phase at 100 kHz
Theoretical results	6.0 dB	0 deg.	3.2 dB	-89.6 deg.	-37.7 dB	beyond -180 deg
Experimental results	5.0 dB	0 deg	3.0 dB	-98.0 deg	-43.0 dB	beyond -180 deg



(a) Experimental results. Vertical: 12 dB/div.



(b) Theoretical results. Vertical: 20 dB/div.

Fig. 4.10 Comparison between the experimental and theoretical gain of the open voltage loop power circuit.

Comparison between theoretical and experimental results are shown in Table 4.1, which shows that they are in a good agreement.

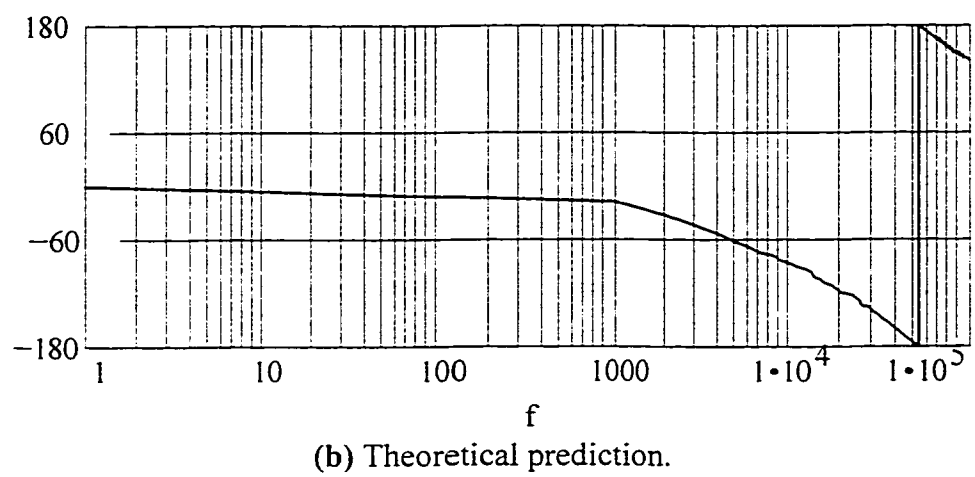
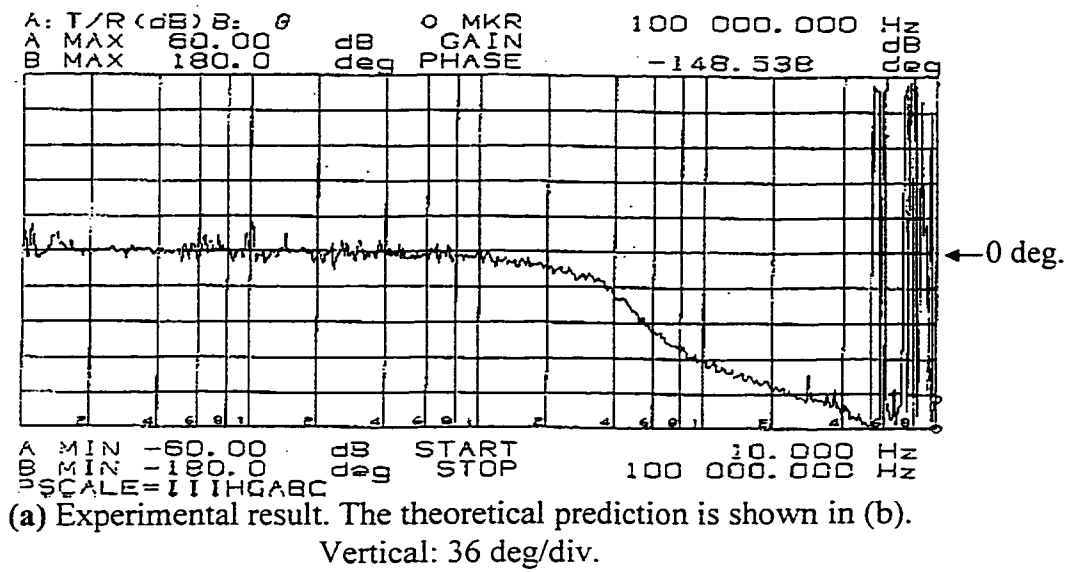


Fig. 4.11 Comparison between the phase shift of the open voltage loop power circuit transfer function.

Figs. 4.12 through 4.14 shows the experimental results of transient responses of the forward circuit under step force. The circuit is stable under these step changes. Experiment of the step up of the input voltage is not able to carry out for the difficulty in getting a fast step change in the dc line with available instruments.

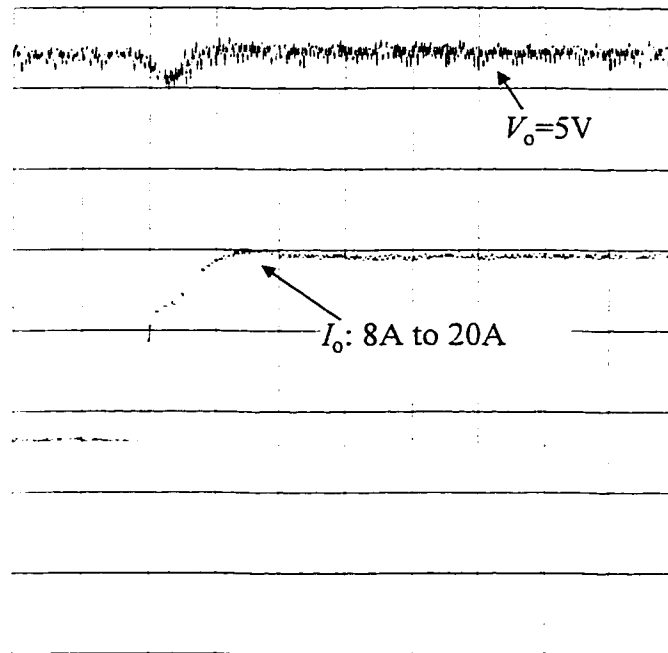


Fig. 4.12 Experimental results of the forward converter: transient response. I_o steps up from 8A to 20A. Conditions: $V_{in} = 50V$, $f_s = 300kHz$. Vertical--5A/div., 1V/div., Horizontal--50 μs /div.

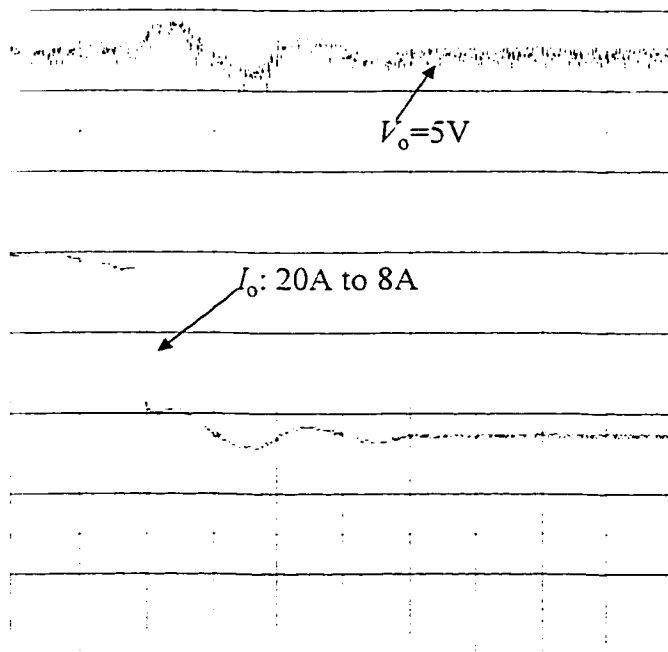


Fig. 4.13 Experimental results of the forward converter: transient response. I_o steps down from 20A to 8A. Conditions: $V_{in} = 50V$, $f_s = 300kHz$. Vertical--5A/div., 1V/div., Horizontal--50 μs /div.

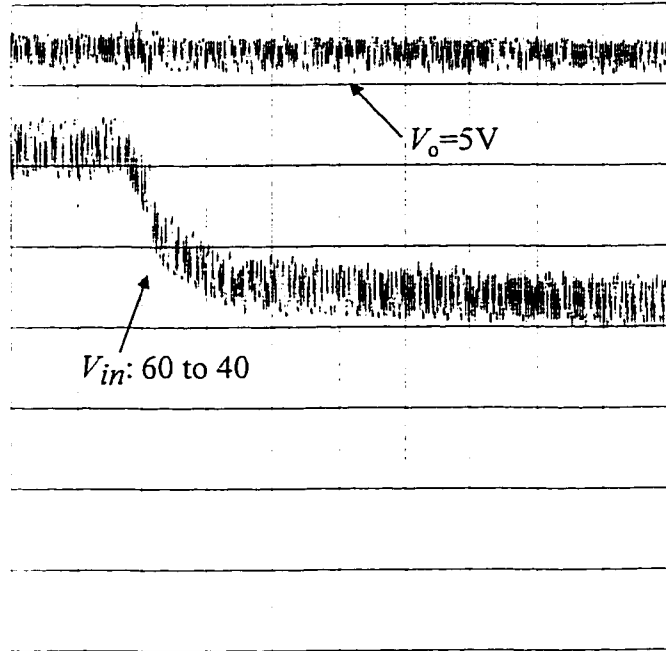


Fig. 4.14 Experimental results of the forward converter: transient response. V_m steps down from 60V to 40A. Conditions: $P_o=100W$, $f_s=300kHz$. Vertical--5A/div.. 0.5V/div.. Horizontal--500 μ s/div.

4.6 CONCLUSIONS

Small signal models of the proposed circuits in the average current mode control and the closed loop stability compensation have been discussed in this chapter. The proposed flyback converter can utilize the previously established model for the standard flyback and the compensation can follow the conventional scheme and process.

As there is no suitable model for the proposed forward converter, the model is thus derived in this chapter. The additional inductor L_x of the auxiliary circuit brings a pole at the frequency in proportional to the switching frequency and L_x . Compensation of the are simple and straightforward.

CHAPTER 5

DESIGN PROCEDURES

5.1 INTRODUCTION

This chapter presents the design procedures of the proposed converters. The design is based on the required specifications, such as the input voltage range, output voltage, output power, switching frequency, permitted ripple in the output voltage, etc., and uses the analysis presented in the previous chapters.

Design for generating gating pattern for the auxiliary switch in the proposed converter topologies is also presented in the case where a single output PWM control chip other than UC3855 is employed.

The structure of this chapter is as follows. In Section 5.2, the design of the flyback converter is presented and an example is given. In Section 5.3, the design of the forward converter and an example are presented. In Section 5.4, an implementation of the gating pattern generating for the auxiliary switch in the proposed converters is illustrate and verified experimentally.

5.2 DESIGN PROCEDURE OF THE FLYBACK CONVERTER

Assume the following specifications and parameters are known.

D_{\max} --Maximum duty cycle

f_s --Switching frequency, Hz

P_o --Full load output power, W

V_{in_max} --Maximum input voltage, V

V_{in_min} --Minimum input voltage, V

V_o --Output voltage, V

ΔV_m --Permitted peak-peak ripple in V_m , V

ΔV_o --Permitted peak-peak ripple in V_o , V

5.2.1 Design of the Power Circuit

The following design procedures are referred to the circuit shown in Fig. 2.1. All parameters are in SI units.

(1) Turns ratio of the transformer, N_p/N_s

According to Eq. (2-56), and considering the forward voltage drop V_F of the rectifier diode,

$$V_o = \frac{D}{D'} n V_m - V_F = \frac{N_s}{N_p} \cdot \frac{D_{\max}}{D'} V_{in_min} - V_F \quad (5-1)$$

where, $D' (< 1 - D_{\max})$ is the equivalent duty cycle of the rectifier current, and

V_F is the forward voltage drop of the rectifier.

Eq. (5-1) gives

$$\frac{N_p}{N_s} = \frac{D_{\max}}{D'} \cdot \frac{V_{in_min}}{V_o + V_F} \quad (5-2)$$

and

$$n = \frac{N_s}{N_p} = \frac{D'(V_o + V_F)}{D_{\max} V_{in_min}} \quad (5-3)$$

(2) Magnetizing inductance, L_m

In the discontinuous conduction mode, from Eq. (2-40), there should be

$$I_s - \frac{V_o}{n^2 f_s L_m} D' \leq 0 \quad (5-4)$$

Combining Eqs. (5-4) and (2-39) gives

$$L_m \leq \frac{V_o^2}{2n^2 f_s P_o} D'^2 \quad (5-5)$$

(3) Output capacitor, C_o

Fig. 5.1 shows the relationship between the output rectifier current i_s and load current I_o in the case of discontinuous conduction mode operation. Assuming all the ripple current component of i_s flows through C_o and the average current flows through R_o . It can be calculated that

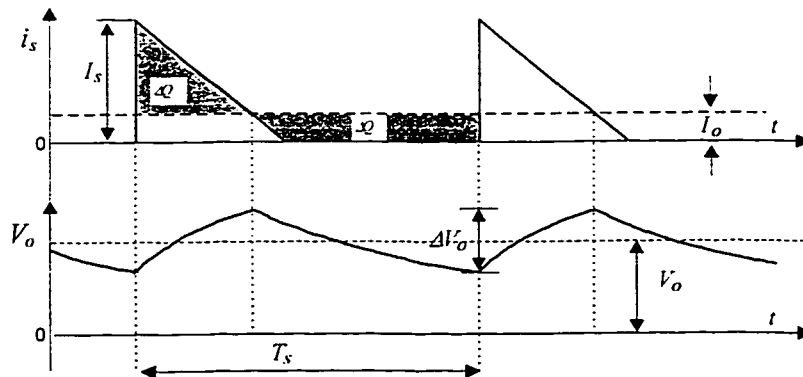


Fig. 5.1, The secondary current and the output voltage ripple in the converter of Fig. 2.1. The operation mode is assumed to be discontinuous conduction.

$$\Delta Q = \left(\frac{I_{sp} - I_o}{I_{sp}} \right)^2 I_o T_s \quad (5-6)$$

As I_{sp} is determined by Eq. (2-39), and

$$I_o = \frac{P_o}{V_o} \quad (5-7)$$

and

$$\Delta V_o \geq \Delta Q / C_o \quad (5-8)$$

The output capacitor can be found from Eqs. (2-39) and (5-6) through (5-8):

$$C_o \geq \frac{n^2 L_m}{2V_o \Delta V_o} \left(\sqrt{\frac{2P_o}{n^2 L_m f_s}} - \frac{P_o}{V_o} \right)^2 \quad (5-9)$$

(4) Selection of the main switch, $Q1$

By Eq. (2-33), the voltage rating of $Q1$ is determined by

$$V_{DSS_Q1} \geq V_m + \frac{1}{n}(V_o + V_F) \quad (5-10)$$

where, V_{DSS_Q1} is the drain to source breakdown voltage rating of $Q1$.

The rms current is determined by Eq. (2-60), and the average current rating is determined

by

$$I_{D_Q1} \geq 1.5 \frac{P_o}{V_{m_min}} \quad (5-11)$$

where, the constant 1.5 accounts for the worst case efficiency of 70%, and

I_{D_Q1} is the continuous drain current rating.

From Eqs. (2-26) and (2-55), the peak pulse drain current rating is

$$I_{MD_Q1} > n I_s = \sqrt{\frac{2P_o}{f_s L_m}} \quad (5-12)$$

where, I_{MD_Q1} is the pulse drain current rating.

Besides these ratings, a MOSFET which has the lowest ON resistance on the product catalogue should be selected.

(5) Selection of the output rectifier, D_o

The rectifier should be fast rectifier diode or Schottky diode. Its voltage rating is determined by

$$V_{R_{D_o}} > nV_{in_max} + V_o \quad (5-13)$$

where, $V_{R_{D_o}}$ is the reverse voltage rating.

Its current rating is determined by

$$I_{av_D_o} > \frac{P_o}{V_o} \quad (5-14)$$

where, $I_{av_D_o}$ is the average rectified current rating.

(6) Selection of the input capacitor, C_{in}

The input capacitor is determined by [23]:

$$C_m = \frac{P_o \Delta t_{sus}}{V_{m_min} \Delta V_m} \quad (5-15)$$

where, ΔV_m is the allowable peak-to-peak ripple voltage in the input line, and

Δt_{sus} is the time for which C_m must supply the current in case the input line fails.

5.2.2 Design of the Auxiliary Circuit

(1) Auxiliary duty cycle, D_{aux}

D_{aux} should be limited by

$$D_{aux} \leq (1 - 2 D_{max}) \quad (5-16)$$

In this way, the auxiliary circuit does not affect the resetting of the core of T_r .

D_{aux} may also be determined by the control chip like UC3855, where it is fixed. In this case the design should observe the fixed factor.

(2) Snubber capacitor, C_{snb}

The value of C_{snb} determines the rise time of $Q1$'s voltage at its turnoff. as described in Eq. (2-28). For a very short duration, we can approximate

$$\Delta u_{Q1}(t) \approx V_{in_min} \frac{\omega_0^2 D_{max}}{f_s} \Delta t \quad (5-17)$$

Limit the rise of u_{Q1} to be below V_{in} within the demanded time t_r . Thus, from Eqs. (2-29) and (5-17),

$$C_{snb} > \frac{D_{max} t_r}{f_s L_m} \quad (5-18)$$

On the other hand, the rise time should not exceed the gap left by $2D_{max}$ and D_{aux} , which gives a limit

$$t_4 - t_3 \leq (1 - 2D_{max} - D_{aux}) T_s \quad (5-19)$$

From Eqs. (2-28) and (2-33), there is an approximation

$$t_4 - t_3 \approx \frac{f_s}{\omega_0^2 D_{max} V_{in_min}} (V_{in_min} + \frac{1}{n} V_o) \quad (5-20)$$

Combining Eqs. (2-28), (5-19) and (5-20),

$$C_{snb} \leq \frac{(1 - 2D_{max} - D_{aux}) D_{max} V_{in_min}}{f_s^2 L_m (V_{in_min} + \frac{1}{n} V_o)} \quad (5-21)$$

The voltage rating of the capacitor should not be less than that of $Q1$.

(3) Primary of the coupled inductor, L_{ap}

As analyzed in Section 2.4.1, D_{aux} is fixed and corresponds to a quarter of the

resonant period of the network consisting of L_p and C_{snb} . Referring to Fig. 2.2, there exists a relationship:

$$D_{aux} = (t_2 - t_1)/T_s \quad (5-22)$$

According to Eqs. (2-10) and (5-22),

$$D_{aux} T_s = \frac{\pi}{2} \sqrt{L_{ap} C_{snb}} \quad (5-23)$$

which gives

$$L_{ap} = \frac{4 D_{aux}^2}{\pi^2 f_s^2 C_{snb}} \quad (5-24)$$

The core of the coupled inductors should be selected so that it can handle a power as given by

$$P_a = \frac{1}{2} L_{ap} I_{ap}^2 f_s \quad (5-25)$$

where, I_{ap} is defined by Eq. (2-16).

(4) Selection of the auxiliary switch, $Q2$

The on-resistance of $Q2$ should be as small as possible. Its voltage rating is the same as that of $Q1$. It should have a current rating capable of handling the peak discharging current I_{ap} , and an RMS current $I_{RMS} Q2$ as given by Eq. (2-61).

(5) Secondary of the coupled inductor, L_{as}

According to Section 2.4.3, L_{as} should be as big as possible, so as to minimize the voltage stress (refer to Eq. (2-25)) and hence the turnoff losses in $Q2$. But a bigger L_{as} will also extend the energy releasing time.

From Eqs. (2-18) and (2-24), and with reference to Fig. 2.2, the energy releasing time is determined by

$$t_a - t_2 = \frac{I_{ap}}{V_{in}} \sqrt{L_{ap} L_{as}} \quad (5-26)$$

In order to release the stored energy in the core completely within switching cycle. there should be a limitation,

$$t_a - t_2 < (1 - D_{aux}) T_s \quad (5-27)$$

Thus, from Eqs. (5-26) and (5-27), it is determined that

$$L_{as} < \frac{1}{L_{ap}} \left[\frac{(1 - D_{aux}) V_{in_min}}{f_s I_{ap}} \right]^2 \quad (5-28)$$

(6) Selection of the blocking diodes, D_1 and D_2

Both the diodes are fast recovery diodes with low voltage drop. D_1 is optional. and is only applicable to cases where the releasing current of L_{as} may reach zero before $Q1$ is turned OFF. or

$$t_a - t_2 = \frac{I_{ap}}{V_{in}} \sqrt{L_{ap} L_{as}} > D_{max} T_s \quad (5-29)$$

Without D_1 , the charged output capacitor of $Q2$ will discharge into $Q1$ after the turn-off of $Q2$, increasing the losses. Therefore D_1 is only dispensable in the design where Eq. (5-29) is valid.

D_1 should be selected so that it is able to handle a peak current of I_{ap} . As it is in parallel with $Q2$ when $Q1$ is ON and $Q2$ is OFF, thus, from Eq. (2-25), its voltage stress is

$$V_{R_{D1}} = \sqrt{L_{ap}/L_{as}} V_{m_max} \quad (5-30)$$

Similarly, D_2 should be able to handle a peak current of I_{as} given in Eq. (2-19). Its voltage stress is

$$V_{R_{D2}} = (1 + \sqrt{L_{as}/L_{ap}}) V_{m_max} + \sqrt{L_{as}/L_{ap}} V_o / n \quad (5-31)$$

5.2.3 A Design Example

A prototype flyback converter works under the following conditions:

- (i) Input voltage: $V_{m_max}=160$ V, and $V_{m_min}=90$ V
- (ii) Outputs: two outputs, (a) $V_{o1}=5$ V, $P_{o1}=10$ W, and (b) $V_{o2}=20$ V, $P_{o2}=20$ W. Total: 50W
- (iii) Permitted ripples in the outputs: $\Delta V_{o1}=50$ mV (i.e., 1%) , $\Delta V_{o2}=200$ mV (i.e., 1%)
- (iv) Maximum duty cycle: $D_{max}=0.4$
- (v) Switching frequency: $f_s=200$ kHz
- (vi) Auxiliary duty cycle: $D_{aux}=0.075$ (fixed by UC3855)
- (vii) Input capacitor voltage sustaining time: $\Delta t_{sus}=100/f_s$

Table 5.1 The parameters of the prototype flyback converter

parameter	selection	ratings	parameter	selection	ratings
n_1	1/18		$Q1$	IRFP450	500V, 14A, 0.4 Ω
n_2	1/5		C_{snb}	3.3 nF	
L_m	50 μ H		L_{ap}	15 μ H	
C_{o1}	220 μ F		L_{as}	90 μ H	
C_{o2}	100 μ F		$Q2$	IRF730	400V, 5.5A, 1.0 Ω
C_m	200 μ F		D_1, D_2	HFA08TB	600V, 8A
D_{o1}	MBR735	35V, 7.5A	Controller	UC3855	
D_{o2}	MBR810	100V, 8A			

Table 5.1 shows the design and selection of each component and device of the prototype converter, which is made by following the design procedure presented above.

5.3 DESIGN PROCEDURE OF THE FORWARD CONVERTER

The design of the forward converter is also based on the specifications of the application. Assume the following specifications and parameters are known.

D_{e_max} --Effective maximum duty cycle

f_s --Switching frequency, Hz

P_o --Full load output power, W

ΔV_m --permitted peak-peak ripples in V_m , V

V_{m_max} --Maximum input voltage, V

V_{m_min} --Minimum input voltage, V

V_o --Output voltage, V

ΔV_o --permitted peak-peak ripples in V_o , V

5.3.1 Design of the Power Circuit

The following design procedures are referred to the circuit shown in Fig. 2.1. All parameters are in SI units.

(1) **Turns ratios of the transformer, N_p/N_s , N_p/N_r**

From Eq. (3-75)

$$\frac{N_p}{N_s} = \frac{1}{n} = \frac{V_o}{V_{m_min} D_{e_max}} \quad (5-32)$$

where, D_{e_max} is the effective duty cycle of the main switch, i.e., $D_{e_max}=D-D_x$.

Taking into account the forward drop of the rectifier, it is modified as

$$\frac{N_p}{N_s} = \frac{1}{n} = \frac{V_o + V_F}{V_{m_min} D_{e_max}} \quad (5-33)$$

When $D_{e_max} < 0.5$, usually

$$\frac{N_p}{N_r} = 1 \quad (5-34)$$

If $D_{e_max} > 0.5$, to guarantee successful core resetting, the turns ratio should be

$$\frac{N_p}{N_r} \leq \frac{1}{1 - D_{e_max}} \quad (5-35)$$

(2) Output inductor, L_o

Assume the converter is at the boundary of the continuous conduction mode operation when its output power is a twentieth of P_o . Hence there is [23]

$$\frac{1}{20} \frac{P_o}{V_o} \geq \frac{D_{e_max}}{2 f_s L_o} (n V_{m_min} - V_o) \quad (5-36)$$

which gives

$$L_o \geq 10 \frac{D_{e_max} V_o}{f_s P_o} (n V_{m_min} - V_o) \quad (5-37)$$

(3) Output capacitor, C_o

The ripple voltage can be found as given by [23]

$$\Delta V_o = \frac{V_o}{8 f_s^2 C_o L_o} (1 - D_{e_max}) \quad (5-38)$$

Hence, C_o should be chosen as

$$C_o \geq \frac{V_o}{8 f_s^2 L_o \Delta V_o} (1 - D_{e_max}) \quad (5-39)$$

(4) Magnetizing inductance, L_m

Assume the magnetizing current accounts for less than one twentieth of the peak input current, that is,

$$I_m \leq \frac{1}{20} \frac{P_o}{V_{m_min} D_{e_max}} \quad (5-40)$$

Because,

$$I_m = \frac{V_{m_min}}{f_s L_m} D_{e_max} \quad (5-41)$$

Hence,

$$L_m \geq \frac{20 D_{e_max}^2 V_{m_min}^2}{f_s P_o} \quad (5-42)$$

(5) Selection of the main switch, $Q1$

The switch should be selected so that it has the lowest ON resistance among the product catalogue. The voltage rating is determined by Eq. (3-51) as

$$V_{DSS_Q1} \geq 2V_m \quad (5-43)$$

where, V_{DSS_Q1} is the drain to source breakdown voltage rating of $Q1$.

The rms current is determined by Eq. (3-85), and the average and peak current ratings are determined by

$$I_{D_Q1} > 1.5 \frac{P_o}{V_{m_min}} \quad (5-44)$$

$$I_{MD_Q1} > 1.5 \frac{P_o}{V_{in_min} D_{max}} \quad (5-45)$$

where, the constant 1.5 accounts for the worst case efficiency of 70%,

I_{D_Q1} is the continuous drain current rating, and

$I_{MD\ QI}$ is the pulse drain current rating.

(6) Selection of the output rectifier, D_{o1} and D_{o2}

The rectifiers should be fast rectifier diodes, Schottky diodes or synchronous rectifier MOSFETs. Their voltage rating is determined by

$$V_{R_Do} > nV_{in_max} \quad (5-46)$$

where V_{R_Do} is the reverse voltage rating.

Its current rating is determined by

$$I_{av_Do1} > \frac{P_o}{V_o} D_{max} \quad (5-47)$$

$$I_{av_Do2} > \frac{P_o}{V_o} (1 - D_{min}) \quad (5-48)$$

where, I_{av_Do1} and I_{av_Do2} are the average current rating of D_{o1} and D_{o2} , respectively.

(7) Selection of the input capacitor, C_m

The selection criterion for C_m is the same as Eq. (5-15).

5.3.2 Design of the Auxiliary Circuit

(1) Auxiliary duty cycle, D_{aux}

The maximum D_{aux} should be limited by Eq. (5-16) so as not to affect the resetting of the core of T_r . It should be noted that, in the case of the Forward converter topology, D_{aux} corresponds to half the resonant period of the network consisting of L_p , C_{snb} and T_r .

(2) Snubber capacitor, C_{snb}

The value of C_{snb} determines the rise time of the drain voltage of QI at its turnoff,

as described in Eq. (3-46). For a very short duration, it is approximated to

$$\Delta u_{Q1}(t) \approx \frac{n I_o}{C_{snb}} \Delta t \quad (5-49)$$

Limit the rise of u_{Q1} below V_m within the demanded time t_r . Thus, from Eq. (5-49),

$$C_{snb} \geq \frac{n I_o}{V_m} t_r \quad (5-50)$$

On the other hand, the rise time should not exceed the gap left by $2D_{max}$ and D_{aux} , which gives a limit

$$t_5 - t_4 \leq (1 - 2D_{max} - D_{aux}) T_s \quad (5-51)$$

Combining Eqs. (5-49) and (5-51),

$$C_{snb} \leq \frac{n I_o}{2V_m} (1 - 2D_{max} - D_{aux}) T_s \quad (5-52)$$

(3) Primary of the coupled inductor, L_{ap}

From Eqs. (3-3) and (3-16),

$$\omega_n = \sqrt{\frac{2}{L_{ap} C_{snb}}} \quad (5-53)$$

Because D_{aux} corresponds to a half of the resonant period, i.e.,

$$D_{aux} T_s = \frac{2\pi}{2} \sqrt{\frac{L_{ap} C_{snb}}{2}} \quad (5-54)$$

It gives

$$L_{ap} = \frac{2 D_{aux}^2}{\pi^2 f_s^2 C_{snb}} \quad (5-55)$$

The core of the coupled inductors should be selected so that it is able to handle the power given by Eq. (5-25), where I_{ap} is determined by Eq. (3-25).

(4) Additional inductor, L_s

From Eq. (3-17), it can be determined that

$$L_s = n^2 L_{ap} \quad (5-56)$$

L_s can be integrated into the secondary windings of the power transformer.

(5) Selection of the auxiliary switch, $Q2$

The on-resistance and inherent capacitances of $Q2$ should be low in the product catalogue. Its voltage rating is the same as of $Q1$. The current rating should be able to handle the peak discharging current I_{ap} given by Eq. (3-17), and an RMS current $I_{RMS\ Q2}$ given by Eq. (3-87), and an average current given by Eq. (3-88).

(6) Secondary of the coupled inductor, L_{as}

From Eq. (2-37), L_{as} should be large in value so as to reduce the turnoff voltage stress on $Q2$. However, Eq. (5-27) should also be satisfied so as to release the energy stored in the core of the coupled inductor within one switching cycle. From Eqs. (3-22), (3-25), (3-31) and (5-27),

$$L_{as} \leq \left(\frac{1 - D_{aux}}{D_{aux}} \right)^2 L_{ap} \quad (5-57)$$

(7) Selection of the blocking diodes, D_1 & D_2

D_1 and D_2 should be able to handle a peak current of I_{ap} and I_{as} , respectively. Their voltage ratings should be higher than their voltage stress given by Eqs. (2-23) and (5-32), respectively.

5.3.3 A Design Example

The specifications of the prototype forward converter is as follows.

- (i) Input voltage: $V_{in_max}=75$ V, and $V_{in_min}=35$ V
- (ii) Output: $V_o=5$ V, $P_o=100$ W
- (iii) Permitted ripple in the output: $\Delta V_o=50$ mV (i.e., 1%)
- (iv) Maximum duty cycle (effective): $D_{e_max}=0.4$
- (v) Switching frequency: $f_s=300$ kHz
- (vi) Auxiliary duty cycle: $D_{aux}=0.075$ (fixed by UC3855)
- (vii) Input capacitor voltage sustaining time: $\Delta t_{sus}=100/f_s$

Table 5.2 shows the design and selection of each component and device of the prototype converter, which is made by following the design procedure presented above. The design of the synchronous rectification stage is based on the design procedure presented in [18].

Table 5.2 The parameters of the prototype forward converter

parameter	selection	ratings	parameter	selection	ratings
n	1/3		C_{smb}	10 nF	
N_p/N_r	1/5		L_{op}	3 μ H	
L_m	120 μ H		L_{as}	90 μ H	
C_o	200 μ F		L_s	330 nH	
C_m	200 μ F		$Q2$	IRF640	200V, 18A, 0.18 Ω
D_{o1}, D_{o2}	MTP75N05*	50V, 75A, 9.5m Ω	D_2, D_r	HFA08TB	600V, 8A
$Q1$	IRF640*	200V, 18A, 0.18 Ω	Controller	UC3855	

* Two in parallel in order to reduce the conduction losses in the switch.

5.4 GATING GENERATION FOR THE AUXILIARY SWITCH

UC3855 can be directly employed as the PWM control chip of the proposed converters. It produces two gating signals to drive the main and auxiliary switches. The auxiliary gating signal has a fixed duty cycle of about 0.075. The major features of UC3855 include (i) average current mode control, allowing better stability and easier control loop design, and (ii) internal current synthesizer, simplifying the current sensing method (see Appendix I).

A problem in using UC3855 is that the auxiliary duty cycle is not adjustable. As a result, the auxiliary duty cycle may not be the optimal one, which will result in the least losses in the auxiliary circuit. Another problem is that UC3855 is expensive as compared to most of the single output PWM chips.

When a PWM chip of single output is selected as the control chip, gating for the auxiliary switch can be generated with an additional sub-circuit as presented below.

5.4.1 Gating pattern generation by additional logic and drive circuit

Fig. 5.2 shows an example of the simple implementation of the auxiliary gating pattern. It consists of a Schmitt trigger, a Op-Amp, inverters and AND gates. Other logic combinations exist but the function it fulfills is the same: to split the original PWM pulse from the single output PWM chip into two pulses: one for the auxiliary switch and the other for the main switch. The additional logic and drive circuits form a splitter.

Fig. 5.3 shows key waveforms at the indicated points in Fig. 5.2. The auxiliary duty cycle is adjusted by varying the time constant of the R_B - C_B network of Fig. 5.2.

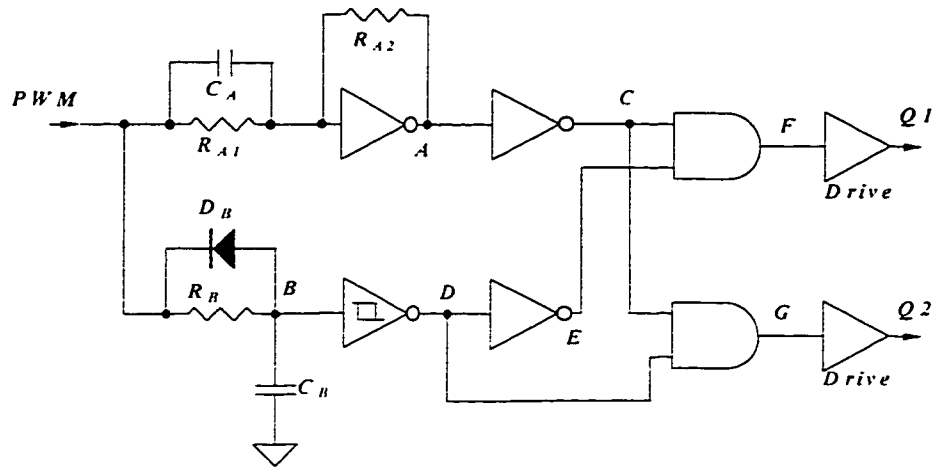


Fig. 5.2, The gating generation circuit, a splitter, which generates the auxiliary gating on basis of the original PWM signal

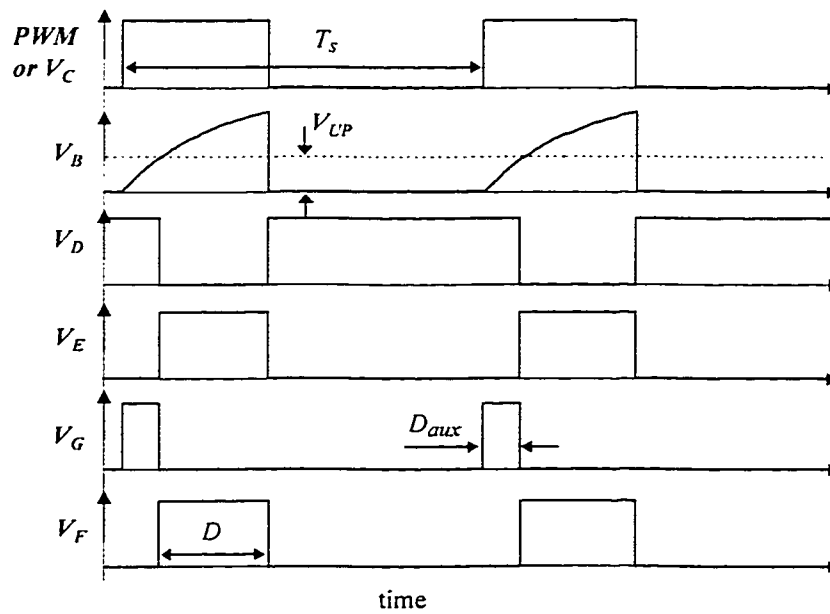


Fig. 5.3, The operational waveforms in the splitter: voltage waveform at the corresponding point in Fig. 5.2

In Fig. 5.3, V_F and V_E appear to have the same wave shape. The AND gate between point E and F , seemingly unnecessary, is of practical importance. This is because all the gates have delays in their response. In order to synchronize the two gating signals to an accurate timing sequence, a symmetrical structure in the splitter is required, which results in the least difference in delay for the two output gating signals.

5.4.2 The design of the splitter

(1) Selection of R_B , C_B and D_B

The duty cycle of the auxiliary switch, or the pulse width of the auxiliary gating signal, can be set by the proper value of R_B and C_B in the splitter in Fig. 5.2. The following equation should be satisfied

$$V_{UP} = V_{PWM} [1 - \exp(-\frac{D_{aux} T_s}{R_B C_B})] \quad (5-58)$$

where V_{PWM} is the high voltage level from the PWM chip output.

Eq. (5-58) yields

$$R_B C_B = -\frac{D_{aux} T_s}{\ln(1 - \frac{V_{UP}}{V_{PWM}})} \quad (5-59)$$

The diode D_B is introduced to follow the fast drop of PWM signals. It should be a fast diode.

(2) The voltage divider, R_{A1} and R_{A2}

Because V_{PWM} is usually about 10~15V, while the high output voltage V_{OH} (logical level) is usually 6V, a direct connection of V_{PWM} to the logic circuit may destroy it. Therefore, the linear voltage amplifier is inserted between the PWM output and the logic

circuit. The magnitude of the amplification is less than one, and should obey the relation:

$$\frac{R_{A2}}{R_{A1}} = \frac{V_{OH}}{V_{PWM}} \quad (5-60)$$

An additional capacitor C_A is introduced to balance the stray capacitors of R_{A1} and R_{A2} , making the amplifier a purely linear device. Its value is decided experimentally.

(3) The selection of the logic gates and the driver

All the logic gates should be capable of high speed response. CMOS logic circuits are suitable for the splitter. High speed drivers should be selected.

5.4.3 A Design Example

Table 5.3 shows the parameters of the splitter of Fig. 5.2 in a design example. UC2844 is used as the PWM control chip. It has only one gate drive. The splitter is thus employed to generate the gate drive for the auxiliary switch. Fig. 5.4 shows the experimental results of the gating signals, which verify the design.

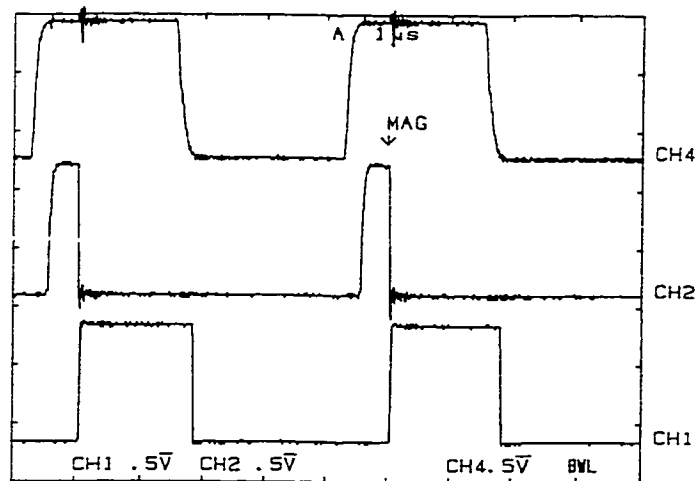


Fig. 5.4 The experimental results of the gating patterns generated by the splitter of Fig. 5.2.

channel 1: original PWM signal from UC2844

channel 2: gating for auxiliary switch $Q2$

channel 3: gating for main switch $Q1$

Table 5.3 The parameters of the splitter in a design example

parameter		parameter	
R_{A1}	180 k Ω	D_B	IN4148
R_{A2}	91 k Ω	Inverters*	TC74HC04P
CA	0.22 μ F	AND gate	MC74HC08A
R_B	2.2 k Ω	Drivers	IR2110
C_B	500 nF		

* The Schmitt trigger and the Op-amp are substituted with inverters in the example.

CHAPTER 6

CONCLUSIONS

6.1 SUMMARY

This thesis has discussed zero voltage switching (ZVS) flyback and forward converter topologies. Such a topic is of special importance, because both the topologies are very popular in industrial applications, especially in the distributed power systems of the advanced communication and computer networks.

This thesis can be summarized as follows. In chapter 1, existing ZVS flyback and forward converter topologies are briefly reviewed and their drawbacks are summarized. These topologies lose ZVS at light load, require complicated gate drive schemes, achieve ZVS at the cost of increasing the conduction losses, have restrictions on use due to patents.

In Chapters 2 and 3, ZVS flyback and forward converter topologies which employ an auxiliary circuit have been presented. The modes of operation of each circuit is identified. During each switching cycle, the flyback converter operates in five distinct intervals and the forward converter operates in seven intervals. By selecting the values of

the snubber capacitor and the coupled inductors, ZVS can be always achieved. Steady state analysis is performed, and the factors influence the performance of the circuit is investigated. Experiments on the prototype converters are carried out and the analysis and design are verified.

In Chapter 4, the small signal models and closed loop stability are discussed. Transients responses are obtained experimentally. Finally, in Chapter 5, design procedures of both converters and of the gating pattern generation for the auxiliary switch are presented and design examples are given.

6.2 CONCLUSIONS AND CONTRIBUTIONS

The following conclusions can be made.

- (i) The auxiliary circuit is simple, and only a few low power rating components and devices are required.
- (ii) The gate drive scheme for the auxiliary switch is simple. No isolated, variable duty cycle gate drive is required by the auxiliary switch.
- (iii) ZVS can be always achieved whatever line/load conditions, and no conduction losses are increased.
- (iv) The prototype flyback converter has about 7% higher efficiency than its hard switching counterpart. The efficiency is measured under the following conditions: switching frequency is 200 kHz, input dc line voltage range is from 90 V to 160 V, two outputs, one of which is 10 W at 5 V and the other is 40 W at 20V.

(v) The prototype forward converter has about 5% higher efficiency than its hard switching counterpart. The efficiency is measured under the following conditions: switching frequency is 300 kHz, input dc line voltage range is from 40V to 60V, the load power is 100 W at 5 V, synchronous rectifiers are employed.

(vi) The small signal analysis show that the flyback converter can utilize the small signal model previously developed for the conventional flyback. The forward converter has a pole proportional to the switching frequency and the additional inductance inserted into the secondary circuit. The closed loop design based on the derived model has a good dynamic response.

(vii) The disadvantage of the auxiliary circuit is that it has hard switching at turn-off, though the losses associated with it can be reduced by increasing the ratio of the two coupled inductors.

The major contributions of this thesis include:

- (i) Systematically analyses of the proposed converters are performed,
- (ii) Design procedures are developed,
- (iii) Prototype converters are built and experiments are carried out and the analysis and design are verified experimentally,
- (vi) Higher efficiencies have been obtained.

6.3 SUGGESTIONS FOR FUTURE WORK

The following suggestions can be made for future work.

- (i) The results obtained in this thesis have shown the advantage of the proposed converters. The prototype converters on printed circuit board (PCB) should be built and use optimal magnetics to further optimize the performance.
- (ii) To further improve the efficiency, new synchronous rectification techniques with resonant gate drives must be investigated in the proposed circuit topology.

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APPENDIX I

THE CONTROL CHIP UC3855



UC1855A/B
UC2855A/B
UC3855A/B

PRELIMINARY

High Performance Power Factor Preregulator

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Fixed Frequency Average Current Mode Control Minimizes Line Current Distortion
- Built-in Active Snubber (ZVT) allows Operation to 500kHz, improved EMI and Efficiency
- Inductor Current Synthesizer allows Single Current Transformer Current Sense for Improved Efficiency and Noise Margin
- Accurate Analog Multiplier with Line Compensator allows for Universal Input Voltage Operation
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Overvoltage and Overcurrent protection
- Two UVLO Threshold Options
- 150µA Startup Supply Current Typical
- Precision 1% 7.5V Reference

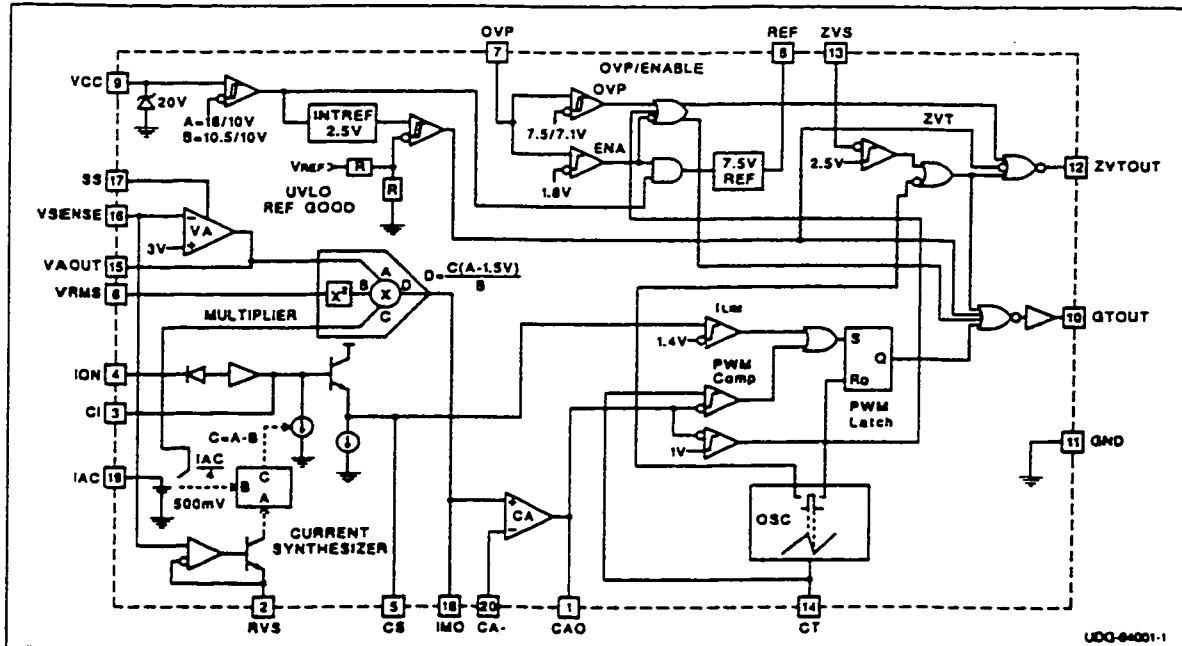
DESCRIPTION

The UC1855A/B provides all the control features necessary for high power, high frequency PFC boost converters. The average current mode control method allows for stable, low distortion AC line current programming without the need for slope compensation. In addition, the UC1855 utilizes an active snubbing or ZVT (Zero Voltage Transition technique) to dramatically reduce diode recovery and MOSFET turn-on losses, resulting in lower EMI emissions and higher efficiency. Boost converter switching frequencies up to 500kHz are now realizable, requiring only an additional small MOSFET, diode, and inductor to resonantly soft switch the boost diode and switch. Average current sensing can be employed using a simple resistive shunt or a current sense transformer. Using the current sense transformer method, the internal current synthesizer circuit buffers the inductor current during the switch on-time, and reconstructs the inductor current during the switch off-time. Improved signal to noise ratio and negligible current sensing losses make this an attractive solution for higher power applications.

The UC1855A/B also features a single quadrant multiplier, squarer, and divider circuit which provides the programming signal for the current loop. The internal multiplier current limit reduces output power during low line conditions. An overvoltage protection circuit disables both controller outputs in the event of a boost output OV condition.

Low startup supply current, UVLO with hysteresis, a 1% 7.5V reference, voltage amplifier with softstart, input supply voltage clamp, enable comparator, and overcurrent comparator complete the list of features. Available packages include: 20 pin N, DW, Q, J, and L.

BLOCK DIAGRAM



License Patent from Pioneer Magnetics. Pin numbers refer to DIL-20 J or N packages.

APPENDIX II

SCHEMATICS OF THE PROTOTYPE CONVERTERS

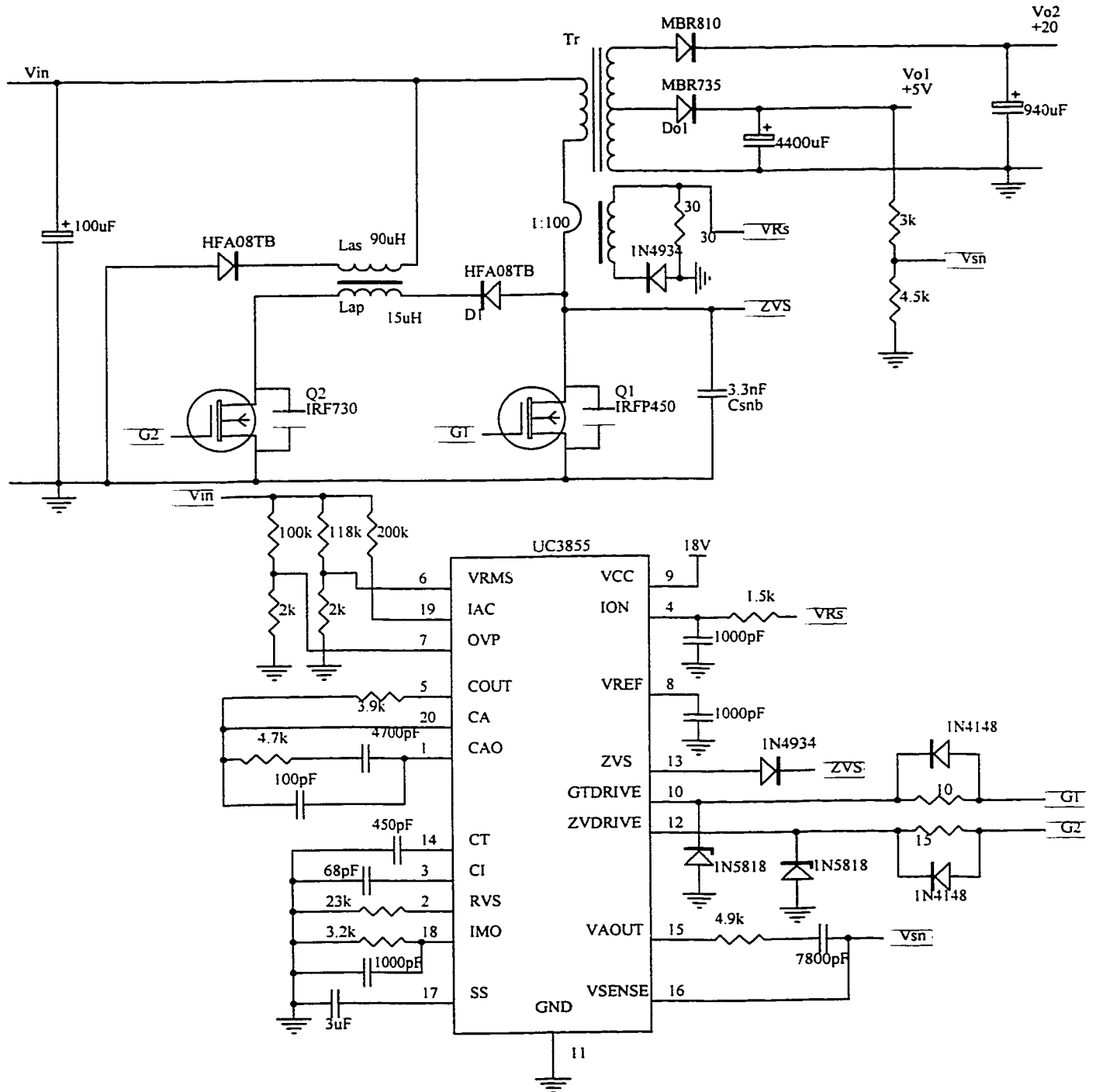


Fig. II.1 Prototype flyback converter

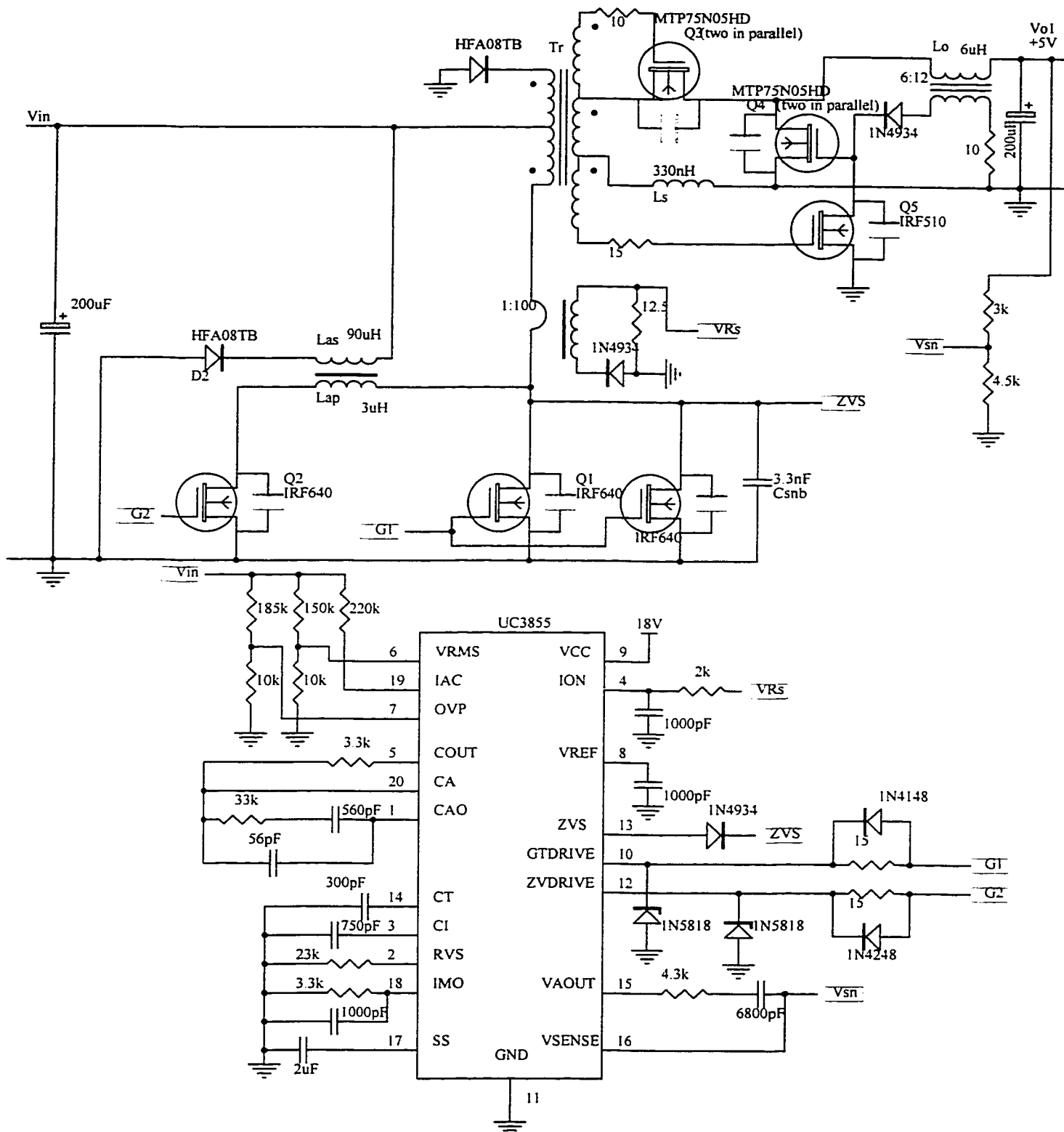


Fig. II.2 Prototype forward converter