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HIGH FREQUENCY SWITCHING PARALLEL PROCESSING TOPOLOGY FOR AC UNINTERRUPTIBLE POWER SUPPLY

Hai Bo Zhang

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements
for the Degree of Master of Applied Science at
Concordia University
Montréal, Québec, Canada

August 1997

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ABSTRACT

HIGH FREQUENCY SWITCHING PARALLEL PROCESSING TOPOLOGY FOR AC UNINTERRUPTIBLE POWER SUPPLY

Hai Bo Zhang

This thesis presents the description , analysis and design of a high frequency parallel processing ac uninterruptible power supply. Compared to the standard UPS system used today, the proposed system has higher efficiency, smaller size and less weight, this is due primary to the usage of a high-frequency switching topology.

The main power circuit configuration is shown to describe the steady state behaviour of the system in both ac line supply and battery backup modes of operation. A stability analysis is developed to describe the system behaviour against the load variation and the input disturbance. The detailed design of the output voltage control loop is carried out. A transient analysis is presented to describe the transition between the two operation modes of ac line supply and dc battery backup. From this analysis a fast switching transition control circuit is designed. A design procedure is illustrated to select the system components for a 300W UPS. The corresponding system performance such as efficiency is evaluated. All the theoretical results obtained in this thesis are experimentally verified.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my supervisor, Dr. P. K. Jain, for his guidance, encouragement, friendship and support, during the course of this study.

I would like to thank my colleagues at Power Electronics Laboratory very much for their kindness and help in every aspect, and for the numerous valuable discussions we have shared.

Finally, I would like to express my thanks to my wife and my dearest parents for their everlasting love, spirtual encouragement and strong support, during these years.

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LIST OF ACRONYMS

AWG	American Wire Gauge
ac	Alternative Current
dc	Direct Current
KVL	Kirchhoff's Voltage Law
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PID	Proportional-Integral-Differential network
PWM	Pulse Width Modulation
rms	Root Mean Square value
UPS	Uninterruptible Power Supply

LIST OF PRINCIPAL SYMBOLS

A_c bobbin winding area of the transformer

A_e core effective area of the transformer

B_{max} peak operating flux density

C_b capacitance of the filter in the battery charging converter

C_{df} detecting filter capacitance

C_f capacitance of the output dc filter

C_i capacitor, i - the series number of the capacitor in the circuit

D conducting ratio of the MOSFET

D operating current density

D_i diode, i - the series number of the diodes in the circuit

D_{Qi} diode antiparallel with the MOSFET inside, i - the series number of the MOSFET in the circuit

DB_1 input voltage detecting rectifier bridge

f_m modulation frequency in the high-frequency rectifier

f_s switching frequency

G(s) transfer function

$G_c(s)$ compensator transfer function

I_D drain current of the power MOSFET

$I_{F(AV)}$ average rectified forward current of the diode

I_{FD} forward current pass through the diode

I_{hb} current pass through the half-bridge inverter

I_{ir} input ac current

I_{o_ac} output ac current

I_{or} current pass through the high-frequency output rectifier diode

I_{pp} current pass through the push-pull inverter

i_{Lf} instantaneous current pass through the filter inductor

K_a constant of the relation between the V_{o_ac} and V_{o_dc}

K_f constant of the feedback path

L_b inductance of the filter in the battery charging converter

L_f inductance of the output dc filter

N_i winding of the high-frequency transformer, i - the series number of the windings

n transformer turns ratio

P_{acl} total power loss in the normal power supply mode

P_{bal} total power loss in the backup power supply mode

P_{b_ac} power of the battery charging converter

P_{fdcl} conducting power loss of the ultrafast recovery diode

P_{fdtl} turn-on power loss of the ultrafast recovery diode

P_{hb} output power of the half-bridge inverter

P_{hbl} total power loss in the half-bridge inverter

P_{hbcl} conducting power loss in the half-bridge inverter

P_{hbsl} switching power loss in the half-bridge inverter

P_{i_ac} total input ac power

P_{ir} output power of the input rectifier

P_{irl} total power loss in the input rectifier

P_{mtl} total power loss of the main high-frequency transformer

P_{o_ac} output power

P_{o_dc} output dc power

P_{orl} total power loss in the high-frequency output rectifier

P_{pp} output power of the push-pull inverter

P_{ppl} total power loss in the push-pull inverter

P_{ppcl} conducting loss in the push-pull inverter

P_{ppsl} switching loss in the push-pull inverter

P_{qscl} conducting power loss in the quasi-square wave inverter

P_{qssl} switching power loss in the quasi-square wave inverter

P_{qsl} total power loss in the quasi-square wave inverter

$R_{DS(on)}$ MOSFET static drain-source on-resistance

R_L rated load resistance

Q_i power MOSFET, i - the series number of the power MOSFET in the circuit

T_{ac} period of input ac power supply

T_{bat} period of battery power supply

T_{ds} period of detecting signal delay

T_{o_ac} cycle of the output ac voltage

T_B flyback transformer for battery charging

T_D ac line voltage detecting transformer

T_M main high-frequency transformer

T_m cycle of the modulation frequency

T_s cycle of the switching frequency

t_r rise time of the power MOSFET

t_f fall time of the power MOSFET

t_{rr} reverser recovery time of the diode

V_{b_dc} battery dc voltage

V_{c_ac} input ac voltage for the battery charging converter

V_{cc} voltage of auxiliary power for the IC chips

V_{c_dc} dc voltage after the rectifier diode of the battery charging converter

V_{DS} voltage across the MOSFET drain-source

V_{ds} Voltage of ac line voltage detecting signal

V_{h_ac} output voltage of the half-bridge inverter

V_{i_ac} input ac line voltage

V_{i_dc} output dc voltage of the input ac rectifier

V_{Ni} voltage on the high-frequency transformer windings, i - the series number of the windings

V_{o_dc} output dc voltage

V_{o_ac} output quasi-square wave voltage

V_R dc blocking voltage of the diode

V_r ripple voltage on the V_{i_dc}

V_{r_dc} output dc voltage of the high-frequency rectifier

V_{ref} reference voltage in the system

V_s control voltage

V_{t_ac} input ac voltage of the high-frequency rectifier

V_{TH} high threshold voltage of the hysteresis comparator

V_{TL} low threshold voltage of the hysteresis comparator

v_1 voltage on the primary winding of the flyback transformer

v_2 voltage on the secondary winding of the flyback transformer

$v_{i\_dc}(t)$ instantaneous voltage after the input rectifier diode

v_{Lf} instantaneous voltage of the filter inductor

v_{r_dc} instantaneous output voltage of the high-frequency rectifier

ΔI_{o_dc} ripple current of the dc output

ΔV_{o_dc} ripple voltage of the dc output

δ duty ratio

ϕ magnetic flux

τ_d time constant of ac line voltage detecting circuit

τ_f time constant of the input rectifier circuit

η_{ac} system efficiency in the normal power supply mode

η_{dc} system efficiency in the backup power supply mode

ω_o angular frequency of the output ac voltage

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Uninterruptible power supply (UPS) is designed to provide continuous power to the load during utility power interruptions. Presently there are two basic UPS topologies: off-line and on-line. Each topology can feature one or more technical variations described in details in Section 1-2, although the basic operation is about the same within each group.

All UPS systems use an internal battery that produces ac power via an inverter. The off-line UPS is the simplest form of backup power system. The inverter is normally off. The off-line UPS is also known as a standby power source. The on-line UPS is continuously converts ac utility power to dc by an ac-to-dc converter to provide battery charging. The dc bus is supported by the battery and feeds a dc-to-ac inverter with appropriate filtering. The on-line UPS provides the highest level of protection since it continuously supplies ac power, regardless of the utility line condition [1] [2] [3].

A new UPS topology, which is called a "parallel-processing UPS"[4] [5], combines with two advantages of both the off-line and on-line topologies, such as high

efficiency, ac-input voltage regulation, and continuity of output power during any type of ac-input power disturbance.

This chapter will introduce characteristics of the parallel-processing UPS topology compared with the other topologies. Then a high-frequency switching parallel-processing system is proposed.

1.2 TOPOLOGIES OF UPS

1.2.1 Off-line UPS

An off-line UPS is shown in Fig. 1-1. In this system, the ac-input power, when acceptable, flows through a transfer switch directly to the UPS's output. The inverter is off, standing by, and is disconnected from the output. A separate low-power recharge rectifier floats the battery. During ac-input power disturbances, the transfer switch disconnects the ac-input and connects the inverter to the UPS's output, usually in a break-before-make sequence. The inverter is then activated.

A standby system can be very small and efficient because the inverter is normally off, the transfer switch has negligible conduction loss, and the recharge rectifier's capacity is designed for only about 10% of UPS rated power. Many low-power, standby UPSs have recently appeared, most of which use a square wave or quasi-square wave inverter, and are intended for a single personal computer application. A standby system suffers from a long "transfer time" due to the detection and switching action of the transfer switch's sequential operation. Also, this system usually has no ac-input voltage

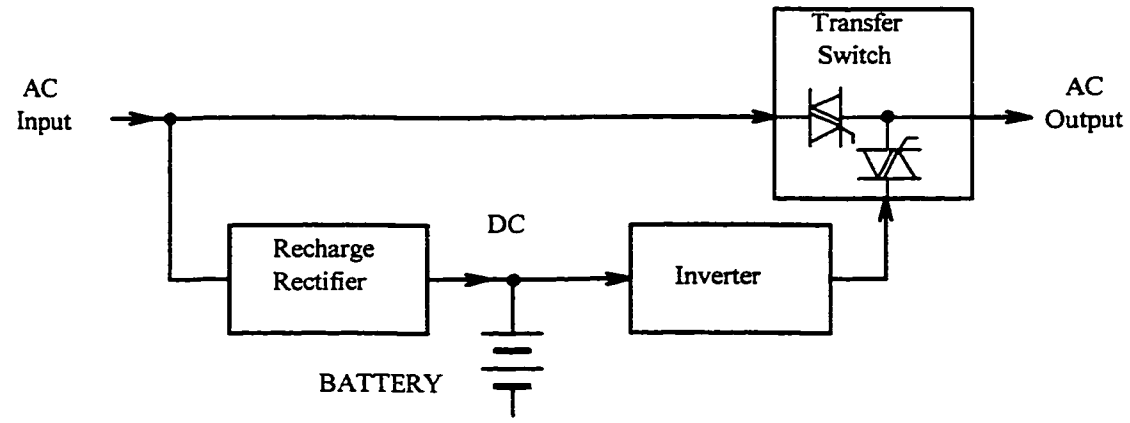


Fig. 1-1 Off-line ac-uninterruptible power supply.

regulation and must synchronize its inverter to the ac-input voltage for continuity of phase during transfer switch operation.

1.2.2 On-line UPS

The on-line UPS is shown in Fig. 1-2. In this system, the ac-input power, when acceptable, passes through a rectifier that converts the ac-input voltage to a regulated dc voltage. A portion of the rectifier's dc-output power recharges the battery. The remainder of the dc power immediately passes through an inverter that reconverts the dc voltage to the ac-output voltage. The inverter continuously provides power to the UPS's output. During ac-input power disturbances, the system's battery supplies the dc power to the inverter.

The on-line UPS has almost total separation between utility ac input and ac output. This provides good noise immunity, ac-input voltage regulation, and continuous

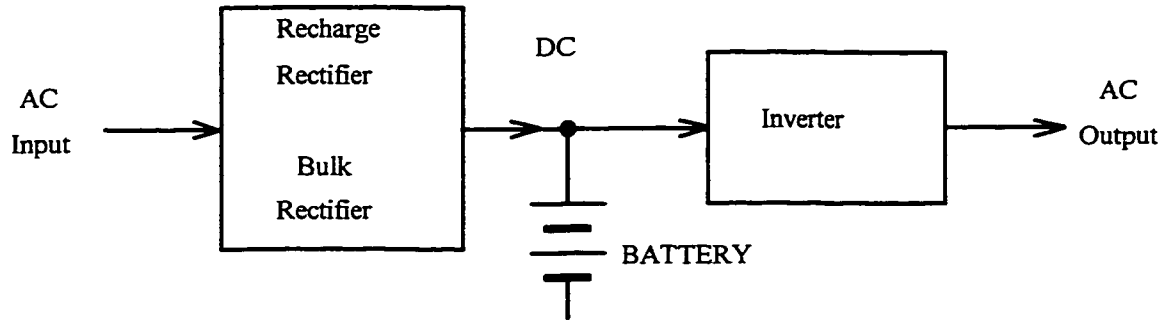


Fig. 1-2 On-line ac-uninterruptible power supply.

output power when the ac-input power fails. This traditional system has been used in critical applications for many years. However, this system suffers from poor operating efficiency due to the double power conversion between input and output when the ac-input power is acceptable. It is also complex due to the need for a high-power, well-regulated rectifier to provide normal inverter power and recharged current while accurately floating the battery.

1.2.3 Parallel processing UPS

The system shown in Fig. 1-3 is a "parallel-processing" UPS. The ac-input power, when acceptable, passes through an ac parallel-processing element that filters and regulates the amplitude of the ac-input voltage. The power then passes directly to the UPS's output. An inverter and recharge rectifier are electrically connected to the element, but if the ac-input power is acceptable, the inverter does not deliver power to the load and the rectifier recharges or floats the batteries. The delivery of inverter power is controlled

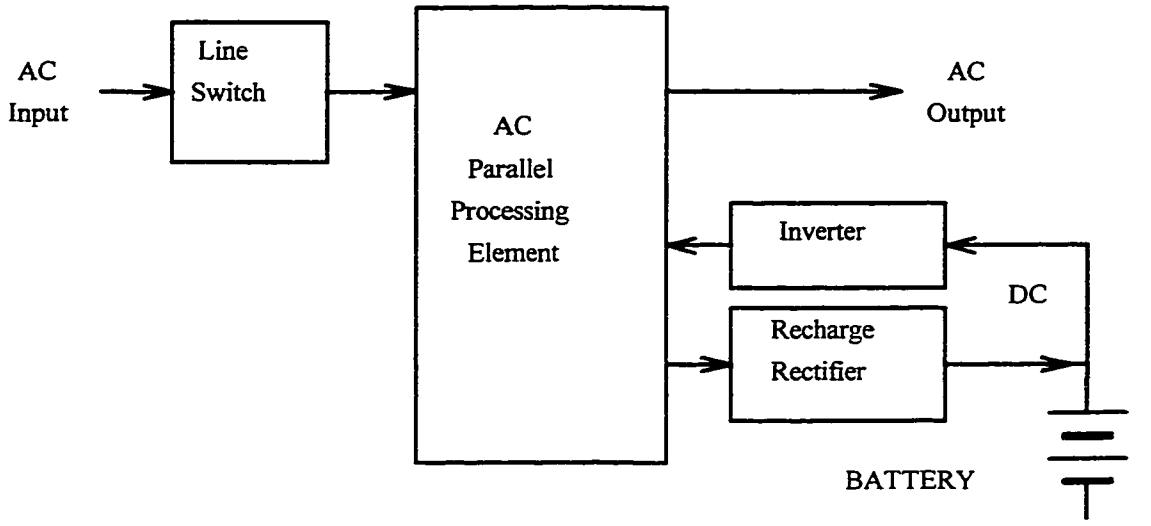


Fig. 1-3 Parallel processing ac-uninterruptible power supply.

by adjusting the inverter's output phase or inhibiting the inverter output. A line switch disconnects the element from the ac input when the inverter is delivering power. During ac-input power disturbances, the UPS's control circuit ensures continuity of the UPS's output power by appropriately phase shifting or activating the inverter.

The parallel-processing system combines the features of a high operating efficiency, ac-input voltage regulation, and continuous output power during ac-input power disturbances.

1.3 HIGH-FREQUENCY SWITCHING PARALLEL PROCESSING UPS

The parallel processing UPS topology does provide higher operating efficiency, ac-input voltage regulation, and continuous output power during ac-input power disturbances, however, problems such as input/output isolation and heavy weight are still present.

Considering the advantages of high-frequency switching topologies, the improvement of the high efficiency parallel processing UPS system is proposed to overcome the above mentioned problems. The system is shown in Fig. 1-4.

The ac-input power, when acceptable, is rectified to dc voltage, which is then chopped into high frequency ac voltage by the PWM (Pulse Width Modulation) inverter 1. Through the high frequency isolation transformer, the power is transferred to the output side and rectified to a more stable dc voltage. Finally this voltage is inverted to a low frequency quasi-square wave voltage. While ac-input power is interrupted, the UPS's control circuit ensures continuity of the UPS's output power by the PWM inverter 2 in the battery side. The parallel processing element is a multi-winding isolated high-frequency transformer. A recharge converter is electrically connected to the element and by which the battery is recharged or floating recharged from the ac input power. However, it is inhibited to function while battery is backup the power to the output. The output power can be regulated by PWM controller against to the variations of the ac-input

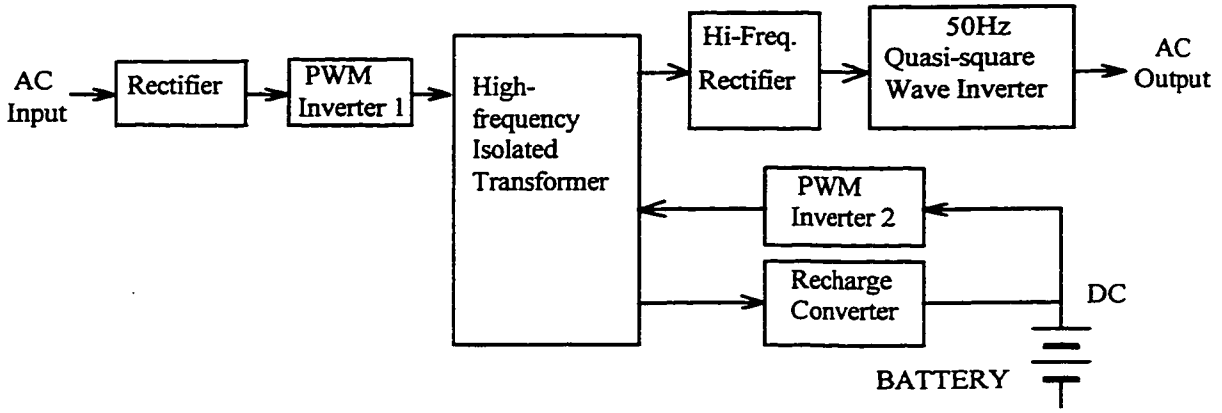


Fig. 1-4 High-frequency switching parallel processing UPS.

or dc-battery power in terms of the voltage level, frequency, phase, and waveform. Compared with the normal parallel processing UPS topology, the high switching frequency topology makes the proposed system become light weight and small size, however, at the cost of having an extra rectifier and PWM inverter at the ac input side.

Compared to the performance with the off-line, on-line and normal parallel UPS, the advantages and disadvantages of the high-frequency switching parallel processing UPS are listed as follows:

Advantages:

(i) Regulated output voltage;

(ii) Immunity, against noise from ac input;

(iii) Isolation between the ac-input power and ac-output power;

(iv) Continuous output power when the ac-input power fails;

(v) Small size, light weight, and low cost;

(vi) The system efficiency is higher than the on-line UPS system;

(vii)No strict limitation for the phase synchronization between the ac-input power and the ac-output power.

Disadvantages:

(i) The design of the high frequency transformer is a little bit more complicated;

(ii) The system efficiency is lower than the off-line UPS system.

1.4 SCOPE AND OBJECTIVES

High-frequency switching parallel processing UPS system is the research topic in this thesis with the emphasis on improving the efficiency, size, weight and cost. The main objectives of this thesis are:

(i) To propose a novel topology;

(ii) To develop the steady state and transient analysis;

(iii) To illustrate a design procedure; and

(iv) To demonstrate the system performance.

1.5 THESIS OUTLINE

Chapter 2 presents the circuit configuration of a high-frequency switching parallel processing UPS. The power flow during the two operation modes of ac line power supply and battery backup supply is analysed. The experimental steady state waveforms of the two operation modes are shown.

Chapter 3 shows the design of the output voltage control loop. A stability analysis is developed to describe the system behaviour against the load variation and the input disturbance. The theoretical results are verified experimentally.

Chapter 4 shows the analysis of the transition between two operation modes and the design of a corresponding transition control circuit. The experimental results illustrate the system transition performance.

Chapter 5 discusses the design procedure to select the power components and evaluates the power losses of the system. The theoretical system efficiency is verified experimentally.

Finally in Chapter 6, the main contributions of this thesis are outlined.

CHAPTER 2

HIGH-FREQUENCY SWITCHING PARALLEL PROCESSING AC UPS

2.1 INTRODUCTION

This chapter presents the configuration of the proposed high-frequency switching parallel processing UPS based on a 300W consumer UPS system. The system consists of seven parts: ac-input rectifier, half-bridge inverter, push-pull inverter, parallel processing element, high frequency rectifier, quasi-square wave inverter, and battery charging converter. Each part is described and analysed in this chapter. Two operating modes of ac line power supply or battery power supply are considered.

In Section 2.2, each function part of the main power system circuit is described and analysed. In Section 2.3, two operation modes of normal power supply (ac to ac) and backup power supply (dc to ac) are discussed. In Section 2.4, two converter topologies, half-bridge converter and push-pull converter, are analysed. The operating principle of the quasi-square wave inverter for the output is described in Section 2.5. The battery charging converter is discussed in Section 2.6. Finally, the experimental steady state waveforms of the two operation modes are shown.

2.2 MAIN POWER CIRCUIT CONFIGURATION

A 300W UPS circuit diagram of high-frequency switching parallel processing topology is illustrated in Fig. 2-1. The basic functions of the seven parts in the circuit diagram are described as follows:

2.2.1 Ac input rectifier

Ac input rectifier consists of ac input rectifier diode bridge and the filter capacitors. The rectifier diode bridge, D_1 - D_4, converts the single phase input ac line voltage V_{i_ac} into dc voltage V_{i_dc} at its output terminal. This dc voltage feeds the half-bridge inverter while the UPS system is operating under ac to ac mode. C_1 and C_2 divides the input dc voltage V_{i_dc} into half which is the basic request for the half-bridge inverter.

2.2.2 Half-bridge inverter

The half-bridge inverter consists of two MOSFETs (Q_1 and Q_2) and the primary winding N_1 of the main high-frequency transformer which is known as the parallel processing element. The top Q_1 and the bottom Q_2 conduct alternatively for maximum 45° (δ_{max}) per cycle. Consequently a high frequency PWM voltage is generated on the winding N_1, which one terminal connects to the joint of the two MOSFETs and another terminal connects to the centre joint of two filter capacitor, C_1 and C_2. The pulse width is regulated by the special control chip, UC3526A [Appendix 1].

As described above, the half-bridge circuit inverts V_{i_dc} to the high frequency square voltage V_{h_ac} to provide the power for the main transformer while the input ac line

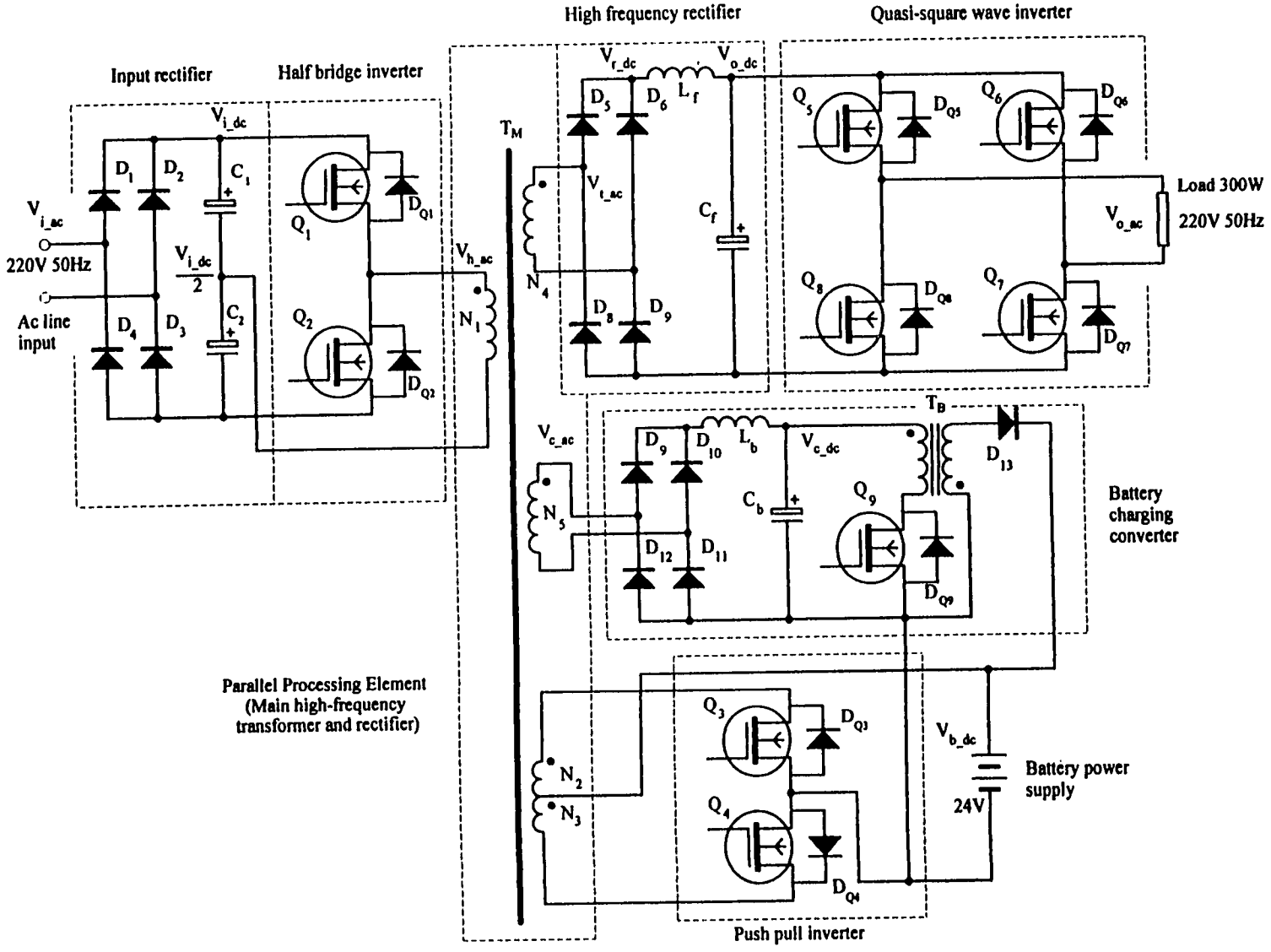


Fig. 2-1 The main power circuit diagram of the high frequency switching parallel processing UPS.

voltage is normal. The diodes D_{Q1} and D_{Q2} in antiparallel with the MOSFETs Q_1 and Q_2 are used as commutating diodes for protecting the switches.

2.2.3 Push-pull inverter

The push-pull inverter is arranged by two MOSFETs (Q_3 and Q_4) and the windings N_2 & N_3 of the main high-frequency transformer. Q_3 and Q_4 are symmetric and conduct alternatively for maximum 45° (δ_{max}) per cycle. A high frequency PWM magnetic flux is generated in the main transformer ferrite core. The pulse width is regulated by the same special control chip UC3526A. Therefore, the push-pull circuit inverts V_{b_dc} to high frequency square wave voltage, which supplies the power to the main transformer when input ac line fails.

2.2.4 Parallel processing element

Parallel processing element combines the power from two different inverters in one element. This is realised by a high frequency transformer with a ferrite core. The parallel processing element is also named as Main Transformer T_M. Under the proper control of the logic circuit, the operation of the main transformer is described as follows:

(i) During the operation mode of the normal power supply, the main transformer boosts V_{h_ac} which is generated by half-bridge inverter to the rated output voltage V_{t_ac}. At the same time, winding N_4 of the main transformer transfers the power to the battery charging converter.

(ii) During the operation mode of the backup power supply, the main transformer boosts V_{N2} and V_{N3} which are generated by the push-pull inverter to the rated V_{t_ac}.

The diodes D_{Q3} and D_{Q4} in antiparallel with the MOSFETs Q_3 and Q_4 are used as free wheel diodes for protecting the switches.

2.2.5 Output High frequency rectifier

Ultrafast recovery diodes D_5 - D_8 constitute a high frequency bridge rectifier, and a filter circuit with inductor L_f and capacitor C_f is connected on the dc side. The high frequency square wave voltage, V_{t_ac}, on the output of the main transformer is converted to dc voltage by D_5 - D_8. The inductor L_f smoothes the dc current and the value is chosen based on the allowable ripple current. The capacitor C_f filters out the ripple voltage and maintains the constant output dc voltage, V_{o_dc}, for the quasi-square wave inverter.

2.2.6 Quasi-square wave inverter

Quasi-square wave inverter inverts the dc voltage V_{o_dc} to 50Hz ac quasi-square wave voltage for the system output, V_{o_ac}. A full-bridge inverter which consists of MOSFETS Q_5 - Q_8 modifies the output voltage waveform by the fixed modulation control signal. The diodes D_{Q5} - D_{Q8} in antiparallel with the MOSFETs Q_5 - Q_8 are used as commutating diodes for protecting the switches.

2.2.7 Battery charging converter

Battery charging converter, a commonly used fly-back converter, regulates the battery charging current and voltage under the conditions of limit current and constant voltage. Diodes D_9 - D_{12} rectifies the high frequency voltage V_{c_ac} from the main transformer to dc voltage V_{c_dc} with filter inductor L_b and filter capacitor C_b. L_b and C_b limit the current ripple and voltage ripple. Transformer T_B, MOSFET Q_9, and output rectifier diode D_{13} constitute a flyback converter and supply the power to charge or floating charge the battery.

2.3 OPERATION MODE

The basic operation of the UPS can be divided into two modes:

Mode 1: when input ac line voltage is normal, the system transfers the ac line power to the output. It can be called as normal power supply mode or ac-input to ac-output mode.

Mode 2: when input ac line voltage fails or becomes lower than the allowable operating voltage, the system transfers power from battery dc power source to the ac output. It can be called as backup power supply mode or dc-input to ac-output mode.

The detailed analysis of these modes in the parallel processing ac-UPS is given in the following sub-sections.

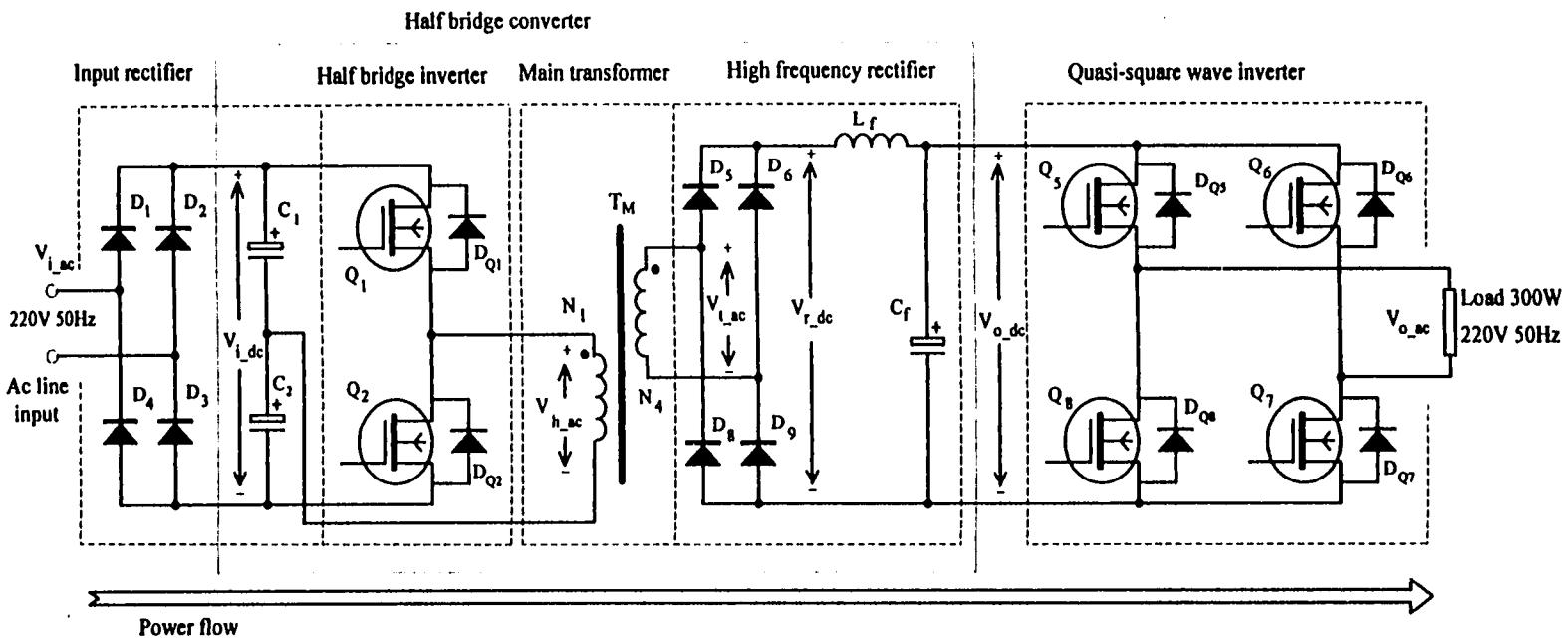


Fig. 2-2 The equivalent circuit and power flow of operation mode 1.

2.3.1 Operation Mode 1: ac-input to ac-output

During the Mode 1, the dc-battery inverter ceases working, the equivalent circuit for this operation mode is shown in Fig. 2-2. The output power flow is from the ac-input to the ac-output through input rectifier, half-bridge inverter, the main-transformer, high frequency rectifier, and quasi- square wave inverter.

The power conversion is described as follows, and the related waveforms are shown in Fig. 2-3.

(i) The power from the ac line is rectified to dc voltage, V_{i_ac} to V_{i_dc}.

(ii) The half-bridge inverter converts this dc voltage to the high frequency square voltage, V_{i_dc} to V_{h_ac}.

(iii) The high frequency transformer steps V_{h_ac} up to a square voltage with the proper peak value, V_{h_ac} to V_{t_ac}.

(iv) The high frequency rectifier with the filter converts the high frequency square wave voltage into the dc ripple free voltage, V_{t_ac} to V_{r_dc} to V_{o_dc}.

(v) Finally, the quasi-square wave inverter modifies the dc voltage to a quasi-square voltage to the load, V_{o_dc} to V_{o_ac}.

As described above, in this operation mode, the half-bridge inverter, main transformer, and high frequency rectifier constitute a half-bridge dc-dc converter.

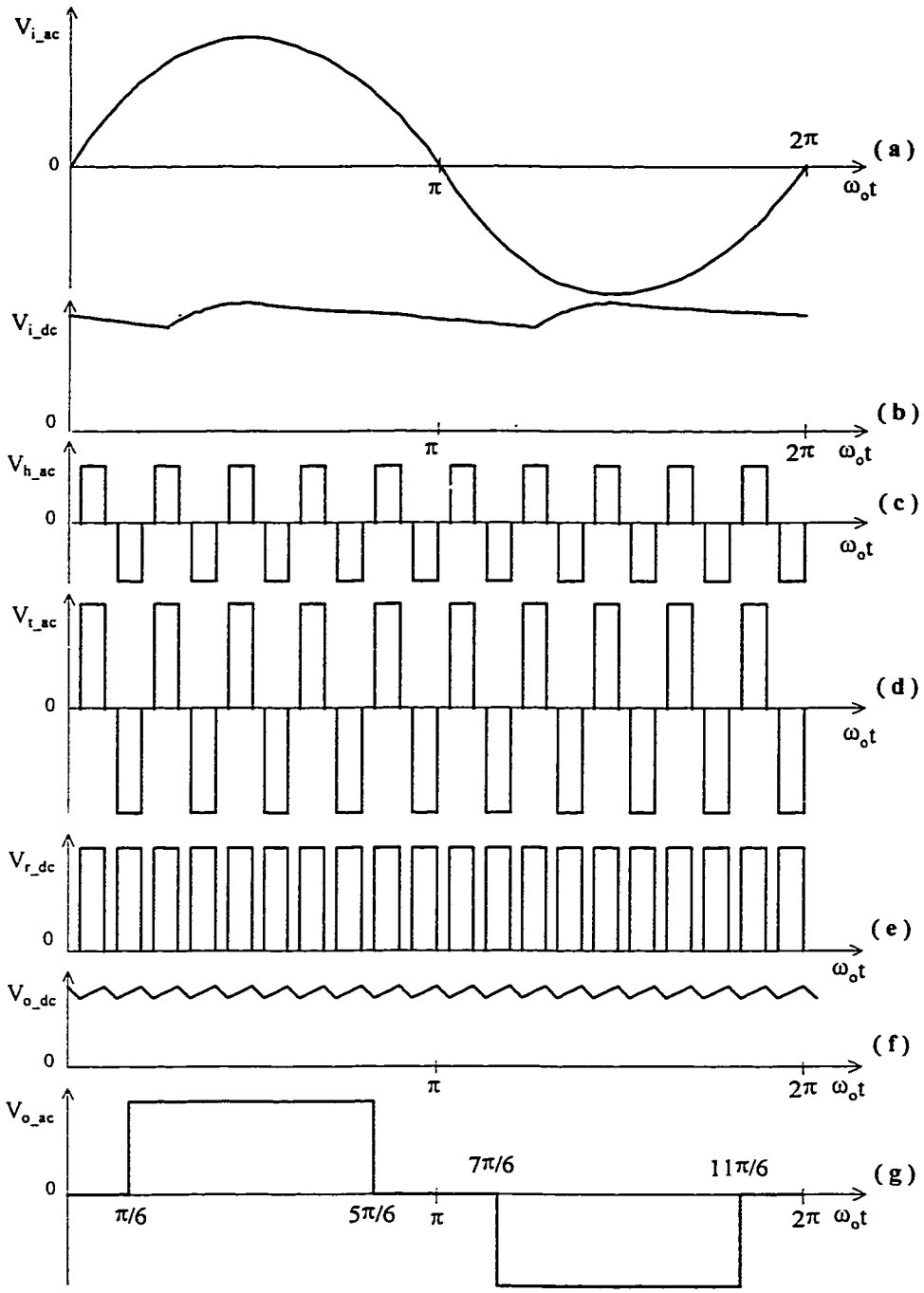


Fig. 2-3 The main voltage waveforms in operation mode 1: **(a)** input ac line voltage V_{i_ac}. **(b)** input rectifier voltage V_{i_dc}. **(c)** half-bridge inverter voltage V_{h_ac} on the winding N_1. **(d)** high frequency transformer output voltage V_{t_ac} on the winding N_4. **(e)** high frequency rectifier voltage V_{r_dc}. **(f)** output dc voltage V_{o_dc} after filter. **(g)** output quasi-square voltage V_{o_ac}.

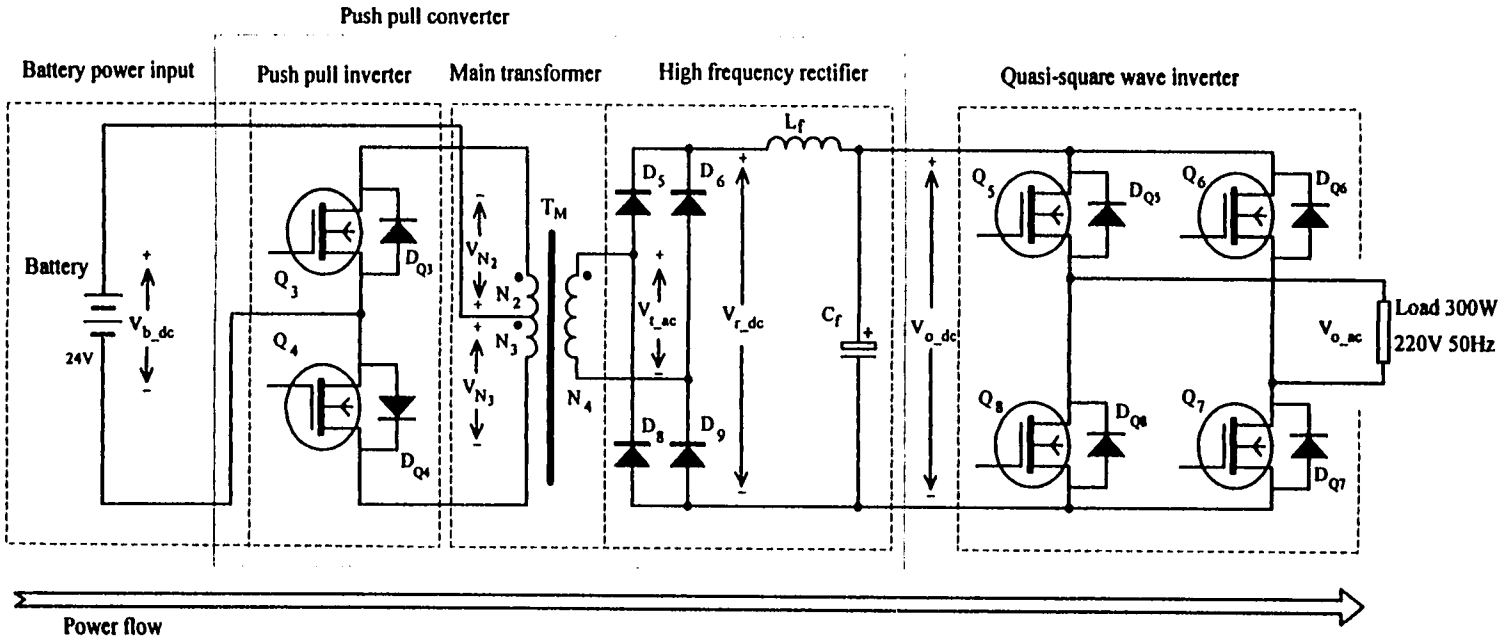


Fig. 2-4 The equivalent circuit and power flow of operation mode 2.

2.3.2 Operation Mode 2: dc-input to ac-output

When the ac-input power fails, the push-pull inverter at the battery side starts working. Fig. 2-4 shows the equivalent circuit and the power flow path. The power flow is from the battery dc power to the ac-output through the push-pull inverter, main transformer, high frequency rectifier, and quasi-square wave inverter.

The power conversion is described as follows, and the related waveforms are shown in Fig. 2-5.

(i) The push-pull inverter converts the battery dc voltage to the high frequency square voltage, V_{b_dc} to V_{N2} and V_{N3}.

(ii) The main transformer boosts V_{N2} and V_{N3} to square voltage with a proper peak value, V_{N2} and V_{N3} to V_{t_ac}.

(iii) The high frequency rectifier with the filter converts high frequency square voltage to ripple-free dc voltage, V_{t_ac} to V_{r_dc} to V_{o_dc}.

(iv) Finally, the quasi-square wave inverter modifies the dc voltage to a quasi-square voltage to the load, V_{o_dc} to V_{o_ac}.

As described above, in this operation mode, the push-pull inverter, main transformer, and high frequency rectifier constitute a push-pull dc-dc converter.

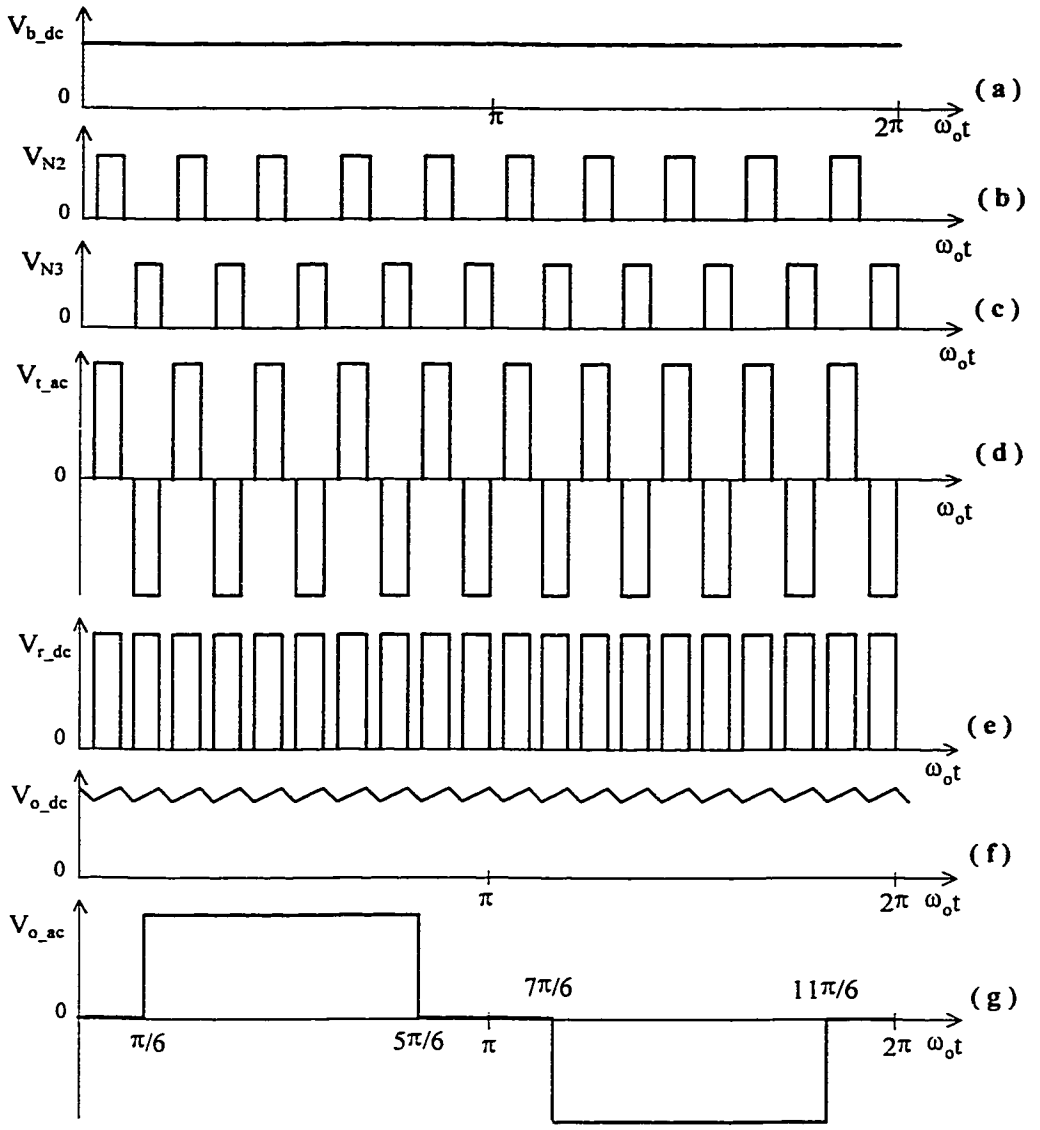


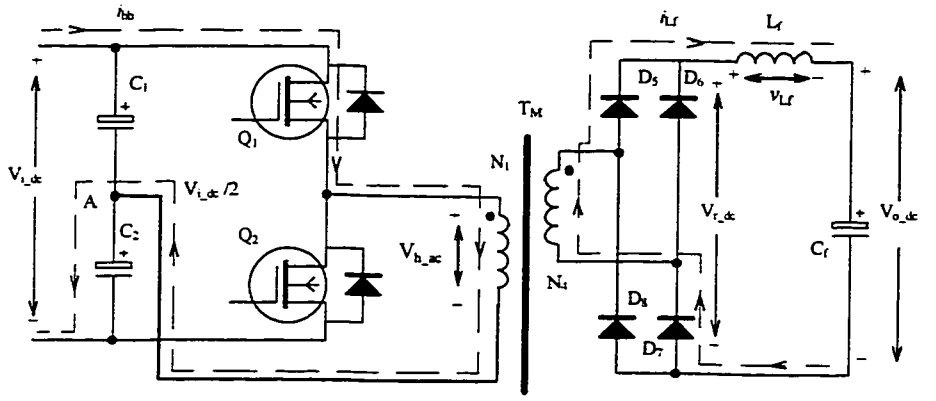
Fig. 2-5 The main voltage waveforms in operation mode 2: **(a)** input dc battery voltage V_{b_dc}. **(b)** winding N_2 voltage V_{N2}. **(c)** winding N_3 voltage V_{N3}. **(d)** high frequency transformer output voltage V_{t_ac} on the winding N_4. **(e)** high frequency rectifier voltage V_{r_dc}. **(f)** output dc voltage V_{o_dc} after filter. **(g)** output quasi-square voltage V_{o_ac}.

2.4 HALF-BRIDGE CONVERTER AND PUSH-PULL CONVERTER

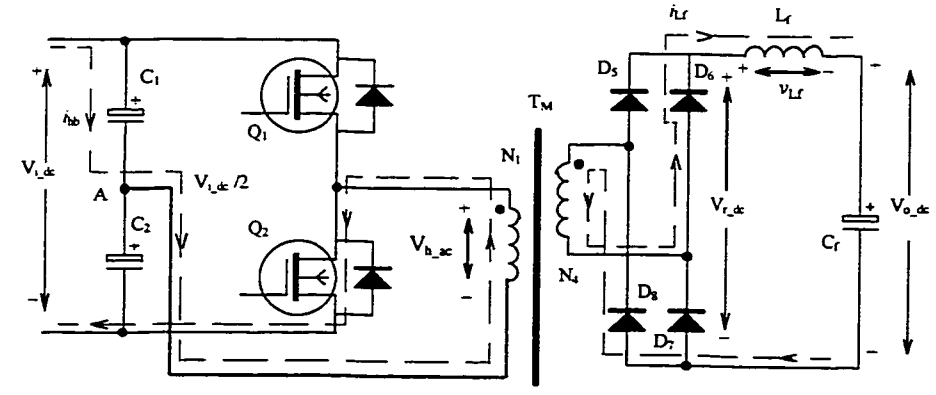
Depending on the different operation modes, the parallel system is combined by two switching topology: half-bridge converter and push-pull converter.

2.4.1 Half-bridge converter

The half-bridge converter topology is suitable for power lower than 500 Watts [6]. In the half-bridge configuration as shown in Fig. 2-6 (the dashed line indicates the current



(a) Current flow in the positive cycle



(b) Current flow in the negative cycle

Fig. 2-6 Current flow in the half-bridge converter.

flow path), the power transformer has one side connected to a floating voltage potential created by the series capacitors C_1 and C_2, which has a value of $V_{i\_dc}/2$. The other end of the transformer is connected at the junction of the Q_1 source and Q_2 drain. When Q_1 turns on, this end of the transformer goes to the positive bus, generating a voltage pulse of $V_{i\_dc}/2$. When Q_1 turns off and Q_2 turns on, the polarity of the transformer primary reverse, since it is now connected to the negative bus, generating a negative pulse of $V_{i\_dc}/2$. The turn-on-turn-off action of Q_1 and Q_2 therefore will generate a V_{i_dc} peak-to-peak square wave, which in turn is stepped up, rectified, and filtered to produce the output dc voltage V_{o_dc}.

In connection with the half-bridge converter, the capacitors C_1 and C_2 establish a voltage midpoint between 0 and the input dc voltage V_{i_dc}. The switches Q_1 and Q_2 are turned on alternatively, each for an interval t_{on}. With Q_1 on, $V_{r\_dc} = (N_4/N_1)(V_{i\_dc}/2)$ as shown in Fig. 2-6. Therefore, the voltage across the inductor L_f is

$$v_{L_f} = \frac{N_4}{N_1}\left(\frac{V_{i\_dc}}{2}\right) - V_{o\_dc} \qquad 0 < t < t_{on} \qquad (2\text{-}1)$$

During the interval t_{off}, when both switches are off, the inductor current splits equally between the two secondary halves. Assuming ideal diodes, $v_{r\_dc} = 0$ and, therefore,

$$v_{L_f} = -V_{o\_dc} \qquad t_{on} < t < (t_{on} + t_{off}) \qquad (2\text{-}2)$$

In the steady state, the waveforms repeat with a period $T_s/2$ and

$$t_{on} + t_{off} = \frac{T_s}{2} \qquad (2\text{-}3)$$

Equating the time integral of the inductor voltage during one repetition period to zero using Eqs (2-1) through (2-3) yields

$$\frac{V_{o\_dc}}{V_{i\_dc}} = \frac{N_4}{N_1} D \qquad (2\text{-}4)$$

where $D = t_{on}/T_s$ and $0 < D < 0.5$. (In practice, to maintain a small blanking time to avoid turning both the switches on simultaneously, D should be kept smaller than 0.45). The average value of v_{r_dc} in Fig. 2-7 equals V_{o_dc} [7].

Diodes D_{Q1} and D_{Q2}, which are used across the MOSFETs Q_1 and Q_2 and called commutating diodes , have a dual function.

(i) When the MOSFET turns off, the commutating diode steers transformer leakage inductance energy back to the main dc bus. Thus high-energy leakage inductance spikes are not present.

(ii) The commutating diode prevents the drain of the on MOSFET from swinging negative with respect to its source in the event of a sudden off-load situation due to an increase in transformer flux. In such an event the commutating diode will bypass the MOSFET until the drain goes positive again, preventing the device from an inverse conduction and possible damage.

The advantages of this topology are:

(i) Reducing the voltage stress imposed on the switching MOSFET to no more than V_{i_dc}. The MOSFET with this rated voltage can be easily found on the market with low price.

(ii) Balancing the volt-second integral of each switching MOSFET automatically to avoid core saturation.

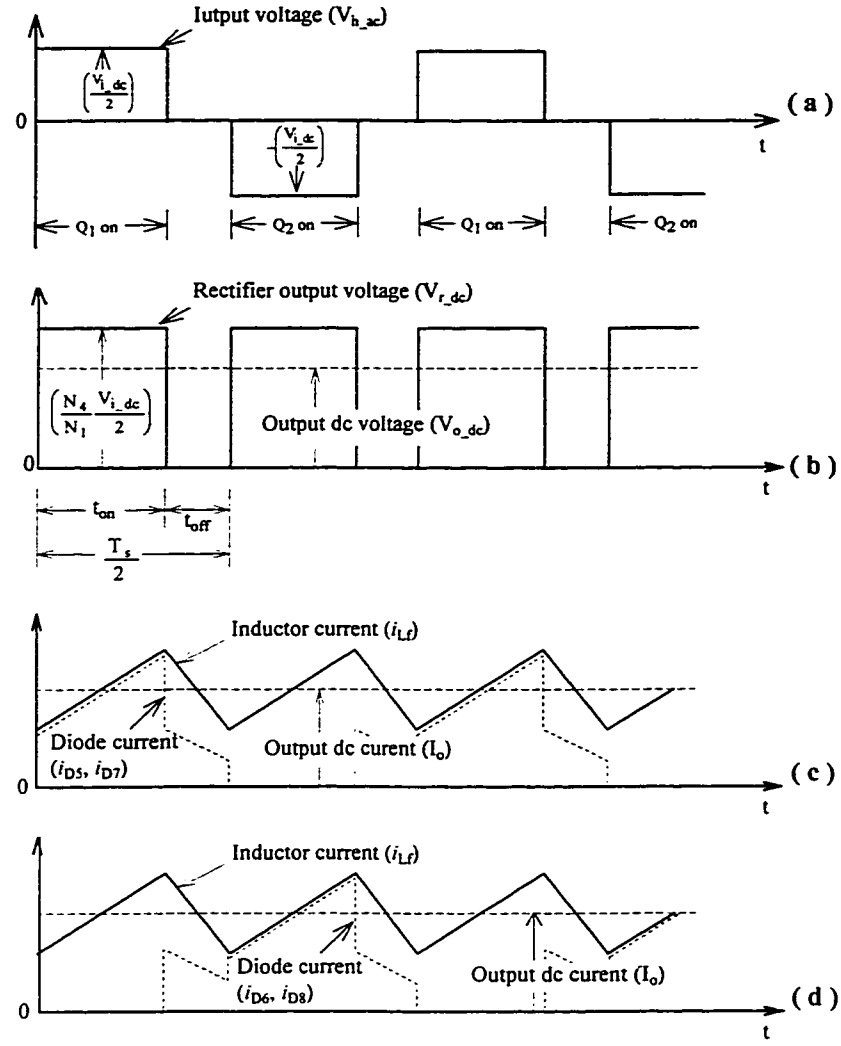


Fig. 2-7 The main waveforms related to the half-bridge converter: **(a)** input voltage V_{h_ac} on transformer winding N_1. **(b)** rectifier output voltage V_{r_dc} and filtered output dc voltage V_{o_dc}. **(c)** filter inductor current i_{Lf} and rectifier diode current i_{D5} & i_{D7}. **(d)** filter inductor current i_{Lf} and rectifier diode current i_{D6} & i_{D8}.

The value of the bridge capacitors is calculated from the known primary current and operating frequency. For a total output power of P_{i_ac}, primary current is

$$I_{hb} = \frac{P_{i\_ac}}{V_{i\_dc}/2} \qquad (2\text{-}5)$$

For an operating switching frequency f_s, the transformer primary is fed effectively from C_1 and C_2 in parallel. When Q_1 is on, current flows through the primary into node *A* in Fig. 2-6, replenishing the charge lost by both capacitors in the half cycle when Q_2 was on and drew current out of node *A*. The voltage change across the capacitor, for C_1=C_2, is then

$$\Delta V = \frac{I_{hb}\Delta t}{C_1} = \left[\frac{P_{i\_ac}}{(V_{i\_dc}/2)(C_1 + C_2)}\right]\left(\frac{1}{2f_s}\right) = \frac{P_{i\_ac}}{2V_{i\_dc}f_sC_1} \qquad (2\text{-}6)$$

The percentage change in dc voltage across the capacitors is the same as the percentage change in rectified output voltage. Thus, for a percentage output ripple of V_r,

$$V_r = \frac{100\Delta V}{V_{i\_dc}/2} = \frac{100P_{i\_ac}/2V_{i\_dc}f_sC_1}{V_{i\_dc}/2} = \frac{100P_{i\_ac}}{V_{i\_dc}^2 f_s C_1} \qquad (2\text{-}7)$$

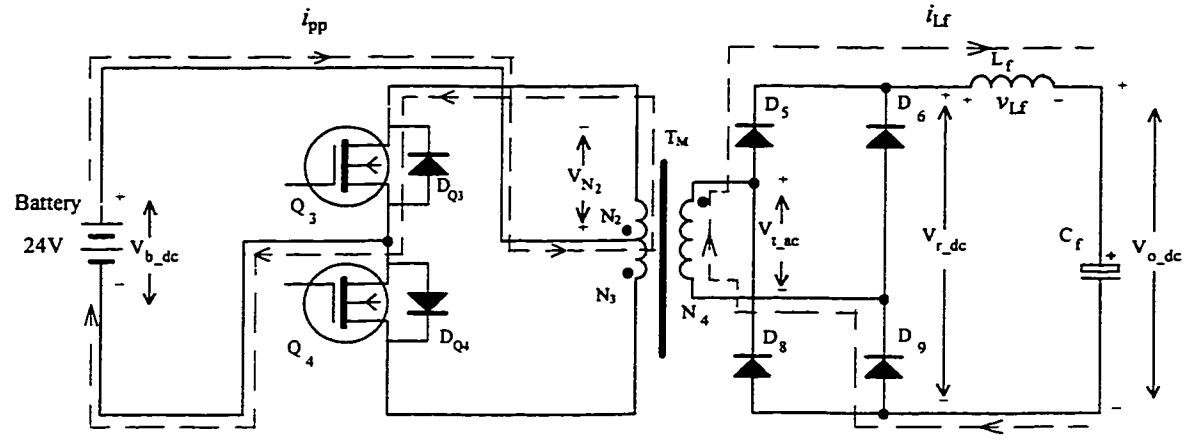
And the magnitude of C_1 for output ripple percentage V_r is

$$C_1 = C_2 = \frac{100P_{i\_ac}}{V_{i\_dc}^2 f_s V_r} \qquad (2\text{-}8)$$

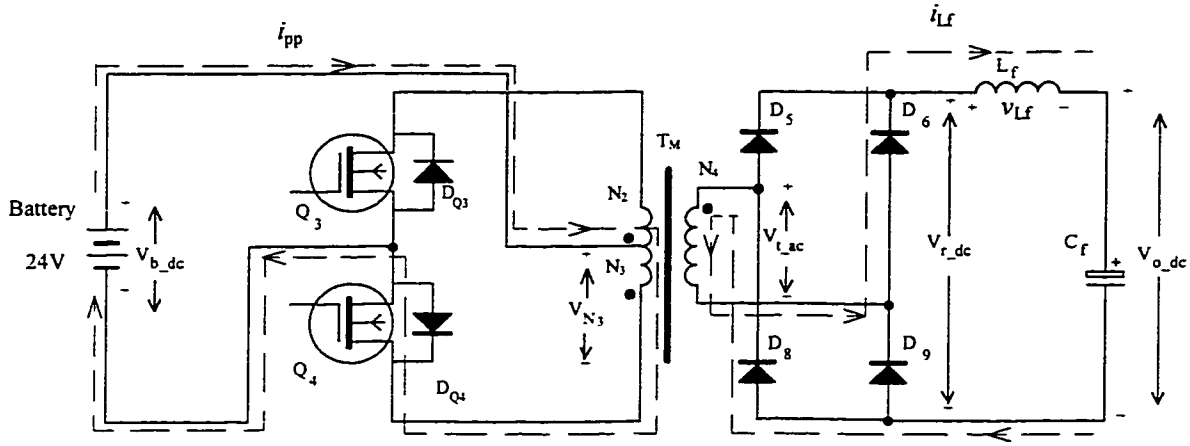
2.4.2 Push-pull converter

Fig. 2-8 shows the simplified push-pull configuration. Actually it is an arrangement of two forward converters working in antiphase. Both halves of the push-pull converter are delivering power alternatively to the load at each half cycle.

In Fig. 2-8, when Q_3 is on, D_5 and D_7 conduct, D_6 and D_8 get reverse biased. This results in $v_{r\_dc} = (N_4/N_2)V_{b\_dc}$ in Fig 2-9. Therefore, the voltage across the filter inductor is given as



(a) Current flow in the positive cycle.



(b) Current flow in the negative cycle.

Fig. 2-8 Configuration of the push-pull converter.

$$v_{Lf} = (N_4/N_2)V_{b\_dc} - V_{o\_dc} \qquad 0 < t < t_{on} \qquad (2\text{-}9)$$

and i_{Lf} through D_5 and D_7 increases linearly as shown in Fig. 2-9.

During the interval t_{off}, the inductor current splits equally between the two secondary half-windings and $v_{r\_dc} = 0$. Therefore, during $t_{on} < t < (t_{on} + t_{off})$,

$$v_{Lf} = -V_{o\_dc} \qquad (2\text{-}10)$$

and

$$i_{D5} = i_{D6} = i_{Lf}/2 \qquad (2\text{-}11)$$

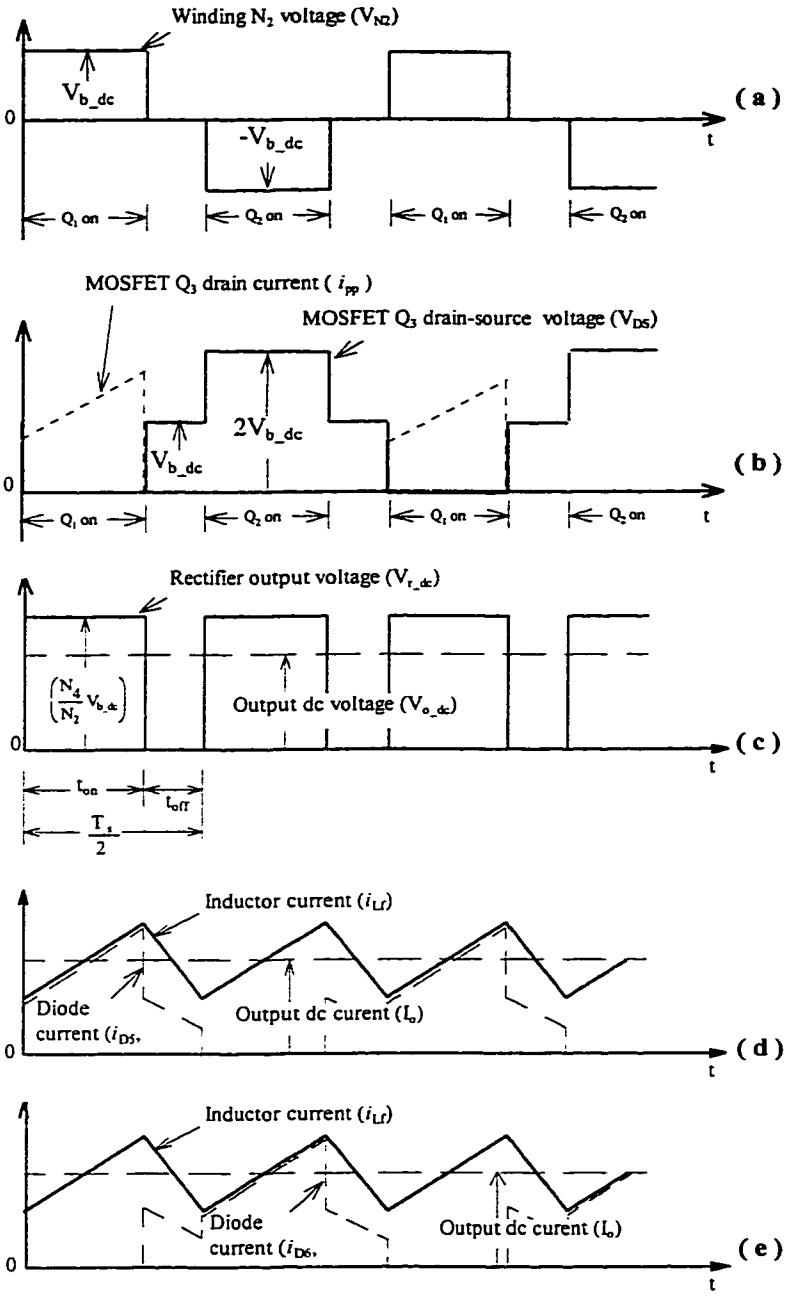


Fig. 2-9 The main waveforms related to the push-pull converter operation: **(a)** transformer winding N_2 voltage V_{N2}. **(b)** MOSFET Q_3 drain current I_D and drain-source voltage V_{DS}. **(c)** rectifier output voltage V_{r_dc} and filtered output dc voltage V_{o_dc}. **(d)** filter inductor current i_{Lf} and rectifier diode current i_{D5} & i_{D7}. **(e)** filter inductor current i_{Lf}, and rectifier diode current i_{D6} & i_{D8}.

The next half-cycle consists of t_{on} (during which Q_3 is on) and the interval t_{off}. The waveforms repeat with a period $T_s/2$ and

$$t_{on} + t_{off} = T_s / 2 \qquad (2\text{-}12)$$

Equating the time integral of the inductor voltage during one repetition period $T_s/2$ to zero using Eqs(2-9), (2-10), and (2-12) yields

$$V_{o\_dc} / V_{b\_dc} = 2\,D\,(N_4/N_2) \qquad 0 < D < 0.5 \qquad (2\text{-}13)$$

where $D = t_{on}/T_s$ is the duty ratio of the switches Q_3 and Q_4 and the maximum value it can attain is 0.5 (in practice, to maintain a small blanking time to avoid turning both the switches on simultaneously, D should be kept smaller than 0.45). The average value of v_{r_dc} waveform in Fig. 2-9 equals V_{o_dc} [7].

Assuming in the push-pull converter that the conduction times of the two MOSFETs are equal (or they are forced to be equal) the transformer will use both halves of the B-H curve and the volume of the core will be halved. An air gap may not be necessary.

The volume of the transformer [8] is given by

$$\text{Volume} = \frac{4\mu_0\mu_e I^2_{mag\_L_f}}{B^2_{max}} \qquad (2\text{-}14)$$

where $I_{mag\_Lf} = nV_{out}T_s/4L_f$ is the magnetising current. And, n is the transformer turns ratio of N_2 to N_4.

The voltage across each MOSFET at turn-off is limited to

$$V_{DS\_max} = 2V_{b\_dc} \qquad (2\text{-}15)$$

The peak drain current of each MOSFET I_D is given by

$$I_D = \frac{I_{L_f}}{n} + I_{mag} \qquad (2\text{-}16)$$

Assuming that $I_{mag} << I_{Lf}/n$. then

$$I_D = \frac{I_{L_f}}{n} \qquad (2\text{-}17)$$

However, the first limitation is the voltage rating of the MOSFETs, which should handle twice the input voltage to the converter plus any leakage spike that might result because of transformer leakage inductance. The second and more sever of the problems associated with push-pull circuit, that is, transformer core saturation. In order for the two areas of the flux density to be equal, the saturation and switching characteristics of the switching MOSFETs must be identical under all working conditions and temperatures. If the MOSFET characteristics are not identical, "flux walking" to one direction of the B-H curve occurs, driving the core into the saturating region.

The advantages of this topology are:

(i) No more than one switch in series conducts at any instant of time. This is very good for converting low voltage, such as a battery.

(ii) The control drives for the two switches have a common ground, which made base drives simple and nonisolation.

2.5 QUASI-SQUARE WAVE INVERTER

A full-bridge inverter is used for generating a 50Hz AC quasi-square waveform, which does not contain the 3rd harmonics in the output waveform compared with the pure

square wave. The comparison between this two kinds of square waveform in terms of harmonics is shown in Fig. 2-10.

The Fourier series of the square waveform in Fig. 2-10 (a) is expressed as

$$V_{o\_ac}(\omega_o t) = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{2n-1}\sin[(2n-1)\omega_o t] \qquad (2\text{-}18)$$

Therefore, the output voltage with square waveform has the 3rd, 5th, 7th,... harmonics, as shown in its harmonic spectrum.

The Fourier series of the quasi-square waveform in Fig. 2-10 (b) is expressed as:

$$V_{o\_ac}(\omega_o t) = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(\frac{n\pi}{3})\sin(\frac{n\pi}{2})\sin(n\omega_o t) \qquad (2\text{-}19)$$

When $\frac{n\pi}{3} = k\pi$ or $\frac{n\pi}{2} = k\pi$, $\quad k = 0, 1, 2, 3, \ldots,$

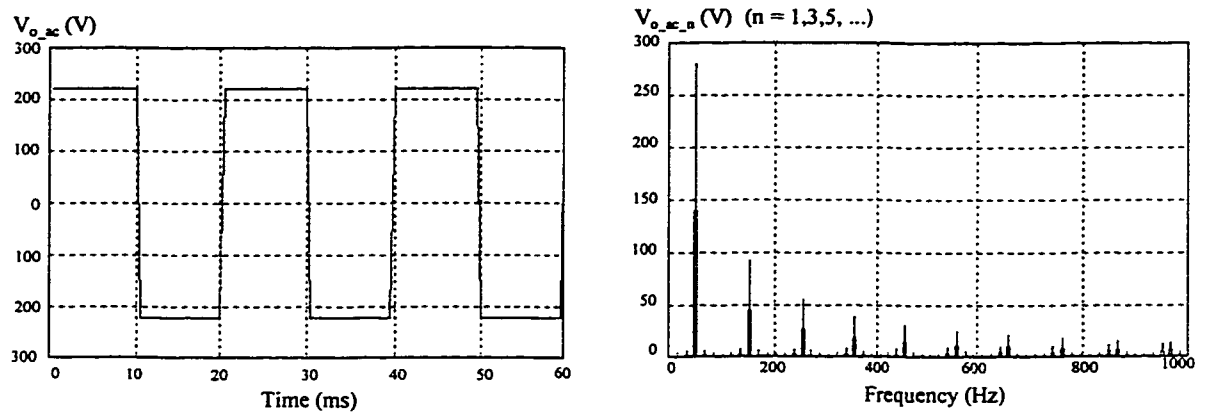
$n = 3k$ or $n = 2k$

The coefficient of $\sin(\omega_o t)$: $\quad \sin\left(\frac{n\pi}{3}\right)\sin\left(\frac{n\pi}{2}\right) = 0$

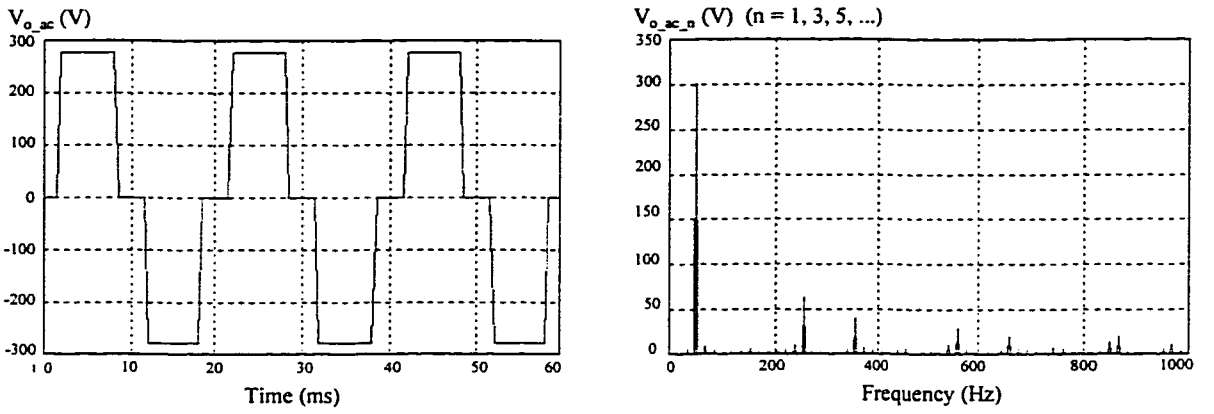
Compared with the square waveform, the output voltage with quasi-square waveform is improved by eliminating the order of 3k harmonics (3rd, 9th, 15th, ...) in its harmonic spectrum.

For the quasi-square wave circuit, the relationship between the input and the output is given by

$$V_{o\_ac} = \left[\frac{1}{\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} V_{o\_dc}^2 d\mathrm{t}\right]^{\frac{1}{2}} \qquad (2\text{-}20)$$



(a) Output voltage and its harmonic spectrum (50 Hz square waveform).



(b) Output voltage and its harmonic spectrum (50 Hz quasi-square waveform).

Fig. 2-10 The comparison of output voltage between the square waveform and the quasi-square waveform.

In order to regulate the ac-output voltage linearly by regulating the dc output voltage V_{o_dc}, V_{o_dc} should be kept constant by the voltage control loop. Therefore, Eq (2-20) can be changed to

$$V_{o\_ac} = \left[\frac{1}{\pi}\left(V_{o\_dc}\right)^2\left(\frac{5\pi}{6} - \frac{\pi}{6}\right)\right]^{\frac{1}{2}} = \sqrt{\frac{2}{3}}V_{o\_dc} \qquad (2\text{-}21)$$

The relationship between V_{o_ac} and V_{o_dc} becomes linear.

2.6 BATTERY CHARGING

Battery charging is another important part in the UPS system. Normally, there are three battery charge methods: voltage constant, current constant, and pulse fast-speed charge. Since the consumer UPS doesn't need a special battery charge, a constant voltage converter with current limit is a simple method for the implementation [9]. The charging voltage is limited under 26V (for 24V lead-acid battery) [10], which avoids chemical material to be unrecoverable in the battery.

A fly-back converter is selected for this application and its simple structure is shown in Fig. 2-11.

When the switch is on, due to the winding polarities, the diode D_{13} becomes reverse biased. The continuous-current-conduction mode in a buck-boost converter corresponds to an incomplete demagnetisation of the inductor core. Therefore, the inductor core flux

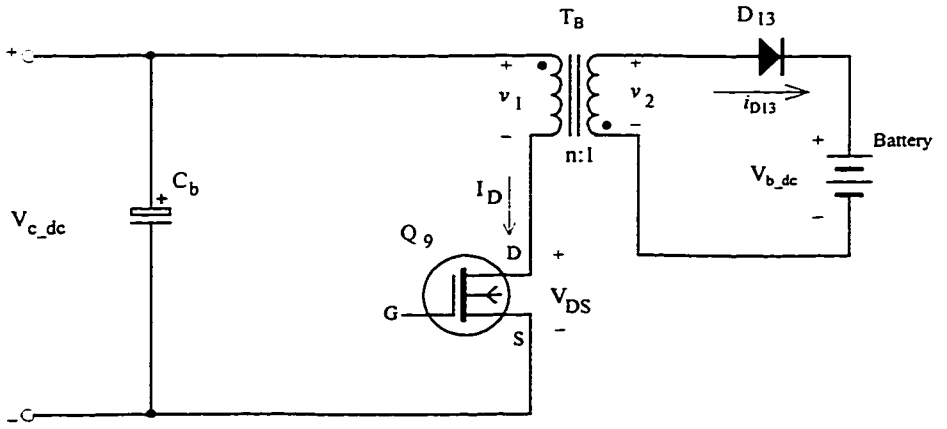


Fig. 2-11 A flyback converter for battery charging

increases linearly from its initial value $\phi(0)$, which is finite and positive in Fig. 2-12:

$$\phi(t) = \phi(0) + \frac{V_{c\_dc}}{n} t \qquad 0 < t < t_{on} \qquad (2\text{-}22)$$

and , the peak flux ϕ_p at the end of the on interval is given as

$$\phi_p = \phi(t_{on}) = \phi(0) + \frac{V_{c\_dc}}{n} t_{on} \qquad (2\text{-}23)$$

After t_{on} the switch is turned off and the energy stored in the core causes the current to flow in the secondary winding through the diode D_{13}. The voltage across the secondary winding $v_2 = -V_{b\_dc}$ and therefore, the flux decreases linearly during t_{off}:

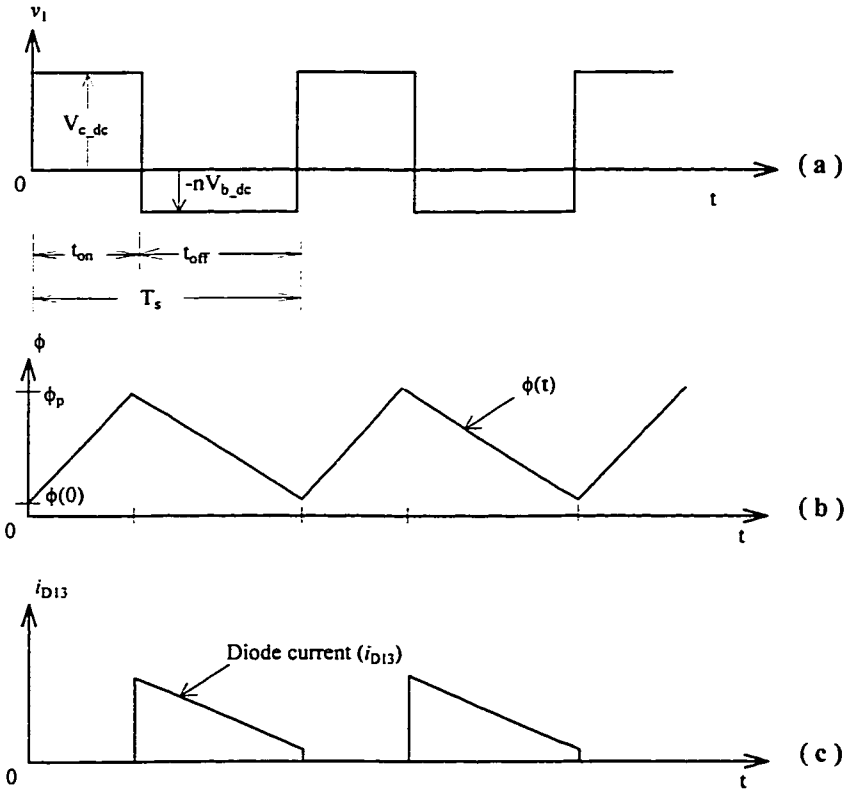


Fig. 2-12 The main waveforms related to the flyback converter operation: **(a)** primary winding voltage v_1 of the flyback converter transformer. **(b)** flux waveform $\phi(t)$ of the transformer core. **(c)** current i_{D13} through the output rectifier diode D_{13}.

$$\phi(t) = \phi_p - V_{b\_dc}(t - t_{on}) \qquad t_{on} < t < T_s \qquad (2\text{-}24)$$

The maximum voltage across the switch during the off interval equals

$$V_{DS\_max} = \frac{V_{c\_dc}}{1 - \delta_{max}} \qquad (2\text{-}25)$$

The expression for the MOSFET working current, I_D, in terms of output power

$$I_D = \frac{2P_{b\_dc}}{\eta_{fly} V_{c\_dc} \delta_{max}} \qquad (2\text{-}26)$$

2.7 EXPERIMENTAL WAVEFORMS OF THE TWO OPERATION MODES

Fig. 2-13 to Fig. 2-21 present the main steady state waveforms related to the system operation in two modes. These waveforms are obtained from the experiments based on a 300W UPS. The switching frequency is 25.6kHz. The output voltage is 220Vrms 50Hz quasi-square wave. Fig. 2-13 shows the rectifier voltage V_{i_dc} with 18V ripple while the input ac line voltage is 220Vrms 60Hz. Fig. 2-14 indicates the voltage across the MOSFET Q_1 V_{DS} = 280V and the corresponding MOSFET drive signal V_{GS}. Fig. 2-15 shows the voltage and current waveforms on the winding N_1 of the main high-frequency transformer. The peak current through the winding N_1 is about 6A which also passes through MOSFETs Q_1 and Q_2 in the half-bridge inverter. Fig. 2-16 shows the voltage on the winding N_4 of the main high-frequency transformer. Voltage spike exists due to the leakage inductance in the main transformer, which need to choose the ultrafast recovery rectifier with high dc

blocking voltage. Fig. 2-17 indicates the voltage across the ultrafast recovery diode D_4. Fig. 2-18 shows the voltage waveform of the output rectifier and filter. The output dc voltage V_{o_dc} is regulated at 270V. Fig. 2-19 shows the output dc voltage V_{o_dc} at the rated output load condition. The voltage V_{o_dc} has ripple about 22V due to the quasi-square wave inverter operation. Fig. 2-20 shows the output ac voltage of the quasi-square wave inverter and its harmonic spectrum. The 3rd harmonics is depressed. Fig. 2-21 shows the voltage and current waveform on the MOSFET Q_3 in the push-pull inverter. V_{DS} of Q_3 is about 48V and the peak value of current I_D is about 20A. These experimental results testify that the proposed high-frequency parallel processing ac UPS is working properly.

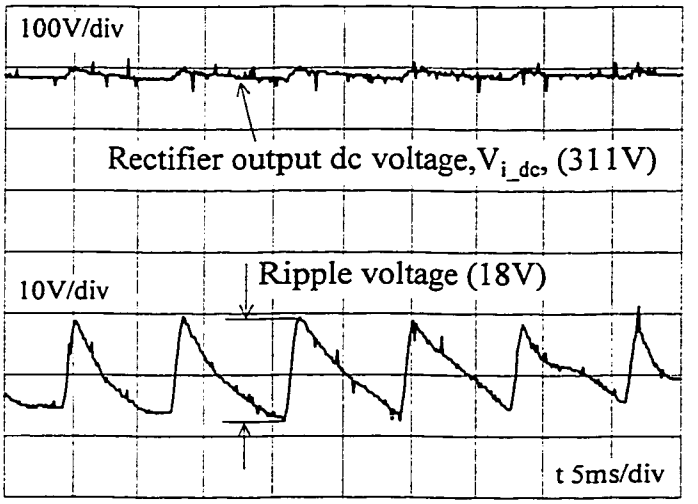


Fig. 2-13 Input rectifier dc voltage V_{i_dc} and its amplified waveform.

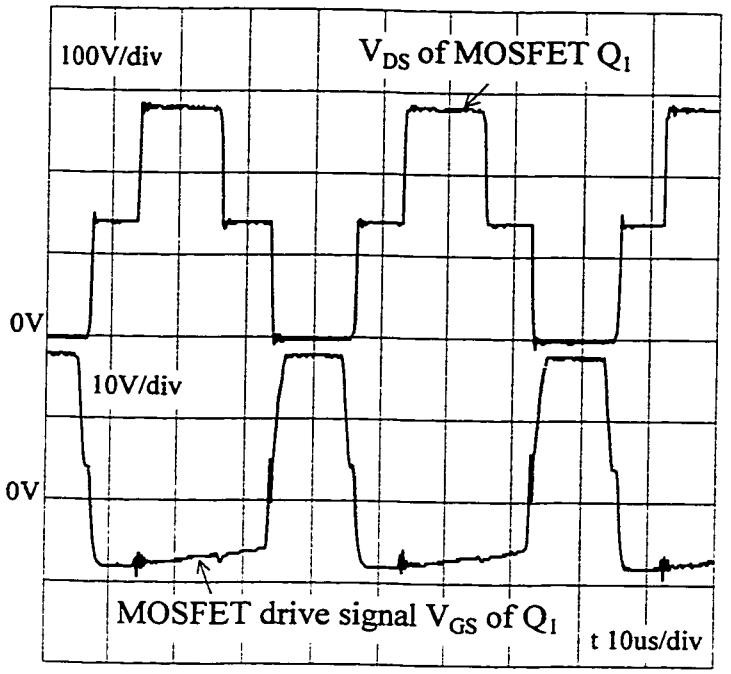


Fig. 2-14 MOSFET Q_1 drain-source voltage waveform and date-source drive signal waveform in the half-bridge inverter.

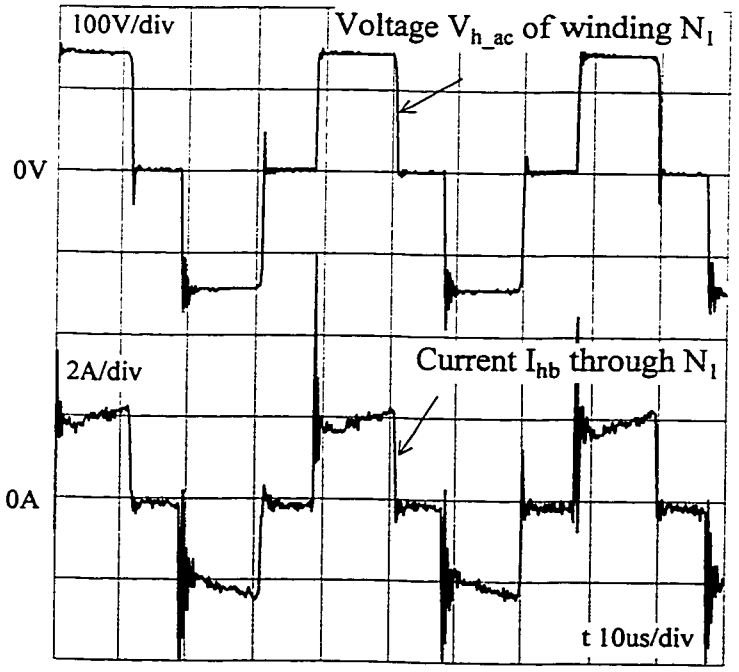


Fig. 2-15 The voltage and current waveform in the high frequency transformer winding N_1.

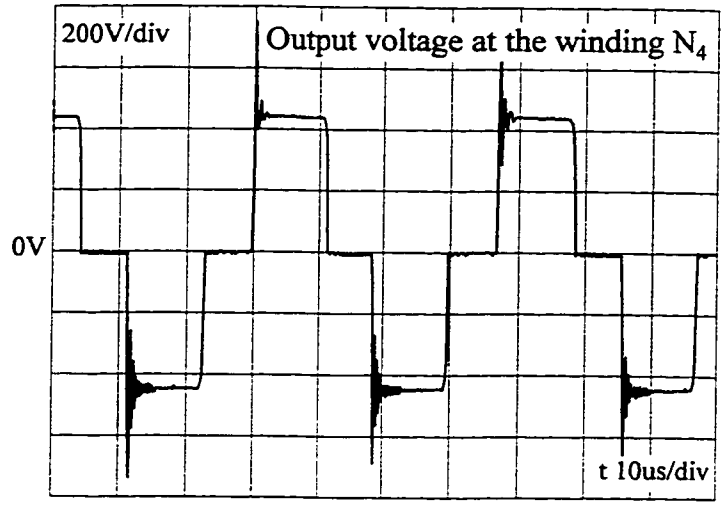


Fig. 2-16 Output voltage V_{t_ac} of the high frequency transformer winding N_4.

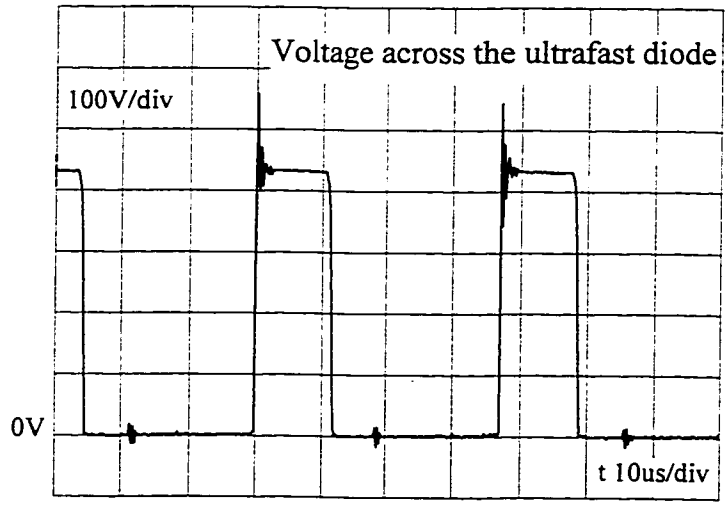


Fig. 2-17 Voltage waveform across the ultrafast recovery diode D_4.

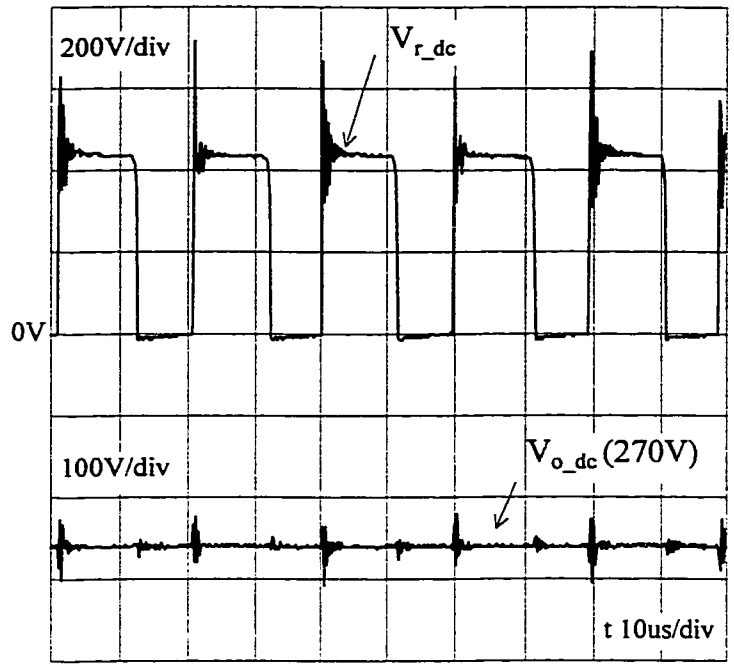


Fig. 2-18 The rectified dc voltage V_{r_dc} and the filtered output dc voltage V_{o_dc}.

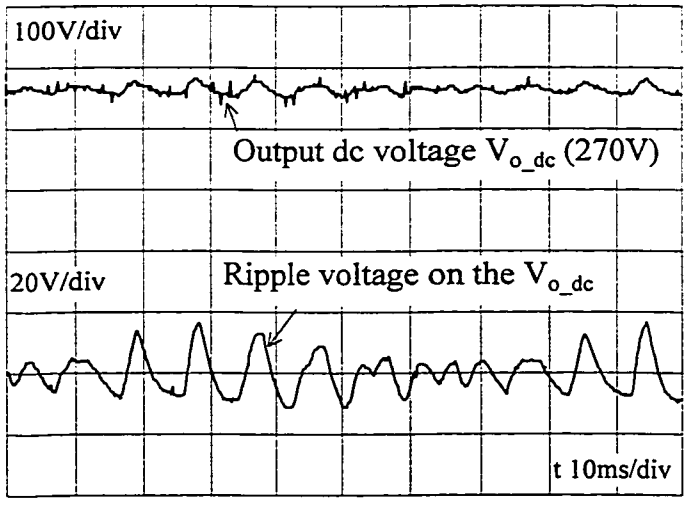


Fig. 2-19 Output dc voltage and its amplified waveform under the rated output load.

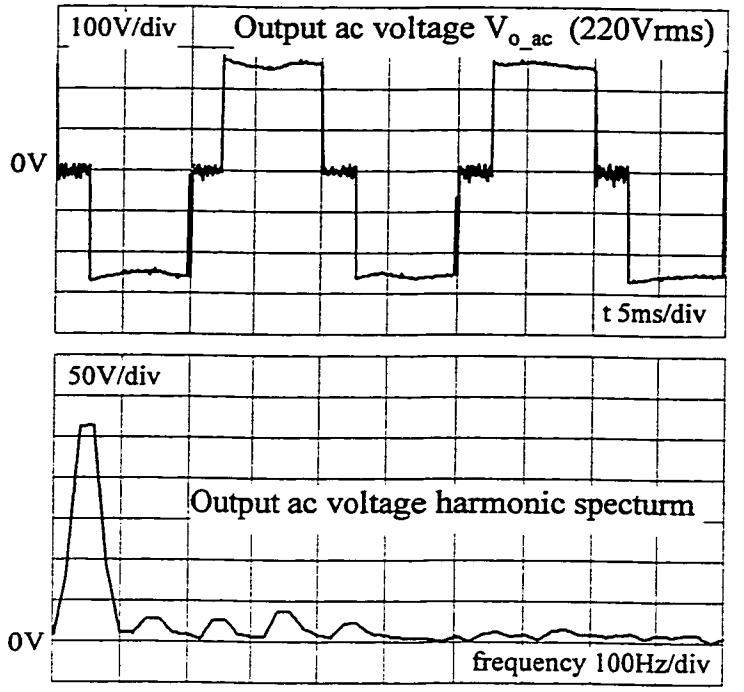


Fig. 2-20 Output ac voltage wave form V_{o_ac} and its harmonic spectrum.

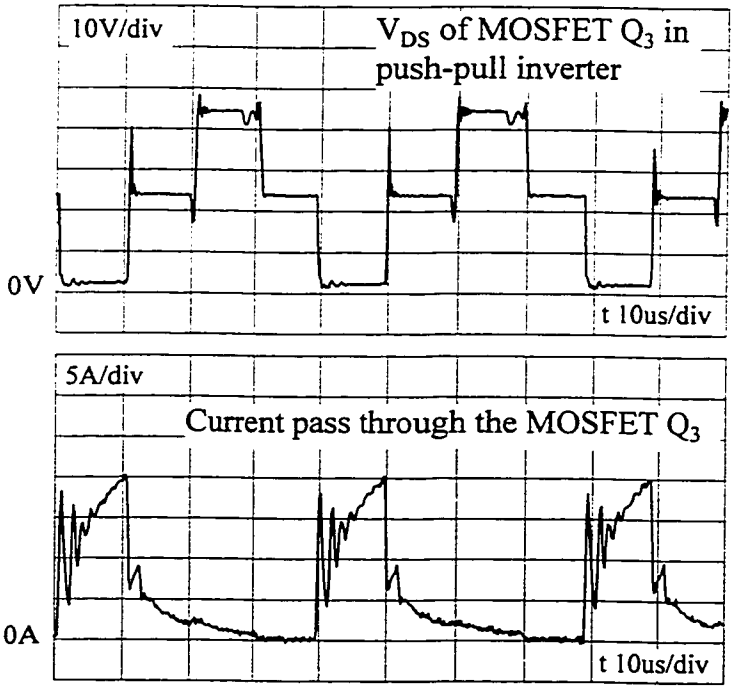


Fig. 2-21 The voltage waveform, V_{DS}, across the MOSFET drain-source of Q_3 in the push-pull inverter and the current waveform, I_{pp}, through the MOSFET Q_3 drain.

2.8 CONCLUSION

The proposed high-frequency switching parallel processing ac-uninterruptible power system is based on two converter topologies, half-bridge converter and push-pull converter. They make the contribution in the two different operation modes. Compared with other UPS topologies, the proposed UPS system, by using the high frequency transformer, has high efficiency, stable and isolated output voltage, light weight and small size. Moreover, the design and analysis for the system are as simple as those for the normal switching power supply. The system steady state performance is illustrated by the experimental waveforms.

CHAPTER 3

ANALYSIS AND DESIGN OF THE OUTPUT VOLTAGE CONTROL LOOP

3.1 INTRODUCTION

This chapter presents the system control structure of the parallel processing ac UPS. Although the UPS system works under two modes with the different converter topologies, the converter transfer functions are the same. This results in the possibility of realising a system close loop control by using one PID (Proportional-Integral-Differential) regulator. The experiment results about the system stability support the theory analysis.

In section 3.2, the system open loop transfer functions are described based on averaged model of the converters [11]. In section 3.3, the design of the system close loop compensation is carried out. Finally, in section 3.4, the experiment results are given for different changes in the input voltage and load.

3.2 OPEN LOOP TRANSFER FUNCTION

Fig. 3-1 shows the system control diagram. According to the feedback control system theory, the standard close control loop should sample the feedback signal from the ac output directly. However, it has the disadvantage of requiring more complicated circuit to process low frequency feedback signal. To simplify the feedback processing in the

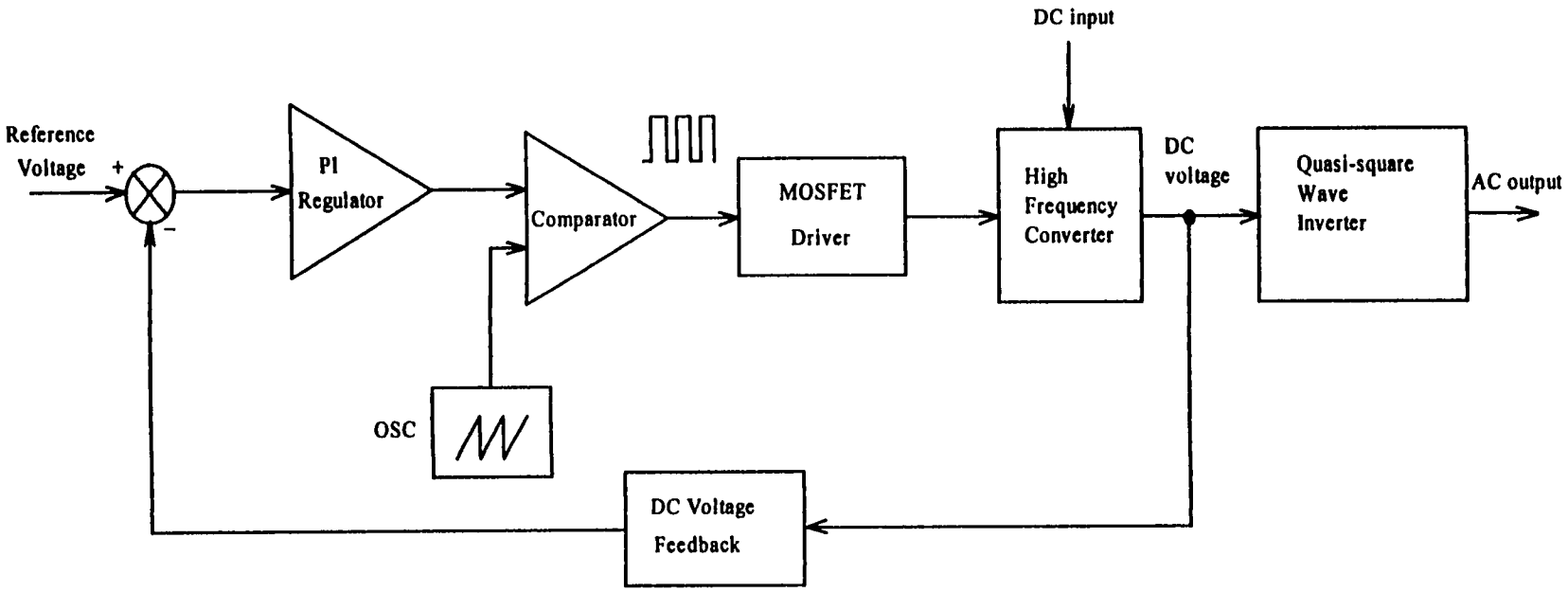


Fig. 3-1 Close loop control diagram.

proposed control loop, the feedback signal is obtained from the output dc side. The linear relation between the V_{o_ac} and V_{o_dc}, which has mentioned in Eq. (2-19), makes this deign possible. When the system control loop is closed from the V_{o_dc}, the system transfer function analysis can be simply classified;

a) Half-bridge converter transfer function in the operation mode 1,

b) Push-pull converter transfer function in the operation mode 2.

3.2.1 Half-bridge converter transfer function

The half-bridge converter in Fig. 2-3 can be equivalent to the circuit in Fig. 3-2 [12]. The half-bridge converter transfer function is easy to be derived by Kirchhoff's Voltage Law (KVL). The average model of the half-bridge converter circuit is shown in Fig. 3-3. The half-bridge converter transfer function is:

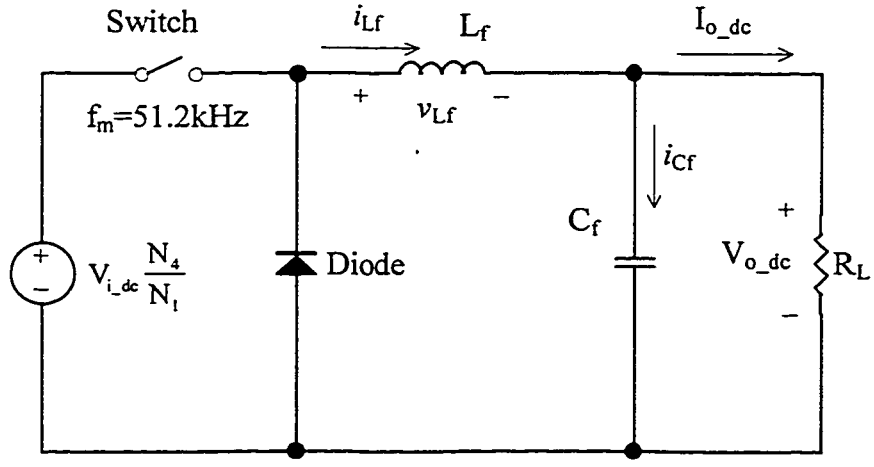


Fig. 3-2 Equivalent circuit of half-bridge converter.

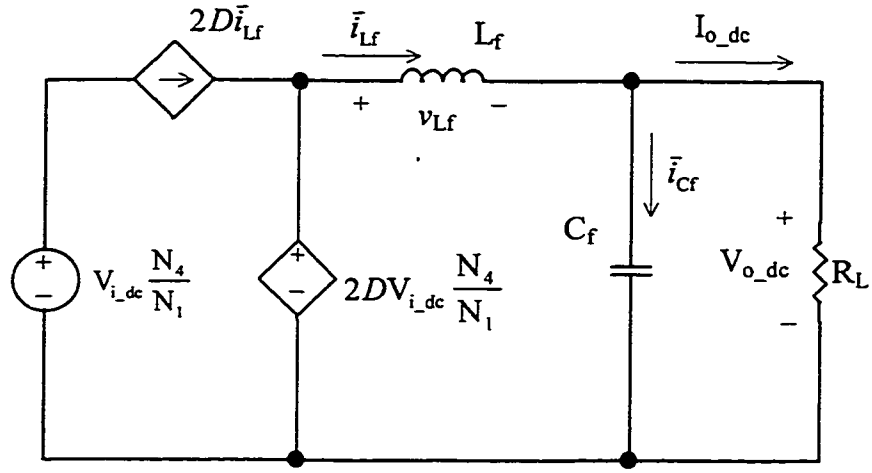


Fig. 3-3 Averaged circuit for half-bridge converter.

$$G(s)=\frac{V_{o\_dc}(s)}{V_{i\_dc}(s)}=2D\left(\frac{N_4}{N_1}\right)\frac{R_L}{s^2L_fC_fR_L+sL_f+R_L} \qquad (3\text{-}1)$$

where R_L is the equivalent resistance of the output load and the factor 2 is related with two half cycles.

3.2.2 Push-pull converter transfer function

The push-pull converter circuit is functional only when the DC battery supplies the power. The post part of the system, high frequency rectifier and modification sine wave circuit, are the same as ac line power supply. Fig. 3-4 shows the equivalent circuit. The push-pull converter transfer function is easy to be derived from the circuit in Fig. 3-4 by KVL. The average model of the push-pull converter circuit is shown in Fig. 3-5. The push-pull transfer function is:

$$G(s)=\frac{V_{o\_dc}(s)}{V_{b\_dc}(s)}=2D\left(\frac{N_4}{N_2}\right)\frac{R_L}{s^2L_fC_fR_L+sL_f+R_L} \qquad (3\text{-}2)$$

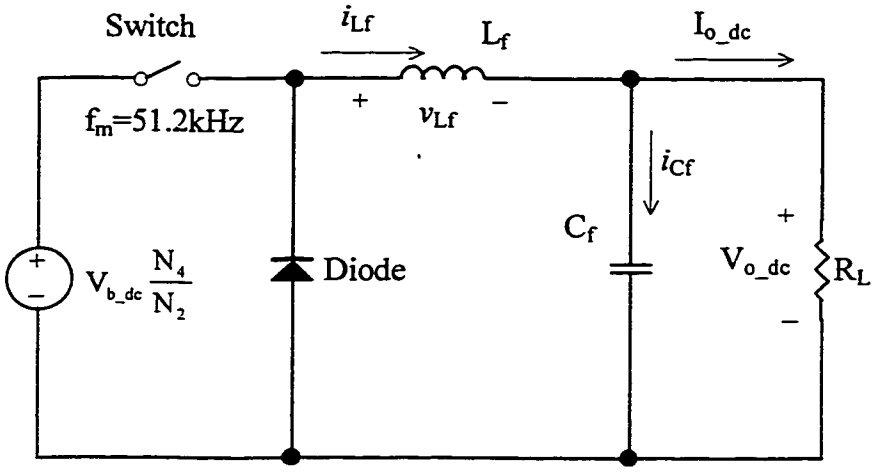


Fig. 3-4 Equivalent circuit of push-pull converter.

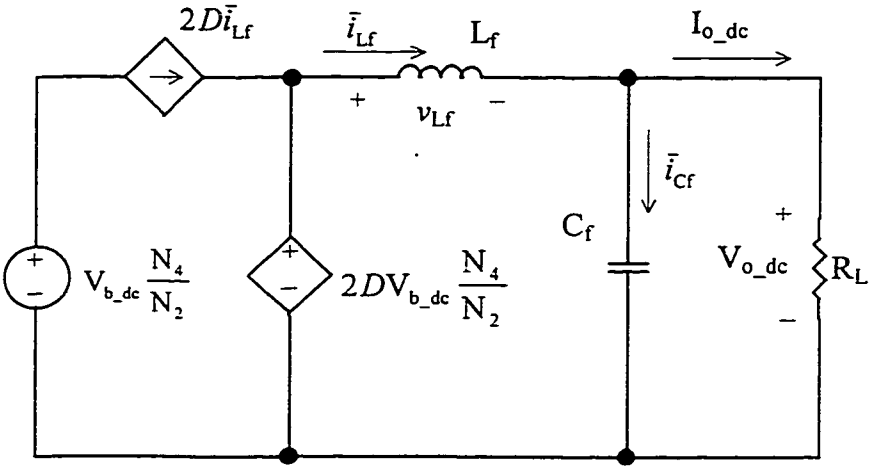


Fig. 3-5 Averaged model of push-pull converter circuit.

where the fector 2 is related with two half cycles.

Compared with Eq.(3-1) and (3-2), if the transformer turns ratio is carefully calculated, the same transfer function G(s) from control-to-output is obtained, no matter that the system is operating under half-bridge status or push-pull status. The transfer

function G(s) is only influenced by the parameters of the transformer ratio, the output filter inductor, and the capacitor, while the output load is fixed.

3.2.3 Output filter

The parameters of the filter inductance and capacitance with the load condition decide the performance of the open loop system as shown in Eq (3-1) and (3-2). On the other hand, the presence of output filter is two-fold: first it stores energy during the off or "notch" periods in order to keep the output current flowing continuously to the load, and second it aids to smooth out and average the output voltage ripple to acceptable levels. Fig 3-6 shows the output filter circuit and its associated voltage and current waveforms. The voltage across the inductor is given by

$$v_{Lf} = L_f \frac{di_{Lf}}{dt} \tag{3-3}$$

Since $v_{Lf} = v_{r\_dc} - v_{o\_dc}$ and $di_{Lf} = \Delta I_{o\_dc}$

$$L_f = \frac{\left(V_{r\_dc} - V_{o\_dc}\right)\Delta t}{\Delta I_{o\_dc}} \tag{3-4}$$

where ΔI_{o_dc} is allowable ripple value of the output dc current.

In the case of the PWM half-bridge or push-pull converter, the voltage V_{r_dc} is approximately twice the value of the output voltage V_{o_dc} at the maximum primary input voltage V_{i_dc} or V_{b_dc}. The time interval Δt is equal to the maximum dead time, or "notch" time, t_{off}, which occurs between alternate switching half cycles.

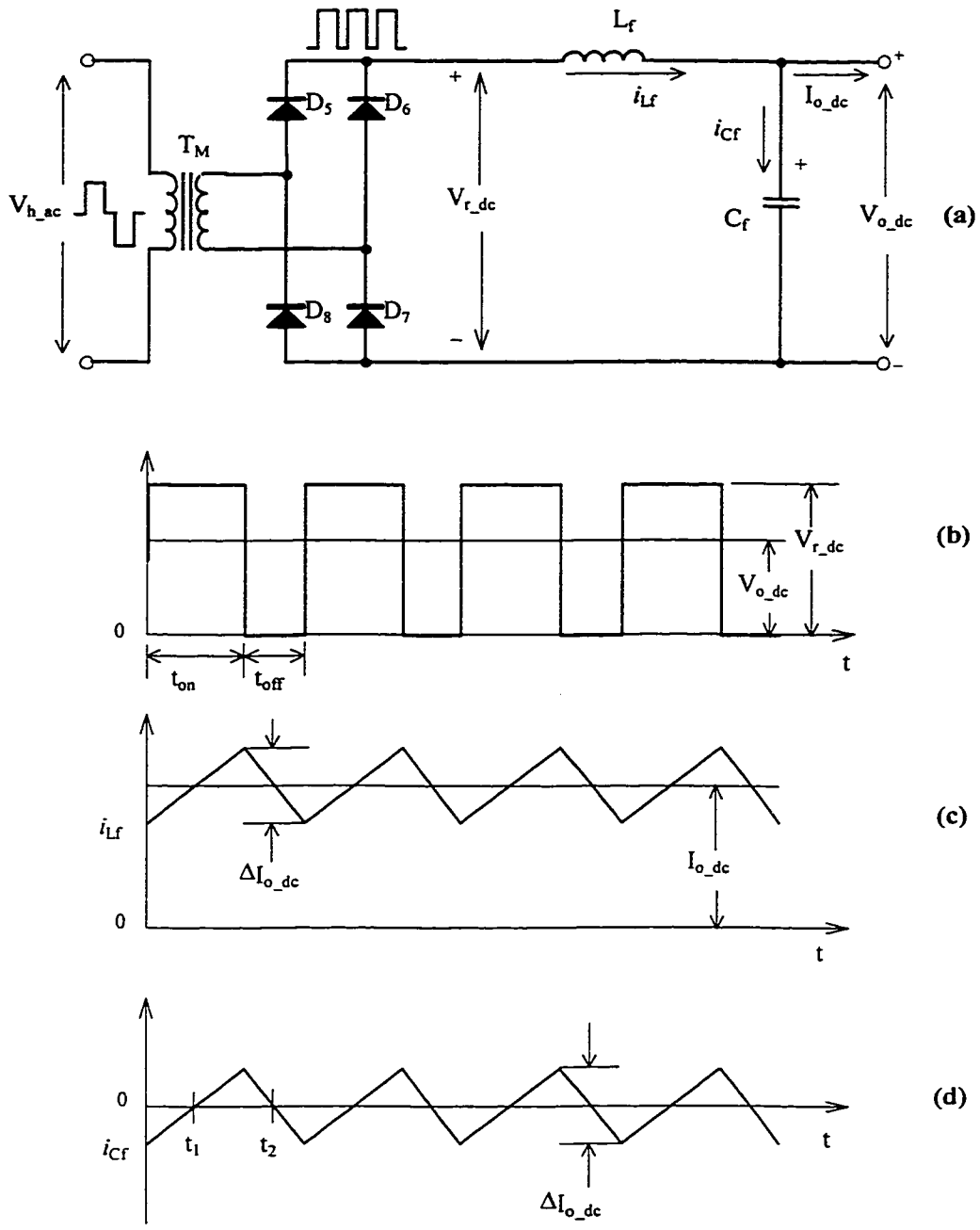


Fig. 3-6 The output filter circuit and its associated voltage and current waveforms. **(a)** output rectifier circuit with the filter inductor L_f and capacitor C_f. **(b)** rectifier output dc voltage V_{r_dc} and filter output dc voltage V_{o_dc}. **(c)** Inductor current i_{Lf} and output dc current I_{o_dc}. **(d)** Capacitor current i_{Cf}.

Maximum t_{off} occurs at maximum input line voltage, since the transistor conduction time t_{on} is at a minimum. Therefore, the inductor must be designed to store enough energy to provide continuous output current during the notch periods. Expressing Δt in terms of secondary voltage V_{r_dc} and V_{o_dc} yields

$$t = t_{off} = \frac{1}{2}\left(\frac{1 - V_{o\_dc}/V_{r\_dc}}{f_m}\right) \qquad (3\text{-}5)$$

where f_m is the converter's modulation frequency, 51.2kHz, which is double of the switching frequency. The factor 1/2 relates the notch time t_{off} to the entire switching cycle, since the total switching period encounters two notch time intervals. In order to keep low inductor peak current and good output ripple, ΔI_{o_dc} should not be greater than $0.25\ I_{o\_dc}$ [8].

Based on the above discussion, Eq (3-4) can be rewritten as

$$L_f = \frac{V_{o\_dc} t_{off}}{0.25 I_{o\_dc}} \qquad (3\text{-}6)$$

While the V_{o_dc} = 270V, t_{off} = 9.76us, and I_{o_dc} = 1.35A, the filter inductance L_f is 7.75mH. In the experimental circuit, the inductance is 8mH.

The current will produce a ripple voltage ΔV_{o_dc} which is given by

$$V_{o\_dc} = \frac{1}{C_f}\int_{t_1}^{t_2} i_{Cf}\,dt \qquad (3\text{-}7)$$

The average current is $\Delta I_{o\_dc}/4$. Therefore, integrating Eq(3 - 7) yields

$$V_{o\_dc} = \frac{\Delta I_{o\_dc}}{4C_f}\frac{T}{2} = \frac{\Delta I_{o\_dc} T}{8C_f} = \frac{\Delta I_{o\_dc}}{8f_m C_f} \tag{3-8}$$

where T is the total period of the on time t_{on} and the off time t_{off}.

Rearranging terms, the minimum output capacitance is

$$C_f = \frac{\Delta I_{o\_dc}}{8f_s \Delta V_{o\_dc}} \tag{3-9}$$

where ΔI_{o_dc} and ΔV_{o_dc} are the allowable peak-to-peak output current and voltage ripple respectively. While I_{o_dc} = 1.35A, f_s = 25.6kHz, then $\Delta I_{o\_dc} = 0.25 I_{o\_dc}$ and ΔV_{o_dc} = 50mV, the capacitance is 33uF. In the experimental circuit, the capacitance is 50uf.

3.2.4 Gain of the open loop

The LC output filter has been designed to have a resonant corner frequency at 250Hz. Since the PWM regulator UC3526A is used as controller, the control voltage V_s swings 2.5V to change the comparator's driver waveform from 0 to 1. The input voltage is 220Vac for half-bridge converter, and 24V battery voltage for push-pull converter. The control-to-output voltage gain for the half-bridge converter is

$$(\text{dc.gain})_{dB} = 20\log\left(\frac{V_{i\_dc}/2}{V_s}\frac{N_4}{N_1}\right) = +45\text{dB} \tag{3-10}$$

the control-to-output voltage gain for the push-pull converter is

$$(\text{dc.gain})_{dB} = 20\log\left(\frac{V_{b\_dc}}{V_s}\frac{N_4}{N_2}\right) = +45\text{dB} \tag{3-11}$$

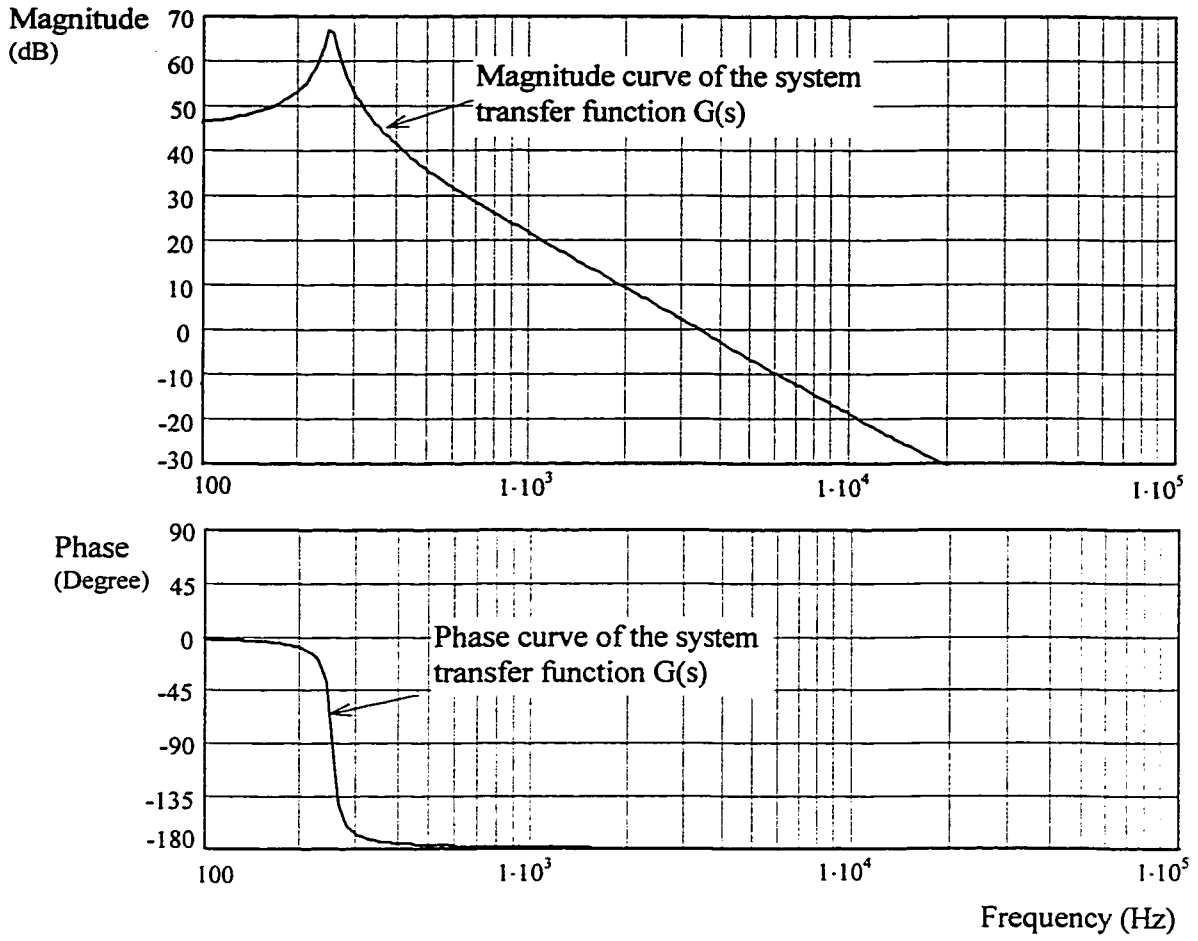


Fig. 3-7 Bode plot of the open loop transfer function G(s).

The results show that two converters have the same characteristics. The Bode plot and phase plot of the open loop transfer function is shown in Fig. 3-7.

3.3 CLOSE LOOP CONTROL

3.3.1 Compensation

The compensated feedback amplifier is designed under taking the following considerations:

(i) Choose an amplifier configuration shown in Fig. 3-8 as a compensation net to have a good transient response;

(ii) Choose the crossover frequency where the gain is unity and the Bode plot crosses at a -1 slope (-20dB per decade);

(iii) Theoretical limits set the crossover frequency at half the switching frequency, but from practical experience less than one-fifth of the switching frequency is used.

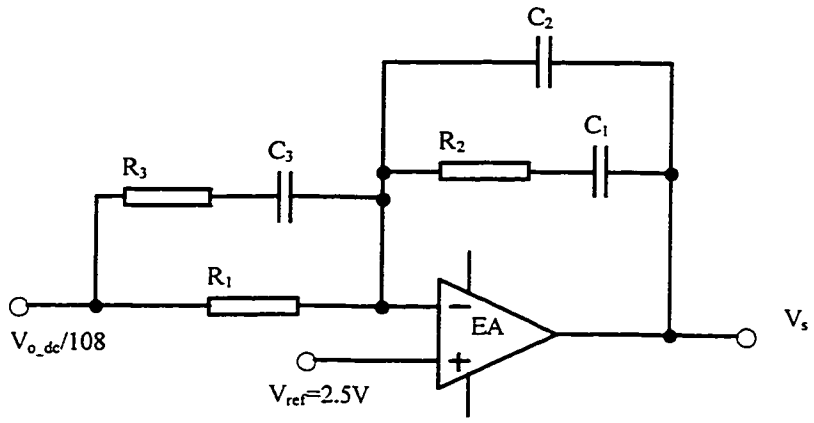


Fig. 3-8 Compensated feedback amplifier.

For this analysis a crossover frequency of 4kHz is chosen, which is about one-fifth the switching frequency and one-tenth the dc output modulator frequency [13] [14].

From Fig. 3-7 by inspection, the control-to-output gain is +45dB at low frequencies, rolling off above 250Hz at -40dB per decade, so that at the chosen crossover frequency of 4kHz the control-to-output gain is -2.5dB. Therefore, for an overall loop gain of zero, the feedback amplifier gain must be made +2.5dB at 4kHz.

The important thing is that the switching power supply will be stable if the overall loop gain crosses over the 0-dB line at a -1 slope. The feedback amplifier must supply a +1 slope at this point for a resulting slope of -1(-20dB per decade). Again, the feedback amplifier gain at 4kHz must be +2.5dB (or 1.33) with a +1 slope. Since the input line voltage to the switching power supply swings from low to high line, the +1 slope must have some margin to span the range of crossover frequencies as the modulator's gain changes with input voltage.

The modulator gain at 250Hz is

$$AV_1 = \frac{250Hz}{4kHz}(1.33) = 0.083 \text{ or } -21 \text{ dB} \qquad (3\text{-}12)$$

Assuming the following characteristics for the feedback amplifier is for plotting its Bode graph. The gain is +2.5 dB at 4kHz and -21dB at 250Hz. A double zero is desired at 250Hz, a pole at 10kHz, and a second pole at 30kHz. The dash line in Fig. 3-9 is a ideal compensation curve. The following parameters are got from the graph

$$AV_1 = -21dB \text{ or } 1.33 \qquad (3\text{-}13)$$

$$AV_2 = 11 \text{ dB or } 3.55 \qquad (3\text{-}14)$$

and

$$f_1 = f_2 = 250 \text{ Hz} \qquad (3\text{-}15)$$

$$f_3 = 10 \text{ kHz} \qquad (3\text{-}16)$$

$$f_4 = 30 \text{ kHz} \qquad (3\text{-}17)$$

The values of resistors and capacitors to give the required results depicted in Fig. 3-8 are calculated as follows. Assuming R_1 = 10 kΩ, and the feedback signal from the output voltage is reduced by 20 times.

$$R_2 = AV_1(R_1) = 16.6k\Omega \quad (3\text{-}18)$$

$$R_3 = \frac{R_2}{AV_2} = 240\Omega \quad (3\text{-}19)$$

$$C_1 = \frac{1}{2\pi f_1 R_2} = 0.038\mu F \quad (3\text{-}20)$$

$$C_3 = \frac{1}{2\pi f_2 R_1} = 0.063\mu F \quad (3\text{-}21)$$

$$C_2 = \frac{1}{2\pi f_4 R_2} = 0.00032\mu F \quad (3\text{-}22)$$

The Bode plot of this compensator transfer function is show in Fig. 3-9.

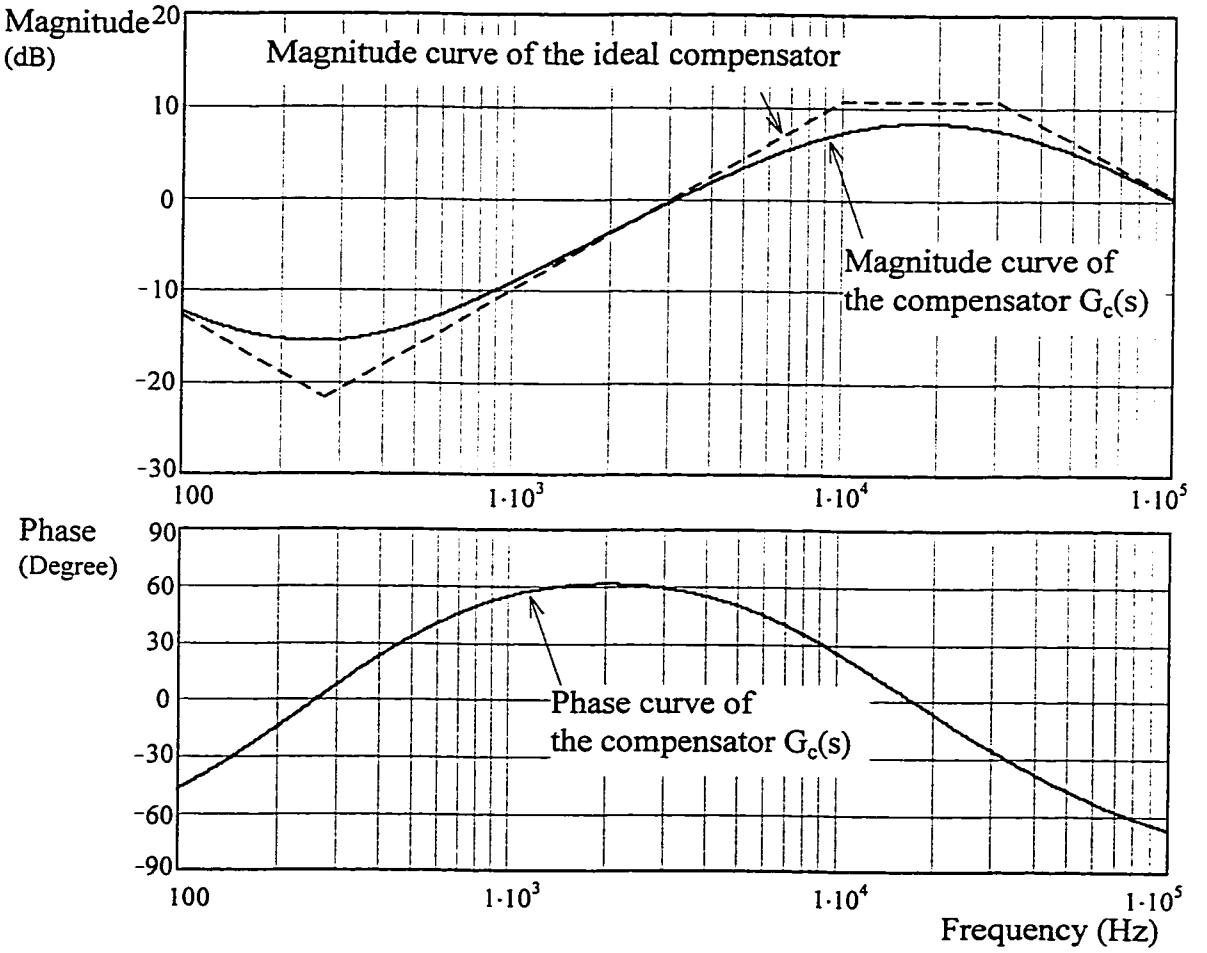


Fig. 3-9 Bode plot of the compensator $G_c(s)$.

3.3.2 Stability

The system transfer function block diagram of the designed close loop control system is shown in Fig. 3-10.

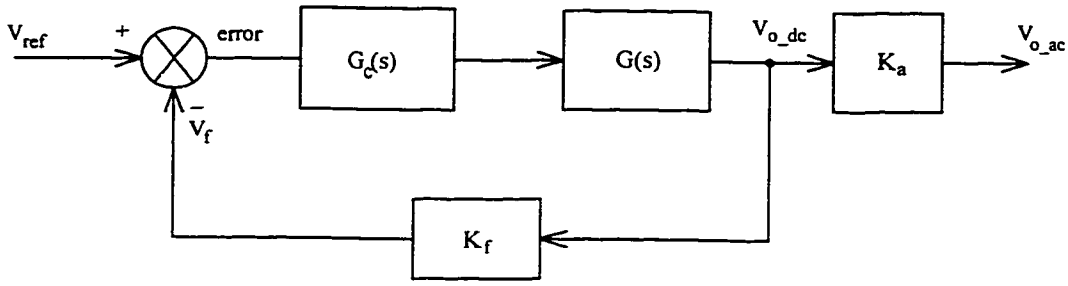


Fig. 3-10 Close control block diagram.

where

$$G(s) = \frac{178}{4 \cdot 10^{-7} s^2 + 4.8 \cdot 10^{-5} + 1} \tag{3-23}$$

$$G_c(s) = \frac{(6.3 \cdot 10^{-4} s + 1)(6.5 \cdot 10^{-4} s + 1)}{3.8 \cdot 10^{-4} s(5.3 \cdot 10^{-6} s + 1)(1.5 \cdot 10^{-5} s + 1)} \tag{3-24}$$

$$K_a = \sqrt{\frac{2}{3}} \tag{3-25}$$

$$K_f = \frac{1}{20} \tag{3-26}$$

The overall loop gain Bode plots are shown in Fig. 3-11. It is shown that the system phase has the margin of 60° at the unity crossover frequency.

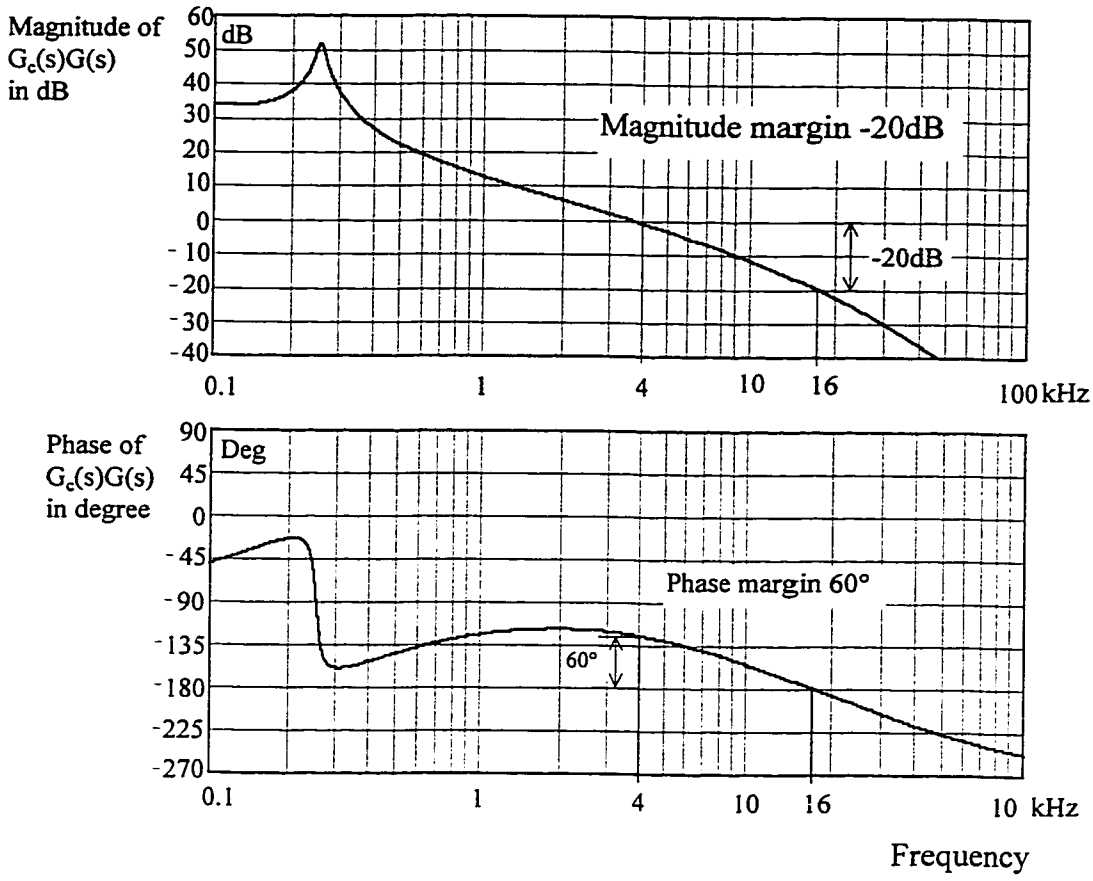


Fig. 3-11 Bode plots of the frequency response of the $G_c(s)G(s)$.

3.4 EXPERIMENTAL RESULTS

3.4.1 System response for load variation

Fig. 3-12 shows responses of the V_{o_ac} and V_{o_dc} to the load variation from 40% to 100% rated, under the ac line input voltage V_{i_ac} of 220V at 60Hz. The results show that the output voltage ripple ΔV_{o_dc} at 100% rated output power is larger than that at 40% rated output power. However the output ac voltage V_{o_ac} still keeps stable. The same results are obtained from battery backup power supply mode. Fig. 3-13 show the

responses of V_{o_ac} and V_{o_dc} to the load condition changing from 40% to 100% rated load, under the battery voltage V_{b_dc} of 24V.

In fact, when quasi-square inverter is working, the output circuit is operating under full load and no load alternatively. It can be seen clearly in Fig. 3-14.

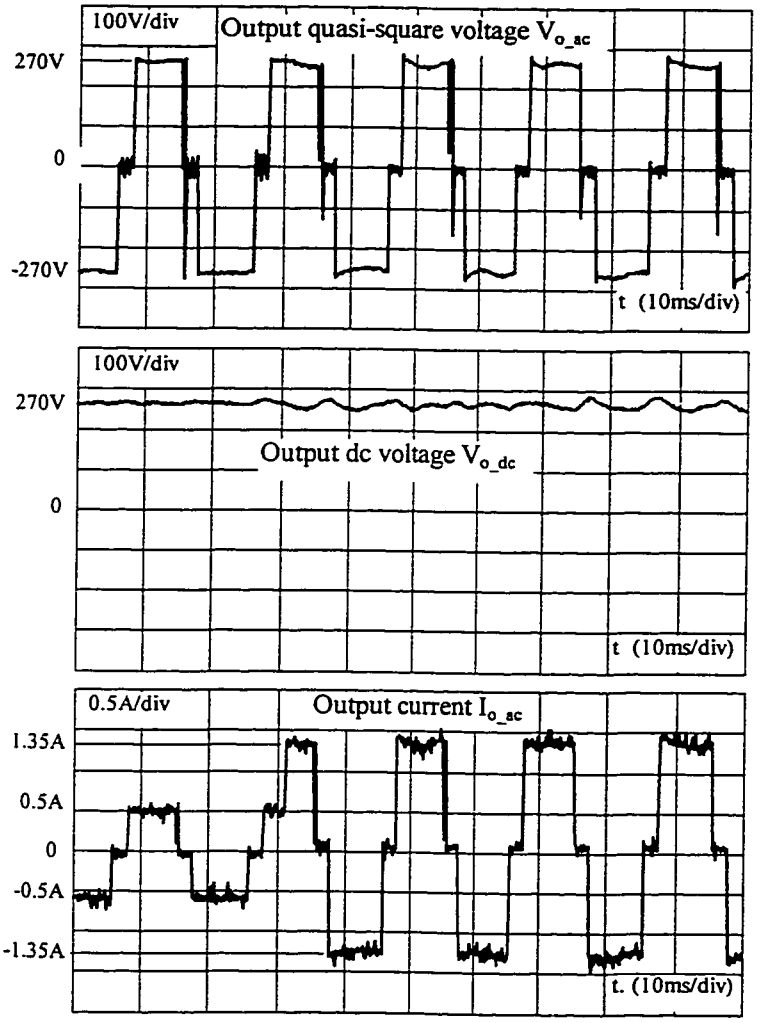


Fig. 3-12 System response to the load variation in the operation mode of ac line power supply.

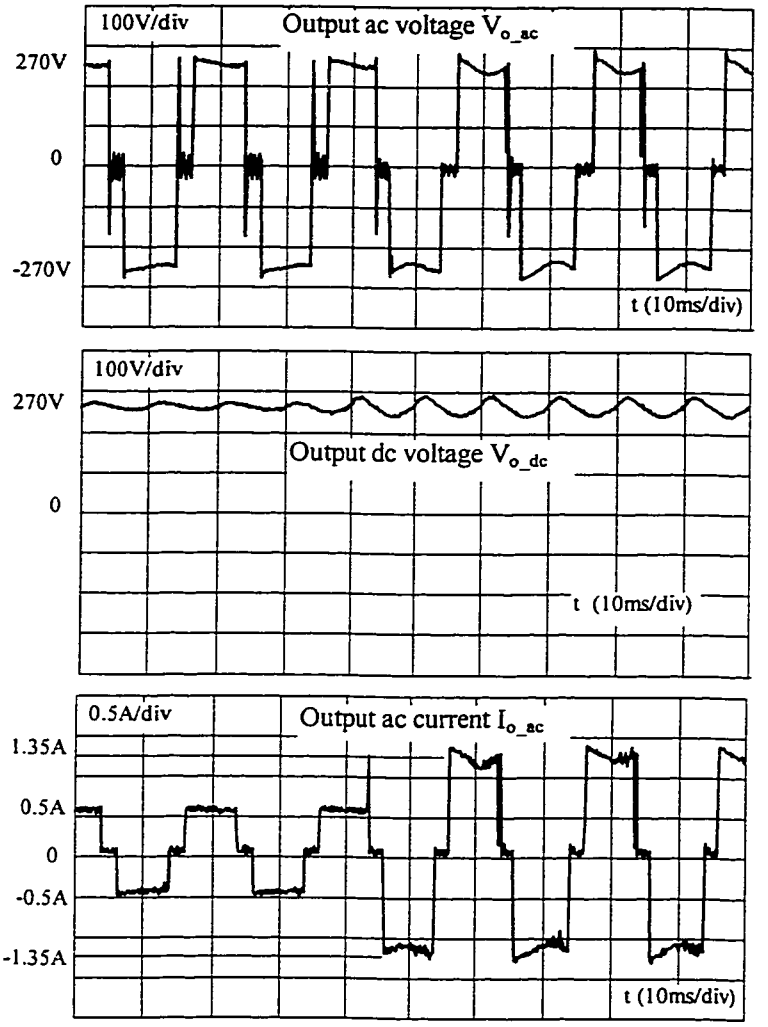


Fig. 3-13 System response to the load variation in the operation mode of battery backup power supply.

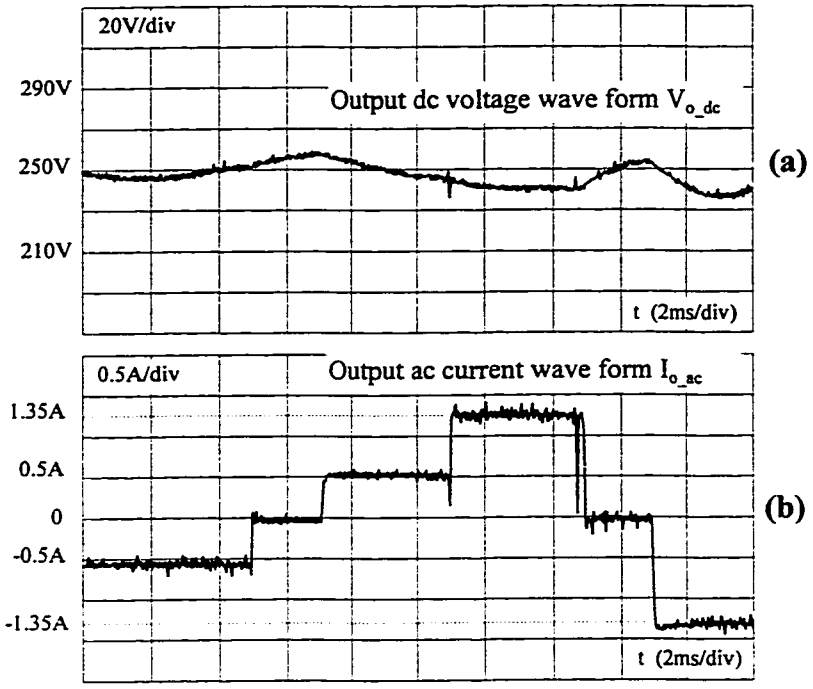


Fig. 3-14 One period waveform of the output ac voltage and current response to the load variation in ac line supply mode.

3.4.2 System response to the input voltage variation

Fig. 3-15 shows the responses of V_{o_ac} and V_{o_dc} to the ac line voltage variation from 180V to 260V. As expected the output is stable against the quick disturbance of the input voltage, and even temporal interruption of the ac line power supply. That means the system has very good quality to anti input power inference. The same results are obtained for V_{o_ac} and V_{o_dc} response against the battery voltage variation from 22V to 24V in Fig. 3-16.

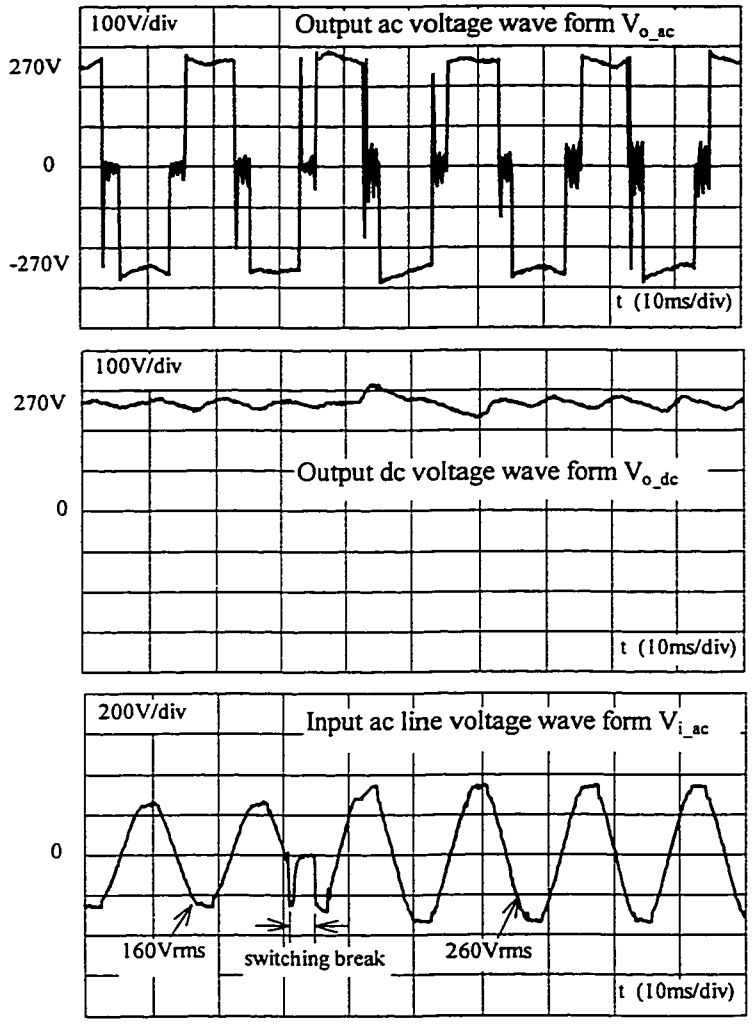


Fig. 3-15 System response to the ac line voltage varies from 160Vrms to 260Vrms.

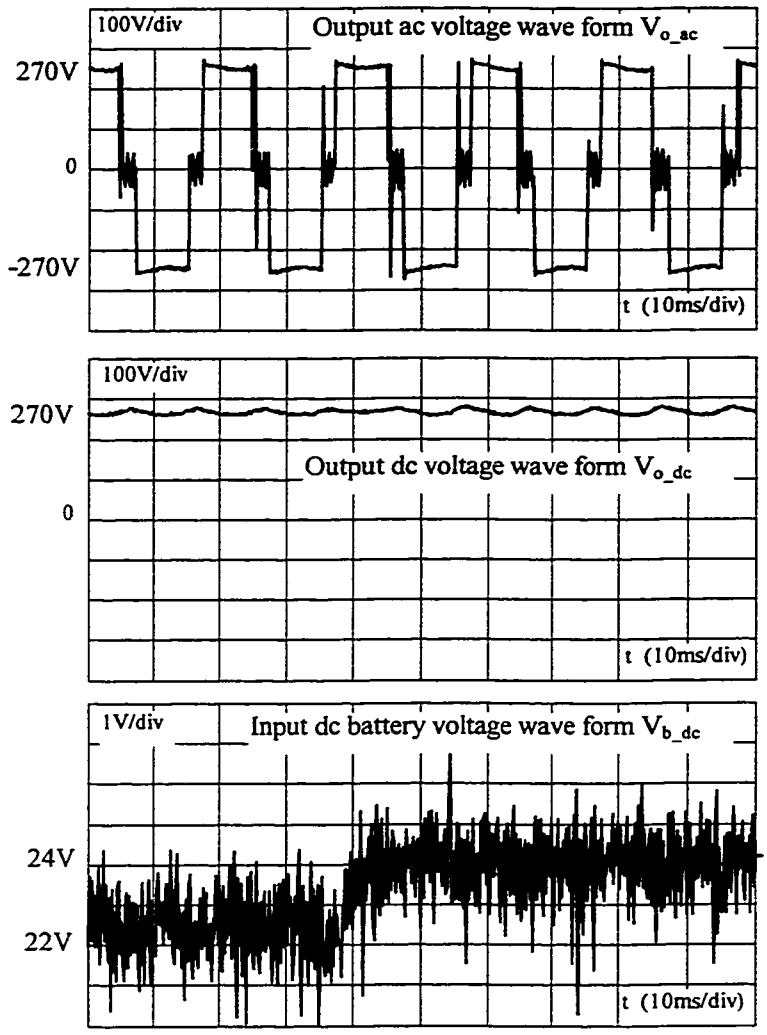


Fig. 3-16 System response to the battery voltage varies from 22V to 24V.

3.5 CONCLUSION

According to the analysis and discussion of the transfer functions, in the proposed control topology, only one simple PWM regulate circuit is required to control both the half-bridge converter and the push-pull converter. The proper operation can be seen from the experimental results. The system has the expected response to the input power

disturbances and the load variations in the two operation status, the system performance is satisfied with the requirements for the consumer application. Furthermore, the close voltage control loop from the output dc side makes the system control simple and easy to implement.

CHAPTER 4

THE ANALYSIS OF THE UPS TRANSITION

4.1 INTRODUCTION

The transfer performance is a very important feature in a UPS system. Generally, the user need fast transition from ac line to backup mode, upon the ac line failure. On-line UPS is the best one for satisfying this requirement. In this chapter, the transitions of the parallel processing ac UPS are discussed.

In section 4.2, the principle of the transition from ac line power supply to dc battery and the reverse process are presented.

In section 4.3, the transition control circuit is analysed.

In section 4.4, the transition experimental results are shown.

4.2 THE TRANSITION BETWEEN AC LINE AND DC BATTERY

4.2.1 Ac line fail

Normally, a fast transition is expected for an on-line UPS system. Fast transition reduces the interference in the operation of the user equipment. The proposed fast switching transition from the ac line to the dc battery supply in this design is finished

within one system switching period, 39us. As there is an output filter before the quasi-square waveform inverter, the switching transition does not produce any influence for the output dc voltage. That means the transition for the system output from the ac line to the dc backup power supply is zero. The basic explanatory curves for the realization of the fast switching transition are shown in Fig. 4-1.

In Fig. 4-1, when ac line fails, the fail signal is generated after the delay of the detector circuit. The maximum delay is depending on the input ac line voltage value. When the ac line fail signal is detected, the switch control circuit does not directly transfer the MOSFET gate control signal from the half-bridge converter circuit to push-pull converter circuit. In stead of that, the gate control signal is still kept to the end of this half period and then the gate signal is transferred while the next half period is coming. Design in this way guarantees the main transformer core will not be of saturate status during the unbalance. This transition operation period is less than 39us. Although the ac line has failed, the energy which is stored in the filter capacitor C_1 and C_2 is still converted to the output in the period of detecting delay, T_{ds}. Based on the analysis in Chapter 2, the input rectifier filter capacitors C_1 and C_2 are designed as to maintain the voltage at the input terminal of the half-bridge converter within this period. Since the detecting delay period is dependent on the lowest allowable voltage on the filter capacitor, the capacitor can support enough energy before the switching transition is coming. The output dc voltage of the half-bridge converter V_{o_dc} is well regulated by PWM control chip as normal. It ensures that there is no any influence in the quasi-square waveform inverter, and the system output voltage transition is zero.

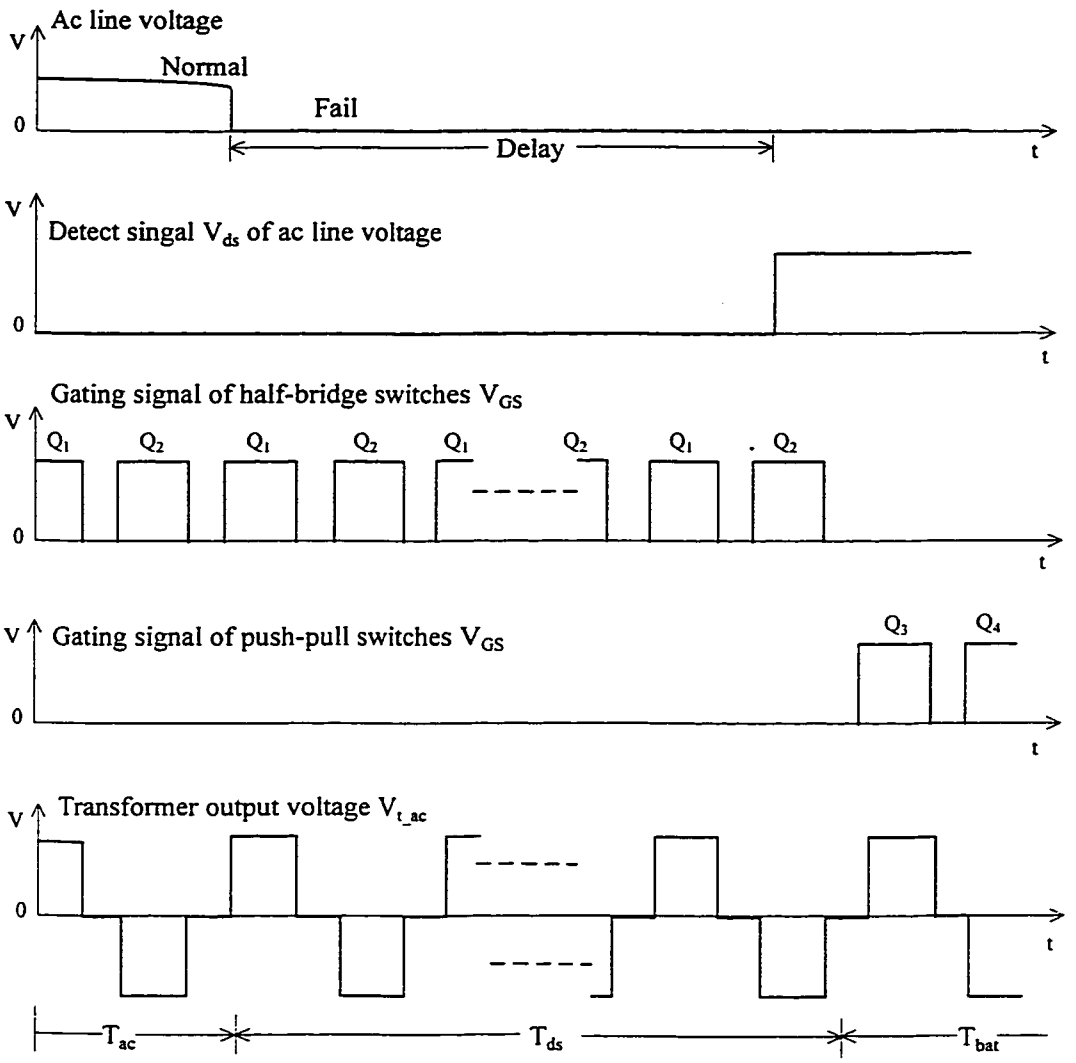


Fig. 4-1 Switching transition during the ac line fails.

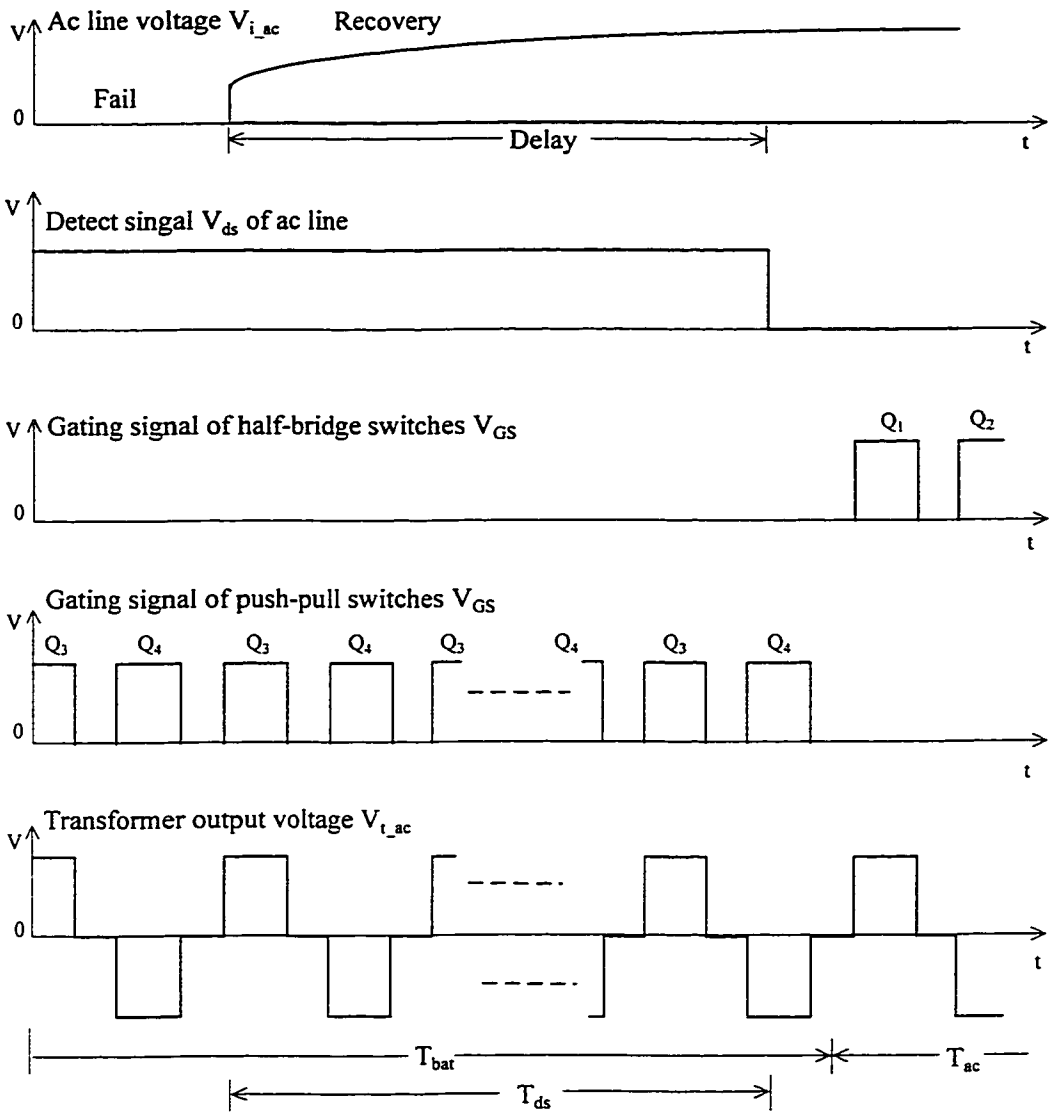


Fig. 4-2 Switching transition while ac line recovery.

4.2.2 Ac line recovery

Fig. 4-2 shows the transitions of the ac line recovery. While the ac line is recovered, the half-bridge converter does not resume to operate immediately. In order to avoid the transformer saturation, it does not drive the half-bridge converter until the end of switching period, then the gating signal is transferred from push-pull converter to half-bridge converter at the beginning of the next switching period. The maximum signal detecting delay is less than 10ms, because the filter capacitor charging can be finished within half cycle of the ac line frequency. The battery energy is continually converted to the output during the detecting delay period. The same results as in the case of ac line failure, the system output dc voltage is not influenced by switching transition from the dc battery to the ac line. There is almost no any influence on the ac output side.

4.3 SWITCHING TRANSITION CONTROL CIRCUIT

In this function control part, the hardware consists of ac line fail and recovery signal detector and signal processor. It is able to control the driver of the half-bridge MOSFETs or the push-pull MOSFETs. The circuit is shown in Fig. 4-3.

4.3.1 Ac line signal detector

The component DB_1 is a full bridge rectifier. C_{df} is a detecting filter capacitor. The time constant τ_d is given by C_{df}, R_1 and R_2:

$$T_d = C_{df}(R_1 + R_2) \qquad (4\text{-}1)$$

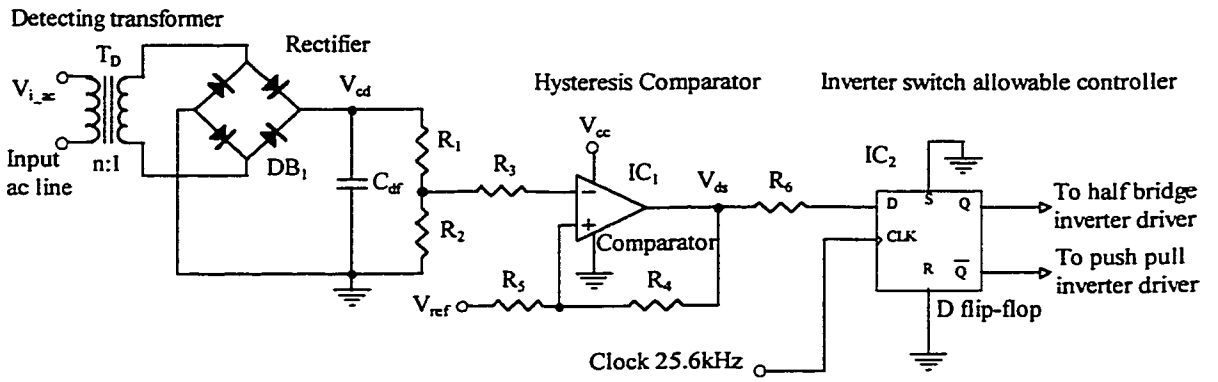


Fig. 4-3 Two inverter switching transition control circuit.

For properly responding to the ac signal variation, τ_d should be equal to the time constant τ_f of the dc filter circuit at the ac line input. When the system output is rated at 300W, the filter capacitance of the half-bridge inverter circuit is selected large enough to maintain the ripple voltage less than 10%. Therefore, the ripple voltage is:

$$V_r = 10\%\sqrt{2}V_{ac} = 30V \qquad (4\text{-}2)$$

According to the Equation (2-8), the filter capacitance after the input rectifier is

$$C = \frac{100P_{i\_ac}}{V_{i\_dc}^2 f_o V_r} = 240uF \qquad (4\text{-}3)$$

where $C = C_1/2 = C_2/2$. In the real circuit, two 800uF capacitors in series to obtain C = 400uF. The time constant of the filter circuit at the rated output is:

$$\tau_f = CR_L = 66ms \qquad (4\text{-}4)$$

where R_L is the rated output load, 165Ω.

According to Eq (4-1), the capacitance C_{df} is

$$C_{df} = \frac{\tau_d}{R_1 + R_2} \qquad (4\text{-}5)$$

While R_1 is 8.2K and R_2 is 5.6K, C_{df} is about 4.8uF.

To meet the requirement of the application, the UPS is operating under the ac line input voltage within 160V to 260V. While the input voltage V_{i_ac} is minimum, 160V, the lowest allowable voltage across the capacitor $V_{i\_dc\_min}$ is

$$V_{i\_dc\_min} = \sqrt{2}V_{i\_ac\_min} - V_r = 196V \qquad (4\text{-}6)$$

This voltage is also the judgement level for the switching transition detecting signal.

When the ac line is interrupted, the filter capacitor voltage V_{i_dc} begins to drop from certain value. Before that voltage drops to 196V, the half-bridge converter is still working and converts the energy which is stored in the capacitor to the output. Fig. 4-4 shows the curves of capacitor voltage dropping from input ac line voltage of 260V, 220V, and 160V respectively. The detecting signal delay period can be verified from the following formulas

$$v_c(t) = V_{i\_dc} e^{-(1/\tau_d)t} \qquad t \geq 0 \qquad (4\text{-}7)$$

where $v_c(t)$ is the instantaneous voltage on the input filter capacitor. While the $v_c(t)$ drops to 196V which is a point of detecting level, the period of the detecting signal delay T_{ds} is:

$$T_{ds} = \tau_f \ln \frac{V_{i\_dc}}{V_{i\_dc\_min}} \qquad (4\text{-}8)$$

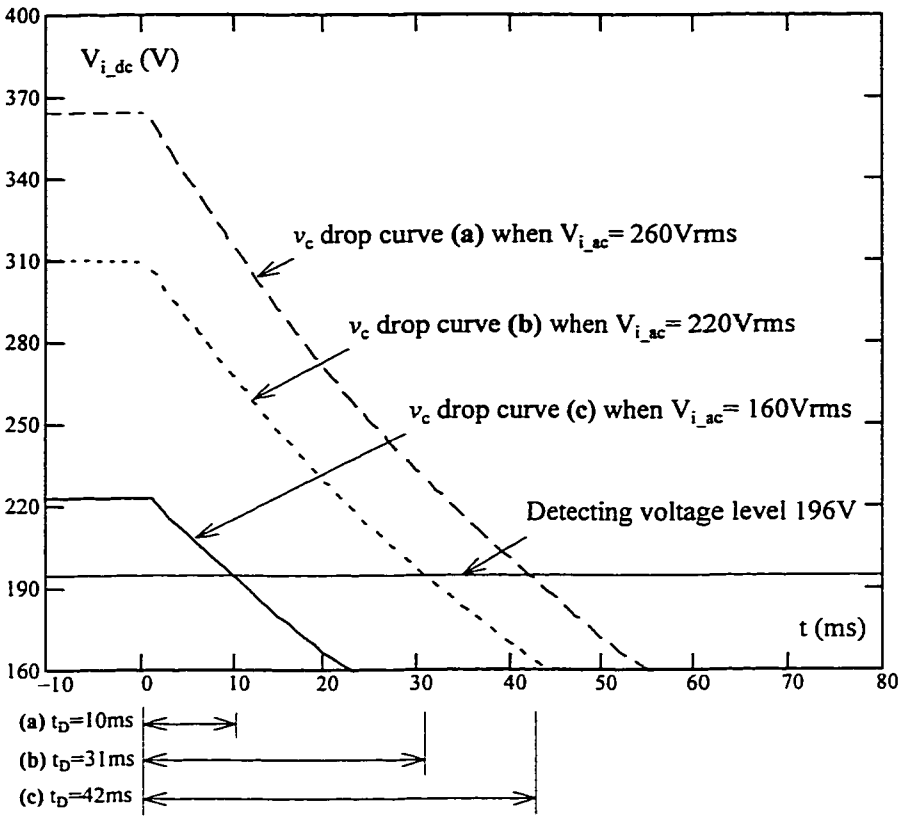


Fig. 4-4 Capacitor voltage dropping curves.

4.3.2 Hysteresis comparator

To avoid the error function, the battery back-up operation starts when ac line voltage is below 160V, and the half-bridge converter operation starts after ac line voltage recovers above 180V. Therefore a hysteresis comparator is used as signal processor and its operation principle is shown in Fig. 4-5. The high threshold voltage V_{TH} is given by

$$V_{TH} = \frac{R_5}{R_4 + R_5}(V_{cc} - V_{ref}) + V_{ref} \qquad (4\text{-}9)$$

where V_{cc} is the control auxiliary power supply voltage, 15V, and

V_{ref} is a reference voltage, 5V.

The low threshold V_{TL} is

$$V_{TL} = \frac{R_4}{R_4 + R_5} V_{ref} \qquad (4\text{-}10)$$

This comparator can effectively overcome the unstable operating situation while the ac line input voltage is around 160V to 180V.

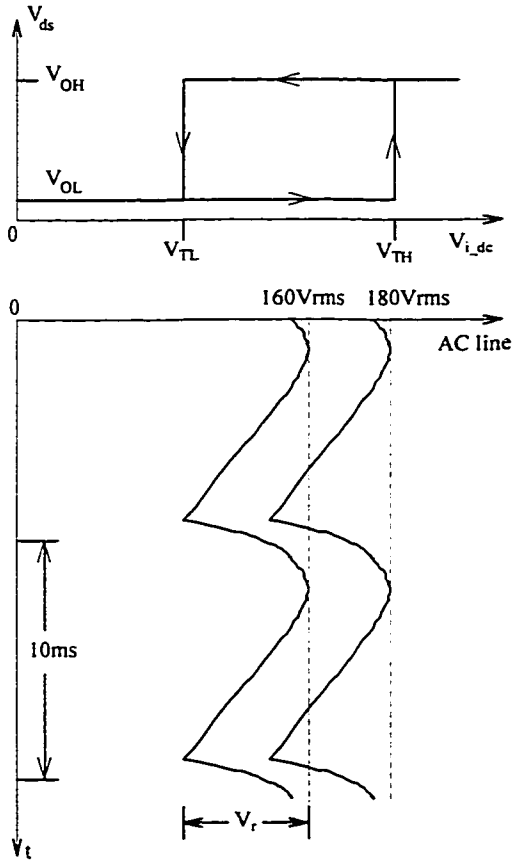


Fig. 4-5 Hysteresis comparator function

4.3.3 D flip-flop

The used D flip-flop chip is a key chip to define the system operation mode depending on the detecting signal from the ac line. Two inputs pins, D and CLK, receive the ac line detecting signal and clock signal respectively. The clock signal is 25.6kHz which is divided from the oscillator in the PWM control chip by a counter. The system operation mode is decided by the status of the two outputs Q and $\overline{Q}$. The truth table of this D flip-flop is shown in Table 4-1.

Table 4-1 D flip-flop truth table

CLK	D	Q	$\overline{Q}$
⎍	0	0	1
⎍	1	1	0
⎎	X	Q	$\overline{Q}$

At the rising time of the clock signal, the output Q and $\overline{Q}$ are changed depending on the status of the D. If the ac line power is normal, D = 0, and thus Q = 0. The half-bridge gating signals are allowable to be sent. The system is operating in mode 1. When ac line fails or is lower than 160V, D = 1 and then $\overline{Q}$ = O, the push-pull converter gating signals are allowable to be sent. The system is operating in mode 2.

4.4 EXPERIMENTAL RESULTS

Fig. 4-6 (a), (b) and (c) show the experimental results of the detecting signal delays corresponding to the ac line voltage of 160V, 220V, and 260V respectively. In Fig. 4-6, the detecting signal V_{ds} is measured at the output of IC1 in the circuit of Fig. 4-3. Fig. 4-6. (a) indicates the ac line fail from 160Vac. V_{ds} delays about 11ms. Fig. 4-6 (b) indicates the ac line fail from 220V. Since the filter capacitor takes longer time to discharge the voltage to the lowest allowable value, V_{ds} delays longer, about 34ms. Fig. 4-6 (c) indicates the ac line fail from 260VAC, V_{ds} delays about 40ms.

For the ac line recover case, there is also signal detecting delay, but it is always less than 10ms. Fig. 4-7 shows that delays are 4ms, 3.6ms, and 2.2ms for the ac voltage of 180Vrms, 220Vrms, and 260Vrms respectively.

The experimental results of output ac transition while ac line fails and recovers are shown in Fig. 4-8, and Fig. 4-9 respectively. In Fig. 4-8, after the ac line fails about 34ms, the detecting signal become active to start the backup power supply mode. The output quasi-square waveform is kept well during the operation mode transition. For the case of the ac line power recovery, there is maximum 10ms delay time to get the detecting signal. In Fig. 4-9, the V_{ds} is delayed about 4ms and the output transition is zero.

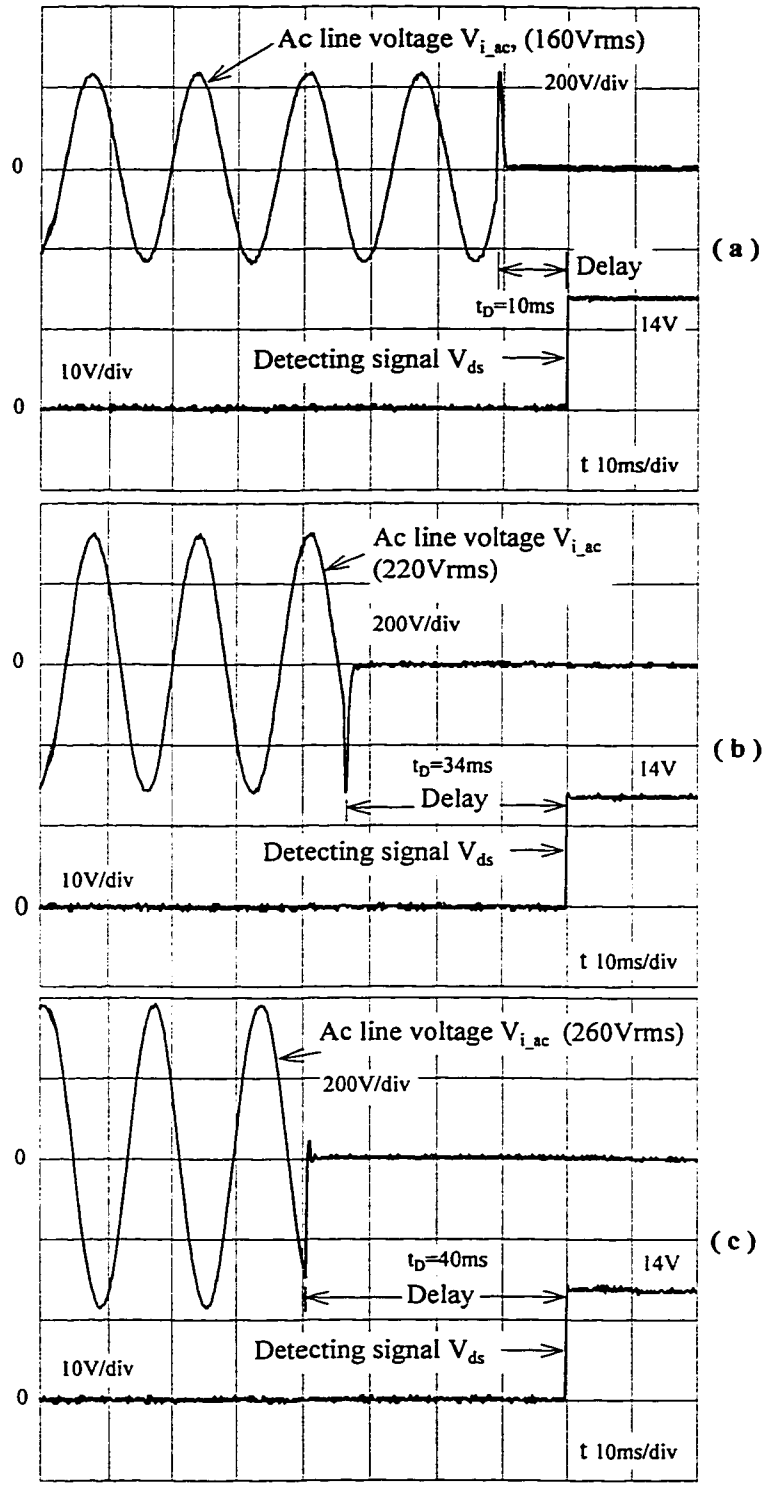


Fig. 4-6 Delay of the detecting signal V_{ds} while the ac line fails.

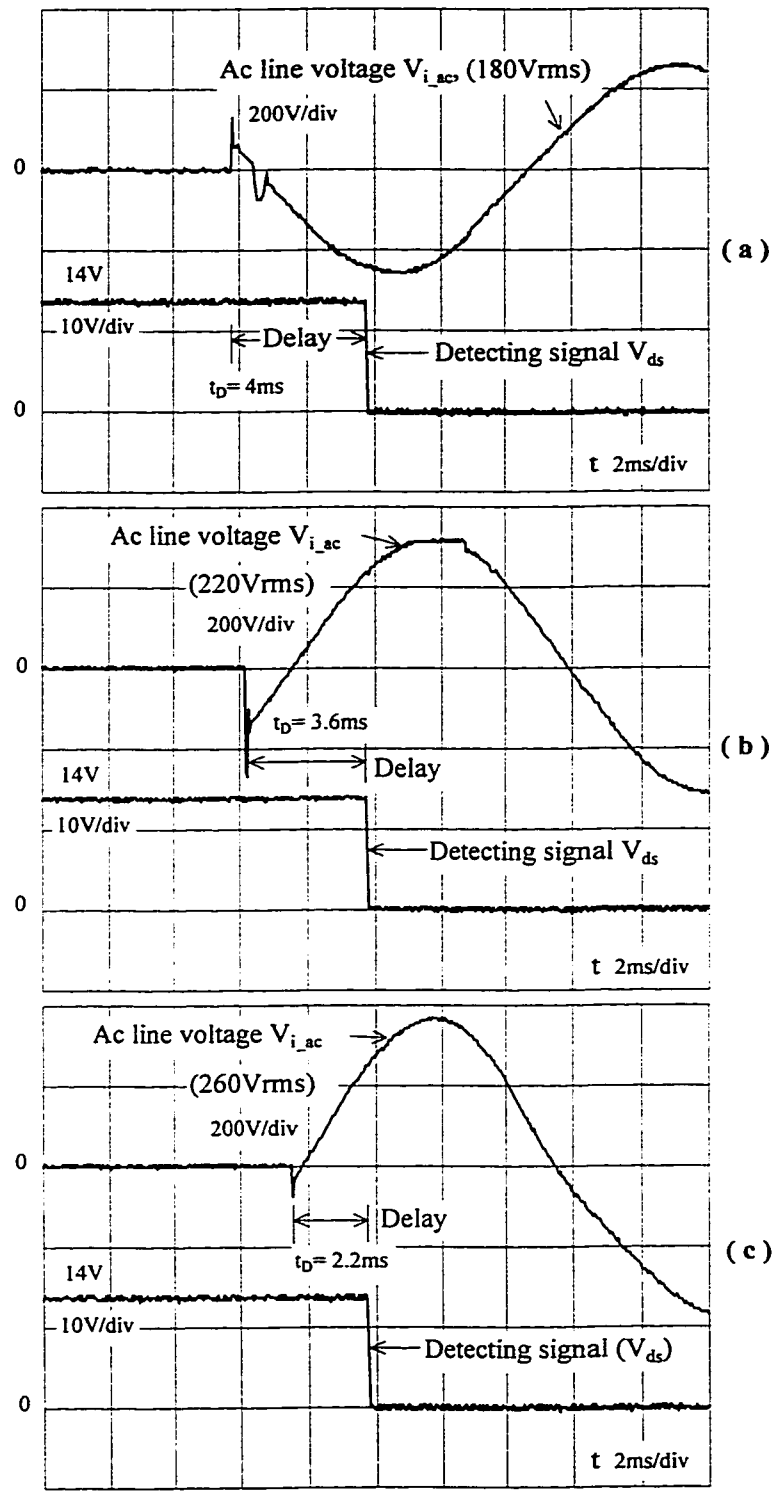


Fig. 4-7 Delay of the detecting signal V_{ds} while ac line recovers

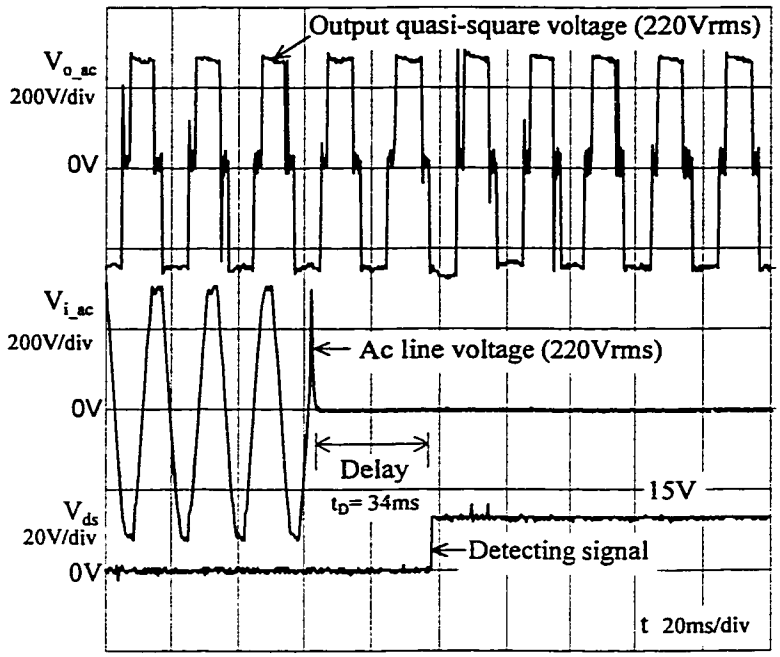


Fig. 4-8 The transition of the ac line fail.

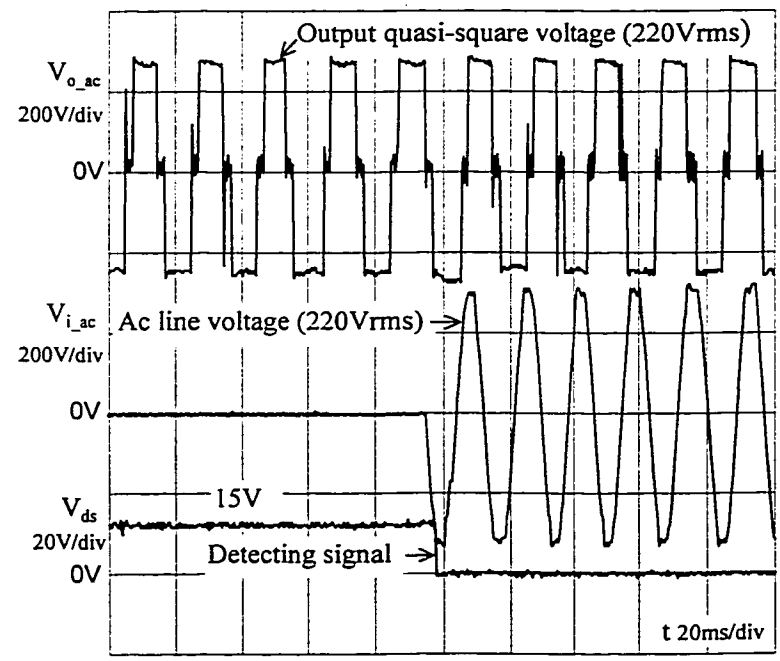


Fig. 4-9 The transition of the ac line recovery.

Observing the output quasi-square waveform and input ac line waveform in these experimental results, there is no synchronic problem in the two operation modes. This advantage is achieved by designing the ac output's frequency and phase dependent on the oscillator in the control chips, and independent on the input ac line's frequency and phase .

4.5 CONCLUSION

As discussed and analysed in this chapter, the transition control circuit effectively realises the zero transition performance. Although there is a detecting delay for both cases of ac line fail and recovery, the filter capacitors which store enough energy support the half-bridge converter to operate during the detecting signal delay. Design in this way ensures the zero transition on the output of the UPS. The control signal switching between two converters, half-bridge converter and push-pull converter, is finished within the normal system switching cycle. The parallel processing topology provides an advance transition performance for the ac UPS.

CHAPTER 5

DESIGN PROCEDURE AND SYSTEM EFFICIENCY

5.1 INTRODUCTION

This chapter discusses the selection of the power components in the six function parts of the parallel processing ac UPS. At the same time, the power loss in each part is analysed. Finally, the efficiency of the two operation modes are presented by the means of calculation and experiment.

Section 5.2 shows the formulas to calculate the components rating and the power loss in each function. Section 5.3 gives the analysis and the experimental results of the system operation efficiency in the two operation modes.

5.2 DESIGN OF THE POWER COMPONENTS

The system specification for designing a 300W UPS is given by:

(i) Output voltage is 220V 50Hz quasi-square wave;

(ii) Input voltage : ac line 160V ~ 260Vrms 50Hz, dc battery 22V ~26V; and

(iii) System switching frequency: 25.6kHz.

5.2.1 Quasi-square wave inverter

Quasi-square wave inverter is a full bridge circuit. Four MOSFETs are used in this part. The output current is

$$I_{o\_ac} = \frac{P_{o\_ac}}{V_{o\_ac}} \qquad (5\text{-}1)$$

Where the peak value of V_{o_ac} is equal to V_{o_dc}, and

$$V_{o\_dc} = \sqrt{\frac{3}{2}} V_{o\_ac} \qquad (5\text{-}2)$$

The peak current pass through the MOSFET is

$$I_{o\_ac\_peak} = \sqrt{\frac{3}{2}} \frac{P_{o\_ac}}{V_{o\_dc}} \qquad (5\text{-}3)$$

Therefore, V_{o_dc} and $I_{o\_ac\_peak}$ give the blocking voltage rating V_{DS} and the conducting current rating I_D of the MOSFETs ($Q_5 \sim Q_8$) respectively.

According to the system specification, P_{o_ac} = 300W and V_{o_ac} = 220V, the $I_{o\_ac\_pek}$ and V_{DS} can be obtained as $I_{o\_ac\_pek}$ = 1.35A and V_{DS} = 270V. Considering the margins of the MOSFET drain current I_D and drain-source voltage V_{DS}, the selected MOSFET should have continuous drain current larger than 3A and drain-source breakdown voltage larger than 400V.

There are two kinds of power losses in this inverter, MOSFET switching power losses and conducting power loss. The total switching power loss P_{qssl} is

$$P_{qssl} = \frac{2I_D V_{DS}(t_r + t_f)}{T_{ac}} \quad (5\text{-}4)$$

where t_r is the rise time of the MOSFET,

t_f is the fall time of the MOSFET,

T_{ac} is the cycle of the output ac voltage.

The total conducting power loss P_{qscl} is

$$P_{qscl} = 2\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} I_D^2 R_{DS(on)} dt = \frac{4}{3} I_D^2 R_{DS(on)} \quad (5\text{-}5)$$

where $R_{DS(on)}$ is the MOSFET static drain-source on-resistance. The total power loss in quasi-square wave inverter, P_{qsl}, is

$$P_{qsl} = P_{qssl} + P_{qscl} \quad (5\text{-}6)$$

5.2.2 High frequency rectifier

The high frequency rectifier circuit consists of four ultrafast recovery diodes and a inductor-capacitor filter.

As the filter parameters have been analysed in section 3.2.3, the filter inductance L_f is

$$L_f = \frac{V_{o\_dc} t_{off}}{0.25 I_{o\_dc}} \quad (5\text{-}7)$$

and the filter capacitance is

$$C_f = \frac{\Delta I_{o\_dc}}{8 f_s \Delta V_{o\_dc}} \qquad (5\text{-}8)$$

where ΔI_{o_dc} and ΔV_{o_dc} are the allowable peak-to-peak output current and voltage ripple respectively. While $I_{o\_dc} = 1.35A$, $f_s = 25.6kHz$, then $\Delta I_{o\_dc} = 0.25 I_{o\_dc} = 0.34$, and $\Delta V_{o\_dc} = 50mV$, The inductance is about 8mH and the capacitance is 33uF.

The maximum current through the fast rectifier diode I_{or_max} is equal to the maximum current through the filter inductor, that is

$$I_{or\_max} = I_{o\_dc} + \Delta I_{o\_dc} = 1.25 I_{o\_dc} \qquad (5\text{-}9)$$

The input ac line voltage has the variation between 160Vrms to 260Vrms. Corresponding to the minimum allowable input voltage of 160Vrms, assuming that the maximum conducting angle δ_{max} is 0.8, then the minimum conducting angle δ_{min} is given by:

$$\delta_{min} = \delta_{max} \frac{V_{i\_ac\_min}}{V_{i\_ac\_max}} = 0.49 \approx 0.5 \qquad (5\text{-}10)$$

The voltage across the diode reaches its maximum value $V_{r\_dc\_max}$ when the input ac voltage is 260Vrms:

$$V_{r\_dc\_max} = \frac{V_{o\_dc}}{\delta_{min}} \qquad (5\text{-}11)$$

When V_{o_dc} is 270V and I_{o_dc} is 1.35A, $V_{r\_dc\_max}$ is 540V, and the forward conducting current I_{FD} is 1.7A. The ultrafast recovery diode should be selected as: dc blocking voltage $V_R > 800V$, and average rectified forward current $I_{F(AV)} > 3A$.

Assuming the filter inductor and capacitor are ideal and lossless components, the power losses P_{orl} in the high frequency rectifier also include two parts, ultrafast recovery diode conducting power loss and turn-on power loss. The conducting power loss P_{fdcl} is

$$P_{fdcl} = 2I_{or}V_F \qquad (5\text{-}12)$$

where V_F is the maximum instantaneous forward voltage of the diode. The fast diode turn-on power loss P_{fdtl} is

$$P_{fdtl} = 2\frac{\frac{1}{2}I_{or}V_{r\_dc}t_{rr}}{T_s/2} = 2\frac{I_{or}V_{r\_dc}t_{rr}}{T_s} \qquad (5\text{-}13)$$

where t_{rr} is the reverse recovery time of the diode. T_s is the system switching period. V_{r_dc} is the voltage across the diode.

5.2.3 High frequency transformer

The core size of the high frequency transformer [8] [15] is

$$A_eA_c = \frac{\left(0.68P_{o\_dc}D\right)10^3}{f_sB_{max}}\text{cm}^4 \qquad (5\text{-}14)$$

Where A_e = core effective area, cm^2

A_c = bobbin winding area, cm^2

D = operating current density, c.m./A

B_{max} = peak operating flux density of core, G.

The number of primary turns [8] is

$$N_1 = \frac{(\frac{1}{2} V_{i\_dc\_min})10^8}{K f_s B_{max} A_e} \qquad (5\text{-}15)$$

Where K = 4, since the transformer voltage waveform is square.

The transformer turns ratio is

$$\frac{\frac{1}{2} V_{i\_dc\_max}}{N_1} = \frac{V_{o\_dc}/\delta_{min}}{N_2} = \frac{V_{b\_dc\_max}}{N_3} \qquad (5\text{-}16)$$

There are two power losses in the transformer, core losses and copper losses. Core loss depends on the core material and effective core square. Copper losses depend on the magnetic wire AWG. The skin-effect has also influence on the resistance of the magnetic wire. To optimise the transformer size and heat distribution, the core power loss is normally designed to be equal to the copper power loss. Core power loss specification is provided by the manufacturer.

5.2.4 Half-bridge inverter

The half-bridge inverter should be capable of providing power to the output load and compensating the power losses in the quasi-square wave inverter, high frequency rectifier, and high frequency transformer. Therefore, the maximum current through the MOSFET Q_1 drain I_{hb} is

$$I_{hb} = \frac{P_{hb}}{\delta_{max} V_{i\_dc\_min}/2} = \frac{P_{o\_ac} + P_{qsl} + P_{orl} + P_{mtl}}{\delta_{max} V_{i\_dc\_min}/2} \qquad (5\text{-}17)$$

where P_{hb} is the output power of half-bridge inverter. P_{mtl} is the power loss of high frequency transformer. Assuming the total power loss is less than 20% of the output power, I_{hb} is about 4.2A.

The maximum voltage across the MOSFET Q_1 (Q_2 is the same) V_{DS_max} is equal to $V_{i\_dc\_max.}$, and $V_{i\_dc\_max}$ = 368V corresponding to the maximum ac line voltage 260V. Therefore, the selected MOSFET should have $V_{DS} > 400V$, and $I_D > 6A$.

The switch conducting power loss in the half-bridge inverter, P_{hbcl}, is,

$$P_{hbcl} = \delta_{max} I_{hb}^2 R_{DS(on)} \qquad (5\text{-}18)$$

And, switching power loss P_{hbsl} is

$$P_{hbsl} = \frac{I_{hb} V_{DS} (t_r + t_f)}{T_s} \qquad (5\text{-}19)$$

The total power loss in the half-bridge, P_{hbl}, is

$$P_{hbl} = P_{hbcl} + P_{hbsl} \qquad (5\text{-}20)$$

5.2.5 Push-pull inverter

The push-pull inverter should be capable of providing power to the output load and compensating the power losses in the quasi-square wave inverter, high frequency rectifier, and high frequency transformer. Therefore, the maximum current through the MOSFET Q_3 drain, I_{pp}, is

$$I_{pp} = \frac{P_{pp}}{\delta_{max} V_{b\_dc\_min}} = \frac{P_{o\_ac} + P_{qsl} + P_{orl} + P_{mtl}}{\delta_{max} V_{b\_dc\_min}} \qquad (5\text{-}21)$$

where P_{pp} is push-pull inverter output power. If the total power loss is less than 20% of the output power, I_{pp} is about 22A.

The maximum voltage across the MOSFET Q_3 (Q_4 is the same) V_{DS_max} is equal to $2V_{b\_dc\_max.}$ Since $V_{b\_dc\_max} = 26V$. The selected MOSFET should be $V_{DS} > 60V$, and $I_D > 30A$.

The power loss in the push pull inverter is also caused by switching and conducting power losses of the MOSFETs. The switch conducting power loss in the push-pull inverter, P_{ppcl}, is,

$$P_{ppcl} = \delta_{max} I_{pp}^2 R_{DS(on)} \qquad (5\text{-}22)$$

And, switching power loss, P_{ppsl}, is

$$P_{ppsl} = \frac{I_{pp} V_{DS} (t_r + t_f)}{T_s} \qquad (5\text{-}23)$$

The total power loss in the push-pull inverter, P_{ppl}, is

$$P_{ppl} = P_{ppcl} + P_{ppsl} \qquad (5\text{-}24)$$

5.2.6 Input rectifier

The average current pass through the rectifier diodes, I_{ir}, is

$$I_{ir} = \frac{P_{ir}}{V_{i\_ac\_min}} = \frac{P_{hb} + P_{hbl}}{V_{i\_ac\_min}} \qquad (5\text{-}25)$$

The maximum voltage across the rectifier diode is

$$V_{r\_max} = 2\sqrt{2}V_{i\_ac\_max} \quad (5\text{-}26)$$

Therefore the rectifier diode is chosen to be $V_R > 800V$ and $I_{F(AV)} > 3A$ when 80% of the system efficiency is considered.

The power loss in the input rectifier is not the same as that of the high frequency rectifier. There is no switching power loss of the diode, because the input voltage wave form is sinusoidal.

$$P_{irl} = 2I_{ir}V_F \quad (5\text{-}27)$$

5.2.7 Power Components

Based on the above discussion, the power MOSFETs in the main power circuit of the UPS are chosen as in Table 5-1. The diode parameters are shown in Table 5-2. Table 5-3 shows the main high frequency transformer parameters.

Table 5-1 MOSFET parameters [16]

Symbol	Mode	V_{DSS}	$R_{DS(on)}$	I_D	t_r	t_f
Q_1, Q_2	IRFP460	500V	0.27Ω	20A	59ns	58ns
Q_3, Q_4	IRFP150	100V	0.055Ω	41A	120ns	81ns
Q_5 to Q_8	IRF840	500V	0.85Ω	8A	23ns	20ns

Table 5-2 Diodes parameters [17]

Symbol	Mode	V_R	$I_{F(AV)}$	V_F	t_{rr}	t_{fr}
D_1 to D_4	1N5408	1000V	3A	1.2V	-	-
D_5 to D_8	MUR4100	1000V	4A	1.85V	100ns	75ns

Table 5-3 The transformer parameter [15]

Symbol	Mode	A_e	A_c	Core loss	Weight	N_1:N_2:N_4
T_m	PC30EE65	2.66cm^2	5.53cm^2	5.99W	214g	44:6:124

5.3 EFFICIENCY

5.3.1 Efficiency in operation mode 1

In operation mode 1, the power flow path has been shown in Figure 2-2. The efficiency is influenced by ac-input rectifier power loss (P_{irl}), half-bridge inverter power loss (P_{hbl}), main high-frequency transformer power loss (P_{mtl}), output high-frequency rectifier power loss (P_{orl}), quasi-square wave inverter power loss (P_{qsl}), and flyback converter power loss (P_{flyl}). When the battery is full, the flyback converter power loss can be neglected. The total power loss (P_{acl}) is

$$P_{acl} = P_{irl} + P_{hbl} + P_{mtl} + P_{orl} + P_{qsl} \qquad (5\text{-}28)$$

According to the power loss formulas derived in the section 5.2 and the components parameters shown in the section 5.2.7, the power of each part can be obtained by the following steps:

(i) Quasi-square wave inverter power loss P_{qsl}

The conducting power loss P_{qscl} is

$$P_{qscl} = 2 \times \frac{2}{3} I_D^2 R_{DS(on)} = 2 \times \frac{2}{3} \times 1.35A^2 \times 0.85\Omega = 2W \qquad (5\text{-}29)$$

and the switching power loss P_{qssl} is

$$P_{qssl} = 2 \times \frac{\frac{1}{2} I_D V_{DS} (t_r + t_f)}{T_{ac}/2}$$

$$= 2 \times \frac{\frac{1}{2} \times 1.35A \times 270V(23ns + 20ns)}{20ms/2} = 1.6 \times 10^{-3} W \qquad (5\text{-}30)$$

The MOSFET switching power loss can be neglected compared with P_{qscl}. The power loss in the quasi-square wave inverter is

$$P_{qsl} = P_{qscl} + P_{qssl} = 2W \qquad (5\text{-}31)$$

(ii) Output high-frequency rectifier power loss P_{orl}

The total power loss in the high frequency rectifier is

$$P_{orl} = 2\left[I_{or} V_F + \frac{\frac{1}{2} I_{or} V_{r\_dc} t_{rr}}{T_s/2} \right]$$

$$= 2 \times \left[1.35A \times 1.85V + \frac{\frac{1}{2} \times 1.35A \times 540V \times 100ns}{19.5us} \right]$$

$$= 9W \qquad (5\text{-}32)$$

(iii) Main high-frequency transformer power loss P_{mtl}

As mentioned in TDK Ltd for its product, PC30EE65/65/13-Z, the power loss is less than $6W$ at 25kHz [15]. Assuming the copper power loss of the transformer is the same as core power loss, the total power loss of the main transformer P_{mtl} is 12W.

(iv) Half-bridge inverter power loss P_{hbl}

The maximum current through the MOSFET Q_1, I_{hp}, is

$$I_{hb} = \frac{P_{hb}}{\delta_{max} V_{i\_dc\_min}/2} = \frac{P_{o\_ac} + P_{qsl} + P_{orl} + P_{mtl}}{\delta_{max} V_{i\_dc\_min}/2}$$

$$= \frac{300W + 2W + 9W + 12W}{0.8 \times 226V / 2} = 3.6A \qquad (5\text{-}33)$$

The switch conducting power loss in the half-bridge inverter, P_{hbcl}, is,

$$P_{hbcl} = \delta_{max} I_{hb}^2 R_{DS(on)} = 0.8 \times 3.6A^2 \times 0.27\Omega = 2.8W \qquad (5\text{-}34)$$

and, switching power loss P_{hbsl} is

$$P_{hbsl} = 2 \times \frac{\frac{1}{2} I_{hb} V_{DS} (t_r + t_f)}{T_s}$$

$$= 2 \times \frac{\frac{1}{2} \times 3.6A \times 156V(59ns + 58ns)}{19.5us} = 3.4W \qquad (5\text{-}35)$$

The total power loss in the half-bridge, P_{hbl}, is

$$P_{hbl} = P_{hbcl} + P_{hbsl} = 2.8W + 3.4W = 6.2W \qquad (5\text{-}36)$$

(v) Ac-input rectifier power loss P_{irl}

The current through the rectifier diode, I_{ir}, is

$$I_{ir} = \frac{P_{hb} + P_{hbl}}{V_{i\_ac\_min}} = \frac{323W + 6.2W}{160V} = 2A \qquad (5\text{-}37)$$

The power loss in the rectifier is

$$P_{irl} = 2I_{ir}V_F = 2 \times 2A \times 1.2V = 4.8W \qquad (5\text{-}38)$$

Considering all the power losses discussed above (i) ~ (v), the total system power loss can be obtained by,

$$P_{acl} = P_{irl} + P_{hbl} + P_{mtl} + P_{orl} + P_{qsl} = 4.8W + 6.2W + 12W + 9W + 2W$$

$$= 34W \qquad (5\text{-}39)$$

Therefore, the system efficiency, η_{ac}, is

$$\eta_{ac} = \frac{P_{o\_ac}}{P_{o\_ac} + P_{acl}} = \frac{300W}{300W + 34W} = 89.8\% \qquad (5\text{-}40)$$

The experimental results of the efficiency in the operation mode 1 is shown in Table 5-4. It has a close agreement with the theoretical value obtained from Eq. (5-40).

Table 5-4: Experiment results of system efficiency in the operation mode 1

Condition	Input power	Output power	Efficiency
20% load	70.3*W*	60.4*W*	85.9%
40% load	135.4*W*	120.2*W*	88.8%
60% load	200.7*W*	180.3*W*	89.8%
80% load	268.2*W*	240.7*W*	89.7%
100% load	339.4*W*	302.0*W*	88.9%

5.3.2 *Efficiency in operation mode 2*

In the operation mode 2, the battery provides power for the output by the push pull inverter. The power flow is different from mode 1 and the total power loss is caused mainly by quasi-square wave inverter, high frequency rectifier, transformer, and push pull inverter.

Because the power losses in the quasi-square wave inverter, high frequency rectifier, transformer are the same as that in the half-bridge inverter status, the total power distributed into the main transformer is 317W. For reducing the switch conducting power loss, two MOSFETs are parallel with Q_3 and Q_4.

The current through the MOSFET Q_3 is

$$I_{pp} = \frac{P_{pp}}{\delta_{max} V_{b\_dc\_min}} = \frac{P_{o\_ac} + P_{qsl} + P_{orl} + P_{mtl}}{\delta_{max} V_{b\_dc\_min}}$$

$$= \frac{323W}{0.8 \times 22V} = 18.4A \qquad (5\text{-}41)$$

The switch conducting power loss in the push-pull inverter, P_{ppcl}, is,

$$P_{ppcl} = \delta_{max} I_{pp}^2 R_{DS(on)} / 2 = 0.8 \times 18.4A^2 \times 0.055\Omega / 2 = 7.5W \qquad (5\text{-}42)$$

And, switching power loss, P_{ppsl}, is

$$P_{ppsl} = 2 \times \frac{\frac{1}{2} I_{pp} V_{DS} (t_r + t_f)}{T_s}$$

$$= 2 \times \frac{\frac{1}{2} \times 18.4A \times 24V(110ns + 92ns)}{19.5us} = 4.6W \qquad (5\text{-}43)$$

The total power loss in the push-pull inverter, P_{ppl}, is

$$P_{ppl} = P_{ppcl} + P_{ppsl} = 7.5W + 4.6W = 12W \quad (5\text{-}44)$$

The total power loss of the operation mode 2 can be calculated by,

$$P_{bal} = P_{ppl} + P_{mtl} + P_{orl} + P_{qsl} = 12W + 12W + 9W + 2W$$

$$= 35W \quad (5\text{-}45)$$

Therefore, the system efficiency, η_{dc}, is

$$\eta_{dc} = \frac{P_{o\_ac}}{P_{\_ac} + P_{bal}} = \frac{300W}{300W + 35W} = 89.5\% \quad (5\text{-}46)$$

The experimental results of system efficiency is shown in Table 5-5. The little difference from the theoretical analysis is caused by connecting the battery to the board. In the experiments, due to the high current, there are extra nonnegligible power losses dissipated in the connecting wire and connectors between the battery and board.

Table 5-5: Experiment results of system efficiency in operation mode 2.

Condition	Input power	Output power	Efficiency
20% load	68.2*W*	59.8*W*	87.6%
40% load	135.9*W*	120.1*W*	88.3%
60% load	204.4*W*	179.9*W*	88.0%
80% load	275.2*W*	240.2*W*	87.3%
100% load	345.0*W*	300.5*W*	87.1%

Fig. 5-1 shows the system efficiency curves corresponding to the experimental results in Table 5-1 and Table 5-2. During both two operation modes, the system always has the efficiency above 85%.

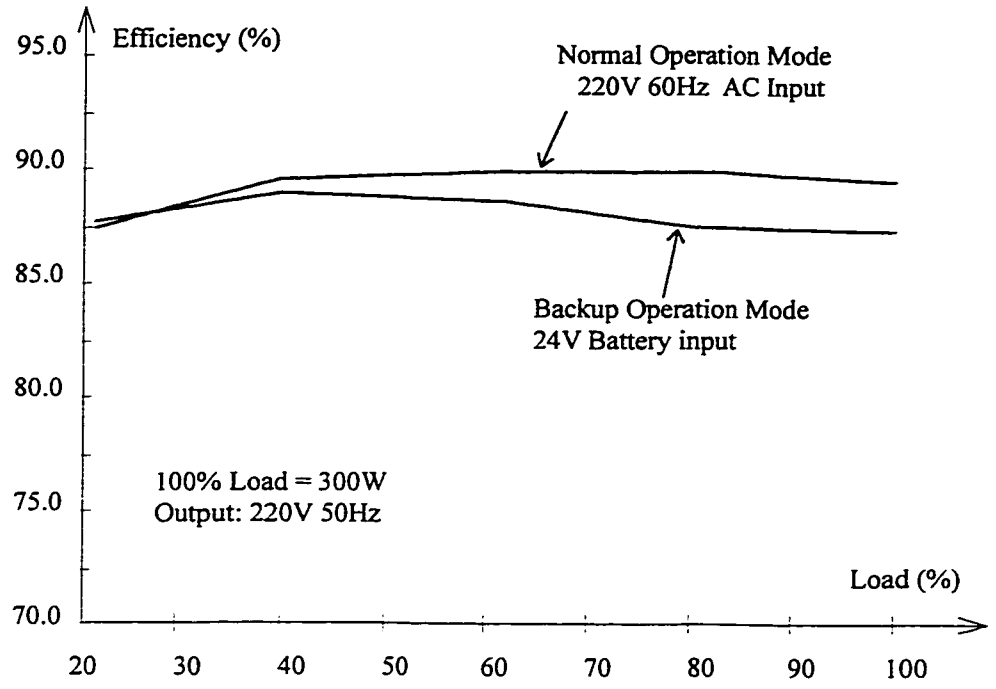


Fig. 5-1 Experimental efficiency curves in two operation modes.

5.4 CONCLUSION

This chapter presents the corresponding formulas to select proper power components and to calculate the system efficiency. From the theoretical analysis and the experimental results, it is shown that the proposed UPS system has an efficiency over 85% in two operation modes.

CHAPTER 6

CONCLUSIONS

6.1 CONCLUSIONS

In this thesis, a high frequency parallel processing ac uninterruptible power supply system has been presented. Two power supply operation modes, normal power supply and backup power supply, of this system are described. The main power circuit topology, output voltage control loop, and operation modes transition control circuit are proposed. The major contributions of this thesis are:

(i) Design of a high frequency parallel processing ac UPS topology. The proposed topology makes the system small and light by using a high frequency transformer. The system steady state performance in both ac line supply and battery backup modes of operation is experimentally verified.

(ii) Design of the system output voltage control loop. According to the derived transfer function, only one PID regulator is required for the control circuits in the both two operation modes. The system stability performance against the input disturbances and the load variations is experimentally verified.

(iii) Design of the fast switching transition control circuit. The transient behavior during the transition between the two operation modes is described. The experimental results show the zero transition for the system output while the ac input line fails and recovers.

(iv) Selection of the power components in the main power circuit for a 300W UPS system.

(v) Evaluation of the system efficiency. Both the theoretical analysis and experimental results show that the system always has the efficiency above 85% for both two operation modes.

6.2 FURTHER WORK REQUIRED

The following works are proposed in the future research:

(i) Using phase shift technique to control the quasi-square wave inverter for more load property application.

(ii) Improving high frequency rectifier topology to reduce the reverse voltage on the rectifier diode, so that the selected diode can be easily found in the market with lower price.

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APPENDIX 1

INTEGRATED CIRCUITS
UNITRODE

UC1526A
UC2526A
UC3526A

Regulating Pulse Width Modulator

FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600kHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation (V_{IN} = Vc = V_{REF} = 5.0V)

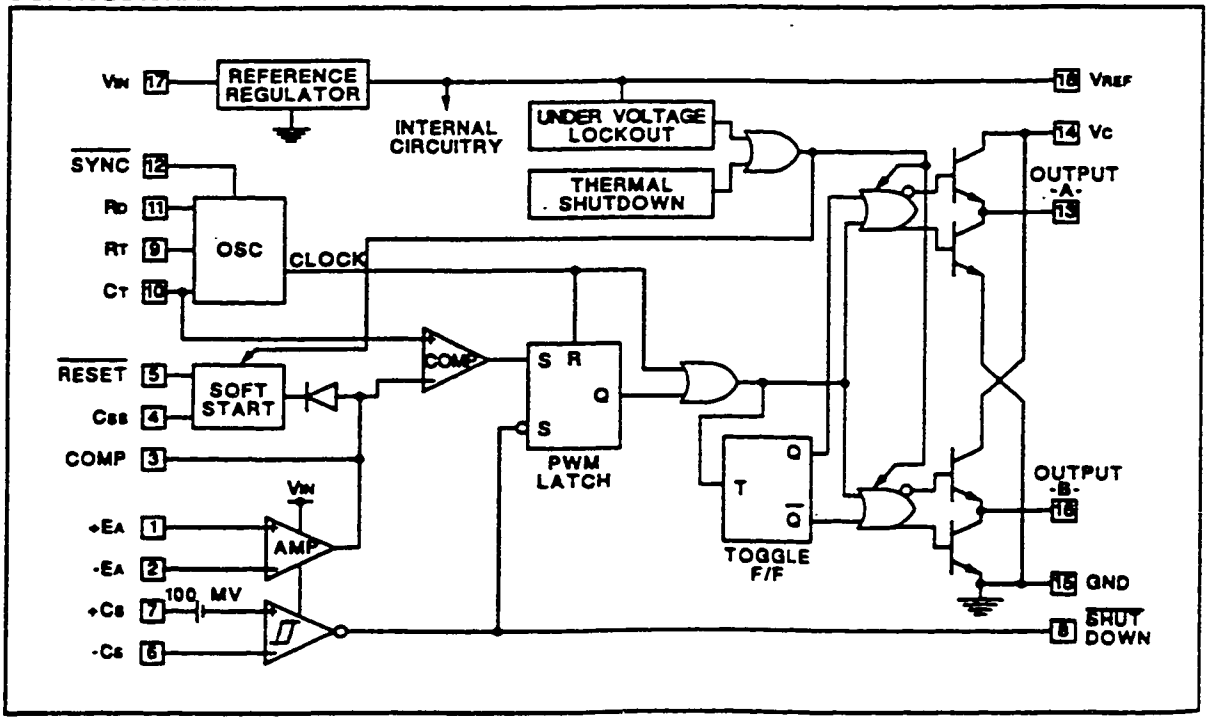
DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non- "A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting V_{IN}, Vc and V_{REF} to a precision 5V input supply. Consult factory for additional information.

BLOCK DIAGRAM



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