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SMR TOPOLOGIES WITH ADVANCED WAVESHAPING FEATURES

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ABSTRACT

SMR TOPOLOGIES WITH ADVANCED WAVESHAPING FEATURES

Athuri Rama Prasad, Ph.D.
Concordia University, 1989

In switch mode ac-to-dc power conversion, a high quality input ac current and output dc voltage are of primary importance. However switch-mode-rectifier (SMR) converters are often designed to produce clean, well regulated outputs while problems with the input side are either ignored or inadequate compensation is provided through the use of typical L-C filters. The present proliferation of switching converters and other non-linear loads is changing this approach and forcing designers to consider converters as generators of both input ac current and output dc voltage waveforms. These ac-to-dc converters are expected to be rugged, cheap, compact, reliable non-interfering with other loads in the vicinity of the converter and isolated for safety and load matching. While these requirements can be met by existing structures at low power levels (less than 1 (one) kW), for medium power levels (3 kW to 20 kW) the above requirements cannot be satisfied because of the bulky L and C components which comprise the various converter filters.

In this thesis, passive and active input-current waveshaping methods suitable for single-phase and three-phase fed ac-to-dc SMR converters are proposed, analyzed and experimentally verified. All these methods discussed maintain high quality input current and output voltage waveforms while providing the necessary ohmic isolation. Finally the associated improved output

voltage control methods needed to compensate for input voltage and load variations are also discussed.

The different modes of operation of the single-phase and three-phase ac-to-dc SMR converters are analyzed in detail and the design expressions are derived. A systematic and comprehensive analysis and design approach is established. This approach is subsequently used to design and implement of the proposed methods.

Finally, in order to establish the feasibility of the proposed passive and active input current waveshaping methods and the associated output voltage control methods, analytical computer based results are verified experimentally.

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Table of Contents

List of Figures

List of Tables

List of Acronyms

HCBR	Half-Controlled Bridge Rectifier
HFL	High Frequency Link
HFT	High Frequency Transformer
PF	Power Factor
PWM	Pulse Width Modulation
SMR	Switch Mode Rectifier
THD	Total Harmonic Distortion
VA	Volt-Ampere
TVA	Total Volt-Ampere

List of Principal Symbols

A_c	Amplitude of the carrier signal
A_f	Amplitude of the reference signal
C_f	Dc link high frequency capacitor
C_i	Input ac filter capacitor of single-phase SMR converter
C_{ia}, C_{ib}, C_{ic}	Three-phase SMR converter input ac filter capacitors
C_o	Dc link filter capacitor
C_r	Resonant ac filter capacitor
C_s	SMR output filter capacitor
D	Duty cycle of the boost switch
d	Order of the dominant harmonic component
E	RMS value of the ac input voltage (E_i)
E_{an}, E_{bn}, E_{cn}	Three-phase SMR converter input ac source phase voltages
$E_{an(peak)}$	Peak value of the input ac voltage E_{an}
E_i	Input ac voltage of single-phase SMR converter
f_c	Carrier frequency
f_{nc}	Normalized carrier frequency
f_s	Switching frequency of the inverter
f_{sw}	Boost switch switching frequency
I_c	Resonant capacitor (C_r) current
I_d	Current through the front-end rectifier diode

I_{db}	Boost diode current
$I_{db,0}$	Average diode current through the diode D_b
$I_{d,0}$	Average current through the front-end rectifier diode
$I_{d,peak}$	Peak current through the front-end rectifier diode
$I_{d,rms}$	RMS current through the front-end rectifier diode
I_f	High frequency transformer primary current
I_{fa}, I_{fb}, I_{fc}	Three-phase high frequency link line currents
I_i	Input ac current of single-phase SMR converter
I_{ia}, I_{ib}, I_{ic}	Three-phase SMR converter front-end rectifier input currents
$I_{ia(peak)}$	Peak value of the current I_{ia}
$I_{ian(rms)}$	RMS value of I_{ian}
$I_{ia,n}, I_{ib,n}, I_{ic,n}$	Amplitudes of the n^{th} harmonic components of currents I_{ia}, I_{ib}, I_{ic}
$I_{ia,1(rms)}$	RMS value of the fundamental component of current I_{ia}
$I_{i,n}$	Amplitude of the n^{th} harmonic component of the current I_i
$I_{i,peak}$	Peak value of current I_i
$I_{i,rms}$	RMS current of I_i
I_{i1}, I_{i2}, I_{i3}	Three-phase SMR converter input ac currents
I_L	SMR dc load current
I_l	Resonant inductor (L_r) current
I_o	Front-end rectifier output current
$I_{o,0}$	Average rectifier output current
$I_{o,n}$	Amplitude of the front-end rectifier output current n^{th} har-

	monic component
I_{rms}	RMS current through the inverter switch
I_s	SMR output current before filtering
$I_{s,n}$	Amplitude of the n^{th} harmonic component of current I_s
$I_{s,n(rms)}$	RMS value of the n^{th} harmonic component of current I_s
L_{fa}, L_{fb}, L_{fc}	Three-phase high frequency transformer equivalent leakage inductances referred to primary
L_i	DC link filter inductor
L_{ia}, L_{ib}, L_{ic}	Three-phase SMR converter inductors
L_{i1}, L_{i2}, L_{i3}	Three-phase SMR converter input ac filter inductors
L_L	Single-phase high frequency transformer leakage inductance referred to primary
L_M	Single-phase high frequency transformer magnetizing inductance
L_r	Resonant ac filter inductor
M_f	Modulation factor of the PWM method
N_p	Number of turns on the transformer primary winding
N_s	Number of turns on the transformer secondary winding
n	Order of the n^{th} harmonic component
P_o	SMR output power
P_r	Front-end rectifier output power
S	Overall switching function of the high frequency inverter and rectifier stages

S_d	Switching function of the front-end three-phase diode rectifier
S_{d1}	Switching function of the boost diode (D_b)
S_i	Switching function of the inverter stage
S_{i1}	Three-phase inverter stage switching function under small line inductance
S_{wb}	Boost switch
T_c	Period of the carrier signal
T_f	Period of the reference signal
T_s	Inverter operating time period
T_{sw}	Boost switch average operating time period
t_{on}	Boost switch 'on' time
t_{off}	Boost switch 'off' time
$\overline{t_1}$	Average 'on' time of the boost switch
$\overline{t_2}$	Average 'off' time of the boost switch
V_{en}	Reflected front-end rectifier input phase voltage
$V_{en,1}$	Amplitude of the fundamental component of the reflected front-end rectifier input voltage
$V_{en,d}$	Amplitude of the dominant harmonic component of V_{en}
V_f	High frequency transformer primary voltage
$V_{fab}, V_{fbc}, V_{fca}$	Three-phase high frequency link line-line voltages
V_G	Gating signal for boost switch
V_{in}	Front-end rectifier output voltage

V_L	DC bus voltage
$V_{L(min)}$	Minimum dc bus voltage
V_r	Voltage across the resonant link
V_s	SMR output voltage
V_{sw}	Inverter switch peak forward voltage
$V_{s,o}$	SMR output dc voltage
$X_{C\,r}$	Impedance of the C_r at fundamental input frequency
$X_{C\,ia,1}$	Impedance of the C_{ia} at fundamental input frequency
$X_{L\,r}$	Impedance of the L_r at fundamental input frequency
$X_{L\,ia,1}$	Impedance of the L_{ia} at fundamental input frequency
Z_n	Equivalent n^{th} harmonic impedance of the input resonant filter
δ	Phase angle between the input ac phase voltage and V_{cn}
ϕ	Input power factor angle
ϕ_1	Phase angle between the input fundamental ac input voltage and the fundamental component of the current
ω	Angular frequency of the input ac source at fundamental frequency
ω_n	Angular frequency of oscillation of the inductor and capacitor
ω_s	Angular frequency of the inverter output frequency

CHAPTER 1

Introduction

1.1 General Introduction

Today, a large number of power conversion equipment produced for telecommunication, military, and space applications are of either thyristor controlled or ferro-resonant design. In both cases the frequency of conversion is 60 Hz. This results in units that are relatively heavy, large, and noisy. The silicon controlled rectifier (SCR) may not be on its way out, but it is certainly being challenged by a number of new semiconductor devices. Among the new devices are the high-power bipolar-junction transistor (HPBT), the power MOS field-effect transistor (MOSFET), the gate turnoff (GTO) thyristor, and the insulated-gate bipolar transistor (IGBT). More efficient, easier to control, and switching faster than the SCR, they are replacing that old standby power supply in a variety of applications. As the new devices become available in more impressive voltage and current ratings, they are bringing about a quiet revolution for the electrical industry. Designers have embraced their broad usefulness for such diverse tasks as switching and uninterruptible power supplies, electronic ballasts for fluorescent lighting, induction heating and welding, automotive power systems, appliances, drives equipment ranging from robots to railroad locomotives, and adjustable speed drives for brushless dc motors and induction motors.

All these new devices function as controlled switches, processing power in conditioning circuits to match the source with the requirements of the load: dc to dc or ac, ac to ac or dc. The high switching frequency means more

circuits can be accommodated into a given space, making power-conditioning systems more compact, since size of inductors, transformers and capacitors needed for filtering and energy storage in such systems shrinks as frequency increases. The high switching frequency also brings faster system response than can be achieved with SCRs.

The main design objective in any high frequency ac-to-dc switch-mode-rectifier (SMR) converter is the minimization of the converter's size and weight while maintaining acceptable component stresses and providing isolation for safety and load matching. Furthermore, control of the output voltage is essential in most power supply systems either to compensate for input source voltage variations and internal regulation or because the load demands adjustable voltage or both. Consequently, SMR converters consist of two main power conversion stages as shown in Fig. 1.1. The first stage is an ac-to-dc rectifier fed from a single-phase or a three-phase ac source. The second stage is a dc-to-dc converter with a high frequency transformer. An increase in the switching frequency is used for size reduction because the volume of the converter depends mainly on the size of the magnetic components and associated filter capacitors. To increase the switching frequency, the switching losses of the power switching device should be minimized to prevent overheating. There are two methods to increase the switching frequency. One is to make use of high speed switching devices and are called Switch mode rectifier (SMR) converters. These SMR converters directly rectify the 60-Hz utility voltage, invert at high frequency, transformer couple, and rectify the load voltage. The advantages of these systems are small size, light weight and high efficiency. These circuits generally operate at fixed frequency and control the load voltage by multi pulse pulse-width-modulation (PWM) of the inverter switching devices. The switching device current and voltage can be

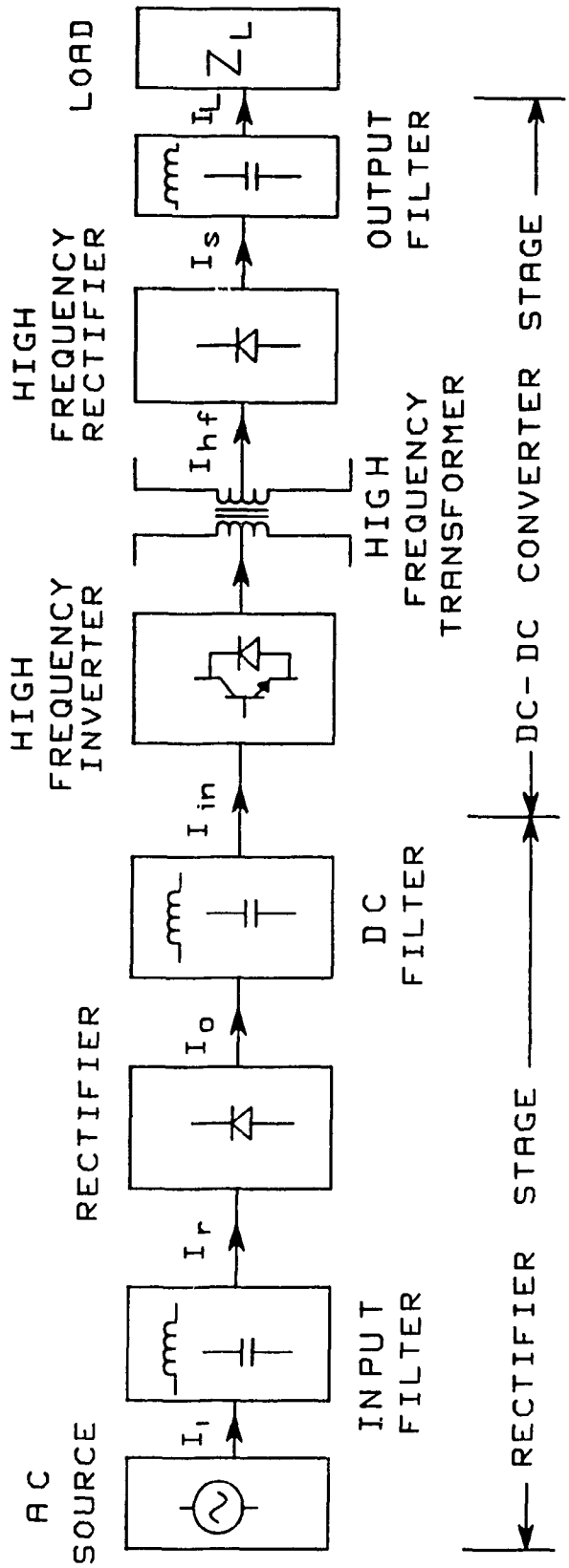


Fig. 1.1: Block diagram of an ac-to-dc SMR converter

approximated by rectangular pulses. The main disadvantage of the SMR converter is the nature of the pulsed current being drawn from the input ac source. This pulsed input current creates number of problems for the power distribution network. These problems are explained later in this chapter.

A second form of high frequency inverter incorporates reactive elements (capacitors and reactors) in conjunction with the switching devices to form a resonant inverter. These circuits control the output voltage by varying the operating frequency of the power semiconductor switches. The advantages of these circuits are low semiconductor switching losses and sinusoidal waveforms. However, resonant converters exhibit increased component count, increased switching stresses (peak current, rms current), and require wide operating frequency variations in order to maintain constant output voltage under large variations of ac input voltage and load.

In a conventional ac-to-dc SMR converter front end single-phase or three-phase line commutated rectifiers or diode rectifiers are used. These rectifiers are attractive because of their inherent ruggedness and simplicity. They require few power circuit elements and control signals are easily generated by simple circuitry (or, as in case of diode rectifier, none are required). However, these circuits impose certain disadvantages upon the power system design. The output voltage of the rectifier is not pure dc but contains a substantial ripple component. The magnitude of this ripple becomes worse as the rectifier delay angle is increased and a dc filter must generally be included to reduce the effect of this ripple on the other blocks in Fig. 1.1 (i.e. high frequency inverter and transformer). This filter now creates additional problems at the ac input to the rectifier. The input current waveform, due to combined effects from the filter and from phase-control action, becomes quite non-

sinusoidal. Depending upon the particular dc filter configuration, the harmonic content of the input current may vary as the phase delay is increased. Furthermore, as the phase delay angle is increased the fundamental component of the input current becomes increasingly phase shifted with respect to the sinusoidal input voltage.

The nonideal character of the input current drawn by standard rectifier circuits creates a number of problems for the power distribution network and for other electrical systems in the vicinity of the rectifier. Phase displacement of the current and voltage fundamentals requires that the source and distribution equipment (i.e., generators and transmission lines) handle reactive power thus increasing their volt-ampere rating. Similarly, the harmonic currents which the power system is required to provide cause an increase in heating and sometimes in peak current levels in the power distribution system. In addition, the impedance of the distribution network will cause these harmonics to distort the supply voltage, causing increased losses and interference on the other loads elsewhere on the power lines (such as computers, appliances, industrial motors, power line carrier communication systems, and relaying equipment).

These effects are undesirable in any power system and as the use of off-line power conditioning equipment becomes more widespread and densely packed, their effect could well be intolerable. It is clear that some form of correction must be used to restrain these problems. In the past, system designers have employed a number of methods to compensate for the poor quality waveforms drawn by the rectifier equipment. These methods include harmonic and reactive compensation by passive elements, multiphase rectification, and active compensation using shunt power converters with a

reactive load. All these methods require extra power handling equipment in addition to the basic rectifier (either 60-Hz capacitors and/or magnetics, or a separate power converter). These extra components add size, weight, and cost to the ac-to-dc conversion system and often have a severe effect on the overall system efficiency, since the rms input current is high.

In a conventional ac-to-dc high frequency link (HFL) converter the second stage consists of an inverter, a high frequency transformer, a high frequency rectifier, an output filter and a load. The inverter block shown in Fig. 1.1 generally operates at fixed frequency and controls the output voltage by multi pulse PWM of the inverter switching devices. Consequently the inverter input current harmonics are pushed to higher frequencies. If the dc filter does not contain any inductance, the inverter input current harmonics can degrade further the input current drawn from the ac input voltage. Therefore some inductance is necessary in the dc filter to improve the input current waveshape. If this dc filter inductor value is too high then it will have a negative impact on the associated inverter control strategy. If the inverter input dc voltage contains any unwanted harmonics, these harmonics will propagate into the high frequency link through the inverter and degrades the performance of the high frequency transformer. Operating the inverter at higher frequencies essentially reduces the size and cost of the isolation transformer considerably.

This thesis addresses the design of a class of ac-to-dc HFL converters which in addition to generating high quality output dc voltage they draw high quality current wave forms from the ac power source. In contrast to conventional HFL converters by utilizing active means the proposed design draws a nearly sinusoidal line current which is in-phase with the input line voltage

thus operating under unity input power factor conditions. It therefore avoids harmonic interference with other loads which are connected to the same ac power source. Furthermore, reactive currents are kept out of the power system, so that the most efficient use is made of the generation and transmission equipment. This class of converters are intended for use in critical applications, such as telecommunications, substations, and hospitals.

1.2 Review of Previous Work

In this section, previous work related to the single-phase and three-phase ac-to-dc HFL converters is reviewed.

1.2.1 Single-Phase Rectifiers

Previous work on single-phase rectifiers can be classified based on the rectifier input current waveshaping method used as a passive and active methods. One of the passive methods frequently used is the diode rectifier with LC filter [1,3]. The maximum input power factor of this method is 0.763. Other passive methods reported in the literature are (i) resonant input filter and (ii) ferro resonant transformer [3]. Both of these methods have the advantage of nearly unity input power factor and also the disadvantage of the high cost of the series capacitor and ferro resonant transformer.

On the other hand, active input current waveshaping methods reduce the size of the rectifier and maintain nearly unity input power factor [3, 12-15,48]. With these methods the dc filter inductor current emulates the ac source voltage and is referred to as a resistor emulator. The disadvantages of this

method are that the switching frequency of the rectifier is load dependent and also that it requires a means of sensing and processing the input ac voltage.

Ohnishi and Okitsu [19] investigated the power factor improvement by means of bias voltage control. In this case the rectifier input voltage is obtained by subtracting the bias voltage from the source voltage. A transformer has been used to give the bias voltage by the output voltage across the load. The cost of the additional transformer and diode bridge makes this scheme not very attractive.

Stihi and Ooi [15] investigated the improvement of input current waveform by hysteresis control. In this method all the diodes are replaced with transistors and feed back diodes. If regeneration is not an issue then the rectifier with a diode bridge and a single active switch for chopping is likely to be cheaper. It also has the disadvantages mentioned above for active methods.

Finally Manias et al. [10], investigated the improvement of the input power factor using a synchronous front end reactor. This method yields nearly unity input power factor using PWM control methods and forces the unwanted harmonic component to higher frequencies. However, it has the disadvantage of complementary switch anti-parallel diode conduction before the transistor turns on and requires the use of at least four additional switches.

1.2.2 Three-Phase Rectifiers

Forced commutated rectifiers are chosen in order to eliminate the drawbacks of the traditional line commutated rectifier. Hence, the application of

PWM control methods to rectifiers is of great interest. However, mainly because of the ruggedness of the line commutated rectifier, PWM rectifiers have attracted little attention in comparison to PWM inverters.

Ziogas et al. [22], investigated the performance of the PWM rectifier. The input and output filter component sizes are reduced by forcing the unwanted harmonics to higher frequencies. However it has the disadvantage of requiring both input and output filter components, which increases the component count.

Malesani and Tenti [23] investigated the PWM converter analysis to obtain the sinusoidal ac line currents with minimum filter requirements. In this method line currents are forced to emulate the input ac source voltage waveform. However the switching frequency of the converter is load dependent.

Ooi et al. [24], investigated the controlled-current PWM converter to obtain the leading power factor. In this method the ac line currents are forced to be within the narrow band of the reference waveform. However this method also has the disadvantage that the switching frequency is load dependent.

The active input power factor improvement method for three-phase rectifiers has been reported in several references [4, 12-14]. In all these references three single-phase rectifiers with active power factor correction method are used with suitable input and output connections. This type of input power factor correction methods exhibits increased component count, and requires complicated input synchronization logic.

1.2.3 DC-DC Converters

For low output power levels the conventional buck, boost, and buck-boost circuits are more economical [16,28]. As the output power level increases, the pulsating either input and/or output current of the buck, boost and buck-boost converters requires large either input and/or output filters.

Steigerwald [11] investigated the performance of high frequency resonant dc-dc converters. However output voltage is controlled by varying the switching frequency of the inverter. This type of output voltage control is not efficient in applications such as these ones considered in this thesis where input ac voltage and load are expected to vary widely.

Jeff Shortt et al. [16], investigated the use of a multi-stage phase-shifted-parallel dc-to-dc converter for reducing the size of the filter components. However this scheme increases significantly the component count and therefore is not of much practical interest.

Al Haddad et al. [43], investigated the resonant dc-dc converter using dual thyristors. In this converter high efficiency of operation is obtained due to the use of lossless snubbers. However this conversion scheme has the disadvantage of requiring wide frequency variation for output voltage regulation.

Manias et al. [9], proposed the bilateral dc-dc converter using single-phase high frequency link. In this conversion scheme the inverter is operated at high frequency using multi pulse PWM control methods. At low output power levels the proposed converter yields the desired results. However, as the output power level goes up the multi pulse PWM control method becomes less efficient.

The three-phase dc-dc converter was realized by several authors [12,13] using three single-phase dc-dc converters. This method not only increases the component count but it also increases the size of the overall unit.

There has been some previous work reported on the application of dc-dc converters for interfacing a dc source to a utility grid [6,8,47]. In particular Steigerwald et al. [8], investigated the application of high frequency links for interfacing a dc source to a utility grid. Moreover, Rajagopalan et al. [47], investigated the application of dual series resonant converter for utility interface. Also Savary et al. [6], investigated the application of dc-dc converters in photovoltaic array power conditioners. Finally Bhat and Dewan [27] investigated the application of dc-to-dc converter in utility interfaced high-frequency link photovoltaic power conditioning system.

1.3 Scope of the Thesis

The previously reviewed ac-to-dc HFL converter topologies can be classified into rectifier and high frequency inverter sections. The input current waveform distortion because of the associated inverter stage operation can be eliminated by proper design of the rectifier output filter inductor and capacitor values. Regarding the front end rectifier stage the disadvantages of existing topologies could be summarized as follows:

(i) Low efficiency because of large rms value of input current.

(ii) Low input power factor and contain low order harmonics of considerable amplitude.

(iii) Input ac mains voltage distortion because of the associated higher peak currents.

(iv) Interference with other loads.

(v) Converters are bulky and heavy.

(vi) Switching frequency is load dependent in active power factor correction method.

(vii) requires means of sensing and processing the input ac voltage for high input power factor.

However, the power semiconductor industry has been making available more efficient, easier to control and faster switching devices. The objective is to use these new devices to design cheaper, more compact, and more efficient HFL converters which require only few and small passive components. However, because of the aforementioned disadvantages existing ac-to-dc HFL converter topologies cannot be used to achieve these objectives.

The main objective in this thesis is to provide practical and viable solutions to the above mentioned problems including the design of more efficient and reliable ac-to-dc HFL converters capable of maintaining high quality input current and output voltage waveforms.

Moreover, the contributions of this thesis include the analysis and design of single-phase and three-phase fed ac-to-dc HFL converters which maintain high quality input ac current and output dc voltage waveforms while providing the necessary isolation for medium power levels. Different modes of operation of these converters are discussed in detail and design expressions are derived. Finally this thesis also presents for the first time the advantages of introducing three-phase inverters and three-phase transformers in HFL converters to achieve light weight and compact power supplies.

The contents of this thesis have been organized in five chapters as follows.

In Chapter 2, single-phase fed HFL converters with passive input current waveshaping methods have been investigated extensively. Relevant input current and output current waveforms, component ratings, and power factor values have been derived. Different modes of operation are discussed as a means of obtaining high performance. It has been shown that application of the proposed passive input filter topology reduces the size of the reactive components considerably. Finally, predicted results have been verified experimentally on laboratory prototype units.

In Chapter 3, single-phase and three-phase fed HFL converter active input current waveshaping methods have been investigated. It has been shown that application of PWM control method to three-phase diode rectifiers can reduce the size of the SMR converter considerably. Relevant input current and output current waveforms, component ratings, and power factor values have been derived. These methods are next used to control the output voltage of the HFL converters. The different modes of operation of three-phase fed boost active filter topology are analyzed in detail. It has been shown that three-phase and single-phase boost active filter topologies can improve the performance of the converter substantially. Also the proposed synchronous active filter topology controls the output voltage from zero to rated load while maintaining the high input power factor. A laboratory prototype has been built and tested to verify the analytically predicted results.

In Chapter 4, single-phase and three-phase HFL characteristics have been investigated extensively. The commutation of single-phase and three-phase inverters are discussed in detail. The methods of output voltage control in conjunction with the single-phase and three-phase passive and active filter topologies discussed in Chapters 2 and 3 have been presented. The different

modes of operation of three-phase inverter circuits are analyzed in detail. It has been shown that three-phase inverters and three-phase transformers can improve the performance of the converter considerably. It has been shown that converter size can be reduced substantially by eliminating the dc link reactive components. Finally, predicted analytical results have been verified experimentally.

Chapter 5 reviews the entire work presented in this thesis and presents relevant conclusions. It also focuses on future research in the area of SMR converters.

CHAPTER 2

Passive Input Current Waveshaping Section

2.1 Introduction

Traditionally, conversion of ac line voltages (from utilities or generators) to dc voltages has been done by using a diode rectifier and a large dc capacitor connected to the rectifier output as shown in Fig. 2.1. Such a conversion approach has the disadvantage of generating pulsed ac line currents drawn from the ac distribution network. As discussed in Chapter 1 the non-ideal character of these input currents creates a number of problems for the power distribution network and for other electrical systems in the vicinity of the rectifier. Shaping of the input current waveforms can be also obtained by using passive reactive components while the output voltage is controlled by a post regulator (dc-to-dc converter). The resulting advantages include more reliability and high input power factor. The object of this chapter is to propose and analyze a novel passive waveshaping method for single-phase fed ac-to-dc front-end rectifier which yield high quality input current waveforms, eliminates all the disadvantages discussed in Chapter 1 and exhibits high input power factor values. The passive input current (I_i) shaping methods generally need more stored energy and hence larger reactive components than active methods.

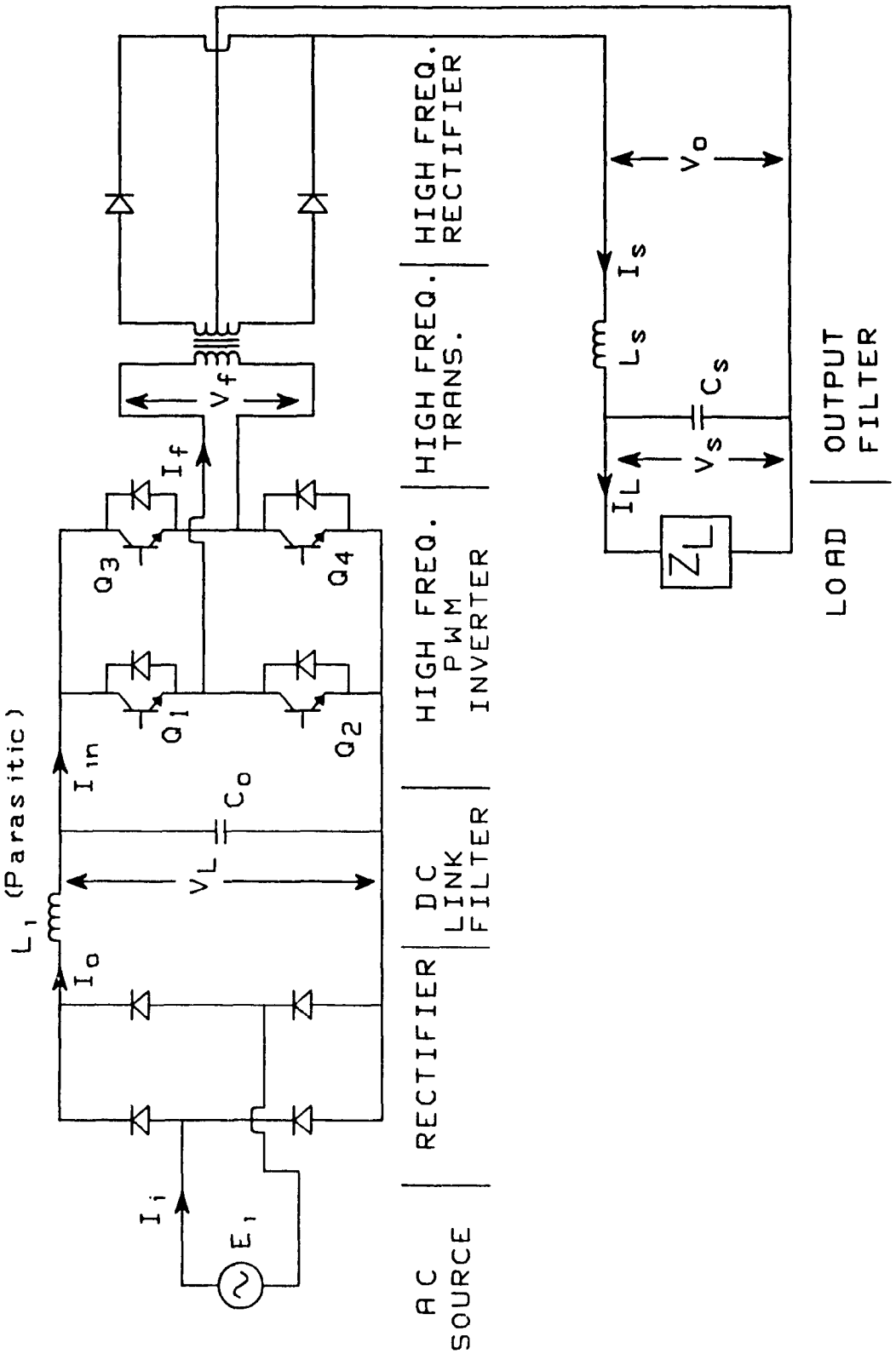


Fig. 2.1: Conventional SMR converter

2.1.1 Passive Waveshaping Methods

Power supply systems for low to medium power applications use a front-end single-phase diode rectifier which feeds the respective dc bus capacitors through a very low inductance path (Fig. 2.1). This approach has many disadvantages, including:

(i) high input current harmonic components;

(ii) low rectifier efficiency because of large rms values of the input current;

(iii) input ac mains voltage distortion because of the associated higher peak currents;

(iv) maximum input power factor of approximately 0.50 while a larger filter inductor is required for a high input power factor.

In the past system designers have used three passive waveshaping methods to improve the input power factor of a conventional ac-to-dc SMR converter (Fig. 2.1):

(i) input passive filter method;

(ii) resonant passive input filter method;

(iii) ferro resonant transformer method.

All these methods have the advantage of being easy to understand, easy to implement and service, and typically more reliable than active power factor correction methods. A simple way to improve the input current waveform of a conventional diode bridge rectifier (Fig. 2.1) is to place an inductor in series with its output (Fig. 2.2). This method is easy to understand and relatively cheap. The analysis and the design of the diode bridge rectifier with an LC

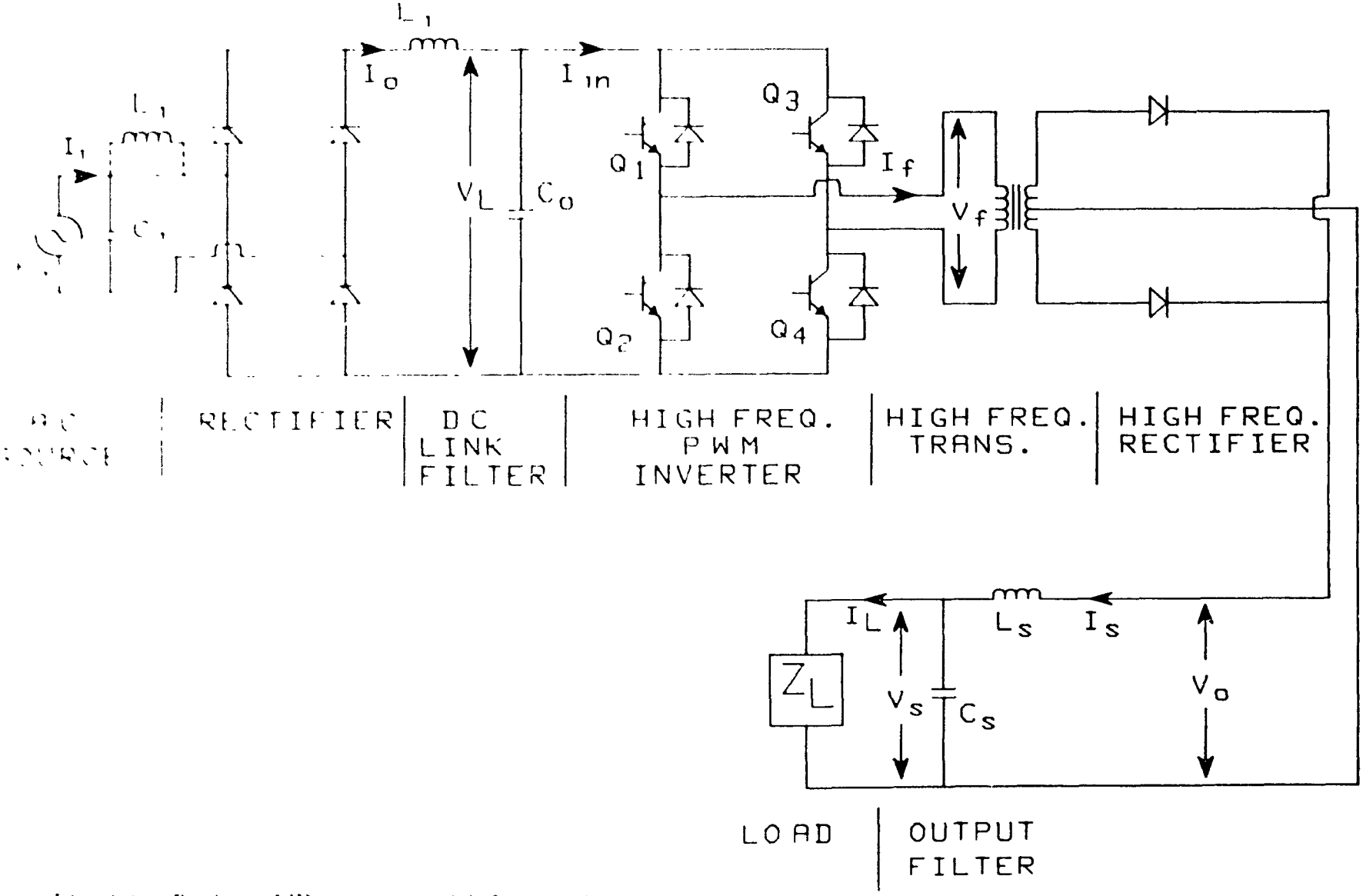


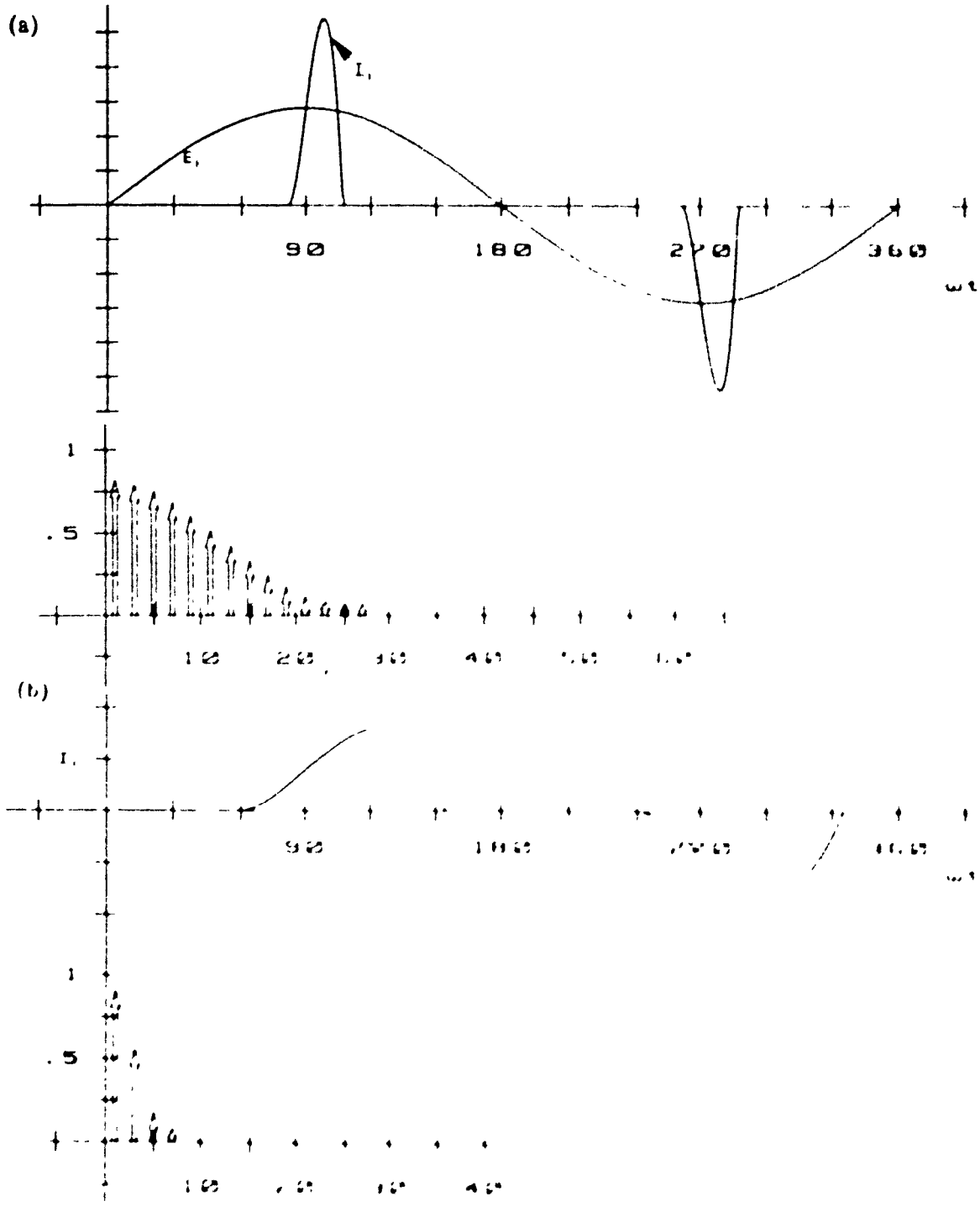
Fig. 2.2 [illegible] full-wave rectifier front-end passive filter topology

filter (Fig. 2.2) have already been discussed in literature [1,3]. This topology is clearly superior to the conventional diode bridge rectifier (Fig. 2.1). For low values of filter inductance (L_f) the diode bridge rectifier system operates in the discontinuous input current (I_i) mode and the input current (I_i) goes to zero before $\omega t = \pi$. For sufficiently low values of L_f, the input current becomes a narrow spike nearly centered in the voltage half-sine wave as shown in Fig. 2.3. The Fourier analysis of such an input current (I_i) waveform clearly shows the presence of a third harmonic component of considerable amplitude which is the main cause for low input power factor. Consequently, some form of filtering is necessary to remove the third harmonic component from the input current (I_i) and to improve the input power factor. In other words a larger filter inductor is required to improve the input power factor. However, a larger filter inductor (L_f) has a negative impact on the associated post regulator control strategy because of increased dc source voltage regulation. Improving the input power factor by connecting a capacitor (C_f) at the input terminals has some disadvantages including:

(i) low efficiency because of large rms values of the rectifier input current;

(ii) input ac mains voltage distortion because of the associated rectifier high peak currents.

The second disadvantage is particularly important for office or residential applications. A series resonant filter (Fig. 2.4) is an alternate way to passively shape the input current (I_i). When the quality factor and characteristic impedance of the series resonant circuit are both high enough, only currents at the 'notch' frequency can get through to the line and the power factor will be near unity. The major disadvantages of the resonant input filter are the


(a)
I_1
E_1
90
180
270
360
ωt
1
.5
(b)
I_1
1
.5

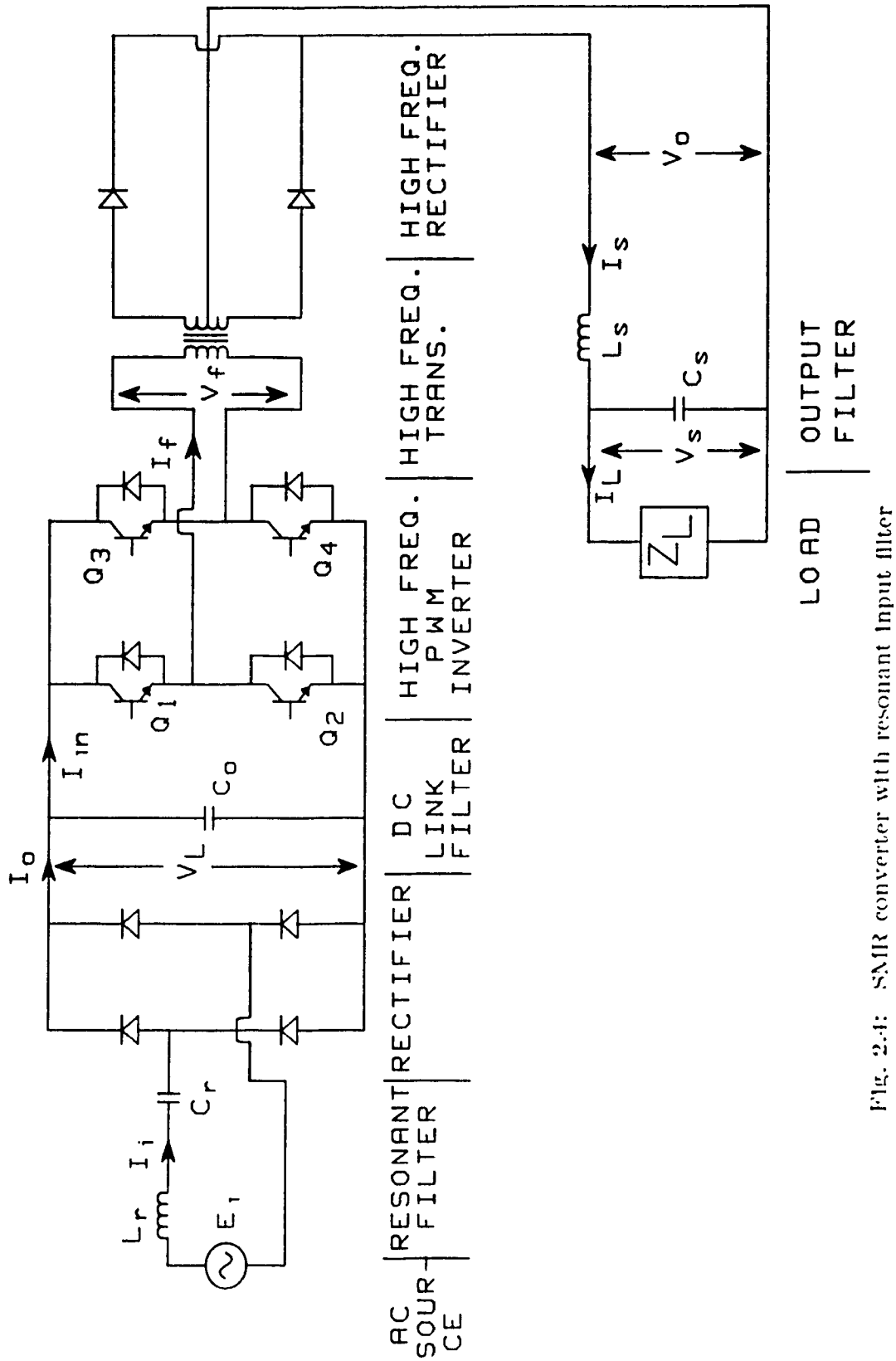


Fig. 2.4: SMR converter with resonant input filter

large size of the reactive elements and the large rms currents in the capacitors C_o and C_r. The resonant input filter is similar in some ways to the ferro resonant transformer. Like the resonant input filter the ferro resonant transformer is heavy and is considered mainly for its ruggedness. The proposed passive power factor correction method (Fig. 2.5) eliminates all the above disadvantages and improves the input power factor while reducing the size of the passive reactive components. However the proposed passive input current waveshaping method (Fig. 2.5) also has the disadvantage of increased complexity of the operation.

2.2 Typical Front-end Passive Filter Topology

The principles of operation of the diode rectifier with input passive filter method (standard diode bridge rectifier Fig. 2.2) are presented in several references [1-3]. Based upon the instant at which the steady state rectifier output current (I_o) goes to zero, the rectifier system shown in Fig. 2.2 has three possible modes of operation.

(I) Discontinuous mode I : The bridge rectifier operates in the discontinuous mode I if the steady state output current (I is discontinuous and goes to zero before t =

(II) Discontinuous mode II : The bridge rectifier operates in the discontinuous mode II if the steady state output current (I is continuous and goes to zero after t =

(III) Continuous mode III : The bridge rectifier operates in the continuous mode if the steady state output current (I never goes to zero

However the [illegible] operate in the [illegible]

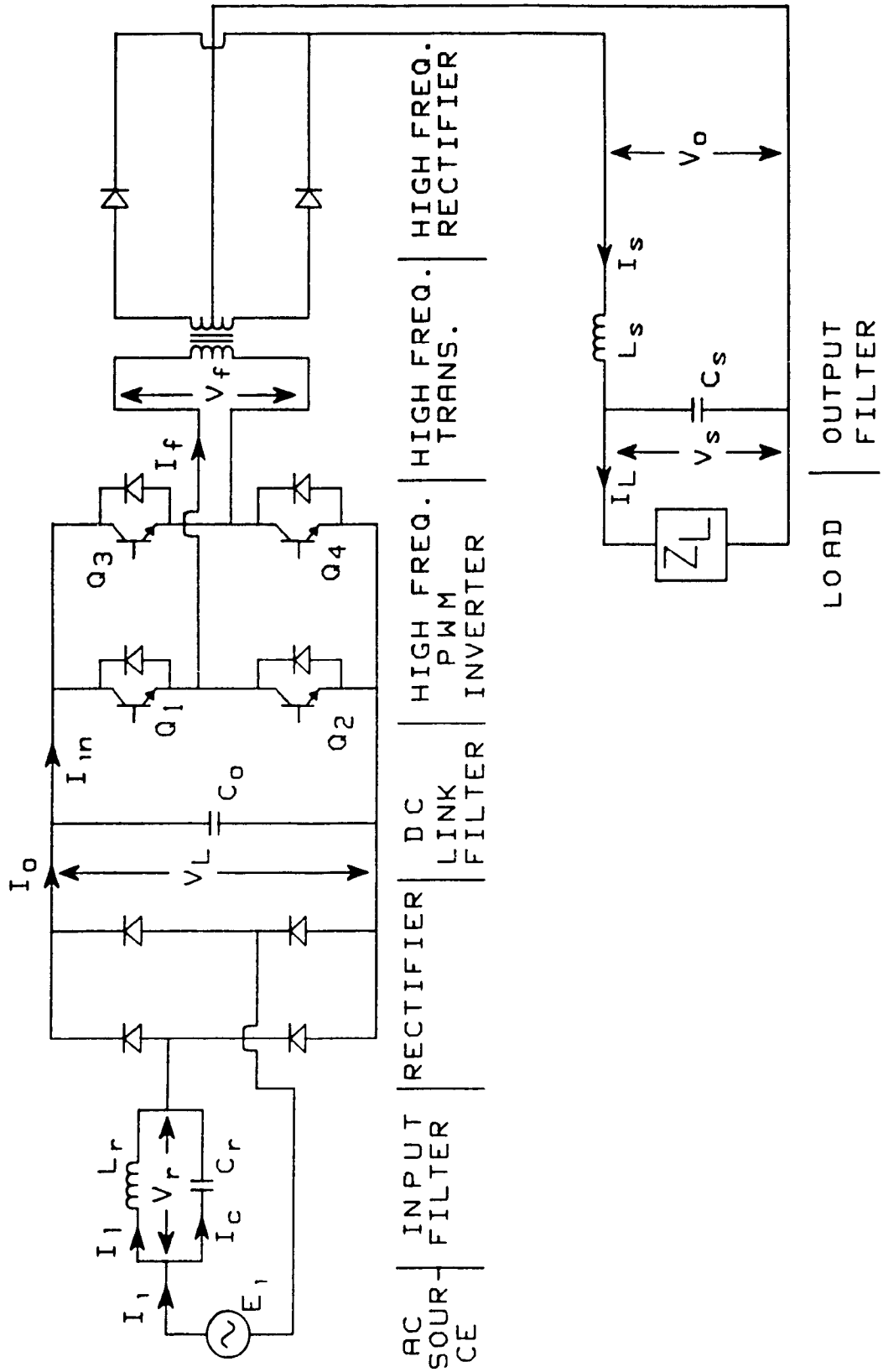


Fig. 2.3: SMR converter with proposed front-end passive filter topology

the relevant expressions are presented here. The angle, α_L at which the diodes start conduction is given by $\sin^{-1}\left[\frac{V_L}{\sqrt{2}E}\right]$. The input current I_i in discontinuous mode-I during the period $\alpha_L \leq \omega t \leq \beta_L$ is given by

$$I_i(\omega t) = \frac{\sqrt{2}E}{\omega L_i}\left[\cos(\alpha_L) - \cos(\omega t) - m(\omega t - \alpha_L)\right] \qquad (2.1)$$

where β_L is the angle at which the input current I_i becomes zero and $m = \frac{V_L}{\sqrt{2}E}$. The performance of the diode bridge rectifier is discussed in the next section.

2.2.1 Front-end Rectifier

The analysis of a single-phase fed converter system shown in Fig. 2.2.1 is based upon the following assumptions.

(i) The filter capacitance (C_o) is assumed to be sufficiently large so that the output voltage (V_L) is ripple free constant dc voltage.

(ii) The ac source E_i is considered ideal.

(iii) The losses in inductor (L_i), capacitor (C_o) and the bridge rectifier are neglected.

(iv) The load is modeled as a variable resistance since the effect of high frequency ripple is negligible as per assumption (i).

Moreover, the rated rms ac input voltage (E_i) and rated rectifier output power (P_o) are assumed to be

E_i = 110 volts

P_o = 100 watts

In Fig. 2.2 the diode rectifier can operate either in the continuous or discontinuous conduction mode. However a large filter inductor (L_i) is required in continuous conduction mode to yield a high input power factor. The input power factor of the diode rectifier is calculated from the following expression.

$$Power\ Factor = \frac{\frac{I_{i,1}}{\sqrt{2}}}{\sqrt{\sum_{n=1}^{\infty}\left(\frac{I_{i,n}}{\sqrt{2}}\right)^2}}\cos(\phi_1) \qquad (2.2)$$

Using Eqn. (2.2) the variation of the input power factor in discontinuous modes-I and II with load voltage (V_L) is shown in Fig. 2.6. Evidently, the maximum input power factor in the discontinuous mode-I is 0.763. The output power (P_r) of the bridge rectifier is given by

$$P_r = V_L * I_{o,o} \qquad (2.3)$$

where $I_{o,o}$ is the average rectifier output current. Using Eqn. (2.3), the variation of the output power (P_r) is shown (Fig. 2.7) as a function of voltage V_L for different values of L_i. From Figs. 2.6 and 2.7 the value of L_i at maximum input power factor to deliver 1.0 pu P_r is found to be 0.1 pu.

2.2.2 Rectifier Output Filter

At maximum input power factor the value of the inductor (L_i) to deliver 1.0 pu output power is 0.1 pu. The amplitude of the second order voltage harmonic component across the rectifier output filter capacitor (C_o) is given by

$$V_{L,2} = \frac{I_{o,2}}{2\omega C_o} \qquad (2.4)$$

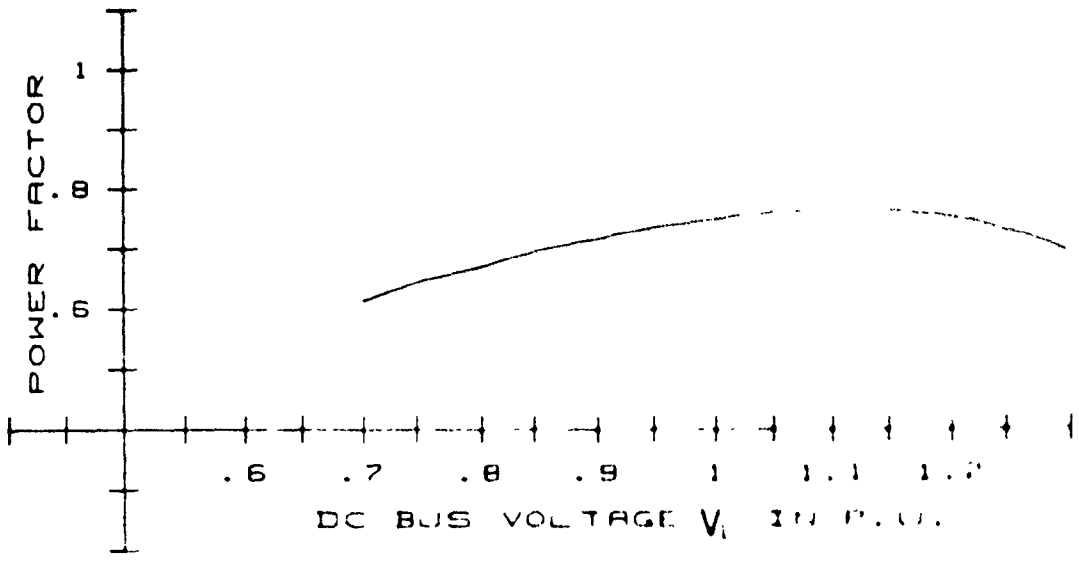


Fig. 2.6: Variation of input power factor with dc bus voltage (V_i)

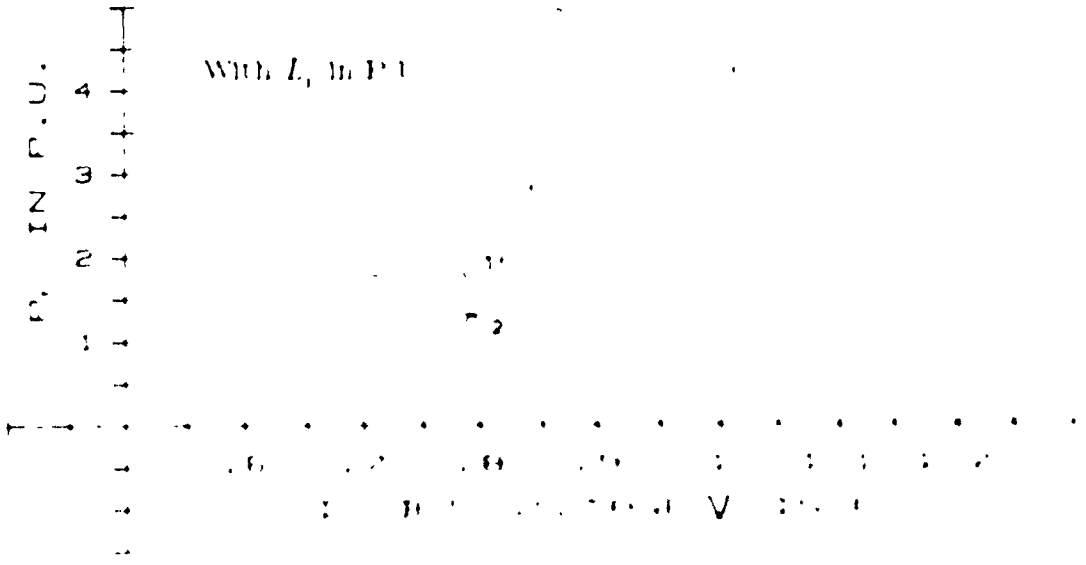


Fig. 2.7 Variation of [illegible] with dc bus voltage V_i [illegible]

Moreover the allowable inverter input voltage ripple can be defined by

$$Ripple\ \% = \frac{100 * V_{L,2(rms)}}{V_{L,o}}$$

Substituting the above equation in Eqn. (2.4) the value of this capacitor is

$$C_o = \frac{100 * I_{o,2}}{\sqrt{2} * V_{L,o} * 2 * \omega * (Ripple\ \%)} \tag{2.5}$$

2.2.3 Component Ratings

From the aforementioned assumptions and derived analytical expressions the voltage and current rating values of the various system components at maximum input power factor ($V_L = 1.1pu$) when L_i has a value of 0.1 are as follows. The average current ($I_{d,0}$) through the rectifier diode under this condition is given by

$$I_{d,0} = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_i(\omega t)\, d\omega t = 0.4581 \quad pu \tag{2.6}$$

The rms current ($I_{d,rms}$) through the diode is given by

$$I_{d,rms} = \frac{I_{i,rms}}{\sqrt{2}}$$

$$I_{d,rms} = \frac{1}{\sqrt{2}}\left[\sqrt{\sum_{n=1}^{\infty}\left(\frac{I_{i,n}}{\sqrt{2}}\right)^2}\right] = 0.9508 \quad pu \tag{2.7}$$

The peak current ($I_{d,peak}$) through the diode is given by

$$I_{d,peak} = \sqrt{\left[\sum_{n=1}^{\infty}(I_{i,n})^2\right]} = 1.901 \quad pu \tag{2.8}$$

where the peak forward voltage of the diode is 1.414 pu and

the reverse blocking voltage of the diode is 1.414 pu

The rms value of the current through L_1 is 1.345 pu and the peak value of the current through L_f is 1.901 pu. Moreover because of the discontinuous current mode of operation of the rectifier the filter inductor can be placed on the input ac side as shown in Fig. 2.2 (dotted lines). Therefore the volt-ampere (VA) ratings of the reactive components are defined as follows: The ac inductor rating is

$$LVA = \sum_{n=1}^{51} \left[\frac{I_{1\,n}}{\sqrt{2}} \right]^2 nX_{L_1} \tag{2.9}$$

The capacitor rating is

$$CVA = \sum_{n=1}^{51} \left[\frac{I_{0\,n}}{\sqrt{2}} \right]^2 \left[\frac{X_{C_f}}{n} \right] \tag{2.10}$$

and the total VA (TVA) is

$$TVA = LVA + CVA \tag{2.11}$$

The VA rating of the filter inductor (L_1) and the value of the output filter capacitor (assuming 5-percent ripple) are calculated using Eqns (2.9) and (2.5). The variation of total VA (TVA) of the reactive components with output power is shown in Fig. 2.8 for different values of I_{1}. From Fig 2.8 the minimum value of TVA to deliver 1.0 pu output power (I_{1} = 3.8 pu

2.2.4 Design Example

To illustrate the significance and validity of the theoretical results obtained in the previous section the following design example is presented. The SMR converter has the following specifications

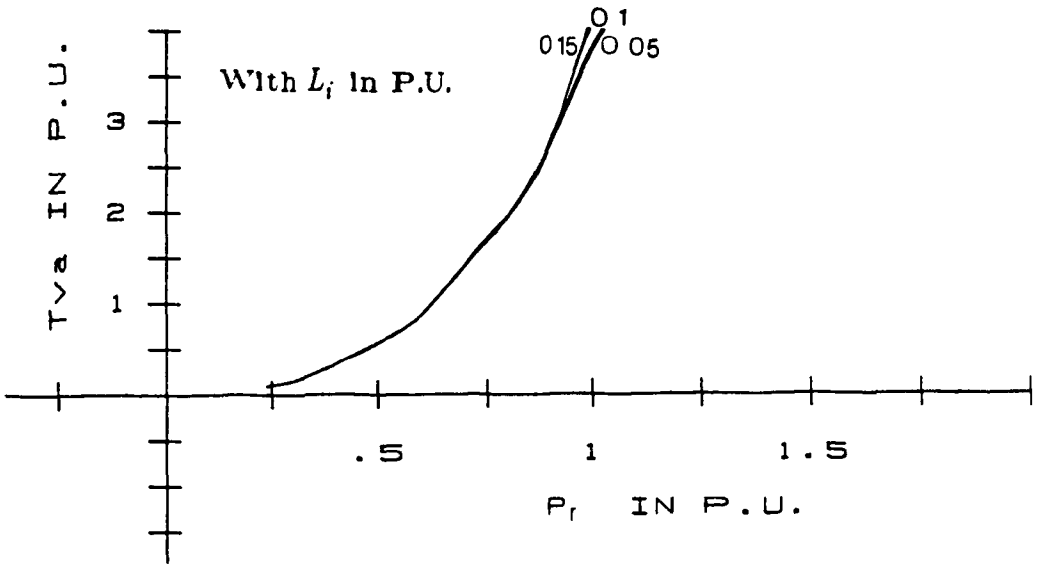


Fig. 2.8: Variation of Tva with output power (P_r) for different values of L_i

V_{in} = 208 rms ≡ 1 pu Volts.

P_r = 5,000 W ≡ 1 pu Watts.

Output voltage (V_L) ripple = 5%

From these values

$$1 \text{ pu Current} = \frac{5{,}000}{208} = 24.04 \text{ Amps.}$$

$$1 \text{ pu Impedance} = \frac{208}{24.04} = 8.65 \text{ Ohms}$$

$$1 \text{ pu Inductance} = \frac{8.65}{377} = 23 \text{ mH}$$

$$1 \text{ pu Capacitance} = \frac{1}{8.65 * 377} = 306.65 \ \mu\text{F}$$

$$1 \text{ pu Angular frequency} = 2\pi f = 377 \text{ rad./s}$$

From Figs. 2.6 and 2.7 the value of the inductor, L_1 to deliver 1.0 pu output power is 0.1 pu which is equal to 2.3 mH. Using the pu values shown in section 2.2.3 the voltage and current ratings of the rectifier diode and filter capacitor C_o are as follows:

Rectifier Diode

Average current, $I_{d\ o}$: 0.4581 * 24.04 = 11.01 Amps.

RMS current, $I_{d\ rms}$: 0.95 * 24.04 = 22.84 Amps.

Peak current, $I_{d\ peak}$: 1.901 * 24.04 = 45.7 Amps.

Peak forward voltage : $\sqrt{2}$ * 208 = 294.15 Volts

DC Filter Inductor L_1

Value of the Inductor : 0.1 * 23 = 2.3 mH

RMS current : 1.345 * 24.04 = 32.34 Amps

Peak current : 1.902 * 24.04 = 45.73 Amps

DC Filter Capacitor C_o

Peak voltage : 1.12 * 208 = 232.96 Volts.

120 Hz ripple current, $I_{o,2}$: 1.317 * 24.04 = 31.6 Amps.

Value : 8.31 * 306.65 = 2549.48 μF

2.2.5 Experimental Results

To verify the predicted results a 600 watt experimental SMR has been implemented with the following circuit parameters:

- AC input rms voltage ($E_{i(rms)}$) = 100 Volts.
- Angular frequency of the ac source = 377 rad./sec.
- Filter inductor (L_t) = 8 mH.

Experimental waveforms of the typical front-end passive filter topology are shown in Fig. 2.9. The input power factor is as follows:

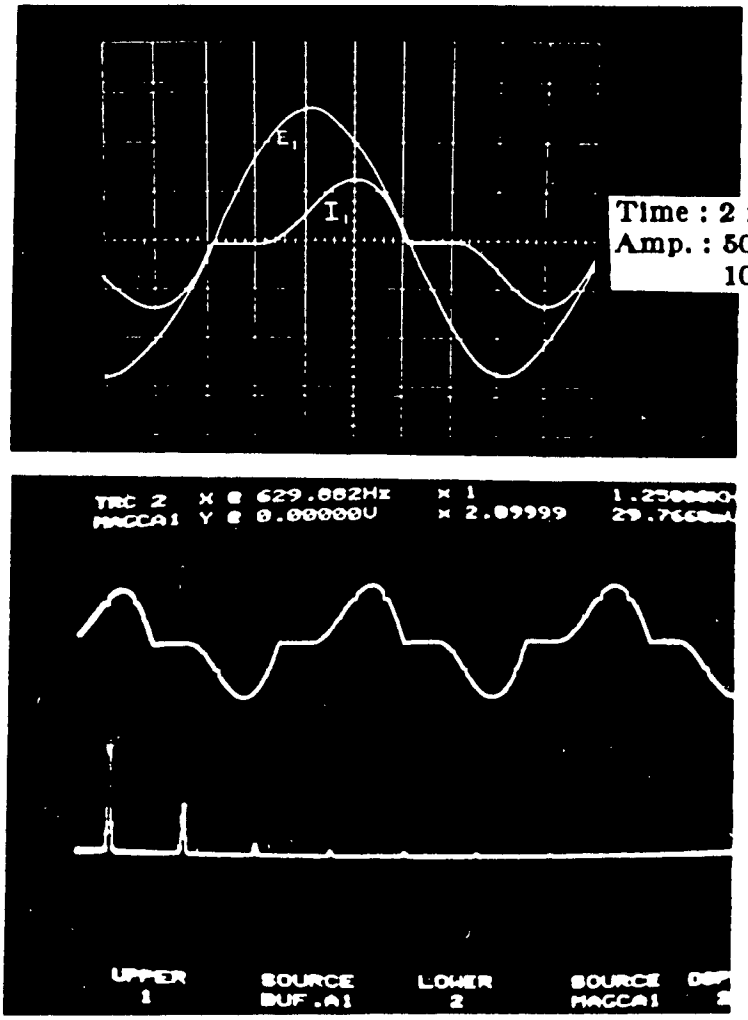
- AC input rms current ($I_{i(rms)}$) = 8.0 Amps.
- Load dc voltage (V_L) = 100 Volts.
- Load dc current (I_{in}) = 6 Amps.

Using the above information the input power factor is given by

$$Power\ Factor = \frac{100 * 6}{100 * 8.0} = 0.75 \qquad (2.12)$$

which is in good agreement with the simulated results shown in Fig. 2.6.

(a)



(b)

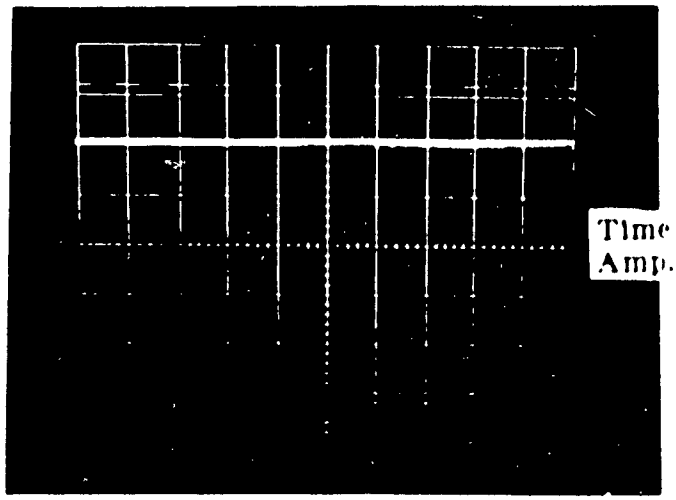


Fig. 2.9: Typical front-end passive filter topology experimental waveforms:
(a) Input ac source voltage, input current (I_1) and its spectrum.
(b) DC bus voltage (V_l)

2.2.6 Conclusions

This section has presented the analysis of the front-end input passive filter topology in discontinuous mode of operation. Performance evaluation and related design data were provided for implementation and comparison of the input passive filter topology. Finally, key predicted results were verified experimentally.

2.3 Proposed Front-end Passive Filter Topology

For low values of line inductance L_i the input current of a standard diode rectifier has a third harmonic component (Fig. 2.3) of considerable amplitude which is the main cause for low input power factor. Consequently the proposed passive input filter topology (shown in Fig. 2.5) consists of an input L-C parallel resonant tank whose inductor and capacitor values are selected so that the input filter presents an infinite (theoretically) impedance to the third harmonic input current component. The resulting advantages over the existing passive filter topologies include:

(i) lower value of input peak current and hence no input voltage distortion;

(ii) high input power factor;

(iii) high efficiency because of the low rms values of the input current;

(iv) reduced reactive component sizes.

2.3.1 Input Filter

The n^{th} harmonic component of the equivalent impedance of the input parallel resonant filter is given by

$$Z_n = \frac{nX_{L_r} * \frac{X_{C_r}}{n}}{jnX_{L_r} - j\frac{X_{C_r}}{n}} \tag{2.13}$$

where

X_{L_r} is the impedance of the input resonant inductor (L_r) at fundamental frequency.

X_{C_r} is the impedance of the input resonant capacitor (C_r) at fundamental frequency.

From Eqn. (2.13) the third harmonic impedance of the input resonant filter becomes infinity (theoretically) when

$$3X_{L_r} = \frac{X_{C_r}}{3}$$

or

$$L_r = \frac{1}{9\omega^2 C_r} \tag{2.14}$$

where ω is the angular frequency of the input ac source (V_s). Based upon the instant at which the steady state rectifier output current (I_o) goes to zero, the rectifier system shown in Fig. 2.5 has three possible modes of operation:

(I) Discontinuous mode I : The bridge rectifier operates in the discontinuous mode I if the steady state output current (I_o) is discontinuous and goes to zero before $t =$

(II) Discontinuous mode II : The bridge rectifier goes to the discontinuous

tinuous mode II if the steady state output current (I_o) is discontinuous and goes to zero at $\pi < \omega t < \pi + \alpha$.

(iii) Continuous mode III : The bridge rectifier operates in the continuous mode if the steady state output current (I_o) never falls to zero.

In Fig. 2.5 the angle (α) at which the diodes start conduction depends upon the voltage, V_L, and the resonant capacitor voltage, V_r. The steady state capacitor voltage V_r can be obtained by considering the initial voltage, V_r, across the resonating capacitor is zero volts and the initial current, I_l, through the inductor is zero amperes. During the first positive half cycle of the input voltage (E_i) wave the angle (α) at which the conduction starts is given by $\sin^{-1}(\frac{V_L}{\sqrt{2}E})$. Where E is the rms value of the input ac voltage (E_i). The conduction period (γ) of the rectifier system depends upon the value of the load voltage (V_L). Assuming that the input current (I_i) goes to zero at an angle β and $\pi < \beta < (\pi + \alpha)$, then the conduction period is $\gamma = \beta - \alpha$. During the period from α to β the current (I_l) through the inductor and the current (I_c) through the capacitor are given by

$$I_l(\omega t) = \frac{\sqrt{2}E}{\omega L_r}\left[\cos(\alpha) - \cos(\omega t) - m(\omega t - \alpha)\right] \qquad (2.15)$$

$$\text{where m} = \frac{V_L}{\sqrt{2}E}$$

and

$$I_c(\omega t) = \sqrt{2}E * \omega C_r * \cos(\omega t) \qquad (2.16)$$

The voltage across the capacitor (C_r) at the end of the conduction period 3 is given by

$$V_r(\beta) = \frac{1}{C_r}\int_{\alpha}^{\beta} I_c(\omega t)\,dt$$

$$= \sqrt{2}E\left[\sin(\beta) - \sin(\alpha)\right] \tag{2.17}$$

At an angle β the input current I_i goes to zero and the conducting diodes during the positive half cycle of the bridge rectifier system are turned off. During the negative half cycle of the input voltage E_i, the angle (α_1) at which the other two diodes start conduction depends upon the value of the capacitor voltage (V_r). From β to α_1 the capacitor (C_r) starts resonating with the inductor (L_r) and changes its polarity. During the period $\beta \leq \omega t \leq \alpha_1$ the current through the capacitor is given by

$$I_c(\omega t) = A\cos(\omega_n(\omega t - \beta)) + B\sin(\omega_n(\omega t - \beta)) \tag{2.18}$$

where $\omega_n = \dfrac{1}{\sqrt{L_r C_r}}$, $I_c(\beta) = 0$, and $V_r(\beta)$ is given by Eqn (2.17). Substituting these initial conditions in Eqn (2.18) yields

$$I_c(\omega t) = \omega_n C_r \sqrt{2} I \left[\sin(\beta) - \sin(\alpha)\right] \sin(\omega_n(\omega t - \beta)) \tag{2.19}$$

$$I_c(\omega t) \qquad I(\omega t)$$

and

$$V_r(\omega t) = \sqrt{2} L \left[\sin(\beta - \sin(\alpha)\right] \cos(\omega_n(\omega t - \beta)) \tag{2.20}$$

The voltage V_r across the capacitor changes at a frequency determined by the inductor (L_r) and capacitor (C_r). The frequency is at three times the input ac source frequency. The angle α_1 at which the [illegible] the negative half cycle is the angle α_1 at which

$$\sqrt{2} I \omega_n L \left[\sin(\beta) - \sin(\alpha_1)\right] = V_r \tag{2.21}$$

This transcendental equation [illegible] may be [illegible] the angle α_1 [illegible] the angle α_1 [illegible]

current $I_l(\alpha_1)$ through the inductor is $-I_c(\alpha_1)$. The conduction period (γ_1) during the negative half cycle is given by $\gamma_1 = \beta_1 - \alpha_1$ and the current I_l and current I_c during this period are given by

$$I_l(\omega t) = \frac{\sqrt{2}E}{\omega L_r}\left[\cos(\alpha_1) - \cos(\omega t) + m(\omega t - \alpha_1)\right] + i_l(\alpha_1) \qquad (2.22)$$

and

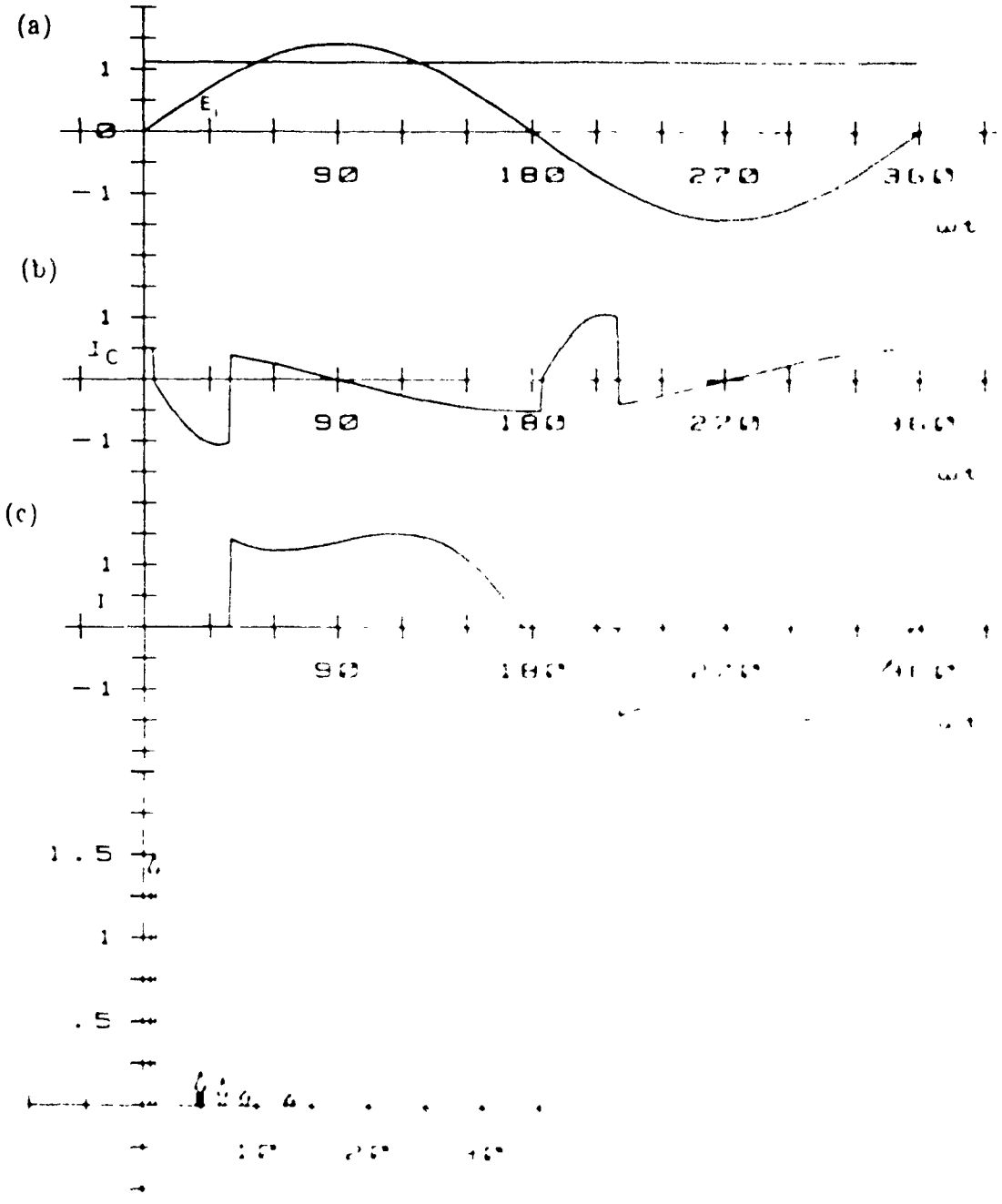
$$I_c(\omega t) = \sqrt{2}E\,\omega C_r \cos(\omega t) + V_r(\alpha_1) \qquad (2.23)$$

The voltage (V_r) across the capacitor at the end of the negative half cycle conduction period (β_1) is given by

$$V_r(\beta_1) = V_r(\alpha_1) + \sqrt{2}E\left[\sin(\beta_1) - \sin(\alpha_1)\right] \qquad (2.24)$$

At the end of the conduction period (γ_1) the capacitor (C_r) starts resonating with the inductor (L_r). Now the initial conditions are set for the second positive half cycle. During the subsequent cycles the above operation repeats during the positive and negative half cycles. After a few cycles of operation steady state is reached. The steady state input current (I_i), inductor current (I_l), capacitor current (I_c), and the voltage across the capacitor (V_r) are shown in Fig. 2.10.

For lower values of the load voltage (V_L) the conduction period (γ) increases. Assuming that the conduction during the positive half cycle ends at $180 + \alpha$. To start conduction in the negative half cycle the capacitor voltage (V_r) has to fall to a value at which the negative half cycle diodes will be forward biased. In contrast, in the case of input passive filter method, conduction in the negative half cycle starts at $180 + \alpha$. From the description presented above it is clear that the proposed diode bridge rectifier will not operate in the continuous current mode and will always operate in discontinu-


(a)
1
0
−1
E_1
90
180
270
360
ωt
(b)
1
I_C
−1
90
180
ωt
(c)
1
I
−1
1.5
1
.5

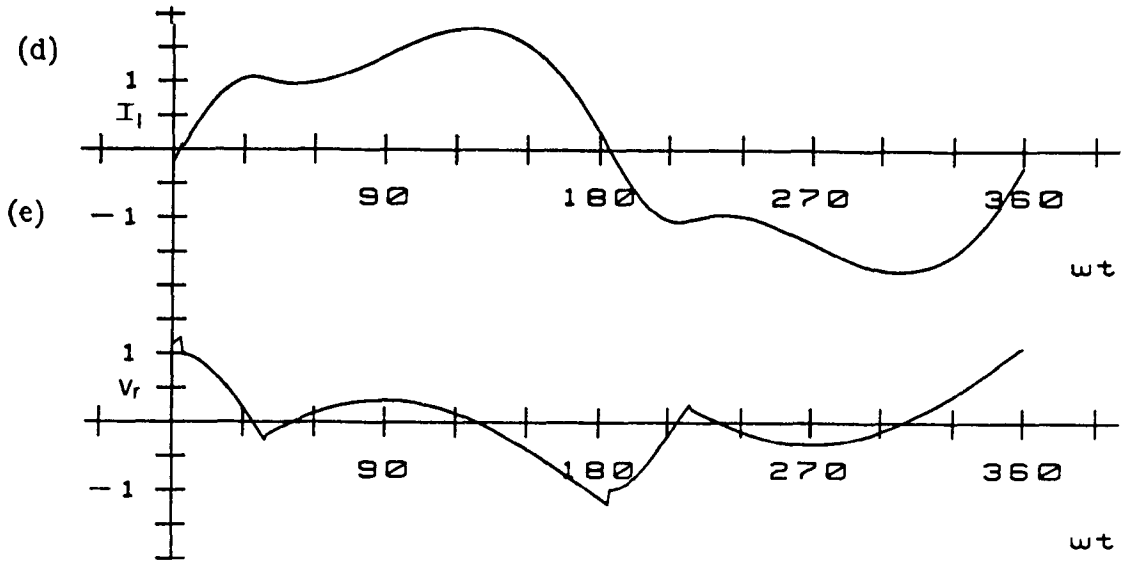


Fig. 2.10: Proposed front-end passive filter topology simulated waveforms
(a) Input ac source voltage (E_s) and dc bus voltage (V_L).
(b) Resonant capacitor current (I_c).
(c) Input current (I_s) and its spectrum.
(d) Resonant inductor current (I_l).
(e) Resonant capacitor voltage (V_r).

ous current mode. As the load voltage (V_L) is increased the conduction period decreases and the angle (α) at which the conduction starts increases. For higher and higher values of the load voltage (V_l) the steady state output current goes to zero before $\omega t = \pi$. This operation continues during subsequent cycles and reaches a steady state value.

2.3.2 Front-end Rectifier

The analysis of the front-end of a single-phase fed converter system shown in Fig. 2.5 is based upon the following assumptions.

(i) The filter capacitance (C_o) is assumed to be sufficiently large so that the output voltage (V_l) is ripple free constant dc voltage.

(ii) The ac source E_i is considered ideal.

(iii) The losses in inductor (L_s), capacitor (C_s, C_o) and the bridge rectifier are neglected.

(iv) The load is modeled as a variable resistance since the effect of high frequency ripple is negligible as per assumption (i).

Moreover, the rated rms ac input voltage (E_i) at rated supply frequency (f) are assumed to be

$$E_i = 110 \text{ volts} \qquad (2.2)$$

$$f = 60 \text{ cps} \qquad (2.3)$$

From the description presented in the previous section, the operation of the proposed bridge rectifier system is governed by the [illegible] the steady state performance of the proposed rectifier system [illegible]

As described in section 2.3.1, the steady state condition has been reached after a few cycles of operation. The steady-state input current (I_i) and its spectrum, inductor current (I_l), and capacitor current (I_c) are shown in Fig. 2.10. The conduction period of the diodes varies with the load voltage (V_L). The input power factor of the diode rectifier is calculated from the following expression.

$$Power\ Factor = \frac{\frac{I_{i,1}}{\sqrt{2}}}{\sqrt{\sum_{n=1}^{\infty}\left(\frac{I_{i,n}}{\sqrt{2}}\right)^2}}\cos(\phi_1) \tag{2.26}$$

where $I_{i,n}$ is the n^{th} harmonic component of the input current I_i and ϕ_1 is the phase angle between the input fundamental ac voltage (E_i) and the fundamental component of the current (I_i).

The variation of the input power factor using Eqn. (2.26) with dc bus voltage (V_L) is shown in Fig. 2.11. Comparison of Figs. 2.6 and 2.11 show that the proposed front-end passive filter topology has a better input power factor than the standard diode bridge rectifier (Fig. 2.2). It is also observed that the proposed bridge rectifier exhibits a high input power factor when the conduction period of the diodes ceases at approximately 180^o. The output power (P_r) of the bridge rectifier is given by

$$P_r = V_L * I_{o,0} \tag{2.27}$$

where $I_{o,0}$ is the average rectifier output current. The variation of P_r with load voltage (V_L) is shown in Fig. 2.12 for various values of L_r. From Figs. 2.11 and 2.12 at maximum input power factor the value of L_r to deliver 1.0 pu output power (P_r) is 0.31 pu. Evaluation of Figs. 2.6, 2.7, 2.11 and 2.12 show the advantages of the proposed diode bridge rectifier (Fig. 2.5) over the

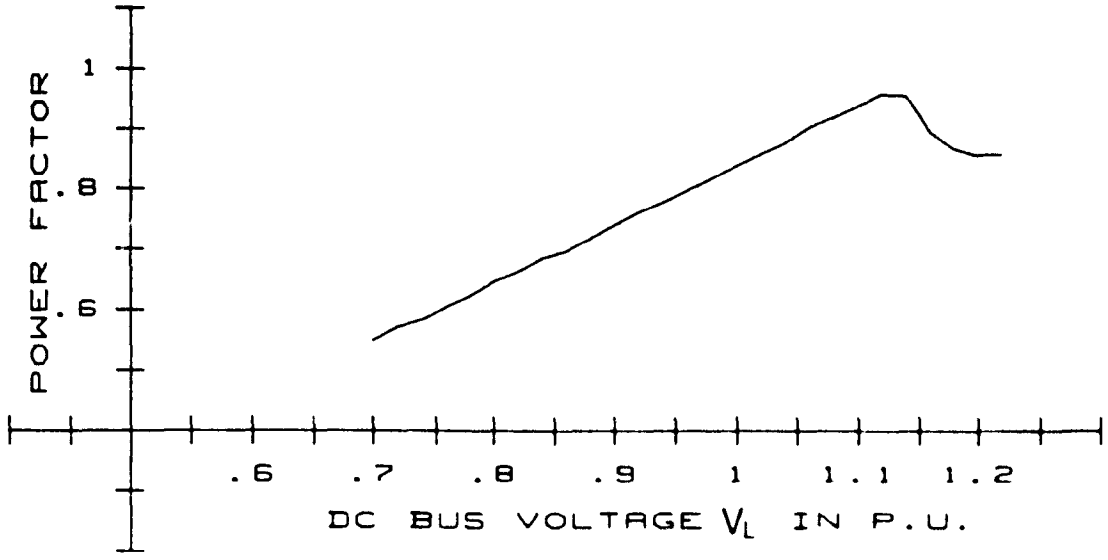


Fig. 2.11: Variation of input power factor with dc bus voltage (V_L)

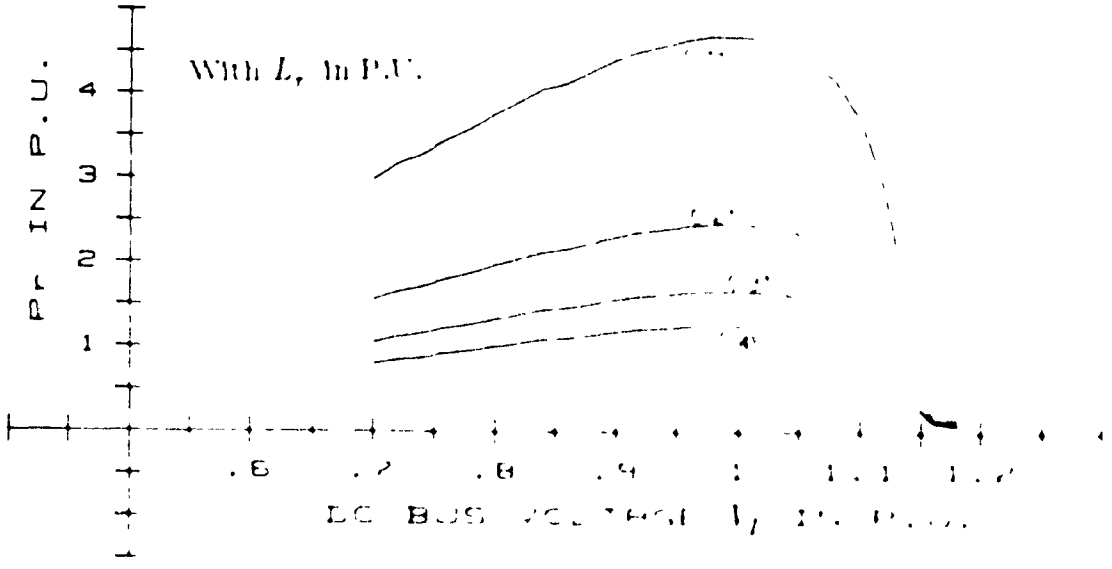


Fig. 2.12: Variation of [illegible] with dc bus voltage (V_L) for different values of L_r.

standard diode bridge rectifier (Fig. 2.2). In particular from Figs. 2.7 and 2.12 it is noted that the power delivered by the proposed front-end passive filter topology is higher than the standard rectifier for the same inductor value.

2.3.3 Rectifier Output Filter

The amplitude of the second order voltage harmonic component across the rectifier output filter capacitor (C_o) is given by

$$V_{L,2} = \frac{I_{o,2}}{2\omega C_o} \tag{2.28}$$

Moreover the allowable inverter input voltage ripple can be defined by

$$Ripple\ \% = \frac{100 * V_{L,2(rms)}}{V_{L,o}}$$

Substituting the above equation in Eqn. (2.28) the value of this capacitor is

$$C_o = \frac{100 * I_{o,2}}{\sqrt{2} * V_{L,o} * 2 * \omega * (Ripple\ \%)} \tag{2.29}$$

2.3.4 Component Ratings

From the aforementioned assumptions and derived analytical expressions the voltage and current ratings of the various components at maximum input power factor when L_r has a value of 0.31 pu are as follows. The average current ($I_{d,0}$) through the rectifier diode under this condition is given by

$$I_{d,0} = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_i(\omega t)\, d\omega t = 0.4573 \quad pu \tag{2.30}$$

The rms current ($I_{d,rms}$) through the diode is given by

$$I_{d,rms} = \frac{I_{i,rms}}{\sqrt{2}}$$

$$I_{d,rms} = \frac{1}{\sqrt{2}}\left[\sqrt{\sum_{n=1}^{\infty}\left(\frac{I_{i,n}}{\sqrt{2}}\right)^2}\right] = 0.7686 \quad pu \tag{2.31}$$

The peak current ($I_{d,peak}$) through the diode is given by

$$I_{d,peak} = \sqrt{\left[\sum_{n=1}^{\infty}(I_{i,n})^2\right]} = 1.537 \quad pu \tag{2.32}$$

where the peak forward voltage of the diode is 1.414 pu and

the reverse blocking voltage of the diode is 1.414 pu

From Figs. 2.11 and 2.12 at maximum input power factor the value of the inductor (L_r) to deliver 1.0 pu P_r is 0.31 pu. The rms current through L_r is 1.23 pu and the peak value of the current is 1.74 pu. Using Eqn. (2.14) the value of the capacitor (C_r) is 0.358 pu. The rms current through C_r is 0.43 pu and the peak value of the current is 0.608 pu. The volt-ampere (VA) ratings of the reactive components are defined as follows: The inductor rating is

$$LVA = \sum_{n=1}^{\infty}\left[\frac{I_{i,n}}{\sqrt{2}}\right]^2 \cdot nX_l \tag{2.33}$$

The capacitor rating is

$$CVA = \sum_{n=1}^{\infty}\left[\frac{I_{z,n}}{\sqrt{2}}\right]^2\left[\frac{X_c}{n}\right] \tag{2.34}$$

where $I_{z,n}$ is the amplitude of the n^{th} harmonic component of capacitor current I_z and the total VA is

$$TVA = LVA + CVA \tag{2.35}$$

The variation of TVA of the resonant components of the inverter

ogy (L_r, C_r, and C_o) is shown in Fig. 2.13 for different values of L_r. Using Eqns. (2.13) and (2.29) the values of C_r and C_o (assuming 5-percent ripple voltage) are calculated. Fig. 2.13 shows that the TVA value of the proposed passive topology is minimum when L_r has a value of 0.31 pu at 1.0 pu rectifier output power. Evaluation of Figs. 2.8 and 2.13 show that the proposed passive diode bridge rectifier (Fig. 2.5) requires a smaller (VA) total reactive VA to deliver 1.0 pu power. Furthermore, the currents through the rectifier diodes found in Eqns. (2.6) to (2.8) are higher than the respective values found in Eqns. (2.30) to (2.32) for the proposed rectifier (Fig. 2.5). Comparative component ratings in pu of the proposed passive waveshaping method, the standard diode bridge rectifier are summarized in Table 2.1.

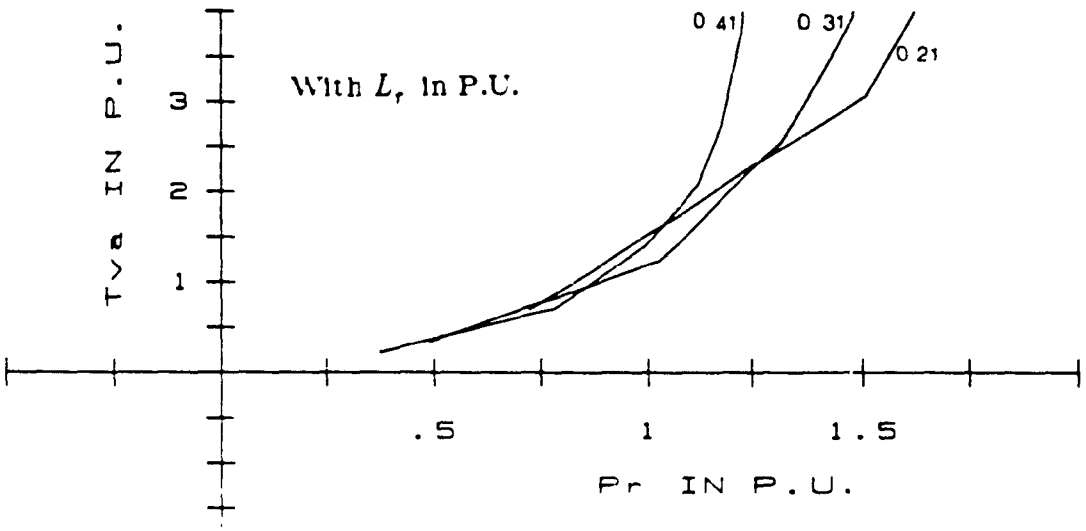


Fig. 2.13: Variation of Tva with output power for different values of L_r

Table - 2.1

Comparative Component Ratings of Passive Waveshaping Methods

	Standard Method (Fig. 2.2)	Proposed Passive Method (Fig. 2.5)
Inductor		
L_i / L_r	0.1	0.31
$I_{i(rms)}$	1.3445	1.087
Rectifier Diode		
$I_{d,0}$	0.4581	0.4573
$I_{d,rms}$	0.95	0.7686
$I_{d,peak}$	1.901	1.537
Output Capacitor(C_o)	8.314	4.65
$I_{o,2}/I_{db,2}$	1.3167	0.736
Power (P_r)	1.026	1.024
Power factor	0.763	0.957
TVA Rating	4.0658	1.234

Evaluation of Table 2.1 shows that, the proposed passive filter topology maintains high input power factor, lower rectifier diode current stresses, low input rms current and lower total VA rating of the reactive components than the standard diode rectifier. Moreover, the rectifier output current ripple is also lower than the value found for the standard diode rectifier. Thus

decreasing the size of the filter capacitor while delivering the same output power.

2.3.5 Design Example

To illustrate the significance and validity of the theoretical results obtained in the previous sections, the following design example is presented. The converter has the following specifications:

V_{in} = 208 rms ≡ 1 pu Volts.

P_r = 5,000 W ≡ 1 pu Watts.

From these values

$$1 \text{ pu Current} = \frac{5{,}000}{208} = 24.04 \text{ Amps.}$$

$$1 \text{ pu Impedance} = \frac{208}{24.04} = 8.65 \text{ Ohms}$$

$$1 \text{ pu Inductance} = \frac{8.65}{377} = 23 \text{ mH}$$

$$1 \text{ pu Capacitance} = \frac{1}{8.65 * 377} = 306.65\ \mu F$$

$$1 \text{ pu Angular frequency} = 2\pi f = 377 \text{ rad./s}$$

From Figs. 2.11 and 2.12 at maximum input power factor the value of the inductor, L_r at 1.0 pu output power is 0.31 pu which is equal to 7.13 mH. Using Eqn. (2.14) the value of the capacitor C_r is given by

$$C_r = \frac{1}{9\omega^2 L_r} = 0.3584 pu$$

$$= 109.9\ \mu F$$

Using the pu values shown in section 2.3.4 the voltage and current ratings of the various rectifier components are as follows:

Rectifier Diode

Average current, $I_{d,o}$: 0.4573 * 24.04 = 10.99 Amps.

RMS current, $I_{d,rms}$: 0.7686 * 24.04 = 18.477 Amps.

Peak current, $I_{d,peak}$: 1.537 * 24.04 = 36.95 Amps.

Peak forward voltage : $\sqrt{2}$* 208 = 294.15 Volts.

Filter Inductor L_r

Value : 0.31 * 23 = 7.13 mH

RMS current : 1.23 * 24.04 = 29.57 Amps.

Peak current : 1.735 * 24.04 = 41.817 Amps.

Filter Capacitor C_r

Value : 0.3584 * 306.65 = 109.9 μF

RMS current : 0.43 * 24.04 = 10.33 Amps.

Peak current : 0.608 * 24.04 = 14.62 Amps.

DC Filter Capacitor C_o

Peak voltage : 1.12 * 208 = 232.96 Volts.

120 Hz ripple current, $I_{o,2}$: 0.736 * 24.04 = 17.7 Amps.

Value : 4.65 * 306.65 = 1425.93 μF

.t is noted that the rectifier diode currents and C_o values found above are lower than the respective rectifier diode currents and C_o values found in section 2.2.3 for the typical front-end passive filter topology (fig. 2.2).

2.3.6 Experimental Results

To verify the predicted results an 1 kVA experimental converter has been implemented with the following circuit parameters:

- AC input rms voltage $E_{i(rms)} = 100$ Volts.
- Resonant Inductor $L_r = 8$ mH.
- Angular frequency (ω) of the ac input voltage = 377 rad./s

Using Eqn. (2.14) the value of the capacitor (C_r) is given by

$$C_r = \frac{1}{9 * \omega^2 * L_r} = 97.72 \ \mu F$$

Choosing a 100 μF ac capacitor, the experimental waveforms are shown in Fig. 2.14. In particular evaluation of Fig. 2.14(a) shows that the input current I_i and its spectrum are in agreement with the predicted per unit results shown in Fig. 2.10. The power factor of the proposed front-end rectifier is calculated as follows:

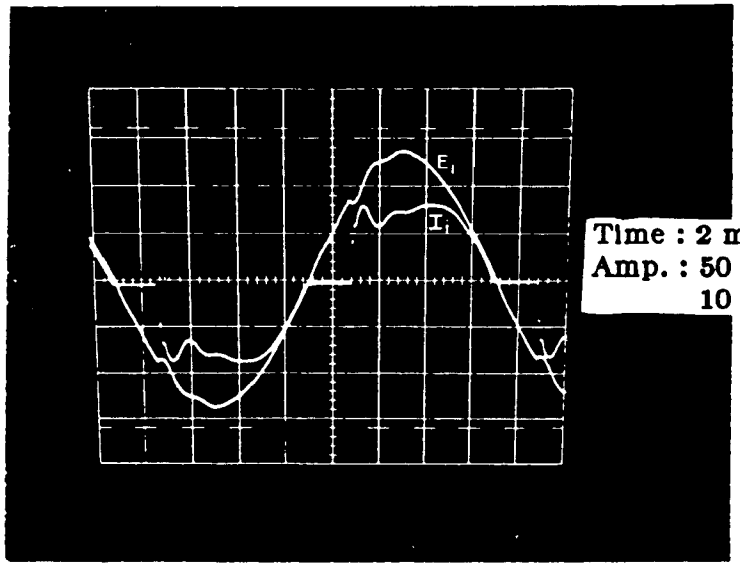
- Input ac rms voltage ($E_{i(rms)}$) = 100 Volts.
- Input ac rms current ($I_{i(rms)}$) = 12.4 Amps.
- Load dc voltage (V_L) = 100 Volts
- Load dc current (I_{in}) = 11 Amps.

Using the above information, the input power factor is given by

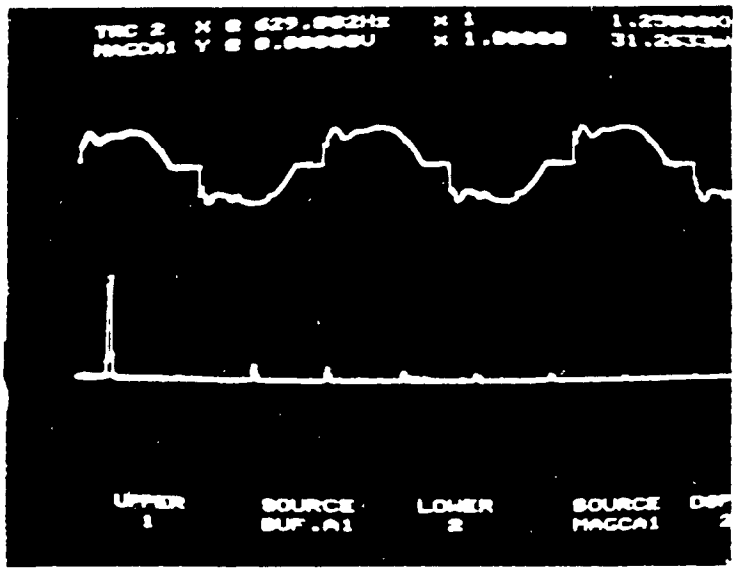
$$Power\ Factor = \frac{V_L * I_{in}}{E_{i(rms)} * I_{i(rms)}} = 0.887 \qquad (2.36)$$

Comparison of Eqns. (2.12) and (2.36) shows that the proposed passive bridge rectifier exhibits high input power factor while delivering more output power.

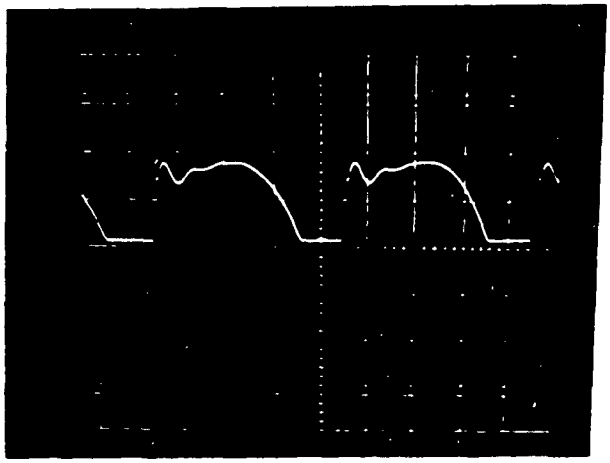
(a)



Time : 2 ms/div.
Amp. : 50 V/div.
10 A/div.

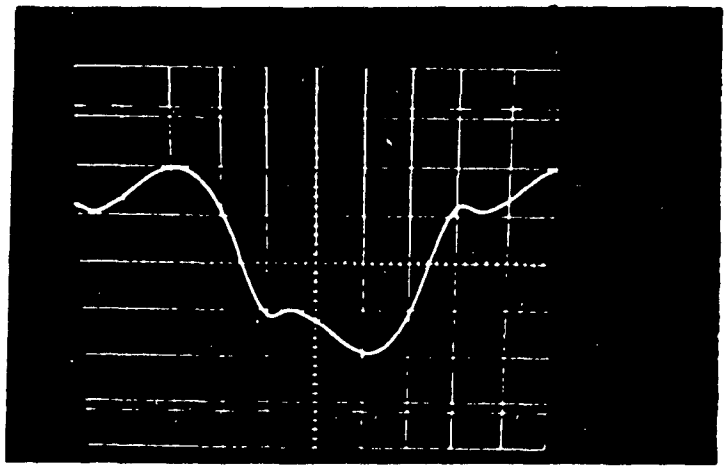


(b)



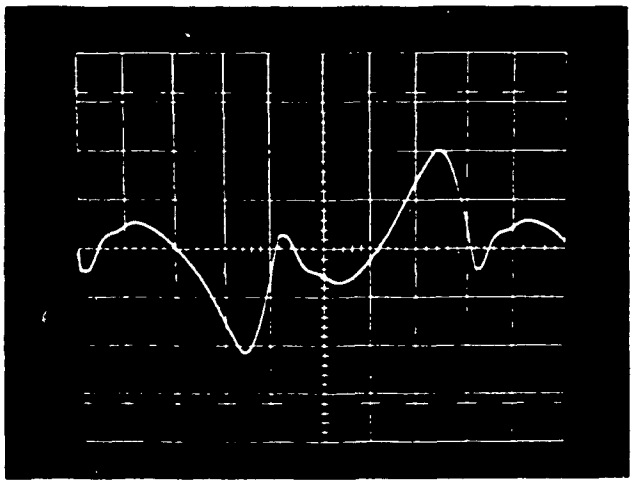
Time : 2 ms/div.
Amp. : 10 A/div.

(c)



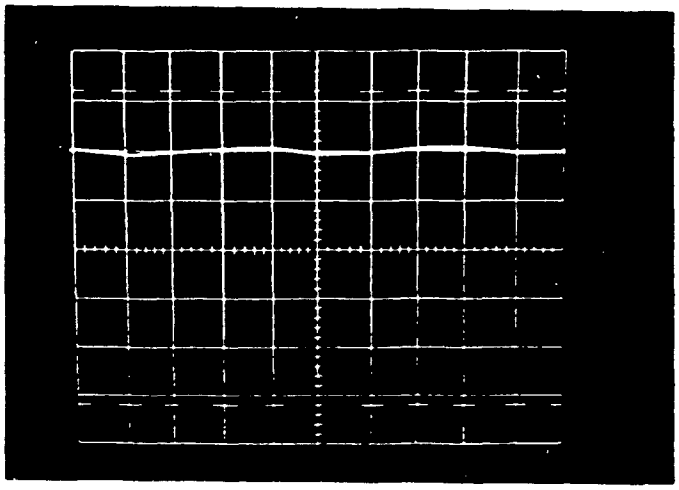
Time : 2 ms/div.
Amp. : 10 A/div.

(d)



Time : 2 ms/div.
Amp. : 50 V/div.

(e)



Time : 2 ms/div.
Amp. : 50 V/div.

Fig. 2.14: Experimental waveforms of the proposed passive SMR converter
(a) Input ac voltage (E_i), input current (I_i) and its spectrum.
(b) Rectifier output dc current (I_o).
(c) Resonant inductor current (I_l).
(d) Resonant capacitor voltage (V_r).
(e) Output dc voltage (V_L).

The variation of input power factor on the one kVA laboratory unit is shown in Fig. 2.15 with the output voltage (V_L). The experimental results shown in Fig. 2.15 are in agreement with the predicted results shown in Fig. 2.11.

2.3.7 Conclusions

In this section a novel passive input current waveshaping method for single-phase fed SMR converters has been proposed. The front-end bridge rectifier operation has been analyzed in detail and the steady state performance has been obtained. Performance evaluation and related design data have been provided for implementation of the front-end diode rectifier. Detailed input current and output current analysis has shown that the proposed passive input filter topology yields higher input power factor and delivers more output power as compared to the conventional front-end diode rectifier. Finally, predicted features such as input/output waveforms associated harmonic spectra have been verified experimentally on a one kVA laboratory unit.

2.4 Conclusions

In this chapter some key analysis and design aspects of passive input current waveshaping methods have been presented. Performance evaluation and related design data are provided for implementation of the front-end diode rectifier. Detailed input current and output current analysis has shown that the proposed passive bridge rectifier topology (Fig. 2.5) exhibits the following advantages over the conventional front-end diode rectifier topologies.

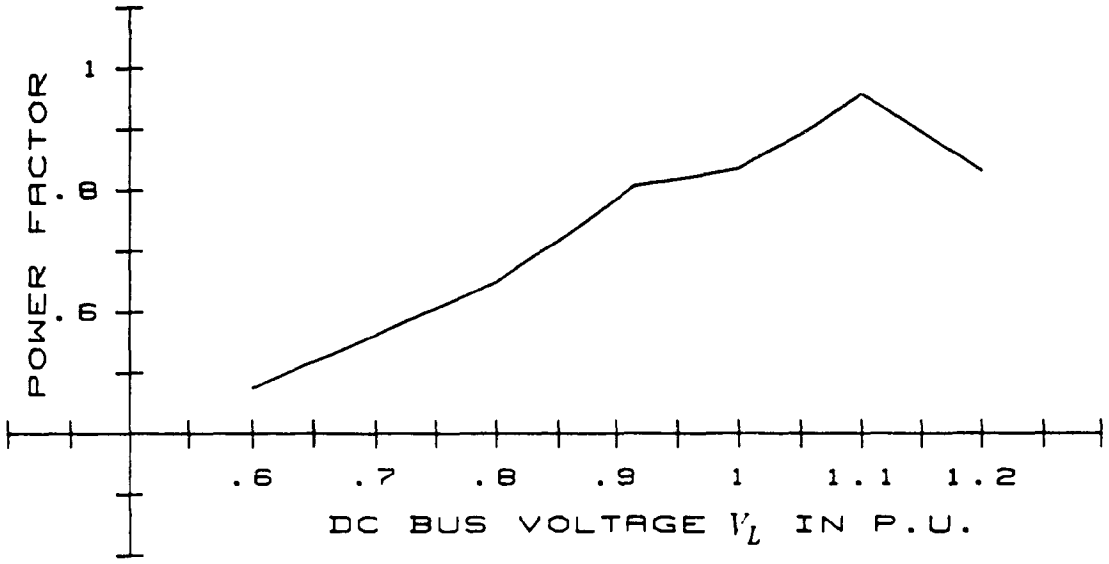


Fig. 2.15: Experimental variation of input power factor with dc bus voltage (V_L)

(i) High input power factor.

(ii) Low total VA rating of the reactive components.

(iii) Low input rms current.

(iv) Lower rectifier diode current stresses.

Finally, selected key results have been verified experimentally.

CHAPTER 3

Active Input Current Waveshaping Section

3.1 Introduction

3.1.1 Active Waveshaping Methods

In general passive input current waveshaping methods discussed in Chapter 2 have the advantages of being easy to understand, easy to implement, high input power factor and they are more reliable than their active counterparts. However they also have several disadvantages including:

(i) they are bulky and heavy;

(ii) the input power factor can be optimized only for a narrow range of operating points;

(iii) the cost of the series capacitor in the resonant input filter method and the cost of the ferro resonant transformer in the ferro resonant transformer method, is relatively high;

(iv) the relatively large input inductor results in a significant dc bus voltage regulation which will have a negative impact on the associated inverter voltage control strategy.

(v) the output voltage is controlled by the post voltage regulator (dc-to-dc converter) which in turn will reduce the performance of the dc-to-dc converter.

These disadvantages can be eliminated through the use of active input current

waveshaping methods [3,5] (Fig. 3.1).

3.1.1.1 Boost Active

An excellent description of five (5) different current control methods suitable for active input current waveshaping are presented in detail in [5]. These are:

(i) the bang-bang hysteresis control method;

(ii) the constant-off-time control method;

(iii) the constant-on-time control method;

(iv) the constant frequency with turn-on at clock time control method;

(v) the constant frequency with turn off at clock time control method.

Application of the first method in improving the input power factor of single-phase supplied ac-to-dc converters is presented in detail in [3]. This reference proposes two different active current waveshaping methods. With the first method the boost inductor current, I_o, emulates the ac source voltage, E_i, and is referred to as a resistor emulator (Fig. 3.2(a)). The advantage of this method is that it yields a near unity input power factor. However it requires some means of sensing and processing the respective input voltage waveform. With the second method the boost inductor current is maintained constant for each operating point (Fig. 3.2(b)) and is referred to as an inductor emulator. Consequently no voltage sensing is required. However the input power factor value decreases from near unity to 0.9. The power factor can be improved to 0.95 by forcing the current to be constant only for 120 degrees during the each half cycle instead of 180 degrees (Fig. 3.2(c)).

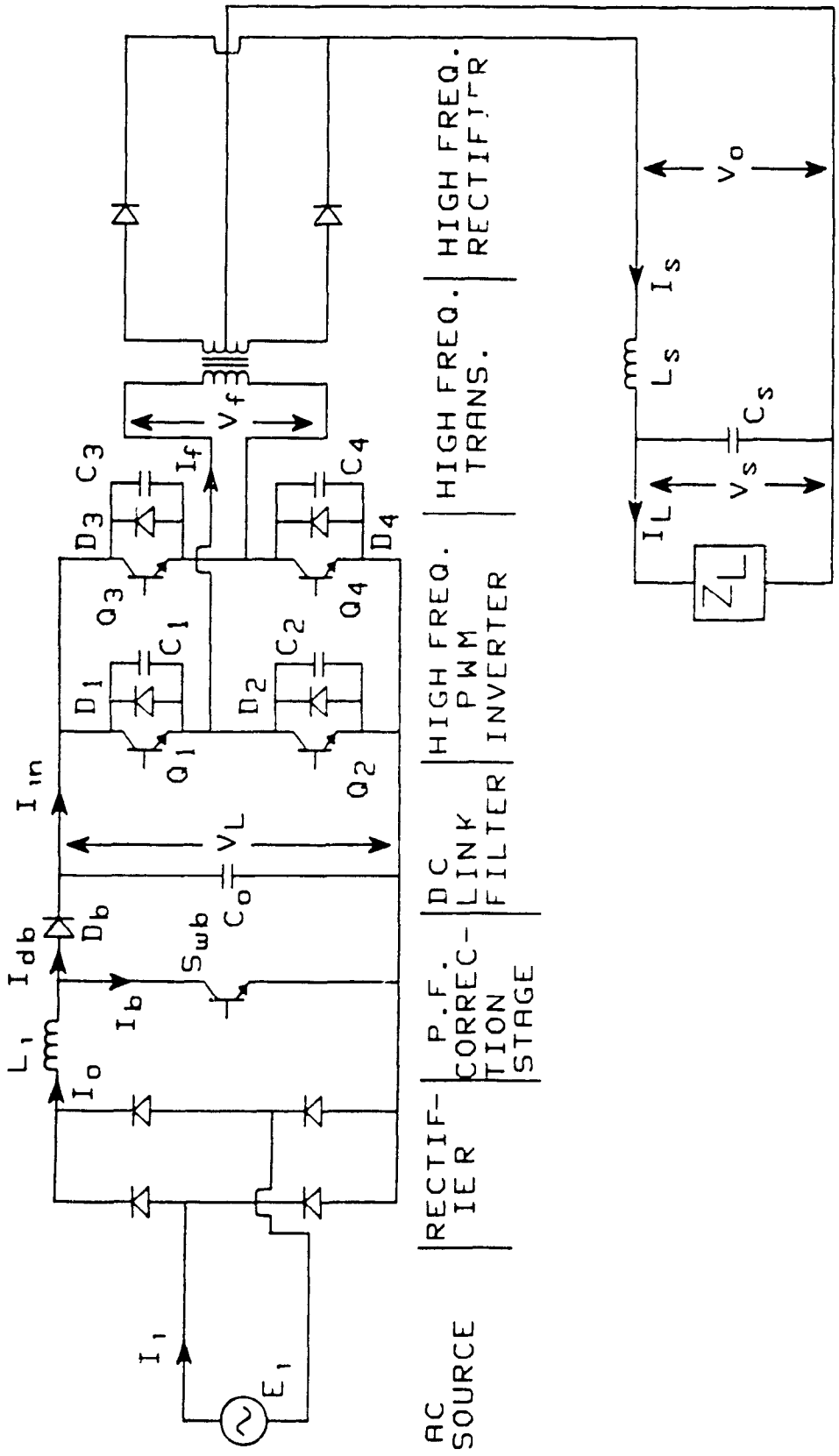


Fig. 3.13 SMR converter with front-end active filter topology

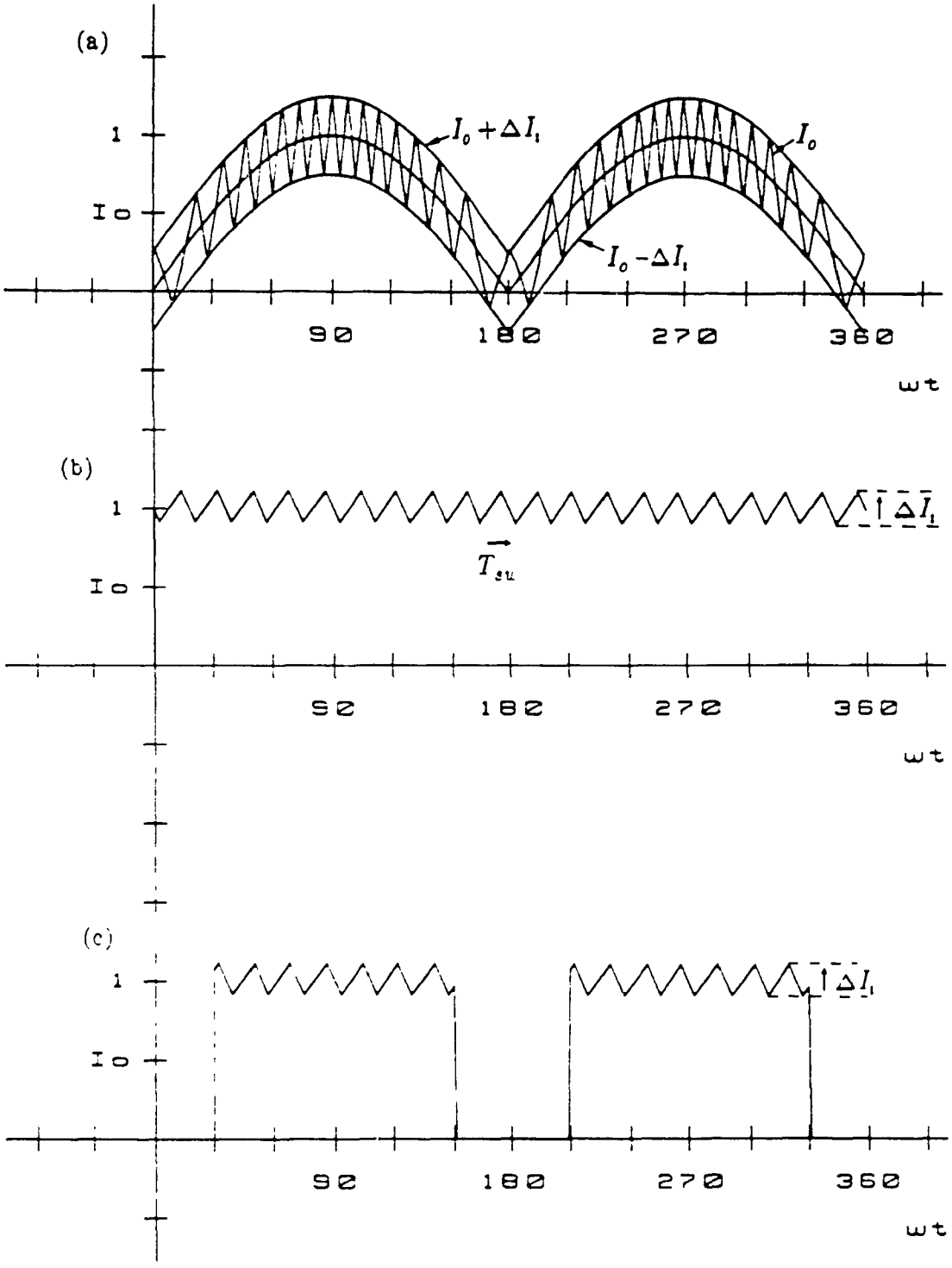


Fig. 3.2: Active input current waveshaping dc link inductor current (I_o)
(a) In resistor emulator;
(b) In inductor emulator;
(c) In modified inductor emulator.

One additional and crucial advantage of the above active current wave shaping methods is that they can also be used to regulate the converter dc bus voltage. Therefore deterioration of converter performance because of ac input voltage and source variations can be avoided [21]. Specifically, the resulting ac-to-dc active filter topology (Fig. 3.1) has the following advantages:

(i) lower power semiconductor device current ratings (peak current etc.);

(ii) higher efficiency because of the low rms value of the input current;

(iii) a lower second order harmonic component which in turn reduces the size of the filter capacitor;

(iv) increased operating range;

(v) raised output power levels per module.

However in the bang-bang hysteresis control method, the switching frequency of the converter is load dependent. The proposed single-phase fed boost active power factor correction method eliminates the above disadvantage and maintains unity input power factor from maximum to minimum load variation while keeping the switching frequency constant. The passive input power factor correction method is more and more attractive where the reliability of the converter is of prime importance.

For medium to high power applications (3 kW to 20 kW) the front-end diode rectifier is fed from a three-phase ac source. Application of the bang-bang hysteresis control method to improve the input power factor of a three-phase ac-to-dc converter has been discussed by several authors [4,12,13]. In these references the three-phase ac-to-dc converter has been realized using three single-phase ac-to-dc converters using suitable input and output

connections (Fig. 3.3). This topology yields unity input power factor and is clearly much superior to the original phase controlled ac-to-dc topologies. However, it also exhibits some disadvantages including:

(i) It requires complicated input synchronization logic.

(ii) Owing to the variations in power circuit control parameters among the three individual converters, a complete triplen harmonic elimination from the input line current (I_{ia}) cannot be achieved.

(iii) The switching frequency is load dependent.

(iv) The number of components required for three-phase ac to dc converter is three times the single-phase ac to dc converter.

The objective of this section is to propose and analyze a novel single-phase and three-phase fed ac-to-dc active filter topologies which draws high quality input current waveforms from the ac source and exhibits none of the above mentioned disadvantages. However, the proposed front-end three-phase fed active filter topology has the disadvantages of substantially increasing the current and voltage stresses of the boost switching device and the high frequency ripple content of the pre-filtered ac input currents. Finally, key theoretical results are verified experimentally on a one kVA laboratory prototype unit.

3.1.1.2 Synchronous Active

For medium power applications the three-phase fed boost active filter topology that uses a diode rectifier and a single switch is a good choice to satisfy the requirements mentioned in section 3.1.1.1. However it exhibits

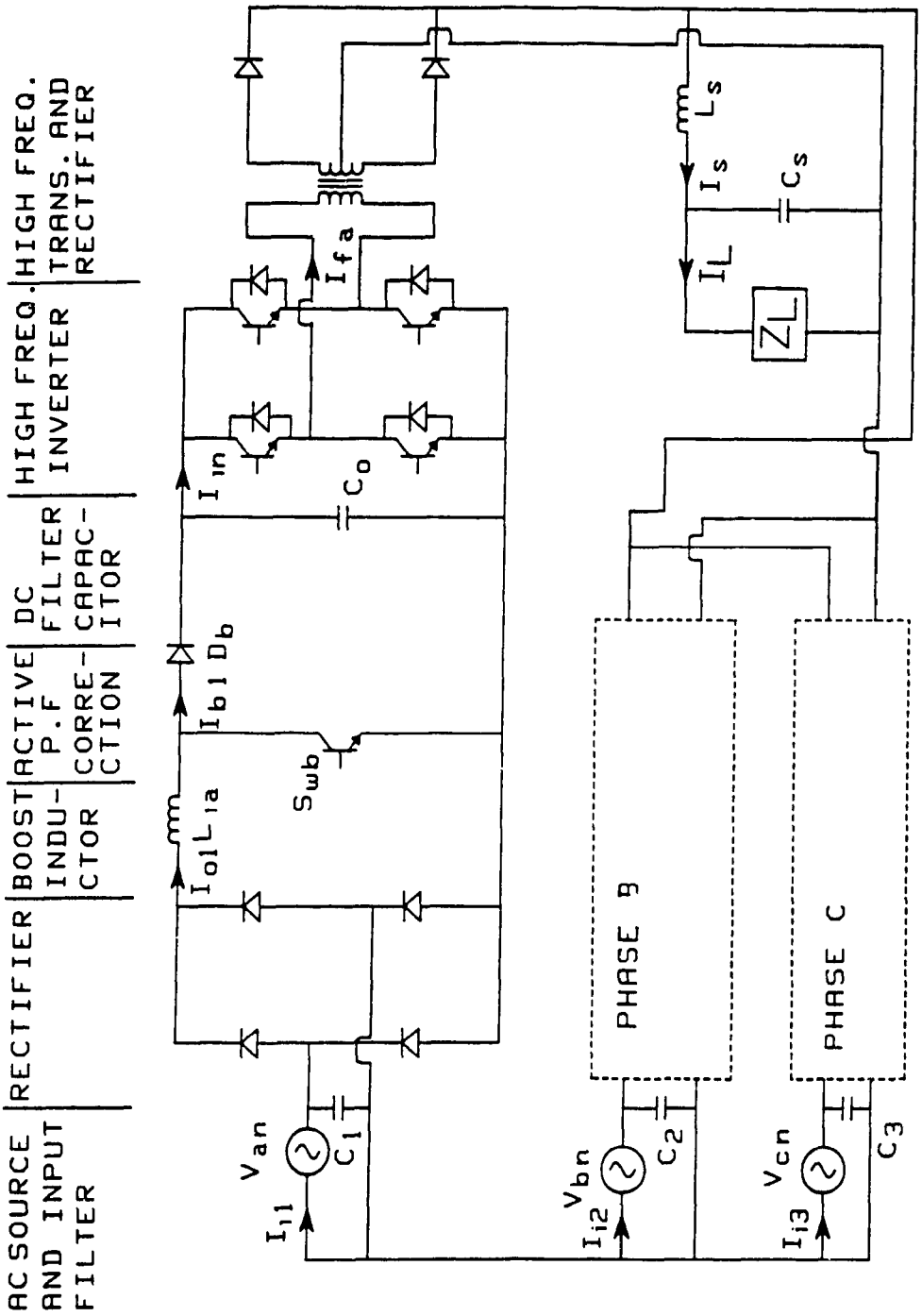


Fig. 3.3: Conventional three-phase ac-to-dc active filter topology

certain disadvantages including:

(i) increases the switching stresses of the switching devices;

(ii) dc bus voltage has to be maintained always higher than the peak ac input voltage. In case of three-phase fed boost topology dc bus voltage is approximately five (5) times the ac source rms voltage.

(iii) output voltage control is achieved from maximum to minimum load variation only.

The objective of this section is to propose and analyze a novel three-phase fed ac-to-dc synchronous active filter topology which draws high quality input current waveforms from the ac source and exhibits none of the above mentioned disadvantages. Moreover, the proposed inductor fed synchronous rectifier topology eliminates all the above disadvantages and exhibits high power density, improved reliability, elimination of the input filter ac capacitors, and elimination of the dc filter inductor.

Finally, experimental results from a prototype rectifier unit are compared and verified with the analytically predicted results.

3.2 Proposed Single-Phase Fed Boost Active Filter Topology

In section 3.1.1.1 several active waveshaping methods to improve the input power factor of a single phase diode rectifiers have been mentioned. Each one of these methods was found to have its own inherent limitations. The proposed active waveshaping method eliminates most of the disadvantages discussed in section 3.1.1.1 and exhibits the following advantages.

(i) practically sinusoidal input currents and unity input power factor from minimum to maximum load variation;

(ii) robust and low cost implementation which does not require sensing of input voltage (and if required can employ resistors for the sensing of the input current and the dc bus voltage);

(iii) a constant switching frequency which is a significant improvement over the 'bang-bang' hysteresis approach.

The power circuit diagram of the proposed single-phase fed active current waveshaping topology is shown in Fig. 3.4. In Fig. 3.4, C_i is the ac input high frequency capacitor that removes the switching frequency ripple (20-100kHz) from the ac input current. The high frequency capacitor C_f has been placed in parallel with an electrolytic dc capacitor C_o to absorb and to protect C_o from the high frequency current component in the diode current I_{db}. The description of one of the many possible converter control circuits is as follows. The control circuit (Fig. 3.5) accepts three inputs and produces one output (V_g). The inputs are:

(i) the boost inductor current signal I_o (obtained across the sensing resistor R_s);

(ii) the dc bus capacitor voltage signal V_L;

(iii) the high frequency ramp signal V'_{rmp}.

The only generated output signal is the boost switch S_{wb} gating signal V_g. The dc bus capacitor voltage signal V_L is first reduced in amplitude and prefiltered by the voltage divider arrangement of components. Finally, the ramp signal V'_{rmp} which has been conditioned by multiplication and the current signal I_{fd} are fed to the comparator inputs. The output of the com-

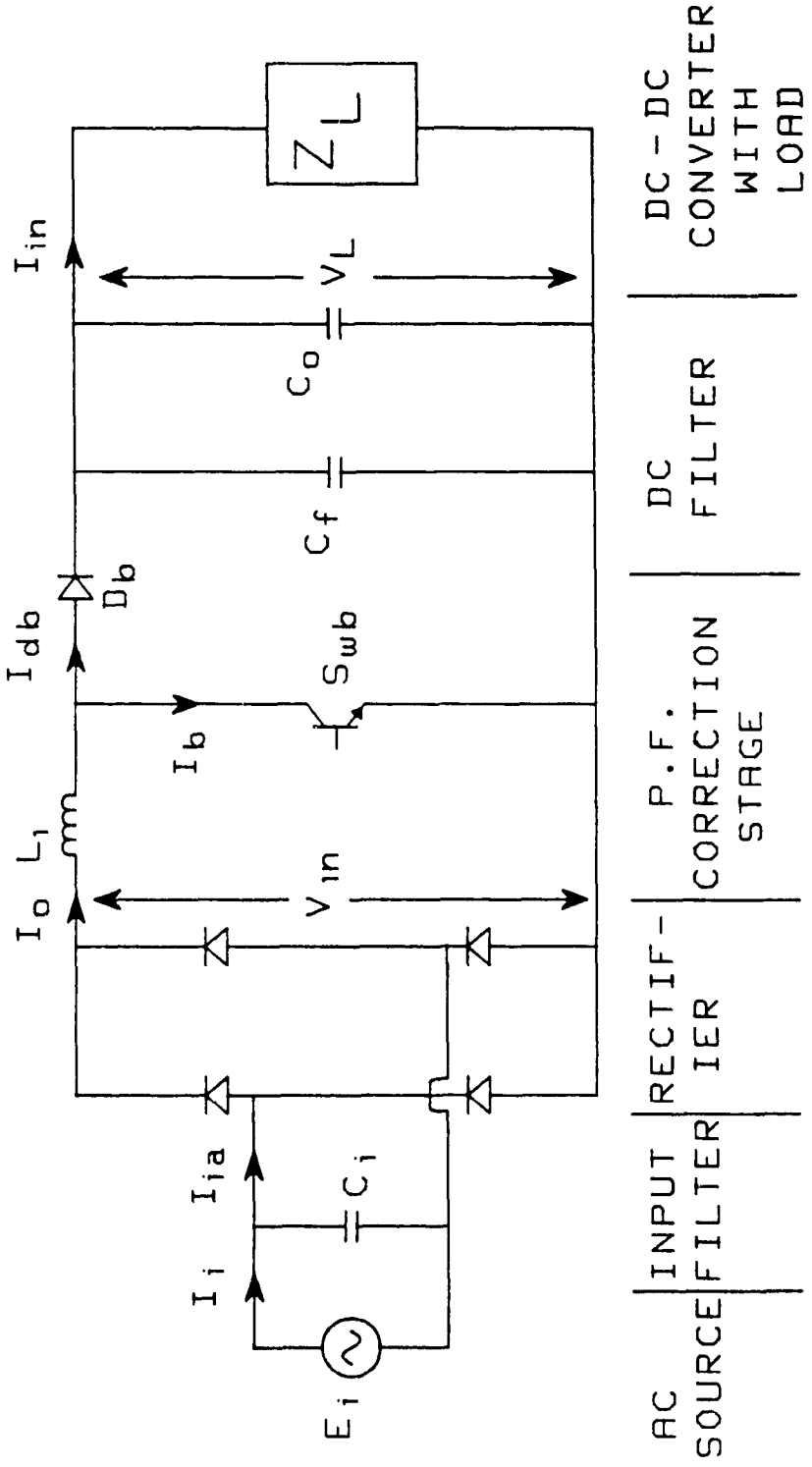


Fig. 3.1: Proposed front-end active filter topology

parator is next supplied to the 'driver' integrated circuit gate (4050) which in turn outputs the boost switch, S_{wb}, gating signal, V_g. It is noted that in this realization the gating signal V_g is applied to S_{wb} through an opto-isolation stage.

3.2.1 Principles of Operation and Topology

The basic block diagram of the proposed current waveshaping circuit is shown in Fig. 3.5. The simplified circuit diagram of the respective power circuit is shown in Fig. 3.6. From these two figures the basic principles of operation are as follows:

(i) The power circuit (Fig. 3.6) employs the boost inductor, L_i, and switch S_{wb} to force the input current, I_i to become nearly sinusoidal and in phase with the input voltage thus providing a nearly unity input power factor.

(ii) The control circuit (Fig. 3.5) consists of two control loops and associated signal conditioning components. The internal (current) loop senses the boost inductor current, I_o, as a voltage drop across a sensing resistor R_s and after appropriate conditioning compares it with a constant frequency (20-100kHz) ramp waveform, V'_{rmp}. The comparator outputs a positive pulse V_g whenever V'_{rmp} is greater than I_{fd}. V_g becomes the gating signal for the boost switch S_{wb}. Consequently, if for some reason (e.g. load short circuit) I_{fd} is greater than V'_{rmp} no gating signal is provided to S_{wb}, thus preventing switch damage. The comparator action also ensures (see section 3.2.2) that the input current is sinusoidal. From the above

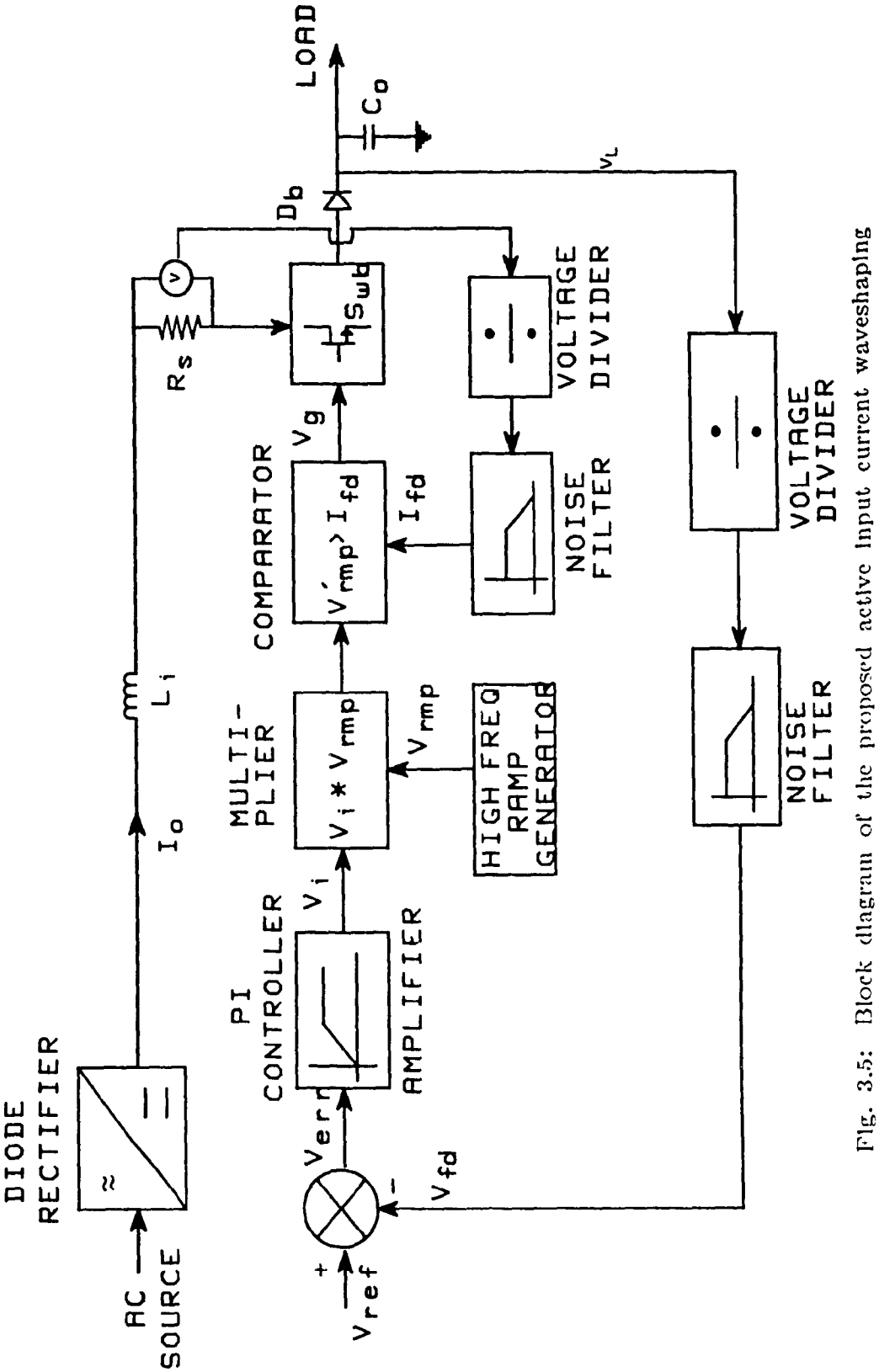


Fig. 3.5: Block diagram of the proposed active input current waveshaping circuit

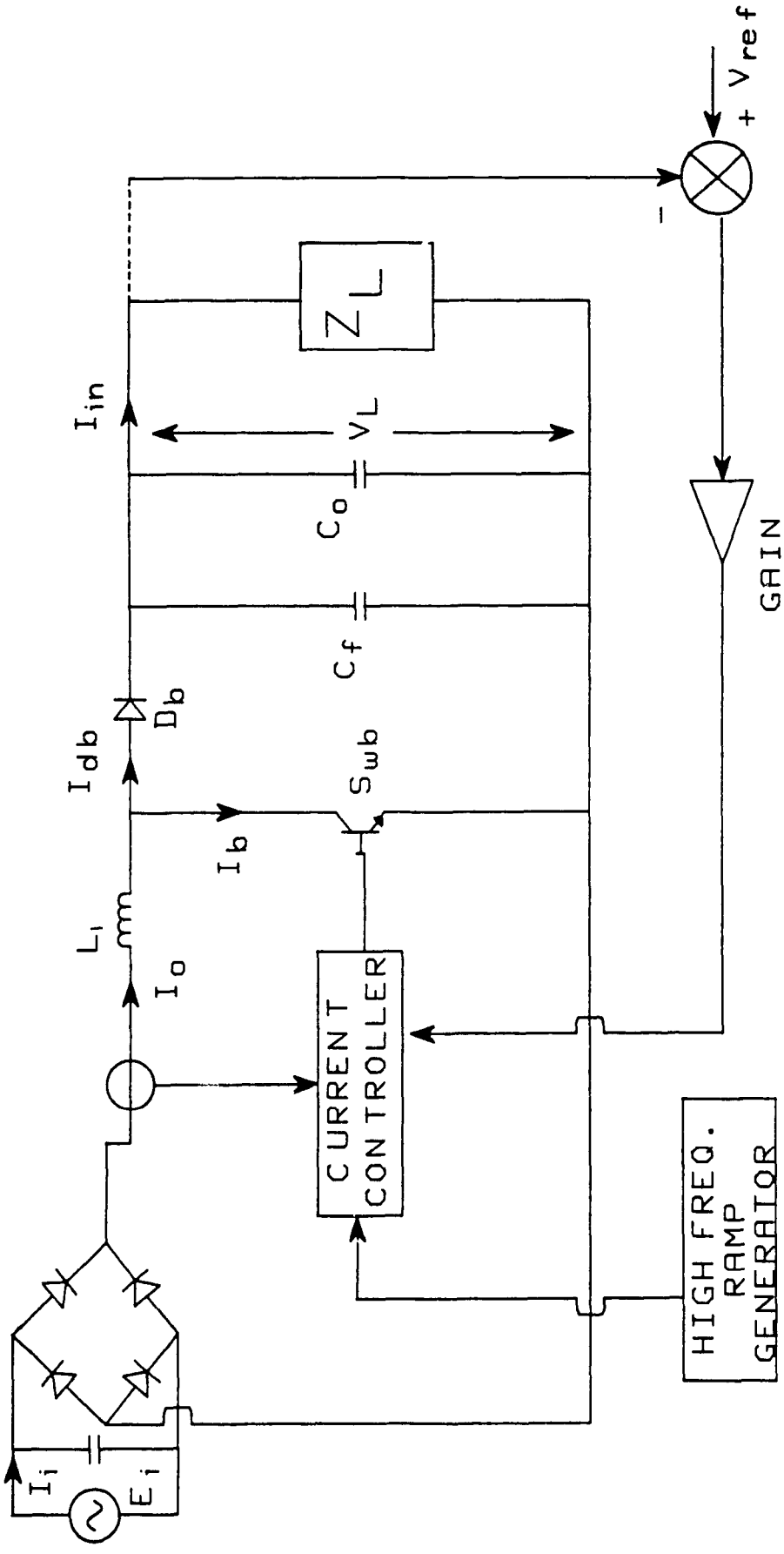


Fig. 3.6: Simplified circuit of the proposed active input current waveshaping method

discussion it also follows that if the amplitude of V'_{rmp} increases or decreases input current I_i will be similarly affected. For this reason the original ramp signal V_{rmp} is multiplied with the output of the voltage loop error amplifier signal V_i. Therefore, if the dc bus voltage V_L goes above the equilibrium value set by V_{ref} then V_{fd} will also increase which in turn will cause the V_{err} and V_i signals to decrease. Also, this action will in turn decrease signal V'_{rmp} which will finally decrease the rectifier output current I_0 by decreasing the on-time of switch S_w. This sequence of actions ensures that V_L always returns to the value dictated by the reference voltage V_{ref}.

3.2.2 Principles of Input Current Control and Waveshaping

The current I_{fd} (Fig. 3.7) represents the conditioned instantaneous input current during a given period of control ramp V'_{rmp}. Then from Fig. 3.7

$$t_{off} = \frac{I_{fd}}{V_p} T_{sw} \Rightarrow t_{on} = T_{sw} - t_{off} = T_{sw}\left(1 - \frac{I_{fd}}{V_p}\right)$$

where V_p is the peak value of the ramp V'_{rmp}. Also the duty cycle, D, is

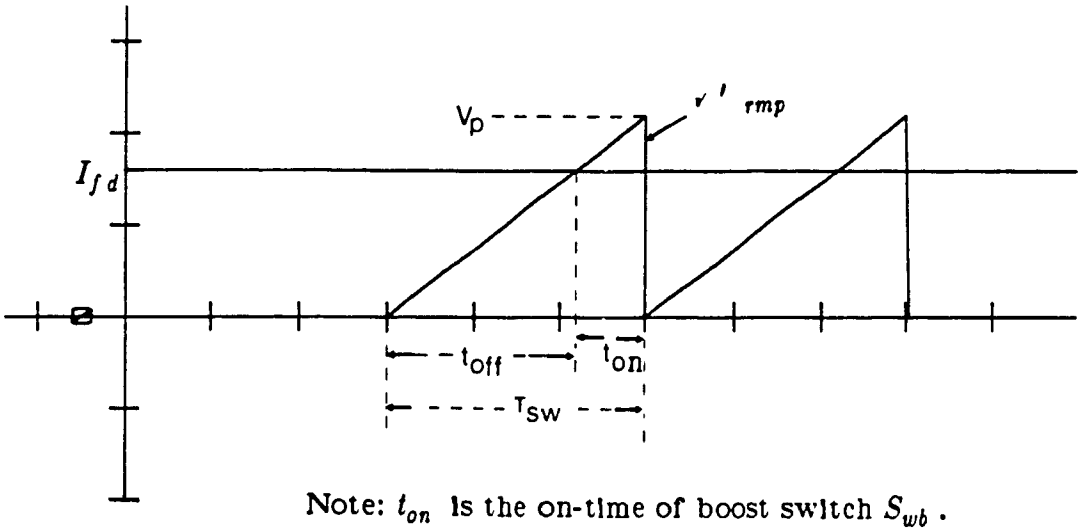
$$D = \frac{t_{on}}{T_{sw}} = 1 - \frac{I_{fd}}{V_p}$$

or

$$1 - D = \frac{I_{fd}}{V_p} \tag{3.1}$$

For any boost chopper

$$\frac{V_L}{V_{in}} = \frac{1}{1 - D} \tag{3.2}$$



Note: t_{on} is the on-time of boost switch S_{wb} .

Fig. 3.7: Principle of the active input current current control

From Eqns. (3.1) and (3.2)

$$\frac{V_L}{V_{in}} = \frac{1}{\frac{I_{fd}}{V_p}} \Rightarrow I_{fd} = \left(\frac{V_p}{V_L}\right) V_{in}$$

but

$$V_{in} = \sqrt{2} * E \left|\sin(\omega t)\right| \tag{3.3}$$

$$\Rightarrow I_{fd} = \frac{V_p}{V_L}\sqrt{2} * E \left|\sin(\omega t)\right|$$

$$\Rightarrow I_{fd} = k_1 \left|\sin(\omega t)\right|$$

Finally, since the input ac current $I_i = K_2 I_{fd}$

$$I_i = K_3 \sin(\omega t) \tag{3.4}$$

Equations (3.3) and (3.4) show that with the adopted current waveshaping method (assuming a ramp frequency $f_{rmp} >> 60$ Hz) the input ac current I_i and voltage E_i are identical in shape and in phase with the exception of the f_{rmp} ripple component. Therefore for all practical purposes the input power factor is unity. Thus, compared to the 'bang-bang' hysteresis control method, this method is superior in that it does not require input voltage waveshape sensing and in that the switching frequency is constant and load independent.

3.2.3 Front-end Section

The Converter is analyzed under the same assumptions used in section 2.2.1. Also by assuming the filter capacitor voltage to be about 10-percent above peak input voltage the rated dc bus voltage is

$$V_L = 1 * \sqrt{2} * 1.1 = 1.556 \quad pu \tag{3.5}$$

Also, the peak value, $I_{i,peak}$, of the rectifier input current I_i (Fig. 3.6) becomes

$$I_{i,peak} = \sqrt{2} \quad pu \tag{3.6}$$

By further assuming a ±5-percent peak-to-peak average current ripple (or 10-percent $\overline{\Delta I_i}$)

$$I_{i,max} = 1.485 \quad pu \tag{3.7}$$

and

$$I_{i,min} = 1.343 \quad pu \tag{3.8}$$

with $\overline{\Delta I_i}$ having been defined and the switching frequency, f_{sw}, known, the value of the boost reactor L_i can be estimated. In Fig. 3.8, $\overline{V}_{in}$, the average value of the rated rectifier dc output voltage and, V_L, the rated dc bus voltage are given by

$$\overline{V}_{in} = \frac{\sqrt{2} * 2}{\pi} = 0.9 \quad pu \tag{3.9}$$

and

$$V_L = 1.556 \quad pu$$

Also from the same figure

$$\overline{t}_1 = \frac{(\overline{\Delta I_i})(L_i)}{\overline{V}_{in}}, \quad \overline{t}_2 = \frac{(\overline{\Delta I_i})(L_i)}{V_L - \overline{V}_{in}}$$

where,

$\overline{t}_1$ is the average on time of the boost switch S_{wb}.

$\overline{t}_2$ is the average off time of the boost switch S_{wb}.

or

$$T_{sw} = \overline{t}_1 + \overline{t}_2 = (\overline{\Delta I_i})(L_i)\frac{V_L}{(V_L - \overline{V}_{in})\overline{V}_{in}}$$

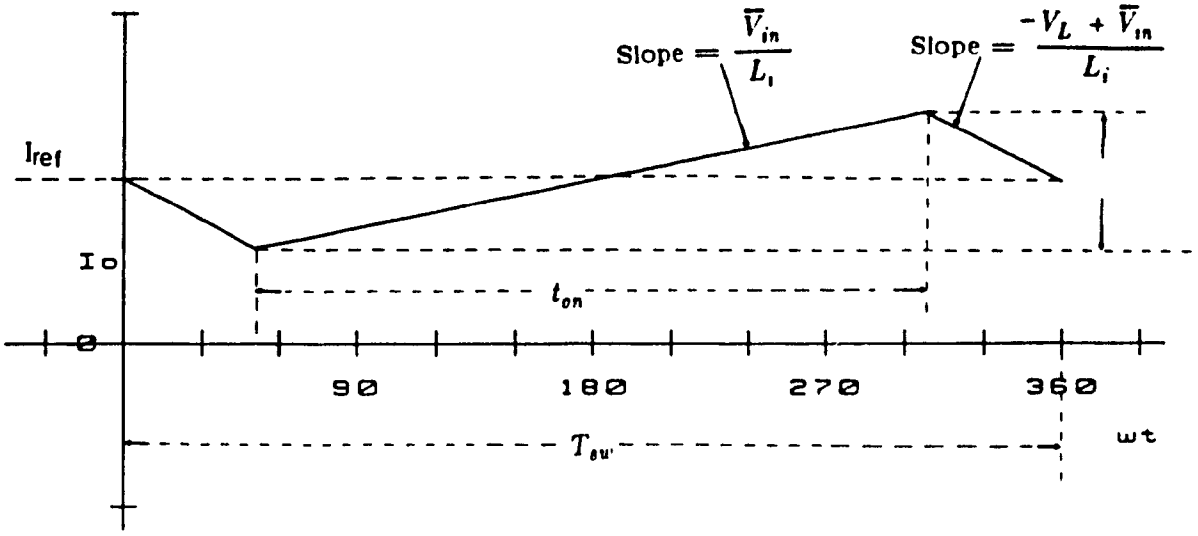


Fig. 3.8: Input current waveform for a random switching period (T_{sw})

and

$$L_i = \left(T_{sw} \right) \frac{\left(V_L - \overline{V}_{in} \right) \overline{V}_{in}}{V_L \left(\Delta \overline{I}_i \right)} \tag{3.10}$$

Now from boost converter theory it is known that

$$\frac{V_L}{\overline{V}_{in}} = \frac{1}{1 - \overline{D}}$$

where $\overline{D}$ in this case is the average duty cycle.

Therefore

$$\frac{V_L}{\overline{V}_{in}} = \frac{1}{1 - \overline{D}} = \frac{1.556}{0.9} \approx 1.73 \tag{3.11}$$

$$\overline{D} \approx 0.442 \tag{3.12}$$

Also from Eqn. (3.11);

$$D(t) = 1 \quad \frac{V_{in}(t)}{V_L} = 1 \quad 0.01 \left| \sin(377t) \right| \tag{3.13}$$

Therefore, the discontinuous expression for the boost switch current becomes

$$I_{sw} = \sqrt{2}(1 - 0.01 \left| \sin(377t) \right|) * \left| \sin(377t) \right| \ pu \tag{3.14}$$

and for the diode D_1

$$I_{d1} = 1.285 \sin^2(377t) = 0.643 \quad 0.643 \cos(754t) \ pu \tag{3.15}$$

The dc component $I_{d1\ 0} = \frac{1}{1.556} = 0.643$ pu of current I_{d1} goes to the load.

Consequently the filter capacitor current is given by

$$I_{d1\ 2} = \frac{1.285}{2} \cos(754t) \ pu \tag{3.16}$$

Therefore, the filter capacitor second harmonic ripple voltage is to be limited to 5-percent (or 0.05 * 1.556 = 0.0778 pu) the respective X_c value becomes

$$X_{co} = \frac{0.0778 * 2 * 2 * \sqrt{2}}{1.285} = 0.342 \ \ pu \tag{3.17}$$

and

$$C_o = 2.915 \ \ pu \tag{3.18}$$

3.2.4 Component Ratings

From the aforementioned assumptions and derived analytical expressions the voltage and current ratings of the various system components are as follows:

Rectifier Diode

Average current, $I_{d,o}$: 0.555 pu

RMS current, $I_{d,rms}$: 0.743 pu

Peak current, $I_{d,peak}$: 1.485 pu

Peak forward voltage : $\sqrt{2}$ pu

Boost Reactor L_i

Value of L_i : Eqn. (3.10)

Peak L_i current : 1.485 pu

Rms L_i current : 1.011 pu

Boost Switch S_{wb}

Peak forward Voltage : 1.556 pu

Peak current : 1.485 pu

Rms current $=\sqrt{1-(0.72)^2}$: 0.69 pu

Average current : 0.26 pu

Boost Diode D_b

Peak reverse blocking voltage : 1.556 pu

Rms current $= \sqrt{(0.643)^2 + \left(\frac{0.643}{\sqrt{2}}\right)^2}$: 0.72 pu

Average current : 0.643 pu

DC filter Capacitor C_o

Peak Voltage : 1.556 pu

Rms ripple current : 0.454 pu

Value : 2.915 pu

Comparative component ratings in pu of the proposed passive waveshaping method, the standard diode bridge rectifier and proposed active waveshaping method are summarized in Table 3.1.

Table - 3.1

Comparative Component Ratings of Single-phase Waveshaping Methods

	Standard Method (Fig. 2.2)	Proposed Passive Method (Fig. 2.5)	Proposed Active Method (Fig. 3.4)
Inductor			
L_i / L_r	0.1	0.31	Eqn. (3.10)
$I_{i\,(rms)}$	1.3445	1.087	1.011
Rectifier Diode			
$I_{d\,,0}$	0.4581	0.4573	0.555
$I_{d\,,rms}$	0.95	0.7686	0.743
$I_{d\,,peak}$	1.901	1.537	1.485
Output Capacitor(C_o)	8.314	4.65	2.915
$I_{o\,,2}/I_{db\,,2}$	1.3167	0.736	0.643
Power (P_r)	1.026	1.024	1.0
Power factor	0.763	0.957	1.0
Tva Rating	4.0658	1.234	-

Evaluation of Table 3.1 shows that, the proposed passive filter topology maintains high input power factor, lower rectifier diode current stresses, low input rms current and lower total VA rating of the reactive components than the standard diode rectifier. Moreover, the rectifier output current ripple is also lower than the value found for the standard diode rectifier. Thus

decreasing the size of the filter capacitor while delivering the same output power.

Evaluation of proposed active and passive methods show that the switching stresses of the diodes, input power factor, and output filter capacitor values are further improved by the active waveshaping method. Moreover the main advantage of the active method over the passive method is that the inductor size can be controlled by changing the input current ripple or by increasing the switching frequency. Hence comparison of inductor is omitted. However active method has the disadvantage of requiring additional control logic over the passive method.

3.2.5 Design Example

To illustrate the significance and understanding of the theoretical results obtained in the previous sections, the following design example is presented. The active filter topology has the following specifications

V_{in} = 208 rms = 1 pu Volts.

P_r = 5,000 W = 1 pu Watts.

Boost switch switching frequency = 20 kHz.

From these values

$$1 \text{ pu Current} = \frac{5,000}{208} = 24.04 \text{ Amps.}$$

$$1 \text{ pu Impedance} = \frac{208}{24.04} = 8.65 \text{ Ohms}$$

$$1 \text{ pu Inductance} = \frac{8.65}{377} = 23 \text{ mH}$$

$$1 \text{ pu Capacitance} = \frac{1}{8.65 * 377} = 306.65 \ \mu\text{f}$$

1 pu Angular frequency $= 2\pi f = 377$ rad./s

Using Eqns. (3.5) and (3.9) the dc bus voltage and the rectifier dc output voltage are given by

$$V_L = 1.556 * 208 = 324 \text{ V}$$

and

$$V_{in} = 0.9 * 208 = 187 \text{ V}$$

Using the pu values shown in section 3.2.4 the voltage and current ratings of the various system components are as follows:

Rectifier Diode

Average current, $I_{d,o}$: $0.555 * 24.04 = 13.34$ Amps.

RMS current, $I_{d,rms}$: $0.743 * 24.04 = 17.86$ Amps.

Peak current, $I_{d,peak}$: $1.485 * 24.04 = 35.7$ Amps.

Peak forward voltage : $\sqrt{2} * 208 = 294.15$ Volts.

Boost Reactor L_i

Assuming 15-percent average peak to peak current ripple, using Eqn. (3.10) the boost inductor L_i is given by

$$L_i = 50 * \frac{(324 - 187)187}{324 * 0.15 * 34} = 775.0\mu H$$

RMS L_i current $= 24.04 * 1.011 = 24.31$ Amps.

Peak L_i current $= 24.04 * 1.485 = 35.64$ Amps.

Boost Switch S_{wb}

Peak forward voltage : $1.556 * 208 = 324$ Volts.

Peak current : 1.485 * 24.04 = 35.64 Amps.

Rms current : 0.69 * 24.04 = 16.62 Amps.

Average current : 0.26 * 24.04 : 6.26 Amps.

Boost Diode D_b

Peak reverse blocking voltage : 324 Volts.

Rms current : 0.72 * 24.04 = 17.34 Amps.

Average current : 0.643 * 24.04 = 15.5 Amps.

DC Filter Capacitor C_o

Peak voltage : 324 * 1.05 = 340 Volts.

120Hz ripple rms current* : 0.454 * 24.04 = 11 Amps.

Value : 2.915 * 306.65 = 893.88 μF

+ It is noted that this current is chopped at the frequency of 20 kHz.

3.2.6 Experimental Results

The proposed active filter topology experimental evaluation has been carried out with the arbitrary parameter values of.

(I) boost inductor, $L_1 = 775\mu H$;

(II) switching frequency, $f_{sw} = 20$ kHz, and ;

(III) input current ripple factor, $\overline{\Delta I_1} = 10\%$.

The performance of the power factor improvement converter was evaluated with a resistive load. The respective experimental waveforms are

shown in Figs. 3.9 to 3.17.

Fig. 3.9 shows the ac input current I_i (Figs. 3.4 and 3.7) under full load conditions (5.5 kW). As predicted, the input current waveform is practically sinusoidal and ripple free. Figs. 3.10 and 3.11 depict both input current and voltage waveforms in order to show that the input power factor is practically unity. Furthermore Figs. 3.11, 3.13 to 3.16 show that unity power factor is maintained up to minimum load. Fig. 3.17 shows the high frequency control ramp (20kHz) and master oscillator waveforms and was included to provide some insight into the functioning of the logic control circuit (Figs. 3.4 to 3.8).

However, since the L_i value is inversely proportional to the $\overline{\Delta I_i}$ and f_{su} values, it is possible to further reduce L_i either by increasing f_{su} or by allowing a larger ripple on the input current. For example, if $f_{su} = 40$ kHz and $\overline{\Delta I_i} = 20$-percent then $L_i \approx 200\mu$H. Increasing the switching frequency, however, has the following disadvantages:

(i) reduced efficiency because of increased switching and skin effect losses;

(ii) limiting the choice of boost switch to FETs;

(iii) increased cost by increasing the price of some power and logic circuit components;

(iv) decreased reliability because of increased peak current values especially under transient conditions.

From this discussion it follows that at this stage it is premature to specify the 'optimum' L_i and f_{sw} values. It also follows that such values should be based on the cost analysis and evaluation of the overall rectifier-boost converter-inverter system. Moreover, the proposed converter design can

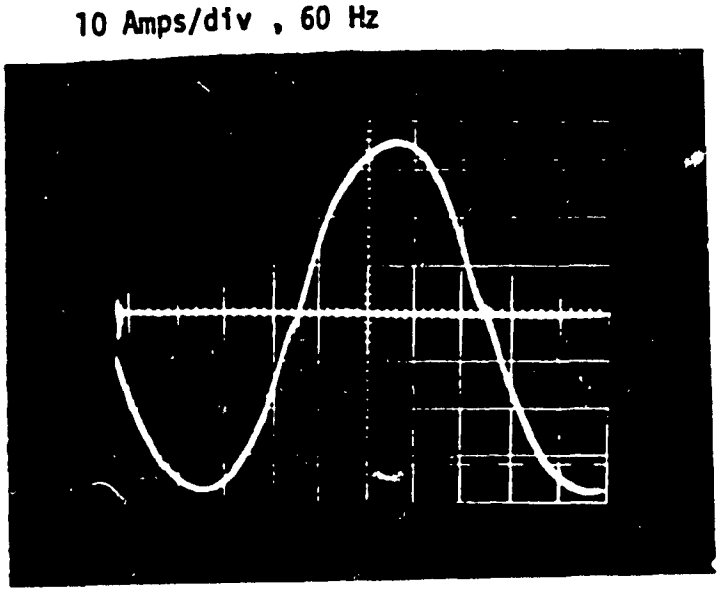


Fig. 3.9: Experimental ac input current (I_i) at rated load

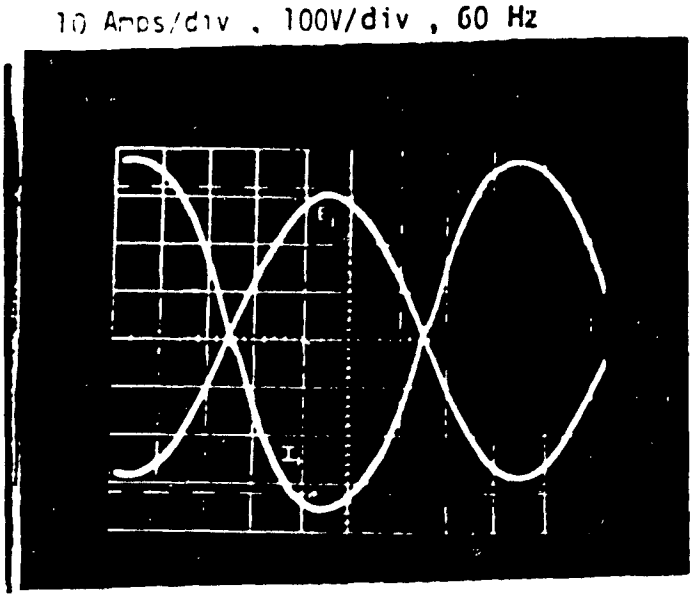


Fig. 3.10: Experimental ac input voltage (E_i) and input current (I_i) at rated load (180° out of phase)

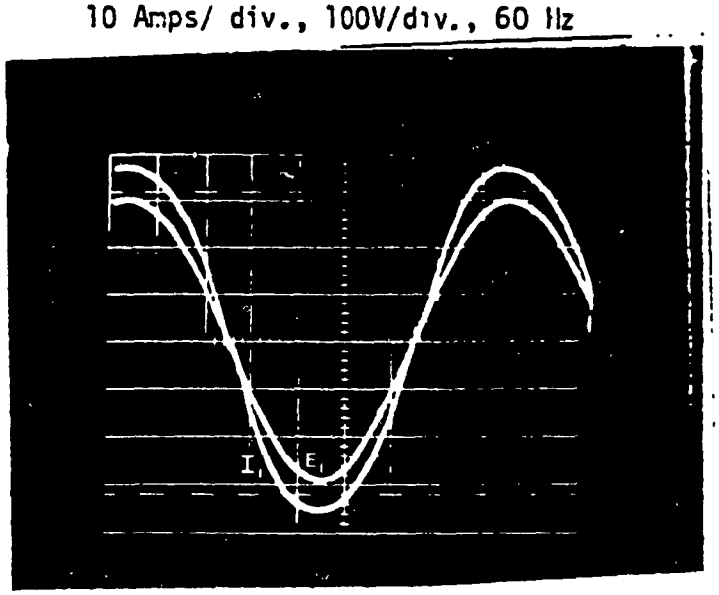


Fig. 3.11: Experimental ac input voltage (E_i) and input current (I_i) at rated load (in-phase)

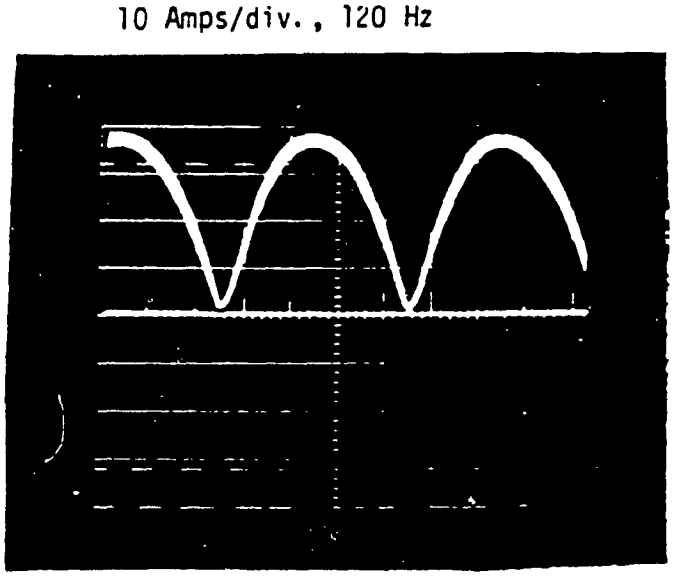


Fig. 3.12: Experimental dc link inductor current (I_o) at rated load

10 Amps/div., 100V/div., 60 Hz

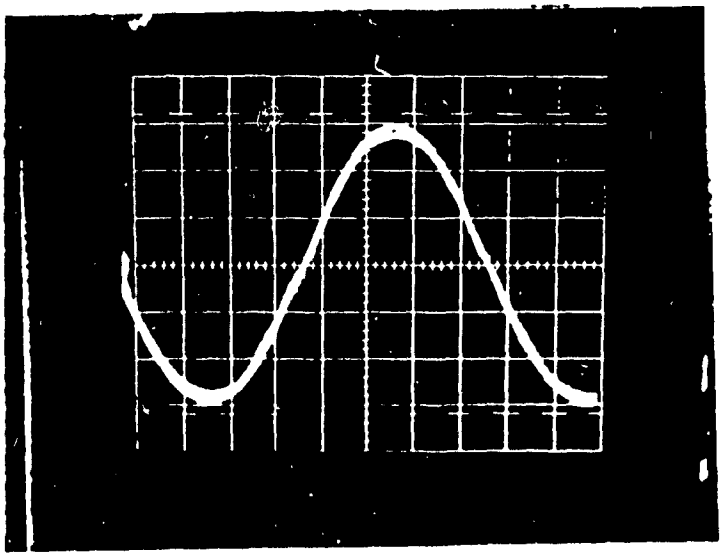


Fig. 3.13: Experimental ac input voltage (E_i) and current (I_i) at 75-percent rated load

10 Amps/div., 100V/div., 60 Hz

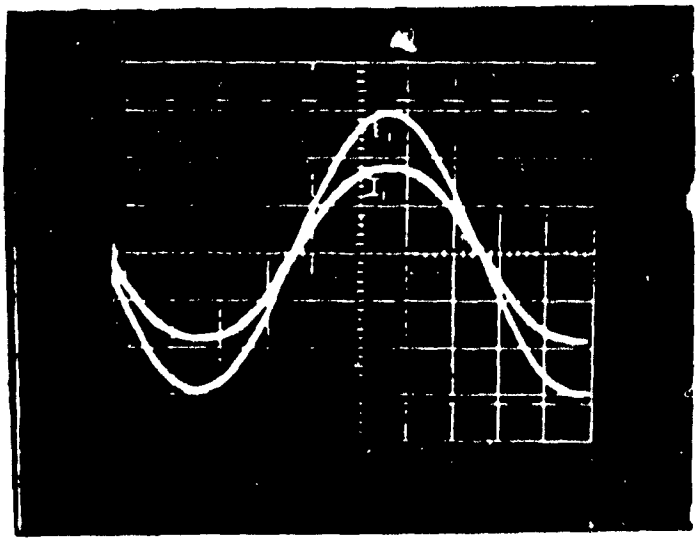


Fig. 3.14: Experimental ac input voltage (E_i) and current (I_i) at 50-percent rated load

10 Amps/div., 100V/div., 60 Hz

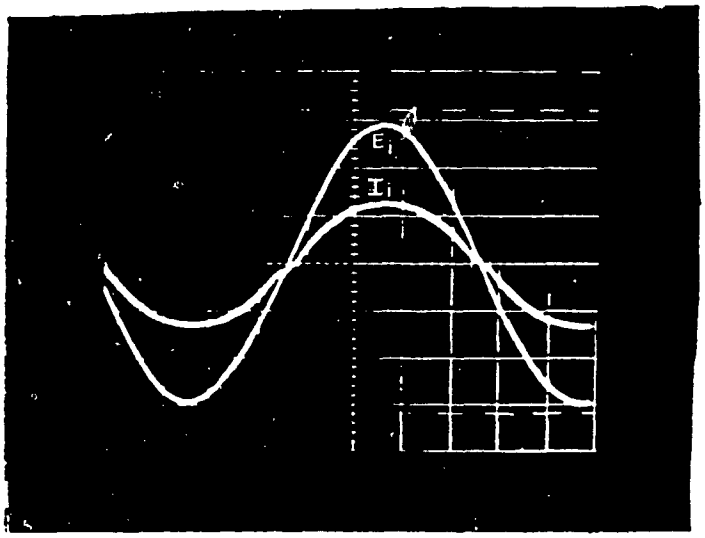


Fig. 3.15: Experimental ac input voltage (E_i) and current (I_i) at 33-percent rated load

10 Amps/div., 100V/div., 60 Hz

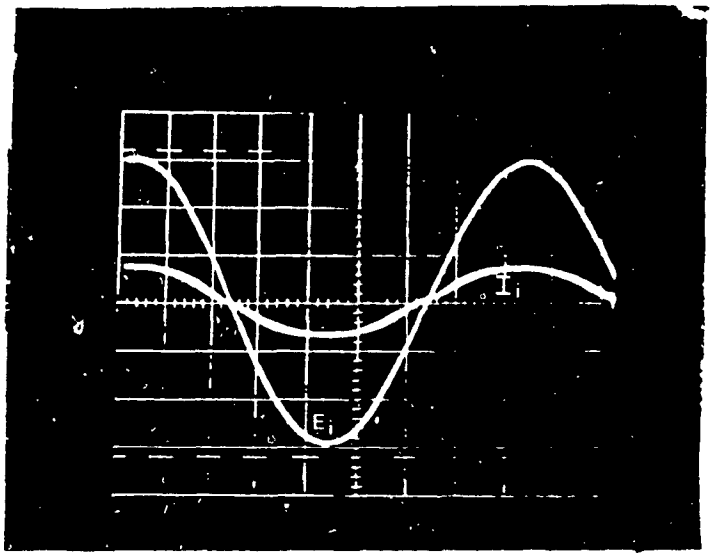


Fig. 3.16: Experimental ac input voltage (E_i) and current (I_i) at 14-percent rated load

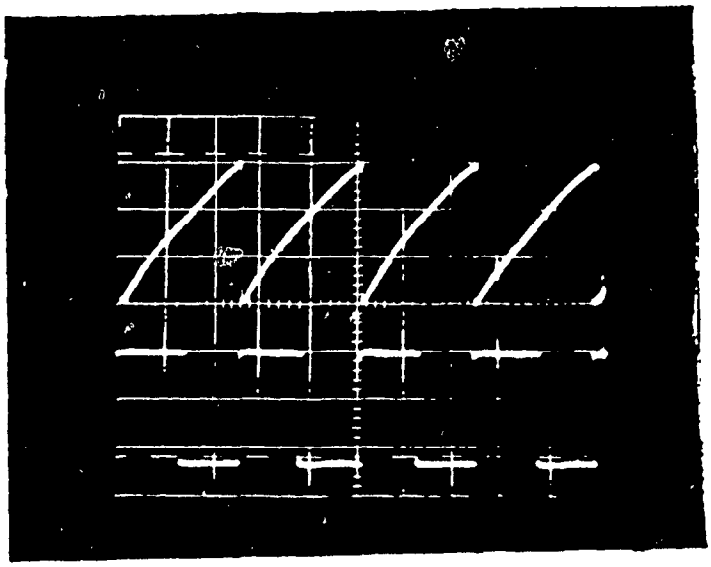


Fig. 3.17: Experimental high frequency (20 kHz) ramp waveform (upper trace) and respective oscillator output waveform (lower trace)

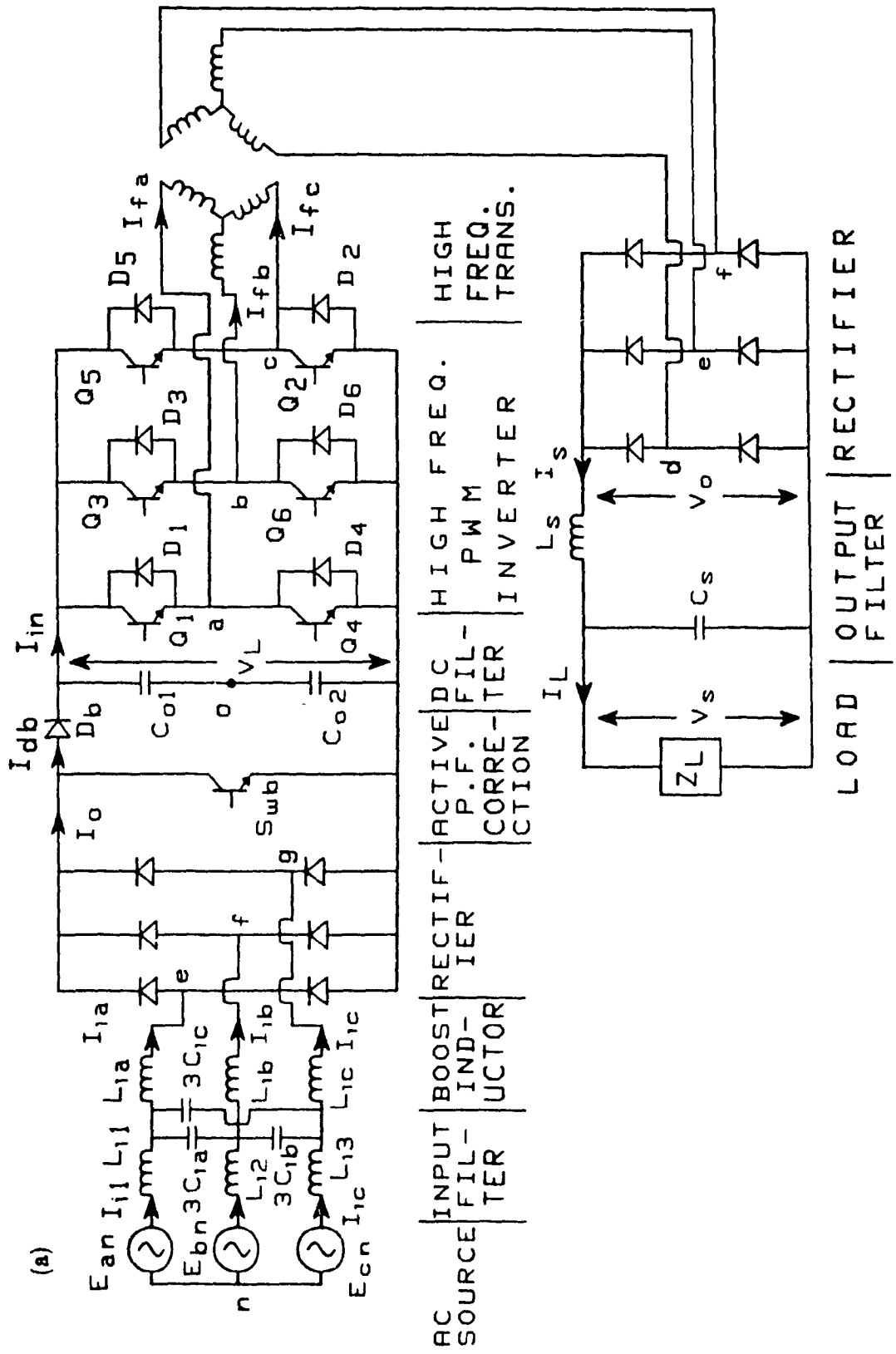
readily accept a wide range of L_i and f_{sw} values and respective changes in the switching frequencies can be easily realized through adjustments in ramp oscillator and ramp amplitude potentiometers.

3.2.7 Conclusions

In this section a novel active input current waveshaping method for single-phase fed active front-end rectifier topology has been proposed. This active topology exhibits practically ripple free sinusoidal ac input current. Furthermore, the proposed design allows the converter to operate at constant switching frequency. Finally, predicted features such as input current waveforms have been verified experimentally on a 5.5 kW laboratory unit. However the proposed active input current waveshaping method also has the disadvantage of requiring additional control logic components.

3.3 Proposed Three-Phase Fed Boost Active Filter Topology

Analysis and design of single-phase fed boost active filter topology has been discussed extensively in section 3.2. This section deals with the analysis and design of a novel three-phase fed boost active filter topology. The proposed three-phase ac-to-dc converter (Fig. 3.18) consists of two main power conversion stages. The first stage is a three-phase ac to dc rectifier consisting of an input filter, three boost inductors, a three-phase diode rectifier, a boost switch, and a dc link filter capacitor. The second stage can be assumed to be any type of load requiring a regulated or unregulated dc bus such as general purpose single-phase or three-phase inverter.


(a)
AC SOURCE
INPUT FIL-TER
BOOST IND-UCTOR
RECTIF-IER
ACTIVE P.F. CORRE-CTION
DC FIL-TER
HIGH FREQ. PWM INVERTER
HIGH FREQ. TRANS.
RECTIFIER
OUTPUT FILTER
LOAD
Ean
Ebn
Ecn
n
Ii1 Li1 Li1a
Ii1a
Ii1b Li1b 3Ci1a
Ii1c Li1c 3Ci1b
Li2
Li3 3Ci1c
e
f
g
Io
Idb
Db
Swb
Iin
Co1
Co2
o
VL
a
b
Q1
Q2
Q3
Q4
Q5
Q6
D1
D2
D3
D4
D5
D6
Ifa
Ifb
Ifc
c
d
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Is
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Cs
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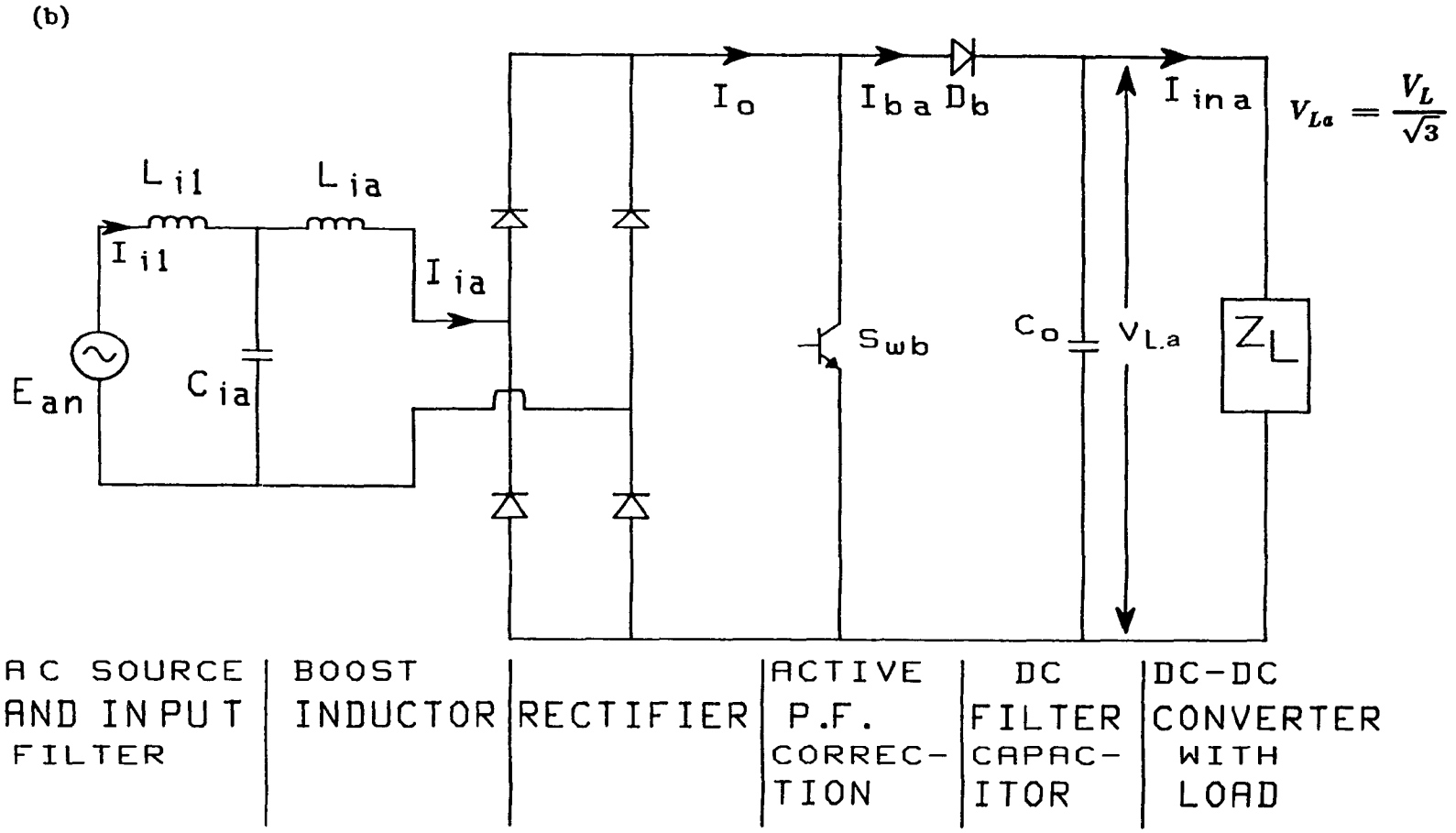
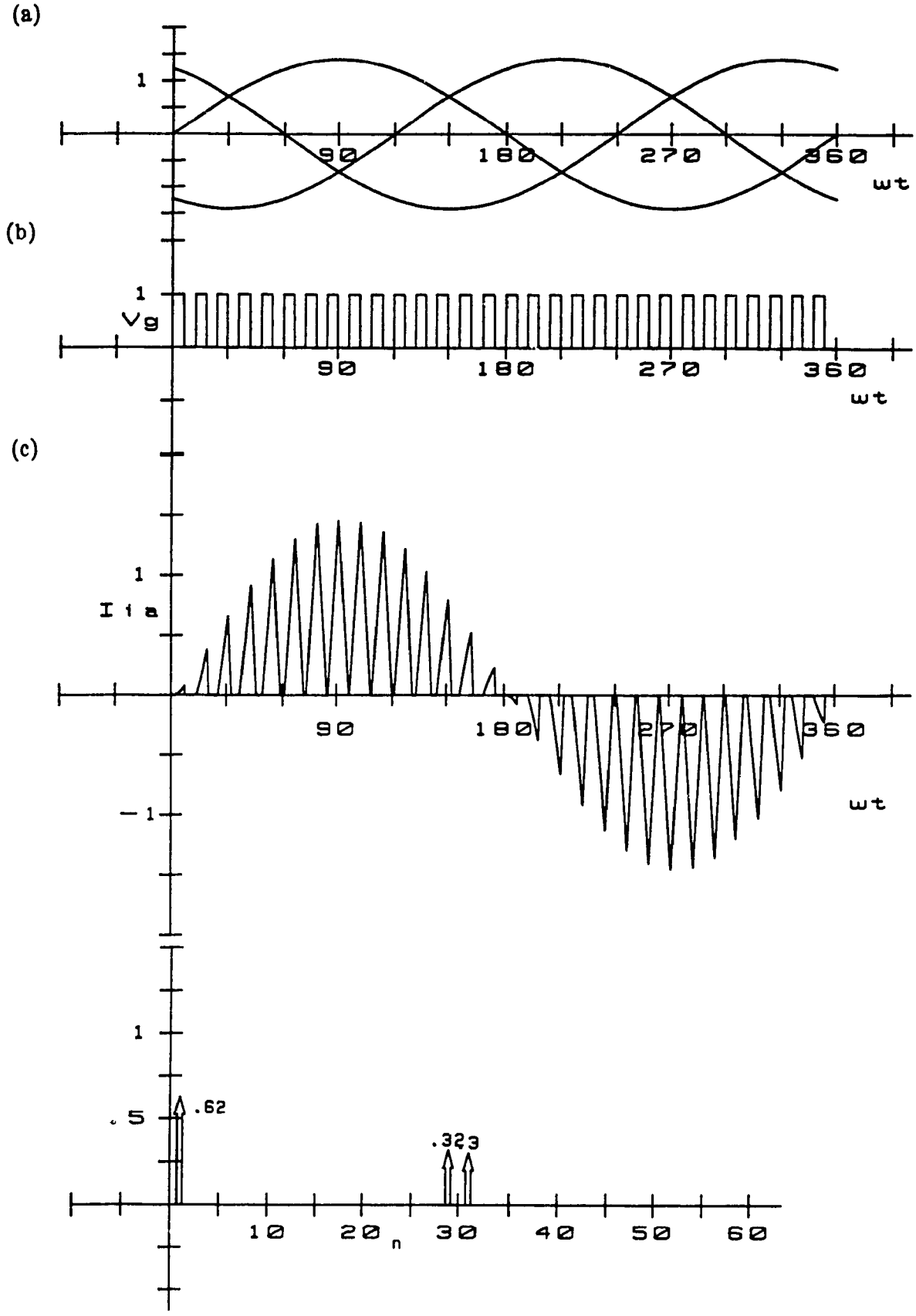


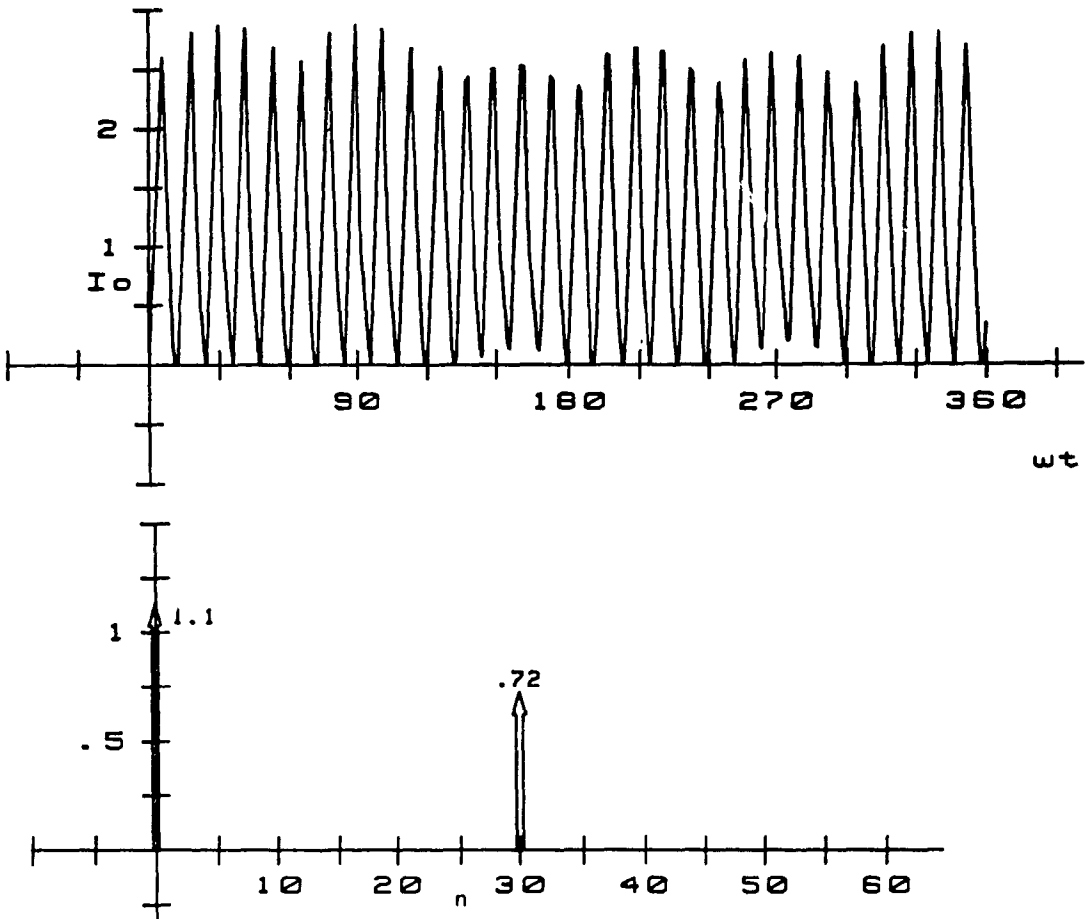
Fig. 3.18: Proposed three-phase ac-to-dc converter and its single-phase equivalent circuit.

3.3.1 Principles of Input Current Control and Waveshaping

The active waveshaping of the input current waveform is obtained through the use of the boost stage components L_{ia}, L_{ib}, L_{ic}, S_{wb}, and D_b, as shown in Fig. 3.18. The boost switch, S_{wb}, is turned on at constant frequency. The duty cycle of S_{wb}, is varied for load variation only and it is such that the input current is always discontinuous. During the 'on' period of the boost switch all three input ac phases become shorted through inductors L_{ia}, L_{ib}, and L_{ic}, the six rectifier diodes, and the boost switch. Consequently the three input currents I_{ia}, I_{ib}, and I_{ic} begin simultaneously to increase at a rate proportional to the instantaneous values of their respective phase voltages. Moreover the specific peak current values during each 'on' interval (Fig. 3.19(c)) are proportional to the average values of their input phase voltages during the same 'on' interval. Since each of these average voltage values varies sinusoidally, the input current peaks also vary sinusoidally (Fig. 3.19(c)). Moreover, since the current pulses always begin at zero, it means that their average values also vary sinusoidally. Consequently all three input ac currents consist of the fundamental (60 Hz) component and a band of unwanted high frequency components centered around the switching frequency of the boost switch (f_{sw}). Since the frequency, f_{sw}, can be in the order of several tens of kHz, filtering out of the unwanted input current harmonics becomes a relatively easy task. From Fig. 3.19 it is also seen that input power control (or output voltage regulation) can be achieved through pulse width modulation of the boost switch 'on' interval at a constant frequency (f_{sw}). Incidently, f_{sw} can be easily locked to the mains 60 Hz frequency to avoid 'beat frequency' effects in the input currents.


(a)
1
90
180
270
360
ωt
(b)
1
Vg
90
180
270
360
ωt
(c)
1
I i a
90
180
270
360
ωt
−1
1
.5
.62
.323
10
20
n
30
40
50
60

(d)


2
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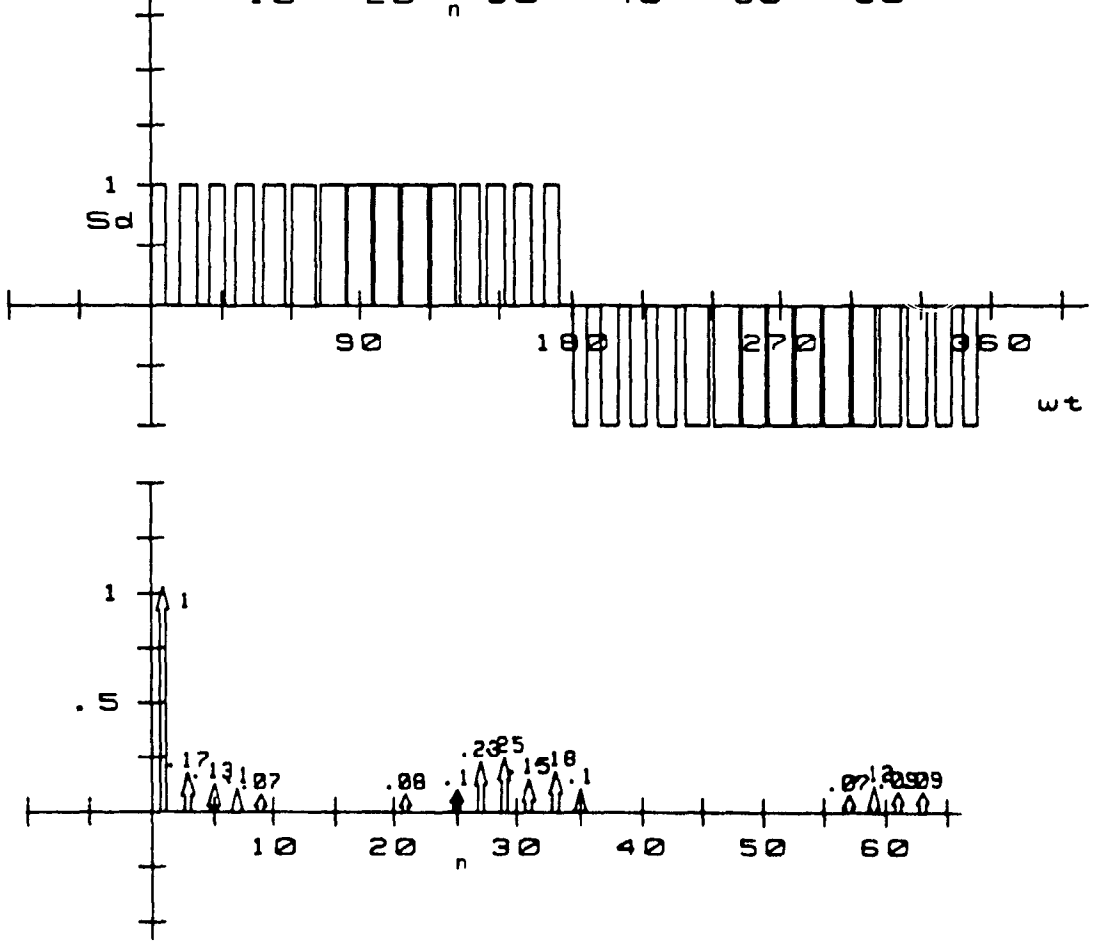
(e)


1
Sd
90
180
270
360
wt
1
.5
1
.17
.13
.1
.07
.08
.1
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.15
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10
20
30
40
50
60
n

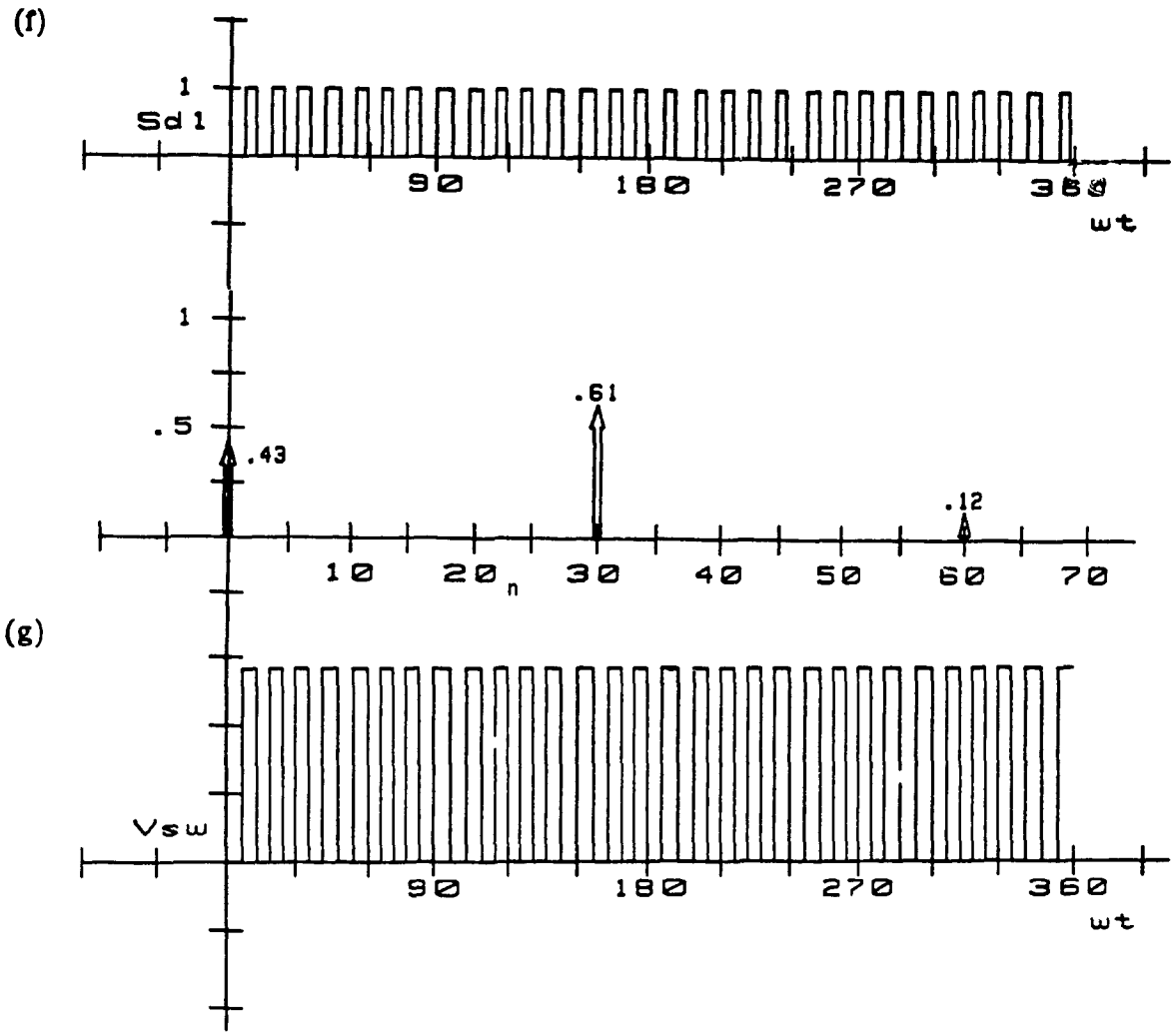


Fig. 3.19: Proposed three-phase ac-to-dc converter simulated waveforms.

(a) Three-phase ac source phase voltages.

(b) Boost switch (S_{wb}) gating signals.

(c) Rectifier input current (I_{ia}) and its spectrum..

(d) Rectifier output current (I_o) and its spectrum.

(e) Three-phase diode rectifier switching function (S_d) and its spectrum.

(f) Boost diode (D_b) switching function and its spectrum.

(g) Voltage across the boost switch (S_{wb}).

Finally, under the operating conditions described here the 'displacement input power factor' ($\cos(\phi_1)$) is unity before filtering. Consequently, the overall input power factor (before filtering) becomes equal to the 'harmonic input power factor' and it is given by

$$Power\ Factor = \left[\frac{\frac{I_{ia,1}}{\sqrt{2}}}{\sqrt{\sum_{n=1}^{\infty} \left(\frac{I_{ia,n}}{\sqrt{2}}\right)^2}} \right] \tag{3.19}$$

where $I_{ia,n}$ is the Fourier component of the n^{th} harmonic component of current I_{ia} and $\cos \phi_1$ is the displacement factor. It is noted that the current harmonics associated with this power factor can be suppressed by a relatively small input capacitor (C_{ia}) and inductor (L_{i1}) because of their high frequencies. Therefore the overall input power factor after filtering (i.e. at the ac source) is very close to unity.

3.3.2 Input Current

During the period when the boost switch (S_{wb}) is turned 'on', (Fig. 3.18) the equivalent single-phase circuit is as shown in Fig. 3.20(a). The input current (I_{ia}) rises at a rate determined by the input source voltage (E_{an}) and the inductor (L_{ia}). The current (I_{ia}) through the inductor during this period ($\beta \leq t \leq t_1$) is given by

$$E_{an} = \sqrt{2} * E * \sin(\omega t) = L_{ia} \frac{dI_{ia}}{dt}$$

Solving the above expression for I_{ia} and substituting the initial conditions, $I_{ia}(\omega t) = 0$, when $t=\beta$ yields

$$I_{ia}(\omega t) = \frac{\sqrt{2} * E}{\omega L_{ia}} \left[\cos(\omega \beta) \quad \cos(\omega t) \right] \tag{3.20}$$

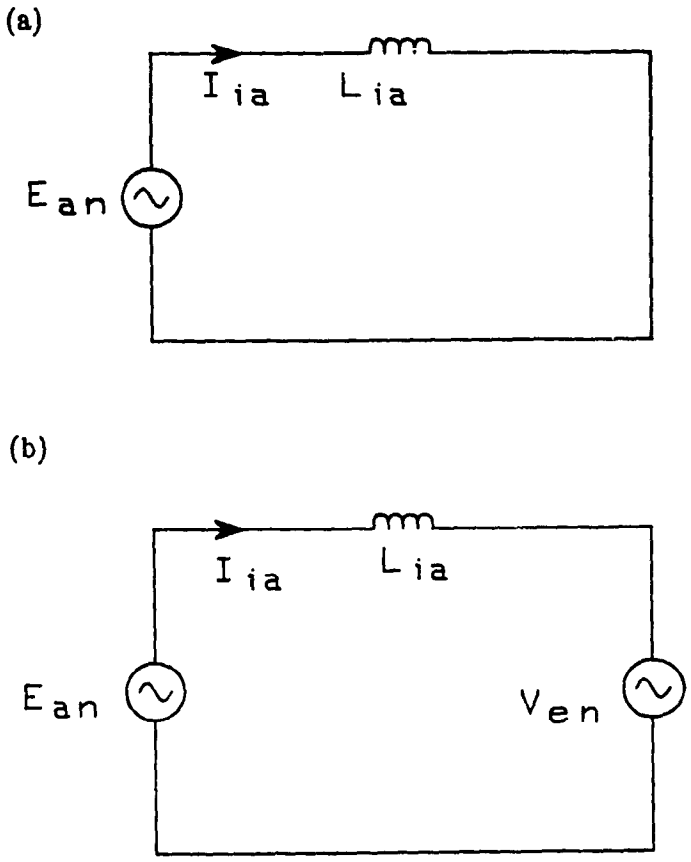


Fig. 3.20: Equivalent circuits during the boost switch (S_{wb}) operation
(a) Equivalent single-phase circuit when the boost switch is 'on'.
(b) Equivalent single-phase circuit when the boost switch is 'off'.

Where β is the angle at which the boost switch (S_{wb}) is turned on, with reference to the input voltage E_{an} and t_1 is the boost switch (S_{wb}) 'on' period. During the period when the boost switch (S_{wb}) is 'off' the current through the inductor decreases at a rate determined by the input voltage (E_{an}), output dc voltage (V_L), and the inductor (L_{ia}). The single phase equivalent circuit under this condition is shown in Fig. 3.20(b). When the boost switch is off, the boost converter theory indicates that the rectifier input phase voltage (V_{en}) of Fig. 3.20(b) given by

$$V_{en}(\omega t) = \frac{1}{1 - D} E_{an}(\omega t) \tag{3.21}$$

where D is the duty cycle of the boost switch (S_{wb}). The current (I_{ia}) through the inductor (L_{ia}) during the period when the boost switch is off, $t_1 \leq t \leq T_{sw}$, is given by

$$\sqrt{2} * E * \sin(\omega t) = L_{ia} \frac{dI_{ia}}{dt} + V_{en} \tag{3.22}$$

Solving Eqn. (3.22) for I_{ia} and substituting the initial condition $I_{ia}(\omega t) = I_{ia}(\omega t_1)$ when $t = t_1$ yields

$$I_{ia}(\omega t) = \frac{\sqrt{2} * E}{\omega L_{ia}} \left[\cos(\omega\beta) - \cos(\omega t)\right] - \frac{V_{en}}{L_{ia}}(t - t_1) \tag{3.23}$$

For the designer the worst operating point is switching on the boost switch (S_{wb}) at the peak input voltage ($E_{an(peak)}$). Under this condition the current through the inductor (L_{ia}) increases at its maximum rate and reaches its maximum value at the end of t_1. Also, under this condition the time required for the current (I_{ia}) to fall to zero is maximum. Therefore, the frequency of the boost switch (S_{wb}) is a function of the ac input voltage (E_{an}) and the output dc voltage (V_L). Substituting $\beta = 90^\circ$ and $t = (90^\circ + t)$ in

Eqn. (3.20) yields

$$I_{ia}(\omega t) = \frac{\sqrt{2} * E}{\omega L_{ia}} \sin(\omega t) \tag{3.24}$$

In practice the boost switch switching frequency, f_{sw}, is of the order of 20-40 kHz and the boost switch 'on' period (t_1) is small in comparison to the input source voltage (E_{an}) time period. For small values of ωt, $\sin\omega t$ is approximately equal to ωt. Consequently Eqn. (3.24) becomes

$$I_{ia}(\omega t) = \frac{\sqrt{2} * E}{L_{ia}} t \; ; \qquad 0 \leq t \leq t_1 \tag{3.25}$$

At time t_1 the inductor current (I_{ia}) reaches its maximum value and the boost switch (S_{wb}) is turned off by its appropriate control signal. Substituting $\beta = 90^o$ and t = (90^o + t) in Eqn. (3.23) yields

$$I_{ia}(\omega t) = \frac{\sqrt{2} * E}{\omega L_{ia}} \sin(\omega t) - \frac{V_{en}}{L_{ia}} (t - t_1) \tag{3.26}$$

and substituting ωt for $\sin(\omega t)$, the above equation becomes

$$I_{ia}(\omega t) = \frac{\sqrt{2} * E}{L_{ia}} t - \frac{V_{en}}{L_{ia}} (t - t_1) \; ; \qquad t_1 \leq t \leq T_{sw} \tag{3.27}$$

The current $I_{ia}(\omega t) = 0$ at time t=t_2. Substituting this condition in the above equation yields

$$\frac{t_2}{t_1} = \frac{V_{en}}{V_{en} - \sqrt{2} * E} \tag{3.28}$$

Therefore, the minimum dc bus voltage, $V_{L(min)}$ is given by

$$V_{L(min)} = V_{en} * \sqrt{3} \tag{3.29}$$

If the dc bus voltage(V_L) is less than the above value then the rate at which the inductor current (I_{ia}) falls to zero decreases. Consequently, the boost switch frequency has to be decreased to a value at which the inductor current

(I_{ia}) becomes zero before turning on the boost switch (S_{wb}) again. In other words the the duty cycle of the boost switch must be decreased for a given boost switch switching frequency (f_{sw}). Therefore the switching frequency of the boost switch (S_{wb}) is a function of the dc bus voltage (V_L). The variation of the minimum dc bus voltage (V_L) with duty cycle of the boost switch is shown in Fig. 3.21.

From the description presented above, the simulated inductor current (I_{ia}) and its spectrum, the diode rectifier switching function ($S_d(\omega t)$) and its spectrum, and the diode (D_b) switching function ($S_{d1}(\omega t)$) and its spectrum, are derived and shown in Fig. 3.19. Evaluation of Fig. 3.19 clearly shows the elimination of the low frequency components from the rectifier input and output currents (I_{ia}, I_o).

The input current (I_{ia}) can be expressed in terms of the Fourier series as

$$I_{ia}(\omega t) = \sum_{n=1,3}^{\infty} \left[A_n \cos(n\omega t) + B_n \sin(n\omega t) \right]$$

where A_n and B_n are the Fourier coefficients of the current I_{ia}. The above expression can be further simplified to

$$I_{ia}(\omega t) = \sum_{n=1,3}^{\infty} C_n \sin(n\omega t + \theta_n) \qquad (3.30)$$

where

$$C_n = \sqrt{A_n^2 + B_n^2} \quad \text{and} \quad \theta_n = \tan^{-1}\frac{A_n}{B_n}$$

The values of C_n and θ_n depend upon the value of the operating frequency of the boost switch for a given inductor value (L_{ia}). The variation of the input power factor of the proposed converter (without input filter) with a boost switch duty cycle is shown in Fig. 3.22. The low input power factor is due to

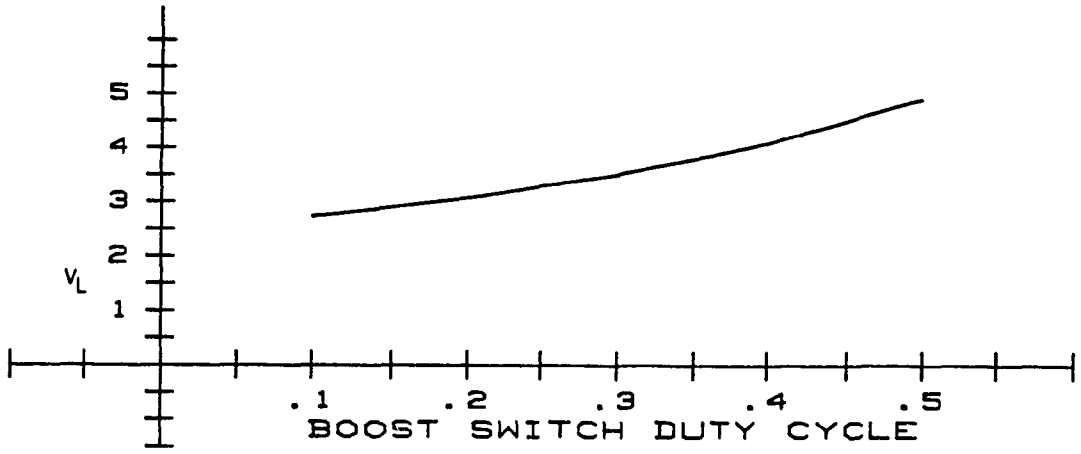


Fig. 3.21: Variation of minimum dc output voltage (V_L) with the boost switch duty cycle.

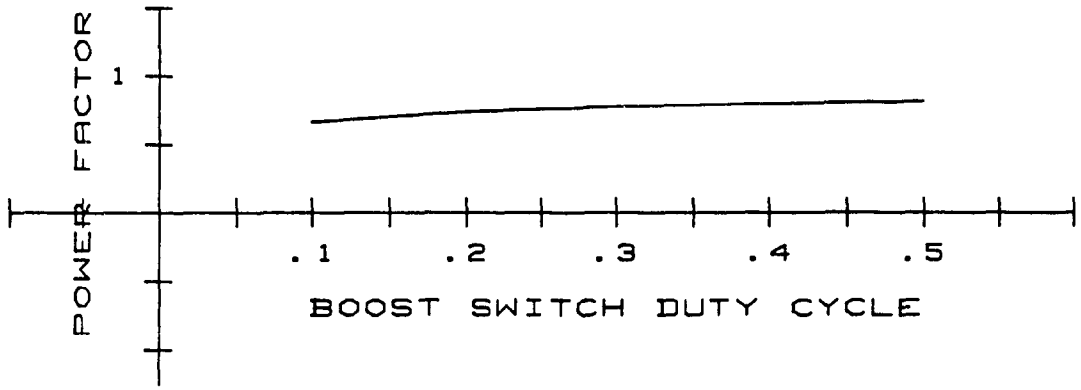


Fig. 3.22: Variation of power factor (without input filter) with boost switch duty cycle.

the presence of the high frequency harmonic components in the current (i_{ia}). These high frequency current harmonics can be filtered easily with a small input filter thus providing a nearly unity input power factor. The peak inductor current (I_{ia}) depends upon the value of the inductor (L_{ia}), the operating frequency, and the duty cycle of the boost switch.

3.3.3 Front-end Section

In this section the proposed front-end boost section is analyzed under steady-state conditions. The expressions derived are subsequently used to obtain the information necessary for proper converter design. The converter is analyzed under the following assumptions:

(i) all power switching devices are ideal and the forward drop and reverse leakage currents of the diodes are negligible;

(ii) filter components are ideal;

(iii) the load voltage is ripple free.

Moreover, the rated input rms phase voltage, E, and rated output power, P_o, are assumed to be

$$E = 1.0 \ pu \ V$$
$$P_o = 1.0 \ pu \ W$$

By further assuming that the ac source angular frequency is 1.0 pu, from Fig. 3.19(c), the value of the peak current $I_{ia\,(peak)}$ for $L_{ia} = 0.1$ pu is given by

$$I_{ia\,(peak)} = \frac{\sqrt{2} * E}{L_{ia}} * \frac{T_{su}}{2} = 1.48 \quad pu \tag{3.31}$$

Where T_{su} is the boost switch time period. The amplitude of the fundamen-

tal component of current $I_{ia,1}$ is 0.62. The peak value of current I_{ia} (Eqn. 3.31) depends upon the values of L_{ia}, $E_{an(peak)}$, and T_{sw}. From Fig. 3.19(c) the ratio of current $I_{ia,1}$ to $I_{ia(peak)}$ is 0.418. Therefore the general expression for the current $I_{ia,1}$ is given by

$$I_{ia,1} = I_{ia(peak)} * 0.418$$

Substituting Eqn. (3.31) the above equation becomes

$$I_{ia,1} = \frac{\sqrt{2} * E}{L_{ia}} * \frac{T_{sw}}{2} * 0.418 \tag{3.32}$$

From Eqn. (3.32) the maximum value of the inductor L_{ia} for any boost switch switching frequency can be calculated.

3.3.4 Output filter

The rectifier output current, I_o, in Fig. 3.18 is given by

$$I_o(\omega t) = \left[\sum_{k=0}^{2} I_{ia}(\omega t - \frac{2k\pi}{3}) * S_d(\omega t - \frac{2k\pi}{3}) \right] \tag{3.33}$$

where $S_d(\omega t)$ is the diode rectifier switching function shown in Fig. 3.19(e) and it can be expressed in Fourier series as

$$S_d(\omega t) = \sum_{n=1,3}^{\infty} \left[D_n \cos(n\omega t) + E_n \sin(n\omega t) \right]$$

$$S_d(\omega t) = \sum_{n=1,3}^{\infty} F_n \sin(n\omega t + \varsigma_n) \tag{3.34}$$

where

$$F_n = \sqrt{D_n{}^2 + E_n{}^2} \quad and \quad \varsigma_n = \tan^{-1}\frac{D_n}{E_n}$$

Substituting Eqns. (3.30) and (3.34) into Eqn. (3.33) yields the diode rectifier output current

$$I_o(\omega t) = \sum_{k=0}^{2}\left[\sum_{n=1,3}^{\infty} C_n \sin(n(\omega t - \frac{2k\pi}{3}) + \theta_n) * \sum_{m=1,3}^{\infty} F_m \sin(m(\omega t - \frac{2k\pi}{3}) + \varsigma_m)\right]$$

$$= \sum_{k=0}^{2}\left[\left(C_1\sin(\omega t - \frac{2k\pi}{3} + \theta_1) + C_3\sin(3\omega t - 2k\pi + \theta_3) + \ldots.\right)\right.$$

$$\left. * \left(F_1\sin(\omega t - \frac{2k\pi}{3} + \varsigma_1) + F_3\sin(3\omega t - 2k\pi + \varsigma_3) + \ldots..\right) ..\right] \quad (3.35)$$

Since the harmonic components of $I_o(\omega t)$ are all multiples of six (i.e. 6,12,18...) and since the boost switch switching frequency, f_{sw}, is also assumed to be a multiple of six Eqn. (3.35) becomes

$$I_o(\omega t) = 3\left[\frac{C_1F_1}{2}\cos(\theta_1-\varsigma_1) + \ldots. + \frac{C_{f_{sw}-1}F_{f_{sw}-1}}{2}\cos(\theta_{f_{sw}-1}-\varsigma_{f_{sw}-1}) + \ldots..\right]$$

$$- \ldots.. - \left(\frac{3C_1F_{f_{sw}-1}}{2}\cos(f_{sw}\omega t + \theta_1 - \varsigma_{f_{sw}-1})\right.$$

$$\left. - \frac{3C_1F_{f_{sw}+1}}{2}\cos(f_{sw}\omega t + \theta_1 - \varsigma_{f_{sw}+1}) ..\right)$$

$$- \left(\frac{3F_1C_{f_{sw}-1}}{2}\cos(f_{sw}\omega t - \varsigma_1 + \theta_{f_{sw}-1})\right.$$

$$\left. - \frac{3F_1C_{f_{sw}+1}}{2}\cos(f_{sw}\omega t - \varsigma_1 + \theta_{f_{sw}+1}) + \ldots.. .\right) \quad (3.36)$$

A close examination of Eqn. (3.36) reveals that the dominant harmonic component of the rectifier output current (I_o) is at f_{sw}. If the boost switch switching frequency is not a multiple of six then the dominant frequency of the rectifier output current (I_o) is a multiple of six around f_{sw} since the harmonics of frequency f_{sw} cancel each other on the dc side. Evaluation of Fig. 3.19(c) shows that the dominant harmonic component of the current (I_{ia}) is at f_{sw} -1, where f_{sw} is the boost switch switching frequency. Furthermore,

the switching function (S_{d1}) of the diode, D_b, shown in Fig. 3.19(f) can be expressed by the Fourier series

$$S_{d1}(\omega t) = G_0 + \sum_{n=1}^{\infty} \left[H_n \cos(n\omega t) + K_n \sin(n\omega t) \right]$$

$$= G_0 + \sum_{n=1}^{\infty} L_n \sin(n\omega t + \eta_n) \qquad (3.37)$$

where

$$L_n = \sqrt{H_n{}^2 + K_n{}^2} \quad and \quad \eta_n = \tan^{-1}\frac{H_n}{K_n}$$

The dominant harmonic component of the diode (D_b) switching function (S_{d1}) is f_{sw}. Therefore the dominant harmonic component of the dc current (I_{db}) before dc filter capacitor (C_o) is given by

$$I_{db,f_{sw}(peak)} = L_{f_{sw}} * I_o(0) + G_o(0) * F_{f_{sw}} \qquad (3.38)$$

The converter output current ($I_{db}(\omega t)$) consists of a modulated train of pulses and consequently some form of filtering is necessary to separate the dc component from the undesired harmonic components. Furthermore, the amplitude of the $f_{sw}{}^{th}$ order voltage harmonic component across the output filter capacitor (C_o) is given by

$$V_{L,f_{sw}} = \frac{I_{db,f_{sw}(peak)}}{f_{sw}\omega C_o} \qquad (3.39)$$

where $I_{db,f_{sw}(peak)}$ is the amplitude of the $f_{sw}{}^{th}$ harmonic component of current I_{db}. Moreover, by assuming that the ripple voltage across the filter capacitor, C_o, is less than 0.01-percent (i.e. less than 30mV at the load terminals at V_L = 300V) the output voltage (V_L) ripple can be defined by

$$Ripple\ \% = \frac{100\, V_{d,f_{sw}(rms)}}{V_{L,0}} \qquad (3.40)$$

Substituting Eqn. (3.40) into Eqn. (3.39), the value of the output filter capacitor (C_o) is given by

$$C_o = \frac{I_{b\,2.f_{sw}(peak)} * 100}{\sqrt{2} * V_{L,0} * (Ripple\ \%) * f_{sw} * \omega} \tag{3.41}$$

Substituting Eqns. (3.21) and (3.29) into Eqn. (3.41) yields

$$C_o = \frac{I_{db\,.f_{sw}(peak)} * 100 * (1-D)}{\sqrt{2} * (Ripple\ \%) * f_{sw} * \omega * \sqrt{2} * E * \sqrt{3}} \tag{3.42}$$

3.3.5 Input Filter

In most specifications for power supplies the total harmonic distortion (THD) content of the input line current ($I_{i\,1}$) is $\leq$5-percent. Also it can be shown that if the amplitude of the dominant harmonic component of $I_{i\,1}$ is reduced to 3-percent of the amplitude of the respective fundamental then THD $\leq$5-percent can be ensured. Therefore for the PWM method shown in Fig. 3.19 the order of the dominant harmonic component of the inductor current (I_{ia}) is f_{sw} - 1. The harmonic equivalent circuit per phase for the input filter is shown in Fig. 3.23. The filter inductor current harmonic components, $I_{i\,1,n}$, shown in Fig. 3.23 are given by

$$I_{i\,1,n} = \frac{X_{C_{ia},1} I_{ia\,.n}}{n^2 X_{L_{i\,1,1}} - X_{C_{ia},1}} \tag{3.43}$$

where

- n is the order of the harmonic;
- $X_{C_{ia},1}$ is the filter capacitor (C_{ia}) reactance at fundamental frequency;
- $X_{L_{i\,1,1}}$ is the filter inductor ($L_{i\,1}$) reactance at fundamental frequency.

Equation (3.43) can be further simplified as

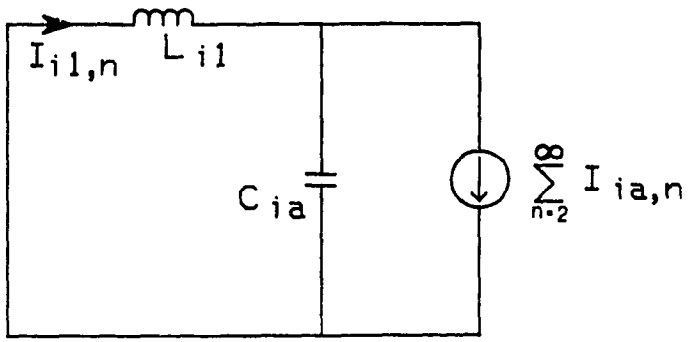


Fig. 3.23: Single-phase equivalent circuit for input filter design.

$$\frac{X_{L_{i1,1}}}{X_{C_{ia,1}}} = \frac{1}{n^2}\left[\frac{I_{ia,n}}{I_{i1,n}} + 1\right] \tag{3.44}$$

The dominant harmonic component of the current I_{ia} is at $f_{sw} - 1$ therefore Eqn. (3.44) reduces to

$$\frac{X_{L_{i1,1}}}{X_{C_{ia,1}}} = \frac{1}{(f_{sw} - 1)^2}\left[\frac{I_{ia,f_{sw}-1}}{I_{i1,f_{sw}-1}} + 1\right] \tag{3.45}$$

Evaluation of Eqn. (3.45) reveals that size of the filter components is a function of the boost switch switching frequency (f_{sw}). The size of the filter components becomes smaller and smaller for higher switching frequencies (f_{sw}). Consequently all of the harmonics of the input current (I_{i1}) become smaller and smaller and the input power factor is nearly unity. However the proposed method also has the disadvantages of increasing the switching stresses of the switching devices.

3.3.6 Component Ratings

From the aforementioned assumptions and derived analytical expressions the voltage and current ratings of the various system components are as follows.

Inductor L_{ia}

Value of L_{ia} :0.1 pu

Rms L_{ia} current $= \sqrt{\sum_{n=1}^{\infty}\left(\frac{I_{ia\ n}}{\sqrt{2}}\right)^2}$: 0.59 pu

Peak L_{ia} current $= \sqrt{\sum_{n=1}^{\infty} I_{ia\ n}{}^2}$: 2.01 pu

Rectifier Diode

Average current : 0.137 pu

Rms current : 0.42 pu

Peak current : 2.01 pu

Boost Switch S_{wb}

Peak forward voltage : 4.89 pu

Peak current : 1.06 pu

Average current : 0.205 pu

Boost Diode D_b

Peak reverse voltage : 4.898 pu

Peak current : 1.06 pu

Average current : 0.205 pu

DC Filter Capacitor C_o

Value : Eqn. (3.42)

Peak voltage : 4.898 pu

The conventional three-phase ac-to-dc converter (Fig. 3.3) consists of three single-phase ac-to-dc converters with suitable input and output connections. Therefore, the component ratings derived in section 3.2.4 are valid in this case also. However in three-phase converter (Fig. 3.3) each individual converter unit delivers 0.33 pu output power while delivering total converter unit 1.0 pu output power (P_r). Therefore all the current ratings derived in section 3.2.4 are to be reduced to $\frac{1}{3}$ of their values (assuming the dc bus voltage is 1.556 pu).

Comparing the boost switch ratings of the proposed three-phase active

filter topology (Fig. 3.18) with $\frac{1}{3}$ of the current ratings found in section 3.2.4 clearly shows that the proposed three-phase ac-to-dc active topology (Fig. 3.18) has the disadvantages of higher peak current and peak forward voltage as compared to the conventional three-phase ac-to-dc active filter topology (Fig. 3.3).

3.3.7 Design Example

To illustrate the significance and facilitate the understanding of the theoretical results obtained in preceding sections, the following design example is given. The front-end rectifier topology has the following specifications.

- The ac source rms phase voltage (E) = 50V = 1.0 pu
- The supply frequency = 60Hz. = 1.0 pu
- The rated output power = 1.0 kW. = 1.0 pu
- The boost switch switching frequency (f_{sw}) = 24 kHz. = 400 pu

From these values

$$1 \text{ pu current} = \frac{1000}{3 * 50} = 6.66 \text{ A}$$

$$1 \text{ pu impedance} = \frac{50}{6.66} = 7.50\Omega$$

$$1 \text{ pu angular frequency} = 2\pi f = 377 \text{ rad/sec.}$$

$$1 \text{ pu inductance} = \frac{7.50}{377} = 0.023\text{H}$$

$$1 \text{ pu capacitance} = \frac{1}{377 * 7.5} = 353.66\ \mu\text{F.}$$

Equation (3.32) is used to find the maximum value of the inductor (L_{ia}) required at 24 kHz (400 pu) switching frequency to deliver 1.0 pu (rms)

current is given by

$$L_{ia} = \frac{\sqrt{2}*50}{\sqrt{2}*6.66} * \frac{1}{24000} * \frac{0.418}{2} = 65.37\mu H$$

Using Eqns. (3.21) and (3.29) the following values are computed:

- Duty cycle of the boost switch $S_{wb} = 0.5$
- Rectifier input phase voltage $V_{en} = \frac{50*\sqrt{2}}{1-.5} = 141.4$ Volts.
- Minimum output voltage $V_L = \sqrt{3}*V_{en} = 141.4*\sqrt{3} = 244.91$ V.

Choosing an input filter capacitor ($C_{ia,1}$) value of 0.1 pu and using the Eqn. (3.44) the value of the input filter inductor (L_{i1}) value is obtained.

The dominant ripple frequency = 24000 - 1 = 23.99 kHz = 399.98 pu

and

$$L_{i1,1} = \frac{1}{0.1*(399.98)^2}\left[\frac{0.7}{0.03} + 1\right] = 0.00152 \ \ pu \ = 30.41\mu H$$

$$\textit{Output filter capacitor } (C_o) \textit{ (Eqn. (4.24))} = \frac{0.7*100*0.5}{\sqrt{2}*0.01*400*1*\sqrt{2}*\sqrt{3}}$$

$$= 2.53 \ \ pu \ = 893.63\mu F$$

3.3.8 Experimental Results

To verify the selected predicted results a 1.0 kVA experimental converter has been implemented using power MOSFET switch with the following circuit parameters:

- The operating frequency of the boost switch $f_{sw} = 25.64$ kHz.;
- The input ac source rms phase voltage (E) = 50V;

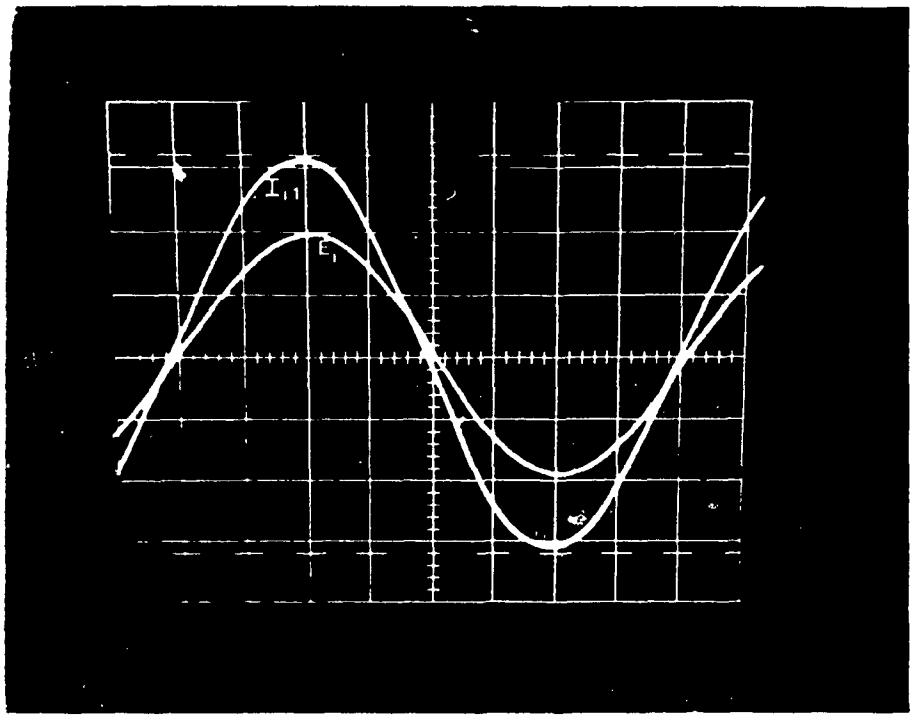
- The rectifier ac input rms current I_{ia} = 11.4 Amps.;
- The duty cycle of the boost switch S_{wb} = 0.5;
- The inductor (L_{ia}) = 45 μH;
- The dc bus voltage (V_L) = 300 V;
- The rectifier output dc current (I_o) = 4.0 Amps.;

Experimental waveforms obtained with this prototype are shown in Fig. 3.24. In particular, evaluation of the input current (I_{i1}) shown in Fig. 3.24(a) is in phase with the ac voltage as predicted. Furthermore, the inductor current (I_{ia}), rectifier output current (I_o), and the voltage across the switch are in close agreement with the simulated results shown in Figs. 3.19(c), 3.19(d), and 3.19(g) respectively. However, with the conventional method (Fig. 3.3) the rated rectifier input rms current required to deliver 1200 Watts is $(\frac{1200}{3 * 50})$ 8.0 Amps.. Moreover, with the proposed method the rectifier input ac rms current is 11.4 Amps.. Hence as predicted the rectifier has the disadvantage of increasing the current stresses of the switching devices in comparison with the conventional three-phase ac to dc converter shown in Fig. 3.3.

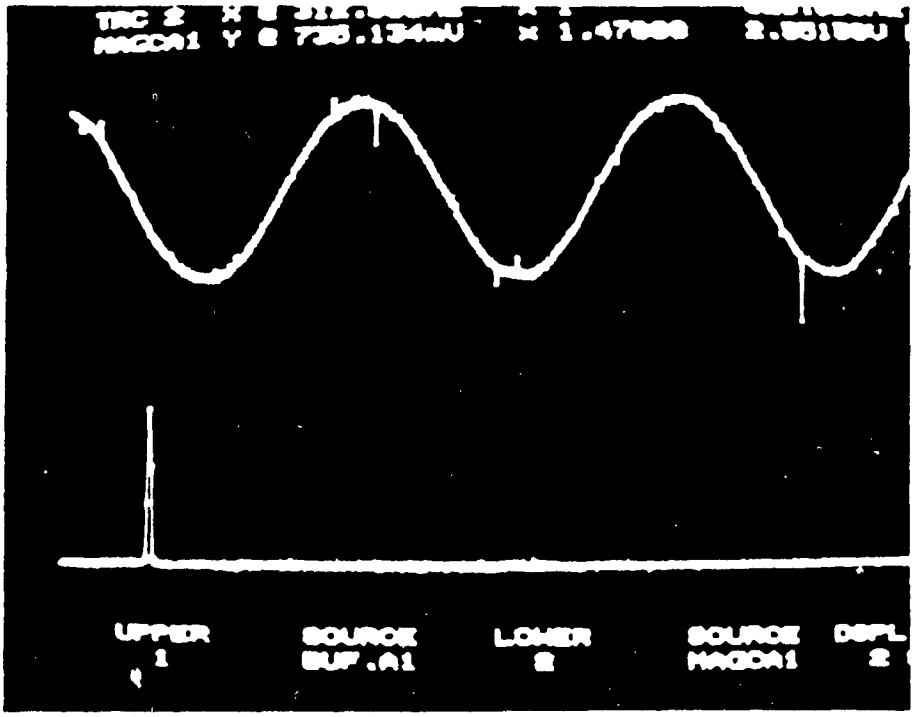
3.3.9 Conclusions

In this section a novel three-phase fed boost active filter topology has been proposed. This topology draws high quality input current waveforms from the ac source. The front-end bridge rectifier operation has been analyzed in detail and the steady state performance is obtained. Performance evaluation and relevant design data have been provided for implementation of the front-end rectifier. Detailed input and output current analysis has shown

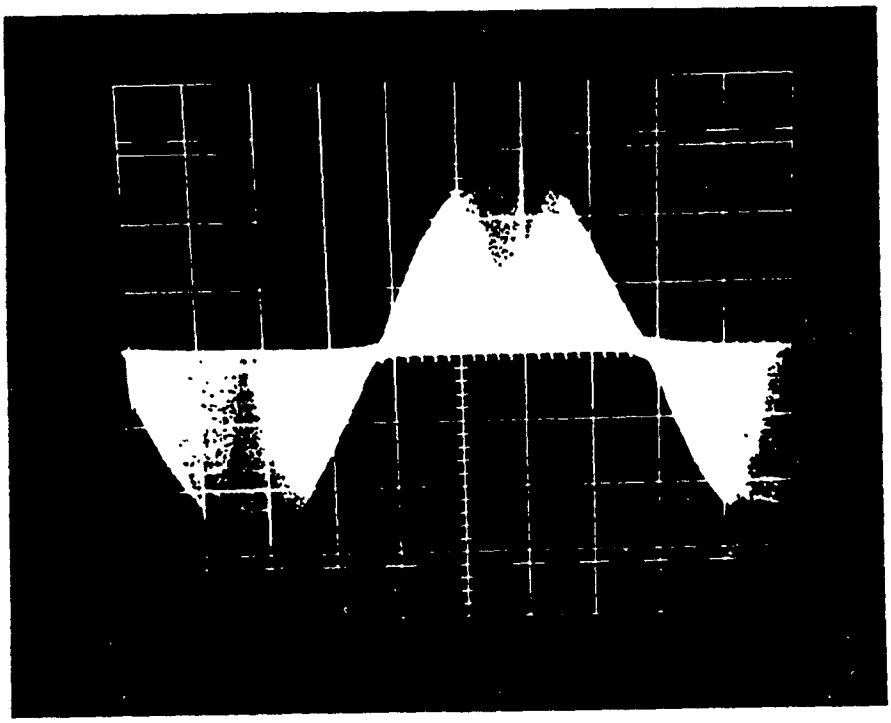
(a)



Time : 2 ms/div.
Amp. : 100 V/div.
5 A/div.

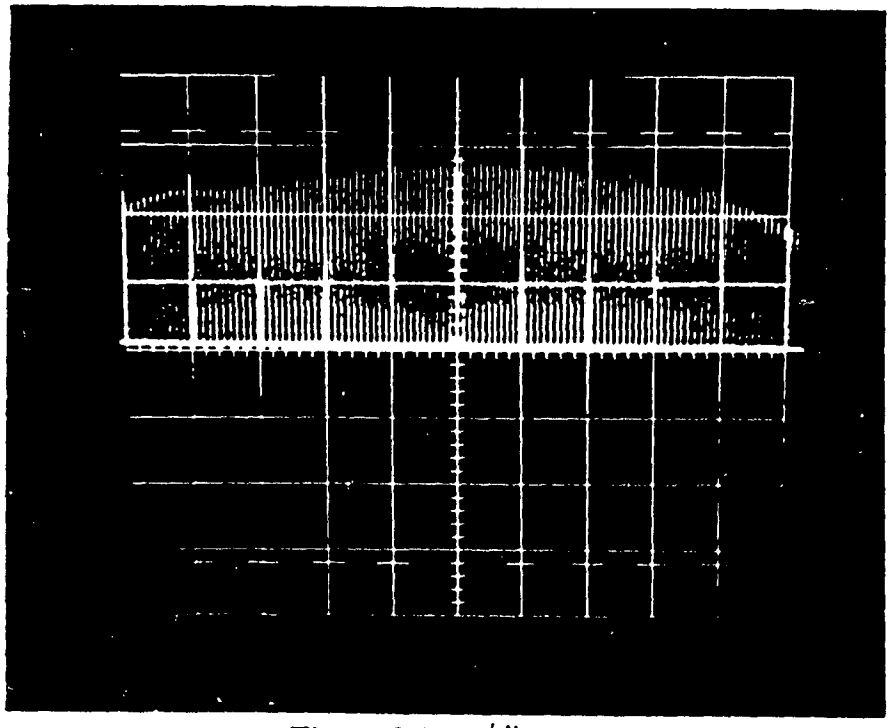


(b)



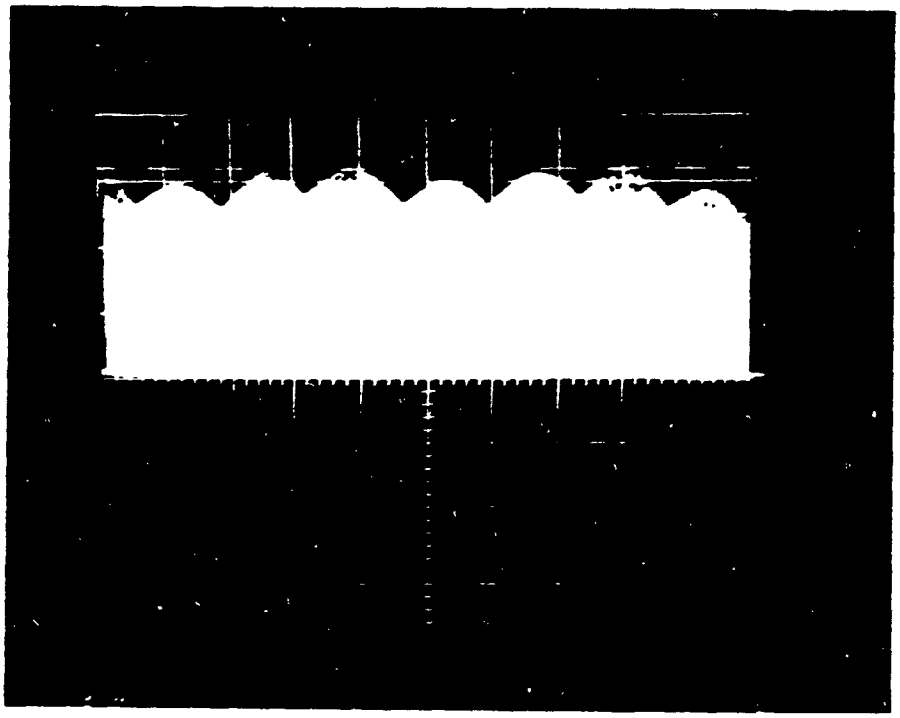
Time : 2 ms/div.
Amp. : 10 A/div.

(c)



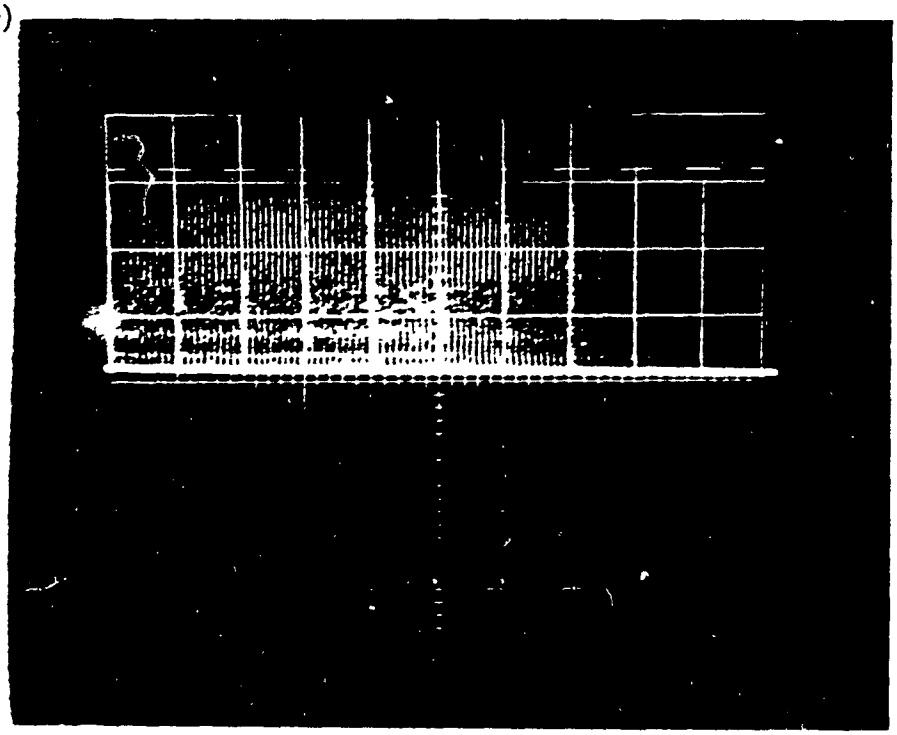
Time : 0.4 ms/div.
Amp. : 10 A/div.

(d)



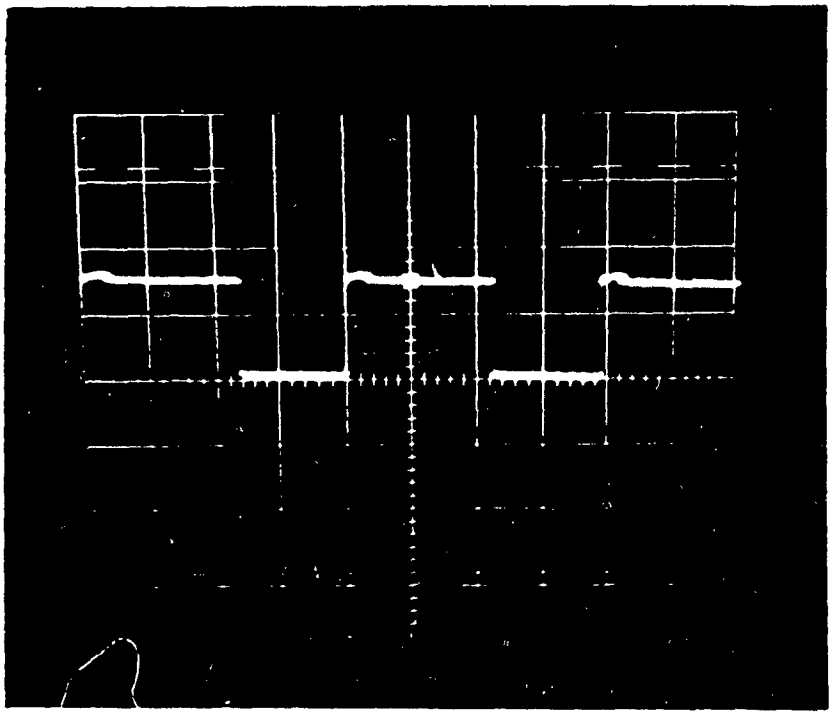
Time : 2 ms/div.
Amp. : 10 A/div.

(e)



Time : 0.4 ms/div.
Amp. : 10 A/div.

(f)



Time : 10 μs/div.
Amp. : 100 V/div.

Fig. 3.24: Experimental waveforms of the proposed three-phase ac-to-dc SMR converter.

(a) Input ac phase voltage, Input current (I_{i1}) and its frequency spectrum.

(b) Rectifier input current (I_{ia}).

(c) Expanded version of (b).

(d) Rectifier output current (I_o).

(e) Expanded version of (d).

(f) Voltage across the boost switch at reduced input voltage.

that the proposed converter yields unity input power factor, eliminates the synchronization logic requirement, and reduces the component count considerably in comparison with the conventional converter. However the proposed front-end active filter topology has the disadvantage of increasing the switching stresses of the semiconductor devices. Finally, key predicted results such as input/output waveforms and associated harmonic spectra have been verified experimentally on laboratory prototype units.

3.4 Proposed Three-Phase Fed Synchronous Active Filter Topology

The boost active filter topology (Fig. 3.18) discussed in section 3.3 has the disadvantage of increasing the current and voltage stresses of the semiconductor components. The synchronous active filter topology discussed in this section retains all the advantages of boost active filter topology and eliminates its disadvantage. As mentioned earlier, a different but equally effective method of 'constructing' a sinusoidal ac input current waveform is through the application of synchronous link techniques. The proposed three-phase fed active synchronous rectifier topology (Fig. 3.25) consists of a synchronous PWM rectifier that employs the harmonic injection sinusoidal PWM (HISPWM) control method [31,32] for elimination of the input line current unwanted harmonic components. The HISPWM control technique was chosen because it can provide a dc current (I_0) with minimum unwanted dc harmonic components [32]. Simulated waveforms of the proposed synchronous rectifier are shown in Fig. 3.26.

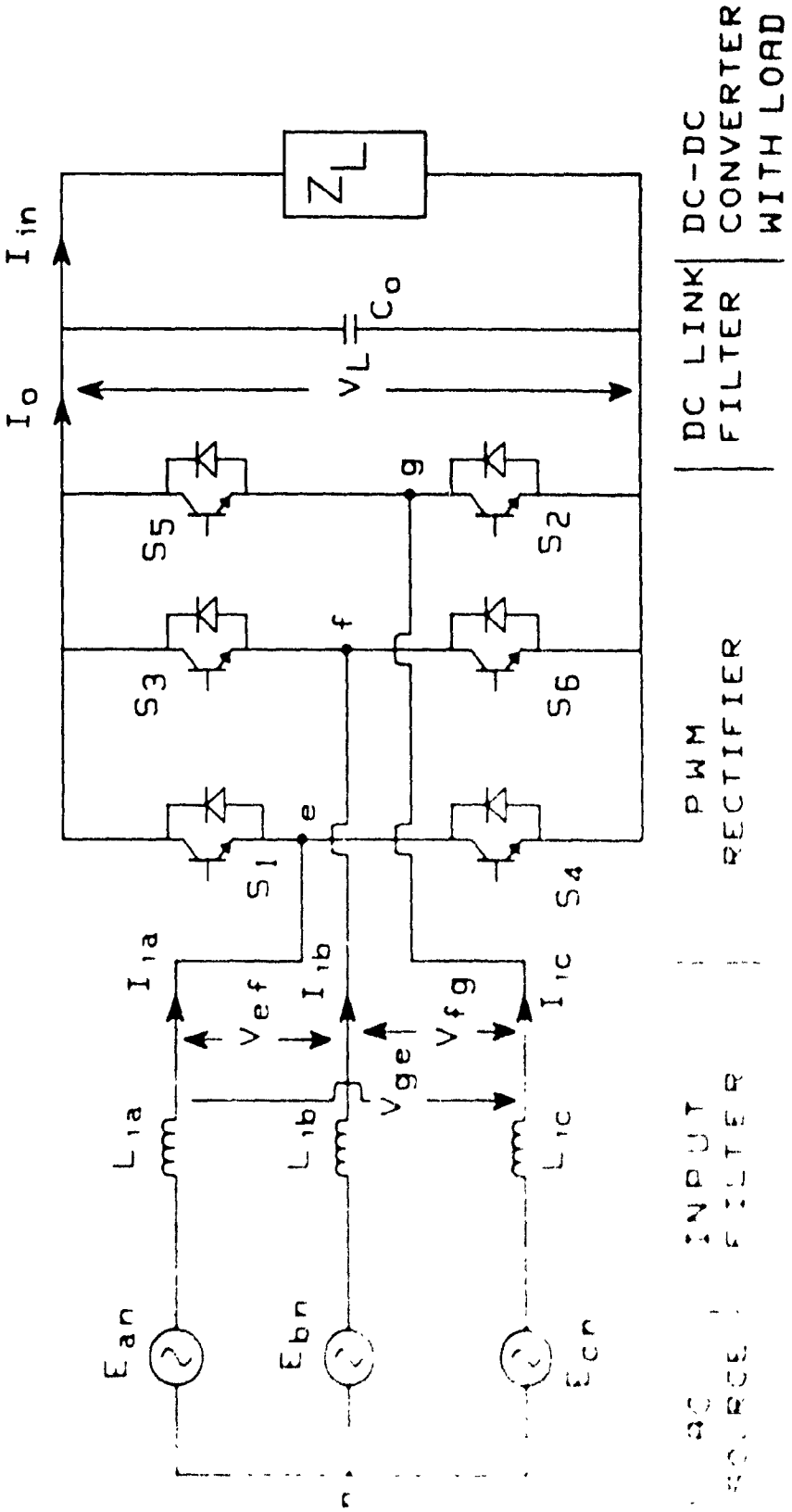


Fig. 3.23 Proposed synchronous rectifier fed three-phase ac-to-dc converter.

3.4.1 Principles of Operation

The operating principles of the synchronous rectifier topology are discussed next with the help of the equivalent circuit shown in Fig. 3.27(a). In this circuit E_{an} represents one of the three phases of the ac source; L_{ia} represents the synchronous interface reactor; and V_{en} is the PWM rectifier input line to neutral voltage. The main performance characteristics of the synchronous rectifier can be deduced from Fig. 3.27(a) as follows:

(I) Real power flow is in principle bilateral, going from E_{an} to V_{en} into the rectifier for lagging δ and vice-versa for leading δ. This power is given by the well known from synchronous machine theory expression

$$P = \frac{EV_{en,1(rms)}}{X_{L_{ia}}}\sin\delta \tag{3.46}$$

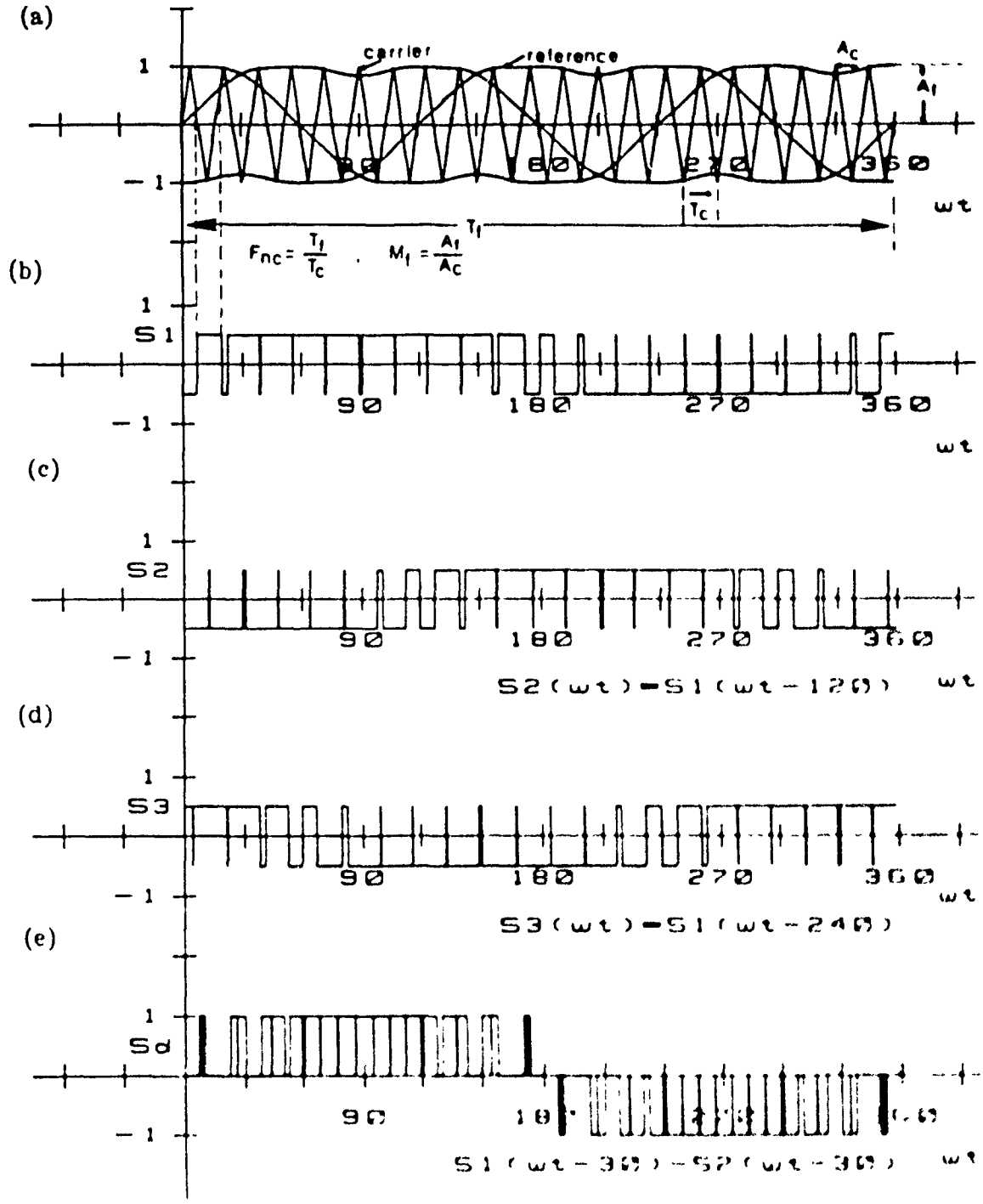
(II) For the special case of $\delta = 0^o$, the input power factor angle ϕ becomes 90^o and consequently only reactive power flows (excluding losses).

(III) For any load condition there is always a set of voltages, ($V_{en,1(rms)}$) and δ values, which yield unity input power factor ($\phi = 0^o$) as shown in Fig. 3.27(c). The relationship between V_{en} and δ that ensures unity power factor is given by (Fig. 3.27(c))

$$V_{en,1(rms)} = \frac{E}{\cos\delta} \tag{3.47}$$

3.4.2 Control Principles

In Figs. 3.25 and 3.26(f) the rms value of the fundamental component of V_{en} is given by


(a)
carrier
reference
A_c
A_f
1
−1
90
180
270
360
ωt
T_c
T_f
$F_{nc} = \frac{T_f}{T_c}$, $M_f = \frac{A_f}{A_c}$
(b)
S1
(c)
S2
S2(ωt)=S1(ωt−120)
(d)
S3
S3(ωt)=S1(ωt−240)
(e)
Sd
S1(ωt−30)−S2(ωt−30)

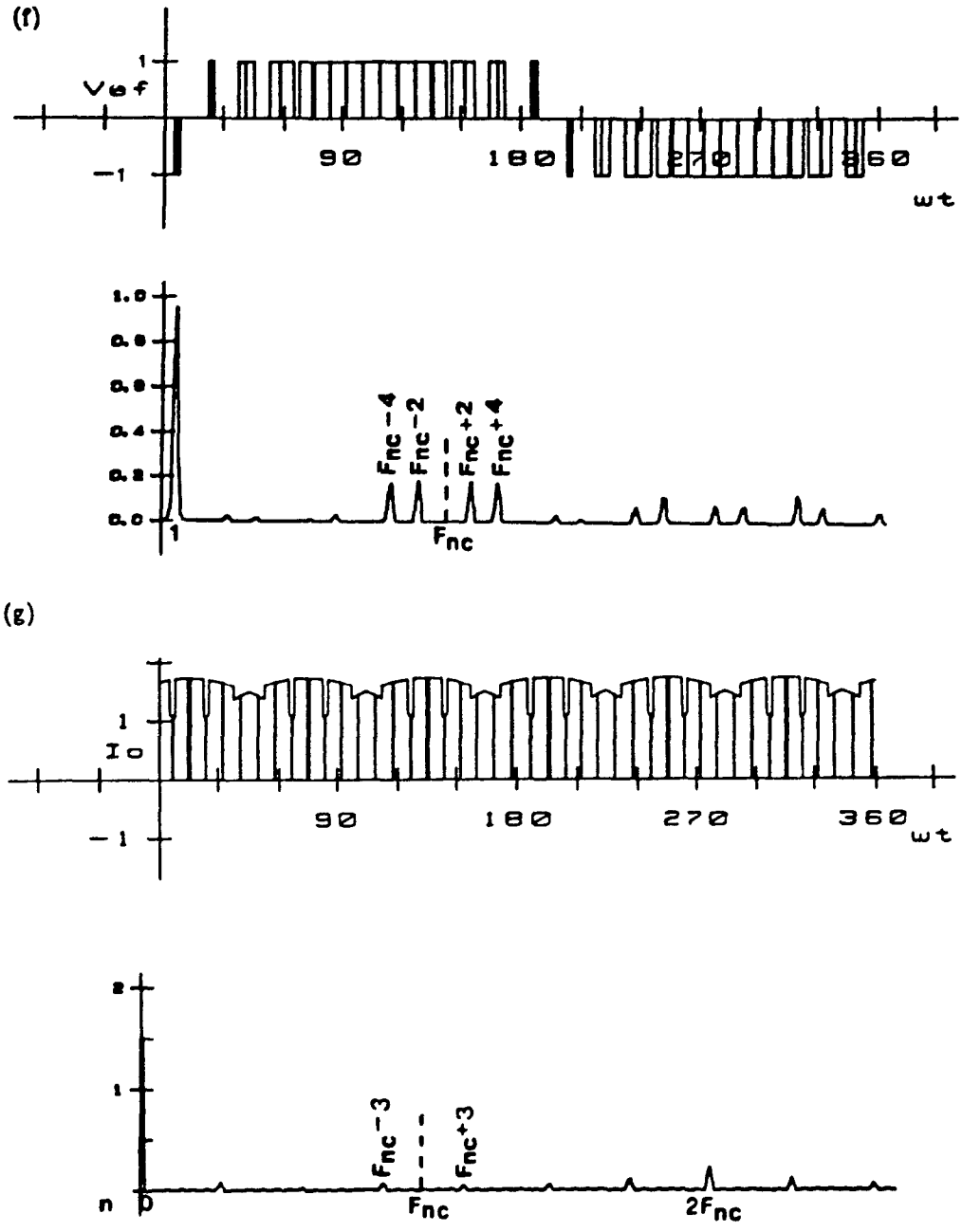


Fig. 3.26: Proposed synchronous active filter topology simulated waveforms.

(a) Definition of HISPWM

(b,c,d)
Waveforms obtained from a.

(e) PWM rectifier switching function (S_d).

(f) PWM rectifier input line-to-line voltage (V_{ef}) and its frequency spectrum.

(g) DC link current (I_o) and its respective frequency spectrum.

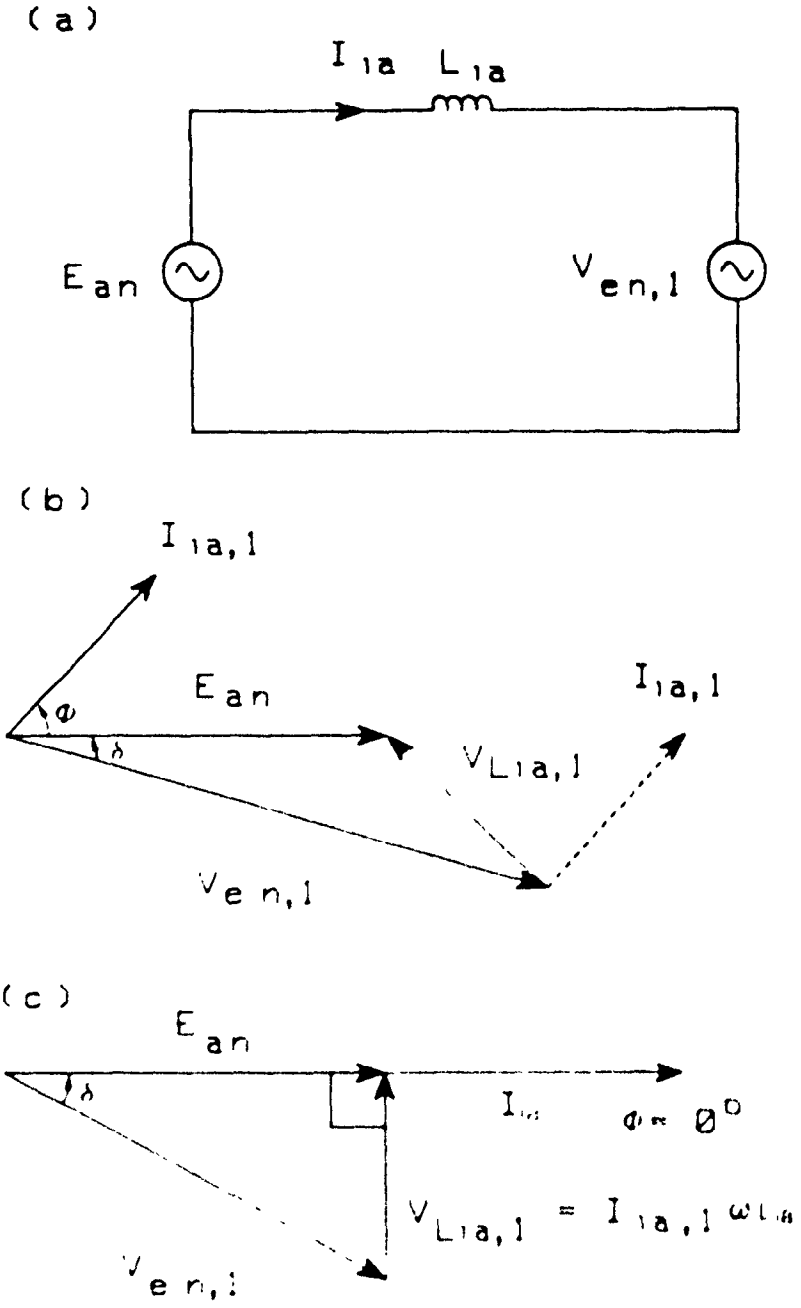


Fig. 3.27: Single-phase equivalent circuit of the synchronous front-end rectifier section and phasor diagrams.

(a) Single-phase equivalent circuit

(b) Phasor diagram for voltages and currents identified in (a)

(c) Phasor diagram for voltages and currents identified in (a) that ensure a unity input power factor.

$$V_{en,1(rms)} = \left[\frac{V_{L,0}}{\sqrt{3}}\right]\left[\frac{M_f}{\sqrt{2}}\right]$$
$$= \frac{V_{L,0}M_f}{\sqrt{2}\sqrt{3}} \tag{3.48}$$

Furthermore, in Fig. 3.27(c) the value of $V_{en,1(rms)}$ is given by

$$V_{en,1(rms)} = \frac{E}{\cos\delta} \tag{3.49}$$

Therefore, using Eqns. (3.46) and (3.48) the value of the synchronous rectifier dc output voltage is given by

$$V_{L,0} = \frac{\sqrt{2}\sqrt{3}E}{M_f \cos\delta} \tag{3.50}$$

Also from Eqns. (3.46) and (3.47)

$$P = \frac{E^2}{X_{L_{ls}}}\tan\delta \tag{3.51}$$

and by setting

$$E = 1\ pu \tag{3.52}$$
$$P = 1\ pu\ (i.e.\ rated\ output\ power\ ) \tag{3.53}$$

then Eqns. (3.49) and (3.51) yield

$$\tan\delta = X_{L_{ls}} \tag{3.54}$$
$$\cos\delta = \frac{1}{\sqrt{1 + X^2{}_{L_{ls}}}} \tag{3.55}$$

Moreover, by using Eqn. (3.54) and setting P = 0 pu Watts, Eqn. (3.51) yields

$$\tan\delta = 0 \tag{3.56}$$
$$\cos\delta = 1 \tag{3.57}$$

Finally, combination of Eqns. (3.50),(3.52),(3.53),(3.55) and (3.57) yields

$$\frac{\sqrt{2}\sqrt{3}}{M_f} \leq V_{L,0} \leq \frac{\sqrt{2}\sqrt{3}}{M_f}\sqrt{1 + X^2{}_{L_{ls}}} \quad pu \tag{3.58}$$

$$for \quad 0 \leq P \leq 1 \quad pu \tag{3.59}$$

A block diagram of the overall synchronous topology including the control loops required to ensure unity power factor and output voltage regulation is shown in Fig. 3.28. The control circuitry of Fig. 3.28 can be simplified by eliminating the unity power factor control loop (dotted line loop) at the cost of slightly reducing the input power factor as follows.

From Eqns. (3.49) and (3.55)

$$V_{en\,,1(rms)_{(max)}} = E\sqrt{1 + X^2_{L_{max}}} \tag{3.60}$$

or

$$V_{en\,,1(rms)_{(max)}} = \sqrt{1 + X^2_{L_{max}}} \quad pu \tag{3.61}$$

Therefore, while output power P varies between

$$0 \leq P \leq 1 \text{ pu}$$

$V_{en\,,1(rms)}$ will vary between

$$1 \leq V_{en\,,1(rms)} \leq \sqrt{1 + X^2_{L_{max}}} \quad pu \tag{3.62}$$

Eqn. (3.62) shows that if $X_{L_{max}}$ is kept sufficiently small ($\leq$ 0.1 pu)

$$V_{an\,,1(rms)} \approx E = 1 \quad pu \tag{3.63}$$

While load conditions change from no load to rated load, maintaining $V_{an\,,1(rms)} \approx E$ has the advantage of eliminating the unity power factor control loop shown in Fig. 3.28 thus reducing the complexity of the control circuitry.

The effect of maintaining $V_{en\,,1(rms)} = E = 1$ pu volts on the input power factor is examined next with reference to Fig. 3.29. Since $E = V_{en\,,1(rms)}$ the voltage triangle shown in Fig. 3.29 is isosceles and the $V_{L_{max}}$ and $I_{s,1}$ phasors are perpendicular to each other the input power factor angle ϕ is given by

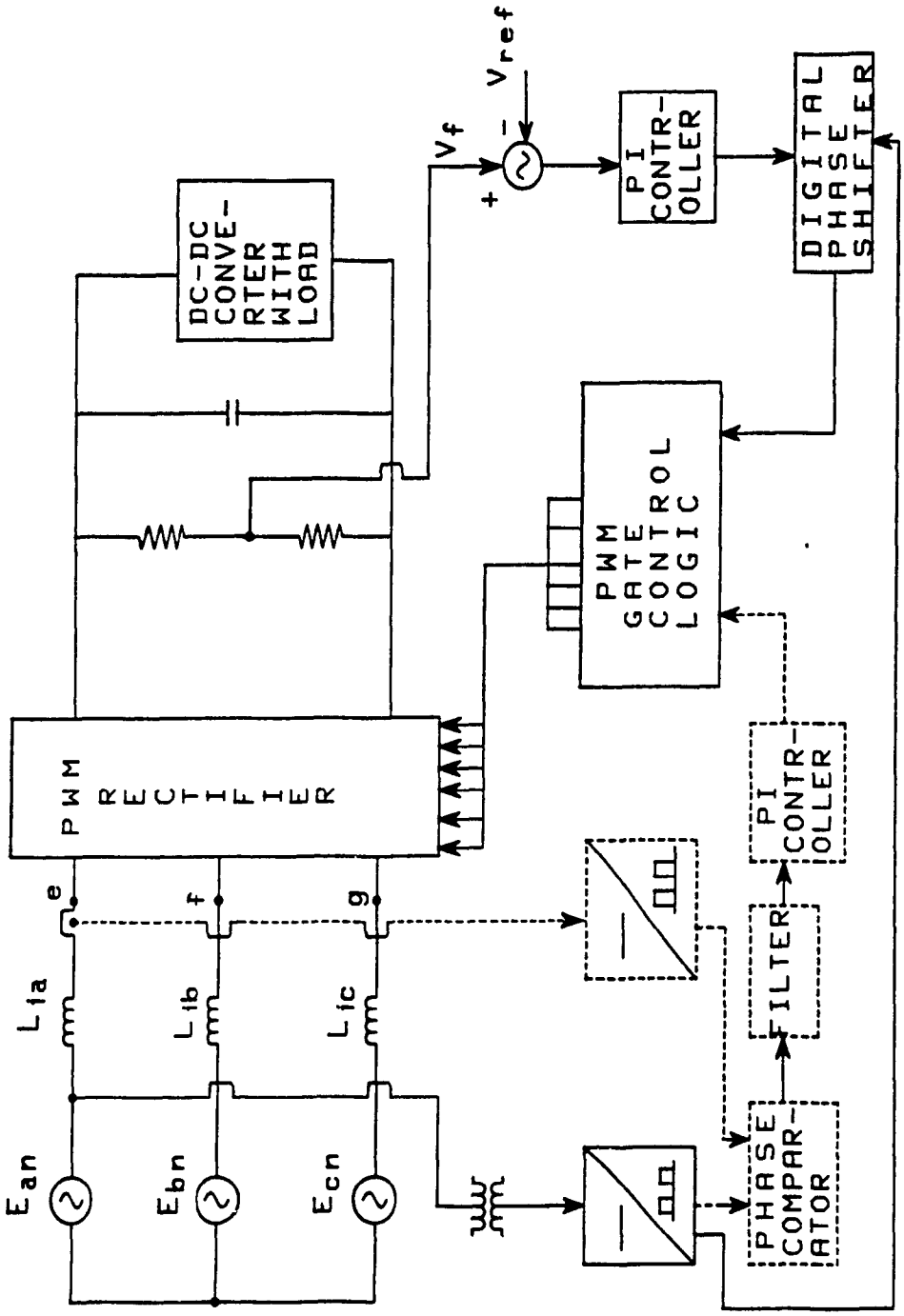


Fig. 3.28: Block diagram of the overall synchronous rectifier unit which includes the control loops required to ensure unity input power factor and output voltage regulation.

$$V_{L\,1a} = I_{1a.1} \bullet X_{L\,1a} \quad P.U.$$

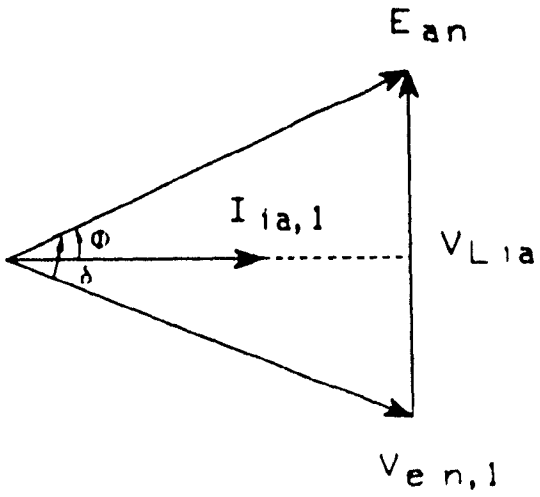


Fig. 3.29: Phasor diagram for voltages and currents identified in Fig. 3.27(a) by setting $E_{an} = V_{en\,1}$.

$$\phi_{max} = \frac{\delta}{2} = Tan^{-1}\left[\frac{V_{L_{is}(rms)}}{2E}\right]$$
$$= \tan^{-1}\left[\frac{X_{L_{is}}}{2}\right] \qquad (3.64)$$

where $X_{L_{is}}$ is the pu reactance of the input filter inductance. If, for example, $X_{L_{is}}$ is selected to be 0.1 pu then the maximum ϕ value becomes

$$\phi_{max} = 3^o$$

This implies a minimum input power factor value of

$$PF = \cos(3^o) = 0.998 \qquad (3.65)$$

which is clearly acceptable.

3.4.3 Active Synchronous Filter Topology

In this section the proposed synchronous filter topology is analyzed under steady-state conditions. The derived expressions are subsequently used to obtain the information necessary for proper front-end rectifier design. The converter is analyzed using the following assumptions:

(1) All power switching devices are ideal and diodes forward drop and reverse leakage currents are negligible.

(2) The filter components are ideal.

(3) The load voltage is ripple free.

Moreover, for the rated input rms voltage E and rated input rms current, $I_{ia,1(rms)}$ values, it is assumed that

$$E = 1\ pu\ \ Volts \qquad (3.66)$$
$$I_{ia,1(rms)} = 1\ pu\ \ Amps \qquad (3.67)$$

where

$$1\ pu\ RMS\ current = \frac{rated\ output\ power}{3\ (Efficiency)\ (RMS\ value\ of\ the\ ac\ source\ phase\ voltage)} \tag{3.68}$$

keeping in mind that power factor is almost unity.

Assuming that the THD of the input line current is $\leq 5\%$ (Fig. 3.25) the rectifier output current before filtering is given by

$$I_o(\omega t) = \left[\sum_{k=0}^{2} S_d(\omega t - \frac{2k\pi}{3}) I_{ia,1} \sin(\omega t - \frac{2k\pi}{3} - \phi)\right] \tag{3.69}$$

where

$S_d(\omega t)$ is the PWM rectifier switching function shown in Fig. 3.26(c) and its harmonic coefficients are given by

$$S_d(\omega t) = \sum_{n=1,5,7}^{\infty} A_n \sin(n\,\omega t) \tag{3.70}$$

Also, the frequency spectrum of the PWM rectifier switching function, $S_d(\omega t)$ is given in Table 3.2

Table 3.2

Frequency spectrum of the Rectifier Switching function, $S_d(\omega t)$

Harmonic order(n)	For $M_f = 1$	For $M_f = .7$
1	1	.7
f_{nc} -4	-.18	-.1
f_{nc} -2	-.16	-.1
f_{nc} +2	-.16	-.1
f_{nc} +4	-.18	-.1
$2f_{nc}$ -7	-.056	-.02
$2f_{nc}$ -5	-.13	-.06
$2f_{nc}$ -1	-.083	-.34
$2f_{nc}$ +1	+.083	+.34
$2f_{nc}$ +5	+.13	+.07
$2f_{nc}$ +7	+.056	+.024

Substituting Eqns. (3.70) into (3.69) and assuming that the rectifier input line currents are balanced

$$I_o(\omega t) = \sum_{k=0}^{2} \Bigg[A_1 \sin(\omega t - \frac{2k\pi}{3}) + A_{f_{nc}-4} \sin((f_{nc}-4)\omega t - \frac{2k\pi}{3}) + A_{f_{nc}-2} \sin((f_{nc}-2)\omega t - \frac{2k\pi}{3}) + A_{f_{nc}+2} \sin((f_{nc}+2)\omega t - \frac{2k\pi}{3}) + A_{f_{nc}+4} \sin((f_{nc}+4)\omega t - \frac{2k\pi}{3}) + \ldots \Bigg] * \Bigg[I_{ta,1} \sin(\omega t - \frac{2k\pi}{3} - \phi) \Bigg] \quad (3.71)$$

As $I_o(\omega t)$ has harmonic components which are multiples of six of the fundamental (i.e. 6,12,18,24,.....) Eqn. (3.71) becomes

$$
\begin{aligned}
I_o(\omega t) = {} & \frac{3A_1 I_{ia,1}}{2}\cos\phi \\
& - \left\{\frac{3A_{f_{nc}-4} I_{ia,1}}{2} - \frac{3A_{f_{nc}-2} I_{ia,1}}{2}\right\}\cos((f_{nc}-3)\omega t + \phi) \\
& - \left\{\frac{3A_{f_{nc}+2} I_{ia,1}}{2} - \frac{3A_{f_{nc}+4} I_{ia,1}}{2}\right\}\cos((f_{nc}+3)\omega t + \phi) \\
& - \frac{3A_{2f_{nc}-7} I_{ia,1}}{2}\cos((2f_{nc}-6)\omega t - \phi) \\
& + \frac{3A_{2f_{nc}-5} I_{ia,1}}{2}\cos((2f_{nc}-6)\omega t + \phi) \\
& - \left\{\frac{3A_{2f_{nc}-1} I_{ia,1}}{2} - \frac{3A_{2f_{nc}+1} I_{ia,1}}{2}\right\}\cos(2f_{nc}\omega t + \phi) \\
& - \frac{3A_{2f_{nc}+5} I_{ia,1}}{2}\cos((2f_{nc}+4)\omega t + \phi) \\
& + \frac{3A_{2f_{nc}+7} I_{ia\,1}}{2}\cos((2f_{nc}+6)\omega t + \phi) \qquad (3.72)
\end{aligned}
$$

where $f_{nc} = 21,27,33$ ....

A close examination of Eqn. (3.72) reveals that the (f_{nc}-3) and (f_{nc}+3) harmonic components cancel each other thus providing a harmonic free dc link current. Also from Eqn. (3.72) it can be observed that the dc and dominant harmonic components of $I_o(\omega t)$ under worst operating condition (M_f =.7) are given by

$$
\begin{aligned}
I_{o\,0} &= \frac{3A_1 I_{ia\,1}}{2}\cos\phi = (\frac{3}{2})(M_f)(\sqrt{2})(\simeq 1) \\
&= 2.1M_f \qquad (3.73)
\end{aligned}
$$

$$
\begin{aligned}
I_{o\,2f_{nc}} &= \frac{3(-A_{2f_{nc}\,1} + A_{2f_{nc}+1})I_{ia\,1}}{2} \\
&= \frac{3(\frac{3+3}{7})\sqrt{2}}{2} = 1.82 \qquad (3.74)
\end{aligned}
$$

Fig. 3.26(g) shows the simulated waveform of the rectifier output current before filtering and its respective frequency spectrum.

3.4.4 Output Filter

In Fig. 3.26(g) the front-end rectifier output current, $I_o(\omega t)$, consists of a modulated train of pulses and consequently some form of filtering is necessary to separate the dc component from the undesired harmonic components. Furthermore, the amplitude of the $2f_{nc}$ order voltage harmonic component across the output filter capacitor, C_o, is given by

$$V_{L,2f_{nc}} = \frac{I_{o,2f_{nc}}}{2f_{nc}\omega C_o} \tag{3.75}$$

Moreover, the allowable rectifier output voltage ripple can be defined by

$$Ripple\ \% = \frac{100 V_{o,2f_{nc}(rms)}}{V_{L,0}} \tag{3.76}$$

Substituting Eqns. (3.74) and (3.76) into (3.75), the value of the output filter capacitance is given by

$$\begin{aligned} C_o &= \frac{I_{o,2f_{nc}} 100}{\sqrt{2}(2f_{nc})(\omega)(Ripple\ \%)(V_{L,0})} \\ &= \frac{(1.82)100}{\sqrt{2}(2f_{nc})(1)(Ripple\%)(\frac{\sqrt{2}\sqrt{3}}{M_f})} \quad pu \\ &= \frac{26.3M_f}{(f_{nc})(Ripple\%)} \quad pu \end{aligned} \tag{3.77}$$

where

$$1\ pu\ capacitance = \frac{1}{(\ 1\ pu\ frequency\ )(\ 1\ pu\ impedance\ )} \tag{3.78}$$

and

$$1\ pu\ angular\ frequency\ = \omega\ rad/sec \tag{3.79}$$

3.4.5 Input Filter

In most specifications for power supplies the THD content of the input line current, I_{ia} , is required to be $\leq$ 5% [33]. Also it can be shown that if the amplitude of the dominant harmonic component of I_{ia} is reduced to 3% of the amplitude of the respective fundamental, then a THD $\leq$ 5-percent can be ensured. Therefore,

$$I_{ia,d} = \frac{V_{en\ d}}{d * X_{L_n}} = 0.03 \quad pu \tag{3.80}$$

Moreover, for the harmonic injection sinusoidal PWM (HISPWM) control technique shown in Fig. 3.26, the order of the dominant harmonic component of the PWM rectifier input voltage (Fig. 3.26(f)) and its respective amplitude under the worst operating condition ($M_f = 1$) are given from Table 3.2 as follows.

$$d = f_{nc} - 4 \tag{3.81}$$

$$V_{en\ d} = V_{L\ 0}\left[\frac{0.18}{\sqrt{3}}\right] \tag{3.82}$$

By substituting Eqn. (3.57) into Eqn. (3.82) then

$$V_{en\ d} = 0.25\sqrt{1 + X^2_{L_n}}\ pu$$

$$\approx 0.25 \quad pu \tag{3.83}$$

Therefore substituting Eqn. (3.83) into (3.80) the value of the input filter reactance is given by

$$X_{L_n} = \frac{8.3}{f_{nc} - 4} \quad pu \tag{3.84}$$

As expected, the choice of the synchronous reactance value $X_{L_{ia}}$ involves a trade-off between switching frequency and inductor size and weight.

3.4.6 Component Ratings

From the aforementioned assumptions and derived analytical expressions the voltage and current ratings of the various system components are as follows.

Inductor L_{ia}

Value of L_{ia} :0.1 pu

Rms current $(I_{ia,rms}) = \sqrt{\sum_{n=1}^{\infty} \left(\frac{I_{ia,n}}{\sqrt{2}} \right)^2}$: 1.0 pu

Peak current $(I_{ia,peak}) = \sqrt{\sum_{n=1}^{\infty} I_{ia,n}{}^2}$: $\sqrt{2}$ pu

Rectifier Switch

Average current : 0.707 pu

Rms current $= \frac{I_{ia(rms)}}{\sqrt{2}}$: 0.707 pu

Peak current : $\sqrt{2}$ pu

DC Filter Capacitor C_o

Value : Eqn. (3.77)

Rms ripple current : 1.287 pu

Peak voltage : 2.5 pu

It is noted that the ratio of the rms input current (I_{ia}) to the peak value of the input current is higher in the proposed synchronous active filter topol-

ogy than in the single switch front-end section (from section 3.3.6) for the same inductor value of 0.1 pu. Moreover dc bus voltage is approximately reduced to half the value. Therefore the proposed synchronous filter topology exhibits a higher power density.

3.4.7 Design Example

In order to illustrate the significance and facilitate the understanding of theoretical results obtained in previous sections the following design example is given. The rectifier unit has the following specifications.

- DC load voltage ($V_{L\,0}$)= 48V
- DC load current (I_L)= 100A
- AC source rms phase voltage (E) = 120V
- Modulation factor (M_f) = 1
- Supply frequency (f_s) = 60HZ
- Normalized carrier frequency (f_{n_c}) = 61
- Load voltage ripple (R%) = 2%
- Rectifier efficiency = 85%

Assuming balanced input line currents and using the above specifications

1 pu Volts = 120V

1 pu current = $I_{s\,1\,rms}$ = $\frac{(48)(100)}{(3)(.85)(120)}$ = 15.7A

1 pu frequency = $2\pi f_s$ = 377 rad/sec

1 pu impedance = $\frac{120}{15.7}$ = 7.6Ω

$$1 \text{ pu capacitance} = \frac{1}{(377)(7.6)} = 3.47 * 10^{-4} \text{ Farads}$$

Using Eqns. (3.84) and (3.77) the input and output filter components are given by

$$X_{L_{ia}} = \frac{8.3}{61-4} = 0.14 \quad pu$$

$$X_{L_{ia}} = (0.14)(7.6) = 1\Omega$$

$$L_{ia} = \frac{X_{L_{ia}}}{\omega} = \frac{1}{377} = 2.6mH$$

$$C_o = \frac{26.3 * 1}{(61)(2)} \quad pu$$

Therefore

$$C_o = 0.21557 \text{ pu}$$

or

$$C_o = 0.216 * 3.47 * 10^{-4} = 74.8 \quad \mu F$$

Also using Eqns. (3.64) and (3.65) the maximum power factor angle and power factor are given by

$$\phi_{\max} = \frac{\delta}{2} = \tan^{-1}(\frac{0.14}{2}) = 4^o$$

$$PF = \cos(4) = .997$$

3.4.8 Experimental Results

To verify selected predicted results an experimental 2 kW front-end synchronous rectifier topology has been implemented using power MOSFETs. Results obtained with this synchronous rectifier experimental unit are shown

in Fig. 3.30. Evaluation of experimental results shows that they are in close agreement with the simulated results shown in Fig. 3.26.

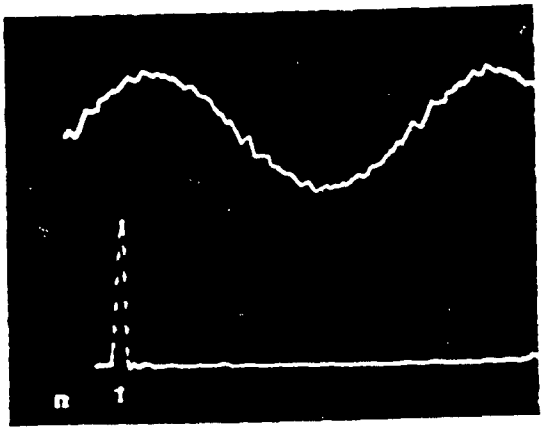
3.4.9 Conclusions

In this section a novel three-phase fed synchronous active filter topology has been proposed. This topology draws high quality input current waveforms from the ac source. The synchronous front-end bridge rectifier operation is analyzed in detail and the steady state performance has been obtained. Performance evaluation and relevant design data have been provided for implementation of the front-end bridge rectifier. Detailed input current and output current analysis has shown that the proposed synchronous rectifier exhibits practically sinusoidal ac input current with reduced dc harmonic components. Moreover, the input filter ac capacitor and output filter inductor are eliminated thus decreasing further the size and the cost of the front-end rectifier unit. Moreover since the proposed topology uses a front end reactor it exhibits improved reliability against short circuits. Finally, predicted features such as input/output current, voltage waveforms and associated harmonic spectra have been verified experimentally on laboratory prototype units.

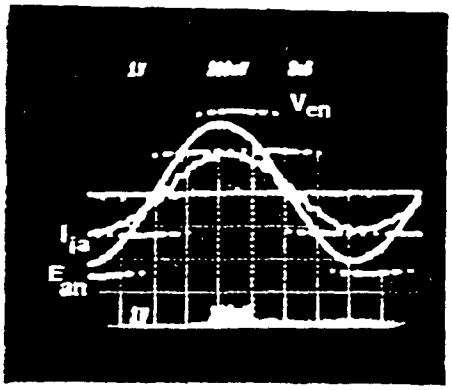
3.5 Conclusions

The proposed front-end single-phase active filter topology (Fig. 3.4 draws practically ripple free sinusoidal ac input current and improves the input power factor further as compared to the passive filter topology discussed

(a)

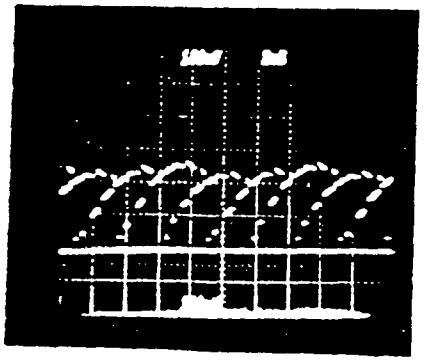


(b)



Amp.:(E_{an}) 100 Volts./Div.
(I_{ia}) 2 Amps./Div.
(V_{cn}) 100 Volts./Div.
Time:2 msec./Div.

(c)



Amp.:(I_o) 1 Amp ./Div.
Time:2 msec./Div.

Fig. 3.30: Experimental waveforms of the proposed synchronous rectifier.
(a) Rectifier input line current and its frequency spectrum.
(b) Rectifier ac source line-to-neutral voltage (E_{an}), input line current (I_{ia}) and PWM rectifier input voltage with respect to neutral.
(c) Dc link current (I_o).

in chapter 2 (Fig. 2.5). Moreover the main advantage of the active method over the passive method is that the inductor size can be controlled by changing the input current ripple or by increasing the switching frequency. Furthermore, the proposed design allows the boost converter to operate at constant switching frequency. Finally, predicted features such as input current waveforms have been verified experimentally on a one kVA laboratory unit.

Moreover, in this chapter a novel three-phase fed boost active filter topology has been proposed. This topology draws high quality input current waveforms from the ac source. The front-end bridge rectifier operation has been analyzed in detail and the steady state performance is obtained. Performance evaluation and relevant design data have been provided for implementation of the front-end bridge rectifier. Detailed input current and output current analysis has shown that the proposed converter yields unity input power factor, eliminates the synchronization logic requirement, and reduces the component count considerably in comparison with the conventional converter. However the proposed front-end active filter topology has the disadvantage of increasing the current and voltage stresses of the boost switching device. Finally, key predicted results such as input/output current, voltage waveforms and associated harmonic spectra have been verified Experimentally.

Furthermore, in this chapter a novel three-phase fed active filter topology has been proposed. This topology draws high quality input current waveforms from the ac source and reduces the switching stresses of the switching devices. The synchronous front-end bridge rectifier operation has been analyzed in detail and the steady state performance is obtained. Performance evaluation and relevant design data have been provided for implemen

tation of the front-end bridge rectifier. Detailed input current and output current analysis has shown that the proposed synchronous rectifier exhibits practically sinusoidal ac input current with reduced dc harmonic components. Moreover, the input filter ac capacitor and output filter inductor are eliminated thus decreasing further the size and the cost of the synchronous rectifier unit. Moreover since the proposed topology uses a front end reactor it exhibits improved reliability against short circuits. Finally, predicted features such as input/output current, voltage waveforms and associated harmonic spectra have been verified experimentally on laboratory prototype units.

CHAPTER 4

HIGH-FREQUENCY LINK SECTION

4.1 Introduction

Chapters 2 and 3 dealt with the analysis and design of front-end passive and active rectifier section of the high frequency link ac-to-dc converter. This chapter concentrates on the analysis and design of the high frequency link section of the ac-to-dc converter. The main design objectives in any high frequency link converter are minimization of switching transients, and minimization of switching losses. Both of these requirements can be met simultaneously if the chosen circuit topology and/or method of power control ensures switch turn-on under zero-voltage and zero-current conditions, and switch turn-off under zero-voltage conditions. These conditions are naturally satisfied with resonant types of circuit topologies operating with the antiparallel diode conducting when the respective switch is turned on [8,11] (current lagging mode). However for SMR applications, in addition to increased component count, resonant power supplies have the disadvantage of requiring a wide operating frequency range in order to maintain constant output voltage under varying input voltage and varying load conditions. Therefore they are more compatible with topologies that use some form of voltage pre-regulation.

On the other hand, the PWM type of switch mode power supplies can by definition maintain constant output voltage under varying input/output conditions without varying the operating frequency. However, they cannot always ensure the aforementioned critical current-lagging mode of operation.

This is particularly true under high input voltage and light load operating conditions when the respective duty cycle assumes its minimum value.

The object of this chapter is to propose and analyze single-phase and three-phase fed high frequency link sections which yield high quality input current waveforms and high input power factor values. Furthermore the PWM constant frequency inverter section is always operating in the current lagging mode. The resulting advantages include lower inverter switching losses and higher efficiency.

4.1.1 Single-Phase High Frequency Link

Conventional high frequency link (HFL) converter (Fig. 4.1) generally fed from a single-phase front-end diode rectifier, and operated at a fixed inverter frequency control the output voltage by multi pulse PWM method. It is customary to provide a short dead time between the complementary switching devices in order to avoid having them conduct simultaneously. This type of output voltage control is more suitable for low power levels. At medium power levels the storage time of the inverter switches becomes a significant portion of the total high frequency 'on' time when bipolar switches are used. Consequently as operating frequencies increase the output voltage control by multi-pulse PWM of the inverter switching devices has several disadvantages including:

(i) difficulty often experienced at very short conduction times in developing a good turn-off signal;

(ii) pulse dropping during the narrow pulses or a possibility of short circuit across the dc bus;

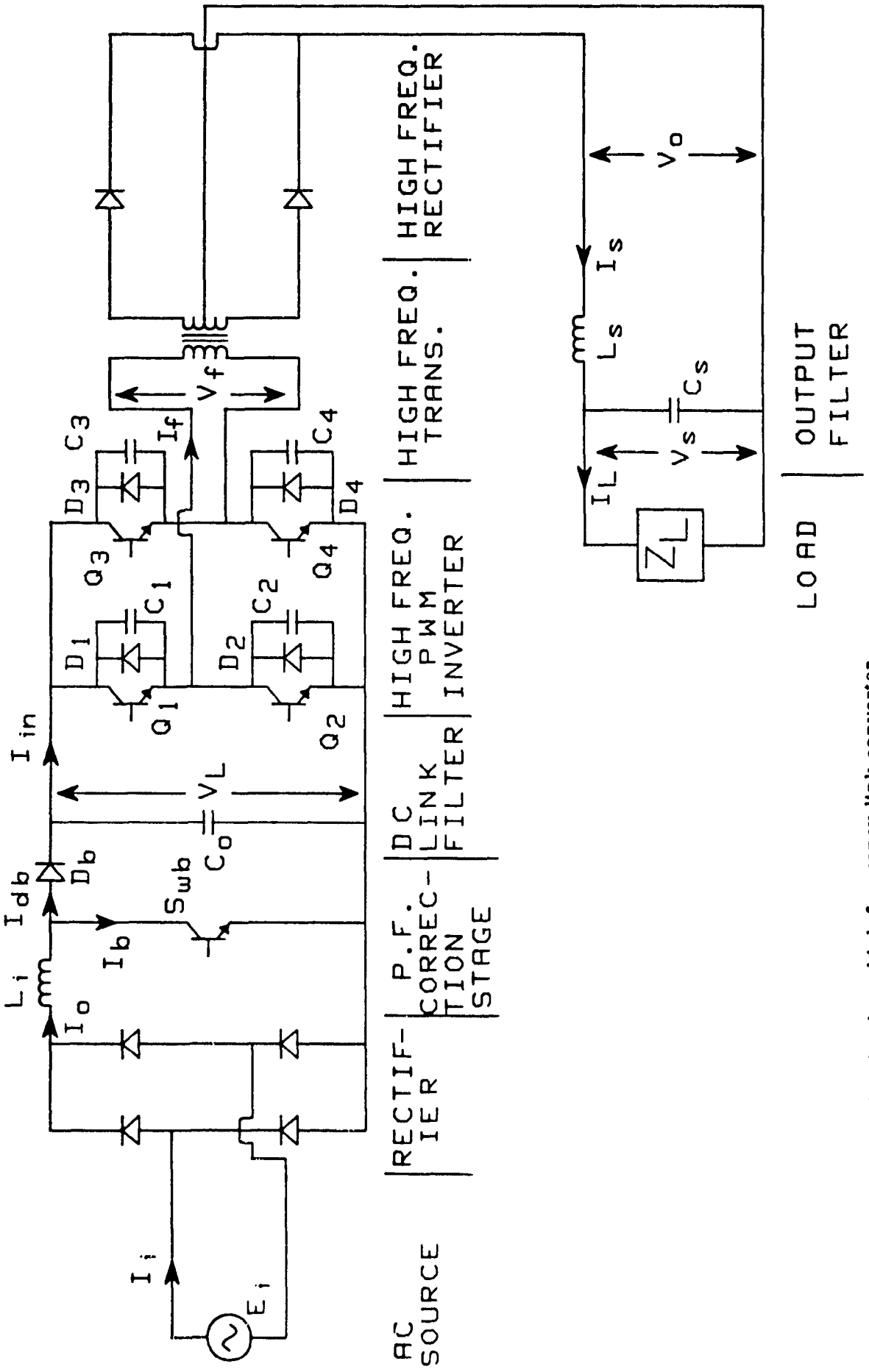


Fig. 4.1: Single-phase high frequency link converter.

(iii) associated turn-on and turn-off losses of the switching devices.

To overcome these problems at medium power level (3kW - 12kW), inverters are often driven with square wave PWM method. By using a square wave drive for each transistor pair in a full bridge inverter (Q_1,Q_4 and Q_2,Q_3), many problems associated with driving bipolar transistors at very narrow duty cycles are completely avoided. By phase shifting the each transistor pair gating signals with respect to the other pair the ends of the primary transformer coil will always be clamped because at least one transistor at each end is always 'on'. This gives better control of the energy in the primary circuit. The results of this clamping effect is less ringing due to circuit parasitics and lower switching losses at rated load. However controlling the output voltage by varying the phase angle of the inverter transistor pair gating signals will not address the problems associated with the transistor antiparallel diode recovery current spikes seen in these systems. In the proposed HFL converter topologies the PWM constant frequency inverter section is always operating in the current lagging mode and the output voltage is controlled by the front-end controlled rectifier. This topology allows the safe use of lossless single capacitor inverter switch snubber from zero to rated load power variation. To ensure the safe and lossless operation of the high frequency stage under all operating conditions, the inverter stage is analyzed in detail and expressions are derived for the snubber capacitor voltage as a function of the high frequency transformer leakage and magnetizing inductances, operating frequency, and the charging time of the snubber capacitors.

4.1.2 High Frequency Link with Suppressed dc Components

For medium power applications the three-phase fed front-end converter that uses a diode rectifier and a single switch is a good choice (discussed in section 3.3) to satisfy the requirements mentioned in section 4.1.1. However it has the disadvantage of increasing the switching stresses of the switching devices. Application of the three-phase fed synchronous front-end rectifier (Fig. 4.2) discussed in section 3.4 eliminates all the above disadvantages and exhibits high power density, improved reliability, elimination of the input filter ac capacitor, and elimination of the dc link capacitor. Finally, experimental results from a prototype HFL converter are compared and verified with the analytically predicted results.

4.1.3 Three-Phase High Frequency Link Section

The ever increasing need for isolated dc power is met today by off-line dc-dc rectifiers or HFL converters that employ single-phase high frequency link inverter circuits such as the one shown in Figs. 4.1 and 4.2. These converters have been shown to perform quite well for power applications ranging from 2 to 10 kW. For higher power levels, however, single-phase inverter circuits face severe component stresses. As an alternative this section proposes the use of three-phase inverter circuits in HFL converters (Fig. 4.3). The resulting advantages include:

(1) a dramatic increase (by a factor of three) in input current and output voltage chopping frequencies;

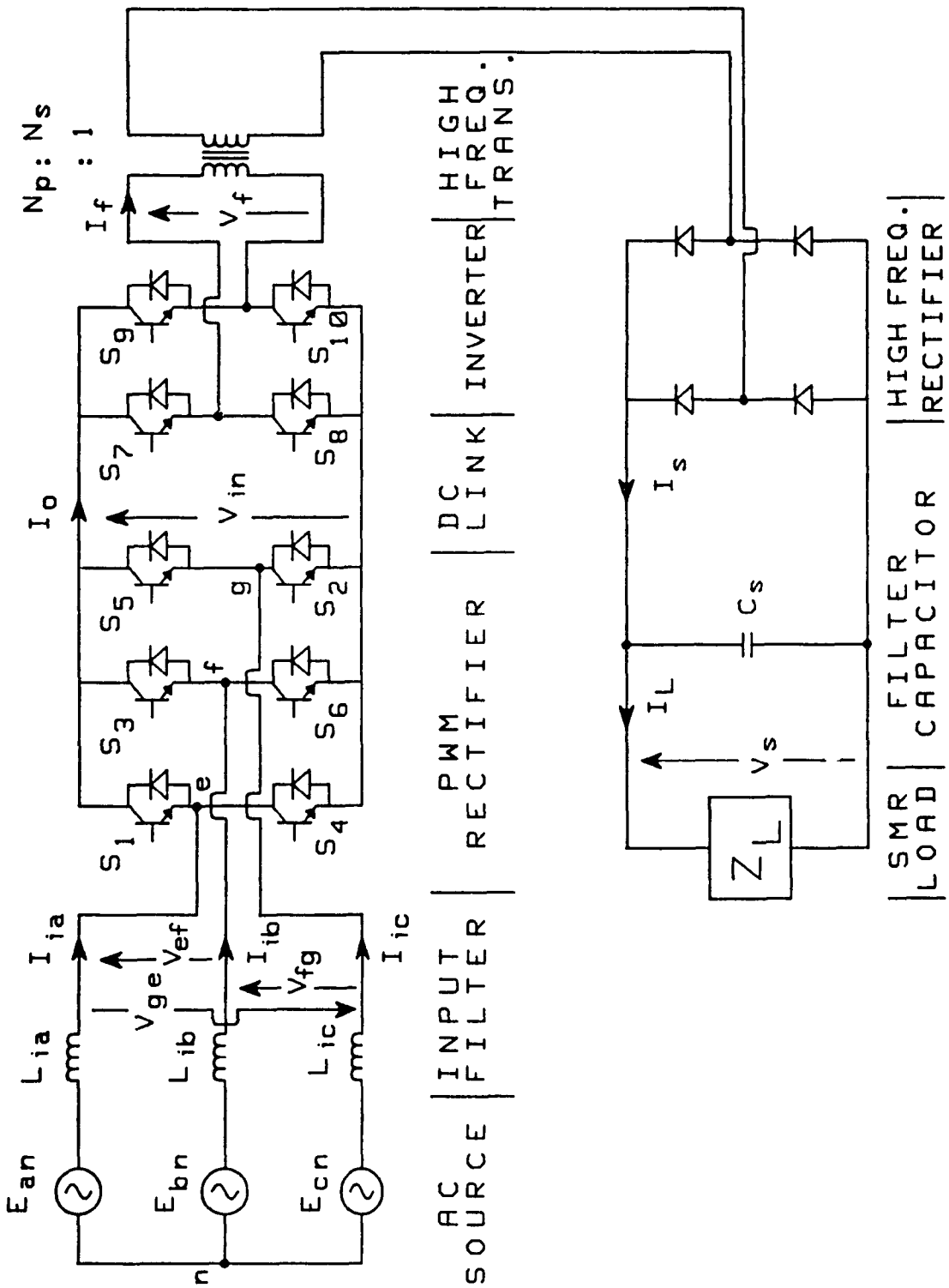


Fig. 4.2: Proposed synchronous rectifier fed three-phase ac-to-dc converter.

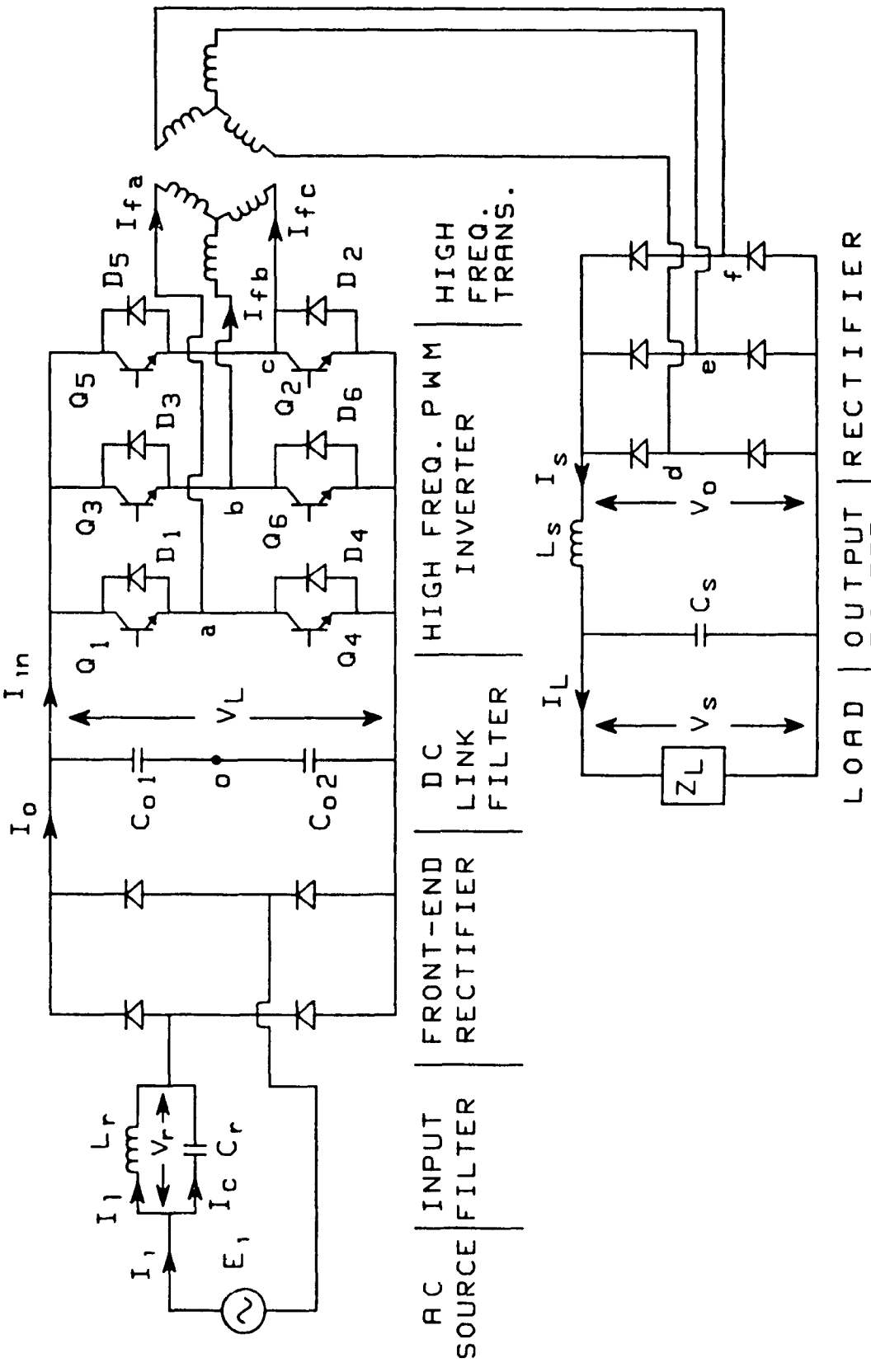


Fig. 4.3: Three-phase high frequency link converter.

(ii) a lower RMS current through the inverter switches or a higher power transfer for the same switch current and voltage stresses;

(iii) a reduction in the size of the reactive (filter) components;

(iv) better transformer copper and core utilization;

(v) inherent delays in switching actions, such as the storage time in BJT's, do not pose conduction overlap problems under converter overload conditions.

The last advantage is particularly important when designing the converter for large input voltage and load fluctuations. However, the proposed topology also exhibits the disadvantage of increased power and control circuit complexity. The different modes of operation of the three-phase inverter, the associated output voltage control methods, and the commutation of the inverter switches have been discussed in detail. This section also presents an analysis and design approach for three-phase HFL converters under large input voltage and load variations. Finally, theoretical results have been verified experimentally. The three-phase PWM inverter employed here must exhibit some unusual operating features including:

(i) switching frequencies above 20 kHz;

(ii) voltage control by a single pulse PWM gating signal;

(iii) inverter feeding (transformer excluded) a three-phase diode rectifier directly.

Consequently the switching times of the semiconductor components become crucial to the inverter performance (commutation).

4.2 Single-Phase High Frequency Link Section

The benefits derived from operating high frequency link PWM power converters in the current lagging mode have already been identified by several researchers [8]. These benefits can be easily visualized by referring to the full bridge inverter circuit shown in Fig. 4.1 and the corresponding current and voltage waveforms shown in Figs. 4.4(a) and 4.4(b). The resulting advantages include:

(i) increased operating frequencies since switching losses have been minimized;

(ii) use of slower switching devices, such as high power bipolars, in high switching frequency applications, since switching losses have been minimized;

(iii) raising the output power levels obtained per single module;

(iv) lowering the cost per HFL module by using cheap lower switching-grade high-power switches.

From Figs. 4.1, and 4.4(a) it is obvious that in the current-lagging mode, the inverter switches turn on when the respective antiparallel diodes are conducting (zero current and voltage condition) and turn off under the zero voltage condition because of the presence of the snubber capacitor. However, as can be seen from Figs. 4.1, and 4.4(b), such operation is not possible when the inverter is operating in the current-leading mode. The reason is that the direct charging and discharging of snubber capacitors through the respective transistor switches can seriously damage these switches.

The main difficulty in exploiting the advantages of the current lagging mode has been the fact that output voltage regulation through inverter duty

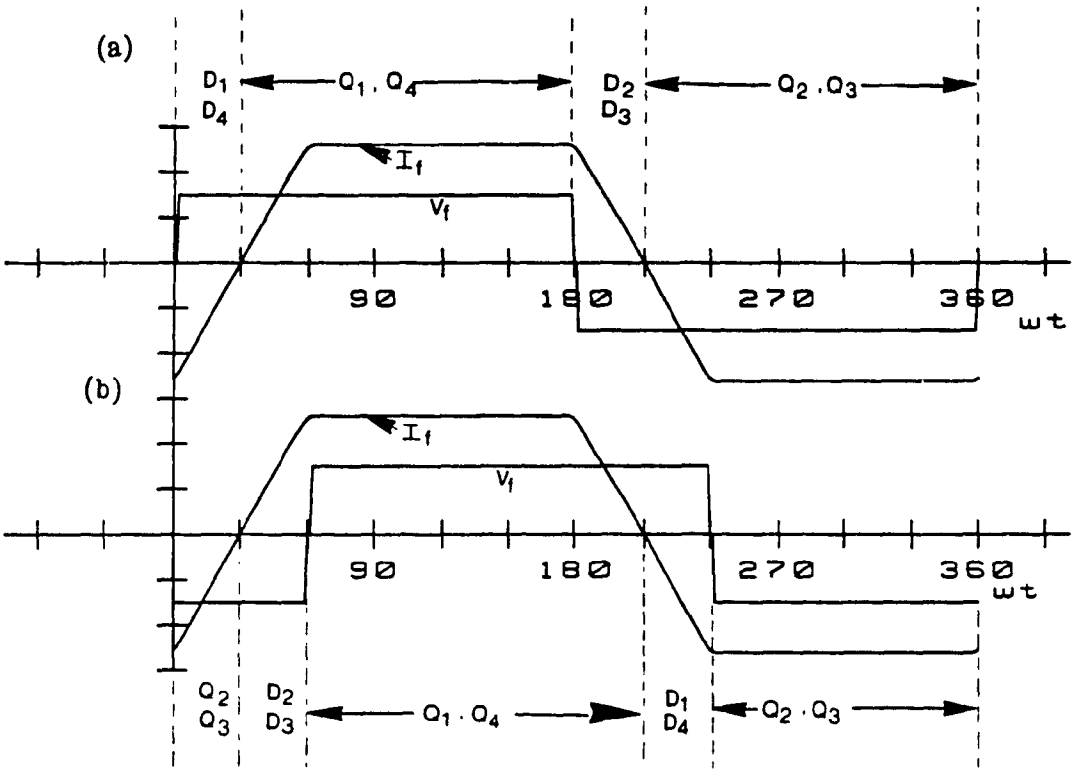


Fig. 4.4: High frequency transformer primary voltage, V_f , and current, I_f .
(a) In lagging mode of operation.
(b) In leading mode of operation.

cycle variation results in partial operation in the current leading mode. Moreover varying the duty cycle of the inverter switches yields lower use of the power semiconductor switches and high component stresses. Consequently the proposed inverter operates at a fixed duty cycle (≈50-percent) and the output voltage is maintained constant by the front-end controlled rectifier from minimum load to maximum load. The high frequency transformer leakage and the magnetizing inductances are designed to ensure the safe commutation of the inverter under varying input voltage and load conditions.

Application of the front-end passive filter topology (Fig. 2.5) in HFL converters (see section 2.3) maintains a high quality input current waveform; however, it has inherent disadvantages such as a lack of control on the output voltage (V_L) and a narrow operating region. Hence, this type of power conversion approach is more and more attractive when the converter is delivering constant power and the input source voltage (E_i) is practically constant. These disadvantages can be eliminated by the use of the active front-end converters in HFL converters (see Chapter 3). This type of power conversion has the advantages of maintaining a high quality input current waveform and output voltage control from minimum to maximum load conditions.

4.2.1 Inverter/Rectifier

In this section the inverter is analyzed under steady state conditions. The derived expressions are subsequently used to obtain the information necessary for proper inverter design. Moreover, the value of the inverter input voltage (V_L) depends upon the front-end rectifier system. The inverter is analyzed under the following assumptions:

(i) all power switching devices are ideal and the forward drop and reverse leakage currents of the diodes are negligible;

(ii) the filter components are ideal;

(iii) the load voltage (V_s) and inverter input voltage (V_L) are ripple free.

Furthermore,

$$V_L = 1.0 \ pu$$

and

$$P_o = 1.0 \ pu$$

As shown in Fig. 4.4, the current flowing through the high frequency transformer (HFT) is a trapezoidal waveform. To ensure the safe commutation of the inverter switches, a small interval of dead time is required between the operation of the complementary switches. This can be explained as follows. Initially transistor Q_1 (Fig. 4.1) carries the load current and the voltage across C_1 is zero. The voltage across C_2 is equal to the dc link voltage V_L and when Q_1 turns off, its current (I_f) is diverted into the capacitor C_1, thus limiting the voltage rise across the switch Q_1. Note that the capacitor C_1 is being charged at the same time capacitor C_2 is being discharged. The complementary switch Q_2 should not be turned on until the voltage across C_1 rises to the dc link voltage, V_L, and the voltage across C_2 falls to zero. If Q_2 turns on before this period, a short circuit occurs between the positive and negative inverter terminals through capacitor C_1. Therefore, a finite dead time is required between gating signals of complementary inverter switches. This dead time depends upon the current I_f, the value of the snubber capacitor, and the HFT leakage and magnetizing inductances. Moreover, the worst operating condition, in terms of commutation of the switches, is the no load

condition. If one can ensure the safe commutation of the inverter at no-load conditions, safe commutation at any other load is certain because the load current is at a minimum at no-load. Further more at no-load the current flowing through the HFT primary winding is as shown in Fig. 4.5. The relevant expressions for voltage across the switch Q_1, and the current through the switch Q_1 are derived as follows:

HFT leakage inductance referred to primary $= L_L$

HFT magnetizing inductance $= L_M$

If we let, $L = L_L + L_M$ then

$$V_L = L\frac{dI_f(t)}{dt}$$

$$I_f(t) = \frac{V_L}{L}(t - \frac{T_s}{4}) \qquad 0 \leq t \leq \frac{T_s}{2}$$

$$= -\frac{V_L}{L}(t - \frac{3T_s}{4}) \qquad \frac{T_s}{2} < t \leq T_s \tag{4.1}$$

At time $t = \frac{T_s}{2}$, transistors Q_1 and Q_4 turn off. Here T_s is the time period of the high frequency inverter. The current flowing through the snubber capacitor is

$$I_f(\frac{T_s}{2}) = \frac{V_L}{4L}T_s \tag{4.2}$$

Assuming constant current during the commutation, the current flowing through the capacitor C_1, the HFT leakage and magnetizing inductances (L), and the capacitor C_4 at time t=0 is given by

$$I_f(0) = \frac{V_L}{4L}T_s$$

Assuming for convenience that the capacitance of the snubber capacitor $= 2C$, the voltage across the capacitor C_1 is given by

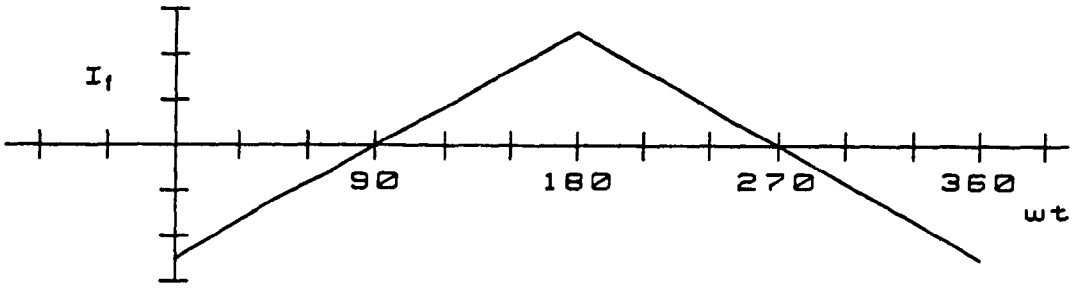


Fig. 4.5: High frequency transformer primary current (I_f) at no load.

$$V_{c1}(t) = \frac{1}{2C}\int_0^t I_f(0)dt$$

$$= \frac{1}{8LC} V_L T_s t \tag{4.3}$$

The time required to charge the capacitor C_1 to the dc link voltage V_L is given by

$$t = \frac{8LC}{T_s} \text{ secs.} \tag{4.4}$$

The maximum time available to charge the capacitor C_1 is $\frac{T_s}{4}$

$$t \leq \frac{T_s}{4} \tag{4.5}$$

Assuming that the current through capacitor C_1 during commutation is not constant, then the equivalent circuit of the commutation is shown in Fig. 4.6. The voltage equation may be written as

$$V_L = \frac{1}{2C}\int I_f(t)dt + \frac{1}{2C}\int I_f(t)dt + L\frac{dI_f(t)}{dt}$$

and

$$\frac{I_f(t)}{C} + L\frac{d^2 I_f(t)}{dt^2} = 0$$

The solution of the above equation is given by

$$I_f(t) = A\cos(\omega_n t) + B\sin(\omega_n t)$$

where

$$\omega_n = \frac{1}{\sqrt{LC}}$$

At the beginning of the commutation

$$I_f(t) = I_f(\frac{T_s}{2}) = \frac{V_L}{4L} T_s$$

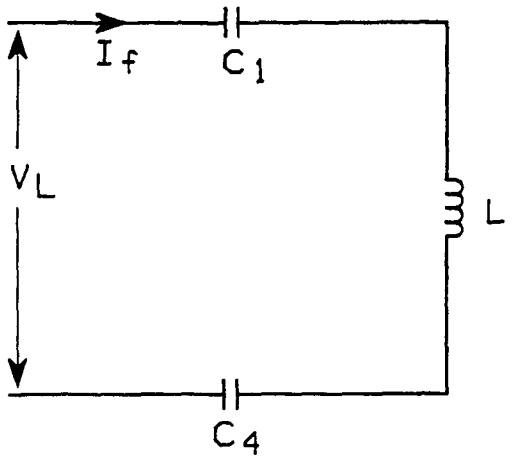


Fig. 4.6: Equivalent circuit during turning-off of a transistor.

$$\frac{dI_f(t)}{dt} = 0$$

and

$$A = \frac{V_L}{4L} T_s \quad ; B = 0$$

$$I_f(t) = \frac{V_L}{4L} T_s \cos(\omega_n t) \tag{4.6}$$

The voltage across the capacitor C_1 is given by

$$V_{c1}(t) = \frac{1}{2C} \int_0^t I_f(t)dt$$

$$= \frac{V_L \omega_n}{8} T_s \sin(\omega_n t) \tag{4.7}$$

The time required to charge the capacitor C_1 to the dc link voltage, V_L, is given by

$$t = \frac{1}{\omega_n} \sin^{-1}\left(\frac{8}{\omega_n T_s}\right) \tag{4.8}$$

and

$$\frac{\omega_n}{f_s} \geq 8 \tag{4.9}$$

Using Eqns. (4.4) and (4.8) the theoretical time required to charge the capacitor C_1 for the constant current case is compared with the actual current when L has a value of 500 μH in Fig. 4.7. For smaller values of the snubber capacitor, it is quite reasonable to assume a constant current during commutation. However, at higher values of snubber capacitance this assumption is not valid.

In order to satisfy the conditions in Eqns. (4.5) and (4.9) the maximum value of the snubber capacitor C is a function of operating frequency and HFT inductance L. The relationship between the inverter operating frequency, the HFT inductance L, and the snubber capacitor C, is shown in Fig. 4.8 for

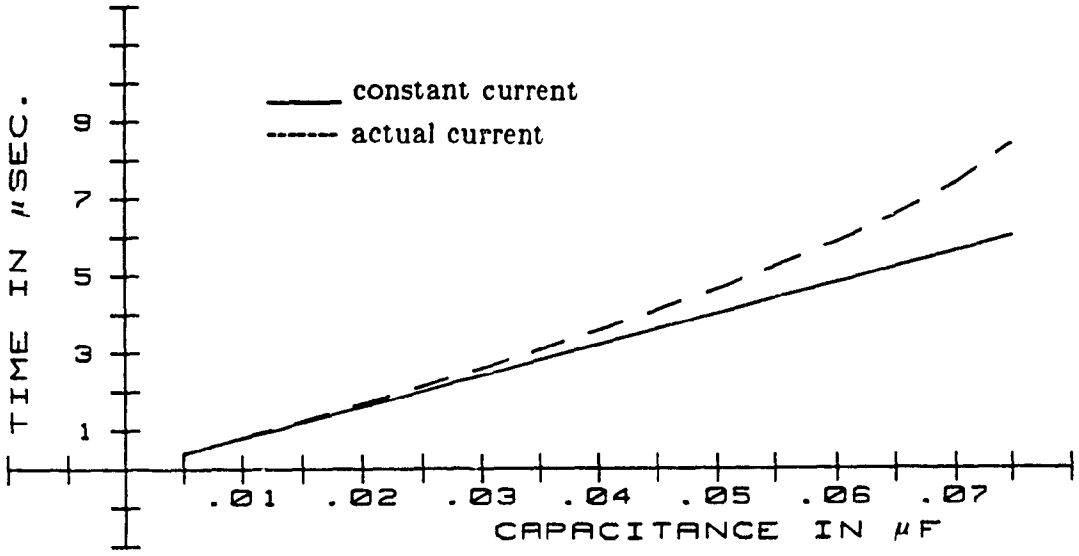


Fig. 4.7: Snubber capacitor versus dead time between inverter complementary switches gating signals at 20 kHz.

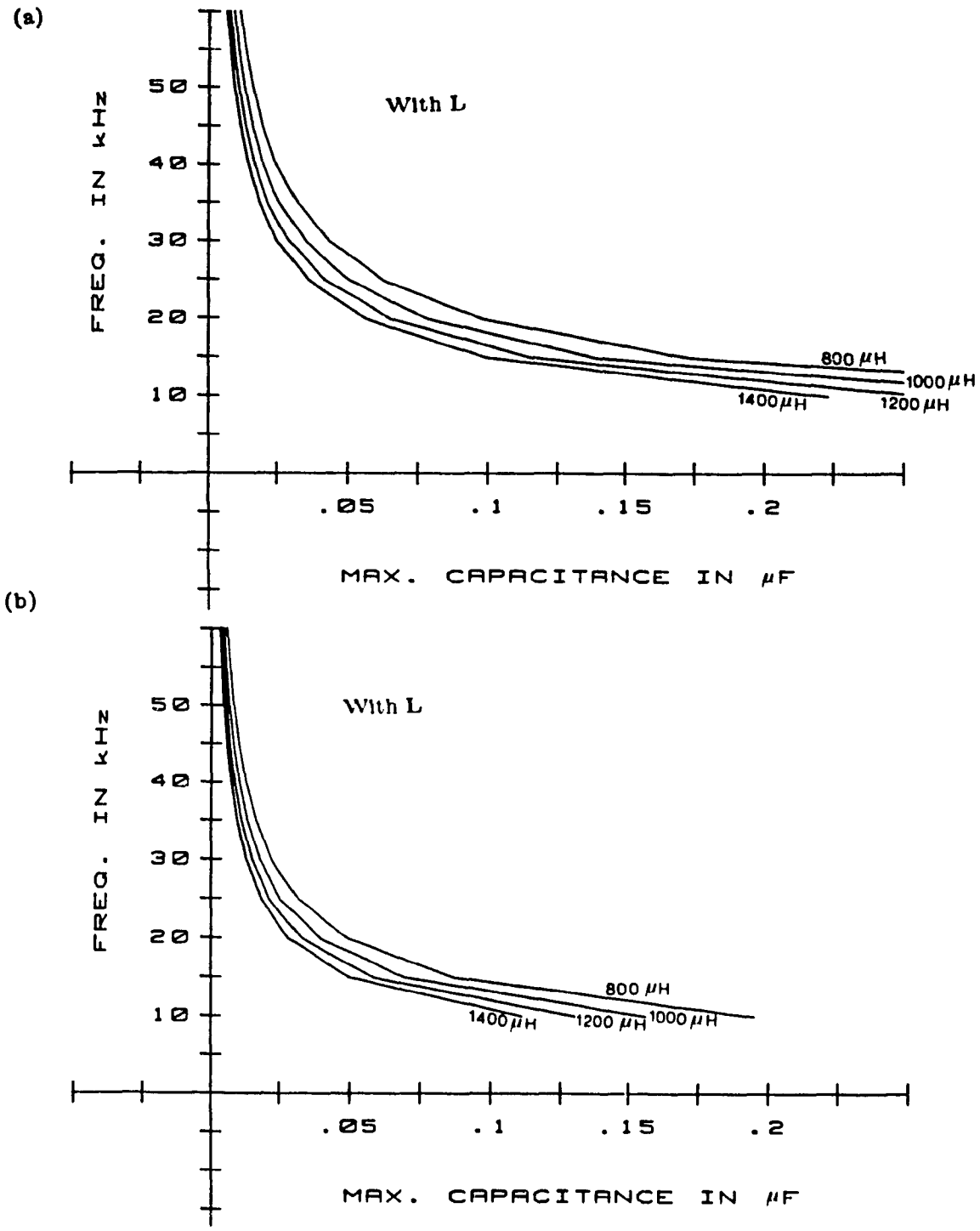


Fig. 4.8: Maximum snubber capacitance versus inverter operating frequency
(a) Constant current during commutation.
(b) Actual current during commutation.

both the constant current and actual current.

4.2.2 Output Filter

In Fig. 4.1 the high-frequency inverter operates at slightly less than 50-percent duty cycle under varying input voltage and load conditions. Therefore the output filter is designed assuming 47-percent duty cycle of the inverter switches. The respective output voltage waveform at the input of the output filter is shown in Fig. 4.9. Also, the equivalent circuit for the output filter design is shown in Fig. 4.9(c). Moreover, Fig. 4.9(b) shows the theoretical waveform of the filter inductor current (I_s). From Fig. 4.9(b) it follows that the value of the average peak to peak current I_s ripple is given by

$$\overline{\Delta I_s} = \frac{V_L - V_s}{L_s} t_{on} = \frac{0.06}{L_s} t_{on}$$

$$= \frac{0.06}{L_s} 0.94 * \frac{T_s}{2}$$

where T_s is the inverter operating time period. By further assuming that $\overline{\Delta I_s}$ = 10-percent current ripple, the value of the filter inductor L_s is given by

$$L_s = \frac{0.0283}{\overline{\Delta I_s}} T_s$$

Therefore, the second harmonic (i.e., twice the inverter operating frequency) ripple current value through the filter inductor becomes

$$I_{s,2} = 0.1414 \quad pu$$

and assuming the ripple voltage across the filter capacitor (C_s) $\leq$ 0.1 percent the value of the filter capacitor is given by

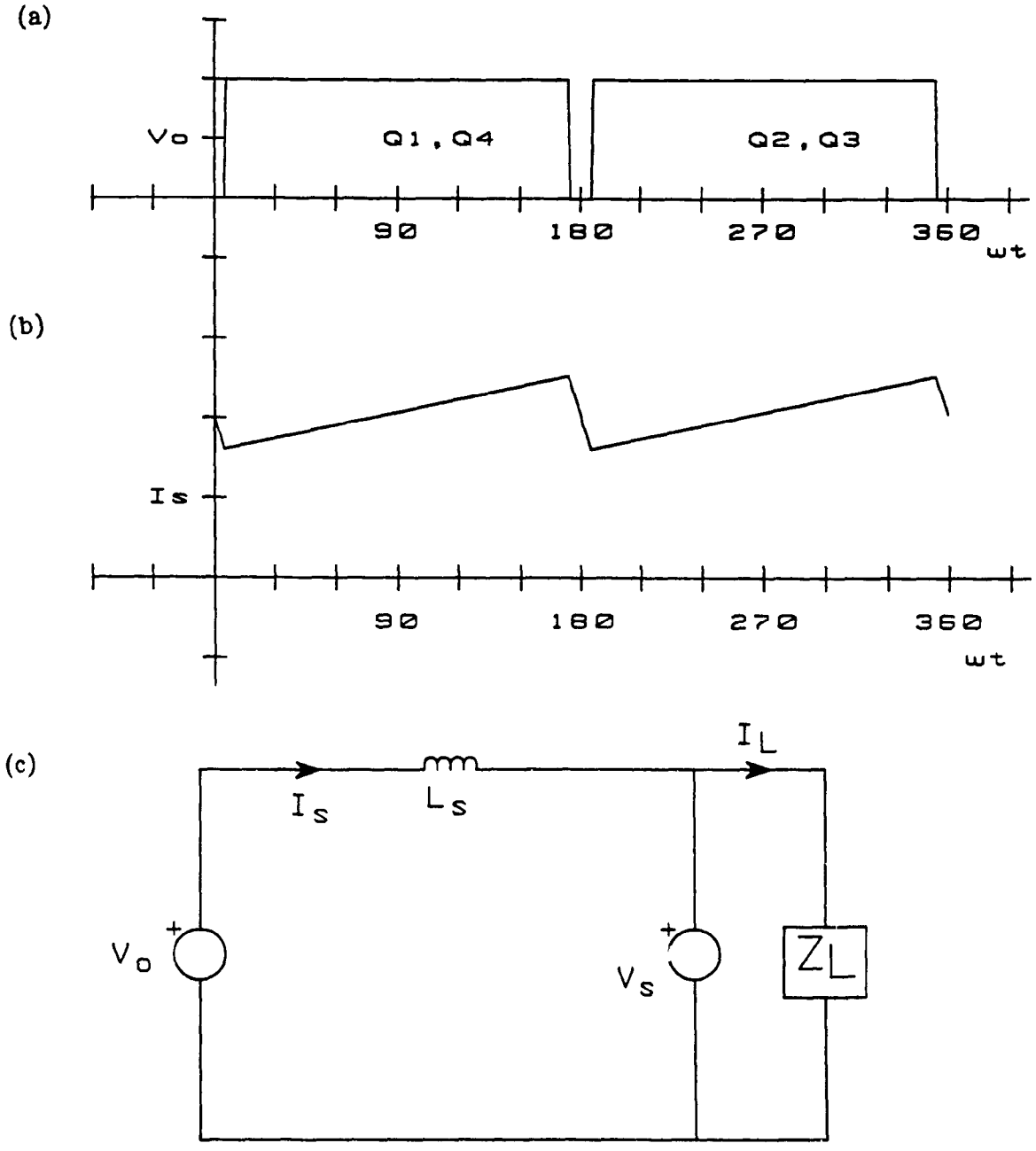


Fig. 4.9: Simulated waveforms and the equivalent circuit for the output filter design

(a) Converter output voltage before filter inductor (V_0).

(b) Converter output filter inductor current (I_s).

(c) Equivalent circuit for the output filter design.

$$C_s = \frac{0.1414 * 100}{2 * \sqrt{2} * 1.0 * 0.1} = 50.0 \ pu$$

It is noted that the 1.0 pu frequency is the operating frequency of the inverter.

4.2.3 Inverter Input Filter

Neglecting the ripple of current, I_s, and the high frequency transformer leakage inductance, the inverter input current, I_{in}, shown in Fig. 4.10(b) is given by

$$I_{in}(\omega t) = S(\omega t) * I_s(\omega t)$$

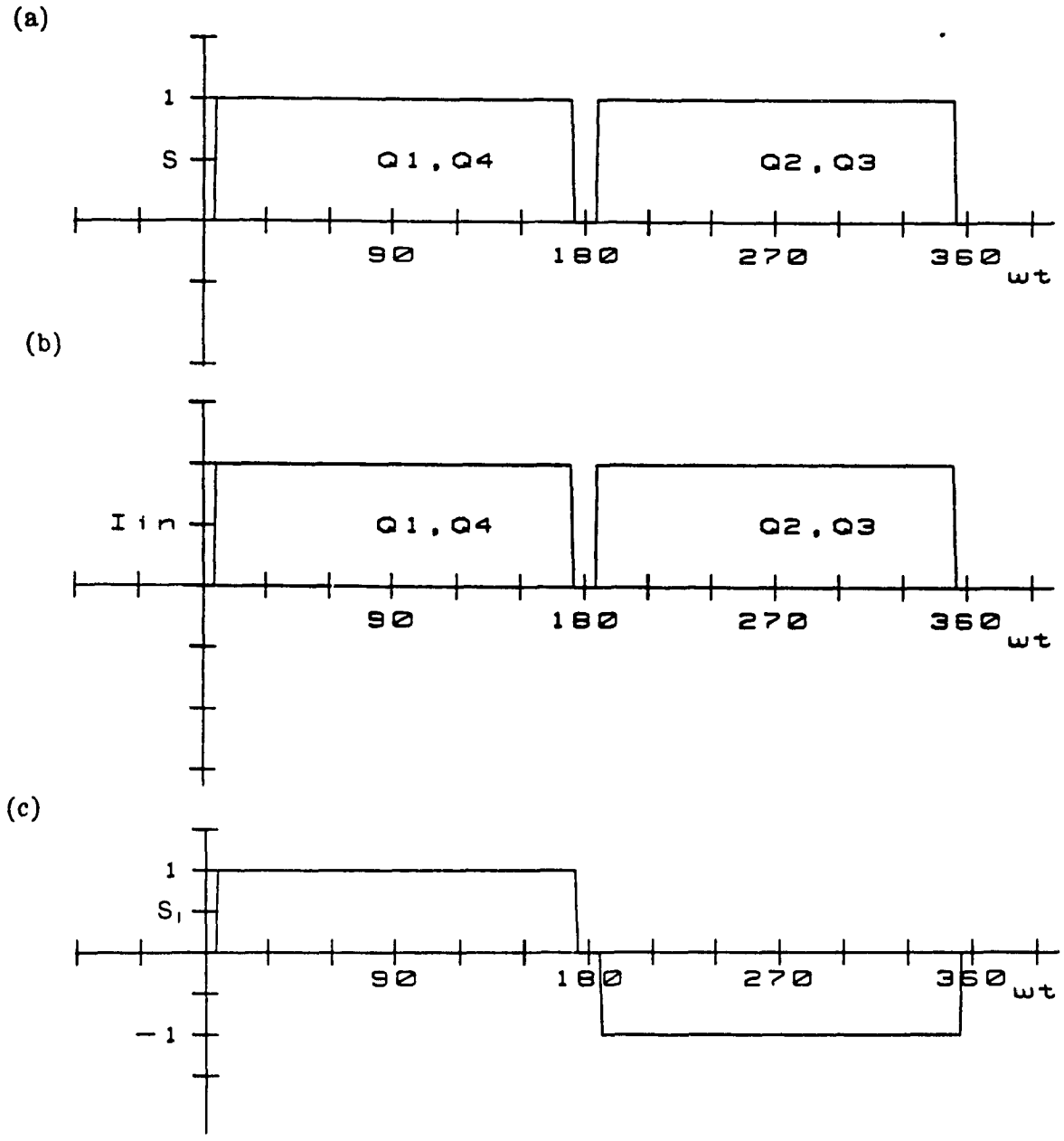
where $S(\omega t)$ is the overall switching function of the high frequency inverter and rectifier stages shown in Fig. 4.10(a). Therefore the dominant harmonic component (twice the inverter operating frequency) of the inverter input current value is given by

$$I_{in,2} = 0.1193 \ pu \tag{4.10}$$

In Fig. 4.1 considering the inverter input current (I_{in}) the equivalent circuit for the dc link filter design is shown in Fig. 4.10(f). In Fig. 4.10(f) the dominant frequency component of I_{db} is 120 Hz and the dominant frequency of I_{in} is twice the inverter operating frequency. Therefore, the amplitude the 120 Hz voltage harmonic component across the filter capacitor is given by

$$V_{L,2} = \frac{I_{db,2}}{2\omega C_o} \tag{4.11}$$

and the amplitude of the 40 kHz voltage harmonic component (assuming 20 kHz inverter operating frequency) across the filter capacitor is


(a)
1
S
Q1, Q4
Q2, Q3
90
180
270
360
ωt
(b)
Iin
Q1, Q4
Q2, Q3
90
180
270
360
ωt
(c)
1
S1
90
180
270
360
ωt
−1

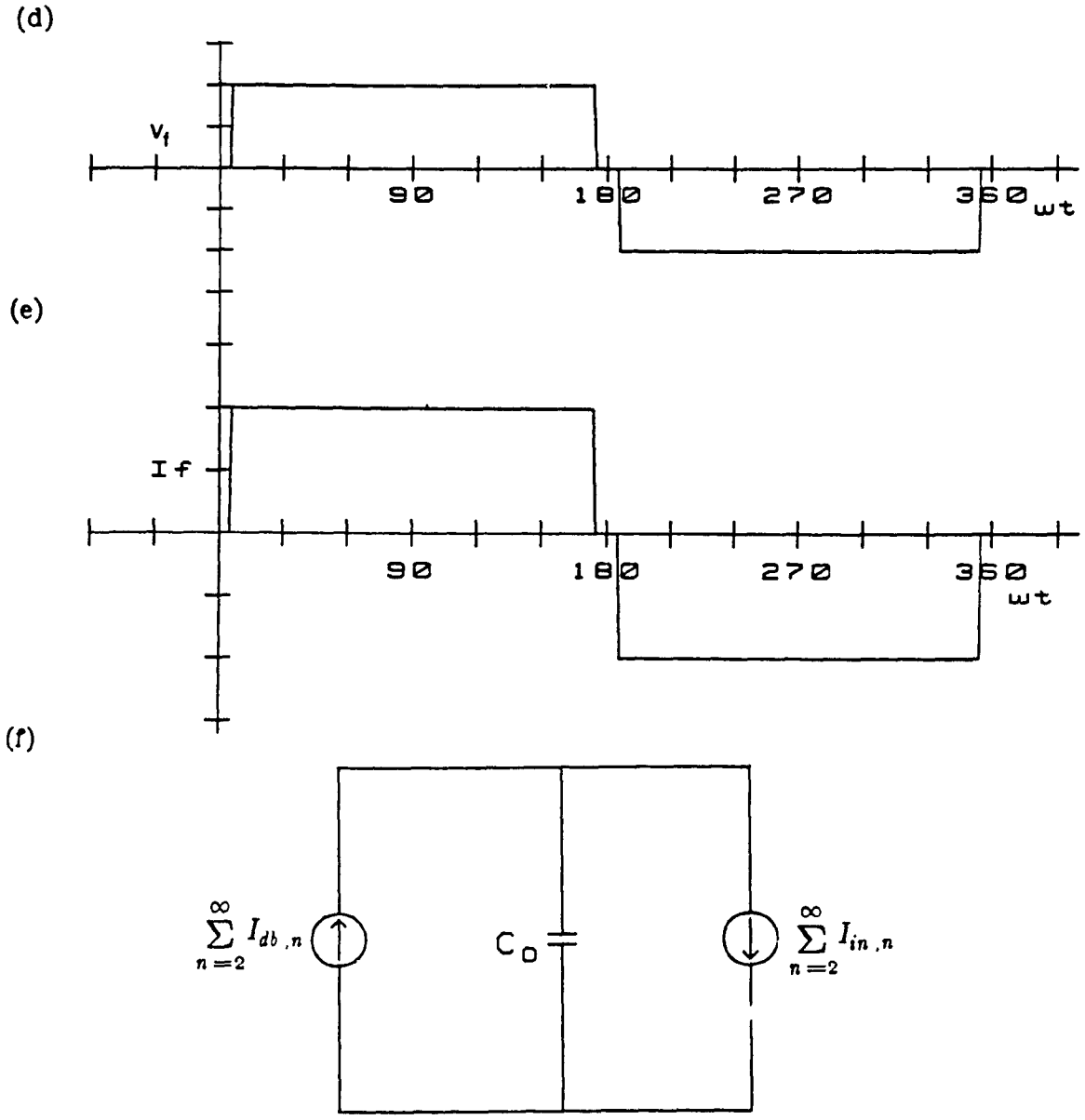


Fig. 4.10: Proposed inverter and high frequency link simulated waveforms

(a) Overall switching function ($S(\omega t)$)
(b) Inverter input dc current ($I_{in}(\omega t)$)
(c) Inverter switching function ($S_i(\omega t)$)
(d) High frequency transformer primary voltage ($V_f(\omega t)$)
(e) High frequency transformer primary current ($I_f(\omega t)$)
(f) Equivalent circuit for dc link filter design

$$V_{L,2in} = \frac{I_{in,2}}{666.66\omega C_o} \tag{4.12}$$

From Eqns. (4.11) and (4.12) the rms ripple voltage across the dc filter capacitor becomes

$$V_{L,ripple} = \frac{1}{\sqrt{2}}\sqrt{V^2_{L,2} + V^2_{L,2in}} \tag{4.13}$$

Moreover, the allowable inverter input voltage ripple can be defined by

$$Ripple\ \% = \frac{100 * V_{L,ripple}}{V_{L,o}} \tag{4.14}$$

From Eqns. (4.11)-(4.14) the value of the filter capacitor is given by

$$C_o = \frac{100 * \sqrt{I^2_{db,2} + \frac{I^2_{in,2}}{333.33^2}}}{\sqrt{2} V_{L,o} * 2 * \omega (ripple\ \%)} \tag{4.15}$$

In Fig. 4.1 at 1.0 pu dc bus voltage the value of 120 Hz ripple component ($I_{db,2}$) for the proposed active filter topology becomes

$$I_{db,2} = \frac{0.643}{1.556} = 0.413\ \ pu \tag{4.16}$$

Using Eqns. (4.10), (4.15) and (4.16) the value of the capacitor (C_o) for 5% ripple voltage (V_L) becomes

$$C_o = \frac{100 * \sqrt{(0.413)^2 + (\frac{0.1193}{333.33})^2}}{\sqrt{2} * 2 * 5} = 2.92\ \ pu \tag{4.17}$$

It is noted that the C_o value found in Eqn. (4.17) is approximately same as the respective C_o value found in Eqn. (3.18) for the proposed active filter topology. Therefore the influence of high frequency inverter on the value of C_o is negligible.

4.2.4 High Frequency Transformer

The high frequency link line voltage shown in Fig. 4.10(d) is given by

$$V_f(\omega t) = V_L(\omega t) * S_i(\omega t)$$

where $S_i(\omega t)$ is the inverter switching function shown in Fig. 4.10(c). Similarly, the simulated high frequency link line current, I_f, is shown in Fig. 4.10(e).

Regarding Fig. 4.1 the high frequency link line voltage, V_f, and current, I_f, are shown in Fig. 4.10(d) and (e). The rms values of voltage V_f and I_f are given by

$$V_{f\,(rms)} = 1.0 \ \ pu$$

$$I_{f\,(rms)} = \frac{\sqrt{2}}{\sqrt{2}} = 1.0 \ \ pu$$

Therefore the total volt-ampere (VA) rating of the transformer = 1.0 pu

4.2.5 Inverter/Rectifier Component Ratings

In Fig. 4.1, the high frequency inverter operates at slightly less than 50-percent duty cycle. The inverter input voltage (V_L) is maintained constant by the front-end rectifier converter under varying source voltage and load conditions. Consequently the peak value of the square current pulses through the inverter switches $I_{in\,(peak)}$ = 1.05 pu (assuming 10-percent current I_s ripple).

Average current through the inverter switches = 0.5 pu

RMS current through the inverter switches (I_{rms}) = 0.707 pu

Peak forward voltage (V_{sw}) = 1.0 pu

$$Total\ inverter\ switch\ VA = \sum_{k=1}^{4} I_{rms,k} * V_{sw,k}$$

$$= 4 * 0.707 * 1.0 = 2.828\ pu$$

The peak value of the square current pulses through the output high frequency rectifier diode is 1.05 pu (assuming 10-percent current I_s ripple).

Average current through the output rectifier diode switches = 0.5 pu

RMS current through the output rectifier diode switches = 0.707 pu

Peak forward voltage = 1.0 pu

4.2.6 Design Example

In order to illustrate the significance and to facilitate the understanding of the theoretical results obtained in the previous sections, the following example is given. The High Frequency Inverter has the following parameters:

High frequency transformer leakage and magnetizing inductances (L) = 1274.5 μh

Operating frequency f_s = 20 kHz

(1) Assuming constant transformer magnetizing current during commutation

From Fig. 4.8(a) the theoretical maximum possible value of capacitor C = 0.061 μ F.

Maximum value of snubber capacitor 2C = 0.1226 μ F.

Choosing the snubber capacitor 2C = 0.01 μ F or C = 0.005 μ F;

the dead time required between the two complementary gating signals is (Eqn.(4.4))

$$t = \frac{8LC}{T_s}$$

$$= 1.0196 \mu sec. \qquad (4.18)$$

(ii) Assuming the current is not constant during commutation

From Fig. 4.8(b) the theoretical maximum possible value of capacitor C = 0.03065 μ F.

Maximum value of snubber capacitor 2C = 0.061 μ F.

Choosing the snubber capacitor 2C = 0.01 μ F or C = 0.005 μ F;

the dead time required between the two complementary gating signals is given by the Eqn.(4.8),

$$t = \frac{1}{\omega_n} \sin^{-1} \left[\frac{8 f_s}{\omega_n} \right]$$

$$= 1.0196 \ \mu \ seconds. \qquad (4.19)$$

4.2.7 Experimental Results

In order to verify the predicted results a 7 kW experimental converter was implemented using IRFK4H 451 power MOSFET transistors with the following circuit parameters.

High frequency transformer leakage and magnetizing inductances (L) = 1274.5 μH

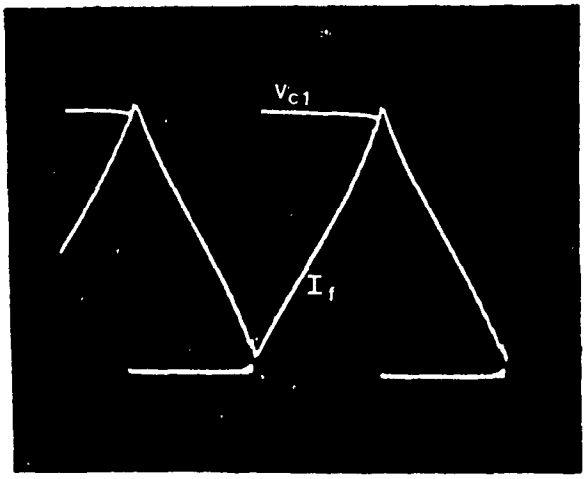
Operating frequency of the inverter (f_s) = 20 kHz

Snubber capacitor 2C = 0.01 μ F

DC bus Voltage V_L = 260 volts

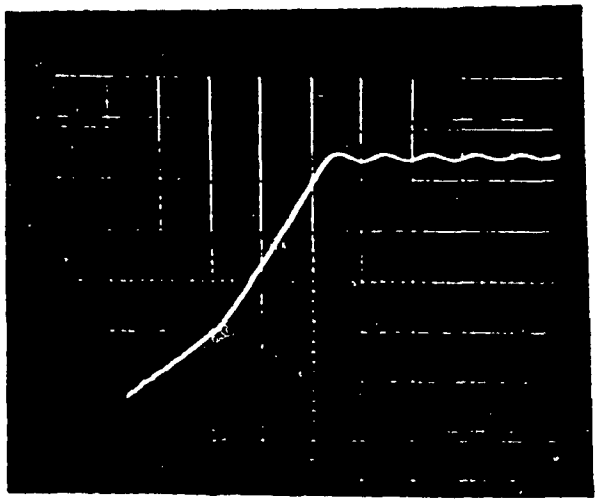
The experimental waveforms are shown in Fig. 4.11. In particular, evaluation of Fig. 4.11(b) shows that the time required to charge the snubber capacitor

(a)



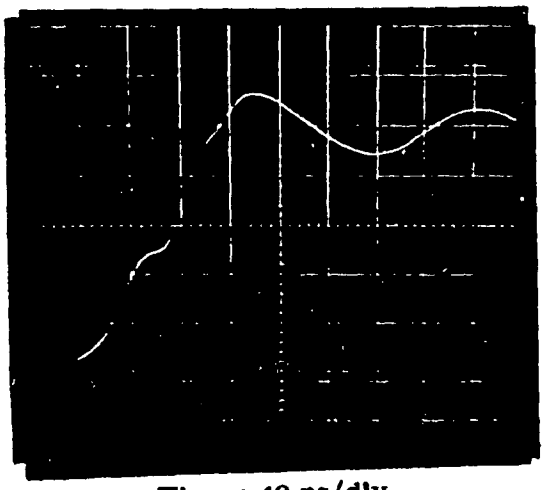
Time : 10 μs/div.
Amp. : 50 V/div.
1 A/div.

(b)



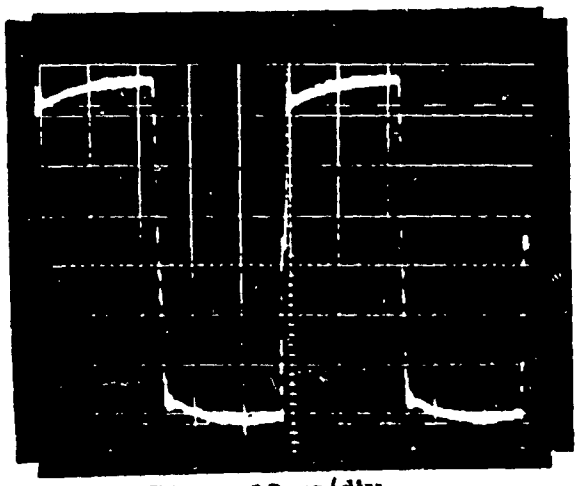
Time : 0.2 μs/div.
Amp. : 50 V/div.

(c)



Time : 40 ns/div.
Amp. : 50 V/div.

(d)



Time : 10 μs/div.
Amp. : 10 A/div.

Fig. 4.11: Experimental waveforms of the proposed inverter operation

(a) Voltage across the transistor (V_{c1}) and the high frequency transformer primary current (I_f) at no load.

(b) Voltage across the transistor (V_{c1}) during turn-off at no load.

(c) Voltage across the transistor (V_{c1}) during turn-off at rated load.

(d) High frequency transformer primary current at rated load.

to the dc link voltage, V_L, during turning off ($\approx 1\mu$sec.) at no load is in close agreement with the values predicted in the design example (Eqns. (4.18) and (4.19)). From the specification sheet of the IRFK4H 451 the fall time, t_f, of the transistor is 70 ns. Moreover, the voltage rise across the transistor during turn-off at rated load is shown in Fig. 4.11(c). Further, the voltage across the transistor at the end of the 70 nsec. period is approximately 110 volts. Therefore, the transistor turn-off switching losses at rated load are approximately 123.2 10^{-6} Joules /turn-off. Moreover, the transistor turn-off switching losses can be decreased considerably for any output power level, by choosing the proper value of the snubber capacitor and the dead time between the complementary power semiconductor switches.

4.2.8 Conclusions

In this section single-phase high frequency link in which the PWM constant frequency inverter section is always operating in the current lagging mode have been presented. These topologies allow the safe use of a lossless single-capacitor snubber from zero to rated load power conditions. Finally, the theoretical results have been verified experimentally.

4.3 High Frequency Link with Suppressed dc Components

The advantages of operating the inverter section in the current lagging mode are discussed in section 4.2. Application of the front-end boost active rectifier topology (discussed in section 3.3) in SMR converters controls the output voltage from maximum to minimum load variation while ensuring the

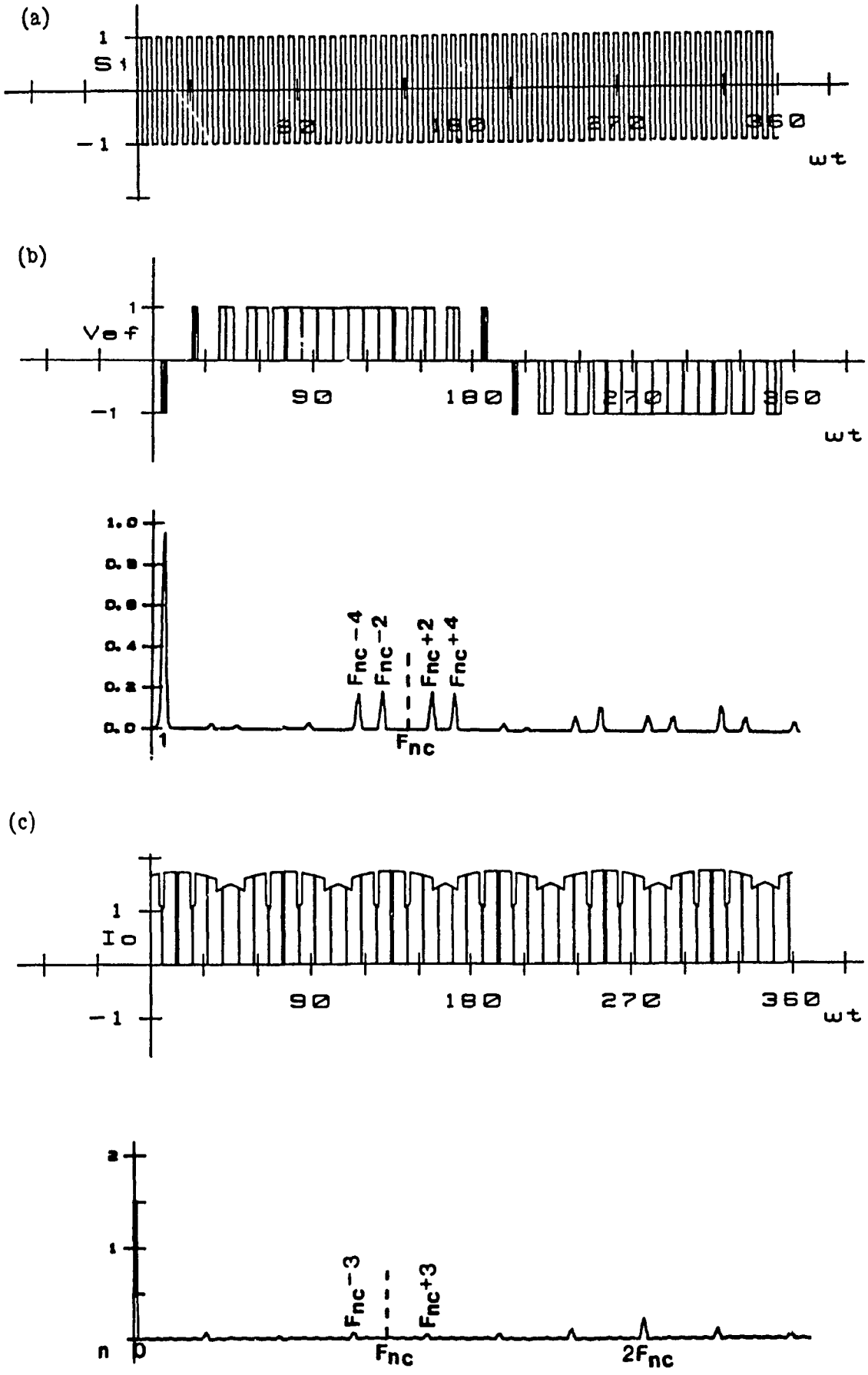
critical current lagging operation of the inverter. However, application of the front-end synchronous rectifier discussed in section 3.4 controls the output voltage from zero to rated load conditions. The proposed three-phase fed single-phase high frequency link converter (Fig. 4.2) consists of two main power conversion stages. The first stage is a PWM rectifier that employs the harmonic injection sinusoidal PWM (HISPWM) control method [31,32] for elimination of the input line current unwanted harmonic components. The HISPWM control technique was chosen because it can provide a dc link current (I_o) with the minimum of unwanted harmonic components [32] which in turn can prevent the generation of unwanted harmonic components in the isolation transformer primary current (I_f). The second stage consists of a high-frequency ($\geq$ 20kHz) fixed duty cycle single-phase inverter that converts the PWM rectifier dc output current into a High-Frequency ac current, a high frequency transformer, a high frequency rectifier, an output filter, and a load. This essentially reduces the size and cost of the isolation transformer considerably. Simulated waveforms of the proposed HFL converter are shown in Fig. 4.12.

4.3.1 Principles of Operation

The operating principles of the front-end synchronous rectifier are discussed in section 3.4 and the relevant aspects are presented here.

(i) Real power flow is in principle bilateral, going from E_{an} to V_{en} into the for lagging δ and vice-versa for leading δ. This power is given by the well known from synchronous machine theory expression

$$P = \frac{EV_{en.1(rms)}}{X_{L_{ac}}} \sin\delta \qquad (4.20)$$


(a)
1
S1
-1
90
180
270
360
ωt
(b)
1
Vef
-1
90
180
270
360
ωt
1.0
0.8
0.6
0.4
0.2
0.0
1
Fnc-4
Fnc-2
Fnc
Fnc+2
Fnc+4
(c)
1
Io
-1
90
180
270
360
ωt
2
1
n
0
Fnc-3
Fnc
Fnc+3
2Fnc

(d)

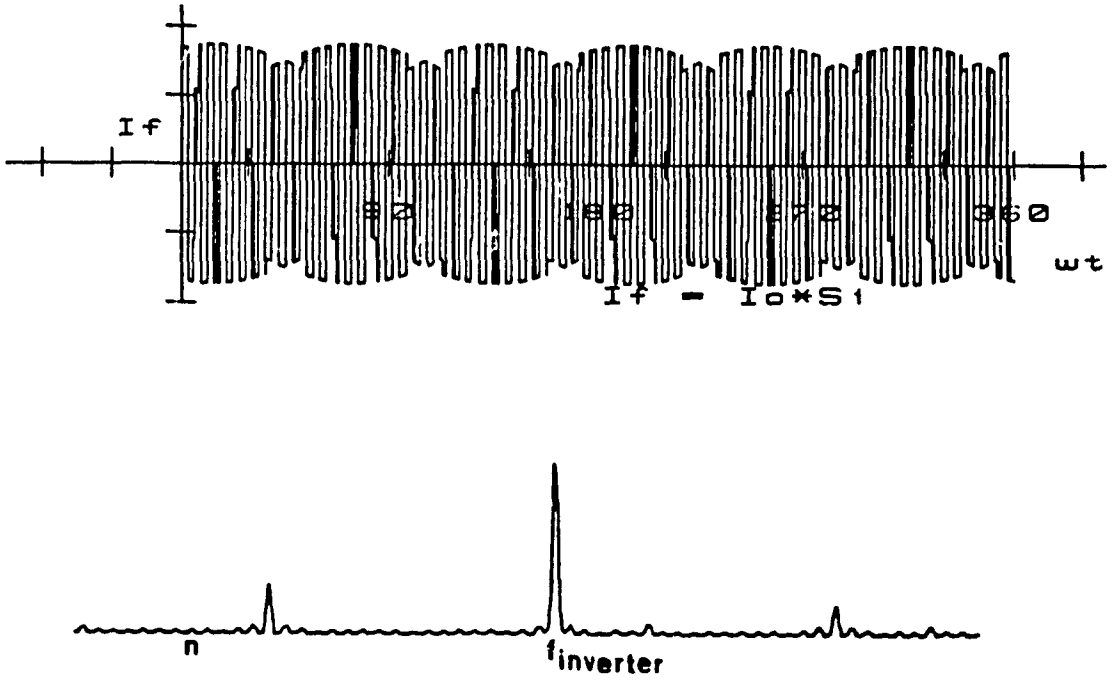


Fig. 4.12: Proposed synchronous rectifier fed HFL converter simulated waveforms.

(a) High frequency inverter switching function (S_1).

(b) PWM rectifier input line-to-line voltage (V_{ef}) and its frequency spectrum.

(c) DC link current (I_o) and its respective frequency spectrum.

(d) Primary current of the isolation transformer (I_f) and its respective frequency spectrum.

(11) For the special case of $\delta = 0^o$,the input power factor angle ϕ becomes 90^o and consequently only reactive power flows (excluding losses).

4.3.2 Control Principles

In Figs. 4.2 and 4.12(b) the rms value of the fundamental component of V_{en} is given by

$$V_{en,1(rms)} = \left[\frac{V_{s,o}}{\sqrt{3}}\right]\left[\frac{N_p}{N_s}\right]\left[\frac{M_f}{\sqrt{2}}\right]$$

$$= \frac{V_{s,o} M_f \alpha}{\sqrt{2}\sqrt{3}} \tag{4.21}$$

where,

$$\alpha = \frac{N_p}{N_s} \tag{4.22}$$

Furthermore, following the procedure described in section 3.4.2 yields

$$\frac{\sqrt{2}\sqrt{3}}{\alpha M_f} \leq V_{s,o} \leq \frac{\sqrt{2}\sqrt{3}}{\alpha M_f}\sqrt{1 + X^2_{L_s}} \quad pu \tag{4.23}$$

$$for \quad 0 \leq P \leq 1 \quad pu \tag{4.24}$$

A block diagram of the overall unit including the control loops required to ensure unity power factor and output voltage regulation is shown in Fig. 4.13. The control circuitry of Fig. 4.13 can be simplified by eliminating the unity power factor control loop (dotted line loop) at the cost of slightly reducing the input power factor as shown in section 3.4.2.

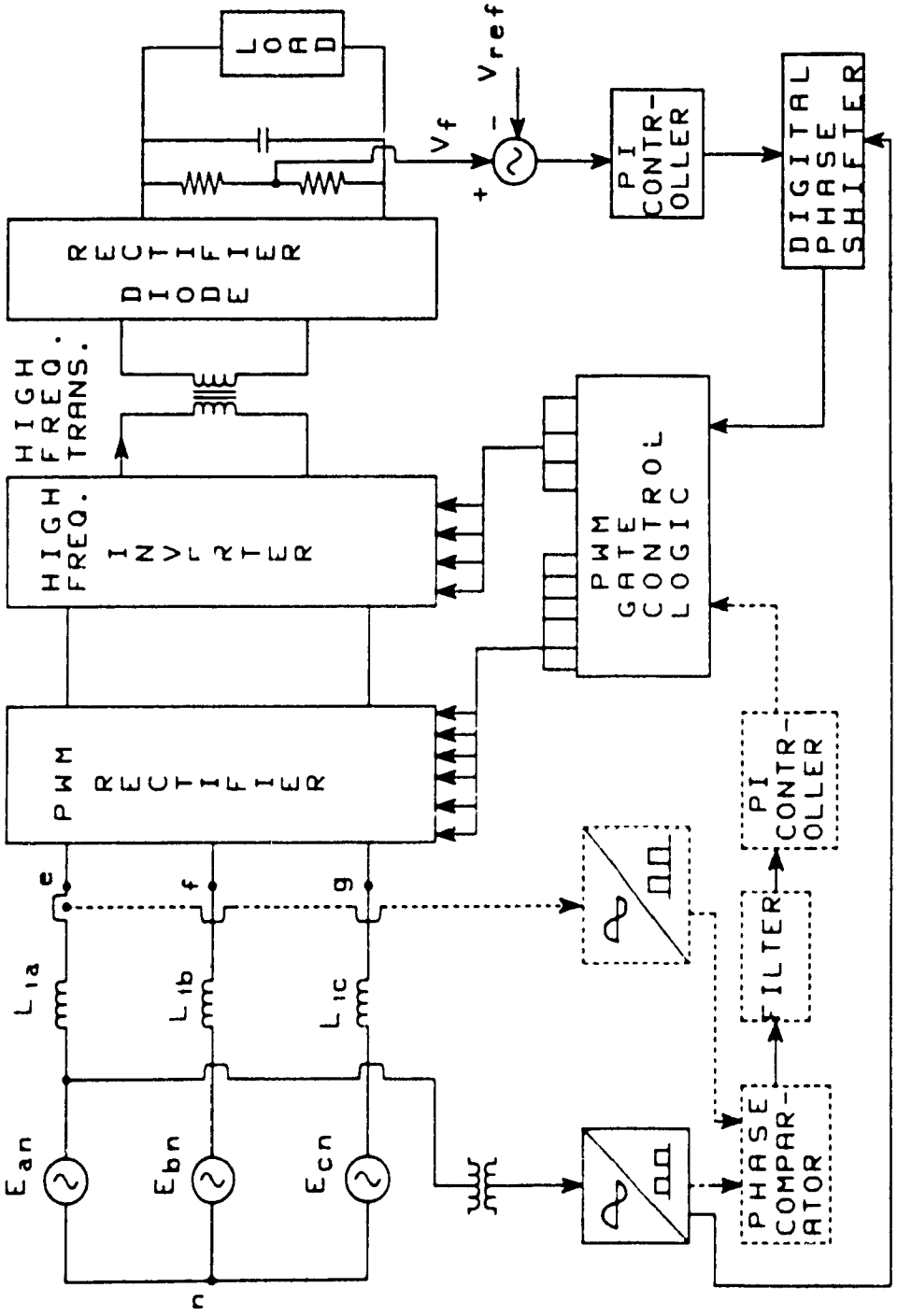


Fig. 4.13: Block diagram of the overall SMR unit which includes the control loops required to ensure unity input power factor and output voltage regulation.

4.3.3 SMR Converter

In this section the proposed HFL converter is analyzed under steady-state conditions. The derived expressions are subsequently used to obtain the information necessary for proper HFL converter design. The converter is analyzed using the following assumptions:

(1) All power switching devices are ideal and diodes forward drop and reverse leakage currents are negligible.

(2) The filter components are ideal.

(3) The load voltage is ripple free.

Moreover, for the rated input rms voltage E and rated input rms current, $I_{ia,1(rms)}$ values, it is assumed that

$$E = 1\ pu\ \ Volts \tag{4.25}$$

$$I_{ia,1(rms)} = 1\ pu\ \ Amps \tag{4.26}$$

where

$$1\ pu\ RMS\ current = \frac{rated\ output\ power}{3\ (Efficiency)\ (RMS\ value\ of\ the\ ac\ source\ phase\ voltage)} \tag{4.27}$$

keeping in mind that power factor is almost unity.

Assuming that the THD of the input line current is $\leq$ 5-percent (Fig. 4.2) the converter output current before filtering is given by

$$I_s(\omega t) = \left[\sum_{k=0}^{2} S_d(\omega t - \frac{2k\pi}{3}) I_{ia,1} \sin(\omega t - \frac{2k\pi}{3} - \phi)\right] * \left[\alpha S_i(\omega t) S_{dr}(\omega t)\right] \tag{4.28}$$

where

$S_d(\omega t)$ is the PWM rectifier switching function shown in Fig. 3(e) and its harmonic coefficients are given by

$$S_d(\omega t) = \sum_{n=1,5,7}^{\infty} A_n \sin(n\omega t) \tag{4.29}$$

$S_i(\omega t)$ is the High Frequency Inverter Switching function shown in Fig. 4.3(f) (Fixed Duty cycle = 50-percent) and its harmonic coefficients are given by

$$S_i(\omega t) = \frac{4}{\pi} \sum_{n=1,3,5}^{\infty} \frac{1}{n} \sin(n\omega_s t) \tag{4.30}$$

ω_s is the inverter stage angular frequency

$S_{dr}(\omega t)$ is the high frequency diode rectifier switching function which is the same as the switching function of the inverter stage.

Since the High Frequency Inverter stage operates at a fixed 50-percent duty cycle

$$S_i(\omega t) S_{dr}(\omega t) = 1 \tag{4.31}$$

Also, the frequency spectrum of the PWM rectifier switching function, $S_d(\omega t)$ is given in Table 3.2.

Substituting Eqns. (4.29) and (4.31) into (4.28) and assuming that the HFL converter input line currents are balanced

$$I_s(\omega t) = \sum_{k=0}^{2} \Big[A_1 \sin(\omega t - \frac{2k\pi}{3}) + A_{f_{nc}-4} \sin((f_{nc}-4)\omega t - \frac{2k\pi}{3})$$
$$+ A_{f_{nc}-2} \sin((f_{nc}-2)\omega t - \frac{2k\pi}{3})$$
$$+ A_{f_{nc}+2} \sin((f_{nc}+2)\omega t - \frac{2k\pi}{3})$$
$$+ A_{f_{nc}+4} \sin((f_{nc}+4)\omega t - \frac{2k\pi}{3}) + \ldots \Big]$$

$$* \alpha \left[I_{ia,1} \sin(\omega t - \frac{2k\pi}{3} - \phi) \right] \tag{4.32}$$

As $I_s(\omega t)$ has harmonic components which are multiples of six of the fundamental (i.e. 6,12,18,24,.....) Eqn. (4.32) becomes

$$\begin{aligned} I_s(\omega t) = {} & \frac{3\alpha A_1 I_{ia,1}}{2} \cos\phi \\ & - \left(\frac{3\alpha A_{f_{nc}-4} I_{ia,1}}{2} - \frac{3\alpha A_{f_{nc}-2} I_{ia,1}}{2} \right) \cos((f_{nc}-3)\omega t + \phi) \\ & - \left(\frac{3\alpha A_{f_{nc}+2} I_{ia,1}}{2} - \frac{3\alpha A_{f_{nc}+4} I_{ia,1}}{2} \right) \cos((f_{nc}+3)\omega t + \phi) \\ & - \frac{3\alpha A_{2f_{nc}-7} I_{ia,1}}{2} \cos((2f_{nc}-6)\omega t - \phi) \\ & + \frac{3\alpha A_{2f_{nc}-5} I_{ia,1}}{2} \cos((2f_{nc}-6)\omega t + \phi) \\ & - \left(\frac{3\alpha A_{2f_{nc}-1} I_{ia,1}}{2} - \frac{3\alpha A_{2f_{nc}+1} I_{ia\,1}}{2} \right) \cos(2f_{nc}\omega + \phi) \\ & - \frac{3\alpha A_{2f_{nc}+5} I_{ia,1}}{2} \cos((2f_{nc}+4)\omega t + \phi) \\ & + \frac{3\alpha A_{2f_{nc}+7} I_{ia,1}}{2} \cos((2f_{nc}+6)\omega t + \phi) \end{aligned} \tag{4.33}$$

where $f_{nc} = 21,27,33 \ldots.$

A close examination of Eqn. (4.33) reveals that the (f_{nc}-3) and (f_{nc}+3) harmonic components cancel each other thus providing a harmonic free dc link current. Also from Eqn. (4.33) it can be observed that the dc and dominant harmonic components of $I_s(\omega t)$ under worst operating condition (M_f =.7) are given by

$$\begin{aligned} I_{s,o} &= \frac{3\alpha A_1 I_{ia,1}}{2} \cos\phi = (\frac{3\alpha}{2})(M_f)(\sqrt{2})(\approx 1) \\ &= 2.1 M_f \alpha \end{aligned} \tag{4.34}$$

$$I_{s,2f_{sc}} = \frac{3\alpha(-A_{2f_{sc}-1} + A_{2f_{sc}+1}) I_{ia,1}}{2}$$

$$= \frac{3\alpha(\frac{.3 + .3}{.7})\sqrt{2}}{2} = 1.82\alpha \qquad (4.35)$$

Fig. 4.12(c) shows the simulated waveform of the converter output current before filtering and its respective frequency spectrum.

4.3.4 Output Filter

In Fig. 4.12(c) the HFL converter output current, $I_s(\omega t)$, consists of a modulated train of pulses and consequently some form of filtering is necessary to separate the dc component from the undesired harmonic components. Furthermore, the amplitude of the $2f_{nc}$ order voltage harmonic component across the output filter capacitor, C_s, is given by

$$V_{s\,2f_{nc}} = \frac{I_{s\,2f_{nc}}}{2f_{nc}\omega C_s} \qquad (4.36)$$

Moreover, the allowable converter output voltage ripple can be defined by

$$Ripple\ \% = \frac{100 V_{s\,2f_{nc}(rms)}}{V_{s\,o}} \qquad (4.37)$$

Substituting Eqns. (4.35) and (4.37) into (4.36), the value of the output filter capacitance is given by

$$\begin{aligned} C_s &= \frac{I_{s\,2f_{nc}}\,100}{\sqrt{2}(2f_{nc})(\omega)(Ripple\ \%)(V_{s\,o})} \\ &= \frac{(1.82\alpha)100}{\sqrt{2}(2f_{nc})(1)(Ripple\%)(\frac{\sqrt{2}\sqrt{3}}{\alpha M_f})} \quad pu \\ &= \frac{26.3\alpha^2 M_f}{(f_{nc})(Ripple\%)} \quad pu \end{aligned} \qquad (4.38)$$

where

$$1\ pu\ capacitance = \frac{1}{(1\ pu\ frequency)(1\ pu\ impedance)} \tag{4.39}$$

and

$$1\ pu\ angular\ frequency = \omega\ rad/sec \tag{4.40}$$

4.3.5 High Frequency Transformer

In Fig. 4.2 the ohmic isolation transformer primary current is given by

$$\begin{aligned} I_f(\omega t) &= I_o(\omega t) S_1(\omega t) \\ &= \alpha I_s(\omega t) S_1(\omega t) \end{aligned} \tag{4.41}$$

Substituting Eqns. (4.30) and (4.33) into Eqn. (4.41) and ignoring the harmonic components of $I_f(\omega t)$ which have an amplitude less than 5-percent of the fundamental component yields

$$\begin{aligned} I_f(\omega t) \approx \frac{12\alpha}{\pi} \Bigg[& \frac{A_1 I_{1a1}}{4} \left[\sin(\omega_s t + \phi) + \sin(\omega_s t - \phi) \right] \\ & + \frac{(A_{2f_{nc}+1} - A_{2f_{nc}-1}) I_{1a1}}{4} \left[\sin((\omega_s + 2f_{nc}\omega)t + \phi) \right. \\ & \left. + \sin((\omega_s - 2f_{nc}\omega)t - \phi) \right] \Bigg] \end{aligned} \tag{4.42}$$

where ω_s is the inverter stage angular frequency

Fig. 4.12(d) shows the simulated waveforms of the isolation transformer primary current, I_f and its respective spectrum. A close examination of Eqn. (4.42) reveals that the fundamental component of $I_f(\omega t)$ is oscillating at the inverter stage switching frequency, $k\omega$, which can be chosen to be above the audible frequency range ($\geq$ 20kHz). Thus the size and cost of the isolation transformer can be reduced considerably. Moreover, only the major unwanted harmonic component of $I_f(\omega t)$ is oscillating at a frequency $(k \pm 2f_{nc})\omega$ which has an amplitude of 20-percent of the fundamental component.

4.3.6 Component Ratings

From the aforementioned assumptions and derived analytical expressions the voltage and current ratings of the various system components are as follows.

Inductor L_{ia}

Value of L_{ia} :0.1 pu

Rms current $(I_{ia\ rms}) = \sqrt{\sum_{n=1}^{\infty} \left(\frac{I_{ia\ n}}{\sqrt{2}} \right)^2}$: 1.0 pu

Peak current $(I_{ia\ peak}) = \sqrt{\sum_{n=1}^{\infty} I_{ia\ n}^{\ 2}}$: $\sqrt{2}$ pu

Inverter Switch

Average current : 1.0605 pu

RMS current (I_{rms}) : 1.5 pu

Peak current : 2.15 pu

DC Filter Capacitor C_f

Value : Eqn. (4.38)

Rms ripple current : 1.287 pu

Peak voltage : 2.5 pu

The current stresses of the high frequency rectifier diode are same as the inverter switch current stresses. It is noted that the ratio of the rms input current (I_{ia}) to the peak value of the input current is higher in the proposed HFL converter than in the single switch front-end section (from section 3.3.6) for the same inductor value of 0.1 pu. Therefore the proposed converter exhibits a higher power density.

4.3.7 Design Example

In order to illustrate the significance and facilitate the understanding of theoretical results obtained in previous sections the following design example is given. The HFL converter has the following specifications.

- DC load voltage ($V_{L,0}$)= 48V
- DC load current (I_L)= 100A
- AC source rms phase voltage (E) = 120V
- Modulation factor (M_f) = 1
- Supply frequency (f_i) = 60HZ
- Normalized carrier frequency (f_{nc}) = 61
- Load voltage ripple (R%) = 2%
- converter overall efficiency = 85%

Assuming balanced input line currents and using the above specifications

1 pu Volts = 120V

1 pu current = $I_{ia,1(rms)} = \frac{(48)(100)}{(3)(.85)(120)} = 15.7A$

1 pu frequency = $2\pi f_i$ = 377 rad./sec.

1 pu Impedance = $\frac{120}{15.7} = 7.6\Omega$

1 pu capacitance = $\frac{1}{(377)(7.6)} = 3.47 * 10^{-4}$ Farads

Using Eqn. (4.38) output filter capacitor is given by

$$C_s = \frac{26.3 * \alpha^2 * 1}{(61)(2)} \quad pu$$

$$where\ \alpha = \frac{\sqrt{2}\sqrt{3}V_{en(rms)}}{V_{s,o} * M_f} = 6$$

Therefore

$$C_s = 7.76 \text{ pu}$$

or

$$C_s = 7.76 * 3.47 * 10^{-4} = 2690\ \mu F$$

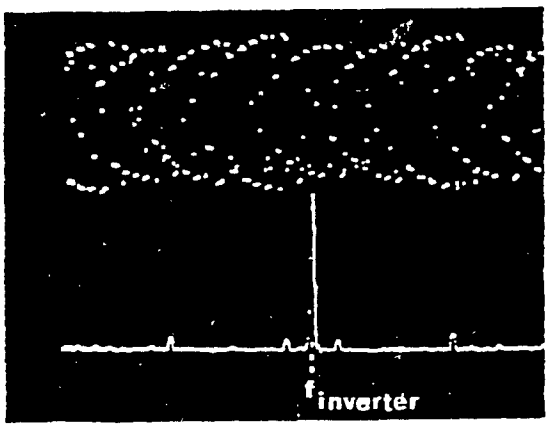
4.3.8 Experimental Results

To verify selected predicted results an experimental 2 kW HFL converter has been implemented using power MOSFETs. Results obtained with this experimental unit are shown in Fig. 4.14. Evaluation of experimental results shows that they are in close agreement with the simulated results shown in Fig. 4.12.

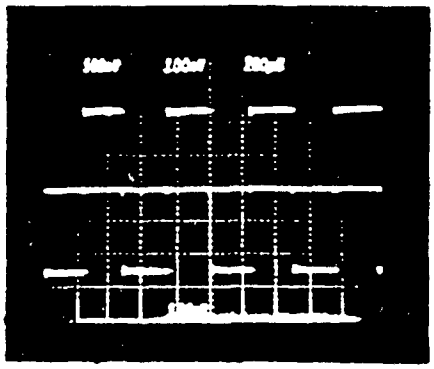
4.3.9 Conclusions

In this section a novel three-phase fed HFL converter with suppressed dc components has been proposed. This HFL converter draws high quality input current waveforms from the ac source. The synchronous rectifier fed HFL converter exhibits practically sinusoidal ac input current with suppressed dc link components. Moreover, the input filter ac capacitor and output filter inductor are eliminated thus decreasing further the size and the cost of the overall converter. Moreover since the proposed topology uses a front end reactor it exhibits improved reliability against short circuits. Finally, predicted features such as input/output waveforms and associated harmonic spectra have been verified experimentally on laboratory prototype unit.

(a)

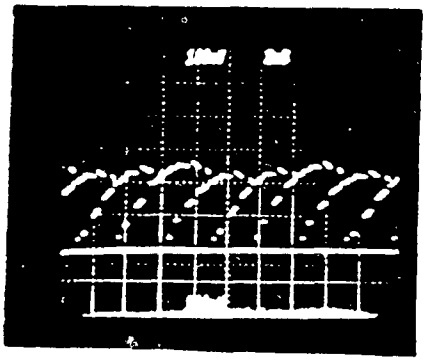


(b)



Amp.:(V_f) 100 Volts./Div.
Time:200 μs/Div.

(c)



Amp.:(I_o) 1 Amps./Div.
Time:2 msec./Div.

Fig. 4.14: Experimental waveforms of the proposed synchronous converter.
(a) Isolation transformer primary current (I_f) and its respective frequency spectrum.
(b) Isolation transformer primary voltage (V_p).
(c) Dc link current (I_o).

4.4 Three-Phase High Frequency Link Section

Sections 4.2 and 4.3 dealt with the analysis and design of single-phase high frequency links in SMR converters. This section concentrates on the analysis and design of three-phase high frequency links in SMR converters. The analysis and design of single-phase fed front-end passive and active filter topologies are presented in sections 2.3 and 3.2. These topologies maintain high quality input current waveform and high input power factor. Application of the front-end passive filter topology (Fig. 2.5) in three-phase HFL converters reduces the size of the converter considerably and the output voltage control is achieved by varying the duty cycle of the high frequency three-phase inverter switches under varying input voltage and load conditions. The analysis and design of the output voltage control method by varying the duty cycle of the three-phase inverter switches are discussed in detail in this section. However, the performance degradation of the three-phase inverter while varying the duty cycle of the inverter switches can be eliminated by replacing the front-end passive filter topology with active filter topology discussed in section 3.2.

The transistorized realization of the three-phase bridge inverter with its feedback diodes is shown in Fig. 4.3. The high frequency transformer turns ratio is assumed to be 1:1 to simplify the discussion. Moreover, in a three-phase inverter circuit each transistor (Fig. 4.3) has a maximum conduction period of 120°. The switching sequence for a three-phase inverter is as shown in Fig. 4.15. In this case the maximum duty cycle of any switch is $\approx$33.33-%, whereas in a single-phase full bridge converter the duty cycle limit would be 50-%. Evidently if the duty cycle is less than 16.66-%, only one switch will

turn on at a time and the output voltage from the converter will be zero. Thus, the required range in the duty cycle of any switch is from 16.66-% to 33.33-% in order to produce zero to rated output voltage. Consequently, in a three-phase bridge inverter (Fig. 4.3), inherent delays in switching actions (such as storage time in BJT's) do not pose conduction overlap problems under converter overload conditions (i.e. small values of duty cycle). As we have just seen, such delays can be as long as one-sixth of the entire time period. For inverter switches the worst operating condition is when the output voltage is controlled by varying the duty cycle of the inverter switches. Under this operating condition (i.e. maximum input dc voltage, V_L, and duty cycle less than 33.33-%) either one transistor switch and two diodes or two transistor switches will be conducting at any time.

When two transistor switches are conducting, one switch is from the Q_1, Q_3, and Q_5 group and the other is from the Q_4, Q_6, and Q_2 group. Consequently, two of the high frequency transformer primary terminals are connected to the dc supply terminals and the third terminal remains floating during any of the above six intervals. The potentials of the terminals connected to the dc source are well defined but the potential of the floating terminal at any instant will depend on the nature of the high frequency link parameters. Moreover, the commutation of the inverter transistor switches and diodes depends upon the equivalent line inductance present in the high frequency link.

4.4.1 Inverter Under Zero Line Inductance

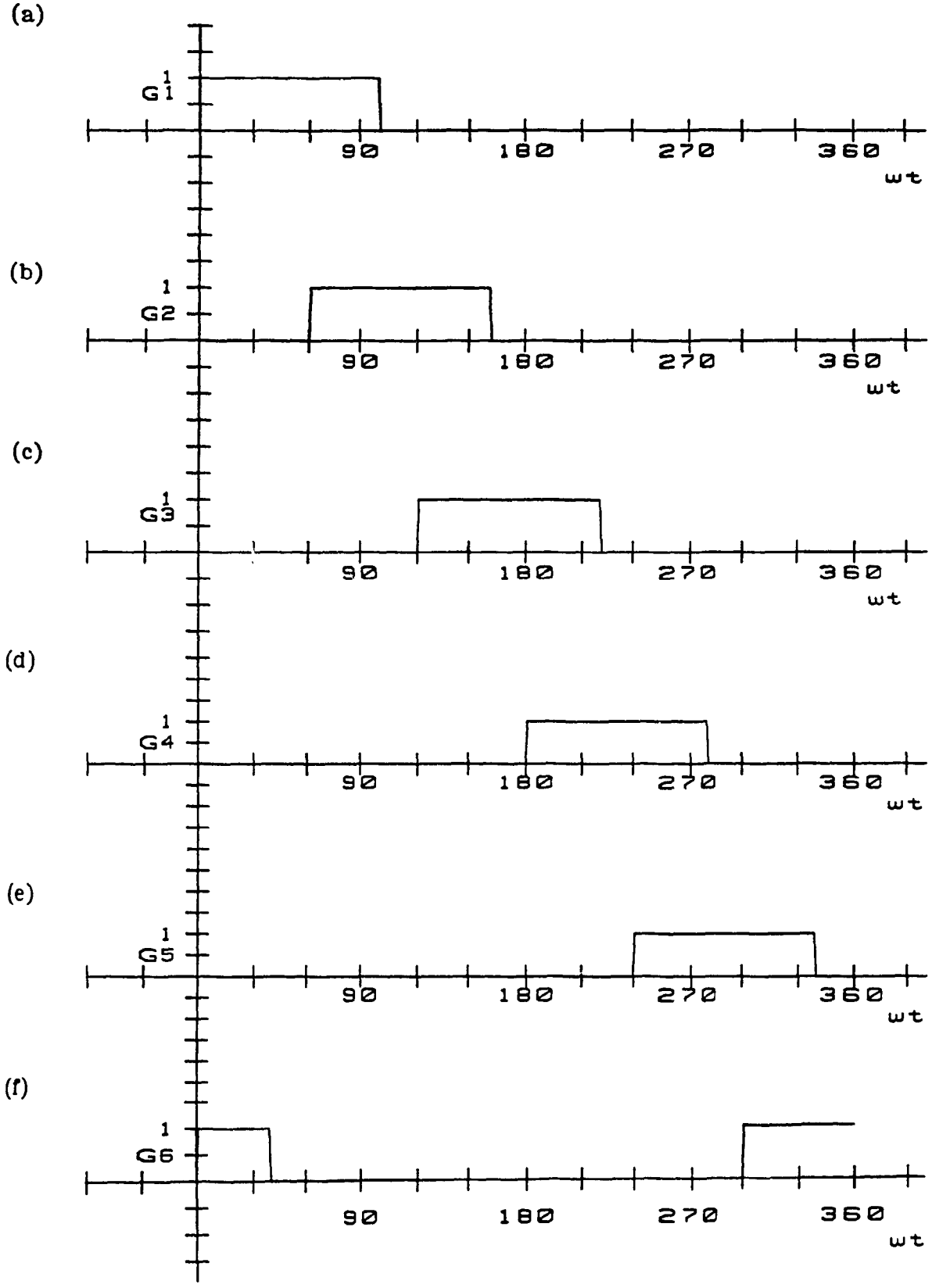
When the circuit is operating under ideal conditions, without a high fre-

quency transformer, the line inductance present in the high frequency link is zero. Gating signals are shown in Fig. 4.15 for a conduction period of 100^{o}. The inverter phase voltages are defined with respect to the fictitious neutral point 'o'. Considering the inverter circuit where Q_1 and Q_6 are conducting and the filter inductor current, I_s, (Fig. 4.3) is increasing in the inductor, L_s, at a rate determined by the difference between the input voltage, V_L, and the load voltage, V_s, as shown in Fig. 4.15(h). When Q_6 turns off, as determined by an appropriate control circuit, the current, I_{fa}, (Fig. 4.3) is forced to zero since the line inductance is zero as shown in Fig. 4.16(e). Under this condition, the current I_s which is maintained by inductor, L_s, attempts to circulate through all six rectifier diodes at a rate determined by load voltage V_s and L_s. During the next interval, Q_2 comes into conduction and the current I_s will attempt to transfer itself entirely to the Q_1 and Q_2 transistor switches. At the end of the Q_1 conduction period, Q_2 will be still conducting and the interval II conditions apply to transistor switch Q_2.

During the next interval, Q_3 comes into conduction and all of the current I_s will attempt to flow through the Q_3 and Q_2 transistor switches. Similar conditions will reappear for Q_1 - Q_6 transistor switches during the subsequent intervals. From the description presented above, the switching function $S_i(\omega t)$, of the inverter is derived and is shown in Fig. 4.16(d).

4.4.2 Inverter Under Small Line Inductance

In some applications, dc-dc converters require a means of providing isolation for safety and load matching. Under these conditions the equivalent transformer leakage inductances L_{fa}, L_{fb}, and L_{fc} (referred to the pri-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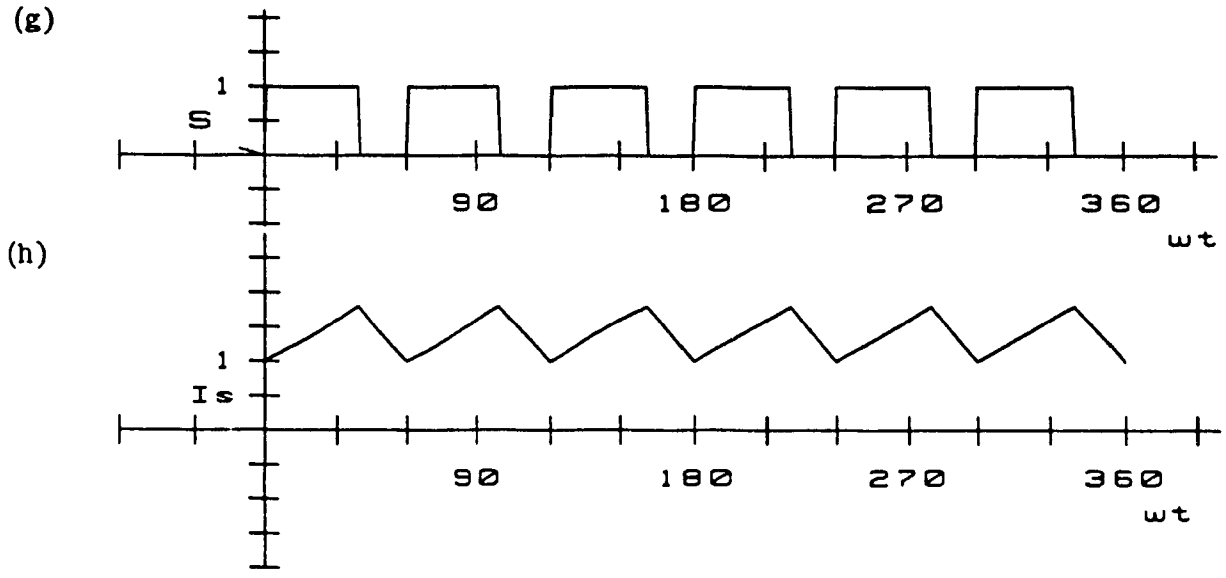
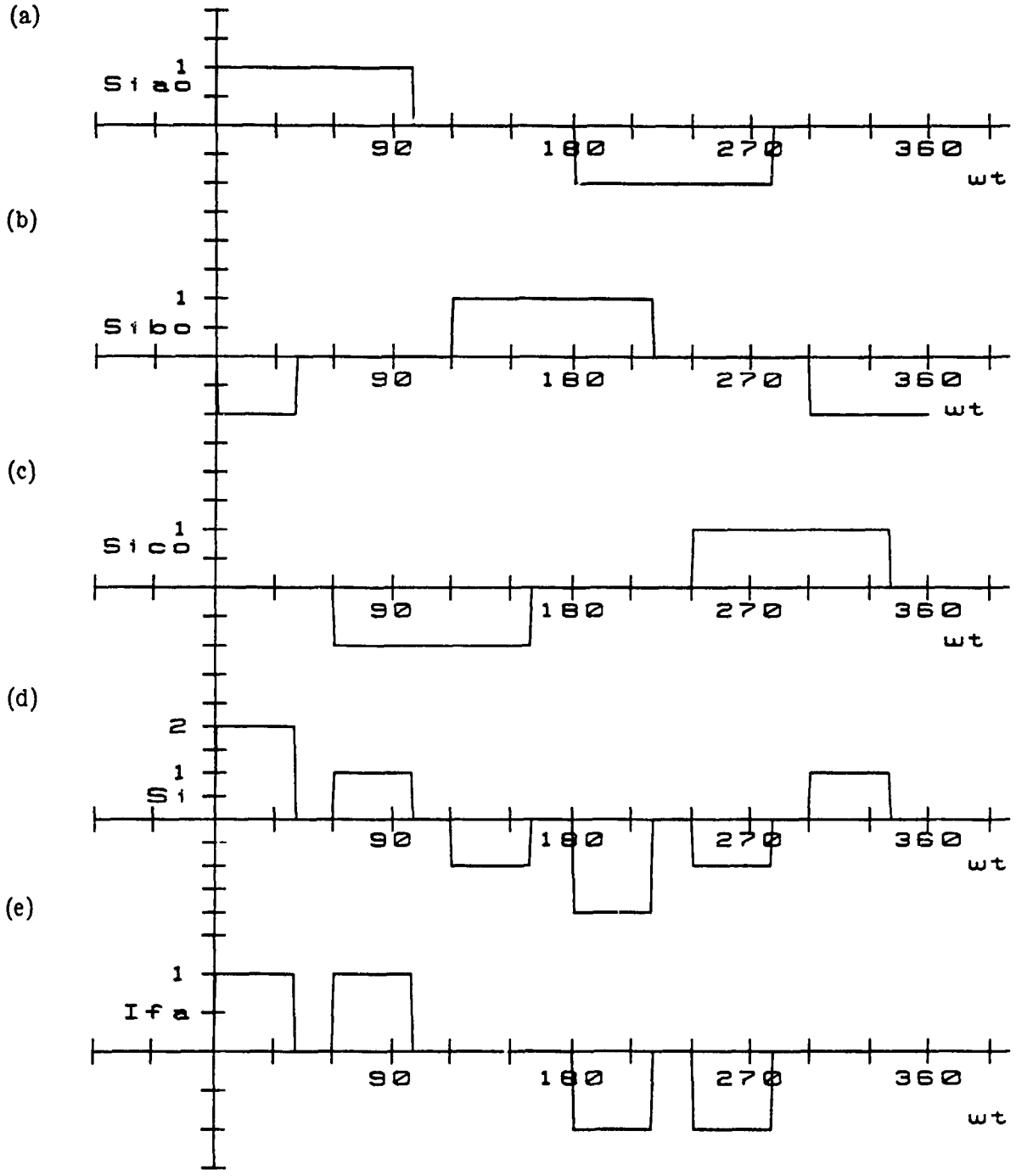


Fig. 4.15: Three-phase high frequency link SMR converter simulated waveforms.

(a)-(f) Three-phase inverter gating signals.

(g) Overall switching function, S (ωt).

(h) Current, I_s (ωt), through the output filter inductor.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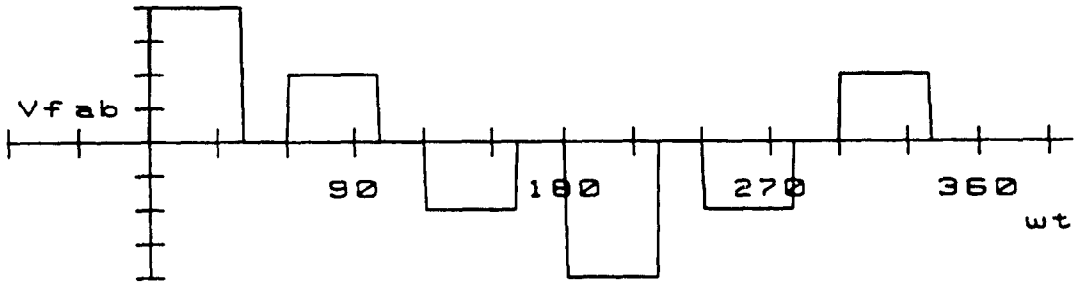


Fig. 4.16: Three-phase inverter and high frequency link simulated waveforms under zero line inductance

(a)-(d) Derivation of the three-phase inverter switching function, $S_1(\omega t)$ under zero line inductance.

(e) High frequency link line current, $I_{fa}(\omega t)$.

(f) High frequency link line to line voltage, $V_{fab}(\omega t)$.

mary) will always be present in the high frequency link phases A, B, and C respectively. Considering the inverter circuit where Q_1 and Q_6 are conducting and the current I_s is increasing in the inductor, L_s, at a rate determined by the difference between the input voltage, V_L, and the load voltage, V_s, is shown in Fig. 4.15(h). The equivalent transformer leakage inductances L_{fa}, L_{fb}, and L_{fc} are much smaller than L_s and have negligible effect on the current I_s. When Q_6 turns off, as determined by an appropriate control circuit, the current, I_{fa}, is forced to transfer to the Q_3 and Q_5 feed-back diodes (D_3 and D_5). The current I_{fa} is transiently maintained by L_{fa} and L_{fb} assuming that the transformer primary and secondary windings are star connected. Under this condition, the current I_s, maintained by inductor L_s, attempts to circulate through all six rectifier diodes. Opposing this I_s current transfer is the primary leakage inductances L_{fa}, and L_{fb} which attempts to maintain current I_{fa}. When all the rectifier diodes are conducting, the high frequency link has the equivalent circuit shown in Fig. 4.17. The voltage which tends to drive the current I_{fa} in L_{fa} to zero is given by $V_{ab} + V_{fe}$ and $V_{ac} + V_{fd}$. With all six rectifier diodes conducting, the voltages V_{fe} and V_{fd} are approximately zero. The voltage V_{ab} is the sum of Q_1's forward drop and Q_3's feed-back diode drop. Similarly the voltage V_{ac} is Q_1's forward drop and Q_5's feed-back diode drop. This voltage is estimated to be on the order of 3V. Thus very little voltage is available to cause the current I_{fa} in the leakage inductance to change. Under ideal conditions (neglecting the forward voltage drop) the current I_{fa} at the end of the turn-off of transistor switch Q_6 will be maintained constant by L_{fa}, L_{fb}, and L_{fc}, as shown in Fig. 4.18(e). During this interval Q_1 carries the load current, I_s, and the diodes D_3 and D_5 each carry half the load current. During the next interval

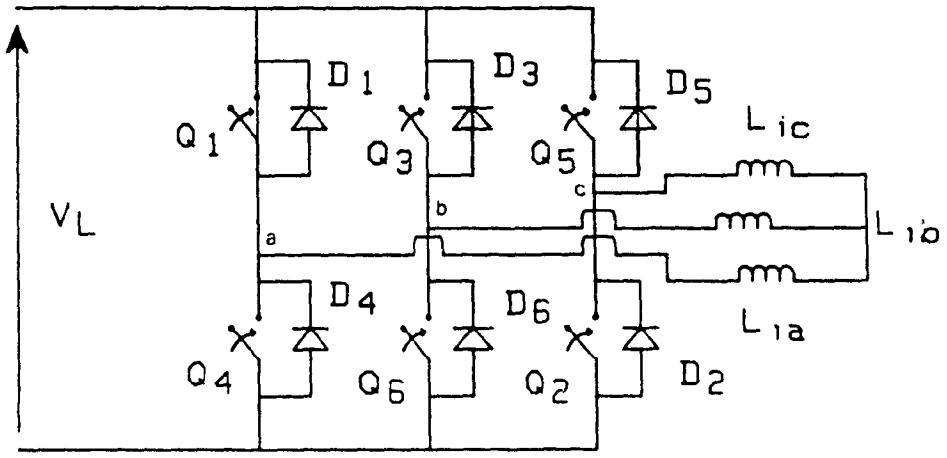


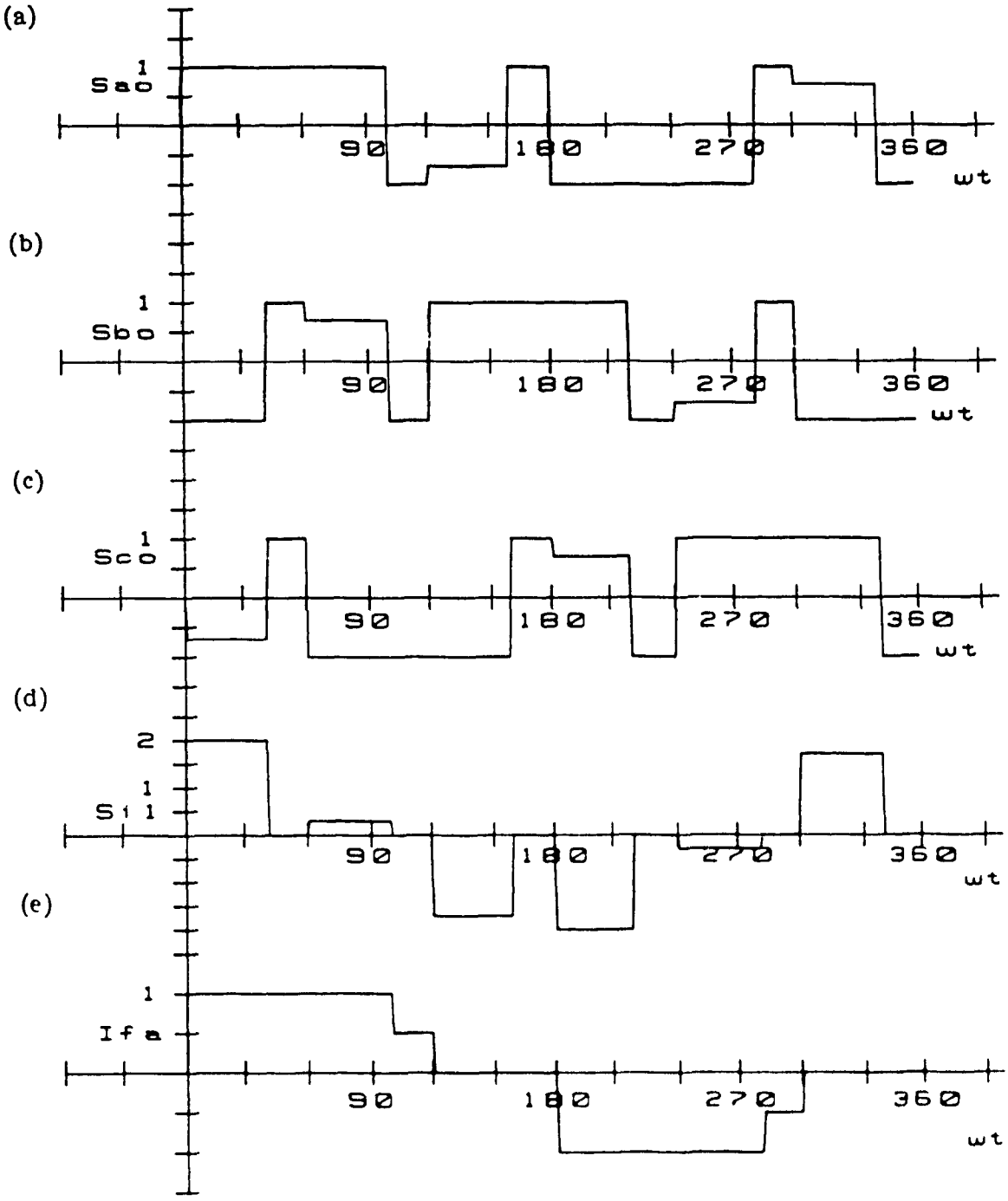
Fig. 4.17: Equivalent high frequency link circuit during free-wheeling period.

Q_2 comes into conduction and the current I_{fa} will attempt to transfer itself entirely to the Q_1 and Q_2 transistor switches. At the end of the Q_1 conduction period, Q_2 is still conducting and the interval II conditions apply to transistor switch Q_2. The current I_{fa} is forced to commutate the feed-back diode of Q_4 (D_4) because L_{fa} and the input dc voltage, V_L, will appear across the transistor switch, Q_1.

During the next interval, Q_3 comes into conduction and the current I_{fa} will attempt to transfer entirely to the Q_3 and Q_2 transistor switches. The current, I_{fa}, flowing through the inductor, L_{fa}, is suddenly interrupted by switching on the transistor, Q_3. At this instant the current, I_{fa}, is changing from its value to zero. Consequently the voltage ($V = L_{fa}\frac{dI_{fa}}{dt}$) at point 'a' depends upon the value of the high frequency link line inductance, L_{fa}, and current, I_s. During this interval (V) the voltage V_{ao} will be less than $\frac{-V_L}{2}$ depending upon the value of L_{fa}. Similar conditions will reappear for the transistor switches Q_1 - Q_6 during the subsequent intervals. From the above description, the switching function of the inverter $S_{i1}(\omega t)$ is derived and is shown in Fig. 4.18(d).

4.4.3 Inverter/Rectifier

In this section the proposed three-phase inverter is analyzed under steady state conditions. The derived expressions are subsequently used to obtain the information necessary for proper HFL section design. The converter is analyzed under the following assumptions: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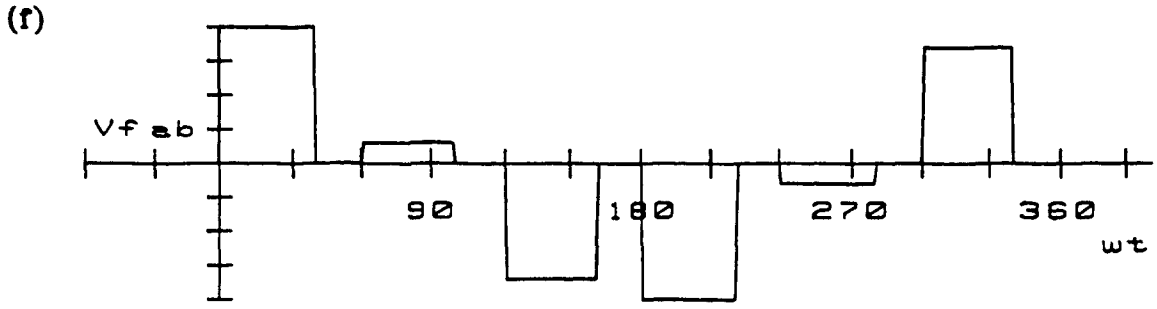


Fig. 4.18: Three-phase inverter and high frequency link simulated waveforms under small line inductance

(a)-(d) Derivation of the three-phase inverter switching function, $S_{i1}(\omega t)$, under small line inductance.

(e) High frequency link line current, $I_{fa}(\omega t)$.

(f) High frequency link line to line voltage, $V_{fab}(\omega t)$.

(i) all power switching devices are ideal and the forward drop and reverse leakage currents of the diodes are negligible;

(ii) the filter components are ideal;

(iii) the load voltage, V_s, is ripple free;

(iv) the inverter input dc voltage, V_L, is ripple free.

Moreover,

The inverter input dc voltage, $V_{L(min)} = 1.0$ pu

The rated output power = 1.0 pu

In order to derive the necessary expressions required for the converter input and output filter design the frequency spectra of the input and output quantities $I_{in}(\omega t)$ and $I_s(\omega t)$ must be known. These quantities can be easily obtained when the switching functions of the high frequency inverter and the high frequency rectifier stages are represented by an overall switching function $S(\omega t)$. The derivation of the overall switching function under maximum input dc voltage, $V_{L(max)}$, and rated load is shown in Fig. 4.15. At rated load, the dead time between the pulses of $S(\omega t)$ decreases as the inverter input voltage decreases. At minimum input dc voltage, $V_{L(min)}$ the overall switching function becomes constant (1.0).

Although the overall switching function shown in Fig. 4.15 helps to visualize how the converter operates, it is also necessary to express the converter operation in mathematical form in order to be able to obtain the required frequency spectra of the converter input and output currents, $I_{in}(\omega t)$ and $I_s(\omega t)$. Such a mathematical form can be obtained by deriving the Fourier series expansion which is given by

$$S(\omega t) = A_o + \sum_{n=0\,12}^{\infty} A_n \sin(n\,\omega t) \qquad (4.43)$$

where,

A_n is the amplitude of the n^{th} harmonic component of $S(\omega t)$.

ω is the inverter operating frequency taken as 1.0 pu

The converter output voltage before the filter shown in Fig. 4.19(a) is given by

$$V_o(\omega t) = V_L S(\omega t) \tag{4.44}$$

From the above discussion and Fig. 4.15 it is evident that the duty cycle variation of the inverter switch for output voltage control results in complementary switch antiparallel diode conduction before turning-on the inverter switch. Therefore charging and discharging of snubber capacitors through the respective transistor switch can seriously degrade the performance of the inverter. Hence the three-phase inverter has to be operated at its fixed duty cycle ($\approx$ 33.33-percent) and the output voltage is controlled by the front-end rectifier system. Furthermore, the value of the inverter input voltage (V_L) depends upon the front-end rectifier system. The component ratings of the three-phase topologies are discussed in the next section.

4.4.4 Output Filter

In Fig. 4.3 the high frequency three-phase inverter operates at slightly less than 33.33-percent duty cycle. The front-end rectifier controls the output voltage under varying input voltage and load conditions. Therefore the output filter is designed assuming a 31.33-percent duty cycle for inverter switches and the respective voltage waveform at the input of the output filter is shown in Fig. 4.19(a). Also, the equivalent circuit for the output filter design is shown in Fig. 4.19(b). Moreover, Fig. 4.19(c) shows the theoretical waveform

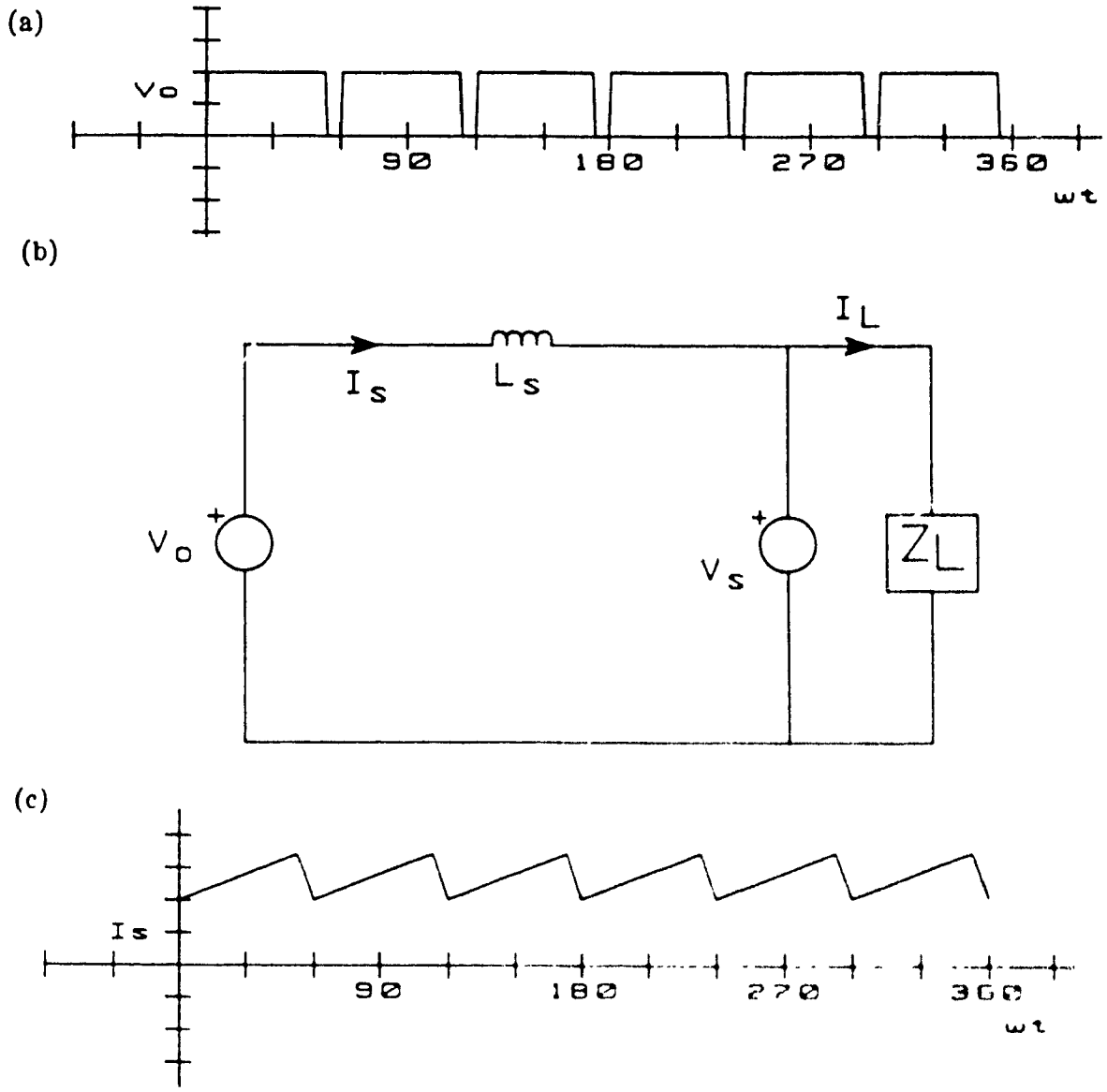


Fig. 4.19: Simulated waveforms and equivalent circuit for the output filter design.

(a) Output voltage before filter, $V_o(\omega t)$.

(b) Equivalent circuit for the output filter design.

(c) Converter output filter inductor current (I_s)

of the filter inductor current I_s. From Fig. 4.19(b) it follows that the value of the average peak-to-peak ripple current is given by

$$\overline{\Delta I_s} = \frac{V_L - V_s}{L_s} t_{on}$$
$$= \frac{1.0 - 0.94}{L_s} t_{on} \qquad (4.45)$$

where,

- t_{on} is the output voltage, V_o, pulse width $= \frac{0.94}{6} T_s$;
- T_s is the operating time period of the inverter taken as 1.0 pu

Substituting the above in Eqn. (4.45) yields

$$\overline{\Delta I_s} = \frac{0.06}{L_s} \frac{0.94}{6} T_s$$
$$= \frac{0.0094 T_s}{L_s}$$

or

$$L_s = \frac{0.0094 T_s}{\overline{\Delta I_s}} \qquad (4.46)$$

Further assuming that $\overline{\Delta I_s}$ = 10-percent peak to peak current ripple, the dominant harmonic ripple component at six times the inverter operating frequency becomes

$$I_{s,6} = 0.1414 \ \ pu \qquad (4.47)$$

Assuming the ripple voltage across the filter capacitor $C_s \leq$ 0.1-percent, then the value of the filter capacitor is given by

$$C_s = \frac{0.1414 * 100}{\sqrt{2} * 6 * 0.1 * 1.0} = 16.66 \ \ pu \qquad (4.48)$$

It is noted that the L_s and C_s values found in Eqns. (4.46) and (4.48) are smaller than the respective values found in section 4.2.2 for the single-phase HFL converter.

4.4.5 Inverter Input Filter

When the current ripple I_s is neglected the input dc current, I_{in}, (Fig. 4.20(a)) is given by

$$I_{in}(\omega t) = S(\omega t) I_s(\omega t) \tag{4.49}$$

Therefore, by neglecting the output filter inductor current ripple, the Fourier analysis of the dominant harmonic component of the input dc current (six times the inverter operating frequency) value is given by (Eqn. (4.43))

$$I_{in\,6} = 0.1193 \quad pu \tag{4.50}$$

From the above equation it is clearly evident that the three-phase inverter input current dominant ripple frequency is three times the dominant ripple frequency of the single-phase inverter input current (see Eqn. 4.10). In Fig. 4.3 considering the inverter input current (I_{in}) the equivalent circuit for the dc filter design is shown in Fig. 4.20(b). In Fig. 4.20(b) the dominant frequency component of I_o is 120 Hz and the dominant frequency of I_{in} is six times the inverter operating frequency. Therefore, the amplitude the 120 Hz voltage harmonic component across the filter capacitor is given by

$$V_{L\,2} = \frac{I_{c\,2}}{2\omega C_o} \tag{4.51}$$

and the amplitude of the 120 kHz voltage harmonic component (assuming 20 kHz inverter operating frequency) across the filter capacitor is

$$V_{L\,6in} = \frac{I_{in\,6}}{6 * 333.33\omega C_o} \tag{4.52}$$

From Eqns. (4.51) and (4.520) the rms ripple voltage across the dc filter capacitor becomes

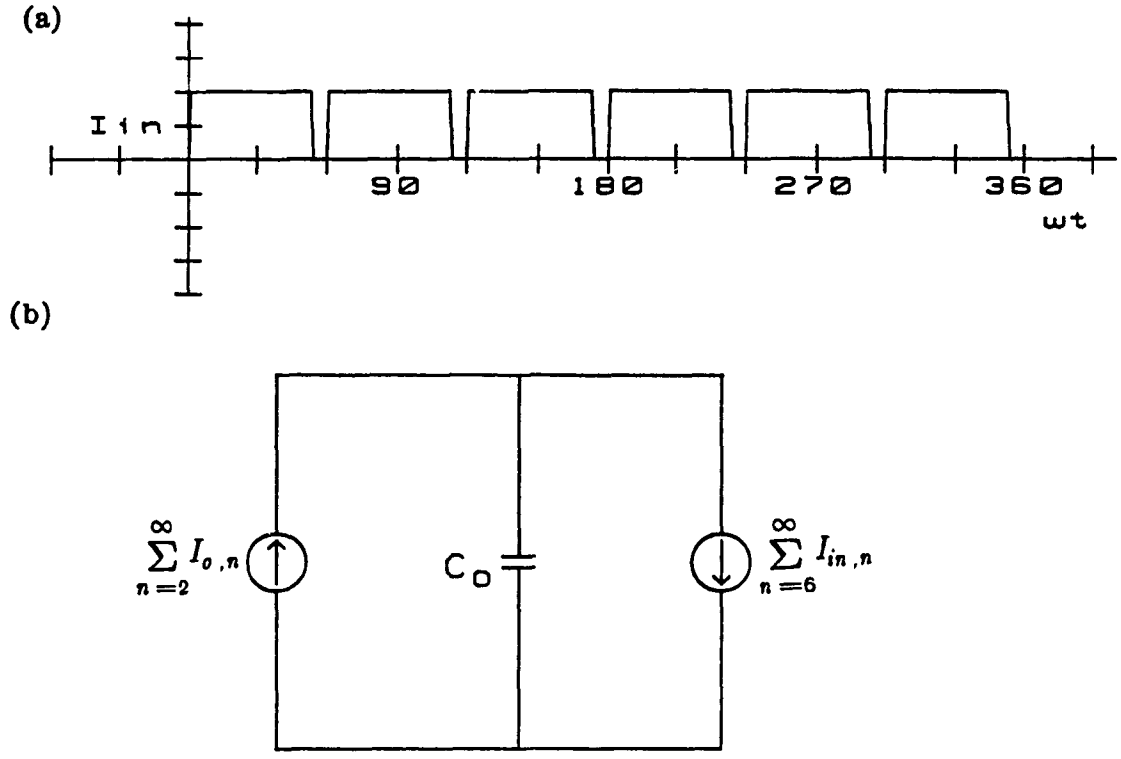


Fig. 4.20: Three-phase inverter input current, $I_{in}(\omega t)$ and the equivalent circuit for dc link filter design (Fig. 4.3).

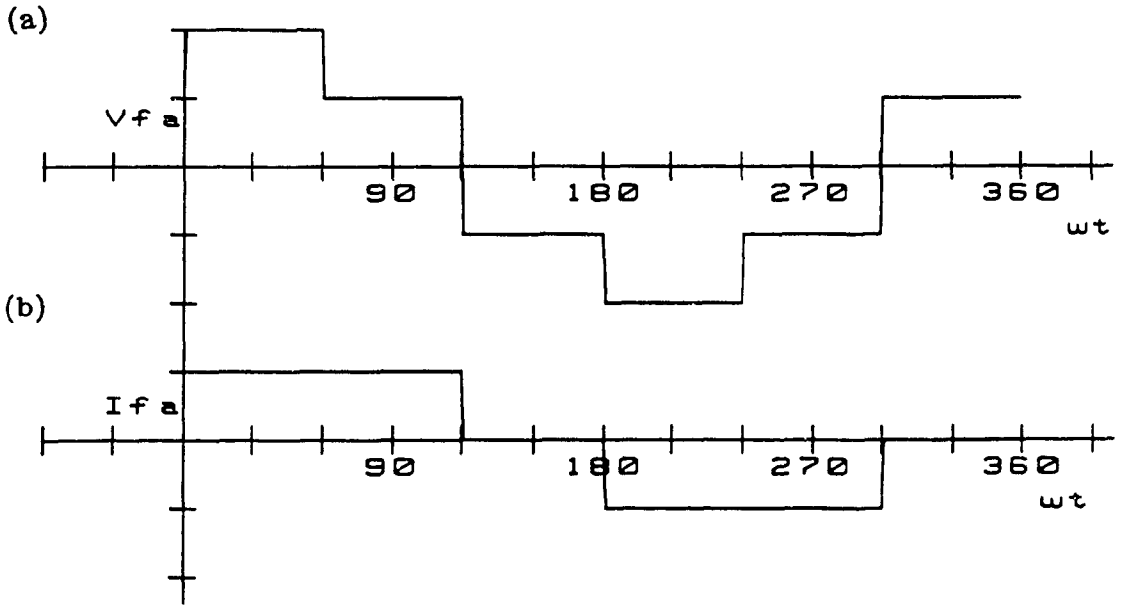


Fig. 4.21: Three-phase SMR converter high frequency link voltage (V_{fat}) and current (I_{fa}) (Fig. 4.3).

$$V_{L,ripple} = \frac{1}{\sqrt{2}}\sqrt{V^2_{L,2} + V^2_{L,6in}} \tag{4.53}$$

Moreover, the allowable inverter input voltage ripple can be defined by

$$Ripple\ \% = \frac{100 * V_{L,ripple}}{V_{L,o}} \tag{4.54}$$

Using Eqns. (4.51)-(4.54) the value of the filter capacitor is given by

$$C_o = \frac{100 * \sqrt{I^2_{o,2} + (\frac{I_{in,6}}{3 * 333.33})^2}}{\sqrt{2} V_{L,o} * 2 * \omega(ripple\ \%)} \tag{4.55}$$

At 1.0 pu dc bus voltage the value of 120 Hz ripple component ($I_{o,2}$) for the proposed passive filter topology becomes

$$I_{o,2} = \frac{0.736}{1.12} = 0.657\ \ pu \tag{4.56}$$

Using Eqns. (4.50), (4.55) and (4.56) the value of the capacitor (C_o) for 5% ripple voltage (V_L) becomes

$$C_o = \frac{100 * \sqrt{(0.657)^2 + (\frac{0.1193}{3 * 333.33})^2}}{\sqrt{2} * 2 * 5} = 4.645\ \ pu \tag{4.57}$$

It is noted that the C_o value found in Eqn. (4.57) is same as the respective C_o value found in Table 2.1 for proposed passive filter topology. Therefore the influence of the high frequency inverter on the value of C_o is negligible.

4.4.6 High Frequency Transformer

Under ideal conditions the high frequency link line to line voltage shown in Fig. 4.21(a) is given by

$$V_{fab}(\omega t) = V_L(\omega t) S_i(\omega t) \tag{4.58}$$

where $S_i(\omega t)$ is the inverter switching function.

The simulated high frequency link line current, I_{fa}, is shown in Fig. 4.21(b).

The high frequency transformer primary line to line voltage, V_{fab}, and current I_{fa}, are shown in Fig. 4.21. The rms values of voltage and current are given by

$$V_{fab(rms)} = 0.7051 \quad pu$$
$$I_{fa(rms)} = \frac{\sqrt{2}}{\sqrt{3}} = 0.8158$$

and the total VA of the transformer is $\sqrt{3} * 0.705 * 0.8158 = 1.0$ pu

For transformation of three-phase power either a bank of three identical single-phase transformers each rated at one-third of the single-phase transformer suitably connected or one three-phase transformer may be employed. Using a single three-phase transformer is obviously the best choice since it requires a smaller core and it is less expensive. This advantage is also true when the 1 pu VA three-phase transformer required here is compared to the 1 pu VA single-phase transformer required by the single-phase HFL converter (Fig. 4.1).

4.4.7 Inverter/Rectifier Component Ratings

Transistor ratings will be selected such that the rms current flowing through the transistor will be equal to the transistor rms current rating, I_{rms}. During a cycle, the high frequency link line current is shared between two transistors. For example, transistor Q_1 (phase A) carries the load current during the positive half cycle and transistor Q_4 during the negative half cycle. Therefore the rms value of the high frequency link line current, $I_{fa(rms)}$,

under rated load conditions is given by

$$I_{fa(rms)} = \sqrt{2} I_{rms} \tag{4.59}$$

where I_{rms} is the rms current through the inverter transistor switch.

The rms current through the transistor is given by

$$I_{rms} = \left[\frac{1}{2\pi} \int_0^{\frac{2\pi}{3}} I_a^2 dt \right]^{1/2}$$

$$= \frac{1}{\sqrt{3}} \ pu = 0.577 \ pu \tag{4.60}$$

The peak current through the inverter switch is 1.05 pu and the average current through the inverter switch is 0.33 pu. Also, the peak forward voltage (V_{sw}) = 1.0 pu

$$\textit{Total converter switch VA} = \sum_{k=1}^{6} I_{rms\ k} * V_{sw\ k}$$

$$= 6 * 0.577 * 1.0$$

$$= 3.462 \ pu$$

For 1:1 high frequency transformer turns ratio the currents through the high frequency output rectifier diode are same as the inverter switch current ratings found above. The currents through the three phase inverter switches are smaller than the respective currents through the single-phase inverter switch found in Section 4.2.5. However the three phase HFL converter also has the disadvantage of requiring higher total inverter switch VA as compared to the single-phase HFL converter

4.4.8 Design Example

In order to illustrate the significance and facilitate the understanding of the results predicted in the previous sections, the following design example is presented.

The dc-to-dc HFL converter has the following specifications:

Inverter operating frequency = 20 kHz

Minimum input dc voltage, V_L = 185.5 Volts

Output power = 2 kVA

From these values

$$1 \text{ pu current} = \frac{2000}{185.5} = 10.781 \text{ Amps}$$

$$1 \text{ pu impedance } \frac{185.5}{10.781} = 17.21\ \Omega$$

$$1 \text{ pu inductance} = \frac{17.21}{2\pi * 20 * 10^3} = 136.98\ \mu\text{H}$$

$$1 \text{ pu capacitance} = \frac{1}{17.21 * 2\pi * 20 * 10^3} = 0.46\ \mu\text{F}$$

Using Eqns. (4.46), (4.48), and (4.60) the following converter component values are computed. The output filter inductor, (L_s) is given by

$$L_s = \frac{0.0094}{1.0781}(50)10^{-6} = 0.4359\ \ \mu H \tag{4.61}$$

The output filter capacitor (C_s) is given by

$$C_s = 16.66 * 0.46 = 7.666\ \ \mu F \tag{4.62}$$

The inverter switch rms current is given by

$$I_{rms} = 0.577 * 10.781 = 6.22 Amps. \tag{4.63(a)}$$

The peak current through the inverter switch is given by

$$I_{peak} = 1.05 * 10.781 = 11.32 Amps \tag{4.63(b)}$$

The average inverter switch current is given by

$$I_{ave} = 0.33 * 10.781 = 3.558 Amps \qquad (4.63(c))$$

and

$$\textit{Total converter switch VA} = 3.462 * 185.5 * 10.7816 = 6923.95 \qquad (4.63(d))$$

Using the equations derived in sections 4.2.2 and 4.2.5 the following converter component values are computed. The output filter inductor (L_s) is given by

$$L_s = \frac{0.0283}{1.0781}(50)10^{-6} = 1.31 \ \mu H \qquad (4.64)$$

The output filter capacitor(C_s) is given by

$$C_s = 50 * 0.46 = 23.14 \ \mu F \qquad (4.65)$$

The inverter switch rms current is given by

$$I_{rms} = 0.707 * 10.781 = 7.62 Amps \qquad (4.66(a))$$

The peak current through the inverter switch is given by

$$I_{peak} = 1.05 * 10.781 = 11.325 \qquad (4.66(b))$$

The average current through the inverter switch is given by

$$I_{avr} = 0.5 * 10.781 = 5.391 Amps \qquad (4.66(c))$$

and

$$\textit{The total converter switch VA} = 2.828 * 185.5 * 10.7816 = 5655.12 \qquad (4.66(d))$$

Evaluation of Eqns. (4.61)-(4.66) shows that as predicted, the three phase HFL converter has the advantages of (I) lower output filter inductor (L_s) and (II) lower output filter capacitor (C_s) values while, increasing the inverter input current (I_{in}) dominant harmonic frequency value from 40 kHz to 120 kHz.

4.4.9 Experimental Results

In order to verify the selected predicted results a 2 kVA prototype experimental converter was implemented using power MOSFET transistors with the following circuit parameters:

Operating frequency of the inverter (f_o) = 20 kHz

Maximum input dc bus voltage ($V_{L(max)}$) = 260 Volts

External high frequency link line inductance (L) = zero

Experimental waveforms obtained with this prototype at maximum input dc voltage are shown in Fig. 4.22. In particular, Fig. 4.22(d) shows that, during the interval II the high frequency link line current at rated load differs slightly from the predicted results shown in Fig. 4.16(e). This is mainly due to the parasitic inductance of the converter leads a phenomenon which cannot be completely eliminated. Further, Figs. 4.22(e) and 4.22(c) show that the output voltage before the filter (V_o) and the high frequency link line voltage (V_{fab}) are in close agreement with the predicted results shown in Figs. 4.19(a) and 4.18(f). The efficiency of the converter at maximum and minimum input dc voltage are as follows:

(a) Maximum input dc voltage = 260 Volts

Input power = 2184 VA

Output power = 2100 VA

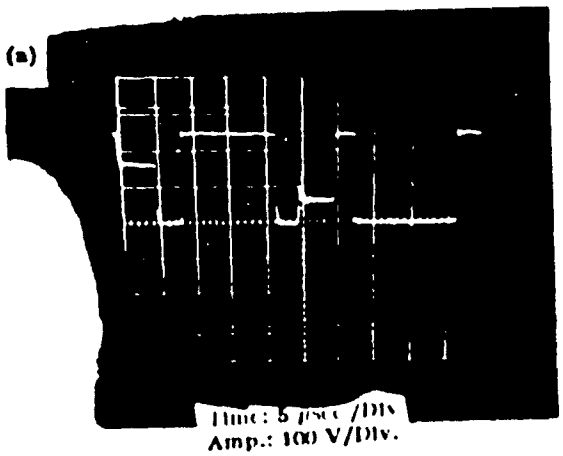
High frequency converter efficiency, η = 96.15%

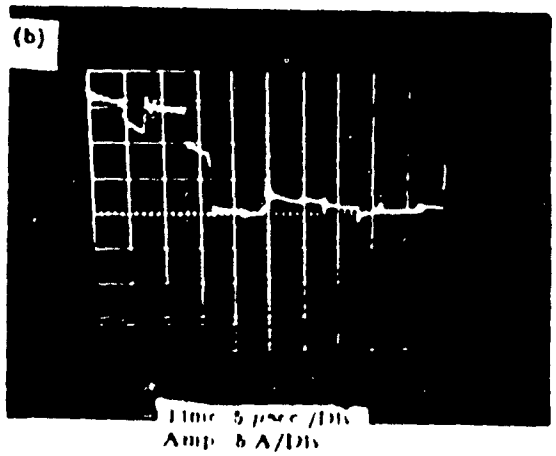
(b) Minimum input dc voltage = 185.5 Volts

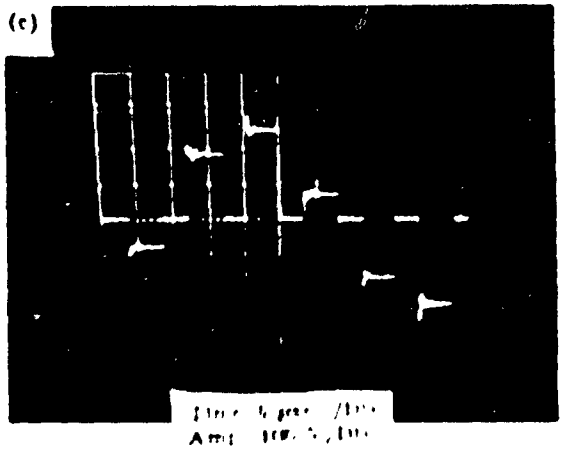
Input power = 2188.9 VA

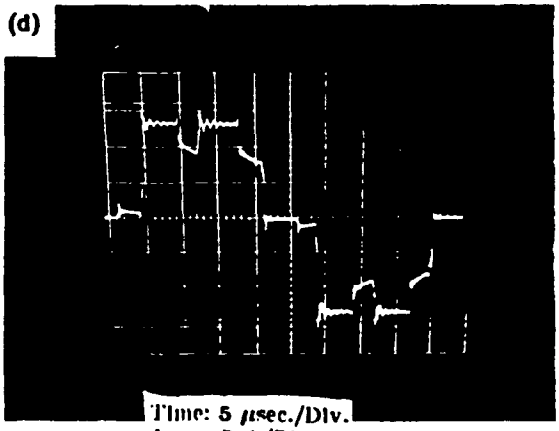
Output power = 2100 VA

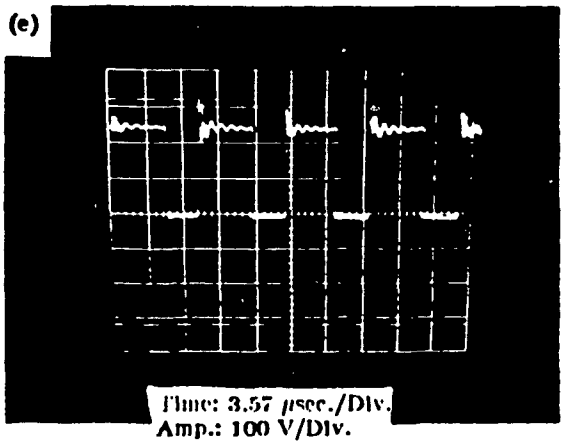
High frequency converter efficiency, η = 96%


(a)
Time: 5 μsec /Div
Amp.: 100 V/Div.


(b)
Time: 5 μsec /Div
Amp: 5 A/Div


(c)





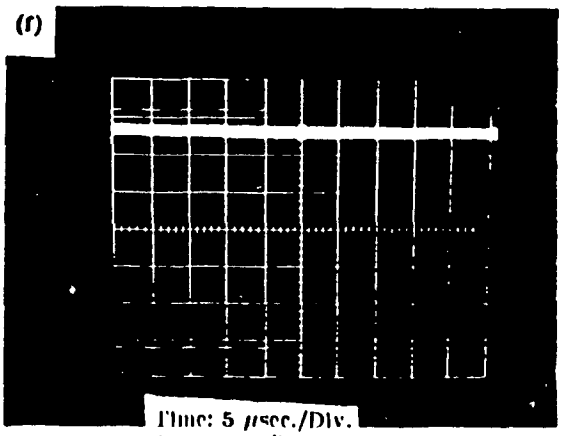


Fig. 4.22: Three-phase SMR converter experimental waveforms.
(a) Voltage across the inverter switch.
(b) Current through the inverter switch.
(c) High frequency link line-line voltage, V_{ab}.
(d) High frequency link line current, I_{fa}.
(e) Output voltage before filter, V_o.
(f) Current through the output filter inductor, I_s.

4.4.10 Conclusions

In this section an analysis and design approach for three-phase high frequency link converters under large input voltage and load variations has been presented. The different modes of operation for the inverter, the commutation process of the inverter switches, and the output voltage control methods are discussed in detail. Theoretical and experimental results have shown that the three-phase HFL converters, as compared to the single-phase equivalent converter, exhibit the following advantages:

(i) lower output filter inductor (L_o) value;

(ii) lower output filter capacitor (C_o) value;

(iii) input dc current dominant harmonic frequency is six times the inverter operating frequency;

(iv) three-phase transformer requires less magnetic core material, weighs less, and occupies less space.

The three-phase HFL converter also has the disadvantage of requiring higher total switch VA as compared to the single-phase HFL converter. Finally, key predicted results have been verified experimentally on a 2 kVA prototype converter.

4.5 Conclusions

This chapter has been presented the single-phase HFL converter power topologies in which the PWM constant frequency inverter section is always operating in the current lagging mode. These topologies allow the safe use of

a lossless single-capacitor snubber from zero to rated load power conditions. In these configurations the high frequency inverter operates with lossless snubbers. To ensure the safe and lossless operation of the high frequency stage under all operating conditions, the inverter stage has been analyzed in detail and relevant expressions are derived. Finally, the theoretical results have been verified experimentally.

Moreover, in this chapter a novel three-phase fed HFL converter with suppressed dc components has been proposed. This HFL converter draws high quality input current waveforms from the ac source. The synchronous rectifier fed HFL converter exhibits practically sinusoidal ac input current with suppressed dc link components. Moreover, the input filter ac capacitor and output filter inductor are eliminated thus decreasing further the size and the cost of the overall converter. Moreover since the proposed topology uses a front end reactor it exhibits improved reliability against short circuits. Finally, predicted features such as input/output waveforms and associated harmonic spectra have been verified experimentally on laboratory prototype unit.

Finally, in this chapter an analysis and design approach for three-phase high frequency link converters under large input voltage and load variations has been presented. The different modes of operation for the inverter, the commutation process of the inverter switches, and the output voltage control methods are discussed in detail. Theoretical and experimental results have shown that the three-phase HFL converters, as compared to the single-phase equivalent converter, exhibit the following advantages:

(1) lower output filter inductor (L_s) value;

(ii) lower output filter capacitor (C_o) value;

(iii) input dc current dominant harmonic frequency is six times the inverter operating frequency;

(iv) three-phase transformer requires less magnetic core material, weighs less, and occupies less space.

The three-phase HFL converter also has the disadvantage of requiring higher total switch VA as compared to the single-phase HFL converter. Finally, key predicted results have been verified experimentally on a 2 kVA prototype HFL converter.

CHAPTER 5

Summary and Conclusions

5.1 Conclusions

Single-phase and three-phase fed ac-to-dc SMR converters proposed in this thesis maintain high quality input ac current and output dc voltage waveforms while providing the necessary ohmic isolation. Different modes of operation of single-phase and three-phase high frequency link converters have been studied. The associated output voltage control methods which compensate for input voltage and load variations have been discussed. Analysis of the respective converters have shown that depending on the particular output power level and specifications, the best combination of front-end ac-to-dc converter topology, inverter topology, and control strategies can be identified. Finally, this thesis has also presented the advantages of introducing three-phase inverters and three-phase transformers in HFL converters so as to achieve light weight, and compact power supplies. In particular, the contributions of this thesis can be stated by chapter as follows.

In Chapter 2 it has been shown that the proposed front-end single-phase passive filter topology (Fig. 2.5) yields a high input power factor and requires lower total VA rating than the conventional passive filters for diode rectifiers. Performance evaluation and related design data have been provided for the implementation of the front-end diode rectifier. Finally, selected key results have been verified experimentally.

In Chapter 3 it has been shown that the proposed front-end active filter

topology (Fig. 3.4) exhibits a low ripple sinusoidal ac input current and improves the input power factor, as compared to the passive filter topology discussed in chapter 2 (Fig. 2.5). Moreover the main advantage of the active method over the passive method is that the inductor size can be controlled by changing the input ripple current or by increasing the switching frequency. Furthermore, the proposed design allows the boost converter to operate at constant switching frequency. Finally, predicted results such as input/output current and voltage waveforms have been verified experimentally on a laboratory prototype unit. Furthermore, in Chapter 3 a novel three-phase fed boost active filter topology has been proposed. Detailed input and output current analysis have shown that the subject current waveshaping method yields near unity input power factor, eliminates the synchronization logic, and reduces the component count considerably when compared to the conventional converter. However, the proposed waveshaping method increases the current and voltage stresses of the semiconductor components. Finally, predicted features such as the input and output current waveforms and associated harmonic spectra are verified experimentally on a laboratory unit. Also in Chapter 3 a novel three-phase fed synchronous active filter topology has been discussed. This topology draws high quality input current waveforms from the ac source and reduces the switching stresses of the switching devices. Performance evaluation and relevant design data have been provided for the implementation of the front-end bridge rectifier. Detailed input and output current analysis has shown that the proposed switch-rectifier exhibits practically sinusoidal ac input current with reduced dc harmonic content. Moreover the input filter requirements are significantly reduced thereby decreasing further the size and the cost of the switch-rectifier unit. Finally, predicted features such as input/output waveforms and associated

harmonic spectra have been verified experimentally on laboratory prototype units.

Chapter 4 presents the single-phase high frequency link converter topologies in which the PWM constant frequency inverter section is always operating in the current lagging mode. These topologies allow the safe use of a lossless single-capacitor snubber from zero to rated load power conditions. In these configurations the high frequency inverter operates with lossless snubbers. To ensure the safe and lossless operation of the high frequency stage under all operating conditions, the inverter stage is analyzed in detail and relevant expressions are derived. Finally, the theoretical results have been verified experimentally. Moreover, in Chapter 4 a novel three-phase fed HFL converter with suppressed dc components has been presented. This synchronous rectifier fed HFL converter exhibits practically sinusoidal ac input current with suppressed dc link components. Furthermore, the input filter ac capacitor and output filter inductor are eliminated thus decreasing the size and the cost of the overall converter. Moreover since the proposed topology uses a front end reactor it exhibits improved reliability against short circuits. Finally, predicted features such as input/output current waveforms and associated harmonic spectra have been verified experimentally on laboratory prototype unit. Also in chapter 4 an analysis and design approach for three-phase high frequency link converters under large input voltage and load variations has been presented. The different modes of operation for the inverter, the commutation process of the inverter switches, and the output voltage control methods have been discussed in detail. Theoretical and experimental results have shown that the three-phase HFL converters, as compared to the single-phase equivalent converter, exhibit the following advantages: (1) the input and output current ripple frequency is six times the inverter operating

frequency, (ii) the associated filter component size is reduced, and (iii) the three-phase transformer requires less magnetic core material, weighs less and occupies less space. However, the three-phase high frequency link inverter also has the disadvantage of requiring higher total switch VA than the single-phase high frequency link inverter. The key predicted results have been verified experimentally on a prototype HFL converter.

In summary, single-phase and three-phase high frequency link converters proposed and analyzed in this thesis maintain high quality input ac current and output dc voltage waveforms while providing the necessary ohmic isolation. Furthermore, the associated output voltage control methods can improve the high frequency inverter performance and the efficiency of the HFL converter considerably than the conventional HFL converters. These HFL converters have been shown to be light weight, compact, rugged, reliable, and exhibit non-interference with other loads. Moreover, key theoretically predicted results have been verified experimentally as a means of establishing the effectiveness of the proposed methods.

5.2 Suggestions for Future Work

The HFL converter topologies discussed in this thesis use the intermediate dc link for converting the 60 Hz input voltage into high frequency ac voltage. Further investigation is therefore required in the area of converting 60 Hz voltage into high frequency ac voltage without an intermediate dc link. Consequently, the converter size can be reduced even further. In Chapter 3 the front-end PWM rectifier uses only a single [illegible] input filter, which is more [illegible]

bilities. Hence further investigation is needed to determine the stability limits of the system. Finally, in Chapter 2 the steady state solution of the passive diode rectifier is obtained by an iteration procedure. Further work can be done to include the analysis of the ac-to-dc rectifiers in discontinuous current mode using power conversion transfer functions.

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