SOME DESIGN AND ANALYSIS TECHNIQUES FOR PRACTICAL SC SAMPLED DATA FILTERS USING UNITY GAIN AMPLIFIERS

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सद्विद्या यदि का चिन्ता वराकोदर पूरणे ।
शुको ऽप्यशनमाप्नोति राम रामेति च ब्रुवण् ॥
जातिभिर्वण्ड्यते नैव चौरेणापि न नीयते ।
दानेन न क्षयं याति विद्यारत्नं महाधनम् ॥
विद्वत्त्वं च नृपत्वं च नैव तुल्यं कदाचन ।
स्वदेशे पूज्यते राजा विद्वान सर्वत्र पूज्यते ॥

- Chanakyya Shlokam

When you possess genuine knowledge, why worry about going hungry? Even Shuka (a small bird) gets fed simply by chanting Rama and Rama (the devine name). Genuine knowledge is the greatest of all wealths. The relatives cannot take it away, thieves cannot steal it, neither does it diminish by dissemination. There never is a comparison between a scholar and a king. A king is respected only in his home country. A scholar is respected everywhere.

ABSTRACT

SOME DESIGN AND ANALYSIS TECHNIQUES FOR PRACTICAL SC SAMPLED DATA FILTERS USING UNITY GAIN AMPLIFIERS

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Concordia University, 1984

This thesis examines, in the context of the present day MOS IC technology, the possibility of designing sampled data filter networks using unity gain amplifiers (UGAs) and switched capacitors (SCs).

Towards this end, it is first shown that by using few basic building blocks, sampled data transfer functions (SDTFs), of any order and of either type (viz., recursive or non recursive) can be realized. The class of linear phase filters is considered in some detail. The work is then concentrated on the realization of biquadratic SDTFs that are related to their popular analog counterparts through the well-known bilinear $s \leftrightarrow z$ transformation. Analyses for designs that use minimum total capacitance and have low sensitivity to capacitance, ratio errors are provided. The challenging problem of UGA based designs, viz., that of parasitic capacitances, is solved by proposing an algorithm for a parasitic tolerant design.

The proposed designs are further improved to the extent where

the component count in them becomes comparable to that in OA based designs. The effect of non zero offset voltages in UGAs, on the improved designs, is also analyzed. An algorithm that yields a parasitic tolerant design and uses minimum total capacitance is suggested. The algorithm can be used to reduce the effect of the non zero offset voltages.

Finally, the bandwidth capability of the proposed designs is analyzed by developing a new method to account for the frequency dependent gain of the active devices. The method is simple, versatile and modular. It utilizes the indefinite admittance matrix for the passive part of the SC network. The technique is illustrated with circuits based on OAs as well as UGAs and operated by a two phase clock. The method is also extended to SC networks operated by multiphase clocks.

Extensive numerical and experimental investigations have been carried out to substantiate the theoretical results. Lacking practical MOS fabrication facilities, the experimental circuits were implemented using discrete capacitors, CMOS switches and UGAs realized from OAs.

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DEDICATED TO

MY PARENTS

AND

MY (LATE) FATHER-IN-LAW

who were so anxious to see the successful culmination of the effort.

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t	: continuous time variable	...	28
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CHAPTER ONE

INTRODUCTION

1.1 GENERAL

A filter may be regarded, in a broad sense, as an electric circuit which supplies a prescribed response to a given excitation[1]. The response is usually different from the excitation in some specific ways, and is defined in terms of its behaviour in either the frequency or the time domain. Thus, a filter performs a function which is normally more sophisticated than the task of simple amplification or logical operations often encountered in electronics. Since the introduction of filter theory in the early part of this century, filters have found use in the generation, shaping and selection of wave forms in various areas of electrical engineering, such as, to mention but a few, communication circuits, control circuits and instrumentation. Depending upon the area and the frequency range of applications, the shapes, sizes and components in the filter change — ranging from microwave striplines to lumped RLC networks used in audio frequencies.

1.2 PRE-SWITCHED CAPACITOR ERA: PROBLEMS AND ACHIEVEMENTS

With the intense growth in the variety and number of applications, reduction in size as well as cost of the filters has become an important consideration to the users. This concern becomes acute for the lumped RLC filters in the audio and subaudio frequency

ranges. The technique of active RC filter design was introduced to respond to this consideration. An active RC filter contains active devices together with passive resistors and capacitors (RCs) and can duplicate the operation of a given RLC network. This is achieved by virtue of the gain of the active components which, when embedded in a suitable RC network, can generate complex pole pairs. It is these complex pole pairs that contribute to the frequency selective property in an electric filter. Advances in the theories and techniques of active RC filter design have been very rapid and significant for the past two decades. Industrial production of electrical filters operating in the low (audio and subaudio) frequencies is now feasible in the hybrid integrated circuit (IC) form. In this hybrid technology, the resistors and capacitors are fabricated using thin film or thick film technology while the active devices (usually operational amplifiers) are fabricated in the monolithic silicon IC technology[2]. This advance towards microminiaturization of filters is a significant one. However, a more preferred solution is the fabrication of the entire filter on a monolithic chip to make it compatible with the digital logic circuit chips.

1.3 MOS TECHNOLOGY IN THE EIGHTIES

Advances in solid state technology have made Metal Oxide Semiconductor (MOS) processes well established in the eighties for the realization of large scale integrated (LSI) digital circuits and subsystems such as memories and microprocessors. The use of microprocessors in automotive, consumer electronics and industrial

applications need interfacing with analog inputs and outputs. This can be achieved by incorporating analog to digital (A/D) and digital to analog (D/A) converters on the same chip. However, this solution may not be the most economical. Consequently, researchers have been led to examine several circuit elements in standard MOS processes having analog characteristics[3]. Most important amongst these are the MOS transistor switches, MOS capacitors and MOS operational amplifiers. It has been found that elementary signal processing operations such as addition, subtraction, multiplication by fixed coefficients and delay (sample and hold) can be performed using only precision ratioed capacitors, analog switches and operational amplifiers. The above operations are typically those that a sampled data filter or a digital filter performs on an input signal. It has also been recognized that a small capacitor switched at a frequency high compared to signal frequencies approximates a large valued resistor. Thus, a collection of capacitors, switches and amplifiers can produce the response, in the sampled data sense, of an analog RLC or active RC filter[4]. The capcitors, switches and the amplifiers, however, are now realizable in a monolithic MOS process. This has led to the concept of Switched Capacitor (SC) Filters and the era of monolithic analog filters using MOS processes.

1.4 SWITCHED CAPACITOR FILTERS: A BRIEF SURVEY

Research work in the area of switched capacitor filters (SCFs) has been vigorous in the past few years. Early workers exploited the equivalence between a passive resistor to the switched capacitor to

propose several basic SC building blocks, derived from the corresponding active RC circuit. Gradually, however, new problems were identified because of the sampled data nature of the SC network and dimensions of work in this area were broadened. SC networks equivalent to grounded inductors and floating inductors were discovered[5],[6]. Various facets of problems encountered in the area of active RC circuits were reviewed on the basis of the new circuit environment containing capacitors, periodically operated switches and amplifiers[7]. New analysis techniques, both in time domain and in frequency domain, were developed[7],[8],[11] and computer aided analysis programs, previously used for analog passive and active filters, were remodelled to analyze SC filter circuits[12],[13]. The amplifiers used in almost all the SCFs were MOS operational amplifiers (OAs) in the inverting mode. A limited number of realizations using unity gain amplifiers (UGAs) were also reported. However, the full potential of UGA based SCF realizations appears to have remained unexplored.

1.5 UNITY GAIN AMIPLIFIERS IN SC FILTERS

The reason for the popularity of OA based SCF realizations is not hard to guess. This is due to the large volume of work existing in the area of active RC circuits which use OAs. With such extensive work based on OAs, it is but natural to overlook the potential of a simpler, more cost effective but less known building block, viz., the UGA. In view of the possibility for monolithic fabrication, there are potentially several attractive advantages of using UGAs rather than

OAs. Firstly, there is the possibility of significant savings in the substrate area[14]. It is a reasonable expectation that a UGA can be fabricated using fewer MOS transitors than those needed to fabricate an OA. Thus, production of monolithic filters using UGAs should need much less substrate area and will be more economical compared with those using OAs. Apart from the fabrication viewpoint, there are other factors that may favour the use of UGAs. Two such factors are the economy in DC power consumption and the reduction in noise compared to what may be encountered in a realization using OAs[14]. These two factors are direct consequences of the smaller number of transitors in a UGA as compared to that in an OA. These factors may assume importance in cases where such filters are needed in large quantities and where the electronic circuit packages should perform with a high DC power efficiency (i.e., give desired operation with low DC power consumption) and with as little degradation in the signal to noise power ratio as is possible. One can visualize such an application in the area of aerospace systems. Finally another advantage, which may be less demanding at present, is the ability of a UGA to operate over a wider bandwidth compared to that of an OA[15]. This feature should assume importance as an extension of switched capacitor networks into frequency bands higher than voice band frequencies, presently used, is sought. A potential area would be in data communication links that employ adaptive equalizers[16]. Such equalizers are basically high order transversal filters. They may be realized by non-recursive sampled data filters and need a large number of building blocks capable of being switched at very high clock rates (> 10MHz). To arrive at an economical design, the individual building blocks should have a small

area, should consume minimal dc power and possess a large bandwidth. Consequently a UGA-based filter should become a preferred technological choice for these applications.

Perhaps the single most important drawback of the UGA, that has deterred researchers from exploring its potential in SCF realizations, is the unavailability of a virtual ground node at the input of the UGA. As a result, the response of the network becomes sensitive to the parasitic capacitances. It may be noted, however, that with the recent state-of-the art in MOS processes, values of such parasitic capacitances can be accurately estimated and included in a particular design[17]. Also, processes have been evolved where such parasitic capacitances have exteremely small values[18],[19].

1.5.1 Realizations Using Unity Gain Amplifiers

The work done in the area of SCFs using UGAs can be broadly classified under three categories, viz., (i) component simulations; (ii) LC ladder filter simulation; and (iii) transfer function simulations. A combination of UGAs, OAs and switched capacitors have been used[5],[6] to realize floating inductors and resistors that approximate the incremental charge-voltage relations corresponding to the bilinear transformation. This has been used to implement an SC version of equally terminated RLC ladder network which is approximately equivalent to the passive prototype RLC ladder. The concept of switched capacitor transconductance and related building blocks has been introduced and realizations of inductors, gyrators, negative

conductances and biquadratic functions (in the variable z^{-1}) have been given[20]. The idea of voltage inverter switches (VIS) using UGAs has the potential to replace, element by element, the components of an LC ladder by a corresponding SC network which could preserve the bilinear mapping between s and z domain. However, terminating resistors cannot simulate the bilinear mapping and thus the bilinear equivalence between the prototype RLC and the SC networks is not complete[21],[23]. Further, these realizations need a more complicated clocking scheme instead of the simple biphase operations used extensively. The realizations are strongly stray sensitive. While bottom plate stray insensitivity can be attained by modifying the topology, the top plate parasitics remain a problem. Some work has been reported to eliminate the effect of such parasitics, but these need additional components (capacitors) and devices (switches, OAs) and sometimes an elaborate clocking scheme[23],[25]. Thus the homogeneity of the active building block (viz., only UGAs or only OAs) is lost in the synthesis procedure. Also the considerations such as minimization of substrate area etc., are compromised. In the category of transfer function simulations, the standard analog biquadratic transfer functions have been realized using SC networks and UGAs. Many of the proposed designs are derived from canonic RC-active filters and hence are canonic, containing only two UGAs and four capacitors [15],[26],[27]. However, almost all of the realizations fail to generate the sampled data transfer functions (SDTFs) that are bilinear counterparts of the corresponding analog biquadratic transfer functions. The only SC network that corresponds to the bilinearly transformed analog counterpart is the high pass one and is limited to low Q_p and low f_p (relative to the clock rate f_s

used) realizations, requiring $\omega_p Q_p < f_s$[27]. Moreover, because of the canonic structures, scaling of the flat gain of the filter is imperative, sometimes by a large factor. This could make such filters unacceptable in applications where no degradation of signal-to-noise power ratio can be tolerated as the signal is processed by the filter. Also, as in the cases of component simulation and LC ladder simulation networks, the effects of stray capacitances, especially those associated with the top plates of the network capacitors have not been considered in these realizations.

It therefore appears desirable to investigate in a systematic and critical manner realizations of SCFs using switches, capacitors and UGAs. In this context, it is worthwhile to review briefly the characteristics of these components fabricated in MOS technology. The SCF realizations presented in this thesis are based on the availability or potential availability of these components.

1.6 MOS SWITCHES, CAPACITORS AND UNITY GAIN AMPLIFIERS

1.6.1 MOS Switches

A MOS transistor (MOST) can function as a good analog switch. The cross sectional structure of a p-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is shown in Figure 1.1[28]. The device consists of two closely spaced, degenerately doped p^+ regions, the "drain" and the "source" which have been diffused into a lightly doped n-type silicon substrate. A thin insulating layer of silicon

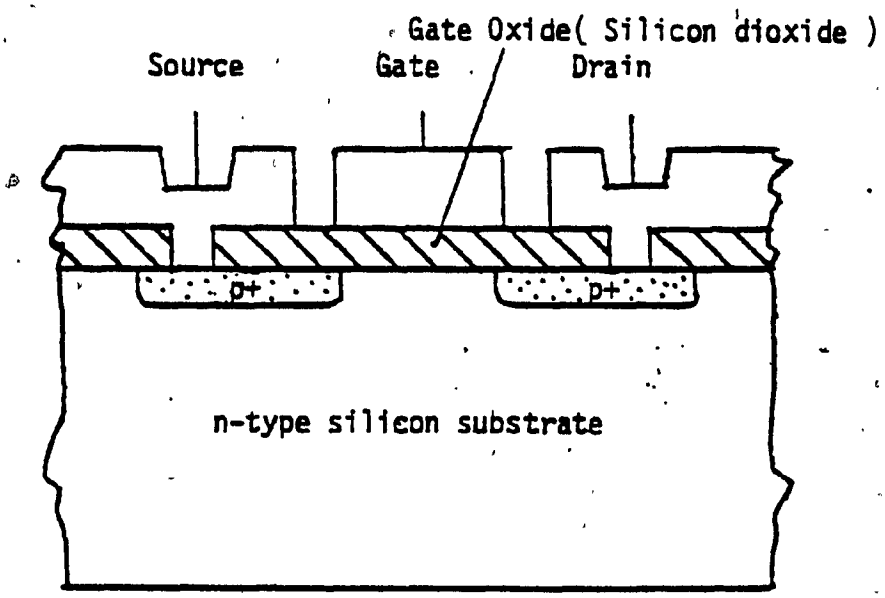


Figure 1.1: Cross section of a p-channel MOSFET

dioxide is formed directly above the region separating the two p^+ diffusions by oxidizing the surface of the silicon at high temperature in an oxygen-rich environment. Metal contacts, usually aluminium, are made to both diffused regions and a "gate" electrode is positioned directly over and completely covering the region between the drain and source. For proper operation, the gate electrode must be a highly conductive material and aluminium is most widely used. However, a great deal of work has been done using both highly doped poly-crystalline silicon and other metals (e.g., gold, titanium). Although the gate electrode need not be of metal and the insulator need not be an oxide, the term metal-oxide semiconductor (MOS) generally relates to the more conventional gate structure consisting of a metal electrode which is separated by a thin layer of oxide from the underlying semiconductor substrate. The structure of an n-channel MOSFET (NMOS) is similar to the device shown in Fig. 1.1, except that n^+ regions are diffused into a p-type silicon substrate. When associated with on chip MOS capacitors, the standard MOS transistor performs as a nearly ideal zero-offset analog switch. In simple NMOS or PMOS circuits, the threshold drop limits dynamic range to one threshold less than the supply voltage. This may not be a serious limitation. The time constant formed by the ON resistance (few kilo ohms) of a small MOS transistor times the capacitance of the largest desirable on-chip capacitor (about 100pF) is usually below 100 ns. Thus, accurate voltage settling to within 0.1 per cent of final value is normally attained in under 1 μsec. This is adequately fast for a very broad range of applications. MOS transistor analog switches can accurately switch voltages to nodes with infinite DC impedance (e.g., capacitors

or MOS transistor gates). These analog switches are, however, not satisfactory for accurate switching of voltages into a resistive load; the magnitude and variability of the switch ON resistances are too great for this purpose[29]. The junction leakage currents of MOSTs may cause slow voltage drifts which reduce the dynamic range available for signals. For a 10pA leakage current, 1 millivolt of offset appears on a 10pF capacitance in 1 milli sec. These are typical numbers and may cause no problem for most applications. The lumped circuit parameters in a typical NMOS together with a cross sectional representation is shown in Figure 1.2. The parasitic overlap capacitances from gate-to-source or gate-to-drain of MOSTs used as analog switches can introduce DC offset at signal nodes. These may be too small to be of any consequence in most AC coupled systems. In DC coupled systems, these parasitic induced offsets can be reduced to 1 millivolt or less with techniques such as charge cancelling circuits[3]. Further, the parasitic capacitances to substrate or ground have no effect if signal nodes are voltage driven or are at virtual ground. Modern MOS processes employing local oxidation and silicon gate processes to achieve self-alignment of field-to-transistor regions and of gate-to-source and drain regions exhibit extremely small values of the various parasitic capacitances mentioned above. A typical fabrication sequence for self aligned PMOS integrated circuit which combines diffusions and ion implantation techniques is shown in Figure 1.3[28]. With the position of the gate electrode in between the diffused source and drain regions in Fig. 1.3(a), the thin oxide layer in the intervening space is bombarded with high energy boron ions so that the silicon regions between the gate electrode and the diffused p^+ areas are implanted with

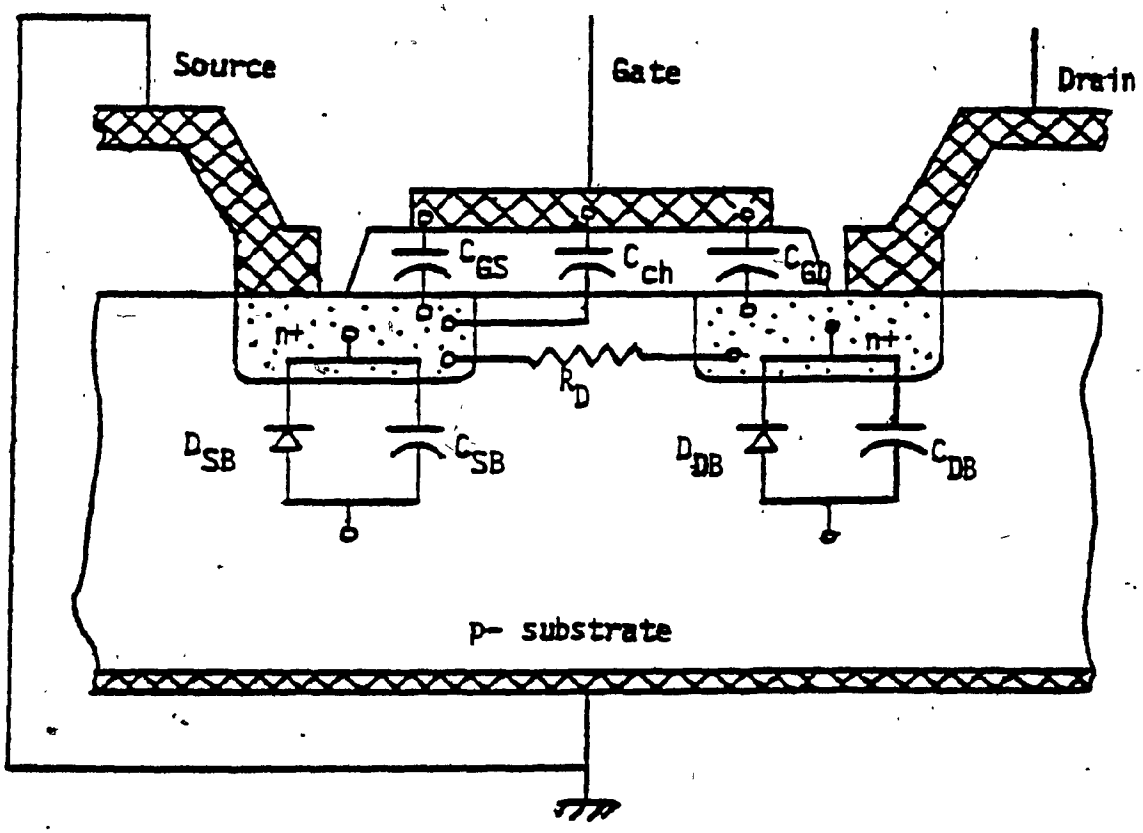
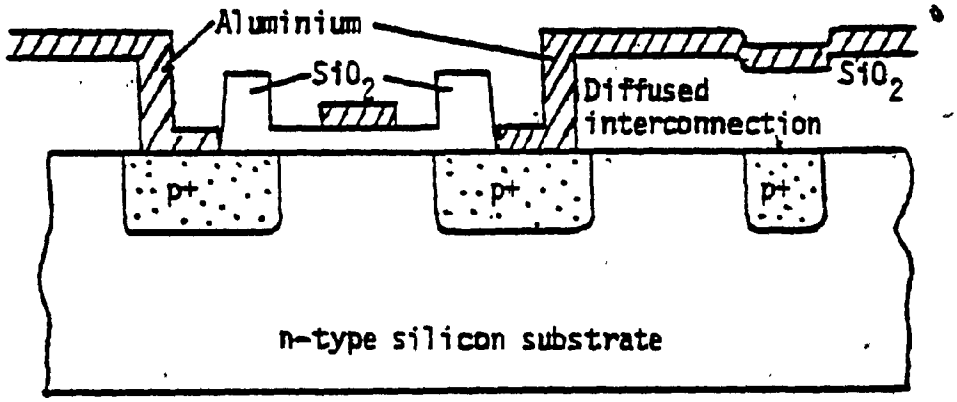
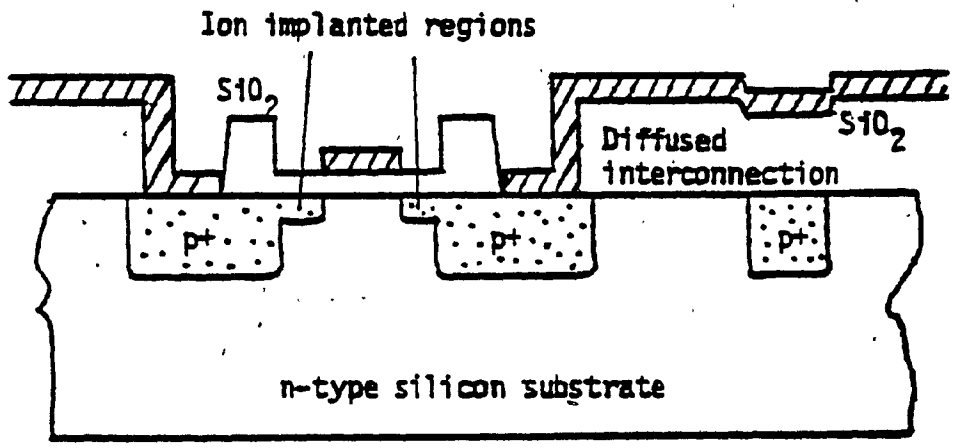


Figure 1.2: Cross-sectional representation of an n-channel MOSFET with associated discrete components to be used in an equivalent circuit model



(a)



(b)

Figure 1.3: Fabrication of self-aligned p-channel MOSFET through the use of ion-implantation

boron, thereby extending the drain and source regions up to the gate electrode and resulting in almost perfect alignment. [Fig. 1.3(b)]. The order of reduction in the parasitic overlap capacitance achieved in the self-aligned ion-implant MOSFET relative to the non-self-aligned processes can be appreciated from Figure 1.4 which shows the dependence of the gate-to-drain (source) negative feedback capacitance on the amount of overlap of the gate electrode over the drain region. The lower abscissa corresponds to a gate oxide thickness of 2000 Å. The bracketted lines represent the range of experimentally measured values for conventional MOSFETs and silicon gate and ion-implanted devices. It can be seen from these experimental data that extremely small values of interelectrode overlap can be achieved through the use of ion implantation to fabricate MOSFET structures. Typical values of the overlap parasitic capacitances that can be achieved nowadays is under 1fF ($=10^{-15}$ Farad) while the parasitic capacitances from source (drain) to substrate can be held below 10fF. Thus, these capacitances may rarely become a limitation on overall circuit or subsystem characteristics.

1.6.2 MOS Capacitors

The classical MOS capacitor exists in the MOS transistor structure between the metal top plate (gate) and the lightly doped bottom plate (source-drain) with the insulating silicon dioxide layer as the dielectric. This kind of capacitor is, however, not useful in precision D/A converters or in precision frequency filters because of large voltage coefficient of capacitance near the MOS transistor

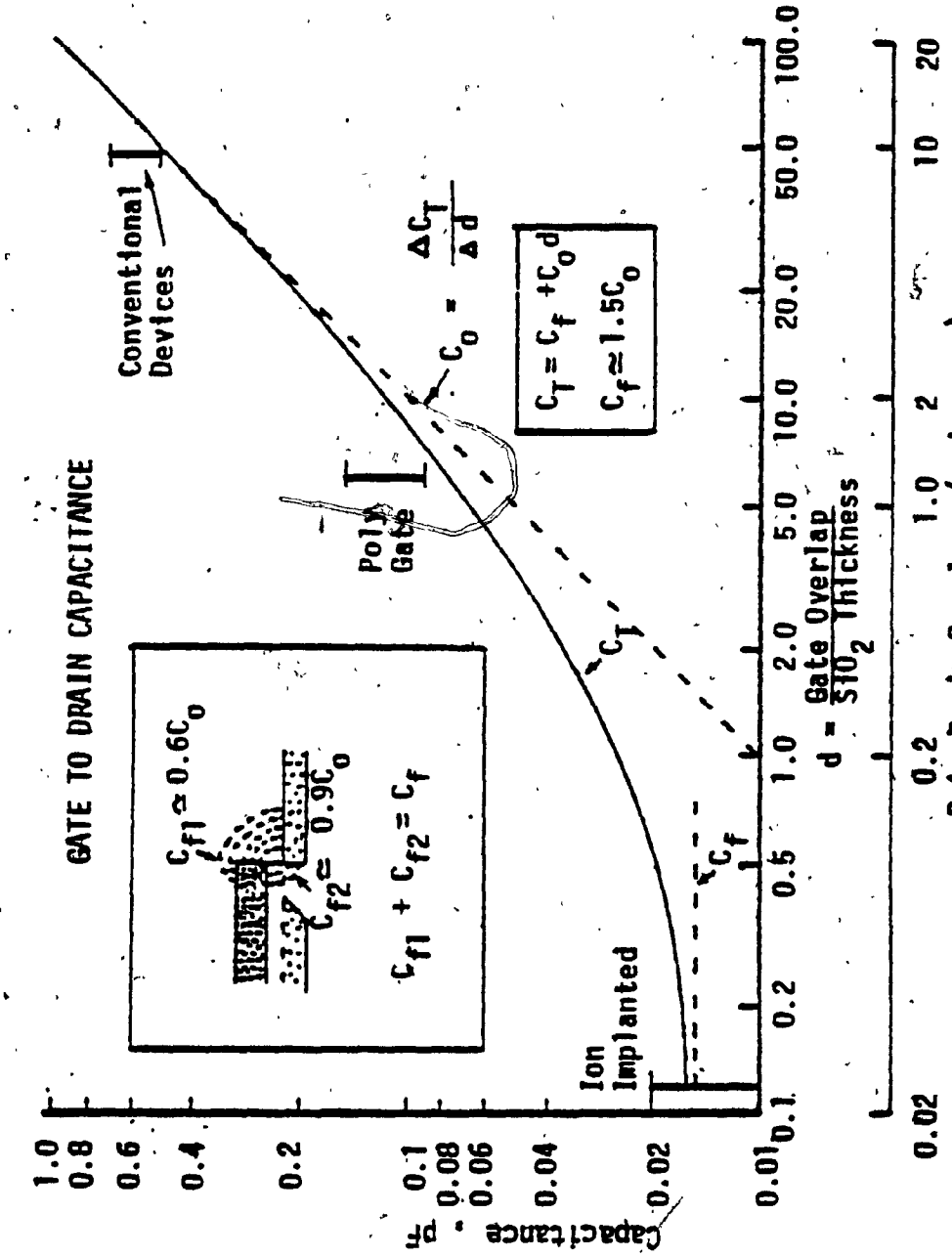


Figure 1.4: Miller feedback capacitance produced by the overlap of the drain by the gate

threshold voltage. Also large non-linearity (more than 0.1% per volt) exists with regard to applied voltages[29]. Four basic types of MOS capacitors are now used in practice. These are classified according to the processes, viz., (a) Metal-Gate, (b) Metal-Poly, (c) Silicon-Gate and (d) Poly 1 – Poly 2 process[18],[29]. The metal gate MOS processes (PMOS, NMOS, CMOS) inherently provide an excellent capacitor with a metal top plate, gate oxide as dielectric and n^+ or p^+ source-drain as bottom plate. Figure 1.5 shows an example. In the metal-poly process, the bottom plate of the capacitor is formed by utilizing a heavily doped (low resistance)region of the silicon substrate. This particular capacitor type is best suited to metal gate CMOS and MOS processes which do not use self-alignment procedures and can thus realize the capacitor directly without process modifications. An example of this type of capacitor is shown in Figure 1.6[19]. In the silicon gate process, a masked implant or diffusion of polarity opposite to that of the substrate is added at the very beginning of the processing sequence. This becomes the bottom capacitor plate. A thin layer of thermal oxide forms the gate oxide. A polycrystalline silicon layer forms the top plate. Fig. 1.7 shows an example of this capacitor structure. The process involved here runs in a reverse sequence as compared with the metal-poly capacitor structures. The poly 1 – poly 2 capacitor structures can be easily derived from silicon gate MOS processes with two layers of polycrystalline silicon, such as standard processes used for electrically programmable read-only memories (EPROMs). The dielectric should be thermally-grown silicon dioxide, obtained by oxidizing poly-1 layer to a thickness of 1000-2000 Å. A typical cross-section is shown in Figure 1.8. Capacitors made by this process may be

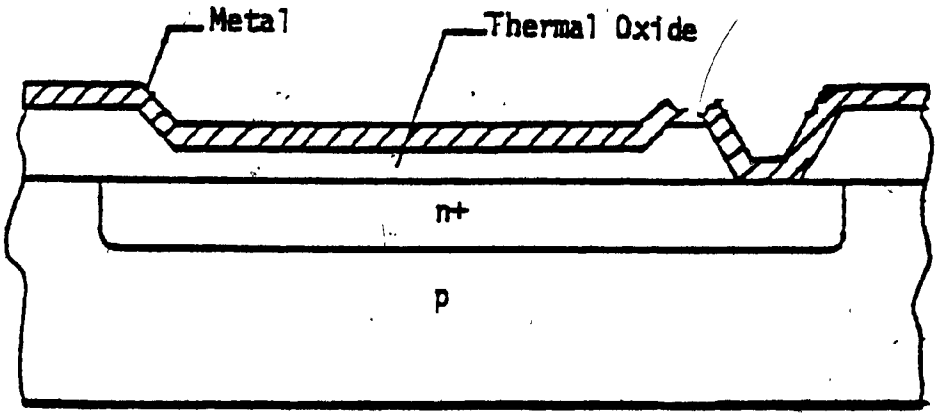


Figure 1.5: MOS capacitor with metal top plate; n+ bottom plate as formed in metal-gate NMOS or CMOS

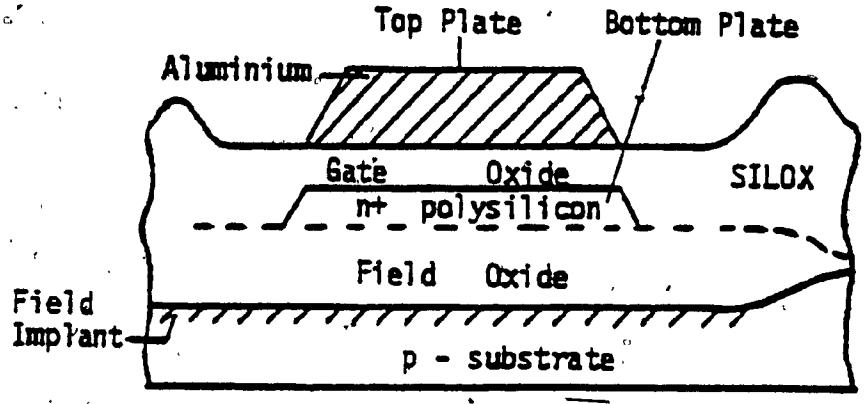


Figure 1.6: MOS capacitor as formed in metal-poly process

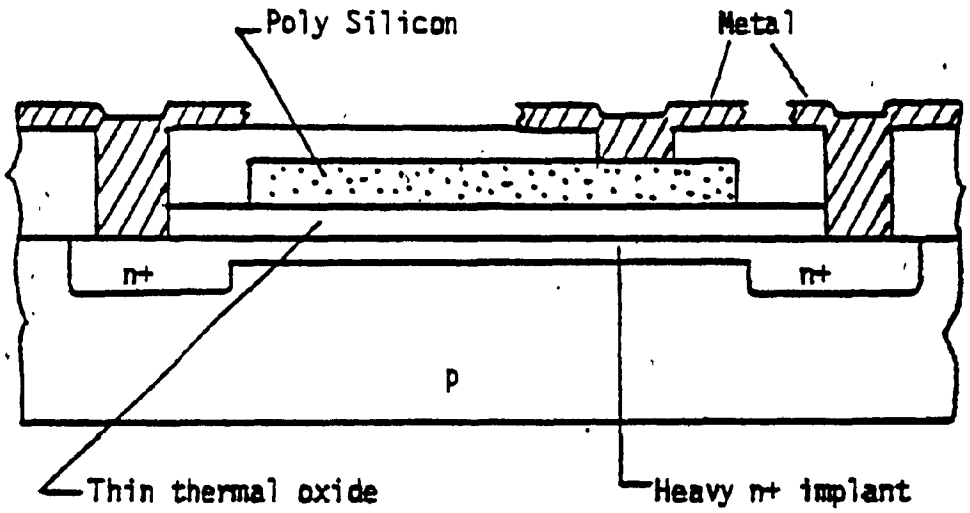


Figure 1.7: Capacitor with poly silicon as top plate and heavily implanted bottom plate, as formed in silicon gate MOS process with an extra implant mask

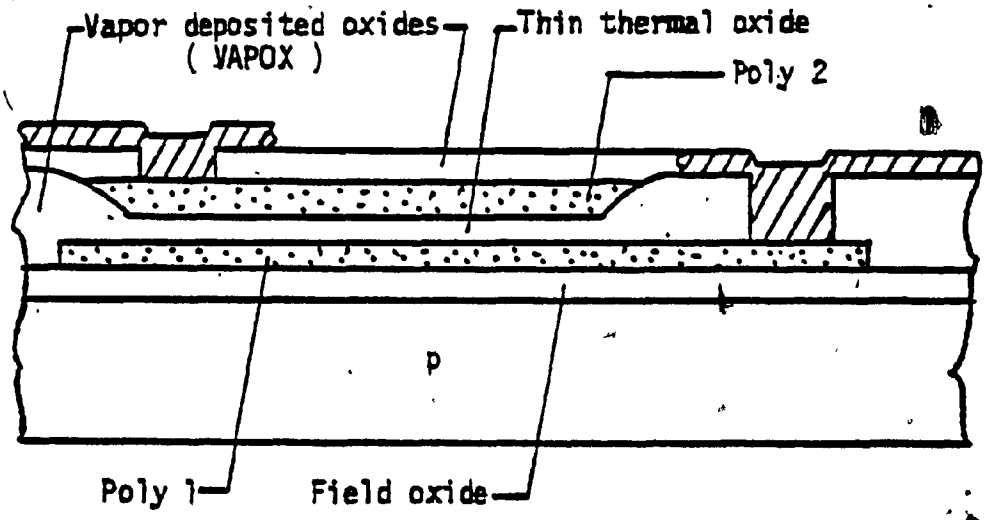


Figure 1.8: MOS capacitors formed between two layers of polysilicon. The oxide dielectric is formed by thermally oxidizing poly 1 before depositing poly 2

trimmed by using silicon fuses.

The capacitance structures mentioned above tend to have common characteristics. From the standpoint of SC filters, the most important ones are[30]:

(a) Ratio Accuracy:

A key aspect of the performance of any frequency selective filter is the accuracy and reproducibility of the frequency response. For SC filters this requires a certain level of accuracy in the ratios of capacitors. The achievable ratio accuracies in MOS capacitors are very good, being better than 1% in most of the cases, while a value of 0.1% is quite common.

(b) Voltage Coefficient and Temperature Coefficients:

This depends upon the MOS process employed to fabricate the capacitor. MOS capacitors made with heavily doped silicon plates display voltage coefficients in the range of 10 to 100 ppm/volt. Temperature coefficients are generally in the range from 20 to 50 ppm/^{o}C. The values are of course much lower for the ratios. These variations are low enough to be insignificant in almost all applications.

(c) Parasitic Capacitances:

In both poly 1 – poly 2 and metal-silicon capacitor, the parasitic component arises out of the p-n junction surrounding the heavily doped region. Typically, this capacitance may have a large value, ranging from 5% to 20% of MOS capacitor itself depending upon the fabrication

process. Also, because the top plate of the MOS capacitor must be connected to other circuitry, a small capacitance will exist from the top plate to the substrate due to the interconnections. This could be about 0.1% to 1% of the desired MOS capacitance and can be reduced to a negligible proportion by proper layout. The parasitic capacitance from the top plate of the MOS capacitor, due to the structure of the capacitor itself, is again process dependent. For fabrication processes which do not use buried contacts and which use self-alignment steps, such parasitic capacitances are very small, amounting to less than 10fF in most cases[17].

The parasitic capacitances mentioned above are unavoidable and the design of SC filters must be done in such a way that these do not produce noticeable degradation in the filter performance.

1.6.3 MOS Unity gain Amplifiers (MOS UGAs)

The schematic of a UGA, in the simplest form, using MOSTs is shown in Figures 1.9(a)-(b)[31]. These simple circuits shall have a low frequency gain which will be less than unity because of the body effect. As is done with MOS operational amplifiers (OAs), the body effect can be reduced via increases in substrate resistivity[3]. Also, using CMOS technology, the body effect can be eliminated by connecting the p-well of the transistor to its source. More refined forms of UGA whose gain shall be very close to unity and which use CMOS process are shown in Figures 1.10(a)-(b)[14]. A UGA circuit that has been fabricated and tested using CMOS technology and metal gate process, is

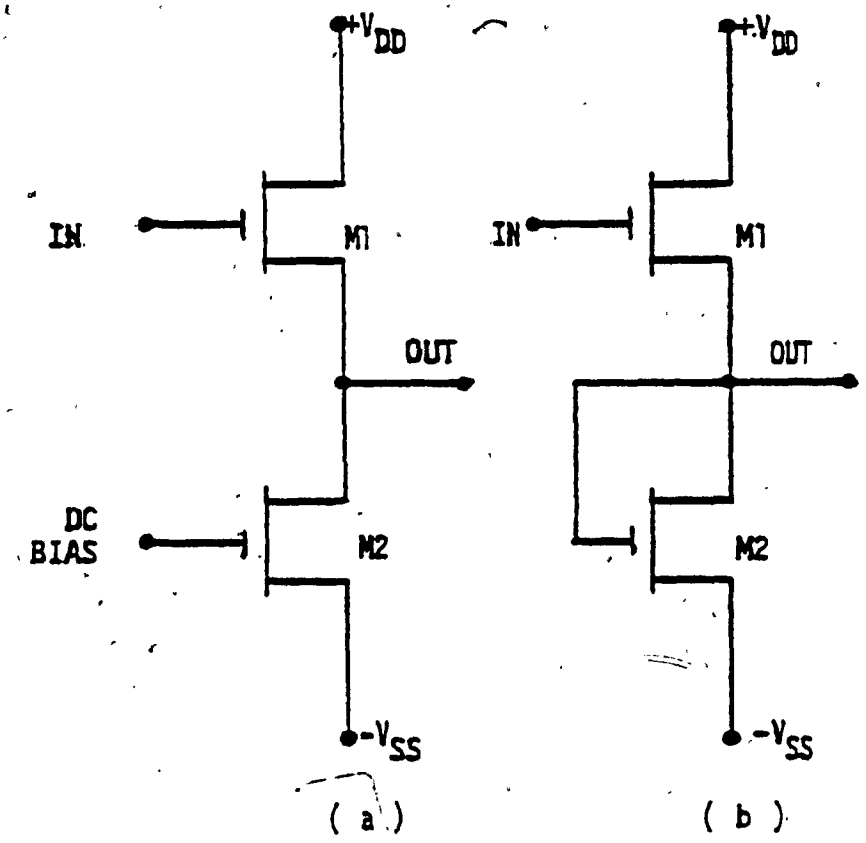
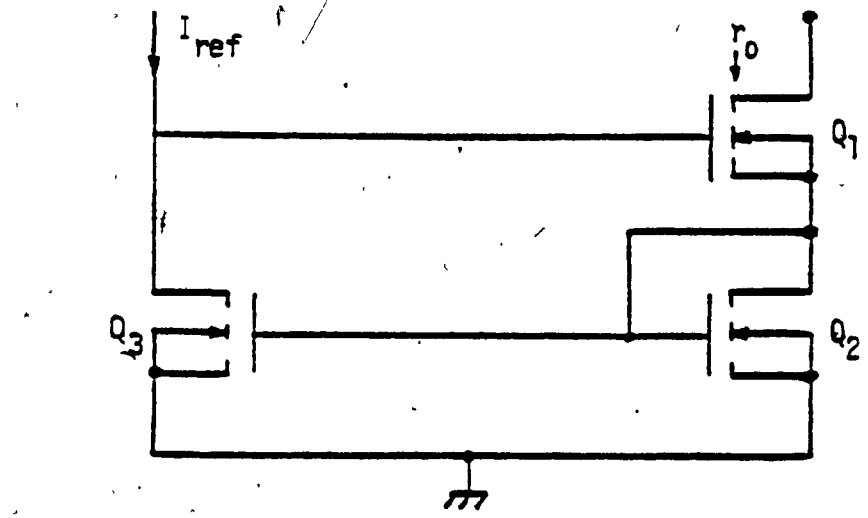
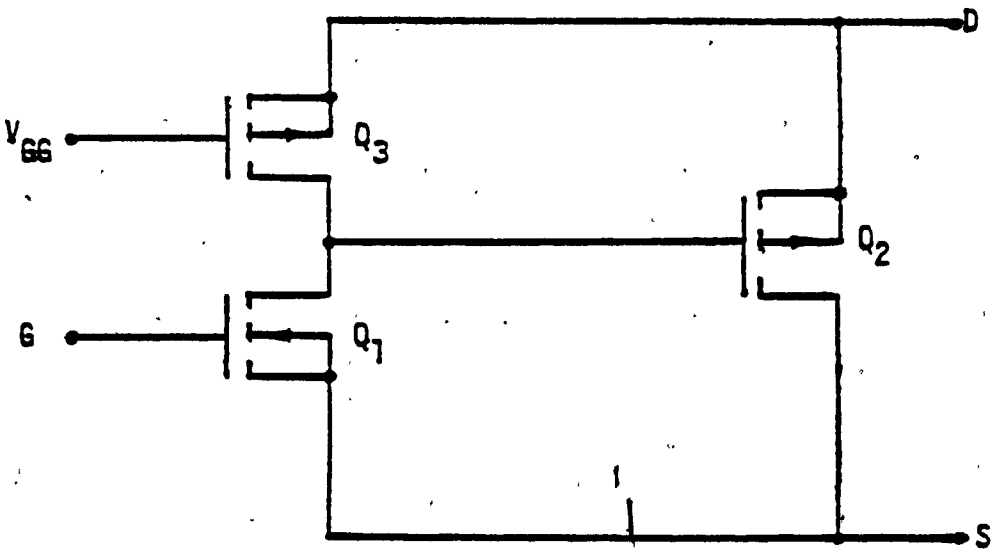


Figure 1.9: MOS buffers in the simplest forms



(a)



(b)

Figure 1.10: Improved MOS buffers with gain very close to unity. (a) a three transistor circuit which increases the output resistance by using a current source load, (b) a CMOS configuration which increases the input transconductance

shown in Figure 1.11[32] with its typical electrical characteristics shown in Table 1.1. It may be expected that with more advancement of technological processes, MOS UGAs of comparable or even better characteristics (wider unity gain bandwidth, lesser power dissipation etc.) could be fabricated using even fewer MOSTs.

1.7 SCOPE OF THE PRESENT WORK

The aim of this thesis is to develop systematic synthesis procedures for sampled data transfer functions (SDTFs), recursive and non-recursive and of any order using UGAs, switches and capacitors. Biquadratic SDTFs (BIQ-SDTFs), bilinearly equivalent to their analog counterparts, and tolerant of the various parasitic capacitances in the circuit, are given special attention. Further, a method is developed for examining the effect of the frequency dependent gain of the active device, UGA or OA, on SDTF realizations.

Towards this end, the basic building blocks that are needed to synthesize an SDTF are developed in Chapter 2 from fundamental principles and using only switches, capacitors and UGAs. Schemes to obtain both non-recursive and recursive SDTFs are presented. A topology is also given for the realization of a BIQ-SDTF.

In Chapter 3, the topology described in Chapter 2 for the realization of BIQ-SDTFs is examined at length. In particular BIQ-SDTFs that are bilinearly equivalent to their popular analog counterparts (LP, HP, BP, notch and AP) are examined in detail. Several practical considerations such as sensitivity of filter

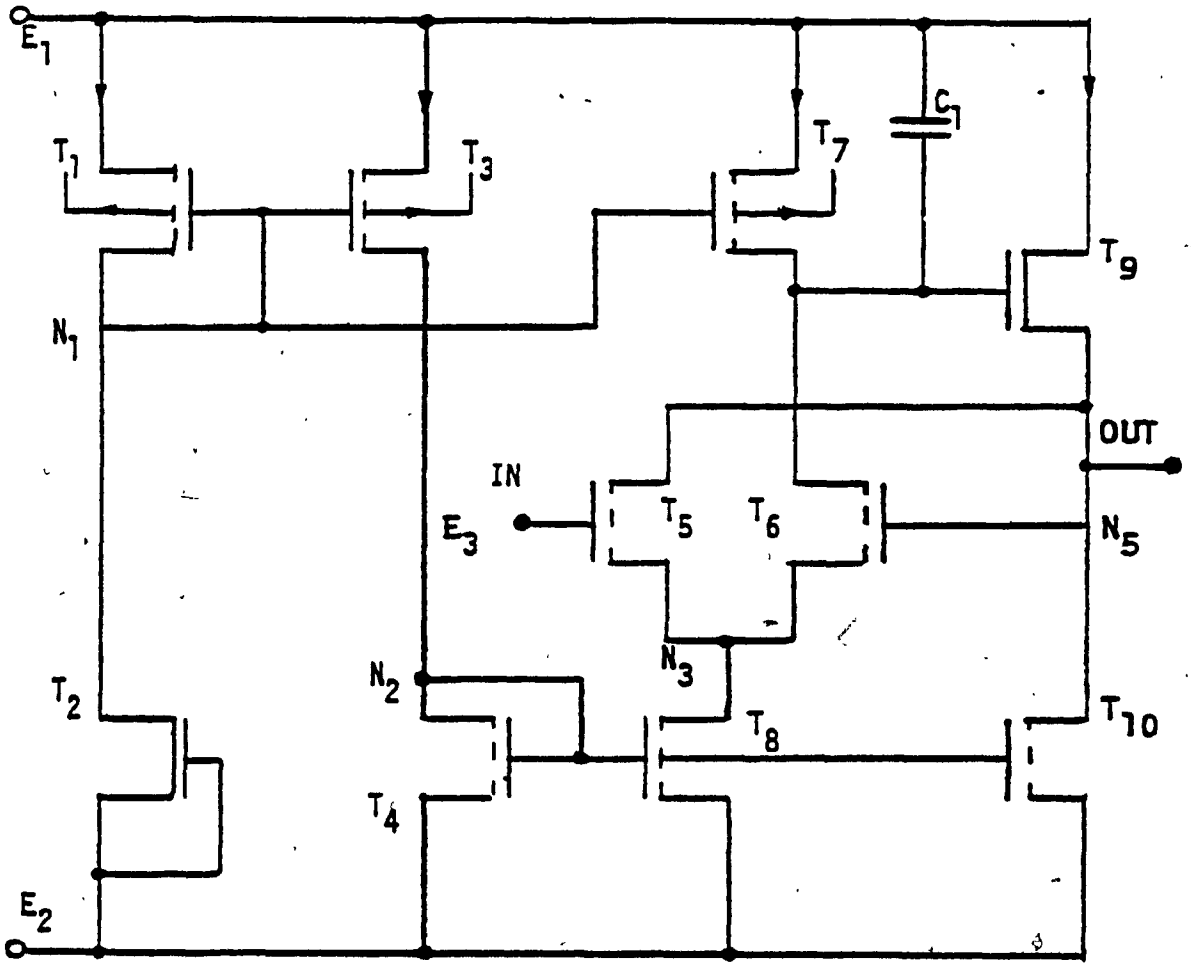


Figure 1.11: Circuit diagram of a unity gain amplifier integrated employing a standard CMOS metal gate process

TABLE 1.1

PERFORMANCE PARAMETERS OF

UNITY-GAIN BUFFER

Power supply voltages	± 5 V
Power dissipation	3.5 mW
Open loop gain	60 dB
Unity gain bandwidth	3MHz
Slew rate	> 10 v/μs
Chip area	0.1 mm^2

parameters (ω_p, Q_p) on capacitance ratio accuracies, effect of sample-hold capacitors, parasitic capacitances etc., are discussed. An opimization algorithm that renders the designs parasitic tolerant while requiring a minimum total capacitance is developed.

Chapter 4 presents an improved topology which requires a reduced number of capacitors, switches and UGAs for the realization of BIQ-SDTFs. Introducing a new building block (composite delay and add), it is shown that the general BIQ-SDTF can be realized using only two UGAs and at most ten capacitors. These are about the same number of components and devices needed to realize BIQ-SDTFs using OAs. Sensitivity properties and the effect of the parastic capacitance as well as the offset voltages in UGAs on the realizations are investigated. Optimization alogorithms that would make the designs parasitic tolerant as well as minimize the detrimental effects of the offset voltages are described. The algorithms also lead to a minimum total capacitance design. A topology that needs almost the minimal number of capacitors and can yield BIQ-SDTFs that are bilinearly equivalent to the analog LP, HP and BP filters is also proposed. The resulting filters are, however, limited to low Q_p and low f_p (relative to the clock frequncy f_s) applications.

Chapter 5 describes an analysis technique to account for the non-ideal DC gain as well as the finite gain bandwidth (GB) product of the active devices on the SDTF realizations. The technique is based on the one pole model of the active devices. It is shown that the analysis is applicable to any OA as well as UGA realizations of the

SDTFs. The analysis method is principally a frequency domain method and uses the indefinite admittance matrix (IAM) of the given passive SC network[11]. The technique is general, versatile and simple to use. The method is applied to estimate the effects of the frequency dependent gain of the UGAs on the BIQ-SDTFs developed in Chapter 4.

To test the validity of the various theoretical analyses, several SCFs were designed and tested in the laboratory. For lack of proper fabrication facilities, the filters were implemented using discrete components and UGAs realized from OAs. Extensive numerical and experimental results are provided to illustrate and substantiate the theoretical investigations.

Chapter 6 summarizes the various theoretical and experimental investigations presented in the thesis. The chapter concludes with suggestions for future improvements and potentials for futher research work.

CHAPTER TWO

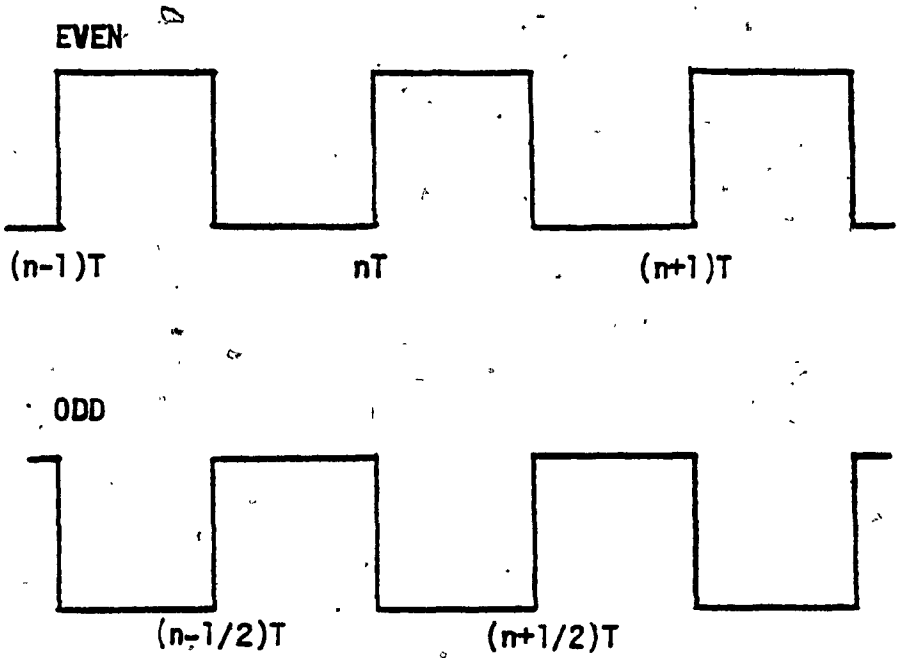
REALIZATION OF GENERAL SAMPLED DATA TRANSFER FUNCTIONS

2.1 INTRODUCTION

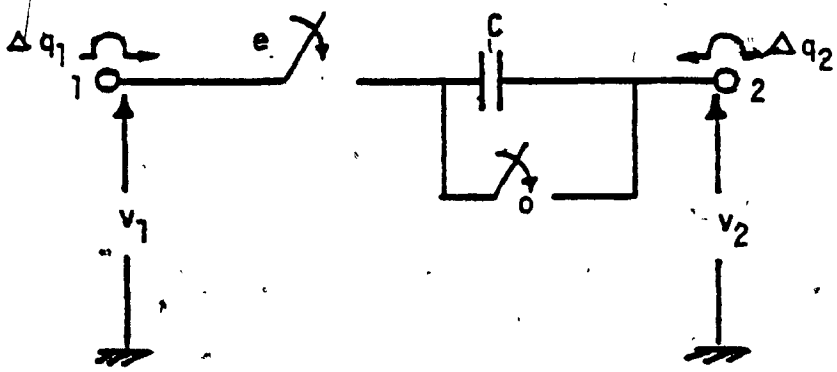
This chapter introduces a systematic approach for realizing SDTFs utilizing very basic principles and employing only UGAs and SCs. The building blocks needed in the realization are described first. Realizations of general SDTFs are developed next. They reveal the possibliity of realizing both non-recursive and recursive filter transfer functions. Sensitivity analysis of the resulting general SDTFs is given. Realization of a special class of non-recursive SDTF (NR-SDTF), viz., linear phase filters, is considered in some detail. The effects of sample-hold spectral shaping, on the filter response, is discussed and a method is suggested to reduce this effect. A topology for second order SDTF is also suggested. The chapter is concluded with experimental results on a number of SDTFs implemented in the laboratory using discrete capacitors, CMOS switches and UGAs realized from OAs.

2.2 BASIC BUILDING BLOCKS

In the following, we shall assume that the switches in the SC network are operated by the two phases (even and odd) of a square wave clock signal with a period T sec. Also, without loss of generality, we assume that $t = nT$ ($n = 1,2,3,\ldots$) refers to the start of an "even" clock interval [Fig. 2.1(a)] so that $t = (n \pm \frac{1}{2})T$ would refer to the



(a)



(b)

Figure 2.1: (a) The two phases of the clock signal, and
(b) The Open Circuit Resistor.

start of an "odd" clock interval. Further, assume that Δq_i represents the incremental charge flow into (or from) the capacitor C from (or to) the node i, through the corresponding switch (even or odd phased) [Figures 2.1(b)-2.1(d)].

2.2.1 Open-Circuit Resistor (OCR)

Consider now Figure 2.1(b), where

$$\Delta q_1(nT) = -\Delta q_2(nT) = C[v_1(nT) - v_2(nT)] \tag{2.1a}$$

$$\Delta q_1[(n + \tfrac{1}{2})T] = -\Delta q_2[(n + \tfrac{1}{2})T] = 0 \tag{2.1b}$$

Thus, this element acts as a resistor between nodes 1 and 2 during even clock phases and acts as an open circuit during odd clock phases. This unit will be called as an open circuit resistor.

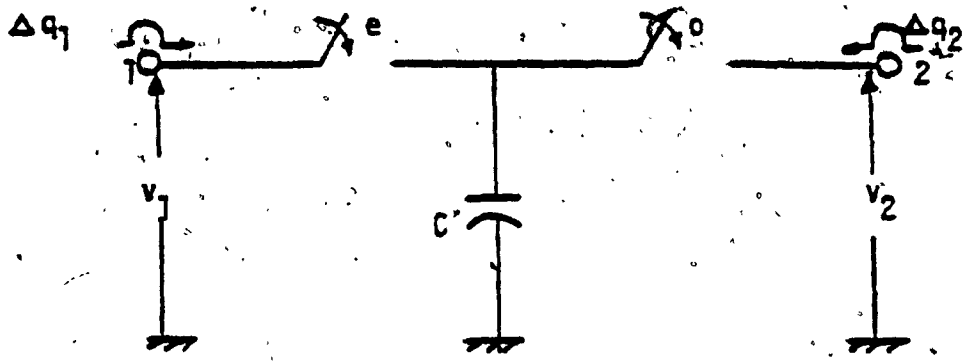
2.2.2 Toggle-Switched Capacitor (TSC)

For the circuit of figure 2.1(c) one has

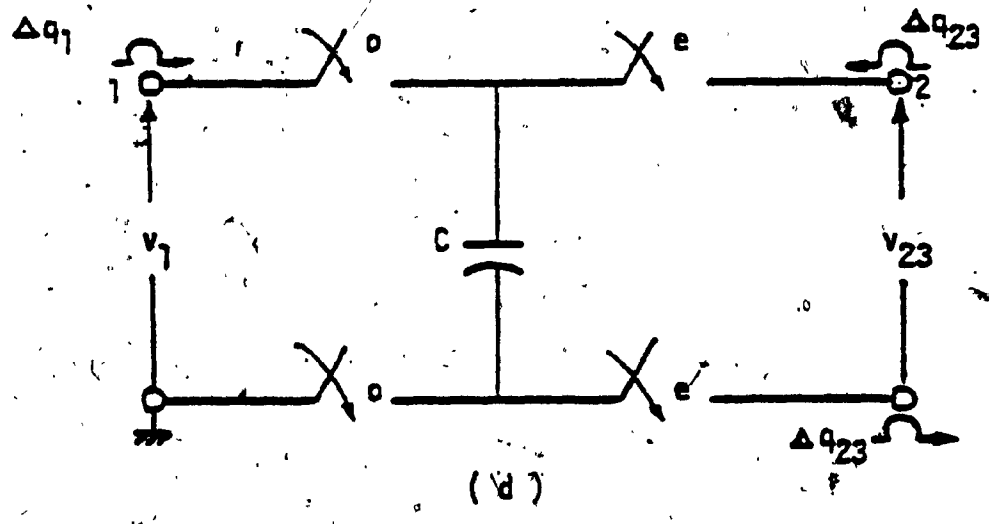
$$\Delta q_1(nT) = C\{v_1(nT) - v_2[(n - \tfrac{1}{2})T]\} \tag{2.2a}$$

$$\Delta q_2[(n + \tfrac{1}{2})T] = C\{v_2[(n + \tfrac{1}{2})T] - v_1(nT)\} \tag{2.2b}$$

$$\Delta q_2(nT), \quad \Delta q_1[(n + \tfrac{1}{2})T] = 0 \tag{2.2c}$$



(c)



(d)

Figure 2.1: (c) The Toggle Switched Capacitor, and

(d) The Toggle Switched Differencer

If port 2 is an open circuit, one shall have $\Delta q_2[(n + \frac{1}{2})T] = 0$, making $v_2[(n + \frac{1}{2})T] = v_1(nT)$. Thus, the TSC with an open circuited output node acts as a simple sample-and-hold circuit (SH), offering a delay equal to one-half of the clock period.

2.2.3 Toggle-Switched Differencer (TSD)

For the circuit of Figure 2.1(d), one has

$$\Delta q_1[(n - \tfrac{1}{2})T] = C\{v_1[(n - \tfrac{1}{2})T] - [v_2(nT) - v_3(nT)]\} \qquad (2.3a)$$

$$\Delta q_{23}(nT) = C\{[v_2(nT) - v_3(nT)] - v_1[(n - \tfrac{1}{2})T]\} \qquad (2.3b)$$

$$\Delta q_1(nT), \quad \Delta q_{23}[(n - \tfrac{1}{2})T] = 0 \qquad (2.3c)$$

If the output nodes are short-circuited at $t = nT$, it follows $v_2(nT) - v_3(nT) = 0$, thereby making $\Delta q_{23}(nT) = -\Delta q_1[(n - \frac{1}{2})T]$. A TSD with a short-circuited output node pair acts as a charge transfer circuit with half a clock period delay.

2.2.4 Unity Gain Amplifier (UGA)

An SC network operates by charging a set of capacitors during one clock phase and redistributing the acquired charge to another set of capacitors, in a desired manner, during the next clock phase. Formulation of such redistribution becomes very simple if a capacitor, after having acquired a known amount of charge, can be completely

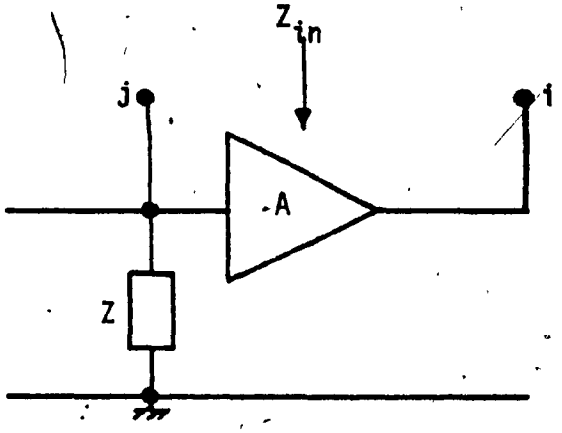
discharged across a node pair in such a way that the node pair by itself does not allow a flow of charge through it but diverts the entire discharge to some other nodes through a defined set of switched (or unswitched) capacitors.

Consider now an ideal voltage amplifier of gain A [Fig. 2.1(e)]. The input impedance (Z_{in}) looking into the terminals i-j is Z(1 - A). For a UGA A = 1 and Z_{in} becomes zero. Similarly, the admittance (Y_{in}) seen between the node j and ground is Y(1 - A) [Fig. 2.1(f)] which too becomes zero when A = 1. Thus, if a charged capacitor is placed across nodes i-j of a UGA with a load impedance Z connected between node j and ground, the capacitor sees zero impedance and will discharge instantaneously, independent of the value of Z. On the other hand, the admittance Y_{in} is zero irrespective of the value of the capacitance placed between i-j. Thus, the entire charge from the capacitor shall flow through the load impedance Z. We see, therefore, that a UGA can serve precisely the purpose of redistribution of charges among the capacitors as mentioned above. If a voltage sampling capacitor is connected periodically between the nodes i-j, its charge, acquired at the sampling port, will entirely flow through Z, producing a charge proportional to the input voltage.

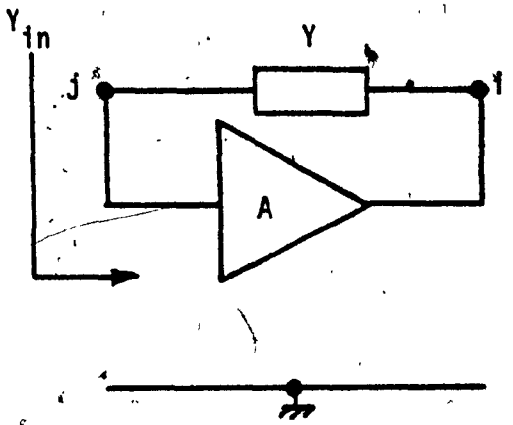
2.3 SAMPLED DATA FILTER REALIZATIONS

2.3.1 Delay and Add (or Subtract) Network

Using the various blocks already presented, a delay and add



(e)



(f)

Figure 2.1: (e) The Z_{in} across the input and output of an ideal voltage amplifier of gain A, and (f) The Y_{in} at the input of the amplifier

network can be realized. Such a network is shown in Figure 2.2(a), and is central to our realization of the sampled data network functions. During even clock phases, [say, $t = (n - 1)T$], the input v_i is sampled and held in C_{Xi}. At the same time, the input is fed through C_{IN} to the summing node X. In the next half interval, i.e. with a delay of T/2, C_{Xi} transfers the charge held earlier to C_{1N}. The capacitor C_{1N} discharges after another half interval delay of T/2, since it is then connected across the UGA, transfering the whole charge through node X to C_{ON}. One thus obtains the charge conservation equation (CCE):

$$C_{ON}v_O(nT) = C_{IN}[v_i(nT) - v_O(nT)] + C_{1N}v_i[(n - 1)T] \qquad (2.4a)$$

Taking $\mathcal{Z}$-transforms of both sides and rearranging the terms, one has

$$V_O(z) = \frac{C_{IN}}{C_{ON} + C_{IN}} \left[1 + \frac{C_{1N}}{C_{IN}} z^{-1}\right] V_i(z) \qquad (2.4b)$$

It is clear that if one interchanges the terminals A and B of C_{1N} in Fig. 2.2(a), one could arrive at

$$V_O(z) = \frac{C_{IN}}{C_{ON} + C_{IN}} \left[1 - \frac{C_{IN}}{C_{IN}} z^{-1}\right] V_i(z) \qquad (2.5)$$

The network of Fig. 2.2(a) shall henceforth be designated as Type-1 delay and add (DA-1) network. Similarly, for the network of Fig. 2.2(b), one can arrive at:

$$C_{ID}[v_o'(nT) - v_o'(nT)] + C_{1D}v_o'[(n - 1)T] = C_{OD}v_o'(nT) \qquad (2.6a)$$

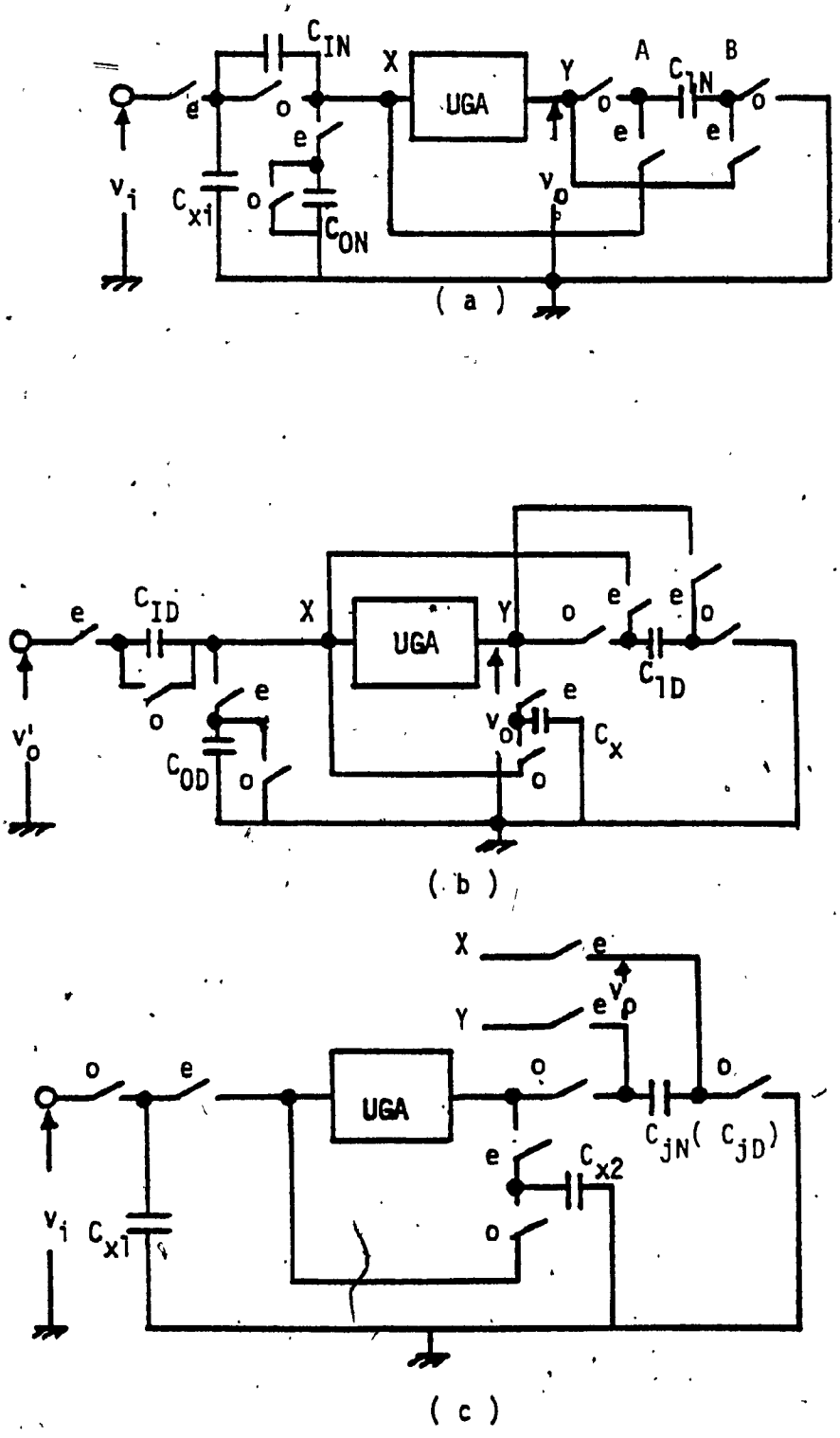


Figure 2.2: (a) Type 1 delay and add network, (b) Type 2 delay and add network, and (c) Delay network

which (on taking $\mathcal{Z}$-transform) would eventually lead to $V_0(z) = V_0'(z)/D(z)$, where

$$1/D(z) = [C_{ID} / (C_{ID} + C_{OD})] / [1 \pm z^{-1} C_{1D} / (C_{ID} + C_{OD})] \quad (2.6b)$$

The $\pm$ sign in the denominator of equation (2.6b) would depend upon the polarities of the terminals of C_{1D} connected across the input and output nodes of the UGA. The network of Fig. 2.2(b) shall be named a Type-2 Delay and Add (DA-2) network.

2.3.2 Delay Network

The delay network is shown in Fig. 2.2(c). Its function is to sample and hold an input voltage and transfer it, through a UGA, with a total delay T sec., to the capacitor C_{jN} (or C_{jD}). The terminals of C_{jN} (or C_{jD}) can be subsequently switched to the summing node of a DA-1 or DA-2 network. This would enable addition (or subtraction) of successively delayed versions of the signal voltage(s). The network of Fig. 2.2(c) shall be designated as a D-network.

2.3.3 Non-Recursive Sampled Data Filter (NR-SDTF)

The transfer function of an N^{th} order NR-SDTF has the standard form[33]

$$H(z) = \sum_{n=0}^{N-1} h(nT)z^{-n} = h(0)[1 + \frac{h(T)}{h(0)} z^{-1} + \frac{h(2T)}{h(0)} z^{-2} + \ldots] \quad (2.7)$$

An extension of equations 2.4(b)-2.5 simulates the NR-SDTF in the form

$$H(z) = \frac{C_{IN}}{C_{ON} + C_{IN}} \left[1 \pm \frac{C_{1N}}{C_{IN}} z^{-1} \pm \frac{C_{2N}}{C_{IN}} z^{-2} \pm \frac{C_{3N}}{C_{IN}} z^{-3} \pm \ldots \frac{C_{jN}}{C_{IN}} z^{-j} \pm \ldots\right] \tag{2.8}$$

Comparing (2.7) and (2.8), we have,

$$h(0) = C_{IN}/(C_{ON} + C_{IN}),\ h(jT)/h(0) = C_{jN}/C_{IN},\ j = 1,2,3\ldots$$

The schematic of a third order NR-SDTF using SC networks and UGAs is shown in Fig. 2.2(d). The schematic of any general N^{th} order NR-SDTF can be easily obtained in a similar fashion by using type DA-1 and D-networks[54].

2.3.4 Recursive Sampled Data Filter (REC-SDTF)

A REC-SDTF has a transfer function $H(z) = N(z)/D(z)$ where each $N(z)$ and $D(z)$ is a polynomial in z^{-1} having the form

$$N(z)\ [\text{or } D(z)] = \sum_{i=0}^{N-1} a_i z^{-i}$$

The polynomial $N(z)\ [\text{or } D(z)] = \sum_{i=0}^{N-1} a_{iN} z^{-i}$ can be easily generated using the scheme shown under NR-SDTF realization where one shall have

$$a_{0N} = C_{IN}/(C_{ON} + C_{IN}),\quad a_{jN} = C_{jN}/(C_{ON} + C_{IN}),\ j = 1,2,\ldots, N-1 \tag{2.9}$$

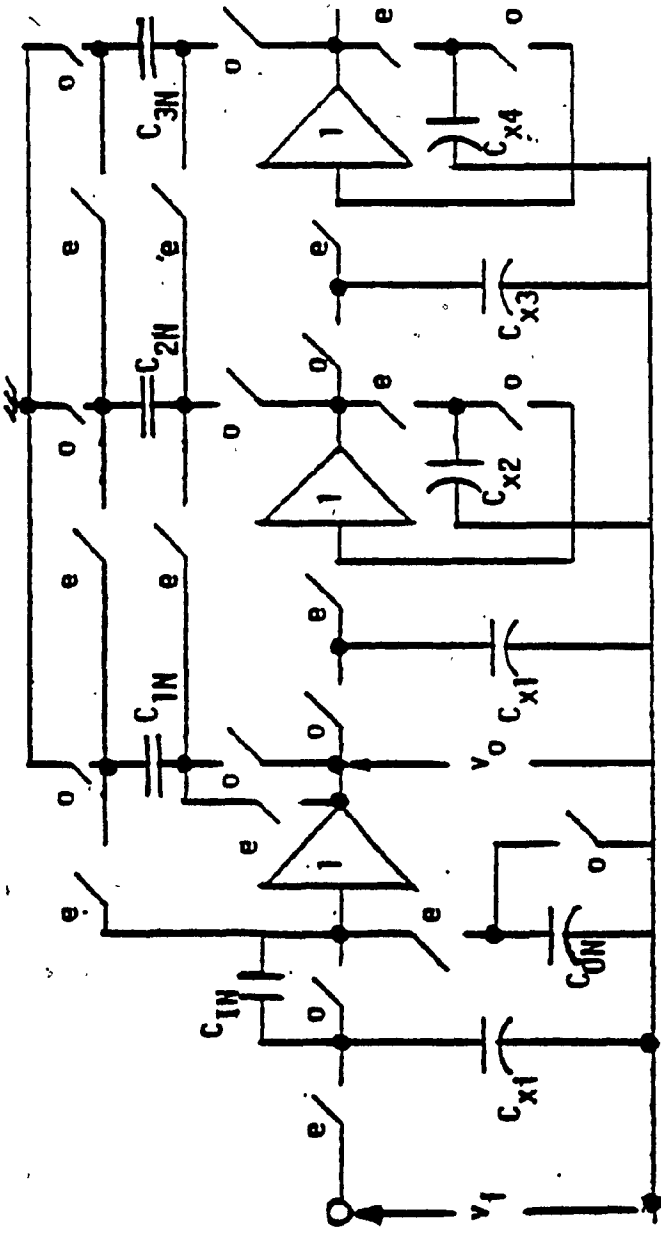


Figure 2.2: (d) A Third order Non Recursive SDTF

The subscript N has been added above to emphasize that the coefficients and the capacitors pertain to the generation of the numerator polynomial. To simulate the denominator polynomial D(z), one needs a relation like

$$V_0(z) = V_{0N}(z)/[a_{0D} + a_{1D}z^{-1} + a_{2D}z^{-2} + \ldots] \qquad (2.10)$$

where $V_{0N}(z)$ corresponds to the input and $V_0(z)$ is the output signal. This can be easily realized by an extension of the basic scheme shown in Figure 2.2(b). In this one have [ref. eqn. 2.6(b)]

$$\frac{1}{D(z)} = \frac{V_0(z)}{V_{0N}(z)} = \frac{C_{ID}}{C_{0D} + C_{ID} \pm C_{1D}z^{-1}}$$ which leads to the form

$D(z) = a_{0D} \pm a_{1D}z^{-1}$ where

$$a_{0D} = (C_{0D} + C_{ID})/C_{ID}\ , \quad \text{and } a_{1D} = C_{1D}/C_{ID} \qquad (2.11)$$

An extension of the above scheme would thus generate D(z) in the form

$$1/D(z) = 1/[a_{0D} + a_{1D}z^{-1} + a_{2D}z^{-2} + \ldots]$$

where $a_{jD} = C_{jD}/C_{iD}$, $j = 1,2,\ldots N-1$.

If now $V_{0N}(z)$ corresponds to the output of an NR-SDTF section, one would realize the REC-SDTF as

$$H(z) = \frac{V_0(z)}{V_i(z)} = \frac{V_0(z)}{V_{0N}(z)} \frac{V_{0N}(z)}{V_i(z)} = \left[\frac{1}{D(z)}\right] [N(z)] \qquad (2.12)$$

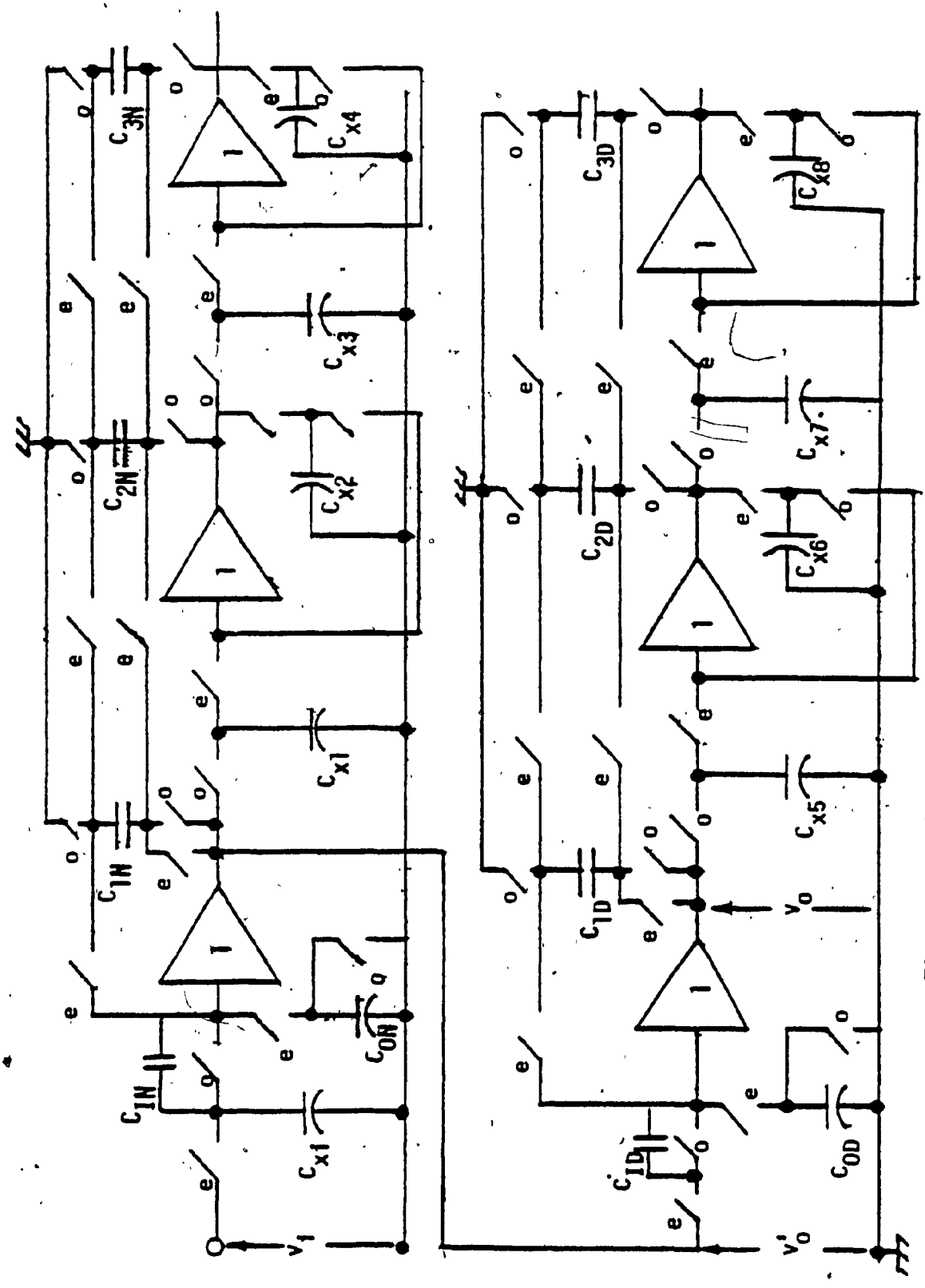


Figure 2.2: (e) A Third order Recursive SDTF

The schematic of a third order REC-SDTF is shown in figure 2.2(e). Any higher order REC-SDTF can be easily realized using DA-1, DA-2 and D networks.

2.4 REALIZATION OF BIQUADRATIC SDTF (BIQ-SDTF)

Biquadratic functions are an important class of filters. A large number of filtering tasks can be accomplished directly by them. Further, they can serve as useful building blocks for the design of higher order filters. Consequently, it is desirable to investigate the possibilities of their realization. A recursive BIQ-SDTF can be synthesized using the above principles. This shall have the transfer function

$$H(z) = h_D \left[1 + a_{1N}z^{-1} + a_{2N}z^{-2}\right] / \left[1 - a_{1D}z^{-1} + a_{2D}z^{-2}\right] \quad (2.13)$$

where

$$a_{1N} = C_{1N}/C_{IN},\quad a_{2N} = C_{2N}/C_{IN},\quad a_{1D} = C_{1D}/(C_{OD} + C_{ID})$$

$$a_{2D} = C_{2D}/(C_{OD} + C_{ID}) \quad \text{and}$$

$$h_D = 1/[(1 + C_{ON}/C_{IN})\ (1 + C_{OD}/C_{ID})].$$

The coefficients a_{1N}, a_{1D} ... etc., can be related to the parameters of the analog filters provided the s↔z mapping is specified. The properties of the BIQ-SDTF are discussed in detail in the next chapter. A practical design procedure is also presented in the same chapter.

2.5 REALIZATION OF LINEAR PHASE NR-SDTF

2.5.1 Constant Delay Filters[33]

Constant delay or linear phase filters are used in a variety of applications[34]. They can conveniently be realized as NR-SDTFs. In a linear phase NR-SDTF, the phase function $\theta(\omega)$ is a linear function of the sampled data angular frequency ω e.g., $\theta(\omega) = -\tau\omega$. Since in this case the phase delay and group delay are given, respectively, by $\tau_p = -\theta/\omega$ and $\tau_g = -d\theta(\omega)/d\omega$, each of them is a constant parameter. Recalling that the general NR-SDTF is given by: $H(z) = \sum_{n=0}^{N-1} h(nT)z^{-n}$, one has the frequency response (letting $z = \exp(j\omega T)$, where T is the sampling frequency):

$$H(e^{j\omega T}) = M(\omega)e^{j\theta(\omega)} = \sum_{n=0}^{N-1} h(nT)e^{-j\omega nT} \qquad (2.14)$$

where $M(\omega) = |\, H(e^{j\omega T})\,|$, $\theta(\omega) = \arg[H(e^{j\omega T})]$. For constant phase delay as well as constant group delay, we have,

$$\theta(\omega) = -\tau\omega = \tan^{-1} \frac{-\sum_{0}^{N-1} h(nT) \sin \omega nT}{\sum_{0}^{N-1} h(nT) \cos \omega nT} \qquad (2.15)$$

Eqn. 2.15 gives

$$\sum_{n=0}^{N-1} h(nT) \{\cos \omega nT \sin \omega\tau - \sin \omega nT \cos \omega\tau\} = 0$$

or

$$\sum_{0}^{N-1} h(nT) \sin(\omega\tau - \omega nT) = 0 \tag{2.16}$$

The solution of this equation can be shown to be

$$\tau = \frac{(N-1)T}{2} \tag{2.17a}$$

$$h(nT) = h([N-1-n)T] \text{ for } 0 \leq n \leq N-1 \tag{2.17b}$$

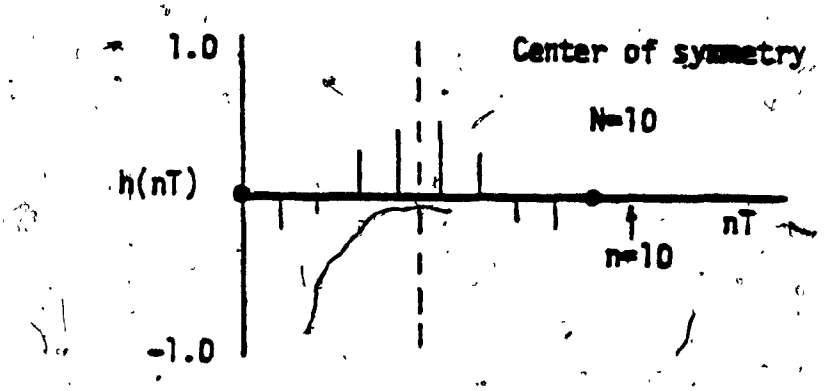
Thus, a NR-SDTF, unlike a REC-SDTF, can have constant phase and group delays over the entire baseband. It is only necessary for the impulse response to be symmetrical about the midpoint between samples (N-2)/2 and N/2 for even N of about sample (N-1)/2 for odd N. The required symmetry is illustrated in Fig. 2.3(a)-(b) for N=10 and N=11.

In many applications only the group delay τ_g need be constant, in which case one can have $\theta(\omega) = \theta_o - \tau\omega$, where θ_o is a constant. Proceeding as above, a second class of NR-SDTF, which has constant group delay, can be obtained, choosing $\theta_o = \pm \pi/2$, the solution is

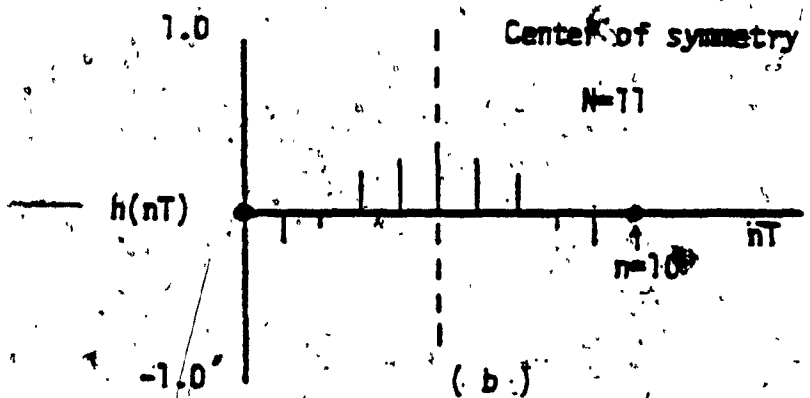
$$\tau = \frac{(N-1)T}{2} \tag{2.18a}$$

$$h(nT) = -h[(N-1-n)T] \tag{2.18b}$$

In this case, the impulse response is antisymmetric about the midpoint between samples (N-2)/2 and N/2 for even N or about sample (N-1)/2 for

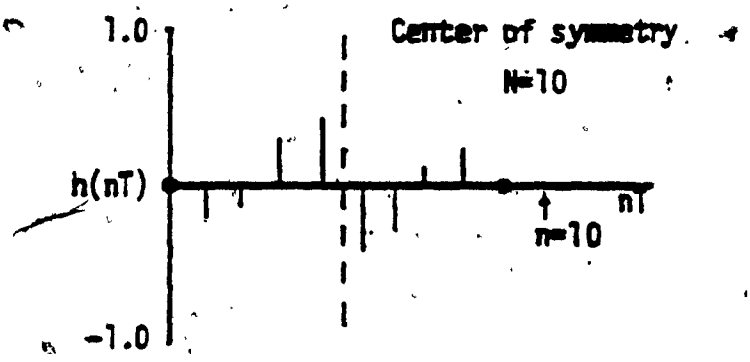


(a)

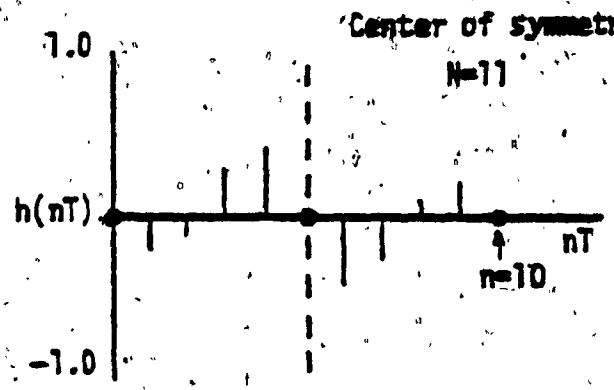


(b)

Figure 2.3: Impulse response for linear phase filters (a) even N, (b) odd N



(c)



(d)

Figure 2.3: Impulse response for constant group delay filters

(c) even N, (d) odd N

odd N, as illustrated in Figs. 2.3(c)-(d) for N=10 and N=11.

2.5.2 Frequency response

Equations 2.17(b) and 2.18(b) lead to simple expressions for the frequency response of the linear phase filters. For a symmetrical impulse response with N odd, eqn. 2.14 can be expressed as:

$$H(e^{j\omega T}) = \sum_{n=0}^{(N-3)/2} h(nT)e^{-j\omega nT} + h[\frac{(N-1)T}{2}]e^{-j\omega(N-1)T/2}$$

$$+ \sum_{n=(N+1)/2}^{N-1} h(nT)e^{-j\omega nT} \qquad (2.19)$$

By using eqn. 2.17 (b) and then letting N-1-n = m, m = n, the last summation in eqn. 2.19 can be expressed as

$$\sum_{n=(N+1)/2}^{N-1} h(nT)e^{-j\omega nT} = \sum_{(N+1)/2}^{N-1} h[(N-1-n)T]e^{-j\omega nT}$$

$$= \sum_{n=0}^{(N-3)/2} h(nT)e^{-j\omega(N-1-n)T} \qquad (2.20)$$

Then using eqns. 2.19, 2.20

$$H(e^{j\omega T}) = e^{-j\omega(N-1)T/2}\{h[\frac{(N-1)T}{2}] + \sum_{n=0}^{(N-3)/2} 2h(nT)\cos[\omega(\frac{N-1}{2}-n)T]\}$$

and hence, with (N-1)/2 - n = k, we have

$$H(e^{j\omega T}) = e^{-j\omega(N-1)T/2}\sum_{k=0}^{(N-1)/2} a_k \cos \omega kT \qquad (2.21)$$

where $a_o = h[\frac{(N-1)T}{2}]$ (2.22a)

$$a_k = 2h[(\frac{(N-1)}{2} - k)T] \quad (2.22b)$$

Similarly, the frequency responses for the case of symmetrical impulse response with N even and for the two antisymmetrical cases can be obtained. The expressions are summarized in Table 2.1[33].

2.6 SOME PRACTICAL CONSIDERATIONS

2.6.1 Coefficient Sensitivity of Sampled Data Filters

In section 2.3.4 we have developed a method for simulating a general Mth order REC-SDTF given by

$$H(z) = h_D[1 + \sum_{j=1}^{M} b_{jN}z^{-j}]/[1 + \sum_{k=1}^{M} b_{kD}z^{-k}] \quad (2.23a)$$

where $b_{jN} = C_{jN}/C_{IN}$, $b_{kD} = C_{kD}/(C_{ID} + C_{OD})$ (2.23b)

and $h_D = \frac{C_{IN}}{C_{IN} + C_{ON}} \frac{C_{ID}}{C_{ID} + C_{OD}}$ (2.23c)

Thus $\frac{dH(z)}{H(z)} = \frac{dh_D}{h_D} + \frac{dN(z)}{N(z)} - \frac{dD(z)}{D(z)}$ (2.24a)

where $N(z) = 1 + b_{1N}z^{-1} + b_{2N}z^{-2} + \ldots$ (2.24b)

and $D(z) = 1 + b_{1D}z^{-1} + b_{2D}z^{-2} + \ldots$ (2.24c)

Ignoring variations due to the argument z, for simplicity, one has

TABLE 2.1

FREQUENCY RESPONSE OF CONSTANT DELAY NONRECURSIVE FILTERS

h(nT)	N	$H(e^{j\omega T})$
Symmetrical	Odd	$e^{-j\omega(N-1)T/2} \sum_{k=0}^{(N-1)/2} a_k \cos \omega kT$
	Even	$e^{-j\omega(N-1)T/2} \sum_{k=0}^{N/2} a_k \sin \omega kT$
Antisymmetrical	Odd	$e^{-j[\omega(N-1)T/2-\pi/2)]} \sum_{k=1}^{(N-1)/2} b_k \cos [\omega(k - \frac{1}{2})T]$
	Even	$e^{-j[\omega(N-1)T/2-\pi/2]} \sum_{k=1}^{N/2} b_k \sin [\omega(k- \frac{1}{2})T]$
where $a_0 = h[\frac{(N-1)T}{2}]$ $a_k = 2h[(\frac{N-1}{2} - k)T]$ $b_k = 2h[(\frac{N}{2} - k)T]$		

$$\frac{dN}{N} = \sum_{i=1}^{M} \frac{b_{iN}}{N} z^{-i} \frac{db_{iN}}{b_{iN}} = \sum_{i=1}^{M} S_{b_{iN}}^{N} \frac{db_{iN}}{b_{iN}} \qquad (2.25)$$

where $S_{b_{iN}}^{N}$ is the sensitivity of N(z) with respect to b_{iN}.
In eqn. 2.25 $S_{b_{iN}}^{N}$ is a complex number and is controlled by the filter specifications. The quantity b_{iN} is a capacitance ratio and $[db_{iN}/b_{iN}]$ is the accuracy with which a given capacitance ratio can be maintained. In MOS technology db_{iN}/b_{iN} typically ranges from 0.1 percent to 1 per cent depending upon the actual size of the capacitors. Clearly, then dN/N in practice is expected to be small.

For the denominator polynomial D(z), one has similarly,

$$\frac{dD}{D} = \sum_{k=1}^{M} S_{b_{kD}}^{D} \sum_{j=1}^{2} S_{\alpha_{jk}}^{b_{kD}} \frac{d\alpha_{jk}}{\alpha_{jk}} \qquad (2.26)$$

where α_{jk} (j=1,2) includes the capacitance ratios C_{kD}/C_{ID} and C_{OD}/C_{ID} needed to realise b_{kD} according to

$$b_{kD} = \alpha_{1k}/(1 + \alpha_{2k}) \qquad (2.27)$$

Substitution in eqn. 2.26 gives

$$\sum_{j=1}^{2} S_{\alpha_{jk}}^{b_{kD}} = \frac{d\alpha_{1k}}{\alpha_{1k}} - \frac{\alpha_{2k}}{1+\alpha_{2k}} \frac{d\alpha_{2k}}{\alpha_{2k}} \qquad (2.28)$$

If α_{1k}, α_{2k}'s are of the same order of magnitude, one can set $\frac{d\alpha_{1k}}{\alpha_{1k}} = \frac{d\alpha_{2k}}{\alpha_{2k}} = \frac{d\alpha}{\alpha}$, which is very well achieved in MOS technology.

Hence:

$$\frac{dD}{D} = \sum_{k=1}^{M} \frac{b_{kD}}{D} z^{-k} \left\{ \frac{1}{1+\alpha_{2k}} \right\} \frac{d\alpha}{\alpha} \tag{2.29}$$

One has similarly,

$$\frac{dh_D}{h_D} = \sum_{j=1}^{2} S_{\alpha_j}^{h_D} \frac{d\alpha_j}{\alpha_j}$$

where $\alpha_1 = C_{0N}/C_{IN}$ and $\alpha_2 = C_{0D}/C_{ID}$. (2.31)

Assuming again, $\frac{d\alpha_1}{\alpha_1} = \frac{d\alpha_2}{\alpha_2} = \frac{d\alpha}{\alpha}$ one has

$$\frac{dh_D}{h_D} = - \frac{\alpha_1 + \alpha_2 + 2\alpha_1\alpha_2}{(1+\alpha_1)(1+\alpha_2)} \frac{d\alpha}{\alpha} \tag{2.32}$$

Writing $b_{iN} = \alpha_{iN}$ and $b_{id} = \frac{\alpha_{id}}{1+\alpha_2}$ where α's are capacitance ratios, one has, after some manipulations,

$$\frac{dH}{H} = \left\{ \sum_{i=1}^{M} z^{-i} \left[\frac{\alpha_{iN}}{N} - \frac{1}{D} \frac{\alpha_{id}}{(1+\alpha_2)^2} \right] - (\alpha_1 + \alpha_2 + 2\alpha_1\alpha_2) h_D \right\} \frac{d\alpha}{\alpha} \tag{2.33}$$

which gives the relative change in H(z) as a function of various capacitance ratios, the specification parameters N(z), D(z), h_D and the capacitance ratio accuracy $d\alpha/\alpha$.

In practice, it is expected that $\frac{dH}{H}$ will be small. It may also be noted that for NR-SDTF, only the quantity dN/N is of interest.

2.6.2 Effect of Sample-Hold Networks

In the development of the general NR-SDTF and REC-SDTF, each delay network [Fig. 2.2(c)] is essentially a cascade of two sample-hold (S/H) circuits, providing a delay by one full clock period. The frequency domain response of each of the S/H networks is the well-known sampling function $Sa(\omega) = \sin(\omega T/2)/(\omega T/2)$[35]. Thus each S/H network shall introduce a $Sa(\omega)$ spectral shaping which will be reflected in the realized coefficients of the general SDTF (NR or REC). This effect will become substantial when the operating frequency is close to the clock frequency $f_s(=1/T)$. Also, this effect accumulates as the order of the filter increases because the signal has to be delayed by more units and hence be subjected to more number of S/H networks. Tracing the path of the signal voltage through the DA-1 and D-networks for a general N^{th} order NR-SDTF, one can find that

$$N(z) = \sum_{i=0}^{N-1} \tilde{a}_{iN} z^{-i} \quad \text{where } \tilde{a}_{ON} = C_{IN}/(C_{IN} + C_{ON}) = a_{ON} \tag{2.34a}$$

$$\text{while } \tilde{a}_{jN} = [Sa(\omega)]^{2j-1} \frac{C_{jN}}{C_{IN} + C_{ON}} = [Sa(\omega)]^{2j-1} a_{jN}, \; j=1,2,..,N-1 \tag{2.34b}$$

where a_{ON}, a_{jN} represent the nominal coefficients as arrived at in connection with eqn. 2.9. Similarly, for the N^{th} order REC-SDTF, one would have

$$1/D(z) = 1/\sum_{i=0}^{N-1} \tilde{a}_{iD} z^{-i}$$

$$\text{where } \tilde{a}_{OD} = (C_{OD} + C_{ID})/C_{ID} = a_{OD} \tag{2.35a}$$

and $$\tilde{a}_{jD} = [Sa(\omega)]^{2j-1} \frac{C_{jD}}{C_{ID}} = [Sa(\omega)]^{2j-1} a_{jD},\ j=1,2,\ldots N-1 \qquad (2.35b)$$

The quantities a_{OD}, a_{jD} represent the nominal coefficients in D(z) as arrived at earlier in eqn. 2.11.

Since $Sa(\omega)$ is frequency dependent, the effect of the perturbations in the nominal coefficients a_{ON}, a_{1N} and a_{OD}, a_{1D} ... cannot be exactly compensated over the entire frequency range of interest. However, if the frequency band of interest is known, an optimization alogorithm can be used to minimize the error between the ideal frequency response and the actual frequency response [when $Sa(\omega)$ spectral shaping is considered]. This procedure shall give the set of coefficients $\hat{a}_{ON}$, $\hat{a}_{1N}$, ... and $\hat{a}_{OD}$, $\hat{a}_{1D}$, ... which when realized using appropriate capacitance ratios (see eqns. 2.9, 2.11, for example) would produce a response which is close to the ideal response within a prescribed error limit. A theoretical basis of such an algorithm is considered next.

2.6.3 Minimization of Mean Square Error Between Ideal and Actual Frequency Responses

Let $H_D(z)$ be the desired response of an SDTF while $H(z)$ is the one actually obtained because of certain perturbations, e.g., the spectral shaping due to the sample hold circuits. The ideal and actual frequency responses are then $H_D(e^{j\omega T})$ and $H(e^{j\omega T})$ respectively [where $z = \exp(j\omega T)$]. Putting $M_d = |H_D(e^{j\omega T})|$, $M_a = |H(e^{j\omega T})|$, the normalized

mean square error in frequency response, computed at a number of discrete frequencies ω_i (i = 1, 2, ..., m) can be expressed as

$$Q(\hat{\theta}) = [(M_a - M_d) / M_d]^2 \tag{2.36a}$$

where $\hat{\theta}$ is a function of the N unknown coefficient, that is,

$$\hat{\theta} = f(\hat{h}_0, \hat{h}_1, \ldots, \hat{h}_{N-1}) \tag{2.36b}$$

and $\hat{h}_0, \hat{h}_1$ ... are the coefficients in the description of H(z). Our object is to find an optimal vector $\hat{\theta}$ and hence the optimal set of coefficients $\hat{h}_0, \hat{h}_1, \ldots, \hat{h}_{n-1}$ such that $Q(\hat{\theta})$ is minimized. Minimization of $Q(\hat{\theta})$ requires use of a nonlinear programming procedure such as the Fletcher Powel algorithm[36]. To use this algorithm, the gradient of the function being minimized must be known. Introducing a new set of variables, x_i (i=1, 2, ..., N) where $x_1 = \hat{h}_0$, $x_2 = \hat{h}_1$, ... one can obtain

$$\frac{\delta Q(\hat{\theta})}{\delta x_i} = \frac{\delta}{\delta x_i} \left[\frac{M_a - M_d}{M_d}\right]^2 \tag{2.37}$$

since M_d is independent of x_i's, one has

$$\frac{\delta Q(\hat{\theta})}{\delta x_i} = \frac{2(M_a - M_d)}{M_d^2} \frac{\delta}{\delta x_i}(M_a) \tag{2.38a}$$

while[37]

$$\frac{\delta}{\delta x_i}(M_a) = \frac{1}{M_a} \mathrm{Re}\left\{ H^*(z) \frac{\delta}{\delta x_i}[H(z)] \right\} \tag{2.38b}$$

where $M_a = |H(e^{j\omega T})| = [H(z)\, H^*(z)]^{1/2}$

From (2.38b), it can be easily shown when H(z)=N(z) (say), that

$$\frac{\delta}{\delta x_i}(M_a) = M_a \, \mathrm{Re}\left[\frac{1}{N(z)} \frac{\delta}{\delta x_i}\{N(z)\}\right] \tag{2.39}$$

Hence, from eqs. 2.26a and 2.27

$$\frac{\delta Q(\hat{\theta})}{\delta x_i} = \frac{2(M_a - M_d)}{M_d^2} M_a \quad \mathrm{Re}\left[\frac{1}{N(z)} \frac{\delta}{\delta x_i}\{ N(z) \}\right] \tag{2.40}$$

which can be readily computed on a digital computer at each of the chosen frequency ω_i (i=1, 2, ..., M). The rest of the procedure for minimizing the error is rather straightforward and can be performed using minimization algorithms[38]. Such algorithms are often available as standard subroutines (e.g. VAØ9A, VA1ØA in the scientific package library of CYBER 172 CDC computers) in modern digital computers.

2.7 EXPERIMENTAL AND NUMERICAL RESULTS

2.7.1 Recursive Sampled Data Filter

The design equations presented in Section 2.3.4 have been tested by designing a third order recursive SDTF bilinearly equivalent to a corresponding analog low pass Butterworth transfer function with f_p=1kHz and a flat gain h_A=5. The clock rate used was f_s=10 kHz and discrete capacitors (film/foil type with polysterene dielectric) with $C_{1N} = 1nF = C_{0N} = C_{1D}$ and $C_{1N} = 3nF = C_{2N}$, $C_{3N} = 1nF$, $C_{1D} = 9.7nF$, $C_{2D} = 6.6nF$, $C_{3D} = 1.533nF$, $C_{0D} = 4.52nF$. The UGAs were realized with OAs using 100% negative feedback (Fig. 2.4). The ideal response is

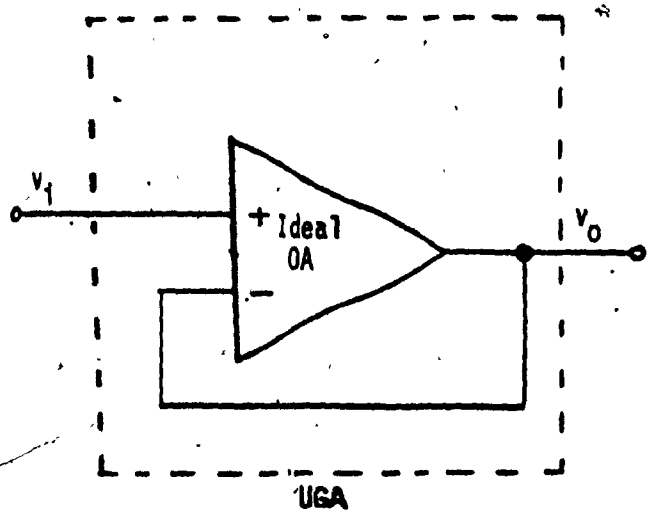


Figure 2.4: Unity Gain Amplifier for experimental work

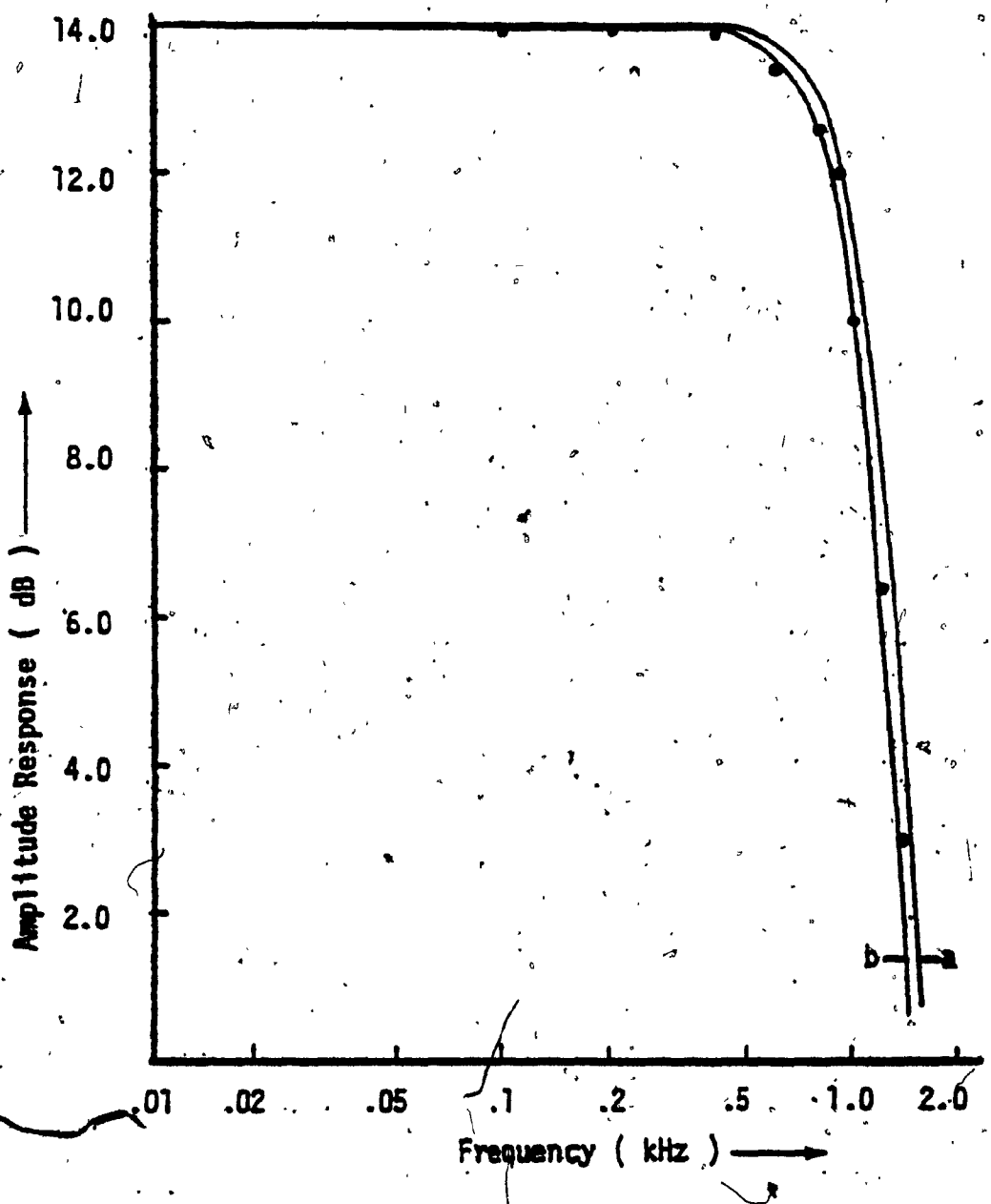


Figure 2.5: Response of third order REC SDTFs , (a) the ideal response, (b) response with the sample hold effect included.

shown in Fig. 2.5(a) while the theoretical response considering the effects of the sample hold networks (refer section 2.6.2) is shown in Fig. 2.5(b). In the experimental circuit no optimization was used to compensate for the effect of the spectral shaping due to the sample hold networks. The experimental results (• •) follow closely the theoretical curve [Fig. 2.5(b)] which is expected.

2.7.2 Non Recursive Sampled Data Filter

The ideas presented in section 2.3.3 have been tested in the laboratory by designing first, second, third, fourth and fifth order NR-SDTFs with $C_{IN} = C_{ON} = 10nF$, $C_{1N} = C_{2N} = \ldots = C_{5N} = 10nF$. The UGAs were realized with uA 741 operational amplifiers using 100% negative feedback (Fig. 2.4). The capacitors were film/foil type with polysterene as dielectric. The switches were CMOS analog switches (RCA 4066B). The clock rate used was 10 kHz (T=0.1 msec). The frequency response characteristics for the third and fifth order filters are shown in Figs. 2.6(a) and (c). The theoretical responses, accounting for the spectral shapings due to the sample and hold circuits (refer section 2.6.2) are shown in Figures 2.6(b) and (d). The experimental results (o o and + +) agree very closely with the theoretical curves 2.6(b) and (d).

2.7.3 Constant Delay NR-SDTF

The design of constant delay NR-SDTF described in Section 2.5.1 was tested for a ninth order NR-SDTF in the laboratory using discrete

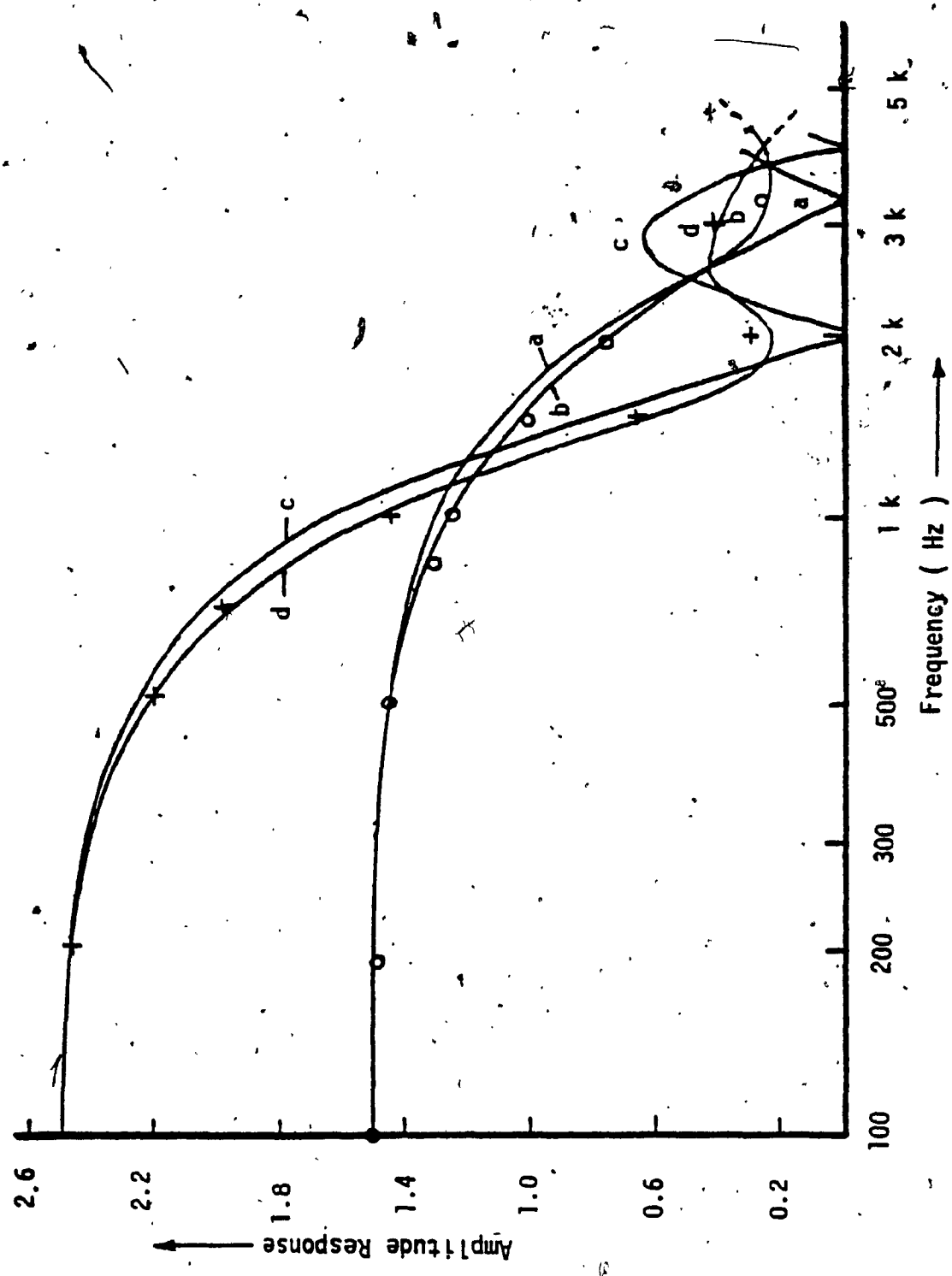


Figure 2.6: Responses of Third and Fifth order NR SDTFs, (a) and (c) ideal case , (b) and (d) with the sample hold effect included, respectively.

capacitors, UGAs (realized from μA 741 OAs) and CMOS switches (RCA type 4066B). The capacitances were chosen so that (with $C_{ON} = C_{IN} = 10$ nF). $h_0 = h_o = h_8 = 1/20$, $h_1 = h_7 = 2.2/20$, $h_2 = h_6 = 3.3/20$, $h_3 = h_5 = 4.7/20$ and $h_4 = 10/20$. The theoretical response with the $Sa(\omega)$ spectral shaping included, is shown by the solid line in Fig. 2.7(b). The experimental points (o o) follow, very closely, the theoretical response. The nominal response (ignoring the $Sa(\omega)$ spectral shaping) is shown by curve (a) in Fig. 2.7. Comparison of Figs. 2.7(a) and (b) reveals that the effect of the sample and hold circuits becomes more noticeable at signal frequencies $\geq f_s/4$. The error minimization procedure, described in section 2.6.3, was employed to arrive at the optimal set of capacitor ratios ($h_0 = 0$, $h_1 = .257$, $h_2 = 0$ $h_3 = .358$, $h_4 = .502$, $h_5 = .353$ $h_6 = 0$, $h_7 = .129$, $h_8 = .04$). The response with corresponding set of capacitors (with $C_{IN} = C_{ON} = 10$ nF) agree with the nominal response [fig. 2.7(a)] within an rms error of less that 3%. The experimental points (+ +) with this optimal set of capacitors shows very good agreement with the nominal response.

2.8 CONCLUSION

A systematic approach for realizing sampled data filter functions is proposed in this chapter. The realization uses the basic building blocks DA-1, DA-2 and D-networks, realized from UGAs and SCs. Realizations of both NR-SDTF and REC-SDTF, of any order, have been illustrated. Realization of an important class of NR-SDTF, viz., constant delay filters, has also been considered. Some practical considerations, namely, the sensitivity of the desired response to

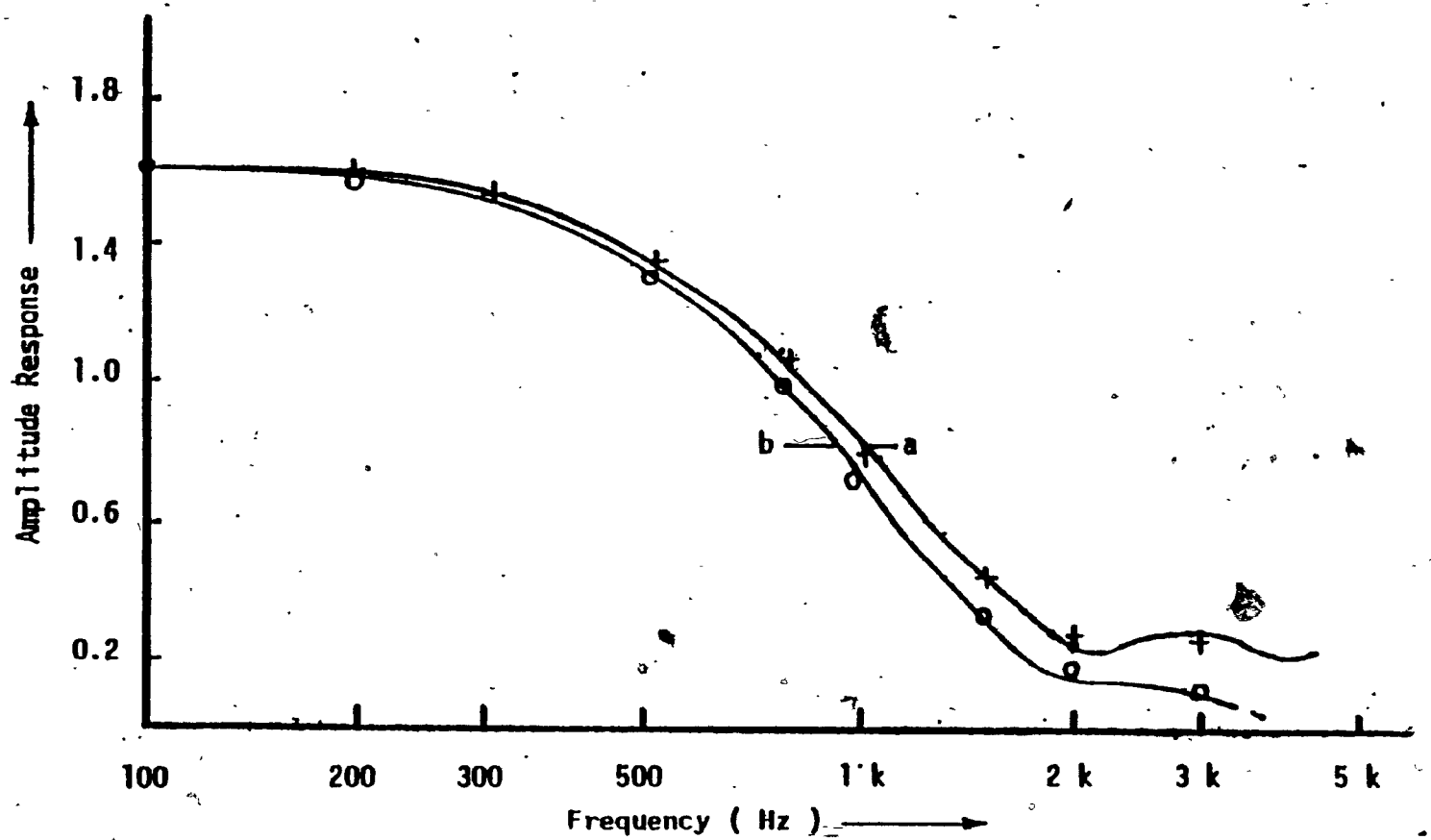


Figure 2.7: Responses of ninth order constant delay NR SDTFs, (a) ideal , (b) with sample hold effect included.

capacitance ratio errors and the effect of spectral shaping due to the sample and hold circuits on the desired response, have been discussed. The theoretical basis of an optimization algorithm to minimize the error between the desired and the realized responses due to the spectral shaping of sample and hold circuits, has been discussed. Numerical simulations as well as experimental results reveal that substantial minimization of error can be achieved by using the indicated optimization procedures. Experimental results carried out on a number of NR-SDTFs show very good agreement with the theoretical results. The topology for a general BIQ-SDTF has been presented. Since biquadratic filters can accomplish a number of important filtering functions and also serve as important building blocks in realizing high order filters, it is of importance to investigate in detail, the characteristics of BIQ-SDTFs. Investigations on BIQ-SDTFs, realized using the basic building blocks introduced in this chapter, are continued in the following chapter.

CHAPTER THREE

BIQUADRATIC SAMPLED DATA FILTER REALIZATION

3.1 INTRODUCTION

A set of SC building blocks has been introduced in Chapter 2. Using these building blocks, schemes have been developed for realizing any SDTF, recursive or non recursive, and of any order. The realization of a BIQ-SDTF, however, has been only briefly discussed in the previous chapter. In this chapter, the case of the BIQ-SDTF is considered in detail. Towards this end, attention is restricted to the class of BIQ-SDTFs that simulate the popular analog biquadratic filters (low pass, high pass, band pass, notch) under the well-known bilinear $s \leftrightarrow z$ transformation. The bilinear transformation is chosen since it offers the possibility of simulating the amplitude response of analog filters with critical frequencies closest to the Nyquist frequency. Various practical aspects, such as guaranteeing low sensitivity of the realizations, minimization of the total capacitance in the circuits, effect of the sample hold capacitors, effect of the stray and parasitic capacitances etc., are examined. Finally, a step-by-step design procedure, easily implemented in a computer, is given. This procedure, starting from the given analog filter specification, yields an SDTF that (i) is bilinearly equivalent to the given analog filter, (ii) has a very low sensitivity to the variations of capacitance ratios, (iii) uses minimum total capacitance and (iv) is tolerant of the various parasitic capacitances in the circuit. Experimental results are given

and these agree very well with the theoretical predictions.

3.2 THE BIQUADRATIC SAMPLED DATA FILTERS

The BIQ-SDTF derived in section 4 of Chapter 2 is shown in Fig. 3.1 here. This network has a transfer function given by eqn. 2.13 which is repeated here for convenience:

$$H(z) = h_D \, (1 + a_{1N} z^{-1} + a_{2N} z^{-2}) \; / \; (1 - a_{1D} z^{-1} + a_{2D} z^{-2}) \qquad (3.1)$$

where $h_D = [(1 + C_{ON}/C_{IN})\,(1 + C_{OD}/C_{ID})]^{-1}$, $a_{1N} = C_{1N}/C_{IN}$,

$a_{2N} = C_{2N}/C_{IN}$, $a_{1D} = C_{1D} \; / \; (C_{OD} + C_{ID})$

and $a_{2D} = C_{2D} \; / \; (C_{OD} + C_{ID})$.

The coefficients a_{1N}, a_{1D}, a_{2N}, a_{2D}, h_D can be related to the parameters of the corresponding analog biquadratic transfer functions provided the $s \leftrightarrow z$ mapping is specified. Assuming the well-known bilinear transformation $s = \frac{2}{T} \; \frac{1-z^{-1}}{1+z^{-1}}$, the various design formulae are shown in Table 3.1. For compactness, the following substitutions have been used:

$$a = 2/T, \; \tilde{\omega}_p = a \tan (\omega_p/a) \; , \; \tilde{\omega}_n = a \tan (\omega_n/a) \qquad (3.2a)$$

$$F_1 = s^2 + (\omega_p/Q_p)\, s + \omega_p^2 \; , \; F_2 = a^2 + (\tilde{\omega}_p/Q_p)\, a + \tilde{\omega}_p^2 \qquad (3.2b)$$

$$a_{1D} = 2(a^2 - \tilde{\omega}_p^2) \; / F_2 \; , \; a_{2D} = [a^2 - (\tilde{\omega}_p/Q_p)\, a + \tilde{\omega}_p^2] \; / \; F_2 \qquad (3.2c)$$

where ω_p, Q_p are the pole frequency and pole Q of the analog filter and $\tilde{\omega}_p$, $\tilde{\omega}_n$ (for notch filter) are the corresponding prewarped frequencies.

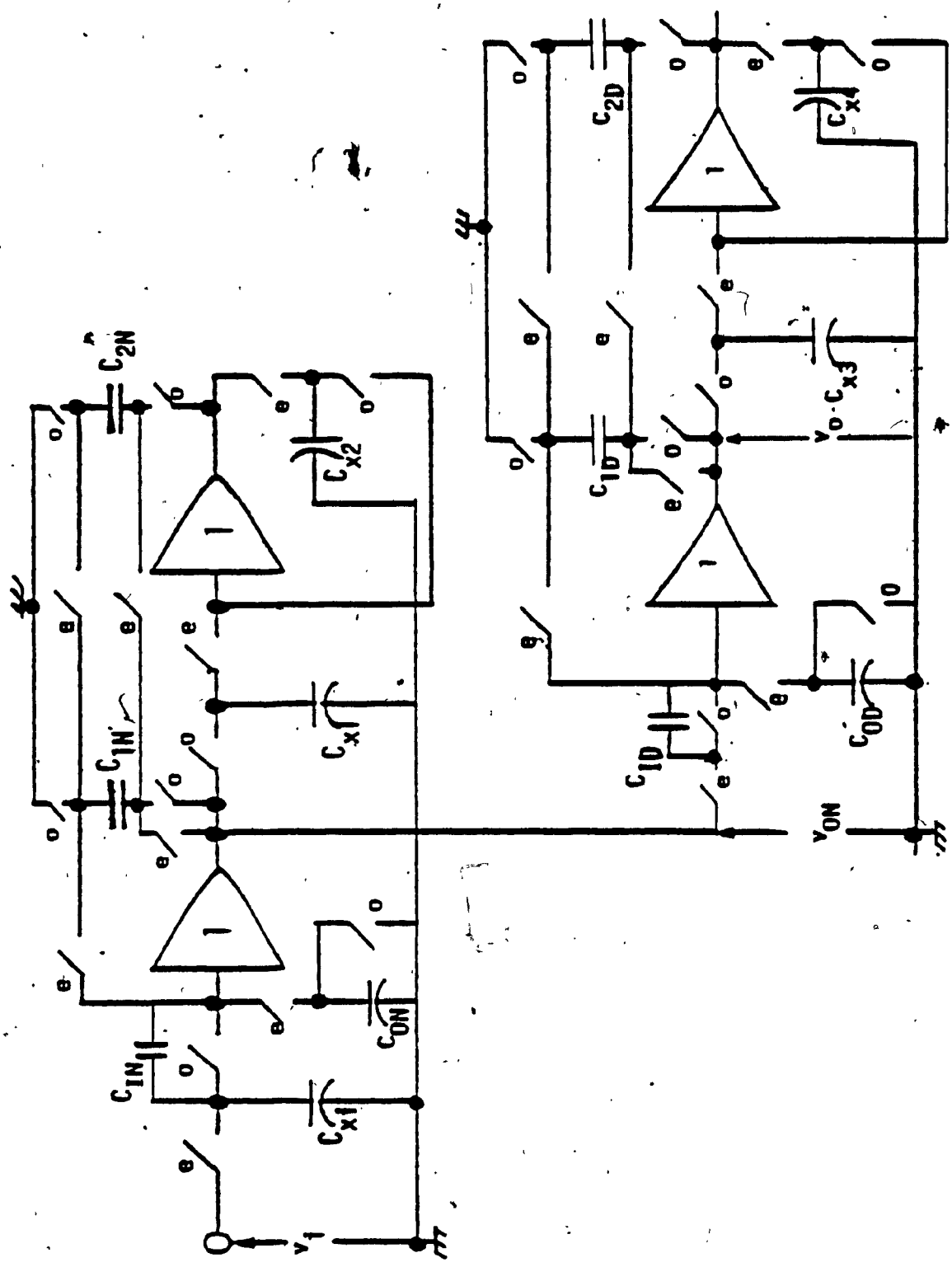


Figure 3.1: Schematic of a UGA based Biquadratic SDTF

TABLE 3.1

DESIGN COEFFICIENTS OF BIQ SDTF BILINEARLY EQUIVALENT TO THE ANALOG BIQUADRATIC FILTERS

Filter Type	Analog Transfer Function	Sampled-Data Transfer Function Coefficients* $H(z)=h_D\,(1+a_{1N}z^{-1}+a_{2N}z^{-2})/[1-a_{1D}z^{-1}+a_{2D}z^{-2}]$		
		h_D	a_{1N}	a_{2N}
LPF	$H_{LP}\,\omega_p^2/F_1$	$H_{LP}\,\tilde{\omega}_p^2/F_2$	2	1
HPF	$H_{HP}\,s^2/F_1$	$H_{HP}\,a^2/F_2$	-2	1
BPF	$H_{BP}(\omega_p/Q_p)s/F_1$	$H_{BP}(\tilde{\omega}_p/Q_p)a/F_2$	0	-1
APF	$H_{AP}\,\frac{F_1-2(\omega_p/Q_p)s}{F_1}$	$H_{AP}\,a_{2D}$	$-a_{1D}/a_{2D}$	$1/a_{2D}$
NOTCH	$H_N\,(s^2+\omega_n^2)/F_1$	$H_N\,(a^2+\tilde{\omega}_n^2)/F_2$	$-\frac{2(a^2-\tilde{\omega}_n^2)}{a^2+\tilde{\omega}_n^2}$	1

* The coefficients a_{1D}, a_{2D} have already been shown in eqn. 3.2(c) in the text.

3.3 SOME PRACTICAL CONSIDERATIONS

3.3.1 ω_p and Q_p Sensitivities

For a BIQ-SDTF, bilinearly eqivalent to an analog filter, the normalized (with respect to $2/T = 2f_s$) pole frequency (ω_p) and pole $Q(Q_p)$ are:

$$\Omega_p = \sqrt{[(1 - a_{1D} + a_{2D}) / (1 + a_{1D} + a_{2D})]} \tag{3.3}$$

and

$$Q_p = \sqrt{[(1 - a_{1D} + a_{2D})(1 + a_{1D} + a_{2D})]} / [2(1 - a_{2D})] \tag{3.4}$$

writing $\alpha_1 = C_{1D}/C_{ID}$, $\alpha_2 = C_{2D}/C_{ID}$, $\alpha_3 = C_{OD}/C_{ID}$, one has

$$a_{1D} = \alpha_1/(1 + \alpha_3),\ \alpha_{2D} = \alpha_2/(1 + \alpha_3) \tag{3.5}$$

At the present state of MOS technology, it is reasonable to assume that the capacitance ratio accuracy is uniform if the spreads are not very large, so that one can write:

$$\frac{d\alpha_1}{\alpha_1} = \frac{d\alpha_2}{\alpha_2} = \frac{d\alpha_3}{\alpha_3} = \frac{d\alpha}{\alpha}$$

After some algebraic manipulations, one arrives at:

$$\frac{d\Omega_p}{\Omega_p} = -\frac{\Omega_p}{8\, Q_p \Omega_p^2}\left[Q_p(1 - \Omega_p^4) + \Omega_p(1 - \Omega_p^2)\right]\frac{d\alpha}{\alpha} \tag{3.6}$$

Similarly, one can obtain

$$\frac{dQ_p}{Q_p} = -\frac{\Omega_p}{4\,Q_p^2}\left[Q_p(3-\Omega_p^2) - \Omega_p\right]\frac{d\alpha}{\alpha} \tag{3.7}$$

In MOS technology $\left|\frac{d\alpha}{\alpha}\right|$ is quite small (.1% to 1%) so that a very low sensitivity operation can be easily obtained if one can maintain

$$-1 < \frac{1}{8\,Q_p\Omega_p^2}\left[Q_p(1-\Omega_p^4) + \Omega_p(1-\Omega_p^2)\right] < 1 \tag{3.8}$$

and

$$-1 < \frac{\Omega_p}{4\,Q_p^2}\left[Q_p(3-\Omega_p^2) - \Omega_p\right] < 1 \tag{3.9}$$

Let $\phi(Q_p,\Omega_p) = Q_p(3-\Omega_p^2) - \Omega_p$ in eqn. (3.9). Then at $\Omega_p = 0$, $\phi(Q_p,\Omega_p) = 3\,Q_p$ and it can be shown that $\phi(Q_p,\Omega_p)$ is monotonically decreasing function of Ω_p with a zero at $\Omega_p \sim \sqrt{3}(1 + 1/24\,Q_p^2 - 1/\sqrt{12}Q_p) \sim \sqrt{3}$ for $12\,Q_p^2 \gg 1$. Hence, for $12\,Q_p^2 \gg 1$, $\phi(Q_p,\Omega_p) > 0$ in the range $0 < \Omega_p < \sqrt{3}$. In such a case the inequality in eqn. (3.9) reduces to the requirement:

$$\phi(Q_p,\Omega_p) = 4\,Q_p^2 - \Omega_p Q_p(3-\Omega_p^2) + \Omega_p^2 > 0 \tag{3.10}$$

This function $\psi(Q_p,\Omega_p)$ has a minimum value of $\psi_{min} = \Omega_p^2[1 - (3-\Omega_p^2)^2/16]$ at $Q_p = Q_c = \Omega_p(3-\Omega_p^2)/8$. The ψ_{min} is always positive in the range $0 < \Omega_p < \sqrt{3}$, so that $\psi(Q_p,\Omega_p) > 0$ should always be satisfied in the range $0 < \Omega_p < \sqrt{3}$. The range $\Omega_p > \sqrt{3}$ is discarded since in that case one would arrive at $f_s/f_p < 2$ which is not permissible by virtue of sampling theorem. Depending upon whether Ω_p

is <1 or >1, the first inequality leads to two lower bounds on $Q_p(Q_{\ell_1}, Q_{\ell_2})$ as (writing $\beta = f_s/f_p$)

$$Q_p > Q_{\ell_1} = \pi\beta(\beta^2 - \pi^2) \,/\, (8\pi^2\beta^2 - \beta^4 + \pi^4),\ \beta = \frac{f_s}{f_p} > \pi \qquad (3.11)$$

and

$$Q_p > Q_{\ell_2} = -\pi\beta(\pi^2 - \beta^2) \,/\, (8\pi^2\beta^2 + \beta^4 - \pi^4),\ \beta = \frac{f_s}{f_p} < \pi \qquad (3.12)$$

The quantity $8\pi^2\beta^2 + \beta^4 - \pi^4$ is positive in the range $2<\beta<\pi$, making Q_{ℓ_2} negative over this range. Hence the inequality in eqn. (3.12) is always satisfied in practice. With regard to eqn. (3.11), the quantity $8\pi^2\beta^2 - \beta^4 + \pi^4$ is positive in the range $\pi<\beta<\beta_c$, zero at $\beta_c = 2\pi[1 + \frac{1}{4}\sqrt{17}\,]^{1/2} \approx 9$ and negative for $\beta>\beta_c$. Hence, care has to be exercised in selecting a β (that is f_s) only in the range $\pi<\beta<\beta_c$ so that the design Q_p is $> Q_{\ell_1}$.

Thus, finally, for $2<f_s/f_p<\pi$ and $f_s/f_p>9$, the only requirement is that $12\,Q_p^2 \gg 1$. For the range $\pi<f_s/f_p<9$, Q_p has to be such that $Q_p>Q_{\ell_1}$ in addition to being $12\,Q_p^2 \gg 1$.

3.3.2 Effect of Sample Hold Capacitors

Each of the capacitors C_{xi}, C_{x1},... modifies the input signal by the sample-hold (SH) function:

$$H_{SH}(j\omega) = [\sin(\omega T/2)/(\omega T/2)]\ \exp[-j\omega T/2] \qquad (3.13)$$

As noted in Chapter 2, the effect of this spectral shaping will be to modify the coefficients a_{1N}, a_{2N}, a_{1D}, a_{2D} of the delay terms z^{-i} ($i=1,2$) over the entire frequency band. One will thus have $a_{jN} \rightarrow \tilde{a}_{jN} = [Sa(\omega)]^{2j-1} a_{jN}$ and $a_{jD} \rightarrow \tilde{a}_{jD} = [Sa(\omega)]^{2j-1} a_{jD}$, $j=1,2$ and $Sa(\omega) = Sin(\omega T/2)/(\omega T/2)$. A general approach to take these perturbations into account will be to predistort the h_D, a_{iN}s, a_{iD}s through an optimization routine to yield the coefficients $\hat{H}$, H_is and D_is so that the frequency response of the BIQ-SDTF (with $\hat{H}$, N_i, D_i as parameters) matches with the analog counterpart within a prescribed error limit (say 5% rms) over the frequency band of interest. Such a technique has already been employed to compensate for the spectral shaping due to $Sa(\omega)$ in some filter designs [39].

3.3.3 Minimum Capacitance Design

In MOS technology, designs that minimize the total capacitance are very attractive. Once the number of capacitors is fixed by the chosen topology, one then has to minimize the spreads amongst the various capcitors. In the following, a scheme is suggested which would minimize the sum of the design capacitors C_{IN}, D_{ID}, ... C_{2N}, C_{2D} in a BIQ-SDTF. The C_xs are ignored for the time being since they can be chosen large enough as long as they give the required SH operation. The eight capcitors in a BIQ-SDTF are constrained by the five design parameters $\hat{H}$, N_1, N_2, D_1, D_2 which are the numerical values obtained after

predistortion of the SDTF coefficients [$h_D, a_{1N}, a_{2N}, a_{1D}, a_{2D}$ (refer Table 3.1)] to accommodate the effect of the spectral shaping by the SH circuits. Thus, three capacitors can be chosen as equal, leaving the other five capacitors to take care of the five constraints as below:

$$\hat{H} = [(1 + C_{ON}/C_{IN})(1 + C_{OD}/C_{ID})]^{-1} \qquad (3.14a)$$

$$N_1 = C_{1N}/C_{IN} \quad , \quad N_2 = C_{2N}/C_{IN} \qquad (3.14b)$$

$$D_1 = C_{1D}/(C_{ID} + C_{OD}) \quad , \quad D_2 = C_{2D}/(C_{ID} + C_{OD}) \qquad (3.14c)$$

Now, assuming a minimum unit capacitance C_u and assigning the number $x_1, x_2, \ldots$ as the ratio of the actual capacitors to the unit capacitance, one can obtain the sum [with $b = \hat{H}/(1-\hat{H})$] of the capacitances given by:

$$\sum_{i=1}^{8} C_u x_i = \left[\frac{bx_2(x_5+x_6)}{x_5 - bx_6}(1+N_1+N_2) + (1+D_1+D_2)(x_5+x_6) + x_2\right]C_u \qquad (3.15)$$

where, we have set:

$$C_{IN} = x_1 C_u \ , \ C_{ON} = x_2 C_u \ , \ C_{1N} = x_3 C_u \ , \ C_{2N} = x_4 C_u, \text{ and}$$

$$C_{ID} = x_5 C_u \ , \ C_{OD} = x_6 C_u \ , \ C_{1D} = x_7 C_u \ , \ C_{2D} = x_8 C_u$$

One can then put $x_2 = x_5 = x_6 = x$, giving the minimum sum of the capacitances as:

$$\left[\frac{2b}{1-b}(1 + N_1 + N_2) + 2(1 + D_1 + D_2) + 1\right] \times C_u \qquad (3.16)$$

and the various capacitors as:

$$C_{ON} = C_{ID} = C_{OD} = x\, C_u$$

$$C_{IN} = \frac{2b}{1-b} x\, C_u,\quad C_{1N} = N_1 C_{IN},\quad C_{2N} = N_2\, C_{IN} \tag{3.17}$$

$$C_{1D} = 2D_1 \times C_u\ ,\quad C_{2D} = 2D_2 \times C_u$$

The above scheme shall be called scheme I for minimum capacitance design. It must be apparent from the above that since all the capacitors have a positive value, one must keep $b < 1$ and $b > 0$, requiring $\hat{H} < \frac{1}{2}$. This is easily achieved in practice by scaling down (if permitted) the gain of the analog filter. If, however, this is not possible, one can arrive at a sub-optimum minimum by choosing only two capacitors of equal value. Thus one can set $x_2 = x_6$, and $x_5 = \lambda x$ where λ is chosen to minimize the sum:

$$S_c = \left[\frac{(1+N_1+N_2)\ (1+\lambda)b}{\lambda - b} + (1+D_1+D_2)\ (1+\lambda)\right] \times C_u \tag{3.18}$$

Ignoring the trivial solution $S_c = 0$ for $x = 0$, one can get the optimum [by setting $\frac{\delta}{\delta\lambda}(S_c) = 0$] as:

$$\lambda_0 = b \pm \sqrt{\frac{b(b+1)\ (1+N_1+N_2)}{1+D_1+D_2}} \tag{3.19}$$

Again, one needs $\lambda_0 > 0$ and $b/(\lambda_0 - b) > 0$ for all the capacitors to be positive. These two inequalities are satisfied if $\lambda_0 > b$ and $b > 0$. The condition $b > 0$ needs $\hat{H} < 1$ while the first condition can be easily achieved by taking:

$$\lambda_0 = b + \sqrt{\frac{b(b+1)\ (1+N_1+N_2)}{1+D_1+D_2}} \qquad (3.20)$$

The set of capacitances corresponding to this optimum choice shall be:

$$C_{ON} = C_{OD} = x\ C_u\ ,\ C_{ID} = \lambda_0 \times C_u\ ,\ C_{IN} = b(1+\lambda_0) \times C_u/(\lambda_0 - b),$$

$$C_{1N} = N_1\ C_{1N}\ ,\ C_{2N} = N_2\ C_{IN}\ ,\ C_{1D} = D_1(1+\lambda_0) \times C_u\ ,$$

$$C_{2D} = D_2(1+\lambda_0) \times C_u$$

This shall be referred to as scheme II of minimum total capacitance design.

3.3.4 Considerations Regarding Parasitic Capacitances

Considerations regarding parasitic capacitances are important in deciding about suitable values for the SH capacitors and the unit capacitance C_u as discussed under the capacitance minimization schemes above. Further, it is important to investigate the effects of the parasitics on the frequency repsonse characteristics of the BIQ-SDTF.

In the circuit topology proposed, the most important parasitic components arise out of the two series capacitances C_{ID} and C_{IN}. For other capacitances, the bottom plates could be grounded (or switched to ground or to the output of an UGA) thereby eliminating the effect of the major part (which amounts to 20% of the respective nominal capacitance values) of the parasitic capacitances. For C_{IN} and C_{ID}, the bottom plates should be oriented towards the voltage source (or the output of the UGA), thereby reducing the effect of the parasitics. Further, a special switching arrangement can be made to ground both plates of C_{IN} and C_{ID} during alternate switching phases. For the capacitors C_{1N}, C_{1D}, etc., the bottom plate should be so oriented that they are connected to the output of the respective UGA (which works like a voltage source) while discharging these capacitors at the summing junction. With all these, however, the parasitics associated with the top plate of the capacitors due to the switches and the input of the UGAs remain to be considered. Nothing much can be done to eliminate all these parasitics, but a judicious choice of C_u and C_xs would make the effects of the parasitics relatively insignificant on the frequency response of the filter. **The resulting design may be called a parasitic tolerant design.** With the present day MOS technological processes, the stray capacitance from each terminal of a switch to ground would be about 20 fF (fF = 10^{-15} Farad) or less while the parasitic at the input of a UGA would be of the same order of

magnitude or slightly higher (say, about 40 fF). Further, the parasitics at the top plates of the capacitors, due to wiring and interconnections would be 0.1% (or less) of the nominal capacitance values. The DA-1, DA-2 and D-networks including all the important parasitics are re-drawn in Figures 3.2(a)-(c). To keep the diagrams tidy, all the parasitics have been lumped together and shown as CP_is ($i = 1,2, \ldots$). Letting PCT_y as the parasitic at the top plate of the capacitor C_y due to interconnections and PS_w as the stray capacitance from either terminal of the switch S_w to ground, the lumped capacitances (C_{pi}s) at the various nodes of DA-1, DA-2 and D-networks can be summarized as shown in Table 3.2. In this, the simplifying but realistic assumption $PS_1 = PS_2 = \ldots = PS_w = PS$ has been used. Also only the parasitic capacitances that contribute to charge flow into the input node [marked X in Figs. 3.2(a)-(c)] of the UGA have been shown. An expression for the transfer function of the BIQ-SDTF, in presence of these parasitic capacitances, can be otained by solving the CCEs around the input nodes of UGA-1 and UGA-3 (Fig. 3.2(d) in the even and the odd phases of the clock signal. The task is considerably eased by first obtaining the voltages $v_{C_{1N}}(n)$ [or $v_{C_{1D}}(n)$] and $v_0(n)$ [or $v_{C_{2D}}(n)$] in terms of the voltages $v_s(n)$ [or $v_0(n)$] by solving for DA-1 (or DA-2) and the D-networks individually. The overall CCEs can then be readily solved. On performing the algebraic manipulations, according to the above, one finally obtains:

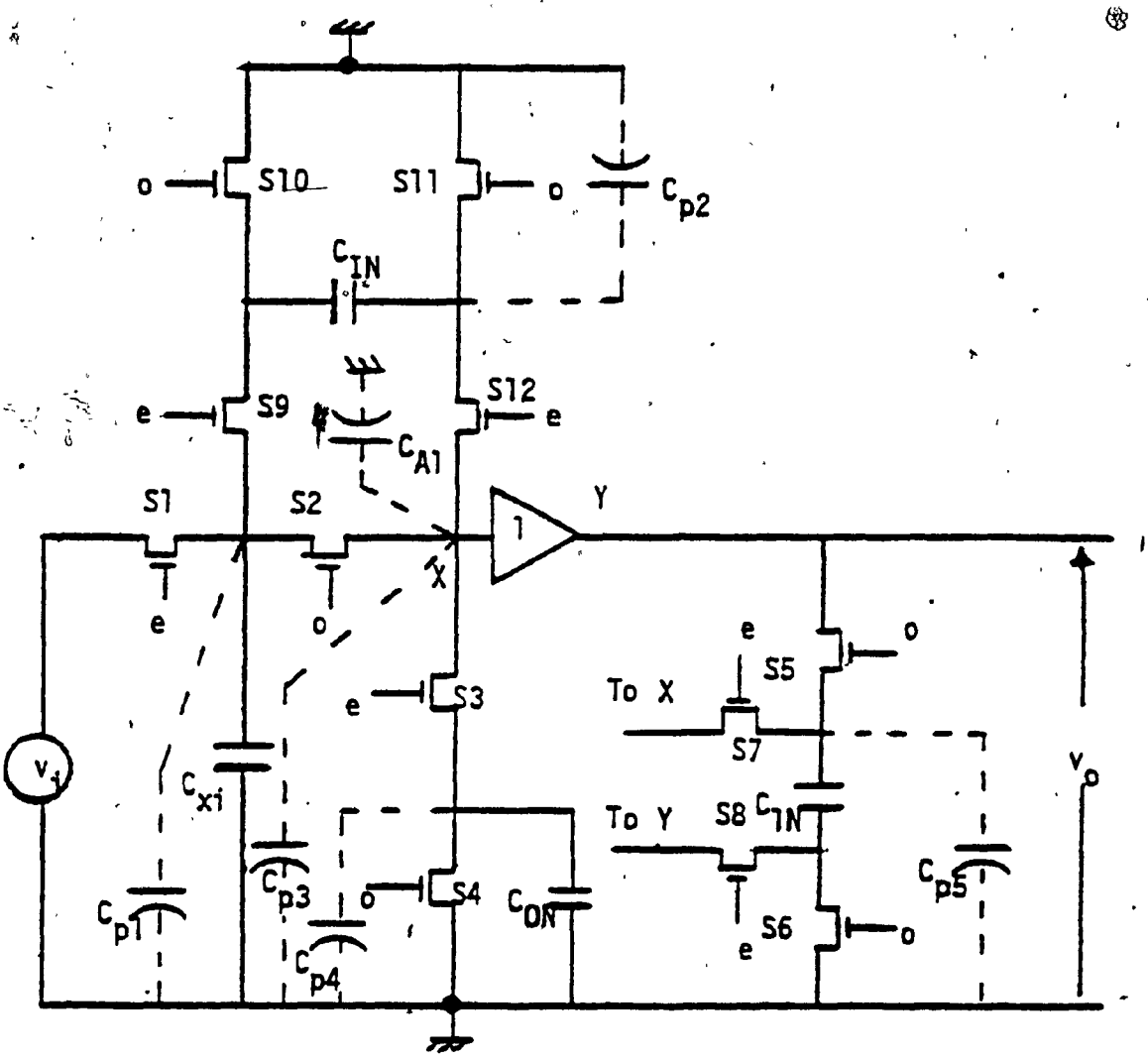


Figure 3.2: (a) The DA-1 network with the parasitic capacitances

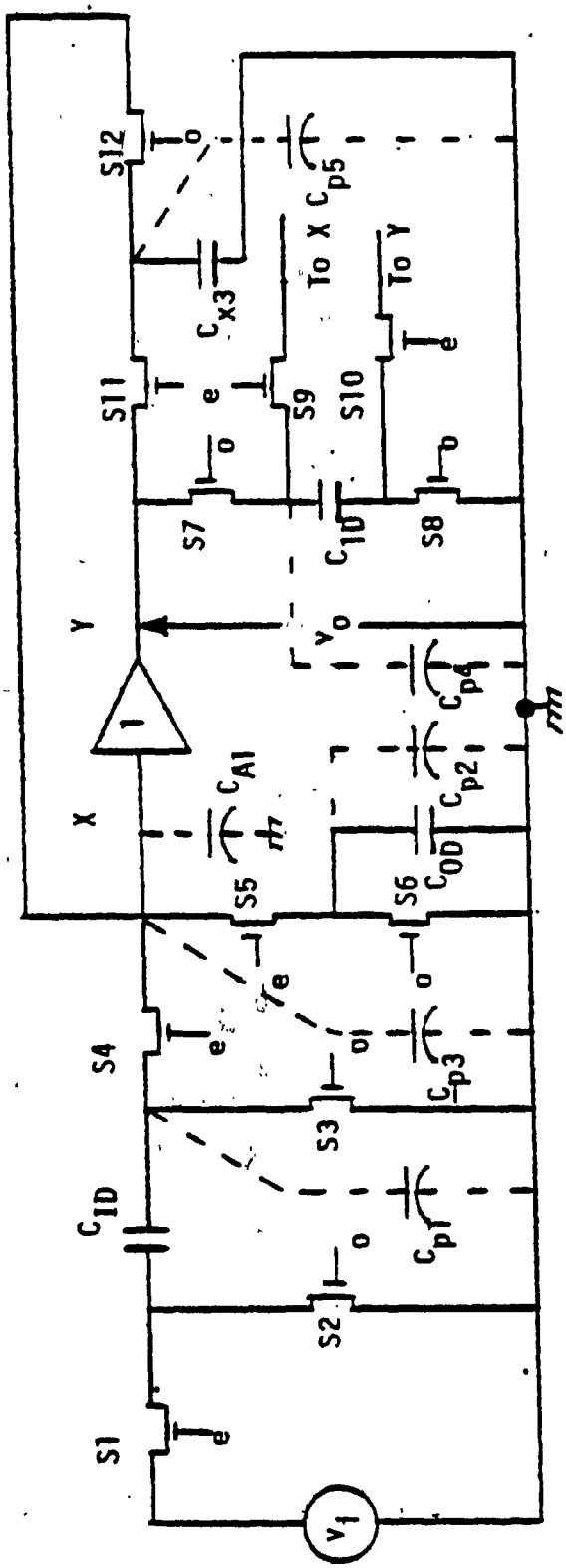


Figure 3.2: (b) The DA-2 network with the parasitic capacitances

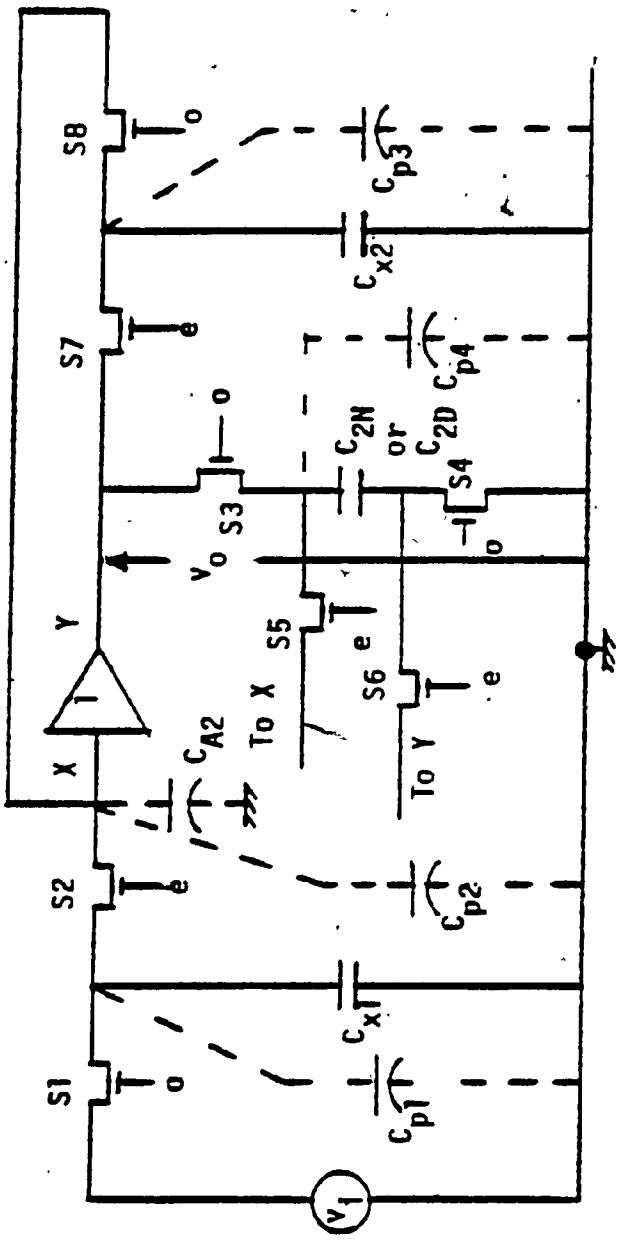


Figure 3.2: (c) The D-network with the parasitic capacitances

TABLE 3.2

PARASITIC CAPACITANCES IN THE DA-1, DA-2 and D-NETWORKS

DA-1 Network	DA-2 Network	D Network
$C_{p1} = 3PS + PST_{xI}$	$C_{p1} = 2PS + PST_{ID}$	$C_{p1} = 2PS + PST_{x1}$
$C_{p2} = 2PS + PST_{IN}$	$C_{p2} = 2PS + PST_{OD}$	$C_{p2} = 2PS$
$C_{p3} = 4PS$	$C_{P3} = 3PS$	$C_{A2} \sim 2PS$
$C_{A1} \sim 2PS$		
$C_{p4} = 2PS + PST_{ON}$	$C_{A1} \sim 2PS$	$C_{p3} = 2PS + PST_{x2}$
$C_{p5} = 2PS + PST_{1N}$	$C_{p4} = 2PS + PST_{1D}$	$C_{p4} = 2PS + PST_{2N(or\ 2D)}$
	$C_{p5} = 2PS + PST_{x3}$	

$$H(z) = \tilde{H}_D \frac{\left[1 + A_1(z) \frac{C_{1N}}{C_{IN}} z^{-1} + \tilde{A}_1(z) A_2(z) \frac{C_{2N}}{C_{IN}} z^{-2} \right]}{\left[1 - A_4(z) \frac{C_{1D}}{C_{ID}+C_{OD}} z^{-1} + A_5(z) \frac{C_{2D}}{C_{ID}+C_{OD}} z^{-2} \right]} \quad (3.21)$$

where the various parameters pertaining to eqn. 3.21 are shown in Table 3.3 [see also Fig. 3.2(d)].

It appears that the effect of the parasitics is to introduce perturbations in the coefficients of the nominal (i.e., ignoring parasitics) BIQ-SDTF in a way similar to the effects of the SH circuits. It should be possible then to arrive at suitable values for the design capacitances by subjecting the transfer function, including the effects of the parasitics and the $Sa(\omega)$ spectral shaping, to an optimization routine and obtaining the necessary design capacitance values for any specific biquad design. Towards this, the minimum circuit capacitance would be taken as PS, which would then lead to suitable values for the C_xs and C_u. The value of C_u in turn would give the values of other design capacitors (viz., C_{IN}, C_{ID}, C_{1D} etc.,) in accordance with the minimum total capacitance design scheme. Two important criteria guiding the optimization routine are that, (i) the C_u value should be as close to the minimum technologically feasible value (0.5pF, for example) as possible, while (ii) all the design capacitance values should lie within the technological range (.5pF to 100pF).

The above ideas could be implemented as a computer aided design algorithm. The salient features in developing this algorithm are described below.

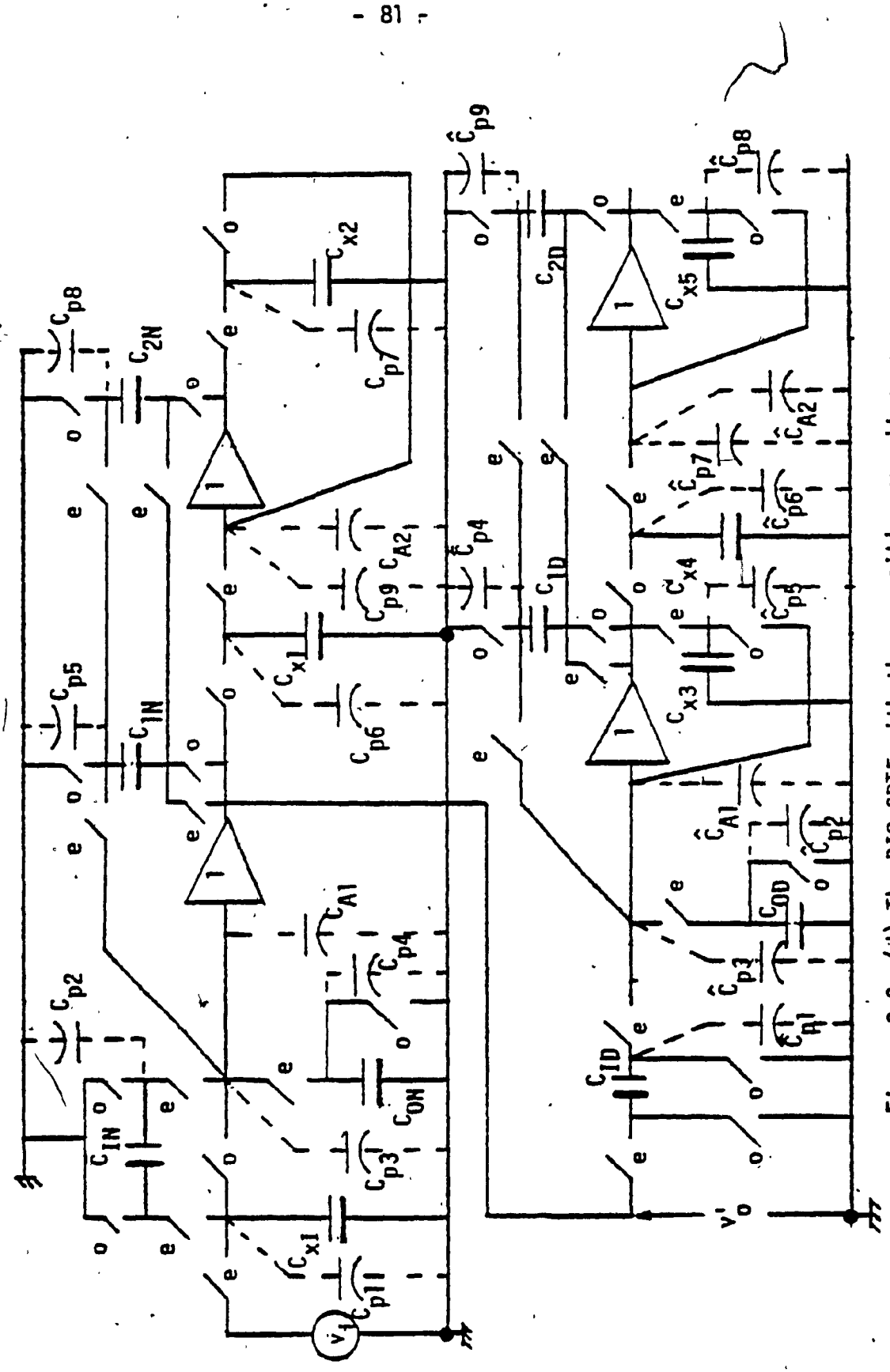


Figure 3.2: (d) The BIQ SDTF with the parasitic capacitances

TABLE 3.3

PARAMETERS OF THE TRANSFER FUNCTION OF THE UGA BASED BIQUADRATIC FILTER WITH PARASITIC CAPACITANCES INCLUDED

Parameter	Expression
ε_1	$(C_{p2} + C_{p3} + C_{p4} + C_{p5} + C_{A1}) \;/\; (C_{IN} + C_{ON})$
ε_2	$(C_{p3} + C_{ps} + C_{A1}) \;/\; C_{1N}$
ε_3	$(C_{p2} + C_{p3} + C_{p4} + C_{p5} + C_{p8} + C_{A1}) \;/\; (C_{IN} + C_{ON})$
ε_4	$(C_{p3} + C_{p5} - C_{A1}) \;/\; C_{1N}$
ε_5	$C_{p8} \;/\; C_{1N}$
$\tilde{A}_1(z)$	$[n(z) \;/\; d(z)]$ where $n(z) = \frac{C_{IN}}{C_{IN}+C_{ON}} \frac{1}{1+\varepsilon_1} \left[\frac{C_{A1}+C_{p3}}{C_{xI}+C_{p1}+C_{p3}+C_{A1}} + \frac{C_{IN}+C_{ON}}{C_{IN}}(1+\varepsilon_1) \frac{C_{xI}+C_{p1}}{C_{xI}+C_{p1}+C_{p3}+C_{A1}} \right]$ $d(z) = 1 - \frac{1+\varepsilon_2}{1+\varepsilon_1} \frac{C_{1N}}{C_{IN}+C_{ON}} \frac{C_{A1}+C_{p3}}{C_{xI}+C_{p1}+C_{p3}+C_{A1}} z^{-1}$
$A_1(z)$	$(1 + \varepsilon_4)\, \tilde{A}_1(z)$
$\tilde{A}_2(z)$	$C_{x1} + C_{p6} \;/\; [(C_{x1} + C_{p6} + C_{p9} + C_{A2}) - (C_{A2} + C_{p9})z^{-1}]$

TABLE 3.3 [cont'd]

Parameter	Expression
$A_2(z)$	$(1 + \varepsilon_5)\,\tilde{A}_2(z)$
ε_7	$(\hat{C}_{p1} + \hat{C}_{p2} + \hat{C}_{p3} + \hat{C}_{p4} + \hat{C}_{p9} + \hat{C}_{A1}) \;/\; (C_{OD} + C_{ID})$
ε_8	$(\hat{C}_{p3} + \hat{C}_{p4} + \hat{C}_{A1}) \;/\; (C_{OD} + C_{ID})$
ε_9	$\hat{C}_{p9} \;/\; C_{2D}$
$\tilde{A}_3(z)$	$(C_{x4} + \hat{C}_{p6}) \;/\; [(C_{x4} + \hat{C}_{p6} + \hat{C}_{p7} + \hat{C}_{A2}) - (\hat{C}_{p7} + \hat{C}_{A2})z^{-1}]$
$A_4(z)$	$(1 + \varepsilon_8) \;/\; (1 + \varepsilon_7)$
A_5	$\tilde{A}_3(z)\,(1 + \varepsilon_9) \;/\; (1 + \varepsilon_7)$
$\tilde{H}_D$	$\dfrac{C_{IN}\,C_{ID}}{(C_{OD}+C_{ON})(C_{ID}+C_{IN})} \cdot \dfrac{1}{(1+\varepsilon_3)(1+\varepsilon_7)}$

3.4 AN ALGORITHM FOR A PARASITIC TOLERANT DESIGN

1. The C_xs are set equal (unity spread).

2. A moderately large ratio values $R_1 = C_u/PS$ and $R_2 = C_x/C_u$ are chosen to start with.

3. Initial design parameters for the filter are computed (for given h_A, Q_p, f_s/f_p) and a firsthand optimization is done including the $Sa(\omega)$ spectral shaping alone. If desired matching with the prescribed frequency response of the nominal filter is not attained (say within 5% rms error), the f_s/f_p ratio is increased from the initial value. This would reduce the effect of the spectral shaping by the SH circuits.

4. Successive optimizations are done at decreasing values of R_1, holding R_2 fixed until a failure in convergence is registered.

5. The immediately preceding value of R_1 is taken. The decrement in R_1 is then subdivided and the algorithm repeated until a minimum feasible R_1 is reached.

6. The design capacitances are determined. The maximum ratio spread (SPMX) among them is computed using the minimum capacitance design scheme I or II, as the case may be. If SPMX turns out to be too large, making some of the capacitors assume values beyond the technological limit (say 100pF), the set of

R_1, R_2 and the capacitors arrived at are rejected. In this case, step 7 is followed.

7. A value of R_2 higher than that assumed in Step 2 is taken and the algorithm repeated from Step 4 with this new initial value of R_2. The initial value of R_1 is taken to be the same as was in Step 2.

8. If the outcome of Step 6 is successful, the set of R_1, R_2 and SPMX is stored and R_2 is decreased in small steps while steps 4 to 6 are repeated. The minimum practical limit of R_2 is set to unity since no practical capacitance can assume a value smaller than C_u.

9. Out of the various acceptable R_1, R_2, SPMX sets, the one with the minimum $S = R_1 + R_2 + SPMX$ is chosen. This ensures that the final design is a minimum capacitance design.

Some additional features that should be incorporated into the algorithm are: (a) the ability to start with a fresh set of R_1, R_2 values should the initial choice fail to give convergence or the required accuracy in approximation, (b) the ability to increase the limit of the maximum design capacitance spread should an initial choice fail to yield capacitances within the specified maximum spread value.

3.5 STEP-BY-STEP DESIGN PROCEDURE

In light of the above discussions, the following procedure may be followed to arrive at a systematic design of a BIQ-SDTF that is tolerant of the parasitic capacitances and that minimizes the total capacitance in the network.

1. Decide upon the error (E%) that can be tolerated with respect to the nominal frequency response.

2. Obtain the minimum f_s/f_p that must be maintained to satisfy the low sensitivity criteria with respect to the capacitance ratio errors (Fig. 3.3).

3. Prewarp the bandlimit frequency ω_p (also ω_n in case of a notch filter) according to the bilinear transformation.

4. Obtain the nominal coefficients h_D, a_{1N}, a_{2N}, a_{1D}, a_{2D} of the BIQ-SDTF using the formulae 3.2(a)-(c) and Table 3.1.

5. Using the above f_s, predistort the nominal BIQ-SDTF coefficients to obtain the design coefficients $\hat{H}$, N_1, ..., D_1 etc. If $\hat{H}$ is $< \frac{1}{2}$, use scheme I of total capacitance minimization. If $\hat{H} > 1/2$, use scheme II.

6. Estimate the values of the parasitic capacitances that may be expected in the circuit layout.

7. Using the above values of the parasitics, f_s, the filter parameters and the error criterion (E%) for the frequency response, use an optimization routine to arrive at the optimal set of values for C_u and C_x.

8. Use the above values for a practical design according to scheme I or scheme II of the minimum capacitance design.

An alogorithm on the above lines has been prepared and used successfully in practice. A flow chart for the algorithm is shown in Table 3.4.

3.6 NUMERICAL AND EXPERIMENTAL WORK

3.6.1 Numerical results

The optimization algorithm considering the parasitic capacitances and including the capacitance minimization scheme was used for a number of values of Q_p (5, 10, 20, 50, 100) and f_s/f_p ratios (5, 10, 15, 20). The filters investigated were LP, HP and BP with a normalized gain of unity. Capacitance values within the present day technological range (0.5 pF to 100 pF) was obtained in every case (using PS = .02 pF). The rms error in frequency response characteristics was set at 5% and standard optimization routine based on gradient method was used. Post optimization error analysis was made after increasing the various capacitance values from the optimum by up to 10%. The error in response was found to remain within the

TABLE 3.4

[FLOW CHART FOR THE PARASITIC TOLERANT DESIGN ALGORITHM]

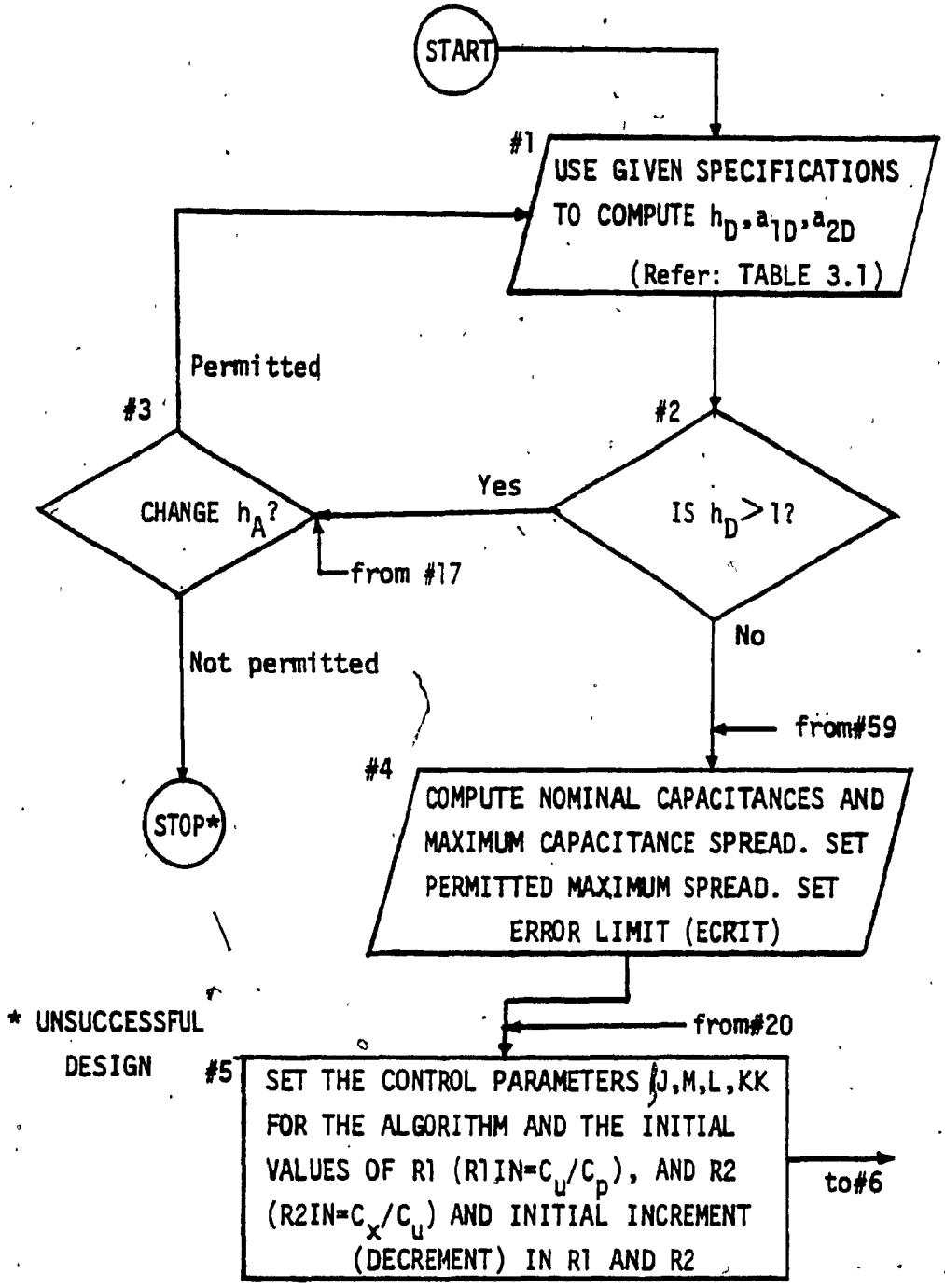


TABLE 3.4 [Cont'd.]

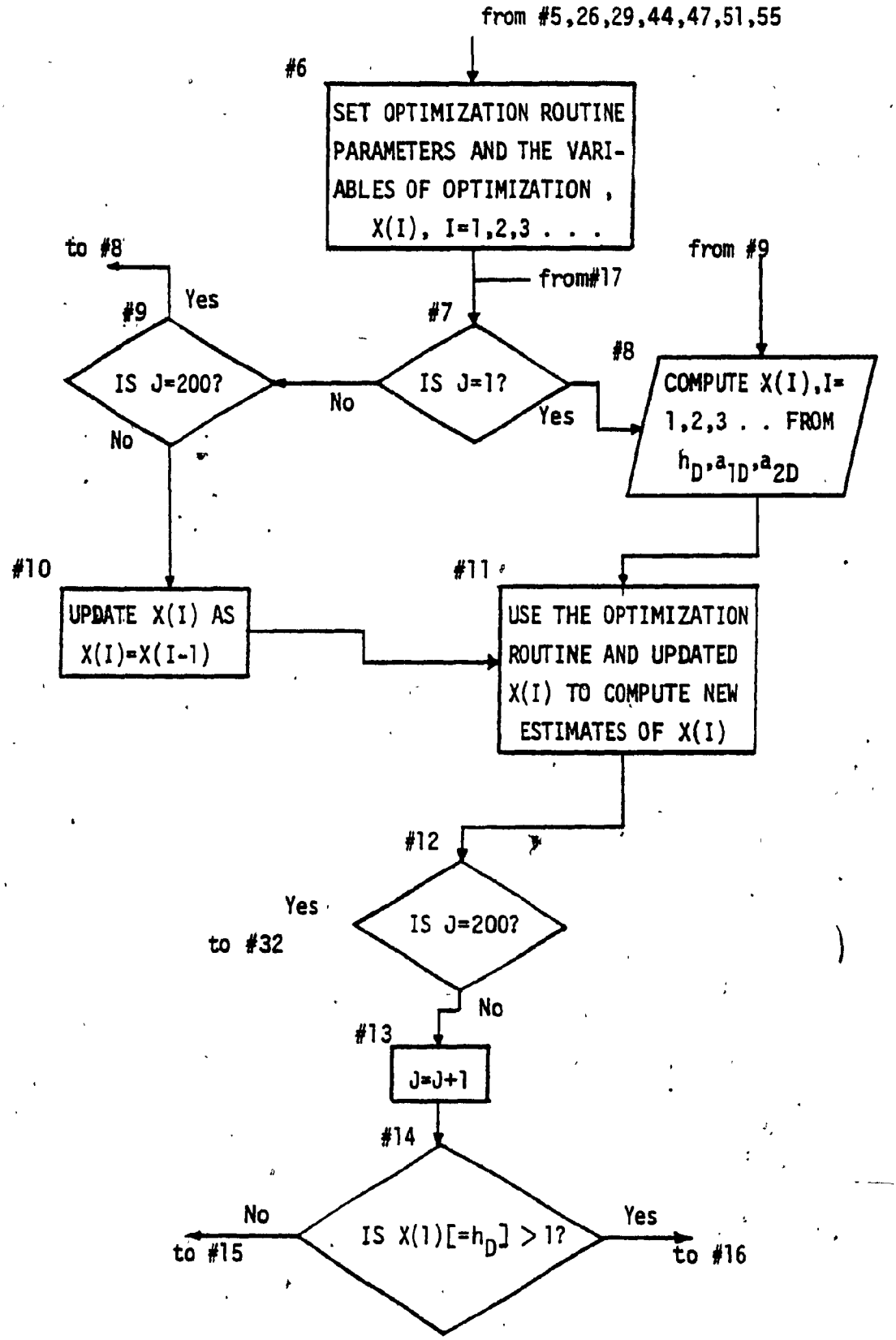


TABLE 3.4 [Cont'd.]

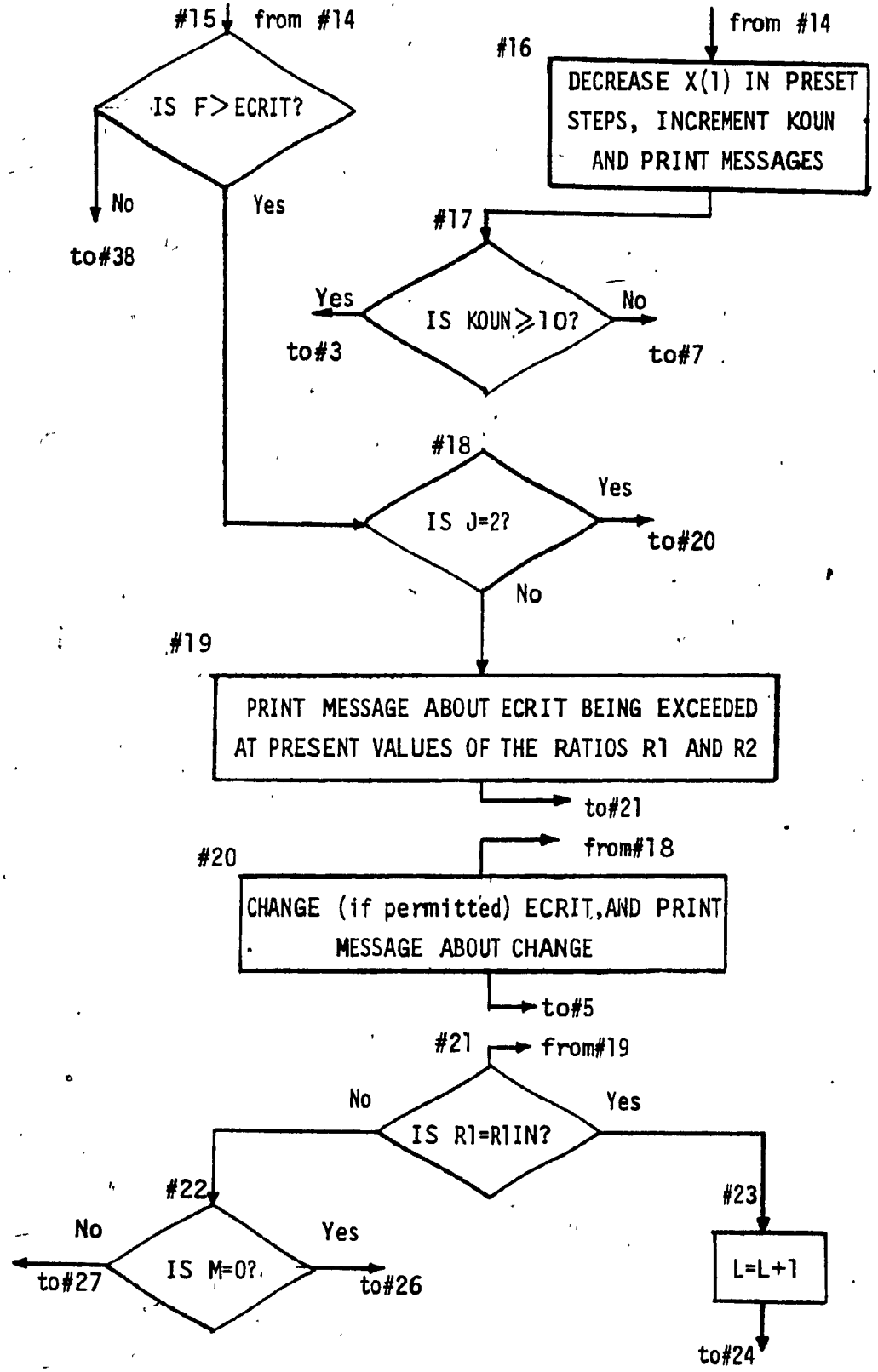


TABLE 3.4 [Cont'd.]

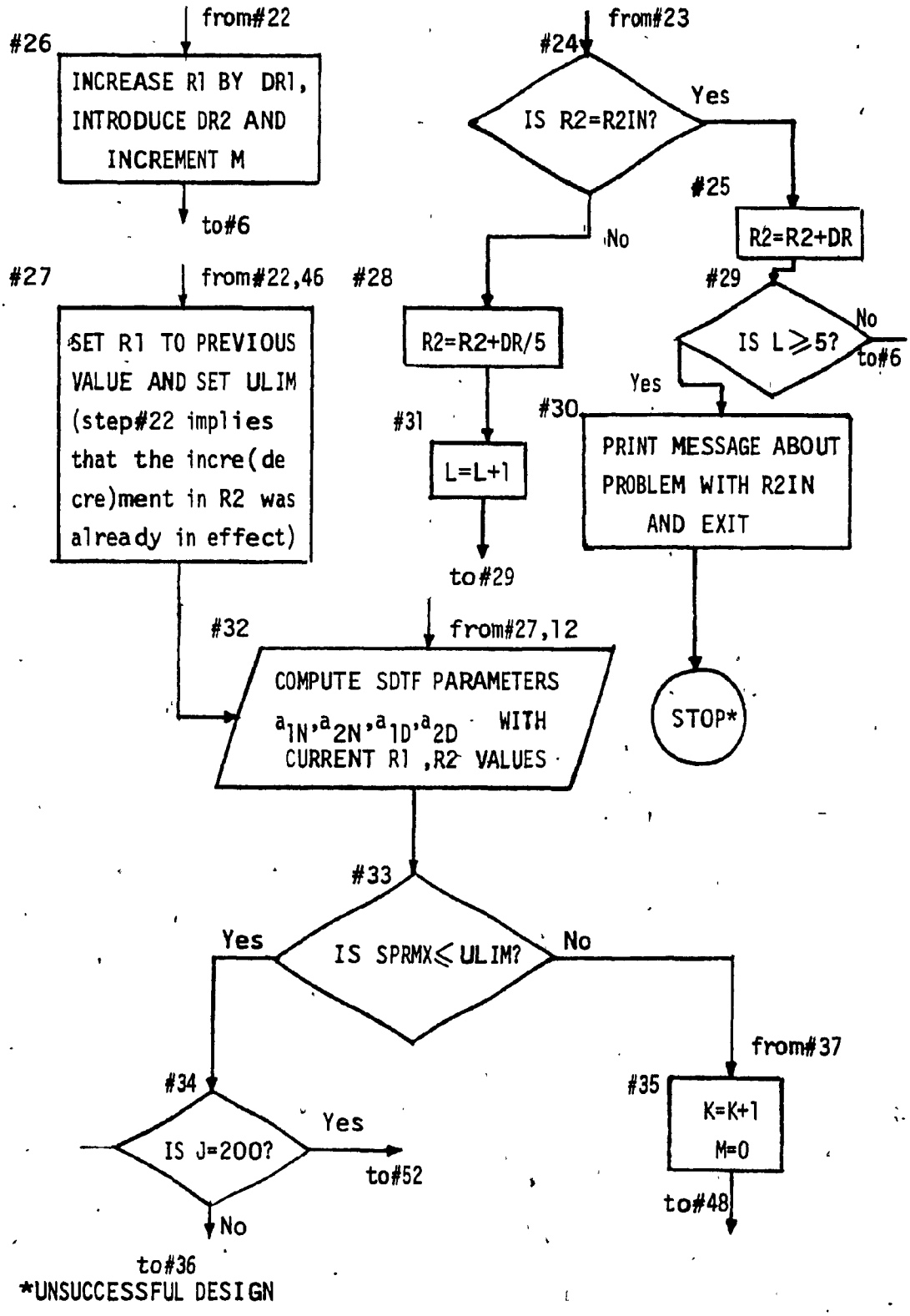


TABLE 3.4 [Cont'd.]

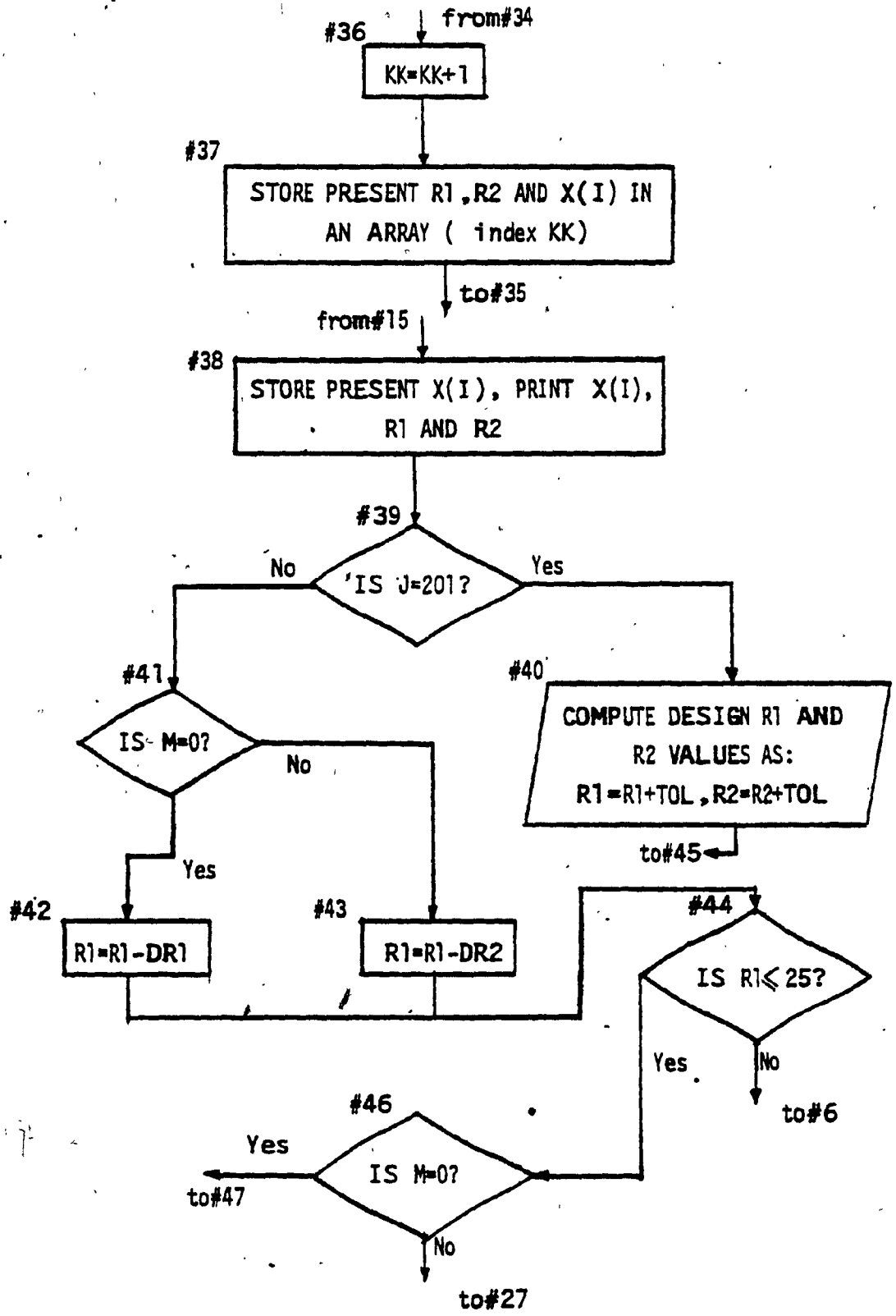


TABLE 3.4 [Cont'd.]

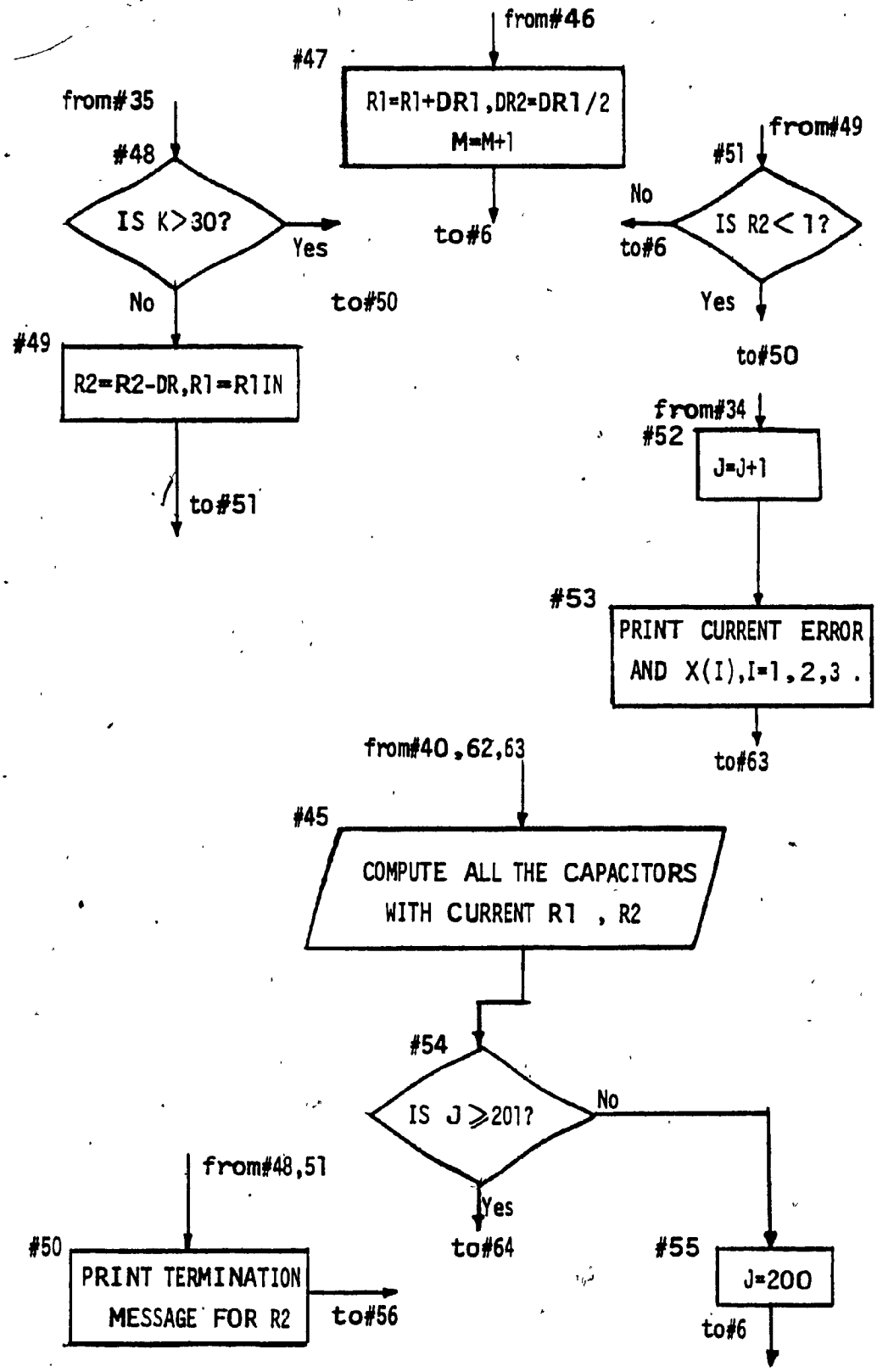
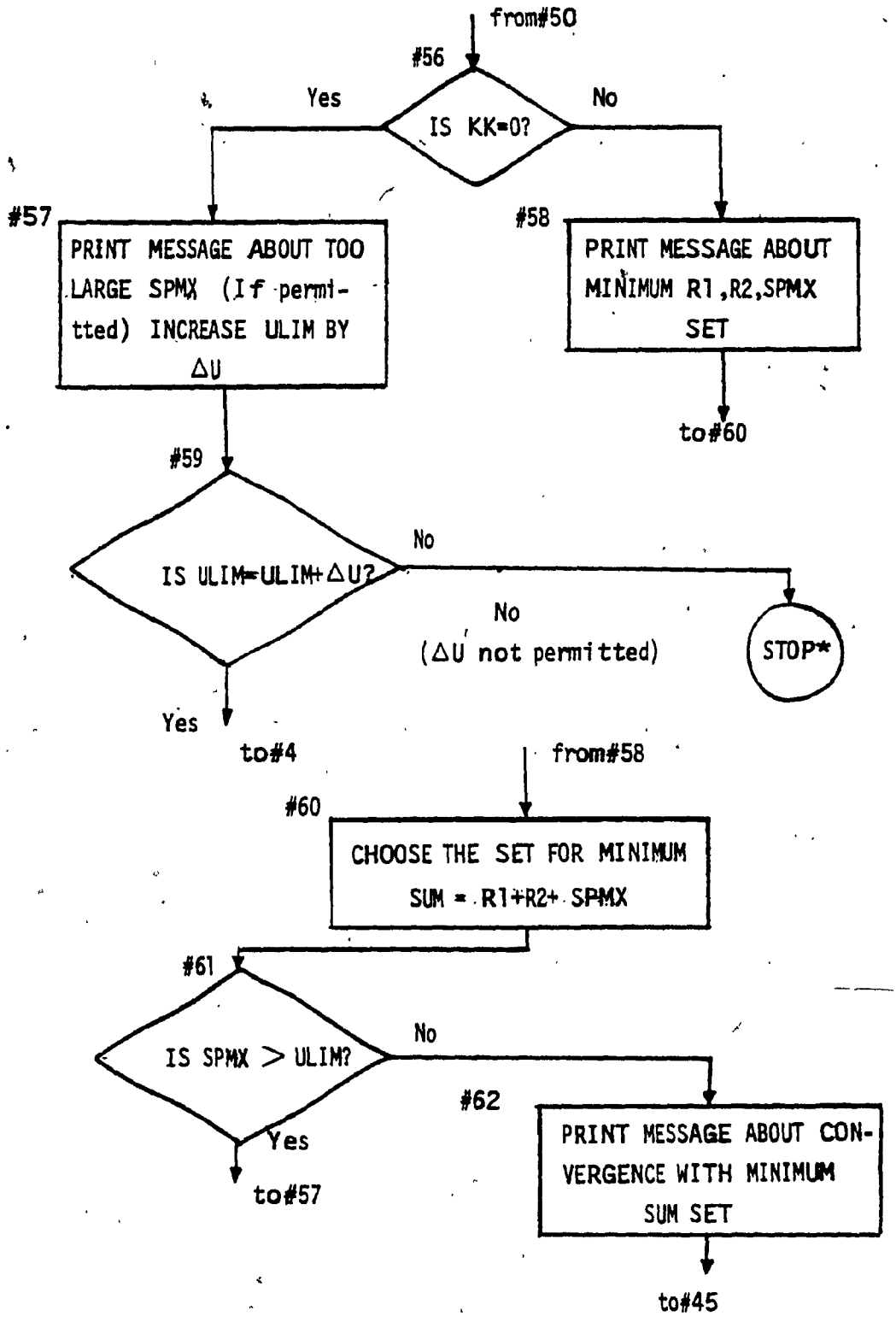
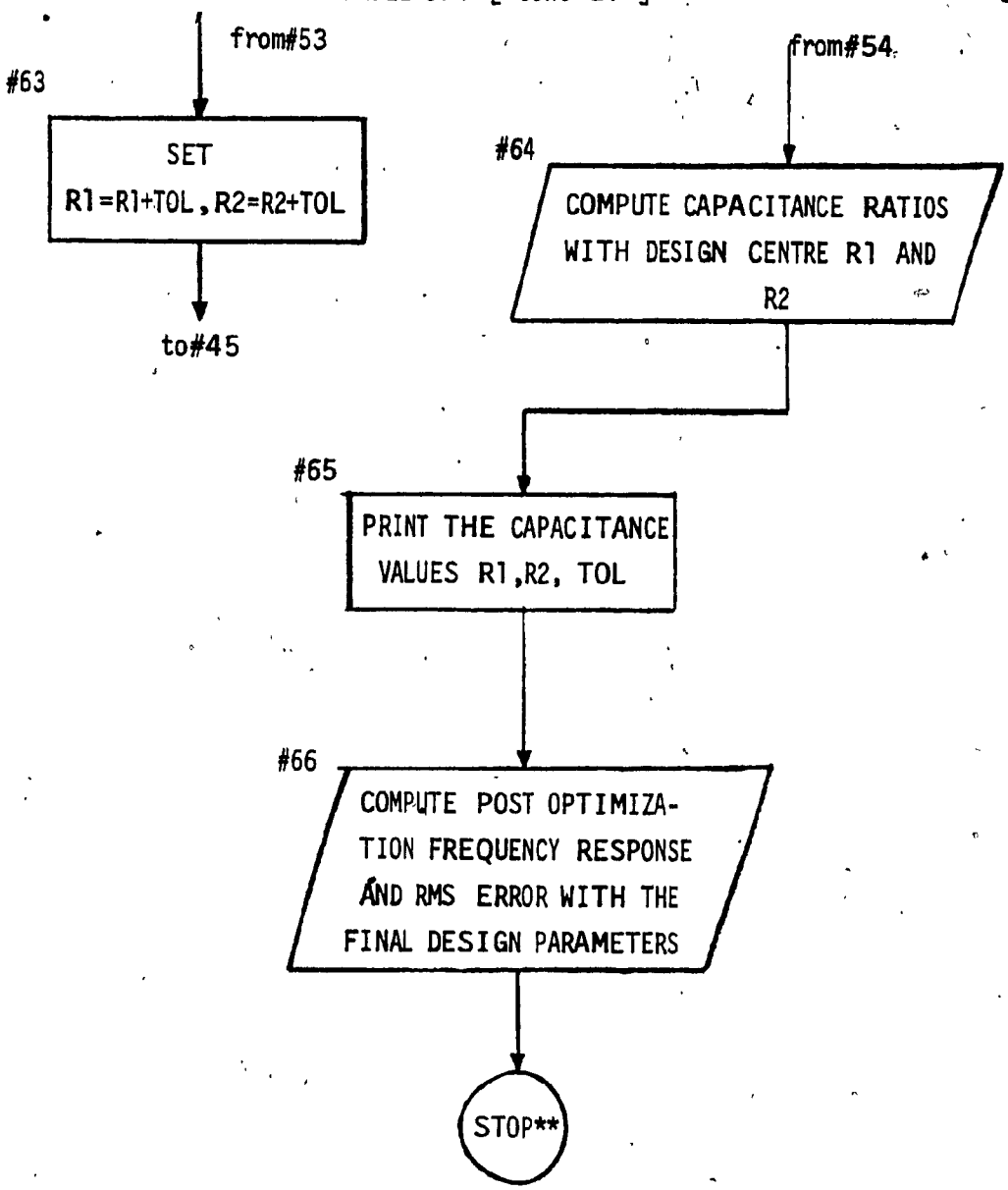


TABLE 3.4 [Cont'd.]



*UNSUCCESSFUL DESIGN

TABLE 3.4 [Cont' d.]



** SUCCESSFUL DESIGN

prescribed limits. However, there was a tendency for the error to increase for variations of 5% or more from the optimal set of values. The result of this investigation revealed that once a minimum set of values of R_1 and R_2 are obtained, increasing the values (up to about 5%) served to produce a better match with the specifications.

Figure 3.3 shows the lower bounds (Q_{ℓ_1}) on Q_p as a function of f_s/f_p to maintain the low sensitivity feature. For a specified Q_p (say, $Q_1 = 5$) the low sensitivity feature will be maintained for $f_s/f_p (=r)$ values between 2 and 8.7 and also for values of r beyond 9. Experimental tests were carried out with $f_s/f_p = 10$.

Figures 3.4(a)-(c) show few representative curves showing the maximum design capacitance spread that is to be expected in a second order bandpass BIQ-SDTF as a function of H_{BP}, Q_p and f_s/f_p ratio. The scheme II of minimization of total capacitance has been used to compute the various capacitances.

3.6.2 Experimental Results

A bandpass filter was designed with $f_s = 10$ kHz for $f_p = 1$ kHz, $Q_p = 5$ and $H_{BP} = 10$. The coefficients a_{1D}, a_{2D} etc. were computed using Table 3.1. The experiments were carried out using discrete capacitors (film/foil type with polysterene dielectric) and analog switches (RCA, type 4066B). Lacking the facility of IC MOS fabrication facilities, the UGAs were realized using μA 741 OAs with 100% negative feedback as shown in Figure 3.5. In the preliminary experiment the

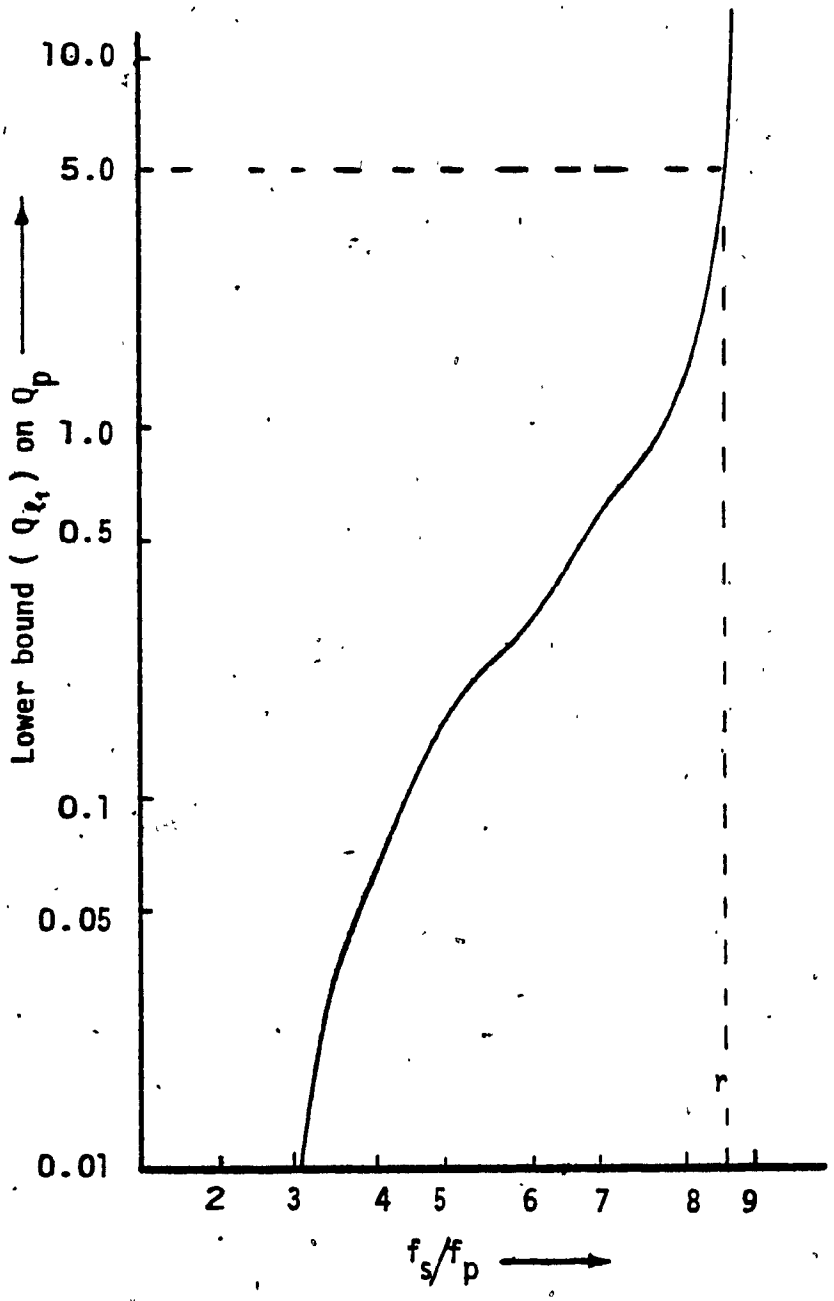


Figure 3.3: Lower bounds on Q_p for a low sensitivity design

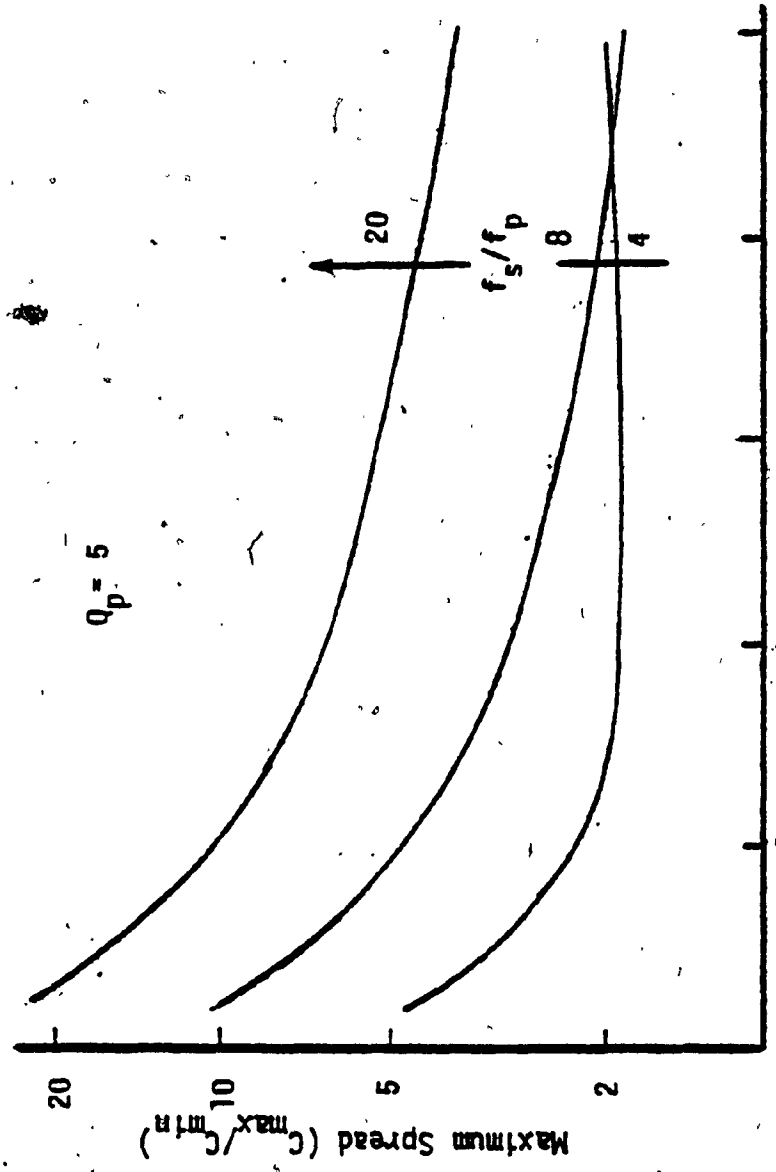


Figure 3.4: (a) Maximum capacitance spread vs. the gain of a bandpass BIQ SDTF realized using UGAs

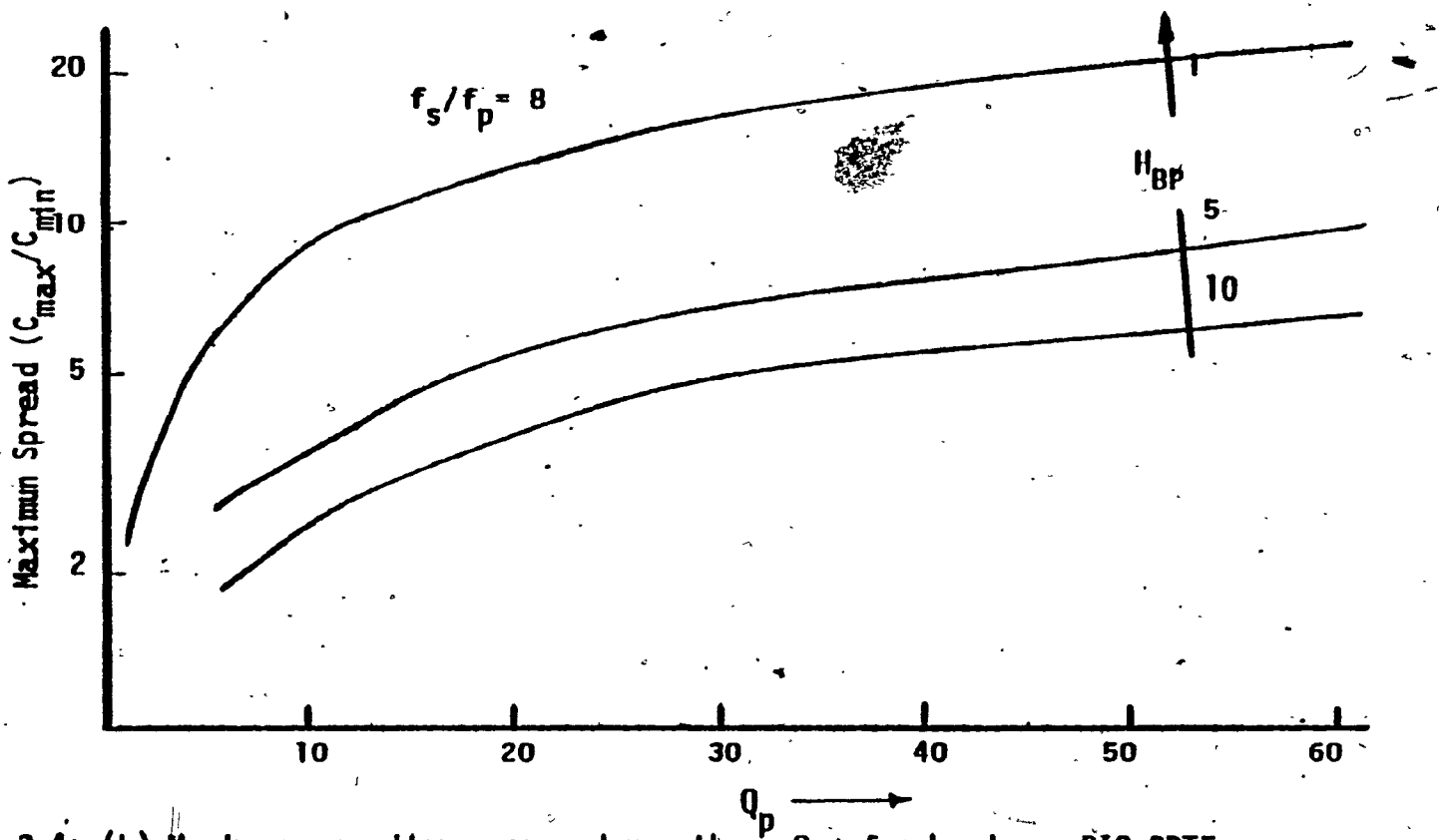


Figure 3.4: (b) Maximum capacitance spread vs. the Q_p of a bandpass BIQ SDTF realized using UGAs

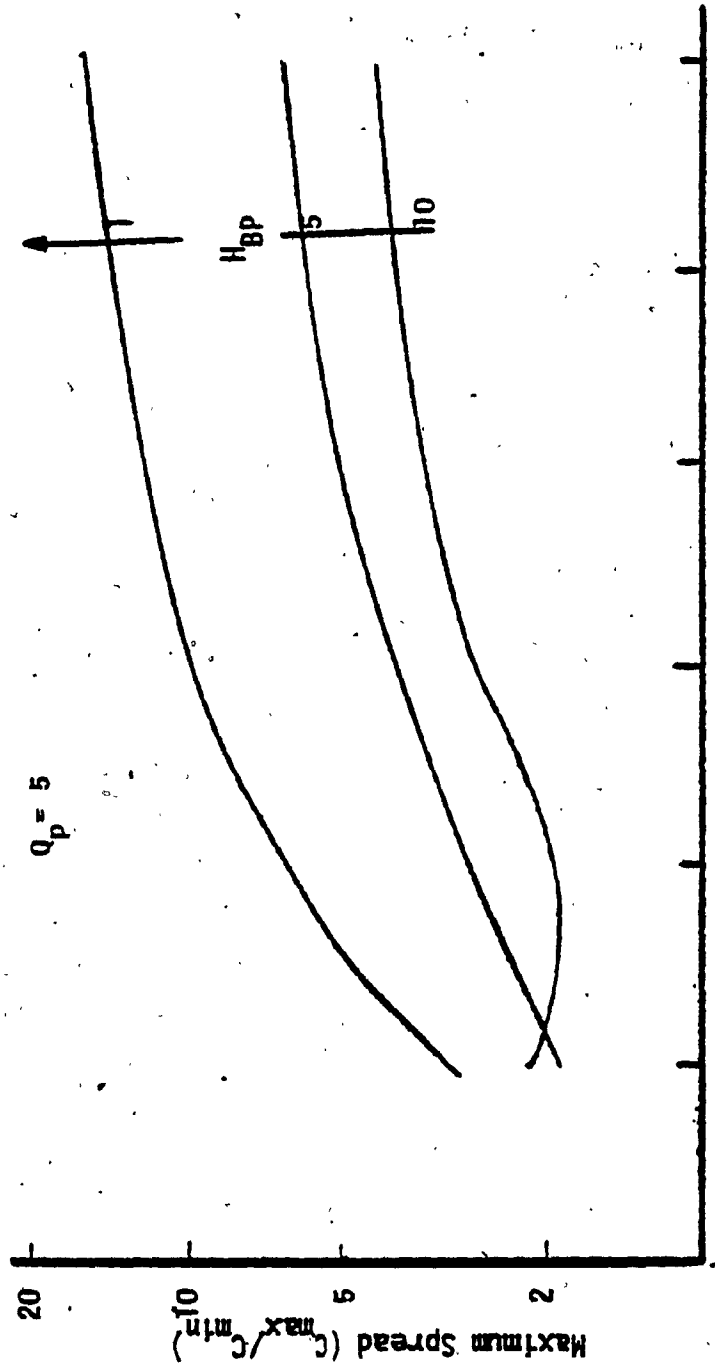


Figure 3.4: (c) Maximum capacitance spread vs. the f_s/f_p ratio in a bandpass BIQ SDTF realized using UGAs

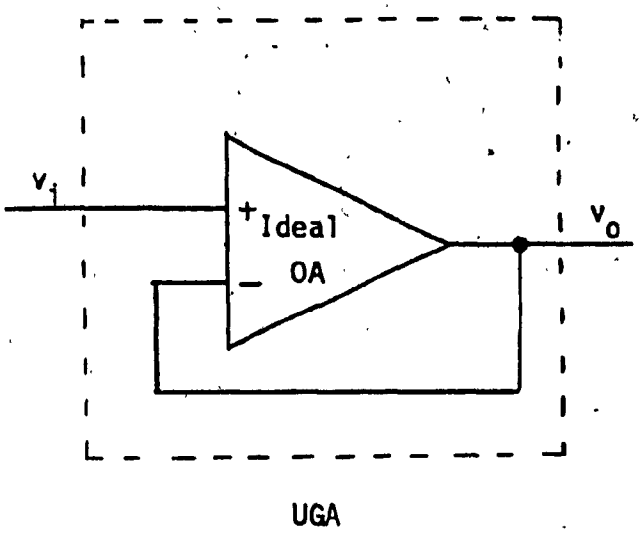


Figure 3.5: Unity Gain Amplifier for experimental work

frequency response [o o] departs markedly from the prescribed response [Fig. 3.6(a)] because of ignoring the Sa(ω) spectral shaping by the SH circuits. Predistorting the parameters h_D, a_{1N}, a_{2N}, a_{1D}, a_{2D} using an optimization algorithm, as discussed in section 3.3.2, and changing the capacitances accordingly produced the response [+ + +], which is very close to the desired response. The capacitances used were in the range 1.68 nF to 18.45 nF. The design was repeated using $H_{BP} = 5$ and $C_u = 1$nF and the capacitance minimization scheme I yielding capacitances in the range 1nF to 3.11 nF. The response was very close to the ideal [Fig. 3.6(b)] and is shown by [Δ Δ].

Experiments were carried out to verify the theoretical predictions using the optimization routine for a parasitic tolerant design. The value of PS in the circuit layout used was of the order of 47 pF. The optimal set of capacitors were accordingly scaled up by an appropriate factor. The agreements with the theoretical responses were very satisfactory.

3.7 CONCLUSION

A systematic procedure for realizing BIQ-SDTFs, bilinearly equivalent to the popular analog biquadratic functions, has been given. A criterion has been developed to choose the clock frequency that yields very low sensitivity realizations. Schemes are proposed to minimize the total capacitance in the circuit. An optimization algorithm has been developed that makes the given design tolerant of the parasitic capacitances. The optimization is extremely efficient in

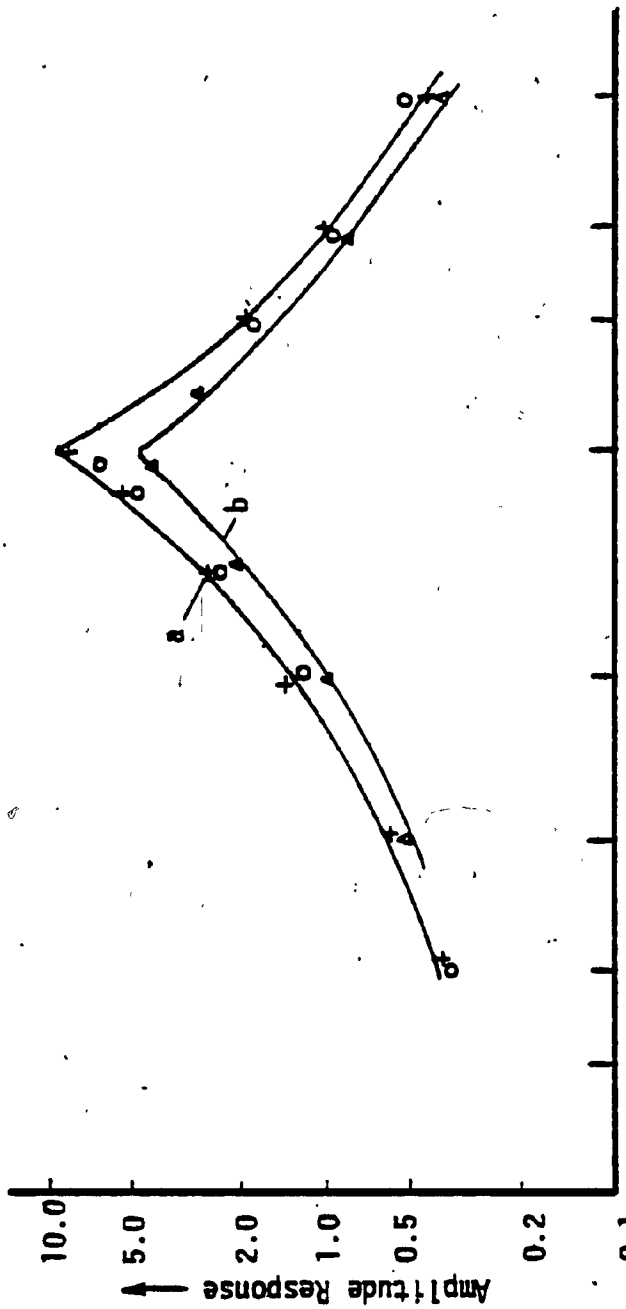


Figure 3.6: Responses of the Switched Capacitor Bandpass filter with Q_p=5,
(a) H_{BP}=10 , (b) H_{BP}=5

that the resulting design is relatively unaffected by the parasitic capacitances even when the exact levels of the parasitic capacitances are not known. Finally, the various practical considerations in the design are incorporated into a step-by-step design procedure. Extensive computer simulations and experimental investigations using discrete capacitors, CMOS switches and IC OAs show close agreements with the theoretical analysis. Although the circuits were tested in the laboratory using UGAs realized from OAs, the possibility exists of constructing the UGAs using MOSFETs only. This would lead to substantial savings in the substrate area in a large scale or very large scale integration technology. Finally, the realizations have the property that the coefficients in the numerator and denominator polynomials of the SDTF functions can be controlled by independent capacitance ratios. Thus, they are attractive candidates for adaptive filter applications.

The main disadvantage with the present designs are the need for a large number of UGAs and capacitors, 4 and 14 respectively. A number of designs already exists in the literature using only two OAs and a reduced number of capacitors. Consequently, even though a UGA may require much less area than an OA, the total substrate area needed for the proposed SDTF may not be substantially less than that in an existing design realizing the corresponding SDTF using two OAs. However, if the number of UGAs is reduced to two and also if the number of capacitors is made comparable to that in the two OA-based realizations, it is reasonable to expect a relative savings in the total substrate area. This problem is considered in the following chapter.

CHAPTER FOUR

IMPROVED REALIZATION OF BIQUADRATIC SAMPLED DATA FILTERS

4.1 INTRODUCTION

Designs of second order sampled data filters, bilinearly equivalent to their analog counterparts, using UGAs and SCs have been presented in the preceeding chapter. In spite of the simplicity in the methodology of the synthesis procedure, the proposed method has one important drawback. It needs a large number of components (4 UGAs, 14 capacitors, 34 switches) to realize the BIQ-SDTF. Consequently, the expected reduction in the substrate area due to employing UGAs as compared to OAs in existing designs may not materialize.

In this chapter, the previous design philosophy is reviewed with an aim to further reduce the number of components. It is shown that by using a new basic building block, viz., a composite delay and add (CDA) network, a BIQ-SDTF can be realized employing only two UGAs and (at most) ten capacitors[55]. These are about the same number of components used in SCF designs employing OAs as infinite gain inverting amplifiers. In what follows, the operation of the CDA netowrk is explained in section 4.2 of this chapter. The sensitivity of the design pole frequency (ω_p) and pole Q (Q_p) of the resulting BIQ-SDTF is studied in the same section. The analysis of the effect of the parasitic capacitance is presented in section 4.3. By a proper choice of the topology, a SDTF can be made insensitive to the parasitics

associated with the bottom plates of the capacitors. On the other hand, SDTFs using UGAs can not be made insensitive to the parasitics associated with the top plates of the capacitors. However, as has been shown in the previous chapter, their effect on the realizations can be made negligible by an optimization procedure. **In effect, the designs can be made parasitic tolerant.** The philosophy of the parasitic tolerant design for the improved BIQ-SDTF developed in this chapter is described in section 4.4, together with a scheme to minimize the total capacitance. A flow chart for the required numerical algorithm is also provided. In addition, the effect of the offset voltage of the UGAs on the realizations is examined in section 4.5. Guidelines are provided to make this effect negligible and should be used wherever possible. In cases where such guidelines become impractical, use of a minimization algorithm is suggested and the considerations pertaining to such minimization algorithm are discussed. Section 4.6 presents an alternative realization of the BIQ-SDTFs that (i) are equivalent to the bilinearly transformed analog counterparts, (ii) need fewer capacitors than the design proposed in section 4.1, but (iii) have similar limitations on realizable Q_p and ω_p values as those of canonic realizations mentioned before[27]. Section 4.7 gives results of the numerical simulations and experimental tests. The full potential of the design presented in this chapter can be realized only if IC MOS buffers [32] are used in them. Since the author did not have access to them, OAs were used for the realizations of the UGAs in the experimental investigations. Experimental results show very good agreement with theoretical predictions.

4.2 ANALYSIS

4.2.1 Realization of BIQ-SDTF using Composite Delay-and-Add Network

Figure 4.1(a) shows the basic building block, namely the composite delay-and-add network for realizing the BIQ-SDTF while Figure 4.1(b) shows the clock signal of period $T(=1/f_s)$. Considering the charge conservation equations (CCEs) around the input node(x_1) of the UGA for the switching instants $t = (n - \frac{1}{2})T$ and $t = nT$, one would have

$$(C_1 + C_{s1})v_{x_1}(n) + C_{s1}v_{x_1}(n - \tfrac{1}{2}) - C_1 v_s(n) = 0 \qquad (4.1a)$$

$$C_{o1}v_{x_1}(n - \tfrac{1}{2}) + C_2 v_s(n-1) + C_3 v_{o2}(n-1) = 0 \qquad (4.1b)$$

where v_s and v_{o2} are the input signals to the CDA network. We have used n for nT. Replacing for $v_{x_1}(n - \frac{1}{2})$ in eqn. (4.1a) from eqn. (4.1b) and since $v_{o1}(n) = v_{x1}(n)$ etc., for the UGA, one gets

$$\begin{aligned} v_{O1}(n) &= [C_1/(C_1 + C_{s1})]\, v_s(n) \\ &+ [C_2C_{s1}/(C_{o1}(C_1 + C_{s1}))]\, v_s(n-1) \\ &+ [C_3C_{s1}/(C_{o1}(C_1 + C_{s1}))]\, v_{02}(n-1) \end{aligned} \qquad (4.2)$$

Writing $A_1 = C_1/(C_1 + C_{s1})$, $A_2 = C_2C_{s1}/(C_{o1}(C_1 + C_{s1}))$, $A_3 = C_3C_{s1}/((C_{o1}(C_1 + C_{s1}))$ and taking $\mathcal{Z}$-transforms on both sides of eqn. 4.2 we have

$$V_{o1}^e(z) = A_1V_s^e(z) + A_2 z^{-1} V_s^e(z) + A_3z^{-1}V_{o2}^e(z) \qquad (4.3a)$$

where $V_y^e(z) = \mathcal{Z}[v_y(n)]$, $y = s, 01\ 02$ (4.3b)

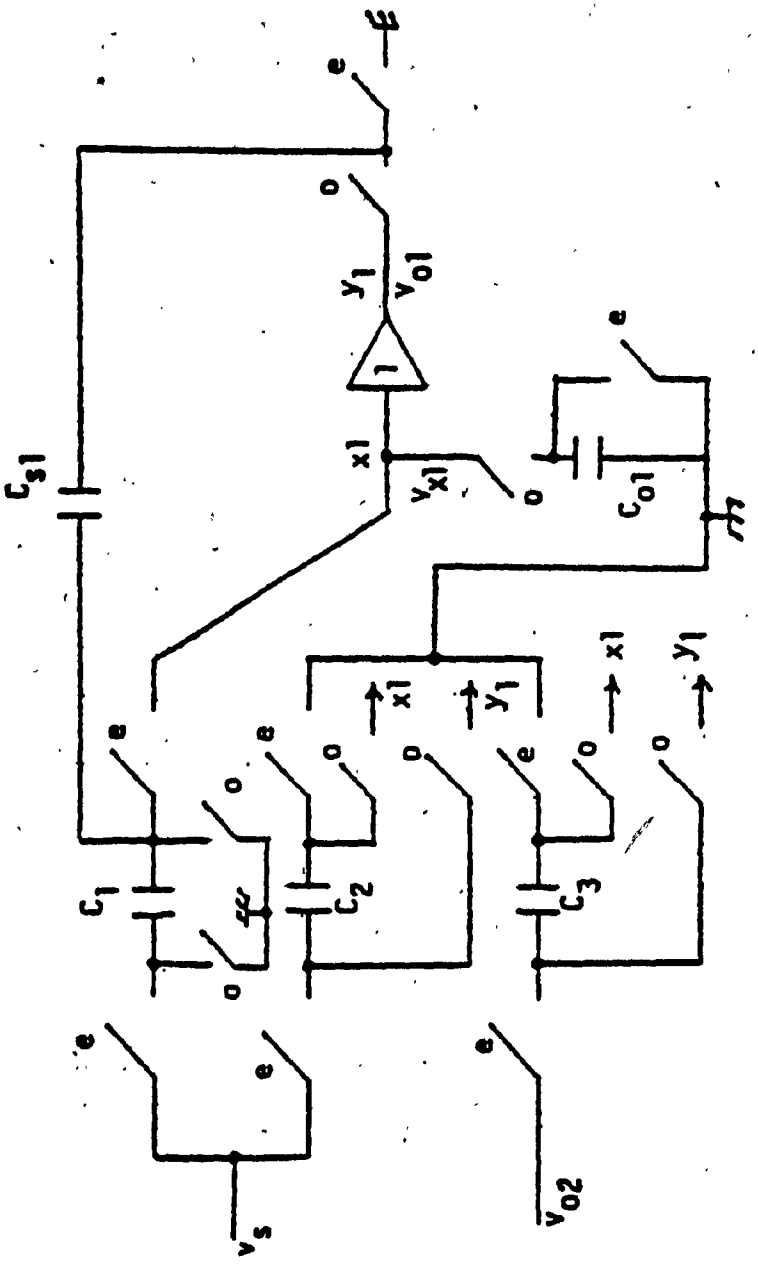


Figure 4.1: (a) The composite delay and add (CDA) network

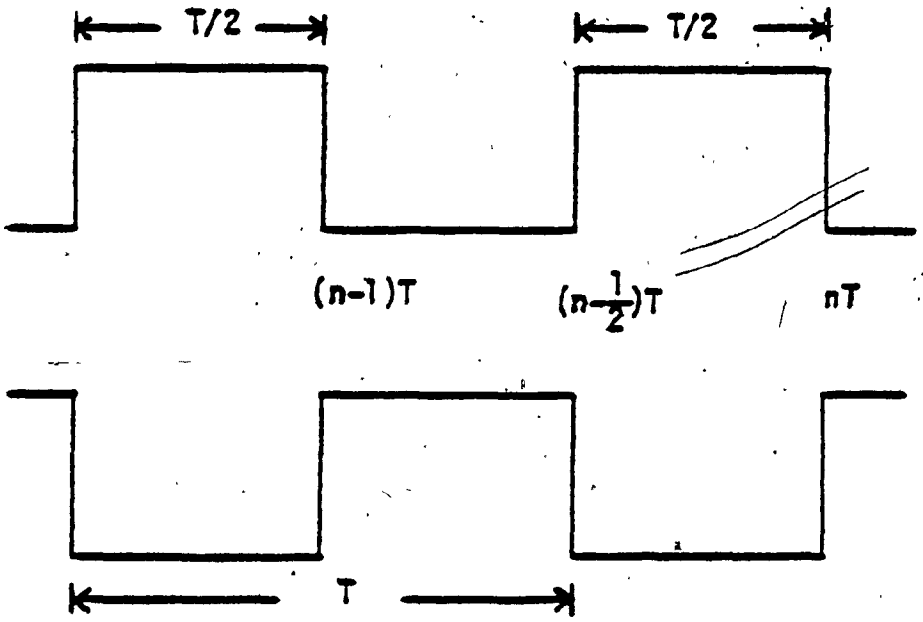


Figure 4.1: (b) The biphase clock signal of period T

Eqn. 4.3 represents a linear sum of the different signals together with their delayed versions and is the fundamental equation for the CDA network. It is observed that the signs of the coefficients A_2 and (or) of A_3 can be easily reversed by reversing the terminals of C_2 and (or) of C_3 during the "odd" phase ($t = (2n-1)T/2$, $n = 1,2,...$). With the basic equation of the CDA available, realization of a general BIQ-SDTF is straightforward and is shown in Fig. 4.2. Omitting the argument z for simplicty, we can derive, as above,

$$V_{o1}^e = A_1 V_s^e + A_2 z^{-1} V_s^e + A_3 z^{-1} V_{o2}^e \tag{4.4a}$$

$$V_{o2}^e = B_1 V_{o1}^e - B_2 z^{-1} V_{o1}^e + B_3 z^{-1} V_s^e \tag{4.4b}$$

which gives

$$[V_{o1}^e / V_s^e] = \frac{A_1 + A_2 z^{-1} + A_3 B_3 z^{-2}}{1 - B_1 A_3 z^{-1} + B_2 A_3 z^{-2}} \tag{4.5}$$

where $B_1 = C_4/(C_1+C_{s2})$, $B_2 = C_5 C_{s2}/(C_{02}(C_4+C_{s2}))$, $B_3 = C_6 C_{s2}/(C_{o2}(C_4+ C_{s2}))$. Eqn. 4.5 represents the BIQ-SDTF desired. Assuming the well-known bilinear transformation $s = \frac{2}{T}(1-z^{-1})/(1+z^{-1})$, one can identify $A_1 = h_d$, $A_2 = h_D a_{1N}$, $A_3 B_3 = h_D a_{2N}$, $B_1 A_3 = a_{1D}$ and $B_2 A_3 = a_{2D}$ where the parameters h_D, a_{1D},... are given in Table 4.1 for the five popular analog biquadratic filters. The following definitions are needed to use Table 4.1.

ω_n, ω_p, Q_p: the notch frequency, pole frequency and pole-Q_p of the analog biquadratic filter, respectively.

h_A: flat gain of the analog filter.

f_s: clock frequency in the SC filter.

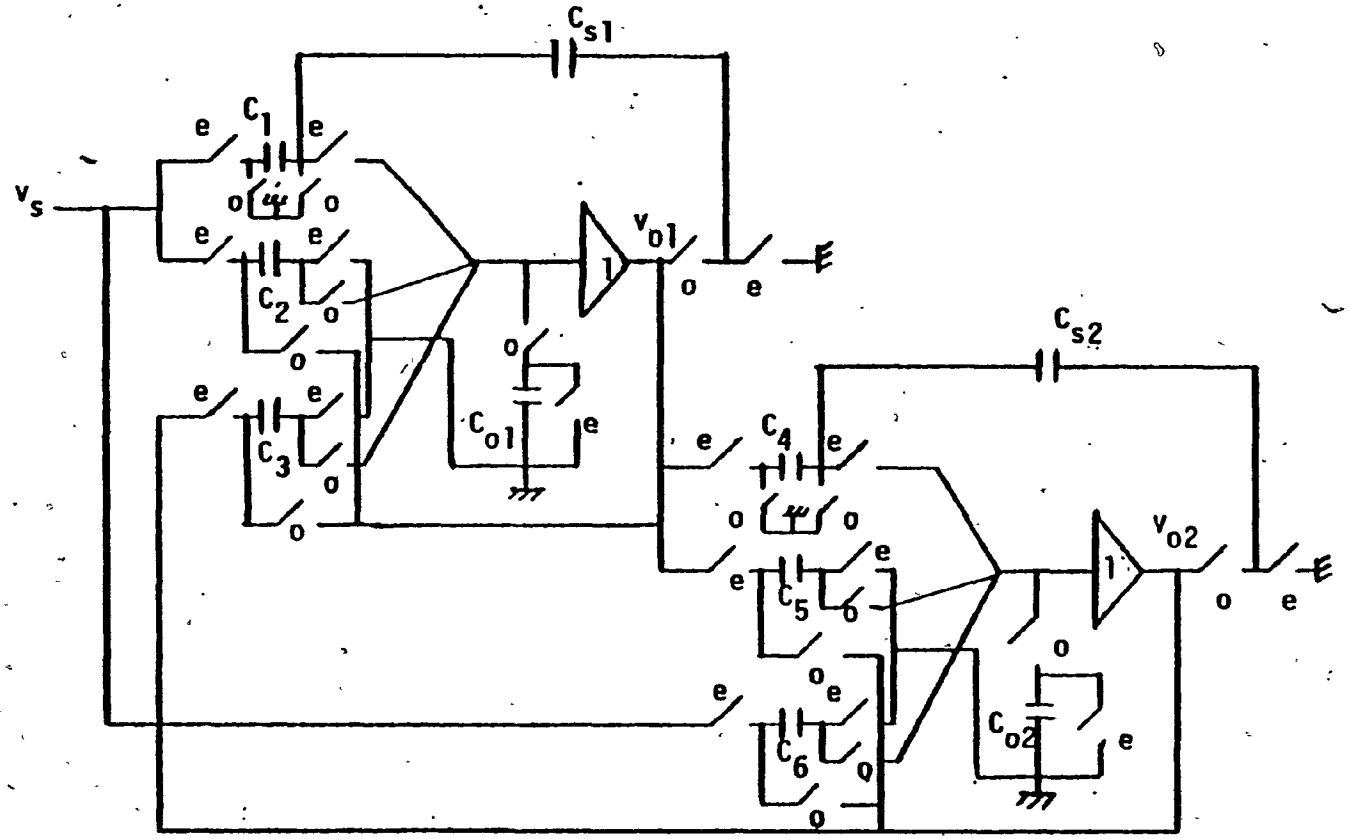


Figure 4.2: The general biquadratic sampled data filter (BIQ-SDTF)

TABLE 4.1

DESIGN COEFFICIENTS OF BIQ SDTF BILINEARLY EQUIVALENT TO THE ANALOG BIQUADRATIC FILTERS

Filter Type	Analog Transfer Function	Sampled-Data Transfer Function Coefficients* $H(z)=h_D\ (1+a_{1N}z^{-1}+a_{2N}z^{-2})/[1-a_{1D}z^{-1}+a_{2D}z^{-2}]$		
		h_D	a_{1N}	a_{2N}
LPF	$H_{LP}\ \omega_p^2/F_1$	$H_{LP}\ \tilde{\omega}_p^2/F_2$	2	1
HPF	$H_{HP}\ s^2/F_1$	$H_{HP}\ a^2/F_2$	-2	1
BPF	$H_{BP}(\omega_p/Q_p)s/F_1$	$H_{BP}(\tilde{\omega}_p/Q_p)a/F_2$	0	-1
APF	$H_{AP}\ \frac{F_1-2(\omega_p/Q_p)s}{F_1}$	$H_{AP}\ a_{2D}$	$-a_{1D}/a_{2D}$	$1/a_{2D}$
NOTCH	$H_N\ (s^2+\omega_n^2)/F_1$	$H_N\ (a^2+\tilde{\omega}_n^2)/F_2$	$-\frac{2(a^2-\tilde{\omega}_n^2)}{a^2+\tilde{\omega}_n^2}$	1

* The coefficients a_{1D}, a_{2D} have already been shown in eqn. 3.2(c) in the text.

$a = 2f_s$

$\tilde{\omega}_x = a \tan(\omega_x/a)$, the prewarped frequency, x = p,n.

$F_1 = s^2 + (\omega_p/Q_p)s + \omega_p^2$, $F_2 = a^2 + (\tilde{\omega}_p/Q_p)a + \tilde{\omega}_p^2$

$a_{1D} = 2(a^2 - \tilde{\omega}_p^2)/F_2$, $a_{2D} = [a^2 - (\tilde{\omega}_p/Q_p)a + \tilde{\omega}_p^2]/F_2$.

4.2.2 ω_p and Q_p Sensitivities

The ω_p and Q_p sensitivities in the BIQ-SDTF are related to the relative accuracies in the capacitance ratios and hence can be kept very low provided certain relations among the filter parameters are satisfied. In an earlier report [40] and also in the previous chapter, such relations lead to a first-hand choice of the clock frequency to be used in the SDTF for a given h_A, ω_p and Q_p. A similar analysis is included here for the case of the BIQ-SDTF proposed in this chapter. To start with, it can be shown that the normalized (with respect to $2f_s$) pole frequency and pole Q_p are related to coefficients of the BIQ-SDTF according to:

$$\Omega_p = \tilde{\omega}_p/2f_s = \sqrt{(1-a_{1D}+a_{2D}) \;/\; (1+a_{1D}+a_{2D})} \qquad (4.6a)$$

$$Q_p = \sqrt{(1-a_{1D}+a_{2D})\,(1+a_{1D}+a_{2D})} \;/\; [2(1-a_{2D})] \qquad (4.6b)$$

Writing $N = 1-a_{1D}+a_{2D}$ and $D = 1+a_{1D}+a_{2D}$ one has

$$\frac{d\Omega_p}{\Omega_p} = \frac{1}{2}\left[\frac{da_{2D} - da_{1D}}{N} - \frac{da_{2D}+da_{1D}}{N}\right] \qquad (4.7a)$$

and

$$\frac{dQ_p}{Q_p} = \frac{1}{2}\left[\frac{da_{2D} - da_{1D}}{N} + \frac{da_{2D}+da_{1D}}{N} + \frac{da_{2D}}{1 - a_{2D}}\right] \qquad (4.7b)$$

where

$$a_{1D} = C_3\, C_{s1}\, C_4/(C_{o1}(C_1+C_{s1})(C_4+C_{s2})) \qquad (4.8a)$$

$$a_{2D} = C_3 C_{s1} C_5 C_{s2}/(C_{o1} C_{o2}(C_1+C_{s1})(C_4+C_{s2})) \qquad (4.8b)$$

Writing $\alpha_1 = C_{s1}/C_1$, $\alpha_2 = C_{o1}/C_1$, $\alpha_3 = C_3/C_1$, $\alpha_4 = C_4/C_1$, $\alpha_5 = C_{s2}/C_1$, $\alpha_6 = C_5/C_1$, $\alpha_7 = C_6/C_1$, $\alpha_8 = C_{o2}/C_1$, one has

$$a_{1D} = \alpha_1\alpha_3\alpha_4/(\alpha_2(1+\alpha_1)(\alpha_4+\alpha_5)) \qquad (4.9a)$$

$$a_{2D} = \alpha_1\alpha_3\alpha_5\alpha_6/(\alpha_2\alpha_8(1+\alpha_1)(\alpha_4+\alpha_5)) \qquad (4.9b)$$

It can be easily seen that

$$da_{1D} = \sum_i \alpha_i \frac{\delta a_{1D}}{\delta \alpha_i}\frac{d\alpha_i}{\alpha_i} \quad \text{and} \quad da_{2D} = \sum_i \alpha_1 \frac{\delta a_{2D}}{\delta \alpha_i}\frac{d\alpha_i}{\alpha_i}$$

where the α_is are to be inserted from the defining eqns. 4.9(a)-(b). Since the capacitance ratio accuracy in MOS technology can be easily controlled, one can assume that $(d\alpha_i/\alpha_i)$s are all equal for the various α_is. Taking this value to be $d\alpha/\alpha$, one has $da_{1D} = [a_{1D}/(1+\alpha_1)]\frac{d\alpha}{\alpha}$ and $da_{2D} = [a_{2D}/(1+\alpha_1)]\frac{d\alpha}{\alpha}$. On noting that $a_{1D} = 2Q_p(1-Q_p^2)/[Q_p(1+Q_p^2)+Q_p]$, $a_{2D} = [Q_p(1+Q_p^2)-Q_p]/[Q_p(1+Q_p^2)+Q_p]$ and $h_D = 1/(1+\alpha_1)$, one has finally:

$$\frac{dQ_p}{Q_p} = h_D \frac{2Q_p(1-Q_p^2)Q_p^2}{Q_p^2[Q_p(1+Q_p^2)+Q_p]^3}\frac{d\alpha}{\alpha} \qquad (4.10a)$$

$$\frac{dQ_p}{Q_p} = h_D \frac{[Q_p(1+Q_p^2)-Q_p][Q_p(1+Q_p^2)+3Q_p]}{2Q_p[Q_p(1+Q_p^2)+Q_p]}\frac{d\alpha}{\alpha} \qquad (4.10b)$$

Since h_D depends on the type of the filter, to proceed further, consider a specific case, viz., a bandpass filter (BPF) with $h_A = 1$. Then $h_D = \Omega_p/[Q_p(1+\Omega_p^2)+\Omega_p]$ and the SC-BPF shall have a very low sensitivity in Ω_p and Q_p if

$$-1 < \frac{2\Omega_p^3(1-\Omega_p^2)}{Q_p[Q_p(1+\Omega_p^2)+\Omega_p]^4} < 1 \qquad (4.11a)$$

and if $-1 < \frac{1}{2} \frac{[Q_p(1+\Omega_p^2)-\Omega_p][Q_p(1+\Omega_p^2)+3\Omega_p]}{[Q_p(1+\Omega_p^2)+\Omega_p]^2} < 1$

Since $\Omega_p < 1$ (for a_{1D} and hence the capacitance ratios to have positive values only), one has from eqn. (4.11a) (the left hand inequality being trivially satisfied),

$$\frac{2\Omega_p^3}{(1+\Omega_p^2)^4} < Q_p^5$$

where we have ignored Ω_p^5 with respect to Ω_p^3 and Ω_p with respect to $Q_p(1+\Omega_p^2)$. The inequalities in eqn. (11b) leads to (the right had inequality being trivially true),

$$\frac{\Omega_p^2}{[Q_p(1+\Omega_p^2)+\Omega_p]^2} < \frac{3}{4}$$

$$\text{i.e.} \quad \frac{\Omega_p}{1+\Omega_p^2} < \frac{\sqrt{3}}{2} Q_p \qquad (4.12b)$$

One can plot the functions $f_1 = [2\Omega_p^3/(1+\Omega_p^2)^4]^{1/5}$ and $f_2 = \frac{2}{\sqrt{3}} [\Omega_p/(1+\Omega_p^2)]$ which would give the lower limits Q_{ℓ_1} and Q_{ℓ_2} for the realizable Q_p values with respect to assumed values of f_s/f_p (which

decides ϱ_p). Accordingly, for a specified Q_p, one can choose the necessary f_s/f_p so that the inequalities are satisfied (i.e., $Q_p > Q_{\ell_1}$ and $Q_p > Q_{\ell_2}$) whence the low sensitivity feature of the designed filter shall be maintained. A similar analysis can be made for other filter types.

4.3. CONSIDERATIONS FOR THE PARASITIC CAPACITANCES

As in the realizations presented in the previous chapter, the input node of a UGA being not at the virtual ground potential, the parasitic capacitances that get lumped at this node together with the network capacitances (C_1,C_2 ... in Fig. 4.2) can substantially alter the network response from the desired one. The terminals of the network capacitances can be arranged such that the bottom plates of the capacitors are either at ground or are switched between the ground and a voltage source (or the output of the UGA) or between a voltage source and the output of the UGA. Consequently, their effects on the transfer function can be eliminated. However, the parasitics associated with the top plates of the capacitors contribute to the CCEs such as in Eqn. 4.1. These parasitics are primarily due to the switches and interconnections in the SC network[25]. Numbering the various switches and the nodes and writing $CPX_{i,j}$ for the parasitic capacitance between node j and ground due to switch X_i, one can represent the network of Fig. 4.1(a) as in Fig. 4.3(a). In this one has $C_{p1} = CPS_{2,2} + CPS_{4,2}$, $C_{p2} = CPS_{6,4} + CPS_{7,4}$, $C_{p3} = CPS_{10,6} + CPS_{11,6}$, $C_{p4} = CPS_{13,8} + CPS_{14,8}$, $C_{p5} = CPS_{15,9} + CPS_{16,9}$, $C_{p6} = C_A + CPS_{2,7} + CPS_{7,7} + CPS_{13,7} + CPS_{14,7}$ and C_A is the input capacitance of the UGA. Note that in Fig. 4.3(a)

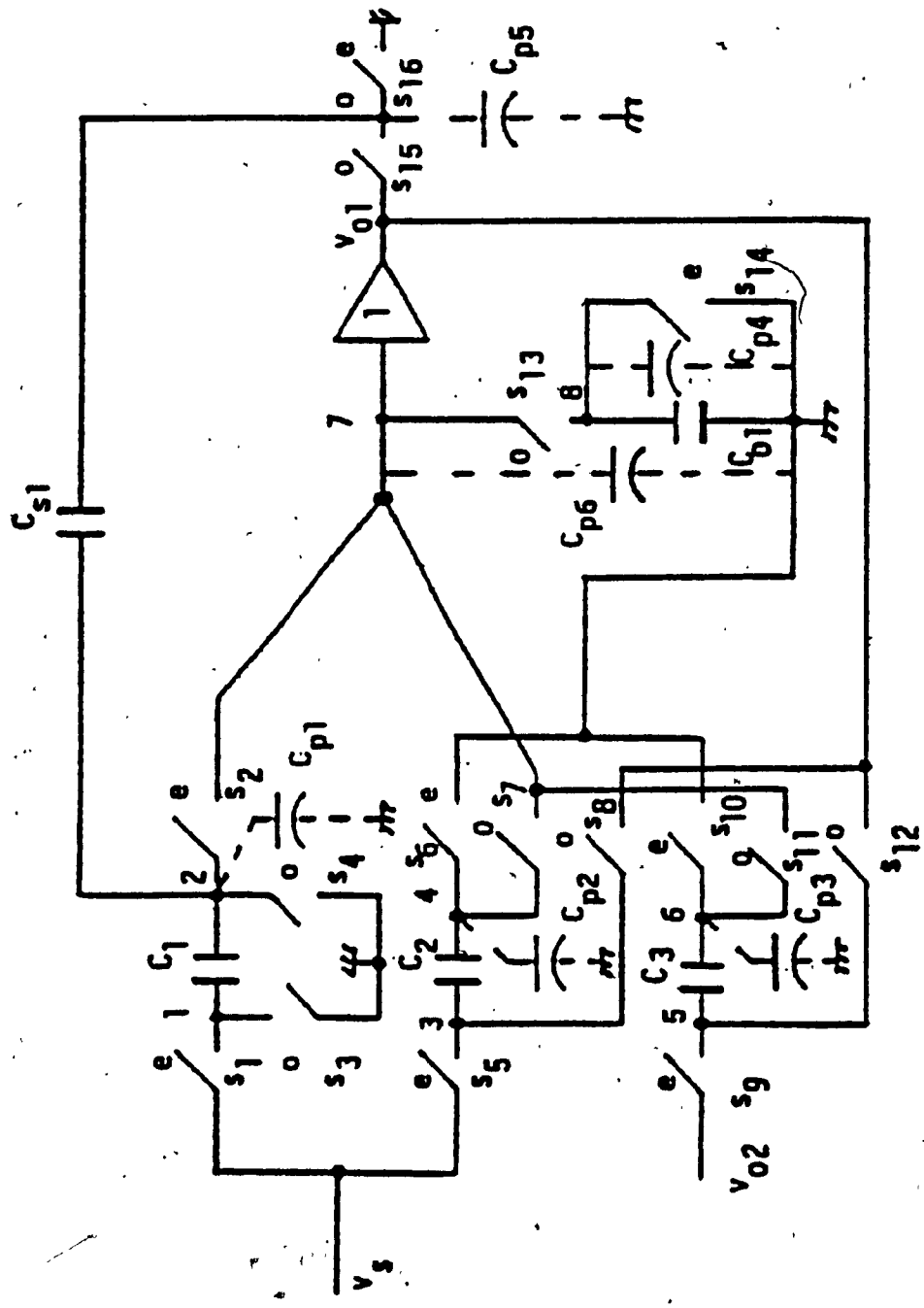


Figure 4.3: (a) Top plate parasitic capacitances associated with the CDA network

only the parasitics that contribute to charge flow into the input node x_1 of the UGA are shown. The parasitics associated with the bottom plates of the capacitors (shown by thick lines) do not influence the CCE and, hence, are not shown. It may be noted that C_{p6} had the contribution from the largest number of parasitic capacitances. This represents the most pessimistic case. It is possible, in specific cases, to combine a number of switches into a single switch, thereby reducing the contribution of the parasitic components to C_{p6}. One such alternative is shown in the network of Fig. 4.3(b) where is is required that the coefficients A_2, A_3 (eqn. 4.4) have positive values only. One can easily see that now $C_{p6} = C_A + CPS_{2,6} + CPS_{7,6}$, $C_{p1} = CPS_{2,2} + CPS_{4,2}$ while C_{p2}, C_{p3}, C_{p4} merge into a single parasitic component $C_p^* = CPS_{6,4} + CPS_{7,4}$ and $C_{p5} = CPS_{10,7} + CPS_{11,7}$. Returning to Fig. 4.3(a) and writing down the CCEs one obtains

$$[(1+\varepsilon_1)(1+\varepsilon_2)+\varepsilon_3(1-\varepsilon_4)z^{-1}]V_{o1}^e$$

$$= A_1(1+\varepsilon_2)V_s^e+A_2(1-\varepsilon_4)z^{-1}V_s^e+A_3(1-\varepsilon_4)z^{-1}V_{o2}^e \qquad (4.13a)$$

where the terms ε_1, ε_2, ε_3 and ε_4 are:

$$\varepsilon_1 = (C_{p1}+C_{p5}+C_{p6})/(C_1+C_{s1}),\ \varepsilon_2 = (C_{p2}+C_{p3}+C_{p4}+C_{p6})/C_{o1}$$

$$\varepsilon_3 = (C_{p6}C_{s1})/(C_{o1}(C_1+C_{s1})),\ \varepsilon_4 = C_{p6}/C_{s1} \qquad (4.13b)$$

One can now write

$$V_{o1}^e = \tilde{A}_1 V_s^e + \tilde{A}_2 z^{-1} V_s^e + \tilde{A}_3 z^{-1} V_{o2}^e \qquad (4.14)$$

which is of the form of eqn. (4.4a) and where now the coefficients $\tilde{A}_1$, $\tilde{A}_2$, $\tilde{A}_3$ contain the contributions due to the parasitic components as

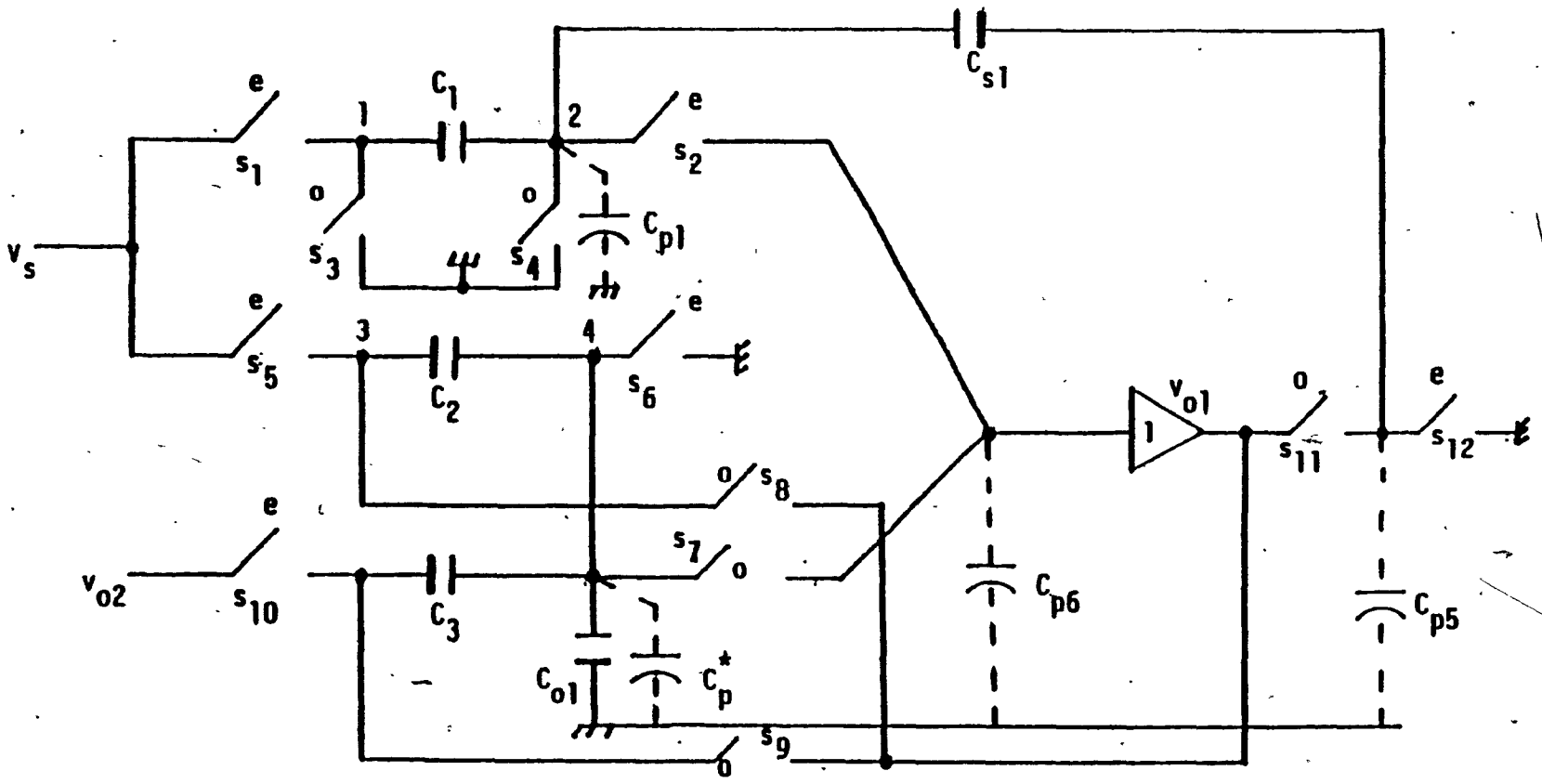


Figure 4.3 : (b) A CDA network topology with reduced contributions from top plate parasitic capacitances than that in Fig. 4.3(a)

follows:

$$\tilde{A}_1 = A_1(1+\varepsilon_2)/D_{11},\ \tilde{A}_2 = A_2(1-\varepsilon_4)/D_{11},\ \tilde{A}_3 = A_3(1-\varepsilon_4)/D_{11}$$

And $D_{11} = (1+\varepsilon_1)(1+\varepsilon_2)+\varepsilon_3(1-\varepsilon_4)z^{-1}$. A similar derivation can be carried out with regard to the network around the second UGA [Fig. 4.3(c)] and one gets:

$$V_{oe}^2 = \tilde{B}_1 V_{o1}^e - \tilde{B}_2 z^{-1} V_{o1}^e + \tilde{B}_3 z^{-1} V_s^e \qquad (41.5a)$$

where $\tilde{B}_1 = B_1(1+\varepsilon_6)/D_{22}$, $\tilde{B}_2 = B_2(1-\varepsilon_8)(1+\varepsilon_9)/D_{22}$, $B_3 = \tilde{B}_3(1-\varepsilon_8)/D_{22}$, $D_{22} = (1+\varepsilon_5)(1+\varepsilon_6) + \varepsilon_7(1-\varepsilon_8)z^{-1}$ and ε_5, ε_6, ε_7, ε_8, ε_9 are given below:

$$\varepsilon_5 = (C_{p7}+C_{p11}+C_{p12})/(C_4+C_{s2})$$
$$\varepsilon_6 = (C_{p8}+C_{p9}+C_{p10}+C_{p12})/C_{o2}$$
$$\varepsilon_7 = C_{p12}C_{s2}/(C_{o1}(C_4+C_{s2})),$$
$$\varepsilon_8 = C_{p12}/C_{s2},$$
$$\varepsilon_9 = C_{p8}/C_5$$

On carefully studying the differences between the coefficients sets A_1, A_2, ...B_3 and $\tilde{A}_1$, $\tilde{A}_2$, ...$\tilde{B}_3$, one finds that the response of the network will be very close to the nominal response (i.e., in absence of parasitics) if the network capacitors C_{o1}, C_{o2} are chosen very large relative to the parasitic components and also if the sum C_1+C_{s1} and C_1+C_{s2} are large compared to the parasitic components. This observation leads to a useful guideline as described in the next section.

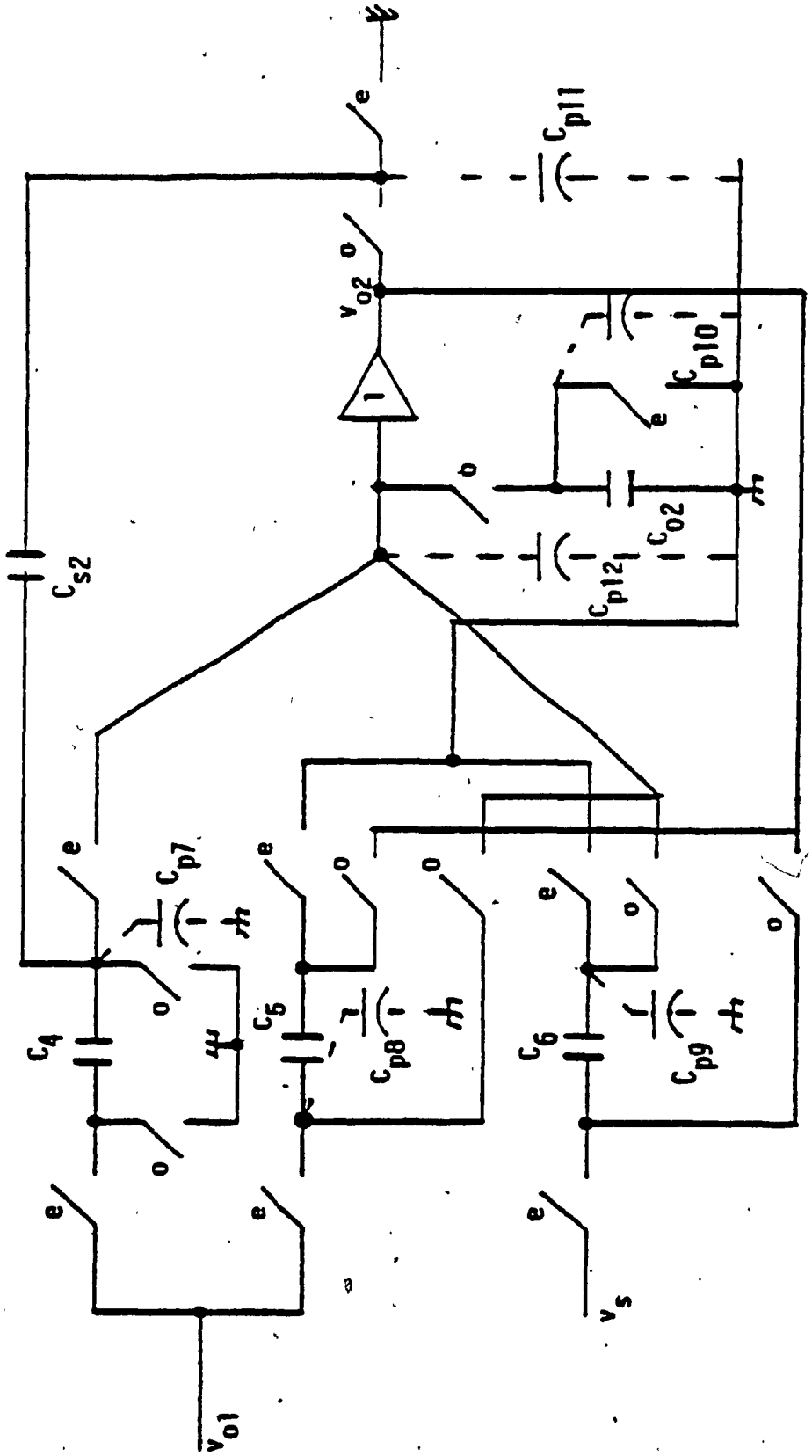


Figure 4.3 : (c) Top plate parasitic capacitances associated with the network around the second UGA of the BIQ-SDTF

4.4 PARASITIC TOLERANT DESIGN OF THE BIQ-SDTF WITH MINIMUM TOTAL CAPACITANCE

As noted above, the transfer function of the BIQ-SDTF, including the effects of the parasitics, is:

$$\frac{V_{o1}^{e}}{V_{s}^{e}} = \frac{\tilde{A}_1+\tilde{A}_2 z^{-1} + \tilde{A}_3\tilde{B}_3 z^{-2}}{1-\tilde{A}_3\tilde{B}_1 z^{-1} + \tilde{A}_3\tilde{B}_3 z^{-2}} = T(z) \qquad (4.16)$$

To minimize the error between T(z) and the given analog filter response T(s) one can employ an optimization algorithm. Towards this, let $C_{o1} = C_{o2} = F_1$ and $C_1+C_{s1} = F_2 = C_4+C_{s2}$. The values of F_1, F_2 should be technologically feasible. Thus one may set $F_1 \approx 90$ pF, $F_2 =$ 100 pf as initial values in the algorithm. Some important considerations now follow. It is recalled that the network capacitances must satisfy the basic constraints that exist between the nominal coefficient set $A_1, A_2, \ldots B_1, \ldots B_3$ and the coefficients of the BIQ-SDTF after bilinear transformation of the prototype analog filter. Thus, keeping $C_{o1}=C_{o2}=F_1$ and $C_1+C_{s1}=C_4+C_{s2}=F_2$, might cause the maximum capacitance in the circuit to exceed the maximum feasible technological value (~100pF) or the minimum capacitance in the circuit may assume a value smaller than the minimum achievable value (~0.5pf) of MOS capacitors at the present time. Again, assigning F_1, F_2 the values almost near the upper limit (~100pF) would make the total capacitance value in the circuit quite large, requiring a large substrate area. Thus, it is desirable that a scheme that yields a minimum total capacitance circuit is associated with the optimization algorithm. It may be noted that in the BIQ-SDTF proposed above there is an extra

degree of freedom with respect to the coefficients - the six coefficients $A_1, A_2, A_3, B_1, B_2, B_3$ are combined to yield the five coefficients $h_D, a_{1N}, a_{2N}, a_{1D}, a_{2D}$ of the nominal BIQ-SDTF. It may also be noted that since $A_1 = h_d$, $A_2 = h_D a_{1N}$, $A_3B_3 = h_D a_{2N}$, $A_3B_1 = a_{1D}$, $A_3B_2 = a_{2D}$, the coefficient A_3 would be the most convenient choice to arrive at minimum total capacitance design. One can set $A_3 = ma_{1D}$ where $m > 1$ (so that $B_1 = C_4/(C_4+C_{s2})$ is < 1) and letting $C_1+C_{s1} = F_1$ (constant) = C_4+C_{s2} and $C_{o1} = C_{o2} = F_2$ (constant), one can minimize the sum $C_1+C_{s1}+C_{o1}+C_2+C_3+C_4+C_{s2}+C_{o2}+C_5+C_6$ with respect to m, obtaining the optimum value for m as:

$$m_o = 1 + \sqrt{(1-h_D)(h_D+a_{2D})}/a_{1D} \tag{4.17}$$

which can be easily computed. The opimum 'm' puts the restriction that $h_D < 1$ which translates down to a restriction on the flat gain of the prototype analog filter. If in any specific case h_D appears as > 1, the flat gain of the analog filter (h_A) has to be scaled down. Extensive numerical simulation has revealed that the above restriction is always satisfied if one maintains $h_A = 1$, especially for low pass and high pass filters. The nominal design capacitors now assume the values:

$$C_1 = h_D F_1 \quad , \quad C_{s1} = (1-h_D)\, F_1$$

$$C_{o1} = F_2 \quad , \quad C_2 = \frac{h_D\, |a_{1N}|}{1-h_D} F_2 \tag{4.18}$$

$$C_3 = \frac{m_o a_{1D} F_2}{1-h_D} \quad , \quad C_4 = F_1 B_1 \quad , \quad C_{s2} = (1-B_1)F_1$$

$$C_{o2} = F_2$$

$$C_5 = \frac{a_{2D}}{a_{1D}(m_o-1)} F_2 \quad , \quad C_6 = \frac{h_D}{a_{1D}(m_o-1)} F_2 \qquad (4.18)$$

Since one has chosen F_2 at about the maximum feasible limit for the technology, one must now carefully consider the ratios $R_1 = \frac{h_D|a_{1n}|}{1-h_D}$, $R_2 = \frac{m_o a_{1D}}{1-h_D}$, $R_3 = \frac{a_{2D}}{a_{1D}(m_o-1)}$ and $R_4 = \frac{h_D}{a_{1D}(m_o-1)}$. If all of these quantities are less than 1, eqn. (4.18) can be applied to yield the various network capacitors. If, however, any one (or more) of these four quantities (R_1, R_2, R_3, R_4) assume a value greater than 1, the capacitor C_{o1} and (or) C_{o2} have (has) to be scaled down by the corresponding factor, thereby ensuring that the highest valued capacitor in the circuit does not exceed the technologically feasible limit (100pF). The design obtained from the above procedure yields a network that satisfies the given error limit and has a minimum total capacitance relative to a specific choice for F_1 and F_2. If the error value yielded by the optimization routine appears less than the prescribed limit, one can subject the network to few more iterative optimizations with successively smaller values for F_1 and F_2. The iterations are terminated either (i) when the prescribed error limit is reached (or exceeded) or (ii) when the minimum capacitance of the network equals (or becomes less) the minimum technologically feasible limit. An algorithm with the above considerations is summarized in Table 4.2.

TABLE 4.2

[OPTIMIZATION ALGORITHM FOR PARASITIC TOLERANT DESIGN]

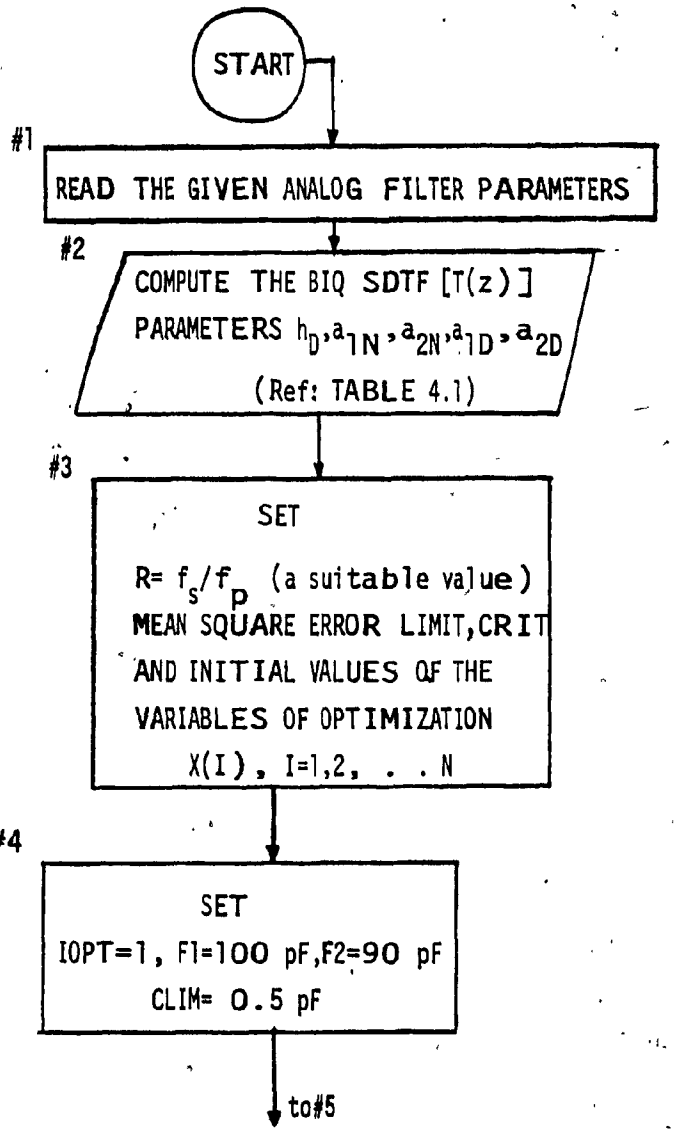
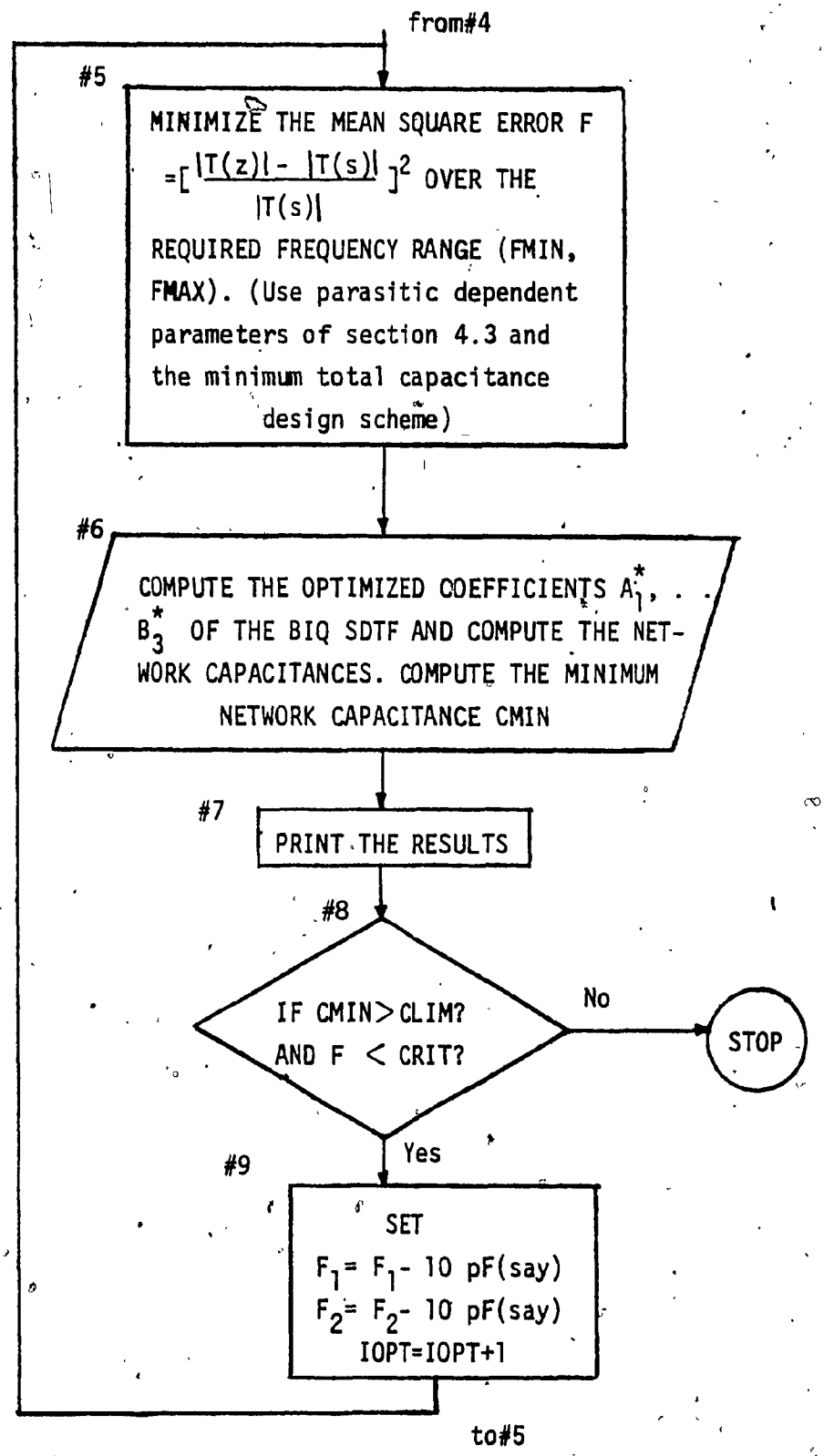


TABLE 4.2 [Cont'd.]



4.5 CONSIDERATIONS FOR THE OFFSET VOLTAGE IN THE UGAs

In the analysis of section 4.2.1, one assumed $v_{o1} = v_{x1}$ and $v_{o2} = v_{x2}$. In a practical UGA, this is not true because of the DC offset voltage v_{os} that exists between the input and output terminals of the UGA. Considering the offset voltage of the UGA, we have an equivalent block shown in Fig. 4.4. This gives, $v_{o1} = v_{x1} + v_{os}$ and $v_{o2} = v_{x2} + v_{os}$. Introducing the above modifications in our previous analysis, one obtains (ref. eqn 4.4):

$$V_{o1}^e = A_1 V_s^e - A_2 z^{-1} V_s^e + A_3 z^{-1} V_{o2}^e + C_{11} V_{os1} \qquad (4.19a)$$

and $$V_{o2}^e = B_1 V_{o1}^e - B_2 z^{-1} V_{o1}^e + B_3 z^{-1} V_s^e + C_{22} V_{os2} \qquad (4.19b)$$

where v_{os1}, v_{os2} [$V_{os1} = \mathcal{Z}\{v_{os1}(n)\}$, $V_{os2} = \mathcal{Z}\{v_{os2}(n)\}$] represent the offset voltage components in UGA1 and UGA2, respectively, and

$$C_{11} = 1 - (1 - A_1 + A_2 + A_3)\, z^{-1/2} \qquad (4.20a)$$

$$C_{22} = 1 - (1 - B_1 + B_2 + B_3)\, z^{-1/2} \qquad (4.20b)$$

From eqn. 4.19(a)-(b), one can obtain (assuming $V_{os1} = V_{os2} = V_{os}$)

$$\frac{V_{o1}^e}{V_s^e} = T_R(z) = T(z) + T_{os}(z) \qquad (4.21)$$

where

$$T(z) = (A_1 + A_2 z^{-1} + A_3 B_3 z^{-2}) / (1 - A_3 B_1 z^{-1} + A_3 B_2 z^{-2}) \qquad (4.22a)$$

and

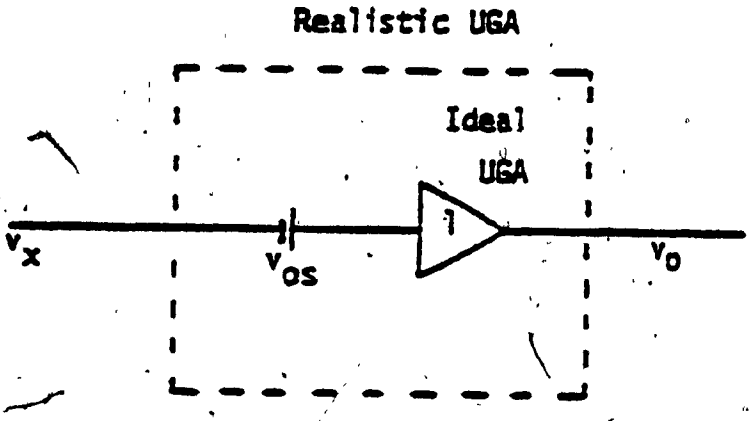


Figure 4.4: A model for the UGA with an offset voltage v_{os}

$$T_{os}(z) = [(A_3C_{22}z^{-1}+C_{11})/(1-A_3B_1z^{-1}+A_3B_2z^{-2})]\ \frac{V_{os}}{V_s^e} \qquad (4.22b)$$

Clearly, $T(z)$ in eqn. (4.22a) represents the desired response while $T_{os}(z)$ is the perturbation component in the realized response $T_R(z)$. In order that $|T_R(z)|$ approximate the desired amplitude response $|T(z)|$, one has to arrange $|T(z)| >> |T_{os}(z)|$. This leads to

$$\left| \frac{V_s^e}{V_{os}} \right| >> | (A_3C_{22}z^{-1} + C_{11})/(A_1+A_2z^{-1} + A_3B_3z^{-2})| \qquad (4.23)$$

If $r_{max} = \max \left| \frac{A_3 C_{22}z^{-1} + C_{11}}{A_1+A_2z^{-1} + A_3B_3z^{-2}} \right|$, over the frequency range of interest, applying an input signal level $|V_s| \geq r_{max}.|V_{os}|$ would accomplish $|T_R(z)| \simeq |T(z)|$. This can be done in practice provided sufficient signal level is available at the input of the SCF and where obtaining a wide dynamic range of operation is not of importance. Numerical simulations reveal that r_{max} increases roughly in proportion to the Q_p of the circuit and decreases in proportion to the gain coefficient h_D (related to the flat gain h_A of the corresponding analog filters) of the BIQ-SDTF. Thus, wherever practical, the SCF can be designed for a higher h_A value than specified, to combat the perturbing effect of the offset voltage on the realized amplitude response.

While the above guidelines would aid making $|T_R(z)| \simeq |T(z)|$, they do not provide exact solution. Moreover, these procedures may not be feasible in some cases, especially where the filter has to work from a low level input signal (the front end of a receiving communication

circuit, for example). The formulations in eqns. 4.20, 4.22 reveal that exact compensation for the effect of non zero v_{os} is not possible in the proposed circuit because of the delayed component of v_{os} in the coefficients C_{11},C_{22} [see eqn. 4.20(a)-(b)]. In cases (especially for high Q_p circuits) where the quantity r_{max} may become rather large, a more acceptable solution could be obtained by minimizing the error between the amplitude responses represented by the net transfer function $T_R(z)$ in presence of non zero v_{os} and that represented by the nominal transfer function $T(s)$, on assuming an acceptable value of r_{max}, for each design. An interactive optimization could be carried out for successively smaller values of r_{max} until the error between the nominal and the actual amplitude responses increases beyond the specified limit or the circuit capacitances fall beyond practical limits. This procedure can be applied together with the method for obtaining a parasitic tolerant design, as discussed earlier. This is elaborated further in section 4.7.

4.6 SCF BIQUADS BILINEARLY EQUIVALENT TO THE ANALOG BIQUADS AND REQUIRING A MINIMAL SET OF CAPACITANCES

It has been pointed out in Chapter 1 that most of the canonic SCF biquad structures proposed by other workers [15],[41],[26],[27] fail to simulate the bilinear $s \leftrightarrow z$ transformed biquadratic transfer function from their analog counterparts. An SCF, based on UGAs, is shown in Fig. 4.5, which can simulate a general BIQ-SDTF. As will be seen, this network can be bilinearly equivalent to its analog counterpart, except for the notch filter. The SCF uses at most six

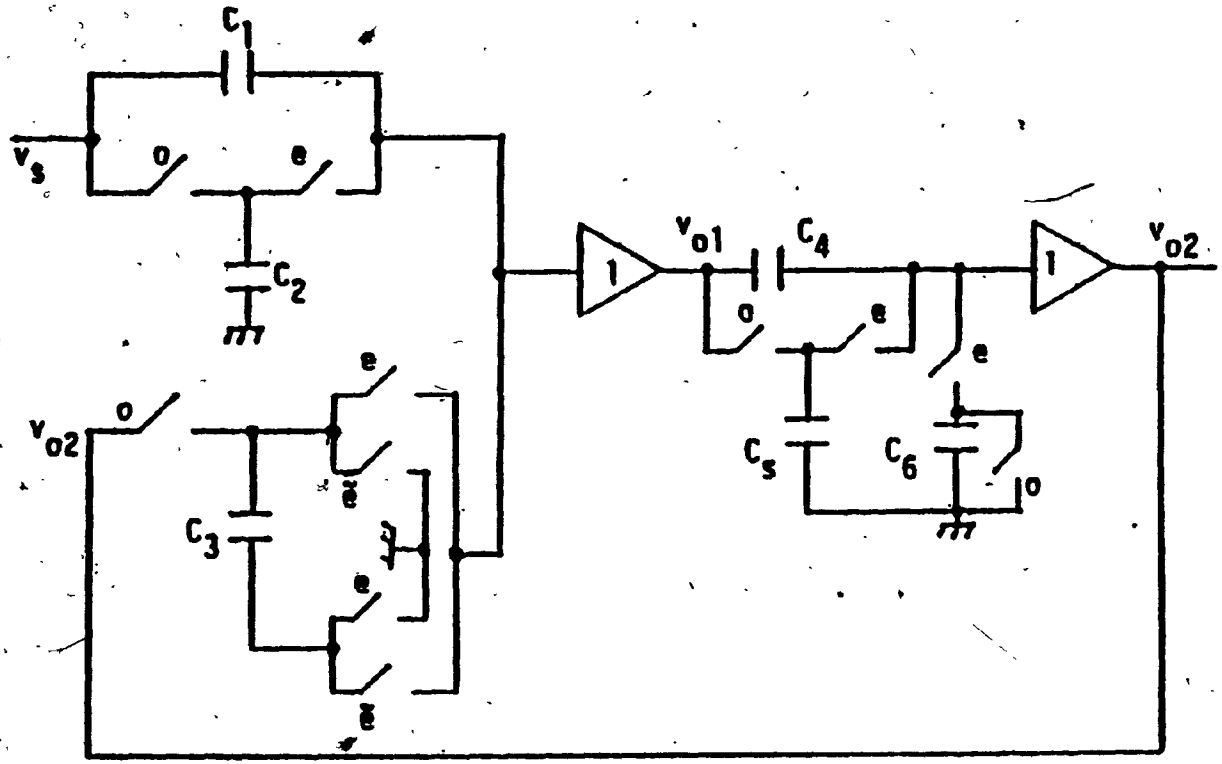


Figure 4.5: The alternative BIQ-SDTF topology requiring minimal set of capacitors

capacitors as compared with ten capacitors required in the circuit presented in section 4.2.1. The circuit of Fig. 4.5 needs to be preceeded by a sample and hold circuit to achieve the input condition $V_s^o = z^{-1/2}V_s^e$. Routine analysis yields:

$$\frac{V_{o2}^e}{V_s^e} = \frac{a_1 b_1[1+(m+n-2)z^{-1} + (m-1)(n-1)z^{-2}]}{1 - (a_1+b_1+a_2b_1)z^{-1} + \{a_1b_1 \mp a_2b_1(n-1)\}z^{-2}} \qquad (4.24)$$

where $a_1 = C_1/(C_1+C_2+C_3)$, $a_2 = C_3/(C_1+C_2+C_3)$, $b_1 = C_1/(C_4+C_5+C_6)$, $m = C_2/C_1$, $n = C_5/C_4$.

In eqn. (4.24), the $\mp$ sign in the deonominator is to take care of the reversal of the terminals of the capacitor C_3. The positive sign is taken when the top terminal of C_3 is grounded during the 'even' switching phase (designated by 'e') and the negative sign applies when the bottom terminal of C_3 is grounded during the 'even' phase (designated by '$\tilde{e}$'). The bottom terminal of C_3 is grounded for the realization of high pass (HP) and bandpass (BP) filters while the top terminal of C_3 is to be grounded for realization of the low pass (LP) filter. For eqn. (4.24) to represent a BIQ-SDTF bilinearly equivalent to LP, HP and BP biquadratic analog transfer functions, one would need the pair (m,n) to have the values m = n, n = 2 for LP; m = 0, n = 0 for HP; m = 2, n = 0 for BP. Further, $a_1+b_1+a_2b_1 = a_{1D}$, $a_1b_1+a_2b_1 = a_{2D}$ and $a_1b_1 = h_D$. Since there are two independent capacitance ratios a_1 (or a_2) and b_1 while three filter parameters ω_p, Q_p and h_A, the condition $a_1b_1 = h_D$ often has to be relaxed (amounting to scaling of the flat gain of the filter as mentioned before) to realize the specified f_p and Q_p. Further, for the HP case, one encounters an

additional restriction, viz., $Q_p\omega_p < f_s$, limiting the realizations to low Q_p and low f_p (relative to f_s) values only. It may be seen that, for the HP case, the network of Fig. 4.5 is identical with the network reported in [27]. If bilinear equivalence is not required, the network of Fig. 4.5 can be reduced to have only four capacitors as used in other canonic designs [15],[41],[26],[27]. It may also be noted that the given network will not realize a notch SC filter bilinearly equivalent to the analog notch filter transfer runction.

The analysis for parasitic capacitances and the effect of the offset voltages in the UGAs can be studied for the network of Fig. 4.5 in a manner similar to that discussed earlier and is omitted here.

4.7 NUMERICAL AND EXPERIMENTAL RESULTS

4.7.1 Results of Numerical Simulations

The optimization algorithm discussed above has been tested extensively for SCF biquads (Fig. 4.2) with Q_p = 5,10,15,20,25 and f_s/f_p = 5,7,10,15. Only moderate to low values of f_s/f_p were used since the application of bilinear transformation together with UGA based designs should be attractive especially for high (pole) frequency of operation (lower f_s/f_p). Some results for a bandpass filter (SC-BPF) are presented. Fig. 4.6 shows the SC-BPF. Fig. 4.7 shows the nominal response [curve (a)] and the actual response [curve (b)] that would be obtained in the presence of the parasitic capacitances, for a BPF with Q_p = 10, f_s/f_p = 10 f_s = 10 kHz and h_A = 5. In the present

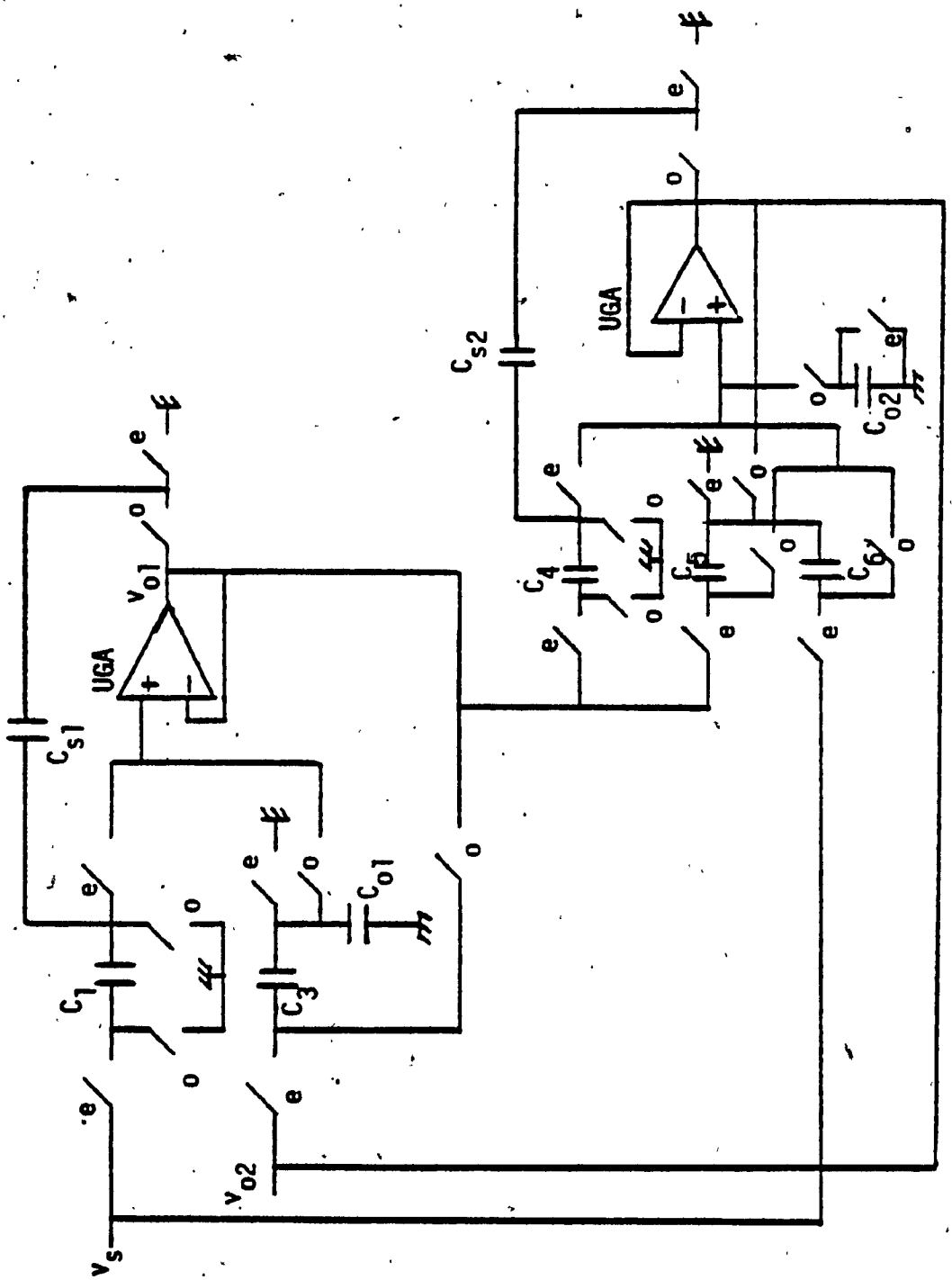


Figure 4.6: The bandpass SCF used for experimental investigation

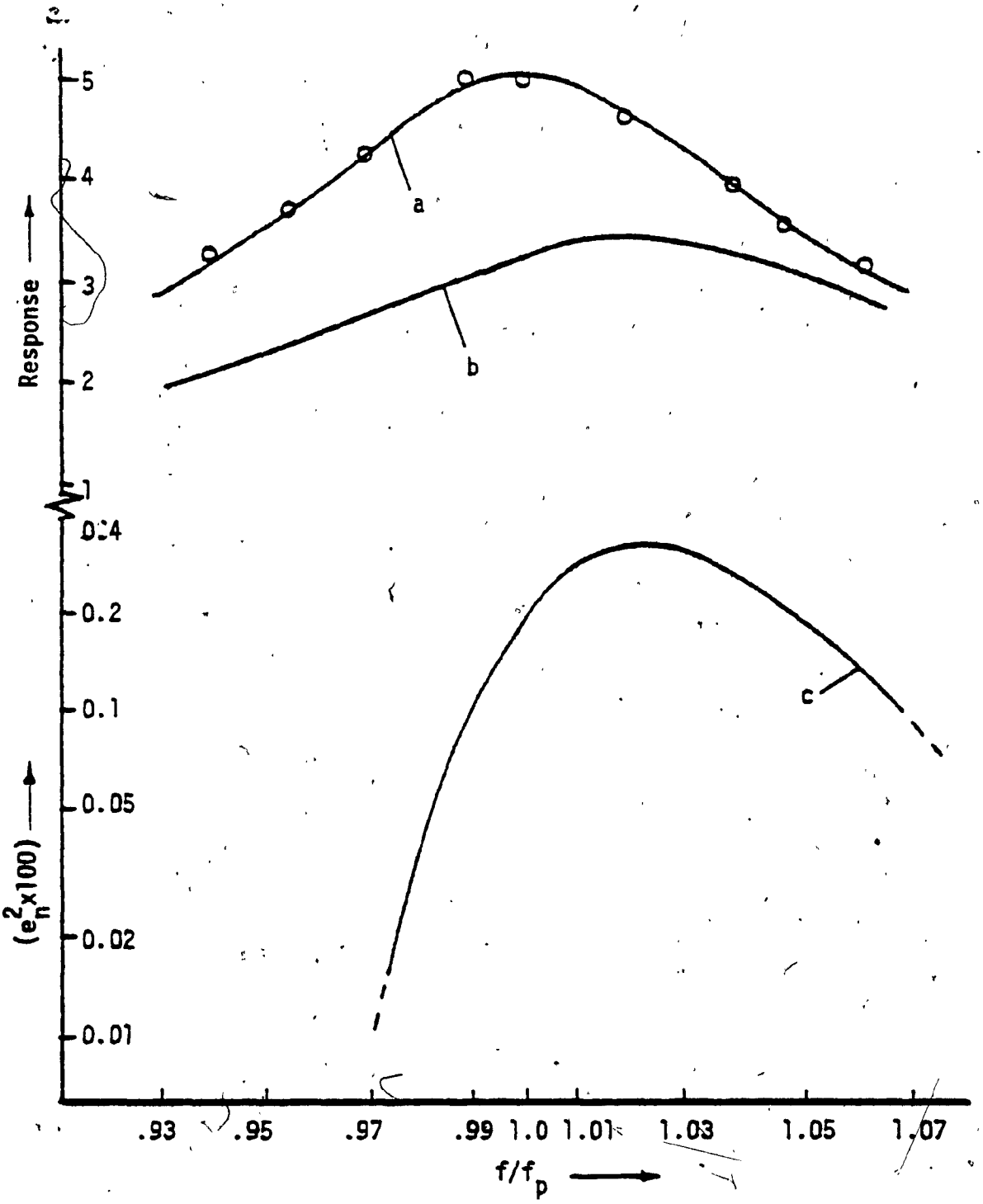


Figure 4.7: (a) The ideal (solid line) and the experimental (with optimal set of capacitors) responses of the SC BPF,
(b) Response without optimization for parasitic tolerant design,
(c) Normalized mean square error between the ideal and the optimized responses

day state-of-the-art, processes have been evolved which lead to MOS circuits with very low parasitic capacitances[19]. Also, the parasitic capacitances can often be estimated accurately [e.g., in self-aligned silicon gate (SAG) process][17],[18]. The parasitic component at the top plate of the MOS capacitors can be neglected, the parasitic components from each node of the MOS switch to ground could be between 10fF to 20fF (1fF = 10^{-15} Farad)[7]. The input capacitance of the UGA would be of the same order as that of a MOS transitor. It may be slightly larger if the input MOS transistors are made large to realize a high DC gain and low noise amplifier. In unity gain buffers, the input capacitance can be reduced very much by bootstrapping[32]. In the numerical simulations, we have assumed all the $CPX_{i,j}$s as equal and equal to 20fF. The C_A has been taken as 40fF. Also, though not required in practice, the parasitic component at the top plate of each capacitor has been taken as 0.1% of the nominal capacitance to yield a worst case analysis. The optimized response was expected to have an rms error equal to or less than 5% over the frequency band $f_p \mp f_p/Q_p$. The frequency increment was chosen as $\sim 1/Q_p$ so that as Q_p is increased, the resolution of the numerical computation was also improved. This is necessary to avoid large errors with a coarse frequency increment for highly selective circuits. Considerations were also paid towards variations in the values of the parasitic components from those assumed for the optimization algorithm. If the parasitic capacitances in the actual fabrication process are less than the limits assumed in the analysis, the optimized set of capacitors should give the desired responses within the prescribed error limit. If, however, the parasitic components assume higher values, the design capacitances have

to be increased. Now the random errors in MOS capacitors due to area fluctuation and variation in the thickness of the dielectric (oxide layer) are expected to lie well below 1% of the nominal capacitance values[42]. While the ratio accuracy of MOS capacitors is likely to be 0.1% or better, the accuracy in the absolute values of the capacitors may be poorer. However, a value of 1% represents about the worst case. Since the parasitic capacitances are an integral part of the MOS circuit components, their variations should be of the same order of magnitude. Thus, a conservative design approach shall be to increase the optimized set of capacitors by a certain factor and use these values in practical design. Fig. 4.8 shows the maximum capacitance (C_{max}), the maximum capacitance spread (SMPX) and total capacitance (C_T) needed for a nominal design with f_p = 1kHz, f_s/f_p = 10, h_A = 5 and Q_p = 5,10,15,20,25. This is obtained using the minimum total capacitance design scheme and F_1 = 100pF, F_2 = 90pF. The curves in Fig. 4.8, designated by $\tilde{C}_{max}$, $\tilde{SPMX}$ and $\tilde{C}_T$ represent the quantities after considering the parasitic capacitances and subsequent optimization using a gradient method[37],[38]. A 2% post optimization increment in the network capacitances has also been allowed to take care of the possible variations in assumed values for the parasitic capacitances. The curve E_R represents the root mean square error (%) that could be achieved by optimization and after a 2% increment to the optimal set of network capacitors. The corresponding results for the iterative optimization, discussed in section 4.2.3 (also refer to Table 4.2, IOPT = 1,2,...) are shown by C^*_{max}, $SPMX^*$, C^*_T and E^*_r of Fig. 4.9 for the case with f_s/f_p = 10 and Q_p = 10, h_A = 5. These results reveal the feasibility of a set of practical network capacitances and

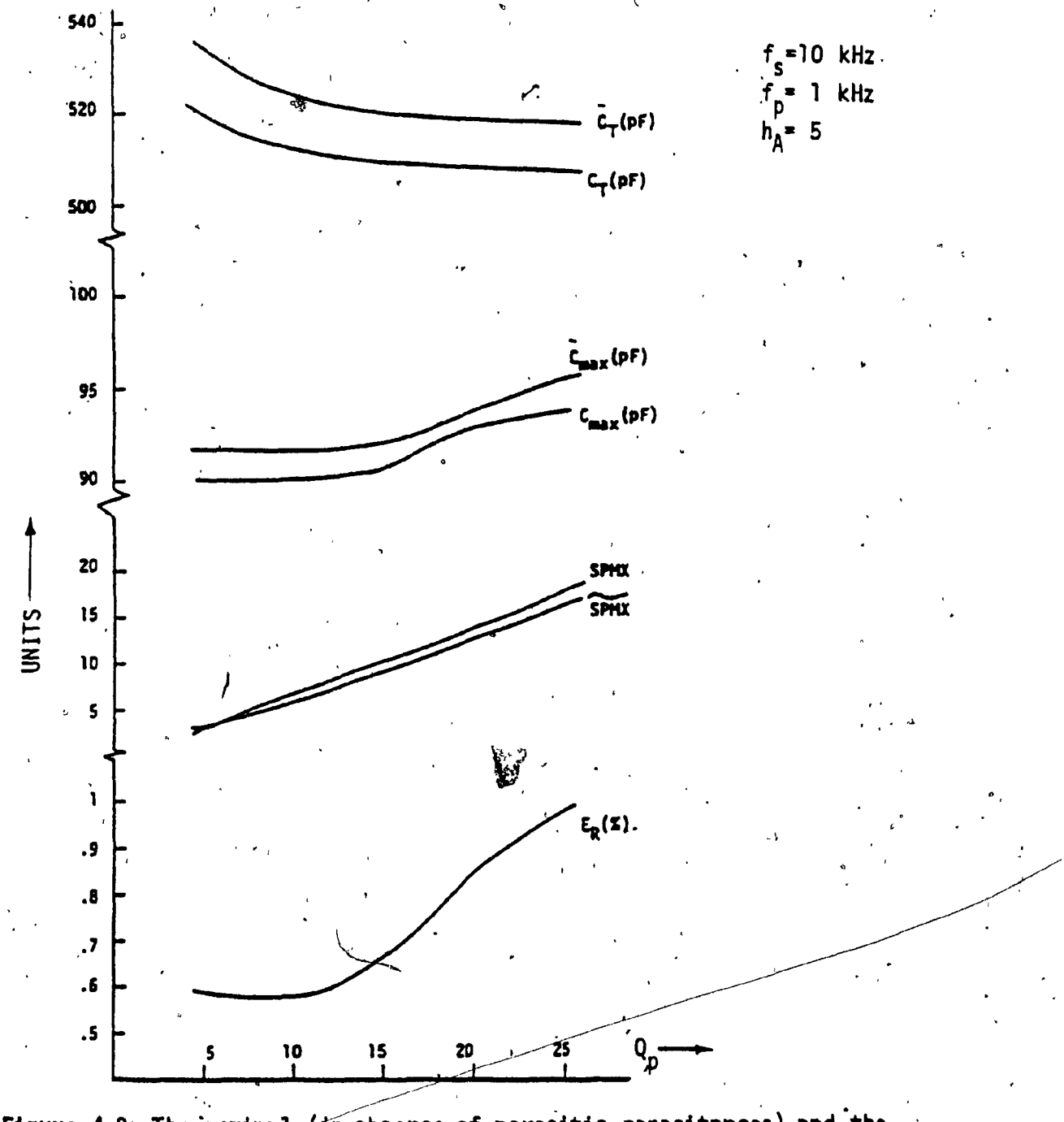


Figure 4.8: The nominal (in absence of parasitic capacitances) and the optimized values of total capacitance $C_T(\tilde{C}_T)$, maximum capacitance $C_{max}(\tilde{C}_{max})$, maximum capacitance spread SPMX($\widetilde{SPMX}$) and the % rms error for the SC-BPF as a function of Q_p

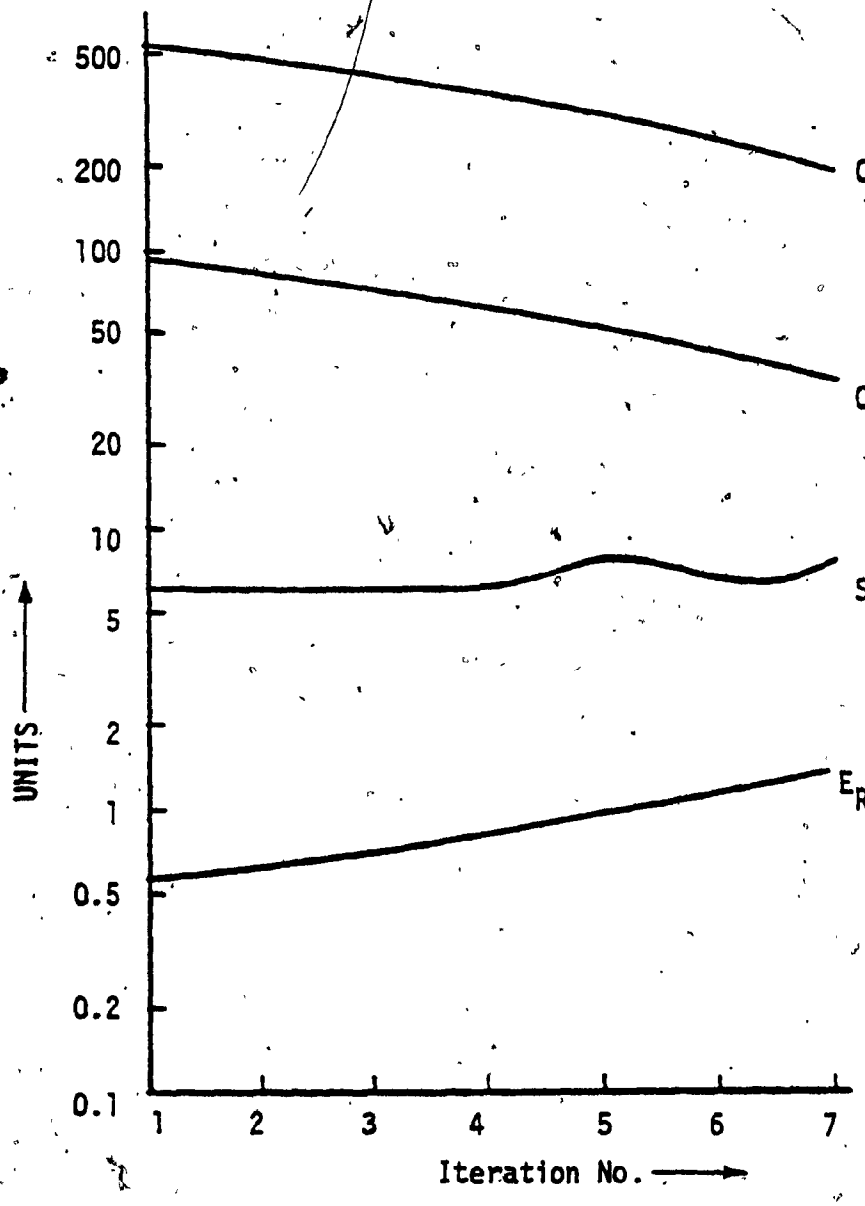


Figure 4.9: The total capacitance C_T^*, the maximum capacitance C_{max}^*, the maximum capacitance spread SPMX* and the % rms error E_R^* in the iterative optimization procedure

realizability of the design employing a small substrate area in an actual fabrication process. The optimized set of capacitors, obtained in each case were increased up to 5% and the results were found to be within the prescribed error limit and the capacitances were within the technologically feasible limits. Hence a design center could be established by making all the capacitors 2.5% higher than the values obtained after optimization. This set of capacitors will then preserve the desired response within the limits of the error criterion even though the parasitic capacitances could increase by 2.5%, from the values assumed during the stage of optimization, due to an accidental fault in the fabrication process. The optimized responses were very close to the desired ones and it would be difficult to distinguish between the pair of curves. Hence, the normalized square error ($e_n^2 \times 100$) is shown as curve (c) in Fig. 4.7. This corresponds to the case $h_A = 5$, $Q_p = 10$, $f_s/f_p = 10$ and the capacitance values correspond to the final stage of the iterative optimizations. Thus, this represents the result for a design that has the lowest total capacitance out of the various minimum total capacitance design corresponding to the various stages of iterative optimizations. Figure 4.10 shows the numerical result for the SC-BPF of Fig. 4.6 with the UGAs realized from OAs and the $v_{os} \neq 0$. The curve (a) and (b) represent the parameter r_{max} [ref. eqn. 4.23] for the cases $h_A = 1$ and 5 with $f_s/f_p = 10$ and $Q_p = 5,10,15,20,25$. The curve for $h_A = 1$ is always higher than that for $h_A = 5$. This indicates that the effect of v_{os} becomes worse (requiring higher level of input signal) for a smaller value of the flat gain h_A. Considering the case of $h_A = 5$ and $Q_p = 10$, it turns out that to obtain the desired response (Fig. 4.10a)

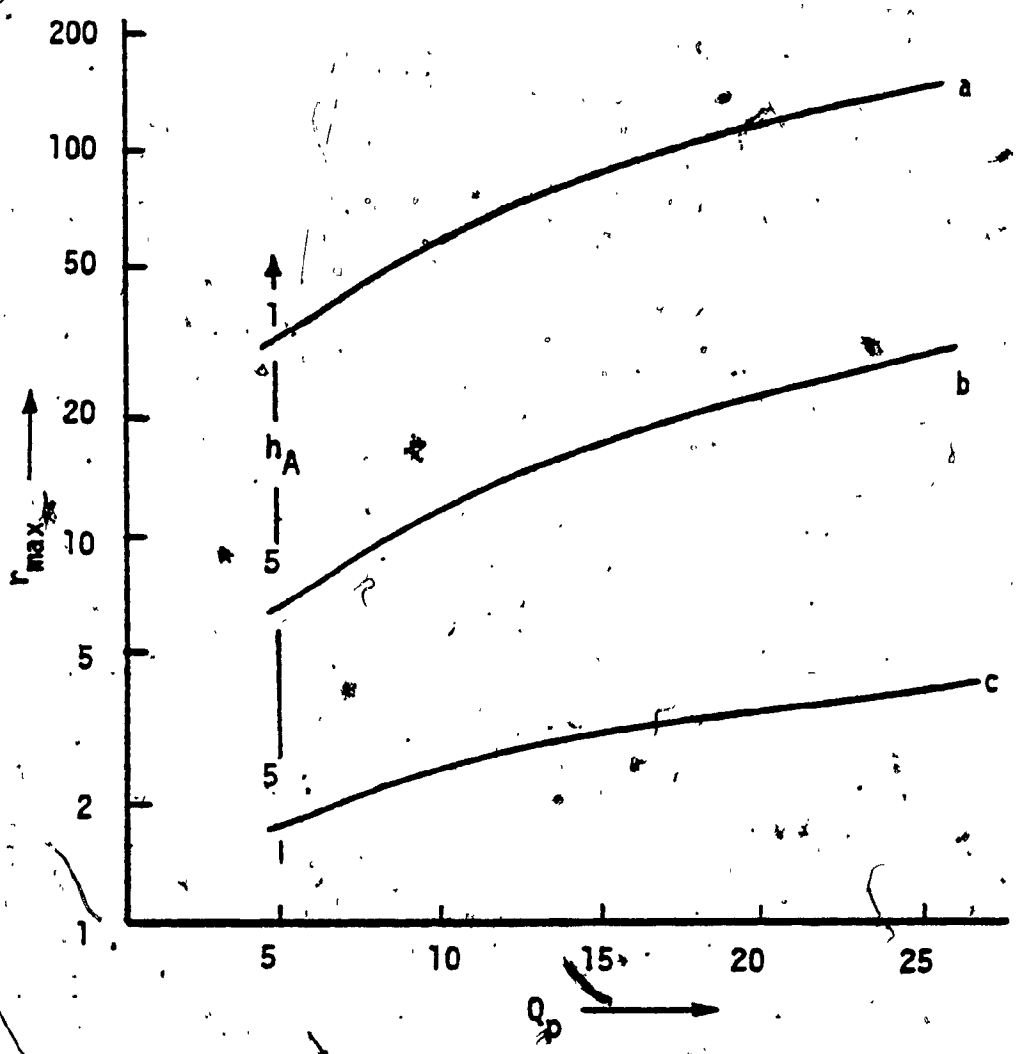


Figure 4.10: The parameter $r_{max} = [|V_s|/|V_{os}|]_{max}$ in the SC-BPF using UGAs with non zero v_{os} . (a),(b) are unoptimized, while (c) values when optimized for minimum error

within the 5% rms error, one needs $|v_s/v_{os}|$ ratio to be $\geq 5r_{max}$, viz., with $v_{os} = \pm 5$ mv one would require $|v_s| \geq 300$ mv ($r_{max} \sim 12$). This may be considered to be a large value of input signal and the error minimization algorithm, as discussed earlier, between the desired amplitude response and the response by considering the non zero value of v_{os} was applied. This has been done with an initial value of $|v_s/v_{os}| = r_{max}$ and successively reducing this ratio until the rms error between the desired response and the actual response including the effect of v_{os} and the parasitic capacitances equals or exceeds the specified error limit (5% rms). The resulting minimized $|v_s/v_{os}|$ ratios ($\hat{r}$) are shown in curve (c) of Fig. 4.10. For the case of $Q_p = 10$, $h_A = 5$, $f_s/f_p = 10$, one finds that a value of $\hat{r} > 2.6$ would be sufficient to attain the prescribed error limit. Compared with the unoptimized case, this represents a gain by a factor of ~23 which should accordingly reduce the pre filtering gain requirement by an equal factor. Fig. 4.11 shows the optimized response expected with $|v_s/v_{os}| = 2.6$ if the design is made with the optimized set of capacitances obtained. The value of $\hat{r}$ (=2.6) was increased in small steps and the error criterion was found to be preserved up to about $1.15\hat{r}$. This implies that while the minimum input signal level must be $\hat{r}|v_{os}|$, a level between $\hat{r}|v_{os}|$ and $1.15\hat{r}|v_{os}|$ would still minimize the effect of the offset voltage for the set of design capacitances corresponding to the optimal value $\hat{r}$ of $|v_s/v_{os}|$ ratio.

4.7.2 Experimental Results

Experimental tests were carried out for an SC-BPF with $f_s = 10$

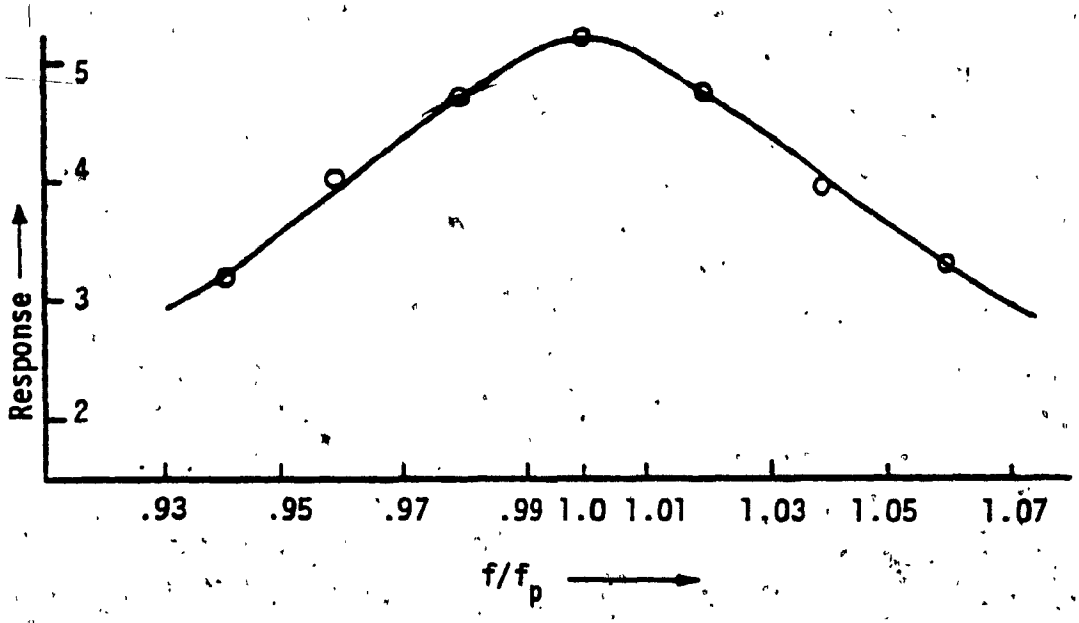


Figure 4.11: The theoretical and the experimental responses for the SC-BPF with v_{os} = 5mv for each UGA and with optimal set of capacitors

kHz, f_p = 1 kHz, Q_p = 10, h_A = 5. The parasitic capacitance in the actual circuit layout was measured to be ~15pF and hence a scaled up version of the network capacitors, arrived at by the optimization algorithm were used. The capacitances C_1 = 5.1 nF, C_{s1} = 25.5 nF, C_3 = 22.9 nF, C_{o2} = 31.3 nF, C_{o1} = 7.2 nF, C_4 = 19.2 nF, C_{s2} = 11.44 nF, C_5 = 22.9 nF and C_6 = 3.43 nF were realized using film/foil type discrete capacitors, with polysterene dielectric, having ±10% tolerance. The UGAs were realized with μA 741 OAs using 100% negative feedback. The switches were CMOS (RCA, type 4066B) analog switches. The offset controls in the OAs were adjusted to make v_{os} = 0 and the experimental data are shown alongside the theoretical curve (a) of Fig. 4.7. The close agreements verify the validity of the parasitic tolerant design method discussed in the text. Next the circuit was redesigned for minimal sensitivity to the offeset voltage in the UGAs. For this the offset controls in the OAs were adjusted to make $|v_{os}|$ = 5mv for each of the OAs. The capacitances corresponding to an optimized $|v_s/v_{os}|$ = 2.6 which minimizes the normalized rms error, due to non zero v_{os}, to below 5% were used. The capacitors were C_1 = 20 nF, C_{s1} = 24.7 nF, C_3 = 37.5 nF, C_4 = 29.2 nF, C_{s2} = 15.8 nF, C_5 = 37.5 nF, C_6 = 10.5 nF, C_{o1} = 7.1 nF and C_{o2} = 31.5 nF. The experimental response is shown alongside the expected response in Fig. 4.11 and the agreements are very good. Using a $|v_s/v_{os}| > 2.6$, better agreeement with the nominal response [Fig. 4.7(a)] was observed. This substantiates the method proposed above to obtain a parasitic tolerant design which is also minimally affected by non zero offset voltages in the UGAs used to synthesize the SC biquadractic filter.

4.8 CONCLUSION

Improved designs of SC biquadratic filters equivalent to the analog biquadratic transfer function under the bilinear mapping between the s and z domains are presented. The active device involved is a unity gain amplifier (buffer) and the number of capacitors needed is comparable to those needed in designs based on OAs used as infinite gain amplifiers. The designs are bottom plate parasitic insensitive. The important question of the parasitic capacitance associated with the top plates of the network capacitors as the input of the UGAs has been examined in detail, and an algorithm to yield a parasitic tolerant design along with minimum total capacitance has been proposed. The effect of a non zero offset voltage in the UGAs on the realizations has been studied and a method has been suggested to minimize this effect. A design that needs very few capacitors and can produce general SDTFs that are bilinear counterparts of the low pass, high pass and bandpass analog functions has also been presented. The flat gain of the analog filter has often to be scaled down in realizing these designs and hence such filters shall have a detrimental effect on the signal to noise power ratio as the signal is processed by the filter. Because of a lack of actual MOS IC fabrication facilities, the UGAs were realized using OAs and detailed experimental tests have been carried out with discrete components. Extensive computer simulations have shown that the filters resulting from the proposed realizations are compatible with the requirements of the current IC technology. The experimental results show very good agreements with the numerically simulated results. The proposed designs present a substantial improvement over

the designs presented in Chapter 3. It is felt that if the realizations are implemented in IC MOS technology, several attractive advantages over the OA realizations will be achieved, such as: reduced substrate area, a higher frequency range of operation, reduced DC power consumption and greater signal to noise power ratio at the output.

To realize the potential of high frequency operation of UGA based SCF designs, a method is needed to account for the frequency dependence of the UGA gain on the SCF realizations. In fact, it is also desirable to have such a method for the OA based realizations. In the following chapter, an elegant analysis technique is developed to examine the effect of the frequency dependent gain of either the UGA or the OA on the performance of the SCFs.

CHAPTER FIVE

THE EFFECT OF FREQUENCY DEPENDENT GAINS OF ACTIVE ELEMENTS IN SC NETWORKS

5.1 INTRODUCTION

The trend followed by earlier workers in the area of SC filters was similar to that in the area of active RC filters, viz., the active device (mostly an OA) in the SC network was assumed to be an ideal element having an infinite value for its DC gain as well as for its gain-bandwidth product (GB). It was soon realized that the finite values of the low frequency (DC) gain and the GB product of the OA have a significant and drastic effect on the performance of an active SC filter as the significant frequency band of the filter and the switching rate are increased. Early investigations in this direction [43], [44] concentrated on an important building block (viz., an SC integrator) using an OA and a biphase clock signal. The proposed methods were principally time domain approaches. This was soon extended to cover the case of SC biquadratic filters realized using OAs[45]. The above methods require solving a set of charge conservation equations (CCEs) together with the differential equations (DEs) of the active devices during each phase of the clock signal. Further, solutions in consecutive phases of the clock signal are related to each other by solving a set of transition equations. Finally, taking the

$\mathcal{Z}$-transforms leads to the sampled data transfer function as a function of frequency [since $z = \exp(j\Omega T)$, Ω = the sampled data frequency]. The approach becomes very laborious even for circuits of moderate complexity (say, a fifth order elliptic filter) in that the CCEs and transition equations have to be written and solved for the entire network on hand. It is, therefore, desirable to investigate the possibility of having a method in which the frequency dependent nature of the active devices in the SC network can be accounted for in a direct and simple manner. Towards this, the z-domain indefinite admittance matrix description of SC networks appears to be a very useful tool. The indefinite admittance matrix (IAM) of passive SC networks can be assembled very easily, in fact, by simple inspection [47]. In the present chapter an analysis method[50] to take into account of the frequency dependent gain of an active device (OA, UGA for example), in an active SC network, using the IAM of the passive part of the network, is presented. The case for biphase clock signal is considered first, which is then extended to the situation where a multiphase clock signal operates the SC network. The basic philosophy of the method consists in identifying, around each active device (AD) in the SC network, a subnetwork N_s of the given SC network N such that (i) N_s contains, apart from the AD, only those nodes that feed directly into the input node of the AD, during a given phase of the clock signal, through switched or unswitched capacitors. The subnetwork N_s is then analysed in the time domain by simultaneously solving for the CCE around the input node of the AD and the DE that relates the input and output node voltages of the AD. Finally, using $\mathcal{Z}$-transformation, constraint equations are obtained relating the input

node voltage of the AD with voltages at other nodes of N_s. Such constraint equations are derived for every phase of the clock signal and the procedure repeated for all the ADs in the network. The constraint equations are then used to modify the IAM of the passive SC network, obtained by removing all the ADs from the original network. This leads us to the IAM for the active SC network. Once the IAM for the active SC network is known, any desired response function can be obtained by routine manipulations on the IAM. In the following, the general analysis method is developed in Section 2 for an AD with a finite low frequency gain and a finite bandwidth and for an SC network operated by biphase clock. In section 3, the method is illustrated by taking three examples. In the first two, the ADs are OAs used as an inverting amplifier. Two well-known parasitic insensitive circuits are analyzed to reveal the simple and modular nature of the proposed analytical procedure. In the third example, the method is applied to the biquadratic sampled data filter (BIQ-SDTF) realized using UGAs as discussed in Chapter 4. In section 4, the analytical procedure is extended to the case where the SC network is operated by a multiphase clock signal. The procedure arrived at in section 4 is illustrated with a simple circuit (a differential SC integrator using one OA). The general analysis technique is then summarized in a number of sequential steps in section 5. Numerical and experimental results are presented in section 6. Since no MOS integrated circuit fabrication facility was available, experimental investigations have been carried out only for non ideal OAs simulated using conventional OAs according to a well known macromodel[44]. The experimental results agree very well with the theoretical predictions.

5.2 . ANALYSIS OF SC NETWORKS WITH TWO PHASE CLOCK SIGNAL

5.2.1 Derivation of the Constraint Equations

Let us first consider an SC network N containing a single active device (AD). Extension to the case of multiple ADs in the network are pointed out later. We assume that the AD has a single input and a single output node with a one pole model for the voltage transfer function, viz., $A(s) = \alpha/(s + \beta)$ in the s-domain. We also assume that the AD has a very high input impedance (ideally infinity) and a very low ouput impedance (ideally zero). In the transfer function A(s) of the AD, β is the 3dB bandwidth of the AD, while $\alpha = \alpha_0\beta$ is the gain bandwidth product (GB) of the AD with a low frequency (DC) gain of α_0. Let us now assume that a subnetwork N_s has been properly identified from N such that N_s (i) contains the AD and (ii) all its nodes, other than the AD input node, contribute to charge flow directly to the input node of the AD through switched or unswitched capacitors. To simplify the analysis, we assume that N_s is of the form shown in Figure 5.1(a). It will be seen later on that if N_s contains additional nodes, they can be easily accounted for. The node "a" might be a source node or an intermediate node in N. In this section, we shall restrict our attention to only SC networks operated by biphase clocks with a duty ratio of unity. If T is the clock period, then the instants of switching are at integral multiples of T/2 [Fig. 5.1(b)]. The interval between two consecutive switching instants constitute a switching phase. In SC networks containing practical switches, one can visualize two distinct intervals of operation in a given switching phase. One is

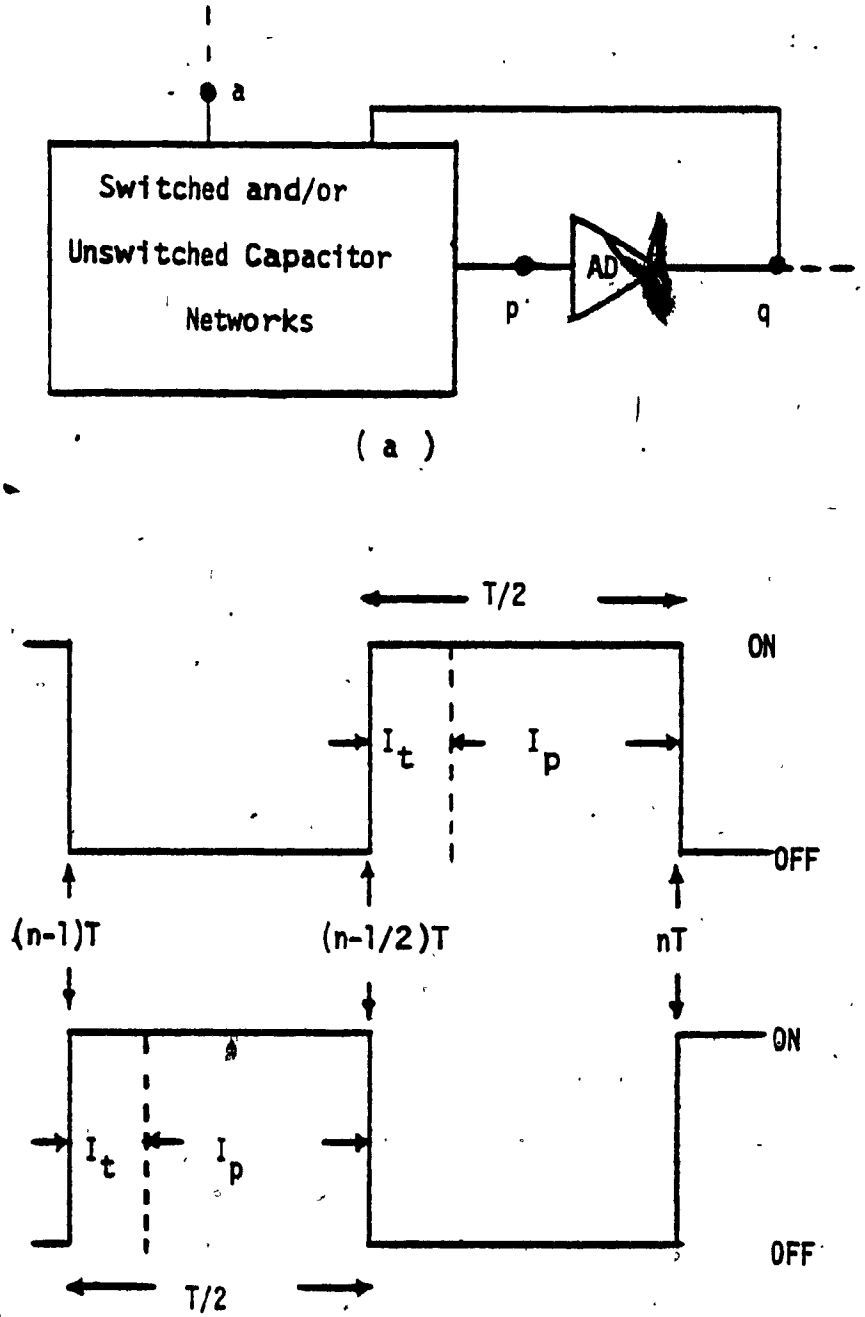


Figure 5.1:(a) A subnetwork (N_s) of N around an AD in a SC filter
(b) Two phase clock signals with clock period T and switching interval T/2

the transition interval I_t during which the circuit topology is in the process of changing from that of the previous phase to that of the given phase. During this time, the switch resistances are changing in an arbitrary but continuous manner from that of one state (say, completely ON) to that of another state (say completely OFF). It is extremely difficult to derive directly mathematical expressions for the nodal voltages in an SC network during this interval. However, any nodal voltage can still be assumed as continuous over this time interval, provided it does not happen to be an input node of the AD. In such a case, the voltage at this node might become discontinuous due to a large feedback from the output of the AD. We shall denote the width of I_t by ε.

Consider now the switching phase defined by the closed interval $[(n - \frac{1}{2})T, nT]$. For this phase, I_t is given by the closed interval $[(n - \frac{1}{2})T, (n - \frac{1}{2})T + \varepsilon]$. We can visualize the other interval, I_p, within the switching phase as the closed interval $[(n - \frac{1}{2})T + \varepsilon, nT]$. For the next switching phase I_t and I_p are $[nT, nT + \varepsilon]$ and $[nT + \varepsilon, (n + \frac{1}{2})T]$, respectively. In any given phase, the circuit topology is linear and time invariant over the interval I_p and consists of completely closed (ON) switches, completely open (OFF) switches, capacitors and ADs. Thus during I_p the network N_s is linear and consequently, a linear CCE can be written for the node p. For any practical SC network, $I_t << I_p$. Consequently, in our subsequent analysis, we shall assume $\varepsilon \to 0$).

Let us consider a given switching phase (say even) defined over

$[(n - \frac{1}{2})T, nT]$. Over the interval I_p for this phase, the voltage $v_p(t)$ at node p [Fig. 5.1(a)] can be expressed using the CCE as:

$$v_p(t) = \alpha_{1q}v_q(t) + \alpha_{1a}v_a(t) + \beta_{1q}v_{qI} + \beta_{1a}v_{a1} + \beta_{1p}v_{pI} \qquad (5.1a)$$

where

$$v_{xI} = v_x(nT - \frac{T}{2} + \varepsilon),\ x = q, a, p \text{ and } \varepsilon \to 0 \qquad (5.1b)$$

The coefficients $\alpha_{1q}, \alpha_{1a}, \beta_{1q}$ and β_{1a} are determined by ratios of capacitances in N_s. The one pole model of the gain function of the AD yields the DE between the output and input voltages of the AD as:

$$\frac{dv_a}{dt} + \beta v_q = \alpha v_p \qquad (5.2)$$

Substituting for $v_p(t)$ from eq. (5.1), we have

$$\frac{dv_a}{dt} + (\beta - \alpha\alpha_{1q})v_q = \alpha\alpha_{1a}v_a + \alpha\beta_{1q}v_{qI} + \alpha\beta_{1a}v_{aI} + \alpha\beta_{1p}v_{pI} \qquad (5.3)$$

Integrating eqn. 5.3 over the interval $I_p \triangleq [t_1 = (n - \frac{1}{2})T + \varepsilon,$ $t_2 = nT]$ one has

$$v_q(nT)e^{k_1 nT} - v_q(nT - \frac{T}{2} + \varepsilon)e^{k_1(nT - \frac{T}{2} + \varepsilon)}$$

$$= \alpha\alpha_{1a} \int_{t_1}^{t_2} v_a(t)e^{k_1 t}dt + \frac{\alpha}{k_1}[e^{k_1 nT} - e^{k_1(nT - \frac{T}{2} + \varepsilon)}]*$$

$$[\beta_{1q}v_{qI} + \beta_{1a}v_{aI} + \beta_{1p}v_{pI}] \qquad (5.4a)$$

where $k_1 = \beta - \alpha\alpha_{1q}$ (5.4b)

In practice the AD may be a UGA or an inverting OA. Experience

shows that in both of these cases, $k_1 >> 1$.

At this point, a few comments are in order. The existing methods of SC filter design implement analog transfer functions through four types of $s \leftrightarrow z$ mapping, viz., (i) backward Euler, (ii) forward Euler, (iii) LDI and (iv) bilinear transformations. Of these, the bilinear tranformation can accommodate the highest cut off frequencies relative to the clock frequency [45] and hence is the most popular. Considering the bilinear transformation, the entire analog frequency spectrum $(0 \rightarrow \infty)$ is mapped into the sampled data frequency band from 0 to $f_s/2 = 1/2T$. In order to preserve a given analog magnitude response, prewarping has to be employed. However, this can be done only at a number of selected frequencies. Consequently, the prewarped transfer function can adequately represent the given magnitude response only if the highest critical frequency of the filter is not too close to the Nyquist limit, viz., $f_s/2$. Numerical simulations using biquadratic transfer functions, have shown clearly that to maintain an rms error of 10% or less over the frequency band of interest, one requires $f_s/f_h > 5$ where f_h is the highest critical frequency of the analog filter. Thus, the interval of integration $t_2 - t_1 = \frac{T}{2}$ in eqn. 5.4(a) is $< T_h/10$, where $T_h = 1/f_h$, so that $v_a(t)$ can be assumed to be changing very slowly over this interval (for circuits that so far have been realized in practice, $\frac{T}{2} < T_h/14$[32]). Hence in $\int_{t_1}^{t_2} v_{a1} e^{k_1 t} dt$, the variation of $v_a(t)$ can be ignored in comparison to that of $e^{k_1 t}$, particularly since k_1 is >> 1. **This step is rigorously valid when $v_a(t)$ is a sampled and held voltage which is often the case in SC circuits where the input source voltage is sampled and held.**

In view of the above, the integral on the right-hand side (RHS) of eqn. 5.4(a) can be expressed as:

$$\int_{t_1}^{t_2} v_a(t)\, e^{k_1 t} dt = \frac{1}{k_1}\left[e^{k_1 t} v_a(t)\right]_{t_1}^{t_2} \tag{5.5}$$

Hence eqn. 5.4 simplifies to:

$$v_q(nT) - v_q(nT - \frac{T}{2} + \varepsilon)e^{-k(\frac{T}{2} + \varepsilon)}$$

$$= \frac{\alpha\alpha_{1a}}{k_1}\left[v_a(nT) - v_a(nT - \frac{T}{2} + \varepsilon)\, e^{-k_1(\frac{T}{2} - \varepsilon)} + \right.$$

$$\left. \frac{\alpha}{k_1}\left[1 - e^{-k_1(\frac{T}{2} + \varepsilon)}\right]\right] \left[\beta_{1q} v_{qI} + \beta_{1a} v_{aI} + \beta_{1p} v_{pI}\right] \tag{5.6}$$

Writing $\lambda_1 = \exp\left[-k_1(\frac{T}{2} + \varepsilon)\right]$, one has

$$\beta_{1q} v_{qI} + \beta_{1a} v_{aI} + \beta_{1p} v_{pI} = \frac{k_1}{\alpha(1 - \lambda_1)} v_q(nT)$$

$$- \frac{k_1\lambda_1}{\alpha(1 - \lambda_1)} v_q(nT - \frac{T}{2} + \varepsilon) - \frac{\alpha_{1a}}{1 - \lambda_1} v_a(nT)$$

$$+ \frac{\alpha_{1a}\lambda_1}{1 - \lambda_1} v_a(nT - \frac{T}{2} + \varepsilon) \tag{5.7}$$

Substituting for the LHS of eqn. 5.7 in eqn. 5.1, one has

$$v_p(t) = \alpha_{1q} v_q(t) + \alpha_{1a} v_a(nT) + \frac{k_1}{\alpha(1 - \lambda_1)} v_q(nT)$$

$$- \frac{k_1\lambda_1}{\alpha(1 - \lambda_1)} v_q(nT - \frac{T}{2} + \varepsilon) - \frac{\alpha_{1a}}{1 - \lambda_1} v_a(nT)$$

$$+ \frac{\alpha_{1a}\lambda_1}{1 - \lambda_1} v_a(nT - \frac{T}{2} + \varepsilon) \tag{5.8}$$

Finally, putting $t = nT$ and noting that $v_q(t)$, $v_a(t)$ are continuous as $\varepsilon \to 0$, one has

$$v_p(nT) = A_{qp}v_q(nT) + B_{qp}v_q(nT \pm \frac{T}{2}) + C_{ap}v_a(nT) + D_{ap}v_a(nT - \frac{T}{2}) \tag{5.9a}$$

where $\lambda_1 = \exp(-k_1 T/2)$

$$A_{qp} = -[\alpha_{1q}\lambda_1 - \frac{\beta}{\alpha}] / (1 - \lambda_1)$$

$$B_{qp} = -[\lambda_1/(1 - \lambda_1)] [-\alpha_{1q} + \frac{\beta}{\alpha}] \tag{5.9b}$$

$$C_{ap} = -\frac{\lambda_1\alpha_{1a}}{1 - \lambda_1} = -D_{ap}$$

In the above equations, the coefficients A_{qp}, B_{qp} are due to AD output node q while C_{ap}, D_{ap} are due to the **intermediate node** "a", obtained from the original network N in the process of identifying the subnetwork N_s. If N_s contains additional intermediate nodes, their presence can be accounted for in a simple fashion by incorporating merely additional coefficients in eqn. (5.9) similar to C_{ap}, D_{ap}. Further, if N contains additional ADs, subnetworks similar to N_s can be identified for each of the ADs. Analysis of these subnetworks will then yield equations similar to eqn. (5.9) for the voltage of the input node of each AD. **In passing, the simplicity, modularity and generality of eqn. 5.9 may be observed.** Denoting the given phase as the even phase and taking -transform on both sides of eqn. (5.9), we have

$$V_p^e(z) = A_{qp}^{ee}V_q^e(z) + A_{qp}^{eo}V_q^o(z) + B_{ap}^{ee}V_a^e(z) + B_{ap}^{eo}V_a^o(z) \tag{5.10a}$$

where $A_{qp}^{ee} = A_{qp}$, $A_{qp}^{eo} = z^{-1/2}B_{qp}$

$$B_{ap}^{ee} = C_{ap}, \quad B_{ap}^{eo} = z^{-1/2}D_{ap} \tag{5.10b}$$

In an analogous manner, one can write down a CCE for the other phase (say odd) with its I_p interval defined over $[nT - T + \varepsilon, nT - \frac{T}{2}]$. From the CCE, one can write, for $(nT - T) < t < (nT - \frac{T}{2})$,

$$v_p(t) = \alpha_{2q}v_q(t) + \alpha_{2a}v_a(t) + \beta_{2q}v_{qI} + \beta_{2a}v_{aI} + \beta_{2p}v_{pI} \quad (5.11a)$$

where $\alpha_{2q}, \alpha_{2a}, \beta_{2q}, \beta_{2a}, \beta_{2p}$ are capacitance ratios pertinent to the given phase and now

$$v_{xI} = v_x\{(n-1)T + \varepsilon\}, \; x = q,a,p \text{ and } \varepsilon \to 0 \quad (5.11b)$$

Following an exactly analogous method of analysis one shall arrive finally at:

$$V_p^o(z) = A_{qp}^{oo}V_q^o(z) + A_{qp}^{oe}V_q^e(z) + B_{ap}^{oo}V_a^o(z) + B_{ap}^{oe}V_a^e(z) \quad (5.12a)$$

where $A_{qp}^{oo} = -[\alpha_{2q}\lambda_2 - \beta/\alpha] \; / \; (1 - \lambda_2)$

$$A_{qp}^{oe} = z^{-1/2} \; \frac{\lambda_2}{1-\lambda_2} \; [\beta/\alpha - \alpha_{1q}]$$

$$B_{ap}^{oo} = - \frac{\lambda_2\alpha_{2a}}{1-\lambda_2}$$

$$B_{ap}^{oe} = z^{-1/2} \; \frac{\lambda_2\alpha_{2a}}{1-\lambda_2}$$

$$\lambda_2 = \exp(-k_2T/2)$$

$$k_2 = \beta - \alpha\alpha_{2q}$$

Eqns. 5.10, 5.12 represent, in the frequency domain, constraints on the voltage of the AD input node due to the presence of the AD in the

biphase SC circuit. In any frequency domain analysis, these constraints have to be accommodated appropriately. For example, equivalent circuit method of analysis due to Laker [10] can be utilized along with the above constraint to analyze small sized SC networks quite successfully. However, for large networks IAM technique is more convenient. In what follows, we shall show how the constraint equations can be used along with the IAM technique to predict the effect of ADs with frequency dependent gains on SC networks.

5.2.2 Derivation of the Definite Admittance Matrix (DAM) for the Active SC Network

Let us assume that the network N contains n nodes including the nodes a,p,q of N_s. By following the method due to Moschytz and Hökenek[47], the IAM of the resulting passive network (Y_p) can be written down by inspection. The constraint eqn. (5.10), (5.12) are valid for specific topologies in the given phases, viz., the topologies obtained with the switches either open or closed. Hence, before incorporating these equations in the IAM, Y_p has to be modified by using the principle of contractions due to switching[47]. Let us denote the resulting matrix by Y_m. Assuming it is of order (m,m) (after deleting the grounded nodes), Y_m can be written in the form:

$$
\begin{array}{c|cccccc|cccccc}
 & 1^e & a^e & p^e & q^2 & \cdots & m^e & 1^o & \cdots & a^o & p^o & q^o & \cdots m^o \\
\hline
1^e & y^{ee}_{11} & y^{ee}_{1a} & y^{ee}_{1p} & y^{ee}_{1q} & \cdots & & y^{eo}_{1a} & & y^{eo}_{1p} & y^{eo}_{1q} & \cdots & \\
a^e & y^{ee}_{a1} & y^{ee}_{aa} & y^{ee}_{ap} & y^{ee}_{aq} & \cdots & & y^{eo}_{aa} & & y^{eo}_{ap} & y^{eo}_{aq} & \cdots & \\
p^e & y^{ee}_{p1} & y^{ee}_{pa} & y^{ee}_{pp} & y^{ee}_{pq} & \cdots & & y^{eo}_{pa} & & y^{eo}_{pp} & y^{eo}_{pq} & \cdots & \\
q^e & y^{ee}_{q1} & y^{ee}_{qa} & y^{ee}_{qp} & y^{ee}_{qq} & \cdots & & y^{eo}_{qa} & & y^{eo}_{qp} & y^{eo}_{qq} & \cdots & \\
\vdots & & & & & & & & & & & & \\
m^e & & & & & & & & & & & & \\
\vdots & & & & & & & & & & & & \\
1^o & y^{oe}_{11} & y^{oe}_{1a} & y^{oe}_{1p} & y^{0e}_{1q} & \cdots & & y^{oo}_{1a} & & y^{oo}_{1p} & y^{oo}_{1q} & \cdots & \\
a^o & y^{oe}_{a1} & y^{oe}_{aa} & y^{oe}_{ap} & y^{0e}_{aq} & \cdots & & y^{oo}_{aa} & & y^{oo}_{ap} & y^{oo}_{aq} & \cdots & \\
p^o & y^{oe}_{p1} & y^{oe}_{pa} & y^{oe}_{pp} & y^{0e}_{pq} & \cdots & & y^{oo}_{pa} & & y^{oo}_{pp} & y^{oo}_{pq} & \cdots & \\
q^o & y^{oe}_{q1} & y^{oe}_{qa} & y^{oe}_{qp} & y^{0e}_{qq} & \cdots & & y^{oo}_{qa} & & y^{oo}_{qp} & y^{oo}_{qq} & \cdots & \\
m^o & & & & & & & & & & & & \cdots\cdots
\end{array}
\qquad (5.13)
$$

The different entries of Y_m are functions of (i) the capacitors in the circuit, (ii) the clock rate ($f_s = 1/T$) applied to the circuit, and (iii) the sampled data variable z. Consider now a row in eqn. (5.13), say the a^eth row. This corresponds to the equation

$$I^e_a = \ldots + y^{ee}_{aa} V^e_a + y^{ee}_{ap} V^e_p + y^{ee}_{aq} V^e_q + \ldots + y^{eo}_{aa} V^o_a + y^{eo}_{ap} V^o_p + y^{eo}_{aq} V^o_q + \ldots \qquad (5.14)$$

To account for the presence of the AD, we now have to substitute of V^e_p and V^o_p from eqn. (5.10) and (5.12). We then have

$$I^e_a = \ldots + (y^{ee}_{aa} + B^{ee}_{ap} y^{ee}_{ap} + B^{oe}_{ap} y^{eo}_{ap}) V^e_a +$$

$$+(y_{aq}^{ee}+A_{qp}^{ee}y_{ap}^{ee}+A_{qp}^{oe}y_{ap}^{eo})V_q^e$$

$$+(y_{aa}^{eo}+B_{ap}^{eo}y_{ap}^{ee}+B_{ap}^{oo}y_{ap}^{eo})V_a^o$$

$$+(y_{aq}^{eo}+A_{qp}^{eo}y_{ap}^{oo}+A_{qp}^{oo}y_{ap}^{eo})V_q^o \quad +... \qquad (5.15)$$

Similarly, the equations corresponding to other rows in (5.13) have to be modified. Further, we note that the rows corresponding to q^e and q^o are redundant since they correspond to the even and odd phases of the current from the output of the AD which behaves like a voltage source. These rows can, therefore, be discarded. Consequently, the DAM of the active SC network is obtained as follows:

(i) delete the rows corresponding to q^e, q^o in Y_m.

(ii) add to the elements of a^e, q^e, a^o q^o columns, the elements of p^e, p^o columns multiplied by appropriate functions as obtained from eqns. (5.10) and (5.12). For example, the new (a^e, q^o)th element, y_{aq}^{eo} of the IAM shal be given by

$$\hat{y}_{aa}^{eo} = y_{aq}^{eo} + A_{qp}^{eo}y_{ap}^{ee} + A_{qp}^{oo}y_{ap}^{eo} \qquad (5.16)$$

(iii) delete the elements corresponding to p^e, p^o columns.

The presence of other AD is accounted for by following a similar procedure for each of the ADs. Once, of course, the IAM is obtained, any other network function of interest can be derived from it.

It may be observed that the only piece of information needed in the proposed method of analysis are the passive IAM and the constraint equations, both of which are derived separately over the I_p intervals

of the two phases. At no stage do we require any information on the state of the circuit in the interval of transition I_t. Consequently, a time domain analysis over I_t is not needed as were in the methods proposed by the others.

5.3 ILLUSTRATION OF THE METHOD

Three examples are now given to illustrate the analysis technique proposed above. The first circuit is the well known stray insensitive SC integrator[44] described by Martin and Sedra and the second is a stray insensitive SC biquadradic filter introduced by Laker and Fleischer[49]. In both these circuits the active devices are OAs, used as inverting amplifiers. The third example is the SC biquadratic filter, proposed in Chapter 4, where the active devices are the UGAs.

5.3.1 An Inverting Stray Insensitive SC Integrator

As has been pointed out above, the AD in this case is an OA having (say) a finite low frequency (DC) gain of $-A_o$ and a finite GB value of B. Thus, in our formulations above, we have to use $\alpha = -B$ and $\beta = B/A_o = \omega_c$, the usual relation for the 3dB frequency of the OA. Consider now Figure 5.2 which shows the SC integrator with the nodes numbered ... a, p, q, ... In the even phase $\{(n-\frac{1}{2})T < t < nT\}$ the CCE is

$$C_1[v_a(t)-v_p(t)]-C_1[v_{aI}-v_{pI}] = C_2[v_p(t)-v_q(t)]-C_2[v_{pI}-v_{qI}] \quad (5.17)$$

where (as in eqn. 5.1), $v_{xI} = v_x(nT - \frac{T}{2} + \varepsilon)$, $x = a,p,q$ and $\varepsilon \to 0$. In

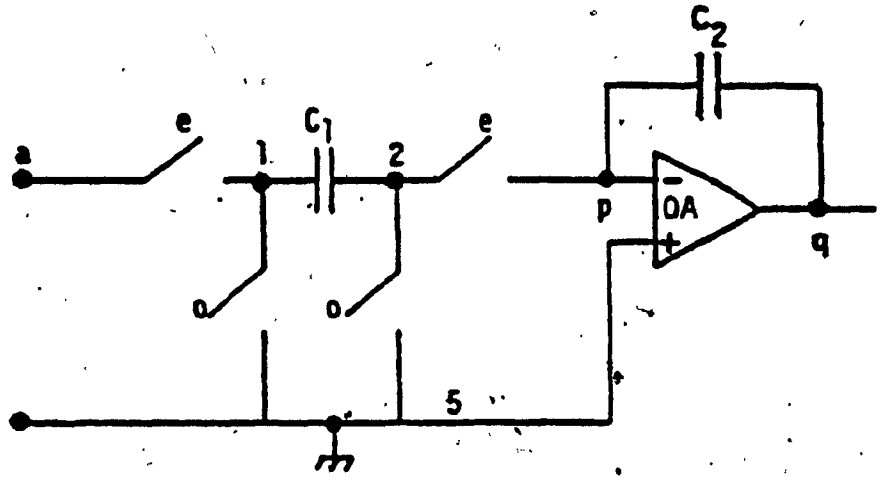


Figure 5.2: A stray insensitive SC integrator

[44] the signal source voltage $v_a(t)$ was assumed as sampled and held (SH). With this, $v_a(t) = v_{aI}$. Thus,

$$v_p(t) = [C_2/(C_1 + C_2)]v_q(t) - [C_2/(C_1 + C_2)]v_{qI} + v_{pI} \qquad (5.18)$$

Comparing this equation with eqn. (5.1), one has

$$\alpha_{1q} = C_2/(C_1 + C_2),\ \beta_{1q} = -\alpha_{1q},\ \alpha_{1a} = 0 = \beta_{1a},\ \beta_{1p} = 1 \qquad (5.19)$$

Further, as in [44], we assume for the OA, $A(s) = -B/s$, that is, $w_c = 0$. This gives, from eqn. (5.4b), $k_1 = \alpha_{1q}B = BC_2/(C_1 + C_2)$, and $\lambda_1 = \exp\{-B \frac{C_2}{C_1 + C_2} \frac{T}{2}\}$. Since this circuit contains only one OA, $V_p^e(z)$ can be expressed as in eqn. (5.10a), whence from (5.9b) and (5.10b) we obtain

$$A_{qp}^{eo} = -[\frac{C_2}{C_1+C_2} \exp\{-B \frac{C_2}{C_1+C_2} \frac{T}{2}\}]/[1-\exp\{-B \frac{C_2}{C_1+C_2} \frac{T}{2}\}]$$

$$A_{qp}^{ee} = -z^{-1/2} A_{qp}^{ee} \qquad (5.20)$$

$$B_{ap}^{ee} = 0 = B_{ap}^{eo}$$

Similarly, for the odd phase $\{(n-1)T < t < (n-\frac{1}{2})T\}$, one has the CCE

$$C_2[v_p(t) - v_q(t)] = C_2(v_{pI} - v_{qI}) \qquad (5.21)$$

which leads to $\alpha_{2q} = 1$, $\beta_{2q} = -1$, $\beta_{2p} = 1$. Proceeding as above but using the relations pertaining to odd phase we can put $V_p^o(z)$ directly in the form of eqn. (5.12a) where

$$A_{qp}^{oo} = -[\exp(-BT/2)]/[1 - \exp(-BT/2)]$$

$$A_{qp}^{oe} = z^{-1/2}\exp(-BT/2)/[1 - \exp(-BT/2)] \qquad (5.22a)$$

$$B_{qp}^{oo} = -\exp(-BT/2)/[1 - \exp(-BT/2)]$$

$$B_{qp}^{oe} = z^{-1/2}\exp(-BT/2)/[1 - \exp(-BT/2)] \qquad (5.22a)$$

The IAM of the passive part of circuit in Fig. 5.2 is given by

$$\begin{array}{c} \\ a^e \\ 1^e \\ 2^e \\ p^e \\ q^e \\ 5^e \\ a^o \\ 1^o \\ 2^o \\ p^o \\ q^o \\ 5^o \end{array}
\begin{array}{c}
\begin{array}{cccccccccccc} a^e & 1^e & 2^e & p^e & q^e & 5^e & a^o & 1^o & 2^o & p^o & q^o & 5^o \end{array} \\
\left[\begin{array}{cccccccccccc}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & C_1 & -C_1 & 0 & 0 & 0 & 0 & \hat{C}_1 & -\hat{C}_1 & 0 & 0 & 0 \\
0 & -C_1 & C_1 & 0 & 0 & 0 & 0 & -\hat{C}_1 & \hat{C}_1 & 0 & 0 & 0 \\
0 & 0 & 0 & C_2 & -C_2 & 0 & 0 & 0 & 0 & \hat{C}_2 & -\hat{C}_2 & 0 \\
0 & 0 & 0 & -C_2 & C_2 & 0 & 0 & 0 & 0 & -\hat{C}_2 & \hat{C}_2 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \hat{C}_1 & -\hat{C}_1 & 0 & 0 & 0 & 0 & C_1 & -C_1 & 0 & 0 & 0 \\
0 & -\hat{C}_1 & \hat{C}_1 & 0 & 0 & 0 & 0 & -C_1 & C_1 & 0 & 0 & 0 \\
0 & 0 & 0 & \hat{C}_2 & -\hat{C}_2 & 0 & 0 & 0 & 0 & C_2 & -C_2 & 0 \\
0 & 0 & 0 & -\hat{C}_2 & \hat{C}_2 & 0 & 0 & 0 & 0 & -C_2 & C_2 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}\right]
\end{array} \qquad (5.22b)$$

where $\hat{C}_i = -z^{-1/2}C_i$, $i = 1,2$.

Allowing for the switch contractions and discarding ground nodes (5^e,

5^o), eqn. 5.22 reduces to

$$\begin{array}{c} \\ a^e \\ p^e \\ q^e \\ p^o \\ q^o \end{array} \begin{array}{c} \begin{array}{ccccc} a^e=1^e & p^e=2^e & q^e & p^o & q^o \end{array} \\ \begin{bmatrix} C_1 & -C_1 & 0 & 0 & 0 \\ -C_1 & C_1+C_2 & -C_2 & \hat{C}_2 & -\hat{C}_2 \\ 0 & -C_2 & C_2 & -\hat{C}_2 & \hat{C}_2 \\ 0 & \hat{C}_2 & -\hat{C}_2 & C_2 & -C_2 \\ 0 & -\hat{C}_2 & \hat{C}_2 & -C_2 & C_2 \end{bmatrix} \end{array} \qquad (5.23)$$

Inserting the constraints as given by eqns. 5.10a, 5.12a, 5.19 and 5.21 in 5.23, one has the DAM (Y_F) for the circuit as

$$\begin{array}{c} \\ a^e \\ p^e \\ p^o \end{array} \begin{array}{c} \begin{array}{ccc} a^e & q^e & q^o \end{array} \\ \begin{bmatrix} C_1 & -A_{qp}^{ee}C_1 & -A_{qp}^{eo}C_1 \\ -C_1 & -C_2+A_{qp}^{ee}(C_1+C_2)+A_{qp}^{oe}\hat{C}_2 & -\hat{C}_2+A_{qp}^{eo}(C_1+C_2)+A_{qp}^{oo}\hat{C}_2 \\ 0 & -\hat{C}_2+A_{qp}^{ee}\hat{C}_2+A_{qp}^{oe}C_2 & -C_2+A_{qp}^{eo}\hat{C}_2+A_{qp}^{oo}C_2 \end{bmatrix} \end{array} \qquad (5.24)$$

Y_F in eqn. 5.24 can be manipulated to obtain the transfer function $V_q^e/V_a^e = \Delta_{12}/\Delta_{11}$ where Δ_{ij} is the cofactor of Y_F coprresponding to i^{th} row and j^{th} column. On calculating the cofactors, one gets

$$\frac{V_q^e(z)}{V_a^e(z)} = -\frac{C_1}{C_2} \frac{1-e^{-k_1}+z^{-1/2}\, ke^{-k_1}(1-e^{-k_2})}{(1-z^{-1})[1-kz^{-1}e^{-(k_1+k_2)}]} \qquad (5.25a)$$

where $k_1 = B\dfrac{C_2}{C_1+C_2}\dfrac{T}{2}$, $k_2 = B\dfrac{T}{2}$, $k = \dfrac{C_2}{C_1+C_2}$

Eqn. (5.24) is the same as the result obtained by Martin and Sedra.

5.3.2 A Second Order Parasitic Insensitive SC Filter

As a second example, let us consider a well-known second order SC band-pass (BP) filter shown in Fig. 5.3[49]. This filter will also be considered later on, for experimental investigations. It may be observed that Fig. 5.3 represents a multi-OA, viz., a two-OA circuit. To apply our analysis technique, we shall now assign the subscript 'i' ($i = 1,2$) to any quantity associated with the i^{th} OA. Thus the constraint eqns. (5.10) and (5.12) would appear as

$$V^e_{pi} = A^{ee}_{qpi} V^e_{qi} + A^{eo}_{qpi} V^o_{qi} + B^{ee}_{api} V^e_{ai} + B^{eo}_{api} V^o_{ai} \qquad (5.26a)$$

where

$$\begin{aligned}
\lambda_{1i} &= \exp(-k_{1i}T/2) \\
k_{1i} &= B_i\alpha_{1qi} + w_{ci} \\
A^{ee}_{qpi} &= -[\alpha_{1qi}\lambda_{1i} + 1/A_{oi}]/(1-\lambda_{1i}) \qquad (5.26b) \\
A^{eo}_{qpi} &= z^{-1/2}[\alpha_{1qi} + 1/A_{oi}][\lambda_{1i}/(1-\lambda_{1i})] \\
B^{ee}_{api} &= -\alpha_{1ai}\lambda_{1i}/(1-\lambda_{1i}) \\
B^{eo}_{api} &= z^{-1/2}\alpha_{1ai}\lambda_{1i}/(1-\lambda_{1i})
\end{aligned}$$

and

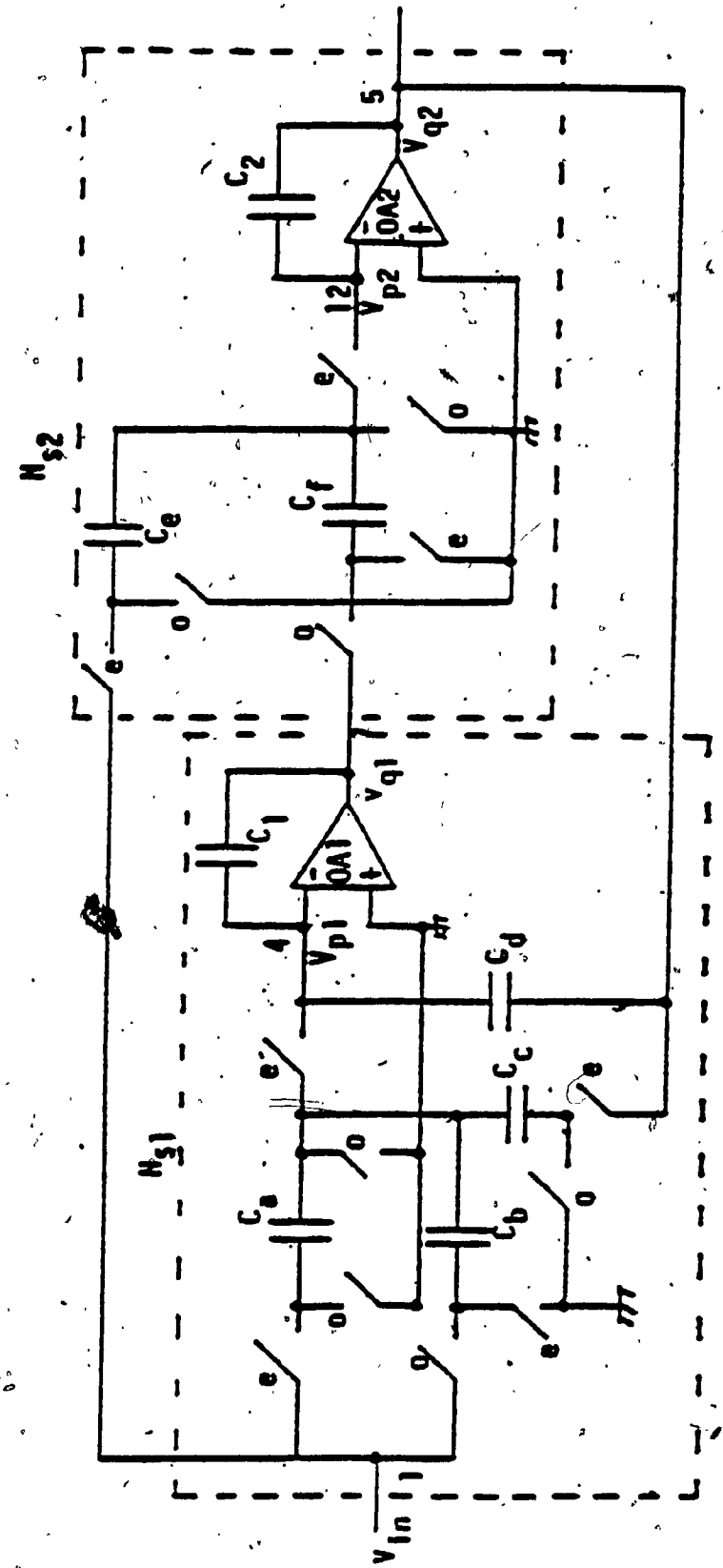


Figure 5.3: The parasitic insensitive SC biquadratic BP filter (using OAs) due to Fleischer and Laker

$$v^{o}_{pi} = A^{oo}_{qpi} v^{o}_{qi} + A^{oe}_{qpi} v^{e}_{qi} + B^{oo}_{api} v^{o}_{ai} + B^{oe}_{api} v^{e}_{ai} \qquad (5.27a)$$

where

$$\lambda_{2i} = \exp(-k_{2i}T/2)$$

$$k_{2i} = B_i \alpha_{2qi} + w_{ci}$$

$$A^{oo}_{qpi} = -[\alpha_{2qi}\lambda_{2i} + 1/A_{oi}]/(1-\lambda_{2i}) \qquad (5.27b)$$

$$B^{oo}_{api} = -\alpha_{2ai}\lambda_{2i}/(1-\lambda_{2i})]$$

$$B^{oe}_{api} = z^{-1/2}\, \alpha_{2ai}\lambda_{2i}/(1-\lambda_{2i})$$

Considering the subnetwork N_{s1} around OA1 of Fig. 5.3 we have from the CCE at the OA input node, for the even phase $[(n - \frac{1}{2})T < t < nT]$

$$v_{p1}(t) = \frac{C_1}{C_{s1}} v_{q1}(t) \frac{C_c+C_d}{C_{s1}} v_{q2} + \frac{C_a}{C_{s1}} v_{in}(t) \qquad (5.28a)$$

$$- \frac{C_1}{C_{s1}} v_{q1I} - \frac{C_c+C_d}{C_{sd1}} v_{q2I} - \frac{C_a}{C_{s1}} v_{inI} + v_{p1I}$$

where $C_{s1} = C_a+C_b+C_c+C_d+C_1$ and $v_{xI} = v_x[(n - \frac{1}{2})T+\varepsilon]$, $x=q_1, q_2, in, p_1$ and $\varepsilon \to 0$

One can write

$$\alpha_{1q1} = C_1/C_{s1},\ \alpha_{1a1} = (C_c+C_d)/C_{s1},\ \alpha_{1b1} = C_a/C_{s1}$$

$$\beta_{1q1} = -\alpha_{1q1},\ \beta_{1a1} = -\alpha_{1a1},\ \beta_{1b1} = -C_a/C_{s1}$$

$$\beta_{1p1} = (C_a+C_b+C_c+C_d+C_1)/C_{s1} \qquad (5.28b)$$

When, using eqn. (5.26), one has

$$V^e_{p1} = A^{ee}_{qp1}V^e_{q1}+A^{eo}_{qp1}V^o_{q1}+B^{ee}_{qp1}V^e_{q2}+B^{eo}_{qp1}V^o_{q2}+C^{ee}_{inp1}V^e_{in}+C^{eo}_{inp1}V^o_{in} \qquad (5.29a)$$

where the different coefficients A^{ee}_{qp1}, A^{eo}_{qp1} ... can be obtained using eqns. 5.26(b) and 5.28(b) with i = 1. In particular:

$$\begin{aligned} B^{ee}_{qp1} &= -\alpha_{1a1}\lambda_{11}/(1-\lambda_{11}) \\ B^{eo}_{ap1} &= -z^{1/2}B^{ee}_{qp1} \\ C^{ee}_{inp1} &= -\alpha_{1b1}\lambda_{11}/(1-\lambda_{11}) \\ C^{eo}_{inp1} &= -z^{-1/2}C^{ee}_{inp1} \end{aligned} \qquad (5.29b)$$

Similarly, from the CCE in the odd phase $\{(n-1)T < t < (n-\frac{1}{2})T\}$ for OA1, one has

$$v_{p1}(t) = \frac{C_1}{C_{s2}}v_{q1}(t) + \frac{C_d}{C_{s2}}v_{q2}(t) - \frac{C_1}{C_{s2}}v_{q1I} - \frac{C_d}{C_{s2}}v_{q2I} + v_{p1I} \qquad (5.30a)$$

where $C_{s2} = C_1 + C_d$. One can write

$$\alpha_{2q1} = C_1/C_{s2},\ \alpha_{2a1} = C_d/C_{s2},\ \beta_{2q1} = -\alpha_{2q1},\ \beta_{2a1} = -\alpha_{2a1} \qquad (5.30b)$$

and $\beta_{2p1} = (C_1 + C_d)/C_{s2}$

Hence, as before, we can obtain

$$V^o_{p1} = A^{oo}_{qp1}V^o_{q1}+A^{oe}_{qp1}V^e_{q1}+B^{oo}_{qp1}V^o_{q2}+B^{oe}_{qp1}V^e_{q2} \qquad (5.31)$$

where the quantities A^{oo}_{qp1}, A^{oe}_{qp1}... etc. can be obtained from (5.30b) and (5.27b) with i = 1.

For OA2, considering N_{s2}, one can obtain from the CCEs in the even and odd phases

$$v_{p2}(t) = \frac{C_2}{C_{s3}} v_{q2}(t) + \frac{C_e}{C_{s3}} v_{in}(t) - \frac{C_2}{C_{s3}} v_{q2I} - \frac{C_e}{C_{s3}} v_{inI} + v_{p2I} \quad (5.32a)$$

and

$$v_{p2}(t) = v_{q2}(t) - v_{q2I} + v_{p2I}, \ \{(n-1)T < t < (n - \tfrac{1}{2})T\} \quad (5.32b)$$

where $C_{s3} = C_2 + C_e + C_f$

Thus

$$\alpha_{1q2} = C_2/C_{s3}, \ \alpha_{1a2} = C_e/C_{s3}, \ \beta_{1q2} = -\alpha_{1q2}, \ \beta_{1a2} = -\alpha_{1a2}$$

$$\beta_{1p2} = (C_2 + C_e + C_f)/C_{s3} \quad (5.33a)$$

and

$$\alpha_{2q2} = 1, \ \beta_{2q2} = -1, \ \beta_{2p2} = 1 \quad (5.33b)$$

Using eqns. (5.33a) , (5.33b), (5.26), (5.27) (with i = 2) one can easily obtain the expressions for V^e_{p2} and V^o_{p2}.

Consider now the BP filter with the OAs removed. We can obtain the IAM of the passive part by inspection. After the switch contraction operations on the IAM and eliminating the ground node, we can derive the DAM, Y_p of the passive part of the circuit as below:

	1^e	4^e	5^e	7^e	12^e	1^o	4^o	5^o	7^o	12^o
1^e	C_a+C_e	$-C_a$	0	0	$-C_e$	0	0	0	0	0
4^e	$-C_a$	C_{s1}	$-(C_c+C_d)$	$-C_1$	0	$-\hat{C}_b$	$\hat{C}_{s2}$	$-\hat{C}_d$	$-\hat{C}_1$	0
5^e	0	$-(C_c+C_d)$	$C_c+C_d+C_2$	0	$-C_2$	0	$-\hat{C}_d$	$\hat{C}_d+\hat{C}_2$	0	$-\hat{C}_2$
7^e	0	$-C_1$	0	C_1	0	0	$-\hat{C}_1$	0	$\hat{C}_1$	0
12^e	$-C_e$	0	$-C_2$	0	C_{s3}	0	0	$-\hat{C}_2$	$-\hat{C}_f$	$\hat{C}_2$
1^o	0	$-\hat{C}_b$	0	0	0	C_b	0	0	0	0
4^o	0	$\hat{C}_1+\hat{C}_d$	$-\hat{C}_d$	$-\hat{C}_1$	0	0	C_{s2}	$-C_d$	$-C_1$	0
5^o	0	$-\hat{C}_d$	$\hat{C}_d+\hat{C}_2$	0	$-\hat{C}_2$	0	$-C_d$	C_d+C_2	0	$-C_2$
7^o	0	$-\hat{C}_1$	0	$\hat{C}_1$	$-\hat{C}_f$	0	$-C_1$	0	C_1+C_f	0
12^o	0	0	$-\hat{C}_2$	0	$\hat{C}_2$	0	0	$-C_2$	0	C_2

(5.34a)

where,

$$C_{s1} = C_a+C_b+C_c+C_d+C_1, \quad C_{s2} = C_1+C_d \tag{5.34b}$$

$$C_{s3} = C_e+C_f+C_2, \quad \hat{C}_x = -z^{-1/2}C_x, \; x = 1,2,b,c,d,f$$

We can then insert in eqn. (5.34a) the constraint equations (c.f. eqns. 5.25, 5.27 with i = 1,2) derived above for the two OAs. The resulting DAM of the active BP filter can be expressed in the form:

$$\begin{array}{c} \\ 1 \\ 4 \\ 12 \\ 1^o \\ 4^o \\ 12^o \end{array} \begin{array}{c} \begin{array}{cccccc} 1 & 5 & 7 & 1^o & 5^o & 7^o \end{array} \\ \begin{bmatrix} \hat{y}_{11} & \hat{y}_{13} & \hat{y}_{14} & \hat{y}_{16} & \hat{y}_{18} & \hat{y}_{19} \\ \hat{y}_{21} & \hat{y}_{23} & \hat{y}_{24} & \hat{y}_{26} & \hat{y}_{28} & \hat{y}_{29} \\ \hat{y}_{51} & \hat{y}_{53} & \hat{y}_{54} & \hat{y}_{56} & \hat{y}_{58} & \hat{y}_{59} \\ \hat{y}_{61} & \hat{y}_{63} & \hat{y}_{64} & \hat{y}_{66} & \hat{y}_{68} & \hat{y}_{69} \\ \hat{y}_{71} & \hat{y}_{73} & \hat{y}_{74} & \hat{y}_{76} & \hat{y}_{78} & \hat{y}_{79} \\ \hat{y}_{10,1} & \hat{y}_{10,3} & \hat{y}_{10,4} & \hat{y}_{10,6} & \hat{y}_{0,18} & \hat{y}_{10,9} \end{bmatrix} \end{array} \tag{5.35}$$

where

$$\begin{aligned} \hat{y}_{i1} &= y_{i1}+C^{ee}_{inp1}\, y_{i2}+B^{ee}_{ap}y_{i5} \\ \hat{y}_{i3} &= y_{i3}+B^{ee}_{qp1}y_{i2}+B^{oe}_{qp1}y_{i7}+A^{ee}_{qp2}y_{i5}+A^{oe}_{qp2}y_{i,10} \\ \hat{y}_{i4} &= y_{i4}+A^{ee}_{qp1}y_{i2}+A^{oe}_{qp1}y_{i7} \\ \hat{y}_{i6} &= y_{i6}+C^{eo}_{inp1}y_{i2}+B^{oe}_{ap2}y_{i5} \\ \hat{y}_{i8} &= y_{i8}+B^{eo}_{qp1}y_{i2}+B^{oo}_{qp1}y_{i7}+A^{eo}_{qp2}y_{i5}+A^{oo}_{qp2}y_{i,10} \\ \hat{y}_{i9} &= y_{i9}+A^{eo}_{qp1}y_{i2}+A^{oo}_{qp1}y_{i7} \end{aligned} \tag{5.36}$$

In eqns. 5.35 and 5.36, $\hat{y}_{ij}$ represents an element of the modified DAM corresponding to the element y_{ij} in 5.34, which is changed after inserting the constraint equations. The row designate i spans the rows 1,2,5,6,7 and 10 in eqn. 5.34 while the column designate j spans the columns 1,3,4,6,8 and 9 in eqn. 5.34.

Note that in the renumbered columns of (5.35) the numbers $1,5,7,1^o,5^o,7^o$ correspond respectively to V^e_{in}, V^e_{q2}, V^e_{q1}, V^o_{in}, V^o_{q2}, V^o_{q1} Invoking the S/H restrictions for the input, used in [49], we shall have $V^o_{in} = z^{-1/2}V^e_{in}$. Further, by virtue of $v_{in}(t) = v_{inI}$ in the CCEs, one would have $C^{ee}_{inp1} = C^{eo}_{inp1} = 0$, $B^{ee}_{ap2} = 0 = B^{eo}_{ap2}$. Using these facts, one can reduce the matrix in eqn. 5.35 further by adding column 1^o multiplied by $z^{-1/2}$ to column 1 and discarding column 1^o and row 1^o and row 1^o thereafter. The result is a 5 by 5 matrix, say Y_F. The voltage transfer function is given by

$$H^{ee}(z) = \frac{V^e_{q2}}{V^e_{in}} = \frac{\Delta_{12}}{\Delta_{11}}, \text{ where } \Delta_{ij} \text{ is the } (i,j)^{th} \text{ cofactor of } Y_F.$$

Substituting expression for the various cofactors, one can obtain the analytic expression for $H^{ee}(z)$.

At this point one may observe that if an analytic expression is not required and only numerical results are wanted, then one can computerize the entire process once the constraint equations around each OA have been derived.

5.3.3 A Second Order SCF Based on UGAs

As a third example of application of the analysis method, we consider a SC BPF using UGAs as developed in Chapter 4. This is a network (Fig. 5.4) containing two UGAs and the subnetworks (N_{s1}, N_{s2}) are outlined by broken lines. Consider Figs. 5.5(a)-(b) which show the network topologies pertaining to the 'even' and 'odd' phases of the clock signal in N_{s1} (around UGA1) including the relevant parasitic capapcitances lumped according to the principles discussed in Chapter 4. Similarly, Figs. 5.5(c)-(d) show the topologies during the "even" and "odd" phases in the subnetwork N_{s2} (around UGA2). Now considering Fig. 5.5(a), the CCE around the input node of UGA1 in the even phase $[(n - \frac{1}{2})T < t \leq nT]$ is given by

$$v_{p1}(t) = \alpha_{1a1}v_s(t) + \beta_{1a1}v_{sI} + \beta_{1x1}v_{xI} \tag{5.37a}$$

where

$$\alpha_{1a1} = C_1/C_{SUM1}$$

$$\beta_{1a1} = -\alpha_{1a1} \tag{5.37b}$$

$$\beta_{1x1} = 1$$

and $C_{SUM1} = C_1 + C_{s1} + C_{p1} + C_{A1}$

Recalling eqn. (5.2) and recognizing that for UGA1 $\beta = B_1$, the bandwidth and $\alpha = \alpha_{o1}B_1$ where α_{o1} is the DC gain (~1) of the UGA, one would have

$$\frac{dv_{q1}}{dt} + B_1 v_{q1} = \alpha\alpha_{1a1}v_s + \alpha\beta_{1a1}v_{sI} + \alpha\beta_{1x1}v_{xI} \tag{5.38}$$

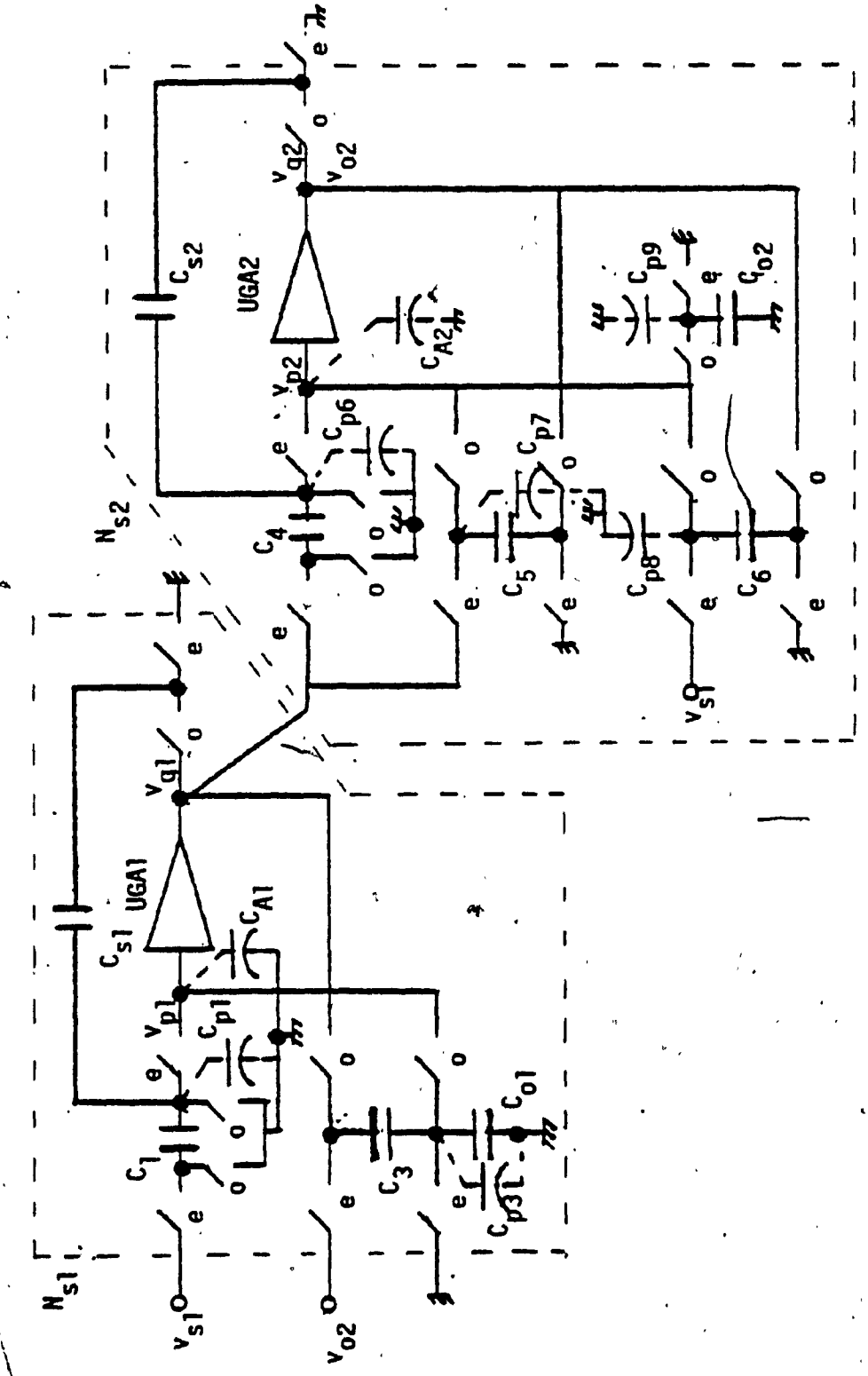


Figure 5.4: The SC BPF using UGAs

which on solving, as before, will give for $v_{p1}(nT)$, the expression

$$v_{p1}(n) = A_{11}v_s(n) - \frac{A_{11}}{1 - L_{11}} v_s(n) + \frac{A_{11}L_{11}}{1 - L_{11}} v_s(n - \tfrac{1}{2})$$

$$+ \frac{k_{11} / \alpha}{1 - L_{11}} v_{q1}(n) - \frac{(k_{11} / \alpha)L_{11}}{1 - L_{11}} v_{q1}(n - \tfrac{1}{2})$$

where

$$A_{11} = \alpha_{1a1}$$

$$k_{11} = B_1$$

and $$L_{11} = \exp(-k_{11}T/2) \qquad (5.40)$$

Taking $\mathcal{Z}$-transforms on both sides will give

$$V^e_{p1} = B^{ee}_{11}V^e_s + B^{eo}_{11}V^o_s + A^{ee}_{11}V^e_{q1} + A^{eo}_{11}V^o_{q1} \qquad (5.41a)$$

where

$$B^{ee}_{11} = - \frac{\alpha_{1a1}L_{11}}{1 - L_{11}}$$

$$B^{eo}_{11} = -B^{ee}_{11}z^{-1/2}$$

$$A^{ee}_{11} = \frac{1}{1 - L_{11}} \frac{1}{\alpha_{o1}} \qquad (5.41b)$$

$$A^{eo}_{11} = - A^{ee}_{11}L_{11}z^{-1/2}$$

Considering, again, the CCE around the input node of UGA1 during the "odd" phase [Fig. 5.5(b)] [$nT - T < t < (n - \frac{1}{2})T$], one shall have

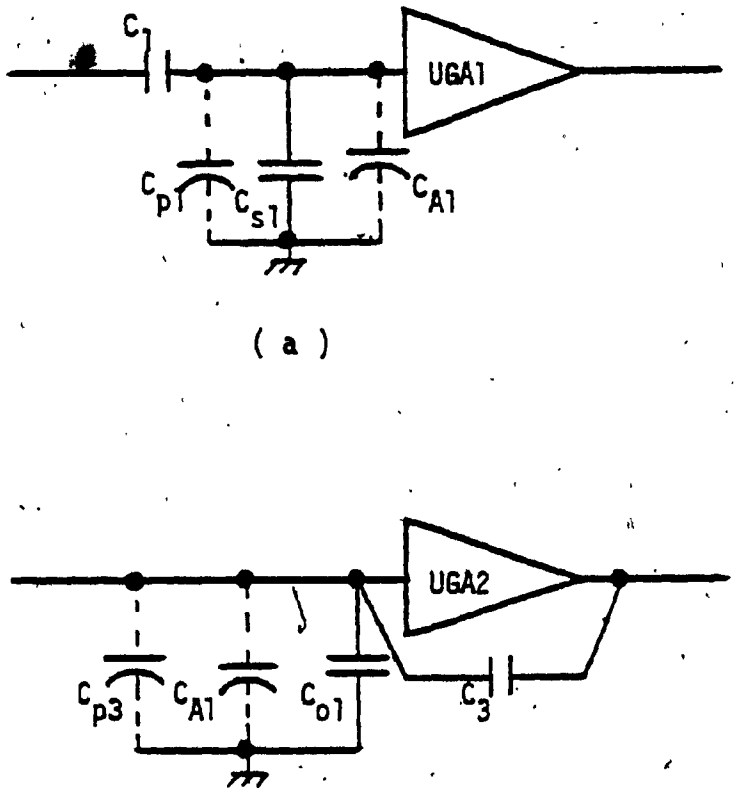


Figure 5.5: (a),(b) The subnetworks around UGA1 during 'even' and 'odd' phases respectively

$$v_{p1}(t) = \alpha_{2q1} v_{q1}(t) + \beta_{2q1} v_{q1I} + v_{p1I} \tag{5.42a}$$

where

$$\alpha_{2q1} = C_3/C_{SUM2}$$

$$\beta_{2q1} = -\alpha_{1q2}$$

$$C_{SUM2} = C_3 + C_{o1} + C_{p3} + C_{A1}$$

Combining eqn. 5.42a with the DE of the UGA, one has

$$\frac{dv_{q1}}{dt} + (B_1 - \alpha_{2q1}\alpha)v_{q1} = \alpha(\beta_{2q1} v_{q1I} + v_{p1I}) \tag{5.43}$$

Using $k_{21} = B_1 - \alpha\alpha_{2q1}$, $L_{21} = \exp(-k_{21}T/2)$, one will have

$$v_{p1}(n - \tfrac{1}{2}) = \frac{(k_{21/\alpha} + \alpha_{2q1})}{1 - L_{21}} v_{q1}(n - \tfrac{1}{2}) - \frac{k_{21/\alpha}}{1 - L_{21}} L_{21} v_{q1}(n - 1) \tag{5.44}$$

Taking $\mathcal{Z}$-transforms on both sides

$$V^o_{p1} = A^{oo}_{21} V^o_{q1} + A^{oe}_{21} V^e_{q1} \tag{5.45a}$$

where $A^{oo}_{21} = (1/\alpha_{o1} - \alpha_{2q1} L_{21})/(1 - L_{21})$

$$A^{oe}_{21} = -(\frac{1}{\alpha_{o1}} - \alpha_{2q1}) \frac{L_{21}}{1 - L_{21}} \tag{5.45b}$$

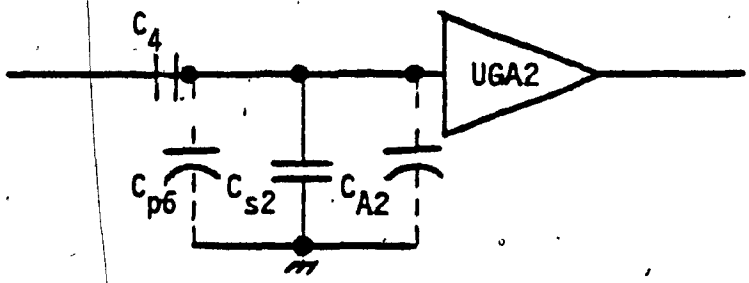
For UGA2 one can carry out a similar procedure to obtain

$$V^e_{p2} = A^{ee}_{12} V^e_{q2} + A^{eo}_{12} V^o_{q2} + B^{ee}_{12} V^e_{q1} + B^{eo}_{12} V^o_{q1} \tag{5.46}$$

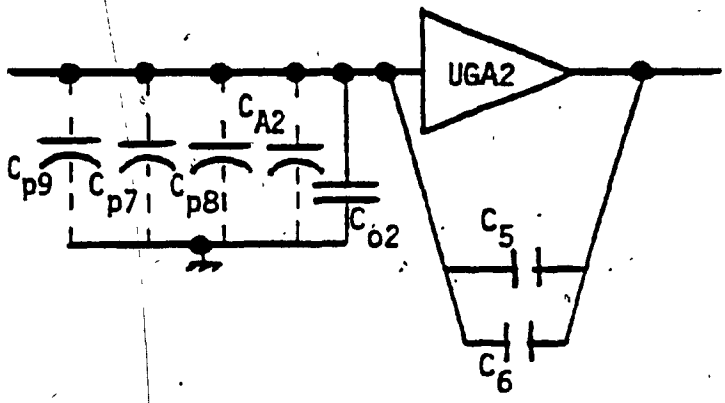
$$V^o_{p2} = A^{oo}_{22} V^o_{q2} + A^{oe}_{22} V^e_{q2} \tag{5.47}$$

where

$$k_{12} = B_2$$



(c)



(d)

Figure 5.5: (c),(d) The subnetworks around UGA2 during 'even' and 'odd' phases respectively

$$L_{21} = \exp(-k_{12}T/2)$$

$$A_{12}^{ee} = \frac{1}{1 - L_{21}} \frac{1}{\alpha_{o2}}$$

$$A_{12}^{ee} = -A_{12}^{ee} L_{21} z^{-1/2} \qquad (5.48)$$

$$B_{12}^{ee} = -\alpha_{1a2} L_{21} / (1 - L_{21})$$

$$B_{12}^{eo} = -B_{12}^{ee} z^{-1/2}$$

$$\alpha_{1a2} = C_4 / C_{SUM3}$$

$$C_{SUM3} = C_4 + C_{s2} + C_{p6} + C_{A2}$$

In eqn. 5.48, B_2 is the bandwidth of UGA2 and α_{02} is the low frequency gain of the UGA2. The parameters in eqn. 5.47 are given by

$$k_{22} = B_2 - \tilde{\alpha}\alpha_{2q2}, \quad \tilde{\alpha} = \alpha_{o2}B_2$$

$$L_{22} = \exp(-k_{22}T/2)$$

$$A_{22}^{oo} = (1/\alpha_{02} - \alpha_{2q2}L_{22}) / (1 - L_{22}) \qquad (5.49)$$

$$A_{22}^{oe} = -(1/\alpha_{02} - \alpha_{2q2}) L_{22} / (1 - L_{22})$$

$$\alpha_{2q2} = (C_5 + C_6) / C_{SUM4}$$

$$C_{SUM4} = C_5 + C_6 + C_{o2} + C_7 + C_{p8} + C_{p9} + C_{A2}$$

Eqns. 5.41a, 5.45a, 5.46, 5.47 are the constraint equations in the z-domain which are to be used in the IAM for the network on hand in the same manner as before. The details are omitted to avoid repetition.

5.4 EXTENSION TO THE CASE OF MULTIPHASE SC NETWORKS

In this section, the above analysis technique is extended to the case of SC networks operated by a multiphase clock signal and containing ADs of finite (DC) gain and finite bandwidth. Multiphase clock signals have been used in SC networks based on OAs [25],[51],[52] to eliminate a number of non ideal effects (e.g., parasitic capacitance, offset voltage due to clock feedthrough) associated with switches and capacitors. The analysis technique proposed in this section is expected to be useful in this regard.

5.4.1 Analysis

Let us consider an SC network N containing a number of ADs, switches and capacitors, operated by an M phase clock signal of durations τ_1, τ_2, ... with a fundamental clock period $T = \sum_{i=1}^{M} \tau_i$. We first set out with the time domain part of the analysis. For this, one has to identify around each AD (say the i^{th}) a subnetwork (say N_{si}) such that N_{si}(i) contains the input and output nodes of AD_i and (ii) all the other nodes of N_{si} contribute to charge flow directly to the input node of AD_i through switched or unswitched capacitors. For convenience of understanding, one may represent N_{si} as in Fig.5.6(a). In Fig. 5.6(a), the nodes a,b, ... are the collection of **intermediate nodes**, p_i and q_i are the input and ouput nodes of AD_i. A typical sequence of the M phase clock signals is shown in Fig. 5.6(b). During each clock phase, say phase 1, of duration τ_1, one can identify the transition subinterval ε and the phase sub interval I_p as shown in Fig.

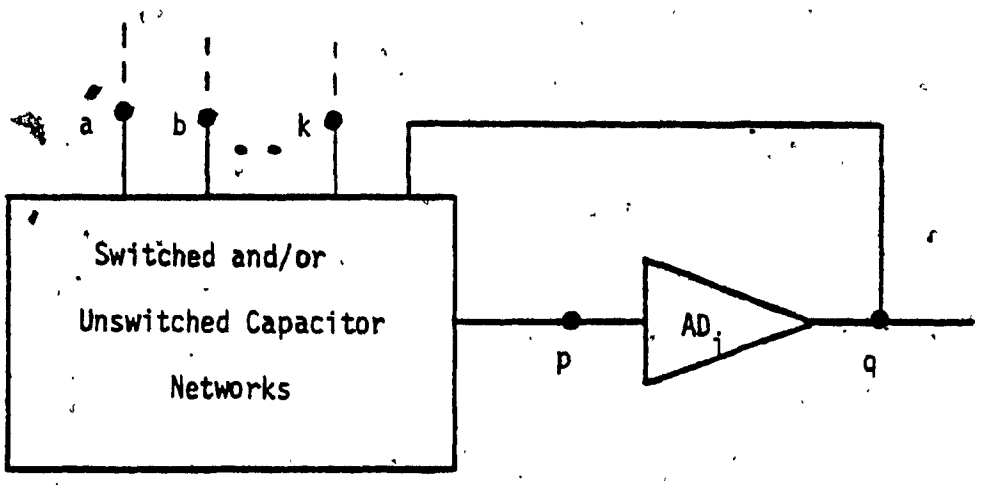


Figure 5.6 : (a) A subnetwork N_{si} around an active device (AD_j) in a multiphase SC network

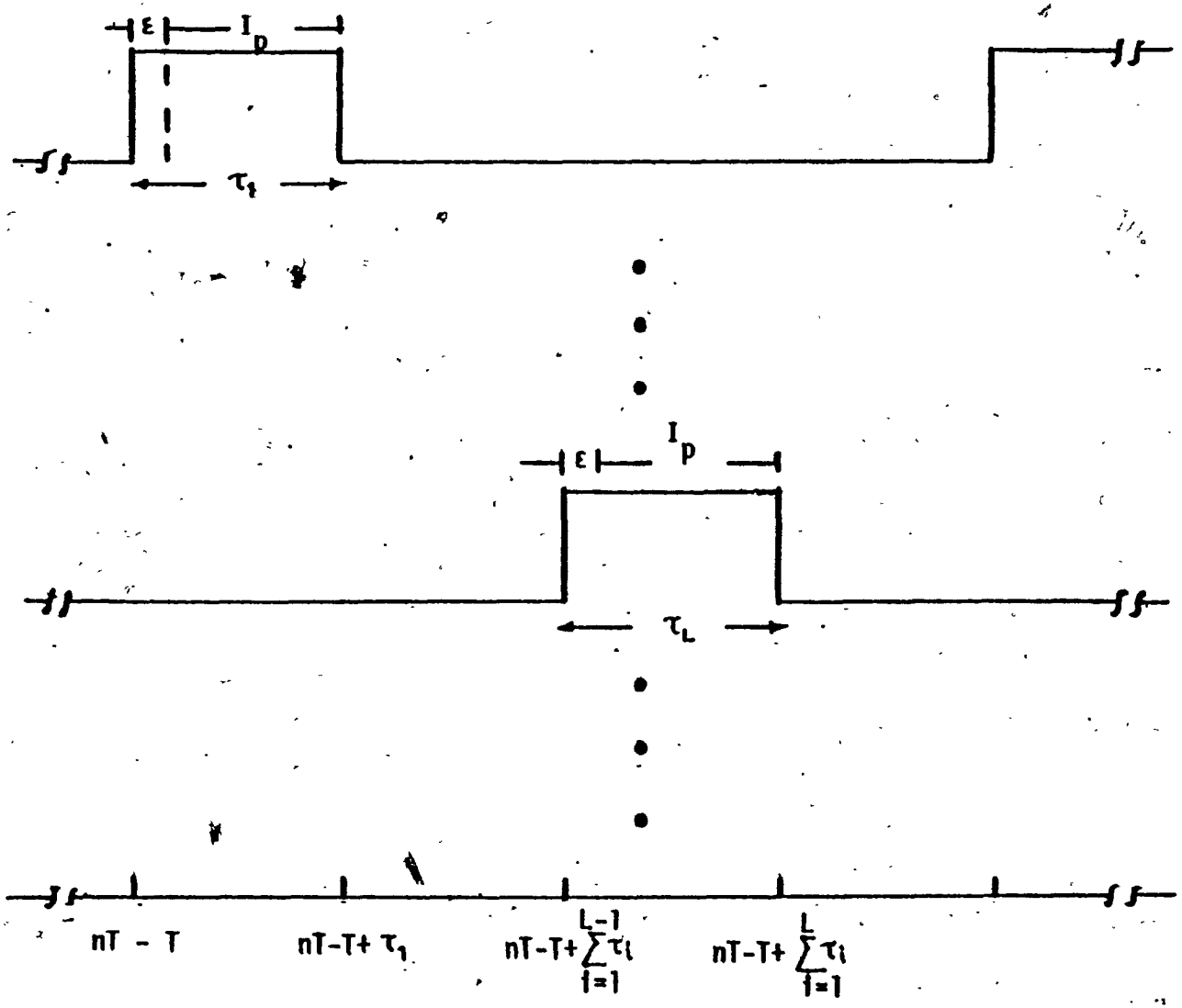


Figure 5.6: (b) , (c) The multiphase clock signal and the phase and transition subintervals (I_p and ε)

5.6(c). According to our previous discussions, I_p is the sub interval when a linear CCE can be written down with regard to the voltages at the various nodes in N_{si}.

Consider now the L^{th} clock phase of duration τ_L with the phase interval defined over $(nT-T+\sum_{i=1}^{L-1}\tau_i+\varepsilon,\ nT-T+\sum_{i=1}^{L}\tau_i)$ [see Fig. 5.6(b)]. Over this interval, the voltage $v_p^{(i)}(t)$ at the input node p_i of AD_i can be expressed using the CCE as:

$$v_{pL}^{(i)}(t) = \alpha_{qL}^{(i)}\, v_{qL}^{(i)}(t) + \sum_j \alpha_{jL}^{(i)} v_{jL}^{(i)}(t) + \sum_k \beta_{kL} v_{kLI} \qquad (5.50)$$

In the above, the superscript (i) represents parameters pertaining to the subnetwork N_{si} around the i^{th} active device. The subscript j in $\sum_j$ represents all the intermediate nodes in N_{si} while the subscript k in $\sum_k$ represents all the nodes in N_{si} (i.e., the intermediate nodes as well as the input and output nodes p_i, q_i of AD_i). Further, $v_{kLI} = v_k(nT - T + \Delta_1)$, with $\Delta_1 = \sum \tau_i + \varepsilon$ and $\varepsilon \to 0$, represent the initial values of the node voltage(s) in N_{si} at the onset of phase L of the clock signal. For compactness we shall represent:

$$t_1 = nT-T+\Delta_1,\ t_2 = t_1+\tau_L,\quad \sum_j \alpha_{jL}^{(i)}\, v_{jL}^{(i)}(t) = \tilde{A}_{iL}\tilde{v}_{iL}(t)$$

and $$\sum_k \beta_{kL}\, v_{kLI} = \tilde{B}_{iL}\tilde{v}_{iLI}$$

where $\tilde{A}_{iL}$, $\tilde{B}_{iL}$ are row vectors and $\tilde{v}_{iL}(t)$, $\tilde{v}_{iLI}$ are column vectors, corresponding to the subnetwork N_{si} around the i^{th} AD and the L^{th} phase of the clock signal. As before, we shall assume a first order gain function. $A^{(i)}(s) = \omega_{ti}/(s + \omega_{ci})$ for the i^{th} AD where ω_{ci} is the

bandwidth of the AD and $\omega_{ti} = \alpha_{oi}\omega_{ci}$ where α_{oi} is the low frequency gain. The above gain model leads to the DE

$$\frac{dv_{qL}^{(i)}}{dt} + \omega_{ci} v_{ql}^{(i)} = \omega_{ti} v_{pL}^{(i)} \tag{5.52}$$

This, combined with eqn (5.50), leads to

$$\frac{dv_{qL}^{(i)}}{dt} + k_L^{(i)} v_{qL}^{(i)} = \omega_{ti} \tilde{A}_{iL} \tilde{v}_{iL} + \omega_{ti} \tilde{B}_{iL} v_{iLI} \tag{5.53a}$$

$$\text{where } k_L^{(i)} = \omega_{ci} - \omega_{ti}\alpha_{qL}^{(i)} \tag{5.53b}$$

Eqn. (5.53a) can be solved over the interval (t_1, t_2) defined in eqn. (5.51) as was done for the case of an SC network operated by a two-phase clock signal. Thus under the assumption that each component in $\tilde{v}_{iL}$ is relatively stationary over the phase interval (t_1, t_2) compared to its associated exponential function, one shall have

$$\tilde{B}_{iL}\tilde{v}_{iLI} = \frac{k_L^{(i)}}{\omega_{ti}[1-\lambda_L^{(i)}]} v_{qL} - \frac{k_L^{(i)}\lambda_L^{(i)}}{\omega_{ti}[1-\lambda_L^{(i)}]} v_{q,L-1}$$

$$- \frac{\tilde{A}_{iL}\lambda_L^{(i)}}{1-\lambda_L^{(i)}} \tilde{v}_{i,L} + \frac{\tilde{A}_{iL}\lambda_L^{(i)}}{1-\lambda_L^{(i)}} \tilde{v}_{1,L-1} \tag{5.54}$$

where we have used $v_{x,L-1} = v_x(t_1)$, $x = q,i$ and $\varepsilon \to 0$ and $\lambda_L^{(i)} = \exp(-k_L^{(i)}\tau_L)$. Writing $t_2 = t_2$ in eqn 5.50 and using eqn. 5.54 one then shall have

$$v_{p,L}^{(i)} = \frac{1/\alpha_{oi} - \alpha_{qL}^{(i)}\lambda_L^{(i)}}{1 - \lambda_L^{(i)}} v_{q,L} - \frac{\lambda_L^{(i)}}{1-\lambda_L^{(i)}} \left[\frac{1}{\alpha_{oi}} - \alpha_{qL}^{(i)}\right] v_{q,L-1}$$

$$- \frac{\mathcal{A}_{i,L}\,\lambda_L^{(i)}}{1-\lambda_L^{(i)}}\,\tilde{v}_{i,L} + \frac{\mathcal{A}_{i,L}\lambda_L^{(i)}}{1-\lambda_L^{(i)}}\,\tilde{v}_{i,L-1} \qquad (5.55)$$

Let us assume now that clock phases are of equal duration, i.e., $\tau_1 = \tau_2 = \ldots \tau_k = \ldots = \tau = T/M$. In that case, one can take $\mathcal{Z}$-transform on both sides of eqn. 5.55 and have

$$V_{p,L}^{(i)}(z) = A_{L,L} V_{q,L}^{(i)}(z) + A_{L,L-1}\, z^{-1/M}\, V_{q,L-1}^{(i)}(z)$$

$$+ \mathcal{C}_{L,L}\,\tilde{V}_{i,L}(z) + \mathcal{C}_{L,L-1}\, z^{-1/M}\,\tilde{V}_{i,L-1}(z) \qquad (5.56)$$

where $V_x(z) = \mathcal{Z}[v_x(nT)]$

$$V_{x,L}(z) = \mathcal{Z}[v_x\{nT - (M-L)\tau\}] = \mathcal{Z}[v_x(nT - \tfrac{M-L}{M}T)]$$

$x = p,q,i$

$$A_{L,L} = [\frac{1}{\alpha_{oi}} - \alpha_{qi}^{(i)}\lambda_L^{(i)}] \,/\, (1-\lambda_L^{(i)})$$

$$A_{L,L-1} = -\frac{\lambda_L^{(i)}}{1-\lambda_L^{(i)}}[\frac{1}{\alpha_{oi}} - \alpha_{qL}^{(i)}] \qquad (5.57)$$

$$\mathcal{C}_{L,L} = -\frac{\mathcal{A}_{iL}\lambda_L^{(i)}}{1-\lambda_L^{(i)}} = -\mathcal{C}_{L,L-1}$$

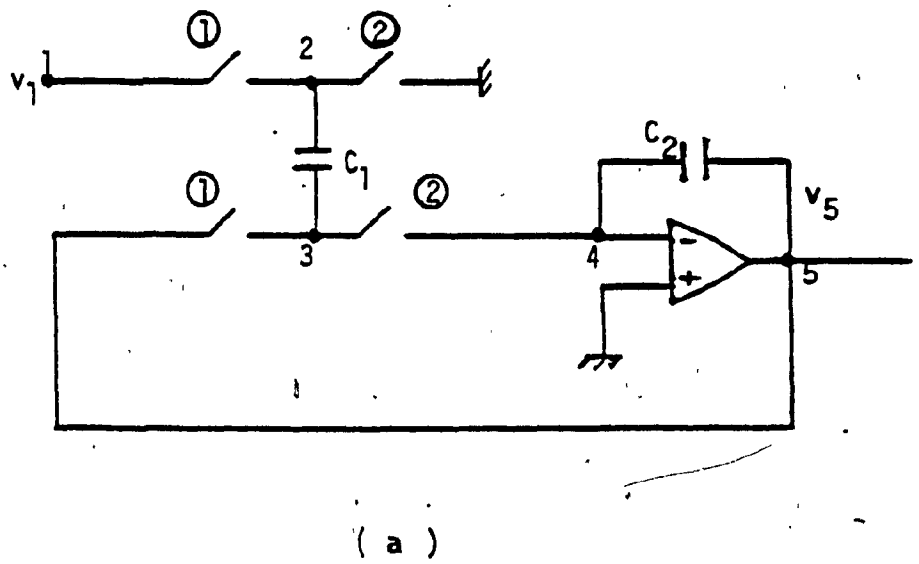
It may be remarked that by virtue of the periodicity of the clock phases, L-1 is equivalent to M when L = 1. It may be mentioned that if a certain element (say the j^{th} element in $\tilde{V}_{i,L}$) is a sampled and held voltage, one would have $V_{j,L}(z) = z^{-1/M}\, V_{j,L-1}(z)$ making the corresponding elements to cancel out in the expression for $\mathcal{C}_{L,L}\,\tilde{V}_{i,L}(z) + \mathcal{C}_{L,L-1}V_{i,L-1}(z)$ in eqn. 5.56 (because $\mathcal{C}_{L,L} = -\mathcal{C}_{L,L-1}$ by eqn. 5.57).

Reverting finally to the scalar notations as in eqn. 5.50, one can write

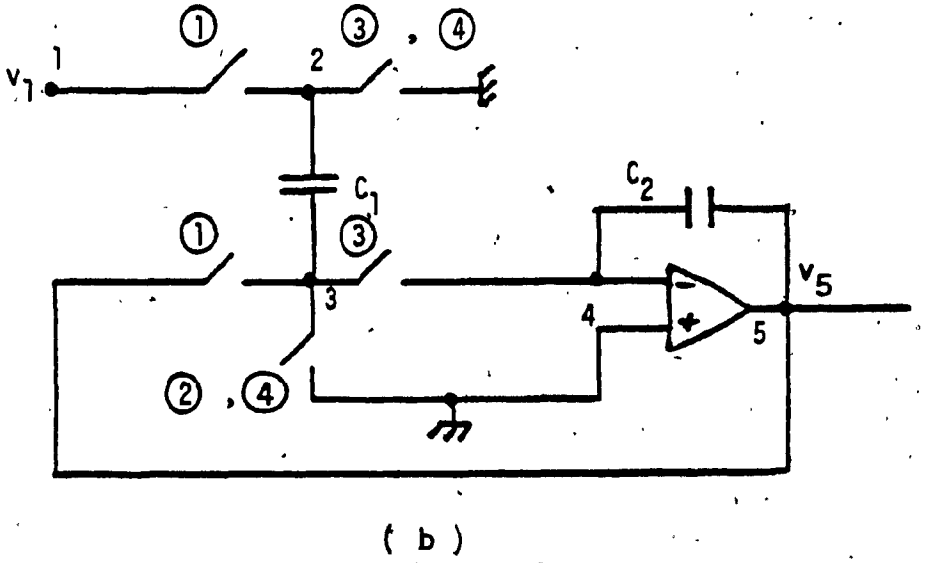
$$V_{p,L}^{(i)}(z) = A_{L,L}^{(i)} V_{q,L}^{(i)}(z) + A_{L,L-1}^{(i)} V_{q,L-1}^{(i)}(z)\, z^{-1/M} + \frac{\lambda_L^{(i)}}{1-\lambda_L^{(i)}} \sum_j \alpha_{jL}^{(i)} \left(V_{j,L}(z) - V_{j,L-1}(z) z^{-1/M}\right) \qquad (5.58)$$

where $\sum_j$ covers all the intermediate nodes in N_{si}. Eqn. (5.58) represents the constraint equation that exists between the node voltage at the input of the i^{th} AD and the voltages at other nodes of the subnetwork N_{si} during the L^{th} phase of the clock signal. Similar expressions can be arrived at for each of the clock phases and for all the other subnetworks around all other ADs in the active SC network. This would complete the time domain part of the analysis for the entire SC network at hand.

As was the case with an SC network with biphase clock, the rest of the analysis for the multiphase case is rather straightforward and follows very much in the same manner with the only difference that the multiphase indefinite admittance matrix (M-IAM)[53] descritpion of the passive part of the SC network is to be employed now. The entire analytical procedure can be easily understood by considering a simple network and is illustrated in the following section.



(a)



(b)

Figure 5.7 : (a) An OA based differential integrator operated by a two phase clock, (b) The OA based DI operated by a four phase clock

5.4.2 Illustration of the Method for a Four-phase Differential Integrator

Consider Fig. 5.7(a) which shows a differential integrator (DI). With a two phase clocking scheme, the voltage transfer function of the circuit remains sensitive to parasitic capacitances. If, however, a four phase clocking scheme is used as in Fig. 5.7(b), the voltage transfer function, with ideal OA is given by

$$\frac{V_5(z)}{V_1(z)} = \frac{C_1}{C_2} \frac{z^{-1}}{1 - \frac{C_2 - C_1}{C_2} z^{-1}} \tag{5.59}$$

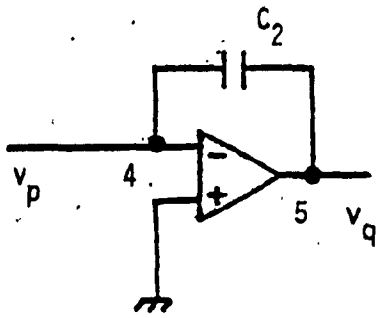
which is insensitive to parasitics. It is immediately apparent that this DI with a 4-phase clocking scheme may serve as a useful building block for realizing second order transfer functions which are parasitic insensitive as well as canonic so far as the number of capacitors are concerned. We shall, however, restrict our analysis to the DI itself when the OA has a finite DC gain A_{o1} and a finite gain bandwidth product value ω_{t1}.

The DI is a typical example of a single OA circuit. There is only one subnetwork and its parts during the various clock phases relevant to writing down the CCEs are as shown in Figs. 5.8(a)-(d). Considering these networks successively, one can write down the following CCEs:

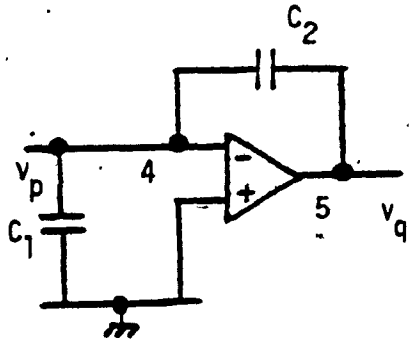
Phase 1: $(n-1)T < t < (n-\frac{3}{4})T$

$$C_2 v_{p1}(t) - C_2 v_{q1}(t) - C_2 v_{p1I} + C_2 v_{q1I} = 0$$

$$\text{or} \quad v_{p1}(t) = v_{q1}(t) - v_{q1I} + v_{p1I} \tag{5.60a}$$



(a),(b) and (d)



(c)

Figure 5.8 : The subnetwork topologies in the DI during the four phases of the clock ; (a),(b) and (d) for phases 1,2,4 and (c) for phase 3

Phase 2: $(n - \frac{3}{4})T < t < (n - \frac{1}{2})T$

$$v_{p2}(t) = v_{q2}(t) - v_{q2I} + v_{p2I} \tag{5.60b}$$

Phase 3: $(n - \frac{1}{2})T < t < (n - \frac{1}{4})T$

$$C_1[v_{p3}(t) - v_{p3I}] = C_2[v_{q3}(t) - v_{q3I}] - C_2[v_{q3I} - v_{p3I}]$$

or
$$v_{p3}(t) = \alpha_{q3}v_{q3}(t) + \beta_{q3}v_{q3I} + \beta_{p3}v_{p3I} \tag{5.60c}$$

where $\alpha_{q3} = C_2/(C_1 + C_2)$, $\beta_{q3} = -\alpha_{q3}$, $\beta_{p3} = 1$

Phase 4: $(n - \frac{1}{4})T < t < nT$

$$v_{p4}(t) = v_{q4}(t) - v_{q4I} + v_{p4I} \tag{5.60d}$$

In writing eqns. 5.60(a)-(d), we have omitted the superscript (1) for simplicity.

On comparing the various CCEs above with the general form (eqn. 5.50), one can visualize that the part $\sum_j \alpha_{jL}^{(i)} v_{jL}^{(i)} \equiv \tilde{A}_{iL}\tilde{v}_{iL}(t)$ is absent in all the eqns. 5.60(a)-(d). Now using the one pole model for the gain function of the OA (used here as an inverting amplifier with positive input terminal grounded), viz., $A(s) = -(A_{01}\omega_{c1})/(s+\omega_{c1})$ one can arrive at the following constraint equations:

$$\begin{aligned}
V_{p,1}(z) &= A_{1,1}V_{q,1}(z) + A_{1,4}z^{-\frac{1}{4}}V_{q,4}(z) \\
V_{p,2}(z) &= A_{2,2}V_{q,2}(z) + A_{2,1}z^{-\frac{1}{4}}V_{q,1}(z) \\
V_{p,3}(z) &= A_{3,3}V_{q,3}(z) + A_{3,2}z^{-\frac{1}{4}}V_{q,2}(z) \\
V_{p,4}(z) &= A_{4,4}V_{q,4}(z) + A_{4,3}z^{-\frac{1}{4}}V_{q,3}(z)
\end{aligned} \tag{5.61}$$

where

$$A_{1,1} = -(\lambda_1 + 1/A_{o1}) \,/\, (1-\lambda_1)\,,\; A_{1,4} = \lambda_1(1+1/A_{o1}) \,/\, (1-\lambda_1)$$

$$A_{2,2} = -(\lambda_2+1/A_{o1}) \,/\, (1-\lambda_2)\,,\; A_{2,1} = \lambda_2(1+1/A_{o1}) \,/\, (1-\lambda_2) \tag{5.62}$$

$$A_{3,3} = -(\lambda_3\alpha_{q3}+1/A_{O1}) \,/\, (1-\lambda_3),\; A_{3,2} = \lambda_3(\alpha_{q3}+1/A_{01}) \,/\, (1-\lambda_3)$$

$$A_{4,4} = -(\lambda_4+1/A_{o1}) \,/\, (1-\lambda_4)\,,\; A_{4,3} = \lambda_4(1+1/A_{o1}) \,/\, (1-\lambda_4)$$

and

$$\lambda_1 = \exp\left[-\frac{\omega_{t1}T}{4}(1+1/A_{o1})\right] = \lambda_2 = \lambda_4$$

$$\lambda_3 = \exp\left[-\frac{\omega_{t1}T}{4}(\alpha_{q3} + 1/A_{o1})\right] \tag{5.63}$$

Eqns. 5.61-5.63 are the outcome of the time domain part of the analysis. The IAM of the passive part (i.e., on removing the OA) of the circuit in Fig. 5.6(b) can be written down by simple inspection in the manner already suggested[53]. After allowing for the switch contractions and elimination of the rows and columns corresponding to ground node(s), the definite admittance matrix of the SC circuit becomes as Y_m, shown in eqn. 5.64. In this we have used $G_x = C_x/\tau$, $S_x = -z^{-1/4}G_x$ and $x = 1,2$. It may be pointed out that the nodes numbered 4 and 5 in Y_m correspond to nodes 'p' and 'q' in our analytical formulae. Also the node groups for each phase of the clock signal have been clearly distinguished in eqn. 5.64. This makes it easy to apply the constraint eqn. 5.61 to Y_m to obtain the final

Phase		①			②			③		④	
		1	4	5	2	4	5	4	5	4	5
①	1	G_1	0	$-G_1$	0	0	0	0	0	0	0
	4	0	G_2	$-G_2$	0	0	0	0	0	S_2	$-S_2$
	5	$-G_1$	$-G_2$	G_1+G_2	0	0	0	0	0	$-S_2$	S_2
②	2	S_1	0	$-S_1$	G_1	0	0	0	0	0	0
	4	0	S_2	$-S_2$	0	G_2	$-G_2$	0	0	0	0
	5	0	$-S_2$	S_2	0	$-G_2$	G_2	0	0	0	0
③	4	0	0	0	$-S_1$	S_2	$-S_2$	G_1+G_2	$-G_2$	0	0
	5	0	0	0	0	$-S_2$	S_2	$-G_2$	G_2	0	0
④	4	0	0	0	0	0	0	S_2	$-S_2$	G_2	$-G_2$
	5	0	0	0	0	0	0	$-S_2$	S_2	$-G_2$	G_2

(5.64)

Phase		①		②		③	④
		1≡2	5	2	5	5	5
①	1≡2	G_1	$\hat{y}_{12}$	0	$\hat{y}_{14}$	$\hat{y}_{15}$	$\hat{y}_{16}$
	4	0	$\hat{y}_{22}$	0	$\hat{y}_{24}$	$\hat{y}_{25}$	$\hat{y}_{26}$
②	2	S_1	$\hat{y}_{32}$	G_1	$\hat{y}_{34}$	$\hat{y}_{35}$	$\hat{y}_{36}$
	4	0	$\hat{y}_{42}$	0	$\hat{y}_{44}$	$\hat{y}_{45}$	$\hat{y}_{46}$
③	4	0	$\hat{y}_{52}$	$-S_1$	$\hat{y}_{54}$	$\hat{y}_{55}$	$\hat{y}_{56}$
④	4	0	$\hat{y}_{62}$	0	$\hat{y}_{64}$	$\hat{y}_{65}$	$\hat{y}_{66}$

(5.65)

DAM(Y_F) of the active SC network that contains an OA with finite DC gain and finite gain bandwidth value. The modified matrix Y_F is shown in eqn 5.65 where the modified elements (because of the constraint equations) have been designated with a hat ($\hat{}$) on top of it. Taking any given row (say the row for node 4 in phase 1) one can easily see that:

$$\hat{y}_{22} = -G_2 + A_{1,1}G_2 \; , \; \hat{y}_{24} = 0 \; , \; \hat{y}_{25} = A_{4,3}z^{-1/4}S_2 \text{ and}$$

$$\hat{y}_{26} = S_2 - A_{4,4}\,S_2 - A_{1,4}z^{-1/4}G_2$$

The other elements of Y_F can be similarly found out. The voltage transfer function $[V_{5,1}(z) \; / \; V_{1,1}(z)]$ is given by Δ_{12}/Δ_{11} where Δ_{ij} is the cofactor of the i^{th} row and j^{th} column of Y_F. It is easy to see that once the parameters α_{q3}, λ_1, λ_3 have been determined, the rest of the analytical procedure can be easily computerized for numerical simulations.

5.5 STEP-BY-STEP ANALYSIS PROCEDURE

In order to aid systematic application of the technique developed in this chapter, the analysis procedure is summarized below in a number of sequential steps.

(i) Identify the subnetworks N_{si} (i = 1,2,...) around each AD in the original SC network N.

(ii) Set up the CCE for the input node of the AD for a given

phase (say, L) in N_{si}.

(iii) Identify the coefficients α_{qL}, α_{jL}, β_{kL}, ... etc., in the CCE in terms of the ratios of capacitances in the circuit see eqn. 5.50 .

(iv) Obtain the parameter $\lambda_L^{(i)}$ through $k_L^{(i)}$ using the given equations.

(v) Obtain the constraint equations for this given phase yielding the coefficients $A_{L,L}$, $A_{L,L-1}$, $\tilde{C}_{L,L}$, $\tilde{C}_{L,L-1}$... etc.

(vi) Repeat steps (iii) through (v) for other clock phases in N_{si} yielding the parameters $\lambda_{L+1}^{(i)}$, $k_{L+1}^{(i)}$, $A_{L+1,L+1}$, ... etc.

(vii) Repeat steps (ii) through (vi) for other subnetworks N_{sj}s ($j \neq i$) around all other ADs.

(viii) Obtain the passive part of the given active SC network by removing all the ADs. From the IAM of this passive network (M-IAM for M phase clock), obtain the DAM after allowing for node contractions due to switching and elimination of ground nodes.

(ix) Apply the constraints arrived at in step (vii) to the

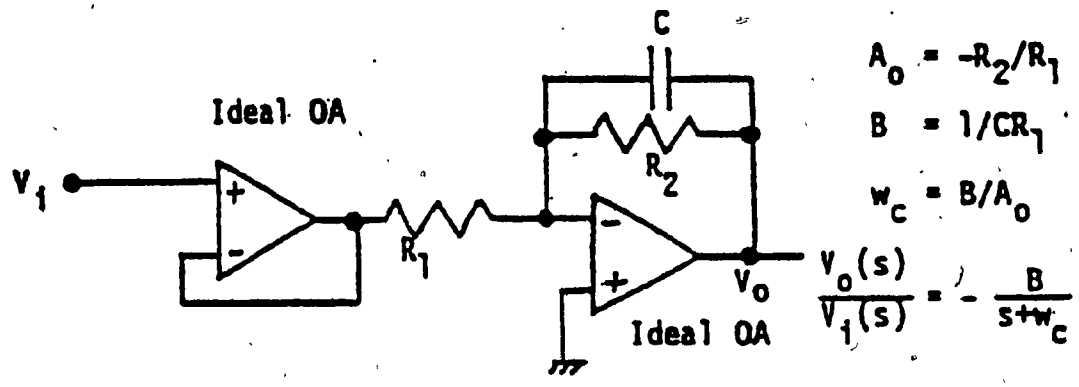


Figure 5.9: Macromodel for an OA with finite dc gain (A_o) and finite gain-bandwidth (B) value

DAM in step (vii) to modify pertinent columns. Subsequently, eliminate the columns corresponding to the AD input node(s) and discard the rows corresponding to the AD output node(s). This gives the final reduced DAM (Y_F) of the active SC network.

(x) Subject Y_F obtained as above to standard matrix operations to obtain the desired network function (e.g. voltage transfer function, transfer impedance etc.).

5.6 RESULTS

5.6.1 Experimental Investigation with OAs, Discrete Capacitors and Switches

The circuit of Fig. 5.3 was experimentally investigated in the laboratory using discrete capacitors, CMOS switches (RCA 4066B) and μA741 Op.Amps. The capacitors were polysterene film/foil type with ±10% tolerance. The experiments were carried out of Q_p = 5 and 25, A_o = 100 and 1000, and GB of 35.6kHz, 106kHz with f_p = 1000 Hz and f_s = 10,000 Hz. The finite DC gain and GB(s) were simulated using the macromodel shown in Fig. 5.9. Results were also taken for the typical values of $A_o(\sim 10^5)$ and GB(~1 MHz) for the OAs using the OAs themselves in the circuit instead of the macromodels. The results corresponding to Q_p = 25 are shown in Fig. 5.10. The solid curves show the theoretical results while the symbols ●, ○, ■, □, + represent the experimental values (ref. legend for the symbols in Fig. 5.10). The experimental

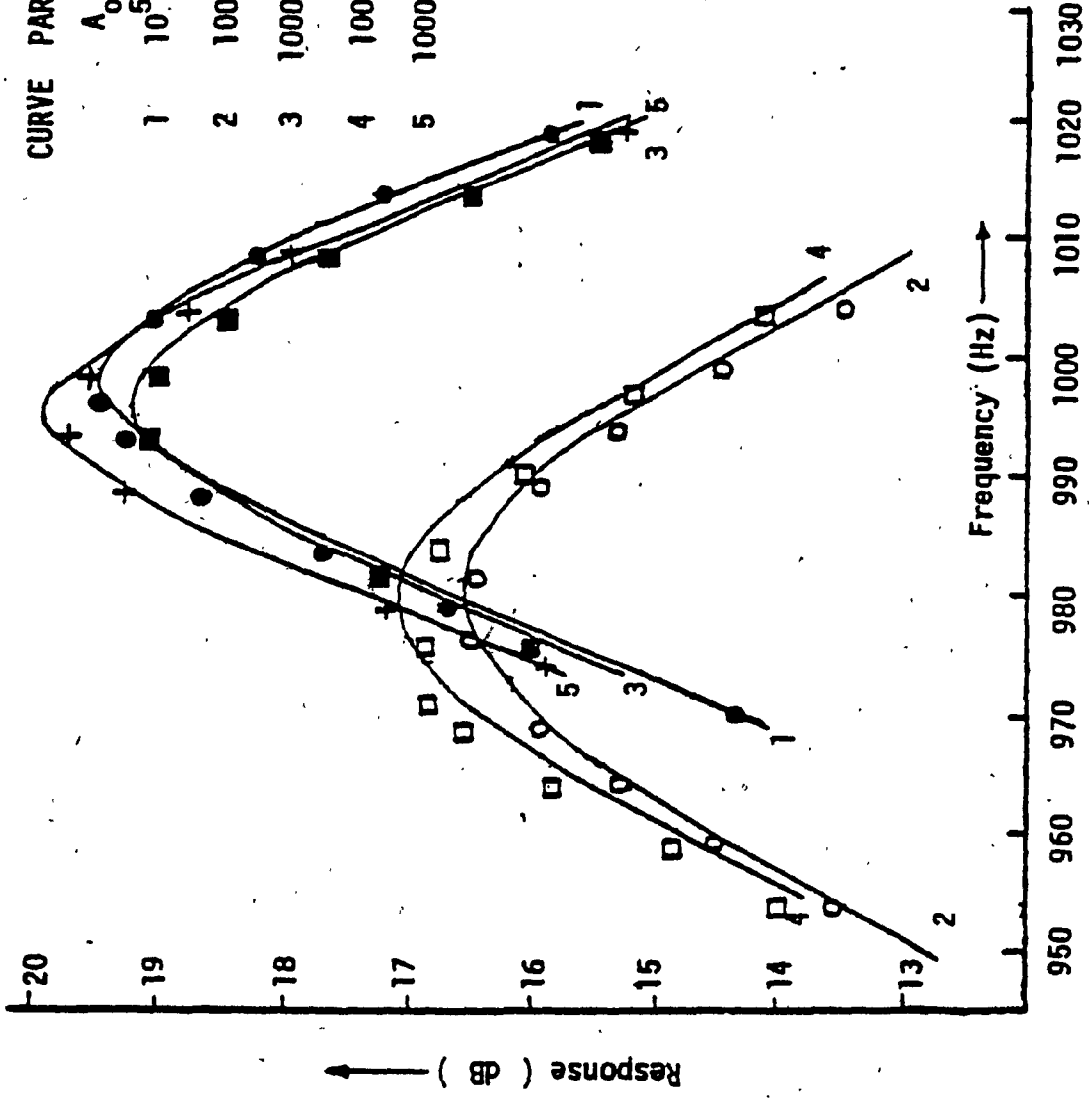


Figure 5.10: Experimental and theoretical responses for the SC bandpass filter of Fig.5.3

results are in very good agreement with the theoretical values.
results are in very good agreement with the theoretical values.
Slightly smaller values for the resonant frequencies and the resonant gains are observed experimentally compared with theoretical values. This is likely to be due for finite values of the ON resistances of the switches which were not accounted for in the theoretical analysis. Also the finite GB values were lowered successively with A_o = 1000 to observe the point where the circuit becomes unstable. The experimental B/w_p ratio when the circuit starts oscillation (at a frequency $\simeq f_p$) was observed to be about 18, which was quite close to the theoretically predicted value of 15. It may be observed that with such low values of B/w_p, the ratio $B/2\pi f_s$ becomes small and hence some of the assumptions used in the theoretical analysis (e.g. $\varepsilon \ll I_p$ in Section 5.2) may not be fully justified. This may account for the difference in the numbers 18 and 15.

The theoretical analysis for a multiphase SC network developed above were verified by taking the four phase differential integrator circuit illustrated in Section 5.4.2. The OAs were μA 741, the capacitors (C_1 = 2.7nF, C_2 = 10 nF) were polysterene film/foil type with ±10% tolerance. The OA of finite DC gains (100, 1000) and finite gain bandwidth values (11.7 kHz, 23.4kHz) were simulated using the model of Fig. 5.9. The clock rate was 10kHz. The ideal response [curve (a)] in Fig. 5.11 corresonds to the nominal values of $A_o(\sim 10^5)$ and GB(~1MHz) of the OA and was realized by replacing the macromodel by the OA itself. The solid curves in Fig. 5.11 represent the theoretical responses as obtained by numerical simulation. The experimental points are shown by the symbols ● , o , X , + (see legend in Fig. 5.11). It is

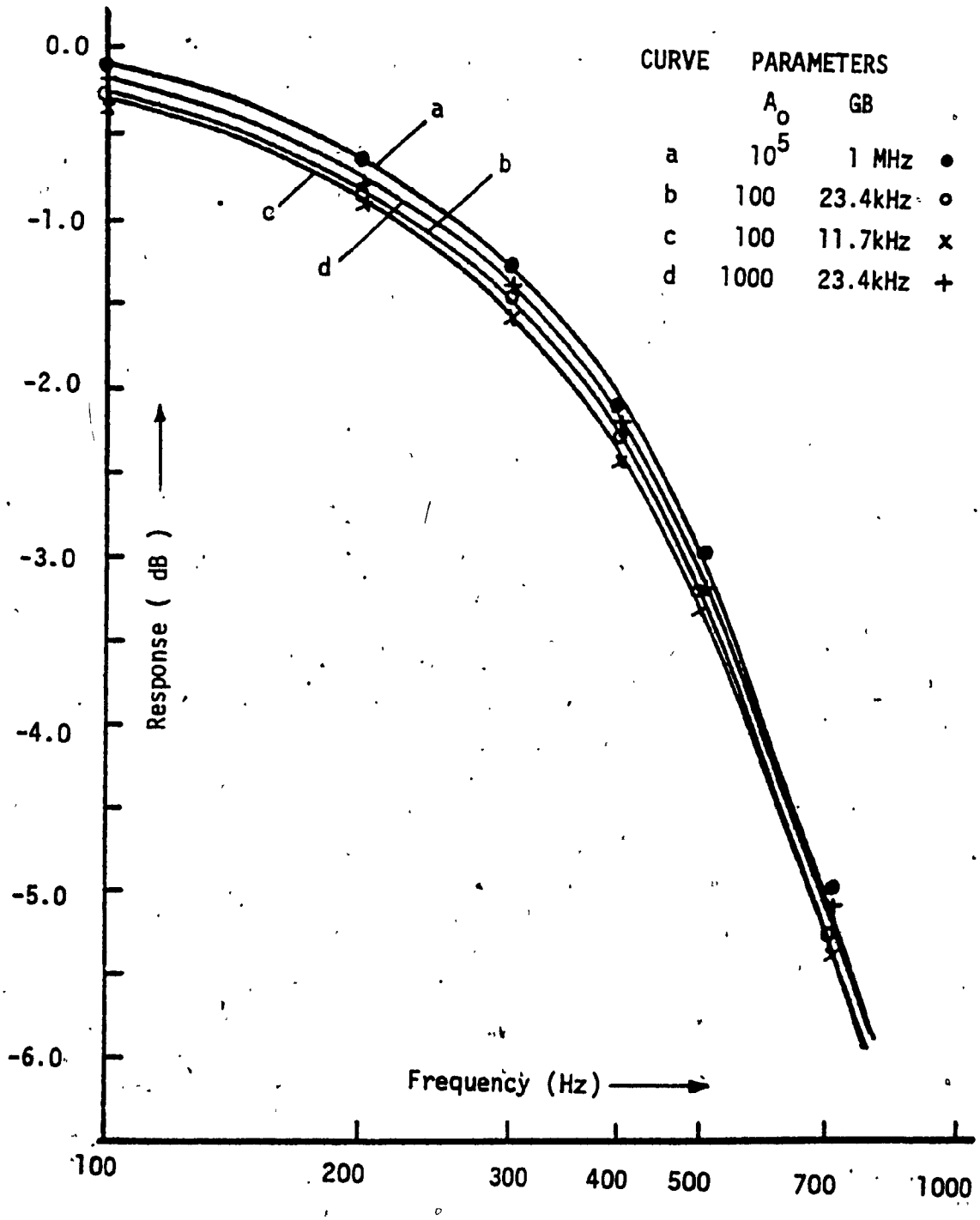


Figure 5.11: Responses of the DI network operated by a four phase clock and containing a non ideal OA

observed that the experimental points closely agree with the theoretical results. It may be remarked that substantial error from the ideal response would occur when the DC gain of the OA is very poor (× × , A_0 = 100). As regards the finite GB value of the OA, Fig. 5.11 shows that this response approaches toward the ideal when the GB value increases (with A_0 fixed at 100). Also for moderate GB values (23.4 kHz and above but small DC gains, the responses show noticeable departures from the ideal, mainly at low frequencies (< 500 Hz).

5.6.2 Numerical Investigation on UGA based BIQ SDTF

An UGA in practice may have two important deviations from its ideal behaviour, namely, the DC gain may not be unity (such as because of body effect in MOSFETs) and the bandwidth is usually finite. Experimental tests using UGAs in SC networks are meaningful only if they are carried out on SC networks implemented in MOS IC technology, or at the very least, if MOS UGAs are available. Since neither monolithic MOS IC fabrication facilities nor MOS UGAs were available, no experimental work with practical UGAs were carried out. It was, however, considered worthwhile to investigate the bandwidth capability (in relation to the pole frequency) of an UGA based BIQ-SDTF as compared with the same filter realized using OAs where the UGAs are also realized using OAs with 100% negative feedback. It can be easily shown that UGAs so realized will have a DC gain slightly less than unity ($\alpha_0 = 1/(1+1/A_0)$, A_0 the DC gain of the OA) and a bandwidth slightly larger ($B_{UGA} = B(1+1/A_0)$, B the GB of the OA) than the GB of the OA. In actual fabrication, however, the UGAs can be expected to

have bandwidths much higher than the GBs of OAs using similar technological processes. The UGA based BIQ-SDTF was the bandpass filter of Fig. 5.4 while the corresponding OA based network was chosen to be the one shown in Fig. 5.3. This latter network was found to have superior performance characteristics among a number of stray insensitive SC bandpass filters[50] (SC-BPF) as regards the effects of finite DC gain and finite GB values were concerned. For the UGA based SC-BPF, a parasitic tolerant design was first obtained by using an optimization algorithm as discussed in Chapter 4 of this thesis. This parasitic tolerant circuit was then tested for the effect of finite DC gain and finite bandwidth of the building blocks (viz., OAs) for the UGAs. The two categories of SC-BPFs were compared for the highest possible bandwidth capability (maximum ω_p/B ratio) as a function of design Q_p values of 5, 10, 15, 20 and 25 which could reproduce the given (analog) response function within a prescribed error limit. The error limit was set at 5% rms over the bandwidth of $(f_p \pm f_p/Q_p)$ of the bandpass filter. Figure 5.12(a)-(b) show the maximum bandwith ratios, (viz, ω_p/B) abbreviated as BWR, that could be achieved in the UGA (realized from OAs with 100% negative feedback) and the OA based SC BPFs respectively as a function of Q_ps with an rms error less than (or equal to) 5% over the significant bandwidth $(f_p \pm f_p/Q_p)$ of the filter. It may be observed that while the UGAs have nearly the same bandwidth as the GB of the OAs (the DC gain was set at $A_o = 10^4$), the BWRs available in the UGA based designs are about 1.5 times larger than the BWRs available with OA based designs. Thus the bandwidth capability of these UGA based filters could be about 50% higher than the corresponding filters designed using OAs. In a practical fabrication

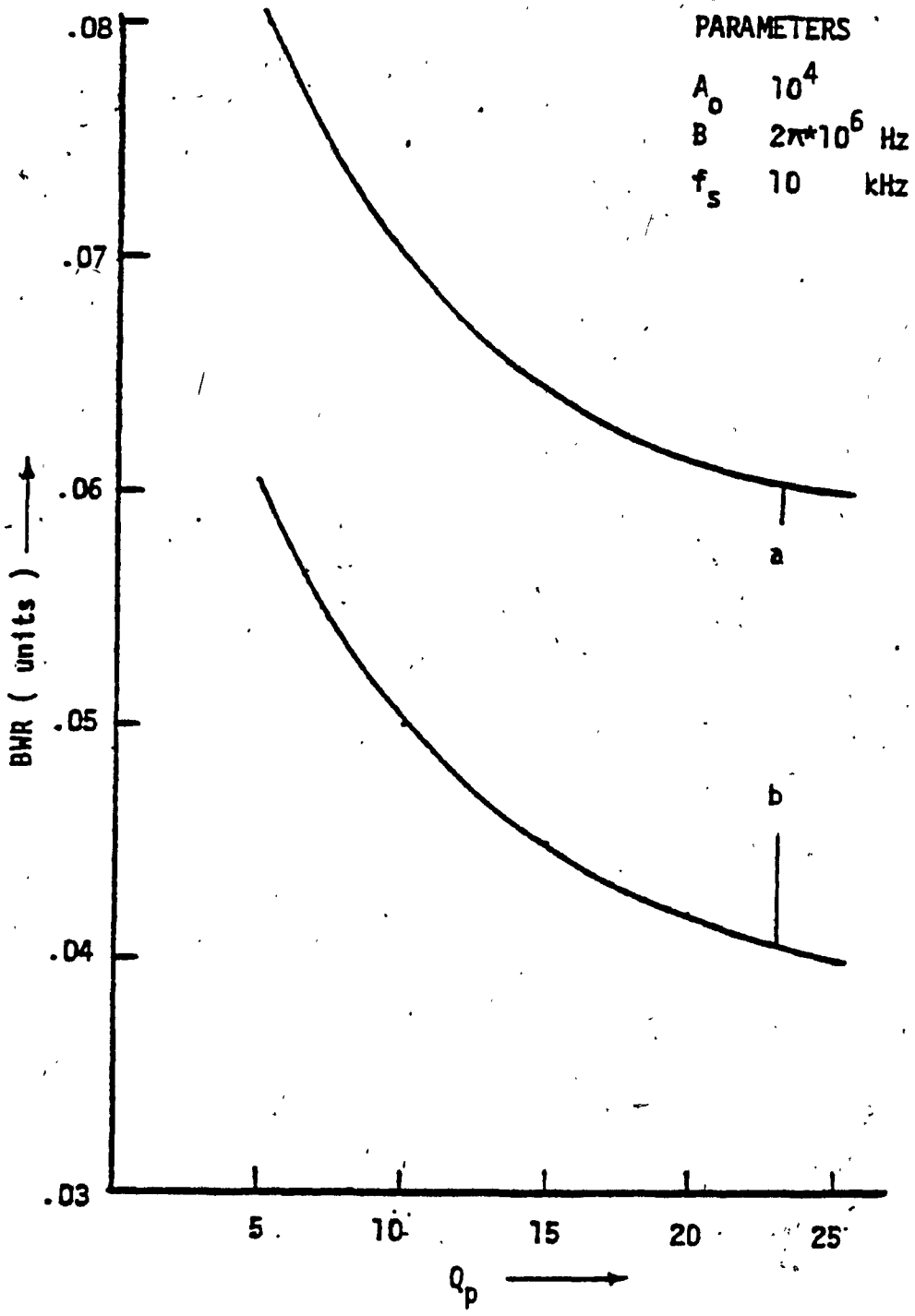


Figure 5.12: Bandwidth capabilities of SC bandpass filters realized using (a) UGAs made from practical OAs, (b) practical OAs

process, where UGAs could perhaps be realized to have bandwidths much higher than the OAs under similar technological constraints, the UGA based SCFs would have significantly higher (perhaps 3 or 4 times) bandwidth capabilities compared with OA based SCFs and yet offer similar performance standards against a specified amplitude response function.

5.7 CONCLUSION

A method is described to take into account the effect of the finite DC gain and gain bandwidth product of the active devices on the response of active SC filters, operated by bi-phase as well as multi-phase clocks. The method is principally a frequency domain method and uses the indefinite admittance matrix (two phase or multiphase IAM) of the passive part of the SC network. The interesting features of the proposed analysis methods are: (i) the time domain analysis that is required is carried out only for simple subnetworks separately around each AD in the SC network. Further, no analysis is required for the interval of transition between the consecutive switching phases. (ii) The method is modular and general in the sense that, for more than one active building block, a similar analysis is repeated for any number of ADs in the circuit of any topology. (iii) The method can be implemented by using the IAM for the passive part of the SC network. This, in most cases, can be done by simple inspection. **The simplicity of the time domain analysis required, the modularity and generality of the technique presented, the ease with which the IAM of a passive SC network can be obtained and manipulated to incorporate the constraints**

imposed by the presence of the ADs in the circuit and finally, the attendant versatility of an admittance matrix formulation should render the proposed technique very attractive. A step-by-step formulation of the procedure is decribed that should help utilization of the method as well as computerization of the analysis procedure. The analysis technique has been illustrated by examining SC networks operated by a two phase as well as a four phase clock signal. The analysis method has also been used to estimate the bandwidth capabilities of two second order SC bandpass filters, one designed with OAs and the other designed with UGAs. Detailed experimental investigations, using discrete capacitors, CMOS switches and conventional OAs, have been carried out in a number of cases. The experimental results are in very good agreement with the theoretical predictions.

CHAPTER SIX

CONCLUSIONS

6.1 SUMMARY

Research work in the area of SC filters (SCFs) has been extensive in the recent past. The majority of design and analysis efforts on SCFs has been concentrated on realizations using OAs. Realizations using UGAs have received relatively less attention. The popularity of OA based designs are, perhaps, due to the large volume of work existing in the area of active-RC filters which are mainly based on OAs. However, if the entire filter is fabricated on a monolithic chip in MOS technology, the possibility exists of significant savings in substrate areas for designs that use MOS UGAs over similar designs using OAs. Other consequent potential benefits for UGA based realizations are expected to be less DC power consumption, wider operating bandwidth and higher signal to noise ratio per active device compared with similar designs using OAs. **In this thesis systematic and efficient synthesis procedure for the design of sampled data transfer functions (SDTFs), recursive or non recursive and of any order, using UGAs, have been developed. Biquadratic SDTFs (BIQ-SDTFs), bilinearly equivalent to their analog counterparts, have been given special considerations. For BIQ-SDTFs, procedures have been proposed that yield designs comparable to OA based realizations. Further, these designs minimize the total capacitance in the circuit as well as the effect of the offset voltages of the UGAs. Also, the designs are tolerant of the various parasitic capacitances in the circuit. Finally, an elegant method has been**

proposed for examining the effect of the frequency dependent gain of the active device, UGA or OA, on SCF realizations.

Towards this end, a systematic approach for realizing SDTFs is first introduced in Chapter 2. The proposed designs are based on a number of building blocks such as delay and add networks etc., realized from UGAs, switches and capacitors. Realizations of both nonrecursive SDTFs (NR-SDTFs) and recursive SDTFs (REC-SDTFs) are illustrated. Realization of an important class of NR-SDTF, viz., constant delay filters, has also been considered in some detail. Several practical considerations, namely, the sensitivity of the desired response to capacitance ratio errors and the effect of spectral shaping due to the sample and hold circuits on the prescribed response, are discussed. The theoretical basis of an optimization algorithm to minimize the error between the prescribed and the realized responses is developed. The design parameters obtained from the above optimization analysis are used in practical designs of both non recursive and recursive sampled data filters. Finally, the topology for a general BIQ-SDTF is introduced in this chapter.

Since biquadratic filters can accomplish a number of important filtering functions and also serve as important building blocks for realizing high order filters, a detailed investigation of this case is pursued in Chapter 3 of the thesis.

It is well known that bilinear transformations yield the lowest possible ratio of clock frequency to the cut off frequency of the

filter (theoretical minimum limit being two, by Nyquist's theorem). Consequently, a systematic procedure for realizing BIQ-SDTFs bilinearly equivalent to the popular analog biquadratic filter functions is developed in Chapter 3. Appropriate analysis leads to a criterion that allows us to choose a clock frequency that yields very low sensitivity realizations. Schemes that minimize the total capacitance in the network have been suggested. A most difficult problem to deal with in UGA based realization of SCFs is the effect of parasitic and stray capacitances on the nominal response. Careful layout can make the design insensitive to the parasitics associated with the bottom plates of the network capacitors. However, the strays and parasitics associated with the switches and the top plates of capacitors remain a vexing problem. An optimization algorithm has been proposed which makes the given design tolerant of the various stray and parasitic capacitances to the extent that a given response is met within a specified error limit. **A post optimization analysis has been included in the optimization alogrithm so that the resulting response is relatively unaffected even when the levels of the parasitic and stray capacitances are not known exactly but only within a statistical variance.** The various practical considerations in the design are finally incorporated in a step-by-step procedure. Extensive computer simulations and experimental investigations using discrete capacitors, CMOS switches and μA 741 OAs (to realize UGAs) show close agreements with the theoretical analysis.

While the methods proposed in Chapter 3 are simple, systematic and effective, their main disadvantage is the requirement of a large

number of components (switches, capacitors and UGAs). A number of OA based designs which use only two OAs and much fewer number of capacitors are already available in the literature. Consequently, even though an UGA may require considerably less substrate area than an OA, the net substrate area demanded by the propsed BIQ-SDTFs may not be substantially less than in an existing OA based design. Clearly then, an UGA based design would be more attractive only if the number of UGAs is reduced to two and the number of capacitors is made comparable to that in the two OA based realizations.

Chapter 4 of the thesis pursues these objectives. This chapter, in particular, presents significantly improved designs of SC biquadratic filters equivalent to the analog biquadratic transfer functions under the bilinear mapping between the s and z domains. The number of UGAs employed are two and the number of capacitors are at most ten. These are about the same number of active devices and capacitors used in comparable designs based on OAs used as infinite gain amplifiers. The problems of parasitic and stray capacitances associated with the top plates of the network capacitors as well as the input of the UGAs have been considered. An algorithm to yield a **parasitic tolerant design** along with minimal total capacitance has been proposed. The effect of the finite non zero offset voltage in the UGAs on the response of the SCFs has been studied and a method has been suggested to minimize this effect. Further, a design that needs far fewer than ten capacitors and can produce a general SDTF that are bilinear counterparts of the low pass, high pass and bandpass analog functions has been proposed. However, the flat gain of the analog

filter has often to be scaled down in realizing these designs and hence such filters may have detrimental effect on the signal to noise power ratio as the signal is processed by the filter. Also in certain cases, such designs have to be restricted to realizations having low values of f_p/f_s ratios, thereby offsetting the primary advantage of realizing an SC filter related to its analog counterpart by bilinear transformation. Extensive computer simulations have shown that the filters resulting from the proposed realization are compatible with the requirements of the current IC MOS technology.

To realize the potential of high frequency operation of UGA based SCF designs, a method is needed to account for the frequency dependence of the UGA gain on the SCF performance. Only a limited amount of results in this area is available in the existing literature. Thus, an elegant analysis method is developed, to examine the effect of the frequency dependent gain of an active element on the performance of the SCFs, in Chapter 5. In particular, the proposed method takes into account the effect of the non ideal DC gain and gain bandwidth product of the active element in an active SC network. In practice, the active component can be either an OA or an UGA. The popular single pole model has been assumed for the gain function of the active device. First, the case for biphase clocking signal is analyzed and then the method is extended to cover SC networks operated by multiphase clock signals. The proposed method is principally a frequency domain method, as opposed to the existing methods that are principally time domain techniques, and uses the indefinite admittance matrix of the passive SC network. The attractive features of the proposed analysis method are:

(i) the time domain analysis is carried out for simple subnetworks separately around each active device in the SC network for each phase of the clock signal; (ii) the method is modular and general in the sense that for more than one active component, a similar analysis is repeated for any number of the active components in the circuit (iii) the method is applicable for a circuit of any arbitrary topology; (iv) the method can be implemented by using the IAM for the passive part of the SC network. **The simplicity of the time domain analysis required, the modularity and generality of the technique presented, the ease with which the IAM of the passive part of a given SC network can be obtained and manipulated to incorporate the constraints imposed by the presence of the active components in the circuit and finally, the attendant versatility of an admittance matrix formulation should render the proposed technique very attractive.** The analysis technique is summarized in a number of sequential steps and is illustrated by applying to a number of practical circuits which use OAs or UGAs as the active building blocks. The bandwidth capabilities of second order bandpass SCFs designed using OAs and UGAs are estimated using the proposed analysis technique. Experimental measurements have been conducted using OAs with finite gain and gainbandwidth values, simulated using a macromodel. The results show very good agreements with theoretical predictions.

6.2 SCOPE FOR FURTHER WORK

Further work to extend the results obtained in this thesis can be carried out in several directions. Some of the possible directions

are discussed in what follows:

(i) In the experimental work undertaken to verify various theoretical predictions about UGA based biquadratic SDFTs, the UGAs were designed using conventional OAs with unity negative feedback. This was done because a fabrication facility of MOS integrated circuits was not available to the author. The fullest potential of the various results reported in the thesis is possible to realize only if MOS buffers are used for the UGAs and the entire circuit is fabricated utilizing monolithic MOS technology.

(ii) While the realization of BIQ-SDTFs using UGAs and SCs has been proposed in this thesis to a level where it requires about the same number of active devices (UGAs) and capacitors as in corresponding designs using OAs as inverting amplifiers, it appears possible to economize further in the number of capacitors. This has been revealed in Chapter 4 where it is shown that it is possible to realize BIQ-SDTFs using as few as four to six capacitors. However, the realization of SC notch filters bilinearly equivalent to the analog notch filter transfer function has not been possible. Also, the low pass, high pass and bandpass filters using this new topology are sometimes restricted to realizations that need scaling down of the flat gain and requiring operations at a greatly reduced pole frequency relative to the clock rate. This situation demands more critical investigations.

(iii) While an elegant method for analyzing the effects of the DC gain and gainbandwidth product values of the OA (or UGA) in an active SC network has been proposed, its potentials have not been adequately exploited. Thus, the given method could be used to realize designs (based on either practical OAs or practical UGAs) that are optimal with regard to bandwidth capabilities for a given set of filter specifications and given gain and gainbandwidth parameters for the active element.

(iv) In developing the analysis method mentioned in item (iii) above, the input and output impedances of the active element have been assumed to have the ideal values (theoretically infinite and zero respectively). Consideration of these impedances for the active element would make the analytical procedure more involved but more practical. Also, the slew rate of the active element (OA or UGA) has not been taken into account. This would perhaps restrict the applicability of the analysis method to clock rates which are not too close to the gain bandwidth of the active element. The present analysis method should be fairly accurate for clock rates up to about one-fourth of the GB of the active element. For clock rates higer than this, the non idealities as mentioned above (in addition to non ideal gain and GB values) are to be taken into consideration.

(v) A number of optimization algorithms has been developed in the course of the various investigations in the thesis. It appears worthwhile to make an effort to incorporate these algorithms

together with the analysis method for non ideal gain and GB of the active components in developing a complete numerical algorithm leading to a compuer aided design and analysis package which could be useful in many practical cases (e.g., in a manufacturing industry).

In conclusion, it is hoped that the results reported in this thesis of the investigations carried out by the author will be useful to others interested or doing research work in the area of design and implementation of switched capacitor filters.

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