CANADIAN THESES

THÈSES CANADIENNES

NOTICE

The quality of this microfiche is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Previously copyrighted materials (journal articles, published tests, etc.) are not filmed.

Reproduction in full or in part of this film is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30.

AVIS

La qualité de cette microfiche dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

Les documents qui font déjà l'objet d'un droit d'auteur (articles de revue, examens publiés, etc.) ne sont pas microfilmés.

La reproduction, même partielle, de ce microfilm est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30.

THIS DISSERTATION HAS BEEN MICROFILMED EXACTLY AS RECEIVED

LA THÈSE A ÉTÉ MICROFILMÉE TELLE QUE NOUS L'AVONS REÇUE

Canada

SOME NOVEL POWER CONVERSION SCHEMES EMPLOYING PULSE WIDTH MODULATED HIGH-FREQUENCY LINKS

Stefanos Manias

A Thesis

in

The Department

of

Electrical Engineering

and

Computer Science

Presented in Partial Fulfillment of the Requirements
for the degree of Doctor of Philosophy at
Concordia University
Montréal, Québec, Canada

September 1984

ISBN 0-315-30666-1

ABSTRACT

Some Novel Power Conversion Schemes
Employing Pulse Width Modulated High-Frequency Links

Stefanos Manias, Ph.D.
Concordia University, 1984

Static power conversion schemes employing Pulse Width Modulated High-Frequency (HF) links, are investigated in this thesis. The employment of HF links in power conversion schemes results in substantial size, weight and cost reduction of the power converter isolation transformer and reactive components. Therefore, in applications where power density is of prime importance the employment of HF links is the natural choice.

The following power conversion schemes employing an HF link are considered in particular.

A voltage source DC to AC inverter consisting of an HF link and a DC to AC inverter stage is investigated. Its main advantage over conventional inverter configurations is the drastic size and weight reduction of the magnetic components. Furthermore, the proposed inverter offers high operating efficiency, step-up/step-down ability, programmable output frequency and transformer isolation at HF link switching frequencies. Inverter performance is obtained using the results of the analysis and a design procedure is given.

A three-phase Current Source DC to AC inverter consisting of an HF link and a DC to AC inverter stage is investigated. The Current Source is created by the HF link stage which together with a high-frequency transformer provides isolation between the source and the load. The output current regulation and circuit protection is performed

by the HF link stage. The function of the DC to AC inverter stage is to create an output current with low harmonic content by applying fixed switching patterns.

An AC to DC converter consisting of an HF link stage is investigated. The proposed power conversion scheme employs an AC to AC cycloconverter as an HF link which together with a high frequency isolation transformer provides isolation between the source and the load. Furthermore, the proposed converter exhibits controlled power factor, step-up/step-down ability and low input Total Harmonic Distortion (THD) with the employment of small sized input filter.

A bilateral HF link power converter is investigated. The proposed power conversion scheme incorporates a battery charger into an inverter by using the existing power circuit components. This power conversion scheme, which can be applied to Uninterruptible Power Supply systems, can also be applied as an AC motor drive and on board battery charger for Electric vehicles where weight and size reduction is of prime importance.

To facilitate understanding and applicability of the analytical results, design examples are presented for all the proposed power conversion schemes. Also selected predicted results are verified experimentally.

ACKNOWLEDGEMENTS

The author wishes to express his gratitude to Dr. P.D. Ziogas for his valuable advice, support, guidance and supervision during the course of this thesis.

He would also like to thank Mr. Danny Juras, technician of the University's Power Electronics Laboratory for his assistance and support, and also to Mrs. Madeleine Klein for the typing of the manuscript.

To my wife Maria and our children
whose overall support was essential
for the completion of my studies

LIST OF PRINCIPAL SYMBOLS

1. Voltages

E	DC bus voltage
E_{min}	Lowest expected E value
E_{max}	Highest expected E value
V_{an}, V_{bn}, V_{cn}	Three-phase line to neutral voltages
V_{ab}, V_{bc}, V_{ca}	Three-phase line to line voltages
V_m	Amplitude of line to neutral voltages
$V_{m(max)}$	Highest expected V_m value
$V_{m(min)}$	Lowest expected V_m value
V_o	Load voltage
$V_{o,n}$	Amplitude of the nth harmonic component of V_o
$V_{o,d}$	Amplitude of the dominant harmonic component of V_o
V_{if}	Voltage before output filtering
$V_{if,n}$	Amplitude of the nth harmonic component of V_{if}
$V_{if,d}$	Amplitude of the dominant harmonic component of V_{if}
V_p	Voltage across the isolation transformer primary
V_s	Voltage across the isolation transformer secondary

2. Current

I_i	Input filter inductor current
$I_{i,n}$	Amplitude of the nth harmonic component of I_i

I_o	Load current
$I_{o,n}$	Amplitude of the nth harmonic component of I_o
I_p	Isolation transformer primary current
I_s	Isolation transformer secondary current
I_{if}	Output filter inductor current
$I_{if,n}$	Amplitude of the nth harmonic component of I_{if}
i_c	Commutation current
I_{PT}	Thyristor peak current
I_{RT}	Thyristor RMS current
I_{AT}	Thyristor average current
I_{AS}	Power switch average current
I_{RS}	Power switch RMS current
I_{PS}	Power switch peak current

3. Capacitances

C_i	Input filter capacitance
C_o	Output filter capacitance
C_s	Intermediate filter capacitance
C_c	Commutation Capacitance

4. Inductances

L_i	Input filter inductance
L_o	Output filter capacitance
L_s	Intermediate filter inductance
L_c	Commutation inductance

5. Impedances

X	Impedance of the commutation inductor
R_{eq}	Equivalent Resistance of the Commutation Circuit
X_{c_i}	Impedance of the input filter capacitor
X_{c_o}	Impedance of the output filter capacitor
X_{c_s}	Impedance of the intermediate filter capacitor
X_{L_i}	Impedance of the input filter inductor
X_{L_o}	Impedance of the output filter inductor
X_{L_s}	Impedance of the intermediate filter inductor
X_{c_1}, X_{c_2}	Impedance of the shunt capacitors of the Current Source Inverter output filter
Z_L	Load impedance
$\|Z_{L,n}\|$	Magnitude of Z_L at the nth harmonic frequency
Z_o	Input impedance of the load filter
$\|Z_{o,n}\|$	Magnitude of Z_o at the nth harmonic frequency

6. Time

T	Waveform period
t_{off}	Power Semiconductor switch turn-off-time specified by the manufacturer
t_g	Thyristor turn-off interval
Δt	Turn-off time safety margin
T_f	Period of the reference signal
T_c	Period of the Carrier Signal

7. Frequencies

f_o	Frequency at which the DC to AC Inverter operates (i.e. f_o = 60Hz)
ω_o	Angular Frequency at which the DC to AC Inverter operates (i.e. $\omega_o = 2\pi f_o$)
f_i	AC input voltage freqeuncy
ω_i	Angular frequency of the AC input voltage
f_{nc}	Normalized (with respect to f_o or f_i) carrier frequency
f_ℓ	HF link switching frequency
$f_{n\ell}$	Normalized (with respect to f_o or f_i) HF link frequency
ω_{bo}	Angular break frequency of the output filter
ω_{bi}	Angular break frequency of the input filter

8. Switching Functions

$S(\omega t)$	Converter overall switching function
$S_c(\omega t)$	Cycloconverter switching function
$S_i(\omega t)$	Inverter Stage Switching function
$S_r(\omega t)$	Rectifier Stage Switching function

9. Miscellaneous Parameters

d	Order of the dominant harmonic
n	Order of the nth harmonic
k	Order of the kth harmonic

K_c	A variable defined as $K_c = \frac{V_o}{E}$
K_{i_i}	Input filter inductor current ripple factor
K_{v_i}	Input filter capacitor voltage ripple factor
K_{i_o}	Output filter inductor current ripple factor
K_{v_o}	Output filter capacitor voltage ripple factor
K_{i_s}	Intermediate filter inductor current ripple factor
K_{v_s}	Intermediate filter capacitor voltage ripple factor
M_f	Modulation factor
ΔI_s	Current Source Reactor current ripple
Q	Coil parameter defined as $Q = \frac{\omega L}{R}$ where ω, L and R are the Operation Angular frequency Induactance and coil Resistance respectively
THD	Total Harmonic Distortion
ϕ_n	Phase displacement between the nth harmonic components of $V_{if}(\omega t)$ and $I_{if}(\omega t)$
ϕ	Phase displacement between the fundamental components of load voltage and current
ϕ_1	Phase displacement between the fundamental components of voltage and current before output filtering

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Introduction

Depending on the power conversion scheme employed, static power converters are divided into two broad classes:

a) The linear-mode converters

b) The switch-mode converters

The linear-mode converter offers excellent voltage regulation and is relatively insensitive to variations in input source frequency. Its initial cost is moderate, but because of low power conversion efficiency, its long term cost increases steeply with time. This type of power converter is widely used on TV sets, audio amplifiers, stereos, and laboratory power supplies, as well as in a wide range of commercial and industrial electronic equipment. In comparison, the Switch-Mode power converter is at least twice as efficient as the linear-mode. Moreover, Switch-Mode converters offer the advantages of reduced size, weight and cost. However, if improperly designed, they can generate Electromagnetic Interference (EMI) that can degrade other systems. Also, a major shortcoming of Switch-Mode converter technology is that they require more complex design. Even with these disadvantages, Switch-Mode converters are being increasingly accepted in industry, particularly where size, weight, cost and efficiency are of prime importance.

The number of applications of Switch-Mode converters has increased rapidly over the past decade. In addition to their wide spread use as DC regulators, these converters have found employment in a variety of applications involving electrical power conversion, including DC to AC

inverters for solar arrays, AC to DC unity input power factor controlled rectifiers for battery charger applications, ringing and tone generators for telephone systems and other applications associated with aerospace and military industries. Fig. 1.1 [1] shows the market distribution of linear and Switch-Mode power converters.

1.2 General background on conventional Switch-Mode converter configurations

Current Switch-Mode converter technology employs five main power converter configurations. These configurations and their salient features are as follows:

a) Ferroresonant converter [2]

Ferroresonant converters, Fig. 1.2(a), operate by resonating a capacitor in the secondary of the isolation transformer with a saturable reactor which is one of the legs of the transformer. Resonance increases the voltage level independently of the input voltage. Its salient features include simplicity, inherent overvoltage protection and poor power factor. Because of its poor power factor and the need for additional reactive components to create the resonance effect the converter becomes complex, bulky and inefficient.

b) Phase control converter [3]

This power converter configuration, Fig. 1.2(b), is normally used for AC to DC power conversion. The simplest phase control converter operates by turning on the power switches of the rectifier for only a portion of each half cycle of the input voltage to which it is connected. Therefore, the corresponding output voltage consists of segments of the input voltage. The salient features include simplicity, poor power

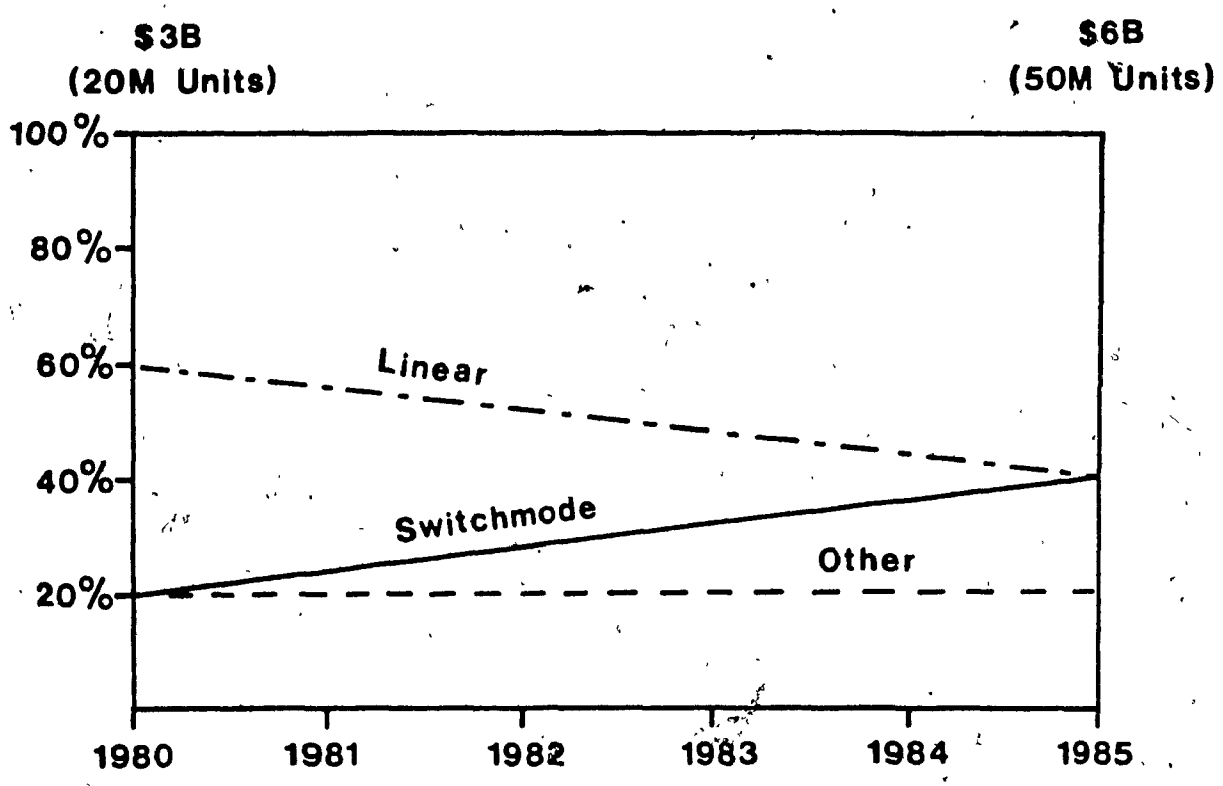


Fig. 1.1: Market distribution of linear and Switch-Mode power converters.

factor, and creation of low order harmonic components in the output voltage. Therefore, because of the ratings of the input and output filter components and the size of the low frequency isolation transformer, the converter becomes bulky, costly and inefficient.

c) Single Stage DC to AC inverter [4]

This power converter configuration, Fig. 1.2(c), is widely employed for DC to AC power conversion. The main disadvantage of this converter is that the high inverter switching frequency is not exploited for reducing the size, weight and cost of the isolation transformer. This high switching frequency results from Sinusoidal Pulse Width Modulation (SPWM) control technique which is typically employed for output voltage regulation and elimination of unwanted harmonic components. The employment of SPWM results in size reduction of the input and output filter components.

d) DC to DC converter using a High Frequency link [5]

This power converter configuration, Fig. 1.2(d), includes all DC to DC converters that are realized using the Boost or Buck chopper configurations or combinations of the two. This scheme of converters employ high switching frequency thus reducing the size of magnetic and reactive components. A further significant advantage of the high switching frequency is that these converters exhibit fast response.

e) DC to AC, AC to DC and AC to AC converters using a High Frequency link

These configurations include all converters realized by;

i) cascading two single power conversion states

or

ii) replacing the unidirectional switching devices of a single conversion stage by bidirectional ones

or

iii) any combination of (i) and (ii)

thus yielding new power schemes with improved properties. These properties include good quality input and output waveforms and substantial size, weight and cost reduction of the reactive elements and isolation transformer.

At present the size and cost of Switch-Mode converter is largely influenced by the:

i) number of power semiconductor devices needed to implement the power conversion scheme.

ii) ratings of the reactive elements of the input and output filters.

iii) ratings of the isolation transformer.

However, power semiconductor technology is rapidly improving, yielding better and better devices at diminishing cost. While reactive elements and magnetic components are not likely to become much cheaper and smaller in the future. Therefore, reactive elements and magnetic components are bound to share increasing amount of the size, weight and cost of the power conversion schemes based on present designs. Consequently, it is preferable to employ two stage power conversion schemes in designs where power density and cost are of prime importance.

Fig. 1.2(e) shows in block diagram form a DC to AC converter which employs a high frequency link. The DC voltage, instead of being directly inverted into the required low output frequency voltage (as in Fig. 1.2(c)), is first inverted into high frequency AC voltage (High frequency link) thus making the size of the isolation transformer to be reduced considerably. The high frequency AC voltage then is rectified and finally inverted by a second power conversion stage to low frequency AC output voltage. Fig. 1.2(f) shows in block diagram form an AC to DC converter which employs a high frequency link. The low frequency input AC voltage, instead of being directly rectified into DC voltage, is first converted into high frequency voltage thus making the size of the isolation transformer to be reduced considerably. The DC output voltage is then obtained by rectifying the high frequency AC voltage. Finally, both power conversion schemes may employ SPWM technique or any other switching function (Appendix D) in order to obtain input and output waveforms with low harmonic distortion using minimum filtering.

1.3 Selection of power converter configuration

The widespread use of Switch-Mode converters and the availability of new power semiconductor devices have generated a need for power conversion schemes with the following new properties:

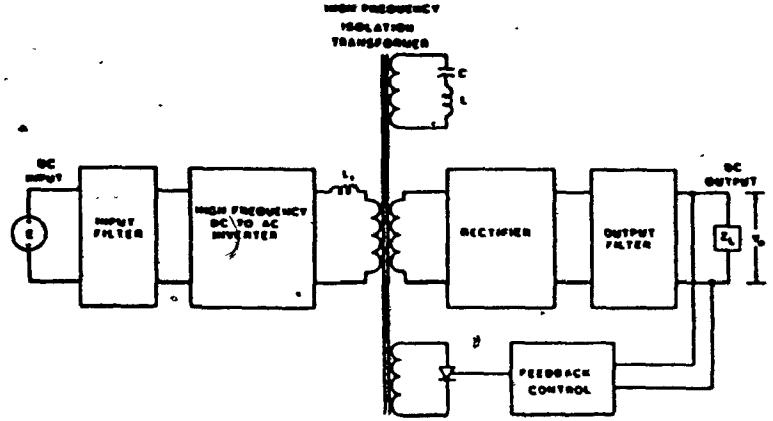
i) To exhibit high power density (reduction of size and weight)

ii) To exhibit controlled power factor.

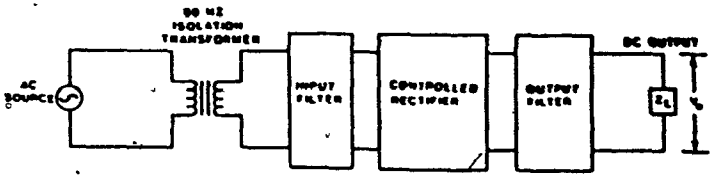
iii) To provide input and output waveforms with low Total Harmonic Distortion (THD) by employing small size filters.

iv) To provide transformer isolation between the source and the load.

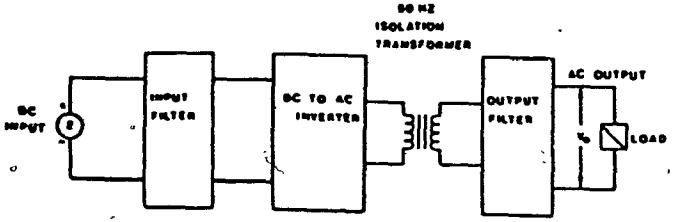
v) To exhibit high power conversion efficiency.



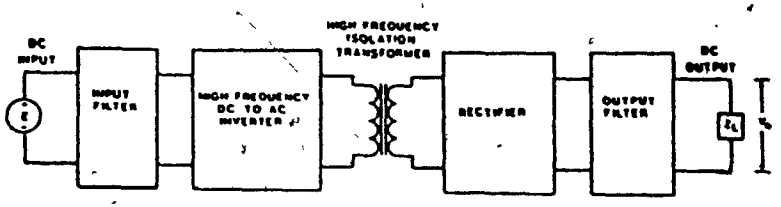
1.2(a): Ferroresonant converter



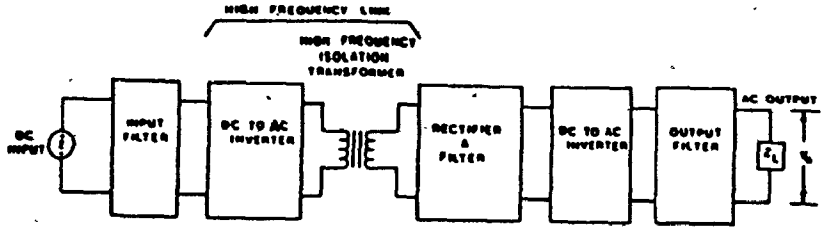
1.2(b): Phase control converter



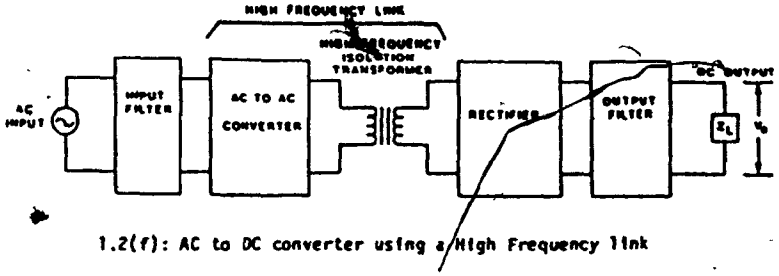
1.2(c): Single-Stage DC to AC inverter



1.2(d): DC to DC converter using a High Frequency link



1.2(e): DC to AC inverter using a High Frequency link



1.2(f): AC to DC converter using a High Frequency link

Fig. 1.2: Current Switch-Mode converter configurations

vi) To exhibit high reliability

vii) To be realized with minimum cost.

These properties have motivated the search for new power conversion schemes (DC to AC and AC to DC) where the High Frequency (HF) Link technique is employed in order to achieve the above mentioned properties. However, since the HF link power conversion schemes generally involve an additional power conversion stage extensive investigation will be required before their credentials are established. For power levels up to few tens of kilo-watts HF links are attractive. Their acceptance has also been accelerated by recent improvements in power semiconductor technology, which have resulted in increased switching speeds for power thyristors and also in continuing improvement in the power handling capability of transistors and MOSFETs. The technique of HF link conversion should therefore become increasingly widespread.

1.4 Review of Previous Work on HF link techniques

The use of an HF link in power conversion schemes has been suggested in the past in connection with various applications.

A DC to DC converter utilizing a series resonant inverter as an HF link was proposed by Schwarz [6]. The rectifier load is connected in series with the LC resonant circuit. The converter therefore possesses the characteristics of a current source. Current is regulated by controlling the frequency of operation of the converter.

McMurray investigated an electronic transformer utilizing an HF link [7]. The 60 Hz AC input voltage is chopped at high frequency of about 10 KHz, using thyristor series inverter. The high chopping

frequency results in reduction of the isolation transformer size. The 60 Hz AC waveform is reconstructed on the secondary of the transformer by further thyristor switches which are operated in sychronism with the switches on the primary side. Thus the input and output are isolated with the employment of a high frequency transformer.

The use of HF links has also been considered for high power utility applications. Gyugyi et al investigated an HF link technique for applications such as interconnection of power system [8].

Espelage et al investigated a DC to AC inverter using an HF link [9]. The overall unit consists of two power conversion stages. A DC to AC inverter stage that creates the HF link and a cycloconverter stage that converts the high frequency voltage generated into a low frequency one. In this power conversion scheme the principle of series resonance is applied.

HF link conversion schemes have been proposed for interfacing solar cell arrays to the AC power line. The small transformer size resulting from high frequency operation makes this arrangement attractive [10] [11]. Considerations of weight and size are of major importance in on-board power supplies for electric vehicles. This is another area where the potential offered by HF links has attracted investigation.

It is noted that most of the previous work on HF links has been focused on converter configurations that incorporate an additional resonance subcircuit. This subcircuit consists of two series connected L_r-C_r components as shown in Fig. 1.3(a). The function of this subcircuit is to generate a resonant high frequency current and to facilitate current commutation when the main power converter switches are realized by non-Gated turn off devices. The resonant HF link converter when

compared to Pulse Width Modulated (PWM) converter (Fig. 1.3(b)) has the following advantages and disadvantages.

Advantages

(i) Exhibits lower switching losses

(ii) Exhibits lower Electromagnetic Interference

Disadvantages

(i) Requires additional passive components

(ii) Exhibits high KVA ratings because of the resonant circuit

(iii) Power switches are subjected to higher peak currents

(iv) Operation is feasible only close to resonance frequencies.

The introduction of higher gain switches adds more weight to disadvantages and subtracts weight from the advantages. Therefore, power conversion schemes employing the PWM HF link technology is the natural choise for satisfying the design objective of this research.

1.5 Scope of the thesis

Briefly, the main objective of this thesis is to propose four novel power conversion schemes which exhibit the properties presented in section 1.3. The aforementioned schemes are novel in that they have not been either described or analyzed in previously published work. For example the scheme described in Chapter 4 includes a circuit configuration conceived, described and analyzed for the first time by the author. Similarly the power conversion scheme described in Chapter 3 is completely original and has for the first time been reported in technical literature [15] by a paper co-authored by the author of this thesis. Finally, the same degree of originality applies to the work described in Chapter 2 [12], 5 and Appendix B [35].

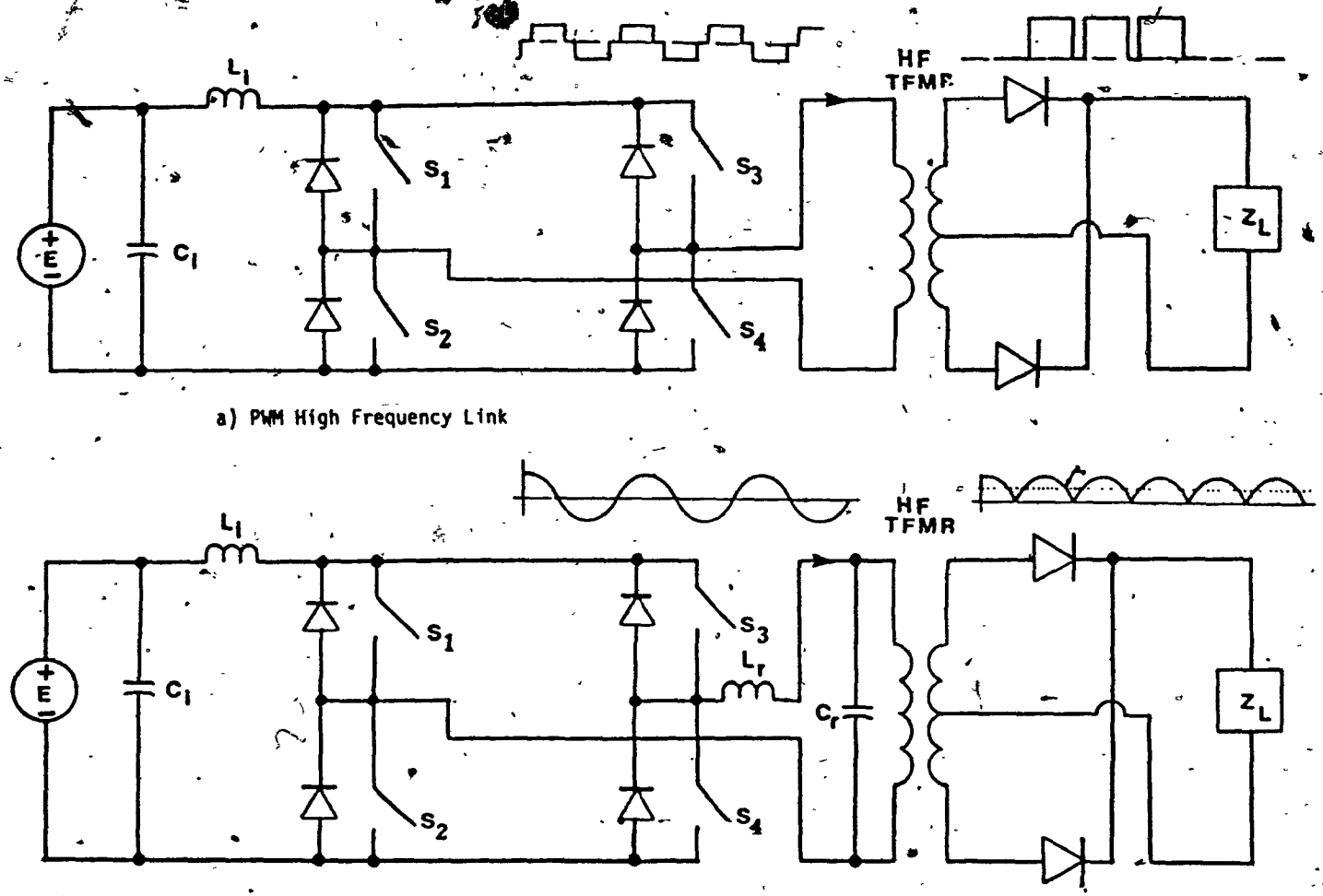


Fig. 1.3: Types of High Frequency Links

The proposed schemes, which employ an HF link, are analyzed and evaluated in a modular form with the aid of computer simulation. The computer simulation obtains spectra of waveforms of interest, determines component ratings and performs waveform analysis. The computer program computes the real time waveforms over a full cycle.

The guidelines for the design of input and output filters are discussed, and the factors commonly employed for their design are defined in terms of the harmonic content of the power conversion scheme variables.

The proposed power conversion schemes are analyzed under steady state conditions and with the following assumptions:

i) All power switching devices are ideal and diodes forward drop and reverse leakage current are ignored.

ii) The filter components are ideal.

iii) The input source voltages are ripple free and in case of a three-phase AC source are balanced.

iv) In the AC to DC power conversion scheme the output filter inductor current is ripple free.

v) In the DC to AC inversion schemes the rated load power factor is allowed to vary from .8 capacitive to .6 inductive.

vi) The input source voltage typically vary from 10% above to 20% below its nominal value.

The contents of this thesis is divided into five chapters and four appendices listed as follows:

In Chapter 2 a novel single phase DC to AC inverter, which employs a DC to DC converter as an HF link, is analyzed. The predicted results are verified experimentally and design guidelines are provided for selecting components.

In Chapter 3 a novel three phase current source DC to AC inverter, which employs a DC to DC converter as an HF link, is analyzed. The advantages and disadvantages of Current Source Inverters (CSI) when compared to Voltage Source Inverters (VSI) are briefly discussed. The predicted results are verified experimentally and design guidelines are provided for selecting components.

In Chapter 4 a novel AC to DC rectifier, which employs an AC to AC converter (cycloconverter) as an HF link, is analyzed. Design guidelines are produced for selecting components.

In Chapter 5 a novel bilateral converter, which employs an HF link in both modes of operation, is analyzed. The predicted results are verified experimentally and design guidelines are provided for selecting components.

In Appendix A the algorithm of the developed computer program, which was used throughout this thesis to analyze the various proposed power conversion schemes, is outlined.

In Appendix B an analysis of a novel current impulse commutated thyristor inverter is presented and analyzed. The proposed inverter is used in this thesis as an HF link for thyristorized power conversion schemes.

In Appendix C the definitions of some important variables used throughout this thesis are presented.

In Appendix D the switching function approach, which is used for the analysis of the proposed power conversion schemes throughout this thesis, is presented.

CHAPTER 2

A VOLTAGE SOURCE DC TO AC INVERTER USING A DC TO DC CONVERTER AS A HIGH FREQUENCY LINK

2.1 Introduction

Fig. 2.1 shows the conventional full bridge inverter where Sinusoidal Pulse Width Modulation (SPWM) control technique is applied. The disadvantage of this power conversion scheme is, that the size of the magnetic components must be designed for the fundamental component instead of the inverter switching frequency. Consequently, the high inverter switching frequency cannot be exploited for reducing the size of the isolation transformer. Furthermore, the power conversion scheme shown in Fig. 2.1 has no means of regulating the inverter input voltage or means of changing the inverter input voltage to a level which would optimize the performance of the inverter components. These drawbacks result in substantial power underrating of the overall inverter unit.

Fig. 2.2 shows the proposed power conversion scheme that has none of the above disadvantages, but it does require an additional power conversion stage. This additional stage is a High Frequency (HF) DC to DC link which inputs the unregulated DC bus voltage and outputs a regulated DC voltage at any desired level. The HF link includes a high frequency transformer which provides isolation at switching frequency, thus resulting in substantial cost, size, and weight reduction for the isolation transformer. The remaining power conversion stage consists of a full bridge DC to AC inverter. Note that because of the high switching frequency the input filter

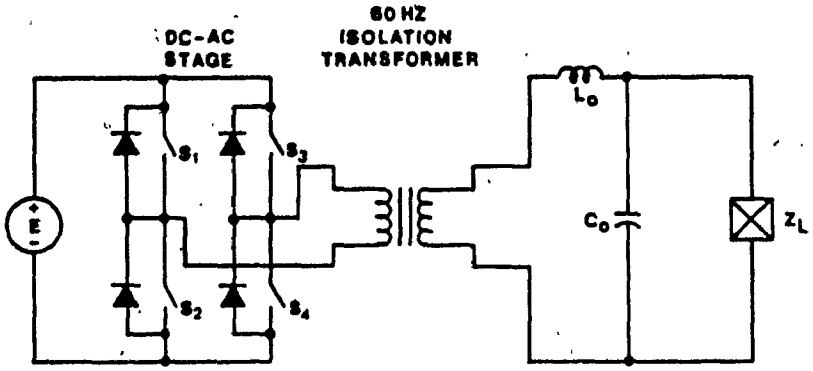


Fig. 2.1: Schematic diagram of the conventional inverter configuration.

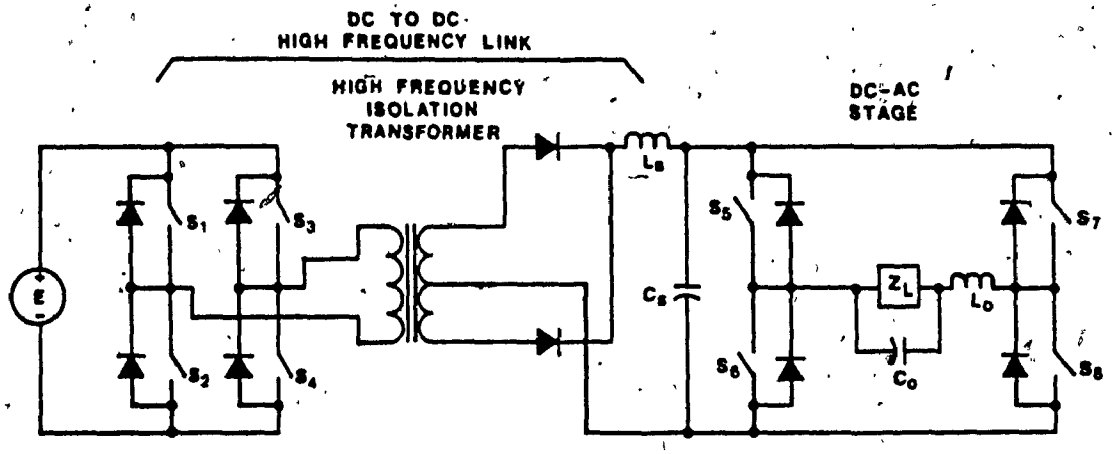


Fig. 2.2: Schematic diagram of the proposed inverter configuration.

components can also be reduced. Furthermore, circuit protection is performed in the HF link stage.

2.2 System description

A variety of semiconductor switches are available that can be used to implement the proposed inverter system. Depending on the DC bus voltage and rated output power these devices can be transistors, GTOs, Assymmetrical SCRs or traditional thyristors. Fig. 2.3 shows a family of transistorized power conversion units employing the proposed scheme. In particular,

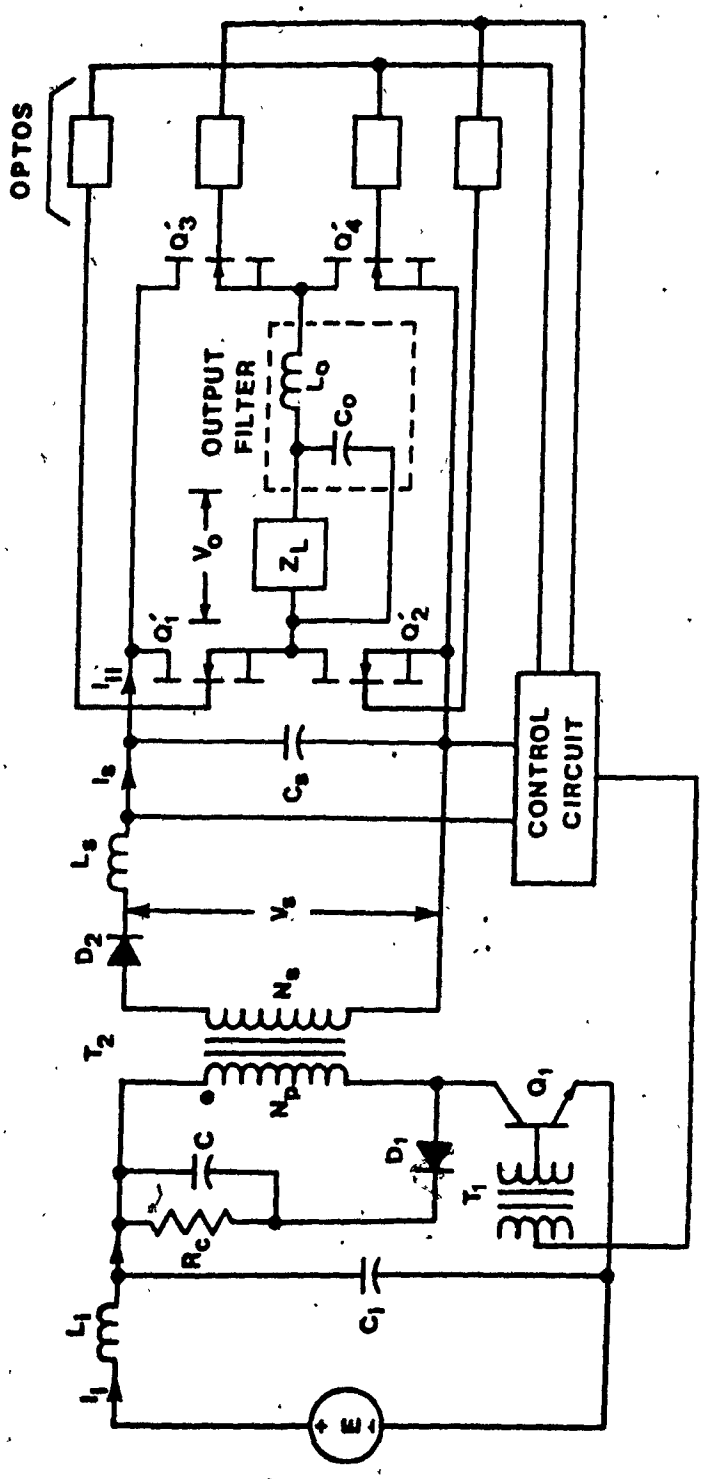
Fig. 2.3(a) shows the flyback configuration,

Fig. 2.3(b) the push-pull configuration, and

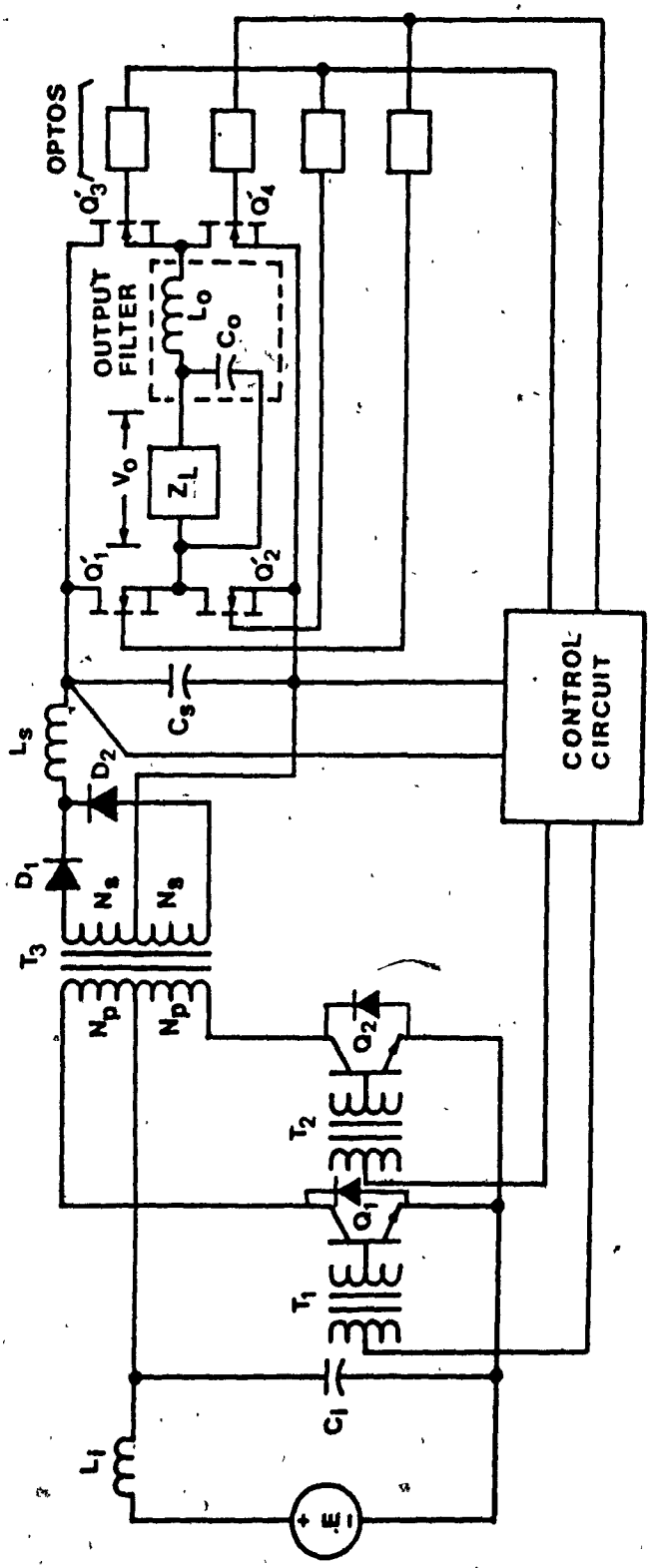
Fig. 2.3(c) the full bridge configuration.

The flyback configuration requires fewer components than the others, resulting, in reduced cost and higher reliability. In addition, there is no "switch through" problem with flyback HF link stage. However, in the flyback configuration the voltage and current stresses of the power switches in the HF link stage are increased by a factor of two compared to the stresses of the power switches in the push-pull and full bridge configurations. Moreover, since the flyback is a forward converter it cannot function without a voltage control loop.

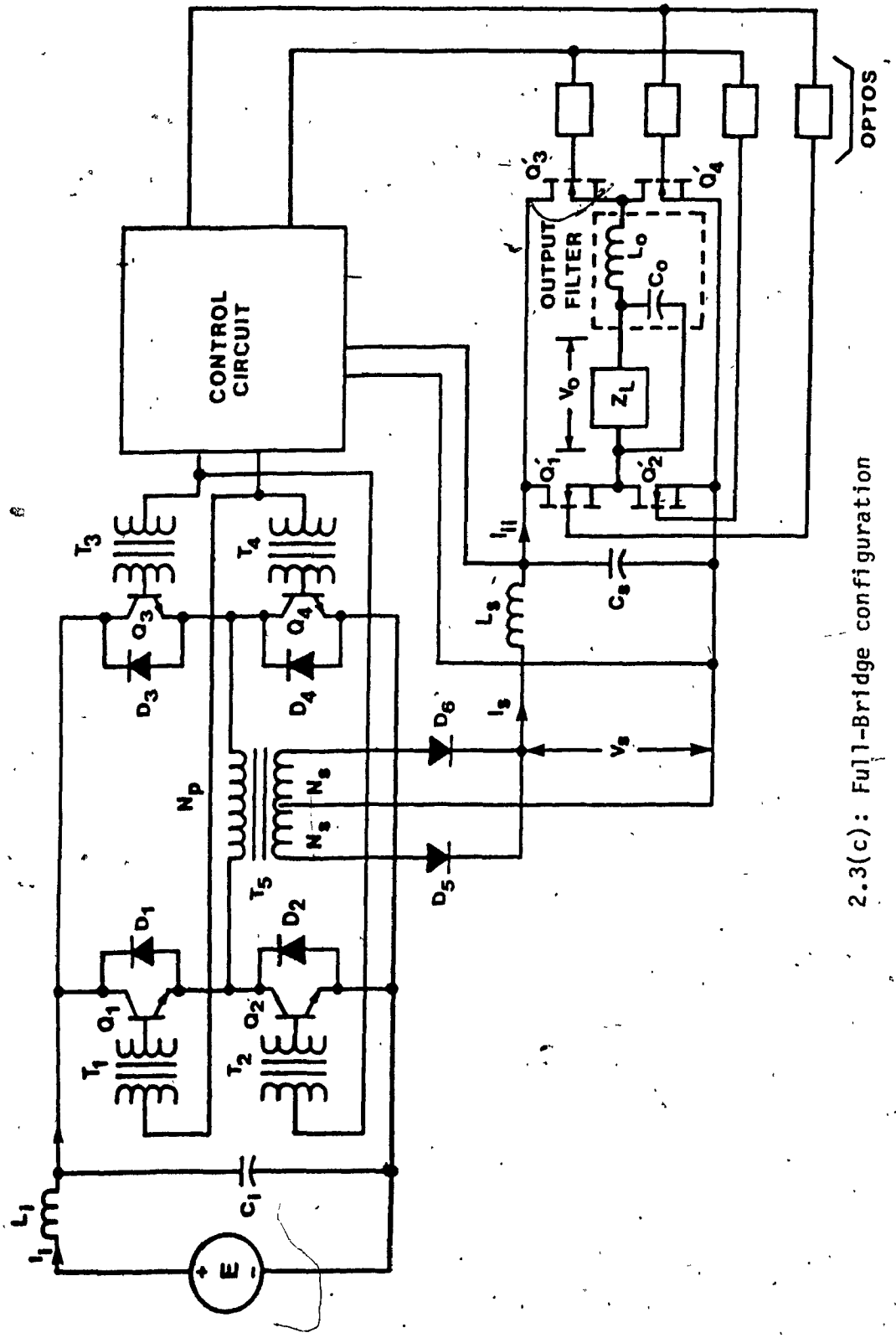
For the DC to AC inverter stage, the full bridge inverter was chosen because it utilizes the full DC bus provided by the HF link and also when connected to the HF link there is no need for centertaping. Since the inverter system output voltage waveform consists of train of pulses (Fig. 2.4(d)) some form of filtering is necessary in order



2.3(a): Flyback configuration



2.3(b): Push-Pull configuration



2.3(c): Full-Bridge configuration

FIG. 2.3: A family of transistorized inverters employing the proposed Power Conversion Scheme.

to separate the fundamental harmonic component from the unwanted components. Moreover, by employing proper switching function patterns (Appendix D) to the inverter stage, the size, weight, and cost of the inverter stage input and output filter components can be minimized. Finally, for this power conversion scheme, the low pass L-C filter configuration was chosen for harmonic filtering in different parts of the inverter system because it satisfies the harmonic distortion requirements with a minimum number of components.

2.3 System analysis

In this section, the proposed power conversion scheme is analyzed under steady state conditions. The derived expressions are subsequently used to obtain the information necessary for the safe design of the system. Finally, the following analysis has also been presented in reference [12].

2.3.1 Load conditions

In order to generalize the analysis of the proposed power conversion scheme the rated output voltage, V_o, and rated output current, I_o, are expressed in per unit as follows:

$$V_{o(rms)} = 1 \text{ p.u. (volts)} \tag{2.1}$$

$$I_{o(rms)} = 1 \text{ p.u. (Amps)} \tag{2.2}$$

2.3.2 Derivation of the inverter stage switching function, $S(\omega t)$

Experience with static converters has shown that the most useful analytical information is obtained when the converter is viewed by the input and output ports as a multi-frequency AC current and/or voltage source generator (Appendix D).

Consequently the converter can be modelled as a black box whose transfer characteristics are analytically described by the Fourier series expansion of its respective set of switching functions [13], [14], [15]. By multiplying converter switching functions with expressions describing respective input voltages, analytical expressions for the converter output voltages are obtained. Therefore, by properly selecting the converter switching functions elimination of unwanted harmonic components from its input or output ports can be achieved. Moreover, the required component ratings are calculated from the product of line currents and voltages with the appropriate switching functions.

There is a number of switching functions that can be employed with the inverter stage for elimination of unwanted harmonic components. These switching functions can be of the following two types:

a) Fixed pattern programmable switching functions [16]. Normally these types of switching functions are employed where small numbers (up to seven) of unwanted harmonic components are to be eliminated, and slow turn-off switching devices (GTOs or Thyristors) are used for the implementation of the power conversion stages. When large numbers of unwanted harmonic components are to be eliminated, this technique becomes analytically very complex. Moreover, considerable computer execution time is needed in order to obtain the required switching angles. Using this technique the resulting maximum RMS value of the fundamental component

of the inverter output voltage is 8.2% less than the value of the DC bus voltage provided by the HF link stage.

b) Fixed pattern switching functions obtained with Sinusoidal Pulse Width Modulation (SPWM) technique by setting the Modulation factor equal to one. These functions can easily employ high switching frequencies. Consequently, they are compatible with fast turn-off switching devices (Bipolars or MosFets). Because of the high switching frequencies that can be realized, the unwanted dominant harmonic component (Appendix C) can be shifted far away from the fundamental (as in Fig. 2.4(e)). This feature can be utilized to reduce the size of the output filter components. Using this technique the resulting maximum RMS value of the fundamental component of the inverter output voltage is 29.3% less than the value of the DC bus voltage provided by the HF link stage.

As mentioned earlier in the introduction of this thesis and in the introduction of this chapter, one of the requirements of the inverter besides the reduction of the isolation transformer was the reduction of the input and output filter components. The reduction of the output filter components requires high-order dominant harmonic components which can be achieved with the employment of high inverter stage switching frequencies. Therefore, since the SPWM fixed pattern can employ high switching frequencies it was chosen as the inverter stage switching function.

Fig. 2.4 shows the derivation of the inverter stage switching function obtained by applying the single-phase unidirectional SPWM technique. The significant variables in the switching functions resulting from the SPWM technique are:

a) The ratio of the normalized carrier frequency, f_{nc}, defined as $f_{nc} = \frac{T_f}{T_c}$ (Fig. 2.4(a)),

b) The modulation factor, M_f, defined as

$$M_f = \frac{V_f}{V_c} \quad \text{(Fig. 2.4(a))}.$$

Furthermore, results obtained with the developed computer program (Appendix A) have shown that for Modulation factor equal to one

a) the value of the normalized carrier frequency (f_{nc}) and the order of the dominant harmonic component (d) of the switching function ($S(\omega t)$) are related by

$$d = 2 f_{nc} - 3 \qquad (2.3)$$

b) the amplitude of the fundamental component of the switching function ($S(\omega t)$) is independent of the value of the normalized carrier frequency (f_{nc}) and is given by

$$A_1 = 1 \qquad (2.4)$$

c) the amplitude of the dominant harmonic component (d) of the switching function ($S(\omega t)$) is independent of the value of the normalized carrier frequency (f_{nc}) and is given by

$$A_d = 0.2 \qquad (2.5)$$

Although switching function patterns (such as Fig. 2.4(d)) help to visualize the generated inverter stage voltage and current waveforms,

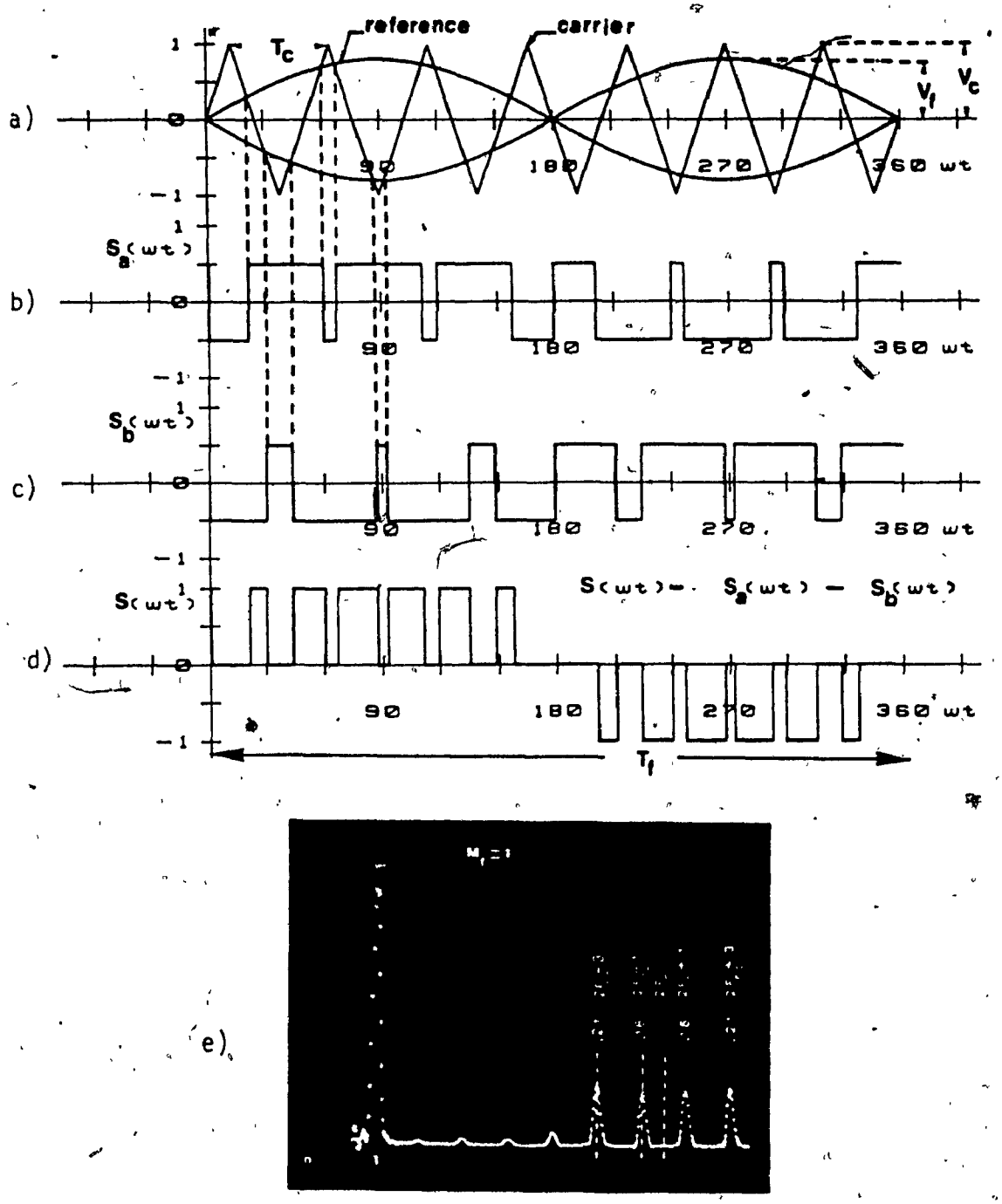


Fig. 2.4: Derivation of the inverter stage switching function, $S(\omega t)$, and its respective frequency spectrum.

they are not suitable for further analytical work. Effective inverter stage analysis requires that the function $S(\omega t)$ should be expressed mathematically. Such expression can be obtained by deriving its Fourier series expansion which is given by

$$S(\omega t) = \sum_{n=1,odd}^{\infty} A_n \sin(n\omega_o t)$$

$$= A_1 \sin(\omega_o t) + \sum_{n=d}^{\infty} A_n \sin(n\omega_o t) \qquad (2.6)$$

where:

ω_o is the inverter operating frequency,

A_1 is the amplitude of the fundamental component of the inverter stage switching function, $S(\omega t)$,

A_n is the amplitude of the nth harmonic component of the inverter stage switching function, $S(\omega t)$,

d is the dominant harmonic component of the inverter stage switching function, $S(\omega t)$.

Therefore, using eqn. (2.6) and the expressions given in Appendix D the inverter stage input and output quantities can be found in mathematical form.

2.3.3 Inverter stage

Regarding Fig. 2.3 and using the switching function relations given in Appendix D the inverter stage output voltage and current are given by

$$V_{1f}(\omega t) = V_{s,o}\, S(\omega t) \qquad (2.7)$$

$$I_{if}(\omega t) = \frac{V_{if}(\omega t)}{Z_o(\omega t)} \tag{2.8}$$

where:

$V_{s,o}$ is the dc component of the voltage provided by the HF link stage (Fig. 2.3),

Z_o is the input impedance of the output filter.

By employing eqn. (2.6) eqns. (2.7) and (2.8) become

$$V_{if}(\omega t) = V_{s,o}\sin(\omega_o t) + V_{s,o}\sum_{n=d}^{\infty} A_n \sin(n\omega_o t) \tag{2.9}$$

$$I_{if}(\omega t) = \frac{V_{s,o}\sin(\omega_o t+\phi_1)}{|Z_{o,1}|} + V_{s,o}\sum_{n=d}^{\infty}\frac{A_n \sin(n\omega_o t+\phi_n)}{|Z_{o,n}|}$$

$$= \sum_{n=1,odd}^{\infty} B_n \sin(n\omega_o t + \phi_n) \tag{2.10}$$

where:

B_n is the amplitude of the nth harmonic component of the inverter stage output current, $I_{if}(\omega t)$,

$|Z_{o,n}|$ is the magnitude of Z_o at the nth harmonic frequency,

$$\phi_n = \tan^{-1}\left(\frac{\text{Imag}(Z_{o,n})}{\text{Real}(Z_{o,n})}\right) \tag{2.11}$$

ϕ_1 is the phase displacement between respective fundamental components of $V_{if}(\omega t)$ and $I_{if}(\omega t)$. For $f_{nc} \geq 17$, $X_{C_o} = 2$ p.u. and $X_{L_o} < .1$ p.u. was found that $\phi_{1(max)} = 51°$ and $\phi_{1(min)} = 0°$ for loads vary from 0.8 leading to 0.8 lagging.

Eqn. (2.9) implies that in order to obtain 1 p.u. rms load voltage (exp. 2.1) the dc component $V_{s,o}$, of the inverter stage input voltage must be

$$V_{s,o} = \sqrt{2} \text{ p.u.} \tag{2.12}$$

Also, by using exps. (2.5) and (2.9) the amplitude of the dominant harmonic component of the inverter stage output voltage, $V_{if,d}$, is found to be

$$V_{if,d} = V_{s,o} \cdot A_d = (\sqrt{2})(0.2) = 0.28 \text{ p.u.} \qquad (2.13)$$

The simulated waveforms with their respective spectra for the voltage and current quantities defined in eqns. (2.9) and (2.10), under worst operating condition for component ratings (0.8 leading power factor) and $f_{nc} = 7$ (f_{nc} has been intentionally chosen low and equal to 7 for waveform clarity), are shown in Figs. 2.5(a) and (b). These waveforms have been obtained by incorporating the aforementioned expressions in the computer program discussed in Appendix A and can be used for computing the inverter stage main component voltage and current ratings.

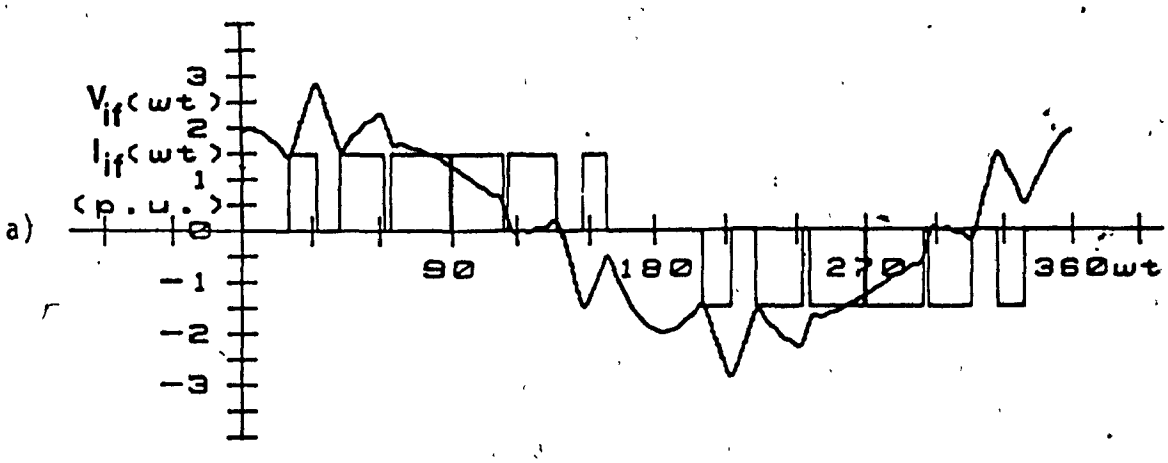
In order to be able to obtain design guidelines for the inverter stage input filter the frequency spectrum of the inverter stage input current has to be known. Therefore, regarding Fig. 2.3 and using the switching function relations given in Appendix D the inverter stage input current, $I_{ii}(\omega t)$, is given by

$$I_{ii}(\omega t) = I_{if}(\omega t) \cdot S(\omega t) \qquad (2.14)$$

Substituting eqns. (2.6) and (2.10) into eqn. (2.14)

$$I_{ii}(\omega t) = \sum_{n=1,\text{odd}}^{\infty} B_n \sin(n\omega_o t + \phi_n) \cdot \sum_{n=1,\text{odd}}^{\infty} A_n \sin(n\omega_o t) \qquad (2.15)$$

Simplifying further eqn. (2.15) the mth harmonic component of the inverter stage input current is given by



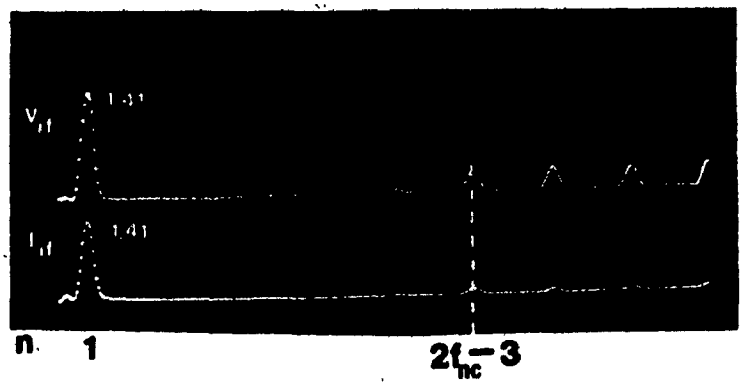


Fig. 2.5: Simulated waveforms with their respective frequency spectra for voltage and current before output filtering, $V_{if}(\omega t)$ and $I_{if}(\omega t)$, obtained with P_f=0.8 leading, M_f=1 and f_{nc}=7.

$$I_{ii,m}(\omega t) = \frac{1}{2}\left[-\sum_{k=1,odd}^{m-1} A_{m-k}B_k \cos(m\omega_o t + \phi_{m-k}) + \sum_{k=1,odd}^{\infty} A_{m+k}B_k \cos(m\omega_o t + \phi_{m+k}) + \sum_{n=1,odd}^{\infty} A_n B_{m+n} \cos(m\omega_o t - \phi_n)\right] \quad (2.16)$$

Where:

$m = 2, 4, 6, 8, \ldots$

Consequently, using eqn. (2.16) the amplitude of the dc and second-order components are given by

$$I_{ii,o} \simeq \frac{A_1 B_1}{2} \cos\phi_1 \quad (2.17)$$

$$I_{ii,2} \simeq \frac{A_1 B_1}{2} \quad (2.18)$$

where:

A_1 is the amplitude of the fundamental component of the inverter stage switching function given by eqn. (2.4),

B_1 is the amplitude of the fundamental component of the inverter stage output current, $I_{if}(\omega t)$, given by

$$B_1 = \sqrt{2} \text{ p.u.} \quad (2.19)$$

for $f_{nc} \geq 17$ (Realistic values of f_{nc} for HF applications)

Furthermore, using exps.(2.4), (2.17), (2.18) and (2.19) and assuming

that the normalized carrier frequency $f_{nc} \geq 17$ (since high switching frequency is applied to the inverter stage) the following expressions required for the inverter stage input filter design are obtained

$$I_{ii,o(min)} = \frac{(1)(\sqrt{2})(\cos 51°)}{2} = .5 \text{ p.u.} \quad (2.20)$$

$$I_{ii,o(max)} = \frac{(1)(\sqrt{2})(1)}{2} = 0.707 \text{ p.u.} \quad (2.21)$$

$$I_{ii,2} = \frac{(1)(\sqrt{2})}{2} = 0.707 \text{ p.u.} \quad (2.22)$$

Finally, Fig. 2.6 shows the simulated waveform of the inverter stage input current, $I_{ii}(\omega t)$, and its respective frequency spectrum obtained with 0.8 leading power factor and $f_{nc} = 7$.

2.3.4 Output filter

In most specifications for power supplies the Total Harmonic Distortion (THD, see appendix C) content of the output voltage, V_o, is $\leq$ 5% at rated load and no load conditions [17], [18]. It can be shown that if the amplitude of the dominant harmonic component ($2 f_{n_c} - 3$) is reduced to 3% of the amplitude of the fundamental then, under worst operating condition (0.8 lagging power factor), a THD $\leq$ 5% can be insured. Therefore, the value by which the amplitude of the dominant harmonic component has to be attenuated by the output filter is given by

$$\Delta A = 20 \log_{10}(0.03) - 20 \log_{10}(V_{if,d}) \quad (2.23)$$

Therefore, using exps. (2.13) and (2.23)

$$\Delta A = - 19.4 \text{ db} \quad (2.24)$$

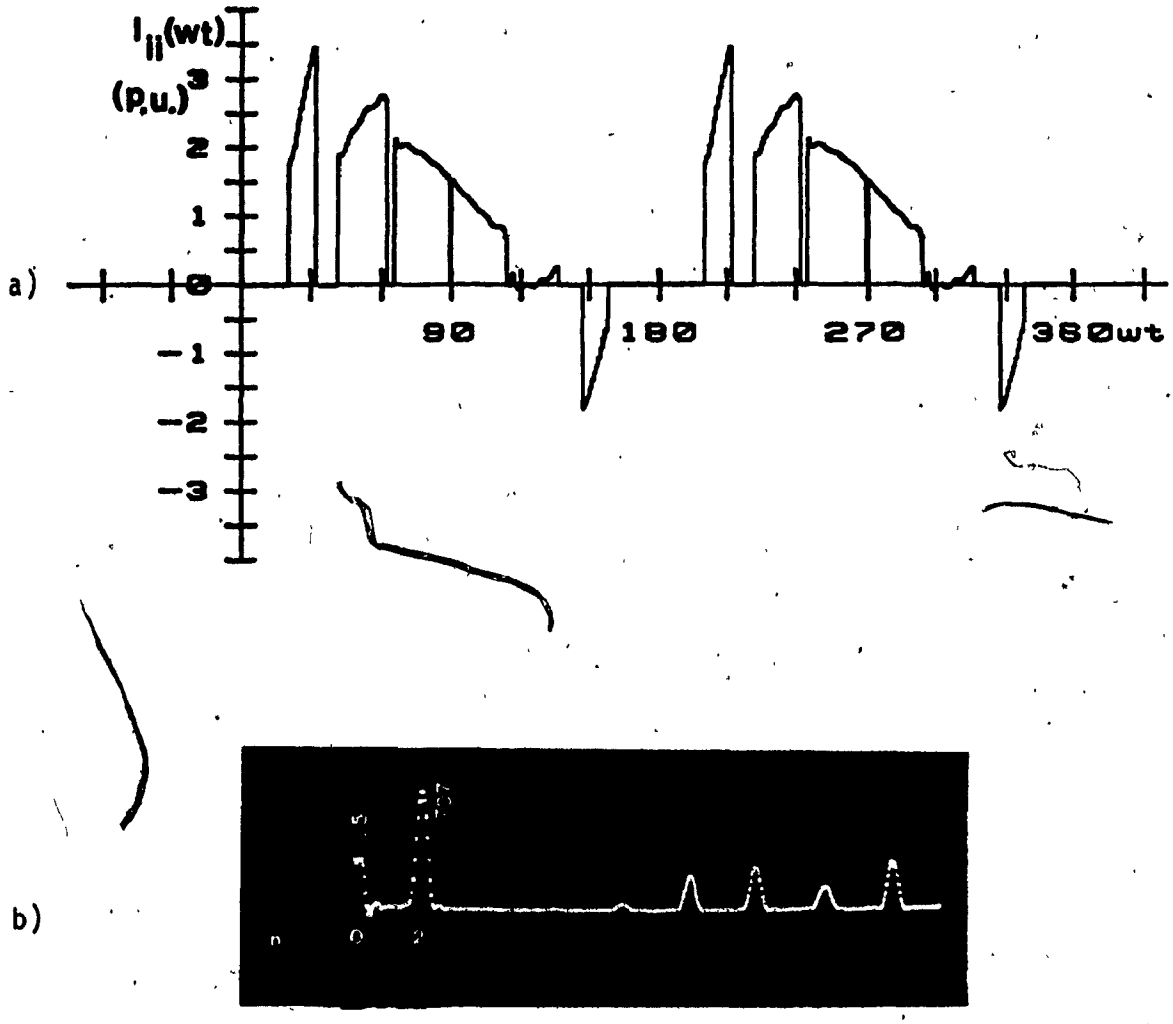


Fig. 2.6: Simulated waveform of the inverter stage input current, $I_{ii}(\omega t)$, and its respective frequency spectrum obtained with P_f=0.8 leading, M_f=1 and f_{nc}=7.

To achieve this attenuation a second order LC filter was chosen for its simplicity (Fig. 2.3). Using the characteristics of the second-order filter and exp.(2.24) the following expression is obtained

$$\frac{19.4}{\log_{10}\omega_{bo}-\log_{10}(2f_{nc}-3)} = \frac{40}{\log_{10}\omega_{bo}-\log_{10}10\omega_{bo}} \qquad (2.25)$$

where:

f_{nc} is the normalized carrier frequency

ω_{bo} is the break frequency of the output filter $\triangleq 1/\sqrt{L_o C_o}$

After further simplification eqn. (2.25) becomes

$$\omega_{bo} = (2f_{nc}-3)(10)^{-19.4/40} \text{ p.u.} \qquad (2.26)$$

where:

1 p.u. frequency is the inverter system operating frequency, ω_o.

Consequently, using eqn. (2.26) the output filter components are given by

$$\frac{X_{L_{o,1}}}{X_{C_{o,1}}} = L_o C_o = \frac{9.32}{(2f_{nc}-3)^2} \text{ p.u.} \qquad (2.27)$$

where:

L_o is the inductance of the output filter,

C_o is the capacitance of the output filter,

$X_{L_{o,1}}$ is the reactance of the output filter inductor at operating frequency,

$X_{C_{o,1}}$ is the reactance of the output filter capacitor at operating frequency,

f_{nc} is the normalized carrier frequency.

There is no "right" answer to how the two filter components should be chosen but the following factors should be considered:

i) In order to prevent the resonance condition in the filter the following inequalities must hold

$$\omega_o L_o < \frac{1}{C_o \omega_o} \quad ; \text{ for the fundamental component}$$

$$d\omega_o L_o > \frac{1}{d\omega_o C_o} ; \text{ for the dominant component}$$

ii) A low L_o/C_o ratio results in larger peak output current, when initially the inverter unit is switched on.

iii) A low L_o/C_o ratio will dissipate much more power.

Therefore, since the output filter input quantities ($V_{if}(\omega t)$, $I_{if}(\omega t)$) are given by eqns. (2.9) and (2.10) respectively and using eqn. (2.27) the expressions for the load voltage and current are expressed as follows:

$$V_o(\omega t) = \sum_{n=1,odd}^{\infty} V_{o,n} \sin(n\omega_o t + \theta_v) \qquad (2.28)$$

$$I_o(\omega t) = \sum_{n=1,odd}^{\infty} I_{o,n} \sin(n\omega_o t + \theta_I + \phi_n) \qquad (2.29)$$

respectively,

where:

$$V_{o,n} = \sqrt{(V_{s,o} \cdot A_n + B_n \cdot X_{L_o} \sin\phi_n)^2 + (B_n \cdot X_{L_o} \cos\phi_n)^2} \qquad (2.30)$$

$$I_{o,n} = \frac{|V_{o,n}|}{|Z_{L,n}|} \qquad (2.31)$$

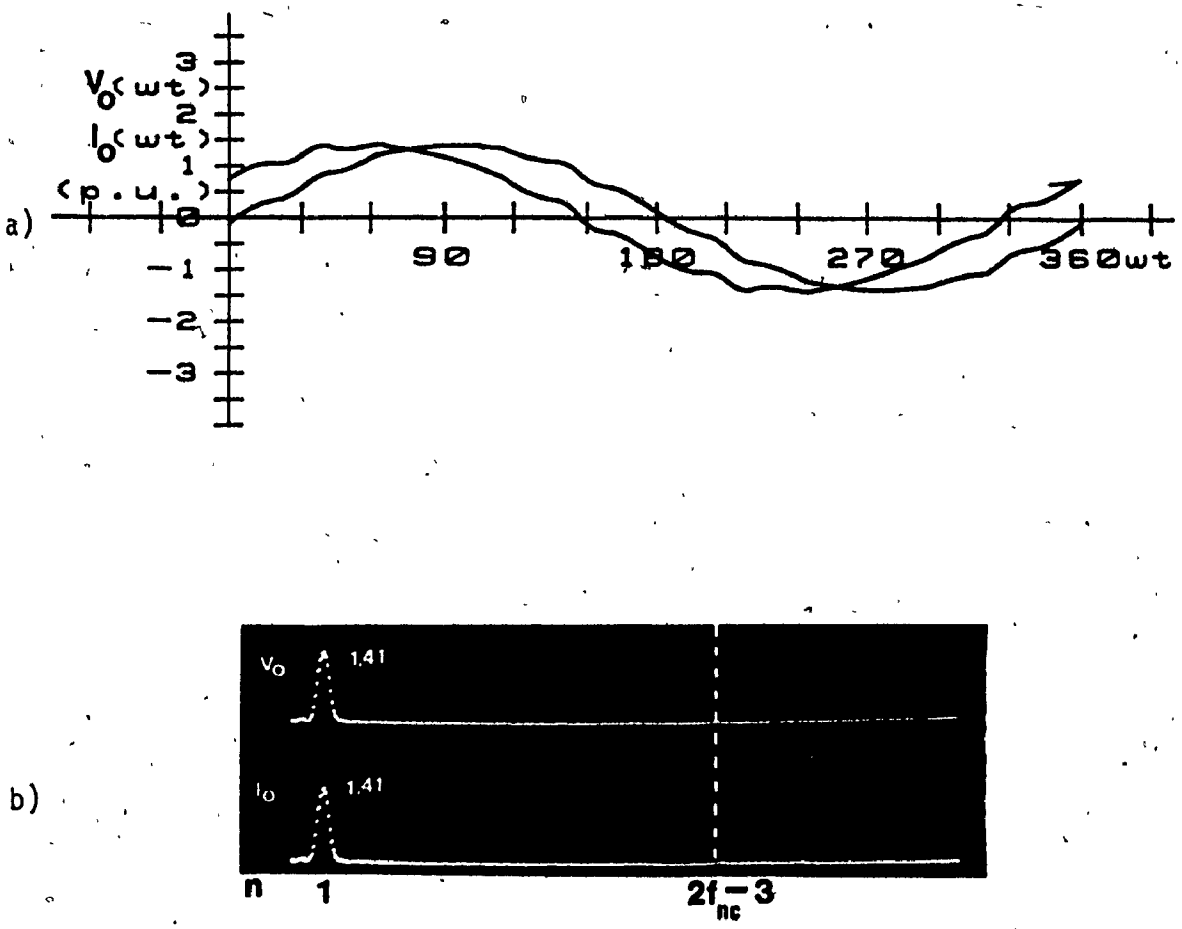


Fig. 2.7: Simulated waveforms with their respective frequency spectra for load voltage and current, $V_o(\omega t)$ and $I_o(\omega t)$, obtained with P_f=0.8 leading, M_f=1 and f_{nc}=7.

and where:

$Z_{L,n}$ is the load impedance at the nth harmonic frequency,

θ_v is the voltage phase shift introduced by the output filter

θ_I is the current phase shift introduced by the output filter

Finally, the simulated waveforms with their respective spectra for load voltage and current quantities, $V_o(\omega t)$ and $I_o(\omega t)$, are shown in Figs. 2.7(a) and (b). These waveforms have been obtained by incorporating the expressions (2.28), (2.29), (2.30) and (2.31) in the computer program in Appendix A.

2.3.5 Inverter stage input filter

The factors affecting the reactive components (L_s,C_s) of the inverter stage input filter are:

a) The specified filter inductor current ripple factor, K_{i_s}.

b) The specified filter capacitor voltage ripple factor, K_{v_s}.

c) The specified switching frequencies of the HF link and inverter stage.

Fig. 2.8(a) shows the harmonic equivalent circuit of the inverter stage input filter. As it can be seen the filter is subjected to two types of harmonics. Current harmonic components reflected by the

inverter stage and voltage harmonic components generated by the HF link stage. However, since the switching frequency of the HF link is normally much higher than the switching frequency of the inverter stage, the main contributor to the size of the filter is the second-order harmonic component that is reflected by the inverter stage. Therefore, the final harmonic equivalent circuit can be presented as shown in Fig. 2.8(b).

Regarding Fig. 2.8(b) the filter inductor current and filter capacitor voltage are given by,

$$I_{s,n} = \frac{1}{\frac{n^2 X_{L_{s,1}}}{X_{C_{s,1}}} - 1} I_{ii,n} \qquad (2.32)$$

$$V_{s,n} = \frac{n X_{L_{s,1}} X_{C_{s,1}}}{n^2 X_{L_{s,1}} - X_{C_{s,1}}} I_{ii,n} \qquad (2.33)$$

where:

$I_{s,n}$ is the amplitude of the nth harmonic component of the filter inductor current,

$X_{L_{s,1}}$ is the reactance of the filter inductor at operating frequency,

$X_{C_{s,1}}$ is the reactance of the filter capacitor at operating frequency,

n is the harmonic order.

The filter inductor current ripple factor (Appendix C), K_{I_s}, and filter capacitor voltage ripple factor, K_{V_s}, are given by

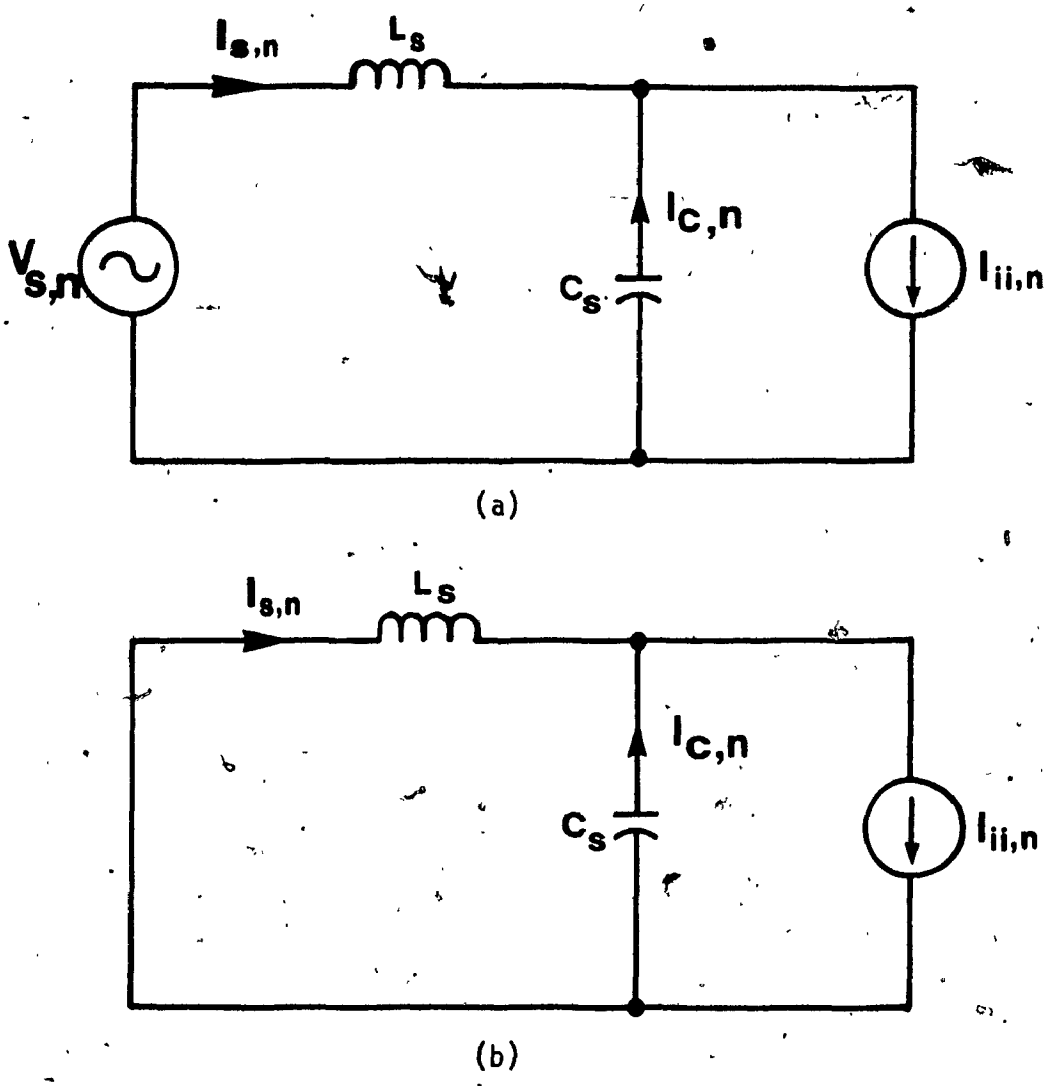


Fig. 2.8: Determination of the inverter stage input ripple current and input ripple voltage.

a) Harmonic equivalent circuit of the inverter stage input filter

b) Final harmonic equivalent circuit of the inverter stage input filter

$$K_{i_s} = \frac{\left[\sum_{n=1}^{\infty} I_{s,n(rms)}^2\right]^{1/2}}{I_{s,o}} \simeq \frac{I_{s,2(rms)}}{I_{s,o}} \qquad (2.34)$$

$$K_{v_s} = \frac{\left[\sum_{n=1}^{\infty} V_{s,n(rms)}^2\right]^{1/2}}{V_{s,o}} \simeq \frac{V_{s,2(rms)}}{V_{s,o}} \qquad (2.35)$$

where:

$I_{s,o}$ is the dc component of the filter inductor current = $I_{ii,o}$,

$I_{s,2(rms)}$ is the rms value of the second-order harmonic component of the filter inductor current,

$V_{s,o}$ is the dc component of the filter capacitor voltage,

$V_{s,2(rms)}$ is the rms value of the second-order harmonic component of the filter capacitor voltage.

Substituting eqns. (2.32) and (2.33) into eqns. (2.34) and (2.35)

$$K_{i_s} = \frac{1}{(4\frac{X_{L_{s,1}}}{X_{C_{s,1}}} - 1)I_{s,o}} I_{ii,2(rms)} \qquad (2.36)$$

$$K_{v_s} = \frac{2X_{L_{s,1}} X_{C_{s,1}}}{(4X_{L_{s,1}} - X_{C_{s,1}})V_{s,o}} I_{ii,2(rms)} \qquad (2.37)$$

Consequently, substituting exps. (2.12), (2.20) and (2.22) into exps. (2.36) and (2.37) the relations of the filter components as a function of the ripple factors are given by

$$\frac{X_{L_{s,1}}}{X_{C_{s,1}}} = \frac{0.25}{K_{i_s}} + K_{i_s} \quad \text{p.u.} \tag{2.38}$$

$$\frac{X_{L_{s,1}} X_{C_{s,1}}}{4X_{L_{s,1}} - X_{C_{s,1}}} = 1.414 K_{v_s} \text{ p.u.} \tag{2.39}$$

Therefore, given the allowable values of K_{i_s} and K_{v_s} and solving the system of eqns. (2.38) and (2.39) the filter component values can be obtained.

2.3.6 HF link stage

Depending on the output power requirements of the inverter one of the following configurations of the DC to DC converters can be used as a HF link in order to regulate DC bus of the inverter stage.

2.3.6.1 Flyback configuration

Regarding Fig. 2.3(a)

$$\frac{V_{s,o}}{V_p} = \frac{N_s}{N_p} \left(\frac{D}{1-D}\right) \tag{2.40}$$

where :

N_p is the isolation transformer primary winding number of turns,

N_s is the isolation transformer secondary winding number of turns,

V_p is the voltage across the primary of the isolation transformer,

$V_{s,o}$ is the dc component of the inverter stage input voltage,

D is the Duty cycle = $\frac{\text{Transistor ON time}}{\text{Transistor OFF time}}$

but since V_p is equal to E and using eqn. (2.12) then eqn. (2.40) becomes

$$\frac{N_s}{N_p} = \frac{\sqrt{2}\, K_c(1-D)}{D} \tag{2.41}$$

where :

$$K_c = \frac{V_{o(rms)}}{E} \tag{2.42}$$

The number of turns in the primary of the transformer is given by [19]

$$N_p = \frac{E \times 10^8}{4.44\, f_\ell A_c B_{max}} \tag{2.43}$$

where :

f_ℓ is the switching frequency of the HF link stage,

A_c is the transformer core cross section area in cm^2,

B_{max} is the maximum flux density in Gauss (1 Weber/cm^2 = 10^8 Gauss).

Regarding Fig. 2.3(a) the peak current that flows through the primary of the isolation transformer is given by

$$\hat{I}_p = \hat{I}_s \left(\frac{N_s}{N_p}\right) \tag{2.44}$$

From Figs. 2.9(a) and (b), which illustrate the waveforms of the current that flows through the primary and secondary windings of the isolation transformer, can be shown that

$$\hat{I}_s = \frac{I_{s,o(max)}}{(1-D)} + \frac{\Delta I_s}{2} \tag{2.45}$$

where :

ΔI_s is the peak to peak allowable inverter stage input ripple current given by

$$= 2\sqrt{2}\, K_{i_s}\, I_{s,o(max)} \qquad (2.46)$$

K_{i_s} is the inverter stage input filter inductor current ripple factor,

$I_{s,o(max)}$ is the maximum dc component supplied to the inverter stage and is given by eqn. (2.21).

Therefore, substituting eqns. (2.21), (2.45) and (2.46) into (2.44) and assuming maximum duty cycle equal to 0.45 then

$$\hat{I}_p = 1.22K_c(2.2 + \sqrt{2}\, K_{i_s})\ \text{p.u.} \qquad (2.47)$$

Regarding Fig. 2.3(a) the peak voltage across transistor Q_1 during OFF period is given by

$$\hat{V}_{CE(Q_1)} = E + \left(\frac{N_p}{N_s}\right) V_{s,o} \qquad (2.48)$$

and by using eqns. (2.41), (2.42) and (2.13) then eqn. (2.48) for maximum duty cycle of 0.45 becomes

$$\hat{V}_{CE(Q_1)} = \frac{1.8}{K_c}\ \text{p.u.} \qquad (2.49)$$

2.3.6.2 Push-Pull and Full bridge configurations

Since for the Push-Pull and Full bridge configurations the voltage across the primary of the isolation transformer is equal to E (Figs. 2.3 (b) and (c)) then the transformer turns ratio is given by

$$\frac{N_s}{N_p} = \frac{V_{s,o}}{2\ E\ D_{max}} = \frac{\sqrt{2}\ K_c}{2\ D_{max}} \tag{2.50}$$

The peak current that flows through the primary of the transformer excluding the magnetizing current is given by

$$\hat{I}'_p = \hat{I}_s\ (\frac{N_s}{N_p}) \tag{2.51}$$

From Figs. 2.9(c) and (d), which illustrates the waveforms of the current that flow through the primary and secondary windings of the transformer, can be shown that

$$\hat{I}_s = \frac{I_{s,o(max)}}{2D_{max}} + \sqrt{2}\ K_{i_s}\ I_{s,o(max)}$$

$$= I_{s,o(max)}\ (\sqrt{2}\ K_{i_s} + \frac{1}{2D_{max}}) \tag{2.52}$$

Assuming that the maximum duty cycle is equal to 0.45 and using eqns. (2.21), (2.50) and (2.52) then eqn. (2.51) becomes

$$\hat{I}'_p = 1.1\ K_c\ (1.1 + \sqrt{2}\ K_{i_s})\ \text{p.u.} \tag{2.53}$$

Also, assuming that the magnetizing current is 10% of $\hat{I}'_p$ then the total peak current that flows through the primary is given by

$$\hat{I}_p = 1.2\ K_c\ (1.1 + \sqrt{2}\ K_{i_s})\ \text{p.u.} \tag{2.54}$$

2.4 Inverter system main component ratings

In this section the ratings of the inverter main components are given as follows:

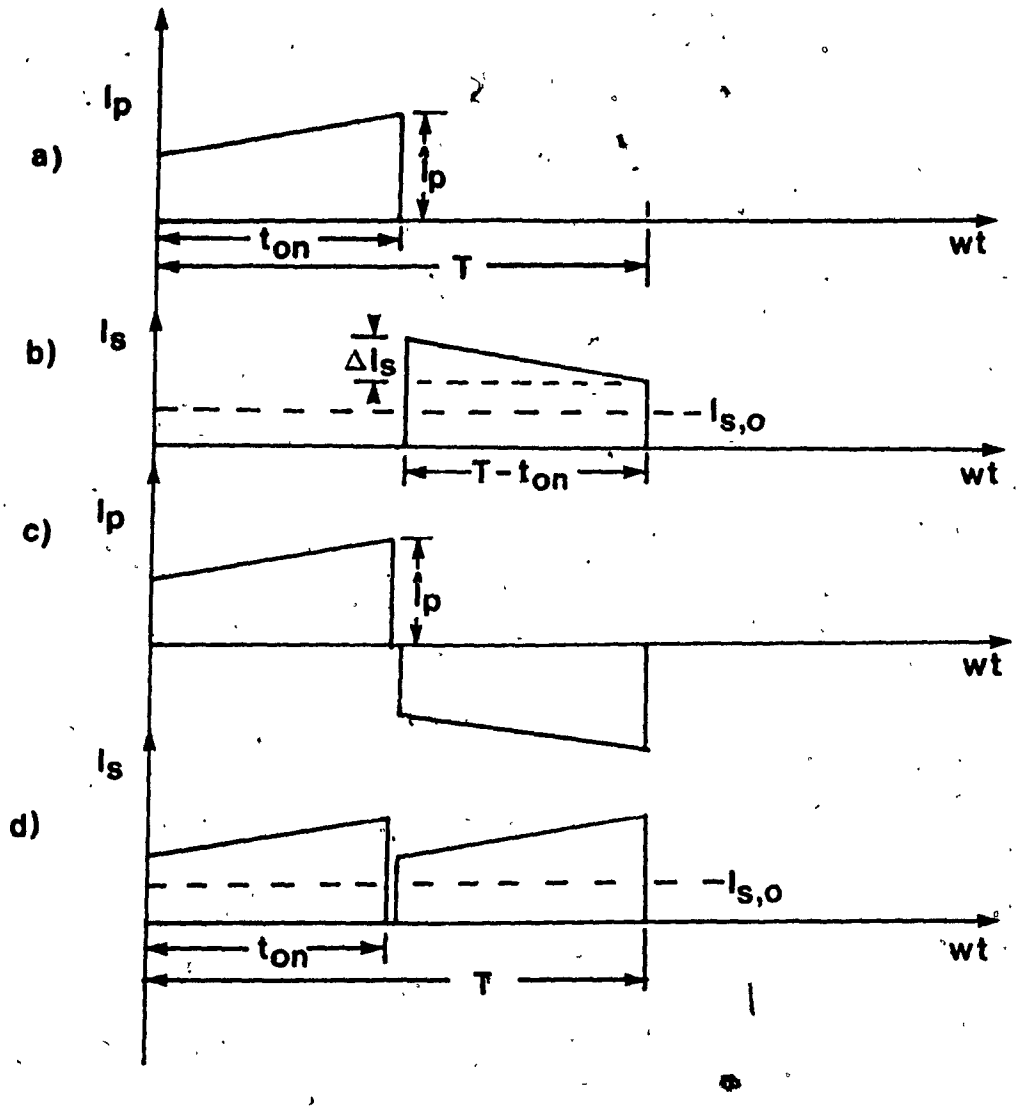


Fig. 2.9: Isolation transformer primary and secondary currents.

(a), (b) Flyback configuration

(c), (d) Push-Pull and Full bridge configurations

Inverter Stage

Peak switch current $I_{PS} = \sqrt{2}$ p.u. (2.55)

RMS switch current $I_{RS} = \frac{\sqrt{2}}{2}$ p.u. (2.56)

Average switch current $I_{AS} = \frac{\sqrt{2}}{\pi}$ p.u. (2.57)

HF Link Stage

a) Flyback configuration

Peak switch current $I_{PS} = 1.22\ K_c(2.2 + \sqrt{2}\ K_{i_s})$ p.u. (2.58)

Peak forward blocking voltage $= \frac{1.8}{K_c}$ p.u. (2.59)

b) Push-Pull configuration

Peak swith current $I_{PS} = 1.2\ K_c(1.1 + \sqrt{2}\ K_{i_s})$ p.u. (2.60)

Peak forward blocking voltage = 2E (2.61)

c) Full-bridge configuration

Peak switch current $I_{PS} = 1.2\ K_c(1.1 + \sqrt{2} K_{i_s})$ p.u. (2.62)

Peak forward blocking voltage = 2E (2.63)

2.5 Design example

In order to illustrate the significance and facilitate the understanding of theoretical results obtained in previous sections the following example is given.

E = Supply voltage = 48V

$V_{o(rms)}$ = RMS load voltage = 86V

$I_{o(rms)}$ = RMS load current = 2 Amps

f_o = Inverter system output frequency = 60Hz

f_{nc} = Normalized carrier frequency = 80

$f_{n\ell} = \frac{f_\ell}{f_c}$ = Normalized link switching frequency = 380

K_{V_s} = Inverter stage input filter capacitor voltage ripple factor = 0.01

K_{i_s} = Inverter stage input filter inductor current ripple factor = 0.2

Thus

1 p.u. volts = 86 V

1 p.u. current = 2 A

1 p.u. impedance = $\frac{86}{2}$ = 43 Ω

1 p.u. frequency = $2\pi f_o$ = 377 rad/sec

Because of the output power requirements the flyback configuration inverter is chosen. From the above p.u. values and using eqn. (2.27) the output filter components are obtained

$$\frac{X_{L_{o,1}}}{X_{C_{o,1}}} = C_o L_o = \frac{9.32}{(2\times 80-3)^2} = 3.78\times 10^{-4} \text{ p.u.} \qquad \text{(E1)}$$

If a 0.5 p.u. capacitance is chosen for the output filter and using exp. (E1)

$$X_{C_{o,1}} = \frac{1}{\omega_o C} = \frac{1}{1\times 0.5} = 2 \text{ p.u.} \qquad \text{(E2)}$$

$$C_o = \frac{1}{2\times 43\times 377} = 30.8\ \mu\text{F} \qquad \text{(E3)}$$

$$X_{L_{o,1}} = \frac{3.78\times10^{-4}}{0.5} = 7.56\times10^{-4} \text{ p.u.} \quad \text{(E4)}$$

$$L_o = \frac{X_{L_{o,1}}}{\omega_o} = \frac{7.56\times10^{-4}\times 43}{377} = 86 \ \mu\text{H} \quad \text{(E5)}$$

Using eqns. (2.38) and (2.39) the inverter stage input filter components are given by

$$\frac{X_{L_{s,1}}}{X_{C_{s,1}}} = \frac{0.25}{0.2} \times 0.2 = 1.3 \text{ p.u.} \quad \text{(E6)}$$

$$\frac{X_{L_{s,1}} X_{C_{5,1}}}{4X_{L_{s,1}} - X_{C_{s,1}}} = (1.414)(0.01) = 0.0141 \text{ p.u.} \quad \text{(E7)}$$

Solving the system of eqns. (E6) and (E7)

$$X_{C_{s,1}} = 0.046 \text{ p.u.} \quad \text{(E8)}$$

$$X_{L_{s,1}} = 0.06 \text{ p.u.} \quad \text{(E9)}$$

$$C_s = \frac{1}{0.046\times43\times377} = 1,341 \ \mu\text{F} \quad \text{(E10)}$$

$$L_s = \frac{0.06\times43}{377} = 6.84 \text{ mH} \quad \text{(E11)}$$

If the maximum duty cycle is taken to be 0.45 and using exp. (2.4) the isolation transformer turns ratio is given by

$$\frac{N_s}{N_p} = \frac{(\sqrt{2})(1.8)(1-0.45)}{0.45} \simeq 3 \quad \text{(E12)}$$

Finally, using exps. (2.55) through (2.59) the ratings of inverter main components are:

HF link stage

Peak switch current = 11.0 Amps (E13)

Peak forward and reverse blocking voltage = 86 volts (E14)

Inverter stage

Peak switch current = $(\sqrt{2})(2) = 2.82$ Amps (E15)

RMS switch current = $(\frac{\sqrt{2}}{2})(2) = 1.414$ Amps (E16)

Average switch current = $(\frac{\sqrt{2}}{\pi})(2) = 2.25$ Amps (E17)

2.6 Control circuit and experimental results

There are numerous control circuits already developed for any of the three configurations of the HF link stage [20], [21]. Therefore, there is no necessity for further explanations. For the inverter stage, the control circuit shown in Fig. 2.10 has been utilized. The intersection points between the reference and carrier signals (Fig. 2.4(a)) were stored in a 16K bit EPROM. The resolution used was 0.2 degrees/bit. The overlapping protection delays between transistors in the inverter stage were incorporated in the gating signals stored in the EPROM.

In order to illustrate the significance and facilitate the understanding of theoretical results obtained in previous sections the flyback configuration inverter was built using power MOSFET transistors. Fig. 2.11 shows the experimental results which are in close agreement with the theoretical ones (Figs. 2.5(a), 2.6(a), 2.7(a)).

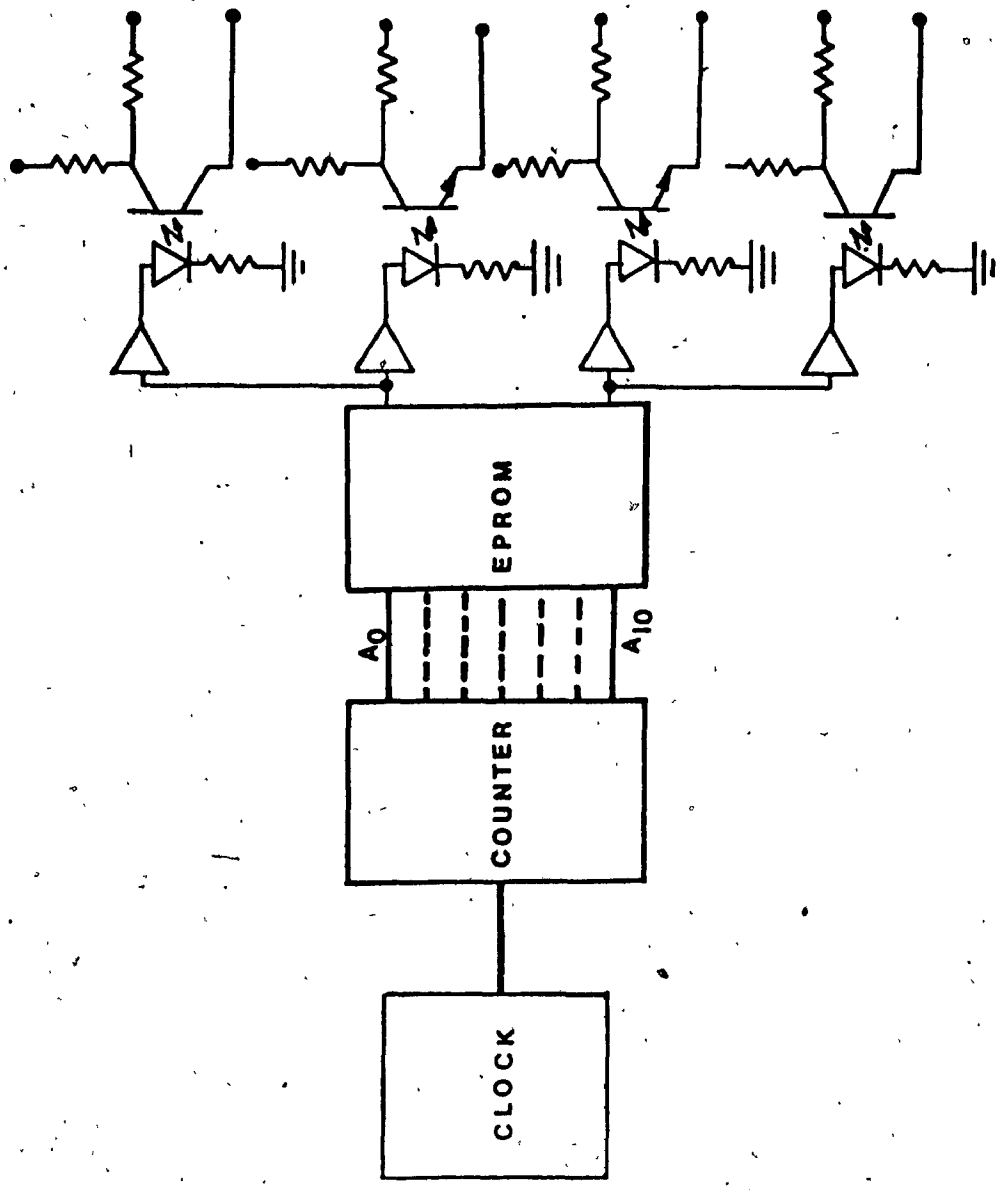
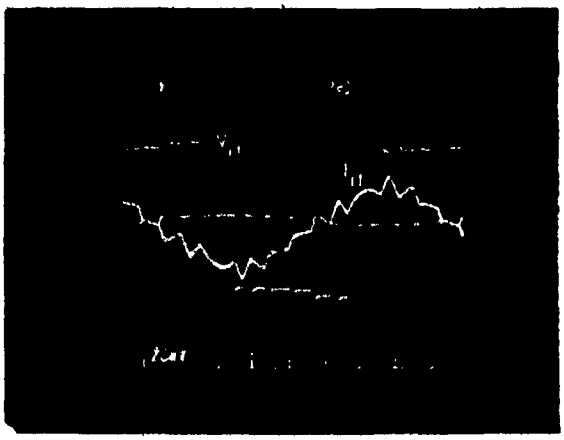
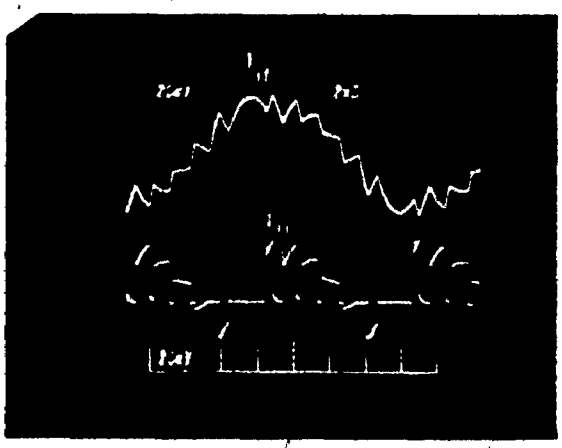


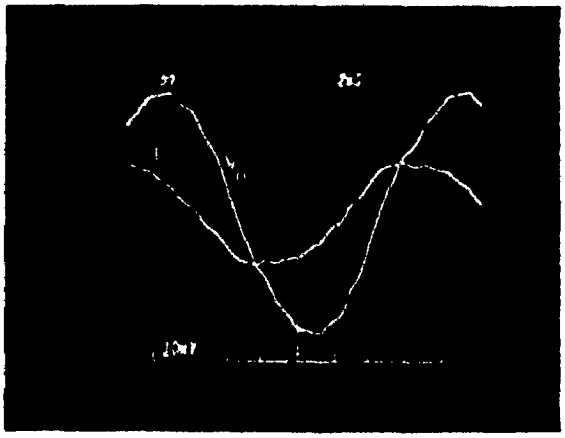
Fig. 2.10: Inverter Stage Control Circuit.



(a)



(b)



(c)

Fig. 2.11: Experimental results obtained with P_f=0.8 leading, M_f=1 and f_{nc}=7.

a) Voltage and current waveforms before output filtering, $V_{if}(\omega t)$ and $I_{if}(\omega t)$

b) Top: Current waveform before output filtering, $I_{if}(\omega t)$

Bottom: Inverter stage input current waveform, $I_{ij}(\omega t)$

c) Load voltage and current waveforms, $V_o(\omega t)$ and $I_o(\omega t)$

2.7 Conclusions

In this chapter, a novel two stage DC to AC inverter has been presented. The main inverter features included an HF link stage for transformer isolation and a regulated DC bus for the inverter stage. The proposed inverter system has been analyzed with various HF link configurations suitable for different output power levels. Theoretical and experimental results have shown that the proposed two stage inverter system yields high operating efficiency, programmable output frequency and high power density. Finally, when an extra power "leg" is inserted in the inverter stage, the proposed conversion scheme can be extended to three-phase output system.

CHAPTER 3

A CURRENT SOURCE DC TO AC INVERTER USING A DC TO DC CONVERTER AS HIGH FREQUENCY LINK

3.1 Introduction

Of the various converter topologies available for power inversion, Current Source Inverts (CSI) seem to offer certain advantages over the Voltage Source Inverters (VSI). The former inverters are characterized by a DC link input which behaves as a DC current source, through the action of a front end converter and a current regulation loop. The latter are characterized by a DC link input which behaves as a DC voltage source.

The principle of operation for VSI's is to supply power to the load by holding the output voltage fixed (in phase) relative to the VSI switching function. Consequently, the output current is forced to fluctuate back and forth from negative to positive. Since the semiconductor switches are unidirectional current devices, the VSI needs free wheeling diodes to operate under these conditions.

In the CSI, the output current is held fixed (in phase) relative to the CSI switching function. Consequently, the output voltage is forced to fluctuate from positive to negative. Thus, the need for free wheeling diodes is eliminated. However, the semiconductor switches must now be capable of blocking reverse voltage (If not a diode must be connected in series).

A schematic diagram of the proposed CSI system is shown in Fig. 3.1 which has the following advantages and disadvantages when compared to VSI (Fig. 2.2).

a) Advantages

i) Since the input DC current is controlled and limited, misfiring of the inverter switches or short circuit in the load is not catastrophic.

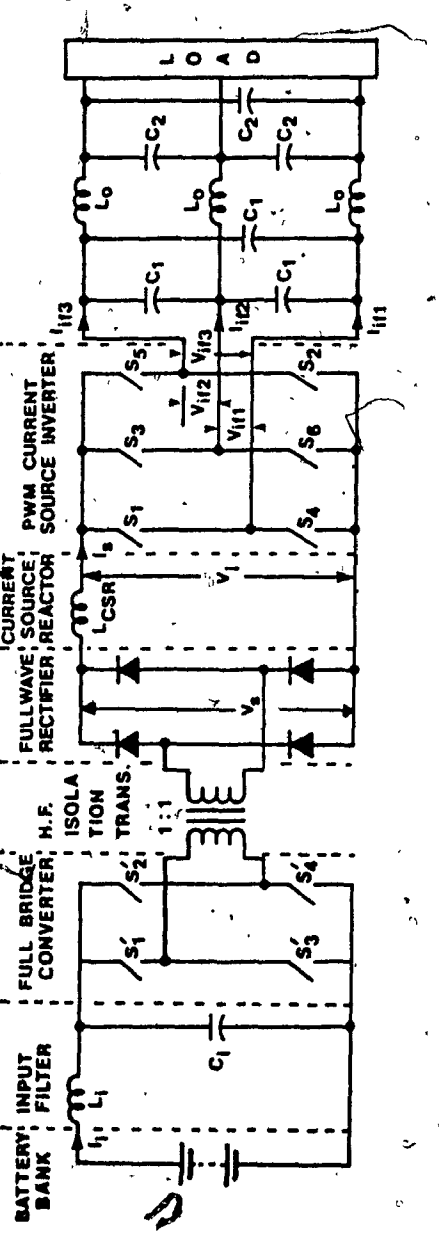


Fig. 3.1: Schematic diagram of the proposed Current Source Inverter.

ii) The negative link voltage capability of the CSI enables the inverter to handle reactive or regenerative loads without the use of free wheeling diodes, in contrast to the VSI which reverses its link current.

iii) The power semiconductor switches are subjected to lower peak current stresses because of the constant supply current.

vi) Since current spikes are filtered by the Current Source Reactor (CSR), the Electromagnetic Interference (EMI) of the CSI is reduced.

v) When thyristors are used to realize the CSI power switches, the commutation inductor is eliminated from the commutation circuit.

b) Disadvantages

i) Utilizes a relatively large DC filter reactor to exhibit current source characteristics. This is especially true for single-phase output inverter configuration and three-phase configuration under unbalanced load conditions. However, for three phase inverter configuration with balanced load (3-ϕ synchronous machines), the size of the filter inductor is considerably reduced.

ii) Exhibits slow current response because of the utilization of the large DC filter reactor.

3.2 System description

A brief description of the function performed and configuration for each system section of the proposed CSI system (Fig. 3.1) is as follows.

3.2.1 High Frequency link converter

The function of the high frequency (HF) link converter is twofold: First, it controls the current level of the current source in response to changes in load and/or changes in the DC voltage feeding the HF link. Second, it provides transformer isolation between the source and the load using a high frequency transformer. The choice of the power switches is based on the output power requirements and input DC bus.

3.2.2 Current Source Reactor (CSR)

The main function of the CSR is to convert the characteristics of the battery subsystem from voltage source into a current source type. Furthermore, the CSR limits the ripple factor of the DC link current to a prescribed level. The factors affecting the CSR inductance value are

a) the specified ripple factor for the DC link current,

b) the switching frequencies of the HF link and CSI stage, and

c) load conditions (balanced or unbalanced).

3.2.3 Current Source Inverter (CSI) Stage

The function of the CSI stage is to convert the DC current fed from CSR into single or three-phase AC balanced currents. Since current continuity cannot be violated there should be always conduction overlap between one of the upper three and one of the lower three switches. To minimize voltage stresses during current transfer from one phase to another the inverter is feeding the load through a capacitor input filter (Fig. 3.1). Also since a CSI does not require free wheeling diodes voltage stresses associated with diode recovery transients are not present.

Switching functions compatible with CSI can have fixed or variable switching patterns as shown in Figs. 3.2 and 3.3 respectively. A switching function with fixed pattern requires that the source current level is variable (to accomodate load changes), while in the case of variable pattern the current level can be either constant or variable. Fixed switching patterns have the advantages of:

a) Yielding maximum current utilization,

b) requiring the lowest switching frequencies and

c) having the simplest hardware implementation.

However, the inverter response to step changes in load is slower than that with the variable switching pattern. In the latter case the inverter can respond practically instantaneously by changing the degree of modulation (i.e. width of pulses) in the switching pattern. However, because variable switching patterns require significantly higher frequencies and yield poor source current utilization, they are considered only briefly in this chapter.

3.2.4 Output filter

The function of the load filter is to maintain the quality (i.e., harmonic distortion content) of the load voltage within specified limits. Since the filter is fed with a train of current pulses, its input component is a capacitor. This choice minimizes pattern distortion in line currents (by allowing sharp current transitions) and suppresses the voltage "spikes" typically associated with step current changes in CSI's.

Fig. 3.4(a) and (b) shows two filter configurations suitable for CSI applications. The obvious advantage of the first-order filter is circuit simplicity. Note, however, that a properly designed third-

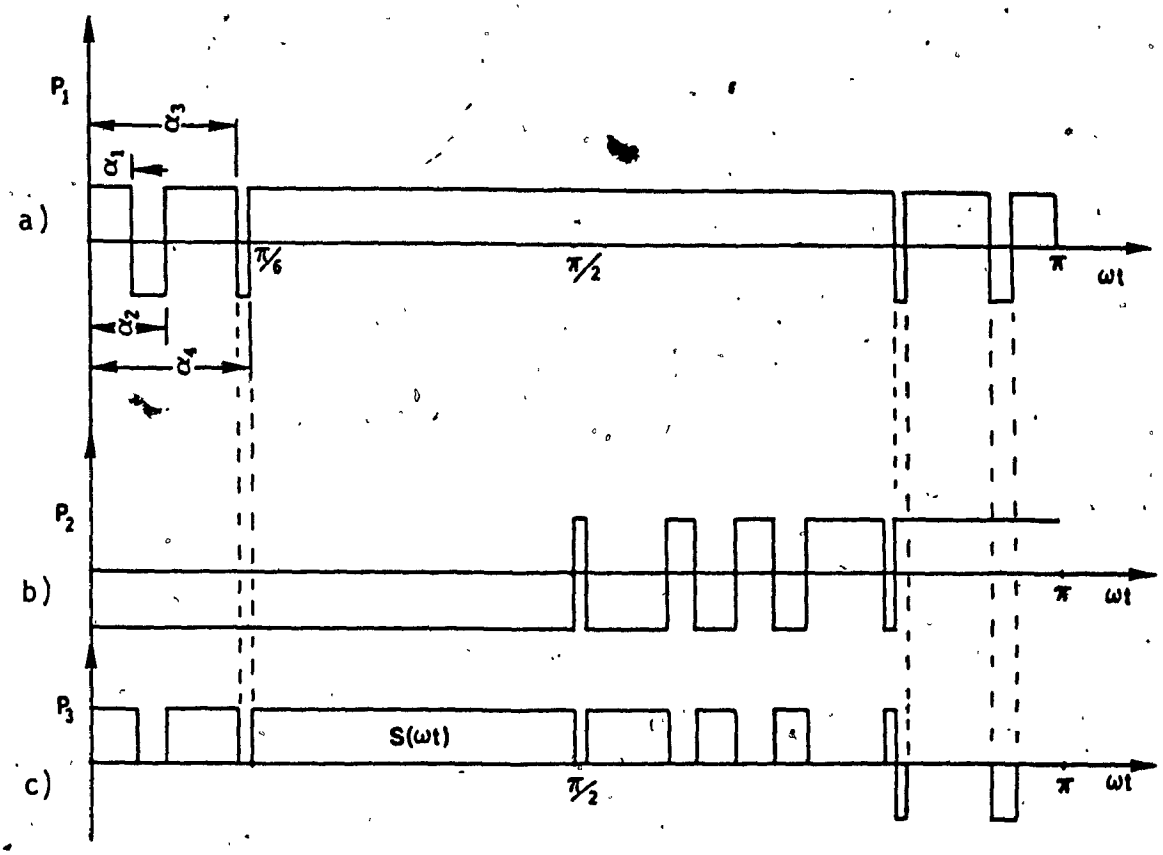


Fig. 3.2: Derivation of a fixed switching pattern for three-phase CS inverters.

a) Basic switching pattern, P_1

b) Pattern $P_2 = P_1 / \underline{120^\circ}$

c) Resulting switching pattern, P_3, for a single line current waveform.

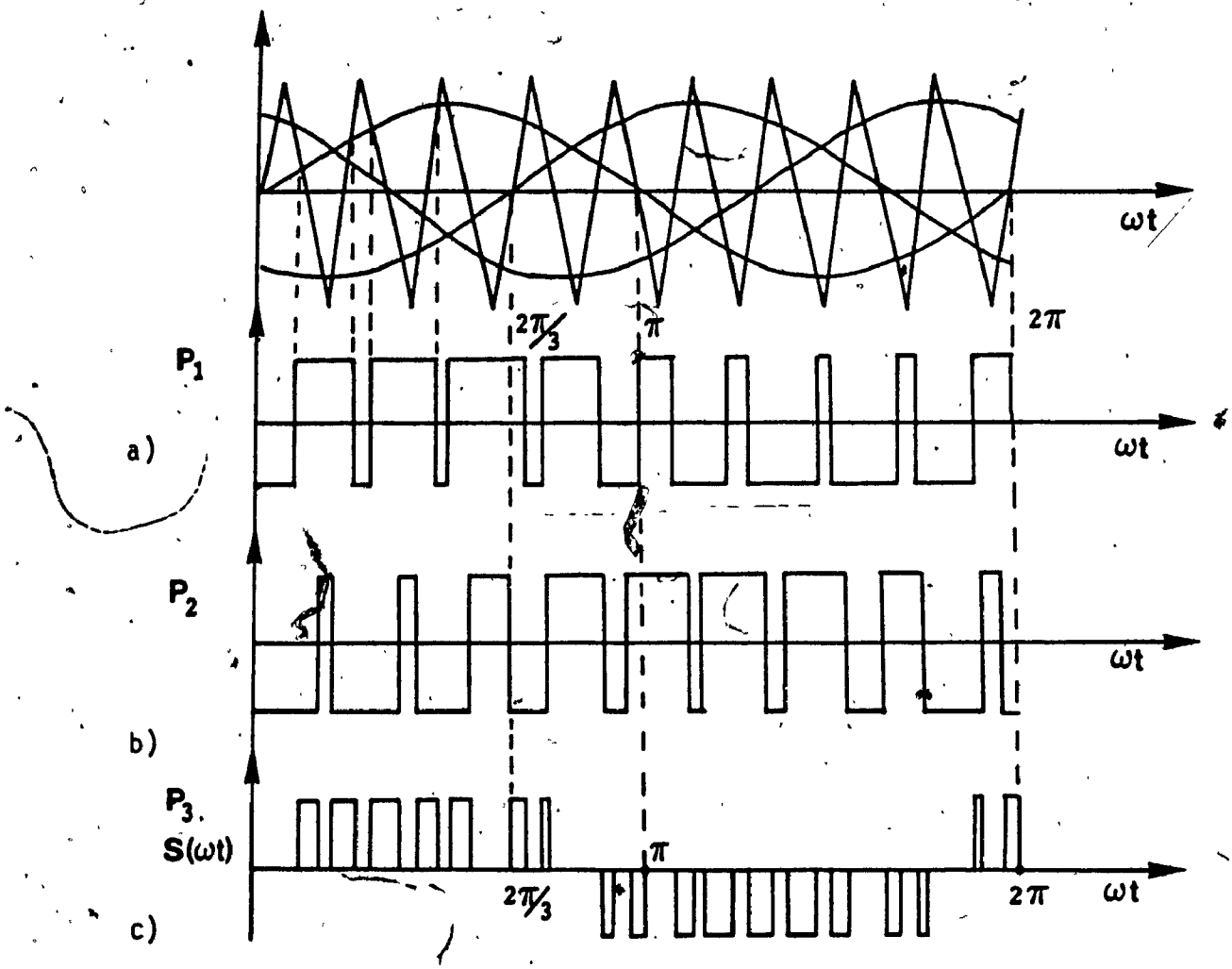


Fig. 3.3: Derivation of a variable switching pattern of three-phase CS inverters.

a) Basic switching pattern, P_1

b) Pattern $P_2 = P_1 / \underline{120°}$

c) Resulting switching pattern, P_3, for a single line current waveform.

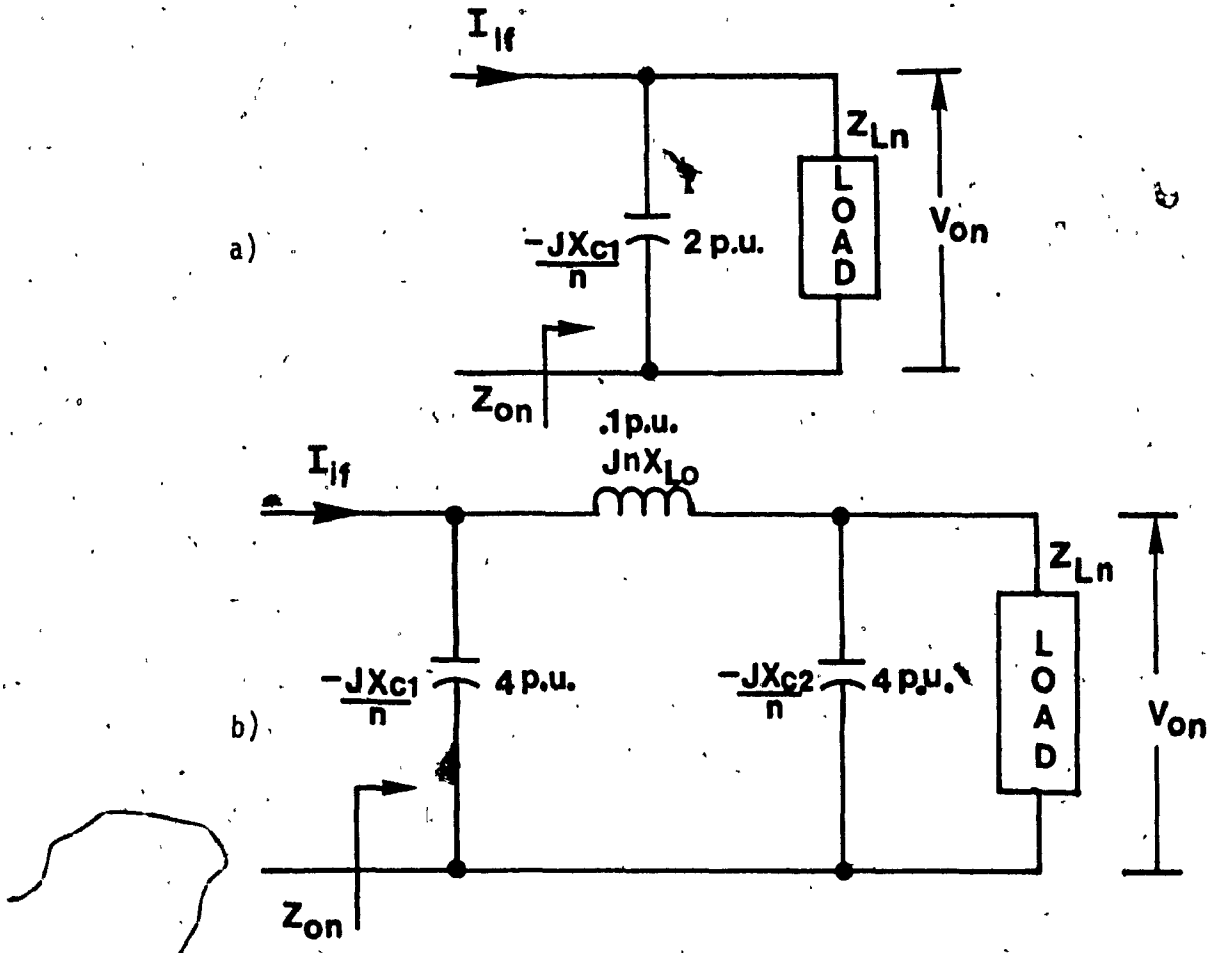


Fig. 3.4: Load filter configurations compatible with current source inverters.

a) First order
b) Third order

order filter yields better quality load voltage while drawing less reactive power.

3.2.5 Load conditions

In order to analyze under steady-stage conditions the proposed CSI inverter, the following per unit load conditions are assumed for the rated output voltage and rated output current.

$$I_o = 1 \text{ p.u. (Amps)}$$

$$V_{o(rms)} = 1 \text{ p.u. (Volts)}$$

Moreover, the load is assumed to be linear and balanced.

3.3 Synthesis of Switching Functions for CSI's

Switching functions that eliminate any number of low-order harmonics from CSI line currents are derived next. The method employed is based on the following three performance characteristics of ideal CSI's:

a) at any instant the line current is conducted by one upper and lower switch only;

b) at any instant the sum of all line currents is equal to zero; and

c) since a CSI is the dual of a VSI, switching patterns encountered in line-to-line voltages of VSI's are also applicable to line currents of CSI's.

3.3.1 Fixed Pattern Switching Functions

Since this topic has already received considerable attention [16], [22], it is appropriate to introduce a generalized method for deriving such function. The proposed method is as follows:

a) The harmonics to be eliminated or severely attenuated are specified first (fifth, seventh, eleventh, etc.).

b) The respective angles $\alpha_1, \alpha_2, \ldots, \alpha_n$ required are computed as outlined [16]. Note that the resulting switching pattern P_1, Fig. 3.2(a), cannot yet be employed on a three-phase CSI.

c) Let pattern $P_2 = P_1 \angle -120°$ as shown in Fig. 3.2(b), and pattern $P_3 = P_1 - P_2$ as shown in Fig. 3.2(c).

d) P_3 is the required switching pattern for the three-phase CSI line current.

The mathematical representation (i.e., switching function), $S(\omega t)$ for P_3 can be easily obtained through Fourier series analysis. The general form for $S(\omega t)$ is illustrated in eqn. (3.1).

3.3.2 Variable Pattern Switching Functions

Such functions can be obtained as follows:

a) The basic switching pattern P_1 is obtained as shown in Fig. 3.3(a). The number of low-order harmonics eliminated in this case depend on the ratio of the frequencies of the carrier to reference waveforms.

b) Let pattern $P_2 = P_1 \angle -120°$ (Fig. 3.3(b)) and pattern $P_3 = P_1 - P_2$. Then P_3 is the required variable switching pattern for the three-phase CSI line current, Fig. 3.3(c).

Finally, because of the disadvantages outlined in section 3.2.3, variable pattern switching functions are not examined any further.

3.4 System analysis

In this section the proposed inverter system is analyzed under steady state conditions. The derived expressions are subsequently used to obtain the information necessary for the safe system design.

3.4.1 Harmonic analysis

Inverter system analysis yields important and unexpected results if the CSI stage is modeled as a voltage harmonic generator to the current source and as a current harmonic generator to the output filter and load. This approach suggests that careful manipulation of the harmonics generated by the inverter can drastically reduce the KVA ratings (and sizes) of the CSR and of the load filter components. To illustrate how these benefits can be achieved, consider the fixed pattern switching function shown in Fig. 3.2(c) and its respective frequency spectrum shown in Table I. From these considerations it follows that if switching angles $\alpha_1, \alpha_2, \ldots, \alpha_n$ are chosen properly, a significant number of low-order harmonics (i.e., from third to $(\ell-1)$th) can be eliminated or severely attenuated. In such a case the respective

a) switching function $S(\omega t)$ can be mathematically described by

$$S(\omega t) = A_1 \cos(\omega_0 t) + \sum_{n=\ell}^{\infty} A_n \cos(n\omega_0 t) \qquad (3.1)$$

where:

A_n is the amplitude of the nth harmonic component of $S(\omega t)$,

ℓ is the order of the lowest (above fundamental) significant harmonic in the $S(\omega t)$ spectrum;

b) three inverter line currents I_{if1}, I_{if2}, I_{if3} are given by

TABLE I

FREQUENCY SPECTRUM OF THE IDEAL SWITCHING FUNCTION NORMALIZED TO THE MAXIMUM POSSIBLE FUNDAMENTAL ($\frac{4}{\pi}$)

SWITCHING ANGLES TO ELIMINATE THE THE 5TH, 7TH, AND 11TH HARMONIC COMPONENTS	HARMONIC ORDER n	AMPLITUDE (p.u.)
	1	0.925
	3	0.000
$\alpha_1 = 8.29°$	5	0.000
	7	0.000
	9	0.000
$\alpha_2 = 13.53°$	11	0.000
	13	0.050
$\alpha_3 = 27.46°$	15	0.000
	17	0.007
	19	0.135
$\alpha_4 = 30.00°$	21	0.000
	23	0.259
	25	0.188

$$I_{if1}(\omega t)=I_s(\omega t)\ S(\omega t) = A_1 I_s \cos(\omega_o t) + I_s \sum_{n=\ell}^{\infty} A_n \cos(n\omega_o t) \quad (3.2a)$$

$$I_{if2}(\omega t)=I_s(\omega t)\ S(\omega t + 120) \quad (3.2b)$$

$$I_{if3}(\omega t)=I_s(\omega t)\ S(\omega t - 120) \quad (3.2c)$$

where I_s is the CSI stage input current (or DC link current);

c) three-phase voltages V_{if1}, V_{if2}, V_{if3} are given by

$$V_{if1}(\omega t) = I_{if1}(\omega t)\ Z_o(\omega t) = A_1 I_s |Z_{o,1}| \cos(\omega_o t + \phi_1) + I_s \sum_{n=\ell}^{\infty} A_n |Z_{o,n}| \cos(n\omega_o t + \phi_n) \quad (3.3a)$$

$$V_{if2}(\omega t) = I_{if2}(\omega t)\ Z_o(\omega t) \quad (3.3b)$$

$$V_{if3}(\omega t) = I_{f3}(\omega t)\ Z_o(\omega t) \quad (3.3c)$$

where:

$Z_o(\omega t)$ is the input impedance of the output filter,

$|Z_{o,n}|$ is the magnitude of Z_o at the nth harmonic frequency

ϕ_n is the phase shift angle between respective voltage and current components introduced by $Z_{o,n}$,

d) inverter input (i.e., DC link) voltage, V_i, by

$$V_i(\omega t) = V_{if1}(\omega t)\ S(\omega t) + V_{if2}(\omega t)\ S(\omega t + 120) + V_{if3}\ S(\omega t - 120) \quad (3.4)$$

where:

$$V_{ifl}(\omega t)S(\omega t) = [A_1\cos(\omega_o t) + \sum_{n=\ell}^{\infty} A_n \cos A_n \cos(n\omega_o t)] \cdot$$

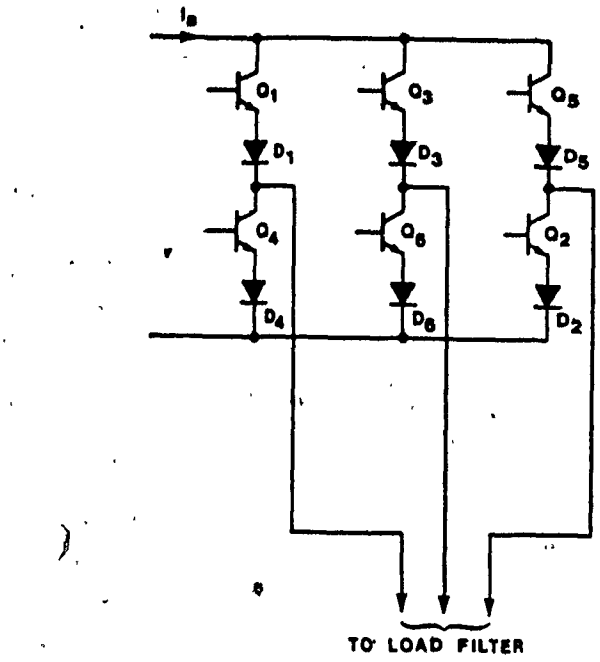
$$\cdot [A_1 I_s |Z_{o,1}| \cos(\omega_o t + \phi_1)$$

$$+ I_s \sum_{n=\ell}^{\infty} A_n |Z_{o,n}| \cos(n\omega_o t + \phi_n)] \qquad (3.5)$$

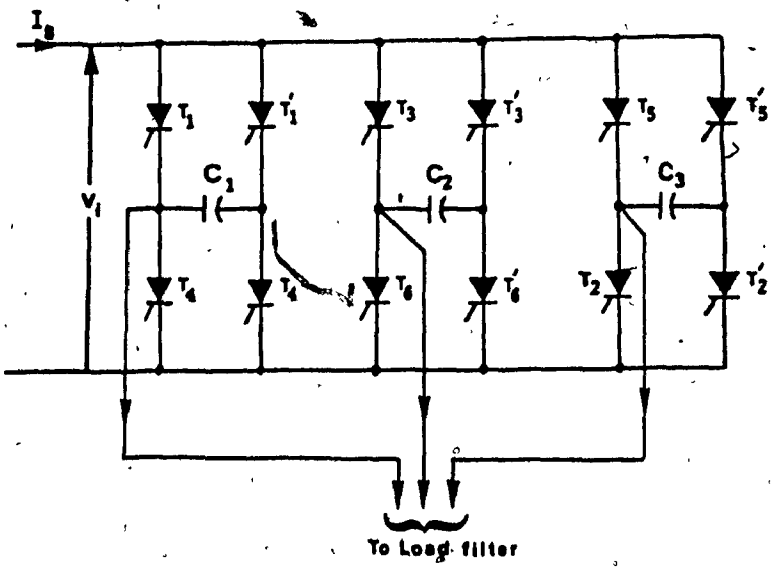
3.4.2 CSI stage analysis

A variety of semiconductor switches are available today that can be used to implement the CSI stage. Depending on the DC bus voltage and rated output power these devices can be transistors, GTOs, Assymetrical SCRs, or traditional thyristors. With devices that cannot support reverse voltage a suitable diode must be connected in series. Fig. 3.5 shows two possible realizations of the CSI stage.

With gate turn-off switches (Fig. 3.5(a)) the gating pulse pattern required to produce a giving switching function can be easily deduced from the line current waveforms. With auxiliary commutated switches however, the complexity of the gating pulse pattern may increase because of the introduction of commutation gating pulses. Moreover, the pattern is now determined not only by the switching function alone but also by the commutation scheme employed. As an example, consider the inverter configuration in Fig. 3.5(b). The configuration in Fig. 3.5(b) [23] employs a voltage commutation scheme that requires additional commutation thyristors and their associated commutation firing pulses. The current transfer from thyristor T_1 and T_3 (with T_1 and T_2 initially conducting) requires



(a)



(b)

Fig. 3.5: Two possible realizations of the CSI stage.

a) firing thyristors T_1', T_2' (this action turns off T_1, T_2 and several microseconds later reverses the voltage polarity of commutation capacitors C_1, C_3),

b) firing thyristors T_4', T_5' and several microseconds later restores the initial polarity across C_1, C_3; and

c) firing thyristors T_3, T_2.

The CSI stage configuration shown in Fig. 3.5(b) when compared to the conventional quasi-resonant CSI [24] has the following advantages and disadvantages.

a) Advantages

i) It does not require series diodes.

ii) It therefore yields lower conduction losses.

iii) It yields lower voltage stresses.

iv) The commutation process is load independent.

b) Disadvantages

i) It requires six extra thyristors.

ii) It requires more complex gating pattern.

The current ratings for the main CSI stage components (worst operating conditions) can be easily deduced from the CSI switching function $S(\omega t)$ in Fig. 3.2(c), and they are as follows:

$$\text{Average switch current} \quad I_{AS} \geq \frac{I_{s,o}}{3} \tag{3.6}$$

$$\text{RMS switch current} \quad I_{RS} \geq \frac{I_{s,o}}{\sqrt{3}} \tag{3.7}$$

$$\text{Peak switch current} \quad I_{PS} \geq 1.2\, I_{s,o} \tag{3.8}$$

where:

$I_{s,b}$ is the maximum DC component of the inverter stage input current. Similarly, with sinusoidal load voltage, the respective voltage ratings are,

Peak switch forward blocking voltage $\hat{V}_{FB} = V_{im}$ (3.9)

Peak switch reverse blocking voltage $\hat{V}_{RB} = V_{im}$ (3.10)

where

V_{im} is the maximum expected value of the CSI stage input voltage.

These ratings become more relevant if one selects:

a) the rms value of the fundamental component of load (line to neutral) voltage 1 p.u. base voltage, and

b) the rms value of the fundamental component of the load current as 1 p.u. base current.

In such a case it can be easily shown (Table III) that with load power factor (P_f) varying from 0.8 leading to 0.8 lagging and for the filter component values shown in Fig. 3.4(a) and (b)

$I_{s,o} = 1.89$ p.u. (3.11)

$V_{im} = 3.20$ p.u. (3.12)

3.4.3 Output filter analysis

The two filter configurations to be analyzed are shown in Fig. 3.4 (a) and (b). The component values (Fig. 3.4) have been chosen rather arbitrarily since filter optimization is outside the scope of this thesis. However, with these component values, it is noted that

a) under no-load conditions both filters "draw" approximately 0.5 p.u. input current, and

b) both filters draw approximately the same (i.e., 0.5 p.u.) reactive power.

The analysis consists of establishing the output voltage to input current transfer characteristics H(nωt) for each filter configuration, with worst-load conditions (i.e., P_f 0.8 leading). By inspection, the two transfer functions can be expressed as,

$$H^a(n\omega t) = \frac{V_{o,n}}{I_{if,n}} = \frac{X_{c1}Z_{L,n}}{X_{c1}+JnZ_{L,n}} \tag{3.13}$$

$$H^b(n\omega t) = \frac{X_{c1}X_{c2}Z_{L,n}-n^2X_{c1}X_{Lo}Z_{L,n}+JnX_{c1}X_{c2}X_{Lc}}{X_{c1}X_{c2}-n^2X_{c2}X_{Lo}+JnX_{c1}Z_{L,n}+JnX_{c2}Z_{L,n}-Jn^3X_{Lc}Z_{L,n}} \tag{3.14}$$

where:

$H(n\omega t)$ is the value of the load filter transfer function at the nth harmonic frequency,

$V_{o,n}$ is the value of the nth load voltage harmonic component,

$I_{if,n}$ is the value of the nth harmonic component of the load filter input current.

H(nωt) plots for the two filter configurations (Fig. 3.4(a) and (b)) with 0.8 load P_f leading are shown in Fig. 3.6(a) and (b). As expected, the third-order filter has much sharper cutoff characteristics around the dominant line current harmonic frequencies (e.g., nineteenth, twenty-third, twenty-fifth) than the first-order one. Consequently, the Total Harmonic Distortion (THD) values of the load voltage, with the switching pattern shown in Fig. 3.2(c) are under worst-load conditions (i.e. P_f 0.8 leading) 7.1% and 2.5% respectively (TABLE III).

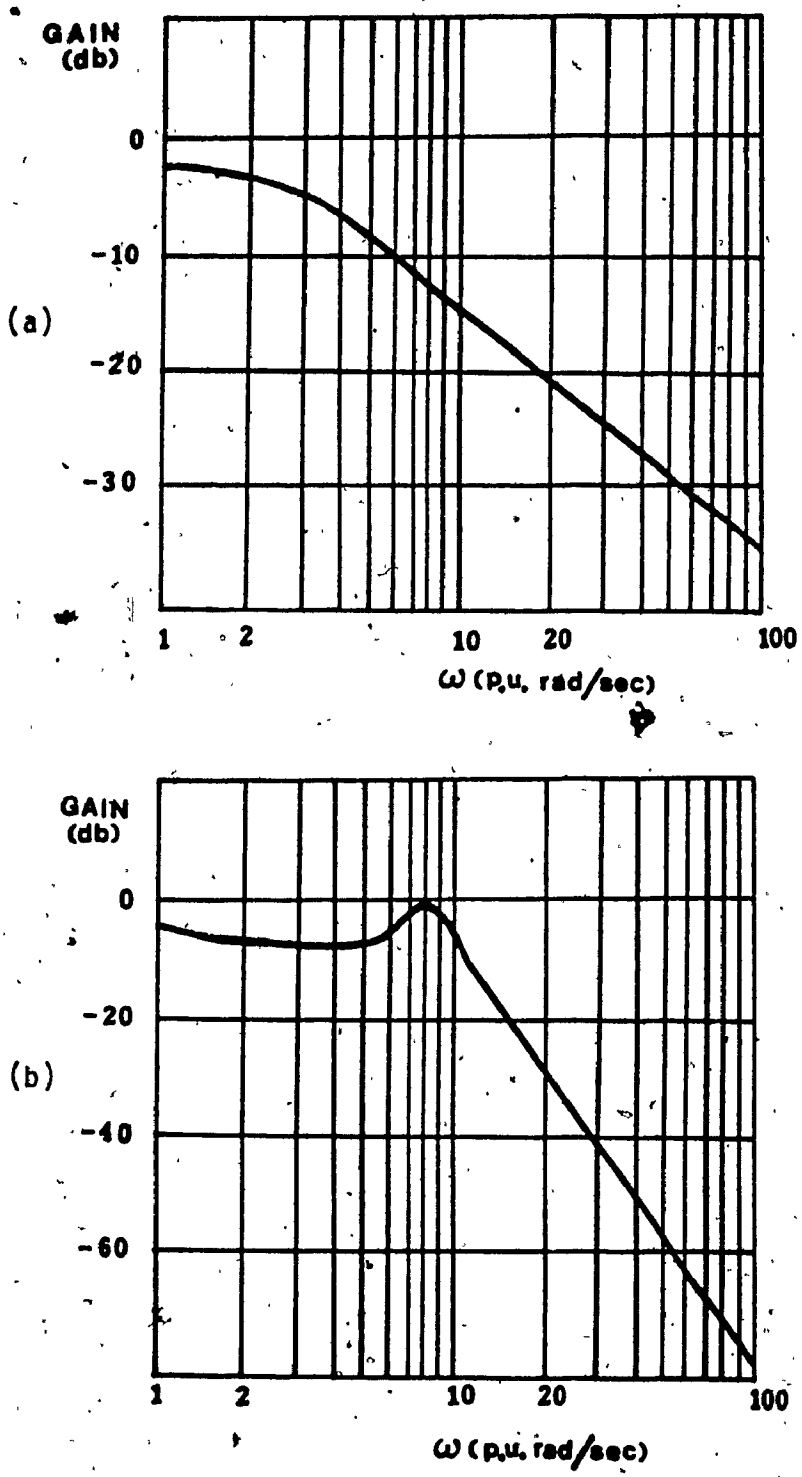


Fig. 3.6: Amplitude response of output filters with load power factor 0.8 leading.

a) For filter shown in Fig. 3.4(a)
b) For filter shown in Fig. 3.4(b)

3.4.4 CSR analysis

As mentioned earlier (section 3.2.2), the factors affecting the value of CSR inductance include

a) the specified ripple for the DC link current ΔI_s, and

b) the switching frequencies of the HF link and CSI stage.

Moreover, as shown in section 3.6, Table III, the effect of ΔI_s on the ripple of the load voltage is negligible if

$$\Delta I_s \simeq \frac{I_{s,d}}{I_{s,o}} \leq 0.2 \qquad (3.15)$$

where:

$I_{s,d}$ is the amplitude of the dominant harmonic component of the DC link current,

$I_{s,o}$ is the DC component of the DC link current.

Also with the switching frequency ω_ℓ of the HF link chosen lower than the frequency of the lowest significant harmonic of $S(\omega t)$ (of CSI), $I_{s,d}$ is given by

$$I_{s,d} \simeq \frac{V_{sm}}{\omega_\ell L_{CSR}} \qquad (3.16)$$

where:

V_{sm} is the maximum amplitude of the fundamental component of the HF link output voltage,

L_{CSR} is the inductance of the CSR,

ω_ℓ is the HF link switching frequency.

Furthermore, since V_{sm} occurs when the HF link is operating with 50% duty cycle,

$$V_{sm} = \left(\frac{4}{\pi}\right)\left(\frac{E_{max}}{2}\right) = \frac{2E_{max}}{\pi} \qquad (3.17)$$

where:

E_{max} is the maximum expected value of the DC bus

The maximum expected value of E_{max} with worst-load conditions (i.e., P_f 0.8 leading) is given by (TABLE III),

$$E_{max} = 2.21 \text{ p.u.} \qquad (3.18)$$

Therefore, from exps. (3.17) and (3.18)

$$V_{sm} = \frac{2}{\pi} \times 2.21 = 1.4 \text{ p.u.} \qquad (3.19)$$

$$L_{CSR} = \frac{V_{sm}}{\frac{\omega_\ell}{\omega_o} I_{s,d}} = \frac{1.4}{\omega_{n\ell} I_{s,d}} \text{ p.u.} \qquad (3.20)$$

where:

ω_o is the operating frequency taken as 1 p.u. base frequency

Also from exps. (3.15) and (3.11),

$$I_{s,d} = 0.2\ I_{s,o} = 0.378 \text{ p.u.} \qquad (3.21)$$

therefore, using eqn. (3.20)

$$L_{CSR} = \frac{1.4}{0.378\ \omega_{n\ell}} = \frac{3.7}{\omega_{n\ell}} \text{ p.u.} \qquad (3.22)$$

As expected, L_{CSR} is inversely proportional to the normalized HF link switching frequency $\omega_{n\ell}$.

Furthermore, current and voltage ratings for L_{CSR} are

Average current ratings $I_{s,o}$ = 1.89 p.u. (3.23)

RMS current rating $(I_{s,o}^2 + (\Delta I_s)^2)^{1/2} \simeq 1.89$ p.u. (3.24)

Peak voltage rating V_{im} = 1.4 p.u. (3.25)

Finally, by neglecting the effects of the CSI stage input ripple voltage, the ripple VA rating, for CSR is found to be

$$VA_{CSR} \simeq (\frac{E_{max}}{2})(I_{s,d}) = (\frac{2.21}{2})(0.378) = 0.418 \text{ p.u.} \quad (3.26)$$

Example: If one considers a three-phase 60Hz 100-KVA system at 115 V_{rms} L-N load voltage, then according to previous discussion,

1 p.u. power = 33.33 KVA (3.27)

1 p.u. volts = 115 V (3.28)

1 p.u. current = $\frac{33.33 \times 10^3}{115}$ = 290 A (3.29)

1 p.u. impedance = $\frac{115}{290}$ = 0.4Ω (3.30)

1 p.u. inductance = $\frac{0.4}{377}$ = 1.06 mH (3.31)

whence, from exps. (3.26) and (3.27)

$$VA_{CSR} = (0.481)(33.33) = 14 \text{ KVA} \quad (3.32)$$

Moreover, assuming a HF link switching frequency of 720 HZ,

$$\omega_{n\ell} = \frac{720}{60} = 12 \quad (3.33)$$

Therefore, from exps. (3.22), (3.25) and (3.33),

$$L_{CSR} = (1.06)(\frac{3.7}{12}) \simeq 0.326 \text{ mH} \quad (3.34)$$

Finally, from exps. (3.23) - (3.25) and (3.29),

Average L_{CSR} current $I_{s,o}$ = (1.89)(290) = 548 A (3.35)

RMS L_{CSR} current ≃ (1.89)(290) = 548 A (3.36)

Peak L_{CSR} voltage = (5.44)(115) = 622 V (3.37)

3.4.5 HF link analysis

Depending on the input DC voltage level, E, rated output power, and chosen HF link switching frequency, the HF link can be implemented by using bipolar transistors, GTO's, or fast turn-off thyristors. Fig. 3.7(a) and (b) shows two possible realizations of the HF link.

Regarding Fig. 3.7(a) when transistors Q_2' and Q_3' are conducting current is being built up in the CSR at a rate determined by the difference between the DC input voltage E, and the instantaneous value of voltage reflected by the CSI stage. When the current has reached the desired value as determined by an appropriate control circuit (current limit) Q_2' or Q_3' is turned off to reduce the applied DC voltage to zero and thereby allow current to free wheel through the bridge rectifier. In this case Q_2' is turned off, thus forcing the current to transfer to Q_4's feedback diode. Under this condition, the current maintained by the CSR attempts to circulate through all four rectifier diodes. When it is desired to build current up in the CSR again Q_3' is turn off Q_1' on, which will once again effectively apply DC voltage, E, to CSR and to the load. Fig. 3.8 shows the typical waveforms of the HF link presented in Fig. 3.7(a). Regarding Fig. 3.8 the ratings for the HF link components are as follows:

$$\text{Average HF link switch current } I_{s,o} = 1.89 \text{ p.u.} \tag{3.38}$$

$$\text{Peak HF link switch current } I_{s,o}(1+0.2)=2.27 \text{ p.u.} \tag{3.39}$$

$$\text{RMS HF link switch current } [I_{s,o}^2+(\Delta I_s)^2]^{1/2}=1.89 \text{ p.u.} \tag{3.40}$$

$$\text{Peak HF link switch voltage } E_{max}=2.21 \text{ p.u.} \tag{3.41}$$

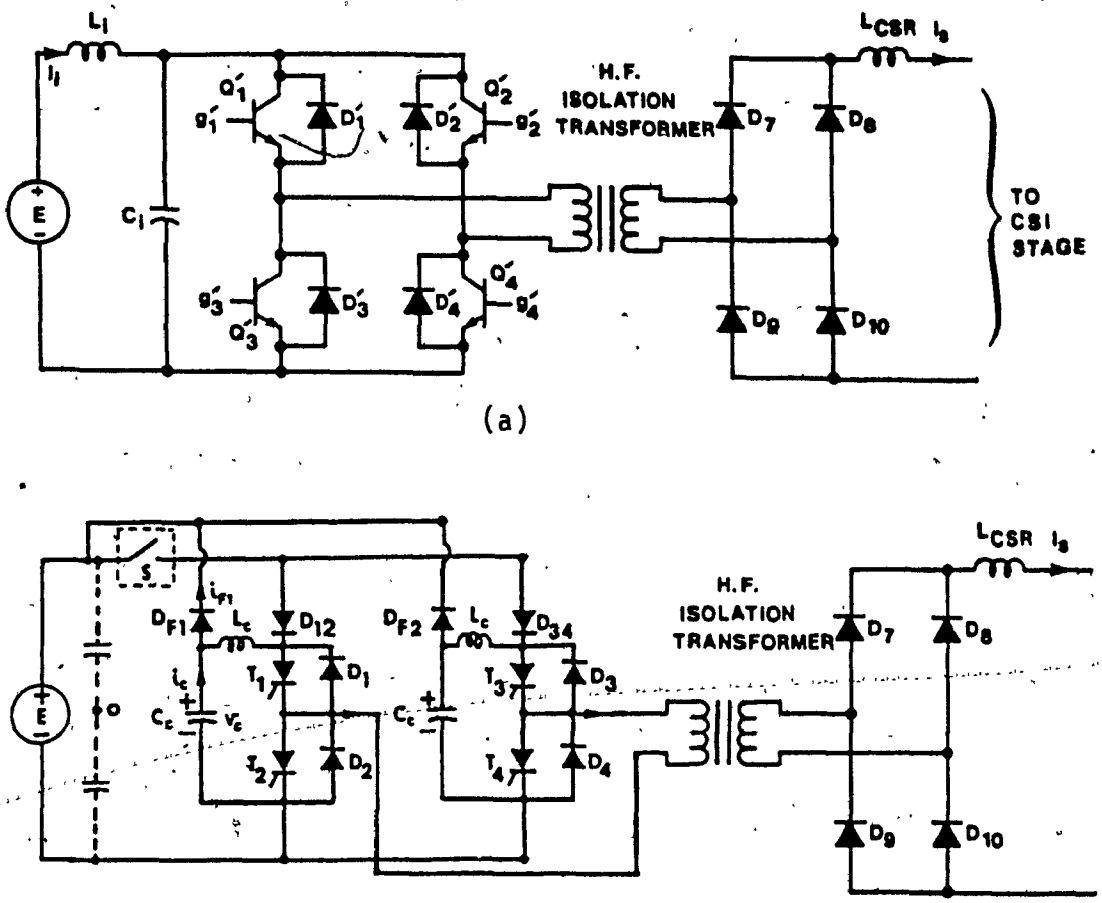


Fig. 3.7: Two possible realizations of the HF link stage.

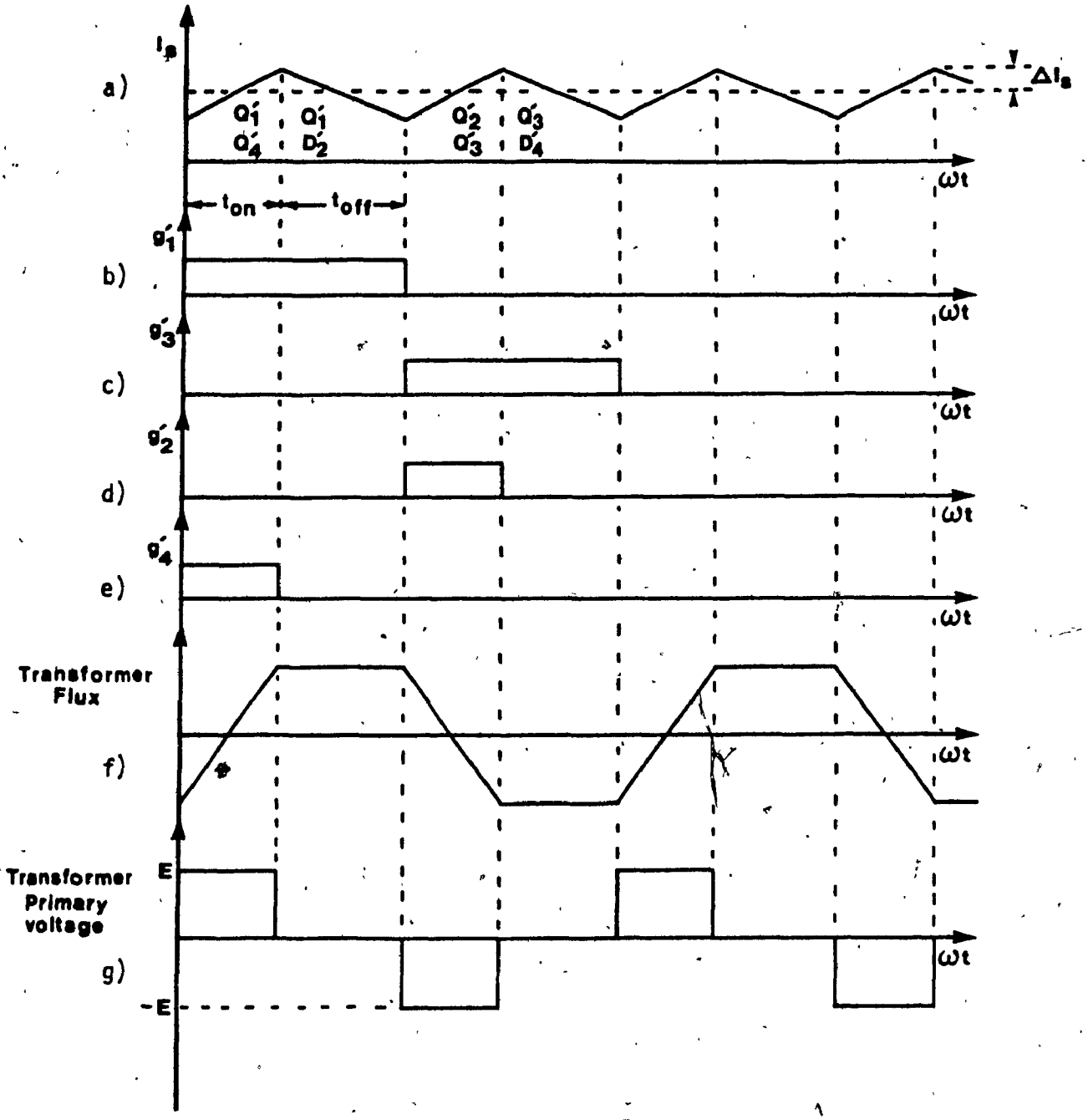


Fig. 3.8: Typical waveforms of the HF link stage.

(a) HF link output current, $I_s(\omega t)$

(b)-(e) HF link gating signals

(f) Isolation transformer flux

(g) Isolation transformer primary voltage

The proposed thyristorized realization of the HF link, which is shown in Fig. 3.7(b), is analyzed in appendix B.

3.5 Computer-aided harmonic analysis

In the earlier sections it has been claimed that

1) properly selected pulse width modulation (PWM) switching functions, such as $S(\omega t)$ (section 3.4), can minimize input and output filtering requirements;
2) if HF link switching frequency, ω_ℓ, is chosen less than the frequency of the lowest significant harmonic of $S(\omega t)$, then, as shown in eqn. (3.16), the main-source for the DC link ripple current ΔI_s is V_{sm} (i.e., fundamental component of the HF link output voltage); and
3) if ΔI_s is kept below 20% (see eqn. (3.15)) the effects of ΔI_s on the ripple of the load voltage are negligible.

To validate these statements a computer-aided analysis based on eqns. (3.1) - (3.3) has been performed (Appendix A) with the following input data,

a) The CSI stage switching function, $S(\omega t)$, is as shown in Fig. 3.2(c), with switching angles as specified in Table I.
b) The normalized HF link switching frequency, $\omega_{n\ell}$, is taken 18.
c) The load filter assumes the configurations and component values in Fig. 3.4(a) and (b).
d) The load P_f varies from 0.8 leading to 0.8 lagging.
e) The fundamental component of the line-to-neutral voltage (rms) at the inverter output terminals is taken equal to 1 p.u. voltage base.

f) The fundamental component of the inverter load current is taken as 1 p.u. current base.

g) The ripple in the DC link current may be increased up to 20%.

The results of the computer-aided analysis have been tabulated as follows. Table II contains the spectra of voltage and current waveforms, at key system points, obtained with ripple-free DC link current, I_s, and $P_f = 1$. In particular columns 1, 3 and 5 depict the order of individual harmonics. Columns 2, 4 and 6 depict the spectra of CSI stage line current, CSI stage load voltage and CSI stage input voltage, respectively.

From the contents of Table II it is evident that a properly selected $S(\omega t)$ function significantly improves the harmonic spectra of the CSI stage input and output voltages (by eliminating or severely attenuating low-order harmonics). This conclusively satisfies statement (1) regarding input and output filtering requirements. It is also evident that the amplitudes of dominant CSI stage input voltage harmonics are below 0.33 p.u. (column 6, for n=18,24,30). From eqn. (3.17) and (3.18), however, V_{sm}=1.4 p.u. Therefore statement (2) regarding the dominant source (e.g., V_{sm}) of the DC link ripple current is also true.

Also, statement (3) regarding the effects of the DC link ripple current, ΔI_s, on load voltage ripple can be shown to be true by examining respective current and voltage THD values (with ripple-free and non-ripple-free DC link current), depicted in Table III. Specifically, it is shown that 20% ΔI_s produces, under worst-load operating conditions, a 20% rise in the THD value of the load voltage (columns 3,6).

Moreover, table III, illustrates some differences in the performance of first and third-order load filters. As expected, the third-order filter provides substantially better quality load voltage (i.e., lower THD values) for the same operating conditions.

3.6 Experimental results

To demonstrate the feasibility of the proposed CSI system and verify selected predicted results an experimental 2-KVA unit has been implemented. Results obtained with this breadboard unit are depicted in Figs. 3.9 - 3.11.

Fig. 3.9(a) and (b) illustrate the CSI stage line current and line-to-neutral voltage waveform with their respective spectra. These experimental results were obtained with ripple-free DC link current, first-order filter (Fig. 3.4(a)) and unity load power factor. Comparison between predicted (Table II columns 2 and 4) and experimental results shows that they are in close agreement.

The CSI stage input voltage and its spectrum obtained with ripple-free DC link current, first-order filter and unity power factor are shown in Fig. 10. It can be seen that the results of Fig. 3.10 agree with the predicted results of Table II column 6.

The effects of the 20% ripple current on the frequency spectra of (a) DC link current, (b) CSI stage line current, and (c) load voltage are illustrated in Figs. 3.11 (a), (b) and (c) respectively. Fig. 3.11(a) illustrates, as predicted in eqn. (3.16), that the main source of the DC link ripple current is the fundamental harmonic, V_{sm}, generated at

TABLE I-I

PREDICTED SPECTRA OF VOLTAGE AND CURRENT WAVEFORMS
OBTAINED WITH RIPPLE FREE DC LINC CURRENT (1.554 p.u.),
P.F. = 1, AND FIRST ORDER FILTER

RMS CSI LINE CURRENT HARMONICS		RMS CSI OUTPUT PHASE VOLTAGE HARMONICS		RMS INPUT VOLTAGE HARMONICS	
HARMONIC ORDER n	AMPLITUDE (p.u.)	HARMONIC ORDER n	AMPLITUDE (p.u.)	HARMONIC ORDER n	AMPLITUDE (p.u.)
1	1.12	1	1.00	0	1.93
3	0.00	3	0.00	6	0.01
5	0.00	5	0.00	12	0.09
7	0.00	7	0.00	18	0.23
9	0.00	9	0.00	24	0.33
11	0.00	11	0.00	30	0.11
13	0.06	13	0.01	36	0.04
15	0.00	15	0.00	42	0.15
77	0.01	17	0.00	48	0.09
19	0.16	19	0.02	54	0.02
21	0.00	21	0.00	60	0.14
23	0.31	23	0.03	66	0.06
25	0.23	25	0.02	72	0.12
1	2	3	4	5	6

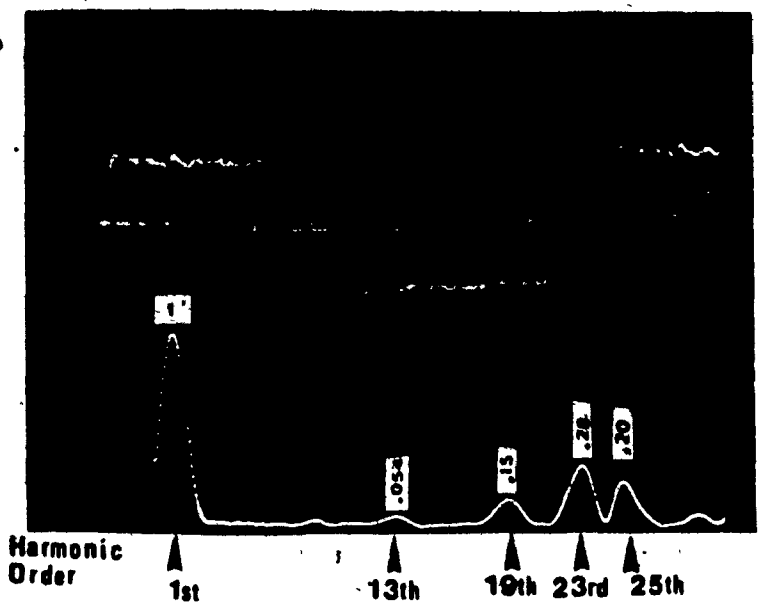
TABLE III

PREDICTED CHARACTERISTICS FOR CSI

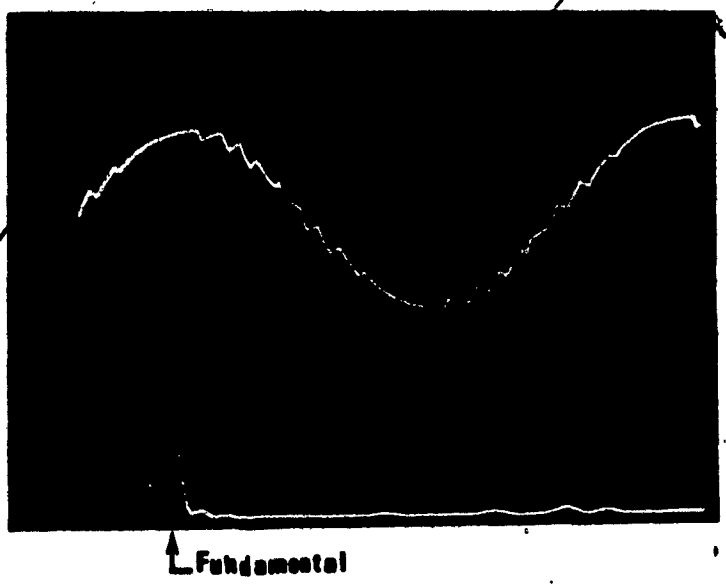
LOAD VOLTAGE (V_{on}), LINE CURRENT (I_{il}), INPUT VOLTAGE (V_i) AND INPUT CURRENT (I_s)

	1ST ORDER FILTER (Fig. 6(a))						3RD ORDER FILTER (Fig. 6(b))					
	RIPPLE - FREE			20% RIPPLE, ω_{nl}=18			RIPPLE - FREE			20% RIPPLE, ω_{nl}=18		
	p.f.=0.8 LAGGING	p.f.=1	p.f.=0.8 LEADING	p.f.=0.8 LAGGING	p.f.=1	p.f.=0.8 LEADING	p.f.=0.8 LAGGING	p.f.=1	p.f.=0.8 LEADING	p.f.=0.8 LAGGING	p.f.=1	p.f.=0.8 LEADING
LOAD VOLTAGE THD	3%	4%	5%	4.3%	5.9%	7.1%	0.8%	1%	1.2%	1.6%	2.1%	2.5%
LINE CURRENT THD	50%	50%	50%	62.8%	60.3%	59.3%	50%	50%	50%	61.4%	60.3%	59%
INPUT VOLTAGE THD	33.1%	38%	59.2%	33.1%	38.6%	60.9%	33.3%	37.4%	57.3%	33.4%	38.9%	61.3%
MAXIMUM INPUT DC VOLTAGE E_m(p.u.)	2.14	1.93	1.27	2.14	1.93	1.28	2.21	1.97	1.30	2.21	1.97	1.30
DC COMPONENT OF DC LINK CURRENT $I_{i,o}$	1.12	1.55	1.89	1.08	1.50	1.83	1.09	1.52	1.85	1.06	1.47	1.79
MAXIMUM INVERTER INPUT VOLTAGE V_{im}(p.u.)	3.07	2.93	2.29	3.08	2.91	2.28	3.17	2.94	2.25	3.20	2.91	2.30
[illegible]	1	2	3	4	5	6	7	8	9	10	11	12

NOTE: THD = $\frac{1}{\text{fundamental}} (\sum (\text{nth harmonic component})^2)^{1/2}$



(a)



(b)

Fig. 3.9: Experimental CSI results obtained with ripple free DC link current, first order filter and unity load power factor.

a) CSI line current and its spectrum (7.0 Amps zero to peak current)

b) CSI line to neutral voltage and its spectrum (T15$\sqrt{2}$ volts zero to peak voltage)

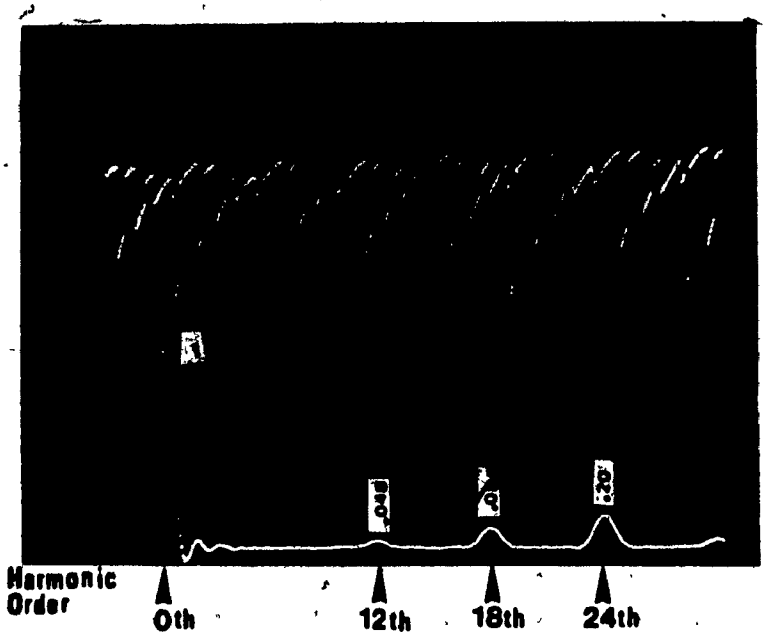
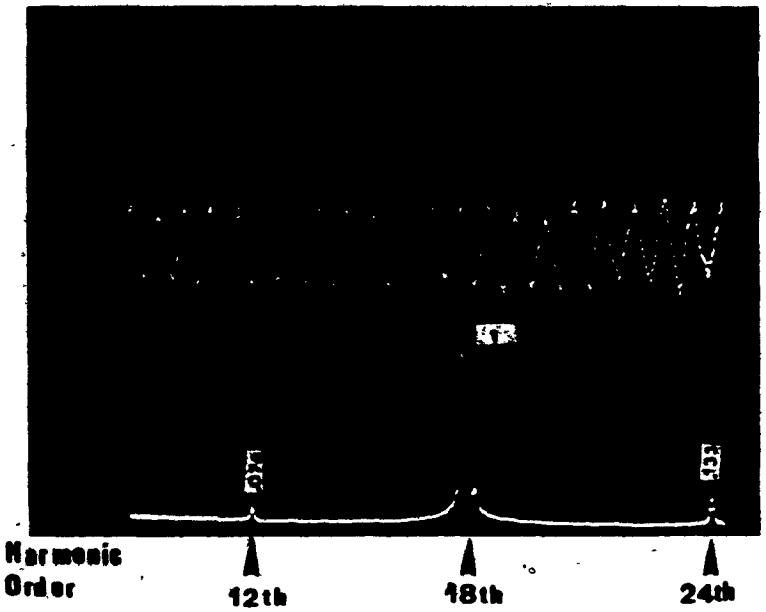
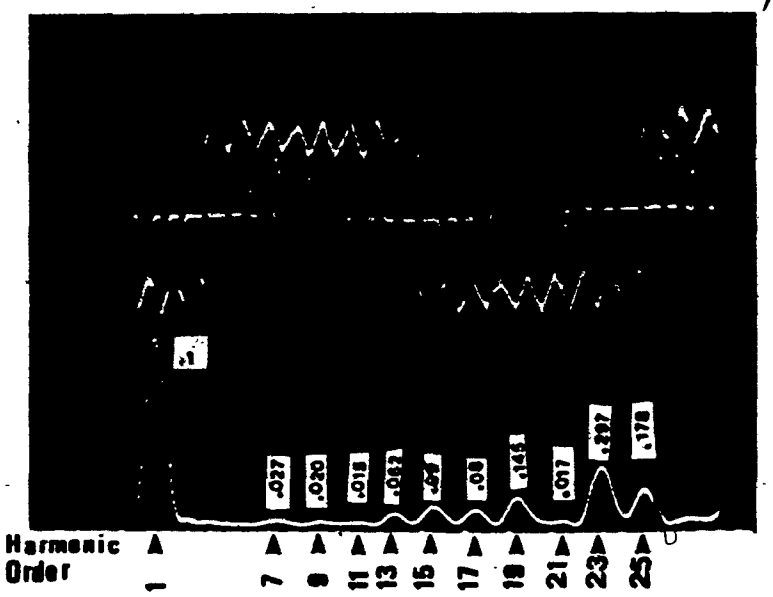


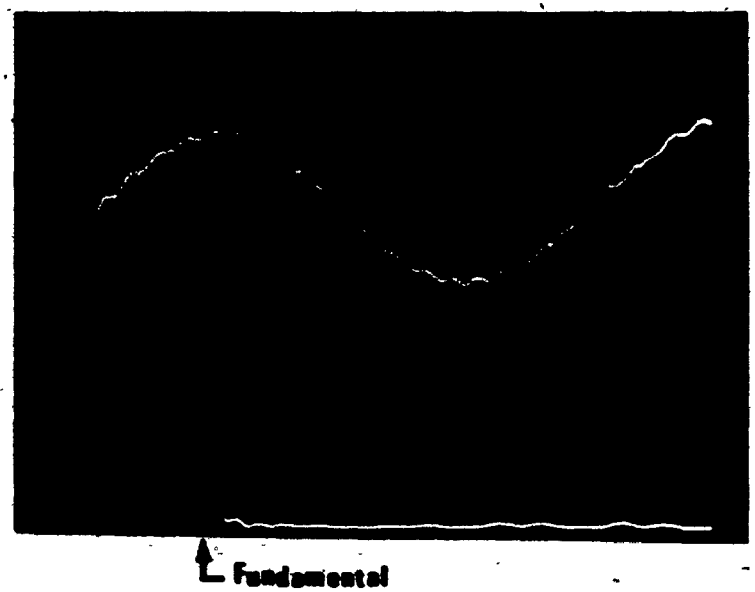
Fig. 3.10: Experimental CSI stage input voltage and its spectrum obtained with ripple free DC link current, first order filter and unity load power factor.



(a)



(b)



(c)

Fig. 3.11: Experimental results obtained with DC link ripple current ΔI_s=20%, first order filter and unity load power factor.

a) DC link ripple current and its spectrum

b) CSI line current and its spectrum (7.0 Amps zero to peak current)

c) CSI line to neutral voltage and its spectrum (115 $\sqrt{2}$ zero to peak voltage)

the output of the HF link. Furthermore, Figs. 3.11(b) and (c) illustrate that the contribution of the 20% ripple current to the distortion of the CSI stage link current and load voltage is minimal.

3.7 Conclusions

In this chapter a current source DC to AC power conversion scheme was presented for three-phase balanced loads. It has been shown that properly selected CSI switching functions can minimize the input and output requirements (i.e. current source and load filter) of the system. The resulting power conversion scheme combines the high reliability of a current source fed system with the fast response of voltage fed system.

CHAPTER 4

AN AC TO DC CONVERTER USING A CYCLOCONVERTER AS HIGH FREQUENCY LINK

4.1 Introduction

Several aerospace and military specifications for off-line AC to DC power conversion schemes require the following specifications [25]:

i) Transformer isolation between source and load,

ii) Controlled input power factor,

iii) The amplitudes of the AC source line current harmonic components to be limited to 3% of the fundamental component for power conditioning, and

iv) Minimum weight, size and cost.

Limiting the AC source line current harmonic components to 3% of the fundamental component results in an input voltage Total Harmonic Distortion (THD, see appendix C) within 5%. If the THD is more than 5% it can cause problems in poorly designed electronic equipment, increase power losses in motors and other magnetic devices, decrease the input power factor, and generate Electromagnetic Interference (EMI).

To satisfy the above mentioned specifications, in the past few years the conventional Switch-Mode Rectifier (SMR) and the Delco approach rectifier schemes were proposed [26], [27], [28], [29]. A schematic diagram of these converters is shown in Fig. 4.1(a) and (b) respectively. These two schemes exhibit the following advantages and disadvantages when compared to the conventional phase control AC to DC power conversion scheme.

a) Advantages

i) The employment of a high frequency DC to DC link results in substantial cost, size and weight reduction for the isolation transformer.

ii) Due to the high switching frequency the size of the output filter is reduced considerably.

iii) The Delco approach offers some improvement regarding the input power factor.

Disadvantages of

a) conventional Switch-Mode Rectifier (Fig. 4.1(a)).

i) It utilizes two rectification stages.

ii) It utilizes an additional filter after the input rectifier stage.

iii) It exhibits low efficiency because of the employment of two power conversion stages.

iv) It exhibits poor input power factor.

b) The Delco approach rectifier (Fig. 4.1(b)).

i) Since it consists of three individual DC to DC converters it utilizes a complex control system.

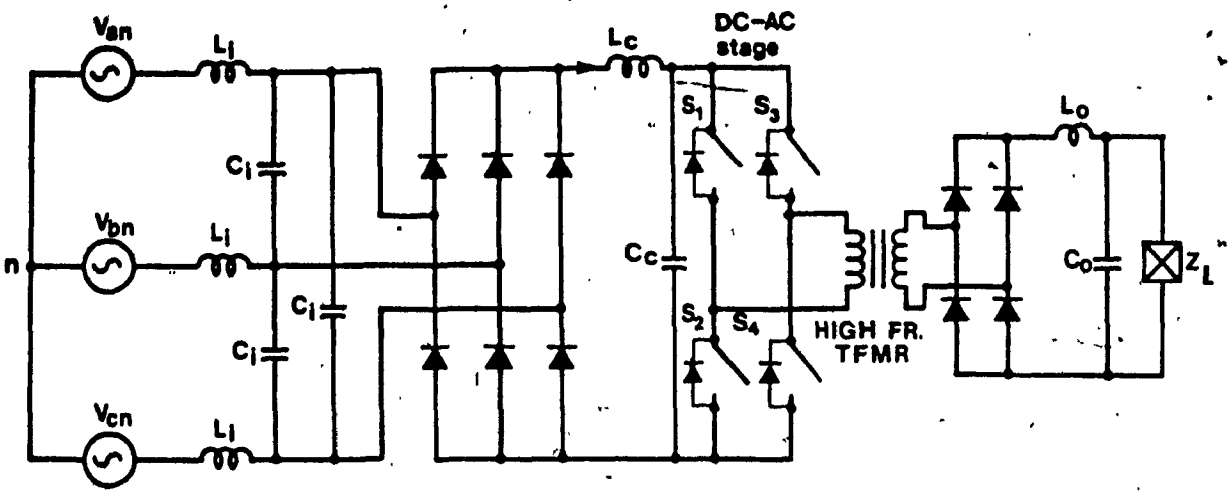
Therefore, from the above mentioned advantages and disadvantages, the Delco approach seems to be superior to the conventional phase control rectifier and the conventional Switch-Mode Rectifier. However, due to the variations in power circuit and control parameters among the three individual converters used in the Delco approach, a complete triplen harmonic cancellation can not be achieved. Moreover, the

conduction angle, α, in the Delco approach, must be higher than 150° in order to maintain 2.2% third harmonic component of the input line current. However, this is not possible due to the fluctuations of the input AC source. For maximum conduction angle utilization the boostrap boost technique was introduced [30] but that makes the control system to become more complex.

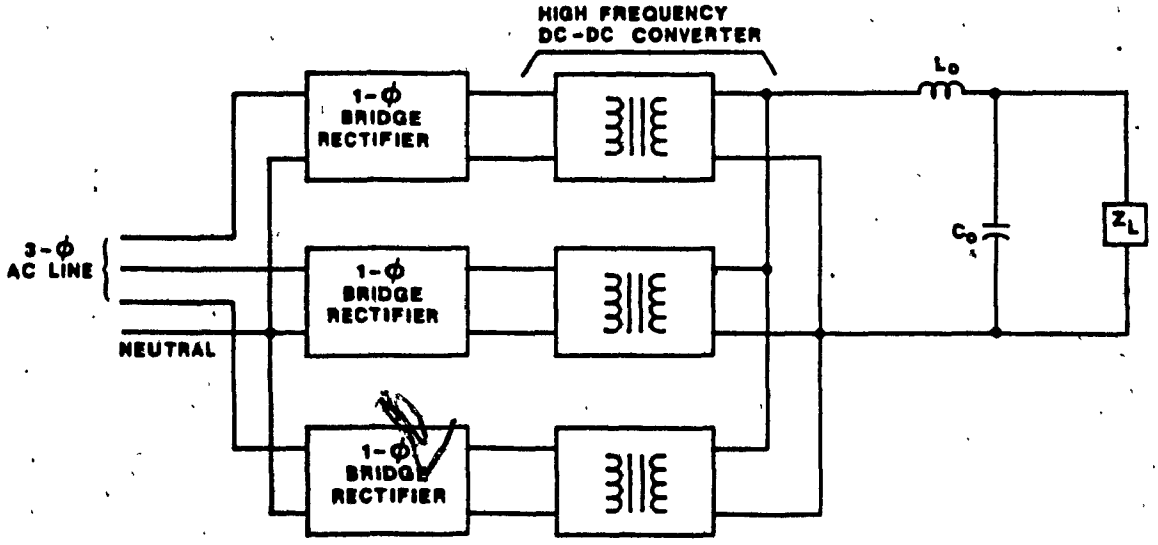
Fig. 4.1(c) shows a schematic diagram of a proposed SMR conversion scheme which has the advantages of the conventional SMR scheme and Delco approach and none of their disadvantages. However, the proposed scheme requires bidirectional power switches for the implementation of the AC to AC stage. Finally, it satisfies the required specifications mentioned previously with mihimum input and output filtering, and allows for controlled input power factor.

4.2 Circuit description

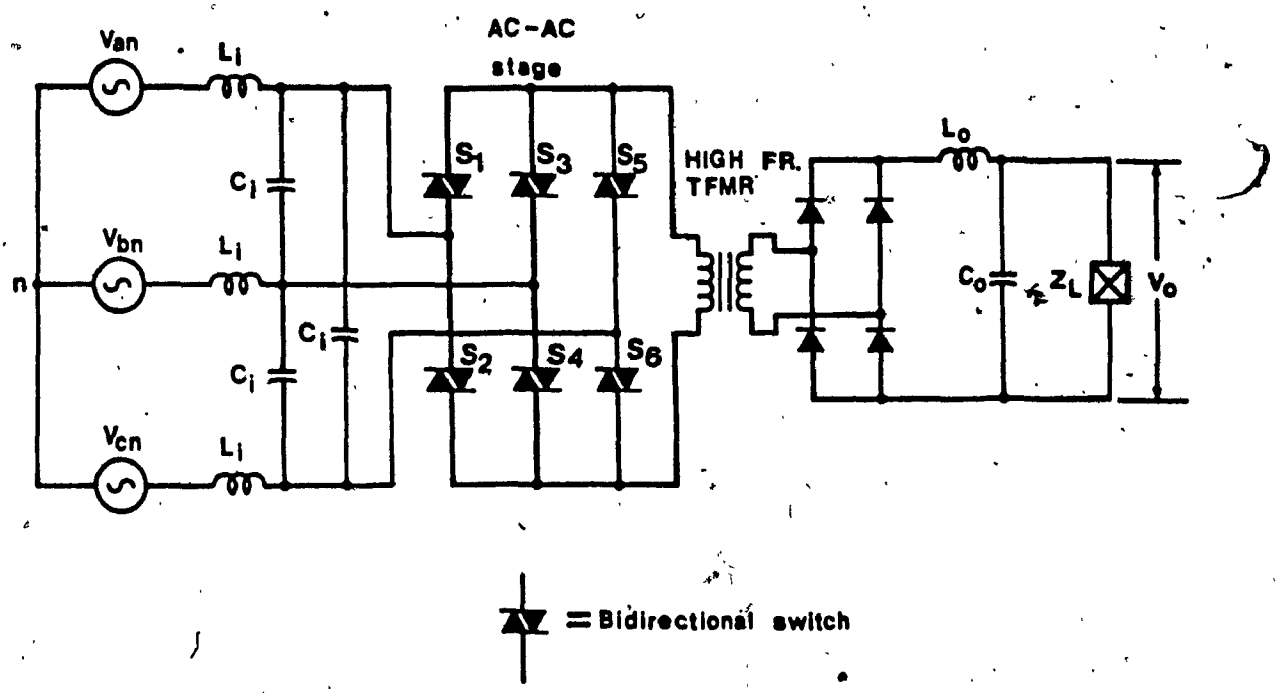
Fig. 4.2 shows a transistorized realization of the proposed AC to DC conversion scheme. The proposed SMR scheme consists of a PWM AC to AC converter (cycloconverter) stage and a full bridge rectifier stage. The main function of the cycloconverter stage is to input the low frequency three-phase AC source and output a high frequency PWM voltage. Thus the size and cost of the isolation transformer is considerably reduced. The main function of the full bridge rectifier is to convert the high frequency output voltage of the cycloconverter into a low frequency one which eventually provides the desired DC output voltage. Since the converter output voltage waveform consists of a train of pulses (Fig. 4.3(c)), some form of filtering is necessary in order to separate the DC component from the unwanted harmonic



4.1(a): Conventional Switch-Mode Rectifier



4.1(b): Switch-Mode Rectifier employing the Delco approach



4.1(c): Proposed Switch-Mode Rectifier

Fig. 4.1: Switch-Mode Rectifier Schemes.

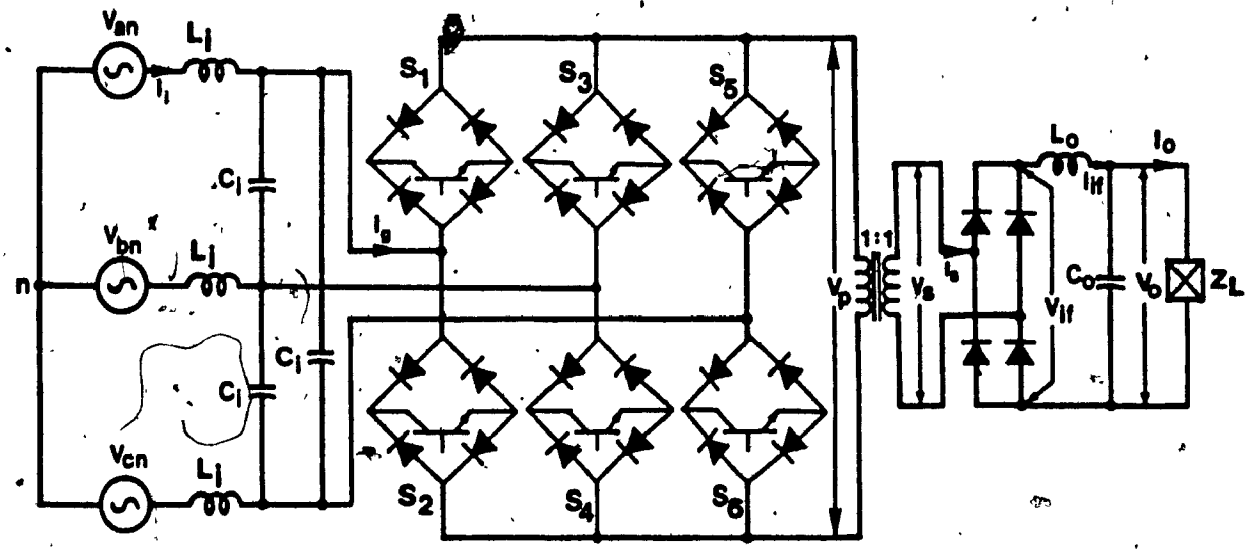


Fig. 4.2: Circuit diagram of the proposed Rectifier scheme.

components. Moreover, in order to minimize the size, weight, and cost of such a filter, the Sinusoidal Pulse Width Modulation (SPWM) technique (Fig. 4.3) was chosen for implementation. Finally, for this power conversion scheme, the low pass L-C filter was chosen for input and output filtering (Fig. 4.2) because it satisfies the harmonic distortion requirements with minimum number of components.

4.3. System analysis

In this section the proposed SMR scheme is analyzed under steady state conditions. The derived expressions are subsequently used to obtain the information necessary for reliable unit design.

4.3.1 Load conditions

In order to analyze the proposed unit, the following per unit load conditions are assumed for the rated output voltage and rated output current respectively.

$$V_o = 1 \text{ p.u. (Volts)} \tag{4.1}$$

$$I_o = 1 \text{ p.u. (Amps)} \tag{4.2}$$

4.3.2 Derivation of the SPWM output voltage

Fig. 4.3 illustrates the principle of Sinusoidal Pulse Width Modulation (SPWM) control technique. The employment of SPWM technique provides output voltage control and the same time it reduces the lower harmonic components of the input line current by proper selection of both normalized carrier frequency, f_{nc}, and Modulation factor, M_f (Fig. 4.3(a)). High order harmonic components of the AC source line current may increase, but these can be easily eliminated by small sized filters.

As in the three-phase inverter design case the normalized carrier frequency (f_{nc}) is selected in multiples of three. This prevents the dominant harmonic components, (see appendix C) present in $S_a(\omega t)$ and $S_b(\omega t)$ (Figs. 4.3(b) and (c)) from appearing in the overall switching function, $S_1(\omega t)$, spectrum. Furthermore by selecting the normalized carrier frequency in odd multiples of three, quarter wave symmetry is achieved which results in the elimination of even order harmonics. Consequently, the normalized carrier frequency is given by

$$f_{nc} = \frac{T_f}{T_c} = 3m \qquad (4.3)$$

where:

T_f = Period of the reference signal (Input voltage)

T_c = Period of the carrier signal

and,

$m = 3, 5, 7, 9, \ldots\ldots\ldots$

Letting $V_{an}(\omega t)$, $V_{bn}(\omega t)$ and $V_{cn}(\omega t)$ be the instantaneous values of the AC source supply and regarding Fig. 4.3(e) the SPWM output voltage, $V_{if}(\omega t)$, of the SMR unit is given by

$$V_{if}(\omega t) = \sum_{k=0,1}^{2} V_{an}(\omega_i t - \frac{2k\pi}{3}) \cdot S_1(\omega_i t - \frac{2k\pi}{3}) \qquad (4.4)$$

where:

$S_1(\omega t)$ is the overall switching function of the SMR unit obtained by employing SPWM (Fig. 4.3(e)) and considering cycloconverter and rectifier stage switching functions as one,

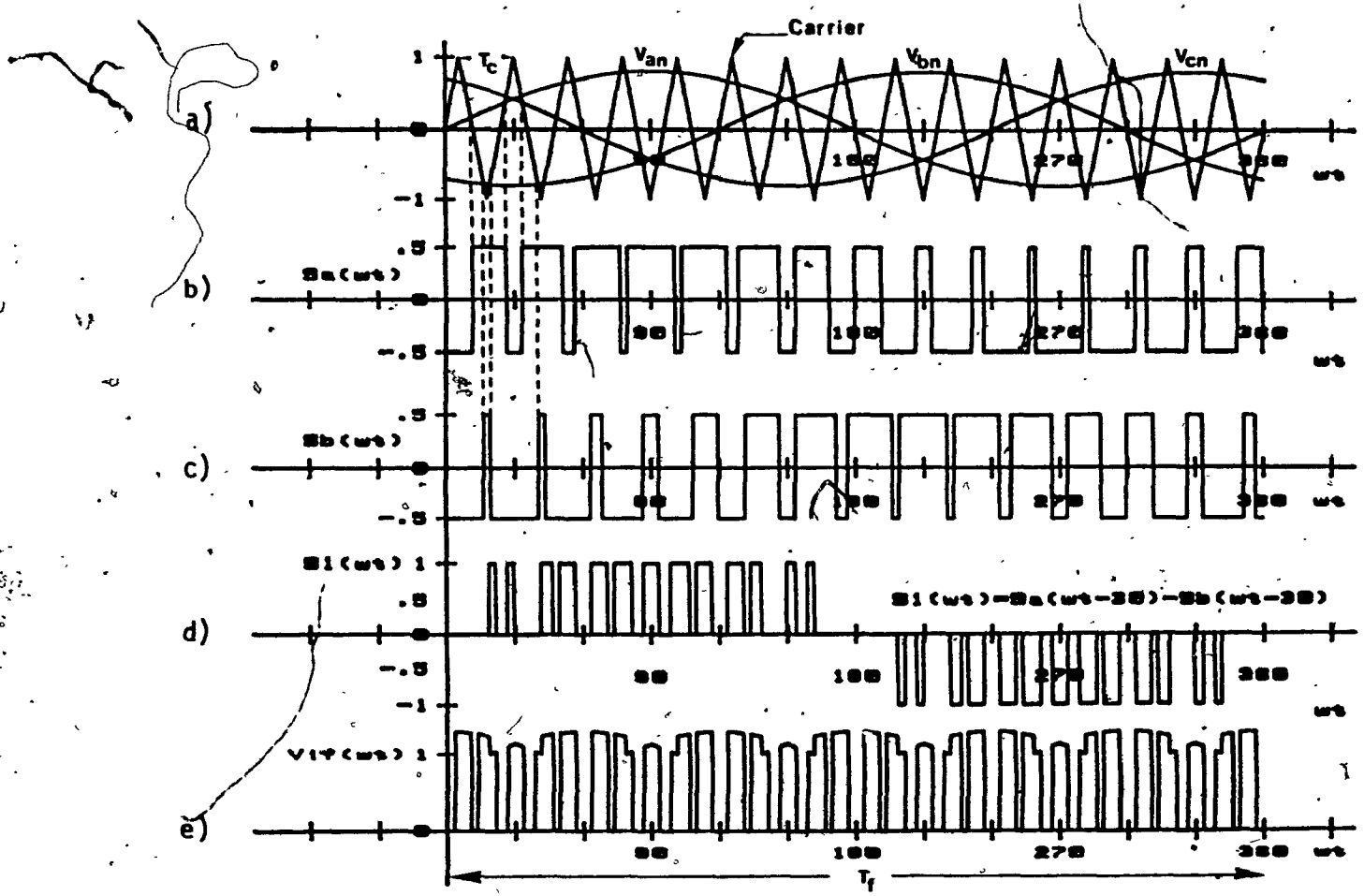


Fig. 4.3: Derivation of SPWM output voltage waveform, $V_{if}(\omega t)$, obtained with $M_f = 0.8$ and $f_{nc} = 15$ (f_{nc} was intentionally chosen equal to 15 for waveform clarity).

ω_i is the AC source operating frequency.

The overall switching function of the SMR unit can be mathematically described by

$$S_1(\omega t) = \sum_{\substack{n=1,5,7,\\ n\neq triplen}}^{\infty} A_n \sin(n\omega_i t) \qquad (4.5)$$

where:

A_n is the amplitude of the nth harmonic component of $S_1(\omega t)$.

Therefore, using eqns. (4.4) and (4.5) and regarding fig. 4.2 the SMR output voltage, $V_{if}(\omega t)$, can be expressed by

$$V_{if}(\omega t) = \sum_{k=0,1}^{2} \sum_{\substack{n=1,5,7,\\ n\neq triplen}}^{\infty} V_m A_n \sin(\omega_i t - \frac{2k\pi}{3}) \cdot \sin(n\omega_i t - 2K\pi) \qquad (4.6)$$

where :

V_m is the peak value of the AC source.

After further simplification eqn. (4.6) becomes

$$V_{if}(\omega t) = \sum_{\ell=0,6,12,}^{\infty} V_{if,\ell} \cos(\ell\omega_i t + \theta_\ell) \qquad (4.7)$$

where:

$$V_{if,\ell} = \frac{3V_m}{2} (A_{\ell+1} - A_{\ell-1}) \qquad (4.8)$$

θ_ℓ is the phase angle of the ℓth harmonic component.

Therefore, using eqns. (4.7) and (4.8) the DC component of the SPWM voltage waveform is given by

$$V_{if,0} = \frac{3V_m}{2} \cdot A_1 \qquad (4.9)$$

where:

A_1 is the amplitude of the fundamental component of the overall switching function, $S_1(\omega t) = (\sqrt{3}/2)M_f$ (4.10)

and where:

M_f is the modulation factor of the SPWM technique that must change in response to the variations of the input AC voltage in order to maintain a constant DC load voltage. For the specified variations (10% above and 20% below its nominal value, as section 1.5) the input AC voltage and assuming $M_f = 0.8$ at nominal input AC voltage then the values of M_f must vary between $0.7 \leq M_f \leq 1$.

Using eqns. (4.1), (4.9) and (4.10) the peak value of the AC source is given by

$$V_m = (\frac{2}{3})(\frac{2}{\sqrt{3}\, M_f}) = \frac{0.77}{M_f} \qquad (4.11)$$

The spectra of the overall function, $S_1(\omega t)$ and SMR output voltage waveform, $V_{if}(\omega t)$, are shown in Fig. 4.4(a) and (b) respectively. From the computer aided analysis (Appendix A) it was observed that the relative amplitude of the dominant harmonic component of $V_{if}(\omega t)$ is independent of the normalized carrier frequency (f_{nc}) value and is given by

$$V_{if,d} = V_{if,f_{nc}-3} = \frac{3}{2}(\frac{0.77}{M_f})(A_{f_{nc}-2} - A_{f_{nc}-4}) \qquad (4.12)$$

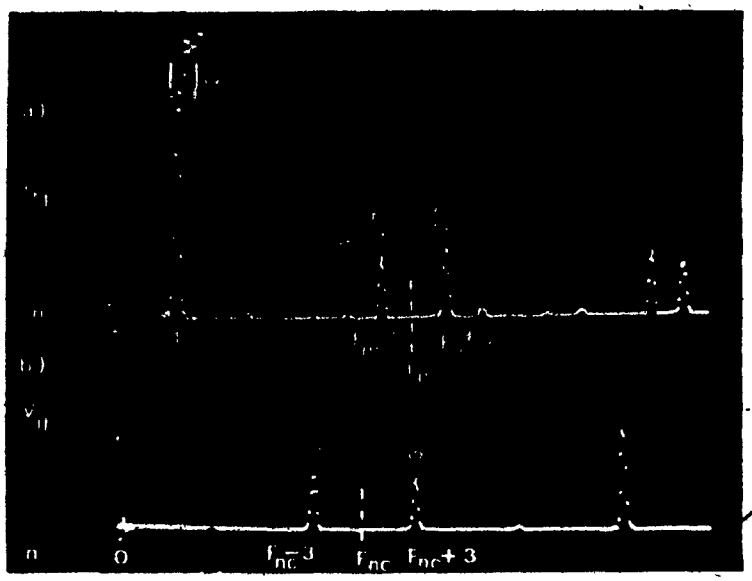


Fig. 4.4: Computer derived frequency spectra obtained for

a) SMR overall switching function, $S_1(\omega t)$

b) SMR SPWM output voltage, $V_{if}(\omega t)$

Therefore, regarding Fig. 4.4(a) and using eqn. (4.12) the dominant harmonic component of $V_{if}(\omega t)$, under worst operating condition ($M_f = 0.7$), is given by

$$V_{if,d} = (\frac{3}{2})(\frac{0.77}{0.7})(0.275-0.0154) = 0.428 \text{ p.u.} \quad (4.13)$$

4.3.3 Output filter

Since the SMR output voltage waveform $V_{if}(\omega t)$, consists of a modulated train of pulses (Fig. 4.3(e)), some form of filtering is necessary in order to separate the DC component from the undesired harmonic components. Therefore, using eqn. (4.13) the amplitude by which the dominant harmonic component (f_{nc}-3) has to be attenuated by the second order LC filter (Fig. 4.2), under no load condition, is given by

$$\Delta A = 20 \log_{10}(K_{v_o}) - 20 \log_{10}(V_{if,d}) \quad (4.14)$$

where:

K_{v_o} is the allowable output voltage ripple factor given by

$$K_{v_o} = \frac{V_{o,d(rms)}}{V_o} \quad (4.15)$$

and where:

$V_{o,d}$ is the rms value of the output voltage dominant harmonic component,

V_o is the output voltage dc component (= 1 p.u.).

Employing the characteristics of the second order filter and using exps. (4.13) and (4.14) the following expression is derived

$$\frac{20 \log_{10}(K_{v_o}) + 7.4}{20 \log_{10}\omega_{bo} - \log_{10}(f_{nc}-3)} = \frac{40}{\log_{10}\omega_{bo} - \log_{10}(10\omega_{bo})} \quad (4.16)$$

where:

ω_{bo} is the output filter break frequency = $\frac{1}{\sqrt{L_o C_o}}$

After further manipulation eqn. (4.16) becomes

$$L_o C_o = \frac{1}{[(f_{nc}-3)(10)^{(20\log_{10}(K_{v_o})+7.4)/40}]^2} \tag{4.17}$$

Finally, to select the filter components the factors of section 2.3.5 must be considered.

4.3.4 Cycloconverter stage

Regarding Fig. 4.1(c) the cycloconverter switching function is given by

$$S_c(\omega t) = S_1(\omega t) \cdot S_r(\omega t) \tag{4.18}$$

where:

$S_1(\omega t)$ is the SMR overall switching function,

$S_r(\omega t)$ is the Rectifier Stage switching function

$$= \frac{4}{\pi} \sum_{k=f_{nc},3f_{nc},5f_{nc},}^{\infty} B_k \sin k(\omega_i t) \tag{4.19}$$

and where:

$$B_k = \frac{f_{nc}}{k} \tag{4.20}$$

f_{nc} is the normalized carrier frequency.

Therefore, using eqns. (4.5), (4.18) and (4.19) eqn. (4.18) becomes

$$S_c(\omega t) = \frac{4}{\pi} \sum_{\substack{n=1,5,7, \\ n\neq triplen}}^{\infty} \sum_{k=f_{nc},3f_{nc},5f_{nc},}^{\infty} A_n B_k \sin(n\omega_i t) \cdot \sin(k\omega_i t) \tag{4.21}$$

After further simplification of eqn. (4.21) the mth harmonic component of the cycloconverter switching function, $S_c(\omega t)$, is given by

$$S_{c,m}(\omega t) = \frac{2}{\pi} \left[\sum_{k=f_{nc},3f_{nc},}^{m-1} A_{m-k}\, B_k \cos(m\omega_i t + \theta_{m-k}) \right.$$

$$+ \sum_{k=f_{nc},3f_{nc},}^{\infty} A_{m+k}\, B_k \cos(m\omega_i t + \theta_{m+k})$$

$$\left. + \sum_{\substack{n=1,5,7, \\ n\neq \text{triplen}}}^{\infty} A_n\, B_{n+m} \cos(m\omega_i t - \theta_n) \right] \qquad (4.22)$$

Therefore, the Fourier series of the switching function, $S_c(\omega t)$ is given by

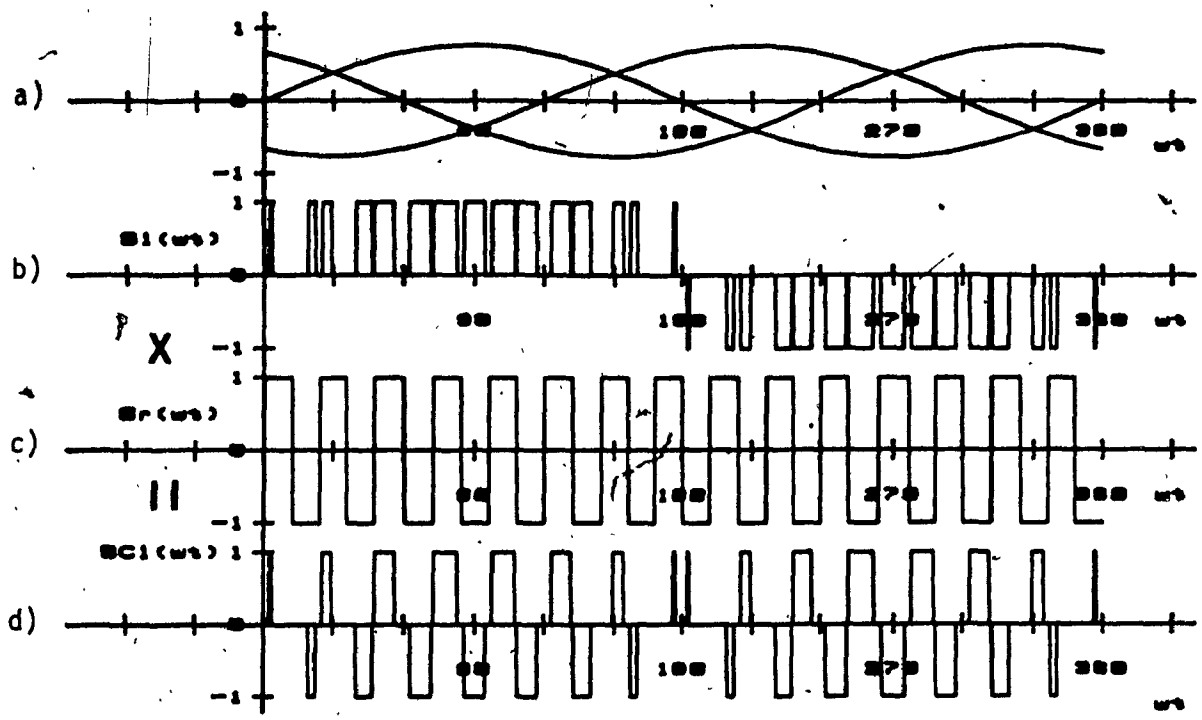
$$S_c(\omega t) = \sum_{\substack{m=2,4,8, \\ m\neq \text{multiple of six}}}^{\infty} C_m \cos(m\omega_i t + \theta_m) \qquad (4.23)$$

where :

C_m is the amplitude of the mth harmonic component of $S_c(\omega t)$ given by eqn. (4.22),

θ_m is the phase angle of mth harmonic component of $S_c(\omega t)$.

Using the digital computer program, the real time waveform of eqn. (4.23) and its respective spectrum were obtained and are presented in Fig. 4.5(d) and (e) respectively.



e)

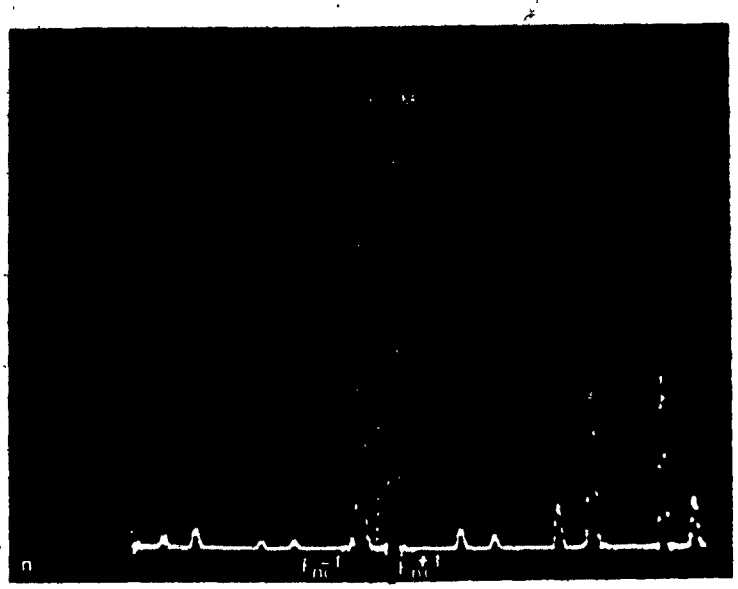


Fig. 4.5: Derivation of the cycloconverter stage switching function, $S_c(\omega t)$.

a) Three-phase AC source
b) SMR overall switching function, $S_1(\omega t)$
c) Rectifier stage switching function, $S_r(\omega t)$
d) Cycloconverter stage switching function, $S_c(\omega t)$
e) Frequency Spectrum of $S_c(\omega t)$

Employing the switching function, $S_c(\omega t)$, to the cycloconverter stage a HF AC to AC link is created which together with the high frequency transformer provides transformer isolation between the source and the load. Regarding Fig. 4.2, the transformer primary voltage is given by

$$V_p(\omega t) = \sum_{K=0,1}^{2} V_{an}(\omega_i t-\frac{2k\pi}{3})\cdot S_c(\omega_i t-\frac{2k\pi}{3}) \qquad (4.24)$$

Therefore, using eqn. (4.23) eqn. (4.24) becomes

$$V_p(\omega t)= \sum_{k=0,1}^{\ell} V_{an}(\omega_i t-\frac{2k\pi}{3})\cdot \sum_{\substack{m=2,4,8,\\ m\neq\text{multiple of six}}}^{\infty} C_m\cos(m(\omega_i t-\frac{2k\pi}{3})+\theta_m)$$

$$= \frac{V_m}{2}\Bigg[\sum_{\substack{m=2,4,8,\\ m\neq\text{multiple of six}}}^{\infty} C_m[\sin((m+1)\omega_i t+\theta_m)+\sin((m-1)\omega_i t+\theta_m)$$

$$+ \sin((m-1)(\omega_i t-120)+\theta_m)+\sin((m-1)(\omega_i t-120)+\theta_m)$$

$$+ \sin((m+1)(\omega_i t-240)+\theta_m)+\sin((m-1)(\omega_i t-240)+\theta_m)\Bigg] \qquad (4.25)$$

Simplifying eqn. (4.25) and using eqn. (4.11), the transformer primary voltage is given by

$$V_p(\omega t) = \frac{(3)(.77)}{2M_f}\sum_{n=3,9,15,21,}^{\infty} D_n\cos(n\omega_i t + \phi_n) \qquad (4.26)$$

where:

$$D_n = \sqrt{(C_{n-1}\sin\theta_{n-1}+C_{n+1}\sin\theta_{n+1})^2+(C_{n-1}\cos\theta_{n-1}+C_{n+1}\cos\theta_{n+1})^2}$$

$$\phi_n = \arctan\left(\frac{C_{n-1}\sin\theta_{n-1}+C_{n-1}\sin\theta_{n+1}}{C_{n-1}\cos\theta_{n-1}+C_{n+1}\cos\theta_{n+1}}\right)$$

Fig. 4.6(a) and (b) presents the real time waveform of $V_p(\omega t)$ and its respective spectrum obtained by the digital computer program. Regarding Fig. 4.6(b), the dominant harmonic component of $V_p(\omega t)$ is located at the normalized carrier frequency (f_{nc}) and its amplitude is independent of the value of f_{nc}. This indicates that the isolation transformer has to be designed to operate at f_{nc} p.u. frequency in order to prevent saturation.

Assuming that the current through the output filter inductor is ripple free (section 1.5 assumption iv), the cycloconverter input current is given by

$$I_g(\omega t) = I_o \cdot S_1(\omega t) \tag{4.27}$$

Therefore, using exps. (4.1), (4.2) and (4.5), exp. (4.27) becomes

$$I_g(\omega t) = \sum_{\substack{n=1,5,7,\\ n\neq triplen}}^{\infty} A_n \sin(n\omega_i t + \theta_n) \tag{4.28}$$

and its spectrum is the same as that shown in Fig. 4.4(a). Regarding Fig. 4.4(a), the dominant harmonic component of cycloconverter input current is located at f_{nc}-2 p.u. frequency. Its amplitude, which is independent of the normalized carrier frequency (f_{nc}) value, is given by

$$I_{g,d} = I_o \cdot A_{f_{nc}-2} = (1)(0.275)$$

$$= 0.275 \text{ p.u.} \tag{4.29}$$

Fig. 4.7 shows the cycloconverter stage input current, the current through a bidirectional switch and the current through a diode of the bidirectional switch. Regarding Fig. 4.7 and using the digital computer program, the following cycloconverter current ratings were obtained.

Average bidirectional switch current I_{AS} = 0.213 p.u. (4.30)

RMS bidirectional switch current I_{RS} = 0.46 p.u. (4.31)

Peak bidirectional switch current I_{PS} = 1 p.u. (4.32)

Average diode current I_{AD} = 0.11 p.u. (4.33)

RMS diode current I_{RD} = 0.34 p.u. (4.34)

Peak diode current I_{PD} = 1 p.u. (4.35)

Finally, using eqn. (4.11) the cycloconverter voltage ratings are given by,

Peak bidirectional switch forward blocking voltage

$$\hat{V}_{FB} = \sqrt{3}\, V_{m(max)} = \sqrt{3}\,(\frac{0.77}{0.7}) = 1.9 \text{ p.u.} \quad (4.36)$$

Peak bidirectional switch reverse blocking voltage

$$\hat{V}_{RB} = \sqrt{3}\, V_{m(max)} = \sqrt{3}\,(\frac{0.77}{0.7}) = 1.9 \text{ p.u.} \quad (4.37)$$

4.3.5 Input filter

As discussed in the introduction of this chapter the AC source line current harmonic components generated by the SMR unit must be less than 3% of the fundamental component. To achieve this requirement an input filter is placed between the AC source and the cycloconverter stage

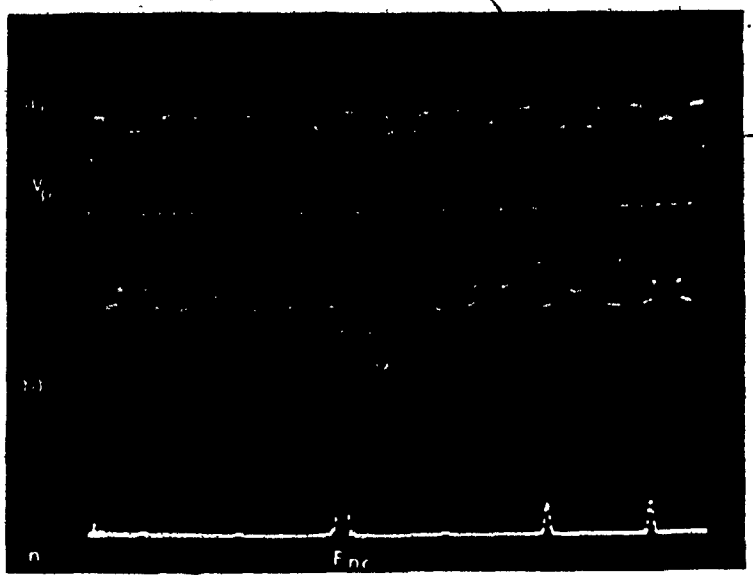


Fig. 4.6: Simulated waveform of the transformer primary voltage, $V_p(\omega t)$ and its respective frequency spectrum.

Fig. 4.7: SMR simulated waveforms.

a) Cycloconverter stage input current, $I_g(\omega t)$

b) Cycloconverter stage switch current, $I_{ct}(\omega t)$

c) Cycloconverter stage diode current, $I_{cd}(\omega t)$

input (Fig. 4.2). Regarding Fig. 4.2, the nth harmonic component of the AC source line current is given by

$$I_{i,n} = \frac{1}{n^2\omega_i^2 L_i(\frac{C_i}{3})-1} I_{g,n} \qquad (4.38)$$

where:

$I_{g,n}$ is the amplitude of the nth harmonic component of the cycloconverter input current, $I_g(\omega t)$,

ω_i is the AC source operating frequency

$$= 1 \text{ p.u.} \qquad (4.39)$$

L_i is the input filter inductance,

C_i is the input filter capacitance,

n is the harmonic order.

The factor 1/3 by which the input filter capacitance is multiplied is determined by the fact that eqn. (4.35) initially was obtained from the wye equivalent of the input filter circuit (Fig. 4.2). Therefore, using exps. (4.29), (4.30) and (4.39) the input filter components are given by

$$L_i C_i = \frac{X_{L_{i,1}}}{X_{C_{i,1}}} = \frac{3(I_{g,n} + I_{i,n})}{(f_{nc}-2)^2 I_{i,n}}$$

$$= \frac{3(.27+.03)}{(f_{nc}-2)^2(.03)} = \frac{30}{(f_{nc}-2)^2} \text{ p.u.} \qquad (4.40)$$

Exp. (4.37) shows the drastic effect of the normalized carrier frequency f_{nc}, on the size of the input filter components C_i and L_i. Finally, to prevent the resonance condition in the filter the following two conditions must hold

$$L_i\omega_i < \frac{1}{C_i\omega_i}; \quad \text{for the fundamental and } (f_{nc}-2)L_i\omega_i > \frac{1}{(f_{nc}-2)C_i\omega_i};$$

for the dominant harmonic component.

4.4 Design Example

In order to illustrate the significance and facilitate the understanding of theoretical results obtained in previous sections the following example is given:

V_o = DC load voltage = 48V

I_o = DC load current = 4A

f_i = Supply frequency = 60 Hz

THD = Input voltage Total Harmonic Distortion < 5%

ΔV_o = Output voltage ripple = .01

f_{nc} = Normalized carrier frequency = 51

Therefore, from the above specifications

1 p.u. volts = 48V

1 p.u. current = 4A

1 p.u. Impedance = $\frac{48}{4} = 12\Omega$

Using eqns. (4.17) and (4.40) the LC products of the input and output filter components are obtained

$$L_iC_i = \frac{29}{(51-2)^2} = 0.012 \text{ p.u.} \qquad \text{(E1)}$$

$$L_o C_o = 0.0163 \text{ p.u.} \tag{E2}$$

Therefore using the above p.u. values and chosing 0.5 p.u. capacitance for C_i and 10 p.u. capacitance for C_o, the p.u. and actual values of both filter components are obtained

$$L_i = \frac{0.012}{0.5} = 0.024 \text{ p.u.} \tag{E3}$$

$$L_i = \frac{0.024 \times 12}{377} = 764 \ \mu H \tag{E4}$$

$$C_i = 0.5 \text{ p.u.} \tag{E5}$$

$$C_i = \frac{0.5}{12 \times 377} = 110.5 \ \mu F \tag{E6}$$

$$L_o = \frac{0.0173}{10} = 0.00163 \text{ p.u.} \tag{E7}$$

$$L_o = \frac{0.00163 \times 12}{377} = 52 \ \mu H \tag{E8}$$

$$C_o = \frac{10}{12 \times 377} = 2,210 \ \mu F \tag{E9}$$

Also, using exps.(4.27) through (4.34), the cycloconverter current and voltage ratings are obtained

$$I_{AS} = 0.213 \times 4 = 0.852 \text{ A} \tag{E10}$$

$$I_{RS} = 0.46 \times 4 = 1.85 \text{ A} \tag{E11}$$

$$I_{PS} = 4 \text{ A} \tag{E12}$$

$$I_{AD} = 0.11 \times 4 = 0.44 \text{ A} \tag{E13}$$

$$I_{RD} = 0.34 \times 4 = 1.36 \text{ A} \tag{E14}$$

$$I_{PD} = 4 \text{ A} \tag{E15}$$

$$\hat{V}_{FB} = \hat{V}_{RB} = 1.9 \times 48 = 91.2 \text{ V} \tag{E16}$$

Finally the peak input voltage is given by

$$V_{m(max)} = \left(\frac{0.77}{0.7}\right) \times 48 = 52.8 \text{ V} \qquad \text{(E17)}$$

4.5 Conclusions

In this chapter a SPWM controlled Switch-Mode Rectifier scheme was presented which provides high frequency transformer isolation between the source and the load. Moreover, the proposed scheme exhibits controlled input power factor, low input THD and requires small sized filter components.

CHAPTER 5

A NOVEL BILATERAL HIGH FREQUENCY LINK CONVERTER

5.1 Introduction

The ever increasing demand for a compact, economical and efficient power conversion unit that incorporates a battery charger into a DC to AC inverter has put a heavy emphasis to propose and analyze such a bilateral power conversion scheme using an HF link. The proposed power conversion scheme has a very wide use in stand-by power supplies and when the output filter is eliminated can be applied as a voltage source AC motor drive and on-board battery charger for electric vehicles.

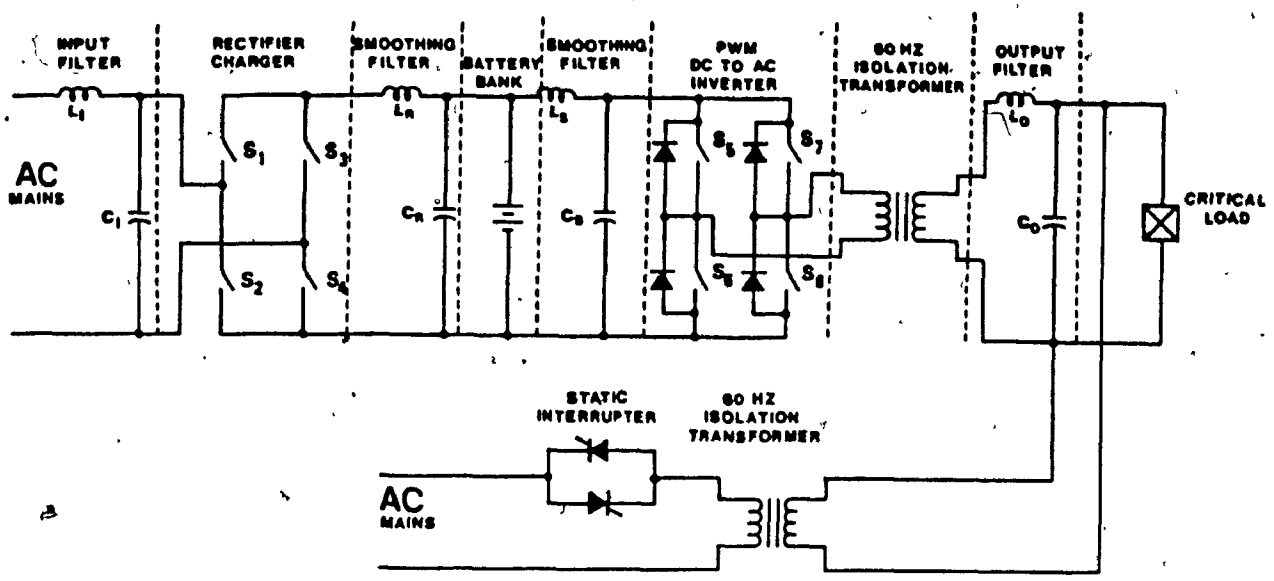
Fig. 5.1(a) shows the conventional Uninterruptible Power Supply (UPS) system which consists of a battery charger, battery and inverter. The battery, which is used to supply DC power to the inverter stage during power disturbances and failures, must be recharged at regular intervals. As it can be seen from Fig. 5.1(a) a separate rectifier-charger is employed for this purpose. However, when the inverter stage is synchronized with the mains then it also can function as an AC to DC converter thus transferring power from the mains to the battery. Fig. 5.1(b) shows a configuration of such a bilateral power conversion scheme. The analysis and operation of this power conversion scheme is presented in references [31], [32]. The disadvantage of this power conversion scheme is that the size of the isolation transformer, which is employed between the DC bus and the load, must be designed for the fundamanetal instead of the inverter switching frequency.

Consequently, the high inverter switching frequency cannot be exploited for reducing the size of the isolation transformer. However, the inclusion of a cycloconverter power conversion stage in such a power conversion scheme can yield considerable reduction of the isolation transformer. Fig. 5.1(c) shows the proposed power conversion scheme that utilizes a bilateral HF link.

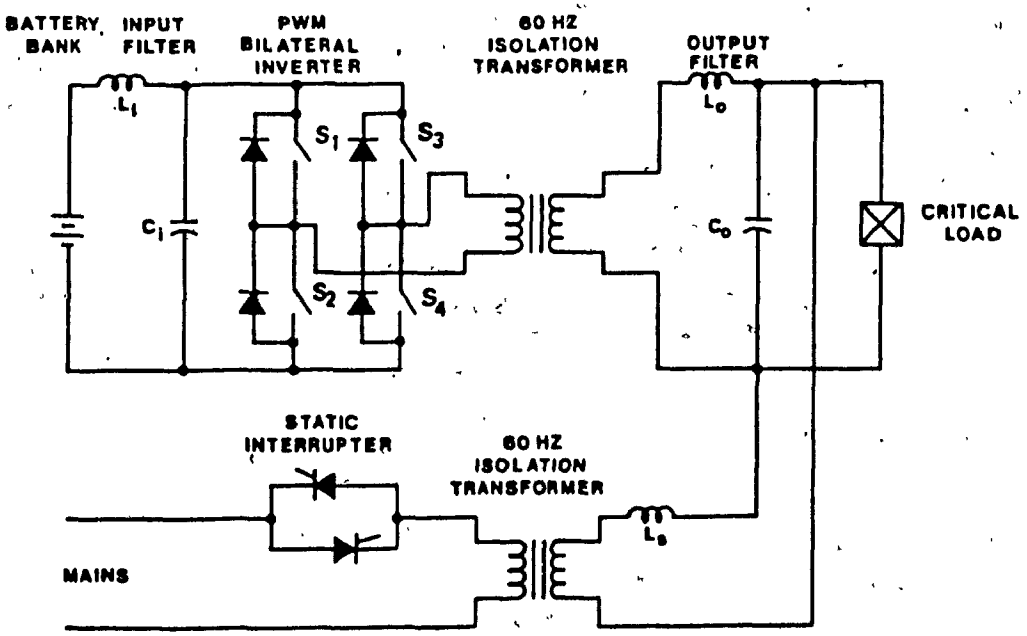
5.2 System description

Fig. 5.2 shows a transistorized realization of the proposed bilateral HF link converter. The proposed converter consists of a PWM inverter stage and a cycloconverter stage. The function of the inverter is two-fold: First, when the converter delivers power to the load the inverter stage acts as an HF link which inputs the DC bus voltage and outputs high frequency Sinusoidal Pulse Width Modulated (SPWM) voltage without saturating the transformer. Also because of the high frequency SPWM used, the isolation transformer is providing isolation at switching frequency thus resulting in substantial cost and weight reduction for the isolation transformer. Second, when the converter delivers power to the DC bus in the AC to DC mode the inverter stage operates as a rectifier rectifying the high frequency voltage provided by the cycloconverter stage.

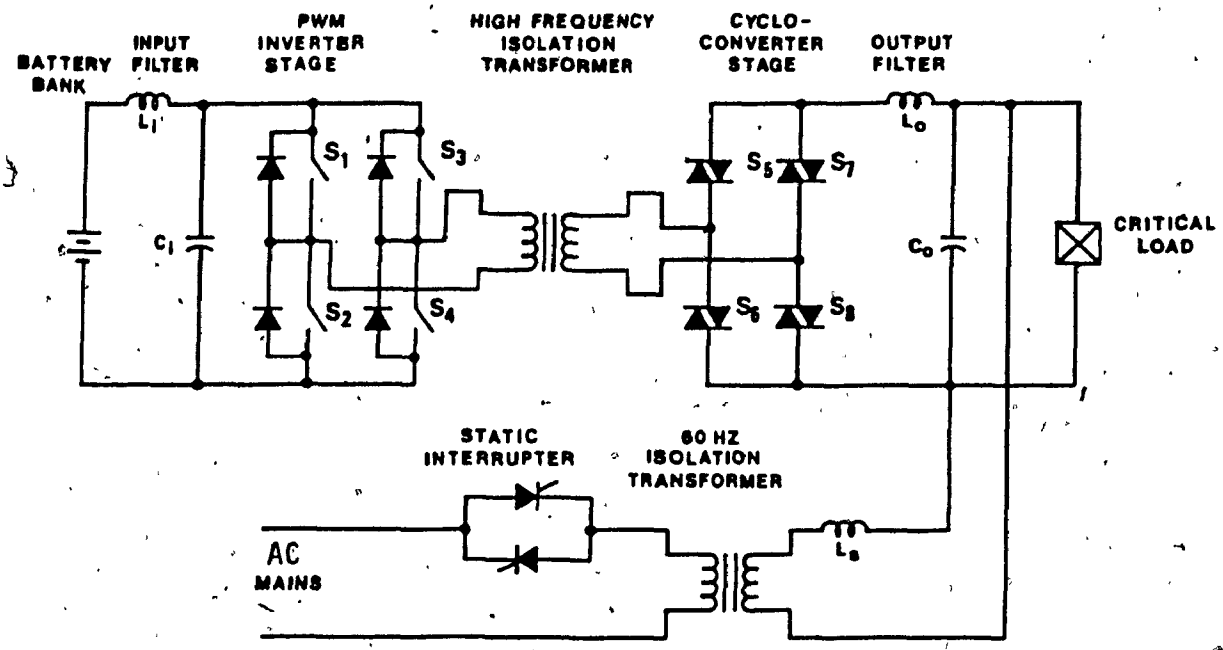
The main function of the cycloconverter stage when the converter operates in DC to AC mode is to convert the high frequency SPWM output voltage of the inverter stage into the required low frequency output voltage. Furthermore, when the converter operates in the AC to DC mode the cycloconverter stage converts the low AC input frequency



5.1(a): Conventional UPS system



5.1(b): UPS system using the conventional bilateral PWM inverter



5.1(c): UPS system using the proposed bilateral HF link converter

Fig. 5.1: Configuration of UPS systems.

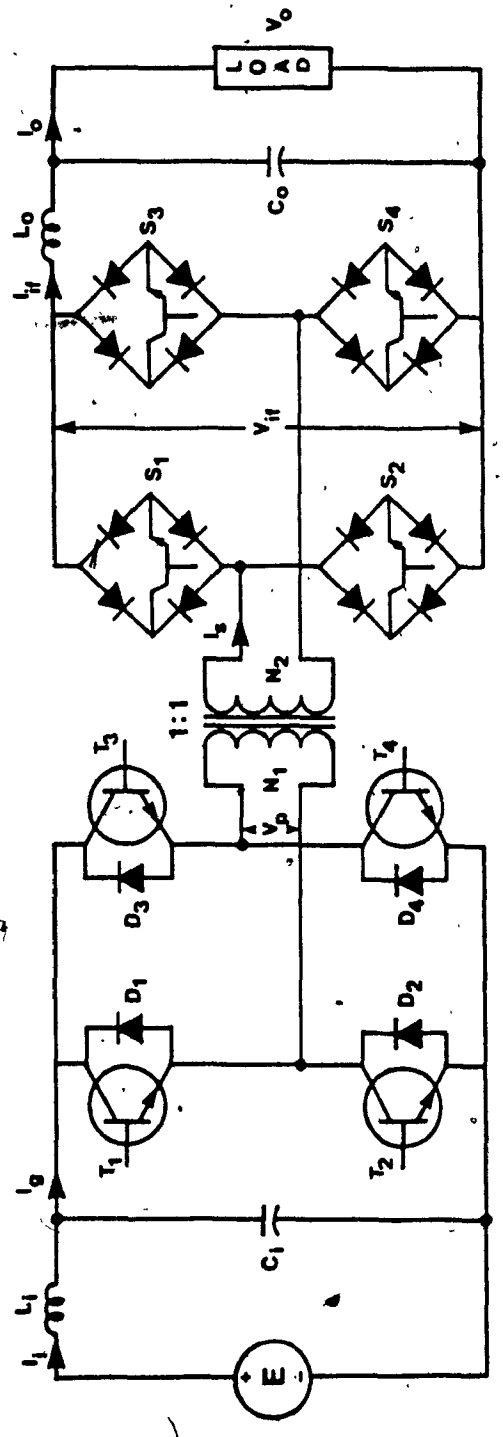


Fig. 5.2: Circuit diagram of the proposed bilateral HF link converter.

voltage into a high frequency voltage in order to prevent the saturation of the high frequency transformer. Therefore, during the AC to DC mode the cycloconverter stage provides an HF link between the source and the battery (load).

5.3 System analysis in the DC to AC mode

In this section the bilateral HF link converter is analyzed under steady-stage conditions. The derived expressions are subsequently used to obtain the information necessary for the safe converter design.

5.3.1 Load conditions

In order to generalize the analysis of the proposed conversion scheme the rated output voltage, V_o, and rated output current, I_o, are expressed in per unit as follows:

$$V_{o(rms)} = 1 \text{ p.u. (volts)} \qquad (5.1)$$

$$I_{o(rms)} = 1 \text{ p.u. (Amps)} \qquad (5.2)$$

5.3.2 Derivation of the proposed converter input and output quantities $V_{if}(\omega t)$, $I_{if}(\omega t)$ and $I_g(\omega t)$

In order to derive the necessary expressions required for the converter input and output filter design the frequency spectra of the input and output quantities $V_{if}(\omega t)$, $I_{if}(\omega t)$ and $I_g(\omega t)$ (Fig. 5.2) must be known. These quantities can be easily obtained when the switching functions of the inverter and cycloconverter stages are represented by an overall switching function, $S(\omega t)$. As mentioned earlier in the introduction of this chapter, one of the requirements of the proposed converter besides the reduction of the isolation transformer was the reduction of the input and output filter components. To achieve this reduction the SPWM control technique with variable

Modulation factor was chosen to be employed as the overall converter switching function for the same reasons that were explained in section 2.3.2.

By using the SPWM control technique with variable Modulation factor (Fig. 2.4) results obtained with the developed computer program (Appendix A) have shown that

a) the amplitude of the fundamental component of the converter overall switching function ($S(\omega t)$) is independent of the value of the normalized carrier frequency (f_{nc}) and is given by

$$A_1 = M_f \qquad (5.3)$$

where:

M_f is the Modulation factor of the SPWM technique that must change in response to the variations of the input DC voltage in order to maintain a constant load voltage. For the specified variations (10% above and 20% below its nominal value, see section 1.5) for the input DC voltage and assuming $M_f = 0.8$ at nominal input DC voltage then the values of M_f must vary between

$$0.7 \leq M_f \leq 1 \qquad (5.3a)$$

b) the value of normalized carrier frequency (f_{nc}) and the order of the dominant harmonic component (d) of the overall converter switching function ($S(\omega t)$), under worst operating condition ($M_f = 0.7$), are related by

$$d = 2f_{nc} - 1 \qquad (5.4)$$

c) the amplitude of the dominant harmonic component (d) of the overall converter switching function ($S(\omega t)$) is independent of the value of the normalized carrier frequency (f_{nc}) and under worst operating condition ($M_f = 0.7$) is given by

$$A_d = 0.354 \tag{5.5}$$

Although the overall converter switching function, $S(\omega t)$, is depicted in Fig. (2.4(d)) it would be required to be expressed in mathematical form in order to be able to obtain the frequency spectra of the required converter input and output quantities ($V_{if}(\omega t)$, $I_{if}(\omega t)$, $I_g(\omega t)$. Such mathematical form can be obtained by deriving its Fourier series expansion which is given by

$$S(\omega t) = \sum_{n=1,odd}^{\infty} A_n \sin(n\omega_o t)$$

$$= M_f \sin(\omega_o t) + \sum_{n=d}^{\infty} A_n \sin(n\omega_o t) \tag{5.6}$$

where:

A_n is the amplitude of the nth harmonic component of $S(\omega t)$.

ω_o is the converter operating frequency taken as 1 p.u.

Therefore, using eqn. (5.6) and the switching function relations given in appendix D the quantities $V_{if}(\omega t)$, $I_{if}(\omega t)$ and $I_g(\omega t)$ are given by

$$V_{if}(\omega t) = E \cdot S(\omega t) = EM_f \sin(n\omega_o t) + E\sum_{n=d}^{\infty} A_n \sin(n\omega_o t) \tag{5.7}$$

$$I_{if}(\omega t) = \frac{V_{if}(\omega t)}{Z_o(\omega t)} = \frac{E\, M_f \sin(\omega_o t+\phi_1)}{|Z_{o,1}|} + \sum_{n=d}^{\infty} \frac{A_n \sin(n\omega_o t+\phi_n)}{|Z_{o,n}|}$$

$$= B_1 \sin(\omega_o t + \phi_1) + \sum_{n=d}^{\infty} B_n \sin(n\omega_o t + \phi_n) \qquad (5.8)$$

$$I_g(\omega t) = I_{if}(\omega t) \cdot S(\omega t)$$

$$= \frac{M_f B_1}{2} \cos\phi_1 + \frac{M_f B_1}{2} \cos(2\omega_o t + \phi_1) +$$

$$+ B_1 \sin(\omega_o t + \phi_1) \cdot \sum_{n=d}^{\infty} A_n \sin(n\omega_o t) +$$

$$+ \sum_{n=d}^{\infty} \sum_{k=d}^{\infty} B_n A_k \sin(n\omega_o t + \phi_n) \cdot \sin(k\omega_o t) \qquad (5.9)$$

where:

B_1 is the amplitude of the fundamental component of the converter output current, $I_{if}(\omega t)$, given by

$$B_1 = \sqrt{2} \text{ p.u.} \qquad (5.10)$$

for $f_{n_c} \geq 17$ (Realistic values for HF applications)

B_n is the amplitude of the nth harmonic component of $I_{if}(\omega t)$,

Z_o is the input impedance of the output filter,

$|Z_{o,n}|$ is the magnitude of Z_o at the nth harmonic frequency

ϕ_1 is the phase displacement between respective fundamental components of $V_{if}(\omega t)$ and $I_{if}(\omega t)$. For $f_{nc} \geq 17$, $X_{c_o} = 2$ p.u.

and $X_{L_o} <$ .1 p.u. was found that $\phi_{1(max)}=51°$ and $\phi_{1(min)}=0°$ for loads vary from 0.8 leading to 0.8 lagging.

$$\phi_n = \tan^{-1}\left(\frac{\text{Imag}\,(Z_{o,n})}{\text{Real}\,(Z_{o,n})}\right) \tag{5.11}$$

Eqn. (5.7) implies that in order to obtain 1 p.u. rms load voltage (exp. 5.1) the input DC bus must be

$$E = \frac{\sqrt{2}}{M_f} \text{ p.u.} \tag{5.12}$$

Moreover, using the inequality (5.3(a)) the maximum and minimum values of the input DC bus are given by

$$E_{max} = \frac{\sqrt{2}}{0.7} = 2 \text{ p.u.} \tag{5.13a}$$

$$E_{min} = \frac{\sqrt{2}}{1} = \sqrt{2} \text{ p.u.} \tag{5.13b}$$

Therefore, using exps. (5.5), (5.7) and (5.13(a)) the amplitude of the dominant harmonic component of the converter output voltage ($V_{if}(\omega t)$), under worst operating condition ($M_f = 0.7$), is given by

$$V_{if,d} = E_{max} \cdot A_d = (2)(0.354) = 0.7 \text{ p.u.} \tag{5.14}$$

Also, using exps. (5.9) and (5.10) and the inequality (5.3(a)), the following expressions necessary for the input and output filter design are derived

$$I_{g,o} = \frac{\sqrt{2}\, M_f}{2} \cos\phi_1 \text{ p.u.} \tag{5.15a}$$

$$I_{g,o(min)} = \frac{(\sqrt{2})(0.7)}{2} \cos\phi_{1(max)} = \frac{(\sqrt{2})(0.7)(0.7)}{2} = 0.35 \text{ p.u.} \tag{5.15b}$$

$$I_{g,o(max)} = \frac{(\sqrt{2})(1)(1)}{2} = \frac{\sqrt{2}}{2} \text{ p.u.} \qquad (5.15c)$$

$$I_{g,2} = \frac{\sqrt{2}\, M_f}{2} \text{ p.u.} \qquad (5.16a)$$

$$I_{g,2(min)} = \frac{(\sqrt{2})(0.7)}{2} = \frac{1}{2} \text{ p.u.} \qquad (5.16b)$$

$$I_{g,2(max)} = \frac{(\sqrt{2})(1)}{2} = \frac{\sqrt{2}}{2} \text{ p.u.} \qquad (5.16c)$$

where

$I_{g,o}$ is the dc component of the converter input current, $I_g(\omega t)$,

$I_{g,2}$ is the amplitude of the second-order harmonic component of the converter input current, $I_g(\omega t)$.

Finally, the simulated waveforms for the quantities $V_{if}(\omega t)$, $I_{if}(\omega t)$ and $I_g(\omega t)$ for $M_f = 1$, $P_f = 0.8$ leading and $f_{nc} = 7$ (f_{nc} has been intentionally chosen low and equal to 7 for waveform clarity) are the same as that shown in Figs. 2.5 and 2.6 of section 2.3.4.

5.3.3 Output filter

Having derived the value of the dominant harmonic component, which is given by eqn. (5.14), the output filter components can be obtained using the procedure discussed in section 2.3.5. Consequently, using eqns. (2.25) and (5.14) in order to insure a THD $\leq$ 5% the output filter break frequency, ω_{bo}, must be

$$\omega_{bo} = (2 f_{nc} - 1)(10)^{-27.5/40} \text{ p.u.} \qquad (5.17)$$

where:

1 p.u. frequency is the converter operating frequency, ω_o.

Consequently, the output filter components are given by

$$\frac{X_{L_{o,1}}}{X_{C_{o,1}}} = L_o C_o = \frac{24}{(2f_{nc}-1)^2} \text{ p.u.} \tag{5.18}$$

5.3.4 Input filter

In this section the input filter components are derived as a function of the allowable filter inductor current ripple factor, K_{i_i}, and filter capacitor voltage ripple factor, K_{v_i}.

Regarding Fig. 2.6 (section 2.3.4) the dominant harmonic component of the inverter stage input current, $I_g(\omega t)$, is the second. Therefore, using the eqns. derived in section 2.3.6 the filter components must satisfy the following two relations in order to insure the specified allowable current and voltage ripple factors

$$\frac{X_{L_{i,1}}}{X_{C_{i,1}}} = \frac{I_{g,2(rms)}}{4\, K_{i_i}\, I_{g,o}} + K_{i_i} \tag{5.19}$$

$$\frac{X_{L_{i,1}}\, X_{C_{i,1}}}{4X_{L_{i,1}} - X_{C_{i,1}}} = \frac{K_{v_i}\, V_{c,o}}{2\, I_{g,2(rms)}} \tag{5.20}$$

where:

$I_{g,2(rms)}$ is the rms value of the second-order harmonic component of the converter input current, $I_g(\omega t)$,

$V_{c,o}$ is the dc component of the input filter capacitor voltage which is equal to E.

Therefore, substituting exps. (5.15(b)), (5.16(b)) and (5.13(a)) into exps. (5.19) and (5.20) the relations of the filter components as function of the ripple factors, under worst operating conditions (M_f = 1 and P_f = .8 leading), are given by

$$\frac{X_{L_{i,1}}}{X_{C_{i,1}}} = \frac{0.28}{K_{i_i}} + K_{i_i} \text{ p.u.} \qquad (5.21)$$

$$\frac{X_{L_{i,1}} X_{C_{i,1}}}{4X_{L_{i,1}} - X_{C_{i,1}}} = 1.414\ K_{v_i} \text{ p.u.} \qquad (5.22)$$

5.3.5 Derivation of the cycloconverter and inverter stage switching functions ($S_c(\omega t)$, $S_i(\omega t)$)

Fig. 5.3(b) shows the derivation of the cycloconverter stage switching function, $S_c(\omega t)$. As it can be seen $S_c(\omega t)$ is a bidirectional square wave (1 or -1 states only) with frequency equal to normalized carrier frequency (f_{nc}), whose states change at the intervals defined by the peaks of the triangular carrier. Regarding Fig. 5.3 the mathematical expression representing $S_c(\omega t)$ is given by

$$S_c(\omega t) = \frac{4}{\pi} \sum_{n=f_{nc},3f_{nc},5f_{nc},}^{\infty} C_n \sin(n\omega_o t - \frac{n\pi}{2}) \qquad (5.23)$$

where

$$C_n = \frac{f_{nc}}{n} \qquad (5.24)$$

$\frac{n\pi}{2}$ is the phase displacement between the nth harmonic component of $S_c(\omega t)$ and $S(\omega t)$.

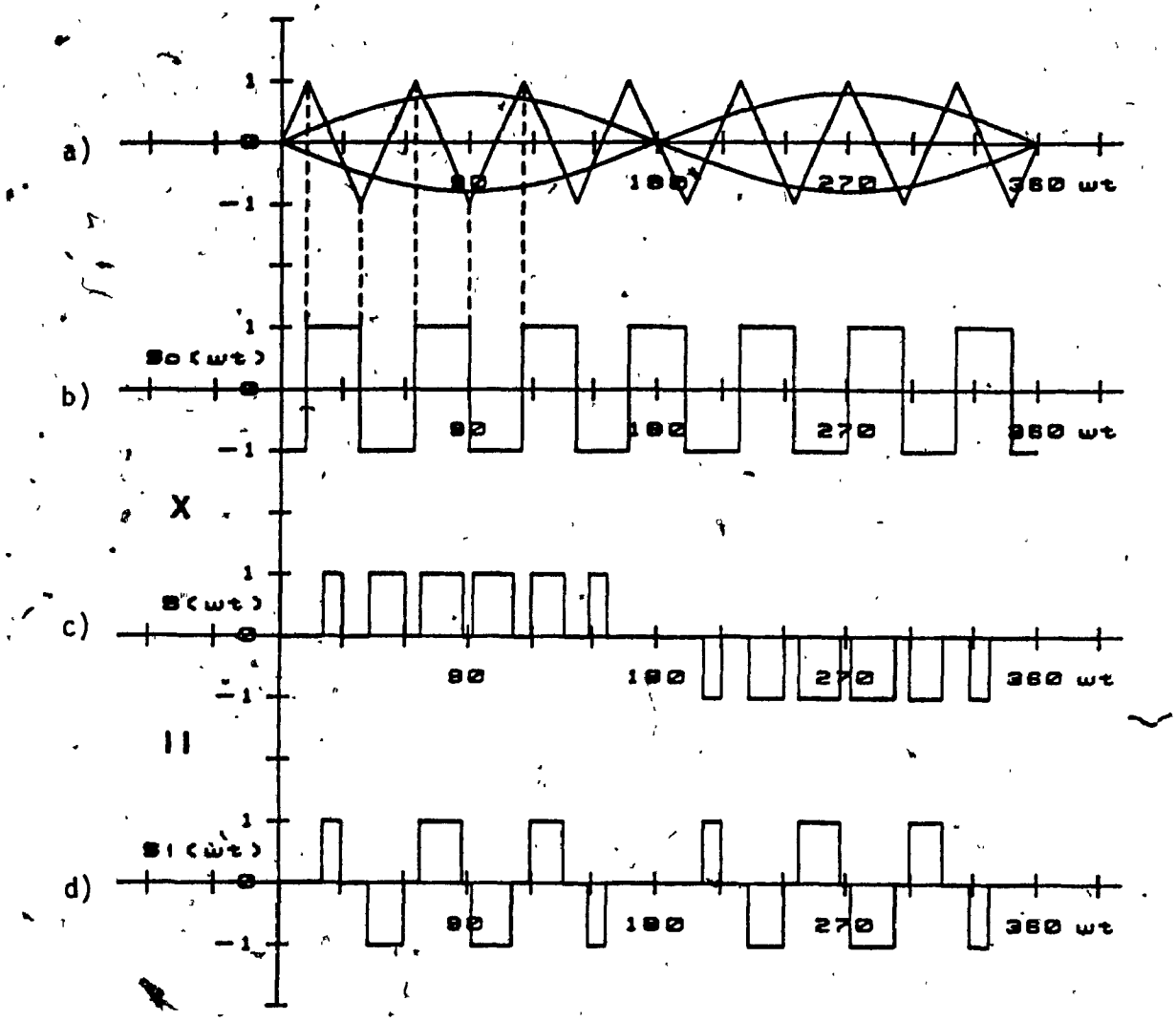


Fig. 5.3: Derivation of the cyclonverter and inverter stage switching functions.

a) References and carrier waveforms
b) Cycloconverter switching function, $S_c(\omega t)$
c) Converter overall switching function, $S(\omega t)$
d) Inverter stage switching function, $S_i(\omega t)$

Also, from Fig. 5.3 it can be seen that the inverter stage switching function is given by

$$S_i(\omega t) = S_c(\omega t) \cdot S(\omega t) \tag{5.25}$$

Therefore, substituting eqns. (5.6) and (5.23) into (5.25) then

$$S_i(\omega t) = \frac{4}{\pi} \sum_{n=1,\text{odd}}^{\infty} \sum_{k=f_{nc},3f_{nc},}^{\infty} A_n C_k \sin(n\omega_o t) \cdot \sin(k\omega_o t - \frac{k\pi}{2}) \tag{5.26}$$

Consequently, using eqns. (5.25) and (5.26) and the switching function relations given in appendix D the cycloconverter stage input current, $I_s(\omega t)$, and the inverter stage output voltage, $V_p(\omega t)$, expressions can be obtained. These quantities, which are necessary for the design of the isolation transformer and for the main component ratings of the inverter and cycloconverter stage, are given by

$$I_s(\omega t) = I_{if}(\omega t) \cdot S_c(\omega t) \tag{5.27}$$

$$V_p(\omega t) \triangleq E\, S_i(\omega t) \tag{5.28}$$

Substituting eqns. (5.8), (5.25) and (5.26) into eqns. (5.27) and (5.28) then

$$I_s(\omega t) = \frac{4B_1}{\pi} \sin(\omega_o t + \phi_1) \sum_{n=f_{nc},3f_{nc},}^{\infty} C_n \sin(n\omega_o t - \frac{n\pi}{2}) +$$

$$+ \sum_{n=d}^{\infty} \sum_{k=f_{nc},3f_{nc},}^{\infty} B_n C_k \sin(n\omega_o t + \phi_n) \cdot \sin(k\omega_o t + \frac{k\pi}{2}) \tag{5.29}$$

$$V_p(\omega t) = \frac{4E}{\pi}\sum_{n=1,\text{odd}}^{\infty}\sum_{k=f_{nc},3f_{nc},}^{\infty} A_n C_k \sin(n\omega_o t)\cdot\sin(k\omega_o t - \frac{k\pi}{2}) \tag{5.30}$$

Moreover, assuming that the normalized carrier frequency $f_{n_c} \geq 17$ (proper choice for high-switching-frequency applications) the double summation of eqn. (5.29) can be neglected because the amplitudes of B_n for $n \geq 9$ are negligible. Consequently, eqn. (5.29) becomes

$$I_s(\omega t) = \frac{2\sqrt{2}}{\pi}\sum_{n=f_{nc},3f_{nc},}^{\infty} C_n[\cos((n-1)\omega_o t - \frac{n\pi}{2} - \phi_1) -$$

$$- \cos((n+1)\omega_o t - \frac{n\pi}{2} + \phi_1)] \tag{5.31}$$

Eqn. (5.31) clearly implies that the isolation transformer must be designed to operate at f_{nc} - 1 p.u. frequency without going into saturation.

Finally, the simulated waveforms with their respective spectra for current and voltage quantities, $I_s(\omega t)$ and $V_p(\omega t)$, are shown in Fig. 5.4. These waveforms have been obtained by incorporating the expressions (5.30) and (5.31) in the computer program discussed in appendix A.

5.4 Simulated waveforms obtained in the AC to DC mode

In this section the simulated waveforms of voltage and current quantities of interest are presented when the converter operates in the AC to DC mode.

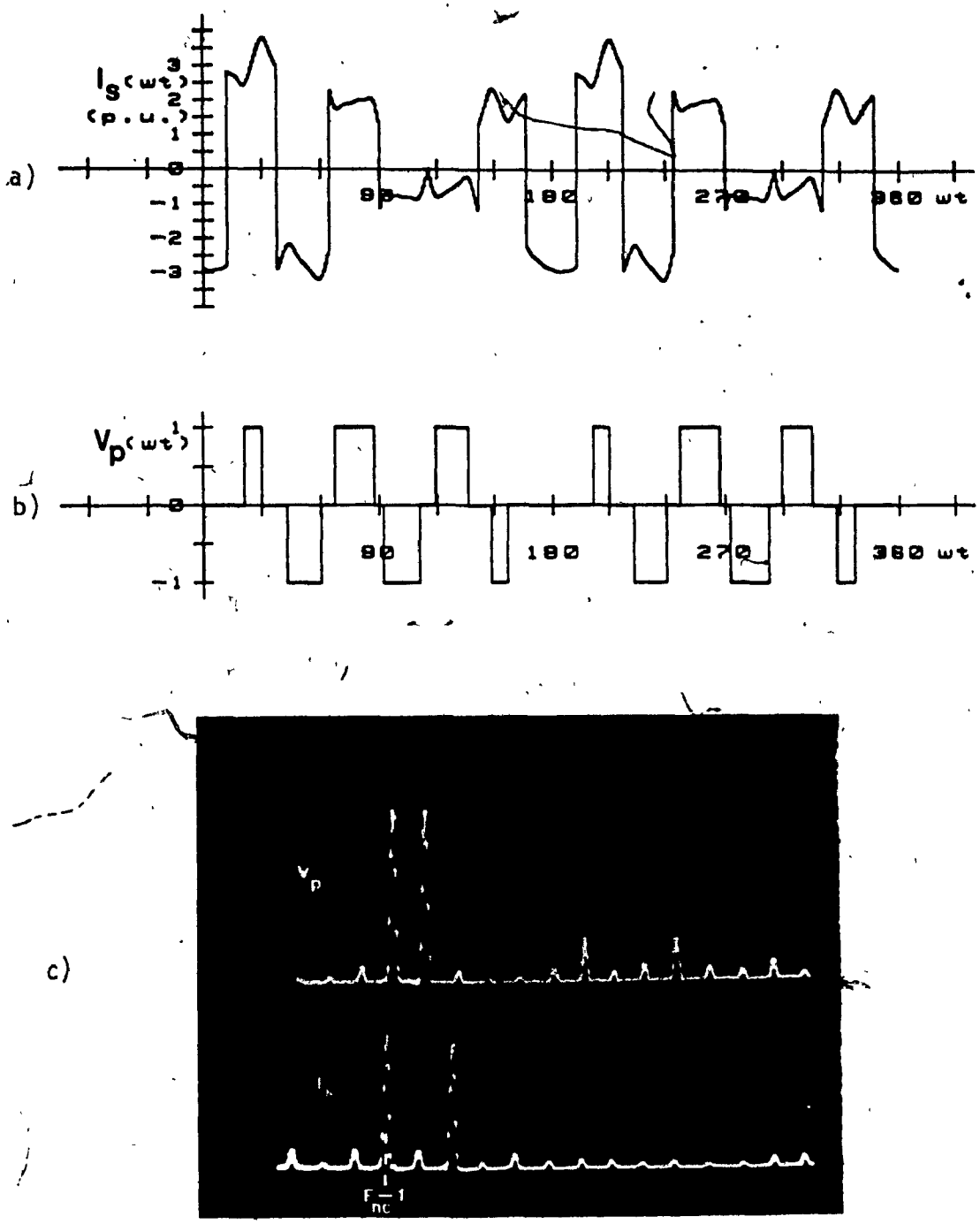


Fig. 5.4: Simulated waveforms of the Isolation Transformer

a) Secondary current, $I_s(\omega t)$

b) Primary voltage, $V_p(\omega t)$

c) Frequency spectra of $I_s(t)$ and $V_p(\omega t)$

Fig. 5.5 shows the primary voltage of the isolation transformer, the inverter stage output voltage, and finally the converter input current. As it can be seen from Fig. 5.5 by using the existing reactive and magnetic components input and output waveforms with low harmonic distortion can be obtained.

5.5 Component ratings

Regarding Fig. 5.2 and assuming that $f_{nc} \geq 17$, the converter main component current and voltage ratings are given by

Inverter Stage

Peak switch current $I_{PS} = \sqrt{2}$ p.u. (5.32)

RMS switch current $I_{RS} = 1$ p.u. (5.33)

Average switch current $I_{AS} = \frac{2\sqrt{2}}{\pi} = 0.9$ p.u. (5.34)

Peak switch forward blocking voltage = $E_{max} = 2$ p.u. (5.35)

Cycloconverter Stage

Peak switch current $I_{PS} = \sqrt{2}$ p.u. (5.36)

RMS switch current $I_{RS} = 1$ p.u. (5.37)

Average switch current $I_{AS} = \frac{2\sqrt{2}}{\pi} = 0.9$ p.u. (5.38)

Peak switch forward blocking voltage = $E_{max} = 2$ p.u. (5.39)

5.6 Design Example

In order to illustrate the significance and facilitate the understanding of theoretical results obtained in previous sections the following example is given

E = Supply voltage = 48 V

$V_{o(rms)}$ = RMS load voltage = 115 V

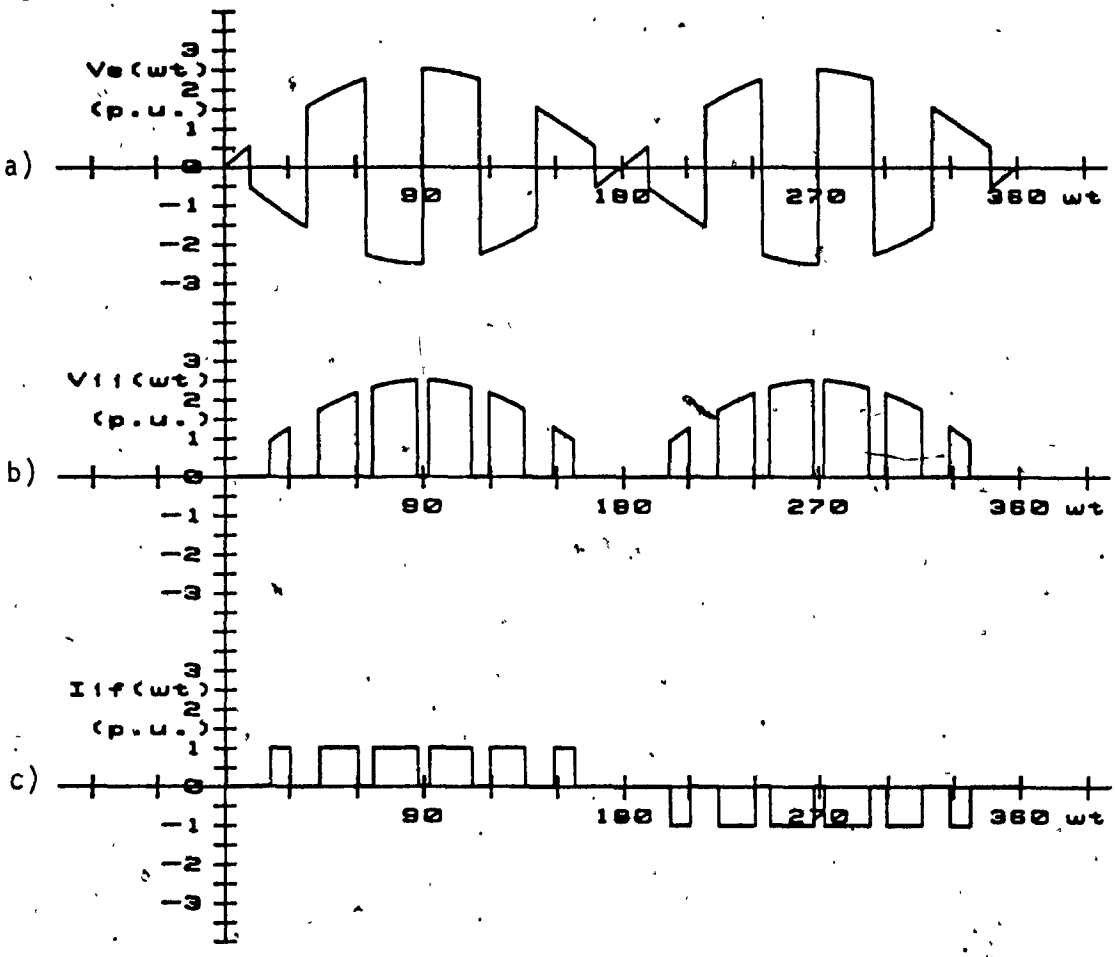


Fig. 5.5: Simulated waveforms obtained in the AC to DC mode.

a) Transformer secondary voltage, $V_s(\omega t)$

b) Inverter stage input voltage, $V_{ii}(\omega t)$

c) Current before output filtering, $I_{if}(\omega t)$

$I_{o(rms)}$ = RMS load current = 4A

f_o = converter output frequency = 60 Hz

f_{nc} = Normalized carrier frequency = 7

K_{i_f} = Input filter inductor current ripple factor = 0.2

K_{v_f} = Input filter capacitor voltage ripple factor = 0.01

THD $\leq$ 5%

From the above specifications the following p.u. values are obtained

1 p.u. volts = 115 V (E1)

1 p.u. current = 4 A (E2)

1 p.u. impedance = $\frac{115}{4}$ = 28.75 Ω (E3)

1 p.u. frequency = $2\pi f_o$ = 377 rad/sec (E4)

Using the above p.u. values and eqn. (5.18) the output filter parameters are obtained

$$L_o C_o = \frac{24}{(2\times 7-1)^2} = 0.14 \text{ p.u.} \quad \text{(E5)}$$

Choosing 0.5 p.u. capacitance,

C_o = 0.5 p.u. (E6)

L_o = 0.28 p.u. (E7)

$$X_{C_o} = \frac{1}{\omega_o C_o} = \frac{1}{0.5} = 2 \text{ p.u.} \quad \text{(E8)}$$

$X_{L_o} = \omega_o L_o$ = 0.28 p.u. (E9)

Therefore, the actual values of the output filter components are given by

$$C_o = \frac{1}{X_{C_o}\omega_o} = \frac{1}{2*28.7*377} = 46\ \mu F \qquad (E10)$$

$$L_o = \frac{X_{L_o}}{\omega_o} = \frac{0.28*28.7}{377} = 21.6\ mH \qquad (E11)$$

Using eqns. (5.21) and (5.22) the input filter component parameters are given by the system of equations

$$\frac{X_{L_{i,1}}}{X_{C_{i,1}}} = \frac{0.28}{0.2} + 0.2 = 1.6\ \text{p.u.} \qquad (E12)$$

$$\frac{X_{L_{i,1}} X_{C_{i,1}}}{4X_{L_{i,1}} - X_{C_{i,1}}} = 1.414(0.01) = 0.0141\ \text{p.u.} \qquad (E13)$$

Solving the system of eqns. (E12) and (E13) the p.u. and actual values of the input filter components are given by

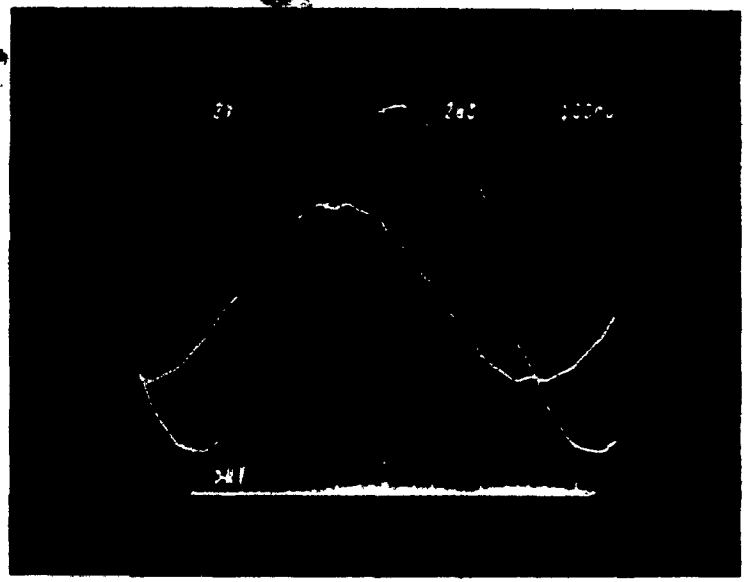
$$X_{C_{i,1}} = 0.0265\ \text{p.u.} \qquad (E14)$$

$$X_{L_{i,1}} = 0.042\ \text{p.u.} \qquad (E15)$$

$$C_i = \frac{1}{0.0265*28.7*377} = 3,488\ \mu F \qquad (E16)$$

$$L_i = \frac{0.042*28.7}{377} = 3.20\ mH \qquad (E17)$$

The current and voltage ratings of the converter main components can be obtained using exps. (5.32) - (5.39). Finally, a breadboard unit was implemented for this design example and the experimental results are depicted in Fig.5.6. Comparison between simulated and experimental results shows that they are in close agreement.



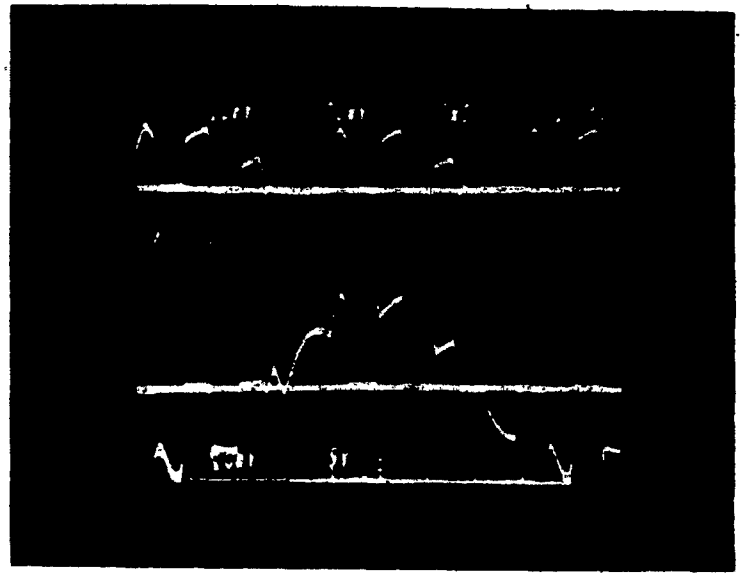


Fig. 5.6: Experimental results obtained with P_f=0.8 leading and f_{nc}=7.

a) Voltage and current waveforms before output filtering, $V_{if}(\omega t)$ and $I_{if}(\omega t)$

b) Top: Inverter stage switch current
Bottom: Cycloconverter switch current

c) Load voltage and current waveforms, $V_o(\omega t)$ and $I_o(\omega t)$

5.7 Conclusions

In this chapter a SPWM controlled bilateral HF link power conversion scheme was presented which provides bilateral high frequency transformer isolation between the source and the load. Analytical expressions have been subsequently derived to provide circuit design guidelines.

Finally, selected experimental results obtained from a 500 VA breadboard unit have been employed to verify respective predicted results.

CHAPTER 6

CONCLUSIONS

6.1 Conclusions

The performance of four novel Switch-Mode power conversion schemes utilizing an HF link as one of the two power conversion stages has been investigated. The employment of the HF link yield high power density for the proposed schemes at the cost of an additional power conversion stage, and/or the replacement of unidirectional power switching devices by bidirectional ones.

A voltage source DC to AC power conversion scheme using DC to DC converter as an HF link has been investigated. The guidelines for the design of the filters involved are discussed and expressions of the filter components are derived as a function of the normalized carrier frequency (f_{nc}), and the allowable voltage and current ripple factors (K_i, K_v). Simulated and experimental results have shown that the proposed power conversion scheme yields high operating efficiency, programmable output frequency and high power density. A family of transistorized schemes were presented for different output applications. When an extra power "leg" is inserted in the inverter stage, the proposed conversion scheme can be extended to three-phase output system.

A current source DC to AC power conversion scheme using DC to DC converter as an HF link has been investigated. The function of the HF link in this proposed power conversion scheme is twofold. First, it creates the current source which is applied to the DC to AC stage and second, together with a high frequency transformer, it provides

isolation between the source and the load. A brief discussion on the comparative advantages and disadvantages between Current Source Inverters (CSI) and Voltage Source Inverters (VSI) was presented. The proposed conversion scheme can be successfully used for AC machine drive applications when the isolation transformer is eliminated.

An AC to DC Switch-Mode Rectifier (SMR) scheme using a cycloconverter as an HF link was investigated. This proposed power conversion scheme exhibits controlled input power factor and low input THD by employing small sized filtering. Moreover, due to the reduction in the size of the isolation transformer and filter components, the scheme exhibits high power density.

A bilateral power conversion scheme using an HF link was investigated. The proposed power conversion scheme incorporates a battery charger into an Inverter by using the existing power circuit components. This power conversion scheme can be applied as an AC motor drive and on-board battery charger for Electric vehicles when it is extended to three-phase output system.

Finally, all four proposed power conversion schemes met the initial design objective of this thesis which was to obtain good quality input and output waveforms with the employment of small sized isolation transformer and reactive components.

REFERENCES

[1] Motorola Handbook on Linear/Switch-Mode Voltage Regulators, 1982.

[2] Onerud, K., and Wolpert, T., "Primary switched power supplies with Ferroresonant stabilization," IEEE Conference Publication, Intelec 81.

[3] Kataoka, T., Kazuhiro, M., and Miyairi, S., "A pulse-width controlled AC to DC converter to improve power factor and waveform of AC line current," IEEE Trans. Industry Applications, Vol. IA-15, No. 6, pp. 670-675, Nov./Dec. 1979.

[4] Chauprade, R., "Inverters for Uninterruptible Power Supplies", IEEE Trans. Industry Applications, Vol. IA-13, No. 4, pp. 281-297, July/Aug. 1977.

[5] Severns, R., "The design of Switchmode converters above 100 KHz, "Application Bulletin A034, INTERSIL INC., 1980.

[6] Schwarz, F.C., "A method of resonant current pulse modulation for power converters", IEEE Trans. Industrial Electronics and Control Instrumentation, Vol. IECI-17, No. 3, pp. 209-221, May 1970.

[7] McMurray, W., "The thyristor electronic transformer. A power converter using a high frequency link," IEEE Trans. Industry and General Applications, Vol. IGA-7, No. 4, pp. 451-457, July/Aug. 1977.

[8] Gyugyi, L., and Cibulka, F., "The high frequency base converter - A new approach to static high-power conversion," IEEE Trans. Industry Applications, Vol. IA-15, No. 4, pp. 420-429, July/Aug. 1979.

[9] Espelage, P.M., and Bose, B.K., "High frequency link power conversion," IEEE Trans. Industry Applications, Vol. IA-13, No. 5, pp. 387-394, Sep./Oct. 1977.

[10] Steigerwald, R.L., Ferraro, A., and Turnbull, F.G., "Application of power transistors to residential and intermediate rating photovoltaic array power conditioners," Conference Record, IEEE-IAS International Semiconductor Power Converter Conference, pp. 84-96, 1982.

[11] Steigerwald, R.L., and Tompkins, R.E., "A comparison of high frequency link schemes for interfacing a DC source to a utility grid," Conference Record, IEEE-IAS Annual meeting, pp. 759-766, 1982.

[12] Manias, S., and Ziogas, P.D., "A novel two stage DC to AC transistorized inverter," Canadian Elec. Engin. Journal, Vol. 8, No. 3, pp. 106-114, July 1983.

[13] Ziogas, P.D., "Synthesis of Optimum Gain Functions for Static Power Converters," IEEE Trans. Industry Applications, Vol. IA-19, No. 3, pp. 401-408, May/June 1983.

[14] Ziogas, P.D., and Photiadis, P.N., "An Exact Input Current Analysis of Ideal Static PWM Inverters," IEEE Trans. Industry Applications, Vol. IA-19, No. 2, March/April 1983.

[15] Ziogas, P.D., Manias, S., and Wiechmann, E., "Application of Current Source Inverters in UPS Systems," Conference Record, IEEE-IAS Annual Meeting, pp. 949-957, 1983.

[16] Patel, H.S., and Hoft, R.G., "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I

Harmonic Elimination," IEEE Trans. Industry Applications, Vol. IA-9, No. 3, pp. 310-317, May/June 1973.

[17] Dewan, S.B., and Ziogas, P.D., "Optimum Filter Design For a Single-Phase Solid-State UPS system," IEEE Trans. Industry Applications, Vol. IA-15, No. 6, pp. 664-667, Nov./Dec. 1979.

[18] Nayak, P.H., and Hoft, R.G., "Optimizing the PWM waveform of a Thyristor Inverter", Conference Record, IEEE-IAS Annual Meeting, pp. 1009-1013, 1974.

[19] Matsch, L.W., "Electromagnetic and Electromechanical Machines," New York, Harper and Row, 1977.

[20] Huatek, E.R., "Design of Solid-State Power Supplies," New York, Van Nostrand Reinhold, 1971.

[21] Presman, A.I., "Switching and linear Power Supply, Power Converter Design," Rochelle Park, New Jersey, Hayden, 1977.

[22] Lienau, W., Hellmann, A., and Skudelny, C.H., "Power Converters for Feeding Traction Motors of Single-phase AC Vehicles," IEEE Trans. Industry Application, Vol. IA-16, No. 1, pp. 103-110, Jan/Feb. 1980.

[23] Brennen, M.B., "A comparative analysis of two commutation circuits for adjustable current input inverters feeding induction motors," IEEE Power Electronic Specialist Conference, pp. 201-212, 1973.

[24] Philips, K.P., "Current Source Converter for AC Motor Drives," IEEE Trans. Industry Applications, Vol. IA-8, No. 6, pp. 679-683, Nov./Dec., 1972.

[25] Kamm, E., "Design guide for Electromagnetic Interference (EMI) reduction in Power Supplies," MIL-HDBK-241B, USA Naval Electronic Systems command.

[26] Waller, P.H., "Forward converter operating directly off the three-phase rectified mains suitable for exchange use," IEE Conference Publication, Intelec 81.

[27] Rosenberg, S.A., Kotlarewsky, P., and Estabrooks, J.R., "A new family of Switched Mode Rectifiers," IEE Conference publication, Intelec 81.

[28] Kocher, M.J. and Steigerwald, R.L., "An AC to DC Converter with high quality input waveforms," IEEE Power Electronic Specialist Conference, pp. 63-75, 1982.

[29] Brewster, R.F., and Barret, A.H., "Three-phase AC to DC voltage converter with power line harmonic current reduction," U.S. Patent 4,143,414, March 6,1979.

[30] Gallios, G.C., "An enhanced technique for reduction of off line converter input harmonics," Proceedings of Powercon 11, 1984, F-2, page 1 to F-2 page 9.

[31] Smollinger, G.J., and Raddi, W.J., "Reverse energy transfer through an AC line synchronized Pulse Width Modulated Sinewave Inverter, IEE conference publication, Intelec 81, pp. 126-131.

[32] Raddi, W.J., and Johnson, R.W., "A utility interactive PWM sine-wave Inverter configured as a high efficiency UPS," IEEE Power Electronic Specialist Conference, 1982.

[33] Dewan, S.B. and Caseres, J., "An input current-commutated three-phase PWM inverter," IEEE Trans. Industry Applications, Vol. IA-16, No. 3, pp. 445-451, May/June, 1980.

[34] Martenez, S., and Aldana, F., "Current-Source Double DC-side Forced commutated Inverter," IEEE Trans. Industry Applications, Vol. IA-14, No. 6, Nov./Dec. 1978.

[35] Manias, S., and Ziogas, P.D., "A novel current Impulse commutation circuit for thyristor inverters," IEEE Trans. Industry Applications, Vol. IA-19, No. 2, pp. 244-249, March/April 1983.

[36] McMurray, W., "SCR Inverter Commutated by an Auxiliary Impulse," IEEE Trans. Communication Electronics, Vol. CE-83, pp. 824-830, 1964.

[37] Dewan, S.B., Power Semiconductor Circuits, Wiley-Interscience, 1975.

[38] Pitel, I.J., Talukdar, S.N., and Wood, P., "Characterization of Programmed-Waveform Pulse width Modulation," IEEE Trans. Industry Applications, Vol. IA-16, No. 5, pp. 707-715, Sept./Oct., 1980.

APPENDIX A

COMPUTER AIDED ANALYSIS METHOD

Since a large number of computations are required for the plotting of voltage and current waveforms (observed at various points of the power conversion system) digital computer programs are employed to perform this task. All these programs share a common algorithm which consists of the following steps:

i) The specified normalized carrier frequency (f_{nc}), Modulation factor (M_f) and load power factor (P_f) are read into the program.

ii) From these values (step i) the intersections between the carrier and reference waveforms (which define in case of an inverter the inverter output voltage waveform before filtering and in case of a Rectifier the Rectifier input line current) are found using the Newton-Raphson method. From these intersection points and using Standard Fourier analysis techniques, the harmonic components ($V_{if,n}$) of the power conversion scheme output voltage (V_{if}) are computed and stored.

iii) Having the voltage before output filtering calculated in (ii) the output filter components are computed and stored insuring a $T\cdot H\cdot D \leq 5\%$.

iv) From the values of the output filter components (found in step (iii)) the complex values of the transfer function (H_n) and the input impedance ($Z_{o,n}$) of the output filter (as "seen"

by each voltage harmonic $V_{if,n}$) are computed and stored.

v) The complex values of the load filter input current harmonics ($I_{if,n}$) and load voltage harmonics ($V_{o,n}$) are computed and stored from equations; $I_{if,n} = V_{if,n}/Z_o$ and $V_{o,n} = V_{if,n} \cdot H_n$, respectively. The harmonic components of other currents or voltages (e.g. the current through the filter capacitor) are found in the same manner.

vi) The desired waveform is plotted from a set of computed waveform points. The computation of these points is performed by evaluating all harmonics at each point and then adding all harmonic values.

vii) The desired peak, rms, average or THD values for any current or voltage waveform are computed from the values of the harmonic components of the same waveform.

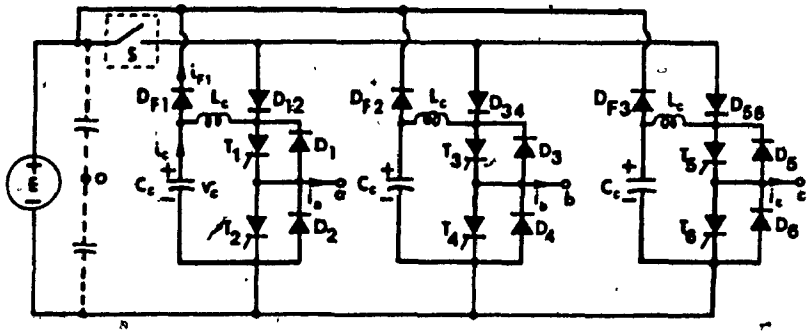
APPENDIX B

ANALYSIS OF A NOVEL CURRENT IMPULSE COMMUTATED THYRISTOR INVERTER

B.1 CIRCUIT DESCRIPTION

The configuration of a three-phase inverter with the proposed commutation circuit is shown in fig. B.1. The commutation scheme utilizes a static switch S whose function is to isolate the dc. bus from the inverter during each commutation interval. With S open current through any of the six thyristors is commutated by firing its respective complementary thyristor. Thus to commutate current through thyristor T_1 (fig. B.1) thyristor T_2 is turned on. This action initiates the flow of an oscillatory current i_c, through circuit L_c - C_c - T_1 - T_2. Current i_c eventually reverses polarity and begins to displace the load current from T_1. A few microseconds later current through T_1 and T_2 decreases to zero with the excess i_c current flowing through diodes D_1, D_2. During the D_1, D_2 conduction interval thyristors T_1 and T_2 become reverse biased, recover their forward blocking capability and they are ready for the next conduction interval.

The function of diodes D_{12}, D_{34}, D_{56} (fig. B.1) is to prevent interaction between the main thyristors of one inverter 'leg' and the L_c - C_c components of the other two legs. Consequently the flow of commutation currents is restricted within the circuits of their respective inverter 'legs'. This eliminates the problem of equal (commutation) current sharing between the three inverter 'legs'.



POSSIBLE SWITCH 'S' REALIZATIONS

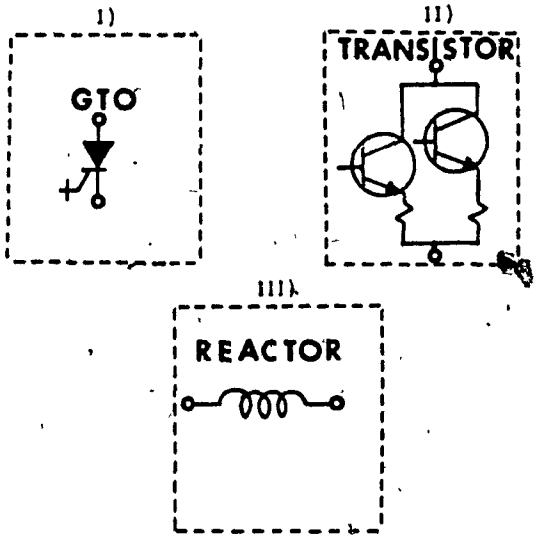


Fig. B.1: Circuit configuration of the proposed three-phase inverter.

The presence of diodes D_{12}, D_{34}, D_{56}, however, prevents the flow of regenerative current from the load to the dc source. To eliminate this problem feedback diodes D_{F1}, D_{F2}, and D_{F3} are introduced as shown in fig. B.1.

Further examination of the inverter configuration reveals that half of redundant commutations cannot occur with the proposed commutation scheme. The reason is that if an antiparallel diode is conducting (e.g. D_1 instead of T_1) when the respective complementary thyrsitor (e.g. T_2) is turned on commutation current i_c cannot flow. This is an important circuit feature since it reduces commutation losses and improves overal efficiency.

Another intrinsic feature of the proposed circuit is that it has "instantaneous" current limit capability. This means that if the load current exceeds a prescribed value all six inverter thyristors can be turned-off simultaneously, forcing the load current to decrease by flowing through the feedback diodes and against the positive potential of the dc bus. To enter this mode of operation the gating signal to switch S is first removed and all six thyristors are subsequently gated only once.

This mode of operation is essential for providing overcurrent protection especially in active load applications such as motor drives.

Discussion: Fig. B.1 suggests that the inverter circuit could be considerably simplified if all six diodes: D_{F1}, D_{F2}, D_{F3}, D_{12}, D_{34}, D_{56} are eliminated and the three L_c - C_c commutation circuits are

replaced by a single $L_c - C_c$ circuit with a thyristor switch, shared by all three inverter 'legs'. This option, known as the 'dc side commutation' [33], [34], is not favored here for the following reasons:

(i) The shared $L_c - C_c$ circuit must have three times the current commutation capability of each of the proposed three independent ones.

(ii) In order to commutate a single thyristor all six inverter thyristors must be commutated. This requirement creates the problem of equal current sharing among the three inverter 'legs'.

(iii) To ensure equal current sharing additional reactive components must be introduced into the inverter ciruit.

Fig.B.1 also shows that switch S is realized with one or more gate turn-off devices such as power transistors (or GTOs). The reason for this choice is that the switching frequency of S is six times the frequency of an individual thyristor. Such realization however, suggests that it might also be preferable to implement the three phase inverter with only six S type switches. This suggestion is rejected here for the following reasons:

(i) In order to match thyristor current and voltage ratings, more than one gate turn-off device may have to be connected in parallel and/or in series. Such arrangements increase the cost and decrease the reliability of the overal system.

(ii) It is very likely that for high power applications the cost and complexity of two or more base drives for bi-polar transistors or GTOs will exceed the cost and complexity of a single L_c - C_c circuit shared by two thyristors. This is mainly because of the relatively low gain of the gate turn-off devices (excluding power FETs).

(iii) Inverter isolation switches, such as S, (fig. B.1) are frequently employed even with all transistor inverters to improve system reliability.

B.2 CIRCUIT ANALYSIS AND DESIGN

In this section the circuit, fig. B.1, for the proposed commutation scheme is analyzed. The analysis yields a set of design equations that specify the size and the voltage and current ratings of circuit components in terms of the:

(i) input dc voltage

(ii) peak load current I_o

(iii) thyristor turn-off time t_{off}.

Moreover the analysis which is supported by reference [35], is performed with the following assumptions:

(i) the dc supply voltage is ripple free

(ii) the load current remains constant during a given commutation interval

(iii) power switches and filter components are ideal.

B.2.1 Circuit Analysis

Consider that thyristor T_2, fig.B.1, has been conducting load current I_o for some time and it is about to be commutated.

At t = 0 sec., when it is assumed that the commutation interval for T_2 begins, commutation capacitor C_c is charged to dc source voltage E and $i_c = 0$. Moreover, at $t = 0^-$ switch S has been turned off and at t = 0 thyristor T_1 is turned on. The ensuing circuit operation can be divided into the four modes of operation shown in fig. B.3.

Mode I begins at t = 0, when thyristor T_1 is turned on. The initial conditions for this mode of operation are:

$$\text{Capacitor } C_c \text{ voltage } V_{co} = E \text{ Volts}$$
$$\text{Capacitor } C_c \text{ current } I_{co} = 0 \text{ Amps.} \qquad (B1)$$

At $t = 0^+$ the oscillatory current i_c (fig. B.3) begins to flow through components $C_c - L_c - T_1 - T_2$ whose equivalent circuit representation is shown in fig. B.2. Since commutation circuits are designed for the highest possible quality factor Q they can be treated as highly underdamped R-L-C circuits. Therefore, from eqns. (B1) and fig. B.2);

$$i_c(t) \simeq \left(\frac{E\, e^{-\frac{\omega t}{2Q}}}{X}\right)\sin(\omega t) \qquad (B2)$$

$$v_c(t) \simeq \left(E\, e^{-\frac{\omega t}{2Q}}\right)\cos(\omega t) \qquad (B3)$$

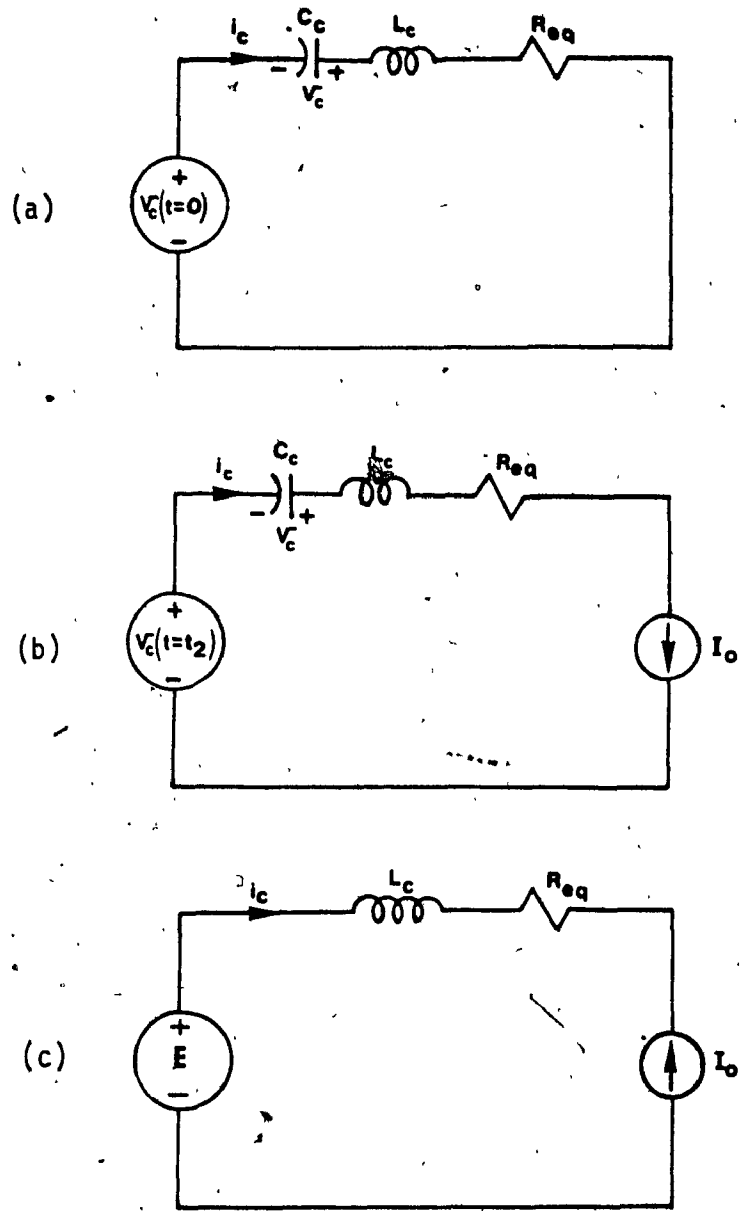


Fig. B.2: Equivalent circuit representation for commutation circuit during commutation intervals.

a) Modes I and II
b) Mode III
c) Mode IV

Where: i_c is the commutation current

v_c is the voltage across the commutation capacitor C_c.

$$\omega^2 = \frac{1}{L_c C_c}$$

$$X = \omega L_c = \left(\frac{L_c}{C_c}\right)^{1/2} \qquad \text{(B4)}$$

$$Q = \frac{X}{R_{eq}}$$

and,

R_{eq} is the sum of the ohmic and equivalent ohmic resistances of the passive and active components respectively, which comprise the i_c path.

As shown in fig. B.3 oscillatory current i_c reverses polarity at $t = \pi/\omega$ and begins to displace load current I_o from thyristor T_2.

Mode I ends when $i_c(t) = I_o$, at which point T_2 stops conducting. In fig. B.3 this is shown to occur at $t = \frac{\pi}{\omega} + t_1$ secs.

Therefore:

$$I_o = i_c\left(\frac{\pi}{\omega} + t_1\right) = -\frac{E\, e^{-\frac{\omega t_1 + \pi}{2Q}}}{X} \sin(\omega t_1 + \pi) = \frac{E\, e^{-\frac{\omega t_1 + \pi}{2Q}}}{X} \sin(\omega t_1) \qquad \text{(B5)}$$

Also from fig. B.3:

$$e^{-\frac{\omega t_1 + \pi}{2Q}} \simeq e^{-\frac{3\pi}{4Q}}.$$

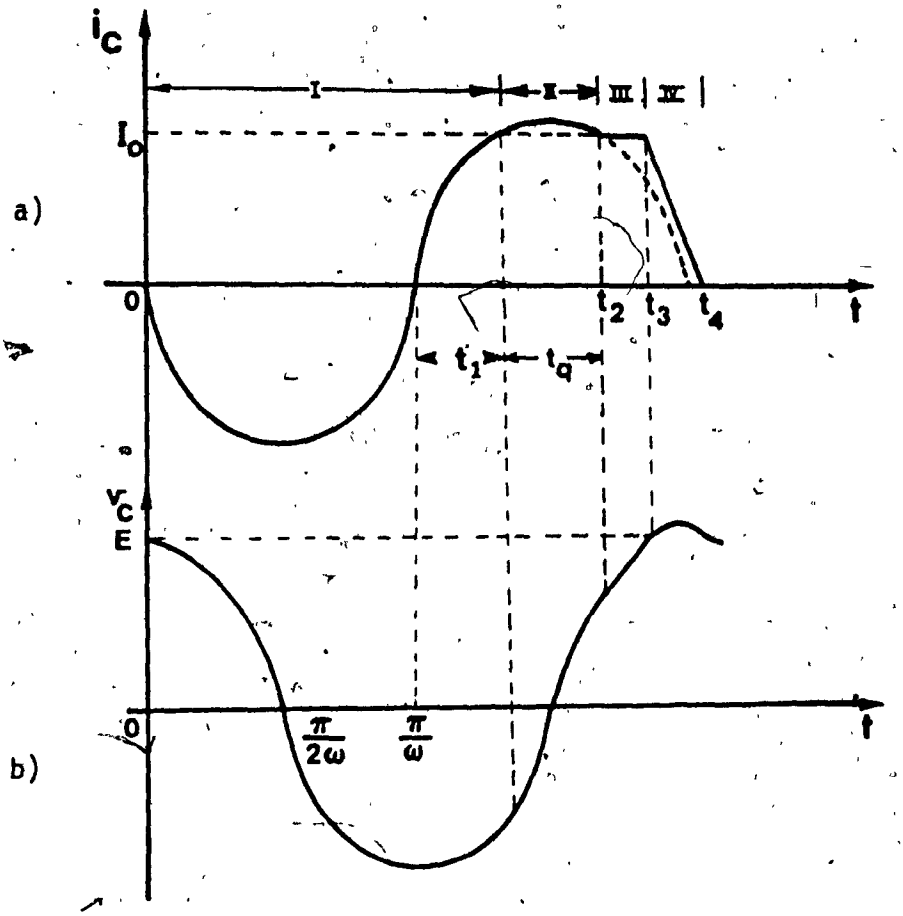


Fig. B.3: Commutation current i_c and voltage v_c waveforms illustrating various modes of operation for one commutation interval.

Therefore:

$$t_1 \simeq \frac{1}{\omega} \sin^{-1}\left(\frac{I_o \times e^{+\frac{3\pi}{4Q}}}{E}\right) \qquad (B6)$$

or;

$$t_1 \simeq \frac{1}{\omega} \sin^{-1}(\rho) \qquad (B7)$$

where:

$$\rho = \frac{I_o}{\hat{I}_c} \qquad (B8)$$

and:

$$\hat{I}_c = \frac{E}{X} e^{-\frac{3\pi}{4Q}} \qquad (B9)$$

is the positive peak value of the commutation current $i_c(t)$.

Mode II begins when commutation current i_c exceeds load current I_o. During this mode diodes D_1 and D_2 conduct currents i_c and $\Delta i_c = i_c - I_o$ respectively, as shown in fig. B.3. This action impresses a reverse bias voltage equal to a diode drop across each of T_1 and T_2 thyristors initiating the respective turn-off interval t_q for T_2.

With reference to fig. B.3, t_q can be found from;

$$\omega t_q \simeq \pi - 2(\omega t_1)$$

$$\therefore t_q = \frac{\pi}{\omega} - 2t_1$$

$$= \frac{1}{\omega}\left[\pi - 2 \sin^{-1}(\rho)\right] \qquad (B10)$$

where:

ρ, eqn. (B8), is the ratio of load current I_o to peak commutation current $\hat{I}_c$ and it is typically employed as an independent design parameter.

Mode II ends the moment $i_c(t)$ falls below I_o at which point diode D_1 ceases conduction.

Mode III is a constant current mode, fig. B.2.b, with load current I_o flowing through components $D_1 - L_c - C_c$. The reason for which I_o flows into C_c instead of through D_{F1} is that;

$$v_c(t = t_2) = (E\, e^{-\frac{\omega t_2+\pi}{2Q}}) \cos(\omega t_2+\pi) < E \qquad (B11)$$

and diode D_{F1} is reversed biased.

During this mode C_c charges with constant current (i.e. $i_c = I_o$) until $v_c = E$ Volts, at which point mode III ends. The duration of this mode can be calculated from the initial $v_c = v_{ci}$ and final $v_c = E$ capacitor voltages and the capacitor current $i_c = I_o$, as follows;

$$t_3 - t_2 = C_c \frac{E - v_{ci}}{I_o} \qquad (B12)$$

where;

$$v_{ci} = v_c(t_2) = (E\, e^{-\frac{\omega t_2+\pi}{2Q}})\cos(\omega t_2+\pi) \qquad (B13)$$

and;

$$t_2 = t_1 + t_q = \frac{1}{\omega}[\pi - 2\sin^{-1}(\rho)] + \frac{1}{\omega}\sin^{-1}(\rho)$$

$$= \frac{1}{\omega}[\pi - \sin^{-1}(\rho)] \qquad (B14)$$

Also, ρ can be computed from eqns. (B8) and (B9).

Mode IV begins when v_c rises slightly above E and diode D_{F1} becomes forward biased. As a result current i_ℓ stops flowing through C_c and begins to flow through D_{F1}. With C_c acting as an open circuit the energy stored in L_c at $t = t_3$, fig. B.3, is gradually being transferred to the dc source through the D_2 - D_1 - L_c - D_{F1} path.

The equivalent circuit for this mode of operation is shown in fig. B.2.c. Fig. B.2.c yields;

$$i_\ell(t') = i_\ell(t_3) - \frac{E}{L_c} t' \qquad \text{(B15)}$$

where;

$$t' = t - t_3$$

and from fig. B.3;

$$i_\ell(t_3) = I_o. \qquad \text{(B16)}$$

Since mode IV lasts until $i_\ell(t') = 0$, its duration is given by;

$$0 = I_o - \frac{E}{L_c}(t_4 - t_3)$$

$$\therefore \quad t_4 - t_3 = \frac{I_o L_c}{E} \text{ secs.} \qquad \text{(B17)}$$

It is noted that modes III and IV of the commutation interval just described are valid only when current through one of the three bottom thyristors (e.g. T_2, T_4, T_6, fig. B.1) is being commutated.

When current through one of the top three thyristors is being commutated modes III and IV do not exist. Instead the commutation current i_c follows the sinusoidal path indicated with a broken line in fig. B.3. Lack of mode III leaves capacitor C_c charged slightly below E volts at the end of such a commutation, as shown by eqn. (B18).

$$V_{cf} = E\, e^{-\frac{\pi}{Q}} \qquad \text{(B18)}$$

The final capacitor voltage v_{cf}, however, increases to E volts a few microseconds after switch S is closed again. It is finally noted that at the end of any commutation interval switch S is gated again and resumes its normal conduction function.

Discussion: The preceding analysis has demonstrated that the proposed commutation scheme has the following two unique features:

(i) The initial and final commutation capacitor voltage is equal to the dc supply voltage E.

(ii) Excess reactor, L_c, energy returns to the source at the end of the commutation interval.

These two features imply minimum voltage stresses across the semiconductor components and the elimination of energy dissipative resistors [36] from the circuit.

B.2.2 Aspects of Circuit Design:

B.2.2.1 Commutation Capacitors and Inductors:

A properly designed commutation circuit must ensure safe current commutation under worst load current conditions. Consequently, the turn-off interval t_q provided by the commutation circuit, with maximum expected load current, must be larger than the respective thyristor t_{off} time provided by the manufacturer's application notes. Therefore, from eqn. (B10);

$$t_q = \frac{1}{\omega}[\pi - \sin^{-1}(\rho)] = t_{off} + \Delta t \qquad (B19)$$

where:

Δt is the turn-off time safety margin.

Also, with initial C_c voltage equal to E volts and by following the design procedure outlined in reference [37], one can easily show that:

$$C_c = \frac{I_o(t_{off}+\Delta t)}{E_{min}\,\rho\,G(\rho)}\, e^{\frac{3\pi}{4Q}}, \quad \text{and} \tag{B20}$$

$$L_c = \frac{\rho E_{min}\,(t_{off}+\Delta t)}{I_o G(\rho)}\, e^{-\frac{3\pi}{4Q}} \tag{B21}$$

where;

$$G(\rho) = \omega t_q = \pi - 2\sin^{-1}(\rho) \tag{B22}$$

and,

E_{min} is the minimum anticipated dc bus voltage.

Moreover, since parameter Q is a function of C_c (eqn. (B4)), it might appear that eqns. (B20) and (B21) cannot be directly evaluated. However, since for typical cases $Q \geq 10$, eqns. (B20) and (B21) can be evaluated with Q = 10, which represents the worst circuit losses condition.

B.3.2-2 Main Switching Components:

With fixed load conditions, the peak and rms current values through the main switching components depend on the modulation scheme employed and the level of the input dc voltage. Therefore, exact current ratings can be determined only when such parameters have been specified.

In relative terms, however, it can be seen, fig. B.1, that the peak current value I_{PS} for switch S is equal to the peak load

current value. Also, it can be easily shown that the respective rms current value I_{RS} is $\sqrt{2}$ times the value of one of the three line currents. Finally, the average current value I_{AS} through switch S can be computed from;

$$I_{AS} = \frac{P_{out(max)}}{\eta \times E_{min}} \qquad (B23)$$

where

$P_{out(max)}$ is the maximum expected real output power

η is the inverter efficiency

and

E_{min} is the minimum expected value of the dc bus voltage.

Similarly, the peak; I_{PT} rms; I_{RT} and average; I_{AT} current values for the six thyristors are related to the respective switch S values as follows;

$$I_{PT} = I_{PS} + E_{max}\sqrt{\frac{C_c}{L_c}}$$

$$I_{RT} = \frac{I_{RS}}{2} \qquad (B24)$$

and

$$I_{AT} = \frac{I_{AS}}{3}$$

It is noted that the $E_{max}\sqrt{C_c/L_c}$ term, in the expression for the thyristor peak current, accounts for the commutation current that also flows through the main thyristors. However, commutation current pulses last for only several microseconds and thyristors can transiently tolerate very high pulse currents. Therefore, this

extra term causes no significant current derating to the respective devices.

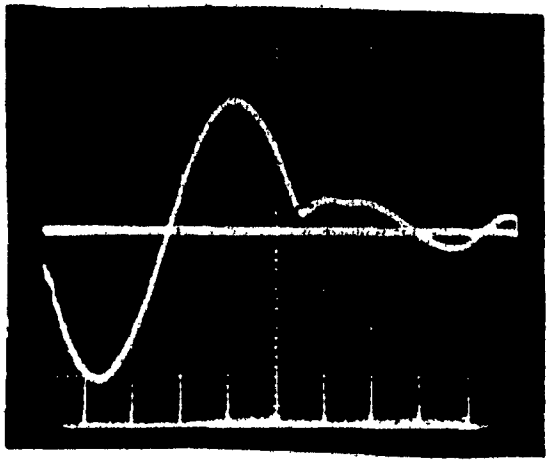
B.3 Experimental Results:

To demonstrate the feasibility of the proposed commutation scheme and verify selected predicted results, an experimental 3 kVA inverter has been implemented. Results obtained with this inverter are depicted in figs. B.4 and B.5.

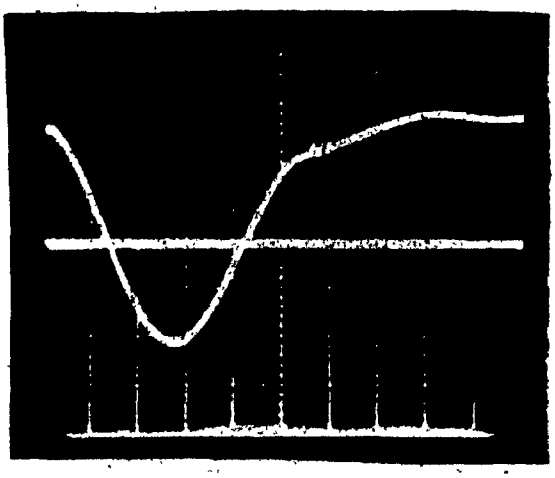
Fig. B.4 illustrates, on various time scales, the voltage and current waveforms of the commutation capacitor C_c. It also shows distinctly the four modes of operation that occur within a commutation interval, as predicted in section B.2 and depicted in fig. B.3. Comparison between predicted and experimental results show that they are in close agreement except for the 'ringing' observed at the end of the commutation interval. This 'ringing' is caused by the stray lead inductances connected in series with C_c and not taken into consideration in the circuit analysis presented in section B.2. Further experimental results are depicted in fig. B.5. In particular, fig. B.5(a) illustrates the waveforms of one of the three line to centre-tap (imaginary, fig. B.1) neutral voltages V_{ao} and its respective line current i_a with R-L load. In fig. B.5(b) the line to neutral voltage has been replaced by its respective line to line voltage.

Moreover the pulse width modulation (PWM) technique depicted in fig. B.5 is the sine PWM. This choice demonstrates the compatability of the proposed commutation scheme with modulation techniques of any complexity.

a)



b)



a,b)

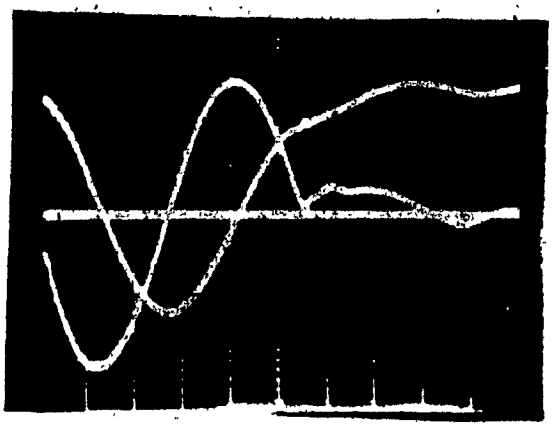
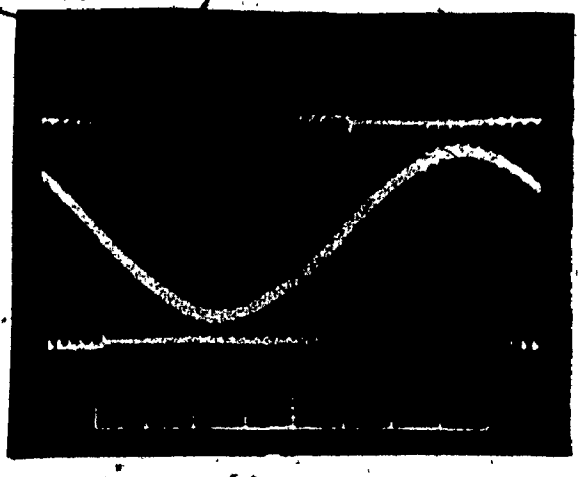


Fig. B.4: Experimental waveforms.

(a) Commutation current i_c. (Vertical scale: 20 A/div. Horizontal scale: 10 µs/ds.)

(b) Voltage v_c. (Vertical scale: 50 V/div. Horizontal scale: 10 µs/div.)

a)



b)

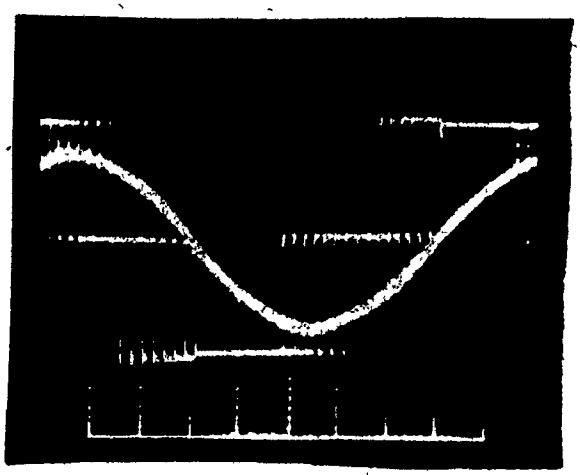


Fig. B.5: Experimental load voltage and current waveforms with delta connected R-L Load.

(a) Line to (fictitious) neutral voltage V_{aO} (Fig. 1) and line current i_a waveforms. Vertical scales: 50 V/div and 10 A/div. Horizontal scale: 2.5 ms/div.

(b) Line to line voltage V_{ab} (Fig. 1) and line current waveforms. Vertical scales: 50 V/div and 10 A/div. Horizontal scales: 2.5 ms/div.

APPENDIX C

USEFULL DEFINITIONS

Total Harmonic Distortion (THD)

The THD is a measure of the closeness in shape between a waveform and its fundamental harmonic. The mathematical definition of THD is

$$THD\% = \frac{100}{V_{x,1}} \left[\sum_{n=2}^{\infty} (V_{x,n})^2 \right]^{1/2}$$

where,

$V_{x,n}$ is the RMS value of the nth harmonic component of an arbitrary waveform V_x,

$V_{x,1}$ is the RMS value of the fundamental component of the waveform V_x,

n is the order of the harmonic component.

Distortion factor (D_f)

The distortion factor, D_f, indicates the amount of harmonic distortion that remains in a particular voltage or current waveform, after the harmonics of that waveform have been subjected to a second-order attenuation (i.e. divided by n^2). Thus, the effectiveness of a particular PWM technique, in reducing unwanted harmonics, can be evaluated without having to specify the values of the (second-order) load filter. The distortion factor mathematically is given by

$$D_f\% = \frac{100}{V_{x,1}}\left[\sum_{n=2}^{\infty}\left(\frac{V_{x,n}}{n^2}\right)^2\right]^{1/2}$$

Ripple Factor

The pulsations, or ripple, caused by the harmonic components in the AC to DC converter output or in the input of a DC to AC inverter are very undesirable in the supply to most electronic equipment. The amount of ripple, compared with the direct component is a measure of purity and is called the ripple factor. The ripple factor is given by

$$\text{Ripple factor} = \frac{\left[\sum_{n=1}^{\infty} V_{x,n(rms)}^2\right]^{1/2}}{V_{x,o}}$$

where,

$V_{x,o}$ is the dc component of the waveform V_x.

Half-wave symmetry:

If a function f(t) is periodic with period T, then the periodic function f(t) is said to have half-wave symmetry when it satisfies the condition

$$f(t) = -f(t + \frac{T}{2})$$

Any periodic function f(t) which has half-wave symmetry contains only odd harmonic components.

Quarter-wave symmetry:

If a function f(t) is periodic with period T, then is said to have Quarter-wave symmetry when f(t) has half-wave symmetry and, in addition, is either an even or odd function.

Symmetry Conditions for periodic waveforms and Fourier Coefficients

Type of Symmetry	Conditions	Form of the Fourier Series	Formulas for the Fourier Coefficients
Even	$f(t) = f(-t)$	$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega_0 t$	$a_n = \frac{4}{T}\int_0^{T/2} f(t)\cos(n\omega_0 t)\,dt$
Odd	$f(t) = -f(-t)$	$f(t) = \sum_{n=1}^{\infty} b_n \sin n\omega_0 t$	$b_n = \frac{4}{T}\int_0^{T/2} f(t)\sin(n\omega_0 t)\,dt$
Half-wave	$f(t) = -f\left(t + \frac{T}{2}\right)$	$f(t) = \sum_{n=1}^{\infty} [a_{2n-1}\cos(2n-1)\omega_0 t + b_{2n-1}\sin(2n-1)\omega_0 t]$	$\begin{matrix} a_{2n-1} \\ b_{2n-1} \end{matrix} = \frac{4}{T}\int_0^{T/2} f(t)\begin{Bmatrix}\cos \\ \sin\end{Bmatrix}[(2n-1)\omega_0 t]\,dt$
Even quarter-wave	$f(t) = f(-t)$ and $f(t) = -f\left(t + \frac{T}{2}\right)$	$f(t) = \sum_{n=1}^{\infty} a_{2n-1}\cos(2n-1)\omega_0 t$	$a_{2n-1} = \frac{8}{T}\int_0^{T/4} f(t)\cos[(2n-1)\omega_0 t]\,dt$
Odd quarter-wave	$f(t) = -f(-t)$ and $f(t) = -f\left(t + \frac{T}{2}\right)$	$f(t) = \sum_{n=1}^{\infty} b_{2n-1}\sin(2n-1)\omega_0 t$	$b_{2n-1} = \frac{8}{T}\int_0^{T/4} f(t)\sin[(2n-1)\omega_0 t]\,dt$

Dominant harmonic component

Given a specific frequency spectrum of an arbitrary waveform the dominant harmonic component (d) is the component that contributes maximum individual distortion factor. The distortion factor of an individual harmonic component is given by

$$d_n\% = 100\ \frac{V_{x,n}}{n^2}$$

Lowest significant harmonic component

In a frequency spectrum the harmonic component, which is nearest to the fundamental component, and its amplitude is greater than or equal to 3% of the fundamental component is called the lowest significant harmonic component.

KVA rating of the filter components

The KVA ratings of the filter components are given by

$$\text{Inductor Rating} = I \cdot R = \sum_{n=1}^{\infty} |I_{x,n}|^2 \cdot X_{L_n}$$

$$\text{Capacitor Rating} = C \cdot R = \sum_{n=1}^{\infty} \frac{|I_{x,n}|^2}{X_{C_n}}$$

where,

$I_{x,n}$ is the RMS value of the filter inductor nth current harmonic component,

X_{L_n} is the reactance of the filter inductor at the nth harmonic frequency,

X_{C_n} is the reactance of the filter capacitor at the nth harmonic frequency.

APPENDIX D

SWITCHING FUNCTIONS

Most AC to DC and DC to AC power conversion schemes fall into one of the following two categories:

a) Voltage Source, in which the input DC bus is made to appear like a voltage source to the power conversion scheme.

b) Current Source, in which the input DC bus is made to appear like a current source to the power conversion scheme.

For either category a general model can be formulated [38] that provides relationships between the input and output port variables of the conversion scheme by ignoring the specific circuit topology. Such a model is shown in Fig. D.1.

Regarding Fig. D.1 the input and output port variables for the two power conversion categories are related as follows:

a) Voltage Source

$$E = V_2(0) \tag{D1}$$

$$V_{ac} = I_1(\omega t) \tag{D2}$$

$$I_2(\omega t) = S(\omega t) \cdot I_1(\omega t) \tag{D3}$$

$$V_1(\omega t) = S(\omega t) \cdot E \tag{D4}$$

b) Current Source

$$E = I_2(0) \tag{D5}$$

$$V_{ac}(\omega t) = V_1(\omega t) \tag{D6}$$

$$I_1(\omega t) = S(\omega t) \cdot E \tag{D7}$$

$$V_2(\omega t) = S(\omega t) \cdot V_{ac}(\omega t) \tag{D8}$$

Where $S(\omega t)$ is a function that describes the switching operations of the power switches S_1 through S_4. This function is given by

$$S(\omega t) = \frac{V_2(\omega t)}{V_1(\omega t)} = - \frac{I_2(\omega t)}{I_1(\omega t)} \qquad (D9)$$

and is allowed to assume the states +1, 0 and -1. Therefore, with the aid of switching functions waveform synthesis can be achieved. By proper selection of switching functions any number of low-order harmonic components (unwanted components) can be eliminated from the input or output port variables of the power conversion scheme. Fig. D.2 shows an example of high frequency waveform synthesis for a DC to AC power conversion scheme. Multiplication of the inverter input voltage E (Fig. D.2(a)) with the selected switching function $S(\omega t)$ (Fig. D.2(b)) yields the output voltage waveform $V_o(\omega t)$ (Fig. D.2(c)). Moreover, from the switching function $S(\omega t)$ the gating signal waveforms for the power switching devices S_1 and S_2 can be obtained. For the half-bridge power conversion scheme application (Fig. D.2(a)) the upper half of $S(\omega t)$ defines the gating signal waveform of the upper switch S_1 and the lower half of $S(\omega t)$ defines the gating signal waveform of the lower switch S_2 (Figs. D.2(d) and (e)).

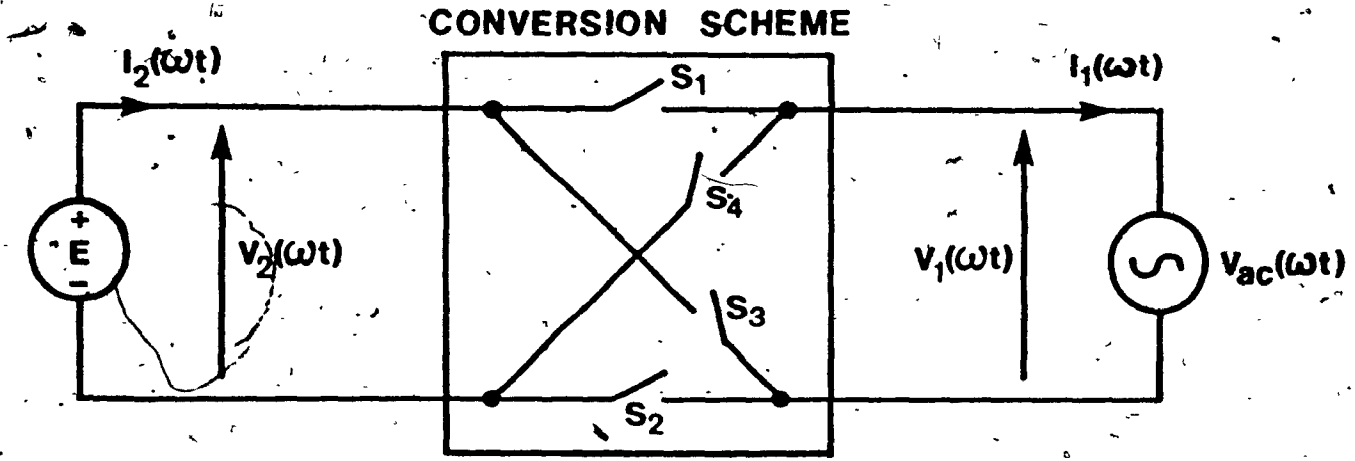


Fig. D.1: General converter model

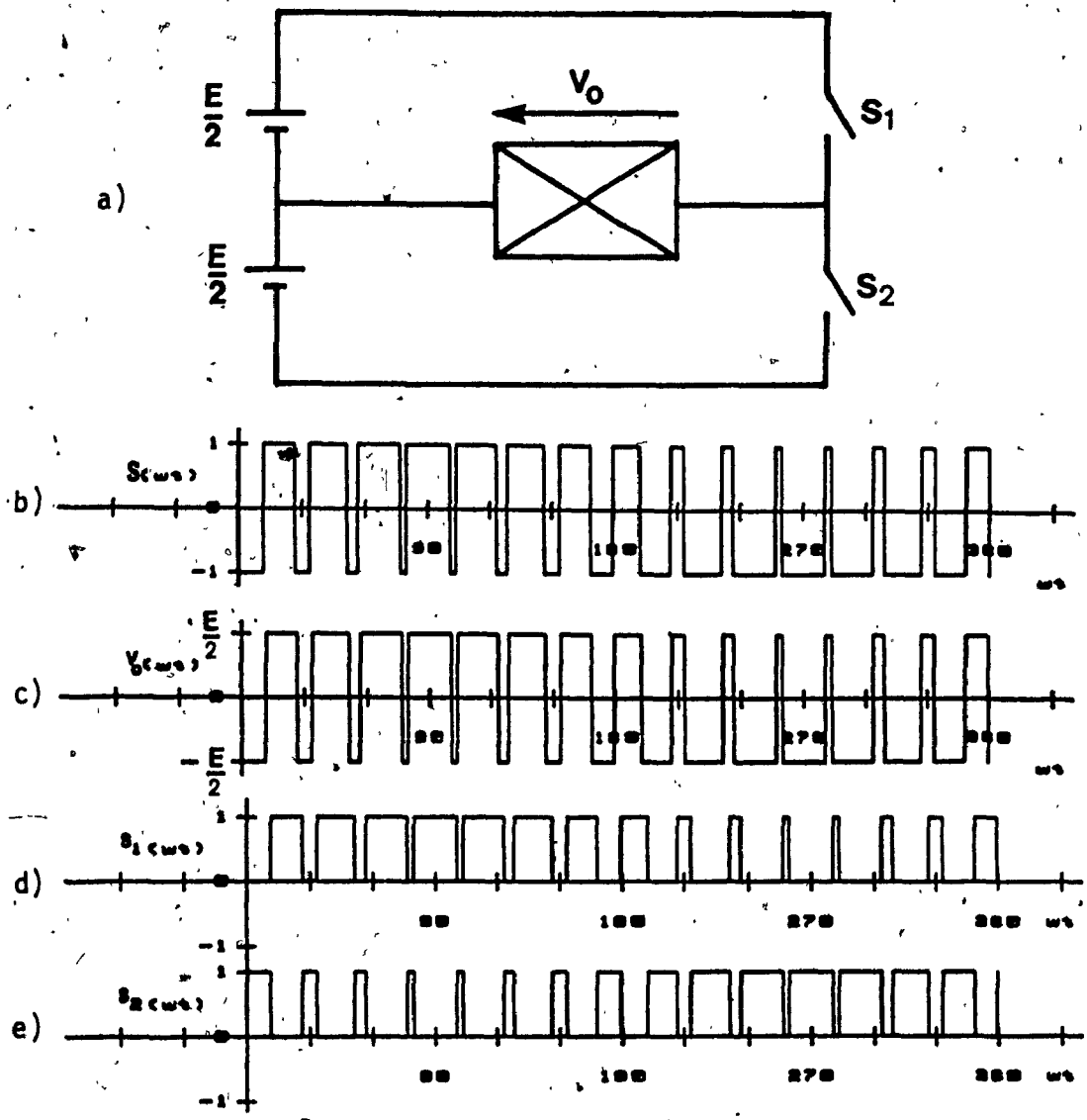


Fig. D.2: Example of high frequency waveform synthesis.

a) Half-bridge inverter
b) Half-bridge inverter switching function, $S(\omega t)$
c) Half-bridge inverter output voltage, V_o
d) Gating signal waveform employed to S_1
e) Gating signal waveform employed to S_2