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Supply Current Estimation in
CMOS VLSI Circuits

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A Thesis

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ABSTRACT

Supply Current Estimation

in CMOS VLSI Circuits

Fredj Rouatbi

A methodology for estimating supply current waveforms in CMOS VLSI circuits is presented. The method depends on a piece-wise linear current model, an analytical delay model and event driven simulation. Our approach differs from previous ones in that it takes into account circuit topologies, effect of nodes capacitances, input ramp effects and feed-through (short-circuit) current. Short and long channel MOSFETs are modeled. The model was tested for various circuits of different complexities and compared to SPICE level 3. We have achieved a much closer current estimates than previous models for event driven simulators. Our approach achieved a speed-up of 3 to 4 orders of magnitude as compared to SPICE. The simulated waveforms showed a worst case 5% difference on the average current and 10% difference on the peak current as that obtained by SPICE.

Acknowledgments

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Fredj Rouatbi

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CHAPTER 1

Introduction and Literature Review

Time-domain supply current waveforms are important tools in the design of integrated circuits. The transient current-density waveforms allow the designer to choose the Metal-lines width to avoid electromigration [22]. The peak current estimates are used to determine the worst case voltage drop across the power and ground busses [22-23]. The average current measures the heat dissipation of the circuit, and is used to determine the packaging of the chip. The instantaneous current identifies power intensive operations. However, the simulation of a complex CMOS circuit with a large number of transistors for current estimation is time consuming and the simulation time increases largely with the number of inputs. Different methods have been developed to reduce the simulation time and keep an acceptable accuracy.

a- Equivalent inverter method

An approach based on collapsing a CMOS gate into an equivalent inverter is presented in [1]. This approach deals with the peak current estimation in CMOS circuits. An algorithm for peak current estimation is presented. The algorithm deals with the problem at three levels of hierarchy, gate level, macro level and power/ground distribution level. A macro consists of a collection of gates having certain signals as primary inputs. A gate is collapsed into an *equivalent inverter* in order to determine the time domain supply current waveform. The procedure can be described as follows. Two parallel connected transistors with respective transconductances $\beta 1$, $\beta 2$ are replaced with a single transistor with an equivalent transconductance $\beta_{equ} = \beta_1 + \beta_2$. And two series-connected transistors will be replaced by a transistor with an equivalent transconductance $1/\beta_{equ} = 1/\beta_1 + 1/\beta_2$. The different internal node capacitances are lumped to the output node. The current waveforms in the equivalent inverter is determined using numerical analysis involving

solving differential equations with iteration. The maximum current in a CMOS macro depends on the transitions of the primary inputs. The estimation of the peak current in a CMOS macro by enumeration of all possible input transitions is computationally inefficient even for a small number of primary inputs. A branch-and-bound algorithm is used to estimate the peak current in a CMOS macro. Given a partially specified input state the algorithm defines an upper bound. The upper bound is the maximum current that can occur by specifying all the inputs. If the maximum current already determined for a totally specified input state is higher than the upper bound, the algorithm can stop the search at non-leaf nodes. The algorithm achieves computation saving of 2 orders of magnitude compared to SPICE. An algorithm estimating the maximum branch current in a power/ground distribution network using the macro maximum current is presented. This method will lead to an over estimation of the peak current, the peak current estimated can be 50% higher than SPICE estimates. This method can achieve good estimates of the peak current for circuits built from simple gates such as inverters, 2-input nand, 2-input nor etc., but the accuracy will decrease for circuits with complex series/parallel structures ex. domino-logic circuits. In a stage with series parallel transistors the current waveform depends on different factors, for example the current depends on which transistor is switched, by collapsing the stage into a single inverter this factor is ignored. Also this method ignores that the transistors can be in different modes, ex. *saturation, linear* mode. Finally this method requires numerical simulation of the inverter, and this increases the simulation time.

b- Library of modeled current patterns

Another technique to reduce the simulation time is to use an event driven simulator [2]. The operation of such a simulator can be summarized briefly as follows: the circuit is divided into stages, the time-domain current waveforms are estimated for the stage separately based on the transitions in the event pool. The delay is determined for each stage, and the new events are added to the event pool. This operation is repeated until the event

pool is empty. At the end all the current waveforms are added to get the total supply current. The time domain waveforms for the stage are determined from formulas in the library. The library consists of delay formulas for some switch level conducting patterns such as typical logic gates. More complicated functional blocks are composed hierarchically from these patterns. The basic patterns are simulated with SPICE, the generated data is curve fitted into a simple formula which represent the delay as a function of transistor sizes, input rise and fall times, and the node capacitances. In case a pattern is not covered in the library, the delay is estimated based on a simple RC model. For each conducting pattern in a gate the charge is calculated as $\sum c_i V_i$ where i is any node in the conducting pattern, Ci is the node capacitance and Vi is the voltage swing at node i. Finally the current is modelled by a symmetrical triangle with a base equal to the delay of the gate and an area equal to the charge. This method achieves a speed-up of 3 to 4 orders of magnitude. The main drawbacks of such a method is its requirement for numerical fitting of gates in order to estimate the delay, and it only takes in to account the dynamic power dissipation. Also the current model used is not appropriate for complex CMOS circuits. Finally this method approximates the supply current to the capacitor load current and ignores the short-circuit current.

c- Library of SPICE patterns

A variation of this method is presented in [4], in this work the digital simulation, which is necessary for circuit verification, is combined with the results from analog simulations done on single cells using SPICE. A database is created consisting of cell names, input capacitances and fanouts with their respective simplified current model. The analog simulations, necessary once, for the creation of the database are made using SPICE. Since most of the current in CMOS circuits flows during transitions, the current shapes from the database are combined with the event table to derive the supply current. The main drawbacks of this method is the requirement to use standard cells, also the effect of the inputs rise/fall time on the current is not taken into account in the database. Including all

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the factors that affect the supply current i.e. input rise/fall time, output capacitance, transistor sizes, input transitions etc., will increase the database size and will be computational inefficient. On the other hand, reducing the parameters in the database and extrapolating the results will lead to inaccurate current estimates.

d- Switch-level current estimation tool

A current analysis tool that generates the current waveform flowing in the interconnections of VLSI circuits is presented in [3]. The current simulator interrogates a switch-level mode simulator (i.e. RNL [21]) and extracts information on resistance, capacitance. The current waveforms are generated by analyzing the RC equivalent circuit. The waveforms generated are suitable for predicting electromigration effects. The main advantage of this approach is achieving switch-level simulation speed. The RC model constitutes a simple model for CMOS circuit analysis, and it fails to give good approximation for the current waveforms for complex CMOS gates.

e- Probabilistic methods

Current estimators based on *statistical* and *probabilistic simulation* are used in [15][19]. These estimators can predict the *expected currents* as a function of time. This technique can be briefly summarized as follows, the logic values are replaced by *signal probabilities* and logic transitions by *transition probabilities*. An event driven *probabilistic simulation* is performed. An event at a node *i* is specified by the time of the transition and the probability of the transition. The simulator propagates the *probability waveforms* into the circuit using the transistor level description. Also the supply current at every event is estimated. These values are summed to give an *expected current waveform*.

f- Analytical modeling of CMOS gates

Different works have been done in the analytical modeling of CMOS VLSI circuits. The modeling of a long channel CMOS inverter is extensively discussed in [7]. Closed form delay formulas are obtained for a ramp input, also the output voltage is determined as

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a function of time. The short circuit power dissipation of a basic inverter is presented in [8]. The effect of the output load on the short-circuit current is discussed. The delay analysis of long-channel domino logic circuits is presented in [5], a global analytical model for CMOS domino-logic circuits made from a number of series-connected n-channel transistors and a pull-up transistor is developed. The delay modelling of series-connected short-channel MOS transistors is presented in [6], closed-form delay formulas for inverters and series-connected MOSFET structures are obtained. No work to our knowledge, has attempted the detailed analytical current modeling of complex CMOS gates.

g- Analytical modelling of MOS transistors

An engineering model for short-channel MOS devices is presented in [9], the model includes the effects of carrier drift velocity saturation. A Simplified large signal model is also included. Another short-channel model is presented in [24], the model is based on an *nth* power law MOS model.

e- Our work

This work presents a new approach to overcome the limitations described. Our approach is based on a *detailed piece-wise linear current model* that closely approximates supply current waveforms during switching of a complex CMOS gate. Combined with an event driven simulation with *accurate delay models*. All waveforms are determined analytically, this permits fast estimation of these waveforms and maximum speedup of the simulation. The different factors that affect the current waveforms are included in our model. These factors can be summarized as follows, (1) input rise and fall time, (2) the position of the transistor with the triggering input that causes the discharging (or charging) of the output node, (3) the node capacitances, (4) accounting for the different modes (saturation, linear, cut-off) of transistors in the current path, (5) the circuit topology of the switching circuit and its effect on both delay and current. Our new approach showed a good agreement with SPICE for different circuits, and it achieved a speedup of 3 to 4 order of

magnitude. The material presented in this thesis is organized as follows. Chapter 2 deals with current estimation in a circuit with multiple stages. Chapter 3 describes our analytical delay and current model and discusses how this model takes into account different factors that affect the current waveforms. Chapter 4 compares the results of our approach with SPICE on different parameters like the peak, average and instantaneous current for both dynamic and short-circuit current. In Chapter 5 we present The short channel effects on the current waveforms. A comparison between SPICE and the short-channel model is presented in Chapter 6. Also, a method for obtaining these models for a VLSI CMOS technology is presented. Finally Chapter 7 summarizes our work.

CHAPTER 2

Current Estimation in Large CMOS Circuits

2.1- Introduction

In this chapter, we present the method of handling a complex CMOS circuit with multiple stages to obtain the supply current waveforms and switching delays. Current estimation is done within an event driven simulator by decomposing the circuit into stages (Section 2.2). Two types of stages can be obtained, stages that correspond to complementary logic gates (Section 2.3) and stages including logic gates and pass gates (Section 2.4). These stages are then collapsed to an equivalent gate (rather than an inverter as done in [1]) that produces accurate current waveforms (Section 2.5). *Circuits with feed-back are not considered.*

2.2- General Approach

Our approach estimate the current in a large CMOS circuit composed of multiple stages, based on event driven simulation of the circuit combined with an analytical delay and supply current estimation. Event driven simulation is particularly suitable for current estimation in CMOS circuits, because the current flows in a CMOS gate only during switching of the gate. Therefore the current can be considered as the sum of all gate current waveforms. A large CMOS circuit can be viewed as a collection of CMOS stages [1] [14]. In circuits without pass gates the stage decomposition is static and corresponds to logic gates [14] (Fig. 2.2). For circuits with pass transistors the stage decomposition is dynamic and depends on the input transitions [14] (Fig. 2.1). A stage consists of nodes and transistors forming an electrical path from a strong signal source to some node. A strong signal can be an input node, V_{DD}, Ground or a very high capacitance. Stages generally correspond to logic gates except for pass transistor logic gates. Pass gates are included with the gates that drives them and this process is dynamic as shown in Fig. 2.1. When breaking

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the circuit into stages, each stage is assigned a number. Stage numbers are assigned so that the input to the ith stage is driven by an output of the jth stage, such $i>j$. Dividing the circuit into stages and processing them in the order of their numbers ensure that each inputs of a stage are known at the time when the stage is processed.
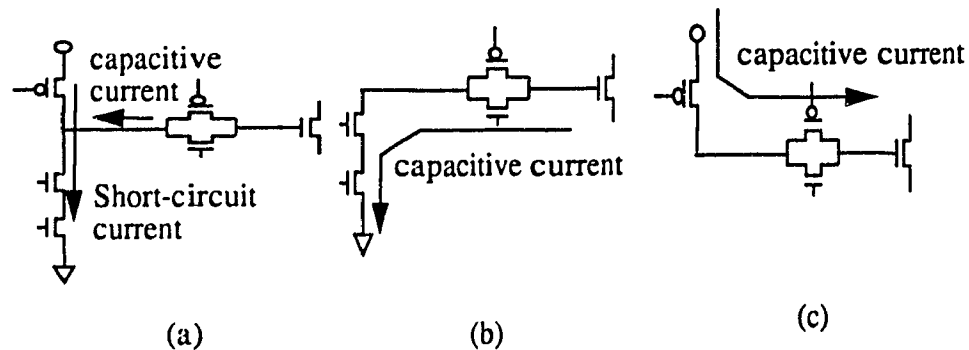
Fig. 2.1 Stage extraction during different phases of analysis

A timing analysis of the circuit, based on event driven simulation is performed at the stage level. The results of the timing simulation are combined with the estimation of supply current waveforms in each stage. The current waveforms are shifted by the corresponding stage delay. Finally the current waveforms of all stages are added to estimate the total supply current. Given a general CMOS circuit the supply current is estimated as follows:

(1) The circuit is divided into stages.

(2) The input vectors are scheduled in an event pool.

(3) An event is picked from the event pool and the supply current waveforms for each affected stage is determined. Current waveforms are obtained based on a detailed model that corresponds to stage input conditions and characteristics.

(4) Schedule the new events into the event pool, go to step (1) until the event pool is empty.

(5) Add all the current time-domain waveforms at all events simulated.

To explain our approach further we take an example of a typical circuit shown in Fig. 2.2. The circuit has no pass gates. Therefore the stage decomposition is static and corresponds to logic gates. An input vector is fed to the circuit. The circuit is divided into 6 gates as shown in Fig. 2.3. The gates are numbered from 1 to 6. Gate 1 is processed first and the supply current waveform is determined, the delay of stage 1 is estimated, also the output rise and fall time of the output of gate 1 is determined, this is put in the event pool. These parameters will permit processing of gate 2. The current waveforms are estimated for gate 2. In a similar manner the delay and output rise/fall times of all gates are determined and put in the event pool. When the event pool is empty all the current waveforms to be combined according to the delay analysis of the circuit are added to obtain the total current waveform as shown in Fig. 2.4.

Fig. 2.2 Carry-look ahead circuit

Output voltages waveforms

Gate 1 — Gate 2 — Gate 3 — Gate 4 — Gate 6

Gate 5
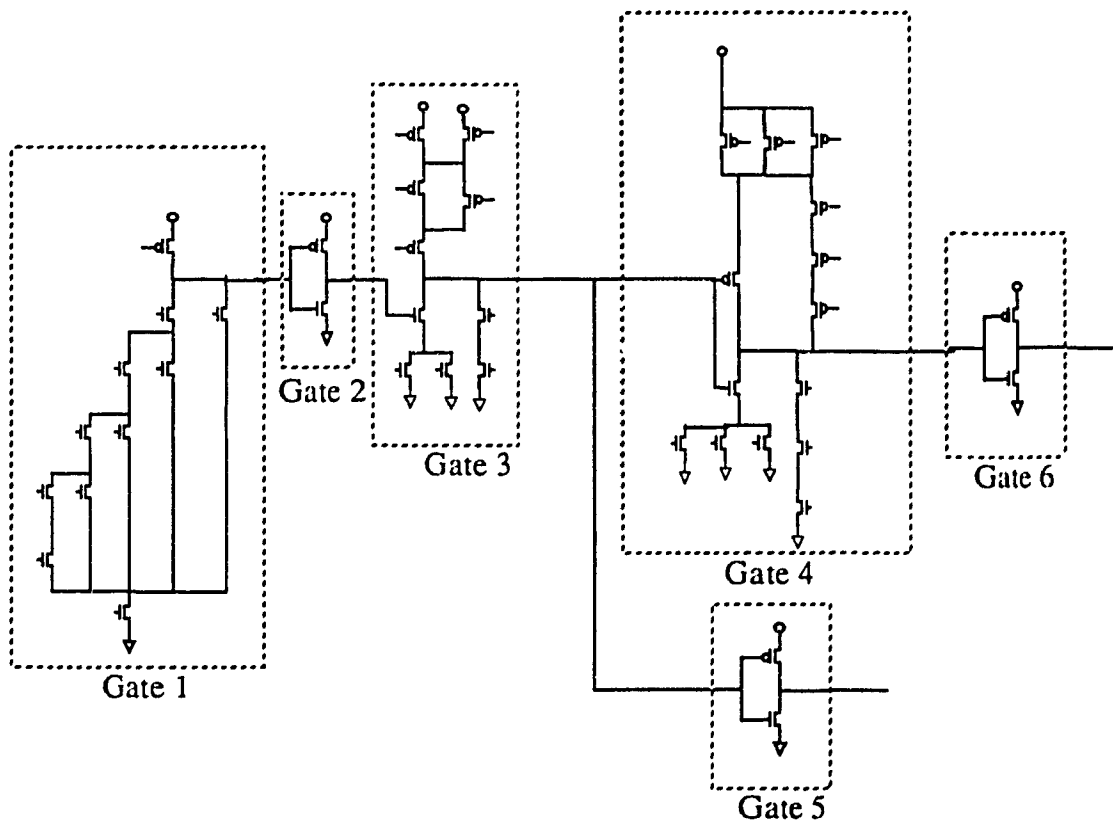
Supply current waveforms
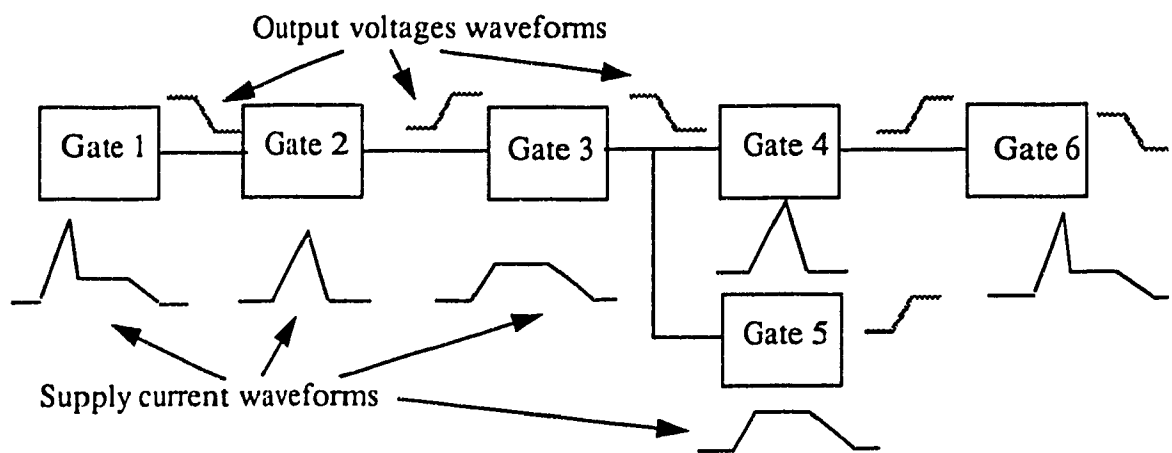
Fig. 2.3 Timing simulation combined with current estimation in each stage

Current

Current

time

time
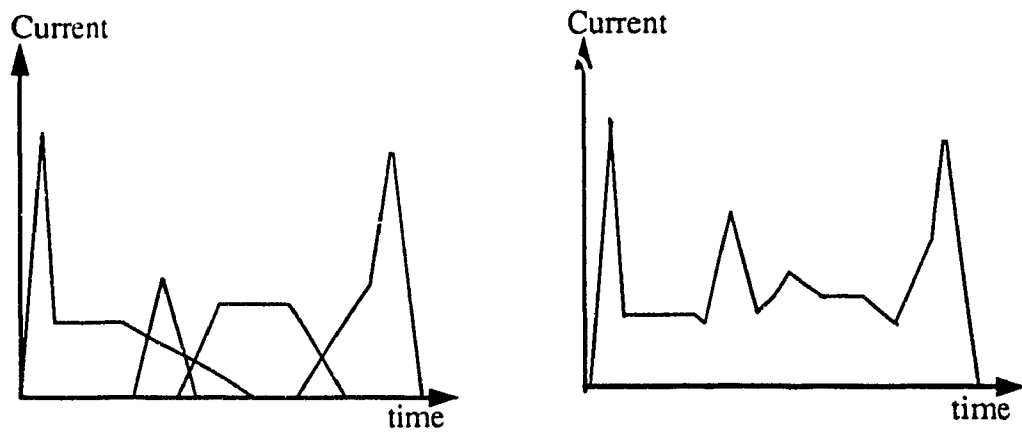
a- supply current for each stage

b- supply current for the circuit

Fig. 2.4 Supply current waveforms estimation

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2.3- Current Estimation in a Complex CMOS Gate

In this section we detail the different currents in a CMOS gate during switching. The supply current during switching of a CMOS gate has two components, the capacitive current and the short-circuit current. The capacitive current is the current needed to charge or discharge the node capacitances in the gates. The short-circuit current is the current flowing from power to ground supply lines during switching. The short-circuit power dissipation is in general less than 20% of the total power dissipation depending on the load[8].

2.3.1- Currents in a CMOS gate during switching

The supply current flows in a CMOS gate only during the transition of the output node, Fig. 2.5 shows the currents during the switching of a CMOS gate. The trigger input is defined as the transistor that causes the charging or discharging of the output node. C_n and C_p represent the node capacitances for the pull-up and the pull-down networks.

a- High to Low transition   b- Low to High transition
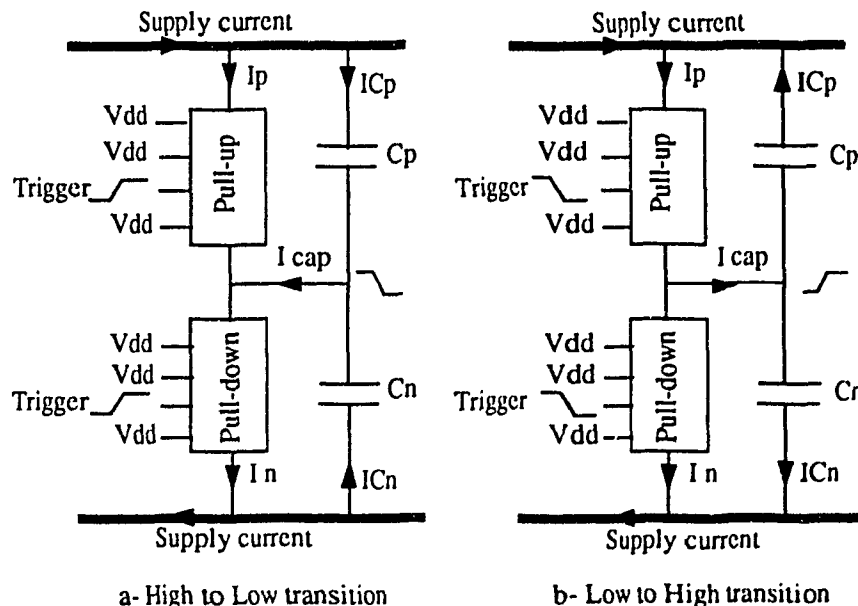
Fig. 2.5 Current in a stage during switching

The supply current for a high to low transition can be written as follows:

$$I_{supply} = I_p + I_{cp}$$

since

$$I_{cp} = C_p \frac{dV_{out}}{dt}$$

and

$$I_{short} = I_p$$

$$I_{cap} = (C_n + C_p) \frac{dV_{out}}{dt}$$

then

$$I_{supply} = I_{short} + \frac{C_p}{(C_n + C_p)} I_{cap}$$

And in the same way we can obtain the current for both transitions:

$$I_{supply} = \begin{cases} I_{short} + \dfrac{C_p}{(C_n + C_p)} I_{cap} & \text{high to low transition} \\[3mm] I_{short} + \dfrac{C_n}{(C_n + C_p)} I_{cap} & \text{low to high transition} \end{cases} \qquad \text{(EQ. 2.1)}$$

As can be seen from EQ. 2.1 the supply current can be easily derived from the capacitive current and the short-circuit current.

Capacitance estimation

Also EQ. 2.1 shows that the supply current depends strongly on the estimation of C_n and C_p. C_n and C_p represent the contribution of the different node capacitances in the gate. The node capacitances can be estimated on an individual basis as drain, source or gate capacitances. However the contribution of these node capacitances to C_n and C_p is difficult to estimate [1]. The current flowing in these node capacitances depends on the individual node voltage waveforms. In order to asses the contribution of these node capacitances we have to estimate the individual node voltages in the gate. This is not possible, especially in

a complex CMOS gate. Therefore, all capacitances associated with the pull-up are added to estimate C_p and all the capacitances associated with the pull-down are added to estimate C_n. Our model presents basic waveforms to quickly estimate the capacitive current and the short circuit current. These two waveforms are then combined using EQ. 2.1 to estimate the supply current. Each gate is processed through different steps in order to estimate the capacitive and short-circuit current.

2.4- Currents in stage with pass gates

Pass gates are used in CMOS circuits for clocking and control. Different clocking strategies can be used in digital design i.e. 2-phase clocking, 4 -phase clocking. Fig. 2.6 shows a dynamic logic circuit with 2-phase clocking. In this clocking scheme the first stage is precharged during ϕ_1 and evaluated during ϕ_2. While the first stage is evaluated the second stage is precharged and the first stage output are stored on the second stage input. The pass gate is active when latching the outputs of stage 1 to the inputs of stage 2. The currents involved when a pass gate is active are shown in Fig. 2.6. In the general case, the currents in a stage made of a logic gate driving a network of pass gates are shown in Fig. 2.7. The Supply current can be derived in a similar way to the current in a logic gate (section 2.3), and is given by EQ. 2.1.
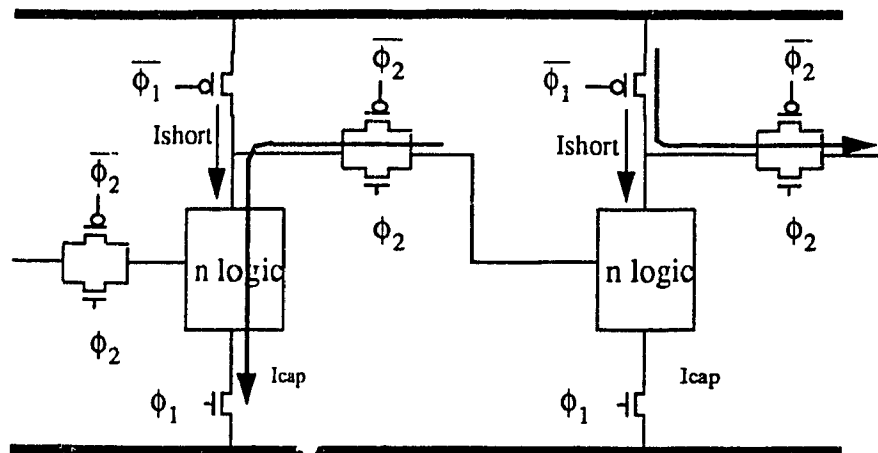
Fig. 2.6 Dynamic logic with 2-phase clocking

a- High to Low transition   b- High to Low transition
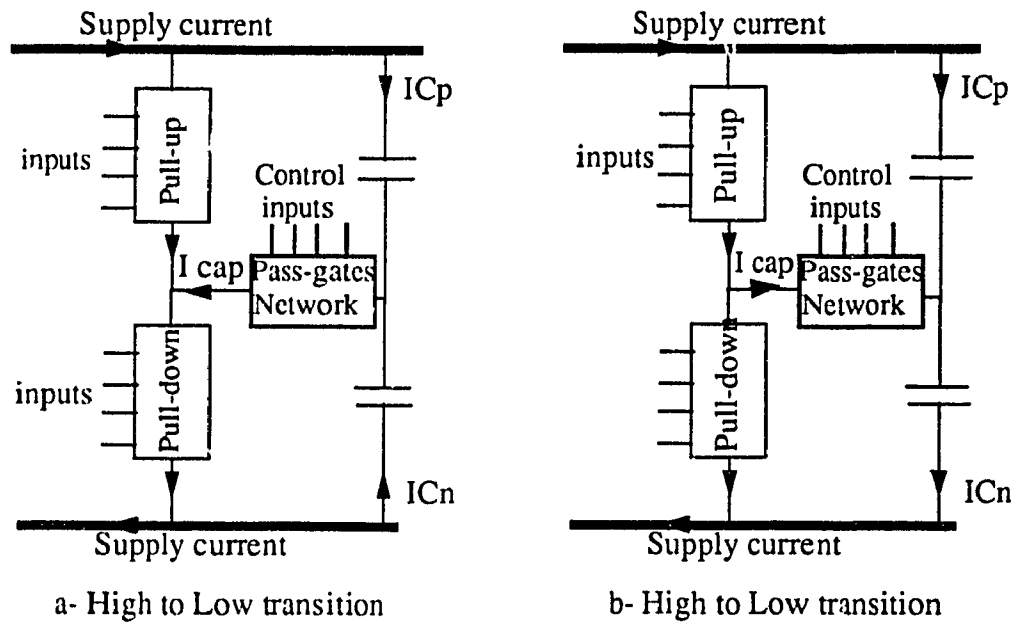
Fig. 2.7 Current in stages with pass gates

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2.5- Capacitive Currents and Short-Circuit Currents Estimation

We take the case where a gate is switched from high to low, the case where the gate is switched from low to high is symmetrical. Our model is based on basic time-domain current waveforms to estimate the capacitive and short-circuit current. We have determined through careful analysis and simulation that 4 waveforms cover all the possibilities of inputs and capacitances values. One waveform cover the short circuit current. Fig. 2.8 shows these waveforms for a high to low transition. The CMOS gate is processed through different steps to estimate the parameters included in these waveforms.

Note :

We did not consider the effect of signal skew between p-block and n-block on the model. In the case where there is a signal skew and the n-block and p-block are triggered, a large short-circuit current occurs. This normally does not happen in a properly designed circuit.

The current estimation in a CMOS gate is summarized as follows:

1- The pull-up network is replaced with an equivalent transistor, This is a valid approximation for complementary logic CMOS circuit. In fact the pull-up conducts only for the duration of the input trigger transition, when all inputs to the pull-up will be at V_{DD} all transistors in the pull-up will be cut-off. An example of the resulting circuit is shown in Fig. 2.9.

2- Determine the trigger transistor. The first transistor that creates a path to ground is selected as the trigger transistor. We assume that both triggers are the same for the pull-up and pull-down.

3- Determine the shortest "on" path P in the pull-down from the output node to the ground (Fig. 2.9).

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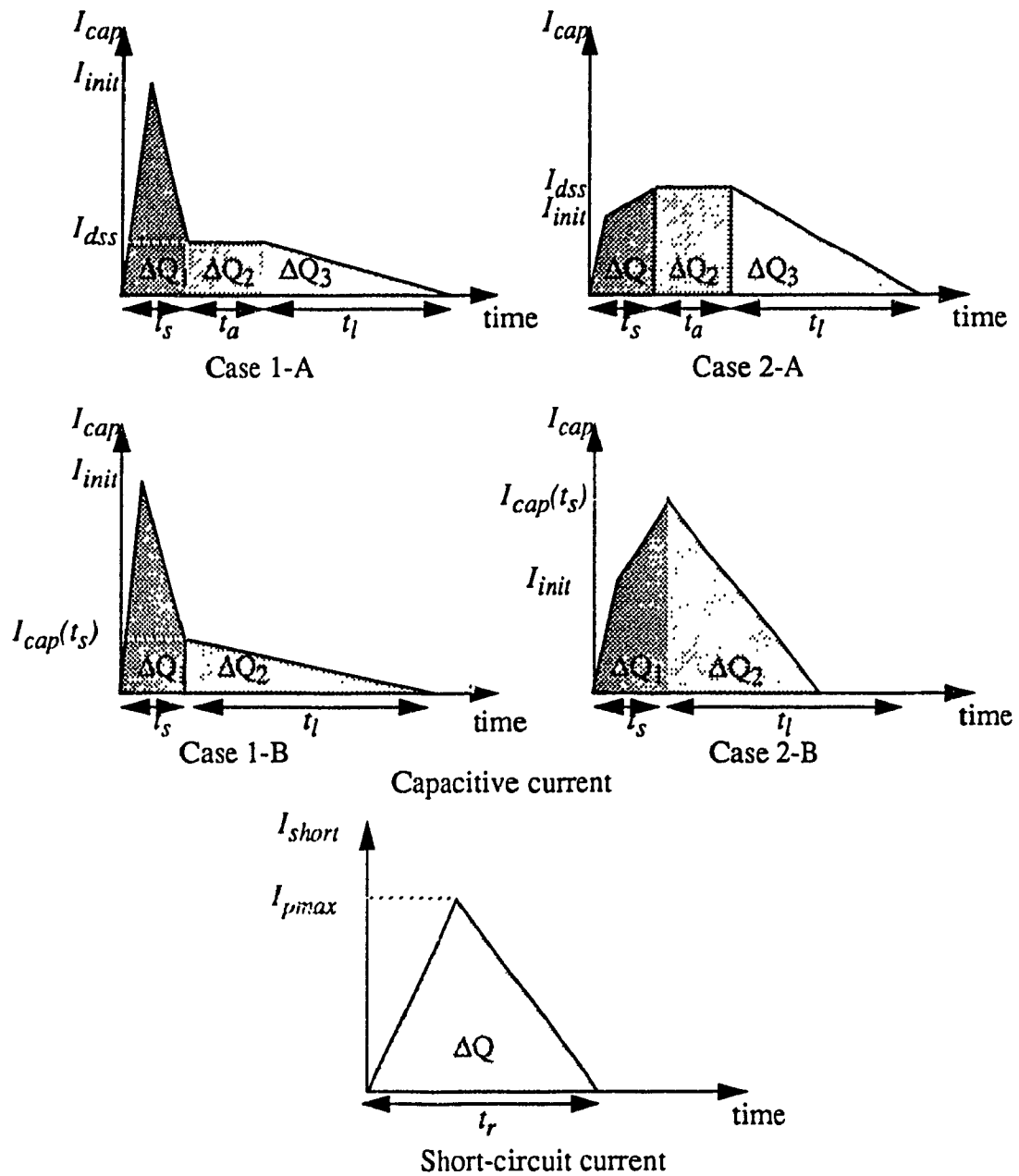
Fig. 2.8 Basic current waveforms

4- Collapse all parallel/series networks of "on" transistors in parallel with any transistor included in P into an equivalent transistor by series/parallel transformations. The result of this step is a network of series connected MOS transistors shown in Fig. 2.10.

5- The circuit of Fig. 2.10 is then collapsed in two ways to obtain two equivalent gates. Gate 1 is used to estimate the capacitive current surge due to the switching (Fig. 2.11), and gate 2 is used to estimate the capacitive current waveform (Fig. 2.12). Gate 1 is obtained as follows, all transistors in the pull-down (Fig. 2.10) from the drain of the trigger Ti to the output node are collapsed to one transistor Ttop (Fig. 2.11), and all the transistors from the drain of the trigger transistor to the ground are collapsed to one transistor Tbottom (Fig. 2.11). This way of collapsing gives a good approximation of the current surge due to switching because all the capacitance nodes below the trigger are discharged and all the capacitances nodes above the trigger are charged. Gate 2 is determined as follow, all the transistors from T2 to Tn (Fig 2.10) are collapsed to an equivalent transistor (Fig. 2.12). The collapsed gate gives a good estimate of the capacitive current waveform. The circuit is collapsed in this way because T1 will start in saturation mode while all other transistors (T2 to Tn) will be in the linear mode. In this step we use the models of Fig. 2.11 and 12 to determine the capacitive current. The effect of the pull-up is neglected and is considered separately in step 7.

6- In order to estimate the short-circuit current, the stage is collapsed into an equivalent inverter shown in Fig. 2.13. The pull-up current is neglected when estimating the output voltage waveform, this waveform can still be used to estimate the short-circuit current. The estimation of the short-circuit current is presented in section 3.3. The delay of this gate is estimated and the output fall time is determined. The delay estimation is presented in Section 3.4.

7- Finally, the short-circuit and capacitive current waveforms are combined using EQ. 2.1 to estimate the supply current.
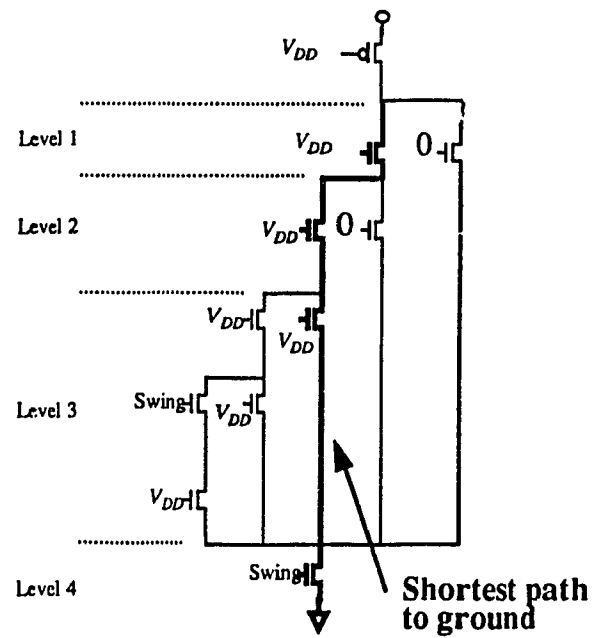
Fig. 2.9 Complex CMOS gate
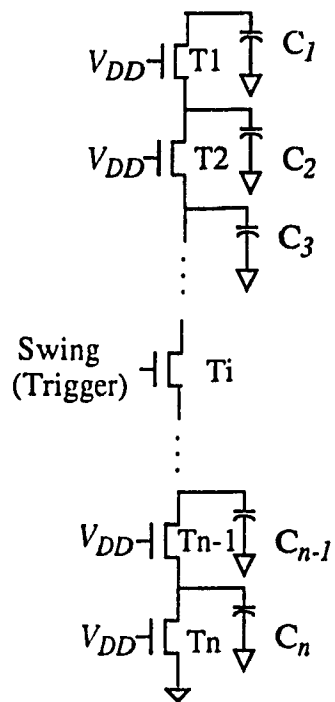
Fig. 2.10 Equivalent series-connected MOS transistors network

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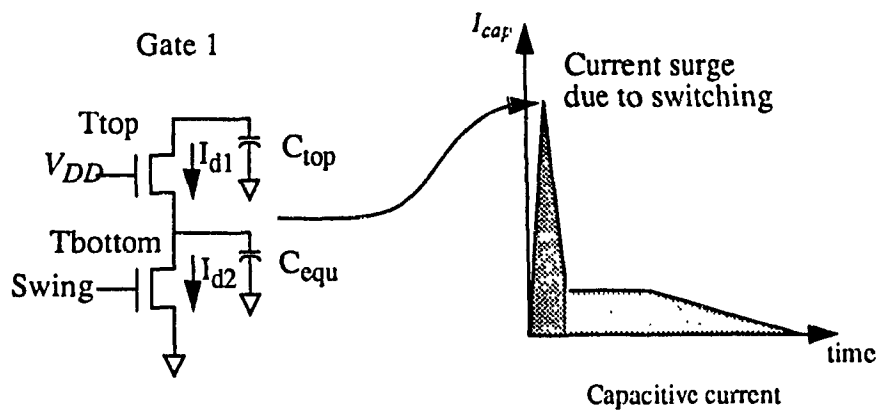
Fig. 2.11 Equivalent circuit for current surge estimation
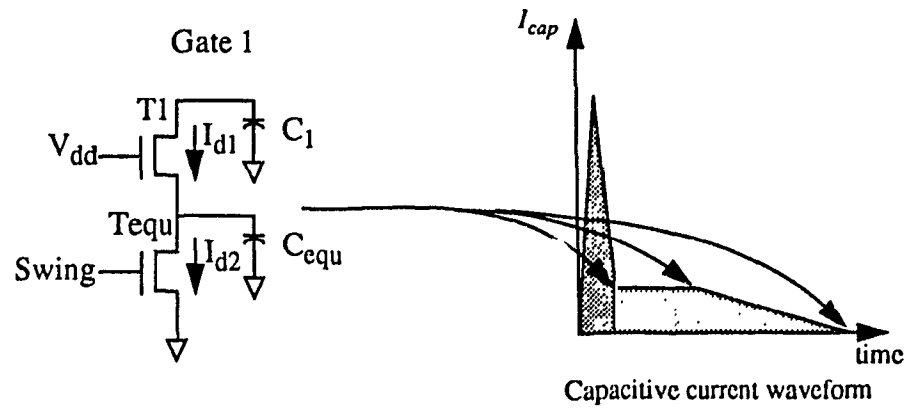
Fig. 2.12 Equivalent circuit for capacitive current estimation

short-circuit current,
delay, output fall time
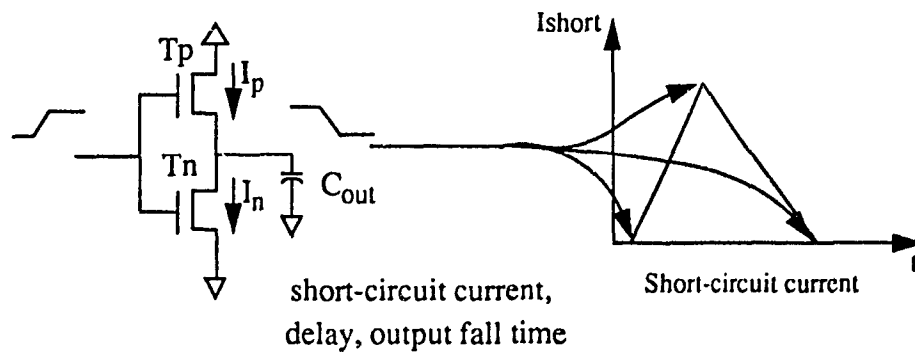
Fig. 2.13 Equivalent inverter

2.6- Collapsing a Complex CMOS Gate

Collapsing a complex CMOS gate to an equivalent simpler circuit is a widely used approach in order to reduce the simulation time. To achieve a good accuracy, the collapsed circuit should preserve the delay, power (charge conservation) and current waveforms.

2.6.1- Delay considerations

To illustrate the delay comparison between a series-connected MOS network and an equivalent transistor we take a series-connected transistors network of Fig. 2.14.
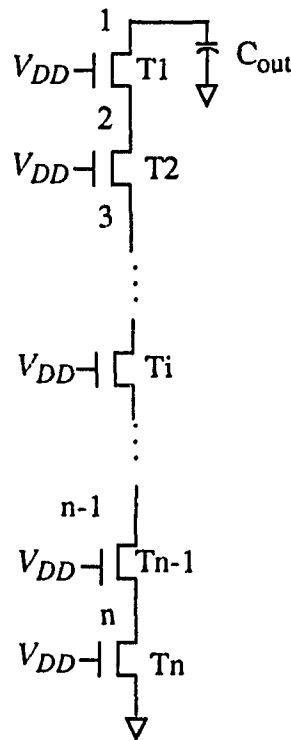
Fig. 2.14 Series-connected MOS transistors

Assuming a step input and a large load compared to the node capacitances, a straight forward solution of the problem is presented in [6] for long-channel CMOS transistors. We present this solution to illustrate the collapsing considerations. Neglecting the node

capacitance current, because of the large load we can write:

$$I_{d1} = I_{d2} = \ldots = I_{di} = \ldots = I_{dn}$$

The drain current of transistor T_i in the linear region is given by:

$$I_i = \beta_i \left[(V_{DD} - V_T - V_{i+1})(V_i - V_{i+1}) - \frac{1}{2}(V_i - V_{i+1})^2 \right]$$

This can be re-written as follows:

$$\frac{I_i}{\beta_i} = \left[(V_{DD} - V_T)V_i - \frac{1}{2}V_i^2 \right] - \left[(V_{DD} - V_T)V_{i+1} - \frac{1}{2}V_{i+1}^2 \right] \qquad \text{(EQ. 2.2)}$$

defining $f(V) = (V_{DD} - V_T)V - 1/2\ V^2$ we can write:

$$\frac{I_1}{\beta_1} = f(V_1) - f(V_2)$$

$$\frac{I_3}{\beta_2} = f(V_2) - f(V_3)$$

$$\vdots$$

$$\frac{I_i}{\beta_i} = f(V_i) - f(V_{i+1})$$

$$\vdots$$

$$\frac{I_n}{\beta_n} = f(V_n) - f(0)$$

adding all the above equations and simplifying, we have:

$$\sum_1^n \frac{I_i}{\beta_i} = f(V_n) - f(0)$$

Since all drain currents are equal, I_i can be taken out of the sum and the equivalent conductance will be:

$$\frac{1}{\beta_{equ}} = \sum_{1}^{n} \frac{1}{\beta_i}$$

Assuming equal transistors sizes:

$$\beta_{equ} = \frac{\beta_i}{n} \qquad \text{(EQ. 2.3)}$$

For this simplified case we can conclude that the delay in n series-connected MOS transistors is n times the delay of a single transistor. An RC model will predict that n series-connected MOS transistors will have n times the delay of a single transistor when the load capacitance is dominant. This relation does not hold for short channel transistors, and the delay ratio is given in [6] by:

$$\frac{\beta \, (n - transitors)}{\beta \, (inverter)} \approx \frac{1}{2} N \frac{Vdsat}{(1 - V_T)} (1 - \gamma) (n - 1) \qquad \text{(EQ. 2.4)}$$

where $Vdsat$ is the saturation voltage when $V_{GS} = V_{DS} = V_{DD}$

V_T is the threshold voltage

N is an empirical factor

γ is the body effect coefficient

In the case of a small output load capacitance an RC model predicts that n series-connected MOS transistors with small output load capacitance will have a delay n^2 time the delay of a single inverter, However in [6], it is shown that the situation is more favorable for series-connected MOS transistors and EQ. 2.4 is still an acceptable approximation. The physical interpretation of the ratio improvement in the submicron region is that each transistor will have a smaller V_{DS} compared to a single transistor and therefore the velocity saturation is less severe in series-connected MOS transistor, so the current improvement induced by the smaller V_{DS} dominates the degradation induced by the body effect.

Therefore EQ. 2.4. is an acceptable approximation for both large and small loads. For the purpose of our model the equivalent transconductance is obtained in the same way as in EQ. 2.4 for a long-channel devices and in EQ. 2.4 for short-channel devices.

The problem is more complex for a complex series/parallel connected MOS network. Different work has been done on delay estimation in RC trees [11] [12] and applied to MOS pass networks [13], but the improvement in the quality of results when applying these methods to complex series/parallel connected MOS transistors is not obvious. For the purpose of our model we apply EQ. 2.4 and 2.5 for series-connected transistors, in the case of parallel transistors, their conductance is added in order to obtain an equivalent transistor circuit.

2.6.2- Charge considerations

Another important issue in the collapsing process is the charge stored in the circuit. The dynamic power dissipation of a CMOS circuit with a DC power supply is proportional to the charge stored in the circuit. In order to model the average power dissipation accurately, the original circuit and the equivalent circuit used by the model must hold the same charge stored. This can be shown as follows:

$$P_{avg} = \frac{1}{T}\int_0^T V_{DD}I_{DD}dt$$

Since V_{DD} is constant, it can be taken out of the integral:

$$P_{avg} = \frac{V_{DD}}{T}\int_0^T I_{DD}dt$$

$$P_{avg} = \frac{V_{DD}}{T}Q$$

where Q is the charge stored in the circuit:

$$P_{avg} = \alpha Q \qquad\qquad \text{(EQ. 2.5)}$$

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To model accurately the average power dissipation in the network, we have to determine the charge stored in the network, before switching i.e.:

$$Q = \sum C_i V_i (t = 0)$$

Where C_i is the node capacitance and Vi is the node voltage.

So in order to have the same charge in the two circuits we must have:

$$V(0) = \frac{\sum C_i V_i (t = 0)}{C_{equ}}$$

(EQ. 2.6)

EQ. 2.7 is used to estimate the initial voltage in the equivalent circuit. This equation is particularly important in series-connected transistors. For example given the network of Fig 2.14, if transistor Ti is the trigger transistor, then all the nodes above Ti are charged to V_{DD}-V_T except the output node which is charge to V_{DD} and all the nodes below the trigger are at 0v. Using EQ. 2.7 the initial voltage in the equivalent circuit becomes dependent on the transistor triggered.

2.6.3- Body effect in series-connected MOS transistors

In order to model series-connected transistors correctly, we have to take into account the back-gate bias effect, the maximum threshold voltage at the pinch-off point is given by [5]:

$$V_{Tn} = V_{Tn0} + \Upsilon_n \left[\left(\frac{\Upsilon_n^2}{4} - V_g + \Upsilon_n \sqrt{2\phi_F} + 2\phi_F \right)^{1/2} + \sqrt{2\phi_F} + \frac{\Upsilon_n}{2} \right]$$

(EQ. 2.7)

Where V_{Tno} is the threshold voltage with $V_{SB} = 0$, V_{SB} being the voltage difference between the source and the body, Υ_n is the body effect coefficient, Φ_F is the equilibrium Fermi level potential and V_g is the gate to substrate voltage. When transistors are operating in the linear region, the threshold voltage is approximated by the average of the maximum

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and minimum voltages [5]:

$$\overline{V_{Tn}} = \frac{V_{Tno} + V_{Tn}}{2}$$

(EQ. 2.8)

While for transistors operating in saturation, the threshold voltage is expressed as αV_{Tn}, where α is a correlation factor ranging from 0.5 to 1.0.

2.6.4- Multiple input transitions

In the case where multiple input transitions occur, the first transistor that creates a path to the ground is selected as the trigger. The problem arises when the pull-down network has a delayed trigger input(s) that sets a new path(s) to ground when the gate is still switching. This case is illustrated in Fig. 2. 15.
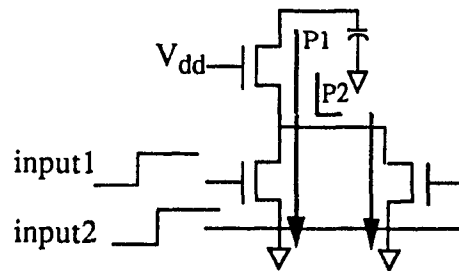
Fig. 2.15 Delayed trigger transition

Input 1 arrives first and sets path P1 from the output node to the ground. While the gate is still switching input 2 arrives and sets path P2 from the output node to ground, and affects the current waveform. This problem is solved by defining a time window from the time the first path to ground is created until the time the output node is completely switched. If there is input transitions in that time window, the pull-down is collapsed again each time a new path is set by these delayed transitions. The current waveform is adjusted according to these new paths. This procedure is illustrated in Fig. 2.16 for the circuit of Fig. 2.15.
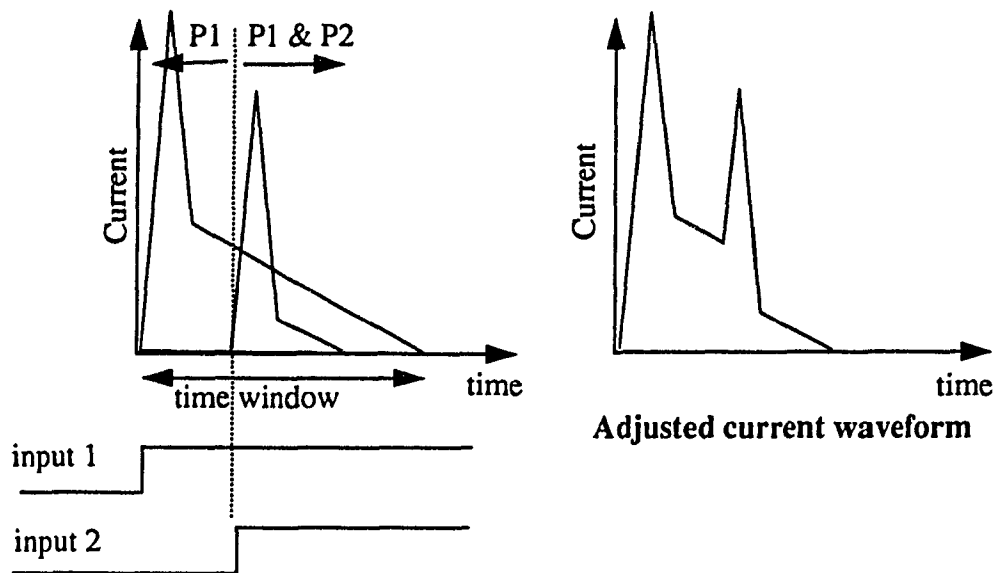
Fig. 2.16 Current adjustment for a delayed trigger input

The circuit of Fig. 2.15 is simulated using SPICE level 3 to show an example of this case. The supply current is shown in Fig. 2.17.
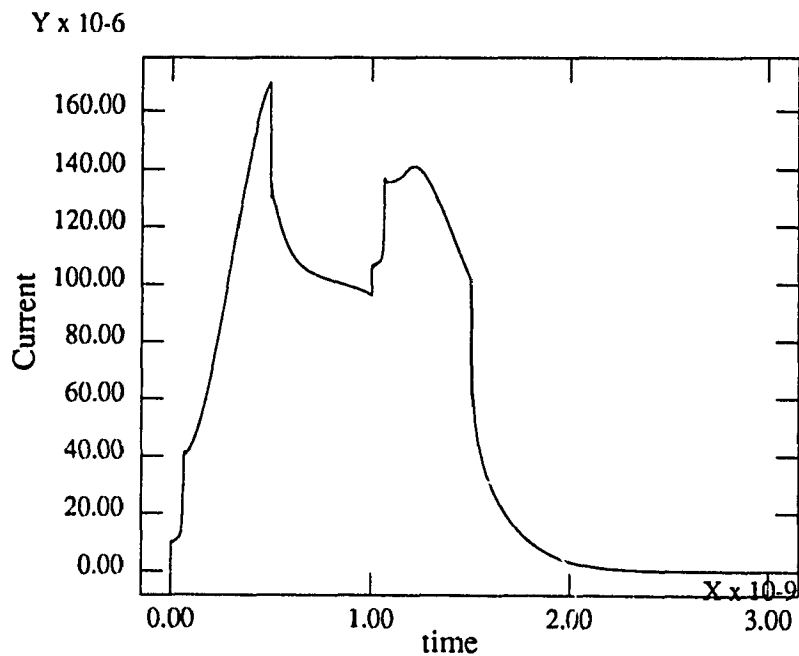
Fig. 2.17 SPICE simulation of a circuit with a delayed trigger transition

CHAPTER 3

Analytical Model of Long-Channel MOSFETs

3.1- Introduction

As discussed earlier our approach to current estimation is based on event driven simulation. A piece-wise linear model is used to estimate the supply current waveforms. The supply current in each stage is estimated from the capacitive current and short-circuit current. In this chapter we present the analytical model for capacitive current and short-circuit current estimation in a gate. Also, the delay and output rise/fall time are determined. The rise/fall times of the output node is particularly important in the estimation of the supply current, since it has a direct effect on the short-circuit current and the capacitive current waveform shapes. The supply current for each stage of the multi-stage network is shifted by the corresponding delay time. Finally all the supply current waveforms are added to estimate the total supply current. *We assume throughout the analysis a long channel MOSFET model.*

3.2- Model Description

We assume that the output node of the gate is switched from high to low, the other case is symmetrical. As was presented in Section 2.2, in order to estimate the capacitive current in a complex CMOS gate, the pull-down is collapsed to a series-connected MOS network. Fig. 3.1 shows such network. Before the switching of the trigger transistor, all the nodes capacitances above the trigger are charged to $V_{DD} - V_T$ and all the nodes capacitances below the trigger are discharged to 0.

First we model the current waveform if the input trigger is a step input, the case of a ramp input will be discussed in Section 3.4. When the trigger transistor is switched "on"

a current surge occurs due to the switching (segment 1, Fig. 3.2). All transistors from T2 to Tn are in the linear region, T1 starts in the saturation mode (Fig. 3.1). When T1 is in the saturation region the internal node voltages rise to a plateau value for the nodes below the trigger, and fall to a plateau value for the nodes above the trigger as shown in the example of Fig. 3.2. Whether the node voltages will reach their plateau value depends on how long T1 stays in the saturation region. If the internal node voltages reach their plateau value (segment2, Fig. 3.2), all the capacitances C_2 to C_n currents are almost zero, except for the current in the load capacitance C_1. The current I_{cap} in this time is constant. C_1 continues to discharge until T1 gets out of the saturation region and passes to the linear mode. When all transistors are in the linear mode, all internal node voltages will fall to 0 (segment 3, Fig. 3.2). This behavior is illustrated in Fig. 3.2.
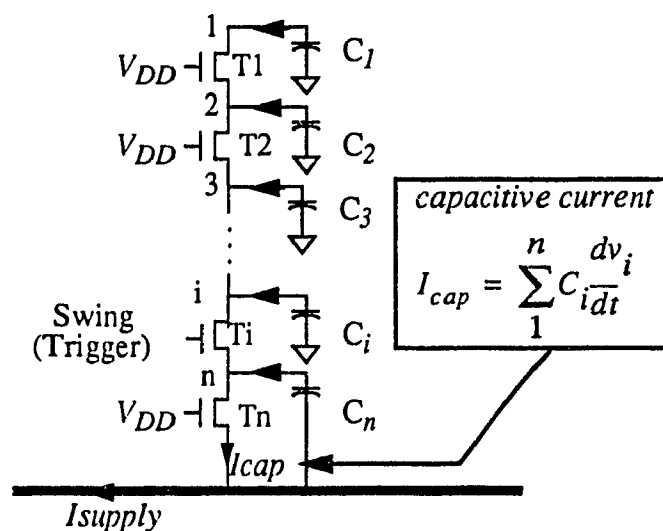
Fig. 3.1 Current in series-connected MOS transistors

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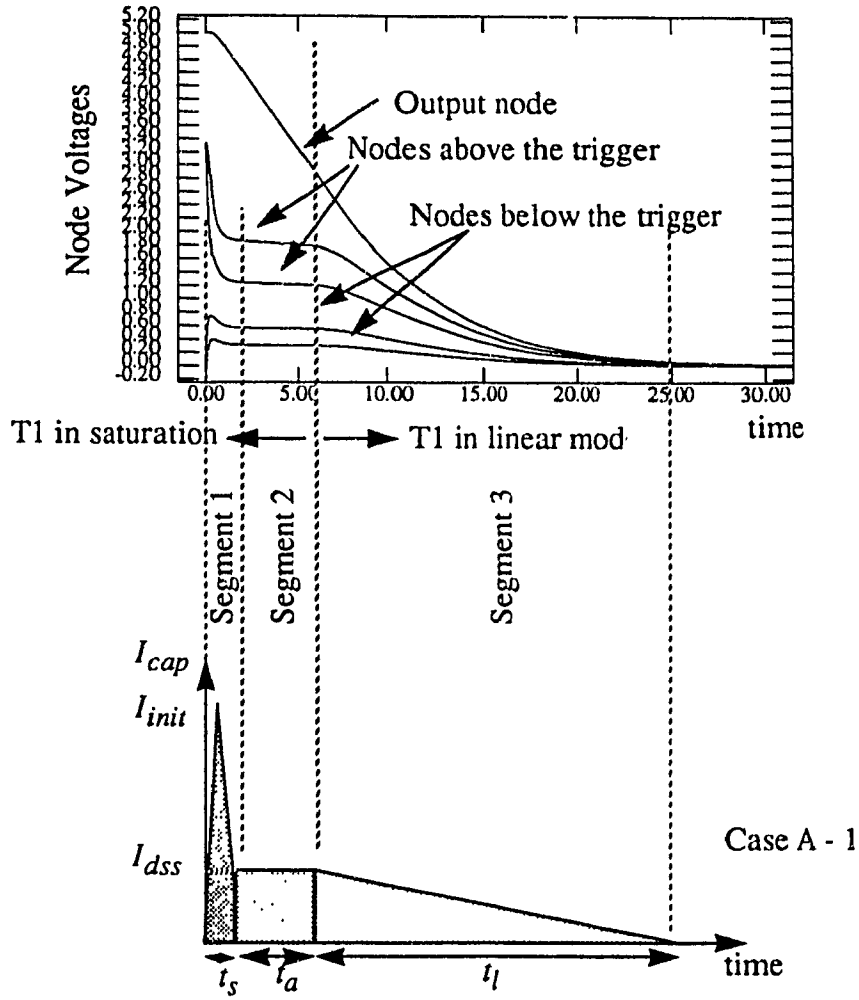
Fig. 3.2 Capacitive current model

Our model is based on 3 time segments (Fig. 3.2). Segment 1 represents the period where all internal nodes are charging or discharging to their plateau value. The duration of this segment is t_s, t_s is defined as the time it takes for the internal node voltages to charge to within 1% of the plateau value. The ground current during this period will rise to Iinit then fall to a plateau value I_{dss}. The value I_{init} can be larger or smaller than I_{dss} depending on the transistor triggered. Segment 2 with duration t_a represents the period where all internal nodes are at their plateau value. The ground current in this segment is constant at I_{dss}. Segment 2 is omitted if T1 gets out of the saturation before the internal nodes reach their plateau value, and the current will be modeled only by Segment 1 and Segment 3, and

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I_{dss} is replaced by $I_{cap}(t_s)$ which represents the capacitive current at t_s. Segment 3 represents the period where all the internal nodes discharge from their plateau value to 0. The duration of this segment is t_l. The ground current in this segment will fall from I_{dss} to 0. The current waveform in general will take the 4 shapes shown in Fig. 3.4. For the purpose of mathematical correctness, the 3 time segments described are defined as follows, segment 1 starts at t=0 and ends at t=t_1, segment 2 starts at t=t_1 and ends at t=t_2 and segment3 starts at t=t_2 and ends at t=t_3. This is illustrated in Fig. 3.3.

Segment 1   Segment 2   Segment 3

0   t_1 t_2 t_3

t_s t_a t_l
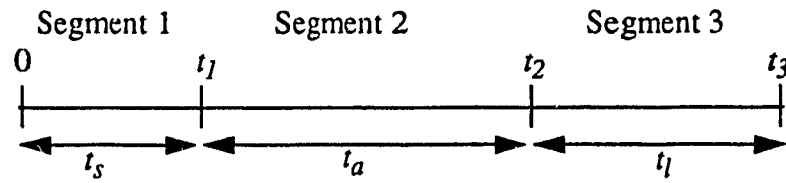
Fig. 3.3 Segments definition

3.3- Circuit Analysis for a Step Input

In this section we propose to determine an analytical approximation of the capacitive current in series-connected transistors. The short-circuit current is zero for a step input. Fig. 3.1 shows a network of series-connected MOS transistors. This kind of circuit has been analyzed in [5] to estimate the delay in domino-logic circuits. We use a similar approach to derive the current waveform for a step input. For our analytical analysis one input will be selected as the trigger. The capacitive current I_{cap} is equal to the sum of all the currents in the node capacitances (Fig. 3.1):

$$I_{cap} = \sum_{1}^{n} C_i \frac{dV_i}{dt} \qquad \text{(EQ. 3.1)}$$

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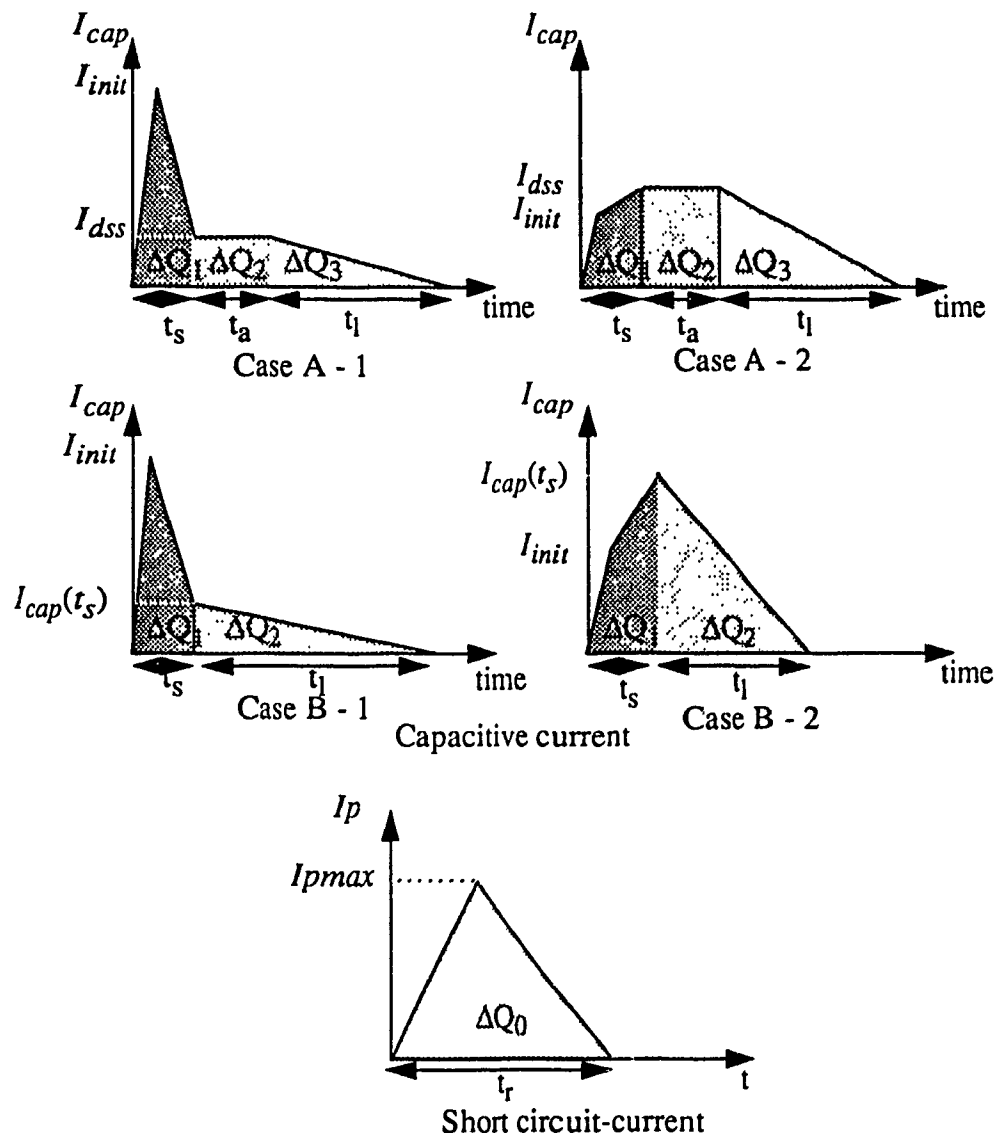
Fig. 3.4 Basic current waveforms

The goal of the model is to get an accurate peak current, average current and instantaneous current. In order to model the average accurately, the charge in the original circuit and the equivalent circuit must be the same. The peak current in series-connected MOS network is more difficult to estimate, it depends on the circuit topology, transistor switched, node capacitances and transistor sizes. As can be seen in Fig. 3.2 the peak current can have two values I_{init}, I_{dss} depending on the case that will be discussed later. The value I_{dss} can be determined accurately, but I_{init} is more difficult to estimate since it depends strongly on the node capacitances, transistor sizes and the trigger. In order to have an acceptable estimate of I_{init} we use the approximation shown in Fig. 3.5. Assuming that transistor Ti is the trigger, all transistors from node i to the ground are replaced with an equivalent transistor, and all corresponding capacitances are added into C_{equ}. From the resulting circuit I_{init} is determined.
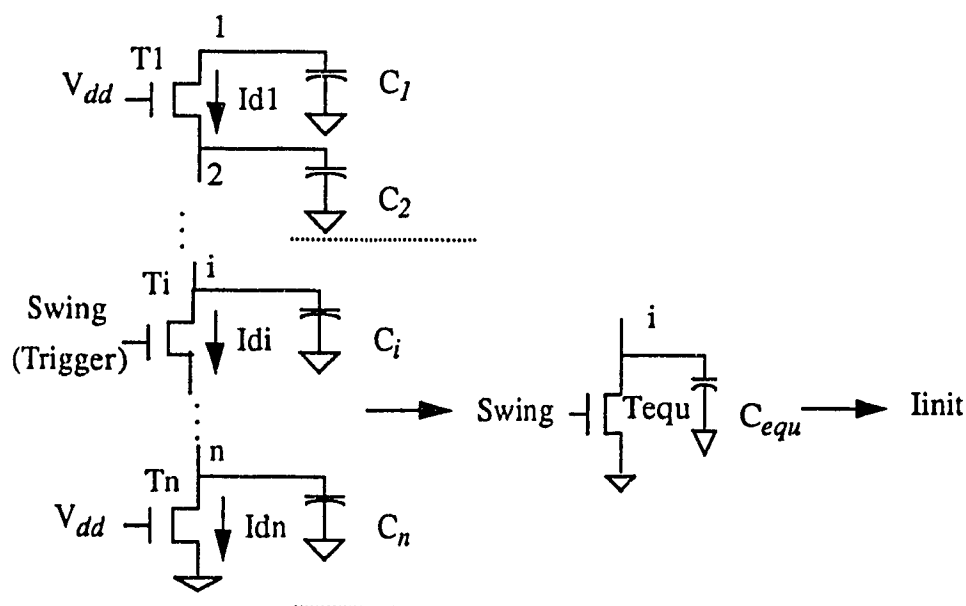
Fig. 3.5 I_{init} estimation

This approximation is valid for fast inputs and gives an acceptable estimate for practical input rise and fall time. In the case of a step input, the current in the equivalent circuit starts at:

$$I_{init} = \frac{\beta_{equ}}{2}(V_{DD} - V_T)^2 \qquad\qquad \text{(EQ. 3.2)}$$

β_{equ} represents the transconductance of the equivalent transistor and V_T the threshold voltage. We model the instantaneous capacitive current using a piece-wise linear model given some important points shown in Fig. 3.2. For the case of a step input these points are given as (time, current) are $(0, I_{init})$, $(t1, I_{dss})$, $(t2, I_{dss})$, $(t3, 0)$. Our model is based on these four (time,current) points in the current waveform. In this section we derive these points analytically. For a step input the pull-up current will not be considered, since the PMOS pull-up transistor will be cut off immediately. Before switching transistor Ti in Fig. 3.1, all the internal node capacitances above Ti are charged to $V_{DD} - V_T$ approximately, except the output node which is charged to V_{DD}, and all the internal nodes below Ti are at 0v. When the trigger transistor is switched on, T1 will be in saturation, and all the other MOS transistors will be in the linear mode. Transistor T1 will act as a voltage controlled current source, and the current is given by [5]:

$$I_{d1} = \frac{\beta_1}{2}[V_{DD} - \alpha V_{Tn} - v_2(t)]^2$$

Where α is a correlation factor ranging from 0.5 to 1 presented in Section 2.6.3, pp. 25. Two cases are to be considered, case 1 when the internal nodes (i.e. node 2 to n, Fig. 3.1) capacitances reach their plateau values while T1 is still in saturation and case 2 is when T1 gets out of the saturation region before the internal node voltages reach their plateau values. Fig 3.5 shows the equivalent circuit used to estimate the capacitive current. Tequ is the equivalent transistor for all transistors from T2 to Tn, the equivalent transconductance of the Tequ is given by EQ. 2.4 for long channel transistors. C_{equ} represent the sum of all the node capacitances C_2 to Cn (Fig. 3.1). When lumping node capacitances, the equivalent circuit (Fig. 3.6) must have the same charge as the original circuit (Fig. 3.1):.

$$\sum_{2}^{n} v_i C_i \bigg|_{t=0} = v_2 C_{equ} \bigg|_{t=0}$$

Then we can set the initial node 2 voltage at:

$$v_2(0) = \frac{\sum\limits_{2}^{n} C_i v_i (t = 0)}{C_{equ}}$$

(EQ. 3.3)
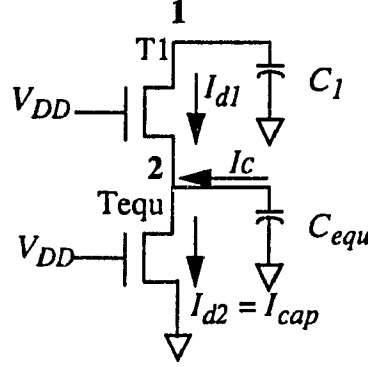
Fig. 3.6 Equivalent circuit for the estimation of the capacitive current

3.3.1- Case 1: T1 stays in saturation until all node voltages reach their plateau values)

Fig. 3.2 shows a typical case 1 circuit. The internal node voltages (i.e. node 2 to n, Fig. 3.1) reach their plateau values while T1 is in saturation. In this case the capacitive current waveform will be modelled based on 3 segments.

Case 1, segment 1: When T1 is in the saturation region and the node voltages are charging (or discharging) to a plateau voltage. This segment has a duration of t_s

Case 1, segment 2: All internal voltages are settled to a plateau voltage and T1 is still in the saturation region. The duration of this segment is t_a.

Case 1 Segment 3: When T1 leaves the saturation region to the linear region. All transistors are in the linear mode. The duration of this segment is t_l.

We will analyze these segments in detail to show how the different parameters are derived.

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i- Case 1, segment 1

Segment 1 starts at the time the trigger transistor is switched and ends when the internal node voltages is within 1% of plateau value. The current rises to I_{init} at the beginning of the segment and equals to I_{dss} at the end.

a- Current at the beginning of segment 1, I_{init}

The estimation of I_{init} was discussed earlier in section 3.3. and is given by EQ. 3.2.

b- Current at the end of segment 1, I_{dss}

When all internal node voltages reach their plateau values all the voltages V_i will be stabilized momentarily in this period. Then all the currents in the capacitances will be zero, since all $\frac{dV_i}{dt} \approx 0$. The currents I_{d1} and I_{d2} (or I_{cap}) of Fig 3.5 are given by:

$$I_{d1} = \frac{\beta_1}{2} [V_{DD} - \alpha V_{Tn} - v_2(t)]^2 \qquad \text{(EQ. 3.4)}$$

$$I_{d2} = \beta_{equ} \left[(V_{DD} - \overline{V_{Tn}}) v_2(t) - \frac{1}{2} v_2(t)^2 \right] \qquad \text{(EQ. 3.5)}$$

Since at the end of segment, $I_{d1} \approx I_{d2}$, we can equalize the two above equations and resolve for v_{2ss} which is the plateau value at node 2. v_{2ss} is given in [5]:

$$v_{2ss} = \frac{\Omega - \sqrt{\Omega^2 - n(n+1)V_e^2}}{n+1} \qquad \text{(EQ. 3.6)}$$

Where $\Omega = nV_e + (V_{DD} - \overline{V_{Tn}})$

$$n = \frac{\beta_1}{\beta_{equ}}$$

$$V_e = V_{DD} - \alpha V_{Tn}$$

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Once v_2 at the end of segment 1 is known I_{cap} at the end of the segment is given by:

$$I_{cap} = I_{dss} = \beta_{equ}\left[(V_{DD} - \overline{V_{Tn}}) v_{2ss} - \frac{1}{2} v_{2ss}^2\right] \qquad \text{(EQ. 3.7)}$$

b- Duration of segment 1, t_s

We know now the value of the capacitive current, I_{dss} at the end of this segment. We have to determine the duration of this segment. The duration t_s is the time needed for node 2 to reach 99% of v_{2ss}. The node equation at node 2 for the circuit of Fig. 3.6 is given by:

$$\frac{\beta_1}{2}[V_{DD} - v_2(t) - \alpha V_{Tn}]^2 = C_{equ}\frac{d}{dt}v_2(t) + \beta_1\left[(V_{DD} - \overline{V_{Tn}}) v_2 - \frac{1}{2} v_2^2\right]$$

Resolving the above differential equation will lead to [5]:

(1) if $v_2(t=0) < a2$

$$v_2(t) = \frac{a_2 - a_1 e^{-At+B}}{a_2 - e^{-At+B}} \qquad \text{(EQ. 3.8)}$$

(2) if $v_2(t=0) > a2$

$$v_2(t) = \frac{a_2 + a_1 e^{-At+B}}{a_1 + e^{-At+B}} \qquad \text{(EQ. 3.9)}$$

Where:

Once we have the expression of $v_2(t)$, we can determine t_s. Since $v_2(t)$ cannot reach v_{2ss} within a finite time, we choose $0.99\, v_{2ss}$ as a level to calculate t_s:

$$t_s = \frac{C_2}{\beta_{equ} V_f}\left[B - \ln\left|\left(\frac{0.99 v_{2ss} - a_2}{0.99 v_{2ss} - a1}\right)\right|\right] \qquad \text{(EQ. 3.10)}$$

c- Charge lost during segment 1

To determine the charge lost by the circuit during segment 1 (charge lost from capacitance C_1 and C_{equ}) we have to determine the internal node voltages at the end of segment 1. The

$$a_1, a_2 = \frac{nV_e + V_c}{n+1} \pm \left[\left(\frac{nV_e + V_c}{n+1}\right)^2 - \frac{nV_c^2}{n+1} \right]^{1/2} = V_h \pm V_f$$

$$A = \frac{\beta_{equ}(n+1)V_f}{nC_{equ}}$$

$$B = ln\left(\frac{v_2(0) - a_2}{v_2(0) - a1}\right)$$

$$V_e = V_{DD} - \alpha V_{Tn}$$

$$V_c = V_{DD} - \overline{V_{Tn}}$$

voltage at node 2 of Fig. 3.6 starts at $v_2(0)$ and equals to v_{2ss} at the end of this segment. The voltage at node 2 starts at V_{DD} and equals to $v_1(t_s)$ at the end of this segment.

$$\Delta Q_1 = C_1 [V_{DD} - v_1(t_s)] - C_{equ}[v_2(0) - v_{2ss}] \tag{EQ. 3.11}$$

$v_2(0)$ and v_{2ss} are given by EQ. 3.3 and 3.6. We need to determine $v_1(t_s)$. The expression of $v_1(t)$ in this segment is given by:

$$v_1(t_s) = C_1[v_2 + K_1 ln(v2(t_s) - a_1) + K_2 ln(v2(t_s) - a_2)] \tag{EQ. 3.12}$$

where $v_2(t), A, a1, a2$ are given in EQ. 3.8 and 3.9

$$C = \frac{AC_1\beta_1}{2}$$

$$k_1 = \frac{(a_2 - V_e)(2a_1 - V_e - a_2)}{a_1 - a_2}$$

$$k_2 = \frac{(a_1 - a_2)(2a_2 - V_e - a_1)}{a_2 - a_1}$$

The derivation of EQ. 3.12 is given in appendix A-1.

ii- Case 1, segment 2

In segment 2 all the node voltages (i.e. node 1 to node n, Fig. 3.1) have settled to a practically constant value, and T_1 is still in the saturation region.

a- Current during segment 2

Since v_2 is constant, transistor T_1 will act as constant current source. And the value of the current is given by:

$$I_{dss} = \beta_{equ}\left[(V_{DD} - \overline{V_{Tn}})v_2 - \frac{1}{2}v_2^2\right]$$

(EQ. 3.13)

b- Duration of segment 2, t_a

The voltage at node 1 will decrease at a constant rate of $\dfrac{I_{dss}}{C_1}$. Transistor T_1 will leave the saturation region when v_1 equals V_{DD} - αVTn, in other words v_1 has to drop by αV_{Tn}, Then the duration of this segment, t_a, is given by:

$$t_a = C_1 \frac{\alpha V_{Tn} - [V_{DD} - v_1(t_s)]}{I_{dss}}$$

(EQ. 3.14)

The drain current through all transistors is the same and equals to I_{dss}, and no current is flowing in or out of the node capacitances since the node voltages are almost constant.

c- Charge lost during segment 2

The Charge lost by the circuit during this stage $\Delta Q2$ is:

$$\Delta Q_2 = I_{dss}t_a$$

(EQ. 3.15)

iii- Case 1, Segment 3

In this segment all the transistors in the network are in the linear region, and the ground current will decrease from I_{dss} to 0 during this stage. Knowing the initial charge of the circuit and the charge lost during stage 1 and stage 2 we can determine the charge lost

by the circuit during this period:

a- Current in segment 3

We approximate the current to be linear. The current starts at I_{dss} and decreases linearly to 0.

b- Charge lost during segment 3

Knowing the charge lost by the circuit during segment 1 and segment 2 (i.e. $\Delta Q1$, $\Delta Q2$) we can determine the charge lost by the circuit during segment 3:

$$\Delta Q_3 = Q_{initial} - (\Delta Q_1 + \Delta Q_2) \qquad \text{(EQ. 3.16)}$$

Where

$$Q_{initial} = \sum C_i V_i (t = 0)$$

c- Duration of segment 3, t_l

If we assume that the current is decreasing linearly, knowing the initial current I_{dss} and the charge we can determine t_l as:

$$t_l = 2\frac{\Delta Q_3}{I_{dss}} \qquad \text{(EQ. 3.17)}$$

iv- Validity of case 1 model

In order to use the analytical model of case1, all nodes should have been settled to a constant voltage while T_1 is still in the saturation region. This condition is satisfied when:

$$v_1 (t = t_s) < \alpha V_{Tn} \qquad \text{(EQ. 3.18)}$$

and $v_1(t)$ is given in EQ. 3.12 and is evaluated at $t = t_s$:

$$v_1 (t_s) = C_1 [v_{2ss} + K_1 ln (v_{2ss} - a_1) + K_2 ln (v_{2ss} - a_2)] \qquad \text{(EQ. 3.19)}$$

Case 1 model is valid for large load capacitances compared to the inner nodes capacitances.

Case 2, that will be presented in the next section, is valid for small load capacitances.

v- Capacitive current modelling case 1 (summary)

Case 1 - A: $I_{init} > I_{dss}$ Case 1 - B: $I_{init} < I_{dss}$
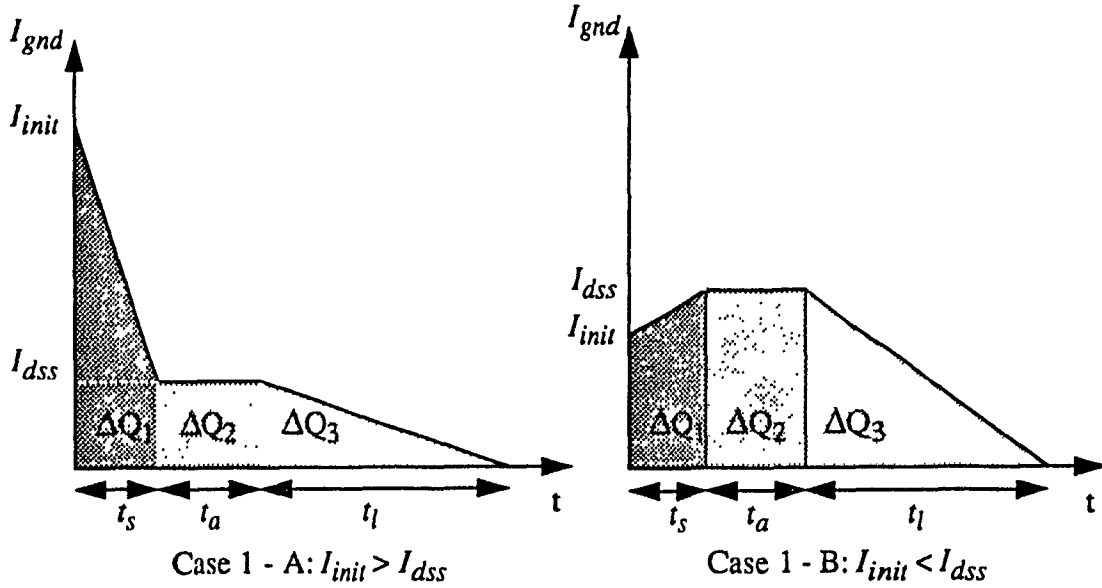
Fig. 3.7 Case 1 model summary

The average current dissipation is given by:

$$I_{avg} = \frac{1}{T} \left(\frac{(I_{max} - I_{dss}) t_s}{2} + (t_s + t_a) I_{dss} + \frac{I_{dss} t_l}{2} \right) \qquad \text{(EQ. 3.20)}$$

Where T is the period at which the gate is switched.

3.3.2- Case 2: T1 gets out of the saturation before the node voltages reach their plateau values

With reference to Fig. 3.1, in this case the top transistor T1 leaves the saturation, while the node voltages have not reached their plateau values. Fig 3.8 shows a typical case 2 circuit, where segment 2 has been reduced to zero. The top transistor will leave the saturation state if v_1 will drop by V_T, and all transistors will be in the linear region. In this case the circuit will be modelled with only two segments, segment 1 when T1 is in

saturation mode, segment 3 when T1 is in the linear mode.
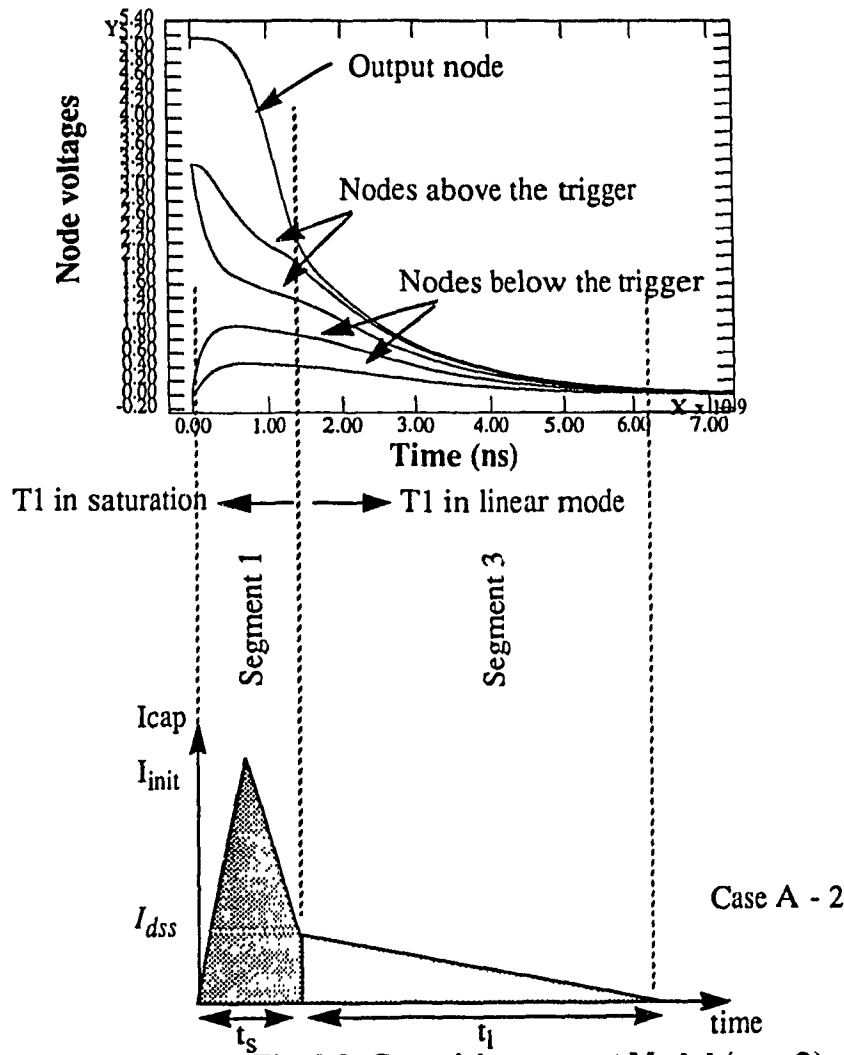
Fig. 3.8 Capacitive current Model (case 2)

i- case 2, segment 1

a- Duration of segment 1, t_s

For this case we have to determine when T1 gets out of the saturation (Fig. 3.8). The internal nodes are not settled to their plateau values. $v_1(t)$ is given by EQ. 3.12 at $t = t_s$:

$$v_1(t_s) = C [v_2 + K_1 ln (v2 (t_s) - a_1) + K_2 ln (v2 (t_s) - a_2)] = V_{DD} - V_T$$

(EQ. 3.21)

EQ. 3.21 cannot lead to a closed form solution for t_s. Knowing that t_s in case 2 is smaller

than t_s in case 1, which can be determined using EQ. 3.10, we use $t_{step} = t_s(\text{case}1)/10$ and iterate t between 0 and $t_s(\text{case}1)$ and check that the condition $v_1 (t= t_s) < V_T$ is still satisfied, if not then that value is taken as t_s. The maximum number of iterations is 10, and we can achieve a good accuracy since $v_1(t)$ is a "smooth" function of t.

b- Current at the beginning of segment 1, I_{init}

The estimation of Iinit was discussed earlier in section 3.3. and is given by EQ. 3.2.

c- Current at the end of segment 1, $I_{cap}(t_s)$

Knowing t_s, we can determine $v_2(\text{ts})$ (EQ. 3.8 and 3.9), Icap(ts) is given by:

$$I_{cap}(t_s) = \beta_{equ}\left[(V_{DD} - V_{TN}) v_2(t_s) - \frac{1}{2}v_2(t_s)^2\right] \qquad \text{(EQ. 3.22)}$$

d- Charge lost during segment 1

The charge, ΔQ_1 lost by the circuit during this stage is:

$$\Delta Q_1 = [v_1(0) - v_1(t_s)]C_1 + [v_2(0) - v_2(t_s)]C_{equ} \qquad \text{(EQ. 3.23)}$$

ii- Case 2, Segment 3

a- Charge lost by the circuit during segment 3

At this stage transistor T_1 will leave the saturation region and all other transistors will be in the linear mode. Knowing the initial charge of the circuit and the charge lost during period 1 we can determine the charge lost by the circuit during this period:

$$\Delta Q_3 = Q_{initial} - \Delta Q_1 \qquad \text{(EQ. 3.24)}$$

b- Current in segment 3

current starts at Icap(ts) and decreases linearly to 0.

c- Duration of segment 3, t_l

If we make a linear approximation of the current, since the initial current Icap(ts) and the charge $\Delta Q2$ are known then we can determine the duration t_l of this stage:

$$t_l = 2\frac{\Delta Q_3}{I_{dss}}$$

<div align="right">(EQ. 3.25)</div>

iii- Capacitive current modelling case 1 (summary)

The general model of the current for case 2 is divided into 2 basic waveforms, case 2-A where $I_{init} > I_{cap}(t_s)$ and case 2-b where $I_{cap} > I_{cap}(t_s)$. This model is valid for case 2 when T_1 leaves the saturation region and the node voltages are still charging (or discharging) to their plateau value.

Case 2 - A: $I_{init} > I_{dss}$ Case 2 - B: $I_{init} < I_{dss}$
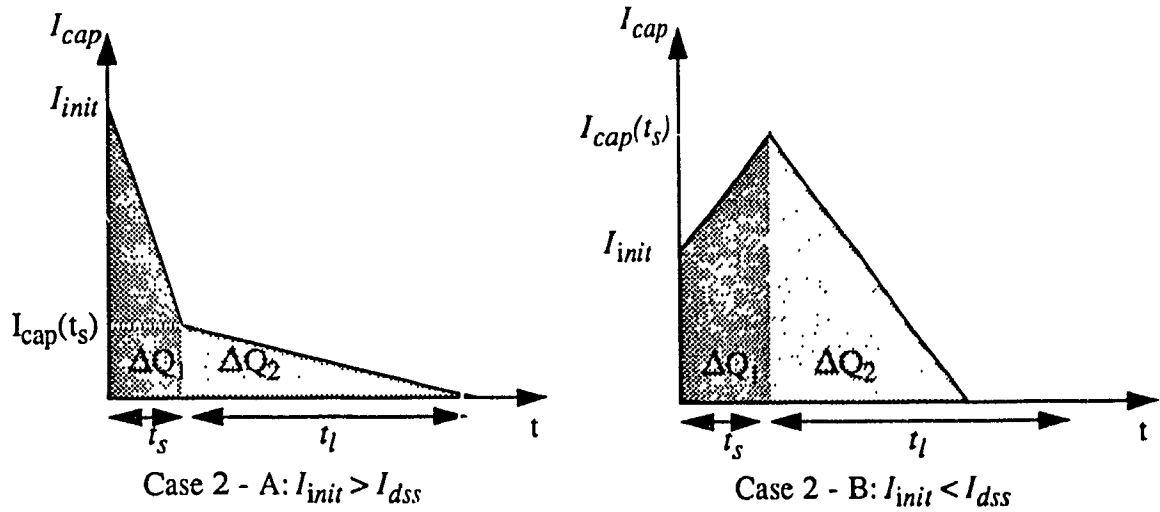
Fig. 3.9 Case 2 model summary

The average power dissipation will be given by:

$$I_{avg} = \frac{1}{T}\left(\frac{(I_{max}-I_{dss})\,t_s}{2} + t_s I_{dss} + \frac{I_{dss}t_l}{2}\right)$$

<div align="right">(EQ. 3.26)</div>

Where T is the period at which the gate is switched.

iv-Validity of case 1 model

In order to use the analytical model of case1, all nodes should have been settled to a constant voltage while T_1 is still in the saturation region. This condition is satisfied when:

<div align="center">43</div>

$$v_1 \, (t = t_s) > \alpha V_{T_n} \qquad \text{(EQ. 3.27)}$$

Case 2 is valid for small load capacitances compared to inner nodes capacitances.

3.3.3- Summary of the Model Parameters Calculations

```
┌─────────────────────────────┐
│  Calculate I_init from EQ.   │
└─────────────────────────────┘
              │
┌─────────────────────────────┐
│  Calculate v_2ss from EQ.    │
└─────────────────────────────┘
              │
┌─────────────────────────────┐
│  Calculate I_dss from EQ.    │
└─────────────────────────────┘
              │
┌─────────────────────────────┐
│  Calculate t_s from EQ.      │
└─────────────────────────────┘
              │
┌─────────────────────────────┐
│  Calculate v_1(t_s) from EQ. │
└─────────────────────────────┘
```

Case 1	Case 2
Calculate ΔQ_1 from EQ.	Recalculate t_s from EQ.
Calculate t_a from EQ.	Calculate $I_{cap}(t_s)$ from
Calculate ΔQ_2 from EQ.	Calculate ΔQ_1 from EQ.
Calculate ΔQ_3 from EQ.	Calculate ΔQ_3 from EQ.
Calculate t_l from EQ.	Calculate t_l from EQ.
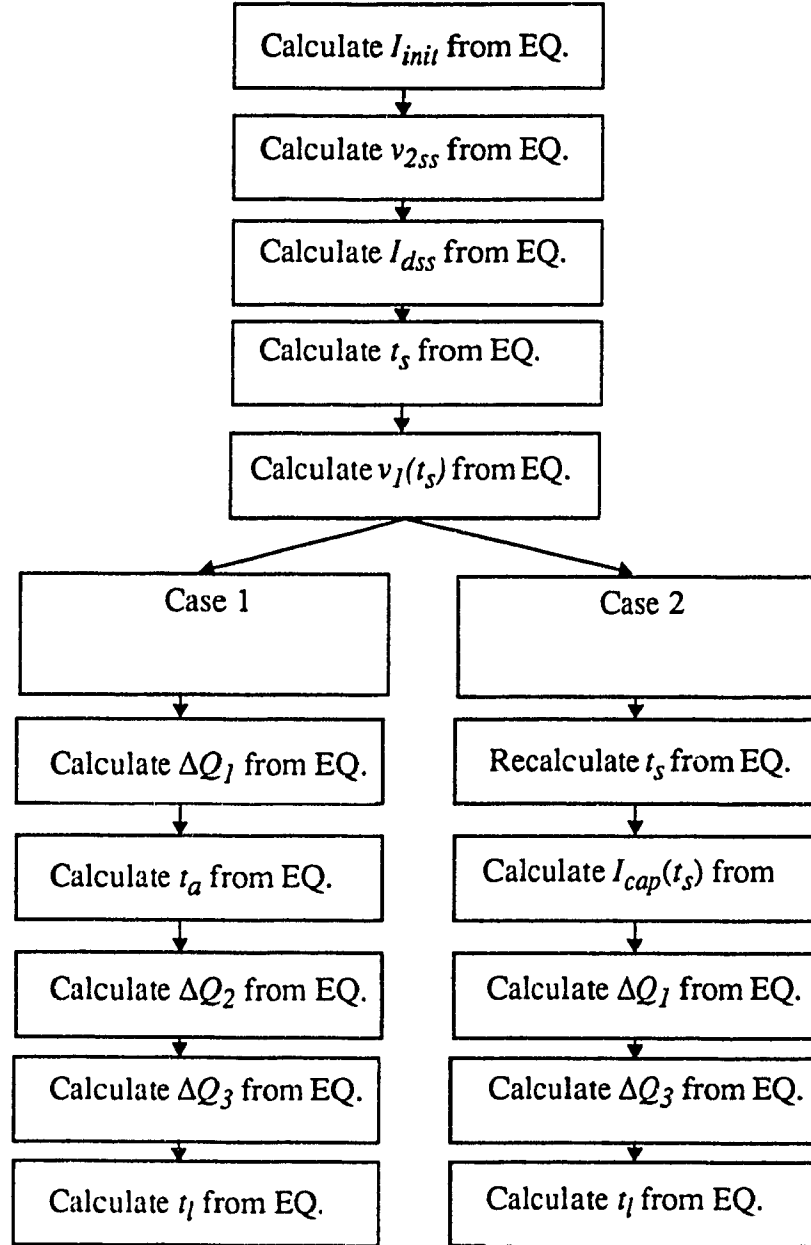
3.4- Circuit Analysis for a Ramp Input

The model strategy for a ramp input is to build on the model derived for a step input as shown in Fig. 3.10. The input signal slope affects the ground current waveform during the rise time. During this time some model parameters, derived for a step input, are affected. When the input reaches V_{DD}, the same model derived for a step input is used. For the case of a ramp input, we have to take in consideration the short-circuit power dissipation. The short-circuit power dissipation is in general less than 20% of the total power depending on the load and the input rise time [7]. Therefore the output voltage is mainly determined from the dynamic power dissipation. The pull-up current can be neglected when determining the output voltage. Still this voltage can be used to calculate approximately the short-circuit power dissipation [8]. Although this means that we neglected the short-circuit power dissipation when both transistors are conducting, it is an acceptable approximation as long as the short-circuit power dissipation is small compared to the power needed to charge the output node capacitor [7]. The additional parameter we have to determine is the charge, ΔQ_0 contributed by the pull-up during the transition time (Fig. 3.10).

The short-circuit current effect is included by adding the pull-up current estimated to the ground current. In order to determine the pull-up current we use the equivalent circuit shown in Fig. 3.11, where all the pull-down transistors are collapsed to a single transistor Tn and the pull-up transistors are collapsed to Tp. We use the same approach derived in [7]. This approach is to estimate the output voltage neglecting Ip and still use the results to estimate Ip. This a valid approximation as long as the short-circuit power dissipation is small compared to the dynamic power dissipation.
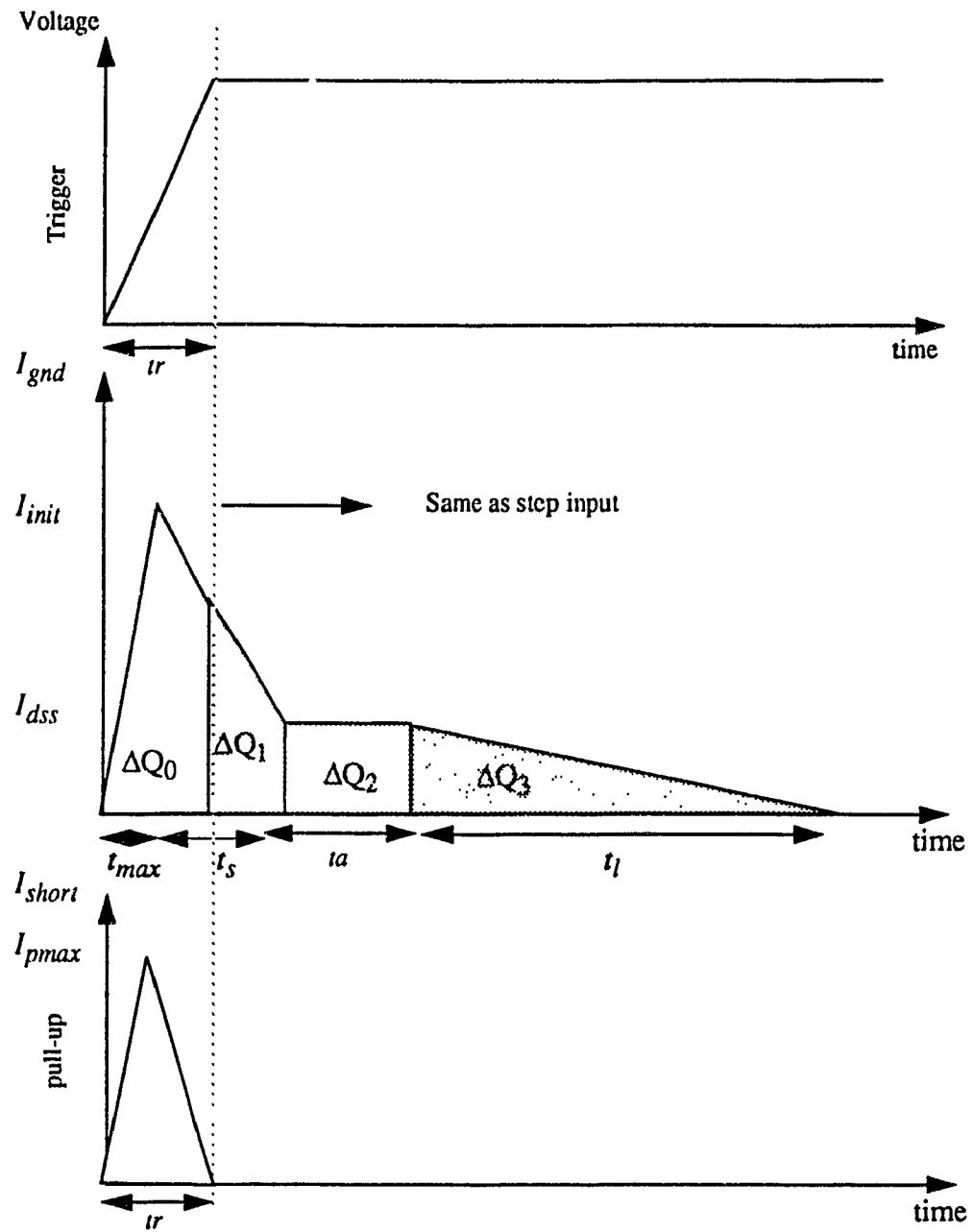
Fig. 3.10 Current modelling for a ramp input
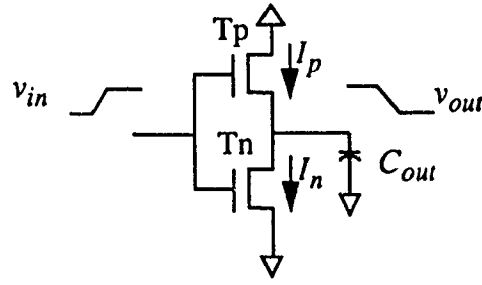
Fig. 3.11 Equivalent circuit for short-circuit power estimation

3.4.1- Closed-form solution of v_{out}

The analytical analysis of an inverter with a ramp input is derived in [7], the closed form solution of the output voltage are given for the following two regions of operation:

(1) Pull-down in the saturation region

$$v_{out} = 1 - \frac{\beta_{equ}}{2C_{equ}s}(st - V_{TN})^3 \qquad \text{(EQ. 3.28)}$$

(2) Pull-down in the linear region

Two cases are identified:

a- input is still a ramp

In this case v_{out} is given by:

$$\frac{1}{v_{out}} = e^{\frac{\beta_{equ}V_{DD}}{2C_{equ}s}(st-V_T)^3}\left[\frac{1}{v_{sat}e^{\frac{\beta_{equ}V_{DD}v_{sat}^2}{2C_{equ}s}}} + \sqrt{\frac{\pi\beta_{equ}V_{DD}}{8C_{equ}s}}\left(erf\left(\sqrt{\frac{\beta_{equ}V_{DD}v_{sat}}{2C_{equ}s}}\right) - erf\left(\sqrt{\frac{\beta_{equ}V_{DD}(st-V_T)^2}{2C_{equ}s}}\right)\right)\right]$$

$$\text{(EQ. 3.29)}$$

Where:

$$v_{in} = st$$

$$s = \frac{V_{DD}}{tr}$$

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v_{out}, v_{sat}, V_T are normalized to V_{DD}.

v_{step} is defined as the value of v_{out} when the input reaches V_{DD}.

v_{sat} is defined as the output voltage when Tn switches from the saturation region to the linear region, and is given by:

$$v_{sat} = 1 - \frac{\beta_{equ} V_{DD}}{6s C_{equ}} v_{sat}^3$$

b- input reaches V_{DD}

In this case v_{out} is given by:

$$\frac{1}{v_{out}} = \frac{1}{V_{DD} - V_T} \left[\frac{1}{2} + \left(\frac{V_{DD} - V_T}{v_{step}} - \frac{1}{2} \right) e^{(t - tr) \beta_{equ} (V_{DD} - V_T)} \right] \qquad \text{(EQ. 3.30)}$$

3.4.2- Short-circuit current

Once the output voltage V_{out} is known the pull-up current (short-circuit current) is solved and we get:

$$I_P = \begin{cases} \beta_p \left[(v_{in} - V_{DD} - V_{TP})(v_{out} - V_{DD}) - \frac{(v_{out} - V_{DD})^2}{2} \right] & \text{for } v_{in} - V_{TP} < v_{out} \\ \\ \frac{\beta_p}{2} (v_{in} - V_{DD} - V_{TP})^2 & \text{for } v_{in} - V_{TP} > v_{out} \end{cases}$$

$$\text{(EQ. 3.31)}$$

Iterating EQ. 3.30 between 0 and t_r, using tstep $= t_r/10$ we can determine the pull-up peak current Ipmax in 10 iterations.

3.4.3- The effect of the input rise time on I_{init}

The input slope affects I_{init} and its timing. We estimate this value using the same method used for the step input. All transistors from the trigger to the ground are collapsed into T_{equ}, and all the corresponding node capacitance are lumped into C_{equ}. The effect of the

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transistors between the trigger and the output node is neglected (Fig. 3.12).
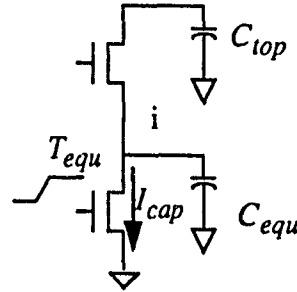
Fig. 3.12 Iinit estimation for a ramp input

The equations derived for this circuit are the same as EQ. 3.28, 3.29 and 3.30. The current during the saturation is an increasing function of the time, as shown in EQ. 3.31, then the peak current occurs during the linear region. The voltage in the linear region is given by EQ 3.28, 3.29. Therefore the current is given by:

a- Tequ in the saturation region

$$I_{cap} = \frac{\beta_{equn}}{2} (st - V_T)^2 \qquad \text{(EQ. 3.32)}$$

b- Tequ in the linear region

$$I_{cap} = \beta_{equ} \left[(st - V_T) V_i - \frac{V_i^2}{2} \right] \qquad \text{(EQ. 3.33)}$$

Where v_i is given by EQ. 3.27, 28 and 3.29 replacing v_{out} with v_i.

In order to find the peak value of the current and the timing of the peak EQ. 3.32 is iterated from t_{sat} to tr. Where t_{sat} is defined as the time when Tequ gets out of the saturation, and t_r is the input rise time. t_{sat} is given by:

$$t_{sat} = \frac{V_{sat} + V_T}{s} \qquad \text{(EQ. 3.34)}$$

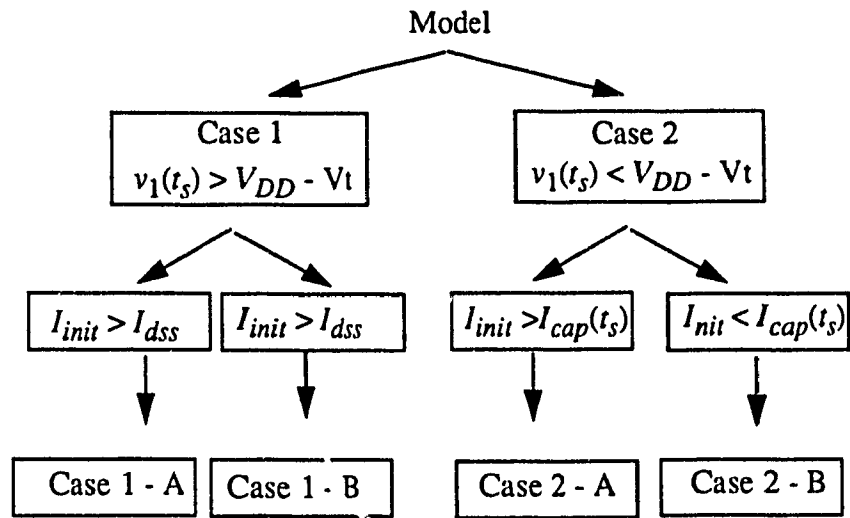Finally in order to include the effect of the short-circuit power dissipation the pull-up

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current waveform is added to the ground current waveform.

3.5- Delay and Output Rise/Fall Time Estimation

In order to estimate the delay in a CMOS gate, the gate is collapsed into an equivalent inverter. The delay is defined as the difference in time between when the input reaches 50% of V_{DD} and the time the output reach 50% of V_{DD}. Equations 3.27, 3.28 and 3.29 describe the output voltage. When the output node reaches $0.5*V_{DD}$, Tn will be in the linear region. Therefore in order to have an expression for the delay we have to resolve EQ. 3.28 or 3.29 for t, unfortunately we can't have a closed form solution for t at $v_{out} = 50\%$ V_{DD}. The same argument applies to the estimation of the output fall time, which is defined as the difference between the time the output is at 90% of V_{DD} and the time it reaches 10% of V_{DD}. Since Tn will be in the linear region when the output will be at $0.1*V_{DD}$, then to estimate the propagation delay and fall time EQ. 3.27, 3.28 and 3.29 are numerically evaluated for a defined time step to have an accurate delay and output rise/fall time. The time step can be fixed to Δt in order to estimate the delay to in order to estimated the delay Δt accuracy. A macro model of RC time constant is used to evaluate Δt. For practical delay and output rise/fall time the number of iterations should not exceed 20 iterations. We cannot use in this case a simple RC model for the estimation of the propagation delay and rise/fall time, because the rise/fall time particularly has an effect on the current shape and need to be estimated accurately.

3.6- Discussion

Our model has been presented, it is based on basic current waveforms determined analytically from CMOS circuits and is summarized in Fig. 3.13. To prove the validity of our model, in the next Chapter we present a detailed comparison between our model and SPICE for different circuits.

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Model

Case 1	Case 2
$v_1(t_s) > V_{DD} - V_t$	$v_1(t_s) < V_{DD} - V_t$

$I_{init} > I_{dss}$	$I_{init} > I_{dss}$	$I_{init} > I_{cap}(t_s)$	$I_{nit} < I_{cap}(t_s)$

Case 1 - A	Case 1 - B	Case 2 - A	Case 2 - B

Fig. 3.13 Model summary for a high to low switching of a CMOS gate

CHAPTER 4

Comparison of Analytical Supply Current with SPICE for Long-Channel MOSFETs

4.1- Introduction

In order to verify the accuracy of our model, we will compare it to SPICE level 3. The comparison is made for different kinds of complex circuits, and by varying all the parameters that affect the current. The current depends on the load capacitance, the node capacitances, the transistor switched, transistor sizes and input rise time. By varying these parameters we can quantify the difference between our model and SPICE, and prove its validity. In Section 4.2 we perform time-domain current waveform comparisons between SPICE and our model on a 5-input nand gate, and by varying different circuit parameters. Also a comparison of the peak current and average current is done. In Section 4.3 we analyze a dynamic-logic circuit with pass gates. In Section 4.4 we perform comparisons on the supply current waveforms in a carry look-ahead adder circuit. In Section 4.5 a comparison of the supply current for a parity generator are made. The model results showed a good agreement with SPICE estimates for the circuits described. Our results give an overall 10% deviation from SPICE.

4.2- 5-Input Nand Gate

In this section we compare our model to SPICE for a 5-input nand gate (Fig 4.1). The transistors channel length is 3 microns. The comparison is done for the capacitive current and the short circuit current used to derive the supply current. For the purpose of proving our model we added the node capacitances as shown in Fig. 4.1.
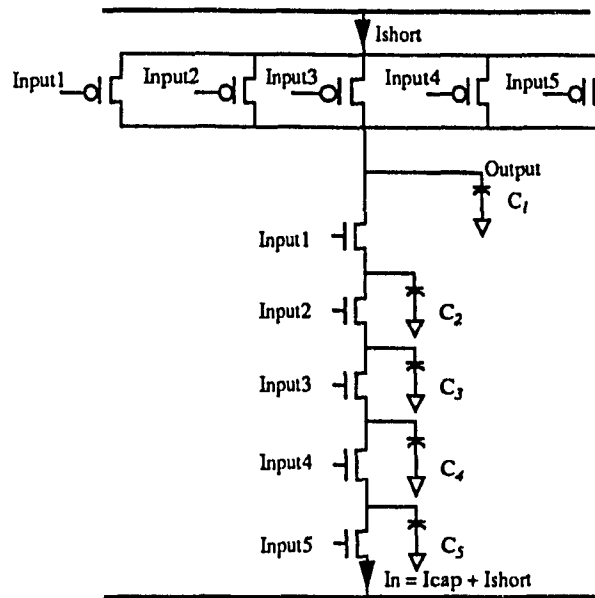
Fig. 4.1 5-input nand gate

4.2.1- Effect of the load capacitance on the current

The effect of the load capacitance on the current is shown by varying C1 (1 fF, 10 fF, 50 fF, 100 fF, 200 fF). Transistor T5 is switched with a rise time of 1ns and all the other inputs are kept high. The short-circuit current for a 1ns input rise time is negligible and the current is mainly capacitive. The model and SPICE results are shown in Fig. 4.2. The model results give a good agreement with SPICE as shown in Fig. 4.3.
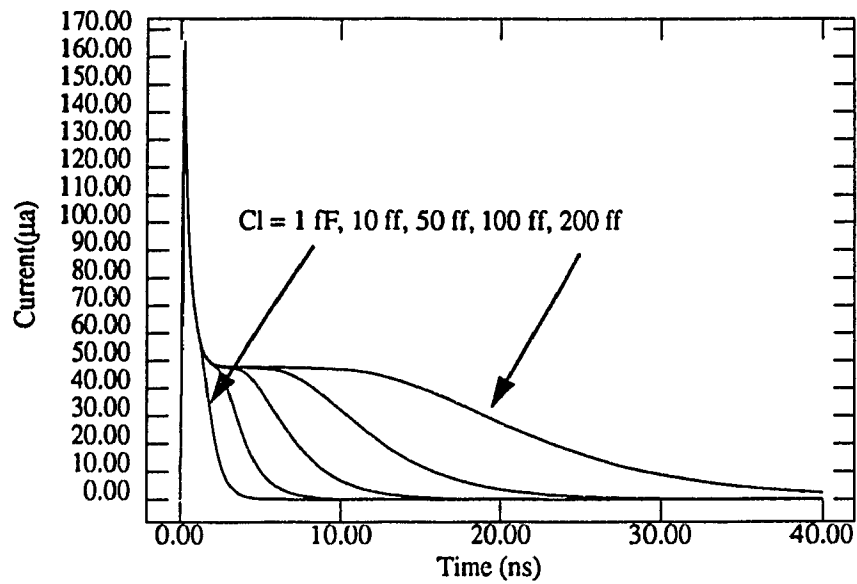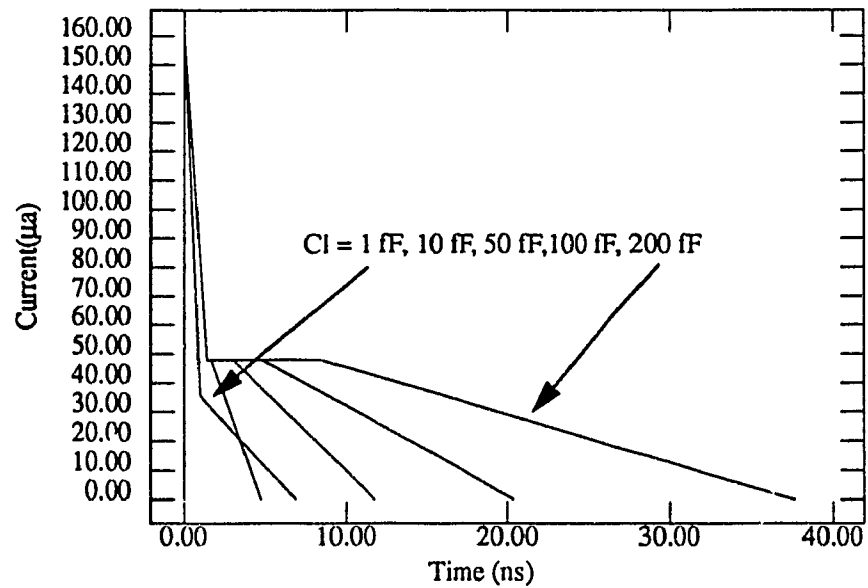
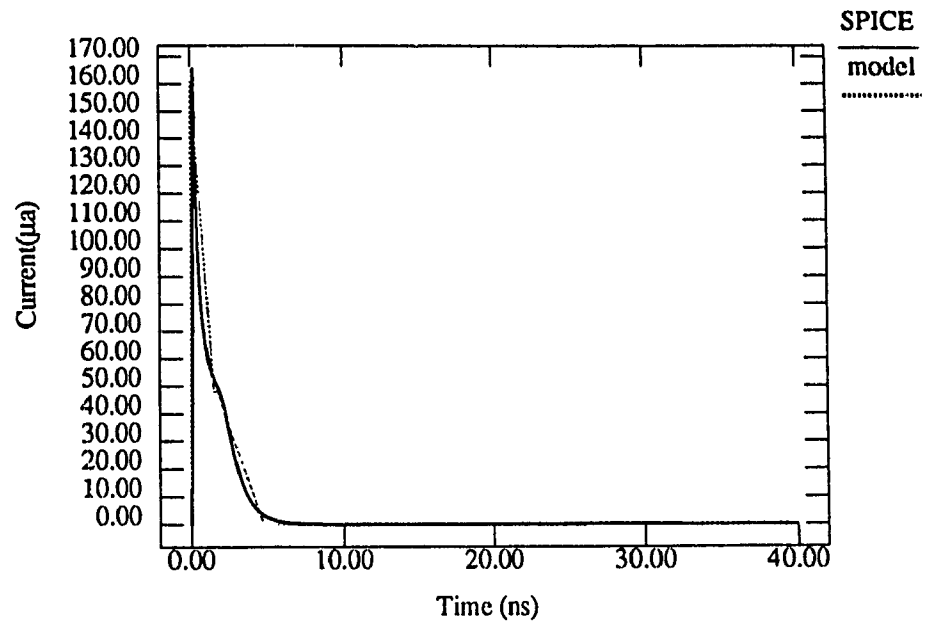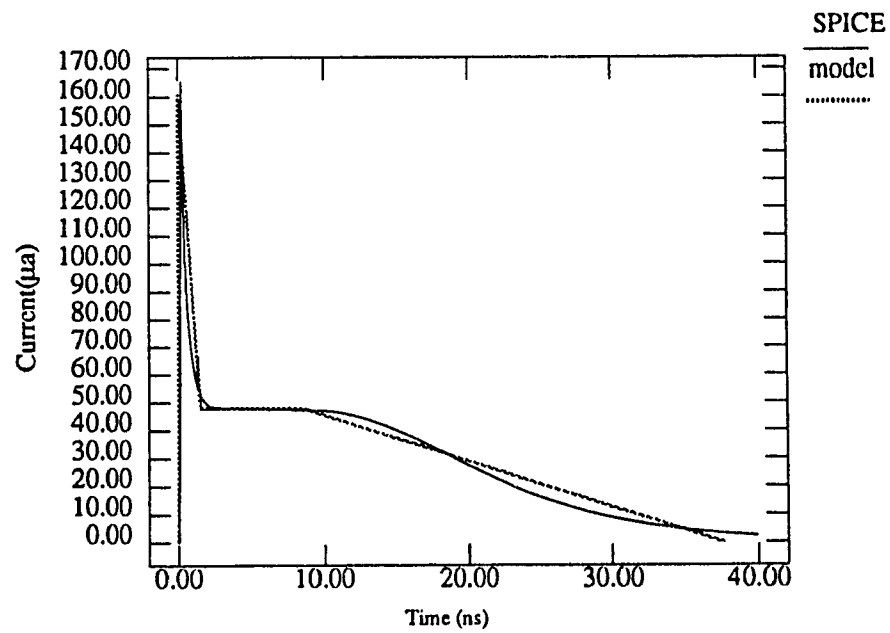Fig. 4.2 Time-domain current waveforms for different loads

a- C1 = 1 fF

b- C1 = 200 fF

Fig. 4.3 Comparison between the proposed model and SPICE

A more detailed comparison between SPICE and our model is shown in Fig. 4.4 and the difference is shown in Fig. 4.5. The average current increases linearly with the load capacitance. There's a step difference between the curves for different transistors switched, because some node capacitances will be charged or discharged depending on which transistor is switched. An empirical factor for small loads is introduced. The load capacitance is multiplied by $1+A\dfrac{C_o}{C_{load}}$, where A is an empirical factor (A $\approx$ 2.0 for this process), and C_0 is the gate to drain capacitance. Fig. 4.4 shows an excellent agreement between SPICE and our model, the percentage difference is less than 1% as shown in Fig. 4.5.
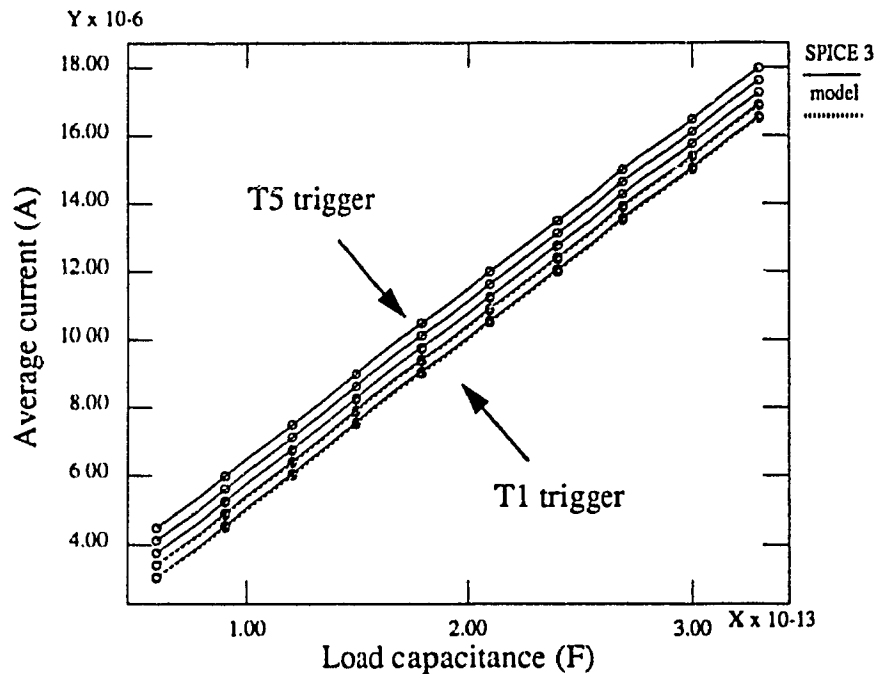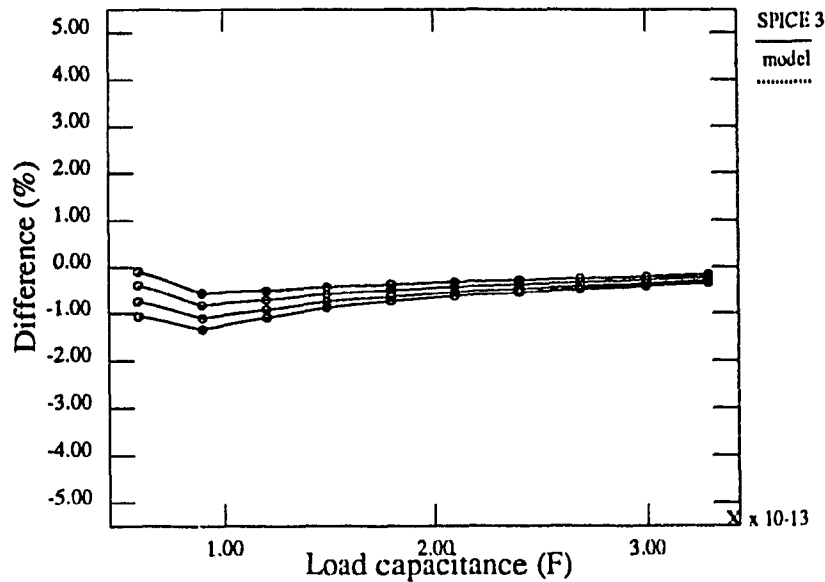

Fig. 4.4 Average capacitive currents for different loads

Fig. 4.5 Difference between SPICE and model for different loads

The effect of the load capacitance on the peak current is shown in Fig. 4.6. The peak current is not affected by the load capac'tance, because the bottom transistor is switched and especially for fast rising time input, the peak current is only dependent on the capacitance just above the trigger transistor. The physical explanation is that the node transistors will have a tendency to discharge one after the other for fast inputs. The peak current is dependent on the trigger transistor as shown in Fig. 4.6. As discussed in Section 3.2 the peak current can be equal to either I_{init} or I_{dss}. I_{dss} is independent of the load capacitance (EQ. 3.7). I_{init} depends on the node capacitances and is affected by C_l and is more difficult to estimate. The model gives an acceptable approximation of the peak, and the percentage difference is less than 10% as shown in Fig. 4.7.
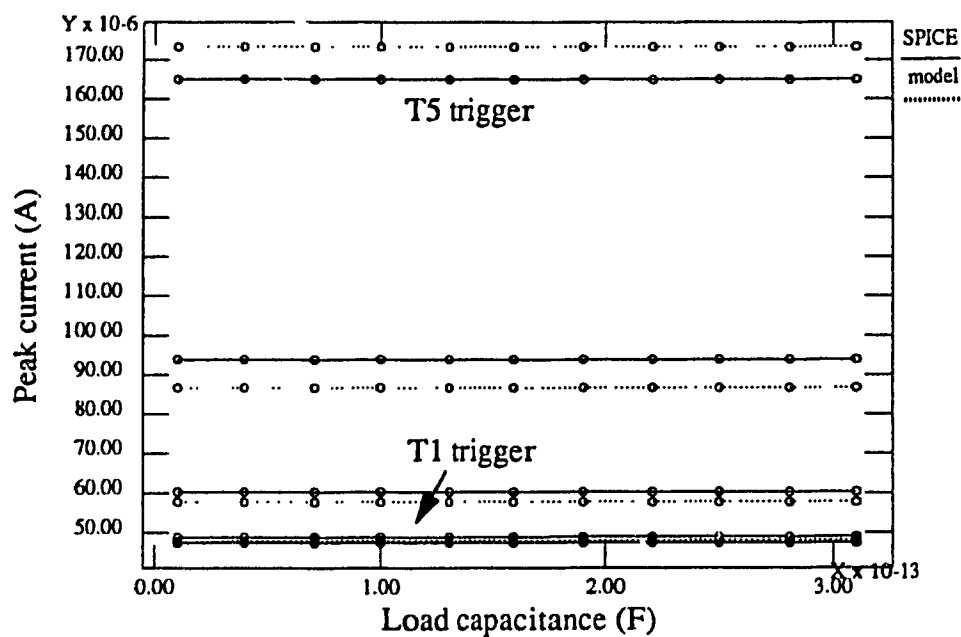
Fig. 4.6 Peak capacitive current for different loads
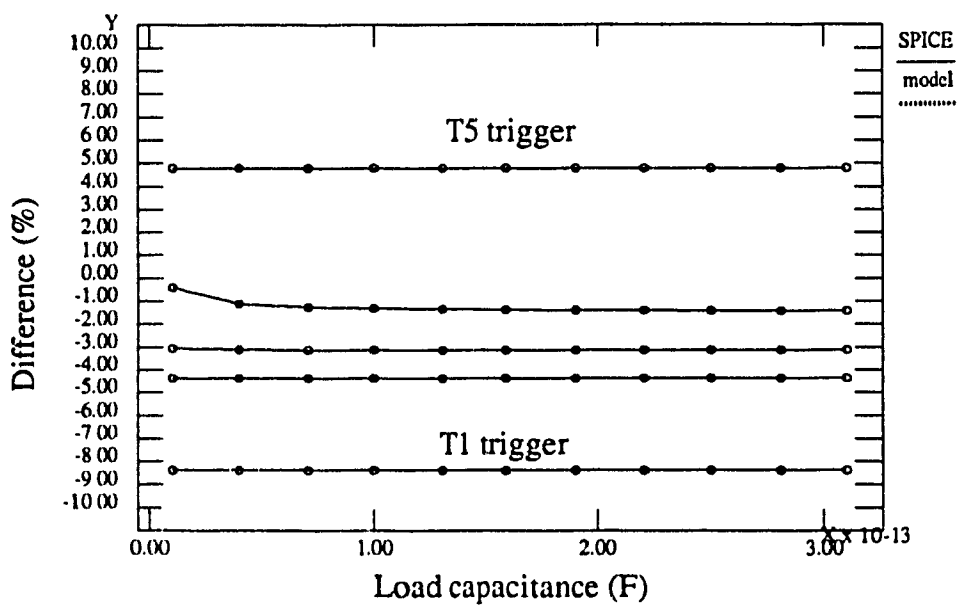
Fig. 4.7 Difference between SPICE and the model for different loads

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4.2.2- Effects of nodes capacitances on the current

The effect of the node capacitance on the current parameters is shown in Fig. 4.8 by varying C3 and taking T1 as the trigger (Fig. 4.1). The Average current increases linearly with C3 when a transistor bellow C3 is switched (T1, T2, T3) since C3 is charged before the switching in these cases. The Average current is independent of C3 when a transistor above C3 is switched (T1, T2), since C3 is not charged before switching. Fig. 4.9 shows less than 2% difference between our model and SPICE (Fig. 4.9). Fig. 4.10 show a comparison of the current waveform for C3 = 1fF.
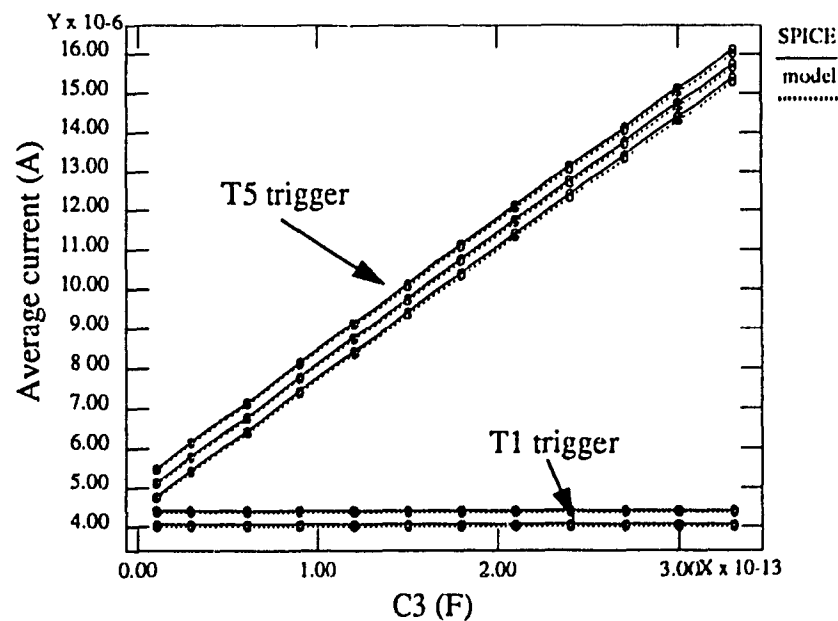
Fig. 4.8 Average capacitive current for different C3 values

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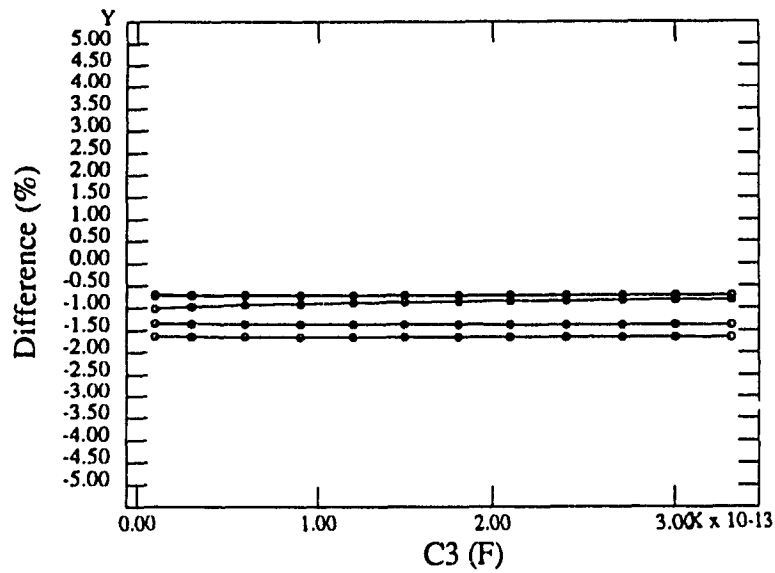
Fig. 4.9 Difference between SPICE and model for different C3 values
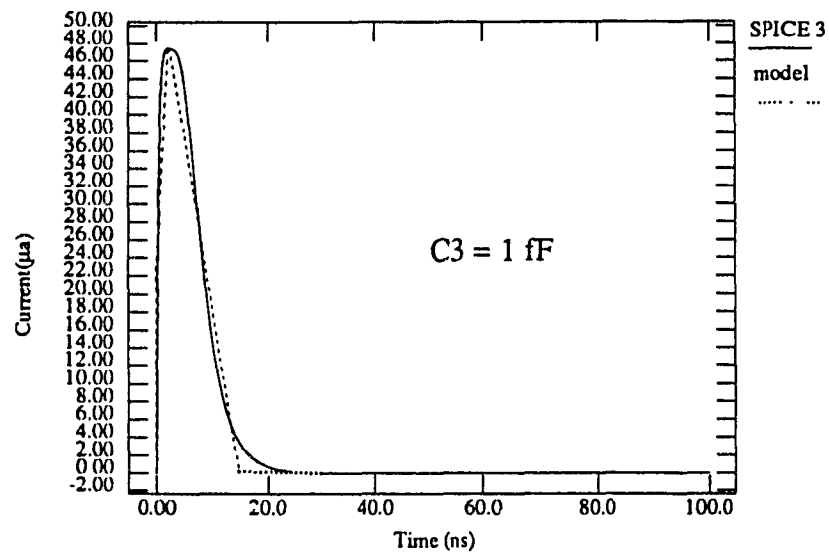
Fig. 4.10 Comparison between SPICE and model for C3 = 1fF

4.2.3- Effects of the trigger on the current

The effects of the transistor switched on the peak and average current are shown in Fig. 4.11 and 12. The peak and average current are higher when a transistor closer to the ground is triggered.
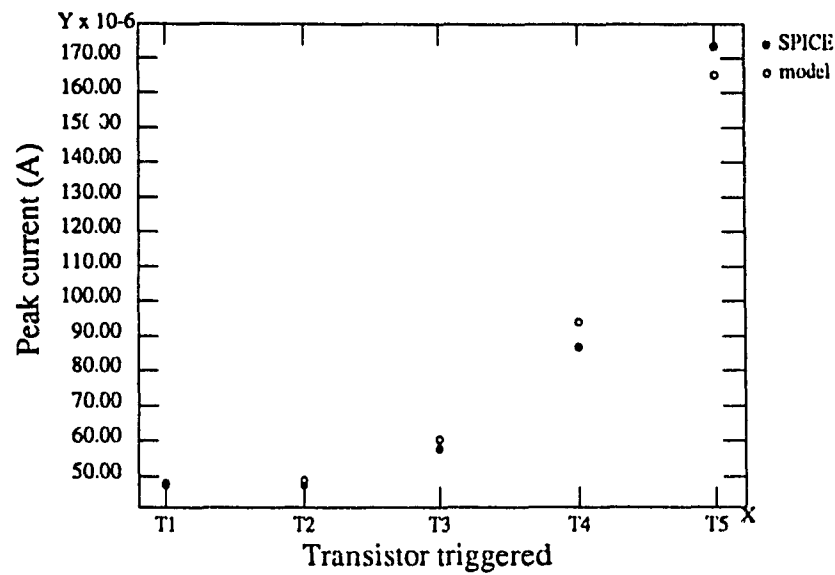
Fig. 4.11 Effect of transistor switching on the peak capacitive current
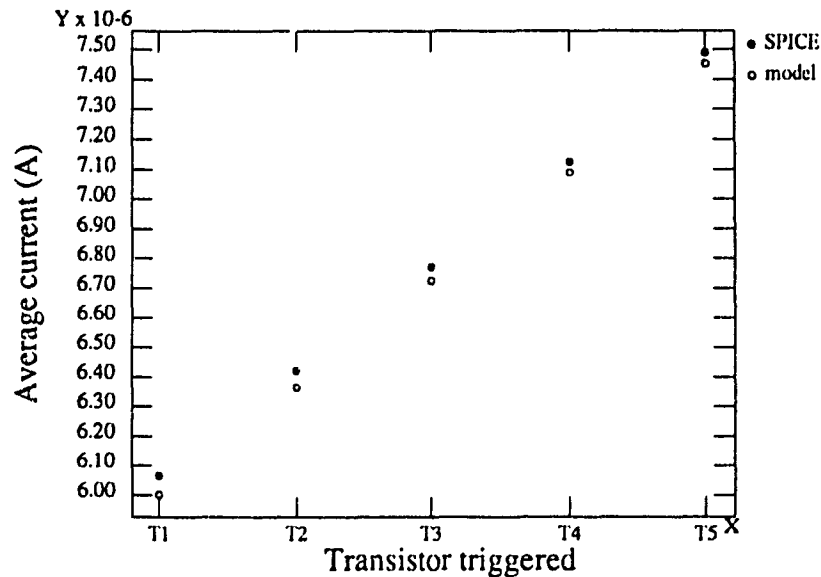
Fig. 4.12 Difference between SPICE and the model for different trigger

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4.2.4- Effect of the input rise time on the current

The effect of the input rise time on the average and the peak current is shown in Fig. 4.13 and 14. The average power dissipation increases with input rise time, because the short-circuit power dissipation increases. The peak current decreases for slower input transitions as shown in Fig. 4.14.
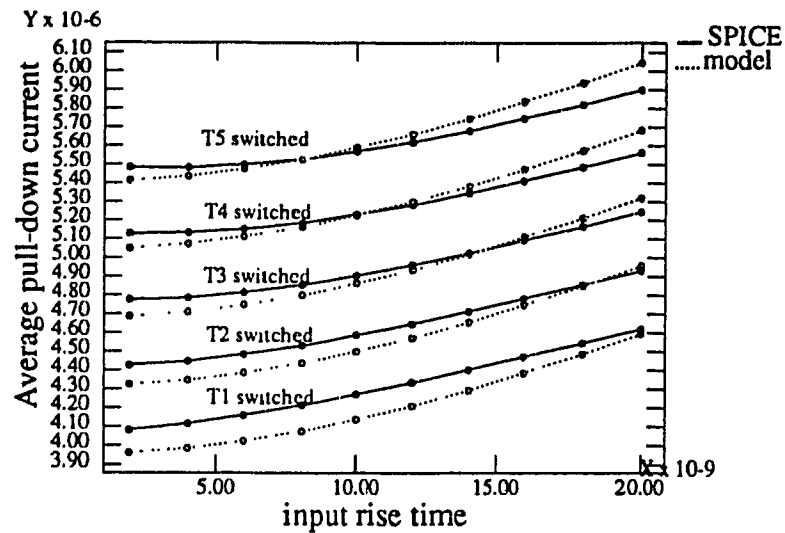
Fig. 4.13 Effects the input rise time on the average pull-down current
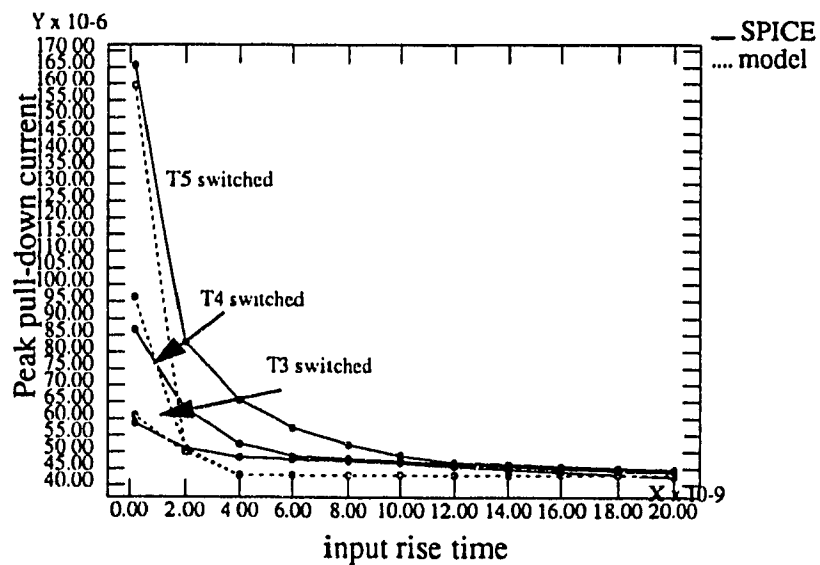
Fig. 4.14 Effects of input rise time on the peak pull-down current

Short-circuit current

The pull-up current (short-circuit) is dependent on the input rise time as shown in Fig. 4.15 and 4.16. The short-circuit current model does not take in account the effects of the transistor triggered (Fig. 4.15 and 4.16). This is due to the collapsing of the circuit to an equivalent inverter to estimate the short-circuit current. The information about which transistor is triggered is lost in the collapsing.
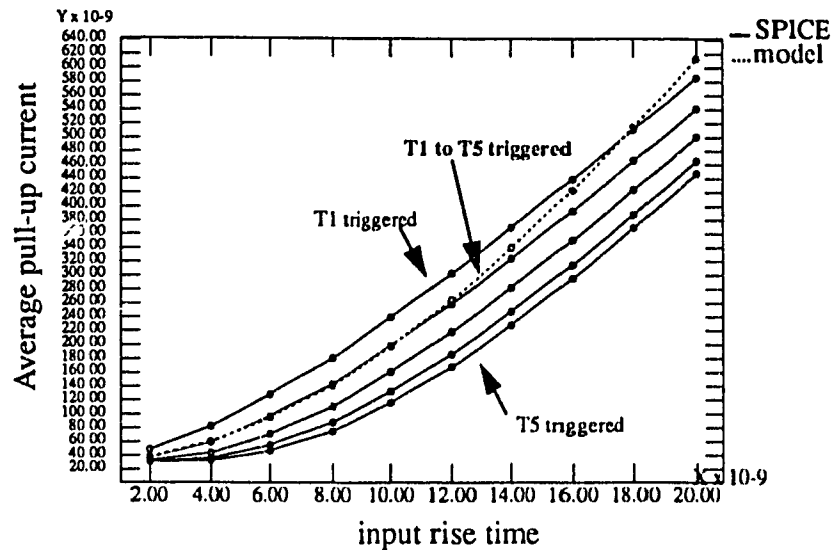
Fig. 4.15 Effects of input rise time on the average short-circuit current
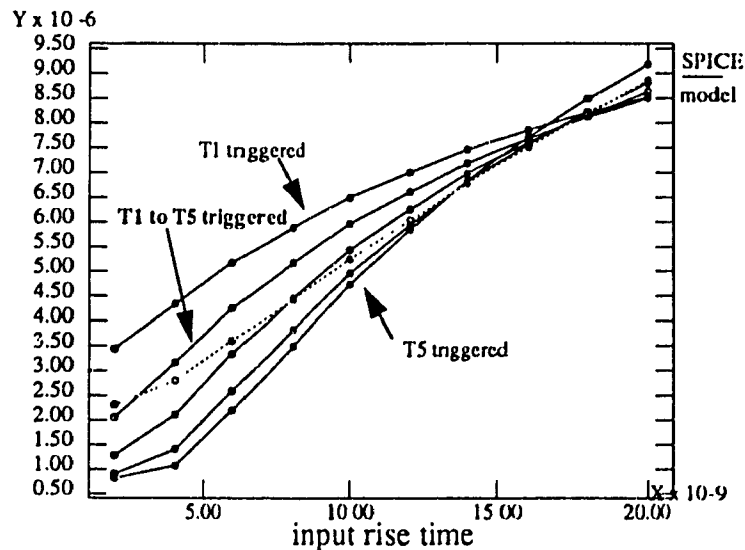
Fig. 4.16 Effects of input rise time on the short-circuit peak current

4.3- Stage with pass gates

In this Section we compare our model to SPICE for a dynamic-logic circuit with a pass gate, using 2-phase clocking (Fig 4.17). The transistor's channel length is 3 microns. The short-circuit current is negligible since the clock ϕ_1 has a small rise time (Fig. 4.17). A comparison between SPICE and our model waveforms is shown in (Fig. 4.18).
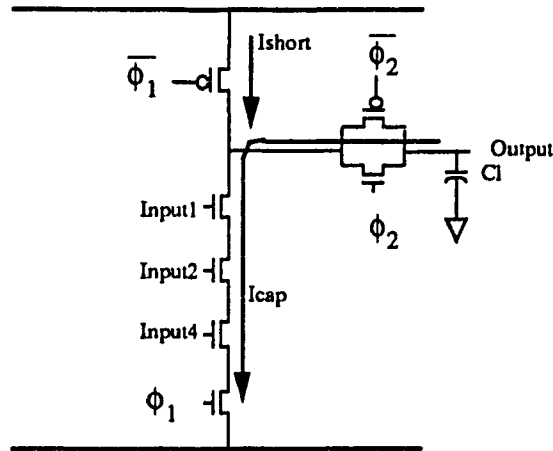
Fig. 4.17 Dynamic-logic circuits

a- SPICE
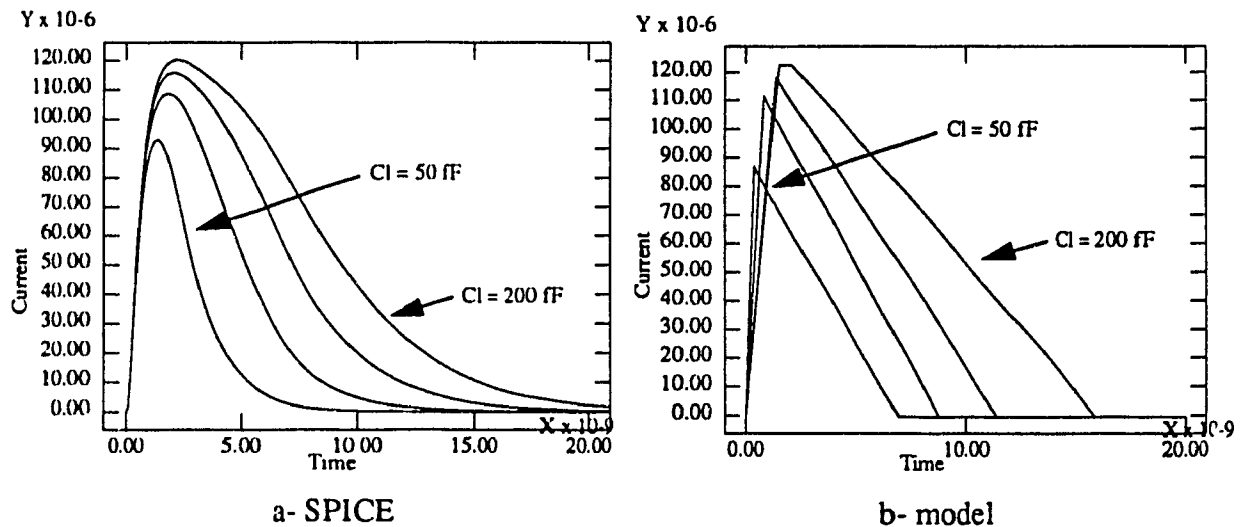
b- model

Fig. 4.1 Currents in a dynamic-logic circuit for different loads

4.4- Carry Look-Ahead Adder Circuit

In order to test the developed model with a circuit of different topology and complexity, we have tested our model with a carry look ahead-adder (Fig. 4.19) under different input conditions. The node capacitances are estimated from the gate, source and drain capacitances of the transistors. The circuit is divided into stages and an event-driven simulation (Fig 4.20) is performed, at the end all the current waveforms are combined to obtain the supply current. Fig 4.21 a, b, c shows a good agreement between SPICE and model estimates for the supply current.
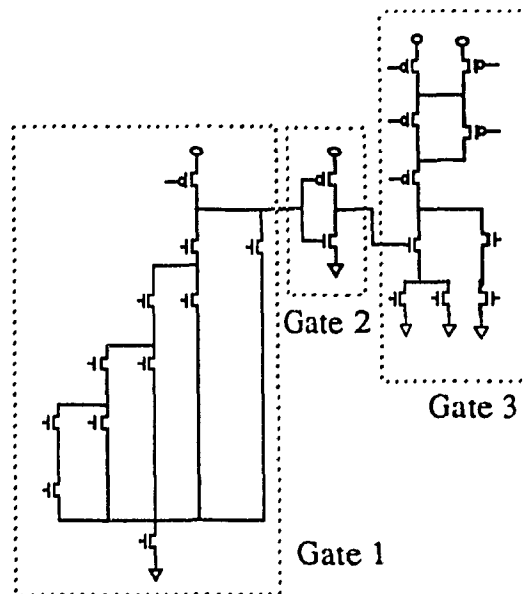
Fig. 4.19 Carry look-ahead adder
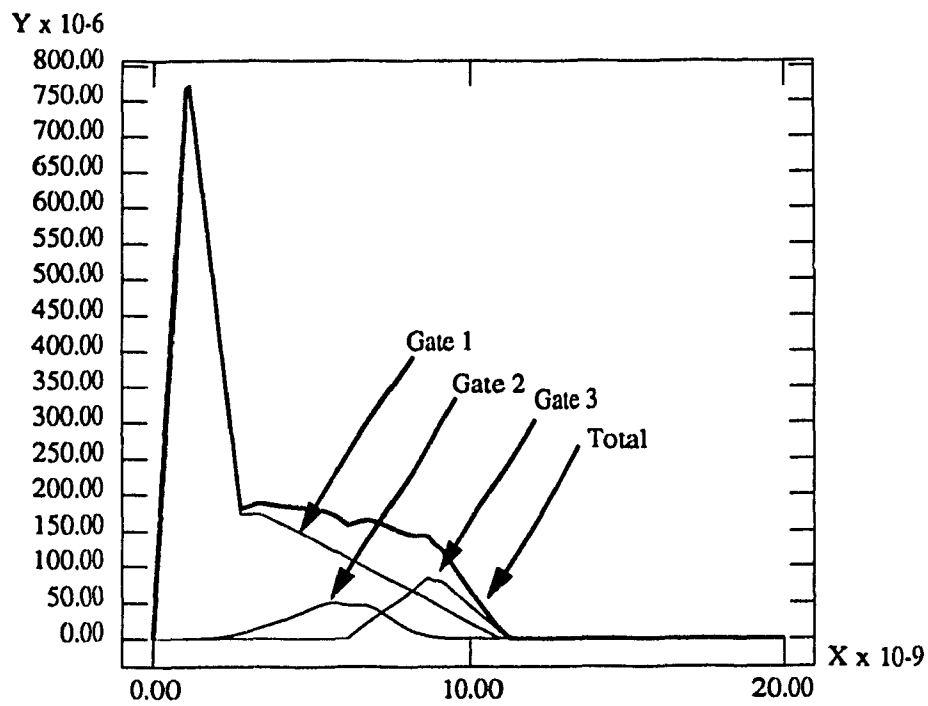
Fig. 4.20 event-driven simulation

Labels in figure: Y x 10-6, 800.00, 750.00, 700.00, 650.00, 600.00, 550.00, 500.00, 450.00, 400.00, 350.00, 300.00, 250.00, 200.00, 150.00, 100.00, 50.00, 0.00; Gate 1, Gate 2, Gate 3, Total; X x 10-9; 0.00, 10.00, 20.00
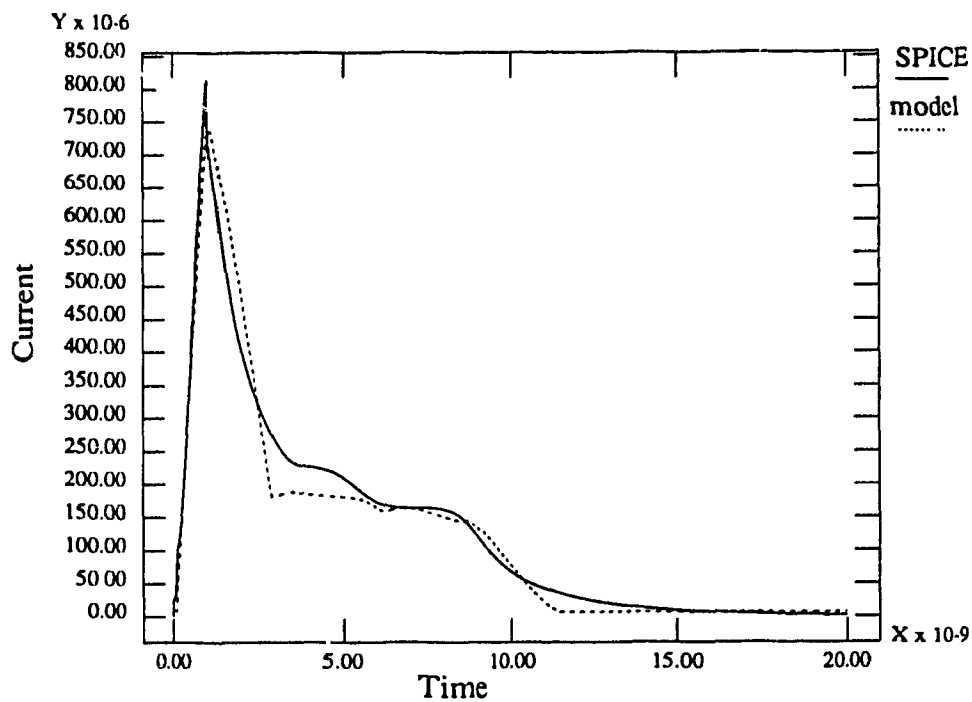
Fig. 4.21.a Supply currents for different input vectors

Labels in figure: Y x 10-6, 850.00, 800.00, 750.00, 700.00, 650.00, 600.00, 550.00, 500.00, 450.00, 400.00, 350.00, 300.00, 250.00, 200.00, 150.00, 100.00, 50.00, 0.00; Current; SPICE, model; X x 10-9; 0.00, 5.00, 10.00, 15.00, 20.00; Time
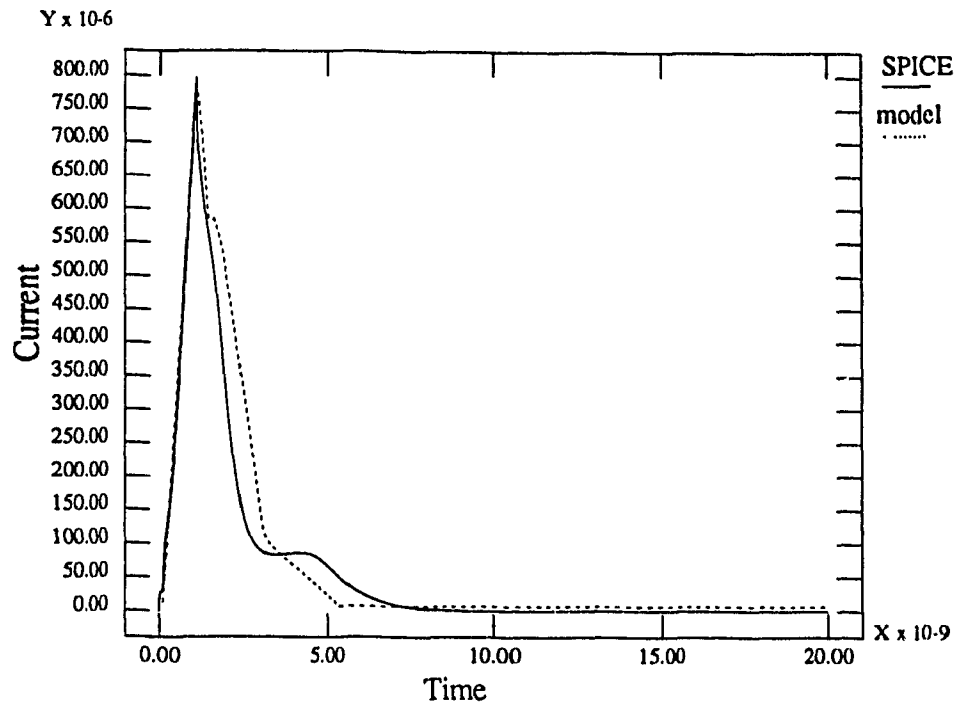
Fig. 4.21.b Supply currents for different input vectors
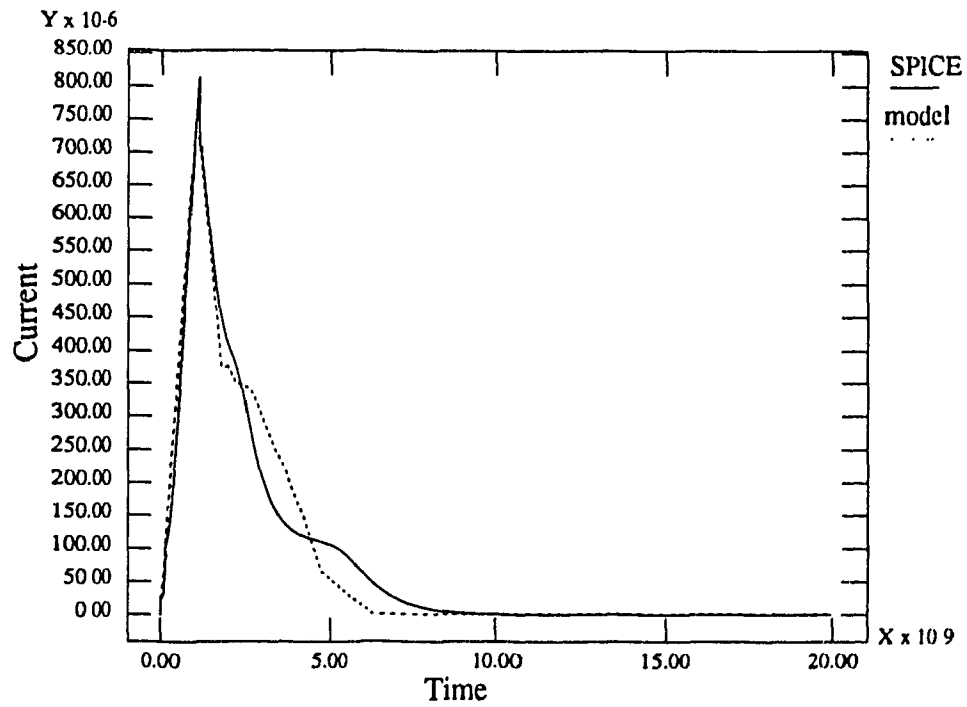
Fig. 4.21.c Supply currents for different input vectors

4.5- Parity Generator

A comparison between our model and SPICE is performed for a parity generator circuit of Fig. 4.22. This circuit has a topology different from the previous two circuits tested. The model is applied to the circuit, although it is not complementary CMOS logic. The results are shown in Fig 4.23 for the charging and discharging of the output node. The average current is within 10% of SPICE estimates and the peak is within 20%.
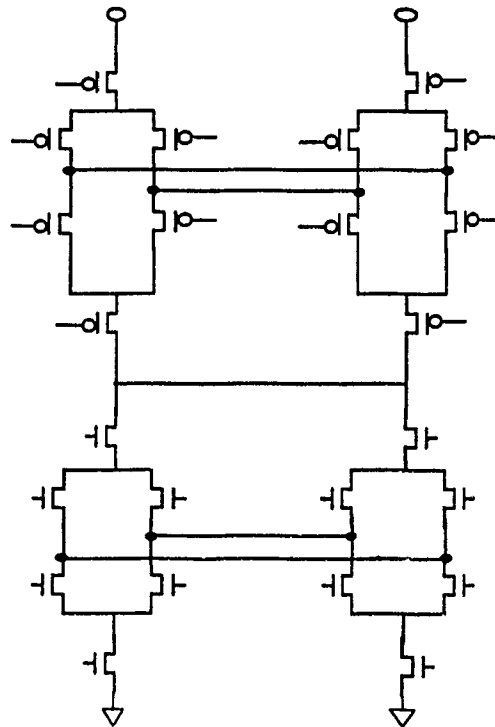
Fig. 4.22 Parity generator circuit
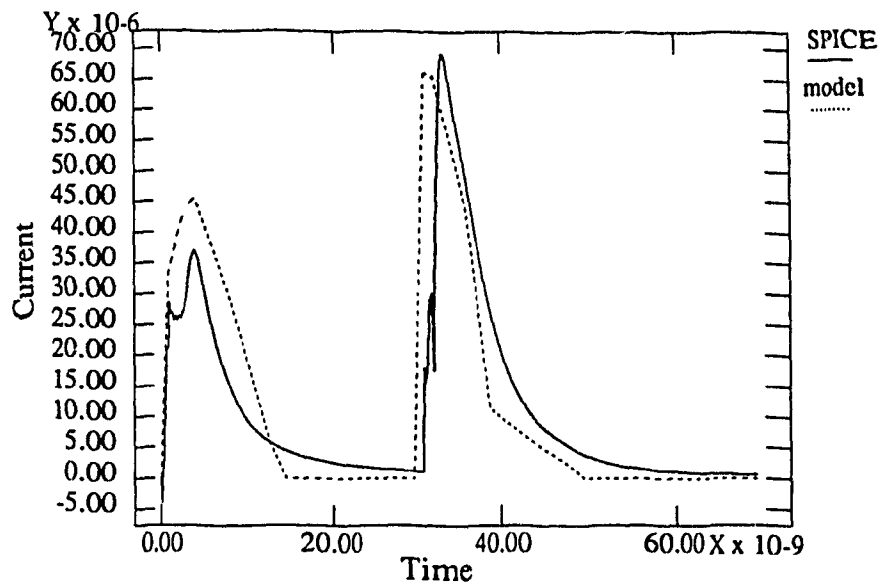
Fig. 4.23 Supply current of a parity generator circuit

4.6- Discussion

We have presented an overall comparison between SPICE and our model for various CMOS circuits of different topology and complexity, and have shown that the percentage difference between our model and SPICE are within 10%. In the next chapter we will discuss the short-channel effects, and how these effects are included in our model.

CHAPTER 5

Analytical Model of Short-Channel MOSFETs

In this chapter we consider the short-channel effects on the supply current waveforms. We applied the model presented in chapter 3 for long channel MOSFETs to a 0 8 micron technology carry look-ahead adder circuit, the results of the comparison are shown in Fig. 5.1. The long channel model does not give a good approximation of the supply current. The short channel model, that will be presented in this chapter, closely approximates the supply current. The main reason that the long-channel electrical characteristics deviate from the short-channel devices is carrier drift velocity saturation in small geometry devices. Section 5.1 presents an engineering DC model for short channel MOS devices, in Section 5.2 the short-channel supply current model is derived.

Y x 10 -6

(a) Short-channel model

(b) Long-channel model

(c) SPICE level 3
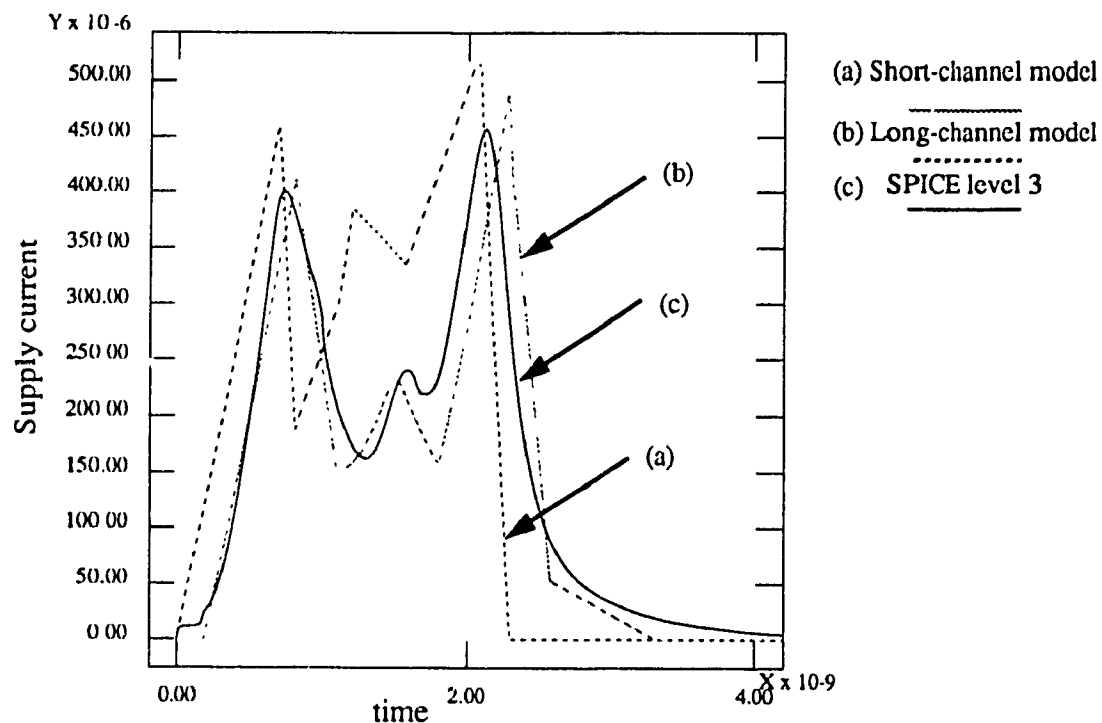
Fig. 5.1 Short-channel effects

5.1- Large-Signal Model for Short-Channel MOS devices

A short channel model for MOS devices is presented in [9]. The model is suitable for analytical calculations. In long channel devices the carrier drift velocity is given by $v = \mu_{eff}E$ where the effective carrier mobility μ_{eff} is assumed constant and E is the longitudinal channel field. In short channel devices μ_{eff} is no longer constant and is a function of transverse field in the inversion layer. The velocity saturation is no longer proportional to E due to high field effects [9]. These effects are summarized in a large-signal model presented in [9]:

$$
I_D = \begin{cases}
\dfrac{\mu_{eff}C_{ox}W}{L_{eff}} \dfrac{1}{1 + \dfrac{V_{DS}}{E_c L_{eff}}} (V_{GS} - V_T - \frac{1}{2}V_{DS}) V_{DS} & \text{for } V_{DS} \leq V_{Dsat} \quad \textbf{Linear region} \\
\\
K ve_{sat} C_{ox} W (V_{GS} - V_T) & \text{for } V_{DS} \geq V_{Dsat} \quad \textbf{Saturation region} \quad \text{(EQ. 5.1)}
\end{cases}
$$

Where

ve_{sat} Carrier drift velocity saturation

C_{ox} gate capacitance per unit area

W device width

L_{eff} effective channel-length between the source and the drain

V_{DS} drain-to-source voltage

V_{GS} gate-to-source voltage

V_{dsat} saturation voltage, defined as the voltage at which the carrier drift velocity saturates

E_C is given by $E_C = \dfrac{2ve_{sat}}{\mu_{eff}}$

V_{dsat} is given by:

$$V_{dsat} = (1 - K) (V_{GS} - V_T)$$

where

$$K = \left(1 + \frac{E_c L_e}{V_{GS} - V_T}\right)^{-1}$$

L_e is the device electrical length and is given by

$$L_e = L_{eff} - X_d$$

X_d depletion width into the channel from the drain in the saturation region. X_d may be calculated as follows,

$$X_d = \frac{1}{A} ln\left(\frac{A (V_{DS} - V_{Dsat}) + E_d}{E_c}\right)$$

where

$$E_d = \sqrt{1 + \left[\frac{A (V_{DS} - V_{Dsat})}{E_c}\right]^2}$$

A is a semi-empirical constant (For our 0.8u technology $A \approx 0.2*10^8$).

5.2- Current Model for Short-Channel MOS Devices

The voltage waveforms for long and short channel devices are similar, only the time constant is different [6]. The same applies to the supply current, the overall current *shapes* for both long and short channel devices are similar. The time constant and current values are different. We apply the same modelling strategy of Chapter 3. The model parameters are derived using the DC current equations 5.1 to include the short-channel effects. A symbolic mathematical software package (Maple version 4.2, Watcom, University of Waterloo) has been used to solve the differential equations.

5.3- Circuit Analysis for Step Input

The analysis of series-connected short-channel devices is similar to the approach used for long channel devices. The same cases discussed in Section 3.1 applies to short-channel devices (Fig. 3.4). In this Section we present the derivation of the model parameters, using the modelling strategy presented in Section 3.1.
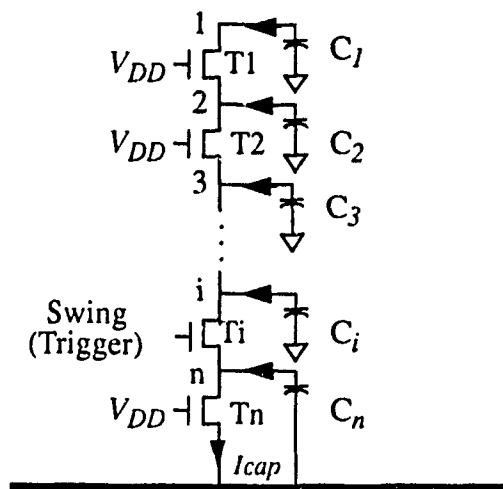
Fig. 5.2 Currents in short-channel series-connected MOS transistors
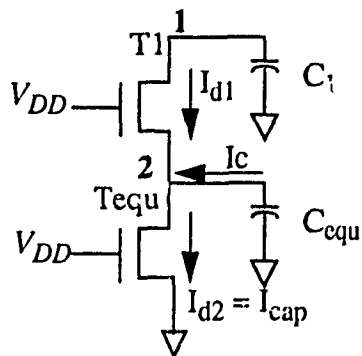
Fig. 5.3 Equivalent circuit for the estimation of the capacitive current in short-channel transistors

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5.3.1- Case 1: T1 stays in saturation until all node voltages reach their plateau value

i- Case 1, segment 1

a- Estimation of I_{init}

The same methodology approximation used for long-channel devices is applied to the short-channel device analysis. Hence the circuit of Fig. 5.2 is reduced to the circuit of Fig. 5.4 as before. In the case a step input, the current in the equivalent circuit starts at:

$$I_{init} = \frac{\mu_{eff} C_{ox} W_{equ}}{L_{eff_{equ}}} \frac{1}{1 + \frac{V_{DD}}{E_c L_{eff}}} \frac{(V_{DD} - V_T)^2}{2} \qquad \text{(EQ. 5.2)}$$

Where:

$W_{eff_{equ}}, L_{eff_{equ}}$ are the equivalent transistor sizes

Fig. 5.4 Estimation of I_{init} for sub-micron devices

b- Estimation of I_{dss}

At the end of segment 1 all the nodes capacitances are settled to their plateau values and the current flowing in the capacitances is almost zero. Since all the transistors from T2 to Tn are in the linear mode they are replaced by an equivalent transistor. T1 is in the saturation mode. The equivalent circuit is shown in Fig. 5.3. Since at the end of this segment no current flows in the nodes capacitances (i.e. C_{equ}) we can write:

$$I_{d1} = I_{d2}$$

replacing I_{d1} and I_{d2} by their expression of EQ. 5.1 we have:

$$k_1 (V_e - v_{2ss}) = \frac{k_2}{1 + \dfrac{v_{2ss}}{k_3}} (V_c - \frac{v_{2ss}}{2}) v_{2ss} \qquad \text{(EQ. 5.3)}$$

Where $\quad k_1 = K v e_{sat} C_{ox} W$

$$k_2 = \frac{\mu_{eff} C_{ox} W}{L_{eff}}$$

$$k_3 = E_c L_{eff}$$

Solving EQ. 5.1 for v_{2ss} we obtain:

$$v_{2ss} = \frac{1}{2} (-2 k_1 V_e + 2k_1 k_3 + 2k_2 k_3 V_c \pm 2 (k_1^2 V_e^2 + 2k_1^2 V_e k_3 - 2k_1 V_c k_2 k_3 V_e + k_1^2 k_3^2$$
$$+ 2k_1 k_3^2 k_2 V_c + k_2^2 k_3^2 V_c^2 - 2k_1 V_e k_3^2 k_2)^{1/2} / (-2k_1 + k_2 k_3)) \qquad \text{(EQ. 5.4)}$$

$$I_{dss} = k_1 (V_e - v_{2ss}) \qquad \text{(EQ. 5.5)}$$

c-Duration of segment 1, t_s

Now we have to determine an expression for t_s, the current equation at node 2 (Fig 5.3) is:

$$C_{equ}\frac{d}{dt}v_2(t) = I_{d1} - I_{d2} \qquad \text{(EQ. 5.6)}$$

$$I_{d1} = k_1(V_e - v_2(t))$$

$$I_{d2} = \frac{k_2}{1 + \frac{v_2(t)}{k_3}}(V_c - \frac{v_2(t)}{2})v_2(t)$$

Where

$$k_1 = \frac{\mu_{eff}C_{ox}W}{L_{eff}}$$

$$k_2 = E_c L_{eff}$$

$$k_3 = ve_{sat}C_{ox}W$$

The solution for EQ. 5.6 is given by:

$$t_s = f(0.99v2ss) \qquad \text{(EQ. 5.7)}$$

The full expression of $f(v2)$ is given in appendix A.2.

d- Charge lost by the circuit

In order to determine the charge lost by the circuit during this stage we have to determine the voltage drop Δv_1 of node 1 (Fig 5.3). Node 1 equation is given by:

$$C_1\frac{dv_1}{dt} = -I_{d1} \qquad \text{(EQ. 5.8)}$$

EQ. 5.8. cannot lead to an expression of $v_1(t)$, but we can have an expression $v_1(v_2)$, and the solution is given by:

$$v_1 = h(v2) \qquad \text{(EQ. 5.9)}$$

The full derivation and expression of $h(v_2)$ is given in appendix A-2. The voltage drop, Δv_1 during segment 1 is given by:

$$\Delta v_1 = h[v_2(0)] - h[0.99v_{2ss}] \qquad \text{(EQ. 5.10)}$$

The charge lost by the circuit during segment 1 is given by

$$\Delta Q_1 = C_1 \Delta v_1 - C_{equ}[v_2(0) - 0.99v_{2ss}] \qquad \text{(EQ. 5.11)}$$

ii-Case 1, segment 2

In this segment the current is constant and equal to I_{dss} (Fig. 3.2), we have to determine the duration of this stage. The duration of the segment depends on how long T1 stays in the saturation region.

a- Duration of segment 2, t_a

T1 will get out of the saturation when node 1 (fig. 5.3) drops under V_{dsat}. Node 1 has already dropped by Δv_1 during segment 1and is given by EQ. 5.10. Since the current through T1 is constant node 1 will drop at a constant rate and the duration of the segment is given by:

$$t_a = C_1 \frac{V_{DD} - V_{dsat} - \Delta v1}{I_{dss}} \qquad \text{(EQ. 5.12)}$$

b- Current during segment 2

The current during this stage is given by:

$$I_{cap} = I_{dss} \qquad \text{(EQ. 5.13)}$$

c- Charge lost during segment 2

The charge lost by the circuit during segment 2 is given by:

$$\Delta Q_2 = I_{dss}t_a \qquad \text{(EQ. 5.14)}$$

iii- Case 1, segment 3

In segment 3 (Fig. 3.2) all the transistors are in the linear mode and the current will drop gradually to 0, we model the current linearly from I_{dss} to 0.

a- Current during segment 3

The current starts at Idss and drops linearly to 0.

b- Charge lost by the circuit during segment 3

Knowing the charge lost by the circuit during segment 1 and segment 2 (i.e. $\Delta Q1$, $\Delta Q2$) we can determine the charge lost by the circuit during segment 3:

$$\Delta Q_3 = Q_{initial} - (\Delta Q_1 + \Delta Q_2) \qquad \text{(EQ.5.15)}$$

c- Duration of segment 3, t_l

Knowing the charge lost by the circuit during this segment $\Delta Q3$ we determine the duration of this stage t_l:

$$t_l = 2\frac{\Delta Q_3}{I_{dss}} \qquad \text{(EQ.5.16)}$$

iv- Validity of case 1 model

We present a condition to use the formulas developed in case 1. In order to use case1 all the nodes should settle to a plateau voltage while T_1 is still in the saturation region. This condition is satisfied when:

$$v_1 (t = t_s) < \alpha V_{Tn} \qquad \text{(EQ. 5.17)}$$

and $v_1(v_2)$ is given in EQ.5.9 and is evaluated at $v_2 = 0.99\ v_{2ss}$,

$$v_1 (t_s) = h (0.99 v_{2ss}) \qquad \text{(EQ. 5.18)}$$

5.3.2 Case 2: T1 gets out of the saturation before the node voltages reach their plateau values

i- Case 2, segment 1

In this case T1 will get out of saturation while the node voltages are still charging or discharging to their plateau values.

a- Current at the beginning of segment 1, I_{init}

The estimation of Iinit is the same as in Case 1 and is given by EQ. 5.2.

b- Duration of segment 1, t_s

The duration of this stage depends on when T1 get out of the saturation or in other words drops under V_{dsat}. We have (EQ. 5.9):

$$v_1 = h(v2)$$

Unfortunately we cannot get h^{-1} in closed form. Knowing that v_2 is between $v_2(0)$ and v_{2ss} for this interval, the above equation is iterated between $v_2(0)$ and v_{2ss} for a maximum of 10 iterations, to determine at which value of v_2, $v_1 = V_{dsat}$. Knowing v_2 we can determine t_s from EQ. 5.7:

$$t_s = f(v2)$$

c- Current at the end of segment 1, $I_{cap}(t_s)$

and $I_{cap}(t_s)$ is given by:

$$I_{cap}(ts) = \frac{k_2}{1 + \dfrac{v_2(t_s)}{k_3}} (V_c - \frac{v_2(t_s)}{2}) v_2(t_s) \qquad \text{(EQ. 5.19)}$$

and the charge lost by the circuit is:

$$\Delta Q_1 = C_1 [V_{DD} - V_{dsat}] - C_{equ} [v_2(0) - 0.99 v_{2ss}] \qquad \text{(EQ. 5.20)}$$

ii- Case 2, segment 3

At this stage T_1 transistor will leave the saturation region and all the transistors will be in the linear mode.

a- Current in segment 3

The current starts at $I_{cap}(t_s)$ and decreases linearly to 0.

b- Charge lost during segment 3

Knowing the initial charge of the circuit and the charge lost during stage 1 we can determine the charge lost by the circuit during this period:

$$\Delta Q_3 = Q_{initial} - \Delta Q_1 \qquad \text{(EQ. 5.21)}$$

c- Duration of segment 3, t_l

If we make a linear approximation of the current (Fig. 3.2) and Knowing the initial current $I_{cap}(t_s)$ and the charge ΔQ_3 we can determine the duration t_l of this stage:

$$t_l = 2\frac{\Delta Q_3}{I_{dss}} \qquad \text{(EQ. 5.22)}$$

5.4- Ramp Input Effects

The model strategy for a ramp input is to built on the model derived for a step input as discussed in section 3.4. We present the values affected by the input slope, the initial current Iinit, it's timing tmax and the short circuit current.
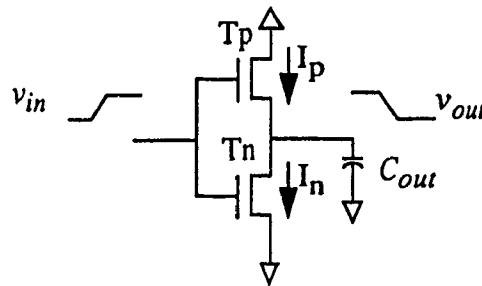

Fig. 5.5 Equivalent inverter for short-channel transistors

5.4.1- Closed-form solution of v_{out}

If we neglect the pull-up current, we can write the output node equation (Fig. 5.5) as follows:

$$C_{out}\frac{dv_{out}}{dt} = \begin{cases} -ve_{sat}C_{ox}WK(v_{in}-V_T) & \text{Pull-down in linear} \\ \dfrac{k_2}{1+\dfrac{v_{in}}{k_3}}(v_{in}-V_T-\dfrac{v_{out}}{2})v_{out} & \text{Pull-down in saturation} \end{cases}$$

(EQ. 5.23)

The input ramp v_{in} is given by:

$$v_{in}= \begin{cases} st & \text{for } t \leq t_r \\ V_{DD} & \text{for } t \geq t_r \end{cases}$$

The detailed resolution of EQ. 5.23 is given in appendix A-3, the solution is as follows:

i- Pull-down in saturation and $t \leq t_r$

$$v_{out} = V_{DD}-\frac{ve_{sat}C_{ox}W}{C_{out}}\left[\left[\frac{1}{2}st^2 -V_Tt -tk_3 +\frac{k_3^2}{s}ln(st-V_T+k_3)\right]-\frac{k_3}{s}ln(-V_T+k_3)\right]$$

Where $k_3 = E_cL_e$

(EQ.5.24)

ii- Pull-down in saturation and $t > t_r$

$$v_{out} = v_{step}-ve_{sat}C_{ox}WK(V_{DD}-V_T)(t-\frac{V_{DD}}{s})$$

(EQ.5.25)

iii- Pull-down in linear region and $t \leq t_r$

$$\frac{1}{v_{out}} = e^{\frac{kV_{DD}}{2C_{equ}s}(st-n)^2}\left[\frac{1}{V_{dsat}e^{\frac{kV_{DD}}{2C_{equ}s}}} + \sqrt{\frac{\pi k V_{DD}}{8C_{equ}s}}\left(erf\left(\sqrt{\frac{\pi k v_{sat}^2}{8C_{equ}s}}\right) - erf\left(\sqrt{\frac{kst-n^2}{8C_{equ}s}}\right)\right)\right] \quad \text{(EQ.5.26)}$$

iv- Pull-down in linear region and $t > t_r$

$$\frac{1}{v_{out}} = \frac{1}{2(V_{DD}-V_T)}\frac{\left(-2(-v_{step}+2V_{DD}-2V_T)(V_{DD}-V_T)e^{-\left(kt\frac{(-V_{DD}+V_T)}{C_{equ}}\right)}\right)}{-2v_{step}(V_{DD}-V_T)e^{\left(\frac{-kt_{step}(V_T-V_{DD})}{C_{equ}}\right)}} \quad \text{(EQ.5.27)}$$

Where t_{step}, v_{step} are the time at which the input ramp reaches V_{DD} and the output voltage at that time.

5.4.2- Short-circuit current

Knowing the output voltage v_{out} we can determine the pull-up current by applying EQ. 5.1:

$$I_{DP}= \begin{cases} k_2\dfrac{1}{1-\dfrac{v_{out}-V_{DD}}{k_3}}\left(v_{in}-V_{DD}-V_T-\frac{1}{2}(v_{out}-V_{DD})^2\right)(v_{out}-V_{DD}) & \begin{array}{l}\textbf{Linear region}\\ v_{out}-V_{DD} \leq v_{Dsa}\end{array} \\[2em] ve_{sat}C_{ox}WK(v_{in}-V_{DD}-V_T) & \begin{array}{l}\textbf{Saturation region}\\ v_{out}-V_{DD} \geq v_{Dsat}\end{array} \end{cases}$$

$$V_{dsat} = (1-K)(v_{in}-V_{DD}-V_T) \quad \text{(EQ.5.28)}$$

$$K = \left(1-\frac{E_cL_e}{v_{in}-V_{DD}-V_T}\right)^{-1}$$

The expressions for v_{out} are given in equations EQ. 5.24, 25, 26, 27, these equation are

iterated from 0 to tr to estimate the peak short-circuit current and its timing. The time step is fixed to tr/10 to limit the number of iterations to 10.

5.4.3 Effect of the input rise time on I_{init}

The Initial current I_{init} is affected by the input rise time, as discussed in Section 3.4. Using the equivalent circuit of Fig. 5.4, the equations for the voltage at node i are the same as EQ. 5.24, 25, 26, 27. These equations are numerically evaluated from 0 to tr to estimate I_{init} and its timing, the maximum number of iterations is limited to 10 iterations.

5.5- Delay and output fall time estimation

Given the complexity of the output voltage expressions, it is not possible to have an analytical expression for the delay and rise/fall time, these equations are numerically evaluated to have an accurate delay, and output rise/fall time. The time step can be fixed to Δt to estimate the delay. The delay is determined at Δt accuracy. A macro model of RC time constant is used to evaluate Δt. For practical delay and output rise/fall time the number of iterations should not exceed 20.

CHAPTER 6

Comparison of Analytical Supply Current with SPICE for Short-Channel MOSFETs

Our short channel model has been tested on a variety of circuits using a 0.8 micron technology to prove its validity.

6.1- A 5-Input Nand Gate

A first set of test on a 5-input nand gate (Fig. 6.1) is presented in this section. Short-circuit and capacitive currents are estimated and compared to SPICE results.

Effects of the load capacitance on the current
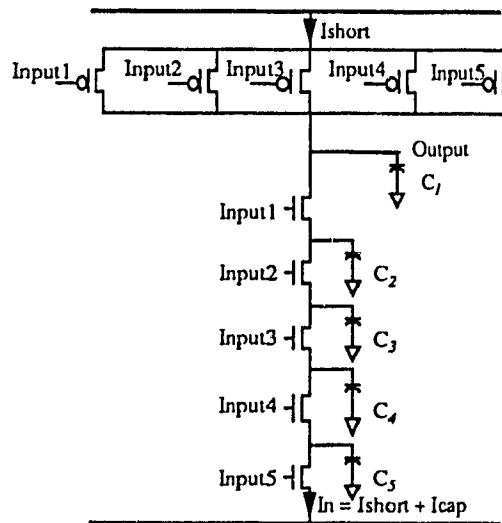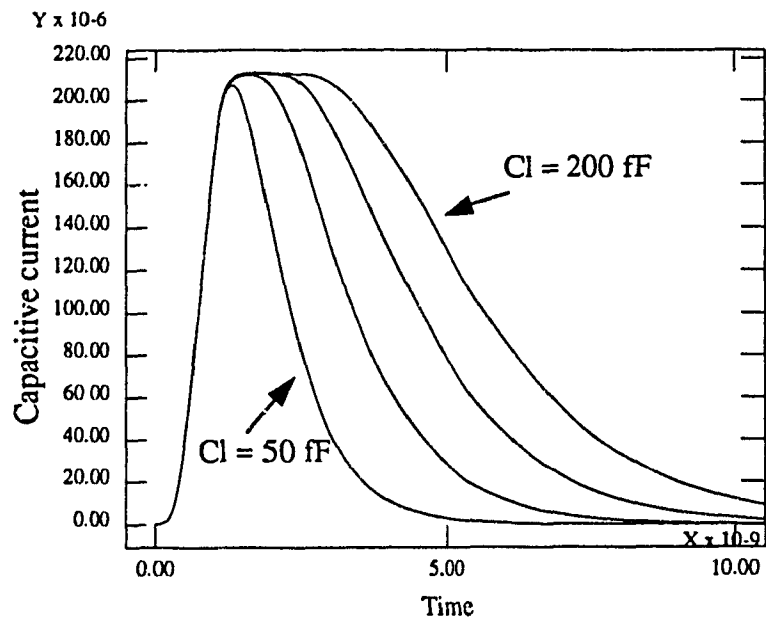
The load capacitance is varied and compared with SPICE
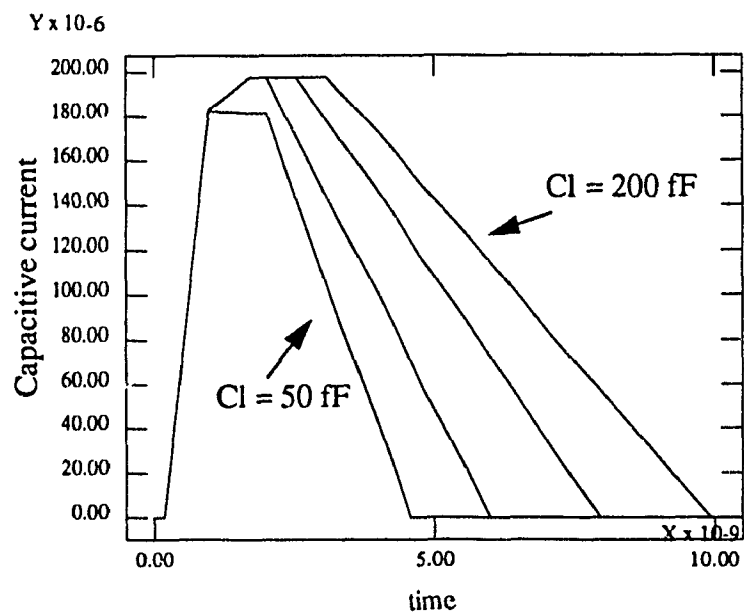

Fig. 6.1 A 5-input nand gate using 0.8 micron technology

Fig 6.2 shows a comparison between SPICE and model results for different loads, this Figure shows a good agreement between SPICE and our model.

a- SPICE

b- Model

Fig. 6.2 Capacitive current for different loads

A more detailed comparison is shown in Fig. 6.3 and the difference between our model and SPICE is shown in Fig. 6.4. The difference is less than 1%.
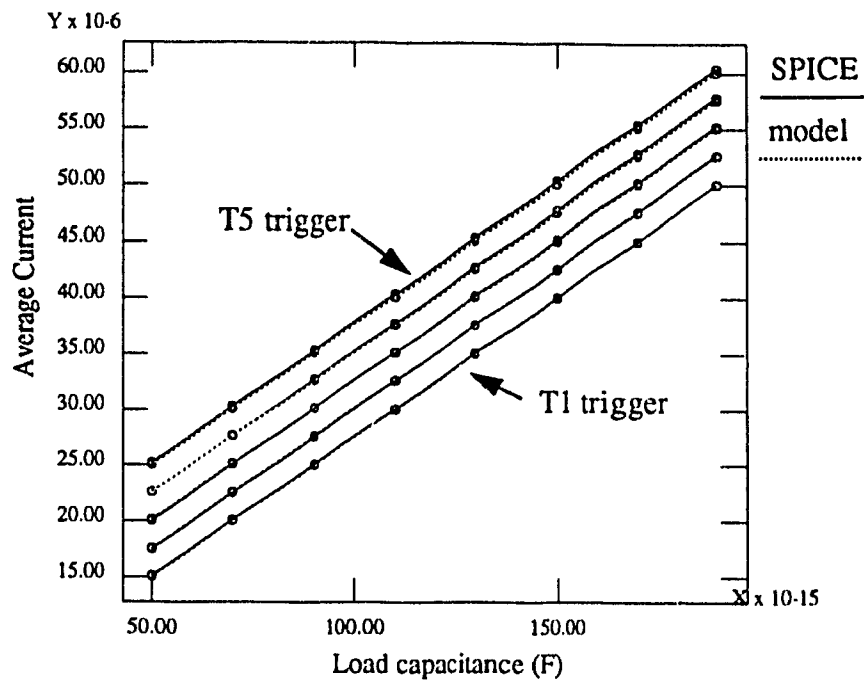

Fig. 6.3 Average capacitive current for different loads

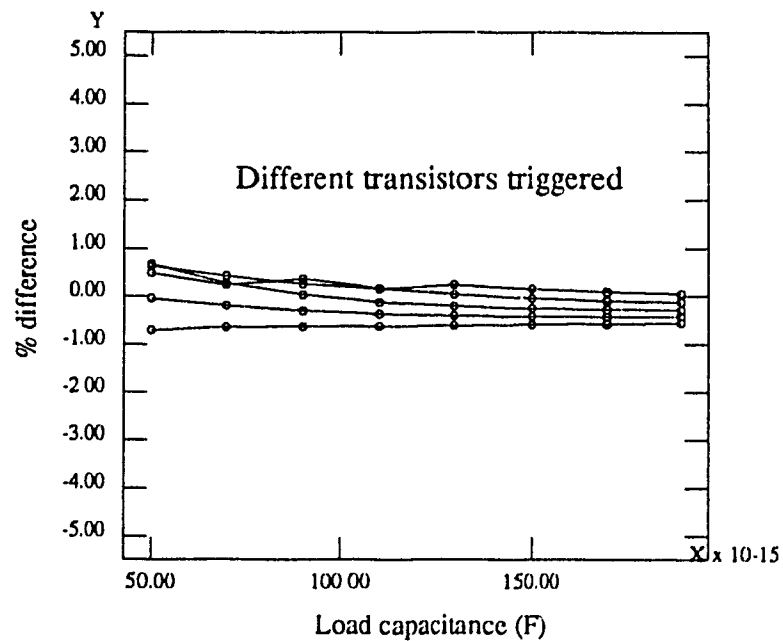Fig. 6.4 Percentage difference for different loads

The effect of the load on the peak current

The effect of the load on the peak capacitive current is shown in Fig. 6.5 and the difference with SPICE is shown in Fig. 6.6. The model shows a difference less than 10% with SPICE results.
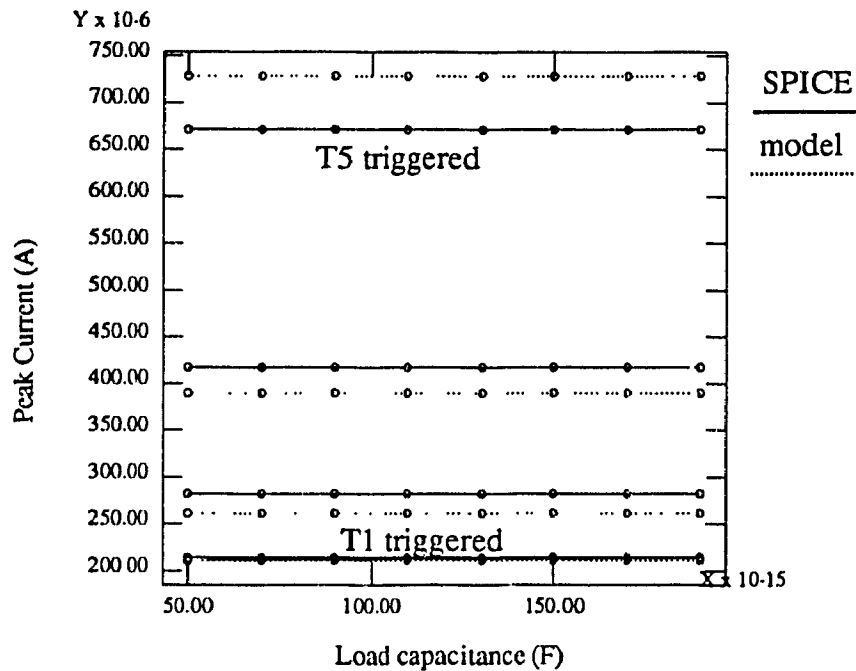
Fig. 6.5 Peak capacitive current for different loads

Fig. 6.6 Difference between model and SPICE for different loads

Effects of the internal node capacitances

The effect of the internal node capacitance C3 (Fig. 6.1) on the average capacitive current is shown in Fig. 6.7 and 6.8. The difference on the average current is less than 1%.
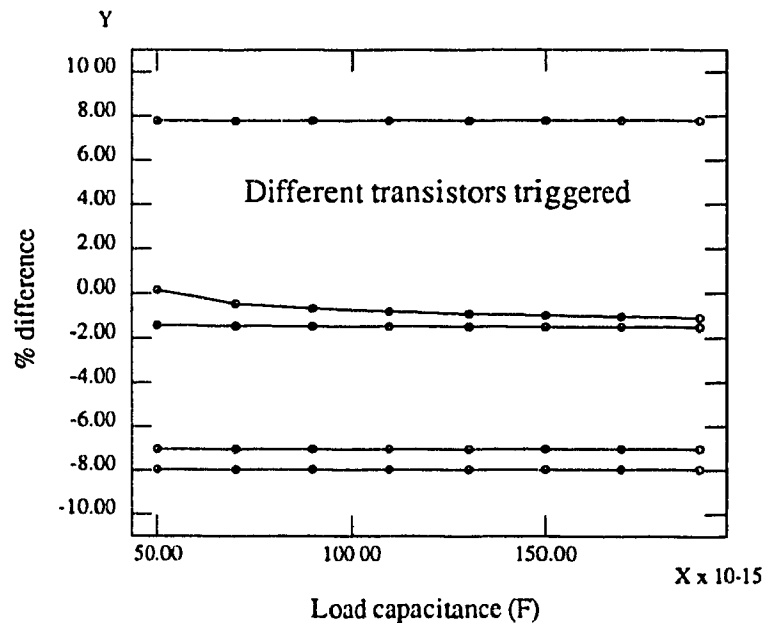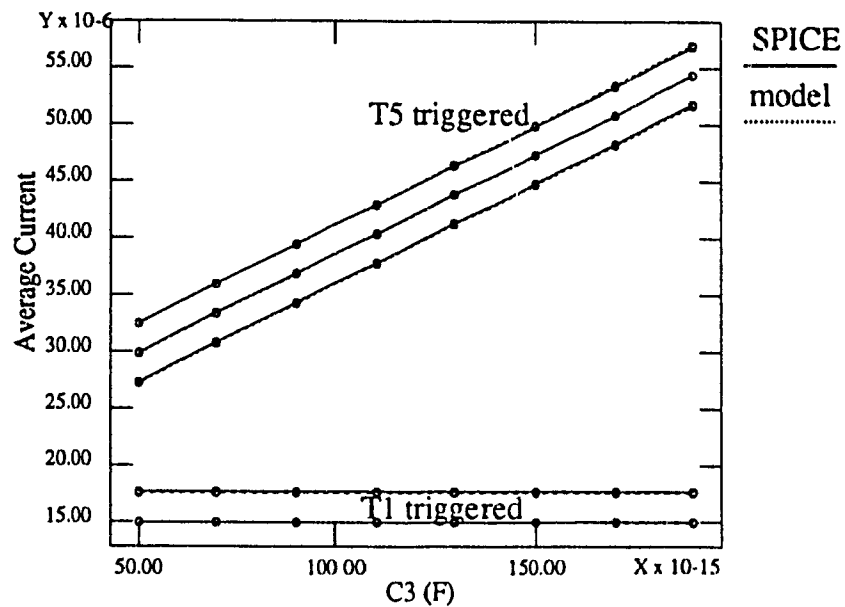

Fig. 6.7 Average capacitive current for different C3 values
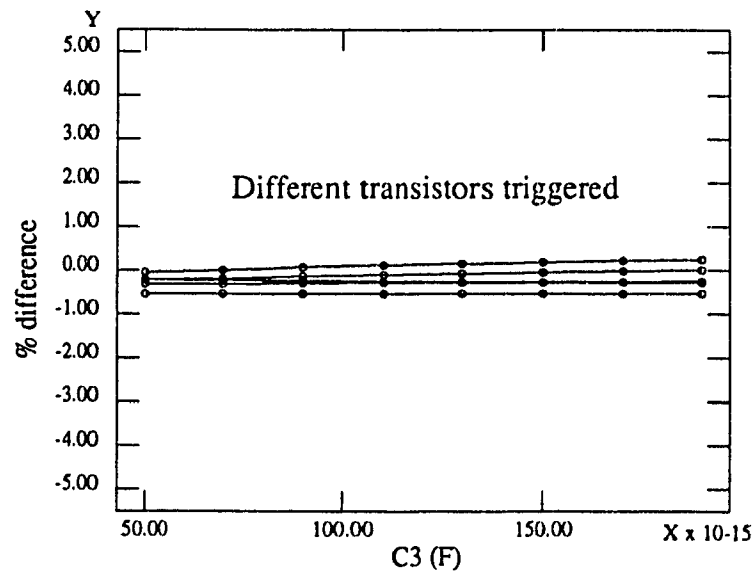
Fig. 6.8 Difference between model and SPICE for different C3 values

Effect of the trigger transistor on the capacitive current

The effect of the trigger on the capacitive current is shown in Fig. 6.9 and 6.10. One transistor is switched at a time and all the other inputs are kept high. The average current increases if the transistor closer to the ground is switched, since more node capacitances will be charged. The peak current increases as the transistor switched is closer to the ground. The maximum difference is less than 10%.
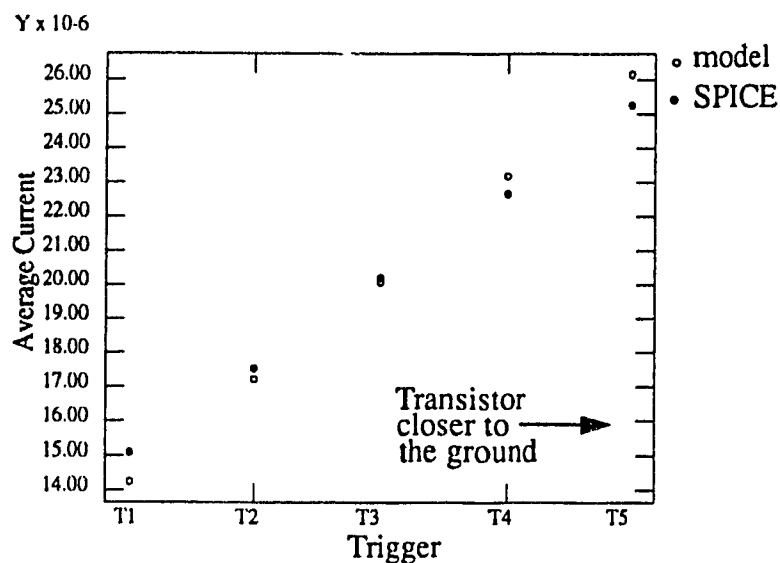
Fig. 6.9 Average capacitive current for different transistor switched
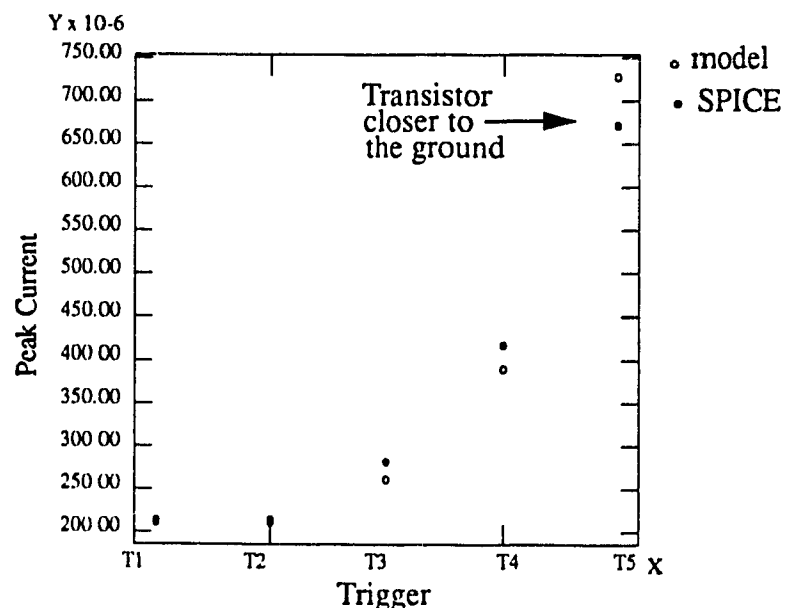
Fig. 6.10 Peak capacitive current for different transistor switched

Effect of the input rise time

The effect of the input rise time on the capacitive current is shown in Fig. 6.11-a and b. Transistor T5 (Fig. 6.1) is switched with different input rise times. The model results show good agreement with SPICE.
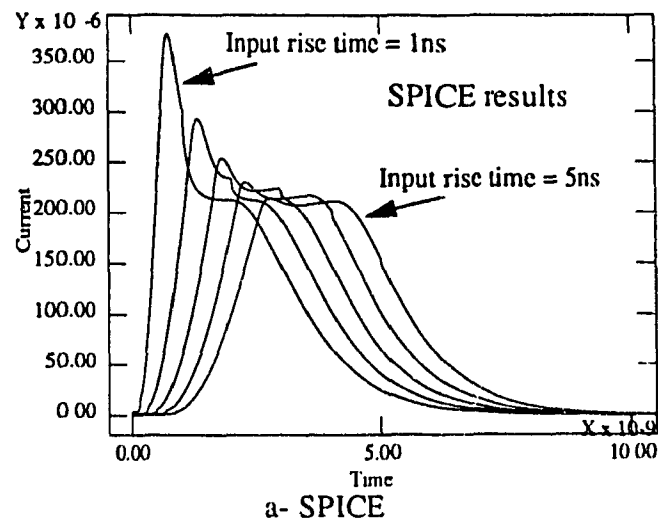
a- SPICE

Fig. 6.11.a Pull-down current for different input rise time
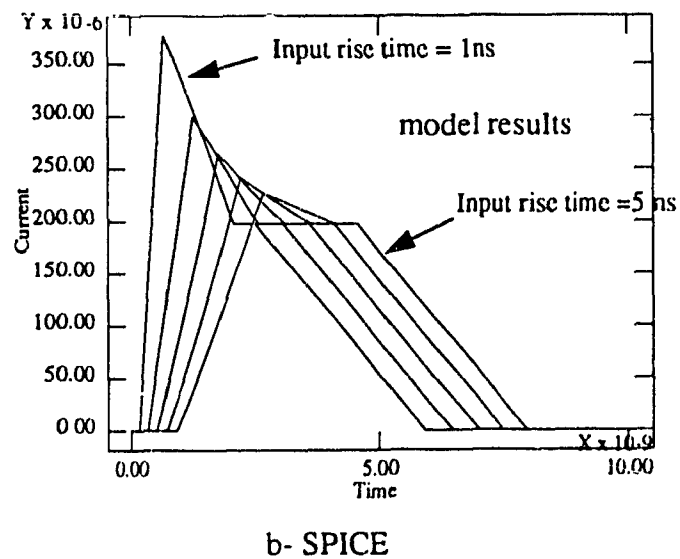
b- SPICE

Fig. 6.11.b Pull-down current for different input rise time

The effect of the input rise time on the peak capacitive current is shown in Fig. 6.12. The model shows a good agreement with SPICE for practical rise and fall times.
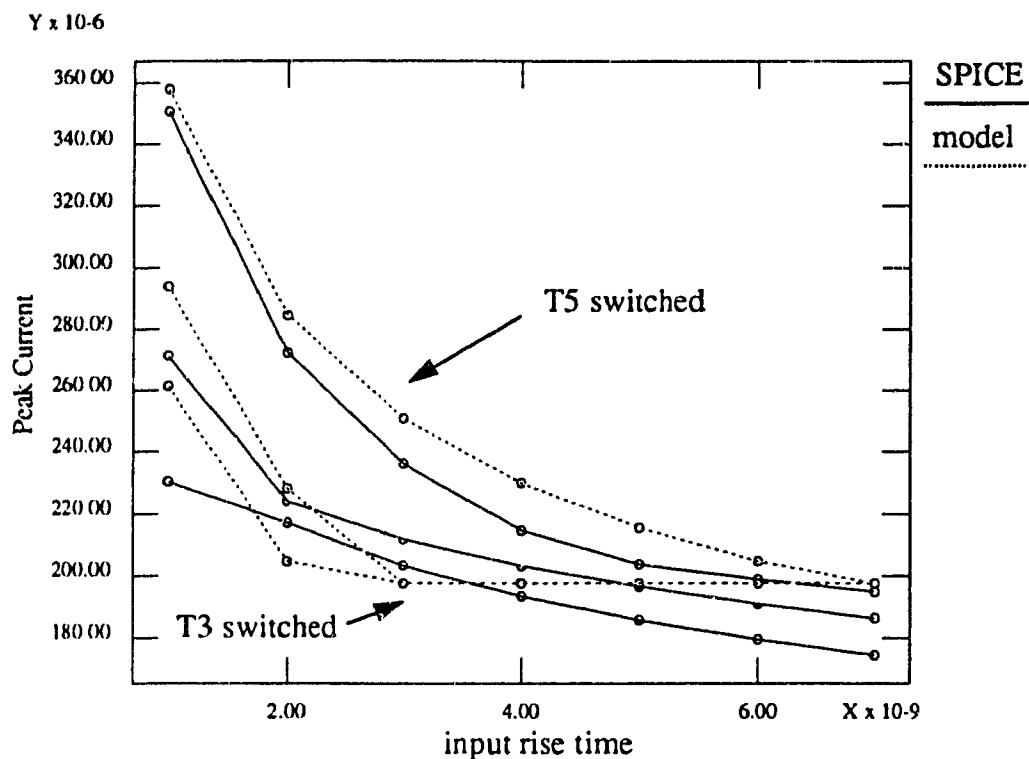
Fig. 6.12 Peak pull-down current for different input rise times

The short-circuit current for different input rise time is shown in Fig. 6.13 and Fig. 6.14. The model results are independent of the transistor triggered. The model uses an equivalent inverter for the calculation of short-circuit current, and the effect of the trigger is not included. The results of Fig. 6.13 and Fig. 6.14 show acceptable estimates of the short-circuit current.
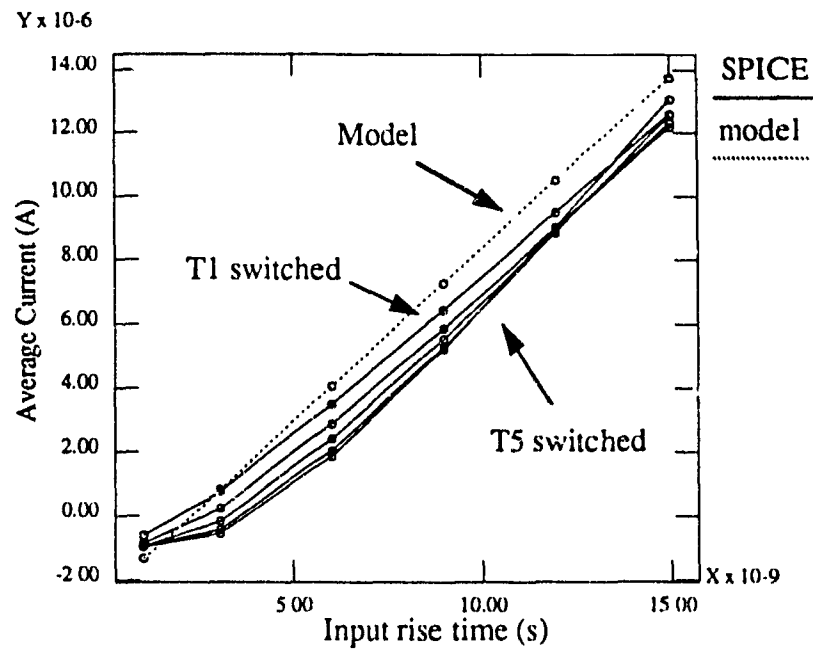
Fig. 6.13 Average short-circuit current for different input rise times
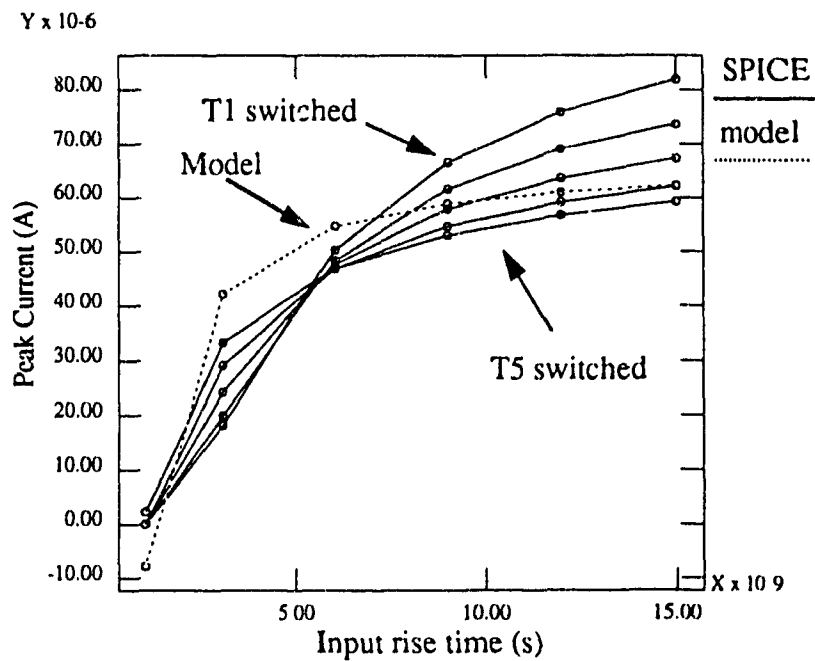
Fig. 6.14 Short-circuit current for different input rise times

6.2- Carry Look-Ahead Adder Circuit

The model is used for a carry look-ahead circuit. A timing analysis using delay model was presented in section 5.5. The timing analysis results is combined with the model estimation of the current developed for short channel devices to obtain the supply current. Fig. 6.15-.a, b, c show a comparison between our model and SPICE for different input conditions. The model shows a good agreement with SPICE results.
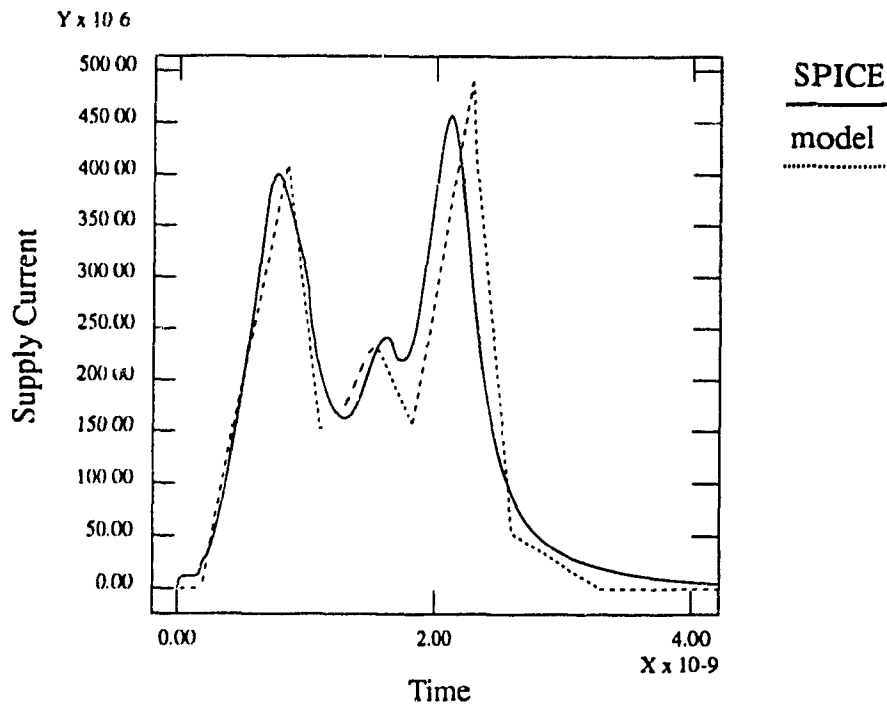
Fig. 6.15.a Supply current for different input vectors
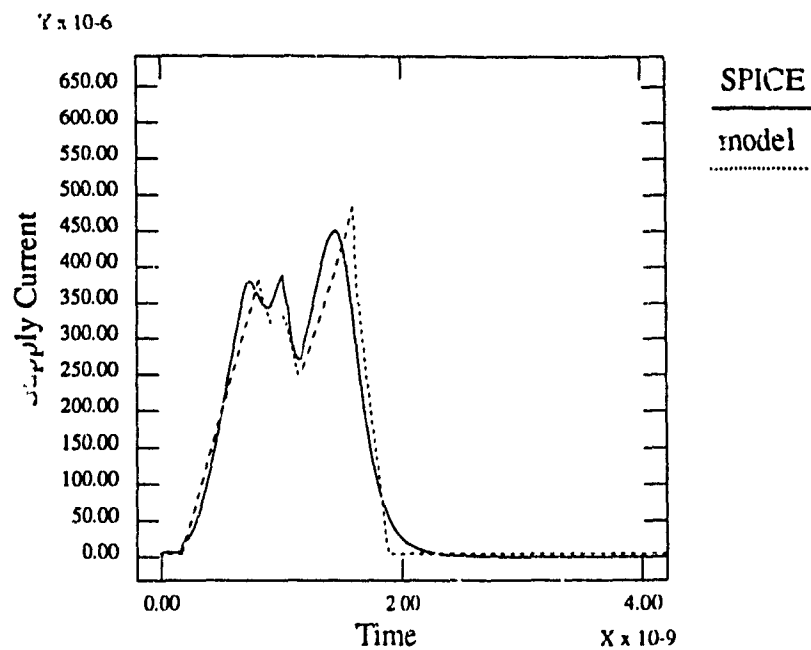
Fig. 6.15.b Supply current for different input vectors
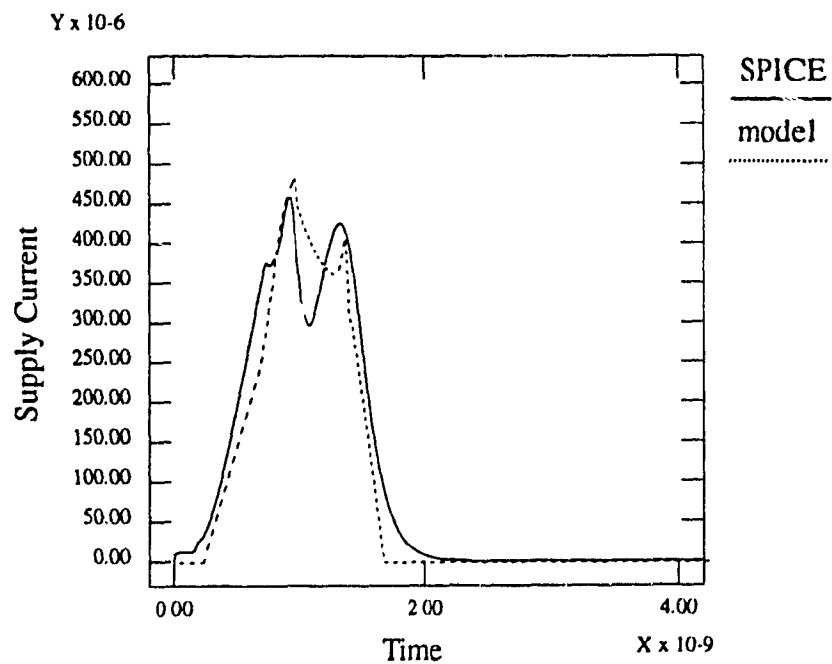
Fig. 6.15.c Supply current for different input vectors

6.3- A 4-mA I/O Pad Driver

In integrated circuits an important fraction of the supply current is due to the charging and discharging of I/O pads. We tested our model on a 4-ma I/O pad shown in Fig. 5.21 for different loads and the results of the comparison is shown in Fig. 5.22. Our model shows a good agreement with SPICE on a wide range of output loads.
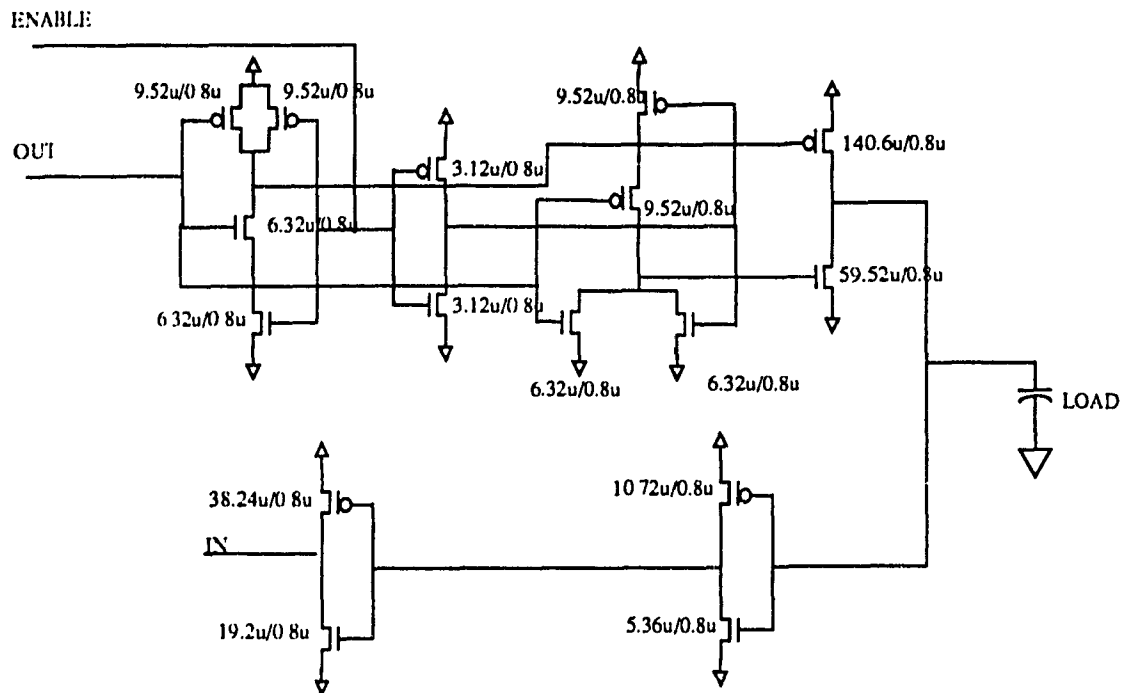
Fig. 6.16 A 4-mA I/O pad driver
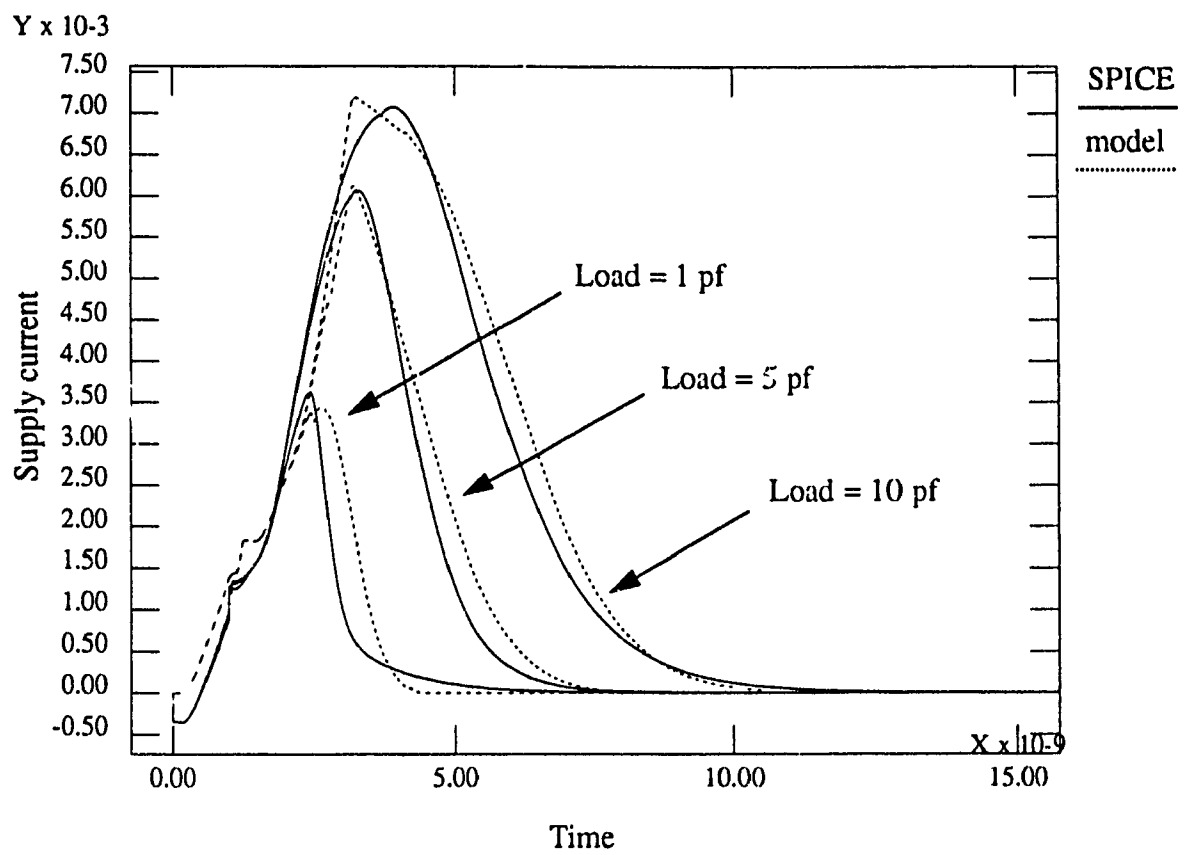
Fig. 6.17 Supply current for different loads

6.4- A 4-bit Carry Look-Ahead Adder with Output Pad Drivers

In order to increase the complexity of the circuits we have tested our model on a 4-bit carry look-ahead adder with pad drivers as shown in Fig. 6.18. The results of the current estimation as compared to SPICE is given in Fig. 6.19. The results once more confirm the validity of our model.
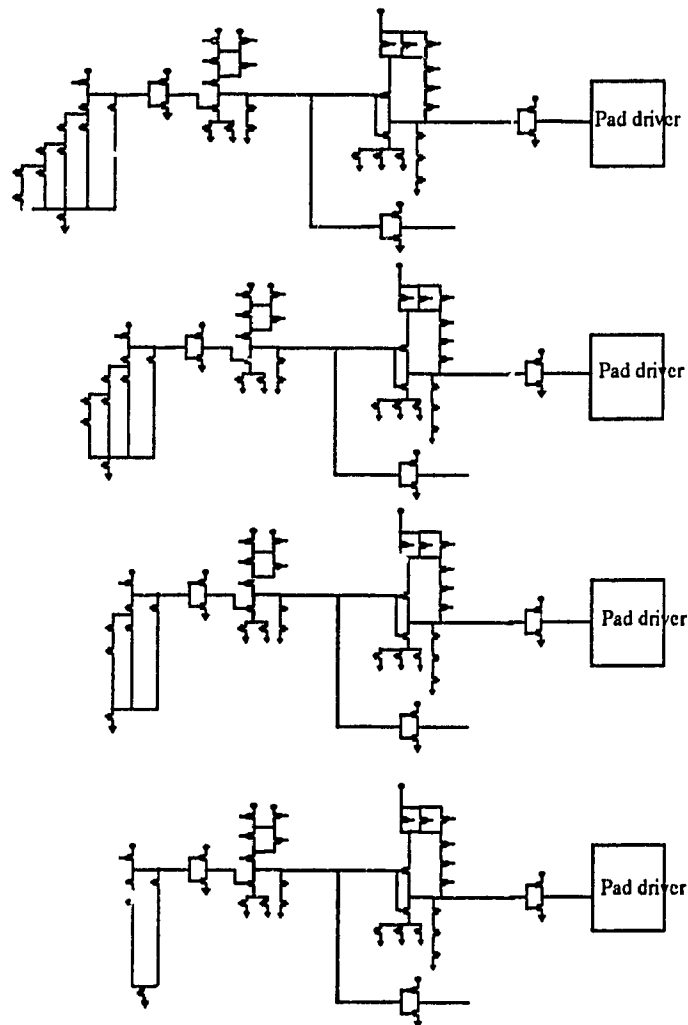
Fig. 6.18 A 4-bit carry look-ahead adder with I/O pad drivers
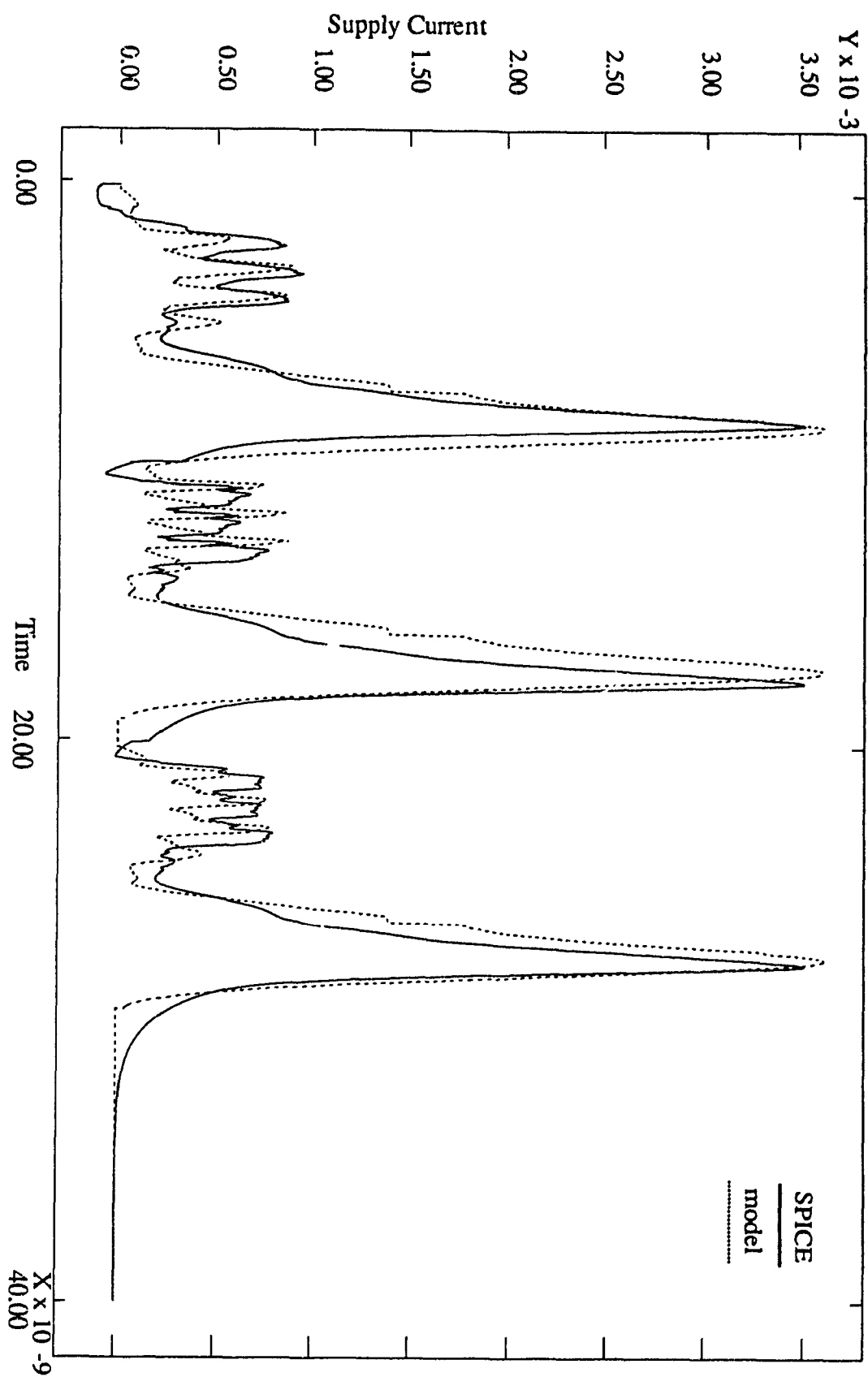
Fig. 6.19 Supply current for a 4-bit carry look-ahead circuit with pad drivers

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6.5- Run Time Comparison between SPICE and Model

Table 1 shows a speedup of 3 orders of magnitude and the speed-up is expected to increase with the number of gates in the CMOS circuit. Table 1 is obtained by running the model and SPICE on different circuits. The execution time is obtained with the UNIX command *time*.

Table 1: Run time comparison between SPICE & model

nbr of transistors	nbr of gates	SPICE (s)	model (s)	Speed-up
24	3	170	0.1	1700
78	9	480	0.3	1860
800	132	3 780	1.4	2700

6.6- Model Fitting for a New CMOS Technology

Given a transistor technology file, we propose a methods to extract the different model parameters. First the transistor model DC parameters are fitted to the new technology as shown in Fig. 6.20. The parameters used for the fitting are ve_{sat}, *Leff* and *A* defined in Section 5.1. The DC parameters are fitted with SPICE results for a minimum size transistor, then for a transistor with a width 10 times larger. The values of ve_{sat}, *Leff* and *A* are then determined in the intervals between the two fittings.

The next step is to fit the current model parameters. Fig. 6.21 reproduce the current model of case A-1 to facilitate the reading. Three values are fitted in the current model, I_{init}, I_{dss} and the charge. I_{init} depends on the node capacitances, input rise time and trigger position. I_{init} is fitted using a network of 5 series connected transistors. By triggering the transistors from T1 to T5 with different rise times we estimate a correcting factor for I_{init}. The next value to be fitted is I_{dss}, which is independent of the capacitances and trigger position, it

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Ids
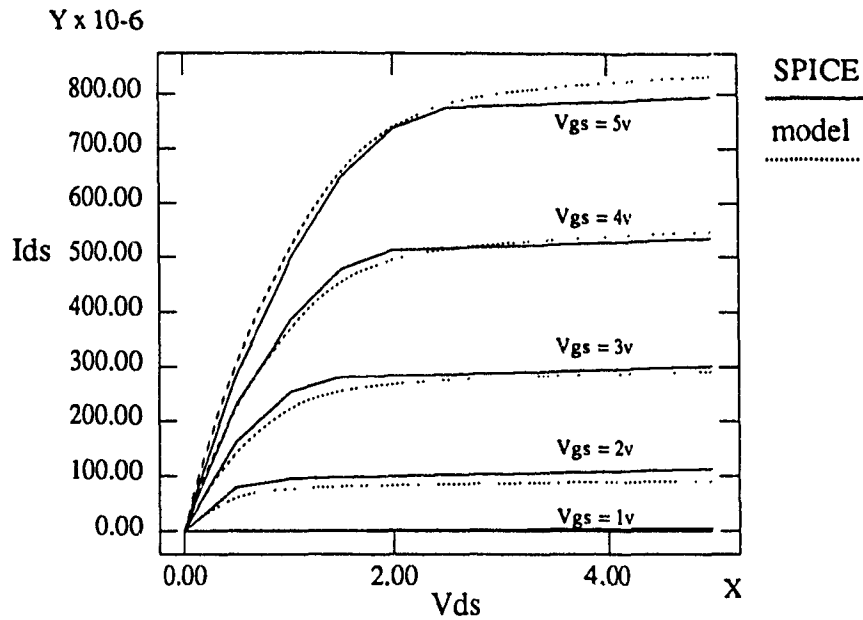
Fig. 6.20 Transistor DC model fitting

depends only on the transistor sizes. Therefore in order to fit I_{dss} we take different series

connected MOS transistors including 2, 3, 4 and 5 transistors. Then we obtain a correcting

factor to fit our model with SPICE estimates The last value to be fitted is the charge, which

is equal to $\sum_i C_i V_i^2$. In order to model the charge we have to estimate the capacitances

correctly. The different node capacitances are estimated as linearized gate, drain and

source capacitances. But these capacitances are highly voltage dependent, therefor they

are multiplied by a correcting factor. A network of 5 series-connected transistors with

different sizes is used, a fast input is applied to minimize the short-circuit current. The

dynamic power dissipation of the circuit, which is proportional to the charge (EQ. 2.5), is

estimated and compared to SPICE. The model capacitance estimates are corrected by a

factor between 0.5 and 1.
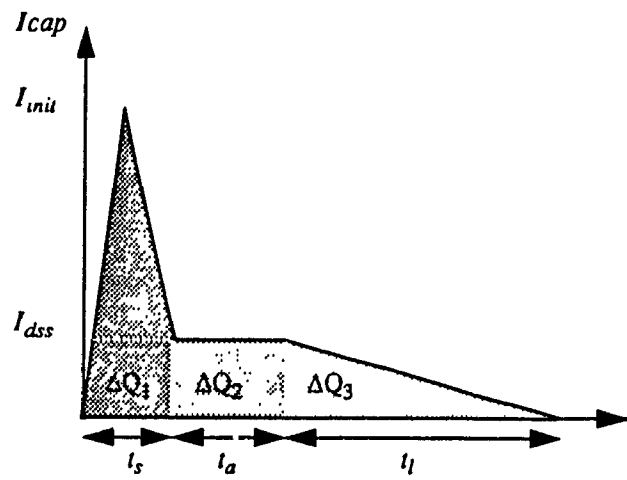
Fig. 6.21 Model fitting

CHAPTER 7

Conclusion

Supply current time domain waveforms are used by the designer to size the ground and power busses. Standard simulators are time consuming, and not practical for large VLSI circuits. Event driven simulators reduce the simulation time substantially. But reported current models have limitations and they may lead to inaccurate current estimation. In this thesis we presented a novel approach to estimate the supply current time-domain waveforms in CMOS VLSI circuits. Our approach is based on event driven simulation and a piece-wise linear analytical current model. An event driven timing simulation of the circuit is carried out. The results of the timing simulation are combined with the current estimation at the stage level to obtain the total supply current.

a- Piece-Wise Linear Current Model

We performed a detailed analysis of the supply current waveforms in CMOS gates. Based on this analysis we modeled the capacitive current with 4 waveforms and the short-circuit current with one waveform. These waveforms cover all the possibilities of the current waveforms depending on the stage characteristics. Different factors that affect the current waveforms are taken into account. The effects of the circuit topology, node capacitances and trigger position are considered. Input ramp and short-channel effects are modeled. Both short-circuit and dynamic current are included. The current model derived can be appended to any switch-level simulator to obtain accurate supply current waveforms.

b- Collapsing Technique

A new collapsing strategy is presented to model the supply current more accurately. Our model uses a pull-down (pull-up) equivalent circuit with two transistors as compared to the equivalent inverter method. The circuit is collapsed in different equivalent circuits in order to make an accurate estimation of the supply current

waveforms. When collapsing a gate to an equivalent circuit we pass maximum information to the collapsed gate. Therefore the equivalent circuit will have the same charge and delay as the original circuit. The collapsing method is sensitive to multiple input transitions. Especially in the case of a delayed trigger input occurring when the gate is still switching, the gate is collapsed again to include the new path(s) set by the input (section 2.6.4). The proposed collapsing technique is appropriate for complementary CMOS logic, but still gives good estimates for a general CMOS structure such as the parity generator circuit shown in Section 4.4 . The stage collapsing is dynamic (depends on the inputs to the stage) to include pass gates. Two kinds of stages are considered. Stages that correspond to logic gates, and stages made of a logic gate driving a pass gate (or a network of pass gates). These kinds of stages cover most of the standard CMOS circuits. The limitations of this method is the modelling of circuits with feedback and circuits that cannot be reduced with parallel/series transformations.

c- Results

Our approach compares favourably with SPICE (level 3) on the peak and average current and delay. A detailed comparison between our model and SPICE is performed on different circuits. Our model showed a maximum 5% deviation from SPICE on the average current, and a maximum 10% deviation on the instantaneous current. The event driven simulation has achieved a speed-up of 3 to 4 orders of magnitude compared to SPICE.

d- Implications and Future Work

Our current models can be added to standard switch level simulators to obtain the supply current waveforms. The proposed collapsing technique brings enhancements to event driven simulation. By combining our model and collapsing technique we achieve closer estimates of the supply current compared to previous approach. The implication of our approach is to develop fast and accurate current

estimation tool. This tool can be used to size the ground and power lines in VLSI chips. This work can be extended to determining the input vector (or input sequence) that causes the maximum current. The results may then be used to redesign the circuit to avoid these sequences and reduce the power consumption of the circuit.

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Appendix A-1

In this appendix we determine an expression for $v_1(t)$ during segment 1. In segment 1 T1 is in saturation and Tequ is in linear mode. The node equations of the equivalent circuit (Fig. 3.5) can be written as follows:

$$C_1 \frac{d}{dt} v_1(t) = \frac{\beta_1}{2} [V_e - v_2(t)]^2 \qquad \text{(EQ. A-1.1)}$$

$$\frac{\beta_1}{2} [V_e - v_2(t)]^2 = C_{equ} \frac{d}{dt} v_2(t) + \beta_1 \left[(v_2(t)) Vc - \frac{1}{2} v_2(t)^2 \right] \qquad \text{(EQ. A-1.2)}$$

EQ. A-1.1 can be rewritten as:

node 1 $\qquad dv_2 = A(v_2 - a_1)(v_2 - a_2) dt \qquad$ (EQ. A-1.3)

node 2 $\qquad dv_1 = -\frac{\beta_1}{2C_1} (v_2 - a_3)^2 dt \qquad$ (EQ. A-1.4)

where $\quad a_1, a_2 = \dfrac{nV_e + V_c}{n+1} \pm \left[(\dfrac{nV_e + V_c}{n+1})^2 - \dfrac{nV_c^2}{n+1} \right]^{1/2}$

$a_3 = V_e$

$A = \dfrac{\beta_{equ}(n+1)V_f}{nC_{equ}}$

Combining the EQ. A-1.3 and A-1.4 will lead to the following equation:

$$\frac{dv_1}{dv_2} = -\frac{\beta_1}{2C_1 A} \frac{(v_2 - a_3)^2}{(v_2 - a_1)(v_2 - a_2)} \qquad \text{(EQ. A-1.5)}$$

The closed-form solution for $v_1(t)$ is given by:

$$v_1(t) = C_1 [v_2 + K_1 ln(v2(t) - a_1) + K_2 ln(v2(t) - a_2)] \qquad \text{(EQ. A-1.6)}$$

where $v_2(t)$ is given by EQ. 3.8 and 3.9

$$C = \frac{AC_1\beta_1}{2}$$

$$k_1 = \frac{(a_2 - a_3)(2a_1 - a_3 - a_2)}{a_1 - a_2}$$

$$k_2 = \frac{(a1 - a2)(2a_2 - a_3 - a_1)}{a_2 - a_1}$$

Appendix A-2

In this appendix an expression of $v_2(t)$ during segment 1 is derived. The node 2 (Fig. 5.3) equation during segment 1 is given by:

$$C_{equ}\frac{d}{dt}v_2(t) = k_1(V_e - v_2(t)) - \frac{k_2}{1 + \frac{v_2(t)}{k_3}}(V_c - \frac{v_2(t)}{2})v_2(t) \qquad \text{(EQ. A-2.1)}$$

The solution of the above equation is given by:

$$\frac{t}{C_{equ}} = \frac{f(v2)}{C_{equ}} = -2\frac{g(v_2)k_3}{a} + (ln(2k_1V_ek_3 + 2k_1V_ev_2 - 2k_1v_2k_3 - 2k_1v_2^2$$

$$-2k_2k_3v_2V_c + k_2k_3v_2^2))/(-2k_1 + k_2k_3) \qquad \text{(EQ. A-2.2)}$$

$$-2\frac{g(v_2)}{(-2k_1 + k_2k_3)a}(-k_1V_e + k_1k_3 + k_2k_3V_c) + b$$

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where

$$a = k_1^2 V_e^2 + 2k_1^2 V_c k_3 - 2k_1 V_e k_2 k_3 V_c + k_1^2 k_3^2 + 2k_1 k_3^2 k_2 V_c + k_2^2 k_3^2 V_c^2 - 2k_1 V_e k_3^2 k_2$$

$$g(v_2) = \text{atanh}((-k_1 + k_2 k_3) v_2 + k_1 V_e - k_1 k_3 - k_2 k_3 V_c)$$

b is determined from the initial condition at t=0 and $v_2(0)$

Appendix A-3

An expression of v_1 as a function of v_2 is determined. This expression is used to determine the voltage drop of node 1 (Fig. 5.3) During segment 1. This is possible since v_2 is known at the beginning of segment 1 and at the end. The node equations of the equivalent circuit Fig. 5.3 are given by:

node 2 $$C_{equ}\frac{d}{dt}v_2(t) = k_1(V_e - v_2(t)) - \frac{k_2}{1 + \frac{v_2(t)}{k_3}}(V_c - \frac{v_2(t)}{2})v_2(t)$$

(EQ. A-2.3)

node 1 $$C_1\frac{d}{dt}v_1(t) = -k_1(V_e - v_2(t))$$

(EQ. A-2.4)

rewriting the above equations:

$$C_{equ}\frac{d}{dt}v_2(t) = \left(-\frac{k_1}{k_3} + \frac{k_2}{2}\right)\frac{[v_2(t) - v_{2ss1}][v_2(t) - v_{2ss2}]}{1 + \frac{v_2(t)}{k_3}}$$ (EQ. A-2.5)

(EQ. A-2.6)

$$C_1\frac{d}{dt}v_1(t) = -k_1(V_e - v_2(t))$$

ıere

$$v_{2ss1}, v_{2ss2} = \frac{1}{2}(-2k_1 V_e + 2k_1 k_3 + 2k_2 k_3 V_c \pm 2(k_1^2 V_e^2 + 2k_1^2 V_e k_3 - 2k_1 V_c k_2 k_3 V_e$$
$$+ k_1^2 k_3^2 + 2k_1 k_3^2 k_2 V_c + k_2^2 k_3^2 V_c^2 - 2k_1 V_e k_3^2 k_2)^{1/2}/(-2k_1 + k_2 k_3))$$

Combining the two equation we get:

$$\frac{d}{dv2} v1 = \frac{A\,[V_e - v_2(t)]\left(1 + \dfrac{v_2(t)}{k_3}\right)}{(v_2(t) - v_{2ss1})\,(v_2(t) - v_{2ss2})} \qquad \text{(EQ. A-2.7)}$$

Where $\quad A = -\dfrac{C_{equ}}{C_1}\dfrac{k_1}{-\dfrac{k_1}{k_3} + \dfrac{k_2}{2}}$

The solution for equation A-2.7 is given by:

$$\frac{v1}{A} = \frac{h(v2)}{A} = -\frac{v_2}{k_3} - \frac{(-V_e k_3 - V_e v_{2ss1} + k_3 v_{2ss1} + v_{2ss1}^2)\,ln\,(-v_2 + v_{2ss1})}{k_3\,(-v_{2ss2} + v_{2ss1})}$$

$$+ \frac{(-V_c k_3 - V_c v_{2ss2} + k_3 v_{2ss2} + v_{2ss2}^2)\,ln\,(-v_2 + v_{2ss2})}{k_3\,(-v_{2ss2} + v_{2ss1})} + Cte$$

$$\text{(EQ. A-2.8)}$$

Cte is determined from the initial condition $\quad h(v2(0)) = V_{DD}$

Appendix A-4

Given the equivalent circuit of Fig. 5.5. we neglect the affect of the pull-up current when determining the output voltage waveform as discussed in Section 3.4 this is a valid approximation for practical input rise times. The pull-down will start in the saturation region. In the case of a fast input, v_{in} will reach V_{DD} and stay constant at V_{DD} while the pull-down is still in the saturation. In the case of a slow input the pull-down will change to the linear mode while the input is still a ramp.

a- fast inputs

i- saturation region

When the input is still a ramp the output node equation is given by:

$$C_{out}\frac{dv_{out}}{dt} = -ve_{sat}C_{ox}WK\,(st-V_T) \qquad \text{(EQ. A-4.1)}$$

where $\quad K = \dfrac{1}{1 + \dfrac{E_cL_e}{st-V_T}}$

The solution of this equation is given by:

$$v_{out} = -\frac{ve_{sat}C_{ox}W}{c1}\left(\frac{1}{2}st^2 - V_Tt - tk_3 + \frac{k_3^2}{s}ln\,(st-V_T+k_3)\right) + Cte \qquad \text{(EQ. A-4.2)}$$

Where $\quad k_3 = E_cL_e$

Cte is determined from the initial condition $v_{out}(0) = V_{DD}$

$$Cte = V_{DD} + \frac{ve_{sat}C_{ox}W}{c1}\left(\frac{k_3}{s}ln\,(-V_T+k_3)\right)$$

Defining v_{step} as the output voltage when the input becomes V_{DD}

$$v_{step} = v_{out}(\frac{V_{DD}}{s})$$

When the input reaches V_{DD} the node equation becomes:

$$C_{out}\frac{dv_{out}}{dt} = -ve_{sat}C_{ox}WK\,(V_{DD}-V_T) \qquad \text{(EQ. A-4.3)}$$

where $\quad K = \dfrac{1}{1 + \dfrac{E_cL_e}{V_{DD}-V_T}}$

The solution for that equation is given by:

$$v_{out} = v_{step} - v_{sat}C_{ox}WK\,(V_{DD}-V_T)\,(t-\frac{V_{DD}}{s}) \qquad \text{(EQ. A-4.4)}$$

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depending on the case it can move to the linear region while the input is still rising or when the input is equal to V_{DD}.

ii- linear region

When the output voltage drops to V_{dsat} the pull down will be in the linear region and the node equation becomes:

$$C_{out}\frac{dv_{out}}{dt} = \frac{k_2}{1+\frac{st}{k_3}}(V_{DD} - V_T - \frac{v_{out}}{2})v_{out} \qquad \text{(EQ. A-4.5)}$$

The above equation cannot lead to a close-form solution and is rewritten as follows:

$$C_{out}\frac{dv_{out}}{dt} = \frac{k_2}{k_{short}}(V_{DD} - V_T - \frac{st}{2})st \qquad \text{(EQ. A-4.6)}$$

where k_{short} is a factor that models the velocity saturation effect.

we define $K_n = \dfrac{k_2}{k_{short}}$

The EQ. A-4.6 solution is given by:

$$\frac{1}{v_{out}} = e^{\frac{kV_{DD}}{2C_{equ}s}(st-n)^2}\left[\frac{1}{V_{dsat}e^{\frac{kV_{DD}}{2C_{equ}s}}} + \sqrt{\frac{\pi kV_{DD}}{8C_{equ}s}}\left(erf\left(\sqrt{\frac{\pi kv_{sat}}{8C_{equ}s}}\right) - erf\left(\sqrt{\frac{kst-n^2}{8C_{equ}s}}\right)\right)\right] \qquad \text{(EQ. A-4.7)}$$

b- slow inputs

In the case of a slow input, the pull-down will get out from the saturation region before the input reach V_{DD}.

i- saturation region

In the saturation region the output voltage is given by:

$$v_{out} = -\frac{v_{sat}C_{ox}W}{c1}\left(\frac{1}{2}st^2 - V_Tt^2 - tk_4 + \frac{k_4}{s}\ln(st - V_T + k_4)\right) + Cte$$

(EQ. A-4.8)

Where $\quad k_4 = E_cL_e$

$$Cte = \dot{V}_{DD} + \frac{v_{sat}C_{ox}W}{c1}\left(\frac{k_4}{s}\ln(-V_T + k_4)\right)$$