Switched-Current Circuit Design Techniques for Signal Processing

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ABSTRACT

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A complete digital signal processing system requires analog circuits acting as interfaces between the digital system and the outside world that is mostly analog. Usually, these circuits are designed by using switched-capacitor (SC) techniques. However, there are two problems with the SC circuits. One is that the process technology used for these circuits are not compatible with the standard digital process technology and the other is that performance of these circuits worsens for low-voltage operations. To overcome these problems, a new technique called the switched-current (SI) technique has been proposed recently. Due to the problems such as accuracy, dynamic range, and linearity, SI circuits are still less attractive than SC circuits. Further, the SI technique being a new technology, there are many application related problems that are yet to be resolved.

In this thesis, several new SI design techniques are proposed to provide improved performance and to resolve the application related problems of the SI circuits. Specifically, the present investigation is aimed at developing SI techniques for the design of high-performance building-block cells, programmable filters, and ratio-independent algorithmic D/A and A/D converters.

A high-performance SI memory cell design technique, based on the use of a single-ended differential amplifier, is proposed. The new technique uses differential amplifier as the input stage and a complementary regulated cascode circuit as the output stage of the memory cell. Theoretical analysis shows that the memory cell can achieve a very low gain

error, small harmonic distortions, and a wide dynamic range. Two example memory cells are designed by using the structures of a transconductance amplifier and a folded cascode amplifier, respectively. The simulation results show that the proposed memory cells give better performance as compared with other existing memory cells. Both the proposed cells are implemented using the standard 1.2 μ N-well CMOS process technology. The prototype chip test results show that the cells have the gain error less than 0.1 dB and harmonic distortions less than -61 dB.

A fully-programmable SI filter design technique based on the use of digital filter structures is proposed. The resulting SI filters have very regular structures and the coefficients of the filter transfer function are directly matched to the sizes of the transistors. Infinite impulse response filters (IIR) are designed using the proposed high performance memory cells. A prototype chip consisting of six second-order IIR filters is designed and implemented using the standard 1.2 μ CMOS process technology. The chip test results are seen to be in agreement with those theoretically predicted or obtained through simulation.

A novel SI ratio-independent algorithmic multiplication D/A converter design techniques is proposed. A new design circuit for A/D converter is also presented. The designed converters are capable of achieving high-resolution and high-accuracy data conversion without requiring matching of the components. The conversion errors caused by non-ideal MOS devices are studied. A practical SI ratio-independent D/A converter circuit is designed using the proposed SI memory cells. A prototype D/A converter chip is designed and implemented using the standard 1.2 μ N-well CMOS process technology and tested. The test results show that the converter achieves an 8-bit resolution with nonlinearity error less than one-half of the least significant bit.

Acknowledgements

I would like to take this opportunity to thank my supervisor, Dr. M. Omar Ahmad, for his able and tireless guidance throughout the course of this research. His invaluable advice, assistance, and inspiration are the keys to the success of this work.

I would like to thank my colleagues Zhao Zhen for carrying out some of the simulation work and Limin Chen for her help in testing the prototype chips in this investigation. I would also like to expresses my appreciation to Dave Hargreaves and Girish Patel for their help in providing the necessary support in the VLSI Laboratory during the course of this investigation

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List of Symbols and Abbreviations

β	MOS transistor gain factor
λ	Channel length modulation factor
f_s	Sampling frequency
f_i	Input signal frequency
g_o	Output transconductance
I_i	Input current
I_o	Output current
I_{ref}	Reference current
k_p	Process gain factor
V_{dd}	Power supply voltage
V_{dp}	Power supply distortion
V_{ref}	Reference voltage
ω_n	Normalized 3-db frequency
A/D	Analog-to-digital
D/A	Digital-to-analog
DMC-I	Differential memory cell I
DMC-II	Differential memory cell II
DSP	Digital signal processing
FDMC	Fully differential memory cell
IIR	Infinite Impulse response
LSB	Least significant bit
MSB	Most significant bit
PSRR	Power supply rejection ratio
RCMC	Regulated cascode memory cell
R_p	Passband ripple
R_s	Stopband ripple
SC	Switched-Capacitor
SI	Switched-Current
S/H	Sample-and-hold
THD	Total harmonic distortion

Chapter 1

INTRODUCTION

In the past two decades, the field of digital signal processing (DSP) has experienced a very rapid growth and recognition in many areas of science and engineering such as telecommunications, robotics, geophysics, medicine etc. This upsurge in DSP related activities can be attributed mainly to the recent development in the very large scale integration (VLSI) technology that has allowed the integration of ever powerful DSP systems into inexpensive chips. While the increased performance and reduced cost of integrated-circuit DSP systems have brought a universal acceptance of the usefulness of the area of DSP, there are still some problems that limit the integration of a complete DSP system into a single chip. A single-chip DSP system is a mixed analog and digital integrated circuit that requires analog circuits, such as digital-to-analog (D/A) and analog-to-digital (A/D) converters, sample-and-hold (S/H) circuits, prefilters, postfilters, etc., acting as interfaces between the digital systems and the outside world that is mostly analog [1], [2]. Figure 1.1 shows the block diagram of a complete DSP system.

Many techniques, with the switched-capacitor technique being the most common one, have been developed for the design and implementation of these analog circuits. However, these techniques are not suitable for the design and implementation of a mixed analog and digital circuit DSP system as a single chip. Design and implementation of an

efficient mixed analog and digital chip requires that the analog circuits use the process technology that is compatible with that of the digital circuits, and that both the analog and digital circuits use the same power supply.

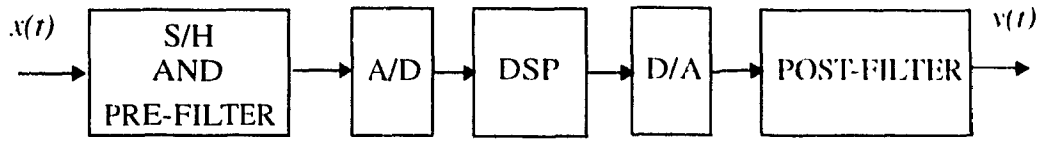


Fig. 1.1. A complete signal processing system

1.1 Switched-Capacitor Techniques

A switched-capacitor (SC) circuit is an analog sampled data circuit that realizes an analog signal processing task using an analog sampled data processing technique. Switched-capacitor circuits do not require absolute accuracy of the resistors and capacitors. In a SC circuit, resistors can be replaced by switches and capacitors. The result is that the circuit performance is determined by the ratios of the capacitors rather than their absolute values. Ratios of the elements are always easier to control in an IC process technology [3]. This advantage of the SC technique make the SC circuits very suitable for MOS process technology. However, there are still two outstanding problems that are yet to be resolved.

The first is that the switched-capacitor circuits need linear floating capacitors that act as storage components. This requires the use of double poly process which is not compatible with the standard digital VLSI process technology. As the analog part of a single-chip DSP system may occupy as much as 10 ~ 20% of the total chip area, the required extra processing becomes disproportionately high.

The second problem is that the performance of a switched-capacitor circuit worsens for low power supply voltages. In future, as the feature sizes shrink further into the sub-

micron region, digital systems with higher circuit density will be possible. But this will lead to higher power dissipation. Further, smaller dimensions will create higher device electric fields resulting in a poorer MOSFET performance. To contain this situation, the industry has proposed lowering of the standard power supply from 5 V to 3.3 V [4]. In that case, the VLSI process technology will have to be optimized for the digital performance rather than the analog performance. The threshold voltage will be lowered, and logic gate leakage will prevent it from being reduced far enough for an optimum switched-capacitor performance. The performance of a switched-capacitor circuit will suffer doubly in this case: the reduced voltage swings will have a direct impact on the dynamic range, and the sub-optimal threshold voltages will worsen the performance of MOS switches [5], [6]. Although the extra threshold options beyond the requirement of that of digital circuits could help the SC circuits maintain their performance, this will increase the process cost and make the SC circuits to be less attractive.

1.2 Switched-Current Techniques

To overcome the limitations of the SC circuits mentioned above, researchers have proposed many new techniques that are mostly current mode circuits for analog signal processing [7], [8], [9]. Specifically, the switched-current technique (SI) proposed by J. B. Hughes, N. C. Bird and L. C. Macbeth in 1989 [7], and a similar technique called the current copier technique, proposed by S. J. Daubert, D. Vallancourt, and Y. P. Tsividis in 1988 [8], are analog sampled data circuits, in which signals are represented by currents rather than voltages. The SI technique relies on the ability of a MOS transistor to maintain its drain current with its gate opened by the charge stored on its gate capacitor. This means that the SI circuits do not require linear floating capacitors, and the double poly process technology is thus not required. This makes the SI circuits fully compatible with the standard digital VLSI process technology. Further, since SI circuits work in the current

domain, the power supply voltage can be reduced.

The SI circuits are still less attractive than the SC circuits due to the problems of lower accuracy, smaller dynamic range, non-linearity etc. Since the SI technique is a new technique, there are still many application problems not yet resolved. Furthermore, in the area of VLSI design, the design automation is an important evaluation parameter of any new design technique. If its automation level is low, it will be less attractive to designers. A wide-range application of SI circuits in VLSI design will, to a great extent, depend on the automation level of the design technique used.

1.3 Scope and Organization of the Thesis

The objective of this research is (i) to investigate the problems of low accuracy and small dynamic range of SI circuits, (ii) to propose a SI building block that has a low current-gain error, a wide dynamic range and small harmonic distortion, and (iii) to develop efficient SI design and implementation techniques for analog circuits, such as filters and converters encompassing the features of programmability and design automation. The focus throughout this investigation is on the simplicity of the design technique and implementation with good performance of the resulting circuits.

In Chapter 2, the basic concepts and the principle of the SI techniques are reviewed, and some applications of the SI techniques in signal processing are discussed. The effects of non-ideal MOS devices on a simple memory cell are studied. An overview of some of the existing SI memory cells is also given in this section.

Since the memory cell is the basic and most important building block used in SI systems, the characteristics of a SI memory cell will determine the performance of the overall system. Therefore, the design of a high-performance SI memory cell is essential for a SI circuit. Chapter 3 proposes a new high-performance SI memory cell design technique.

Using this technique, two differential SI memory cells are designed. The behavior of the new memory cells are analyzed and simulated using HSPICE. The simulation results are compared with other memory cells. The new memory cells are also implemented with a standard 1.2 μ N-well CMOS process technology and tested in the laboratory.

Since filtering is a major application of a SI technique, in Chapter 4, a new design technique for fully-programmable switched-current filter is described. The filter consists of unit delays, coefficient multipliers and adders. The objective here is to develop a design methodology that is simple and yields filters whose structure is regular. As an example, a second-order IIR filter is designed using the developed technique, and implemented using the SI memory cell designed in Chapter 3. The filter is simulated by using HSPICE and the results are analyzed using FFT. An experimental prototype second-order switched-current IIR filter array consisting of six second-order filters is fabricated with the standard 1.2 μ CMOS process technology. The hard-wiring technique is used for programming of these filters. The test results are also given in this chapter.

In Chapter 5, new SI ratio-independent algorithmic multiplication D/A converter design technique is presented. The design technique is aimed at achieving high-resolution and high-accuracy data conversion without requiring matching of components. A new design circuit for SI A/D converter is also presented. The effects of non-ideal characteristics of MOS transistors on the designed converters are studied. Using the differential SI memory cell proposed in Chapter 3, the effects of switch charge injection and finite impedance are reduced to improve the conversion accuracy in the designed D/A converter. A prototype D/A converter chip is implemented with the standard 1.2 μ CMOS process technology and tested in the laboratory.

Chapter 6 gives the conclusions of the present investigation and suggests some future works in the area.

Chapter 2

REVIEW OF THE SI TECHNIQUES

A SI system may be thought of as a system using analog sampled data circuits in which signals are represented by current samples. The basic circuit element of a SI system is called the SI memory cell. It can sample and hold the current signals through the charge stored on the gate capacitor of a MOS transistor. Using this current memory cell, SI integrators, differentiators, and delay blocks can be built. SI filters can be designed using these blocks. As with the SC technique, the SI technique can also be used for the design of A/D and D/A converters. In this chapter, the principle of operation of a SI memory cell is reviewed, followed by an introduction of SI integrators and differentiators. Next, SI filters using these blocks are discussed. The applications of the SI technique in A/D and D/A converters are also given through some examples. Since the non-ideal characteristics of MOS devices affect the performance of the SI circuit significantly, the analysis of these effects to the simple memory cell are introduced. Finally, an overview of existed SI memory cells with improved performance is given and their advantages and disadvantages are discussed.

2.1 Principle of the SI Technique

The principle of operation of the SI technique can be described in terms of the operation of a SI memory cell. There are two basic types of SI memory cells referred to as the

first- and second-generation current memory cells. Fig. 2.1 shows a first-generation current memory cell. It is a simple current mirror with a switch S separating the gates of two transistors. When the switch S is closed, the circuit works in the sample mode and both gate capacitors, C_{g1} and C_{g2}, are charged to V_{gs}, establishing the drain current $I_{d1} = J + I_i$. By normal current mirror action, we have $I_{d2} = -AI_{d1}$ and this results in the output current $I_o = -AI_i$. Therefore, the current I_o is available simultaneously with the input sample. When S is opened, the circuit is in the hold mode, a voltage close to V_{gs} is held on C_{gs2}, and the circuit maintains the output current I_o close to the value of $-AI_i$.

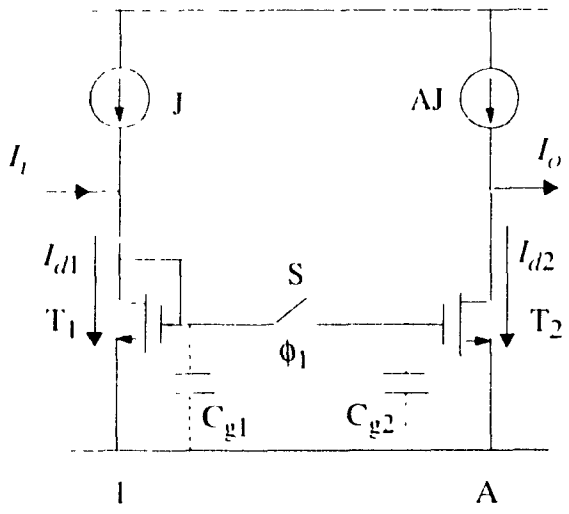


Fig. 2.1 A first-generation SI memory cell

A second-generation SI memory cell is shown in Fig. 2.2. The operation of this cell is as follows. On clock phase ϕ_1, switches S_1 and S_2 are closed and S_3 is opened. The memory MOS transistor T_1 is diode-connected. The drain current of T_1 becomes $J + I_i$ and it charges the gate capacitor C_g. A gate voltage V_g that is required to maintain the drain

current of $J + I_i$ is established and it is stored on the gate capacitor C_g. On phase ϕ_2, S_1 and S_2 open and S_3 closes. Since C_g remains charged with the voltage V_{gs}, T_1 maintains the drain current $J + I_i$, and therefore, the output current I_{o1} of the memory cell is equal to $-I_i$ which is an inverted copy of the input current. To scale the current, an extra output stage can be used to give $I_{o2} = -AI_i$. Since the transistor T_1 is used alternately as an input diode and as an output transistor, I_{o1} is available only during phase ϕ_1. The output current I_{o2} is available for the whole period, as with the first-generation memory cell

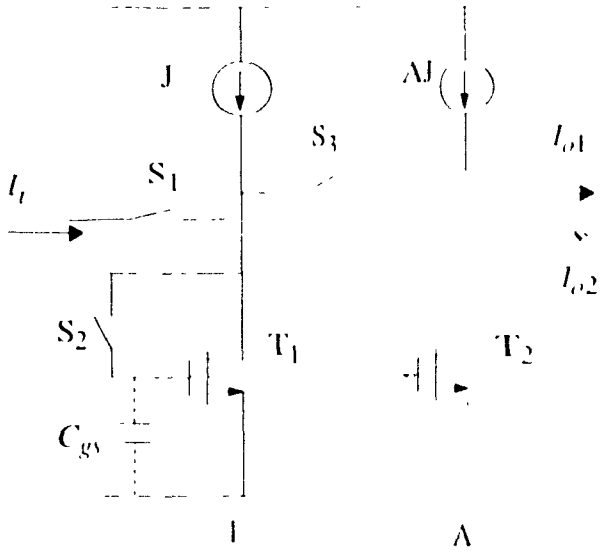


Fig. 2.2 A second-generation SI memory cell

Obviously, the memory cells discussed above require only a grounded capacitor to hold the voltage V_{gs} at the value imposed by the current $J + I_{in}$. With ideal MOS transistor, the current is transferred linearly from the input to the output without requiring linear capacitors.

2.2 SI Integrators and Differentiators

Using the SI memory cells discussed in Section 2.1, with proper switch clock sequence, we can build a SI integrator or a SI differentiator. In [6] and [7], several different SI integrators and differentiators have been introduced. Either the first- or second-generation SI memory cell can be used to design a SI integrator or a differentiator. Fig. 2.4 shows a non-inverting SI integrator [6] which is built using the second-generation memory cell. The operation of the circuit is as follow. On phase ϕ_2 of the clock period n-1, transistor T_2 is diode-connected and its drain current I_2 is given by

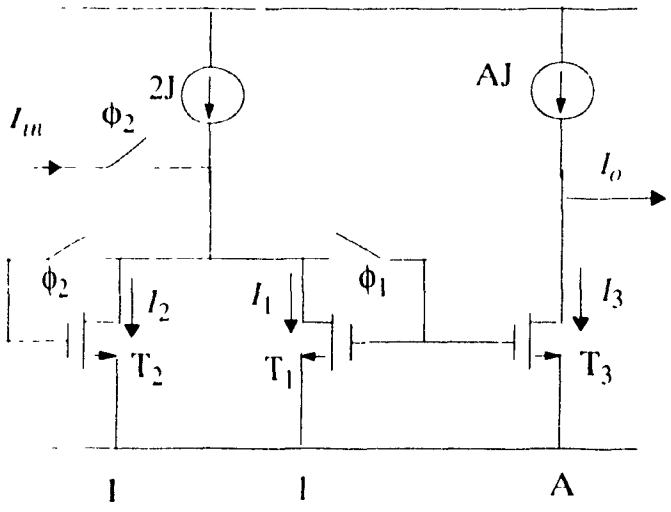


Fig. 2.3 A second-generation SI non-inverting integrators

$$I_2 = 2I + I_{in}(n-1) - I_1 \quad \text{(EQ. 2.1)}$$

and the drain current I_3 of T_3 is given by

$$I_3 = AI_1 - AJ - I_o(n-1) \quad \text{(EQ. 2.2)}$$

By substituting (EQ. 2.2) into (EQ. 2.1), I_2 becomes

$$I_2 = J + I_{in}(n-1) + \frac{I_o(n-1)}{A} \qquad \text{(EQ. 2.3)}$$

On the next phase ϕ_1 of the clock period n, the transistor T_1 is diode connected and its drain current I_1 is given by

$$I_1 = 2J - I_2 = J - I_{in}(n-1) - \frac{I_o(n-1)}{A} \qquad \text{(EQ. 2.4)}$$

The output current I_o at the clock period n now becomes

$$I_o(n) = AJ - I_3 = AJ - AI_1 = I_o(n-1) + AI_{in}(n-1) \qquad \text{(EQ. 2.5)}$$

From this equation, the z-domain transfer function can be written as

$$H(z) = \frac{I_o(z)}{I_{in}(z)} = \frac{Az^{-1}}{1-z^{-1}} \qquad \text{(EQ. 2.6)}$$

This transfer function corresponds to a forward-Euler z-transform transfer function of a lossless integrator [6].

By changing the input current sampling phase, the non-inverting SI integrator becomes an inverting integrator. Fig. 2.4 shows the second-generation inverting SI integrator. Its z-domain transfer function is given by

$$H(z) = \frac{I_o(z)}{I_{in}(z)} = -\frac{A}{1-z^{-1}} \qquad \text{(EQ. 2.7)}$$

This transfer function corresponds to a backward-Euler z-transform transfer function of a lossless integrator [6].

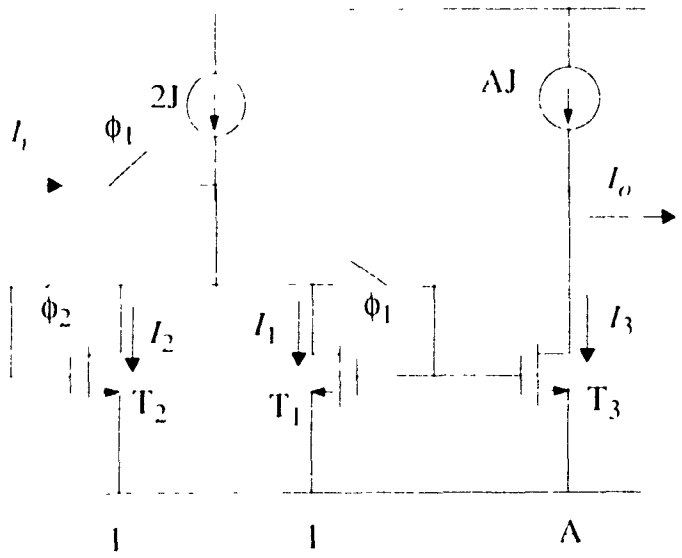


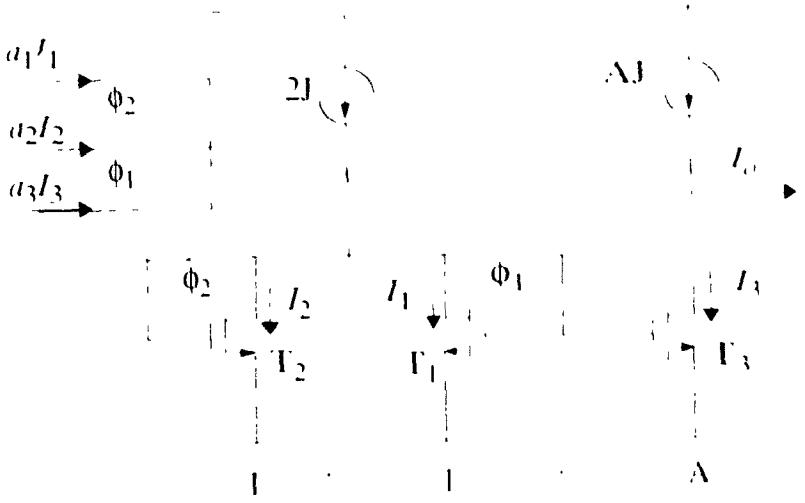
Fig. 2.4 A second-generation SI inverting integrator

Fig. 2.5 shows a SI integrator with multiple inputs. The forward-Euler, backward-Euler and feed-forward input currents are weighted with a_1, a_2 and a_3 by scaling the W/L ratios of the output stages supplying these input currents. The output stage has a unit weight. The output current in the z-domain is given by

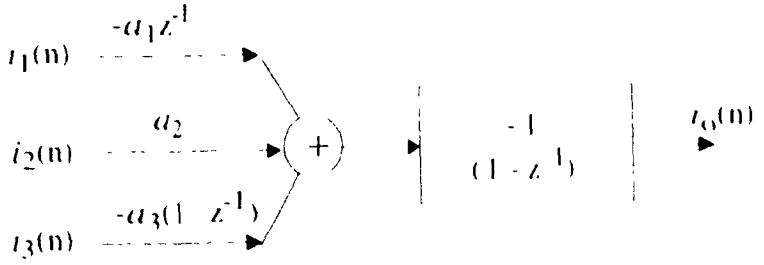
$$I_o(z) = \frac{A_1 z^{-1}}{1 - z^{-1}} I_1(z) - \frac{A_2}{1 - z^{-1}} I_2(z) - \frac{A_3(1 - z^{-1})}{1 - z^{-1}} I_3(z), \qquad \text{(EQ. 2.8)}$$

where $A_1 = a_1$, $A_2 = a_2$ and $A_3 = a_3$.

Using the SI memory cells, the SI differentiators can also be built. Fig. 2.6 shows a second-generation SI inverting differentiator. The operation of the differentiator is follows.



(a) Circuit schematic



(b) The z-domain block diagram

Fig. 2.5 A second-generation SI integrator with multiple inputs

On phase ϕ_2 of the clock period n-1, transistor T_1 is diode-connected and its drain current I_1 is given by

$$I_1 = J + I_1(n-1) \qquad \text{(EQ. 2.9)}$$

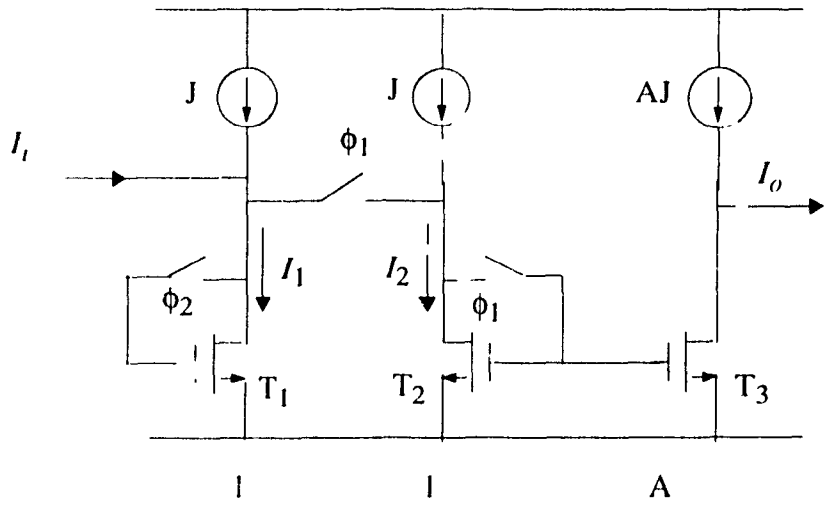


Fig. 2.6 A second-generation SI inverting differentiator

On the next phase ϕ_1 of clock period n, transistor T_2 is diode-connected and its drain current I_2 is given by

$$I_2 = J + I_i(n) - I_i(n-1) \qquad \text{(EQ. 2.10)}$$

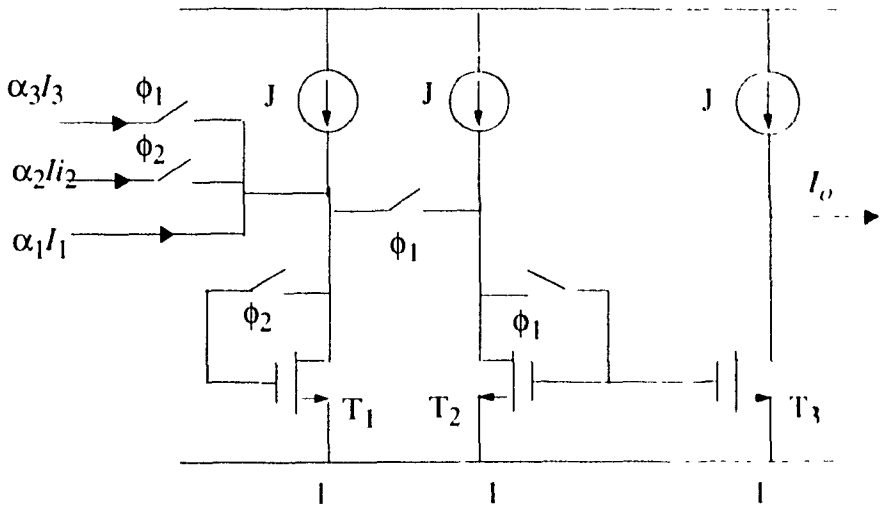
By the current mirror operation of T_3, the output current I_o is given by

$$I_o(n) = (-A)\,[I_i(n) - I_i(n-1)], \qquad \text{(EQ. 2.11)}$$

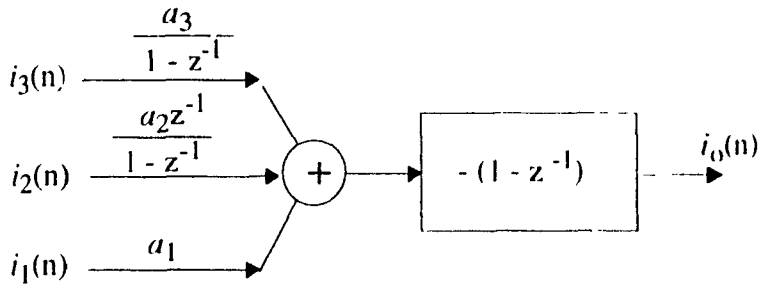
and thus, the z-domain transfer function of the differentiator is obtained as

$$H(z) = \frac{I_o(z)}{I_i(z)} = -A\,(1 - z^{-1}) \qquad \text{(EQ. 2.12)}$$

This equation represents a backward-Euler lossless differentiator [6].



(a) Circuit schematic



(b) The z-domain block diagram

Fig. 2.7 A second-generation SI differentiator with multiple inputs

As with the SI integrator, for a multi-input application, all input currents can be connected to the input of the differentiator directly. Fig. 2.7 shows a differentiator with multi-

ple inputs [6]. The output current of the differentiator is given by

$$I_o(z) = -a_1(1-z^{-1})I_1(z) + a_2 z^{-1} I_2(z) - a_3 I_3(z) \qquad \text{(EQ. 2.13)}$$

The first term of the equation corresponds to the backward Euler mapping of a lossless differentiator, the second term to a unit delay, and the third term to inversion and feed-forward operations.

2.3 SI Filters

Filtering is a major application of the switched-current technique. There are a number of papers dealing with the SI filter design [10],[11],[12]. Since the SI integrator and differentiator, from the transfer function point of view, correspond directly to the switched-capacitor integrator and differentiator, respectively, all the synthesis techniques developed for the design of switched-capacitor filters can be used for synthesizing switched-current filters. Mapping from a SC filter to a SI filter is a straight forward process with the second-generation integrator, as there is a direct correspondence between capacitor ratios in the SC filter and aspect ratios W/L in the SI counterpart.

As an example, a z-domain block diagram of a biquadratic section [5] is shown in Fig. 2.8 and its transfer function is given by

$$H(z) = \frac{I_o(z)}{I_i(z)} = \frac{(a_5 + a_6)z^2 + (a_1 a_3 - a_5 - 2a_6)z + a_6}{(1 + a_4)z^2 + (a_2 a_3 - a_4 - 2)z + 1} \qquad \text{(EQ. 2.14)}$$

The circuit implementation with second-generation SI inverting integrator and non-inverting integrator is shown in Fig. 2.9 [6]

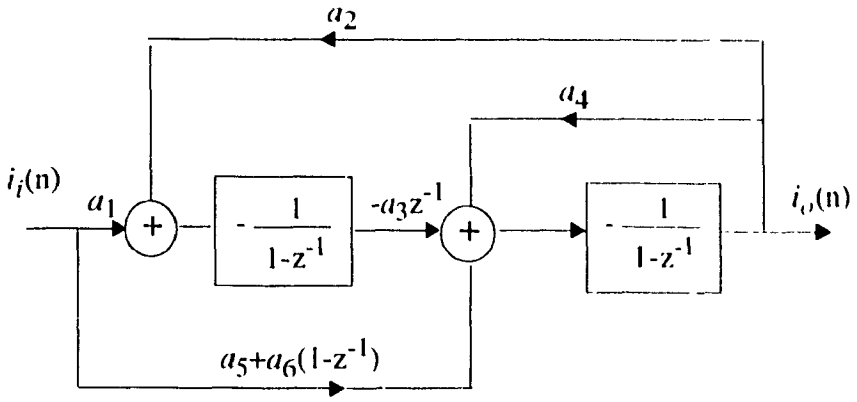


Fig. 2.8 A z-domain block diagram of an integrator-based biquadratic section

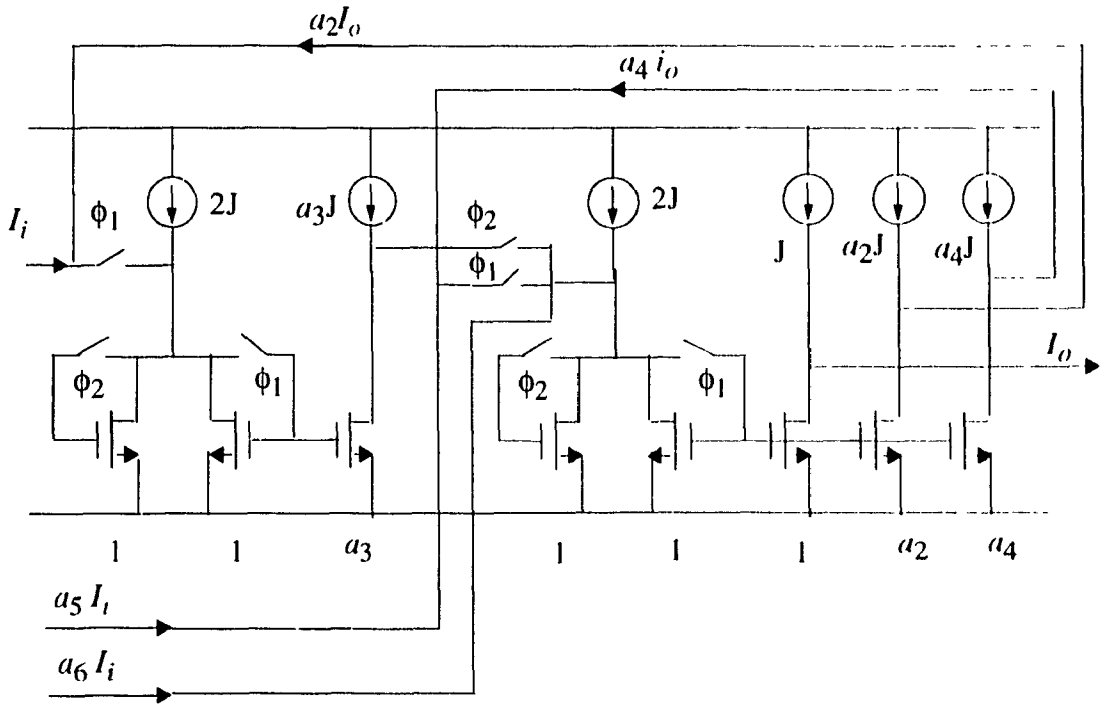


Fig. 2.9 A second-generation SI integrator-based biquadratic section

2.4 SI D/A and A/D Converters

The switched-current technique is an attractive means of implementing data conversion schemes, since switched-current circuits do not require linear capacitors and, in general, are capable of working with low supply voltages.

Some switched-current D/A and A/D converters have been proposed that use algorithmic structure or Σ-Δ modulator [13], [14], [15], [16]. Fig. 2.10 shows a simple example

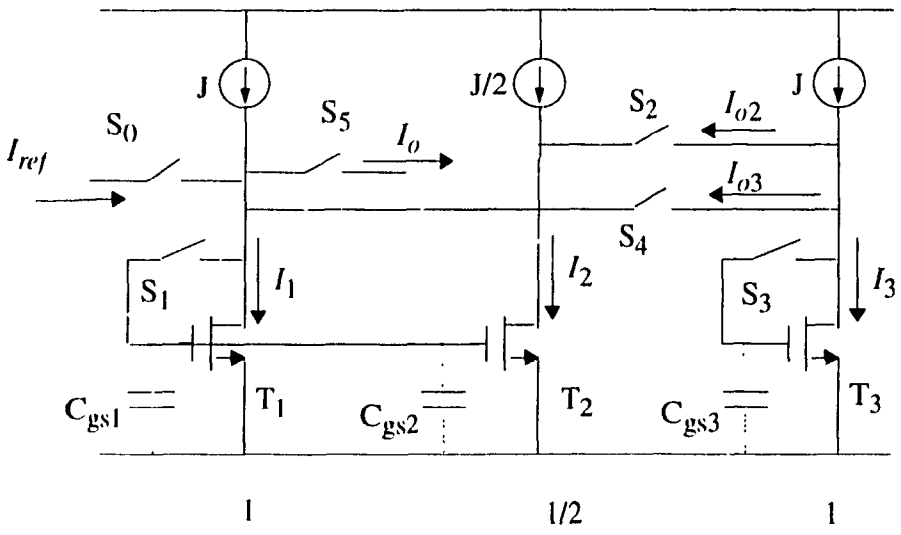


Fig. 2.10 A SI algorithmic D/A converter

of an algorithmic D/A converter. The circuit consist of two SI memory cells. The memory cell T_1 has an extra 1/2 scaling stage used for the implementation of divide-by-two function. The operation of the conversion is started from the least significant bit (LSB). Conversion of each bit (one conversion cycle) needs 2 clock cycles. The operation of the converter is as follows. In the first clock cycle, switches S_0 and S_1 are closed if the first digital bit is '1', the current I_1 is set to (J + I_{ref}). The current I_2 becomes (J + I_{ref})/2 and therefore, I_{o2} equals to I_{ref}/2. The reference current is divided by two at this point. If first digital bit is '0', S_0 is opened. The current I_1 equals to J, I_2 equals to J/2, and therefore, I_{o2}

is zero. The transistor T_3 samples and holds I_{o2} by closing the switches S_2 and S_3 and $I_3 = J + I_{o2}$. Next, S_1 and S_4 are closed, $I_{o3} = J - I_3 = I_{o2}$. If the second digital bit is '1', S_0 is closed, T_1 samples and holds the reference current and the current from T_3, the current I_1 is set to $J + I_{ref} + I_{o3}$. If the second digital bit is '0', T_1 only samples and holds the current from T_3, and I_1 will be set to $(J + I_{o3})$. The operation is repeated until the most significant digital bit (MSB) is converted. In contrast, T_1 adds and holds the current signals from switches S_0 and S_4 at every conversion cycle, and this current is divided by two and loaded into T_3 through T_2. In other words, during each conversion cycle the previous conversion current is divided by two and added with the reference current or the zero current. The algorithm of the D/A converter, therefore, is given by

$$I_o(n) = I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k \qquad \text{(EQ. 2.15)}$$

At the end of the conversion, switch S_5 is closed to present the converted current to the output. The accuracy and resolution of the D/A converter is limited by the ratio-error of T_1 and T_2.

Fig. 2.11 gives an example of an A/D converter that uses ratio-independent algorithmic conversion operation[16]. The advantage of the circuit is that the conversion accuracy is not dependent on the ratio of transistors. The conversion starts with the MSB. The operation of the A/D converter is as follows. In the beginning, switches S_1, S_2 and S_3 are closed, the current $I_1 = I_i$. Then, switches S_2 and S_3 are opened while S_4 and S_5 are closed, and the current $I_2 = I_i$. Both currents I_1 and I_2 are loaded into T_3 by opening S_1 and S_5 and closing S_2, S_4, S_6 and S_7. The current I_3 now becomes $2I_i$. Then, opening the switches S_2, S_4 and S_7, and closing S_6 and S_8, the doubled input signal $2I_i$ is compared with the reference current I_{ref}. If the signal exceeds the reference, the MSB is a '1', otherwise it is a '0'. To convert the next bit, the signal current, which is stored in T_3, is loaded into T_1 by clos-

ing S_2, S_3 and S_6. If the previous output digital bit is '1', S_8 is closed and the signal current in T_3 is subtracted by the reference current. If the previous output digital bit is '0', S_8 is opened, and the signal in T_3 remains unchanged. Once T_1 is set, T_2 is also set in a similar way. The conversion is then repeated with the same operation as with the MSB operation and it continues until the desired resolution is achieved.

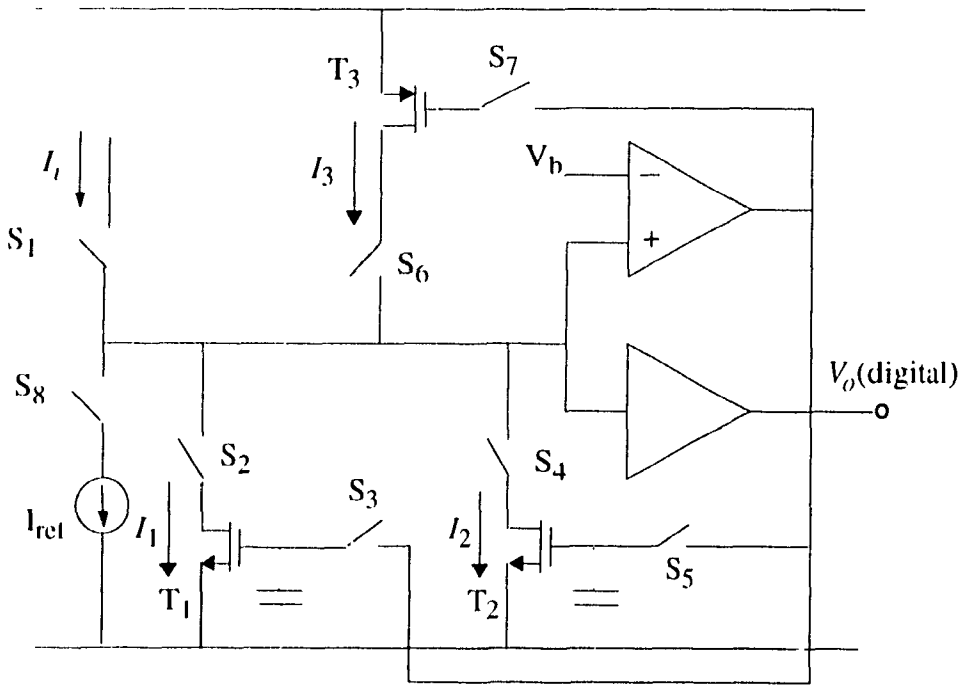


Fig. 2.11 A current mode ratio-independent algorithmic A/D converter

The conversion speed of the circuit is 4 clock cycles for each bit of conversion. Thus, an N-bit conversion requires 4N clock cycles. The maximum conversion accuracy and resolution is limited by the switch charge injection and the finite impedance of the MOS transistors.

2.5 Analysis for the Effects of Non-Ideal MOS Devices

So far, we have reviewed the principle of the SI technique and their applications. However, the performance of these SI circuits is based on the assumption of employing ideal MOS devices. As we know, a MOS device in practice is never ideal. A SI circuit will suffer from degraded performance through analog errors resulting from the non-ideal MOS transistor characteristics. In this section, we will study the effects of using non-ideal MOS devices through an analysis of the second- generation SI memory cell, hereafter designated as the simple memory cell.

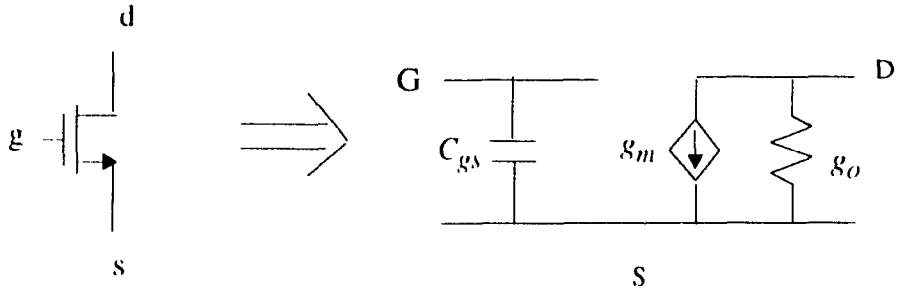
The non-ideal characteristics of MOS transistors stem from:

1. Channel length modulation caused by the drain voltage variation resulting from the changes in the drain current.
2. Gate-drain and gate-source parasitic capacitances, and channel charge that produce the switch charge injection resulting in memory current error and harmonic distortion.
3. Non-zero closure resistance of MOS switches causing incomplete charging of the memory transistor gate capacitor when the transistor is diode-connected, and thus leading to settling time error.
4. Process mismatches between the memory transistor and scaling transistors (current mirror transistors) causing current gain error, offset error, and harmonic distortion.
5. MOS transistor thermal noise and 1/f noise resulting in memory current errors.

Since the thermal noise and 1/f noise are not significant in SI circuits [6] as compared with other errors, they are not considered in this thesis.

2.5.1 Effects of Channel Length Modulation and Non-Zero Closure Resistance

The channel length modulation, also called the finite impedance problem, is caused by the channel shortening of the MOS transistor. When the simple SI memory cell works in the sample mode, the memory transistor's drain voltage is forced to be of the same value as the gate voltage. When the memory cell works in the hold mode, the gate voltage is held almost constant and the memory transistor outputs a current to its load. If the drain voltage changes, the output current also changes because of the channel length modulation. The change in drain voltage causes an error in the output current.



(a) An NMOS transistor (b) Equivalent circuit

Fig. 2.12 An NMOS transistor equivalent circuit

Fig. 2.12 shows the small signal equivalent circuit of an NMOS transistor. When considering the channel length modulation effect, the drain current of a MOS transistor is given by

$$I_d' = \frac{\beta}{2}(V_{gs} - V_t)^2(1 + \lambda V_{ds}) \qquad \text{(EQ. 2.16)}$$

where λ is the channel length modulation factor, $\beta = k_p(W/L)$, and k_p is the process gain factor. This effect may be modified for small signals by a drain conductance g_o and it is given by

$$g_o = \frac{\partial I'_d}{\partial V_d} = \lambda I_d \quad , \qquad \text{(EQ. 2.17)}$$

where I_d is the ideal drain current. When considering a cascaded SI memory cell application, a current error is produced due to the output conductance g_{o1} of the previous stage, the output conductance g_{o2} of the present stage, and the non-zero closure resistance $1/g_3$ of the MOS switch. Fig. 2.13 illustrates the effects of the finite output impedance of MOS devices. With the finite output impedance of MOS transistors, the input current i' to the next SI memory cell is given by

$$i' = \frac{i}{1 + \dfrac{g_{o1} + g_{o2}}{g_{m2}} + \dfrac{g_{o1}}{g_3}} \qquad \text{(EQ. 2.18)}$$

Letting $g_{o1} = g_{o2} = g_o$, and since in typical applications, $g_o << g_m, g_3$, (EQ. 2.18) can be rewritten as

$$i' \approx i\left(1 - \frac{2g_o}{g_{m2}} - \frac{g_o}{g_3}\right) \qquad \text{(EQ. 2.19)}$$

Hence, the error current Δi due to the finite impedance is given by

$$\Delta i = i - i' \approx i\left(\frac{2g_o}{g_{m2}} + \frac{g_o}{g_3}\right) \qquad \text{(EQ. 2.20)}$$

Thus, it is obvious that the channel length modulation of the memory MOS transistors and

non-zero closure resistance of MOS switch produce a current gain error. Usually, when the signal current is small, the effect of the non-zero closure resistance $1/g_3$ of the switch can be ignored. The error current then becomes

$$\Delta I = I - I' = I\left(\frac{2g_o}{g_{m2}}\right) \qquad \text{(EQ. 2.21)}$$

However, when signal current is large, such as in D/A or A/D converter applications, the non-zero closure resistance affects the SI circuit performance. To reduce the effect of channel length modulation, there are two solutions. The first is to keep the drain voltage constant and the second is to increase the output resistance of the memory cell.

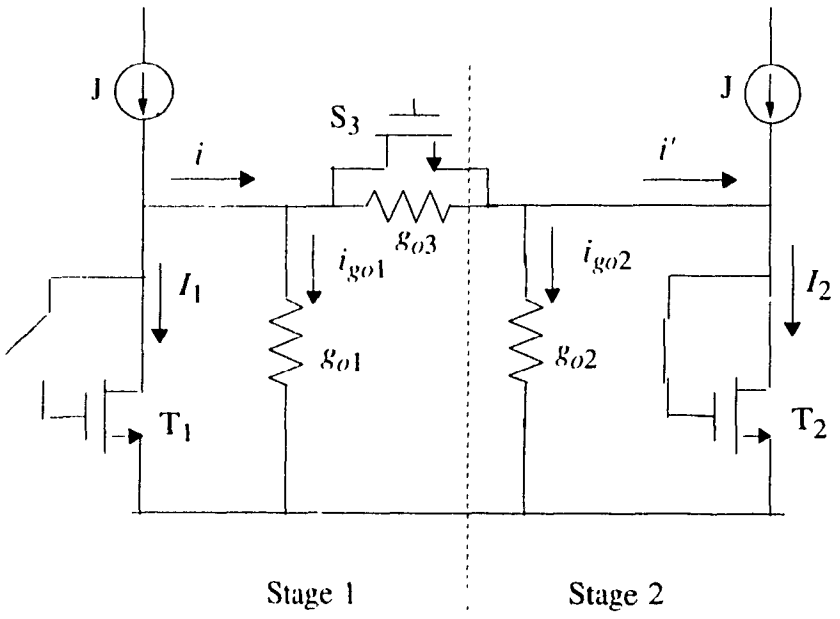
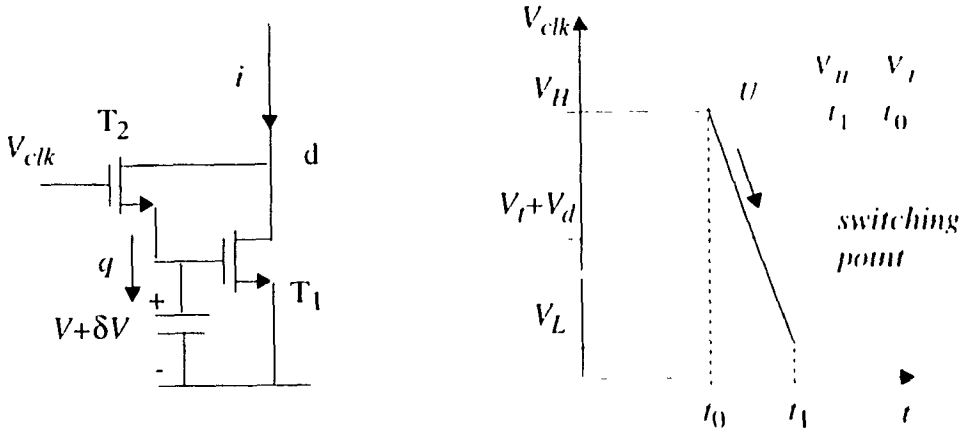


Fig. 2.13 An illustration of the effect of the finite output impedance of MOS transistors

2.5.2 Effect of Switch Charge Injection

When a MOS transistor switch is turned on, a quantity of charge is stored in its channel. When the switch turns off, the charge is injected into its surrounding circuit nodes. In addition to the charge from the intrinsic channel, the charge associated with the feedthrough effect of the gate overlap capacitance also adds to the charge injection effect [24]. The switch charge injection creates an error voltage in the gate of the memory transistor of the SI memory cell, as illustrated in Fig. 2.14. The analysis of switch charge injection is quite complicated because the value of the error voltage is the function of the switch turn-off rate, the aspect ratio of gate capacitance of T_1 and T_2, the switch transistor resistance, and the signal source resistance.



(a) Memory cell with switch charge injection (b) Clock waveform

Fig. 2.14 An illustration of the switch charge injection effect

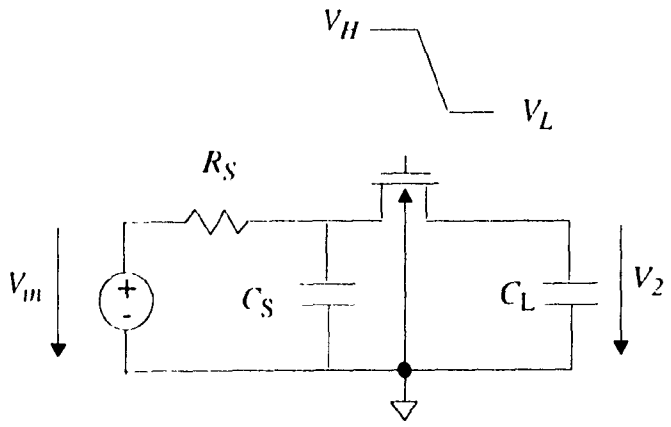


Fig. 2.15 Circuit for switch charge injection analysis

Fig. 2.15 shows a circuit which is used for switch charge injection analysis. Capacitance C_S is the lumped capacitance at the data-holding node. The resistance R_S is the output resistance of the signal source, and C_S is the lumped capacitance associated with signal source output capacitance. A numerical solution [24] shows that the charge injected into the data holding capacitor C_L depends on the ratio of the capacitors, C_S/C_L, and on the value of channel charge parameter B given by

$$B = (V_H - V_{11})\sqrt{\beta/(UC_1)}, \qquad \text{(EQ. 2.22)}$$

where $V_{11} = V_1 + V_{in}$ and U is the falling rate dV/dt of the switching clock.

1. When the switch turn-off time is much smaller than the time constant RsCs, the channel charge is shared between C_S and C_L. It is independent of the ratio C_S/C_L.

2. When the switch turn-off time is much larger than the time constant, the majority of

channel charge goes to the node with large capacitance. The charge splits according to the ratio of C_S/C_L.

3. When the switch turn-off time is comparable to the time constant, the charge sharing depends on the value of B.

4. When ratio $C_S/C_L = 1$, the channel charge is shared equally regardless of the value of B.

The switch charge injection error voltage causes an error in the output current of a SI memory cell. Fig. 2.16 illustrates the error current caused by the switch charge injection

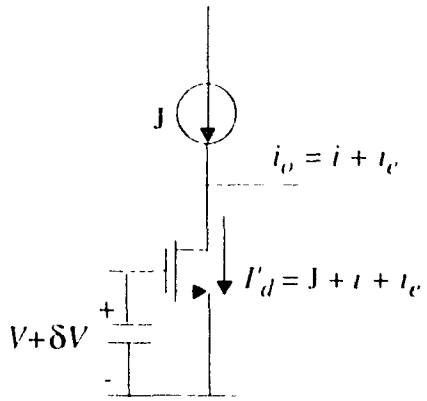


Fig. 2.16 An illustration of the error current caused by the switch charge injection

error voltage δV. The drain current I'_d contains three parts: a dc current J, an ideal signal current i, and an error current i_e. The dc current J is given by

$$J = \frac{\beta}{2}(V_{GS} - V_t)^2 \qquad \text{(EQ. 2.23)}$$

where $\beta = k_p(W/L)$ and V_t is the threshold voltage. In the ideal case, the drain current I_d is given by

$$I_d = \frac{\beta}{2}(V_{GS} + V_{gs} - V_t)^2 \qquad \text{(EQ. 2.24)}$$

By considering the switch charge injection error voltage δV, the drain current of the memory transistor is given by

$$I'_d = I + i + i_e = \frac{\beta}{2}(V_{GS} + V_{gs} - V_t + \delta V)^2 \qquad \text{(EQ. 2.25)}$$

By comparing the ideal and non-ideal cases, we have

$$\frac{I'_d}{I_d} = \left(\frac{V_{GS} + V_{gs} - V_t + \delta V}{V_{GS} + V_{gs} - V_t}\right)^2$$

$$= 1 + \frac{2\delta V}{V_{GS} + V_{gs} - V_t} + \frac{\delta V^2}{(V_{GS} + V_{gs} - V_t)^2} \qquad \text{(EQ. 2.26)}$$

From (EQ. 2.23) and (EQ. 2.24), we have

$$\frac{1}{V_{GS} + V_{gs} - V_t} = \frac{1}{V_{GS} - V_t}\sqrt{\frac{I}{I + i}} \qquad \text{(EQ. 2.27)}$$

using (EQ. 2.24) and (EQ. 2.27) in (EQ. 2.26) and letting $i + i_e = i_o$, we obtain the output current of the memory cell as

$$i_o = I + \frac{2\delta V I}{V_{GS} - V_t}\sqrt{\frac{I + i}{I}} + \frac{\beta}{2}\delta V^2 \qquad \text{(EQ. 2.28)}$$

By applying the binomial expansion, the output current given by (EQ. 2.30) can be written as

$$i_o = i_{odc} + i_{oac} \quad \text{(EQ. 2.29)}$$

where

$$i_{odc} = \frac{\beta}{2}\delta V^2 + \frac{2\delta VJ}{(V_{GS} - V_t)} \quad \text{(EQ. 2.30)}$$

and

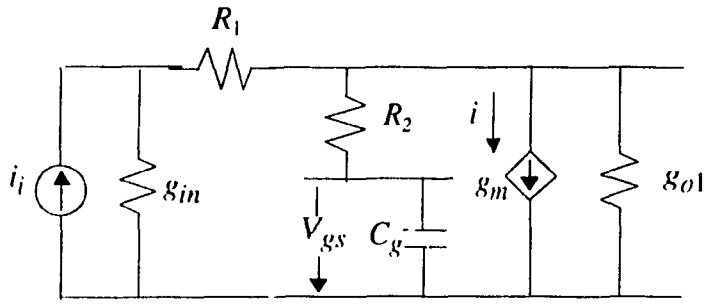
$$i_{oac} = i\left[1 + \frac{\delta V_t}{(V_{GS} - V_t)}\right] + \frac{2\delta VJ}{(V_{GS} - V_t)}\left[-\frac{1}{8}\left(\frac{i}{J}\right)^2 + \frac{1}{16}\left(\frac{i}{J}\right)^3 - \frac{5}{128}\left(\frac{i}{J}\right)^4 + \cdots\right] \quad \text{(EQ. 2.31)}$$

From the (EQ. 2.30) and (EQ. 2.31), it is seen that the switch charge injection error voltage produces a dc offset current, an ac current gain error and harmonic current distortion components. The dc offset error is determined by (EQ. 2.30), the ac gain error is determined by the first term of (EQ. 2.31) and the harmonic distortion is determined by the second term.

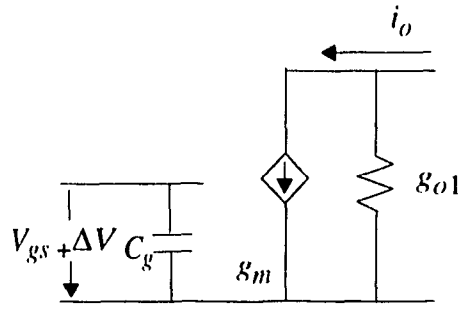
2.5.3 Settling Time Error

The operation of the SI memory cell involves charging of its gate capacitor to the gate voltage of a diode-connected memory transistor. If the charging is not completed during the sample period in which switches S_1 and S_2 are closed, a residual error voltage results. At the end of the sample period, the switches S_1 and S_2 are opened, the error voltage is stored in the gate capacitor and results an output current error as illustrated in Fig. 3.6, where g_m

is the signal source output conductance, g_o is the memory cell output conductance, and R_1 and R_2 are the closure resistance of the switches S_1 and S_2, respectively.



(a) Equivalent circuit of the simple SI memory cell with switches S_1 and S_2 closed, and S_3 opened



(b) Equivalent circuit of the simple SI memory cell with switches S_1 and S_2 opened, and S_3 closed

Fig. 2.17 An illustration of the memory cell settling time error

In a practical circuit, g_{in} and g_o are very small as compared with g_m. The resistors R_1 and R_2 can also be ignored. Therefore, the s-domain transfer function of the circuit is simply given by

$$\frac{i_o(s)}{i_{in}(s)} = \frac{1}{s\tau + 1} \qquad \text{(EQ. 2.32)}$$

where τ is the time constant and it is approximately equal to C_g / g_m. This time constant causes a non-zero settling time error described by

$$i = i_{in}(1 - e^{-1/\tau}) \qquad \text{(EQ. 2.33)}$$

For low-frequency applications, the effect of non-zero settling time error is not significant. However, for high-frequency applications, non-zero settling time error causes current distortion [25].

2.5.4 Process Mismatches Between the Current Mirror Transistors

When a scaled output current is required, a current mirror circuit is used. The process mismatch between current mirror transistors produces scaled output current errors. The mismatches between transistors could be in the threshold voltage V_t, the device aspect ratio W/L, the process gain factor K_p, or in the channel length modulation parameter λ. Most process mismatches result only in the current gain error in a SI memory cell, but threshold voltage mismatch causes dc error, current gain error, and harmonic distortion. The threshold voltage mismatch between the mirror transistors creates an error voltage ΔV_t as shown in Fig. 2.18. Thus, the effect of the ΔV_t is the same as that of the switch charge injection error voltage.

2.6 An Overview of the Existing SI Memory Cells

As discussed previously, the performance of the simple SI memory cell (the second-generation cell) is significantly affected due to the non-ideal characteristics of the MOS devices, such as channel length modulation, switch charge injection, non-zero closure resistor of MOS switches, and mismatch between the memory transistor and a scaling transistor if a scaled output is required. To overcome theses problems, several SI memory cell

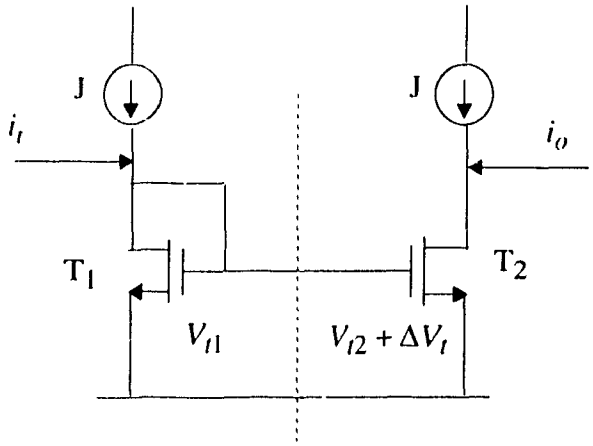


Fig. 2.18 An illustration of the effect of the threshold voltage mismatch

design techniques have been proposed. Two typical examples of these memory cells are given bellow and their performance are discussed.

2.6.1 Regulated Cascode SI Memory Cell

The effect of the channel length modulation can be reduced by using a cascode circuit which replaces the single memory transistor with a cascoded or regulated cascoded transistor. Fig. 2.19 shows a regulated cascode memory cell (RCMC) [17]. When the operation of T_1 is in its saturated region, an improvement of three orders of magnitude is possible in the output resistance of the cell as compared with the simple memory cell. Alternatively, T_1 can be operated in the unsaturated region, in which case an improvement of only two orders of magnitude in the output resistance is achieved. But, this gives a somewhat improved performance with respect to the switch charge injection error. However, this circuit still suffers from an unsatisfactory switch charge injection problem.

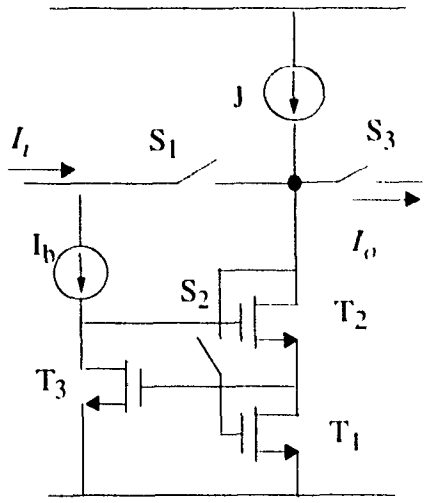


Fig. 2.19 A regulated cascode memory (RCMC) cell

2.6.2 Fully Differential SI Memory Cell

With the output resistance of the SI memory cells much improved by using the cascode or regulated cascode structure, the switch charge injection becomes the dominant performance limitation of the SI technique. There are several ways to reduce the effects of the switch charge injection [18], [19]. The most common methods are based on various matching mechanisms to achieve switch charge injection cancellation, such as the use of dummy switches or CMOS switches. Unfortunately, these methods are not very efficient in reducing the effect of switch charge injection and in some cases the effect may even worsen. In order to overcome the problem of the switch charge injection, an algorithmic SI memory cell [20] has been proposed. The algorithmic SI memory cell uses three basic cells and needs six clock cycles to achieve the cancellation of the charge injection. Although the algorithmic SI memory cell can reduce the effect of switch charge injection by as much as two orders of magnitude as compared with the simple memory cell, it increases power consumption by a factor of three and reduces the operating speed to one-sixth of the simple memory cell. To overcome these problems, a fully differential SI mem-

ory cell (FDMC) [14] has been proposed.

Fig. 2.20 shows the fully differential SI memory cell proposed in [14]. The fully differential circuit achieves the highest level of analog performance by the first-order cancellation of the switch charge injection offset, and by reducing the cross-talk from the neighboring digital circuits through the common-mode rejection and the power supply rejection of the amplifier. However, the complexity of the circuit is quite high because of the use of the common-mode feed back circuit, double switches, double wires, etc. In a filtering application, the coefficient transistors are also required to be doubled. This inevitably increases the chip area.

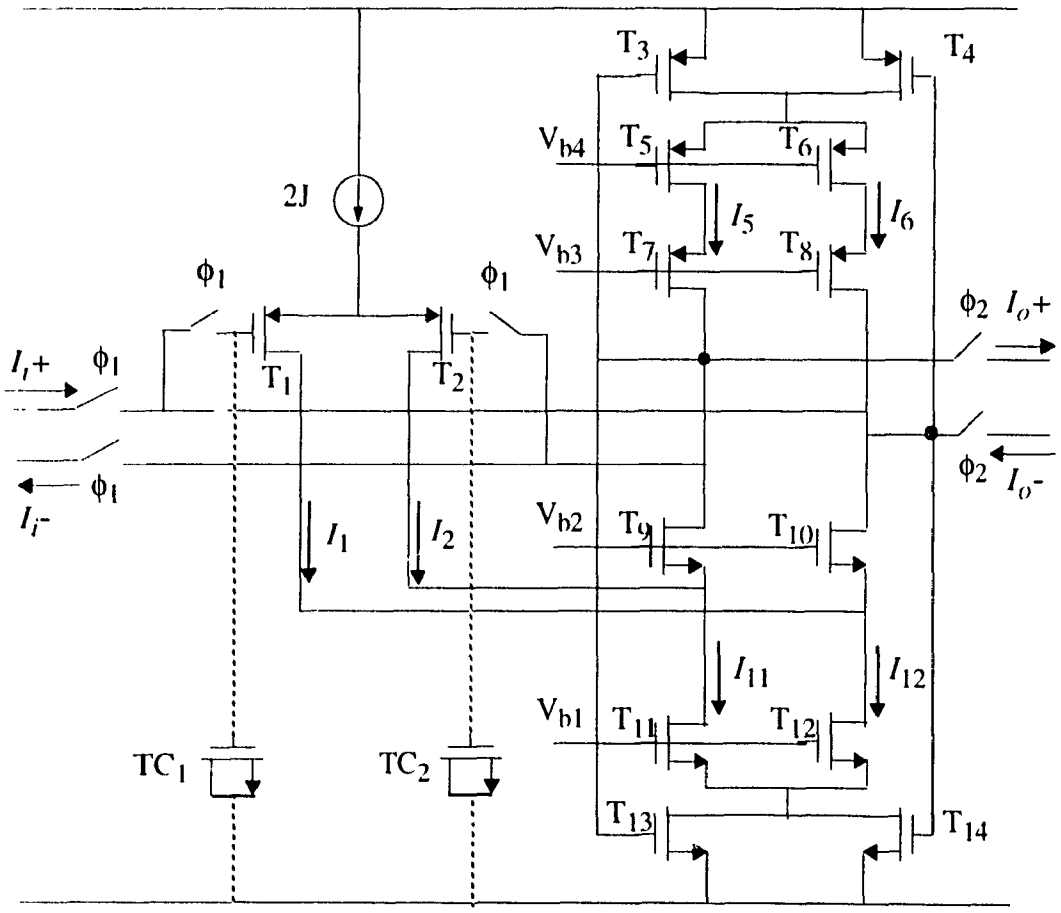


Fig. 2.20 A fully differential memory cell (FDMC) with common-mode feedback

2.7 Summary

In this chapter, the SI technique for analog signal processing has been reviewed. A SI circuit can sample and hold the current signals through the charge stored on the gate capacitor of a MOS transistor. Therefore, a SI circuit can perform the analog sample data processing without requiring linear capacitors. Since the signals in a SI circuit are presented as current, it is possible to work with low power supply voltages.

The effects of non-ideal characteristics of the MOS device in the simple memory cell have been analyzed. From the analysis, it is seen that the performance of the simple SI memory cell is strongly dependant on the characteristics of the MOS transistor used in the cell. Since a SI memory cell is the key building block of a SI circuit, the non-ideal MOS transistor can significantly affect the performance of the SI circuits. Because of the non-ideal characteristics of the MOS transistors, the simple SI memory cell produces unacceptably large analog errors that make the SI circuits less attractive than the SC circuits. To reduce the effects of non-ideal MOS devices, some SI memory cells with improved performance have been proposed. However, these cells still have the problems of low accuracy, low dynamic range and circuit complexity, etc.

Chapter 3

HIGH-PERFORMANCE SI MEMORY CELL DESIGN

Switched-current circuits are built around switched-current memory cells as building blocks. A switched-current memory cell is the most important functional unit, as its characteristics determine the performance of the overall switched-current circuit. As discussed in Chapter 2, the simple memory cell produces large analog errors due to the non-ideal characteristics of MOS devices used in the design of the cell. These analog errors significantly affect the performance of SI circuits. Therefore, design of a high-performance SI memory cell is essential to the SI circuit design. Although several SI memory cell design techniques have been proposed to provide improved performance [6],[17],[20],[21], there are still problems, such as switch charge injection, settling time error, parameter mismatching, circuit complexity and dynamic range, that must be dealt with to provide high-performance cells. In this chapter, we will propose a new high-performance SI memory cell design technique using a single-ended differential amplifier. A new differential SI memory cell is then introduced which uses a modified operational transconductance amplifier [1]. The new SI differential memory cell uses a differential amplifier as the input stage, where two matched switches are used for both of the inputs of the differential amplifier for data sampling. This cancels the clock feedthrough problem and reduces the channel charge injection. At the output stage of the SI memory cell, a complementary (PMOS and NMOS) regulated cascode circuit is used. The output resistance of the memory cell is, therefore,

expected to be increased. In order to further reduce the settling time without risking instability, a modified differential memory cell is proposed. The modified memory cell is also designed using a folded amplifier structure. The proposed cells are theoretically analyzed taking into consideration the non-ideal characteristics of the MOS devices. An HSPICE simulation is carried out for the current gain error, settling time, harmonic distortion, and power supply rejection ratio (PSRR). Finally, the cells are implemented using the standard 1.2 μ N-well CMOS process technology and tested in the laboratory.

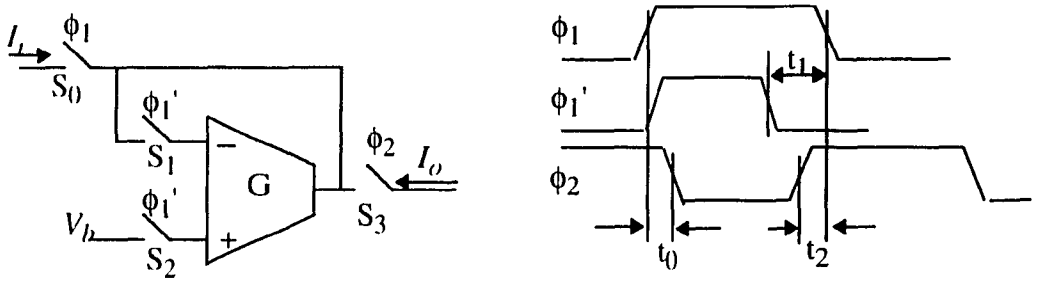
3.1 Proposed Differential SI Memory Cells

To overcome the problems associated with the non-ideal MOS transistor characteristics and to decrease the circuit complexity, a high-performance SI memory cell design technique using transconductance operational amplifier and single-ended folded cascode amplifier is proposed. In this section, we will first give design technique and then discuss the performance of designed cells based on the theoretical analysis and simulation results.

3.1.1 Principle of SI Memory Cell Design Using a Differential Amplifier

As discussed in the previous section, a fully differential SI memory cell achieves the first-order cancellation of switch charge injection offset because of the common mode rejection feature of the circuit. However, in the current mode, a single ended differential amplifier can achieve a performance similar to that the fully differential amplifier. Fig. 3.1 shows the block diagram of the SI memory cell using a single ended differential amplifier and the switching control waveform used for its operation. In this memory cell, two matched switches S_1 and S_2 are connected to the inputs of the differential amplifier. The operation of the circuit is as follows. When the clocks ϕ_1 and ϕ_1' are high, and ϕ_2 is low, the switches S_0, S_1 and S_2 are closed, and S_3 is opened, the memory cell is in the sample mode and it samples the input current I_i. When the clock ϕ_1' goes low, the switches S_1 and

S_2 are opened. Since the S_1 and S_2 are matched, the switch charge injection from S_1 and S_2 become a common-mode signal to the differential amplifier and it is rejected by the amplifier. Next, when the clock ϕ_1 goes low and ϕ_2 goes high, S_0 opens and S_3 closes, the memory cell is in the hold mode and it outputs the current $I_o = -I_i$. Note that the clocks ϕ_1 and ϕ_2 are designed to be overlapped for removing the current glitch. Thus, it is seen that the memory cell using the single-ended differential amplifier achieves the common-mode rejection in the current-mode operation as the one using fully differential amplifier.



(a) Block diagram (b) Switching control waveform

Fig. 3.1 A SI memory cell using differential amplifier

3.1.2 Differential Memory Cell Using Transconductance Amplifier (DMC-I)

Fig. 3.2 shows a schematic of a differential SI memory cell (DMC-I) built with the structure of an operational transconductance amplifier. A differential amplifier is used as the input stage and the output stage consists of complementary (PMOS and NMOS) regulated cascode circuits for increasing the output resistance.

Assume that N is the ratio of the transistors T_4 to T_8 or transistors T_6 to T_{12}. By the current mirror circuits, we have $I_5 = NI_3 = NI_1$ and $I_4 = NI_2$. When the input current signal I_i is zero, the currents $I_1 = I_2 = J$ and thus, $I_5 = NJ$ and $I_4 = NJ$. The operation of the cell is as follows. On phase ϕ_1, switches S_1, S_2 and S_3 close and S_4 opens, giving $I_5 = (NJ + I_i/2)$ and $I_4 = (NJ - I_i/2)$. Since $I_5 = NI_3 = NI_1$ and $I_4 = NI_2$, I_1 becomes $(J + I_i/2N)$ and I_2

becomes (J - I_i/2N). The current I_i charges the gate capacitor of T_1 to a voltage of V_{g1} establishing a differential input voltage $\Delta V = V_{g1} - V_{g2}$ that is required to maintain the currents I_4 = (NJ - I_i/2) and I_5 = (NJ + I_i/2). On phase ϕ_2, S_1, S_2 and S_3 open and S_4 closes. Since the differential voltage $\Delta V = V_{g1} - V_{g2}$ remains unchanged, the cell maintains I_4 = (NJ - I_i/2) and I_5 = (NJ + I_i/2), giving the output current $I_o = I_4 - I_5 = -I_i$.

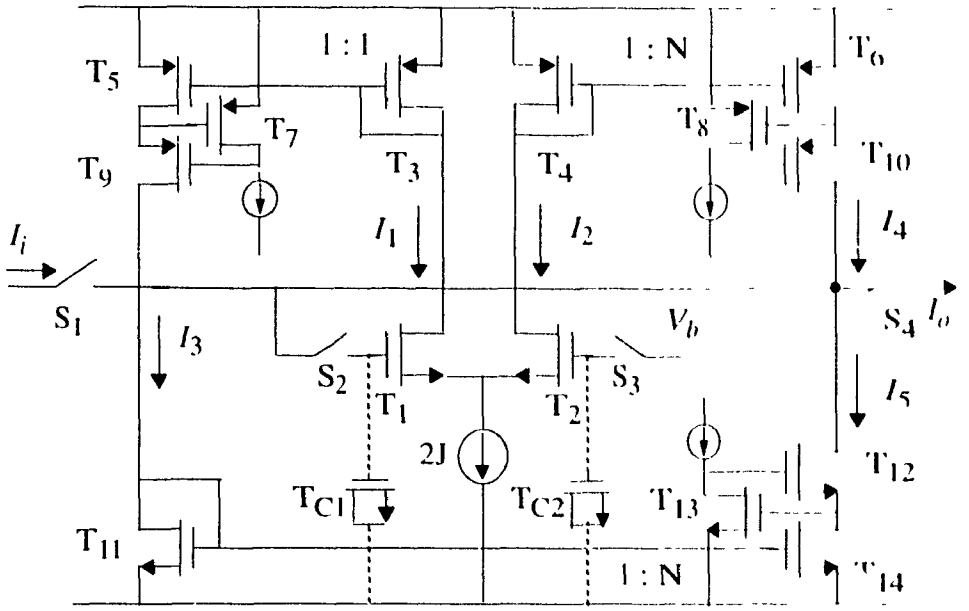


Fig. 3.2 A differential memory cell using transconductance amplifier structure (DMC-I)

Transistors T_{C1} and T_{C2} are two optional components connected as MOS capacitors. The use of T_{C1} and T_{C2} is to increase the gate capacitances of the memory transistors. In applications requiring very small analog errors, such as high-accuracy A/D and D/A converters, T_{C1} and T_{C2} can be used to reduce the switch charge injection effect.

3.1.3 Differential Memory Cell Using Folded Cascode Amplifier (DMC-II)

Fig. 3.2 gives the schematic of another differential memory cell (DMC-II) built with the structure of folded cascode amplifier. Similar to DMC-I, a differential MOS transistor

pair is used as the input circuit and the output circuit consists of a complementary (PMOS and NMOS) regulated cascode circuits connected in a folded cascode form.

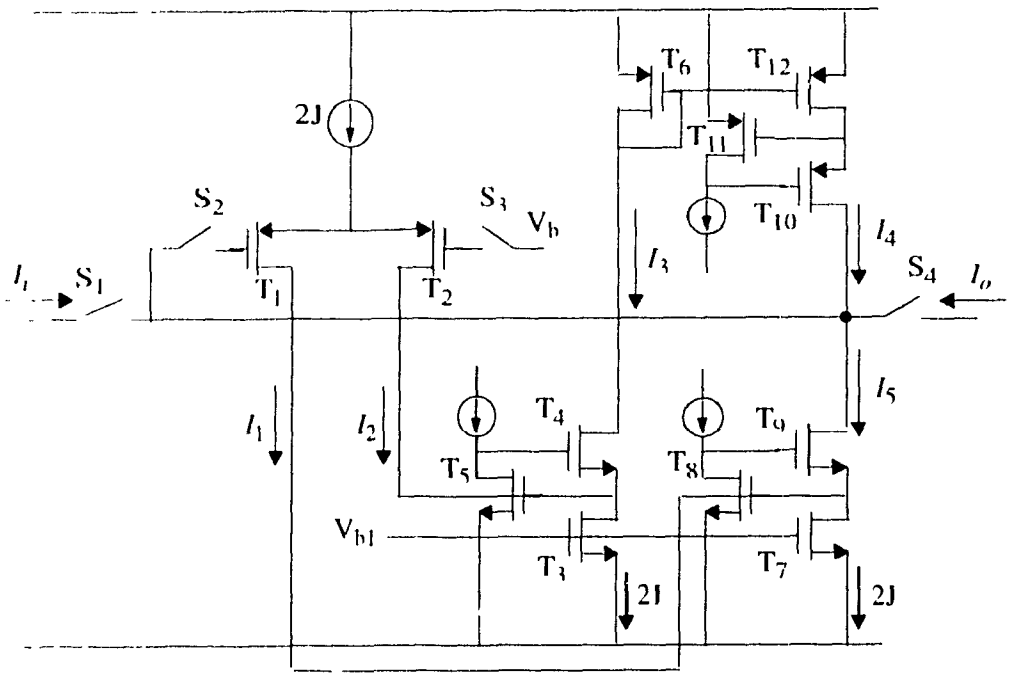


Fig. 3.3 A differential memory cell using folded cascode amplifier structure (DMC-II)

The operation of the cell is as follows. On phase ϕ_1, switches S_1, S_2 and S_3 close and S_4 opens, giving $I_4 = (J - I_i/2)$ and $I_5 = (J + I_i/2)$. Since the $I_4 = I_3$, I_1 becomes $(J - I_i/2)$ and I_2 becomes $(J + I_i/2)$. The current I_i charges the gate capacitor of T_1 to a voltage of V_{g1}, establishing a differential input voltage $\Delta V = V_{g1} - V_{g2}$ that is required to maintain the currents $I_4 = (J - I_i/2)$ and $I_5 = (J + I_i/2)$. On phase ϕ_2, S_1, S_2 and S_3 open and S_4 closes. Since the differential voltage $\Delta V = V_{g1} - V_{g2}$ remains unchanged, the cell maintains $I_4 = (J - I_i/2)$ and $I_5 = (J + I_i/2)$, giving the output current $I_o = -I_i$.

Just as in DMC-I, two capacitors, T_{C1} and T_{C2} can be used in DMC-II to increase the gate capacitors of the memory transistors and to reduce the effect of switch charge injection.

3.1.4 Analysis of the Proposed Differential Memory Cells

The performance of the differential memory cells is, in general, improved in reducing the effects of non-ideal characteristics of the MOS transistors. In this section, we will study the performance of the two proposed differential memory cells, DMC-I and DMC-II, through an analysis of the cells taking into consideration the non-ideal characteristics of the MOS transistors.

- *Channel Length Modulation*

Fig. 3.4 shows the regulated cascode circuit part of proposed memory cell and its equivalent circuit for the calculation of the output resistance of the memory cell.

From Fig. 3.4, we have

$$V_o \approx -g_{m12} r_{o12} \left[1 + g_{m11} r_{o11} \left(1 + g_{m10} r_{o10} \right) \right] V_{in} \qquad \text{(EQ 3.1)}$$

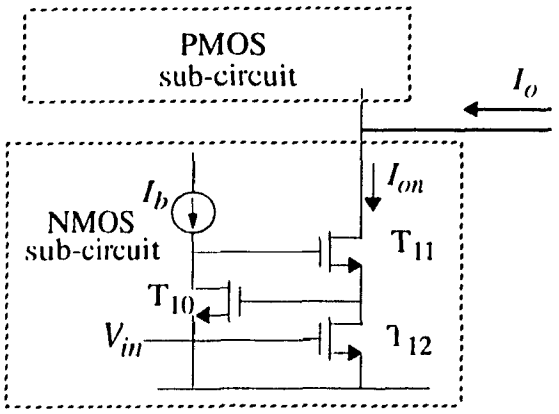
$$I_{on} \approx g_{m12} V_{in} \qquad \text{(EQ 3.2)}$$

By using (EQ 3.1) and (EQ 3.2), the output resistance of the regulated cascode circuit can be written as

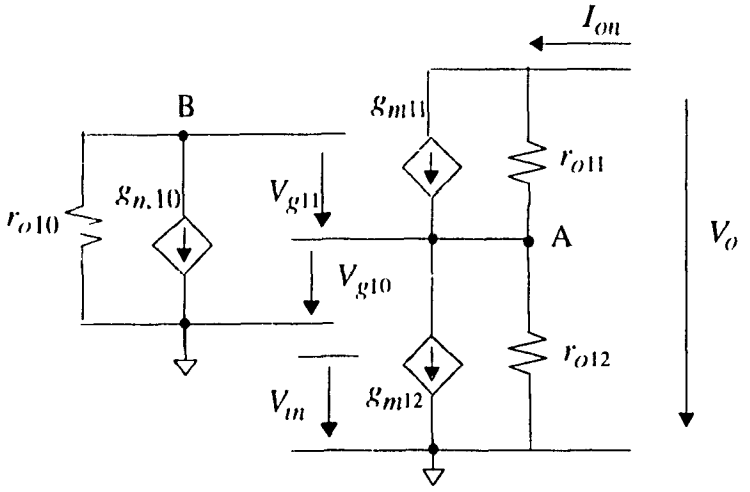
$$r_{on} = \frac{V_o}{I_{on}} \approx r_{o12} \left[1 + g_{m11} r_{o11} \left(1 + g_{m10} r_{o10} \right) \right] \qquad \text{(EQ 3.3)}$$

In practical circuits, $g_{m11} r_{O11} >> 1$, and $g_{m10} r_{O10} >> 1$. Assuming that $g_{m10} = g_{m11} = g_{m12} = g$ and $r_{O10} = r_{O11} = r_{O12} = r$, (EQ 3.3) can be simplified as

$$r_{on} \approx g^2 r^3 \qquad \text{(EQ 3.4)}$$



(a) The regulated cascode part of DMC-I or DMC-II



(b) The equivalent circuit of the regulated cascode circuit

Fig. 3.4 The circuit used for the analysis of the output resistance of the proposed cells

This equation gives the output resistance of the NMOS part of the cell,. In a similar manner, we can obtain the output resistance r_{op} of the PMOS part. The total output resistance of the cell is given by

$$r_o = \frac{r_{on} r_{op}}{r_{on} + r_{op}} \approx \frac{g^2 r^3}{2}, \qquad \text{(EQ 3.5)}$$

where it has been assumed that $r_{on} = r_{op} = r$.

Thus, by the use of the regulated cascode circuits as the output stage of the proposed memory cells, the output resistance of the cell is improved by three orders of magnitude as compared with that of the simple memory cell.

Another feature of the proposed memory cells is that despite an improvement of the three orders of magnitude in the output resistance, the output voltage swing remains $2V_{GS} - V_t$. This feature is very useful for a memory cell working with low supply voltages.

- *Switch Charge Injection Cancellation*

The differential memory cell shown in Fig. 3.1 uses a differential amplifier as the input stage and two matched switches to sample the differential signal. The clock feedthrough problem introduces the same error voltages on the two input gate capacitors giving a common signal error in the sampled value. Although the differential input voltage introduces the difference of two channel charges into the two matched switches, this error is less than what it is in a non-differential memory cell. The proposed memory cells are now analyzed for the effect of switch charge injection using the block diagram shown in Fig. 3.1 (a). Fig. 3.5 depicts an equivalent circuit for determining the charge injection. The channel charge from the switches S_1 and S_2 create error voltages δV_{d1} and δV_{d2}, respectively, and we have $\delta V = \delta V_{d1} - \delta V_{d2}$. From (EQ. 2.22), the channel charge parameters for the two switches are given as

$$B_1 = (V_H - V_{TE1}) \sqrt{\beta_1 / (UC_1)} \qquad \text{(EQ 3.6)}$$

$$B_2 = (V_H - V_{TE2}) \sqrt{\beta_2 / (UC_2)} \qquad \text{(EQ 3.7)}$$

Assuming that the switches S_1 and S_2 are matched, we have $\beta_1 = \beta_2 = \beta$ and $C_1 = C_2 = C$. The only difference between B_1 and B_2 is that $V_{TE1} = V_t + V_{in1}$ and $V_{TE2} = V_t + V_{in2}$.

Therefore, in general, the channel charge injection will introduce the same error voltage on the capacitors C_1 and C_2, thus, giving no differential error in the sampled values. Although the differential input voltage $V_{in} = V_{in1} - V_{in2}$ introduces a difference of the channel charge in the two matched switches, the value of V_{in} is very small in the differential SI memory cell, since the gain of the memory cell is large. Thus, the effect of switch charge injection is very small, since it depends on the value of V_{in}.

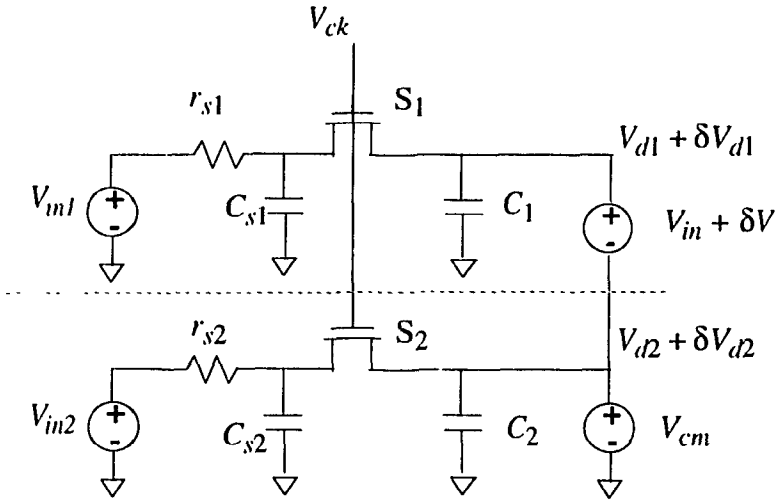


Fig. 3.5 An equivalent circuit for determining the effects of switch charge injection in the proposed memory cell

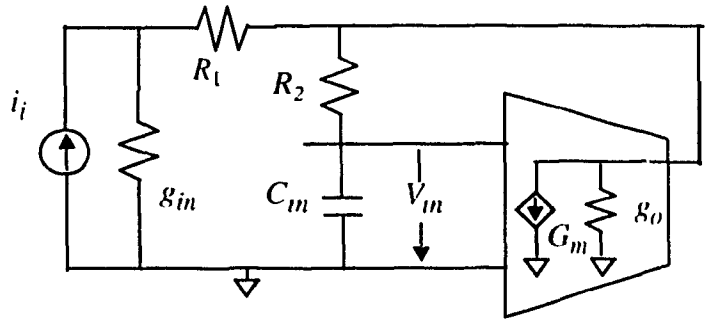
- *Input and Output Current Dynamic Range*

Usually, the maximum input and output current dynamic range of memory cells are determined by the bias current of the memory transistors. However, the memory cell DMC-I can achieve a large dynamic range by increasing the value of the ratio N. The total bias current of DMC-I is $I_b = (3 + N)J$. For large N, the maximum dynamic range of the current I_i or I_o is about $\pm$ 2NJ. Thus, the maximum dynamic range of the cell is approximately equal to the 4 times the base current. This is compared with maximum dynamic range of $2I_b$ for the simple cell and the RCMC, and I_b for the FDMC.

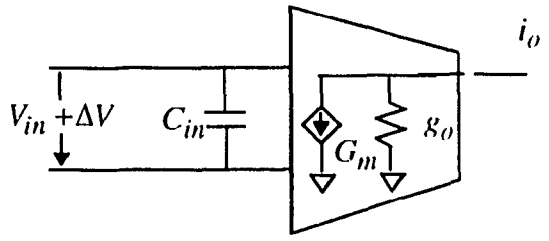
The maximum dynamic range of output current I_o of DMC-II is about $\pm 2J$. The total bias current I_b of the DMC-II is about 4J. Therefore, the maximum dynamic range of DMC-II is equal to the base current, which is the same as achieved with the FDMC.

- *Settling Time*

The analysis of the settling time error is the same as that of the simple memory cell, when a single-input, single-output equivalent of the differential memory cell is used. Here, as shown in the Fig. 3.6, the time constant of the differential memory cell is $\tau = C_g / G_m$,



(a) An equivalent circuit of the proposed memory cells with switches S_1 and S_2 closed, and S_3 opened



(b) An equivalent circuit of the proposed memory cells with switches S_1 and S_2 opened, and S_3 closed

Fig. 3.6 The circuit used for analysis of the settling time of the proposed memory cells

where G_m is the gain of the memory cell and C_g is the gate capacitor. If the gain of the cell G_m is large, the settling time can be reduced. The gain of the differential memory cell DMC-I could be very large by increasing the ratios of aspect ratios W/L of the transistors (T_8, T_4) and (T_{12}, T_{16}). However, a large gain would cause a stability problem, since DMC-I is built by a two-stage operational amplifier structure. Compensation circuit may be required for fast settling time applications. This can be easily accomplished by attaching a small shunt capacitor to the output of the cell [1]. The value of the compensation capacitor C can be determined as

$$C = \frac{g_{m1}(g_{m12} + g_{m8})}{2g_{m4}GB} , \qquad \text{(EQ 3.8)}$$

where GB is the gain-bandwidth product of the amplifier.

3.1.5 Simulation Results of the Proposed Memory Cells

To verify the performance of the proposed differential memory cells, HSPICE simulation tool is used with typical 1.2 μ CMOS process parameters. The simulation results of DMC-I (shown in Fig. 3.2) and DMC-II (shown in Fig. 3.3) are compared with those of the simple memory cell (shown in Fig. 2.2), the RCMC (shown in Fig. 2.19), and the FDMC (shown in Fig. 2.20).

- *Current Transmission Error*

In this experimentation, two identical memory cells are connected as shown in Fig. 3.7 The error current detected includes the switch charge injection and channel length modulation. To avoid the settling time error, the sampling frequency is set to only 100 KHz. Since the effect of the switch charge injection can be reduced by using large gate capacitors of the memory transistors, to compare the simulation results with other of memory cells, the size of the memory transistors of the all the cells are set to be of comparable

values. Table 3.1 lists the size of the transistors of the memory cells. The transistor ratio parameter N in DMC-I is set to a value of 8.

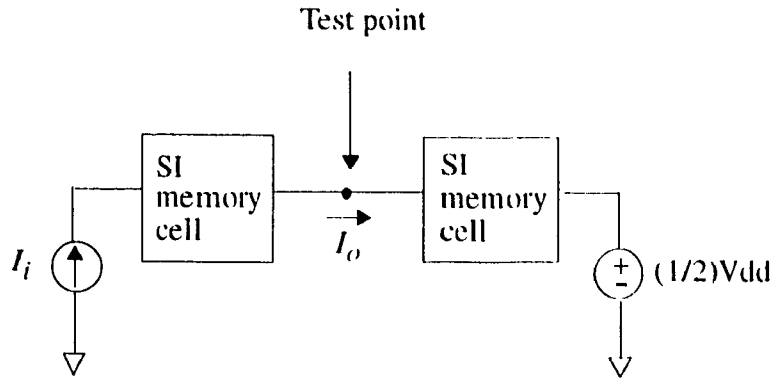


Fig. 3.7 Simulation circuit for the measurement of the current transmission error

Fig. 3.8 shows the simulation results of the current transmission error. It can be seen that DMC-I has the smallest current transmission error, and the current transmission error of DMC-II is very close to that of DMC-I. When the signal current is less than 1 μA, the errors (offset error) of DMC-I and DMC-II are a little larger than that of the fully differential cell. The offset error can be reduced by increasing the gate capacitor (the sizes of T_{C1} and T_{C2}).

Table 3.1 List of transistor sizes and base currents of various memory cells

Memory cell	Size of memory transistor (W/L)	Size of capacitor transistor (W/L)	Bias current I
Simple	40 μm / 20 μm	-	100 μA
RCMC	40 μm / 20 μm	-	100 μA
FDMC	100 μm / 2 μm	20 μm / 10 μm	100 μA
DMC-I	40 μm / 2 μm	20 μm / 10 μm	20 μA
DMC-II	100 μm / 2 μm	20 μm / 10 μm	100 μA

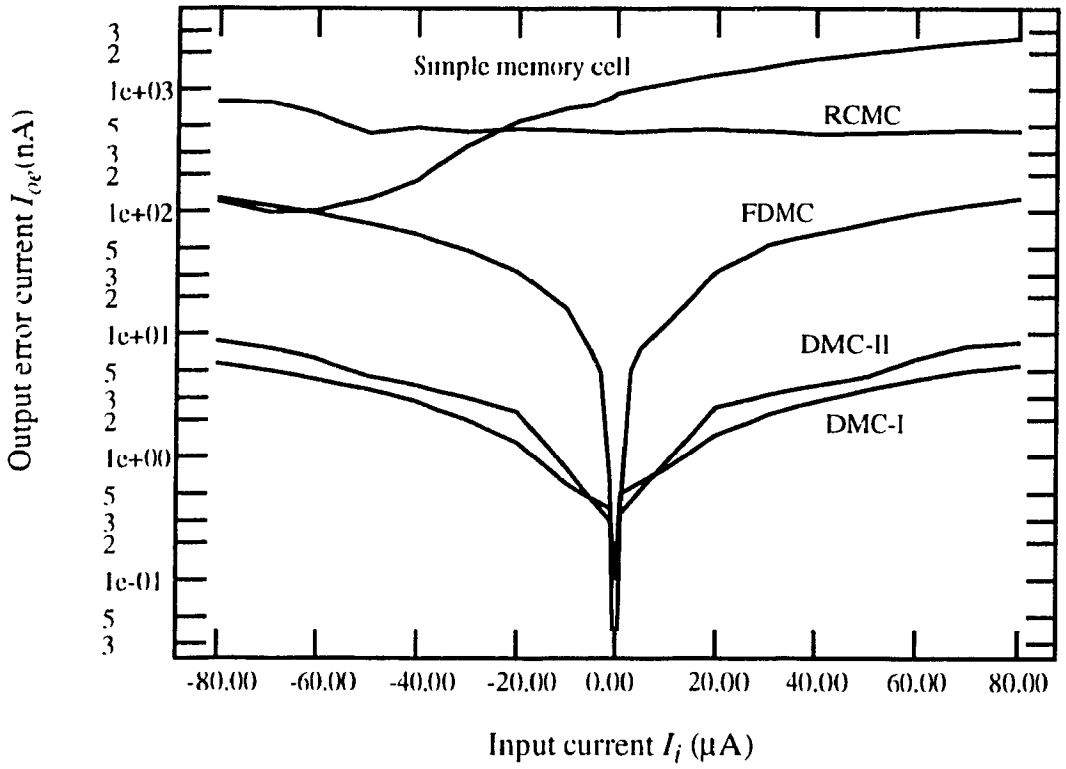


Fig. 3.8 Current transmission errors of various SI memory cells

- *Power Supply Rejection Ratio (PSRR)*

In order to examine the PSRR of the proposed memory cells, HSPICE simulation is used with a distortion signal V_{dp} (the peak-peak voltage of V_{dp} is 1 V) added to the power supply of the memory cells. Fig. 3.10 and Fig. 3.11 show the simulation results in which the PSRR of DMC-I is compared to that of the FDMC. DMC-I has the same level of PSRR in the voltage mode as that of the FDMC in the practical range of 0 to 1 KHz distortion of the power supply voltage. In the current mode, the differential memory cell has better PSRR value than the fully differential cell when frequency is less than 1 MHz. From Fig. 3.10, we can also see that when the frequency of distortion signal is higher than 1 KHz, the PSRR of DMC-I is getting worse than FDMC. However, for the frequency higher than 100 KHz, the

output voltage of DMC-I becomes almost constant (about 25 mV) and there is a valley at the frequency of 20 MHz. This is because of the use of regulated cascode circuit as the output stage of DMC-I.

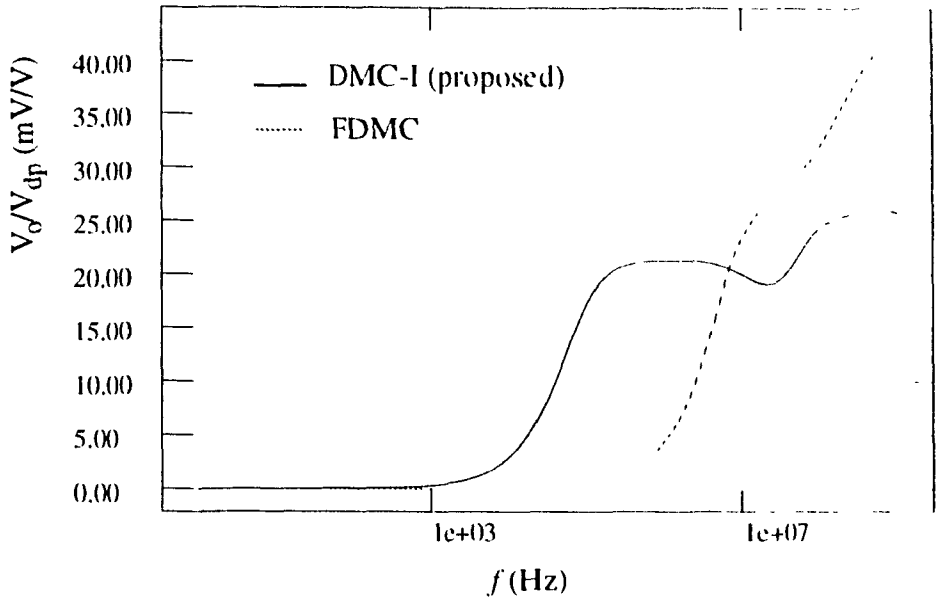


Fig. 3.9 Simulation results of I/PSRR of memory cells when voltage is the output

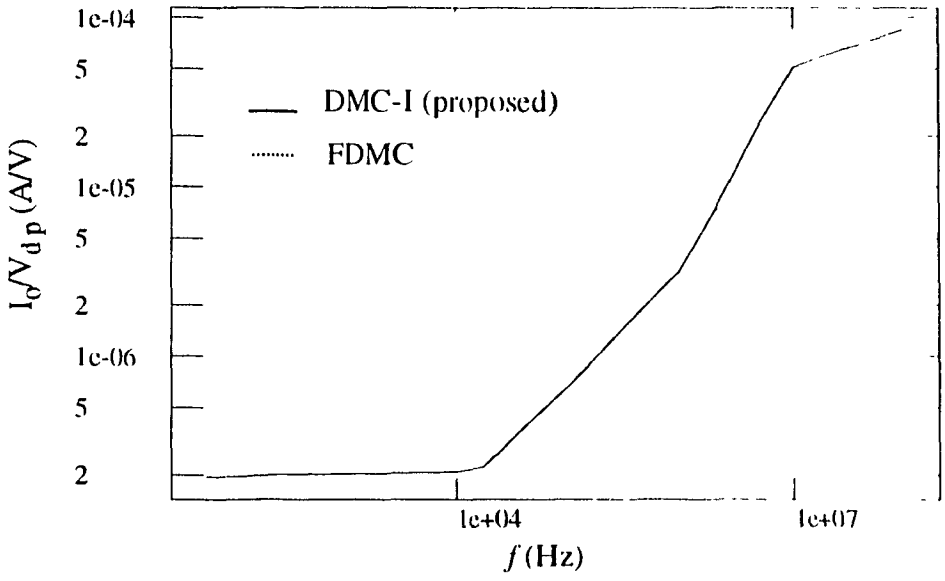


Fig. 3.10 Simulation results of I/PSRR of memory cells when the current is the output

- *Settling Time*

As discussed in Section 3.1.4, a small settling time can be achieved by increasing the gain of the memory cell, however, a large gain causes a stability problem. To investigate the relationship between the gain of the memory cell, settling time and stability, we simulate DMC-I with various sizes of the memory transistors and gate capacitors. Table 3.2 gives the sizes of the memory transistors and capacitors where value of the ratio N is 10, and J is 20 μA. Fig. 3.11 shows the simulation results. It is seen that when the gain of the

Table 3.2 Sizes of memory transistors and gate capacitors

Transistors	Curve (1)	Curve (2)	Curve (3)
W/L (μm) of T_1, T_2	10/2	10/2	10/10
W/L (μm) of T_{C1}, T_{C2}	-	10/10	-
Settling time t_r (μs)	0.14	0.4	0.17

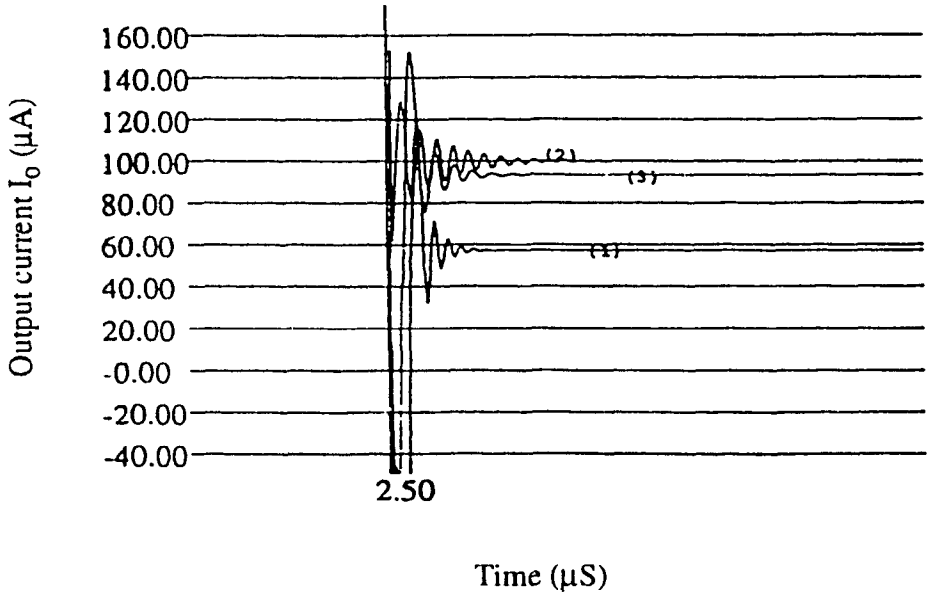


Fig. 3.11 Settling time of the DMC-I

cell is small, the cell has greater settling time. On the other hand, a larger gain reduces the settling time, but this may lead to a stability problem. The larger gate capacitor would increase the settling time significantly but improve the accuracy.

Fig. 3.12 shows the simulation results of the settling time of the DMC-II. Since the DMC-II is built with a single-stage amplifier structure, it is not prone to the stability problem. The settling time ($t_r \leq 70$ ns) is also much shorter than that of DMC-I. Therefore, DMC-II is very suitable for high-speed applications.

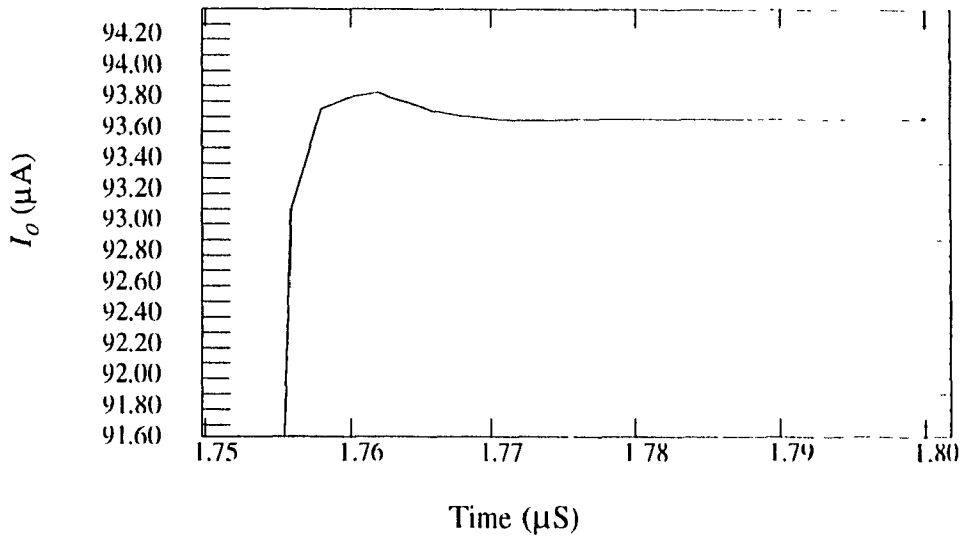


Fig. 3.12 Settling time of the DMC-II

- *Unit Gain Error and Total Harmonic Distortion (THD)*

To evaluate the harmonic distortion of the proposed memory cell DMC-I, its dynamic behavior is simulated using HSPICE and then the simulated results are analyzed by using the FFT. Fig. 3.13 depicts the dynamic behavior of the output current which is shown as sample and hold pulses. Fig. 3.16 gives the analysis results. It is clear that the maximum harmonic distortion is less than -71.6 db and signal-to-noise ratio is larger than 71 db at the input frequency of 100 KHz.

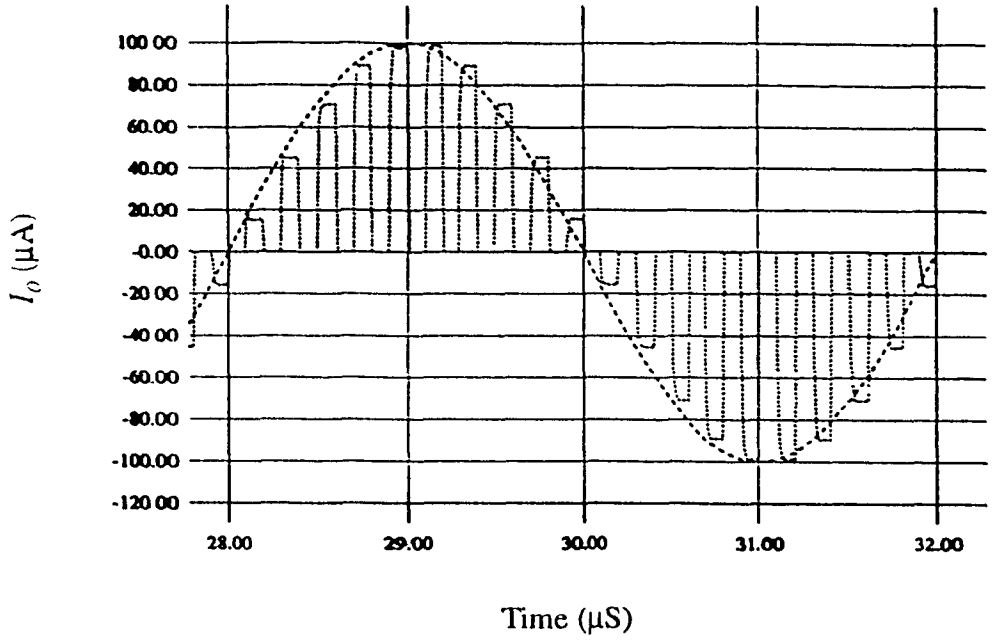


Fig. 3.13 Dynamic behavior of DMC-I

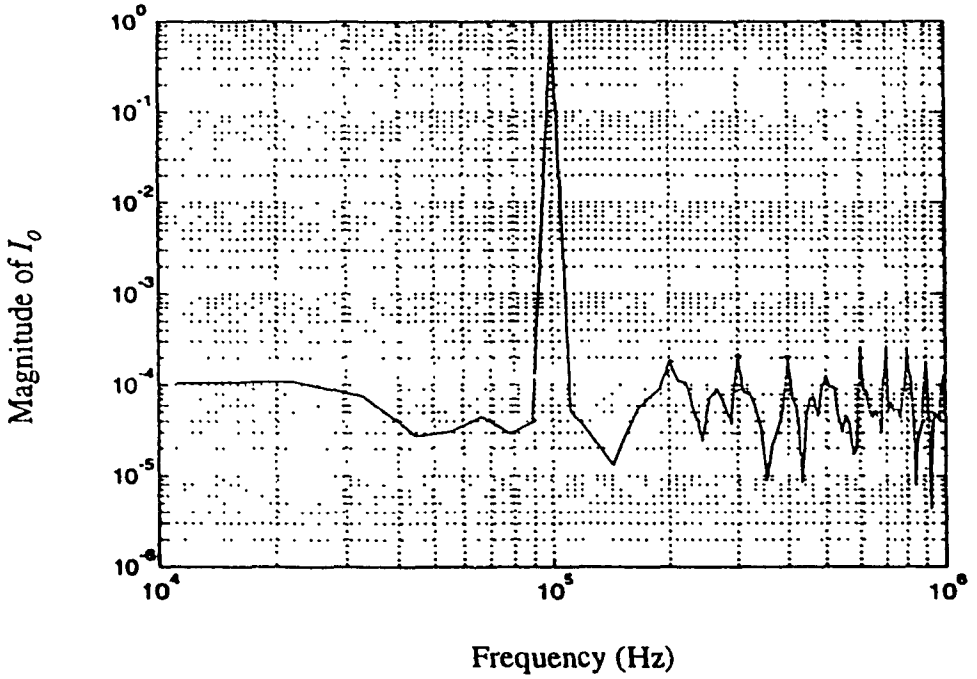


Fig. 3.14 Magnitude frequency spectrum of the DMC-I

3.2 Prototype Chip Design and Testing

In this section, both the proposed memory cells are designed and implemented using the standard 1.2 μ N-well CMOS process technology. The DMC-I is designed in two different sizes for inve tigating the current gain effect. One of them is designed with a smaller open-loop gain and other with a larger gain. The DMC-II is designed only with one open-loop gain. The three cells are referred to as Cell #1, Cell #2, and Cell #3, respectively. The three chips were tested in the laboratory and the results are discussed in this section.

3.2.1 Chip Layout Design

Fig. 3.15 to Fig. 3.17 show the layouts of the designed differential memory cells. Table 3.3 lists the sizes of the memory transistors and capacitors of the cells.

Table 3.3 The sizes of memory transistors and capacitors of the designed cells

Transistors	Cell #1	Cell #2	Cell #3
W/L (μm) of T_1 and T_2	40/2	60/2	432/1.2
W/L (μm) of T_{C1} and T_{C2}	23.1/27	23.1/27	34/21.5

Since DMC-I may have stability problem, the layouts of Cell #1 and Cell #2 contain the frequency compensation circuit for the frequency compensation. The compensation circuit consists of a MOS capacitor and a small size transistor used as a resistor and it is connected between the cell output and the ground. The size of the capacitor is about 27 X 35 μm^2 (C = 0.06 pF). The size of the resistor transistor is 3.9 μm/ 39 μm. The capacitor is connected from the output of the memory cell to the resistor and the resistor's other terminal is connected to the ground.

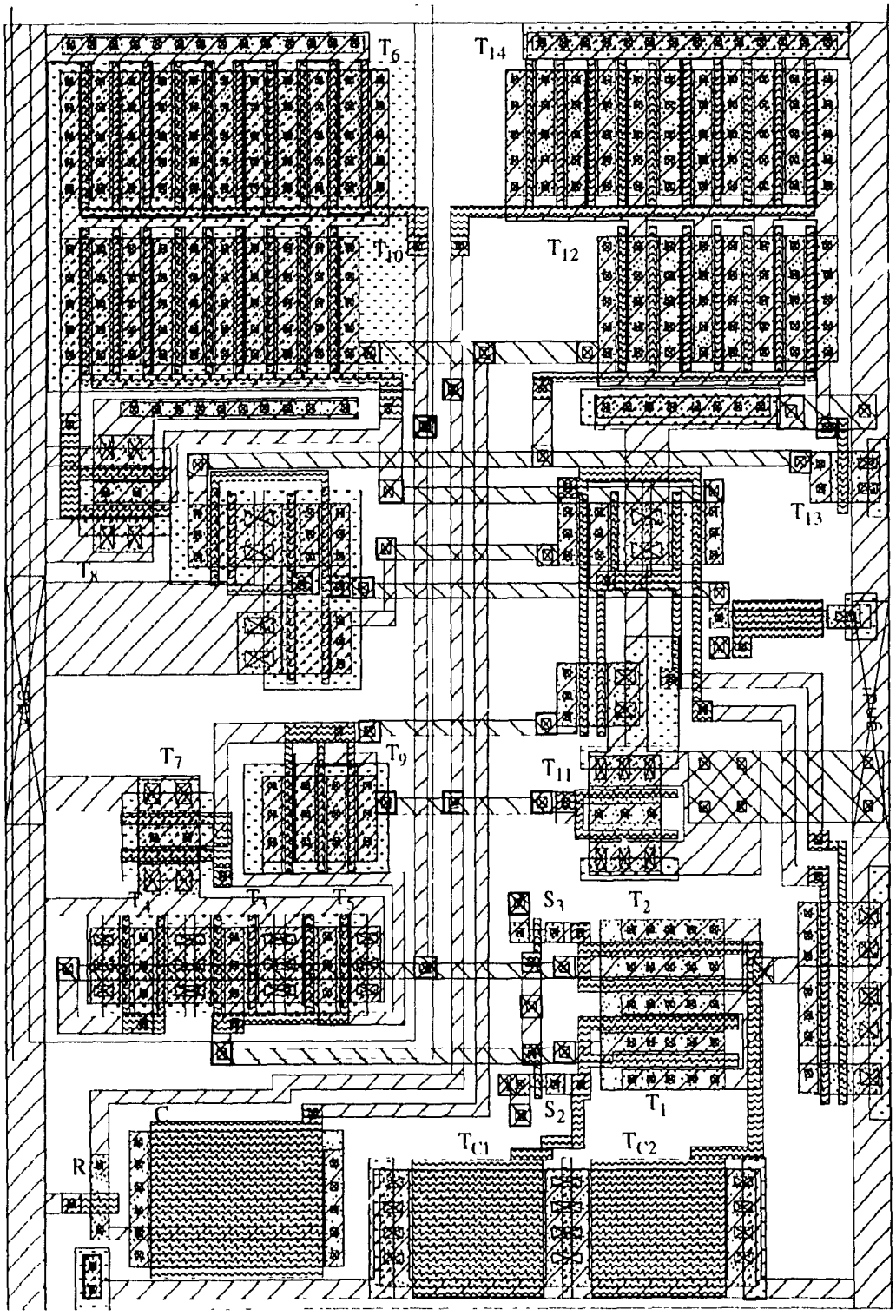


Fig. 3.15 Layout of Cell #1

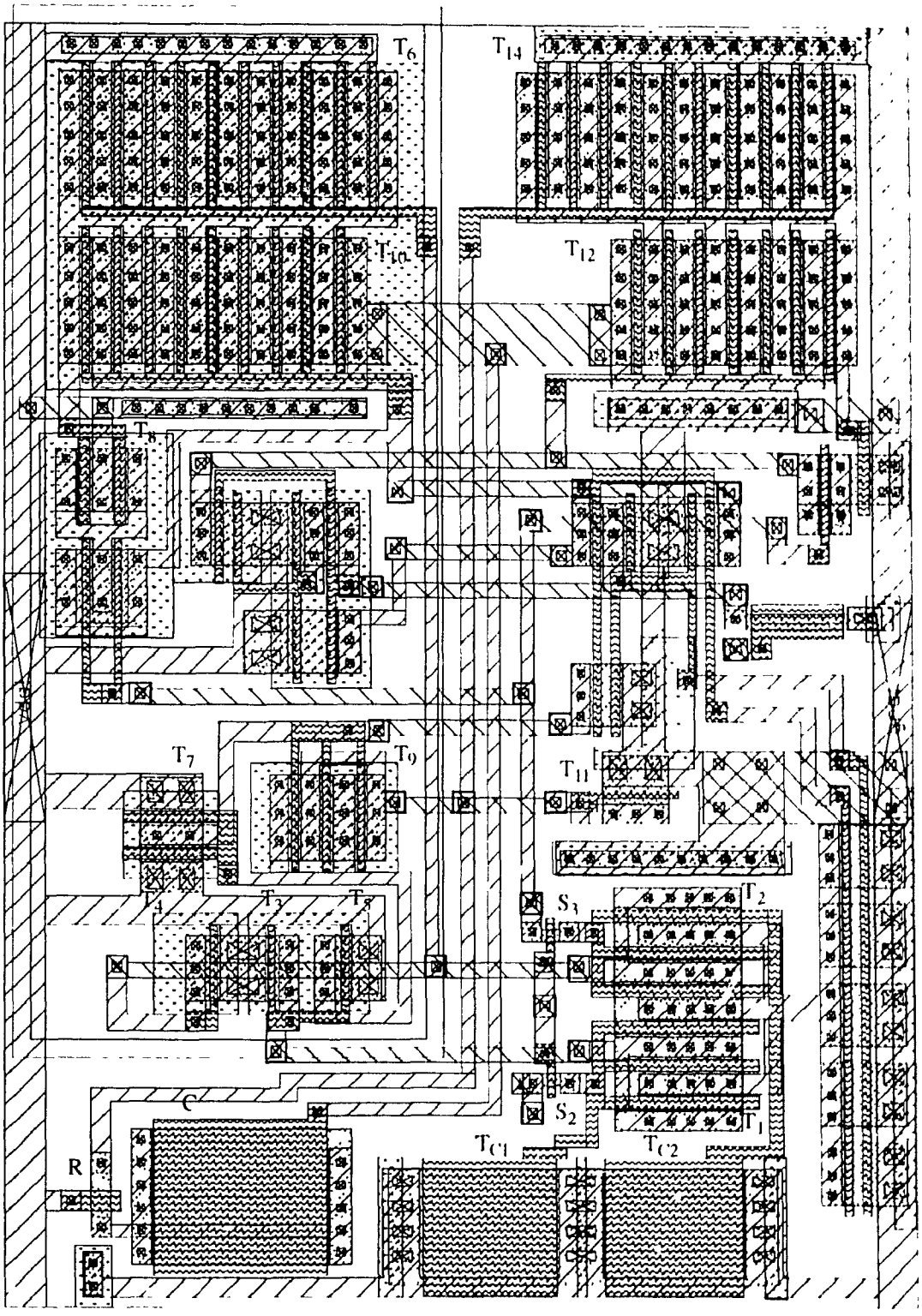


Fig. 3.16 Layout of Cell #2

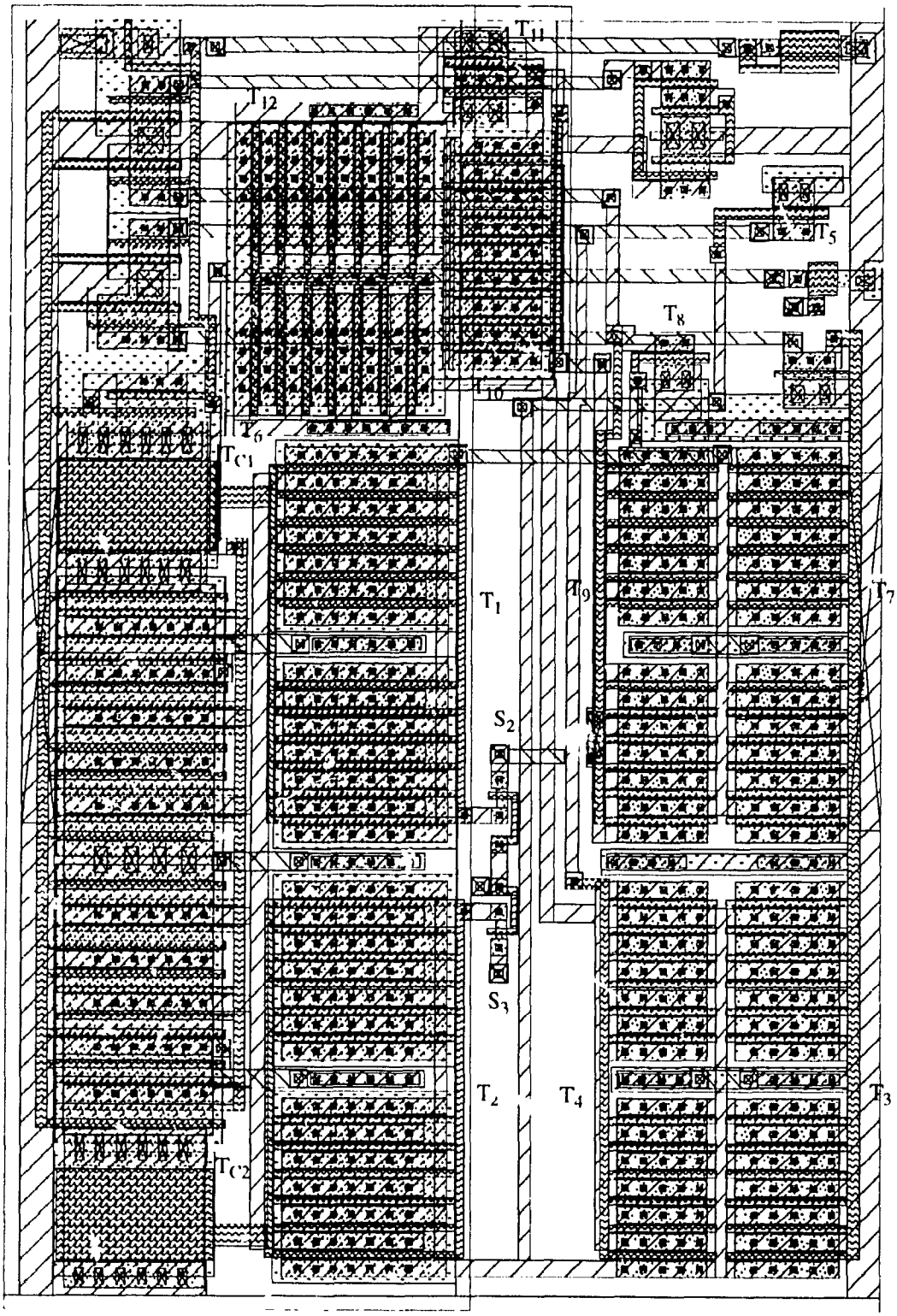


Fig. 3.17 Layout of Cell #3

3.2.2 Test Results of the Prototype Chips

The three differential memory cells were tested in the laboratory. The performance of the cells were evaluated in terms of the dynamic behavior, unit gain error, THD, settling time, and PSRR. These parameters were tested separately with 5 V and 3.3 V power supplies. Fig. 3.18 shows the circuit for testing the cells. The input current is obtained by connecting a resistor between signal generator and the cell input. A BiCMOS operational amplifier is used as a current-voltage converter for testing the output currents.

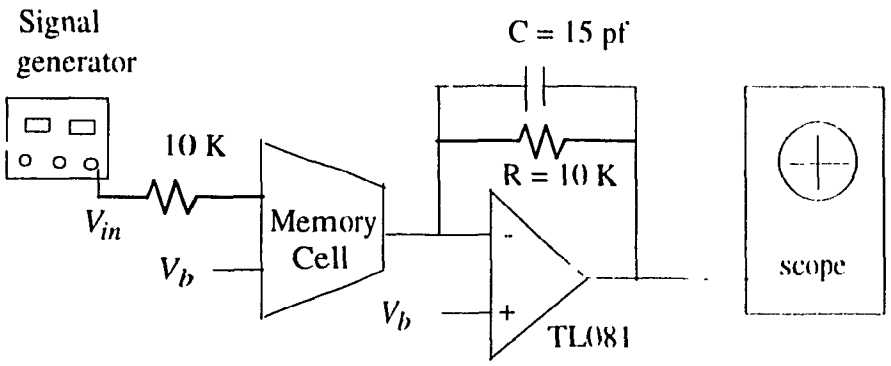


Fig. 3.18 The memory cell testing circuit

- *Dynamic Behavior*

The test results show that the dynamic behavior of all the memory cells are the same. Fig. 3.19 shows the behavior of cell #1. In this testing, the memory cell works as a sample and hold circuit for a sinusoid input signal. The sampling frequency (f_s) is 100 KHz, V_{dd} = 5 V, V_b = 2.5 V, and the input signal frequency (f_i) is about 10 KHz with peak-to-peak voltage (V_{p-p}) of 1 V. The dynamic behavior remains the same when the power supply voltage is changed to 3.3 V.

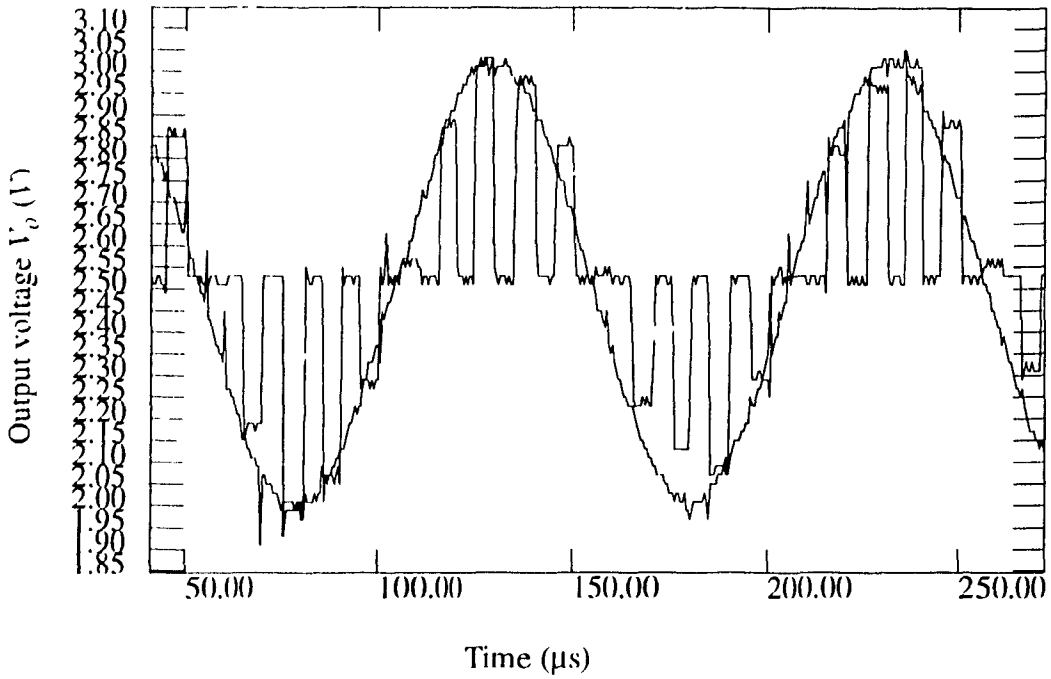


Fig. 3.19 Dynamic behavior of Cell #1 with f_i =10 KHz and f_s = 100 KHz

- *Gain Error and THD*

The current gain and the THD of Cell #1 and Cell #2 were tested with the power supply voltage V_{dd} = 5 V, and Cell #3 with the power supply V_{dd}= 4.6 V (Cell #3 has the best performance when V_{dd} is 4.6 V). The sampling frequency f_s = 100 KHz and input signal frequency f_i = 5 - 10 KHz. Fig. 3.20 to Fig. 3.22 show the test results. An ideal SI memory cell should have a current gain of 1. From the unit gain error, we can evaluate the current transmission error, and therefore, the effects of the switch charge injection and the channel length modulation. The total harmonic distortion is a more important parameter than the gain error in many signal processing applications. From Fig. 3.20 to Fig. 3.22, we clearly see that the second and third harmonic distortions are small. However, by examining the frequency spectrum of the input signal from the signal generator (see Fig. 3.23), it is seen that the second and third harmonic distortions are also partially due to the imperfection of

the input signal generator. The SI memory cells create harmonic distortions less than 0.2%. Table 3.4 lists all the measured results (since the second and third harmonic distortions are the largest distortions, the THD values given in Table 3.4 are calculated from the second and third harmonics). From the test results, we see that Cell #3 has the best performance in the terms of gain error and harmonic distortions, and Cell #2 is the worst.

Table 3.4 Test results of the gain error and THD of the prototype chips with V_{dd} = 5 V and f_s = 100 KHz

Parameters	Cell #1	Cell #2	Cell #3
Power supply V_{dd} (V)	5	5	4.6
Current gain error (db)	0.4	-0.8	-0.1
THD (db)	- 55.2	- 31.4	-61.8
PSRR (db) (V_{dp} = 1 V)	-59.4	-51.1	67.3

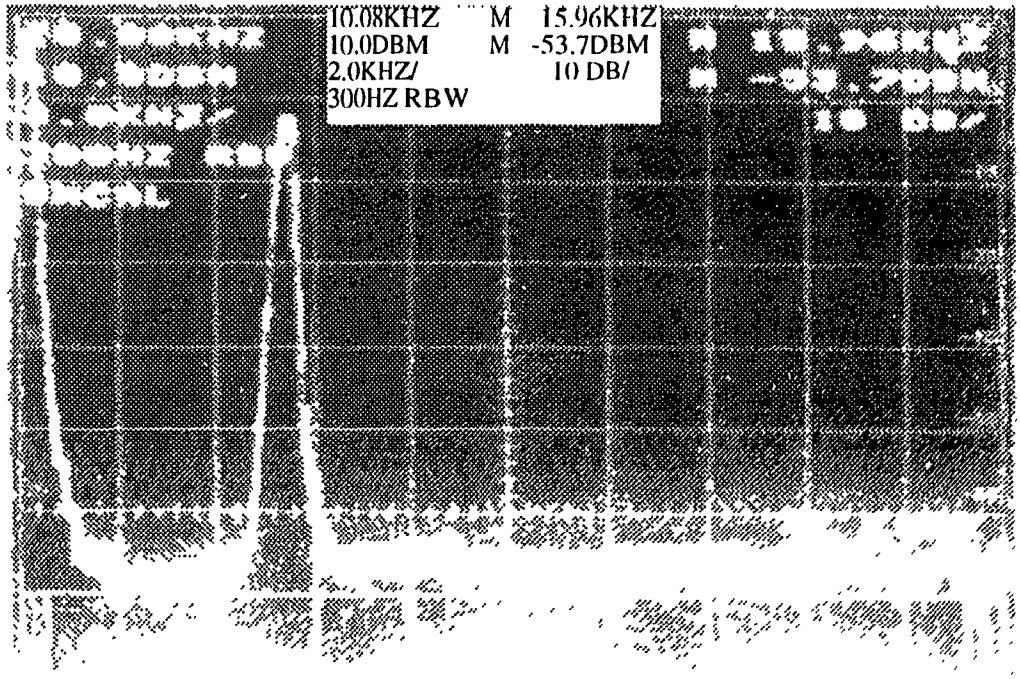


Fig. 3.20 Magnitude frequency spectrum of Cell #1 (V_{dd} = 5 V and f_s = 100 KHz)

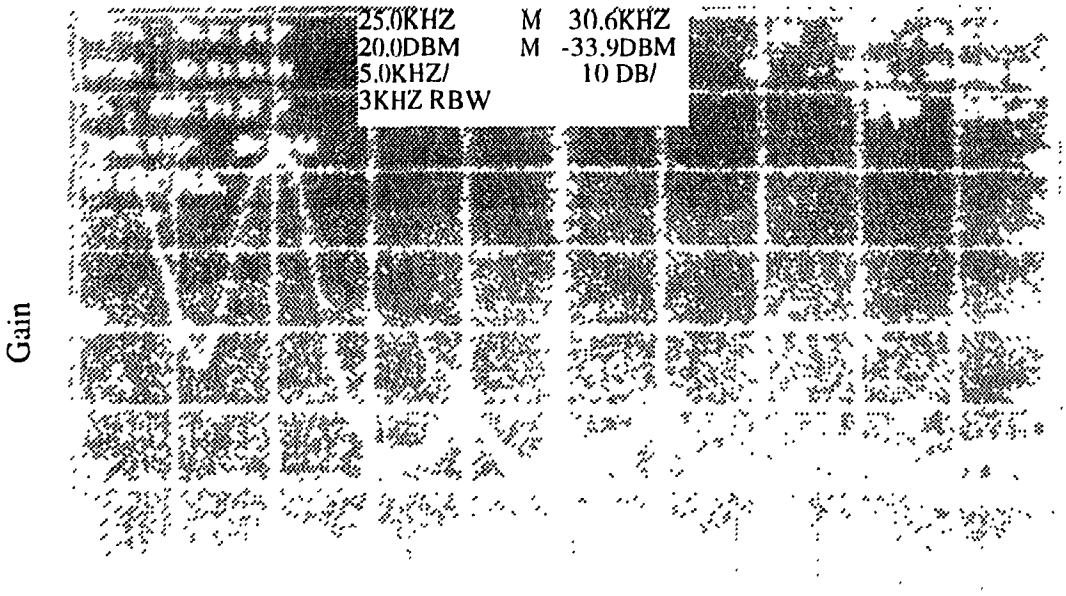


Fig. 3.21 Magnitude frequency spectrum of Cell #2 (V_{dd} = 5 V and f_s = 100 KHz)

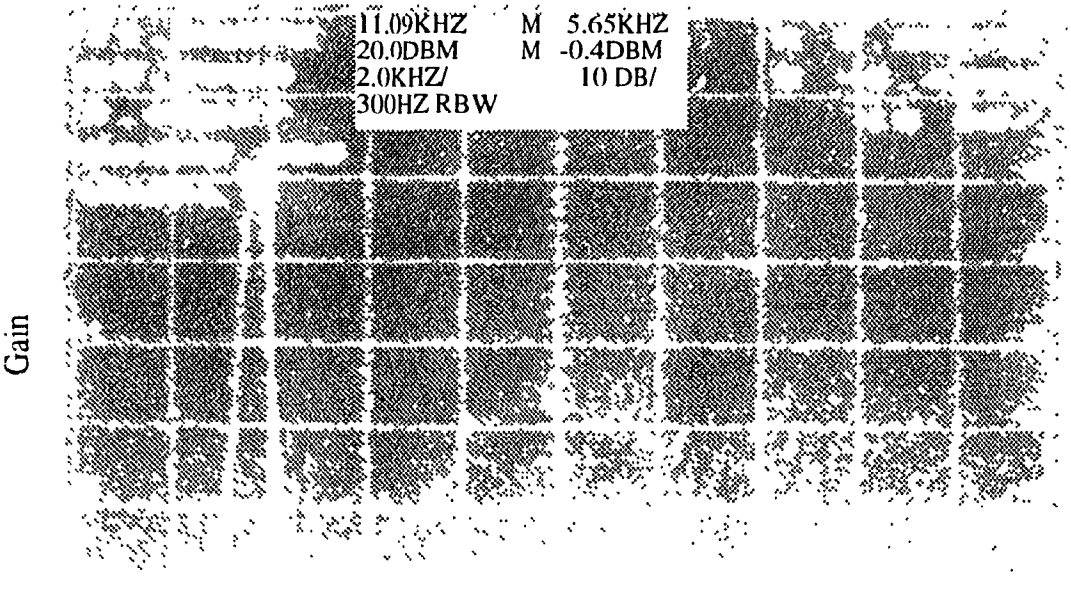


Fig. 3.22 Magnitude frequency spectrum of Cell #3 (V_{dd} = 4.6 V and f_s = 100 KHz)

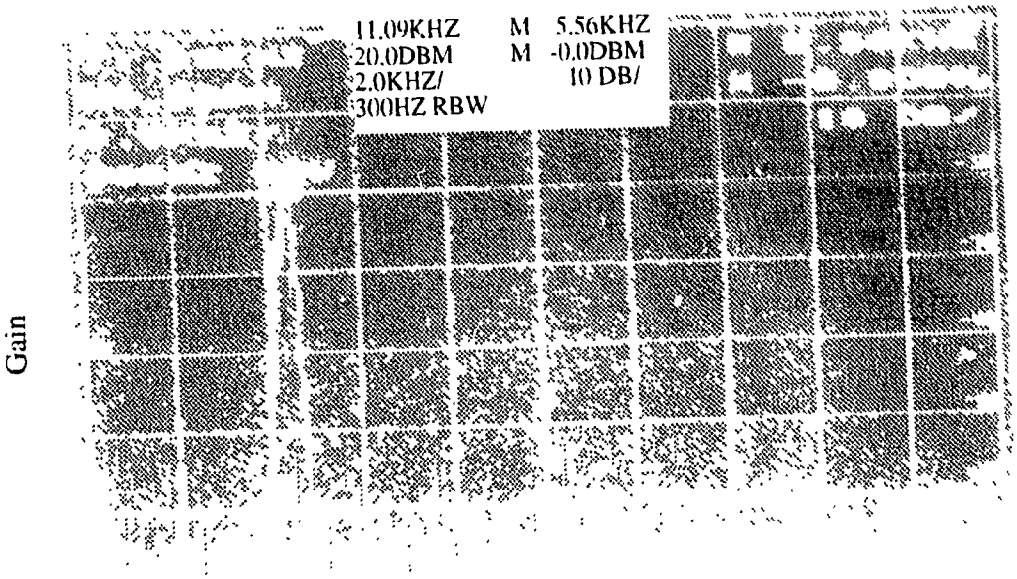


Fig. 3.23 Magnitude frequency spectrum of the input sinusoid signal

To investigate the performance of the memory cells at a lower power supply voltage, we reduce the power supply voltage form 5 V to 3.3 V. Fig. 3.24 to Fig. 3.26 show the test results with this power supply voltage. Table 3.5 lists all the measured results. From the test results, we see that the three differential memory cell have similar performance with Cell #3 providing the best results.

Table 3.5 Test results of the gain error and THD of the prototype chips with V_{dd} = 3.3 V and f_s = 100 KHz

Parameters	Cell #1	Cell #2	Cell #3
Power supply V_{dd} (V)	3.3	3.3	3.3
Current gain error (db)	-0.7	-0.9	-0.1
THD (db)	-52.3	-49.7	-52.9
PSRR (db) (V_{dp} = 0.5 V)	57.5	50.1	58.9

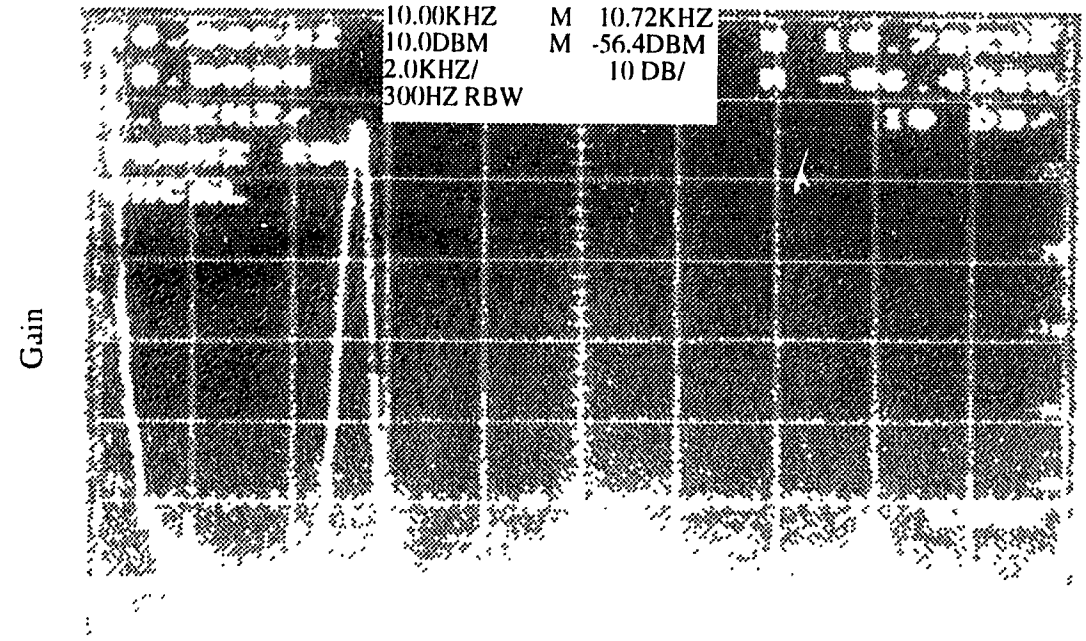


Fig. 3.24 Magnitude frequency spectrum of Cell #1 (V_{dd} = 3.3 V and f_s = 100 KHz)

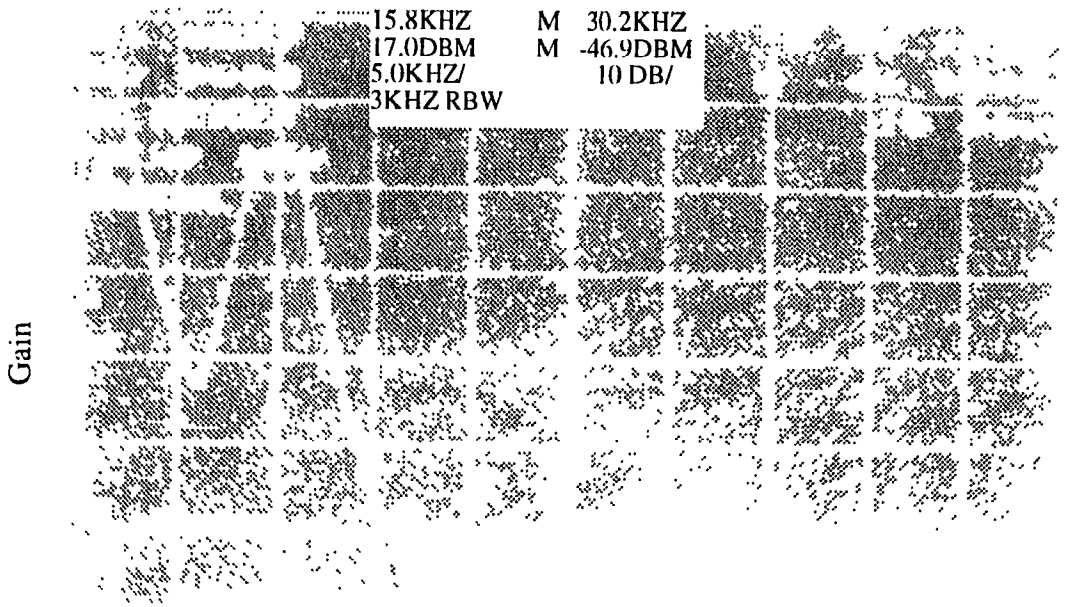


Fig. 3.25 Magnitude frequency spectrum of Cell #2 (V_{dd} = 3.3 V and f_s = 100 KHz)

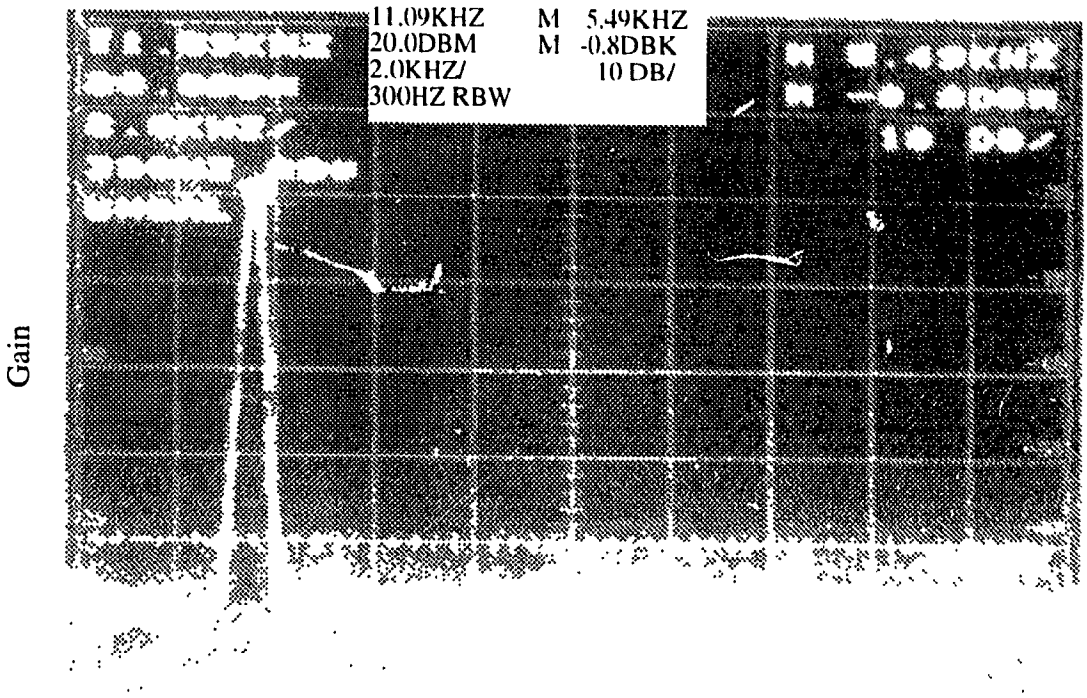


Fig. 3.26 Magnitude frequency spectrum of Cell #3 (V_{dd} = 3.3 V and f_s = 100 KHz)

Comparing the test results when the power supply voltage 5 V with those when it is 3.3 V we find that the gain error of the memory cell is slightly increased when the supply voltage is lowered, and the harmonic distortion of the memory cells become a little lager. Overall, the gain and distortion performance of the cells remains quite satisfactory when the supply voltage is decreased to 3.3 V.

- *Current Dynamic Range*

Fig. 3.27 shows the test results of the current dynamic range for the prototype chips. From the test results, we see that Cell #1 has a very large dynamic range (when current change from 0 to 800 μA, the current gain error is less than 0.5 db), and the dynamic range of Cell #3 is small (about 200 μA). However, it is still satisfactory.

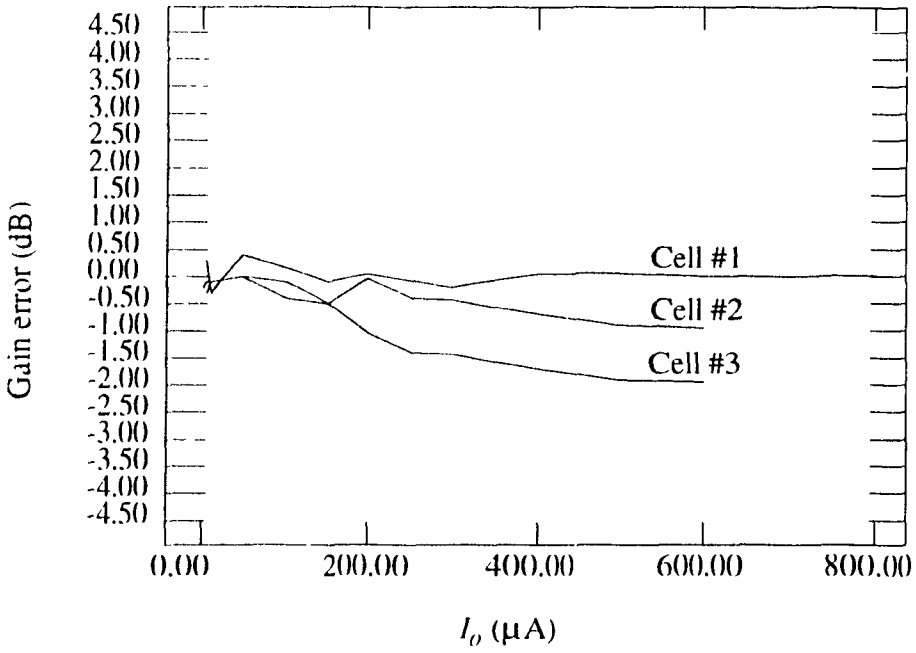


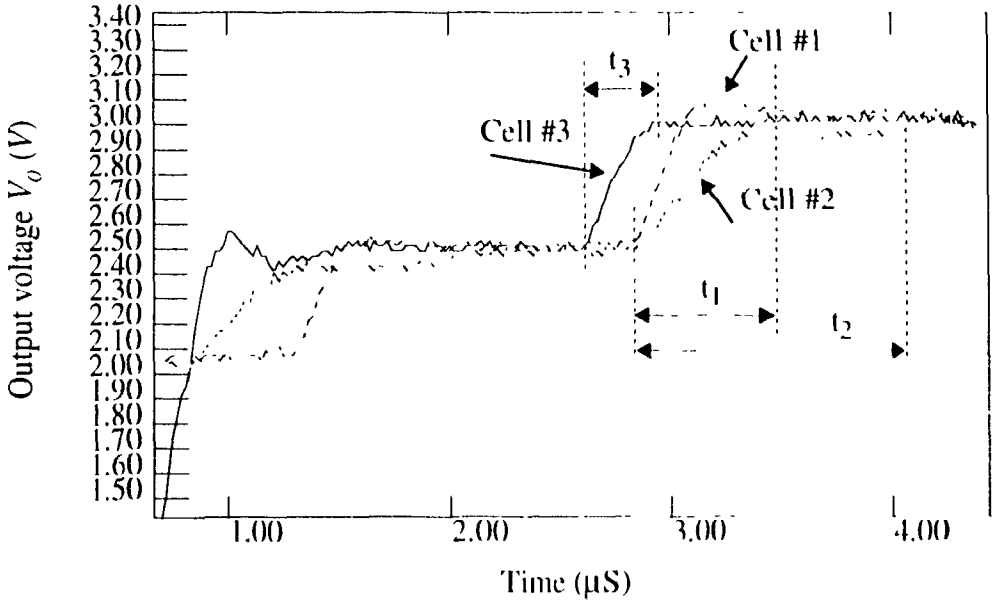
Fig. 3.27 Dynamic range of the prototype chips

- *Settling Time*

The chips were te. ted for the settling time. Cell #2, when tested, was found to have a stability problem. Thus, the value of the capacitor C (see Fig. 3.18) was increased to 31 pf for this cell. All chips test results are shown in Fig. 3.28, from which we see that Cell #3 has the shortest settling time and achieves monotonic settling. Cell #2 (with C = 31 pf) has the worst settling time. Since an operational amplifier is used for current to voltage conversion in the test circuit, the settling time shown in Fig. 3.28 includes the slew rate of the operational amplifier TL081 (about 13 V/μS).

To verify the settling time error effects, chips were tested to give the frequency spectrums with the sampling frequency f_s = 500 KHz and the input signal frequency f_i = 50 KHz, and they are shown in Fig. 3.29 to Fig. 3.31. Table 3.6 gives measured results of the

gain error, THD and the settling times of the chips. It is clear from this table that the performance of Cell #1 and Cell #2 gets worse when the sampling frequency is increased from 250 KHz to 500 KHz. However, the performance of Cell #3 is approximately the same for both the sampling frequencies. Thus, the folded cascode SI memory cell (Cell #3) has a better high-speed performance.



t_1: settling time of Cell #1
t_2: settling time of Cell #2
t_3: settling time of Cell #3

Fig. 3.28 Output voltages of the cells to determine the settling time

Table 3.6 Test results of the gain error and THD of the prototype chips with V_{dd} = 5 V and f_s = 500 KHz

Parameters	Cell #1	Cell #2	Cell #3
Power supply V_{dd} (V)	5	5	5
Current gain error (dB)	-2.7	-0.9	1.1
THD (dB)	-26	-15.2	-51
Settling time (ns)	600	1250	300

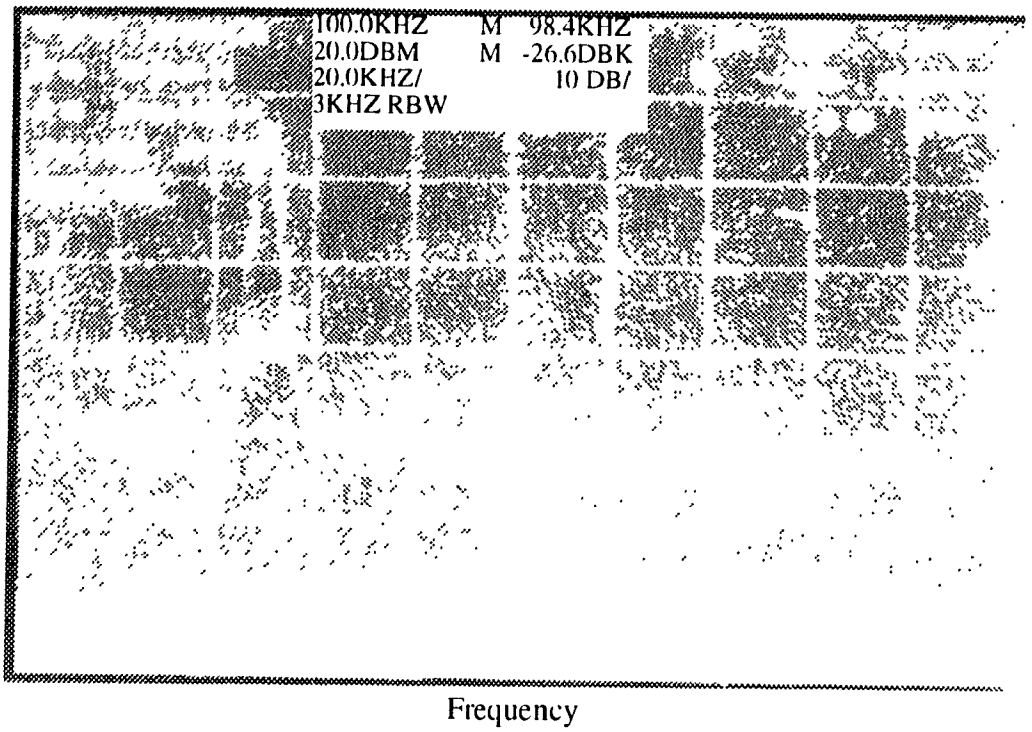


Fig. 3.29 Magnitude frequency spectrum of Cell #1 (V_{dd} = 5 V and f_s = 500 KHz)

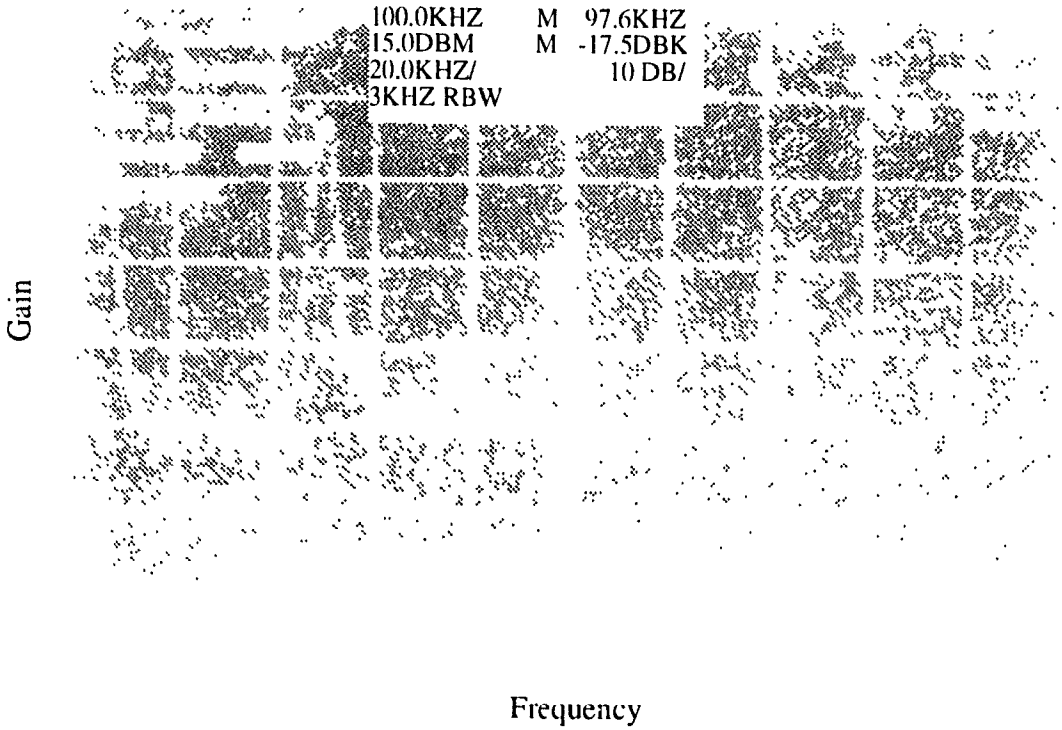


Fig. 3.30 Magnitude frequency spectrum of Cell #2 (V_{dd} = 5 V and f_s = 500 KHz)

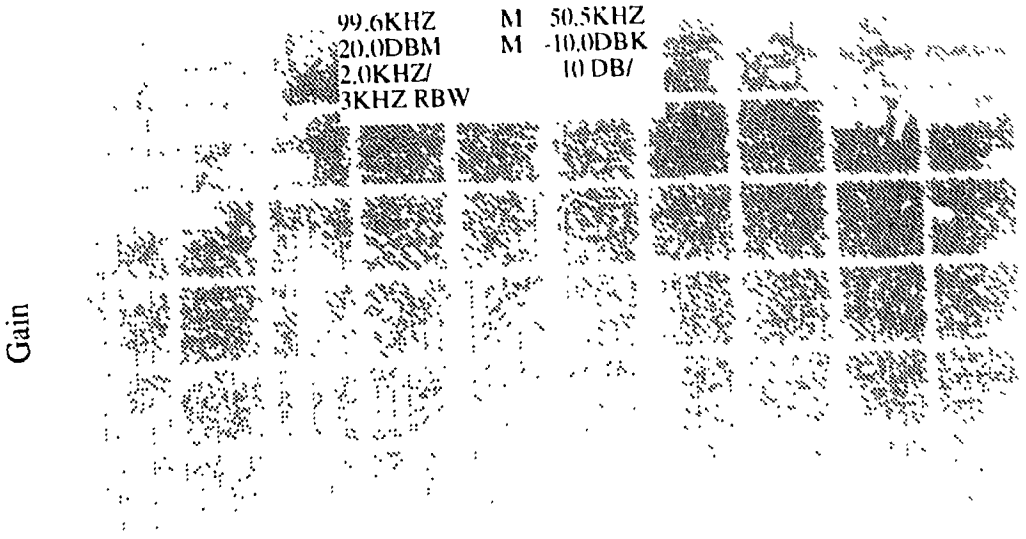


Fig. 3.31 Magnitude frequency spectrum of Cell #3 (V_{dd} = 5 V and f_s = 500 KHz)

3.3 Summary

As a memory cell is the most fundamental building block of any SI circuit or system, a design technique of a high-performance differential SI memory cell using a single-ended differential amplifier has been described in this chapter. Using this design technique two memory cells have been proposed, one using a transconductance amplifier (DMC-I) and the other using folded cascode amplifier (DMC-II). The DMC-I has a very small current gain error and a very wide dynamic range. Since it is a two . ige configuration, it requires a compensation circuit due to the stability problem. However, its use in high-frequency applications is still limited. The DMC-II is a single-stage configuration and, as such, gives much better stability performance for high-speed applications. Both the cells have been

theoretically analyzed, simulated using HSPICE with 1.2 μ N-well CMOS process paramcters. The simulation results indicate several very interesting properties listed below when compared with the existing SI memory cells.

1) *Very small current transmission error*: Since the switch charge injection is reduced significantly by employing the differential structure at the input, the clock feedthrough problem (signal-independent switch charge injection) is cancelled. The output resistance of the cells is very high and the output voltage is very close to V_b (a fixed bias voltage). Consequently, the channel length modulation is very much reduced. Also, the signal-dependent switch charge injection is reduced.

2) *PSRR comparable to that of fully differential memory cell (FDMC):* Noise due to the power supply imperfection affects the output voltage. But, the output current is affected simply by the differential input voltage ΔV_g and the base current J, since the cell operates in the current mode. Thus, its output current is immune to distortions in the power supply voltage.

3) *Small base current and large dynamic range*: For the same power dissipation, the dynamic range of the proposed memory cell DMC-I is about twice of any other switched-current memory cell.

4) *Monotonic settling*: Despite an increased accuracy, the cell using the folded amplifier structure, the DMC-II, maintains the same monotonic settling as that of the simple cell or the regulated cascode memory cell (RCMC).

5) *Simple and easy to use*: Compared with the fully differential SI memory cell, the proposed cells have much lower complexity, since the these cells do not use the common-mode feedback (CMF) circuit, double switches, double wires or double scaling transistors.

The proposed memory cells have been fabricated and tested in the laboratory. The test results have shown that the two cells generally give current gain errors smaller than 0.4 dB, harmonic distortions less than -55 dB, and both can operate satisfactorily with power supply voltages in the range 5 V to 3.3 V. While both the cells provide a good dynamic range, DMC-I is better than DMC-II in this respect. The DMC-I can operate satisfactorily with the sampling frequency as high as 100 KHz, whereas, for DMC-I this frequency can be up to 500 KHz.

Chapter 4

FULLY-PROGRAMMABLE SI FILTER DESIGN

Analog designs have become the bottleneck in mixed-mode circuit designs, since the design of analog circuits cannot be afforded with the existing CAD tools which are mostly developed for digital designs. The major problem is the physical design methodology. In an analog design, components must be modelled in a detailed fashion, since their electrical behavior affects the final results significantly. In particular, parasitic components introduced in the layout phase must be controlled in order to meet the performance specification such as bandwidth, gain, etc. Therefore, an optimal design requires intensive design experience and often has to be hand-crafted by experts [26].

A programmable analog circuit could serve as a possible solution, since for different applications, the circuit does not have to be redesigned by an expert in physical design and layout. The circuit can be made to achieve the desired performance simply by programming. However, programmable analog circuits are also difficult to design. For example, a programmable SC filter needs a large array of unit capacitors with digitally controlled switches for coefficient variations. These switches introduce extra parasitic resistances and capacitances, and therefore, affect the coefficient values. Use of a SI circuit is easier than that of a SC circuit for programmable filter design. Programming of coefficient values in a SI filter is done with a transistor array connected in parallel through a set of digitally con-

trolled switches. The MOS switches do not affect the value of the coefficients, since the coefficient values depend on the aspect ratio of the current mirror transistors. However, the existing SI filter design techniques mostly employ SC filter synthesis methods. In this case, a SI filter employs SI integrators and/or differentiators. Although the resulting SI filter can enjoy some of the features of the SC circuits, the structure of the SI filters are not regular. To achieve a fully-programmable filter design, not only the coefficient values need to be programmable, but also the structure of the filter is required to be programmable. Therefore, these methods are not very suitable for programmable filter design. Recently, a methodology to realize programmable SI wave analog filters has been reported [29]. However, this technique requires SI building blocks for implementing series and parallel adapters. This adds to the overall complexity of the implemented SI filter.

In this chapter, SI filters are designed based on digital synthesis technique, i.e. the synthesis technique relies on neither the SC nor wave realization technique. Thus, the resulting SI filter is simpler than that of [29], and is fully programmable. The filter consists of only unit delays, coefficient multipliers, and adders. The structure of the filter is very regular and it does not require modifications in its structure to change the filter characteristics. As an example, a second-order IIR filter is designed using this technique. To reduce the effect of switch charge injection and channel length modulation, the high-performance differential switched-current memory cell, DMC-I designed in Chapter 3 is used as a basic building block. An experimental prototype second-order switched-current IIR filter array which consists of six second-order IIR filters has been fabricated using the standard 1.2 μ N-well CMOS process technology. Hard wiring technique is used for programming of the filters. The fabricated chip is tested in the laboratory to verify its performance.

In Section 4.1, a brief review of realizing some simple digital filter structures is given. Section 4.2 introduces a SI filter design technique based on the digital filter structure discussed in Section 4.1. The effects of non-ideal MOS characteristics on the filter

coefficients are discussed. The SI filters are then implemented using the memory cells of Chapter 3. The layout design consideration are also given in this section. Finally, the test results of the fabricated filters are presented in Section 4.3.

4.1 A Brief Review of Digital Filter Synthesis

A digital filter uses a sampled data process technique for signal processing. Compared with the SC or SI filters, the signal in digital filters must be discrete not only in time, but in amplitude as well. This means the amplitude of the sampled signal has to be quantized to a given accuracy and represented by a corresponding number of binary digital number or bits.

Early digital filters were exclusively implemented in software form; that is, they consisted of algorithms or difference equations with operations involving summation, multiplication, and storage on the associated digital computer [30]. With the development of VLSI technology, it is now feasible to implement a digital filter in hardware form as a special-purpose device. This device still performs the basic operations of addition, multiplication, and storage of iterating the difference equations as in the software implementation. Synthesis of digital filters essentially deals with obtaining digital filter structures from the digital transfer functions. Numerous synthesis techniques have been developed leading to general or specialized structures [31]. A linear time-invariant infinite impulse response (IIR) digital filters is characterized by a z-domain digital transfer function given by

$$H(z) = \frac{N(z)}{D(z)} = \frac{\sum_{m=0}^{M} b_m z^{-m}}{1 + \sum_{n=1}^{N} a_n^{-n}} \qquad \text{(EQ 4.1)}$$

When this transfer function is realized directly, it gives a structure shown in Fig. 4.1.

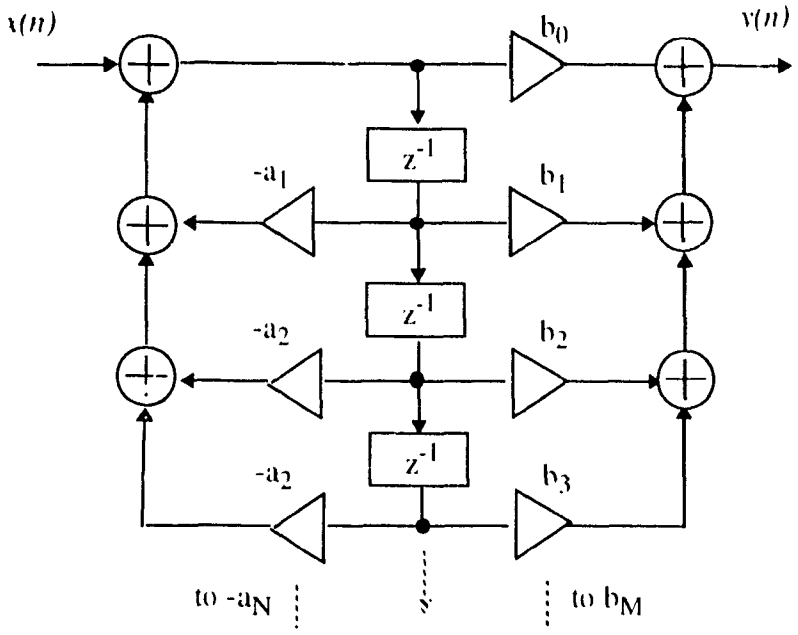


Fig. 4.1 Direct-form structure

The transfer function given in (EQ 4.1) can be expanded using a partial-fraction expansion as

$$H(z) = \beta_0 + \sum_{i=1}^{L} \frac{\beta_{0i} + \beta_{1i} z^{-1}}{1 + \alpha_{1i} z^{-1} + \alpha_{2i} z^{-2}} \qquad \text{(EQ 4.2)}$$

with

$$L = \left[\frac{N+1}{2} \right]_{int} \qquad \text{(EQ 4.3)}$$

where $[.]_{int}$ denotes the largest integer less than or equal to the argument. If N is odd, there is a first-order term in (EQ 4.2). Realization of this form of the transfer function yields a structure shown in Fig. 4.2 which is called the parallel structure.

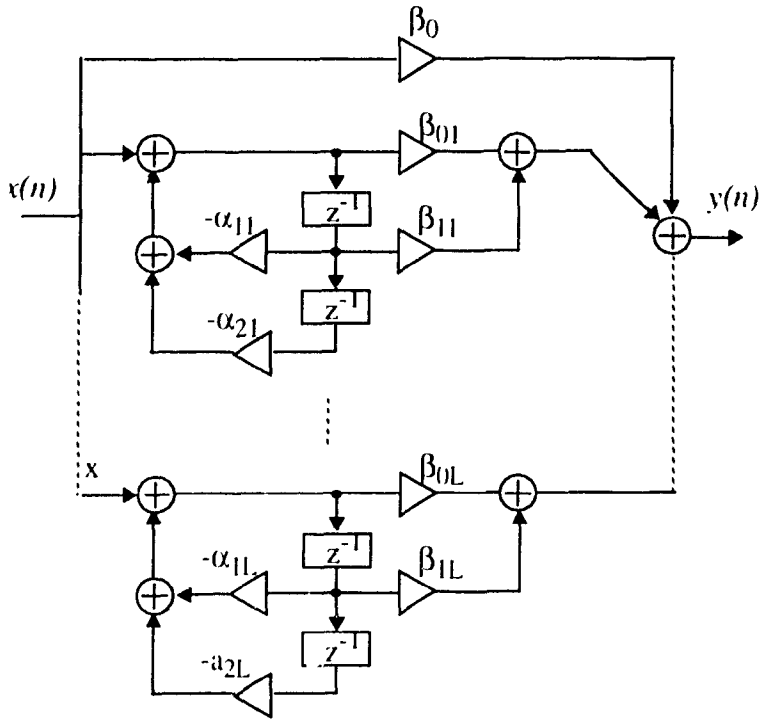


Fig. 4.2 Parallel structure

By factoring the denominator polynomial D(z) of (EQ 4.1) into second-order polynomials, the system function can be written as the product

$$H(z) = b_0 \prod_{i=1}^{L} H_i(z), \qquad \text{(EQ 4.4)}$$

where

$$H_i(z) = \frac{1 + \beta_{1i} z^{-1} + \beta_{2i} z^{-2}}{1 + \alpha_{1i} z^{-1} + \alpha_{2i} z^{-2}} \qquad \text{(EQ 4.5)}$$

in which L is again given by (EQ 4.3), and $\alpha_{2L} = \beta_{2L} = 0$ if N is odd. Since H(z) is formed as the product of the second-order functions $H_i(z)$, the corresponding filter structure comprises a cascade of second-order sections. Fig. 4.1 shows such a structure.

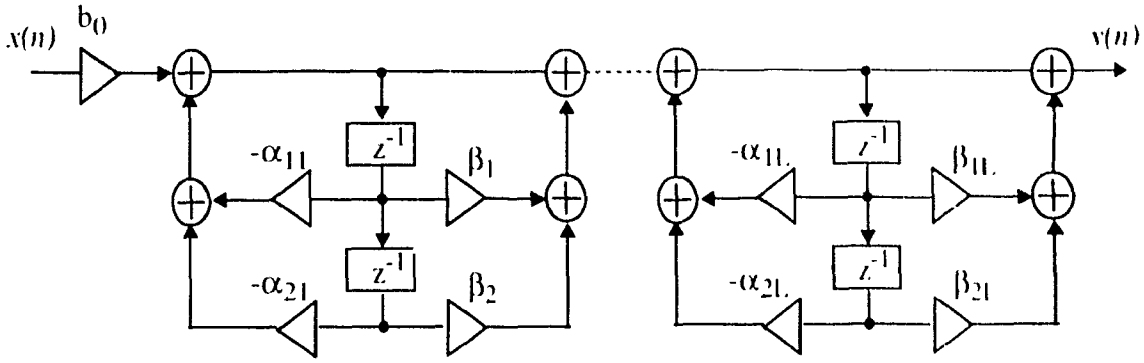


Fig. 4.3 Cascade structure

One of the concerns in the design of digital IIR filters is their stability. To obtain the conditions for the coefficients of the parallel or cascade forms that ensure the stability of the filter the second-order denominator factors of these forms are written as

$$D_i(z) = 1 + \alpha_{1i} z^{-1} + \alpha_{2i} z^{-2}$$

$$= (1 - p_{1i} z^{-1})(1 - p_{2i} z^{-1}) \qquad \text{(EQ 4.6)}$$

where $\alpha_{1i} = -(p_{1i} + p_{2i})$ and $\alpha_{2i} = p_{1i} p_{2i}$. The poles of the filter must lie inside the unit circle of the z-plane for stability, i.e.,

$$|p_{1i}|, |p_{2i}| < 1 \qquad \text{(EQ 4.7)}$$

Hence, we have

$$\alpha_{2i} = |p_{1i} p_{2i}| < 1 \qquad \text{(EQ 4.8)}$$

The corresponding condition on α_{1i} can be obtained from the expression

$$p_{1i}, p_{2i} = \frac{-\alpha_{1i} \pm \sqrt{\alpha_{1i}^2 - 4\alpha_{2i}}}{2} , \qquad \text{(EQ 4.9)}$$

and is given by

$$|\alpha_{1i}| < 1 + \alpha_{2i} \qquad \text{(EQ 4.10)}$$

Sensitivity is another concern in the implementation of a digital filter. It is a measure of the deviation in some performance characteristic of the filter due to some change in nominal value of one or more of the elements of the network. Low-sensitivity circuits are naturally preferred over high-sensitivity circuits. In a filter characterized by

$$H(z) = f(z, m_1, m_2, \ldots) , \qquad \text{(EQ 4.11)}$$

where $m_1, m_2, \ldots$ are the multiplier coefficients, the sensitivities are given by

$$S_{m_i}^{H} = \frac{m_i}{H} \frac{\partial H}{\partial m_i} \qquad i = 1, 2, \ldots \qquad \text{(EQ 4.12)}$$

For analysis of a second-order IIR filter, (EQ 4.5) can be rewritten as

$$H(z) = \frac{N(z)}{D(z)} = \frac{1 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \qquad \text{(EQ 4.13)}$$

Examining just the poles of the filter and assuming that a complex pair of poles is required at $z_{1,2} = re^{\pm j\theta}$, the transfer function of denominator polynomial of (EQ 4.13) can be written in the form

$$H_D(z) = \frac{1}{(z - re^{j\theta})(z - re^{-j\theta})} , \qquad \text{(EQ 4.14)}$$

or as

$$H_D(z) = \frac{1}{1 - 2r\cos\theta z^{-1} + r^2 z^{-2}} \qquad \text{(EQ 4.15)}$$

Comparing (EQ 4.13) with (EQ 4.15), we have

$$a_1 = 2r\cos\theta \qquad \text{(EQ 4.16)}$$

and

$$a_2 = r^2 \qquad \text{(EQ 4.17)}$$

The sensitivity of r, θ and H_D with respect to the coefficients a_1 and a_2 can be obtained as

$$S^r_{a_1} = \frac{\partial r}{\partial a_1} = 1 \qquad \text{(EQ 4.18)}$$

$$S^r_{a_2} = \frac{\partial r}{\partial a_2} = \frac{1}{2} \qquad \text{(EQ 4.19)}$$

$$S^\theta_{a_1} = \frac{\partial \theta}{\partial a_1} = \frac{-1}{\theta\tan\theta} \qquad \text{(EQ 4.20)}$$

$$S^\theta_{a_2} = \frac{\partial \theta}{\partial a_2} = \frac{1}{2\theta\tan\theta} \qquad \text{(EQ 4.21)}$$

$$S^H_{a_1} = \frac{\partial H}{\partial a_1} = \frac{2r^2}{1 - r^2} + \frac{1}{(\tan\theta)^2} \qquad \text{(EQ 4.22)}$$

$$S^H_{a_2} = \frac{\partial H}{\partial a_2} = \frac{r^2}{1 - r^2} - \frac{1}{(\tan\theta)^2} \qquad \text{(EQ 4.23)}$$

As the order of the polynomial increases, the coefficient sensitivity will increase. Therefore, for reducing the sensitivity of a higher-order filter design, the structure of the filter should use a cascade, parallel, or lattice form, etc.

As we can see, the value of the coefficients in the z transfer function determine the pole and zero locations, and therefore, determine the characteristic of the filter. There are

several available techniques that can be used to obtain the coefficient values from a given filter specification [30].

4.2 SI Filter Design

As seen above, a digital filter synthesis technique uses unit delays which are usually implemented by digital master-slave registers, digital multipliers which multiply the signals with the associated coefficients stored in digital memory (RAM or ROM), and digital adders. Whence the circuit of the digital filter is implemented, we can obtain different filter characteristics simply by changing the coefficient values stored in the memory without requiring any change in the circuit. This feature of digital filters is referred to as programmability. The digital filter synthesis techniques of transforming a filters structure into a digital circuit can also be used in the design of SI filters.

4.2.1 Design Using Digital Filter Structure

The building blocks of any digital filter structure are simply multipliers, unit delays and adders. Two SI memory cells can be used to implement an analog unit delay. Each multiplier coefficient of the filter can be realized by including an additional coefficient transistor in the cell. The coefficient transistors are connected in a current mirror configuration with the memory transistors. The output of the coefficient transistors can be connected directly for current summation.

Fig. 4.4 shows an example circuit of a SI delay with two multiplier coefficients. We refer to this circuit as a SI delay-multiplier unit. The circuit uses two simple SI memory cells and two coefficient transistors. The two memory cells are cascaded as an analog master-slave register which performs the unit delay function. The size ratio of transistors T_1 and T_2 is c_1, and that of T_3 and T_4 is c_2. The operation of the circuit is as follow: On phase ϕ_2 of the clock period (n - 1), transistor T_1 samples the signal current I_i(n - 1). On the next

phase ϕ_1 which falls in the next clock period (n), T_1 holds the current J + I_i(n - 1) and loads the signal current I_i(n - 1) into the second memory cell T_3, since T_3 is now in the sample mode. Meanwhile, because of the mirror circuits, we have $I_{c1} = -c_1 I_i$(n - 1), and $I_{c2} = c_2 I_i$(n - 1). On the next phase ϕ_2 (still in clock period (n)), T_3 is in the hold mode and it holds the current J + I_i(n - 1) and the output current $I_o(n) = I_i$(n - 1). The relationship between the input and output current signals can be expressed as

$$I_o(n) = I_i(n-1) \qquad \text{(EQ 4.24)}$$

$$I_{c1}(n) = -c_1 I_i(n-1) \qquad \text{(EQ 4.25)}$$

$$I_{c2}(n) = c_2 I_i(n-1) \qquad \text{(EQ 4.26)}$$

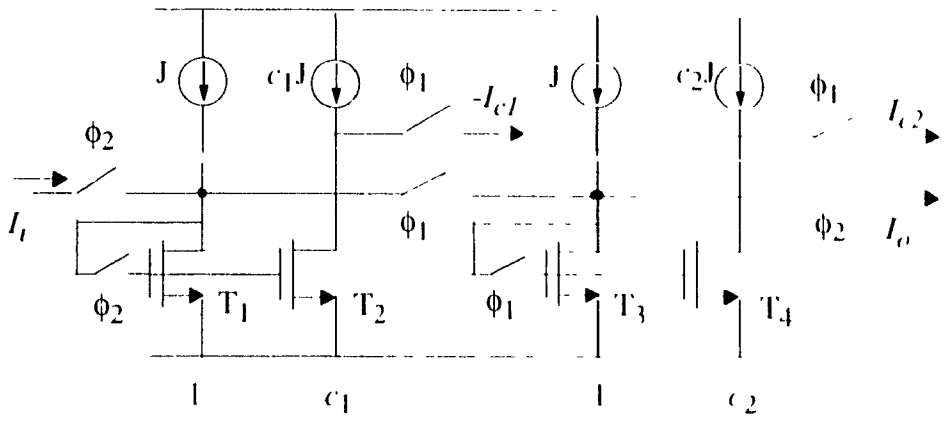
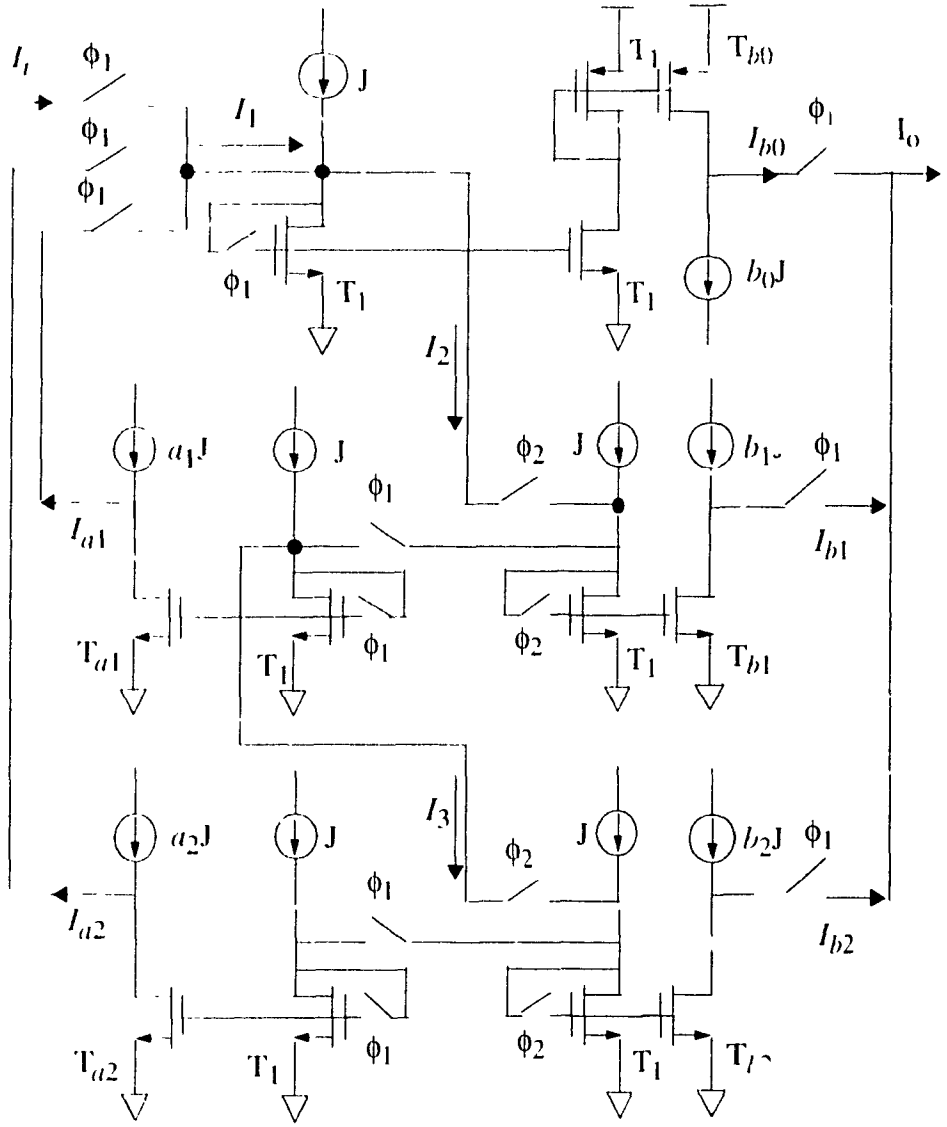


Fig. 4.4 A SI delay unit with two coefficient transistors
(a SI delay-multiplier unit)

The circuit of Fig. 4.4 realizes the unit delay operation and generates the delayed and multiplied negative and positive current signals $-I_{c1}$ and I_{c2}. The values of the scaling factors of c_1 and c_2 implement analog multiplier coefficients of the filter. Each of the SI delay

multiplier unit can be connected to other such units directly in order to perform the current addition operation.



T_m represents a transistor with the size ratio equal to m

Fig. 4.5 A second-order SI IIR filter.

A complete second-order SI IIR filter is shown in Fig. 4.5. For this second-order filter, two SI delay-multiplier units and one coefficient amplifier (referred to as the SI multi-

plier unit) are used. The output currents of these units can be expressed as

$$I_{a1}(n) = -a_1 I_1(n-1) \quad \text{(EQ 4.27)}$$

$$I_{a2}(n) = -a_2 I_1(n-2) \quad \text{(EQ 4.28)}$$

$$I_{b0}(n) = b_0 I_1(n) \quad \text{(EQ 4.29)}$$

$$I_{b1}(n) = b_1 I_1(n-1) \quad \text{(EQ 4.30)}$$

$$I_{b2}(n) = b_2 I_1(n-2) \quad \text{(EQ 4.31)}$$

where $I_1(n)$ is given by

$$I_1(n) = I_i(n) + I_{a1}(n) + I_{a2}(n) \quad \text{(EQ 4.32)}$$

The output current of the filter is obtained as

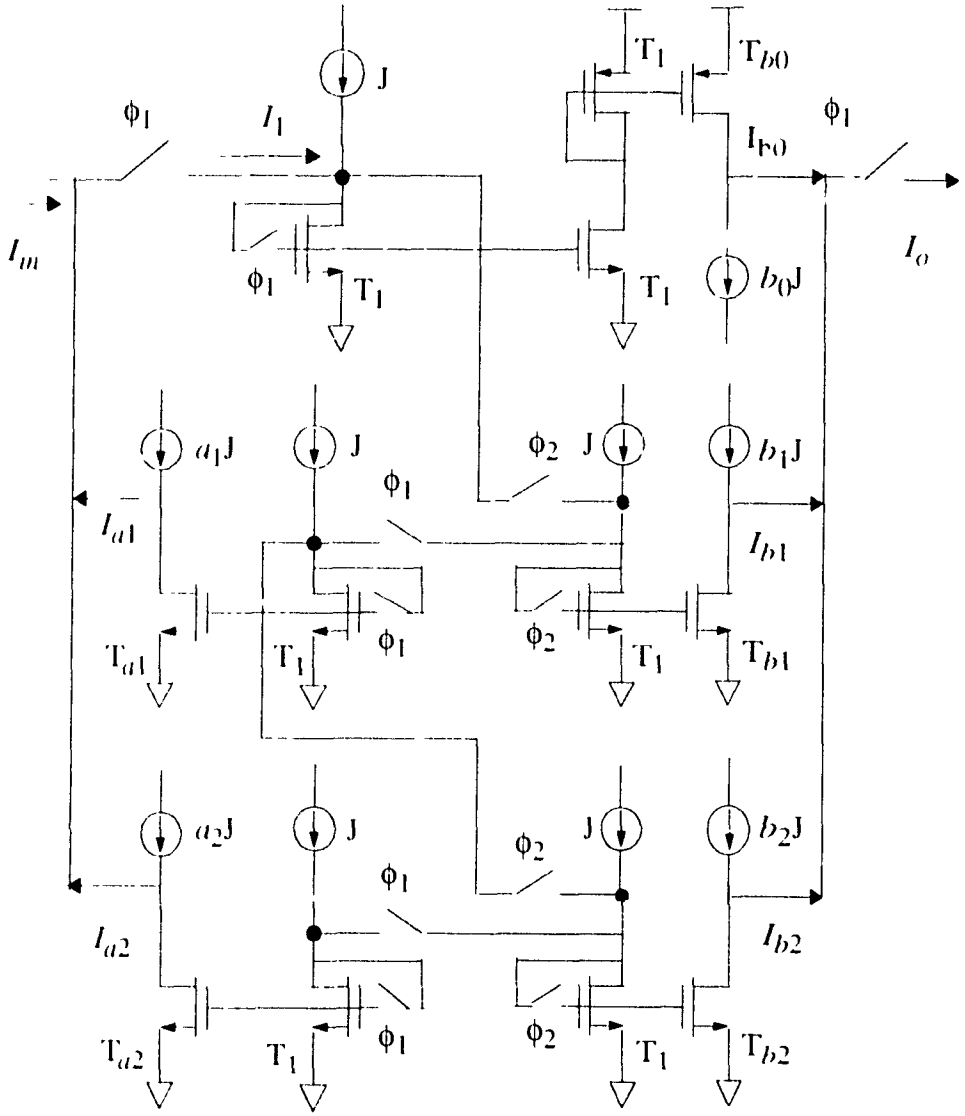
$$I_o(n) = I_{b0}(n) + I_{b1}(n) + I_{b2}(n) \quad \text{(EQ 4.33)}$$

From (EQ 4.27) through (EQ 4.33), we can obtain the z-domain transfer function of the filter, as

$$H(z) = \frac{I_o}{I_i} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \quad \text{(EQ 4.34)}$$

Thus, by employing the circuit of Fig. 4.4 we can obtain a SI filter corresponding to the digital filter structure of Fig. 4.1 (or corresponding to any other digital filter structure). Obviously, the coefficients of equation (EQ 4.34) are directly matched, one to one, to the scaling coefficients of the transistors of the SI filter. By simply changing the aspect ratios

of the coefficient transistors, the desired characteristics of the filter can be achieved. Therefore, this technique is very suitable for programmable SI filter design. By applying the re-timing technique, the filter in Fig. 4.5 can be redrawn in the form shown in Fig. 4.6, which has four fewer switches.



T_m represents a transistor with the size ratio equal to m

Fig. 4.6 A second-order SI IIR filter after re-timing

4.2.2 Analysis of the SI Filters with Non-Ideal MOS Devices

As discussed in Section 4.2.1, the building blocks of the proposed SI IIR filter are the SI delay-multiplier unit and the SI multiplier unit. The delay-multiplier unit consists of two SI memory cells and two current mirror circuit which are used for generating a multiplier coefficient. In a practical filter design, the effects of the non ideal characteristics of MOS transistors, such as switch charge injection, channel length modulation, and mismatch between current mirror transistors, have to be considered. In this sub section, we will discuss the effects of non-ideal MOS characteristics on the performance of the SI delay-multiplier unit that uses the simple SI memory cell.

- *Unit-Delay Gain Error Due to the Finite Impedance and the Switch Charge Injection of the Memory Cell*

The finite impedance and switch charge injection affect the filter performance through an error in the current gain of the unit-delay part of the SI delay-multiplier unit. Considering only the finite impedance, we have, from (EQ. 2.19), the gain of the unit delay as

$$A = \frac{I_o}{I_i} = \left(1 - \frac{2g_o}{g_m} - \frac{g_o}{g_s}\right), \qquad \text{(EQ 4.35)}$$

where g_m is the transconductance of the memory transistor T_1 or T_3, g_o is the output transconductance of memory cell T_1 or T_3, and g_s is the closure resistance of the switch (see Fig. 4.4). In practice, the current signal in the filter is small (< 100 μA) and the effect of the non-zero closure resistance of the switch can be ignored. Therefore, the gain of the unit delay can be simplified to be

$$A = \frac{I_o}{I_i} = \left(1 - \frac{2g_o}{g_m}\right) \qquad \text{(EQ 4.36)}$$

The output currents I_{o1} and I_{o2} from the coefficient transistors, therefore become

$$I_{oi} = c_i\left(1 - \frac{2g_o}{g_m}\right)I_i, \qquad i = 1, 2 \tag{EQ 4.37}$$

Thus, because of the finite impedance, the unit delay has a gain error.

When considering the switch charge injection effect, from (EQ 2.28) the output current of the unit delay is given by

$$I_o = I_i + \frac{2\delta VJ}{V_{GS} - V_t}\sqrt{\frac{J+1}{J}} + \frac{\beta}{2}\delta V^2 \tag{EQ 4.38}$$

and the output currents from the coefficient transistors are given as

$$I_{oi} = c_i\left(I_i + \frac{2\delta VJ}{V_{GS} - V_t}\sqrt{\frac{J+1}{J}} + \frac{\beta}{2}\delta V^2\right) \tag{EQ 4.39}$$

Thus, the switch charge injection creates an offset error, gain error, and harmonic distortions.

- *Coefficient Error Due to Current Mirror Mismatch*

Since the multiplier outputs are generated by using current mirror circuit, the mismatch between the current mirror transistors will cause errors in the coefficient transistor output currents. As mentioned in the Section 2.5.4, the mismatch could happen in terms of the threshold voltage V_t, the device aspect ratio W/L, the process gain factor k_p, and the channel length modulation parameter λ. Most of these process mismatches result in current gain errors in the current mirror circuit, but the threshold voltage mismatch also causes the harmonic distortions in the output current.

- *Settling Time Error*

For high-frequency filtering applications, the settling time error have to be taken into account. The effect of the settling time error is very similar to that of switch charge injection. It creates an offset error, a gain error and harmonic distortions. The maximum operating frequency of the filter is limited by the settling time of the memory cell.

4.2.3 Design of SI Delay-Multiplier Unit Using DMC-I

As discussed in Section 4.2.2, the non-ideal characteristics of MOS devices can significantly affect the performance of the filters. In order to reduce the unit-delay gain error, high performance SI memory cells are required. Any existing enhanced SI memory cells can be used to replace the simple memory cell. A fully differential SI memory cell may have a good performance, since the cell can achieve cancellation of first-order switch charge injection and cross-talk from neighboring digital circuits. However, the overall SI delay-multiplier unit circuit will become very complicated and the size of the chip will almost double, since the coefficient transistors, switches and internal connect wiring will all be doubled. In this prototype programmable filter design, the simple memory cells are therefore, replaced by the differential SI memory cell DMC-I described in Chapter 3. The DMC-I with coefficient transistors is shown in Fig. 4.7, which implements one-half of the SI delay-multiplier unit. In this implementation, the error voltage due to the clock feedthrough problem becomes a common-mode signal appearing at the input of the memory cell and it is rejected by the amplifier. Therefore, the effect of signal-independent switch charge injection is eliminated. The output stage of the memory cell employs PMOS and NMOS regulated cascode circuits. The output resistance of the memory cell is, therefore, increased significantly and the effect of channel length modulation is much reduced. The voltage gain of the memory cell is also very large due to a very large output resistance. Therefore, the voltage at node B (Fig. 4.7) becomes very close to the base voltage V_b when

circuit operates in the sample mode. In a SI filter circuit, the output of the memory cell and coefficient transistors are connected to the next input of the memory cell. Using DMC-I keeps the output voltage constant and approximately equal to the base voltage. Therefore, the use of DMC-I in the implementation of the SI delay-multiplier unit can be expected to reduce the unit-delay gain error.

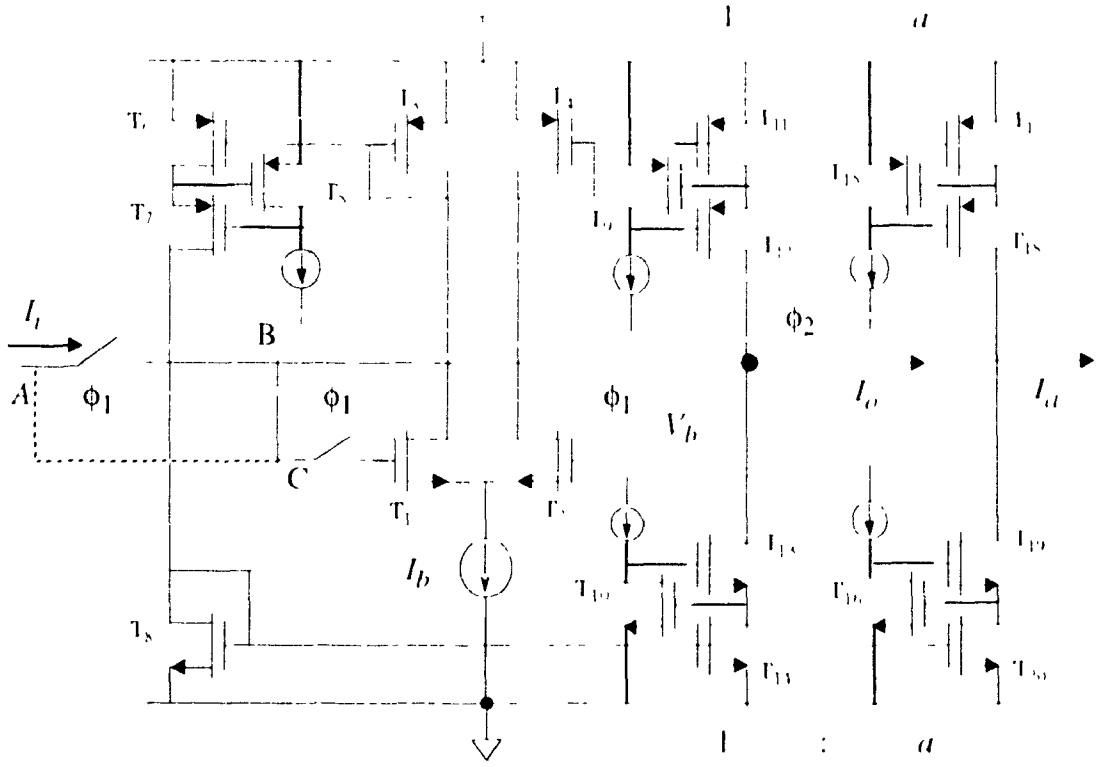


Fig. 4.7 One-half of the SI delay-multiplier unit using DMC-I

4.2.4 Simulation Results

A second-order elliptic lowpass SI IIR filter with the specification of passband ripple < 1 dB, stop-band ripple < -20 dB and a bandwidth of 0.2 percent of the sampling frequency is designed using the proposed design technique and employing DMC-I as the

memory cells. The coefficient values are obtained from the Matlab digital signal processing package. Table 4.1 lists the coefficient values of the filter.

Table 4.1 The coefficient values of a second-order elliptic lowpass IIR filter

a_1	a_2	b_0	b_1	b_2
-0.517	0.362	0.264	0.318	0.263

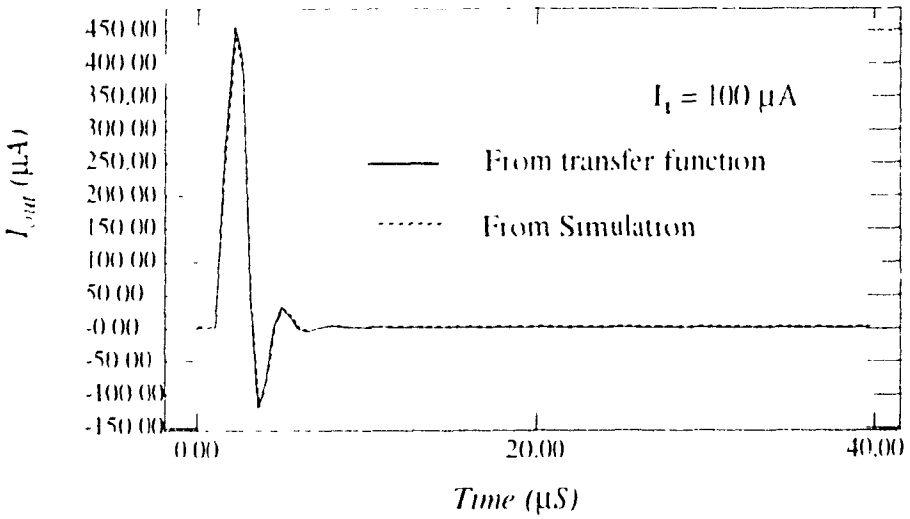
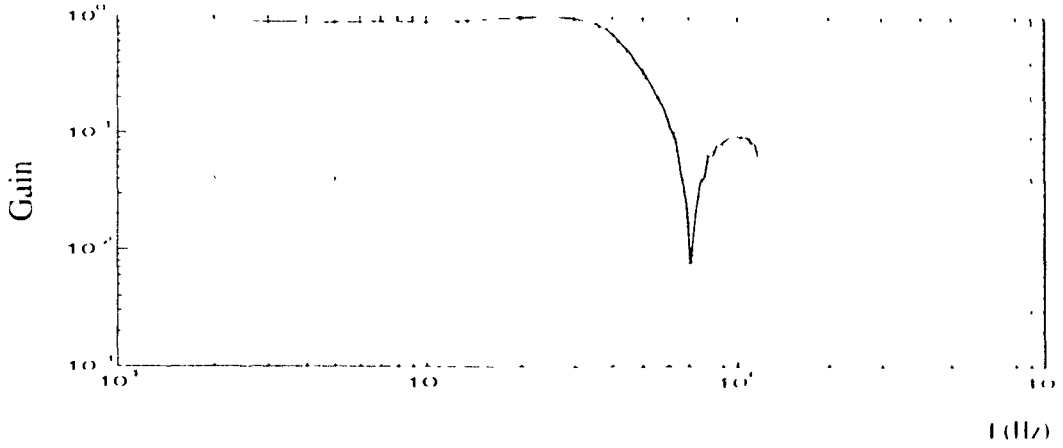


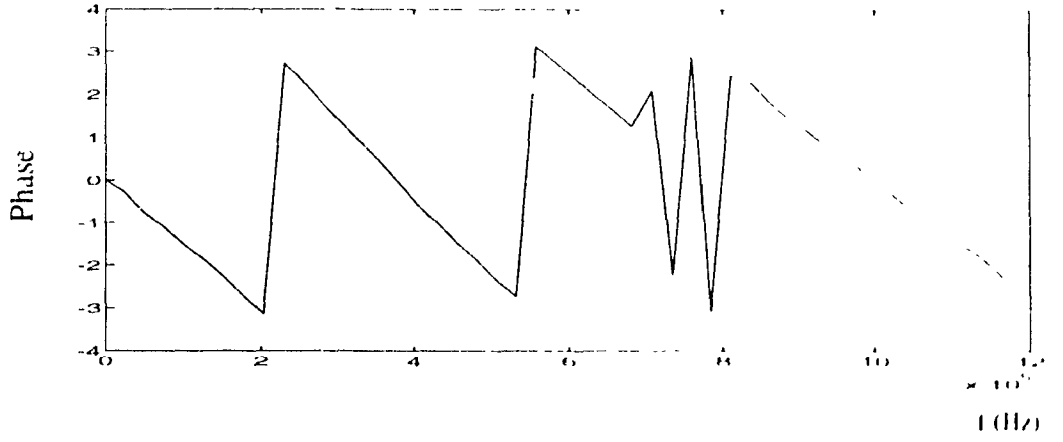
Fig. 4.8 The impulse response of the SI IIR filter.

In order to estimate the designed filter's characteristics, HSPICE simulation is used with the parameter set of the 1.2 μ N-well CMOS process technology. Since the SI filter operates with discrete signals, the ac analysis of HSPICE cannot be used to evaluate the frequency characteristics of the filter directly. For evaluating these characteristics, the impulse response of the filter is simulated using the transient analysis of HSPICE. The HSPICE transient analysis can simulate the effects of the switch charge injection, channel length modulation, settling time error, and the MOS transistors ratio mismatch error in the time domain. From Fig. 4.8, we see that the simulation results are very close to those obtained from the filter transfer function. For evaluating the frequency response of the fil-

ter, the FFT analysis method is employed. The FFT analysis can transform the time domain information into the frequency domain giving the filter's characteristics such as the ripple and bandwidth. Fig. 4.8 shows the impulse response of the filter obtained from the HSPICE simulation, and Fig. 4.9 gives the results of the FFT analysis giving the magnitude and phase responses.



a) Magnitude



b) Phase

Fig. 4.9 FFT analysis of the filter frequency characteristics

From Fig. 4.9, we see that the filter has a 3-dB cut-off frequency of about 400 KHz with the sampling frequency of 2 MHz, a passband ripple of about 1 dB, and a minimum stopband attenuation of -20 dB. They are very close to the given specifications.

4.3 Chip Design and Implementation of the Proposed SI Filter

A complete filter requires some other sub-circuits that work as interfaces between the input signal or control signal and internal filter circuits. In this section, we will first discuss these sub-circuits. Next, in order to verify the proposed SI filter design concepts, we proceed to design an experimental prototype chip of the filter and the associated sub-circuits. In this connection, we also discuss the design consideration of the chip layout. Finally, the test results of the prototype chip are presented.

4.3.1 Sub-Circuits Used for Programmable SI Filter Design

A complete SI filter may require some other sub-circuits such as a voltage-current converter which is used as a interface for converting the voltage-mode signals to current-mode signals, an overlapped clock generator for removing the glitches, etc. In this section, we will present these circuits to be used in the prototype chip design.

- *Voltage-Current Converter*

The DMC-I, used in the circuit of Fig. 4.7, can also be used as a high-quality voltage-current converter (by changing the switch connection C from node B to node A as shown by the dashed line in Fig. 4.7) because of the cell has high-output resistance and differential input pairs [43]. Fig. 4.10 shows the application of the memory cell in switched voltage-current converter mode. On phase ϕ_1, the input current I_i is given by

$$I_i = \frac{V_{in} - V_b}{R} \qquad \text{(EQ 4.40)}$$

On phase ϕ_2, the memory cell holds the input, and the output current I_o becomes $-I_i$. This voltage-current converter is used in prototype SI filter.

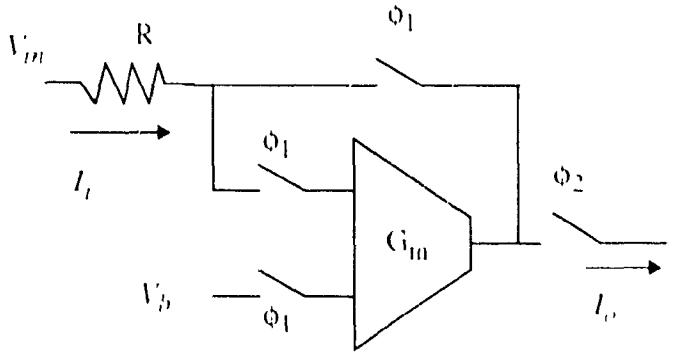


Fig. 4.10 Voltage-current converter using proposed SI memory cell

- *Overlapped Clock Generator*

To reduce the glitches in the SI memory cell, an overlapped clock generator is required to control the performance of the SI filters. Fig. 4.11 gives an overlapped clock generator circuit which uses the delay gate to achieve the overlap. Again, this circuit is used in the prototype filter chip design.

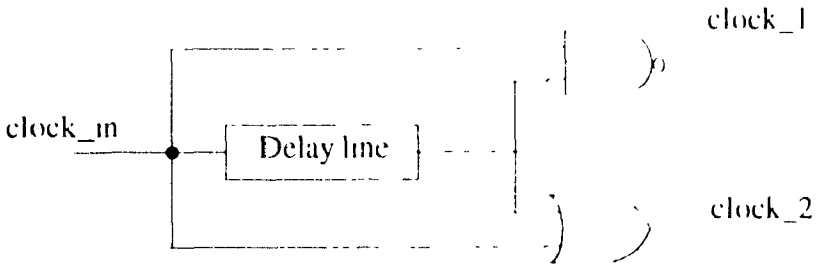


Fig. 4.11 Circuit for overlapped clock generator

4.3.2 Chip Layout Design

In a programmable filter design, the ratio of the coefficient transistors must be programmable. This is realized by using a transistor array in the chip layout design. Use of a transistor array for the coefficient and memory transistors implementation can also reduce the transistor mismatch problem. Normally, the transistor array consists of unit or minimum size transistors. However, for a programmable SI filter design and implementation, this would make the area of the transistor array too large. For example, if the required accuracy of the coefficients are within three decimal places, the transistor array should contain one thousand unit transistors to implement one coefficient transistor, and another one thousand unit transistors to implement one memory transistor. Five similar size transistor arrays are required for implementing a second-order IIR filter, since the filter has five multiplier coefficients.

In order to reduce the chip area in the prototype implementation, a transistor array using three different sizes of transistors are used. Fig. 4.12 shows the layout of the transistor array. The three different sizes of the transistors in the array represent the ones, tens and hundreds of decimal places. The memory transistors and the most significant bit transistors are implemented using the largest size transistors from the array. Therefore, they create smaller mismatches. On the other hand, the least significant bits of the multiplier coefficients are implemented using the largest size memory transistors and the smallest size coefficient transistors. Thus, the mismatch error in this case would be large. However, since an error in the implementation of the least significant bits is not critical, the overall accuracy is not significantly affected. Further, since the total number of transistors in the array is significantly reduced, the overall chip area is much reduced. By programming the connection of the coefficient transistors array, we can obtain the required coefficient values. For example, if we want a coefficient value of 0.987, we connect ten largest-size transistors for the implementation of a memory transistor, and nine largest-size transistors,

eight mid-size transistors and seven smallest-size transistors for the generation of one coefficient.

In this prototype programmable SI filter design, Cell #1 designed in Chapter 3, is used for the implementation of both the memory cell as well as the voltage current converter. The logic gates from standard digital cells library are used for implementation of the overlapped clock generator.

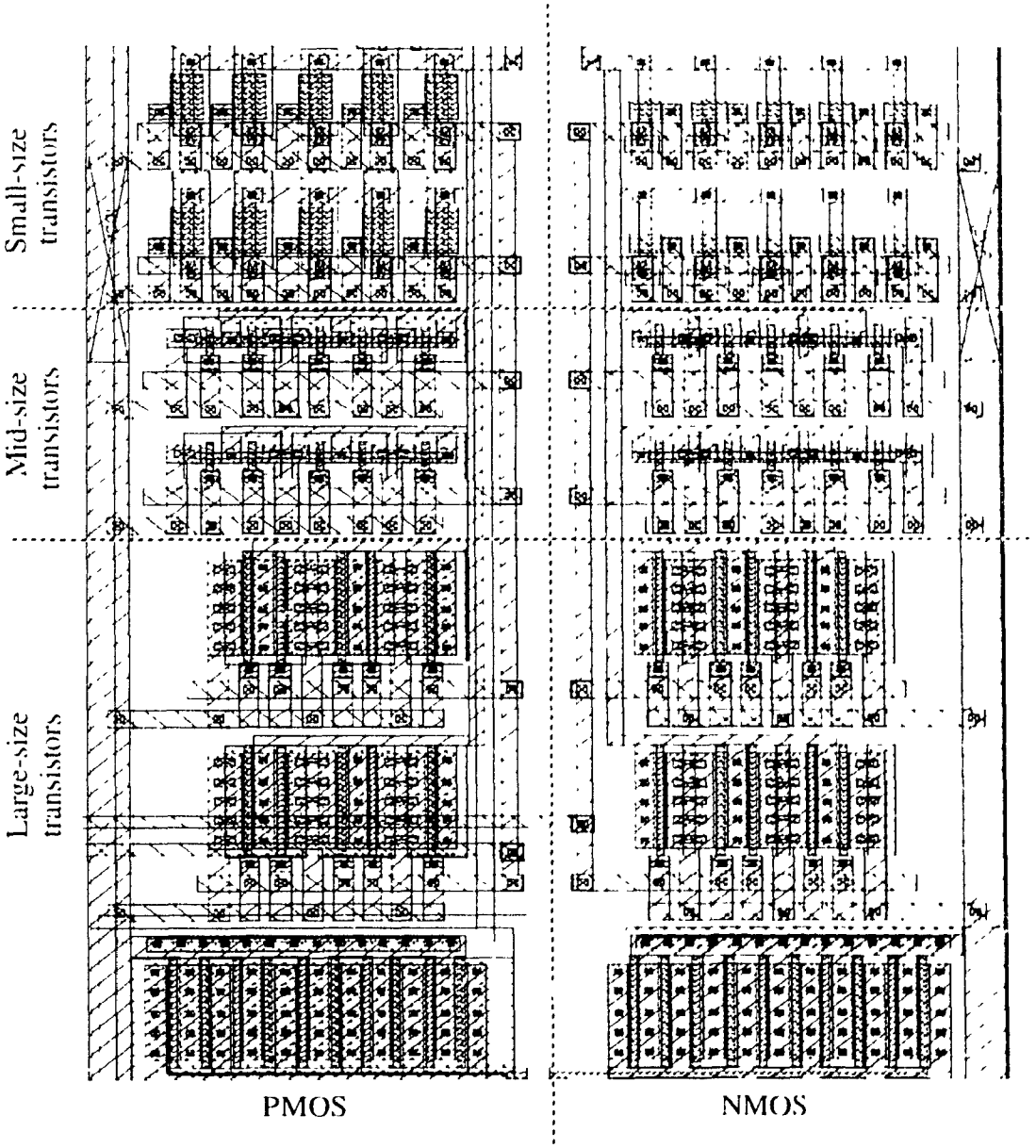


Fig. 4.12 Layout of the coefficients transistor and memory transistor array

To verify the programmability of the circuit design, an array of six second-order IIR filters is designed using the standard 1.2 μ N-well CMOS process technology. The chip layout is shown in Fig. 4.13, where the six second-order filters are marked as F1, F2, F3, F4, F5 and F6. Fig. 4.14 shows the photograph of one of the six programmable second-order SI filter cell. Hard wiring technology is used for programming the filters. For this layout, all the six filters are designed to be elliptic. Filter F1 is programmed as a first-order lowpass filter, filters F2 and F3 as second-order lowpass filters, filter F4 as a first-order highpass filter, and filters F5 and F6 as second-order highpass filters. The coefficient values used in programming the six filters are given in Table 4.2. The coefficients of the filters F1, F2 and F3 given in this table are obtained from the fifth-order elliptical lowpass filter specifications given in Table 4.3 using MATLAB. Similarly, the coefficients of the filters F4, F5 and F6 are obtained from the fifth-order elliptic highpass filter specification given in Table 4.3.

Table 4.2 The coefficient values of the filters

Filter	a_1	a_2	b_0	b_1	b_2
F1	-0.333	0.000	0.333	0.333	0.000
F2	-0.517	0.362	0.264	0.318	0.263
F3	-0.339	0.787	0.572	0.310	0.572
F4	-0.077	0.000	0.756	-0.756	0.000
F5	-0.461	0.318	0.500	-0.898	0.500
F6	-0.872	0.783	0.500	-0.773	0.500

Table 4.3 Specifications of fifth-order low- or high-pass filters

Filter	N	R_p	R_s	ω_n
Lowpass	5	0.03	48	3.3/16
High-pass	5	0.03	48	6/16

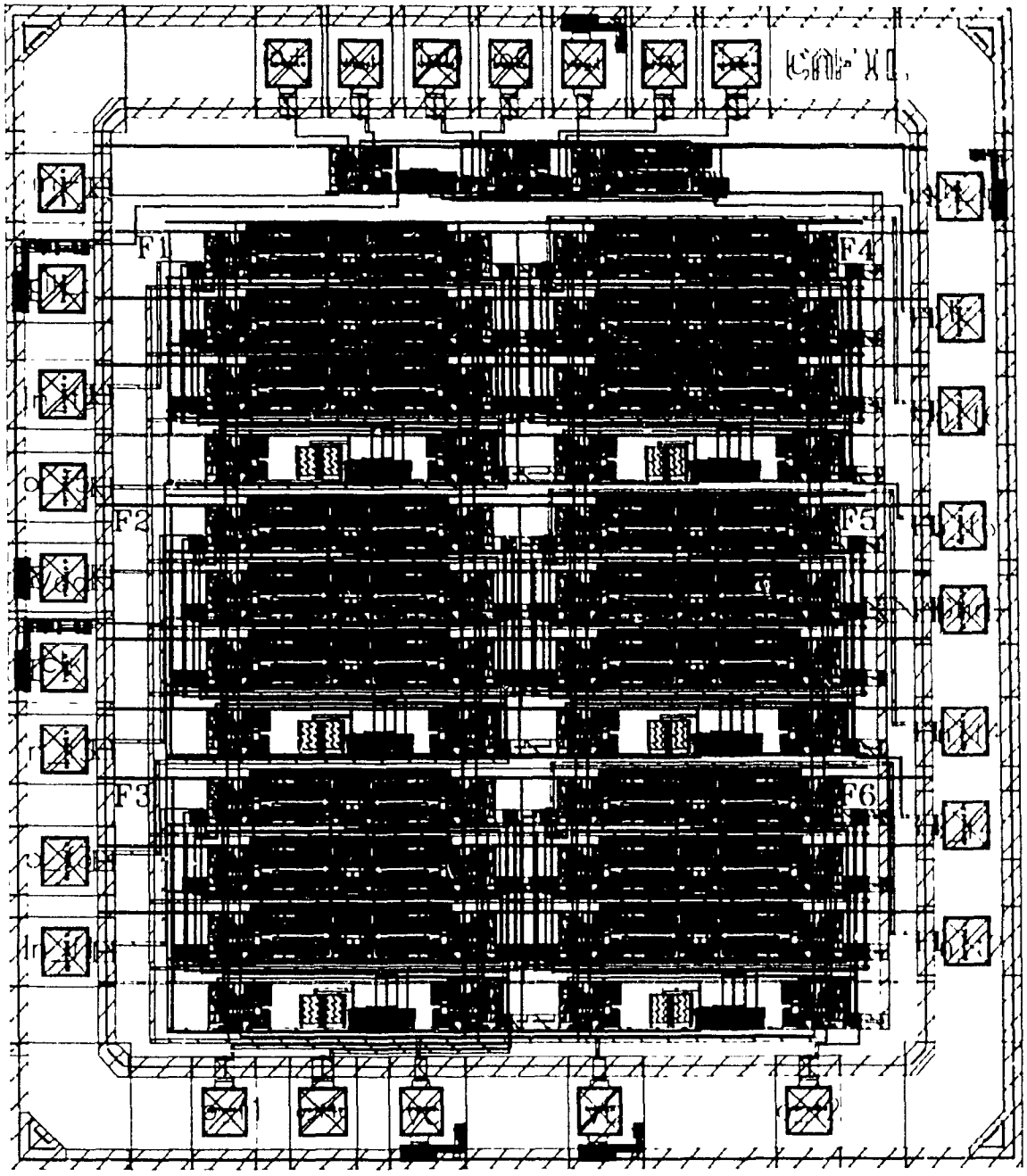


Fig. 4.13 The layout of prototype chip

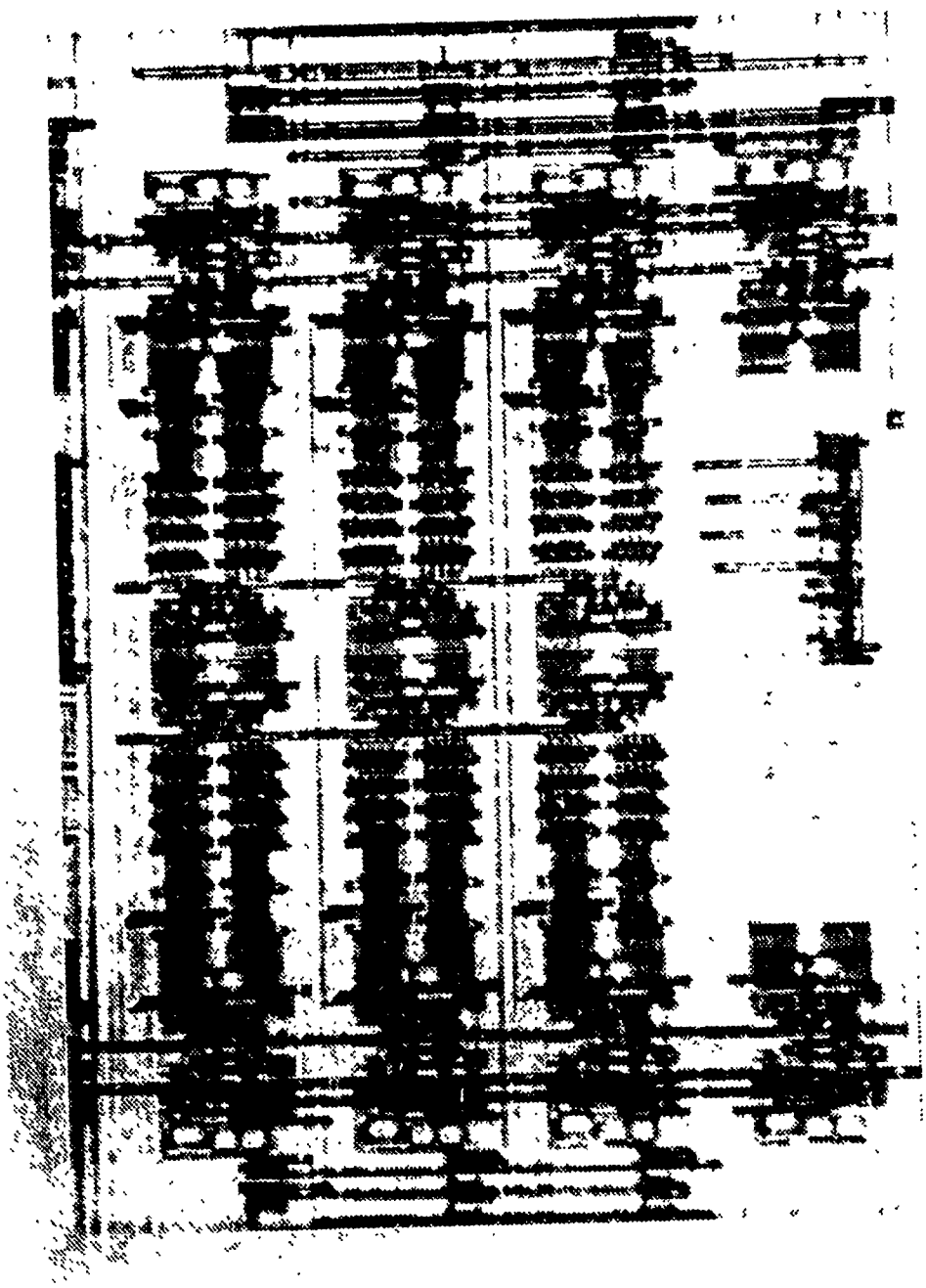


Fig. 4.14 The photograph of a programmable second-order SI filter

4.3.3 Prototype Chip Test Results

The chip containing the six designed SI filters are tested in the laboratory. Fig. 4.19 to Fig. 4.20 show the magnitude responses of the filters F1 to F6. The testing conditions are V_{dd} = 5 V, and the sampling frequency f_s = 250 KHz. The test results are given in Table 4.4. The THDs in Table 4.4 are calculated from second and third harmonic distortions. From the test results, we see that the proposed technique is quite successful in achieving the programmability of the filters and the characteristics of designed filters are close to those obtained directly from the coefficients given in Table 4.2.

Table 4.4 Test results of filters F1 to F6 with V_{dd} = 5 V and f_s = 250 KHz

Parameters	Value
-3 dB cutoff frequency (F1)	45 KHz
THD (F1)	-40.2 dB
-3 dB cutoff frequency (F2)	63.7 KHz
THD F(2)	40.2 dB
-3 dB cutoff frequency (F3)	53.5 KHz
THD (F3)	40.3 dB
-3 dB cutoff frequency (F4)	33.7 KHz
THD (F4)	40.2 dB
-3 dB cutoff frequency (F5)	36.7 KHz
THD (F5)	-40.4 dB
-3 dB cutoff frequency (F6)	46.3 KHz
THD (F6)	- 41.6 dB
Chip power dissipation	257.5 mW
Size of filter cell	1.39 mm^2

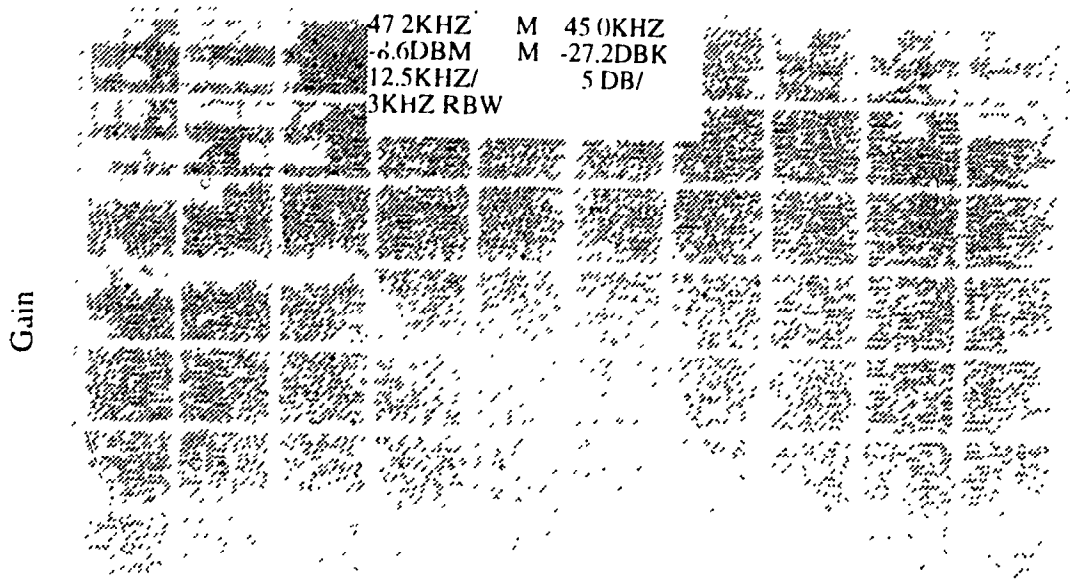


Fig. 4.15 Magnitude frequency response of filter F1 (V_{dd} = 5 V and f_s = 250 KHz)

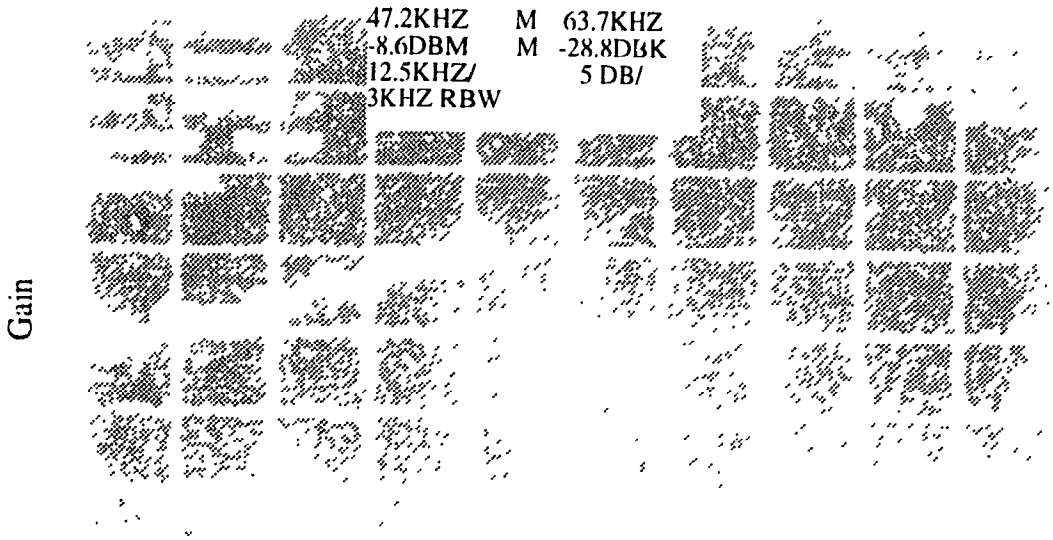


Fig. 4.16 Magnitude frequency response of filter F2 (V_{dd} = 5 V and f_s = 250 KHz)

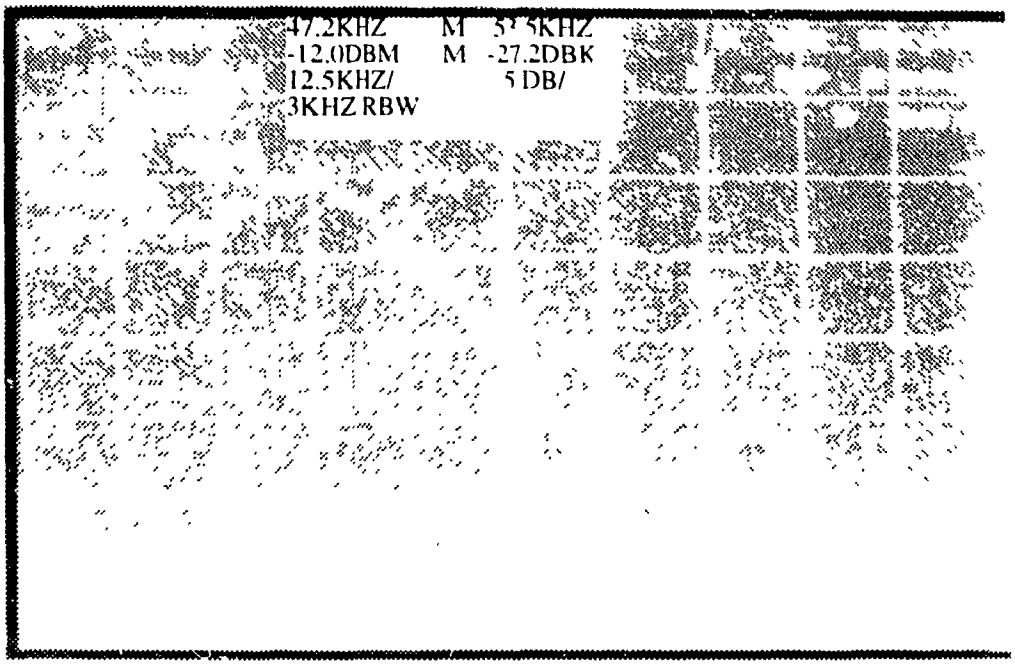


Fig. 4.17 Magnitude frequency response of filter F3 (V_{dd} = 5 V and f_s = 250 KHz)

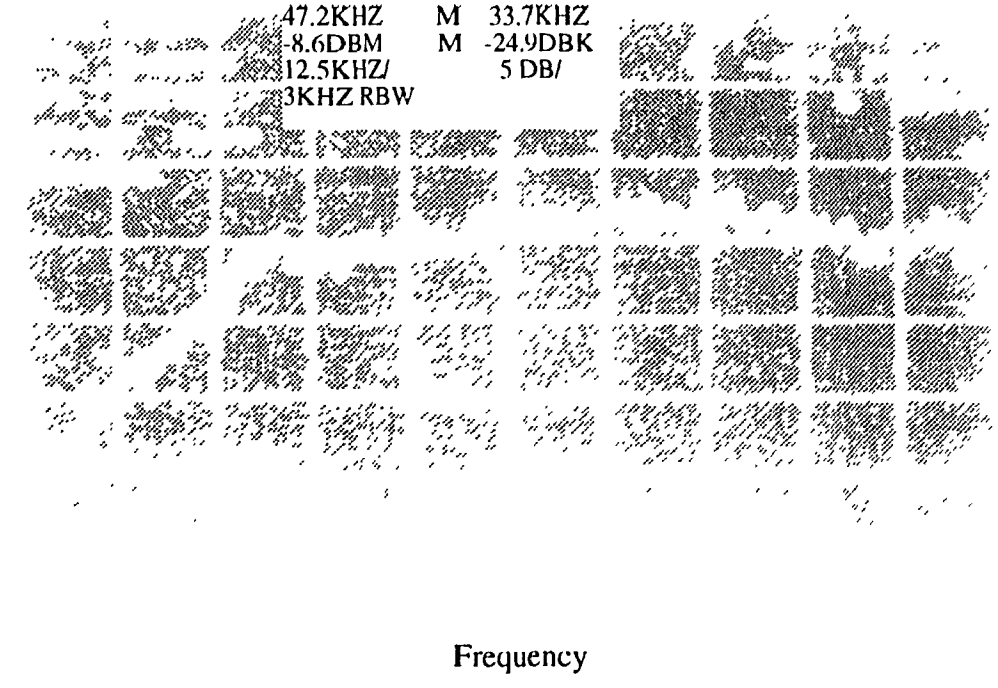


Fig. 4.18 Magnitude frequency response of filter F4 (V_{dd} = 5 V and f_s = 250 KHz)

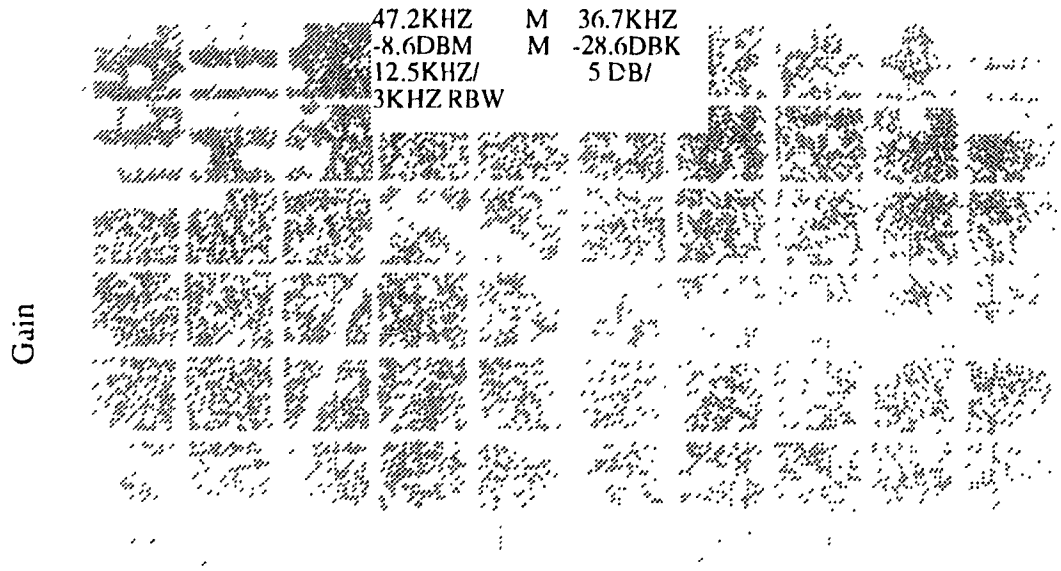


Fig. 4.19 Magnitude frequency response of filter F5 (V_{dd} = 5 V and f_s = 250 KHz)

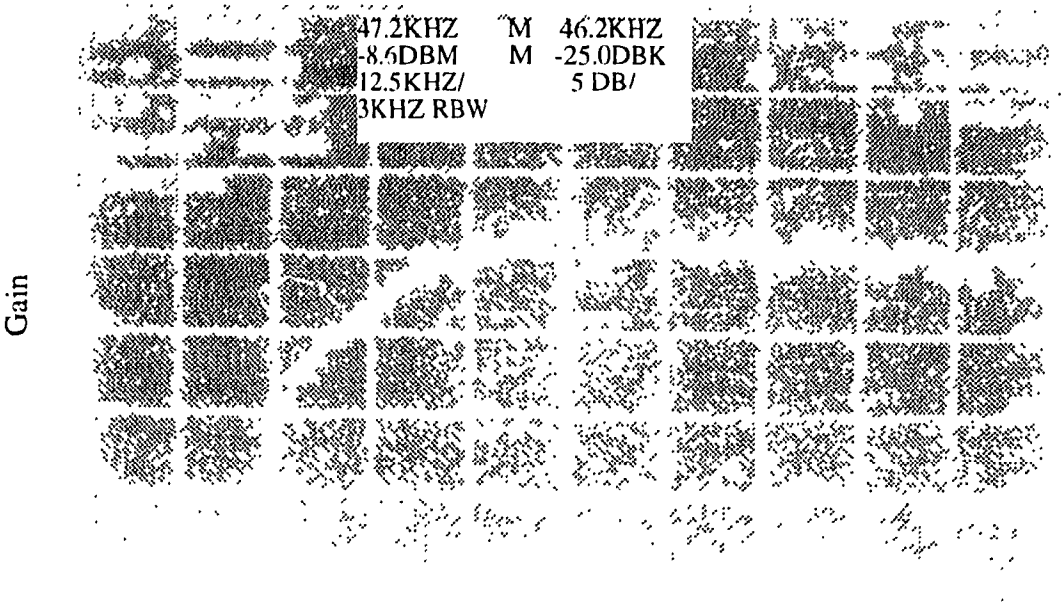


Fig. 4.20 Magnitude frequency response of filter F6 (V_{dd} = 5 V and f_s = 250 KHz)

By cascading the filters from the array, higher-order filters are obtained. Fig. 4.21 to Fig. 4.23 show the magnitude frequency response of the higher-order filters and Table 4.5 lists the test results. The performance of each these filters satisfy the given specifications, except that the attenuation of about -25 dB of the cascaded filter differs from the -48 dB value in the given specification. However, this discrepancy could be due to the parasitic capacitors and resistors of the external connections introduced because of the test circuits.

Table 4.5 Test results of higher-order filters with V_{dd} = 5 V and f_s = 250 KHz

Parameters	Value
-3 dB cutoff frequency (5th-order high pass)	43.5 KHz
THD (5th-order high pass)	-45.2 dB
-3 dB cutoff frequency (5th-order low pass)	51.7 KHz
THD (5th-order low pass)	-39.9 dB
-3 dB cutoff frequency (10th-order band pass)	43.2 KHz, 56.2 KHz
THD (10th-order band pass)	-55.7 dB

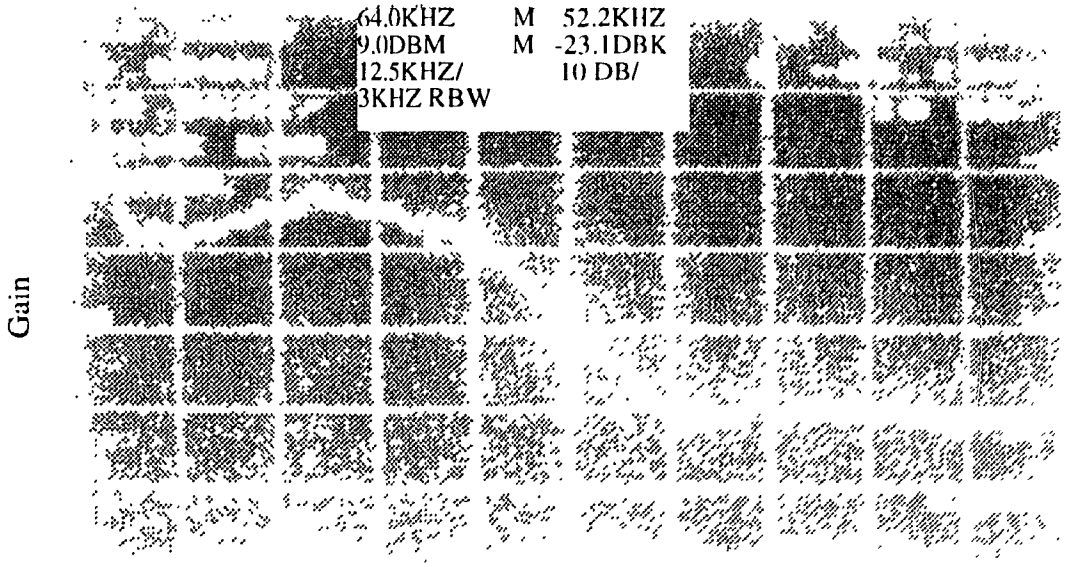


Fig. 4.21 Magnitude frequency response of the 5th-order lowpass filter obtained from the cascade of F1, F2 and F3 (V_{dd} = 5 V and f_s = 250 KHz)

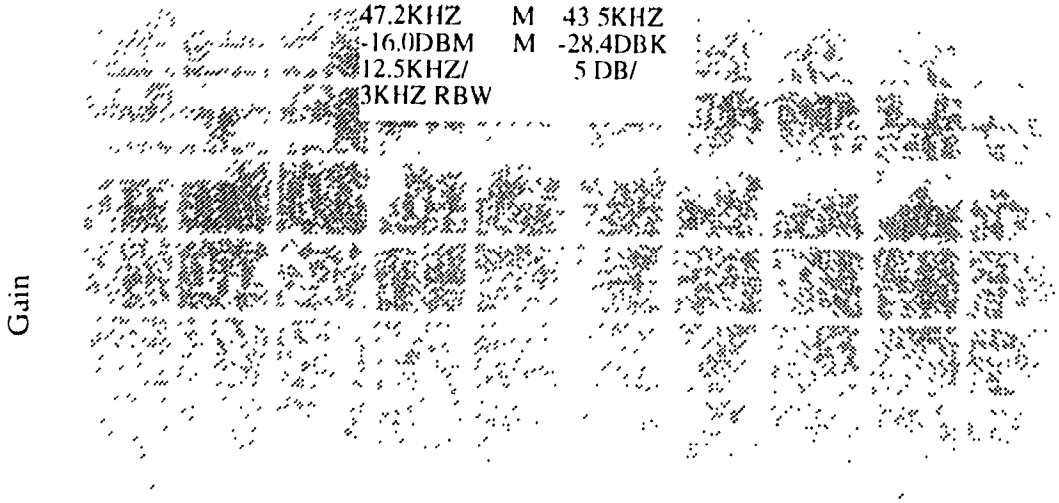


Fig. 4.22 Magnitude frequency response of the 5th-order highpass filter obtained from the cascade of F4, F5 and F6 (V_{dd} = 5 V and f_s = 250 KHz)

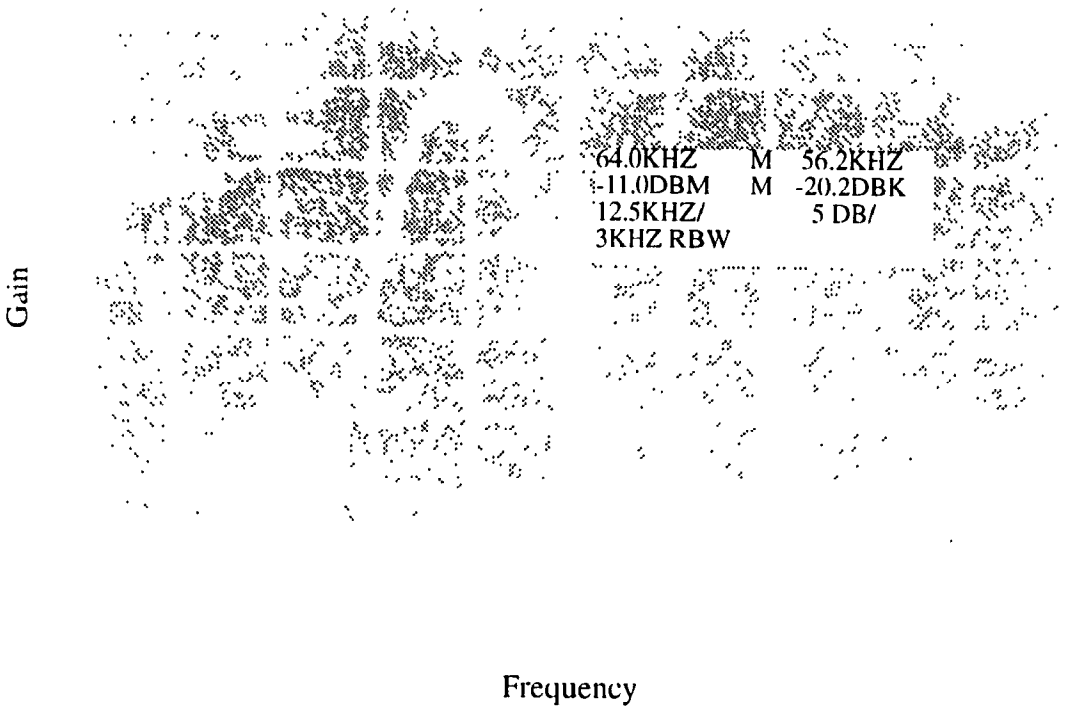


Fig. 4.23 Magnitude frequency response of the 10th-order bandpass filter obtained from the cascade of F1 to F6 (V_{dd} = 5 V and f_s = 250 KHz)

To investigate the low-power supply voltage performance, the filters were tested with a supply voltage of V_{dd} = 3.3 V. Fig. 4.24 and Fig. 4.25 give the magnitude frequency response of the filters F3 and F6, and Table 4.6 lists the test results. Comparing the test results listed in Table 4.5 and Table 4.6, it is seen that the THD and the passband ripple of the filters are increased when power supply voltage is reduced. However, the stopband attenuation and bandwidth are maintained remain roughly the same. The power dissipation is much reduced.

Table 4.6 Test results of the filters with V_{dd} = 3.3 V and f_s = 250 KHz

Parameters	Value
-3 dB cutoff frequency (F3)	52 KHz
THD (F3)	-38.2 dB
-3 dB cutoff frequency (F6)	46.2 KHz
THD (F6)	-31.0 dB
Power Dissipation	31.5 mA

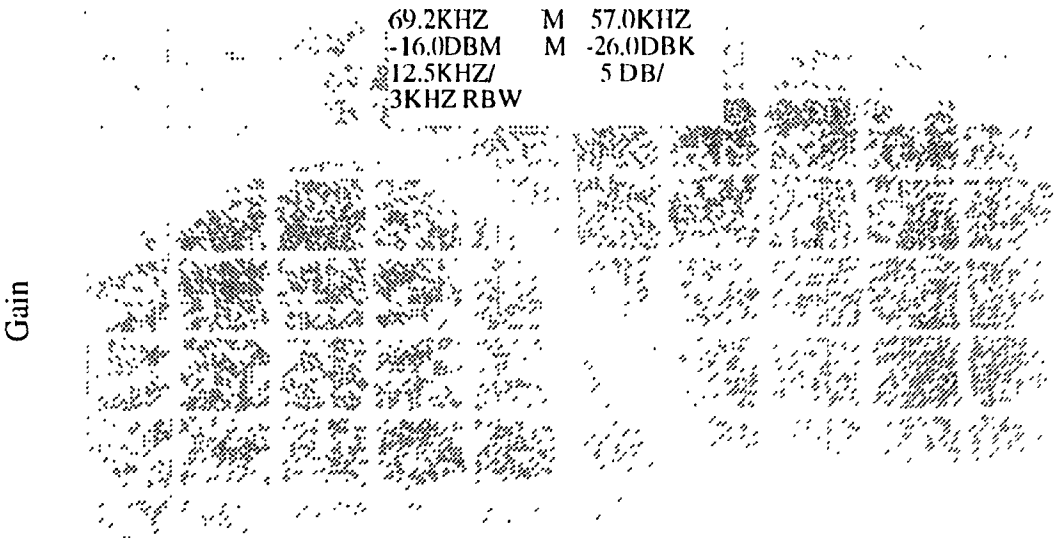


Fig. 4.24 Magnitude frequency response of filter F3 (V_{dd} = 3.3 V and f_s = 250 KHz)

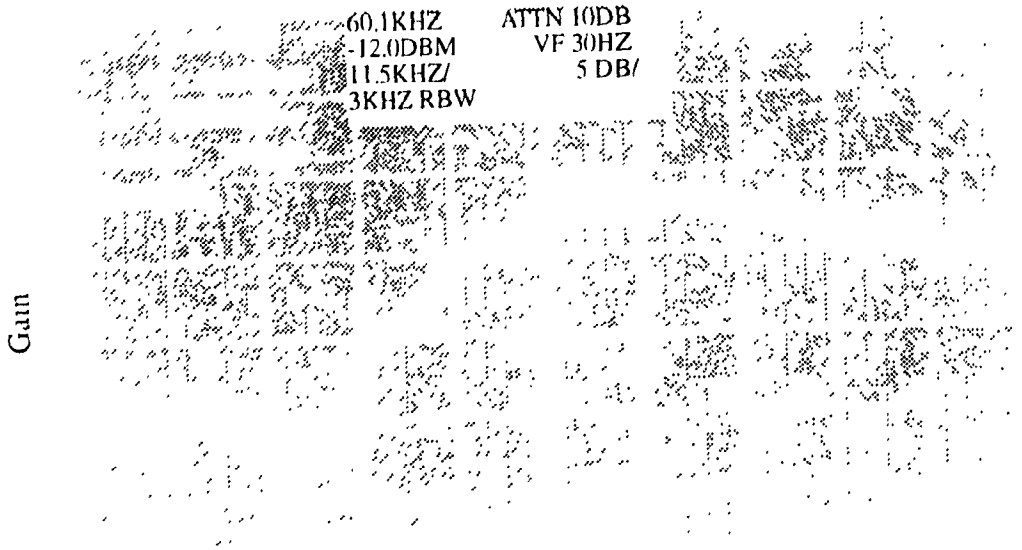


Fig. 4.25 Magnitude frequency response of filter F6 (V_{dd} = 3.3 V and f_s = 250 KHz)

To test the high-frequency performance, the sampling frequency was increased from 250 KHz to 500 KHz, and the filters were tested again. Fig. 4.26 and Fig. 4.27 show the magnitude frequency responses of filters F3 and F6. Table 4.7 lists the test results. It seen that when the sampling frequency increased, the THDs become larger and the performance gets worse because of the increase in settling time error.

Table 4.7 Test results of the filters with V_{dd} = 5 V and f_s = 500 KHz

Parameters	Values
-3 dB cutoff frequency (F3)	80 KHz
THD (F3)	-34.5 dB
-3 dB cutoff frequency (F6)	75 KHz
THD (F6)	-29.4 dB

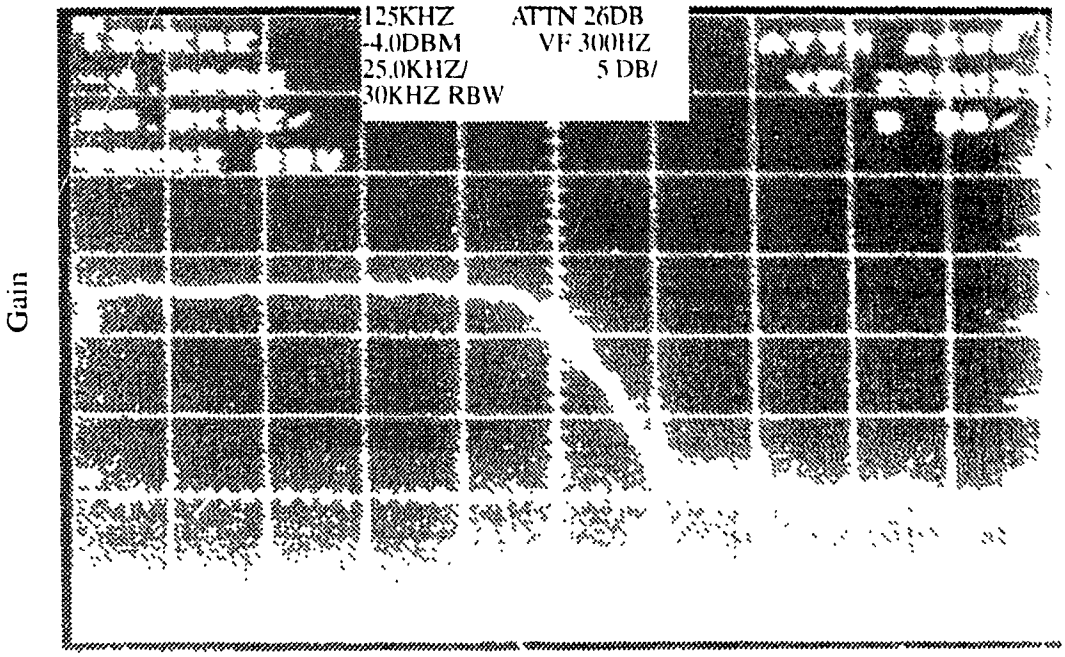


Fig. 4.26 Magnitude frequency response of filter F3 (V_{dd} = 5 V and f_s = 500 KHz)

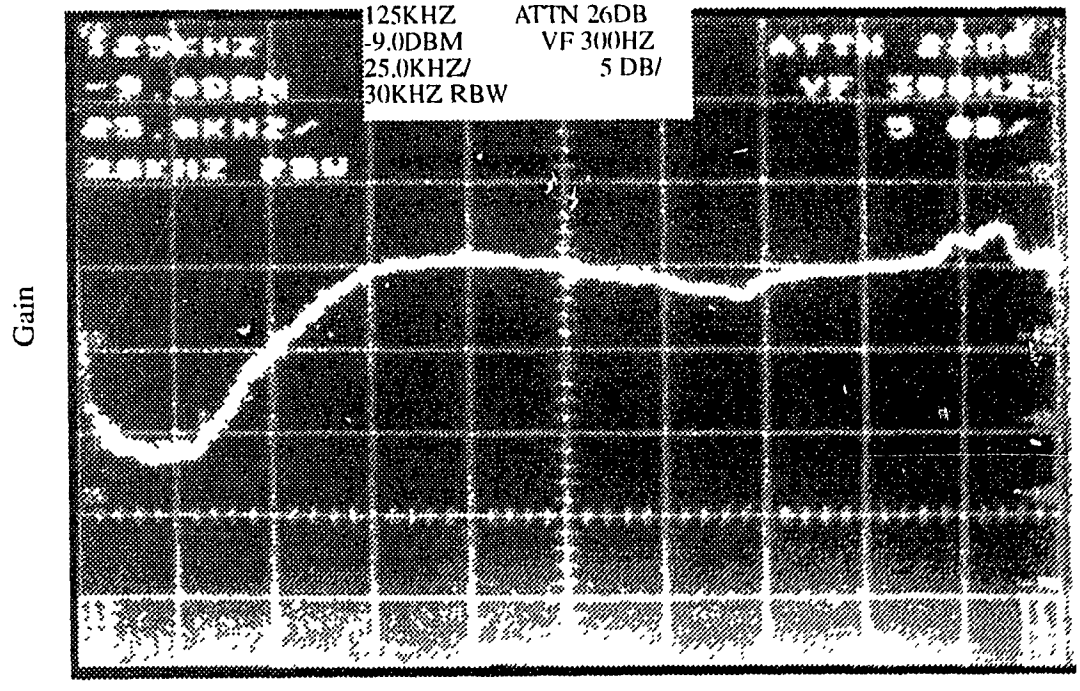


Fig. 4.27 Magnitude frequency response of filter F6 (V_{dd} = 5 V and f_s = 500 KHz)

4.4 Summary

A programmable SI filter design technique has been described. The design technique relies on digital filter synthesis techniques for obtaining the filter structure as well as the SI circuits. The coefficients of the transfer function are matched to the coefficient transistors of the filter directly. By just changing the size ratios of the coefficient transistors, different frequency characteristics of the filters can be obtained, thus making the filters easily programmable. For the implementation of the multiplier coefficients, an array consisting of transistors with three different sizes is designed instead of using a unit transistor array. Use of different size transistors in the transistor array reduces the area of the chip efficiently, while maintaining the accuracy of the most significant bits.

A prototype chip with six second-order programmable filters has been designed and fabricated using the 1.2 μ N-well CMOS process technology. The test results prove the effectiveness and feasibility of the methodology in designing SI programmable filters. The performance of the filters also benefits from the use of the high-performance differential SI memory cell (DMC-I) designed in Chapter 3.

Chapter 5

SI RATIO-INDEPENDENT ALGORITHMIC D/A AND A/D CONVERTERS

In signal processing systems, digital-to-analog (D/A) and a analog-to digital (A/D) converters are often key building blocks. For development of a high performance D/A or A/D converter, some special process technologies are necessary. In weighted network D/A and A/D converters, because of the requirement of matching of the components to an accuracy comparable to the linearity of the conversion, trimming techniques using laser [32], zener zapping [33], dynamic element matching [34], or digital method of self calibration [35], [36] are used to obtain the matched components. Although these trimming techniques yield components matched to an extremely high precision, they have the disadvantages of requiring an excessively large area for the placement of the components to be trimmed, large capacitors for the dynamic element matching, or extra calibration cycles and a fairly large area for a sub-D/A converter using RAM or ROM for self-calibration.

To overcome the trimming problem, some D/A and A/D converters design techniques (ratio independent algorithmic D/A and A/D converters, Σ-Δ modulator) which usually employ SC circuits have been developed [36], [37], [38], [39]. In these techniques the double poly process is required for realizing linear capacitors. As mentioned previously, the SC circuits are not compatible with the standard digital VLSI process technology and

their performance is affected by the low supply voltages. Therefore, these D/A and A/D converter design techniques are not very suitable for mixed-mode VLSI implementation.

In [14], a current mode Σ-Δ modulator has been introduced. Since Σ-Δ modulation is based on oversampling of the analog signal, the requirement of accuracy in the analog circuit is much reduced. However, to achieve a high-accuracy high-resolution data conversion, the oversampling ratio has to be increased or higher order Σ-Δ modulator has to be used. An increase in the oversampling ratio means an increase in the sampling frequency. This limits the frequency bandwidth of the analog circuit. When the order of the Σ-Δ modulator is increased to more than two, the stability determination becomes a complicated problem due to the complexity of the circuit [41]. In [16], a new SI approach for A/D converter design has been presented. It is capable of achieving high accuracy data conversion without requiring any special process technology. However, the accuracy of the converter is limited by the switch charge injection.

In this chapter, a new SI ratio-independent algorithmic D/A converter design technique [15] is presented. This technique has an advantage over the SC ratio-independent algorithmic D/A converter design technique [37] in achieving a high speed conversion and not requiring linear capacitors. A new SI ratio-independent algorithmic A/D converter circuit is also presented in this chapter. The theoretical analysis results of the conversion errors of the proposed D/A and A/D converters are carried out. The proposed design techniques have the advantage of reducing the effect of switch charge injection in comparison with the technique introduced in [16].

Using the proposed D/A converter design technique, a practical converter is designed and simulated. The converter is implemented using 1.2 μ N-well CMOS process technology. The test results of the prototype chip are also included in this chapter.

5.1 D/A Converter Design Technique

In this Section, we present a new SI ratio-independent algorithmic D/A converter design technique. First, the principle of an algorithmic multiplication D/A converter is presented. Then, this principle is used in developing a SI ratio-independent algorithmic D/A converter design technique. Finally, a theoretical analysis for the conversion error of proposed D/A converter is carried out.

5.1.1 Principle of Algorithmic Multiplication D/A Conversion

The algorithmic converter, also known as the cyclic converter, is superior in terms of circuit simplicity and requiring fewer highly accurate components as compared with other types of D/A converters. A block diagram of the algorithmic multiplication D/A converter is shown in Fig. 5.1 The converter consist of a multiply-by-two amplifier (2x), a sample and hold (S/H) circuit, a reference sum circuit, and two switches (S_1 and S_2). The switch S_1 is controlled by the input digital data.

The conversion operation starts in the first cycle with S_2 open. If the first digital bit is '1', S_1 is connected to the reference voltage V_{ref}. The S/H circuit samples and holds V_{ref}

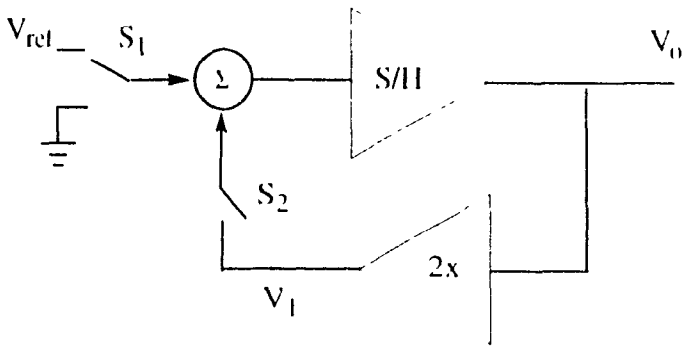


Fig. 5.1 The block diagram of the algorithmic multiplication D/A converter

which is then multiplied by two by the 2x amplifier. Thus, V_o equals to V_{ref} and V_1 equals to $2V_{ref}$. If the first bit is '0', S_1 is connected to the ground, and V_o becomes zero. From the second cycle to the nth cycle, S_2 is always closed, and S_1 is connected to V_{ref} or ground depending on the state of the corresponding input bit. The signal from S_1 and V_1 are added by the summer and sampled and held by the S/H circuit. The 2x amplifier doubles the signal at the end of each cycle. In other words, in the cyclic multiplication D/A conversion, during each cycle the previous conversion voltage doubles and is added to the reference voltage or the ground voltage. The algorithm of the cyclic multiplication D/A converter, therefore, is given by

$$V_o(1) = b_1 V_{ref} \qquad \text{(EQ 5.1)}$$

$$V_o(i) = 2V_o(i-1) + b_i V_{ref}, \qquad i = 2, \ldots, n. \qquad \text{(EQ 5.2)}$$

where b_i = '0' or '1' is the ith bit of the n-bit digital data. This operation is repeated from the MSB to the LSB. After n cycles are completed, (EQ 5.1) and (EQ 5.2) yield the converted voltage as

$$V_o(n) = V_{ref} \sum_{k=1}^{n} 2^{k-1} b_k \qquad \text{(EQ 5.3)}$$

This equation shows that an n-bit digital data is converted into an analog voltage V_o in the range from 0 to $(2^n - 1)V_{ref}$.

From the previous discussion, it is apparent that the accuracy of the cyclic multiplication D/A converter is determined mainly by the accuracy of the gain of the multiply-by-two amplifier. A gain of two for the 2x amplifier is necessary and it can be realized by using a ratio-independent multiplication structure.

5.1.2 SI Ratio-Independent Algorithmic D/A Converter Design Technique

In Section 5.1.1, the principle of the operation of an algorithmic multiplication D/A converter has been described in the voltage mode. For the SI circuit design of an algorithmic D/A converter, we shall first change the reference voltage V_{ref} to a reference current I_{ref}, then use the SI memory cell to replace the voltage sample and hold circuit (S/H). For implementing the function of the ratio-independent multiplication function, we need two more SI memory cells. Fig. 5.2 shows the resulting circuit of the proposed D/A converter. The converter consists of three simple SI memory cells (T_1, T_2 and T_3) and several switches. Fig. 5.3 gives the switch-controlling waveforms.

- *Ratio-Independent Multiplication Operation*

The circuit given in Fig. 5.2 can perform the function of ratio independent multiplication. The operation is started at clock cycle 1. The the switches S_1 and S_2 are closed during this clock cycle, the reference current I_{ref} is sampled and held by T_1, and the current stored in T_1 becomes $I_1 = J + I_{ref}$. Next, switches S_3 and S_4 are closed during the clock cycle 2. The memory transistor T_1 outputs the current I_{ref} to T_2 which in turn samples and holds this current, giving $I_2 = J - I_{ref}$. During the clock cycle 3, switches S_5 and S_6 are closed and the output of T_1 is switched to T_3, giving $I_3 = J - I_{ref}$. During the clock cycle 4, switches S_2, S_4 and S_6 are closed. Both T_2 and T_3 feed the current I_{ref} back to T_1, and T_1 samples and holds the sum of the current from T_2 and T_3. Assuming that the switches S_4 and S_6, and memory transistors T_1, T_2 and T_3 are ideal, the current stored in T_1 becomes $I_1 = J + 2I_{ref}$. That is, the reference current I_{ref} is multiplied by two, and this multiplication is independent of the ratio of the transistors T_1 and T_2, or of the transistors T_1 and T_3. The current $2I_{ref}$ is output to T_2 and T_3 again in the next two clock cycles, and is doubled in the seventh clock cycle in T_1. This process continues and after $3n$ clock cycles, the current I_{ref} will be multiplied by 2^{n-1}. Each multiplication operation takes three clock cycles.

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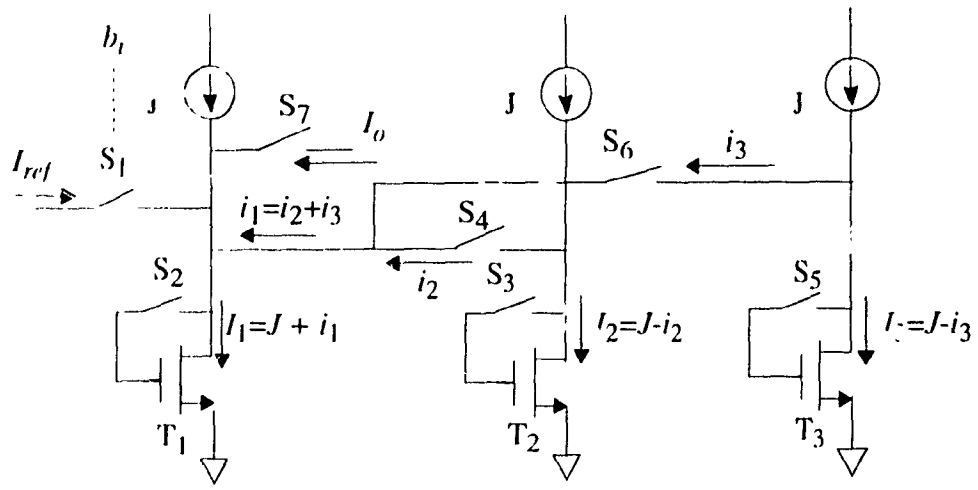
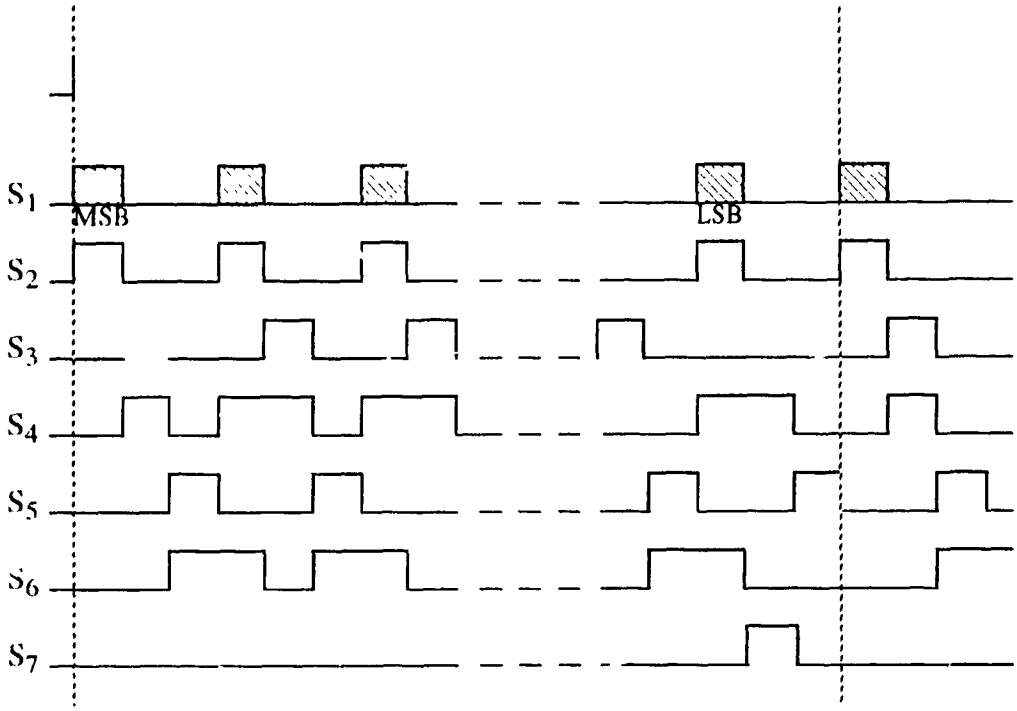


Fig. 5.2 A SI ratio-independent algorithmic D/A converter using the simple memory cells



- *Ratio-Independent Cyclic D/A Conversion*

During the ratio-independent multiplication operation, switch S_1 is always opened except during the clock cycle 1. If we control S_1 to be closed or opened depending on the state of the corresponding digital bit, the circuit will perform the D/A conversion. The operation of D/A conversion is as follows. During the first conversion cycle (one conversion cycle contains three clock cycles), if the most significant bit b_1 is '1', switch S_1 is closed in the clock cycle 1, and the current I_{ref} is sampled and held by T_1. On the other hand, if b_1 is '0', S_1 is opened, and I_{ref} is not sampled and held by T_1. The current stored in T_1 can be expressed as

$$I_1(1) = J + b_1 I_{ref} = J + i_1(1) \qquad \text{(EQ 5.4)}$$

The signal $b_1 I_{ref}$ is doubled after the next two clock cycles. During the second conversion cycle, if the second most significant bit b_2 is '1', S_1 is closed, and if b_2 is '0', S_1 is opened. Therefore, the signal $b_2 I_{ref}$ is added to the signal $2b_1 I_{ref}$. Thus, I_1 becomes

$$I_1(2) = J + 2b_1 I_{ref} + b_2 I_{ref} = J + i_1(2) \qquad \text{(EQ 5.5)}$$

Obviously, this operation is the same as the D/A conversion described in Section 5.1.1. In the circuit given in Fig. 5.2, during each conversion cycle, the previous conversion current gets doubled and added to the reference current or zero current. After n conversion cycles, the current stored in T_1 is given by

$$I_1(n) = J_1 + I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k \qquad \text{(EQ 5.6)}$$

The output current of the circuit, therefore, can be expressed as

$$I_o(n) = I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k \qquad \text{(EQ 5.7)}$$

5.1.3 D/A Conversion Error Analysis

The expression for the output current as given in (EQ 5.7) has been obtained based on the assumption that the switches and the memory cells are ideal. In practice, the output resistance of a switched-current memory cell is finite, switch closure resistance is never zero, and there exists a switch charge injection associated with each switch. In this section, we will discuss the effects of these non-ideal characteristics.

- *Effect of Finite Impedance of SI Memory Cell*

As discussed in Chapter 3, the finite impedance problem in a SI memory cell is caused by the channel length modulation which produces an error in the output current. This current error affects the data conversion accuracy. We will now analyze the effect of the finite impedance problem. Fig. 5.4 illustrates the effect of finite impedance problem when the current is transferred from T_1 to T_2.

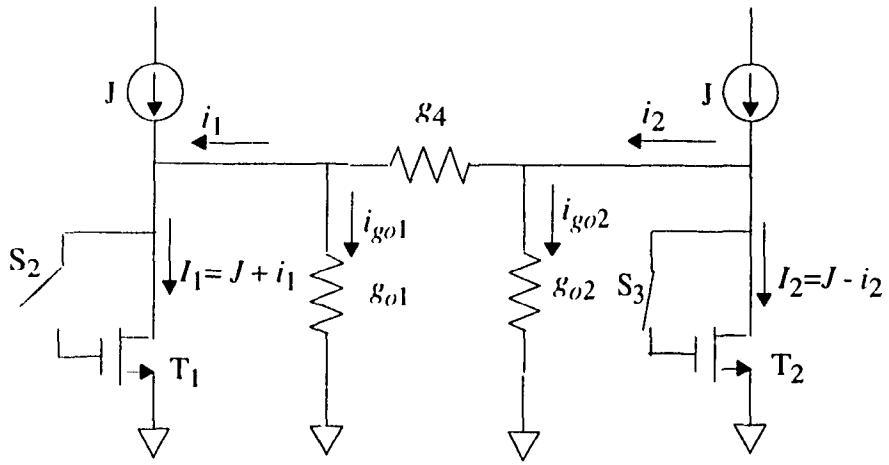


Fig. 5.4 An illustration of the effect of finite impedance problem when the current is transferred from T_1 to T_2

During the first conversion cycle, T_1 first samples and holds the reference current and then transfers it to T_2 and T_3. Thus, from (EQ 5.4), we have

$$i_1(1) = I_{ref} b_1 , \tag{EQ 5.8}$$

and from (EQ. 2.18), we have

$$i_2(1) = \frac{G_{m2}}{G_{m2}+G_{12}} i_1(1) , \tag{EQ 5.9}$$

where $G_{m2} = g_{m2}g_4$, g_{m2} is the transconductance of T_2, and $G_{12} = (g_{o1}+g_{o2})g_4 + g_{o1}g_{m2}$. In the same way we can obtain $i_3(1)$, the current transferred from T_1 to T_3, as

$$i_3(1) = \frac{G_{m3}}{G_{m3}+G_{13}} i_1(1) , \tag{EQ 5.10}$$

where $G_{m3} = g_{m3}g_4$, g_{m3} is the transconductance of T_3, and $G_{13} = (g_{o1}+g_{o3})g_6 + g_{o1}g_{m3}$. During the second conversion cycle, as illustrated in Fig. 5.5, the current stored in the memory transistors T_2 and T_3 are transferred back to T_1, and we have

$$i_1(2) = I_{ref} b_2 + \frac{G_{m12}}{G_{m12}+G_{21}} i_2(1) + \frac{G_{m13}}{G_{m13}+G_{31}} i_3(1), \tag{EQ 5.11}$$

where $G_{m12} = g_{m1}g_4$, $G_{m13} = g_{o1}g_6$, $G_{21} = (g_{o1}+g_{o2})g_4 + g_{o2}g_{m1}$, and $G_{31} = (g_{o1}+g_{o3})g_6 + g_{o3}g_{m1}$. Using (EQ 5.8), (EQ 5.9) and (EQ 5.10) in (EQ 5.11), we have

$$i_1(2) = I_{ref} b_2 + \frac{G_{m12}G_{m2}}{(G_{m12}+G_{21})(G_{m2}+G_{12})} I_{ref} b_1$$

$$+ \frac{G_{m13}G_{m3}}{(G_{m13}+G_{31})(G_{m3}+G_{13})} I_{ref} b_1 \tag{EQ 5.12}$$

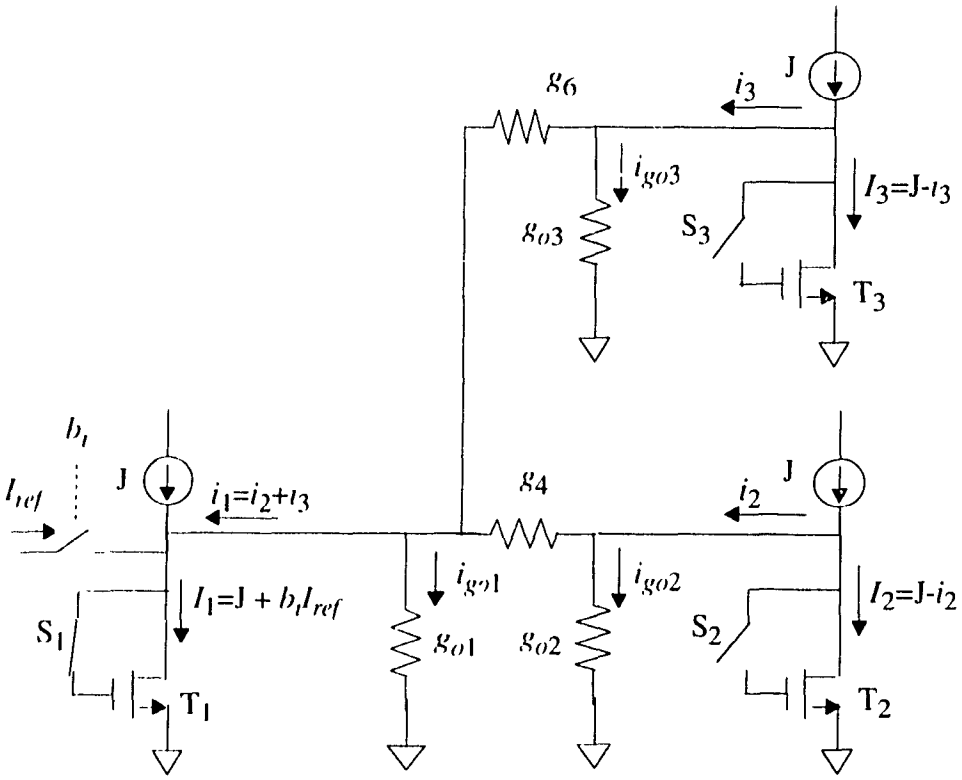


Fig. 5.5 An illustration of the effect of finite impedance problem when the current is transferred from T_2 and T_3 to T_1

Assuming that $G_{m12} = G_{m13} = G_{m2} = G_{m3} = G_m$, and $G_{12} = G_{13} = G_{21} = G_{31} = G$, we can rewrite (EQ 5.12) as

$$i_1(2) = I_{ref} b_2 + \frac{2G_m^2}{(G_m + G)^2} I_{ref} b_1 \qquad \text{(EQ 5.13)}$$

Continuing in this manner, after the nth conversion cycle, the current $i_1(n)$ is given by

$$i_1(n) = I_{ref} \sum_{k=1}^{n} \left(\frac{2G_m^2}{(G_m + G)^2} \right)^{k-1} b_k \qquad \text{(EQ 5.14)}$$

In a practical circuit, since $G_m >> G$, (EQ 5.14) can be simplified as

$$i_1(n) \approx I_{ref} \sum_{k=1}^{n} 2^{k-1} \left(1 - \frac{G}{G_m}\right)^{k-1} b_k \qquad \text{(EQ 5.15)}$$

Expanding $(1 - G/G_m)^{k-1}$, and ignoring the second- and higher-order terms, we have

$$i_1(n) \approx I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k + \frac{I_{ref} G}{G_m} \sum_{k=1}^{n} 2^{k-1} b_k + \left(-\frac{I_{ref} G}{G_m}\right) \sum_{k=1}^{n} 2^{k-1} k b_k \qquad \text{(EQ 5.16)}$$

Since the output current $I_o = i_1$, we have

$$I_o(n) = i_1(n) = I_{oideal} + i_{eg} - i_{en} , \qquad \text{(EQ 5.17)}$$

where

$$I_{oiedeal} = I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k , \qquad \text{(EQ 5.18)}$$

$$I_{eg} = \frac{I_{ref} G}{g_m} \sum_{k=1}^{n} 2^{k-1} b_k , \qquad \text{(EQ 5.19)}$$

and

$$I_{en} = \left(-\frac{I_{ref} G}{g_m}\right) \sum_{k=1}^{n} 2^{k-1} k b_k \qquad \text{(EQ 5.20)}$$

In (EQ 5.17), I_{oideal} represents the ideal output current, I_{eg} represents the gain error current, and I_{en} represents the nonlinearity error current. It is seen that the finite impedance of the switched-current memory produces gain and the nonlinearity errors. However, the errors can reduced by increasing the gain of the memory cell.

- *Effect of Switch Charge Injection*

As shown in Section 2.5.2, the switch charge injection produces an error in the gate voltage which causes the output current to have an offset error (signal-independent error), a gain error, and harmonic distortions (signal-dependent error) in a SI memory cell. We now analyze the effect of these errors on the accuracy of the data conversion.

Fig. 5.6 illustrates the effect of the current error in data conversion. Assuming that the switch charge injection causes a current error I_j, the output current of the memory cell, as each time the SI memory cell changes from the sample mode to the hold mode, is given by

$$i_k' = i_k + I_{jk} , \quad k = 1, 2, 3 , \qquad \text{(EQ 5.21)}$$

where i_k is the output current of the memory cell T_k, and I_{jk} is the error current created by the switch charge injection in the memory cell T.

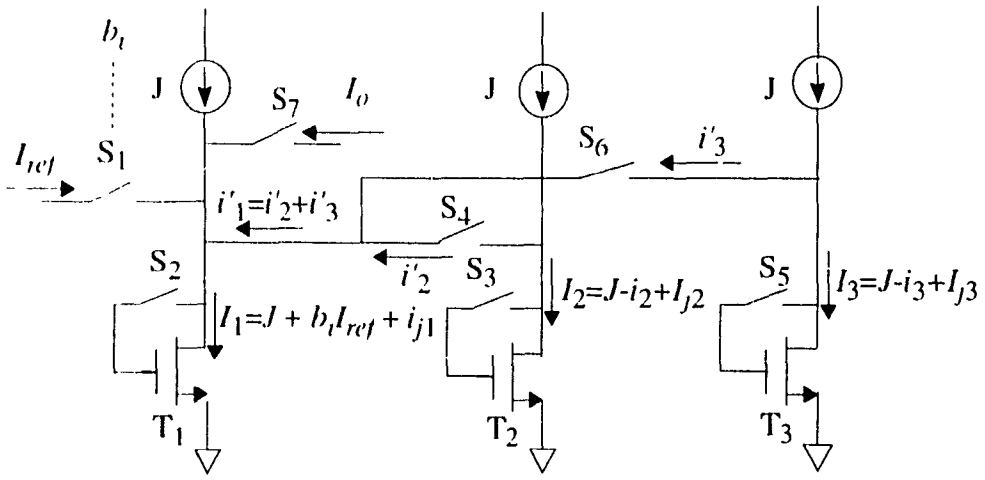


Fig. 5.6 An illustration of the switch charge injection effect

Including the effect of switch charge injection, the current i'_1 during the first conversion cycle can be expressed as

$$i'_1(1) = b_1 I_{ref} + I_{j1} \qquad \text{(EQ 5.22)}$$

The current i'_1 is transferred to T_2 and T_3 during this conversion cycle, giving

$$i'_2(1) = i'_1(1) - I_{j2} = b_1 I_{ref} + I_{j1} - I_{j2} \qquad \text{(EQ 5.23)}$$

$$i'_3(1) = i'_1(1) - I_{j3} = b_1 I_{ref} + I_{j1} - I_{j3} \qquad \text{(EQ 5.24)}$$

During the second conversion cycle, i'_1 is given by

$$i'_1(2) = b_2 I_{ref} + i'_2(2) + i'_3(2) \qquad \text{(EQ 5.25)}$$

Substituting (EQ 5.23) and (EQ 5.24) into (EQ 5.25), we have

$$i'_1(2) = b_2 I_{ref} + 2(b_1 I_{ref} + I_{j1}) - I_{j2} - I_{j3} \qquad \text{(EQ 5.26)}$$

Thus, after the nth conversion cycle, i'_1 can be expressed as

$$i'_1(n) = I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k + (2^{n-1} - 1)(2I_{j1} - I_{j2} - I_{j3}) \qquad \text{(EQ 5.27)}$$

The output current, therefore, is given as

$$I_o(n) = I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k + (2^{n-1} - 1)(2I_{j1} - I_{j2} - I_{j3}) + I_{j1}$$

$$= I_{oideal} + I_{ej} \qquad \text{(EQ 5.28)}$$

where $I_{output} = \sum_{k=1}^{n} 2^{k-1} b_k$ represents the ideal output current, and $I_{ej} = (2^{n-1}-1)(2I_{j1}-I_{j2}-I_{j3}) + I_{j1}$ represents the error current created by the switch charge injection.

As seen from (EQ 5.28), the switch charge injection produces an offset current. Since the directions of the switch charge injection error currents I_{j2} and I_{j3} are complementary to the direction of the error current I_{j1}, the effect of the switch charge injection can be reduced by making switches and memory transistors of the SI memory cells to be matched.

The above analysis has assumed that the switch charge injection creates a signal-independent current error. When considering the signal-dependent current error, the effect of switch charge injection is similar to the effect of finite impedance that produces a gain error and nonlinearity conversion error.

- *settling Time Error*

When the D/A converter operates at high speed, the non-zero settling time error creates an output current error in the SI memory cell. The effect of the settling time error is the same as that of the switch charge injection current error. This current error creates an offset current, a gain error, and a nonlinearity error in the data conversion. The higher the speed, the bigger is the settling time error. Therefore, the speed of the D/A converter is limited by the settling time of the memory cells used.

5.2 A/D Converter Design Technique

The SI technique can also be used for algorithmic A/D converter design. In [16], a SI ratio-independent algorithmic A/D design technique has been introduced. However, the accuracy of the converter is limited by the switch charge injection. In this section, using the ratio-independent algorithmic design technique, we present a new SI A/D converter

circuit which uses three SI memory cells and one comparator. It is shown that the effect of switch charge injection can be reduced by making the memory cells matched. The principle of an algorithmic A/D converter is reviewed first. Then, a new design technique for the SI ratio-independent algorithmic A/D converter is proposed. Finally, the effects of non-ideal characteristics of the devices, the switch charge injection, and finite impedance on data conversion accuracy are analyzed.

5.2.1 Review of the Principle of Algorithmic A/D Converter

Similar to the algorithmic D/A converter, an algorithmic A/D converter consist of a multiply-by-two amplifier (2x), a sample and hold (S/H) circuit, a reference sum circuit, and two switches (S_1 and S_2), as shown in the block diagram of Fig. 5.7. Besides these units, a comparator is used for extracting the digital signal. The operation of the A/D converter is as follows. The conversion consists of first sampling the input signal onto the S/H circuit. This is done by selecting the input signal instead of the loop signal using the switch S_2. The input signal is then passed onto the multiply-by-two (2x) amplifier which doubles its value. To extract the digital information from the input signal, the output voltage V_o of the amplifier 2x is compared with the reference voltage V_{ref}. If it is larger than the reference voltage, the corresponding bit is set to '1' and the reference is then subtracted from V_o. Otherwise, this bit is set to '0' and the signal V_o is kept unchanged. The resulting signal

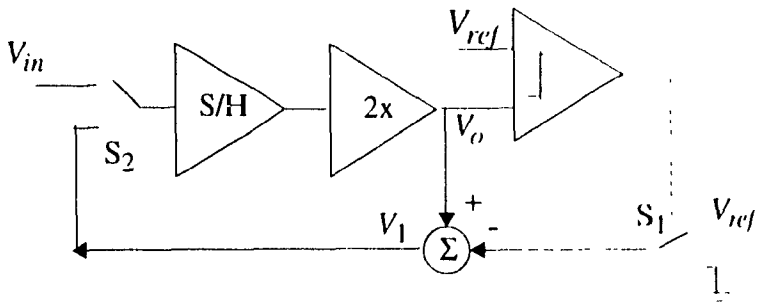


Fig. 5.7 The block diagram of the algorithmic multiplication A/D converter

V_1 is then transferred, by the switch S_2, back into the analog loop for further processing. This process continues until the desired number of bits have been obtained. The converter then samples a new input signal for the next conversion.

5.2.2 SI Ratio-Independent Algorithmic A/D Converter Design Technique

Fig. 5.8 shows the SI design circuit of an algorithmic A/D converter with the simple SI memory cells. Fig. 5.9 gives the switch-controlling waveforms. The circuit can perform the ratio-independent algorithmic A/D conversion operation. The data conversion is started with the MSB. The operation of the circuit is as follows. During the first clock cycle, the switches S_1 and S_2 are closed and T_1 samples the input signal I_i, giving $I_1 = J + I_i$. In the second clock cycle, S_1 and S_2 are opened, and S_3 and S_4 closed, T_1 holds the input signal and loads it into T_2, giving the current $I_2 = J - I_i$. During the clock cycle 3, S_5 and S_6 are closed and T_3 samples the current signal from T_1 giving the current $I_3 = J - I_i$. During the 4th clock cycle, the switch S_7 closes, the currents i_2 and i_3 are compared with the reference current I_{ref}, where $i_2 = J - I_2 = -I_i$ and $i_3 = J - I_3 = -I_i$. If the doubled input current $2I_i > I_{ref}$, the comparator outputs '1' (MSB = '1') and the switch S_8 is closed, giving $i_4 = 2I_i - I_{ref}$. The current i_4 is sampled by T_1 at the fifth clock cycle. If the current $2I_i < I_{ref}$, the comparator outputs '0' (MSB = '0'), the switches S_8 and S_7 are opened, and S_4 and S_6 are closed. Then, $2I_i$ will be sampled by T_1. Once T_1 samples and holds the current from i_2 and i_3 or from i_4, T_2 and T_3 proceed to operate in same manner as before. This sequence is repeated until the desired resolution has been achieved. The converter requires 4 clock cycles for each bit of conversion and an n-bit conversion takes 4n clock cycles. After the nth bit conversion is completed, the output current $i_1(n)$ of T_1 can be expressed as

$$i_1(n) = J - I_1(n) = 2^n I_i - I_{ref} \sum_{k=1}^{n} 2^{k-1} b_{k-1}, \qquad \text{(EQ 5.29)}$$

where b_{k-1} is the (k-1)th digital bit with a value of '1' or '0'.

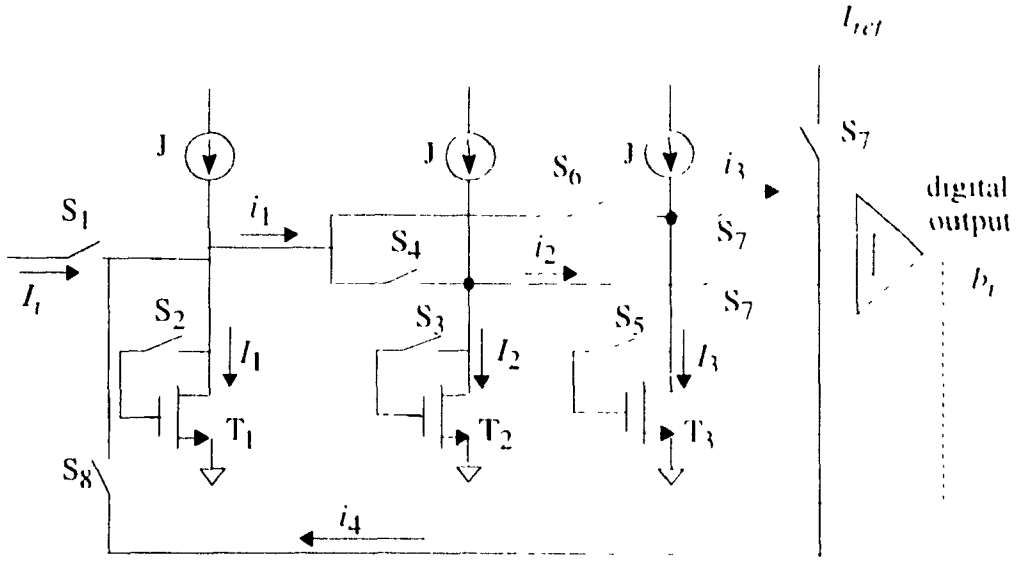


Fig. 5.8 A SI ratio-independent algorithmic A/D converter using simple memory cells

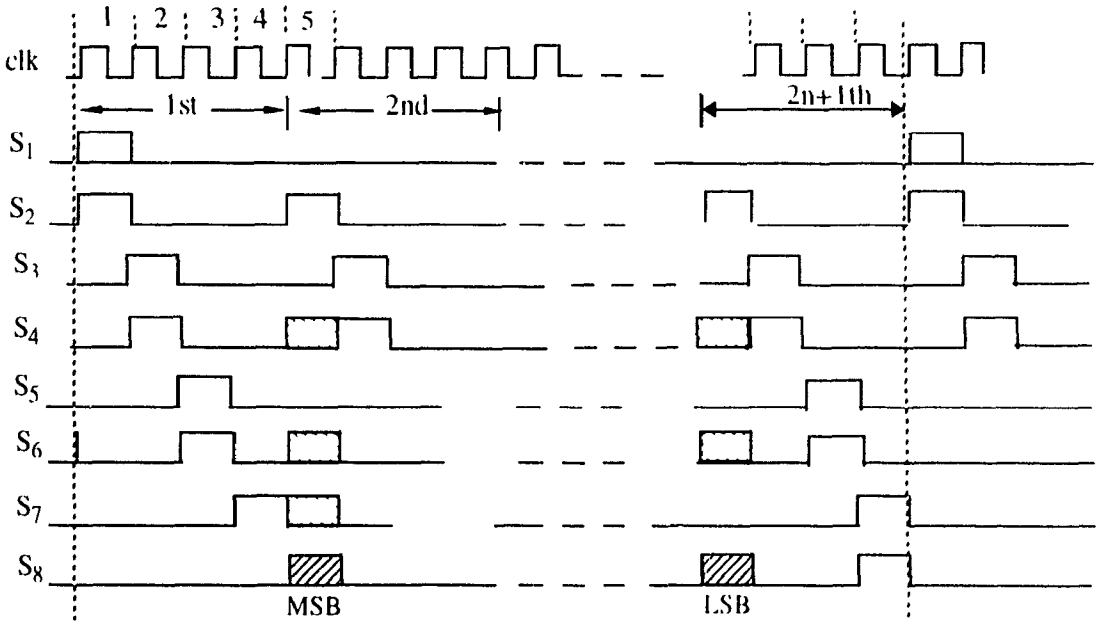


Fig. 5.9 The switch-controlling waveforms for A/D operation

5.2.3 A/D Conversion Error Analysis

As with the D/A converter, the finite impedance of the memory cell, non-closure resistance of the switches, and the switch charge injection will all affect the performance of the A/D converters. Besides these, the data conversion accuracy of the A/D converter is also affected by the input offset voltage of the comparator. In what follows, we will analyze effects of these non-ideal characteristics.

- *Effect of Finite Impedance of SI Memory Cell*

Taking into consideration the effects of finite impedance of the memory cells, the currents of i_1, i_2 and i_3, during the first conversion cycle, are given by

$$i_1(1) = I_i \qquad \text{(EQ 5.30)}$$

$$i_2(1) = \frac{G_{m2}}{G_{m2}+G_{12}} i_1(1) \qquad \text{(EQ 5.31)}$$

$$i_3(1) = \frac{G_{m3}}{G_{m3}+G_{13}} i_1(1) , \qquad \text{(EQ 5.32)}$$

where $G_{m2} = g_{m2}g_4$, g_{m2} is the transconductance of T_2, g_4 is the transconductance of the switch S_4, $G_{12} = (g_{o1}+g_{o2})g_4 + g_{o1}g_{m2}$, $G_{m3} = g_{m3}g_4$, g_{m3} is the transconductance of T_3, $G_{13} = (g_{o1}+g_{o3})g_6 + g_{o1}g_{m3}$, and g_6 is the transconductance of the switch S_6.

During the clock cycle 4, the currents i_2 and i_3 are compared with I_{ref} giving $i_2 + i_3 - I_{ref}$. This current is transferred to T_1 during the clock cycle 5 (start of the second conversion cycle) and thus, the current i_1 becomes

$$i_1(2) = \frac{G_m}{G_m+G} i_2(1) + \frac{G_m}{G_m+G} i_3(1) - I_{ref} b_1 \qquad \text{(EQ 5.33)}$$

To simplify the conversion error analysis, we assume that $G_{m2} \quad G_{m3} \quad G_m$, and G_{12} $G_{13} = G$. Thus, (EQ 5.33) can be rewritten as

$$i_1(2) = 2\left(\frac{G_m}{G_m + G}\right)^2 I_{in} - I_{ref} b_1 \qquad \text{(EQ 5.34)}$$

Continuing in this manner, after the nth conversion cycle, the current i_1 is given by

$$i_1(n) = 2^n\left(\frac{G_m}{G_m + G}\right)^n I_{in} - I_{ref} \sum_{k}^{n} 2^{k \quad 1} b_{k \quad 1} \qquad \text{(EQ 5.35)}$$

In practical circuits, we have $G_m >> G$. Thus, (EQ 5.35) can be simplified to be as

$$i_1(n) \quad 2^n (1 - \frac{G}{G_m})^n I_{in} - I_{ref} \sum_{k}^{n} 2^{k \quad 1} b_{k \quad 1} \qquad \text{(EQ 5.36)}$$

Expanding $(1 - G/G_m)^{k-1}$, and ignoring all second- and higher-order terms, we have

$$i_1(n) = 2^n I_{in}^n - I_{re} \sum_{k}^{n} 2^{k \quad 1} b_{k \quad 1} - 2^n n (\frac{G}{G_m}) I_{in} \qquad \text{(EQ 5.37)}$$

Thus, we see the finite impedance of the SI memory cells creates a nonlinear error equal to $2^n n(G/Gm)I_m$.

- *Effect of Switch Charge Injection*

Assuming that the switch charge injection causes a current error I_f, the output current of the memory cell, as each time when the SI memory cell changes its mode from sample to hold, can be written as

$$i_k' = i_k + I_{fk}, \qquad k = 1, 2, 3, \qquad \text{(EQ 5.38)}$$

where i_k is the output current of memory cell T_k, and I_{jk} is the error current created by the switch charge injection.

Including the effect of switch charge injection, the current i'_1 during the first conversion cycle can be expressed as

$$i'_1(1) = I_{in} + I_{j1} \qquad \text{(EQ 5.39)}$$

The current $i'_1(1)$ is transfer ed to T_2 and T_3 during this conversion cycle, giving

$$i'_2(1) = i'_1(1) - I_{j2} = I_{in} + I_{j1} - I_{j2} \qquad \text{(EQ 5.40)}$$

$$i'_3(1) = i'_1(1) - I_{j3} = I_{in} + I_{j1} - I_{j3} \qquad \text{(EQ 5.41)}$$

During the second conversion cycle, i'_1 is given by

$$i'_1(2) = i_2(2) + i_3(2) - b_1 I_{ref} \qquad \text{(EQ 5.42)}$$

Substituting (EQ 5.40) and (EQ 5.41) into (EQ 5.42), we have

$$i'_1(2) = 2(I_{in} + I_{j1}) - I_{j2} - I_{j3} - b_1 I_{ref} \qquad \text{(EQ 5.43)}$$

Thus, after the nth conversion cycle, i_1 is given by

$$i'_1(n) = 2^n I_{in} - I_{ref} \sum_{k=1}^{n} 2^{k-1} b_k + 2^{n-1}(2I_{j1} - I_{j2} - I_{j3}) \qquad \text{(EQ 5.44)}$$

From (EQ 5.44), we see that the switch charge injection produces an offset current $2^{n-1}(2I_{j1} - I_{j2} - I_{j3})$. Just as in the proposed D/A converter, the direction of the switch charge injection error current I_{j2} and I_{j3} is complementary to the direction of current error

I_{j1}. Thus, the effect of the switch charge injection can be reduced by making the switches and the memory transistors of the SI memory cells matched. Since all the memory cells in the proposed A/D converter are of the same, matching of the cells is relatively easier than that in the case of the A/D converter of [16], in which different types of cells are used.

The analysis given above is based on the assumption that the switch charge injection creates just a signal-independent current error. In practical circuits, the switch charge injection will also create a signal-dependent current error. When considering the signal-dependent current error, the effect of the switch charge injection is similar to the effect of the finite impedance, producing a nonlinearity conversion error.

- *Settling Time Error*

Similar to the case of the D/A converter, when the proposed A/D converter operates at high speeds, the non-zero settling time error creates an output current error in the SI memory cell. The effect of this error is same as that of the switch charge injection error. It creates an offset current error and a nonlinearity error. The higher the speed, the bigger is settling time error. Therefore, the speed of the A/D converter is limited by the settling time of the memory cells used.

- *Offset of Comparator*

In the SI A/D converter, the memory cell performs just the function of doubling the current and the comparator extracts the digital signal from the current information. If the difference between the doubled current signal and reference current is smaller than the offset of the comparator, the comparator would not able to recognize this difference, and therefore, it will not extract the digital signal. Thus, the maximum resolution of the A/D converter is limited by the offset of the comparator.

5.3 Practical Design of the Proposed SI D/A Converter

As analyzed in Section 5.1.3, the non-ideal characteristics of the SI memory cells and the switches creates large analog errors. These errors affect the conversion accuracy of the converter significantly. In this section, we will discuss the practical design considerations to reduce the effects of non-ideal characteristics of the SI memory cells and switches.

A SI D/A converter is designed using the high-performance SI memory cells proposed in Chapter 3. To verify the performance of designed converter, the circuit is simulated using HSPICE. A prototype chip is designed and fabricated using the standard 1.2 μ N-well CMOS process technology and tested in the laboratory. Both the simulation results and test results are presented in this section.

5.3.1 Practical Design Considerations

As mentioned above, although the proposed D/A converter does not require matching of the components, the finite impedance of the memory cell and the switch charge injection may significantly affect the conversion accuracy. To reduce the effects of finite impedance and switch charge injection, a high performance memory cell has to be used in place of the simple memory cell. The memory cells DMC-I and DMC-II presented in Chapter 3 can be used for the proposed D/A converter design. The new memory cells provide improvements of three orders of magnitude in the output resistance and two orders of magnitude in the switch charge injection of the memory cell as compared with the simple current memory cell.

In Section 5.1.3, the effect of the non-zero closure resistance of the switch was analyzed. Since it produces the data conversion gain error and the non-linearity error, the size of each switch has to be chosen carefully. The NMOS switch closure resistance can be

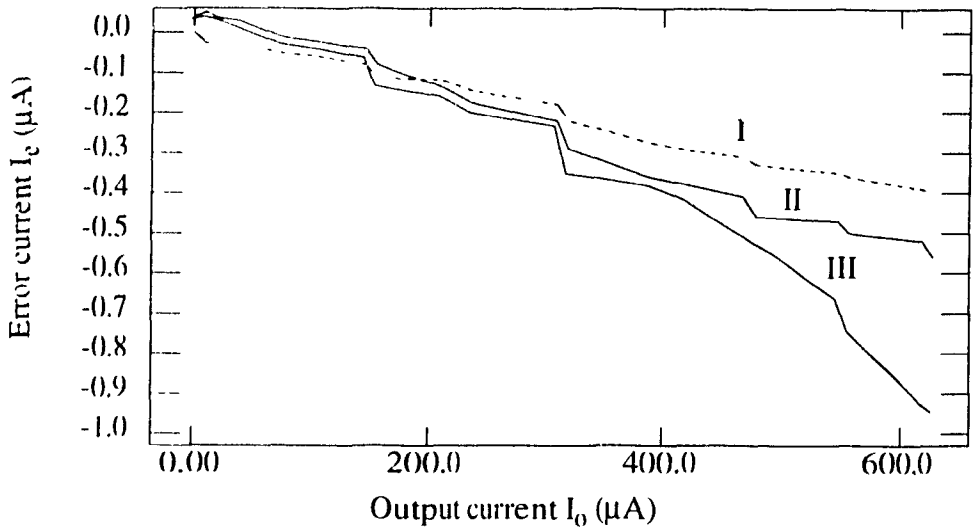
obtained as

$$R_{on} = \frac{1}{(\partial I_{DS}) / (\partial V_{DS})} = \frac{1}{(k_p \frac{W}{L})\ (V_{GS} - V_T - V_{DS})} \qquad \text{(EQ 5.45)}$$

Thus, it is seen that the larger the ratio W/L, the smaller is the closure resistance of the MOS switch. Therefore, the design is a trade-off between the chip area and the conversion accuracy.

5.3.2 Simulation Results of the Proposed D/A Circuit

The proposed D/A converter circuit with the high-performance SI memory cells of Chapter 3 was simulated using HSPICE based on the standard 1.2 μ CMOS process technology parameter set. The simulation results with I_{ref} = 20 nA are given in Fig. 5.10 The nonlinearity error is within ± 0.2 μA (curve I) when the full scale output current is about 640 μA. This corresponds to an accuracy of a 12-bit D/A converter. In low output current band, the dynamic range of the converter is limited by the leakage current of the MOS transistors. On the other band, in the high output current band, it is limited by the chip area, since the maximum current of a MOS transistor is dependant on the aspect ratio of the transistor. The simulation results also show that the nonlinearity error, and gain error are reduced, when the aspect ratio of switches S_4, and S_6 are increased, As the size of the capacitor transistor T_C is increased, resulting in an increased C_{Tc}, not only the offset error gets reduced, but also the nonlinearity and gain errors are decreased. From the simulation results, we can see that the switch charge injection not only produces an offset error, but it also creates a nonlinearity error. This is, because the output voltage V_o of the memory cell is not constant. As a matter of fact. V_o changes by hundreds of *mV*s creating a signal-dependent switch charge injection error when the conversion current changes by hundreds of *mA*s. The nonlinearity is increased when the output current is increased.



Curve I. The size of T_C is W/L= 20 μ /10 μ,
The size of switches S_4 and S_6 is W/L = 300 μ / 1.2 μ

Curve II. The size of T_C is W/L= 10 μ /10 μ,
The size of switches S_4 and S_6 is W/L = 300 μ /1.2 μ

Curve III. The size of T_C is W/L= 10 μ /10 μ,
The size of switches S_4 and S_6 is W/L = 100 μ/ 1.2 μ

Fig. 5.10 The plot of error currents of the proposed D/A converter obtained from simulation

5.3.3 Prototype Chip Test Results

A prototype D/A converter chip containing two D/A converter circuits was designed and fabricated using the standard 1.2 μ N-well CMOS process technology. The chip layout is shown in Fig. 5.11. The layout consist of 8 differential SI memory cells (marked M_1 to M_8) and several MOS switches. The cells M_1 to M_4 use operational transconductance amplifier structure (Cell #2), and cells M_5 to M_8 use folded amplifier structure (Cell #3). Cell M_1 is designed as a voltage-to-current converter and M_5 is used as the sample and hold circuit for the output current. The cells M_2 to M_4 are connected by switches to form a D/A converter (D/A #1), and the cells M_6 to M_8 are connected by switches to form another D/A converter (D/A #2).

Due to the use of high-gain cells, the converter D/A #1 suffered from the stability problem. The test results of the converter D/A #2 showed no stability problem. All the test results that follow are for the D/A #2 circuit.

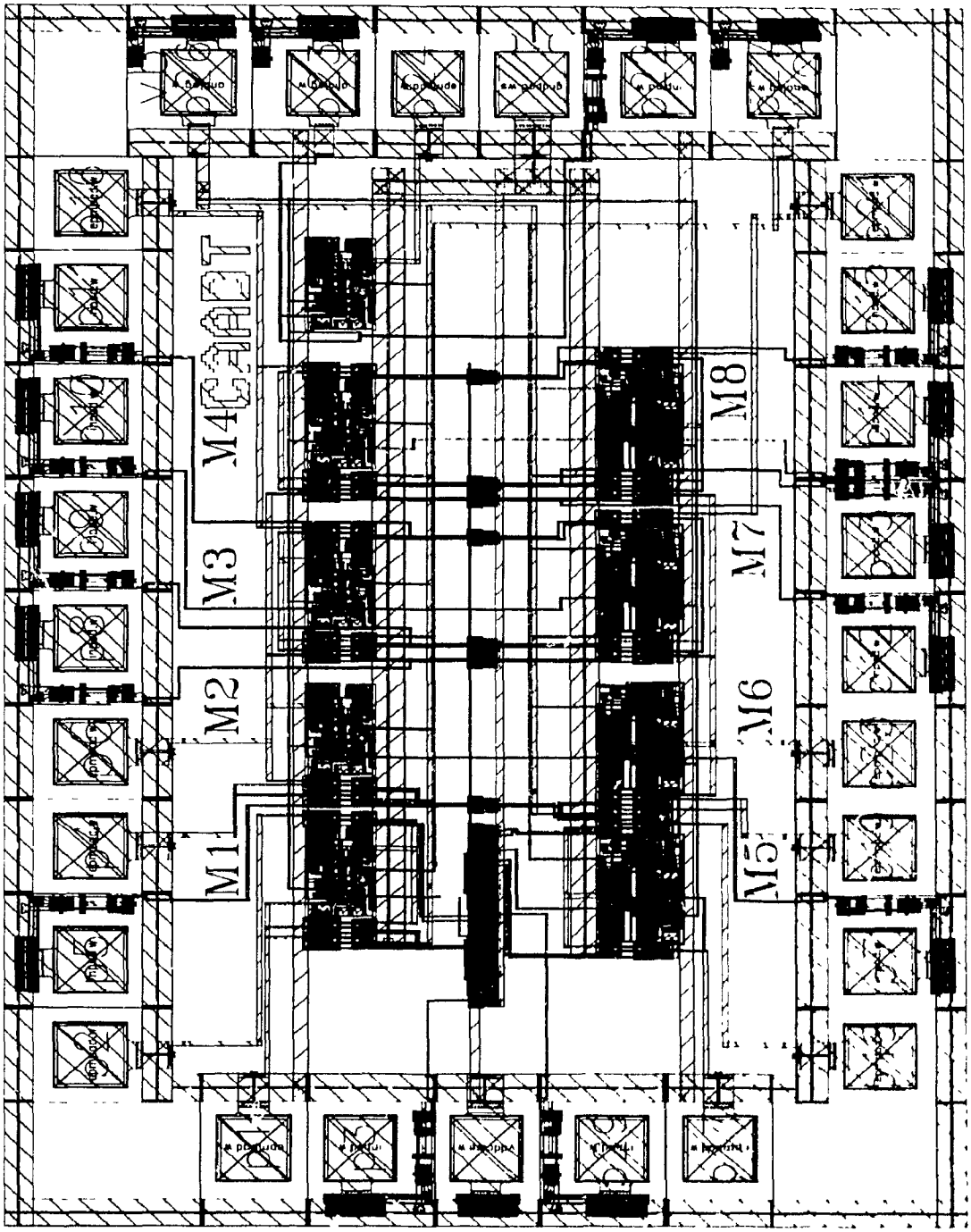


Fig. 5.11 Layout of two SI ratio-independent algorithmic D/A converters

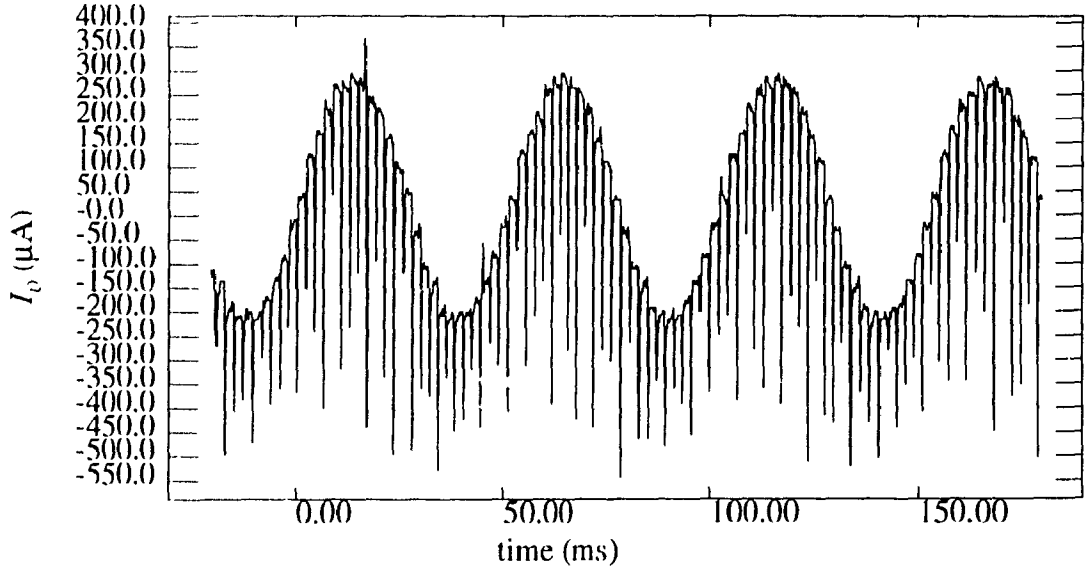


Fig. 5.12 Dynamic behavior of the D/A converter (D/A #2)

Fig. 5.12 shows the dynamic behavior of the converter D/A #2. The input digital code to the converter is a sinusoid. The output of the D/A is then analyzed using the FFT to transform the time-domain information into the frequency domain for investigating the nonlinearity errors [42]. Fig. 5.13 shows the FFT analysis results. It is seen that the har-

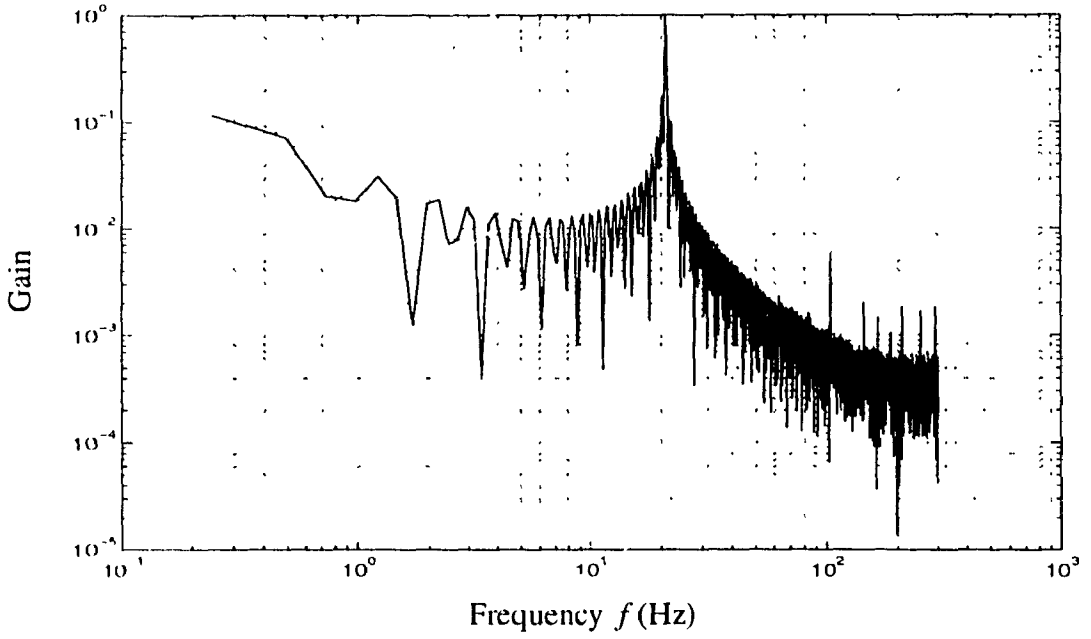


Fig. 5.13 Magnitude spectrum analysis results of the D/A converter (D/A #2) output

monics of the D/A converter are about -48 dB below the fundamental which corresponds to an 8-bit integral linearity. Fig. 5.14 shows the differential nonlinearity error of the D/A

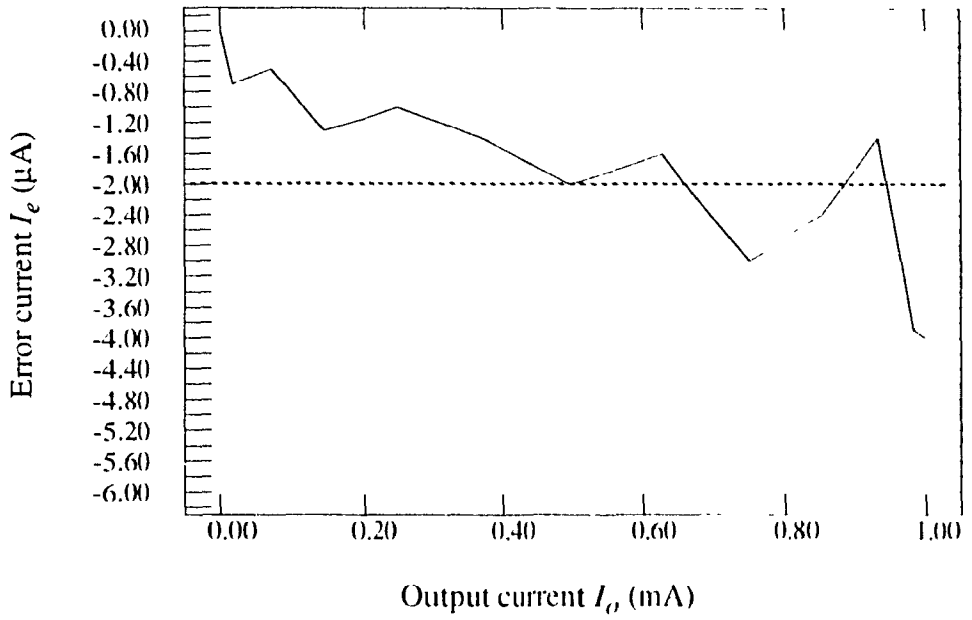


Fig. 5.14 The differential nonlinearity of the D/A converter (D/A # 2)

converter. The differential nonlinearity error of the converter is less than $\pm$ 2 μA. From Fig. 5.14, we can see that the gain error of the D/A converter is increased as the output current increases. Comparing the results of Fig. 5.14 with the simulation results shown in Fig. 5.10, and referring to the conversion error analysis discussed in Section 5.1.3, it is clear that the nonlinearity errors of the converter are caused by the switch charge injection and the finite impedance of the memory cells. Therefore, by increasing the size of gate capacitors T_C and the size of the switches S_4 and S_6 (refer to Fig. 5.2), the nonlinearity errors and gain error of the D/A converter can be reduced further. The complete test results of the prototype D/A converter are given in Table 5.1.

Table 5.1 Test results of the D/A converter chip

Parameter	Value
Power supply (V)	5
Clock frequency (KHz)	30
Resolution (bit)	8
THD (dB)	-48
Power dissipation (mW)	25
Chip area (mm^2)	0.43

5.4 Summary

A new SI ratio-independent algorithmic multiplication D/A converter design technique has been described. The effects of the non-ideal MOS transistor characteristics on conversion accuracy are theoretically analyzed. The technique provides a high-accuracy and high-resolution data conversion without requiring matching of the components. Since the converter uses a SI technique, it does not require linear capacitors, and therefore, the double poly process is not necessary. Because the converter requires only 3 clock cycles for each bit D/A conversion, it is 1.3 times faster than the SC ratio-independent algorithmic D/A converter [37].

A SI ratio-independent algorithmic A/D converter circuit has also been given in this chapter. A theoretical analysis of the effects of the non-ideal MOS transistors characteristics on the conversion accuracy of the A/D converter designed using this technique has been carried out.

The proposed D/A converter has been simulated using HSPICE with the parameter

set of a typical 1.2 μ CMOS process technology. The simulation results are very close to those obtained from the theoretical analysis. A prototype D/A converter chip has been designed and implemented by using the standard 1.2 μ CMOS process technology, and the chip tested in the laboratory. The test results show that the proposed D/A converter chip has an 8-bit conversion accuracy. The nonlinearity error measurement results are in good agreement with those obtained from the theoretical analysis or from simulation results. The conversion accuracy can be improved by increasing the values of the gate capacitors and the size of the switches. The size of the gate capacitors used in this prototype chip design is only 21.5 μm x 34 μm (the value of capacitor is about 0.05 pF), and the chip area for the D/A converter is about 0.43 mm^2.

Chapter 6

CONCLUSIONS AND SUGGESTIONS FOR FURTHER RESEARCH

6.1 Concluding Remarks

In recent years, the traditional role of analog circuits has changed from a main signal processor to an interface between a DSP system and the outside world that is still mostly analog. Thus, in their new role, they must be made to acquire all the characteristics needed for them to co-exist with the dominant digital environment. The performance of analog circuits has to be matched with that of digital circuits and they have to be implemented using a process technology that has been optimized for the implementation of digital circuits.

The SI technique is a possible solution to make the analog circuits matched with the digital circuits both in performance and implementation process technology. The switched-current techniques are finding an increasingly greater role in the design and implementation of analog circuits, since they do not require linear capacitors and are capable to work with low power supplies. Since linear capacitors are not required, a SI integrated circuit is not dependent on a special analog process technology and it is fully compatible with the digital process technology. In SI circuits, lowering the supply voltage should not reduce its dynamic range or signal-to-noise ratio. However, the non-ideal characteristics of MOS transistors affect the performance of the SI circuits significantly, and has made the use of the SI circuits still less attractive in comparison with the SC circuits. This thesis has been

concerned with the problems of switched-current circuit design for signal processing taking into consideration the effects of non-ideal characteristics of MOS transistors and other application-related problems.

To reduce the effects of non-ideal characteristics of MOS transistors, a high-performance differential SI memory cell design technique that uses a differential amplifier and the regulated cascode circuit has been developed. The effects of the non-ideal MOS transistor have been analyzed. The theoretical analysis and the simulation results show that the proposed differential SI memory cells achieve the best performance as compared with the existing SI memory cells in terms of current transmission operation and a performance similar to that of the fully differential SI memory cell in terms of power supply rejection ratio. The circuit complexity of the differential SI memory cells is much simpler than the fully differential SI memory cell. The settling time and the stability problem of the memory cells have also been studied. Two practical SI memory cells have been designed with the structures of transconductance amplifier and folded cascode amplifier, respectively. Three prototype chips have been designed and implemented using a standard 1.2 μ CMOS process technology. The prototype chips have been tested. The performance of the memory cells have been evaluated in the terms of gain error, total harmonic distortion, settling time and supply voltage. The test results have shown that the cells achieve very small gain error, very small total harmonic distortion, and are capable of working with power supply voltage ranges in the range of 3.3 V to 5 V.

Since the analog filters and A/D and D/A converters are integral parts of a DSP system, attention also been focused on new SI circuit designs for these circuits. A new SI technique has been proposed for the design of fully-programmable SI filters, and a novel ratio-independent algorithmic multiplication SI technique has been proposed for the design of D/A converters.

The proposed SI filter design technique uses digital filter structures and design synthesis techniques. The resulting SI filter has very regular circuit structure. Without requiring modification of the circuit structure of the filter, the characteristics of the filter can be changed by properly selecting the sizes of the coefficient transistors in an array of transistors. Since an array of unit transistors occupies a much larger chip area, a transistor array consisting of three different size transistors has been used. It has been shown that proposed scheme can reduce the chip area significantly, while maintaining the accuracy of the most significant bits of the filter coefficients. As an example, a second-order IIR filter has been designed using the developed technique. The filter has been simulated using HSPICE in the time domain and the results are analyzed using the FFT to evaluate the characteristics of the filter in the frequency domain. The results are very close to those obtained from the theoretical analysis. A prototype chip which contains six second-order IIR filters has been designed and fabricated using the standard 1.2 μ N-well CMOS process technology. Hard wiring technique is used for programming of these filters. The chip has been tested in the laboratory. The test results have shown that the characteristics of the fabricated filters satisfy the design specifications. The use of the proposed high-performance SI memory cells in the filter implementation has provided an improved performance.

A novel SI ratio-independent algorithmic technique for the design of D/A converters has been proposed. The technique employ a ratio-independent algorithm for data conversion. The converters can achieve high-resolution, high-accuracy data conversion without requiring matching of components. The proposed D/A converter requires only 3 clock cycles for each bit of conversion. It is 1.3 time faster than a SC ratio-independent algorithmic D/A converter. A new SI ratio-independent algorithmic A/D converter circuit has also been presented. The effects of non-ideal characteristics of MOS transistors have been studied and some suggestions have been made to improve the converters' performance. The high-performance SI memory cells developed in Chapter 3 have been used in the design of

D/A converter to reduce the effects of switch charge injection and finite impedance of the memory cell. The proposed D/A converter was simulated using HSPICE and the simulation results have been found to be very close to those theoretical predicted. A prototype chip of the D/A converter has been designed and implemented using the standard 1.2 μ N well CMOS process technology and tested in the laboratory. Test results have shown that the D/A converter achieves an 8-bit resolution with non-linearity error less than one-half of the least significant bit.

6.2 Scope for Future Investigations

The future requirements of the analog interface circuits in a DSP system could be those of lower cost, higher operating speed and lower power supply voltages.

The process technology presently used for the SI circuit is the same as those used for digital circuits. However, future decrease in the cost of the analog circuits would heavily rely on our capability to develop new analog design techniques that are compatible with the emerging new digital process technologies.

The present SI circuits cannot be used in high-frequency applications such as video signal processing. In order for this to happen, the SI design techniques have to be developed to be compatible with the sub-micron process technology for increasing the frequency bandwidth of the MOS transistors.

The present SI circuits cannot operate with supply voltages lower than 3 V. The industry has proposed lowering of the supply voltage to 2.4 V or even as low as 1.8 V for the next generation digital VLSI circuits. Therefore, for the next generation DSP systems, SI techniques ought to be evolved to provide non-degraded performance at low power supply voltages.

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