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A MODIFIED PULSEWIDTH MODULATED CURRENT SOURCE INVERTER

GERASIMOS MOSCHOPOULOS

A Thesis

in

The Department

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Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

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ABSTRACT

A MODIFIED PULSEWIDTH MODULATED CURRENT SOURCE INVERTER

GERASIMOS MOSCHOPOULOS

Current source inverters (CSIs) have several features that make them attractive in induction motor drives; however, they are not as widely used as voltage source inverters (VSIs) because of the drawbacks they have. These drawbacks include the appearance of overvoltage spikes on the inverter output voltage and the restriction of pulsewidth modulation techniques (PWM) that can be implemented. To overcome these drawbacks, it has been proposed to add additional components to the basic power circuit configuration; however, these modified topologies use a substantial number of additional components (thus increasing cost and complexity). Another proposed solution is to provide a short circuit path for the inductor current through the inverter itself but this results in the rise of the dc link current.

In this thesis, a modified pulsewidth modulated (PWM) CSI topology is proposed. This topology allows any PWM technique to be implemented no matter how low the modulation index or the fundamental frequency is, improves the dynamic response of the CSI, and allows the inverter output voltage spikes to be suppressed without the disadvantages of other previously proposed solutions. These benefits are obtained at the cost of only one additional switch connected in the dc link and some additional input filtering. The operating principles of the proposed CSI are discussed and its characteristics under steady-state conditions are examined. The feasibility of the proposed converter is demonstrated with simulated results, and with experimental results obtained from a 5 kVA prototype unit.

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I would like to thank Mr. Joseph Woods and Mr. Donato Vincenti for helping me with the experimental set-up and for being generous with their time and expertise.

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LIST OF ACRONYMS

3HIPWM	Third Harmonic Injection Pulsewidth Modulation
AC	Alternating Current
ASCI	Autosequentially Commutated Inverter
BJT	Bipolar Junction Transistor
CSI	Current Source Inverter
DC	Direct Current
EPROM	Erasable Programmable Read Only Memory
EPWM	Equal Pulsewidth Modulation
GTO	Gate Turn-Off Thyristor
HIPWM	Harmonic Injection Pulse Width Modulation
ICCC	Instantaneous Current Control Capability
kVA	kilo Volt-Ampere
MCSI	Modified Current Source Inverter
MSPWM	Modified Sinusoidal Pulsewidth modulation
ms	milli seconds
mH	milli Henry
PWM	Pulsewidth Modulation
RMS	Root Mean Square
RPM	Revolution Per Minute
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulsewidth modulation
TPWM	Trapezoidal Pulsewidth Modulation
VSI	Voltage Source Inverter
VA	Volt-Ampere
μF	micro Farad

LIST OF PRINCIPAL SYMBOLS

A_{dc}	attenuation factor for dc link inductor design
A_o	attenuation factor for output capacitor design
C_f	value of the input filter capactors
D_m	ratio of I_{ac} to I_{acr}
f	frequency
f_b	break frequency
f_h	harmonic frequency
f_{in}	input frequency
f_o	inverter fundamental switching frequency
f_r	frequency equal to six times the input frequency
f_{sw}	inverter switching frequency
G	GTO
I_{ac}	fundamental rms component of input line current
I_{acl}	output ac line current
I_{acr}	total rms value of input line currents
I_d	rectifier output current
I_{dc}	dc bus current or its average value
$I_{dc,peak}$	value of top part of dc bus current
I_h	harmonic current
I_L	load current
I_{Ldc}	dc link inductor current
$I_{Ldc,rat}$	rated dc link inductor current
I_n	nth current harmonic
I_o	inverter output current
k	number of switching angles
K	PWM pattern constant
K_{ac}	ratio of input line current fundamental rms component to the average value of the dc bus current

$K_i(M)$	ac gain factor of PWM pattern as a function of M
K_s	duty cycle of auxiliary switch
L-N	line-neutral
L-L	line-line
L_{dc}	dc link inductor
L_f	value of the input filter inductors
M	modulation index
N_p	number of pulses
pf	power factor
pu	per unit
P	real power at input and output
Q	quality factor for input filter
R_f	input filter resistance
R_L	load or line resistance
R'_r	rotor resistance
R_s	stator resistance
s	slip
SW	switch or switching function
t_1	time instant
T	thyristor
V_{ac}	ac rms line-neutralinput voltage
V_d	rectifier output voltage
V_{dc}	inverter input voltage
V_h	harmonic voltage
V_{in}	input voltage
V_o	fundamental rms component of the output line-neytral voltage
V_r	voltage ripple on dc bus
X_c	output filter capactor impedance for f_o
X_{ch}	output filter capacitor impedance for any f_h
X_m	magnetizing reactance

X'_r	rotor reactance
X_s	stator reactance
Z_L	load impedance
Z_o	output impedance
α	rectifier firing angle
ϕ_o	output phase angle

CHAPTER 1 - INTRODUCTION

1.1. Introduction

The induction motor - particularly the squirrel cage type - is rugged, reliable, efficient, and has low maintenance requirements; therefore it is the most widely used electric motor. This, however, was not always the case because the applications of the induction motor were limited to those requiring constant speed as methods of speed control were either expensive, inefficient, or limited. For example, one method of speed control was to connect the induction motor to a variable frequency source made up of a dc motor - ac generator set; this was impractical because of the cost and required maintenance of two machines in addition to tne load.

The advent of power semiconductor devices in the 1950's and 60's, such as thyristors, has led to the widespread use of static power conversion as a means of constructing variable frequency sources for induction motors. Among the various power conversion circuits in existence, the inverter, which converts a dc source into a three-phase ac source, is the one that is generally used in induction motor drives. There are two types of inverters that are used today: the voltage source inverter (VSI) and the current source inverter (CSI); both of these are shown in this chapter and their characteristics are compared. Since the focus of this thesis is on CSIs, a review of previously proposed CSI topologies is given. Finally, the objective, scope, contributions and summary of the thesis are given.

1.2. Voltage source inverter

A voltage source inverter (Fig. 1.1) requires a dc voltage at its input. This voltage is generally obtained by converting the voltage from the ac mains into a dc voltage with a rectifier then eliminating the harmonics with an LC filter. The inverter converts the dc voltage at its input into three symmetrical ac voltages through the appropriate firing of its switches. The ac voltages that are fed to the motor are not sinusoidal but are made up of square pulses, and it is the motor leakage inductances that attenuate the harmonics. The diodes are added to permit reverse current flow during reactive power flow or during regeneration, to clamp the load voltage to that of the input level, and to use in the forced commutation (turn-off) of the switches when thyristors are used.

1.3. Current source inverter

A current source inverter is fed from a current source which is made up of an inductor in series with a voltage source since an ideal current source does not exist. The inverter converts the dc input current into three symmetrical ac line currents that are then fed to the load.

The first CSI to be developed was the autosequentially commutated inverter (ASCI) [1]-[4]. This topology (Fig. 1.2) used thyristors as the main inverter switches

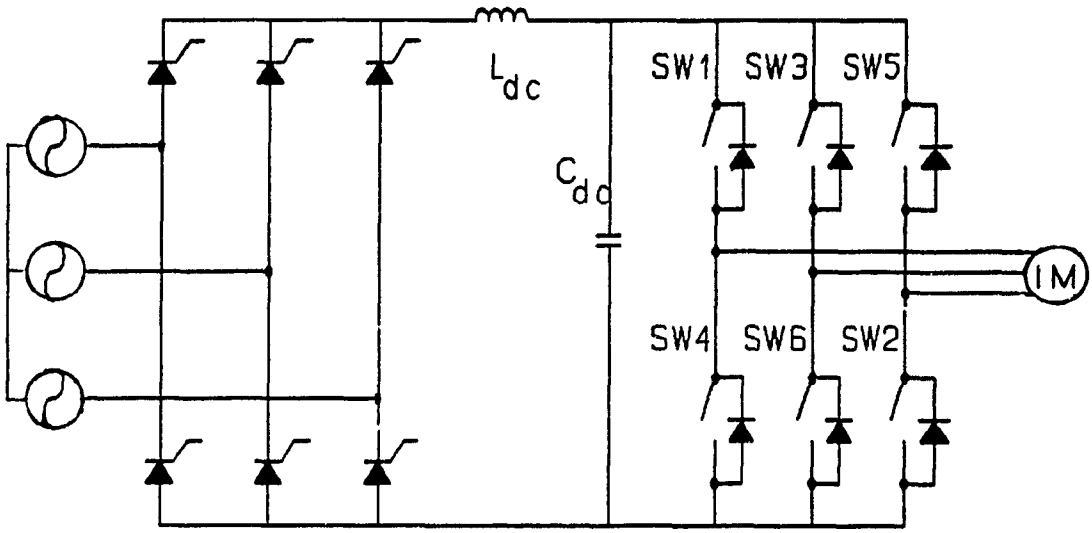


Fig. 1.1. Voltage source inverter.

and was the standard CSI topology of the 1970's. The topology got its name from the fact that if the thyristors were fired in sequence (T1-T6), then the firing of one switch would automatically commutate another. No additional circuitry was needed to commutate the thyristors because this was done by the diodes and capacitors in the inverter.

The advances in power semiconductor technology in the early 1980's such the development of gate turn-off thyristors (GTO) and bipolar junction transistors (BJT) led to the development of a new CSI topology as the ASCI was a thyristor based topology that could not take advantage of the new devices. The pulsewidth modulated CSI (PWM CSI) [5]-[6], shown in Fig. 1.3, has been gradually replacing the ASCI and is now the standard CSI topology [7] since it can produce almost sinusoidal line currents and has a higher range of operating frequencies. Since the inverter switches can be self-commutated, the commutating capacitors that were placed in the ASCI are removed. The PWM CSI, however, does have capacitors and they are used to filter out harmonics in the line currents and to provide current paths for the energy trapped in the leakage inductance of the motor whenever commutation takes place.

1.4. Voltage source inverter vs current source inverter

The relative advantages and disadvantages of VSI and CSI drives are given below. With these in mind, a designer can select the type of inverter best suited for

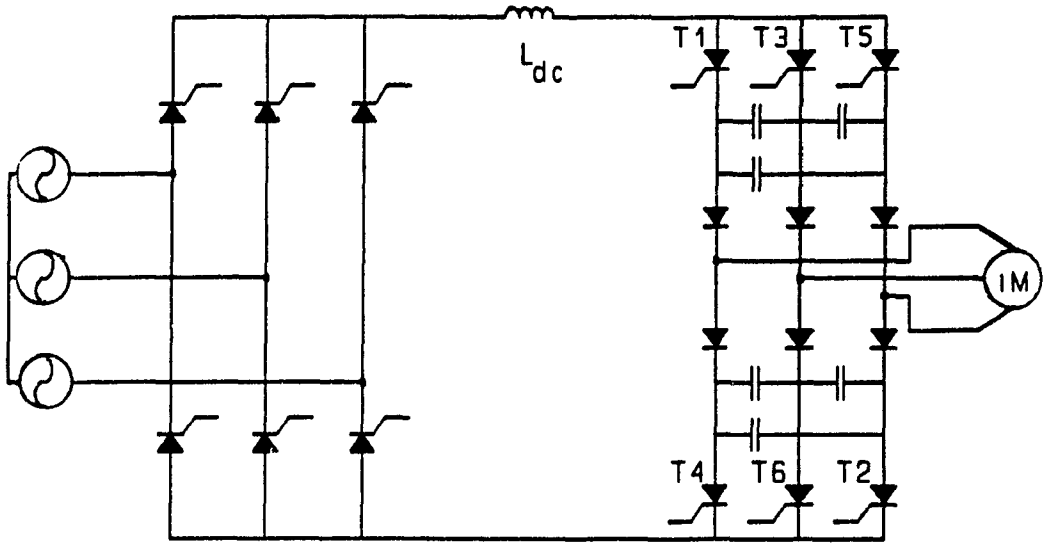


Fig. 1.2. The autosequentially commutated inverter (ASCI).

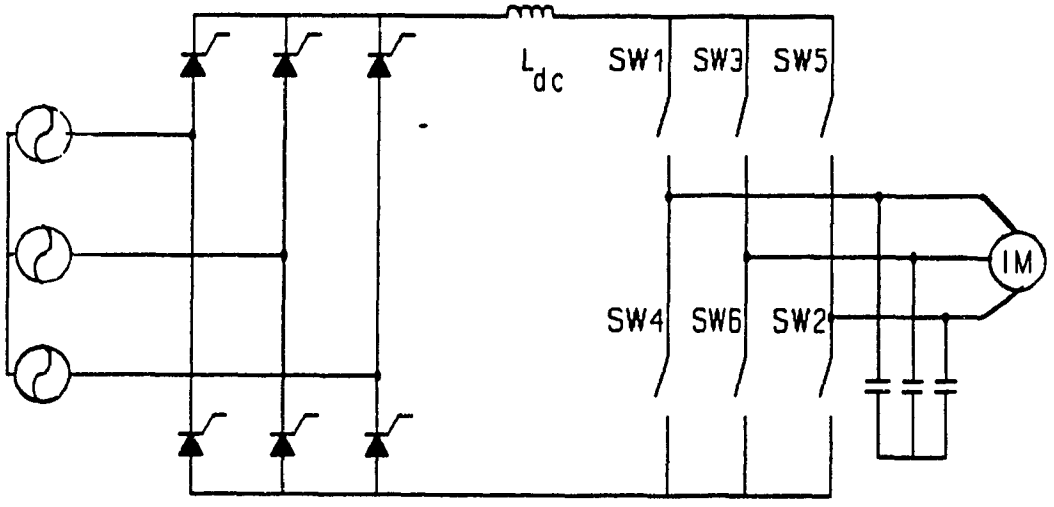


Fig. 1.3. The PWM current source inverter.

a particular application.

1) A CSI is more reliable than a VSI because it can tolerate a short-circuit in the inverter caused by the misfiring of the switches, by commutation failure, or by a fau.t in the load. Should any of the above occur, the resultant current can be regulated by controlling the rectifier output voltage.
2) A CSI has inherent four-quadrant operation capability and does not require any additional power circuitry for regeneration to occur. On the other hand, a VSI requires an additional converter connected anti-parallel to the front-end rectifier to provide a path for the current whenever regeneration occurs.
3) Multi-machine load on a single inverter or a multi-inverter load on a single rectifier is very difficult with CSIs; however this is not so for VSIs and they can be used wherever multi-machine or multi-inverter capability is required.
4) The inverter is more interactive with the load in a CSI than it is in a VSI. A large leakage inductance lengthens the current transfer interval in a CSI thus limiting the range of inverter operating frequency and speed of operation. Also, the output filter capacitor and the motor inductance produce a resonance effect that amplifies the harmonics near the resonant frequency. These problems do not exist in a VSI.

1.5. Literature review

Although the CSI has several advantages over the VSI, it is not as widely used because it has several drawbacks. In order to overcome some of these drawbacks, several researchers have proposed modifications to the standard ASCI and PWM CSI topologies. In this section, some of these drawbacks are examined along with a review of previously proposed modifications to the ACSI and the PWM CSI is given.

The problem that has sparked the most research into modified topologies is that the inverter output voltage contains large overvoltage spikes that can damage the inverter components and the load. These spikes are caused by the energy that is stored in the inverter capacitors and the motor leakage inductance, and appear whenever an inverter switch is commutated. This problem exists for both the ASCI and the PWM CSI, and is worse for the ASCI because the conduction interval for a switch is much longer thus the capacitors have more energy stored in them by the time commutation occurs. In order to reduce or suppress the output voltage spikes something must be done with the energy stored in the reactive elements.

One solution to the problem is to add a voltage clamping circuit to the inverter [8]-[9]. Voltage clamping circuits that have been proposed include zener diode circuits and transistor-capacitor-resistor circuits. The basic function of these circuits is to dissipate the reactive energy through a zener or a resistor whenever the inverter output voltage spikes reach a certain level. However, since energy is wasted

in the voltage clamping circuit, this method of reducing the inverter output spikes is not very efficient.

The overvoltage spike problem can also be solved by adding an energy rebound circuit to the inverter [10]-[12]. With this circuit, the energy stored in the motor leakage inductances is stored in a capacitor then fed back to the inverter whenever desired instead of being dissipated. Another advantage to having an energy rebound circuit has been shown by Matsuse and Kubota [13]. Since the storage capacitor acts as a dc voltage source at selected intervals, current does not have to always flow through the rectifier, and can be made zero whenever desired, thus allowing PWM techniques to be used with a standard thyristor rectifier. Although there are benefits to adding an energy rebound circuit to the inverter, one major disadvantage is that the circuit requires many additional components such as a diode rectifier and switches which increase the cost and complexity of the current source inverter.

Another drawback that the CSI has is that its dynamic response - the time it takes for the amplitude of the load currents to change after the command for change has been given is poor - especially when a phase-controlled rectifier is used as the front-end converter. The reason for the poor dynamic response is the size of the inductor in the dc link needed to ensure a stiff dc current; the current fed into the inverter cannot be quickly changed if the inductor is large. Several researchers have proposed solving this problem by firing the inverter switches in such a way so as to provide a short-circuit path for the inductor current through the

inverter itself [14]-[16]. This, however, results in a dc link current boost effect particularly at low operating frequencies and at low modulation indices.

A third drawback that the CSI has is that the topology limits the way that the inverter switches can be fired. As a result, the output line currents that are produced by the CSI contain more low-frequency harmonics than do the output voltages of a voltage source inverter and this causes problems at the output including a decrease in the efficiency of the motor. In order to increase the gating techniques that can be implemented, thus reducing the problems caused by line current harmonics, several researchers have modified the CSI by adding additional switches external to the inverter [17]-[18].

When the ASCI was the standard topology, researchers tried to increase its range of operating frequency by adding additional components in the inverter circuit [15]. [19]-[20]. This range was limited to low frequencies because the commutation process needed to turn off the thyristors was slow as it took time for the charge on the capacitor to reverse. The additional circuitry enabled the charge on the capacitor to reverse quickly or to reduce the charge in a way similar to the voltage clamping circuits.

The range of operating frequency of the PWM CSI is much higher than that of the ASCI because it does not have any commutating circuits as self-commutated switches are used. At high operating frequencies, however, the switching losses of the PWM CSI become higher. In order to reduce these losses, Murai and Lipo [21] proposed adding a series - resonant circuit to the dc link and making the

current into positive half-sinusoidal pulses. The new topology allowed for zero-current switching of the inverter switches to occur since the dc link current had zero points at which the switches were fired.

1.6. Scope and contributions

The objective of this thesis is to propose and analyze a modified PWM CSI topology that overcomes several of the drawbacks mentioned in the previous section, and to compare its performance to that of the conventional PWM CSI. The scope of this thesis is limited to an analysis of the characteristics of the proposed topology under steady-state conditions as the performance of the converter with an induction motor load under closed loop conditions is not considered. Emphasis is placed on demonstrating the operating principles, unique characteristics, and benefits of the proposed inverter topology.

The principal contributions of this thesis are as follows:

1) A modified current source inverter is proposed and analyzed. It is shown that the proposed inverter is simple and has several advantages over the conventional PWM CSI. The proposed topology allows any PWM technique to be used, has an excellent dynamic response, and does not have overvoltage spikes on the inverter output voltage.
2) The technique of variable modulation index control is examined in detail and its effect upon the operation of the conventional PWM CSI and the proposed

inverter is investigated and compared.

3) Since the inverter is an unconventional one, the standard design procedure for the conventional PWM CSI cannot be used; a design procedure to find steady-state operating points for the proposed CSI is presented.

1.7. Summary of the thesis

The contents of this thesis have been organized as follows:

In Chapter 2, the general rules for firing the CSI switches are given and several gating techniques for the inverter switches are examined. It is shown that the techniques that were originally proposed contain low-order harmonics and that the original gating rules were unnecessarily restrictive. PWM techniques that produce output line currents containing no low-frequency harmonics are presented. It is explained how the conventional PWM CSI does not allow certain techniques to be used and how this restriction can be removed by modifying the power circuit topology.

In Chapter 3, the operating characteristics of the conventional PWM CSI are examined. Equations relating the inverter operating parameters (i.e. the modulation index of the pattern) to the dc bus quantities are presented and are used to demonstrate the effect that a change in the parameters has on the dc bus. The dynamic response of the PWM CSI and the inverter output voltage spike problem are also considered. It is shown that the dynamic response cannot be improved and

the spike problem cannot be solved without some trade-offs, but that these trade-offs are not necessary for the proposed CSI topology.

In Chapter 4, the proposed topology is introduced and its steady-state operating characteristics are shown and contrasted to those of a conventional PWM CSI. A design procedure to calculate operating points for the inverter and the load is presented along with a design procedure for the output filter capacitors and the ratings of the switches. An example is presented to show how the design procedure can be used to calculate the steady-state dc bus and inverter output values for two load operating points. Finally, the feasibility of the proposed topology is verified with simulated and experimental results.

In Chapter 5, the input characteristics of the proposed topology are examined. Equations relating the dc bus quantities to those at the input are presented, and are used in a design example and in a comparison of power factor with other CSIs. Efficiency considerations for the proposed topology, the ASCI and the conventional PWM CSI are also given. A design procedure for the input filter is presented and verified with simulated and experimental results.

In Chapter 6, the conclusions of this thesis are given along with suggestions for future work.

CHAPTER 2 - PULSEWIDTH MODULATION TECHNIQUES AND PATTERNS FOR CURRENT SOURCE INVERTERS

2.1. Introduction

An inverter pattern can be defined as the line current waveform produced when the inverter switches are fired in a particular way. The pattern is very important to the operation of a CSI because it determines the CSI's performance and operating characteristics. Patterns can be designed to meet the desired criteria (i.e. elimination of lower order harmonics) for a particular application. In this chapter, the general rules for CSI patterns are presented along with several patterns used in ASCIs and PWM CSIs. It is shown these patterns are limited in the number of low-order harmonics that they can eliminate, but that this limitation can be relaxed so that more PWM patterns can be implemented and the performance of the CSI can be improved. The benefits of adding an auxiliary switch to the CSI are also investigated.

2.2. General rules for CSI patterns

There are limits that must be placed on the inverter pattern that can be used because of the CSI six-switch configuration. In general, the pattern for a CSI must be such that only one top inverter switch and one bottom inverter switch are on at any moment. If there are less than two switches on, then there is no path for the

dc link inductor current to flow through the inverter and the energy stored in the dc link inductor would damage the switches by forcing a path to appear. If there are more than two switches on at the same time, then the output line current waveforms are not defined (since there are multiple paths for the current to flow) and thus contain undesired and uncharacteristic harmonics. The inverter pattern must ensure that there is always one and only one path for the dc link inductor current.

The pattern must also ensure that the output line currents have the same waveform and that each current has a phase difference of 120° with respect to the other two. Moreover, the pattern should contain half-wave and quarter-wave symmetry. Balanced and symmetrical line currents ensure that no even or triplen harmonics are fed to the load.

2.3. The autosequentially commutated inverter in the six step mode of operation

It was mentioned in Chapter 1 that the ASCI got its name from the fact that when the thyristors were fired in a certain sequence, then commutation took place automatically. In this sequence, each of the thyristors T1 to T6 was fired in order once in every period at 60° intervals, and kept on for 120°. This "six-step" method of operating the ASCI produced output currents that were made up of two pulses of 120° width - one positive and one negative. It can be seen in Fig. 2.1 that the line currents were symmetrical and well-defined, thus satisfying the general rules for CSI

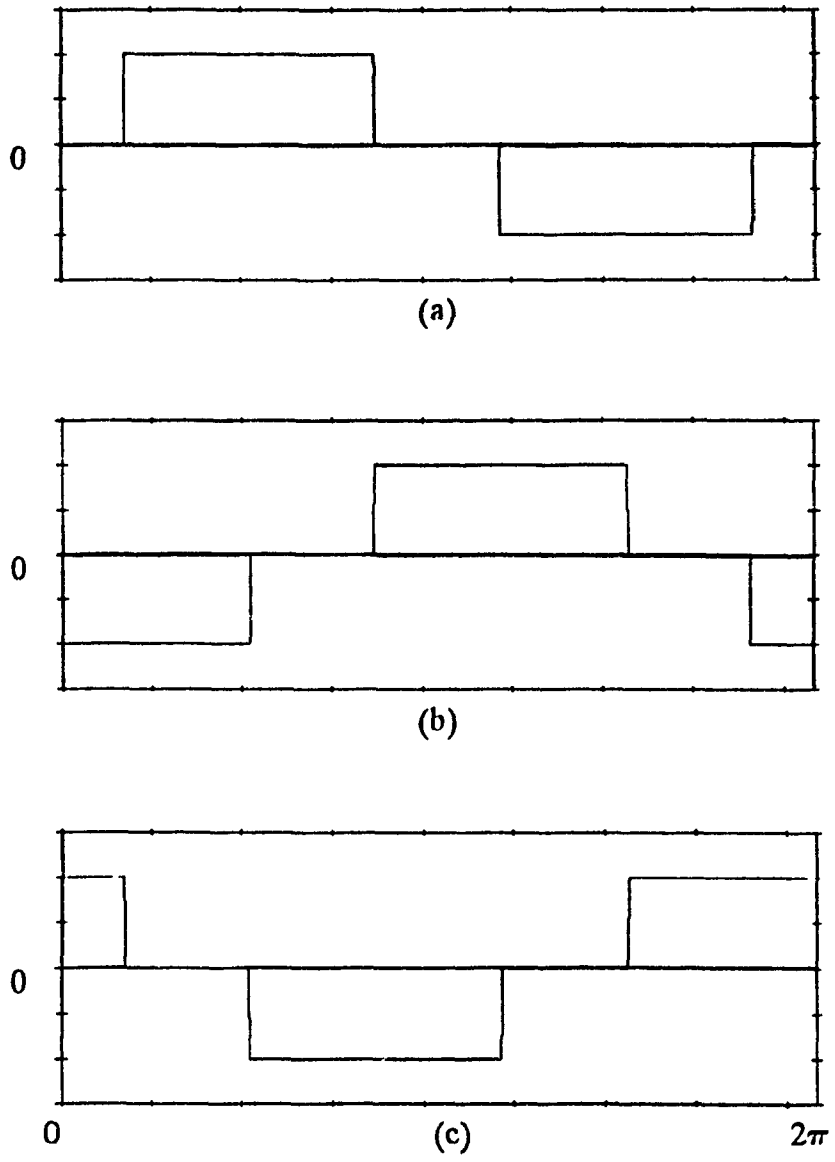


Fig. 2.1. ASCI output line currents (a) Phase A. (b) Phase B. (c) Phase C.

patterns .

The line current for each phase can be expressed as a Fourier series as

$$I(t) = \sum_{i=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \qquad (2.1)$$

where

$$a_n = \frac{1}{\pi}\int_0^{2\pi} I(t) \cos n\omega t \, d\omega t \qquad (2.2)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} I(t) \sin n\omega t \, d\omega t \qquad (2.3)$$

Since each line current has half-wave symmetry and quarter-wave symmetry, there are no even harmonics and

$$a_n = 0 \qquad (2.4)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} I(t) \sin n\omega t \, d\omega t \qquad (2.5)$$

The line current for phase A can be expressed as

$$b_n = \frac{4 I_{dc}}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \sin n\omega t \, d\omega t \qquad (2.6)$$

because of the symmetries, and this gives

$$b_n = \frac{2\sqrt{3}}{n\pi} I_{dc} \qquad (2.7)$$

where n is odd. If the fundamental line current component I_1 has an amplitude of then the amplitude of any harmonic I_n with respect to I_1 is

$$I_1 = \frac{2\sqrt{3}}{\pi} I_{dc} \tag{2.8}$$

$$I_n = \frac{I_1}{n} \tag{2.9}$$

Although for many years the standard method of operation for an ASCI in induction motor drives was the six-step mode, there were several disadvantages to operating the ASCI in this manner. Most of these were due to the presence of large low-order harmonics in the line currents (i.e. the fifth harmonic was 20% of the fundamental component) which caused the following problems:

1) The motor had severe torque pulsations at low speeds that caused the shaft to cog.
2) The motor had to be derated because of thermal loading.
3) The efficiency of the motor at light loads was poor. [22]

It was the need to reduce and eliminate the low frequency harmonics that led to the development of pulsewidth modulation (PWM) patterns for the ASCI and then for the PWM CSI.

2.4. PWM techniques

2.4.1. Introduction

When PWM techniques for CSIs were first developed in the late 1970's and early 1980's [23]-[26], this was done by cutting out pulses from the 120° wide line

current pulses and redistributing them to the other phases. This, however, meant that no PWM could be done in the center 60° of each half-cycle and the patterns that were implemented on the CSI had to be fixed since any attempt to modify them online could have violated the general inverter pattern rules. As a result, PWM patterns for CSIs were generally restricted to the following two which are examined in this section:

1) Selective harmonic elimination
2) Trapezoidal PWM

The result of allowing PWM within the center 60° of each half-cycle can be seen in Fig. 2.2. Fig. 2.2(a) shows an output line current having PWM in the center 60° regions while Fig. 2.2(b) and (c) show the appearance of unwanted (circled) pulses on the other two phases. These pulses must appear on the line currents because the pulses that have been cut out of the center 60° blocks of the current in (a) must be shifted to another phase to satisfy the constraint that there always be a path for current to flow through the inverter and the load. This causes the line currents to have more and larger harmonics than they would have if the pulses did not appear.

2.4.2 Selective harmonic elimination

Selective harmonic elimination (SHE) was first proposed for voltage source

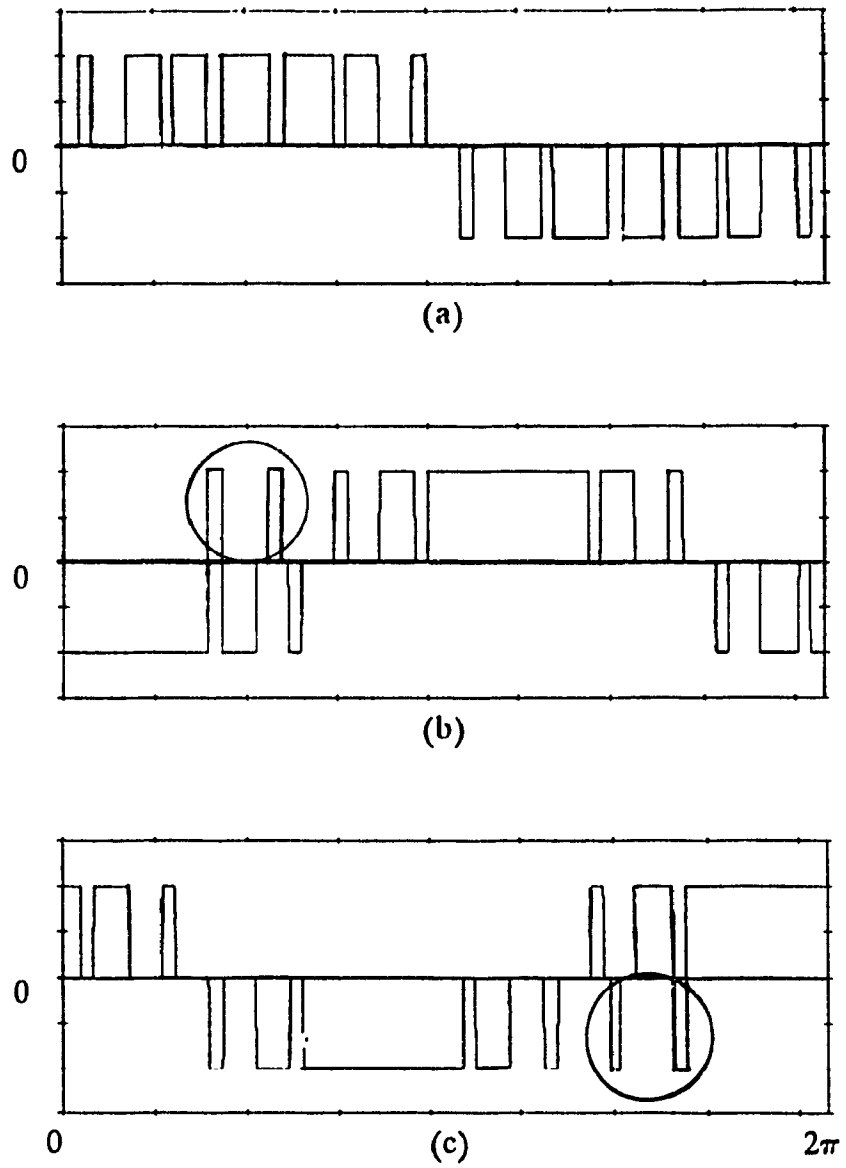


Fig. 2.2. PWM output line currents with unwanted pulse problem: (a) Phase A. (b) Phase B. (c) Phase C.

inverters by Patel and Hoft [27], then was later adapted for CSIs. The line current waveform produced with this technique (Fig. 2.3) has no PWM in the center 60° blocks and contains several symmetries - the 120° to 180° range is a mirror image of the 0° to 60° range, and the 30° to 60° range is an inverse mirror image of the 0° to 30° range. Using this technique, undesired harmonics can be eliminated from the line current by deriving its Fourier series and calculating the switching angles that set the magnitude of the undesired harmonics to zero. Once these angles are known, then the position and width of the pulses in the 0° to 30° range can be determined and the rest of the pattern can be constructed using the symmetries. The procedure to calculate the switching angles is as follows.

The line current waveform can be expressed as

$$I(t) = \sum_{i=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \qquad (2.10)$$

where

$$a_n = 0 \qquad (2.11)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} I(t) \sin n\omega t \, d\omega t \qquad (2.12)$$

because of half-wave and quarter wave symmetry. If k is defined as

$$k = \frac{N_p - 1}{2} \qquad (2.13)$$

where N_p is the number of pulses per half-cycle, then equ. 2.12 can be expanded as

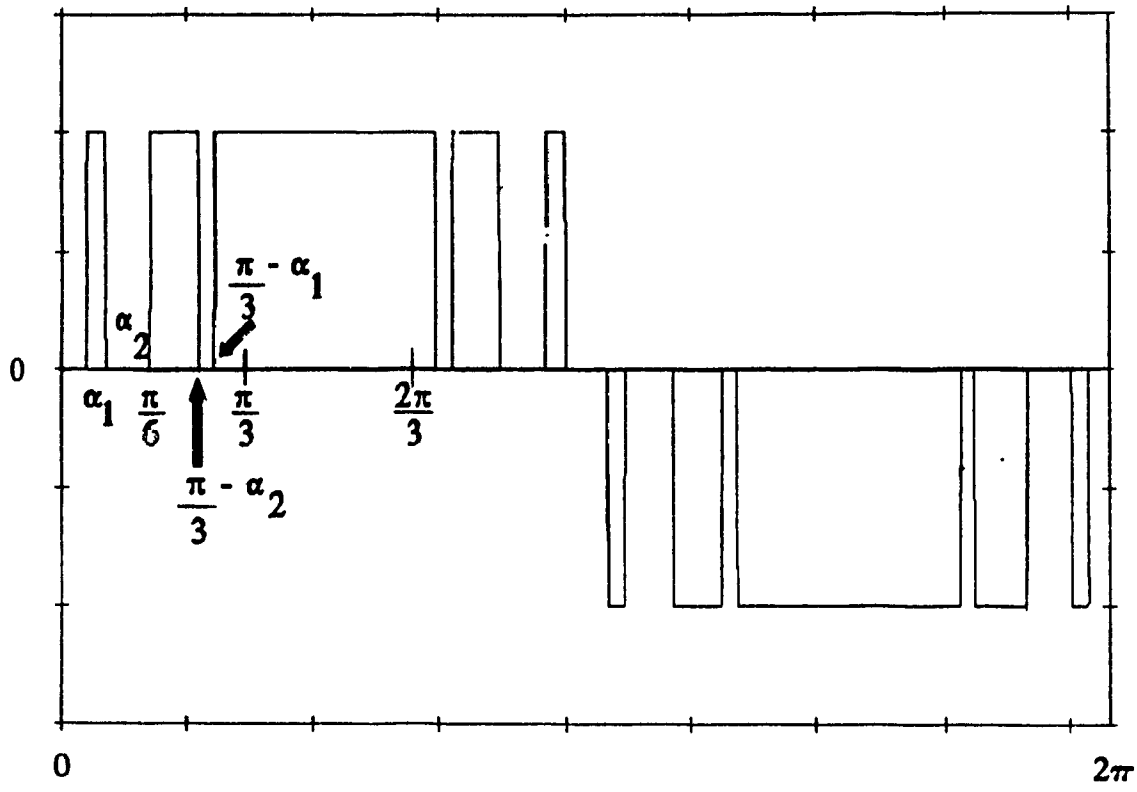


Fig. 2.3. A typical selective harmonic elimination pattern.

$$b_n = \frac{4I_{dc}}{\pi}\left(\int_{\alpha_1}^{\alpha_2}\sin n\omega t\, d\omega t + \ldots \int_{\alpha_k}^{\frac{\pi}{6}}\sin n\omega t\, d\omega t + \int_{\frac{\pi}{3}-\alpha_k}^{\frac{\pi}{3}-\alpha_{k-1}}\sin n\omega t\, d\omega t + \ldots \int_{\frac{\pi}{3}-\alpha_1}^{\frac{\pi}{2}}\sin n\omega t\, d\omega t\right) \tag{2.14}$$

when k is odd or

$$b_n = \frac{4I_{dc}}{\pi}\left(\int_{\alpha_1}^{\alpha_2}\sin n\omega t\, d\omega t + \ldots \int_{\alpha_{k-1}}^{\alpha_k}\sin n\omega t\, d\omega t + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}-\alpha_k}\sin n\omega t\, d\omega t + \ldots \int_{\frac{\pi}{3}-\alpha_1}^{\frac{\pi}{2}}\sin n\omega t\, d\omega t\right) \tag{2.15}$$

when k is even. If equ. 2.16

$$\int_{\theta_1}^{\theta_2}\sin n\omega t\, d\omega t = \frac{1}{n}(\cos n\theta_1 - \cos n\theta_2) \tag{2.16}$$

is plugged into 2.14 and 2.15 then they can be written as

$$b_n = \frac{4I_{dc}}{\pi}\left(\cos(n\alpha_1) + \cos\left[n\left(\frac{\pi}{3}-\alpha_1\right)\right] - \cos(n\alpha_2) - \cos\left[n\left(\frac{\pi}{3}-\alpha_2\right)\right] + \ldots + \cos(n\alpha_k) + \cos\left[n\left(\frac{\pi}{3}-\alpha_k\right)\right] - \cos\left(n\frac{\pi}{6}\right)\right) \tag{2.17}$$

when k is odd or

$$b_n = \frac{4I_{dc}}{\pi}\left(\cos(n\alpha_1) + \cos\left[n\left(\frac{\pi}{3}-\alpha_1\right)\right] - \cos(n\alpha_2) - \cos\left[n\left(\frac{\pi}{3}-\alpha_2\right)\right] + \ldots - \cos(n\alpha_k) - \cos\left[n\left(\frac{\pi}{3}-\alpha_k\right)\right] + \cos\left(n\frac{\pi}{6}\right)\right) \tag{2.18}$$

when k is even.

If k switching angles are derived for a pattern having N_p pulses per half-cycle using equ. 2.17 or 2.18, then k harmonics can be eliminated. For example, if a pattern has five pulses per half-cycle, then two switching angles can be calculated.

If the fifth and seventh harmonics are to be eliminated then the appropriate equations are

$$\cos(5\alpha_1) + \cos[5(\frac{\pi}{3} - \alpha_1)] - \cos(5\alpha_2) - \cos[5(\frac{\pi}{3} - \alpha_2)] + \cos(5\frac{\pi}{6}) = 0 \quad (2.19)$$

$$\cos(7\alpha_1) + \cos[7(\frac{\pi}{3} - \alpha_1)] - \cos(7\alpha_2) - \cos[7(\frac{\pi}{3} - \alpha_2)] + \cos(7\frac{\pi}{6}) = 0 \quad (2.20)$$

These transcendental equations can be solved by using a numerical method such as the Newton-Raphson method, and the switching angles α_1 and α_2 can be obtained.

Although SHE is an improvement over the ASCI six-step mode pattern, the number of harmonics that can actually be eliminated with this method are few. The reason for this is that the rigid symmetrical constraints placed on the pattern limit the switching angles that can actually be derived to the 0° to 30° range. If it was desired to eliminate many harmonics, then the pulses in this region - thus the pulses in the rest of the pattern - would be so thin that the inverter switches would not have enough time to switch on and off properly and the output line currents would be distorted. Therefore, SHE is generally used to eliminate up to four harmonics unless the frequency is very low; only then can more harmonics be eliminated as the pulses are wider. Since only four harmonics can be eliminated, these must be selected so that at least one corresponds to the resonance frequency, which is dependent on the value of the filter capacitors and the motor inductances. If the harmonic closest to the resonance frequency is not eliminated, then it will be

amplified thus worsening the harmonic content of the output currents.

2.4.3. Trapezoidal PWM

Trapezoidal PWM (TPWM) is a carrier PWM technique in which a trapezoidal modulating waveform is compared with a triangular carrier wave to produce a switching function from which the gating signals of an inverter leg are obtained (Fig. 2.4) [26],[28]. It can be seen that the triangular waveform is suppressed in the center 60° block of each half-cycle to avoid any PWM in this region.

The PWM pattern is dependent on two parameters, the modulation index, M and the number of pulses per half-cycle, N_p. M is the amplitude ratio of the modulating waveform, A, to the carrier waveform, B, and controls the width of the pulses. N_p is determined by the relationship between the frequency of the carrier to that of the modulating waveform. Since there is no PWM performed on the center 60° block of each half-cycle, the technique is extremely limited in the number of harmonics that can actually be eliminated; however, the magnitudes of selected harmonics can be minimized with the appropriate value of M and N_p. For example, if $M = 0.82$ and $N_p = 7$ then the fifth harmonic is eliminated but there is a substantial seventh harmonic; if M is set to 1 then the seventh harmonic is reduced but the fifth becomes larger [26]. Although it can be calculated online with analog devices, the pattern that is used must be predetermined in some way because there

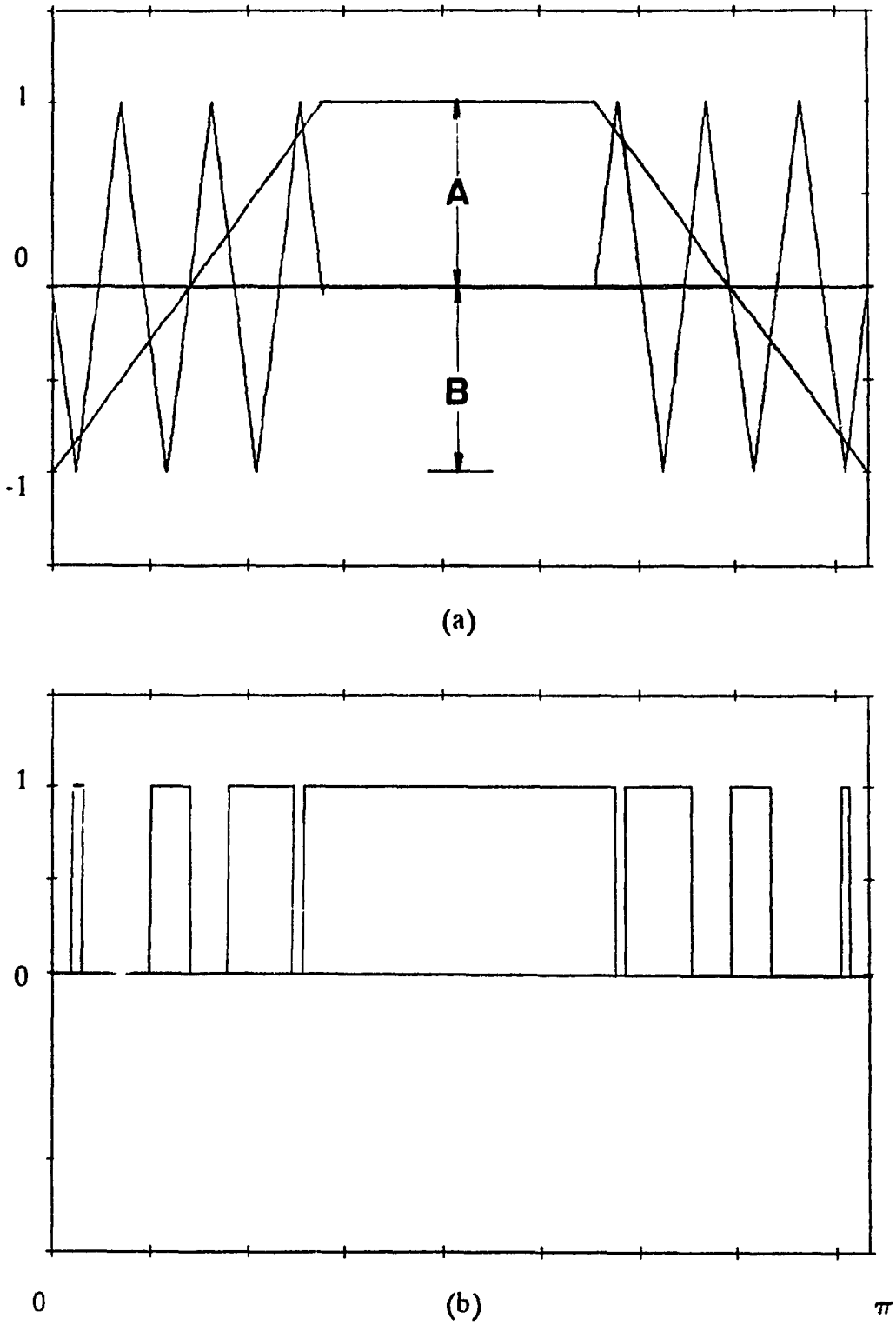


Fig. 2.4. (a) TPWM scheme. (b) TPWM pattern.

is no direct relationship between the harmonic content of the line currents and M and N_p. For TPWM, the switching angles of many switching functions - each with its own combination of M and N_p - must be derived first, then Fourier analysis must done so that the harmonic content of all the derived switching functions can be compared. This is in contrast to SHE where the desired harmonics to be eliminated are selected first, and then the pattern is constructed.

As with SHE, the harmonics near the resonant frequency should be the ones that are reduced. TPWM should be used whenever the inverter fundamental frequency is low since N_p can be high and more line current harmonics can be reduced or eliminated than with SHE. SHE, however, should be used when the inverter is operated at higher frequencies because it can eliminate more low-order harmonics as N_p for TPWM must be low.

2.5. Dc bus short-circuiting

2.5.1. Harmonic elimination

The two PWM techniques that have been presented so far are limited in the number of line current harmonics that they can eliminate because of the lack of PWM in the center 60° region of each half-cycle of the pattern. As was shown earlier, PWM in this region would result in the appearance of unwanted line current pulses. These pulses would not appear if it were possible to make all three line currents zero while providing a path for the dc link inductor current to flow through

the inverter whenever PWM in the center 60° region was required. This can be done if both switches of an inverter leg are made to be on at the same time so that the dc bus is short-circuited and the dc link current bypasses the load [29]-[30]. Inverter patterns that allow for the short-circuiting of the dc bus to take place while satisfying the constraint that there always be only one top switch and one bottom switch on at the same time can be designed.

Since short-circuiting the dc bus allows PWM in the center 60° region to appear, the number of PWM techniques that can be used in a CSI are substantially increased. Moreover, techniques that have been used previously in VSIs can be adapted for use in CSIs. For example, sinusoidal PWM - a common VSI carrier PWM technique - can be converted to a CSI technique as shown in Fig. 2.5. In Fig. 2.5(a), a sinusoidal modulating wave is compared with a triangular carrier wave and the two-level switching function shown in Fig. 2.5(b) is produced; this function corresponds to the line-neutral output voltage and thus can be considered as a "line-neutral" function. If this procedure is done for each phase then three line-neutral switching functions will be produced, SW_A, SW_B, and SW_C. If these switching functions are subtracted from one another then three three-level "line-line" switching functions will be produced, SW_{AB} (Fig. 2.5(c)), SW_{BC}, and SW_{CA}. Each switching function corresponds to a VSI line-line output voltage, but it can also correspond to a CSI line current since this too is a three-level waveform. Therefore, VSI PWM techniques, in general, can be adapted for use in CSIs if the two-level VSI switching functions are converted to three - level CSI switching functions from which the

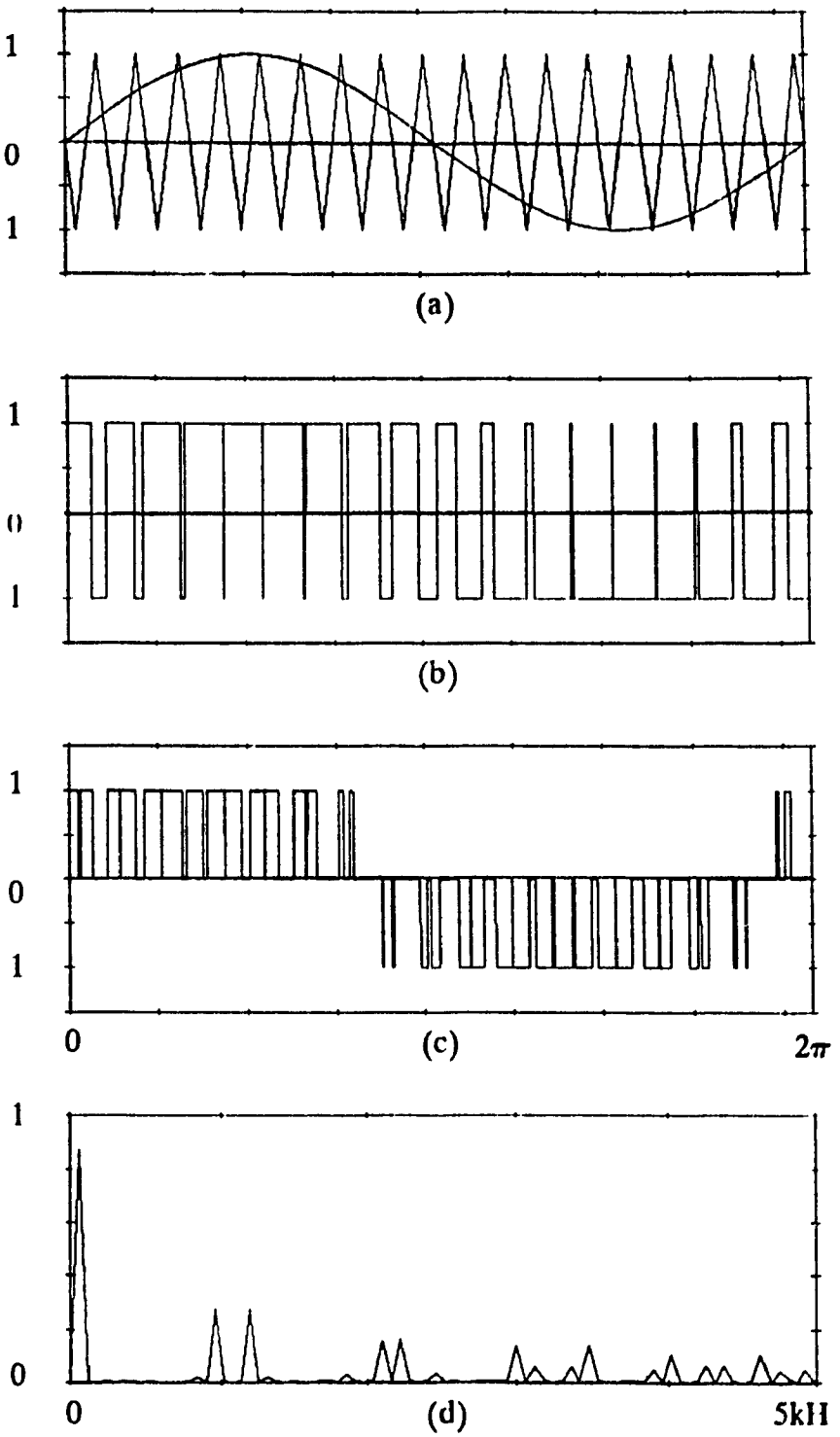


Fig. 2.5. Sinusoidal PWM for 60 Hz fundamental. (a) SPWM scheme. (b) Line-neutral waveform. (c) Line-line waveform (CSI pattern). (d) Fourier spectrum of line-line pattern.

appropriate inverter switch gating signals can be obtained.

2.5.2. Amplitude control

Another benefit that can be gained by short-circuiting the dc bus at selected time intervals is an improvement in the dynamic response of the CSI (the time it takes for the load currents to change their amplitude once the command for change has been given) since it is possible to change the fundamental component of the output currents at the inverter. Although a discussion about dynamic response is postponed until Chapter 3, it will be shown here how the fundamental component can be controlled by the inverter pattern.

The basic principle of keeping the dc link inductor current constant while using short-circuiting or shoot-through pulses in the inverter pattern to change the fundamental component of the line currents was first proposed by Deng et al. and by Biswas et al. in [14] and [15] respectively. In [14], an ASCI was operated in the six-step mode and the amplitude of the fundamental component was controlled by placing notches in the output line currents then varying the width of the notches - the wider the notches were, the more the amplitude of the fundamental line current component was reduced. The principle of "notch control" is shown in Fig. 2.6. where the inverter switch pairs are T1 and T4, T3 and T6, and T5 and T2. As can be seen, the position and width of the notches are determined by how the switches are fired - both switches of an inverter leg are on at the same time whenever it is

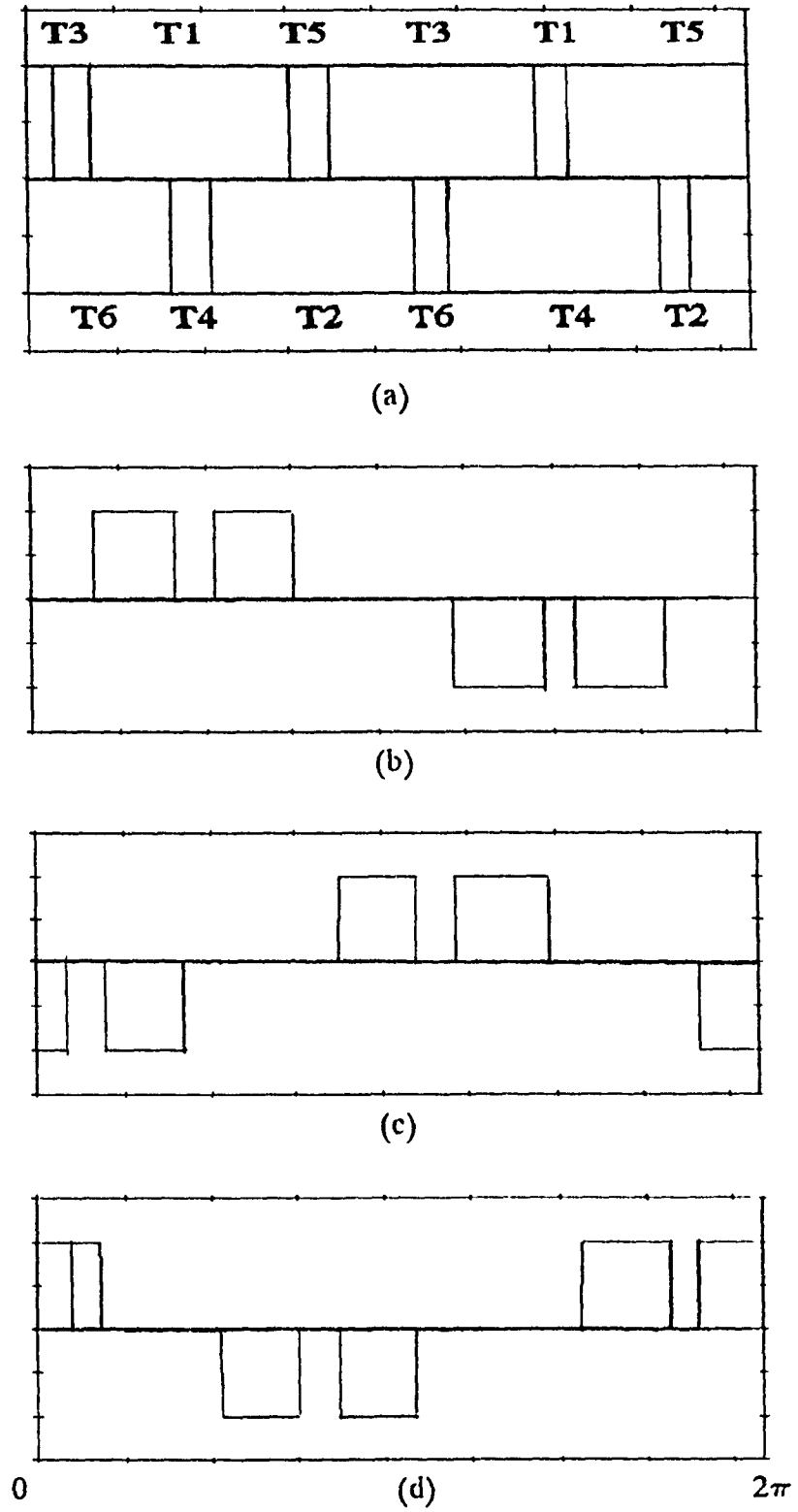


Fig. 2.6. (a) Notch control firing sequence. (b)-(d) Output line currents.

desired to place a notch in the line currents. The width of the notches is equal to the short-circuiting interval.

Although notch control made amplitude control possible, the technique had a drawback - since it was implemented on an ASCI operating in the six-step mode, the harmonic content of the line currents was poor. In [15], amplitude control was implemented on an ASCI using a technique that could have been called "equal PWM" (EPWM) as a PWM pattern with an odd number of equal width pulses per half-cycle was used. The fundamental component was controlled by varying the width of the pulses using short-circuiting as with notch control; however, a better harmonic content was obtained with EPWM although low-order harmonics were still present.

2.6. Selective harmonic elimination with PWM in the center 60° region

It was shown in section 2.4.2 that the number of harmonics that can be eliminated using SHE is limited because the symmetrical constraints placed on the pattern restrict the switching angles that can be calculated to the 0° to 30° range. A new, less restrictive pattern (Fig. 2.7) can be obtained by short-circuiting the dc bus and having PWM in the center 60° region [31]-[32]. Like the previous SHE pattern, the 120° to 180° is the mirror image of the 0° to 60°, however, the center 60° interval is obtained by folding the first and last 60° intervals around the 60° and 120° points respectively; this folding ensures that the shoot-through pulses do not affect

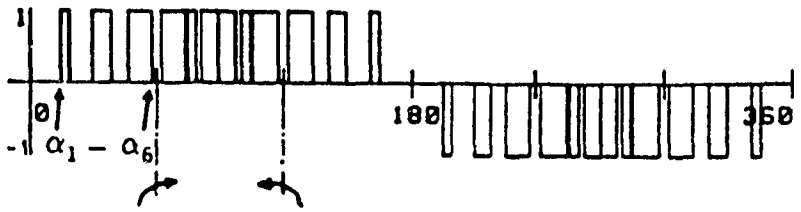


Fig. 2.7. SHE pattern with PWM in the center 60° region of each half-cycle.

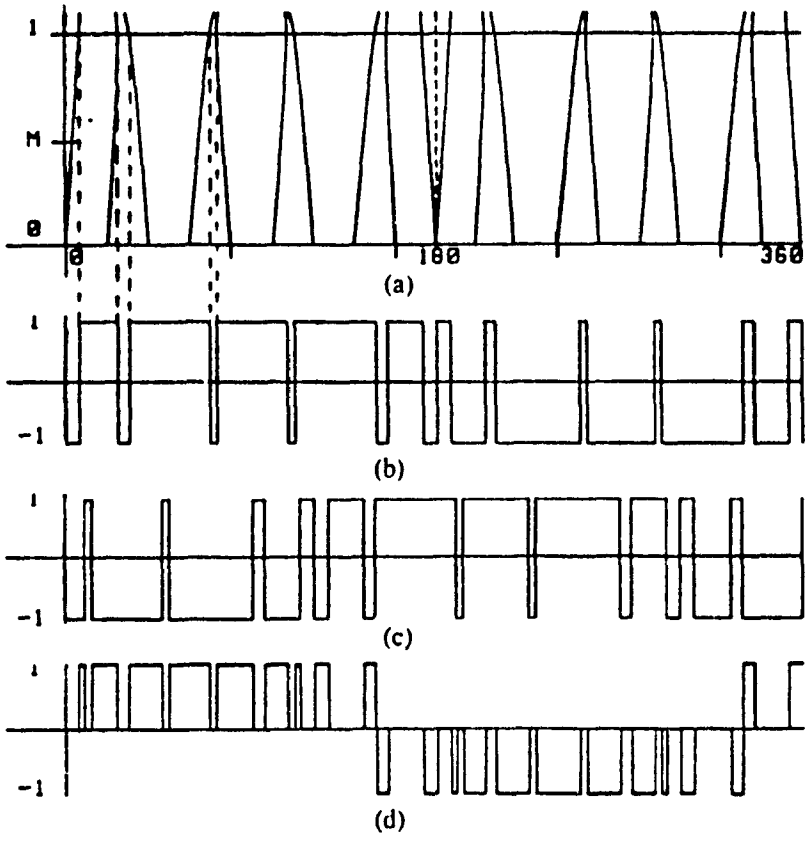


Fig. 2.8. (a) PWM function for variable modulation index control. (b) Two-level switching function $F_1(t)$. (c) Two-level switching function $F_2(t)$. (d) PWM pattern for CSI.

the quarter-wave symmetry of the pattern. Unlike the pattern presented in section 2.4.2, the 30° to 60° range is not the mirror image of the 0° to 30° range thus the range of calculated switching angles is expanded to the 0° to 60° range. Therefore, the number of undesired harmonics that can be eliminated is increased (from 4 to about 20) because the pulses derived from the switching angles are wide enough so that the inverter switches have time to turn on and off properly. The switching angles can be calculated by using the same procedure as the one shown in section 2.4.2.

In [16], Enjeti et al presented a method of amplitude control that was implemented on a PWM CSI and used this SHE pattern. In this case, the appropriate switching angles were derived for various values of ac gain (the ratio of the peak value of the fundamental component to that of the unfiltered pulses) for the SHE pattern and the pattern shown in Fig. 2.8(a) was obtained. By comparing this function with a dc signal (whose value can be considered as the modulation index), a two-level function, $F_1(t)$ (Fig. 2.8(b)) was produced. Fig. 2.8(c) shows another two-level function and Fig. 2.8(d) shows the PWM pattern for a CSI.

It can be seen in Fig. 2.8 that if the level of the dc signal in (a) is varied then this will affect the width and number of the pulses in (b) and (c) which in turn will affect the width and number of the pulses in (d) - similar to the way notch control affected the ASCI line currents. Since the amplitude of the fundamental component of the line current is controlled by the level of the dc signal or modulation index, this method of amplitude control can be called variable modulation index control.

2.7. Sinusoidal PWM and its variations

Sinusoidal PWM (SPWM) is a carrier PWM technique that has PWM in the center 60° region of each half-cycle unlike the other carrier PWM technique shown in this chapter, TPWM. The presence of PWM in this region gives SPWM the following advantages over TPWM:

(1) It is easier to control the harmonic content of the output line current when SPWM is used. Unlike TPWM, a suitable pattern - one with no low-order harmonics or harmonics near the resonance frequency - can be easily determined using SPWM because the location of the dominant (largest) harmonics is dependent on the frequency of the triangular carrier and this is easy to adjust. For example, the frequency of the carrier waveform in Fig. 2.5 is 21 times that of the modulating waveform, so that the harmonics that appear are the 19th and 23rd, which are sidebands of the 21st, and the 41st and 43rd, which are sidebands of the 42nd (2 x 21) harmonic. The 21st and the 42nd harmonics do not appear because triplen harmonics cannot appear on a balanced three-phase system. If, for some reason, it is desired to place the dominant harmonics around the 36th or xth harmonic, then all that needs to be done is to set the carrier frequency to 36 or x times that of the modulating waveform. Therefore, if the frequency of the carrier waveform is controlled independently from that of the modulating waveform (which it can be when the comparison between the two waveform is done with analog

devices), then the position of the line current harmonics can be fully controlled.

(2) Amplitude control using TPWM is limited because of the unmodulated center 60° block. However, it is possible to control the amplitude of the fundamental component of the line current with SPWM using variable modulation index control as described in section 2.6.2. This amplitude is directly proportional to the modulation index so that if it is desired to reduced it to one-half or one-quarter of its original value, then it can be done by making M equal to 0.5 or 0.25.

SPWM does have one disadvantage over TPWM and that is that its ac gain is lower, 0.866 vs. 1; therefore, more current must be fed to the inverter to get the same output with SPWM than with TPWM. Techniques such as the modified SPWM (MSPWM) and the third-harmonic injection techniques (3HIPWM) were derived to improve the ac gain of SPWM [33]. In the MSPWM technique (Fig. 2.9), only the first and last 60° intervals per half-cycle of the line-neutral switching functions are directly defined by the intersections of the modulating and carrier waveforms while the 60° to 120° range is obtained by folding the first and last 60° intervals around the 60° and 120° points respectively. This technique, however, is difficult to implement using analog devices and thus is rarely used. In the 3HIPWM technique (Fig. 2.10), the modulating waveform has been modifed so that it is

$$y = 1.15\sin\omega t + 0.19\sin 3\omega t \qquad (2.21)$$

and the pattern is obtained in the same manner as SPWM. It is important to note

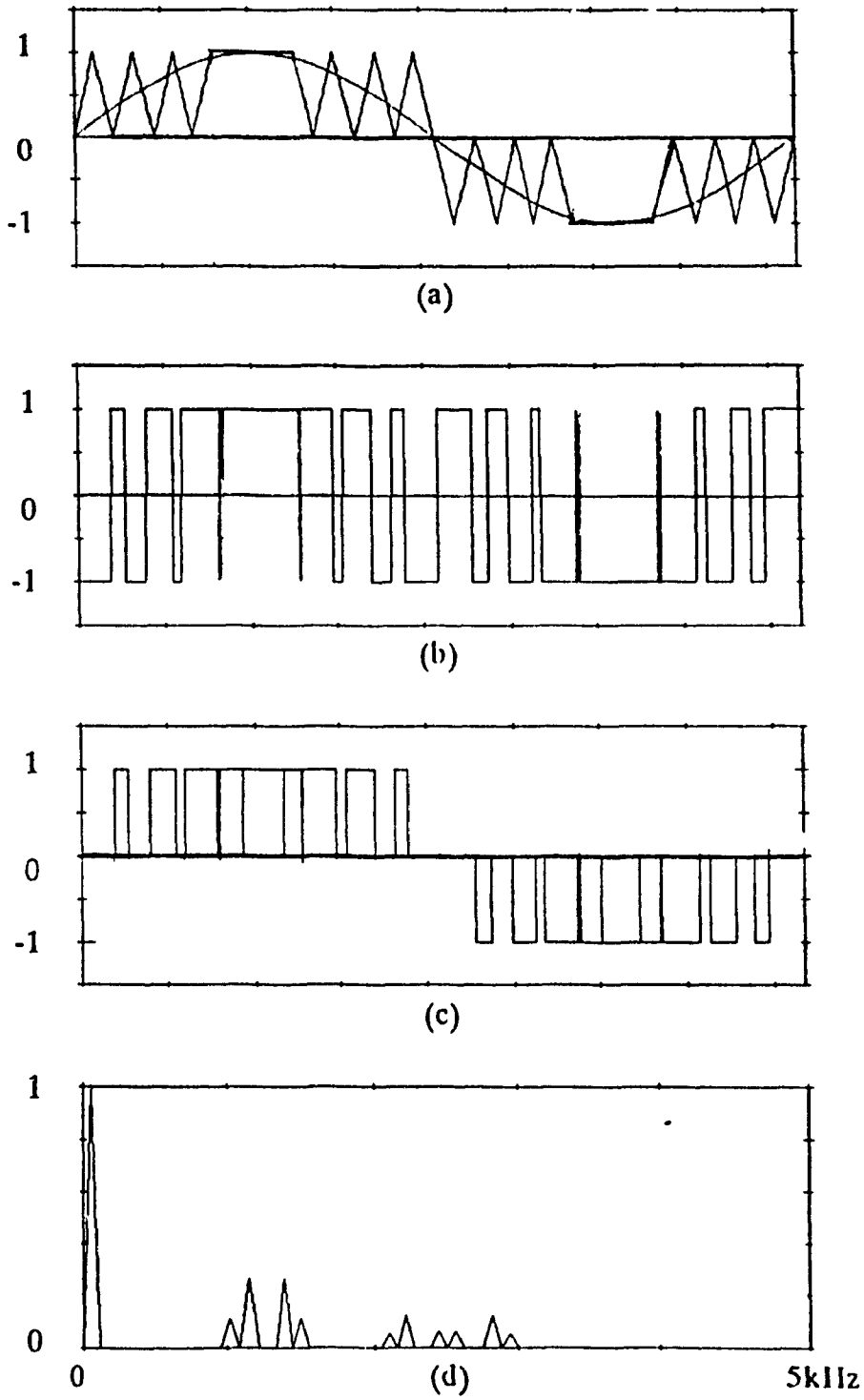


Fig. 2.9. Modified SPWM for 60 Hz fundamental (a) MSPWM scheme. (b) Line-neutral waveform. (c) Line-line waveform (CSI pattern). (d) Fourier spectrum of line-line waveform.

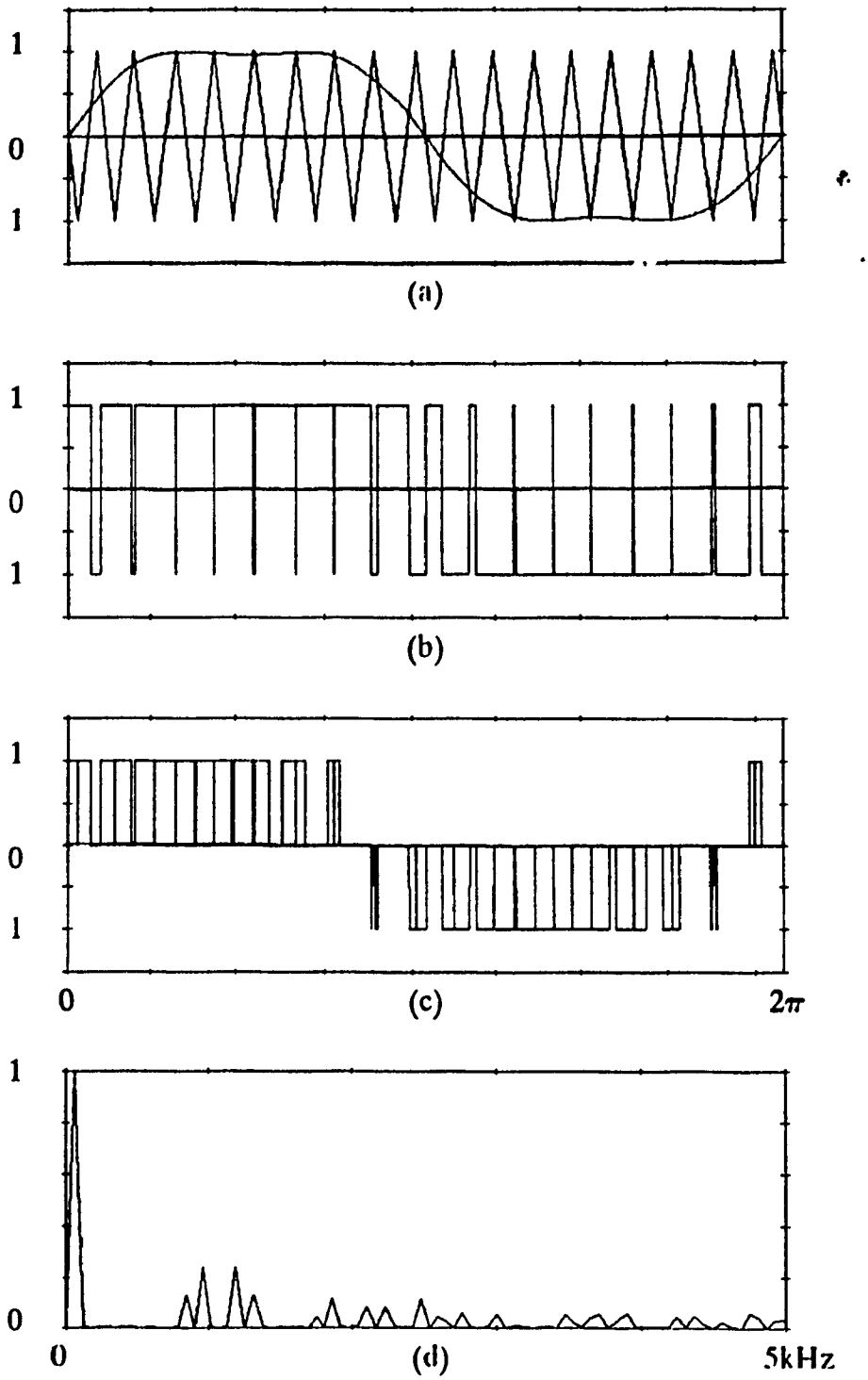


Fig. 2.10. Third harmonic injection SPWM for 60 Hz fundamental (a) 3IIIPWM scheme. (b) Line-neutral waveform. (c) Line-line waveform (CSI pattern). (d) Fourier spectrum of line-line waveform.

that the ac gain of both of these techniques is increased to unity but at the cost of making the overall harmonic content worse.

2.8. Operation of CSI with an auxiliary switch

It is very difficult to implement carrier PWM patterns with shoot-through pulses using analog devices because the inverter switch gating signals cannot be obtained directly from the pattern without violating the general rules for CSI operation. Some procees must be carried out to construct the signals from the pattern. Since it is difficult to do this with analog devices, carrier PWM techniques can only be implemented by storing the gating signals in an EPROM as is done with SHE techniques. The use of an EPROM, however, takes away the benefits of using carrier PWM techniques because:

(1) An EPROM can only store a limited number of PWM patterns.

(2) If an EPROM is to be used then it is preferable to use SHE because it has a lower switching frequency. [31]

The benefits of carrier PWM techniques are best obtained when they are implemented using analog devices. In order to get these benefits, an auxiliary switch must be implemented in the dc link, external to the inverter because the gating signals of the switches can be easily derived from the pattern as is shown in Fig. 2.11 for typical CSI pattern. Fig. 2.11(a) shows the three-level switching function and Fig. 2.11(b) shows the gating signals for the top switch and bottom switch of an

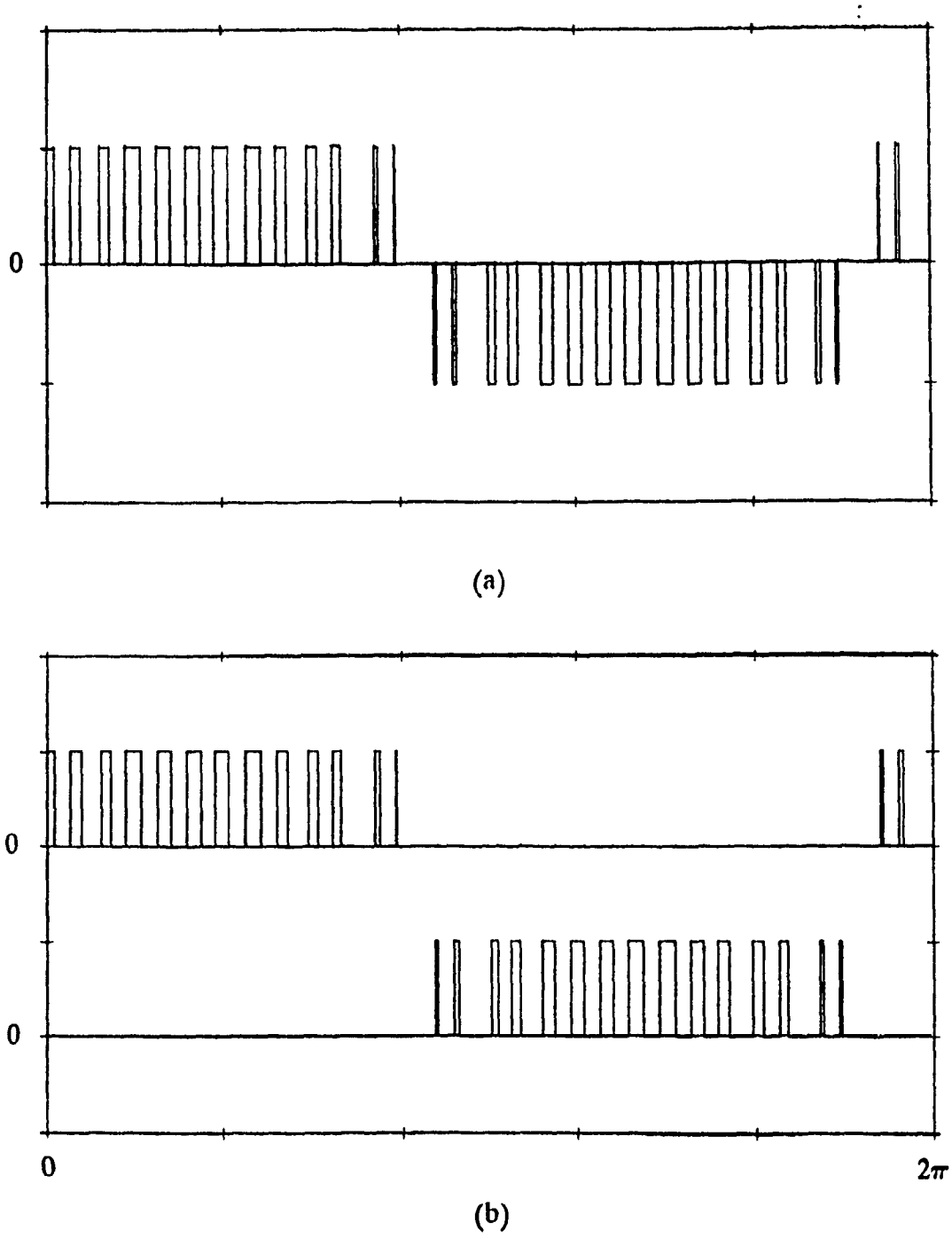


Fig. 2.11. (a) Typical CSI pattern with PWM in the center 60° region of each half-cycle. (b) Gating signals for the top and bottom switch of an inverter leg.

inverter leg - note that these signals have been obtained simply by separating the top half and bottom half of the switching function.

Obtaining the inverter switch gating signals in this manner, however, means that the inverter does not always provide a path for current; therfore, the gating of the auxiliary switch must be synchronized with that of the inverter switches to ensure that current will flow through the switch when it cannot flow through the inverter. The auxiliary switch gating signal for a typical CSI carrier PWM pattern is shown in Fig. 2.12 along with the gating signal of the top three inverter switches. It can be seen that the auxiliary switch is gated whenever the top switches are not thus allowing the dc link current to bypass the inverter and the load. As a result, the auxiliary switch allows carrier PWM techniques requiring shoot-through pulses to be implemented using analog devices since the gating signals can be obtained directly from the pattern without violating the general rules for CSI patterns

2.9. Conclusion

It has been shown that the presence of low-order harmonics in the line currents produced by the ASCI six-step mode of operation made the development of PWM techniques necessary. Initially, the patterns that could be used in a CSI were restricted to those with no PWM in the center 60° of each half-cycle. Two standard PWM techniques have been presented - selective harmonic elimination and trapezoidal PWM. These techniques are limited in the number of harmonics that

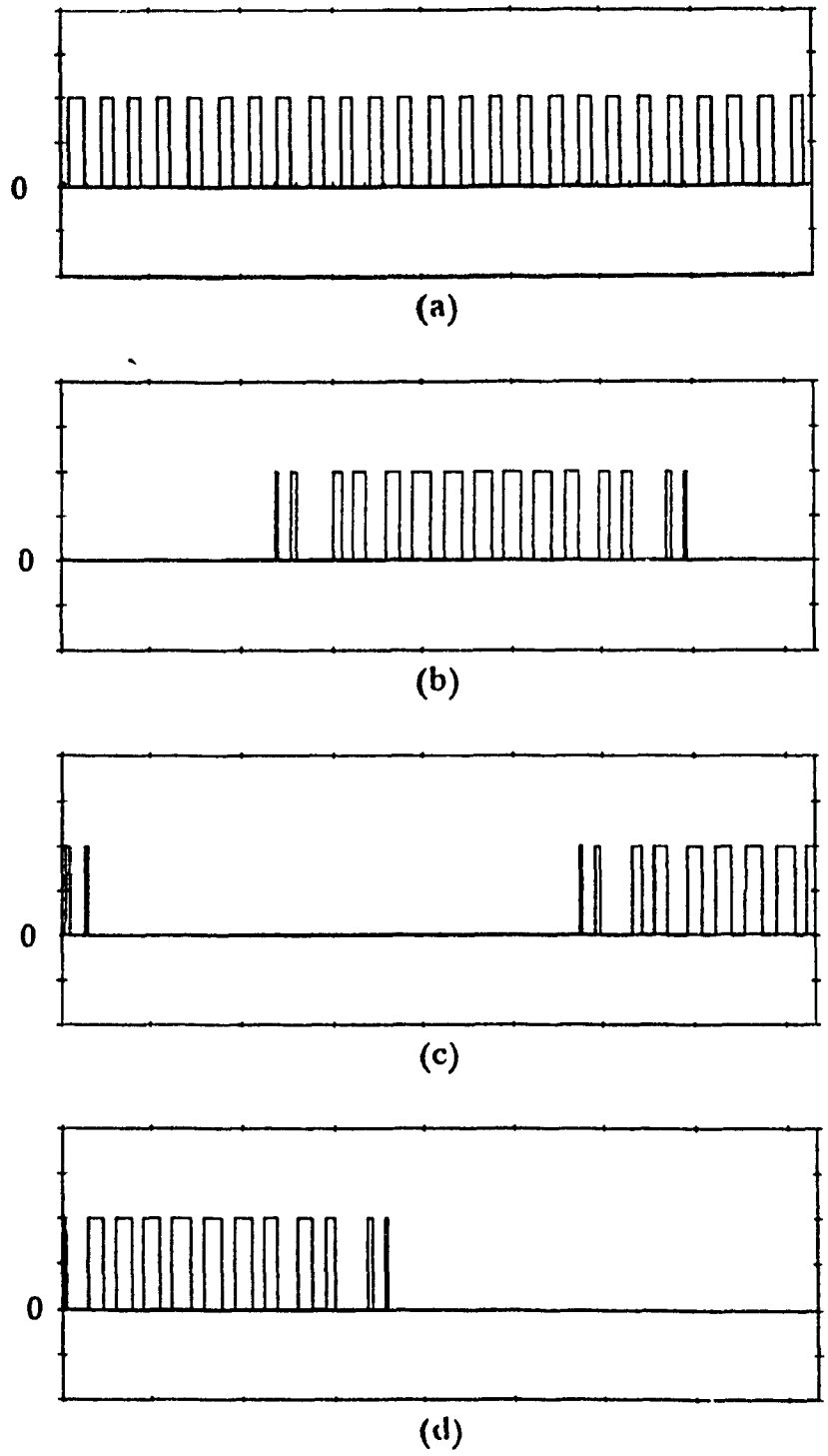


Fig. 2.12. Typical gating signals for a CSI with an auxiliary switch in the dc link (a) Auxiliary switch gating signal. (b)-(d) Gating signals for the top three inverter switches.

they can eliminate because of the absence of PWM in the center 60° region of the pattern. The technique of short-circuiting the dc bus has been shown to remove this limitation as less restrictive VSI patterns can be implemented. Short-circuiting the dc bus also allows the fundamental component of the line currents to be varied at the inverter using variable modulation index control. The use of shoot-through pulses in carrier PWM techniques means that they cannot be implemented on a conventional PWM CSI using analog devices - this negates the benefits that can be obtained with these techniques. The addition of an auxiliary switch in the dc link, external to the inverter, removes this limitation.

CHAPTER 3 - PULSEWIDTH MODULATED CURRENT SOURCE INVERTER OPERATING CHARACTERISTICS

3.1. Introduction

The need to eliminate low-order harmonics for the output line currents was emphasized in Chapter 2 since harmonic elimination results in more sinusoidal load currents which, in turn, affect the operation of the load. However, when looking at the performance of the PWM CSI, there are other factors that must be taken into consideration - factors that are dependent on the converter topology itself. In this chapter, the operating characteristics of the PWM CSI are examined beginning with the relationship between the inverter input quantites and those at the output. This is important because the modulation index and the fundamental frequency of the inverter pattern affect the level dc link inductor current needed to get a desired output and also the input power factor. Other characteristics of the PWM CSI that are examined include its dynamic response and its output voltage, which contains overvoltage spikes. Ways to improve both and thus improve the performance of the CSI are investigated. Finally, it is shown that the conventional PWM CSI has limitations, but that these limitations can be removed by modifying the topology.

3.2. Steady-state inverter relationships

The inverter in a CSI drive system can be considered as a current transformer

that converts a dc input current into three ac output line currents with its gain being dependent on the PWM pattern and the modulation index. The relationship between the quantities on the dc side of the inverter and those on the ac side can be considered if it is assumed that the inverter is lossless. Under this condition, the power at the dc bus is equal to that at the inverter output and the following equation can be obtained

$$V_{dc}I_{dc} = 3V_oI_o\cos\varphi_o \qquad (3.1)$$

where V_{dc} = inverter input voltage

I_{dc} = dc bus current

V_o = fundamental rms component of the output line-neutral voltage

I_o = fundamental rms component of output current

ϕ_o = output impedance phase angle.

If it is assumed that the ac gain of the inverter is proportional to the modulation index M by a factor $K_i(M)$ so that

$$I_o = K_i(M)\,MI_{dc} \qquad (3.2)$$

and that

$$V_o = Z_oI_o \qquad (3.3)$$

(where Z_o is the magnitude of the output impedance) then the following equation can be derived by plugging equ. 3.2 and 3.3 into equ. 3.1

$$V_{dc} = 3Z_o K_i^2(M) M^2 I_{dc} \cos\varphi_o \qquad (3.4)$$

If it is assumed that $K_i(M)$ and the load impedance are constant, then the following relationship can be obtained

$$V_{dc} \propto M^2 I_{dc} \qquad (3.5)$$

If the modulation index of the inverter PWM pattern is originally M = 1 and is decreased, and V_{dc} is not varied, then I_{dc} will rise by a factor of $1/M^2$; for example, if M is reduced from 1 to 0.5 then I_{dc} will rise to four times its original value. This means that whenever variable modulation index control is used, the rectifier output voltage (equal to V_{dc}) must be adjusted or else there will be a substantial rise in I_{dc} as can be seen in Fig. 3.1.

If it is assumed that $K_i(M)$, M and Z_o are constant for various operating points - which can be done when the impedance of the filter capacitor at fundamental frequency is large enough so that its effect on Z_o is minimal - then the following relationship can be obtained

$$V_{dc} \propto I_{dc} \cos\varphi_o \qquad (3.6)$$

where cos ϕ_o is the output power factor.

Fig. 3.2. shows the effect that the output power factor has on I_{dc} when the rectifier output voltage is not varied for the case that I_{dc} is 1 pu under rated conditions for a load having a unity power factor. It can be seen that as power factor decreases (which is the case when the inverter frequency increases), I_{dc} increases; therefore, the rectifier output voltage must be decreased in order to

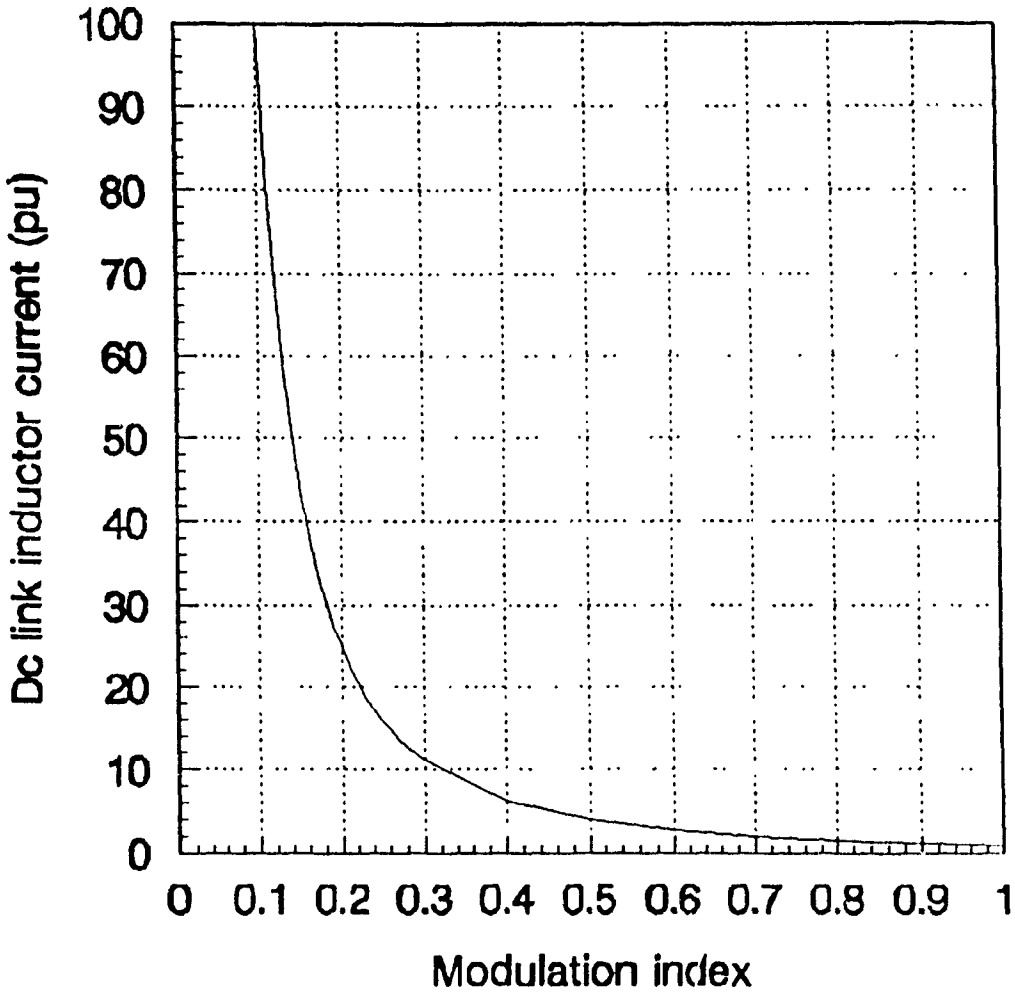


Fig. 3.1. Dc link inductor current (pu) vs modulation index when V_{dc} is constant.

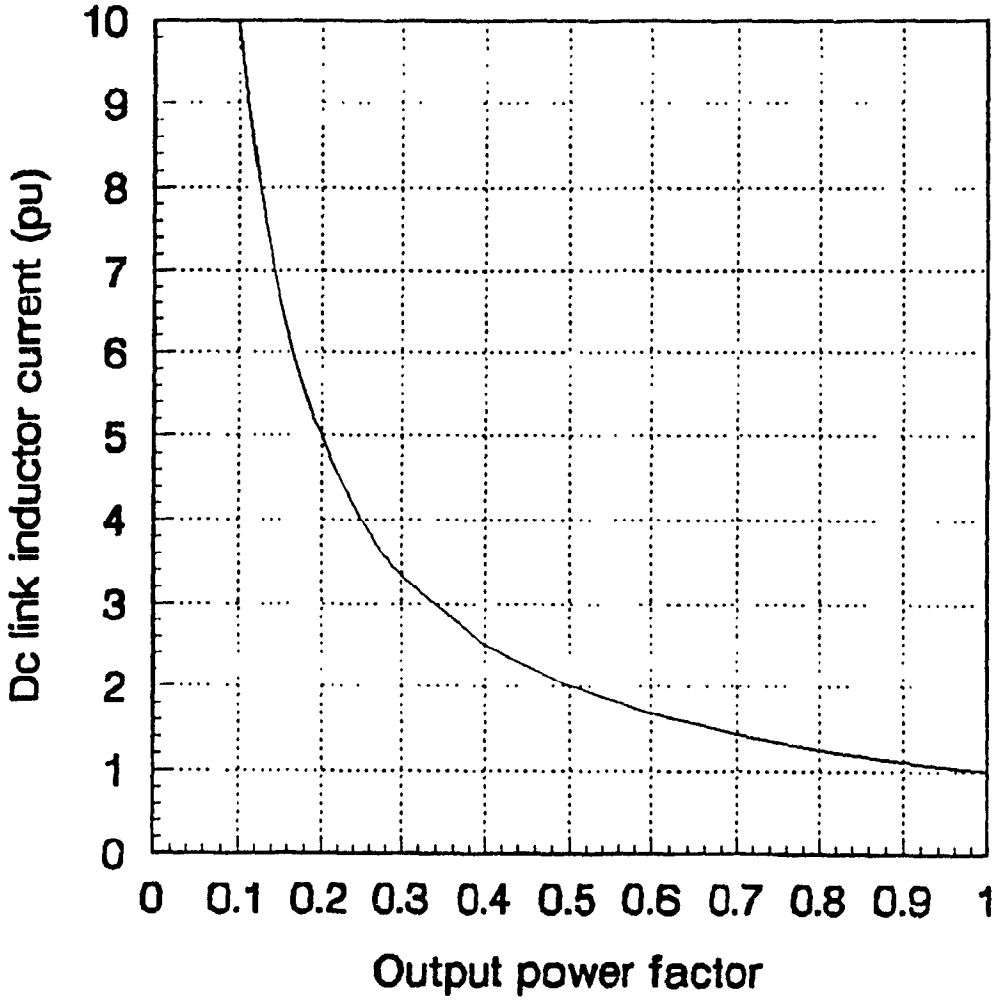


Fig. 3.2. Dc link inductor current (pu) vs output power factor when V_{dc} is constant.

prevent this rise in current from occuring.

3.3. CSI dynamic response

There are two methods by which the amplitude of the output load currents can be controlled: rectifier control and variable modulation index control. With rectifier control, the output currents are changed by varying the rectifier output voltage and this changes the dc current entering the inverter. Since a PWM CSI is usually operated with an inverter pattern that is either fixed (cannot be changed online) or has a fixed current gain, rectifier control is the standard method of controlling the amplitude of the output currents. If the dc link inductor is large, however, then the use of rectifier control results in the CSI having a slow dynamic response since it will take some time for the current (and thus the output currents) to change as the di/dt is small. When the front-end converter is a phase-controlled rectifier, a large inductor must be used to reduce the ripple on the dc link current caused by the presence of low-order harmonics such as the 6th and the 12th. In order to reduce the size of the inductor and thus improve the dynamic response, these harmonics must be reduced somehow. One way is to use a PWM rectifier as the front-end converter instead of a phase-controlled rectifier since it can be used with PWM patterns that do not produce low-order voltage harmonics on the bus. A PWM rectifier, however, must be implemented with GTOs, which are more expensive and less reliable than thyristors, and has more switching losses than the

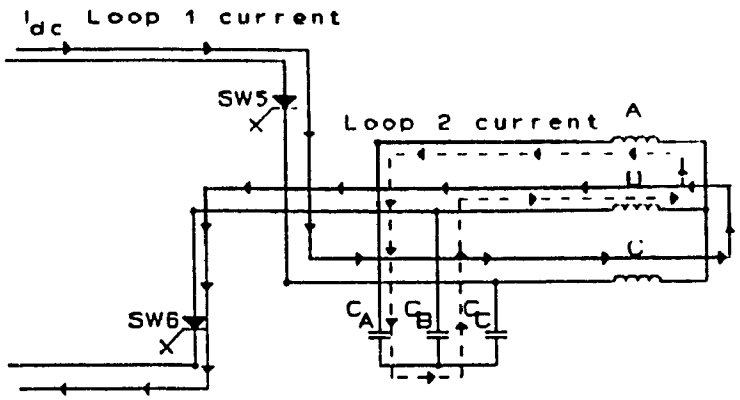
phase-controlled rectifier.

If variable modulation index control is used, then a large inductor can be used to reduce the current ripple without affecting the dynamic response because the dc link current is kept constant (by adjusting the rectifer output voltage) while the change in output current is taking place. It does not matter what the size of the inductor is provided that the CSI is set to operate so that the maximum desired load current is obtained when the rectifier output voltage (and the dc link current) is close to its maximum value and the modulation index is set to M = 1. This ensures that a fast dynamic response can be obtained over a wide range of current values. However, if it is desired for the load curents to be higher than what is normally desired then the dc link current can only be increased using rectifier control.

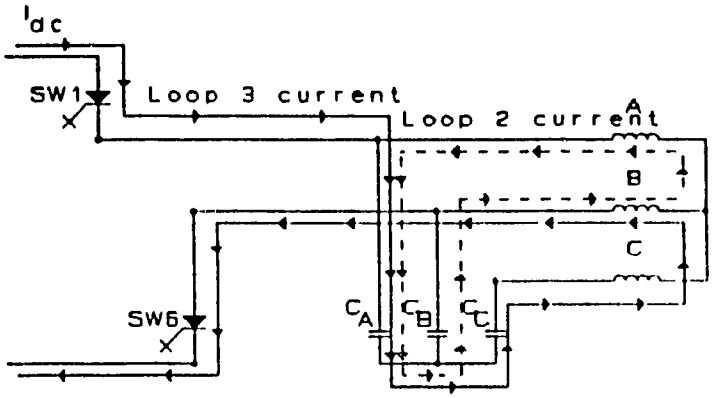
3.4. Inverter output overvoltage spikes

A problem that the CSI has had since it was first developed is the appearance of overvoltage spikes on the inverter output voltage. A novel way of suppressing these spikes was proposed by Hombu et al. in [5], and the discussion that follows is based on this paper.

The mechanism that produces inverter output voltage spikes can be shown by the following example in which the operation of the inverter is analyzed for a short interval of time $(0 - t_1)$ and the current flowing through line B during this time is assumed to be negative. Suppose that at t = 0 the inverter is shown in Fig. 3.3(a)



(a)



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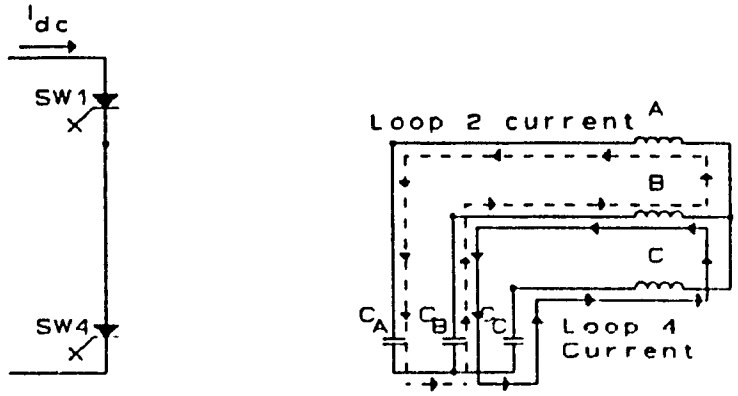


(c)

Fig. 3.3. Equivalent circuit when (a) t = 0, (b) t = t_1, (c) short-circuiting dc bus.

in which GTOs G_5 and G_6 are on and the dc link current I_d flows through a path consisting of G_5, phase C of the load, phase B of the load and G_6 (loop 1). In addition to this current, there is another current that is flowing at this time and this is the sinusoidal current of phase A of the load; this current is the result of the line current i_A being filtered and is always flowing through phase A even though i_A may be zero at the time. This current must have a path to flow through and thus flows through phase A of the load, capacitor C_A, capacitor C_B, and phase B (loop 2). This current is shown to flow in the negative direction of phase A of the load in Fig. 3.3(a).

Suppose that at $t = t_1$ the inverter is in the state shown in Fig. 3.3(b) in which G_5 has been turned off and G_1 has been turned on so that I_d has been transferred from line C to line A, and current flows through G_1, C_A, C_C, phase C of the load, phase B, and G_6 (loop 3). It can be seen from the diagram that C_A is now charged by the loop 3 current and the loop 2 current while C_B is charged by the loop 2 current and this causes the voltage v_{AB} - the sum of the voltages across C_A and C_B - to increase. If during this time G_6 is kept on and I_d is transferred back and forth between loops 1 and 3 by alternate conductions of G_5 and G_1, then the voltage across C_A and C_B will build up and so too will v_{AB}. It is this voltage build up that causes the spikes on the output voltage to appear, and the voltage rise stops only when the sinusoidal phase A current of the load reverses. This reverse the direction of the loop 2 current, and C_A and C_B are discharged.

In order to reduce the voltage spikes on the output, some way must be found

to prevent C_A and C_B from overcharging, and Hombu et al. have shown that this can be done as follows. Suppose that at t = 0, the inverter is in the state shown in Fig. 3.3(a). If the time comes to transfer the dc link current I_d from line C to line A by turning off G_5 and turning on G_1, then G_6 should be turned off and G_4 be turned on first, before the transfer takes place - this short-circuits the dc bus and isolates the load from the bus (Fig. 3.3(c)). Because of this, what was previously loop 1 current now flows through phase C of the load, phase B of the load, C_B, and C_C (loop 4); therefore, C_A is prevented from being overcharged for a while and the loop 4 current, which is higher than the loop 2 current discharges C_B. This prevents v_{AB} from building up, thus eliminating the mechanism that causes spiking to occur. The final step in the process is to turn off G_4 and turn on G_1 thus transferring current from line C to line A.

The overvoltage spikes on the inverter output voltage can be reduced by short-circuiting the dc bus at selected intervals which is what has to be done whenever the inverter pattern has PWM in the center 60° region of each half-cycle. Therefore, the overvoltage spikes do not appear on the inverter output voltage when a technique such as SPWM is used. Moreover, since the spikes can be suppressed by the inverter pattern, the size of the output filter capacitors can be reduced. This reduces the cost and size of the inverter and also pushes the output resonance frequency to a higher value, making it easier to implement desired PWM techniques.

3.5. Boost effect due to the short-circuiting of the dc bus

So far in this thesis, it has been shown that short-circuiting the dc bus at selected intervals of time is advantageous because:

1) PWM patterns having no low-order harmonics can be implemented on a CSI.

2) The dynamic response of the CSI can be improved.

3) The overvoltage spikes on the inverter output voltage can be suppressed.

There is a drawback, however, to short-circuiting the dc bus and it is as follows.

Whenever the dc bus is short-circuited, the dc link reactor appears across the rectifier with one side connected to the rectifier's positive terminal and the other connected to its negative terminal. Since the rectifier usually has a large voltage across it, the current through it will rise (experience a boost effect) according to the equation

$$\Delta i = \frac{V}{L}\Delta t \qquad (3.7)$$

where Δi = rise in inductor current (A)

V = voltage across inductor (V)

L = inductance (H)

Δt = time (s).

The rise in dc link inductor current is dependent on two factors, one of these being the size of the inductor. According to equation 3.7, the inductor should be as large as possible to minimize the rise in current, however, this contradicts the

criterion that the inductor be small enough so that a reasonable dynamic response is obtained; therefore, a compromise must be made between the two criteria. The other factor affecting the rise in current is the length of the short-circuiting intervals - if the PWM pattern used has a low modulation index or the inverter is operated at a low frequency, then this can be substantial. In order to avoid a significant rise, the dc link inductor current must be regulated by reducing the dc voltage across the rectifier when the dc bus is short-circuited; this worsens the input power factor when a phase-controlled rectifier is used. If the amount of short-circuiting done is limited to keep the current from rising then the PWM patterns that can be used must be restricted to those having no PWM in the center 60° block.

3.6. Modifications based on short-circuiting considerations

In order to get the benefits obtained by short-circuiting the dc bus without the boost effect, it is necessary to modify the conventional PWM CSI topology in some way. One modified PWM CSI topology was proposed by Nonaka and Neba [18], [34-36] and was designed so that the overvoltage spikes that normally appear on the inverter output voltage can be suppressed without short-circuiting the dc bus. The topology, shown in Fig. 3.4, has two auxiliary GTOs connected across the dc bus and their midpoint is connected to the neutral of the the filter capacitors. With the addition of the auxiliary switches, the output voltage spikes can be suppressed without short-circuiting the dc bus because the auxilary GTOs can be fired in such

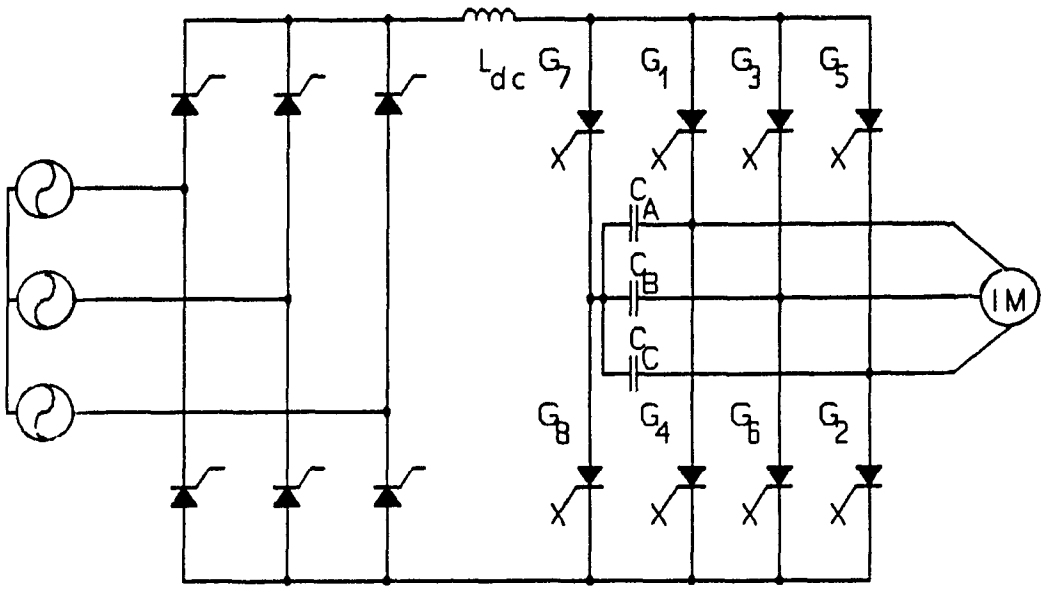


Fig. 3.4. The modified PWM CSI topology proposed by Nonaka and Neba.

a way so that the overcharging of the capacitors caused by the flow of current through them during a conduction interval is avoided. By firing an auxiliary GTO, the flow of current through the capacitors can be changed so that they are discharged, which suppresses the voltage spikes. The two auxiliary GTOs do not have to be both on at the same time when suppressing spikes for TPWM.

In Fig. 3.5, the derivation of the gating signals of the inverter and auxiliary GTOs are shown. It can be seen that the gating signals of the inverter GTOs can be obtained using TPWM while those of the auxiliary GTOs are such that they result in the line currents having PWM in the center 60° block of each half-cycle. The presence of the two auxiiary switches allows this CSI to be used with non-standard patterns. For example, in [36], Nonaka and Neba demonstrated that their inverter can also be used with a SPWM pattern and with variable modulation index control, however, dc bus short-circuiting had to be done when this type of control was used, and the auxiliary GTOs were both on at selected intervals.

It was shown in section 2.8 that the addition of only one auxiliary switch in the dc link, external to the inverter increases the number of PWM patterns that can be implemented on a CSI since the general rule that current must always flow through the inverter can be violated. This approach was in fact proposed by Matsui et al. in [17], where an auxiliary GTO was added across the dc bus, and the inverter pattern rules were shown to be less restrictive than those for a standard CSI. In spite of the benefits that can be obtained with this switch, the boost effect caused by short-circuiting the dc bus still remains if it is connected across the dc bus. In

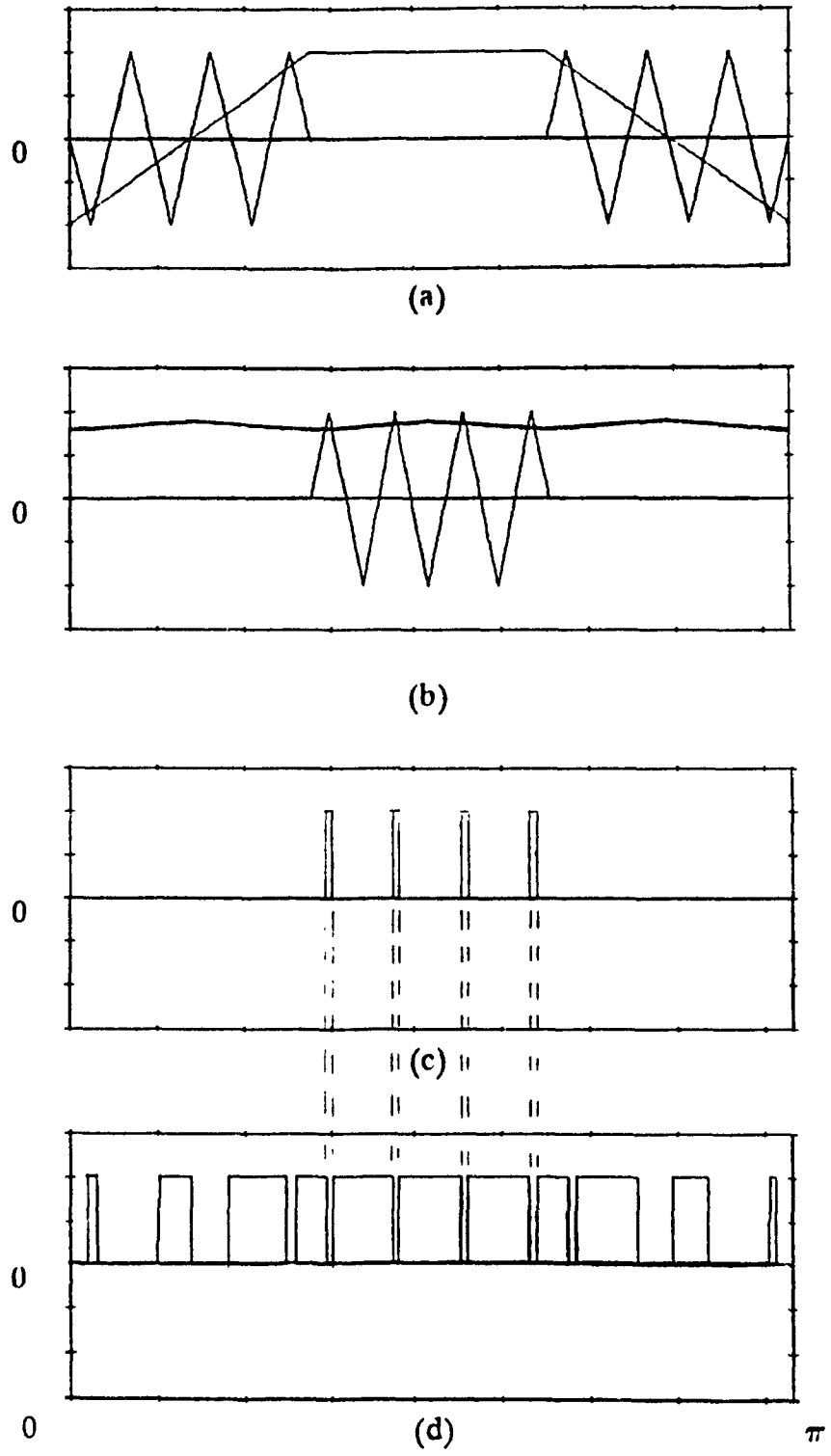


Fig. 3.5. (a) Main GTO control signals. (b) Auxiliary control GTO signals. (c) Main GTO PWM pattern (G_1 current). (d) Auxiliary GTO PWM pattern (G_7 current).

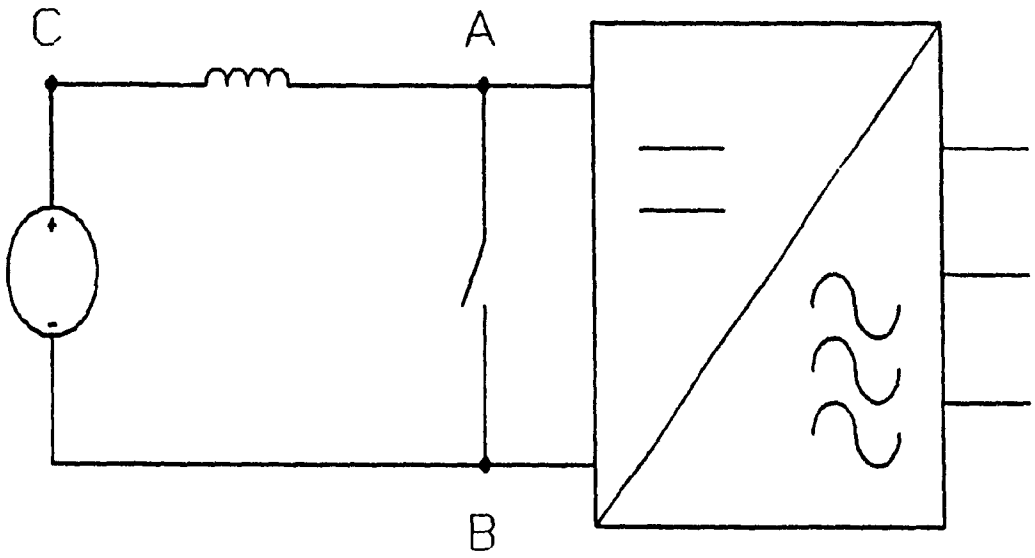


Fig. 3.6. Equivalent dc bus circuit diagram.

Fig. 3.6, the equivalent dc bus circuit for a CSI is shown with the rectifier represented as a dc source, the inverter and the load represented as a black box and an auxiliary switch connected across the bus. Since the current flowing at pt. B is the same as that flowing at pt. C, it is possible to connect the auxiliary switch at C instead of B and obtain an equivalent circuit which has the benefits of the previous topology without the disadvantages of short-circuiting. This topology was proposed in [37]-[38] and will be examined in detail in Chapter 4.

3.7. Conclusion

In this chapter, the characteristics of the PWM CSI have been presented. It has been demonstrated that a change in the modulation index of the inverter PWM pattern or the output power factor will affect the dc link inductor current unless the rectifier output voltage is adjusted. It has also been shown that the PWM CSI has a poor dynamic response and overvoltage spikes on its output voltage unless the dc bus is short-circuited; however short-circuiting the bus causes the dc link inductor current to rise unless it is regulated. If the conventional PWM CSI topology is modified by adding an auxiliary switch across the dc link inductor, then the benefits of short-circuiting the bus can be obtained without the associated boost effect.

CHAPTER 4 - DC BUS & OUTPUT CHARACTERISTICS OF THE MODIFIED CURRENT SOURCE INVERTER

4.1. Introduction

In this chapter, a new PWM CSI topology, which is referred to as the modified current source inverter (MCSI), is presented. The MCSI, shown in Fig. 4.1, provides sinusoidal output line currents without having the disadvantages of the conventional PWM CSI mentioned in the previous chapter. The distinguishing feature of the proposed topology is an auxiliary switch connected across the dc link inductor that allows it to operate with most PWM techniques (no matter how low the modulation index or inverter fundamental frequency) and with a fast dynamic response.

The principles of operation for the MCSI are presented along with typical waveforms at the dc bus and at the output; these waveforms are unique to the MCSI as they are dependent upon the operation of the auxiliary switch. It is also shown how the presence of this switch in the dc link gives the MCSI several advantanges over the conventional PWM CSI. Design guidelines for steady state operation, the output filter capacitors, and ratings for the inverter switches are also given along with a design example. Finally, simulated and experimental results of the MCSI operating under motor conditions and simulated results for the MCSI operating under regenerative and transient conditions are presented.

carrier PWM patterns - especially with third harmonic injection SPWM patterns. This is done because third harmonic SPWM is a standard VSI technique that is rarely used in conventional PWM CSIs, and can be used for variable modulation index control.

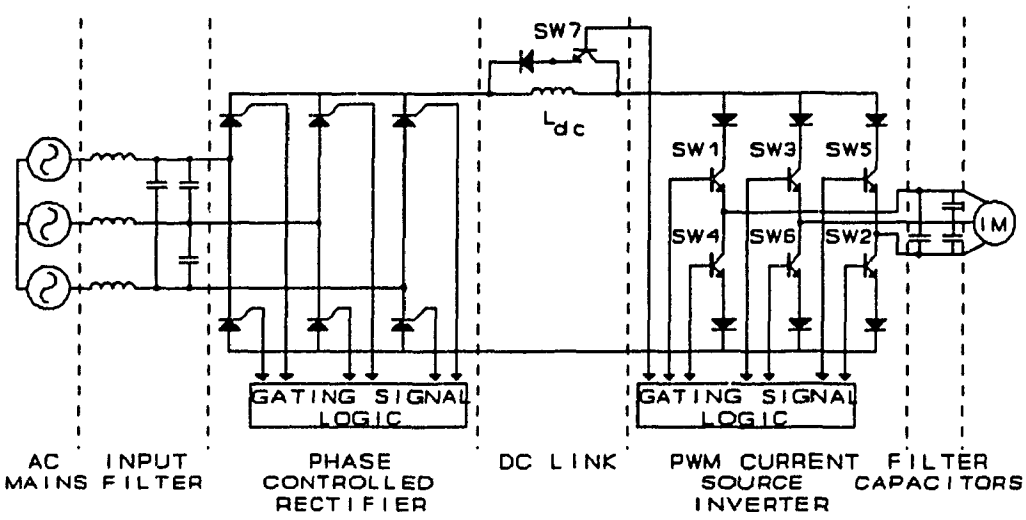


Fig. 4.1. The modified current source inverter (MCSI).

4.2. Principles of operation

The proposed MCSI topology is the same as the conventional PWM CSI topology but with an auxiliary switch connected across the dc link inductor. The topology is not a new one and has been used for many years as a load - commutated thyristor inverter drive for synchronous machines [22]; however, the characteristics of the topology with self-commutated switches have never been

examined. When the topology is used as a synchronous machine drive and the inverter switches are thyristors, it is important to ensure that the thyristors are commutated correctly so that balanced and symmetrical three-phase line currents can be produced. This is not possible when the machine is being started up or is operated at a low speed because the induced back emf is not high enough to provide current commutation in the inverter. Under these conditions, commutation must be done by some other means and can be done by firing the auxiliary switch and allowing the dc link inductor current to flow through it - the thyristors are turned off because current ceases to flow through the inverter. The switch is turned off only after commutation has occured and the next pair of switches has been turned on. The auxiliary switch stops being used as soon as the synchronous machine is operating at a speed high enough to provide enough back emf to commutate the thyristors. It is never used when the machine is operated under steady-state conditions unless the speed is low.

In the MCSI, the firing of the auxiliary switch is synchronized with the firing of the inverter switches so that it is turned on whenever there is no path for the dc link inductor current to flow through the inverter. This allows the current to freewheel through the switch until a path is provided by the inverter - then the switch is turned off. The gating signal of the auxiliary switch together with those of the top three inverter switches is shown in Fig. 4.2. where it can be seen that the auxiliary switch signal is high only when all the other signals are low. The same signals are shown for a reduced modulation index in Fig. 4.3. where it can be seen

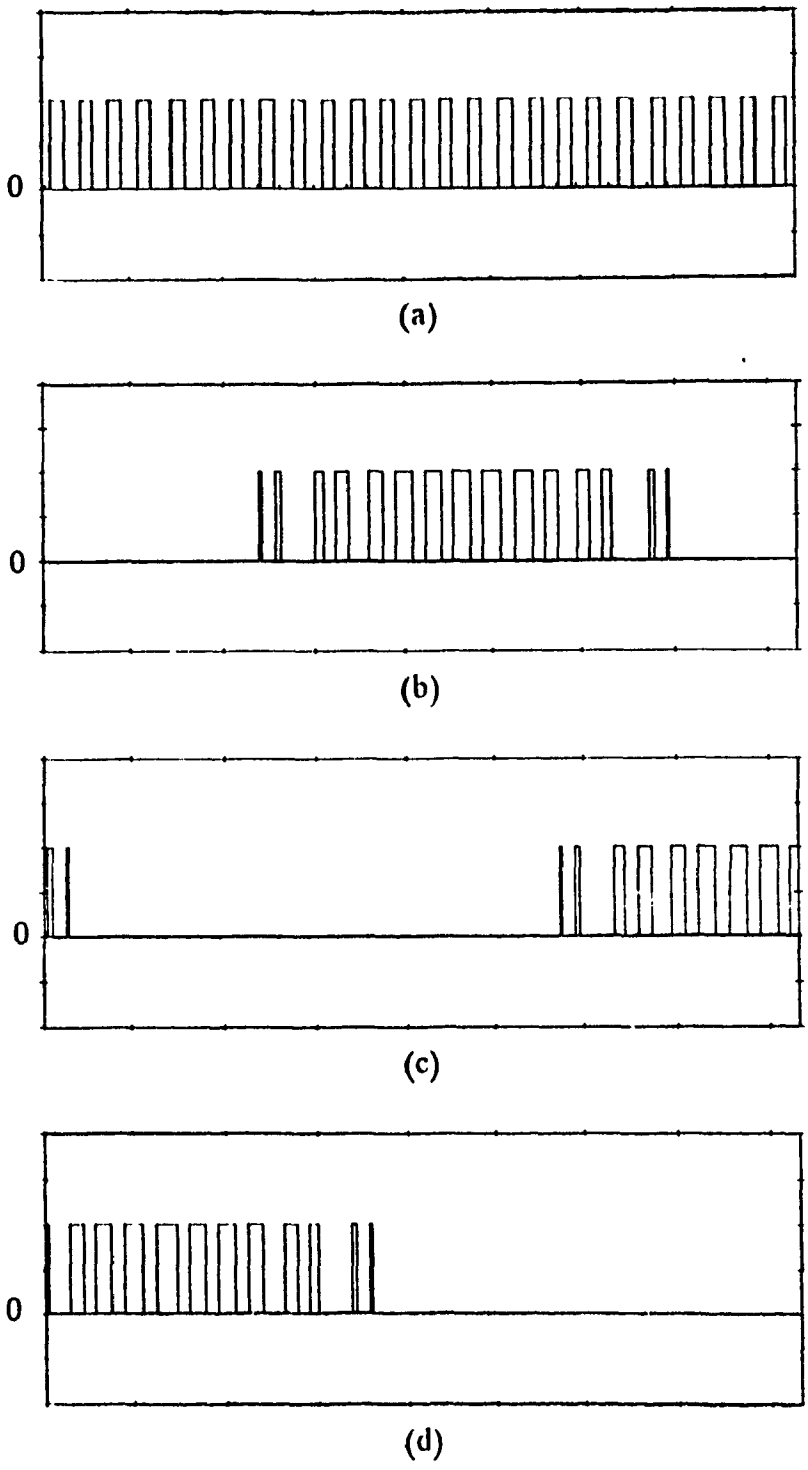


Fig. 4.2. Gating signals for (a) Auxiliary switch. (b)-(d) Top three inverter switches (M = 0.8).

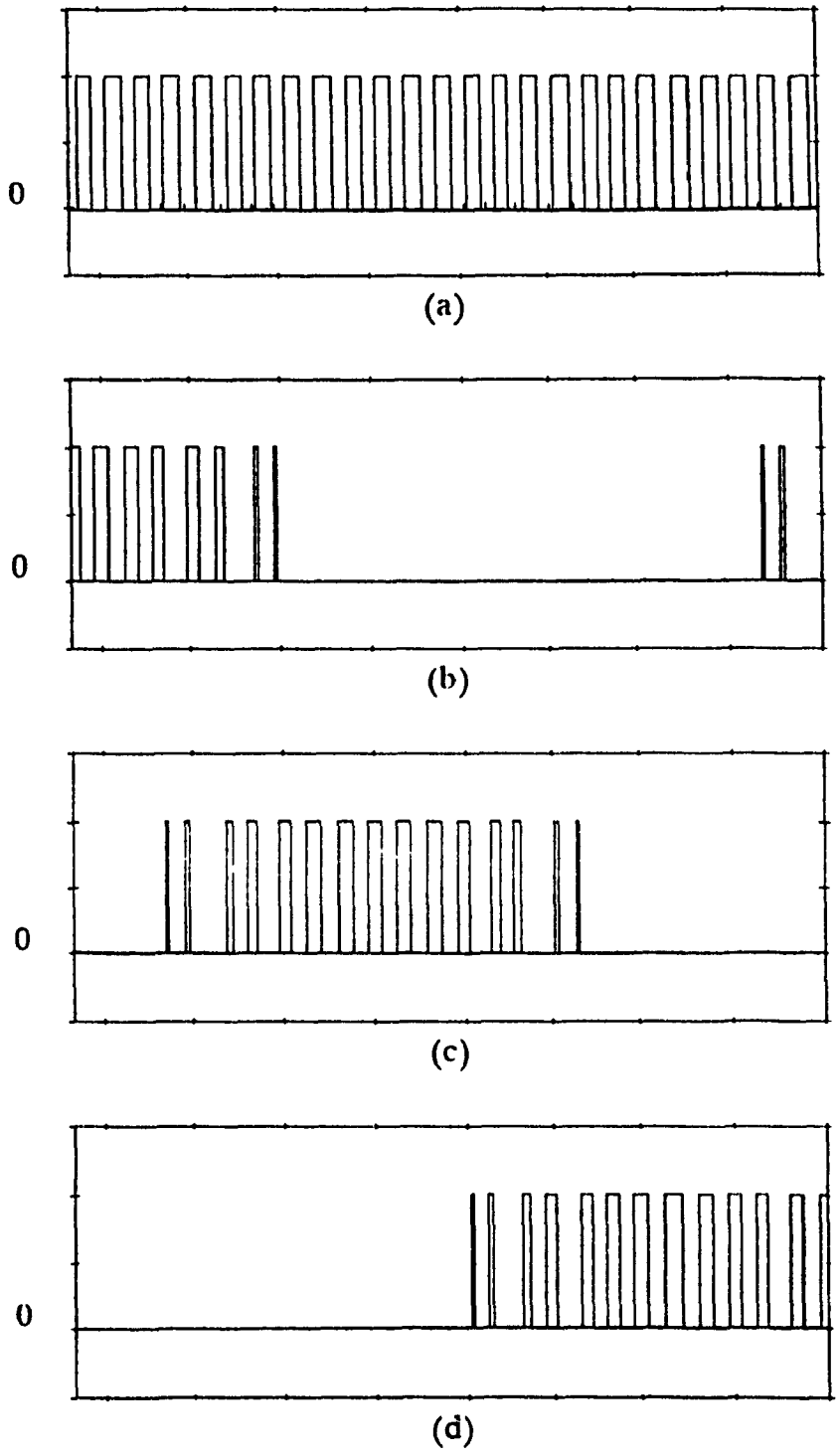


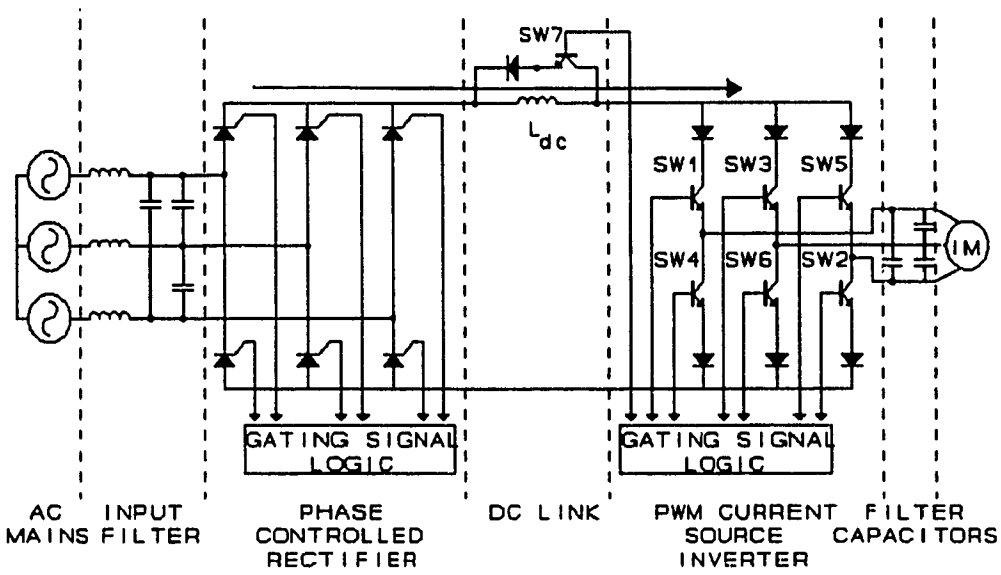
Fig. 4.3. Gating signals for (a) Auxiliary switch. (b)-(d) Top three inverter switches (M = 0.4).

that the inverter gating pulses have become narrower while those of the auxiliary switch have become wider to ensure that the dc link inductor always has a path to flow through. Since a path for current is always provided, the MCSI allows an inverter pattern having any modulation index to be used, and it also allows the pattern to modified safely while the inverter is operating.

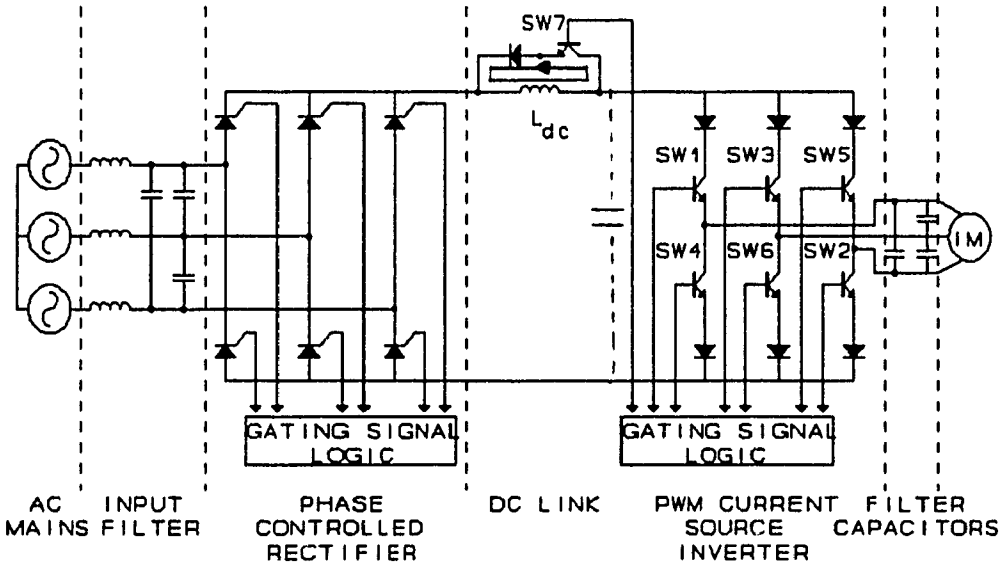
The MCSI has two basic modes of operation. The MCSI operates exactly like a conventional PWM CSI in mode 1 (Fig. 4.4(a)) as current flows through the ac mains, rectifier, dc link, inverter, and load, while in mode 2 (Fig. 4.4(b)), the auxiliary switch is on and current flows only through the switch. The dashed capacitor shown in Fig. 4.4(b) represents the capacitance that is part of the snubber(s) needed to to protect the switches when they are turned on and off; there can be one snubber can be connected at the dc bus or there can be six snubbers in the inverter, one for each switch. The snubber capacitor(s) is the equivalent circuit in mode 2 because the rectifier and the inverter are disengaged from the bus as there is no current flowing in them. The voltage across the capacitor(s) is generally the voltage that was reflected from the inverter output before the auxiliary switch was fired.

The characteristics of the MCSI are different from the conventional PWM CSI in the following ways:

1) Since there is no current flowing in the dc link whenever the auxiliary switch is fired, the dc bus current (Fig. 4.5(a)) - the current flowing at the rectifier output and at the inverter input - is chopped and is equal to either the dc



(a)



(b)

Fig. 4.4. MCSI modes of operation (a) Mode 1. (b) Mode 2.

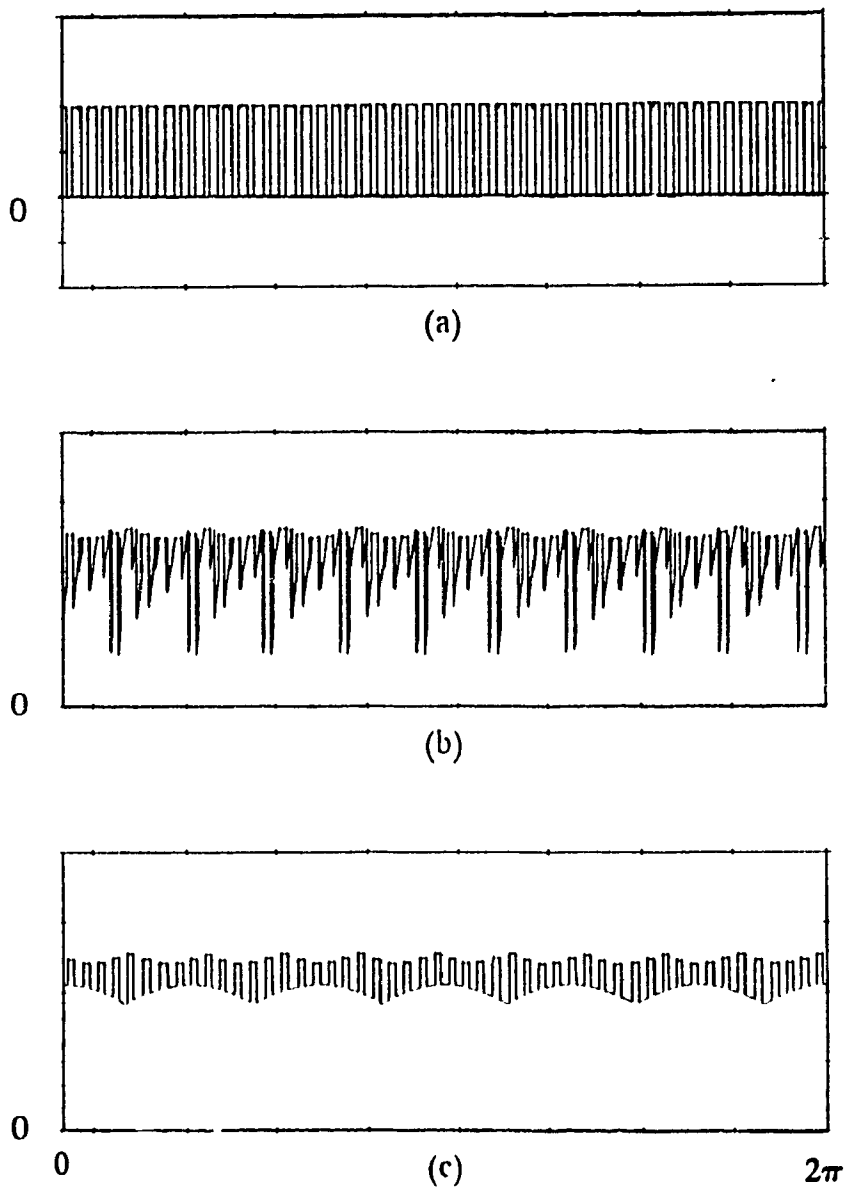


Fig. 4.5. DC bus characteristics: (a) DC bus current. (b) Inverter input voltage. (c) Rectifier output voltage.

link inductor current or zero at any moment. This is unlike the conventional PWM CSI where the dc link inductor current and the dc bus current are the same.

2) Each inverter output line current in a conventional PWM CSI is the product of the dc bus current and a switching function (defined as the gating signal of a top switch minus that of a bottom switch on the same leg and having an amplitude of -1, 0 or 1 at all times) i.e.

$$I_{ac_1} = I_{dc} \cdot SW_1 \qquad (4.1)$$

The magnitude of the fundamental component of the inverter output currents can be changed by keeping the dc bus current constant and changing the inverter PWM pattern thus changing the ratio of I_{ac1} to I_{dc}. In the MCSI, however, each output line current is the product of the dc link inductor current and a switching function, and the PWM operation (chopping) is carried out on the bus instead of the inverter (which simply distributes the current pulses on the dc bus to produce the line currents).

3) When the auxiliary switch is not on, the dc bus voltage at the input of the inverter (Fig. 4.5(b)) is the inverter output voltage reflected on the dc bus through the operation of the inverter switches, and the rectifier output voltage (Fig. 4.5(c)) is what one would normally expect when a thyristor rectifier is used. When the auxiliary switch is on, then these two voltages become equal to the voltage across the snubber capacitor(s). Because of the MCSI's two modes of operation, the rectifier output voltage waveform has

voltage components with a frequency of twice the inverter switching frequency superimposed on it. These components are always higher than the normal rectifier output so that the power relationship between the bus and the inverter output power can be satisfied as power is not transmitted from the dc bus to the inverter output when the auxiliary switch is on (dc bus power must be equal to inverter output power). It is because the components are higher than the normal rectifier output voltage that current stops flowing on the dc bus when the auxiliary switch is on since the rectifier switches are reverse-biased.

4.3. Advantages of the modified current source inverter

The MCSI has several advantages over the conventional PWM CSI, including the following:

1) More PWM patterns can be implemented on the MCSI because the constraint that that the inverter must always provide a path for the link inductor current to flow does not have to be satisfied. For example, carrier PWM techniques that cannot be implemented on a conventional PWM CSI can be on the MCSI due to the auxiliary switch as was seen in section 2.8. Therefore, it is easier to design and implement patterns that satisfy the desired design criteria (i.e having no low-order harmonics).
2) The problems associated with short-circuiting the dc bus of a conventional

PWM CSI such as the rise in dc link inductor current do not exist in the MCSI because the dc bus is never short-circuited. Therefore, it is easier to implement PWM patterns having PWM in the center 60° region of each half-cycle, and to eliminate the overvoltage spikes that can appear on the inverter output voltage.

3) If it is desired for a conventional PWM CSI to have a fast dynamic response then either a PWM rectifier must be used to minimize the dc link inductor or variable modulation index control must be done by short-circuiting the dc bus. The MCSI can have a fast dynamic response with a thyristor rectifier and without short-circuiting the dc bus since variable modulation index control can be done with the auxiliary switch.

4) The auxiliary switch can act as a protection against a fault in the inverter or the load. Stopping the flow of current into the inverter by setting the rectifier output voltage to zero can be a slow process because of the energy stored in the dc link inductor that must be discharged, and the inverter and load can be further damaged while this is happening. The flow of current into the inverter can be interrupted immediately in the MCSI merely by firing the auxiliary switch.

4.4. Equations for steady-state operation and design guidelines

4.4.1. Equations for steady-state operation

Since the characteristics of the MCSI are different from those of the

conventional PWM CSI, the standard equations used to calculate steady-state operating points for the inverter and the load cannot be used and new ones must be derived as is done in this section. The equations presented here are for the dc bus and output quantities only as those for the input quantities will be presented in Chapter 5. The derivation of the equations is based on the following assumptions:

1) Only the fundamental rms component of the ac quantities and the average value of the dc quantities are considered.
2) The load is an induction motor, which can be modelled with inductances and resistances as shown in Fig. 4.6. Furthermore, if a value of slip (s) is assumed, then this model is reduced to an impedeance Z_L that is made up of a resistor in series with an inductor.
3) The inverter is assumed to be lossless.

A line diagram showing the relevant parameters for steady state operation is presented in Fig. 4.7.

For a given output power and load current I_L, the inverter output voltage V_o and current I_o are

$$V_o = I_o Z_L \tag{4.2}$$

and

$$I_o = I_L \left(\frac{X_c}{X_c + Z_L}\right)^{-1} \tag{4.3}$$

where X_c is the impedance of the capacitor.

The equation defining the dc link inductor current I_{Ldc} (which is also the top

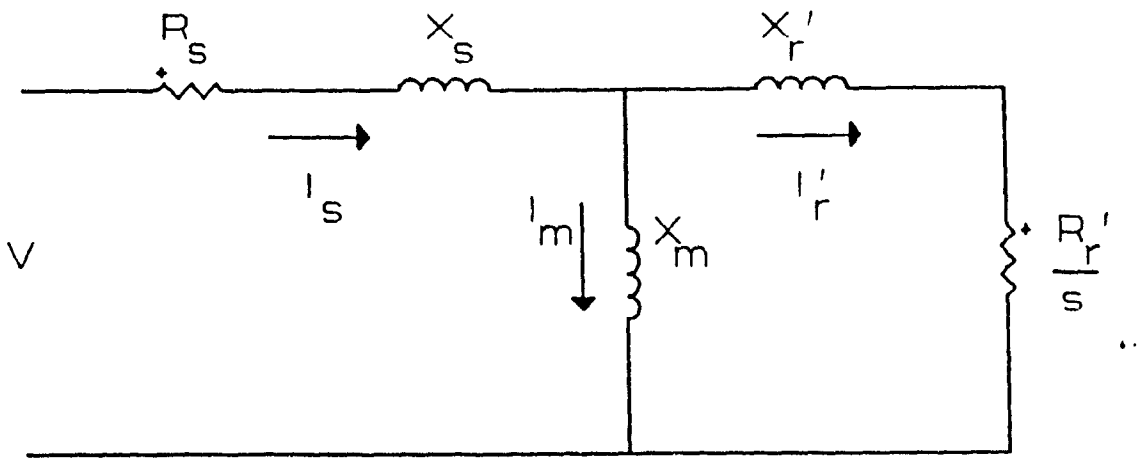


Fig. 4.6. Per phase equivalent circuit of an induction motor.

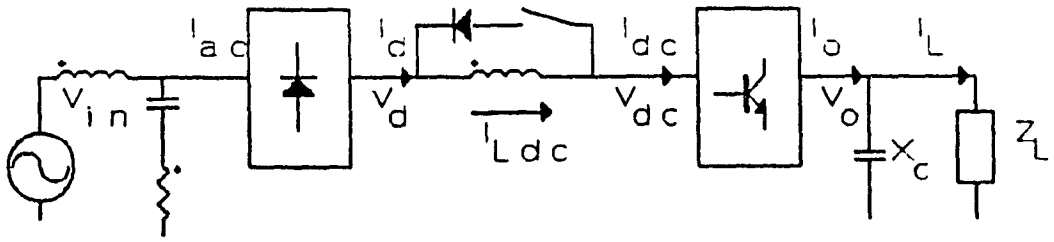


Fig. 4.7. MCSI line diagram.

part of the dc bus current $I_{dc,peak}$) from I_o is

$$I_{Ldc} = \frac{I_o}{MK_I(M)} = I_{dc,peak} \qquad (4.4)$$

where M is the inverter modulation index,

$K_I(M)$ is the inverter current gain and is a function of the PWM pattern and its modulation index (i.e. $K_I(M)$ is always 0.707 for third harmonic injection SPWM).

The average dc link current is

$$I_{dc} = (1 - K_s)\, I_{dc,peak} \qquad (4.5)$$

where K_s is the duty cycle of the auxiliary switch and

$$K_s = (1 - KM) \qquad (4.6)$$

where K is a constant and a function of the PWM pattern (i.e. K = 0.955 for third harmonic injection SPWM). Equ. 4.5 can also be expressed as

$$I_{dc} = KM I_{Ldc} \qquad (4.7)$$

Since the inverter output real power is equal to the inverter input real power for a lossless inverter, then

$$V_{dc} I_{dc} = 3 V_o I_o \cos\varphi_o \qquad (4.8)$$

where V_{dc} is the inverter input voltage

ϕ_o is the phase difference between V_o and I_o

Substituting equ. 4.4 into 4.8 gives

$$V_{dc}I_{dc} = 3Z_oM^2K_i^2(M)\,I_{Ldc}^2\cos\varphi_o \qquad (4.9)$$

where

$$Z_o = \frac{V_o}{I_o} \qquad (4.10)$$

If equ. 4.7 is plugged into 4.9 then

$$V_{dc} = \frac{3Z_oK_i^2MI_{Ldc}\cos\varphi_o}{K} \qquad (4.11)$$

Equ. 4.11 is also valid for the rectifier output voltage (V_d) as there is no dc voltage across the dc link inductor.

The equations that have just been derived can be used to examine the effect that modulation index and output power factor have on the MCSI dc link inductor current as was done in Chapter 3 for the conventional PWM CSI. If it is assumed that $K_i(M)$ and the load impedance are constant then the following relationship exists

$$V_{dc} \propto MI_{Ldc} \qquad (4.12)$$

If the modulation index of the inverter PWM pattern is originally M = 1 and is decreased using variable modulation index control while the rectifier output voltage is constant, then the dc link inductor current I_{Ldc} will rise by 1/M instead of $1/M^2$ as it did in the conventional PWM CSI under the same conditions. This is shown in Fig. 4.9 for the case when I_{Ldc} is 1 pu when M = 1. Since the purpose of variable modulation index control is to change the amplitude of the line currents while

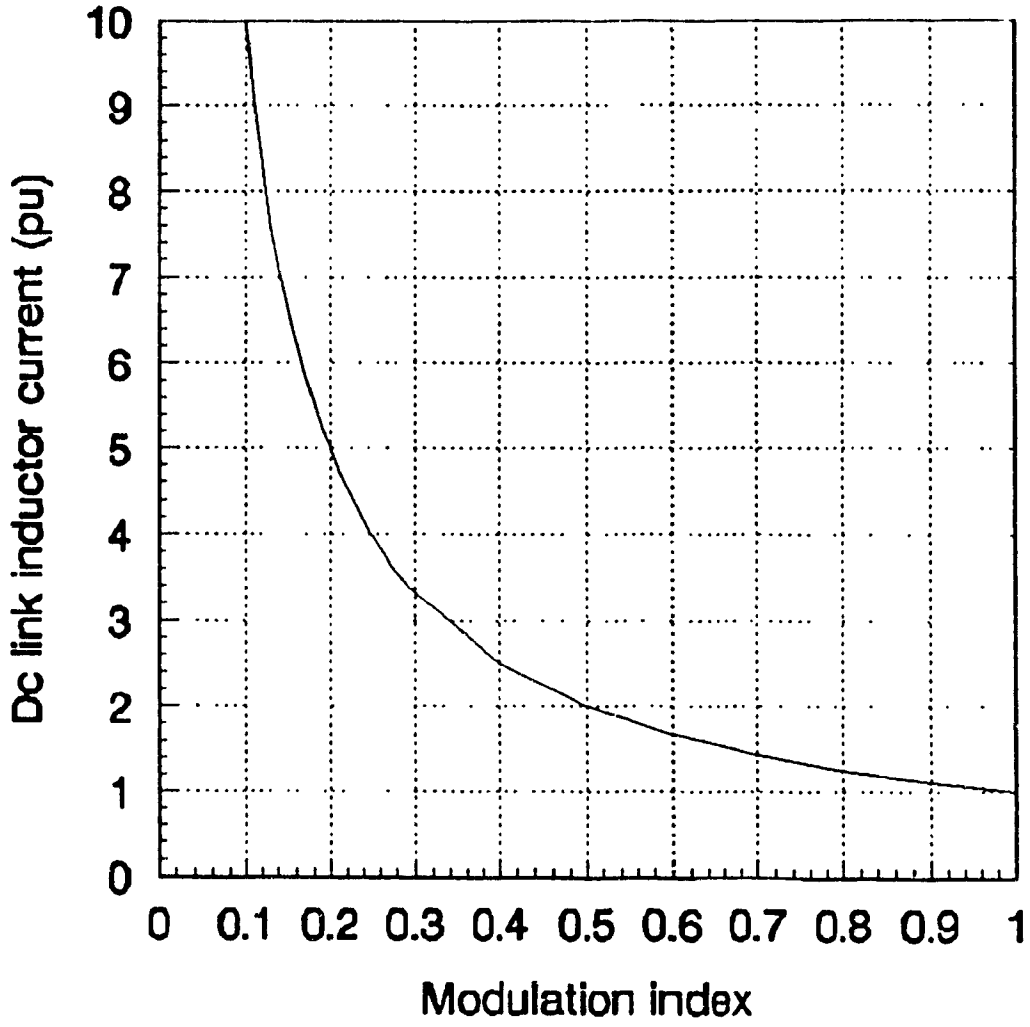


Fig. 4.8. Dc link inductor current (pu) vs modulation index when V_{dc} is constant.

keeping the dc link inductor current constant, the rectifier output voltage must be appropriately adjusted whenever the modulation index is changed. The level of adjustment needed to maintain the dc link inductor current constant is much less for the MCSI than it is for the conventional PWM CSI - especially when the inverter pattern has a low modulation index.

If it is assumed that $K_i(M)$, M, and Z_o are constant then the following relationship exists

$$V_{dc} \propto I_{Ldc}\cos\varphi_o \qquad (4.13)$$

This shows that as the inverter output power factor is decreased (i.e. by increasing the inverter frequency) then the dc link current will increase if the rectifier output voltage is kept constant. The amount of current rise is the same as that for the conventional PWM CSI and is shown in Fig. 4.10 for the case when I_{Ldc} is 1 pu when the load has unity power factor.

4.4.2. Design of the output filter capacitor

The purpose of the output capacitors is to attenuate the switching frequency (f_{sw}) components of the inverter line currents so that the load voltage and current become sinusoidal. A simple design criterion is to specify the output voltage ripple resulting from the lowest (first) switching frequency harmonics of the line currents - their amplitude is dependent on the inverter PWM pattern and the modulation index. For example, the first two harmonic components (sidebands at the switching

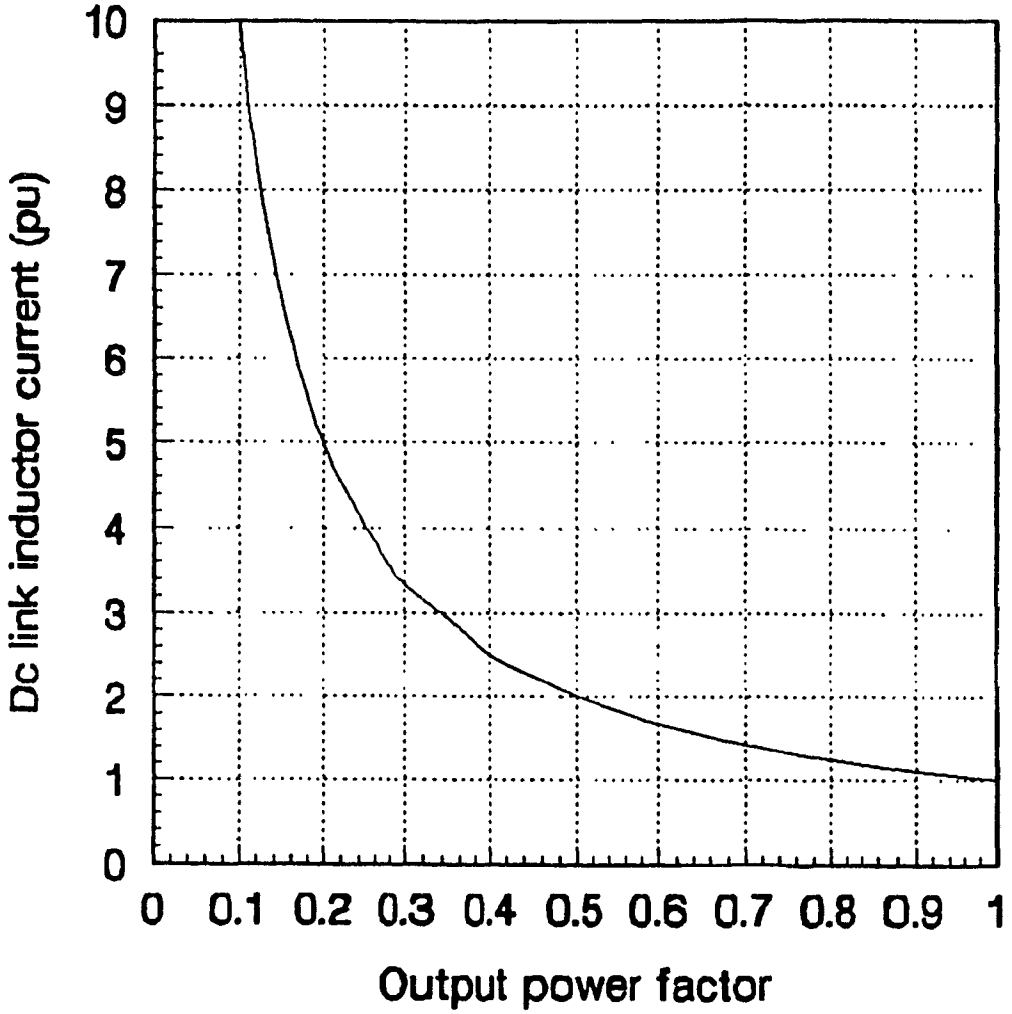


Fig. 4.9. Dc link inductor current (pu) vs modulation index when V_{dc} is constant.

frequency f_{sw}) of the SPWM pattern are largest when M = 0.5, thus the capacitors should be designed for this worst-case condition. Applying the criterion, and assuming that the output capacitors have a low impedance at the switching frequency gives the relation

$$V_h = \frac{V_1}{A_o} = I_h X_{ch} \qquad (4.14)$$

where V_h is the harmonic voltage component (rms)

V_1 is the fundamental voltage (rms)

A_o is the attenuation on the harmonic voltage component

I_h is the total rms value of the first two harmonic current sidebands

X_{ch} is the filter capacitor impedance at f_{sw}.

from which the value of the capacitor, C, can be found.

$$C = \frac{A_o I_h}{2\pi f_{sw} V_1} \qquad (4.15)$$

4.4.3. Inverter system switch rating

The worst case operation in terms of inverter rms switch current occurs when the modulation index of the pattern is 1.0. Since the auxiliary switch duty cycle is typically very small under these conditions, the inverter operates with current and voltage rms values similar to those of the conventional PWM CSI. When the auxiliary switch is open, the voltage across an inverter switch has the same

characteristics as in a conventional CSI. When the switch is closed, no current flows through the inverter switches, and the voltage, which has a maximum value of twice the peak line to line output voltage in the worst case, is shared by two switches so that each switch sees the peak of the line voltage. Inverter switch current and voltage ratings are therefore very close to those of the conventional CSI.

For the auxiliary switch, the worst case for current corresponds to low modulation indices, where the rms current approaches the rated dc link inductor current. The voltage appearing across the switch is the difference between the rectifier output voltage and the inverter reflected voltage. The maximum theoretical value of this voltage is twice the peak rated line-line output voltage and can occur under transient conditions when a transition is being made from motoring to regenerative braking operation or vice versa.

4.4.4. Steady state operation - design example

The equations derived in section 4.4.1 can be used to calculate the values of the inverter quantities for various load steady-state operating points. An example is presented here for a 460 V, 33 kVA, 60 Hz, 1176 rpm, 6 pole, Y connected squirrel-cage induction machine that has the following equivalent circuit parameters

$R_s = 0.29\ \Omega$ $R'_r = 0.145\ \Omega$ $X_m = 13.3\ \Omega$

$X_s = 0.21\ \Omega$ $X'_r = 0.50\ \Omega$

The motor is supplied from a CSI operating with a third harmonic injection SPWM inverter PWM pattern having a switching frequency f_{sw} that is 15 times the

fundamental. The CSI is supplied from a three-phase 420 V source. The flux is maintained close to the rated value by using V/f control. The steady-state inverter values are calculated for two operating points:

(1) The machine is operated under rated conditions at 60 Hz frequency and with rated torque. Under these conditions, the modulation index of the inverter PWM pattern is set to M = 1.

(2) The machine is operated at 30 Hz frequency and with half-rated torque. This operating point can be reached using variable modulation index control.

The dc bus voltage, dc bus current, dc link inductor current, and the modulation index are calculated in this section and the input current and rectifier firing angle will be calculated in Chapter 5.

Under rated conditions, the synchronous speed of the machine is 1200 rpm, the slip is 0.02, and the stator voltage, which is the inverter output voltage V_o, is 265.6 V line-neutral. The stator (load) current I_L can be calculated from the equivalent circuit model and is 40.5 A rms, lagging the voltage by 31.9°. The equivalent circuit can be reduced to a load impedance Z_L that is made up of a 5.57 Ω resistance in series with a 3.46 Ω reactance and has a magnitude of 6.56 Ω. Since the values of power, voltage, current, and impedance have been calculated for rated conditions, they can be taken as the base values in a per unit system so that

$$kVA_b = 33 \text{ kVA}$$

$$V_b = 265.6 \text{ V}$$

$$I_b = 40.5 \text{ A}$$

$$Z_b = 6.56\ \Omega$$

$$f_b = 60\ \text{Hz}$$

A value for the filter capacitor can be calculated using equ. 4.15. For a third harmonic injection SPWM pattern, the two sidebands are highest when the modulation index is M = 0.5 and both are approximately 25% of the fundamental. Since the load current is 40.5 A, the two sidebands are approximately 10.12 A, the total rms value of the sidebands is I_h = 14.3 A. If the attenuation factor is selected to be 20 (so that the output voltage ripple is less than 5% of the fundamental), and f_{sw} = 900 Hz and V_1 = 265.6 V are substituted into equ. 4.15. then

$$C = \frac{(20)(14.32)}{2\pi(900)(265.6)} = 190\mu F\ (0.47pu) \qquad (4.16)$$

and the impedance of the capacitor is X_c = 13.91 Ω (2.13 pu).

From equ. 4.3. the inverter output current I_o is

$$I_o = 40.5\angle -31.8\left(\frac{13.91\angle -90}{13.91\angle -90 + 6.56\angle 31.8}\right) = 34.46\ (0.85pu)\angle -3.84 \qquad (4.17)$$

From I_o, the dc link inductor current I_{Ldc} and the dc bus current I_{dc} can be calculated using equ. 4.4 and 4.7

$$I_{Ldc} = \frac{34.46}{(1)(0.707)} = 48.74A\ (1.20pu) \qquad (4.18)$$

$$I_{dc} = (0.955)(1)(48.74) = 46.55A\ (1.15pu) \qquad (4.19)$$

The average inverter input and rectifier output voltage V_{dc} can be calculated using

equ. 4.11 and is

$$V_{dc}=\frac{3(7.7)(0.70)^2 1(48.7)\cos(3.8)}{0.955}=589V(2.2pu) \quad (4.20)$$

When the output frequency is reduced to 30 Hz and V/f control is used, the synchronous frequency, the equivalent circuit reactances and the stator voltage are reduced by one-half. In order to operate the machine with half-rated torque, the slip speed must also be reduced by a half. Since this is 24 rpm (1200 - 1176 rpm) under rated conditions it must be changed to 12 rpm; therefore the machine is operated at 588 rpm (600 - 12 rpm) with slip s = 0.02. Since the slip, stator (inverter output) voltage and circuit parameters are known, the stator (load) current, the inverter output current and the inverter output phase difference can be found using the same procedure as before and are given below.

$$I_L = 26.09 \text{ A } (0.64 \text{ pu})$$

$$I_o = 22.83 \text{ A } (0.56 \text{ pu})$$

$$\phi_o = 38.5^\circ \text{ lagging}$$

Since variable modulation index control is used, the link inductor current has not been changed and the modulation index of the pattern can be found from equ. 4.4 with $K_i = 0.707$ for a third harmonic injection SPWM pattern.

$$M = \frac{22.83}{(0.707)(48.74)} = 0.66 \quad (4.21)$$

The dc bus quantities can be found using the same procedure as above and are listed below.

I_{Ldc} = 48.74 A (1.20 pu)

I_{dc} = 30.82 A (0.76 pu)

V_{dc} = 230.94 V (0.87 pu)

4.5. Simulated and experimental results

4.5.1. Motoring conditions

The MCSI topology was tested on the PSPICE simulation program [39] to verify its feasibility with various PWM techniques and to verify the design equations. The power rating of the converter was taken to be 5 kVA and the following were set as the base values:

VA_b = 5 kVA

V_b = 120 V

I_b = 13.89 A

Z_b = 8.64 Ω

f_b = 60 Hz

The load was modelled by using a static load having a resistance of 11 Ω (1.27 pu) and an inductance of 7 mH (0.31 pu), and the filter capacitor was 30 μF line-neutral (0.1 pu). The inverter frequency was set to 100 Hz and the switching frequency was f_{sw} = 1500 Hz. The simulated results are shown in Figs. 4.10, 4.12, 4.14, 4.16.

A 5 kVA prototype was constructed to further confirm the feasibility of the proposed topology. The power circuit and gating signal logic circuit of the prototype

are presented in the appendix. The experimental results obtained are in close agreement with the theoretical and simulated results. Figs. 4.11, 4.13, 4.15, 4.17 show the waveforms obtained for operation with modulation indices of 0.8 and 0.5 respectively for the same passive R-L load as above. The features of the waveforms can be summarized as follows:

1) The load currents are sinusoidal.

2) There are no overvoltage spikes on the output voltage.

3) The dc bus current is chopped.

4) There are overvoltage components on the rectifier output voltage.

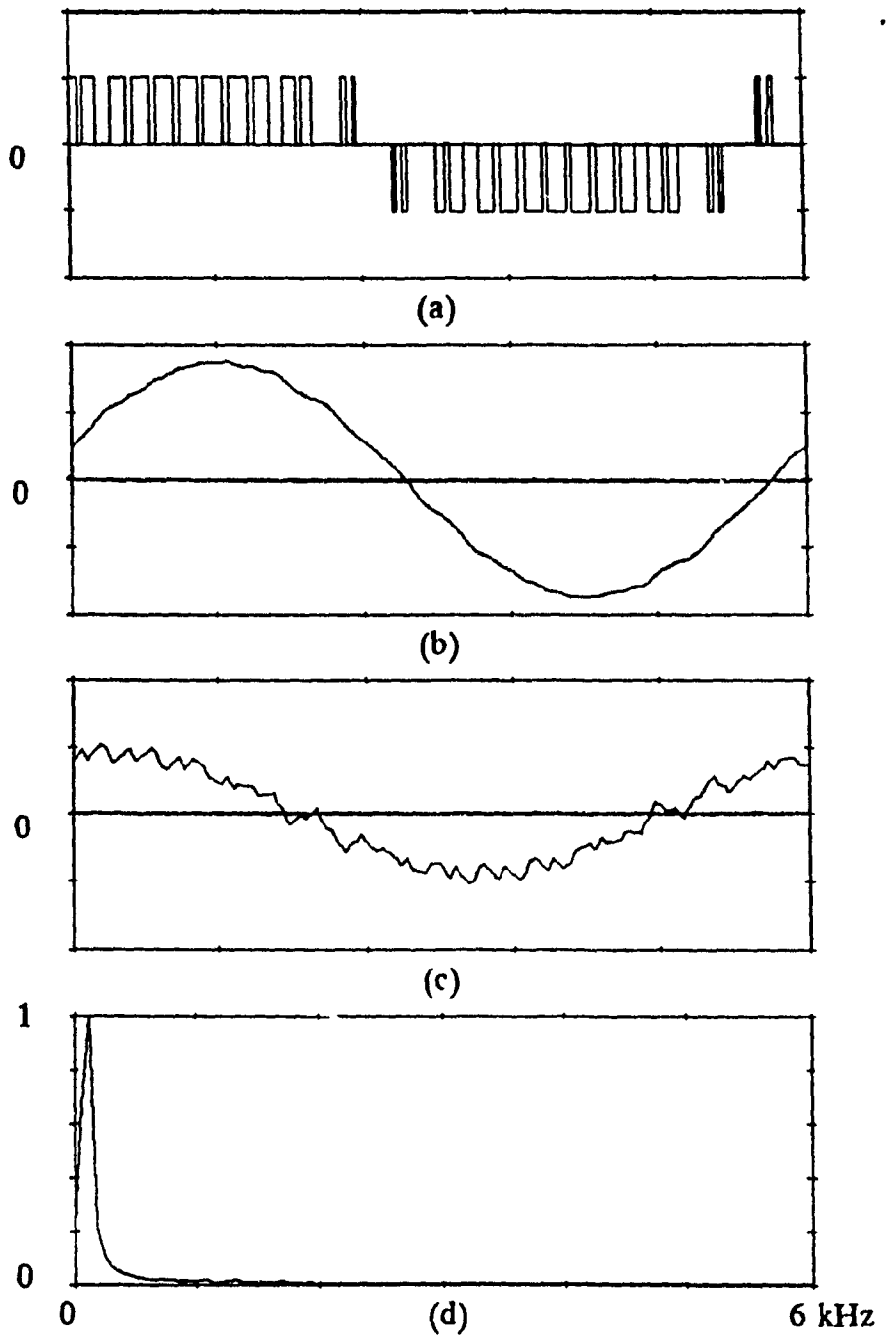


Fig. 4.10. Simulated results at output for MCSI with M = 0.8, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Inverter output current, scale 10 A/div., 2 ms/div. (b) Load current, scale 5 A/div., 2 ms/div. (c) Line-line voltage, scale 200 V/div., 2 ms/div. (d) Fourier spectrum of load current, scale 1 kHz/div.

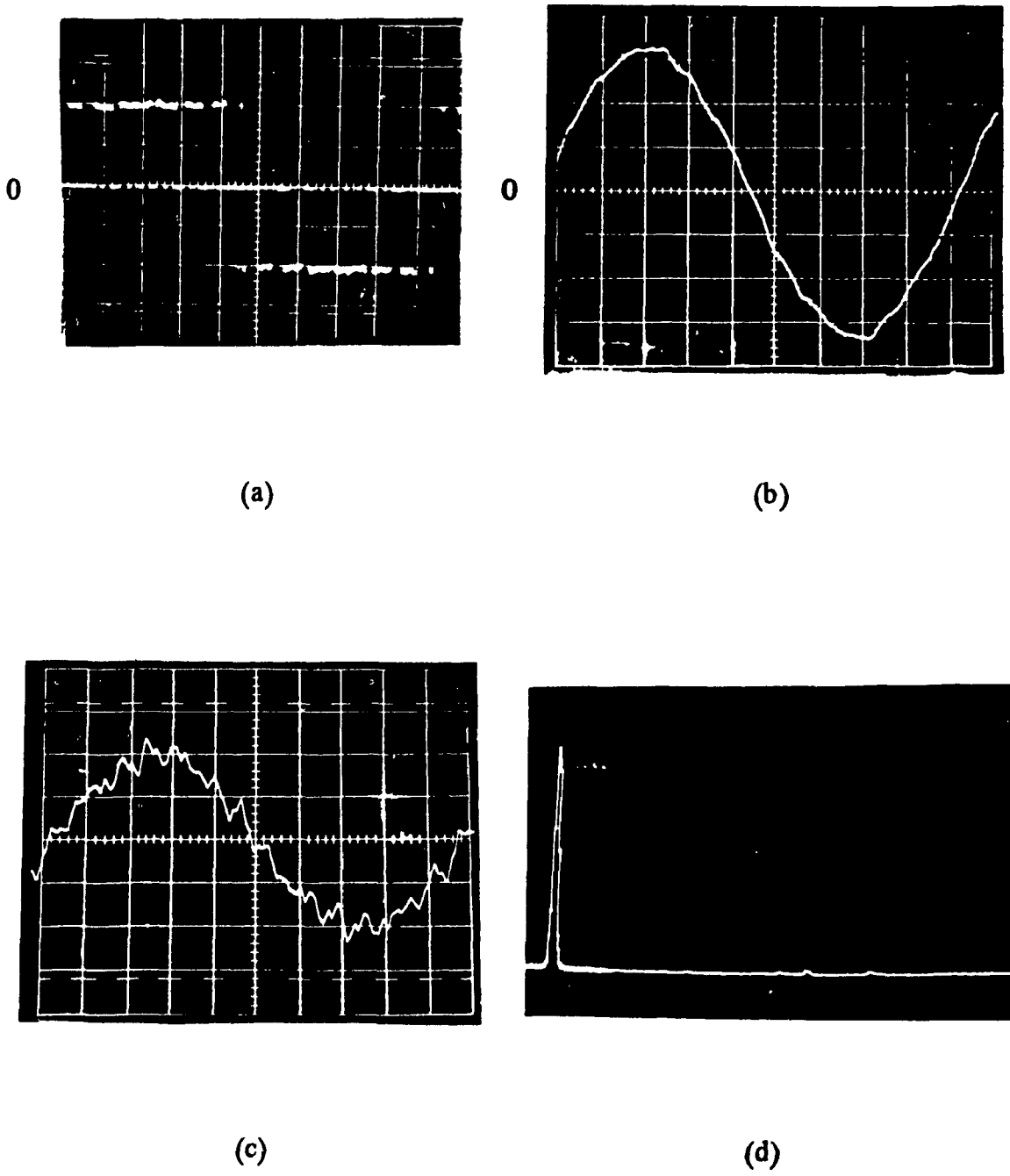


Fig. 4.11. Experimental results at output for MCSI with M = 0.8, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Inverter output current, scale 5 A/div., 1 ms/div. (b) Load current, scale 2.5 A/div., 1 ms/div. (c) Line-line voltage, scale 100 V/div., 1 ms/div. (d) Fourier spectrum of load current, range (0-3 kHz)

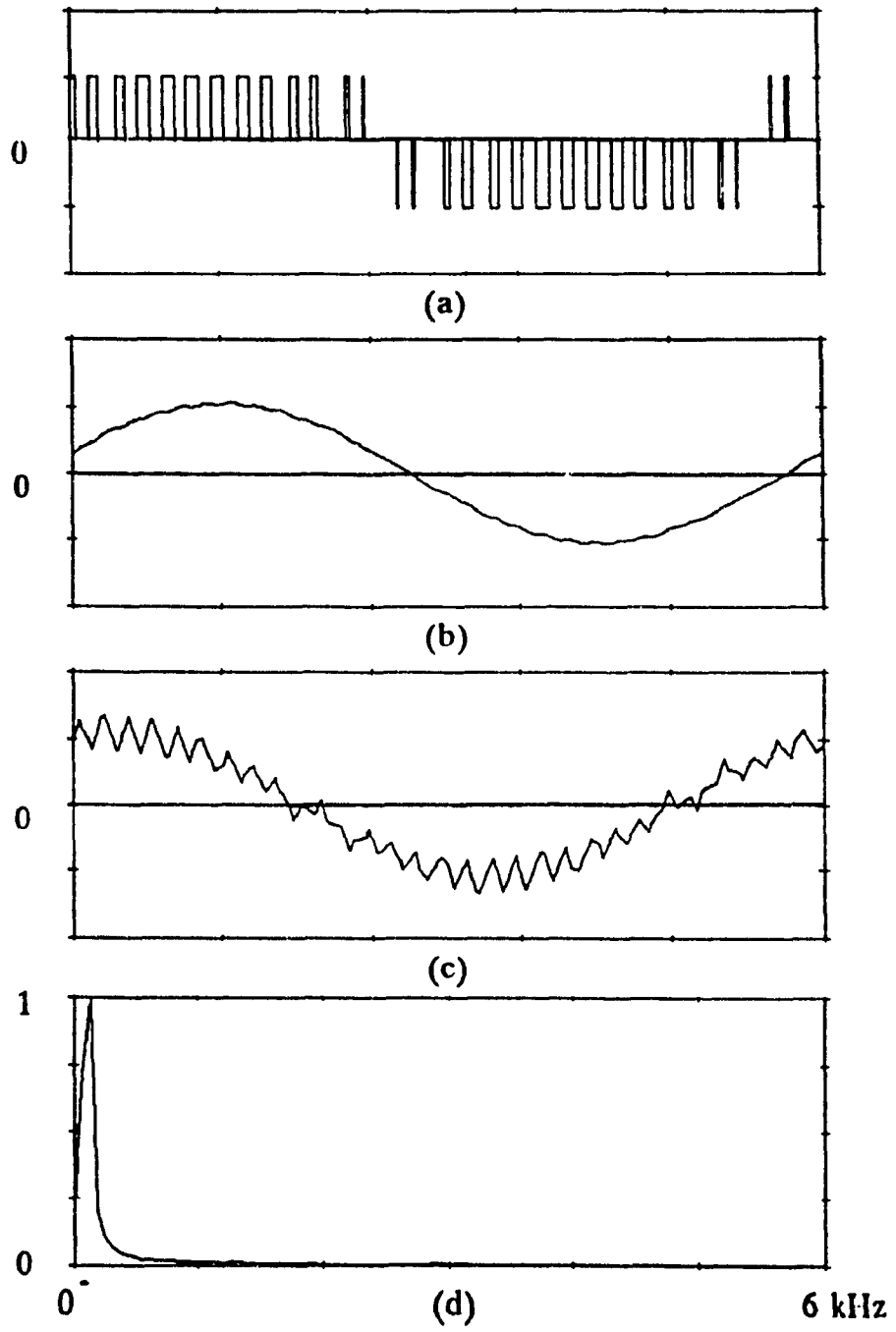
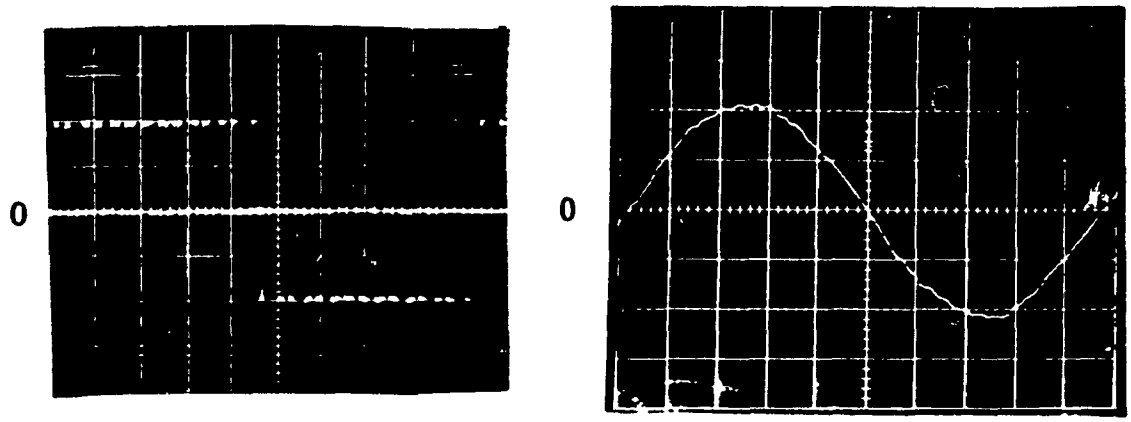
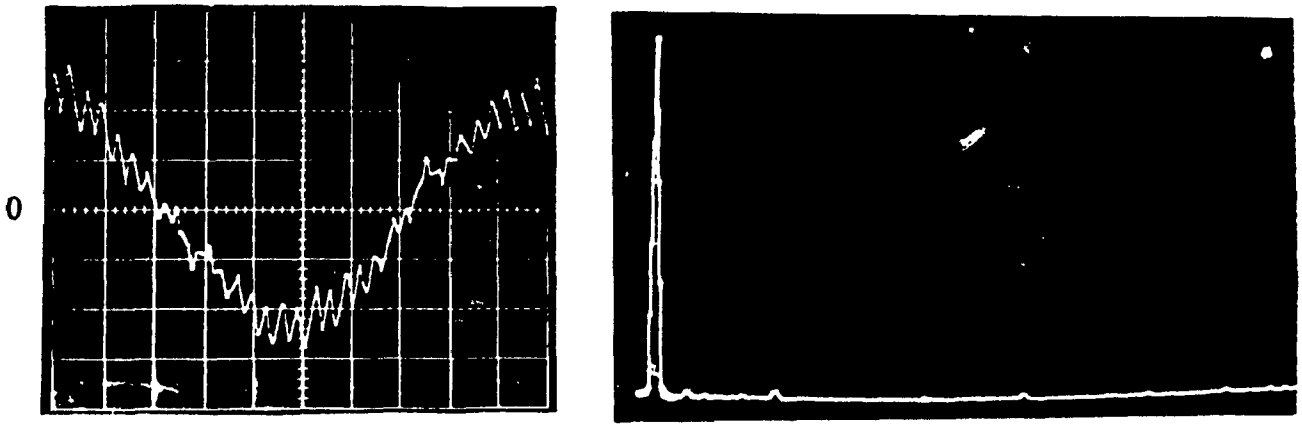


Fig. 4.12. Simulated results at output for MCSI with M = 0.5, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Inverter output current, scale 10 A/div., 2 ms/div. (b) Load current, scale 5 A/div., 2 ms/div. (c) Line-line voltage, scale 100 V/div., 2 ms/div. (d) Fourier spectrum of load current, scale 1 kHz/div.



(a) (b)



(c) (d)

Fig. 4.13. Experimental results at output for MCSI with M = 0.5, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Inverter output current, scale 5 A/div., 1 ms/div. (b) Load current, scale 2.5 A/div., 1 ms/div. (c) Line-line voltage, scale 50 V/div., 1 ms/div. (d) Fourier spectrum of load current, range (0-3 kHz)

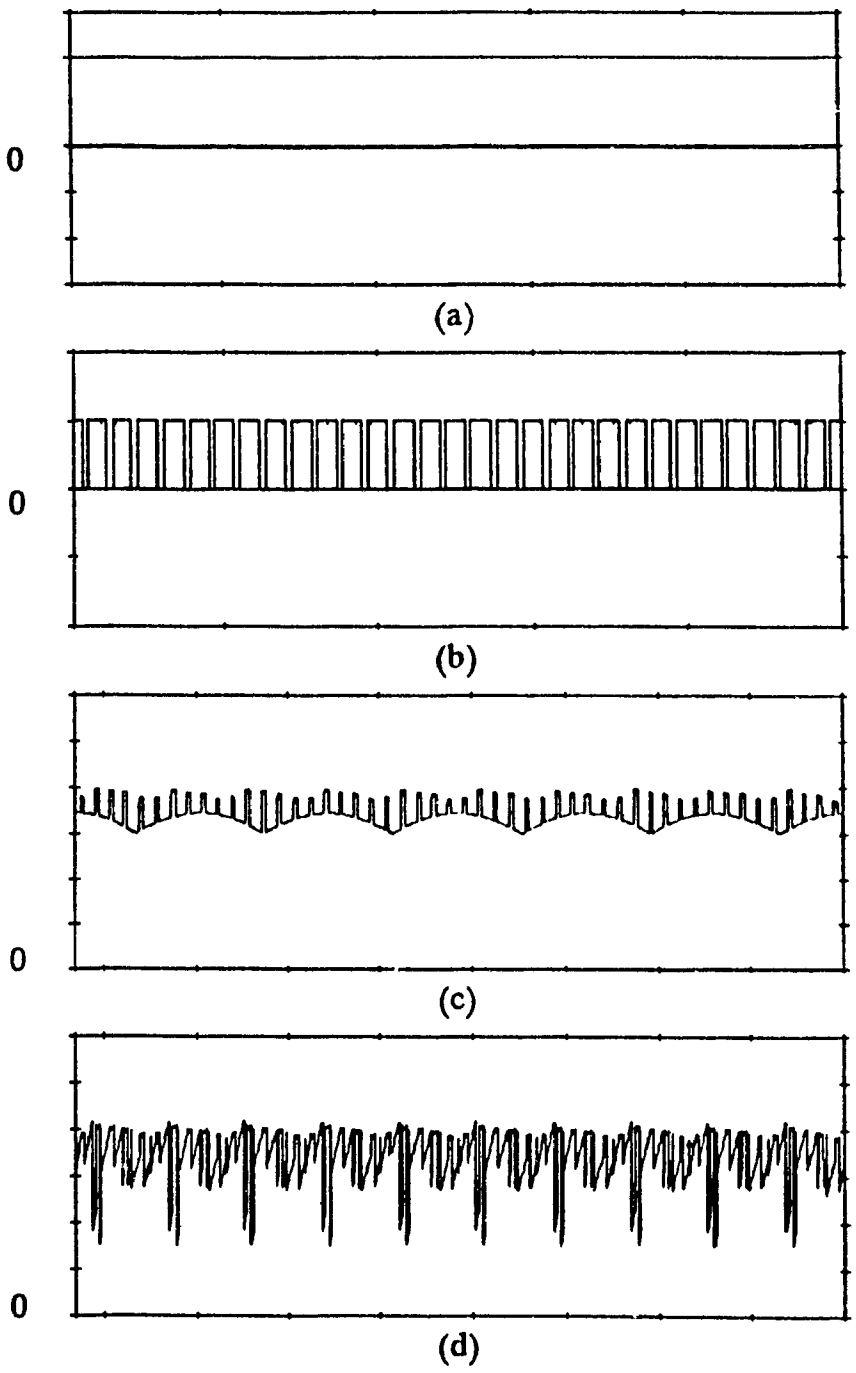
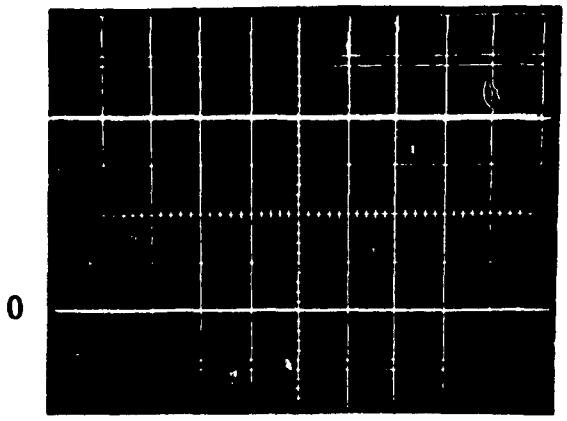
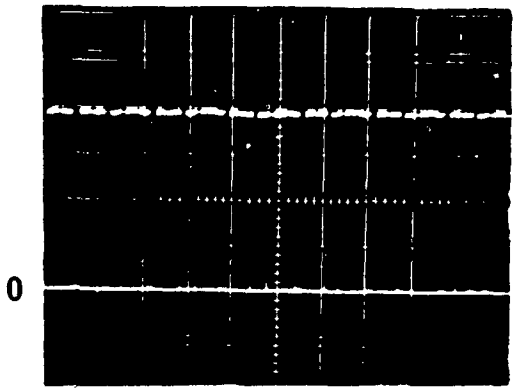


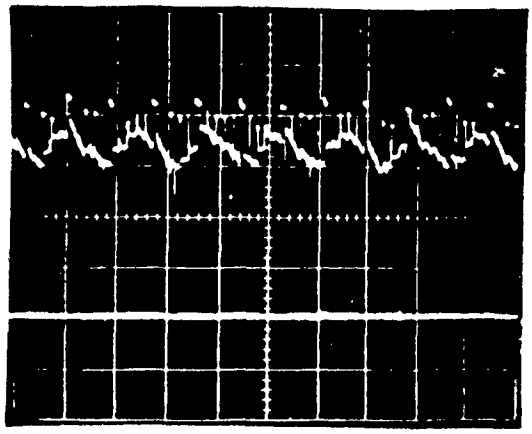
Fig. 4.14. Simulated results at dc bus for MCSI with M = 0.8, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Dc link inductor current, scale 10 A/div., 2 ms/div. (b) Dc bus currrent, scale 10 A/div., 2 ms/div. (c) Rectifier output voltage, scale 50 V/div., 2 ms/div. (d) Inverter input voltage, scale 50 V/div., 2 ms/div.



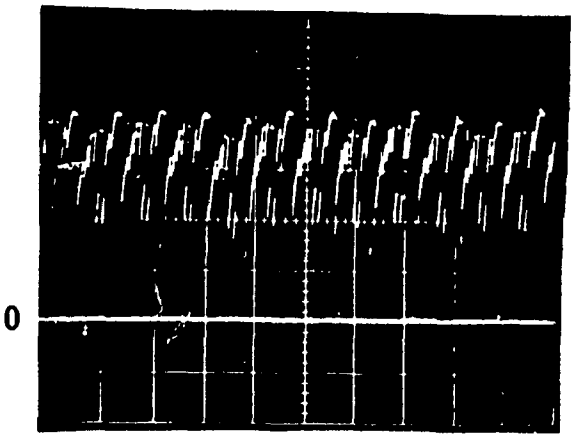
(a)



(b)



(c)



(d)

Fig. 4.15. Experimental results at dc bus for MCSI with M = 0.8, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Dc link inductor current, scale 2.5 A/div., 1 ms/div. (b) Dc bus current, scale 2.5 A/div., 1 ms/div. (c) Rectifier output voltage, scale 50 V/div., 2 ms/div. (d) Inverter input voltage, scale 50 V/div., 2 ms/div.

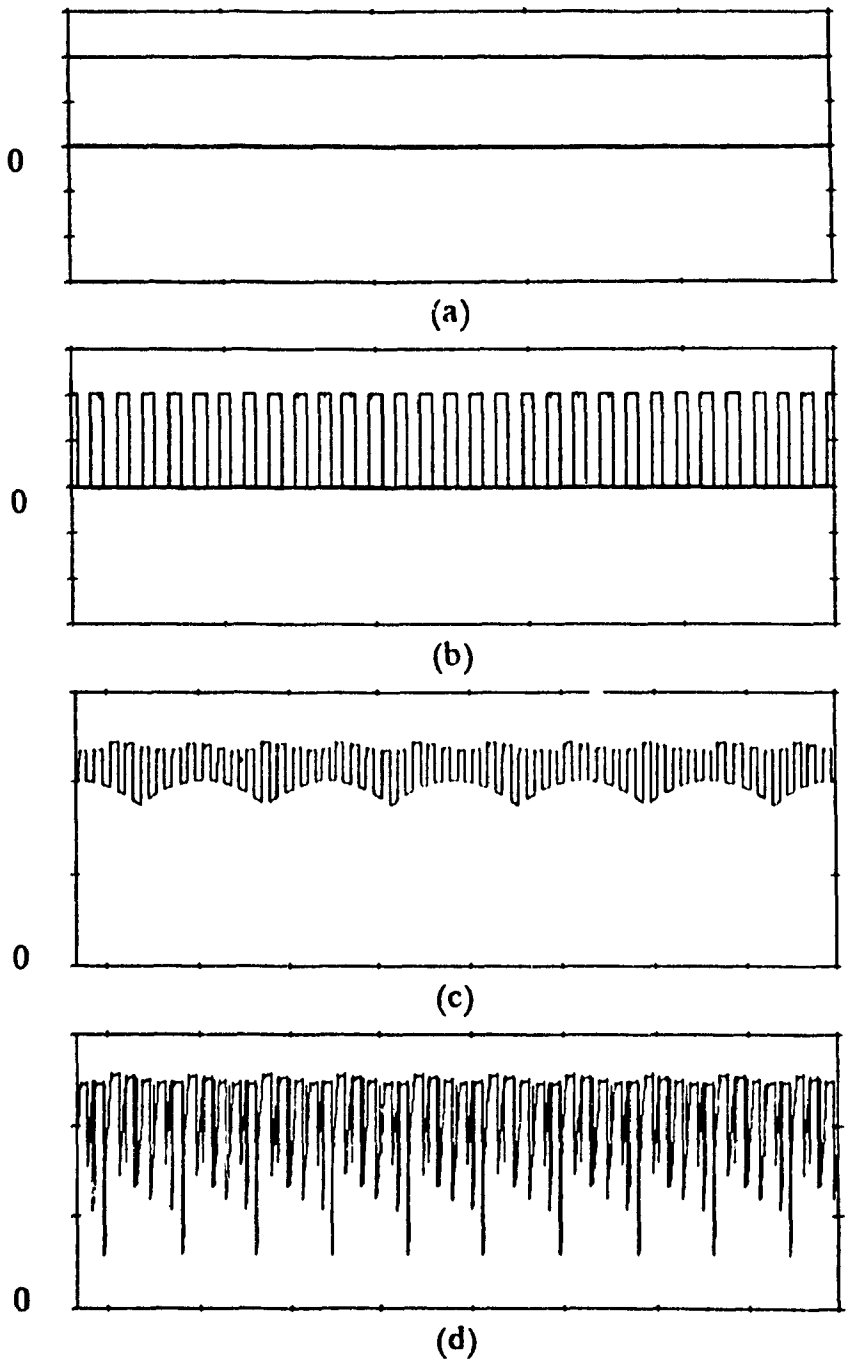


Fig. 4.16. Simulated results at dc bus for MCSI with M = 0.5, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Dc link inductor current, scale 10 A/div., 2 ms/div. (b) Dc bus currrent, scale 10 A/div., 2 ms/div. (c) Rectifier output voltage, scale 50 V/div., 2 ms/div. (d) Inverter input voltage, scale 50 V/div., 2 ms/div.

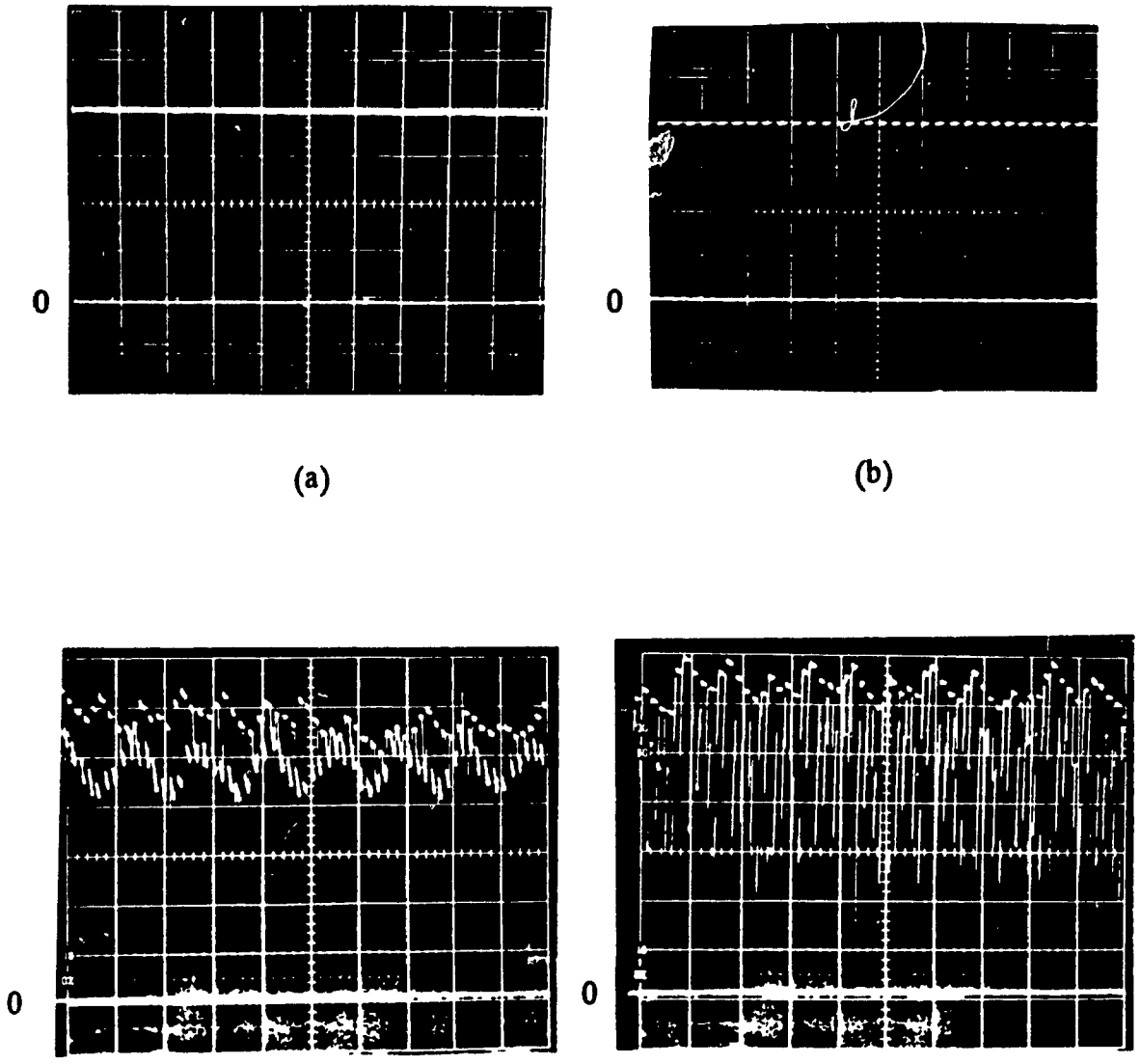


Fig. 4.17. Experimental results at dc bus for MCSI with M = 0.5, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, and C = 10 μF (L-L): (a) Dc link inductor current, scale 2.5 A/div., 1 ms/div. (b) Dc bus current, scale 2.5 A/div., 1 ms/div. (c) Rectifier output voltage, scale 50 V/div., 2 ms/div. (d) Inverter input voltage, scale 20 V/div., 2 ms/div.

4.5.2. Regenerative conditions

A notable characteristic of any CSI is that it does not require an additional converter for regeneration to occur unlike a VSI. In order to verify that the proposed topology can in fact operate under regenerative conditions, and that the switch connected across the dc link inductor does not detract from this capability in any way, the MCSI was tested under these conditions using the PSPICE program. The simulated results are shown in Fig. 4.18 and it can be seen that the power at the dc bus and inverter output is negative as the dc bus voltage is negative and the phase difference between the load current and line-neutral voltage is greater than 90°.

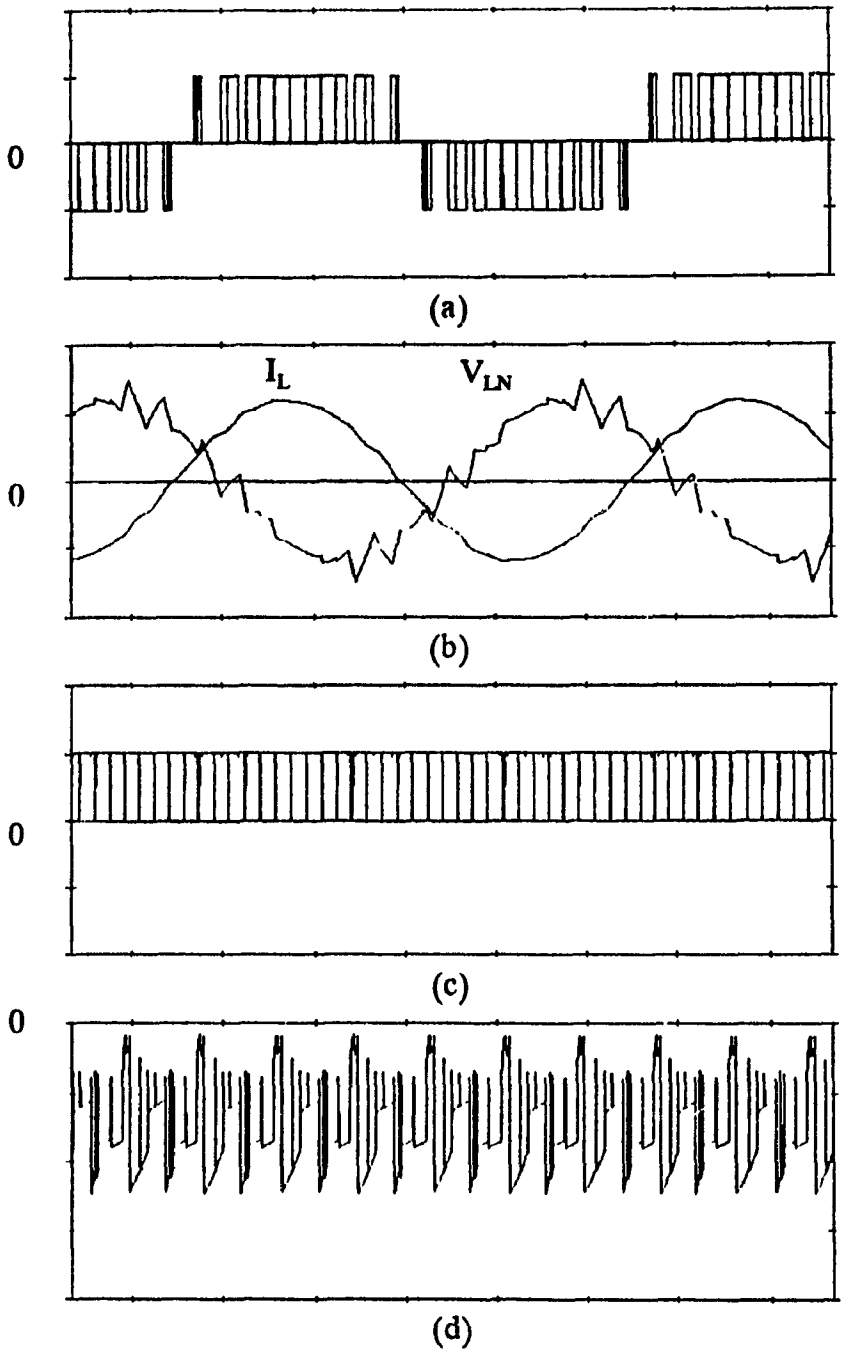


Fig. 4.18. Simulated results obtained for MCSI under regenerative conditions with M = 1, f_o = 100 Hz, and load R = 11 Ω, L = 7 mH, C = 10 μF (L-L): (a) Inverter output line current, scale 20 A/div., 2 ms/div. (b) Load current, scale 20 A/div., 2 ms/div., and line-neutral voltage, scale 200 V/div., 2 ms/div. (c) Dc bus current, scale 20 A/div., 2 ms/div. (d) Inverter input voltage, scale 200 V/div., 2 ms/div.

4.5.3 Transient conditions

It has been stated throughout this thesis that variable modulation index control allows the amplitude of the load currents to be changed instantaneously thus improving the dynamic response of a CSI with a phase-controlled front-end rectifier. In Fig. 4.19 variable modulation index control for the case where the amplitude of the load currents is to be reduced by half is compared to rectifier output control using a phase-controlled thyristor rectifier and a PWM rectifier. It can be seen that variable modulation index control allows the MCSI to have the best dynamic response of all the three cases and that the worst dynamic response is obtained when rectifier control is used and the front end converter is a phase-controlled rectifier.

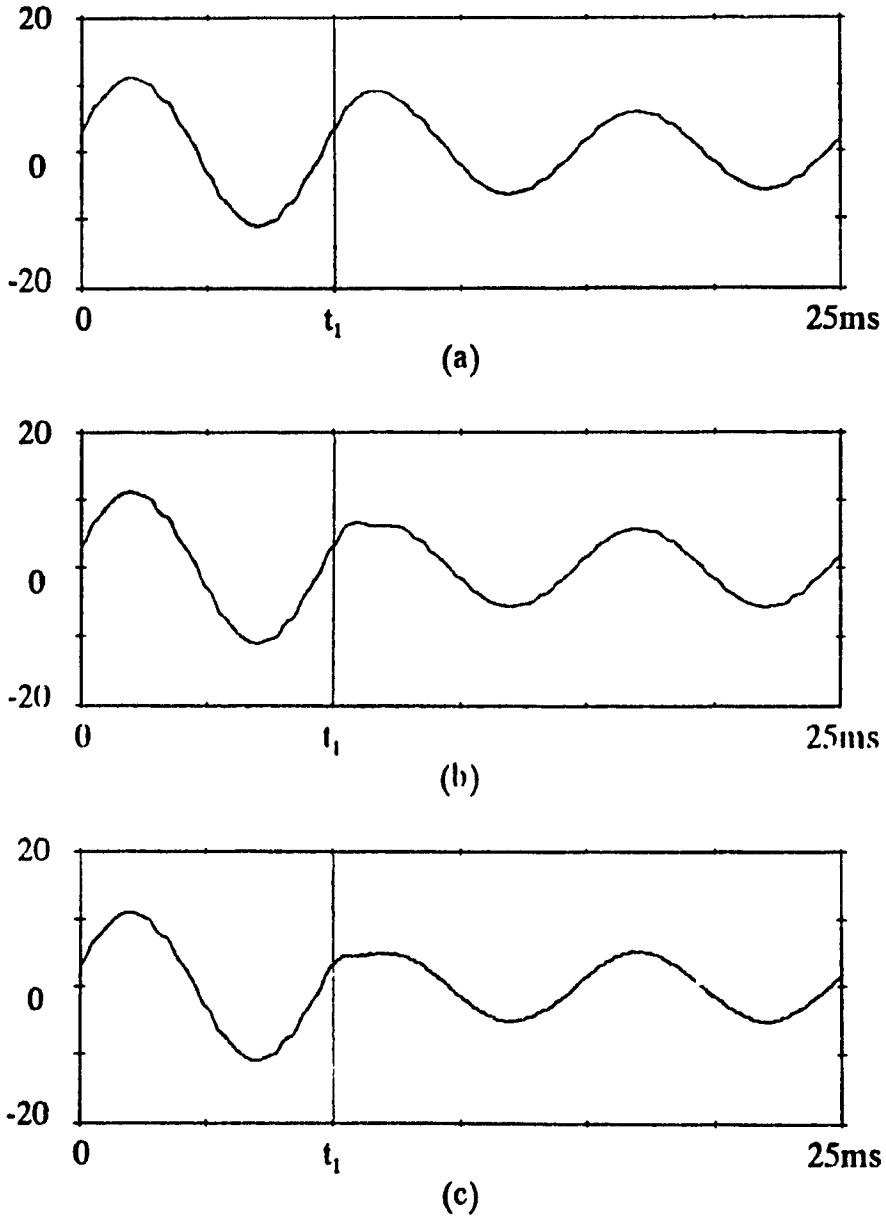


Fig. 4.19. Transient response of a CSI load current when it is reduced by one-half. f_o = 100 Hz, load R = 11 Ω and C = 10 μF (L-L): (a) Response when rectifier control is used with a thyristor rectifier and the dc link inductor is 40 mH. (b) Response when rectifier control is used with a PWM rectifier and the dc link inductor is 10 mH. (c) Response when variable modulation index control is used with the MCSI and the dc link inductor is 50 mH.

4.6. Conclusion

A modified PWM current source inverter (MCSI) with an auxiliary switch connected across the dc link inductor has been presented in this chapter. This switch allows any PWM pattern to be used, including VSI patterns and patterns with low modulation indices. It also allows the MCSI to be operated without short-circuiting the dc bus, and with a fast dynamic response. Since the operation of the MCSI differs from that of the conventional PWM CSI because of the switch, its characteristics are unique; therefore, the equations that are normally used to derive steady state operating points for a PWM CSI have been modified and design guidelines have been given. The equations derived have been used to examine several inverter relationships and used in a design example. Finally, the feasibility and performance of the MCSI have been verified by simulation and experimental implementation on a 5 kVA prototype.

CHAPTER 5 - INPUT CHARACTERISTICS OF THE MODIFIED CURRENT SOURCE INVERTER

5.1. Introduction

The MCSI has several unique characteristics which are not found on the conventional PWM CSI, such as a chopped dc bus current and overvoltages on the rectifier output voltage. The differences between the MCSI and the conventional PWM CSI are not only at the dc bus and output, but are also at the input. In this chapter, the input characteristics of the MCSI are presented, and the analysis of steady-state operation that was begun in the previous chapter is continued. Equations for the input current, rectifier firing angle and power factor are derived and are used to complete the design example. A comparison of several CSIs is then made on the basis of power factor and efficiency, and a design procedure for the dc link inductor and the input filter is presented. Finally, simulated and experimental results obtained on a 5 kVA prototype are shown to verify the filter design procedure.

5.2. The input ac line currents

It was shown in Chapter 4 that the MCSI has two basic modes of operation: mode 1, in which current is flowing through the rectifier, dc link, inverter and load and mode 2, in which current is freewheeling through the auxiliary switch. Since the

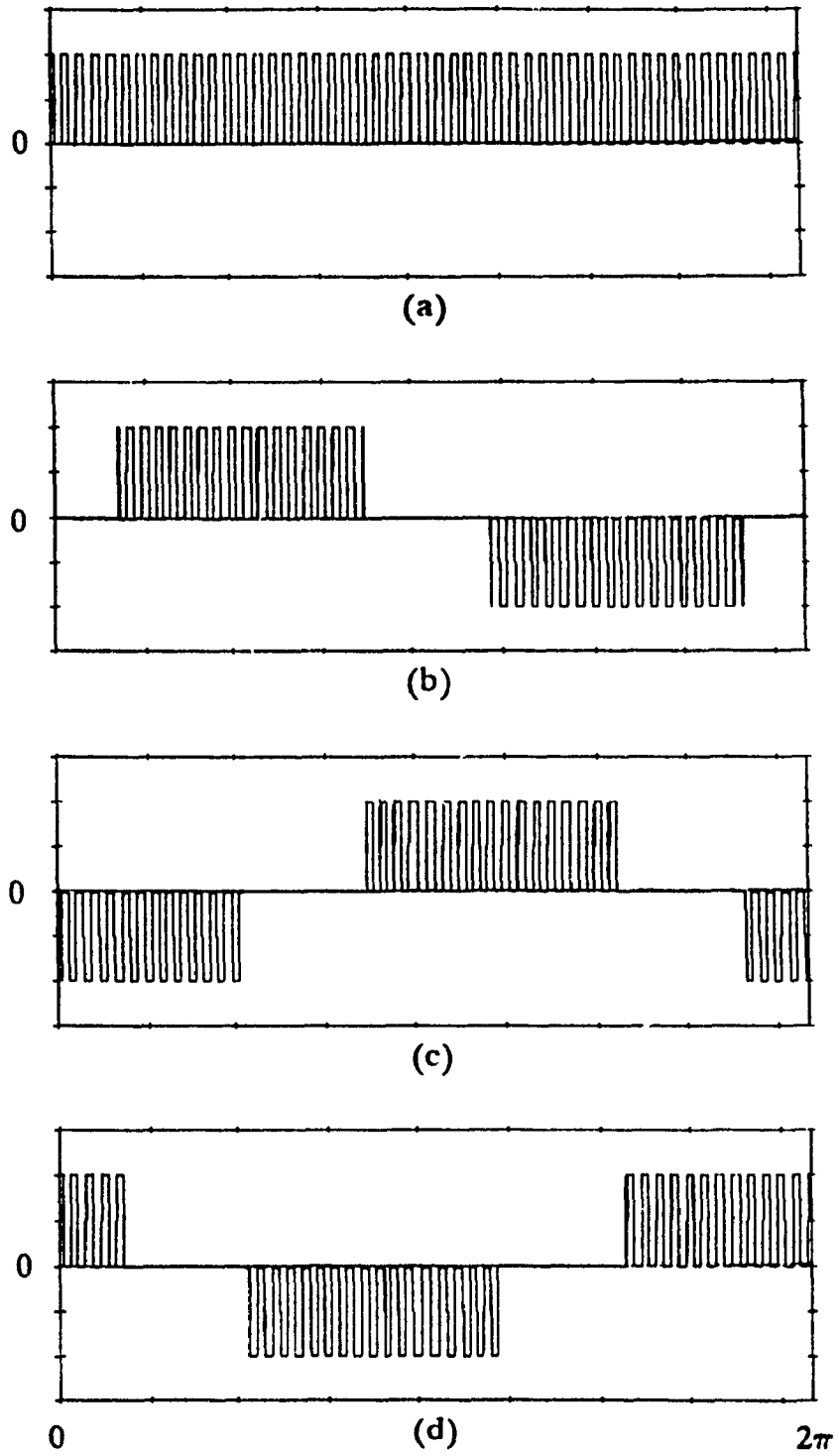


Fig. 5.1. (a) Dc bus current. (b)-(d) Input ac line currents

rectifier output current is chopped because of the two modes (Fig. 5.1(a)), so too are the input ac line currents. If the MCSI is fed by a thyristor rectifier, then the input currents are like those for a standard CSI - two square pulses of 120° width, one positive and one negative - but with the pulses chopped at twice the inverter switching frequency (Fig. 5.1(b)-(d)). The current spectrum contains harmonics associated with the operation of the rectifier along with additional high frequency harmonics due to the inverter operation. This phenomenon will be examined in greater detail in section 5.6 where the input filter design procedure is shown.

A design procedure to find steady-state operating points for the MCSI was presented in Chapter 4; however, since this chapter dealt with dc bus and output characteristics, the last step shown was the derivation of the average dc bus current and voltage, I_{dc} and V_{dc} (Fig. 5.2). Continuing from this point and assuming that the rectifier is lossless, the fundamental rms component of the ac input line current is

$$I_{ac} = K_{ac} I_{dc} \qquad (5.1)$$

where $K_{ac} = 0.78$.

The value of this constant can be found by considering that the dc bus current has an average value of I_{dc} (Fig. 5.3(a)), and that an ac input line current is made up of two 120° regions of the dc bus current containing I_{dc} as shown in Fig. 5.3(b). Therefore, the input current can be considered to be a six-step waveform (Fig. 5.3(c)) with additional high frequency components. The fundamental rms component of the line current is that of the six-step waveform and is 0.78 I_{dc} according to the equation derived in Chapter 2 for the ASCI. It has also been

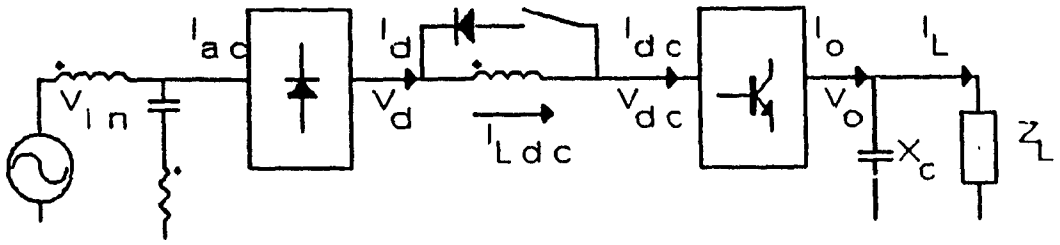


Fig. 5.2. MCSI line diagram.

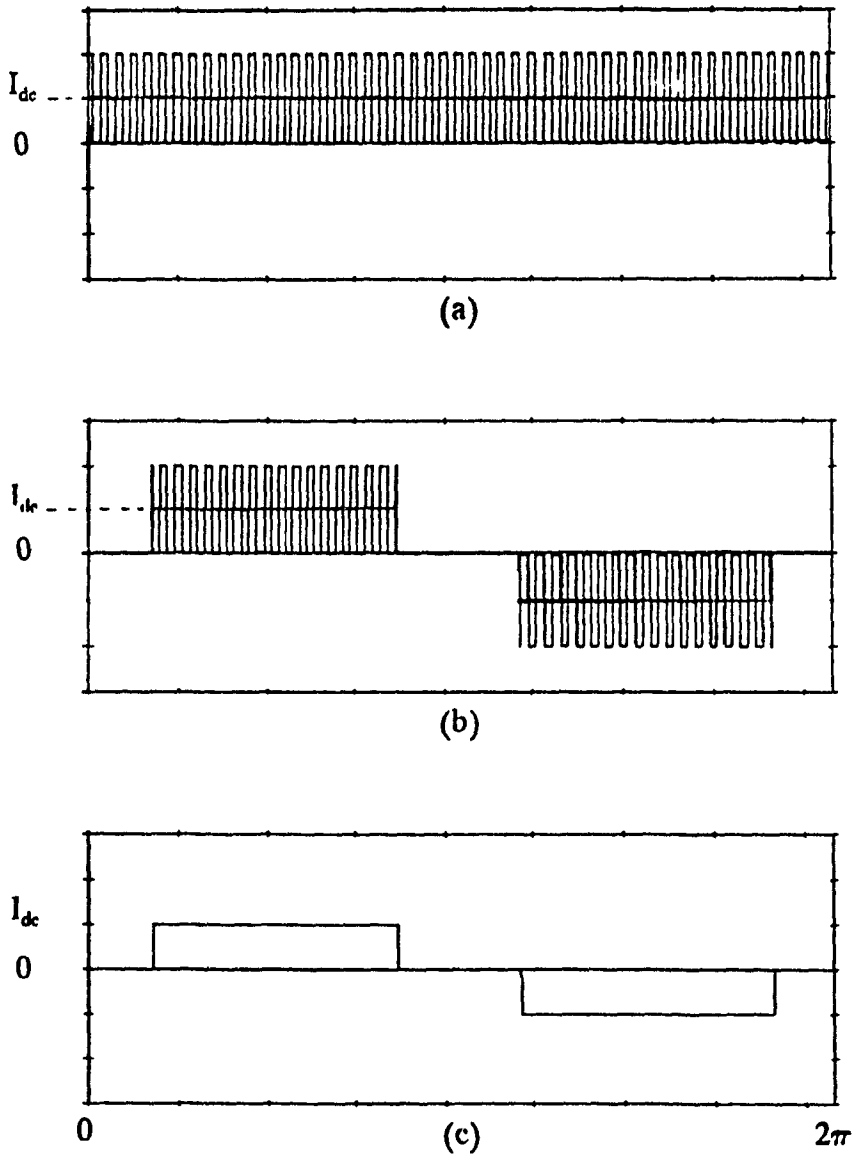


Fig. 5.3. (a) Dc bus current. (b) Input ac line current. (c) Equivalent input line current.

experimentally verified that the value of K_{ac} is in fact 0.78.

The total rms value of the input line current is

$$I_{acr} = \frac{I_{ac}}{D_m} \qquad (5.2)$$

where D_m is the ratio of the rms value of the fundamental component of the input ac line current to its total rms value. The value of D_m is dependent on the inverter PWM pattern used and the modulation index, and the relationship between D_m and M for a third harmonic injection SPWM pattern is shown in Fig. 5.4.

The rectifier firing angle is

$$\alpha = \cos^{-1}\left(\frac{P}{3 V_{ac} I_{acr} D_m}\right) \qquad (5.3)$$

where P = power on the dc bus

V_{ac} = input line to neutral voltage.

Finally, the input power factor is

$$pf = D_m \cos\alpha \qquad (5.4)$$

5.3. Design example (continued)

In chapter 4, a design example was presented for two induction motor operating points, one at rated conditions and the other at half-rated frequency and torque. The dc bus quantities were found to be

I_{dc} = 46.55 A (1.15 pu)

V_{dc} = 589.0 V (2.22 pu)

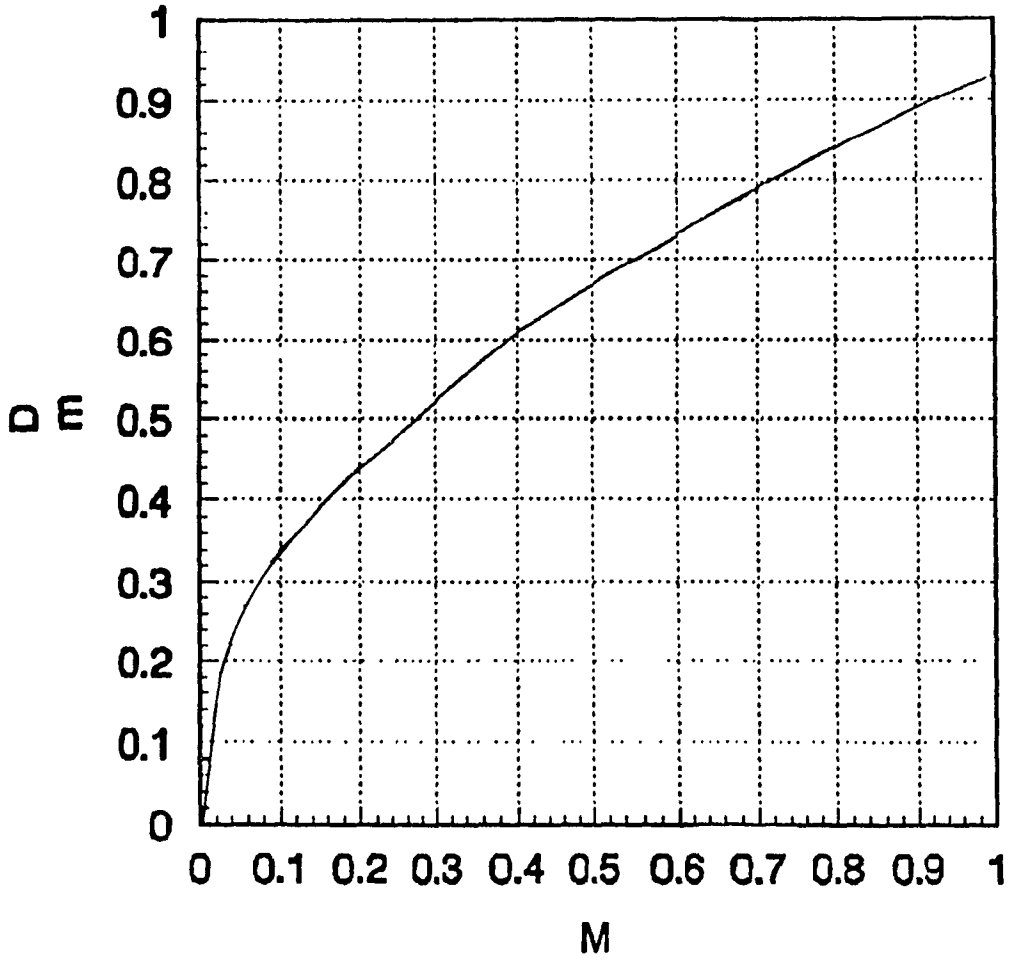


Fig. 5.4. Ratio of the rms value of the fundamental component to the total rms value of the input line current (D_m) vs modulation index (M) for a third harmonic injection SPWM pattern.

for rated conditions and

$$I_{dc} = 30.82 \text{ A } (0.76 \text{ pu})$$

$$V_{dc} = 230.94 \text{ V } (0.87 \text{ pu})$$

for half-rated frequency and torque. The example is continued here from where it was left off.

The fundamental rms component of the ac input line current can be calculated from equ. 5.1 and is

$$I_{ac} = (0.78)(46.55) = 36.31(0.90pu) \qquad (5.5)$$

The value of D_m for modulation index M = 1 for the third harmonic injection SPWM pattern used is 0.93, and the total input rms current can be found from equ. 5.2 and is

$$I_{acr} = \frac{36.31}{0.93} = 39.04(0.96pu) \qquad (5.6)$$

Since the input voltage is known to be 420 V line-line (or 242.5 line-neutral) and the dc bus quantities are known, they can be plugged into equ. 5.3 and the rectifier firing angle can be calculated to be

$$\alpha = \cos^{-1}\frac{(589.0)(46.55)}{(3)(242.29)(39.04)} = 15.26^\circ \qquad (5.7)$$

Finally, the input power factor can be calculated from equ. 5.4 and is

$$pf = 0.93\cos(15.26^\circ) = 0.90 \qquad (5.8)$$

The following values can be calculated for the second operating point by

using the same procedure:

$$I_{ac} = 24.04 \text{ A } (0.59 \text{ pu})$$

$$I_{acr} = 31.22 \text{ A } (0.77 \text{ pu})$$

$$\alpha = 71.70°$$

$$pf = 0.25$$

Note that the average output voltage of the rectifier in this case would normally be 178 V (1.35 x 420 cos 71.70°) but because of the overvoltage components on the bus it is 231 V instead.

5.4. Power factor considerations

In this section, the input power factor of the MCSI operating with a third harmonic injection SPWM pattern will be compared to that of the following three CSIs:

1) The autosequentially commutated inverter (ASCI) operating in the six-step mode (Fig. 5.5(a)).
2) The conventional six switch PWM CSI using the selective harmonic elimination technique (SHE CSI) shown in Fig. 5.5(b)). In this case, the peak of the fundamental component of the inverter output current, I_o is always equal to the average value of the dc link current, I_{dc} and the load current can only be changed by rectifier firing angle control.
3) The conventional PWM CSI with instantaneous current control capability

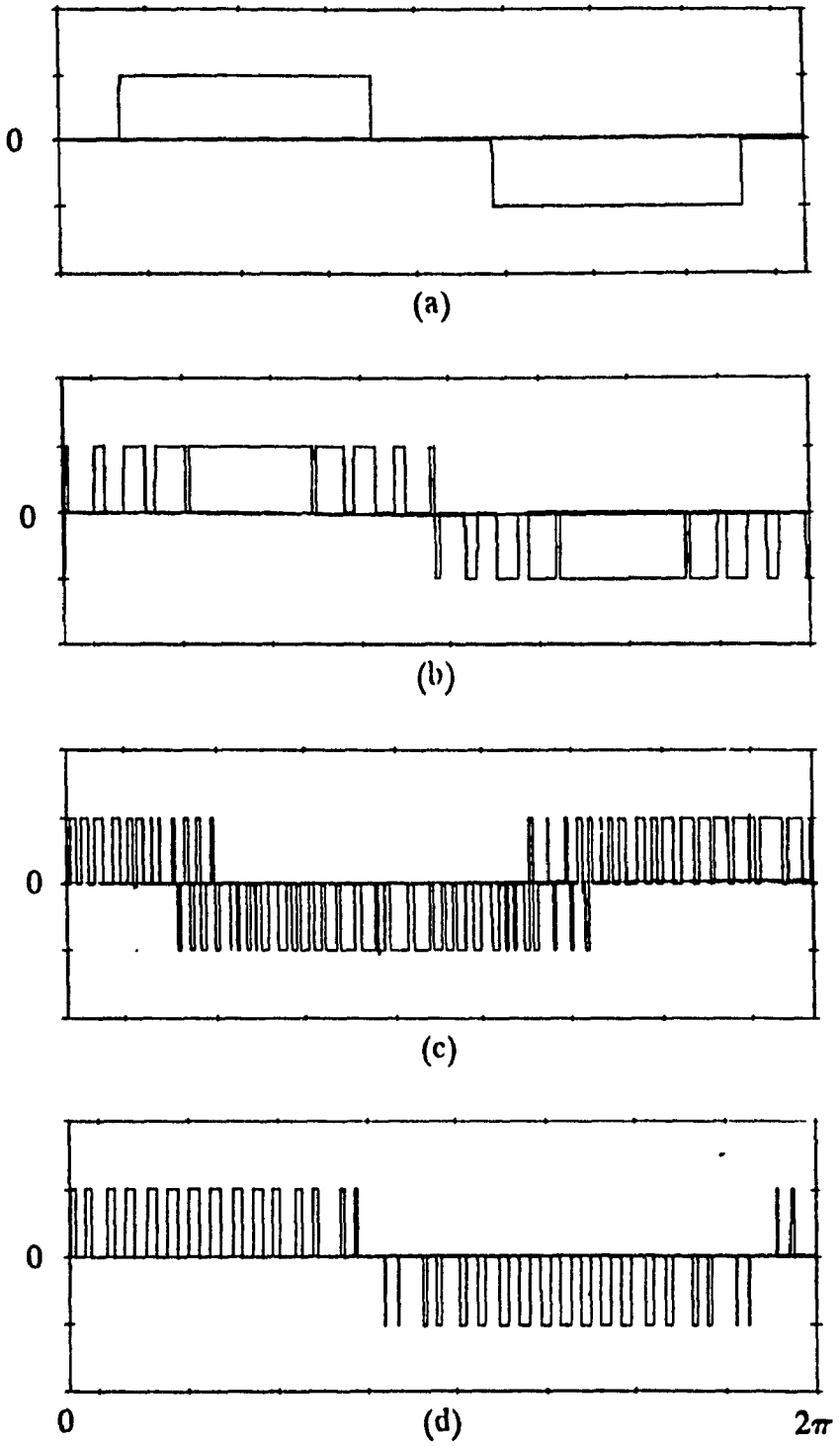


Fig. 5.5. Inverter output line currents for (a) ASCI. (b) SHE CSI. (c) ICCC CSI. (d) MCSI.

(ICCC CSI) as proposed by Enjeti et al. in [16]. In this case, variable modulation index control is implemented by short-circuiting the dc bus and the inverter pattern (Fig. 5.5(c)) is such that the peak of the fundamental component of I_o is equal to M times I_{dc}.

All these CSIs have a six switch inverter topology and square wave input currents as the inverter is fed by a phase-controlled rectifier. The following assumptions have been made for all four cases:

1) Only the rms value of the fundamental component of the ac quantities and the average value of the dc quantities are considered unless noted otherwise.
2) The output impedance, output power, and inverter output current of the inverter are identical.
3) The inverter and rectifier are lossless.
4) The rectifier firing angle is 0° for rated output power.

The equations defining the input power factor for the MCSI can be used to find the power factor for the other three cases with the following modifications:

1) Since there is no auxiliary switch and the current flowing into the inverter is the dc link reactor current, the value of K_s in equ. 4.5 is zero and equ. 4.4 becomes

$$I_{Ldc} = K_{dc} I_o \qquad (5.9)$$

where K_{dc} is 1.28 for the ASCI, 1.41 for the SHE CSI, and 1.41 / M for the ICCC CSI.

2) The value of D_m in equ. 5.2 is always 0.955.

The four CSIs can be compared on the basis of input power factor versus output power (pu) as is done in Fig. 5.6 and 5.7 for a load with 1 pu impedance and a 0.8 power factor. Fig. 5.5 shows the case when the load current is changed by varying only the firing angle of the input rectifier. The modulation index of the two variable modulation index controlled CSIs (the ICCC CSI and the MCSI) has been kept constant at M = 1. It can be seen from the graph that the power factor of the MCSI is slightly lower than that of the other CSIs - this is because of the distortion due to the chopping of the input line current.

Fig. 5.7 shows the case when variable modulation index control is used. From this graph, it can be seen that the MCSI has the better power factor although it is lower than that obtained using rectifier firing angle control. This is because the MCSI requires less adjustment at the rectifier to keep the dc link inductor current constant than the ICCC CSI, as was shown in chapter 4. This advantage, however, is partially offset by the distortion factor of the input current - especially when the modulation index is low - thus the power factor is not as high as it would be otherwise.

5.5. Efficiency considerations

In this section, the efficiency of the MCSI will be compared to that of the ASCI operating in the six-step mode and the conventional PWM CSI. The following three sources of losses are considered:

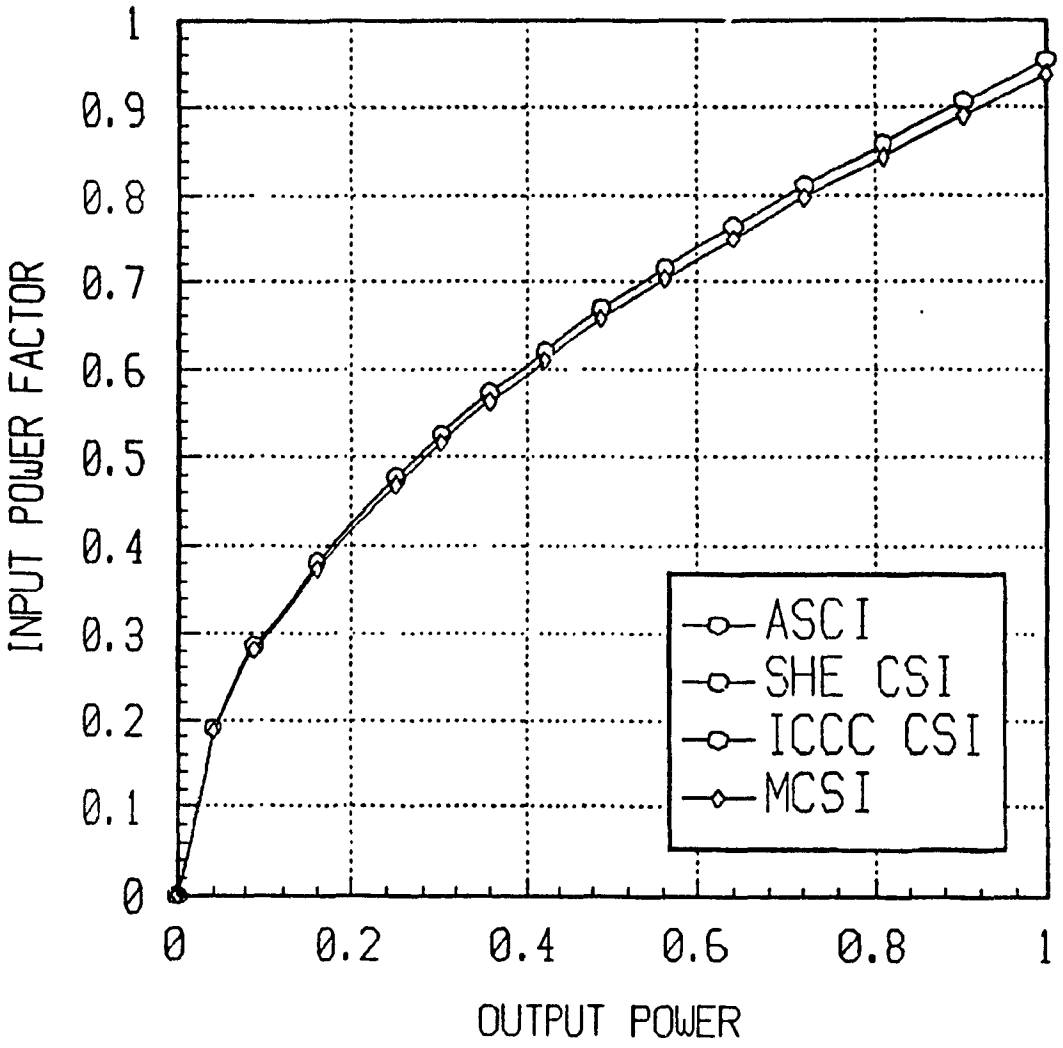


Fig. 5.6. Input power factor vs. output power (pu) when rectifier firing angle is used.

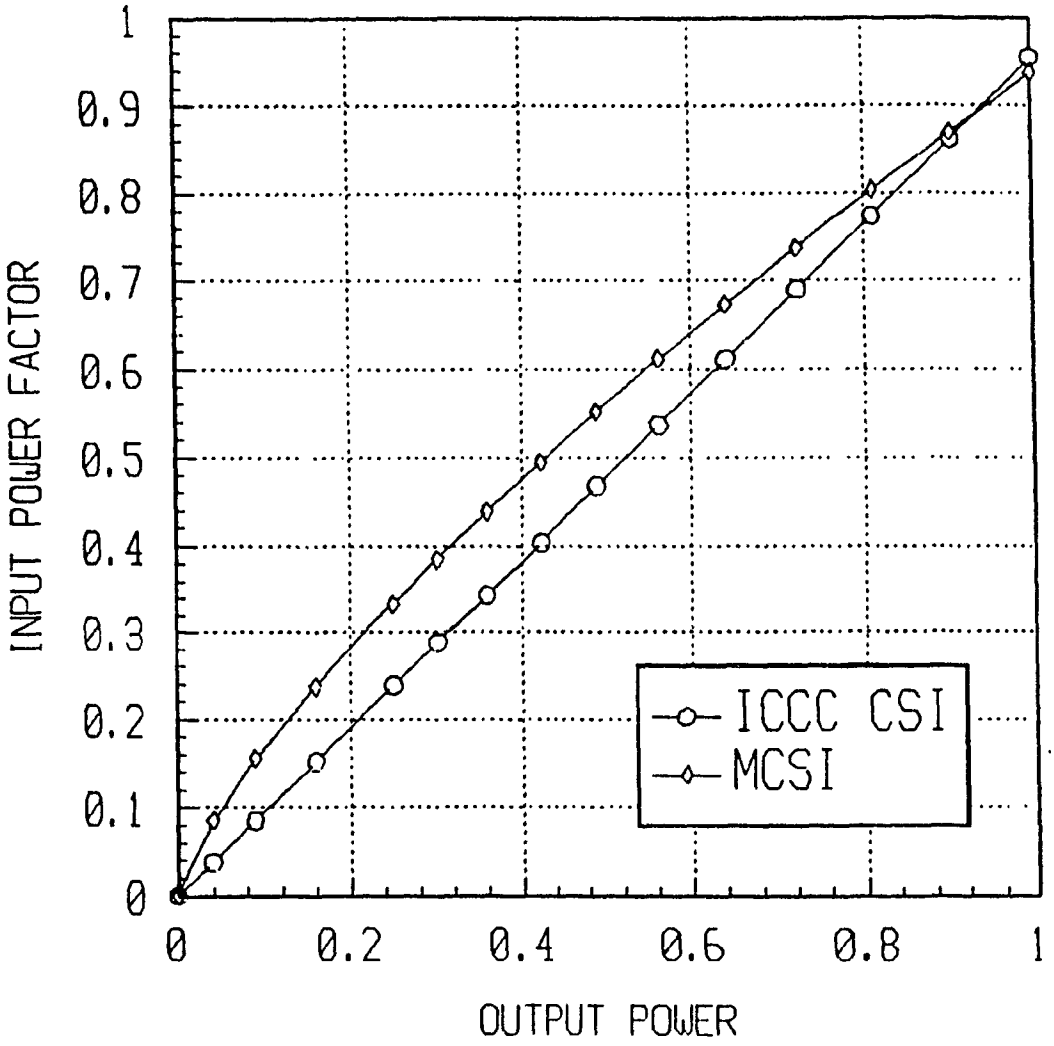


Fig. 5.7. Input power factor vs. output power (pu) when variable modulation index control is used.

1) Conduction losses

2) Switching losses

3) Harmonic losses in the load.

Input losses will be considered later in this chapter.

Of the three types of CSI considered, the MCSI has the lowest rectifier and inverter conduction losses because the current flowing in these converters is interrupted whenever the auxiliary switch is fired. This is not the case for the ASCI or the PWM CSI because current must always be flowing in the rectifer and the inverter. Therefore, conduction losses in the MCSI are reduced, especially when the modulation index of the inverter PWM pattern is lov and the auxiliary switch is fired more often.

The ASCI has the lowest switching losses because each switch is turned on and off only once per period. The MCSI has lower switching losses than the PWM CSI because for certain transitions, the inverter switches switch under zero current conditions. This occurs when the inverter switches turn off after the auxiliary switch is fired and current is freewheeled, and turn on just before current is about to be transferred from the auxiliary switch to the inverter. The auxiliary switch, however, has switching losses because it is not turned on or off under zero current conditions. Therefore, the switching losses of the MCSI are only slightly lower than those for the PWM CSI.

Although the ASCI has the lowest switching losses, it has by far the most harmonics losses at the load due to its square wave output currents. This makes the

ASCI inefficient from the load point of view, especially at light loads. This is not the case for the PWM CSI or for the MCSI because both produce sinusoidal load currents, even with a small filter, and thus induce low harmonic losses. It is easier, however, to reduce the harmonic losses in the MCSI because it is easier to implement PWM patterns having a low harmonic content on the MCSI than it is on the conventional PWM CSI.

From the comparison of the three types of CSI it can be concluded that at the dc bus and the load, the MCSI is the most efficient converter since its combined conduction, switching and load harmonic losses are the lowest.

5.6. Component design procedures

5.6.1. Design of the Link Inductor

The purpose of the link inductor is to convert the rectifier, which is a voltage source, into a current source and to attenuate the voltage ripple on the dc bus so that that a ripple free dc link inductor current can be obtained. A design procedure for this component must take the harmonics produced by the input rectifier into account since they contribute to the voltage ripple along with those produced by the inverter input operation. In general, a compromise in the size of the inductor must be made between the small inductance needed for a good transient response and the large inductance needed to minimize the voltage ripple; however, since the MCSI can be operated with variable modulation index control, the inductor can be

oversized without affecting the transient response.

The voltage ripple is applied across the inductor whenever the auxiliary switch is open. The dominant components produced by the inverter are at multiples of six times the inverter fundamental frequency and close to multiples of the switching frequency. The dominant component produced by the rectifier, V_r, is at six times the line frequency (f_r = 360 Hz). This rectifier component is the dominant overall component in terms of ripple generated and is largest when the rectifier delay angle is 90°. If it is assumed that the inductor current ripple resulting from this component is attenuated by a factor A_{dc}, with respect to the rated average inductor current, $I_{Ldc,rat}$, then the following equation can be derived,

$$\frac{V_r}{2\pi f_r L_{dc}} = \frac{I_{Ldc,rat}}{A_{dc}} \qquad (5.10)$$

or

$$L_{dc} = \frac{A_{dc} V_r}{2\pi f_r I_{Ldc,rat}} \qquad (5.11)$$

For example, the link inductor for the inverter used in the design example can be found to be 35.72 mH by substituting $I_{Ldc,rat}$ = 48.74 A, V_r = 225 V (for a 420 V ac rectifier input), f_r = 360 Hz, A_{dc} = 20 into equ. 5.11.

5.6.2. Input filter considerations

5.6.2.1. Theoretical considerations

Since the MCSI input ac line current are two 120° wide square pulses that are chopped due to the freewheeling of the current through the auxiliary switch (Fig. 5.1), the harmonic content of the line current consists not only of harmonics due to the operation of the rectifier, which occur at

$$f_h = (6n \pm 1) f_{in} \qquad (5.12)$$

but also of harmonics produced by the inverter operation which occur at

$$f_h = 2nf_{sw} \pm f_o \qquad (5.13)$$

where n = 1, 2, 3, ...

f_{in} = input frequency

f_{sw} = output switching frequency

f_o = output frequency.

Therefore, input filtering is required to prevent these additional harmonics from being dumped onto the ac mains. This can be done by using a second order filter consisting of a line inductor L_f, and a capacitor C_f connected in series with a damping resistor R_f. R_f prevents the amplification of harmonics close to the L_fC_f resonant frequency.

When designing the input filter, the following should be considered:

1) The filter should be designed to attenuate only the additional line current

harmonics created by the chopping of the dc bus current without affecting the harmonics caused by the rectifier operation. To do this, the break frequency (f_b) of the filter should be placed in an empty band of the rectifier input current harmonic spectrum. The value of R_f should be large enough so that the low frequency harmonics are not significantly amplified when f_b is low, yet small enough so that R_f-C_f filter branch has a low impedance at two times the switching frequency. Equations for the break frequency and R_f are

$$f_b = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{5.14}$$

$$R_f = Q\sqrt{\frac{L_f}{C_f}} - R_L \tag{5.15}$$

where Q is the quality factor of the filter and R_L is the line resistance.

2) The dominant high frequency harmonics occur at $2f_{sw} - f_o$, and $2f_{sw} + f_o$, and their amplitude is the highest when the modulation index of the inverter PWM pattern is 0.5.

In addition to attenuating harmonics, the filter can also offset the decrease in power factor when variable modulation index control is used for the MCSI. This is because the filter capacitor can act as a reactive power source supplying VARs to the system thus improving the power factor and reducing the drawback of using variable modulation index control.

In order for this to be done, however, the break frequency of the filter must

be low and the damping resistor R_f is needed to prevent the harmonics near f_b from being amplified. If R_f is present in the filter, then there will be an increase in the losses at the input. These losses, however, can be minimized if the inverter switching frequency f_{sw} is made high enough so that little if any resistance is needed to prevent the filter from amplifying the low frequency line current harmonics caused by the operation of the rectifier. Therefore, even with the input filter, the MCSI is still more efficient than the ASCI and the conventional PWM CSI; however, the poorer input power factor resulting from variable modulation index control will not be compensated.

5.6.2.2. Input filter design example

In order to illustrate the use of the input filter design equations, an example is presented for a three phase 5 kVA, 208 V, 60 Hz system with a load resistance of 11Ω and a load inductance of 7 mH per phase. The output frequency, f_o is 100 Hz and the output switching frequency, f_{sw} is 1500 Hz - these values are the same as those used in section 4.5.

The break frequency of the filter is set to 720 Hz (12 x 60 Hz). From equ. 5.14, $L_f C_f$ is 4.9 x 10^{-8}; if the value of L_f is set to 2 mH then C_f is equal to 25 μF. If the quality factor of the filter is set to 1.1 and R_L is considered negligible then R_f is equal to 10 Ω. Since the output switching frequency is f_{sw} = 1500 Hz, the dominant high frequency harmonics will be at 2900 Hz and 3100 Hz (2 x 1500 - 100,

2 x 1500 + 100).

The VA rating of the filter components are as follows:

C_{fva} = 136 VA = 0.08 pu

L_{fva} = 142 VA = 0.09 pu

Total VA per phase = 278 VA = 0.17 pu

Fig. 5.8 shows that the input filter offsets the decrease in power factor for a load with 1 pu impedance and a 0.8 power factor. Figs. 5.9(a) and 5.9(c) show the Fourier spectrum of a simulated unfiltered input line current with the modulation index of the inverter pattern equal to 0.8 and 0.5 respectively while Figs 5.8(b) and 5.8(d) show the filtered spectrum. From these waveforms, it can be seen that the high frequency harmonics have in fact been attenuated.

5.7. Experimental results

A 5 kVA prototype was constructed to confirm all the theoretical results, including the input characteristics of the MCSI, and the input filter design procure. Figs. 5.10 and 5.11 show the waveforms obtained under the conditions mentioned in the previous section with modulation indices of 0.8 and 0.5 respectively. It can be seen that the distortion introduced by the high frequency line current components has been effectively reduced. There is, however, a slight discrepency between the simulated and experimental results since there are some additional low order harmonics in the experimental input line currents because they are not

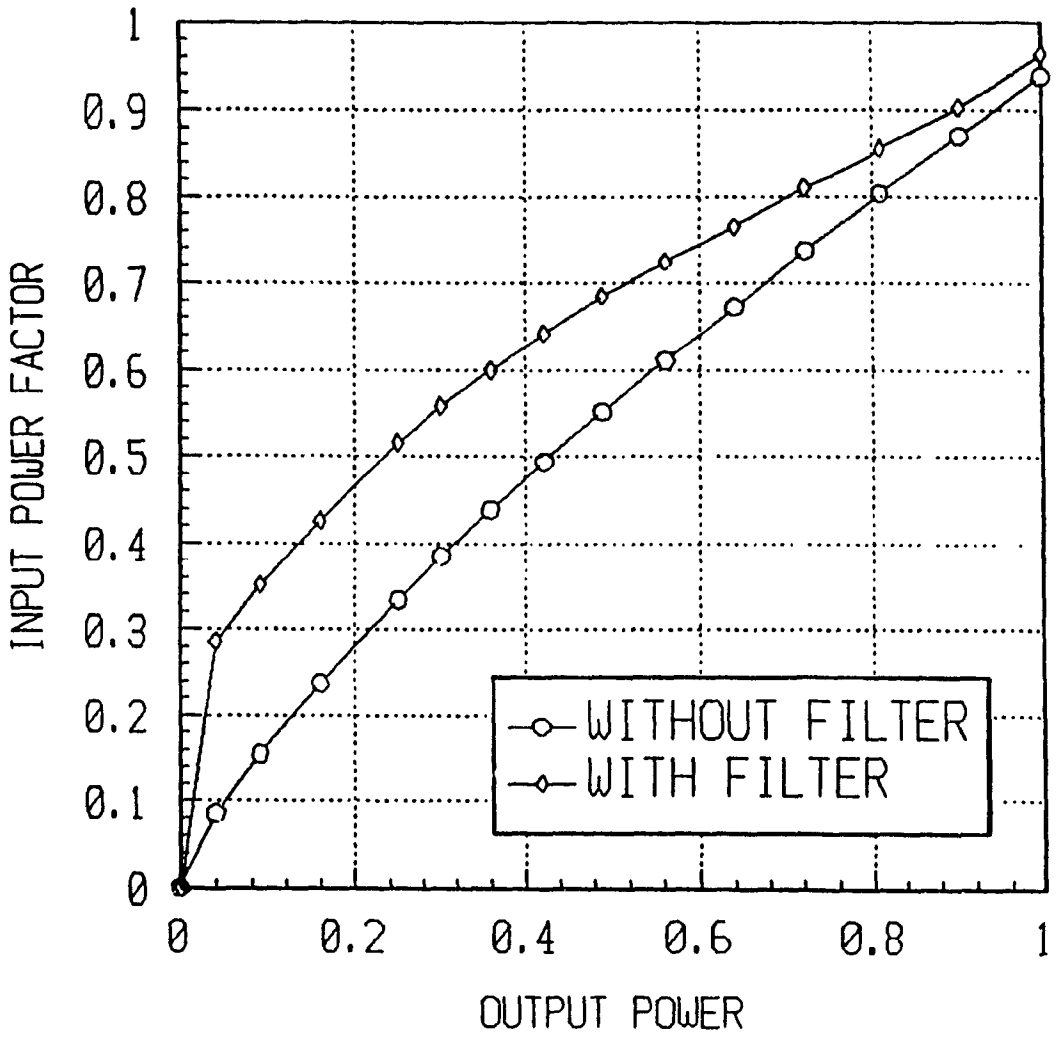


Fig. 5.8. Input power factor vs. output power (pu) for MCSI with and without input filtering.

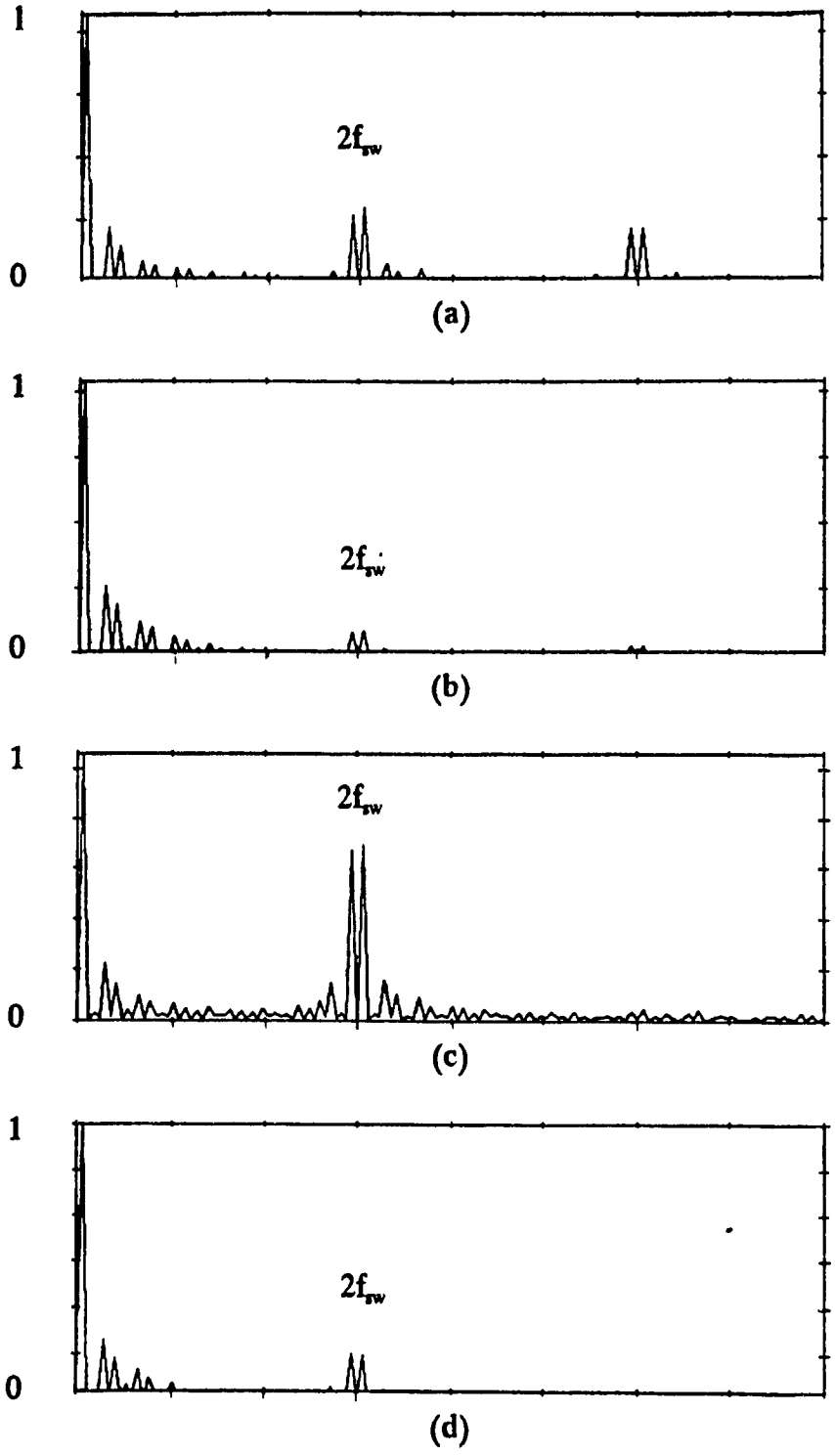
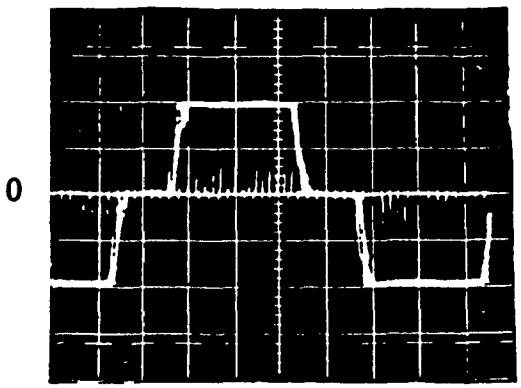
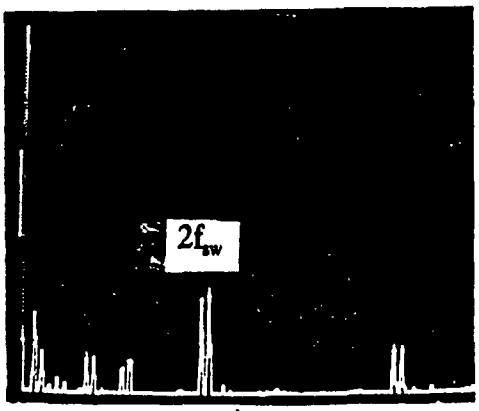


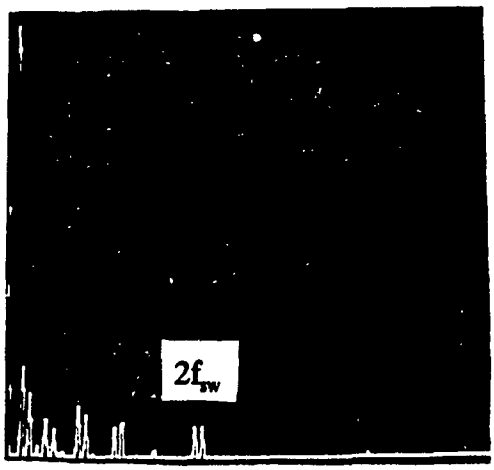
Fig. 5.9. Input current harmonic spectrum when f_o = 100 Hz and f_{sw} = 1500 Hz for (a) M = 0.8, unfiltered. (b) M = 0.8, filtered. (c) M = 0.5, unfiltered. (d) M = 0.5, filtered (range 0 - 8 kHz).



(a)

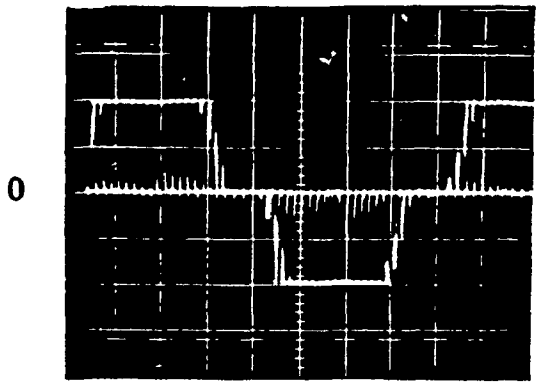


(b)



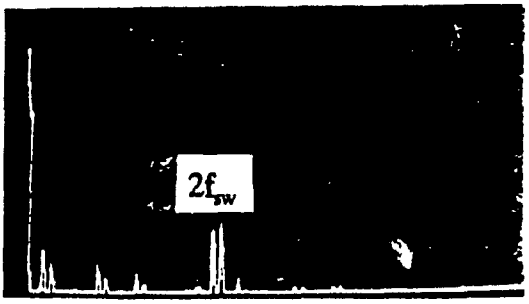
(c)

Fig. 5.10. Experimental results for MCSI with M = 0.8, f_o = 100 Hz, and f_{sw}: (a) Rectifier input line current, scale 5 A/div., 2 ms/div. (b) Rectifier input line current harmonic spectrum, range 0-8 kHz. (c) Filtered line current harmonic spectrum, range 0-8 kHz.



(a)

(b)



(c)

Fig. 5.11. Experimental results for MCSI with M = 0.5, f_o = 100 Hz, and f_{sw}: (a) Rectifier input line current, scale 5 A/div., 2 ms/div. (b) Rectifier input line current harmonic spectrum, range 0-8 kHz. (c) Filtered line current harmonic spectrum, range 0-8 kHz.

perfectly square but are trapezoidal instead.

5.8. Conclusion

The input characteristics of the MCSI have been investigated in this chapter. Equations describing the steady state operating input characteristics have been derived and used to compare the input characteristics of the MCSI with those of other CSIs. These comparisons have shown that the combined displacement and distortion power factor of the MCSI for modulation index M = 1 is only slightly lower than that of a six step inverter and other PWM CSIs. Moreover, when variable modulation index control is used, its power factor is superior to that of a conventional PWM CSI although this type of control tends to make the input power factor worse. A design procedure for the dc link inductor and the input filter has also been presented and it has been shown that the filter improves the input power factor in addition to eliminating high frequency harmonics so that the advantages of the MCSI can be gained without any penalty on input power factor and system efficiency. Finally, the input characteristics of the MCSI and the input filter design procedure have been verified on an experimental 5 kVA prototype.

CHAPTER 6 - CONCLUSION

6.1. Summary of the thesis

The contents of this thesis can be summarized as follows. In Chapter 2, several existing CSI PWM patterns have been presented. It has been shown that patterns having PWM in the center 60° region of each half-cycle eliminate more low-order harmonics than those that do not, and that these patterns can be implemented only when the dc bus is short-circuited at selected time intervals. Short-circuiting the dc bus also allows the output current to be controlled from the inverter instead of from the rectifer. The conventional PWM CSI topology limits the use of carrier PWM techniques, however, this limitation can be removed with the addition of an auxiliary switch.

It has been demonstrated in Chapter 3 that if the rectifier output voltage is not adjusted, then the dc link current of a conventional PWM CSI will rise whenever the modulation index of the inverter pattern or the output power factor is decreased. The dc bus current will also rise if it is attempted to improve the dynamic response of the CSI and suppress the overvoltage spikes on the inverter output voltage by short-circuiting the dc bus - especially if the modulation index of the inverter pattern or the fundamental frequency of the inverter is low. A new topology - one with an auxiliary switch connected across the dc link inductor - from which the benefits of short-circuiting the dc bus (such as an improved transient response) can be obtained

without the disadvantages has been proposed.

The characteristics of the new topology have been presented in Chapter 4 and compared to those of the conventional PWM CSI. Some of the more notable characteristics of the modified current source inverter (MCSI) are the appearance of overvoltage components on the rectifier output voltage, and a dc link current that is chopped. A design procedure for the proposed topology has been derived and used in an example to calculate the inverter quantities for two load operating points. The feasibility of the converter has been verified by simulation and experimental implementation.

The input characteristics of the MCSI have been presented in Chapter 5. It has been shown that the operation of the auxiliary switch causes the ac input line currents to be chopped, unlike those for the conventional PWM CSI. Equations relating the dc bus quantities to the input quantities have been derived and used to compare the input power factor of the MCSI to that of other CSIs. The input power factor and efficiency has been compared to other CSIs. Since the MCSI input line currents contain high frequency harmonics, input filters must be designed to filter out these harmonics. A design procedure for the input filters has been presented and confirmed by simulated and experimental results.

6.2. Conclusions

The following can be concluded from the analysis and comparisons of the

proposed topology with the conventional PWM CSI:

1) The MCSI has all the advantages that can be obtained by short-circuiting the dc bus of a conventional PWM CSI without the associated disadvantages. These benefits include the implementation of PWM patterns having PWM in the center 60° of each half-cycle (i.e carrier PWM), the use of variable modulation index control, and the suppression of the inverter output voltage spikes.
2) Variable modulation index control allows the MCSI to have a fast dynamic response even though it has a phase-controlled rectifier as the front-end converter and a large inductor in the dc link. This type of control results in a poorer input power factor than when rectifier control is used as the front-end rectifer must be phased back to prevent the dc link inductor current from rising. However, the input power factor obtained when using variable modulation index control is used with the MCSI is not as poor as it is when this type of control is used with a conventional PWM CSI.
3) The benefits of the MCSI are obtained at the expense of an extra switch and additional input filters. The input filters eliminate the high frequency components that appear on the ac mains due to the operation of the auxiliary switch, but not the low order harmonics due to the operation of the rectifier. The input filter capacitor has been shown to improve the input power factor of the CSI obtained when variable modulation index control is used but this can be done only when the break frequency of the filter is low. In this

however, a damping resistor is needed to prevent the amplication of low-order harmonics and this increases the losses at the input.

6.3. Suggestions for future work

The following suggestions can be made for future work.

1) The presence of an auxiliary switch in the dc link allows a greater number of PWM patterns to be implemented on the MCSI than on the conventional PWM CSI because the general rule that the inverter must always provide a path for current can be violated. Since the rules for MCSI patterns are less restrictive, new and improved PWM patterns can be developed for CSIs (i.e. patterns with less line current harmonics or patterns that produce smaller switching losses).
2) The characteristics of the MCSI have been studied with a static load and under open loop conditions, but not with an induction motor load under closed loop conditions; therefore, research into the operation of the MCSI when used under closed loop conditions can be done.

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APPENDIX

The layout of the experimental prototype is shown in Fig. A.1. The inverter was fed from an autotransformer that was connected to the 208 V ac mains. A diode rectifer was used as the front-end converter and the load was a static R-L load. This rectifier and load were used because it was considered unnecessary to connect the prototype to a phase-controlled rectifier and an induction motor load in order to prove that the proposed topology was feasible, and to analyze its characteristics.

The gating signals for the inverter switches and the auxiliary switch were obtained from the logic circuit shown in Fig. A.2. The main component of this circuit was an EPROM which contained 16 third harmonic injection SPWM patterns with various modulation indices ranging from 0.1 to 1. The modulation index of the pattern was selected with the variable resistor at the A/D converter, while the frequency of operation was selected with the variable resistor at the frequency generator.

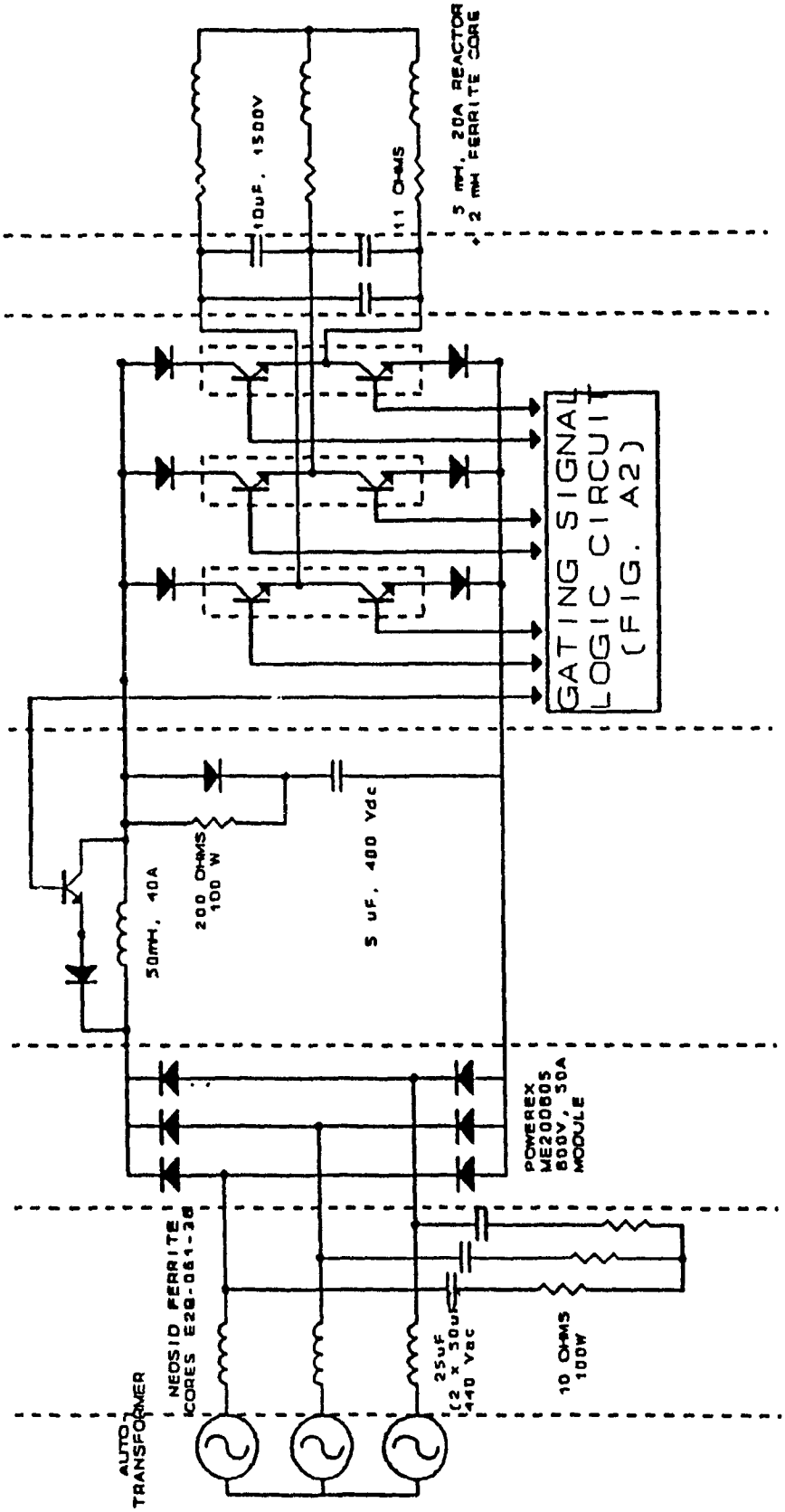

Fig. A1. 5 kVA experimental prototype unit.

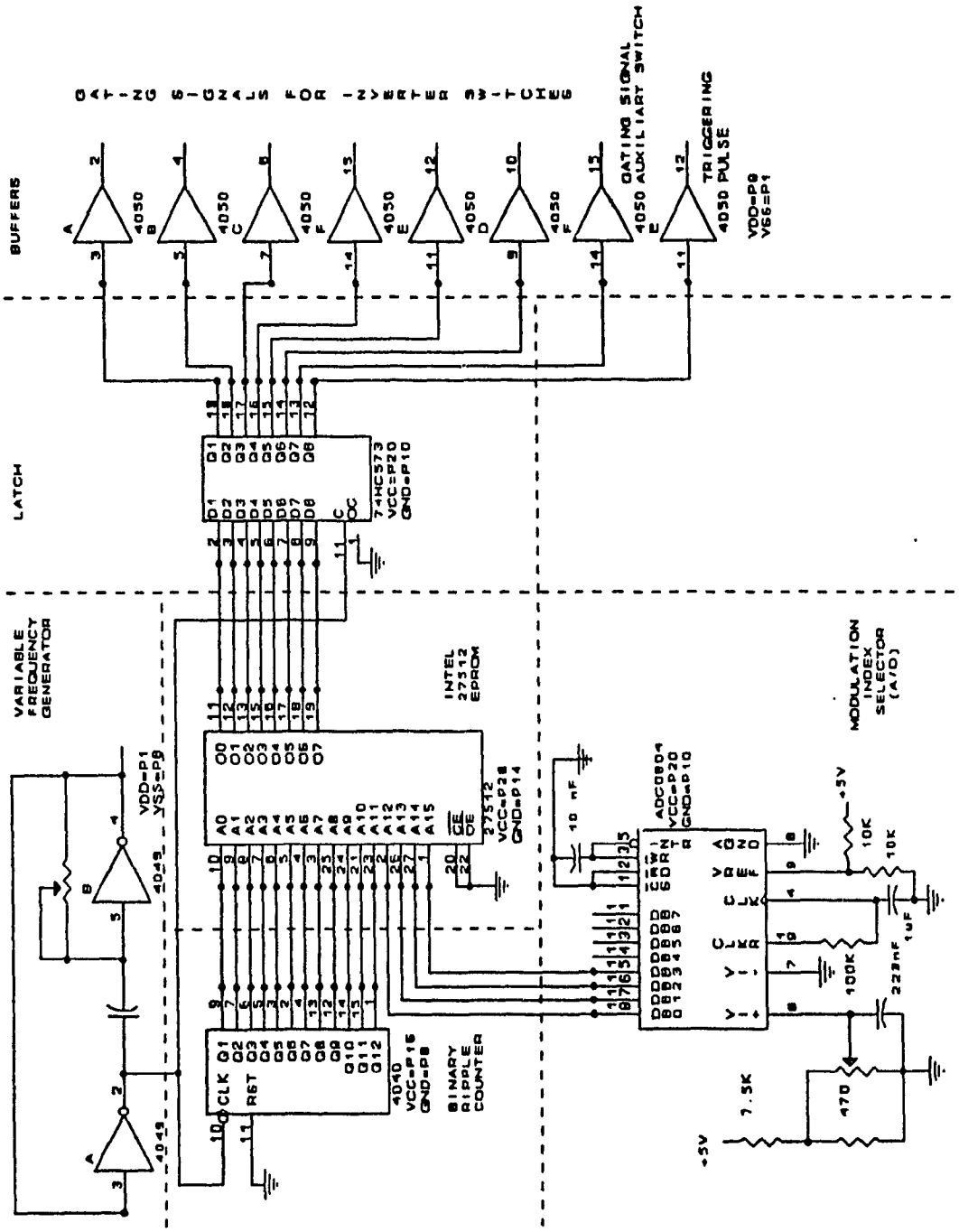

Fig. A2. Layout of gating signal logic circuit.