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AC/DC POWER CONVERSION SCHEMES WITH UNITY POWER FACTOR AND MINIMUM HARMONIC DISTORTION

Navid Reza Zargari

A Thesis

in

The Department of Electrical & Computer Engineering

Presented in Partial Fulfilment of the Requirements

for the Degree of Doctor of Philosophy at

Concordia University

Montréal, Québec, Canada

March 1995

ISBN 0-612-01278-6

Canada

ABSTRACT

AC/DC POWER CONVERSION SCHEMES WITH UNITY POWER FACTOR AND MINIMUM HARMONIC DISTORTION

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Concordia University, 1995.

In most line-interfaced power converter applications the ac mains voltage is first rectified into a dc voltage or current, which is subsequently converted into voltages and currents of appropriate amplitude, frequency and shape to meet the load requirements. The front-end rectifier must satisfy three main requirements: (a) Minimum harmonic injection into the ac mains should comply with limits imposed by recommended standards such as IEEE-519, IEC-555. (b) High input power factor to reduce the reactive power requirements. (c) High efficiency and reliability and low cost to ensure competitiveness on the market. The challenge is therefore to provide a conversion scheme which delivers high quality output waveforms without distorting the ac mains and without drawing any reactive power. Successful application of PWM techniques to forced commutated converters has prompted recent investigation in finding more suitable topologies for ac to dc conversion. Two structures have evolved based on the characteristics of the dc link: the current source topology and the voltage source topology. This thesis investigates these two topologies and proposes a number of control schemes to achieve unity displacement factor operation and fast response. For the current source topology two control methods, a closed loop and a feed-forward scheme, are proposed. The feed-forward scheme is based on phase shifting the gating patterns of individual switches to compensate the effect of the input filter and load operating point. Furthermore, the feed-forward scheme is combined with a control strategy to eliminate the need for damping resistors. For the voltage source topology, a simple control strategy is proposed to obtain a near unity power factor input stage for voltage source inverter based ac drive applications. Also, performance of current controlled voltage source type rectifiers in rotating and stationary frames is investigated.

Small signal models are developed for both topologies and different transfer functions are derived for each structure. The theoretical considerations are verified by simulation and by experiments on laboratory prototypes.

ACKNOWLEDGEMENTS

I wish to express my sincere gratitude to my supervisor, Dr. Geza Joos for his valuable guidance and encouragement throughout the course of this study.

Special appreciation goes to late Dr. P.D. Ziogas with whom this work was initiated, for his useful advice and discussions.

Thanks are extended to my many friends in the Power Electronics Lab, who made the period of this study more pleasant and fruitful. Special thanks to Mr. José Espinoza for many helpful discussions we shared.

Financial support from Natural Science and Engineering Research Council of Canada (NSERC) and Québec Ministry of Education (FCAR) are gratefully acknowledged.

To my parents

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List of Acronyms

ASD	Adjustable Speed Drive
CSI	Current Source Inverter
DF	Distortion Factor
GTO	Gate Turn Off thyristor
IDF	Input Displacement Factor
IGBT	Insulated Gate Bipolar Transistor
HVDC	High Voltage Direct Current
NN	Neural Network
PF	Power Factor
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PWM	Pulse Width Modulated
PWMBR	Pulse Width Modulated Buck Rectifier
PWMSR	Pulse Width Modulated Synchronous Rectifier
rms	root mean square
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse Width Modulated
SVM	Space Vector Modulated
THD	Total Harmonic Distortion
VSI	Voltage Source Topology

List of Main Symbols

Currents:

I	peak ac current
I_{rms}	rms value of the current
I_{sw}	switch rms current
I_{ave}	average switch current
I_{dc}	dc current
$I_{dc,ref}$	dc current reference
$I_{d,ref}$	d-axis current reference
$I_{q,ref}$	q-axis current reference
$i_{c,a}(t)$	filter capacitor current, phase *a*
$i_{rec,a}(t)$	rectifier input current, phase *a*
$i_{rec,h}(t)$	hth harmonic component of the rectifier input current
$i_{l,h}(t)$	hth harmonic component of the line current

Voltages:

V	peak ac voltage
V_{rms}	rms value of the voltage
V_{peak}	peak reverse switch voltage
V_{dc}	dc voltage
$V_{dc,ref}$	dc current reference
V_{phase}	phase voltage
$v_{rec}(t)$	rectifier input terminal voltage

$v_{c,a}(t)$ filter capacitor voltage, phase a

Switch and Switch Related Parameters:

S_i switch i

S_{bi} bi-level switching function

S_{tri} basic tri-level switching function

S_{sh} short circuit switching function

$Gate_i$ gating signals for switch i

SW_l line-to-line switching function

SW_p phase switching function

Power Circuit Components:

L, C filter components on the ac side

L_{dc}, C_{dc} filter components on the dc side

R_s line resistance

R_f filter resistance

r_o motor equivalent resistance

L_o motor equivalent inductance

Z_L line impedance

Z_C capacitor branch impedance

Control Circuit:

K_i, K_v current and voltage sensor gains

K_p, τ proportional gain and time constant of the PI regulator

K_{pdi}, K_{ii}, K_{di} proportional, integral and derivative gain of the PID regulator

General:

M	modulation index
M_{max}	maximum modulation index
M_{min}	minimum modulation index
θ	input displacement angle
ω	fundamental angular frequency
ω_b	filter break frequency in rad/s
δ	power angle
ξ	damping factor
η	efficiency
σ	control (phase shift) angle
α	filter attenuation factor
f_m	carrier frequency
f_{sw}	switching frequency
f_b	filter break frequency

CHAPTER 1

INTRODUCTION

1.1 AC-DC Conversion

Environmental and safety issues related to energy consumption led to a basic question for our society. How can we improve our standard of living without endangering our environment? The answer lies in generating electrical energy by cleaner and more efficient power plants and consuming the generated power more efficiently. One possible solution is energy conservation by wide spread use of Power Electronics. It has been estimated that in the USA roughly 15%-20% of energy can be saved by more efficient use of electricity with the help of Power Electronics. Approximately 60% to 65% of the generated energy is consumed in electrical motors. This has made the motor drive systems a major target for numerous energy-saving schemes. It is well established that Adjustable Speed Drives (ASDs) can save a considerable amount of energy by adding flexibility to the processes. Therefore, more and more customers are using these systems. This means that more electrical devices are connected

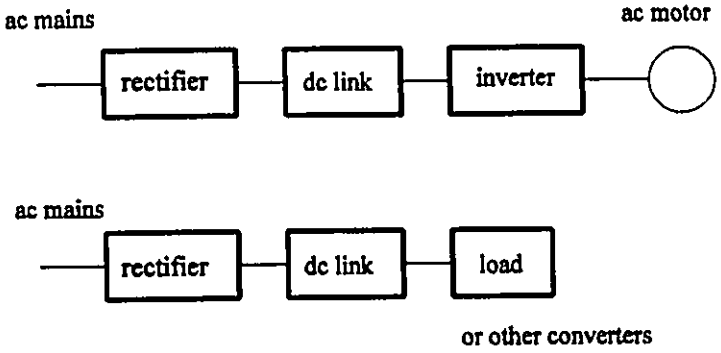

Fig. 1.1 Typical connection of static converters to ac mains.

to the ac system. Fig. 1.1 shows a typical configuration. There are also other applications which need interfacing with ac mains. These include indirect frequency changers, dc power supplies, battery chargers and HVDC transmission systems, Fig. 1.1. Interfacing with the ac system is usually achieved through an ac/dc conversion stage, or rectifier. As the number of applications of adjustable speed drives increase and static power converters proliferate, there is a need to understand and quantify their impact on the power system. Interactions between the power system and the converter and conversely the effect of power system disturbances on the converter performance have therefore become a major issue in the widespread use of Power Electronic conversion.

A. Generation of Harmonics

The switching action of converters causes a current to be drawn from the system which is far from the ideal sine wave shape. The distorted current flowing through the supply system

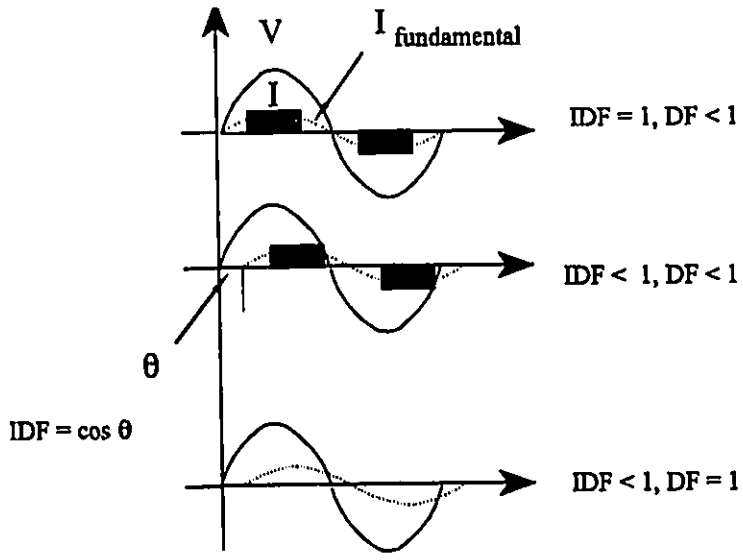

Fig. 1.2 Representation of Input Displacement Factor, IDF and Distortion Factor,DF.

impedances will produce distorted voltages at various points of coupling with other loads in the system. These voltage distortions can interfere with the acceptable operation of loads and other converters, resulting in serious problems such as resonance overvoltage, harmonic instabilities, reduced efficiency and interference with communication circuits. It is possible to express distorted current in terms of the fundamental sinusoidal wave plus a number of other sinusoidal waves of higher frequencies (Fourier series). These sinusoidal components of the periodic waveform with integer multiple of the fundamental frequency are defined as harmonics. Measures must be taken to reduce/eliminate harmonics wherever possible. The role of utility engineers and converter designers is to study the effect of harmonics and: 1) determine the possibility of harmonic resonance occurring and 2) calculate the magnitudes and orders of harmonic voltages and currents under various load conditions. Since it is not economical nor desirable to eliminate the harmonic currents from individual converters, analysis and guidelines are necessary to determine whether or not there will be a problem created by the harmonics injection into the power system. Such useful guidelines and recommendations are provided in standards such as IEEE-519 and IEC-555 to aid in the application of converters and to ensure the high power quality to which North America has become accustomed.

B. The Input Power Factor

The power factor of converter is made up of two components: Input Displacement Factor (IDF) and Distortion Factor (DF), Fig. 1.2. The PF can be given by:

$$PF = IDF \times DF \tag{1.1}$$

The effect of the two are combined to obtain the total Power Factor (PF). The displacement

component is the ratio of the active power (in W), to the apparent power (in VA), considering only the fundamental waveform. This is the power factor seen by the utility metering devices (kW. hs and var. hs). The distortion component is the component associated with harmonic voltages and currents. Displacement power factor is the power factor that is measured by metering equipment, and is the one on which utility penalties are based (utilities expect loads to have a 0.9 PF or better). Therefore, it is necessary to reduce the phase displacement between the fundamental waveforms of current and voltage, in order to reduce the cost of operation.

In order to comply with harmonics limits, and to minimize the amount of kVA drawn from the system, the front-end rectifier must draw near sinusoidal currents at high power factor. Furthermore, the converter must achieve high operating efficiency with low cost, in order to be competitive on the market. In other words, the challenge is to provide a high quality conversion scheme which delivers high quality (low ripple) output waveforms without distorting the ac mains and without drawing any reactive power [1]-[5]. A brief review of the

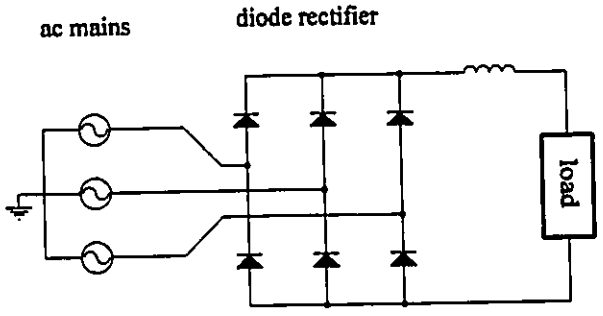

Fig. 1.3 Three-phase diode bridge rectifier.

existing front-end rectifier topologies is given in the following.

1.2 Front-End Rectifier Topologies

1.2.1 Diode Bridge Rectifier

A three phase bridge converter for ac/dc conversion is shown in Fig. 1.3. The conversion of power is accomplished by periodic switching in the conducting legs of the converter. The "switches" in the case of Fig. 1.3 are diodes. The ac source is connected to the load by combinations of one top and one bottom switch. The resulting output voltage is made up of the crests of the sinusoidal waveforms (60°). For the sake of simplicity the dc current is considered to be constant. Therefore, the line currents will consist of square waveforms of 120° width. Thus, harmonic current will flow in the supply lines. Fourier analysis confirms that each 6th harmonic in the dc voltage, results in $6n \pm 1$ harmonic currents in the ac line. The magnitudes of these harmonic currents are inversely proportional to the harmonic order. Therefore, the diode rectifier injects large current harmonics in the mains, while maintaining

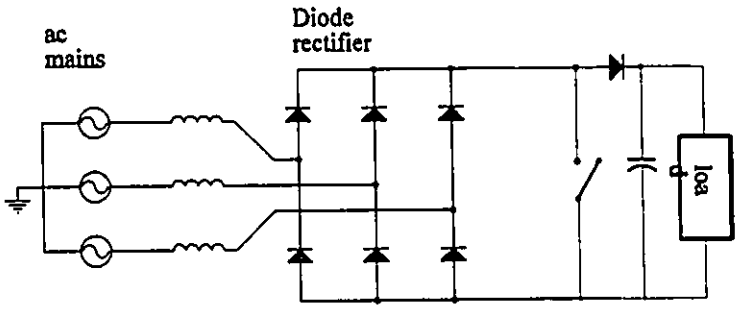

Fig. 1.4 Diode rectifier with input current waveshaping.

a high Input Displacement Factor (IDF = 1). A. R. Parasad *et al* in [6] proposed a simple method of improving the input power factor of a three phase diode rectifier by waveshaping the input line currents with the help of an additional switch, Fig. 1.4. However, the design of the input filter for this scheme is difficult and the input current must be discontinuous.

1.2.2 Phase Controlled Rectifier

The diodes in Fig. 1.3 will start conducting as soon as a voltage is applied in the forward, or current carrying direction. As a result, the output voltage of the converter is uncontrolled. If these diodes are replaced by thyristors, Fig. 1.5, the output voltage can be controlled by delaying the firing angle (the instant at which the thyristors are turned on). Firing angle also influences the magnitude of the current harmonics, [3,4]. This topology is attractive due to its inherent ruggedness, high efficiency and simple control circuitry. However, it has the well-documented drawbacks of:

- poor input power factor,

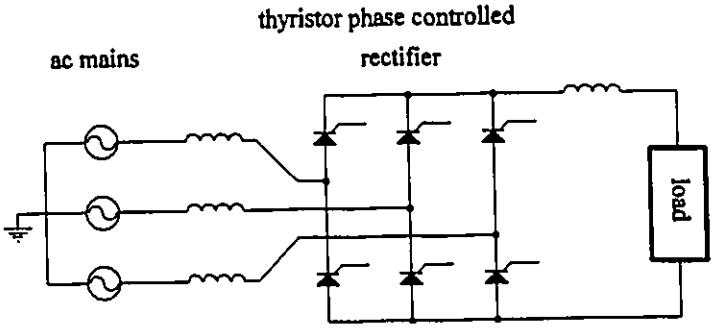

Fig. 1.5 Line-commutated phase-controlled rectifier.

- large low order harmonics in the input line currents.

The former property is due to the phase displacement required for output power control and is an inherent characteristic of phase-controlled rectifiers. With the growing use of phase control, utility systems are facing serious power quality problems. As it was mentioned before, recently proposed standards tend to severely restrict harmonic injection into power line. Bulky and expensive filters have been used to suppress the injected harmonics. However, the cost and complexity of such compensating schemes, will tend to reduce phase-controlled converters applications in the future [3,4,5].

1.2.3 PWM Front-End Rectifiers

Recent advances in power semi-conductor technology have produced high voltage/high current fast gate turn-off switching devices (such as GTOs and IGBTs.) Consequently, the thyristor switches in converter are being replaced by these devices, making it feasible to apply Pulse Width Modulation (PWM) techniques to converters. By using PWM switching patterns, the frequency spectra of the input waveforms can be shaped and harmonic components moved to a higher frequency. Operation of the converters with PWM switching patterns offers features such as sinusoidal input current at unity displacement power factor and a high quality dc output voltage. This results in reduced input current harmonics and ac voltage distortion of the ac mains [5,7]. These features consequently lead to a smaller size of the input/output filter and reduced losses in the input transformer. Successful application of PWM techniques to forced commutated converters has prompted recent investigations in finding more suitable topologies for ac to dc conversion. Two structures have evolved:

- The current-source topology, Fig. 1.6 or PWM Buck Rectifier;

- The voltage-source topology, Fig. 1.8, (PWM Synchronous or Boost Rectifier).

1.2.3.1 Current Source Topology (PWM Buck Rectifier)

The high power and high quality current-source PWM rectifier of Fig. 1.6 has a good potential for applications in high power ac drives and frequency changers. The PWM

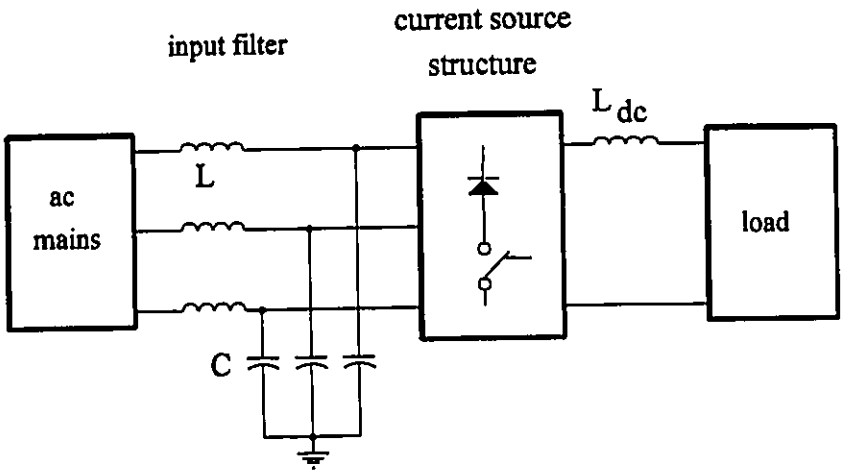

Fig. 1.6 Current-source topology, PWM Buck Rectifier.

rectifier shown in Fig. 1.6, establishes a dc current link by means of unidirectional (regarding current)/ bidirectional (regarding voltage) switches. This structure has good reliability and ruggedness. Due to the time-discontinuous operation (switching), energy storage elements must be provided on the dc/ac side in order to make the exchange of power (during switching) possible. As can be seen from Fig. 1.6, since the ac source is not ideal, an LC filter is needed at the ac terminal of the PWM rectifier. The input capacitors also suppress the voltage spikes across the switches. This makes the PWM rectifier prone to resonance problems. Therefore, proper damping must be provided in the filter circuit either by inserting additional resistive

elements or by using control methods. The other difficulty of current source rectifier is the generation of proper switch gating signals. A path for the output dc current must exist at all times which requires short-circuiting pulses when no current is drawn from the ac supply. These must be added to the tri-level gating signals [8]. The control schemes used to operate the PWM Buck rectifier can be divided into open loop and closed loop techniques.

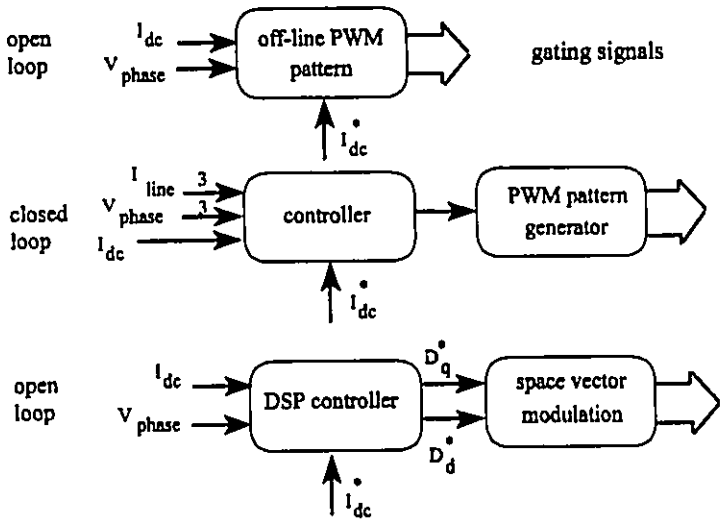

Fig. 1.7 Control schemes for current source PWM Rectifier.

A. Open Loop Control Schemes

A number of publications have investigated the performance and characteristics of the current source type PWM rectifier operating with off-line PWM patterns [9]-[14]. The control of the output current is obtained by varying the modulation index and/or phase shifting of the pattern. Ideal input/output characteristics such as ripple-free dc link current and sinusoidal input voltages are assumed. These publications mostly deal with the PWM patterns. Pattern generation can be divided into two main categories:(a) carrier based techniques and (b)

programmed PWM techniques. These techniques can be adapted to optimize/minimize certain performance factors/errors. As a general conclusion, the programmed techniques are more suitable for high power applications where the switching frequency is limited. As it was mentioned earlier and in general, using carrier-based techniques for a current source rectifier requires an additional stage to meet the current source pattern requirements. However, use of techniques such as Trapezoidal PWM is straight-forward. Combination of carrier-based and programmed techniques is also suggested [15]. In this scheme the Trapezoidal PWM is used for the low output frequency range and the Selective Harmonic Elimination (SHE) is adopted for the higher frequency range. Reviews of most commonly used carrier-based and programmed techniques are given in [16],[17] respectively.

Different PWM patterns are developed in [18] and the effect of the switching patterns on the harmonics generated and on the size of the input/output filter is studied. Various performance factors are defined and used to evaluate the proposed PWM patterns. Also, an algorithm is presented to achieve optimum design of input/output filters [19]. However, the problem of damping is not considered and the Input displacement Factor of the rectifier is not studied.

The single phase Buck rectifier is studied in [20]. The basis of duality is laid out and a structure which is the dual of the voltage source topology is proposed and investigated [21]. The rectifier is operated with delta modulation control of the input capacitor voltage and the operating limits are determined. A more in depth study of both current source and voltage source topologies and PWM patterns is presented in [22]. The duality of the two structure is studied and similarities are clarified. The above publications are more concerned with the

operation of the current source topology and the method of pattern generation. However, recently and concurrently with the work presented in this thesis, some researchers have focused on the correction of Input Displacement Factor, IDF.

Hiti *et al* [23] proposed a three-phase PWM rectifier with compensation of the IDF. A control low is derived to obtain unity power factor and DSP implementation of the controller in *dqo* frame is presented. The pattern generator is based on Space Vector Modulation (SVM) (Fig. 1.7) which is described in detail in [24],[25]. The Space Vector Modulation technique offers the advantage of optimized switching instants and therefore reduces switching losses.

B. Closed Loop Control Schemes

In all of the studies mentioned above, the PWM Rectifier is controlled in an open loop fashion with modulation index or phase shift control. Since in most cases, the PWM pattern is stored in an EPROM, the modulation index control is discontinuous and speed of response is slow [26,27]. Moreover, sufficient damping must be provided in the power circuitry to avoid oscillations of the input line currents. Recently, attempts have been made to adapt closed loop control techniques for PWM rectifiers. Wang, *et al* developed an on-line PWM pattern generator with Digital Signal Processor (DSP) implementation for current source topologies. The pattern generator is used in [28] to control a PWM Buck Rectifier and obtain unity power factor operation independently of the rectifier operating point. The control circuitry proposed in [28] is complex and requires DSP implementation.

Another control scheme is proposed by Sato *et al* in [29] in which the state variables of the rectifier and the input filter are controlled in closed loop fashion to obtain sinusoidal steady state ac waveforms and to reduce the transient oscillation of the ac side current. The

proposed circuit however is very complicated and needs extensive use of hardware. The main stream of control techniques applied to current source PWM rectifiers are depicted in Fig. 1.7. Small signal analysis of current source rectifiers is presented in [30],[31].

Application of current-source rectifiers in ac drives is investigated in [32]-[35]. In these schemes, the dc link current regulation is normally obtained by phase control of the input thyristor rectifier. Increase in speed of response and effective damping the oscillations resulting from the presence of the filter capacitors is still a challenge to designers [32].

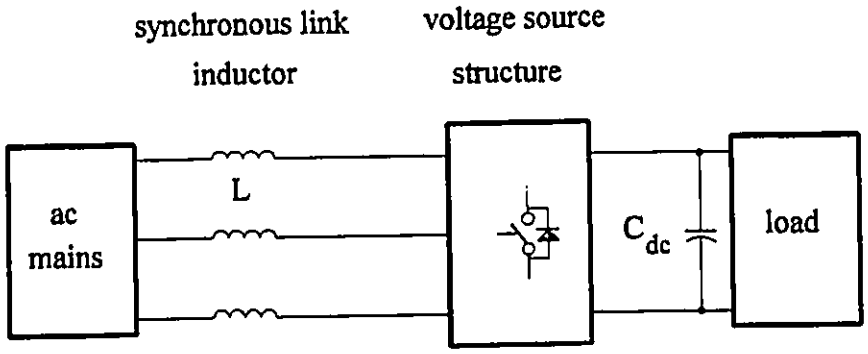

Fig. 1.8 Voltage-source topology, synchronous link rectifier.

1.2.3.2 Voltage Source Topology (Synchronous Rectifier)

The voltage-source topology finds application in dc voltage link ac drives and self-controlled dc bus var compensators. This topology, interfaces the ac and dc systems by means of bidirectional (current)/ unidirectional (voltage blocking) switches, Fig. 1.8. The structure consists of an inductor on the ac side and a capacitor on the dc side. The gating signals of the

top and bottom switches of the same leg are complementary, hence easy to produce from the PWM pattern. This feature has contributed to the popularity of this structure and as a result, many control strategies have been developed. The literature on the subject is briefly described below, Fig. 1.9.

A current-controlled Synchronous Rectifier was proposed by Ooi *et al* [36]. The three line currents are controlled to obtain sinusoidal currents with unity power factor. The reference current template can be either generated from phase voltages or be stored in an EPROM and synchronized with the ac mains. The amplitudes of the reference currents are varied according the dc load voltage demand. The rectifier is operated with a hysteresis technique which has the drawback of variable switching frequency. Reports of transient test on the proposed converter and application as an ac drive system are presented in [37],[38] respectively. Further investigations on performance and control of synchronous link converters can be found in [39],[40]. The current sensors were eliminated in the indirect current control of synchronous

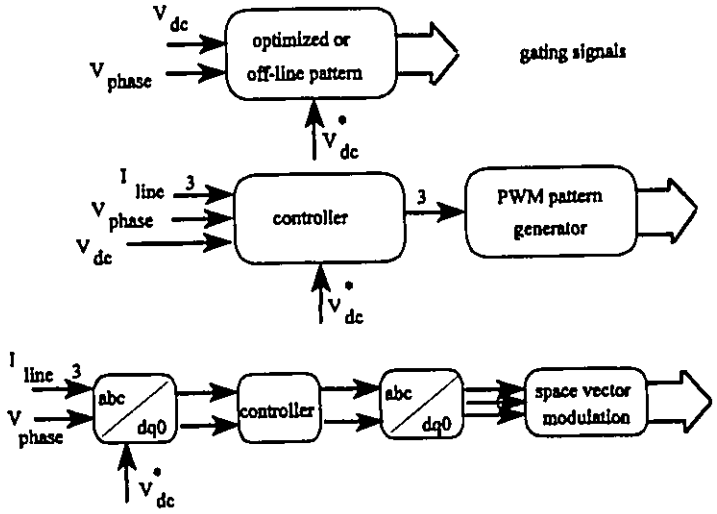

Fig. 1.9 Control schemes for Synchronous Rectifier.

link rectifier proposed in [41]. However, the region of stability with this control method is very limited. The stability limitation was improved by implementing a more complex control scheme [42].

In [43], a Synchronous (Boost) Rectifier with a predictive current control with fixed switching frequency is proposed. The idea is to correct the error between the reference and the actual current within one switching period. Based on this criterion, the gating signals of the six switches are generated. The calculation of the duty cycle of the switches is dependent of the circuit parameters, making the method sensitive to parameter variation. Analysis of Synchronous Rectifier is presented in [44],[45], but operating region limitations are not brought out. The operation of a Synchronous Rectifier as a var compensator is investigated in [46].

Phase angle control of voltage- source PWM rectifier is presented in [47],[48]. The real and reactive power of the rectifier are controlled based on the derived equations. This means controlling the power angle in a closed loop fashion. The controller can be realized in either stationary (abc) or rotating (dqo) frames. The method is suitable for low switching frequency high power applications, and the speed of response is very slow. The converter may exhibit some oscillatory response under transient conditions. Recently, multi-level voltage source PWM rectifiers with closed loop control are been considered for high power applications [49],[50].

Due to simplicity of derivation of switch gating signals for voltage-source rectifier, many control techniques have been developed and implemented [51],[52]. For DSP implementation, a promising technique in pattern generation is the Space Vector Modulation.

This technique is becoming more and more popular due to the advances in computer technology and price reduction/speed improvement of microprocessors [53-55]. The existing ac/dc conversion schemes with their typical control options are depicted in Fig. 1.10.

1.3 Scope and Contributions of the Thesis

In view of the above, this thesis focuses on developing techniques to meet specific performance requirements and to satisfy special applications for PWM ac/dc converters. In particular, improving system performance regarding the Input Displacement Factor is emphasized. By studying similarities and the duality of current-source and voltage-source type

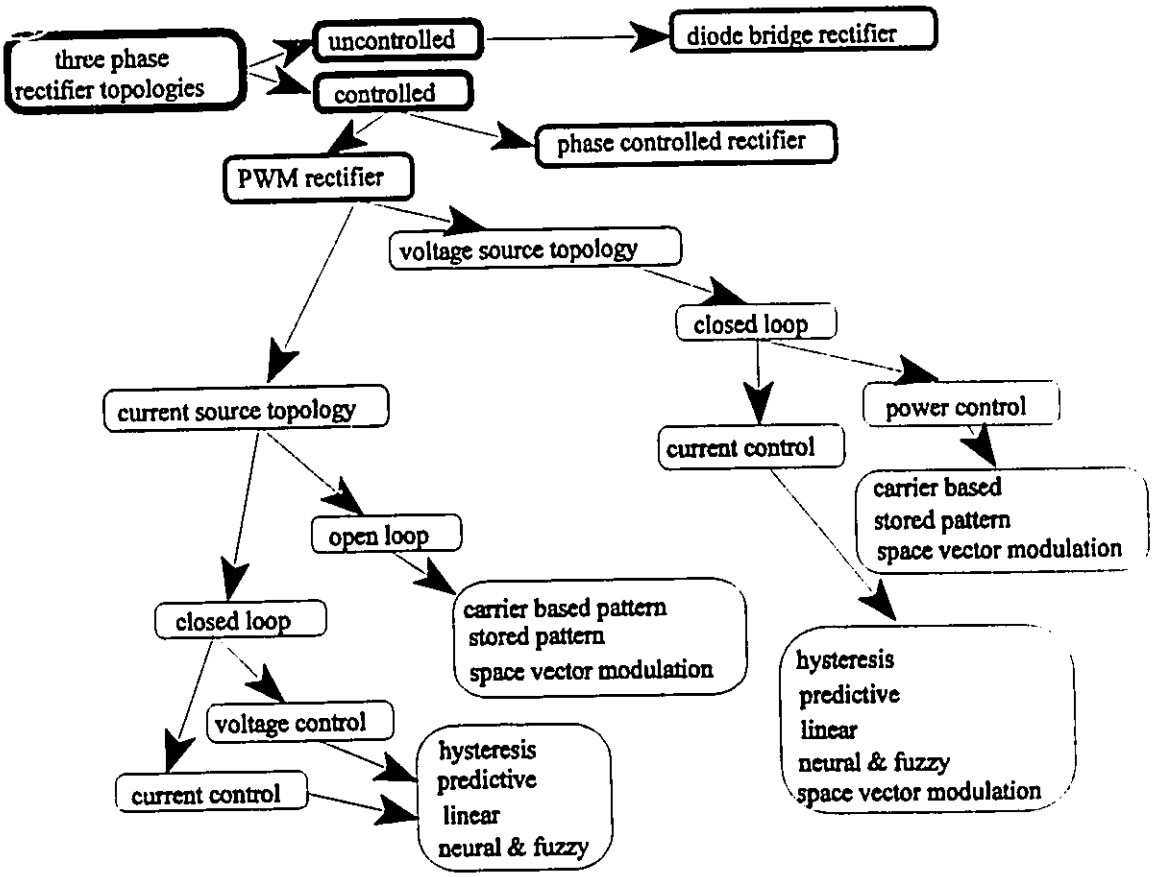

Fig. 1.10 Existing rectifier topologies.

topologies, it is possible to transfer the insights and experiences of one topology to the other. In particular, closed loop techniques developed for voltage source topology can be adopted for current-source type. Therefore, wherever applicable, new methods of control and/or novel topologies are proposed in the thesis, practical problems are addressed and viable solutions are proposed. The particular contributions of this thesis are:

A. Current Source Topology

- A feed-forward scheme is proposed to achieve unity power factor through compensation of the Input Displacement Factor. The proposed scheme is very simple and does not need any added transducers.
- A user friendly approach to design of input filter for PWM rectifiers is proposed. Different design objectives are defined and compared and the effects of filter components on the Input Displacement Factor (IDF) are studied.
- The effects of circuit components and control techniques on damping in PWM rectifiers are investigated. A new control scheme is proposed which needs no damping resistors in the input filter circuit and results in a better system performance during transient conditions and a higher efficiency.
- Closed loop control of PWM rectifiers is studied. In particular, a current-controlled PWM rectifier is proposed, analyzed and designed. Load independent unity power factor operation is achieved. Different types of controllers are investigated. These include Proportional-Integral (PI), Proportional-Integral-Derivative(PID) and Neural Networks (NN) based controllers.

B. Voltage Source Topology

- A unity power factor input stage with minimum hardware requirements is proposed for ac drive applications.
- A current-controlled voltage regulated dc power supply based on voltage source topology is proposed. The design and performance of the controller in both stationary and rotating frames are investigated and compared. Design procedure is given and transient response is studied using rotating frame transformation.

1.4 Thesis Outline

The thesis is divided into 9 chapters. A brief outline of each chapter is as follows:

In ***Chapter 2***, the steady state characteristics of three-phase PWM rectifier topologies are investigated. The study includes: principles of operation, graph and switch realization comparison, converter and switch ratings, operating regions, filtering requirements, power factor considerations and control aspects. The theoretical considerations are verified by simulation and experimental results on laboratory prototypes [56].

Practical problems of input filter design for PWM rectifiers are discussed in ***Chapter 3*** and a simple systematic procedure for design of the input filter is proposed [57]. The chapter includes study of power factor, kVA ratings, system efficiency and effect of parameter variations. Two design examples are provided and the corresponding characteristics are compared.

Chapter 4 proposes a compensation scheme to achieve unity Input Displacement Factor independently of the rectifier operating point. The modulating signals are phase shifted according to the rectifier operating point to always result in unity IDF. The control circuit is

very simple and does not require any additional transducer. It uses a feed-forward dc current loop and the standard dc voltage/current regulation loop to regulate the amplitude and phase of the modulating signals. Parameter sensitivity, effect of variations of input voltages and the limitations of the proposed scheme are studied [58].

In ***Chapter 5*** a current source type PWM rectifier with on-line pattern generation and inherent synchronization with the ac mains is proposed. This results in a very fast starting and a much improved transient response. Also, the need for the damping resistors is eliminated due to the effective damping provided through the modulating of the capacitor voltages. The control scheme proposed in this chapter results in a system with higher efficiency due to the elimination of the damping resistors. The proposed scheme is investigated for ac drive applications under various transient and fault conditions. Also, a topology for non-regenerative applications is proposed that requires only three base drives. Experimental results verify the feasibility of the proposed non-regenerative topology and the pattern generation method used [59],[60].

Chapter 6 proposes closed loop control of PWM rectifiers. The three input line currents are controlled to obtain low harmonic currents with unity IDF. The proposed current controlled PWM rectifier exhibits excellent steady state operation and good transient dynamics, a result of the current control method used. Output dc voltage regulation is achieved by varying the amplitudes of the current references. Analysis and design guidelines are provided and the key predicted results are experimentally verified on laboratory prototypes [61]. Different types of controllers are implemented. These include: Proportional Integral (PI), Proportional Integral Derivative (PID) and a Neural Networks (NN) based controller. The performances of the three

controllers are compared [62],[63].

Chapter 7 presents an application of a PWM Synchronous Rectifier as the input stage of an ac drive system, this results in improved performance with a simple control scheme. To allow the output inverter to operate in the PWM mode at rated speed, a Synchronous Rectifier is proposed to slightly boost the dc bus voltage. The output inverter is current-controlled, therefore, the dc bus requirements are not stringent. This allows for a simpler control strategy to be used to operate the input rectifier, the main purpose being to ensure unity power factor operation. Experiments on a laboratory prototype are used to verify the simulation and theoretical results.

Chapter 8 proposes a current controlled PWM Synchronous Rectifier. It provides near sinusoidal input currents with unity power factor and a low output voltage ripple. Moreover, it produces a well-defined input current harmonic spectrum, exhibits fast transient response to load voltage variations and is capable of regenerative operation. PWM pattern generation is based on a carrier technique and the current controller is implemented in the (a) stationary (abc) frame and (b) rotating (dqo) frame. The design and performance of the two controller options are investigated and compared.

CHAPTER 2

PERFORMANCE COMPARISON OF PWM BUCK AND SYNCHRONOUS RECTIFIERS

2.1 Introduction

PWM converters have been shown to offer a better alternative to thyristor phase-controlled rectifiers with respect to power factor and input current/cutput voltage harmonics. This chapter presents a systematic comparison of the two existing topologies (current source, voltage source) from point of view of graph structure and switch realization, converter and switch kVA ratings, PWM patterns, input/output filtering requirements, power factor, operating regions and control aspects. Experimental results obtained on laboratory prototypes are used to validate the theoretical considerations.

2.2 Principles of Operation

2.2.1 Current Source Topology

The PWM rectifier shown in Fig. 2.1 has current-source characteristics at the dc terminal (dc side inductor, L_{dc}) and voltage-source characteristics at the ac terminal (either an ideal voltage source or ac side capacitor). The ac and dc sides are interfaced by operating the six unidirectional (current)/bidirectional (voltage) switches. These switches must be operated so as to avoid an open circuit on the dc link or a short circuit on the ac side. The following criterion is used to generate typical PWM patterns:

- The line currents must be well defined. This means that only two switches are conducting at any instant, one from the top row and one from the bottom row.

The top and bottom row switches in a current source topology can be best represented by two

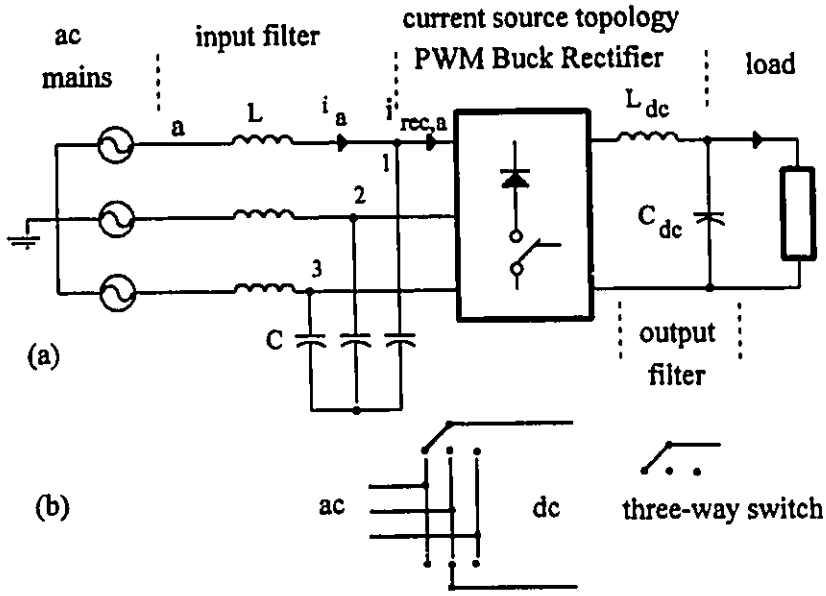

Fig. 2.1 (a) Current-source topology, PWM rectifier, (b) representation by two "three-way" switches.

Table 2.1 Switch combinations for current source and voltage source topologies.

	current source topology						voltage source topology					
state	S_1	S_2	S_3	S_4	S_5	S_6	S_1	S_2	S_3	S_4	S_5	S_6
0	1	0	0	1	0	0						
	0	0	1	0	0	1	1	0	1	0	1	0
	0	1	0	0	1	0	0	1	0	1	0	1
1	1	1	0	0	0	0	1	1	0	0	0	1
2	0	1	1	0	0	0	1	1	1	0	0	0
3	0	0	1	1	0	0	0	1	1	1	0	0
4	0	0	0	1	1	0	0	0	1	1	1	0
5	0	0	0	0	1	1	0	0	0	1	1	1
6	1	0	0	0	0	1	1	0	0	0	1	1

$S_i = 0$ means the i-th switch is open.
$S_i = 1$ means the i-th switch is closed.

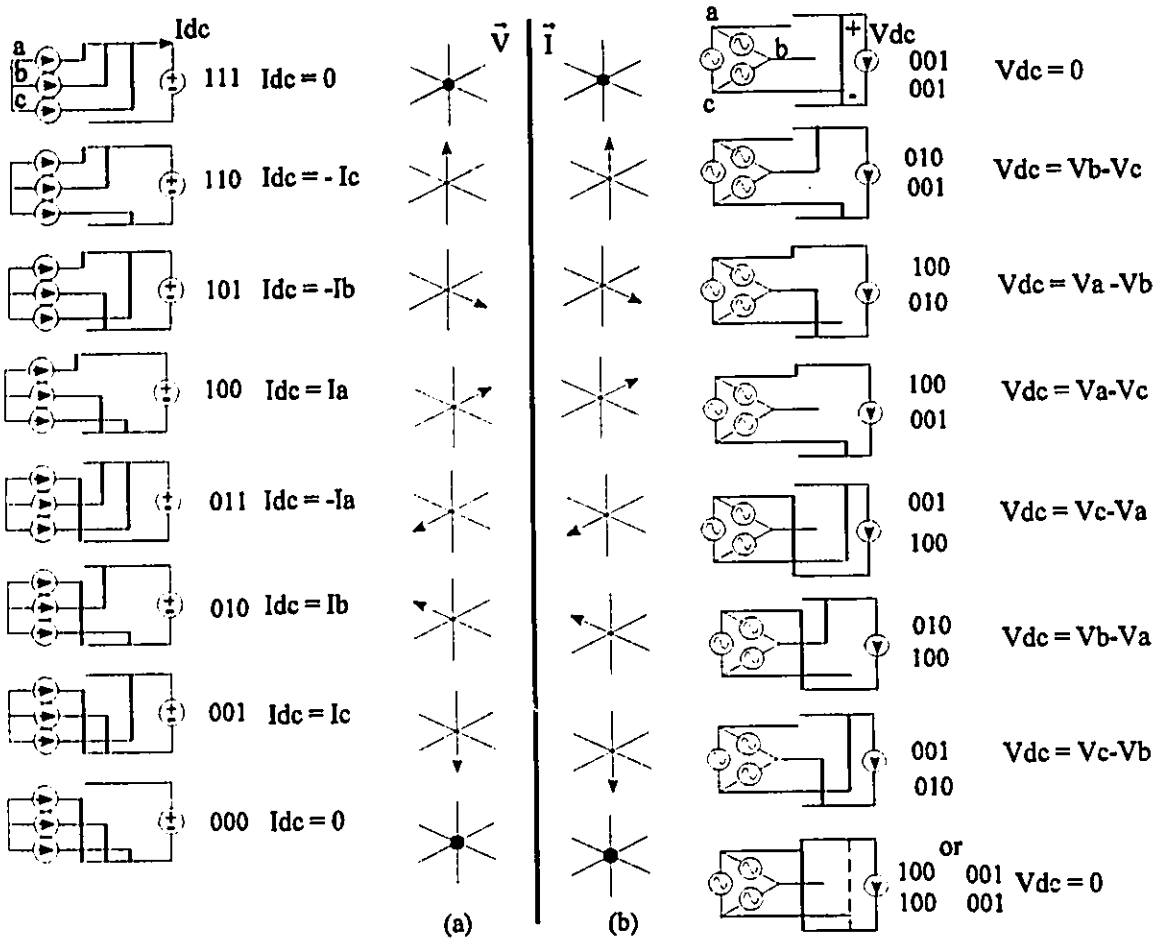

Fig. 2.2 Possible switch combinations, (a) voltage source topology, (b) current source topology.

"three-way" switches, Fig. 2.1.b. Therefore, the number of possible switch combinations can be calculated as:

$$number\ of\ combinations = (number\ of\ ways)^{(number\ of\ switches)} = 3^2 = 9 \qquad (2.1)$$

These nine combinations result in only seven different states since three of these combinations are the zero states during which the ac side is insulated from the dc side and the dc link current is circulating

through one of the bridge legs. An ideal current source PWM rectifier with all possible switch combinations are depicted in Fig. 2.2.b and the switch combinations are tabulated in Table 2.1, where $S_i = 0$ means that the i-th switch is open and $S_i = 1$ means that it is closed. In Fig. 2.2.b the ac side consists of three voltage sources connected in delta and the dc side is a current source. Thick lines show a connection through the corresponding switch either, to the top or the bottom dc bus.

Any three functions of time that satisfy $g_a(t) + g_b(t) + g_c(t) = 0$, can be represented by a vector $\vec{G}$ in a two-dimensional space by using the following transformation:

$$\vec{G} = \frac{2}{3}\left(g_a(t) + g_b(t)e^{j\frac{2\pi}{3}} + g_c(t)e^{-j\frac{2\pi}{3}}\right) \tag{2.2}$$

Therefore, the states shown in Table 2.1 can be transformed to vectors in two-dimensional space. For example, for state 1, we have:

$$\begin{Bmatrix} i_a(t) = I_{dc} \\ i_b(t) = 0 \\ i_c(t) = -I_{dc} \end{Bmatrix} \tag{2.3}$$

and this will obtain the following vector as depicted in Fig. 2.2.b:

$$\vec{I}_1 = \frac{2}{3}\left(I_{dc} + 0 - I_{dc}e^{-j\frac{2\pi}{3}}\right) = \frac{2}{\sqrt{3}} I_{dc} e^{j\frac{\pi}{6}} \tag{2.4}$$

where I_{dc} is the amplitude of the dc link current. The transformation of these six states forms a hexagon. Each vector presents the location of the line current vector in the new space. The zero state is located at the centre of this hexagon, representing zero line currents, Fig. 2.2.b.

The input/output equivalent circuits of the PWM rectifier are shown in Fig. 2.4(a,b). Here output dc current and input rectifier voltage are the independent variables and output dc voltage and rectifier input currents are the dependent variables. Therefore, the input/output current/voltage relationships are given by:

$$v_{dc}(t) = SW_{l,a}(t)v_{rec,a}(t) + SW_{l,b}(t)v_{rec,b}(t) + SW_{l,c}(t)v_{rec,c}(t) \tag{2.5}$$

$$i_{rec,j}(t) = SW_{l,j}(t)\, i_{dc}(t) \qquad for \quad j \in \{a,b,c\} \tag{2.6}$$

where: $v_{dc}(t)$ = rectifier output dc voltage, $SW_{l,j}(t)$ = line-to line switching function, $v_{rec,j}(t)$ = input rectifier voltages, $i_{dc}(t)$ = rectifier output dc current, $i_{rec,j}(t)$ = rectifier input currents. From (2.5), the dc output voltage can be obtained as:

$$V_{dc} = \frac{3}{2}\|SW_l\| V_{rec} M \tag{2.7}$$

$$where \quad M_{max} = \frac{2}{\sqrt{3}} \quad and \quad \|SW_l\|_{max} = \frac{\sqrt{3}}{2} \tag{2.8}$$

where $\|SW_l\|$ is the magnitude of the line to line switching function, M is the modulation index, and V_{rec} is the peak value of the rectifier input phase voltage. The maximum voltage that can be obtained by a current source topology is:

$$V_{dc,max} = \frac{\sqrt{3}}{2}\sqrt{6}\, V_{rec,rms} = 2.12\, V_{rec,rms} \tag{2.9}$$

where $V_{rec,rms}$ is the rms value of the rectifier input phase voltage.

As it can be seen from (2.7), the output dc voltage is proportional to the modulation index M. Therefore, the converter behaves as a buck configuration as far as the dc output voltage is concerned. The similarity between current-source PWM rectifier and dc/dc Buck converter can also be realized by comparing the "switch-diode-inductor" arrangement. A single phase Buck converter and a current source PWM rectifier (for one possible state of the switches) are depicted in Fig. 2.3. It is assumed that phase c is the most negative phase, hence switch 2 is always conducting. It is seen

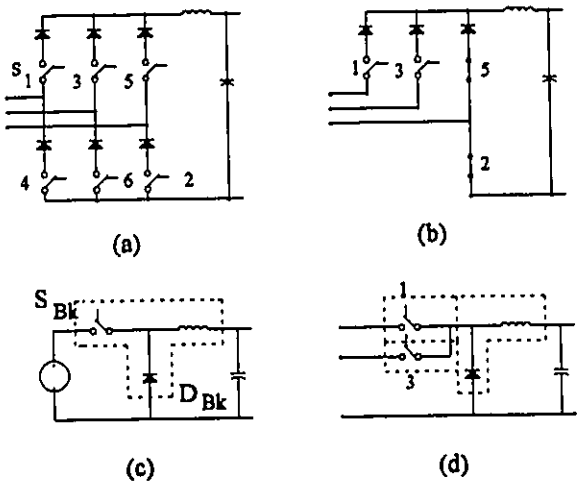

Fig. 2.3 (a) Current source topology, (b) arbitrary state of switches, (c) dc/dc Buck converter, (d) the same switch state as in (b).

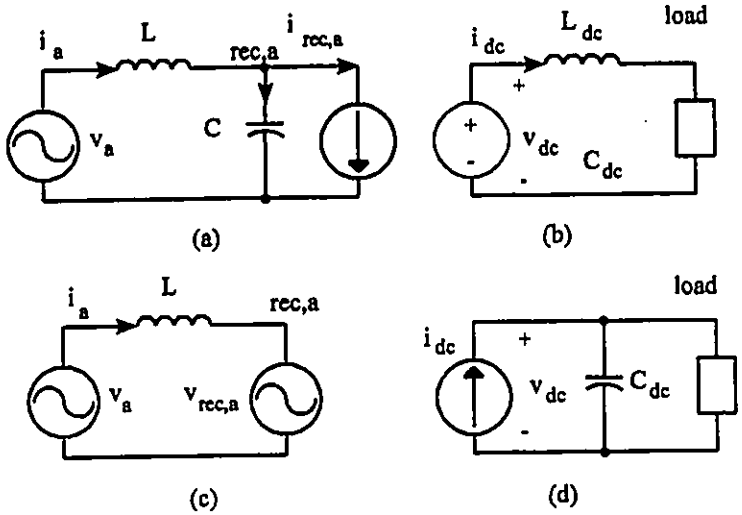

Fig. 2.4 Current source topology, (a) input (b) output equivalent circuit. Voltage source topology, (c) input (d) output equivalent circuit.

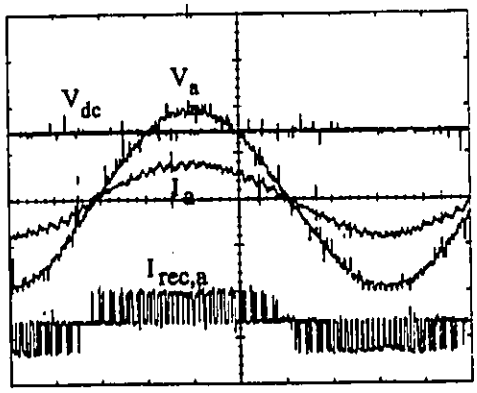

Fig. 2.5 Experimental results, PWM Buck Rectifier.

that when S_2 is closed, a buck configuration is obtained with either S_1 or S_3 acting as the Buck switch, S_{Bk}. The role of S_5 is similar to that of the Buck diode, D_{Bk} in the buck topology. The switch-diode combination shown in Fig. 2.1 can be realized by using a single GTO switch with reverse blocking

capability, although for high voltage ratings a series connection of these switches might be needed. The use of the input filter of the PWM rectifier in Fig. 2.1 is not essential to operation of the converter. However, the filter capacitor also acts as a snubber to suppress the voltage spikes across the switches. The input /output waveforms of the PWM rectifier are depicted in Fig. 2.5. The input rectifier current has the same shape as the line-to-line switching pattern. The input filter is designed to meet the desired specifications in terms of Total Harmonic Distortion (THD) for the line current THD_i and the rectifier input voltage THD_v. The resonant frequency of the filter circuit must be away from the converter switching frequency harmonics. The design of the input filter will be discussed in *Chapter 3*.

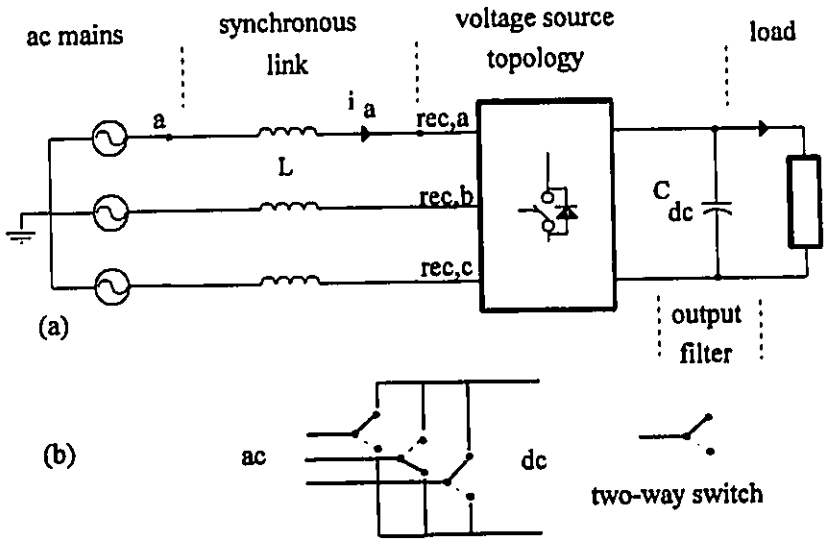

Fig. 2.6 (a) Voltage-source topology, Synchronous Rectifier, (b) representation by three "two-way" switches.

2.2.2 Voltage Source Topology

The voltage-source topology shown in Fig. 2.6 has voltage -source characteristics at the dc terminal (dc side capacitor) and the ac terminal exhibits current source characteristics (ac side inductor, synchronous link). The ac and dc sides are interfaced by six bidirectional (current)/unidirectional (voltage) switches. The switching action must avoid short circuit on the dc side or open circuit of the ac side. The following criterion holds:

-The three midpoints of the bridge must have a defined voltage. This means they must be either connected to the bottom or top bus on the dc side, in other words the gating patterns of the top and bottom switch of the same leg are complementary. Therefore, the switching action in a voltage source topology can be represented by three "two-way" switches. The number of possible combinations are obtained from:

$$number\ \ of\ combinations\ \ = (number\ \ of\ ways)^{(number\ of\ switches)} = 2^3 = 8 \qquad (2.10)$$

These eight combinations result in six non-zero states and two zero states during which the three switches are all connected to the top or bottom dc bus and the dc and ac sides are isolated from each other. These states are similar to those obtained for the current source rectifier and form a similar hexagon. The ideal voltage source topology for different switch combinations and the hexagon of voltage states are shown in Fig. 2.2.a. The ac side is a set of three star connected current sources, and the dc side is modelled by a dc voltage source. For each switch combination, a dual state for the voltage source topology exists. This means that PWM patterns applied to the voltage source type can be adapted to obtain the dual pattern for the current source topology.

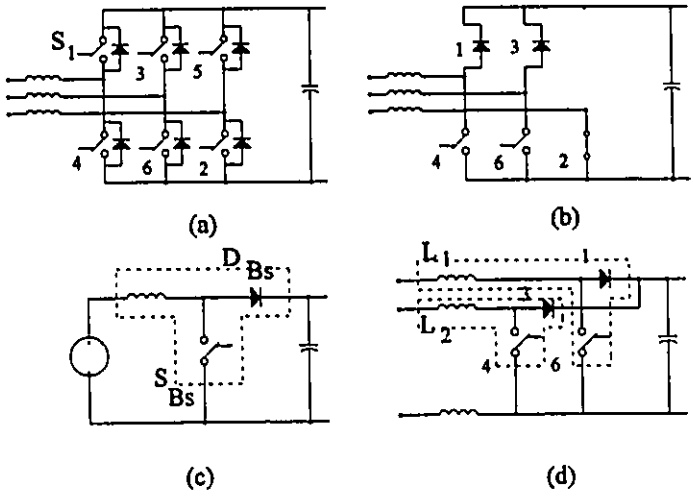

Fig. 2.7 (a) Synchronous link converter, (b) arbitrary state of switches, (c) dc/dc Boost converter, (d) same switch state as in (b).

The single-line equivalent circuits of the input/output terminals are shown in Fig. 2.4(c,d). A comparison of Figs. 2.4(a,b) and Figs. 2.4(c,d) reveals the duality between the two schemes except for the fact that current-source is usually obtained by means of a voltage source in series with an inductor. The converter has a single inductor input filter which makes it more immune to system resonant frequencies. However, power conversion and transfer is more complex. From Fig. 2.4.c it is seen that the voltage source topology is modelled as a voltage source at the input terminals. Therefore, there are two voltage sources connected across an inductor. It is concluded that the input inductor is necessary for operation of this converter. Also, the current through the input inductor must be controlled in a closed-loop fashion. In the voltage-source topology, output dc voltage and input line currents are the independent variables while input ac voltages and output dc current are the dependent variables. From the above, the input/output current/voltage relationships can be described

by:

$$i_{dc}(t) = SW_{p,a}(t)\,i_a(t) + SW_{p,b}(t)\,i_b(t) + SW_{p,c}(t)\,i_c(t) \tag{2.11}$$

$$v_{rec,j}(t) = SW_{p,j}(t)\; v_{dc}(t) \qquad for \quad j \in \{a,b,c\} \tag{2.12}$$

where $SW_{p,j}(t)$ is the phase switching function. The output dc voltage is obtained from the following:

$$V_{dc} = \frac{2\,V_{rec}}{M} \tag{2.13}$$

$$where \qquad M_{max} = \frac{2}{\sqrt{3}} \tag{2.14}$$

where M is the modulation index and V_{rec} is the peak value of the rectifier ac line-to neutral input voltage. Therefore, the minimum voltage that can be achieved by a voltage source topology rectifier is:

$$V_{dc,min} = \sqrt{6}\,V_{rec,rms} = 2.449\; V_{rec,rms} \tag{2.15}$$

As seen from (2.13), the dc voltage here is inversely proportional to the modulation index M, which is typical of a boost configuration. A voltage source topology (for one possible switch state) and a Boost dc/dc converter are shown in Fig. 2.7. Again it is assumed that phase c has the most negative voltage, hence switch 2 is always closed. It is seen that the "diode-switch-inductor" arrangement in the PWM Synchronous Rectifier is similar to that of the dc/dc Boost converter. Two possible boost configurations are obtained through (L_1,D_1,S_6) or (L_2,D_3,S_4). Results for the voltage-source topology

are shown in Fig. 2.8. The input line-to-line voltage of the converter has the same shape as the line-to-line switching pattern. The harmonics are attenuated by the input inductor (synchronous link).

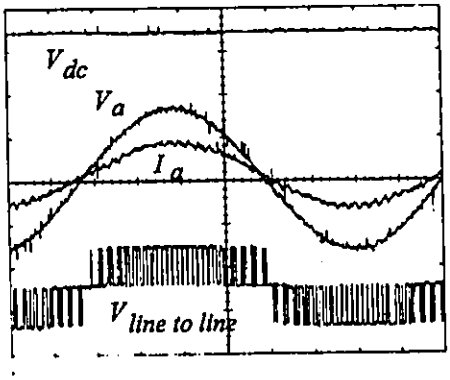

Fig. 2.8 Experimental results, Synchronous Rectifier.

Table 2.2 Per unitized values. ($M = 1, f = 60$ Hz)

	current source	voltage source
Z_{dc}	1	1
$I_{a,rms}$	1	1
$V_{ph,rms}$	1	1
P_{dc}	3	3
I_{dc}	1.633	1.061
V_{dc}	1.837	2.828

Table 2.3 KVA ratings in pu.

kVA rating of the switches		
	PWMBR	PWMSR
ISW_{ave}	0.544	1.061
ISW_{rms}	0.943	0.707
ISW_{peak}	1.633	1.414
P_{dc}	3	3
SW_{ut}	0.375	0.393
$KVA_{converter}$	3.06	3.23
V_{peak}	2.449	2.828

kVA rating of filter components		
	PWMBR	PWMSR
X_L	0.2	0.4
X_C	4.15	---
X_{Ldc}	0.22	---
X_{Cdc}	---	7.67
KVA_C	0.822	---
KVA_L	0.269	0.385
KVA_{total}	1.091	0.385
W_{Ldc}	0.124	---
W_{Cdc}	---	0.237
W_{total}	0.124	0.237

2.3 Comparison of the Two Topologies

In order to obtain a fair comparison, the following are assumed:

- Identical switching patterns (Sinusoidal PWM, $M = 0.91$, switching frequency $f_{sw} =$ 27 pu),
- equal input power and input voltage,
- ideal converter components (input power = output power),
- unity power factor operation,
- identical Total Harmonic Distortion (THD) of input/output waveforms.

The rms values of the input line current and the input phase voltage are chosen as the base values and are identical in both cases. The per-unitized quantities are given in Table 2.2.

2.3.1 Switch and Converter KVA Ratings

Switch and converter kVA ratings are given in Table 2.3. In obtaining these values only the fundamental component is considered and $M = 1$. The switch utilization factor is defined by:

$$SW_{ut} = \frac{P_{dc}}{N_{sw} ISW_{ave} V_{peak}} \tag{2.16}$$

where N_{sw} is the number of switches, P_{dc} is the dc power, V_{peak} is the peak voltage rating of the switch and ISW_{ave} is the average switch current. The stored energy in the dc link inductor and capacitor are defined in per unit as:

$$\left\{ \begin{array}{l} W_{Ldc} = \frac{1}{2} X_{Ldc} I_{dc}^2 \\ W_{Cdc} = \frac{1}{2} \frac{V_{dc}^2}{X_{Cdc}} \end{array} \right\} \qquad (2.17)$$

where X_{Ldc}, X_{Cdc} are the dc side impedances. The converter kVA rating is calculated by multiplying the rms values of the rectifier input current and its terminal voltage. From Table 2.3 it can be concluded that PWM Synchronous Rectifier (PWMSR) has higher voltage rating and lower current ratings and it results in better switch utilization. However since both converters are operating with unity power factor, the VAR of the input filters must be supplied through the converter. Because of a larger size of input inductor for PWMSR, the converter kVA rating is higher than that of the PWM Buck Rectifier. This fact becomes clear later, when the input filters are designed and phasor diagrams studied. The switches used in PWMSR must be bidirectional, which means 6 switches and 6 diodes are needed.

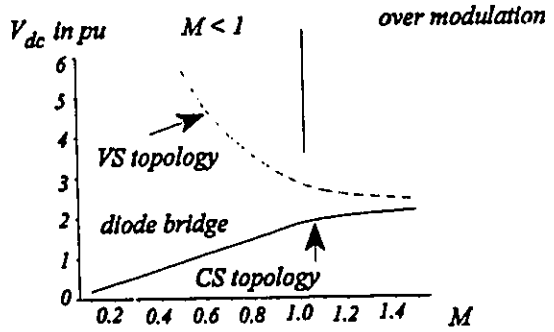

Fig. 2.9 Operating regions.

2.3.2 Operating Regions

The regions of operation for both converters are shown in Fig. 2.9. The case of a three-phase diode rectifier is also included for comparison purposes. For the same input ac source, the PWMSR results in higher dc output voltage for all modulation indices. As seen from Fig. 2.7.a, the six antiparallel diodes form a bridge rectifier if they are forward biased. Therefore proper operation of the Synchronous Rectifier places restrictions on the output voltage. This limit is given by the following:

$$\sqrt{3}\ \| V + j\omega L I \| \le V_{dc} \tag{2.18}$$

where L is the line inductance. For unity power factor operation (2.18) can be rewritten as:

$$I^2 \le \frac{(\frac{V_{dc}^2}{3} - V^2)}{(\omega L)^2} \tag{2.19}$$

Fig. 2.10 depicts the allowed region of operation of the PWMSR obtained from (2.19). For

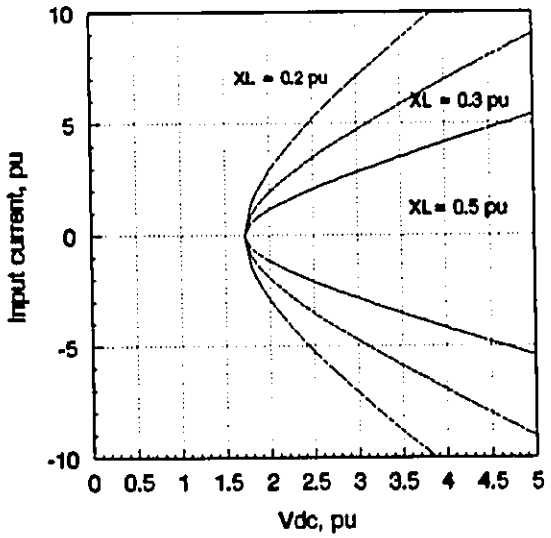

Fig. 2.10 Regions of possible unity power factor operation.

proper operation of the PWMSR, the output capacitor should be initially charged to a voltage higher than specified in Fig. 2.9.

2.3.3. Filtering Requirements

The objective of this section is to design and compare minimum filter requirements for the two rectifier topologies. First certain input/output constraints must be specified. These constraints are the Total Harmonic Distortion (THD) of the input line current and the ripple of the output dc voltage. The THD of a waveform in general is defined as:

$$THD_{wave} = \frac{\sqrt{wave_{rms}^2 - wave_1^2}}{wave_1} \times 100 \qquad (2.20)$$

where the subscript *rms* and *1* denote the rms value and the fundamental component of that waveform.

A. PWM Buck Rectifier

In order to design the input filter, it is first assumed that the output dc current is ripple free and the filter components are designed to meet the input THD requirements. These are obtained from the followings:

$$\begin{Bmatrix} X_C = \dfrac{THD_v V_1}{\sqrt{\sum_{h=2}^{\infty} \left(\dfrac{I_{rec,h}}{h}\right)^2}} \\ X_L = \dfrac{X_C \sum_{h=2}^{\infty} \dfrac{I_{rec,h}}{h^2}}{I_1 THD_i} \end{Bmatrix} \qquad (2.21)$$

where h is the harmonic order and L,C are the ac side filter components. The value of output inductor is then chosen from the constraint on the output dc current. In this case, the input currents and voltages are assumed sinusoidal waveforms and the output inductor is calculated from:

$$X_{Ldc} = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_{dc,h}}{h}\right)^2}}{I_{dc}THD_{i,dc}} \tag{2.22}$$

The results for a PWM Buck Rectifier with the designed input filter are given in Fig. 2.5 while simulation results for a rectifier without the input filter are shown in Fig. 2.11. The input filter reduces the input THD_i to 5%. As a result however, the rectifier input voltage is distorted and

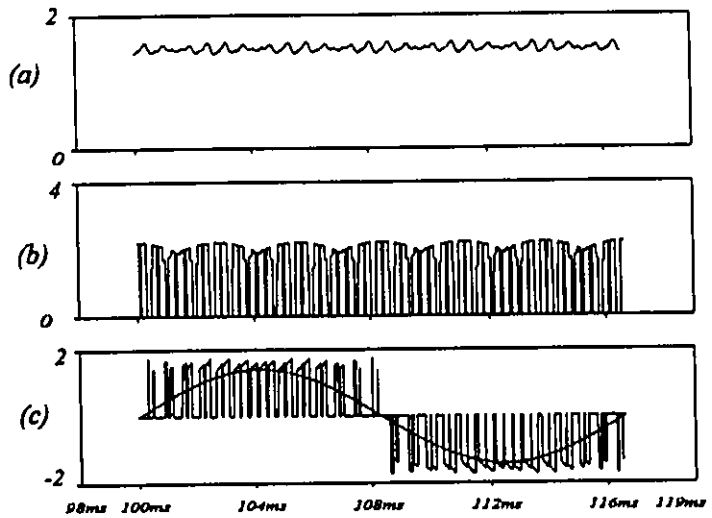

Fig. 2.11 Input/output characteristics of current source topology without the input filter. (a) Output dc current, (b) output dc voltage, (c) input line current and phase voltage.

the dc output voltage is deformed. In order to avoid low frequency harmonic components in the dc output voltage, the input rectifier THD_v must be limited to a small value (here 10%) and also proper damping should be provided in the filter circuit.

B. PWM Synchronous Rectifier

It is assumed that the output voltage is pure dc and the link inductor is designed accordingly to meet the input THD_i requirements. The following equation is used:

$$X_L = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{V_h}{h}\right)^2}}{I_1 THD_i} \tag{2.23}$$

When the input filter is calculated, the input line current are assumed to be ideal sine waveforms and the following equation gives the value for the dc capacitor:

$$X_{Cdc} = \frac{THD_{v,dc} V_{dc}}{\sqrt{\sum_{h=2}^{\infty}\left(\frac{I_{dc,h}}{h}\right)^2}} \tag{2.24}$$

The values of the filter components and their kVA ratings are given in Table 2.3. It is concluded that the filter components for the PWM Rectifier are larger than those needed for the PWMSR with the same input/output harmonics specifications. Also, the input inductor for PWMSR is much larger than that of the PWMBR.

2.3.4 Power Factor Considerations

Fig. 2.12.a shows the single-line phasor diagram for PWMSR with unity power factor

operation. When the input power factor is unity, the input voltage and the input current of the converter have a phase shift of δ degrees. Therefore the converter must supply the inductive VAR required by the synchronous link inductor. This results in higher converter kVA rating (Table 2.3). Unity power factor can be achieved for different levels of power transfer and different modulation indices as long as the following equation is satisfied:

$$R_{dc} > \frac{X_L}{\sqrt{\frac{3}{V_{dc}^2}(1 - \frac{3}{V_{dc}^2})}} \tag{2.25}$$

where R_{dc} is the load resistance.

Fig. 2.12.b shows the single-line phasor diagram for PWMBR with unity power factor operation. Under this condition the modulating signal must be in phase with the rectifier current. The position of this signal varies with operating point. A phase shifting scheme to operate the PWMBR with unity power factor is proposed in ***chapter 4***.

2.3.5 Operation with Unbalanced AC Inputs

A. PWMBR

According to (2.5) and (2.6) and assuming balanced three-phase switching patterns, the input line currents of a PWMBR are always balanced. However with unbalanced input ac sources the input rectifier voltages will be unbalanced which result in a distorted dc output voltage. Due to the reflection of the unbalanced input voltages into the dc side, the dc output voltage will contain uncharacteristic harmonics of order of ($2h$ pu, h = 1,2,...). These abnormal harmonics require a larger output filter to achieve similar ripple in the output current.

B. PWMSR

Since the output dc voltage is the independent variable and is assumed to be constant, for balanced three-phase switching patterns, the input voltages of the converter will be balanced. From Fig. 2.3.c it is concluded that the input line currents will be unbalanced, requiring an increase in synchronous link inductor. Therefore line currents contain uncharacteristic harmonics ($2h$ pu, h = 1,2,..) which were not present in PWMBR under unbalanced operation. Also, the output dc current will contain uncharacteristic harmonics which should be attenuated by a larger output filter.

2.3.6. Control Aspects

In current source PWM rectifiers the adjustable dc output voltage can be obtained through controlling the modulation index M or phase shifting of the PWM switching pattern. Since the phase shifting inherently yields poor input power factor, control by the modulation index is used over most of the operating range. However at low output voltages, the pulse width may become too short and phase shifting may then be employed to control the output voltage. The PWM pattern can be synchronized with the rectifier input voltage and near unity power factor obtained for M = 1. As M decreases the rectifier furnishes reduced (leading) power factors.

The operation of PWMSR is based on the control of power transfer instead of direct modulation index control which is the case in PWMBR. The power delivered to the dc load can be varied in a number of ways for example, by controlling the phase shift angle (δ) between the ac mains $\vec{V}_a$ and the converter input voltage $\vec{V}_{rec}$, Fig. 2.12.a. Therefore a closed loop control scheme is needed in all cases to balance the input and the output power. This complicates the

converter design.

2.4 Summary of Operating Characteristics

The operating characteristics and features of PWM rectifiers and synchronous link converters can be summarized as follows:

- The PWMSR always leads to higher dc output voltage than the PWMBR.
- The PWMSR is capable of regenerative operation by dc current reversal, whereas the PWMBR by dc voltage reversal (this is a drawback in many applications).
- The PWMSR has smaller filter size and is immune to resonance frequencies. The input inductor is essential to converter proper operation. PWMBR needs a larger filter and the filter resonant frequency should avoid harmonics.
- Unity power factor operation of the PWMSR is obtainable for different power levels and different modulation indices through the phase shifting of the switching pattern. This is also true for PWMBR, as will be shown in a later chapter.

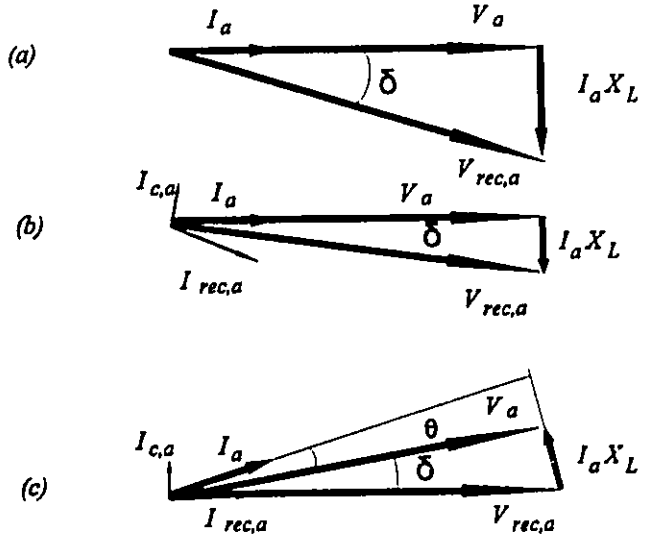

Fig. 2.12 Phasor diagrams. (a) Voltage source topology unity PF, (b) current source topology unity PF, (c) current source topology, pattern in phase with rectifier input voltage.

- Minimum kVA rating of the switches for PWMBR is achieved when input voltage and input current of the rectifier are in phase.

- Under unity power factor operation the VAR required by the input filters must be supplied through the converter. In the case of PWMSR this VAR requirement is larger than that of the input inductor of the PWMBR (due to larger size of the input inductor and since there is no capacitor), resulting in a larger converter kVA rating.

- When operating with unbalanced ac mains and with a balanced pattern, input currents of PWMBR are always balanced, but the input currents of PWMSR are unbalanced and contain uncharacteristic harmonics.

- closed loop control is essential to operate a synchronous link converter.

- In order to start up the PWMSR the dc capacitor must be initially charged to a minimum value to reverse bias the anti-parallel diodes.

2.5 Conclusions

The PWM Synchronous Rectifier and the PWM Buck Rectifier are compared when operating with unity power factor, the same modulation index ($M = 0.91$) and delivering similar output power. In general it is concluded that Synchronous Rectifier gives a higher performance but is more complicated to operate. Unity power factor and regenerative operation are achieved with closed loop control. PWM Buck Rectifier provides good performance with simple control strategies. It requires a larger filter to suppress the input line harmonics, but is simple to operate since open loop operation is possible.

CHAPTER 3

INPUT FILTER DESIGN FOR PWM CURRENT-SOURCE RECTIFIERS

3.1 Introduction

Static power converters when operated from an ac power system generate current harmonics which are injected back into the ac system. These current harmonics result in voltage distortions which affect the overall ac system. The principal method of reducing the harmonics generated by static converters is by providing input filters using reactive storage elements. Filtering requirements for PWM current-source rectifiers are usually satisfied through the use of low-pass LC input filters. This chapter presents a systematic and user-friendly approach to choosing the filter components. Two types of filter configuration are discussed. Design of LC filters involves the positioning of the resonant frequency to meet the harmonic attenuation requirements, and introducing damping at the resonant frequency to avoid amplification of residual harmonics. The problem is further complicated by considerations related to cost, power factor, voltage attenuation, system efficiency and filter parameter variation. Practical design considerations are detailed and design equations derived. Two examples with different design objectives are presented and compared. Simulated results are

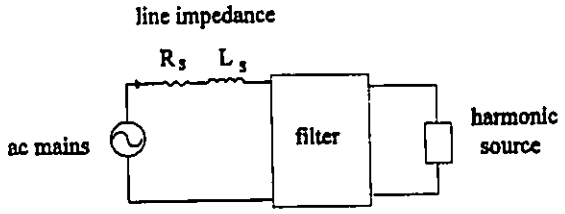

Fig. 3.1 Typical filter connection.

presented to validate the design approach.

3.2 Description Of The Filter Characteristics

A typical connection of PWM converters to the ac mains through an input filter is shown in Fig. 3.1. Different types of filter can be used to suppress the harmonics generated by the harmonic source shown in Fig. 3.1. If the harmonic source has a current source characteristic, the commonly preferred choice would be a second order LC filter due to its simplicity and minimum number of components required. In order to avoid an infinite gain at the resonant frequency, damping resistors are needed in the filter. There are two possibilities for the location of the damping resistors. They can be inserted either in series with the capacitor (type A) or in parallel with the filter inductor (type B). The single line diagrams for these two types of filter connected between the ac source and PWM converter, for fundamental and harmonic frequencies are shown in Fig. 3.2. From Fig. 3.2.d, the transfer function of the filter type A is obtained as:

$$\left\{ \begin{array}{l} \dfrac{I_{Lh}}{I_{rec,h}}(s) = \dfrac{1 + R_f C s}{LCs^2 + (R_f + R_s)Cs + 1} = G(s) \\ \omega_b = \dfrac{1}{\sqrt{LC}} \\ \xi = \dfrac{(R_f + R_s)}{2}\sqrt{\dfrac{C}{L}} \end{array} \right\} \qquad (3.1)$$

where R_s, L are the line impedance (including the added filter inductance), R_f, C are the filter components and ξ and ω_b are the damping factor and resonant frequency. For a type B filter the transfer function is given by:

$$\left\{ \begin{array}{l} \dfrac{I_{l,h}}{I_{rec,h}}(s) = \dfrac{R_f + L_s s}{(R_f + R_s)LC\,s^2 + (R_f R_s C + L)s + R_f} = G(s) \\ \omega_b = \dfrac{R_f}{(R_s + R_f)\sqrt{LC}} \\ \xi = \dfrac{(R_f R_s C + L)}{2\sqrt{R_f (R_s + R_f) CL}} \end{array} \right\} \qquad (3.2)$$

The line resistance R_s changes the position of the resonant frequency. If the line resistance is neglected, the two configurations result in similar resonant frequencies. Since a resistance has to be connected in parallel with the line inductance, the type B filter has implementation problems. Therefore, from now on only the type A filter is studied. Although the procedure equally applies to any filter.

3.3 Proposed Design Procedure

The first step in designing a filter is to identify the position and amplitude of harmonics to be attenuated. If the PWM pattern of the converter is known, the amplitude and order of the harmonics

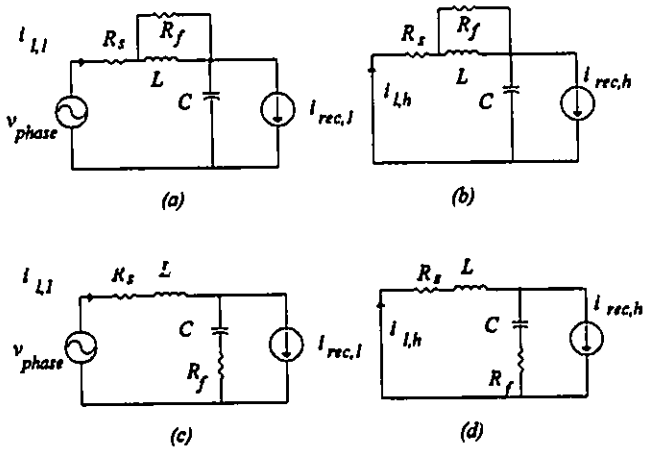

Fig. 3.2 Single-line diagrams for fundamental and harmonic frequencies. (a,b) Filter type B, (c,d) filter type A.

injected can be obtained. Also, the worst operating point in terms of harmonics (modulation index) can be identified. The second step is to choose a suitable break frequency for the filter. This is done based on the following considerations:

(a)- To achieve a desired attenuation of the dominant harmonic, which is at a multiple of switching frequency, f_{sw}.

(b)- To avoid amplification of the residual harmonics in the dead-band.

To satisfy the first constraint, the gain of an LC filter for harmonic components should be obtained. To meet the second specification, the required damping of the filter is designed considering the amplitudes of residual harmonics in the dead-band and the maximum amplification allowed. For a given value of the attenuation factor (α), the maximum amplification of the residual harmonics in the dead band (A) and the gain of the filter at the fundamental frequency f_1 (B), the filter components can be obtained from the following set of equations:

$$\left\{ \begin{array}{l} \left| \dfrac{I_{l,h}}{I_{rec,h}} \right|_{f=f_{sw}} = \alpha \\ \left| \dfrac{I_{l,h}}{I_{rec,h}} \right|_{f=f_b} = A \\ \left| \dfrac{I_{l,h}}{I_{rec,h}} \right|_{f=f_1} = B \end{array} \right\} \tag{3.3}$$

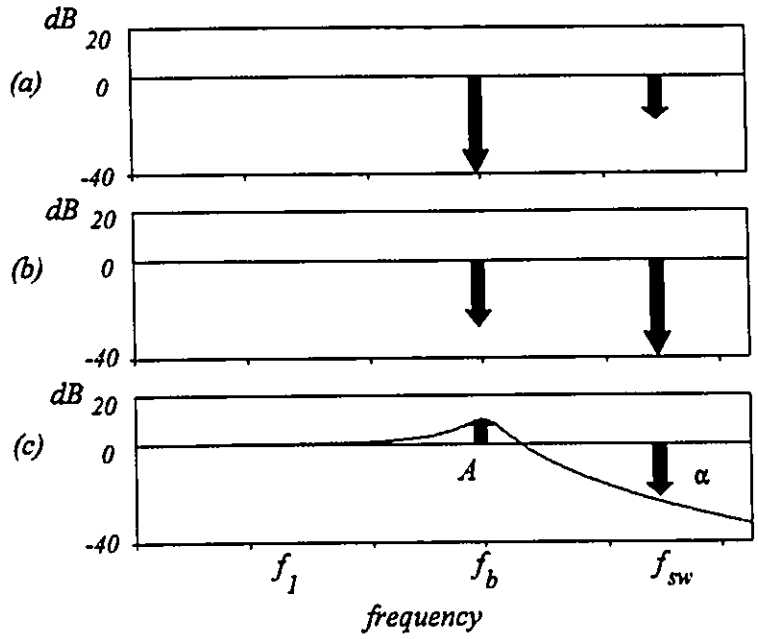

Fig. 3.3 (a) Frequency spectrum of the harmonic current source, (b) desired frequency spectrum of the line current, (c) characteristics of the input filter (A and α are in dB.)

In order to provide a better representation of the above procedure, (3.1) can be rewritten in logarithm as follows:

$$\|G\|(\log) = \|I_{Lh}\|(\log) - \|I_h\|(\log) \tag{3.4}$$

From (3.4), it is seen that the filter transfer function can be obtained by subtraction in logarithmic domain. The design procedure is illustrated in Fig. 3.3. The frequency spectrum of the line current before filtering, $\|I_{rec,h}\|$, is shown in Fig. 3.3.a. Since the desired THD of the line current is specified and since the rectifier switching pattern is known, the desired line current spectrum can be calculated, Fig. 3.3.b. By subtracting Fig. 3.3.a from Fig. 3.3.b, the values of A and α (in dB) are obtained. Knowing the gain of the filter at three different frequencies (A, B, α) , the filter characteristics, is obtained (Fig. 3.3.c). The design of the filter by using (3.3) is not complete if the performance specifications are not met by the designed filter. Also the input filter distorts the converter input

voltage and changes the harmonics generated by the converter. Thereby this distortion should be considered in filter design procedure. The final design of the filter is obtained through an iterative process to meet the desired specifications. The flow chart of filter design is given in Fig. 3.4. Since the filter involves design of two components (L&C), assigning two constraints (THD_i, THD_v) fixes the values of L&C. However, one can choose to put other constraints such as kVA or displacement angle minimization. A trade off has to be made and the overall specifications can be put together in a filter optimization program to obtain the optimum filter design. These factors and other constraints are discussed later.

3.4 Practical Considerations

3.4.1 Input Power Factor

The phasor diagram of the PWM rectifier is shown in Fig. 3.5, where it is assumed that the switching pattern is synchronized and is in phase with the rectifier input ac voltage (the capacitor

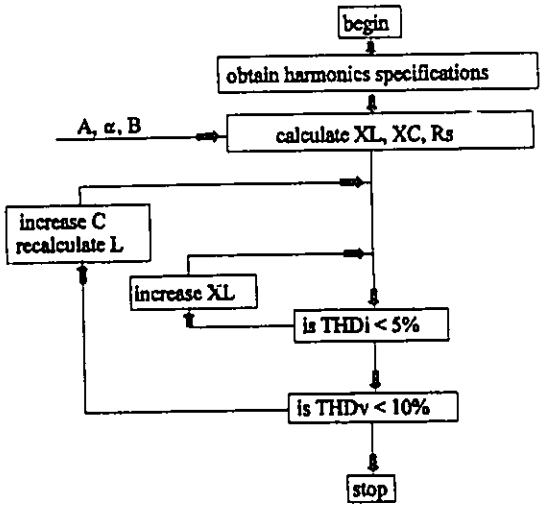

Fig. 3.4 Flow chart of the filter design procedure.

voltage). The input power factor is defined as:

$$PF = IDF \times DF \tag{3.5}$$

where the Distortion Factor, DF quantitize the harmonics content of the current waveform and is defined by:

$$DF = \frac{I_{l,1}}{I_{l,rms}} = \frac{1}{\sqrt{1 + THD_i^2}} \tag{3.6}$$

The Input Displacement Factor, IDF is given by:

$$IDF = \cos\theta \tag{3.7}$$

where θ is the displacement angle between the fundamental components of the line current and voltage, Fig. 3.5. Using a filter at the input terminals of the PWM rectifier increases the Distortion Factor but decreases the Input Displacement Factor. Therefore, it may as well decrease the overall input Power Factor. Thereby, it is necessary to limit the displacement angle (θ in Fig. 3.5). The displacement angle can be calculated by the following equations:

$$\theta = \theta_1 - \delta \tag{3.8}$$

$$\tan\delta = \frac{Z_L I_{rec} \sin(\angle Z_C)}{V_{rec}\left[1 + \frac{Z_L}{Z_C}\cos(\angle Z_L - \angle Z_C)\right]} \tag{3.9}$$

$$\tan\theta_1 = \frac{\frac{V_{rec}}{Z_C}\sin(-\angle Z_C)}{I_{rec} + \frac{V_{rec}}{Z_C}\cos(-\angle Z_C)} \tag{3.10}$$

$$\angle Z_L = \tan^{-1}\frac{\omega L}{R_s} \quad and \quad \angle Z_C = -\tan^{-1}\omega R_f C \tag{3.11}$$

where Z_L and Z_C denote the line impedance and the filter capacitor branch impedance, V_{rec} is the amplitude of the rectifier input voltage and I_{rec} is the amplitude of the rectifier input current which varies with the modulation index as:

$$I_{rec} = \frac{\sqrt{3}}{2} M I_{dc} \tag{3.12}$$

where I_{dc} is the dc link current. When line resistance and damping resistors are neglected ($\angle Z_C = -90°$, $\angle Z_L = 90°$), the angle θ is given by the following:

$$\theta = \tan^{-1}\frac{V_{rec}}{I_{rec} X_C} - \tan^{-1}\frac{X_L I_{rec}}{V_{rec}(1-\frac{X_L}{X_C})} \tag{3.13}$$

where X_L and X_C are the line and capacitor branch impedance. The displacement angle θ is dependent on the modulation index M, since I_{rec} varies with M. Figure 3.5 depicts the dependency of θ to modulation index M with the break frequency f_b as a parameter. It is seen that increasing M increases θ, hence decreasing the input displacement power factor. Figure 3.7 shows variation of θ as a function of X_L with modulation index M as a parameter. As the input inductance increases, the phase

displacement between input current and input voltage decreases and there is a value of X_L which obtains unity IDF. Therefore the filter can be designed in a way that unity IDF at $M = 1$ is achieved and as M decreases the rectifier furnishes leading power factors (Figs. 3.6, 3.7).

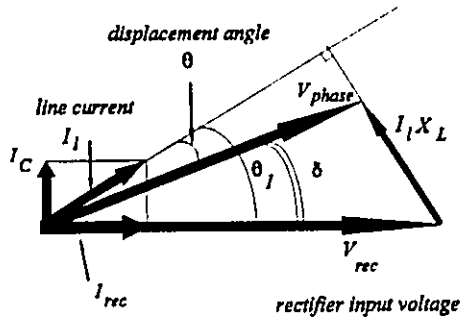

Fig. 3.5 Phasor diagram of PWM Buck Rectifier, pattern is synchronized with the capacitor voltage.

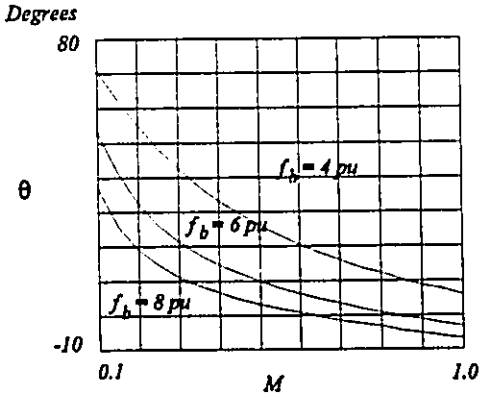

Fig. 3.6 Displacement angle as a function of modulation index M, (X_L = 0.2 pu, f_{sw} = 27 pu).

3.4.2 KVA Ratings

The total kVA of the filter is given by the following:

$$TKVA = \frac{1}{2}\sum_{h=1}^{\infty}\left(h\, I_{l,h}^2\, X_L + \frac{h\, V_{rec,h}^2}{X_C}\right) \tag{3.14}$$

where h is the order of harmonics. As expected, $TKVA$ increases when X_C is decreasing, and X_L is increasing. Also, as modulation index M decreases the kVA decreases. Figure 3.8 shows the variation of $TKVA$ as a function of modulation index M. The cost of the filter is given by:

$$cost \propto \frac{1}{2}\sum_{h=1}^{\infty}\left(\rho\, h\, I_{l,h}^2\, X_L + \frac{h\, V_{rec,h}^2}{X_C}\right) \tag{3.15}$$

where ρ is the ratio between the cost of the inductive and capacitive kVA. If $\rho = 1$, the cost of filter is proportional to $TKVA$. The $TKVA$ is mostly capacitive which means that in order to minimize the cost of the filter, the value of the input capacitor must be minimized. However, at a constant filter break frequency (f_b), decreasing C will result in increasing L and consequently decreasing lagging IDF. Therefore a trade off between the cost of the filter and the input IDF exists. Assuming the

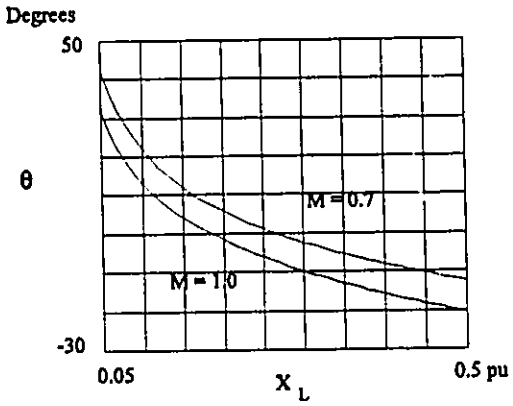

Fig. 3.7 Displacement angle as a function of filter inductance X_L, (f_b = 5.4 pu).

harmonic distortion of the line current and the voltage drop across the line inductor are very small and all the harmonic currents generated flow in the capacitor branch, the current and voltage of the capacitor branch are calculated as follows:

$$I_{C,rms} = \sqrt{\frac{1}{2}\sum_{h=2}^{\infty} I_{rec,h}^2 + \left(\frac{V}{X_C}\right)^2} \tag{3.16}$$

$$V_{C,rms} = V_{rec,rms} = \sqrt{\frac{1}{2}\sum_{h=2}^{\infty} \left(\frac{I_{rec,h}X_C}{h}\right)^2 + V^2} \tag{3.17}$$

where I_h = hth harmonic component of the rectifier input current, and V = input ac phase voltage. The kVA of the capacitor is defined as:

$$KVAC = I_{C,rms}V_{C,rms} \tag{3.18}$$

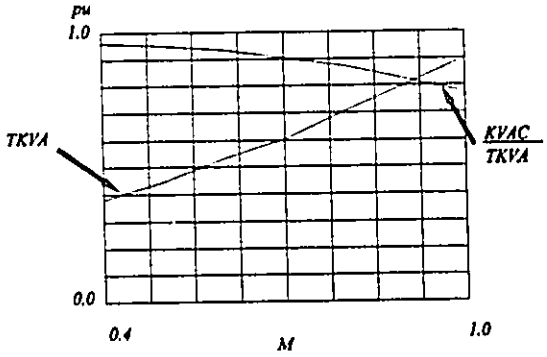

Fig. 3.8 *TKVA* as a function of modulation index M.

By equating the derivative of the above equation, the value of X_C which minimizes $KVAC$ is obtained as:

$$X_C = \frac{V}{\left(\sum_{h=2}^{\infty}\left(\frac{I_{rec,h}}{h}\right)^2 \sum_{h=2}^{\infty} I_{rec,h}^2\right)^{\frac{1}{4}}} \tag{3.19}$$

However, the above value of X_C does not guarantee that THD_v constraint is met. The variation of *KVAC* as a function of X_C is depicted in Fig. 3.9. It is seen that there is a valley where the *KVAC* does not vary rapidly with the change in *C*. Therefore, it is possible to obtain a value of *C* that provides low kVA rating and achieves near unity IDF. This fact can be used to change the design flow chart given in Fig. 3.4.

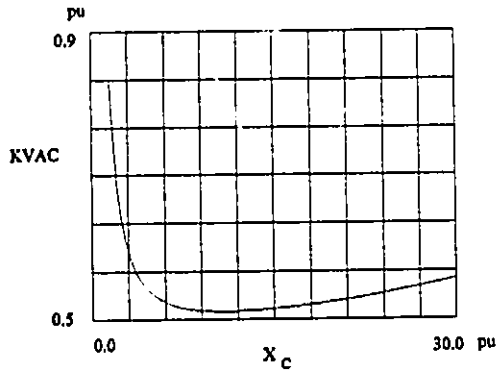

Fig. 3.9 Capacitive kVA as a function of capacitor impedance X_C.

3.4.3 Damping

By using PWM techniques, the frequency spectra of the input waveforms can be shaped and harmonic components moved to a higher frequency. This results in the creation of a "dead-band" where no unwanted harmonic components exist. The break frequency of the LC filter can therefore be positioned in this dead-band, Fig. 3.10. However in practice due to the presence of imperfections such as asymmetry in gating signals, asynchronism in the PWM method, switching delays and other inaccuracies in implementation, some unwanted harmonics with small amplitudes exist in the dead-band, Fig. 3.10. These harmonics can be amplified by the filter, if no damping is provided. On the

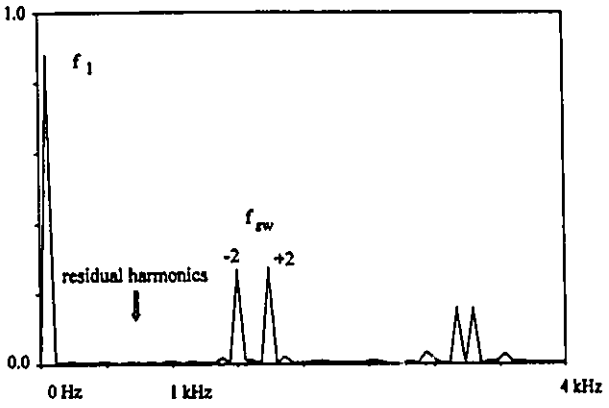

Fig. 3.9 Harmonic spectrum of SPWM switching pattern ($M = 1, f_{sw} = 27$ pu).

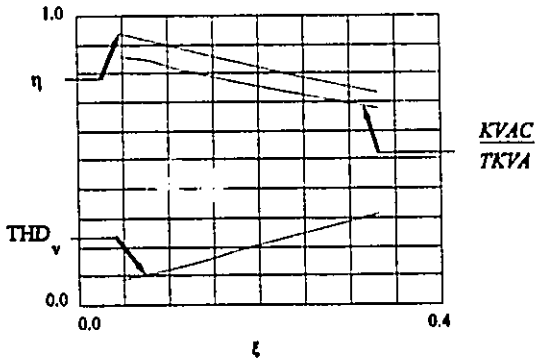

Fig. 3.11 Effect of damping on the circuit specifications, η= efficiency, ξ = damping factor.

other hand, a highly damped filter will not necessarily meet the harmonics attenuation requirements [67]. In order to avoid amplification of the residual harmonics in the dead-band region, proper damping of the LC filter is required. Since the amplitude of the residual harmonics are expected to be less than 1%, an amplification of 4-7 times can be tolerated. This gives a criteria for choosing the parameter A in the set of equations (3.3). Adding damping resistors has two major effects on the performance of the system; it reduces the system efficiency, and increases the THD_v

It is preferred to only add the damping in the capacitor branch, since the current flowing in this branch is smaller than the inductor branch. The additional losses are calculated from:

$$P_{loss} = I_{C,rms}^{2} R_f \tag{3.20}$$

Inserting the damping resistor introduces a zero in the filter transfer function. Therefore, for high frequencies, the filter behaves as a first order filter which has a reduced attenuation factor. The effect of damping on THD_v and efficiency are shown in Fig. 3.11.

3.4.4. Parameter Variation

Variations in the values of the filter components results in the variation of break frequency of the filter. This variation can be critical to operation of a tuned filter. But, for a low pass filter, the effect of this variation is negligible, especially if the filter is properly damped. However, the

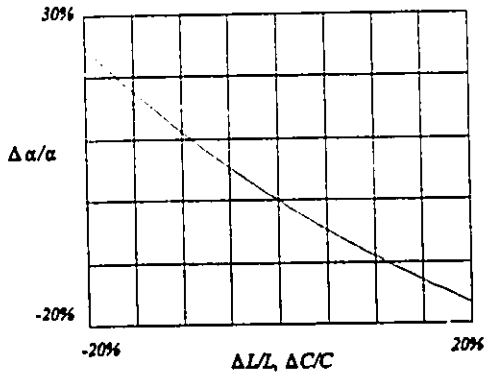

Fig. 3.12 Effect of parameter variation on the attenuation factor, (α).

attenuation factor (α) of the filter will differ from the one predicted for the nominal values. The variation of α is given by:

$$\frac{\Delta\alpha}{\alpha} = -\frac{\frac{\Delta C}{C} + \frac{\Delta L}{L}}{1 + \frac{\Delta C}{C} + \frac{\Delta L}{L}} \tag{3.21}$$

The change in the attenuation factor ($\Delta\alpha$) as a function of ΔL/ or ΔC is depicted in Fig. 3.12.

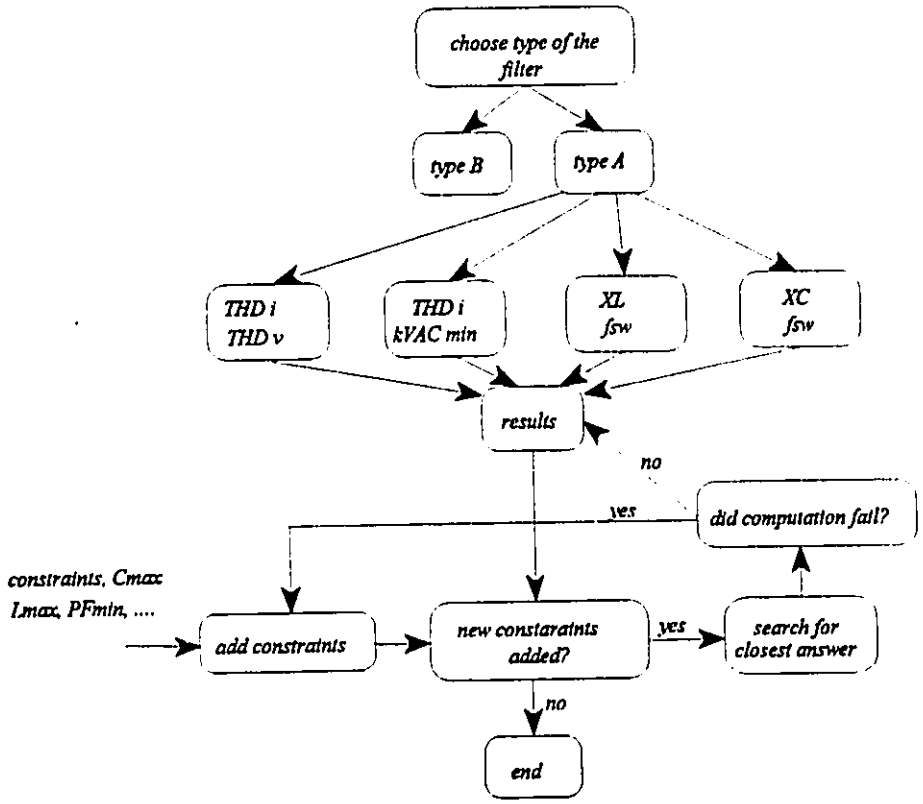

Fig. 3.13 Flow chart of the filter design procedure.

3.4.5. Effect of the Filter on the Rectifier Performance

The addition of an input filter to the PWM rectifier distorts the input ac voltages at the rectifier input terminals. The output dc voltage is given by:

$$v_{dc}(t) = SW_{l,a}(t)v_{rec,a}(t) + SW_{l,b}(t)v_{rec,b}(t) + SW_{l,c}(t)v_{rec,c}(t) \tag{3.22}$$

where $v_{dc}(t)$ = output dc voltage and $v_{rec,j}(t)$ = rectifier input voltages. A distorted input voltage will change the output voltage harmonics and must be considered in the design of the output filter. Therefore, input voltage distortion must be limited to a reasonable value, for the converter to perform as predicted at a particular operating point. Also, it is necessary to ensure capacitive characteristics at the rectifier input terminals. These put additional constraint on the value of the capacitor filter which may override the kVA consideration. An alternative flow chart is shown in Fig. 3.13.

3.5 Design Example

An input filter is designed for a PWM rectifier. Two types of designs are considered.

Design A.

The filter is designed to achieve unity IDF at $M = 1$. The filter break frequency is given by the followings:

$$f_b = \sqrt{\alpha}\, f_{sw} \tag{3.23}$$

$$C = \frac{1}{L(2\pi f_b)^2} \tag{3.24}$$

for a given attenuation factor (α) and rectifier switching frequency f_{sw}, the values of L, C and R_f are found using eqns. 3.(3,23,24).

Design B.

In this case, the cost (*TKVA*) of the filter is minimized. The capacitor value is obtained from (3.19). Then L and R_f are calculated for the same break frequency and damping factor as desgin A.

The results and the specifications of the two designs are given in Table 3.1.

Table 3.1 Filter components.

	Design *A*	Design *B*
X_L	0.17 pu	0.34 pu
X_C	5.1 pu	10.2 pu
THD_i	<5%	<5%
THD_v	10%	19%
V_{dc}	1.69 pu	1.63 pu
P_{dc}	0.872 pu	0.806 pu
R_f	0.09 pu	0.09 pu
θ	1.1°	-13.8°
KVAC	0.68 pu	0.62 pu

basc values; I = 100 A, V = 120V

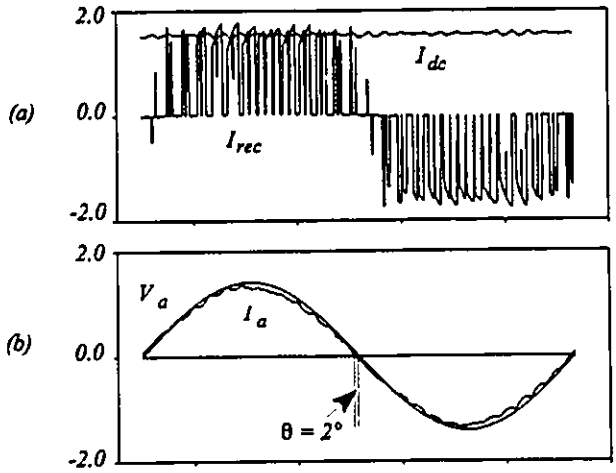

Fig. 3.14 Simulation results of design *A*, (a) input rectifier current I_{rec}, output dc current I_{dc}, (b) phase *a* voltage and current waveforms, V_a, I_a, (in pu).

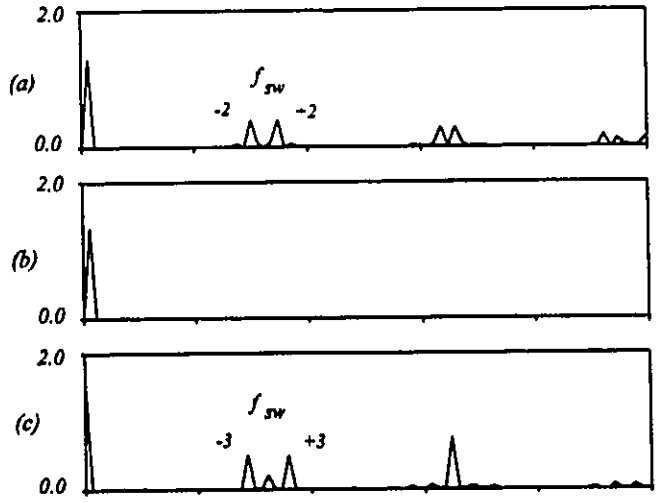

Fig. 3.15 Frequency spectra of input/output waveforms, (a) rectifier input current, (b) input line current, (c) output dc voltage.

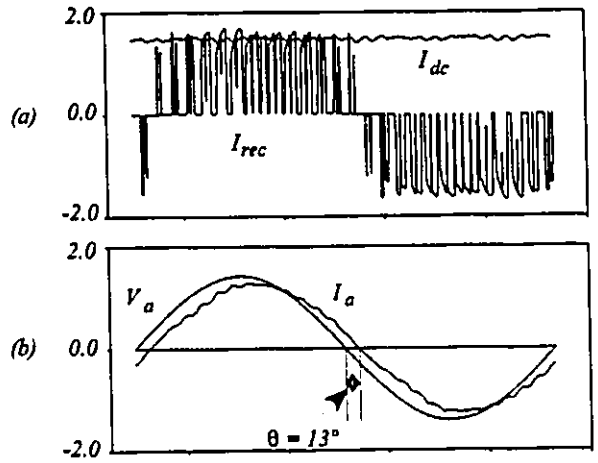

Fig. 3.16 Simulation results of design *B*, (a) input rectifier current I_{rec}, output dc current I_{dc}. (b) phase *a* voltage and current waveforms, V_a, I_a.

3.6 Results

The simulation results for the filter of design *A* in Section 3.5 are depicted in Figs. 3.14, 3.15. Input line current, Input ac voltage and rectifier input current are shown in Fig. 3.14. Input Displacement Factor is unity at $M = 1$. The input line current has a high quality with THD_i less than 5%. Frequency spectra of line current before and after filtering are shown in Fig. 3.15. The frequency spectrum of line current clearly shows the effect of the filter and indicates that there is no amplification of residual harmonics. Simulation results for design *B* are shown in Fig. 3.16. The filter capacitor is minimized but the phase displacement between input current and voltage is increased by about 15°.

3.7 Conclusions

A systematic design procedure for a passive LC input filter for current source PWM

rectifiers is proposed. Basic filtering requirements as well as practical problems such as filter kVA rating, efficiency, damping and converter input power factor are discussed. It is shown that, with the synchronization scheme used, input power factor is affected by both filter inductor and capacitor, while the cost of the filter is decided by the filter capacitor. The design equations and the design procedure are confirmed by simulation results.

CHAPTER 4

CURRENT-SOURCE PWM RECTIFIER WITH FEED-FORWARD COMPENSATION

4.1 Introduction

In ***chapter 3*** it was seen that due to the input filter (needed for current harmonic suppression), the Input Displacement Factor (IDF) is less than unity. Moreover, it varies with the rectifier operating point and may result in unacceptable low values.

In this chapter, a new compensation scheme is proposed which provides unity IDF independent of the rectifier operating point. The characteristics of the proposed scheme are: (a) use of a feed-forward dc current loop and the standard dc voltage/or current regulation loop to regulate the amplitude and phase of the modulating signals; (b) on-line generation of the PWM pattern which results in good system dynamics; (c) simple implementation with minimum hardware since no additional transducer is required. The rectifier is analyzed and design equations are derived. A design example is given and theoretical considerations are verified through simulation. Experimental results obtained on a 1kVA laboratory prototype confirm the

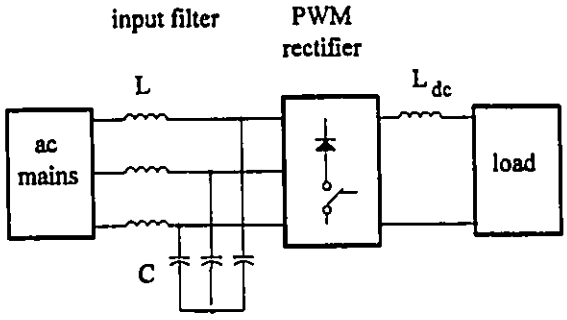

Fig. 4.1 Three-phase current-source PWM rectifier.

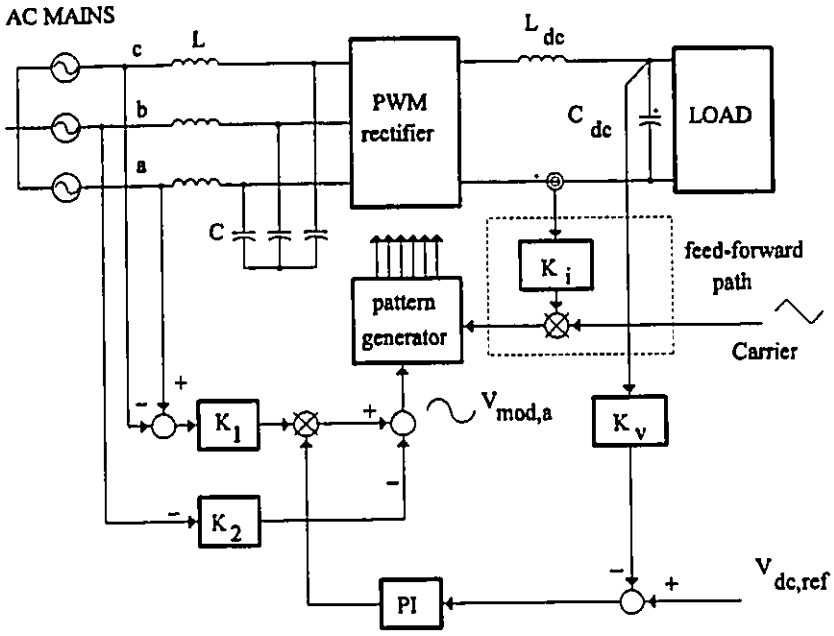

Fig. 4.2 The proposed input displacement compensation scheme, $V_{mod,a}$ denotes the modulating signal for phase *a*.

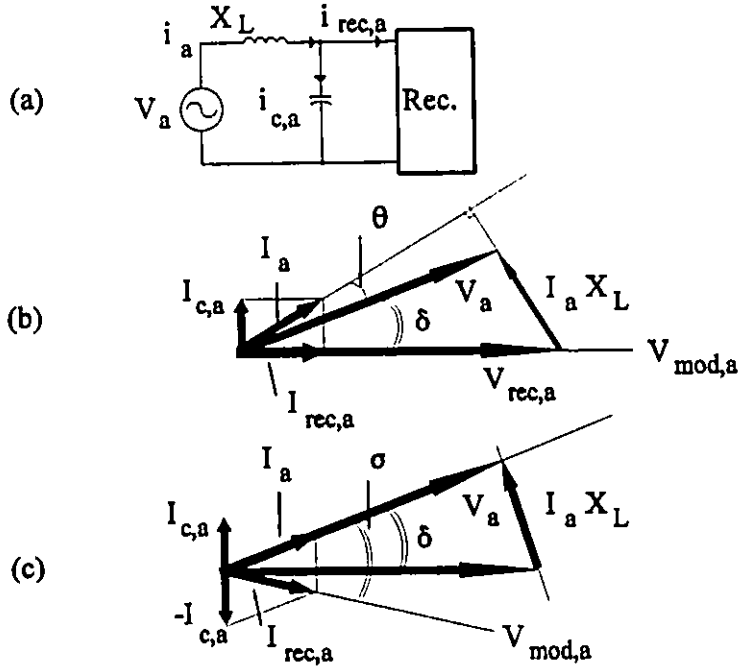

Fig. 4.3 (a) Single line diagram, (b) non-unity displacement factor operation(leading power factor), (c) unity displacement factor operation (θ=0).

feasibility of the proposed compensation scheme.

4.2 Description of the Proposed Compensation Scheme

The current-source PWM rectifier is shown in Fig. 4.1. If the PWM pattern is synchronized with the capacitor voltages, the displacement factor at the rectifier terminal is unity (rectifier input currents are in phase with capacitor voltages), Fig. 4.3.b. However, in this case the ac source must supply/absorb the reactive power absorbed/supplied by the input filter. Therefore, the input power factor at source is not unity and there is a phase-displacement between input ac voltage and line current, θ in Fig. 4.3.b. From Fig. 4.3.b it is concluded that if the rectifier modulating signal is phase shifted properly, the input phase displacement between the current $\vec{I}_a$ and voltage $\vec{V}_a$, can be eliminated, Fig. 4.3.c. In order to calculate the required phase shift, it is necessary to find out the position of the capacitor voltage and then the rectifier current under unity displacement factor operation. Assuming unity displacement factor operation and neglecting the current distortion and line and filter resistances, the input line current and phase voltage can be expressed by:

$$v_a(t) = V \sin \omega t, \qquad i_a(t) = I \sin \omega t \tag{4.1}$$

where V and I denote the amplitudes of phase voltage and line current respectively. The fundamental component of the capacitor voltage in steady state is given by:

$$v_{rec,a}(t) = v_{c,a}(t) = -\omega LI \cos \omega t + V \sin \omega t \tag{4.2}$$

where L is the line inductance and ω is angular frequency. The input rectifier current is:

$$i_{rec,a}(t) = i_a(t) - i_{c,a}(t) \tag{4.3}$$

or:

$$i_{rec,a}(t) = I(1 - \omega^2 LC)\sin \omega t - V\omega C \cos \omega t \tag{4.4}$$

where C is the filter capacitance. In order to achieve unity displacement factor, a modulating signal is needed that generates a fundamental component identical to (4.4). There are many different switching strategies which can generate the desired fundamental rectifier current $i_{rec,a}$ (t). It is not the purpose of this thesis to discuss the best modulation method because this matter has been thoroughly addressed in many references [16],[17]. The sinusoidal PWM is selected because it is relatively simple to implement and is a very well known method.

From the characteristics of a current source PWM rectifier, we know that the rectifier current has the shape of the line-to-line switching pattern. Therefore, if (4.4) is normalized, the required line-to-line modulating waveform is obtained. The normalizing can be done either by dividing (4.4) by the amplitude of the dc current, or by multiplying the carrier waveform by that amplitude. The latter is used in this chapter. The phase modulating signal is obtained by introducing a 30° delay to the line-to-line signal. The resulting phase modulating signal is given by:

$$v_{mod,a}(t) = K_1 F \sin\left(\omega t - \frac{\pi}{6}\right) - K_2 \cos\left(\omega t - \frac{\pi}{6}\right) \tag{4.5}$$

where K_1 and K_2 are calculated by comparing (4.4) and (4.5) as:

$$K_1 = 1-\omega^2 LC, \qquad K_2 = V\omega C \tag{4.6}$$

for a pattern in phase with the ac mains we have:

$$K_1 = 1\ , \qquad K_2 = 0 \tag{4.7}$$

F is the amplitude of the line current which replaces I in (4.4) and is obtained by the output of the PI in the voltage regulation loop. It is described in s-domain by:

$$F(s) = K_p\left(\frac{1+s\tau}{s\tau}\right) \tag{4.8}$$

where K_p and τ are the gain and time constant of the PI regulator of the voltage loop. The gain of the dc voltage sensor is denoted in Fig. 4.2 by K_v. The compensation scheme is built by producing (4.5) in hardware as depicted in Fig. 4.2. The three modulating signals are then

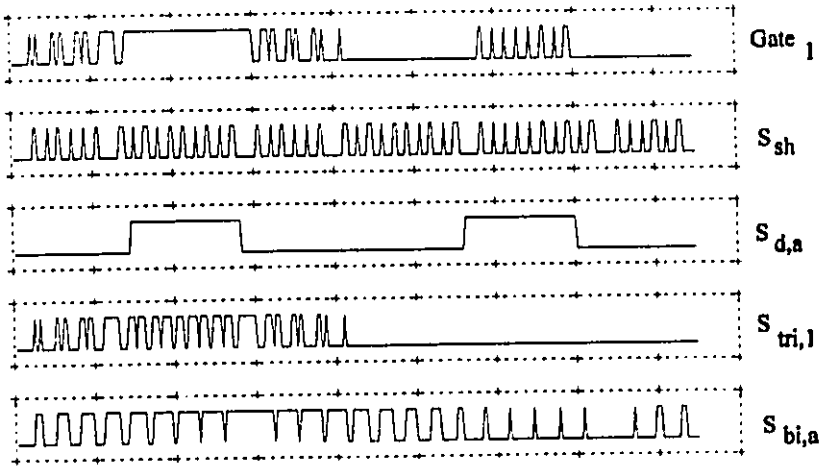

Fig. 4.4 Waveforms of the on-line pattern generator.

passed into an on-line PWM pattern generator. The inputs to the pattern generator are three modulating signals and a triangular carrier waveform. The outputs are six gating patterns for individual switches.

4.3 On-Line Pattern generator

The operation of the on-line PWM pattern generator is based on the following criteria:

- only two switches are conducting at any instant (one top and one bottom switch).
- The required shorting pulses are added to obtain the switch gating signals. These pulses create a dc bus short through one leg of the inverter whenever all top or all bottom switches are open.

A bi-level pattern is first generated by comparing the triangular carrier with the modulating signal:

$$S_{bi,a} = \begin{cases} 1 & if \quad v_{mod,a} \geq carrier \\ 0 & if \quad v_{mod,a} < carrier \end{cases} \tag{4.9}$$

Next, the tri-level switching pattern, $S_{tri,1}$, which produces the expected line current is obtained by combining the two consecutive bi-level patterns, $S_{bi,a}$, $S_{bi,b}$, $S_{bi,c}$:

$$\begin{cases} S_{tri,1} = S_{bi,a} \cap S'_{bi,b} \\ S_{tri,4} = S_{bi,b} \cap S'_{bi,a} \\ \cdots\cdots\cdots\cdots \\ \cdots\cdots\cdots\cdots \\ S_{tri,5} = S_{bi,c} \cap S'_{bi,a} \\ S_{tri,2} = S_{bi,a} \cap S'_{bi,c} \end{cases} \tag{4.10}$$

After obtaining the basic tri-level pattern, it is necessary to add the shorting and overlap pulses to ensure that the dc bus current is never interrupted. The shorting pulse signal, S_{sh}, is derived

by detecting the absence of pulse either in the top or bottom half of the converter:

$$S_{sh} = (S_{tri,1} \cup S_{tri,3} \cup S_{tri,5})' \cap (S_{tri,4} \cup S_{tri,6} \cup S_{tri,2})' \tag{4.11}$$

The interval in which the shorting pulses are applied, is defined by another pulse located in the centre of the conduction interval of the top and bottom switches of a given leg, for example $S_{d,a}$. Then the gating signal of the switch is defined as:

$$Gate_{1} = S_{tri,1} \cup (S_{sh} \cap S_{d,a}) \tag{4.12}$$

The on-line PWM pattern generator ensures equal distribution of shorting pulses to all the switches. Therefore, the resulting line current has quarter-wave and half-wave symmetry. Building signals of the switch gating signals are depicted in Fig. 4.4. The complete circuitry and the operation of the pattern generator are detailed in [68].

4.4 Design of the Regulator

The block diagram for the control system design of the PWM rectifier is shown in Fig.

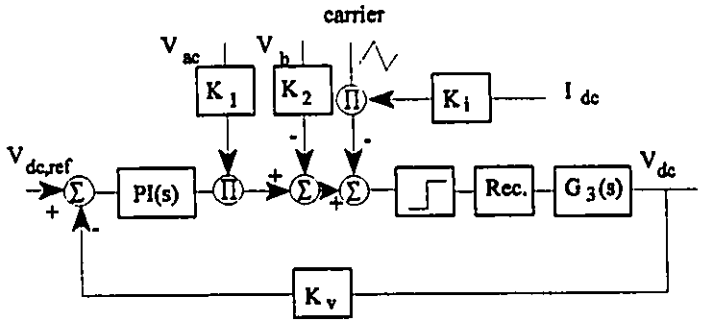

Fig. 4.5 Block diagram of the control circuit.

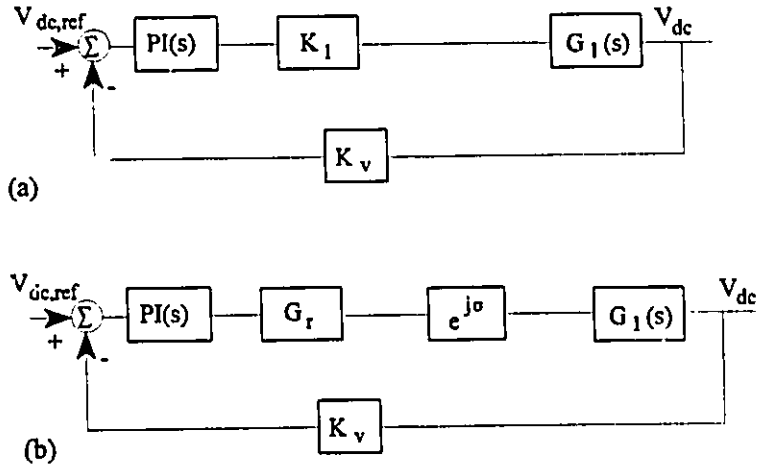

Fig. 4.6 Simplified block diagrams, (a) modulation index control, (b) modulation index and phase shift control.

4.5. The gains of the voltage and current sensors in the block diagrams are denoted by K_v and K_i respectively. The output of the PI regulator dictates the amplitude of the rectifier current. Also, in order to make the loop independent of the output current, the magnitude of the triangular carrier is multiplied by the dc current. Two simplified block diagrams are derived from Fig. 4.5 and are shown in Fig. 4.6. Fig. 4.6.a depicts a simplified version which includes only the effect of modulation index control. $G_1(s)$ is the transfer function from modulation index to output dc voltage which is derived in the Appendix. Therefore, $G_1(s)$ must be replaced by:

$$G_1(s) = \frac{\hat{v}_{dc}(s)}{\hat{m}(s)} \tag{4.13}$$

Fig. 4.6.b includes the effect of phase shift control. The phase shifter is simplified to a phase shift and a gain which is given by:

$$G_r = \frac{K_1 - jK_2}{K_t I_{dco} V_m} \tag{4.14}$$

where V_m is the amplitude of the carrier waveform and I_{dco} is the output dc current for the operating point. The PI regulator is designed with the help of these two block diagrams. Closed loop frequency responses for these two block diagrams are depicted in Fig. 4.7 and Fig. 4.8. In order to verify the validity of these models, time domain simulation of the circuit shown in Fig. 4.1 is performed using PSIM software. Small signal harmonics of various frequency are injected into the dc voltage reference and the closed loop frequency response of the system (both with and without the phase shift) is obtained. The data obtained from these simulation programs are marked on Fig. 4.7 and 4.8 for comparison purposes. It can be seen that the derived small signal models are in close agreement with results obtained from simulation.

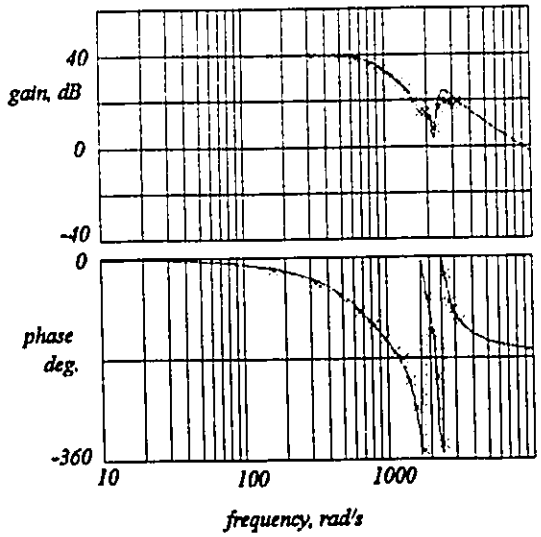

Fig. 4.7 Closed loop frequency response of the overall system, modulation index control, time domain simulation results are included.

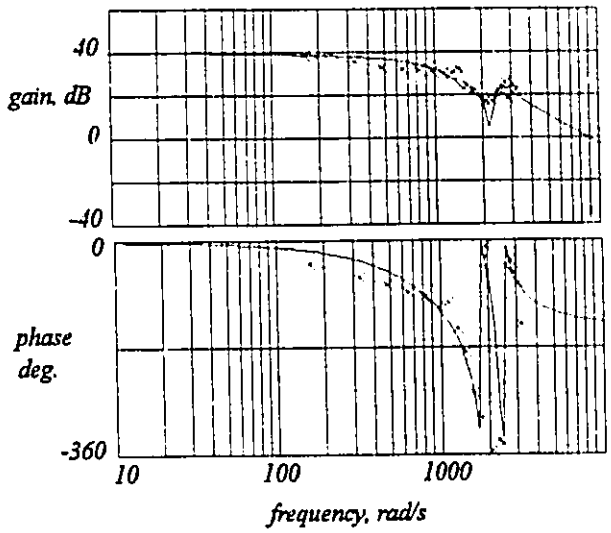

Fig. 4.8 Closed loop frequency response of the overall system, modulation index and phase shift control, time domain simulation results are included.

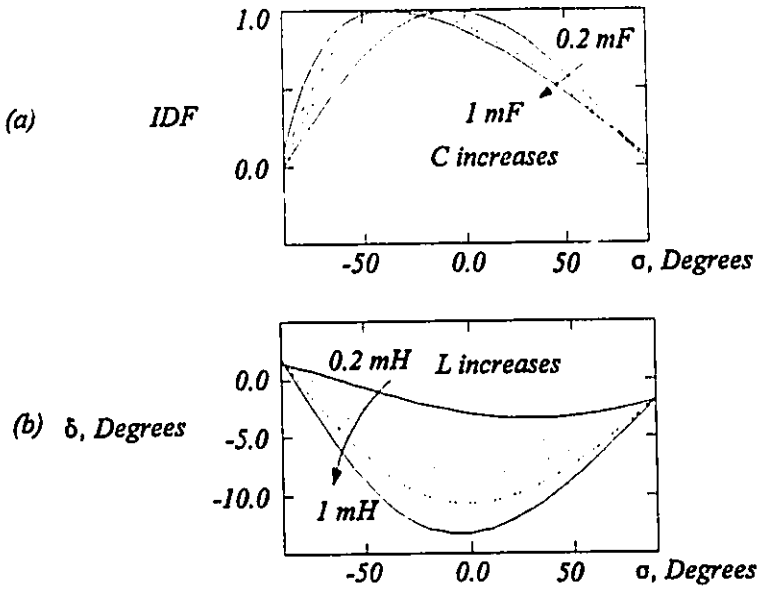

Fig. 4.10 Effect of pattern phase shifting, (a) on the input displacement factor, (C as parameter), (b) on the power angle, (L as parameter), ($M = 1$).

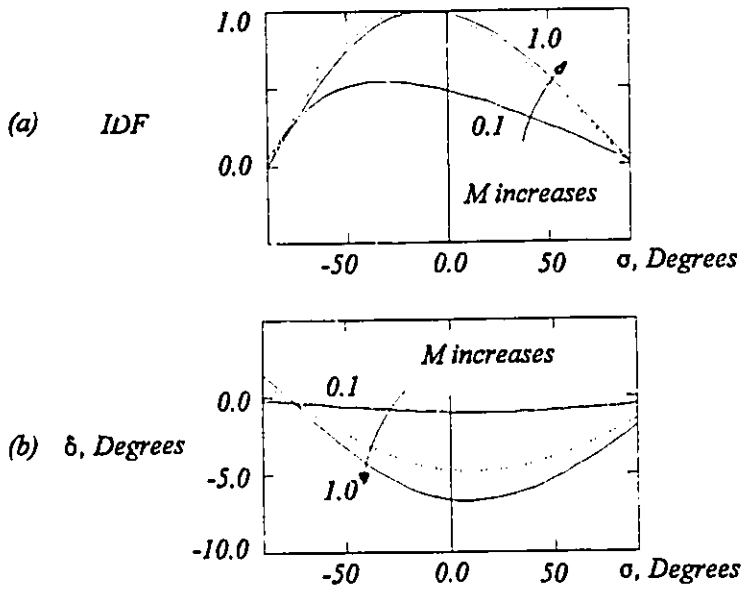

Fig. 4.9 Effect of pattern phase shifting, (a) on the displacement angle, (b) on the power angle. (M as parameter.)

4.5 Limitations of Displacement Compensation

4.5.1 Limitations Based on Filter Components

The compensation of the displacement angle θ is limited by the power circuit components. This can be seen from Fig. 4.3. The reactive component of the rectifier current must compensate for the capacitor current. This means that a minimum rectifier current is required to compensate the var required by the input filter capacitor. This minimum value is given by:

$$I_{rec,\min} = V_{rec}\omega C \tag{4.15}$$

Assuming a constant dc current, (4.15) can be rewritten in terms of the modulation index as:

$$M_{\min} = \frac{2 V_{rec} \omega C}{\sqrt{3} I_{dc}} \tag{4.16}$$

As the above equation suggest, the minimum modulation index is dependent on the filter components. Alternative equations in terms of minimum output voltage or minimum output power can be obtained. In order to quantify the effect of parameter variations, and for a graphic representation the actual IDF must be calculated. Then effect of modulation index, filter capacitance and filter inductance can be independently identified. The control angle (σ) which is generated by the control circuitry is given by:

$$\sigma = \tan^{-1} \frac{-V \omega C}{(1-\omega^2 L C)\ I_{dc} \frac{\sqrt{3}}{2} M} \tag{4.17}$$

Knowing the control angle, the rectifier input current, can be calculated as:

$$\vec{I}_{rec,a} = M I_{dc} \frac{\sqrt{3}}{2} e^{j\sigma} \tag{4.18}$$

where $\rightarrow$ denotes vector representation. From the above equation, the capacitor voltage is obtained as:

$$\vec{V}_{rec,a} = \frac{\vec{V}_a - Z_L \vec{I}_{rec,a}}{1 + \frac{Z_L}{Z_C}} \tag{4.19}$$

where Z_L, Z_C are the line and filter impedances respectively and $\vec{V}_a, \vec{V}_{rec,a}$ are the ac mains and rectifier input voltage vectors respectively. From (4.18), (4.19), the capacitor and line currents

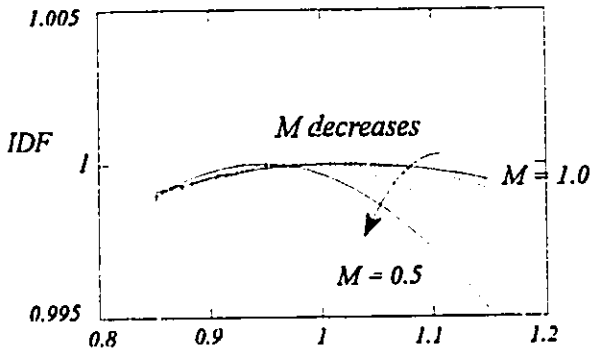

Fig. 4.11 Effect of input voltage variation on IDF.

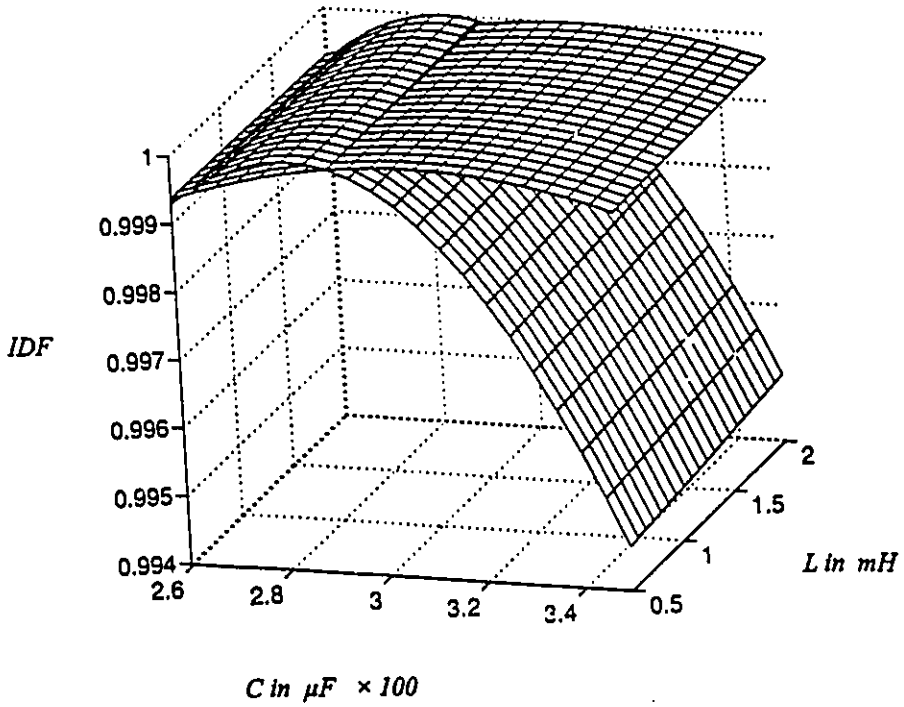

Fig. 4.12 Effect of parameter (L&C) variations on IDF.

are calculated and finally the Input Displacement Factor is obtained from the following:

$$\vec{I}_a = \vec{I}_{C,a} + \vec{I}_{rec,a} \quad , \quad IDF = arg\,(\vec{I}_a) \tag{4.20}$$

where $\vec{I}_a$ and $\vec{I}_{C,a}$ are the input line and capacitor currents of phase a respectively. The Input Displacement Factor is calculated from (4.20) and as a function of the phase shift of the modulating signal (σ) is depicted in Fig. 4.9.a. For high modulation indices, there is always a value for control angle (σ) that obtains unity IDF. But as modulation index decreases, the maximum IDF decreases, (for example for $M = 0.1$, $IDF_{max} \approx 0.5$). Also, shown in Fig. 4.9.b is the power angle (δ) as a function of the phase shift of the modulating signal. A higher line (filter) inductance results in a larger δ. The modulation index is assumed constant, ($M = 1$). Fig. 4.10 shows the effect of filter components. It was seen that the input capacitor has a more significant effect on the input displacement factor, than the input inductor.

4.5.2 Effect of Parameter Variation

The required phase shift for unity power factor operation is calculated from (4.5) with the assumption of a constant ac mains voltage. Therefore, the ac bus variation affects the IDF. The effect of this amplitude variation however, is minimal as shown in Fig. 4.11. From this figure it is concluded that overvoltages have more effect than ac undervoltages. Also, as expected the effect is more significant as the modulation decreases.

Since K_1 and K_2 are dependent on the filter components, the control scheme is parameter sensitive. However, large variations in L and C ($\pm$ 15%) results in only 1% change in the IDF, Fig. 4.12. The effect of parameter variation on IDF is more pronounced as the modulation index decreases. The two surface plots shown in Fig. 4.12 correspond to M=1 and

M=0.5. From this graph one can conclude that the filter inductance has little effect on IDF, especially for low modulation values.

4.6. Results

4.6.1. Steady State and Transient Response

Simulation results obtained from PSPICE program for a PWM rectifier with the dc voltage regulation loop are shown in Fig. 4.13. Since, no compensation scheme for input displacement factor is used, the line current has a phase displacement with respect to the ac source. The output dc voltage is varied, so the effect of modulation index on the input displacement angle (θ) can be seen. The PWM rectifier with the same components was simulated with the proposed compensation scheme in place. From the results depicted in Fig. 4.14, it can be seen that near unity displacement factor is achieved for different modulation indices. Also, the response to the transients is very fast, due to the on-line pattern generation. Fig. 4.15 shows the variation of the input displacement factor as a function of output dc voltage (a) and output dc current (b), obtained from simulation results. The effectiveness of the proposed compensation scheme for a wide range of load conditions is confirmed by Fig. 4.15.

4.6.2. Experimental Results

In order to prove the feasibility and effectiveness of the proposed feed-forward scheme, a laboratory prototype was built. Table 4.1 includes the component values and specifications of the prototype. Steady state input phase voltage and current are shown in Fig. 4.16. Unity displacement power factor is achieved. A step change is applied to the output dc voltage reference and the input line current and voltage under this transient condition are depicted in Fig. 4.17. The speed of response to the dc transients is limited by the output dc filter.

Table 4.1 Design example.

output (rated)	P_{dc} = 990 W, V_{dc} = 100V
input (rated rms values)	V_a = 60V, I_a = 5.5A
sensor gains	$K_v = K_i = 0.01$
PI parameters	$K_p = 0.2$, $\tau = 0.005$ s
input filter	L = 3 mH, C = 50 μF, R_f = 2.5Ω
output filter	L_{dc} = 5mH, C_{dc} = 800μF, R_{dc} = 10Ω

4.7 Conclusions

A new compensation scheme for Input Displacement Factor of three-phase PWM buck rectifier is proposed. The method is simple and requires minimum hardware, since it uses the standard dc voltage loop and a feed-forward dc current path without any additional transducer. Unity IDF is achieved by phase shifting the modulating signals according to the converter operating point. Small signal models are derived and used for design of the regulators and effects of circuit parameters and ac bus variations on the proposed scheme are studied. Experimental results on a 1kVA laboratory prototype shows that compensation scheme is effective for various load conditions.

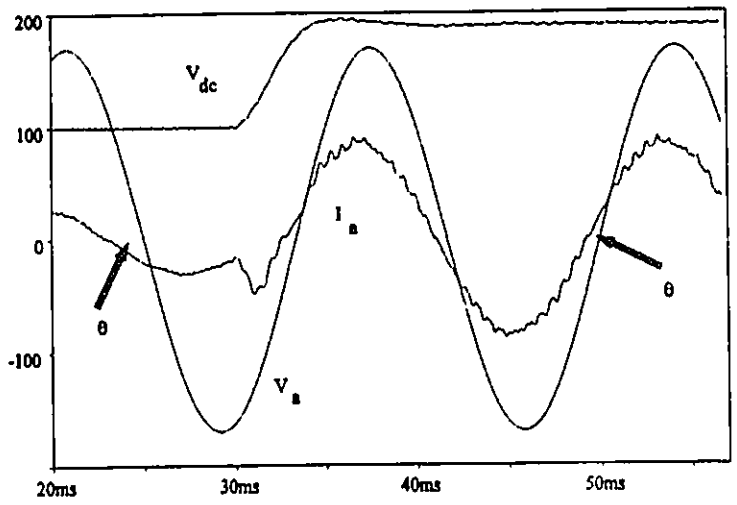

Fig. 4.13 PWM rectifier without displacement compensation. Output dc voltage V_{dc}, input line current I_a, input phase voltage V_a.

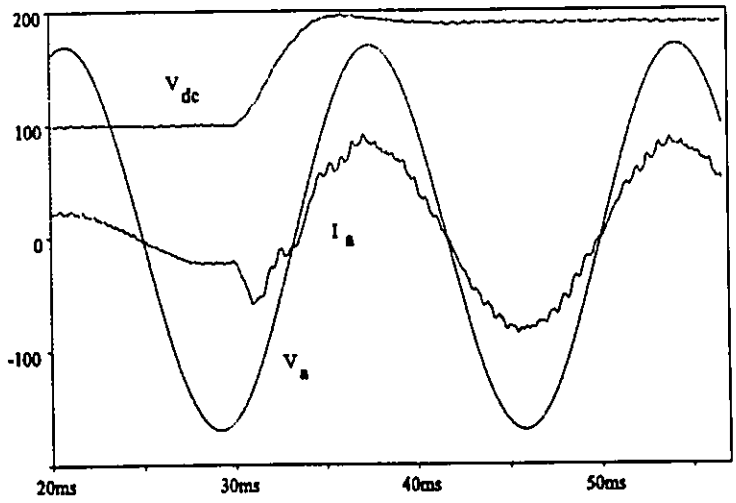

Fig. 4.14 PWM rectifier with displacement compensation. Output dc voltage V_{dc}, input line current I_a, input phase voltage V_a.

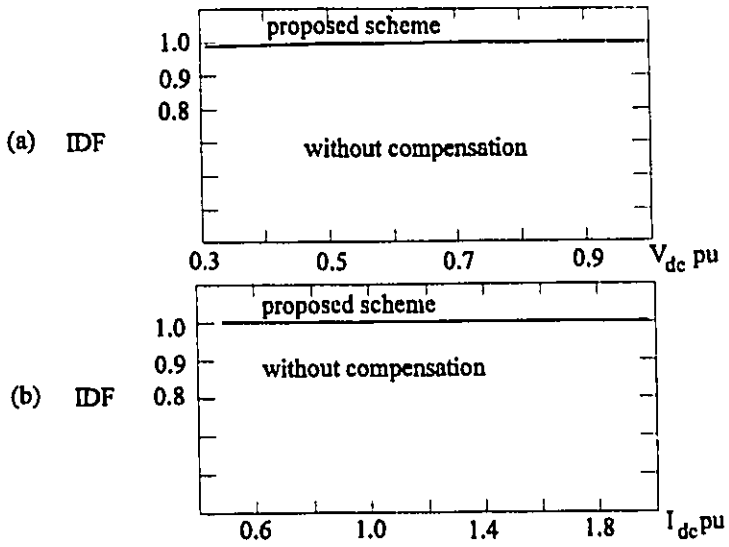

Fig. 4.15 IDF with and without compensation, (a) output voltage variation, (b) output load variation, V_{dc} = 190V.

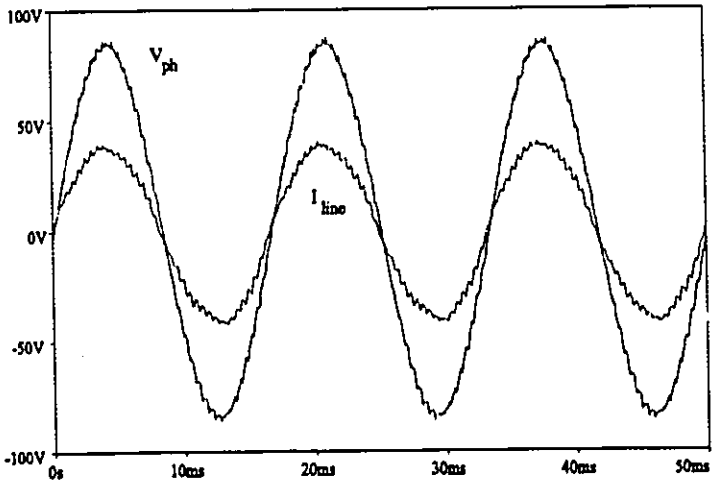

Fig. 4.16 Experimental result, steady state input voltage and line current(X5).

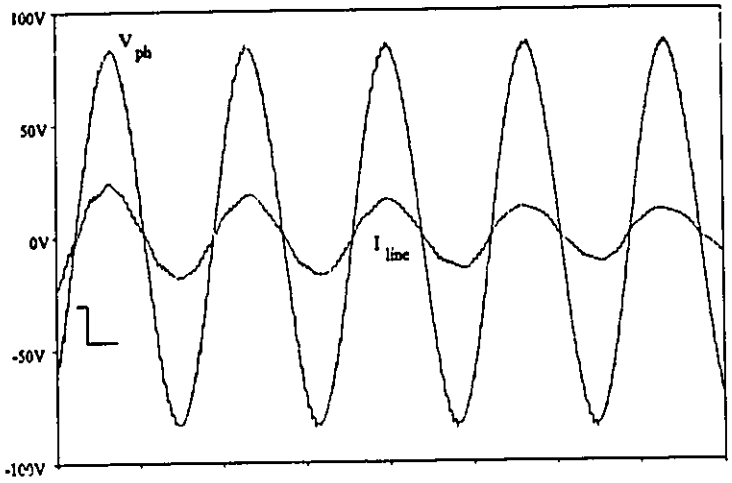

Fig. 4.17 Transient response. Input phase voltage and line current.

CHAPTER 5

AN ON-LINE OPERATED UNITY POWER FACTOR PWM RECTIFIER WITHOUT PASSIVE DAMPING REQUIREMENTS

5.1 Introduction

Drawbacks of the conventional off-line operated PWM rectifiers include slow transient response, load dependent input power factor and the need for damping resistors to avoid harmonic amplification and current oscillations, particularly under transient conditions. In this chapter, an on-line operated PWM rectifier is proposed with a new modulation scheme which uses the voltages across the input filter capacitors as templates. This results in the following improved features: (a) inherent synchronization with the ac mains; (b) inherent damping without the need for damping resistors; (c) fast self starting capability and (d) excellent transient response. Moreover, the phase-shifting technique proposed in ***chapter 4*** is adapted to achieve unity power factor, independently of the dc link current variations. A current feedback loop regulates the dc link current according to the load demands. The chapter includes the performance investigation of the proposed rectifier under various input conditions such as dc transients, ac bus transients and unbalanced input voltages. Experimental results on a 1 kVA laboratory prototype confirm the feasibility of the proposed control structure.

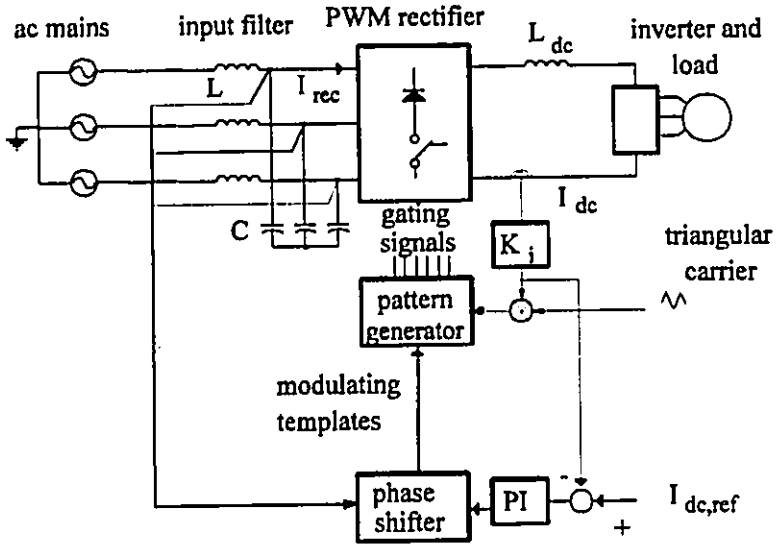

Fig. 5.1 The proposed PWM rectifier circuit.

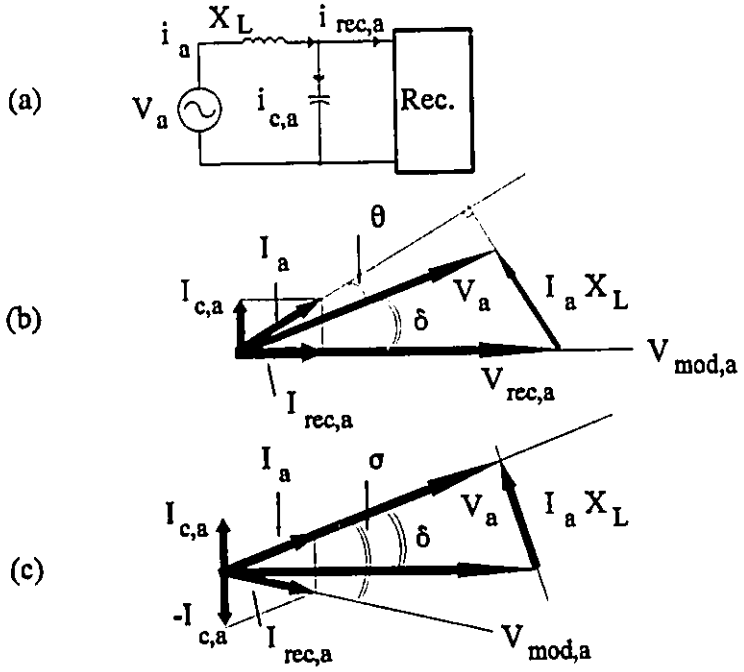

Fig. 5.2 (a) Single line diagram, (b) non-unity displacement factor operation (leading power factor), (c) unity displacement factor operation (θ=0).

5.2 Description of the Proposed Rectifier

The complete rectifier system, Fig. 5.1, includes an on-line PWM pattern generation scheme with a dc bus current regulation loop and a phase-shifting circuitry for unity power factor operation.

5.2.1 Pattern Generation Scheme

The proposed pattern generation scheme is shown in Fig. 5.1. The three capacitor voltages are chosen as the modulating signals and the damping resistors are completely eliminated. Small signal analysis presented in the Appendix confirm that choosing the capacitor voltages as the modulating signals results in a properly damped system. The amplitudes of the modulating signals are varied according to the output dc current requirements. The waveforms are then compared to a triangular carrier to obtain the switching pattern. The gatings of the individual switches are obtained by first producing the line-to-line switching pattern and then adding proper short-circuit pulses to ensure a path for the flow of dc inductor current. The pattern generator was described in ***chapter 4***.

5.2.2 Phase-Shifting Circuitry

The phase shifting concept was explained in ***chapter 4***. However, in this case since the modulating signals are constructed from the capacitor voltages, the reference point is the capacitor voltage of phase (a) and the equation describing the modulating waveform is slightly changed. Choosing the capacitor voltage as reference, for unity displacement factor operation, from Fig. 5.2.c one obtains:

$$v_{rec,a}(t) = V_{rec} \sin \omega t \qquad (5.1)$$

$$v_a(t) = V\sin(\omega t - \delta), \quad i_a(t) = I\sin(\omega t - \delta) \tag{5.2}$$

where δ is the phase shift between the capacitor voltage and ac mains and is given by:

$$\sin\delta = \frac{-\omega LI}{\sqrt{V^2 + (\omega LI)^2}} \tag{5.3}$$

In order to calculate the position of the modulating signal, the steady state rectifier input current must be calculated. This is given by:

$$i_{rec,a}(t) = I\cos\delta\sin\omega t - (I\sin\delta + \omega CV_{rec})\cos\omega t \tag{5.4}$$

Now, if the angle δ is small ($\omega LI << V$), it can be approximated by:

$$\cos\delta = 1, \quad \sin\delta = \frac{-\omega LI}{V} \tag{5.5}$$

The rectifier current is given by:

$$i_{rec,a}(t) = I\sin\omega t - (V_{rec}\omega C - \frac{\omega LI^2}{V})\cos\omega t \tag{5.6}$$

The modulating signal should generate a rectifier current equal to (5.6). The current amplitude (I) can be obtained from the output of the PI regulator. However, the term (I^2) requires an additional multiplier which results in noise problems. Therefore, this term is approximated by:

$$I^2 \approx 2kI_oF \tag{5.7}$$

where I_o is the rated value of output dc current and F is the current amplitude obtained from

the output of the PI regulator. Performance investigations have shown that a factor of $k = 0.5$ gives the best overall power factor correction results. The error generated due to approximations remains small as long as the dc operating point does not increase significantly above the rated value I_o. This error is less than 5° for the entire operating range, Fig. 5.3.b. The transfer function of the PI regulator and is given by:

$$PI(s) = K_p \frac{\tau s + 1}{\tau s} \tag{5.8}$$

where K_p and τ are the gain and the time constant of the PI regulator respectively. The line-to-line modulating signal can be obtained from the capacitor voltages and the output of the PI regulator, as follows:

$$v_{mod,ab}(t) = F \sin \omega t - \left[V_c \omega C - \frac{\omega L (I_o F)}{V} \right] \cos \omega t \tag{5.9}$$

The phase modulating signal is obtained by phase shifting (lagging) the sine and cosine signals in (5.9) by 30°. The phase modulating signal can then be written as:

$$v_{mod,a}(t) = F(\sin(\omega t - \frac{\pi}{6}) + K_1 \cos(\omega t - \frac{\pi}{6})) - K_2 \cos(\omega t - \frac{\pi}{6}) \tag{5.10}$$

where K_1 and K_2 are:

$$K_1 = \frac{\omega L I_o}{V}, \qquad K_2 = V_{mc} \omega C \cong V \omega C \tag{5.11}$$

V is the amplitude of the phase voltage (assumed constant). The triangular carrier must be multiplied by the output current. Generation of (5.10) in hardware is shown in Fig. 5.4. In order to normalize the modulating signal (5.10), the triangular carrier must be multiplied by the

output current.

5.3 Filtering Requirements Of Modulating Signals

Since the capacitor voltages are used as the modulating signals, their harmonic contents contributes to the generation of additional harmonics of new frequencies, amplitude remains

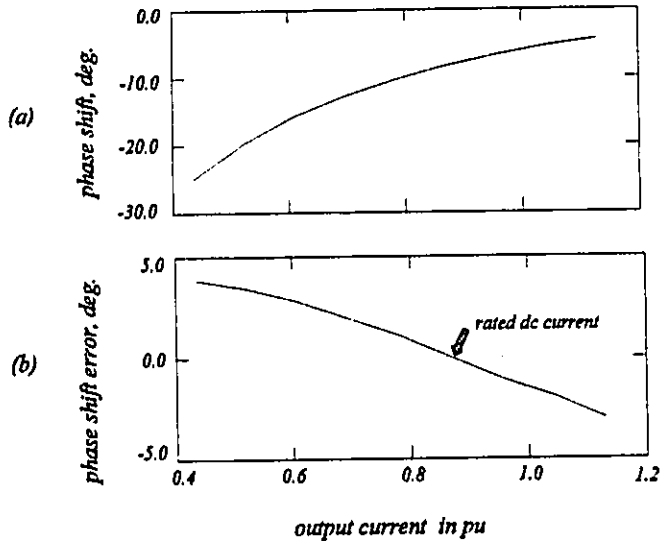

Fig. 5.3 (a) Generated phase shift, (b) generated error due to the approximation used.

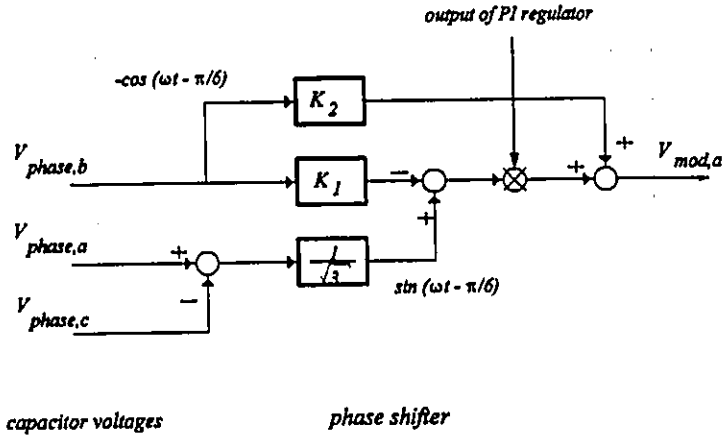

Fig. 5.4 Generation of modulating signal for phase *a*.

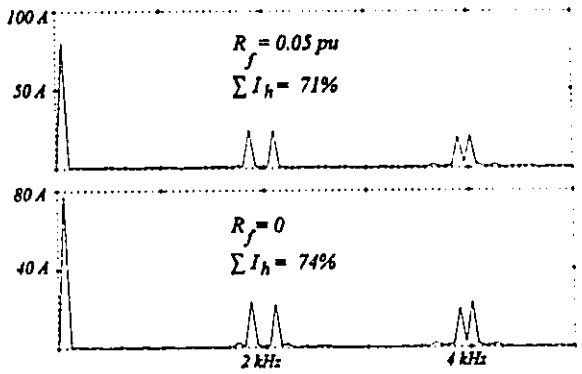

Fig. 5.5 Frequency spectrum of rectifier input current, (a) conventional scheme, (b) proposed scheme.

small (less than 2% increase in individual harmonics amplitudes, Fig. 5.5). Therefore, the question is to determine whether the effect of these additional harmonics is significant. Studies show that there is no need for additional filtering when the converter is operating in the rectification mode. However, for the regenerative mode of operation, the capacitor ripple constitutes a positive feedback through the control circuit and this results in an unstable operation (note that there is no damping resistor in the circuit). Therefore, it is necessary to provide a filter in the control circuitry. This filter is bypassed during rectification. The filter for phase (a) is shown in Fig. 5.6. A first order filter is sufficient. The filter break frequency is set close to that of the input LC filter. The dc voltage is sensed, filtered and multiplied by (-1) and is used to control a switch. During regeneration the output dc voltage reverses polarity, the control switch is gated and the filter capacitor branch is connected. Otherwise the output dc voltage is positive and the filter is disconnected.

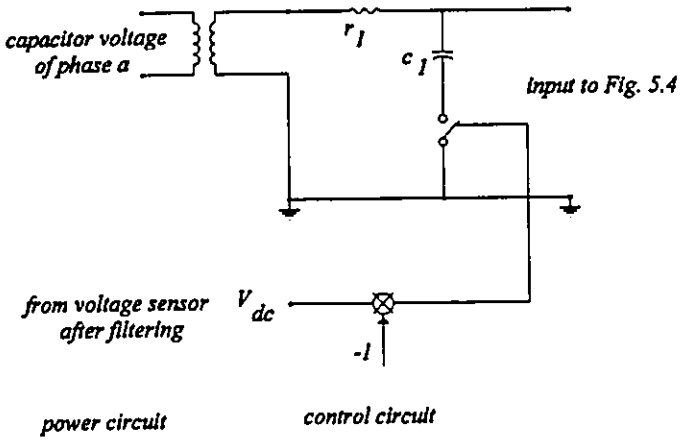

Fig. 5.6 Filtering of modulating signal of phase *a*.

Table 5.1 Steady state results.

Base values:	V_{rms} = 120 V, I_{rms} = 69.4 A, f = 60 Hz		
power circuit:	X_L = 0.1 pu, X_C = 5.1 pu, X_{Ldc} = 1.1 pu, R_{dc} = 1.1 pu		
control circuit:	K_p = 0.2 pu, τ = 0.5 mS, K_v = 0.01, f_{sw} = 27 pu		
		conventional	proposed
Balanced inputs	input power	0.823	0.765
	output power	0.73	0.73
	input kVA	0.846	0.766
	Power Factor	0.973	0.998
	relative efficiency	86.6%	95.4%
Unbalanced inputs	input power	0.829	0.78
	output power	0.734	0.745
	input kVA	0.0.869	0.787
	Power Factor	0.954	0.991
	relative efficiency	88.5%	95.5%

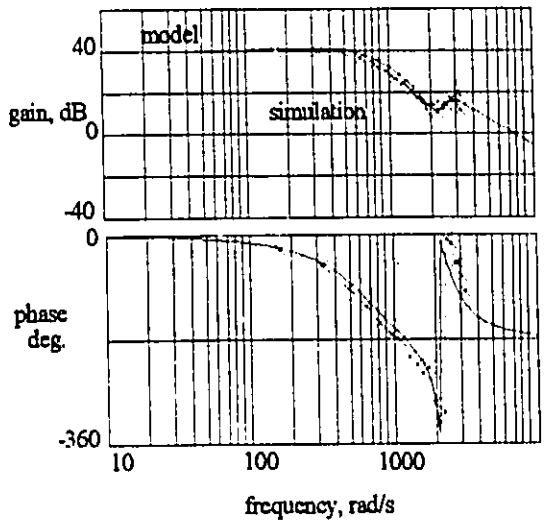

Fig. 5.7 Closed loop frequency response of the overall system (modulation index control, same circuit parameters as ***chapter 4***, $R_f = 0$).

5.5 Design Guidelines

The design of the PWM rectifier involves the design of the input/output filters and the PI regulator. The input/output filters are designed to limit the THD of the input waveforms and the ripple of the output current to acceptable values. The PI regulator components are the same as those in ***Chapter 4***. The frequency response of the closed loop system is shown in Fig. 5.7. By comparing Fig. 5.7 with Fig. 4.8, one can conclude that the proposed modulation scheme results in higher damping and therefore the damping resistors can in fact be eliminated. Additional figures for comparison purposes are included in the Appendix. The data obtained from time domain simulation (marked on the figure) confirm that the small signal model is valid and therefore can be used for accurate design of the regulators. The design example parameters

used for simulation are specified in Table 5.1.

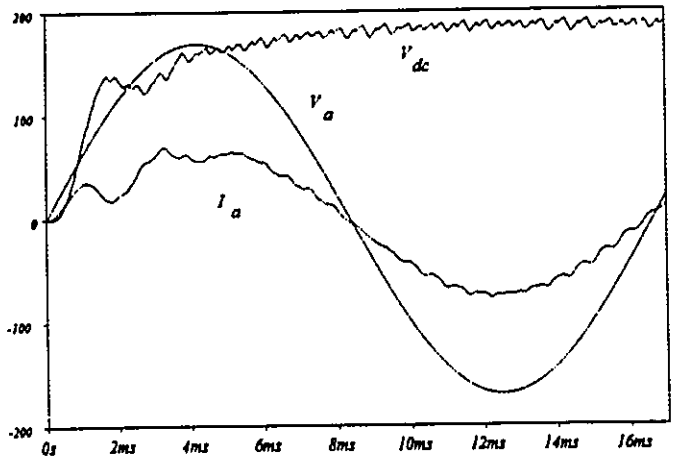

Fig. 5.8 Start up, proposed scheme with IDF compensation, output dc voltage V_{dc}, line current I_a, phase voltage V_a.

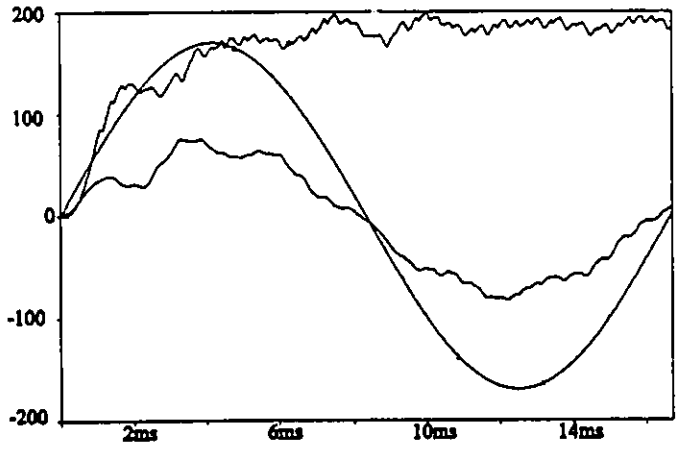

Fig. 5.9 Start up, conventional scheme with IDF compensation.

5.5 Operating Characteristics

5.5.1 Simulation Results

5.5.1.1 Start Up and Steady State

The PWM rectifier with capacitor voltage reference is more immune to oscillations and reaches the steady state faster than the rectifier with pattern generated from the ac mains, compare Fig. 5.8 and Fig. 5.9 (IDF compensation scheme was included). The oscillations are more apparent in the output dc voltage. It was noted that if the output dc capacitor is present, these oscillations increase and the line currents will reach steady state in 2-3 cycles. The proposed rectifier has a higher relative efficiency since the damping resistors are eliminated (Table 5.1). The term relative efficiency is used, since the switches are assumed to be ideal and switching losses are neglected. The damping resistor used for the conventional scheme is 0.14 pu.

5.5.1.2 DC Transients

The output dc current reference is increased from 50A to 100A (voltage changes from 95V to 190V) and the response of the system is depicted in Fig. 5.10. The proposed rectifier exhibits excellent transient response. The power factor remains close to unity (0.998) independently of load variations.

5.5.1.3 Effect of Line Transients

Due to the other loads connected to the Point of Common Coupling (PCC), capacitors may be needed for var compensation, Fig. 5.11. Voltage oscillations which appear on the ac bus during switching of these capacitors may affect the performance of the rectifier. Effect of

these switching transients at PCC with typical voltage oscillations is shown in Fig. 5.12. Despite the oscillations on the ac bus, the rectifier performance is satisfactory and the phase shifter retains unity power factor after the first cycle. Also, the voltage spike on the dc bus at the input of the inverter is less than 20%.

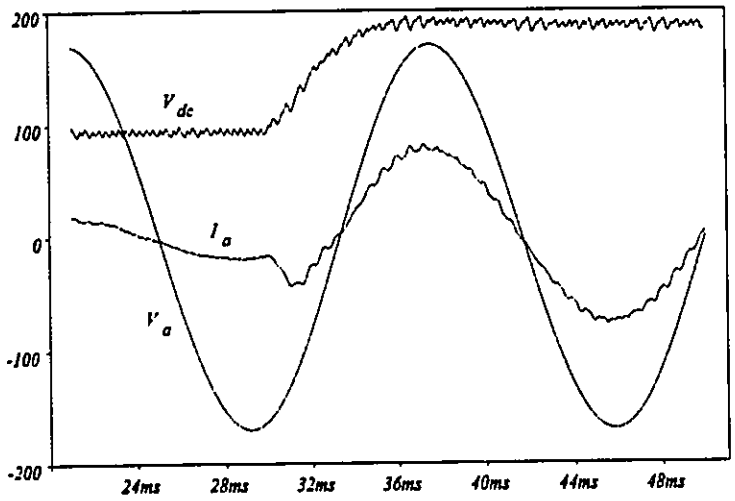

Fig. 5.10 DC transients, output dc voltage and input line current and voltage are shown.

5.5.1.4. Regeneration

A negative voltage source is connected to the dc bus to simulate the regeneration mode. The voltage reversal is done in 1/3 of a cycle by adding a negative voltage source at the output terminal. As it was mentioned before, when the output dc voltage reverses, the capacitor voltages are passed through the three first order filters. The results are depicted in Fig. 5.13. The steady state is reached in less than two cycles. At the beginning of the voltage reversal period, the dc link current builds up to almost twice its original value.

5.5.1.5 Operation with Unbalanced Input Voltages

A set of input voltages on the ac bus containing 15% negative sequence components

is considered. The input voltages are given as:

$$\left\{ \begin{array}{l} v_a(t) = 1.15\,V\sin\omega t \\ v_b(t) = V\sin(\omega t - \frac{2\pi}{3}) + 0.15\,V\sin(\omega t + \frac{2\pi}{3}) \\ v_c(t) = V\sin(\omega t - \frac{2\pi}{3}) + 0.15\,V\sin(\omega t - \frac{2\pi}{3}) \end{array} \right\} \qquad (5.12)$$

If the input line inductors are neglected, the same unbalancies appear across the capacitor voltages which are used as the modulating signals. These unbalanced modulating signals result in unbalanced rectifier input currents. The frequency spectra of the input/output waveforms for the proposed scheme are shown in Fig. 5.14 It can be seen that with this set of unbalanced currents more power is transferred to dc bus than with a set of balanced currents such as generated from off-line PWM patterns (compare Fig. 5.14 and Fig. 5.15), (Table 5.1). The second harmonic component of the output dc voltage is 75% larger for the proposed rectifier than that of the rectifier with balanced pattern. Therefore, the value of the input/output filter inductor must be increased to obtain similar dc current ripple. The phase shifter generates line currents which are in phase with the corresponding phase voltages. The overall PF is higher than for the rectifier with off-line pattern (Table 5.1).

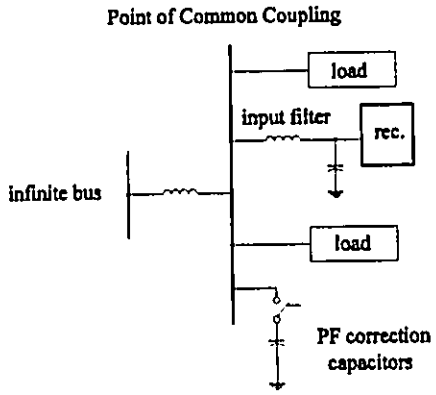

Fig. 5.11 Typical connection of rectifier and other loads to ac bus.

5.5.1.6 Non-Regenerative Applications

In this case the output loop is replaced by a voltage loop and the power circuit is similar to that of ***Chapter 4***. The dc transients for non-regenerative applications is shown in Fig. 5.16.

5.5.2 Experimental Results

A 1 kVA rectifier system is operated with the proposed control scheme. The damping resistors are completely eliminated and the phase shifter is implemented to achieve unity power factor operation. The specifications of the experimental set up are given in Table 5.2. The two components of the modulating signal are depicted in Fig. 5.17. The sine waveform in Fig. 5.17 is obtained from the output of multiplier and incorporates the effect of load operating point. The cosine component in Fig. 5.17 has a fixed amplitude and therefore becomes more effective for low modulation indices resulting in PF close to unity. The steady state input current and voltage are shown in Fig. 5.18. The rectifier performance is satisfactory as expected. The steady state results for the non-regenerative circuit are shown in Fig. 5.19. The input line current, phase voltage and the phase modulating signal which is a duplication of the input filter

Table 5.2 Experimental set up components.

rms rated values	V_a = 60 V, I_{dc} = 10 A, P_{dc} = 900 W
input filter	L = 3 mH, C = 50 μF
output filter	L_{dc} = 6 mH, R_{dc} = 9Ω

capacitor voltage are shown.

5.6 Conclusions

An on-line operated PWM rectifier is proposed which generates the PWM pattern using a template obtained from the capacitor voltages. The theoretical considerations, confirmed by experimental results on a 1 kVA laboratory prototype, show that the PWM pattern generation scheme features inherent ac synchronization and effective damping, self-starting capability and fast and oscillation-free transient response. The phase shifting circuitry maintains the line current in phase with the phase voltage and therefore results in unity displacement factor operation. The chapter includes the study of rectifier performance under various transient and fault conditions.

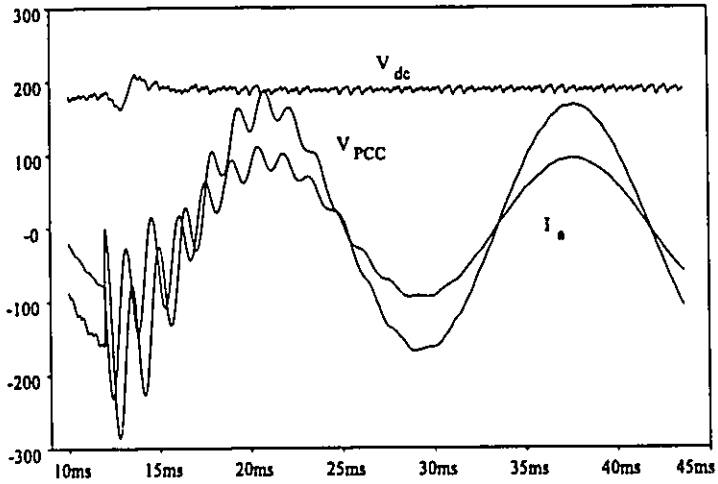

Fig. 5.12 Line transients, dc voltage V_{dc} , voltage at PCC V_{PCC} and line current I_a.

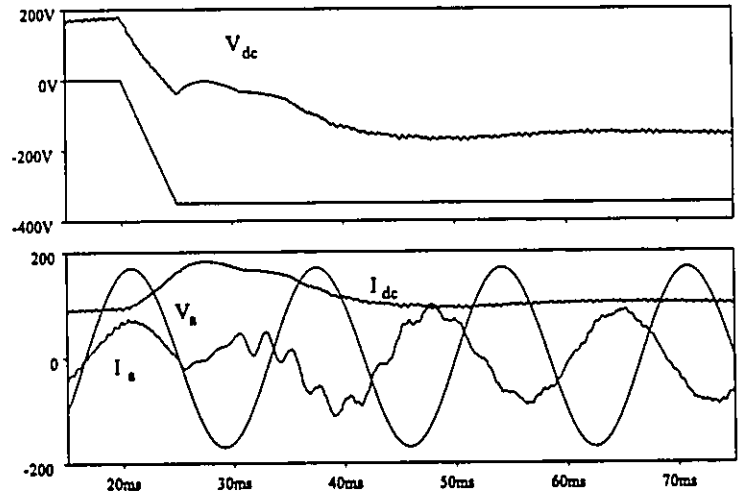

Fig. 5.13 Regeneration, (a) output voltage $V_{dc,}$ (b) output dc current I_{dc}, input line current I_a and voltage V_a.

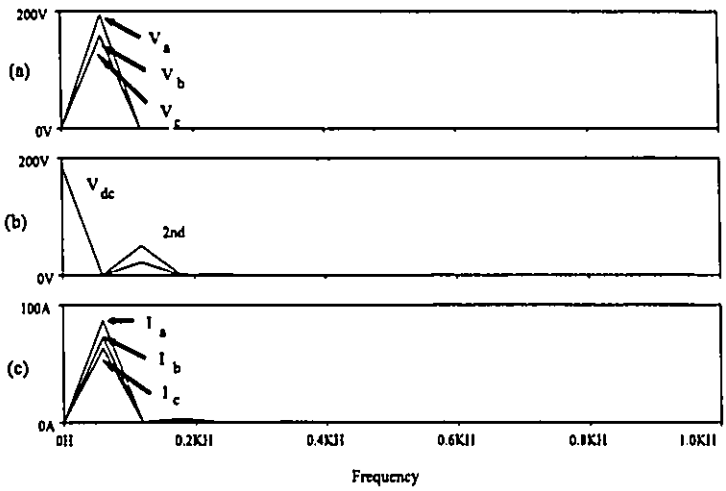

Fig. 5.14 Proposed scheme, (a) unbalanced input voltages, (b) output dc voltage before and after filtering, (c) line currents.

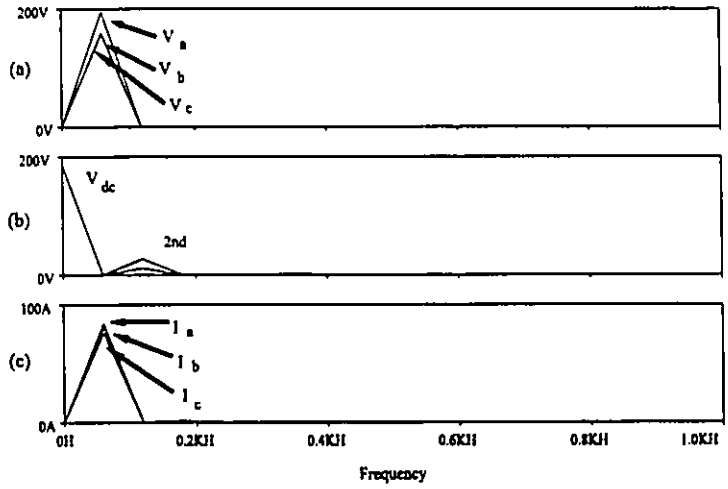

Fig. 5.15 Balanced pattern, (a) unbalanced input voltages, (b) output dc voltage before and after filtering, (c) line currents.

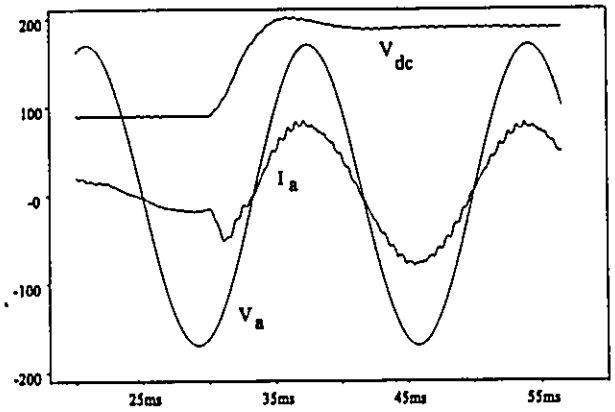

Fig. 5.16 Transient response for non-regenerative topology, output dc voltage, V_{dc}, input line current I_a, and input ac voltage, V_a.

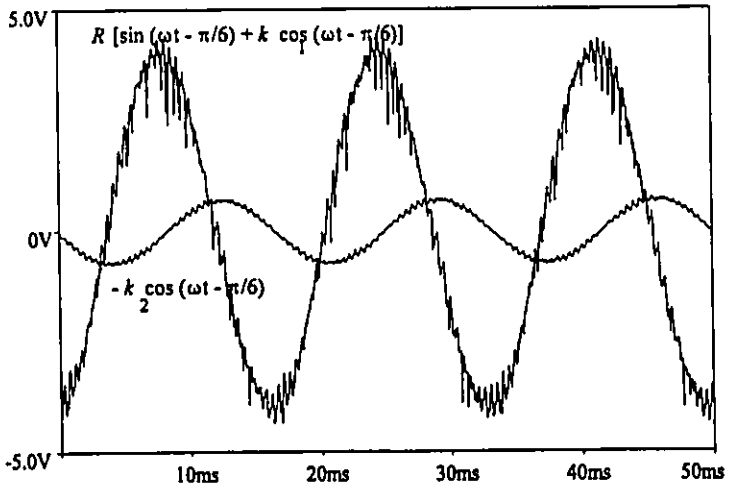

Fig. 5.17 Experimental results, components of the modulating signal.

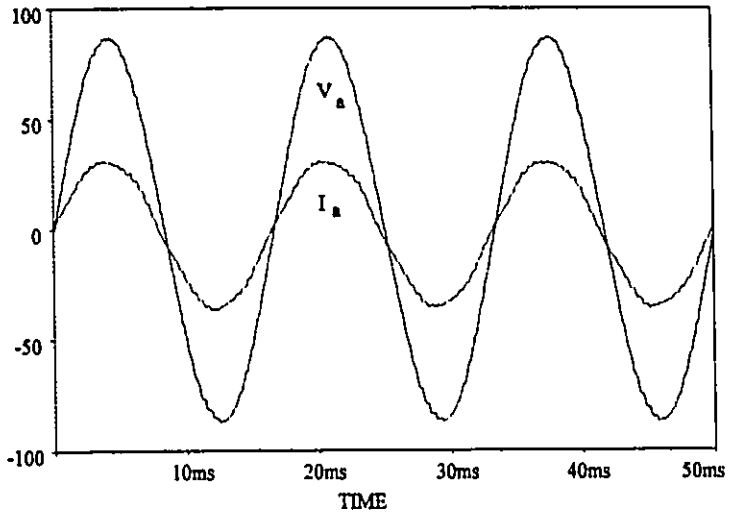

Fig. 5.18 Experimental results, steady state waveforms (I_a X 5).

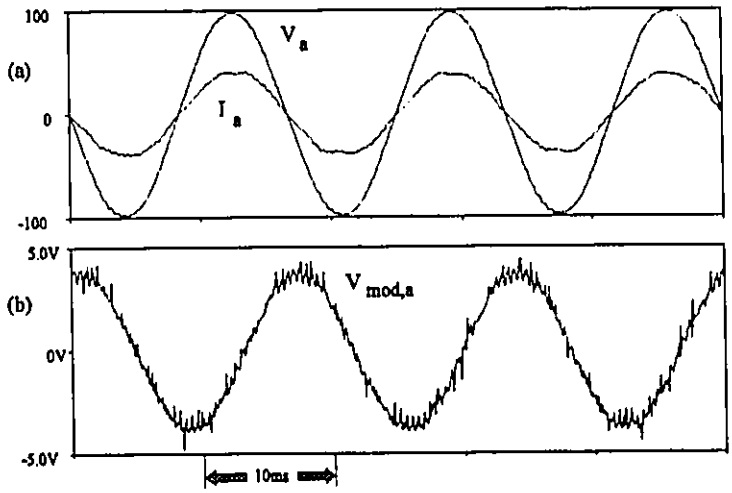

Fig. 5.19 Experimental results for non-regenerative topology, (a) input line current and phase voltage, (b) modulating signal of phase (a).

CHAPTER 6

A CURRENT-CONTROLLED CURRENT SOURCE UNITY POWER FACTOR PWM RECTIFIER

6.1 Introduction

In previous chapters, the current source PWM rectifier was operated by feed-forward techniques. This chapter investigates closed loop control of the input line currents as an alternative to achieve unity IDF operation. The three input line currents are controlled to obtain sinusoidal currents with low oscillations during transients and unity IDF operation independently of load/input parameters variations. Furthermore, output dc voltage is regulated by varying the amplitudes of the ac input current references. The proposed current-controlled PWM rectifier exhibits excellent steady state operation and good transient dynamics. Three types of controllers are implemented in the current loop: Proportional-Integral (PI), Proportional-Integral-Derivative (PID) and Neural Network (NN) based controllers. This later type of controller, which is radically different from the conventional linear controllers (PI and PID), has been investigated for the following reasons: (a) the rectifier is non-linear and of high order which makes modelling using standard small perturbation techniques difficult, (b) because of the non-linear nature of the rectifier, the use of a standard controller does not yield optimum performance for all operating points. NN controllers, by their nature, do not require controller design and are capable of handling non-linearities. Therefore, an elementary and well known NN implementation has been investigated as an alternative to standard controllers.The performances of these controllers are compared. Analysis of the PWM rectifier and control circuitry is given and design guidelines are discussed. Theoretical results and design equations

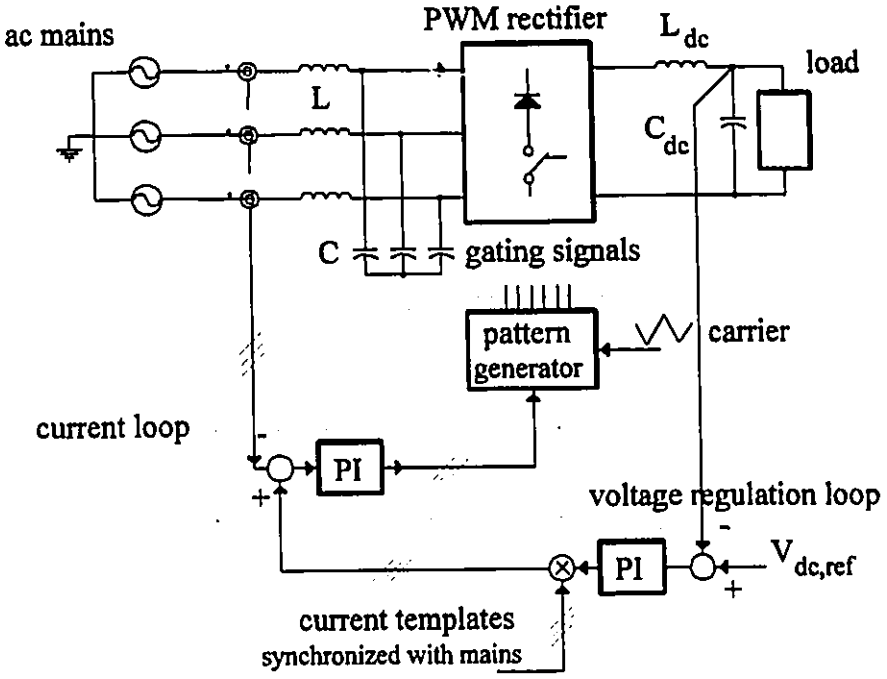

Fig. 6.1 Proposed current controlled PWM rectifier.

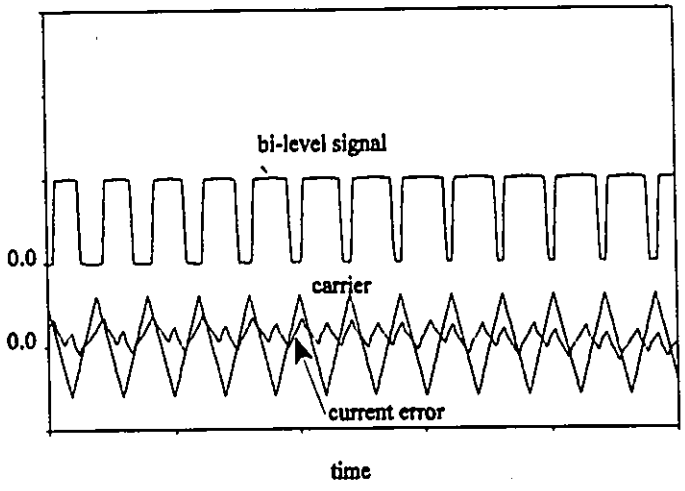

Fig.6.2 Principles of operation of the current control technique.

are verified by simulation and some experiments on a 1.5 kVA prototype unit.

6.2. Proposed Control Scheme

The proposed current-controlled PWM rectifier is shown in Fig. 6.1. The control scheme includes an inner current loop, an external dc voltage/ (current) regulation loop and the on-line PWM pattern generator.

6.2.1 Current Control Loop

The role of the current loop is to obtain sinusoidal line currents with unity displacement factor irrespective of load/input variations. Also, the oscillations of the input currents due to the variation of the dc output voltage reference are suppressed by this loop. As can be seen from Fig. 6.1, the sinusoidal shape of the input currents and the proper phase shift is dictated by the current templates which are in phase and synchronized with the ac mains. The current control is based on ramp comparison technique. The actual line current is compared with a sinusoidal reference waveform and the error is input to a current regulator (PI, PID or NN based), (in case of the NN based controller, the control circuitry is slightly different and is discussed in a later section). The outputs of the three current regulators and a triangular carrier waveform are then input to the on-line pattern generator which was described in ***Chapter 4***. The outputs of the PI regulators are compared with the triangular carrier. If intersections are available, a gating pattern (as in Fig. 6.2) is obtained which forces the current error to remain within the band defined by the amplitude of the triangular waveform (Fig. 6.2). This results in constant switching frequency and low harmonic distortion in the current.

6.2.2 DC Voltage/Current Regulation Loop

The amplitudes of the line current reference waveforms are varied by implementing a

dc voltage/current regulation loop. In this chapter the rectifier is designed as a non-regenerative topology, therefore a dc capacitor exists in the dc side, Fig. 6.3.a. The dc output voltage is compared with a voltage reference and the error is fed to a PI regulator. The output of the PI is multiplied by the current template waveforms to vary the amplitudes of the current references, Fig. 6.1. If the rectifier is used as a front-end for ac drive applications with regenerative capability, a dc current regulation must be used. In that case the output dc capacitor must be eliminated and the output voltage can be made negative, hence operating in the regeneration mode (positive current, negative voltage). The adjustments for a current regulation loop are shown in Fig. 6.3.b.

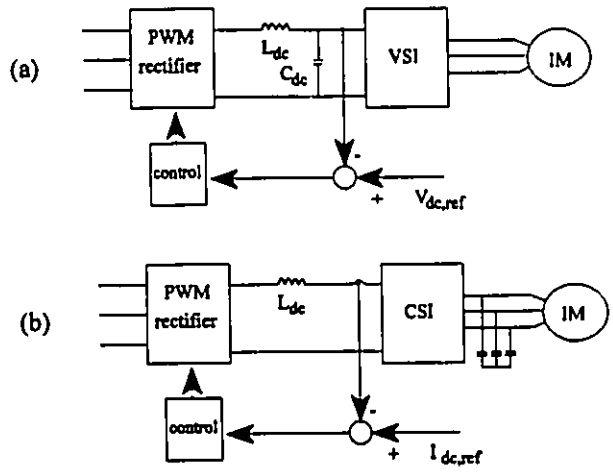

Fig. 6.3 DC voltage/current regulation loops, (a) VSI drive without regeneration capability, (b) CSI drive with regeneration capability.

6.2.3 On-Line PWM Pattern Generator

The operation of the on-line PWM pattern generator was described in detail in *Chapter*

4. The only difference here is that the three modulating signals are generated by the current controller and their amplitude is dictated by the dc regulation loop. The current templates are in phase with the ac mains to achieve unity power factor, however if desirable the rectifier can operate with lagging/leading power factors. The limitations on the input power factor are the same as those discussed in ***chapter 4***.

6.3 Analysis And Design Guidelines

6.3.1. Power Circuit Design

The input and output filters are designed to achieve desired input current THD and output voltage ripple. If an off-line pattern is used to control the PWM rectifier, the harmonics will be amplified/ attenuated according to the filter current transfer function. Therefore, there is a possibility of oscillation of harmonics around the filter break frequency. By implementing a current feedback loop, these oscillations can be properly damped, as it will be shown in a later section.

6.3.2 Control Circuit Design

6.3.2.1 Linear Controllers

If a linear controller such as PI or PID is used in the current loop, one needs to design amplitude and frequency of the triangular carrier, the regulator (PI or PID) in the current loop, and the regulator (PI) in the voltage loop. The following sections describe the design procedure.

A. Design of the Triangular Carrier

In order to ensure intersections required to obtain the bi-level pattern (see Fig. 6.2), and to avoid multiple switching, the slope of the current regulator output must always be less than

the slope of the carrier waveform. Assuming a proportional (P) regulator and using circuit equations to calculate required slopes, the following condition can be obtained:

$$M\omega I_{dc} + \omega^2 C V < 4 V_m f_m \tag{6.1}$$

where M is the modulation index, I_{dc} is the output dc current, C is the input filter capacitor, V

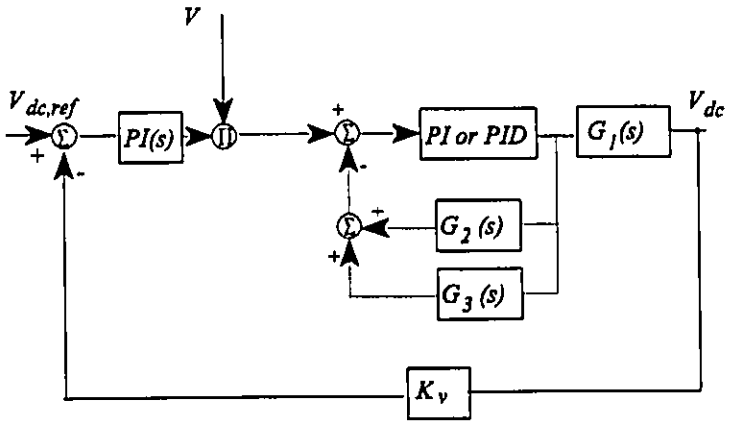

Fig. 6.4 Block diagram of the overall system.

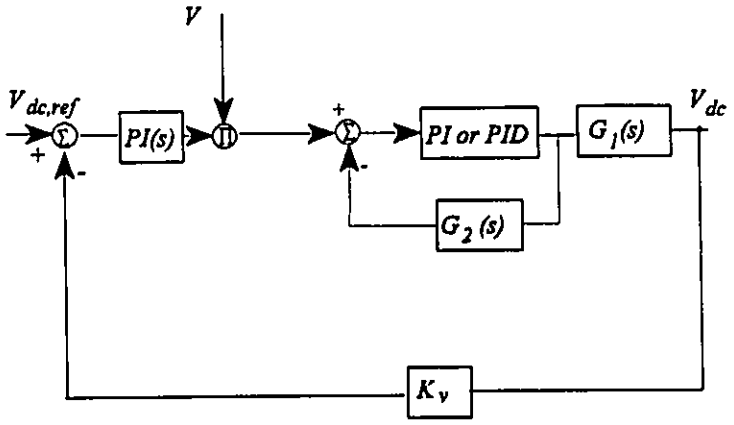

Fig. 6.5 Simplified block diagram.

is the peak value of the input ac voltage, V_m is the carrier amplitude, and f_m is the carrier frequency which dictates the switching frequency ($f_{sw} = f_m$). Since the value of the filter capacitor (C) is already known, a relation between the two unknowns, i.e., switching frequency ($f_{sw} = f_m$), and the amplitude of the carrier waveform V_m can be found from (6.1).

B. Design of the Regulators

The block diagram of the overall system is depicted in Fig. 6.4. The following transfer functions are defined:

$$G_1(s) = \frac{\hat{v}_{dc}(s)}{\hat{m}(s)} \tag{6.2}$$

$$G_2(s) = \frac{I_{qo}}{I_{ao}} \frac{\hat{i}_q(s)}{\hat{m}(s)} \tag{6.3}$$

$$G_3(s) = \frac{I_{do}}{I_{ao}} \frac{\hat{i}_d(s)}{\hat{m}(s)} \tag{6.4}$$

where I_q, I_d and I_a are the d-axis, q-axis and line currents and subscript o denotes the operating point around which the system equations are linearized. The procedure to derive the above transfer functions are explained in the Appendix. A typical PI regulator is specified by:

$$PI_i(s) = K_{pi}\left(\frac{1 + s\tau_i}{s\tau_i}\right) \tag{6.5}$$

with K_{pi} and τ_i being the gain and the time constant of the PI and the index i specifies that this is a PI used in the current loop. The PID transfer function is given by as:

$$PID_i(s) = \left(K_{pdi} + \frac{K_{ii}}{s} + K_{di}s\right) \tag{6.6}$$

where K_{pdr} K_{il} and K_{dl} represent the proportional, integral and derivative gains respectively. The loop transfer function is obtained by:

$$T_{loop}(s) = V\ PI_v(s)\frac{PI_i(s)}{1+PI_i(s)\,(G_2(s)+G_3(s))}\,G_1(s)K_v \tag{6.7}$$

where V is the amplitude of the ac mains and K_v is the voltage sensor gain. With unity power factor, the d-axis current becomes zero (I_{do} = 0), and the block diagram of Fig. 6.4 can be simplified to that shown in Fig.6.5. The loop transfer function therefore, reduces to the following equation:

$$T_{loop}(s) = V\ PI_v(s)\frac{PI_i(s)}{1+PI_i(s)\,G_2(s)}\,G_1(s)K_v \tag{6.8}$$

The above transfer function can be used for the proper design of the regulators. The bode plots of the closed loop system of such a design are depicted in Fig. 6.6. A PI is implemented in the current loop and the system has a phase margin of 75°. The need for damping resistors can be eliminated if the PI regulator is replaced with a more complicated regulator that introduces a zero in the transfer function, such as a PID. The zero of this PID is set equal to the knee of the PI transfer function. The bode plots for this new design are given in Fig. 6.7. The same phase margin is achieved while the damping resistors are reduced by 70%. Moreover, since the gain of the voltage loop is increased, a higher bandwidth for the overall system is achieved. The effect of the derivative of the line currents (obtained by the D component in the PID) on increasing the damping of the system is investigated in the Appendix. Also, since the damping resistors are reduced, the efficiency of the overall system (with PID regulator) is improved. Effect of the damping resistor on the efficiency was investigated in ***Chapter 5***. The current

control technique proposed here can be implemented either in rotating or stationary coordinates.

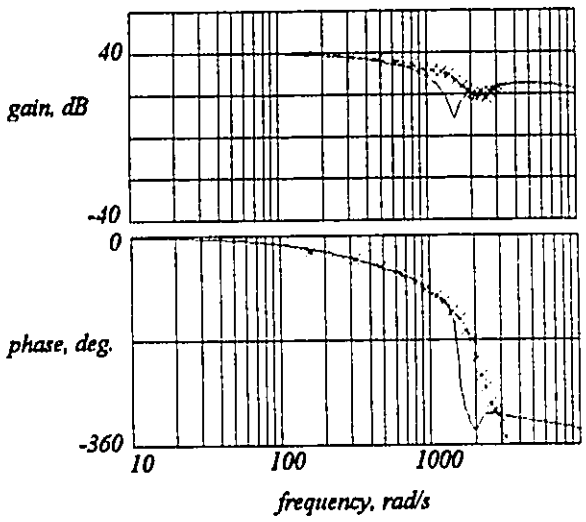

Fig. 6.6 Closed loop frequency response, PI regulator in the current loop.

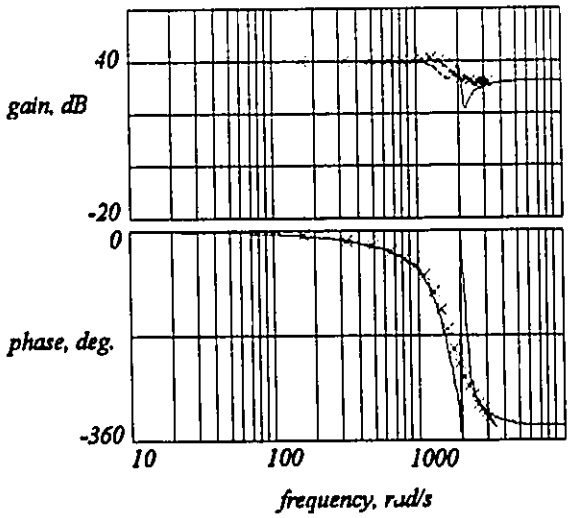

Fig. 6.7 Closed loop frequency response, PID regulator in the current loop.

6.3.2.2 Neural Network Controller

The main objective of this section is to show that it is possible to use a Neural Network controller instead of the traditional linear controllers for converter systems and synthesize a rugged controller. Therefore, this section does not include any in depth study of NNs and it should only be considered as a case study which opens the door for more research and investigation in the area.

NNs have self adapting capabilities which makes them well suited to handle non-linearities and uncertainties which may occur in a controlled plant. Preliminary investigations have shown that NN technology has the potential to improve the control of the power electronic systems [69]-[70]. Here, the task of the NN controller is to waveshape the input line currents of the PWM rectifier to obtain unity power factor operation, effectively damp low frequency resonance of the input LC filter and regulate the output voltage. The bi-level switching patterns (Fig. 6.2) for the three phases are defined as the targets for each output of the net(o_1, o_2, o_3). The NN is designed to emulate the action of the three PI regulators and comparators in the current loop. The weights are then adjusted to minimize the error between the net outputs and their targets. The PI regulator of the dc voltage loop is incorporated into the net. The target for this fourth output (o_4) is the amplitude of the current references. The NN structure, the pattern generation method and some design considerations are discussed below.

A. The NN Structure

A Back Propagation NN structure is shown in Fig. 6.8. Each neuron in the Back Propagation neural Network (BPN) has multiple inputs and one output. Each input flows

through a connection weight. Each neuron's output is a function of the input, the weights associated with that layer, a bias term and a node activation function [71]. The NN used consists of three distinct layers. The input layer, which is used to establish connection points transferring the input signal to the nodes in the hidden layer. A hidden layer which begins the learning process and an output layer to continue the learning process. Once the signal flows through the connection weights associated with the hidden layer (w^h), it is combined with a bias term (b^h) and fed through the node non-linearity, Fig. 6.9. This signal becomes the input to the output layer, flowing through connection weights (w^o), to be combined with bias term (b^o) and then processed by the output layer to provide the gating signals to the rectifier. The equations associated with the signals flowing from each layer to the next are:

$$i_j = f_j\left(\sum_{i=1}^{N} w_{ji}^{\,h}\, x_i + b_j^{\,h}\right)$$
$$o_k = f_k\left(\sum_{j=1}^{L} w_{kj}^{\,o}\, i_j + b_k^{\,o}\right) \qquad (6.9)$$

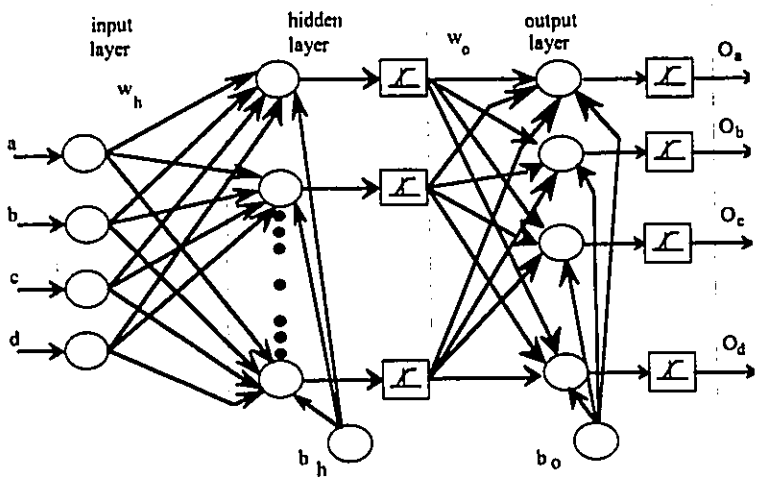

Fig. 6.8 NN structure.

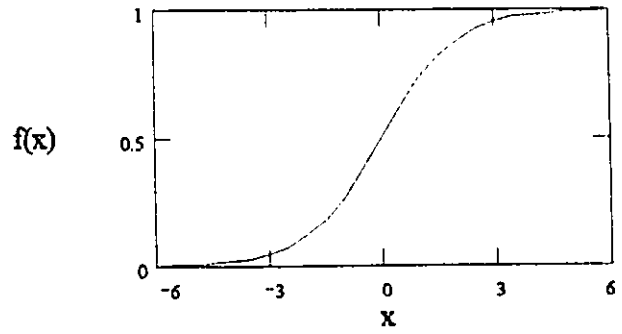

Fig. 6.9 The characteristic S-shape of the sigmoid function.

where N = number of input, L = number neurons in the hidden layer, i_j = the input to the output layer, o_k = the output of the NN, f = the sigmoid non-linearity shown in Fig. 6.9, x_i = the input and b_j , b_k = bias for each term, i expands over inputs, j expands over number of neurons in the hidden layer and k expands over the outputs. Steepest descent gradiant method is used to optimize the weights on each layer such that the output of the NN will approach the desired trajectory (minimize the error between the target and the net output). The weight update equations are the following for the input and the output layers [71]:

$$\left\{ \begin{aligned} w_{kj}^{o}(t+1) &= w_{kj}^{o}(t) + \eta\ \partial_k^o\ x_j \\ w_{ji}^{h}(t+1) &= w_{ji}^{h}(t) + \eta\ \partial_j^h\ i_j \end{aligned} \right\} \tag{6.10}$$

where, w^h = weight on the hidden layer, w^o = weight on the input layer, η = learning rate, ∂^h_j = error signal term associated with the hidden layer, i_j = output of the hidden layer (i.e. input to the output layer) and ∂^o_k = error signal term associated with the output layer of the net and the desired target. The NN will then provide the required gating to force the PWM rectifier to have a constant output dc voltage while maintaining unity power factor at the input ac source.

B. The Pattern Generation Scheme

The current error is input to a PI regulator whose output is then compared with a triangular carrier and the targets for the NN are is obtained based on the following rule:

$$\left\{ \begin{array}{ll} if\ e > carrier & target = 1 \\ else & target = 0 \end{array} \right\} \tag{6.11}$$

However, since the output of the net is not digitized a hard limiter has to be used to generate the bi-level signal. The hard limiter is described by:

$$\left\{ \begin{array}{ll} if\ O_t > 0.5 & O_t = 1 \\ else & O_t = 0 \end{array} \right\} \tag{6.12}$$

Therefore, the net produces a PWM pattern based on (6.11) which is used as the bi-level signal required in the pattern generator. The actual gating signals of the individual switches are

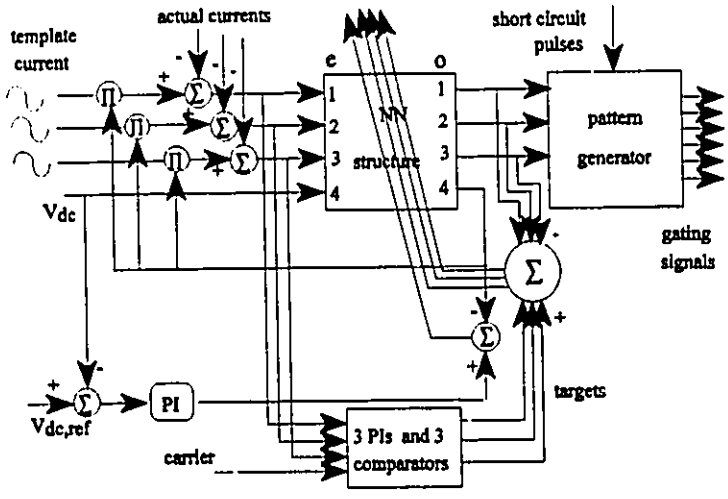

Fig. 6. 10 The proposed NN based controller.

obtained after adding the proper short circuit and protection pulses. The principle of operation of the pattern generator was described in previous chapters.

C. The DC Voltage Regulation Loop

Although a standard voltage loop with a PI regulator can be used to vary the output voltage according to the load demands as that in Fig. 6.1, it is intended to incorporate the voltage regulation loop into the NN structure. Therefore, the dc bus voltage is entered the net as the fourth input and the error is used to adjust the weights of the NN (Fig. 6.10). The fourth output (o_4) of the net is used to vary the amplitudes of the current reference signals.

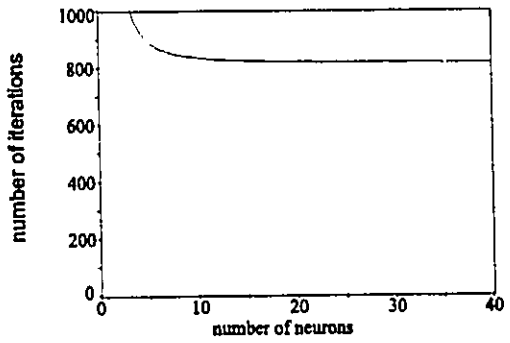

Fig. 6.11 Effect of number of neurons on the convergence time

D. Design of the Hidden Layer

The number of neurons in the hidden layer was chosen considering the convergence time. The NN for the control schem shown in Fig. 6.10 needed a minimum of 18 neurons to achieve good results. Fig. 6.11 indicates that increasing the number of neurons does not necessarily improve the convergence time. Also, simulation results showed that the transient response of the system is not significantly affected by an increase in number of neurons. The

learning rates of the input and output layers are obtained by trial and error. It was seen that too high a rate results in divergence and a solution could not be found. The information regarding the NN structure are given in Table 6.1.

Table 6.1 System specifications.

power circuit	ac side	$L = 0.7$ mH, $C = 370\mu$F, $R_a = 0.05\Omega$
	dc side	$L_{dc} = 3$ mH, $C_{dc} = 200\mu$F, $R_{dc} = 1.95\Omega$
control circuit (PI in current loop, $R_f = 0.5\ \Omega$)	current loop PI	$K_p = 1$, $\tau = 0.001$s
	voltage loop PI	$K_p = 0.1$, $\tau = 0.001$s
control circuit (PID in the current loop, $R_f = 0.15\ \Omega$)	current loop PID	$K_{pdi} = 1$, $K_{ii} = 1000$, $K_{di} = 0.01$
	voltage loop PI	$K_p = 0.5$, $\tau = 0.002$s
control circuit (NN controller, $R_f = 0.5\ \Omega$)	4 inputs	
	4 outputs	
	18 neurons in the hidden layer	
	$\eta = 0.2$	

6.4 Results

6.4.1 Simulation Results

Input/output characteristics of the proposed PWM rectifier (with PI regulator) under steady state operation are shown in Fig. 6.12. The low ripple output dc voltage and the rectifier input current before filtering are shown in Fig. 6.12.a. The rectifier input current has the same shape as the line-to-line (tri-level) gating signals. The input line current and the corresponding phase voltage are shown in Fig. 6.12.b. Unity power factor is achieved as it can be seen from

Fig. 6.12.b. The response of the PWM rectifier to a 50% change in the output dc voltage and to a reduction in the load resistance for the three proposed controllers (PI, PID and NN) are depicted in Fig. 6.13, 6.14, 6.15 respectively. It can be seen that the input line current remains near sinusoidal with unity power factor. The NN controller results in a wider range of operation than the rectifier with the PI regulator. For low modulation indices, the PWM rectifier with PI regulator results in oscillatory operation.

6.4.2 Experimental Results

To confirm the feasibility of the proposed control scheme and the correctness of the analytical results, a 1.5 KVA PWM rectifier with the specifications given in Table 6.2 was designed. The triangular carrier, current loop and voltage loop were designed with the help of (6.1) and bode plots of Fig. 6.6. The values are given in Table 6.2. The steady state waveforms shown in Fig. 6.16 are in good agreement with simulation. The output voltage is varied by 25% and the dc bus transient is shown in Fig. 6.17. The speed of the response is limited by the size of the output filter. The new steady state is reached in (1/4) of a cycle.

6.5 Conclusions

Closed loop control of the input line currents of a current source type PWM rectifier is studied. A current controlled unity power factor PWM rectifier is proposed that obtains high quality/low harmonic currents and achieves unity power factor operation for different operating points. It combines excellent steady state performance and fast response to reference changes. Three types of controllers are investigated. The NN controller is shown to be more rugged and capable of operating over a wider range of output dc voltages. The theoretical derivations and obtained models are verified through simulation and experimental results.

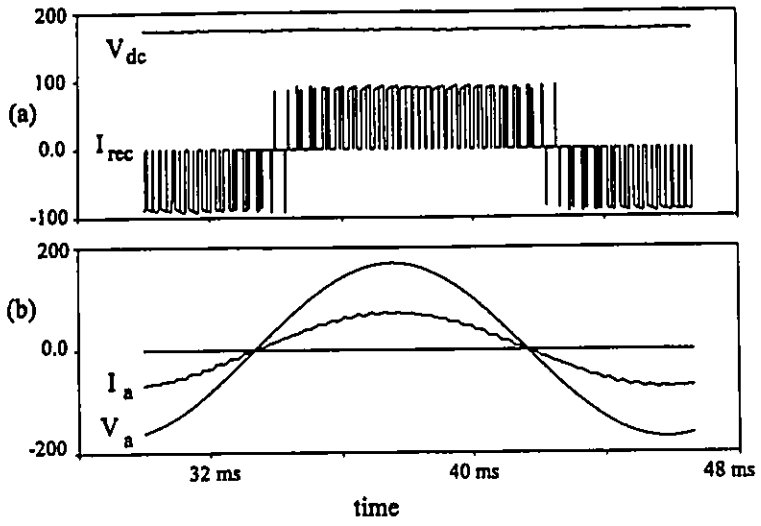

Fig. 6.12 (a) Output dc voltage V_{dc}, rectifier input current I_{rec}, (b) input line current I_{line}, input ac voltage V_a.

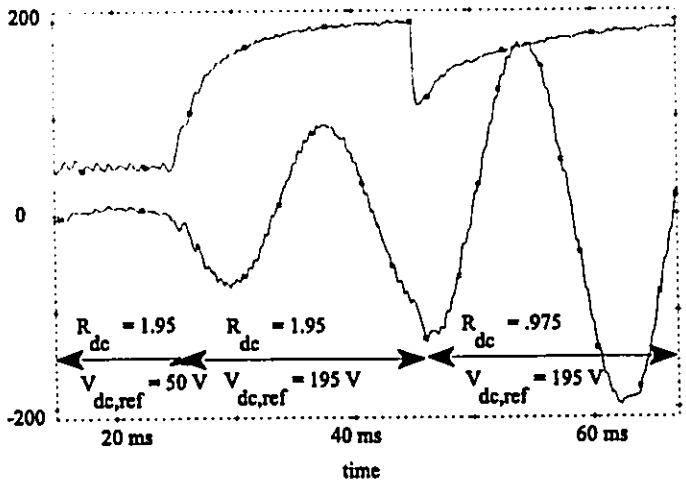

Fig. 6.13 Transient response, PI controller.

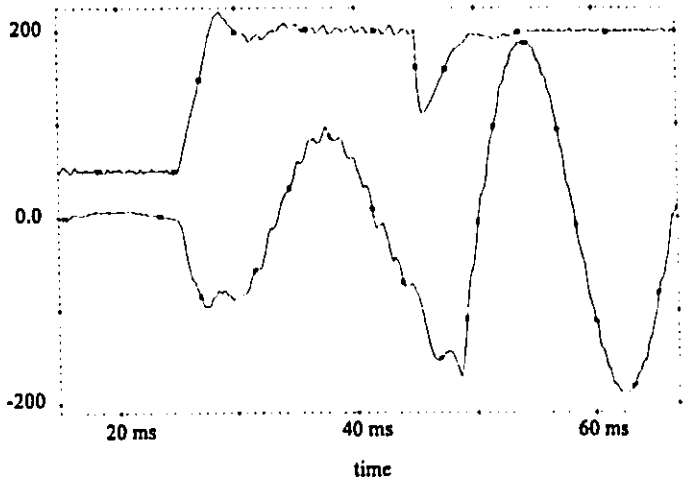

Fig. 6.14 Transient response, PID controller.

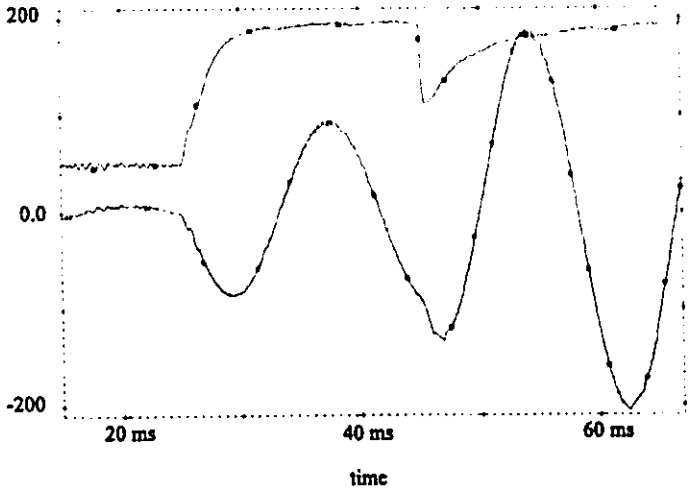

Fig. 6.15 Transient response, NN based controller.

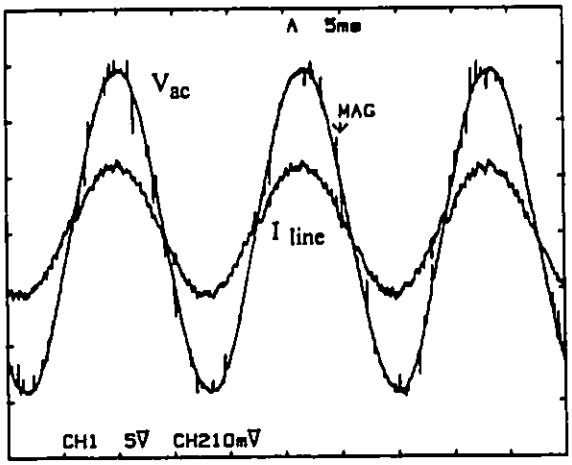

Fig. 6. 16 Experimental results. Input line current, I_{line}, input phase voltage, V_{ac}, (50V/div, 5A/div, 5ms/div).

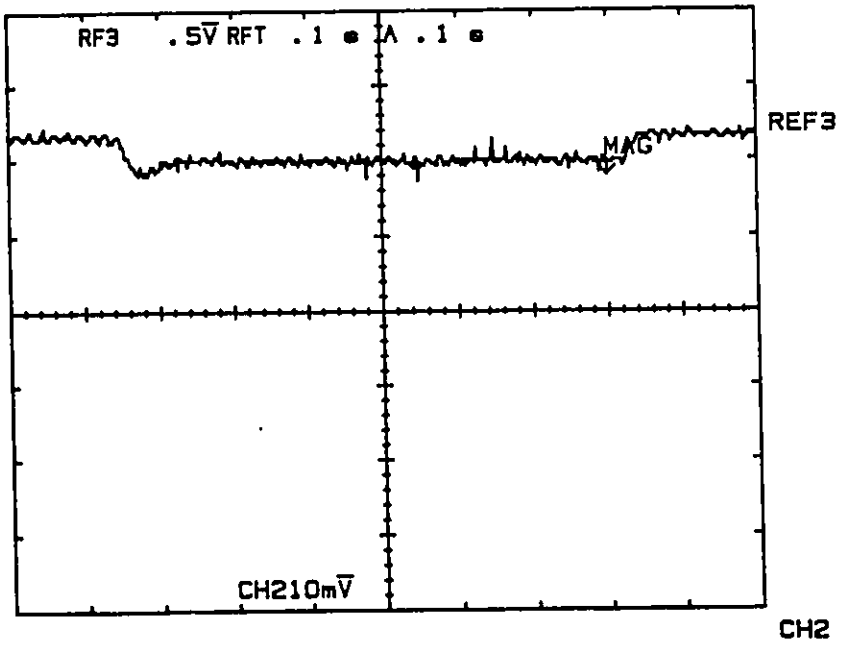

Fig. 6.17 Experimental results, dc output voltage, (50V/div, 5ms/div).

CHAPTER 7

A NEAR UNITY POWER FACTOR INPUT STAGE WITH MINIMUM CONTROL REQUIREMENTS FOR AC DRIVE APPLICATIONS

7.1 Introdction

Conventional ac induction motor drives use PWM Voltage Source Inverter (VSI) fed from a diode rectifier (Fig. 7.1). Due to voltage drops and the inverter voltage gain, six-step operation of the inverter is required at rated speed, resulting in large low order harmonic current and torque components. It was shown in ***chapter 2*** that of the two main structures available for ac to dc conversion, the Synchronous Rectifier is the one capable of producing a boost in the dc bus voltage. Therefore, in order to allow the inverter to operate in the PWM mode at rated speed, a Synchronous Rectifier is used in this chapter to slightly boost the dc bus voltage. The resulting converter system presents all the advantages associated with active front-end rectifiers such as near sinusoidal ac input currents and regenerative capabilities. The output inverter is current controlled, therefore, the dc bus control requirements are not stringent. This allows a simple control structure for the input rectifier, the main purpose being to ensure unity power factor operation. The rectifier is operated at a fixed modulation index, close to unity, and power transfer is controlled by pattern phase-shifting. The chapter presents an analysis and design guidelines for the complete drive system. Simulation and experimental results on a 1.5 kVA converter confirm the feasibility and advantages of the proposed structure.

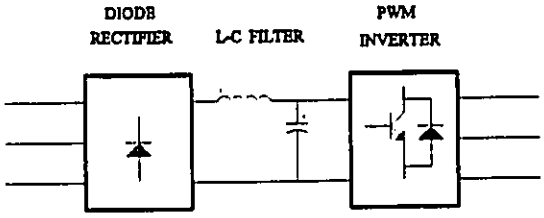

Fig. 7.1 Conventional ac drive system.

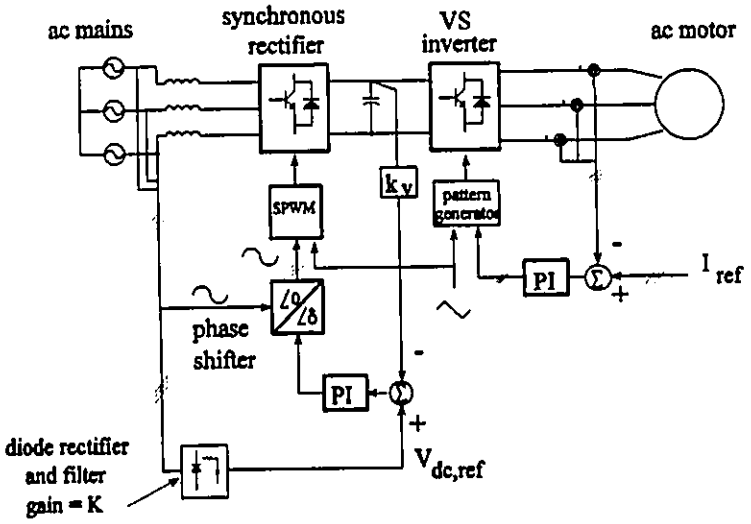

Fig. 7.2 The proposed ac drive system.

7.2 Description of the Proposed AC Drive System

The drive system shown in Fig. 7.2 includes two identical voltage source topology converters as input rectifier and output inverter and a dc link filter capacitor to isolate these two stages. A description of each stage with its control method follows.

7.2.1 Load Inverter

The output inverter stage is current controlled. For each phase the line current is compared with the reference waveform and the current error is fed to a PI controller and its output is compared with a triangular carrier which dictates the operating switching frequency. The integral term improves the tracking by reducing the instantaneous error between the reference and the actual current. The controller is the same as the one studied in ***Chapter 6*** and similar steps can be followed for the design procedure. The output line impedance determines the slope of current and therefore the existence of the intersections required to create the PWM pattern. For an induction motor load, the motor equivalent inductance varies with operating point which means the resulting slope changes and multiple switching may occur [72]. The problem can be solved or minimized by designing for the worst case. Therefore, the load is replaced by an inductive load with an equivalent power factor of 0.8. With this assumption, the existence of intersections can be guaranteed if the following condition is satisfied:

$$\frac{V_{dc}}{2L_o} \cdot 2\pi f I_p < 4 V_m f_m \qquad (7.1)$$

where V_m , f_m are the amplitude and frequency of the carrier, I_p , f are the amplitude and frequency of the output current reference, V_{dc} is the dc bus voltage , and L_o is the output line inductance. The above equation gives a means for design of the amplitude of the carrier

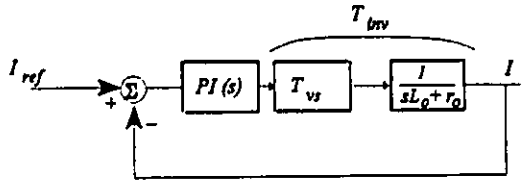

Fig. 7.3 Block diagram of the current loop.

waveform for a particular switch frequency ($f_{sw} = f_m$). Assuming the switching frequency is much higher than the fundamental output frequency, the inverter can be modelled by a simple gain, obtaining fundamental sinusoidal voltage waveforms at the output ac terminals. Therefore, the open loop transfer function of the inverter control circuitry can be given by:

$$G_i(s) = T_{pi}(s) \cdot T_{vs} \cdot \frac{1}{sL_o + r_o} \tag{7.2}$$

where T_{vs} is the inverter voltage gain and is given by:

$$T_{vs} = \frac{V_{dc} M_i}{2 V_m} \tag{7.3}$$

where M_i is the modulation index of the output inverter. Typical transfer function of a PI is given by:

$$T_{pi}(s) = K_{pi}\left(\frac{1 + s\tau_i}{s\tau_i}\right) \tag{7.4}$$

where subscript i denotes the parameters for the inverter control loop and K_{pi} is the gain and

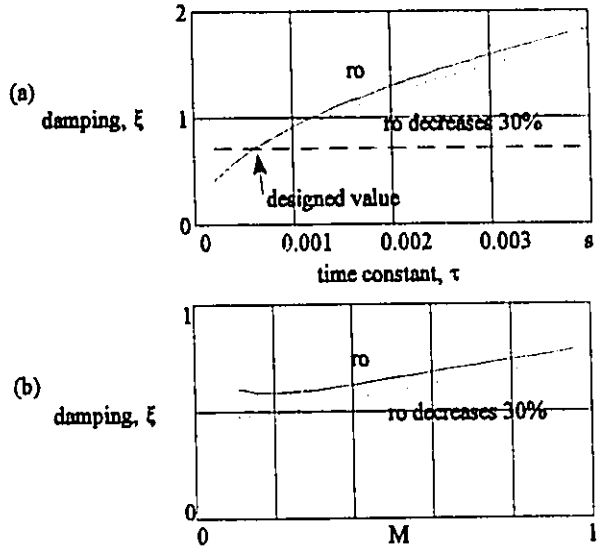

Fig. 7.4 (a) Damping factor vs modulation index, (b) damping factor vs PI time constant.

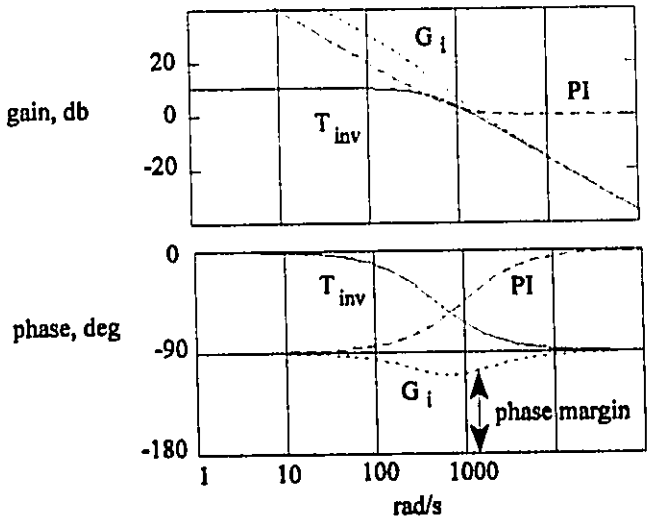

Fig. 7.5 Design of the current loop, (inverter T_{inv}, PI regulator and designed system G_i).

τ_i is the time constant. The block diagram of the inverter control loop is shown in Fig. 7.3. The overall transfer function is a second order system. The components of the PI regulator can be

designed to obtain a desired overshoot in the current step response to achieve a desired phase margin. The damping factor of the closed loop current transfer function is calculated from (7.2), (7.3), (7.4) and is given by:

$$\xi = \left(\frac{r_o}{2} + \frac{K_{pi} V_{dc} M_i}{4 V_m}\right)\sqrt{\left(\frac{2\tau_i V_m}{K_{pi} V_{dc} M_i L_o}\right)} \tag{7.5}$$

where V_{dc} is the dc bus voltage and M_i is the modulation index of the output inverter module. Dependency of damping factor on the modulation index M_i, and on the PI time constant (τ_i), are shown in Fig. 7.4. From Fig. 7.4 it can be seen that r_o and M_i have little effect on the damping factor. The time constant of the PI regulator was designed to obtain a damping factor close to 0.7, shown in Fig. 7.4. Effect of r_o on the phase margin (damping factor) is relatively small, since the second term in the paranthesis in (7.5) is the dominant factor. The bode plots of the open loop current transfer function are shown in Fig. 7.5, where it is seen that a phase margin of 60° is achieved.

7.2.2 Synchronous Rectifier

A PWM Synchronous Rectifier is used on the line side which obtains a dc voltage proportional to the inverse of the modulation index M. In the proposed scheme, the modulation index is fixed and the dc bus is therefore proportional to the ac input voltage:

$$\left\{ \begin{array}{c} V_{dc} = \dfrac{2\sqrt{2}\,V_{rec}}{M} \\ V_{dc} \propto V_{rec} \propto V_{phase} \quad for \ fixed \ M \end{array} \right\} \tag{7.6}$$

where V_{rec} is the amplitude of the rectifier input voltage. The modulation index would be set

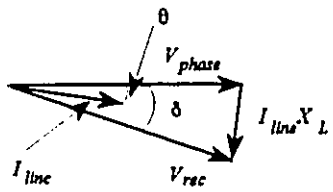

Fig. 7.6 Phasor diagram of the input Synchronous Rectifier.

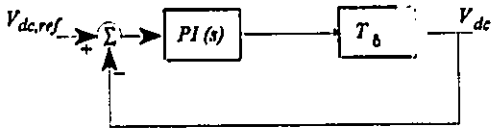

Fig. 7.7 Block diagram of the voltage loop.

to $M = 1$ if both converters use the same type of pattern generator and losses are neglected. The value will have to adjust to a lower value, typically $M = 0.9$ to account for losses.

In order to maintain near unity power factor, the rectifier ac input voltage is made equal to the ac line voltage. Assuming the link reactor is less than 0.4 pu, the resulting power factor

is greater than or equal to 0.98 (for a load angle $\delta = 24°$, the current phase shift $\theta = 12°$, Fig. 7.6). Under rated conditions and for a given modulation index M, this yields a given value of the dc bus voltage from (7.6). Therefore, rather than measure the ac input ac voltage, the base equivalent dc voltage is computed and used as a reference for the control loop or can be obtained from the line voltages by using the filtered output voltage of a three phase diode rectifier as shown in Fig. 7.2. The error between the reference and the actual dc bus voltage provides the error or control signal to the load angle or phase shift generator, Fig. 7.2.

In order to start the system, the six anti-parallel diodes must be reverse-biased. This means that the dc link capacitor must be initially charged to a voltage higher than that of a three-phase diode bridge rectifier. The dc capacitor can be charged to this value through the existing six anti-prallel diodes while the gate drives for the switches are turned off. After the capacitor is charged, the gatings of the switches can be connected and the control circuit will

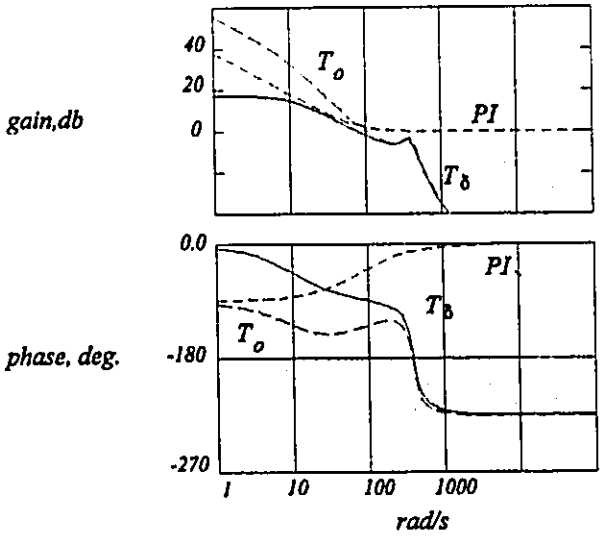

Fig. 7.8 Design of the control loop of the Synchronous Rectifier.

then charge the dc capacitor to the reference dc voltage (which is typically 10% higher).

The speed of response of the dc bus voltage control loop is not critical since the inverter will compensate for variations of the dc bus voltage under transient conditions. Therefore, the time constant of the PI regulator in the voltage loop can be chosen so that the response time is 10 times larger than that of the current loop. However, a more precise design is achievable using the transfer function of the input rectifier. The transfer function is computed by means of a dqo transformation and the linearization of the equations with small signal perturbations (explained in the Appendix). As it can be seen from Fig. 7.2, in order to design the regulator in the voltage loop, it is required to derive a transfer function from control angle δ to dc output voltage V_{dc}. This transfer function is given by the following:

$$\frac{V_{dc}(s)}{\delta(s)} = \frac{E1 \,.E2(s) + E5}{E3(s).E2(s) + E4(s)} = T_{\delta}(s) \tag{7.7}$$

where $E1$, $E2$(s), $E5$, $E3$(s) and $E4$(s) are given as follows:

$$E1 = \frac{3M_o}{R_s^2+(\omega L)^2}[V(\omega L\cos\delta_o - R_s\sin\delta_o) - \frac{M_o V_{dc}\omega L}{2}] \tag{7.8}$$

$$E2(s) = (s+\frac{R_s}{L})^2 + \omega^2 \tag{7.9}$$

$$E3(s) = 2C_{dc}(s+\frac{1}{RC_{dc}}) \tag{7.10}$$

$$E4(s) = \frac{3M_o^2}{4L}(s + \frac{R_s}{L}) \tag{7.11}$$

$$E5 = \frac{3M_o^2 \omega V_{dc}}{4L} \tag{7.12}$$

where: R_s = line resistance, R = equivalent resistance of the output inverter referred to dc bus, C_{dc} = dc capacitor, δ_o = power angle for the operating point, M_o = modulation index for the operating point, V_{dc} = dc bus voltage. The block diagram of the voltage loop is depicted in Fig. 7.7. The bode plots of the open loop voltage transfer functions are shown in Fig. 7.8. A PI regulator is designed to obtain a stable system with a phase margin close to 60°. The bode plots of the PI and the overall open loop transfer function, T_o are also shown (Fig. 7.8).

7.2.3 PWM Pattern Generator

Since the modulation index is fixed, any pattern generator can be used for the input stage, including the off-line optimized and stored patterns. However, advantage can be taken of carrier based optimized techniques, if it is desired to synchronize carriers for the rectifier and inverter stages. In particular, patterns with dead-bands, that result in an effective reduction of the switching frequency by one third, are particularly well suited for operation at a high modulation index. Furthermore, these carrier techniques give superior performance to stored patterns under transient conditions since response to changes in reference are instantaneous and there is no risk of producing dc components in the pattern during transitions. For the results presented in this chapter the conventional SPWM pattern is used.

7.2.4 Design of the DC Bus Capacitor

The dc bus capacitor must be designed to satisfy the following criteria:

- To comply with the minimum ripple requirement of the dc bus voltage.
- To limit the dc bus voltage fluctuation during load or input voltage transients.

It is concluded that the size of the capacitor is mainly limited by the second condition. DC bus voltage fluctuations can be due to the inverter current (load power) transients or the ac mains transients, such as switching capacitors or other loads on the ac bus. The dc voltage fluctuation generated by the inverter current transients are calculated from:

$$\Delta V_{dc} = \frac{1}{C_{dc}} \int_{t_1}^{t_2} (i_{rec}(t) - i_{inv}(t))\, dt \tag{7.13}$$

where $i_{inv}(t)$ and $i_{rec}(t)$ are the inverter and rectifier dc currents respectively. However, the main role of the capacitor during ac transients is to maintain the balance of power within the response time of the voltage control loop. The capacitor therefore can be calculated using the power balance equation during this transtion time which is given by:

$$\frac{1}{2} C_{dc}(V_{dc} + \Delta V_{dc})^2 T_r = P_{out} + \Delta P_{out} \tag{7.14}$$

where ΔP_{out} is the output power variation, ΔV_{dc} is the dc bus voltage variation and T_r is the response time of the voltage loop. Eliminating the steady state terms, neglecting the second order small terms and solving for the minimum capcitor value yields:

$$C_{dc} > \frac{\Delta P_{out} T_r}{V_{dc} \Delta V_{dc,max}} \tag{7.15}$$

where $\Delta V_{dc,max}$ is the maximum voltage drop allowed in the dc bus without loss of control. The input synchronous link rectifier is controllable as long as the anti-parallel diodes are reversed biased. Therefore, the maximum voltage drop is obtained from:

$$\Delta V_{dc,max} = V_{dc,nominal} - V_{dc,min} \tag{7.16}$$

From (7.15), (7.16) the minimum value of the dc link capacitor is calculated.

7.3 Design Example, Results and Comments

The specifications of the designed ac drive system are given in Table 7.1. The complete system is simulated and results for steady state and different transient conditions are obtained.

7.3.1 Steady State

Steady state operation for rated current is illustrated in Figs. 7.9,7.10. The followings can be concluded: (a) the dc bus voltage ripple is small and the average value is 30% higher than the normal diode rectifier voltage; (b) the output motor current is sinusoidal and has no low frequency components; (c) the input ac line current is sinusoidal and nearly in phase with the phase voltage, resulting in nearly unity power factor.

7.3.2 Inverter Current Transients

The current reference waveforms of the output inverter are decreased by 25% and the effect on the dc bus voltage is shown in Fig. 7.11. It is seen that the dc voltage regulation (δ loop) is not fast, however, the output inverter has fast response due to current control. The dc bus voltage ripple/fluctuation is rejected in the output currents. The step-up inverter transient is depicted in Fig. 7.12. The dc voltage variation is limited to $\pm$ 2.5%. The inverter is forced to operate in the overmodulation region and the error phase shift is increased.

7.3.3 AC Mains Transients

AC mains transients are due to the switching of the other loads on the ac bus. These will create overvoltage/undervoltage on the dc link. The loss of control happens when the input voltages are high enough to forward bias the diodes. However, the controllability is regained when the ac transient is diminished. Figure 7.13 shows a case where switching of the other loads at Point of Common Coupling (PCC) has resulted in a 10% decrease in the line voltage. The output currents are established in less than 2 cycles of transient conditions, while the dc bus reaches its steady state after 3 cycles.

7.3.4 Operation With Unbalanced Input Voltages

The ac mains with 10% amplitude unbalance is simulated and results are shown in Fig. 7.14. As expected the second harmonic components are generated in the dc bus, however, the amplitude of these components are very small (1%), due to the size of the dc capacitor. The input power factor remains near unity.

Table 7.1 Design example used in simulation.

V_{rms} =120 V, P_{out} = 2500 W
C_{dc} =2500 μF, L = 11.83 mH, R = 1Ω,
L_a = 25 mH, r_a = 12 Ω
V_{dc} = 377 V, M = 0.9
k_{pi} = 1, k_{pv} = 1.2, τ_i = 0.001, τ_v = 0.014, k_v = 0.01

7.4 Experimental Results

A 1.5 kVA laboratory prototype was built to confirm the feasibility of the proposed

control scheme. The values given in Table I were adapted to the 1.5 kVA power level. The steady state experimental results are shown in Fig. 7. 15. The power factor is near unity (θ = 10°, Displacement Factor = 0.98). Because of the control scheme used, the power factor remains near unity for different output dc voltages. A three phase resistive load was connected to the ac line to create a voltage drop on the line (due to the increase of the voltage drop across the line resistance). The dc output voltage and line current under this transient condition are shown in Fig. 7.16 (note the variation in dc bus voltage resulting from the scheme used).

7.5 Conclusions

A near unity power factor input stage with minimum control requirements is proposed for ac drive applications. A synchronous rectifier is used to slightly boost the dc bus voltage. The output inverter is current-controlled, therefore, the dc bus control requirements, both in steady state and transient, are not stringent. This allows for a simple control scheme for the input synchronous rectifier to ensure near unity power factor operation. Since a fixed modulation index for rectifier is used, the switching frequency can be reduced by appropriate choice of PWM pattern. Analysis and design guidelines are presented. The operation of the overall system under various transient and fault conditions is investigated. Feasibility and advantages of the proposed structure is confirmed by simulation and experimental results.

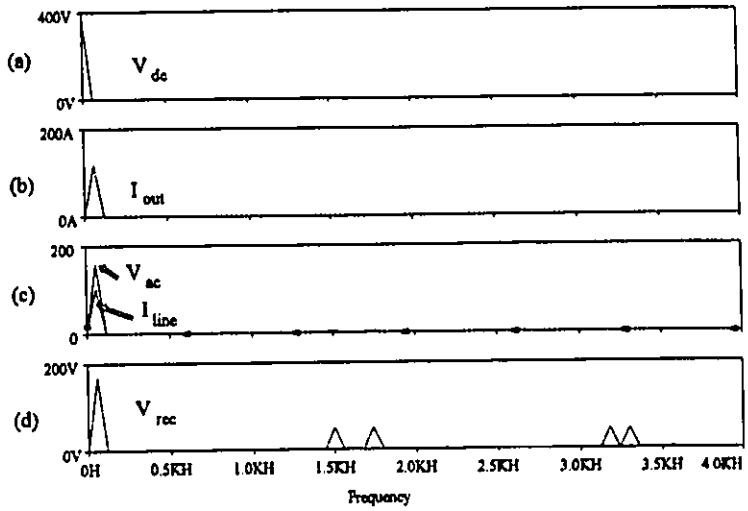

Fig. 7.9 (a) DC bus voltage, (b) inverter output current, (c) input line current (scaled) and line voltage,(d) rectifier input voltage.

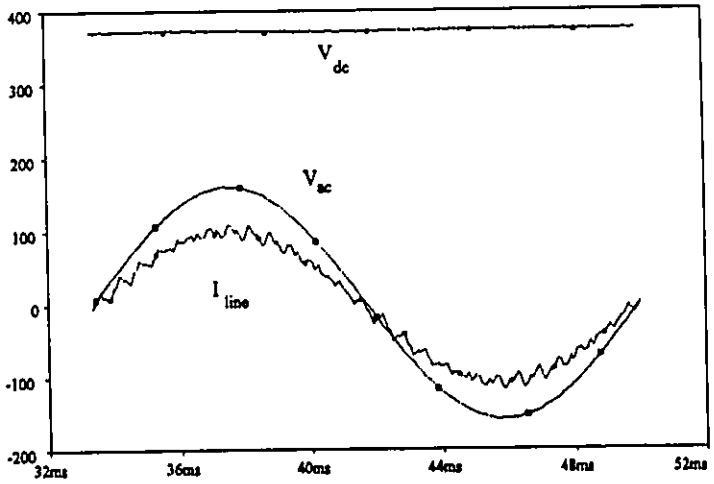

Fig. 7.10 Steady state waveforms. Input line current I_{line} (scaled), input ac voltage V_{ac}, dc bus voltage V_{dc}.

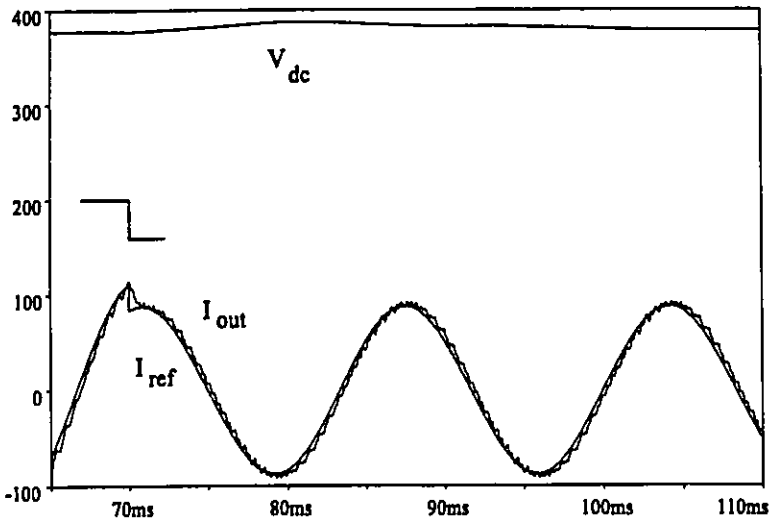

Fig. 7.11 Step down in the ouput inverter current. The currents are scaled (×10).

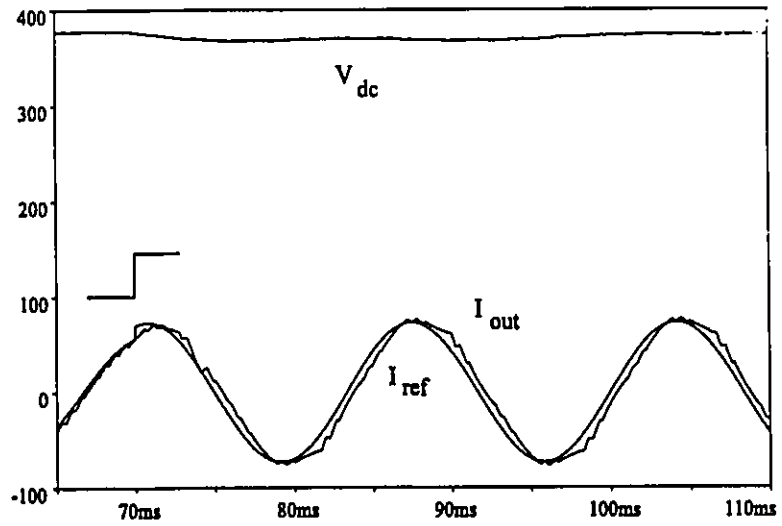

Fig. 7.12 Step up in the output inverter current. The currents are scaled (×5).

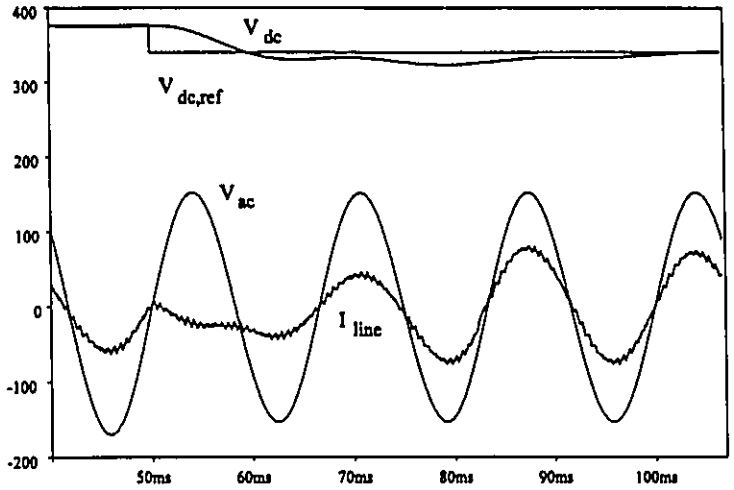

Fig. 7.13 AC transients, 10% step down in the ac line voltages.

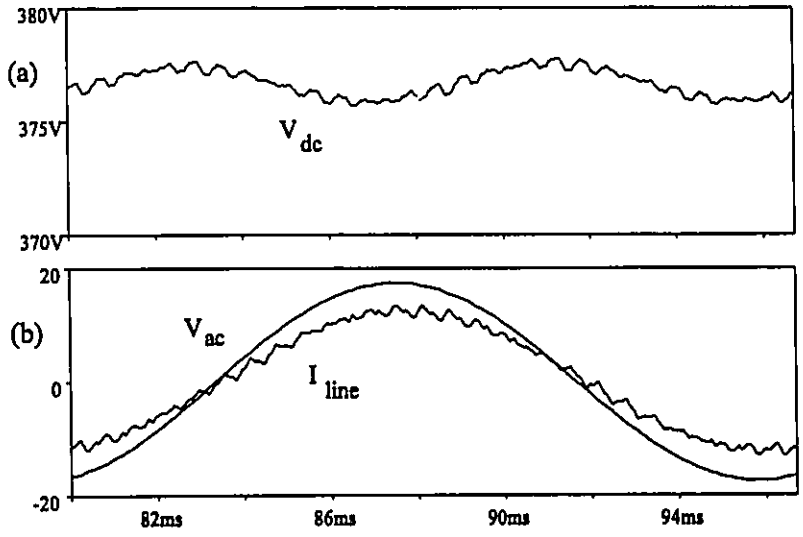

Fig. 7.14 Operation with unbalanced input voltages, (a) dc bus voltage, (b) input line current and voltage.

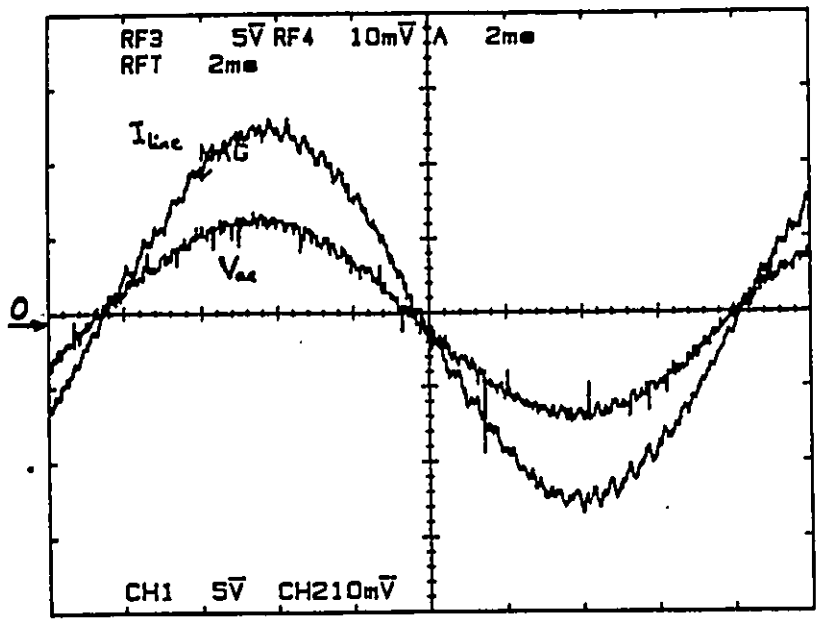

Fig. 7. 15 Experimental results, line current and phase voltage, (50V/div, 5A/div, 2ms/div).

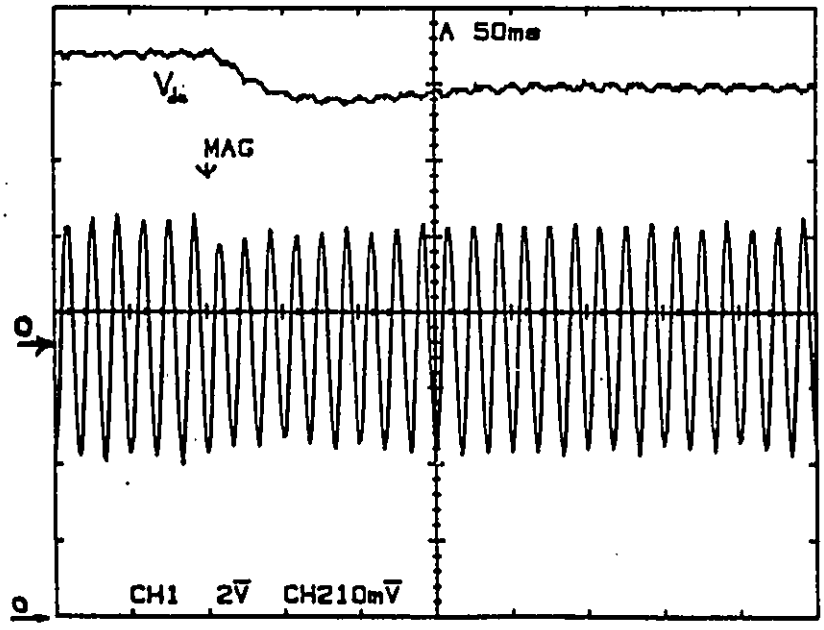

Fig. 7. 16 Experimental results, dc voltage transients, line current and dc voltage, (50V/div, 10A/div, 50ms/div).

CHAPTER 8

PERFORMANCE INVESTIGATION OF A CURRENT-CONTROLLED VOLTAGE-REGULATED PWM RECTIFIER IN ROTATING AND STATIONARY FRAMES

8.1 Introduction

The voltage source inverter approach with the Synchronous Rectifier as the input stage is superior to the conventional current source in terms of number of components and control options in low power applications. PWM rectifiers based on voltage source topology allow a full control over both active and reactive power exchange between the ac mains and dc source. The straight-forward power angle (δ) control of the rectifier is characterized by a slow response and potential stability problems. This chapter proposes a current-controlled PWM rectifier as an alternative. It provides near sinusoidal input currents with unity power factor and a low output voltage ripple. PWM pattern geneartion is based on ramp comparison technique, characteristics of which include fixed switching frequency which results in a well defined input current harmonic spectrum, fast dynamic response and simple control circuitry, ***Chapter 6***. The controller is implemented in (a) stationary (abc) frame, (b) rotating (dqo) frame. The design and the performance of the two controller options are investigated and compared.

8.2. Principles of Operation

8.2.1 Instantaneous Current Controller and Pattern Generator

The current controller was described in ***Chapter 6***. The instantaneous current error is fed to a Proportional-Integral (PI) regulator. The resulting output of the PI regulator is compared with a triangular carrier. If intersections are obtained, the error is forced to remain within the band defined by the amplitude of the triangular waveform. All three phases use a

common carrier signal. The integral term improves the tracking by reducing the instantaneous error between the reference and the actual current.

8.2.2 Stationary (abc) Frame Controller

The complete rectifier system includes a voltage-source topology PWM rectifier, a current-control loop and a dc voltage loop, Fig. 8.1. The switching pattern of the rectifier is generated by means of the current control scheme and the input line impedance determines the slope of the current and therefore the existence of the intersections required to create the PWM pattern. The amplitude of the current reference is obtained from the dc voltage loop. The output dc voltage is compared with a voltage reference and the error is fed to a PI regulator to reduce the steady state voltage error. The output of the PI regulator is then multiplied by a current waveform template to provide the three ac current references with the desirable input power factor and proper phase-shift, Fig. 8.1. To achieve unity power factor the current templates must be in phase with the input voltages. The modulating signals can be expressed by:

$$[e_{abc}] = (k_1 + k_2 \int dt)\ [[i_{abc,ref}] - [i_{abc}]] \tag{8.1}$$

where k_1 , k_2 are proportional and integral gain of the PI respectively and $[i_{abc}]$, $[i_{abc,ref}]$ are reference and actual line currents. In order to compare the two controllers, it is necessary to transform (8.1) to the rotating frame as given by the following:

$$[e_{dq}] = [T]^{-1}(k_1 + k_2 \int dt)[T][[i_{dq,ref}] - [i_{dq}]] \tag{8.2}$$

where [T] is the transformation matrix and $[e_{dq}]$ is the set of modulating signals in the dqo

frame. The transformation matrix is given by:

$$T = 2/3 \begin{bmatrix} \cos \omega t & \cos(\omega t - 120) & \cos(\omega t + 120) \\ \sin \omega t & \sin(\omega t - 120) & \sin(\omega t + 120) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{8.3}$$

8.2.3 Rotating (dqo) Frame Controller

The rotating frame controller is depicted in Fig. 8.2. The three line currents are transferred to (dqo) frame and the controller desribed in Section 8.2.1 is used to provide the necessary gating signals. The magnitudes of the reference currents in (dqo) frame ($I_{d,ref}$, $I_{q,ref}$) are dictated by the voltage feedback loop. Any arbitrarily rotating frame (Fig. 8.3.a) can be chosen as the reference frame. However, if the q axis is in phase with the phase a (Fig. 8.3.b), in order to achieve unity power factor operation, the reference signals for the dq axis currents must satisfy:

$$I_{d,ref} = 0, \qquad I_{q,ref} = I_{dc} \tag{8.4}$$

Since in the chosen reference rotating frame d-axis component represents reactive power. The modulating signals for the rotating frame controller as:

$$[e_{dq}] = (k_1 + k_2 \int dt)\ [[i_{dq,ref}] - [T]^{-1}[i_{abc}]] \tag{8.5}$$

which can also be rewritten in the form of:

$$[e_{dq}] = (k_1 + k_2 \int dt)\ [[i_{dq,ref}] - [i_{dq}]] \tag{8.6}$$

8.2.4 Comparison of Current Controllers

For a ramp comparison pattern generation scheme, the features and characteristics of the two controllers can be summarized as follows:

- By comparing (8.2) and (8.6) it can be concluded that the stationary and rotating frame controllers are identical if the integral part of the regulator is eliminated i.e. ($k_2 = 0$).
- The amplitude and phase are the control variables in the stationary frames. The controller handles ac signals in the steady state. These variables are transformed into dc quantities (dqo components) in the rotating frame.
- The rotating frame controller eliminates the steady state error, since it operates on dc quantities and the integrator has an infinite gain at zero frequency. The stationary controller regulates ac signals (ac fundamental component) and the integrator has a finite gain at this frequency. Therefore, there is an inherent amplitude and phase error. This error depends on the input frequency.
- The command signals are decoupled for the rotating frame controller. This allows alternate implementations of P and Q control of the rectifier.
- The stationary frame controller has the obvious advantage of simplicity since it can be implemented by simple analog circuitry, whereas digital calculations are required for the rotating frame controller. However, for applications which require high accuracy, the rotating frame controller is the preferred solution.

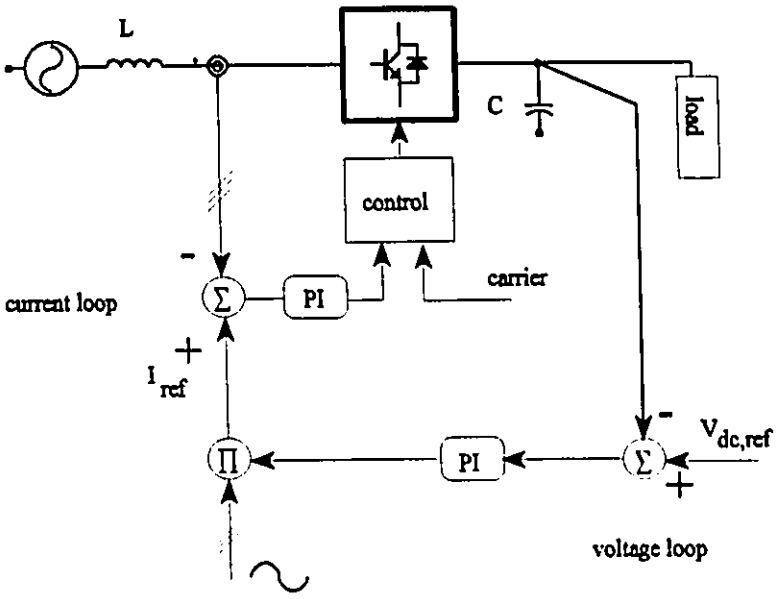

Fig. 8.1 PWM rectifier with stationary frame controller.

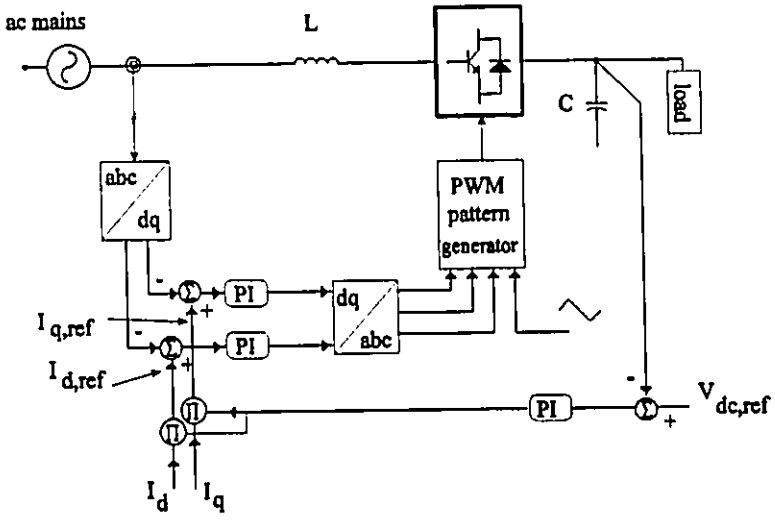

Fig. 8.2 PWM rectifier with rotating frame controller.

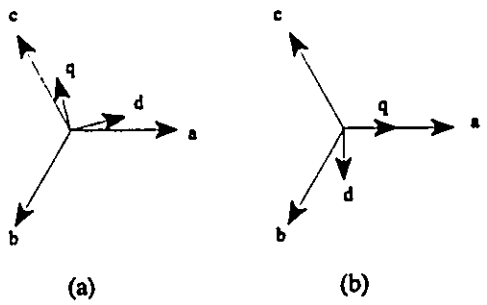

Fig. 8.3 (a) An arbitratry rotating frame, (b) the chosen reference rotating frame.

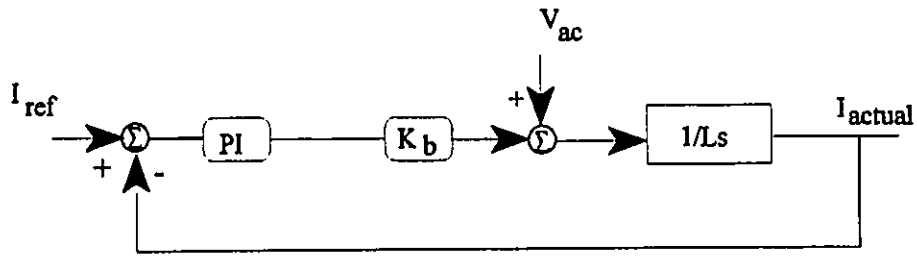

Fig.8.4 Block diagram of the current loop.

8.3 Control System Design

8.3.1 Design of Instantaneous Current Controller

The current controller is the same as the one designed in ***Chapter*** 7. It involves the choice of the frequency and amplitude of the carrier signal and the components of the PI regulator. The slope condition that guarantees intersections in this case is found to be:

$$2\pi f I_m + \frac{V_{tri} + 0.5\ V_{dc}}{L} < 2 f_s V_{tri} \qquad (8.7)$$

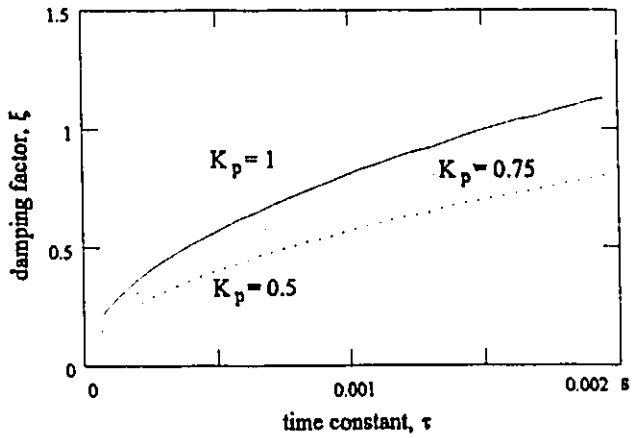

Fig. 8.5 Damping factor as a function of PI time constant (proportional gain, K_p as parameter).

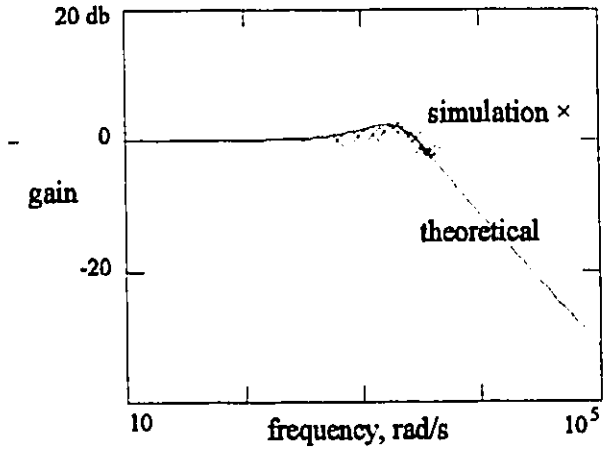

Fig. 8.6 Closed loop frequency response of the current loop, simulation vs theoretical results.

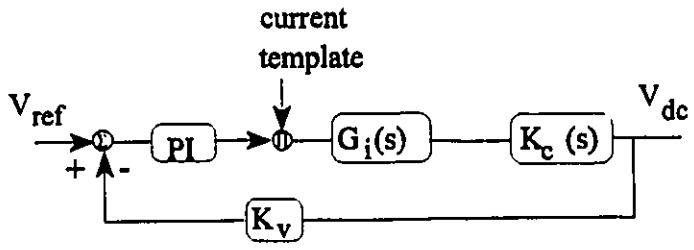

Fig. 8.7 Block diagram of the overall system.

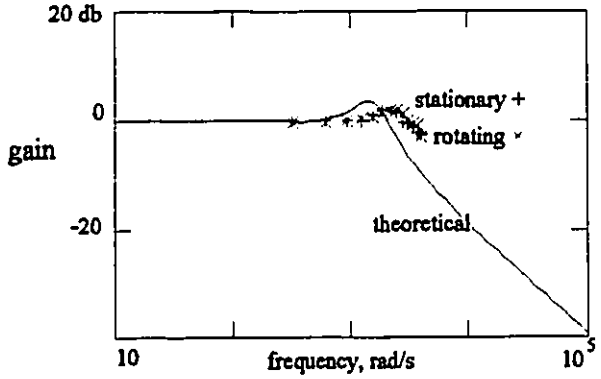

Fig. 8.8 Closed loop frequency response of the overall system, simulation vs theoretical results.

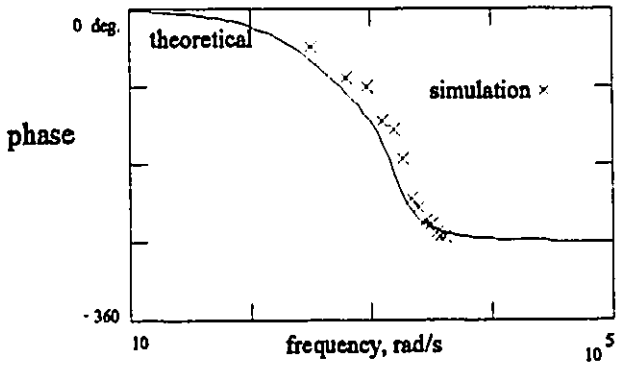

Fig. 8.9 Phase response of the overall system.

where V_{in} = rectifier input voltage, V_{dc} = output dc voltage, f_m, V_m are the frequency and the amplitude of the triangular carrier and can be chosen to satisfy (8.7). In obtaining (8.7), the effect of the integral part on the slope of the error was ignored. Since, in the absence of the integral component, both controllers are essentially the same, the slope condition is identical for both controllers. Furthermore, unlike applications to VSI and induction motors, slope conditions can be usually met, since the input ac inductance is well defined.

8.3.2 Design of the Stationary Frame Controller

It is assumed that the control technique produces fundamental line-to neutral voltages

which are proportional to the modulation index M. Therefore the rectifier leg is modelled as a constant gain. The block diagram of the current loop with the above assumptions is shown in Fig. 8.4. The transfer function of the current loop is given by:

$$Gop_i(s) = K_b\, PI_i(s)\frac{1}{Ls} \tag{8.8}$$

where L is input line inductor. K_b denotes the voltage gain of the converter and is given by:

$$K_b = \frac{V_{dc}M}{2\sqrt{2}V_m} \tag{8.9}$$

where M is modulation index. PI_i(s) in (8.8) is a typical representation of PI regulators consisting of a gain $K_p = k_1$ and a time constant $\tau(= k_1/k_2)$. A second order transfer function can be found for the closed loop system from Fig. 8.4. This transfer function is used to choose the components of the PI regulator. The variation of the damping factor of the current loop as a function of time constant of the current loop PI regulator is shown in Fig. 8.5. It is concluded that a smaller time constant results in a larger overshoot. The current controller can then be designed to obtain a desirable (%5) overshoot (in closed loop) to step change in the amplitude of the current reference. This design procedure is confirmed by simulation results in a later section (current waveforms transformed to dq frame shown in Fig. 8.10). The bode plots for the closed loop current transfer function are depicted in Fig. 8.6. The actual system behaviour obtained from simulation matches closely the proposed model.

8.3.3 Design of the Rotating Frame Controller

For comparison purposes, a PI with the same components as those of the stationary

frame controller is used for the rotating frame.

8.3.4 Design of Voltage Loop

The instantaneous power equation relating input and output quantities of the rectifier is obtained by differentiating the energy quantities:

$$\frac{d}{dt}\left(\frac{1}{2}C_{dc}V_{dc}^{2}\right) + \frac{V_{dc}^{2}}{R} = \frac{3}{2}\left[V_{s}I_{s}\cos\phi - \frac{d}{dt}\left(\frac{1}{2}LI_{s}^{2}\right)\right] \tag{8.10}$$

where: C_{dc}, R = dc side capacitor and load resistance;

V_s, I_s = amplitudes of input ac voltage and line current;

$\cos\phi$ = input power factor;

V_{dc} = output dc voltage.

The converter is assumed to be ideal (no losses, no energy storage element, high frequency switching). Linearizing the power equation around the operating point (V_{dco}, I_{so}) and considering unity power factor operation ($\phi = 0$) yields:

$$K_{c}(s) = \frac{\Delta V_{dc}}{\Delta I_{s}} = \frac{-\frac{3}{2}LI_{so}s + V_{so}}{C_{dc}V_{dco}s + \frac{2V_{dco}}{R}} \tag{8.11}$$

The right hand zero of (8.11) indicates that the system has a non-minimum phase characteristic. This results in a negative transient during dc transients as shown in Figs. 8.10 and 8.11. The overall transfer function is:

$$Gop_{v}(s) = PI_{v}(s)K_{c}(s)G_{i}(s) \tag{8.12}$$

where $G_i(s)$ is the closed loop current transfer function. The block diagram of the voltage loop is shown in Fig. 8.7. The components of the PI regulator are designed with the help of (8.12) to stabilize the system and obtain the required performance. The bode plots for the overall system transfer function are shown in Figs. 8.8, 8.9 and compared with the corresponding simulation results. The models describe the converter properly, although the exact break frequency is removed from the predicted one.

8.4. Results

8.4.1 Steady State

The complete system operating at a 3.1 kHz switching frequency is simulated (specifications in Table 8.1) and the following results are obtained. Fig. 8.10.a shows the operation of the PWM rectifier in the steady state. The input currents are sinusoidal and the input power factor is unity, however there is a small phase/amplitude error in the steady state which is depicted in Fig. 8.10.b (phase error = 2°, amplitude error = 2%). Fig. 8.11 shows the results for the rotating frame controller under the same conditions. It can be seen that in this case, there is no phase/amplitude error in the steady state, Fig. 8.11.b.

Table 8.1 Simulation circuit parameters.

rated values	P_{dc} = 25 kW, V_{rms} = 120 V, I_{rms} = 69.4 A
power circuit components	L = 1.83 mH = 0.4 pu, C_{dc} = 250 μF
current loop PI regulator	K_p = 1, τ = 0.0006 s
voltage loop PI regulator	K_p = .15, τ = 0.00075 s
voltage sensor gain	K_v = 0.01

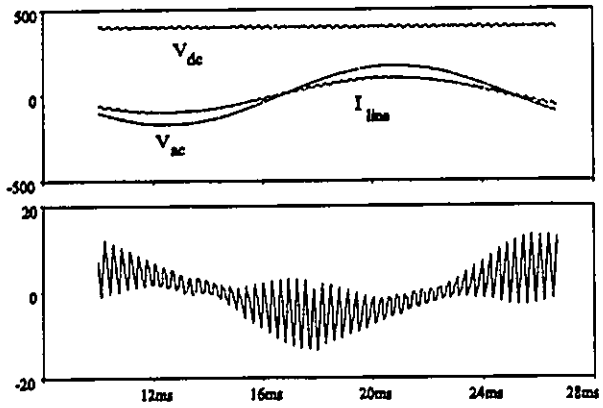

Fig. 8.10 Simulation results for stationary frame controller, (a) output dc voltage, input phase voltage and current, (b) steady state error.

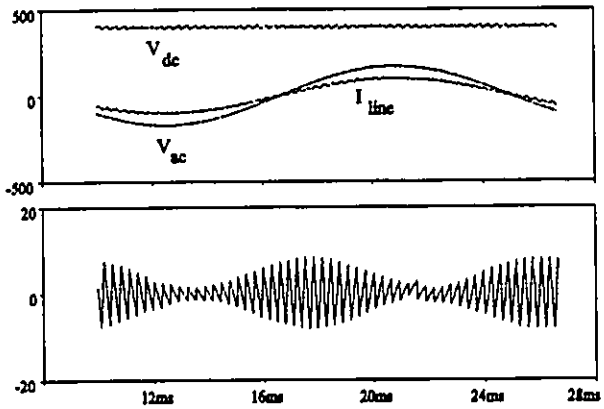

Fig. 8.11 Simulation results for rotating frame controller, (a) output dc voltage, input phase voltage and current, (b) steady state error.

8.4.2 DC Transients

The dc output voltage is changed by 25% and the results are depicted in Fig. 8.12. There is a negative overshoot during transient conditions which can be explained mathematically by the right hand zero. This negative step is typical of all non-minimum phase systems. The overall response of the system and the amplitude of this negative overshoot depend on the speed of response and the size of the power circuit parameters. For example

reducing the value of the input inductor reduces the negative overshoot.

The current waveforms are transformed to rotating frame (I_d, I_q) for a better presentation of the transients and better observation of the overshoot. The transient in the ac currents are presented as step changes in the d and q axis currents. The damping factor of the current loop as calculated by (8.7) is 0.65. The dq current components also show the characteristics of a sightly underdamped system, (as predicted by equations). The transient response of the rotating frame controller is shown in Fig. 8.13 and is almost identical to the previous case. The transient response of the rectifier with power angle (δ) control is shown in Fig. 8.14. The results show that control by phase shifting the PWM pattern (δ control) results in a very slow response.

8.5. Conclusions

A high performance three phase current-controlled voltage-regulated rectifier is presented. A carrier comparison type current-control technique produces the switching pattern for instantaneous control and waveshaping of the input currents. The control technique operates with fixed switching frequency and has a fast response to system transients. The control scheme is rugged and has a simple circuitry. The current controller is presented in both stationary (abc) and rotating (dqo) frames. The performance and design considerations of the two controller options are compared. It is concluded that the rotating frame controller has zero steady state error hence very good steady state accuracy. The transformation of ac quantities to the dqo frame is found to be a very useful tool in evaluating the controller designs. A complete analysis of the overall system with design equations for control circuits is given. The theoretical results obtained are verified through simulation.

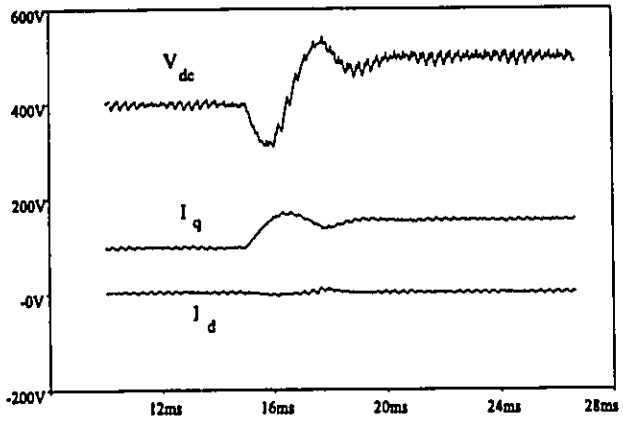

Fig. 8.12 Transient response for stationary frame controlier, output dc voltage V_{dc}, d-axis and q-axis currents.

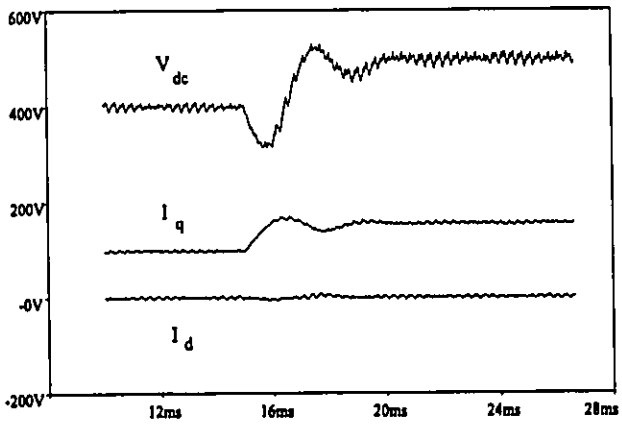

Fig. 8.13 Transient response for rotating frame controller, output dc voltage V_{dc}, d-axis and q-axis currents.

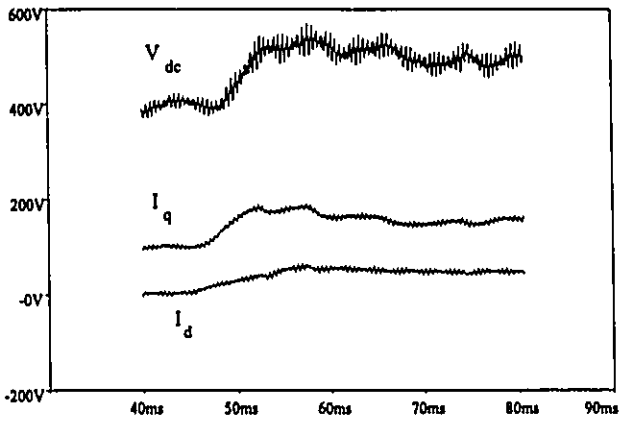

Fig. 8.14 Transient response of PWM rectifier with phase shift control, output dc voltage V_{dc}, d-axis and q-axis currents.

CHAPTER 9

SUMMARY AND CONCLUSIONS

9.1 Summary

The challenge in operating an ac to dc conversion scheme is to obtain high quality (low distortion) output waveforms while injecting minimum current harmonics into the ac mains. Of particular importance is the reactive power requirement which is quantified by the Input Displacement Factor. PWM ac/dc power conversion schemes are categorized according to the characteristics of the dc link which can consist of either an inductor (current source topology) or a capacitor (voltage source topology). In the thesis, these two topologies are investigated from the point of view of principles of operation, switch realization comparison, converter and switch ratings, operating regions, filtering requirements, power factor considerations and control aspects. Potential problems are recognized and viable solutions are proposed to optimize the performance of the two topologies mostly in terms of the Input Displacement Factor. In particular, the following contributions are made.

A. Current Source Topology

- A systematic procedure for design of the input filter is proposed.
- A new compensation scheme is proposed to achieve unity Input Displacement Factor independently of the rectifier operating point. The proposed method is very simple and does not require additional transducers. It uses a feed-forward dc current loop and the standard dc voltage/current regulation loop to regulate the amplitude and phase of the modulating signals. Parameter sensitivity, effect of variations of input voltages and the limitations of the proposed scheme are studied.
- A new control scheme that eliminates the need for damping resistors in the input LC

filters is proposed. The effectiveness of the proposed method is confirmed through small signal analysis. The current source PWM rectifier with the proposed pattern generation scheme has a higher efficiency due to the elimination of the damping resistors. The proposed scheme is investigated for ac drive applications and various transient and fault conditions are studied. Also, a topology for non-regenerative applications is proposed that requires only three base drives and can be used in non-regenerative applications.

- Closed-loop current control of current source PWM rectifier is investigated. The input line currents are controlled to obtain low harmonic currents with unity Displacement Factor. This method is similar to the conventional method used for the voltage source topology. Output dc voltage regulation is achieved by varying the amplitudes of the current references. Different types of controllers such as Proportional Integral (PI), Proportional Integral Derivative (PID) and a Neural Networks (NN) based controller are investigated.

B. Voltage Source Topology

- A near unity Displacement Factor input stage for VSI based ac drive systems is proposed. The propo :d topology uses a voltage source PWM rectifier to slightly boost the dc link voltage, hence allowing for operation of the inverter in the PWM mode under rated conditions. The output inverter is current-controlled therefore, a less stringent dc bus voltage is required and a simpler control strategy for the input rectifier can be used, the main purpose being to ensure unity power factor operation. The front-end rectifier is operated by controlling the amplitude of the rectifier ac terminal voltage.

By keeping this voltage equal to the amplitude of the ac mains voltage, IDF remains near unity.

- A current-controlled voltage source PWM rectifier is investigated in both rotating (dqo) and stationary (abc) frames. The proposed system provides near sinusoidal input currents with unity power factor and low output voltage ripple.
- Small signal analysis of both current source and voltage source type rectifiers are obtained and various transfer functions are derived which can be used for accurate design of the regulators. The feasibility and advantages of all the proposed schemes are verified by simulation and by experimentation on laboratory units.

9.2 Conclusions

It is concluded that the voltage source topology attains higher performance with more control options but requires closed loop control. This topology is better suited for lower power rating and higher switching frequencies. The current source topology offers reliability with inherent short circuit protection. Therefore, the current source topology is more attractive in high power/ high voltage applications.

Unity Displacement Factor operation can be achieved in the current source topology by properly phase shifting the switch gating signals. The method is useful in retrofit applications since no added transducer and major change to the design and control circuitry is required.

Conventional closed loop current control techniques used for voltage source topology are applicable to current source topology with some modifications to the pattern generator. It has been shown in the thesis that a derivative component of the line current contributes to the damping of the system. This leads to elimination of damping resistors and results in a higher

efficiency.

9.3 Suggestion for Future Work

The current source topology has been found to be more suitable for high power applications. However, for these applications, the switching frequency may have to be limited to 500 Hz (if GTO technology is used). Therefore, future work can be concentrated in finding proper switching strategies that can reduce the effective switching frequency. Also, an investigation in snubber topology and resonant switching strategies can result in reduction of switching losses, making an increase in the switching frequency possible.

Non-linear controllers such as fuzzy controllers and Neural Network based controllers have been proposed for controlling non-linear systems. These techniques are currently under investigation for implementation in power electronics systems, but more work is needed before widespread implementation can be considered. The current source PWM rectifier with the input filter is a non-linear system for which the PI regulator (used in the current control loop) cannot be optimized for a large range of operation. Therefore, this system is a good case study for implementing a non-linear controller.

Unbalanced input voltages can affect the performance of PWM rectifiers. A more complete analysis of this case is needed to provide a solution as to what switching/control strategy is the more suitable. These solutions in general depend on the power level and types of applications. The small signal models developed in the thesis can be modified to include this particular case.

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APPENDIX A

A.1 Introduction

A procedure for deriving small signal models for converter topologies is explained in this appendix. The method is first described in a general form which is applicable to all converter systems which interface dc and ac sides through a switching action. Then the procedure is used to derive various transfer functions for the converter systems proposed in previous chapters. These transfer functions were used to design the regulators for the proposed systems.

A.2 General Method for Obtaining Small Signal Models of Converter Systems

The procedure to derive small signal models and input to output transfer functions, is divided into six steps which are described below:

step 1:

A set of differential equations describing the overall dynamic system (in general having m inputs, n outputs and l state variables) and is written. The state variables are chosen and the equations are organized in the following matrix form:

$$\left\{\begin{array}{l} pX_{l\cdot 1} = A_{l\cdot l}X_{l\cdot 1} + B_{l\cdot m}U_{m\cdot 1} \\ Y_{n\cdot 1} = C_{n\cdot l}X_{l\cdot 1} + D_{n\cdot m}U_{m\cdot 1} \end{array}\right\} \qquad \text{(A.1)}$$

where: p is the derivative operator;

X is a column matrix ($l\times 1$) of state variables;

Y is a column matrix ($n\times 1$) of outputs;

A is the state ($l\times l$) matrix;

U is the column matrix ($m\times 1$) of inputs;

B,C,D are matricies of proper size obtained from the arrangement of the equations.

step 2:

In converters, the switching action is represented by a switching function which can be replaced by its fourier series. However, if PWM pattern is used, the higher order harmonics (frequencies) can be neglected, i.e. only the fundamental component is used. For example a set of balanced switching functions can be given by:

$$\left\{ \begin{array}{l} S_1(t) = M \sin(\omega t + \sigma) \\ S_2(t) = M \sin(\omega t - \frac{2\pi}{3} + \sigma) \\ S_3(t) = M \sin(\omega t + \frac{2\pi}{3} + \sigma) \end{array} \right\} \qquad \text{(A.2)}$$

where M is the modulation index, σ is the control angle (phase shift with respect to the ac mains) and ω is the fundamental angular frequency.

step 3:

The differenatial equations of (A.1) usually include multiplication of variables by time varying signals such as (A.2). In other words, the differential equations are time variant and non-linear. In order to solve this problem, the reference frame is changed to a frame which is rotating with an angular speed of ω (equal to the frequency of the fundamental component of the switching functions). This results in a set of time invariant differenatial equations. The method is well known and the transformation matrix (also known as Park equations) is given by:

$$T = 2/3 \begin{bmatrix} \cos \omega t & \cos(\omega t - 120) & \cos(\omega t + 120) \\ \sin \omega t & \sin(\omega t - 120) & \sin(\omega t + 120) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \qquad \text{(A.3)}$$

with this transformation matrix, the following relations hold:

$$\begin{aligned} X_{dqo} &= T\, X_{abc} \\ X_{abc} &= T^{-1}\, X_{dqo} \end{aligned} \tag{A.4}$$

The differential equation of (A.1) can be rewritten in the dqo frame as:

$$\left\{ \begin{array}{c} pX_{dqo} = [TAT^{-1} - Tp(T^{-1})]X_{dqo} + TBU \\ Y = CT^{-1}X_{dqo} + DU \\ or\ Y_{dqo} = [TCT^{-1}]X_{dqo} + TDU \end{array} \right\} \tag{A.5}$$

where the subscript *dqo* represents variables un the dqo frame.

step 4:

At this stage, the steady state values (operating point condition) can be calculated from (A.5) be equating the derivative operator p to zero ($p = 0$). The steady state values are later used when deriving the small signal models.

step 5:

After calculating the steady state values, the equations are linearized around the operating point, using small signal purturbation method. After simplification, the small signal model is obtained which is typically shown in the following form:

$$\left\{ \begin{array}{l} p\Delta X_{dqo} = A_{dqo}\Delta X_{dqo} + B_{dqo}\Delta U \\ \Delta Y_{dqo} = C_{dqo}\Delta X_{dqo} + D_{dqo}\Delta U \end{array} \right\} \tag{A.6}$$

where Δ is used for small signals (when arranged in a matrix form) and subscript *dqo* represents matricies transformed to the new reference frame. However, for the sake of

simplicity from now on, this subscript is eliminated. The eigenvalues of the matrix A represent the poles of the system. All different transfer functions of this system have the same poles, however, the zeros are dependent on the particular input and output variables.

step 6:

In order to derive a particular transfer function from input $\hat{u}$ to output $\hat{y}$, the linearized dynamic equations of (A.6) can be rewritten as:

$$\left\{ \begin{array}{l} p\,\Delta X = A\,\Delta X + b_{1\cdot 1}\hat{u} \\ \hat{y} = c_{1\cdot 1}\Delta X + d_{1\cdot 1}\hat{u} \end{array} \right\} \tag{A.7}$$

The first equation in (A.7) is the system state equation with a single input variable $\hat{u}$, and the second equation is an output equation with a single output variable $\hat{y}$. Solving (A.7) in Laplace domain yields:

$$\frac{\hat{y}(s)}{\hat{u}(s)} = \frac{N(s)}{D(s)} = c_{1\cdot 1}(sI - A)^{-1}b_{1\cdot 1} + d \tag{A.8}$$

where N(s) and D(s) are the numerator and denominator polynomials respectively. This equation indicates that the formulation of transfer function is dependent only on the coefficients of the state and output equations (A.7).

A.3 Small Signal Model of Synchronous Rectifier

For the voltage source PWM rectifier, the three ac line currents and the output dc voltage are chosen as the state variables. The state matrix (in abc frame) is given by:

$$A = \begin{bmatrix} \frac{-R_s}{L} & 0 & 0 & \frac{-S_a(t)}{2L} \\ 0 & \frac{-R_s}{L} & 0 & \frac{-S_b(t)}{2L} \\ 0 & 0 & \frac{-R_s}{L} & \frac{-S_c(t)}{2L} \\ \frac{S_a(t)}{2C_{dc}} & \frac{S_b(t)}{2C_{dc}} & \frac{S_c(t)}{2C_{dc}} & \frac{-1}{R_{dc}C_{dc}} \end{bmatrix} \tag{A.9}$$

where the switching functions are defined as:

$$\left\{ \begin{array}{l} S_a(t) = \frac{M}{2} \sin(\omega t + \delta) \\ S_b(t) = \frac{M}{2} \sin(\omega t - \frac{2\pi}{3} + \delta) \\ S_c(t) = \frac{M}{2} \sin(\omega t + \frac{2\pi}{3} + \delta) \end{array} \right\} \tag{A.10}$$

The state variables and control inputs are:

$$\begin{aligned} X &= [i_a \;\; i_b \;\; i_c \;\; v_{dc}]^T \\ U &= [v_a \;\; v_b \;\; v_c \;\; 0]^T \end{aligned} \tag{A.11}$$

Since there are four differential equations, the transformation matrix must be modified to a 4×4 matrix as follows:

$$T_{4\cdot4} = \begin{bmatrix} T_{3\cdot3} & 0 \\ 0 & 1 \end{bmatrix} \tag{A.12}$$

After transformation to dqo frame, performing small signal perturbation, simplification and neglecting the second order small signal terms, the new state matrix A is obtained as:

$$A = \begin{bmatrix} -\frac{R_s}{L} & -\omega & \frac{M_o \sin\delta_o}{2L} \\ \omega & -\frac{R_s}{L} & -\frac{M_o \cos\delta_o}{2L} \\ -\frac{3M_o \sin\delta_o}{4C_{dc}} & \frac{3M_o \cos\delta_o}{4C_{dc}} & -\frac{1}{R_{dc}C_{dc}} \end{bmatrix} \qquad \text{(A.13)}$$

where sunscript o denotes the operating point values. Two control inputs namely, modulation index and control angle are considered and the B matrix is given as:

$$B = \begin{bmatrix} 0 & \frac{M_o V_{dco} \sin\delta_o}{2} & V_{dco} \cos\delta_o \\ \frac{1}{L} & V_{dco} \cos\delta_o & -\frac{M_o V_{dco} \sin\delta_o}{2} \\ 0 & -\frac{3I_{do} \sin\delta_o}{4C_{dc}} + \frac{3I_{qo} \cos\delta_o}{4C_{dc}} & -\frac{3I_{do} \cos\delta_o}{4C_{dc}} - \frac{3I_{qo} M_o \sin\delta_o}{4C_{dc}} \end{bmatrix} \qquad \text{(A.14)}$$

Finally, the state variables and control inputs in dqo frame are defined as:

$$\begin{aligned} \Delta X &= \begin{bmatrix} \hat{i}_d & \hat{i}_q & \hat{v}_{dc} \end{bmatrix}^T \\ \Delta U &= \begin{bmatrix} \hat{v} & \hat{m} & \hat{\delta} \end{bmatrix}^T \end{aligned} \qquad \text{(A.15)}$$

Now, any (output/input) transfer function can be obtained if the proper b and c column matricies as described in *step 6* are calculated.

A.3.1 Desired Transfer Functions

For the rectifier proposed in ***Chapter 7***, the desired transfer function is $\frac{\hat{v}_{dc}(s)}{\hat{\delta}(s)}$ which is derived and used for design of the regulators. In this case we have:

$$c = [0 \quad 0 \quad 1]$$
$$b = \left[V_{dco}\cos\delta_o \quad -\frac{M_o V_{dco}\sin\delta o}{2L} \quad -\frac{3M_o\cos\delta_o I_{do}}{4C_{dc}} \quad -\frac{3M_o\sin\delta_o I_{qo}}{4C_{dc}} \right]^T \tag{A.16}$$
$$d = [0]$$

A.4 Small Signal Model of PWM Buck Rectifier

For a current source type rectifier, the state matrix is more complicated since there are eight state variables (three line inductor currents, three input capacitor voltages, the output inductor current and the output capacitor voltage). Also, the existance of the damping resistors in the input filter makes the differential equations more complicated. The state matrix in the abc frame is given by:

$$A = \begin{bmatrix} -\frac{R_s + R_f}{L} I_{3\times3} & -\frac{1}{L} I_{3\times3} & -\frac{R_f}{L} \Re_{3\times1} & 0_{3\times1} \\ \frac{1}{c} I_{3\times3} & 0_{3\times3} & -\frac{1}{C} \Re_{3\times1} & 0_{3\times1} \\ \frac{R_f}{L_{dc}} \Re_{1\times3} & \frac{1}{L_{dc}} \Re_{1\times3} & -\frac{R_f}{L_{dc}} \cdot \frac{3}{2} & -\frac{1}{L_{dc}} \\ 0_{1\times3} & 0_{1\times3} & \frac{1}{C_{dc}} & \frac{-1}{R_{dc}C_{dc}} \end{bmatrix} \tag{A.17}$$

where, 0 is a null matrix, I is the Identity matrix and $\Re_{3\times1}$ is a column matrix containing the fundamental components of the three line-to-line switching functions. These functions are

similar to (A.6) and can be given by:

$$\Re_{3\cdot 1} = \begin{bmatrix} S_a(t) = \frac{M\sqrt{3}}{2} \sin(\omega t - \sigma) \\ S_b(t) = \frac{M\sqrt{3}}{2} \sin(\omega t - \frac{2\pi}{3} - \sigma) \\ S_c(t) = \frac{M\sqrt{3}}{2} \sin(\omega t + \frac{2\pi}{3} - \sigma) \end{bmatrix} \tag{A.18}$$

Since the state matrix is 8×8, the conversion matrix must be modified. The new 8×8 conversion matrix is given by:

$$T_{8\cdot 8} = \begin{bmatrix} T_{3\cdot 3} & 0_{3\cdot 3} & 0_{3\cdot 2} \\ 0_{3\cdot 3} & T_{3\cdot 3} & 0_{3\cdot 2} \\ 0_{2\cdot 3} & 0_{2\cdot 3} & I_{2\cdot 2} \end{bmatrix} \tag{A.19}$$

The state variables, inputs and desired outputs (in the abd frame) are as follows:

$$\begin{aligned} X &= \begin{bmatrix} i_a & i_b & i_c & v_{c,a} & v_{c,b} & v_{c,c} & i_{dc} & v_{dc} \end{bmatrix}^T \\ U &= \begin{bmatrix} v_a & v_b & v_c & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \end{aligned} \tag{A.20}$$

After applying the six step procedure described before, the state variables, the state matrix and the control inputs in dqo frame are derived. These are given by:

$$A = \begin{bmatrix} -\frac{R_s + R_f}{L} & -\omega & -\frac{1}{L} & 0 & -\frac{R_f M_o \sin\sigma_o}{L} & 0 \\ \omega & -\frac{R_s + R_f}{L} & 0 & -\frac{1}{L} & \frac{R_f M_o \cos\sigma_o}{L} & 0 \\ \frac{1}{C} & 0 & 0 & -\omega & \frac{M_o \sin\sigma_o}{C} & 0 \\ 0 & \frac{1}{C} & \omega & 0 & -\frac{M_o \cos\sigma_o}{C} & 0 \\ -\frac{3M_o R_f \sin\sigma_o}{2L_{dc}} & \frac{3M_o R_f \cos\sigma_o}{2L_{dc}} & -\frac{3M_o \sin\sigma_o}{2L_{dc}} & \frac{3M_o \cos\sigma_o}{2L_{dc}} & \frac{3R_f}{2L_{dc}} & -\frac{1}{L_{dc}} \\ 0 & 0 & 0 & 0 & \frac{1}{C_{dc}} & -\frac{1}{R_{dc}C_{dc}} \end{bmatrix} \quad \text{(A.21)}$$

The B matrix which is a 3×3 matrix given by:

$$\begin{bmatrix} \frac{R_f M_o \cos\sigma_o I_{dc}}{L} & \frac{R_f \sin\sigma_o I_{dc}}{L} & 0 \\ \frac{R_f M_o \sin\sigma_o I_{dc}}{L} & -\frac{R_f \cos\sigma_o I_{dc}}{L} & \frac{1}{L} \\ \frac{M_o \cos\sigma_o I_{dc}}{C} & \frac{\sin\sigma_o I_{dc}}{C} & 0 \\ \frac{M_o \sin\sigma_o I_{dc}}{C} & -\frac{\cos\sigma_o I_{dc}}{L} & 0 \\ -\frac{3M_o \cos\sigma_o}{2L_{dc}}(V_{do} - R_f I_{do}) - \frac{3M_o \sin\sigma_o}{2L_{dc}}(V_{qo} - R_f I_{qo}) & -\frac{3M_o \cos\sigma_o}{2L_{dc}}(V_{do} - R_f I_{do}) - \frac{3M_o \sin\sigma_o}{2L_{dc}}(V_{qo} - R_f I_{qo}) & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad \text{(A.22)}$$

The state variables and control inputs in dqo frame are:

$$\begin{aligned} \Delta X &= \begin{bmatrix} \hat{i}_d & \hat{i}_q & \hat{v}_d & \hat{v}_q & \hat{i}_{dc} & \hat{v}_{dc} \end{bmatrix}^T \\ \Delta U &= \begin{bmatrix} \hat{\theta} & \hat{m} & \hat{v} \end{bmatrix}^T \end{aligned} \quad \text{(A.23)}$$

A.4.1 Desired Transfer Functions

In order to design the regulators for the schemes proposed in Chapter 4, and 6, the following transfer functions must be calculated:

$$\frac{\hat{v}_{dc}(s)}{\hat{\delta}(s)}, \quad \frac{\hat{v}_{dc}(s)}{\hat{m}(s)}$$
$$\frac{\hat{i}_{d}(s)}{\hat{m}(s)}, \quad \frac{\hat{i}_{q}(s)}{\hat{m}(s)}$$

In order to derive the transfer function from modulation index to output dc voltage, the following matrices must be chosen:

$$c = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1], \quad d = 0,$$

$$b = \begin{bmatrix} \frac{R_f \sin \sigma_o I_{dc}}{L} \\ -\frac{R_f \cos \sigma_o I_{dc}}{L} \\ \frac{\sin \sigma_o I_{dc}}{C} \\ -\frac{\cos \sigma_o I_{dc}}{C} \\ -\frac{3M_o \cos \sigma_o}{2L_{dc}}(V_{do} - R_f I_{do}) - \frac{3M_o \sin \sigma_o}{2L_{dc}}(V_{qo} - R_f I_{qo}) \\ 0 \end{bmatrix} \tag{A.24}$$

For the transfer function from control angle to output dc voltage, the following matricies are obtained:

$$c = [0\ 0\ 0\ 0\ 0\ 1], \quad d = 0,$$

$$b = \begin{bmatrix} \dfrac{R_f M_o \cos\sigma_o I_{dc}}{L} \\ \dfrac{R_f M_o \sin\sigma_o I_{dc}}{L} \\ \dfrac{M_o \cos\sigma_o I_{dc}}{C} \\ \dfrac{M_o \sin\sigma_o I_{dc}}{C} \\ -\dfrac{3M_o \cos\sigma_o}{2L_{dc}}(V_{do} - R_f I_{do}) - \dfrac{3M_o \sin\sigma_o}{2L_{dc}}(V_{qo} - R_f I_{qo}) \\ 0 \end{bmatrix} \tag{A.25}$$

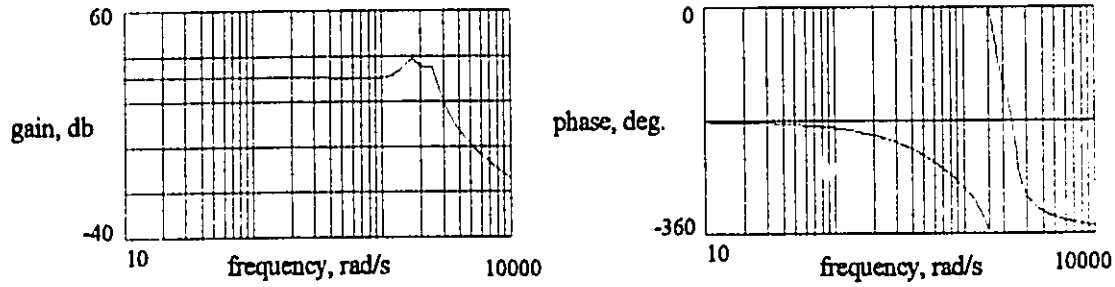

Fig. A.1 Bode plots, $\frac{\hat{v}_{dc}(j\omega)}{\hat{\sigma}(j\omega)}$.

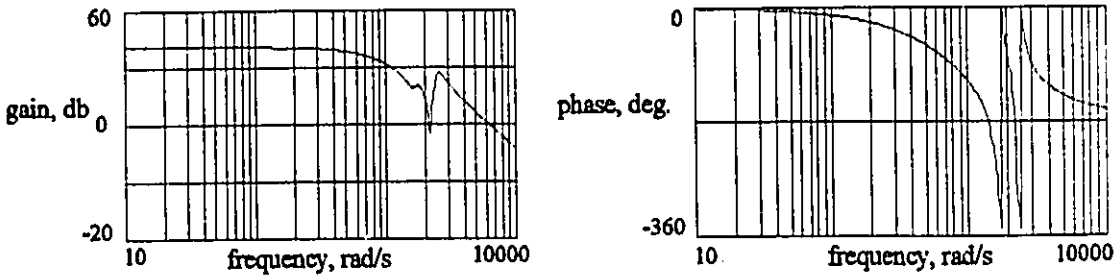

Fig. A.2 Bode plots, $\frac{\hat{v}_{dc}(j\omega)}{\hat{m}(j\omega)}$.

The bode plots obtained from these transfer function are shown in Fig. A.1 and Fig. A.2. The state matrix obtained in (A.15) includes the effect of damping resistors, however if these resistors are eliminated then r_f has to be set to zero.

In ***Chapter 5*** a pattern generation scheme was proposed with inherent damping and the damping resistors were eliminated. For the proposed control scheme, the state matrix is slightly different since the pattern is generated from capacitor voltages. Therefore, the set of three line-to-line switching functions are given by:

$$\Re_{3\cdot 1} = \left\{ \begin{array}{l} S_a(t) = M \dfrac{v_{c,a}(t)}{V} \\ S_b(t) = M \dfrac{v_{c,b}(t)}{V} \\ S_c(t) = M \dfrac{v_{c,c}(t)}{V} \end{array} \right\} \tag{A.26}$$

Also, the new state matrix is given by:

$$A = \begin{bmatrix} -\dfrac{R_s}{L} & -\omega & -\dfrac{1}{L} & 0 & 0 & 0 \\ \omega & -\dfrac{R_s}{L} & 0 & -\dfrac{1}{L} & 0 & 0 \\ \dfrac{1}{C} & 0 & -\dfrac{M_o I_{dco}}{C V_o} & -\omega & \dfrac{M_o \sin\sigma_o}{C} & 0 \\ 0 & \dfrac{1}{C} & \omega & -\dfrac{M_o I_{dco}}{C V_o} & -\dfrac{M_o \cos\sigma_o}{C} & 0 \\ 0 & 0 & -\dfrac{3M_o \sin\sigma_o}{2L_{dc}} & \dfrac{3M_o \cos\sigma_o}{2L_{dc}} & 0 & -\dfrac{1}{L_{dc}} \\ 0 & 0 & 0 & 0 & \dfrac{1}{C_{dc}} & -\dfrac{1}{R_{dc}C_{dc}} \end{bmatrix} \tag{A.27}$$

Finally, the new B matrix is:

$$\begin{bmatrix} \frac{R_f M_o \cos\sigma_o I_{dc}}{L} & \frac{R_f \sin\sigma_o I_{dc}}{L} & 0 \\ \frac{R_f M_o \sin\sigma_o I_{dc}}{L} & -\frac{R_f \cos\sigma_o I_{dc}}{L} & \frac{1}{L} \\ \frac{M_o \cos\sigma_o I_{dc}}{C} & \frac{\sin\sigma_o I_{dc}}{C} & 0 \\ \frac{M_o \sin\sigma_o I_{dc}}{C} & -\frac{\cos\sigma_o I_{dc}}{L} & 0 \\ -\frac{3M_o \cos\sigma_o}{2L_{dc}}(V_{do} - R_f I_{do}) - \frac{3M_o \sin\sigma_o}{2L_{dc}}(V_{qo} - R_f I_{qo}) & -\frac{3M_o \cos\sigma_o}{2L_{dc}}(V_{do} - R_f I_{do}) - \frac{3M_o \sin\sigma_o}{2L_{dc}}(V_{qo} - R_f I_{qo}) & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad \text{(A.28)}$$

The bode plots depicted in Figs. A.3 and A.4 clearly show the effect of this scheme in the damping of the system (compare with Figs. A.1 and A.2).

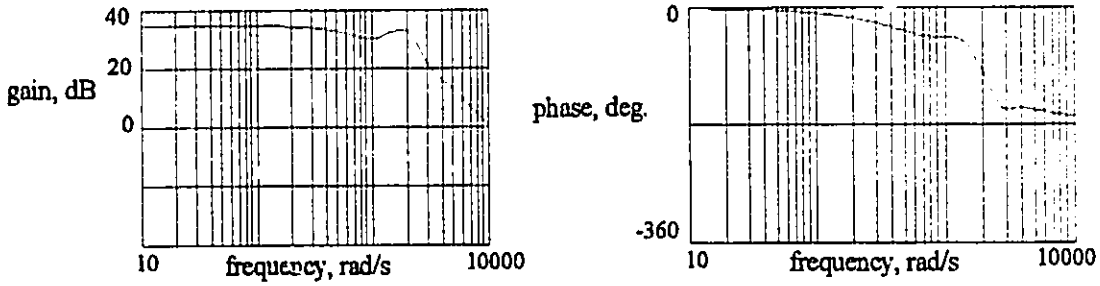

Fig. A.3 Bode plots, $\frac{\hat{v}_{dc}(j\omega)}{\hat{\sigma}(j\omega)}$.

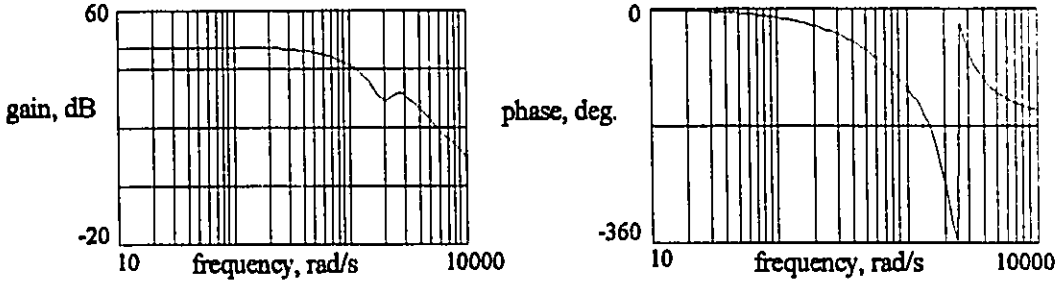

Fig. A.4 Bode plots, $\frac{\hat{v}_{dc}(j\omega)}{\hat{m}(j\omega)}$.

APPENDIX B

B.1 Experimental Set-Up for Testing a Non-Regenerative Current Source Rectifier

For non-regenerative applications such as dc power supplies or ac drives without regeneration capability, the six series diodes can be removed from the bridge circuit and rearranged as a high frequency three-phase diode rectifier, Fig. B.1. This topology is used in the experiments in ***Chapters 4*** and ***5*** since it can be easily implemented by re-configuring a standard VSI. This arrangement has two obvious advantages:

- The high frequency diode bridge rectifier can be manufactured separately and then be added to an existing voltage source topology converter.
- Since the two switches on the same leg are connected back-to-back, they can be gated with a common signal. This signal is produced according to:

$$Gate_{1} = Gate_{4} = S_{trl,1} \cup S_{trl,4} \tag{B.1}$$

where $Gate_1$ and $Gate_4$ denote the gatings of the corresponding switches and $S_{trl,1}$ is the

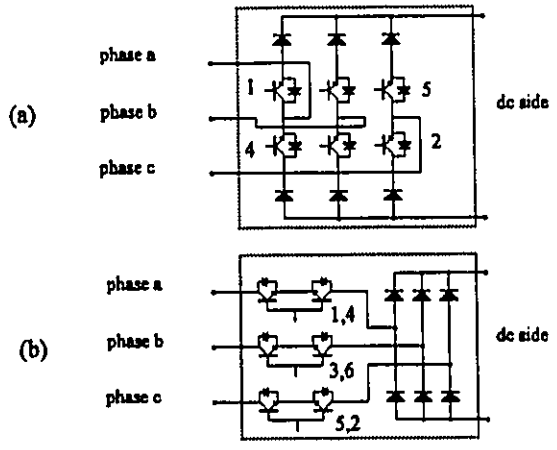

Fig. B.1 (a) Standard PWM rectifier, (b) proposed non-regenerative topology.

basic line-to-line switching function which was described in ***Chapter 4***. In this way only three base drives are needed to operate the six switch converter. Generation of the line to line pattern is sufficient to operate the switches, since short circuit path is provided by the output diode rectifier. The gating signal which is applied to both switch 1 and 4 is depicted in Fig. B.2.

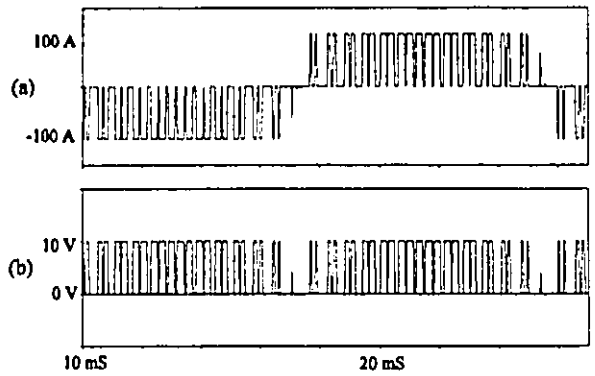

Fig. B.2 (a) Rectifier input current, (b) gating signal applied to switch 1 & 4.