THE DESIGN AND IMPLEMENTATION OF AN UNDERWATER ACOUSTIC TELEMETRY SYSTEM DECK UNIT

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ABSTRACT

AN UNDERWATER ACOUSTIC TELEMETRY SYSTEM
DECK UNIT

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This thesis describes the design and development of the receiver of an underwater acoustic telemetry system. It begins with a summary of the dispersion problems associated with underwater communications followed by an in-depth look at the hardware and software of the system. The hardware description includes a detailed look at the Fast Fourier Transform processor and Time Synchronizer. Also covered are the software algorithms for doppler correction, time estimation, tone demodulation and error correction. Finally some test results obtained from sea trials and some suggestions for improvements and applications are presented.

ACKNOWLEDGEMENTS

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CHAPTER I

INTRODUCTION

A significant disadvantage of measuring tides with bottom-mounted gauges is that the tidal information can be obtained only upon recovery of the instrument at the completion of the survey. This disadvantage may be overcome by the use of an ocean bottom-mounted tide gauge which can transmit to the survey ship, on demand, the tidal information gathered over several weeks. A device of this type allows the hydrographer to maintain an up-to-date account of corrected soundings and greatly expedites the progress of a hydrographic survey, especially in the Artic. To this end, a prototype acoustic telemetry system has been developed and tested by Concordia University for the Bedford Institute of Oceanography, Dartmouth, Nova Scotia. The system consists of two parts: the bottom-mounted unit which collects tidal data and transmits it to the Deck unit upon request, and the Deck unit described in this thesis which is responsible for receiving and demodulating the information transmitted from the Bottom unit, while correcting for frequency and temporal dispersion of the underwater environment.

The sea is far from an ideal sound-propagation medium [I.1]; sound-waves, apart from being contaminated by noise, also suffer from time and frequency dispersion. Time dispersion, or multipath, is due to the reflections of the rays by the surface and bottom before reaching the receiver. Sound signals travel different paths, and as a result, arrive at different instants at the receiver, thus extending the duration of transmission. A second form of dispersion, frequency dispersion, is caused by reflection of the rays from the ocean surface. Frequency dispersion is dependent on the roughness of the ocean surface and it

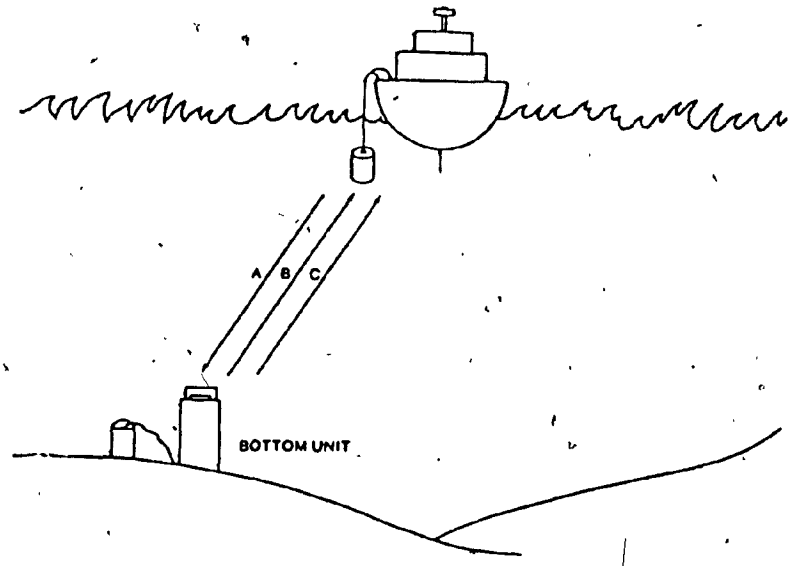
can result in angle or amplitude modulation of the incident tone [I-2]. Besides these two dispersions that are introduced by the medium, doppler shift is also present. Doppler shift is present whenever there is relative motion between transmitter and receiver.

The effect of doppler shift is to make frequency tones transmitted appear to be of another frequency, due to expansion or contraction of the time axis. Signal strengths fluctuate greatly as severe fading can occur. This effect is minimized by employing five-fold frequency diversity in the Bottom unit. In order to achieve reliable communications between the Bottom and Deck unit, care must be taken in the design to account for the time and frequency dispersion, doppler shift, and signal fading. A method to predict the beginning and the end of transmission must be incorporated in the design. Tones arriving at the receiver must be adjusted for frequency spreading and shifting. Fluctuations in signal strength must be overcome by continuously optimizing the gain of the amplifiers.

Each of these problems is addressed in the design of the telemetry system. To allow for multipath decay, the Bottom unit transmits for 125 ms followed by 125 ms of dead time. Four pilot tones are transmitted during all transmissions, and the presence of these tones is used in predicting the time of transmission of the next batch of data. To correct for frequency dispersion, the Deck unit processing considers the energy adjacent to the tones received, in effect increasing the bandwidth of the received narrow band filters. For doppler shift, the pilot tones are examined for average change to correct frequency shift and changes are made to the local voltage-controlled oscillator. Fading

is minimized by employing 5-fold diversity in the modulation scheme of the Bottom unit, and an efficient gain adjustment system in the Deck unit.

As described earlier, the telemetry system consists of an ocean Bottom unit and a Deck unit placed on board a survey ship as shown in Figure I.1a. The Bottom unit, which is moored to the ocean floor, is continuously collecting tidal data which it stores in its memory. When the survey ship carrying the Deck unit comes within range of the Bottom unit, an interrogation command is sent from the Deck unit to the Bottom unit. The interrogation command consists of a 250 ms tone burst which contains five tones spaced 400 Hz apart in a 2048 Hz bandwidth centered at 8192 Hz.



A. 250 ms ALERT PREAMBLE
B. 16 PHASE SYNCHRONIZATION PREAMBLE
C. MESSAGE $P \approx 10^{-4}$

Fig.I.1 (a) THE INTERROGATION ARRANGEMENT BETWEEN THE DECK AND BOTTOM UNIT

The Bottom unit is designed with the necessary hardware and software algorithms to recognize the interrogation pattern. The Bottom unit then transmits 16 preambles, each of 125 ms, followed by 125 ms of dead time. These preambles enable the Deck unit to estimate time dispersion, signal strength, doppler shift, and make the appropriate corrections. Following these 16 preambles, the Bottom unit sends up the tidal data. A dense MFSK modulation scheme in which M=4 and the number of frequency diversity channels D=5 is employed to convert tidal and coded data into frequency tones. In this method each 16-bit data word is converted into 40 tones from a set of 160 tones. Four pilot tones are interleaved between the 5 diversity channels, for a total of 44 tones as shown in Figure I.2.

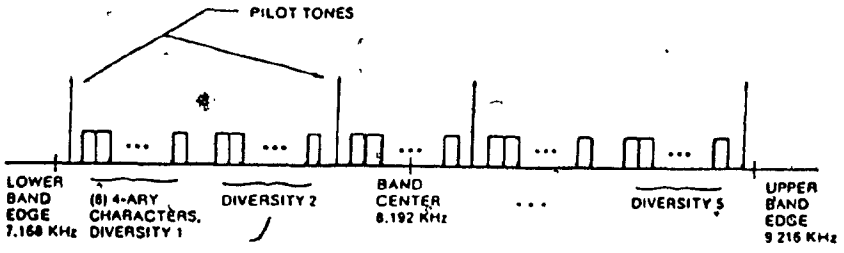


Fig. I.2 PILOT TONES AND DATA SPECTRAL ALLOCATIONS

The analog and digital hardware employed to receive and demodulate the tidal data in the Deck unit is shown in Figure I.3.

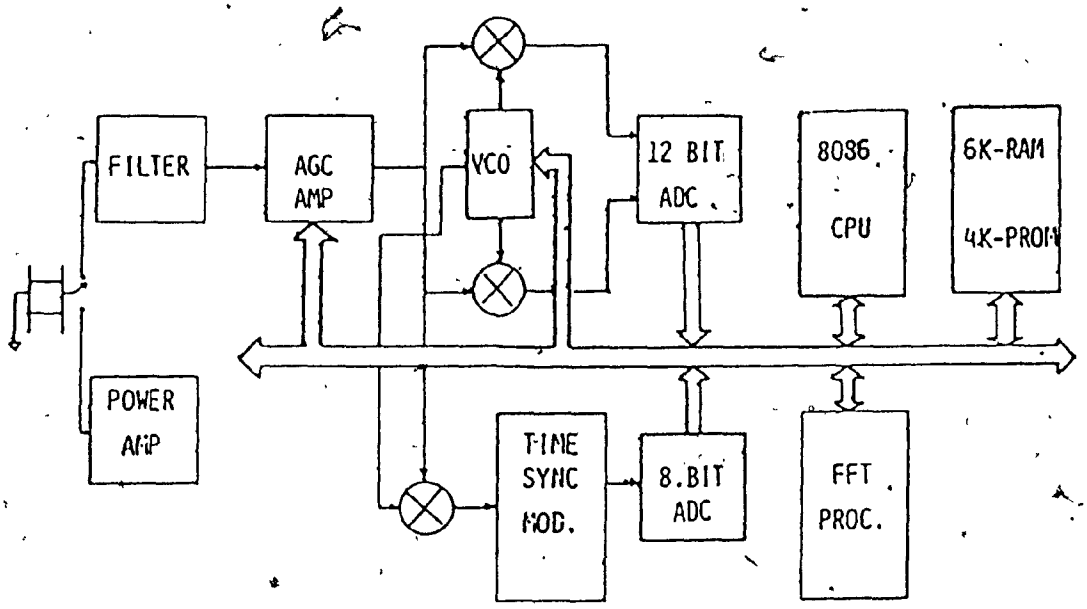


Fig. I.3 BLOCK DIAGRAM OF DECK UNIT

An INTEL 8086 16-bit microprocessor provides all the control and processing required. A 512-point complex FFT processor is used to demodulate the MFSK tones to bits. Time synchronization is provided by the synchronizer module. Other hardware consists of data storage memory, analog hardware in the preprocessor for automatic gain control (AGC), and a voltage controlled oscillator (VCO) circuitry for doppler correction. The Deck unit includes an RS232 serial output port for data transfer and a tone generator and power amplifier for interrogation of the Bottom unit.

CHAPTER I

REFERENCES

I.1 Quazi Azizul H., and William L. Konrad, "Underwater Acoustic Communication", IEEE Communications Magazine, Vol. 20, No. 2, March 1982.

I.2 Morgera, S.D., "Optimum Underwater Acoustical Telemetry Techniques", Prepared for Canadian Department of Environment, Oceans and Fisheries, Contract 07SC.KF806-8-E330, 28 February 1979.

CHAPTER II

THE ACOUSTIC CHANNEL

II.A. INTRODUCTION

The sea is far from the ideal sound propagation medium. Sound waves, apart from being obscured by noise, also suffer time and frequency dispersion. [II.A.1.]. Time dispersion or multipath spread is due to multiple reflection of rays from the ocean surface and bottom before reaching the receiver. Sound signals transmitted take different paths and, as a result, arrive at different time instants at the receiver. Frequency dispersion is caused by reflection from the ocean surface and second-order relative transmitter-receiver motion effects. [II.A.2.]. The effect of these two phenomena on the received signal must be considered in the design of the transmitter and receiver. If the amount of dispersion can be reasonably predicted a communication system can be designed to accomodate.

Two other parameters inherent in acoustic propagation must also be addressed, transmission loss and noise. Transmission loss is caused by spherical spreading of the beam, absorption, and interfering multipaths. [II.A.3.]. To account for this loss, sufficient gain must be designed into the Deck unit, as well as enough transmitter power in the Bottom unit. Noise includes shallow water ambient noise (water depth less than 300 m) due to temperature and wind, and noise radiated into the water by machinery. [II.A.2.]. Bottom unit transmitter power should be sufficient to provide sufficient signal above the noise level at the receive hydrophone.

Doppler shift is a source of error in this system since the relative movement of the transmitter and receiver causes time expansion and compression. These five parameters will be studied in this chapter and estimates calculated.

The requirements for the Deck unit will then be presented in accord with these estimates.

II.B PROPAGATION LOSS AND NOISE

II.B.1 INTRODUCTION

The performance of a one-way acoustic communications system is described by Equation (II.B.1),

$$(S/N)_{receiver} = L_S + (N_{DI})_R - T_L - L_N \qquad \text{(II.B.1)}$$

where $(S/N)_{receiver}$ is the signal-to-noise ratio at the receiver; L_S is the source level; T_L is the transmission, or propagation, loss; and L_N is the noise level in the band of interest. The term $(N_{DI})_R$ is the directivity index of the receiver. [II.A.3.].

Each of the terms in (II.B.1) is dependent on other factors. These relationships are shown below in (II.B.2) and (II.B.3).

II.B.2 SOURCE LEVEL

The source level is dependent on the directivity, and the acoustic conversion efficiency of the transmitting hydrophone, i.e.,

$$L_S = 10 \log(\beta p) + 71.5 + (N_{DI})_T \qquad \text{(II.B.2)}$$

where β is the electroacoustic conversion efficiency, the factor 71.5 provides the conversion from watts to dB//1μbar, and $(N_{DI})_T$ is the directivity index of the transmitter.

II.B.3 TRANSMISSION LOSS

The transmission loss (T_L) for short distances of 1 to 2 kilometers is determined by the spherical spreading loss, absorption, and other factors due to multipath scattering,

$$T_L = 20 \log R + \alpha R + (60-K_L) \qquad \text{(II.B.3)}$$

where R is the range; the first term, 20 log R is the loss due to spherical spreading of the wave; in the second term, α is the frequency-dependent absorption coefficient; and the final term, the multipath structure. The coefficient α is a function of frequency, temperature, salinity, and pressure. However, the dominant contribution to transmission loss is the attenuation of the direct path due to spherical spreading and absorption. [II.A.3.]. Table II.B.1 summarises the transmission loss for two Bottom types and three temperature ranges.

		Sea State and Bottom Type											
		0		1		2		3		4		5	
	T(°C)	Sand	Mud	Sand	Mud	Sand	Mud	Sand	Mud	Sand	Mud	Sand	Mud
7 kHz	-10	57.4	57.9	58.7	59.2	59.0	59.5	59.4	60.1	59.7	60.1	59.9	60.3
	0	56.9	57.4	58.2	58.7	58.5	60.0	58.9	59.6	59.2	59.6	59.4	59.8
	10	56.5	57.0	57.8	58.3	58.1	58.6	58.5	59.2	58.8	59.2	59.0	59.4
16 kHz	- 10	61.2	61.7	62.2	62.6	62.4	62.9	62.7	63.0	62.9	63.3	63.1	63.4
	0	59.5	60.0	60.5	60.9	60.7	61.2	61.0	61.3	61.2	61.6	61.4	61.7
	10	58.7	59.2	59.7	60.1	59.9	60.4	60.2	60.5	60.4	60.8	60.6	60.9

TABLE II.B.1 SHALLOW WATER TRANSMISSION LOSS (dB)

The effect of temperature, bottom type and sea state is slight as shown in Table II.B.1. Table II.B.2 is a condensed version of Table II.B.1 showing the corresponding worst case attenuation for R=1 and 2Km. [II.A.3.]

		SEA STATE					
	f(KHz)	0	1	2	3	4	5
R = 1 Km	7	57.9	59.2	59.5	60.1	60.1	60.3
	16	61.7	62.6	62.9	63.0	63.3	63.4
R = 2 Km	7	65.2	66.5	66.8	67.4	67.4	67.6
	16	71.6	72.5	72.8	72.9	73.2	73.3

Table II.B.2 SHALLOW WATER TRANSMISSION LOSS FOR R=1 AND 2 KM, T=-10°C, AND MUD BOTTOM

II.B.4 BANDLEVEL NOISE

The bandlevel noise, L_N, is the ambient noise which obscures the signal. Ambient noise in shallow water is at least 10 dB higher than noise in deep-water. Other factors such as oil drilling rigs can contribute as much as 20 dB of additional noise. [II.A.3.]. Table II.B.3 summarises the ambient noise in shallow water of a depth less than 300 meters, for six sea states, and two transmitting frequencies. The total loss figure (T_L+L_N), for six sea states, two transmitting frequencies and two ranges is shown in Table II.B.4. [II.A.3.].

	SEA STATE					
Frequency	0	1	2	3	4	5
7 kHz	-25.39	-16.29	-11.09	-7.29	-4.39	-1.99
16 kHz	-31.49	-22.39	-17.19	-13.39	-10.49	-8.09

Table II.B.3 SPECTRUM LEVEL OF SHALLOW WATER AMBIENT NOISE (dB//1μbar/Hz)

		Sea State					
	f(KHz)	0	1	2	3	4	5
R = 1 Km	7	32.5	42.9	48.4	52.8	55.7	58.3
	16	30.2	40.2	45.7	49.6	52.8	55.3
R = 2 Km	7	39.8	50.2	55.7	60.1	63.0	65.6
	16	40.1	50.1	55.6	59.5	62.7	65.2

Table II.B.4 LOSS FIGURE $(TL + L_N)$ (dB)

From these figures it is evident that the source level plus the directivity index must exceed the total loss by a sufficient amount for reliable communications.

II.C.1 TIME DISPERSION

A serious problem in underwater sound transmission is the temporal distortion that occurs as a result of multipath. Closely spaced multipath distortion (time smear) also occurs because of forward scattering in the medium. This scattering is the result of thermal microstructures.i.e. small volumes of water at different temperatures [II.A.3.]. It is difficult to describe the precise decay of multipaths relative to the decay of the direct path, because of a lack of experimental data. The geometry of ray paths indicates that the higher order rays which undergo many reflections from the surface and bottom before reaching the receiver, make steeper angles with the boundary surfaces than the lower rays and, consequently suffer greater bottom absorption and surface scattering. Also, the paths of higher order rays are longer than lower order rays and suffer greater attenuation from spherical spreading and absorption over the total path length [II.A.3.].

One obvious solution to eliminate multipath arrival, is by combining careful signal design and the use of transducers arrays that form directional beams. Directional receiving beams discriminate against energy outside of the intended arrival direction, and directional transmit beams project the energy so that the minimum number of possible propagation paths are excited. However the conventional acoustic source usually radiates side lobes although at a lower level than the main beam, may still cause multiple arrival. A parametric source however is capable of reducing a narrow beam with very low side lobe levels [II.A.1.] . The use of directional beams involves the exact orientation of the hydrophones, which in this application is not possible, as the receiver hydrophone is constantly being moved by the ship and current. To minimize cost, simple transducers are used therefore a good estimate of multipath

spread is required. The waveform received at the vehicle may be expressed as

$$y(t) = \sum_{n=1}^{N} a_n \, x[t - \tau_n(t)] \qquad \text{(II.C.1)}$$

where $x(t)$ is the transmitted waveform, $\{\tau_n(t)\}$ is the set of propagation path delays, and $\{a_n\}$ is the set of respective path amplitudes. Multipath spread may be simply calculated as $(\tau_n - \tau_1)$ where τ_n is the nth path and τ_1 is the direct path. This is not a realistic approach as it gives equal weight to nth path even though the nth path has lost much of its energy due to reflection and absorption. A better approach to determine multipath spread would be to calculate the path delays for a set of selected paths. [II.A.3.].

$$\bar{\tau} = \frac{1}{N} \sum_{\omega \in \Omega_r} \tau_\omega \qquad \text{(II.C.2)}$$

$$L = \left[\frac{1}{N'-1} \sum_{\omega \in \Omega_r} (\tau_\omega - \bar{\tau})^2\right]^{\frac{1}{2}} \qquad \text{(II.C.3)}$$

where $\bar{\tau}$ is the mean path delay and L is the estimate of the multipath spread. The symbol Ω_r denotes the set

$$\Omega_r = \{\omega | \frac{a\omega}{a_1} \geq r: \text{where} \quad \omega = 1,2,\ldots N\} \qquad \text{(II.C.4)}$$

A more complicated estimate is one in which both the propagation loss and delay profiles are taken into consideration as shown in II.C.5 and II.C.6.

$$\bar{\tau} = \sum_{n=1}^{N} a_n^2 \tau_n \Big/ \sum_{n=1}^{N} a_n^2 \qquad \text{(II.C.5)}$$

$$L = \left[\sum_{n=1}^{N} a_n^2 (\tau_n - \bar{\tau}) \right] / \sum_{n=1}^{N} a_n^2 \qquad \text{(II.C.6)}$$

Seven geographical locations were designated by the Bedford Institute of Oceanography as typical areas of interest. The sound velocity profiles (SVP) are shown in Figure II.C.1. The specific geographical locations are listed below.

SVP A Typical winter profile

SVP B Centre of Hudson Bay (summer)

SVP C Hudson Bay near Churchill (summer)

SVP D Main Bank 57°-17.0'N, 60°-0.18'W

SVP E Main Bank 57°-9.5'N, 60°-31.6'W

SVP F Off Nova Scotia 43°-0.6'N, 63°-30.5'W

SVP G Lancaster Sound 74°-36.6'N, 94°-20.4'W

The multipath spread (L) using the SVP's for the above regions were estimated and tabulated in Table II.C.1 [II.A.3.].

Multipath order n	Description	R_n(Km)	ΔR_n(m)	$\Delta\tau_n$(ms)	θ_n(deg)
0	direct path	1.8288	0	0	0
1	S	1.8291	0.3	0.2	1
2	S-B	1.8654	36.6	24.8	11
3	S-B-S	1.8745	45.7	30.9	12
4	S-B-S-B	1.9660	137.2	92.8	22
-1	B	1.8593	30.5	20.6	10
-2	B-S	1.8654	36.6	24.8	11
-3	B-S-B	1.9658	137.0	92.7	21
-4	B-S-B-S	1.9660	137.2	92.8	22

Table II.C.1 WORST CASE TIME DISPERSION (S = SURFACE REFLECTION, B = BOTTOM REFLECTION) R_n = PROPAGATION DISTANCE, ΔR_n = PROPAGATION PATH LENGTH DIFFERENCES, AND θ_n = GRAZING ANGLE

The geometry of ray paths indicates that the higher order rays, which undergo many reflections from surface and bottom before reaching the receiver, make steeper angles with the boundary surfaces than lower order rays and consequently, suffer greater bottom absorption and surface scattering. Also, the paths of higher order rays are longer than lower order rays and suffer greater attenuation from spherical spreading and absorption over the total path length. If the energy due to multipaths higher than third or fourth order are considered negligible then the worst case time dispersion occurring when both the transmitter and receiver are at a relatively shallow depth is on the order of 30 to 100 milliseconds [II.A.3.].

II.D FREQUENCY DISPERSION

II.D.1 INTRODUCTION

Another important influence on the received waveform is frequency dispersion. Frequency dispersion is caused by reflection of the waves from the ocean surface and by the vertical and axial motion of the vehicle on which the Deck unit is placed. Morgera [II.A.3.] has studied these two effects and has estimated a frequency spread for the telemetry system for different sea states. What follows is a summary of this work.

Frequency dispersion (B_s) due to the reflected spectrum is dependent on the surface roughness, which is proportional to the Rayleigh number $r\omega$. The surface is divided into three categories-smooth, moderately rough surface, and rough surface. The Rayleigh numbers $r\omega < 1$, $= 1$, and >1 characterize these three surfaces, respectively. A time-varying surface produces different forms of modulation on an incident tone, as shown in Figure II.D.1. At low Rayleigh numbers, angle modulation dominates and discrete sidebands are produced. At high Rayleigh numbers, both angle and amplitude modulation are present, resulting in smeared higher order sidebands [II.A.3.].

The frequency dispersion caused by the reflection from the ocean surface at angles of 3° and 6°, for three sea states was determined using Bi-frequency functions and various Rayleigh numbers. As shown in Table II.D.1 for the 7 KHz frequency signal frequency dispersions of 0.9 Hz to 3.0 Hz were estimated. [II.A.3.].

f(KHz)	SS 2-3, $\theta = 3^0$	SS 4, $\theta = 6^0$
7	0.9	3.0
16	1.9	6.8

Table II.D.1 FREQUENCY DISPERSION (B_s) in Hz

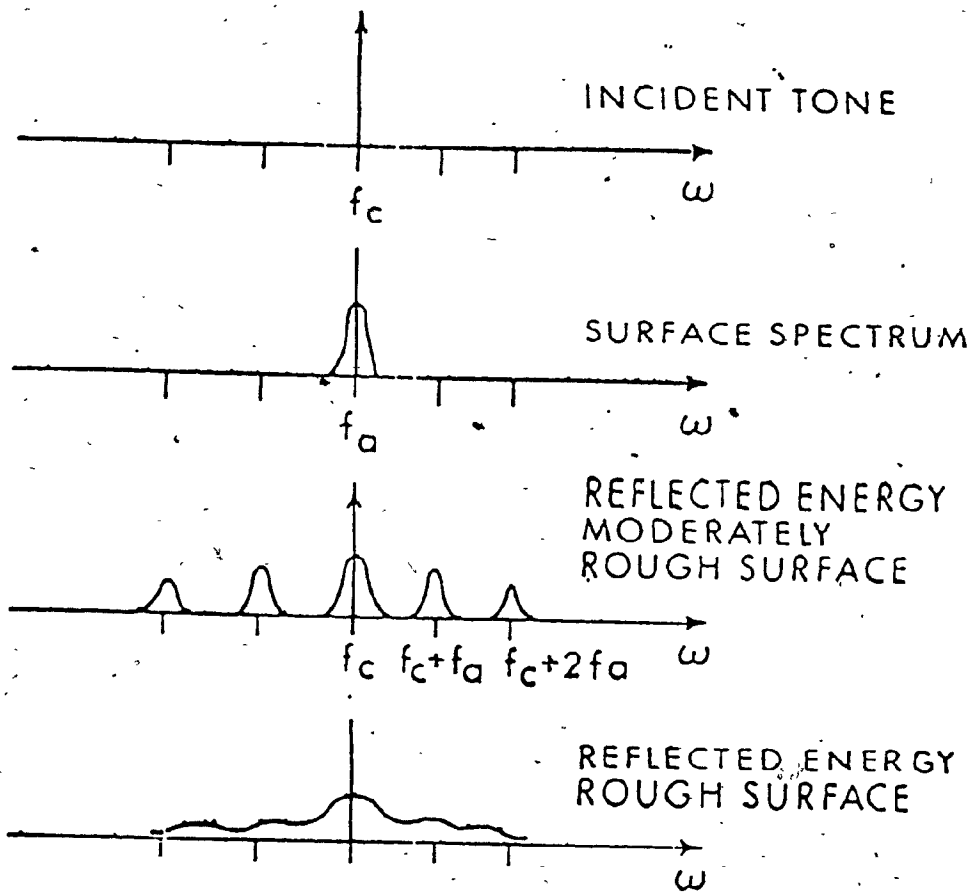


Fig. II.D.1 SURFACE REFLECTED SPECTRUM

II.D.2 FREQUENCY DISPERSION DUE TO VEHICLE MOTION

Frequency dispersion due to vehicle motion is difficult to estimate. The analysis is lengthy and complex and based on many assumptions. [II.A.2.]. The study was carried out for a vehicle movement in two axes, i.e., the horizontal axis (normal axis motion) and vertical axis (normal translation or pitch). The calculations are based on a vehicle horizontal motion of 5 knots and current of 2 knots. The vertical motion was set at 1 to 2 meters with a period of 10 to 20 seconds.

An indepth analysis is not attempted here save to say that each reflected path due to vehicle motion is essentially a frequency (angle) modulated signal. Higher order sidebands with little energy and higher order paths having weak signals are not considered. Morgera, using the ray path structures for the seven sound velocity profiles (SVP), calculated the frequency spread (B_V) for two distances and 4 vehicle speeds. The results of this calculation are shown in Table II.D.2. [II.A.2.].

	R = 1.094 Kyd, 2.187 Kyd			
SVP	V = 0.1 Kt	1 Kt	2 Kt	5 Kt
	SSO SS4			
A	.14, .18	1.38,1.79	2.70,3.60	6.70,9.00
B	.19, .15	1.88,1.50	3.75,3.00	9.40,7.40
C	.17, .16	1.65,1.63	3.26,3.26	8.20,8.15
D	.15, .23	1.45,2.25	2.95,4.58	7.40,11.30
E	.17, .14	1.70,1.40	3.40,2.84	8.60,7.00
F	.14, .14	1.43,1.38	2.85,2.80	7.10,7.00
G	.19, .14	1.90,1.46	3.80,2.74	9.50,6.70

Table II.D.2 DOPPLER SPREAD DUE TO VEHICLE MOTION B_V(HZ) FOR TWO COMMUNICATION RANGES AND OPTIMUM RECEIVER DEPTH D*

The data in Table II.D.1 for B_s and Table II.D.2 for B_v provide some guidelines for the Deck unit design. In comparing the doppler spread B_s due to surface scattering and the doppler spread B_v due to vehicle-current motion the following points are noted:

(1) for sea state (SS) 2 and 3 conditions, B_v is the dominant spreading component except at very low vehicle-current velocities. (<1 knot).

(2) - for SS4 conditions, B_s is the dominant component except at vehicle-current velocities in excess of 3 knots.

Since relatively high sea states are to be expected, an attempt must be made to maintain vehicle-current velocity below about 3 knots and use a receive frequency resolution consistent with the combined estimates of B_s and B_v. [II.A.2]. The combined estimate B, (the RMS sum of B_s and B_v) for a vehicle speed of 5 knots is 8.3 Hz for SSO (averaged over geographical locations) and 8.8 Hz for SS4. Whereas, for the lower speed of 2 knots B = 3.41 Hz for SSO and B=4.45 Hz for SS4. These estimates are used in Section II.E. to determine the frequency resolution and pulse time duration requirements of the system. [II.A.2.].

II.D.3 DOPPLER SHIFT

In Section II.D.2 it is shown that vehicle-current motion results in frequency dispersion of the transmitted signal. Vehicle-current movement is also responsible for doppler shift. Doppler shift is the contraction or expansion of the time axis due to the relative velocity between the receiver

and transmitter. It is a function of the relative velocity, velocity of sound in the medium, and the operating frequency. [II.D.1.].

$$\Delta f = \frac{V}{C} f$$

where v is the relative velocity, C is the velocity of sound in water and f is the operating frequency.

In practical terms,

$$\Delta f = \pm .345 \text{ Hz/knot } [f(\text{KHz})]$$

for the operating frequency of 8.192 kHz, we have

$$\Delta f = \pm 2.82 \text{ Hz/knot}$$

which, for a vehicle velocity of $\pm$ 4 knots and current velocity of $\pm$ 2 knots becomes,

$$\Delta f = \pm 16.96 \text{ Hz maximum}$$

The $\pm$ sign indicates that the approaching ship produces a higher frequency (time compression) and a receding ship produces a lower frequency (time expansion).

The band of the transmitted signal covers 2048 Hz; therefore the maximum doppler will vary from 14.83 Hz to 19.0 Hz. Correction for doppler shift as will be explained in Section III.D. is based on the average shift in the band.

II.E. SYSTEM REQUIREMENTS

In the previous sections, environmental parameters which affect underwater acoustic communications were discussed. These estimates determine the system requirements of both the Bottom and Deck units. For reliable communication, the Bottom unit must provide adequate signal levels in order that sufficient signal levels are received by the Deck unit. The Deck unit, on the other hand, must have sufficient dynamic gain to accomodate different signal levels. Time uncertainty, L, and frequency uncertainty, B, will determine the transmitted pulse duration and frequency resolution of the tones transmitted by the Bottom unit. Frequency spread must be considered in the Deck unit if accurate evaluation of tonal energy is to be made. Doppler shift can be minimised by keeping low vehicle speeds ($\leq$ 3 knots) and corrected by the use of specialised hardware in the Deck unit.

The telemetry system utilises MFSK signalling with M=4 - ary characters, N=8 characters per baud, and D=5 - fold frequency diversity. The required error probability per 16-bit message is $\approx 10^{-4}$. [II.E.1.]. To achieve this, average total and average per tone received energy-to-noise power density ratios per message are 30 dB and 14 dB, respectively. A (32,16) quasi-cyclic code provides a net signal-to-noise ratio gain (coding gain) of 3.6 dB. Therefore, the S/N requirements are reduced to 26.4 dB total and 10.4 dB per tone. [II.E.1.]. After correction for the pulse length of 125 ms, the average S/N required is 22.43 dB/tone. Table II.E.1 summarises the signal power-to-noise power density ratio per tone (dB) at 8 kHz for SS0 and SS4 at two communications ranges. [II.E.1.].

	R = 1.094 Kyd				R = 2.187 Kyd			
	PL(coh)		PL(incoh)		PL(coh)		PL(incoh)	
SVP	SSϕ	SS4	SSϕ	SS4	SSϕ	SS4	SSϕ	SS4
A	24.0	21.3	28.0	25.3	14.0	10.3	21.1	18.3
B	22.4	20.9	30.5	30.5	32.7	32.5	30.8	30.8
C	29.2	25.6	28.4	32.9	24.9	0.2	24.1	5.9
D	35.7	31.6	32.0	29.3	17.1	18.6	24.3	19.9
E	9.6	24.5	28.9	26.2	24.1	20.6	23.9	21.3
F	27.4	22.7	27.2	24.3	22.3	18.0	18.2	14.9
G	(SS3)	20.1	26.8		7.2		9.9	

Table II.E.1 AVAILABLE SIGNAL POWER-TO-NOISE POWER DENSITY RATIO PER TONE (dB) AT 8 KHz FOR VARIOUS ENVIRONMENTAL PARAMETERS AND TWO COMMUNICATIONS RANGES

The averages of the coherent and incoherent S/N ratios of Table II.E.1 indicate that the signal-to-noise ratios per tone at the Deck unit are between 23.3 dB and 34.25 dB at a range of 1.094 Kyd for sea state 0 and sea state 4 respectively. This range of signal-to-noise ratios is adequate to meet the requirement of 22.43 dB for an error probability of $\approx 10^{-4}$. The S/N ratio is also satisfied for most of the cases at the longer communications range of approximately 2 Kyd. The Bottom unit is equipped with a transmitter capable of delivering 6.2 watts of power, sufficient for reliable communications at distances up to 2 Kyd. [II.E.1.].

To determine the fixed and variable gain required in the Deck unit, a knowledge of the received signal levels will be required. From Table II.B.1 the maximum propagation loss, (PL) is 63.4 dB at 1094 yds. Using the PL loss graphs from [II.A.2.] we obtain a propagation loss of 30 dB for a distance of 100 yds. This implies that the gain can change by as much as 33.4 dB depending on the range. Since the ship can be moving towards or away from the Bottom Unit, there is a need for gain adjustment during transmission.

Signal levels at the transducer at a transmission range of 1 Kyd with a Bottom unit transmitter output of 6 watts varies from 119μV to 11.9 mV per tone depending on the propagation loss [II.E.2.]. The lowest signal level of 119μV/tone requires 98.5 dB gain to produce a 10-Volt signal at the input to the analog-to-digital convertor. Since there are 44 tones, a 16.43 dB (10 log 44) reduction in gain is required. Therefore, the maximum gain of the preprocessor should be 82.07 dB of which 33.4 dB is variable.

Frequency spread B was estimated in Section II.C. for two vehicle speeds. For a vehicle speed of 5 knots the spread was 8.3 Hz to 8.8 Hz depending on the sea state, but for low speeds of 2-3 knots, the estimates ranged from 3.41 Hz to 4.45 Hz. The lower speed estimates are relevant to this application as the ship is expected not to exceed 3 knots. The Bottom unit transmits data for 125 ms in a 250 ms period; as a result, the transmitted tones have a bandwidth of 8 Hz (1/.125 Hz). The tones arriving at the receiver will be approximately 12 Hz wide. The Deck unit performs a spectral analysis of the received signal by passing it through a bank of 6 Hz-wide filters. To consider the total

energy of the received tone, the Deck unit adds half the energy from the tone bins adjacent to the received tone, in effect increasing the bandwidth of the filters to 12 Hz. The software algorithm to implement this conversion is described in Chapter IV.

In Section II.D.3, doppler shift for a vehicle and current velocity of $\pm$6 knots was calculated to be $\pm$16.96 Hz. The Deck unit must incorporate circuitry for this doppler shift. Since it is practically impossible for changes in ship's speed to occur instantaneously, sudden doppler shifts will not occur. It is adequate if doppler corrections are made once every 1/2 second, which is the time required to transmit one 16-bit data word and its 16-bit code word.

To summarise, the requirements for the Deck unit due to environmental conditions are the following:

(1) Signal amplification up to 82 dB, of which approximately 34 dB must be variable.

(2) To compensate for frequency spreads of approximately 4 Hz.

(3) Doppler shift correction of at least $\pm$16.96 Hz.

In the following two Chapters, hardware and software algorithms used to satisfy these requirements are discussed.

CHAPTER II

REFERENCES

II.A.1 Quazi Azizul H., and William L. Konrad", Underwater Acoustic Communications", IEEE Communications Magazine, Vol. 20, No. 2, March 1982.

II.A.2 Morgera, S.D., "A Conceptual Design of an Underwater Acoustic Telemetry System, Phase II Study", prepared for Canadian Department of Environment, Oceans and Fisheries, Contract 07SC.KF806-8-E330, 20th February 1980.

II.A.3 Morgera, S.D., "Optimum Underwater Acoustical Telemetry Techniques", prepared for Canadian Department of Environment, Oceans and Fisheries, Contract 07SC.KF806-8-E330, 28th February 1979.

II.D.1 Urick, R.J., Principles of Underwater Sound, McGraw-Hill, New York, 1967.

II.E.1 Morgera, S.D., "Ocean Bottom Unit Transmitter Power Requirements", prepared for Canadian Department of Environment, Oceans and Fisheries, 20th November 1980.

II.E.2 Dinn, D.F., "Deck Unit Signal Processing", unpublished Memorandum, Bedford Institute of Oceanography, Dartmouth, Nova Scotia, April 1981.

CHAPTER III
HARDWARE DESIGN AND IMPLEMENTATION

III.A SYSTEM OVERVIEW

This chapter describes in detail the hardware used in the Deck unit. As shown in Figure III.A.1, the Deck unit consists of six functional blocks. The hardware description is separated into six sections, each covering one of the functional blocks. Central to the Deck unit, because it controls all aspects of the processing, is the CPU module described in Section III.B. The 16-bit 8086 CPU performs all the signal processing, except the FFT algorithm. The microcode used to support all the software routines described in Chapter IV is all stored on the CPU module. The CPU module memory consists of 6 K of ram memory for storage of data and constants, and 4 K of eprom with the machine code to support all the processing. Since the 8086 processor is interrupt driven from four sources, an interrupt controller is included to provide prioritized interrupt level control. A clock generator supplies the 4.9 mHz clock necessary for the CPU and a wait state generator synchronizes the CPU with slower peripherals. All decoding for memory and I/O is performed on the CPU module. Since the CPU communicates with all the modules, except the interrogation unit, the nature of the bus timing is covered in detail.

The remaining functional blocks under the control of the CPU are: (1) The time synchronizer, (2) The preprocessor, (3) The FFT processor, and (4) The RS 232 serial port. The timing synchronizer is covered in Section III.C and detects the four pilot tones transmitted

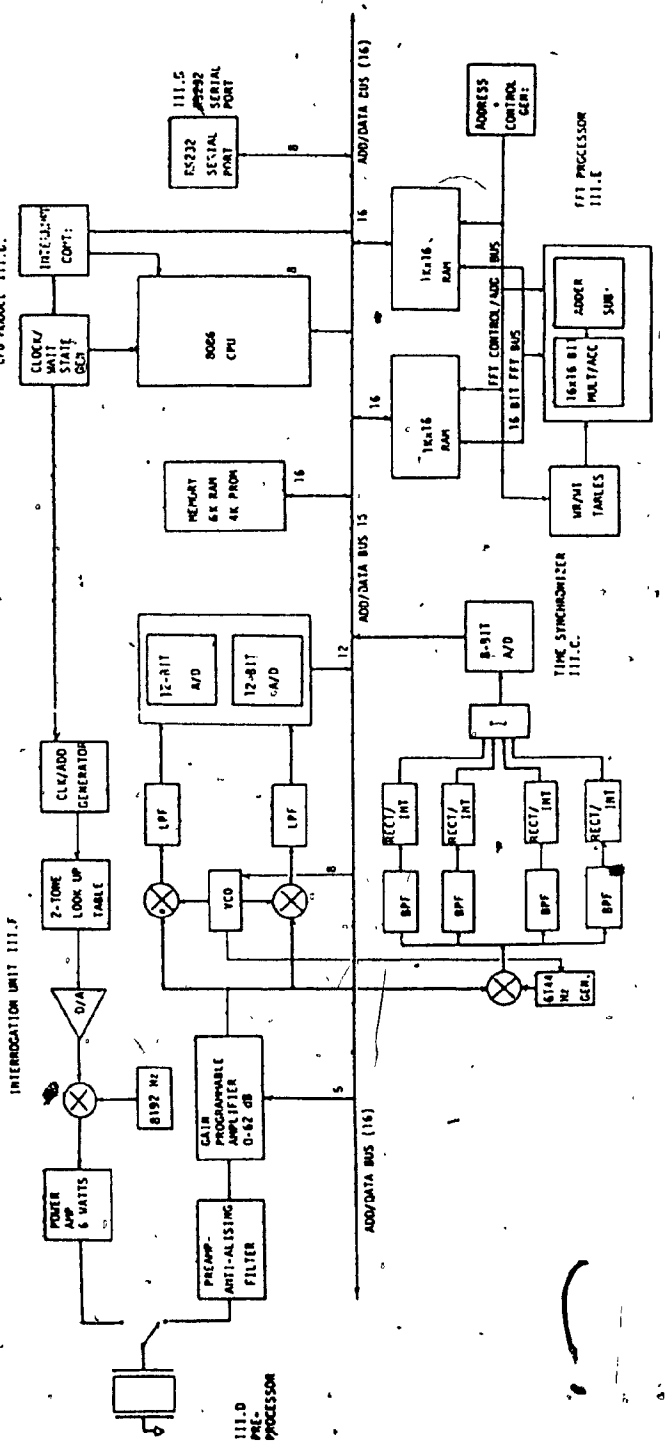


Fig. III.A.1 DECK UNIT HARDWARE

from the Bottom unit and supplies this information to the CPU. The pilot tones are used for initial time synchronization, as well as periodic time resynchronization of the system. First the pilot tones are translated down in frequency, before being passed through four sharply tuned bandpass filters. The output of each filter is rectified and integrated, and then the four detected outputs are summed to provide incoherent frequency diversity protection for the synchronizer. The combined output of the four integrators is then digitized at the rate of 256 Hz by the CPU. The resulting 8-bit samples are used as input to a 7-point Finite Impulse Response (FIR) filter for estimation of Bottom unit transmission time. The FIR filter coefficients are those of a relatively wideband differentiator.

The preprocessor consists of an anti-aliasing filter followed by a preamplifier with 16 dB gain. To prevent fading, a gain-programmable amplifier provides 78 dB of dynamic gain. A voltage controlled oscillator (VCO) with a range of 8192 Hz $\pm$ 18 Hz is included for doppler correction. Other devices include two mixers for shifting the signals down to baseband, followed by two filters and two 12-bit A/D convertors. The A/D convertors are sampled at a rate of 3072 Hz, with 512 complex samples stored for the FFT processor. Both the gain-programmable amplifier and VCO are controlled by the CPU. The preprocessor is covered in Section III.D.

For spectral analysis and subsequent MFSK demodulation, a fast Fourier transform (FFT) processor is employed. Section III.E. begins with a review of different FFT algorithms, followed by a description of the algorithm selected. The hardware consists primarily of a 2K x 16 ram

for input sample and temporary storage; coefficient storage for the implementation of the FFT butterfly; and a 16-bit adder/subtracter and a high-speed 16x16-bit multiplier/accumulator, used to implement the butterfly. A 32-step microprogram provides all the signals for the processor. Three different address schemes are required and are all generated in hardware. The time taken to process a 512-point complex FFT is 30 ms.

The RS 232 serial interface is covered in Section III.G. Storage of data to external peripherals is possible at baud rates of 110 to 9600.

The final module, the interrogation unit, produces five tones with a maximum power of 6 watts to drive a transducer. The five tones are produced by a rom look-up table and a frequency multiplier. A single chip commercial audio power amplifier with a step-up transformer provides the required drive for the transducer. The interrogation unit is controlled by the operator, and is covered in Section III.F.

Wherever possible, all the hardware design is detailed, however, due to limitation on space every gate and resistor cannot be covered, therefore this description of hardware deals with the most important devices. In cases where a device is used more than once, only one explanation is given. Multipliers are a good case in point, as frequency translation is often required. Since only one type of multiplier was used and since the applications, save for the input frequencies, were the same, one detailed description is presented. Another important piece of hardware are the filters used. The Burr-Brown universal active filter was used extensively; here again, one detailed explanation is presented.

The presentation of the filter designs gave rise to another problem for this thesis. The subject is covered in the Appendix where all

the design equations are shown. Three types of filter implementation were used; Butterworth, Chebyshev, and Elliptic. The Butterworth filters are used in the preprocessor, where a flat passband amplitude response is required. The Chebyshev filters are used in the time synchronizer for pilot tone detection, where phase is unimportant, and selectivity is a consideration. The front-end filter used is an elliptical type, as these filters have rapid transition band roll-off. [III.A.1.].

In the digital hardware, the 8086 CPU is dealt with in detail as its performance is central to the system. The 16x16-bit TRW multiplier also deserved attention for its importance in performing the FFT butterfly operations. Finally, circuit diagrams are shown with the text and whenever necessary, tables are included.

III.B. THE CPU BOARD

III.B.I INTRODUCTION

The CPU motherboard provides all the timing, control and storage requirements for the system. It consists of an 8086 16-bit CPU, with 6k of RAM and 4K of Program Prom. A wait state generator is utilised in order to facilitate communication with slower peripherals. A 4.9 mHz clock provides the basic timing for the system. Included on the board is an interrupt controller with 8 interrupt levels. All the buffering and demultiplexing of the bus is implemented on the board and distributed throughout the system via the back plane. Fig. III.B.1 is a block diagram of the CPU motherboard.

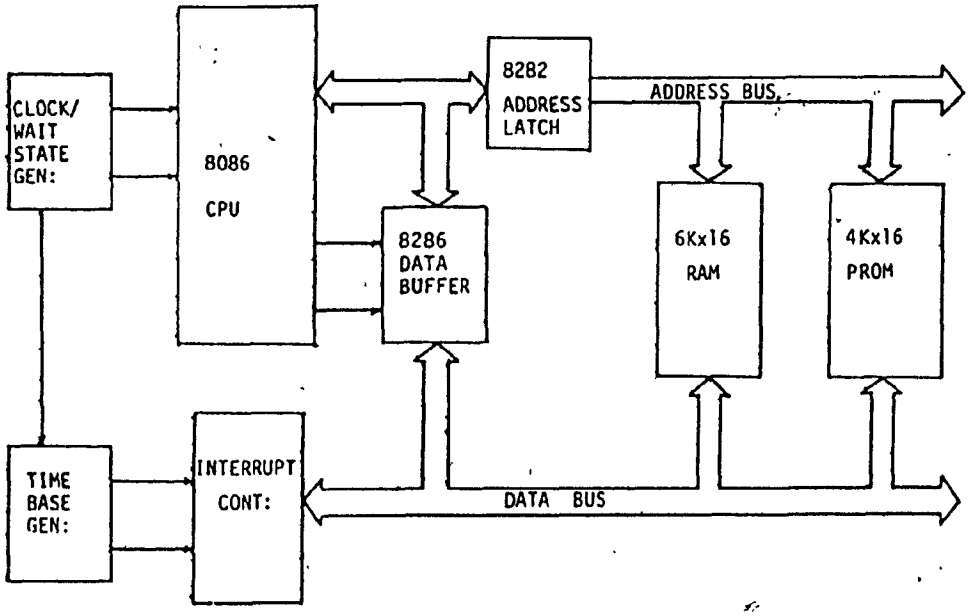


Fig. III.B.1 BLOCK DIAGRAM OF CPU MOTHERBOARD

III.B.2 ARCHITECTURE OF THE 8086 CENTRAL PROCESSING UNIT

The Intel 8086 Central Processing unit is a 16-bit microprocessor with 16-bit internal and external paths, one megabyte of memory address space, and a separate 64K-byte I/O address space. Performance of the 8086 is seven to ten times better than the 8080A. The improved performance is realized by combining a 16-bit internal data path with a pipeline architecture that allows instructions to be prefetched during space bus cycles. Also contributing to this performance is a compact instruction format that enables more instructions to be fetched in a given amount of time. Pipelining is made possible by having two separate processing units within the CPU. The execution unit (EU) executes the instructions; whereas, the bus interface unit (BIU) fetches the instructions, reads operands, and writes results. The two units can operate independently of one another and are able, under most circumstances, to extensively overlap instruction-fetch with execution. Refer to Figure III.B.2. [III.B.1.].

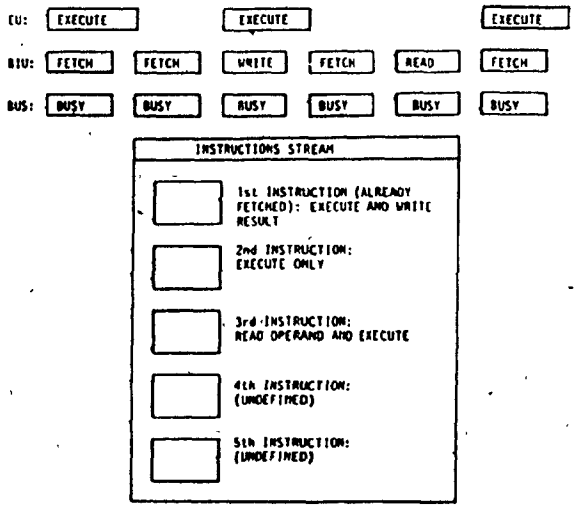


Fig. III.B.2 OVERLAPPED INSTRUCTION FETCH AND EXECUTION

III.B.3 HARDWARE DESIGN CONSIDERATIONS

In order to interface the 8086 CPU efficiently, an understanding of the 8086 bus timing is necessary. The CPU communicates with the external environment via a twenty-bit multiplexed address and data and command bus. To transfer data or fetch instructions, the CPU executes a bus cycle, as shown in Figure III.B.3. The minimum bus cycle consists of four clock cycles called 'T' states, (T1, T2, T3, T4). In 'T1' state, the CPU places an address on the 20-bit bus. In 'T2' state , the CPU performs a *READ*, *WRITE* or *INTERRUPT* acknowledge on the lower 16-bit bus, while on the upper 4 bits it provides status information which can be used for diagnostic monitoring. During the 'T3' state, the CPU continues to provide status information on the upper 4 lines of the bus, while on the lower 16 it places write data or samples read data. It is in this state that *WAIT* states can be inserted for slow peripheral devices. If no *WAIT* states are inserted, then the CPU will latch data onto the bus. The manner in which *WAIT* states are generated and inserted is described in Section III.B.9. The 'T4' state is the termination of the bus sycle. The bus cycle appears to devices as an asynchronous event consisting of an address to select a device followed by a *READ* or *WRITE* strobe. On termination of the command, the device latches write data or disables the bus drivers. The only control the device has on the bus cycle is to insert *WAIT* states. [III.B.1.].

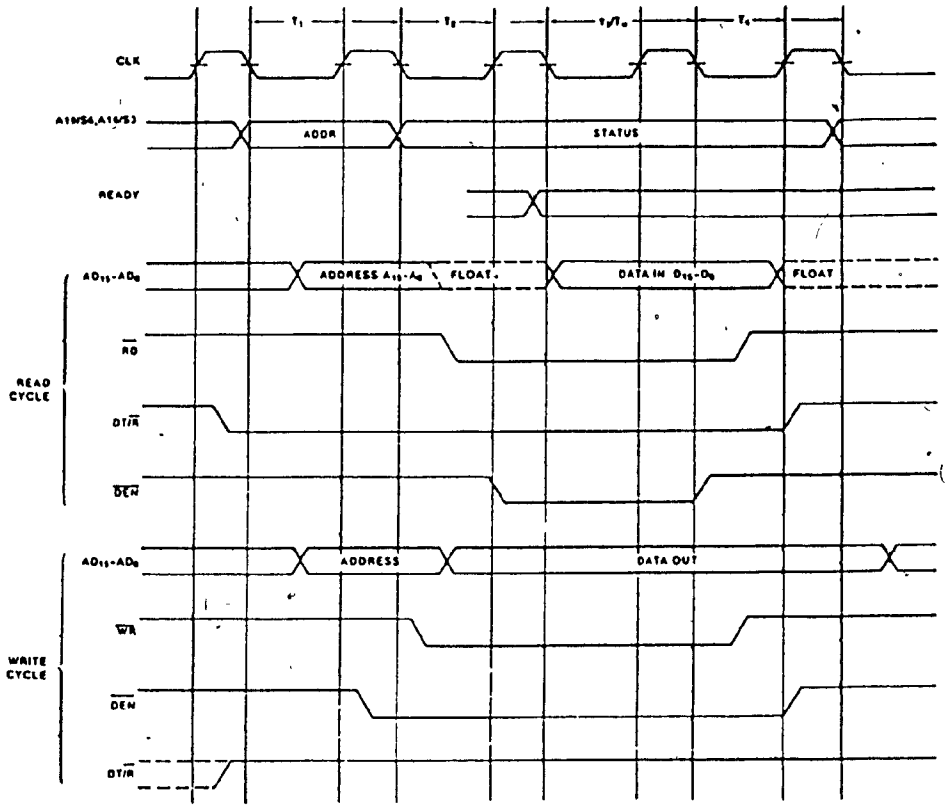


Fig. III.B.3 BASIC 8086 BUS CYCLE

III.B.4 ADDRESS AND DATA BUS

The multiplexed 8086 CPU bus has a drive capability of 2 mA, which is insufficient for this application. Furthermore, some form of bus de-multiplexing is necessary. The address and data information is time-multiplexed on to the CPU bus, with the address appearing during the 'T1' cycle. To latch the address, the 8086 provides an *ADDRESS LATCH ENABLE (ALE)* signal to capture the address as shown in Figure III.B.4. The 8282 8-bit bi-stable latches are used for this purpose. The latches have outputs driven by tri-state buffers that supply 32 mA drive capability and can switch a 300 pf capacitive load in 30 ns. The latches are

transparent when *ALE* is high and latch the address onto the falling edge of *ALE*. Figure III.B.4 shows the configuration of the multiplexed data bus. [III.B.1.].

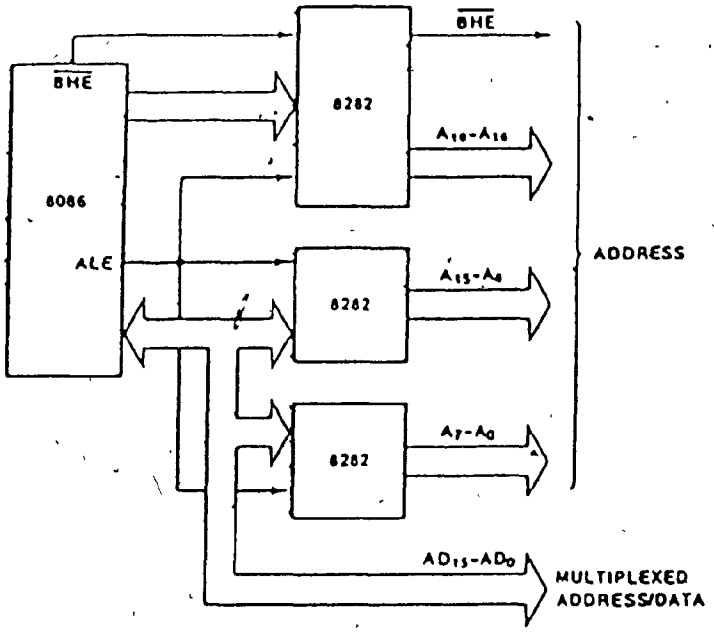


Fig. III.B.4 MULTIPLEXED DATA BUS

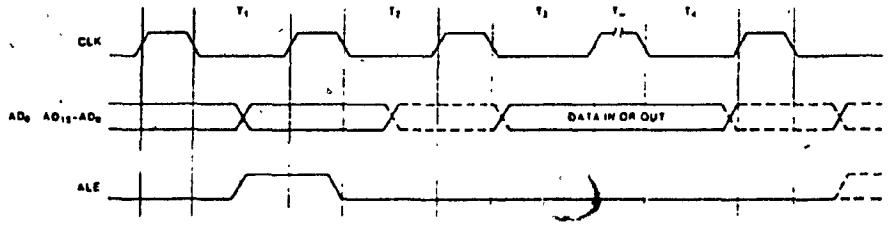


Fig. III.B.5 DIAGRAM ALE TIMING

To satisfy the capacitive and drive requirements of the system, the

data bus has to be buffered. Buffering is provided by two 8086 octal transceivers. These transceivers have tri-state outputs that can drive loads of 32 mA on the bus interface and 10 mA on the CPU interface, and can switch capacitive loads of 300 pf on the bus side and 100 pf on the CPU side. To control the transceivers, the CPU provides two control lines; $\overline{DEN}$ to enable the drivers, and $DT/\overline{R}$ to control the direction of the data, as shown in Figure III.B.6. [III.B.2.].

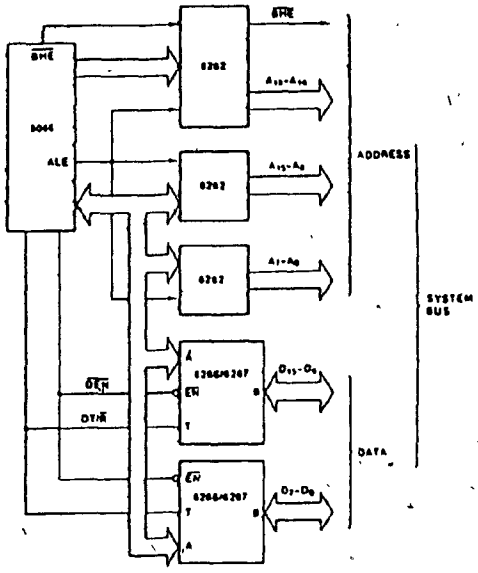


Fig. III.B.6 BUFFERED DATA BUS

III.B.5 MEMORY ORGANISATION

The CPU motherboard contains 6K of ram and 4K of prom memory. Of the 6K of ram, the lower 2K is reserved for scratch pad and interrupt vector storage. The upper 4K is used for tidal data storage. Above the ram memory is 4K of prom. Since program instruction can be on odd or even address boundaries, the prom address must be capable of selecting the upper or lower byte in the word. The 8086 CPU provides

an active low signal, $\overline{BHE}$ (byte high enable), to select the upper byte, and the A0 address line is used to select the lower byte. Both these signals are provided by the CPU and are latched in the same manner as the address lines.

The same method of byte selection is provided for the lower 2K of ram; whereas, the upper 4K of ram is only word selectable (two bytes) as tidal data is 16 bits wide ~~and is always~~ stored on even boundaries.

The selection of each 1Kx16 bank is accomplished by decoding bits *A11*, *A12*, *A13* of the address bus. An 8205 three-to-eight decoder is suitable for this purpose. Table III.B.1 describes the manner in which memory banks are selected. To protect against memory or I/O address conflicts, the memory-I/O (*M/IO*) line is also used to enable the decoder as shown in Figure III.B.7. Individual word and byte selection is provided by address lines *A1* thru to *A10*.

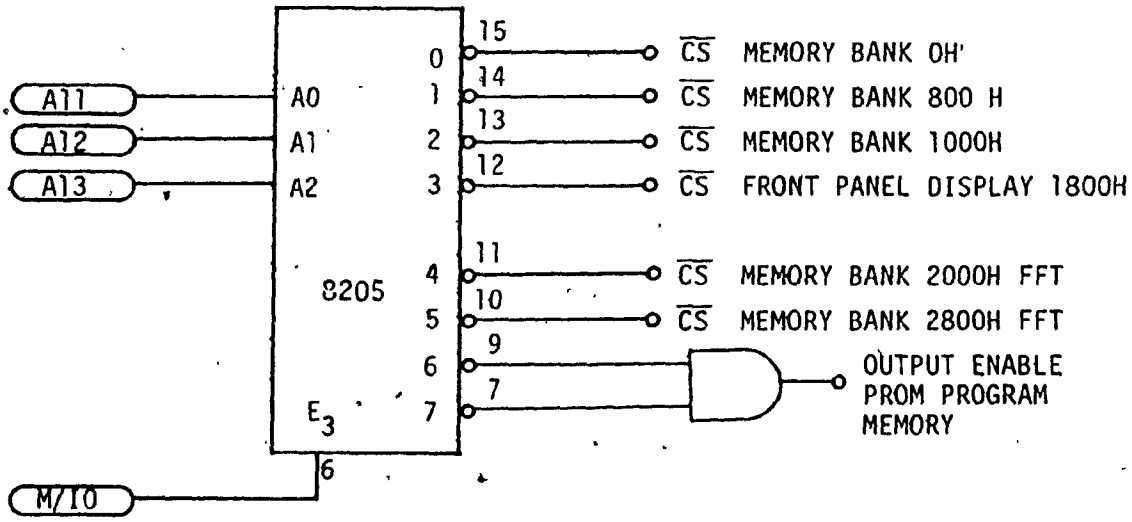


Fig. III.B.7 MEMORY BANK SELECTION

M/IO	A/3	A12	A11	OUTPUTS 0	1	2	3	4	5	6	7	MEMORY BANK ADDRESS
0	X	X	X	1	1	1	1	1	1	1	1	DISABLED
1	0	0	0	0	1	1	1	1	1	1	1	0H
1	0	0	1	1	0	1	1	1	1	1	1	800H
1	0	1	0	1	1	0	1	1	1	1	1	1000H
1	0	1	1	1	1	1	0	1	1	1	1	1800H
1	1	0	0	1	1	1	1	0	1	1	1	2000H
1	1	0	1	1	1	1	1	1	0	1	1	2800H
1	1	1	0	1	1	1	1	1	1	0	1	F000H
1	1	1	1	1	1	1	1	1	1	1	0	F800H

E1=GND, E2=$\overline{DEN}$, E3=M/IO

Table III.B.1 TRUTH TABLE MEMORY BANK SELECTION

III.B.6 TIMING FOR MEMORY READ, WRITE, AND SELECT

MEMORY READ

The read timing consists of conditioning the bus, activating the read command, and establishing the data transceivers enable and direction control. Data transmit-receive ($DT/\overline{R}$) is established early in the bus cycle T1 and stays active until T4. The $\overline{DEN}$ signal (data enable) must allow the transceivers to propagate data to the CPU with the appropriate data set-up time and continue to do so until the required data hold time. The $\overline{DEN}$ turn-on delay allows 127 ns transceiver enable time prior to valid data required by the CPU. Since the CPU data hold time and $\overline{DEN}$ turn off delay are both 10 ns minimum relative to the same

clock edge, the hold time is guaranteed. Furthermore, $\overline{DEN}$ must disable the transceivers before the CPU redrives the bus with the next address; however, the transceivers are disabled at least 105 ns before the CPU drives the address onto the multiplexed bus. [III.B.2.].

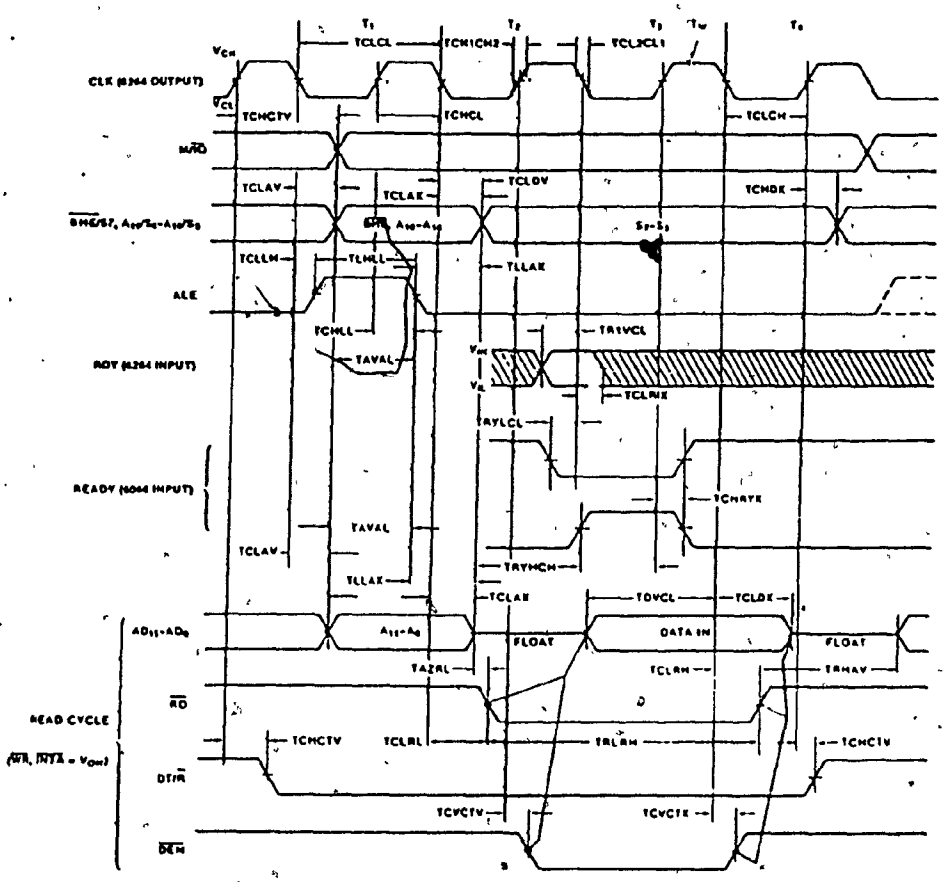


Fig. III.B.8 8086 BUS TIMING - MINIMUM MODE SYSTEM

The memory chips used in this system are 2142-3, 1kx4 static rams, with a maximum access time of 300 ns. Since the minimum delay from read active to valid data at the CPU is 205 ns, it is necessary to slow down

or introduce wait states during the T3 cycle. One wait state $1/f_{CLK}$ (f_{CLK} = 5 mHz) would increase this time to 205 ns + 200 ns = 405 ns, which is sufficient for the 2142-3 ram and its maximum access time of 300 ns. See Figure III.B.9 for the RAM timing requirements. [III.B.2.].

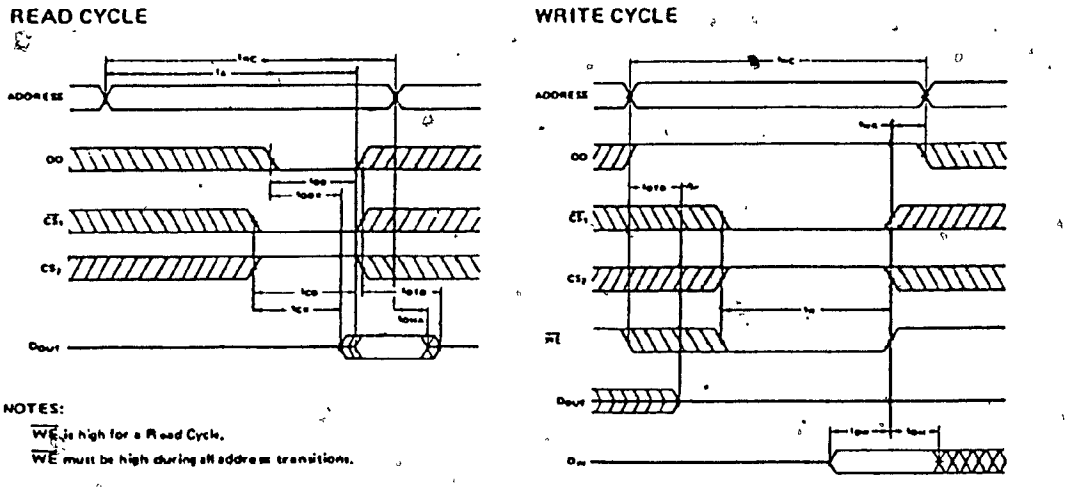
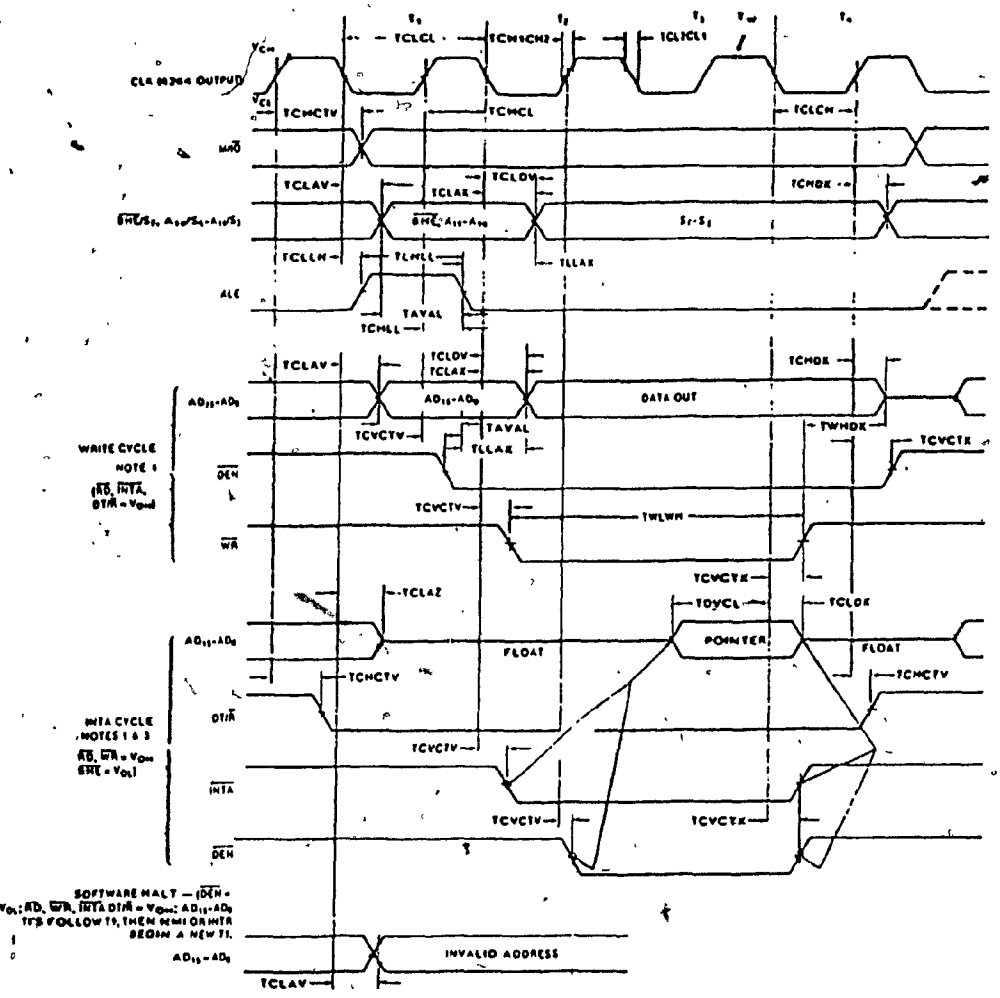


Fig. III.B.9 2142-3 RAM TIMING REQUIREMENTS

MEMORY WRITE CYCLE

The write cycle involves providing write data to the RAM, generating the write command, and controlling the data bus transceivers. $DT/\overline{R}$, the transceiver direction control is conditioned by the CPU to transmit at the end of each read cycle and does not change during the write cycle. Therefore, $\overline{DEN}$ can be active early while the addresses are valid since the transceivers are already driving the memory bus. The write command and the write data are both enabled at the trailing



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. BOTH INTA CYCLES RUN BACK-TO-BACK. THE 8086 LOCAL ADDR/DATA BUS IS FLOATING DURING THE SECOND INTA CYCLE. CONTROL SIGNALS SHOWN FOR SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

Fig. III.B.10 8086 MEMORY WRITE CYCLE [III.B.1].

edge of T2. Write data becomes valid 100 ns after write is active, therefore, the 2142-3 ram should be able to capture data on the trailing edge of the write command. The data from the 8086 is valid a minimum of 300 ns before the trailing edge of the write command; this is seen to be more than sufficient, as the 2142-3 ram requires data to be valid 150 ns before the write rising edge strobe. The write pulse width required for the 2142-3 is 300 ns, which is well within the range of the write command of the CPU at 340 ns. $\overline{DEN}$ is disabled 18 ns after the write command, but this is of no consequence as the 2142-3 ram requires 0 ns for data hold time after the write command. Therefore, no wait states are required as in the read cycle. [III.B.2.].

Individual memory bank selection is implemented by decoding address lines *A11*, *A12*, *A13*, as previously mentioned; further conditioning of the address lines is provided by M/IO and $\overline{DEN}$. Refer to Table III.B.1 For the 2142-3 memory chips, chip select ($\overline{CS}$)-to-output valid time is 100 ns, and since $\overline{CS}$ is dependent on *M/IO*, address line settle time, and $\overline{DEN}$ which is active 127 ns prior to valid data, $\overline{CS}$-to-data valid times of the 2142-3 are met. During the write cycle $\overline{DEN}$ is enabled by *ALE*, as shown in Figure III.B.10 and therefore is not a factor.

III.B.7 INPUT-OUTPUT DEVICE SELECTION

I/O device selection is accomplished by decoding the A3, A4, and A5 address lines through an 8205 three-to-eight decoder. *M/IO* and $\overline{DEN}$ are used to enable the decoder, as shown in Figure III.B.11 and Table III.B.2.

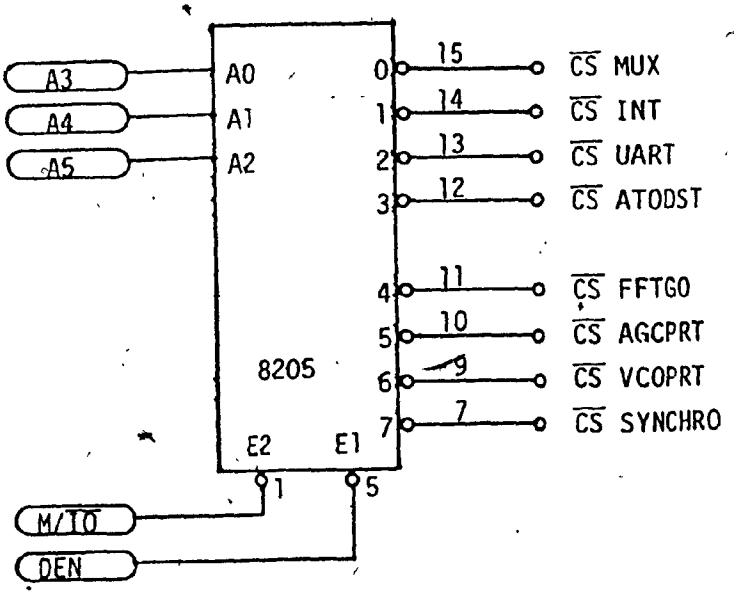


Fig. III.8.11 I/O PORT SELECTION

INPUT-OUTPUT PORT DESCRIPTION

MUX: An output port that controls the A/D convertors in the FFT channels.

INT: Interrupt controller.

UART: RS232 serial interface port using 8251 uart

ATODST: Status of A/D convertors in FFT channel and FFT data input port.

15	0
STATUS FLAG	15 BIT OF DATA (12 BIT SIGN EXTEND.)

FFTGO: Control port for FFT processor.

AGCPRT: Port to control gain of programmable amplifiers in

preprocessor.

VCOPRT: Port to control voltage controlled oscillator in preprocessor.

SYNCHRO: Input data from time synchronizer A/D.

Table III.B.2 describes the manner in which I/O port selection is accomplished.

M/IO	DEN	A5	A4	A3	OUTPUTS 0	1	2	3	4	5	6	7	I/O PORT
1	1	X	X	X	1	1	1	1	1	1	1	1	DISABLE
1	0	X	X	X	1	1	1	1	1	1	1	1	DISABLE
0	1	X	X	X	1	1	1	1	1	1	1	1	DISABLE
0	0	0	0	0	0	1	1	1	1	1	1	1	MUX
0	0	0	0	1	1	0	1	1	1	1	1	1	INTR
0	0	0	1	0	1	1	0	1	1	1	1	1	UART
0	0	0	1	1	1	1	1	0	1	1	1	1	ATODST
0	0	1	0	0	1	1	1	1	0	1	1	1	FFTGO
0	0	1	0	1	1	1	1	1	1	0	1	1	AGC
0	0	1	1	0	1	1	1	1	1	1	0	1	VCO
0	0	1	1	1	1	1	1	1	1	1	1	0	SYNCHRO

E1=$\overline{DEN}$, E2=M/IO, E3=+5V

Table III.B.2 TRUTH TABLE I/O PORT SELECTION

III.B.8 THE CLOCK GENERATOR

The clock generator provides all the timing for the system. An Intel 8284 clock generator driver which accepts a crystal input was

used for this purpose. A crystal with a fundamental frequency of 14.7456 mHz was chosen as this frequency was a multiple of the baud rates and all the other frequencies required, such as the 256 Hz synchronization data sample; 3072 Hz data sample rate; and 4.9 mHz CPU clock. The clock generator itself divides the crystal frequency of 14.7456 mHz to produce a 4.9 mHz clock for the CPU. It provides two internally synchronised signals reset (RST) to initialise the system on power up or when reset manually and ready (RDY) which holds the CPU in order to insert wait states. Figure III.B.12 shows the clock and wait state generator. [III.B.1.].

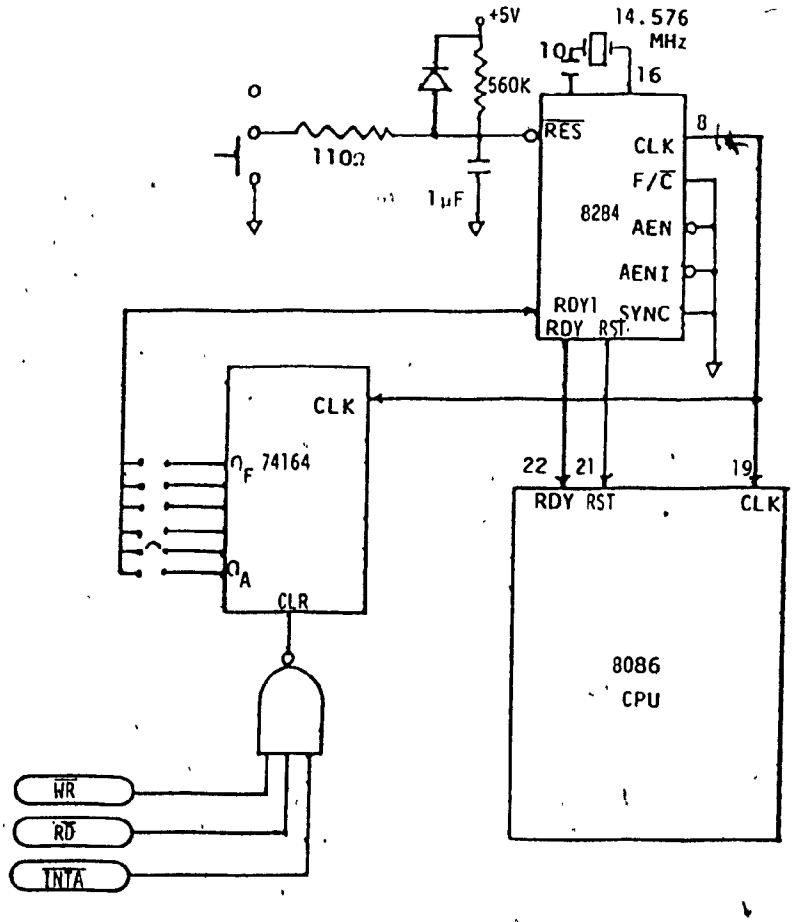


Fig. III.B.12 CLOCK AND WAIT STATE GENERATOR

The sample and time-based clocks are generated by dividing down the peripheral clock (PCLK) output of the clock generator. Referring to Figure III.B.13, the PCLK output which is half the rate of the system clock is divided by 2,100 and then by 8 and 12 to produce the required rates of 3072 and 256 Hz.

III.B.9 THE WAIT STATE GENERATOR

The wait state generator allows 'wait states' to be inserted into the CPU bus cycle to compensate for slow peripherals, I/O or memory. Referring to Figure III.B.12, the wait state generator is cleared following every read, write or interrupt cycle and subsequently is enabled at the beginning of the next read, write or interrupt cycle when the clear (CLR) input to the wait state generator goes inactive. When enabled, the wait state generator, a 74L164 shift register, begins to shift a 'one' through the register. When the selected number of shifts, two in this system, have occurred pin 6 goes active high, which causes the RDY1 input of the clock generator to go active, thereby causing the RDY output to the CPU to go high. [III.B.1.].

III.B.10 THE INTERRUPT CONTROLLER

Four functions of the system are interrupt driven; they are, in order of priority:

(1) Sample interrupt - this interrupt is activated for 160 ms to collect data for the FFT processor. A total of 512 complex (in-phase and quadrature) samples are collected

at a 3072 Hz rate.

(2) Time-base interrupt - this interrupt serves as the main time-base for the system. It determines time frames of 250 ms during which data is collected and processed. It occurs every 4 ms (256 Hz).

(3) Begin interrupt - this is a manual interrupt which informs the CPU to begin processing.

(4) Dump interrupt - this interrupt allows the operator to abort the current task and dump all data and system parameters to a printer or terminal.

Any one of the above can cause an interrupt by pulling one of the 8259A's interrupt request pins (pin 18, 19, 20, 21) high. Referring to Figure III.B.13, if the 8259A honors the request, pin 17 (INT) will go high, driving pin 18, the interrupt request pin (*INTR*), on the CPU, high. Since this pin is asynchronous, the 8086 will accept it provided it has been prepared to do so via the software. The CPU responds by sending a sequence of two *INTA* interrupt acknowledge pulses to the 8259A (Pin 26). The first *INTA* only signals the interrupt controller that the request has been honored, the second *INTA* pulse causes the 8259A to place a single interrupt vector byte onto the lower half of the data bus. The CPU reads the bus and multiplies the value by four to obtain the address of the particular interrupt type. Figure III.B.10 shows the hardware timing of the events described above. The CPU read/write lines are used to program (in the write case) or read the status of the 8259A interrupt controller. [III.B.2.].

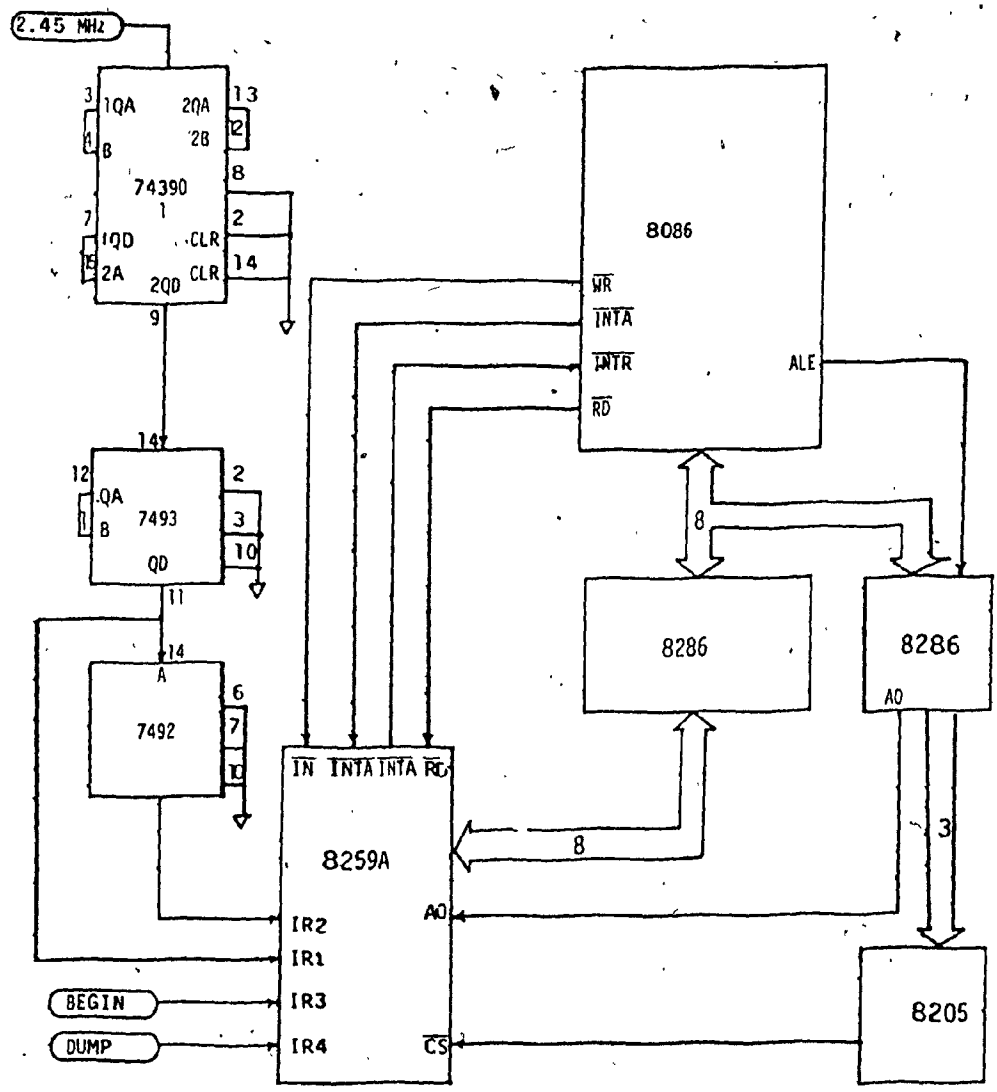


Fig. III.B.13 THE INTERRUPT CONTROLLER

III.C. THE TIME SYNCHRONIZER

III.C.1 OVERVIEW

In order to properly demodulate the transmitted tones, some form of synchronization is required between the Bottom and Deck unit. The Bottom unit observes a period of silence (no transmission) between successive data words. Therefore, each 16-bit word is transmitted for 125 milliseconds followed by 125 ms of dead time as shown in Figure III.C.1.

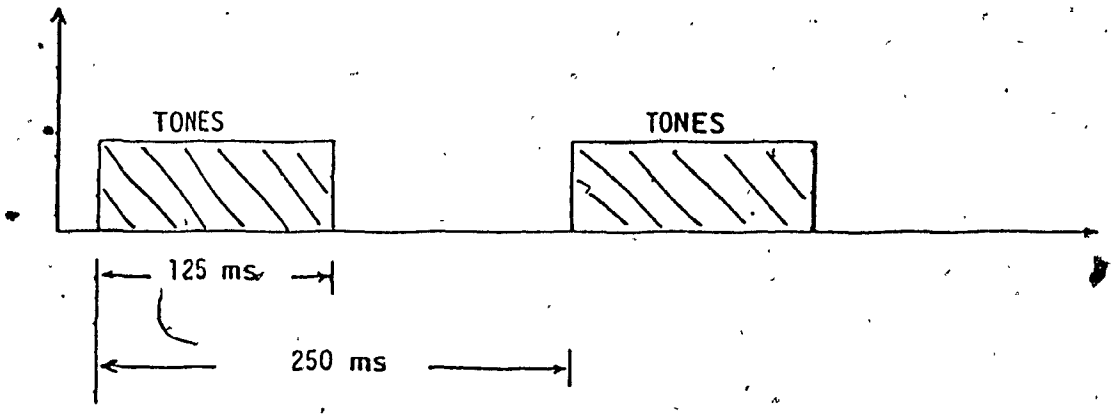


Fig. III.C.1 TRANSMISSION FORMAT

As described in Chapter 1, the Bottom unit encodes 16 bits of data words into 40 tones as shown in Figure III.C.2

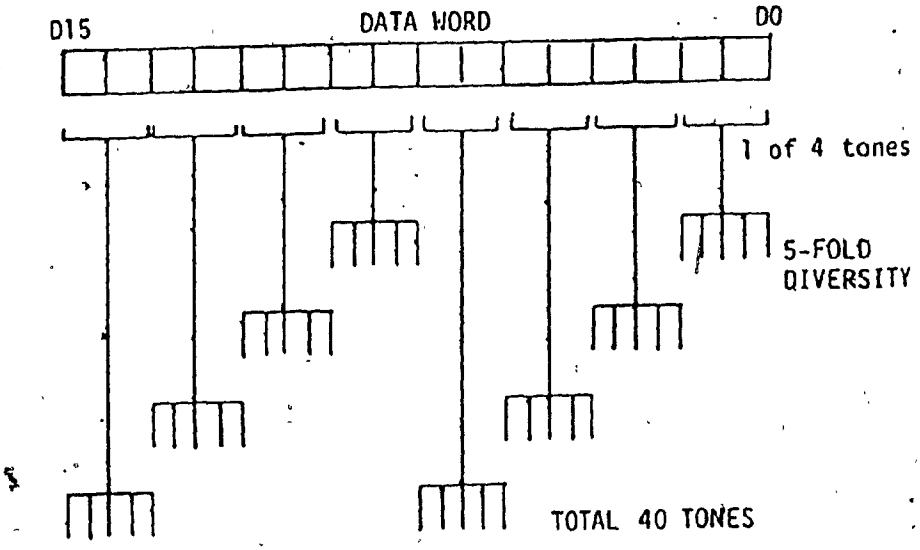


Fig. III.C.2 DATA-TO-TONE CONVERSION FORMAT

Interleaved between the five diversity bands are four pilot tones placed at ± 216 Hz and ± 1020 Hz. These pilot tones are transmitted regardless of the data pattern and are used to provide synchronization. Refer to Figure III.C.3.

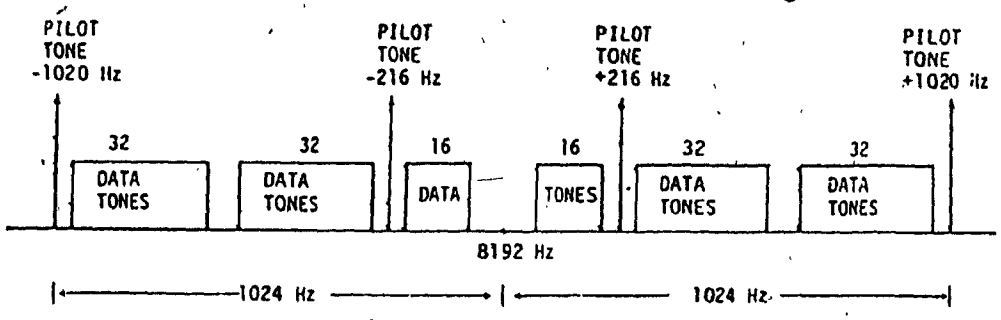


Fig. III.C.3 TONE SPECTRAL ALLOCATIONS

Upon receipt of the interrogation command from the Deck unit the Bottom unit transmits 16 preambles. Each preamble transmission consists of the preamble indentification label and the four pilot tones. The synchronization process consists of filtering of the four pilot tones, rectification and integration of each filter output; diversity combination of the four envelopes, and A/D conversion. Refer to Figure III.C.4. The 8-bit A/D convertor output is then used as input to a seven point finite impulse response (FIR) filter, timing markers are derived from the positive slope of the FIR filter output. The FIR algorithm and conversion process is controlled by the 8086 µp. See Chapter IV for details of the filter algorithm and threshold testing. The impulse response of which implements a bandlimited differentiator (high pass filter).

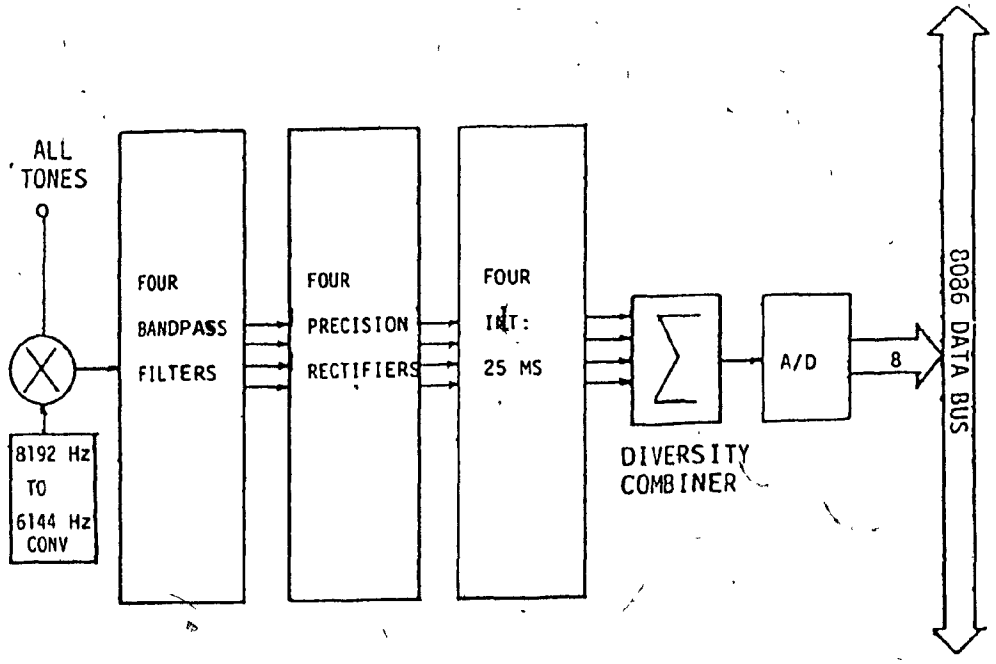


Fig. III.C.4 BLOCK DIAGRAM OF TIME SYNCHRONIZER

III.C.2 FREQUENCY TRANSLATION

Upon transmission from the Bottom unit, the pilot tones are located at 9212 Hz, 8408 Hz, 7976 Hz, and 7172 Hz in the frequency spectrum. In order to reduce the quality Q factor required for the bandpass filters, the tones are shifted down in the frequency by beating the incoming signal with a 6144 Hz carrier. The result of this multiplication moves the pilot tones down to 1028 Hz, 1832 Hz, 2264 Hz, and 3068 Hz, respectively. The balanced modulator MC 1496 is used to perform the frequency multiplication. It consists of an upper quad differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. This produces an output signal which is a constant times the product of the two input signals, plus other secondary components, as shown in Figure III.C.5. Mathematical analysis of linear AC signal multiplication indicates that the output frequency spectrum will consist of only the sum and difference of the input frequencies. [III.C.1].

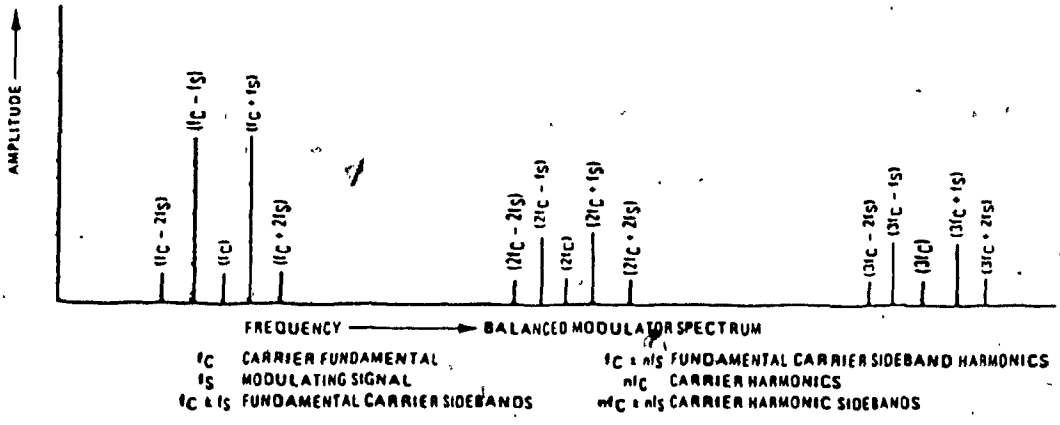


Fig. III.C.5 OUTPUT SPECTRUM OF BALANCED MODULATOR MC 1496

The complete multiplication circuit using the MC 1496 is shown in Figure III.C.6. The multiplier is operated in the linear region so as to produce only the sum and difference frequencies of the input signals with no other harmonics.

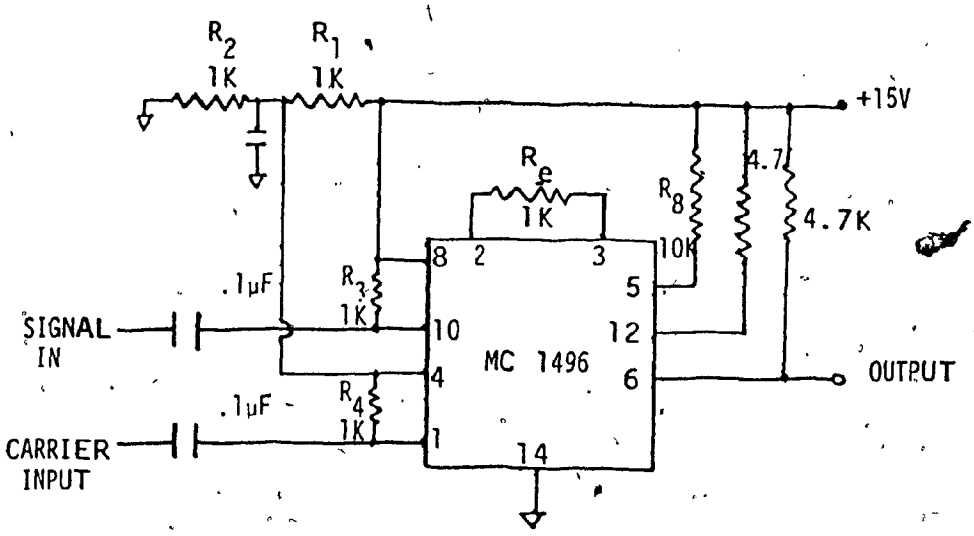


Fig. III.C.6 FREQUENCY DOWN TRANSLATION

To achieve this performance certain biasing conditions are suggested by the manufacturer. The signal gain is defined as,

$$A_{vs} = \frac{V_o}{V_s} = \frac{R_L}{R_e+2r_e} \qquad \text{where} \quad r_e = \frac{26\ mV}{I_5(me)} \qquad \text{(III.C.1)}$$

A constant DC potential is applied to the carrier input terminals to fully switch two of the upper transistors 'on' and two transistors 'off'. Linear operation requires that the signal input be below a critical value determined by R_e and the bias current I_5. The condition is,

$$V_s \leq I_5 R_e \quad \text{(Volts peak)} \qquad \text{(III.C.2)}$$

The carrier level suggested by the manufacturer is 60 mV (rms); this is the optimum value to prevent carrier feedthrough. With this input level, a carrier suppression of 44 dB was achieved in the prototype. Besides these requirements the MC1496 multiplier requires three dc bias voltages to be set externally. Equations (III.C.3, C.4, and C.5) define the relationship for these voltages [III.C.1].

$$30 \text{ Vdc} \geq [(V_6, V_{12}) - (V_{10}, V_8)] \geq 2 \text{ Vdc} \qquad \text{(III.C.3)}$$

$$30 \text{ Vdc} \geq [(V_{10}, V_8) - (V_1, V_4)] \geq 2.7 \text{ Vdc} \qquad \text{(III.C.4)}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc} \qquad \text{(III.C.5)}$$

III.C.3. 6144-Hz CARRIER GENERATION

In order to shift the pilot tones down in frequency, they are multiplied by a locally generated 6144 Hz carrier. To retain some control over doppler shift, the 8192 Hz sinusoid generated in the preprocessor by the VCO is used. First, the 8192 Hz sinusoid is squared, then divided by four, and, finally, the 6144 Hz harmonic is filtered. For the squaring of the signal, a LM 311 voltage comparator with a response time of 200 ns is used. [III.C.2]. Refer to Figure III.C.7. To provide some noise immunity, R_1 and R_2 provided a voltage threshold level of about 1.0 Volt. Two D-type flip-flops are used to divide the output by 4. These operations produce a 2048 Hz pulse.

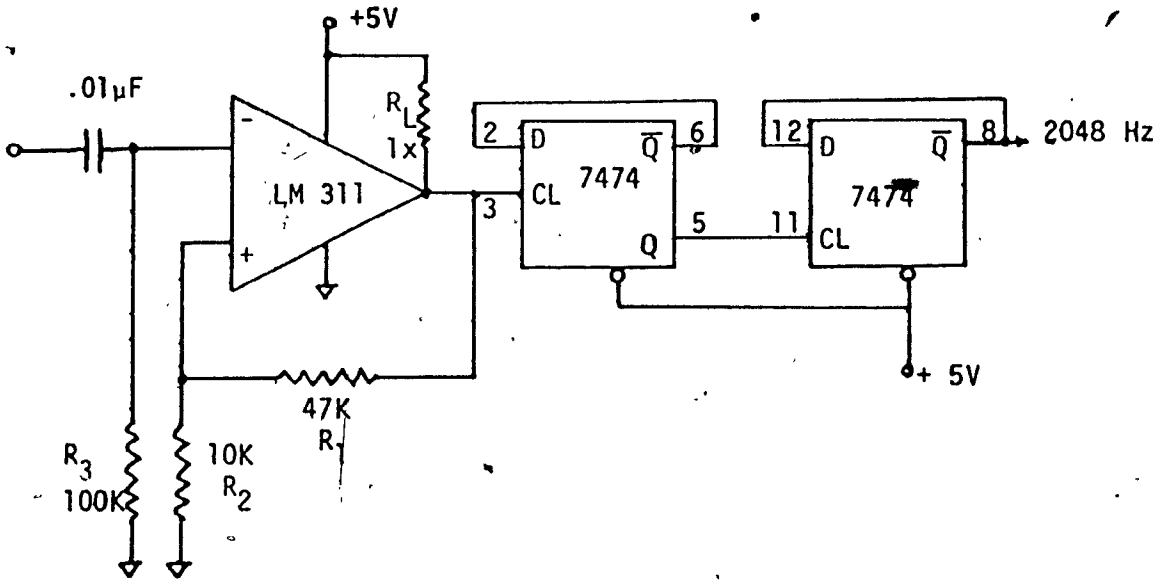
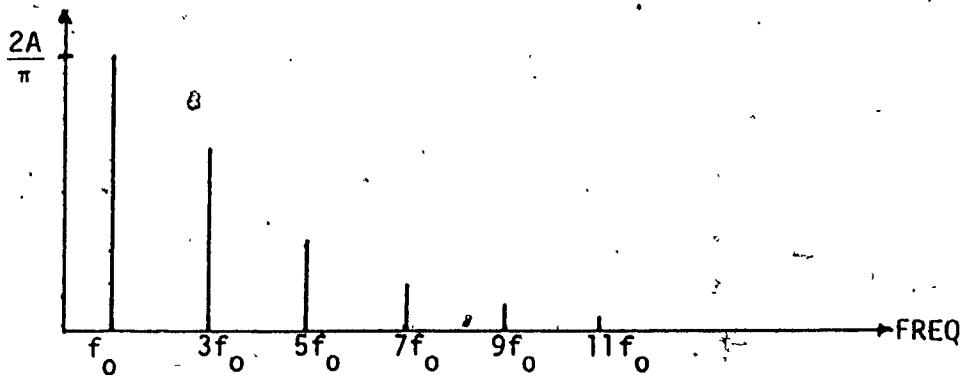


Fig. III.C.7 2048 Hz PULSE GENERATOR

The frequency spectrum of a 2048-Hz pulse is shown in Figure III.C.8. The Fourier series representation of the pulse is described in Eq. (III.C.6) [III.C.3]



f_o = 2048 Hz

Fig. III.C.8 FREQUENCY SPECTRUM OF A 2048 Hz PULSE

$$f(t) = A\left(\frac{1}{2} + \frac{2}{\pi}\cos\omega_o t - \frac{2}{3\pi}\cos 3\omega_o t \ldots\right) \qquad \text{(III.C.6)}$$

From Equation (III.C.6) and Figure III.C.8, it can be seen that the pulse of 2048 Hz contains a spectral component at 6144 Hz. A fourth order VCVS Bandpass active filter was designed with a center frequency of 6144 Hz and a Q of 12 as shown in Figure III.C.9. The response of the filter is shown in Figure III.C.10.

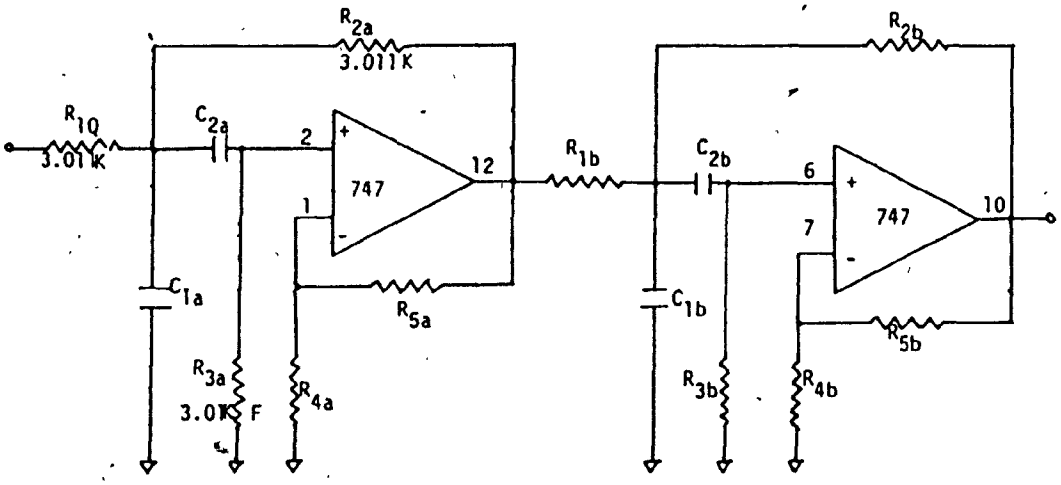


Fig. III.C.9 4TH ORDER VCVS BANDPASS FILTER

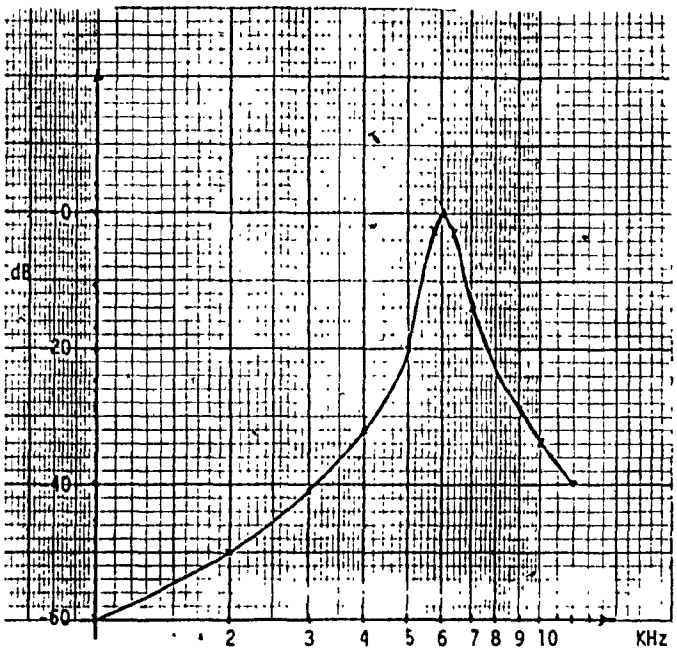


Fig. III.C.10 FREQUENCY RESPONSE OF THE 4TH ORDER BPF

III.C.4 PILOT TONE BANDPASS FILTER

Once the incoming signal has been shifted down in frequency, the tones have to be passed through four bandpass filters. To achieve some immunity from doppler shift and adjacent tone interference, the filters were designed with a bandwidth of 36 Hz, since the maximum doppler shift envisaged was ± 18 Hz and the nearest tone was located 24 Hz away. This requirement imposed very stringent requirements on the filters. Six-pole Chebyschev filters with a ripple of 1.5 dB were chosen as these type of filters. These filters provide a high roll-off at the cost of increased ripple.

The UAF 41, a universal active filter, was ideal for this purpose due to its simplicity in design and the high Q's obtainable. It is a

versatile 2-pole active filter using the state variable technique to produce a basic second order transfer function given by Equation (III.C.7) [III.C.4.].

$$T_{BP} = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)s + \omega_o^2} \qquad \text{(III.C.7)}$$

The state variable approach uses two op-amp integrators, A2 and A3, and a summing amplifier A1 to provide simultaneous lowpass, bandpass and highpass responses as shown in Figure III.C.11. One UAF41 is required for each pole pair of a bandpass filter section. [III.C.4]. Design equations supplied by the manufacturer, Burr Brown, were used to calculate the values of R_{F1}, R_{F2}, R_G, and R_Q. A Fortran program also supplied was used to make the lowpass to bandpass transformation. The final design configured three UAF41 active filters, one tuned to the tone frequency, and the other two to ± 1.5 Hz of the tone frequency. Each filter was designed with very high Q's. The response curve of one of the filters is shown in Figure III.C.12. Figure III.C.12b denotes the different specifications of all the filters.

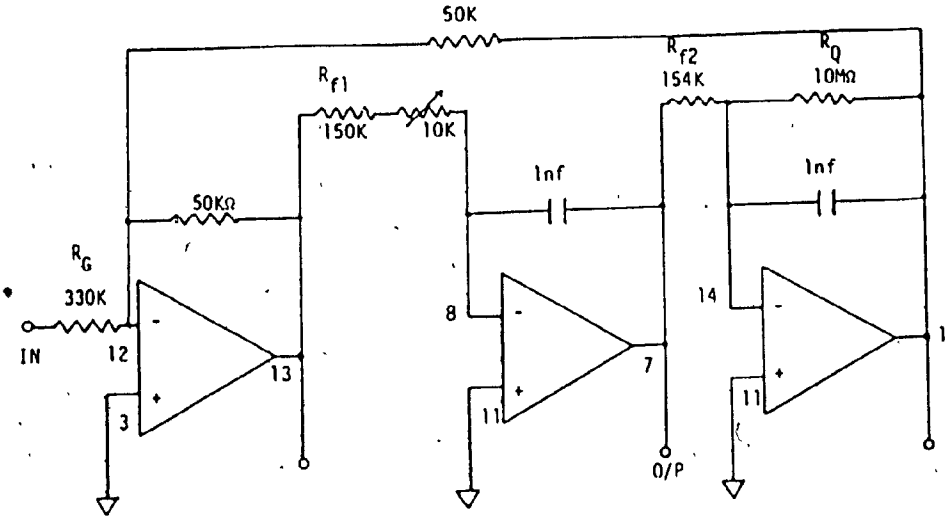


Fig. III.C.11 TWO POLE CHEBYSCHEV BANDPASS FILTER

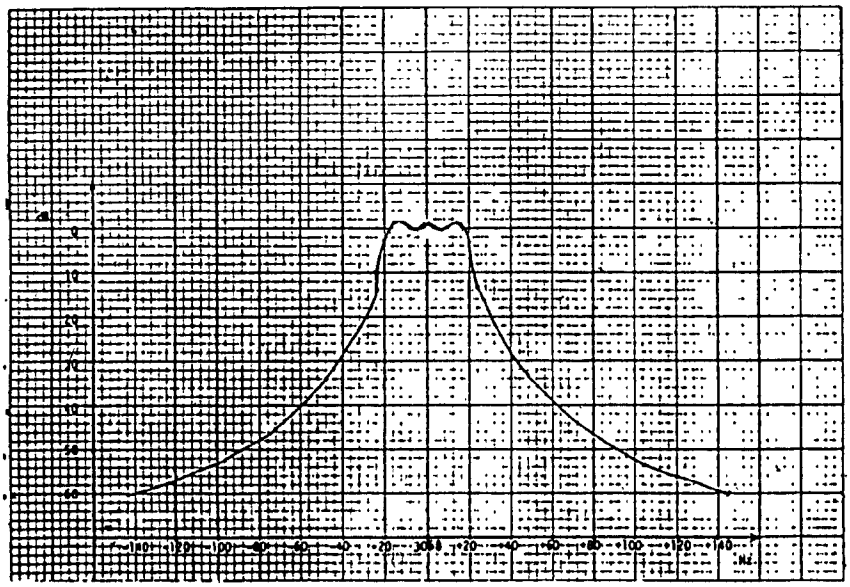


Fig. III.C.12a 6-POLE CHEBYSHEV RESPONSE CURVE

	TONE #1	TONE #2	TONE #3	TONE #4
SEC:1	1028 Hz	1832 Hz	2264 Hz	3068 Hz
SEC:2	1043 Hz	1847 Hz	2279 Hz	3083 Hz
SEC:3	1013 Hz	1817 Hz	2249 Hz	3053 Hz
B.W.	40 Hz	40 Hz	40 Hz	40 Hz
RIPPLE	±1.5 dB	±1.5 dB	±1.5 dB	± 2 dB

Fig. III.C.12b PILOT TONE FILTER CHARACTERISTIC

III.C.5. PRECISION FULL-WAVE RECTIFIERS

The outputs of the four bandpass filters are converted to their equivalent RMS voltage by precision full-wave rectifiers, refer to Figure III.C.13. Two LM 308 precision operational amplifiers having offset voltages of 2 mV are employed for this purpose. A1 is used as a half-wave rectifier that produces an inverted halfwave of the input signal. A2 is used as the summer where the two inputs are added with the proper amplitude and phase to produce a full-wave rectifier output.

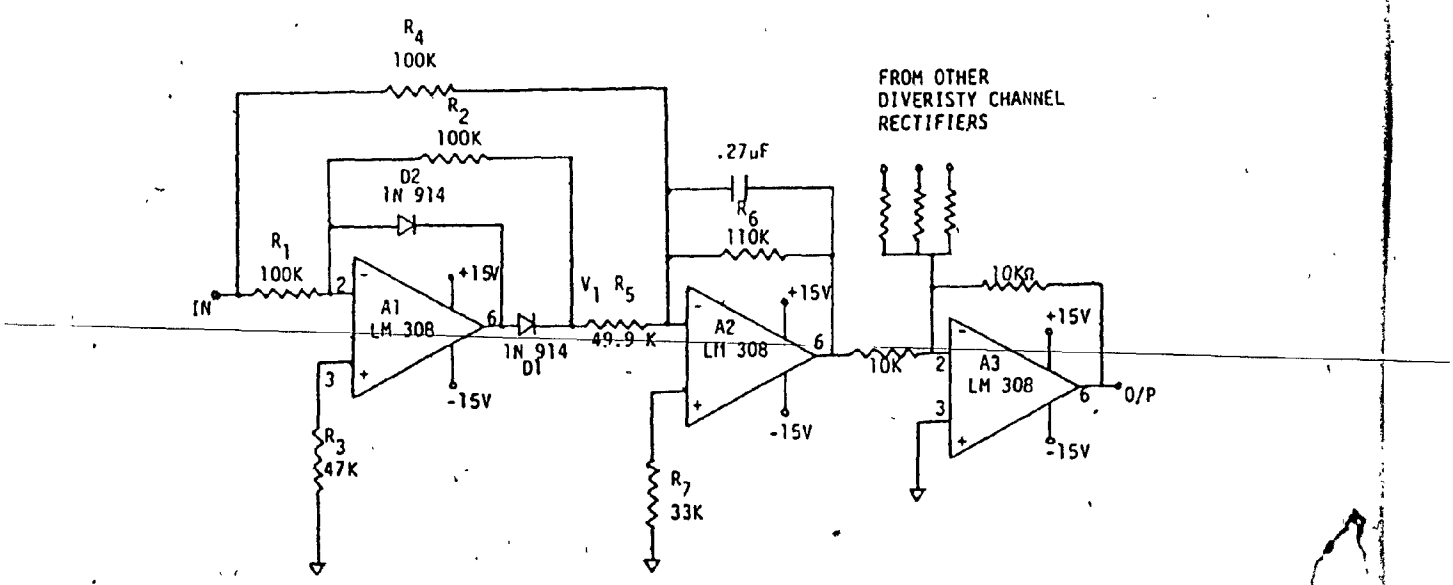


Fig. III.C.13 FULL-WAVE PRECISION RECTIFIER AND DIVERSITY COMBINER

For negative input signals at R_1, the output of A1 is positive, forward biasing D_1 and closing a negative feedback loop through R_2. This produces an inverted gain of almost exactly one, since R_1 and

R_2 are closely matched. For positive input signals, the amplifier output is negative and D_1 is off. D_2 is on in this case, applying negative feedback to the summing point and clamping the op-amp output to -0.6V. The output is added to the original input signal in A2. Positive signals at V_{1N} result in no output at V_1 due to rectification. V_{1N} feeds A2 through a 20 kΩ resistor and V_1 is fed through a 10 kΩ resistor. The net effect of this scaling is that, for equal amplitudes of V_{1N} and V_1, V_1 will produce twice as much current flow into the summing point. The positive cycle of V_1 produces twice the input current of that caused by V_{1N}. This causes a current of precisely half the amplitude which V_1 alone would generate due to the subtraction of V_{1N}. It is the equivalent of having V_1 feed through a 20 kΩ input resistor and having V_{1N} zero during this half cycle, and results in a negative-going output at A2. During the positive cycle of V_{1N}, V_1 is absent and V_{1N} produces the alternate output swing which, in summation, produces the desired full-wave rectified response. A2 served a double purpose as a summer and an integrator, with a time constant of 30 ms, to smooth the ripple of the full-wave rectifier.

III.C.6 DIVERSITY COMBINATION

The rectified outputs of the four pilot tones are summed in order to protect against fading which may affect the amplitude of one or more tones. The diversity combiner is simply a summing amplifier, with a gain of -1. An LM308 operational amplifier sums the outputs of the rectifiers which are negative, to produce a positive output as shown in Figure III.C.13.

III.C.7 ANALOG TO DIGITAL CONVERSION

The diversity combined output in Figure III.C.14a is sampled at a rate of 256 Hz by the CPU. The data obtined is used as inputs to the 7-point FIR filter. The AD 7574, an 8-bit convertor with a conversion speed of 25 μsec, is well-suited for this application. [III.C.5.].

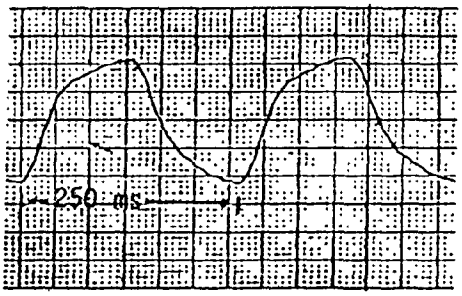


Fig. III.C.14a DIVERSITY COMBINER OUTPUT

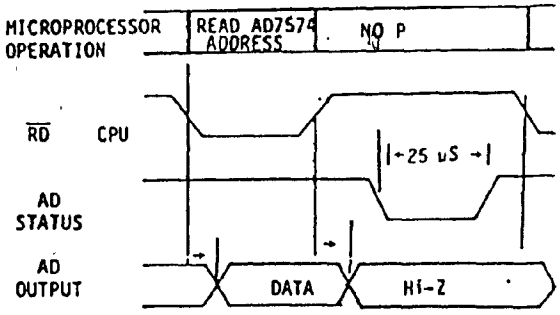


Fig. III.C.14b TIMING DIAGRAM

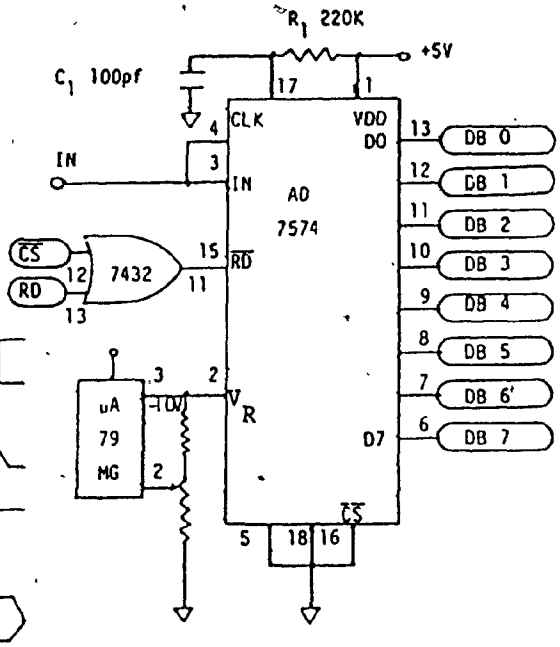


Fig. III.C.14c 8-BIT ADC

The convertor is designed to be operated as a memory-mapped input device. $\overline{CS}$ is held low and the convertor operation is controlled by the $\overline{RD}$ signal gated with the decoded device address, $\overline{CS}$. Gating was required due to the timing differences between the convertor and the CPU generated signals. The timing diagram for the acquisition of data is

shown in Figure III.C.14b. Resistor R_1 and capacitor C_1 determine the conversion time of 25 μs. A constant reference voltage of -10V is assured by using a 79MG voltage regulator. The 8-bit output is therefore a straight binary code. [III.C.5.]. Refer to Figure III.C.14c. All control operators are under command of the 8086 μp.

III.D. PREPROCESSOR

III.D.1 INTRODUCTION

The preprocessor conditions the incoming signal for eventual A/D conversion. It consists of a front-end filter, a gain programmable amplifier, multipliers for demodulation, a voltage controlled oscillator for doppler shift correction, sample and hold circuits, and two 12-bit A/D convertors, as shown in Figure III.D.1. The signal received through the transducer is first passed through a bandpass filter to limit the out-of-band noise. Since the tones at baseband occupy the frequency spectrum $\pm$ 1024 Hz, a sampling rate of 3072 Hz was deemed adequate. The Sampling Theorem states that "a band-limited signal having no spectral components above a frequency BHz is determined uniquely by its values at uniform intervals spaced no greater than 1/2B seconds apart". [III.D.1.]. Obviously any noise components above 1536 Hz would cause aliasing due to under-sampling. Refer to Figure III.D.2. [III.D.2].

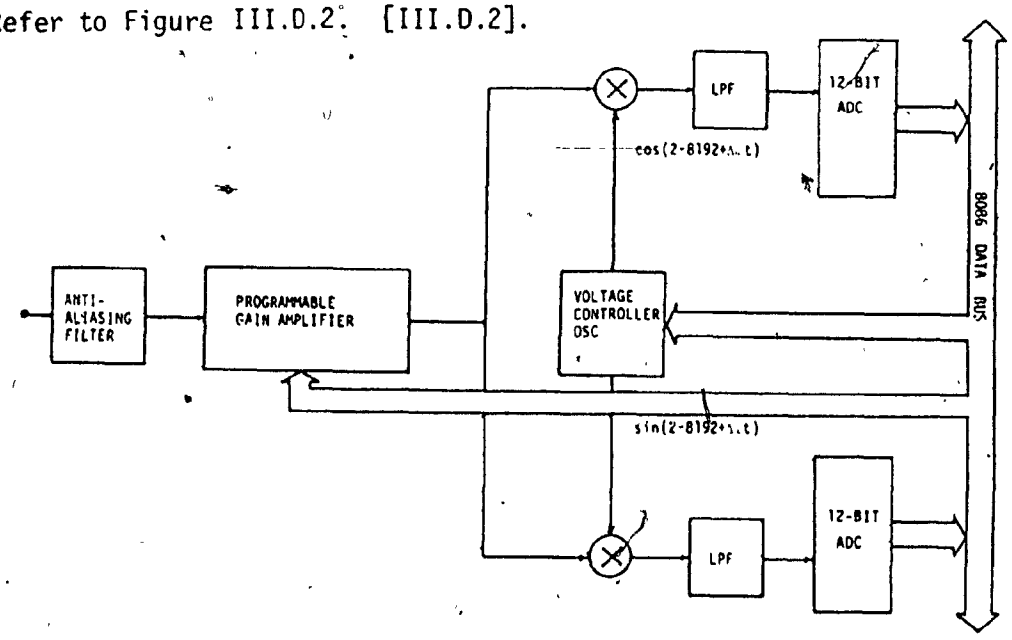
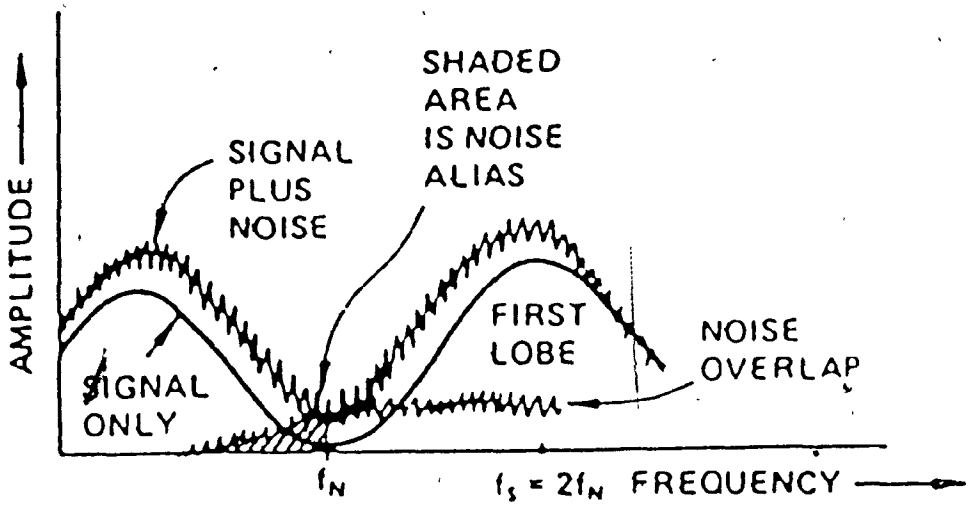


Fig. III.D.1 BLOCK DIAGRAM OF PREPROCESSOR
NOTE: $\Delta\omega$ IS CPU-CONTROLLED DOPPLER SHIFT CORRECTION

A preamplifier with a gain of 16 dB amplifies the signal before band limiting occurs. Following the anti-aliasing filter, a gain programmable amplifier controls the signal. The amplifier consists of four separate amplifiers with gains of 2 dB, 4 dB, 8 dB, 16 dB, and 32 dB. All four amplifiers are under software control of the 8086 CPU.



f_n FREQUENCY OF HIGHEST COMPONENT

f_s SAMPLING FREQUENCY

Fig. III.D.2 NOISE COMPONENTS CREATE ALIASING DUE TO UNDER SAMPLING

Every 250 ms the CPU reads the time synchronizer port to determine signal strength and adjusts the gain of the amplifiers accordingly. The amplifiers have a total gain of 62 dB which can be changed in 2 dB steps. The gain-adjusted signal is then multiplied by $\cos(2\pi\ 8192t)$ and $\sin(2\pi\ 8192t)$ to produce the two quadrature channels for demodulation. The quadrature reference components at 8192 Hz are produced by a voltage controlled oscillator (VCO) which is under the control of the CPU. The VCO can make changes as small as $\pm$2Hz and has a total

range of ±18 Hz for doppler correction. The two quadrature channels are filtered using frequency f_c = 1200 Hz to reject the sum components produced by the multiplication process. Finally, the two channels are sampled again by the CPU at the rate of 3072 Hz and converted into 12-bit data words. The relative slowness of the A/D convertors (25 μs) necessitated the use of sample and hold amplifiers. [III.D.3.]. All the software algorithms used in the preprocessor are described in Chapter IV.

III.D.2 THE GAIN PROGRAMMABLE AMPLIFIER

Signal strength fluctuations due to fading are a common occurrence in underwater communications [III.A.3]. To compensate for these changes, the gain of the preprocessor is adjusted to optimize the signal level fed to the demodulator. A four stage amplifier is used in conjunction with analog switches to provide gain control. The MC 1458 internally compensated monolithic operational amplifiers (op-amp) are utilized with the analog switches controlling their gain control resistors. The basic method employed is shown in Figure III.D.3. The op-amps are configured in the non-inverting amplifier mode and their gain is calculated by Equation (III.D.1). [III.D.4].

$$\text{GAIN} = (R_f + R_{in})/R_{in} \qquad \text{(III.D.1)}$$

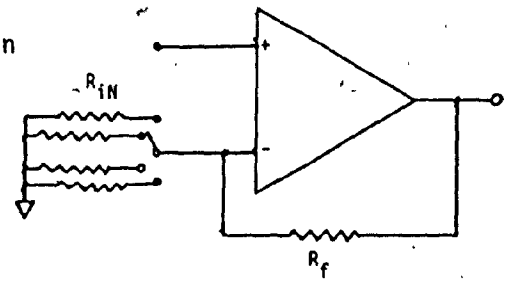


Fig. III.D.3 SELECTABLE GAIN AMPLIFIER

The op-amps have a gain-bandwidth product of 1 mHz which is adequate as the maximum frequency of the signals is 9216 Hz and the highest gain of the amplifier is 32 dB. The circuit for the preprocessor is shown in Figure III.D.4. Three of the op-amps are under control of the CPU, while A2 is under manual control. The amplifiers A1, A3 and A4 provide gains ranging from 0 dB to 62 dB in steps of 2 dB. Refer to Table III.D.1.

For switching the gain resistors, CMOS analog multiplexers/demultiplexers were used. The CD4052, produced by RCA, Inc., is a differential 4-channel multiplexer having two binary control inputs, A and B. The two binary input signals select 1 of 4 pairs of channels to be turned on. The maximum 'on' resistance of these switches is 125Ω, which is negligible whem compared to the resistors they are switching. [III.D.5.]. Table III.D.1 summarises the gains of each amplifier for all the switch settings.

BIT			GAIN (in dB)		
SW1	SW2	SW3	A_4	A_3	A_1
0	0 0	0 0	0	0	0
0	0 0	0 1	2	0	0
0	0 0	1 0	4	0	0
0	0 0	1 1	6	0	0
0	0 1	0 0	0	8	0
0	1 0	0 0	0	16	0
0	1 1	0 0	0	24	0
1	0 0	0 0	0	0	32

Table III.D.1 SWITCH SETTING-TO-GAIN ADJUSTMENT IN DB

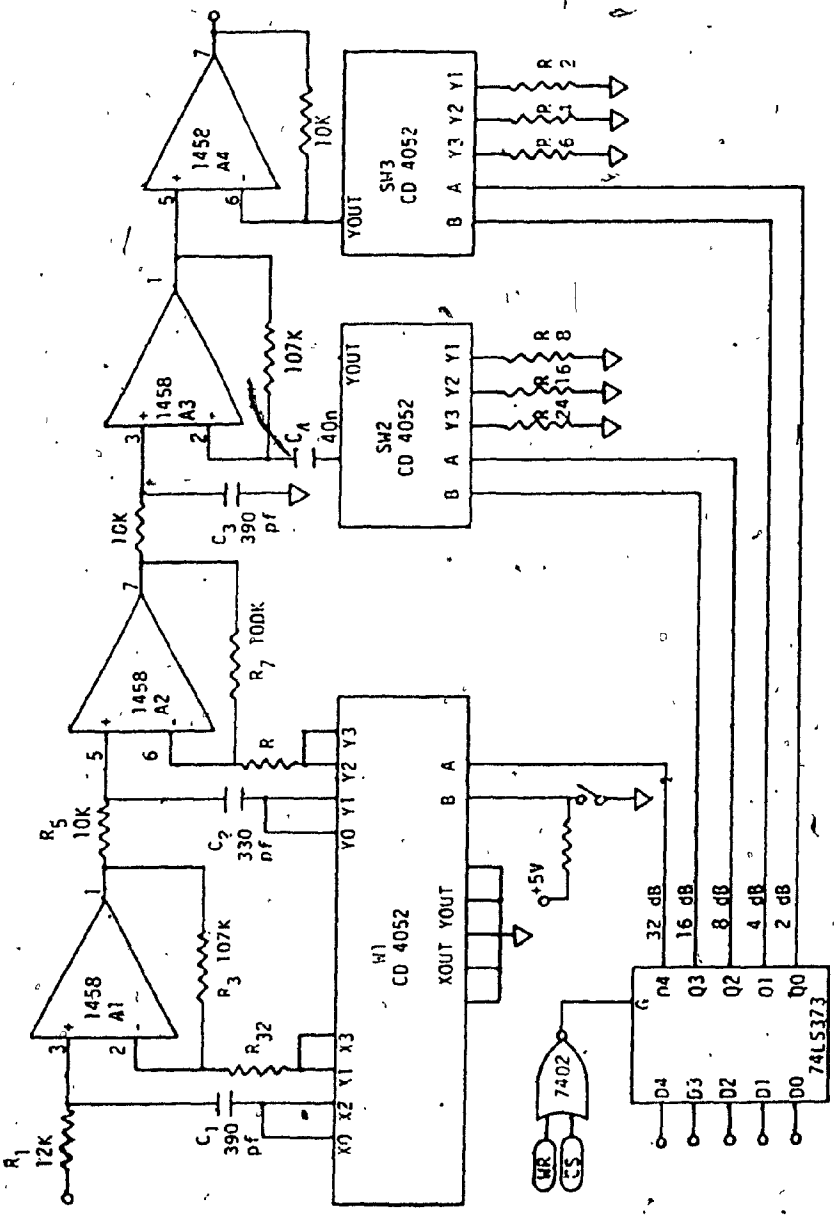


Fig. III.D.4 GAIN PROGRAMMABLE AMPLIFIER

Referring to Figure III.D.4, A1 provides 32 dB of gain when select line A of *SW1* is high and R32 is connected to ground. Resistor R32 is floating when select line A is low and A1 then acts as a unity gain amplifier. A2 is controlled by select line B which is activated by a switch on the front panel; A2 is designed for a gain of 16 dB, and is used in situations where the signal is known to be weak. A3 is designed for three levels of gain which are chosen by select line A and B of SW2; choosing R24, R16 and R8 programs A3 for gains of 24 dB, 16 dB, and 8 dB. Similarly A4 is controlled by SW3, which chooses the resistors to provide gains of 6 dB, 4 dB, and 2 dB. In all cases when the select lines are both low, the amplifiers have gains of 0 dB.

The five select lines are controlled by the CPU via the AGC port (AGC PRT). The AGC PRT is an 8-bit octal latch, 74LS373. Data present at the inputs is held when the enable line is pulled low. [III.D.6]. The enable line (G) is controlled by the memory write $\overline{WR}$ pulse of the CPU which is gated through a NOR gate with the address select line of the AGC port. I/O port selection is covered in Section III.B.

III.D.3 FREQUENCY CONVERSION

The incoming signals are down-converted to baseband. In this method the signal is multiplied by quadrature references, $\sin(2\pi\ 8192t)$ and $\cos(2\pi\ 8192t)$. The multipliers used in this application are the MC 1496 dual balanced modulators. They are operated in the linear mode, and as a result produce sum and difference frequency components. Therefore, after multiplication there are two bands of frequencies: one centered around DC (0Hz) and the other around 16384 Hz, as shown in

Figure III.D.5. The design of the multipliers is the same as that described in Section III.C.2 on the time synchronizer. Matched components are used for both multipliers to keep any amplitude or phase distortions to a minimum.

In order to keep the sample rate low, the high frequency components located at 16384 Hz are filtered out. A fourth order lowpass filter with corner frequency f_c = 1200 Hz is used. The Butterworth configuration was selected because of its maximally flat passband response. Once again matched components are used in the design. The circuit diagram and the response curve for these filters is shown in Figure III.D.6. The transfer function of the filter is given by Equ. (III.D.2) A study of the response curve shows that the sum components are attenuated by more than 40 dB. This met design specifications. For design equations, see Appendix [III.A.1.].

$$H(s) = \left(\frac{K_a b_1}{s^2+a_1 s+b_1}\right)\left(\frac{K_b b_2}{s^2+a_2 s+b_2}\right) \qquad \text{(III.D.2)}$$

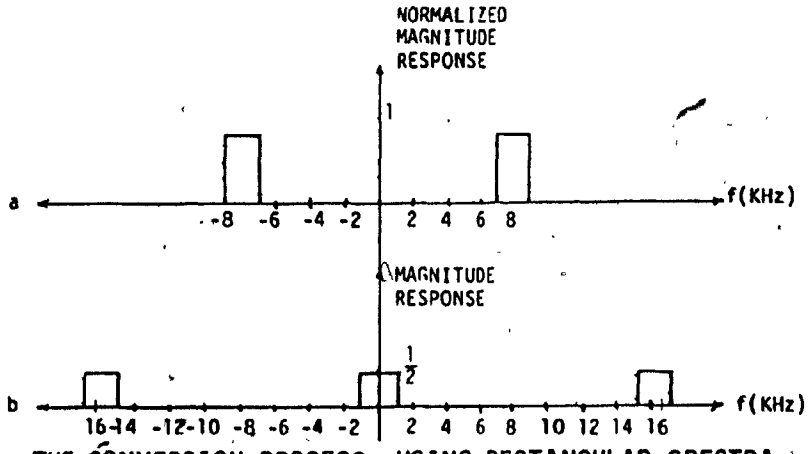


Fig. III.D.5 THE CONVERSION PROCESS, USING RECTANGULAR SPECTRA EXAMPLE. (a) RECEIVED SIGNAL (b) AFTER CONVERSION

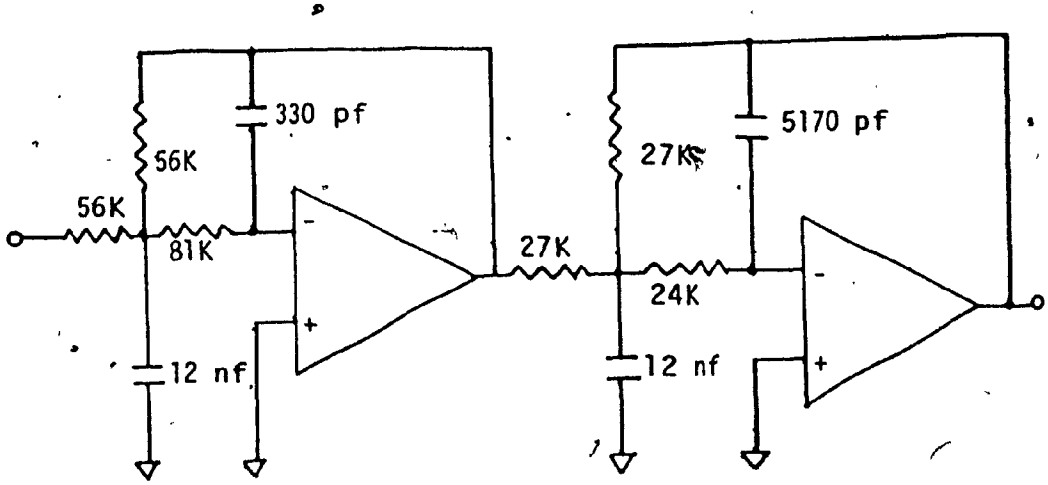


Fig. III.D.6a 4th ORDER LOWPASS FILTER

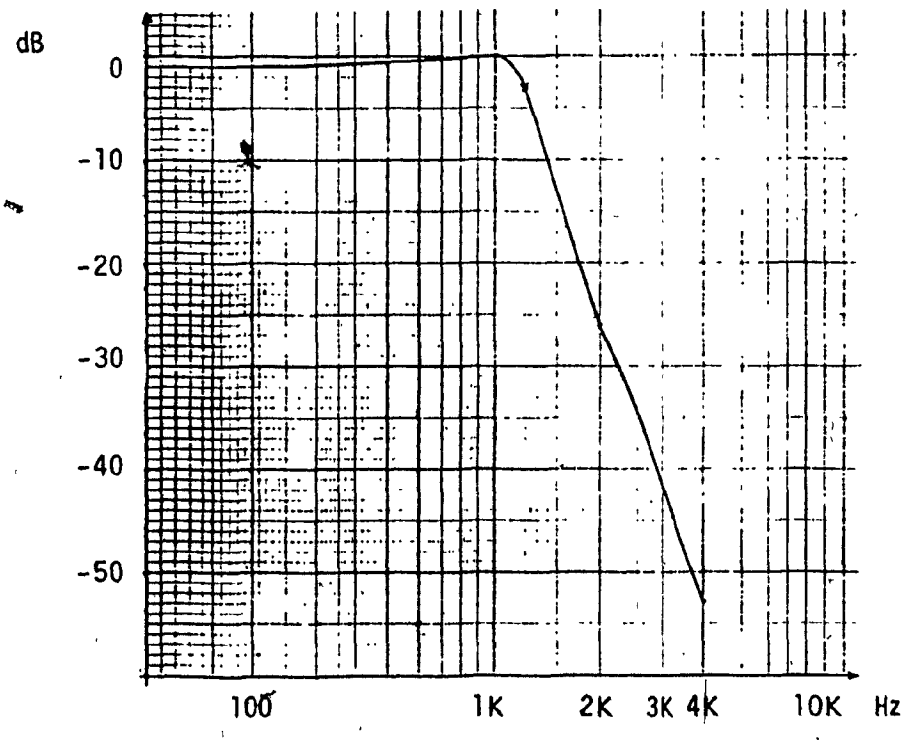


Fig. III.D.6b 4th ORDER LOWPASS FILTER RESPONSE

III.D.4 PROGRAMMABLE VOLTAGE CONTROLLED OSCILLATOR

The need for a voltage controlled oscillator (VCO) arises because of doppler shift. Doppler shift is present whenever there is a relative motion between transmitter and receiver. In this application, the Deck unit is located on a ship which is in motion. The transducer which is lowered from the ship is under the influence of the ship's motion and the current of the ocean. The effect of this is to make frequency tones, transmitted by the Bottom unit, appear to be of another frequency due to expansion or contraction of the time axis [II.D.1.]. As a first approximation to doppler correction, frequency is varied to compensate for this shift. In order to make the correction as accurate as possible, the doppler shift is estimated at several points within the system bandwidth. An average doppler correction is then applied. As was mentioned earlier, the Bottom unit transmits four pilot tones at 7172 Hz, 7976 Hz, 8408 Hz, and 9212 Hz. The Deck unit performs a spectral analysis on the received pilot tones and identifies the freqency change of each pilot tone. Once the frequency shifts have been calculated, they are averaged, and the CPU corrects the VCO. The software algorithm to identify and correct for doppler shift is presented in Chapter IV. In Chapter II, calculations of the maximum doppler shift for 6 knots was found to be $\pm$16.96 Hz. Therefore, a programmable VCO was designed with a range of $\pm$18 Hz. Because incoherent demodulation is used, the VCO has to produce quadrature components at the carrier frequency.

The VCO consists of three parts; a highly stable frequency generating oscillator, a control circuit to vary the frequency, and finally,

an interface between the CPU and the control circuit as shown in Figure III.D.7.

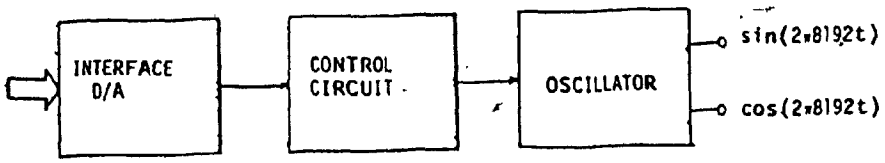


Fig. III.D.7 BLOCK DIAGRAM OF VCO

A highly stable oscillator was designed using the Burr-Brown UAF41 active filter. The filter was configured as a biquad filter and made to oscillate by designing for a very high Q and by providing some positive feedback to sustain the oscillation. The filter is already described in Section III.C.4. It uses two integrators and, therefore the quadrature components of the oscillating frequency are easily obtained. The chip has a frequency stability of ±0.002%/C°, with Q's ranging up to 500. [III.C.4.].

The biquad design has a transfer function as described in Eq. (III.D.3),

$$\frac{V_2}{V_1} = \frac{K\omega_0 s/Q}{s^2 + \frac{\omega_0}{Q} + \omega_0^2} \qquad \text{(III.D.3)}$$

The biquad filter has some unique features which enhance its use for this application. The centre frequency is easily tuned by adjusting one resistor R_f, as shown in Figure III.D.8. The absolute

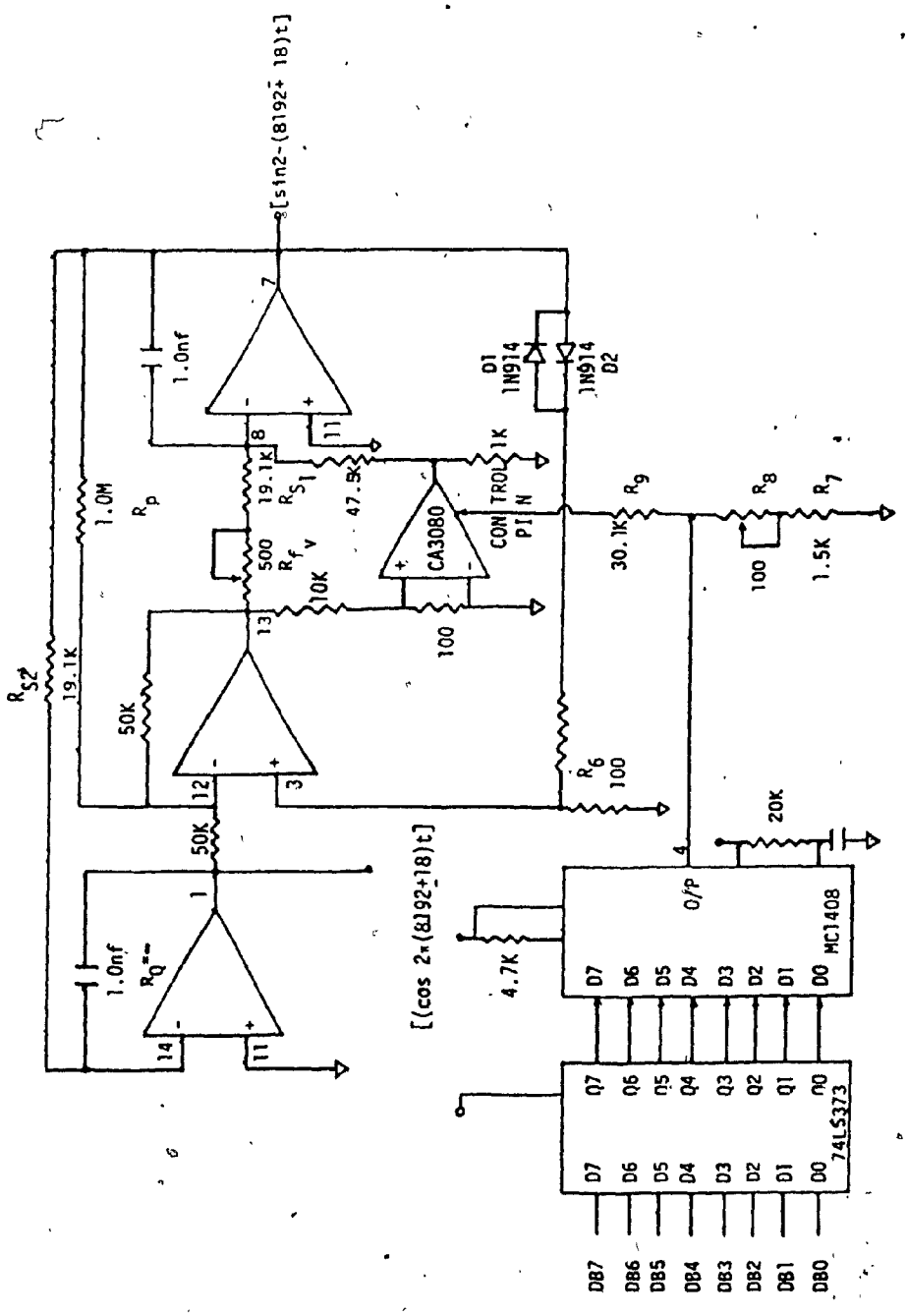


Fig. III.D.8 PROGRAMMABLE VOLTAGE CONTROLLED OSCILLATOR

bandwidth of this filter does not change with changes in center frequency. [III.D.7.].

The filter is tuned to 8192 Hz using the design equations described in Appendix VI.D.1 This results in a value of R_f, of 19.433 Kohms. A variable resistor is added in series with R_f, for fine tuning. The Quality (Q) factor determining resistor R_Q is not used, which gives the filter a very high Q. A 1.0MΩ resistor R_p is added to the regular biquad design between pin 12 and pin 7 of the filter, for some positive feedback. Finally in order to keep the output in the linear region (no clipping), two diodes in parallel and a voltage divider R5 and R6 provide negative feedback. The two diodes make the feedback non-linear, since their effective resistance decreases when the level increases.

An operational transconductance amplifier (OTA) is used in parallel with R_f, to change the frequency. The output resistance of an OTA is modeled as a current source in parallel with the output resistor. [III.D.8]. The CA3080 is a programmable OTA suitable for this purpose as its gain is made fully adjustable by controlling the current flowing through its control pin. Refer to Figure III.D.8. Changing the gain of the OTA which is in parallel with R_{f1} drives current into pin 8 of the filter, changing the effective resistance of R_f, and therefore, the frequency.

To drive the OTA control pin, a MC 1408 digital-to-analog (D/A) converter is used. The D/A convertor in turn is driven by the VCO port, consisting of a 74L373 octal latch. The writing of the VCO control word by the CPU into the latch is exactly the same as for the programmable amplifier described in Section III.D.2. The 8-bit byte

is then converted to a current which is used to drive the OTA. The MC 1408 is an 8-bit monolithic convertor whose output current is a linear product of an 8-bit digital word. [III.C.1]. Resistors R_7, R_8, and R_9 are used to scale the output current to provide ±20 Hz shift in frequency. Table III.D.2 shows the relationship between the control byte and output frequency.

CONTROL BYTE	D/A-OUT VOLTS	FREQ. (Hz)
0010 0000	-1.556	8212.1
0010 1000	-1.724	8210.4
0011 0000	-1.895	8208.7
0011 1000	-2.06	8207.0
0100 0000	-2.23	8205.3
0100 1000	-2.40	8203.7
0101 0000	-2.57	8202.0
0101 1000	-2.74	8200.5
0110 0000	-2.91	8198.6
0110 1000	-3.08	8196.9
0111 0000	-3.25	8195.2
0111 1000	-3.42	8193.6
1000 0000	-3.59	8191.9
1000 1000	-3.76	8190.2
1001 0000	-3.93	8188.5
1001 1000	-4.10	8186.8
1010 0000	-4.27	8185.3
1010 1000	-4.44	8183.4
1011 0000	-4.61	8181.8
1011 1000	-4.77	8180.0
1100 0000	-4.95	8178.3
1100 1000	-5.11	8176.6
1101 0000	-5.28	8174.8
1101 1000	-5.45	8173.1
1110 0000	-5.62	8171.4

Table III.D.2 RELATIONSHIP BETWEEN CONTROL BYTE AND VCO FREQUENCY

III.D.5 QUADRATURE CHANNEL ANALOG-TO-DIGITAL(A/D) CONVERSION

The two quadrature channels produced by the multiplication and filtering process are the input data stream for the FFT processor. These two analog channels have a bandwidth of ±1024 Hz and are sampled at a rate of 3072 Hz. It should be noted that the FFT input requires a time record of 512 complex data points. This means that in order

to fill this memory, data must be collected for 1/6th of a second. However, care must be taken so that the two channels retain the same phase relationship throughout the conversion. Any phase error would result in unwanted harmonics. [III.D.9]. One possible source of error is the amplitude changes of the input signal during A/D conversion. The 12-bit A/D convertors used were manufactured by Analog Devices Inc., and had a conversion speed of 25 μs. This implies that a 1 kHz signal would vary by as much as 9° (360x25/1000). A study of system performance with different phase error showed that the system would not tolerate more than +1° phase difference [III.D.9]. As a result, sample and hold (S/H) circuits were used to hold the signal steady during A/D conversion. Refer to Figure III.D.11.

The S/H circuits used for this purpose were the LF 398A, produced by National Semiconductor, Inc. The LF 398A are monolithic S/H circuits which utilize Bi-FET technology to obtain ultra-high dc accuracy, with fast acquisition of signal and low droop rate. Operating as a unity-gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 μs which is fast enough for this application, as the hold signal also serves as the sample interrupt to the CPU and the response time of the CPU to an interrupt is 12 μsec after the hold signal is given. A polystyrene capacitor was used for C_H, polystyrene capacitors have low leakage and very low hysteresis. Refer to Figure [III.D.11]. The output droop for a .01 μF capacitor is 8×10^{-2} V/sec. [III.C.2].

Due to the lack of time, two A/D convertors were employed. The AD 574A shown in Figure III.D.9a is a complete 12-bit successive

approximation type A/D convertor, with 3-state output buffer circuitry. The device consists of two chips, one containing a precision 12-bit DAC with voltage reference, the other containing the comparator, successive approximation register, clock, output buffers, and control circuitry [III.C.5]. It is used in a bipolar configuration and accepts analog inputs of ±10 V. Calibration is provided by the trim pot R. The stand-alone mode was selected for this application as it required the least amount of control lines. Figure III.D.9b shows the timing requirements for a single conversion.

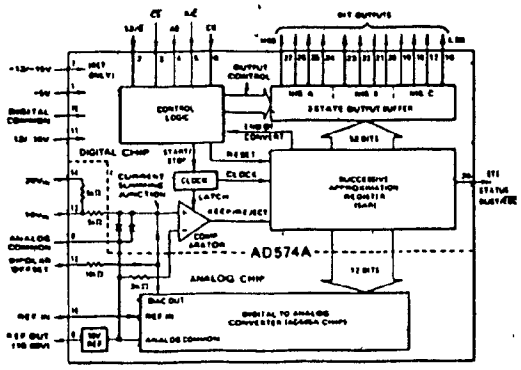


Fig. III.D.9a BLOCK DIAGRAM AD 574A

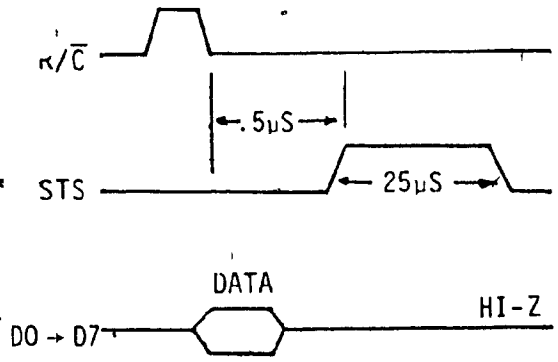


Fig. III.D.9b 12-BIT A/D TIMING

Two ports, one input and one output port, are assigned to the A/D convertors. The output port is used to store the read/convert ($R/\overline{C}$) commands to the convertors, while the input port provides buffering between the convertors and the CPU bus for the status line and output data. The 8086 μP writes out the command for the convertors to a CD4076 four-bit latch, which serves as the output port. The CD4076 is a 4-bit register consisting of four D-flip-flops [III.D.5]. The port is enabled by the address select line generated by the I/O address decoder circuitry,

and the write pulse is used to clock the command. Refer to Figure III.D.11.

The sequence of events for one complex sample conversion is as follows. The R/$\overline{C}$ lines for both convertors are set low by the CPU - this initiates a conversion. The status line goes high to indicate conversion progress. The two status lines are ORed and occupy bit 15 of the input port. The CPU reads the input port to test bit 15. When the input port is low, the CPU pulls the R/$\overline{C}$ line of *A1* high. Data from *A1*, according to Figure III.D.9(b), is available 25 ns later. The CPU reads the port and stores the data. It then pulls R/$\overline{C}$ of *A1* low and R/$\overline{C}$ of *A2* high. The data from *A2* is then read. The 12-bit data from the convertors is shifted left by 3 bits by tying them to bit 14 to bit 0 (zero), with the four LSBs of the port tied together as shown in Figure III.D.10. One further shift is performed in software, in effect multiplying 12-bit data upto 16-bit data.

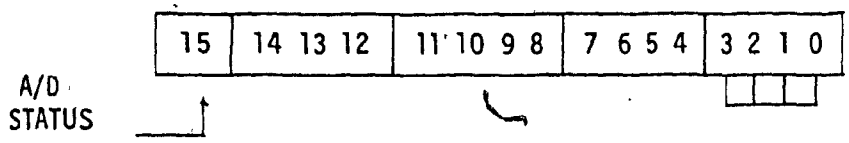


Fig. III.D.10 QUADRATURE CHANNEL INPUT PORT PIN ASSIGNMENT

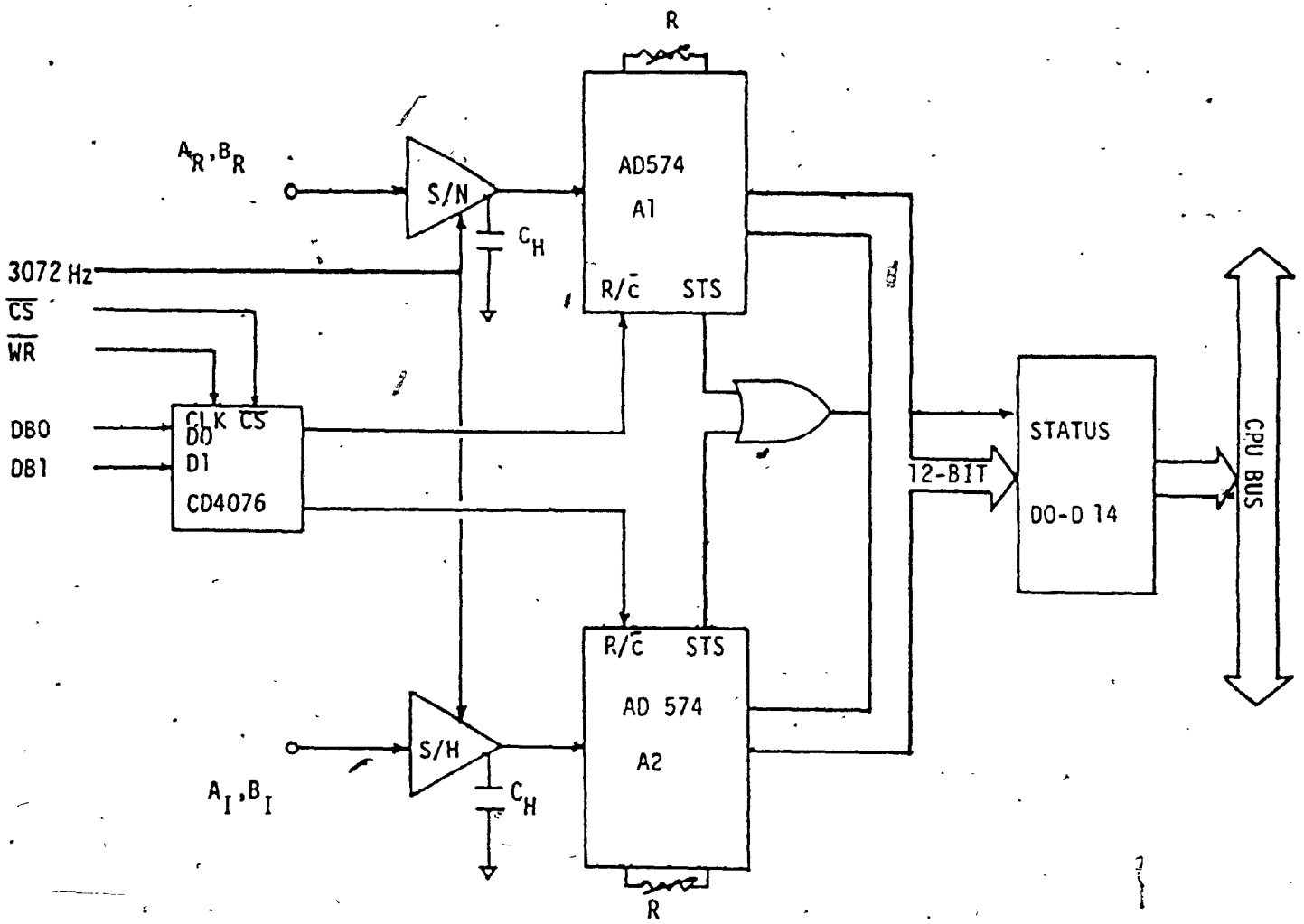


Fig. III.D.11 QUADRATURE CHANNEL A/D CONVERTOR

III.D.6 THE ANTI-ALIASING FILTER

The tones transmitted by the Bottom unit occupy a bandwidth of approximately 2048 Hz. These tones are sampled at 3072 Hz for 160 ms to produce 512 complex points which are stored in the FFT input buffer. Since the sample rate is relatively low, there is a need to band limit the input signal to prevent aliasing [III.D.2]. An elliptic filter was selected for this purpose as these filters have the fastest transition between the passband and stopband.[III.A.1]. A bandpass filter having a bandwidth of 2048 Hz and a center frequency of 8192 Hz was designed with a passband ripple of $\leq$ 1.5 dB and a return lobe attenuation of at least 40 dB.

The filter was tuned to have a first stopband zero (null) at 8192 $\pm$1536 Hz (8192 $\pm$ 3072/2) Hz. Since precise control of the parameters of the filter is required, a state variable (biquad) elliptic function approach was selected. On the basis of sensitivity and flexibility, the biquad configuration is the optimum method for constructing precision active elliptic-function bandpass filters. [III.A.1]. The transfer function for this type of filter is given in Eq. (III.D.4.). The circuit diagram for the filter is illustrated in Figure III.D.12. [III.A.1].

For the case where $f_\infty < f_r$, the transfer function is given by

$$T(s) = -\frac{R_6}{R}\,\frac{s^2 + \frac{1}{R_2R_3C^2}\left(1 - \frac{R_3R}{R_4R_5}\right)}{s^2 + \frac{1}{R_1C} + \frac{1}{R_2R_3C^2}} \qquad \text{(III.D.4.)}$$

when $f_\infty > f_r$, the corresponding transfer function is

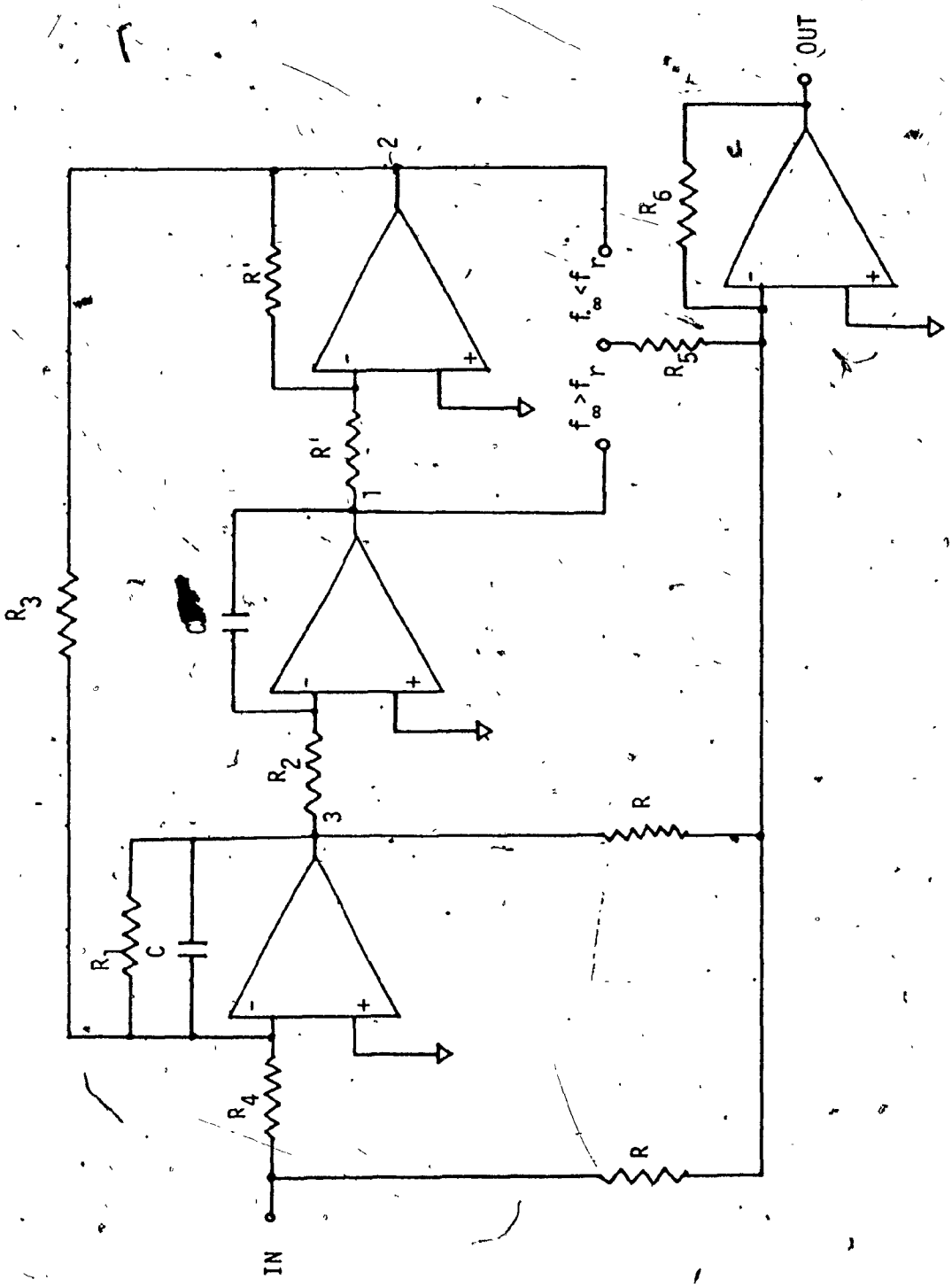


Fig. III.D.12 BIQUAD ELLIPTIC-FUNCTION BANDPASS FILTER

$$T(s) = -\frac{R_6}{R}\,\frac{s^2 + \frac{1}{R_2R_3C^2}\left(1 + \frac{R_3R}{R_4R_5}\right)}{s^2 + \frac{1}{R_1C}s + \frac{1}{R_2R_3C^2}} \qquad \text{(III.D.4.)}$$

where f_∞ is the notch frequency and f_r is the resonant frequency.

The complete filter is composed of five sections: two highpass, two lowpass, and one bandpass section. The response curves for each section are illustrated in Figure III.D.13. The total response of the filter is shown in Figure III.D.14. A UAF41, universal active filter produced by Burr Brown is employed in the design of each section. The configuration shown in Figure III.D.12. is used for the lowpass and highpass filter configuration. By connecting R_5 either to node 1 or to node 2, the zero (null) can be located above or below the resonant frequency. For the bandpass configuration the output is obtained from node 3. A block diagram, Figure III.D.15, shows the order in which the different sections are cascaded. Design equations used to obtain resistor and capacitor values are given in the Appendix. VI.D.1 Table III.D.3. lists the resonant frequency f_r, the Quality factor Q, and the notch frequency f_∞, for each section.

SECTION	TYPE	f_r(Hz)	f_∞(Hz)	Q
1	LOW PASS	8866	10193.5	17.5
2	HIGH PASS	7450.9	6177.6	17.5
3	LOW PASS	9211.1	9791.7	62.6
4	HIGH PASS	7171.7	6746.5	62.6
5	BANDPASS	8127.7	-	10.2

Table III.D.3. SPECIFICATIONS OF ELLIPTIC FILTER SECTIONS

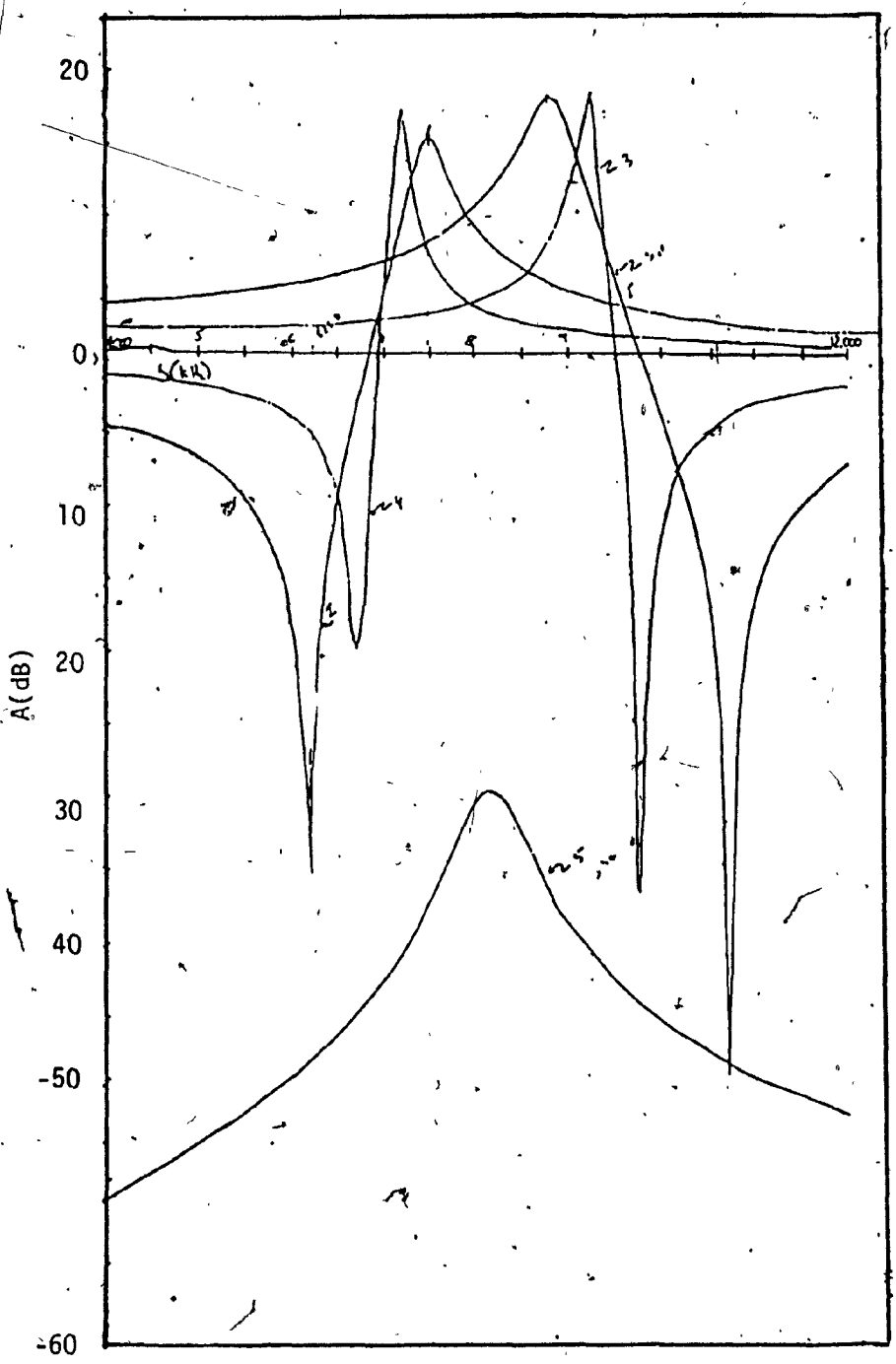


Fig. III.D.13 RESPONSE CURVES OF EACH SECTION

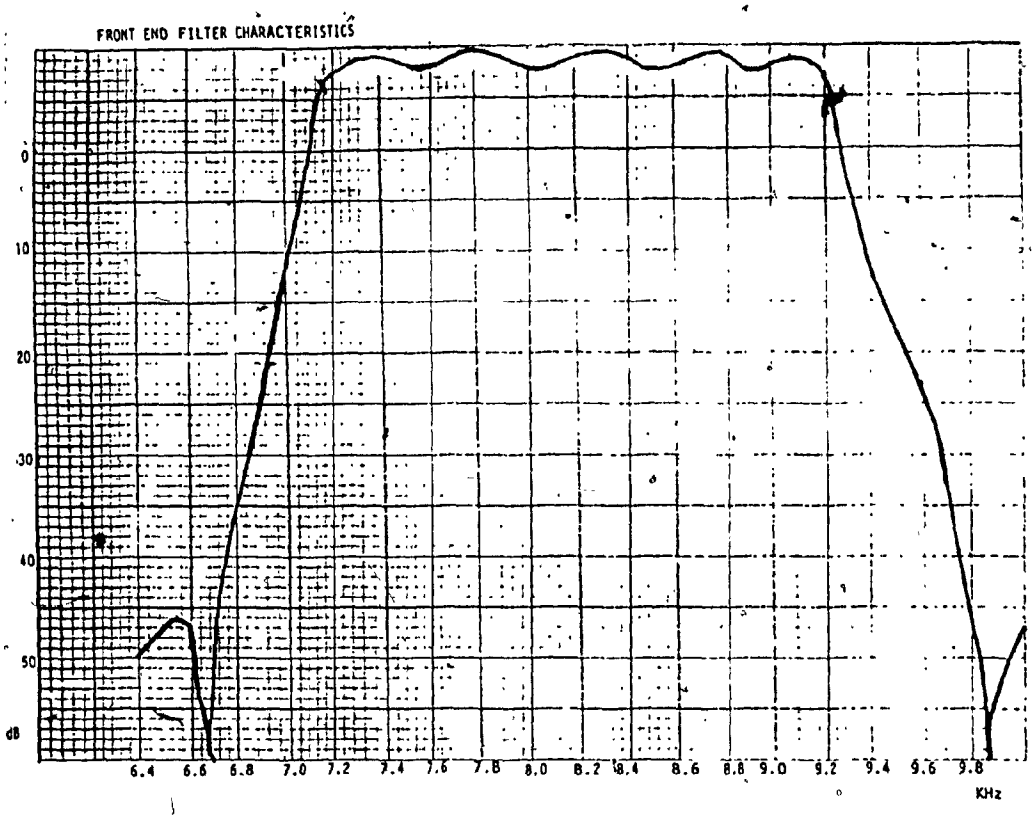


Fig. III.D.14 RESPONSE OF ANTI-ALIASING FILTER

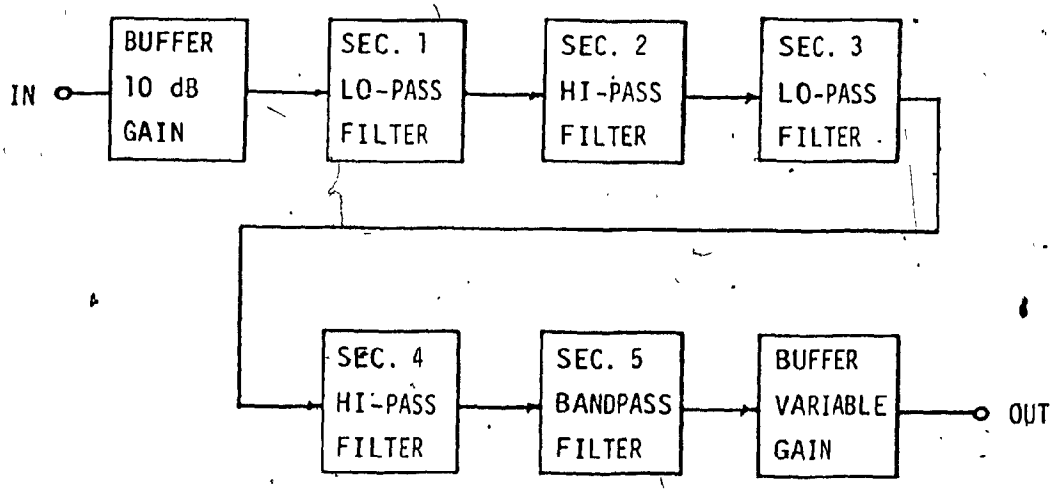


Fig. III.D.15 CASCADED FILTER SECTIONS

The resonant frequency f_r, can be adjusted by varying R_3. Resonance is monitored at node 3 (see Figure III.D.12) and is determined by the phase shift of 180° between node 3 and the input. The Q of each section is controlled by R_1. Frequency f_∞, the notch frequency, can be adjusted by R_5. The biquad approach is a highly stable and flexible implementation for precision active elliptic function filters. [III.A.1].

An impedance matching buffer precedes the elliptic filter. The buffer has an input impedance of 1600 ohms, to match the tranducer output impedance and provides a gain of 10 dB for the signals before filtering. An output buffer with a variable gain is used to amplify the band limited signals. The total gain of the filters and amplifiers is adjusted for 18 dB.

III.E. FAST FOURIER TRANSFORM PROCESSOR

III.E.1 INTRODUCTION

In the dense incoherent MFSK system employed in the Bottom unit, the data tones are spaced 12 Hz apart, while the pilot tones are spaced 24 Hz away from the nearest data tone as shown in Figure III.E.1. The function of the Deck unit is to demodulate these tones so as to reproduce the data bits. A problem encountered in the design of the Deck unit was to select a method for conversion which was simple, efficient and cost effective. The simplest method to detect the presence of a tone would be to design a bandpass filter at the tone frequency and to test for the presence of energy at the output of the filter. This approach would require a total of 164 bandpass filters, each with a bandwidth of 12 Hz as shown in Figure III.E.2. This method was not employed, as the task of building 164 bandpass filters with narrow bandwidths would be tedious and certainly not cost-effective, besides it is doubtful that reliable filter-to-filter phase and amplitude tracking could be achieved and maintained.

An alternate approach would be to design a single filter and allow the input to be swept accross the frequency band of interest. Refer to Figure III.E.3. In this approach the incoming signal is multiplied by a local oscillator which is swept so as to cover the whole frequency spectrum of interest. By associating the instantaneous oscillator frequency with the energy out of the filter, the presence of tones and their respective frequencies can be ascertained. Since the Bottom unit transmits tones for only 125 ms, the oscillator would have to be swept very rapidly. Unfortunately, though, the sweep rate cannot be too fast because of the response time of the filter. The filter

takes a finite time to respond to changes in its input; the narrower the filter, the longer it takes to respond. [III.E.1].

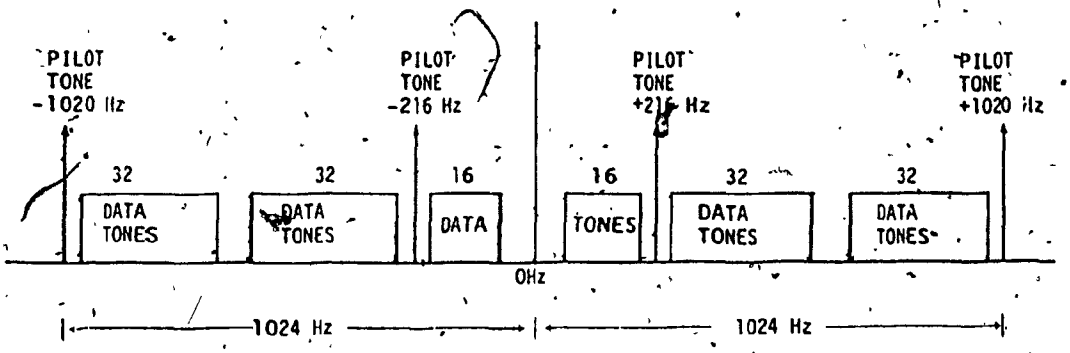


Fig. III.E.1 DATA AND PILOT TONE SPECTRUM

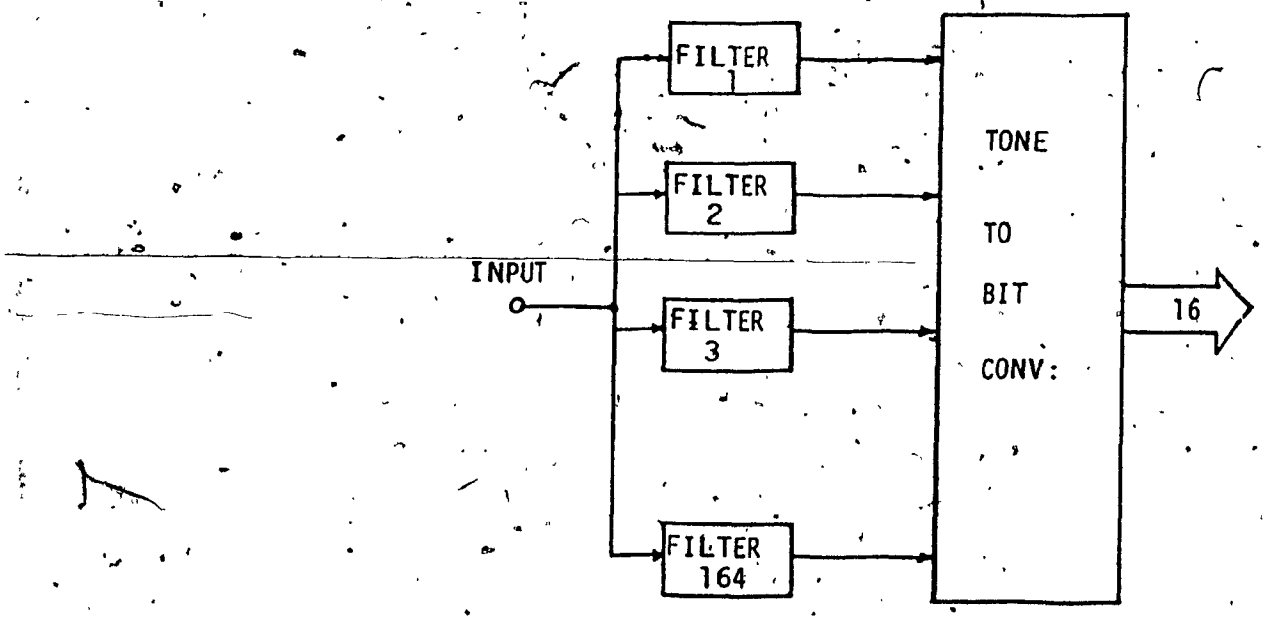


Fig. III.E.2 PARALLEL FILTER TONE-TO-BIT CONVERTOR

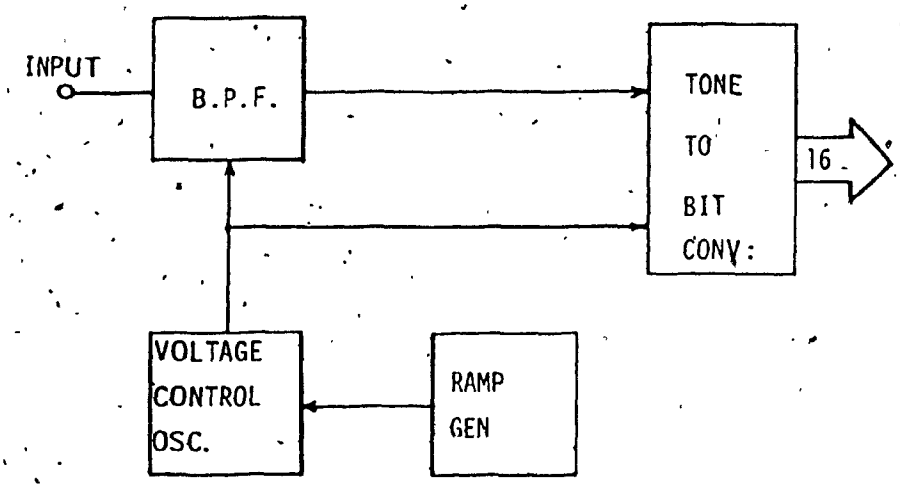


Fig. III.E.3 SWEPT FREQUENCY TONE-TO-BIT CONVERTOR

The final approach examined was that of a Dynamic Signal Analyzer. Dynamic Signal Analyzers are based on a high speed calculation routine which acts like a parallel filter analyzer, discussed earlier, but without the low resolution limitations. Dynamic Signal Analyzers are based on the Discrete Fourier Transform (DFT). The DFT is a method for transforming both time-and frequency-limited data from the time domain to the frequency domain. The DFT based analyzer is extremely accurate; although, because it implies digital implementation, a longer time must be allowed for computation as compared to a parallel filter analog approach. This, however, is not an obstacle in this application as the period between transmissions is 250 ms, with tones actually transmitted for 125 ms. The DFT processing could then be performed during the dead time. In the next section a study of various Fast Fourier Transform (FFT) techniques is presented and the approach best-suited to the application is chosen for implementing the DFT.

III.E.2 RATIONALE FOR FFT IMPLEMENTATION TECHNIQUE

The set of algorithms known as the Fast Fourier Transform (FFT) consists of a variety of methods for reducing the computational time required to compute a discrete Fourier transform (DFT) [III.E.2]. The best known algorithms are the radix-2-decimation-in-time and decimation-in-frequency algorithms.

a. Radix-2 FFTS

The DFT of a finite duration sequence $\{x(n)\}$, $0 \le n \le N-1$ is defined as,

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j(2\pi/N)nk} \qquad k=0,1,\ldots,N-1 \qquad \text{(III.E.1)}$$

Letting

$e^{-j(2\pi/N)} = \omega$, equation (III.E.1) becomes,

$$X(k) = \sum_{n=0}^{N-1} x(n)\omega^{nk} \qquad \text{(III.E.2)}$$

A direct evaluation of an N-point DFT requires $(N-1)^2$ complex multiplications and $N(N-1)$ complex additions when $x(n)$ is a complex sequence. Therefore, for a 512-point DFT this translates to $\approx 2^{18}$ multiplications and $(512)\times(511) \approx 2^{18}$ additions. This obviously would require large amounts of processing time. The idea behind the FFT is to break the original N-point sequence into two shorter sequences, the DFT's of which can be combined to give the DFT of the original N-point sequence.

Therefore if N were even and the original N-point sequence were broken into two, (N/2)-point sequence, it would require on the order of $(N/2)^2 \cdot 2 = N^2/2$ complex multiplications to evaluate the desired N-point DFT, this result is a savings of a factor of 2, minus the time required to combine the two results. [III.E.2.].

Let $x(n)$ be the N-point sequence we wish to evaluate; furthermore, let $x_1(n)$ and $x_2(n)$ be the odd and even sub-sequences of $x(n)$.

$$x_1(n) = x(2n) \quad \text{where } n=0,1,2,\ldots, N/2-1 \tag{III.E.3}$$

$$x_2(n) = x(2n+1) \quad \text{where } n=0,1,2,\ldots,N/2-1 \tag{III.E.4}$$

The N-point DFT of $\{x(n)\}$ can be written as

$$X(k) = \sum_{\substack{n=0 \\ n \text{ even}}}^{N-1} x(n)\, \omega_N^{nk} + \sum_{\substack{n=0 \\ n \text{ odd}}}^{N-1} x(n)\omega_N^{nk} \tag{III.E.5}$$

$$= \sum_{n=0}^{N/2-1} x(2n)\, \omega_N^{2nk} + \sum_{n=0}^{N/2-1} x(2n+1)\omega_N^{(2n+1)k} \tag{III.E.6}$$

but since $\omega_N^2 = [e^{-j(2\pi/N)}]^2 = e^{-j[2\pi/(N/2)]} = \omega_{N/2}$ we may tranform Equation (III.E.6) to,

$$X(k) = \sum_{n=0}^{N/2-1} x_1(n)\omega_{N/2}^{nk} + \omega_N^k \sum_{n=0}^{N/2-1} x_2(n)\omega_{N/2}^{nk} \tag{III.E.7}$$

$$= X_1(k) + \omega_N^k X_2(k) \tag{III.E.8}$$

where $X_1(k)$ and $X_2(k)$ are seen to be the N/2-point DFT's of the sub-sequences, $x_1(n)$ and $x_2(n)$. Equation (III.E.8) shows that the N

point DFT. $X(k)$ can be decomposed into two N/2-point DFT's that can be combined according to the rule of Equation (III.E.9).

Since $X(k)$ is defined for $0 \leq k \leq N-1$ and $X_1(k)$ and $X_2(k)$ are defined for $0 \leq k \leq N/2-1$, a rule must be given for how to interpret Equation (III.E.8) for values of $k \geq N/2$. Due to the periodicity property of the DFT we have,

$$X(k) = \begin{cases} X_1(k) + \omega_N^k X_2(k) & 0 \leq k \leq N/2-1 \\ X_1(k-N/2) + \omega_N^k X_2(k-N/2) & N/2 \leq k \leq N-1 \end{cases} \quad \text{(III.E.9)}$$

Since $\omega_N^{k+N/2} = -\omega_N^k$ then equation (III.E.9) becomes

$$X(k) = X_1(k) + \omega_N^k X_2(k), \qquad 0 \leq k \leq N/2-1$$

$$= X_1(k-\frac{N}{2}) - \omega_N^{k-N/2} X_2(k-\frac{N}{2}) \qquad \frac{N}{2} \leq k \leq N-1 \quad \text{(III.E.10)}$$

Figure III.E.4 illustrates the processes involved in evaluating an eight-point DFT using two four-point transforms. The input sequence $X(n)$ is first shuffled into even and odd members to give $X_1(n)$ and $X_2(n)$, which are then transformed to give $X_1(k)$ and $X_2(k)$.

The right side of Figure III.E.4 defines the open circle as being an adder-substracter; the sum always appears at the top and the difference at the bottom. The arrow (⟶) is defined as a multiplier, with the value of the multiplier (a) being given above the arrow. In general, all variables are complex numbers. [III.E.2.].

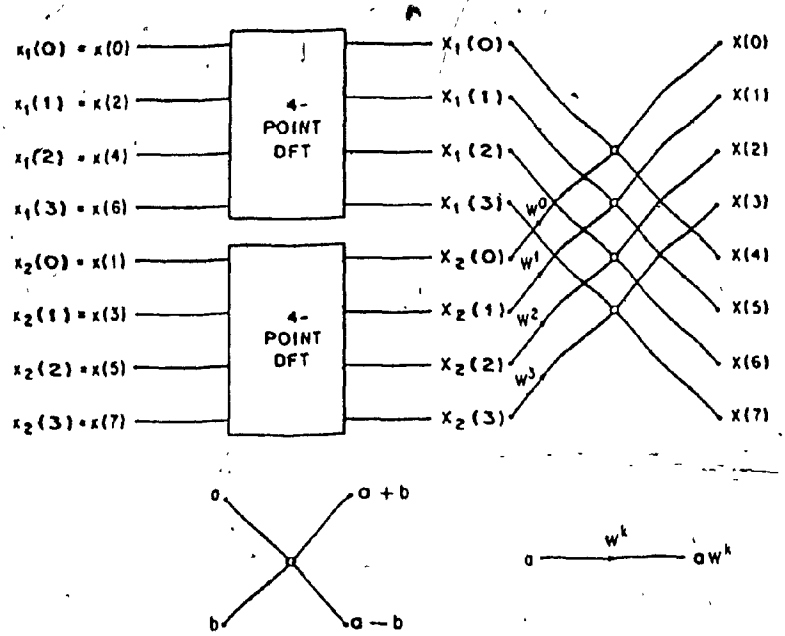


FIG. III.E.4 CONSTRUCTION OF AN EIGHT-POINT DFT FROM TWO FOUR-POINT DFT'S

In a manner similar to the one described above, the (N/2)-point DFT's can now be expressed as a combination of (N/4)-point DFT's: i.e., $X_1(k)$, $0 \leq k \leq N/2-1$ can be written as

$$X_1(k) = A(k) + \omega_{N/2}^{k} B(k) \qquad \text{(III.E.21)}$$

or

$$X_1(k) = A(k) + \omega_{N}^{2k} B(k) \qquad \text{(III.E.22)}$$

where A(k) is the (N/4)-point DFT of the even sub-sequence of $X_2(n)$

and B(k) is the (N/4)-point DFT of the odd sub-sequence of $X_1(n)$. Figure III.E.5 shows the resulting flowgraph when the four-point DFT's of Figure III.E.4 are evaluated using Equation (III.E.22).

The process above of reducing an L-point DFT (L is a power of 2) to (L/2)-point DFT's can be continued until we are left with two-point DFT's to evaluate. If L=8, a two-point DFT,

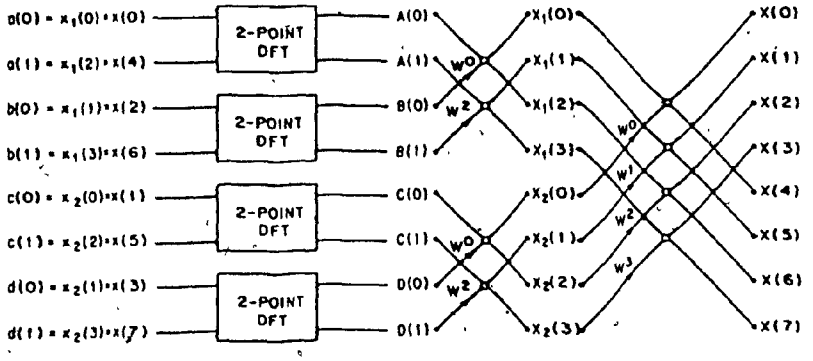


FIG. III.E.5 CONSTRUCTION OF AN EIGHT-POINT DFT FROM TWO FOUR-POINT DFT'S THAT ARE IN TURN CONSTRUCTED FROM TWO-POINT DFT'S.

F(k), k=0,1 may be evaluated (using no multiplications) as

$$F(0) = f(0) + f(1)\ \omega_8^0$$

$$F(1) = f(0) + f(1)\ \omega_8^4 \qquad \text{(III.E.23)}$$

where f(n), n=0,1 is the two-point sequence being transformed. Since $\omega_8^0 = 1$, and $\omega_8^4 = -1$, no multiplications are required to evaluate, (III.E.23). Thus, the eight-point DFT of Figure III.E.4 and (III.E.5)

finally reduces to that of Figure III.E.6.

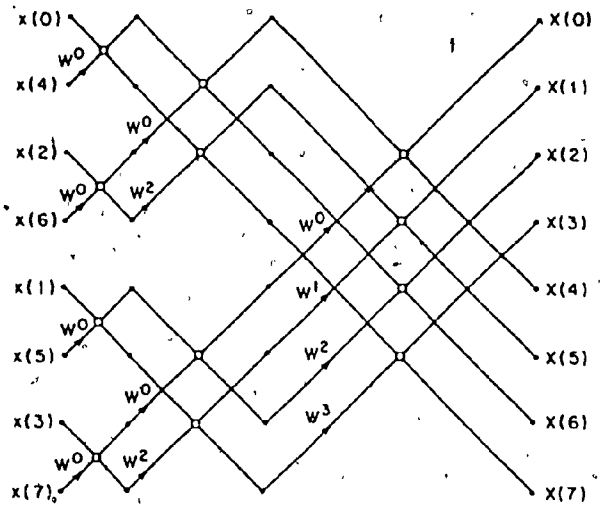


Fig. III.E.6 EIGHT-POINT FFT OBTAINED BY SUCCESSIVE SPLITTING INTO TWO'S.

Each stage of the FFT required $N/2$ complex multiplications, to combine the results of the previous stage. Since there are $(\log_2 N)$ stages, the number of complex multiplications required to evaluate an N-point DFT is approximately $N/2\log_2 N$. The algorithm described above is called the decimation-in-time (DIT) algorithm since at each stage of the process the input time sequence is divided, or decimated, at each stage into smaller sequences for processing [III.E.1].

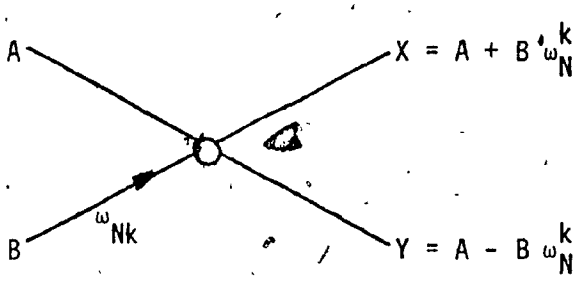
b. Decimation-in-Time (DIT) Algorithm

The basic operation of the DIT algorithm is the so-called Butterfly in which two inputs A and B (which are usually complex quantities) are combined to give two outputs X and Y by Equation III.E.24 shown below.

$$X = A + \omega_N^k B$$

$$Y = A - \omega_N^k B \qquad \text{(III.E.24)}$$

The notation for the flow graph of the Butterfly is shown below



This means that for the DIT algorithm each stage requires N/2 multiplications, but the value of $B\omega_N^k$ has to be computed and saved before any addition or substraction can take place. In hardware terms this would mean an extra buffer for storage; furthermore, no parallel processing such as additions and multiplications can simultaneously be performed.

Another point worth noting about the DIT algorithm is that for the output sequence to be in natural order (i.e., X(k), k=0,1,2,3,...,N-1), the input sequence has to be stored in shuffled order. The shuffled order is the bit-reversed order shown in Table III.E.1. [III.E.2.].

TABLE 1A

INDEX	BINARY REP:	BIT REV: BINARY	BIT REV: INDEX
0	000	000	0
1	001	100	4
2	010	010	2
3	011	110	6
4	100	001	1
5	101	101	5
6	110	011	3
7	111	111	7

Table III.E.1 BIT-REVERSED INDEX

This is equivalent to twisting the address lines to the input buffer memory [III.E.2].

c. Decimation-in-Frequency (DIF) Algorithm

Another form of FFT algorithm, for Nth power of 2, is the so called decimation-in-frequency (DIF) algorithm. In this method the input sequence $\{x(n)\}$ is partitioned into two sub-sequences each of length (N/2) samples in the following manner. The first sequence $\{x_1(n)\}$ consists of the first N/2 points of $\{x(n)\}$, and the second sequence $\{x_2(n)\}$ consists of the second N/2 points of $\{x(n)\}$; thus,

$$x_1(n) = x_n \quad \text{where} \quad n=0,1,\ldots,N/2-1$$

$$x_2(n) = x(n+N/2) \quad \text{where} \quad n=0,1,\ldots,N/2-1 \qquad \text{(III.E.25)}$$

The N-point DFT of $x(n)$ can now be written in the form

$$X(k) = \sum_{n=0}^{N/2-1} x(n)\, \omega_N^{nk} + \sum_{n=N/2}^{N-1} x(n)\, \omega_N^{nk} \qquad \text{(III.E.26)}$$

$$= \sum_{n=0}^{N/2-1} x_1(n)\, \omega_N^{nk} + \sum_{n=0}^{N/2-1} x_2(n)\, \omega_N^{(n+N/2)k} \qquad \text{(III.E.27)}$$

$$X(k) = \sum_{n=0}^{N/2-1} [x_1(n) + e^{-j\pi k} x_2(n)]\, \omega_N^{nk} \qquad \text{(III.E.28)}$$

where $\omega^{Nk/2} = e^{-j\pi k}$.

Considering the even and odd samples of the DFT separately,

$$X(2k) = \sum_{n=0}^{N/2-1} [x_1(n) + x_2(n)]\, (\omega_N^2)^{nk} \qquad \text{(III.E.29)}$$

$$= \sum_{n=0}^{N/2-1} [x_1(n) + x_2(n)]\, \omega_{N/2}^{nk} \qquad \text{(III.E.30)}$$

$$X(2k+1) = \sum_{n=0}^{N/2-1} [(x_1(n) - x_2(n)]\, \omega_N^{n(2k+1)} \qquad \text{(III.E.31)}$$

$$= \sum_{n=0}^{N/2-1} \{[x_1(n) - x_2(n)]\, \omega_N^{n}\}\, \omega_{N/2}^{nk} \qquad \text{(III.E.32)}$$

Equations (III.E.30) and (III.E.32) show that the even and odd-valued samples of the DFT can be obtained from the (N/2)-point DFT's of the sequences $f(n)$ and $g(n)$, respectively, where,

$$f(n) = x_1(n) + x_2(n)$$

$$n=0,1,2,\ldots,N/2-1 \qquad \text{(III.E.33)}$$

$$g(n) = [x_1(n) - x_2(n)]\ \omega_N^n$$

Thus, we have reduced the problem of obtaining an N-point DFT to one of obtaining two N/2-point DFTs. Figure III.E.7 illustrates the procedure for N=8 [III.E.2].

d. The Constant Geometry Algorithm

A constant geometry algorithm was chosen because of its simple hardware design. In this algorithm the butterfly outputs are not put back where they come from so it is not an in-place algorithm; however the indexing is kept constant from stage to stage. This permits a simple hardware implementation. The inputs are normally ordered while the outputs are bit reversed. An N-point constant geometry algorithm does require 2N registers as opposed to N-registers for in-place algorithms but in-place algorithms require more complex timing for hardware. Therefore the not-in place algorithm was chosen. Fig. III.E.8 shows the implementation of the algorithm for a 16-point constant geometry DFT.

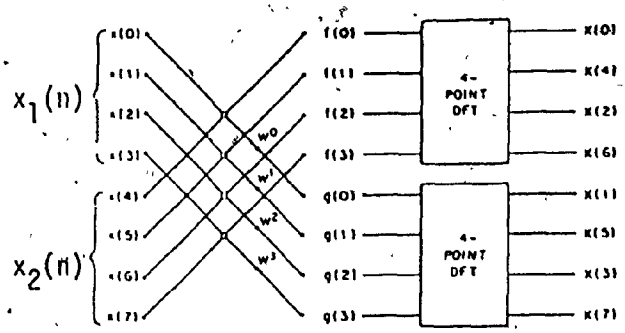


Fig. III.E.7a REDUCTION OF AN EIGHT-POINT DFT TO TWO FOUR-POINTS DFT'S BY DECIMATION-IN-FREQUENCY

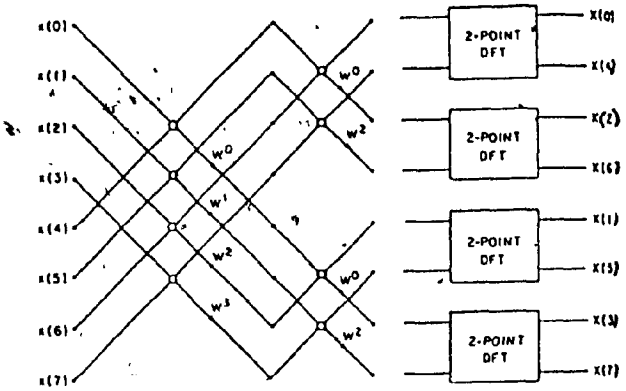


Fig. III.E.7b FURTHER REDUCTION OF FIG. III.E.7a

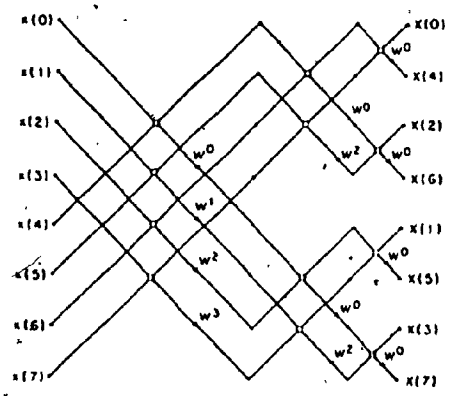


Fig. III.E.7c COMPLETE EIGHT-POINT IN-PLANE DECIMATION-IN-FREQUENCY FFT

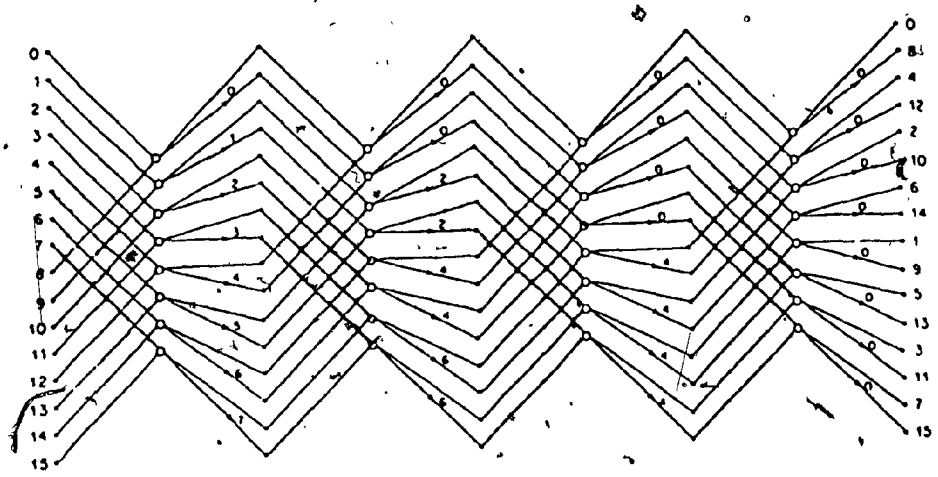


Fig. III.E.8 CONSTANT GEOMETRY ALGORITHM, RADIX 2, 16 POINTS NOT-IN-PLACE, NORMALLY ORDERED INPUTS, BIT-REVERSED OUTPUTS

The circles correspond to one butterfly operation which for a complex DFT consists of four additions and four multiplications. The complex input samples A and B occupy two words each (for real, imaginary) which are separated by N/2 samples, where N is the total number of sample points. The outputs, X and Y, are stored in consecutive locations. [III.E.2].

e. DIT or DIF Implementation

The constant geometry FFT may be implemented using either DIT or DIF, as previously described. In comparing these two computational algorithms two differences are apparent. In the DIT algorithm, the input is bit-reversed while the outputs are in natural order: the

reverse, however, is true for the DIF. The second difference is a more important one; in the DIF butterfly the multiplication takes place after the add - substract operation. This enables some form of pipelining as the multiplication can be implemented while the sum quantities are being stored. The DIT implementation requires the multiplication to occur before any add - substract operation. The two butterflies are illustrated below. The decimation in frequency algorithm was chosen for the butterfly operations of the constant geometry FFT.

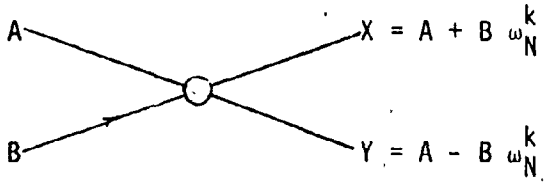


Fig. III.E.9a THE DIT BUTTERFLY

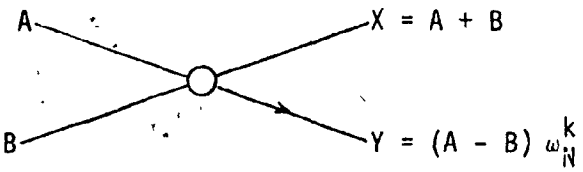


Fig. III.E.9b THE DIF BUTTERFLY

III.E.3 GENERAL DESCRIPTION OF THE FFT PROCESSOR HARDWARE

The FFT processor is a stand-alone processor that has two modes of operation. The two modes are: (1) loading or outputting data, i.e., communication with the CPU and (2) performing a 512-point complex FFT. Aside from these two modes, the only dependence it has on the CPU is the *start-FFT* command. The FFT processor itself consists of

the following major components.

(1) A high speed butterfly (HSB) which performs the elemental two-point complex transformation for the DIF operation.

(2) Buffers consisting of two 1K x 16 bits of RAM, which can hold 1024 complex points of data.

(3) Coefficient tables stored in EPROM (512 words).

(4) Indexing and control circuits which generate addresses and control signals for the FFT processor.

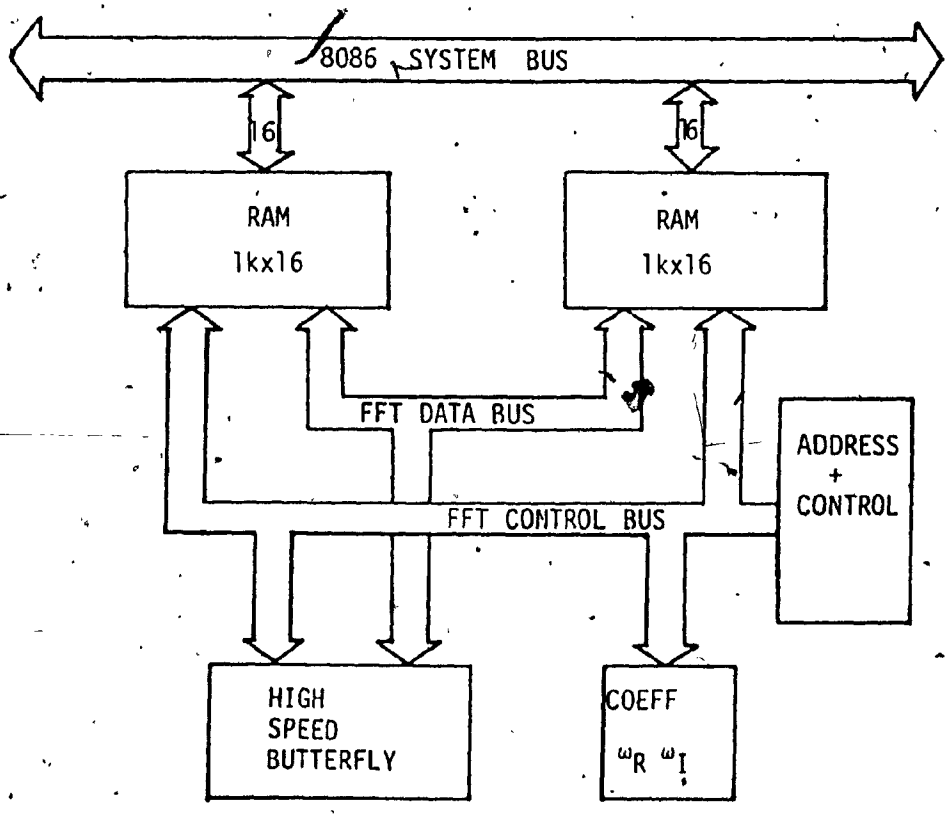


Fig. III.E.10 FFT PROCESSOR BLOCK DIAGRAM

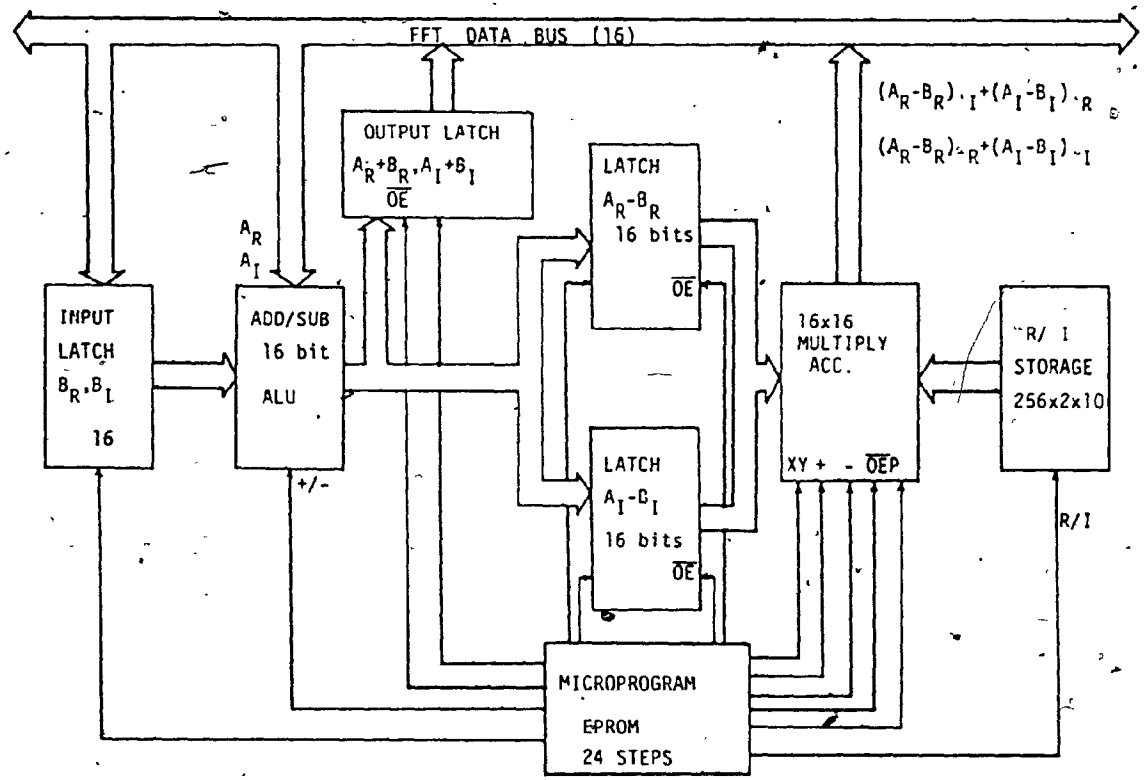


Fig. III.E.11 BLOCK DIAGRAM HIGH SPEED BUTTERFULY

a. The High Speed Butterfly

The block diagram of the high speed butterfly processor is shown in Fig. III.E.11. It consists of a 16-bit-adder/subtractor, a 16x16 multiply-accumulator, 16-bit latches to hold results temporarily, a 512x16 coefficient table and a twenty-four step microprogram. Since speed was not a prime factor most operations of the butterfly occur sequentially.

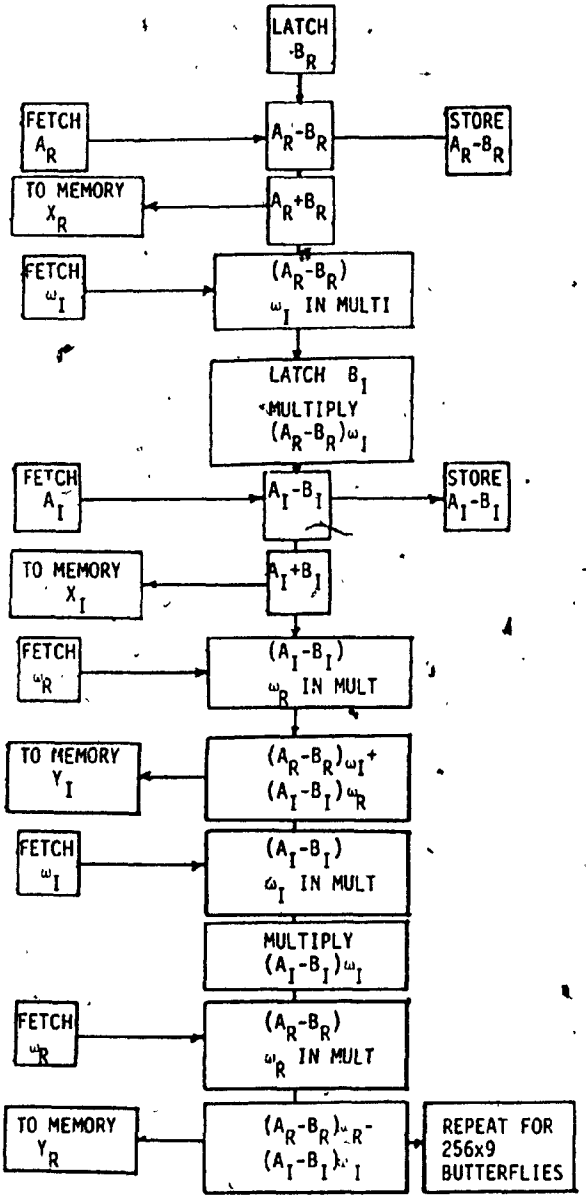
The high speed butterfly performs the complex arithmetic operation described by Equation (III.E.34)

$$X = A + B$$
$$Y = (A-B)\omega \qquad \text{(III.E.34)}$$

Equation (III.E.34) can be expanded into the following components,

$$X_R = A_R + B_R \qquad \text{(III.E.35)}$$
$$X_I = A_I + B_I \qquad \text{(III.E.36)}$$
$$Y_R = (A_R-B_R)\omega_R - (A_I-B_I)\omega_I \qquad \text{(III.E.37)}$$
$$Y_I = (A_I-B_I)\omega_R + (A_R-B_R)\omega_I \qquad \text{(III.E.38)}$$

The four quantities A_R, B_R, A_I and B_I are fetched from the memory buffers, and the two coefficients ω_R, ω_I from the coefficient tables. Since the algorithm chosen for the FFT is the radix-2 constant geometry DIF algorithm, A_R, A_I and B_R, B_I are separated by N/2 points in the memory, as shown in Figure III.E. . Output data from the butterfly is stored sequentially. The microprogram provides two select lines which determine A or B, and Real or Imaginary. The flow-chart for



X_R, X_I, Y_R, Y_I ARE RESULTS OBTAINED AFTER HSB

Fig. III.E.12 SEQUENCE OF OPERATIONS FOR ONE BUTTERFLY

one butterfly operation is shown in Figure III.E.12. A detailed description of the hardware implementation follows.

The sequence of operations in the high speed butterfly is optimised so that a minimum number of operations is required while keeping the implementation simple. The butterfly hardware consists of a sixteen-bit adder/subtractor, a 16x16-multiplier-accumulator, and registers for temporary data storage.

b. The 16-bit Adder-Subtractor

The 74181 arithmetic logic units (ALU) are used for the add-subtract operation. The 74181 ALU's are 4-bits wide and have a typical add-subtract time of 140 ns [III.D.6]: add or subtract functions are implemented by conditioning the appropriate select lines via a microprogram.

Referring to Figure III.E.13, register latches A6 and A7 are 8-bit octal latches [III.B.2]. They are used to hold the data samples B_R and B_I from the FFT buffers. The outputs of these latches are always enabled, while the strobe is provided by the microprogram. After a data sample corresponding to B_R or B_I is latched, the FFT control circuit selects A_R or A_I. Therefore, the data points for addition or subtraction are available at the input to the 74181 ALU's. The four 74181 ALU's B3, B4, B5, and B6 are wired to provide sixteen bit arithmetic. The microprogram first conditions the select lines for addition and A_R+B_R is produced. A_R+B_R is then strobed into two 8282 octal latches A4, A5 before being written into memory. To write this sum data the microprogram first strobes it into A4, A5, then it enables the

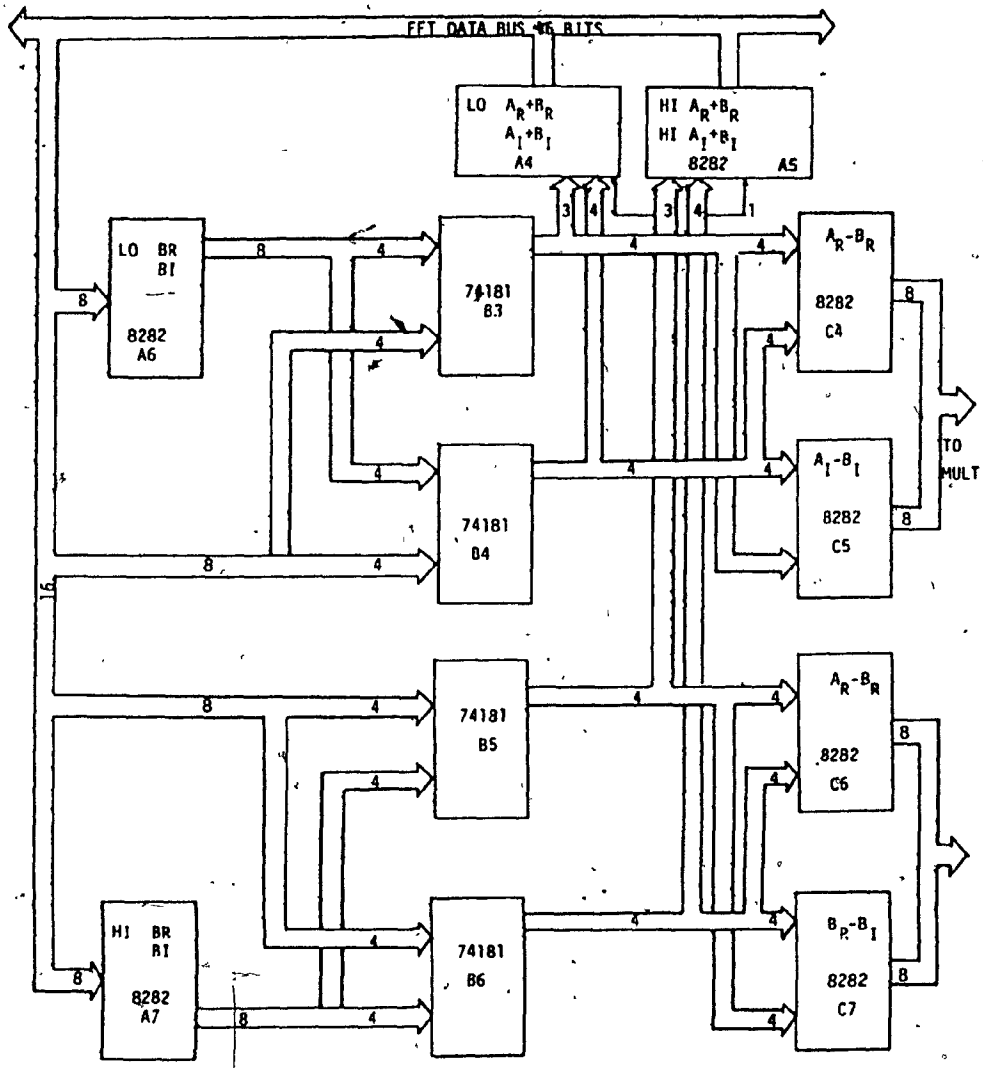


Fig. III.E.13 ADD/SUBTRACT IMPLEMENTATION

output of A4, A5 and finally provides the write pulse. The microprogram then changes the select lines on the ALU to a subtract operation. A_R-B_R is then strobed into the 8282 latches C4, C6 for input to the multiplier. Similarly, A_I and B_I are fetched from the FFT buffer, and A_I+B_I is strobed and then written into memory; and A_I-B_I is stored in C5 and C7. C4, C5, C6, C7 all have output enables and the microprogram enables the appropriate pair when required by the multiplier. In order to retain the same word size in the FFT processing, the results from the butterfly have to be scaled. For the sum quantities A_R+B_R and A_I+B_I, the least significant bit D_0 from the adder is dropped and the most significant bit is extended up one bit. In practice, this has the effect of dividing the data by two (shift right one bit). Sum of product quantities are treated similarly. Refer to the Section on the multiplier for more details.

c. The Hi Speed Multiplier-Accumulator

In the previous section the manner in which the sum and difference quantities are produced was described. The sum quantities A_R+B_R and A_I+B_I are stored in memory; therefore, all that remains to complete the FFT butterfly is Equation (III.E.39)

$$Y_R = (A_R-B_R)\omega_R - (A_I-B_I)\omega_I \qquad \text{(III.E.39a)}$$

$$Y_I = (A_I-B_I)\omega_R + (A_R-B_R)\omega_I \qquad \text{(III.E.39b)}$$

The quantities A_R-B_R and A_I-B_I are already computed in the previous stages and are stored in C4, C5, C6 and C7 registers whereas, ω_R

and ω_I are stored in two 2758 EPROMS.

To complete the computation, four multiplies and one add and subtract are required. The TRW 1010J is suitable for this purpose. The TRW 1010J is a 64-pin high speed multiplier-accumulator. This multifunction arithmetic unit is capable of performing a 16x16-bit multiplication and product accumulation in 115 ns. See figure for timing [III.E.3].

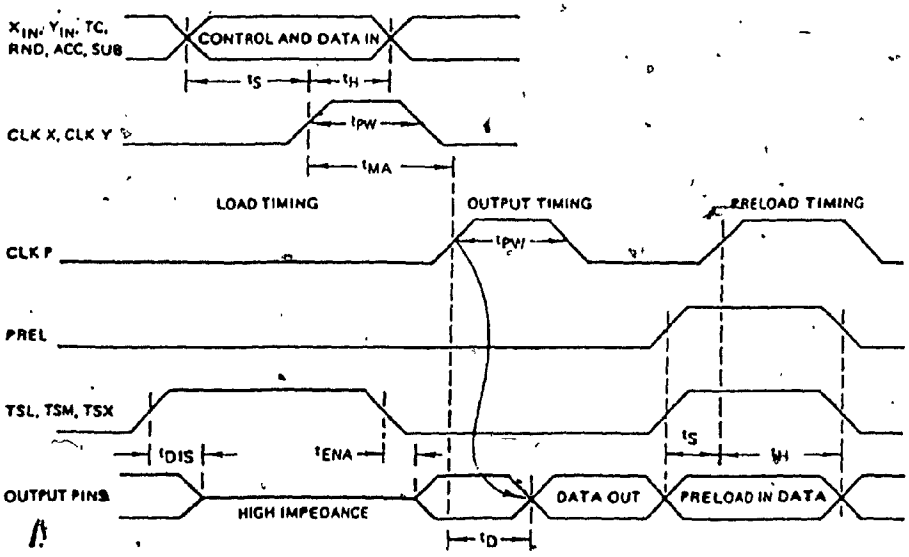


Fig. III.E.14 TIMING DIAGRAM FOR TRW 1010J MULTIPLIER

d. Description of the 16x16 Multiplier

The TRW 1010J multiplier chip, two 16-bit data registers, and one four-bit control register (see Figure [III.E.15]) comprise the 16x16 multiplier. These three registers are all positive edge latches. The X-input word is loaded into the chip on the zero-to-one transition of *CLKX*, and the Y-input word is similarly loaded by *CLKY*. The controls (*ACC*, *SUB*, *TC*, and *RND*) are loaded on the rising edge of [*CLKX* + *CLKY*]. These two clocks are internally or-gated on the chip to form the composite instruction register clock. The output of the multiplier is also latched just before the 3-state buffers. This latch is strobed by the rising edge of *CLKP*. Four control lines affect the output register and the output 3-state buffers. When the preload function is off (*Prel* = 0), the 3-state buffers are controlled by the other 3 lines: *TSM*, *TSL*, *TSX*. When one or more of these lines is low, the corresponding group of output buffers will be on, or low impedance outputs; when they are high, the corresponding buffers are off, or high impedance outputs. When *Prel* = 1, however, all output buffers are turned off and the other three control pins change function. If *Prel* and the other output control pins are high, any data put onto the output pins from an external source will be loaded directly into the output register on the rising edge of *CLKP*. If any of the three controls (*TSM*, *TSL*, *TSX*) are low those corresponding registers will be in hold state.

Four controls (*ACC*, *SUB*, *TC* and *RND*) are loaded into the instruction register on the chip. When *ACC* is low the accumulate function is turned off. The chip will multiply X and Y and bring the product directly to the output register. When *ACC=1*, whatever is in the output register will be added to (*Sub*=0) or subtracted from (*Sub*=1) the next

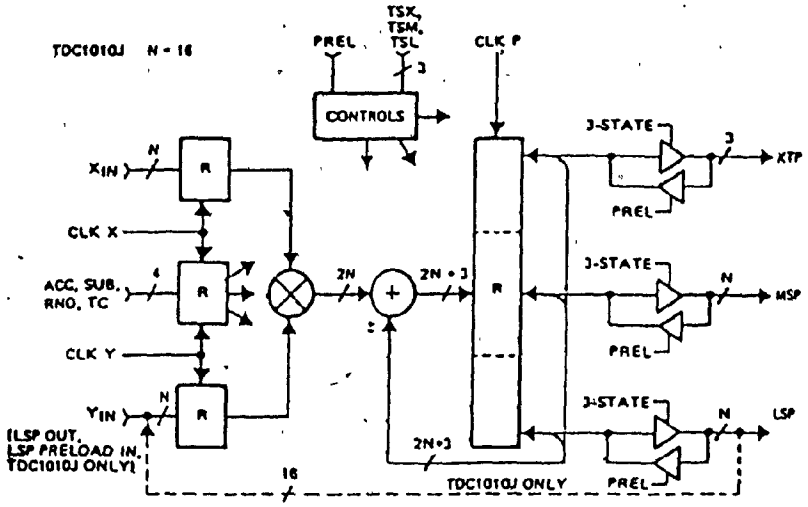


Fig. III.E.15a BASIC BLOCK DIAGRAM OF TDC1010J

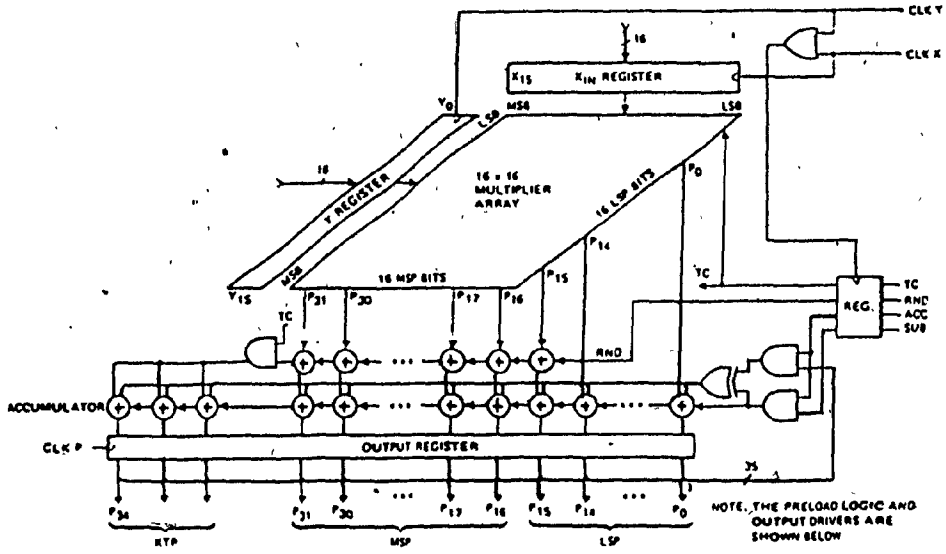


Fig. III.E.15b CONCEPTUAL LOGIC DIAGRAM TDC1010J

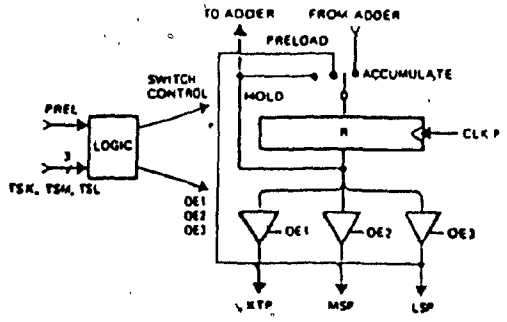


Fig. III.E.15c OUTPUT REGISTER LOGIC TDC1010J

X times *Y* product, and that result will be brought to the output register. *TC* is the pins's complement control. When it is high, the two operands are defined as two's complement numbers, and the multiplier array is adjusted accordingly after the *TC* is low, both input words are assumed to be in sign-magnitude number notation. The *RND* control allows the user to round up the double precision accumulated answer back to single precision, or single precision plus added bits. (The XTP bits). Whenever *RND* control is high, a one will be added to the MSB (most significant bit) of the least significant part (LSP) when the two input words are multiplied. If the MSB of the LSP is one, the carry generated will increment the most significant part (MSP). Three extra bits (XTP) are provided for the sum of products, where each product can be a maximum value. Sixteen-bit single precision answers can be obtained from the output word P19 (LSB) through P34 (MSB). [III.E.4].

e. Application of the TDC 1010J to the FFT Butterfly

The input data registers are fed with (A_R-B_R) and ω_I. These two quantities are strobed into the *X* and *Y* registers of the multiplier. Simultaneously, *ACC*, *SUB*, and *RND* are all inactive and strobed into the control register. The microprogram which provides all the timing signals then strobes the *PCLK* input with a positive going pulse. This results in the product $(A_R-B_R)\omega_I$ being produced and stored in the output buffer.

Next, (A_I-B_I) and ω_R are clocked into the input registers. *ACC* is set high, *Sub*=0 and *RND*=0, with these controls strobed in with the input data. *PCLK* is then activated and the sum of products

$(A_I-B_I)\omega_R + (A_R-B_R)\omega_I$ is computed and stored in the output register. The maximum input word size is 15 bits plus sign. Therefore, each product is 30 bits plus sign; after accumulation the largest number possible is 31 bits plus sign. These bits are obtained from the (MSP) of the multiplier as the product bits P_{16} to P_{31}. Therefore, the input word size is maintained and it is unnecessary to scale them as was the case when the (A_R+B_R) and (A_I+B_I) sum terms were produced. Finally, the MSP output is enabled and the data is written into the FFT buffers. All the control signals, such as output enable, chip select, and write pulses are obtained from the microprogram. Refer to the microprogram timing diagram. From the previous multiplication, (A_I-B_I) is already in the multiplier X-input, therefore ω_R is strobed into the Y-register. ACC, *Sub*, and *RND* are all kept inactive during this period. The microprogram then strobes the *CLKP* line and $(A_I-B_I)\omega_R$ is stored in the output register. The inputs to the multiplier are then changed to (A_R-B_R) and ω_I. ACC and *Sub* are both active for this computation. *CLKP* is again strobed by the microprogram with the result $(A_R-B_R)\omega_R - (A_I-B_I)\omega_I$. The MSP output is enabled and the data is again written into the FFT memory buffers.

f. FFT Start-Status Hardware

Figure III.E.17 shows the logic required for the control of the FFT processor. The $\overline{TEST}$ line, pin number 5 of A2, reflects the status of the FFT processor. When $\overline{TEST}$ is high, the FFT is in progress and when $\overline{TEST}$ is low the FFT is disabled. The test line serve two purposes:

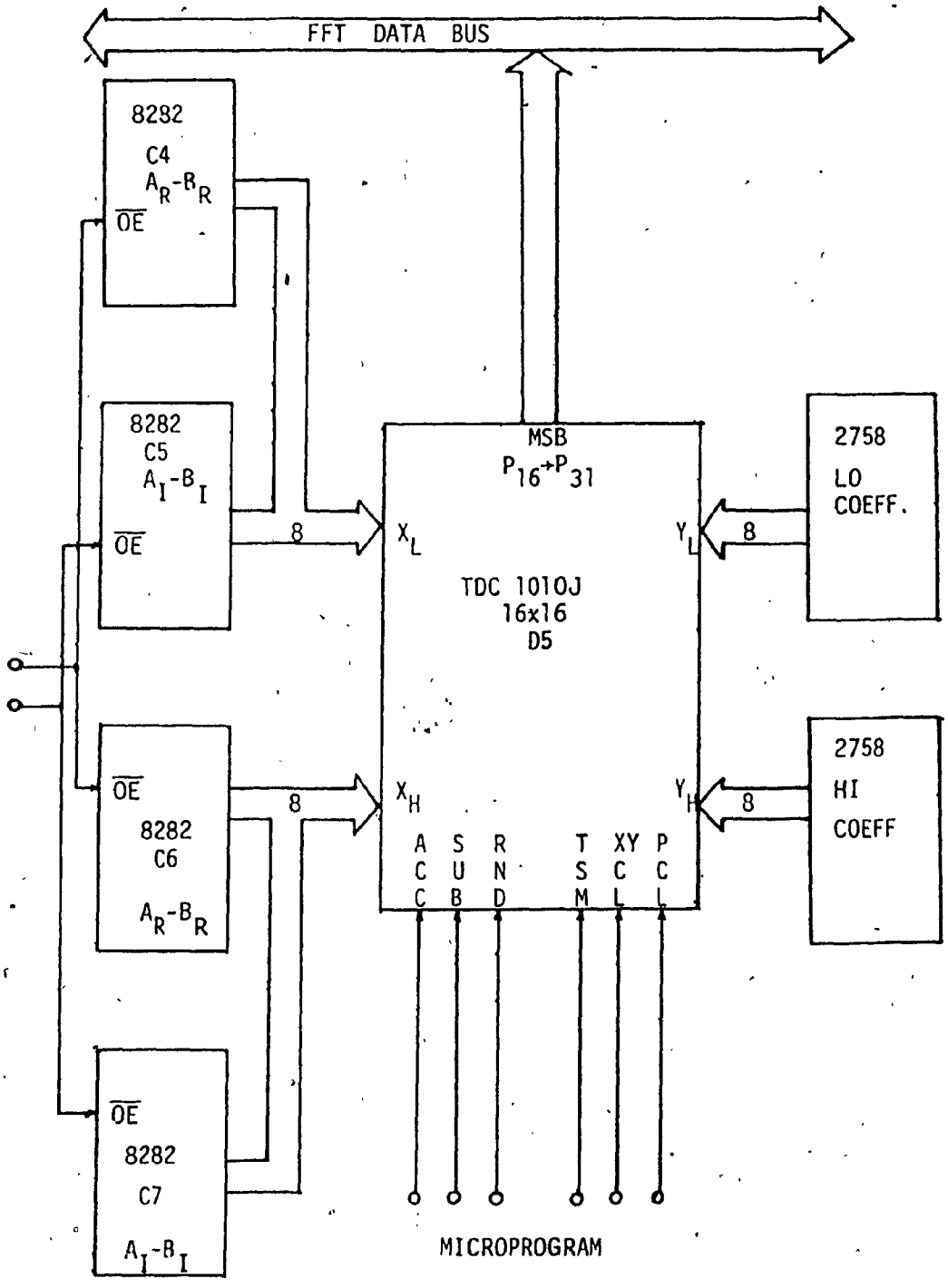


Fig. III.E.16 MULTIPLY-ACCUMULATOR DESIGN

(1) to inform the CPU of the status of the FFT processing, and

(2) to initialise the FFT processing hardware.

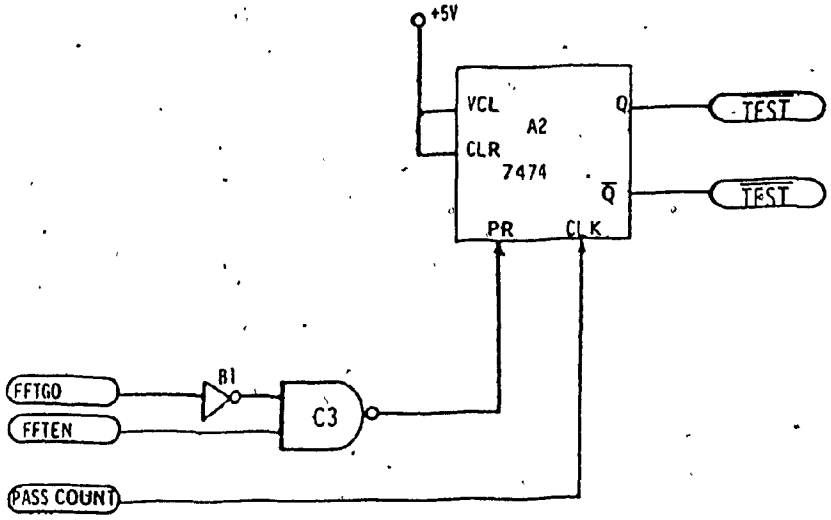


Fig. III.E.17 FFT START/STATUS CONTROL

Essentially the hardware consists of a 7474 positive edge triggered flip-flop with independent clear (CLR) and preset (PR) [III.E.3]. The present line is enabled via C3 and B1 by the CPU. The CPU treats these devices as a port and controls them by writing out data to them. See truth Table III.E.2. The clock (Pin 3) of the flip-flop is active during the FFT mode and is enabled when the FFT pass counter has exceeded nine passes (512 points). This resets the flip-flop, as the input is tied to ground. The Q output goes low and $\overline{TEST}$ = 0. This

signals the CPU that the FFT process is complete and access to its memory is possible.

FFT-GO	FFT-ENABLE	PRESET	$\overline{Q}$ TEST	DESCRIPTION
0	0	1	0	FFT DISABLED
0	1	0	1	FFT ENABLED IN PROGRESS
1	0	1	0	FFT DISABLED
1	1	1	0	FFT DISABLED

Table III.E.2 TRUTH TABLE FFT START-STATUS

g. The Microprogram Generator

The microprogram which controls the flow of data to generate the butterfly is stored in two 2758 eproms. The program code occupies 24 locations, but for the prototype 32 locations were reserved. The speed at which the eproms can be read is limited by their access time; for the 2758 eprom the typical access time is 250 ns. The nearest clock period available and convenient to generate was 4.9 mHz ÷ 4 = 1.225 mHz, or a cycle time of 800 ns.

Referring to Fig. III.3.18, the 4.9 mHz clock is divided by eight using D-flip-flops. The three 7474 D-flip-flops are wired to each produce a divide-by-two operation. The output of A2b is therefore 4.9 mHz ÷ 8 Hz. This results in a pulse width of 800 ns, which is the (LSB) least significant bit for the eprom address. The 4.9 mHz ÷ 8 clock is further divided down by a 7493 4-bit binary

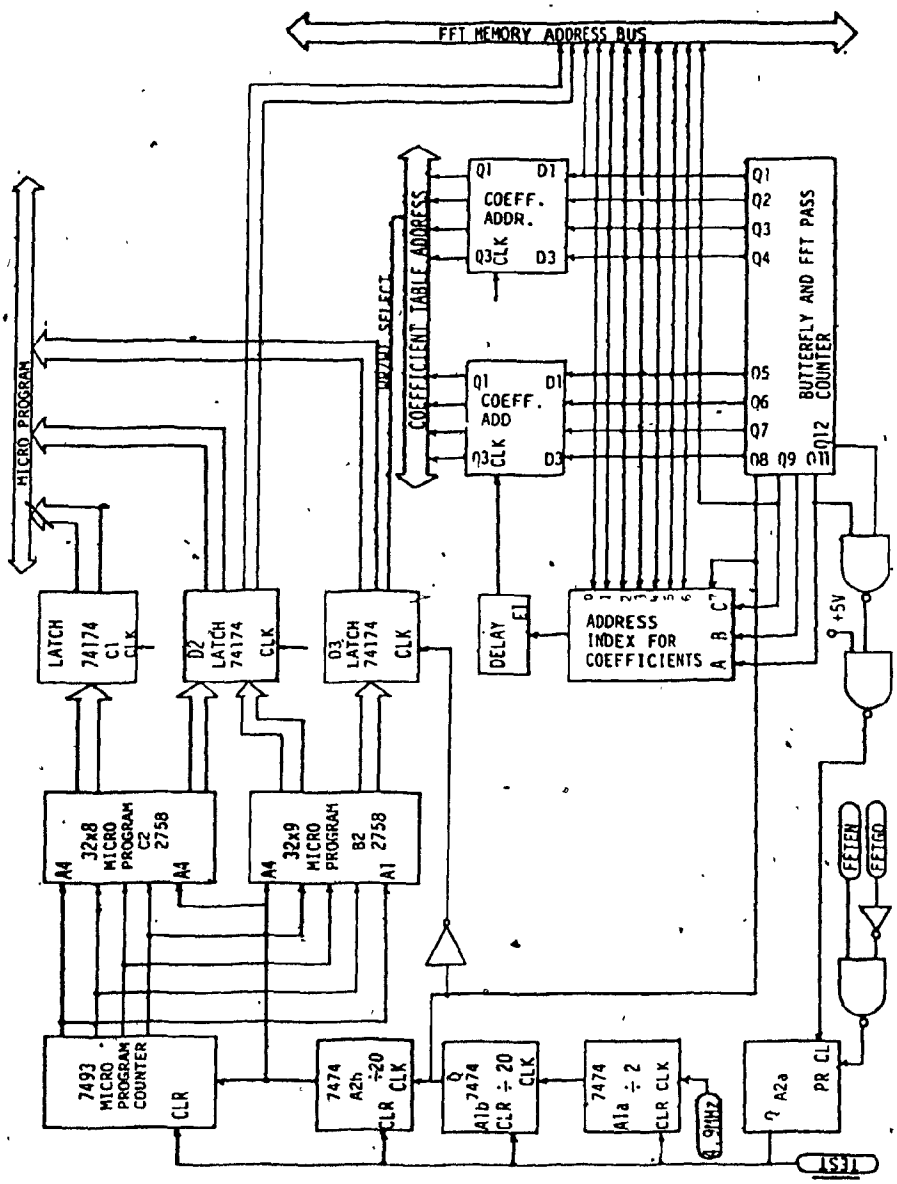


Fig. III.E.18 MICROPROGRAM AND ADDRESS GENERATOR

counter to produce the remaining four bits of address for the microprogram eproms. The microprogram is obtained by simply stepping through the 32 addresses. Data, however, is only stable after 250 ns due to the access time of the eproms [III.B.2]. To avoid this ambiguity the output data is latched into three 74174 latches 400 ns after the change of address. See the timing diagram in Figure III.E.19.

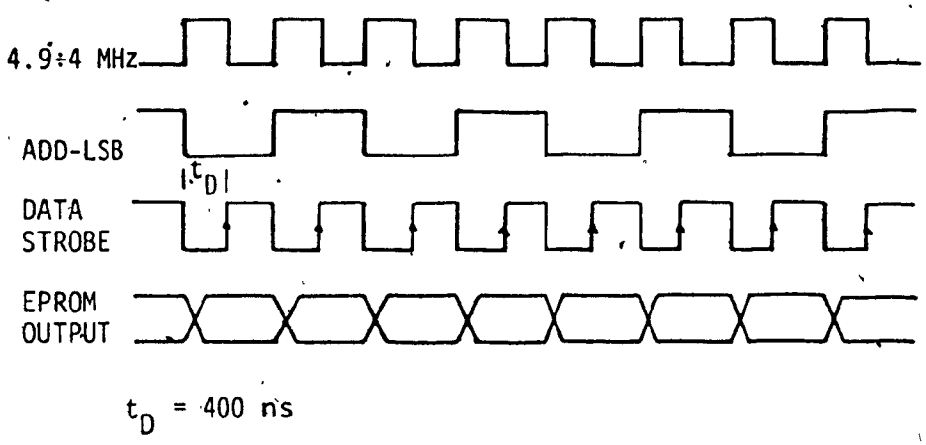


Fig. III.E.19 TIMING FOR MICROPROGRAM DATA

h. FFT Data Storage Buffers

Two 1Kx16 rams are used to store FFT input data and output data, besides providing temporary storage during the FFT processing. Each buffer is comprised of four 1K x 4 rams (2142-3) having an access time of 300 ns [III.B.2]. The buffers are alternately used as input or output buffers depending on the pass within the FFT. Since they both share the common FFT data bus, care must be taken in order to

avoid bus conflicts. Furthermore, they both must be accessible from the CPU. Figure III.E.20 shows these buffers and their associated control circuitry. Address lines are supplied by both the CPU and the FFT address eproms. $\overline{TEST}$ is the control line which determines when the FFT is active; this line is used to enable or disable the address latches from the CPU or the addresses stored in eprom for FFT processing as shown in Table III.E.3.

$\overline{TEST}$	2000 H BUFF	280 0H BUFF
0	CPU	CPU
1	FFT	FFT

Table III.E.3 FFT MEMORY ACCESS SELECTION

The manner in which $\overline{TEST}$ is generated is explained in the section on FFT control. When $\overline{TEST}$ is low, the FFT buffers are available to the CPU. In this mode the CPU loads data into the buffer at address 2000H and reads data from the buffer at address 2800H. For addressing three 8282, 8-bit latches strobe the addresses with the *ALE* pulse provided by the CPU. Since each buffer is 1024 words long, 10 address lines are required. Referring to Figure III.E.20, the chips B1 and B3 provide 8 (eight) lines each for buffer 2000H and 2800H, respectively, and the chip B2 provides the remaining two lines for each. The necessity for keeping the address lines separate arises because the buffers, when used as temporary storage in the FFT processing, require different

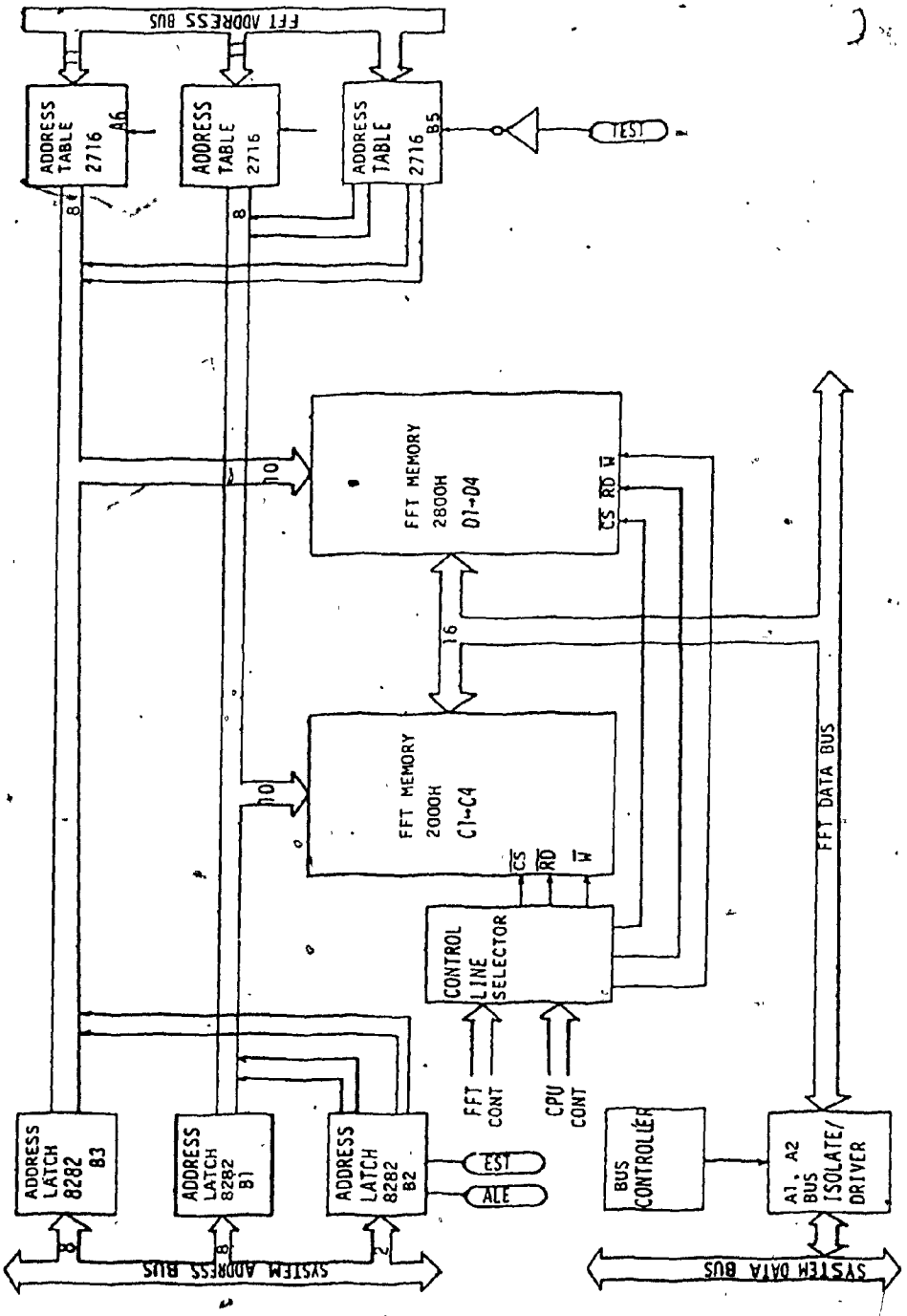


Fig. III.E.20 FFT MEMORY

addressing schemes. The three latches have tri-state buffers which are enabled when $\overline{TEST}$ is low.

In the FFT mode, $\overline{TEST}$ is high and the three latches are disabled. Now, however, the three 2716 eproms are enabled and provide the appropriate addresses for the buffers. Chips A5 and A6 provide eight lines each for the FFT buffers 2000H and 2800H while B5 provides the remaining two lines. Timing requirements for the latches and eproms are shown below in Figure III.E.21 [III.B.2].

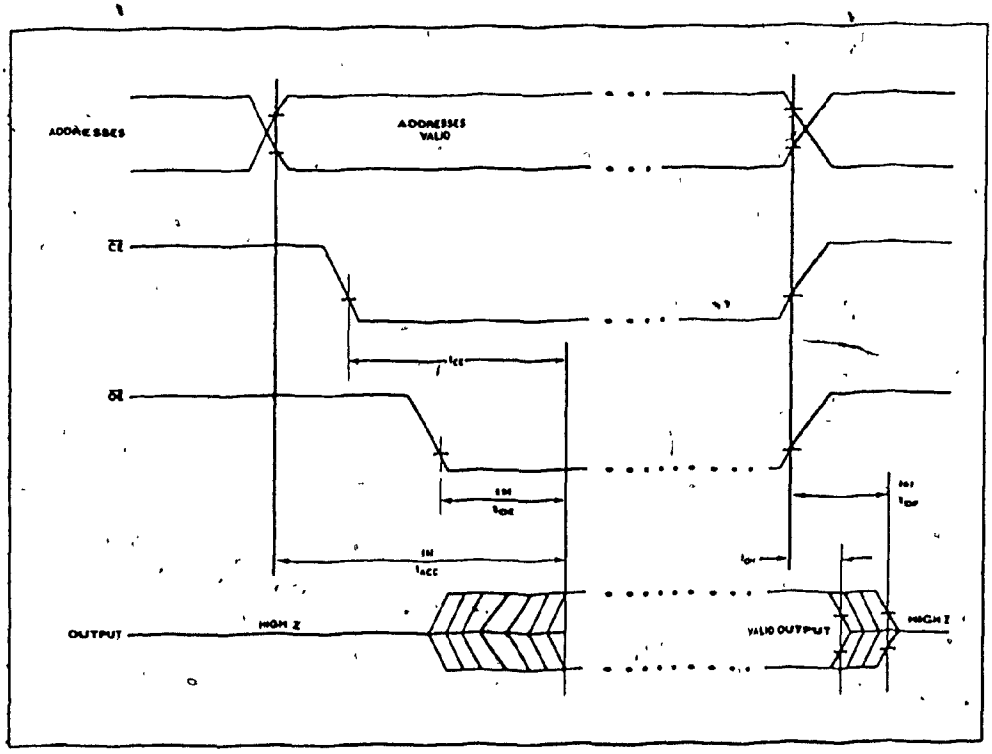


Figure III.E.21a TIMING FOR 2716 EPROMS

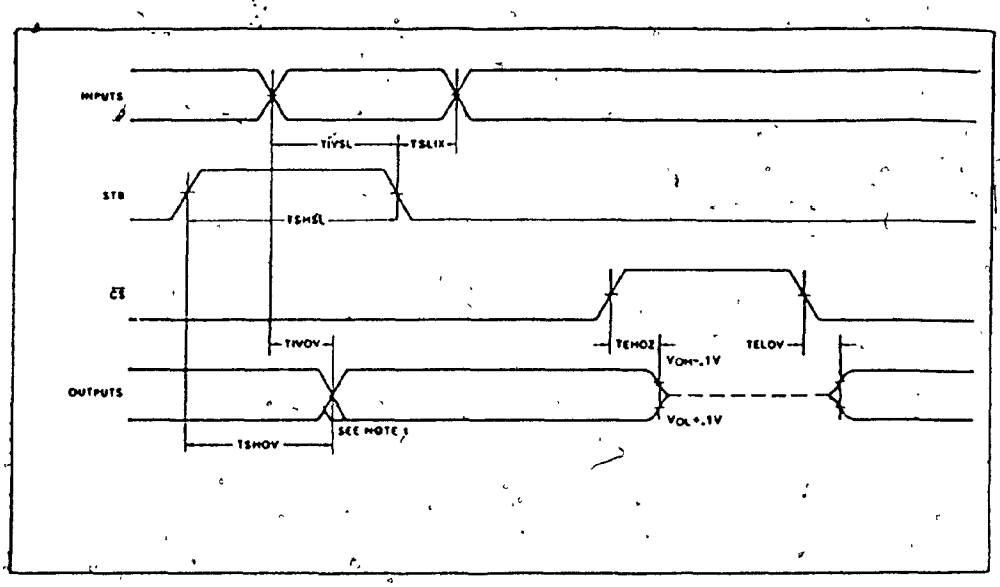


Fig. III.E.21b TIMING FOR 8282 LATCHES

The data bus for both buffers drives the FFT data bus, and communicates with the CPU data bus through two 8286 bus drivers-isolators. The 8286 is a bi-directional 8-bit buffer with both direction and tri-state controls. Direction control is only valid in the CPU mode, and, therefore, the DT/R line of the CPU is used for this purpose. The output buffer control, however, requires a more sophisticated form of gating; Figure III.E.22 shows the bus controller. Here, again, $\overline{TEST}$ is the arbitrator for the bus. When $\overline{TEST}$ is high, both D5A and D5B are inactive, therefore, D5C is active and C7, the or gate, is active high which results in A1 and A2 being disabled (Hi-Z). However, when $\overline{TEST}$ is low (CPU mode) D5A and D5B are active and allow the $\overline{CS}$ (chip select of 2000H or 2800H) to pass through; D5C will be low if either the $\overline{CS}$ of 2000H or 2800H is active low. C7 provides one more level of gating with $\overline{DEN}$ which is the bus enable line from the CPU in order

to avoid timing conflicts on the CPU data bus. Refer to Table III.E.4 for more details.

$\overline{TEST}$	$\overline{CS}$ 2000 H	$\overline{CS}$ 2800 H	DEN	BUS 5E	OPERATION
0	0	0	0		DOES NOT EXIST
0	0	0	1		DOES NOT EXIST
0	0	1	0	0	2000 H
0	0	1	1	1	TRI-STATE
0	1	0	0	0	2800 H
0	1	0	1	1	TRI-STATE
0	1	1	0	1	
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	1	
1	0	1	0	1	
1	0	1	1	1	
1	1	0	0	1	
1	1	0	1	1	
1	1	1	0	1	
1	1	1	1	1	

Table III.E.4 TRUTH TABLE FOR BUS ISOLATOR

The remaining control lines for the buffer are $\overline{RD}$ (read), $\overline{WR}$ (write), and $\overline{CS}$ (chip select). The sources for these lines depend on the status of the FFT processor; here, again, $\overline{TEST}$ determines the

source of the control lines. Referring to Figure III.E.19. Two 74157 quad 2-to-1-line data selector/multiplexers are used. These devices allow selection of one four-bit word from one of the sources. C6 has the $\overline{WR}$ and $\overline{RD}$ lines of the CPU for its 'A' inputs and the $\overline{WR}$ and $\overline{RD}$ of the FFT microprogram for its 'B' inputs. The select line is tied to $\overline{TEST}$. When $\overline{TEST}$ is high, FFT $\overline{WR}$ and $\overline{RD}$ are selected. See Table III.E.5 below.

$\overline{TEST}$	$\overline{WR}$ $\overline{RD}$ $\overline{CS}$
0	C P U
1	F F T

Table III.E.5 MODE SELECTION

Chip C5 is used to select the $\overline{CS}$ lines from the CPU or the FFT processor, in which both buffers are always selected. The buffers in the FFT mode are used alternately as input or output buffers. In order to minimize the number of control lines, some form of routing the appropriate control signals was necessary. Chip C7 and B4 of Fig. III.E.22 provided such a facility. The pass counter of the FFT processor determines the function of the buffers. When the LSB of the pass counter is low, C7B and C7C are disabled and the $\overline{RD}$ line is routed to buffer 2000 H and the $\overline{WR}$ line to buffer 2800 H. When the LSB is high, C7A and C7D are disabled and the $\overline{RD}$ line now enables buffer 2800H and the $\overline{WR}$ line buffer 2000H. See Table III.E.6.

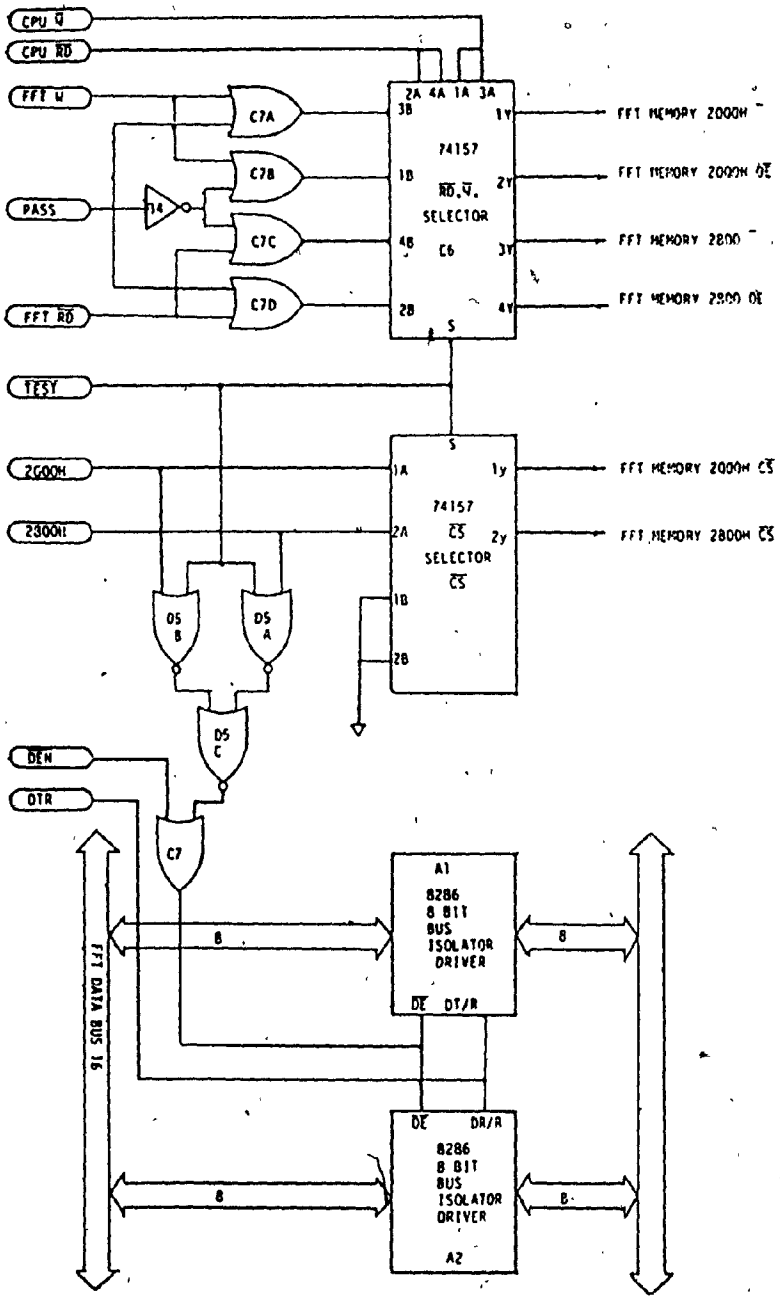


Fig. III.E.22 FFT MEMORY CONTROL

below.

LSB PASS	BUFF 2000 H	BUFF 2800 H
0	READ	WRITE
1	WRITE	READ

Table III.E.6 FFT BUFFERS MODE SELECTION

I. Address Generation

The address indexing scheme required depends on the particular FFT algorithm selected. The decimation in frequency (DIF) algorithm was chosen because multiplications occur after additions. Constant geometry, not in place, normally ordered inputs, and bit-reversed outputs employ the most simple address indexing. Figure III.E.23a shows a 16-point FFT of this type [III.E.2].

According to Fig. III.E.23a, it is obvious that four different modes of indexing are required.

(1) Addressing for input data read (fetch)

(2) Addressing for output data (store)

(3) Addressing for the coefficients

(4) Bit-reverse addressing for FFT output.

The first three modes are required for each pass of the FFT algorithm and the final mode, to read the FFT output data for further processing.

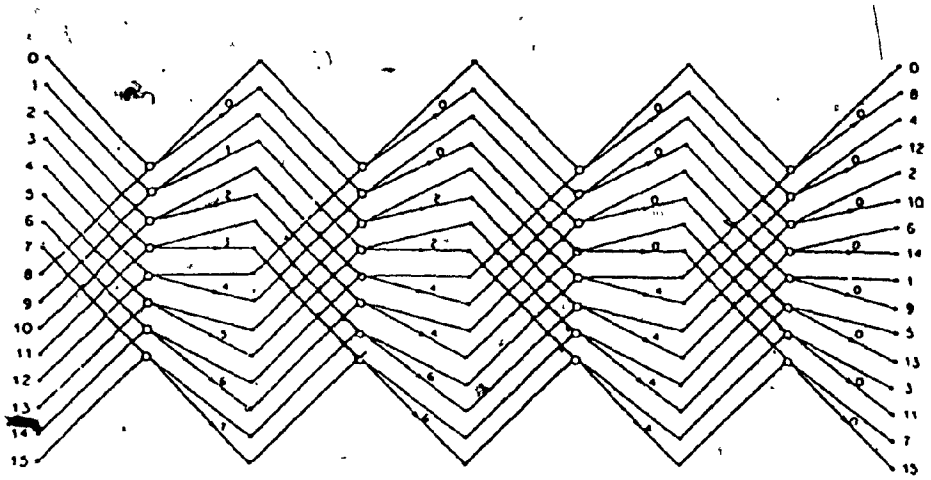


Fig. III.E.23a CONSTANT GEOMETRY ALGORITHM, RADIX 2, 16 POINTS; NOT IN PLACE, ORDERED INPUTS, BIT-REV. OUTPUTS

j. Address Indexing for Input Data Fetch

In the DIF algorithm, the input sequence $\{x(n)\}$ is partitioned into two sequences each of length N/2 samples. The first sequence $\{x_1(n)\}$ consists of the first N/2 points of the $\{x(n)\}$ samples, and the second sequence $\{x_2(n)\}$ consists of the remaining N/2 points of $\{x(n)\}$. For a complex FFT four data points, (the complex quantities), two from each sequence, are used as inputs to the butterfly as shown in Figure III.E.23b.

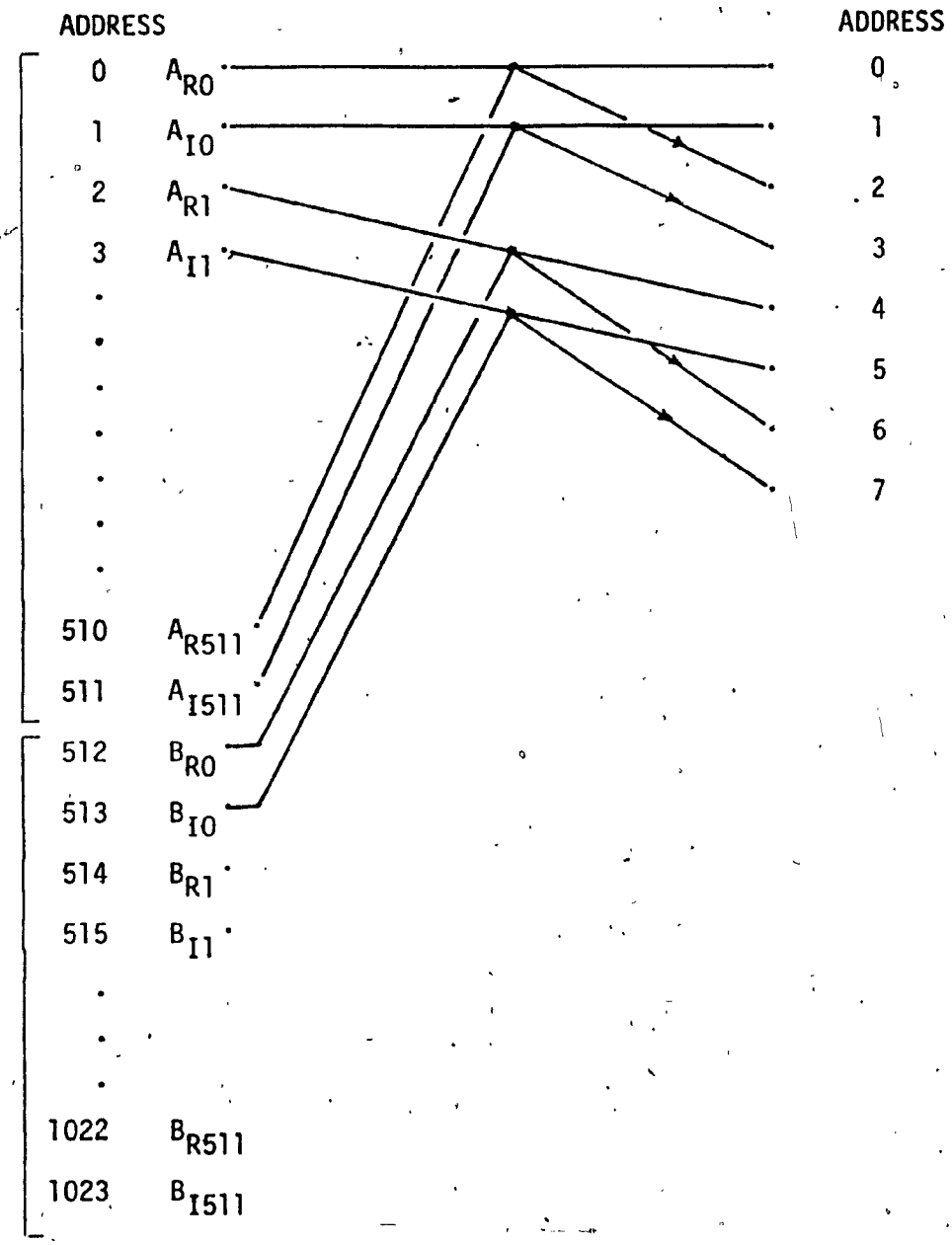


Fig. III.E.23b INPUT READ ADDRESS-OUTPUT WRITE ADDRESS

k. Address Indexing for Output Data Store

For the DIF algorithm, the output on each pass of the FFT is stored at consecutive address locations in the output buffer as shown in Figure III.E.23b.

For a 512-point complex FFT, the buffers must each have a capacity of 1024 registers and as such, require 10 address lines (2^{10}=1024) as shown in Figure III.E.24.

Real data points are stored on even boundary addresses, while imaginary data points on odd boundary addresses for both buffers. Therefore, the LSB A0 of the address lines determines the location of a real or imaginary data point.

On the other hand, A9 determines which half of the memory is selected, therefore, it is used to discriminate between the two input data sequences. The other eight lines A1 through A8 are allowed to increment once every butterfly sequence is complete. Therefore, A0 and A9 are selected by the microprogram of the butterfly, while A1 to A8 are obtained from a ripple counter which is incremented by each butterfly sequence as shown in Fig. III.E.24. However, the FFT processor utilises two 1kx16 buffers, which depending on the pass, of which there are nine (2^9=512), serve as the input or output buffers. Since, as Figure III.E.26 shows, it is necessary to read from the input buffer from two series of data streams separated by N/2 and write into consecutive addresses in the output buffer, it becomes necessary to have two addressing schemes for each pass. Furthermore, since the function of the buffers alternates, the addressing scheme must do likewise. This being the case, the address lines to the buffers have to be

separated. The problem still remains of generating two sets of addresses. Since there already exists a counter for the number of butterflies processed, this count was decoded to provide addresses to two 2kx10 eproms in which the addresses to the buffers are stored as detailed in Figure III.E.24.

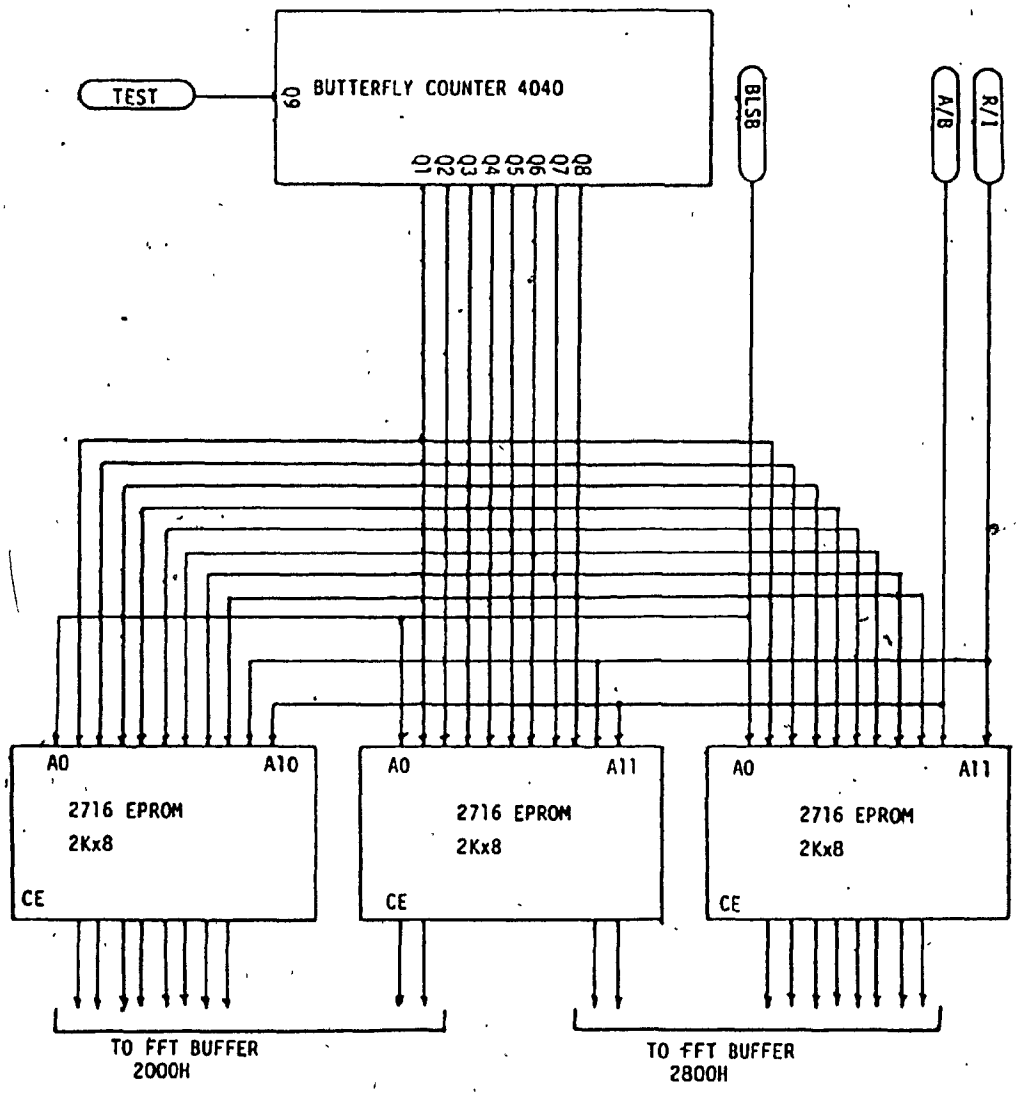


Fig. III.E.24 FFT DATA ADDRESS GENERATOR

The butterfly counter is incremented each time a butterfly has been completed. It is a twelve-bit counter which keeps track of the number of butterflies and the number of passes of the FFT batch. There are 512 points of complex data pairs which supply the input data for 256 butterflies for each pass. The number of passes is 9, since $2^9=512$. Pins Q1 to Q8 of the butterfly counter (CD4040) contain the butterfly count within each pass, and pins Q9 to Q12 sequence from zero (0) to nine for the nine passes. Since pin Q9 toggles between (0) zero and (1) one for each pass, it determines the function of the two FFT buffers (i.e., input or output). See Table III.E.7.

Q12	Q11	Q10	Q9	PASS #	READ BUFF.	WRITE BUFF.
0	0	0	0	ONE	2000 H	2800 H
0	0	0	1	TWO	2800 H	2000 H
0	0	1	0	THREE	2000 H	2800 H
0	0	1	1	FOUR	2800 H	2000 H
0	1	0	0	FIVE	2000 H	2800 H
0	1	0	1	SIX	2800 H	2000 H
0	1	1	0	SEVEN	2000 H	2800 H
0	1	1	1	EIGHT	2800 H	2000 H
1	0	0	0	NINE	2000 H	2800 H

Table III.E.7 TRUTH TABLE FOR BUFFER MODE

ℓ. FFT Buffer Address Generating Eproms

The address generating eproms have a capacity to store 2048 addresses. Since each 2716-1 eprom has 2048x8-bit capacity, and since the FFT buffers are 1024x16 words, 10 address lines are necessary. Three 2716-1 eproms are used. Two of the eproms supply eight address lines to each buffer while the third 2716-1 supplies the remaining two address lines.

Address data in the eproms is separated into two 1024x10 bit blocks, each block being used for reading (input data) or writing (output data), depending on the pass in the FFT processing the (LSB) least significant bit of the pass count is used to select the appropriate half. As an example, on the first pass data is read from FFT buffer 2000 H from two sequences of data separated by N/2 (or 256 complex) samples. Therefore, the addresses must be generated in the following sequence: 0, 1, 512, 513 ...2, 3, 514, 515 ... 510, 511, 1022, 1023.

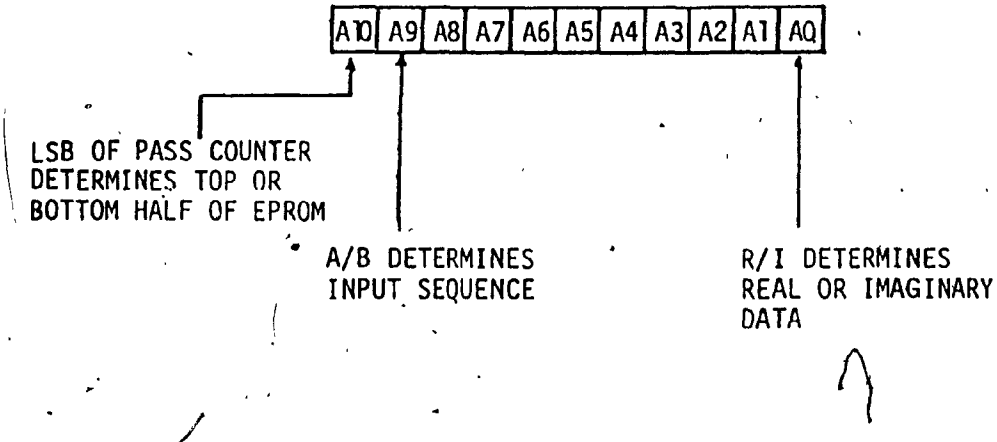


Fig. III.E.25 ADDRESS LINES FOR FFT MEMORY

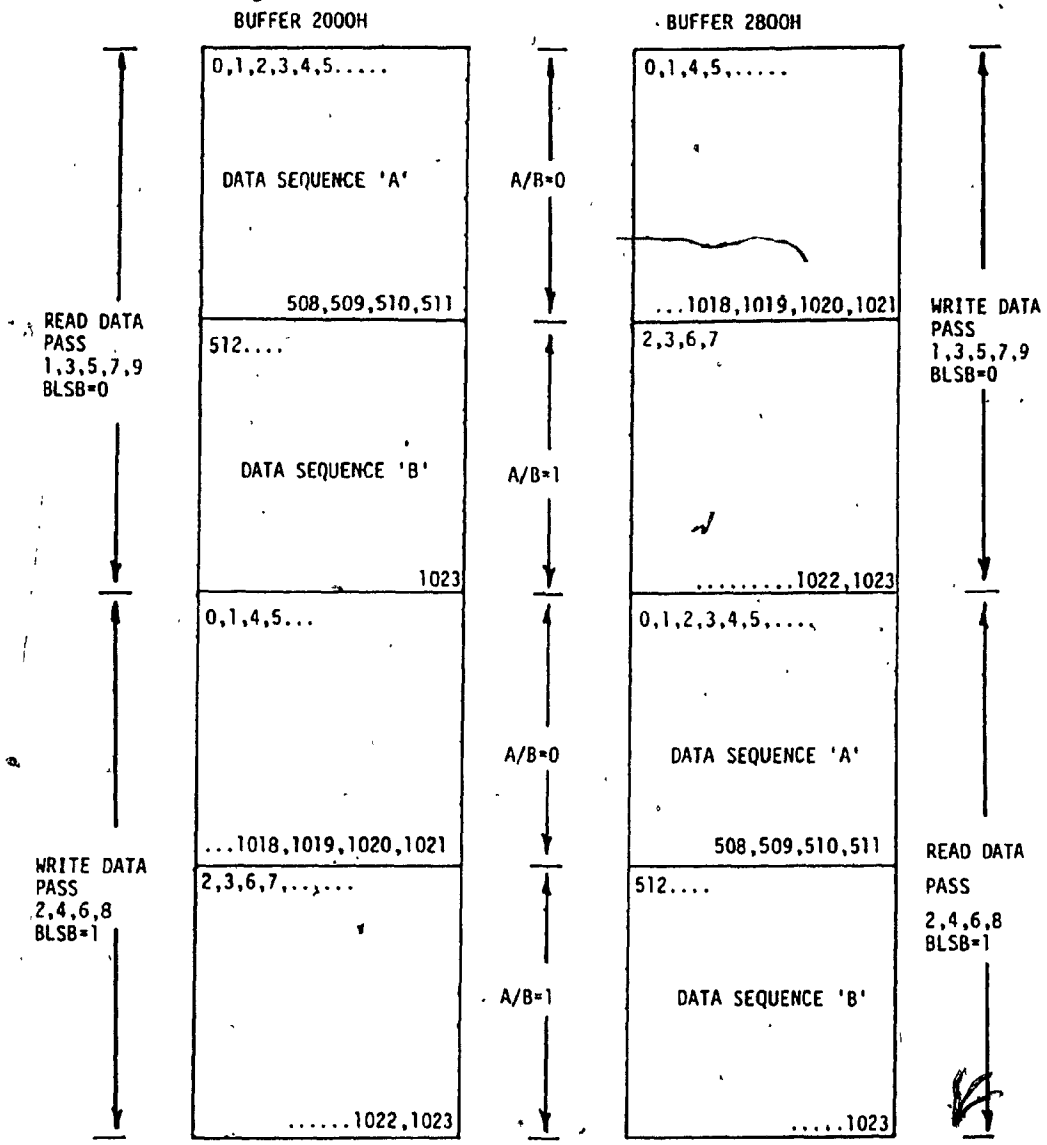


Fig. III.E.26 CONTENTS OF ADDRESS GENERATING EPROMS

Data is then written into buffer 2800H into consecutive address locations. Therefore, addresses must be generated in the following order: 0, 1, 2, 3, 4, ... 1023. In order to use the same address generating scheme the addresses in the eprom must be stored as shown in Figure III.E.26. During pass two data is read from buffer 2800H and written into buffer 2000H, for the even passes, addresses are generated from the bottom half of the eprom as shown in Figure III.E.26.

m. FFT Coefficient Addressing

A 512-point complex FFT process requires 256 complex coefficients for its implementation. The 256 complex coefficients are stored in 2758 eproms and supplied to the multiplier when required. However, all the 256 coefficients are required for the first pass only. For subsequent passes, of which there are eight, 256/2p, where 'P' is the pass number, coefficients are required. A description of the hardware required for the generation of coefficients follows.

The 12-bit ripple counter CD 4040 generates all the 256 addresses required for the coefficient tables. Since a new set of coefficients must be presented to the multiplier for each butterfly, the clock for the ripple counter is obtained from the butterfly microprogram counter. Therefore, the clock rate or the address change rate of the coefficients is (.8μs×32 steps) = 25.6μs. The state of the counter advances one count on the negative transition of each input pulse [III.D.5]. Pins Q1 to Q8 of the counter are used as address lines to the coefficient tables, whereas, pins Q9 to Q12 are used to count the number of passes in the FFT. The counter can be reset from two

sources: (1) the 8086 CPU under program or (2) self-reset when the nine passes have been completed. In the self-reset mode, the two pass counter lines Q12 and Q9 are *anded*. When both are high, the nine passes of the FFT are complete and the output of C3, the and gate, goes high. The result is an active high clock pulse on the D-type flip-flop (7474, A2) which transfers the data on the D-input to the Q output. Since the D-input is tied low, the $\overline{Q}$ output goes high and thus resets the ripple counter. Refer to timing diagram III.E.27.

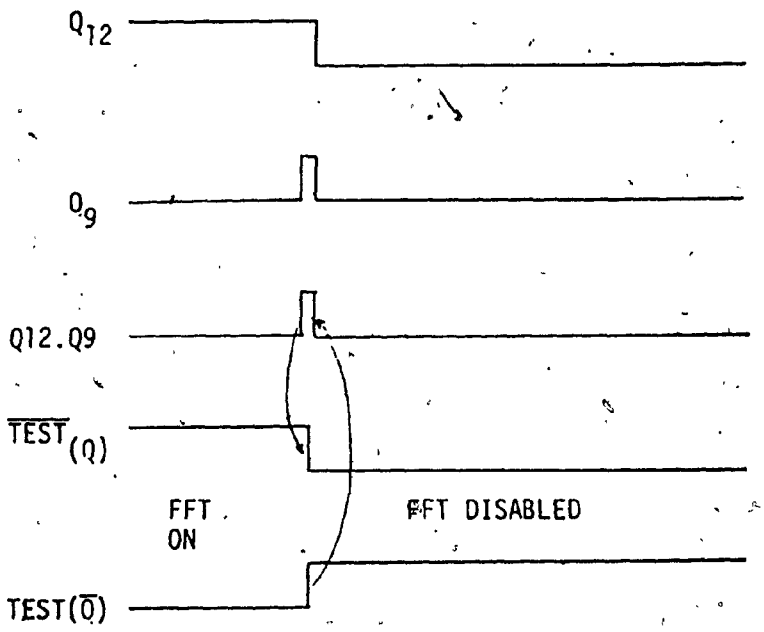


Fig. III.E.27 SELF-RESET TIMING

Pins Q1 to Q7 not only are the addresses for the coefficient look-up tables but are also the clock for the latches (two 74175; chips E4, E5) which hold the addresses. Clocking for these address latches is through an eight-to-one multiplexer CD 4051(E2). The CD4051 is a single 8-channel multiplexer having three binary control

inputs which are supplied by pins Q9, Q10, and Q11 of the pass-counter. These three lines select one of the eight input lines which are the butterfly count Q1 to Q7 and the clock. Therefore, when pins Q9, Q10, and Q11 are all low, the clock is selected by the multiplexer and, thus, every address Q1 to Q8 is latched by the 74175 address latches. On the other hand, if Q9 is high and Q10, Q11 are low, Q1 is selected by the multiplexer and, therefore, every other address is latched and the previous address is held when no latching occurs. Thus, the addresses for the look up table will be 0, 0, 2, 2, 4, 4, ... 254, 254. Refer to Table III.E.8 and Figure III.E.28 for more details.

PASS Q12	Q11	Q10	Q9	LATCH CLOCK	ADDRESSES
0	0	0	0	CLK	0,1,2,3,4,.....
0	0	0	1	Q1	0,2,4,6,.....
0	0	1	0	Q2	0,4,8,12,.....
0	0	1	1	Q3	0,8,16,24,.....
0	1	0	0	Q4	0,16,32,48,.....
0	1	0	1	Q5	0,32,64,.....
0	1	1	0	Q6	0,64,128,.....
0	1	1	1	Q7	0,128
1	0	0	0	RESET	

Table III.E.8 RELATIONSHIP BETWEEN FFT PASS NUMBER AND COEFFICIENT ADDRESS

The 74174 address latches require an input data setup time of 20 ns; therefore, the clock signal for them must be delayed since they are generated from the same counter. A 74121 monostable is used for this purpose. The monostable is triggered from the output of the multiplexer on the falling edge of the pulse, $\overline{Q}$ goes low when it is triggered and stays low for a period determined by a resistor and capacitor combination. In this case, R=10k, C=330pf; therefore, the delay is 1.5 μs. Refer to Figure III.E.30. [III.D.6].

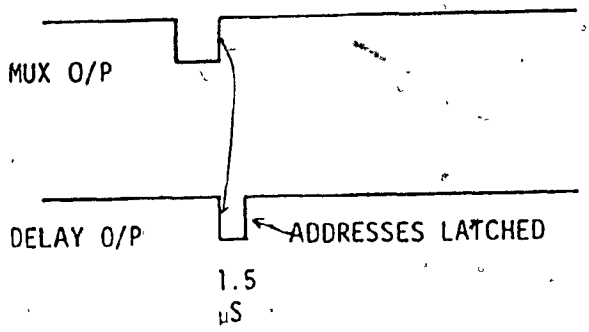


Fig. III.E.30 DELAY TO LATCH ADDRESS

The multiplexer (CD4051) provides proper address indexing for 8 passes of the FFT, but for a 512-point FFT nine passes (2^9=512) are required. Referring to Table III.E.8, it can be seen that on the final pass the only coefficient that is used is the initial one or the contents of address zero in the look up table. Pin 1 (or Q12) of the pass counter, which goes high on the ninth pass, is used to clear the 74175 address latches. This results in the latches being cleared throughout the ninth pass, and the first address of the coefficient table being supplied to the multiplier.

The addresses for the coefficient tables are eight-bit wide, which allows 256 coefficients to be accessed. A 512 point complex FFT requires 256 complex coefficients. Therefore the coefficient tables must hold 512 points of data.

Two 2758 eproms having an access time (refer to Figure III.E.28) of 250 ns are used to provide 16-bit wide coefficients. The coefficient data is stored in two 256 blocks in the eproms. The top 256 locations contain the real parts (ω_R) and the next 256 locations contain the imaginary parts (ω_I). Address line A8 on the eproms determine which block is being used, since this is dependent on how the butterfly is produced. The A8 address line is determined by the microprogram of the FFT butterfly.

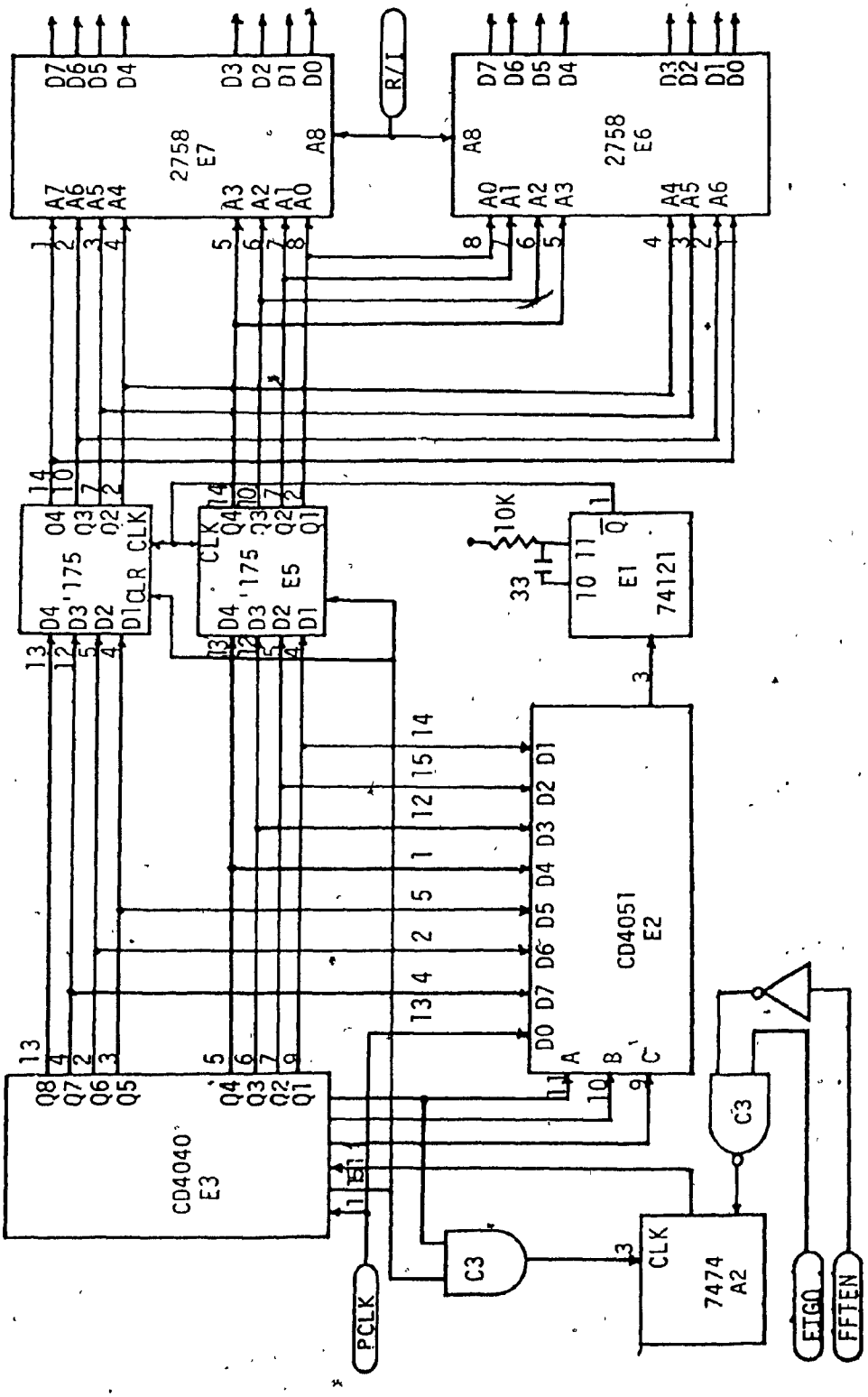


FIG. III.E.28 COEFFICIENT ADDRESS GENERATOR

III.F. THE INTERROGATION UNIT

The interrogation of the Bottom unit consists in transmitting five tones for a duration of 250 ms. The frequencies of the five tones are 8992 Hz, 8592 Hz, 8192 Hz, 7792 Hz, and 7392 Hz. The tones are all 400 Hz apart and situated in each diversity band. To generate these tones, a combination of digital frequency synthesis and analog frequency multiplication is used. Two tones, at 400 Hz and 800 Hz, produced by the ROM look-up table method are multiplied with a 8192 Hz carrier to produce the five tones. The technique is the same as AM, therefore the output spectrum contains the carrier at 8192 Hz and two upper and two lower sidebands as shown in Figure III.F.1.

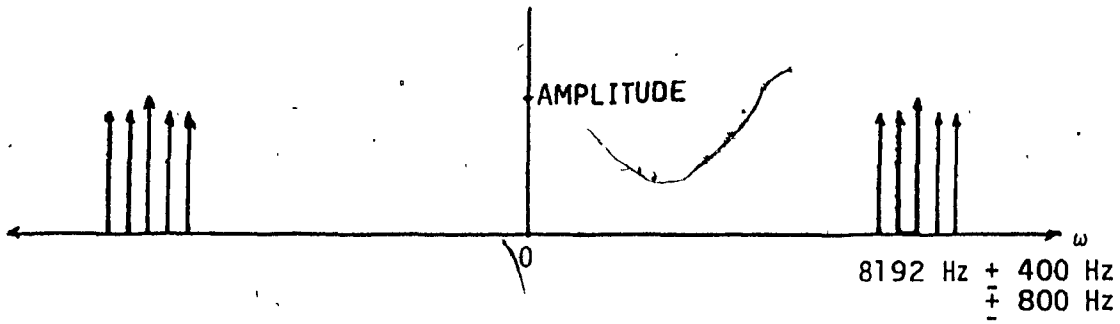


Fig. III.F.1. OUTPUT SPECTRUM OF INTERROGATION COMMAND

III.F.2 FIVE TONE GENERATOR

To generate the 400 Hz and 800 Hz tones, samples of the two frequencies are stored in a 2758 eprom. The sample values were pre-computed and summed, with 256 samples stored in the eprom. The 256 samples contained in the eprom are for two periods of 800 Hz and one period of 400 Hz, therefore no discontinuities are present. The 256 locations of the look-up table were read at a rate of 102.4 kHz (400x256). The 102.4 kHz clock is obtained by dividing the 2.4576 mHz peripheral clock (PCLK) by 24. A 7473 J.K. flip-flop in the toggle mode divides the PCLK by two followed by a 7492 divide-by-twelve counter [III.D.6]. A 12-bit CMOS rippler counter divides the 102.4 kHz clock by 256 to generate the 8 address lines for the look-up table. The samples are stored in the lowest 256 bytes of the 2758 eprom. A 1408 D/A convertor similar to the one described in Section III.D.5 is used to convert the samples to analog voltages. The divider circuit chips are operable upto 30 mHz and the access time of the eprom is 450 ms, well above the demands made for this application. The complete circuit is shown in Figure III.F.2.

As shown in Figure III.F.3, the two tones are mixed with a 8192 Hz carrier. In order to produce a tone burst of 250 ms, the carrier pulse is gated through an AND gate. The gating period of 250 ms is produced by triggering a monostable with a delay of 250 ms. The 74121 monostable, once triggered, produces an output pulse whose width is controlled by R and C. The values for R and C were chosen from the manufacturer's tables to produce a 250 ms delay [III.D.6]. The output of the AND gate is lowpass filtered by an RC passive filter to attenuate the higher harmonics of the 8192 Hz carrier. The output of the filter

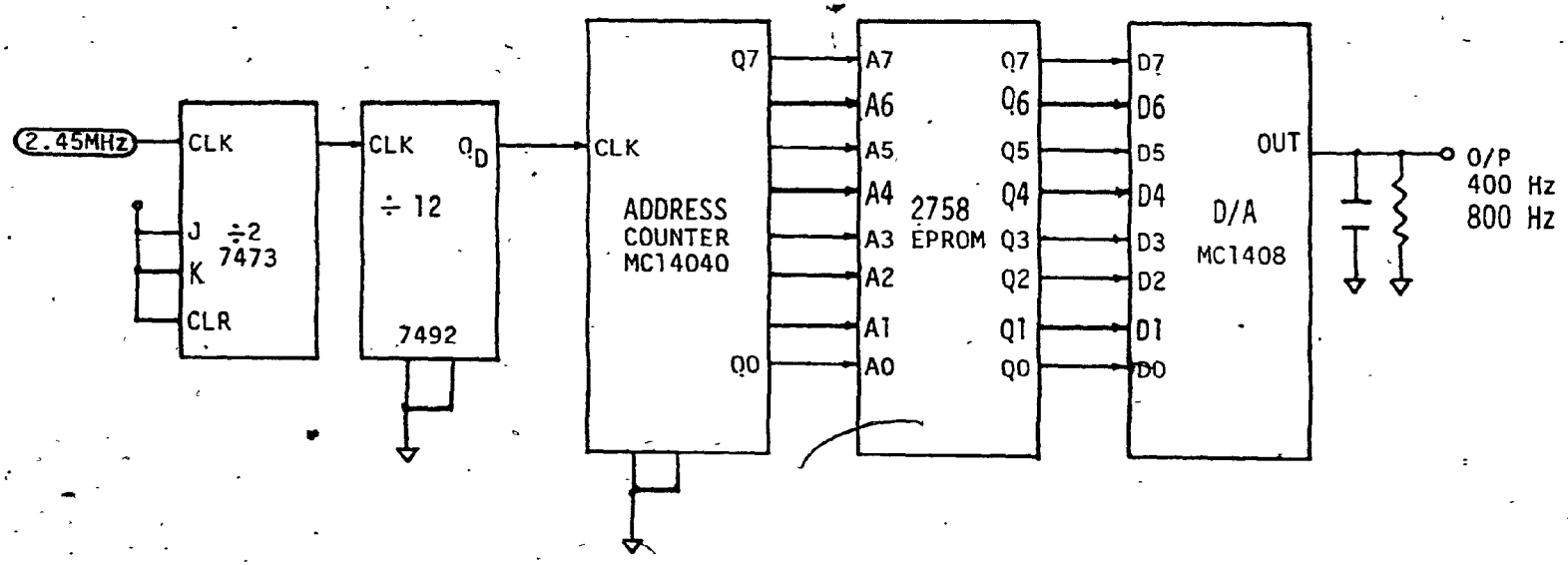


Fig. III.F.2 TWO TONE DIGITAL FREQUENCY SYNTHESIS

is adjusted to give a carrier level of 60 mV as shown in Figure III.F.4.

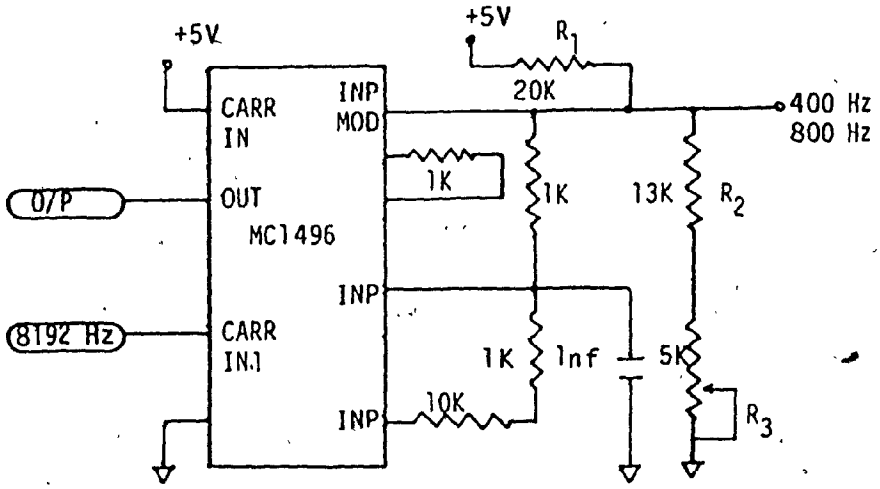


Fig. III.F.3 AM MODULATOR

The modulator circuit shown in Figure III.F.3 is similar to the other mixers used in the preprocessor and time synchronizer. There is one difference, however, and that is the addition of a dc potential to the modulating input. Resistors R1, R2, and R3 offset the modulating 400 Hz and 800 Hz tones with a dc potential. The effect of this is a multiplication of the carrier by a constant, as opposed to a nulling of the carrier as in the previous sections.

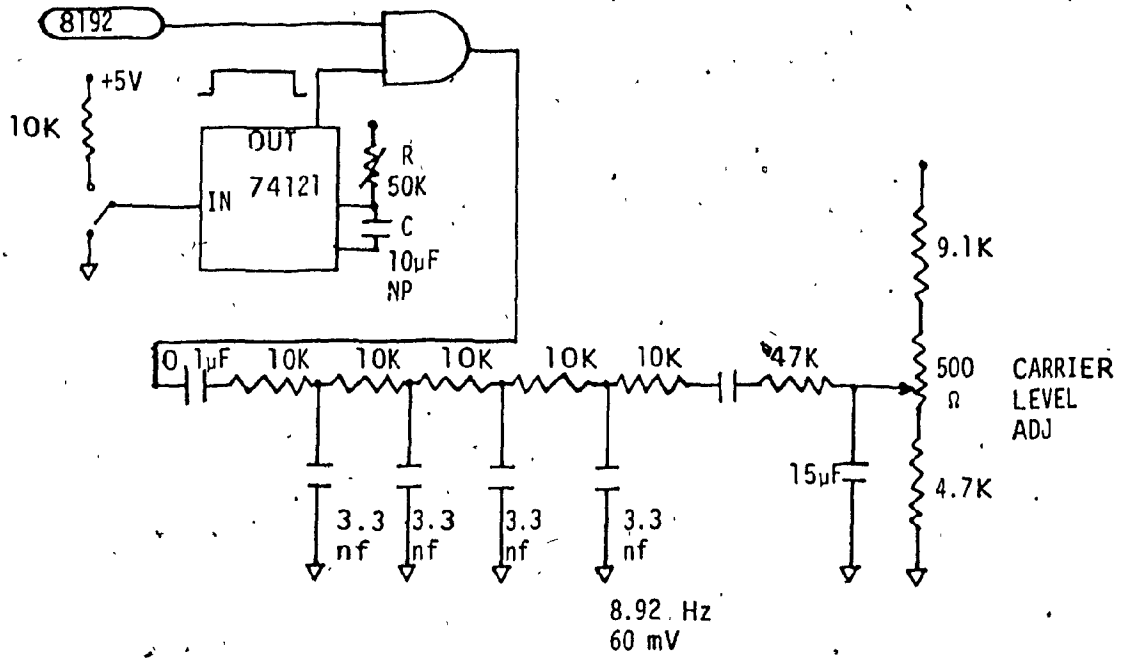


Fig. III.F.4 8192 Hz CARRIER BURST GENERATION

The output of the mixer is amplified by A1 as shown in Figure III.F.5. Amplifier A1 is a variable gain amplifier which controls the transmitted output power. A 4th-order bandpass filter centered around 8192 Hz with a Q=4 band limits the tones before power amplification. Design equations for the filter are given in Appendix VI.B.1.

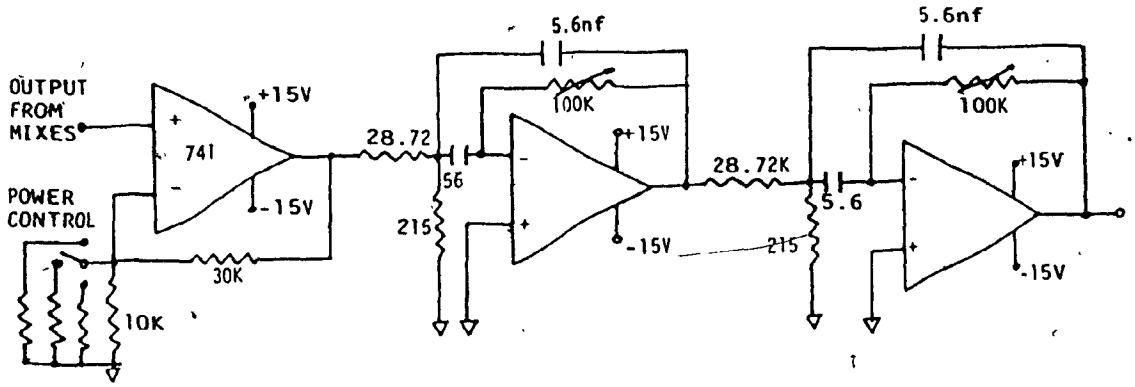


Fig. III.F.5 4th-ORDER BANDPASS FILTER WITH INPUT AMPLIFIERS

III.F.3 THE POWER AMPLIFIER

The LM 383A is a cost-effective high power amplifier able to continuously deliver upto 3.5 amperes of current. With a single chip, 5.5 watts of power into a 4Ω load is easily obtained. In Chapter II, it was estimated that the Deck Unit requires at least 6 watts of power to interrogate the Bottom unit at a distance of 1 km. But the power amplifier when configured as a bridge amplifier as shown in Figure III.F.6., is capable of supplying 16 watts of power. The output stage of the amplifier is a class B type amplifier. In the non-inverting configuration used in Figure III.F.6. the gain is determined by R_1 and R_2 (gain = $1 + R_1/R_2$), which in this application is gain of 101. The power output maybe estimated by assuming each amplifier is driving a load of $R_L/2$, which in this case is 2 Ohms. Therefore, with a 15-volt supply each amplifier can deliver 8 watts, at 10% total harmonic

distortion (THD), for a total of 16 watts. A 100 K ohm potentiometer is used to trim out the differences in individual LM 383A dc output levels since, with a direct connected load, substantial dc power consumption can result if the quiescent output levels are not matched [III.C.2].

Transformer T2, the output transformer, has a turns ratio of 1:20. The primary impedance is 4 ohm, whereas the secondary impedance is 1600 ohms at 8192 Hz. The transducer is a capacitive load and inductance L is added to compensate for load impedance changes due to frequency. Both the transformer and inductor were custom made to insure optimum transfer of power.

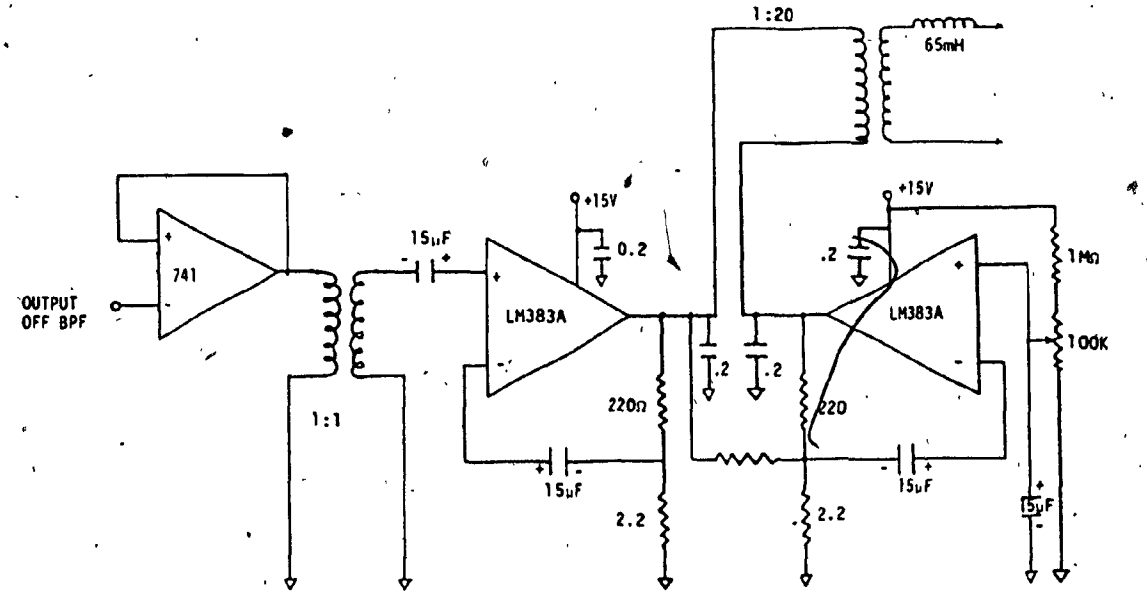


Fig. III.F.6 POWER AMP

III.G.1 SERIAL INPUT-OUTPUT INTERFACE

Once the transmission from the Bottom unit is complete the tidal data received by the Deck unit must be permanently stored for analysis. An interface was designed to communicate with a printer or terminal. The serial interface is based on an Intel 8251A Universal Synchronous/ Asynchronous Receiver/Transmitter (USART) which is operated in the asynchronous mode. A baud rate generator provides rates from 300 to 2400 for use by the USART.

The USART occupies two I/O ports within the on-board I/O address space and since the USART is interfaced to the lower byte of the data bus (DO-D7), both ports have even-numbered port addresses (10H and 12H). The individual USART port functions are determined by the A1 address bit and the $\overline{RD}$ and $\overline{WR}$ signals of the CPU as noted in Table III.G.1.

The 8251A interfaces with the system data bus through an 8-bit, 3-state buffer as shown in Figure III.G.1. Data is transmitted or received by the buffer upon execution of Input or Output instructions of the CPU. Control words, Command words, and Status information are all transferred through the Data Bus Buffer.

The software routine for the serial interface configures the USART by writing an 8-bit command word to the control port of the 8251A. A command word of OCFH configures the USART for 8-bit character length, no parity, two stop bits and a baud rate factor of 64x. As illustrated in Figure III.G.2. the baud rate generator (a 7493 4-bit counter) uses the 307.2 KHz (PCLK/8) signal to provide four baud rate frequencies. Since the USART is operated in the 64xmode, these frequencies are 64 times the corresponding baud rate. Two D-type

flip-flops (7474) divide the 1.2288 MHz, (PCLK/2) by four to generate the 307.2 KHz signal. 75188 and 74189 (E5, E6) are two RS232 transmit receive buffers.

USART Input			Port Addresses	Port Function
A1	$\overline{RD}$	$\overline{WR}$		
0	0	1	10H	Read USART Data
0	1	0	10H	Write USART Data
1	0	1	12H	Read USART Status
1	1	0	12H	Write USART Control

Table III.G.1 USART I/O PORT

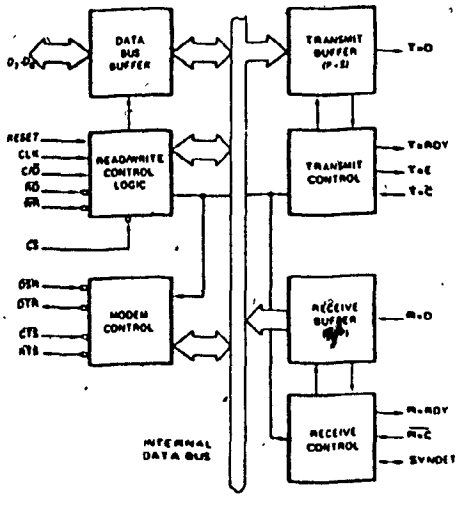


Fig. III.G.1 BLOCK DIAGRAM OF USART

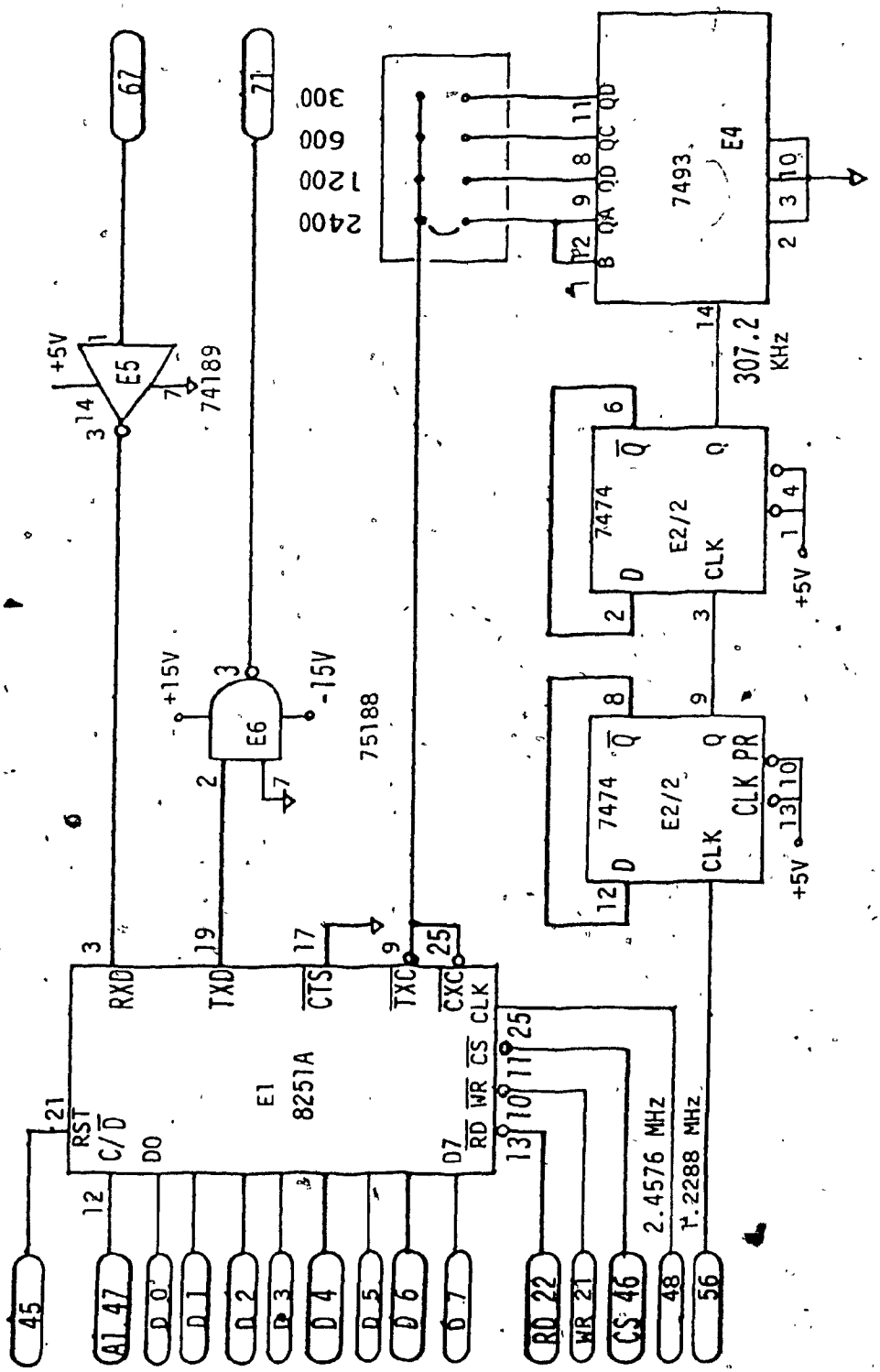


Fig. III.G.2 SERIAL I/O INTERFACE

CHAPTER III

REFERENCES

III.A.1 Williams, A.B., Electronic Filter Design Handbook, McGraw Hill, New York, 1981.

III.B.1 iAPX User's Manual, Intel Corp., August 1981.

III.B.2 Component Data Catalog, Intel Corp., January 1982.

III.C.1 Linear Integrated Circuits, Motorola Inc., 1979.

III.C.2 Linear Data Book, National Semiconductor Corp., 1982.

III.C.3 Engelson,M and Fred Telewski, Spectrum Analyzer Theory and Applications, Artech House, Massachusetts.

III.C.4 Universal Active Filter Application Note, Burr Brown Research Corp., 1976.

III.C.5 Data-Acquisition Data Book, Vol. 1, Analog Devices, 1982.

III.D.1 Jaub and Schilling, Principles of Communication Systems, McGraw Hill, 1971.

III.D.2 The Application of Filters to Analog and Digital Signal Processing, Rockland Systems Corp., 1976.

III.D.3 Analog to Digital Conversion Notes, ed Daniel H. Shringold, Analog Devices Inc., Massachusetts, 1972.

III.D.4 Tobey, Graeme and Huelsman, Operational Amplifier Design and Applications, McGraw Hill, 1971.

II.D.5 Cos/Mos Integrated Circuits, RCA Corp., 1977.

III.D.6 The TTL Data Book for Design Engineers, Texas Instruments Inc., 2nd Edition, 1976.

III.D.7 Tedeschi,F., The Active Filter Handbook, Tab Books, P.A., 1979.

III.D.8 Jung, Walter G., I.C. Op-Amp Cookbook, Howard W. Sams and Co. Inc., 1974.

III.D.9 Morgera, S.D., The Effect of Phase Errors on Demodulation; Unpublished Memorandum, Concordia University, Montreal, 1982.

III.E.1 The Fundamentals of Signal Analysis, Application Note 243, Hewlett Packard Corp., November 1981.

III.E.2 Rabiner., Lawrence R. and Bernard Gold, Theory and Application of Digital Signal Processing, Prentice Hall Inc., New Jersey, 1975, pp. 356-371.

III.E.3 LSI Data Notes, TRW Inc., 1979.

III.E.4 Schirm, L., Multiplier-Accumulator Application Notes, TRW LSI Products, January 1980.

CHAPTER IV

SOFTWARE DEVELOPMENT

IV.A. INTRODUCTION

The software employed in the Deck unit was developed on the Intellec Series II Micro computer Development System. The Intellec System is a multiple-microprocessor system that runs ISIS-II, a disk-based operating system. It supports ASM-86, the assembly language for 8086 CPU, used in the Deck unit. To debug the system ICE-86, the in-circuit emulator for the 8086 microprocessor was extensively used. It consists of a 40-pin probe which emulates the 8086 CPU in the system under test. ASM-86 was used because it provides access to all the processor facilities and because assembly language programs can be written to execute faster and use less memory than programs written in higher level languages [IV.A.1.].

The machine code for the program is stored in two 2716 (4Kx8) Eproms. The address of the program is from F000H to FFFFH, as described in Chapter III. The four interrupt routines are located at the top of the memory followed by the initialisation routine, the main program and the output routine. Tables containing data for doppler correction or the error correcting generator matrix are stored at the bottom of the memory above the system reset routine. Figure IV.A.1 describes the location of code in the memory. In Figure IV.B.1 the flow chart for the complete program is presented followed by a description of the different algorithms. Software for the interrupt controller and the universal synchronous/Asynchronous Receiver/Transmitter is not included as they are not unique to the system.

PROGRAM CODE STORAGE

ADDRESS	FUNCTION
F000H → F2B7H	Interrupt Routines Sample, Time, Begin, Dump.
F2B8H → F360H	Initialization Routine
F361H → F36BH	Long Term Noise Estimation
F3CCH → F3D5H	Interrogation
F3D6H → F3F0H	Diff: Routine
F3F1H → F5D3H	FFT, Doppler demodulation
F5D4H → F753H	Error correction
F754H → F8BFH	Dump Routine
F8C0H → FA36H	Parameter Change Routine
FA37H → FB38H	Not Used
FB38H → FFEEH	Look up Tables, Doppler, Circulant Matrix
FFF0H → FFF4	System Reset

Fig. IV.A.1 PROGRAM CODE STORAGE LOCATION

IV.B.1 SYSTEM OPERATION

In this section the operation of the system is described. The Bottom unit is moored to the ocean floor, where it collects tidal information at intervals that are predetermined by the user. In addition to this function, the Bottom unit is always listening for the interrogation command from the Deck unit. Upon arrival of the ship to the area where the Bottom unit is deployed, the Deck unit is initialised. Initialisation consists in setting system parameters such as gain, differentiator transition threshold, and differentiator amplitude threshold. Since the initial gain of the Deck unit is selected by estimating the noise in the vicinity, the interrogation command transmitter power can be set accordingly. For noisy regions the maximum transmission power of 6 watts may be required. The three system parameters set in the initialisation process may be changed by the operator through the RS232 port, as indicated in Figure IV.B.1.

The Deck unit is now ready to receive data from the Bottom unit. The operator sends the interrogation command via the control on the front panel. The interrogation command consists of a 250 ms burst of five tones. The Deck unit is now in the receive mode. If the interrogation command was of sufficient strength to meet the threshold in the Bottom unit, transmission of tidal data commences. Sixteen preambles used to acquire synchronisation, evaluate signal strength, and estimate doppler shift are transmitted before tidal data is transmitted.

The Deck unit is now in the preamble mode. The first four preambles are used exclusively for gain adjustment. The peak detector algorithm described in Section IV.G.2. finds the maximum signal level and the gain control algorithm optimises the signal level in the

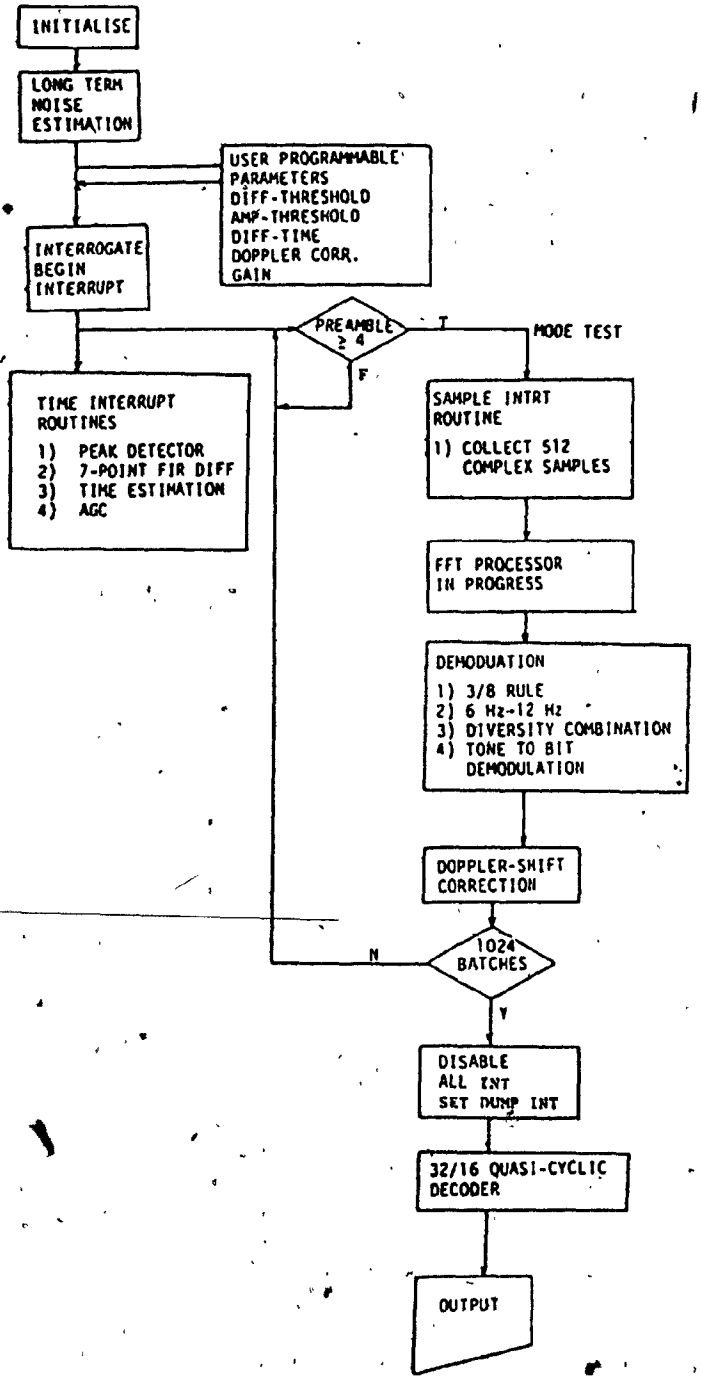


Fig. IV.B.1 FLOWCHART OF SYSTEM OPERATION

preprocessor. The gain adjustment varies depending on the signal level as shown in Figure IV.G.1.

The remaining 12 preambles, besides adjusting the gain, are used to estimate time and doppler shift. Since the Bottom unit has to observe 125 ms of silence for multipath to decay it is important for the Deck unit to predict the time of the next transmission. The diversity combiner output is sampled at a rate of 256 Hz by the CPU; the samples obtained are used as the input to a 7-point FIR differentiator. If the output of the differentiator meets a positive slope threshold for five consecutive times and the amplitude threshold is satisfied, the time base of the sysem is set to a preset value, which was predetermined experimentally. The time base in the Deck unit is a 64 count clock which is incremented once every 3.9 ms for a total period of 250 ms. The time base clock runs continuously after initialisation and is periodically corrected by the time estimates calculated by the differentiator algorithm described in Section IV.C.

To estimate doppler shift spectral analysis of the pilot tones is performed by the FFT processor. The outputs of the filter bins containing the pilot tones are then linearly detected using the 3/8 rule before conversion from 6 Hz to 12 Hz bins and diversity combination is implemented. The pilot tone bins are then tested for any frequency shift and the voltage controlled oscillation in the preprocessor is corrected.

Following the 16 preambles, the Bottom unit transmits the tidal data and its (32, 16) quasi-cyclic code. Forty-four tones (40 data tones and 4 pilot tones) are transmitted for a period of 125 ms of dead time. The processing by the Deck unit is essentially the same

except that all the filter bins in the spectral analysis are considered. After diversity combination, the tones are converted to 16-bit words and stored in memory. One complete transmission consists of 16 preambles and 1024 data and code words. The duration of one transmission is 260 seconds at a bit rate of 32 bps coded.

During the data transmission mode corrections to the time base are made only once every 16 batches; the corrections are based on the average time estimates. Doppler correction is applied once for every two batches (one data word, one codeword). Software safe guards built into the system prevent large changes to any of the system parameters. When transmission is complete a hard copy of the data can be obtained. Error correction described in Section IV.H.1. precedes a data dump. The relevant system parameters such as gain, time estimates, doppler correction and noise level are included in the output. These parameters provide information on the S/N ratios and doppler shift for that particular transmission. A typical data dump is shown in Table IV.B.1.

```
ERROR CORRECTED DATA AND CORRECTION WEIGHT

FFFF 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF 0000 FFFF 0000
CCCC 0000 CCCC 0000 CCCC 0000 CCCC 0000 CCCC 0000 CCCC 0000 CCCC 0000 CCCC 0000
0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000
AAAA 0000 AAAA 0000 AAAA 0000 AAAA 0000 AAAA 0000 AAAA 0000 AAAA 0000 AAAA 0000

TIDAL DATA AND CODE DATA

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
CCCC 9999 CCCC 9999 CCCC 9999 CCCC 9999 CCCC 9999 CCCC 9999 CCCC 9999 CCCC 9999
0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 000C 0000 0000
AAAA 5555 AAAA 5555 AAAA 5555 AAAA 5555 AAAA 5555 AAAA 5555 AAAA 5555 AAAA 5555

FFT OUTPUT DATA 173 BINS -1033HZ TO +1033HZ 12HZ APART

000E 011A 0059 000E 00A6 0062 0042 0212 02E4 008C 0030 0234 0442 0144 0050 0292
04C7 0160 0059 009F 0110 0096 007A 0132 016A 009E 0006 023F 0465 00C8 00A0 0282
068C 010C 009D 0166 02E3 00FD 007C 00BA 014A 00C6 0081 01FC 04A9 0089 0047 0334
0021 014C 0057 020A 0450 0151 00A5 015E 0481 01A7 0096 0254 0426 014C 00F3 0228
0402 018A 0060 015C 0201 00CE 0081 0259 01A4 0082 0107 02EA 0150 0088 0312 0663
0139 006F 0106 0449 0214 04EC 0909 03CF 030C 0104 0065 0231 0457 0107 0007 0303
000F 0229 00A0 0202 060E 0155 00CE 0362 0419 0000 0299 05EA 0290 0082 0208 0480
017E 00CE 0390 0799 02A6 00AC 0426 0549 017E 00C0 0177 0209 017E 00C2 0165 0163
0152 0002 0201 062E 0167 00AA 0290 051E 017D 0084 028F 0690 0145 0009 0142 0364
0157 00C7 0142 020C 005E 0075 0263 0302 000A 0044 01A0 0270 0186 007A 01C4 0306
00F4 0060 000F 011D 0068 0063 000F 0045 006A 0018 00FF 0297 0075

DIVERSITY COMBINED OUTPUT

07D4 1269 06E0 02F6 0810 0F34 05A7 033E 0C74 1973 063A 0234 0005 19FC 06D0 06A0
099C 08FF 05EF 02C0 07EA 0F3D 0612 0302 0804 17E3 040F 035A 0AF0 18FF 0652 0297
AGCH AGC  VCO ERRORS TIMEDELAY

0311 5005 0300 0000 3005
```

Table IV.B.1 TYPICAL TRANSMISSION DATA DUMP. RANGE OF 500 M, WATER DEPTH OF 25 M, BOTTOM UNIT TRANSDUCER DEPTH OF 13 M., TOP UNIT TRANSDUCER DEPTH OF 16 M., BOTTOM UNIT TRANSMIT POWER 1.5 WATTS

IV.C. TIME SYNCHRONIZATION

IV.C.1 INTRODUCTION

The tones from the Bottom unit are transmitted for a period of 125 ms followed by a 125 ms period of silence, to allow for multi-path decay. Each 125 ms burst of tones represents a 16 bit tidal data or parity word. To prevent loss of signal the Deck unit must sample the tone burst at the appropriate time, in short the Bottom and Deck unit must be synchronized. To aid in this synchronization, the Bottom unit transmits four pilot tones together with the data tones. These pilot tones are filtered, rectified, and integrated to form the diversity combined output as shown in Figure IV.C.1.

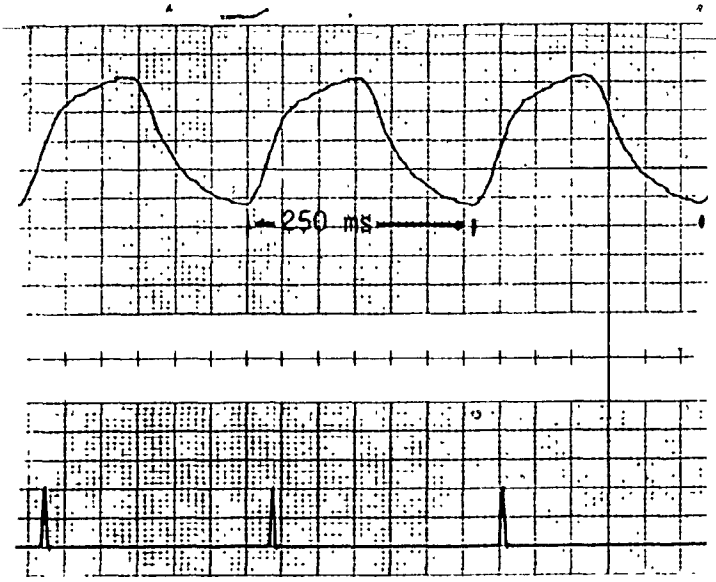
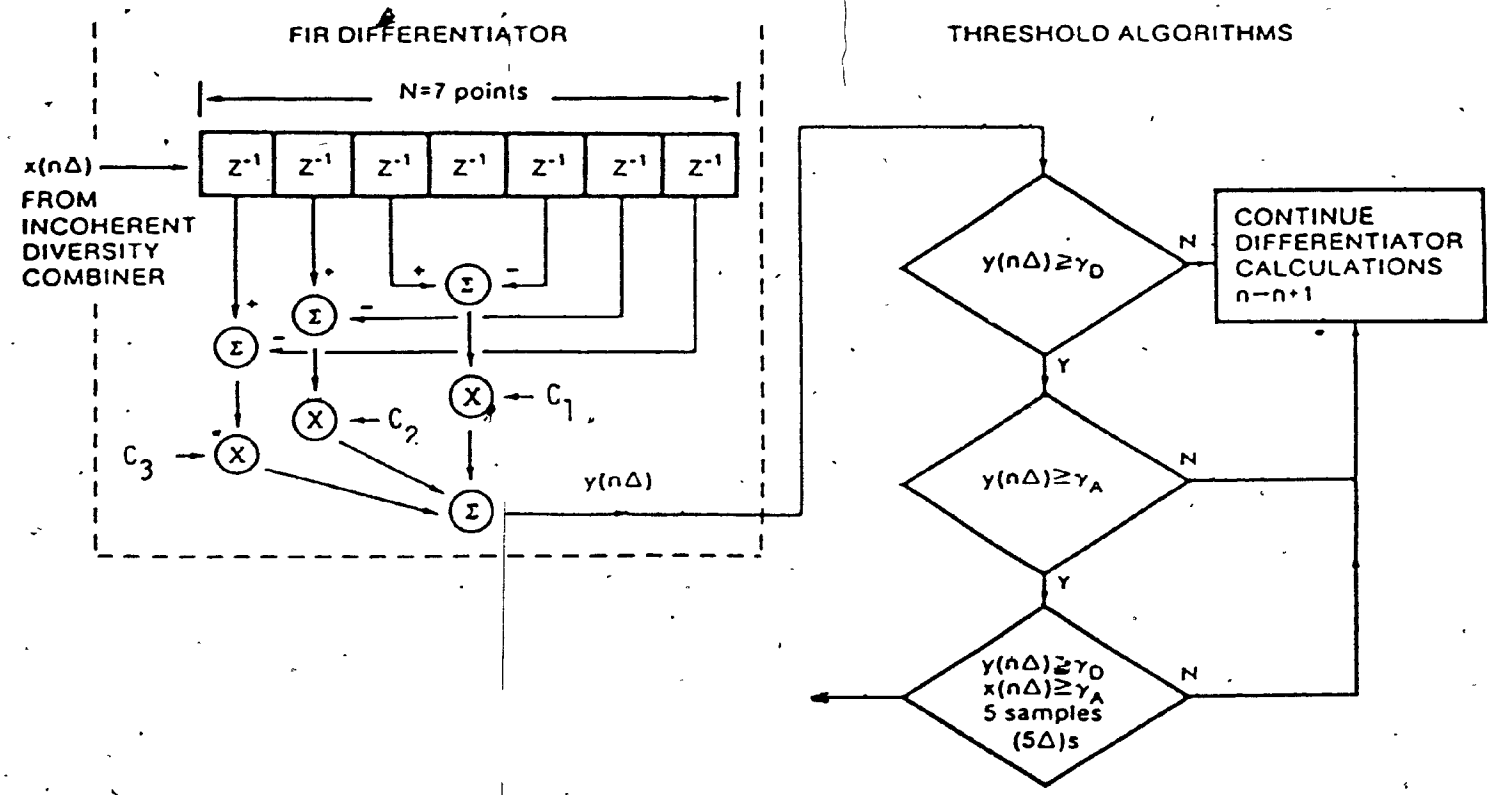


Fig. IV.C.1 DIVERSITY COMBINER OUTPUT AND TIMING MARKER

The output of the diversity combiner is sampled at a rate of 256 Hz by the CPU. These samples are differentiated by a 7-point Finite Impulse Response (FIR) digital high pass filter. By testing for the positive transition, an accurate time estimate is made. The 7-point FIR



NOTES: z^{-1} denotes unit delay, $\Delta = 2\pi/\omega_s$.
T is baud time duration.
$\gamma_D (>0)$ is differentiator output threshold.
$\gamma_A (>0)$ is diversity combiner output threshold.

Fig. IV.C.2 DIGITAL FIR DIFFERENTIATOR AND THRESHOLD ALGORITHMS

Chebyshev-derived differentiator was chosen for its relative insensitivity to noise and acceptable performance even though computations were performed to 8-bit accuracy. [IV.C.1.].

IV.C.2 7-POINT FIR DIFFERENTIATOR ALGORITHM

The flow chart for the implementation of 7-point finite impulse response (FIR) differentiator is shown in Figure IV.C.2. The 7-point differentiator is implemented by Equation (IV.C.1)

$$y(n\Delta) = (X_o - X_{N-6})C_3 + (x_{N-5} - x_{N-1})C_2 + (X_{N-2} - X_{N-4})C_1 \qquad \text{(IV.C.1)}$$

where X_N are input samples obtained from the pilot tone diversity combiner output at the rate of 256 samples/sec.

C_1 = 0C1H, C_2 = 028H, C_3 = 05H, 8-bit (scaled) coefficients.

IV.C.3 TIME ESTIMATION ALGORITHM

The differentiator threshold must be met five consecutive times before an estimate of time can be made. Furthermore, since differentiators are sensitive to noise, input samples must meet an amplitude threshold. The differentiator threshold is tested on the positive edge of the curve to avoid the influence of multipath decay on the time estimate. Once the two thresholds are met, the time based clock is updated immediately in the preamble mode, or once every 16 batches if in the data transmission mode. In the data transmission mode, an average of the time estimates for 16 batches is calculated. The

algorithm for the threshold tests performed on the output of the differentiator is shown in Figure IV.C.3. The algorithm for the average time estimates over 16 batches of data is shown in Figure IV.C.4.

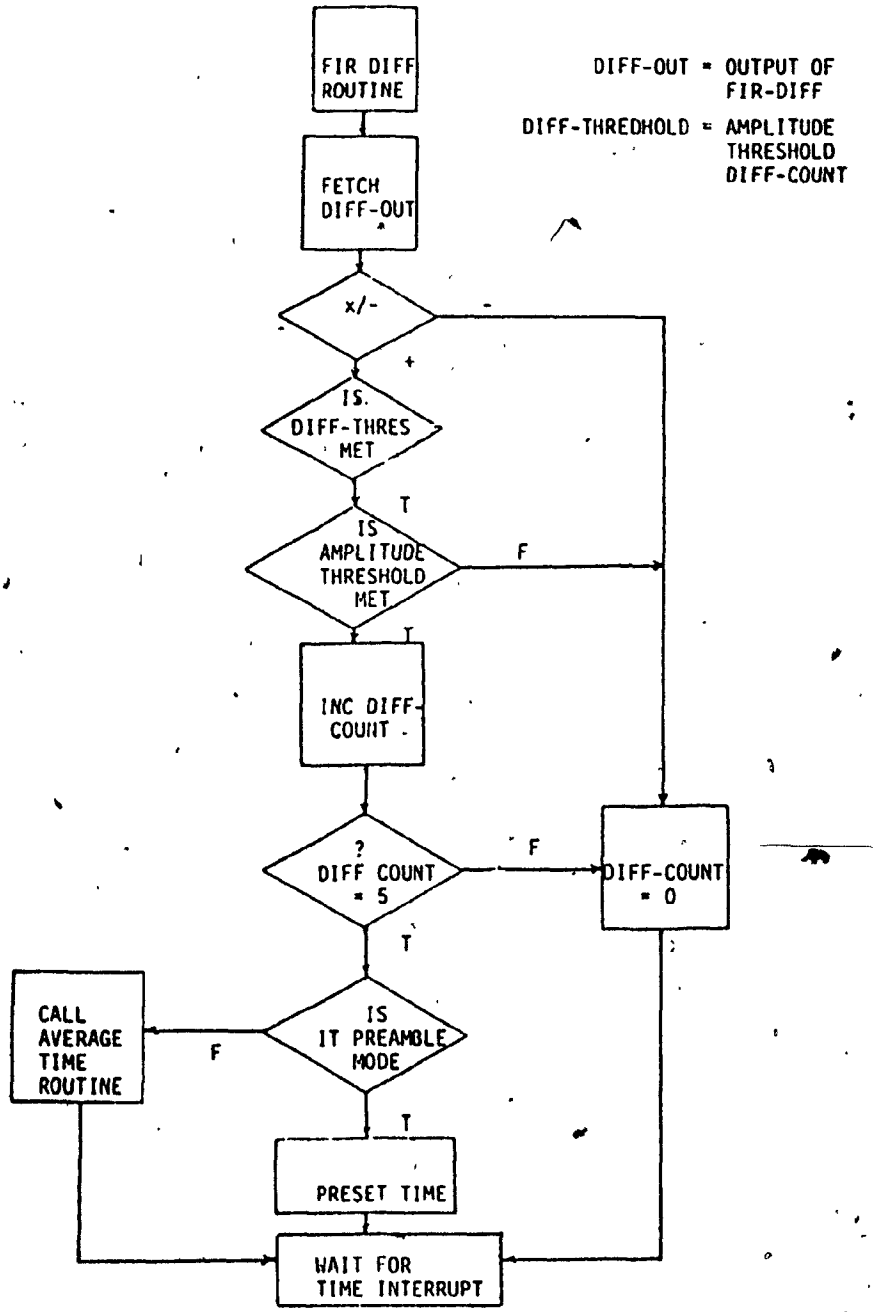


Fig. IV.C.3 DIFF THRESHOLD TESTING

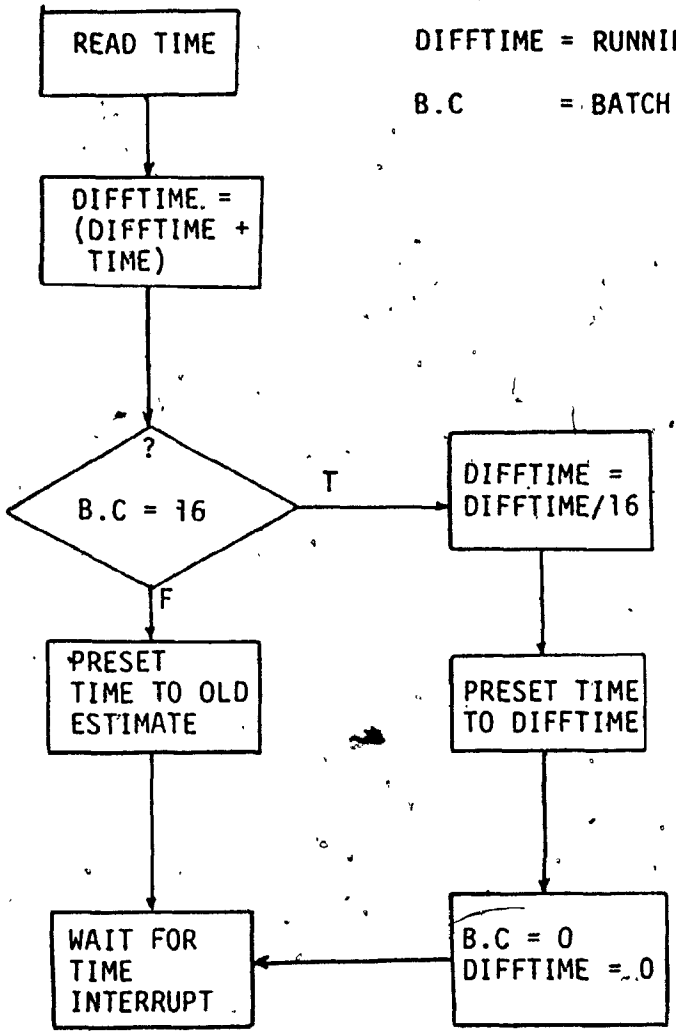


Fig. IV.C.4 TIME AVERAGING OVER 16 DATA BATCHES

IV.D. NOISE ESTIMATION

In chapter II it is shown that the ambient noise varies for the different geographical regions. The software for the Deck unit includes an algorithm for estimating the background noise in the region and adjusting the gain of the preprocessor so that the received signal will fall within the A/D convertor window. This is a particularly important task, as the first preambles transmitted by the Bottom unit are used for *initial* time synchronisation. In Section II.F.1, the worst case signal-to-noise ratio is estimated to be 12 dB. [IV.D.1.]. Since the gain programmable amplifier described in Section III.D.3 is designed to make gain changes of 2 dB, it is necessary to set a window about the desired noise level, rather than having a single desired value. The noise level is adjusted between the 8th and 15th levels of the 8-bit A/D convertor. This leaves 4 bits for the signal, which is approximately 24 dB. This noise level is consistent with the amplitude threshold of 5 bits selected for the differentiation.

The long term noise estimation (*LTA*) algorithm needs the time synchronizer A/D convertor every 4 milliseconds for a total of 1.024 seconds. It then calculates the *LTA* noise as shown in Figure IV.D.1. The gain of the preprocessor is then adjusted until the noise level is between the 8th and 15th levels of the convertor. If the noise in the region is too high and cannot be adjusted, the algorithm sets the minimum gain and informs the operator. The amount of gain required is stored in order to later calculate the average signal-to-noise ratio. The hardware used to collect the noise samples is shown in Figure IV.D.2. This hardware is covered in more detail in Section III.

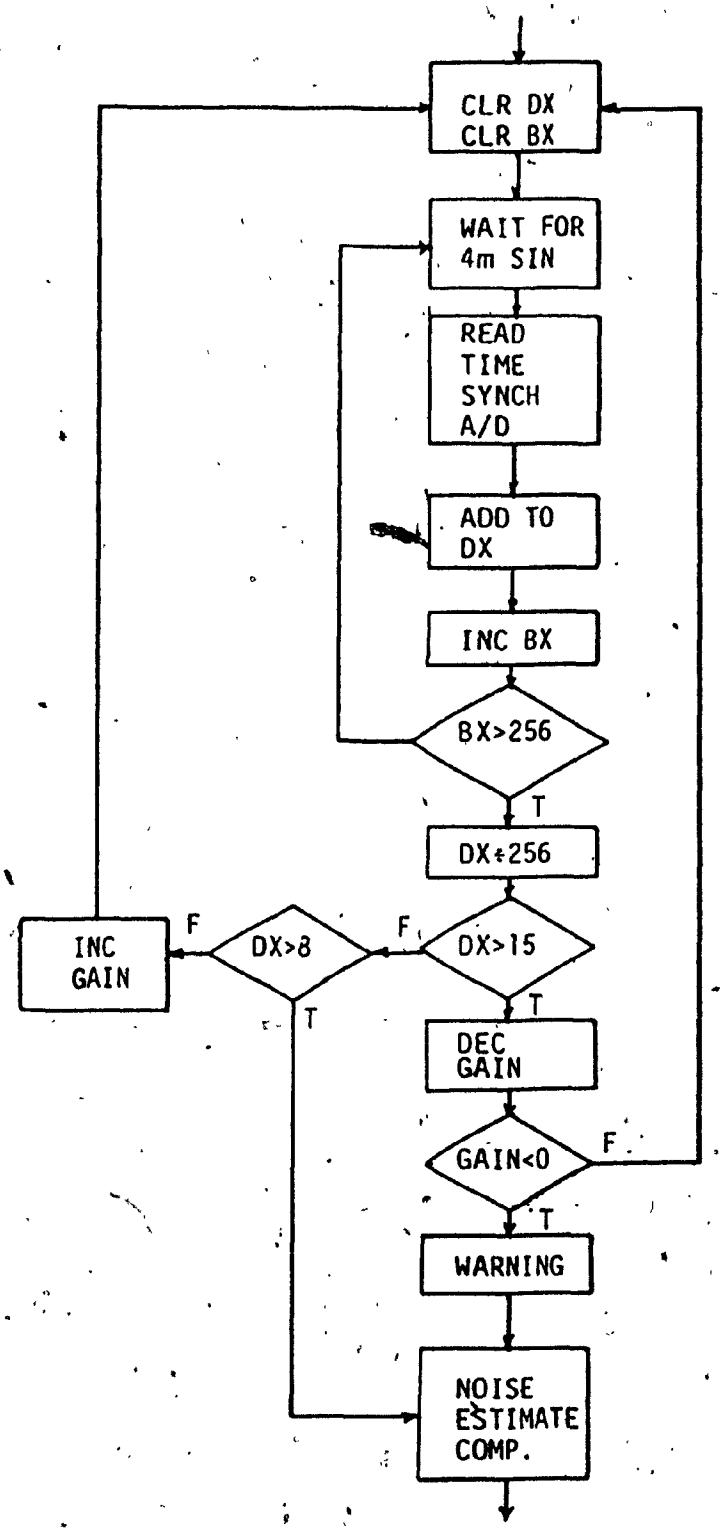


Fig. IV.D.1 FLOW CHART NOISE ESTIMATION

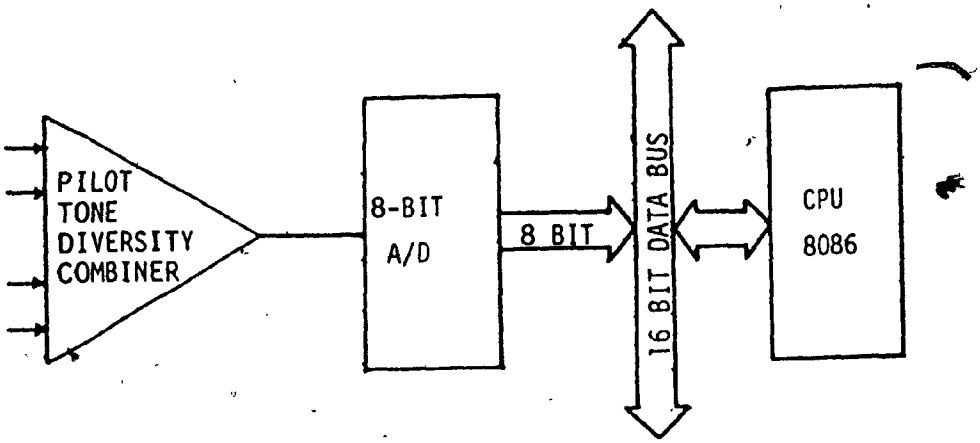


Fig. IV.D.2 HARDWARE FOR NOISE ESTIMATION

IV.E. LINEAR DETECTION

After spectral analysis is complete, linear detection is used to determine the energy of the tones. The tones transmitted from the Bottom unit cover the frequency range of + 1020 Hz to - 1020 Hz; to this band, a guard band of 18 Hz is added to accomodate doppler shift. This total band then contains 346 filter bins of the 512 filter bins produced after spectral analysis. The energy in each bin is evaluated using (IV.E.1), which is known as the "3/8 rule", and provides an approximation to the rms value. The flowchart for the software algorithm is shown in Figure IV.E.1.

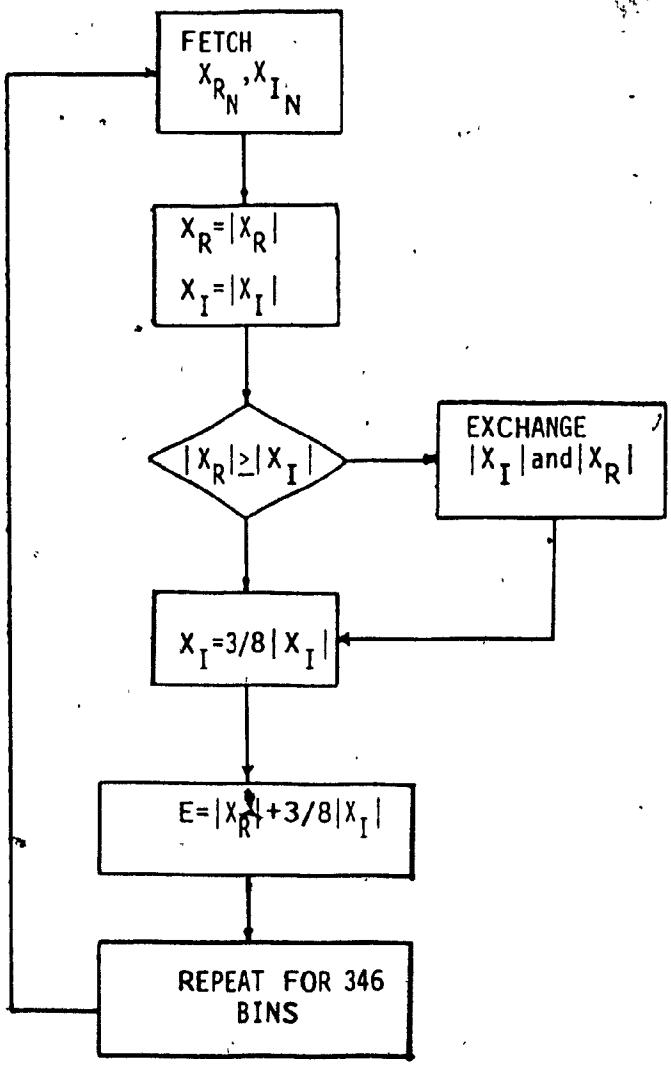


Fig. IV.E.1 FLOW CHART OF LINEAR DETECTION

Loop=counter for 1 bin combination

SI =frequency of bin

DI =storage address for 12 Hz

AX, BX } 16 bit registers

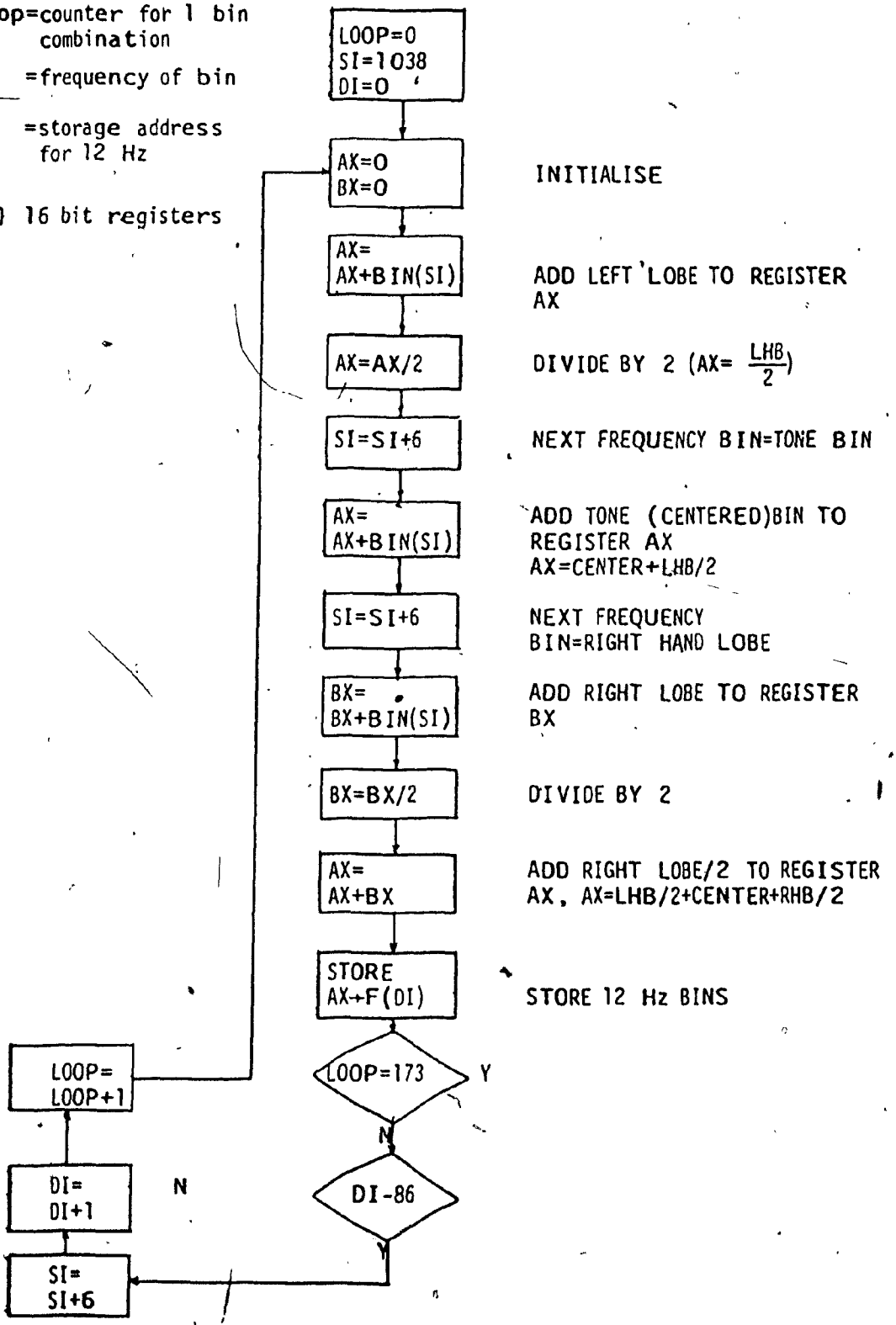


Fig. IV.E.2 FLOW CHART 6 Hz TO 12 Hz BIN

$$\text{Energy of tone} = \begin{cases} |X_R| + 3/8|X_I| & |X_R| \geq |X_I| \\ 3/8|X_R| + |X_I| & |X_R| < |X_I| \end{cases} \qquad \text{(IV.E.1)}$$

where X_R and X_I are the complex Fourier components of the tone. It is seen that the scaling in (IV.E.1) may be accomplished using binary shifts and adds.

IV.E.3 6 Hz to 12 Hz CONVERSION

As described in Section III.D. the input signal is sampled at a rate of 3072 Hz for a period of 1/6 second, and stored in the FFT input memory. Therefore, the dicrete Fourier transform analysis consists in passing the received signal through 512 filters of 6 Hz bandwidth, (BW = $\frac{1}{T}$ = 6), covering the frequency range -1530 Hz to +1536 Hz (range = $f_{s/2}$ = 3072/2). Frequency dispersion increases the width of the received tones to approximately 12 Hz as described in Section II.D. To account for the energy that falls outside the 6 Hz bins, the Deck unit adds half the energy from the two adjacent bins to the energy in the tone bin. The flowchart to implement this conversion is shown in Figure IV.E.2. For other applications or environments the scaling factors of the adjacent tone bins may be easily altered.

IV.E.4 DIVERSITY COMBINATION

In the previous algorithm, energy from the bins adjacent to the tone bins is added to the energy of the tones. This reduces the number of bins from 346 to 173 bins, while increasing the bandwidth of

the bins to 12 Hz. The next step in the demodulation process is to combine the five diversities for the data tones and the four diversities for the pilot tones. The spectral allocation of the data tones and pilot tones is shown in Figure IV.E.3. Each diversity band contains 32 bins, for a total of 160 data bins. Diversity combination consists in summing the five diversity bands. This produces 32 diversity combined bins, each group of 4 carrying 2 bits of data, for a total of 16 bits. The four pilot tones and their two adjacent bins are also summed together. This information is used to determine the average doppler shift. After this addition, three bins of pilot tones remain. Figure IV.E.4a,b is the flowchart for diversity combination.

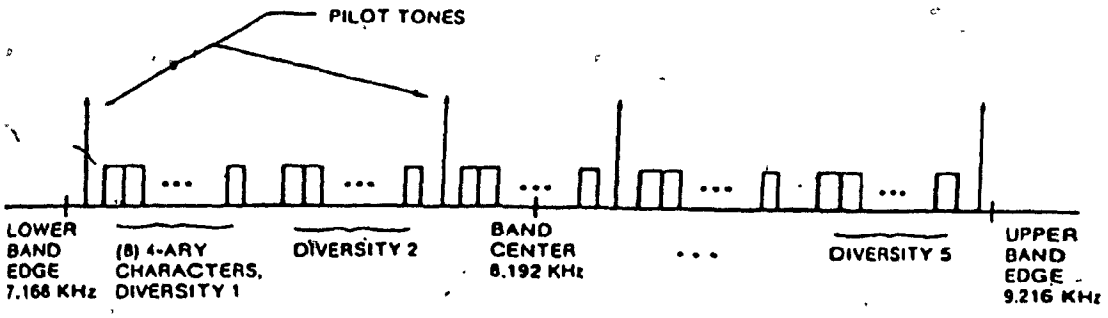


Fig. IV.E.3 SPECTRAL ALLOCATION OF DATA AND PILOT TONES

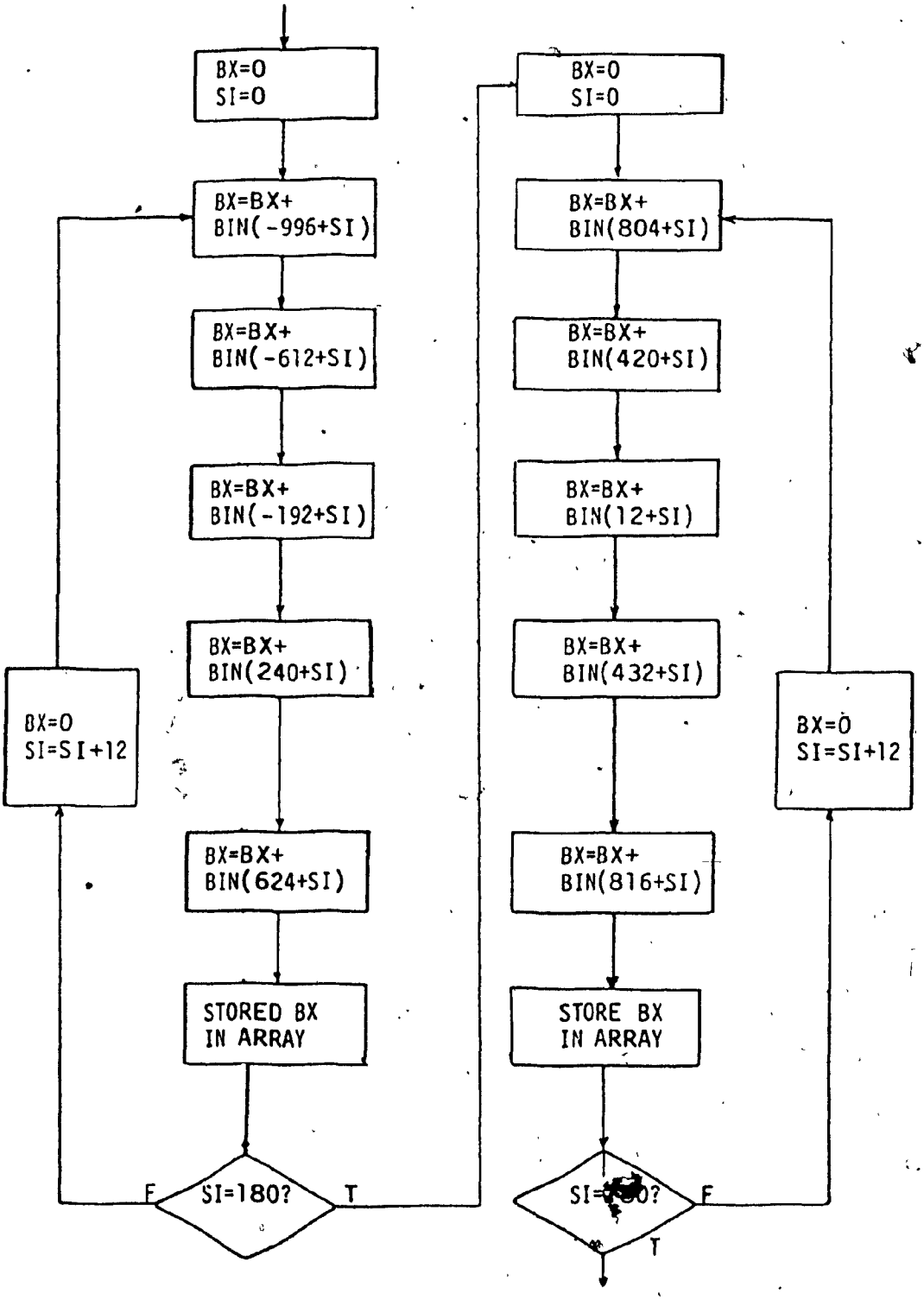


Fig. IV.E.4a DIVERSITY COMBINATION OF DATA TONES

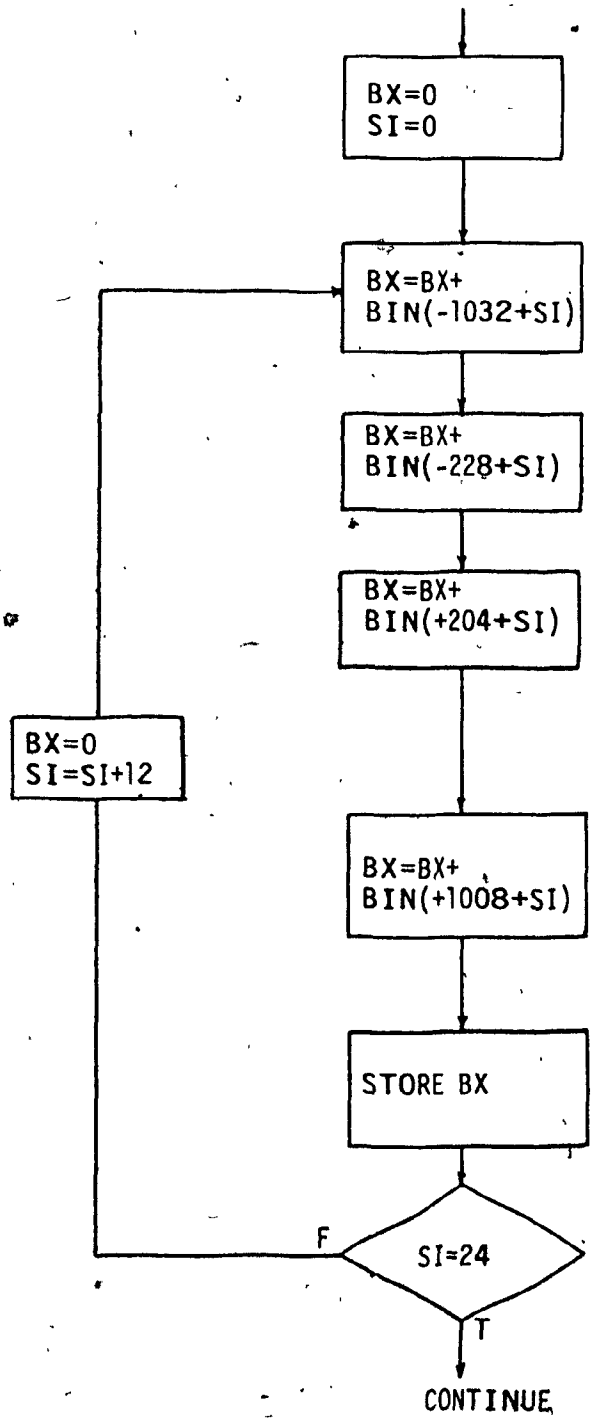


Fig. IV.E.4b PILOT TONE DIVERSITY COMBINATION

IV.E.5 TONE-TO-BIT (MFSK) DEMODULATION

Diversity combination of the data tones has the effect of reducing the number of tone bins to 32. These 32 bins, when properly demodulated will produce a 16-bit data word. Since the MFSK, where m=4, modulation method is used, every four bins represent two bits of data. The four bins represent the bits 00, 01, 10 and 11. The demodulation algorithm finds the largest of the four bins and assigns the proper bits to the 16-bit word. The process is repeated eight times starting with the two most significant bits (MSB). In the flowchart, shown in Figure IV.E.5, A, B, C, D represent the contents of the first four bins in the 32-bin array starting from the highest address, which represents the MSB's of the 16-bit word. The incoherent MFSK modulation scheme chosen is well-suited to the acoustic telemetry application, as it does not require an absolute threshold level for demodulation and is insensitive to the random phases of the received tones.

IV.F. DOPPLER CORRECTION

Doppler shift is estimated by comparing the diversity combined output of the pilot tones with a set of 19 templates. Each template consists of three values, representing the energy in three adjacent 12 Hz filters. These values correspond to the expected ensemble of energies for a pilot tone shifted by $\pm$ 21 Hz, in 19 increments. The software algorithm consists in comparing the 19 templates with the energy in the three pilot tone bins. Since each template represents a frequency shift of 2.3 Hz, the template that most closely correlates the energy in the three pilot tone filters will represent the doppler

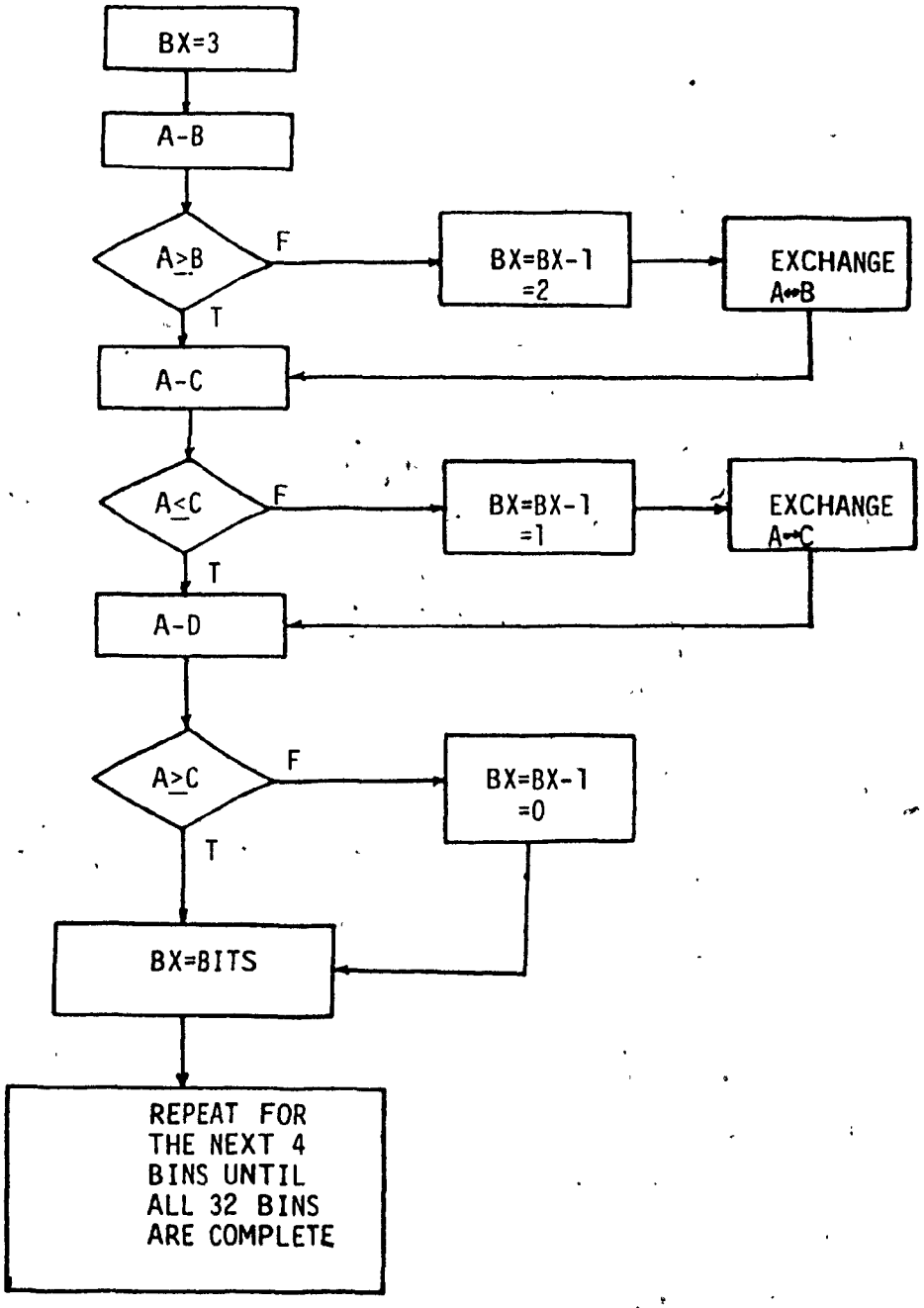


Fig. IV.E.5 FLOW CHART TONES TO BITS CONVERSION

shift that has occurred. The processing may be thought of as using a FIR matched filter for composite hypothesis testing.

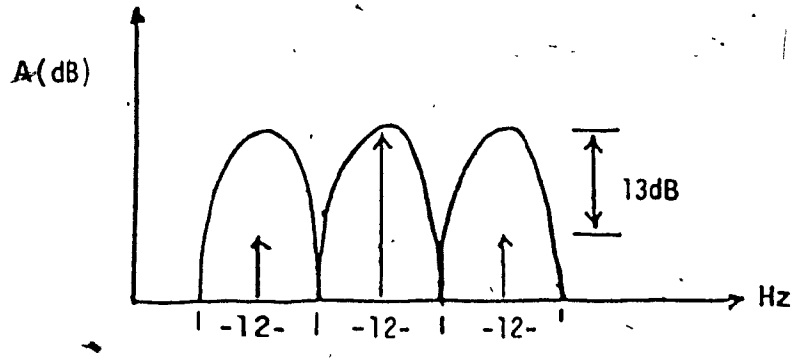


Fig. IV.F.1 DIVERSITY COMBINED PILOT TONE AND ADJACENT BINS NO DOPPLER SHIFT

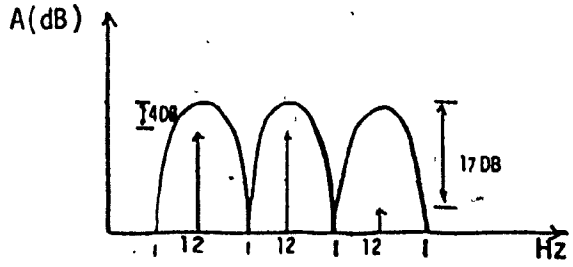


Fig. IV.F.1(b) PILOT TONES SHIFTED -21 Hz

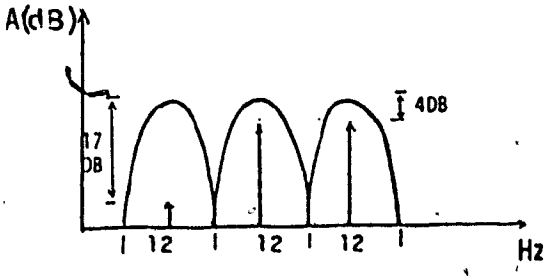


Fig. IV.F.1(c) PILOT TONES SHIFTED +21 Hz

The nineteen templates are arranged into three groups to represent three cases: (1) the center bin has the most energy, (2) the right-hand bin has the most energy and (3) the left-hand bin has the most energy. Each group in turn consists of seven templates with intermediate frequency shifts. The software algorithm first finds the group of templates which most closely matches the pilot tones. The second part of the routine 'fine tunes' the match with one of the seven templates within the group. The Table of Templates is shown in Figure IV.F.2, and the software algorithms in Figure IV.F.3 and Figure IV.F.4.

DOPPLER TEMPLATES

```
                SI
DW      1       4864,8556,42667
DW      4       5335,10193,51893
DW      7       5508,10944,61239
DW      10      6178,14961,65535
DW      13      6964,23097,61239
DW      16      7271,32995,51893
DW      19      8556,42667,42667    ;----------
DW      22      10193,51893,32995
DW      25      10944,61239,23097
DW      28      14961,65535,14961
DW      31      23097,61239,10944
DW      34      32995,51893,10193
DW      37      42667,42667,8556    ;----------
DW      40      51893,32995,7271
DW      43      61239,23097,6964
DW      46      65535,14961,6178
DW      49      61239,10944,5508
DW      52      51893,10193,5335
DW      55      42667,8556,4864
```

Fig. III.F.2 DOPPLER TEMPLATES

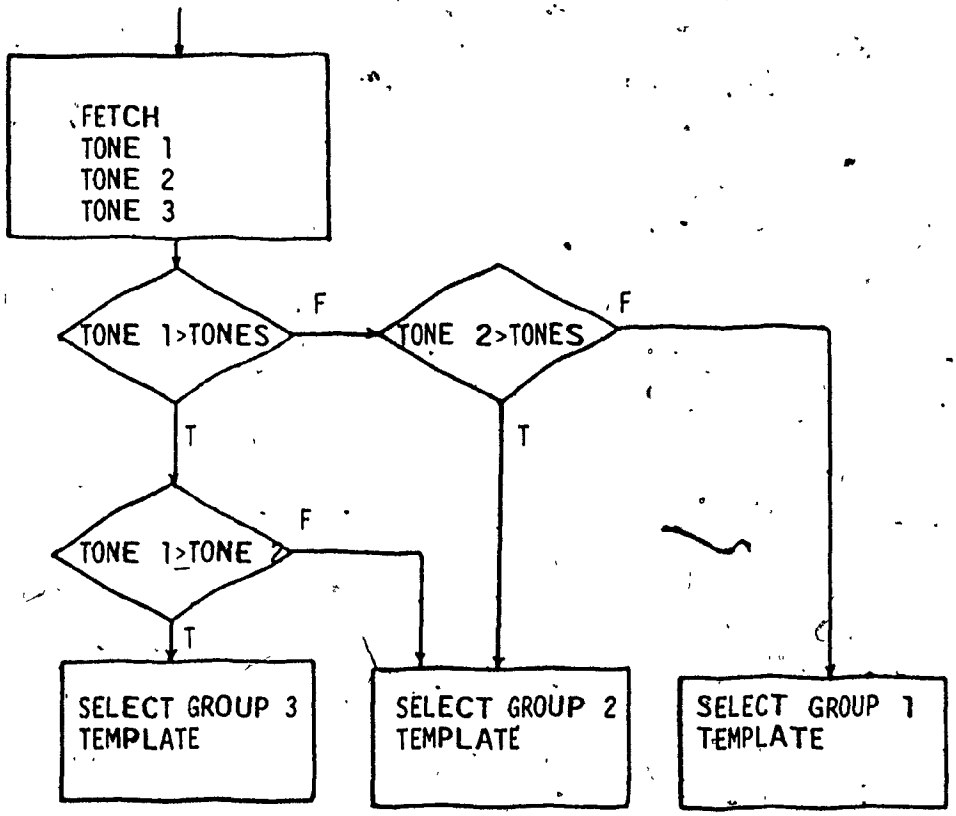


Fig. IV.F.3 FLOW CHART FOR SELECTION OF TEMPLATE GROUP

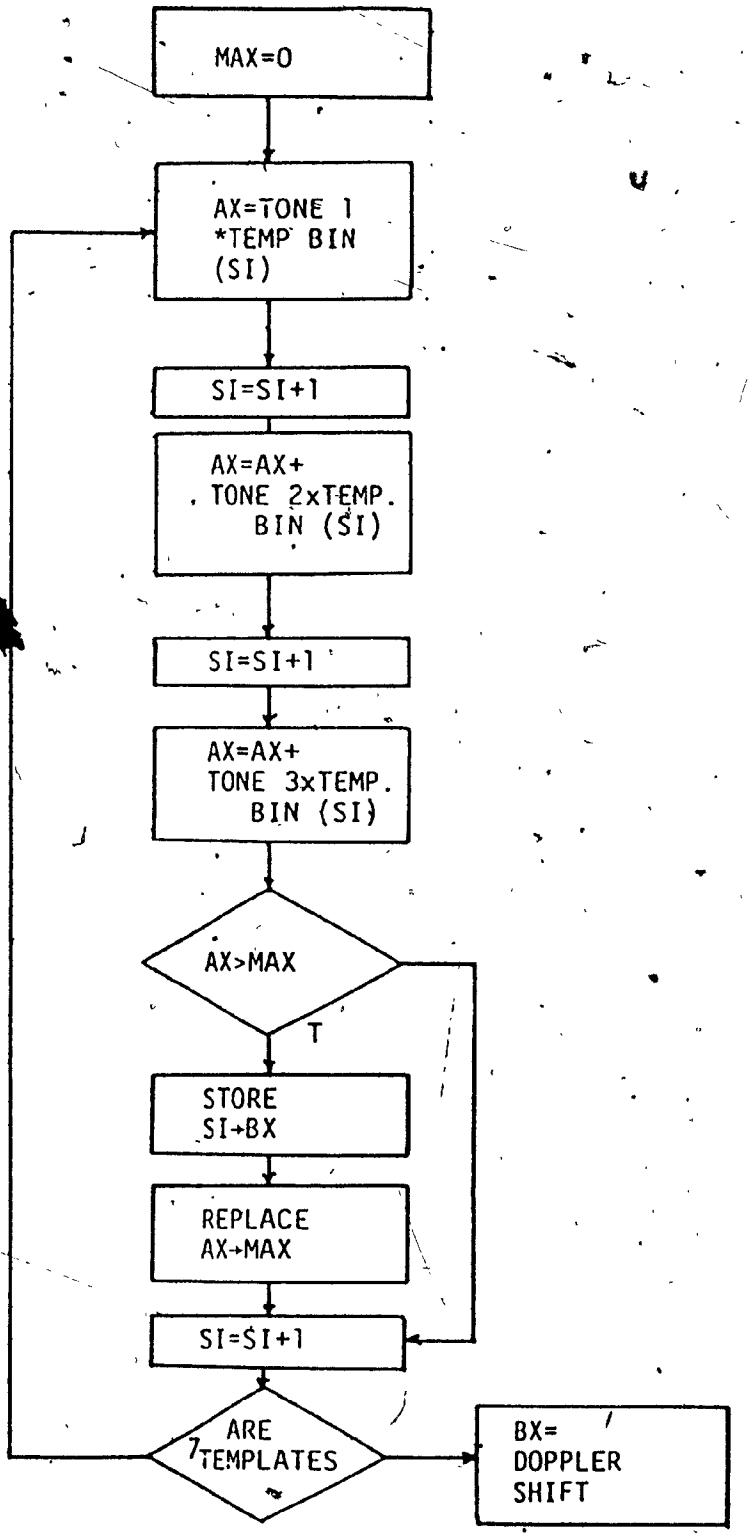


Fig. IV.F.4 FLOW CHART FOR DOPPLER CORRECTION

BX represents the template that matches the doppler shift. The number in BX can vary from 3 for a maximum positive shift, to 30 for zero shift, to 57 for a maximum negative shift. The VCO hardware described in Section III.D.4 . is controlled by an 8-bit word for a total shift of ±25 Hz with a resolution of. Bx is scaled such that it corresponds to an 8-bit word as shown below.

$$BX : 3 \leq 30 \leq 57$$

$$\sim -108 \leq 0 \leq +108$$

Using the VCO characteristics ±128 represents a ±25 Hz shift we have,

$$BX \text{ can equal } \pm 25 \times \frac{108}{128} = \pm 21.09 \text{ Hz}$$

The maximum range of the control word is limited by software to produce only a ±18 Hz shift.

IV.G. AUTOMATIC GAIN CONTROL

The automatic gain control algorithm reads the pilot tone incoherent diversity combiner output to determine the signal strength. There are three types of signals which require different methods of gain adjustment. The three cases are: (1) severe overloading of the A/D convertor and the preprocessing analog amplifiers, (2) A/D convertor saturation and (3) weak signals. Severe overloading is normally present in the synchronisation mode at the beginning of transmission. It is due to a combination of high signal levels and a low noise

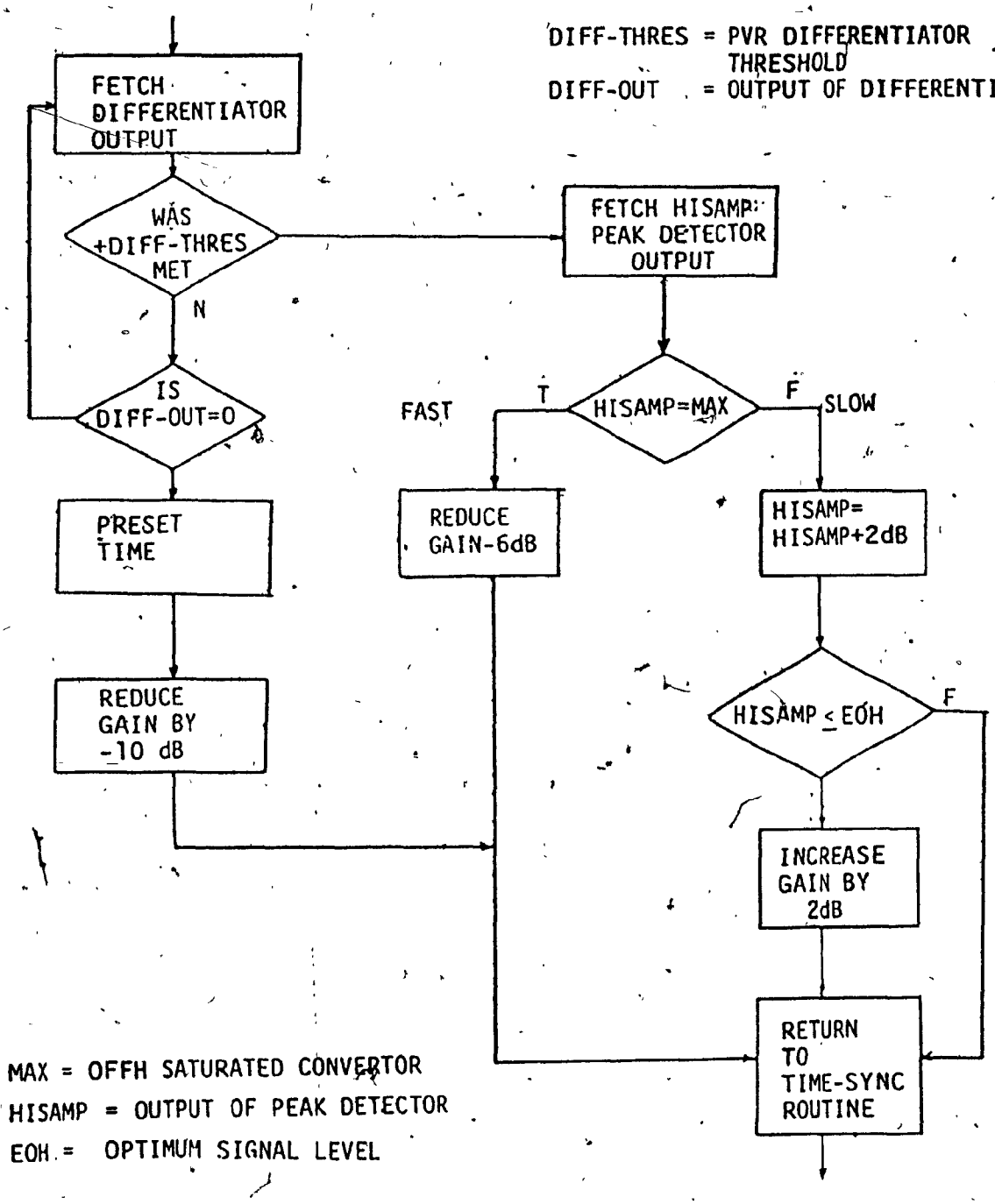


Fig. IV.G.1. FLOW CHART FOR AUTOMATIC GAIN CONTROL

estimate by the Deck unit.

The software algorithm shown in Figure IV.G.1. tests the differentiator output to see if this condition is present. When signal levels are too high, i.e., more than +60 dB above noise, the differentiator output is zero, furthermore the positive differentiator threshold will not be met. Refer to Section IV.C.2. for more details. This will result in the loss of data as synchronisation will be lost. In this case, the software algorithm reduces the gain by 10 dB and presets the time base.

The second type of signal causes saturation of the A/D convertor but does not saturate the differentiator. This condition can occur e.g., if the orientation of the transducers change and the signal strengths increase. The convertor may then saturate for a few samples only but not long enough to cause a zero differentiator output. In this case, the software algorithm reduces the gain by +6 dB. The algorithm is called the "fast attack" AGC, and is shown in Figure IV.G.1.

The final type of signal can also occurs during transmission but does not saturate the convertor. Weak signals may result from fading due to arrival of different signal paths, and changes in the orientation of the transducers. The software algorithm is shown in Figure IV.D.1. In this case, the algorithm makes gain changes of +2 dB, provided the change does not saturate the convertor. To allow for some flexibility in adjusting the gain, the signal is always optimized within 1 dB from the top of the 8-bit A/D convertor. To determine the maximum signal level, a peak detector algorithm is used. The algorithm shown in Figure IV.G.2. compares successive samples from the

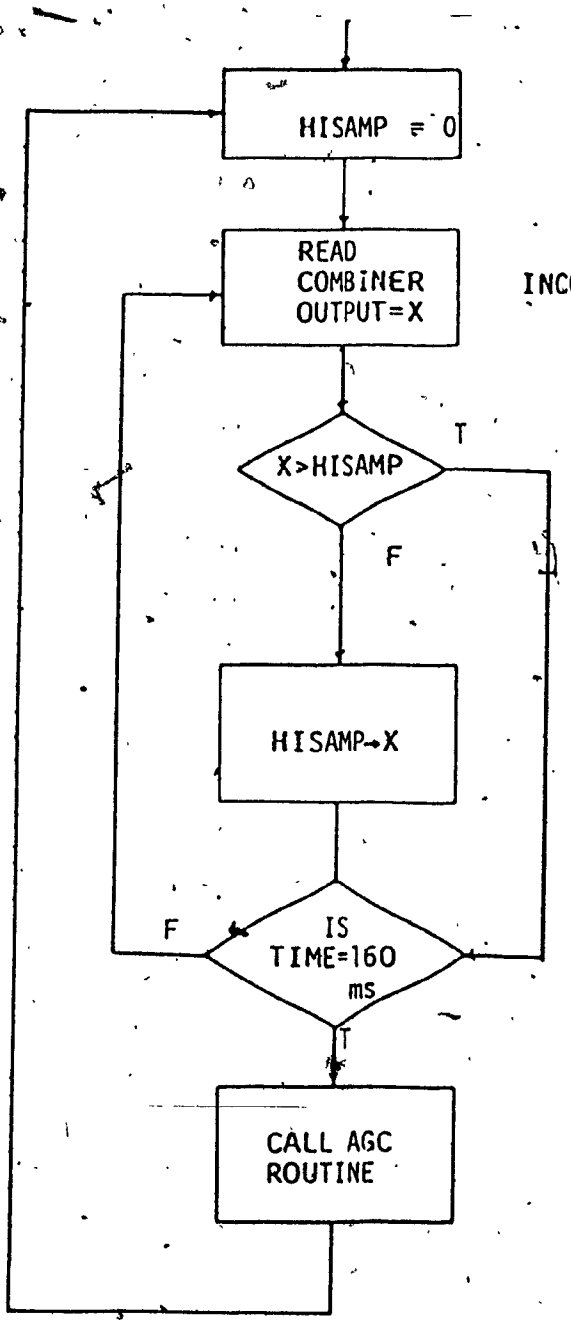


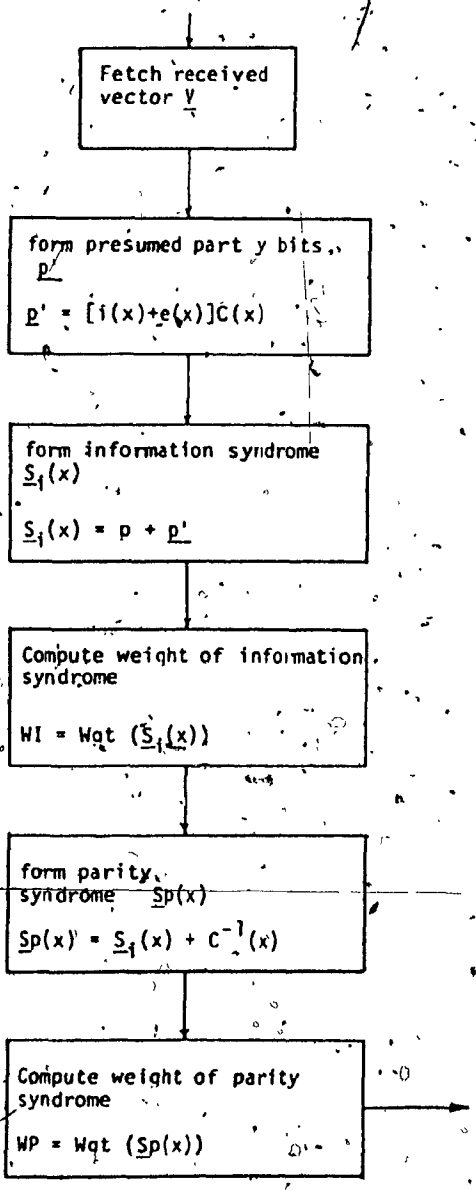
Fig. IV.G.2 FLOW CHART PEAK DETECTOR

pilot tone incoherent diversity combiner, and saves the largest sample in each 250 millisecond time interval.

IV.H ERROR CORRECTION

Coding is employed in the underwater telemetry system to provide some measure of protection from fading. As a result a 16-bit tidal data transmission is followed by its 16-bit parity codeword. A rate one-half quasi-cyclic code is employed in this system as decoding is relatively simple. Decoding is straight forward, if the transmitted code vector $V(x)$ is corrupted by three or less errors and all the errors fall in the information or parity vectors. Decoding is more complex if the errors occur in both the information and parity vectors.

Karlin's decoding algorithm for the decoding of rate one-half quasi-cyclic codes is used. The essential features of this algorithm are that the weight of the information syndrome (WI) and the weight of the parity syndrome (WP) determine the number and location of the errors, (i.e. in the information or parity vector). WI and WP are first computed by the algorithm shown in Figure IV.H.1. The weights of these two terms (WI, WP) determine the method of correction if the number of errors is less than or equal to three, [IV.H.1.]. Refer to Figure IV.H.2.



Received vector, V
information bits, i
parity bits, p

received message y(x)
y(x) = i(x) + e(x)

e(x) = error pattern introduced in the information bits.

C(x) = circulant or generator matrix

Fig. IV.H.1 FLOWCHART OF INFORMATION AND PARITY SYNDROME

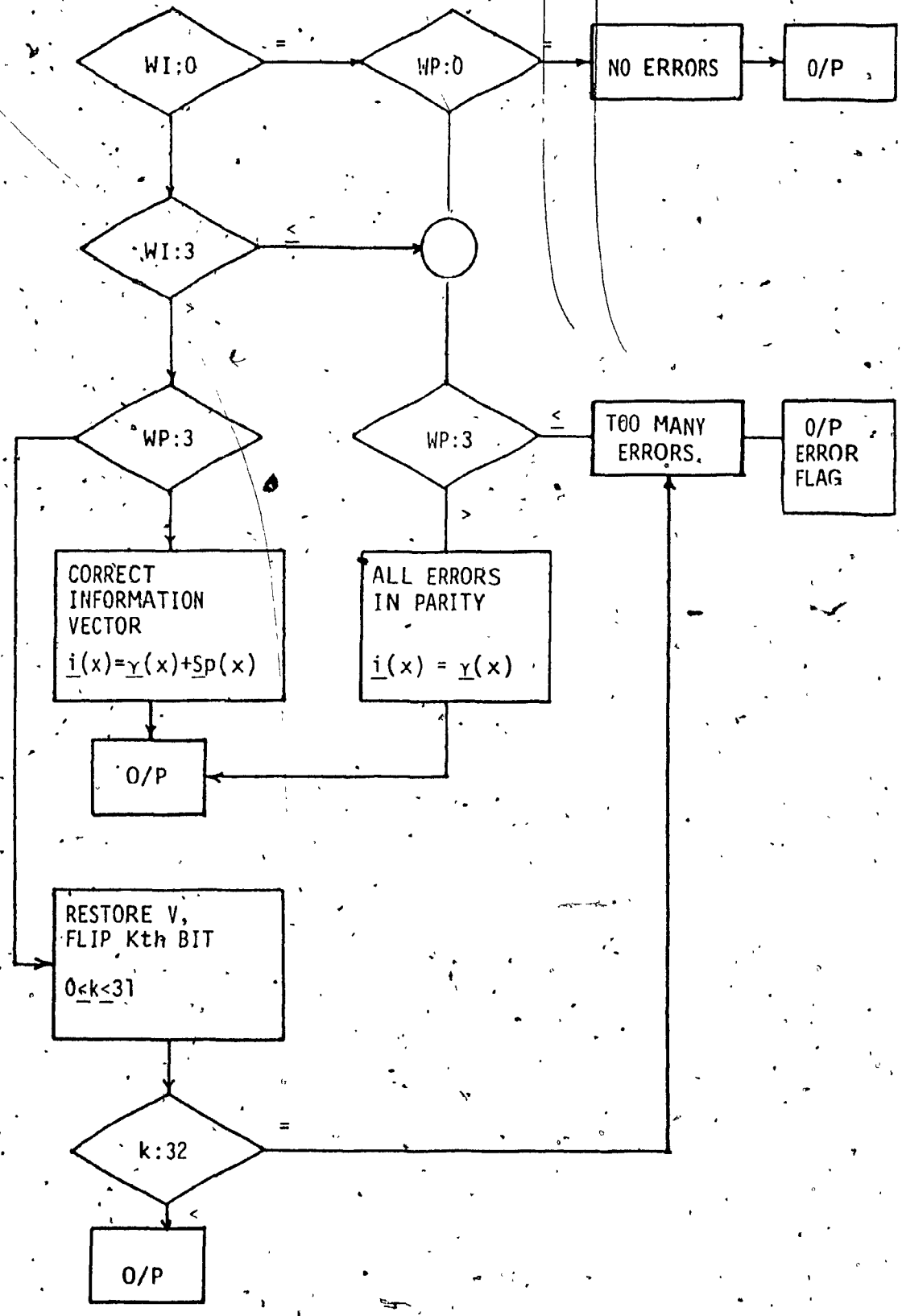


Fig. IV.H.2 ERROR CORRECTION ALGORITHM

CHAPTER IV

REFERENCES

IV.A.1 iAPX User's Manual, Intel Corp., August 1981.

IV.C.1 Morgera, S.D., Digital Filtering and Prediction for Communications Systems Time Synchronization, IEEE Journal of Oceanic Engineering, Vol. OE-7, No. 3, July 1982.

IV.D.1 Dinn, D.F., "Deck Unit Signal Processing", unpublished Memorandum, Bedford Institute of Oceanography, Dartmounth, Nova Scotia, April 1981.

IV.H.1 Lin Shu., An Introduction to Error Correcting Codes, Prentice Hall, New Jersey, 1970.

CHAPTER V

PERFORMANCE AND CONCLUSIONS

V.A. INTRODUCTION

This chapter deals with the performance testing and subsequent design improvements that were made on the Underwater Acoustic Telemetry System. Also included are the results of the sea tests followed by some suggestions for improvements and other applications. The prototype of the telemetry system was completed and delivered to the Bedford Institute of Oceanography (BIO) in December, 1981. Three trials were carried out; one at the BIO laboratories and two sea tests in the Bedford Basin, Halifax. Between these trials dates the equipment was returned to Concordia University for modifications to the design and further tests. The final sea trial on 11, 12 July 1982, was successful and the system is considered ready for further testing in the Arctic.

V.B. FIRST SEA TRIAL

V.B.1 INTRODUCTION

The main areas of concern in the Deck unit were: the time estimation scheme employing the 7-point FIR differentiator, the doppler correction algorithm which is dependent on the performance of the FFT processor, and the gain adjustment algorithm.

During the first sea trial on 3 June 1982 it became apparent that the influence of multipath made accurate time estimation difficult with the scheme used at that time. The extent of multipath was examined by monitoring the output of the diversity combiner with a chart recorder. As shown in Figure V.B.1, the effect of multipath increased the time

at which the negative transition point was reached in the 250 ms time interval. Efforts were made to orient the transducers in such a manner that the multipath problem was reduced. But in doing this, another problem became apparent.

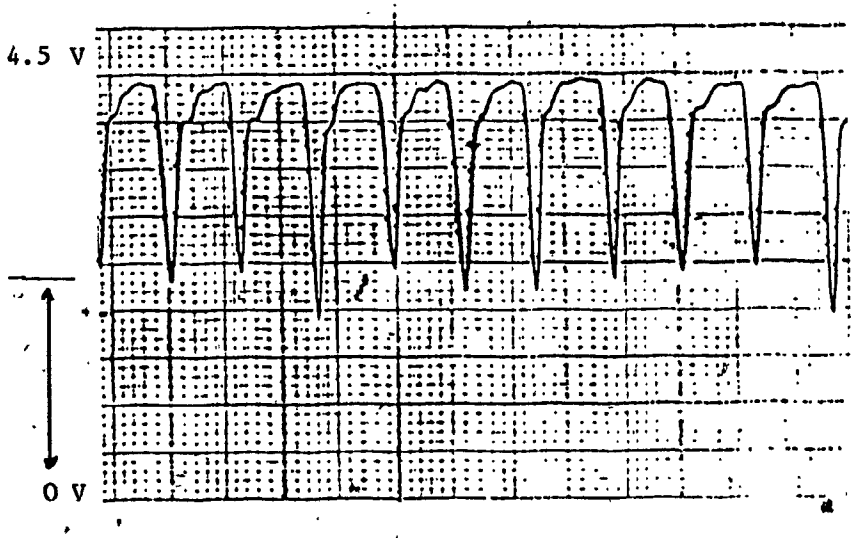


Fig. V.B.1 PILOT TONE DIVERSITY COMBINER OUTPUT IN THE PRESENCE OF MULTIPATH (80 ms).

The initial gain setting of the Deck unit is determined by estimating the noise in the environment. If this gain selection was high, the time synchronizer hardware saturated, preventing the differentiator threshold from being met. Since the Bottom unit in the first design transmitted only two preambles, the loss of data was inevitable. To prevent saturation the transmitter power on the Bottom unit was reduced and communications between the two units was achieved. Despite this,

synchronisation was lost during transmission when fading occurred. From these results it was apparent that a redesign of the time synchronisation scheme was necessary, and the new design should be immune to fading, signal saturation, and multipath.

V.B.2 FIRST MODIFICATIONS

In the first design of the Deck unit time estimates were made based on the negative transition slope of the differentiator. This region of the diversity combiner output corresponds to the dead time in the transmission period, and any signals present are the result of multipath. Estimates of multipath decay from the environmental studies presented in Chapter II varied between 30 ms to 100 ms. Therefore, in the worst case the dead time seen by the Deck unit is reduced to 25 ms; but this also indicates that the beginning of the next batch is free of multipath from the previous batch. The absence of multipath interference on the positive slope of the differentiator made it the obvious choice for setting the time estimate.

The change to the positive transition slope of the differentiator required only a minimal change to the software algorithm. Initial synchronisation would always be attained, since the differentiator threshold of the first batch would always be met regardless of the signal strength. Gain adjustments which are made at a specific time during the 250 ms time frame can reduce the gain for subsequent batches. To add more reliability to the scheme the number of preambles transmitted from the Bottom unit were increased from two to sixteen. The first four are used exclusively for gain adjustments; the remaining eight

correct gain, doppler and time estimates.

Different gain adjustment algorithms for high and low signals were designed. As a measure of insurance a gain algorithm which was dependent on the differentiator output was added. This algorithm reduces gain by 10 dB if the differentiator output is zero, indicating severe saturation. It was felt that very high signals could prevent the differentiator threshold from being exceeded for five consecutive times. These changes provided excellent performance for signal to noise ratios ranging from 16 dB to 60 dB. To prevent loss of synchronisation due to fading, extreme time estimates are ignored and previously calculated estimates used instead.

Testing on the sea had its drawbacks, one of which was the lack of monitoring equipment to aid in on-site modifications. A method to monitor noise estimates, time estimates, and doppler shift before transmission was desirable. Furthermore, if some of the system parameters could be changed by the user a better understanding of the difficulties and changes could be made on-site. Access to the Deck unit was provided via the RS232 send link and software to monitor or modify system parameters were developed. In essence a diagnostic tool was added to the Deck unit, which contributed to the success of the second sea trials.

V.C. SECOND SEA TRIAL

Sea tests of the acoustic telemetry system were conducted on July 12 and 13, 1982, at the Bedford Institute of Oceanography, Darmouth, N.S. The Bottom unit was placed on board the Tudlik and the Deck unit on board the Phoenix. Transducers from both units were lowered into the Bedford Basin and data was transmitted at different transducer depths

TX	SNR (dB)	Bottom unit Transducer depth (m)	Top unit Transducer depth (m)	Range (m)	Bottom Unit Transmit Power Watts	Number of errors	COMMENTS
1	40	6	6	50	.5	0	-
2	36	24	3	100	1.0	0	-
3	26	24	3	100	1.0	6	Destroyer passed by. Burst noise
4	30	15	20	500	3	0	-
5	28	6	6	500	1.5	0	-
6	42	15	20	500	1.0	0	-
7	40	15	20	500	.5	0	-
8	26	6	6	500	3.0	6	Burst error. Maybe due to deep fading.
9	14	6	9	1000	3.0	0	-
10	26	6	6	1000	3.0	2	excessive multipath due to poor geometry of boats with respect to wharf.
11	26	6	9	1500	3.0	0	-

Table V.C.1 Summary of results from some transmission runs during field testing in the Bedford Basin

and distances. Various data patterns were transmitted successfully, which showed that the effects of frequency dispersion was minimal, since certain data patterns produced tones 12 Hz apart.

The Bedford Basin, unlike the open ocean, has closed boundaries making multipath a serious problem. The muddy bottom of the basin attenuated signals significantly and the noise level was higher due to ship traffic and shoreline industries. This contributed to the poor S/N ratios encountered. Despite these conditions, the system performed excellently and error-free transmission was possible up to 1500 meters. A summary of the eleven transmissions is described in Table V.C.1. Fading is apparent in transmission number 8 where a burst of 6 errors occurred. But with a transmitter power of 6 watts and less rigorous conditions in open sea, performance is expected to improve considerably.

V.D. PERFORMANCE AND IMPROVEMENTS

To improve the reliability and performance of the system several design changes are suggested. Hand shaking between the Deck unit and Bottom unit will improve synchronisation. At present, the Bottom unit transmits the preambles followed by the data as soon as it recognizes the Deck unit interrogation command. There is no knowledge of the quality of communication until the end of transmission which lasts approximately 4 minutes. The need is more urgent since most of the difficulties of synchronisation translate to waste of power in the Bottom unit. Two interrogation commands are suggested: one for the preamble sequence, and the other for the data sequence. Furthermore, the preamble sent by the Bottom unit should be labelled with an identification

number. The Deck unit can then make a decision as to communication link by the time estimates and the preamble labels; only if these conditions are satisfied the second command can be sent to the Bottom unit.

The second improvement deals with increasing the bit rate of the system, which is at present 32 bps coded. An increased bit rate can be achived by transmitting only the differences in consecutive data words rather than the full 16 bits. This is a realistic change as tidal levels do not change abruptly under normal weather conditions. Software changes in both units are required; the hardware is unaffected by this improvement. The transmission of data will still represent 16 bits of data but then bits will represent differences between several tidal data readings. The number of readings it can represent will depend on the maximum change in tide levels expected, for the time intervals readings are made.

Some other improvements relate to the hardware. The programmable amplifiers used in the preprocessor can be replaced by a signals package, recently available on the market. Besides reducing the chip count the performance of this new device has noise and dynamic range superior to the presently used amplifiers.

The voltage controlled oscillator requires some improvement vis-a-vis sensitivity to power supply fluctuations. The problem lies in the stability of the reference voltage used in the D/A convertor. A stable reference source should eliminate this problem.

The speed of the FFT processor can be increased from its present rate of 30 ms. The gain in speed can be obtained by introducing more parallel processing and eliminating the multiplication during the last pass of the FFT, which involves multiplications by zeros and ones.

Faster EPROMS in the address indexing and the microprogram generator will reduce the access time and increase the processing speed. Obviously, a radix-4 implementation will increase the speed but at the expense of more hardware.

Computational noise is present because of the mismatch between the input word size (12 bits) and the 16-bit arithmetic used in the FFT butterfly calculation. To maintain the word size the outputs of the 12-bit analog-to-digital convertors were shifted up by four bits. Two solutions are possible; increase the convertors to 16 bits or reduce the multiplier to 12 bits. The latter is a more reasonable approach as 16-bit convertors are costly whereas a 12x12-bit multiplier would reduce the hardware of the FFT processor.

The proposed improvements involve some software and/or hardware modifications. Obviously some are more cost effective than others. The increased transmission rate is a good example; it would significantly reduce the storage hardware or alternately increase the amount of information gathered. The single most important savings would be in the consumption of power, due to shortened transmission time. Since most of the power is consumed during transmission, a longer battery life is desirable especially when deployed in remote areas. Other changes are fine tuning adjustments and the user must decide the improvements in view of the increased cost. Regardless of these suggestions the system in its present condition is an excellent communications system and satisfies the requirements for efficient transmission of data in the underwater environment.

V.E. OTHER APPLICATIONS

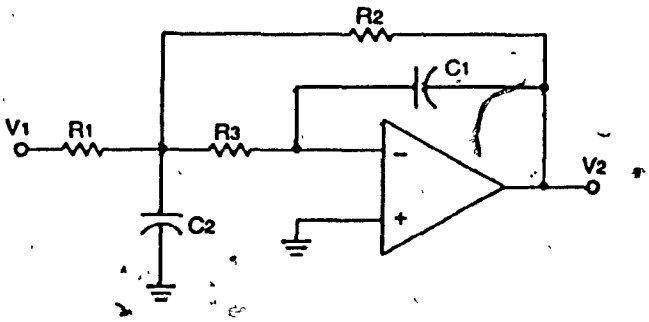
The underwater acoustic telemetry system is a reliable communication link which can be used in many applications where data needs to be conveyed efficiently underwater. The concepts designed into the equipment readily lend themselves to applications other than hydrographic surveying and oceanography. Because of the high data quality possible, the system can be adapted to a number of civil and military uses. These include:

1. the control of seafloor instruments associated with oil exploration and extraction.
2. submarine cable position monitoring.
3. pollution or water quality monitoring.
4. control of submersible vehicles used in ocean exploration and defence.

APPENDIX VI.A

VI.A.1 Design of a Second Order Lowpass Butterworth Filter (Multiple Feedback Filter)

The basic circuit is shown below.



The transfer function of the above filter is

$$\frac{V_2}{V_1} = \frac{-Kb_o}{s^2+b_1 s+b_o} \qquad \text{(VI.A.1)}$$

where b_o, b_1 are constants found in Tables and K is the gain of the filter.

$$b_o = \frac{G_2 G_3}{C_1} \qquad \text{(VI.A.2)}$$

$$b_1 = G_1 + G_2 + G_3 \qquad \text{(VI.A.3)}$$

$$K = \frac{R_2}{R_1} = \frac{G_1}{G_2} \qquad \text{(VI.A.4)}$$

Design Procedure

1) Select $C_2 = 1.0F$

2) Find b_0, b_1 from Tables.

3) Solve (VI.A.2) to (VI.A.4) to find G_1, G_2, G_3

4) Denormalise capacitor and resistors using

$$C_p = \frac{C_n}{u(ISF)} \qquad \text{(VI.A.5)}$$

$$R_p = R_n(ISF) \qquad \text{(VI.A.6)}$$

where f_c = cut off frequency.

f_n = normalised frequency

ISF = impedance scaling factor

where $ISF = \frac{f_c}{20\pi}$

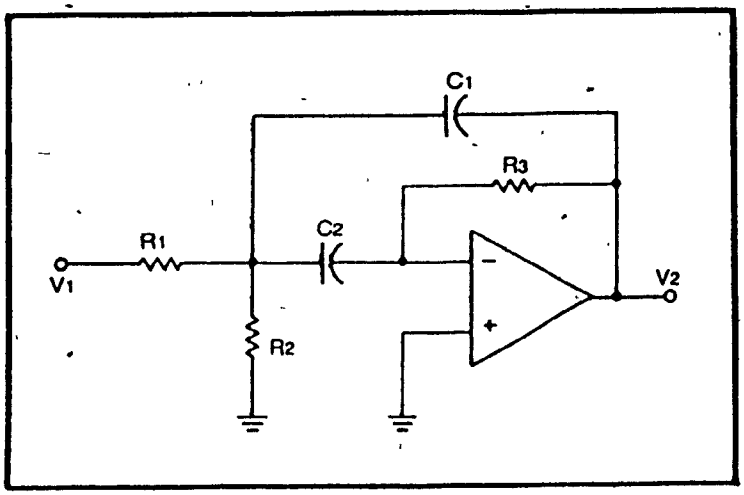
R_p, C_p are practical resistor and capacitor values.

R_n, C_n are normalised resistor and capacitor values [III.D.7.].

APPENDIX VI.B

VI.B.1 Design of a Second Order Bandpass Filter (Multiple Feedback Filter)

The basic circuit



Transfer Function

$$\frac{V_2}{V_1} = \frac{-\frac{Ks}{Q}}{s^2 + \frac{1}{Qs} + 1} \quad \text{or} \qquad \text{(VI.B.1)}$$

where K = gain

Q = quality factor = $\frac{\omega_o}{B}$

where B is the bandwidth and ω_o is normalised to 1 rad/s.

The constants of the transfer function are related to the passive components of the circuit by

$$B = \frac{1}{Q} \frac{(C_1+C_2)G_3}{C_1 G_2} \qquad \text{(VI.B.2)}$$

$$\omega_o^2 = 1 = \frac{G_3(G_1+G_2)}{C_1C_2} \qquad \text{(VI.B.3)}$$

$$K = \frac{G_1C_2}{G_3(C_1+C_2)} \qquad \text{(VI.B.4)}$$

let $C_1 = C_2 = C$ then

$$B = \frac{1}{Q} = \frac{2G_3}{C} \qquad \text{(VI.B.5)}$$

$$\omega_o^2 = 1 = \frac{G_3(G_1+G_2)}{C^2} \qquad \text{(VI.B.6)}$$

$$K = \frac{G_1}{2G_3} \qquad \text{(VI.B.7)}$$

Design Procedure

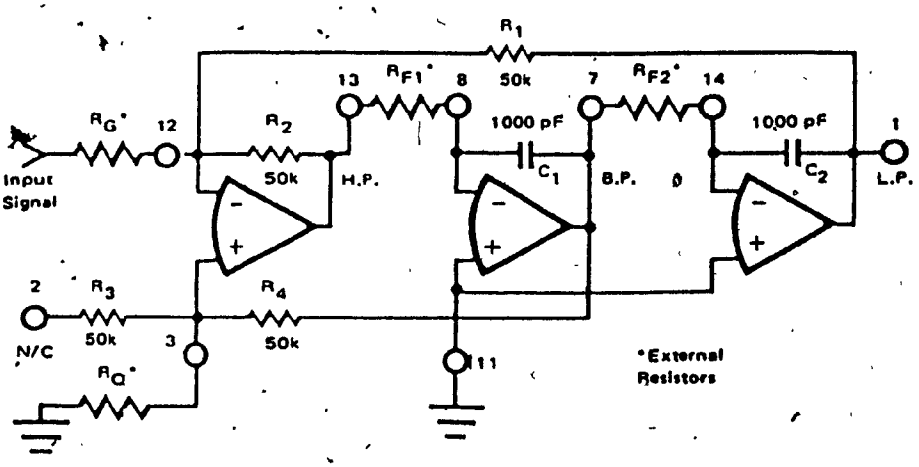
1) Solve for G_1, G_2, G_3

2) Use denormalising method described previously for practical values of R, and C. [III.D.7.].

APPENDIX VI.C

VI.C.1 Design of a Chebyschev Bandpass Fitler Using, a Burr Brown Universal Active Filter, UAF41.

The UAF41 uses a state variable technique; the circuit is shown below for a 2 pole active filter.



Transfer Function

$$T(\text{Bandpass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/(Q)s + \omega_o^2} \qquad \text{(VI.C.1)}$$

Design Procedure

1) Determine normalised lowpass filter parameters (f_n and Q) based on the type of response and the number of poles, and ripple in the passband.

2) Lowpass to bandpass transformation using computer program supplied by Burr Brown.

3) Determine the actual cut off frequency, f_o by multiplying f_n by the actual desired cut off frequency.

4) Use the following equations to determine

$$R_{F1} = R_{F2} = \frac{10^9}{\omega_0} = \frac{1.592 \times 10^8}{f_o} \qquad \text{(VI.C.2)}$$

$$A_{BP} = Q_p A_{LP} = Q_p Q_{HP} \qquad \text{(VI.C.3)}$$

$$R_Q = \frac{5 \times 10^4}{2Q_p + A_{BP} - 1} \qquad \text{(VI.C.4)}$$

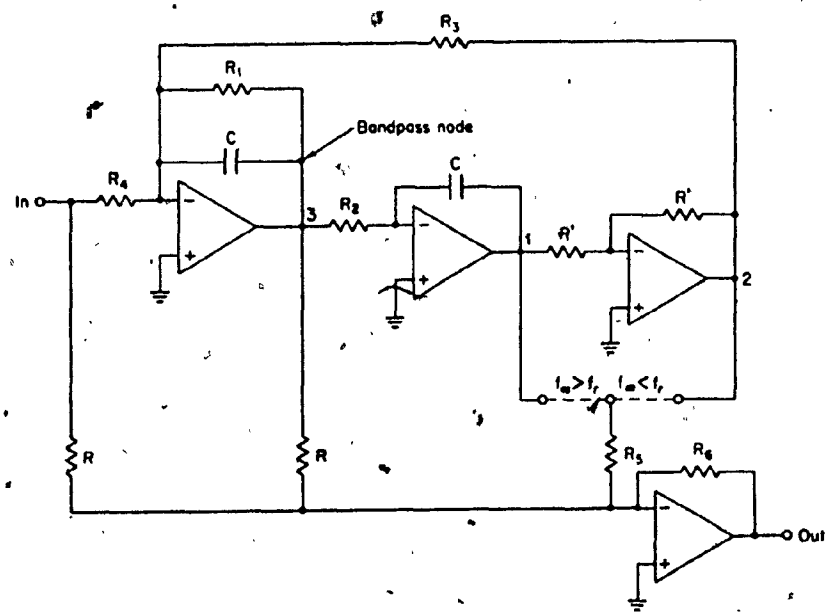
$$R_G = \frac{5 \times 10^4 Q_p}{A_{BP}} \qquad \text{(VI.C.5)}$$

where $Q_p = Q$ and A_{BP} is the gain. [III.C.4].

APPENDIX VI.D

VI.D.1 Design of a Biquad Elliptic-Function Bandpass Filter

The circuit diagram is shown below:



The transfer function for bandpass filter is

$$T(s) = \frac{H(s)}{s^2 + \frac{\omega_\gamma}{Q} + \omega_\gamma^2} \qquad \text{(VI.D.1)}$$

where ω_γ is equal to $2\pi f_\gamma$ the pole frequency in radians per second, Q is the bandpass section and H is a gain constants.

The transfer function for Fig. VI.D.1 is

$$T(s) = -\frac{R_6}{R} \frac{s^2 + \frac{1}{R_2R_3C^2}\left(1 - \frac{R_3R}{R_4R_5}\right)}{s^2 + \frac{1}{R_1C}s + \frac{1}{R_2R_3C^2}} \qquad \text{(VI.D.2)}$$

for notch frequency f_∞ less than resonant frequency f_γ, but when $f_\infty > f_\gamma$ the transfer function is

$$T(s) = -\frac{R_6}{R} \frac{s^2 + \frac{1}{R_2R_3C^2}\left(1 - \frac{R_3R}{R_4R_5}\right)}{s^2 + \frac{1}{R_1C}s + \frac{1}{R_2R_3C^2}} \qquad \text{(VI.D.2)}$$

equating (VI.D.2) with (VI.D.1) we obtain

$$R_1 = R_4 = \frac{Q}{2\pi f_\gamma C} \qquad \text{(VI.D.3)}$$

$$R_2 = R_3 = \frac{R_1}{Q} \qquad \text{(VI.D.4)}$$

$$R_5 = \frac{f_\gamma R}{Q\left|f_\gamma^2 - f_\infty^2\right|} \qquad \text{(VI.D.5)}$$

$$R_6 = \frac{f_\gamma R}{f_\infty^2} \qquad \text{(VI.D.6)}$$

$$R_6 = R \qquad \text{(VI.D.7)}$$

Design Procedure

1) Find the stopband to passband roll off A_s

$$A_s = \frac{\text{STOPBAND}}{\text{PASSBAND}} \qquad \text{(VI.D.8)}$$

2) Select a normalised lowpass filter that makes the same transition from tables.

3) Perform bandpass pole-zero transformation the results of which will indicate the number of sections, their f_γ, Q and f_∞

4) Use equations (VI.D.3) to (VI.D.7) to compute component values. [III.A.1.].