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THE DESIGN OF A SURROUND-SOUND DECODER FOR RESIDENTIAL ENVIRONMENTS

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ABSTRACT

The Design of a Surround-Sound Decoder for Residential Environments

Stephen Kamichik

The reproduction of the spacious acoustics of a live performance in a small listening room is surround sound. A decoder and rear speakers are required for surround sound.

Surround-sound decoders are designed to be used in movie theaters. The residential listening room is much smaller than a movie theater. The surround-sound decoder described in this thesis is designed for residential environments. In the home listening room the front-channel speakers are next to the sound source; therefore, blend circuits and a center monophonic channel for voice reproduction are not necessary.

A rear-channel gain control is incorporated into the system to compensate for the room's absorption characteristic.

The decoder described in this thesis is the first to incorporate a sub-woofer simulator to take advantage of the low-frequency capabilities of the home stereo system. An (L-R) decoder is designed into the system to generate the rear-channel information. An audio time-delay circuit is incorporated into the surround-sound decoder.

The sub-woofer simulator and the (L-R) decoder are active circuits using integrated circuit operational amplifiers. The audio time-delay circuit is designed using digital techniques and is built using integrated circuits. The analog rear-channel signal is fed to an analog-to-digital converter whose eight data output lines are shifted in time by eight 192-stage shift registers. The eight shifted data lines are fed to a digital-to-analog converter yielding a rear-channel signal that is delayed in time. This signal is smoothed by a low-pass active filter. The power supply is designed using three-terminal integrated circuit regulators.

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CHAPTER 1

INTRODUCTION

Surround sound is the reproduction of the spacious acoustics of a live performance in a small listening room. Rear speakers and a decoder are required for surround sound[1][1].

Surround sound in residential environments is possible because of the recent introduction of the stereo television and stereo video cassette recorder. Most households have a stereo system where the left front speaker reproduces the left side of the performance and the right front speaker reproduces the right side of the performance. There are no rear speakers in a stereo system.

Dolby Laboratories invented a system of encoding the rear channel information on the existing stereo channels[1]. A decoder is required to decode the rear channel signal and to feed it to the rear channel amplifier[1]. Most surround-sound decoders are designed for use in the movie theater.

The decoder described in this report is designed for residential environments by the author and the block diagram is shown in figure 1.

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1. Numbers in brackets designate references at the end of the report.

Sound effects such as explosions or thunder contain a lot of information at frequences below 50Hz. Most stereo systems roll-off frequencies less than 30Hz; therefore, very low frequencies must be amplified which requires a sub-woofer simulator to be built into each channel. This enables the existing stereo equipment to reproduce the information at low frequencies.

In the theater, blend circuits are required to add a small amount of the right channel information to the left channel and a small amount of the left channel information to the right channel, reducing front channel separation. Without these blend circuits, only the people sitting in the center seats would get left and right channel information. The people sitting in the extreme left or right seats would receive only the left channel or the right channel information respectively. The home listening room is less than one-fifth the width of a movie theater; hence, the blend circuits are not necessary and have been eliminated from the surround-sound decoder described in this report.

Since the movie theater is a very wide room, a center channel, which is the sum of the left and right channels, is necessary so that speech will appear to emanate from the movie screen. The home listening room is narrow enough so that a center channel is not required; speech will seem to originate from the center of the room because the front channel speakers are close to the television screen.

An audio time-delay circuit of about 20 ms is required to make the sound from the rear channel speakers appear to originate from further back in order to imitate the spacious acoustics of a live performance.

The surround-sound decoder described in this report is affordable and can bring exciting, three-dimensional surround sound into the home.

The surround-sound decoder discussed in this report contains two sub-woofer simulators, one for each front channel. There is an (L-R) decoder to decode precisely the encoded rear-channel information. An audio time-delay circuit has been designed using off-the-shelf components. A 7000 Hz low-pass filter was used to roll-off the high frequencies in the rear channel. A rear-channel gain control was incorporated into the surround-sound decoder. Finally, the power supply for the decoder was designed.

The frequency and phase responses of the sub-woofer simulator and the decoder were measured. Waveforms of various points in the audio time-delay circuit were measured as were output versus input signals at different frequencies. Power supply ripple was also measured.

CHAPTER 2

DESIGN GOALS

Sound effects such as explosions or closing a door contain a lot of low-frequency information[2]. Most stereo systems do not respond to sub-audio frequencies and therefore would benefit from a sub-woofer simulator[2]. A bass boost system is the first design goal.

The most popular surround-sound system is the Dolby Surround System. The rear channel is derived by subtracting the right channel information from the left channel signal. Therefore, an (L-R) decoder is the second design goal.

The third design goal is to maintain the front channel separation. In the movie theater, a small amount of the right channel information is added to the left channel and a small amount of the left channel signal is added to the right channel by blend circuits. This reduces the front left and right channel separation. This is necessary so that the people seated in the extreme left or right seats receive right and left channel information. The home listening room is less than 20 feet wide and hence no blend circuits are required. This eliminates the need for steering circuits to enhance the front channel separation[3]. A steering circuit is an adaptive matrix stage used to provide high-separation outputs[4].

Frequencies less than 700 Hz are not blocked by the human head because the distance between the human ears is half a wavelength or less[5]. These frequencies are localized by the phase difference between the human ears[5].

In the range of 700 Hz to 5000 Hz the directional behavior of the energy field around the listener is important. The head is an obstacle because the wavelength in this frequency range is less than the diameter of the human head[5]. Head movement is used by the brain to estimate the probable subjective mid- and high-frequency sound direction[5].

Sounds of frequencies above 5000 Hz are localized by the pinnae or flaps of the ears which modify sounds from different directions[5]. The pinnae's acoustic obstruction gives good spatial localization[5]. The pinnae localization mechanism appears to rely on the fact that sound from each direction arrive inside the listener's ear with a distinctive colouration[5]. The fourth design goal is to roll-off the high frequencies of the rear channel. The Dolby standard of 7000 Hz is used.

The average listening room is about 12 feet wide with the speakers placed on either side of the stereo television. Speech will therefore appear to emanate from the television[3]. An (L+P) or monophonic center channel is not required in this system. A rear channel gain control is also incorporated into the design.

The 20 ms time delay allows the rear speakers to be placed near the seating, while the sound appears to originate from about 20 feet further back to imitate the spacious acoustics of a live performance[6],[7].

In the surround-sound decoder designed for the movie theater, very complex circuits are used for the audio time-delay line, most of which involve custom-designed integrated circuits. The audio time-delay circuit of the decoder designed in this report uses readily available integrated circuits and it is inexpensive enough to be incorporated into a surround-sound decoder designed for the home. An audio-delay circuit generates noise and distortion[6]. The rear speakers may be placed above the listeners' heads to compensate for the lack of an audio time-delay circuit[6].

High fidelity is one of the design goals. Therefore, the audio time-delay circuit included in the design is optional.

A noise reduction system is not included in this system. A power supply included in the system is also discussed in this report.

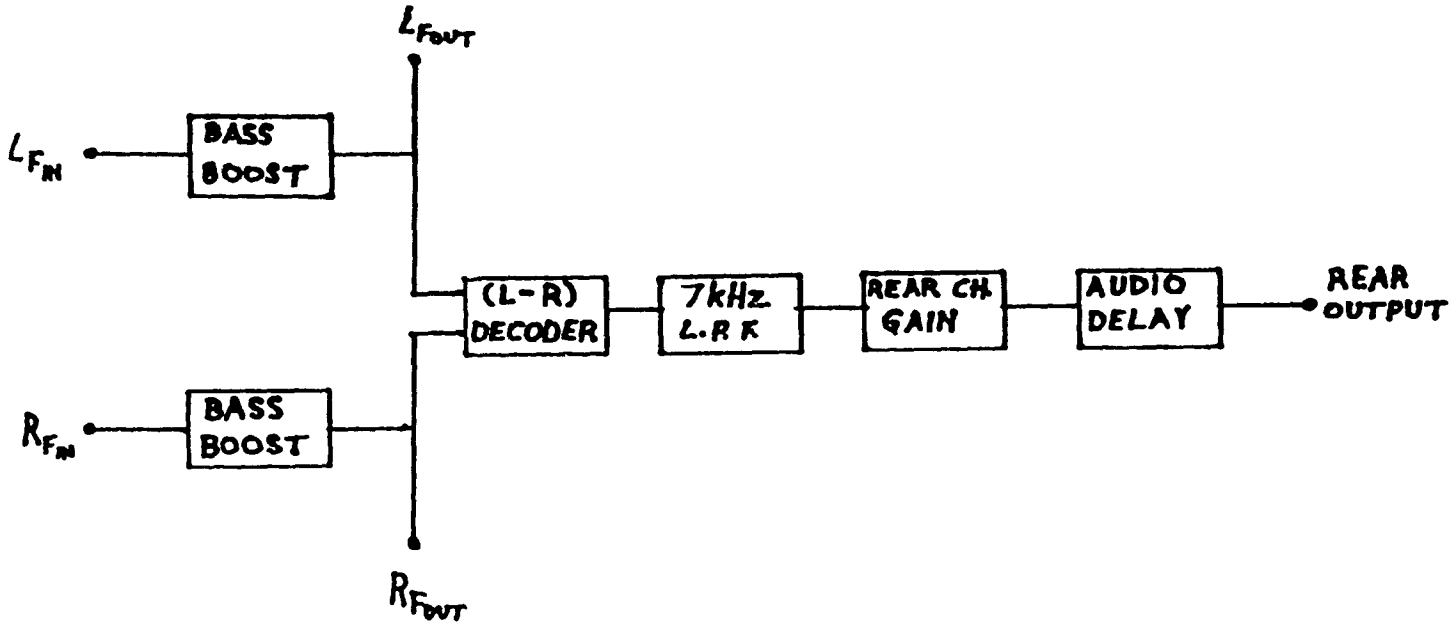


Figure 1 Block Diagram of Surround-Sound Decoder

CHAPTER 3

THE OPERATIONAL AMPLIFIER

The surround-sound decoder must operate in the audio range and the sub-woofer simulator operates in the low and sub-audio range. At frequencies lower than 1000 Hz inductors become bulky and expensive[8]. Passive circuits usually require inductors, while active circuits can emulate most transfer functions using ony resistors and capacitors as the feedback components[8].

The operational amplifier has a high input impedance and a low output impedance and therefore operational-amplifier stages may be cascaded directly[8]. Active circuits require power supplies[8]. Active circuits are more sensitive to component value changes than passive circuits due to heat and age[8]. Active circuits can be unstable if not properly designed[8].

The operational amplifier is used in the system discussed here because the range of frequency operation is low, that is, in the audio range[9]. The various stages can be directly cascaded without buffer amplifiers.

Active circuits require inexpensive components and their responses are independent of source and load impedances[10]. Active circuits can provide gain or attenuation and they may be tuned as well[10].

3.1 Operational-Amplifier Model

The operational amplifier has two inputs and one output[11]. The output voltage is the difference of the two input signals multiplied by the gain of the operational amplifier[11]. Figure 2 is a block diagram of the operational amplifier, where $V_2(t) = A[V_+(t)-V_-(t)]$ (1)

When the input voltages have the same noise, the noise cancels in forming the output signal; this is known as common-mode signals[11]. If the input signals are different, then each is multiplied by the gain of the amplifier; such signals are called differential-mode signals[11].

A model of the operational amplifier is shown in Figure 3. Typical values for the operational amplifier input and output impedances, gain and input voltages are shown in Figure 3. For the purpose of analysis the following assumptions are made: $A = \infty$, $R_i = \infty$ and $R_o = 0$ which also implies that $V_+ = V_-$ and $i_+ = i_- = 0$[11].

Linear operation of an operational amplifier requires the input voltage to be: $| V_+ - V_- | < V_{CC}/A$[11]. Figure 4 is the idealized input-output operational-amplifier characteristic.

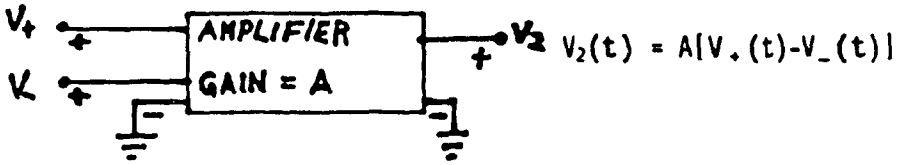


Figure 2 Block Diagram of Operational Amplifier[11]

A = 100000

R_i = 100kΩ

R_O = 100Ω

| V+-V- | < 1 mV

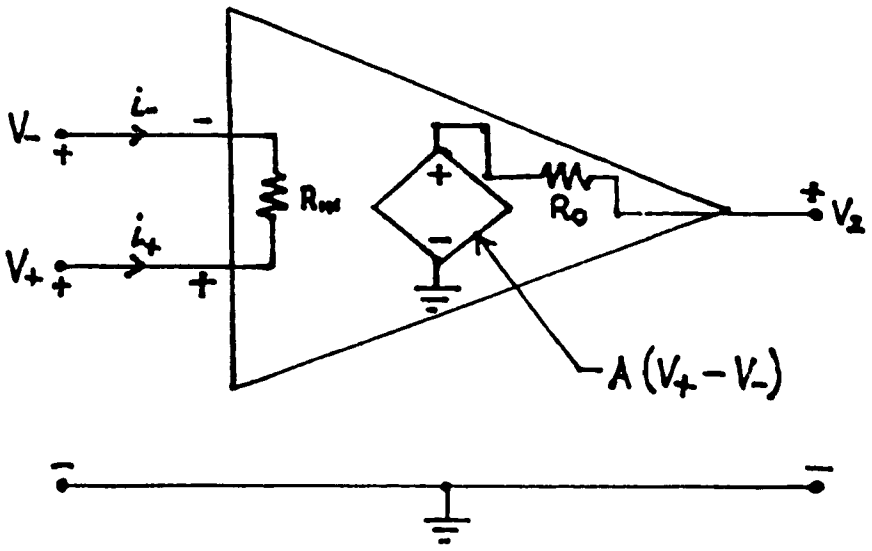


Figure 3 Operational - Amplifier Model[11]

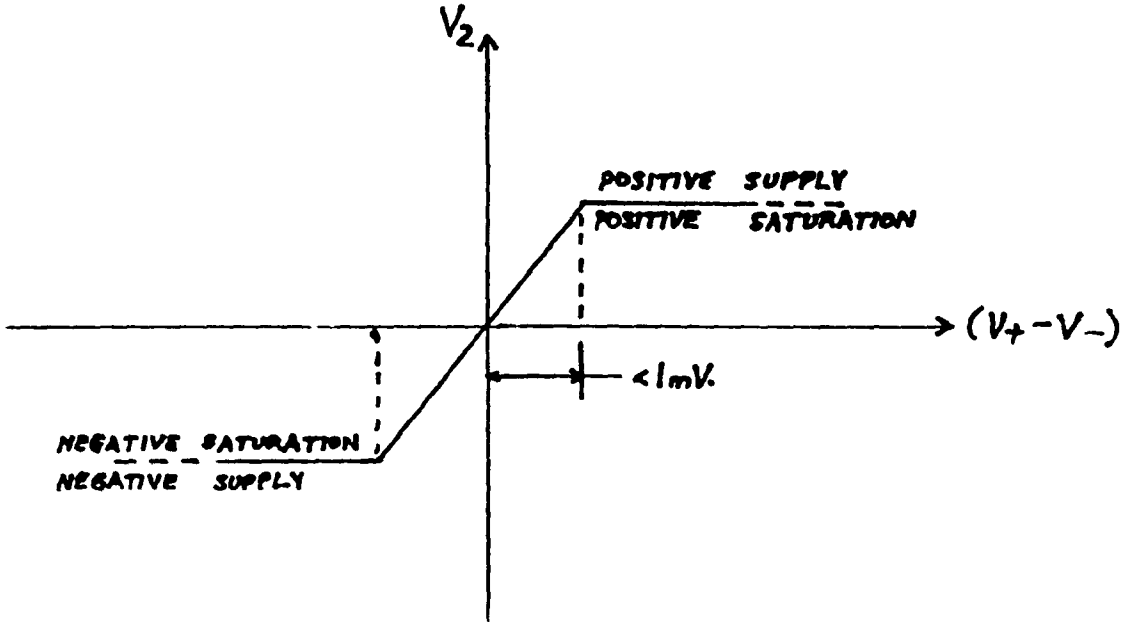


Figure 4 Operational Amplifier Input-Output Characteristic[11]

3.2 Choosing an Operational Amplifier

The important operational-amplifier specifications for the surround-sound decoder are: slew rate, unity-gain bandwidth, CMRR, supply-voltage rejection ratio and noise level.

The slew rate is the time for an amplifier's output to respond to an input signal[12]. Slew rate is critical in high speed and low distortion circuits[12].

Unity-gain bandwidth specifies the highest frequency that an amplifier will pass at a gain of unity without attenuation in the amplification process[12].

CMRR or common-mode rejection ratio is the ability of an operational amplifier to cancel out, within the device, common signals fed to the inverting and the non-inverting inputs[12].

The supply voltage rejection ratio is the ability of an operational amplifier to prevent power supply fluctuations from showing up in the output signal[12].

Low noise is essential in high quality audio and video circuits[12]. The 4136 quad operational amplifier was selected. It appeared to be the best compromise as shown in Table 1. The 4136 is a quad operational amplifier; therefore, more functions may be handled, in a smaller area and at lower cost than with single-amplifier integrated circuits[12].

Table 1 Typical Specifications for Operational Amplifiers[12]

	741	1458 (qual)	LM324 (quad)	LM301	LM308	LM318	TL071	LM351	AD712 (dual)	NE5534	4136 (quad)	OP.42E
Input Impedance (ohms)	2M2	1M	4M	2M	40M	3M	10^{12}	10^{12}	10^{12}	100k	5M	10^{12}
Slew Rate (V/μs)	0.5	0.5	0.5	0.5	0.3	50	13	13	13	13	1	50
Unity Gain Bandwidth (Hz)	1.5M	1M	1M	1M	1M	15M	3M	4M	3M	10M	3M	10M
CMRR (dB)	90	90	70	70	100	100	86	100	66	100	90	98
PSR (dB)	96	96	100	96	96	80	86	100	86	10	30μV/V	9
Offset Voltage (mV)	2	1	2	2	2	4	3	10	0.25	0.5	10	0.4
Noise Voltage (nV/√Hz)	*	*	*	*	60	15	18	16	18	4	10	13
Average Quiescent Current (mA)	1.7	3.0	1.5	18	0.3	5	1.4	1.8	5	4	7	5.1

* Accurate noise data not available

CHAPTER 4

SUB-WOOFER SIMULATOR

The sub-woofer simulator boosts the low-frequency response of the system. It consists of an input amplifier, a low-pass filter and a summing amplifier, as shown in Figure 5. The input amplifier boosts frequencies lower than 100 Hz and provides unity gain at frequencies above 1000 Hz. The low-pass filter rolls-off frequencies greater than 7 KHz. The input amplifier and the summing amplifier invert their input signals. Therefore, the sub-woofer simulator output voltage is in phase with its input signal.

4.1 Input Amplifier

The schematic of the input amplifier is shown in Figure 6. Capacitor C_1 is a coupling capacitor and is used to block direct current signals from entering the sub-woofer simulator.

At very low frequencies, C_1 and C_2 act as open-circuits. The gain of the input amplifier becomes much less than unity. At very high frequencies, C_1 and C_2 act as short-circuits. The gain of the input amplifier is unity at higher frequencies.

The input amplifier may be redrawn for the purpose of analysis as shown in Figure 7.

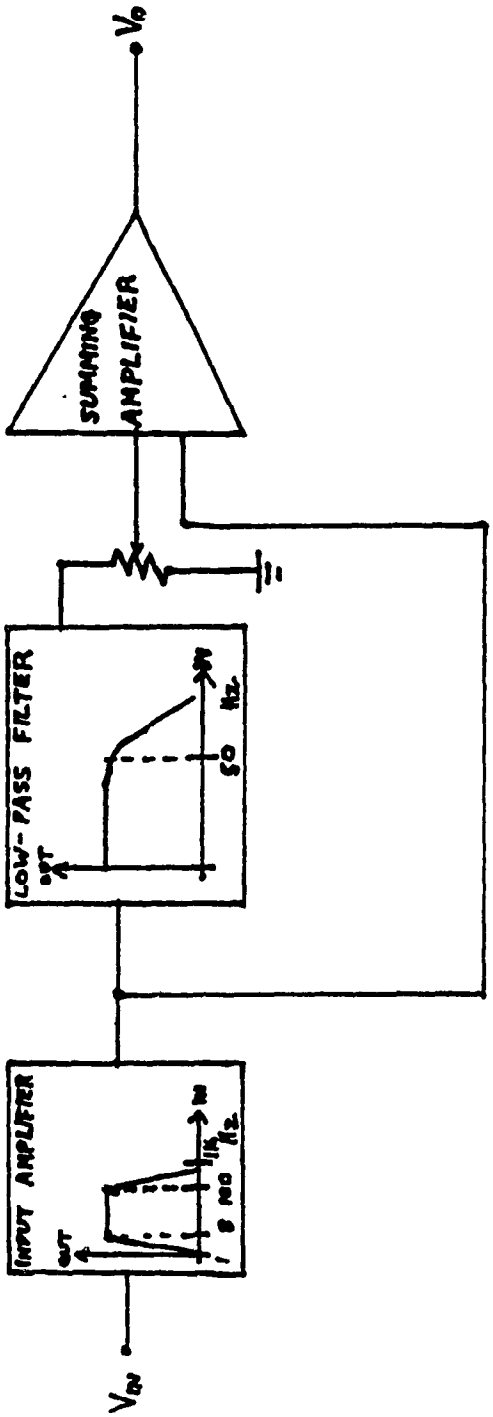
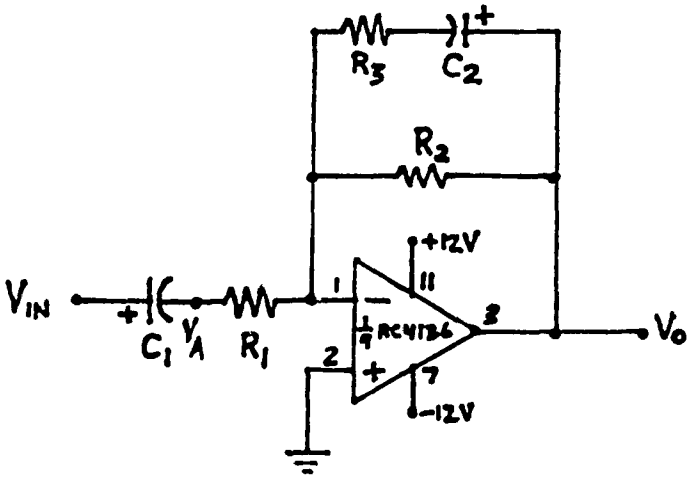


Figure 5 Block Diagram of Sub-Woofer Simulator[2]



R_1 = 47kΩ
R_2 = 270kΩ
R_3 = 56kΩ
C_1 = 1.0μF
C_2 = 0.047μF

Figure 6 Schematic of Input Amplifier

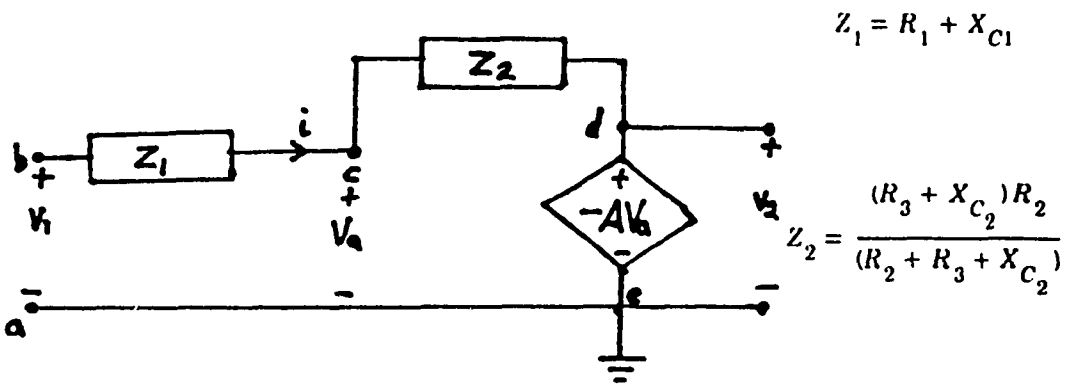


Figure 7 Input Amplifier Representation[13]

Using KVL around path abcde [13],

$$V_1 = iZ_1 + iZ_2 + V_2 \tag{2}$$

Solving for i,

$$i = \frac{(V_1 - V_2)}{(Z_1 + Z_2)} \tag{3}$$

Using KVL around path abca [13],

$$V_1 = iZ_1 + Va \quad (4) \text{ or}$$
$$Va = V_1 - iZ_1 \quad (5)$$

Substituting equation (3) into equation (5),

$$Va = iZ_1 + iZ_2 + V_2 - iZ_1 = i(Z_1 + Z_2 - Z_1) + V_2 = iZ_2 + V_2$$

$$Va = \frac{(V_1 - V_2)Z_2}{(Z_1 + Z_2)} + V_2 = \frac{(V_1Z_2 - V_2Z_2)}{(Z_1 + Z_2)} + \frac{V_2(Z_1+Z_2)}{(Z_1+Z_2)}$$

$$Va = \frac{V_1Z_2 + V_2Z_1}{(Z_1 + Z_2)} = \frac{Z_2}{(Z_1 + Z_2)} V_1 + \frac{Z_2}{(Z_1 + Z_2)} V_2 \tag{6}$$

From equation (1) and this circuit configuration of the operational amplifier:

$$V_2 = -AV_a \tag{7}$$

Equation (6) may be rewritten as [13],

$$-\frac{V_2}{A} = \frac{Z_2}{(Z_1 + Z_2)} V_1 + \frac{Z_1}{(Z_1 + Z_2)} V_2 \tag{8}$$

$$V_2 = \frac{-AZ_2}{(Z_1 + Z_2)} V_1 - \frac{AZ_1}{(Z_1 + Z_2)} V_2$$

$$\frac{V_2}{V_1} = \frac{-AZ_2}{(Z_1 + Z_2)} - \frac{AZ_1}{(Z_1 + Z_1)} \frac{V_2}{V_1}$$

$$\frac{V_2}{V_1}\left[1+\frac{AZ_1}{(Z_1+Z_2)}\right]=\frac{-AZ_2}{(Z_1+Z_2)}$$

$$\frac{V_2}{V_1}=\frac{-AZ_2/(Z_1+Z_2)}{\left[1+\frac{AZ_1}{(Z_1+Z_2)}\right]} \tag{9}$$

$$\frac{V_2}{V_1}=\frac{-AZ_2/(Z_1+Z_2)}{\left[(Z_1+Z_2)+A_{Z_1}\right]/(Z_1+Z_1)}=\frac{-AZ_2}{(Z_1+Z_2)+AZ_1}=\frac{-Z_2}{\frac{(Z_1+Z_2)}{A}+Z_1}$$

$$\frac{V_2}{V_1}=\frac{-Z_2/Z_1}{1+\frac{(Z_1+Z_2)}{AZ_1}}=\frac{-Z_2/Z_1}{\left[1+\frac{1}{AZ_1/(Z_1+Z_2)}\right]} \tag{10}$$

$$\frac{V_2}{V_1}\Bigg|_{A\to\infty}=\frac{-Z_2}{Z_1}$$

Substituting for Z_1 and Z_2,

$$\frac{V_2}{V_1}=\frac{\frac{-R_2(R_3+X_{C_2})}{(R_2+R_3+X_{C_2})}}{(R_1+XC_1)}=\frac{\frac{(-R_2R_3-R_2X_{C_2})}{(R_2+R_2+X_{C_2})}}{(R_1+X_{C_1})}$$

$$\frac{V_2}{V_1}=\frac{(-R_2R_3-R_2X_{C_2})}{(R_2+R_3X_{C_2})(R_1+X_{C_1})}=\frac{(-R_2R_3-R_2X_{C_2})}{(R_1R_2+R_1R_3+R_1X_{C_2}+R_2X_{C_1}+R_3X_{C_1}+X_{C_2}X_{C_1})} \tag{11}$$

At frequencies exceeding 1000 Hz or so, capacitors C_1 and C_2 approach a short circuit, hence,

$$\frac{V_2}{V_1}=-\frac{R_2R_3/(R_2+R_3)}{R_1} \tag{12}$$

4.1.1 Sensitivity of Input Amplifier

From equation (9),

$$\frac{V_2}{V_1} = T = \frac{-AZ_2}{(Z_1 + Z_2 + AZ_1)} \tag{13}$$

For frequencies above 1000 Hz,

$$Z_1 \doteq R_1 \; and, Z_2 \doteq \frac{R_2 R_3}{(R_2 + R_3)} \tag{14}$$

$$Let\ Z_2 \doteq \frac{R_2 R_3}{(R_2 + R_3)} = R_2^{'} \tag{15}$$

$$T = \frac{-AR_2^{'}}{\left| R_1 + R_2^{'} + AR_1 \right|} \tag{16}$$

Therefore from equation (13),

$$S_{R_1}^T = \frac{R_1}{T} \cdot \frac{\partial T}{\partial R_1} = \frac{R_1(R_1 + R_2^{'} + AR_1)}{-AR_2^{'}} \cdot \frac{(R_1 + R_2^{'} + AR_1)(0) + AR_2^{'}(1 + A)}{\left| R_1 + R_2^{'} + AR_1 \right|^2}$$

$$S_{R_1}^T = \frac{AR_2^{'}R_1(1 + A)}{-AR_2^{'}(R_1 + R_2^{1} + AR_1)} = \frac{R_1(1 + A)}{-(R_1 + R_2^{'} + AR_1)} = \frac{-R_1(1 + A)}{(R_1 + R_2^{'} + AR_1)}$$

$$Lim\ A \to \infty \quad S_{R_1}^T \to -1$$

$$S_A^T = \frac{A}{T} \cdot \frac{\partial T}{\partial A} = \frac{A(R_1 + R_2^{'} + AR_1)}{-AR_2^{'}} \cdot \frac{(R_1 + R_2^{'} + AR_1)(-R_2^{'}) + AR_2^{'}R_1}{(R_1 + R_2^{'} + AR_1)^2}$$

$$S_A^T = \frac{A\left|(R_1 + R_2^{'} + AR_1)(-R_2^{'}) + AR_2^{'}R_1\right|}{-AR_2^{'}(R_1 + R_2^{'} + AR_1)} = \frac{(R_1 + R_2^{'} + AR_1 - AR_1}{(R_1 + R_2^{'} + AR_1)} = \frac{(R_1 + R_2^{'})}{(R_1 + R_2^{'} + AR_1)}$$

$$Lim\ A \to \infty \quad S_A^T \to 0$$

$$S^{T}_{R_2'} = \frac{R_2'}{T} \cdot \frac{\partial T}{\partial R_2'} = \frac{R_2'(R_1+R_2'+AR_1)}{-AR_2'} \cdot \frac{(R_1+R_2'+AR_1)(-A)+AR_2'(1)}{(R_1+R_2'+AR_1)^2}$$

$$S^{T}_{R_2'} = \frac{R_2'}{-AR_2'} \cdot \frac{(-AR_1-AR_2'-A^2R_1+AR_2')}{(R_1+R_2'+AR_1)} = \frac{(-AR_1-A^2R_1)}{(R_1+R_2'+AR_1)} \cdot \frac{-1}{A}$$

$$S^{T}_{R_2'} = \frac{(R_1+AR_1)}{(R_1+R_2'+AR_1)}$$

$$Lim\ A \to \infty \quad S^{T}_{R_2'} \to 1$$

For frequencies below 100 Hz

$$\frac{V_2}{V_1}\Big|_{A\to\infty} = \frac{-Z_2}{Z_1}$$

Since

$$Z_1 = (R_1 + \frac{1}{C_1S}) = \frac{(R_1C_1S+1)}{C_1S} \tag{17}$$

and

$$Z_2 = \frac{R_2(R_3+\frac{1}{C_2S})}{(R_2+R_3+\frac{1}{C_2S})} = \frac{\frac{(R_2R_3C_2S+R_2)}{C_2S}}{\frac{(R_2C_2S+R_3C_2S+1)}{C_2S}} = \frac{(R_2R_3C_2S+R_2)}{(R_2C_2S+R_3C_2S+1)} \tag{18}$$

The transfer function can be written as

$$\frac{V_2}{V_1} = \frac{-\frac{(R_2R_3C_2S+R_2)}{(R_2C_2S+R_3C_2S+1)}}{(R_1C_1S+1)/C_1S} = -\frac{(R_2R_3C_2S+R_2)C_1S}{(R_1C_1S+1)(R_2C_2S+R_3C_2S+1)}$$

$$\frac{V_2}{V_1} = \frac{(-R_2R_3C_1C_2S^2-R_2C_1S)}{(R_1R_2C_1C_2S^2+R_1R_3C_1C_2S^2+R_1C_1S+R_2C_2S+R_3C_2S+1)}$$

$$\frac{V_2}{V_1} = \frac{(-R_2R_3C_1C_2S^2-R_2C_1S)}{(R_1R_2C_1C_2+R_1R_3C_1C_2)S^2+(R_1C_1+R_2C_2+R_3C_2)S+1)} \tag{19}$$

Let $$X = \left| (R_1R_2C_1C_2 + R_1R_3C_1C_2)S^2 + (R_1C_1 + R_2C_2 + R_3C_2)S + 1 \right|$$

Therefore

$$S^T_{R_1} = \frac{R_1}{T} \cdot \frac{\partial T}{\partial R_1} = \frac{R_1 X}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} \cdot \frac{(R_2R_3C_1C_2S^2 + R_2C_1S)(R_2C_1C_2S^2 + R_3C_1C_2S^2 + C_1S)}{X^2}$$

$$S^T_{R_1} = \frac{(-R_1R_2C_1C_2S^2 - R_1R_3C_1C_2S^2 - R_1C_1S)}{(R_1R_2C_1C_2 + R_1R_3C_1C_2)S^2 + (R_1C_1 + R_2C_2 + R_3C_2)S + 1} \doteq -1$$

$$S^T_{R_2} = \frac{R_2}{T} \cdot \frac{\partial T}{2\partial R_2} = \frac{R_2 X}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} \cdot \frac{X(-R_3C_1C_2S^2 - C_1S) + (R_2R_3C_1C_2S^2 + R_2C_1S)(R_1C_1C_2S^2 + C_2S)}{X^2}$$

$$S^T_{R_2} = \frac{R_2(-R_3C_1C_2S^2 - C_1S)}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} + \frac{-R_2(R_1C_1C_2S^2 + C_2S)}{X}$$

$$S^T_{R_2} = \frac{(-R_2R_3C_1C_2S^2 - R_2C_1S)}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} - \frac{(R_1R_2C_1C_2S^2 + R_2C_2S)}{(R_1R_2C_1C_2 + R_1R_3C_1C_2)S^2 + (R_1C_1 + R_2C_2 + R_3C_2)S + 1}$$

$$S^T_{R_2} = 1 - \frac{(R_1R_2C_1C_2S^2 + R_2C_2S)}{(R_1R_2C_1C_2 + R_1R_3C_1C_2)S^2 + (R_1C_1 + R_2C_2 + R_3C_2)S + 1} \doteq 0.17$$

$$S^T_{R_3} = \frac{R_3}{T} \cdot \frac{\partial T}{\partial R_3} = \frac{R_3 X}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} \cdot \frac{X(-R_2C_1C_2S^2) + (R_2R_3C_1C_2S^2 + R_2C_1S)(R_1C_1C_2S^2 + C_2S)}{X^2}$$

$$S^T_{R_3} = \frac{R_3\left| X(-R_2C_1C_2S^2) + (R_2R_3C_1C_2S^2 + R_2C_1S)(R_1C_1C_2S^2 + C_2S) \right|}{X(-R_2R_3C_1C_2S^2 - R_2C_1S)}$$

$$S^T_{R_3} = \frac{R_3(-R_2C_1C_2S^2)}{(-R_2R_3C_1C_2S^2 - R_1C_1S)} - \frac{R_3(R_1C_1C_2S^2 + C_2S)}{X}$$

$$S^T_{R_3} = \frac{R_2R_3C_1C_2S^2}{(R_2R_3C_1C_2S^2 + R_1C_1S)} - \frac{(R_1R_3C_1C_2S^2 + R_3C_2S)}{(R_1R_2C_1C_2 + R_1R_3C_1C_2)S^2 + (R_1C_1 + R_2C_2 + R_3C_2)S + 1} \doteq 0.83$$

$$S_{C_1}^T = \frac{C_1}{T} \cdot \frac{\partial T}{\partial C_1} = \frac{C_1 X}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} \cdot \frac{X(-R_2S) + (R_2R_3C_1C_2S^2 + R_2C_1S)(R_1R_2C_2S^2 + R_1R_3C_2S^2 + R_1S)}{X^2}$$

$$S_{C_1}^T = \frac{-C_1R_2S}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} + \frac{-C_1(R_1R_2C_2S^2 + R_1R_3C_2S^2 + R_1S)}{X}$$

$$S_{C_1}^T = \frac{C_1R_2S}{(R_2R_3C_1C_2S^2 + R_2C_1S)} - \frac{(R_1R_2C_1C_2S^2 + R_1R_3C_1C_2S^2 + R_1C_1S)}{(R_1R_2C_1C_2 + R_1R_3C_1C_2)S^2 + (R_1C_1 + R_2C_2 + R_3C_2)S + 1} \doteq -1$$

$$S_{C_2}^T = \frac{C_2}{T} \cdot \frac{\partial T}{\partial C_2} = \frac{C_2X}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} \cdot$$

$$\frac{X(-R_2R_3C_1S^2) + (R_2R_3C_1C_2S^2 + R_2C_1S)(R_1R_2C_1S^2 + R_1R_2C_1S^2 + R_2S + R_3S)}{X^2}$$

$$S_{C_2}^T = \frac{C_2(-R_2R_3C_1S^2)}{(-R_2R_3C_1C_2S^2 - R_1C_1S)} + \frac{C_2(R_2R_3C_1C_2S^2 + R_2C_1S)(R_1R_2C_1S^2 + R_1R_3C_1S^2 + R_2S + R_3S)}{X}$$

$$S_{C_2}^T = \frac{C_2(-R_2R_3C_1S^2)}{(-R_2R_3C_1C_2S^2 - R_2C_1S)} + \frac{-C_2(R_1R_2C_1S^2 + R_1R_3C_1S^2 + R_2S + R_3S)}{X}$$

$$S_{C_2}^T = \frac{R_2R_3C_1C_2S^2}{(R_2R_3C_1C_2S^2 + R_2C_1S)} - \frac{(R_1R_2C_1C_2S^2 + R_1R_3C_1C_2S^2 + R_2C_2S + R_3C_2S)}{(R_1R_2C_1C_2 + R_1R_3C_1C_2)S^2 + (R_1C_1 + R_2C_2 + R_3C_2)S + 1} \doteq 0$$

4.1.2 Input-Amplifier Design and Performance

The coupling capacitor, C_1, of Figure 5 rolls-off the low frequency response of the input amplifier in order to block any input direct current voltages. R_1 is selected arbitrarily as 47000Ω. Capacitor C_1 is selected for a response of -3dB at eight hertz, that is, 0.7071 of V_{IN} appears at V_A, refer to Figure 6. Hence,

$$\frac{R_1}{(X_{C_1} + R_1)} = 0.7071. \tag{20}$$

$$0.7071 = \frac{47\,000}{X_{C_1} + 47\,000} \; which\, yields \, X_{C_1} = 19\,468\,\Omega$$

$$X_C = \frac{1}{2\Pi fC} \tag{21}$$

$$19\,468 = \frac{1}{6.283 \times 8 \times C_1} = \frac{1}{50.264\,C_1}$$

$$1 = 978\,540\,C_1$$

$$C_1 = \frac{1}{978\,540} = 1.0 uF$$

Resistor R_3 is arbitrarily selected as 56,000Ω. R_2 is chosen, so that, at frequencies above 1000 Hz, when C_2 approaches a short circuit, the gain of the input amplifier is unity;

$$\frac{R_2 R_3}{(R_2 + R_3)} = R_1 = 47000\,\Omega \tag{22}$$

$$\frac{56000\,R_2}{56000 + R_2} = 47000$$

$$56\,000\,R_2 = 2.632 \times 10^9 + 47\,000\,R_2$$

$$9\,000\,R_2 = 2.632 \times 10^6$$

$$R_2 = \frac{2632 \times 10^6}{9\,000} = 292444\Omega$$

$$R_2 = 270\,000\Omega \text{ (nearest standard value)}$$

Table 2 lists the design and actual performance of the input amplifier stage. Figure 8 is the frequency-response plots of the input amplifiers. The discrepancy between the left and right channel performance data is due to component tolerances.

4.2 Low-Pass Filter (with fc = 50 Hz)

The Sallen and Key low-pass filter, as shown in Figure 9 was selected because it has good sensitivity characteristics. There are several designs possible with this circuit[14]. The equal component design was chosen. The gain of the circuit is determined by R_A and R_B in the noninverting operational amplifier circuit[14]. Figure 10 is the controlled-source model.

Table 2 Input-Amplifier Performance Data

Freq. (Hz)	Design Values						Actual Values						
	X_{C1} (Ω)	$(R_1 + X_{C1})$ (kΩ)	X_{C2} (Ω)	Rf* (kΩ)	G**	20logG (dB)	V_{1N} (Vp-p)	$V^{\dagger}_{0L}$ (Vp-p)	$V^{\dagger\dagger}_{0R}$ (Vp-p)	$G^{\ddagger}_{L}$	$G^{\ddagger\ddagger}_{R}$	20logG_L (dB)	20logG_R (dB)
1	159K	208K	3.4M	251K	-1.2	1.58	1.0	1.2	1.2	-1.20	-1.20	1.58	1.58
2	79.6K	126.6K	1.7M	240K	-1.9	5.56	1.0	2.0	2.0	-2.00	-2.00	6.02	6.02
5	32K	79K	677K	198K	-2.5	7.96	2.0	5.0	5.0	-2.50	-2.50	7.96	7.96
10	16K	63K	339K	160K	-2.55	8.13	2.0	6.4	7.2	-3.20	-3.60	10.10	11.13
20	8K	55K	169.3K	122.8K	-2.23	6.98	2.0	4 6	5.2	-2.30	-2.60	7.23	8.30
30	5.3K	52.3K	113K	104K	-1.99	5.98	2.0	3.8	3.9	-1.90	-1.95	5.58	5.80
40	4K	51K	84.7K	92.5K	-1.81	5.17	2.0	3.2	3.6	-1.60	-1.80	4.08	5.11
50	3.2K	50.2K	67.7K	84.8K	-1.69	4.56	2.0	3.0	3.2	-1.50	-1.60	3.52	4.08
60	2.7K	49.7K	56K	79K	-1.59	4.03	2.0	2.7	2.9	-1.35	-1.45	2.61	3.23
80	2K	49K	42.3K	72K	-1.47	3.35	2 0	2.5	2.6	-1.25	-1.30	1.94	2.28
100	1.6K	48.6K	34K	67.5K	-1.39	2 86	2.0	2.4	2.5	-1.20	-1.25	1.58	1.94
500	317	47.317K	6.67K	50.9K	-1.07	0.63	2.0	2.1	2.1	-1.05	-1.05	0.42	0.42
1,000	160	47.16K	3.4K	48.7K	-1.04	0.34	2.0	2.0	2.0	-1.00	-1.00	0.00	0.00
5,000	32	47.032K	667	46.8K	-1.00	0.00	2.0	2.0	2.0	-1.00	-1.00	0.00	0.00
10,000	16	47.016K	339	46.6K	-0.99	-0.09	2.0	2.0	2.0	-1.00	-1.00	0.00	0.00

† V_{OL} is left channel output voltage.
‡† V_{OR} is right channel output voltage.
‡ G_L is left channel gain.
‡‡ G_R is right channel gain.

N.B.: G_L and G_R negative sign indicates 180° phase shift

$$* R_f = \frac{R_2(R_3 + X_{C_2})}{(R_2 + R_3 + X_{C_2})}$$

$$** G = \frac{-(R_2R_3 + R_2X_{C_2})}{(R_2+R_3+X_{C_2})(R_1+X_{C_2})}$$

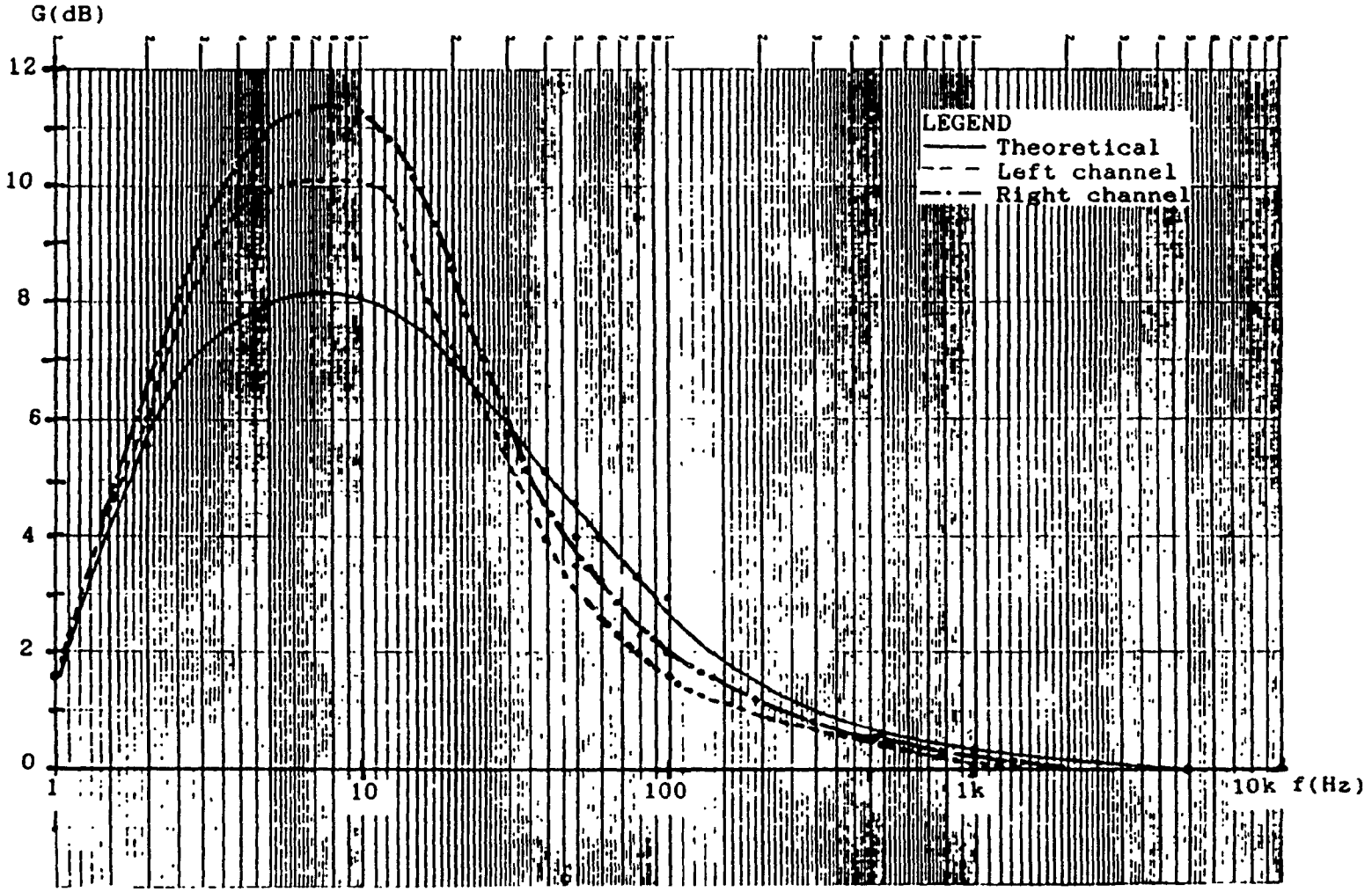


Figure 8 Frequency-Response Plots of Input Stages

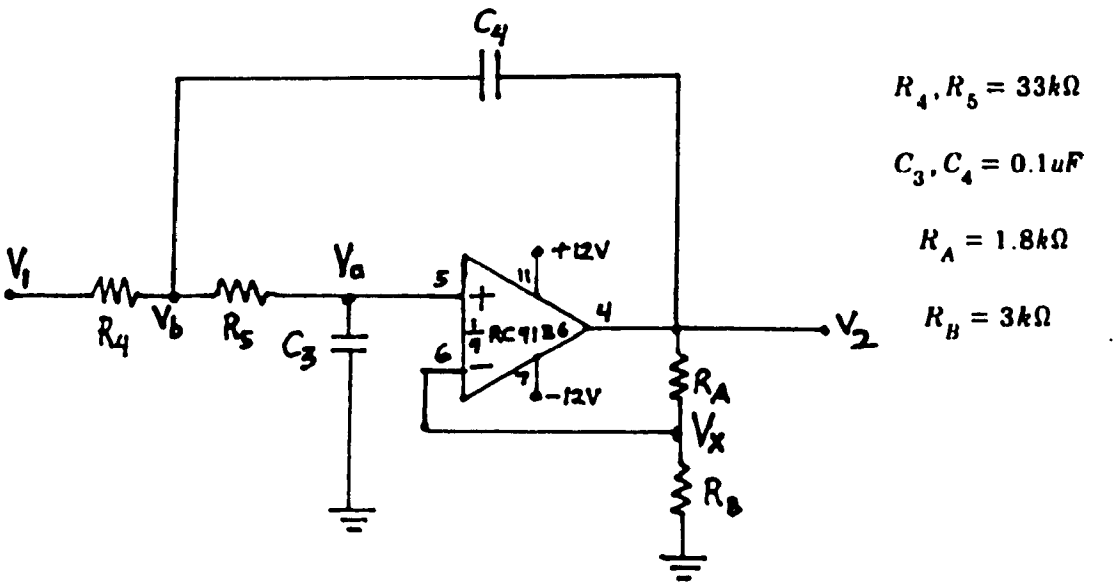


Figure 9 Schematic of Low-Pass Filter (f_c = 50 Hz)

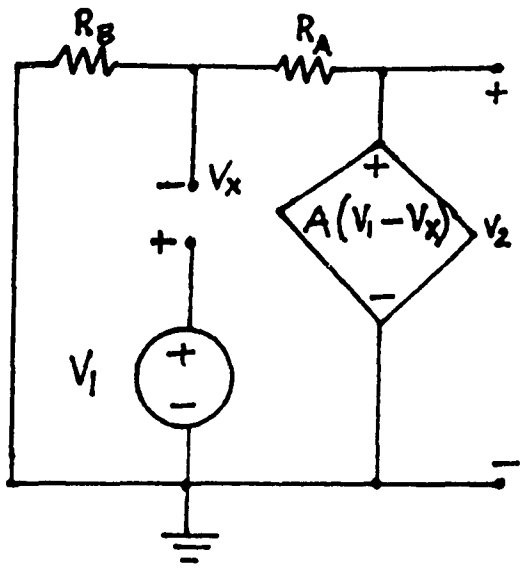


Figure 10 Noninverting Amplifier Model [15]

$$V_2 = A(V_+ - V_-) \tag{1}$$

Comparing Figure 3 and Figure 10, it is evident that

$$V_- = V_X \text{ and } V_+ = V_1 \tag{23}$$

Substituting (23) into (1) :

$$V_2 = A(V_1 - V_x) \tag{24}$$

From Figure 10,

$$V_x = \frac{R_B}{(R_A + R_B)} V_2 \tag{25}$$

Substituting (25) into (24):

$$V_2 = A\left\{ V_1 - \frac{R_B}{(R_A + R_B)} V_2 \right\} = AV_1 - \frac{AR_B V_2}{(R_A + R_B)} \tag{26}$$

Equation (26) may be rearranged:

$$V_2 + \frac{AR_B}{(R_A + R_B)} V_2 = AV_1 = V_2 \left\{ 1 + \frac{AR_B}{(R_A + R_B)} \right\}$$

$$\frac{V_2}{V_1} = \frac{A}{\left\{ 1 + \frac{AR_B}{(R_A + R_B)} \right\}} = \frac{1}{\frac{1}{A} + \frac{R_B}{(R_A + R_B)}} \tag{27}$$

As $A \to \infty$

$$\frac{V_2}{V_1} \to \frac{1}{R_B/(R_A + R_B)} = \frac{(R_A + R_B)}{R_B} = \left\{ 1 + \frac{R_A}{R_B} \right\}$$

Since this relationship is constant, let

$$\frac{V_2}{V_1} = \left\{ 1 + \frac{R_A}{R_B} \right\} = K \tag{28}$$

Figure 11 is the controlled-source model for the Sallen and Key circuit of Figure 9.

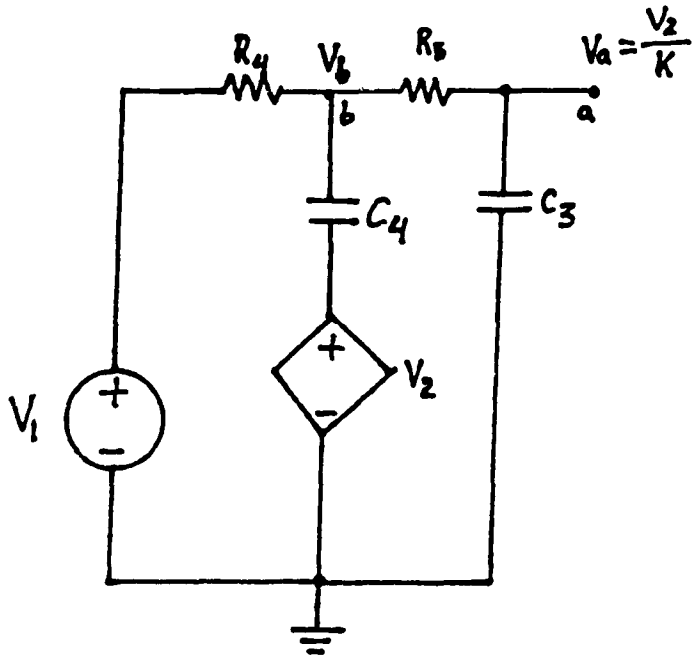


Figure 11 Sallen and Key Filter Model [14]

Using KCL at node A: [14]

$$\frac{1}{R_5}\left\{\frac{V_2}{K} - V_b\right\} + \left\{\frac{V_2}{K} - 0\right\} C_3 S = 0 \tag{29}$$

Using KCL at node B: [14]

$$\frac{1}{R_5}\left\{V_b - \frac{V_2}{K}\right\} + C_4 S\left\{V_b - V_2\right\} + \frac{1}{R_4}\left\{V_b - V_1\right\} = 0 \tag{30}$$

Equation (30) may be rearranged:

$$\left\{\frac{1}{R_5} + C_4 S + \frac{1}{R_4}\right\} V_b - \frac{1}{R_5}\,\frac{V_2}{K} = C_4 S V_2 + \frac{V_1}{R_4} \tag{31}$$

Equation (29) may be rearranged also:

$$-\frac{1}{R_5} V_b + \left\{\frac{1}{R_5} + C_3 S\right\}\frac{V_2}{K} = 0 \tag{32}$$

Equation (32) is used to solve for V_b and this is then substituted into equation (31).

$$V_b = (1 + R_5 C_3 S)\,\frac{V_2}{K} \tag{33}$$

$$\left\{\frac{1}{R_5} + C_4 S + \frac{1}{R_4}\right\}\left\{1 + R_5 C_3 S\right\}\frac{V_2}{K} - \frac{1}{R_5}\,\frac{V_2}{K} = C_4 S V_2 + \frac{V_1}{R_4}$$

$$\left\{\frac{1}{R_5} + C_4 S + \frac{1}{R_4} + C_3 S + R_5 C_3 C_4 S^2 + \frac{R_5}{R_4} C_3 S\right\}\frac{V_2}{K} = -\frac{V_2}{R_5 K} - C_4 S V_2 = \frac{V_1}{R_4}$$

$$V_2\left|\frac{1}{K}\left\{C_4 S + \frac{1}{R_4} + C_3 S + R_5 C_3 C_4 S^2 + \frac{R_5}{R_4} C_3 S\right\} - C_4 S\right| = \frac{V_1}{R_4}$$

$$\frac{V_2}{V_1} = \frac{1}{R_4} \cdot \frac{K}{\left\{ C_4S + \frac{1}{R_4} + C_3S + R_5C_3C_4S^2 + \frac{R_5}{R_4} C_3S - KC_4S \right\}}$$

$$\frac{V_2}{V_1} = \frac{K}{(R_4C_4S + 1 + R_4C_3S + R_4R_5C_3C_4S^2 + R_5C_3S - KR_4C_4S)}$$

$$\frac{V_2}{V_1} = \frac{K}{[R_4R_5C_3C_4S^2 + (R_4C_4 + R_4C_3 + R_5C_3 - KR_4C_4)S + 1]}$$

$$\frac{V_2}{V_1} = \frac{\frac{K}{R_4R_5C_3C_4}}{\left\{ S^2 + \left[\frac{1}{C_3R_5} + \frac{1}{R_5C_4} + \frac{1}{R_5C_4} - \frac{K}{R_5C_3} \right] S + \frac{1}{R_4R_5C_3C_4} \right\}} \qquad (34)$$

where K is given by equation (28).

4.2.1 Sensitivity of Low-Pass Filter

There are five parameters, namely K, C_3,C_4, R_4 and R_5 that can change due to temperature variation and component aging. The sensitivity of the transfer function due to the variation of parameter X is equal to the percentage change in T(S,X) divided by the percentage change in X. In each derivation,

$$Let\, X = (R_4R_5C_3C_4S^2 + R_4C_4S + R_4C_3S + R_5C_3S - K_0R_4C_4S + 1)$$

$$S_K^T = \frac{dT/T}{dK/K} = \frac{K_0}{T} \cdot \frac{dT}{dK} = \frac{K_0}{\frac{K_0}{X}} \cdot \frac{X(1) - K_0(-R_4C_4S)}{X^2}$$

where K_0 is the open-loop gain of the operational amplifier.

$$S^T_{K_0} = \frac{(X + K_0 R_4 C_4 S)}{X} = \frac{(R_4 R_5 C_3 C_4 S^2 + R_4 C_4 S + R_4 C_3 S + R_5 C_3 S + 1)}{(R_4 R_5 C_3 C_4 S^2 + R_4 C_4 S + R_4 C_3 S + R_5 C_3 S - K_0 R_4 C_4 S + 1)}$$

For the ideal operational amplifier, $K_0 = \infty$,

As $K_0 \to \infty$,

$S^T_{K_0} \to 0$

$$S^T_{C_3} = \frac{dT/T}{dC_3/C_3} = \frac{C_3}{T} \cdot \frac{dT}{dC_3} = \frac{C_3}{\frac{K_0}{X}} \cdot \frac{X(0) - K_0(R_4 R_5 C_4 S^2 + R_4 S + R_5 S)}{X^2}$$

$$S^T_{C_3} = -\frac{C_3 K_0}{K_0 X}(R_4 R_5 C_4 S^2 + R_4 S + R_5 S) = \frac{-C_3}{X}(R_4 R_5 C_4 S^2 + R_4 S + R_5 S)$$

$$S^T_{C_3} = \frac{(-R_4 R_5 C_3 C_4 S^2 - R_4 C_3 S - R_5 C_3 S)}{(R_4 R_5 C_3 C_4 S^2 + R_4 C_4 S + R_4 C_3 S + R_5 C_3 S - K_0 R_4 C_4 S + 1)}$$

As $K_0 \to \infty$,

$S^T_{C_3} \to 0$

$$S^T_{C_4} = \frac{dT/T}{dC_4/C_4} = \frac{C_4}{T} \cdot \frac{dT}{dC_4} = \frac{C_4}{\frac{K_0}{X}} \cdot \frac{X(0) - K_0(R_4 R_5 C_3 S^2 + R_4 S - K_0 R_4 S)}{X^2}$$

$$S^T_{C_4} = \frac{C_4}{1} \cdot \frac{-1}{X}(R_4 R_5 C_3 S^2 + R_4 S - K_0 R_4 S)$$

$$S^T_{C_4} = \frac{(-R_4 R_5 C_3 C_4 S^2 - C_4 R_4 S + K_0 C_4 R_4 S)}{(R_4 R_5 C_3 C_4 S^2 + R_4 C_4 S + R_4 C_3 S + R_5 C_3 S - K_0 R_4 C_4 S + 1)}$$

As $K_0 \to \infty$,

$S^T_{C_4} \to -1$

$$S_{R_4}^T = \frac{dT/T}{dR_4/R_4} = \frac{R_4}{T} \cdot \frac{dT}{dR_4} = \frac{R_4}{\frac{K_0}{X}} \cdot \frac{X(0) - K_0(R_5C_3C_4S^2 + C_4S + C_3S - K_0C_4S)}{X^2}$$

$$S_{R_4}^T = \frac{-R_4}{X}(R_5C_3C_4S^2 + C_4S + C_3S - K_0C_4S)$$

$$S_{R_4}^T = \frac{(-R_4R_5C_3C_4S^2 - R_4C_4S - R_4C_3S + K_0R_4C_4S)}{(R_4R_5C_3C_4S^2 + R_4C_4S + R_4C_3S + R_5C_3S - K_0R_4C_4S + 1)}$$

As $K_0 \to \infty$,

$S_{R_4}^T \to -1$

$$S_{R_5}^T = \frac{dT/T}{dR_5/R_5} = \frac{R_5}{T} \cdot \frac{dT}{dR_5} = \frac{R_5}{\frac{K}{X}} \cdot \frac{X(0) - K_0(R_4C_3C_4S^2 + C_3S)}{X^2}$$

$$S_{R_5}^T = \frac{-R_5}{X}(R_4C_3C_4S^2 + C_3S) = \frac{(-R_4R_5C_3C_4S^2 - R_5C_3S)}{(R_4R_5C_3C_4S^2 + R_4C_4S + R_4C_3S + R_5C_3S - K_0R_4C_4S + 1)}$$

As $K_0 \to \infty$,

$S_{R_5}^T \to 0$

It should also be noted that:

As $K_0 \to \infty$,

$$T = \frac{V_2}{V_1} \to \frac{-1}{R_4C_4S}$$

Equation (34) is of the form:

$$\frac{V_2}{V_1} = T_v(s) = \frac{K/w_p^2}{S^2 + S\frac{w_p}{Q_p} + w_p^2} \tag{35}$$

which is the standard form for a second-order low-pass active filter[16]. Comparing (34) and (35) yields:

$$w_p = \frac{1}{\sqrt{R_4 R_5 C_3 C_4}} \tag{36}$$

Let $$a = \left| \frac{1}{R_5 C_3}(1-K) + \frac{1}{R_5 C_4} + \frac{1}{R_4 C_4} \right|$$

Hence

$$a = \frac{w_p}{Q_p} \text{ or } Q_p = \frac{w_p}{a}$$

$$Q_p = \frac{1}{\frac{\sqrt{R_4 R_5 C_3 C_4}}{R_5 C_3}(1-K) + \frac{\sqrt{R_4 R_5 C_3 C_4}}{R_5 C_4} + \frac{\sqrt{R_5 R_4 C_3 C_4}}{R_4 R_4}} = \frac{1}{(3-K)} = 0.707 \tag{37}$$

The ω_p and Q_p are:

Setting [17]

$$R_4 = R_5 = 1\Omega \text{ and } C_3 = C_4 = 1F.,$$

$$S_{R_4}^{\omega_p} = \frac{R_4}{W_p} \cdot \frac{\partial \omega_p}{\partial R_4} = -\frac{1}{2}$$

$$S_{R_5}^{\omega_p} = \frac{R_5}{W_p} \cdot \frac{\partial \omega_p}{\partial R_5} = -\frac{1}{2}$$

$$S_{C_3}^{\omega_p} = \frac{C_3}{W_p} \cdot \frac{\partial \omega_p}{C_3} = -\frac{1}{2}$$

$$S_{C_4}^{\omega_p} = \frac{C_4}{W_p} \cdot \frac{\partial \omega_p}{C_4} = -\frac{1}{2}$$

$$S_K^{W_p} = \frac{K}{W_p} \cdot \frac{\partial \omega_p}{K} = \frac{\partial \omega_p}{W_p} = K\sqrt{R_4 R_5 C_3 C_4} \cdot \quad 0 = 0$$

$$S_{R_4}^{Q_p} = \frac{R_4}{Q_p} \cdot \frac{\partial Q_p}{R_4} = \left| Q_p \frac{\sqrt{R_5 C_4}}{\sqrt{R_4 C_3}} - \frac{1}{2} \right| = -S_{R_5}^{Q_p} = 0.207$$

$$S_{C_3}^{Q_p} = -S_{C_4}^{Q_p} = Q_p \frac{\sqrt{C_4}}{\sqrt{C_3}} \left\{ \frac{\sqrt{R_4}}{\sqrt{R_5}} + \frac{\sqrt{R_5}}{\sqrt{R_4}} \right\} - \frac{1}{2} = 0.914$$

$$S_K^{Q_p} = Q_p \left| \frac{\sqrt{R_4 C_3}}{\sqrt{R_5 C_4}} + \frac{\sqrt{R_5 C_4}}{\sqrt{R_4 C_3}} + \frac{\sqrt{R_5 C_4}}{\sqrt{R_4 C_3}} \right| - 1 = 1.121$$

4.2.2 Low-Pass Filter Performance

The equal component design was used for this filter, that is, $R_4 = R_5$ and $C_3 = C_4$ as shown in Figure 9. This is a second-order low-pass filter, hence α, the damping factor of a Butterworth filter, is $\alpha = 1.414$[18].

Let $C_3 = C_4 = 0.1\mu F$. The frequency scale is given by

$$a = 2\Pi fc = 6.283 \times 50 = 314.15$$

The impedance scale is given by:

$$C_1 = \frac{C_1^*}{ab} \text{ or } b = \frac{C_1^*}{C_1 a}$$

where $C_1^* = 1F$. Thus,

$$b = \frac{1}{0.1 \times 314.15 \times 10^{-6}} = \frac{1}{31.415 \times 10^{-6}} = 31\,832\,\Omega$$

Hence $R_4 = R_5 = 33\,000\Omega$ (nearest standard value)

By normalizing, let

$R_4 = R_5 = 1\Omega$ and $C_3 = C_4 = 1F.$, then equation (34) becomes:

$$\frac{V_2}{V_1} = \frac{K}{(S^2 + [3-K]S + 1)} \tag{38}$$

Comparing equation (35) and equation (38):

$$K = G = (3-\alpha) = \left\{1 + \frac{R_A}{R_B}\right\} \text{ or } \frac{R_A}{R_B} = (2-\alpha) = 0.586$$

Hence, $R_A = 0.586\ R_B$. Let us try $R_B = 3000\Omega$, $R_A = 1758\Omega$. The nearest standard value of R_A is chosen as 1800Ω.

The damping factor, α, is derived as follows:

$$n = 2\ (even)$$

$$1 + S^{2n} = 0$$

$$S^{2n} = -1$$

$$e^{j2n\theta} = -1$$

$$\cos 2n\theta + j \sin 2n\theta = -1$$

$$\left.\begin{aligned} Cos\ 2n\theta &= -1 \\ Sin\ 2n\theta &= 0 \end{aligned}\right\} \quad \text{satisfied when } 2n\theta = (2m+1)\pi,\ m = 0,1,2,\ldots \text{ and } \theta = \frac{(2m+1)\pi}{2n},\ m = 0,1,2,\ldots \text{ and } n \text{ is order of filter}$$

$$Hence, \theta = \frac{(2m+1)\pi}{4},\ m = 0,1,2,\ldots\ Thus \theta = \frac{\pi}{4}; \frac{3\pi}{4}; \frac{5\pi}{4}; \frac{7\pi}{4}; \frac{9\pi}{4}; \ldots$$

Figure 12 is the pole plot for $\frac{(2m+1)\pi}{4} = 0$ *in the s-plane*

To obtain the Hurwitz polynomial, only the left-hand roots are used. Hence, the Hurwitz polynomial is:

$$(s-e^{j3\pi/4})(s-e^{j5\pi/4})$$

$$Tv(s) = \frac{K}{(s-e^{j3\pi/4})(s-e^{j5\pi/4})} = \frac{K}{(s - Cos\frac{3\pi}{4} - j\,sin\frac{3\pi}{4})(s - Cos\frac{5\pi}{4} - j\,sin\frac{5\pi}{4})}$$

$$Tv(s) = \frac{K}{(s - Cos\,135° - j\,sin\,135°)(s - Cos\,225° - j\,sin\,225°)} =$$

$$\frac{K}{(s + 0.7071 - j0.7071)(s + 0.7071 + j0.7071)}$$

$$Tv(s) = \frac{K}{(s^2 + 0.7071\,s + js0.7071 + 0.7071\,s + 0.5 + j0.5 - js0.7071 - j0.5 + 0.5)}$$

$$Tv(s) = \frac{K}{(s^2 + 1.414\,s + 1)}$$

where K is the gain factor.

Hence, for a second order Butterworth filter, α, the damping factor is 1.414.

To obtain the theoretical frequency response of the filter, s = jω is substituted into equation (34).

Normalizing equation (39) with $R_4 = R_5 = 1\Omega$ and $C_3 = C_4 = 1F.$, the following is obtained:

$$\frac{V_2}{V_1} = \frac{K/R_4R_5C_3C_4}{-w^2 + jw\left\{\frac{1}{C_3R_5} + \frac{1}{R_5C_4} + \frac{1}{R_4C_4} - \frac{K}{R_5C_3}\right\} + \frac{1}{R_4R_5C_3C_4}} \qquad (39)$$

$$\frac{V_2}{V_1} = \frac{K}{[-w^2 + jw(3-k) + 1]}$$

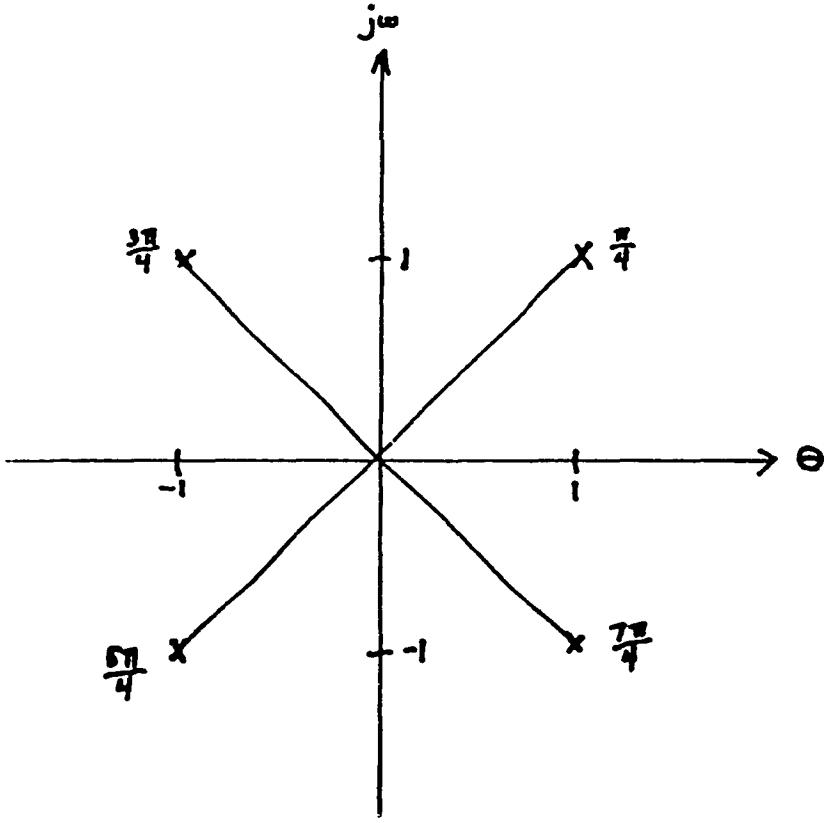


Figure 12 Pole Plot for $\theta = \frac{(2m + 1)\pi}{4}$ in the s-plane

Since $\alpha = (3-K)$,

$$\frac{V_2}{V_1} = T(jw) = \frac{K}{-w^2 + jw\alpha + 1}$$

$$|T(Jw)| = \frac{K}{[(-w^2+jw\alpha+1)(-w^2-jw\alpha+1)]^{\frac{1}{2}}} =$$

$$\frac{K}{\sqrt{(w^4+jw^3\alpha-w^2-jw^3\alpha+w^2\alpha^2+jw\alpha-w^2-jw\alpha+1)}}$$

$$|T(Jw)| = \frac{K}{\sqrt{w^4 + w^2(\alpha^2 - 2) + 1}}$$

Since $\alpha = 1.414$, that is, $\alpha^2 = 2$.

$$|T(Jw)| = \frac{K}{\sqrt{w^4 + 1}}$$

$$20 \log_{10} |T(Jw)| = 20 \log_{10} K - 20 \log_{10} (w^4 + 1)^{\frac{1}{2}} \qquad (40)$$

The normalized theoretical frequency response may be plotted directly from equation (40). The resulting curve may be shifted by the frequency scale a to get the theoretical of the actual filter, using $w^* = aw$, where w^* is a scaled quantity. Table 3 lists the actual and design data of the low-pass filter. For this low-pass filter, a = 314.15, and gain K = 1.586. Figure 13 illustrates the frequency-response plots of the low-pass filters. The phase-response plots are shown on Figure 14. The difference in the left and right channel response curves is due to component tolerances.

Table 3 Low-Pass Filter ($f_c = 50$ Hz) Performance Data

			Theoret-ical	Actual Data								
w (rad/s)	aw (rad/s)	F (Hz)	G(dB)	V_{IN} (V_{p-p})	V_{O_L} (v_{p-p})	$\emptyset_L$ (°)	G_L	G_L (dB)	V_{O_R} (Vp-p)	$\emptyset_R$ (°)	G_R	G_R (dB)
0.1	31.415	5	4.01	2.0	3.2	0	1.6	4.08	3.2	0	1.6	4.08
0.2	62.83	10	4.00	2.0	3.2	-29	1.6	4.08	3.2	-29	1.6	4.08
0.4	125.66	20	3.90	2.0	3.2	-43	1.6	4.08	3.2	-43	1.6	4.08
0.6	188.49	30	3.48	2.0	2.7	-84	1.35	2.61	2.8	-84	1.4	2.92
0.8	251.32	40	2 52	2.0	2.4	-87	1.2	1.58	2.7	-87	1.35	2.61
1.0	314.15	50	1.00	2.0	2.0	-90	1.0	0.00	2.0	-90	1.0	0.00
1.2	376.98	60	-0.87	2 0	1.8	-98	0.9	-0.92	2.0	-98	1.0	0.00
1.4	439.81	70	-2.84	2.0	1.35	-129	0.675	-3.41	1.4	-129	0.7	-3.10
1.6	502.64	80	-4.78	2.0	1.15	-144	0.575	-4.81	1.2	-144	0.6	-4.44
1.8	565.47	90	-6 60	2 0	0.78	-150	0.39	-8.18	0.78	-150	0.39	-8.18
2.0	628.3	100	-8.29	2 0	0 74	-156	0.37	-8.64	0.74	-156	0.37	-8.64
4.0	1256.6	200	-20.09	2.0	0.20	-166	0.1	-20.00	0.20	-173	0.10	-20.00
10.0	3141.5	500	-35.99	2.0	0.033	-180	0.0165	-35.65	0.032	-180	0.016	-35.92
20.0	6283	1,000	-48.04	2.0	0.008	-180	0.004	-47.96	0.008	-180	0.004	-47.96

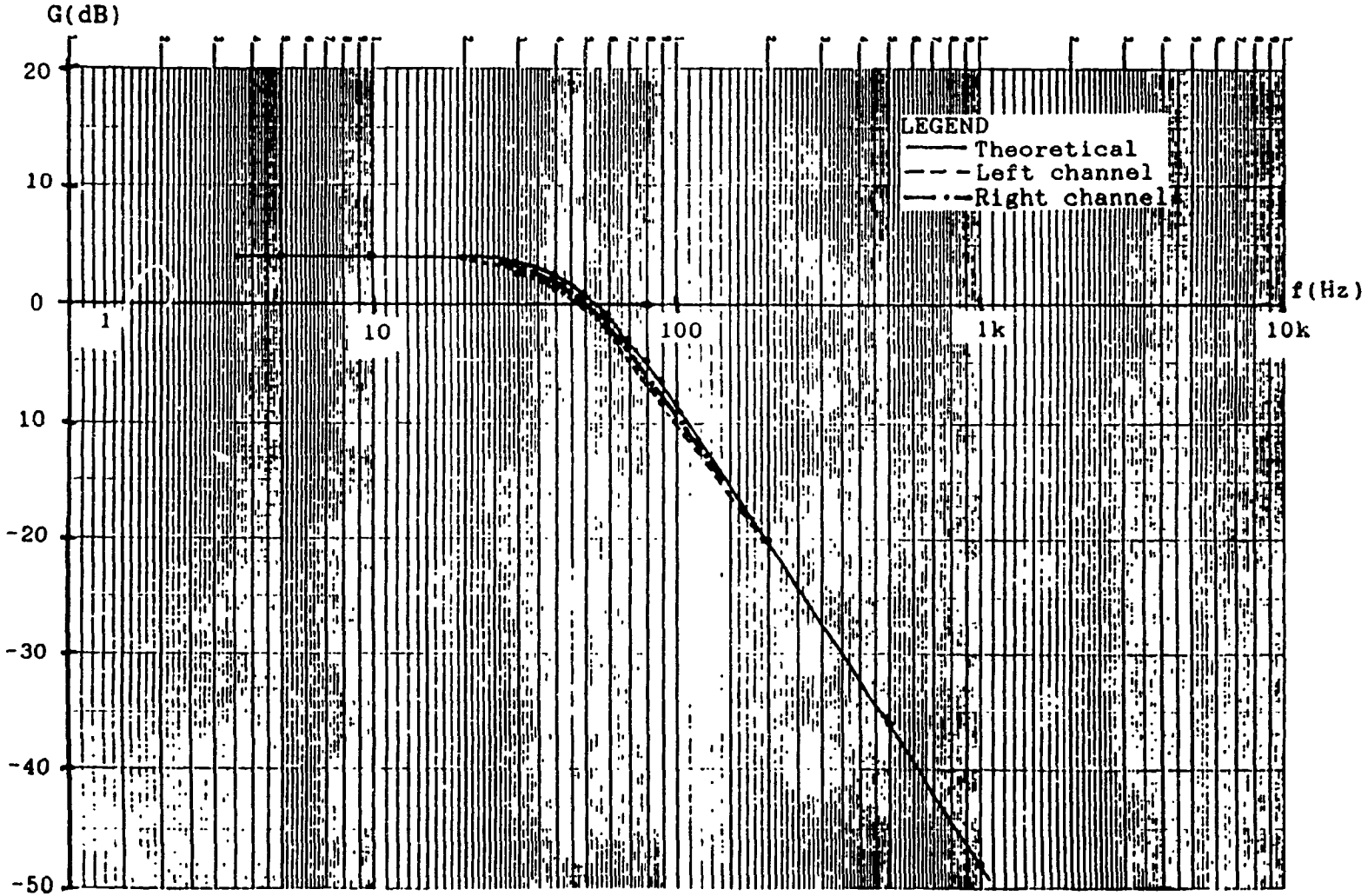


Figure 13 Frequency-Response Plots of Filter
(f_c = 50 Hz)

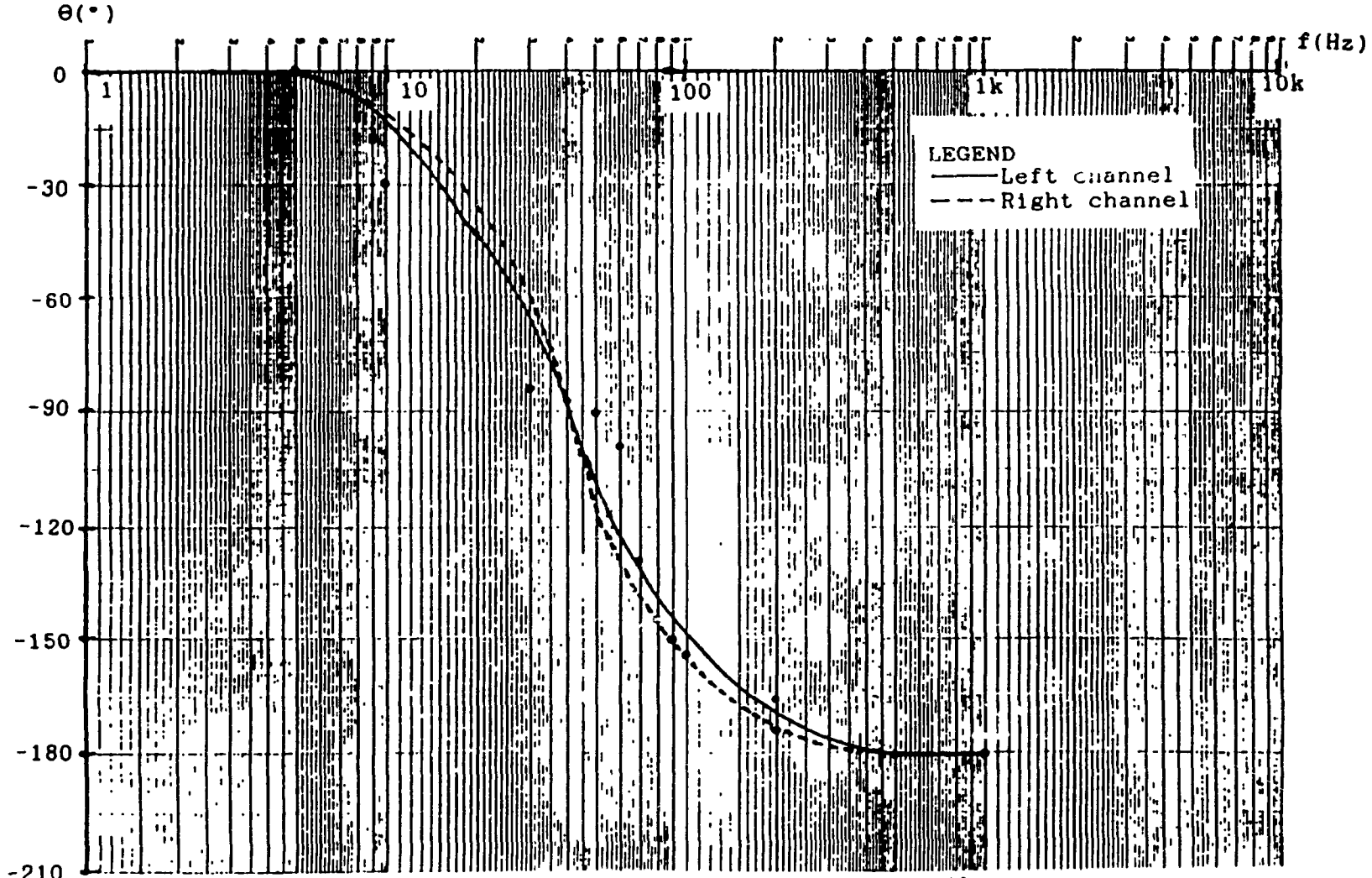


Figure 14 Phase-Response Plots of Filter
(f_c = 50 Hz)

4.3 Summing Amplifier

The summing amplifier yields an output voltage that is 180° out of phase with the input signal. Figure 15 is a schematic of the summing amplifier. Potentiometer R_{P1} is a voltage divider such that:

$$V_{IN_2} = \frac{R_{P1a}}{(R_{P1a} + R_{P1b})} V'_{IN_2} \tag{41}$$

Using KCL at node a, the following is obtained[19]

$$\frac{\left\{(V_{IN_1} - V_x)\right\}}{R_6} + \frac{\left\{(V_{IN_2} - V_x)\right\}}{R_7} = \frac{\left\{(V_x - V_2)\right\}}{R_8} \tag{42}$$

Equation (42) may be simplified by the principle of the virtual short circuit, that is, $V_x = 0$[19].

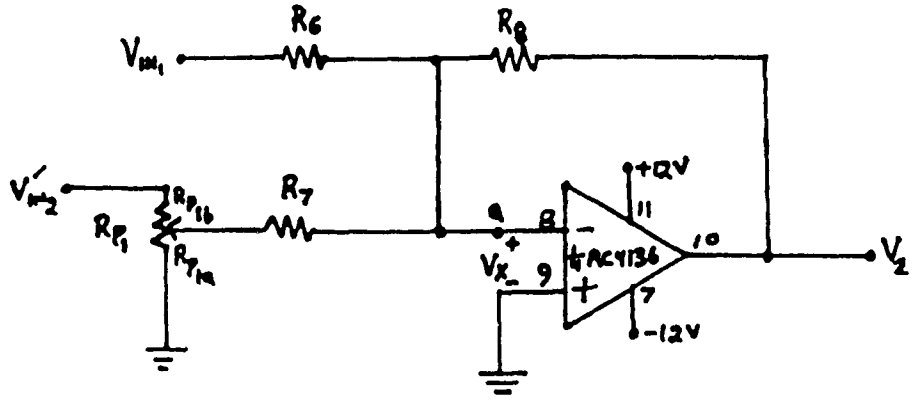
$$\frac{V_{IN1}}{R_6} + \frac{V_{IN2}}{R_7} = \frac{-V_2}{R_8} \tag{43}$$

$$V_{IN_1}\frac{R_8}{R_6} + V_{IN_2}\frac{R_8}{R_7} = -V_2 \tag{44}$$

$$V_2 = \frac{-R_8}{R_6} V_{IN_1} - \frac{R_8}{R_7} V_{IN_2} \tag{45}$$

Substituting equation (41) into equation (45).

$$V_2 = \frac{-R_8}{R_6} V_{IN_1} - \frac{R_8}{R_7} \cdot \frac{R_{P1a}}{(R_{P1a} + R_{P1b})} V'_{IN_2} \tag{46}$$



R_{P_1} = 100kΩ potentiometer

R_6, R_8 = 10kΩ

R_7 = 1.8kΩ

Figure 15 Schematic of Summing Amplifier

4.3.1 Sensitivity of Summing Amplifier

The transfer function of the summing amplifier may also be written as, assuming $V_{IN_1} = V'_{IN_2} = V_1$: (47)

$$V_2 = \frac{-R_8}{R_6} V_1 - \frac{R_8}{R_7} V_1 \tag{48}$$

$$\frac{V_2}{V_1} = \frac{-R_8}{R_6} - \frac{R_8}{R_7} \tag{49}$$

$$T = \frac{V_2}{V_1} = \frac{-R_7R_8 - R_6R_8}{R_6R_7} \tag{50}$$

$$S^T_{R_6} = \frac{dT/T}{dR_6/R_6} = \frac{R_6}{T} \cdot \frac{dT}{dR_6} = \frac{R_6^2R_7}{(-R_7R_8 - R_6R_8)} \cdot \frac{(R_6R_7)(-R_8) + (R_7R_8 + R_6R_8) x R_7}{(R_6R_7)^2}$$

$$S^T_{R_6} = \frac{(-R_6R_7R_8) + (R_7^2R_8 + R_6R_7R_8)}{(-R_7R_8 - R_6R_8)R_7} = \frac{R_7^2R_8}{(-R_7^2R_8 - R_6R_7R_8)} = \frac{R_7R_8}{(R_7R_8 + R_6R_8)}$$

Since $R_6 = R_8$,

$$S^T_{R_6} = \frac{-R_7R_8}{R_8R_8 + R_8R_8)} = \frac{-R_7}{2R_8}$$

Since $R_7 = 0.18R_8$,

$$S^T_{R_6} = \frac{-0.18R_8}{2R_8} = -0.09$$

$$S^T_{R_7} = \frac{dT}{dR_7/R_7} = \frac{R_7}{T} \cdot \frac{dT}{dR_7} = \frac{R_7^2R_6}{(-R_7R_8 - R_6R_8)} \cdot \frac{(R_6R_7)(-R_8) + (R_7R_8 + R_6R_8)R_6}{(R_6R_7)^2}$$

$$S^T_{R_7} = \frac{(-R_6R_7R_8 + R_6R_7R_8 + R_6'^2R_8)}{R_6(-R_7R_8 - R_6R_8)} = \frac{R_6^2R_8}{R_6(-R_7R_8 - R_6R_8)} = \frac{-R_6R_8}{(R_7R_8 + R_6R_8)}$$

Since $R_6 = R_8$,

$$S^T_{R_7} = \frac{-R^2_8}{(R_7R_8+R^2_8)} = \frac{-R_8}{(R_7+R_8)}$$

Since $R_7 = 0.18R_8$,

$$S^T_{R_7} = \frac{-R_8}{1.18R_8} = \frac{-1}{1.18} = -0.8475$$

$$S^T_{R_8} = \frac{dT/T}{dR_8/R_8} = \frac{R_8}{T} \cdot \frac{dT}{dR_8} = \frac{R_6R_7R_8}{(-R_7R_8-R_6R_8)} \cdot \frac{R_6R_7(-R_6-R_7)+(R_7R_8+R_6R_8)(0)}{(R_6R_7)^2}$$

$$S^T_{R_8} = \frac{R_8(-R_6-R_7)}{(-R_7R_8-R_6R_8)} = \frac{(-R_6R_8-R_7R_8)}{(-R_6R_8-R_7R_8)} = 1$$

4.3.2 Component Values of Summing Amplifier

For frequencies above approximately 1000 Hz, the net gain of the sub-woofer simulator is unity. Hence $R_6 = R_8$ and they were set to 10000Ω arbitrarily.

Potentiometer R_{P1} is the bass-boost adjust control. Resistor R_7 was set at 1800Ω to set the maximum gain of this section of the summing amplifier to about 5.56. The potentiometer used is a dual 100000Ω variable resistor. This value is more than ten times the output impedance and the input impedance of the low-pass filter and the summing amplifier respectively; hence, neither one is loaded by the potentiometer.

4.3.3 Performance of Summing Amplifier

The output signal was 180° out of phase with the input voltage. The gain was unity for signals entering V_{IN_1} and the gain was about 5.56 for signals entering V_{IN_2} (refer to Figure 15).

4.4 Sub-Woofer Simulator System

The complete sub-woofer simulator schematic is shown in Figure 16. Two are required, one for each channel.

Frequencies of about 100 Hz or less are amplified, while those above 100 Hz are passed with a gain of unity. Table 4 lists the performance data of the sub-woofer simulator.

Figure 17 is the frequency-response plots of the sub-woofer simulator and Figure 18 is the phase-response plot of the sub-woofer simulator system. In Figure 17, the minimum curves are the responses of the sub-woofer simulator with potentiometer R_{P_1} (see Figure 16) set for minimum bass boost while the maximum curves are the responses of the sub-woofer simulator with potentiometer R_{P_1} set for maximum bass boost. The input and output signals are in phase except for the frequencies in the range of 5 Hz to 500 Hz. Since the human ear is insensitive to phase shift, little distortion is introduced into the system.

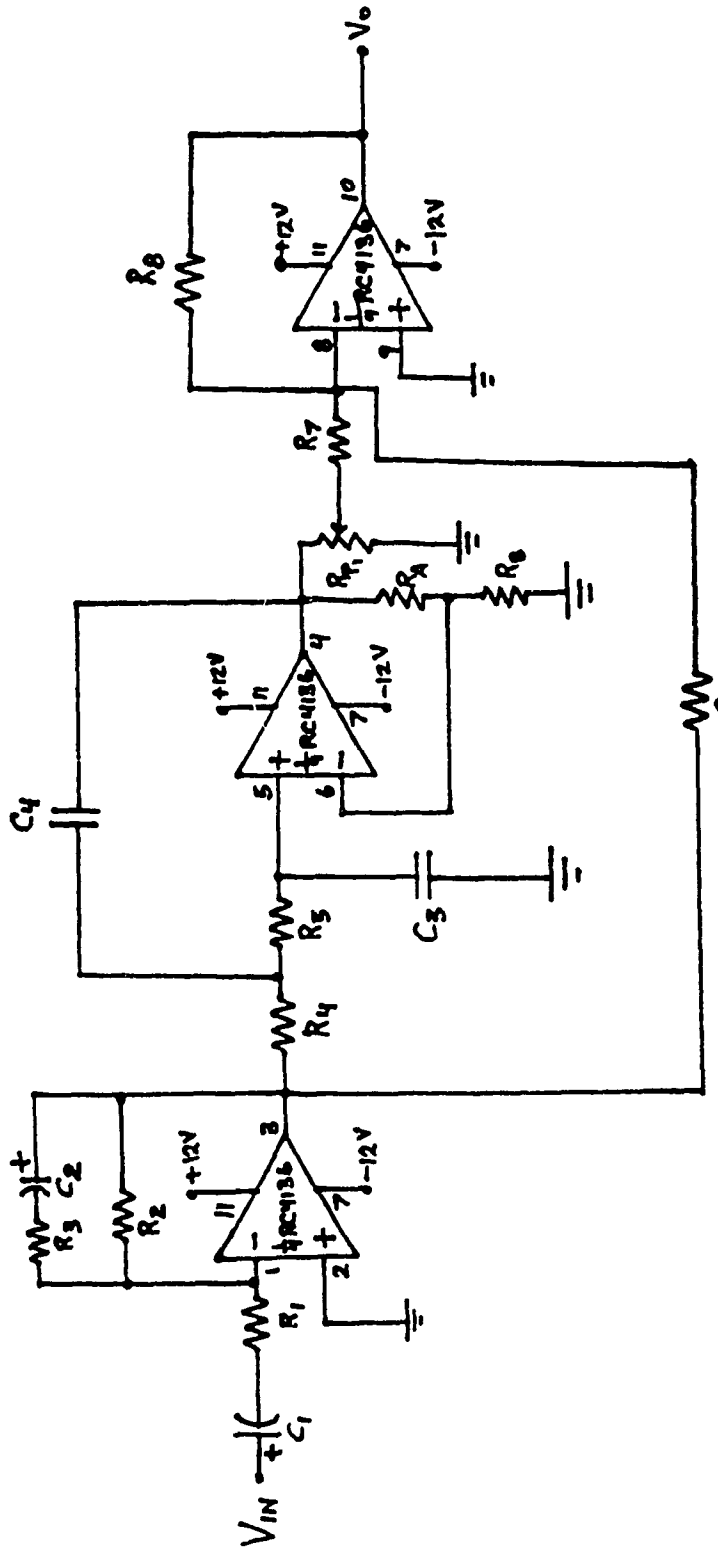


Figure 16 Schematic of Sub-Woofer Simulator

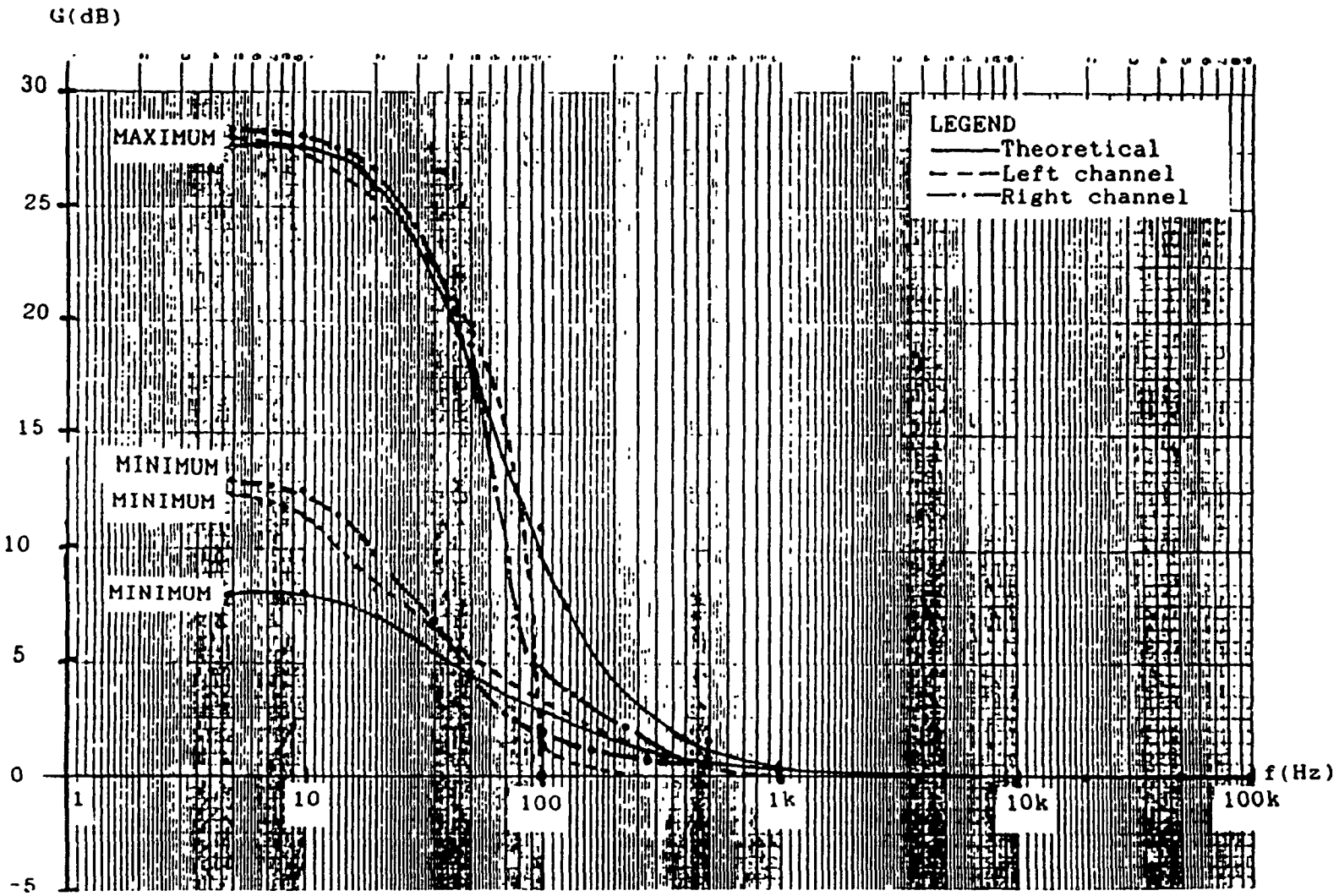


Figure 17 Frequency-Response Plots of Sub-Woofer Simulator

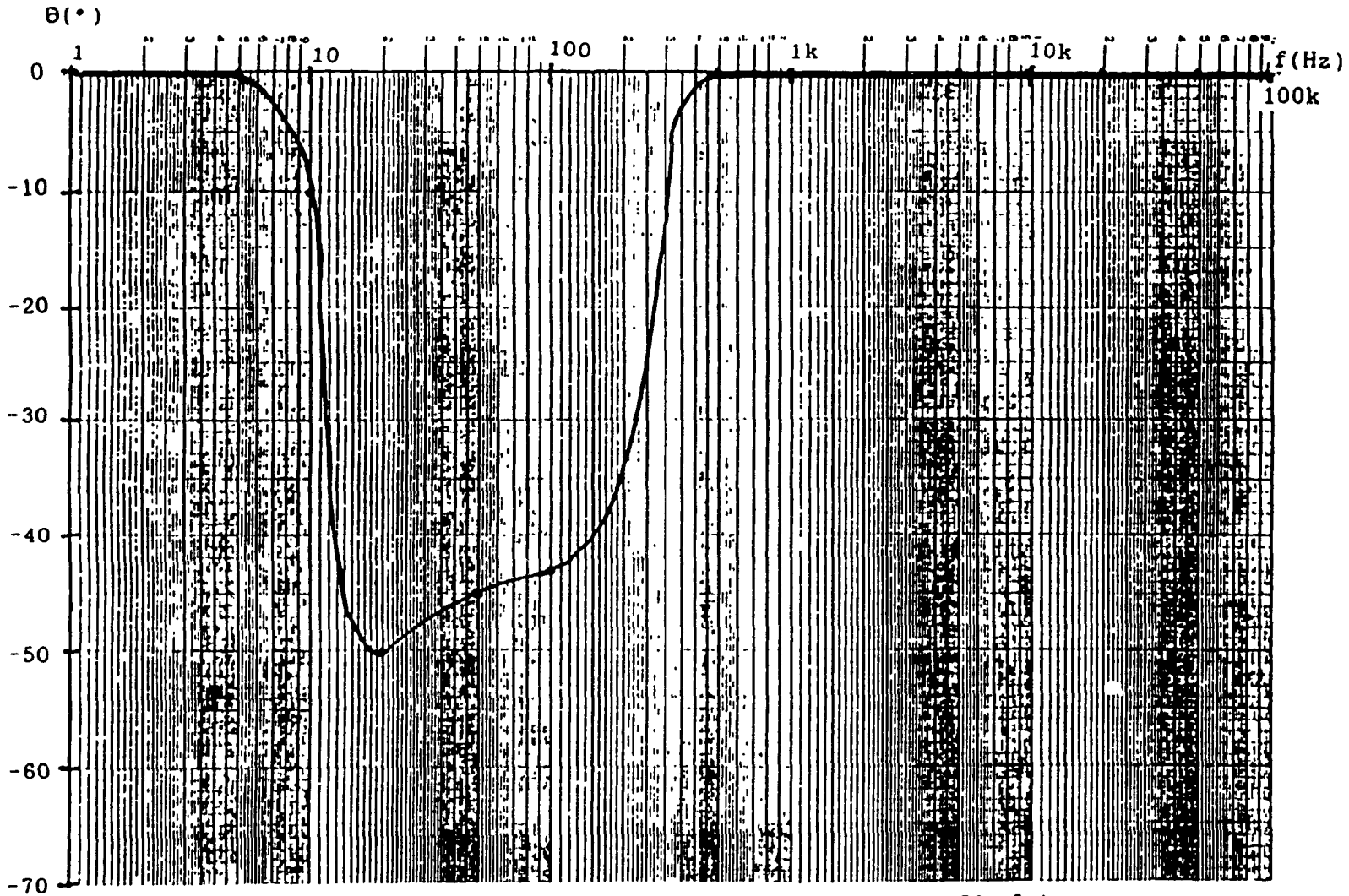


Figure 18 Phase-Response Plots of Sub-Woofer Simulator

Table 4 Sub-Woofer Simulator Performance Data

Freq. (Hz)	Theoretical				Actual Data									
	G^{*}_{MIN}	G_{MIN} (dB)	G^{**}_{MAX}	G_{MAX} (dB)	V_{in} (V_{p-p})	V_{OL} (V_{p-p}) MIN	V_{OL} (V_{p-p}) MAX	G_{LMIN} (dB)	G_{LMAX} (dB)	V_{OL} (V_{p-p}) MIN	V_{OL} (V_{p-p}) MAX	G_{RMIN} (dB)	G_{RMAX} (dB)	∅ (°)
5	2.50	7 96	24.46	27.77	0.5	2.10	19.00	12.46	27 93	2.20	21.00	12.87	28.21	0
10	2.55	8 13	24.51	27.79	0.5	1.90	16.50	11.60	27.31	2.15	18.00	12.67	28.08	-10
20	2.23	6.97	21.70	26.73	0.5	1.30	10.80	8.30	24.40	1.55	13.00	9.83	25.87	-50
50	1.69	4.56	7.97	18.03	0.5	0.90	4.00	5.11	20.19	0 85	4.00	4.61	19.29	-45
100	1.39	2.86	3 56	11.03	0.5	0 50	0.60	0 00	1.58	0.625	0.90	1.94	5.11	-43
500	1.07	0.59	1.16	1.29	0.5	0.60	0.50	1 58	0.00	0.55	0.55	0.83	0.00	0
1K	1.04	0.34	1.06	0.51	0.5	0.50	0.50	0.00	0.00	0.50	0.50	0.00	0.00	0
5K	1.00	0.00	1.00	0.00	0.5	0.50	0.50	0.00	0.00	0 50	0.50	0.00	0 00	0
10K	0.99	-0 09	1.00	0.00	0.5	0.50	0.50	0 00	0.00	0.50	0.50	0.00	0.00	0
20K	0.99	-0.09	1.00	0.00	0.5	0 50	0.50	0.00	0.00	0.50	0.50	0.00	0.00	0
50K	0.99	-0.09	1.00	0.00	0.5	0 50	0.50	0.00	0.00	0.50	0.50	0.00	0.00	0
100K	0.99	-0.09	1.00	0.00	0.5	0.50	0 50	0.00	0.00	0.50	0.50	0.00	0.00	0

* $G_{MIN} = G_{INPUT\ AMP}\ G_{SUMMING\ AMPA}$

** $G_{MAX} = G_{INPUT\ AMP}\ G_{SUMMING\ AMPA} G + G_{INPUT\ AMP} \times G_{L\ P\ F} \times G_{SUMMING\ AMPB}$

where $G_{SUMMING\ AMPA} = 1$

where $G_{SUMMING\ AMPB} = 5.56$

CHAPTER 5

DECODER

The decoder system derives an (L-R) rear-channel signal from the two front channel signals. High frequencies are attenuated by a low-pass filter. The rear-channel amplitude is varied by the rear channel gain control. A block diagram of the decoder is shown in Figure 19.

The decoder passes the left input signal in phase and it inverts the right input signal. The low-pass filter passes all signals in its pass-band in phase with its input voltage.

5.1 Decoder Design

The decoder is a unity-gain differential amplifier. The decoder schematic is shown in Figure 20. The resistors are all of equal value and were arbitrarily chosen as 10000Ω.

The model of the input terminals is shown in Figure 21. The voltage between nodes A and B is zero because of the virtual short property of the operational amplifier[19]. Hence,

$$V_a = V_b \tag{51}$$

Therefore the voltages at nodes A and B are the same[19]. The nodes may not be tied together, and Kirchoff's current law must be used at each node[19].

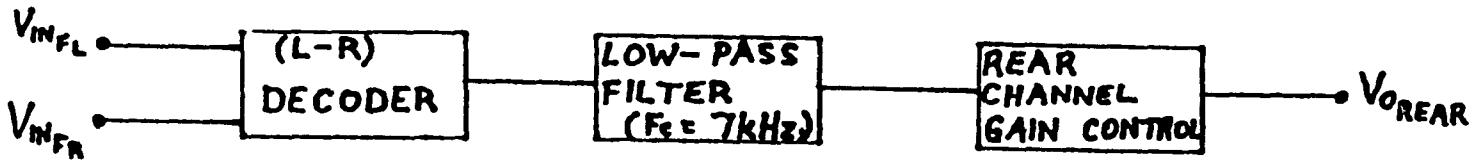


Figure 19 Block Diagram of Decoder

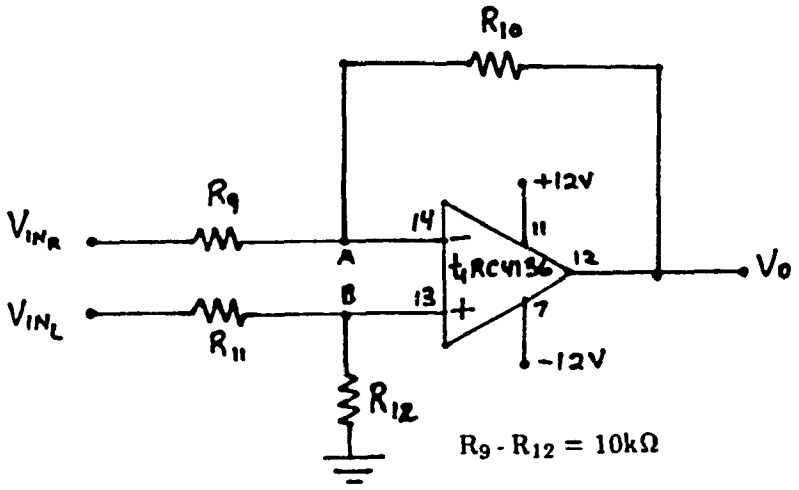


Figure 20 Schematic of Decoder

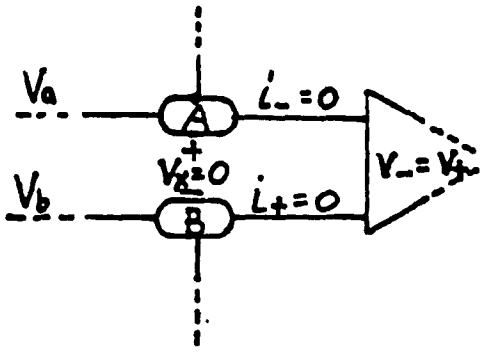


Figure 21 Model of Input Terminals[19]

Since $i_- = 0$ (51), KCL at node A:

$$\frac{\left\{V_{IN_R} - V_a\right\}}{R_9} = \frac{\left\{V_a - V_o\right\}}{R_{10}} \tag{52}$$

At node B, the voltage-divider equation is[19]:

$$V_a = \frac{R_{12}}{(R_{11} + R_{12})} V_{IN_L} \tag{53}$$

Eliminating Va from equations (52) and (53):[19]

$$V_0 = \frac{R_{10}}{R_9} \frac{\frac{R_{10}}{R_9} + 1}{\frac{R_{11}}{R_{12}} + 1} \left\{V_{IN_L} - V_{IN_R}\right\} \tag{54}$$

Since $R_9 = R_{10} = R_{11} = R_{12}$, equation (54) becomes:

$$V_0 = \frac{1}{1} \cdot \frac{2}{2} \left\{V_{IN_L} - V_{IN_R}\right\} = \left\{V_{IN_L} - V_{IN_R}\right\} \tag{55}$$

5.1.1 Decoder Sensitivity

The transfer function of the decoder may be rewritten as, assuming $(V_{IN_L} - V_{IN_R}) \simeq V_{IN}$:

$$V_0 = \frac{R_{10}}{R_9} \frac{\frac{R_{10}}{R_9} + 1}{\frac{R_{11}}{R_{12}} + 1} V_{IN} = \frac{R_{10}}{R_9} \frac{\frac{(R_{10} + R_9)}{R_9} + 1}{\frac{(R_{11} + R_{12})}{R_{12}}} V_{IN} = \frac{R_{10}}{R_9} \frac{(R_{10} + R_9)}{R_9} \cdot \frac{R_{12}}{(R_{11} + R_{12})} V_{IN} \tag{57}$$

$$\frac{V_0}{V_{IN}} = \frac{R_{10}R_{12}(R_9+R_{10})}{R_9^2(R_{11}+R_{12})} \tag{58}$$

$$S_{R_9}^T = \frac{dT/T}{dR_9/R_9} = \frac{R_9}{T}\frac{dT}{dR_9} = \frac{R_9^3(R_{11}+R_{12})}{R_{10}R_{12}(R_9+R_{10})} \cdot$$

$$\frac{R_9^2(R_{11}+R_{12})R_{10}R_{12} - R_{10}R_{12}(R_9+R_{10})2R_9(R_{11}+R_{12})}{|R_9^2(R_{11}+R_{12})||R_9^2(R_{11}+R_{12})|}$$

$$S_{R_9}^T = \frac{R_9^2(R_{11}+R_{12})R_{10}R_{12} - 2R_9R_{10}R_{12}(R_9+R_{10})(R_{11}+R_{12})}{R_9R_{10}R_{12}(R_9+R_{10})(R_{11}+R_{12})}$$

$$S_{R_9}^T = \frac{R_9^2R_{10}+R_{12} - 2R_9R_{10}R_{12}(R_9+R_{10})}{R_9R_{10}R_{12}(R_9+R_{10})} = \frac{R_9}{(R_9+R_{10})} - 2$$

$$S_{R_9}^T = \frac{R_9}{(R_9+R_{10})} - 2$$

Since $R_9 = R_{10}$,

$$S_{R_9}^T = \frac{1}{2} - 2 = \frac{-3}{2}$$

$$S_{R_{10}}^T = \frac{dT/T}{D_{10}/R_{10}} = \frac{R_{10}}{T} \cdot \frac{dT}{dR_{10}} = \frac{R_9^2R_{10}(R_{11}+R_{12})}{R_{10}R_{12}(R_9+R_{10})} \circ$$

$$\frac{R_9^2(R_{11}+R_{12})(R_9R_{12}+2R_{10}R_{12})0}{|R_9^2(R_{11}+R_{12})||R_9^2(R_{11}+R_{12})|}$$

$$S_{R_{10}}^T = \frac{R_9^3R_{12}(R_{11}+R_{12}) + 2R_9^2R_{10}R_{12}(R_{11}+R_{12})}{R_{12}(R_9+R_{10})R_9^2(R_{11}+R_{12})} = \frac{R_9R_{12}+2R_9^2R_{10}R_{12}}{R_9^2R_{12}(R_9+R_{10})}$$

$$S_{R_{10}}^T = \frac{R_9}{(R_9+R_{10})} + \frac{2R_{10}}{(R_9+R_{10})}$$

Since $R_9 = R_{10}$,

$$S_{R_{10}}^T = \frac{1}{2} + 1 = \frac{3}{2}$$

$$S^T_{R_{11}} = \frac{dT/T}{dR_{11}/R_{11}} = \frac{R_{11}}{T} \cdot \frac{dT}{dR_{11}} = \frac{R_9^2 R_{11}(R_{11}+R_{12})}{R_{10}R_{12}(R_9+R_{10})}.$$

$$\frac{R_9^2(R_{11}+R_{12})(0) - R_{10}R_{12}(R_9R_{10})R_9^2}{[R_9^2(R_{11}+R_{12})][R_9^2(R_{11}+R_{12})]}$$

$$S^T_{R_{11}} = \frac{-R_9^2 R_{10}R_{11}R_{12}(R_9+R_{10})}{R_{10}R_{12}(R_9+R_{10})[R_9^2(R_{11}+R_{12})]} = \frac{-R_9^2 R_{11}(R_9R_{10})}{R_9^2(R_9+R_{10})(R_{11}+R_{12})}$$

$$S^T_{R_{11}} = \frac{-R_{11}}{(R_{11}+R_{12})}$$

Since $R_{11} = R_{12}$,

$$S^T_{R_{11}} = \frac{-1}{2}$$

$$S^T_{R_{12}} = \frac{dT/T}{dR_{12}/R_{12}} = \frac{R_{12}}{T} \cdot \frac{dT}{dR_{12}} = \frac{R_{12}R_9^2(R_{11}+R_{12})}{R_{10}R_{12}(R_9+R_{10})}$$

$$\left| \frac{[R_9^2(R_{11}+R_{12})]R_{10}(R_9+R_{10})}{[R_9^2(R_{11}+R_{12})][R_9^2(R_{11}+R_{12})]} - \frac{R_{10}R_{12}(R_9+R_{10})R_9^2}{[R_9^2(R_{11}+R_{12})][R_9^2(R_{11}+R_{12})]} \right|$$

$$S^T_{R_{12}} = \frac{[R_9^2(R_9+R_{10})(R_{11}+R_{12}) - R_9^2 R_{12}(R_9+R_{10})]}{(R_9+R_{10})[R_9^2(R_{11}+R_{12})]}$$

$$S^T_{R_{12}} = \frac{[R_9^2(R_{11}+R_{12}) - R_9^2 R_{12}]}{R_9^2(R_{11}+R_{12})} = \frac{(R_{11}+R_{12}) - R_{12}}{(R_{11}+R_{12})}$$

$$S^T_{R_{12}} = 1 - \frac{R_{12}}{(R_{11}+R_{12})}$$

Since $R_{11} = R_{12}$,

$$S^T_{R_{12}} = 1 - \frac{1}{2} = \frac{1}{2}$$

5.2 Low-Pass Filter (with fc = 7000 Hz)

Very high frequency sounds are directional[5]. In live performances, high-frequency sounds are heard when the listener is on-axis with the high frequency source. A low-pass filter is used to roll-off the high frequencies for the rear channels of the surround-sound system. The schematic of the 7000 Hz low-pass filter is shown in Figure 22.

This is the same Sallen and Key low-pass filter circuit as used in the bass-enhancer system. Refer to section 4.2, and section 4.2.1, for the derivation of the transfer function and the sensitivity characteristics of the Sallen and Key voltage-controlled voltage-source low-pass filter.

$$K = \left\{1 + \frac{R_A}{R_B}\right\} \tag{28}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{K}{R_{13}R_{14}C_5C_6}}{\left\{S^2 + \left|\dfrac{1}{C_5R_{14}} + \dfrac{1}{C_6R_{14}} + \dfrac{1}{C_6R_{13}} - \dfrac{K}{C_5R_{14}}\right| S + 1\right\}} \tag{59}$$

5.2.1 Sensitivity of Low-Pass Filter

$$S_{K_0}^T = \frac{(R_{13}R_{14}C_5C_6S^2 + R_{13}C_6S + R_{13}C_5S + R_{14}C_5S + 1)}{(R_{13}R_{14}C_5C_6S^2 + R_{13}C_6S + R_{13}C_5S + R_{14}C_5S - K_0R_{13}C_6S + 1)}$$

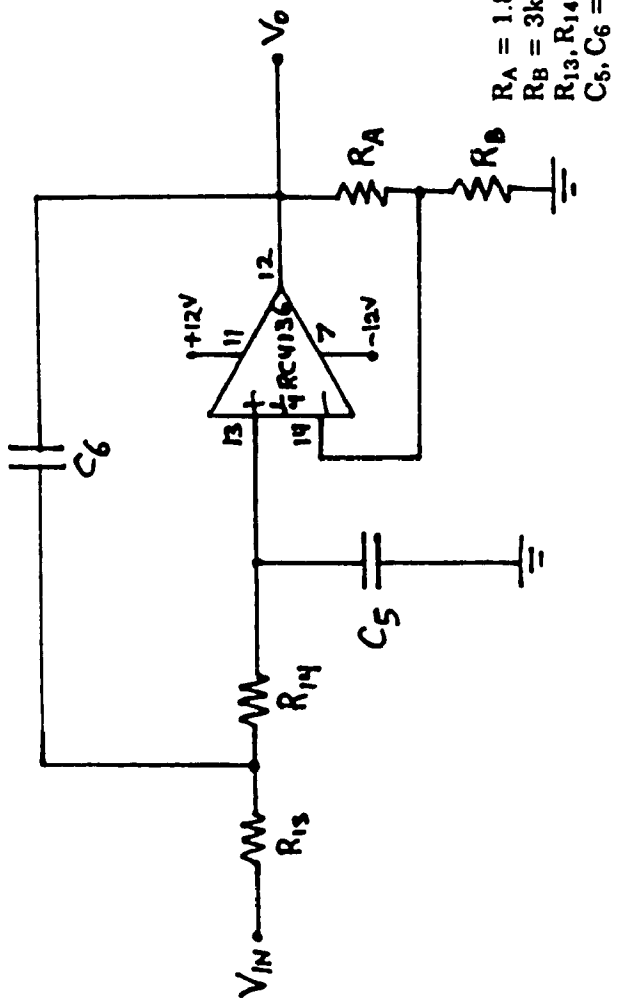


Figure 22 Schematic of Low-Pass Filter
(fc = 7000 Hz)

As $K_0 \to \infty$,

$S^T_{K_0} \to 0$

$$S^T_{C_5} = \frac{(-R_{13}R_{14}C_5C_6S^2 - R_{13}C_5S - R_{14}C_5S)}{(R_{13}R_{14}C_5C_6S^2 + R_{13}C_6S + R_{13}C_5S + R_{14}C_5S - K_0R_{13}C_6S + 1)}$$

As $K_0 \to \infty$,

$S^T_{C_5} \to 0$

$$S^T_{C_6} = \frac{(-R_{13}R_{14}C_5C_6S^2 - R_{13}C_6S + KR_{13}C_6S)}{(R_{13}R_{14}C_5C_6S^2 + R_{13}C_6S + R_{13}C_5S + R_{14}C_5S - KR_{13}C_6S + 1)}$$

As $K_0 \to \infty$,

$S^T_{C_6} \to -1$

$$S^T_{R_{13}} = \frac{(-R_{13}R_{14}C_5C_6S^2 - R_{13}C_6S - R_{13}C_5S + KR_{13}C_6S)}{(R_{13}R_{14}C_5C_6S^2 + R_{13}C_6S + R_{13}C_5S + R_{14}C_5S - KR_{13}C_6S + 1)}$$

As $K_0 \to \infty$,

$S^T_{R_{13}} \to -1$

$$S^T_{R_{14}} = \frac{(-R_{13}R_{14}C_5C_6S^2 - R_{14}C_5S)}{(R_{13}R_{14}C_5C_6S^2 + R_{13}C_6S + R_{13}C_5S + R_{14}C_5S - KR_{13}C_6S + 1)}$$

As $K_0 \to \infty$,

$S^T_{R_{14}} \to 0$

It is also noted that:

As $K_0 \to \infty$,

$$\frac{V_{OUT}}{V_{IN}} \to \frac{-1}{R_{13}C_6S}$$

Equation (59) is of the form:

$$\frac{V_{OUT}}{V_{IN}} = \frac{V_2}{V_1} = \frac{K/w_p^2}{S^2 + S\frac{Wp}{Qp} + w_p^2} \tag{35}$$

which is the standard form for a second-order low-pass active filter[16]. Comparing (59) and (35) yields:

$$w_p = \frac{1}{\sqrt{R_{13}R_{14}C_5C_6}} \tag{36}$$

Let

$$a = \left| \frac{1}{R_{14}C_5}(1-K) + \frac{1}{R_{14}C_6} + \frac{1}{R_{13}C_6} \right|$$

$$Hence\, a = \frac{w_p}{Qp} \; or \; Qp = \frac{w_p}{a}$$

$$Qp = \frac{1}{\frac{\sqrt{R_{13}R_{14}C_5C_6}}{R_{14}C_5}(1-K) + \frac{\sqrt{R_{13}R_{14}C_5C_6}}{R_{14}C_6} + \frac{\sqrt{R_{13}R_{14}C_5C_6}}{R_{14}C_6}} \tag{61}$$

By normalizing,

$$R_{13} = R_{14} = 1\Omega \; and \; C_5 = C_6 = 1F$$

The w_p and Qp are: [17]

$$S_{R_{13}}^{Wp} = \frac{1}{2}$$

$$S_{R_{14}}^{Wp} = -\frac{1}{2}$$

$$S_{C_5}^{Wp} = -\frac{1}{2}$$

$$S_{C_6}^{Wp} = -\frac{1}{2}$$

$$S_K^{Wp} = 0$$

$$S_{R_{13}}^{Qp} = -S_{R_{14}}^{Qp} = \left| Qp \frac{\sqrt{R_{14}C_6}}{\sqrt{R_{13}C_5}} - \frac{1}{2} \right| = 0.207$$

$$S_{C_5}^{Q} = -S_{C_6}^{Q} = Qp \frac{\sqrt{C_6}}{\sqrt{C_5}} \left\{ \frac{\sqrt{R_{13}}}{\sqrt{R_{14}}} + \frac{\sqrt{R_{14}}}{\sqrt{R_{13}}} \right\} - \frac{1}{2} = 0.914$$

$$S_K^Q = Qp \left| \frac{\sqrt{R_{13}C_5}}{\sqrt{R_{14}C_6}} + \frac{\sqrt{R_{14}C_6}}{\sqrt{R_{13}C_5}} + \frac{\sqrt{R_{13}C_6}}{\sqrt{R_{14}C_5}} \right| - 1 = 1.121$$

5.2.2 Low-Pass Filter Performance

The equal component design was used for this filter, that is, $R_{13} = R_{14}$ and $C_5 = C_6$ as shown in Figure 22. This is a second order low-pass filter, hence α, the damping factor of a Butterworth filter, is $\alpha = 1.414$[18].

$$Let\, C_5 = C_6 = 0.001 \mu F$$

The frequency scale is given by

$$a = 2\pi fc = 6\,283 \times 7 \times 10^3 = 43\,981$$

The impedance scale is given by

$$C_1 = \frac{C_1^*}{ab} \text{ or } b = \frac{C_1^*}{C_1 a} \text{ where } C_1^* = 1F$$

where

$$C_1^* = 1F$$

Thus,

$$b = \frac{1}{0.001 \times 10^{-6} \times 43{,}981} = \frac{1 \times 10^6}{43.981} = 22737\Omega$$

$$Hence\ R_{13} = R_{14} = 22000\Omega\ (nearest\ standard\ value)$$

By normalizing,

$$R_{13} = R_{14}\,1\Omega\ and\ C_5 = C_6 = 1F.,\ then\ equation\ (59)\ becomes:$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{K}{(S^2 + |3-K|S + 1)} \tag{62}$$

Comparing equation (35) and equation (62):

$$K = G(3 - \alpha) = \left\{1 + \frac{RA}{RB}\right\} or \frac{RA}{RB} = (2 - \alpha) = 0.586$$

Hence,

R_A = 0.586 R_B. Let us try R_B = 3000Ω.

R_A = 1758Ω. Nearest standard value R_B used is 1800Ω.

The damping factor, α and the theoretical frequency response were derived in section 4.2.2. The nomalized theoretical frequency response of the filter is:

$$20\log_{10}|T(jw)| = 20\log_{10}K - 20\log_{10}(W^4 + 1)^{\frac{1}{2}} \tag{40}$$

The resulting curve is shifted by the frequency scale a. The theoretical values of the actual filter are obtained using w* = aw, where w* is the scaled quantity. Table 5 lists the actual and design performance of the low-pass filter. For this filter, a = 43981 and gain K = 1.5986. Figure 23 is the frequency-response plot of the low-pass filter. The phase-response plot is shown in Figure 24.

5.3 Rear Channel Gain Control

The rear channel gain control is a potentiometer voltage divider as shown in Figure 25. The potentiometer is selected so that neither the output of the decoder circuit nor the input of time-delay circuit are loaded. The input impedance of the time-delay circuit is 5000Ω[20] and the output impedance of the decoder circuit is of the order of 100Ω [21].

The potentiometer must be at least ten times the resistance of the higher of the two connecting stages. Let X be resistance of circuit to be matched. Thus R_{P_2} > 50 000Ω.

$$R_{P_2} > 10X \tag{63}$$

$$R_{P_2} > 10X\,(63)\; R_{NET} = \frac{10X.X}{(10X+X)} = \frac{10X^2}{11X} = \frac{10}{11}X \doteq 0.91X \tag{64}$$

The transfer function of the rear channel gain control is:

$$V_{OUT} = \frac{R_{P_{2B}}}{(R_{P_{2A}})}\,V_{IN} \tag{65}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_{P_{2B}}}{(R_{P_{2A}} + R_{P_{2B}})} \tag{66}$$

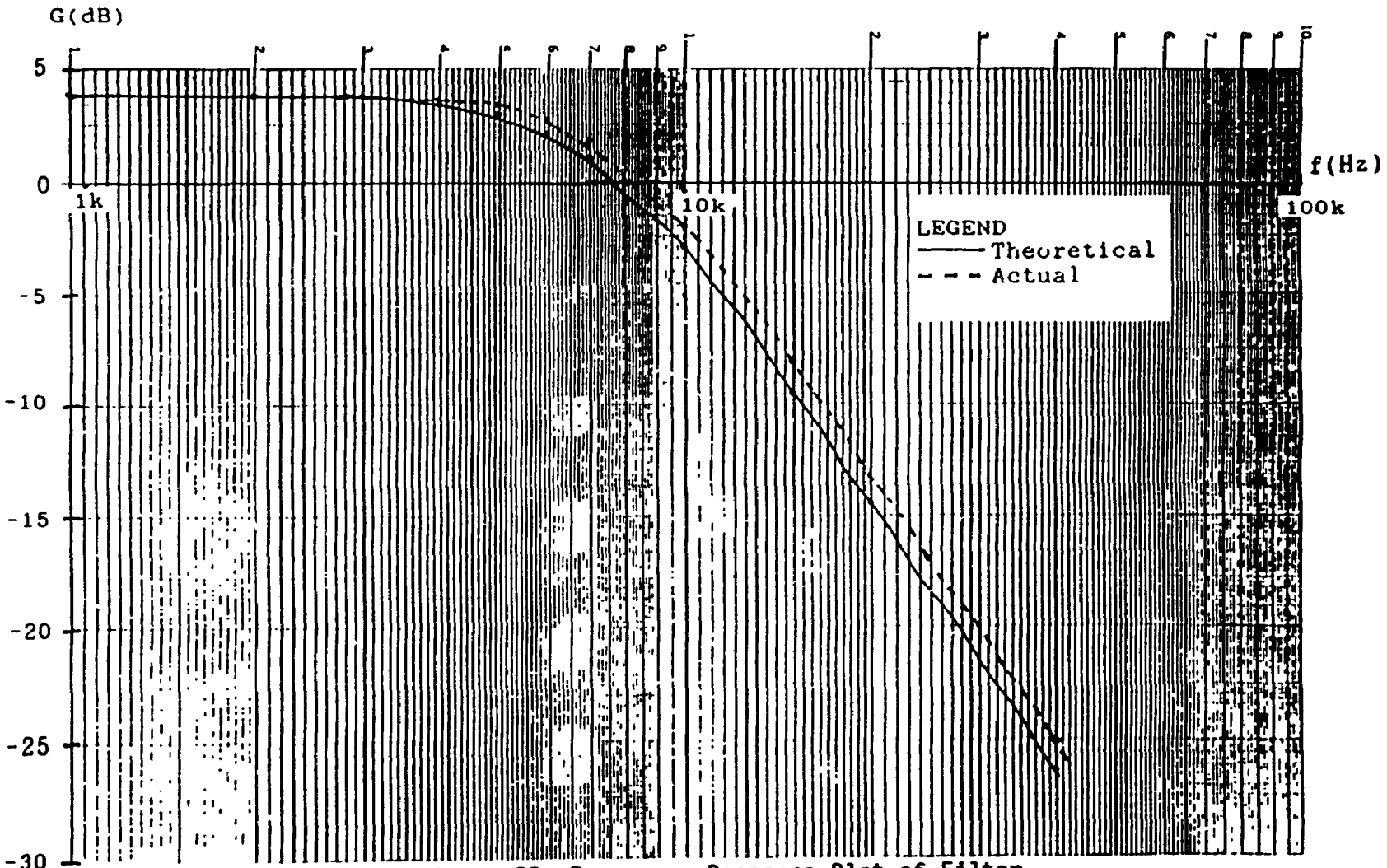


Figure 23 Frequency-Response Plot of Filter
(fc = 7000 Hz)

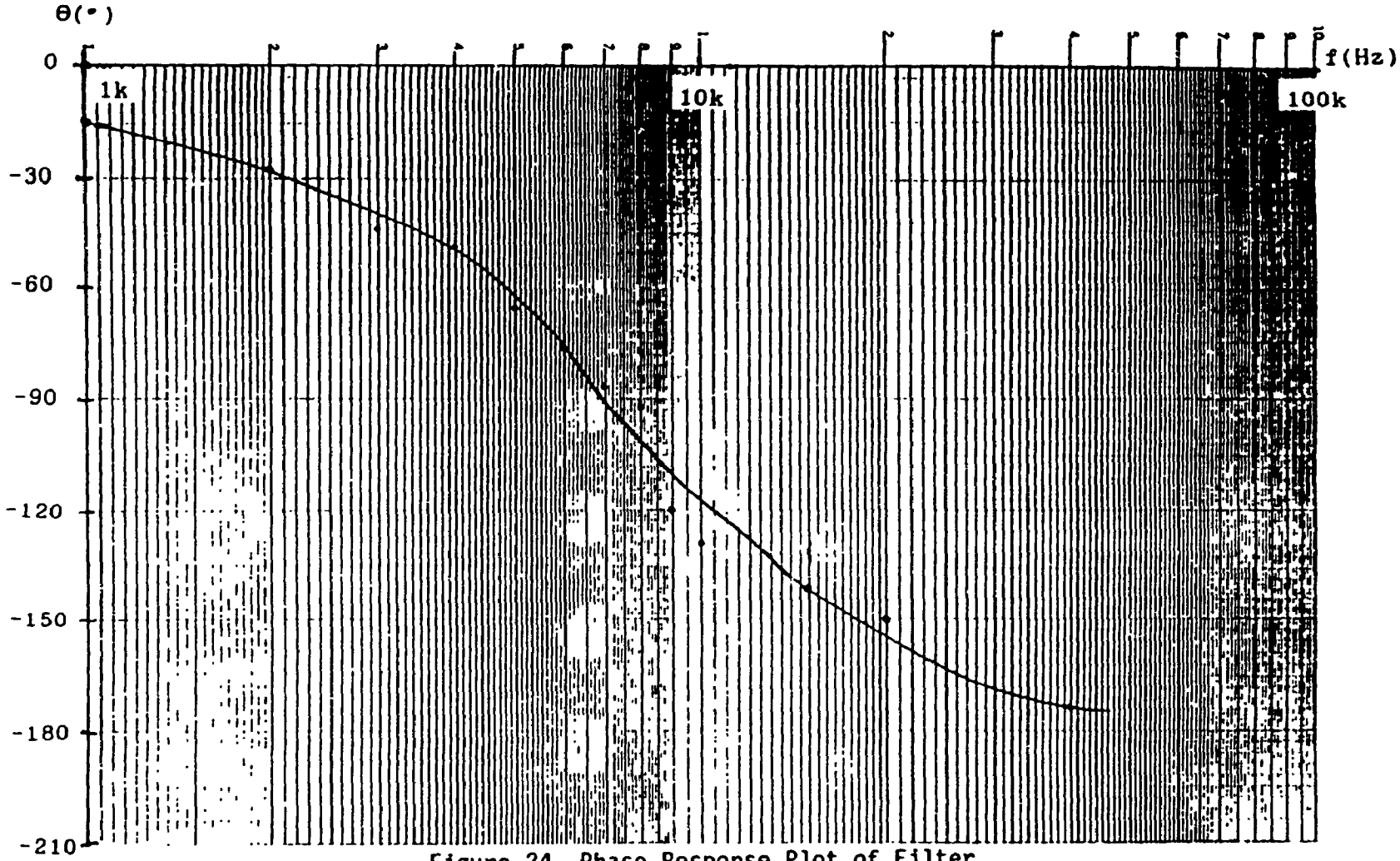


Figure 24 Phase-Response Plot of Filter
(fc = 7000 Hz)

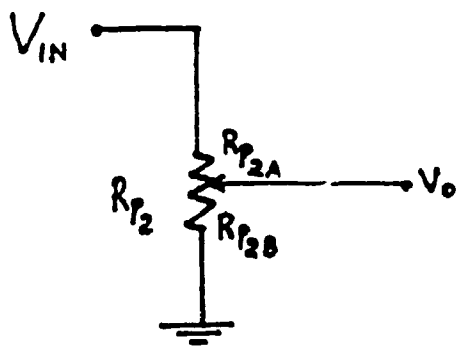


Figure 25 Rear Channel Gain Control

5.4 Decoder System

The complete decoder system is shown in Figure 26. The decoder generates a rear channel signal from regular stereo sources and it decodes Dolby encoded sources such as movies and soundtracks. The frequency-response plot is the same as that of the low-pass filter which is shown in Figure 23 because the decoder is a unity-gain circuit. Refer to Figure 20.

Table 5 Low-Pass Filter (f_c = 7000 Hz) Performance Data

			Theoretical	Actual Data				
w (rad/s)	aw (rad/s)	F (Hz)	G(dB)	V_{IN} (Vp-p)	V_{OUT} (Vp-p)	$\varnothing_{OUT}$ (°)	G	G (dB)
0.1429	6,283	1,000	4.00	2.0	3.20	-14.4	1.60	4.08
0.2857	12,566	2,000	3.98	2.0	3.20	-28.8	1.60	4.08
0.4286	18,849	3,000	3.86	2.0	3.20	-43	1.60	4.08
0.5714	25,132	4,000	3.57	2.0	3.10	-50	1.55	3.81
0.7143	31,415	5,000	3.00	2.0	3.00	-65	1.50	3.52
0.8571	37,698	6,000	2.13	2.0	2.75	-76.5	1.375	2.77
1.000	43,981	7,000	1.00	2.0	2.45	-86	1.225	1.76
1.1429	50,264	8,000	-0.32	2.0	2.00	-92	1.0	0.00
1.2857	56,547	9,000	-1.71	2.0	1.75	-120	0.875	-1.16
1.4286	62,830	10,000	-3.12	2.0	1.60	-130	0.80	-1.94
2.1429	94,245	15,000	-9.44	2.0	0.80	-140	0.40	-7.96
2.8571	125,669	20,000	-14.30	2.0	0.44	-150	0.22	-13.15
5.7143	251,320	40,000	-26.28	2.0	0.11	-173	0.055	-25.19

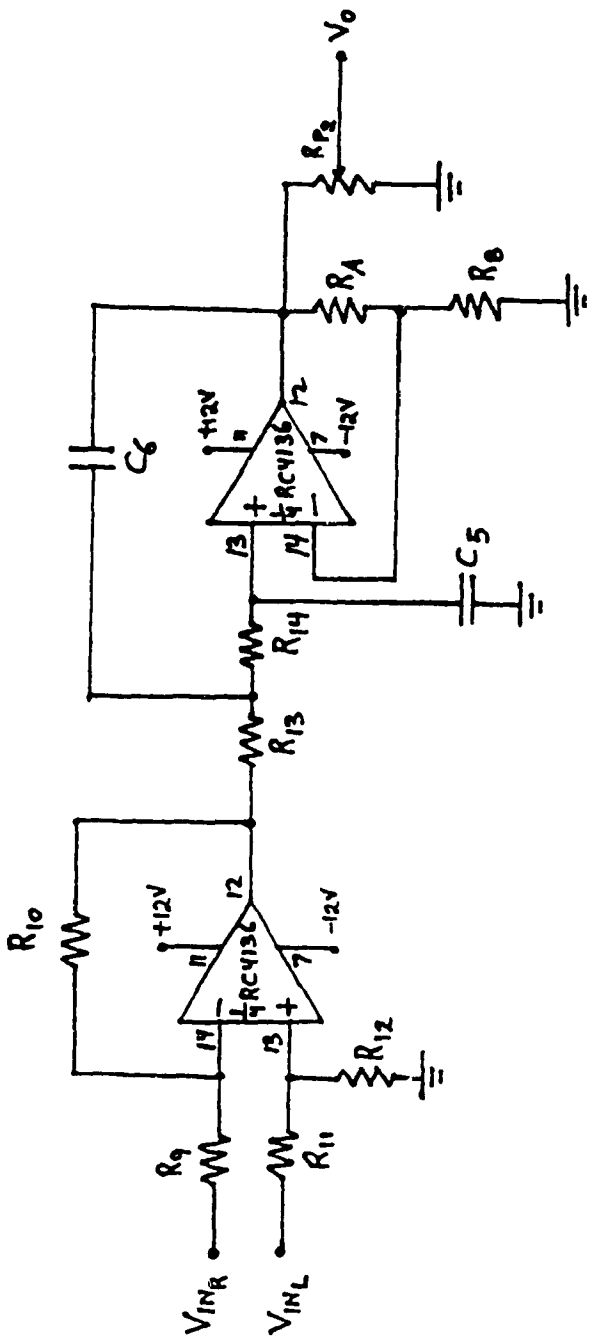


Figure 26 Schematic of Decoder System

CHAPTER 6

AUDIO TIME DELAY

The audio time-delay generator consists of an analog-to-digital converter, eight 192-stage shift registers, a digital-to-analog converter and a low-pass filter, as shown in Figure 27. The time delay is denoted by T and is in the range of 15 to 20 ms.

The analog-to-digital converter converts analog signals into eight-bit digital data. The 192-stage shift registers shift the data in time by 192 clock pulses. The digital-to-analog converter converts the eight-bit digital data into an analog signal from which the low-pass filter removes the high frequency components.

6.1 Analog-to-Digital Converter

The ADC0804 analog-to-digital converter was chosen because it is a successive approximation converter[22]. Successive approximation is a fast way to convert analog into digital data. Each conversion requires from one to eight clock pulses[22].

In successive approximation, successive guesses of the input signal are made in a systematic way[23]. The first guess is 80_H which sets the DAC output to half scale[23]. If 80_H is less than the input, bit D7 is held high[23]. However, if 80_H is greater than the input

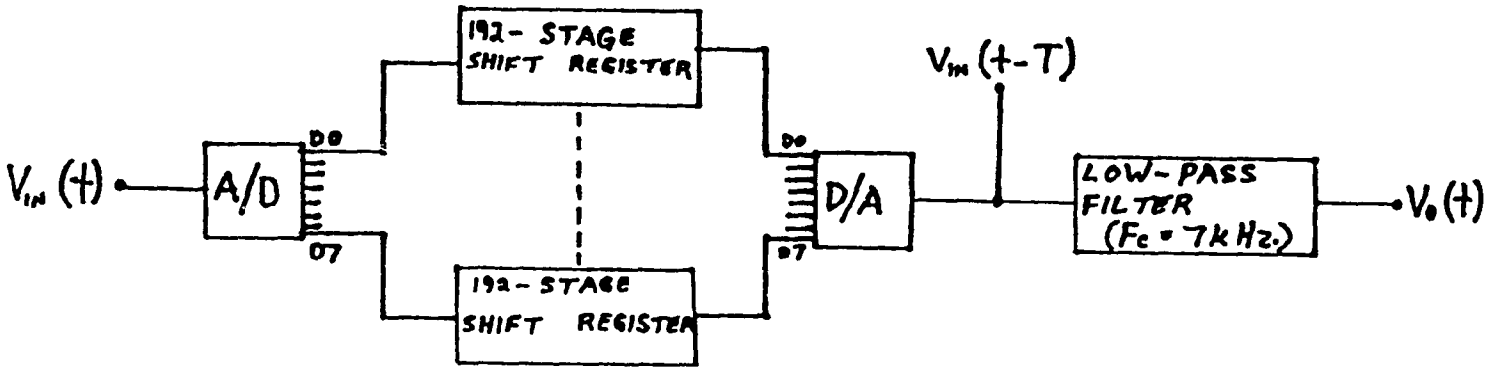


Figure 27 Block Diagram of Time Delay Circuit

signal, bit D7 is set to low[23]. The next bit is set high and this number is tried[23]. This protocol is followed for the remaining bits while resetting the last bit tried if the digital value is greater than the input and setting it high if the digital values is less than the input[23]. Figure 28 illustrates this more clearly.

The ADC0804 tests the most significant bit first and after 64 clock pulses a digital 8-bit code is transferred to an output latch and the $\overline{\text{INTR}}$ pin goes low, indicating a completed conversion[22]. The converter is operated in a continuous conversion mode by connecting the $\overline{\text{INTR}}$ and $\overline{\text{WR}}$ pins together and holding the $\overline{\text{CS}}$ pin low[22]. To ensure start-up, an external WR pulse is required at power-up[22]. The successive-approximation register is cleared as the $\overline{\text{WR}}$ input goes low, when $\overline{\text{CS}}$ is low[22].

Conversion begins one to eight clock pulses after either $\overline{\text{WR}}$ or $\overline{\text{CS}}$ inputs or both inputs go high[22]. The $\overline{\text{INTR}}$ line goes high when the conversion starts[22]. The $\overline{\text{INTR}}$ line remains low until one to eight clock periods after either the $\overline{\text{WR}}$ or the $\overline{\text{CS}}$ input, or both, go high[22]. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs are brought low to read the data, the $\overline{\text{INTR}}$ line will go low, thus enabling the three-state output latches[22]. Figure 29 is a block diagram of the ADC0804.

Since it takes one to eight clock periods for the conversion cycle, [22] the conversion time is:[24]

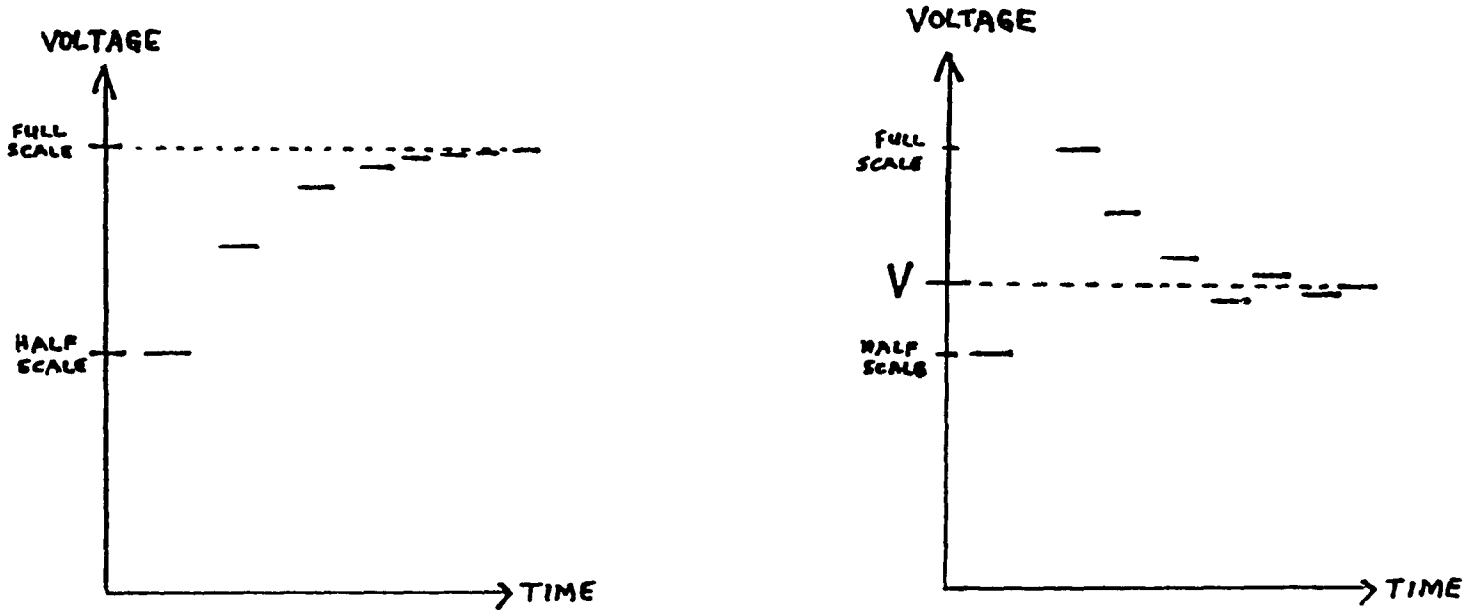


Figure 28 Successive Approximation Method[23]

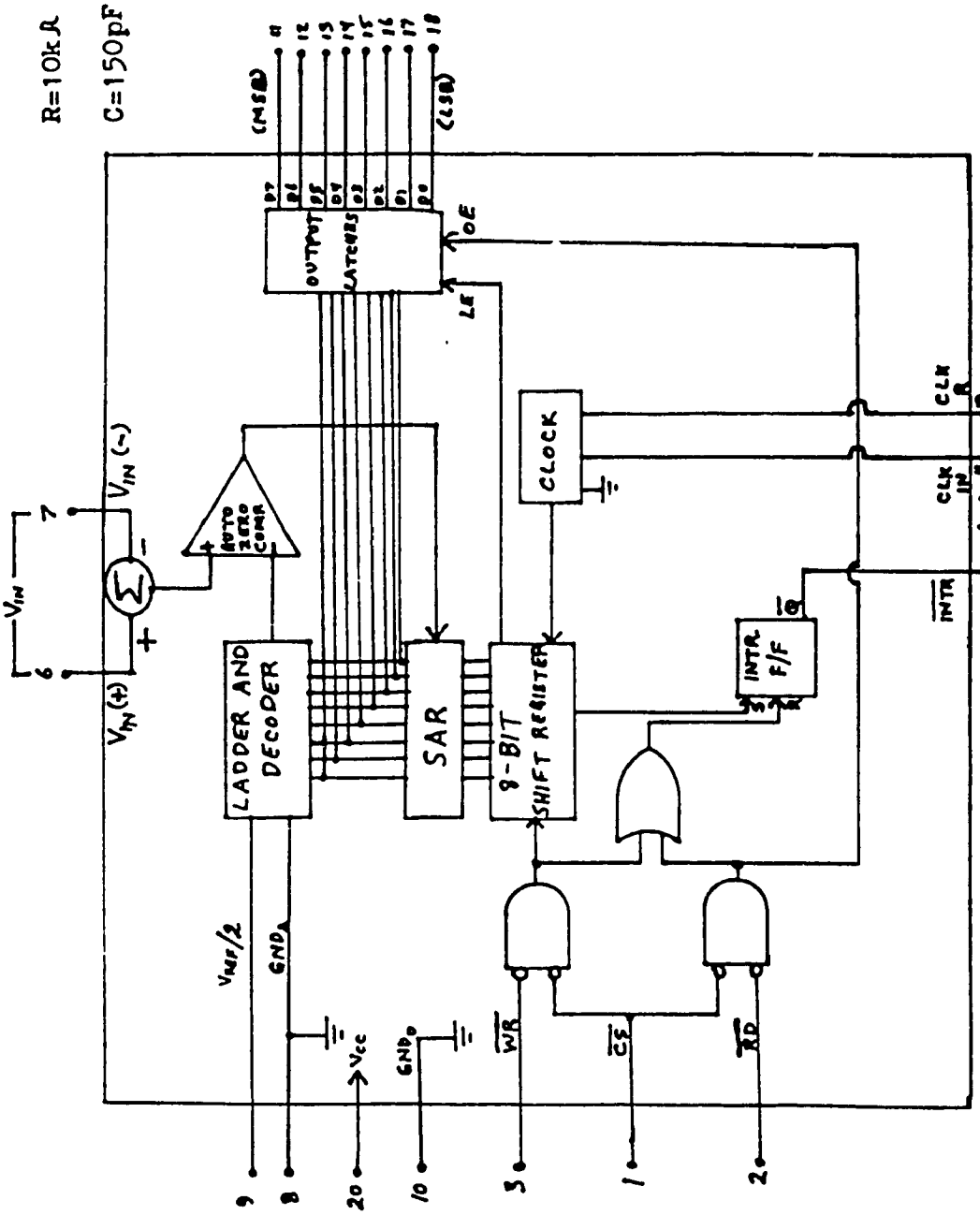


Figure 29 Block Diagram of ADC0804[22]

$$T_{c.p} \leq tc \leq 8T_{c.p.} \tag{67}$$

The maximum number of samples per second is [24]

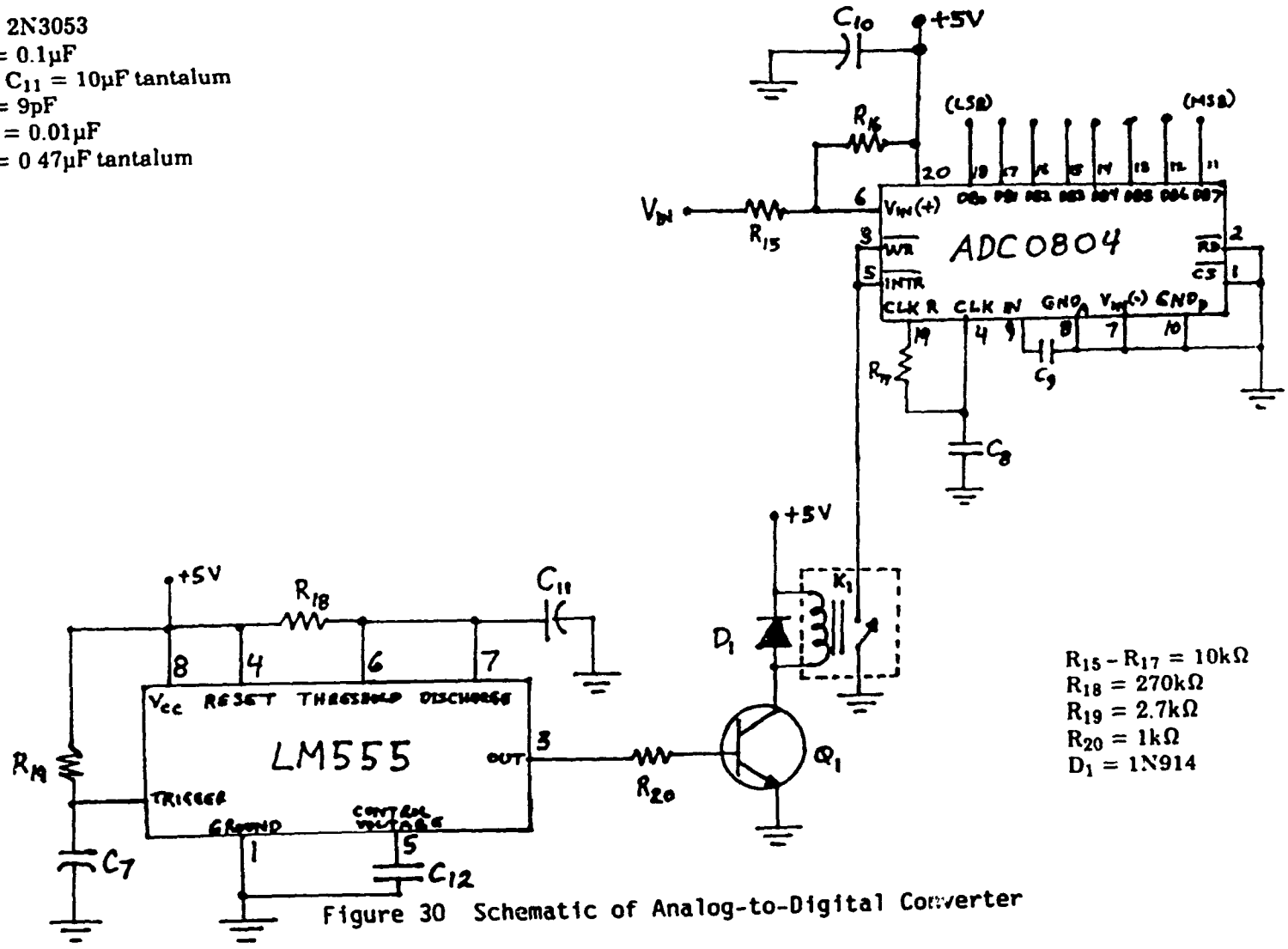
$$F_{s_{max}} = \frac{1}{t_c} \tag{68}$$

The schematic of the analog-to-digital converter is shown in Figure 30.

6.1.1 Analog-to-Digital Converter Circuit Operation

The LM555 timer integrated circuit is used in the monostable mode. The threshold and discharge transistor terminals are connected together[25]. The external capacitor, C_6, is initially discharged by a transistor inside the timer[26]. When a negative trigger pulse of less than $\frac{1}{3}$Vcc is applied to the trigger terminal, the flip-flop is set, which in turn, allows the capacitor, C_6, to charge[25]. The digital output then goes high[25]. The capacitor charges exponentially for a period of $t = 1.1R_4C_6$,(69) at the end of which time the capacitor voltage equals $\frac{2}{3}$Vcc[26]. At this point, the comparator resets the flip-flop which in turn discharges the capacitor and drives the output low[26]. The timing is independent of the power supply because the charge threshold levels of the comparators are directly proportional to the supply voltage[26]. When the output is high, the circuit cannot be retriggered by another trigger pulse[26]. The circuit can be reset during this time by a negative pulse at the reset terminal[26]. When the reset pin is low, the capacitor discharge transistor is turned "on" preventing the capacitor, C_6, from charging[25]. In this application, the reset function is not used, hence the reset pin is connected to the

Q = 2N3053
C_9 = 0.1μF
C_{10}, C_{11} = 10μF tantalum
C_8 = 9pF
C_{12} = 0.01μF
C_7 = 0 47μF tantalum



$R_{15} - R_{17}$ = 10kΩ
R_{18} = 270kΩ
R_{19} = 2.7kΩ
R_{20} = 1kΩ
D_1 = 1N914

Figure 30 Schematic of Analog-to-Digital Converter

power supply. A block diagram of the LM555 timer integrated circuit is shown in Figure 31.

Transistor Q_1 is used as a switching buffer between the timer integrated circuit and the relay K_1. Resistor R_{20} is a current-limiting resistor, and diode D_1, prevents any negative inductive voltage spikes that may be generated by the relay coil from destroying transistor Q_1. When the output pin of the timer is high, the collector of the transistor goes low and the relay coil is energized. The relay switch is closed and the $\overline{WR}$ and $\overline{INTR}$ pins of the analog-to-digital converter are held low for about half a second. Continuous conversion begins one to eight clock, periods after the relay is de-energized. The analog-to-digital converter then operates as described in section 6.1.

The analog-to-digital converter is operated in the bipolar mode with resistors R_{15} and R_{16} in place as shown in Figure 30[20]. The input signal from the decoder system is a bipolar voltage.

6.1.2 Analog-to-Digital Converter Performance

From equation (69), $t = 1.1 \times 270 \times 10^3 \times 10 \times 10^{-6}$ $t = 2.97s$. From oscilloscope readings t = 6.2 div. x 0.5 sec/div. = 3.1s. Relevant waveforms of the WR pulse generator and analog-to-digital converter are shown in Figure 32. The relay used requires 72mA at the five volts to energize its coil. The base drive to the transistor is 5×10^{-3}A. Hence, a transistor with $\beta = 72/5 = 14.4$ is required.

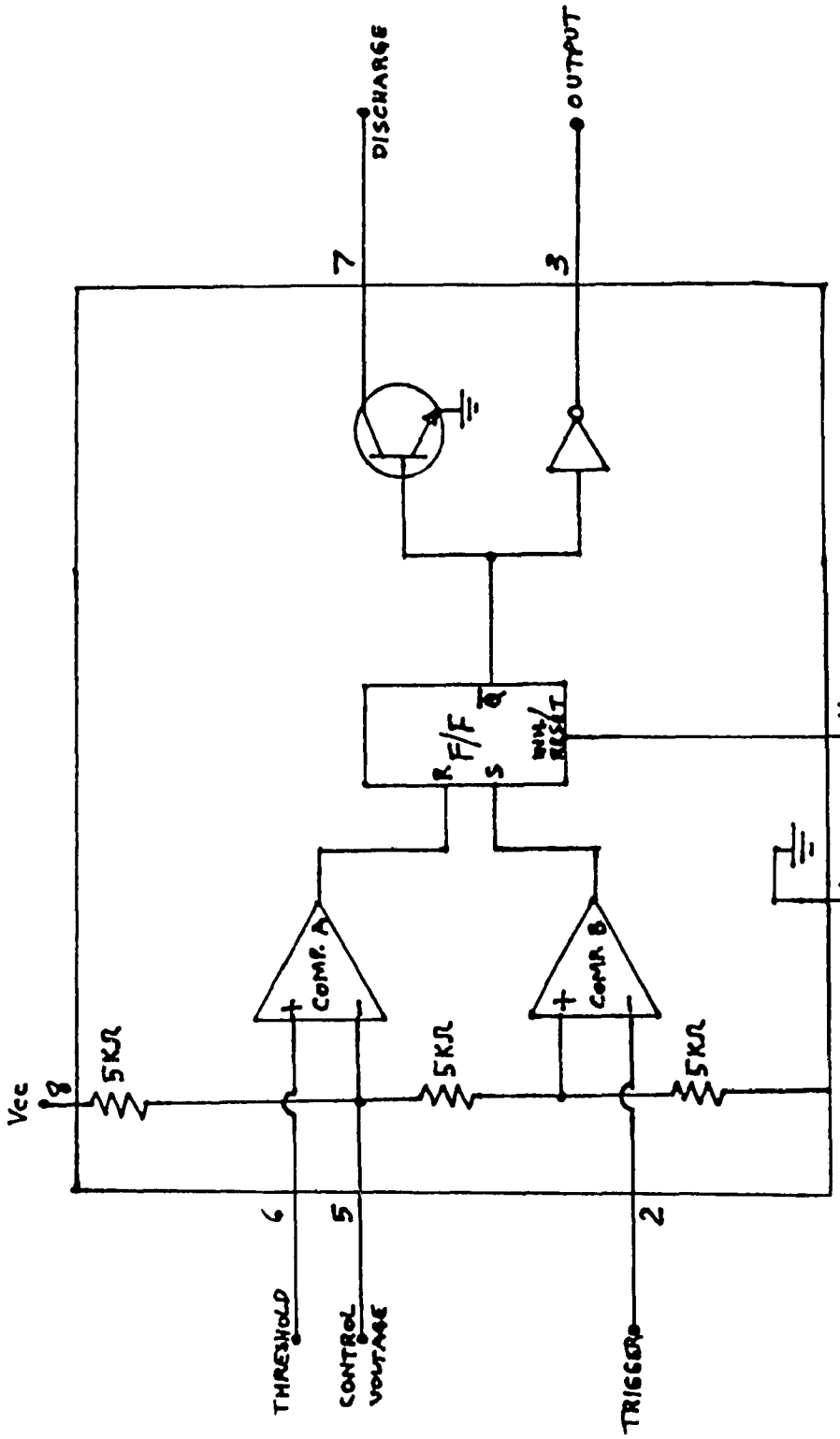


Figure 31 Block Diagram of Timer[25]

$$\beta = \frac{I_{COLLECTOR}}{I_{BASE}} = \frac{72 \times 10^{-3}}{5 \times 10^{-3}} = 14.4 \qquad (70)$$

The transistor dissipates no power. $P_D = I_C V_{CE}$[71]. Referring to Figure 30:

$$t \leq 3.1 \text{ sec:}$$

$$P_D = 72 \times 10^{-3} \times 0.0 = 0.0W \text{ and } t > 3.1 \text{ sec: } P_D = 0.0 \times 4.0 = 0.0W$$

The 2N3053 transistor was selected for its

$$V_{CE_{MAX}} = 30V., I_{C_{MAX}} = 500 \times 10^{-3} A \text{ and } P_{D_{MAX}} = 360 \times 10^{-3} W \qquad [27]$$

The data for the analog-to-digital converter is shown in Table 6. The resolution of the analog-to-digital converter is the number of discrete steps at the output and is equal to 2^n where n is the number of bits[22]. In this case, the resolution is $2^8 = 256$.

In an analog-to-digital converter, there can be an infinite number of different input voltages, but only 2^n possible output codes[22]. The maximum quantizing error is the difference of the maximum and minimum input levels divided by the resolution of the analog-to-digital converter.

Table 6 Analog-to-Digital Converter Performance Data

V_{IN}(V)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Count Difference	Q_{ERR} (mV_1)*	% error (%)**
4.84	1	1	1	1	1	1	1	1	2	55.00	-41
4.73	1	1	1	1	1	1	0	1	7	35.71	8.4
4.48	1	1	1	1	0	1	1	0	6	38.33	1.7
4.25	1	1	1	1	0	0	0	0	6	38.33	1.7
4.02	1	1	1	0	1	0	1	0	8	36.25	7.1
3.73	1	1	1	0	0	0	1	0	6	36.67	6.0
3.51	1	1	0	1	1	1	0	0	6	38.33	1.7
3.28	1	1	0	1	0	0	1	0	7	40.00	-2.6
3.00	1	1	0	0	1	1	1	1	8	33.75	13.5
2.73	1	1	0	0	0	1	1	1	5	44.00	-12.8
2.51	1	1	0	0	0	0	1	0	8	35.00	10.3
2.23	1	0	1	1	1	0	1	0	7	37.14	4.8
1.97	1	0	1	1	0	0	1	1	5	42.00	-7.7
1.76	1	0	1	0	1	1	1	0	9	34.44	11.7
1.45	1	0	1	0	0	1	0	1	4	40.00	-2.6
1.29	1	0	1	0	0	0	0	1	8	36.25	7.1
1.00	1	0	0	1	1	0	0	1	6	41.67	-6.8
0.75	1	0	0	1	0	0	1	1	7	35.71	8.4
0.50	1	0	0	0	1	1	0	0	13	38.46	1.4
0.25	-	-	-	-	-	-	-	-	-	-	-

$$* Q_{ERR} = \frac{VOLT.\,DIFF.}{COUNT\,DIFF.}$$

$$** \%_{ERR} = \frac{(THEOR. - ACT.)}{THEOR.} = 100\%$$

Table 6 Analog-to-Digital Converter Performance Data (Cont'd)

V_{IN}(V)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Count Difference	Q_{ERR} (mV_1)*	% error (%)**
0.00	0	1	1	1	1	1	1	1	14	36.43	6.6
-0.25	-	-	-	-	-	-	-	-	-	-	-
-0.53	0	1	1	1	0	0	0	1	7	35.71	8.4
-0.78	0	1	1	0	1	0	1	0	6	41.67	-6.8
-1.03	0	1	1	0	0	1	0	0	6	38.33	1.7
-1.26	0	1	0	1	1	1	1	0	8	35.00	10.3
-1.54	0	1	0	1	0	1	1	0	5	42.00	-7.7
-1.75	0	1	0	1	0	0	0	1	6	36.67	[illegible]0
-1.97	0	1	0	0	1	0	1	1	7	37.14	4.8
-2.23	0	1	0	0	0	1	0	0	7	40.00	-2.6
-2.51	0	0	1	1	1	1	0	1	7	38.57	1.1
-2.78	0	0	1	1	0	1	1	0	4	42.50	-9.0
-2.95	0	0	1	1	0	0	1	0	8	35.00	10.3
-3.23	0	0	1	0	1	0	1	0	6	40.00	-2.6
-3.47	0	0	1	0	0	1	0	0	7	41.43	-6.2
-3.76	0	0	0	1	1	1	0	1	6	36.67	6.0
-3.98	0	0	0	1	0	1	1	1	7	34.29	12.1
-4.22	0	0	0	1	0	0	0	0	6	41.67	-6.8
-4.47	0	0	0	0	1	0	1	0	8	36.25	7.1
-4.76	0	0	0	0	0	0	1	0	2	85	-117.9
-4.93	0	0	0	0	0	0	0	0	-	-	-

$$*Q_{ERR} = \frac{VOLT\ DIFF.}{COUNT\ DIFF.}$$

$$** \%_{ERR} = \frac{(THEOR. - ACT.)}{THEOR.} = 100\%$$

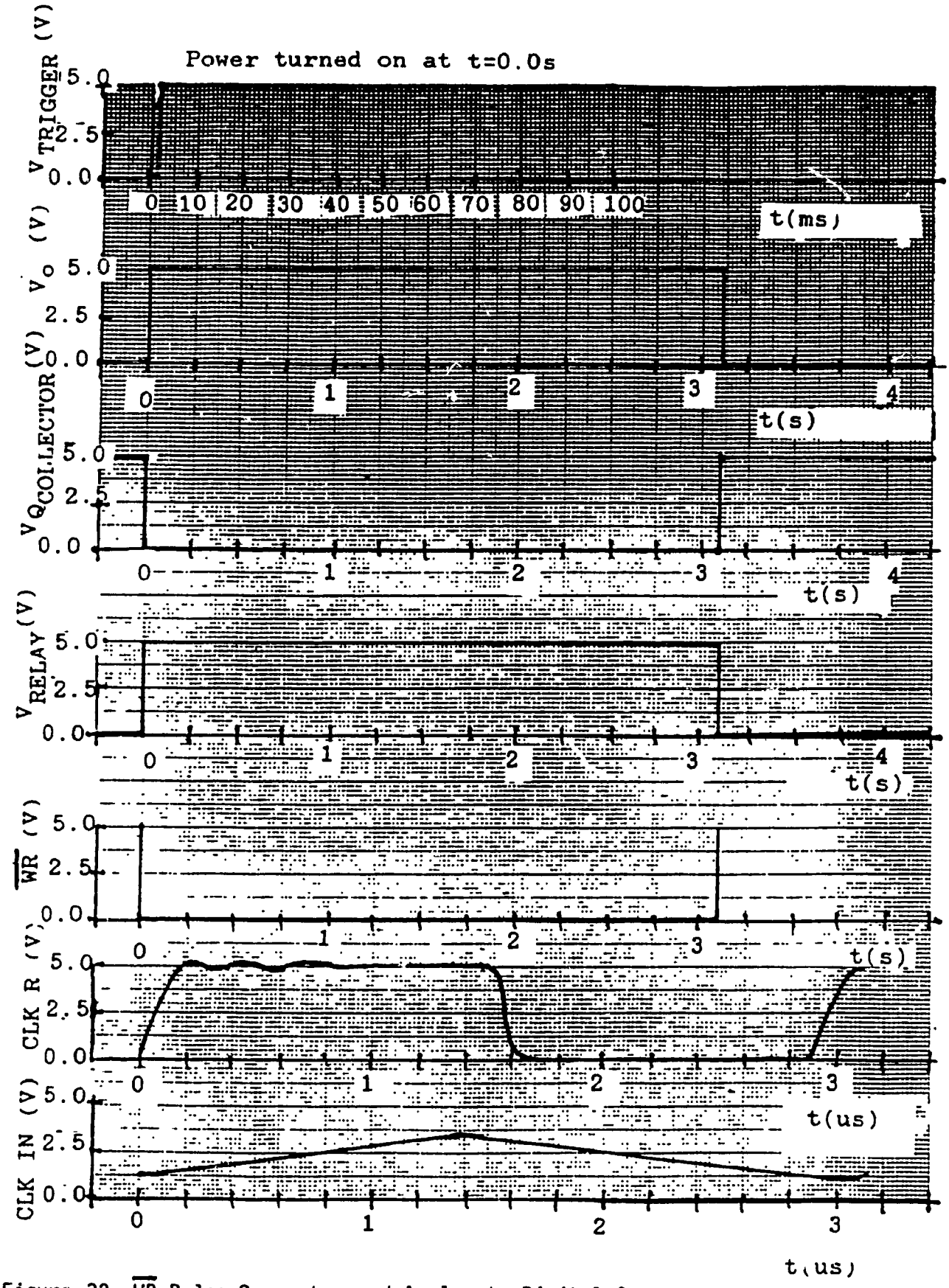


Figure 32 $\overline{WR}$ Pulse-Generator and Analog-to-Digital Converter Waveforms

$$Q_{ERR_{MAX}} = \frac{\left\{V1N_{MAX} - V1N_{MIN}\right\}}{RESOLUTION} \tag{71}$$

$$Q_{ERR_{MAX}} = \frac{(5 - -5)}{256} = \frac{10}{256} = 39 x 10^{-3} V$$

This agrees closely with the values obtained, see Table 6.

The clock period of the analog-to-digital converter is: $T_{CLK} = 2.88 \times 10^{-6}$s, see Figure 30.

From equation (67), the conversion time is:

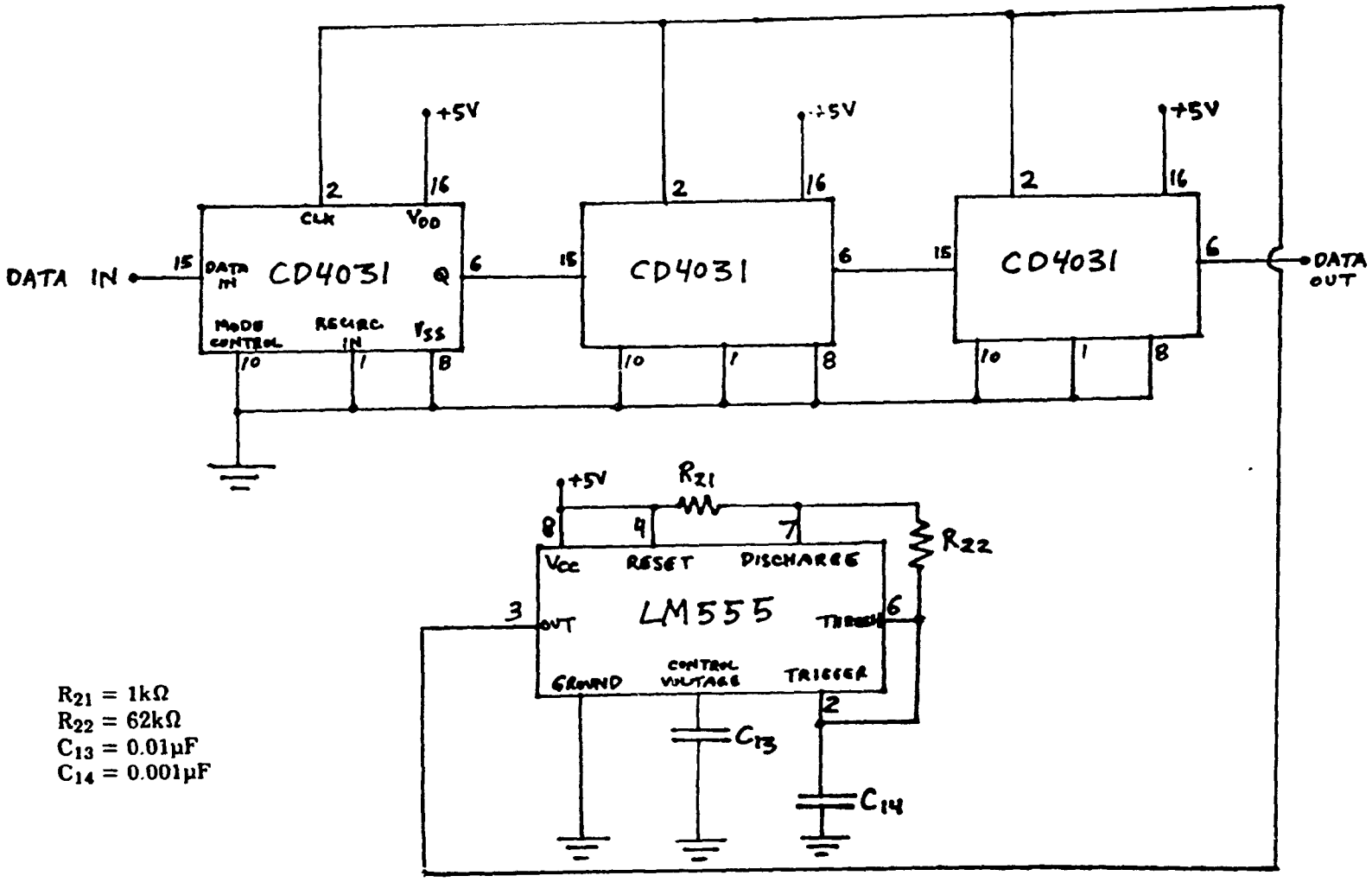
$$2.88 x 10^{-6} s \leq t_c \leq 23.04 x 10^{-6} s$$

From equation (68), the maximum number of samples per second is:

$$43\,403 Hz \leq F_{s_{MAX}} \leq 347\,222 Hz$$

6.2 Time-Delay Circuit

Each data bus goes through a time-delay circuit as shown in Figure 33. The CD4031 is a 64-stage static shift register in which each stage is a D-type flip-flop[28]. The data level at the input is transferred into the first stage after the first positive-going clock transition[28]. It is then shifted one stage at each positive-going clock transition[28]. After 64 clock pulses, the data appears at the



$R_{21} = 1k\Omega$
$R_{22} = 62k\Omega$
$C_{13} = 0.01\mu F$
$C_{14} = 0.001\mu F$

Figure 33 Time-Delay Circuit

output of the 64th stage[28]. The recirculating mode is not used and hence the recirculation in pin 1 is connected to ground, as is the mode control pin[28]. The clock input requires about 10×10^{-12}A of drive current[28]. Since twenty-four such devices are used, the clock generator must supply 240×10^{-12}A which is well within the 200×10^{-3}A drive capability of the LM555 timer integrated circuit[25]. The clock generator is an LM555 timer operating in the astable mode.

In this mode the timer will retrigger itself and cause the voltage capacitor to oscillate between $\frac{1}{3}$Vcc and $\frac{2}{3}$Vcc because the trigger pin and the threshold pin are connected together [25], [26]. The external capacitor charges through $R_{21} + R_{22}$ and it discharges through R_{22}[26]. The charge and discharge times and hence the frequency are independent of the power supply voltage[26].

The charge time (output high) is:[26]

$$t_1 = 0.693 (R_{21} + R_{22}) C_{14} \tag{72}$$

The discharge time (output low) is:[26]

$$t_2 = 0.693 R_{22} C_{14} \tag{72}$$

Combining equation (72) and (73), the total period is:[26]

$$T = \left\{ t_1 + t_2 \right\} = 0.693 \left\{ R_{21} + 2R_{22} \right\} C_{14} \tag{74}$$

The frequency of oscillation is:[26]

$$f = \frac{1}{T} = \frac{1}{0.693\left\{R_{21} + 2R_{22}\right\}C_{14}} = \frac{1.44}{\left\{R_{21} + 2R_{22}\right\}C_{14}} \tag{75}$$

The duty cycle is:[26]

$$D = \frac{R_{22}}{\left\{R_{21} + 2R_{22}\right\}} \tag{76}$$

The minimum value of R_{21} is:[25]

$$R_{21} \geq \frac{Vcc(Vdc)}{I_{pin7}(A)} \geq \frac{Vcc(Vdc)}{0\ 2} \tag{77}$$

Substituting Vcc = 5Vdc into equation (77):

$$R_{21} \geq \frac{5}{0.2} \geq 25\,\Omega \quad Let\, R_{21} = 1000\,\Omega\ (arbitrarily\ chosen)$$

$$Let\, C_{14} = 0.001\mu F\ and\ C_{13} = 0.01\mu F\ (arbitrarily\ chosen)$$

The required frequency of oscillation is 12000Hz, R_{22} may be determined using equation (75):

$$12x10^{3} = \frac{1.44}{\left\{1x10^{3} + 2R_{22}\right\}x10^{-9}} = \frac{1.44}{\left\{1x10^{-6} + 2R_{22}x10^{-9}\right\}}$$

$$1.44 = 12x10^{-3} + 24R_{22}x10^{-6}$$

$$24R_{22}x10^{-6} = 1.44 - 12x10^{-3} = 1.428$$

$$R_{22} = \frac{1.428}{24x10^{-6}} = 0.0595x10^{6} = 59500\Omega$$

Used R_{22} - 62000Ω (nearest standard value)

Substituting into equation (76):

$$D = \frac{62 x 10^3}{1 x 10^3 + 124 x 10^3} = \frac{62 x 10^3}{125 x 10^3} = 0.496$$

D x 100% = 49.6%.

The total time delay of the circuit is: $T_D = t_{CLK} x m$ where m = # stages of shift register (78).

In this case, since three CD4031s are used in each data bus, m = 3 x 64 = 192.

$$Hence: T_D = \frac{1}{12 x 10^3} x 192 = 83.3 x 10^{-6} x 192 = 16 x 10^{-3} s$$

$$t_{CLKACT} = 9.80 \, div \, x \, 10 \, x \, 10^{-6} \, sec = 98.0 x 10^{-6} s$$

$$F_{CLKACT} = 10204 Hz$$

$$D_{ACT} x 100\% = \frac{ON \, TIME}{TOTAL \, TIME} x 100\% = \frac{5.3 x 10 x 10^{-6} x 100\%}{9.8 x 10^{-6}} = 54.1\%$$

$$T_{D_{ACT}} = 98 x 10^{-6} x 192 = 18.8 x 10^{-3} s$$

Figure 34 illustrates the clock-generator waveforms.

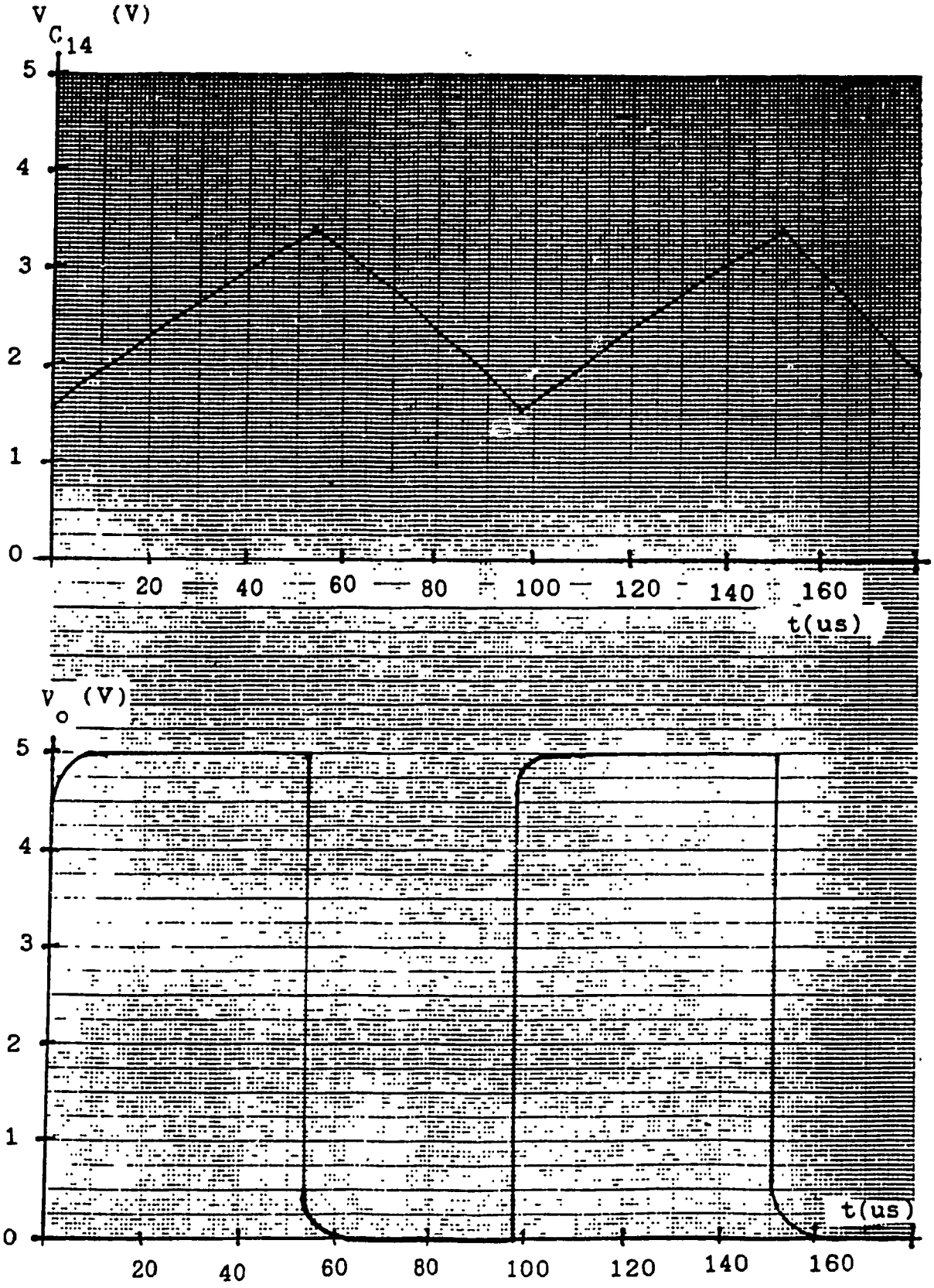


Figure 34 Clock-Generator Waveforms

6.3 Digital-to-Analog Converter

The digital-to-analog converter used is the DAC-08 integrated circuit. The DAC-08 is an eight-bit monolithic high-speed multiplying digital-to-analog converter[29], [30]. The settling time, which is the delay in a digital-to-analog converter from the 50 percent point on the change in the input digital code to the effected change in the output signal, is about 100×10^{9}s[30]. When used as a multiplying digital-to-analog converter, monotonic performance over a 40 to 1 reference current range is possible[29]. Complementary current outputs are available; this enables differential output voltages to be generated[29], [30]. The DAC-08 is monotonic because its output either increases or remains constant when the input code is incremented from any code to the next higher code[22]. Figure 35 is a block diagram of the DAC-08.

6.3.1 Digital-to-Analog Converter Circuit Operation

The DAC-08 employs an R-2R ladder network. The switches are fabricated as semiconductor switches which are usually TTL and/or CMOS compatible[31]. A binary word ($D_7 - D_0$) is applied to the inputs of the switches and sets the geometry of the resistor ladder network such that: [31]

$$I_{OUT} = I_{REF}\left\{\frac{D_7}{2} + \frac{D_6}{4} + \frac{D_5}{8} + \frac{D_4}{16} + \frac{D_3}{32} + \frac{D_2}{64} + \frac{D_1}{128} + \frac{D_0}{256}\right\} \quad (79)$$

As shown in Figure 36 which is a schematic of the digital-to-analog converter, a current to voltage converting operational-amplifier stage is used. A potentiometer is connected to the V_{LC} pin to adjust for a zero output for a zero input.

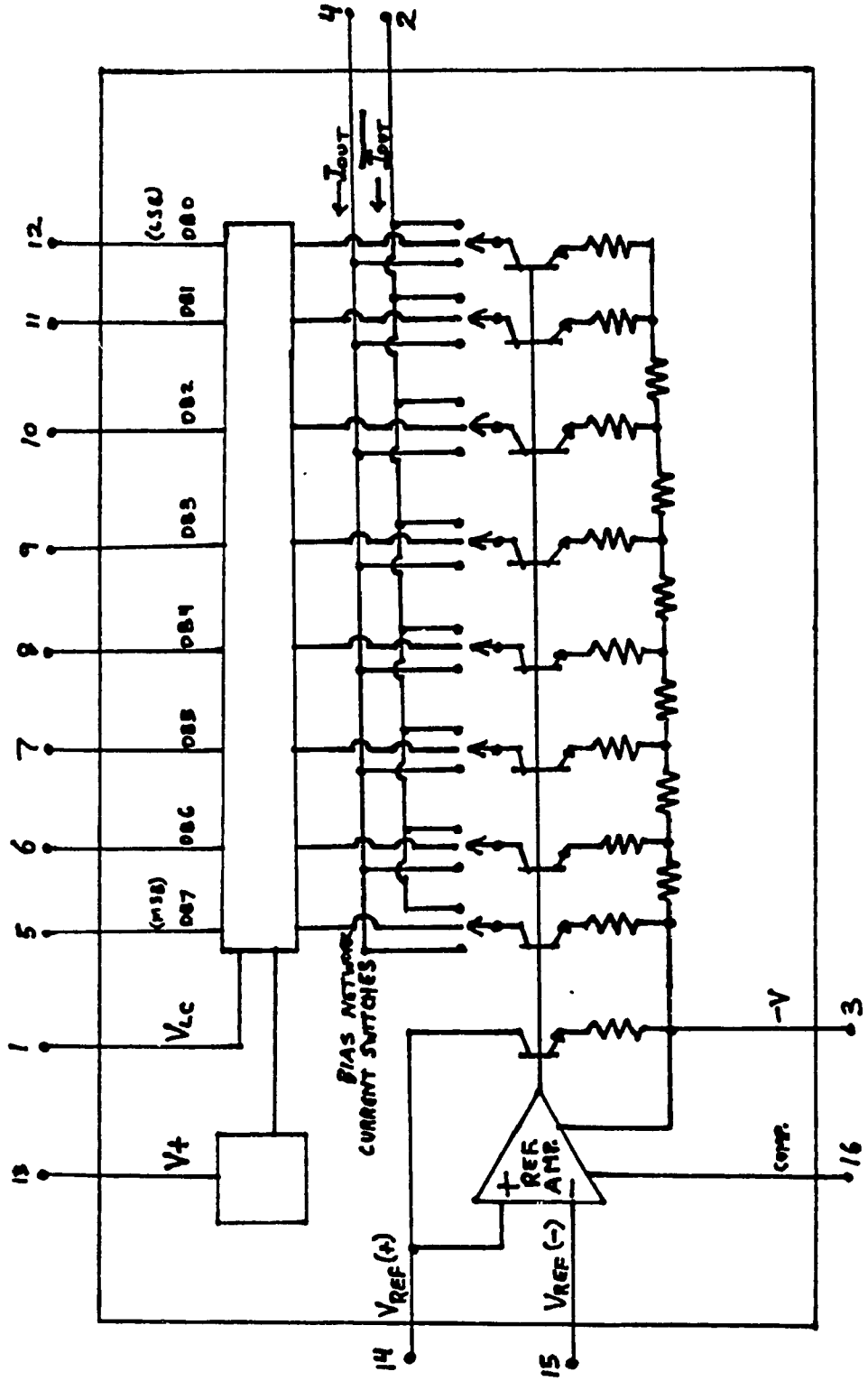


Figure 35 Block Diagram of DAC-08[30]

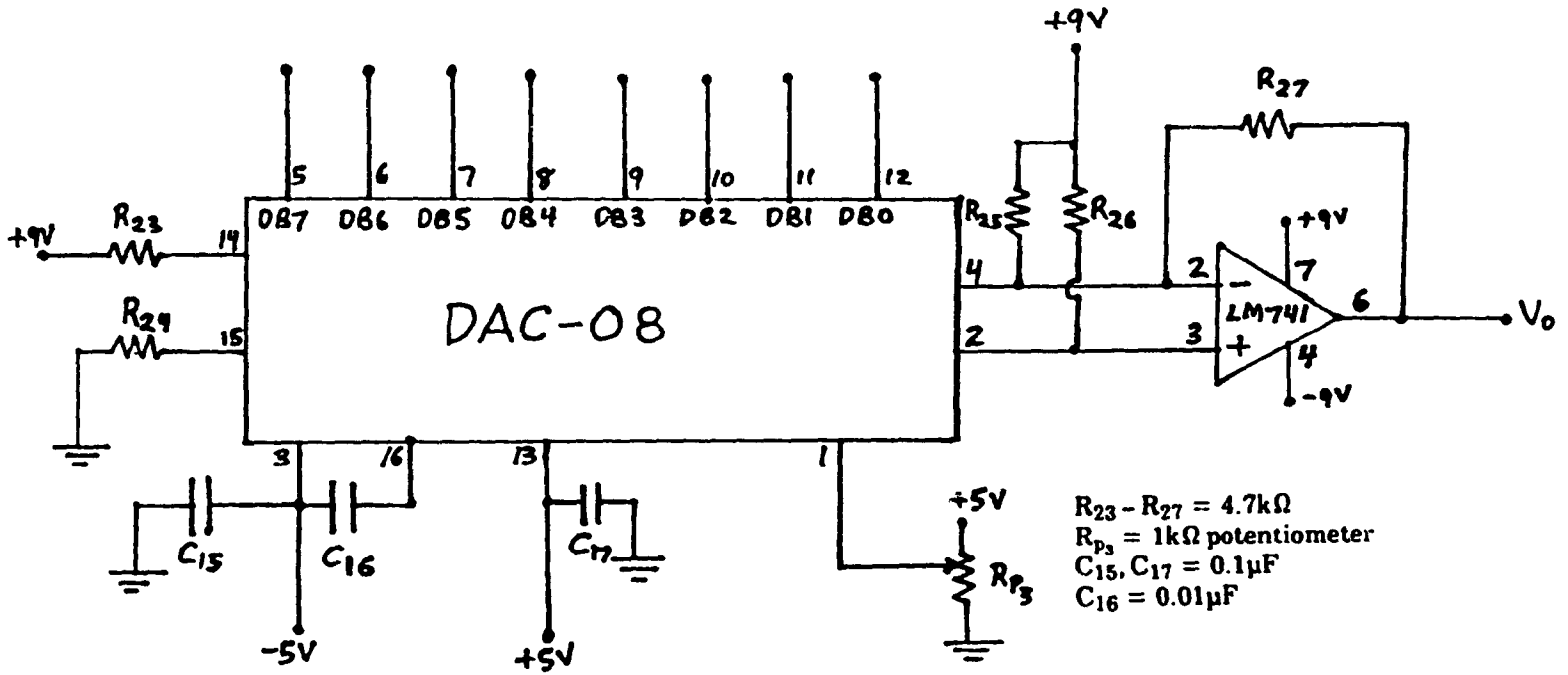


Figure 36 Schematic of Digital-to-Analog Converter

6.3.2 Digital-to-Analog Converter Performance

The performance data of the digital-to-analog converter is listed in Table 7.

Table 7 Digital-to-Analog Converter Performance Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	V_{OUT}
1	1	1	1	1	1	1	1	8.20
1	1	1	1	1	1	0	1	8.15
1	1	1	1	0	1	1	0	8.20
1	1	1	1	0	0	0	0	8.15
1	1	1	0	1	0	1	0	8.17
1	1	1	0	0	0	1	0	8.01
1	1	0	1	1	1	0	0	7.58
1	1	0	1	0	1	1	0	7.14
1	1	0	0	1	1	1	1	6.53
1	1	0	0	0	1	1	1	6.02
1	1	0	0	0	0	1	0	5.85
1	0	1	1	1	0	1	0	4.06
1	0	1	1	0	0	1	1	3.56
1	0	1	0	1	1	1	0	3.00
1	0	1	0	0	1	0	1	2.39
1	0	1	0	0	0	0	1	2.16
1	0	0	1	1	0	0	1	1 52
1	0	0	1	0	0	1	1	1.16
1	0	0	0	1	1	0	0	0.76
1	0	0	0	0	0	0	1	0.00
1	0	0	0	0	0	0	0	-0 02
0	1	1	1	1	1	1	1	0.41
0	0	0	0	0	0	0	0	-7.30
0	0	0	0	0	0	1	0	-7.30
0	0	0	0	1	0	1	0	-7.30
0	0	0	1	0	0	0	0	-6.86
0	0	0	1	0	1	1	1	-6.56
0	0	0	1	1	1	0	1	-6.13
0	0	1	0	0	1	0	0	-5.75
0	0	1	0	1	0	1	0	-5.45
0	0	1	1	0	0	1	0	-4.84
0	0	1	1	0	1	1	0	-4.55
0	0	1	1	1	1	0	1	-4.08
0	1	0	0	0	1	0	0	-3.62
0	1	0	0	1	0	1	1	-3.28
0	1	0	1	0	0	0	1	-2.74
0	1	0	1	0	1	1	0	-2.42
0	1	0	1	1	1	1	0	-1.90
0	1	1	0	0	1	0	0	-1.51
0	1	1	0	1	0	1	0	-1.20
0	1	1	1	0	0	0	1	-0.41

6.4 Low-Pass Filter (with fc = 7000 Hz)

The low-pass filter used here is exactly the same as the one discussed in section 5.2, section 5.2.1 and section 5.2.2. Table 8 is the performance data of the low-pass filter. Figure 37 is its frequency-response plot and Figure 38 is the phase-response plot of the low-pass filter.

6.5 Time-Delay System

A complete schematic of the time-delay system is shown in Figure 39. There is a limit to the frequency range of the time-delay system. From equation (67) and the clock frequency, 357kHz, 43.4kHz $\leq F_{s_{MAX}} \leq$ 347kHz. Depending on the number of clock pulses required per conversion at 7000Hz, the maximum frequency of this system, the signal will be sampled about six to 50 times. The input signal must be a relatively slowly varying voltage or the accuracy of the analog-to-digital converter will suffer[20]. Only above 5000Hz, does the accuracy suffer from the minimal oversampling rate. A sample and hold circuit at the input is not necessary. The analog-to-digital converter can handle bipolar input signals of five volts or less.

The digital-to-analog converter produces bipolar analog signals of eight volts or less, depending on the amplitude of the input signal. This provides a gain of 4.08dB.

Table 8 Low-Pass Filter (fc = 7000Hz)

			Theoretical	Actual Data				
w (rad/s)	aw (rad/s)	F (Hz)	G(dB)	V_{IN} (Vp-p)	V_{OUT} (Vp-p)	$\varnothing_{OUT}$ (°)	G	G (dB)
0.0143	628.3	100	4.01	4.0	6.80	-7.2	1.7	4.61
0.0714	3,141.5	500	4.01	4.0	6.80	-7.2	1.7	4.61
0.1459	6,283	1K	4.00	4.0	6.60	-7.2	1.65	4.35
0.2857	12,566	2K	3.98	4.0	6.60	-25.2	1.65	4.35
0.4286	18,849	3K	3.86	4.0	6.60	-35.4	1.65	4.35
0.5714	25,132	4K	3.57	4.0	6.40	-57.6	1.6	4.08
0.7143	31,415	5K	3.00	4.0	6.20	-68.4	1.55	3.81
0.8571	37,698	6K	2.13	4.0	5.60	-71.1	1.4	2.92
1.0000	43,981	7K	1.00	4.0	4.90	-86.2	1.225	1.76
1.1429	50,264	8K	-0.32	4.0	4.00	-92.9	1.0	0.00
1.2857	56,547	9K	-1.71	4.0	3.60	-104.7	0.9	-0.92
1.4286	62,830	10K	-3.12	4.0	3.05	-108	0.7625	-2.36
1.7143	75,396	12K	-5.83	3.8	2.25	-121	0.59	-4.55
2.1429	94,245	15K	-9.44	3.8	1.20	-134	0.32	-10.01
2.8571	125,660	20K	-14,30	3 8	0.80	-136.8	0.21	-13.53
5.7143	251,320	40K	-26.28	3.8	0.21	-158.4	0.06	-25.15
7.1429	314,150	50K	-30.15	3.8	0.14	-162	0.04	-28.67

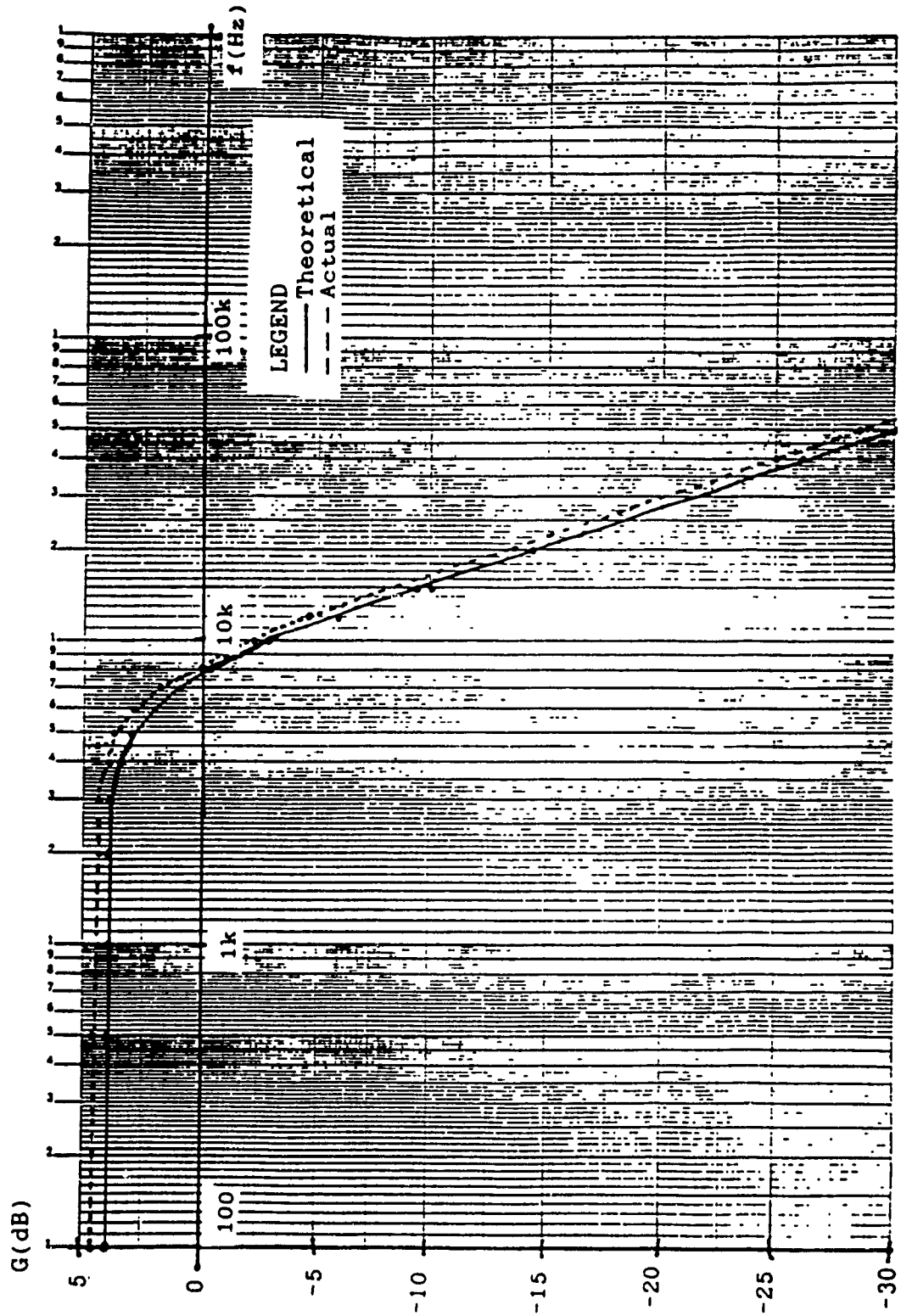


Figure 37 Frequency-Response Plot of 7000 Hz Low-Pass Filter

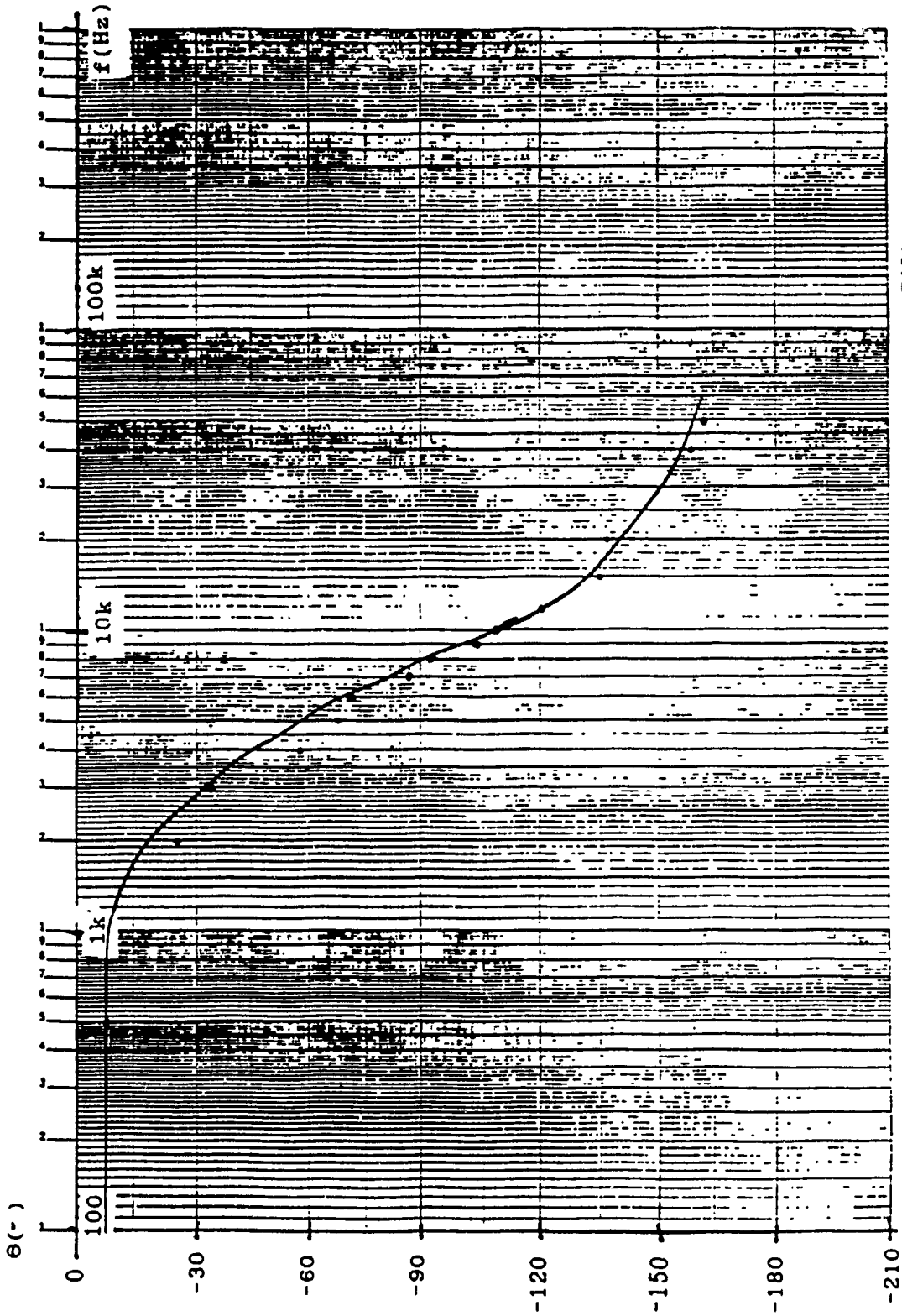


Figure 38 Phase-Response Plot of 7000 Hz Low-Pass Filter

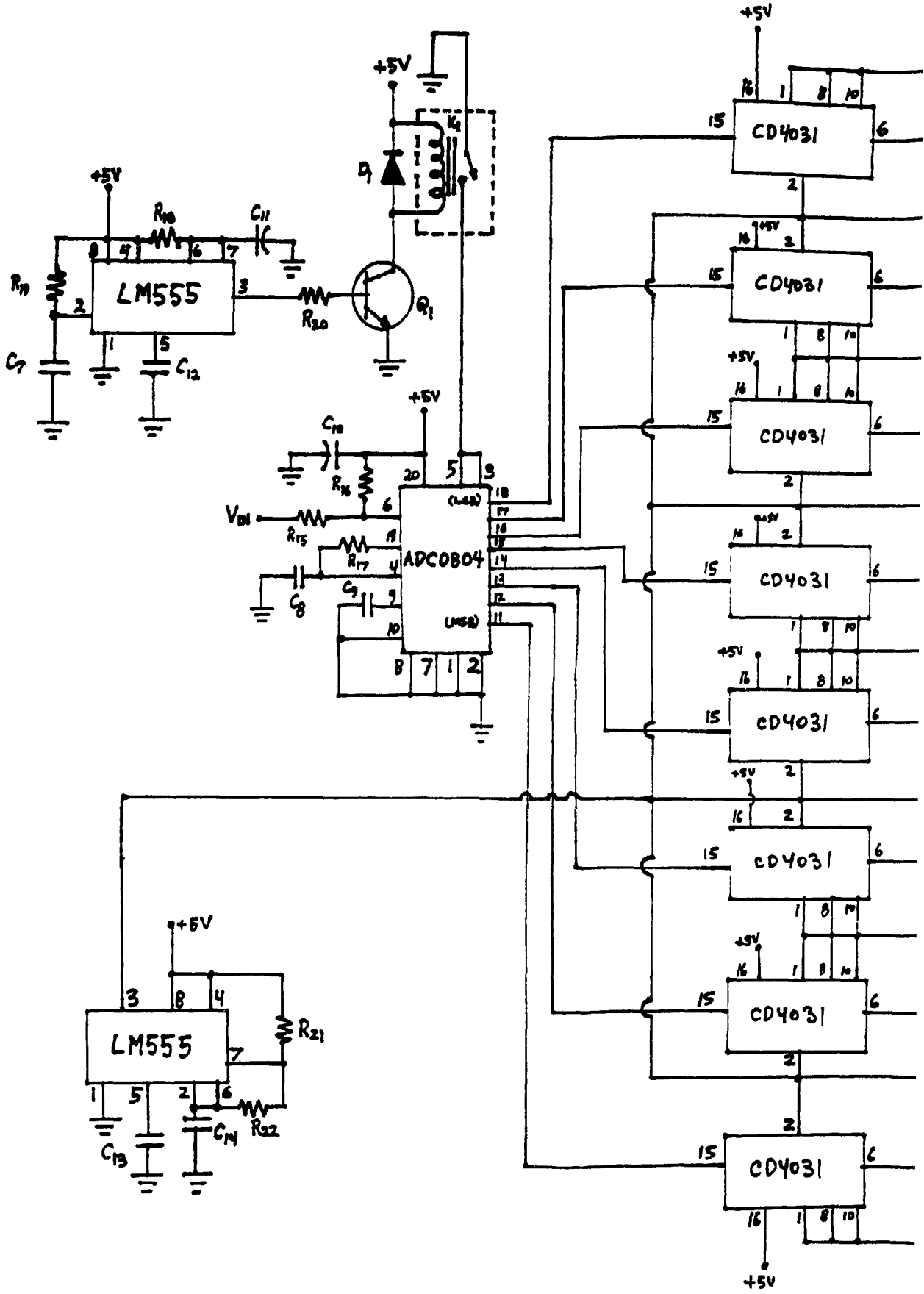
The low-pass filter is used to smooth the output by removing the high frequency components of the digital-to-analog converter output. The cut-off frequency is 7000Hz and is the same circuit as that used in the decoder.

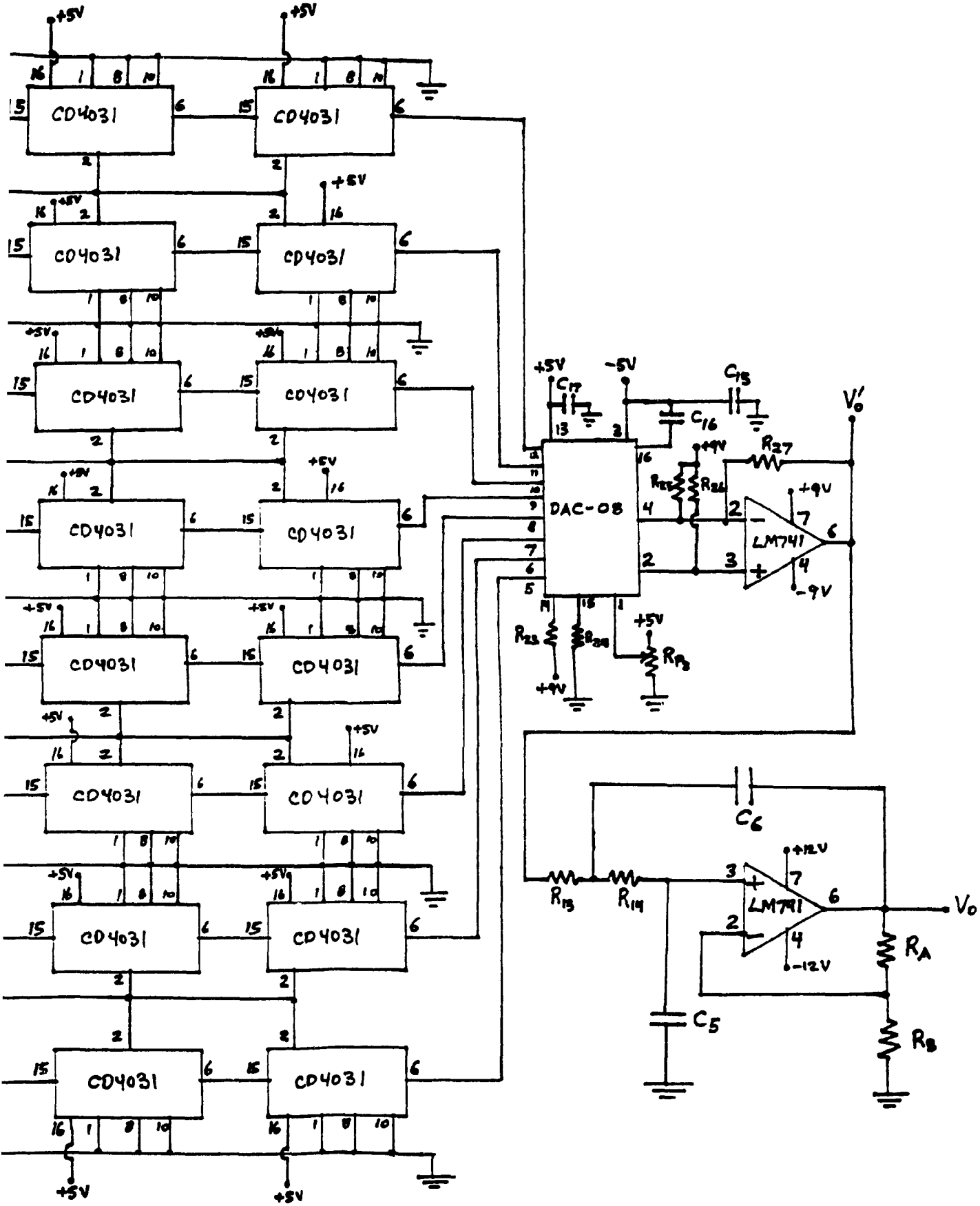
Figure 40, Figure 41 and Figure 42 show V_{in}, the output of the digital-to-analog converter and the output of the low-pass filter at 50Hz, 500Hz and 5000Hz respectively.

At 5000Hz, refer to Figure 40, the output of the time-delay system has some visible distortion. However, at 3500Hz, the output has minimal visual distortion. The distortion is a function of the clock frequency of the analog-to-digital converter. The clock frequency used is about 357kHz. The analog-to-digital converter can operate with a clock frequency of up to 1.46MHz[20]. However, above 640kHz, accuracy is sacrificed[20]. Operating the analog-to-digital converter at 1MHz should reduce the distortion of the output of the time-delay system.

The low-pass filter of the time-delay system provides an additional 4.08dB of gain. The overall gain of the time-delay system is about 2.56 which can be seen in Figure 40, Figure 41 and Figure 42, where a four volt peak-to-peak input signal generates a 10Vp-p output voltage.

The time delay, T_D, is 16×10^{-3}s, as shown in Figure 40. This is close to the theoretical 18.8×10^{-3}s, as discussed in section 6.2.


+5V
LM555
R_{18}
C_{11}
R_{19}
C_7
C_{12}
R_{20}
Q_1
D_1
K_1
C_{10}
R_{16}
V_{IN}
R_{15}
R_{17}
C_8
C_9
ADC0804
R_{21}
R_{22}
C_{13}
C_{14}
CD4031


CD4031
DAC-08
LM741
+5V
-5V
+9V
-9V
+12V
-12V
C_{17}
C_{15}
C_{16}
C_6
C_5
R_{27}
R_{22}
R_{24}
R_{23}
R_{25}
R_{P_3}
R_{13}
R_{14}
R_A
R_B
V_o'
V_o

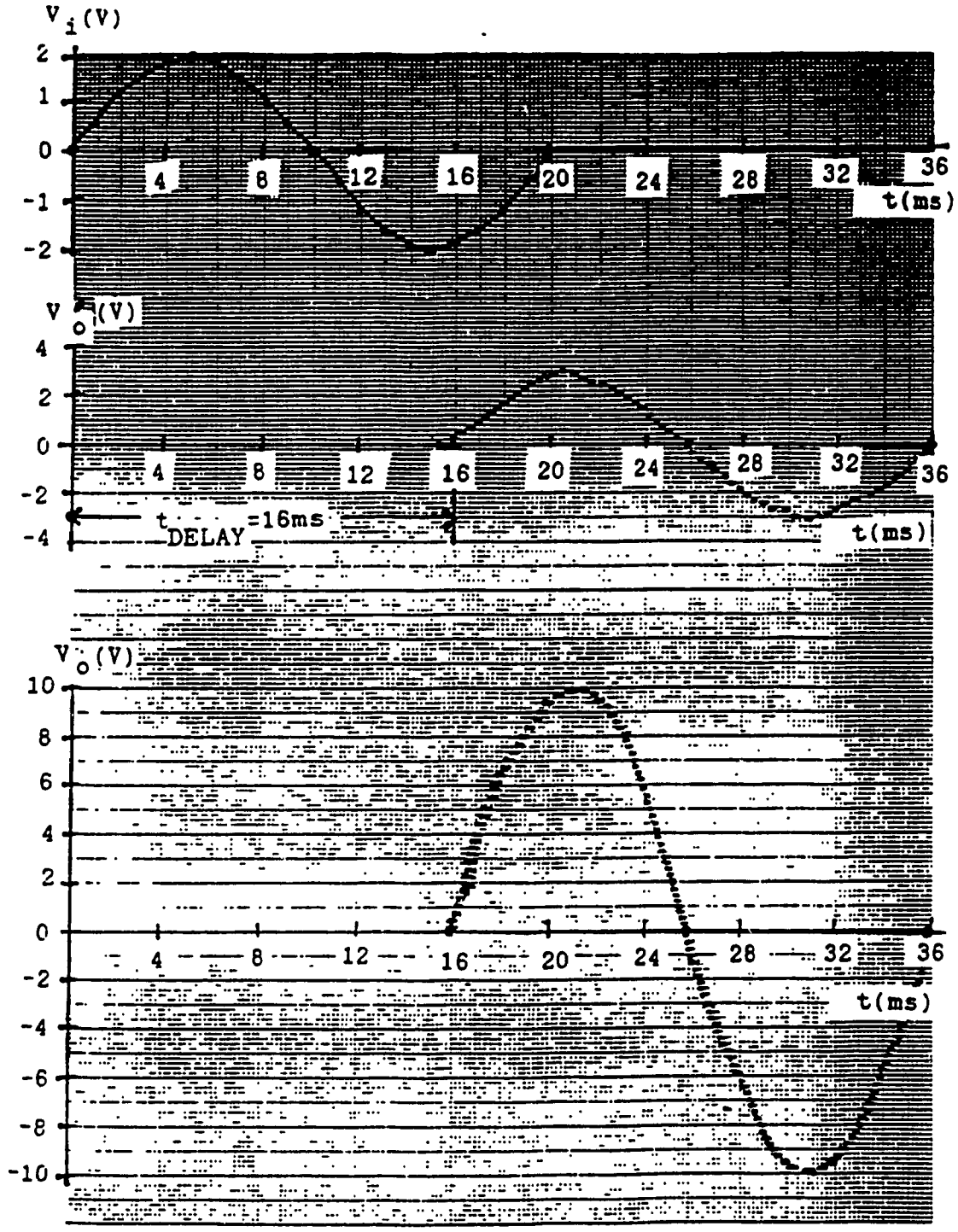


Figure 40 Performance of Time-Delay Circuit at 50 Hz

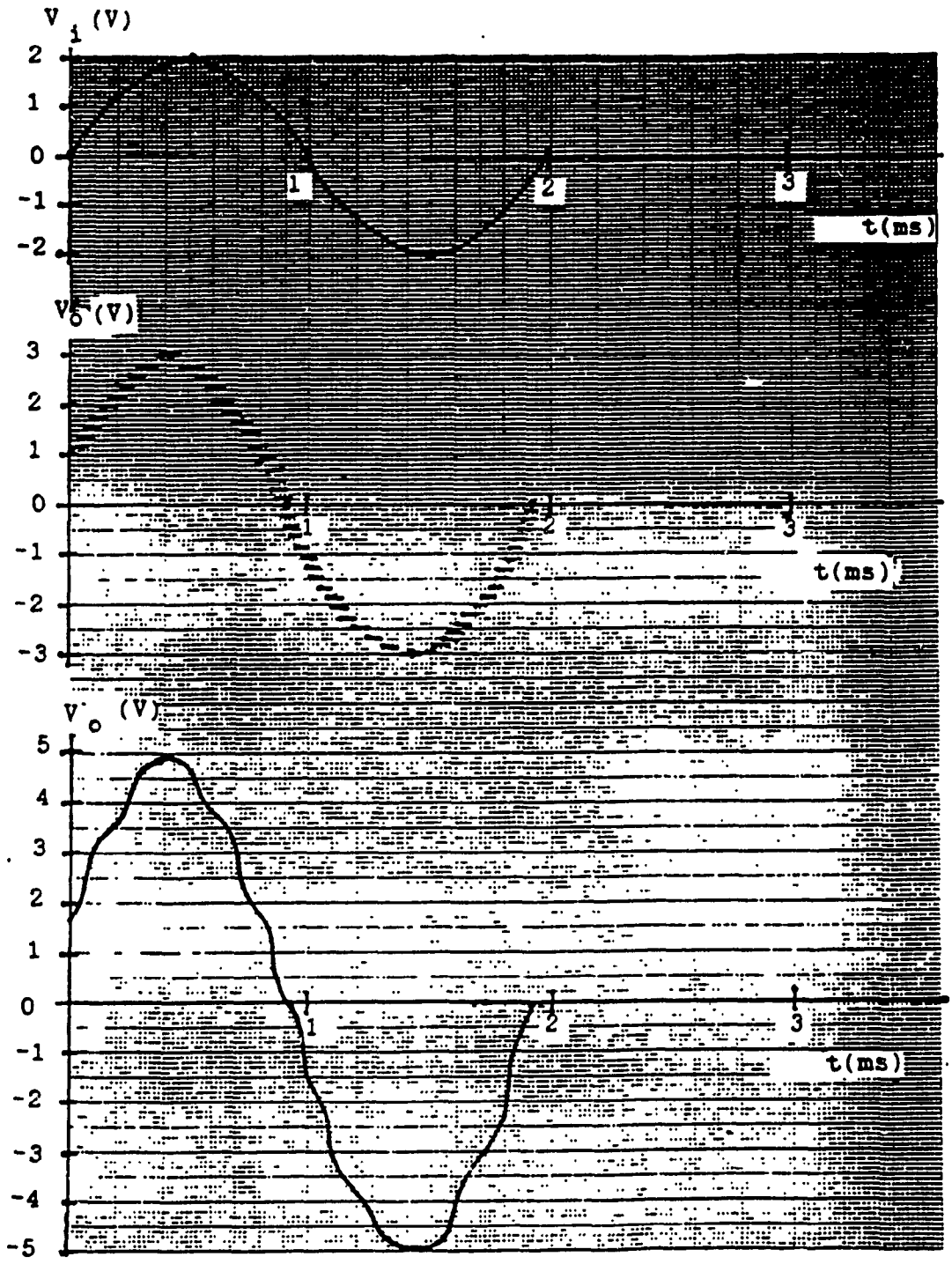


Figure 41 Performance of Time-Delay Circuit at 500 Hz

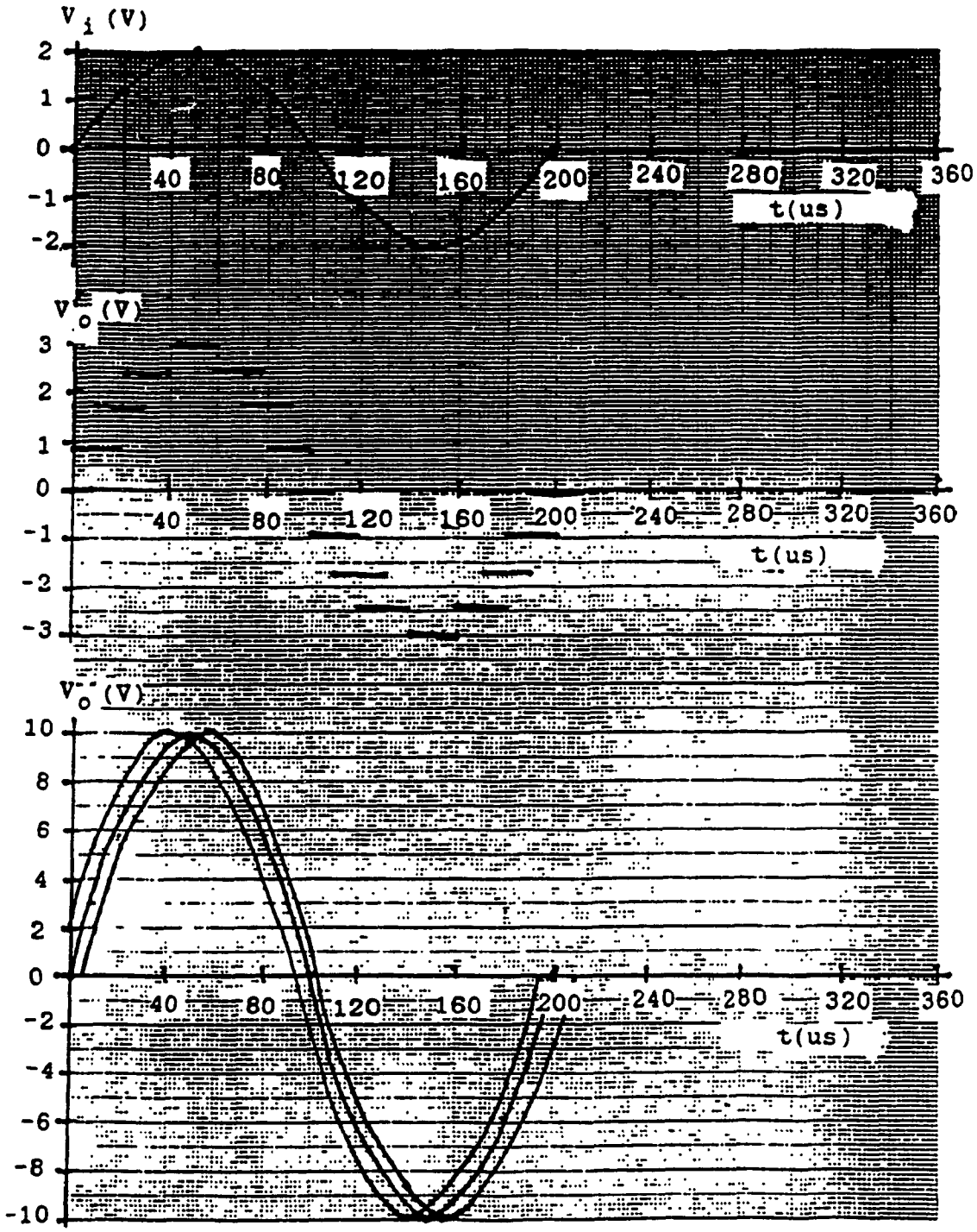


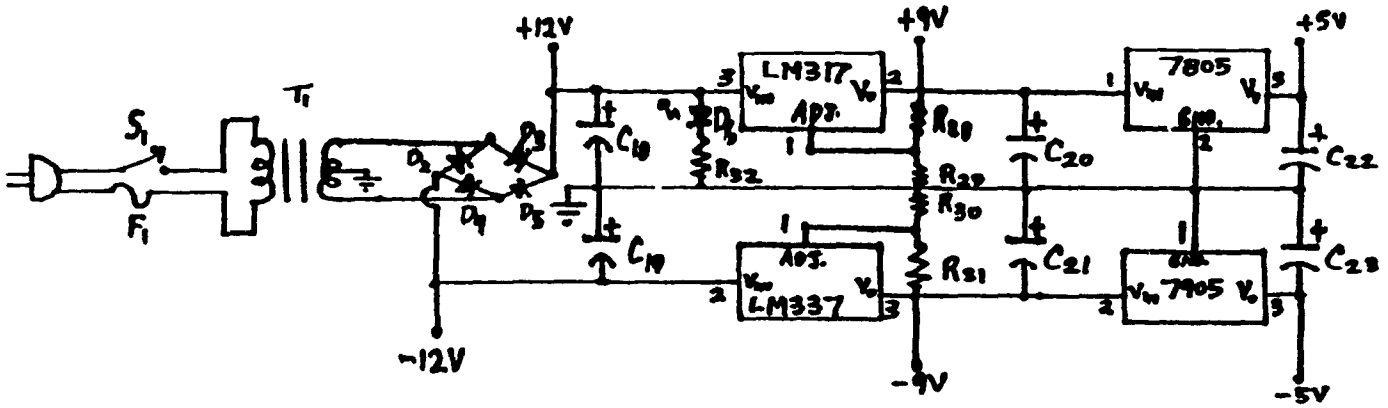
Figure 42 Performance of Time-Delay Circuit at 5000 Hz

CHAPTER 7

POWER SUPPLY

The surround-sound decoder requires a dual 12V supply for the sub-woofer simulator circuit, the decoder circuit, and the low-pass filter of the time delay circuit. The time delay circuit also needs a dual five volt as well as a dual nine volt power supply. Figure 43 is a schematic of the surround-sound decoder power supply.

Diodes D_3 and D_5 rectify the positive half cycles and diodes D_2 and D_4 rectify the negative half cycles of the transformer secondary voltage. Capacitors C_{18} and C_{19} filter the positive and negative voltages respectively. These preregulated outputs are $\pm\sqrt{2}/2V_{SECONDARY}$, that is ± 12.7V. The LM317 and the MC7805 are positive voltage regulators and the LM337 and the MC7905 are negative voltage regulators. Resistors R_{28} and R_{29} determine the voltage output of the LM317 and resistors R_{30} and R_{31} set the output voltage of the LM337. The transient responses of the four voltage regulators are improved by tantalum capacitors C_{20}, C_{21}, C_{22} and C_{23}[32], [33], [34]. Resistor R_{32} limits the current entering D_6 which is a light-emitting diode used as a power on indicator. Switch S_1 is the power switch and fuse F_1 protects the surround-sound system. Transformer T_1 steps down the primary 117Va.c. voltage to a secondary voltage of 18V.c.t. alternating current.



$T_1 = 18V_{ct}$ @ 2A
$R_{28} = 220\Omega$
$R_{29} = 1.35k\Omega$
$R_{30} = 750\Omega$
$R_{31} = 120\Omega$
$R_{32} = 1k\Omega$
$C_{18}, C_{19} = 3300\mu F$
$C_{20} - C_{23} = 0.47\mu F$ tantalum

Figure 43 Schematic of Power Supply

7.1 LM317 and LM337 Voltage Regulators

The fixed voltage regulator MC7800 and MC7900 series are not available as nine volt regulators[32], [33]. Therefore, the LM317 and LM337 voltage regulators are used. They are 3-terminal adjustable output regulators[34]. Only two resistors are required to set the output voltage range of 1.2V to 37V[34]. They also have internal current limiting, thermal shutdown and safe-area compensation[34].

The LM317 maintains a nominal 1.25V reference between the output and adjustment terminals[34]. The reference voltage is converted to a programming current by R_{28}, see Figure 41, and this constant current flows through R_{29} to ground[34]. The regulated output voltage is:

$$V_{OUT} = V_{REF}\left\{1 + \frac{R_{29}}{R_{28}}\right\} + I_{ADJ}R_{29} \tag{80}$$

The I_{ADJ} is less than 100×10^{-6} amperes and hence introduces a minimum error. Thus equation (80) may be rewritten as:

$$9.0 = 1.25\left\{1 + \frac{R_{29}}{R_{28}}\right\} \tag{81}$$

Let R_{28} = 220Ω[35], then substituting values into equation (81):

$$9.0 = 1.25\left\{1 + \frac{R_{29}}{220}\right\} = 1.25 + \frac{1.25}{2.20}R_{29}$$

$$9.0 - 1.25 = \frac{1.25}{220}R_{29}$$

$$1705 = 1.25\,R_{29}$$

$$R_{29} = 1{,}364\Omega\ (used\ two\ 2700\Omega\ in\ parallel)$$

The LM337 operates in a similar manner. Its equation may be written as:

$$-V_{OUT} = -V_{REF}\left\{1 + \frac{R_{30}}{R_{31}}\right\} + I_{ADJ}\,R_{30} \tag{82}$$

Again, I_{ADJ} presents a very small error, therefore equation (82) may be rewritten as:

$$-V_{OUT} = -V_{REF}\left\{1 + \frac{R_{30}}{R_{31}}\right\} \tag{83}$$

Let R_{31} = 120Ω [35], then, substituting values into equation (83):

$$-9.0 = -1.25\left\{1 + \frac{R_{30}}{120}\right\} = -1.25 - \frac{1.25}{120}R_{30}$$

$$-930 = 1.25\,R_{30}$$

$$R_{30} = 744\Omega\ (used\ 750\Omega,\ nearest\ standard\ value)$$

7.2 MC7805 and MC7905 Voltage Regulators

The unregulated input voltage is fed to the control element and the reference voltage circuit[35]. The output voltage is sampled and fed into one of the error amplifier inputs, as shown in Figure 44 [35]. The other error amplifier input is connected to the reference

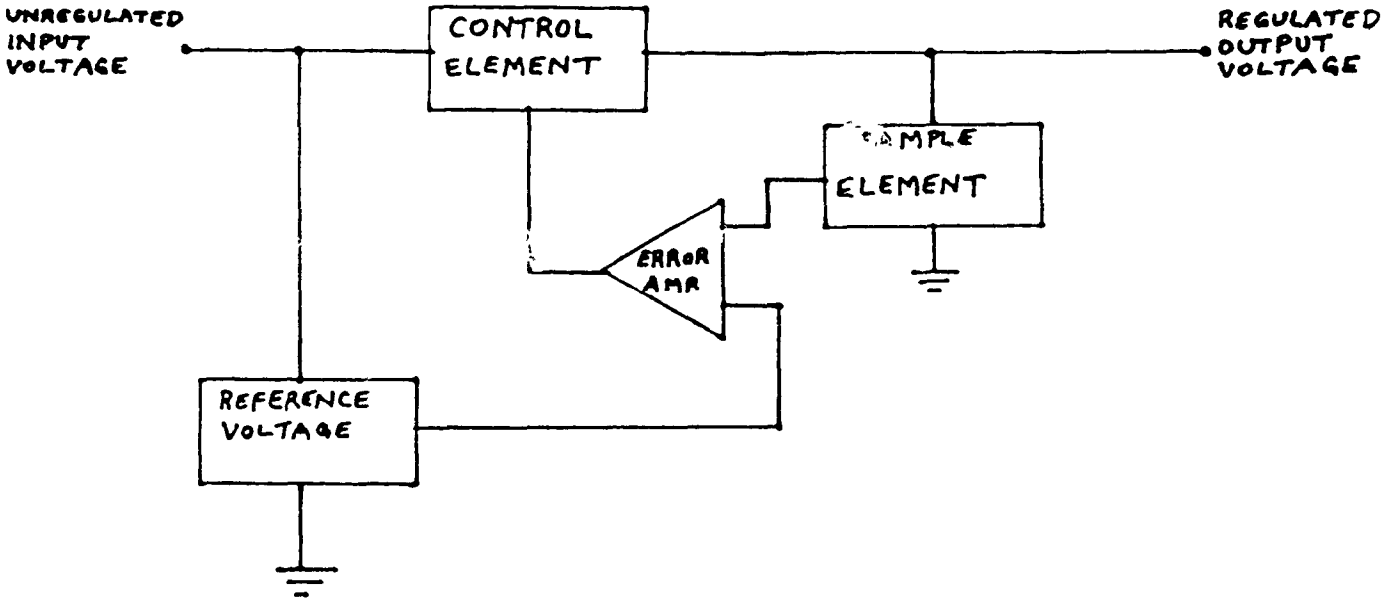


Figure 44 Block Diagram of Typical Linear Regulator (32)

voltage[35]. When the error amplifier senses a difference between the reference and sampling voltages, it acts upon the control element to correct the error by dropping a greater portion of the input[35]. The control element acts as a variable resistor whose resistance is controlled by the error amplifier[35]. The control element is a transistor[35].

As with the LM317 and LM337 regulators, the unregulated input voltage must exceed the regulator's output voltage by at least three volts[35]. The input voltage must not be so large that the regulator device dissipates too much power[35].

The regulator power dissipation is[35]:

$$P_D = \left\{ V_{IN} - V_{OUT} \right\} I_L \tag{84}$$

The MC7805 and MC7905 have an internal thermal protection circuit, a current-limiting circuit and a safe-area protection circuit[35]. The safe-area protection circuit limits the regulator output when the input voltage is too high, ensuring that the pass transistor control element operates within its allowed voltage and current ranges[35].

The four voltage regulators used in the power supply can provide one ampere of current, more than enough for the requirements of the surround-sound decoder system[32], [33], [34]. The power dissipation of the regulators is kept low because the unregulated input voltage is not too high, about four to nine volts, and because the load current is less than 200×10^{-3}A.

7.3 Power-Supply Performance

The ripple waveforms of the positive power-supply rails are shown in Figure 45, while those of the negative supply rails are shown in Figure 46. The dual power supplies are full-wave rectified. The ripple frequency is 120Hz, as shown in Figure 45 and Figure 46. The discharge time, also shown in Figure 45 and Figure 46 is 7×10^{-3}A.

$$\Delta Q = I_{DC} t_D = C\Delta V \tag{85}$$

where ΔQ is charge on capacitor C

where t_D is discharge time

where ΔV is peak-to-peak ripple voltage.

For the positive power supply:

$$7 \times 10^{-3} I_{DC} = 3300 \times 10^{-6} \times 0.15 = 0.495 \times 10^{-3}$$

$$I_{DC} = \frac{0.495}{7} = 70.71 \times 10^{-3} A$$

$$P.R.V._{DIODE} = V_{SEC} = 18 V_{a.c.}$$

$$R.P.I._{DIODE} > 10 I_{DC} > 10 \times 70.71 \times 10^{-3} > 707.1 \times 10^{-3} A$$

$$V_{CAP} = V_{DC} + \tfrac{1}{2} V_{p-p_{RIPPLE}} = 12.7 + 0.075 = 12.775 V$$

The filter capacitors used are rated at 25V. The rectifier diodes used are 1N5404 which are rated at 3A and 400V[36].

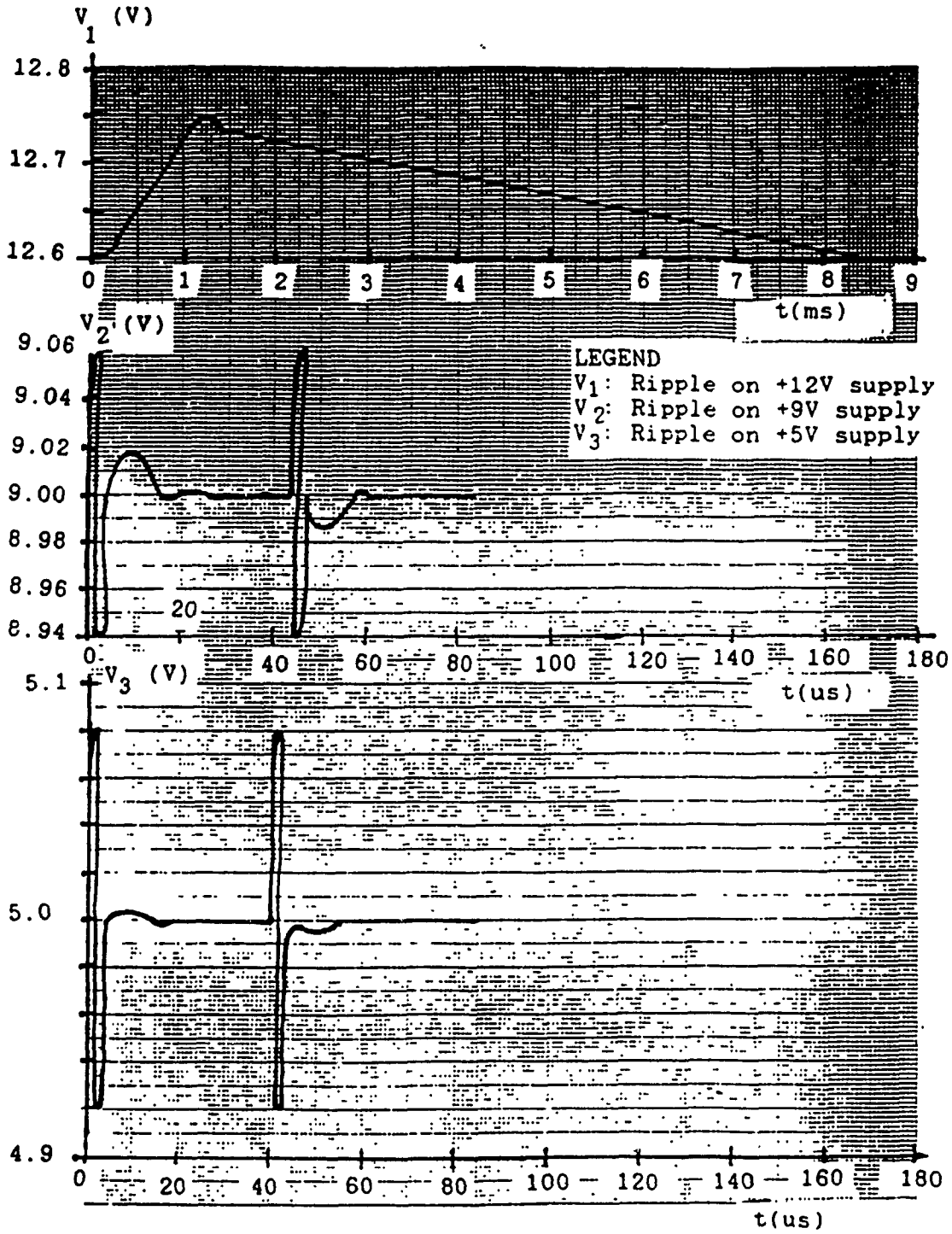


Figure 45 Ripple on Positive Power Supplies

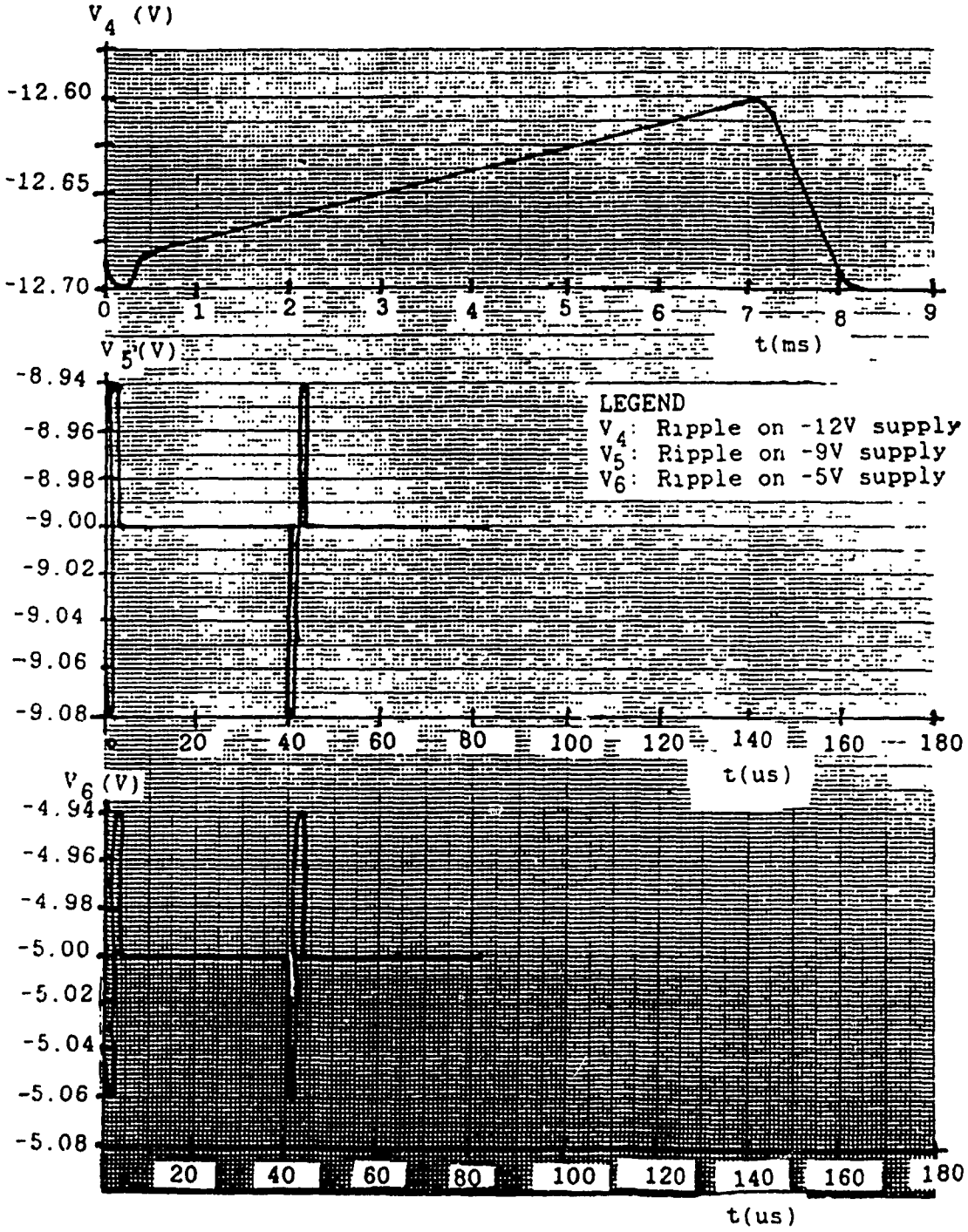


Figure 46 Ripple on Negative Power Supplies

$$\%RIPPLE = \frac{V_{RIPPLE_{RMS}}}{V_{DC}} x\,100\% \tag{86}$$

$$V_{RIPPLE_{RMS}} = \frac{1}{2\sqrt{2}} V_{RIPPLE_{P-P}} = \frac{0.15}{2\sqrt{2}} = 0.053V$$

$$\%RIPPLE = \frac{0.053}{12.675} x\,100\% = 0.42\%$$

This is a 100 fold decrease in the ripple of an unregulated supply, which is:

$$\%RIPPLE = \frac{V_{LAC} x\,100\%}{V_{LDC}} = \frac{0.307EM}{0.637EM} x\,100\% \frac{0.307}{0.637} x\,100\% \tag{87}$$

$$\%RIPPLE = 48.19\%$$

Similarly, for the negative power supply: Substituting into equation (85):

$$7 x 10^{-3} I_{DC} = 3{,}300 x 10^{-6} x 0.1$$

$$I_{DC} = \frac{0.33 x 10^{-3}}{7 x 10^{-3}} = 47 x 10^{-3} A$$

$$P.R.V._{DIODE} = V_{SEC} x 18V_{AC}$$

$$P.R.I._{DIODE} > 10 I_{DC} > 10 x 47 x 10^{-3} > 470 x 10^{-3} A$$

$$V_{CAP} = V_{DC} + \tfrac{1}{2} V_{p-pRIPPLE} = 12.7 + 0.05 = 12.75V$$

$$\%RIPPLE = \frac{0.035}{-12.650} x\,100\% = -0.28\%$$

The negative supply ripple is less than that that of the positive rail because the negative rail delivers less current than the positive power supply. This is expected because the positive supply drives more integrated circuits than the negative power supply rails.

The rectifier diodes and filter capacitors are overrated for the requirements of the system.

The voltage regulators can dissipate up to two watts[35]. From equation (84), they dissipate:

$$LM317\text{: } P_D = (12.675 - 9.0)(70.71 x 10^{-3}) = 260 x 10^{-3} W$$

$$LM337\text{: } P_D = (-12.65 + 9.0)(-47 x 10^{-3}) = 172 x 10^{-3} W$$

$$LM7805.\ P_D = (9 - 5)(70.71 x 10^{-3}) = 283 x 10^{-3} W$$

$$LM7905\text{: } P_D = (-9 + 5)(-47 x 10^{-3}) = 188 x 10^{-3} W$$

All the voltage regulators are well within their performance ratings and therefore no heat-sinks are required.

The outputs of the four voltage regulators have unmeasurable ripples as can be seen from Figure 43 and Figure 44. There is, however, a very low voltage spike or noise.

CHAPTER 8

SYSTEM INSTALLATION AND LISTENING TESTS

8.1 System Installation

The system is designed to go between the pre-amplifier and the power amplifier as shown in Figure 47. The rear speakers should be small bookshelf speakers mounted in the rear corner of the listening room about six feet above the floor.

A schematic of the complete surround-sound decoder is shown in Figure 48.

8.2 Listening Tests

The sub-woofer simulator adds a lot of punch to the lower bass frequencies. This adds a lot of realism to sound effects such as a strong wind or an explosion. Many musical passages also have a lot of low-frequency content, and this information is reinforced by the sub-woofer simulator portion of the surround-sound decoder.

The decoder generates an (L-R) rear channel from all sources. If a Dolby surround-sound encoded source is used, the rear-to-front sound effects of the movie theater is recreated in the home. If the source is not Dolby surround-sound encoded, a rear-channel signal is still

generated by the decoder and the effect makes the music an exciting three-dimensional listening experience.

If the sound source is a monophonic signal, then there is no output from the rear speakers, as expected, because if L = R, then (L-R) = 0.

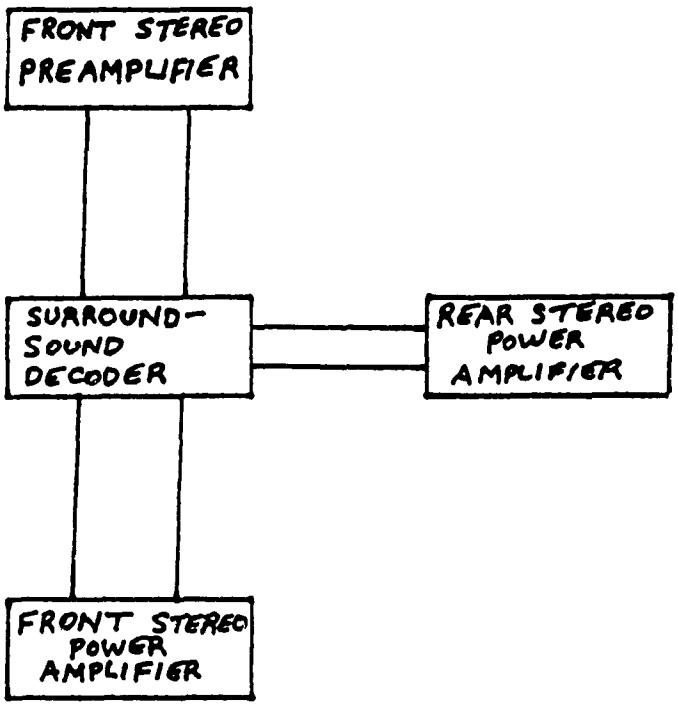
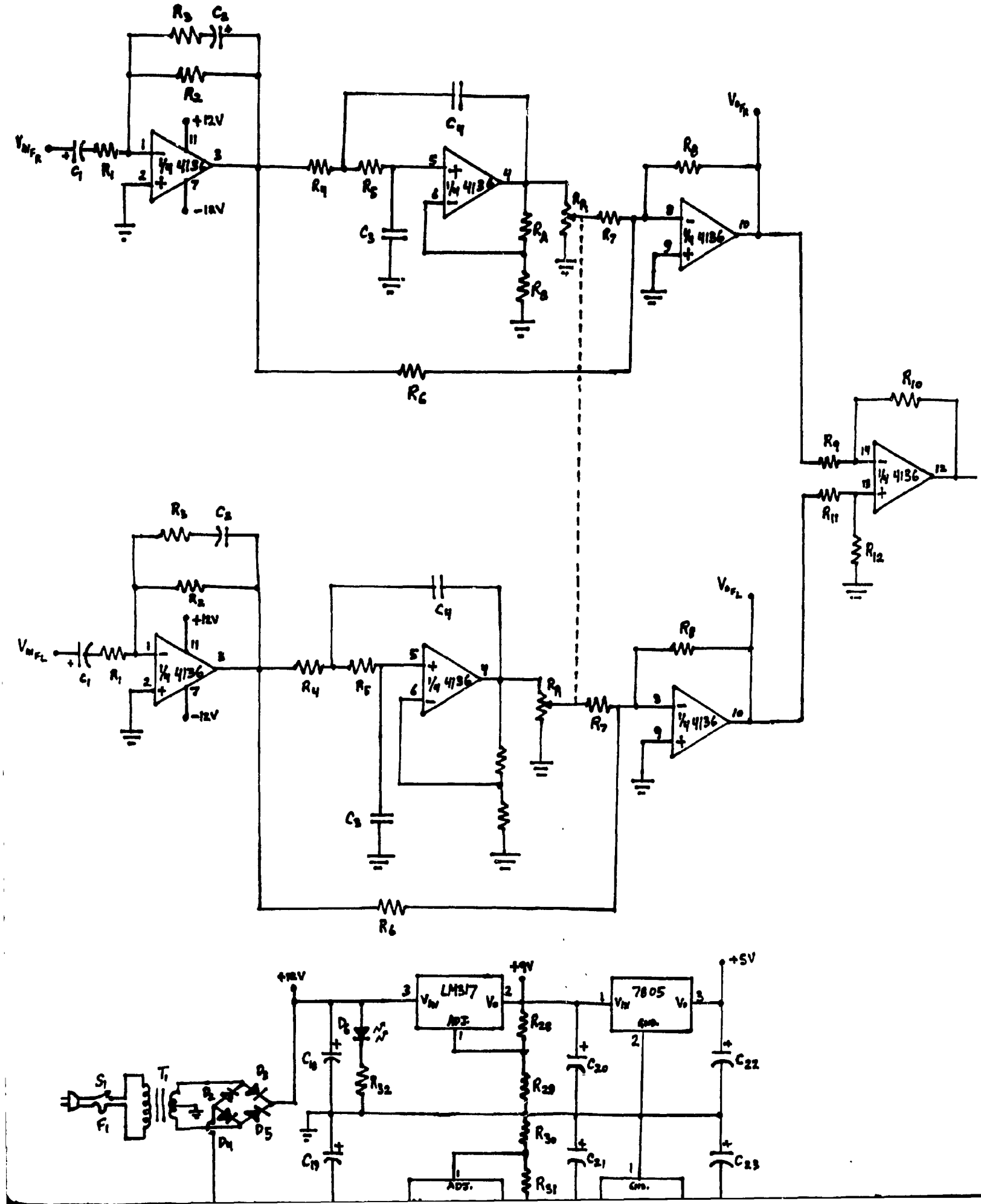
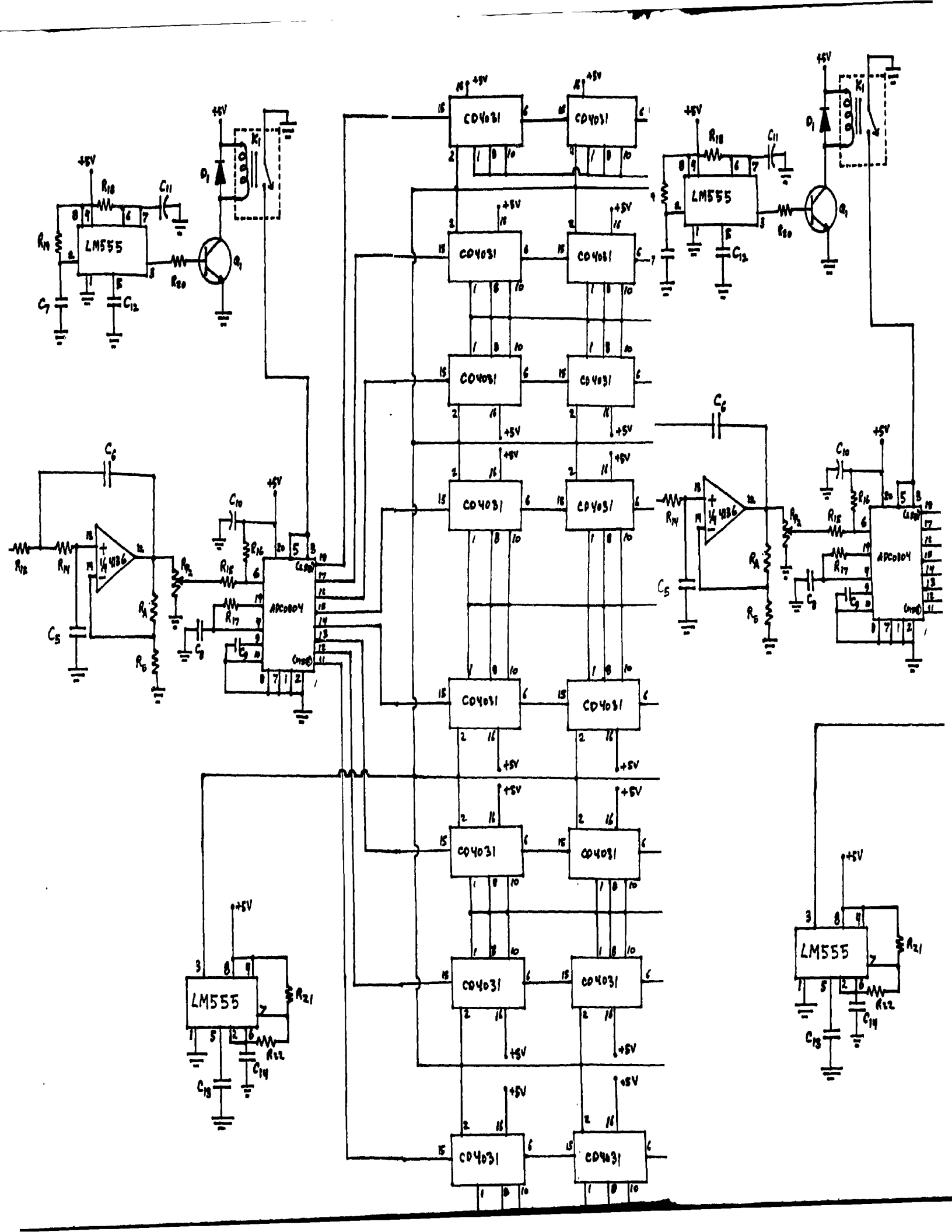
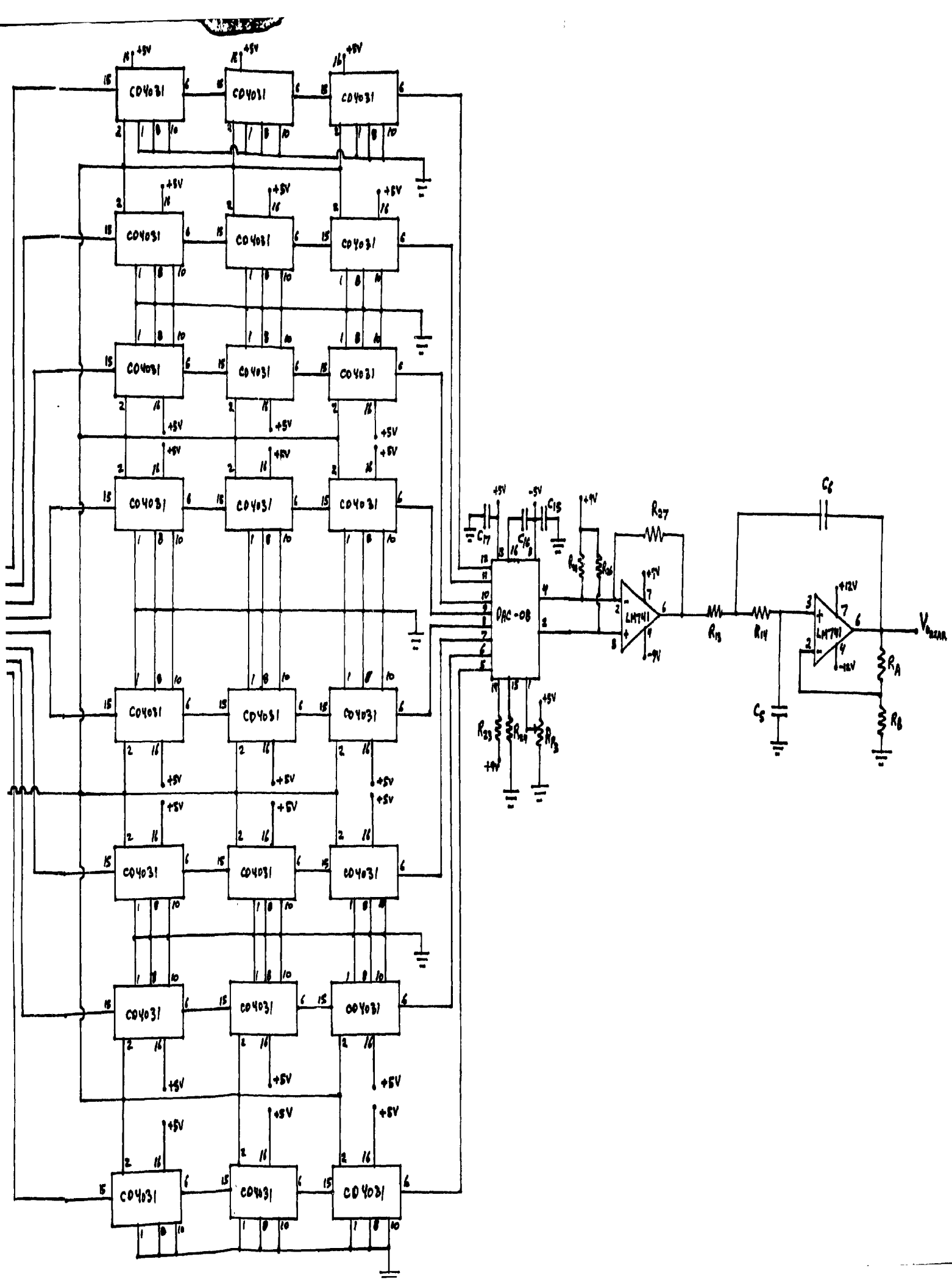


Figure 47 System Configuration


R3 C2
R2
+12V
VINFR
C1
R1
1/4 4136
-12V
C4
R4
R5
C3
R8
R6
R7
VOFR
R10
R9
R11
R12
VINFL
VOFL
LM317
ADJ.
7805
+9V
+5V
T1
S1
F1
D1
D2
D3
D4
D5
C18
C19
R32
R28
R29
R30
R31
C20
C21
C22
C23


+5V
LM555
CD4031
ADC0804
1/4 4136
K1
D1
Q1
C5
C6
C7
C9
C10
C11
C12
C13
C14
R15
R16
R17
R18
R21
R22


CD4031
DAC-08
LM741
+5V
-5V
+9V
-9V
+12V
-12V
C_{17}
C_{16}
C_{15}
R_{27}
C_6
C_5
R_{13}
R_{14}
R_A
R_B
V_{BIAS}

CHAPTER 9

CONCLUSION

The surround-sound decoder of this report consists of a sub-woofer simulator, an (L-R) decoder, a 7000 Hz low-pass filter, a 20 ms audio time delay, a rear channel gain control and a power supply. The front channel separation is maintained in the decoder.

The sub-woofer simulator, the (L-R) decoder and the 7000 Hz low-pass filter are active circuits using operational amplifiers. The low-pass filter is a Sallen-Key Butterworth design.

The audio time-delay circuit was designed using digital techniques. The decoded rear channel signal is fed to an eight-bit analog-to-digital converter. Each of the eight data lines is shifted in time by about 20 ms by a serial 192-stage shift register. Each 192-stage shift register is fabricated by cascading three 64-stage shift registers. The eight shifted data lines are fed to an eight-bit digital-to-analog converter to produce a rear channel signal delayed by 20 ms. This signal is smoothed by a 7000 Hz low-pass filter which is identical to the one in the decoder circuit.

The rear channel control is a potentionmeter wired as a voltage divider. The power supply was designed using three-terminal voltage

regulators to obtain regulated bipolar voltages for the active and digital circuits of the surround-sound decoder.

Blend circuits were not required in the decoder designed for the home; therefore, the front channel separation of the existing stereo system is maintained.

The sub-woofer simulator boosts frequencies in the range of five hertz to 100Hz. A maximum boost of 28dB is achieved at eight hertz. The decoder rolls-off frequencies above 7000Hz and it decodes signals as expected. When the same signal is applied to both front channel inputs, no output is obtained, as expected, because (L-R) = 0 when L=R. The audio time-delay circuit gives a delay of 16 ms. The ripple of the positive and negative 12V supplies are about 150 mV while that of the bipolar nine and five volt supplies are small enough to be considered unmeasurable.

REFERENCES

1. Masters I.G. and Toole, F.E., "The Final Illusion Space and Ambience," Sound & Vision, vol. 3, no. 6, November/December 1987, pp. 10-12.

2. Hill, N.M., "Build This Subwoofer Simulator," Radio-Electronics, vol. 59, no. 5, May 1988, pp. 57-60.

3. "Surround Sound Processors," Sound & Vision, vol. 4, no. 5, September/October 1988, p.116.

4. "Letters," Radio-Electronics, vol. 59, no. 6, June 1988 pp. 22-25.

5. Gerzon, M., "Surround-sound psychoacoustics," Wireless World, vol. 80, no. 1468, December 1974, pp. 483-485.

6. Hill, N.M., "Build This Surround Sound Decoder," Radio-Electronics, vol. 59, no. 4, April 1988, pp. 45-54.

7. Markwick, B., "Periodicity and Perception Why speakers with identical specifications sound different," Electronics & Technology Today, vol. 12, no. 12, December 1988, pp. 9-11.

8. Swamy, M.N.S., Gargour, C.S. An Introduction To Modern Filter Design, (Montreal: Concordia Electrical Engineering Department, 1983), pp. 8.2-8.4.

9. Van Valkenburg, M.E., Analog Filter Design, (New York: Holt, Rinehart and Winston, 1982), pp. 9-12.

10. Lancaster, D. Active Filter Cookbook, (Indianapolis: Howard W. Sams & Company, 1987), pp. 8-9.

11. Van Valkenburg, M.E., pp. 15-19.

References (Cont'd)

12. Fischer, C.R., "Choosing Op Amps for Specific Applications," Modern Electronics vol. 4, no. 11, November 1987, pp. 24-30.

13. Van Valkenburg, M.E., pp. 28-30.

14. Van Valkenburg, M.E., pp. 171-177.

15. Van Valkenburg, M.E., pp. 23-26.

16. Swamy, M.N.S., Gargour, C.S., p. 8.9.

17. Swamy, M.N.S., Gargour, C.S., pp. 8.13-8.14.

18. Swamy, M.N.S., Gargour, C.S., p. 2.6.

19. Van Valkenburg, M.E., pp. 37-40.

20. National Semiconductor Data Conversion/Acquisition Data Book, 1980, pp. 5-21 - 5-44.

21. Melen, R., Garland, H., Understanding IC Operational Amplifiers, (Indianapolis: Howard W. Sams & Co., Inc., 1973), pp. 114-124.

22. Signetics Linear L.S.I. Data and Applications Manual, 1985, pp. 4-3 - 4-10.

23. Dimopoulos, N. Experimental Manual Coen 417, (Montreal: Concordia Computer Engineering Department, 1984), pp. 3.2 - 3.3.

24. Carr, J.J., Interfacing Your Microcomputer To Virtually Anything, (Blue Ridge Summit: Tab Books Inc., 1984), pp. 166-167.

25. Motorola Linear Integrated Circuits, 1979, pp. 6-44 - 4-49.

References (Cont'd)

26. National Linear Integrated Circuits, 1973, pp. 4-12 - 4.13.

27. Transistor Specifications Manual, 6th edition, (Indianapolis: Howard W. Sams & Co., Inc., 1973), p. 27.

28. RCA COS/MOS Integrated Circuits, 1975, pp. 162-167.

29. National Semiconductor Data Conversion/Acquisition Data Book, 1980, pp. 8-5 - 8-12.

30. Signetics Linear L.S.I. Data and Applications Manual, 1985, pp. 4-40 - 4-49.

31. Dimopoulos, N, p. 2.1.

32. Motorola Linear Integrated Circuits, 1979, pp. 4-126 - 4-137.

33. Motorola Linear Integrated Circuits, 1979, pp. 4-153 - 4.161.

34. Motorola Linear Integrated Circuits, 1979, pp. 4-16 - 4-23.

35. Cunkelman, J., "Universal Power Supply," Hands-On Electronics, vol. 5, no. 1, January 1988, pp. 54-57.

36. Active Electronics' 1989 Catalogue, p. 36.