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# BI-DIRECTIONAL DC-DC CONVERTER FOR LOW POWER APPLICATIONS

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A Thesis

in

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## ABSTRACT

## BI –DIRECTIONAL DC-DC CONVERTER FOR LOW POWER APPLICATIONS

Manu Jain

Applications that require exchange of power from the source to the load and vice-versa have conventionally been implemented with two uni-directional converters; each processing the power in one direction. With growing emphasis on compact, smaller and efficient power systems there is increasing interest in the possibility of using bi-directional converters, especially in DC power based applications like space, telecommunication and computer systems. A bi-directional dc-dc converter, capable of bilateral power flow, provides the functionality of two uni-directional converters in a single converter unit. This thesis proposes a topology for a bi-directional dc-dc converter for use in low power applications. The implementation of this converter topology for a battery charger/discharger circuit, with applications in DC UPS systems, demonstrates its feasibility and advantages when compared to the conventionally used circuits. The topology is based on a half-bridge on the primary and a current fed push-pull on the secondary side of a high frequency isolation transformer. The small signal and steady state analyses of the proposed topology are presented. Characteristic curves generated from the analysis aid the design of a laboratory prototype as demonstrated by a detailed design example. Experimental results from the prototype, under different operating conditions, validate and evaluate the topology. Achieving bi-directional flow of power using the same power components provides a simple, efficient and galvanically isolated topology for a low power bi-directional dc-dc converter.

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To my parents and family.....

who believed in me and encouraged me all the way.

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# LIST OF PRINCIPAL SYMBOLS

| | | |
|---|---|---|
| $S_1$ | : | High side switch (MOSFET) of half-bridge topology. |
| $S_2$ | : | Low side switch (MOSFET) of half-bridge topology. |
| $S_3$ & $S_4$ | : | Switches (MOSFETs) of current-fed push-pull topology. |
| $C_1$ & $C_2$ | : | Input capacitors of the half-bridge. |
| $T_1$ | : | High frequency isolation transformer. |
| $N_p$ | : | Number of turns of transformer primary winding. |
| $N_s$ | : | Number of turns of transformer secondary winding. |
| $N$ | : | Ratio of primary to secondary turns of transformer windings. |
| $L_o$ | : | Inductor on secondary side of isolation transformer; output filter for half-bridge. |
| $C_o$ | : | Capacitor on secondary side of isolation transformer; output filter for half-bridge. |
| $D_1$ & $D_2$ | : | Catching diodes for flux balancing of half-bridge. |
| $N_{p_1}$ | : | Auxiliary winding flux balancing of half-bridge. |
| $V_S$ | : | Nominal DC bus voltage. |
| $V_{batt}$ | : | Nominal battery voltage. |
| $i_{bus}$ | : | Nominal DC bus (load) current. |
| $i_{batt}$ | : | Nominal battery charging current. |
| $i_{Lo}$ | : | Nominal inductor voltage. |
| $D_{S_1}$ - $D_{S_4}$ | : | Body diodes of switches $S_1 - S_4$. |
| $T_s$ | : | Converter switching time period for both operating modes. |
| $d_{fw}$ | : | Duty ratio of $S_1$ & $S_2$ in forward mode. |

| | | |
|---|---|---|
| $D$ | : | Duty ratio of $S_3$ & $S_4$ in backup mode. |
| $D_{ov}$ | : | Overlap duty ratio of $S_1$ & $S_2$ in backup mode. |
| $\Delta i$ | : | Peak-to-peak ripple in inductor current. |
| $V_{base}$ | : | Base voltage. |
| $P_{base}$ | : | Base power. |
| $P_{bus}$ | : | Power at the DC bus. |
| $P_{batt}$ | : | Power at the battery end. |
| $f_{base}$ | : | Base frequency. |
| $I_{base}$ | : | Base current. |
| $L_{base}$ | : | Base inductance. |
| $C_{base}$ | : | Base capacitance. |
| $d_{fw_{max}}$ & $d_{fw_{min}}$ | : | Maximum and minimum duty ratio of $S_1$ & $S_2$ in forward mode. |
| $V_{batt_{max}}$ & $V_{batt_{min}}$ | : | Maximum and minimum battery voltage. |
| $V_{S_{max}}$ & $V_{S_{min}}$ | : | Maximum and minimum DC bus voltage. |
| $L_{o_{min}}$ | : | Minimum value of inductor Lo. |
| $I_{batt_{min}}$ & $I_{batt_{max}}$ | : | Maximum and minimum value of battery charging current. |
| $V_{S_1 max}$ & $V_{S_2 max}$ | : | Maximum voltage stress across $S_1$ & $S_2$. |
| $I_{S_1 rms}$ & $I_{S_2 rms}$ | : | Rms current through $S_1$ & $S_2$. |
| $V'_{DS3 max}$ & $V'_{DS4 max}$ | : | Maximum voltage across $S_3$ & $S_4$. |
| $I'_{D_{S3_{avg}}}$ & $I'_{D_{S4_{avg}}}$ | : | Average current through $S_3$ & $S_4$. |

$V_{batt_{peak}}$ : Peak allowable battery voltage.

$V_{ripple}$ : Input voltage ripple for half-bridge converter.

$D_{eq}$ & $C_{eq}$ : Equivalent diode and capacitor for steady state analysis of backup mode operation.

$D_{min}$ & $D_{max}$ : Minimum and maximum duty ratio of $S_3$ & $S_4$ in the backup mode.

$D_L$ : Duty ratio for calculating the $L_{o_{min}}$ in backup mode.

$d_{ss}$ : Duty ratio of switch in equivalent circuit for small-signal analysis of forward mode.

$T_{ss}$ : Switching time period of equivalent circuit for small-signal analysis of forward and backup modes.

$r_l$ : Equivalent series resistance of inductor $L_o$.

$C$ : Equivalent output capacitance for small-signal analysis of forward mode.

$r_c$ : Equivalent series resistance of capacitor $C_o$.

$v_c$ : Voltage across equivalent output capacitor $C$.

$R$ : Resistance representing load for small-signal analysis of forward mode.

$N'$ : Ratio of secondary to primary turns of transformer windings.

$d_{cfsss}$ : Equivalent duty ratio of $S_3$ and $S_4$ for small-signal analysis of backup mode.

# CHAPTER 1

# INTRODUCTION

## 1.1 GENERAL INTRODUCTION

Power electronic circuits primarily process the energy supplied by a source to match the form required by the load, by means of using semiconductor devices to control the voltage and current. The energy is usually available from the utility grid or from a bank of batteries with the applications ranging from high-power conversion equipment processing megawatts to everyday low power equipment with requirements of a few milliwatts.

The majority of power converters are unidirectional with the power being supplied from the source to the load. But, a number of applications like motor drives [1-4], uninterruptible power supplies [5-10], alternate energy systems [11], battery charger-dischargers, telecommunication [12] and space systems [13-14], require the additional exchange of energy from the load to the source. These applications utilize power converters with bi-directional transfer properties.

Conventionally, two independent unidirectional converters were used to achieve bi-directional transfer of power. The escalating cost of energy in recent years has resulted

in growing emphasis on energy management due to the drain on natural resources and environmental pollution, and energy saving techniques are becoming more important. The demand for the development of sophisticated, compact and efficient power systems has prompted research in bi-directional converters providing the desired bilateral power flow and capable of replacing the two unidirectional converters.

Bi-directional power flow is an especially attractive proposition in DC power based systems such as spacecraft applications, telecommunication and computer systems, where the weight and physical size of the power processing modules are a critical aspect of design. Bi-directional dc-dc converters allow transfer of power between two dc sources, in either direction with the ability to reverse the direction of flow of current, and thereby power, while maintaining the voltage polarity at either end unchanged. Such converters are by nature more complex than unidirectional converters.

Although, extensive research has been conducted on unidirectional dc-dc converters, the focus on dc-dc converter topologies applicable for bi-directional power flow has been primarily on medium and high power applications [15-19] with few topologies presented for low power applications. This thesis presents a bi-directional dc-dc converter for low power applications.

## 1.2 LITERATURE REVIEW

In this section, previous work in the area of bi-directional dc-dc converters is reviewed with the objective of defining the current status of research in this area and evaluating topologies for their possible implementation in low power bi-directional dc-dc converters.

### 1.2.1 High Power Bi-directional DC-DC Converters

Various topological variations for DC-DC converters of high power applications with bi-directional power transfer properties have been proposed. The high power dc-dc converters use either resonant [20], soft switching achieved by controlled phase shift [17-19] or hard switched PWM. In general, despite their individual advantages, these topologies are unsuitable for low power applications due to one or all of the following reasons:

- Large number of switches.
- High component count.
- Many switches are active at any given instant of time and the gating pattern may be complicated.
- Limited range of satisfactory operation with high efficiency.
- Complex power and control circuitry.

Operation of the converters in resonant mode [20] uses SCR's, is seen to have high power densities and has the advantage of natural commutation and soft switching ability. However, they have penalties in terms of frequency sensitivity, higher voltage and current stresses in the devices and larger ripple currents in the input and output capacitive filters. Resonant converters also require careful matching of the operating frequency to the resonant tank circuit, and magnetic saturation or drift in the resonant frequency can result in failure.

The dual active bridge presented by Divan et. al. in [17] achieves lower switching losses by controlling the phase shift between the two inverting stages operating at high frequencies. It utilizes the leakage inductance of the transformer as the main energy

transfer element. At high powers and frequencies designing a transformer with controlled leakage is extremely complicated [22]. Also, this topology imposes limitations on the load range and the input voltage range to maintain soft switching for all devices.

The inverse-dual-converter [15-16] does not have the disadvantages of a limited range of operating conditions or complicated transformer design and has high power density at high efficiency. But, this topology is unsuitable for low power applications due to the higher number of switching devices and the sequential commutation technique for their gating.

### 1.2.2 Medium and low power Bi-directional DC-DC converters

As for the higher power applications, medium and low power bi-directional dc-dc converters are also based on either hard switching [6-9, 14, 23-29], soft switching or resonance [13, 30-31]. Most of these dc-dc converters are well suited for a particular application but have one or more of the following drawbacks:

- Lack of galvanic isolation between the battery and the load or source.
- High component stresses.
- Limited operating range when based on resonance or soft switching techniques.
- Large current ripple through the inductors.
- At high frequencies the converters designed to operate under resonance or soft switching may suffer from hard switching of the devices.

The converters operating in the resonant mode [13, 30-31] have a limited range of load and voltage conditions and also subject the devices to high stresses. The presence of

only one active switch in the circuit path during each direction of power flow, leads to higher ratings for the switch and the components as a whole and results in greater costs. In addition, conduction losses in the resonant converter maybe higher. The bi-directional converter topologies presented in [13, 26-31] do not provide galvanic isolation between the battery and the load or source, which is often required in battery operated dc-dc power systems.

Two significant applications of bi-directional dc-dc converters namely, DC UPS [26-28] and battery charger/discharger circuits [13, 14, 23, 29] are based on topologies that aim to achieve lower part count and therefore use components with higher ratings that are expensive and are not optimally selected.

## 1.3 Scope and Contributions of the Thesis

This thesis is concerned with a bi-directional dc-dc converter for low power applications. The purpose is to present a topology that attempts to overcome the drawbacks in the existing topologies. The unique combination of two well known power topologies to achieve the proposed topology of the bi-directional dc-dc converter is the principal contribution of this thesis. The main objectives of the thesis are:

(i) To propose a bi-directional dc-dc converter topology that can be used for low power applications. The specific application of a battery charger/discharger is taken into account as a case study.

(ii) To present the steady state and small-signal analysis of the proposed converter.

(iii) To develop a design procedure for the converter that enables the selection and rating of components for its implementation.

(iv) To verify the feasibility of the proposed converter, the analysis and the design procedure with a design example and the experimental results obtained from the practical setup of the designed converter.

## 1.4 THESIS OUTLINE

The contents of each chapter of the thesis are organized as follows:

Chapter 2 presents the basic topology of the proposed bi-directional converter with application in a battery charger/discharger circuit. The selection of the proposed power topology as opposed to other possible topologies is discussed. The basic components of the converter are described. Operating principles of the bi-directional converter in both the charging and discharging modes are presented. The control of the converter is achieved by peak current mode control and its basic principles and advantages are discussed.

Chapter 3 presents the steady state analysis of the converter in both operating modes. This is used to generate characteristic curves, which provide an insight into the converter and can be used to rate and select the power components in an actual design. The experimental results from the steady state operation of a prototype are used to verify the analysis and the characteristic curves.

Chapter 4 presents the small-signal analysis of the converter while operating in the forward/charging mode and the backup/discharging mode. The key transfer functions for the converter and the error amplifier that aid in the compensated error amplifier design are presented. The theoretical frequency response is compared with the frequency response of the prototype to validate the small-signal analysis. Dynamic response of the

prototype, under switchover from one mode to another and load transients, is presented to demonstrate the closed loop response of the converter.

Chapter 5 presents the detailed design procedure for a laboratory prototype of the proposed converter. The procedure demonstrates the ease of selecting and rating power components when the characteristic curves provided by the steady state analysis are used. The compensated error amplifier in the control loop is designed with the information provided by the transfer functions resulting from the small-signal analysis.

Chapter 6 presents the contributions and conclusions of this thesis and suggestions for future work.

Appendix A shows the detailed mathematical procedure of the small-signal analysis and the derivation of key transfer functions for both operating modes.

# CHAPTER 2

# DESCRIPTION OF THE BI-DIRECTIONAL CONVERTER

## 2.1 INTRODUCTION

As discussed in the previous chapter, some applications require bi-directional transfer of power, which is now being achieved through a single bi-directional converter rather than the conventional approach of using two uni-directional converters. A bi-directional dc-dc converter topology for low power applications is proposed. A battery charger/discharger circuit is chosen as the application where such a converter can be implemented. The battery charger/discharger circuit can be used as part of a DC uninterruptible power supply (UPS).

Conventional battery charger/discharger circuits, Fig. 2-1(a) comprise of two converters; one for the charging the battery from a DC bus and the other to provide power to the DC bus from the battery. The proposed bi-directional converter provides both functions of battery charging and discharging in a single conversion unit with its bi-directional power flow capability, Fig. 2-1(b).

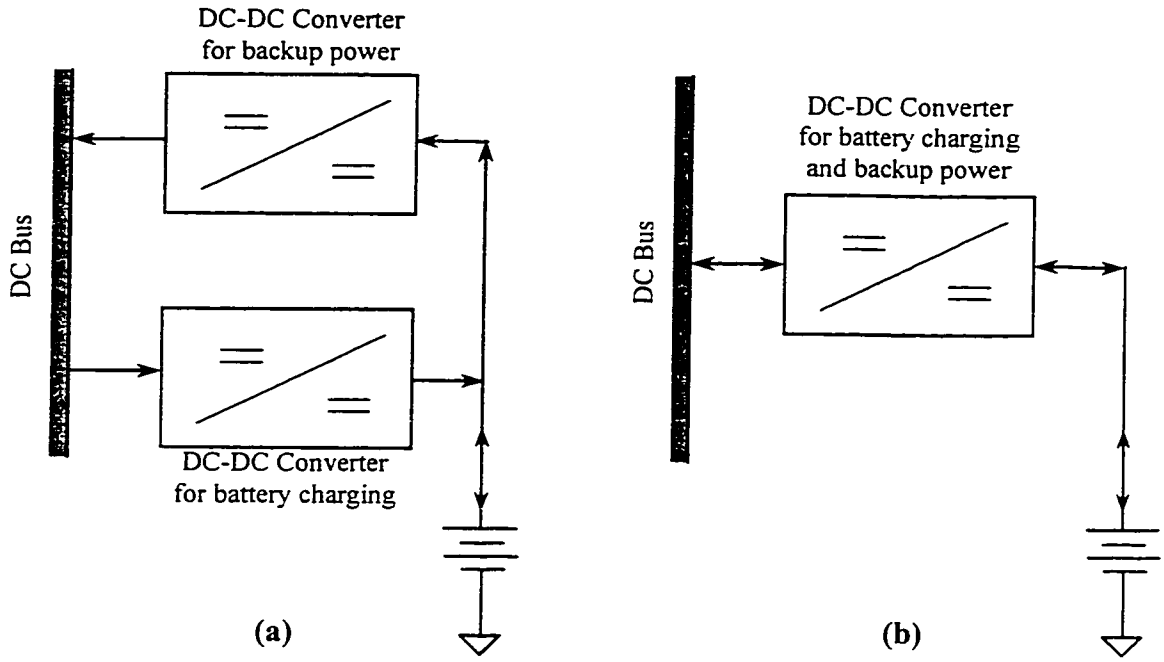



**Fig. 2-1 Battery charger/discharger circuit.**
(a) Conventional circuit using two uni-directional converters. (b) Battery charger/discharger circuit using proposed bi-directional converter.

The basic power topology of the proposed bi-directional converter is shown in Fig. 2-2. The bi-directional converter is seen to consist of a half-bridge topology on the primary of a high frequency isolation transformer and a current-fed push-pull topology on the secondary of the transformer. The DC bus is connected to the half-bridge end and the battery is connected to the current-fed push-pull end of the converter. The converter operates in the forward/charging mode or the backup/discharging mode, depending on the status of the DC mains. All switches are bi-directional and are gated according to the operating mode of the converter.

The objective of this chapter is to describe in detail the topology, modes of operation and the control principle of the proposed bi-directional dc-dc converter for a battery charger/discharger application.

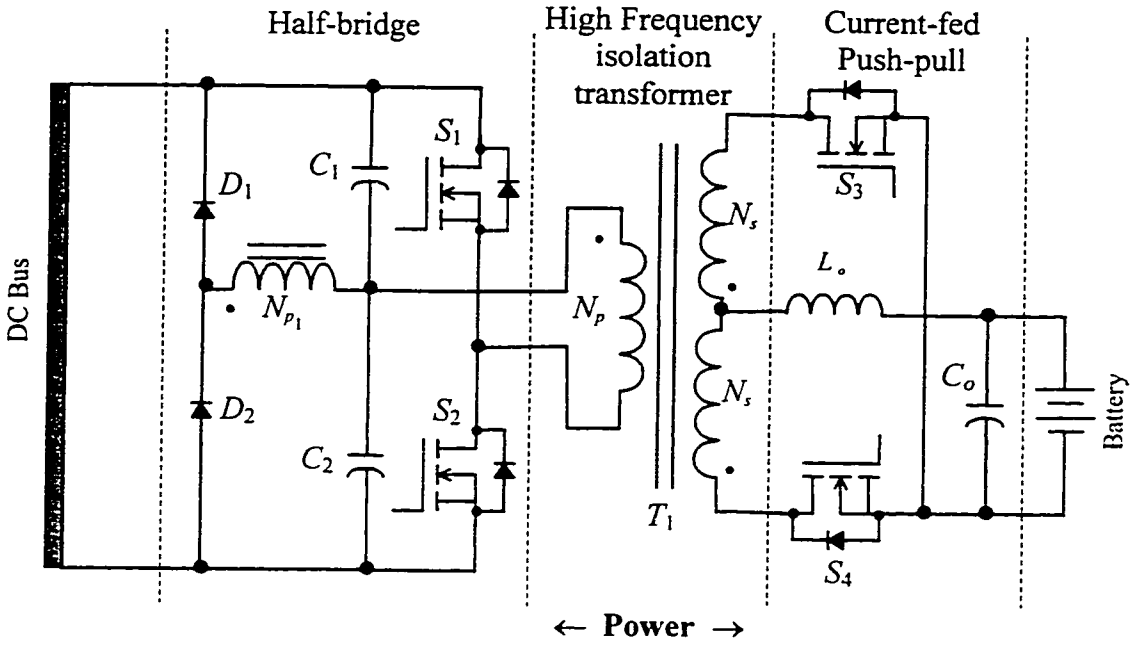



**Fig. 2-2 Topology of the proposed bi-directional dc-dc converter.**

## 2.2 SELECTION OF THE APPROPRIATE POWER TOPOLOGY

Various power topologies can be considered for implementation in bi-directional dc-dc converters. For the battery-charging/forward mode of converter operation, the low voltage battery is charged from the high voltage DC bus and a buck-derived converter must be used. In the backup mode, when the battery supplies the power to the DC bus, a boost-derived circuit is used to produce the higher voltage at the DC bus. Selecting the appropriate topologies is dependent on the application while taking into account their merits and demerits.

The proposed bi-directional dc-dc converter consists of a buck-derived half-bridge circuit on the primary (high voltage end) of the high frequency transformer and a boost-derived current-fed push-pull on the secondary (battery end). The use of these topologies is justified by comparing them to other possible converter topologies.

### 2.2.1 Half-Bridge topology for the buck-derived primary side converter

Bridge topologies are commonly used in converters being fed from a rectified AC line or a high voltage DC bus. Half- and full-bridge topologies subject their switches in the off state to a voltage stress equal to the DC input voltage and not to twice that as do the push-pull, single-ended and interleaved forward converter topologies. In addition, the drawback of voltage spikes on the primary of push-pull and the single-ended forward topologies due to leakage inductance in the transformer primary winding is absent in the bridge topologies. The primary leakage inductance spikes are clamped to the DC supply bus and any energy stored in the leakage inductance is returned to the bus instead of being dissipated in some resistive element. This allows the converters to be used from a high voltage DC bus with switches having lower voltage ratings that are inexpensive and easily available. The inherent problem of transformer saturation in the push-pull is easily overcome in bridge topologies. Bridge topologies also provide better utilization of the transformer windings and core than the conventional push-pull where only one half winding is used during each cycle.

Although the switches in full-bridge topology carry half the peak and rms currents compared to the half-bridge, for the same output power, the number of switches is twice that in the half-bridge. Thus, the full-bridge is usually used in higher power circuits.

The double-ended forward converter also subjects the off state switches to a voltage stress equal to the DC bus voltage like the half-bridge. But, the half-bridge secondary provides a full-wave output compared to a half wave in the forward converter. Thus the square-wave frequency in the half-bridge secondary is twice that in the forward converter, resulting in a smaller output LC inductor and capacitor. The number of

windings on the half-bridge primary is half that in the forward as it must sustain half the supply voltage as compared to the full voltage in the forward, resulting in reduce the winding cost and lower parasitic capacities. The half-bridge topology operates the transformer core in the bipolar flux mode of operation and utilizes the whole primary winding allowing full copper utilization of the transformer.

### 2.2.2 Flux balancing in the half-bridge topology

If the average volt-seconds applied to the primary winding for all positive going pulses is not exactly equal to that for all the negative going pulses, the transformer flux density will increase with each cycle and staircase into saturation. A volt-seconds inequality on alternate half cycles will cause the transformer core to be biased closer towards saturation and enter the curved part of the hysteresis loop. The magnetizing inductance, which is proportional to the slope of the hysteresis loop, decreases and the magnetizing current increases. Under such conditions, small temperature increases can bring about a runaway situation, which drives the core into saturation and destroys the power switches.

In half-bridge implementations using MOSFETs as switching devices, such a situation may arise due to unequal voltage drops across the MOSFETs when they are in the on state. Thus, the junction of $C_1$ and $C_2$ is not exactly at half of the supply voltage. Current-mode control when applied to the half-bridge will ensure that the peak current is identical for each half cycle. In order to correct any volt-second asymmetry a small differential offset in the pulse width will be created, but this results in unequal ampere-seconds drawn through the primary switching devices. Use of a DC blocking capacitor in series with the transformer primary [32] has been suggested, but this will cause a voltage

to build up across it in a direction that reinforces the original volt-second asymmetry. The series capacitor will charge towards one of the supply voltages and alternate half cycles will have unequal voltage amplitudes.

A suitable method of avoiding the runaway saturation of the core is to use a separate balancing winding on the primary side of the transformer with two catching diodes $D_1$ and $D_2$ [33]. This will restore the centerpoint voltage on $C_1$ and $C_2$, compensating for any unequal ampere-seconds in the switching devices by allowing restoration current to flow through them. The wire gauge and the diodes can be small, as they carry only small restoration currents. The number of turns on the balancing winding, $N_{p1}$, should be the same as the primary turns, $N_p$.

### 2.2.3 Current-fed push-pull for the boost-derived secondary side converter

To provide bi-directional power transfer, the output rectifying stage for the half-bridge must be implemented with bi-directional switches. When the converter operates in the backup mode, the battery is the source of energy and provides power to the DC bus. The presence of the output filter inductor of the half-bridge topology in series with the source (battery) results in a current fed topology for the backup mode.

Current-fed converters present numerous inherent advantages, especially at high output voltages and higher output powers, which is the case when the battery is providing backup power to the DC bus. For high output voltages, the size and cost of an output inductor becomes prohibitive. Also, the current-fed converter inherently limits the current provided by the battery.

To allow bi-directional flow of power, the current-fed topology must be a boost-derived circuit. This is evident from the principle of duality for linear electrical networks,

as the half-bridge is a buck-derived circuit. Although switching power converters are nonlinear electrical systems by their very nature, linear duality analysis and principles can be applied to them. This can be demonstrated by the fact that linear small-signal models, using the state-space averaging methods can represent such converters.

A number of boost-derived current-fed topologies have been reported in literature and have been well received as they provide significant advantages over conventional circuits in many applications. Among them the current-fed push-pull operating with overlapping conduction intervals for the switches is probably the mostly widely used topology [34-36]. The disadvantages of other current-fed topologies include:

- poorly controlled inrush current at turn-on,
- use of multiple winding chokes and transformers,
- presence of a tapped input inductor, and
- use of two or more switches in series which reduce the conversion efficiency.

In the proposed converter, the rectifying stage of the half-bridge inverter naturally provides the current-fed push-pull topology. When used with overlapping switch conduction times, the above mentioned topology has the advantage of equal division of inductor current between the switching devices, thereby reducing their average and rms currents as well as the rms current magnitude in the transformer winding $N_s$.

## 2.3 BASIC DESCRIPTION OF THE CONVERTER COMPONENTS

The topology of the bi-directional converter is shown in Fig. 2-2. The basic elements of the converter, their functionality and advantages for both operating modes are described briefly in this section.

### *(i) Capacitors, $C_1$ and $C_2$*

The capacitors $C_1$ and $C_2$ provide the split voltage source at the primary winding of the transformer for the forward operating mode. With their large capacitance values, they are the input filters to the half-bridge converter and remove any ripple that may be present due to the rectified AC line. Also, a lengthy input, which adds series inductance and resistance between the source and the power supply, may not be able to deliver the high-frequency demands of the supply necessary for the fast voltage and current transitions within it. These capacitors will charge at a low frequency and source current over a much higher frequency range. In the backup mode, they form the output filter section for the loads at the DC bus. For the time intervals when the power is not transferred from the battery to the bus, the capacitors discharge to power the load at the DC bus. They are the holdup capacitors during the switchover from forward to backup mode.

### *(ii) Switches $S_1$ and $S_2$*

The power MOSFETs $S_1$ and $S_2$ are the primary switching devices of the half-bridge circuit while the converter is operating in the forward mode. They are gated at a constant frequency with variable on time to provide the necessary regulated output voltage at the battery end, from the DC bus. The intrinsic body diodes of these switches provide rectification at the DC bus end during backup mode operation.

### *(iii) Transformer $T_1$*

The high frequency transformer $T_1$ galvanically isolates the battery from the DC bus, thereby from the loads connected to it. It also performs a voltage step-up and/or step-

down function for the converter depending on the operating mode. $N_p$ represents the transformer primary winding and each half of the center-tapped secondary is represented by $N_s$.

### *(iv) Auxiliary winding, $N_{p_1}$ and diodes $D_1$ and $D_2$*

The auxiliary winding $N_{p_1}$ and the two catching diodes $D_1$ and $D_2$ restore the centerpoint of the capacitors $C_1$ and $C_2$ to half the input DC voltage and prevent staircase saturation of the transformer during operation as a half-bridge converter. In the backup mode, these elements enable equal and simultaneous charging of $C_1$ and $C_2$, which are now the output filter capacitors.

### *(v) Switches $S_3$ and $S_4$*

The power MOSFET $S_3$ and $S_4$ are the main switching devices of the current-fed push-pull converter in the backup mode. They are switched at a constant frequency and their variable on time is controlled according to the load demand on the DC bus or the variation in the battery voltage. In the battery-charging mode, the body diodes of these switches are the rectifying elements for the half-bridge converter and carry the battery charging current, $i_{ban}$.

### *(vi) Inductor $L_o$*

The inductor $L_o$ is a part of the output filter for the half-bridge converter topology and reduces the ripple in the battery charging current. The energy stored in the inductance is used to charge the battery during the intervals when the switches $S_1$ and $S_2$ are not gated. In the backup mode, $L_o$ is in series with the energy source (battery) resulting in a current-fed push-pull topology.

*(vii) Capacitor $C_o$*

The output filter for the half-bridge comprises of $L_o$ and $C_o$. The voltage ripple at the battery side is determined by the capacitor $C_o$. $C_o$ discharges to hold up the battery voltage when primary side switches are not conducting and its charge is replenished by the energy stored in the inductor $L_o$. This capacitance does not play any significant role in the battery discharging mode.

## 2.4 OPERATING MODES OF THE CONVERTER

The converter has two modes of operation. In the forward mode the battery is charged by energy from the DC bus and in the backup mode, in the absence of the DC mains the battery discharges to power the load at the bus.

- **Forward/ Charging Mode:** In the forward/charging mode the converter operates as buck-derived topology. The energy from the DC mains charges the battery over the

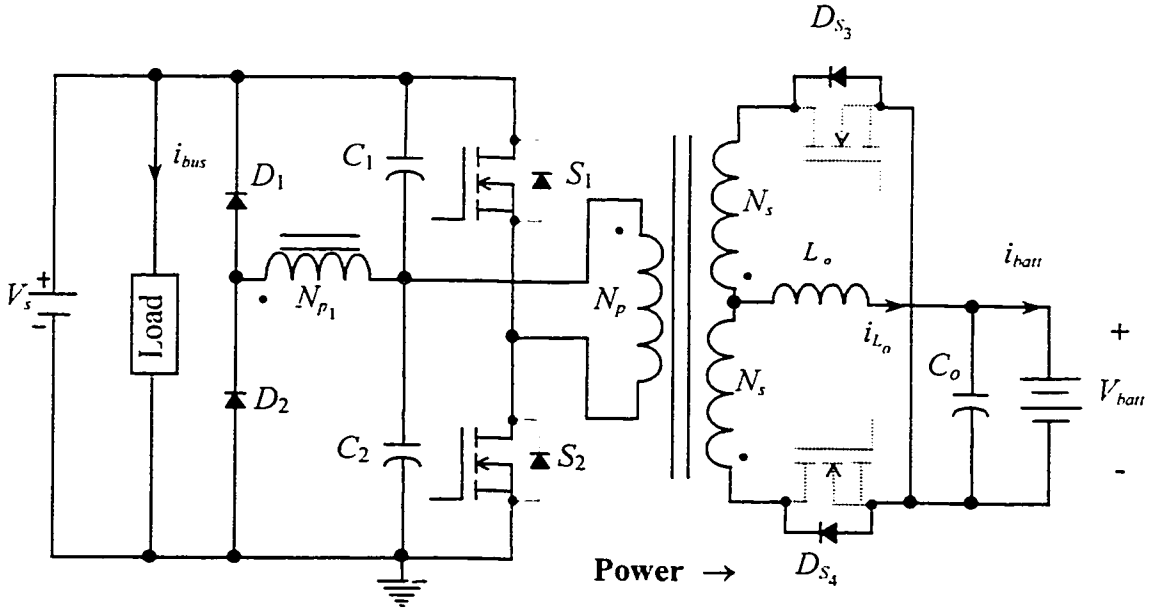



**Fig. 2-3 Converter topology in the forward mode.**

input voltage range of the bus, while also powering the down stream load converters. In this mode only the switches $S_1$ and are $S_2$ gated and the body diodes of the switches $S_3$ and $S_4$ provide battery side rectification. The converter topology for this mode of operation is shown in Fig. 2-3.

- **Backup/ Current-fed Mode:** On failure of the dc mains, reversal of power flow occurs resulting from a switchover to the battery. Now the converter operates in the boost-derived mode. The battery supplies the load power at the DC bus voltage. In this mode, the switches $S_3$ and $S_4$ are gated and the body diodes of the switches $S_1$ and $S_2$ provide rectification at the output DC bus side. This operating mode is shown in Fig. 2-4.

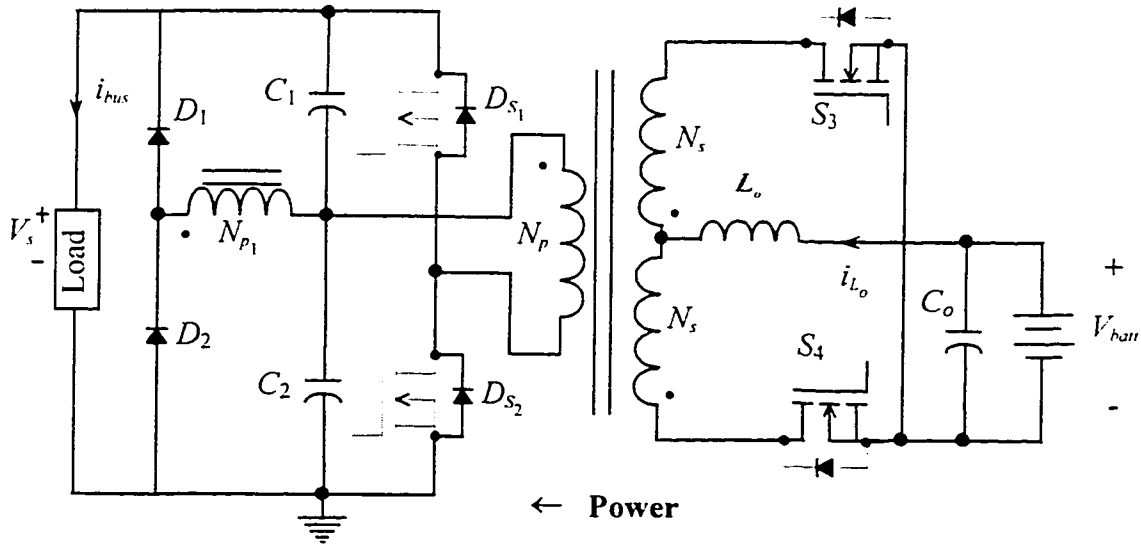



**Fig. 2-4 Converter topology in the backup mode.**

### 2.4.1 Forward/ charging mode under ideal conditions

Fig. 2-6 and Fig. 2-7 show the operation for this mode. The DC bus powers the down stream converters and charges the battery. The bus voltage, $V_S$, is bucked down by the half-bridge converter and charges the battery to the nominal voltage, $V_{batt}$, by supplying the battery charging current, $i_{batt}$. The switches $S_1$ and $S_2$ on the primary side are gated at duty ratios less than 0.5, while $S_3$ and $S_4$ are not switched at all.

The converter operation is repetitive in the switching cycle, $T_s$. The various stages of operation during one switching time period are described by the time intervals between $t_0$ to $t_4$, in the idealized waveforms of Fig. 2-5. Fig. 2-6 and Fig. 2-7 show the converter circuit for each time interval.

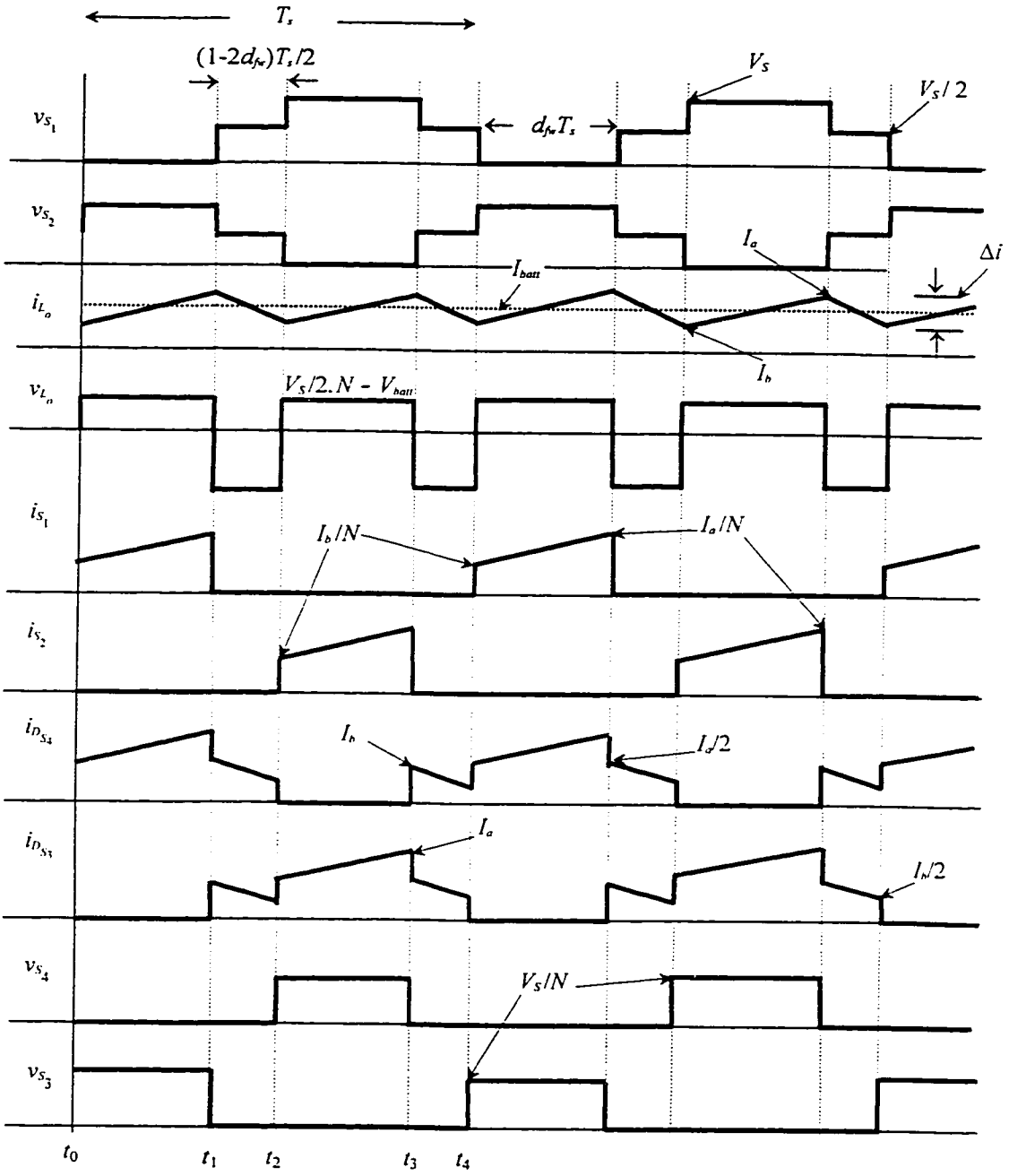


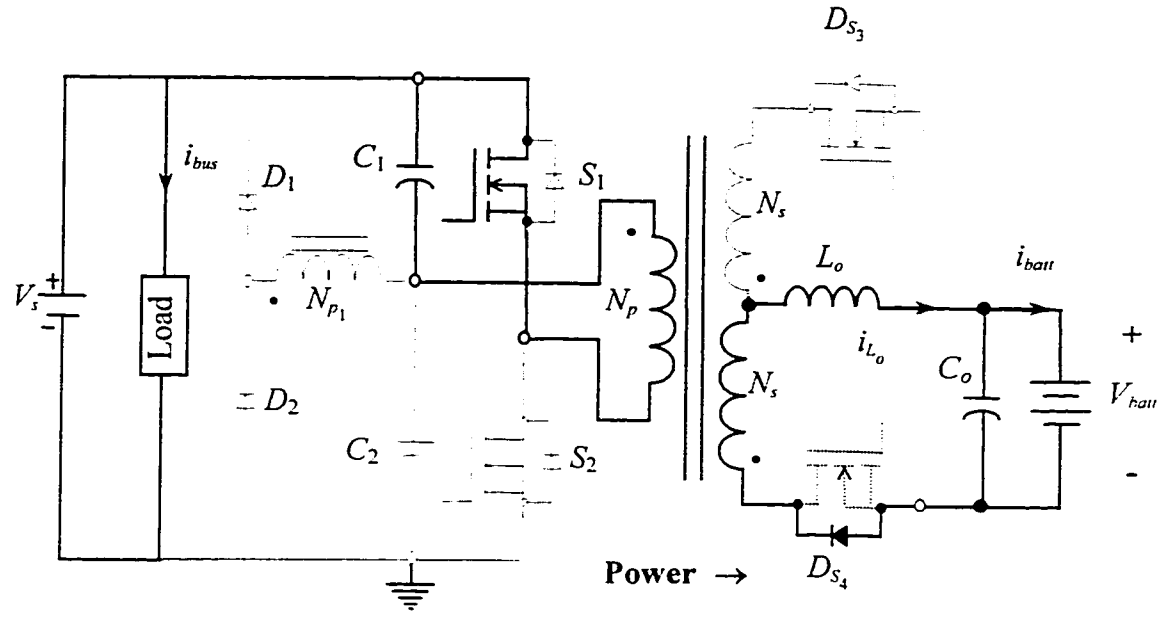

**Fig. 2-5 Idealized waveforms for the forward mode of operation.**
Waveforms for nominal input and battery voltages at full load at the battery end with switch duty ratio less than 0.5.

- ***Interval $t_0$-$t_1$:***

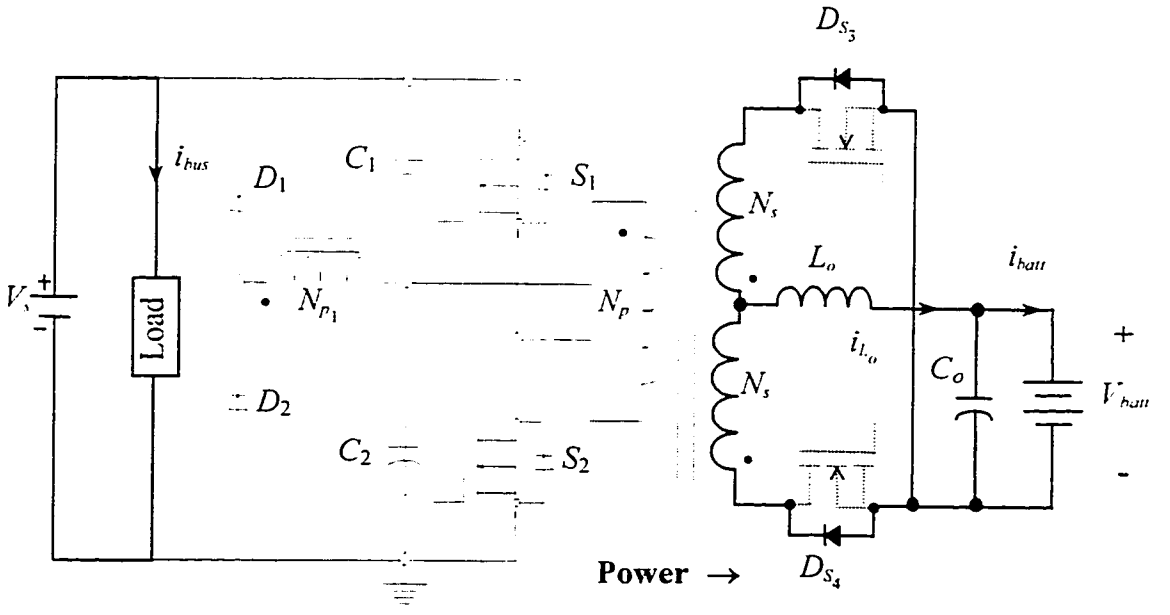
Fig. 2-6(a) shows converter operation during this time interval. Both the switches $S_1$ and $S_2$ are in the OFF state before time $t_0$. Now, switch $S_1$ is turned ON at $t_0$ for a time interval of "$d_{fw}T_s$". The converter operates as a buck-derived half-bridge. A voltage $V_s/2$ appears across the primary winding, $N_p$, and also the OFF switch, $S_2$. On the secondary side only the body diode of the switch $S_4$, $D_{S4}$, is forward biased and provides output rectification. $D_{S4}$ carries the total secondary current. $D_{S3}$ is subject to a reverse voltage stress equal to the voltage across the secondary winding of the transformer and does not carry any current during this interval. The output filter components, $L_o$ and $C_o$, provide the necessary filtering action for the current and voltage at the battery end. The voltage across the inductor results in a linear increase in the inductor current, and therefore the primary switch current $i_{S1}$ for the ON period of primary switch.

- ***Interval $t_1$-$t_2$:***

The converter operation during this time interval is shown in Fig. 2-6(b). Switch $S_1$ is turned OFF at instant $t_1$ while $S_2$ continues to remain OFF. During this dead time interval there is zero voltage across the primary, and therefore secondary windings of transformer, and no power is transferred to the secondary side. The energy stored in $L_o$ from the previous interval provides the battery power. Voltage across the inductor reverses and the inductor current $i_{L_o}$ decreases linearly as it freewheels through the body diodes $D_{S3}$ and $D_{S4}$, both of which are forward biased. The diodes share the current equally during this interval, thereby reducing the rms current through them. As none of the primary side switches, $S_1$ or $S_2$, are conducting they are subject to a reverse voltage stress across them that is equal to half the supply voltage.




**(a)**




**(b)**

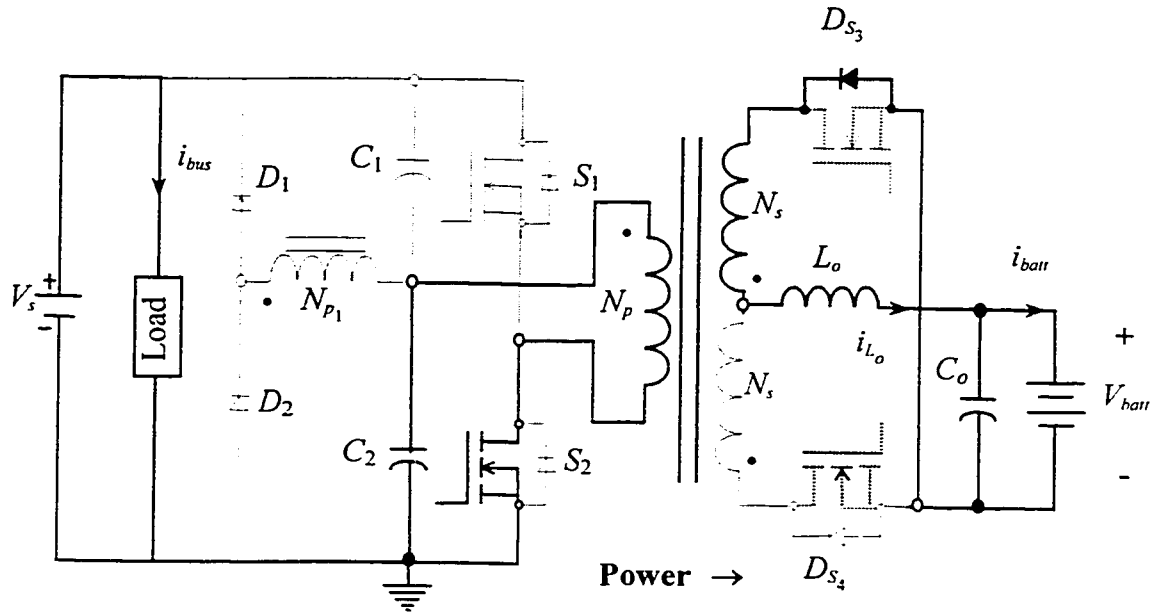
**Fig. 2-6 Converter operation in the forward mode.**
(a) Interval $t_0 - t_1$. (b) Interval $t_1 - t_2$.

- ***Interval $t_2$-$t_3$:***

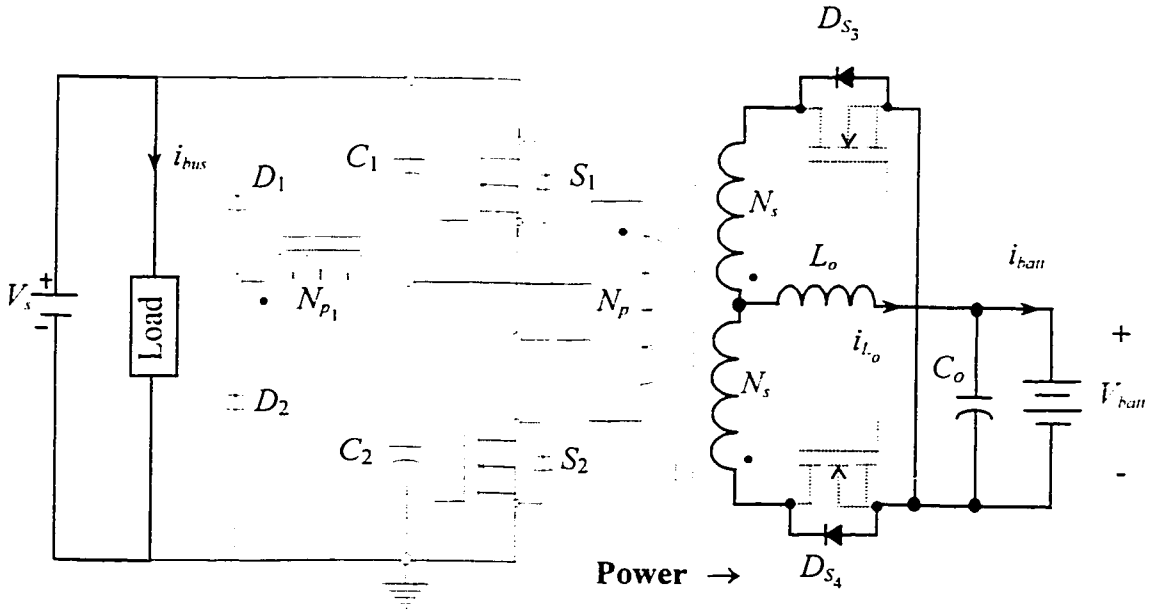
Fig. 2-7(a) describes the converter circuit during this interval. The switch $S_2$ is turned ON at instant $t_2$ while $S_1$ continues to remain in the OFF state. The operation of the converter is similar to that during the interval $t_0$-$t_1$, with $S_2$ and $S_3$ being analogous to $S_1$ and $S_4$ in the interval $t_0$-$t_1$. Now $S_2$ carries the primary side current and the body diode of switch $S_3$, $D_{S3}$, conducts and provides secondary side rectification. The voltage and current stresses for the switches in the OFF and ON states are identical to those in the interval $t_0$-$t_1$.

- ***Interval $t_3$-$t_4$:***

Converter operation during this interval is similar to that in the interval $t_1$ - $t_2$. None of the primary side switches is ON and the battery charging current, is provided by the energy stored in the inductor. The body diodes of both the switches on the secondary side, $D_{S3}$ and $D_{S4}$, conduct simultaneously and share the inductor current equally. This interval is depicted in Fig. 2-7(b).




**(a)**




**(b)**

**Fig. 2-7 Converter operation in the forward mode.**
(a) Interval $t_2 - t_3$. (b) Interval $t_3 - t_4$.

### 2.4.2 Forward mode operation with flux imbalance

The time intervals $t_0 - t_4$ describe the half-bridge operation of the bi-directional converter in the forward/battery-charging mode under ideal conditions without any flux imbalance. As explained in section 2.2.2 of the text, if the voltage at the junction of the capacitors, $C_1$ and $C_2$ drifts away from the ideal condition of half the input DC supply voltage it may result in saturation of the transformer core and thereby damage the power switches irreversibly. Fig. 2-3 shows the balancing winding $N_{p_1}$ and two catching diodes $D_1$ and $D_2$ that maintain the centerpoint voltage at the junction of $C_1$ and $C_2$. The phasing of the balancing winding is in series with the primary winding $N_p$. By the nature of the two series windings of identical turns, the centerpoint of the high voltage capacitors is forced to one-half of the input DC voltage. Any drift in the midpoint voltage will cause a small amount of restoration current to flow through the balancing winding and the diodes. The primary circuit path in the event of a flux imbalance condition when either switch is shown in Fig. 2-8.

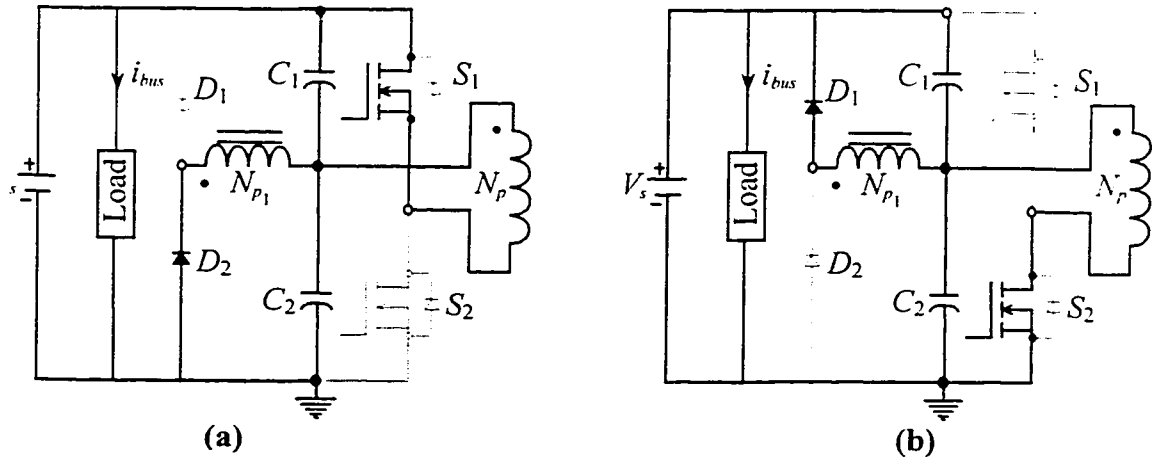



**Fig. 2-8 Converter operation in the forward mode under flux imbalance conditions.**
(a) When switch $S_1$ is ON. (b) When switch $S_2$ is ON.

### 2.4.3 Backup/ Current Fed Mode

The converter operates in this mode, Fig. 2-4, on failure of the DC mains. The backup mode is the boost-derived mode of operation. In the absence of the DC bus, the battery discharges to supply power to the down stream converters connected to the DC bus. The switches $S_3$ and $S_4$ of the current fed push-pull topology are gated at duty ratios greater than 0.5. Rectification at the output is provided by the body diodes of the switches $S_1$ and $S_2$. The backup mode is described with reference to the waveforms presented in Fig. 2-9. As in the charging mode, inductor current is assumed to be continuous. The time intervals between $t_0$ to $t_4$ describe the converter operation, which is repetitive over a switching cycle, $T_s$. Each time interval is also represented by the converter circuits in Fig. 2-10 and Fig. 2-11.

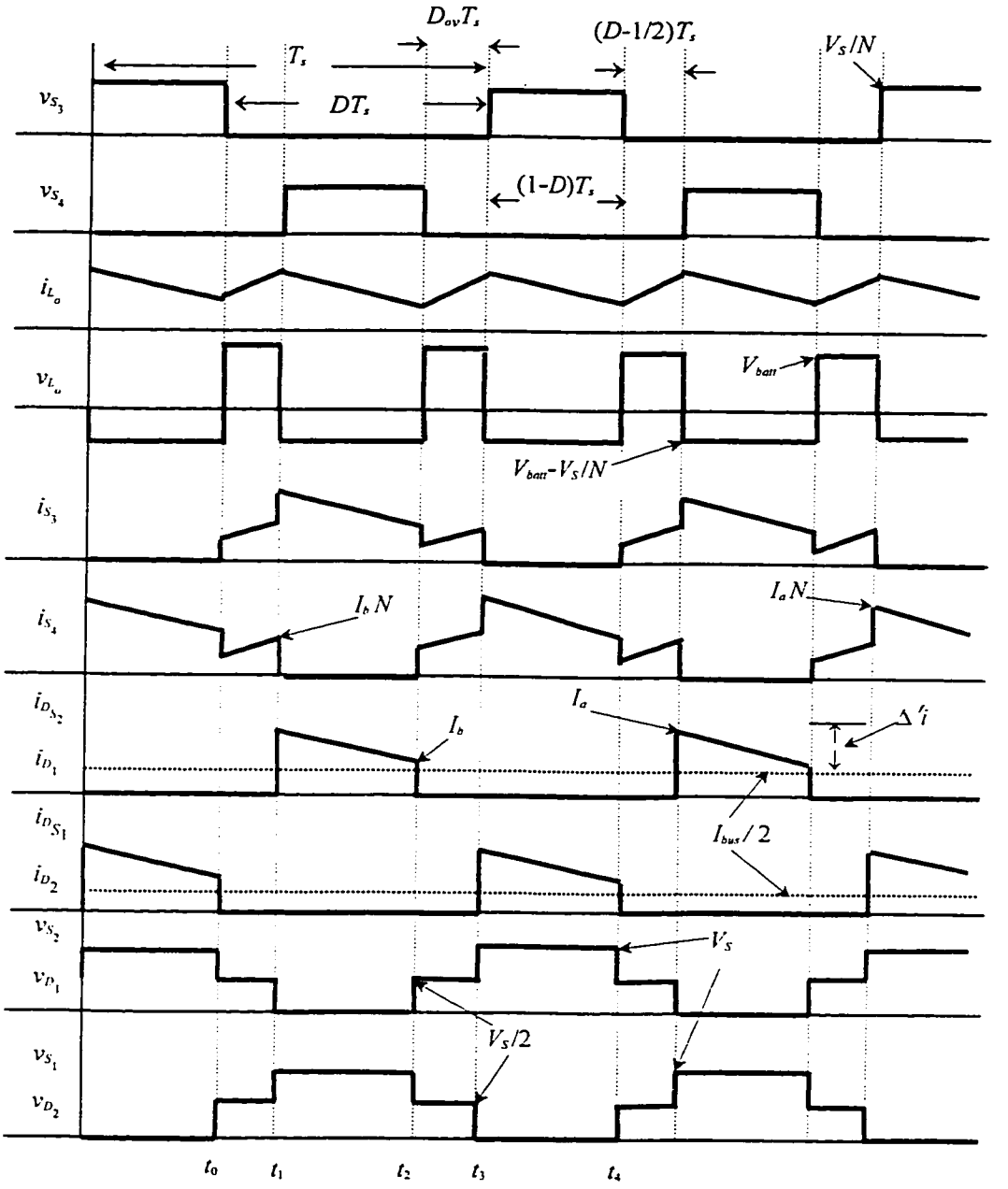


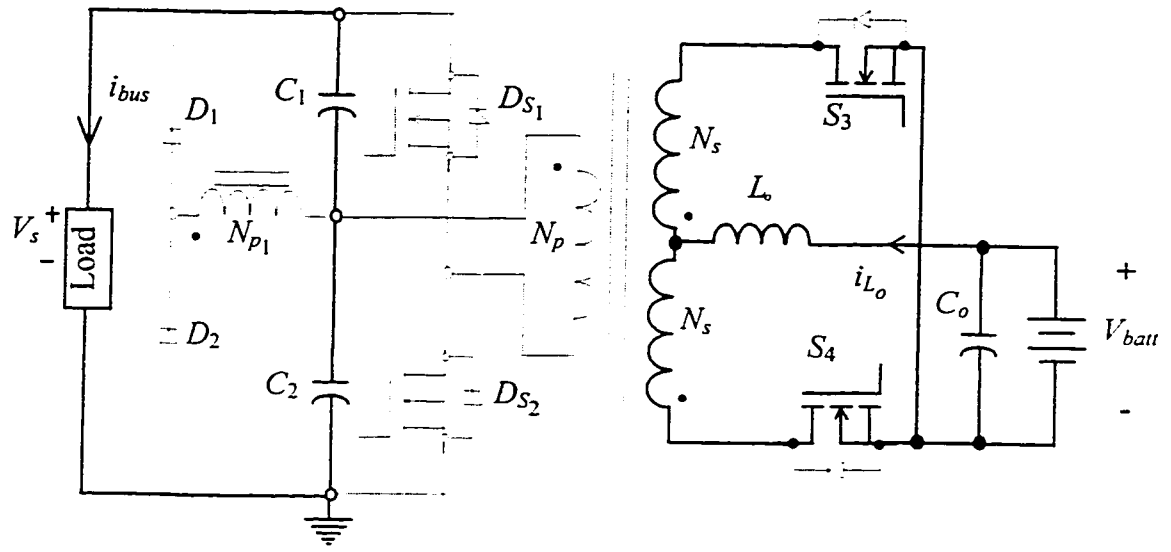

**Fig. 2-9 Idealized waveforms for converter operation in the backup mode.** Waveforms for nominal DC bus and battery voltages at full load at the DC bus end with switch duty ratio greater than 0.5.

- ***Interval $t_0$-$t_1$:***

Switch $S_4$ is assumed to be in the ON state before the time instant $t_0$ and $S_3$ is turned ON at $t_0$ with an ON time equal to $DT_s$. The converter topology during this time interval is shown in Fig. 2-10(a). The transformer secondary windings, $N_S$, are subject to an effective short circuit, which causes the inductor, $L_o$, to store energy as the total battery voltage appears across it. The inductor current, $i_{L_o}$, ramps up linearly and is shared equally by both $S_3$ and $S_4$. During this interval, energy stored in the output bulk capacitors, $C_1$ and $C_2$, provides the load power at the DC bus. There is no transfer of energy from the battery end to the DC bus end. None of the body diodes of the primary side switches is conducting and they are subject to a reverse voltage stress equal to half the output voltage at the DC bus.

- ***Interval $t_1$-$t_2$:***

$S_4$ is turned OFF at instant $t_1$ while $S_3$ continues to remain ON during this interval, described by Fig. 2-10(b). The energy stored in $L_o$ during the previous interval replenishes the charge in the output bulk capacitors and provides load power at the bus. through the body diode $D_{S_2}$ and the diode $D_1$. Consequently, the inductor current ramps down and will reach the value equal to that at instant $t_0$ if the operation is in steady state. Voltages across the auxiliary winding $N_{p_1}$ and the primary winding $N_p$ are identical due to their series phasing and equal number of turns. Thus, equal currents flow through $D_1$ and $D_{S_2}$ allowing simultaneous and equal charging of both $C_1$ and $C_2$, respectively.



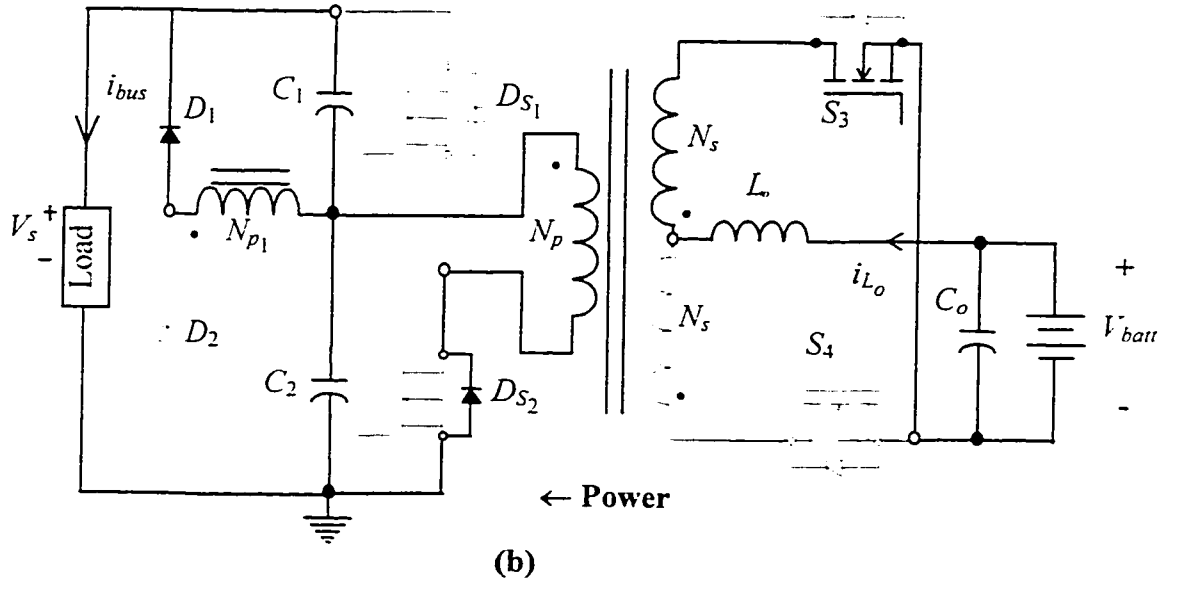



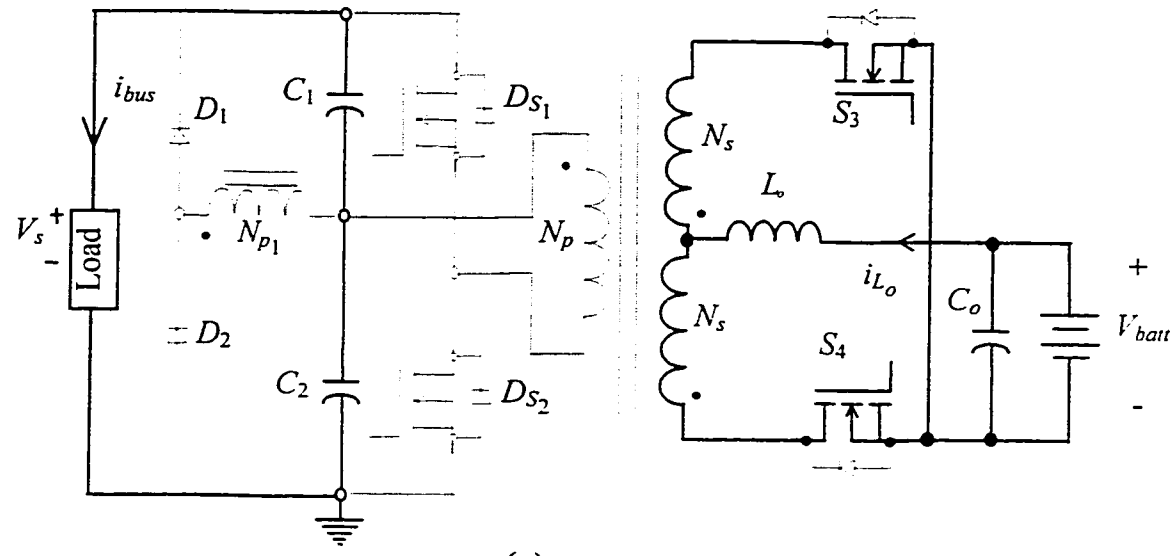

**Fig. 2-10 Converter operation in the backup mode.**
(a) Interval $t_0 - t_1$. (b) Interval $t_1 - t_2$.

- ***Interval $t_2$-$t_3$:***

This interval , Fig. 2-11(a), is similar to interval $t_0$-$t_1$. Switch $S_3$ remains ON and $S_4$ is switched ON at time $t_2$. The duty ratio for $S_3$ is therefore greater than 0.5. With both $S_3$ and $S_4$ turned ON, the transformer secondary is effectively shorted and the inductor core stores energy, resulting in a linear rise in inductor current, $i_{L_o}$. Voltage across both $N_p$ and $N_{p_1}$ is zero, so load power is supplied by the discharge of the bulk capacitors. Current and voltage stresses for the switches on the battery side and the load side are identical to those across them in the interval $t_0 - t_1$.

- ***Interval $t_3$-$t_4$:***

Converter operation during this interval, Fig. 2-11(b), resembles that during the interval $t_1$-$t_2$. $S_4$ remains ON and $S_3$ is switched OFF at instant $t_3$. The stored energy in $L_o$ is transferred to the primary side of the converter through the switch conducting on the secondary side, $S_4$, and the primary diodes $D_{S_1}$ and $D_2$. The conduction of $D_{S_1}$ and $D_2$ results in equal charging of $C_1$ and $C_2$, respectively.

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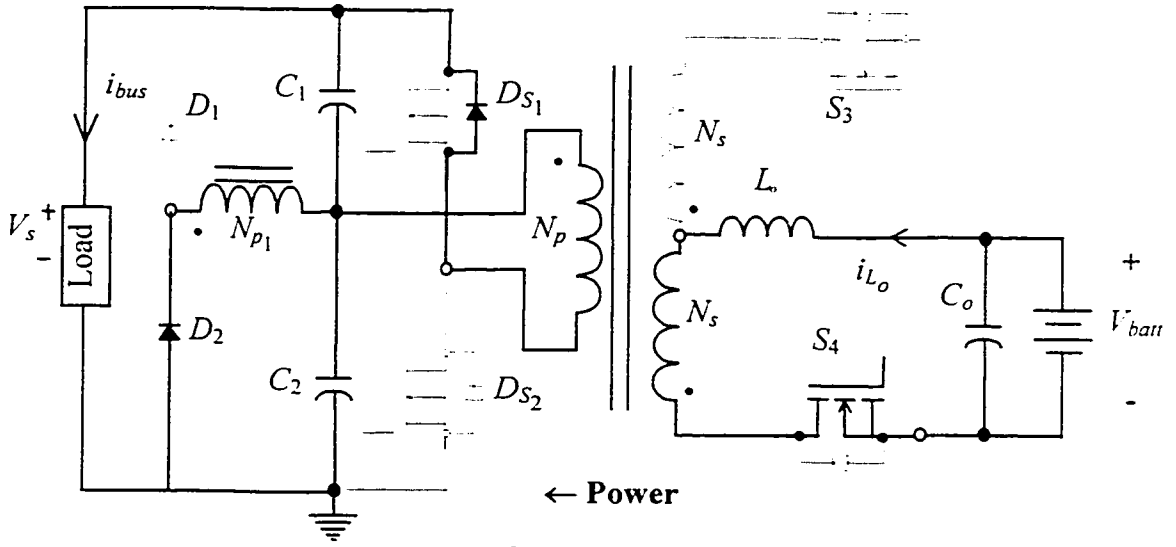



**(b)**

**Fig. 2-11 Converter operation in the backup mode.**
(a) Interval $t_2$ - $t_3$.(b) Interval $t_3$ - $t_4$.

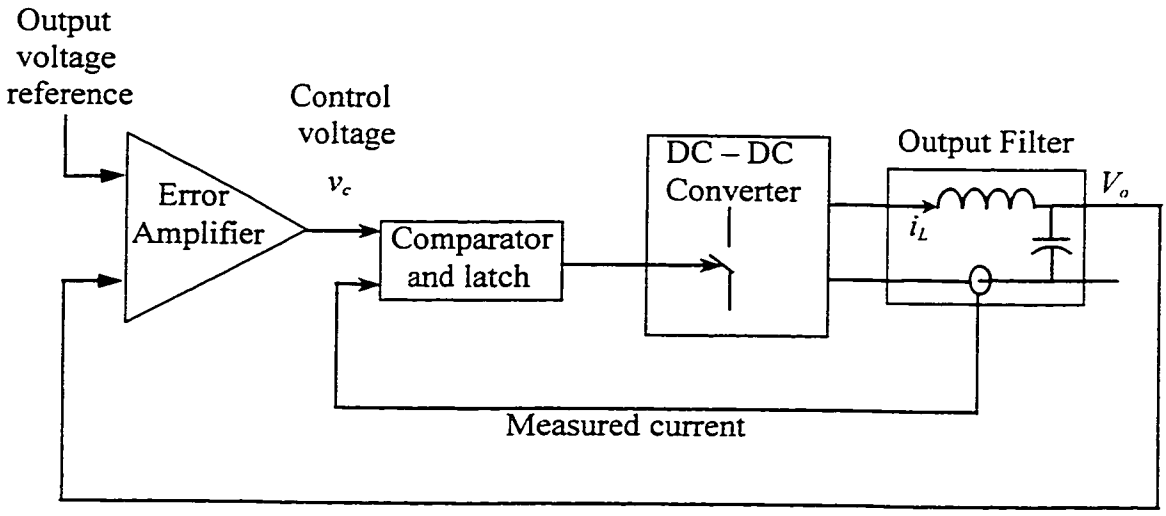
## 2.5 CONTROL PRINCIPLE

The average dc output in DC-DC converters must be regulated within a specified tolerance band around its nominal value in response to changes in the output load and the input voltage variations. Keeping the switching frequency constant, the output voltage of the converter is maintained at the desired level by varying the on time of the switch(es). Voltage or current mode control techniques are used for the regulating the voltage at the output of a converter.

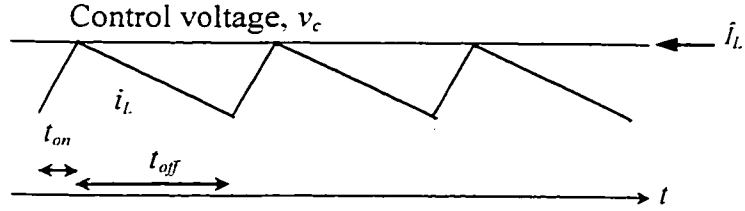
Current mode control, with an additional inner control loop directly controls the inductor current with the error signal rather than controlling the duty ratio of the pulse width modulator. Current mode control presents many advantages, such as:

- improved transient response due to the faster inner current loop,
- automatic symmetry correction which eliminates the problem of transformer core saturation in most topologies,
- simpler loop compensation as it removes one pole from the control-to-output transfer function, especially in the presence of the right-half-plane zero,
- inherent feed-forward of the input voltage,
- capability for modular design of power supplies whereby several power supplies can be operated in parallel and provide equal currents, and
- inherent pulse by pulse limiting of the switch current by measuring it directly or indirectly somewhere in the circuit.

In the proposed converter, both the forward and backup modes use peak current-mode control, Fig. 2-12, to regulate the output voltage. The necessary control action on




**(a)**




**(b)**

**Fig. 2-12 Peak current-mode control.**
(a) Basic logic circuit. (b) Relevant waveforms.

the switch duty ratio is achieved by limiting the peak value of the sensed current against an error signal generated by the comparison of the output voltage with its reference value.

## 2.6 CONCLUSIONS

The bi-directional dc-dc converter is based two converter topologies, namely the half-bridge and the current-fed push-pull. The reasons justifying the choice of these topologies over possible other implementations are presented in this chapter. Bi-

directional converter operation in the forward mode as a buck-derived half-bridge converter and in the backup mode as a boost-derived current-fed push-pull converter is described over one steady state switching period. The advantages of using peak current-mode control for converter regulation are also mentioned.

# CHAPTER 3

# STEADY STATE ANALYSIS

## 3.1 INTRODUCTION

The previous chapter presented the details on the topology, operating modes and the basic elements of the proposed bi-directional dc-dc converter. In order to design a converter it is necessary to quantify circuit characteristics, such as the currents flowing through its elements, the voltages across these elements etc. Thus, the selection of components for the bi-directional converter is influenced by various circuit parameters and operating conditions. The design oriented steady state analysis of the converter in both operating modes provides design equations from which numerical values for steady state converter performance and component stresses are computed and used in the component selection process.

The design oriented steady state analysis is based on the pertinent idealized waveforms shown in Fig. 2-5 and Fig. 2-9. The key concept in the ensuing analysis is the fact that the converter must be boost-derived under all conditions in the backup mode and buck derived under all conditions in the forward mode. Thus the output voltage in the backup mode should always be greater than or at least equal to the lower limit of the DC bus voltage range; an operating condition that is specified before the converter design

commences. This condition must be satisfied under the worst case when the secondary switches are operating at minimum duty ratio with maximum battery voltage. This constraint determines the nominal battery voltage for a given turns ratio of the transformer which consequently effects all other circuit parameters.

The circuit parameters are normalized in this worst case analysis to ensure validity of the results and suitable converter operation over a wide range of operating conditions. Using the steady state design expressions, characteristic curves are generated for the circuit parameters to aid the component selection process. These curves are plotted as a function of the variation in the input DC bus. Other relevant qualitative considerations that must be accounted for while selecting the components in an experimental setup are also presented.

Finally, one must also bear in mind the dual set of constraints arising from the use of the same power circuit for both the operating modes and therefore choose the components accordingly.

## 3.2 SIMPLIFYING ASSUMPTIONS FOR STEADY STATE ANALYSIS

The following simplifying assumptions are made for the steady state analysis of both operating modes. Despite the limitations imposed by these assumptions. the expressions derived in the following sections are accurate enough for practical design purposes.

1. The circuit is operating under steady state, implying that all voltages and currents are periodic.

2. The switches are ideal. Therefore in the conducting state the voltage drops across them are zero and they have infinite resistance in the blocking state.
3. The transformer is ideal with unity turns ratio.
4. The output capacitor is very large and the output voltage is held constant.
5. All circuit parameters are normalized over their base quantities and referred to the primary of the isolation transformer. Secondary side variables reflected to the primary are denoted by a prime " ' ".
6. The output power of the converter in the forward/battery-charging mode is between one-half and one-third the output power delivered in the backup mode.
7. The maximum theoretical duty ratio of the switching devices in the forward mode is 0.5 and the minimum theoretical duty ratio for the switching devices in the backup mode is 0.5.
8. The range in the input DC bus is specified which therefore determines the nominal battery voltage.

## 3.3 DEFINING THE BASE QUANTITIES

To normalize the circuit parameters for the analysis base quantities for voltage. power and frequency are defined and those for impedance and current are derived from the basic defined base quantities.

The output DC bus voltage in the backup mode, $V_S$, is chosen as the base voltage.

1 pu voltage, $V_{base} = V_S$ volts.

The output power at the DC bus in the backup mode is defined as the base power.

1 pu power, $P_{base} = P_{bus}$ watts.

The converter switching frequency in the backup mode is chosen as the base value for frequency.

1 pu frequency, $f_{base} = f_s$ hertz.

Using these defined base quantities the derived base quantities for impedance and current are expressed as,

1 pu current, $I_{base} = P_{bus} / V_S$ amps (base value for current),

1 pu inductance, $L_{base} = P_{bus} / 2\pi f_s$ henries (base value for inductance), and

1 pu capacitance, $C_{base} = 1 / 2\pi f_s P_{bus}$ farads (base value for capacitance).

## 3.4 STEADY STATE ANALYSIS OF THE FORWARD/ CHARGING MODE

The half-bridge operation of the converter in the forward mode is analyzed for continuous inductor current at a fixed switching frequency. The equivalent circuits of Fig. 3-1 represent the two different states of forward mode operation with all parameters reflected to the primary of the isolation transformer.

Fig. 3-1(a) is the equivalent circuit representation of converter when either one of the primary side switches $S_1$ or $S_2$ is in the ON state, for a time interval of $d_{fw} T_s$.

Fig. 3-1(b) is the equivalent circuit representation of the forward mode for the interval $(1-d_{fw})T_s$ when none of the primary side switches is being gated. The output power is delivered by the energy stored in the inductor. Both the body diodes conduct simultaneously and share the battery charging current equally.

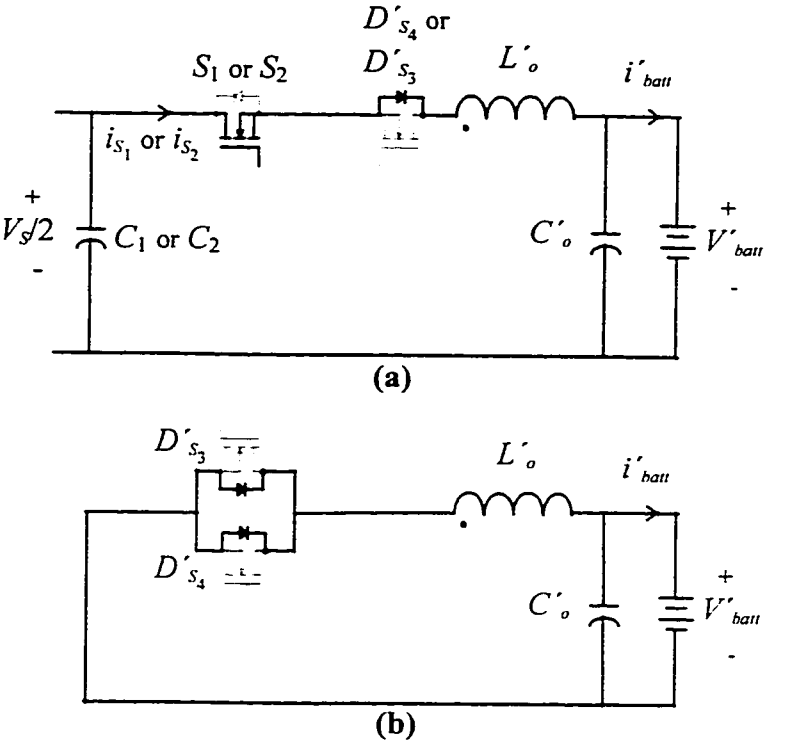



**Fig. 3-1 Equivalent circuit for the forward mode.**
(a) Either $S_1$ or $S_2$ is ON. (b) $S_1$ and $S_2$ are both OFF.

### 3.4.1 Duty ratio of switches $S_1$ and $S_2$

The maximum theoretical ON time for the primary side switches, $d_{fw}T_s$, is 50% of the switching time period $T_s$. The maximum and minimum duty ratios of $S_1$ and $S_2$, $d_{fw_{max}}$ and $d_{fw_{min}}$ are given by the following expressions:

$$d_{fw_{max}} = \frac{V'_{batt_{max}}}{V_{S_{min}}} \tag{3.1}$$

$$d_{fw_{min}} = \frac{V'_{batt_{max}}}{V_{S_{max}}} \tag{3.2}$$

where $V'_{batt_{max}}$ is the normalized value of the maximum battery voltage and $V_{S_{max}}$ and

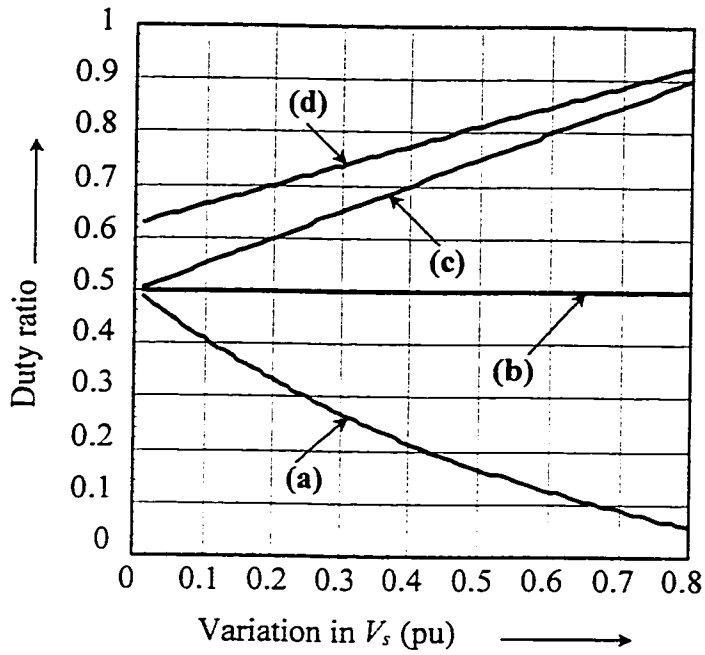



**Fig. 3-2 Duty ratio for switches $S_1$ to $S_4$.**

(a) Minimum duty ratio of $S_1$ and $S_2$. (b) Maximum duty ratio of $S_1$ and $S_2$. (c) Minimum duty ratio of $S'_3$ and $S'_4$. (d) Maximum duty ratio of $S'_3$ and $S'_4$.

$V_{S_{min}}$ are the maximum and minimum voltages at the DC bus in the forward mode. The theoretical values of the duty ratios for a specified variation in the DC bus voltage from its nominal value are shown in Fig. 3-2.

In a practical setup a dead time is provided between the turn OFF instant of one switch and the turn ON of the other to ensure that they do not overlap and thereby present a short circuit at the transformer primary.

### 3.4.2 Minimum value of output inductor $L'_o$

The current through $L'_o$ is assumed to be continuous over the entire operating range of the bi-directional converter in the forward mode. The minimum required value of the output inductor, $L'_{o_{min}}$, is calculated at the boundary of continuous and discontinuous conduction of the inductor under minimum load conditions (i.e. when the

battery draws minimum charging current) at the maximum input DC bus voltage. This lower limit for the inductance value is expressed as

$$L'_{o_{min}} = \frac{V'_{batt_{max}}}{4 \cdot f_s \cdot I'_{batt_{min}}} \cdot \left(1 - 2d_{fw_{min}}\right) \text{ pu}, \tag{3.3}$$

where $I'_{batt_{min}}$ is the minimum pu battery charging current and $V'_{batt_{max}}$ the normalized value of the maximum battery voltage. Fig. 3-3 shows $L'_{o_{min}}$ as a function of the specified variation in the input DC bus voltage for typical values of the power at the battery end.

The actual value of the inductor in an experimental setup maybe larger than $L'_{o_{min}}$ depending on the ripple current specifications for the battery charging current. A suitable tradeoff is be made between the output current ripple, $\Delta' i$, and the size of the inductor.

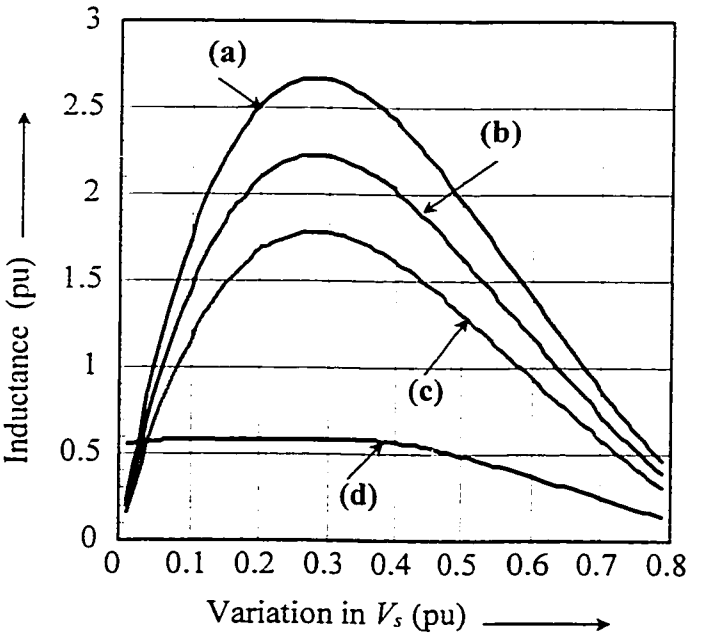



**Fig. 3-3 Minimum value of inductance to maintain continuous inductor current.**
(a) Forward mode, $P_{batt} = 0.33$ pu. (b) Forward mode, $P_{batt} = 0.4$ pu. (c) Forward mode, $P_{batt} = 0.5$ pu. (d) Backup mode, $P_{bus} = 1.0$ pu.

### 3.4.3 Maximum voltage across switches $S_1$ and $S_2$

Power switches are generally the least reliable components within a power supply and must be selected carefully. The selection of the appropriate switch depends primarily on the voltage stresses across it and the rms current through it. The switch must be rated to withstand the maximum reverse voltage across it.

The maximum reverse voltage across the primary side switches, $S_1$ and $S_2$, is equal to the maximum input voltage at the DC bus which is given by the expression,

$$V_{S_1 max} = V_{S_2 max} = V_{S_{max}} \text{ pu} \tag{3.4}$$

where, $V_{s_{max}}$ is the maximum input DC bus voltage. The maximum voltage stress across $S_1$ and $S_2$ are shown in Fig. 3-4.

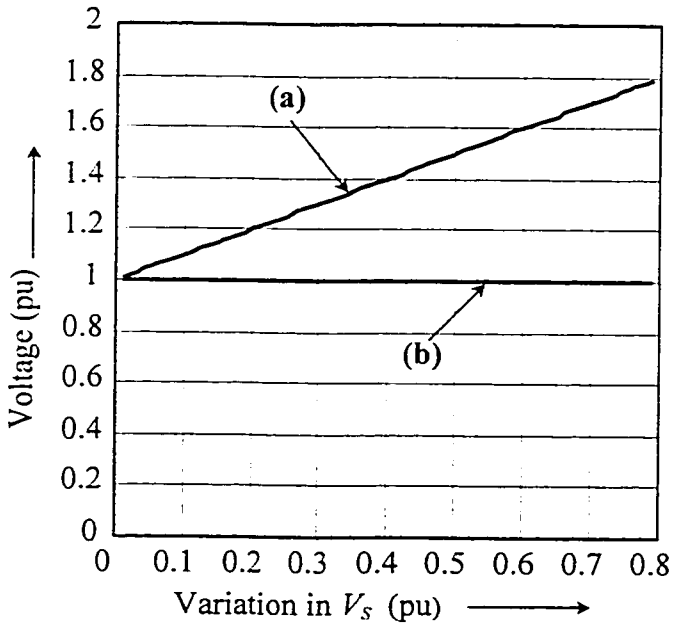



**Fig. 3-4 Maximum voltage stress across switches $S_1$ and $S_2$.**
(a) Forward mode. (b) Backup mode.

### 3.4.4 Maximum current through switches $S_1$ and $S_2$

Once the voltage rating for the switches is determined (3.4), the required current handling capability of the switch must also be calculated. The maximum rms current through the primary side switches, $I_{S_{1rms}}$ and $I_{S_{2rms}}$, is defined under the worst case of minimum input voltage and maximum battery charging current, $I'_{batt_{\max}}$.

The maximum rms current through the switch is given by,

$$I_{S_{1rms}} = I_{S_{2rms}} = \frac{1}{2\sqrt{3}}\sqrt{(12{I'_{batt_{\max}}}^2 + \Delta i'^2)\cdot d_{fw_{\max}}} \quad \text{pu} \tag{3.5}$$

where $\Delta i'$ is the normalized value of the ripple in the inductor current. Fig. 3-5 shows the design curves for the maximum rms current through $S_1$ and $S_2$ for the typical battery charging power levels.

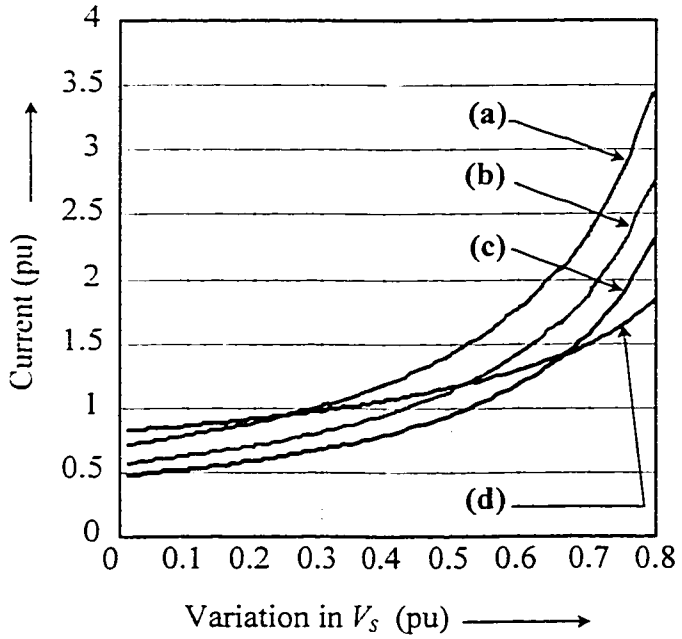



**Fig. 3-5 Rms current through the switches $S_1$ and $S_2$.**
(a) Forward mode, $P_{batt}$ = 0.5 pu. (b) Forward mode, $P_{batt}$ = 0.4 pu. (c) Forward mode, $P_{batt}$ = 0.33 pu. (d) Backup mode, $P_{bus}$ = 1.0 pu.

### 3.4.5 Maximum voltage across the switches $S'_3$ and $S'_4$

The body diodes of the switches $S'_3$ and $S'_4$ provide rectification at the secondary side of the high frequency transformer. Thus, $D'_{S_3}$ and $D'_{S_4}$, are subject to maximum reverse voltages when they are reverse biased. The maximum voltage is determined from when only one diode is in the circuit path. The voltage stress across the body diode and therefore the switch itself, is given by,

$$V'_{DS3\,max} = V'_{DS4\,max} = V_{S_{max}} \quad \text{pu} \tag{3.6}$$

Fig. 3-6 shows the voltage across the secondary side switches reflected to the primary.

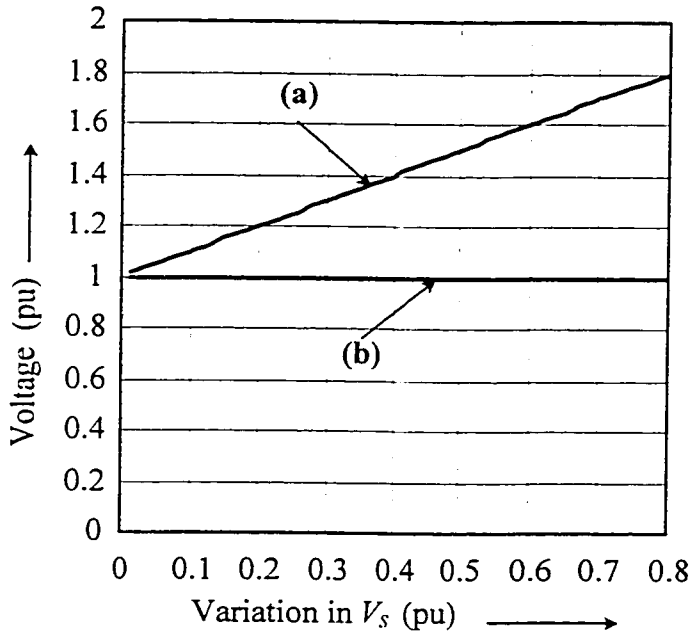



**Fig. 3-6 Maximum voltage stress across switches $S'_3$ and $S'_4$.**
(a) Forward mode. (b) Backup mode.

### 3.4.6 Maximum current through switches $S'_3$ and $S'_4$

The body diodes, $D'_{S3}$ and $D'_{S4}$, carry the battery charging current. The average current through these diodes is therefore calculated to select the switches $S'_3$ and $S'_4$ with appropriate current ratings. The average current through the diodes over one switching time period computed for the worst case condition of minimum input voltage and maximum load conditions is shown in Fig. 3-7 and is given by the expression:

$$I'_{D_{S3_{avg}}} = I'_{D_{S4_{avg}}} = \frac{I'_{batt_{max}}}{2} \text{ pu} \tag{3.7}$$

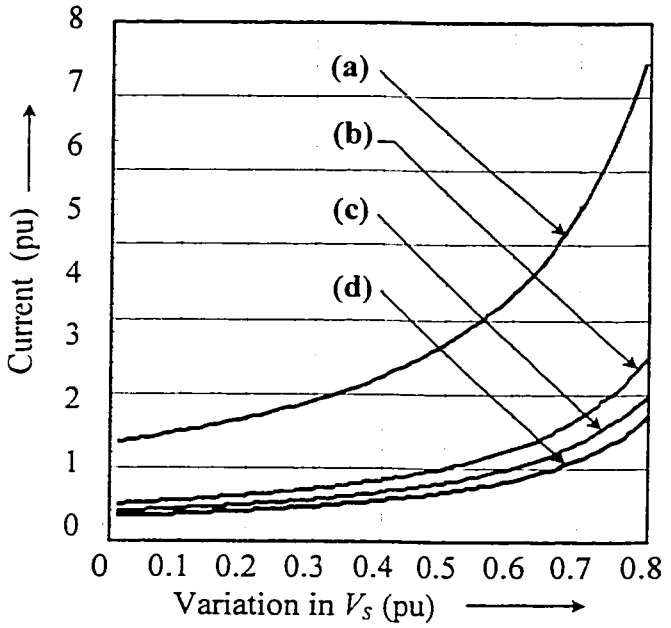



**Fig. 3-7 Average current through the switches $S'_3$ and $S'_4$.**
(a) Backup mode, $P_{bus}$ = 1.0 pu. (b) Forward mode, $P_{batt}$ = 0.5 pu. (c) Forward mode, $P_{batt}$ = 0.4 pu. (d) Forward mode, $P_{batt}$ = 0.33 pu.

### 3.4.7 Output capacitor $C'_o$

While operating in the forward mode, if the battery is suddenly removed, the energy stored in the inductor $L'_o$ must be discharged into the output filter capacitor $C'_o$. This constraint and the maximum allowable value of output voltage ripple on $V'_{batt}$, based on the parasitic equivalent series resistance (*esr*) of the capacitor, define the choice of the filter capacitor $C'_o$. The first, and the dominant, constraint gives the minimum possible value of capacitor that can be used as,

$$C'_o = \frac{L'_o \cdot I'^{\,2}_{batt_{max}}}{V'^{\,2}_{batt_{peak}} - V'^{\,2}_{batt}} \text{ pu} \tag{3.8}$$

where, $V'_{batt_{peak}}$ is the peak allowable battery voltage when the load is removed. Fig. 3-8 shows the capacitor value for different values of output power in the forward mode.

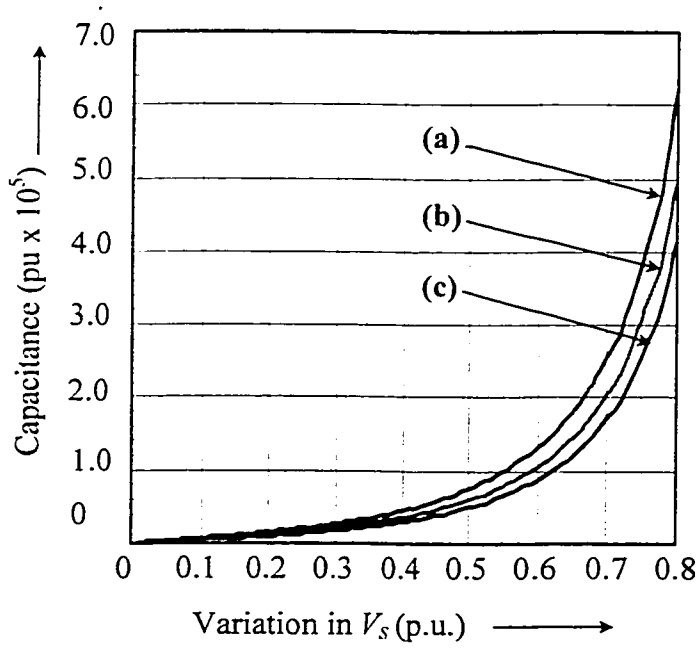



**Fig. 3-8 Output capacitor, $C'_o$.**
(a) Forward mode, $P_{batt}$ = 0.5 pu. (b) Forward mode, $P_{batt}$ = 0.4 pu. (c) Forward mode, $P_{batt}$ = 0.33 pu.

### 3.4.8 Input capacitors $C_1$ and $C_2$

The input bulk capacitors, $C_1$ and $C_2$, Fig. 3-1(a), provide a split voltage source for switches $S_1$ and $S_2$ and are equal in value. These bulk capacitors must provide adequate filtering action for the input voltage ripple, $V_{ripple}$. They must also be large enough to provide sufficient hold up time at the DC bus voltage under dc mains failure, before the converter begins operation in the backup mode. The value of the capacitors is calculated from the expression given below and is shown as a function on the DC bus variation in Fig. 3-9.

$$C_1 = C_2 = \frac{2 \cdot I_{pri}}{V_{ripple}} \cdot t_{dis} \text{ pu} \tag{3.9}$$

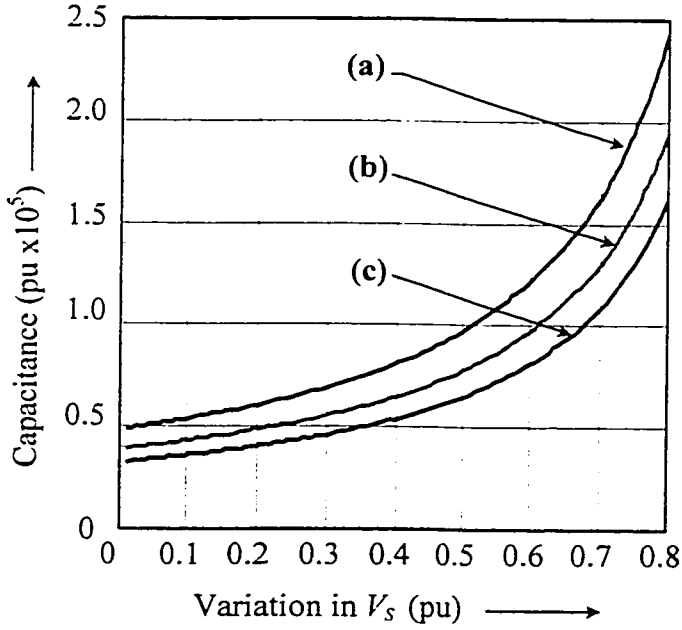



**Fig. 3-9 Input capacitor, plotted as a function of the DC bus variation.**
(a) Forward mode, $P_{batt} = 0.5$ pu. (b) Forward mode, $P_{batt} = 0.4$ pu. (c) Forward mode. $P_{batt} = 0.33$ pu.

where $t_{dis}$ is the capacitor discharge period and $I_{pri}$ is the primary current at minimum input voltage and maximum battery charging current, calculated for an expected converter efficiency of $\eta = 80\,\%$ and is expressed as,

$$I_{pri} = \frac{P'_{batt} \cdot d_{fw_{max}}}{V'_{batt_{max}}} \cdot \frac{100}{\eta} \text{ pu} \tag{3.10}$$

### 3.4.9 Balancing winding $N_{p1}$ and catching diodes $D_1$ and $D_2$

As described in section, the balancing winding $N_{p1}$ must have the same number of turns as the transformer primary winding $N_p$ and be phased in series with it through the ON time of $S_1$ and $S_2$. This will maintain the voltage at the midpoint of $C_1$ and $C_2$ to half the input bus voltage.

As MOSFETs mismatches are small, the average current in the winding and the catching diodes is very small, in mA. Therefore, a wire with smaller diameter can be used for $N_{p1}$ and the current rating of $D_1$ and $D_2$ is also small.

## 3.5 Steady State Analysis for the Backup/ Current Fed Mode

The procedure for the steady state analysis of the backup mode is similar to that of the forward mode. It provides the necessary design equations and characteristic curves for the circuit parameters, plotted as a function of the specified variation in the DC bus voltage about its nominal value. The analysis is based on the idealized waveforms shown in Fig. 2-9 for continuous inductor current.

The equivalent circuits of Fig. 3-10 represent the circuit states of converter operation in the backup mode. All circuit parameters have been normalized by reflecting the secondary side parameters to the primary side of a transformer with unity turns ratio.

The equivalent circuit of Fig. 3-10(a) represents the operation of the converter in the backup mode during the time interval $D_{ov}T_s$, when both switches $S'_3$ and $S'_4$ are ON. The entire battery voltage appears across the inductor. The diode $D_{eq}$ is reverse biased and does not conduct. Output power is supplied by the energy stored in the capacitor $C_{eq}$, which is the equivalent circuit representation of the capacitors $C_1$ and $C_2$ in series.

The equivalent circuit of Fig. 3-10(b) represents the time interval $DT_s$ when any one of the switches, $S'_3$ and $S'_4$, is ON and power is delivered from the battery to the load. $D_{eq}$ is forward biased and carries the load current. $D_{eq}$ is the circuit representation of

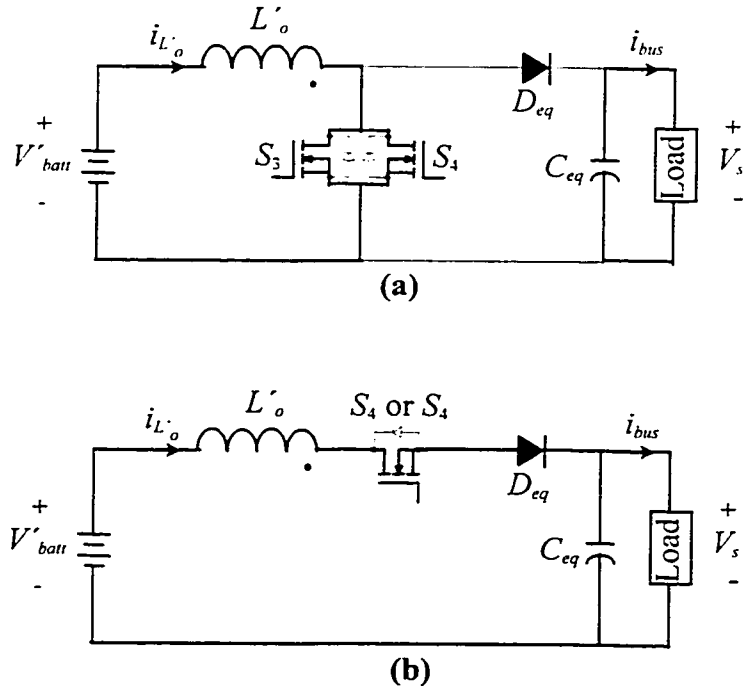



**Fig. 3-10 Equivalent circuit for the backup mode.**
(a) Both switches $S'_3$ and $S'_4$ are ON. (b) Only one switch $S'_3$ or $S'_4$ is ON.

the diode pair $D_1 - D_{S_2}$ or $D_2 - D_{S_1}$. Depending on whether $S'_3$ or $S'_4$ is turned ON one of the diode pairs conducts and charges both capacitors $C_1$ and $C_2$. Thus, each pair carries the total load current with each diode carrying half the output current.

### 3.5.1 Duty ratio for the switches $S'_3$ and $S'_4$

The switches $S'_3$ and $S'_4$ are operated at duty ratios greater than 0.5 to ensure overlap and allow the inductor $L'_o$ to store energy. To operate in the boost-derived mode, the minimum duty ratio for the switches is determined for the worst case condition which occurs at maximum battery voltage when the output voltage at the DC bus is at the lower limit of the specified voltage range $V_{S_{min}}$. The minimum duty ratio is calculated by the expression,

$$D_{min} = 1 - \frac{V_{S_{min}}}{2V_S} \tag{3.11}$$

The maximum possible duty ratio of the secondary switches is now determined when the battery voltage is at its minimum allowable value.

$$D_{max} = \frac{V_S - V'_{batt\,min}}{V_S} \tag{3.12}$$

The minimum and maximum values of the duty ratios are plotted in Fig. 3-2.

### 3.5.2 Minimum value of Inductor $L'_o$

The lower limit value of the inductor, $L'_{o_{min}}$, is computed at the boundary of discontinuous and continuous inductor current for a minimum load, $I_{bus_{min}}$, and maximum

battery voltage. It is expressed as,

$$L'_{o_{min}} = \frac{2.5 \cdot V_S}{f_s \cdot I_{bus_{min}}} \cdot (2D_L - 1) \cdot D_L'^2 \quad \text{pu} \tag{3.13}$$

where the duty ratio $D_L$ is defined under boundary conditions at a minimum load of 0.1 pu at the bus, and $D'_L = 1 - D_L$. $D_L$ is derived from the expression for the minimum inductor current under boundary conditions which is given by,

$$I'_{L_{boundary}} = \frac{V_S D'_L}{2 \cdot f_s \cdot L'_{o_{min}}} \cdot (2D_L - 1) \quad \text{pu.} \tag{3.14}$$

Fig. 3-3 shows the minimum required value of the inductor in the backup mode for different specified voltage ranges at the DC bus.

### 3.5.3 Maximum voltage across switches $S'_3$ and $S'_4$

The first step in choosing the appropriate MOSFET is to determine the maximum reverse voltage across it. The maximum voltage stress across the secondary side switches, Fig. 3-6, $S'_3$ and $S'_4$ occurs when the one of the switches in ON and is given by,

$$V'_{S_{3max}} = V'_{S_{4max}} = V_{S_{max}} \quad \text{pu.} \tag{3.15}$$

### 3.5.4 Current through switches $S'_3$ and $S'_4$

Once the voltage rating for the switches is determined the suitable current rating must be calculated. The rms current through the switches $S'_3$ and $S'_4$, shown in Fig. 3-11, is given by,

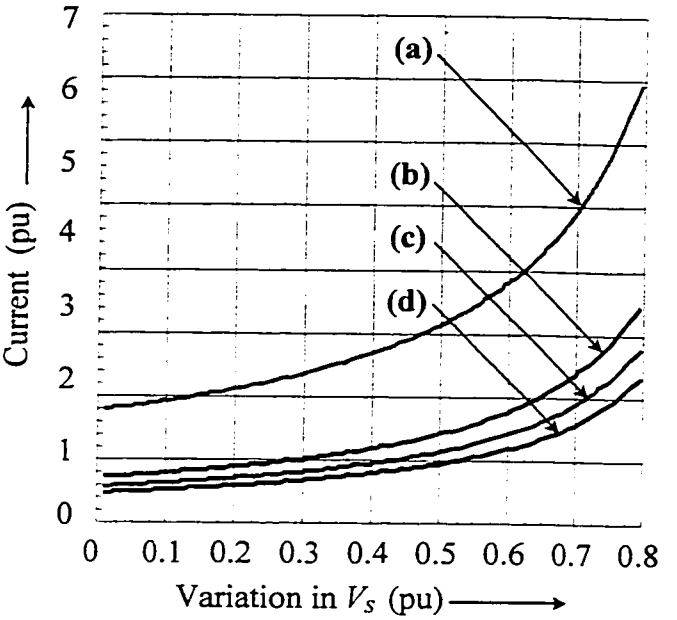



**Fig. 3-11 Rms current through the switches $S'_3$ and $S'_4$.**
(a) Backup mode, $P_{bus}$ = 1.0 pu. (b) Forward mode, $P_{batt}$ = 0.5 pu. (c) Forward mode, $P_{batt}$ = 0.4 pu. (d) Forward mode, $P_{batt}$ = 0.33 pu.

$$I'_{S_{3rms}} = I'_{S_{4rms}} = \frac{\sqrt{3}}{6}\sqrt{\left(\frac{3 \cdot {I_{bus_{max}}}^2}{{D'_{max}}^2} + \Delta' i^2\right) \cdot (3 - 2D_{max})} \quad \text{pu} \tag{3.16}$$

where, $\Delta' i$ is the ripple in the inductor current when reflected to the primary of the ideal and $D'_{max} = 1 - D_{max}$.

### 3.5.5 Maximum voltage across switches $S_1$ and $S_2$

The body diodes of $S_1$ and $S_2$ provide rectification on the primary side of the bi-directional converter in the backup mode. The maximum voltage across $D_{S_1}$ and $D_{S_2}$ is shown in Fig. 3-4 and is be expressed by the equation,

$$V_{S_{1max}} = V_{S_{2max}} = V_{S_{max}} \quad \text{pu} \tag{3.17}$$

### 3.5.6 Current through switches $S_1$ and $S_2$

In the backup mode the body diodes of $S_1$ and $S_2$ must have suitable current ratings to carry the current powering the loads at the DC bus. The average current rating required for these body diodes for maximum load current at the DC bus is given by,

$$I_{D_{S1avg}} = I_{D_{S2avg}} = \frac{I_{bus_{max}}}{2} \quad \text{pu.} \tag{3.18}$$

The average current through the switches is shown as a function the specified variation in the DC bus voltage in Fig. 3-12.

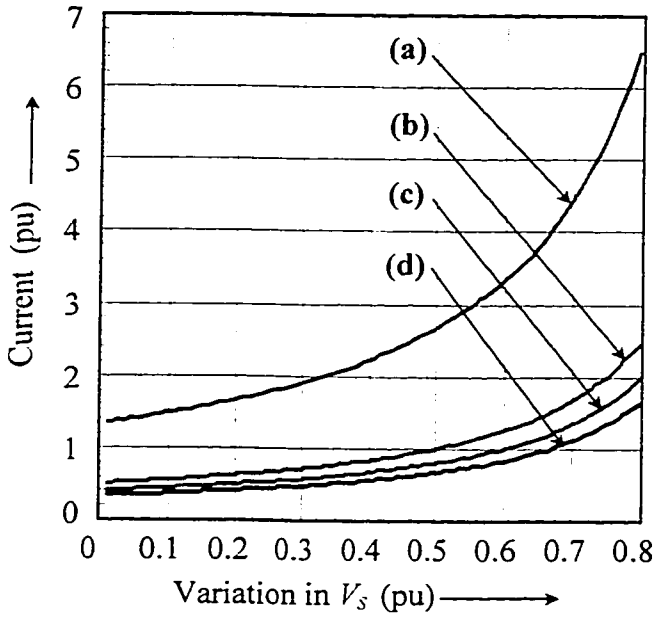



**Fig. 3-12 Average current through the switches $S_1$ and $S_2$.**
(a) Forward mode, $P_{batt}$ = 0.5 pu. (b) Forward mode, $P_{batt}$ = 0.5 pu. (b) Forward mode, $P_{batt}$ = 0.4 pu. (c) Forward mode, $P_{batt}$ = 0.33 pu. (d) Backup mode, $P_{bus}$ = 1.0 pu.

### 3.5.7 Balancing winding $N_{p_1}$ and catching diodes $D_1$ and $D_2$

The balancing winding, $N_{p1}$, and the diodes $D_1$ and $D_2$ enable simultaneous and equal charging of the capacitors $C_1$ and $C_2$, during intervals $t_1$-$t_2$ and $t_3$-$t_4$, as explained in section of the thesis. As the balancing winding carries the same current as the transformer primary winding, they are both wound using wires of equal gauge.

The diodes $D_1$ and $D_2$ are selected according to the maximum reverse voltage across them and the average current flowing through them while charging $C_1$ and $C_2$. Their voltage and current ratings are identical to those for the body diodes of the switches $S_1$ and $S_2$, Fig. 3-4 and Fig. 3-12, due to presence of identical windings $N_p$ and $N_{p1}$.

### 3.5.8 Capacitors $C_1$ and $C_2$

The capacitors $C_1$ and $C_2$ are selected according to the desired output ripple at the dc bus. They must also be large enough to hold the voltage at the bus when the switches $S'_3$ and $S'_4$ overlap, during intervals $t_0$-$t_1$ and $t_2$-$t_3$, under the worst possible case of minimum battery supply voltage and full load.

## 3.6 Experimental Verification of the Steady State Analysis

The performance curves from the design oriented analysis are used in chapter 5 to design a bi-directional converter with specified operating conditions. Experimental results are obtained from the actual implementation of that design. These results are presented in this section to verify the steady state analysis. The design specifications and component details of the experimental setup are provided in chapter 5 with the design

procedure. The waveforms and values presented in this section are not referred to the primary side of the transformer.

### 3.6.1 Experimental waveforms for the forward mode

The experimental results for the forward mode are obtained for the following operating conditions:

Input DC bus voltage, $V_S$ =360 V

Converter operating frequency, $f_s$ = 100 kHz

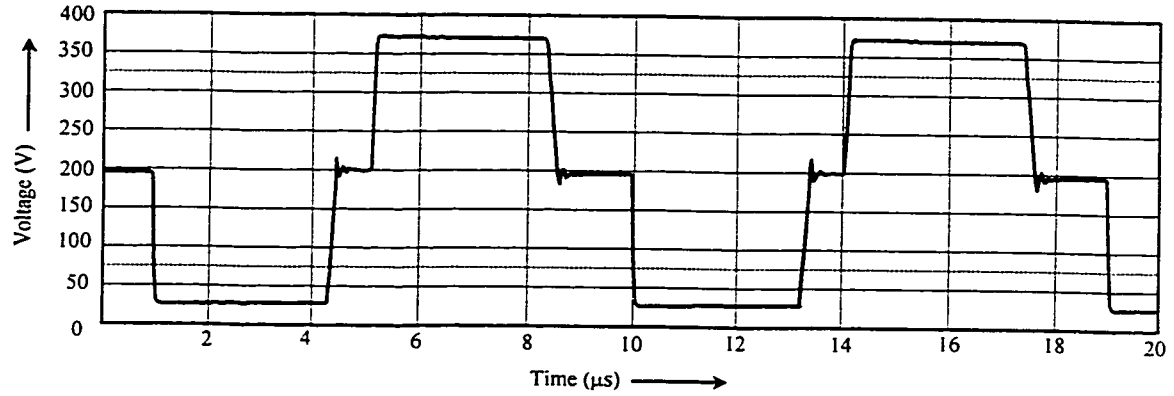
Power at the battery end, $P_{batt}$ = 85 W

Nominal battery voltage, $V_{batt}$ = 48 V

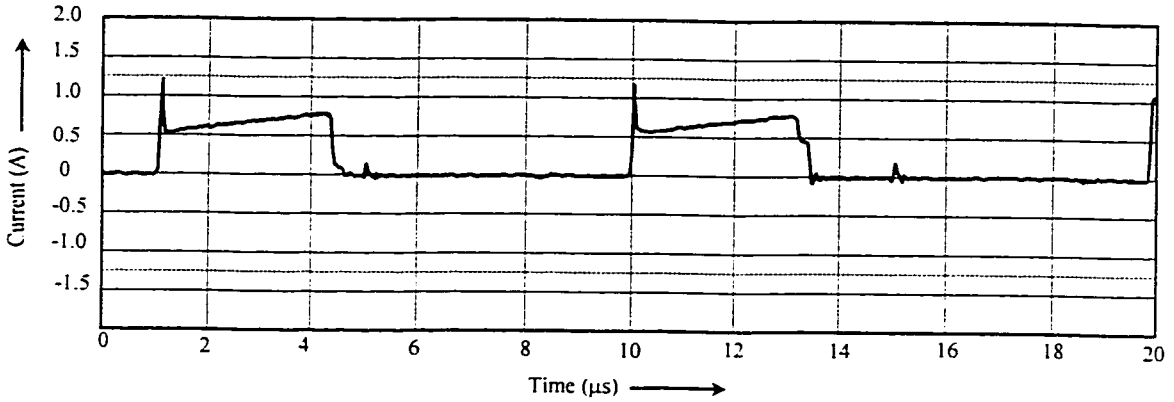
These values are well within the operating limits specified for the converter design. The converter is operating at 75% load at the output.

The steady state current and voltage waveforms for the primary side switches $S_1$ and $S_2$ are shown in Fig. 3-13(a) and (b). Fig. 3-13(c) shows the current in the transformer primary winding which is seen to be symmetrical for each switch, implying that there is no flux imbalance in the transformer core.

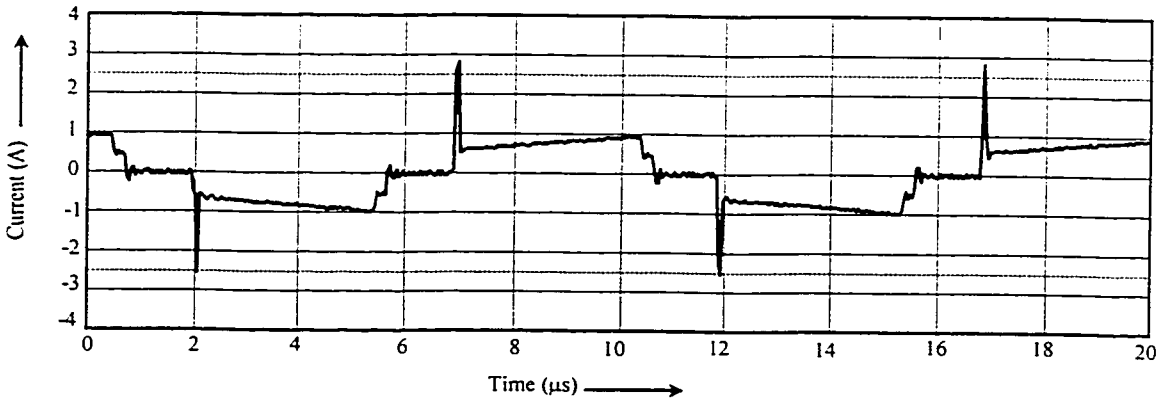
The current and voltage stresses for the secondary side switches $S_3$ and $S_4$ are shown in Fig. 3-14. Fig. 3-14(c) shows the continuous battery charging current of 1.55 A through the output inductor. The ripple in the inductor current is only about 0.2 A. The battery is being charged to 54.5 V, Fig. 3-15. It is seen that the battery voltage has very small ripple content, as is required.




(a)



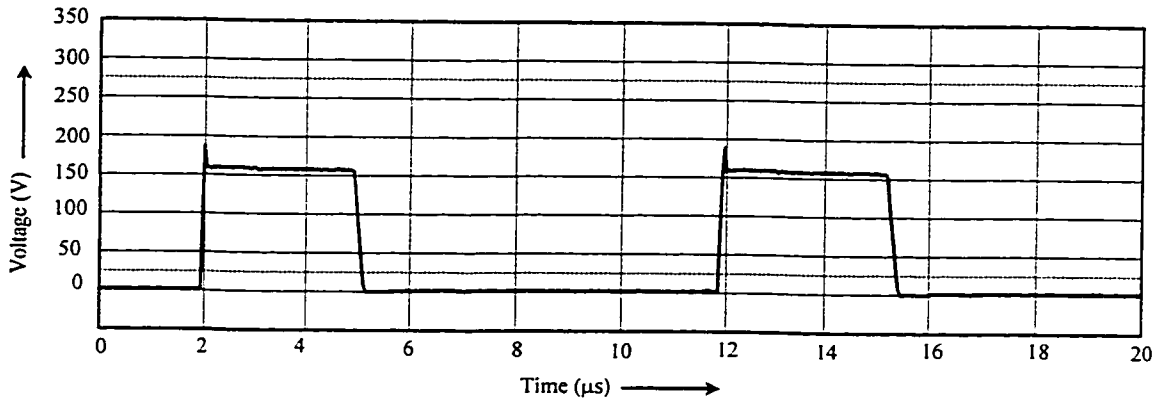

(b)



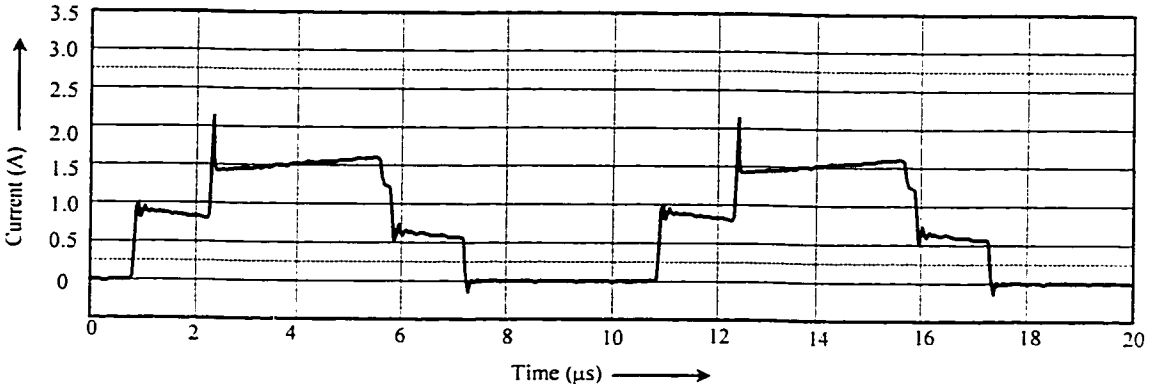

(c)

**Fig. 3-13 Experimental results for the forward mode in steady state.**

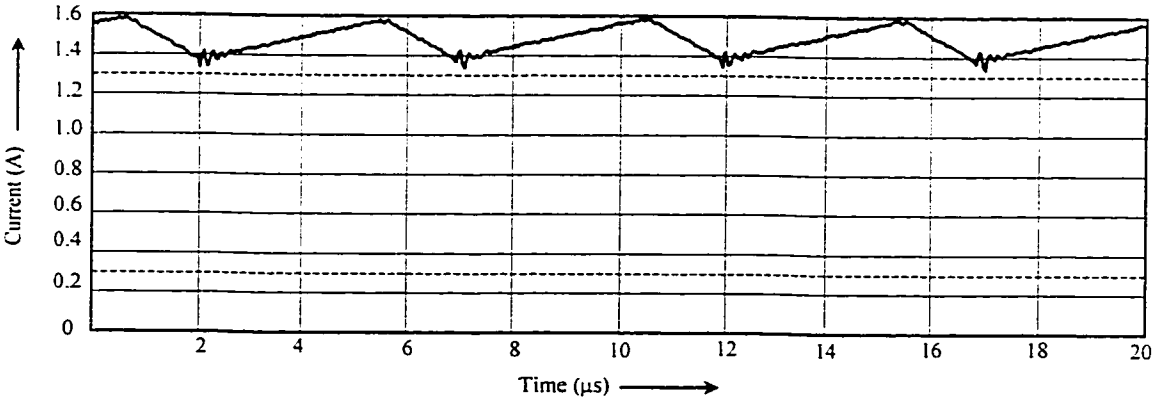
(a) Voltage across primary side switch $S_1$ or $S_2$. (b) Current through primary side switch $S_1$ or $S_2$. (c) Total current in primary winding of transformer. (Input voltage = 360 V, output power = 85 W, output voltage = 54.5 V, switching frequency = 100 kHz.)




(a)




(b)




(c)

**Fig. 3-14 Experimental results for the forward mode in steady state.**

(a) Voltage across secondary side switch body diodes $D'_{S_3}$ or $D'_{S_4}$. (b) Current through secondary side switch body diode $D'_{S_3}$ or $D'_{S_4}$. (c) Current through the inductor $L_o$. (Input voltage = 360 V, output power = 85 W, output voltage = 54.5 V, switching frequency = 100 kHz.)

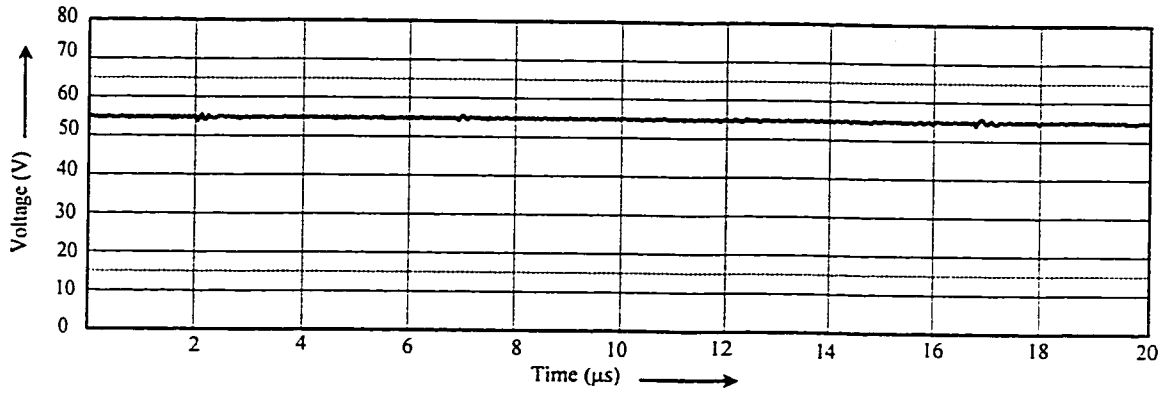



**Fig. 3-15 Experimental results for the forward mode in steady state.**
Voltage at the battery, $V_{batt}$. (Input voltage = 360 V, output power = 85 W, output voltage = 54.5 V, switching frequency = 100 kHz.)

Current spikes are observed in the experimental waveform of Fig. 3-14(c). These are attributed to the reverse recovery of the rectifying diodes. Use of diodes with softer reverse recovery, like Hexfreds, will reduce the current spikes. These diodes have a higher voltage drop but it will not greatly effect the efficiency of the converter because of the low currents flowing through them.

### 3.6.2 Experimental waveforms for the backup mode

Experimental results for the steady state operation of the converter setup described in chapter 5 in the backup mode verify the analytical expressions and the design curves of the backup mode. The results are obtained under the following operating conditions:

Battery voltage, $V_{batt} = 50$ V

Converter operating frequency, $f_s = 100$ kHz

Power delivered to the DC bus, $P_{bus} = 190$ W

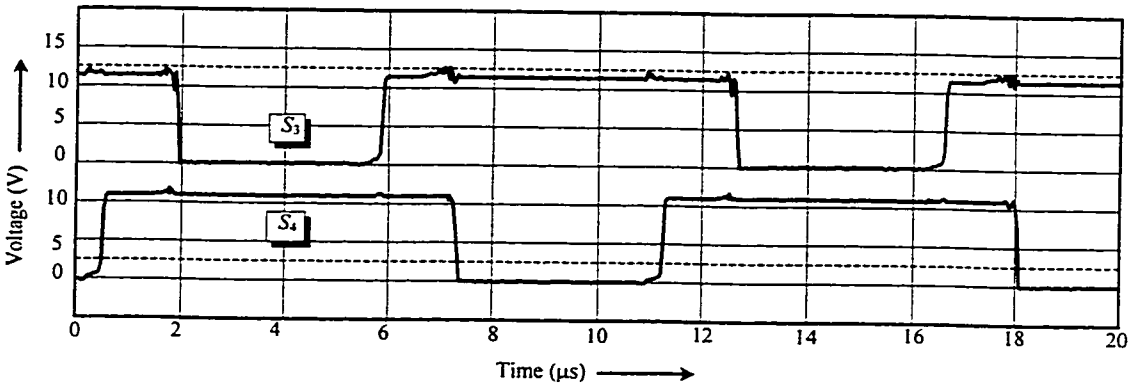
Nominal voltage at DC bus, $V_S = 323$ V

These values are well within the operating specifications for which the converter is designed. The battery is charged and provides load power at 75% of the rated output power. The voltage at the output (DC bus) must be within the specified range of 300 – 400 V to power the down stream converters and has been chosen at 323 V in the experimental setup.

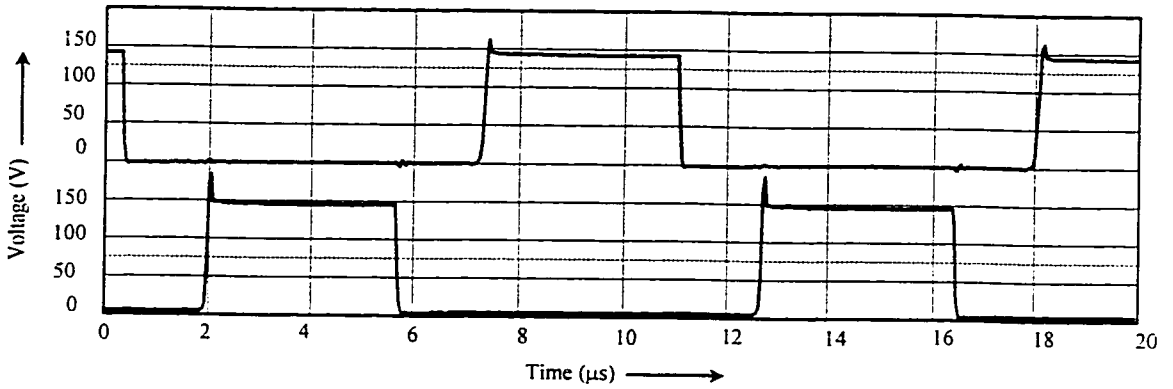
The gating pattern for the secondary side switches $S'_3$ and $S'_4$ is shown in Fig. 3-16(a). This clearly shows the overlap between the ON times of the two switches. The voltage and current stresses across the switches is shown in Fig. 3-16(b) and (c). Current sharing in switches when both of them are ON can be observed from Fig. 3-16(c).

The voltage across the primary side switches and the current through their body diodes is shown in Fig. 3-17(a) and (b). Current in the transformer primary winding is shown in Fig. 3-17(c) and is symmetrical for both the positive and negative halves indicating that the core is not saturated.

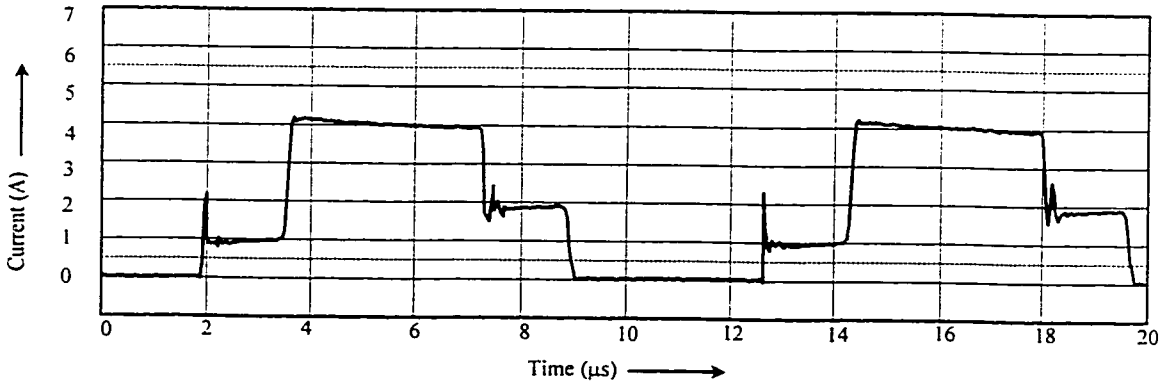
The current through the inductor $L'_o$ in series with the battery is continuous and has an average value of 6 A, Fig. 3-18(a). The output voltage of the converter at the DC bus, Fig. 3-18(b), is 323 V and is seen to have negligible ripple content.




(a)




(b)




(c)

**Fig. 3-16 Experimental results for the backup mode in steady state.**

(a) Gating pattern for the secondary side switches $S'_3$ and $S'_4$. (a) Voltage across $S'_3$ or $S'_4$. (c) Current through $S'_3$ or $S'_4$. (Battery voltage = 50 V, output power = 190 W, output (dc bus) voltage = 323 V, switching frequency = 100 kHz.)

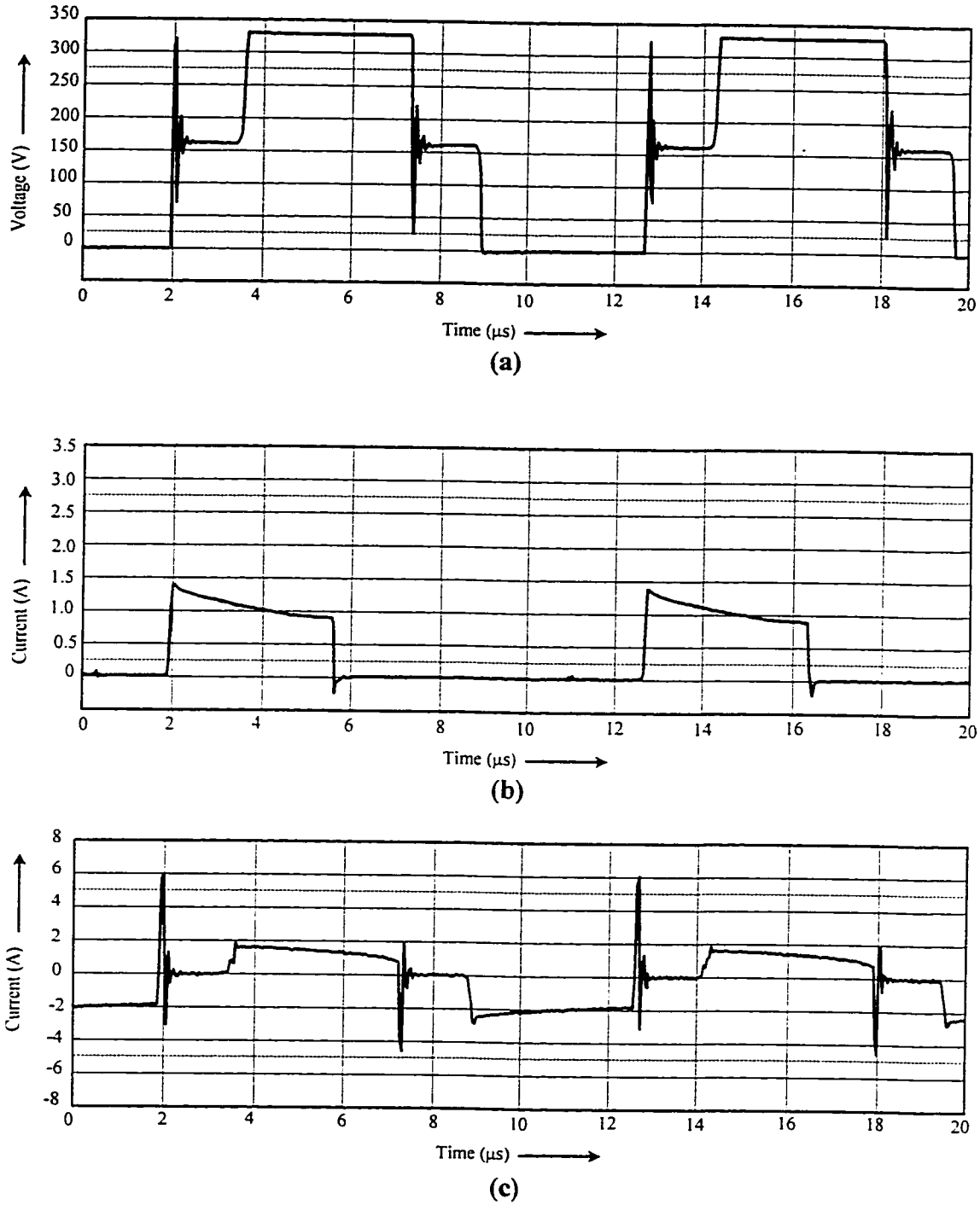



**Fig. 3-17 Experimental results for the backup mode in steady state.**

(a) Voltage across primary side switch body diodes $D_{S_1}$ and $D_{S_2}$ and catching diodes $D_1$ and $D_2$. (b) Current through primary side switch body diodes $D_{S_1}$ and $D_{S_2}$ and catching diodes $D_1$ and $D_2$. (c) Current in the transformer primary winding. (Battery voltage = 50 V, output power = 190 W, output (dc bus) voltage = 323 V, switching frequency = 100 kHz.)

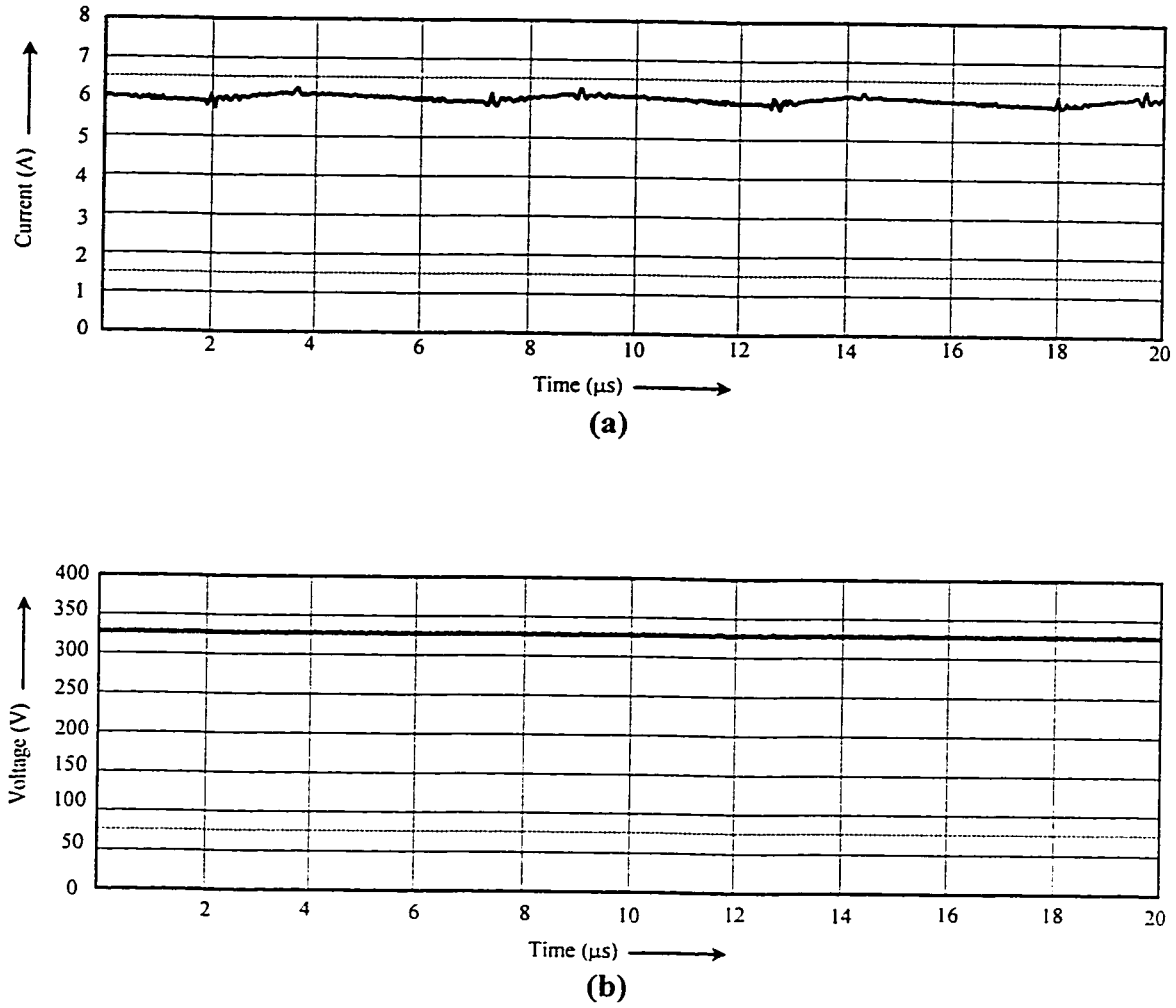



**Fig. 3-18 Experimental results for the backup mode in steady state.**
(a) Current through the inductor, $i_{L_o}$. (b) Voltage at the DC bus, $V_S$. (Battery voltage = 50 V, output power = 190 W, output (dc bus) voltage = 323 V, switching frequency = 100 kHz.)

Reverse recovery spikes in the transformer current in Fig. 3-17(c) are observed due to diode recovery. Use of Hexfreds can reduce this problem to a great extent as explained in section 3.6.1.

## 3.7 STEADY STATE EFFICIENCY EVALUATION

The efficiency of the bi-directional dc-dc converter in steady state operation in both modes is obtained from the experimental setup to evaluate converter performance in steady state.

Converter efficiency in the forward mode is obtained from the experimental setup powered from a 350 V DC bus charging the battery at 54.1 V. Fig. 3-19 shows the steady state forward mode efficiency as a function of the load (battery charging current) for the specified battery voltage. The full load corresponds to the condition of the battery drawing 1.8 A charging current. The efficiency is seen to reach a peak of 86.6 % and decreases as the battery draws less charging current.

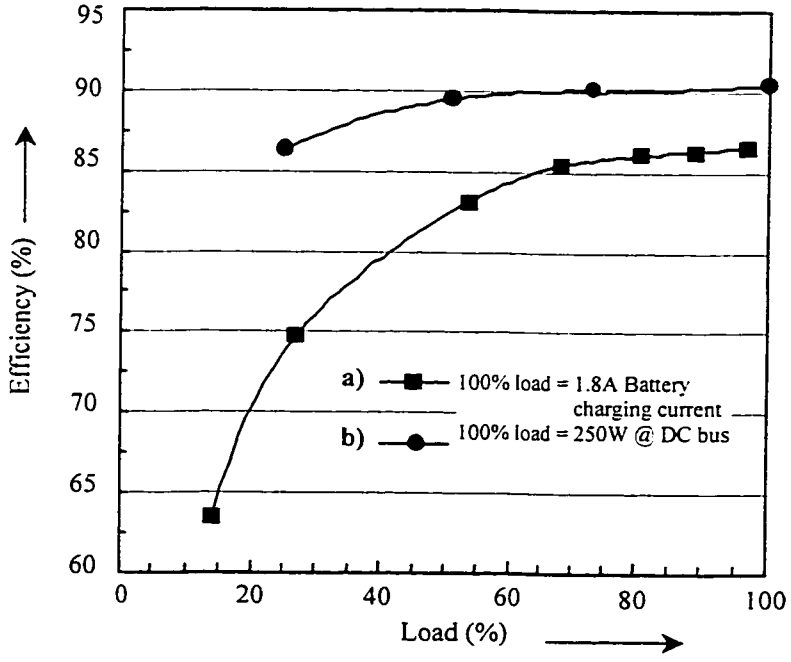



**Fig. 3-19 Converter efficiency in forward and backup modes.**
a) Forward mode. Input voltage = 350 V, battery voltage = 54.1 V. b) Backup mode. Battery voltage = 50 V, DC bus voltage = 325 V.

Fig. 3-19 also shows the steady state efficiency of the practical implementation of the converter in the backup mode. The efficiency for a battery voltage of 50 V powering the DC bus at 325 V is plotted as a function of the load at the DC bus. The full load at the DC bus occurs at 250 W. An peak efficiency of 90.5 % is obtained for this mode.

These experimental results confirm a high efficiency for the proposed topology in both its operating modes.

## 3.8 CONCLUSIONS

The steady state analysis provides the equations that determine circuit parameters and the component ratings of the proposed converter. Normalized design curves are generated from these mathematical expressions to enable converter design over a wide range of operating conditions. Experimental results are obtained for both the forward and backup modes from the laboratory setup of the bi-directional converter described in chapter 5. These results validate the theoretical design expressions and design curves for converter operation in steady state. The prototype of the converter shows high efficiency in both operating modes.

# CHAPTER 4

# SMALL SIGNAL ANALYSIS

## 4.1 INTRODUCTION

The component ratings and the circuit parameters are determined by the steady state analysis presented in the previous chapter. The output voltage of the converter is regulated despite the variations in output load and input voltage, by adjusting the duty ratio of the switching devices. This dynamic response of the converter is achieved by implementing a feedback control system, Fig. 4-1, which provides the desired regulation. A compensated error amplifier is used which compares the output voltage against its nominal operating value and modulates the pulse width of the switching device in the converter.

To design the error amplifier, mathematical expressions that describe the dynamic behavior of the power stage, Fig. 4-1 must be derived. This dynamic behavior can be

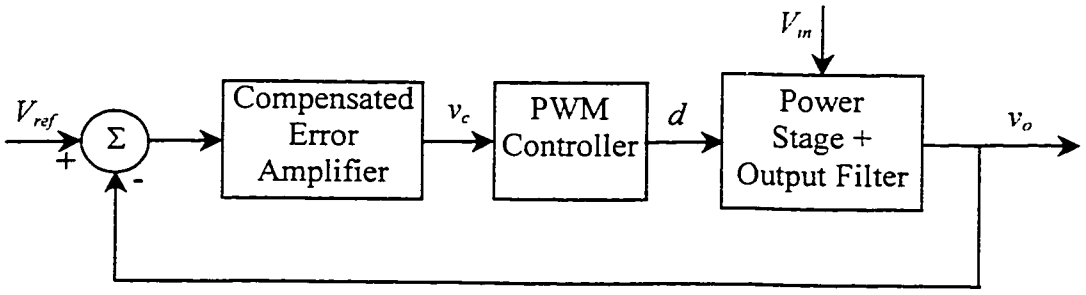



**Fig. 4-1 Block diagram representation of a converter with feedback control.**

described by small-signal transfer functions, expressed in terms of ac perturbations around a steady-state dc operating point of the converter. These transfer functions are used to design the error amplifier in the feedback loop, which provides the overall system with the desired dynamic response. The transfer functions provide an insight into the parameters governing the converter behavior and are suitably controlled in order to design a converter that meets the requirements of efficiency, output regulation, output ripple, stability etc.

This chapter outlines the small-signal ac analysis for both modes of converter operation under current mode control and provides transfer functions describing converter characteristics thereby helping to design and evaluate the compensator in the control loop. Open loop expressions for the forward and backup modes are derived for gain and audio susceptibility, using the state-space approach outlined in [37]. The analysis is validated by the results from the design example described in chapter 5.

## 4.2 STATE-SPACE APPROACH

Switching power supplies are non-linear and discontinuous by nature therefore, some linearizing technique must be used in order to analyze such converters using the simple techniques of linear circuit analysis and synthesis. State-space averaging [37-39] is one such technique that results in a linear model of the power stage including the output filter for small ac signals, linearized around a steady-state operating point. State-space averaging by itself, approximates the switched system to a continuous but non-linear one and the process of linearization allows the resulting non-linear system to be approximated to linear system. The linearizing process does involve some compromise in

accuracy, but is adequately correct for normal design purposes. Bode plots are used to determine the frequency response of the linearized converter to small signal variations in its operating parameters.

State-space averaging provides mathematical expressions describing the small-signal line-to-output and control-to-output transfer properties of the converter. The technique presented by [37] for current-programmed converters is an extension of the technique presented in [38] and has been used to derive the key transfer functions for the converter in both operating modes. Using this technique, the current-programmed converter is expressed as a function of the states, input voltage and the control signal rather than the duty ratio. The inner current loop is absorbed in the forward path of the converter leaving only one simple voltage feedback loop evident, which is also easier to compensate.

The following text presents the basic procedure and some key equations for the small-signal state space analysis of each mode of converter operation. The detailed mathematical procedure for the analysis has been derived in appendix.

## 4.3 SIMPLIFYING ASSUMPTIONS

The small signal ac analysis of the converter is performed with some basic assumptions to aid the procedure. The following assumptions have been made for the analysis using state-space averaging:

- The semiconductor devices are ideal and have instantaneous switching from one state to the other, i.e. offer either zero or infinite resistance to currents.
- The ac perturbations of the variables about their respective dc operating points are

small enough that the product of two ac quantities is negligible.

- The ripple in the output voltage is negligible.
- The corner frequency of the output filter is assumed to be atleast a decade or two below half the switching frequency of the converter.
- The parasitic elements of the inductor and capacitor have been considered, but are negligible when compared to the equivalent load resistance.

## 4.4 SMALL-SIGNAL ANALYSIS OF THE FORWARD MODE

For the small-signal ac analysis of the forward mode, the circuit parameters are reflected to the secondary side according to the appropriate transformer turns ratio. Converter operation is repetitive over half a switching interval, thus the two equivalent circuits in Fig. 4-2 are representative of the two distinct converter states in half the switching period. One circuit state, Fig. 4-2(a) corresponds to the condition when either $S_1$ or $S_2$ is ON for a time duration expressed as $d_{ss}T_{ss}$ where

$$\left.\begin{aligned} d_{ss} &= 2 \cdot d_{fw} \\ T_{ss} &= \frac{T_s}{2} \end{aligned}\right\} \tag{4.1}$$

The other circuit state, Fig. 4-2(b), represents to the duration $(1\text{-}d_{ss})T_{ss}$, when both the primary side switches are in the OFF state.

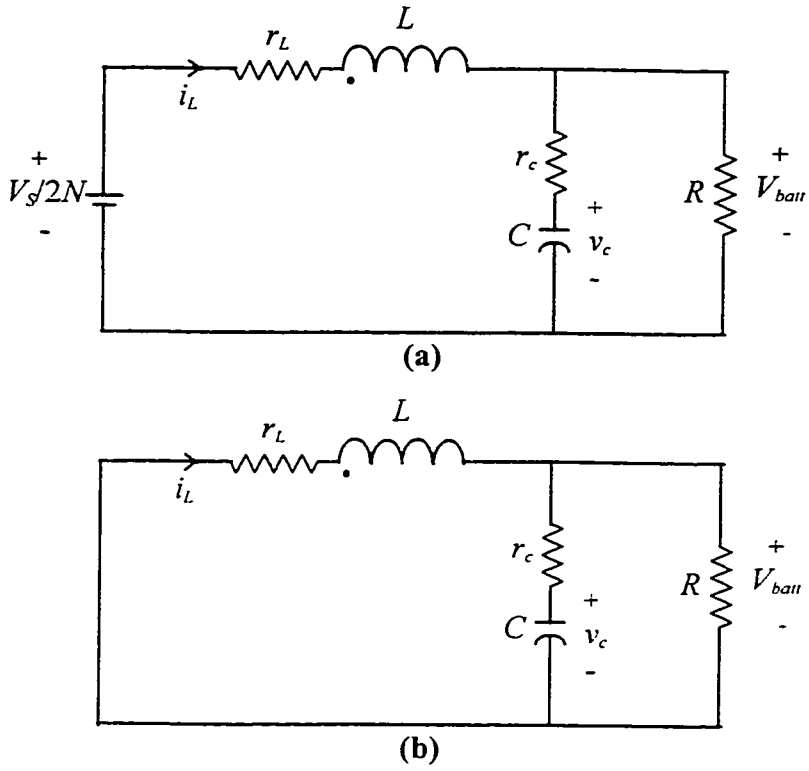



**Fig. 4-2 Equivalent circuit for the small-signal analysis of the forward mode.**
(a) Either primary side switch $S_1$ or $S_2$ is ON for time $d_{ss}T_{ss}$. (b) None of the primary side switches is ON for time $(1-d_{ss})T_{ss}$.

### 4.4.1 State-space equations for the circuit states

The state-space equations for the equivalent circuit state in Fig. 4-2(a) when one of the primary switches is ON are expressed by

$$\left.\begin{aligned} \dot{x} &= A_1 x + B_1 v_S \\ v_{batt_1} &= C_1^T x \end{aligned}\right\} \qquad (4.2)$$

where, " x " is the state variable vector consisting of the inductor current and the capacitor voltage as state variables. (4.2) can be written as

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_c + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{2LN} \\ 0 \end{bmatrix} \cdot v_S$$

$$v_{batt_1} = \begin{bmatrix} r_c & 1 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{4.3}$$

The state-space equations for the circuit state depicted in Fig. 4-2(b), representing the time interval when neither of the primary switches is ON are

$$\left.\begin{aligned} \dot{x} &= A_2 x + B_2 v_S \\ v_{batt_2} &= C_2^T x \end{aligned}\right\} \tag{4.4}$$

which are re-written as

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_c + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \cdot v_S$$

$$v_{batt_2} = \begin{bmatrix} r_c & 1 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{4.5}$$

### 4.4.2 Linearized averaged state-space equation

The state-space equations for each circuit state, (4.3) and (4.5), are averaged over the equivalent switching time period $T_{ss}$ for $d_{ss}$ and (1- $d_{ss}$), respectively. The matrices of the averaged equations maybe nonlinear with respect to the duty ratio $d_{ss}$. Thus, the averaged equations are perturbed around the dc operating point by adding small-signal ac perturbations to the circuit variables,

$$d_{ss} = D_{ss} + \hat{d}_{ss} \qquad \mathrm{x} = \mathrm{X} + \hat{\mathrm{x}} \qquad v_S = V_S + \hat{v}_S \tag{4.6}$$

where the small-signal ac perturbations are denoted by the symbol " ^ " on the variables and the steady state values are denoted in upper case letters. An approximation is made that the perturbations are negligible when compared to the steady-state values:

$$\frac{\hat{d}_{ss}}{D_{ss}} << 1 \qquad \frac{\hat{\mathrm{x}}}{\mathrm{X}} << 1 \qquad \frac{\hat{v}_S}{V_S} << 1 . \tag{4.7}$$

All the nonlinear terms, second order terms, in the perturbed averaged state-space equations are neglected resulting in a linear set of equations. The resulting equations contain both the steady-state (dc) and the dynamic (ac) parts from which the only the dynamic parts are retained, [Appendix A]. This provides the final linearized ac small-signal model,

$$\dot{\hat{\mathrm{x}}} = \mathrm{A}\hat{\mathrm{x}} + \mathrm{B}\hat{v}_S + \left[(\mathrm{A}_1 - \mathrm{A}_2)\mathrm{X} + (\mathrm{B}_1 - \mathrm{B}_2)V_S\right]\hat{d}_{ss} \tag{4.8}$$

which is expressed in the s-domain (using Laplace transforms) to determine the relevant transfer functions describing the converter in the forward mode operation. Thus (4.8) is expressed as

$$\begin{bmatrix} s\hat{i}_L(s) \\ s\hat{v}_c(s) \end{bmatrix} = \begin{bmatrix} -\dfrac{r_c + r_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_L(s) \\ \hat{v}_c(s) \end{bmatrix} + \begin{bmatrix} \dfrac{d_{ss}}{2LN} \\ 0 \end{bmatrix} \cdot \hat{v}_S(s) + \begin{bmatrix} \dfrac{V_S}{2LN} \\ 0 \end{bmatrix} \cdot \hat{d}_{ss}(s) \tag{4.9}$$

### 4.4.3 Control constraint

The control constraint expresses the control signal as a function of the programmed inductor current. As suggested [37] the variations in the programmed current can be approximated to follow those in the control signal exactly, thereby equating the two. However, a second more accurate relationship between the two, from the geometry of Fig. 4-3, gives better description of the effect of the current loop. This second technique has been used in the following analysis and the constraint is expressed as,

$$i_L + \frac{1}{2} m_1 d_{ss} T_{ss} = v_{control} - m_c d_{ss} T_{ss} \qquad (4.10)$$

where $m_1$ is the rising slope of the inductor current, $m_c$ is the slope of the stabilizing ramp and $v_{control}$ the control signal.

Small-signal perturbations are applied to (4.10) and only the linear terms of the dynamic (ac) part are retained. Substitution of appropriate variables will express the

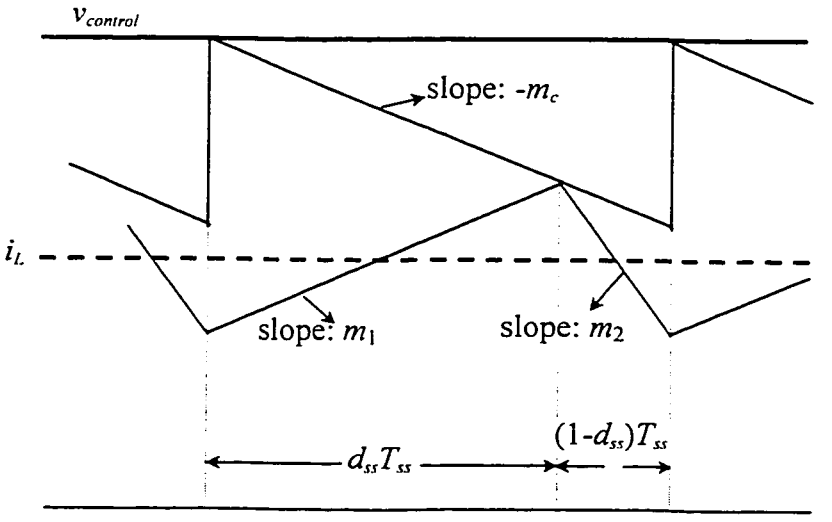



**Fig. 4-3 Waveforms showing relationship between programmed current and control signal in forward mode.**

variation in the programmed inductor current as a function of the variations in the control signal, the state variables, the input voltage and the duty ratio [Appendix A]. Mathematical manipulation provides the variation in the duty ratio is expressed as a function of the variation of the other parameters.

The expression for the variation in the duty ratio is substituted back in the linearized averaged state-space representation of (4.8). The programmed inductor current is now a "driving term" rather than an unknown state and duty ratio looses its status as an independent input. This provides the final current-programmed state equation by expressing the linearized averaged state-space equation as a function of the state variables $\hat{x}(s)$, the input voltage $\hat{v}_S(s)$ and the control signal $\hat{v}_{control}(s)$ as

$$s\hat{x}(s) = A'\hat{x}(s) + B'\hat{v}_S(s) + C'\hat{v}_{control}(s) \tag{4.11}$$

where the matrices A′, B′ and C′ are defined in Appendix A with the detailed derivation of the small signal analysis.

### 4.4.4 Control-to-output transfer function

The control-to-output transfer is one of the key analytical expressions that characterize converter operation. The frequency plot of this transfer function determines the restrictions and requirements on the design of the compensator.

For a constant input voltage, $\hat{v}_S(s) = 0$, the current-programmed state equation (4.11) is reduced to a function of $\hat{x}(s)$ and $\hat{v}_{control}(s)$. This allows $\hat{x}(s)$ to be expressed as a function of $\hat{v}_{control}(s)$ by matrix manipulation,

$$\hat{x}(s) = [sI - A']^{-1} C'\hat{v}_{control}(s) \tag{4.12}$$

where I is the identity matrix.

The small-signal expression for output voltage is given by

$$\hat{v}_{batt}(s) = C\hat{x}(s) \tag{4.13}$$

Substituting for $\hat{x}(s)$ from (4.12) in the above expression gives the small-signal control-to-output transfer function for the forward mode,

$$\frac{\hat{v}_{batt}(s)}{\hat{v}_{control}(s)} = G_{vf} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_L/C_1} + \frac{s^2}{\omega_L\omega_c/C_1}} \tag{4.14}$$

The control-to-output transfer function contains not only the frequency of the dominant pole at the load corner frequency of $\omega_L$, but also the zero frequency at $\omega_z$ and crossover frequency for the inner current loop at $\omega_c$. The mathematical expressions defining these corner frequencies and the open loop gain $G_{vf}$ are derived in the appendix.

### 4.4.5 Line-to-output transfer function

The converter also is subject to perturbations in the input voltage that effect the output voltage. The system response to small variations in the input voltage is expressed as a transfer function describing the relation between the output and input voltage of the converter. The process for deriving this transfer function is similar to that for the control-to-output transfer function. This line-to-output transfer function, also called the audio susceptibility, for the forward mode is expressed as,

$$\frac{\hat{v}_{batt}(s)}{\hat{v}_s(s)} = A_{g_{vf}} \cdot \frac{1+\dfrac{s}{\omega_z}}{1+\dfrac{s}{\omega_L/C_1}+\dfrac{s^2}{\omega_L\omega_c/C_1}}. \tag{4.15}$$

where the corner frequencies are identical to those in the control-to-output transfer function and defined in the appendix.

## 4.5 SMALL-SIGNAL ANALYSIS OF THE BACKUP MODE

The procedure for the small-signal analysis of the backup mode of the bi-directional converter is similar to that of the forward mode. The converter has four states over one switching period defined by the intervals $t_0 - t_4$ in section 2.4.3. Closer observation reveals only two distinct states, as converter operation is repetitive over half a switching time interval. The equivalent circuits, shown in Fig. 4-4 represent the two states of the converter. All parameters are reflected to the primary of the isolation transformer by the appropriate transformation ratio $N'$, which is the ratio of the turns in the secondary to those in the primary winding. The detailed analysis with the nomenclature definition is provided in the appendix.

Fig. 4-4(a) represents the state when both $S_3$ and $S_4$ are closed for a time interval $d_{cfsss}T_{ss}$, where

$$\left.\begin{aligned} d_{cfss} &= 2D-1 \\ T_{ss} &= \frac{T_s}{2} \end{aligned}\right\} \tag{4.16}$$

$D$ being the actual duty ratio of the secondary side switches and $T_s$ the switching time

period of the converter in the backup mode. When only one of the secondary side switches in the ON state, the converter operation can be described by the equivalent circuit of Fig. 4-4(b) for a time interval $(1\text{-}d_{cfss})T_{ss}$. In the equivalent circuit, $C_e$ is the equivalent capacitance of the capacitors $C_1$ and $C_2$ and $r_e$ is the equivalent esr of this capacitance $C_e$.

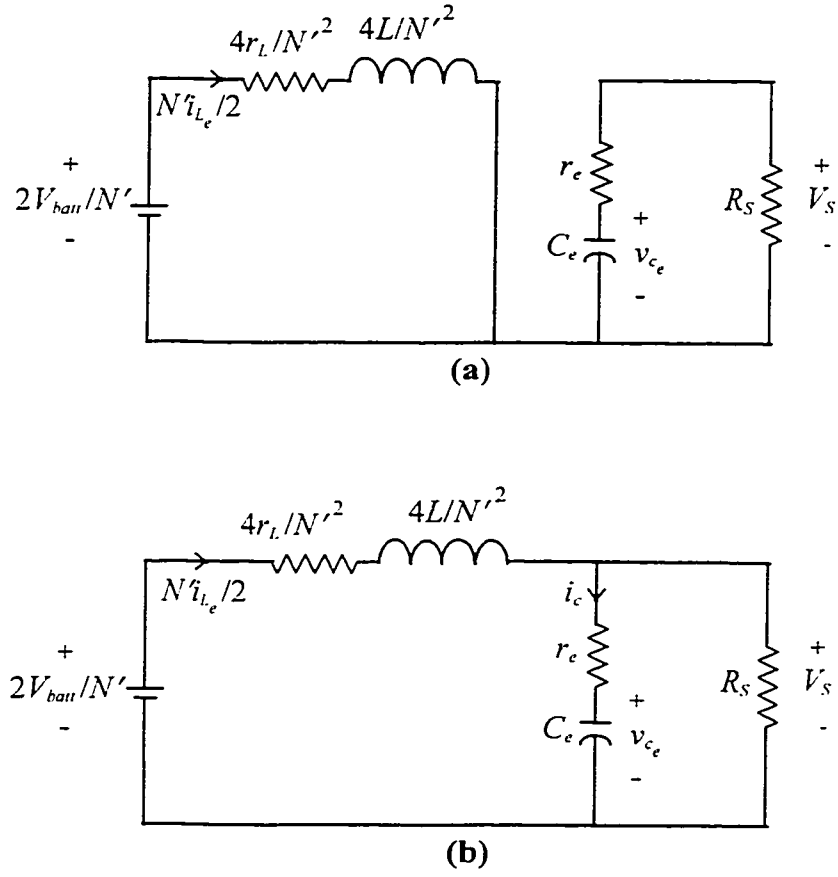



**Fig. 4-4 Equivalent circuit for the small-signal analysis of the backup mode.**
(a) Both secondary side switches $S_3$ and $S_4$ are ON for time $d_{cfss}T_{ss}$. (b) One of the secondary side switches is ON for time $(1\text{-}d_{cfss})T_{ss}$.

### 4.5.1 State-space equations for the circuit states

The state-space equations for the two circuit states are defined in a way similar to that in the forward mode, expressed by,

$$\left.\begin{array}{lll} \text{For interval } d_{cf_{ss}} T_{ss} & & \text{For interval } (1 - d_{cf_{ss}}) T_{ss} \\ \dot{x} = a_1 x + b_1 v_{batt} & & \dot{x} = a_2 x + b_2 v_{batt} \\ v_{batt_1} = c_1^T x, & \text{and} & v_{batt_2} = c_2^T x \end{array}\right\} \quad (4.17)$$

The inductor current and the capacitor voltage are once again chosen as the state variables.

The state-space equations for the interval $d_{cfss}T_{ss}$ when both switches are ON, represented by the circuit state of Fig. 4-4(a) are therefore written as,

$$\begin{bmatrix} \frac{di_{L_e}}{dt} \\ \frac{dv_{c_e}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{(R_S + r_e)C_e} \end{bmatrix} \cdot \begin{bmatrix} i_{L_e} \\ v_{c_e} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{batt} \quad (4.18)$$

$$v_{S_1} = \begin{bmatrix} 0 & \frac{R_S}{R_S + r_e} \end{bmatrix} \cdot \begin{bmatrix} i_{L_e} \\ v_{c_e} \end{bmatrix}$$

Similarly, the state-space equations for the equivalent circuit for the interval $(1\text{-}d_{cfss})T_{ss}$ when only one switch is ON can be written as,

$$\begin{bmatrix} \frac{di_{L_e}}{dt} \\ \frac{dv_{c_e}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\left(r_L + \frac{r_L r_e N'^2}{(R_S + r_e)4}\right) & -\frac{N'R_S}{2L(R_S + r_e)} \\ \frac{R_S N'}{2C_e(R_S + r_e)} & -\frac{1}{(R_S + r_e)C_e} \end{bmatrix} \cdot \begin{bmatrix} i_{L_e} \\ v_{c_e} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{batt} \qquad (4.19)$$

$$v_{S_1} = \begin{bmatrix} \frac{N'R_S r_e}{2(R_S + r_e)} & \frac{R_S}{(R_S + r_e)} \end{bmatrix} \cdot \begin{bmatrix} i_{L_e} \\ v_{c_e} \end{bmatrix}$$

### 4.5.2 Linearized averaged state-space equation

The state-space equations (4.18) and (4.19) describing each circuit state are averaged over the switching time period $T_{ss}$ for their respective time intervals of $d_{cfss}T_{ss}$ and $(1\text{-}d_{cfss})T_{ss}$. Small-signal ac perturbations are added to the DC quantities around the DC operating point as follows:

$$d_{cfss} = D_{cfss} + \hat{d}_{cfss} \qquad \mathrm{x} = \mathrm{X} + \hat{\mathrm{x}} \qquad v_{batt} = V_{batt} + \hat{v}_{batt} \qquad (4.20)$$

As in the forward mode analysis, the ac perturbations are denoted by the symbol " ^ " and the steady state DC quantities are denoted in upper case letters. The perturbations are considered negligible when compared to the DC quantities, so the non-linear second order terms in the perturbed averaged state-space equations are neglected, providing a linear set of equations containing both the steady-state (dc) and the dynamic (ac) parts. The ac part represents the final linearized ac small-signal model of the converter in the backup mode. This can be represented by as in the forward mode, with appropriate values for the matrices by,

$$\dot{\hat{\mathrm{x}}} = \mathrm{a}\hat{\mathrm{x}} + \mathrm{b}\hat{v}_{batt} + \left[(\mathrm{a}_1 - \mathrm{a}_2)\mathrm{X} + (\mathrm{b}_1 - \mathrm{b}_2)V_{batt}\right]\hat{d}_{cfss} \qquad (4.21)$$

The process of obtaining the linearized small-signal equations is given in detail in the appendix. The final Laplace form of (4.8) describing converter operation in the backup mode can be expressed as

$$\begin{bmatrix} s\hat{i}_{L_e}(s) \\ s\hat{v}_{c_e}(s) \end{bmatrix} = \begin{bmatrix} \frac{-r_e N'^2 d'_{cfss}}{4L} & \frac{-N'd'_{cfss}}{2L} \\ \frac{N'd'_{cfss}}{2C_e} & -\frac{1}{R_S C_e} \end{bmatrix} \begin{bmatrix} \hat{i}_{L_e}(s) \\ \hat{v}_{c_e}(s) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \hat{v}_{batt}(s) + \begin{bmatrix} \frac{V_S N'}{2L} \\ \frac{V_S}{R_S C_e d'_{cfss}} \end{bmatrix} \hat{d}_{cfss}(s) \tag{4.22}$$

### 4.5.3 Control Constraint

The relationship between the control signal and the programmed current is similar to that used in the analysis of the forward mode operation, section 4.4.3. Fig. 4-5 shows the programmed current with rising slope $m_a$, falling slope $m_b$ and the slope of the negative compensating ramp as $m_c$, being compared to the error signal $e$.

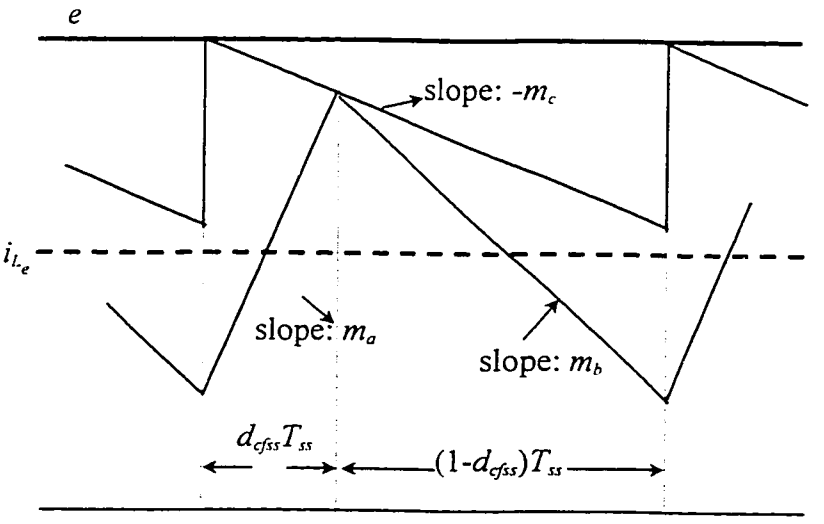



**Fig. 4-5 Waveforms showing relationship between programmed current and control signal in the backup mode.**

From the geometry of Fig. 4-5 the relationship between the programmed current and the control signal is expressed as,

$$i_{L_e} + \frac{1}{2} m_a d_{cfss} T_{ss} = e - m_c d_{cfss} T_{ss} \tag{4.23}$$

After perturbing and linearizing (4.23), the perturbation in the duty ratio is expressed as a function of the perturbed states, input voltage and output voltage. As in the analysis for converter operation in the forward mode, this information is incorporated with the linearized averaged state-space equations. The programmed current changes to a driving term and the duty ratio is not an independent input anymore. The final current-programmed state equation expressed as a function of the perturbations in the state variables $\hat{x}(s)$, the input battery voltage $\hat{v}_{batt}(s)$, and the control signal $\hat{e}(s)$ is,

$$s\hat{x}(s) = a'\hat{x}(s) + b'\hat{v}_{batt}(s) + c'\hat{e}(s) \tag{4.24}$$

### 4.5.4 Control-to-output transfer function

The variation in the output voltage with a variation in the control signal is given by the open-loop control-to-output transfer function. This transfer function is derived in the similar way as in the forward mode, shown in the appendix, and is expressed as,

$$\frac{\hat{v}_s(s)}{\hat{e}(s)} = G_{cf} \cdot \frac{1 - \dfrac{s}{\omega_{z_2}}}{1 + \dfrac{s}{\omega_{L_{cf}}/C_a} + \dfrac{s^2}{\omega_{L_{cf}}\omega_{c_{cf}}/C_a}} \tag{4.25}$$

It provides information on the corner frequencies due to the load, the zero and the crossover of the inner current-loop. The open-loop control-to-output transfer function

determines how the system responds to sinusoidal inputs because reference signals, disturbances etc. can be represented as sinusoids. The loop gain provides information on the overall system stability. The transfer function defines the compensator characteristics required in order to provide the overall open loop response to the system.

### 4.5.5 Line-to-output transfer function

The open loop change in the output voltage due to a variation in the input voltage (audio susceptibility) is given by the expression,

$$\frac{\hat{v}_s(s)}{\hat{v}_{batt}(s)} = A_{g_{cf}} \cdot \frac{1 + \dfrac{s}{\omega_{z_1}}}{1 + \dfrac{s}{\omega_{L_{cf}}/C_b} + \dfrac{s^2}{\omega_{L_{cf}}\omega_{c_{cf}}/C_b}}. \tag{4.26}$$

## 4.6 Theoretical Frequency Response from Small-Signal Analysis

Bode plots are used to determine the frequency response of the converter. The theoretical Bode plot of the control-to-output transfer function uses the numerical values of the components calculated in the design example of the bi-directional described in chapter 5. The compensated error amplifiers for both operating modes are designed and their elements are suitably chosen. For the compensator plot values calculated in chapter 5 during the design of the compensated error amplifier to provide the converter with the desired characteristics have been used.

The theoretical plots show the open-loop frequency response for the open-loop

control-to-output transfer function, the compensated error amplifier and the overall compensated bi-directional converter in both operating modes. These plots are produced using the mathematical software package MathCad 7.0.

### 4.6.1 Bode plots for the forward mode

The theoretical Bode plots for the open-loop control-to-output transfer function, the compensator transfer function and the overall open-loop response of the converter in the forward mode are shown in Fig. 4-6. The relevant corner frequencies clearly indicated on them.

All parameters have been derived and defined in the appendix with the small-signal analysis and their numerical values are chosen from the design example in chapter 5. For the control-to-output transfer function, the 360 V DC bus is charging the battery to 54.65 V at 1 A charging current.

The theoretical Bode plots show a crossover frequency of 2.9 kHz for the compensated converter. The load corner frequency provides the dominant pole at 6.2 Hz. The second pole for the power stage is at the crossover frequency of the loop gain of the minor current loop, $\omega_c$, at $(2\pi)120$ kHz and can be approximated by,

$$\omega_c = \frac{\omega_s}{\pi n(1 - D_{ss})}$$

where $\omega_s$ is the converter switching frequency and $n$ is ratio of the slope of the stabilizing ramp to the inductor current slope during the ON time. $\omega_c$ is the only visible proof of the current loop after it has been absorbed into the new power stage. The zero occurs due to the output capacitor esr, at the corner frequency of $\omega_z$ equal to $(2\pi)6.7$ kHz.

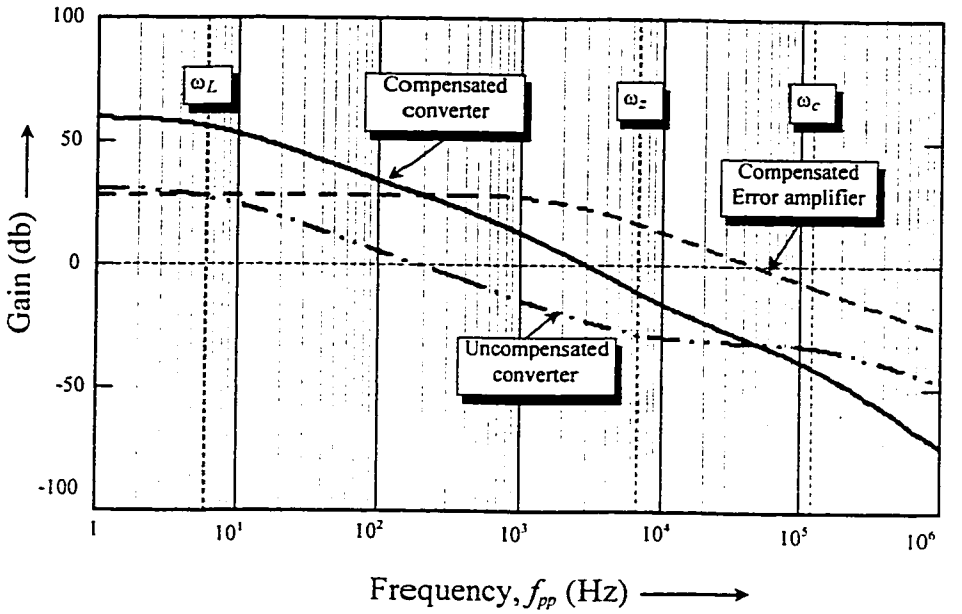



**Fig. 4-6 Theoretical Bode plot for the forward mode.**
Open-loop response of the uncompensated converter, compensated error amplifier and the overall compensated converter. (Input DC bus voltage = 360 V, battery voltage = 54.65 V, battery charging current = 1 A)

The compensating elements of the error amplifier are chosen so as to provide a pole at 1.78 kHz and a gain of about 28 dB. The pole compensates for the zero and provides the desired response characteristics to the converter.

### 4.6.2 Bode plots for the backup mode

The theoretical Bode plots for the small-signal control-to-output transfer function, the compensated error amplifier and the resulting overall compensated system are shown in Fig. 4-7, as also the corner frequencies indicting the poles and zeros of the system. The values for the various parameters of the transfer functions and the design of the compensator are given in the converter design in chapter 5 and Appendix A.

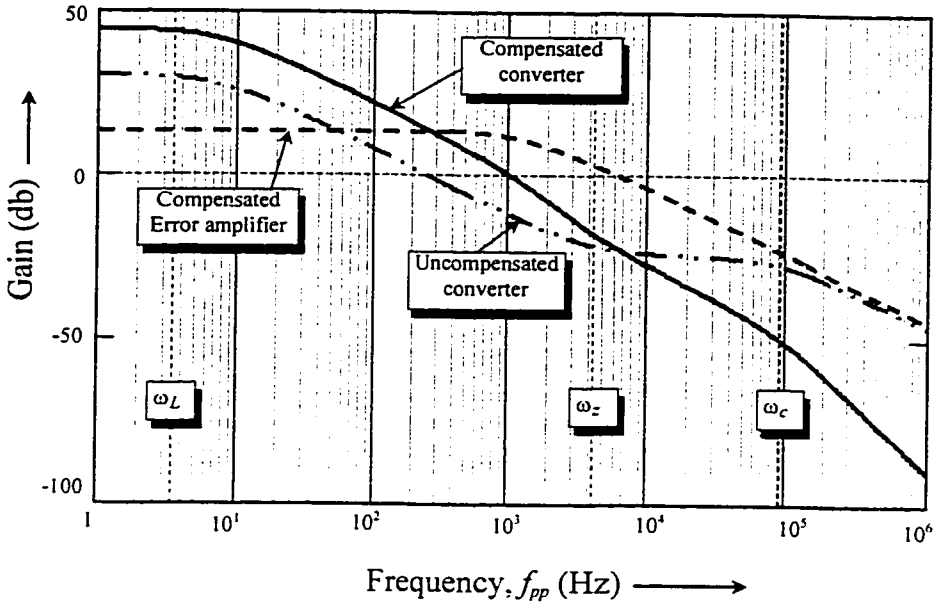



**Fig. 4-7 Theoretical Bode plot for the backup mode.**
Open-loop response of the uncompensated converter, compensated error amplifier, and the overall compensated converter. (Battery voltage = 50 V, output power = 187 W, output (dc bus) voltage = 326 V)

The theoretical Bode is plotted for a battery voltage of 50 V powering the DC at 326 V with 187 W (75%) load at the bus. The gain plot for the power stage shows the presence of the dominant pole due to the load at 3.5 Hz, the right half plane (rhp) zero at the corner frequency of 4 kHz, and the second pole at the crossover frequency of the current loop at 90 kHz. The compensation network of the error amplifier is chosen to compensate for the rhp zero and provide a crossover frequency below the corner frequency of the rhp zero. The choice of the elements of the compensator is detailed in the design example in chapter 5. The compensated error amplifier adds a pole at 1.7 kHz.

The overall open loop response of the converter is now plotted and is seen to have a cross over frequency of 1 kHz for the specific operating conditions. The theoretical value of the gain is also found to be sufficiently high at 44 dB.

## 4.7 EXPERIMENTAL VERIFICATION OF SMALL-SIGNAL ANALYSIS

A bi-directional converter is designed in chapter 5, using the steady state and the small-signal analysis presented in chapters 3 and 4, respectively. The theoretical Bode plots in section 4.6 are plotted with the numerical values of components used in the actual implementation and provide a basis for validating the small-signal analysis. To verify the small-signal analysis and the accuracy of the theoretical Bode plots, the open loop frequency response is obtained for both operating modes from the experimental setup of the converter.

Also, results of the dynamic response of the converter under various transient conditions are obtained from the practical converter setup. The converter response validates the small-signal analysis and the transfer functions.

The transient performance of the bi-directional converter is evaluated under the following conditions:

1 - Step change in load while operating in the backup mode.

2 - Switchover from the forward to the backup mode at 75% load at the DC bus when the battery is in the charged state.

3 - Switchover from forward to the backup mode at 75% load on the DC bus when the battery is drawing a charging current of 1A.

These transient conditions provide a good estimate about the stability and the response time of the converter. The results for the switchover from the backup to the forward mode are not presented as they are not a critical dynamic characteristic of the bi-directional converter. This effect can be explained by the fact that when the ac line comes back, the DC bus voltage rises and on crossing the 325 V threshold, begins to power the

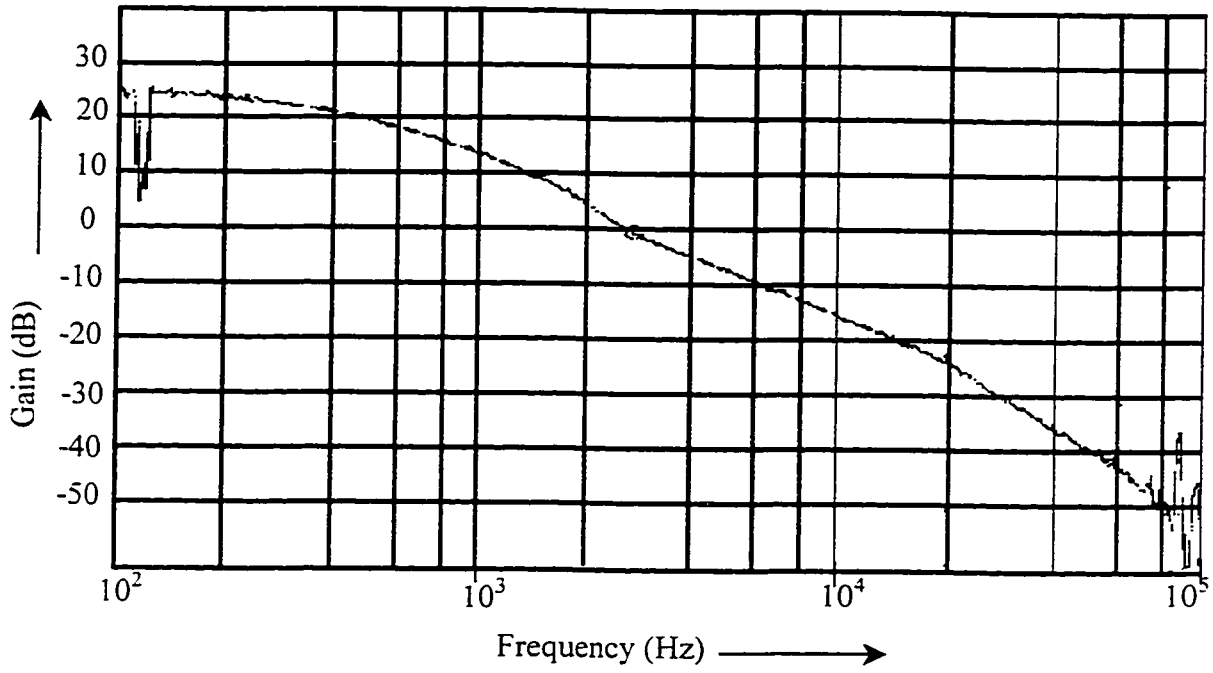
loads at the DC bus. The bi-directional converter now operates in the forward mode to charge the battery. The error amplifier for the backup mode reduces the inductor current resulting in a smooth transition from one operating mode to the another. In the actual setup, a delay is allowed before the battery begins to charge again to ensure the presence of a stable ac line and thereby prevent short unwanted switchovers from the backup to the forward mode and vice-versa.

### 4.7.1 Bode plot of the open loop frequency response in the forward mode

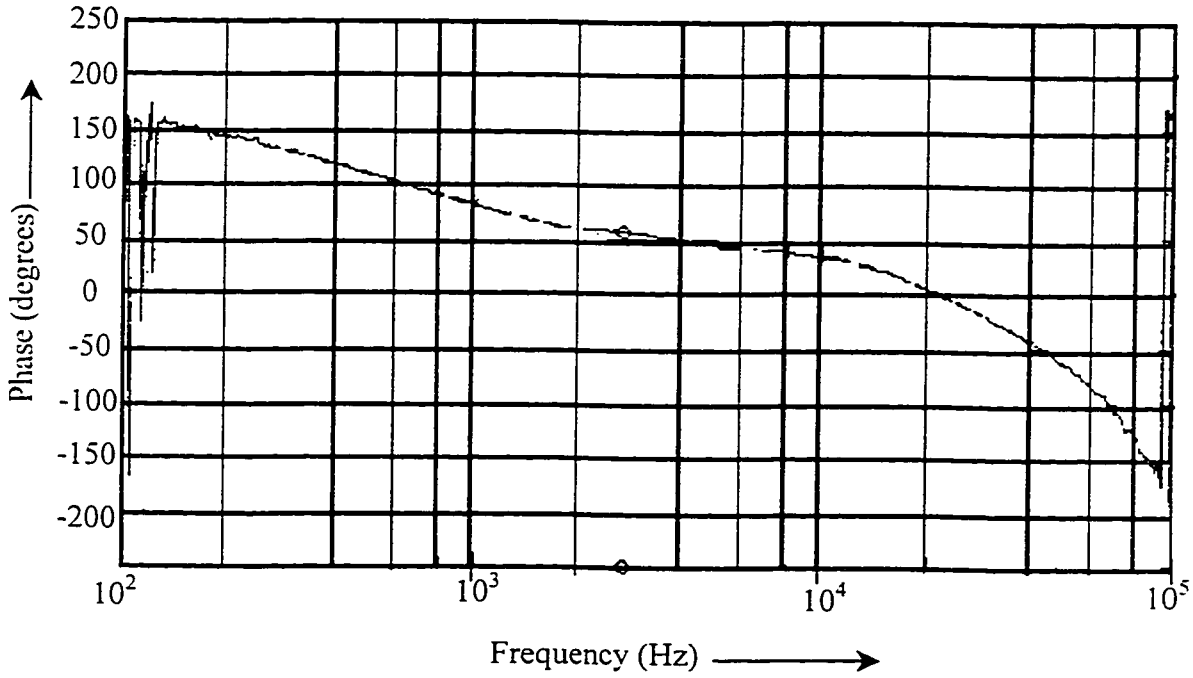
The experimental open loop control-to-output response for the forward mode of the converter designed in chapter 5 is shown in Fig. 4-8. This response is obtained for the converter operating off a 360 V DC bus, charging the battery to 54.65 V at 1 A current.

The magnitude plot, Fig. 4-8(a) shows the crossover frequency of the converter at 2.75 kHz. This crossover occurs below the corner frequency of the zero. The slope of the magnitude plot at the crossover is approximately –20 dB/decade. The laboratory equipment limits the lower value of the frequency to 10 Hz. In addition there is inaccuracy at lower frequencies due to the other test equipment like the transformer. Due to these practical limitations the gain at frequencies lower than 50 Hz may not be accurate. The gain at 100 Hz is approximately15 dB and it is expected that the DC gain is sufficiently high.

The phase plot for the forward mode of operation is shown in Fig. 4-8(b). This plot is the inverted due to the error amplifier configuration and is 180 degrees out of phase. Thus at 0 dB, the phase is –180 + 56 = - 124 degrees and the phase margin is 56 degrees. The magnitude and phase plots suggest that the converter is adequately stable against transient conditions in the forward mode.




(a)




(b)

**Fig. 4-8 Experimentally obtained Bode plot for the forward mode.**

Open loop frequency response of the control-to-output transfer function (a) Magnitude plot. (b) Phase margin plot. (Input DC bus voltage = 360 V, output battery voltage = 54.65 V, output power = 54.65 W)

### 4.7.2 Bode plot of the open loop frequency response in the backup mode

The open loop control-to-output transfer function and the design of the compensated error amplifier in the feedback path is verified by the experimentally obtained open loop frequency response of the converter operating in the backup mode. These results are obtained when the converter is operating with the battery at 50 V powering the DC bus at 326 V at 75 % of the rated load.

The magnitude plot in Fig. 4-9 shows the crossover of the compensated system at 944 Hz. The crossover frequency is below the corner frequency for the right half plane zero so that the phase lag does not exceed 180 degrees and high enough to provide large bandwidth over which the benefits of feedback are realized.

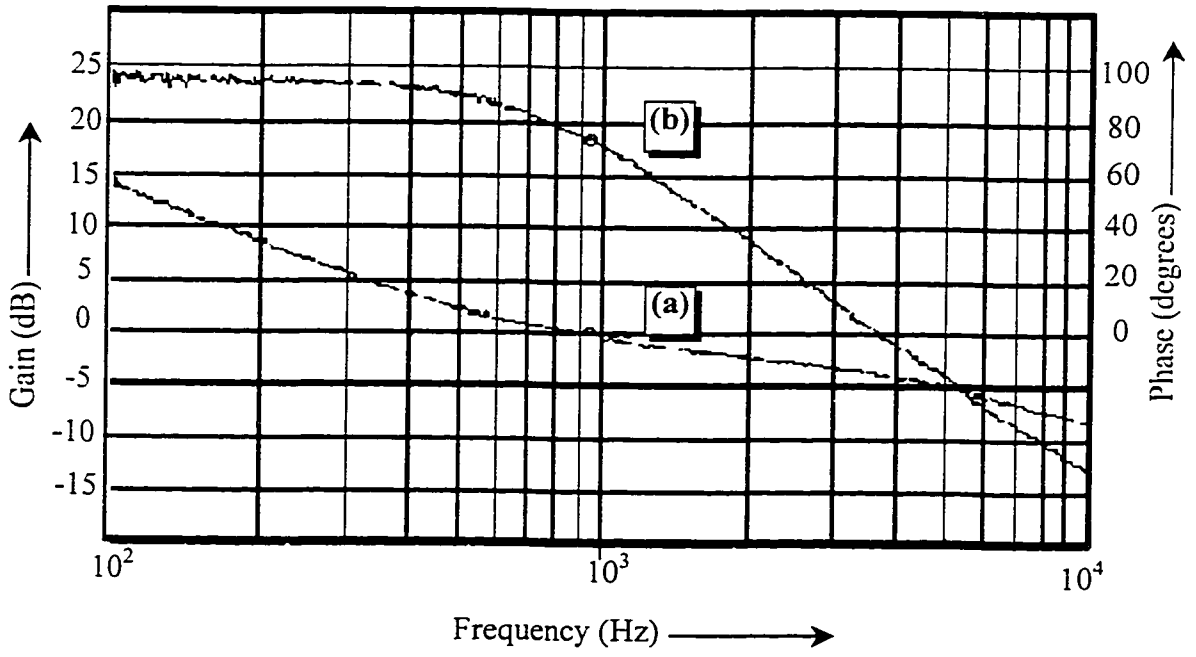



**Fig. 4-9 Experimentally obtained Bode plot for the backup mode.**
Open loop frequency response of the control-to-output transfer function.(a) Magnitude plot. (b) Phase margin plot. (Battery voltage = 50 V, output DC bus voltage = 326 V, output power at DC bus = 190 W.)

The phase plot is once again out of phase by 180 degrees due to the inverting error amplifier. Thus, at unity gain, the phase of 72 degrees in Fig. 4-9 corresponds to an actual phase of $-180 + 72 = -108$ and the phase margin of the voltage loop gain is at an acceptable value of 72 degrees, Fig. 4-9. The Bode plots from the experimental setup verify the small-signal analysis and the choice of the elements of the compensating network in the error amplifier to provide the overall dynamic response to the system.

### 4.7.3 Step change in load in the backup mode

The transient in the load is observed in the backup mode when the load at the DC bus changes from 25% to 75% of the rated full load. The battery voltage is at 50 V and provides backup power to the DC bus. Fig. 4-10 shows the change in the load current $I_{bus}$ from 0.2 A to 0.57 A. The inductor current attains a steady state value of 4.05 A when the load current at the DC bus is 0.57 A.

The output voltage is regulated at 323 V. The waveform for the voltage at the DC bus when shown over a smaller scale indicates a negligible dip of about 2 V during the transient condition. The voltage quickly regains its steady state value and does not cause any adverse stress on the down stream converters being powered from the DC bus.

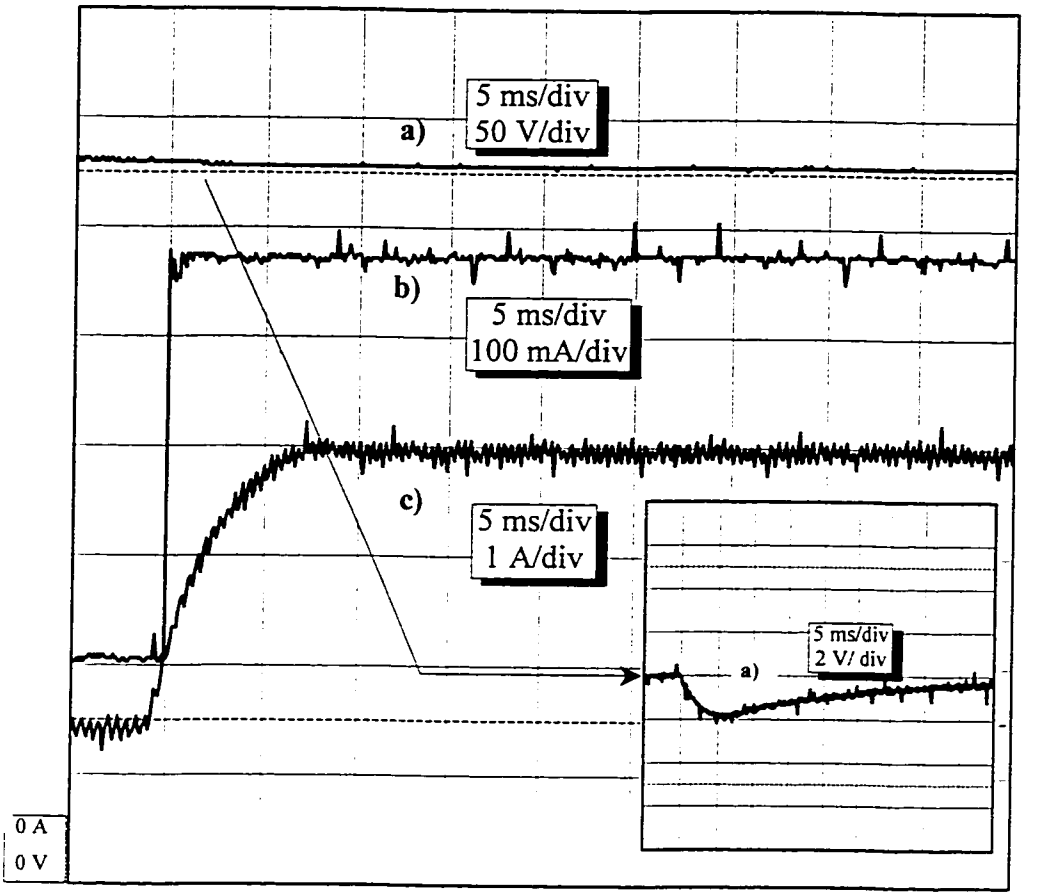



**Fig. 4-10 Step change in load (25% to 75%) in the backup mode.**
(a) Voltage at the DC bus, $V_S$. (b) Current at the DC bus, $i_{bus}$. (c) Current in the inductor, $i_{L_o}$. (Battery voltage = 50 V, output voltage = 323 V)

### 4.7.4 Switchover from forward to backup mode when battery is charged

When the battery is in the charged state and the DC bus fails, the converter must switchover from operation in the forward mode to the backup mode. Fig. 4-11 shows the switchover to the backup mode when the load at the DC bus is 75% of the rated full load and the battery is charged at 53 V, therefore drawing minimal trickle current. In the forward mode, the voltage at the DC bus is 360 V and after the switchover is regulated at 325 V in the backup mode, Fig. 4-11(a).

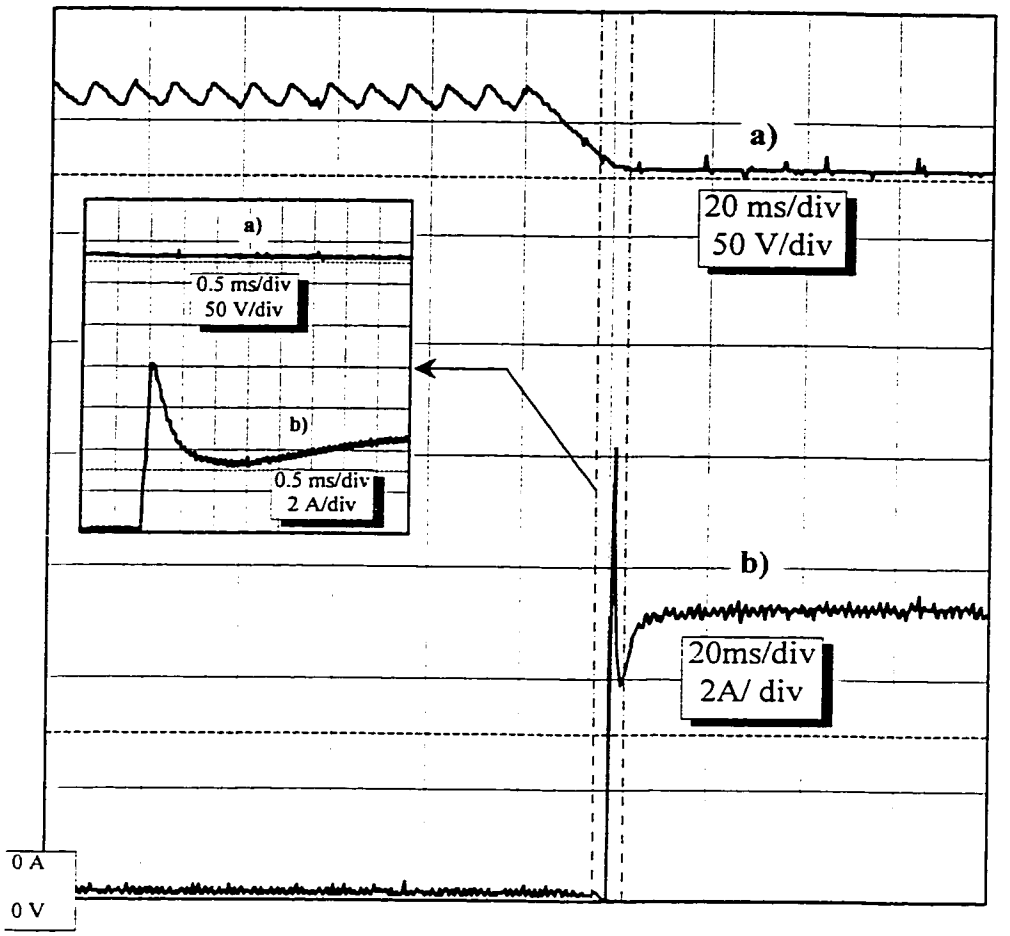



**Fig. 4-11 Switchover from forward to backup mode with a charged battery and 75% load at the DC bus.**

(a) DC bus voltage, $V_S$. (b) Current in the inductor, $i_{L_o}$. (Forward mode: input voltage = 360 V, battery voltage = 53 V, load power at the DC bus = 190 W; Backup mode: Battery voltage = 53 V, DC bus voltage = 323 V, load power at the DC bus = 190 W.)

The voltage at which the backup mode delivers power to the DC bus has been chosen at 325 V but any other value that lies within the operating input voltage range of the DC bus voltage can be selected. This is justified by the fact that the voltage at the DC is the input voltage for down stream converters that have an working input voltage range as that specified for the operating input voltage of the bi-directional converter in the forward mode.

When the ac mains, which is providing power to the DC bus fails the voltage at the DC bus begins to drop. As soon as the bus voltage is detected below 325 V, the converter begins operation in the backup mode and regulates the DC bus to 325 V. As mentioned, other values of the regulated DC bus voltage can be provided for by simple changes in the line and bulk detection circuitry.

The waveforms shown over a smaller time interval clearly demonstrate the change in the direction of the inductor current $i_{L_o}$, Fig. 4-11(b) which reaches the steady state value in a very short time duration. The output voltage has no glitch because the switchover to the backup mode occurs before the DC bus voltage goes out of the operating range.

### 4.7.5 Switchover from forward to backup mode when battery draws current

The dynamic response of the converter is evaluated for the condition when the switchover from the forward to the backup mode occurs with the battery at 50 V drawing a charging current of 1 A. The inductor current and the DC bus voltage waveforms are depicted in Fig. 4-12 for this transient condition. The forward mode operation is at DC bus voltage of 360 V. The load at the DC bus is 75% of the rated full load value. In the backup mode the DC bus voltage is regulated at 325 V. The expanded view of the inductor current over a smaller time interval shows the change in direction in a short time duration.

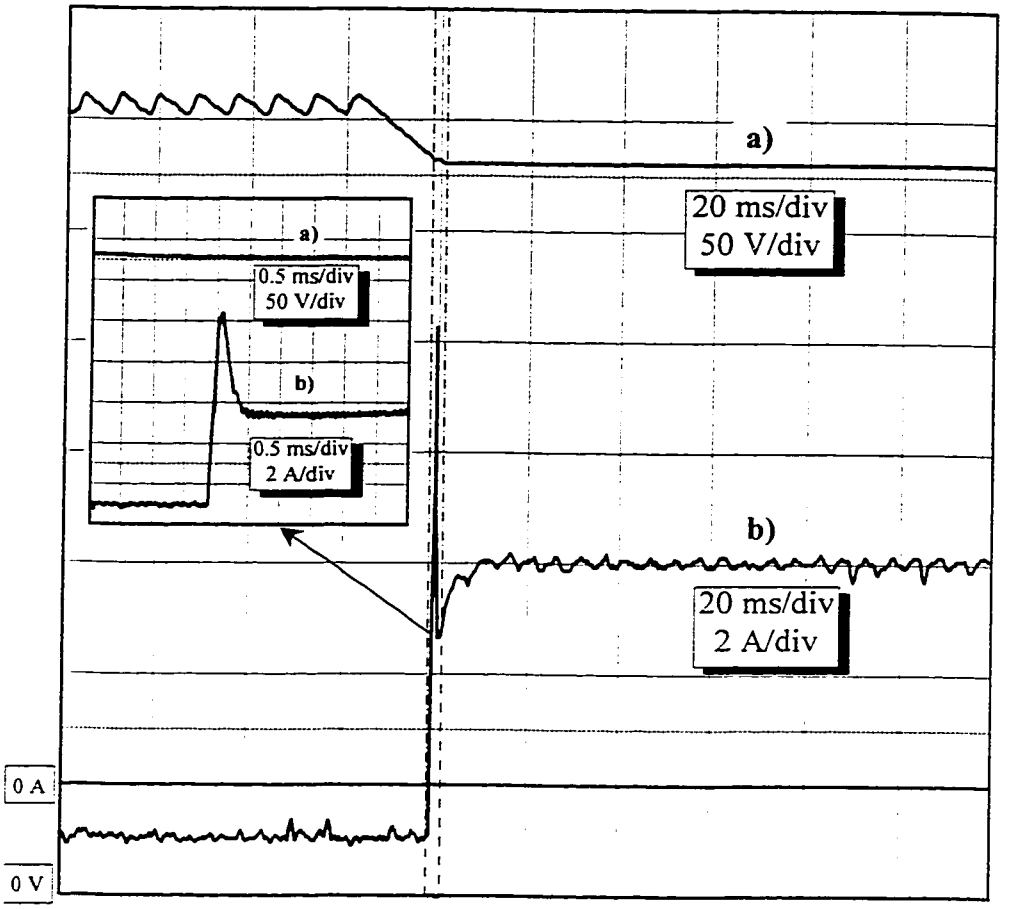



**Fig. 4-12 Switchover from forward to backup mode with the battery drawing charging current and 75% load at the DC bus.**

(a) DC bus voltage $V_S$. (b) Current in the inductor $i_{Lo}$. (Forward mode: input voltage = 360 V, battery voltage = 50 V, battery charging current = 1 A, load power at the dc bus = 190 W; Backup mode: battery voltage = 50 V, dc bus voltage = 325 V, load power at dc bus = 190 W.)

## 4.8 CONCLUSIONS

The small-signal ac characteristics of the bi-directional converter in both operating modes are obtained by means of the state-space averaging technique. Key transfer functions describing the dynamic behavior of the converter are derived which determine the design of the appropriate compensated error amplifiers to ensure desired

response of the compensated converter. Theoretical and experimental frequency response plots provide information on the gain bandwidth and the phase of the converter and are compared to show the accuracy of the small-signal analysis. Experimental results of the practical implementation under the transient conditions validate the selection of the compensation network parameters for both operating modes, which are a direct outcome of the small-signal analysis.

# CHAPTER 5
# DESIGN EXAMPLE

## 5.1 INTRODUCTION

This chapter presents the design procedure for the practical implementation of the bi-directional dc-dc converter. A design example of the converter is given to illustrate the selection of the power components using the characteristic curves and equations derived in chapter 3. The ratings of the components from the design curves provide a good approximation for the final values used in an actual. As the final values of the components used in the implementation are obtained after a few iterations of the theoretically calculated ones, both the theoretical and the actual values used in the experimental setup are provided. The qualitative constraints that define the converter design are also incorporated in the design procedure to provide a detailed design example.

Parameters from the characteristic design curves for operating conditions other than those used in the plots can be obtained easily as the underlying design procedure is the same for all conditions. Once the selection and rating of the basic power components is complete, the values for the compensating network of the error amplifiers in the

feedback paths are chosen. The Bode plots of the transfer functions for both operating modes, presented in chapter 4, provide information on the dynamic characteristics of the converter. Accordingly the parameters of the compensated error amplifier are selected to provide the desired response of the overall system under transient conditions.

## 5.2 DESIGN SPECIFICATIONS

The bi-directional converter is designed according to the following specifications:

Input voltage range at the DC bus = 300 V ($V_{S_{min}}$) – 400 V ($V_{S_{max}}$)

Output power while charging the battery in the forward mode, $P_{batt}$ = 100 W

Switching frequency in the forward mode, $f_s$ = 100 kHz

Output power at the DC bus in the backup mode, $P_{bus}$= 250 W

Output voltage at the DC bus in the backup mode, $V_{bus}$ = 325 V

Switching frequency in the backup mode, $f_s$ = 100 kHz

The reasons for these specifications in the practical implementation are as follows:

(i) The down stream converters (loads) powered from the DC bus have a working input voltage range of 300 V – 400 V and demand 250 W. This defines the operating input voltage range for the bi-directional converter in the forward mode and also the power to be delivered to the DC bus in the backup mode.

(ii) The power delivered to the battery in the forward mode is conventionally between one-half to one-third of that delivered to the DC bus in the backup mode. Using this convention the forward mode power rating has been defined at 100 W.

(iii) The output voltage at the DC bus in the backup mode must be some value between the working voltage range at the DC bus. This value is chosen at 325 V though any other value can easily be selected.

(iv) The switching frequency of the bi-directional converter is specified at 100 kHz to reduce the physical size of the magnetic components in the circuit. A tradeoff is made between a high switching frequency that reduces size of the magnetic components and a lower frequency that would reduce switching losses.

The design curves presented in Fig. 3-2 to Fig. 3-9, Fig. 3-11 and Fig. 3-12 provide suitable normalized ratings of components in the power circuit under worst case conditions to ensure proper operation of the converter. These curves are plotted as a function of the per-unit variation in the DC bus voltage $V_S$ which is defined in the design specifications.

## 5.3 SELECTION OF THE POWER COMPONENTS

The base quantities defined in section 3.3 are used for the selection of the power components. The variation in the DC bus voltage around its nominal value is 0.143 pu which gives values for the variables $V_{S_{max}}$ and $V_{S_{min}}$. The operating frequency in both modes is 1 pu, and the power at the battery end in the charging mode, $P'_{batt}$, is 0.4 pu. For simplicity in calculations the variation in the DC bus is taken as 0.14 pu.

### 5.3.1 Backup battery voltage

The battery voltage must be selected first according to the constraint that the

output voltage of the converter in the backup mode must be greater than or at least equal to the minimum DC bus voltage $V_{S_{min}}$. This condition must be satisfied even when the secondary side switches are being gated at their minimum duty ratio and are being supplied from the maximum battery voltage.

Using this basic constraint, the normalized value of the nominal battery voltage for the bi-directional converter to operate as a boost-derived converter in the backup mode is 0.368 pu, calculated from the following expression:

$$V'_{batt} = \frac{V'_{batt_{max}}}{1.167} \quad \text{pu,} \tag{5.1}$$

where, $V'_{batt_{max}}$ is the maximum pu battery volatge given by,

$$V'_{batt_{max}} = \frac{V_{S_{min}}}{2 \cdot N} \quad \text{pu} \tag{5.2}$$

The normalized value of the battery voltage corresponds to the real value of 128.9 V for a transformer with unity turns ratio.

In the actual experimental setup a lower voltage battery is chosen. A tradeoff is made between the estimated conduction losses in the circuit, that are directly proportional to the maximum charging current drawn by battery, and the physical size and cost of the battery. A 48 V (nominal voltage) battery is chosen.

### 5.3.2 Transformer turns ratio

The design curves in chapter 3 are normalized with the assumption of a unity turns ratio transformer. This implies that with a deviation in the nominal battery voltage from the value calculated for an ideal transformer, the turns ratio can no longer be kept at

unity if the converter operating specifications are to be met. With a 48 V battery the corresponding value of transformer turns ratio, $N$, is calculated from (5.2).

The ratio of the number of turns of the primary to the secondary winding is now calculated to be,

$$N = 2.687 \tag{5.3}$$

Therefore, the values obtained from the design curves must be converted to their real values and then transformed accordingly using the new transformer turns ratio of 2.687.

### 5.3.3 Switch duty ratios

Theoretically, the maximum duty ratio of the switches in the forward mode is 0.5 and the minimum duty of the switches in the backup mode is greater than 0.5 to ensure proper operation of the converter.

For the specified operating conditions, with a unity turns ratio transformer the maximum and minimum duty ratios for the switches $S_1$ to $S_4$ obtained from the characteristic curves for the duty ratios, Fig. 3-2, are:

$$d_{fw_{min}} = 0.377,\ d_{fw_{max}} = 0.5,\ D_{min} = 0.57, \text{ and } D_{max} = 0.678.$$

### 5.3.4 Inductor, $L_o$:

The minimum value of the inductor, $L'_{o_{min}}$, required to maintain continuous inductor current is obtained from Fig. 3-3. For the forward mode operation, with $P'_{batt}$ = 0.4 pu, this value is determined to be $L'_{o_{min}}$ = 1.78 pu. This is calculated at a minimum load at the battery end of 0.04 pu. In the backup mode, $L'_{o_{min}}$ = 0.582 pu with a minimum

load of 0.1 pu at the DC bus.

The normalized values in the forward and backup modes are converted to the real values and then transformed according to the appropriate transformer turns ratio. The minimum inductance in the forward mode corresponds to 192.67 μH and in the backup mode the minimum inductance required to maintain continuous inductor current under worst case conditions is 62.85 μH. Therefore, the worst case value of 192.67 μH from the forward mode is chosen as the minimum value of the inductance $L_{o_{min}}$.

### 5.3.5 Switches, $S_1$ and $S_2$:

The worst case ratings of the primary side MOSFETs are determined for the maximum reverse voltage across them and the current through them, which allows selection of the appropriate switch. Fig. 3-4 indicates that the maximum reverse voltage stress across the primary side switches is 1.14 pu in the forward mode. In the backup mode the body diodes of the switches, $D_{S_1}$ and $D_{S_2}$, are subject to a maximum reverse voltage of 1 pu across them. Thus, the switches must be rated for the maximum voltage stress which is 1.14 pu and corresponds to 400 V.

The maximum rms current through the switches $S_1$ and $S_2$ in the forward mode, given by Fig. 3-5, is 0.658 pu when $P'_{batt}$ = 0.4 pu. The average current through their body diodes in the backup mode is 0.5 pu, obtained from Fig. 3-12. The desired rms current rating of the switch is thus determined to be at least 0.47 A and the maximum average current through the switch body diodes is 0.429 A under the worst conditions.

### 5.3.6 Switches, $S_3$ and $S_4$:

The voltage stress across the switches $S_3$ and $S_4$ is determined by the design curve provided in Fig. 3-6. The body diodes of $S_3$ and $S_4$ provide battery side rectification in the forward mode. They are subject to a maximum voltage stress of 1.14 pu in the forward mode during the interval when they are not forward biased. In the backup mode the switches $S_3$ and $S_4$ are gated and are subject to a voltage stress of 1 pu as indicated in Fig. 3-6. Thus, $S_3$ and $S_4$ are rated for the maximum reverse voltage of 1.14 pu across them. This corresponds to a real value of 400 V.

The maximum average current through $D_{S_3}$ and $D_{S_4}$ in the forward mode is 0.465 pu, Fig. 3-7, and the maximum rms current through the switches $S_3$ and $S_4$ in the backup mode is 1.99 p.u, Fig. 3-11. Thus, the real value of the average current through their body diodes is 0.893 A and the real value of the rms current through $S_3$ and $S_4$ in the backup mode is 3.823 A. The MOSFETs for $S_3$ and $S_4$ are chosen to withstand 400 V across them and carry 3.823 A rms current through them.

### 5.3.7 Output Filter capacitor, $C_o$:

The minimum value of the output filter capacitor is determined by the dominant constraint that it will have to absorb the energy from the inductor if the battery is suddenly removed. The design curve in Fig. 3-8 for $P'_{batt} = 0.4$ pu gives the value of $C'_o$ as $7.42 \cdot 10^3$ pu. This corresponds to a real value of 174 μF for $C_o$.

### 5.3.8 Capacitors $C_1$ and $C_2$:

The capacitors $C_1$ and $C_2$ provide filtering action for the input voltage ripple in the

forward mode and hold-up time during the switchover to the backup mode. The filtering action provided by the capacitors in the forward mode is expressed by (3.9) and shown graphically as a function of the normalized variation in the input DC bus voltage in Fig. 3-9. The characteristic curve gives the value for each capacitor as $3.876 \cdot 10^4$ pu at a battery power of $P'_{batt} = 0.4$ pu. This normalized value corresponds to 125.9 μF when converted to the real value using the appropriate base capacitance.

### 5.3.9 Transformer primary winding, *Np*:

As the voltage applied to the primary winding in the forward mode of operation is a square wave the minimum number of primary turns can be calculated using the volt-second approach according to which the primary volt-seconds per turn is equal to the secondary volt-seconds per turn. The number of turns of the primary winding in the transformer is therefore given by,

$$N_p = \frac{V_S \cdot t \cdot 10^2}{\Delta B_{ac} \cdot A_e} \tag{5.4}$$

where $V_S$ = applied DC voltage across the winding (V)

$t$ = ON time duration (μs)

$\Delta B_{ac}$ = maximum excursion of the ac flux density (Gauss)

$A_e$ = effective cross-sectional area of the core ($cm^2$)

For the design process a PQ 35/35 core was chosen with $A_e = 1.96$ $cm^2$. The total flux excursion was ± 1300 gauss, giving the value of $\Delta B_{ac} = 2600$ gauss. With a

minimum applied DC bus voltage of 300 V and the maximum ON time duration of $d_{fw_{max}} T_s$ the minimum primary turns is calculated from (5.4) as,

$$N_p = \frac{300 \cdot 5 \cdot 10^2}{2600 \cdot 1.96}$$
$$= 14.7$$

To avoid half turns the number of primary turns is taken as 15.

Once the number of primary turns is known and the core material has been selected the magnetizing inductance of the primary winding $L_p$ can be calculated by the following expression:

$$L_p = A_L \cdot N_p^2 \tag{5.5}$$

where $A_L$ = the inductance factor or the inductance per turn ($\mu H/N^2$)

The core material selected is PC 30, for which $A_L$ = 4.86 $\mu H/N^2$. Thus from (5.5) the magnetizing inductance of the primary winding is calculated as,

$$L_p = 4.86 \cdot 15^2$$
$$= 1.10 \text{ mH}$$

### 5.3.10 Transformer secondary winding, $N_s$:

From the value of the transformer turns ratio $N$ (5.3) and the number of turns of the primary winding (5.4) the number of turns of the transformer secondary winding are calculated by,

$$N_s = \frac{N}{N_p} \tag{5.6}$$

Thus the value of $N_s$ is 5.6. This is approximated to 6 whole turns. The magnetizing inductance of the secondary windings is calculated by an expression similar to (5.5) where the number of primary turns is substituted by the number of secondary turns and gives the magnetizing inductance of the secondary winding as $L_s$ = 175 μH.

### 5.3.11 Balancing winding, $N_{p1}$:

The forward mode of operation dictates that the number of turns on $N_{p1}$ be equal to $N_p$, which results in equal magnetizing inductance, to prevent the saturation of the core. In the backup mode, it was determined that the wire diameter for both the windings should be equal as they carry equal current. Thus, the winding $N_{p1}$ is identical to $N_p$ and has 15 turns and 1.10 mH magnetizing inductance.

### 5.3.12 Catching diodes, $D_1$ and $D_2$:

$D_1$ and $D_2$ have voltage and current stresses equal to those of the body diodes of $S_1$ and $S_2$ in the backup mode as they permit simultaneous charging of $C_1$ and $C_2$ in conjunction with the body diodes of the switches. In the forward mode these diodes carry minimal current only when balancing the mid-point of $C_1$ and $C_2$ and are subject to a maximum voltage stress of 1 pu. Thus, they are rated according to the stresses in the backup mode where, the maximum voltage stress across them is 400 V and the average current through them is 0.429 A.

## 5.4 COMPONENT RATINGS AND VALUES USED IN EXPERIMENTAL SETUP

The numerical values for the component ratings and parameters generated by the design curves provide a theoretical basis and close approximation for the values actually used in the experimental setup. In the actual implementation of the prototype some of the values may vary a little due to practical constraints but the above mentioned procedure and the design expressions presented in chapter 3 are valid for the new values chosen. The iterations in obtaining the final values are described in the following text.

In order to provide a dead time between the ON times of the switches in the forward mode the maximum duty ratio of $S_1$ and $S_2$, $d_{fw_{max}}$, is chosen to be 0.435 and not the theoretically ideal value of 0.5. A change in the maximum duty ratio implies a change in the transformer turns ratio if the same battery with 48 V nominal voltage is to be used. For a battery with 48 V nominal voltage, the operating range is specified between 54.65 and 42 V.

The switch duty ratios can be re-calculated for different battery voltages and turns ratio by the following expressions.

$$\left.\begin{aligned} d_{fw_{min}} &= \frac{N \cdot V_{batt_{max}}}{V_{S_{min}}} \\ d_{fw_{max}} &= \frac{N \cdot V_{batt_{max}}}{V_{S_{min}}} \\ D_{max} &= 1 - \frac{V_{batt_{min}} N}{V_S} \\ D_{min} &= 1 - \frac{V_{S_{min}}}{2V_S} \end{aligned}\right\} \qquad (5.7)$$

Substituting the values for the maximum duty ratio for $S_1$ and $S_2$ and the maximum battery voltage in (5.7) gives the transformer turns ratio $N$ as 2.38.

For the same value of $N_p$ the new value of $N_s$ is calculated from (5.6) to be 6.303. This is again approximated to 6 full turns and the magnetizing inductance is $L_s$ = 175 μH.

(5.7) gives the maximum and minimum duty ratios of the switches $S_3$ and $S_4$ by substituting the appropriate values in the equations. Therefore $D_{max}$ = 0.692 and $D_{min}$ =0.6. The maximum voltage across each secondary winding in the backup mode $V_{sec}$ is calculated to be 60 V for the minimum duty ratio and maximum battery voltage conditions. The magnetizing current $I_m$ in the secondary winding under these conditions is determined by the expression,

$$I_m = \frac{V_{sec}}{L_s \cdot D_m} \quad \text{A} \tag{5.8}$$

where $D_m$ = duty ratio for which the voltage appears across a secondary winding.

Thus the magnetizing current is,

$$I_m = \frac{60}{175 \cdot 0.1}$$
$$= 3.43 \text{ A}$$

To reduce the magnetizing current the magnetizing inductance of the secondary winding must be increased. Increasing the inductance will result in an increase in the number of turns of the secondary winding. Thus, while the maintaining the turns ratio constant, $L_s$ and therefore $N_s$ is increased. The magnetizing inductance cannot be increased infinitely as this would result in a very large inductor and lead to leakage between the primary and the secondary windings. Keeping these limiting factors in mind, a tradeoff is made between the size of the secondary winding and the value of the

magnetizing inductance (5.8). The final values chosen are:

$$L_s = 360\ \mu\text{H and } N_s = 8.$$

The corresponding values for primary turns $N_p$ = 19 and the primary winding magnetizing inductance $L_p$ = 2 mH.

The final circuit parameters and component values selected for the practical implementation are shown in Table 5-1.

| Parameters | Value/ Rating | Parameters | Value/ Rating |
|---|---|---|---|
| $D_1, D_2$ | MUR 460 | $L_p, L_{p_1}$ | 2 mH |
| $C_1, C_2$ | 150 μF | $L_s, L_o$ | 360 μH |
| $S_1, S_2$ | IRF 840 | $N_p$ | 19 |
| $S_3, S_4$ | IRFP 250 | $N_s$ | 8 |
| $C_o$ | 470 μF | $d_{fw_{max}}$ | 0.435 |
| $D_{max}$ | 0.725 | $d_{fw_{min}}$ | 0.326 |
| $D_{min}$ | 0.642 | | |

**Table 5-1 Components used in experimental setup.**

## 5.5 COMPENSATED ERROR AMPLIFIER DESIGN

Once the power components are selected, the small signal analysis, discussed in chapter 4, determines the open loop gain transfer functions for both modes of converter operation. The theoretical Bode plots for these transfer functions that describe the dynamics of the converter are plotted for the selected component values, Fig. 4-6 and Fig. 4-7.

To provide the necessary dynamic response characteristics to the converter a compensated error amplifier is added in the feedback path. The error amplifier is a suitably compensated operational amplifier that regulates the circuit so that it stays close to the nominal operating conditions in the face of disturbances and errors. The compensation network of the operational amplifier determines the dynamics of the overall converter.

### 5.5.1 Compensated error amplifier for the forward mode

The open loop control-to-output transfer function (4.14) and its corresponding Bode plot imposes requirements on the frequency response of the compensator. Loop response of the uncompensated power stage provides the necessary information to design the compensated error amplifier to achieve the desired response in the overall compensated converter.

The DC operating point for the theoretical Bode plots is chosen for the following conditions:

DC bus voltage = 360 V

Battery voltage = 54.65 V

Output power at the battery end = 54.65 W

The values for the basic parameters in the expressions of the small-signal analysis derived in chapter 4 are defined from the selected power components as follows.

The output operating point parameter, $R = \frac{(\text{dc output voltage})^2}{\text{output power}} = 54.65$

The *esr* of the output capacitor, $r_c = 50\ \text{m}\Omega$.

The effective current sensing resistor, $R_s = 1.7\ \Omega$

The parameter relating the slope of the stabilizing ramp and the inductor rising slope during the ON time, $n = 0.1$.

The other parameters in the transfer functions are calculated from the existing information of the power circuit components and substitution of the numerical values specified above according to the expressions derived in Appendix A.

The Bode plot in Fig. 4-6 shows the theoretical response of the open loop gain transfer function (4.14) of the power stage including the output filter for the forward mode operation for the selected numerical values.

The compensated error amplifier is designed to provide high gain at low frequencies, to minimize the steady-state error, and as high a crossover frequency as possible to the compensated converter.

The compensator receives its input from the comparator. The comparator compares the control voltage to a voltage proportional to the current flowing in the power stage inductor and thereby determines the instant at which the switch ON time is terminated. The waveforms in Fig. 4-3 show the comparator inputs over one equivalent switching period $T_{ss}$. One comparator input carries the control voltage $v_{control}$ plus the

negative stabilizing ramp of slope $-m_c$. The other input carries the inductor current with a positive slope $m_1$ and a negative slope $-m_2$. The expressions to calculate the numerical values of these parameters are given in the appendix with the detailed procedure for deriving the small-signal transfer functions.

To achieve the desired response in the overall converter the compensated error amplifier, Fig. 5-1, is designed to have a local feedback and is modeled by,

$$A_{comp_{vf}} = \frac{R_f}{R_{in} \cdot \left(1 + sR_f C_f\right)} \tag{5.9}$$

where $R_f$ and $R_{in}$ are feedback and input resistors and $C_f$ is the feedback path capacitor. These elements of the compensating network for the error amplifier are chosen to give the converter desirable dynamic characteristics. The above equation indicates the presence of a pole at a frequency equal to $1/(2\pi R_f C_f)$ which cancels the zero of the output filter in the power stage by proper selection of $R_f$ and $C_f$.

The predicted theoretical response for the transfer function of the compensated error amplifier (5.9) is shown in the Bode plot in Fig. 4-6. This frequency response is plotted for the following values of the compensating network:

$R_f = 270$ kΩ,

$R_{in} = 10$ kΩ, and

$C_f = 330$ pF.

which provide the desired dynamic response of the compensated system.

The overall open loop response is obtained by combining the transfer functions for the compensator (5.9) and the open loop control-to-output for the forward mode of the converter (4.14). This response has also been plotted in the same figure to show the effect

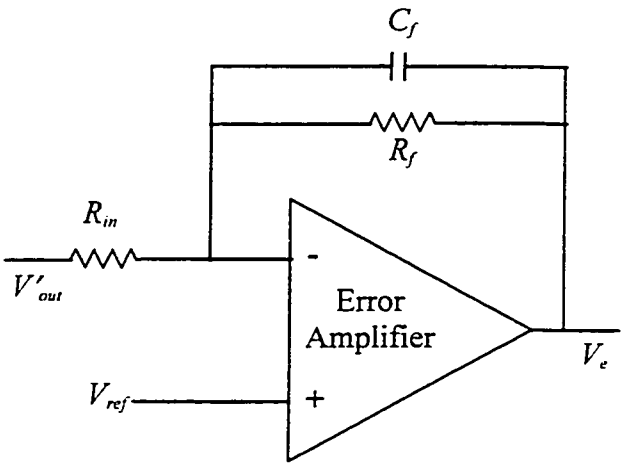



**Fig. 5-1 Compensation circuit for the error amplifier in the forward mode.**

of the compensated error amplifier on the uncompensated system. The compensator is seen to provide a suitably high gain bandwidth of 59 dB and crossover frequency of about 2.9 kHz to the converter.

### 5.5.2 Compensated error amplifier for the backup mode

The selected values of the power components are used to plot the theoretical open loop response of the converter in the backup mode, which is defined by the control-to-output transfer function (4.25). This provides the preliminary information to design the compensated error amplifier that will provide suitable dynamic characteristics to the overall system.

The frequency response is plotted for the following operating conditions:

Battery voltage = 50 V.

Output DC bus voltage = 326 V

Output power at the DC bus = 190 W

The numerical values for the parameters used in the transfer function are obtained from the selected power components. Some basic parameters are defined below and others are derived from the total available information, by the expressions derived in the Appendix A.

The output operating point $R = 605$.

The effective *esr*, $r_e$ , of the output capacitors, $C_1$ and $C_2$, is 50 mΩ.

The effective value of the current sensing resistor, $R_s = 10\ \Omega$

The parameter relating the stabilizing ramp and the inductor rising slope. $n = 0.1$.

The predicted Bode plot for the open loop control-to-output transfer function (4.25) is shown in Fig. 4-7. It describes the converter dynamics without the compensated error amplifier in the feedback path.

Using the Bode plot for the response of the open-loop control-to-output transfer function (4.25), the compensated error amplifier in the feedback loop is designed for the desired overall open-loop system response. The input to the error amplifier is from a comparator once again. The relationship between the two inputs of the comparator is shown in Fig. 4-5. The control voltage is defined by $e$, the slope of the stabilizing ramp is $-m_c$ , the positive slope of the voltage representing the inductor current is $m_a$ and the negative slope is $-m_b$. These parameters are defined by the expressions derived in the appendix.

The compensator response for the backup mode is modeled in the same way as that for the forward mode (5.9) shown in Fig. 5-2. The transfer function is given by,

$$A_{comp_{cf}} = \frac{R_{f_{cf}}}{R_{in_{cf}} \cdot \left(1 + sR_{f_{cf}} C_{f_{cf}}\right)} \tag{5.10}$$

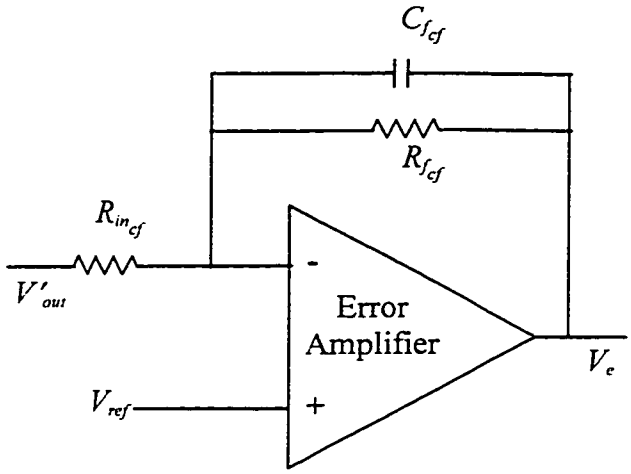



**Fig. 5-2 Compensation circuit for the error amplifier in the backup mode.**

The predicted frequency response of the transfer function of the compensated error amplifier (5.10) is also plotted in Fig. 4-7 for the following values of the compensating network parameters:

$R_f = 390$ kΩ.

$C_f = 330$ pF, and

$R_{in} = 78$ kΩ.

These values are chosen to provide the desired compensation to the power supply. Combining the transfer function of the compensated error amplifier (5.10) and the open loop control-to-output transfer function of the power stage (4.25), gives the theoretical open loop frequency response of the compensated system, Fig. 4-7.

This theoretical open loop response of the overall compensated system is found to be satisfactory with a gain bandwidth of 44 dB and a crossover frequency of 1 kHz, as shown in Fig. 4-7.

## 5.6 CONCLUSIONS

Component values and circuit parameters are defined for the design of a bi-directional converter. The converter is designed to operate over the entire range of the specified operating conditions. The design oriented approach outlined in chapter 3 provides a basis for the selection of the power components, but the final components used in practical implementation of the converter are obtained after suitable iterations. For the converter operation under transient conditions, the small-signal transfer functions derived in chapter 4 are used to design the compensated error amplifiers in the feedback path for both operating modes. The error amplifiers are tailored to provide the desired dynamic characteristics to the bi-directional converter. The design example has demonstrated a simple design process using the design equations and curves to select and rate the components for the practical implementation.

# CHAPTER 6

# SUMMARY AND CONCLUSIONS

## 6.1 SUMMARY

Conventionally, two uni-directional converters have been used to achieved bi-directional transfer of power; each processing the power for one path of the power flow. Battery charger/discharger circuits, which are an integral part of DC uninterruptible power supplies (UPS), are a typical application requiring bi-directional power transfer. The classical approach has been to use two dc-dc converters; one to charge the battery in the presence of the DC mains and the other to provide backup power to the DC bus in the absence of the mains supply. This thesis presents a bi-directional dc-dc converter topology with application in the battery charger-discharger circuit for DC UPS. that achieves both the battery charging and backup mode functions by a single converter. The bi-directional converter integrates the buck-derived half-bridge topology, for charging the battery, and the current-fed push-pull topology, for providing backup power.

The converter operation is described for both the forward/charging and backup modes. Steady state and small-signal analyses are performed for both modes. The results of the analyses are used to generate characteristic curves that provide quantitative explanation of the converter operation and an insight into its behavior. These curves can

be used for design purposes. A design example illustrates the detailed procedure to select and rate the components of the power circuit and the compensator in the feedback loop of the converter. Some qualitative aspects of the circuit implementation are also highlighted. Experimental results are used to evaluate the converter performance under steady state and transient conditions.

## 6.2 CONCLUSIONS

The proposed bi-directional dc-dc converter has been implemented and provides the desired reversible flow of power in a battery charger-discharger circuit for a DC UPS. Its topological advantages include combining two simple converter topologies in a single power processing stage, enabling its operation in either mode. This integrated unit has only one high frequency transformer that provides galvanic isolation for the low voltage battery from the high voltage supply end and the load.

The evaluation of the practical implementation shows good transient performance of the converter under load variations and during the switchover from the charging to the backup mode. The converter exhibits high steady state efficiency for both operating modes.

The proposed bi-directional converter is an industrially viable converter topology that offers substantial improvement in simplicity, efficiency, size, and component count over the conventional battery charger-discharger circuits.

## 6.3 SUGGESTIONS FOR FUTURE WORK

As an extension to the research work presented in this thesis, the following topics are suggested:

(i) Investigate the effect of soft switching on the performance and efficiency of the proposed converter topology and its possible implementation with minimal increase in circuit complexity.

(ii) Implement and achieve desired control for the switches in both modes by using one PWM chip.

(iii) Analyze the effect of starting the converter in the backup mode when the hold up capacitors on the DC bus are discharged and incorporate some form of current limiting, while maintaining converter operation.

(iv) Analyze and compare other topological combinations for possible implementation as a bi-directional converter.

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# APPENDIX A

## A.1 SMALL SIGNAL ANALYSIS FOR FORWARD MODE

The equivalent circuits in Fig. A-1 represent the two circuit states for converter operation in the forward mode. The converter operation is repetitive over half a switching time period, implying that each circuit state occurs twice in one time period.

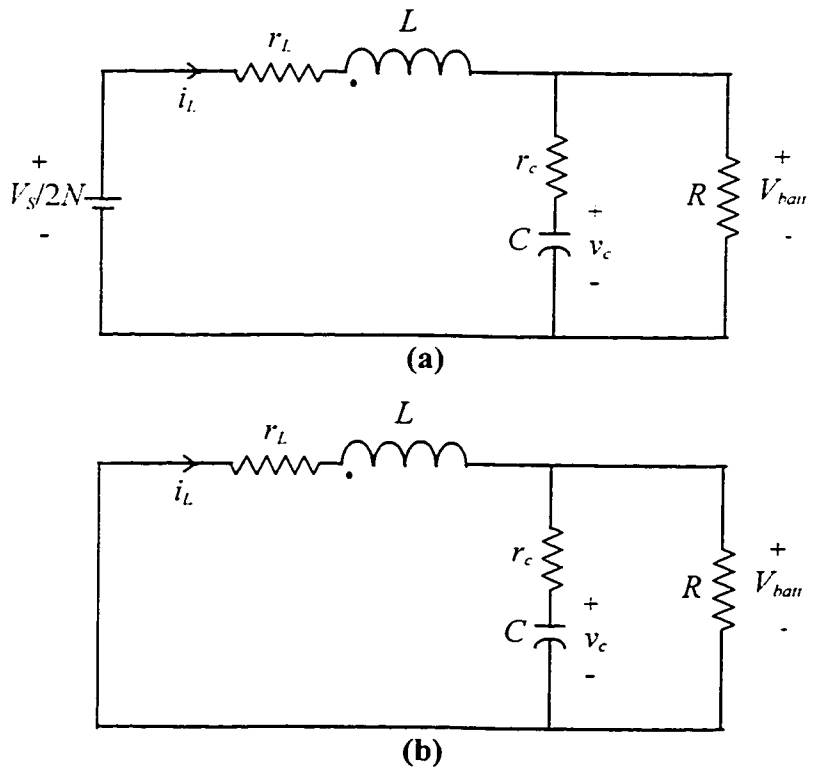


**Fig. A-1 Equivalent circuit representation for the forward mode operation.**
(a) One of the primary side switches $S_1$ or $S_2$ is ON. (b) Both the primary side switches are OFF.

Fig. A-1(a) represents the time interval when only one of the primary side switches $S_1$ or $S_2$ is in the ON state. This equivalent circuit state is valid for the time interval $d_{ss}T_{ss}$ where $d_{ss}$ is the duty ratio of the equivalent switch representing the ON state of either $S_1$ or $S_2$. Thus,

$$\left.\begin{aligned} d_{ss} &= 2 \cdot d_{fw} \\ T_{ss} &= \frac{T_s}{2} \end{aligned}\right\} \qquad \text{(A.1)}$$

$d_{fw}$ = duty ratio of each switch in the forward mode.

$T_s$ = Switching time period of the converter in the forward mode.

Fig. A-1(b) is the circuit representation of the forward mode of operation when both the switches $S_1$ and $S_2$ are in the OFF state. This equivalent circuit represents the power stage for the time interval $(1-d_{ss})T_{ss}$, where $d_{ss}$ and $T_{ss}$ are as defined above.

### A.1.1 State variable description for the circuit states

The equations describing the equivalent linear circuit in Fig. A-1(a) during the interval $d_{ss}T_{ss}$ can be written as follows:

$$\begin{aligned} \frac{di_L}{dt} &= \frac{v_S}{2LN} - \frac{i_L \cdot (r_L + r_c)}{L} - \frac{v_c}{L} \\ \frac{dv_c}{dt} &= \frac{i_L}{C} - \frac{v_c}{RC} \\ v_{batt_1} &= i_1 r_c + v_c \end{aligned} \qquad \text{(A.2)}$$

These equations can be expressed by the state space equations

$$\left.\begin{aligned} \dot{x} &= A_1 x + B_1 v_S \\ v_{batt_1} &= C_1^T x \end{aligned}\right\} \qquad \text{(A.3)}$$

where

x = state-variable vector consisting of the inductor current and the capacitor voltage.

$A_1$ = state coefficient matrix

$B_1$ = source coefficient vector

$C_1$ = output coefficient vector

From the substitution of (A.2) into the state representation in (A.3) we have the matrices for the state space equations, for the circuit state when the switches are ON.

$$x = \begin{bmatrix} i_L \\ \\ v_c \end{bmatrix} \qquad A_1 = \begin{bmatrix} -\dfrac{r_c + r_L}{L} & -\dfrac{1}{L} \\ \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \qquad B_1 = \begin{bmatrix} \dfrac{1}{2LN} \\ \\ 0 \end{bmatrix} \qquad C_1^T = \begin{bmatrix} r_c & 1 \end{bmatrix} \qquad \text{(A.4)}$$

For the interval $(1\text{-}d_{ss})T_{ss}$, with the circuit in Fig. A-1(b) representing the state when both the switches are OFF the describing equations can be written as,

$$\begin{aligned} \frac{di_L}{dt} &= -\frac{i_L \cdot (r_L + r_c)}{L} - \frac{v_c}{L} \\ \frac{dv_c}{dt} &= \frac{i_L}{C} - \frac{v_c}{RC} \\ v_{batt2} &= i_l r_c + v_c \end{aligned} \qquad \text{(A.5)}$$

The state-space equations for this state of forward mode operation are similar to those for the ON state representation.

$$\left.\begin{aligned} \dot{x} &= A_2 x + B_2 v_S \\ v_{batt_2} &= C_2^T x \end{aligned}\right\} \qquad (A.6)$$

The nomenclature for the above representation is similar to that for (A.3).

Combining (A.5) and (A.6) gives,

$$x = \begin{bmatrix} i_L \\ \\ v_c \end{bmatrix} \qquad A_2 = \begin{bmatrix} -\dfrac{r_c + r_L}{L} & -\dfrac{1}{L} \\ \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \qquad B_2 = \begin{bmatrix} 0 \\ \\ 0 \end{bmatrix} \qquad C_2^T = \begin{bmatrix} r_c & 1 \end{bmatrix} \qquad (A.7)$$

## A.1.2 Averaging the state variable equations over one time period

The two linear differential state-space equations, (A.4) and (A.7), describing the operating states of the converter in the forward mode are averaged over one equivalent switching period, $T_{ss}$. This is accomplished by summing the equations for the intervals $d_{ss}T_{ss}$ multiplied by $d_{ss}$ and the equations for $(1\text{-}d_{ss})T_{ss}$ multiplied by $(1\text{-}d_{ss})$. The resulting state-space equation is non-linear with respect to the duty ratio and describes the converter behavior with the switching frequency filtered out. It is represented by,

$$\begin{aligned} \dot{x} &= A\,x + B\,v_S \\ v_{batt} &= C\,x \end{aligned} \qquad (A.8)$$

where

$$\begin{aligned} A &= d_{ss}A_1 + (1 - d_{ss})A_2 \\ B &= d_{ss}B_1 + (1 - d_{ss})B_2 \\ C &= d_{ss}C_1^T + (1 - d_{ss})C_2^T \end{aligned} \qquad (A.9)$$

By simple matrix manipulation from (A.4), (A.7), and (A.9) we can write (A.8) as,

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_c + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{d_{ss}}{2NL} \\ 0 \end{bmatrix} \cdot v_S \qquad (A.10)$$

$$v_{batt} = \begin{bmatrix} r_c & 1 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_c \end{bmatrix}$$

### A.1.3 Linearized averaged state-space description of the forward mode

Since, techniques for linear circuit analysis and synthesis are preferred, the averaged equation (A.10) is perturbed around a DC operating point by introducing small-signal ac perturbations, represented by " ^ ", to the steady state dc quantities, represented by upper case letters. These perturbations are negligible when compared to the dc steady-state values themselves. Therefore,

$$d_{ss} = D_{ss} + \hat{d}_{ss} \qquad \mathrm{x} = \mathrm{X} + \hat{\mathrm{x}} \qquad v_S = V_S + \hat{v}_S \qquad (A.11)$$

where,

$$\frac{\hat{d}_{ss}}{D_{ss}} << 1 \qquad \frac{\hat{\mathrm{x}}}{\mathrm{X}} << 1 \qquad \frac{\hat{v}_S}{V_S} << 1 \qquad (A.12)$$

Using (A.11) in the averaged equation of (A.10) gives a state-space representation containing the steady state, the line variation, the duty cycle and the non-linear term. Using the approximation (A.12) and neglecting the non-linear (second order) terms gives a linear system containing both the ac and dc parts. Discarding the steady state (dc) terms

leaves only the dynamic (ac) terms that represent the linearized small-signal model of the system by,

$$\begin{aligned} \dot{\hat{\mathrm{x}}} &= \mathrm{A}\hat{\mathrm{x}} + \mathrm{B}\hat{v}_S + \left[(\mathrm{A}_1 - \mathrm{A}_2)\mathrm{X} + (\mathrm{B}_1 - \mathrm{B}_2)V_S\right]\hat{d}_{ss} \\ \hat{v}_{batt} &= \mathrm{C}^{\mathrm{T}}\hat{\mathrm{x}} + (\mathrm{C}_1^{\mathrm{T}} - \mathrm{C}_2^{\mathrm{T}})\,\mathrm{X}\hat{d}_{ss} \end{aligned} \tag{A.13}$$

The ac equations are transformed to the s-domain using Laplace transformation and represented by,

$$\begin{bmatrix} s\hat{i}_L(s) \\ s\hat{v}_c(s) \end{bmatrix} = \begin{bmatrix} -\dfrac{r_c + r_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_L(s) \\ \hat{v}_c(s) \end{bmatrix} + \begin{bmatrix} \dfrac{d_{ss}}{2LN} \\ 0 \end{bmatrix} \cdot \hat{v}_S(s) + \begin{bmatrix} \dfrac{V_S}{2LN} \\ 0 \end{bmatrix} \cdot \hat{d}_{ss}(s)$$

$$\hat{v}_{batt}(s) = \begin{bmatrix} r_c & 1 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_L(s) \\ \hat{v}_c(s) \end{bmatrix} \tag{A.14}$$

### A.1.4 Control constraint

The control constraint describes the effects of the current feedback loop. The perturbations in the inductor current are related to the variations in the control signal, the other states, the duty ratio and the input voltage. This control constraint relationship is derived from the waveforms at the input of the comparator in the feedback path over one switching period $T_{ss}$ shown in Fig. A-2. One comparator input carries the control voltage $v_{control}$ plus the negative stabilizing ramp of slope $-m_c$. The other input carries the inductor current with a positive slope $m_1$ and a negative slope $-m_2$.

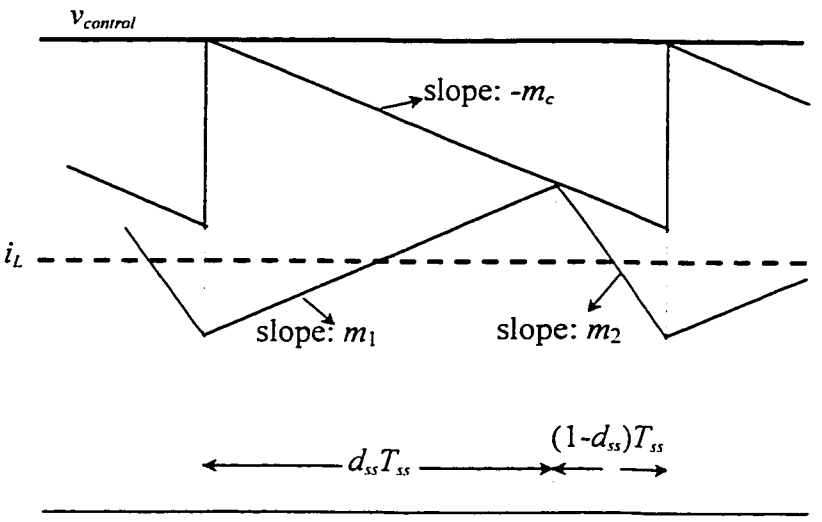


**Fig. A-2 Control constraint waveforms at the input of the comparator for the forward mode.**

The relationship between the programmed inductor current is derived from the geometry of the waveforms and is expressed by,

$$i_L + \frac{1}{2} m_1 d_{ss} T_{ss} = v_{control} - m_c d_{ss} T_{ss} \qquad \text{(A.15)}$$

As in the analysis of the power stage, perturbations are added and only the linear first order terms are retained.

$$i_L = I_L + \hat{i}_L \qquad m_1 = M_1 + \hat{m}_1 \qquad v_{control} = V_{control} + \hat{v}_{control} \qquad \text{(A.16)}$$

Because the compensating slope is constant, $m_c = M_c$.

The perturbed first order ac representation of (A.15) is,

$$\hat{i}_L + \frac{1}{2} M_1 T_{ss} \hat{d}_{ss} + \frac{1}{2} T_{ss} D_{ss} \hat{m}_1 = \hat{v}_{control} - m_c T_{ss} \hat{d}_{ss} \qquad \text{(A.17)}$$

The variables in the above expression are defined by,

$$m_1 = \frac{v_S}{2LN} - \frac{v_c}{L} - \frac{i_L(r_c + r_L)}{L},$$
$$M_1 = \frac{V_{batt}(1 - D_{ss})}{LD_{ss}} \quad \text{and} \quad \hat{m}_1 = \frac{\hat{v}_S}{2LN} - \frac{\hat{v}_c}{L} - \frac{\hat{i}_L(r_c + r_L)}{L} \tag{A.18}$$

$$m_c = nM_2 \tag{A.19}$$

where

$$\frac{M_1}{M_2} = \frac{1 - D_{ss}}{D_{ss}} \tag{A.20}$$

and $n$ is a parameter that must be specified and is expressed as the ratio of the stabilizing slope to the inductor falling slope $M_2$.

Mathematical manipulation and substitution of the information from (A.18), (A.19), and (A.20) into (A.17) gives the expression for the variation in the duty ratio, $\hat{d}_{ss}$, as a function of the variations in the states, the input voltage and the control signal as follows:

$$\hat{d}_{ss}(s) = \frac{(r_c + r_L)T_{ss} - 2L}{T_{ss}V_{batt}(D'_{ss} + 2nD_{ss})} \cdot \hat{i}_L(s) - \frac{D^2{}_{ss}}{2NV_{batt}(D'_{ss} + 2nD_{ss})} \cdot \hat{v}_S(s)$$
$$+ \frac{D^2{}_{ss}}{V_{batt}(D'_{ss} + 2nD_{ss})} \cdot \hat{v}_c(s) + \frac{2LD_{ss}}{T_{ss}V_{batt}(D'_{ss} + 2nD_{ss})} \cdot \hat{v}_{control}(s) \tag{A.21}$$

### A.1.5 Current programmed state equation

Substitution of (A.21) in the linearized state space representation (A.14) gives the current-programmed state equation. This step changes the status of the inductor current from an unknown state to a driving term and the duty ratio is no longer an independent input term. The final current programmed state space representation of the system is of the form

$$s\hat{x}(s) = A'\hat{x}(s) + B'\hat{v}_S(s) + C'\hat{v}_{control}(s), \tag{A.22}$$

where the matrices A′ , B′ and C′ are derived from the substituting of the expression for the perturbation in the duty ratio (A.21) in the state equation of the system of (A.14). The esr of the inductance has been neglected in this representation.

$$A' = \begin{bmatrix} \dfrac{r_c T_{ss}(1 - 2D_{ss} + 2nD_{ss}) - 2L}{T_{ss} L(D'_{ss} + 2nD_{ss})} & -\dfrac{(1 - 2D_{ss} + 2nD_{ss})}{L(D'_{ss} + 2nD_{ss})} \\ \dfrac{1}{C} & \dfrac{-1}{RC} \end{bmatrix} \tag{A.23}$$

$$B' = \begin{bmatrix} \dfrac{(2n-1)\,D^2{}_{ss}}{2NL(D'_{ss} + 2nD_{ss})} \\ 0 \end{bmatrix} \tag{A.24}$$

$$C' = \begin{bmatrix} \dfrac{2}{T_{ss}(D'_{ss} + 2nD_{ss})} \\ 0 \end{bmatrix} \tag{A.25}$$

### A.1.6 Control-to-output transfer function

To calculate the control-to-output transfer function, assume there is no perturbation in the input voltage and put $\hat{v}_S(s)$ equal to zero in the current-programmed state equation of (A.22). Thus the perturbations in the state vector $\hat{\mathrm{x}}$ can be determined by matrix algebra and defined by,

$$\hat{\mathrm{x}}(s) = \left[s\mathrm{I} - \mathrm{A}'\right]^{-1}\mathrm{C}'\hat{v}_{control}(s) \tag{A.26}$$

where

I = identity matrix

$s$ = Laplace operator

Since $C_1^T = C_2^T$, from (A.13) the small-signal output voltage is represented by,

$$\hat{v}_{batt}(s) = \mathrm{C}\,\hat{\mathrm{x}}(s) \tag{A.27}$$

Substituting (A.26) in the above expression gives the transfer function as,

$$\frac{\hat{v}_{batt}(s)}{\hat{v}_{control}(s)} = \mathrm{C}\,\left[s\mathrm{I} - \mathrm{A}'\right]^{-1}\mathrm{C}' \tag{A.28}$$

Substituting for the matrices and performing simple matrix algebra gives us the final representation of the control-to-output transfer function as,

$$\frac{\hat{v}_{batt}(s)}{\hat{v}_{control}(s)} = G_{vf} \cdot \frac{1 + \dfrac{s}{\omega_z}}{1 + \dfrac{s}{\omega_L/C_1} + \dfrac{s^2}{\omega_L\omega_c/C_1}} \tag{A.29}$$

The variables in the above transfer function are defined as follows:

The corner frequency for the zero, $\omega_z = \dfrac{\omega_L R}{r_c}$

The load corner frequency, $\omega_L = \dfrac{1}{(R + r_c)C}$

The current loop crossover frequency, $\omega_c = \dfrac{\omega_s}{2\pi n D'_{ss}} - \dfrac{D_{ss} - D'_{ss} n}{n L D'_{ss}}$

The switching frequency, $\omega_s = \dfrac{\pi}{T_{ss}}$

The gain factor, $G_{vf} = \dfrac{-kR}{r_s P(D_{ss} - D'_{ss} n - k)}$

The conduction parameter $k$, which is a measure of the low frequency current loop gain.

$$k = \frac{4L}{RT_s}$$

$r_s$ is the current sensing resistor

$P$ is the voltage gain factor for the sensed current

The constant $C_1 = \dfrac{r_c(D_{ss} - D'_{ss} n) - kR}{(D_{ss} - D'_{ss} n - k)R}$

## A.1.7 Line-to-output transfer function

To derive the line-to-output transfer function the variation in the control signal is zero. $\hat{v}_{control}(s) = 0$. Combining this information with (A.22) gives another expression for the perturbations in the state vector as,

$$\hat{x}(s) = \left[sI - A'\right]^{-1} B' \hat{v}_s(s) \qquad \text{(A.30)}$$

From the above equation and (A.27) the line-to-output transfer function is expressed as,

$$\frac{\hat{v}_{batt}(s)}{\hat{v}_s(s)} = \mathrm{C}\left[s\mathrm{I} - \mathrm{A}'\right]^{-1}\mathrm{B}' \tag{A.31}$$

Once again by the substitution and manipulation of the matrices in (A.31) we have,

$$\frac{\hat{v}_{batt}(s)}{\hat{v}_s(s)} = A_{g_{vf}} \cdot \frac{1 + \dfrac{s}{\omega_z}}{1 + \dfrac{s}{\omega_L/C_1} + \dfrac{s^2}{\omega_L\omega_c/C_1}} \tag{A.32}$$

The variables in the above expression have been defined above for the control-to-output transfer function.

The gain for the transfer function, $A_{g_{vf}} = \dfrac{D_{ss}(1 - D'_{ss}n)}{2N(D_{ss} - D'_{ss}n - k)}$

## A.2 SMALL SIGNAL ANALYSIS FOR THE BACKUP MODE

The converter operation in the backup mode can be represented by the two equivalent circuits shown in Fig. A-3. The primary side parameters have been reflected to the secondary side of the isolation transformer that has a ratio of secondary to primary turns equal to $N'$. As in the forward mode, the operation is repetitive over half a switching time period, $T_{ss}$. The converter operation can be described as that of a boost converter with the switch ON time equal to $d_{cf_{ss}}T_{ss}$.

Fig. A-3(a) is representative of the time interval $d_{cf_{ss}}T_{ss}$ during which both the secondary side switches $S_3$ and $S_4$ are closed. The energy is stored in the inductor and the capacitors discharge to provide the load power.

$$\left.\begin{aligned} d_{cfss} &= 2D-1 \\ T_{ss} &= \frac{T_s}{2} \end{aligned}\right\} \qquad \text{(A.33)}$$

where,

$D$ = duty ratio of each switch in the backup mode.

$T_s$ = Switching time period of the converter in the backup mode.

The equivalent circuit in Fig. A-3(b) represents the time interval when only one of the switches, $S_3$ or $S_4$, is in the ON state. This corresponds to the an equivalent boost regulator with the switch in its OFF state for a time period $(1\text{-}d_{cf_{ss}})T_{ss}$.

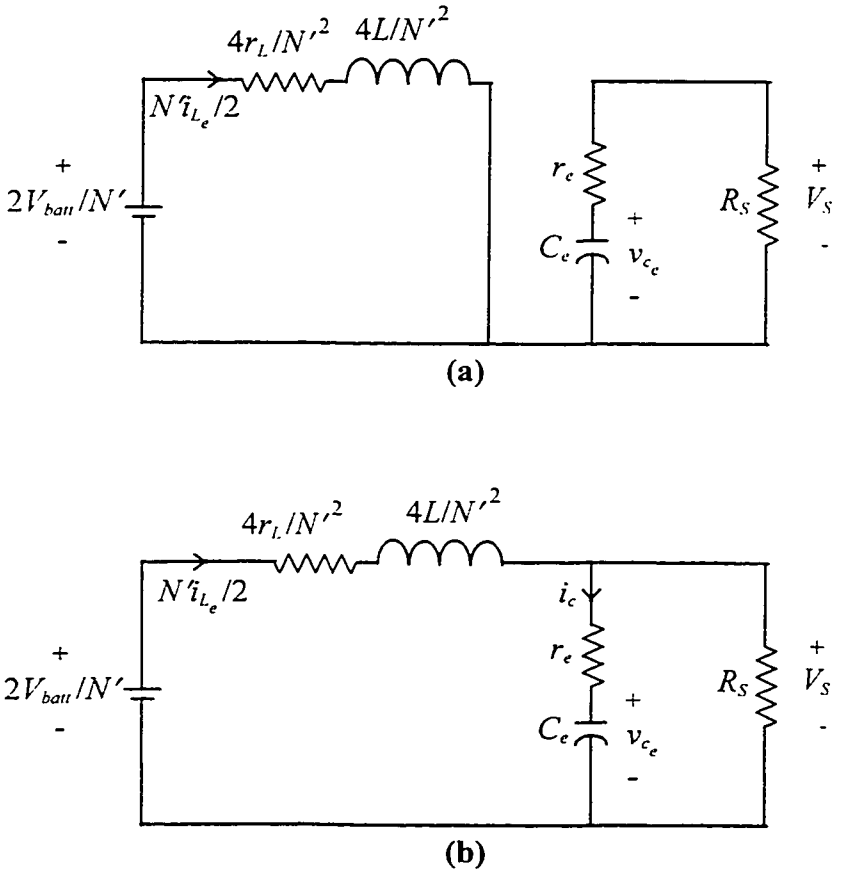


**Fig. A-3 Equivalent circuit representation for the backup mode operation.**
(a) Both the switches $S_3$ and $S_4$ are ON. (b) Only one of the switches $S_3$ or $S_4$ is ON.

### A.2.1 State variable description for the circuit states

The linear circuit of Fig. A-3(a) is representative for the time interval $d_{cf_{ss}} T_{ss}$ and can be described by the following set of equations,

$$\begin{aligned} \frac{di_{L_e}}{dt} &= \frac{v_{batt}}{L} - \frac{r_L i_{L_e}}{L} \\ \frac{dv_{c_e}}{dt} &= \frac{-v_{c_e}}{(R_S + r_e)C} \\ v_{S_1} &= \frac{v_{c_e} R_S}{R_S + r_e} \end{aligned} \tag{A.34}$$

This equivalent circuit can be expressed in the state-space representation as follows:

$$\left.\begin{aligned} \dot{x} &= a_1 x + b_1 v_{batt} \\ v_{batt_1} &= c_1^T x \end{aligned}\right\} \tag{A.35}$$

where,

x = state variable vector consisting of the inductor current and the capacitor voltage.

$a_1$ = state coefficient matrix

$b_1$ = source coefficient matrix

$c_1$ = output coefficient matrix

From (A.34) and (A.35) the matrices are determined as,

$$x = \begin{bmatrix} i_{L_e} \\ v_{c_e} \end{bmatrix} \quad a_1 = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & \frac{-1}{(R_S + r_e)C} \end{bmatrix} \quad b_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad c_1^T = \begin{bmatrix} 0 & \frac{R_S}{R_S + r_e} \end{bmatrix} \tag{A.36}$$

The expressions describing the linear circuit in Fig. A-3(b) which represents converter operation for the interval $(1\text{-}d_{cf_{ss}})T_{ss}$ are given by,

$$\begin{aligned}
\frac{di_{L_e}}{dt} &= \frac{v_{batt}}{L} - \frac{i_{L_e}}{L}\left(r_L + \frac{r_L r_e N'^2}{(R_S + r_e)4}\right) - \frac{N'R_S v_{c_e}}{2L(R_S + r_e)} \\
\frac{dv_{c_e}}{dt} &= \frac{R_S N' i_{L_e}}{2C_e(R_S + r_e)} - \frac{v_{c_e}}{(R_S + r_e)C_e} \\
v_{s_1} &= \frac{R_S v_{c_e}}{(R_S + r_e)} + \frac{N'R_S r_e i_{L_e}}{2(R_S + r_e)}
\end{aligned} \tag{A.37}$$

Once again the state space representation describing this circuit state is given by,

$$\left.\begin{aligned}
\dot{x} &= a_2 x + b_2 v_{batt} \\
v_{batt_1} &= c_2^T x
\end{aligned}\right\} \tag{A.38}$$

where the matrices $a_2$, $b_2$ and $c_2$ are as defined above and are expressed as.

$$x = \begin{bmatrix} i_{L_e} \\ \\ v_{c_e} \end{bmatrix} \qquad a_2 = \begin{bmatrix} -\frac{1}{L}\left(r_L + \frac{r_L r_e N'^2}{(R_S + r_e)4}\right) & -\frac{N'R_S}{2L(R_S + r_e)} \\ \frac{R_S N'}{2C_e(R_S + r_e)} & -\frac{1}{(R_S + r_e)C_e} \end{bmatrix} \tag{A.39}$$

$$b_2 = \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} \qquad c_2^T = \begin{bmatrix} \frac{N'R_S r_e}{2(R_S + r_e)} & \frac{R_S}{(R_S + r_e)} \end{bmatrix}$$

### A.2.2 Averaging the state variable equations over one time period

The averaged state-space equations describing the converter behavior over one switching time period is expressed as,

$$\begin{aligned} \dot{x} &= a\,x + b\,v_{batt} \\ v_S &= c\,x \end{aligned} \tag{A.40}$$

where,

$$\begin{aligned} a &= d_{cf_{ss}} a_1 + (1 - d_{cf_{ss}}) a_2 \\ b &= d_{cf_{ss}} b_1 + (1 - d_{cf_{ss}}) b_2 \\ c &= d_{cf_{ss}} c_1^T + (1 - d_{cf_{ss}}) c_2^T \end{aligned} \tag{A.41}$$

Neglecting the esr of the inductance and approximating terms that contain $R_S$ and $r_c$ to only $R_S$, as $R_S >> r_c$, from (A.36), (A.39) and (A.41) the averaged state-space representation of the converter (A.40) can be expressed as,

$$\begin{bmatrix} \frac{di_{L_e}}{dt} \\ \frac{dv_{c_e}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_e N'^2 d'_{cf_{ss}}}{4L} & -\frac{N' d'_{cf_{ss}}}{2L} \\ \frac{N' d'_{cf_{ss}}}{2C_e} & -\frac{1}{R_S C_e} \end{bmatrix} \cdot \begin{bmatrix} i_{L_e} \\ v_{c_e} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{batt}$$

$$v_S = \begin{bmatrix} \frac{N' r_e d'_{cf_{ss}}}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{L_e} \\ v_{c_e} \end{bmatrix} \tag{A.42}$$

### A.2.3 Linearized averaged state-space description of the backup mode

The variables in the averaged states-space equation of (A.42) are represented by steady state (dc) quantities that have dynamic (ac) perturbations superimposed on them. The dc

quantities, describing an operating point of the converter, are denoted by upper case alphabets and the ac perturbations added to them are denoted by lower case alphabets with the symbol " ^ ". Therefore,

$$d_{cfss} = D_{cfss} + \hat{d}_{cfss} \qquad \mathrm{x} = \mathrm{X} + \hat{\mathrm{x}} \qquad v_{batt} = V_{batt} + \hat{v}_{batt} \tag{A.43}$$

The perturbations are negligible when compared to the steady state quantities, thus

$$\frac{\hat{d}_{cf_{ss}}}{D_{cf_{ss}}} << 1 \qquad \frac{\hat{\mathrm{x}}}{\mathrm{X}} << 1 \qquad \frac{\hat{v}_{batt}}{V_{batt}} << 1 \tag{A.44}$$

Substitution of (A.43) in (A.42) gives the state-space representation of the converter. Applying the approximation (A.44) in this representation and retaining only the ac terms while neglecting the non-linear second order terms gives the linearized small-signal model of the converter that is expressed as,

$$\begin{aligned} \dot{\hat{\mathrm{x}}} &= \mathrm{a}\hat{\mathrm{x}} + \mathrm{b}\hat{v}_{batt} + \left[(\mathrm{a}_1 - \mathrm{a}_2)\mathrm{X} + (\mathrm{b}_1 - \mathrm{b}_2)V_{batt}\right]\hat{d}_{cfss} \\ \hat{v}_S &= \mathrm{c}^{\mathrm{T}}\hat{\mathrm{x}} + (\mathrm{c}_1^{\mathrm{T}} - \mathrm{c}_2^{\mathrm{T}})\,\mathrm{X}\hat{d}_{cf_{ss}} \end{aligned} \tag{A.45}$$

Transforming (A.45) to express it in terms of Laplace transforms from which the transfer functions are derived gives,

$$\begin{bmatrix} s\hat{i}_{L_e}(s) \\ s\hat{v}_{c_e}(s) \end{bmatrix} = \begin{bmatrix} \dfrac{-r_e N'^2 d'_{cfss}}{4L} & \dfrac{-N' d'_{cfss}}{2L} \\ \dfrac{N' d'_{cfss}}{2C_e} & -\dfrac{1}{R_S C_e} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{L_e}(s) \\ \hat{v}_{c_e}(s) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \cdot \hat{v}_{batt}(s) + \begin{bmatrix} \dfrac{V_S N'}{2L} \\ \dfrac{V_S}{R_S C_e d'_{cfss}} \end{bmatrix} \cdot \hat{d}_{cfss}(s) \tag{A.46}$$

$$\hat{v}_S(s) = \begin{bmatrix} \dfrac{r_e N' d'_{cf_{ss}}}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{L_e}(s) \\ \hat{v}_{c_e}(s) \end{bmatrix} - \frac{r_e V_S}{d'_{cf_{ss}} R_S} \cdot \hat{d}_{cf_{ss}}(s)$$

### A.2.4 Control constraint

The control constraint determines the relationship between the programmed inductor current and the control signal. This constraint is derived from the waveforms at the input of the comparator, Fig. A-4, which finally provides the input to the error amplifier in the feedback loop. One comparator input carries the control voltage, defined by $e$, plus the stabilizing ramp, the slope of the stabilizing ramp is $-m_c$. The other input carries the voltage signal representing the inductor current that has a positive slope $m_a$ and a negative slope $-m_b$. From the geometry of the waveforms the desired relationship is expressed as,

$$i_{L_e} + \frac{1}{2} m_a d_{cfss} T_{ss} = e - m_c d_{cfss} T_{ss} \tag{A.47}$$

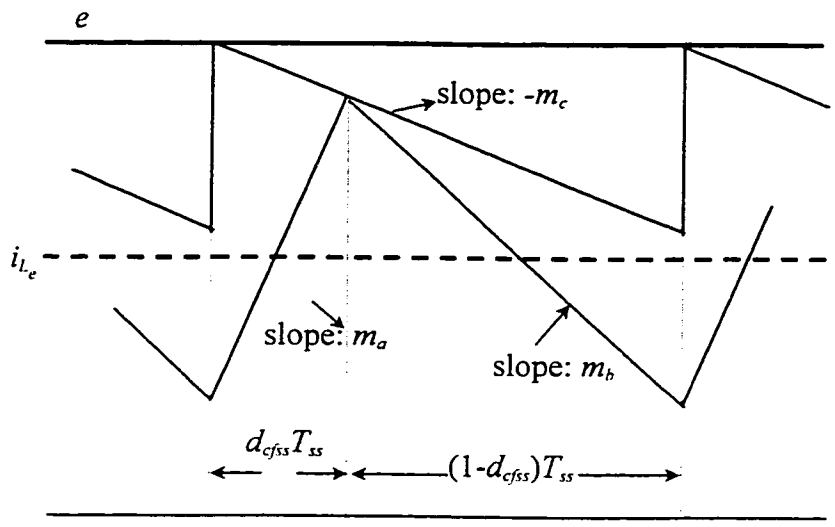


**Fig. A-4 Control constraint waveforms at the input of the comparator in the backup mode.**

Following a procedure similar to that in the forward mode, the variables in the control relationship of (A.47) are expressing them as dc quantities with added ac perturbations.

$$i_{L_e} = I_{L_e} + \hat{i}_{L_e} \qquad m_a = M_a + \hat{m}_a \qquad e = E + \hat{e} \tag{A.48}$$

and only the linear first order terms of the representing the ac model are retained.

$$\hat{i}_{L_e} + \frac{1}{2} M_a T_{ss} \hat{d}_{cf_{ss}} + \frac{1}{2} T_{ss} D_{cf_{ss}} \hat{m}_a = \hat{e} - m_c T_{ss} \hat{d}_{cf_{ss}} \tag{A.49}$$

In the expression above,

$$m_a = \frac{v_{batt}}{L}, \qquad M_a = \frac{V_S N' D'_{cf_{ss}}}{2L}, \text{and} \qquad \hat{m}_a = \frac{\hat{v}_{batt}}{L} \tag{A.50}$$

$$m_c = nM_b \tag{A.51}$$

where,

$$\frac{M_a}{M_b} = \frac{D'_{cf_{ss}}}{D_{cf_{ss}}} \tag{A.52}$$

and, $n$ is the ratio of the compensating slope to the inductor falling slope and must be numerically specified.

The perturbation in the duty ratio is expressed as a function of the perturbations in the input voltage, the control signal and the states of the system by the substitution of (A.50), (A.51), and (A.52) in (A.49).

$$\hat{d}_{cf_{ss}}(s) = \left[\frac{4L}{T_{ss}} \cdot \hat{e}(s) - \frac{4L}{T_{ss}} \cdot \hat{i}_{L_e}(s) - 2D_{cf_{ss}}\hat{v}_{batt}\right] \cdot \frac{1}{V_S N'(D'_{cf_{ss}} + 2nD_{cf_{ss}})} \tag{A.53}$$

## A.2.5 Current programmed state equation

In the current programmed state equation, the inner current loop is absorbed into the forward path of the power stage and only the outer voltage is evident. This is obvious from the fact that the inductor current is now a driving terms and the duty ratio is not an independent input. This is achieved by the substitution of the expression for the duty ratio perturbations (A.53) in the state space representation of the system (A.46). The state-space representation of the current-programmed equation is given by,

$$s\hat{\mathrm{x}}(s) = \mathrm{a}'\hat{\mathrm{x}}(s) + \mathrm{b}'\hat{v}_{batt}(s) + \mathrm{c}'\hat{e}(s) \tag{A.54}$$

where the matrices are defined as,

$$\mathrm{a}' = \begin{bmatrix} \dfrac{-r_e N' D'_{cf_{ss}}}{4L} - \dfrac{2}{T_{ss}(D'_{cf_{ss}} - 2nD_{cf_{ss}})} & \dfrac{-N'D'_{cf_{ss}}}{2L} \\ \dfrac{N'D'_{cf_{ss}}}{2L} + \dfrac{4L}{R_S C_e D'_{cf_{ss}} T_{ss} N'(D'_{cf_{ss}} + 2nD_{cf_{ss}})} & \dfrac{-1}{R_S C_e} \end{bmatrix} \tag{A.55}$$

$$b' = \begin{bmatrix} \dfrac{D'_{cf_{ss}} + D_{cf_{ss}}(2n-1)}{L(D'_{cf_{ss}} + 2nD_{cf_{ss}})} \\ \dfrac{2D_{cf_{ss}}}{R_S C_e D'_{cf_{ss}} N'(D'_{cf_{ss}} + 2nD_{cf_{ss}})} \end{bmatrix} \tag{A.56}$$

$$c' = \begin{bmatrix} \dfrac{2}{T_{ss} D'_{cf_{ss}} + 2nD_{cf_{ss}}} \\ \dfrac{-4L}{R_S C_e D'_{cf_{ss}} N'(D'_{cf_{ss}} + 2nD_{cf_{ss}})} \end{bmatrix} \tag{A.57}$$

### A.2.6 Control-to-output transfer function

The control-to-output transfer function is derived and plotted to give information on the crossover frequency, the corner frequencies for the poles and zeros and the system gain. The transfer function can be derived by assuming there are no perturbations in the input voltage, mathematically meaning $\hat{v}_{batt}(s) = 0$. Using this in the current programmed state space representation of the system (A.54) gives the matrix solution for the perturbation in the states,

$$\hat{x}(s) = [sI - a']^{-1} c' \hat{e}(s) \tag{A.58}$$

From the above equation and the averaged state space representation (A.45) we derive the transfer function. To avoid lengthy calculations with minimal inaccuracy in the end result the effect of the term $(c_1^T - c_2^T)$ in (A.45) has neglected. The transfer function can easily be represented by,

$$\frac{\hat{v}_S(s)}{\hat{e}(s)} = \mathrm{c}\,\left[s\mathrm{I} - \mathrm{a}'\right]^{-1}\mathrm{c}' \tag{A.59}$$

where c is the matrix defined in(A.42), a′ is the matrix defined in (A.55) and c′ has been defined in (A.57). Solving (A.59) with the substitution of the matrices gives the final control-to-output transfer function expressed as,

$$\frac{\hat{v}_s(s)}{\hat{e}(s)} = G_{cf} \cdot \frac{1 - \dfrac{s}{\omega_{z_2}}}{1 + \dfrac{s}{\omega_{L_{cf}}/C_a} + \dfrac{s^2}{\omega_{L_{cf}}\omega_{c_{cf}}/C_a}} \tag{A.60}$$

where,

The corner frequency for the right half plane (rhp) zero, $\omega_{z_2} = \dfrac{2N'D'_{cf_{ss}}(R_S D'_{cf_{ss}} N' - r_e)}{2L + R_S D'_{cf_{ss}} N' r_e}$.

The load corner frequency, $\omega_{L_{cf}} = \dfrac{2}{(R_S + r_e)C_e}$.

The current loop crossover frequency, $\omega_{c_{cf}} = \dfrac{2\omega_s}{\pi n D'_{cf_{ss}}}$.

The switching frequency, $\omega_s = \dfrac{\pi}{T_{ss}}$.

The gain factor, $G_{cf} = \dfrac{4k(RD'_{cf_{ss}} N' - 2r_e)}{(D'^3_{cf_{ss}} N'^2 n + 16k)pr_{sense}}$.

$r_{sense}$ is the current sense resistor and $p$ is the voltage factor for the sensed current.

The conduction parameter, $k = \dfrac{L}{R_S T_{ss}}$.

The constant, $C_a = \dfrac{8kR_S + r_e nD'^2_{cf_{ss}} N'^2}{R_S(16k + nD'^3_{cf_{ss}} N'^2)}$.

### A.2.7 Line-to-output transfer function

The line-to-output transfer function, also called the audio susceptibility, is the variation in the output voltage due to perturbations in the input voltage. This transfer function is derived by a procedure similar to that for the control-to-output transfer function.

The variation in the control signal, $\hat{e}$, is assumed to be zero, i.e. $\hat{e} = 0$. Therefore, the current programmed state-space representation (A.54) can now be expressed as,

$$\hat{\mathrm{x}}(s) = \left[s\mathrm{I} - \mathrm{a}'\right]^{-1} \mathrm{b}' \hat{v}_{batt}(s) \tag{A.61}$$

Using this expression with (A.45) while neglecting the term $(\mathrm{c}_1^{\mathrm{T}} - \mathrm{c}_2^{\mathrm{T}})$ as earlier with little inaccuracy in the end result, the line-to-output transfer function is represented by,

$$\frac{\hat{v}_s(s)}{\hat{v}_{batt}(s)} = \mathrm{c}\left[s\mathrm{I} - \mathrm{a}'\right]^{-1} \mathrm{b}' \tag{A.62}$$

Substitution of the defined matrices gives the line-to-output transfer function as,

$$\frac{\hat{v}_s(s)}{\hat{v}_{batt}(s)} = A_{g_{cf}} \cdot \frac{1 + \dfrac{s}{\omega_{z_1}}}{1 + \dfrac{s}{\omega_{L_{cf}}/C_b} + \dfrac{s^2}{\omega_{L_{cf}}\omega_{c_{cf}}/C_b}} \tag{A.63}$$

where,

The gain factor, $A_{g_{cf}} = \dfrac{16kR_S + 2D'_{cf_{ss}}N'^2[2r_eD^2{}_{cf_{ss}} + D'_{cf_{ss}}(nD'_{cf_{ss}} - D_{cf_{ss}})]}{R_SD'_{cf_{ss}}N'(16k + nD'^3_{cf_{ss}}N'^2)}$.

The corner frequency for the zero,

$$\omega_{z_1} = R_S \frac{2kT_{ss}D_{cf_{ss}} - r_eC_eD'^2_{cf_{ss}}N'^2(D_{cf_{ss}} - D'_{cf_{ss}}n)}{4kR_S + D'_{cf_{ss}}N'^2[2r_eD^2{}_{cf_{ss}} + D'_{cf_{ss}}R_S(nD'_{cf_{ss}} - D_{cf_{ss}})]}.$$

The constant, $C_a = \dfrac{4kR_S + r_enD'^2_{cf_{ss}}N'^2}{R_S(8k + nD'^3_{cf_{ss}}N'^2)}$.