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VOLTAGE CONTROLLED PULSE WIDTH MODULATION PATTERN GENERATORS FOR STATIC POWER CONVERTERS

Manish Pande

A Thesis

in

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ABSTRACT

VOLTAGE CONTROLLED PULSE WIDTH MODULATION PATTERN GENERATORS FOR STATIC POWER CONVERTERS

Manish Pande

Many static power converter systems use uncontrolled diode rectifier bridges at the front end. Due to rectification, the resulting dc link voltage contains characteristic as well as uncharacteristic harmonics. In addition switching devices in a converter system have conduction voltage drops and finite turn-on and turn-off delays. These factors are found to degrade the overall performance of the converter system.

The objective of this research is to investigate the principle of converter output voltage integral duty cycle control. Two schemes, Reset Integral Control (RIC) and Mqdulated Integral Control (MIC) are derived and used in on-line PWM pattern generators for dc-dc and dc-ac converters. The switching pattern generated is a function of the non-ideal conditions. Thus a better performance with almost the same complexity as the conventional pattern generators is achieved. Performance features are illustrated through computer simulation case studies. Experimental results on a laboratory prototype confirm the feasibility of the proposed pattern generators.

ACKNOWLEDGEMENTS

I wish to express my gratitude to Dr. H. Jin and Dr. G. Joos for their valuable advice and support during the course of this research work.

I would like to thank all my research colleagues in Power Electronics Lab for their encouragement and help.

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OVI	output voltage integral
RIC	reset integral control
MIC	modulated integral control
EPROM	erasable programmable read only memory
PWM	pulse width modulation
SPWM	sine pulse width modulation
VSI	voltage source inverter
A/D	analog to digital
D/A	digital to analog
GTO	gate turn off thyristor
BJT	bipolar junction transistor
MOSFET	metal oxide field effect transistor
IGBT	insulated gate bipolar transistor
CC	compensation circuit
PG	pattern generator
PECAN	power electronic analyis program
kW	unit of real power
kVA	unit of apparent power

LIST OF PRINCIPAL SYMBOLS

C	dc link filter capacitor
L	dc link filter inductor
C_f	output filter capacitor in dc-dc converter
L_f	output filter inductor in dc-dc converter
R_o	load resistance in dc-dc converter
R_l	load resistance in dc-ac converter
L_l	load inductance in dc-ac converter
f_{sw}	switching frequency
T_{sw}	switching period
f_i	input ac line frequency
f_o	inverter fundamental frequency
D	duty cycle of a dc-dc converter
D_{max}	maximum duty cycle
V_d	dc link voltage
V_{dc}	mean dc link voltage
f_r	dominant ripple frequency
k_r	dc bus ripple factor
V_{o1}	output voltage of dc-dc converter without switching delay
V_{o2}	output voltage of dc-dc converter with switching delay
ΔV	equivalent dead time voltage
M_n	number of switchings per cycle
t_Δ	dead time interval
V_{AN}	voltage across the bottom switch in a half bridge inverter
i_A	phase current in a half bridge inverter

V_c	carrier waveform
V_m	modulating waveform
SW_{ll}	line switching function
Δt	sampling interval
t	time
t_{on}	on time of the switch
t_{off}	off time of the switch
S_1	area under the reference voltage
S_2	area under output voltage pulse
V_{int}	integrator output
V_{ref}	reference voltage
V_{os}	output voltage of a dc-dc converter
V_o	load voltage of a dc-dc converter
I_l	inductor current
k_s	sensor gain
V_{carr}	triangular carrier
τ	integrator time constant
τ_{min}	minimum integrator time constant
$V_{ref,max}$	maximum reference voltage
P_o	output power
R_i	% maximum current ripple
R_v	% maximum voltage ripple
$f(t)$	switching function
K_h	harmonic attenuation factor
m_r	rising slope of the modulating waveform
m_f	falling slope of the modulation waveform
m_c	slope of the carrier waveform

$V_{con,Q1}$	conduction drop of switch Q1
V_{bias}	dc bias voltage
V_{refa}	reference voltage for Phase A.
V_{refb}	reference voltage for Phase B.
V_{refc}	reference voltage for Phase C.
M	modulation index
M_{max}	maximum modulation index
THD_i	Total harmonic distortion in the line current
THD_{lv}	Low order harmonic distortion in the line voltage
$V_{LL1(rms)}$	fundamental line rms voltage
k_{ac}	voltage gain
$k_{ac,ideal}$	voltage gain at unity modulation index
e_{AN}	error voltage
$f_k(t)$	switching function of the k^{th} pulse
$C(n,k)$	Fourier coefficient
$\theta_{on,k}$	pulse width in the k^{th} interval in radians
f_a	switching function for phase A
f_b	switching function for phase B
f_{ab}	line switching function

CHAPTER 1

INTRODUCTION

1.1. Introduction

Power Electronics[1][2][3] is associated with conversion and control of electrical power at high efficiencies and has found widespread use in industrial, commercial, residential, military and aerospace applications. A modern power electronic equipment, referred to as a Static Power Converter (because it contains no moving parts), comprises of power semiconductor devices that handle the electrical power under the guidance of control signals obtained from electronic chips.

In many application a dc input voltage is required for a converter. Static power converters of this type can be classified in two categories:

- dc to dc converter (chopper). It converts unregulated dc voltage to regulated dc voltage at different levels[4]. PWM dc-dc converters are being widely used in switch mode dc power supplies[5] and in motor drive applications[6].
- dc to ac converter (inverter). It can be either voltage fed or current fed and generates a variable magnitude, variable frequency ac output. PWM inverters provide linear control of output fundamental voltage and frequency and are being widely used in ac motor drive control[7][8], UPS systems and induction heating.

This thesis focuses on improving the performance of dc to dc and dc to ac converters by proposing voltage controlled PWM pattern generators. A generalized converter system is shown in Fig. 1.1.

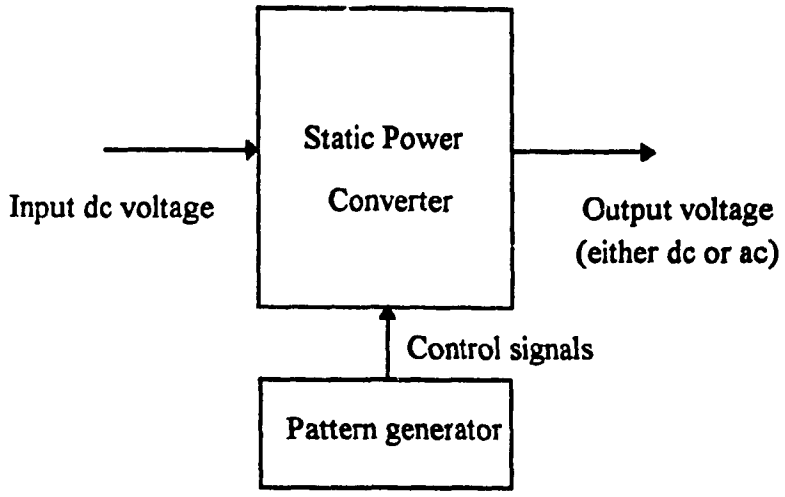


Fig. 1.1. A typical dc-dc or dc-ac power electronic converter system

1.2. Problem definition

The dc input to most PWM converters is obtained by rectifying three phase ac line voltage with the help of a three phase diode bridge and is shown in Fig 1.2. A front end diode rectifier is preferred because it is rugged in nature, requires no external control and thereby reduces the cost in low and medium power applications and wherever regeneration capability is not desired.

A second order dc link filter comprising of passive elements like inductors and capacitors is used to attenuate the harmonics inherent in rectification. It is assumed that a well designed filter can establish a fixed, ripple free dc link voltage. This is the input to the power converter which is transformed into the required form.

It is also assumed that the semiconductor devices in the power converter configuration are ideal, i.e., they switch on or off at the precise instants the control signal dictates them to.

In a practical system these conditions are not always satisfied. Conventional PWM pattern generators in [9][10][11][12][13][14] overlook this fact while analyzing power

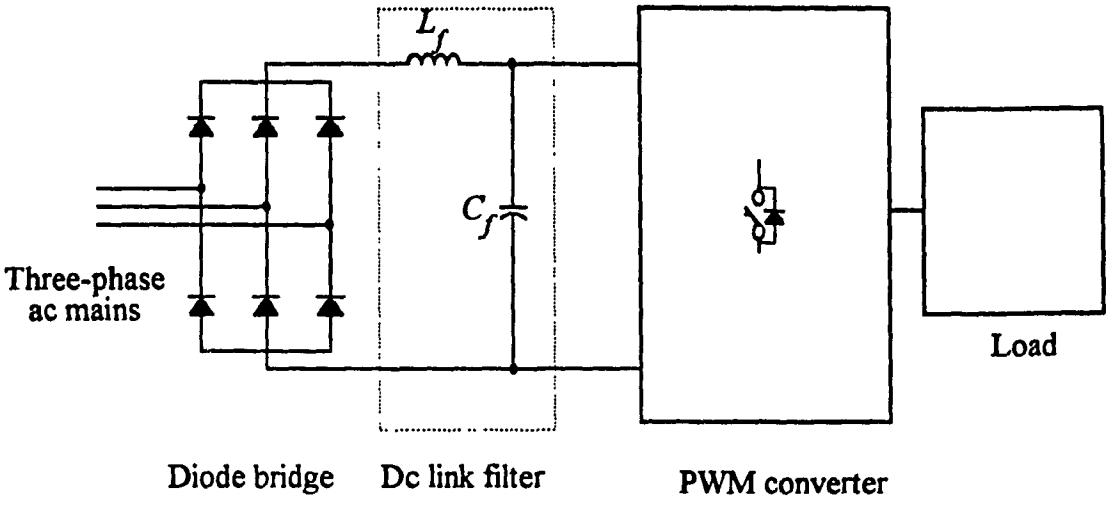


Fig. 1.2. A PWM converter (dc/dc or dc/ac) with a front-end diode rectifier

converters. Thus the performance of such converters is degraded and the quality of the output voltage is not as high as that predicted in [15][16][17][18].

Subsequent sections point as to why these assumptions are not valid and should not be ignored in analysis. A prior knowledge can result in a better and reliable design.

1.2.1 Ripple in dc link voltage

In a practical converter system, dc link voltage cannot be assumed to be ripple free. This section discusses the cause of the ripple and its impact on the performance of PWM converters.

1.2.1.1. Cause of ripple

The notion of a ripple free dc link voltage is based on the filtering capability of a dc link filter. For a good performance the break frequency of the filter is chosen to be almost a decade below the expected lowest dominant harmonic inherent in rectification. As has been discussed in [19], the dc link voltage created with an uncontrolled front end diode bridge has characteristic harmonics of the order of $6nf_i, f_i$ being the input line frequency.

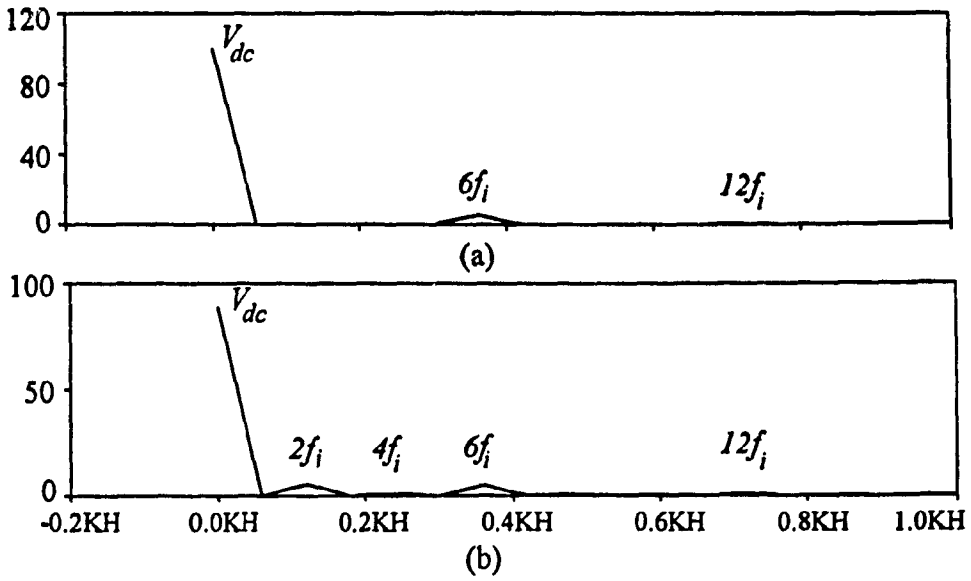


Fig. 1.3. DC bus spectrum. (without an input filter) (a) Balanced input supply. (b) Unbalanced input supply (f_i : ac supply frequency)

Furthermore an unbalance in ac input supply results in additional harmonics of the order of $2nf_i$. This is illustrated in the DC bus harmonic spectra of Fig. 1.3. For an ac line frequency of 60 Hz (1 pu), the dominant characteristic harmonics are the 120 Hz (2 pu) and 360 Hz (6 pu). Also unbalanced and non-linear loads result in waveforms distortions, leading to pollution of dc link with uncharacteristic harmonics.

Thus to obtain a ripple free dc link voltage, a filter with a break frequency that can reduce the low frequency harmonics will result in large values of L and C. This leads to a bulky dc link filter which increases the size of converter, slows the response of the system and reduces the overall efficiency. This is illustrated by designing the break frequency of the filter to be at 12 Hz. Choose C=10000μF. The value of L calculated, is 211 mH, which is very large and impractical. Thus a compromise has to be reached between the size of the filter components and the overall effectiveness of the filter.

It is therefore very difficult to design an input filter which could provide adequate filtering to harmonics present in the dc link voltage and yet have a reasonable size. Thus in a converter system, dc link voltage ripple cannot be ignored in the analysis.

1.2.1.2. Impact of low frequency ripple on converter performance

As discussed in the previous section, there is a substantial low-frequency voltage ripple on the dc link and cannot be neglected in the harmonic analysis of PWM converters. A qualitative analysis can be provided by assuming the ripple to be of a single dominant frequency, f_r.

The ripple in the dc link is the main cause of appearance of harmonics in the converter output not present in the PWM switching function. This increases the harmonic distortion in the output voltage and is hence undesirable.

In PWM dc-dc converters, the output filter is designed to attenuate switching harmonics and for a good performance the cut-off frequency is chosen to be a decade below the operating frequency(f_{sw}). Since the dc-dc converters are usually operated in the range of 10 kHz and greater, the cut off frequency is much greater than the ripple frequency. Therefore there is virtually no attenuation to the ripple frequency which appears in the output dc voltage deteriorating the quality of the output voltage. This is illustrated in the harmonic spectrum of the output voltage of a dc-dc converter working with a non-ideal dc bus (Fig. 1.4). The ripple frequency which is 360 Hz, appears in the output and increases the distortion in the output voltage.

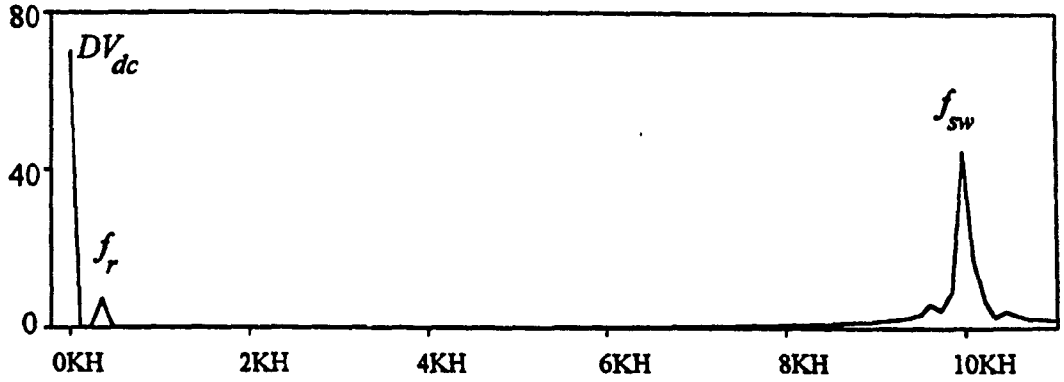


Fig. 1.4. Output voltage spectrum of a dc-dc converter working under non-ideal dc bus. (f_{SW}=10 kHz, D=0.7, f_r=360 Hz)

In PWM dc-ac converters, operating at a fundamental frequency of f_O, ripple in the dc bus causes low order harmonics at $(f_r \pm f_O)$ to appear in the inverter output. These harmonics are difficult to filter and increase the harmonic distortion. These can become an issue in motor drive applications in which the inverter frequency is varied over a range and the subharmonics in inverter output can degrade the performance of the drive system. The effect of a typical inverter operating frequency (60Hz) on the harmonic content of the output voltage has been summarized in Table I.

TABLE I

EFFECT OF DC BUS RIPPLE ON INVERTER OUTPUT

Inverter output frequency(Hz)	DC bus ripple frequency(Hz)	Low order harmonics in inverter output(Hz)	
f_o	f_r	f_r-f_o	f_r+f_o
60	120	60	180
60	360	300	420

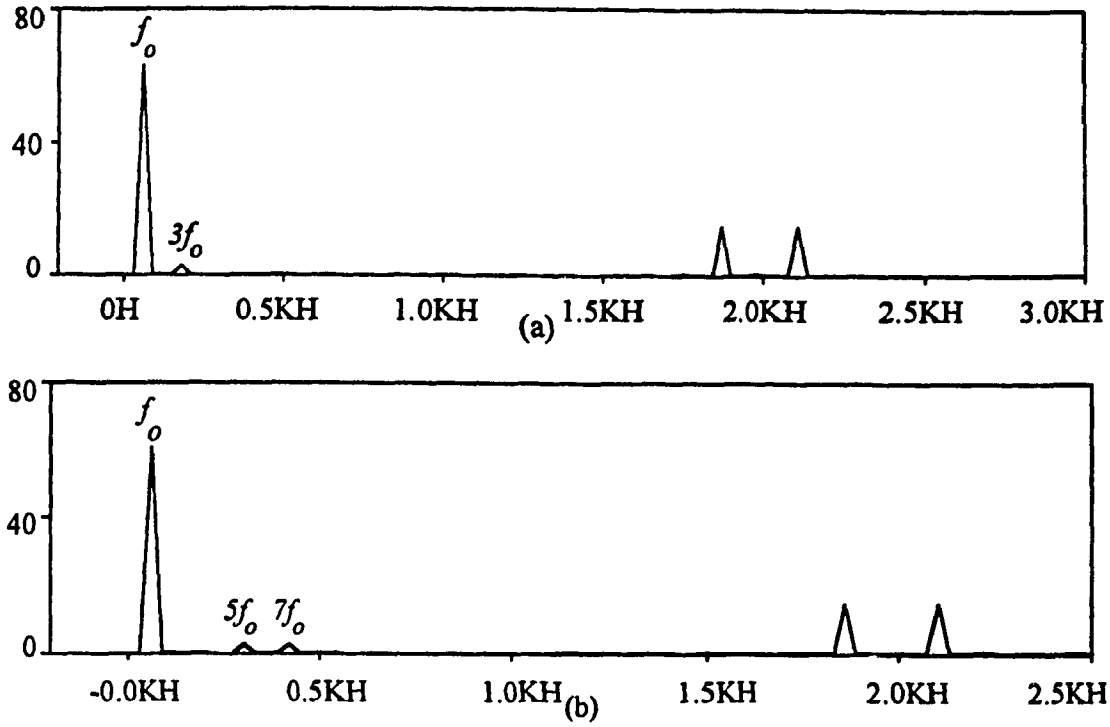


Fig. 1.5. Output voltage spectra of a dc-ac converter working under non-ideal dc bus. (a) f_r=120 Hz (b) f_r=360 Hz.

For a inverter operating at a fundamental frequency of 60 Hz (1 pu) and subject to f_r=2 pu, the low order harmonic is 3 pu (Fig. 1.5(a)). With dominant ripple frequency f_r= 6 pu, the low order harmonics in the line voltage are 5 pu and 7 pu (Fig. 1.5(b)).

1.2.2. Non-ideal power semiconductor devices

A power semiconductor device is assumed to provide processing of electrical power under ideal switching action i.e. with zero switching delays and conduction drops. However, a practical switching device takes a finite amount of time to turn-on and turn off, resulting in switching delays. Also any power device while conducting has a finite on-state resistance resulting in switch conduction drops.

An excellent review of the state-of-the-art devices and their characteristics in [20][21][22], reveals the non-ideal nature of semiconductor devices. Table II summarizes

a few important characteristics often neglected in conventional pattern generators and addressed in this thesis. The values specified are at rated current and voltage levels for typical commercially available devices.

TABLE II [20][21][22]

PROPERTIES OF SWITCHING DEVICES

Characteristics	Thyristor	Triac	GTO	Darlington BJT	MOSFET	IGBT
Conduction drop(V) at rated current	1.9	1.4	4	1.9	3.2	3.2
Turn on time (μs)	1.1	1.7	4	1.7	0.09	0.9
Turn off time (μs)	220	200	10	5	0.14	1.4

It can be inferred from Table II that a practical power conductor device has finite turn-on and turn-off times and conduction losses. Thus at high power, the output voltage (dc voltage in dc/dc converters and fundamental ac voltage in dc/ac converters) shows a considerable deviation from the desired value. Also in single/three phase voltage source inverters, finite turn-off times may cause a short circuit of the dc link at the instant of switch over. Thus dead times [23][24], have to be introduced in the gating signal to avoid shorting of dc link. Introducing dead times is detrimental to the performance of the voltage source inverters. These aspects are discussed in following sections.

1.2.2.1. Effect of switching delay in DC/DC PWM converters

The effect of finite switching delays on the performance of dc-dc converters can be analyzed with respect to Fig. 1.6. As seen the switch turns-off after a certain time delay from the instant it was commanded by the desired gating signal. This results in extra volt seconds at the output of the converter which increases the mean dc voltage(V_{o2}) when the desired output is V_{o1}. This performance is undesirable and can be of significant concern when the device has a greater turn-off time.

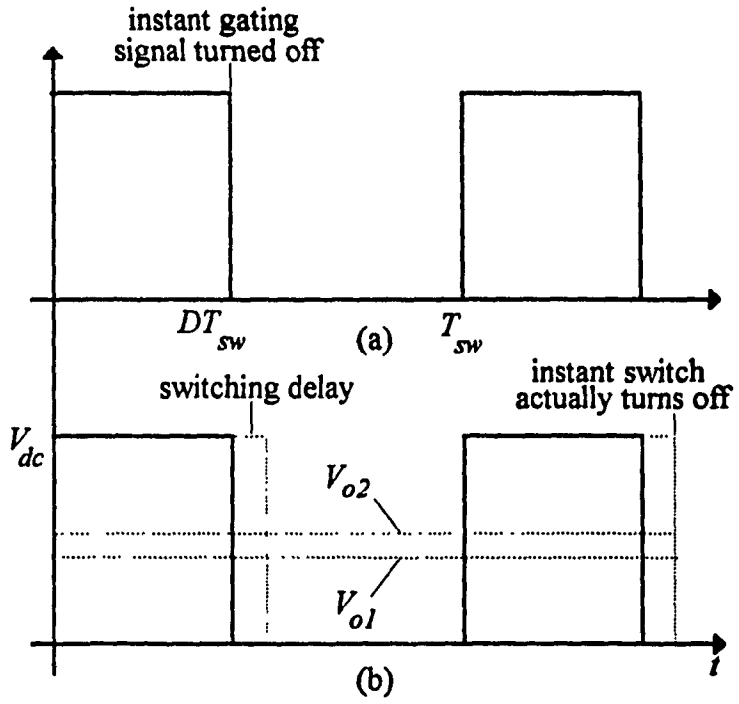


Fig. 1.6. Effect of switching delay in dc-dc converters. (a) Ideal gating signal for the power switch. (b) Output voltage with and without switching delay.

1.2.2.2. Effect of dead times on output voltage in PWM inverters

As discussed in section 1.2.2, because of the finite turn-off and turn-on times associated with a switching device, dead times have to be introduced in the gating signals of a voltage source inverter to prevent short circuit of the dc link. Introducing time delays

guarantees safe operation of the converter. A switch is turned off at the predefined switching instant. However the turn-on of the switch in the same inverter leg is delayed by dead time t_{Δ}, which is typically 10-20 μsec.

Although the dead times are very short, they adversely affect the performance of the inverter. It results in a momentary loss of control causing deviations from precisely designed PWM signal. Since this is repeated over the switching period, the accumulated error may become significant in inverters operating at very high frequency.

A half bridge inverter is used to analyze the effect. The output voltage (V_{AN}) for ideal and delayed base drive signals with positive and negative current directions are shown in Fig. 1.7.

As seen from the Fig. 1.7, each pulse of the output voltage is either shortened or lengthened by an amount according to whether the direction of the phase current is positive or negative respectively.

The average deviation over a half cycle from [23] is given by

$$\Delta V = \frac{M_n \, t_{\Delta} V_{dc}}{T_{sw}} \tag{1.1}$$

where M_n is the number of switching per cycle, V_{dc} is the dc link voltage
T_{sw} is the switching period, t_{Δ} is the dead time interval

Thus the overall effect of the dead time can be studied by considering it as an addition of a square wave of magnitude ΔV and 180° out of phase with the load current to the fundamental output voltage. A sample program was run in MCAD[43] and the results for a case without dead times is shown in Fig. 1.8. With a 10μsec dead time introduced in the analysis the results obtained from MCAD are shown in Fig. 1.9. There is appearance of low order harmonics of the order $4m\pm1$ (m=1,2,3...). Also the fundamental voltage gain is lowered by 7.2%.

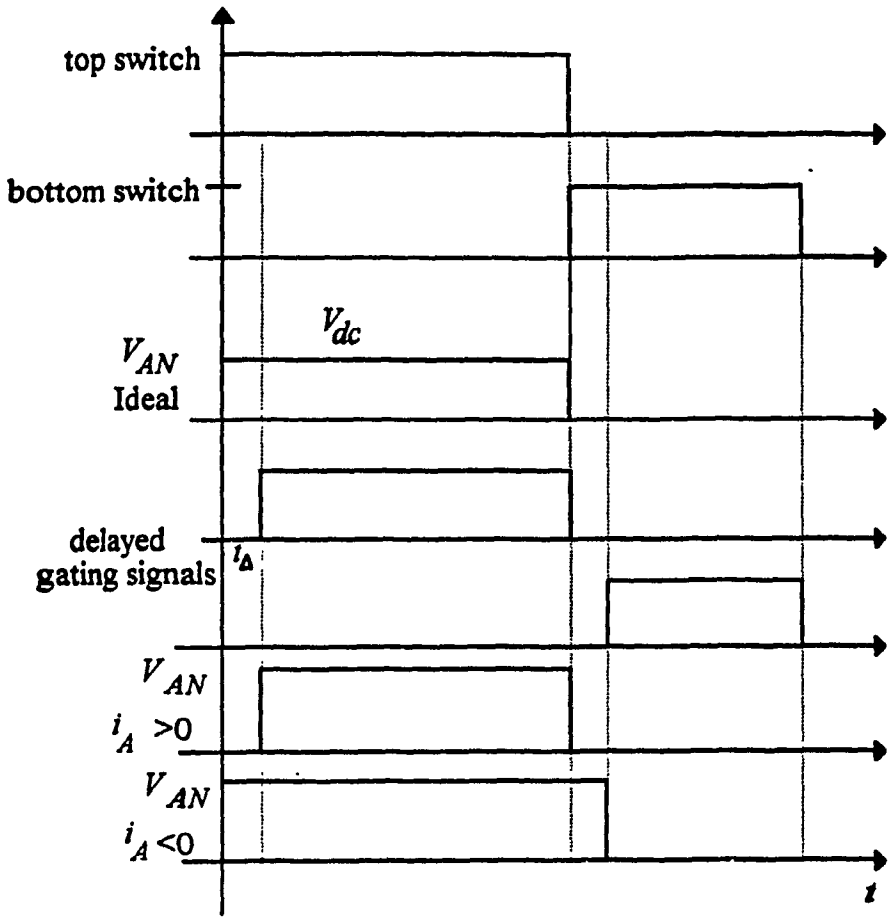


Fig. 1.7. Dead time effects in a half bridge inverter

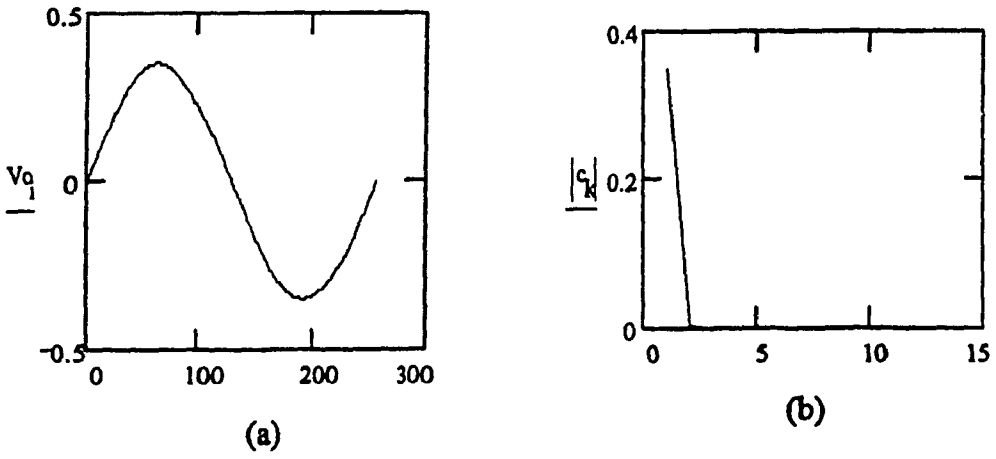


Fig. 1.8. Ideal PWM switching, no dead time. (a) Output voltage. (b) Harmonic Spectra

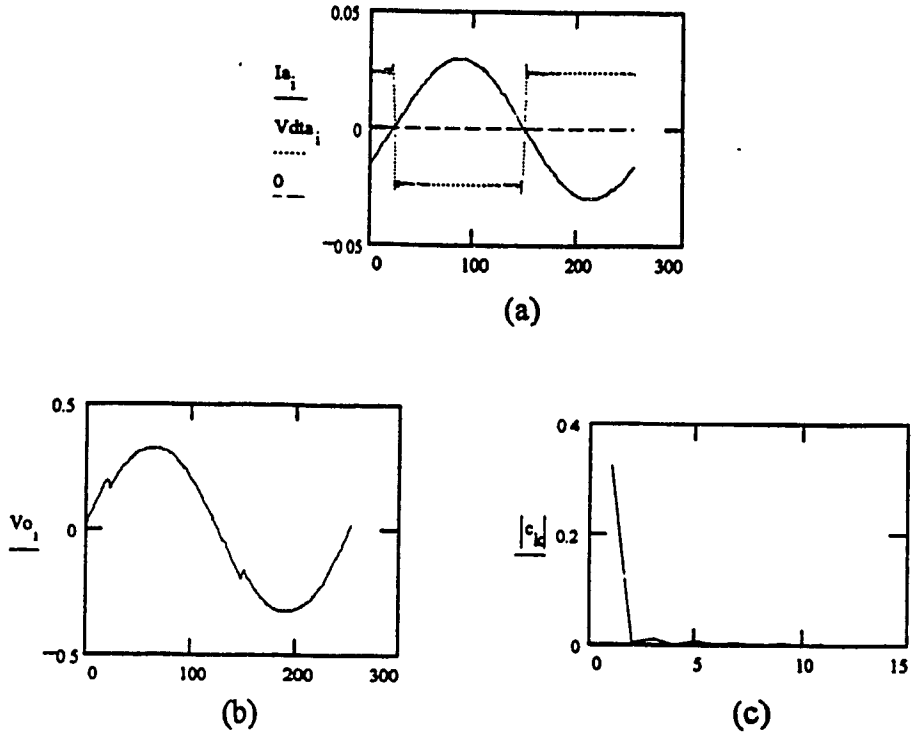


Fig. 1.9. Dead time of 10μsec in gating signals. (a) Load Current and equivalent dead time voltage. (b) Output voltage (excluding the switching harmonics). (c) Harmonic spectrum of the output voltage.

1.3. Review of previous research

In this section, a review of literature addressing the problems of non-ideal dc bus and switching delays in power converters is presented.

1.3.1. Feedforward techniques

It is important to realize that input source harmonics and disturbances are generated prior to the switching converter. Voltage feedforward techniques[25], make use of this feature and try to provide corrective action in the gating signals even before they propagate to the output voltage. This can provide better input harmonic/disturbance rejection.

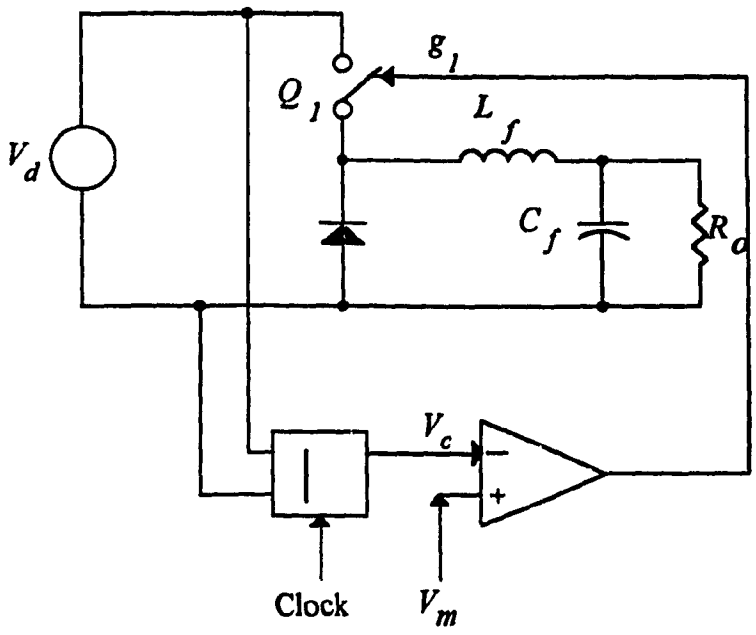


Fig. 1.10. A feedforward dc-dc buck converter

A typical feedforward loop in a dc-dc converter is shown in Fig. 1.10. The input voltage is directly sensed and passed through a integrator to generate the sawtooth ramp. It functions exactly like a direct-duty cycle control with one main exception: the sawtooth ramp is not constant in magnitude and is a function of the instantaneous input voltage. If the input is higher, the slope is higher and vice-versa. If control voltage is fixed, the duty cycle varies inversely with the input voltage resulting in a constant volt-second product. This is illustrated in Fig. 1. 11 which shows the ramp waveform for different input conditions (V_d).

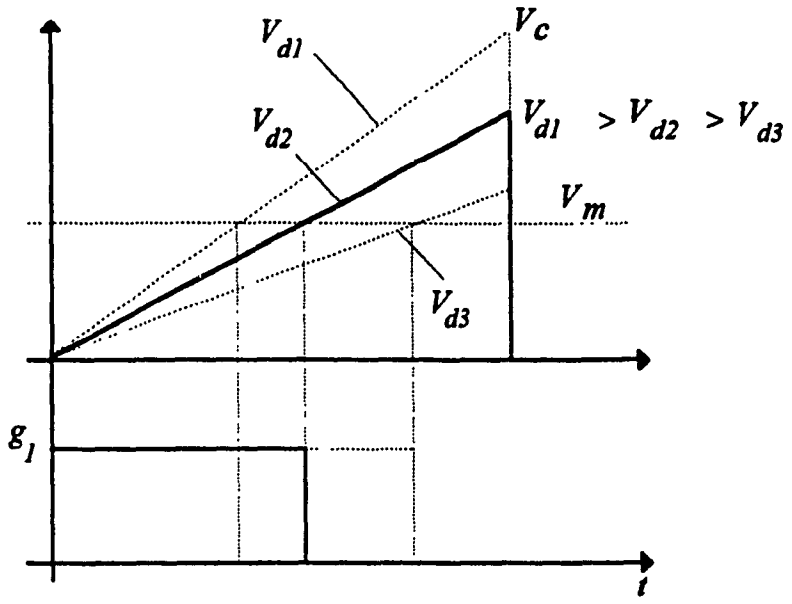


Fig. 1. 11. Effect of a feedforward loop on ramp carrier and switch control signal

Feedforward techniques have been documented in literature. An optimal feedforward compensation [26] was applied to dc-dc converters to reduce dc audio susceptibility. In [27], feedforward control was used to eliminate the input filter interaction with the feedback loop. However none of the above references quantify the harmonic rejection ability of the feedforward loop. Also conventional feedforward schemes based on input voltage sensing cannot compensate for non-ideal switches.

A feedforward technique that determines the exact switching function to eliminate harmonics is the objective of [28]. It is based on input voltage sensing and then determining the gating pulses for the converter switch. The technique however fails to correct for non-ideal conditions present in the switching environment.

In [29], a novel approach (One-cycle control) in controlling switching converters is proposed. In this technique the gating pattern is generated by sensing the voltage across the free-wheeling diode. Potential applications of the technique are identified but not quantified. Design guidelines are not specific. Based on this technique, a modified

feedforward loop is presented in this thesis for a dc-dc converter which can provide better performance than conventional feedforward scheme.

A feedforward technique (Fig. 1.12), involving sensing of the dc voltage is proposed in [30] to eliminate the effect of input dc bus ripple in dc-ac converters. The input dc bus voltage is expressed as:

$$V_d = V_{dc} + k_r V_{dc} \sin(2\pi f_r t) \tag{1.2}$$

where f_r is the dominant ripple frequency present in the dc bus.

This technique generates a new switching function ($\overline{SW_{lln}}$) and is obtained by:

$$\overline{SW_{lln}} = \frac{1}{1 + k_r \sin(\omega_r t)} \overline{SW_{ll}} \tag{1.3}$$

where $\overline{SW_{ll}}$ is the line switching function[31].

The new switching function can thus eliminate the effect of the input dc bus ripple voltage. This switching function is applied to an off-line optimized PWM pattern stored in an EPROM. The technique however requires (a) dc bus voltage sensing (b) additional control circuitry to derive the new switching function and access the optimized pattern.

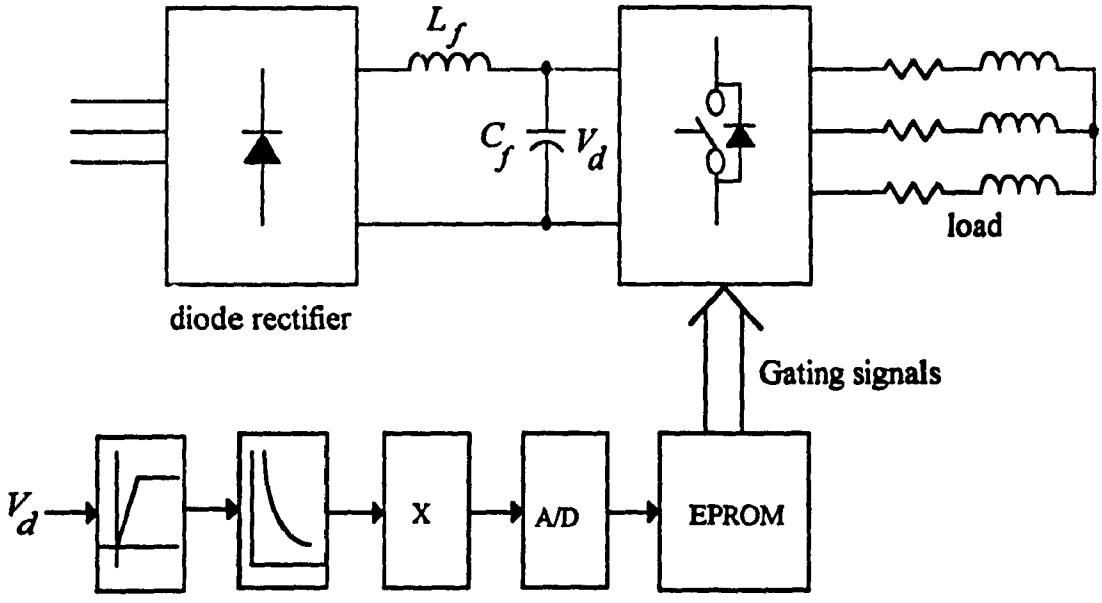


Fig. 1.12. Block diagram implementation of the scheme proposed in [30]

1.3.2. Advanced PWM techniques using microprocessors

To eliminate the effect of the input ripple, a selective harmonic reduction technique is presented in [32]. A sinusoidal reference is replaced by a quasi-sinewave whose magnitude varies inversely with the input voltage. The technique however requires real time calculations and in particular needs a large number of A/D and D/A conversions per cycle. Also the tradeoff involved are not analyzed. This is suitable only for microprocessor based control of PWM converters.

A digital control strategy for a three phase inverter is proposed in [33][34]. The pulse width is computed by sampling (Δt) the input voltage and ensuring the area under the voltage pulse is equal to the area under the reference voltage which in this case is chosen to be a sinusoidal voltage. Thus by ensuring the output voltage pulse follows a sinusoidal reference, a good harmonic rejection is reported. This is shown in Fig. 1.13, in which the area S_1 is made equal to area S_2 .The method to obtain the switching points(t_{on} and t_{off}) is detailed in the reference. The technique requires intensive mathematical computations and hence is suitable only for microprocessor implementation.

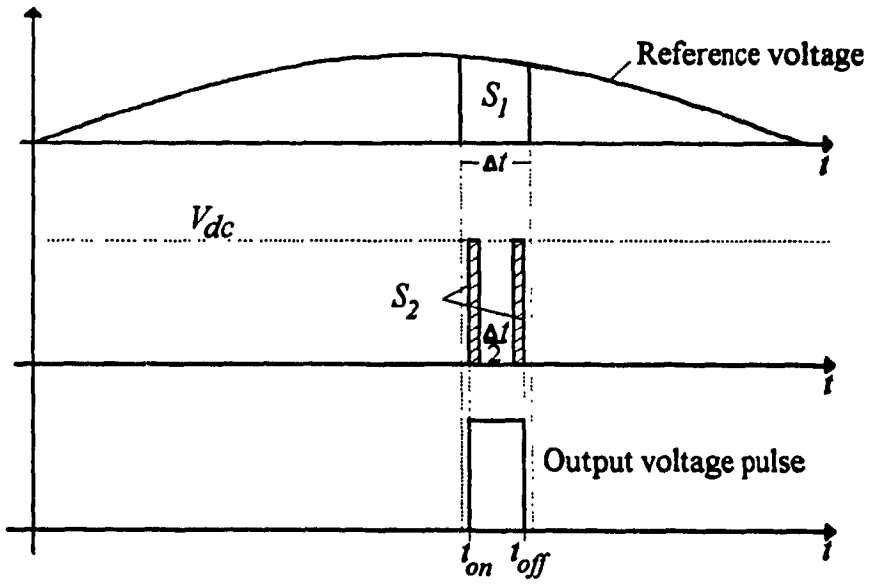


Fig. 1.13. Determination of switching function for technique proposed in [33][34]

A technique somewhat similar in concept, but much easier to implement using analog/digital circuits is introduced in this thesis.

1.3.3. Dead time compensation

To reduce the effect of the dead-times in voltage source inverters, novel control schemes have been proposed in [23][24]. They essentially modify the control signals obtained from an off-line SPWM or memory based techniques in a way to minimize the effect of dead times on the output voltage. The principle of compensation is to detect any deviations in voltage and cancel it in the next switching instant. In [23] correction is based on sensing the line currents. On the other hand in[24], the correction circuit needs sensing of phase voltages for applying correction. Thus immunity to dead times is achieved at the expense of additional control circuitry (Fig. 1.14)

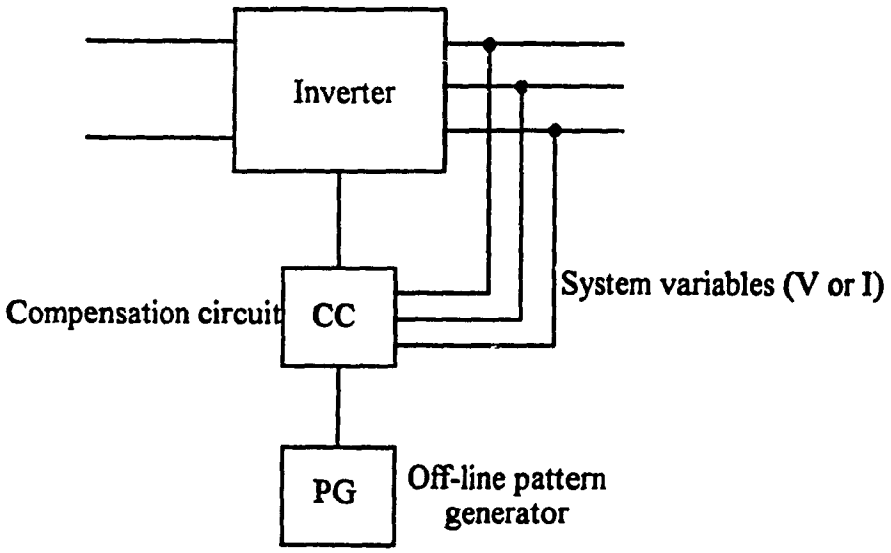


Fig. 1.14. Dead time compensation in [23][24].

1.4. Scope and contribution of this thesis.

This thesis provides solutions to problems associated with a non-ideal dc bus and semiconductor devices in a power converter system. These solutions exploit the concept of converter output voltage integral control to improve the performance of PWM converters. Two control schemes, Reset Integral Control (RIC) and Modulated Integral Control (MIC) are identified based on this concept and applied to dc-dc [35] and three phase dc-ac voltage source inverters [36][37]. The purpose of these schemes is to produce an output voltage that minimize dc bus and inverter generated distortion. They can be used as pre-regulators for further control schemes. Theoretical analysis and computer programs written in FORTRAN[38] are used to compute the respective switching functions. The feasibility is exhibited and quantified through computer simulation on PECAN[39][40][41] software package. Experimental results are obtained on laboratory prototypes comprising of BJT based three phase voltage source inverter and MOSFET based dc-dc buck converter topology. The control circuit is designed using state-of-the-art analog and digital devices.

1.5. Outline of the thesis

The contents of the thesis have been organized as follows:

Chapter 2 identifies an output voltage integral duty control based on which two modified feedforward techniques, Reset Integral Control and Modulated Integral Control are derived. Key simulation results are shown and potential area of applications identified.

In Chapter 3 feedforward techniques based on integral duty cycle control are analyzed for dc-dc converters. Design equations are derived. Simulations results are provided which are validated by experimental results.

Chapter 4 introduces feedforward techniques based on integral duty cycle control for dc-ac converters. The position of the voltage sensor and the control reference is identified. Design equations are derived. Simulations results under different input

conditions are provided. The results are compared with standard SPWM outputs under similar conditions. Feasibility of pattern generators is validated by experimental results.

Chapter 5 concludes the thesis and identifies some areas for future research work.

CHAPTER 2

PRINCIPLES OF OUTPUT VOLTAGE INTEGRAL DUTY CYCLE CONTROL

2.1. Introduction

As discussed in the last chapter, DC input to many modern power converter systems is usually obtained from a three phase, 60 Hz AC source using a front end diode bridge rectifier. Due to the AC/DC conversion and possible line fluctuations, the rectifier output voltage is unregulated and contains large harmonics which cannot be completely filtered. This is found to degrade the performance of the overall converter system fed by the rectifier. The objective of this chapter is to develop two control strategies based on the output voltage integral duty cycle control which can provide fast dynamic response and good input harmonic/perturbation rejection. These control algorithms can be used in PWM pattern generators without introducing much complexity in their implementation.

In this chapter two control schemes, Reset Integral Control (RIC) and Modulated Integral Control (MIC) are derived and their hardware implementation on a general converter presented. These schemes provide real time control of the power converter, capable of correcting the non-ideal conditions in each switching cycle and can be used as voltage pre-regulators for feedback loop design. This results in improved performance and better control. Principle of operation is explained. Complete control logic is illustrated through flow charts. Application of these control techniques to individual converter systems (dc-dc or dc-ac) are discussed in detail in subsequent chapters of the thesis.

2.2. Output Voltage Integral (OVI) Duty Cycle Control

This is a non-linear control technique in which the duty cycle (or the ON time) of a switch is controlled in real time. It is based on sensing the instantaneous output voltage pulse of a converter and adjusting its width in each switching cycle. The heart of the control circuitry is a real time integrator. Since the process of integration is associated with the area under a curve, by integrating the output voltage, the area (equivalently, the volt sec distribution) under the output voltage is being controlled. The criterion for pulse width is that the area under the output voltage pulse in each switching cycle be always equal to a control reference, irrespective of the input dc bus variations, switch conduction drops and switching delays. This is illustrated in Fig. 2.1.

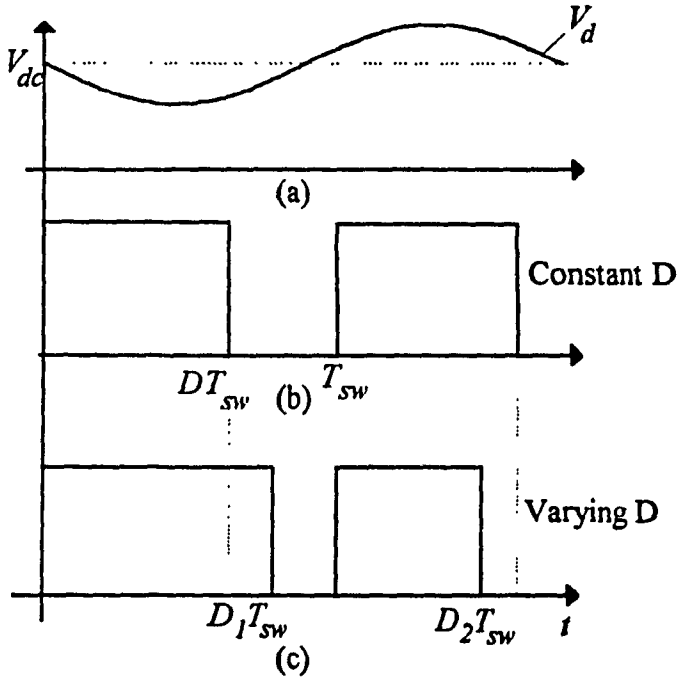


Fig. 2.1. Effect of varying input on duty cycle. (a) Input voltage to the converter(V_d). (b) Open loop control. (c) Output voltage integral duty cycle control.

Consider a time varying input (V_d) to the converter operating at a fixed duty cycle (D). The gating signal of the converter is shown in Fig. 2.1(b). It is obvious that the

output voltage will vary from the desired value. However with the integral control, the pulse width is adjusted to a duty cycle D_1, such that the volt sec distribution averaged over a period ensures the desired value of the output voltage. Similarly in the next switching cycle the pulse width is adjusted to a duty cycle D_2 (Fig.2.1(c)) As is clearly seen:

$$D_1 > D \text{ and } D_2 < D$$

Thus for a given input voltage, the output voltage pulse width with voltage integral control changes in each switching period adjusting to the input voltage variations for a given control reference. When the input is high, the pulse width is small and vice-versa. The pulse width being a function of the non-ideal conditions present in a switching converter, guarantees a high quality output voltage. Since the pulse width is being controlled in each switching cycle, the technique is also referred to as One Cycle control of switching converters.

2.3. Reset Integral Control Technique

This technique is based on the voltage integral duty cycle control discussed in the previous section. The flow chart of the control algorithm is shown in Fig 2.2. The hardware implementation of the proposed pattern generator is in Fig. 2.3. The converter system is generalized as a black box with input and output nodes.

2.3.1. Principles of operation

The clock input to the S-R flip flop provides the ON gating signal (Q) to the switch thus connecting the input to the output of the converter at the beginning of each cycle. The controller determines the off time of the switch resulting in the optimum performance of the converter.

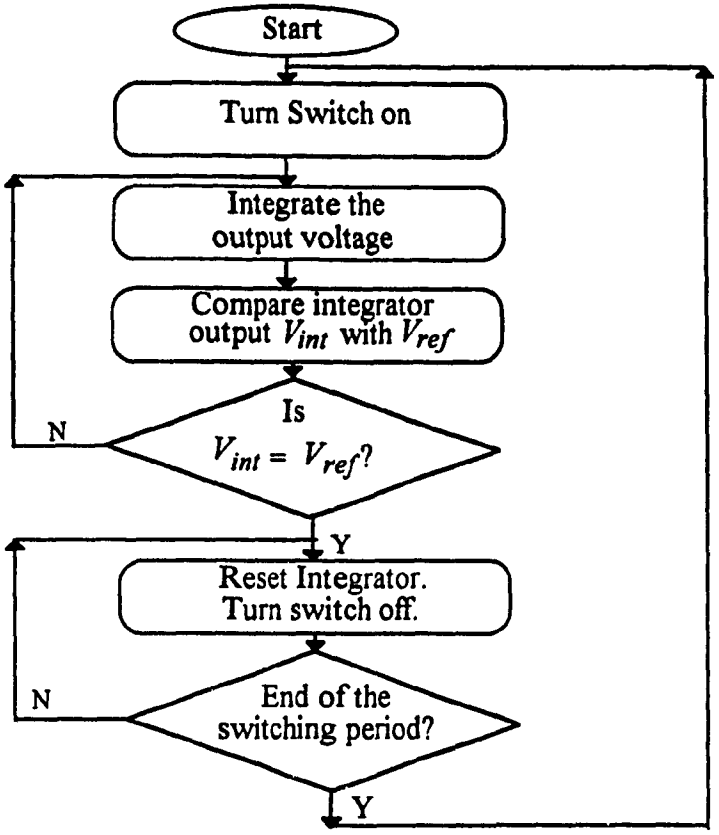


Fig. 2.2. Flowchart for Reset Integral Control technique

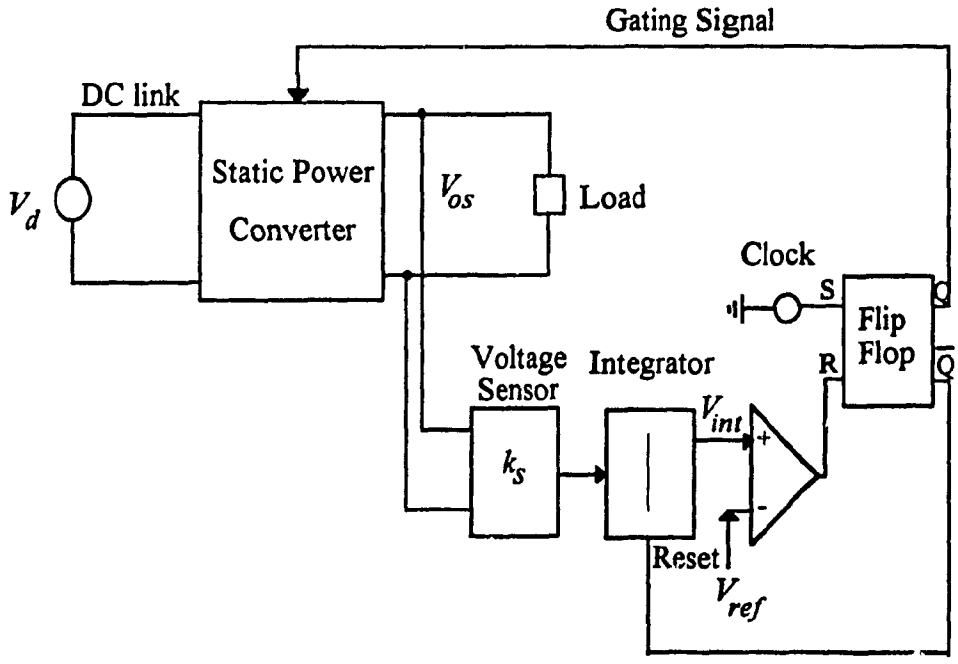


Fig. 2.3. Reset Integral Control Technique for a general converter system

As indicated in Fig 2.3, the output voltage of the converter (input voltage as long as the switch is ON), is sensed with a voltage sensor and fed to a real-time integrator. The integrator output generates the carrier waveform (V_{int}) which is compared with the instantaneous value of the reference waveform (V_{ref}) (a dc voltage for dc/dc converter or a sinusoidal control voltage for dc/ac converter).

When the output of the integrator touches the envelope of the reference voltage, signifying that the volt sec under the output voltage pulse is equal to the desired reference, the comparator output (R input of the flip-flop) goes high and resets the flip-flop. The switch is turned off (Q goes low) and integrator reset (hence the name Reset Integral Control) and disenabled ($\overline{Q}$ goes high) till the next clock pulse.

The gating signal is being generated on line and is a function of the input non-ideal dc voltage and switch conduction drops. Thus the output of the converter is maintained at the desired value and provides a regulated voltage, with low harmonic distortion to the load.

2.3.2. Waveforms

To study the feasibility of the reset integral control technique, key waveforms for two different types of control references are obtained from computer simulation using PECAN.

Fig. 2.4, shows the simulation waveforms with a dc control reference and is used for on-line control of a PWM dc-dc converter. A sinusoidal reference (with a dc bias) is necessary for controlling a dc/ac converter and simulation waveforms are shown in Fig. 2.5.

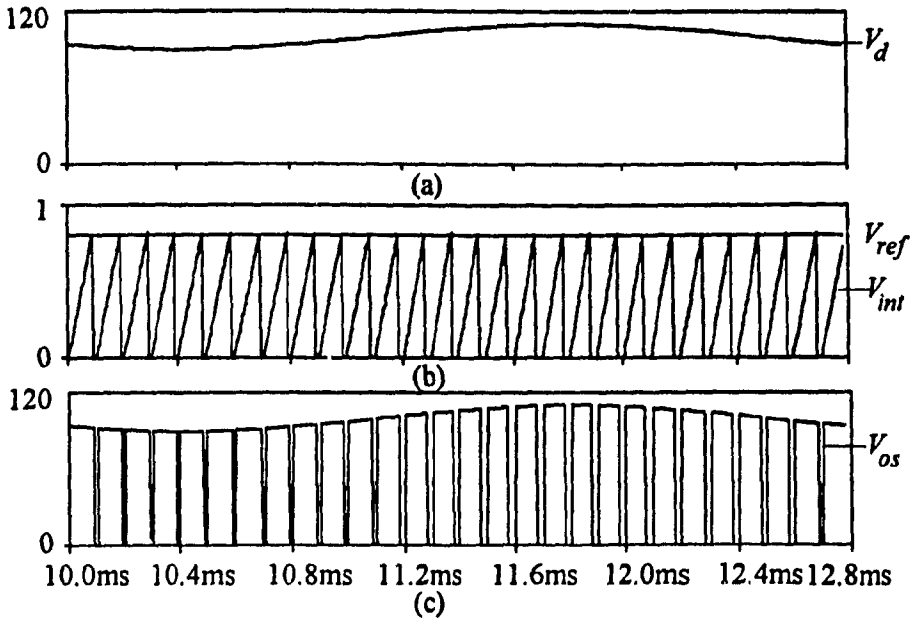


Fig. 2.4. Waveforms under Reset Integral Control technique with a dc reference (a) Input voltage (V_d). (b) Integrator output (V_{int}) and control reference (V_{ref}). (c) Output voltage of the converter (V_{os})

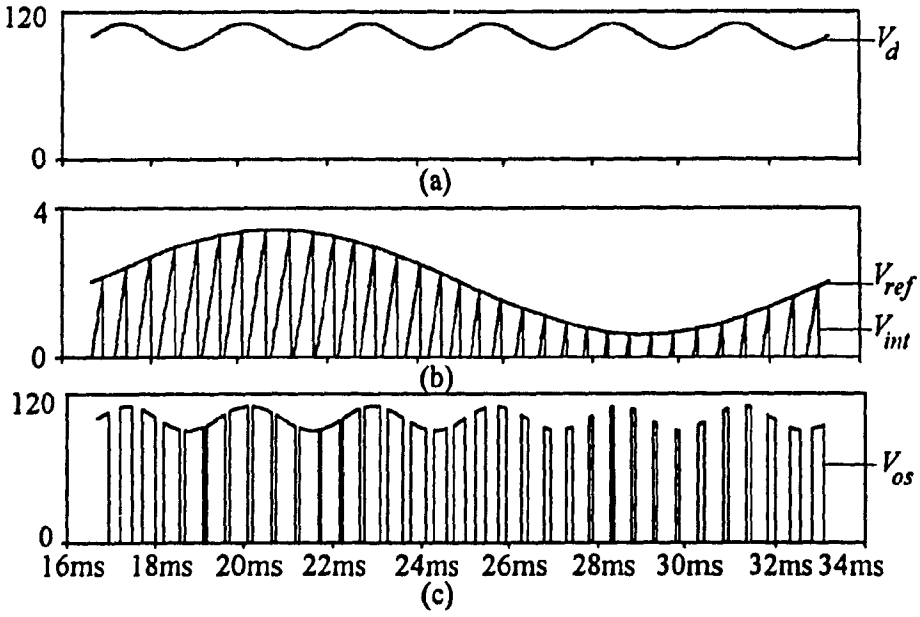


Fig. 2.5. Waveforms under Reset Integral Control technique with a sinusoidal reference. (a) Input voltage (V_d). (b) Integrator output (V_{int}) and control reference (V_{ref}). (c) Output voltage of the converter (V_{os})

2.4. Modulated Integral Control Technique

This is an alternate control strategy based on the voltage integral duty cycle control. However in this case the difference of the output voltage and a control reference (error signal), rather than the output voltage, is integrated to generate the modulating waveform (hence the name Modulated Integral Control). Also the integrator output is not reset. The control algorithm is shown in Fig. 2.6.

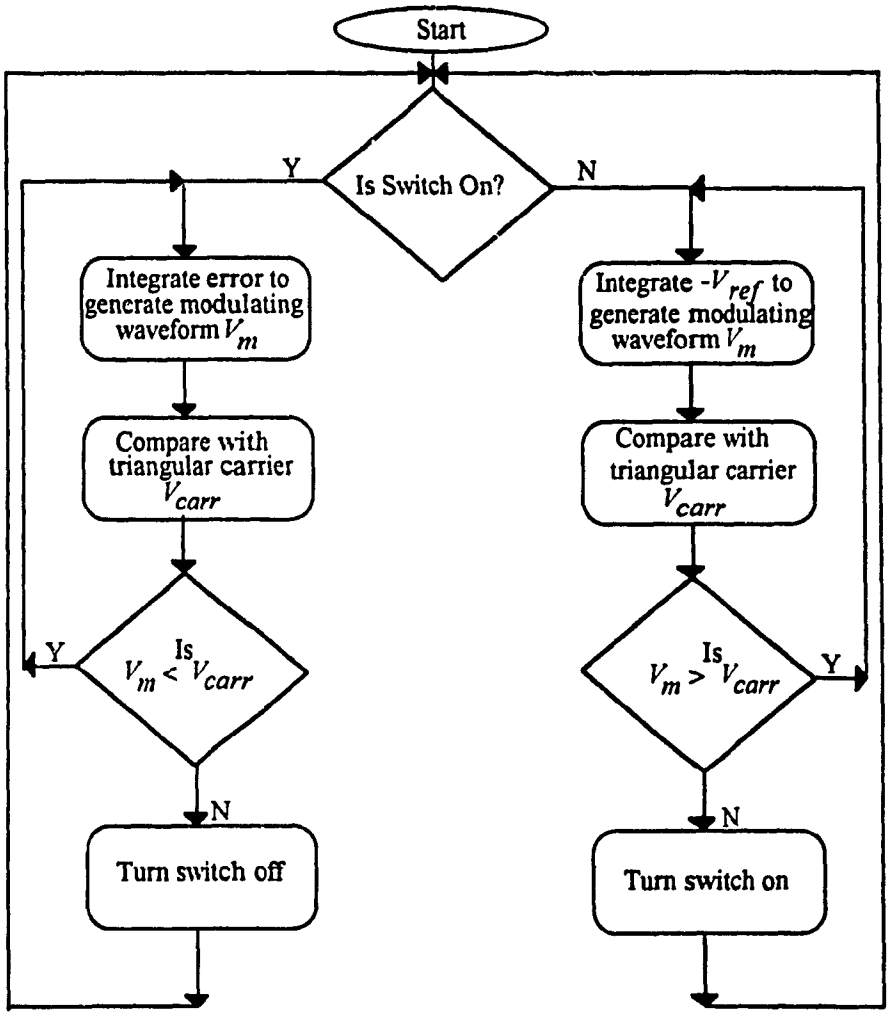


Fig. 2.6. Flowchart for Modulated Integral Control technique

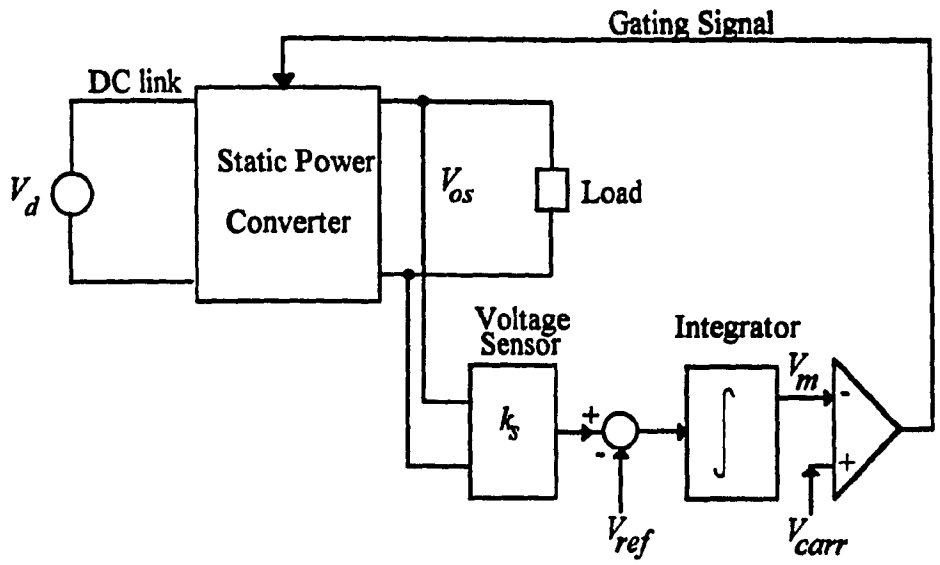


Fig. 2.7. Modulated Integral Control Technique for a general converter system

2.4.1. Principles of operation

As seen from the Fig. 2.7, while the switch is ON, the output voltage is sensed and subtracted from a reference (a dc voltage for dc/dc converter or a sinusoidal control voltage for dc/ac converter). The error is then integrated to generate the modulating signal with a rising slope. The gating signal is obtained by comparing the output with a triangular carrier. When the modulation waveform is equal to the carrier waveform, the switch is turned off. Thereafter $-V_{ref}$ is integrated to generate the modulation waveform with a negative slope and the intersection with the carrier determines the turning on instant of the switch.

2.4.2. Waveforms

Key control waveforms for two different types of control references are obtained from simulation. Fig. 2.8, shows the results with a dc control reference and is used for on-line control of a dc/dc converter. A sinusoidal reference (with a dc bias) is necessary for controlling a dc/ac converter and simulation waveforms are shown in Fig. 2.9.

The advantage of this technique is that the information from previous cycles is retained and utilized in the next period to apply correction to the gating signal. This is particularly important in correcting the errors due to switching delays (turn-on and turn off). In addition it can provide good harmonic rejection thus improving the quality of the output voltage.

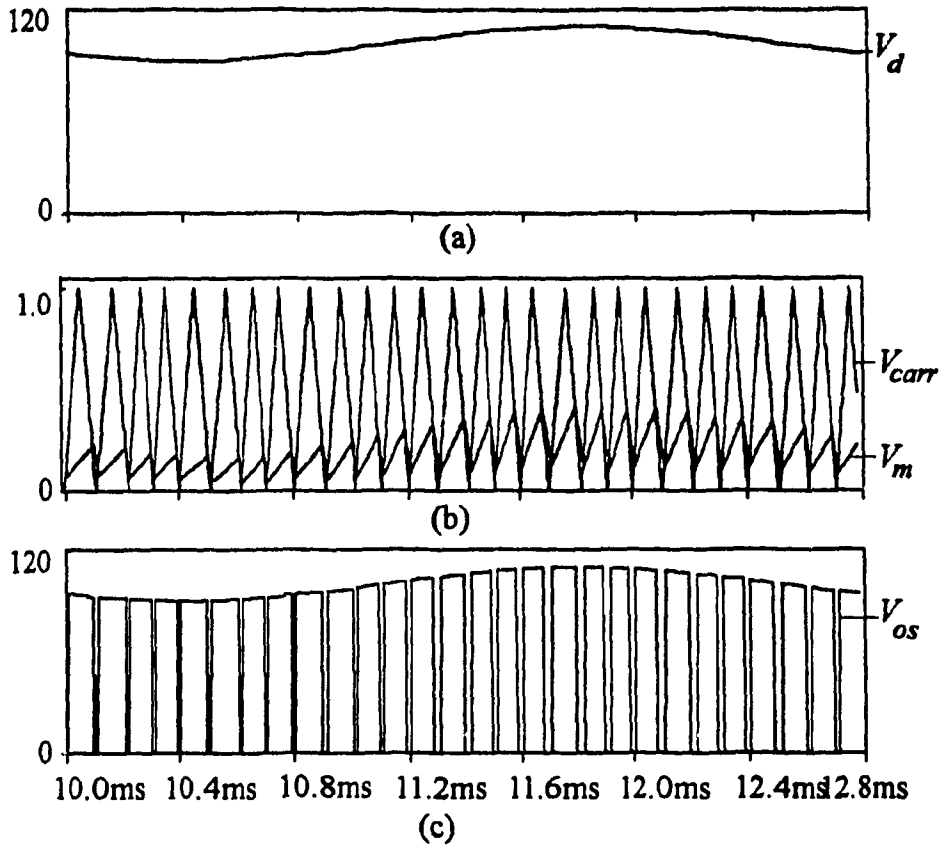


Fig. 2.8. Waveforms under modulated integral control technique with a dc reference (a) Input voltage (V_d). (b) Integrator output (V_m) and carrier waveform (V_{carr}). (c) Output voltage of the converter (V_{os})

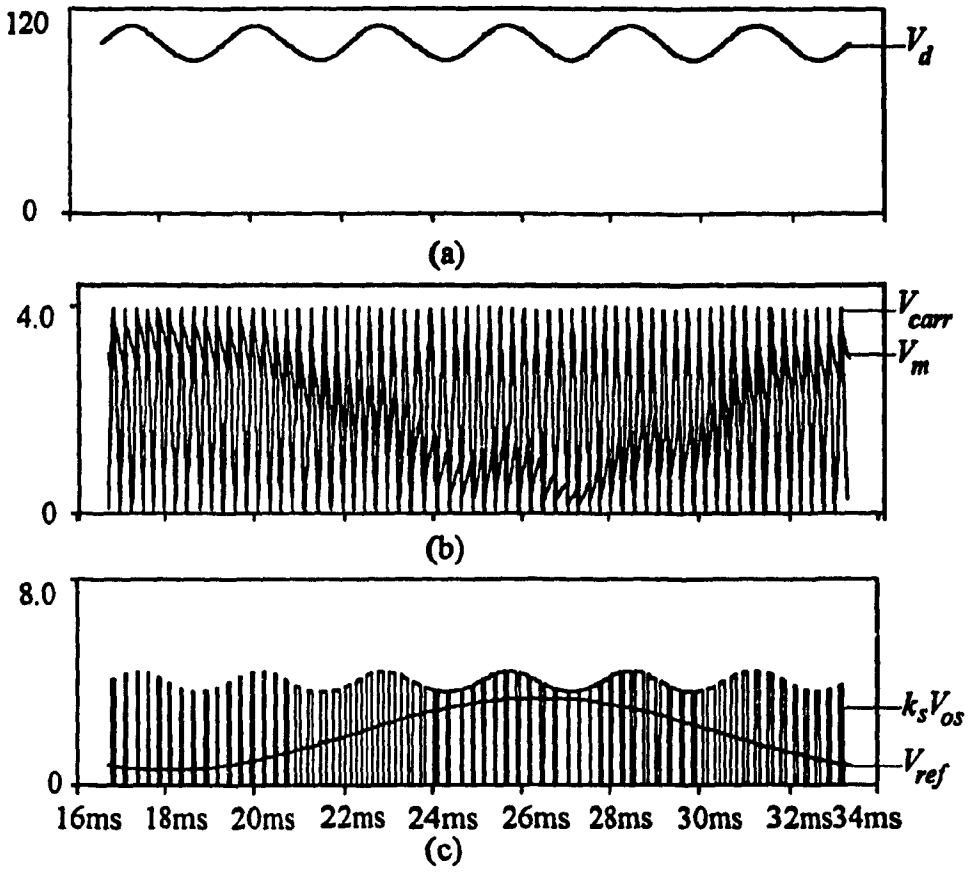


Fig. 2.9. Waveforms under Modulated integral control technique with a sinusoidal reference (a) Input voltage(V_d). (b) Integrator output (V_m) and carrier wave (V_{carr}). (c) Input voltage to the controller ($k_S V_{OS}$) and the desired reference (V_{ref}).

2.5. Conclusions

In this chapter two control strategies based on voltage integral duty cycle control along with their block diagram implementation are presented for a general converter system. The principle of operation is explained. Waveforms show the feasibility of these techniques in improving the performance of dc-dc and dc-ac converters. The techniques are easy to implement using the conventional analog and digital circuits.

CHAPTER 3

PERFORMANCE ANALYSIS OF DC-DC CONVERTERS USING VOLTAGE INTEGRAL DUTY-CYCLE CONTROL

3.1. Introduction

Conventional feedback control schemes have some inherent drawbacks and may not completely satisfy load requirements. This is particularly important in cases where the input is not well regulated and contains harmonics generated from causes other than switching action of the power converter. In such cases feedforward control techniques are found to provide better input line regulation and more effective in rejecting input harmonic disturbances.

In this chapter a voltage control technique for a dc-dc converter is derived from the conventional feedforward control technique by changing the location of the voltage sensor. The generation of the gating signal is then based on output voltage integral duty-cycle control concept introduced in the Chapter 2. Two alternate control techniques: Reset Integral control and Modulated Integral Control, are investigated in detail and found to provide good harmonic rejection. In addition, modulated integral control can correct errors due to switching delays. Complete mathematical analysis and design method is outlined. Simulation results are verified experimentally on a 1 kW laboratory prototype.

3.2. Implementation aspects

In conventional feedforward technique the ramp carrier is generated by integrating the input voltage and resetting the integrator at the end of the switching period. It is noticed that only portion of the input voltage integrated from the beginning of the cycle to t_{on} is effectively used to determine the gating pattern. The ramp voltage greater than the

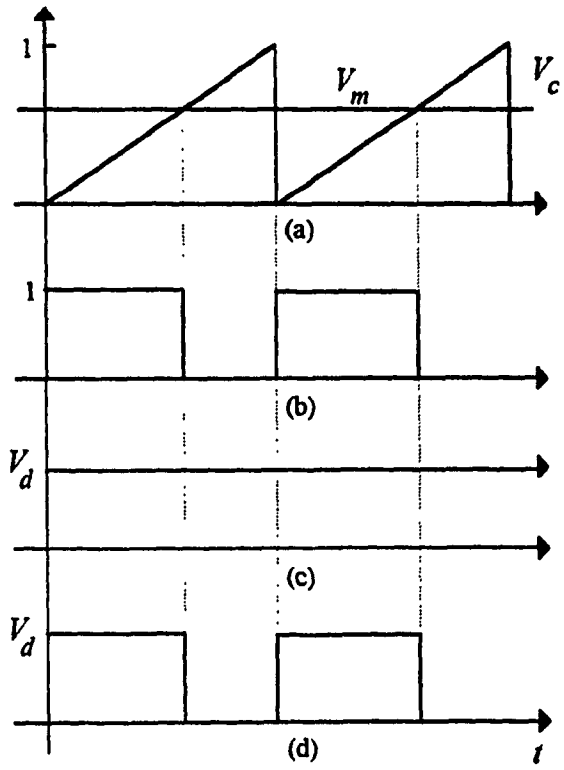


Fig. 3.1. Conventional feedforward technique. (a) Carrier (V_c) and control voltage (V_m). (b) Gating signal for the switch. (c) Input to the integrator. (d) Input effective in generating the gating signal.

control voltage does not contribute in generating the gating pattern and is redundant. Thus the input voltage effectively used in generating the gating waveform can be drawn as shown in Fig. 3.1(d). Assuming an ideal switching characteristic, this voltage is exactly the same as the voltage across the diode. In other words, the voltage feedforward loop can be equally implemented by integrating the voltage across the diode rather than sensing the input voltage directly.

The advantage in doing so, is that now the control loop not only senses the input line voltage but also takes into account the switch conduction drops (Reset Integral Control) and switching delays (Modulated Integral Control). These were hitherto being considered negligible. However in the high power applications these issues can be of

concern. Since it is the output voltage that is being integrated, a constant dc output is always maintained regardless of the input voltage variations or switch conduction losses and delays.

3.3. Reset Integral Control

The principle of the reset integral control was discussed in Chapter 2. In this section, the technique is applied to a dc-dc converter. Fig. 3.2. illustrates the complete circuit diagram of a buck converter under the proposed Reset Integral Control. The voltage sensor is placed across the diode rather than the input voltage and used to control the on-times of the switch (Q_1).

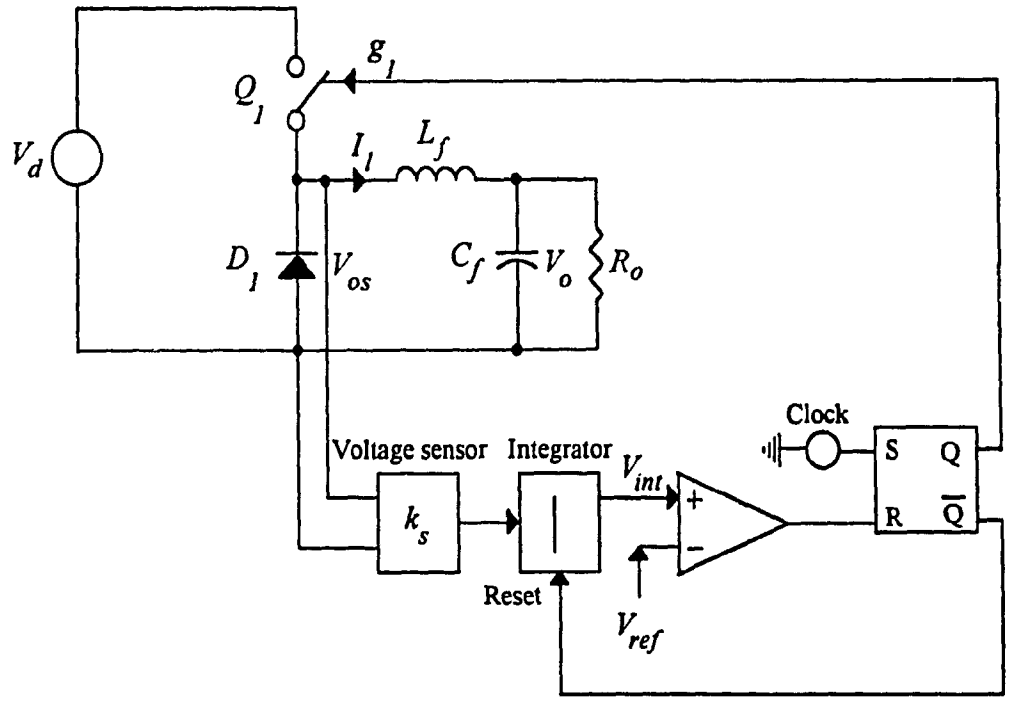


Fig. 3.2. Reset Integral Control technique for a buck converter

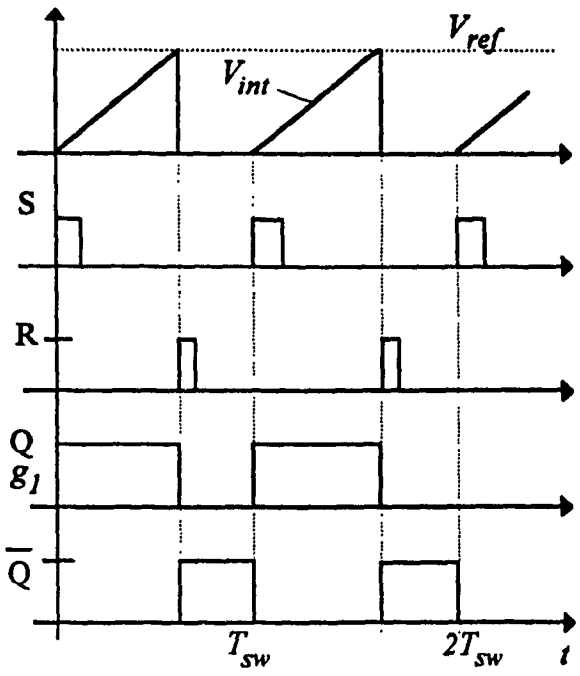


Fig. 3.3. Control Signals under Reset Integral Control

3.3.1. Principles of operation

The clock input to the S-R flip-flop turns the switch on (Q goes high) at the beginning of each switching cycle (T_{sw}). The chopper output voltage (which is the input voltage as long as the switch is on) is integrated and compared with a dc reference (V_{ref}). As it reaches the reference, the comparator output goes high which resets the flip-flop (R goes high) and turn off the switch Q_1 (Q goes low). The integrator is reset ($\overline{Q}$ goes high) and disabled until the beginning of the next switching cycle. The control signals are shown in Fig. 3.3.

The on time of the switch is controlled by the rate of integration (dependent on the input voltage and integrator time constant) and the control voltage (V_{ref}) and can be computed by the following equation:

$$\frac{1}{\tau}\int_0^{t_{on}} V_d \, dt = V_{ref} \tag{3.1}$$

where V_d is the input voltage and V_{ref} the control reference voltage and τ the integrator time constant. The general input can be represented by:

$$V_d = V_{dc} + k_r V_{dc} \sin(2\pi f_r t) \tag{3.2}$$

where k_r is the measure of the harmonic content of the input at single dominant frequency f_r.

Assuming a constant input voltage i.e. $V_d = V_{dc}$, the expression in (3.1) can be rewritten as:

$$t_{on} = \frac{\tau V_{ref}}{V_{dc}} \tag{3.3}$$

The duty cycle (D) defined as $\frac{t_{on}}{T_{sw}}$ can be determined as:

$$D = \frac{\tau V_{ref}}{V_{dc} T_{sw}} \tag{3.4}$$

The output voltage (V_o) of the buck converter is the area under the curve averaged over a time period. The area under the curve for an input V_d, can be found to be:

$$\int_0^{t_{on}} V_d \, dt \tag{3.5}$$

The output voltage can then be found by combining (3.1) and (3.5)

$$\begin{aligned} V_o &= \frac{\int_0^{t_{on}} V_d \, dt}{T_{sw}} \\ &= \frac{\tau V_{ref}}{T_{sw}} \end{aligned} \tag{3.6}$$

For a given system, T_{sw} and τ are fixed. Thus the output voltage is directly proportional to the reference voltage and is independent of the input conditions. Thus a constant output voltage is guaranteed at the output irrespective of the input dc bus variations.

The feedforward corrective action of the technique is evident if the input is considered to varying in magnitude. The slope of integration is directly proportional to the input voltage and integration value is continuously compared with the constant control reference. When the input voltage is higher, the slope of integration is steeper, therefore, the integration value reaches the control reference faster. As a result the duty ratio is smaller. When the input voltage is lower, the duty ratio is larger. This is clearly illustrated in Fig. 3.4 in which D_1 is greater than D_2. The duty cycle with an ideal dc bus is D.

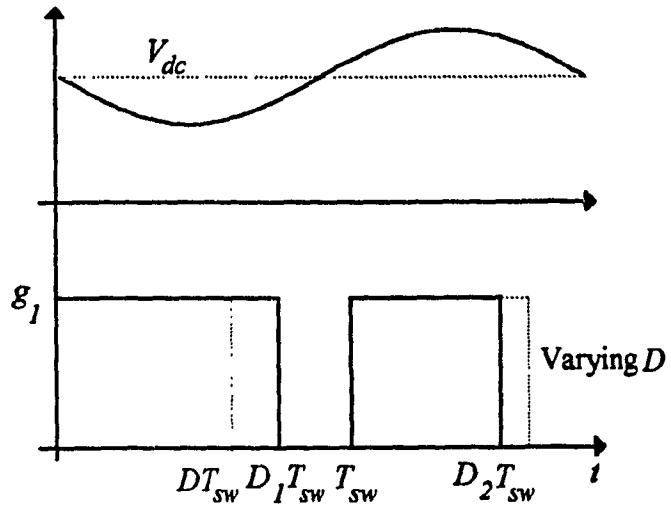


Fig. 3.4. Effect of varying input on the duty cycle of the converter working under reset integral control. (a) Input voltage (V_d). (b) Gating signal (g_1).

3.3.2. Selection of integrator time constant (τ)

In this section the guidelines for choosing the integrator time constant are indicated. The design is carried out for an ideal dc bus. The effect of the ripple voltage on the operating duty cycle of the converter is considered later.

3.3.2.1 Ideal dc bus

An ideal dc bus with no input harmonics and magnitude V_{dc} is considered i.e. k_r= 0 in (3.2).

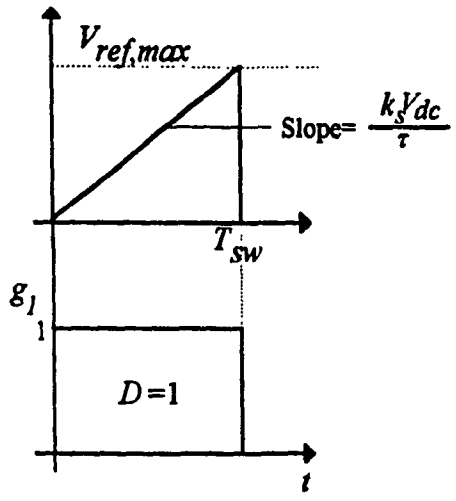


Fig. 3.5. Design of integrator time constant (τ).

From Fig. 3.2, the integrator output is given by:

$$V_{int} = \frac{k_s V_{dc} t}{\tau} \tag{3.7}$$

where k_s is the voltage sensor gain.

With reference to the Fig. 3.5., the design procedure involves in allowing the integrator to integrate to the maximum value of the reference voltage corresponding to a duty cycle D=1 in one switching period.

For D=1, let the reference be $V_{ref,max}$which can be chosen at will by the designer. Thus at the end of the switching period integrator time constant can be equated to the maximum value of the reference.

$$V_{ref,max} = \frac{k_s V_{dc} T_{sw}}{\tau} \tag{3.8}$$

Rearranging:

$$\tau = \frac{k_s V_{dc} T_{sw}}{V_{ref,max}} \tag{3.9}$$

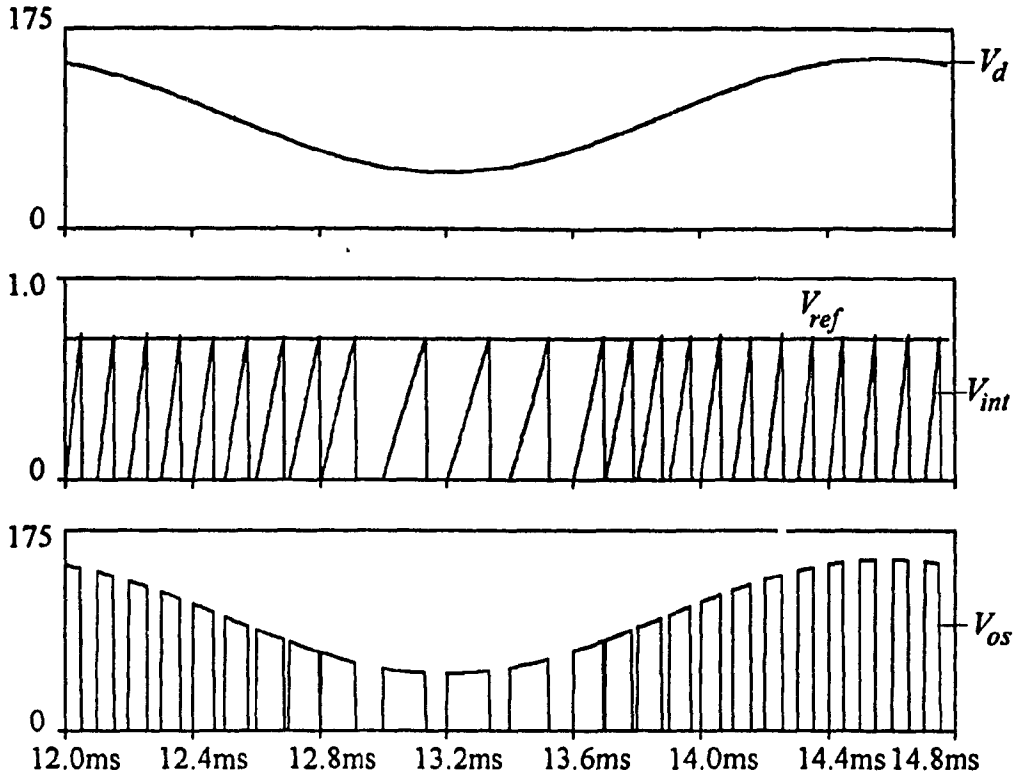


Fig. 3.6. Effect of non-ideal dc bus on design of integrator time constant. (a) Input voltage (V_d). (b) Control waveforms. (c) Output voltage(V_{os}).

3.3.2.2. Non-ideal dc bus

A non-ideal dc bus considered to be having a single dominant frequency of frequency f_r was defined in (3.2).

With a fluctuating input, the integrator cannot integrate up to V_{ref} in one switching period (Fig. 3.6) since for part of a period the input voltage is less than the chosen design value(V_{dc}). This then restricts the range of duty cycle up to which the converter can be operated. The maximum duty cycle now is a function of the amount of ripple($k_r V_{dc}$) present in the input dc bus voltage.

The minimum input to the integrator for a given amount of ripple from (3.2) is $V_{dc}(1-k_r)$. Thus the integrator can integrate only up to a certain fraction of the maximum reference $V_{ref,max}$. This is given by the following equation

$$\frac{k_s V_{dc}(1-k_r)T_{sw}}{\tau} = V_{ref} \tag{3.10}$$

Using (3.8) and rearranging

$$(1-k_r)V_{ref,max} = V_{ref} \tag{3.11}$$

Thus the maximum duty cycle is reduced to ($1-k_r$) and is the penalty imposed for implementing the feedforward loop. E.g. with 10% ripple, the maximum duty cycle (D_{max}) to which the converter can be operated without losing constant frequency operation is 0.9 only. This is shown in Fig. 3.7.

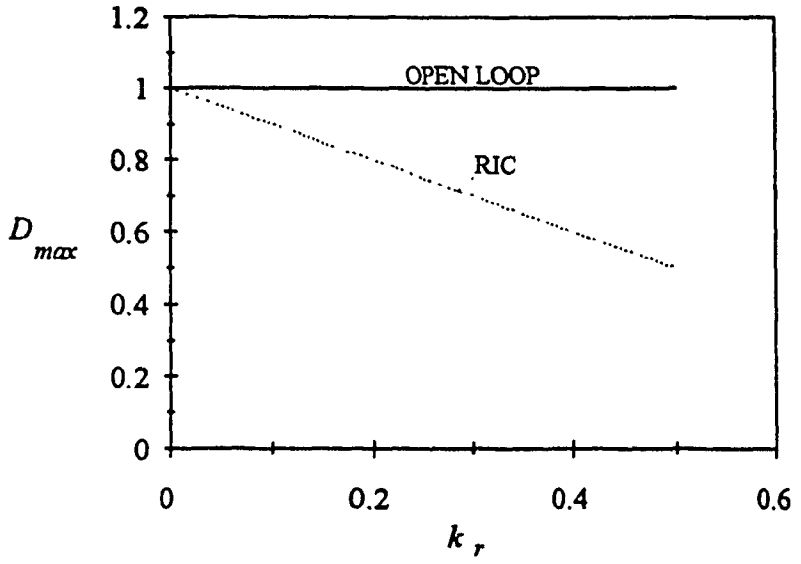


Fig. 3.7. Maximum duty cycle (D_{max}) as a function of ripple factor (k_r)

3.3.2.3. Design example:

A buck converter operating under reset integral control is designed for the following specifications:

- Input voltage (V_{dc})=100 volts
- Output power (P_o)=250 Watts
- Output voltage (V_o)=50 volts
- Switching frequency (f_{sw})=10 kHz

- Maximum reference voltage, $V_{ref,max}$ =1 volts.
- Voltage sensor gain, k_s =0.01.
- Maximum inductor current ripple (R_i)=5%
- Maximum output voltage ripple (R_v)=1%

From[2], the expression the for filter inductor(L_f) and capacitor (C_f) in terms of for R_i and R_v are:

$$R_o = \frac{V_o^2}{P_o}$$

$$L_f = \frac{V_o^2 (1 - \frac{V_o}{V_{in}})}{P_o f_{sw} R_i} \tag{3.12}$$

$$C_f = \frac{(1 - \frac{V_o}{V_{in}})}{8 f_{sw}^2 L_f R_v}$$

Substituting the specifications in (3.12) we have:

$$L_f = 10 \text{ mH} \quad C_f = 6.25 \ \mu\text{F} \quad R_o = 10 \ \Omega \tag{3.13}$$

Substituting the specifications for the integral controller in (3.9) yields

$$\tau = 100\mu\text{sec} \tag{3.14}$$

3.3.3. Steady state results

This section presents steady state results for a dc-dc converter working under Reset Integral Control with an ideal and non-ideal dc bus.

3.3.3.1. Ideal dc bus

In this section simulation results in steady state for a dc-dc converter operating under an ideal dc bus are presented. The converter is designed with a feedforward loop (section 3.3.2.3.) based on the principle of RIC. The results are compared with that obtained for a open-loop controlled buck converter. The dc duty cycle is 0.7. The results in steady state obtained are identical to the open loop case giving the desired output voltage and inductor current ripple specifications and shown in Figs. 3.8 and 3.9.

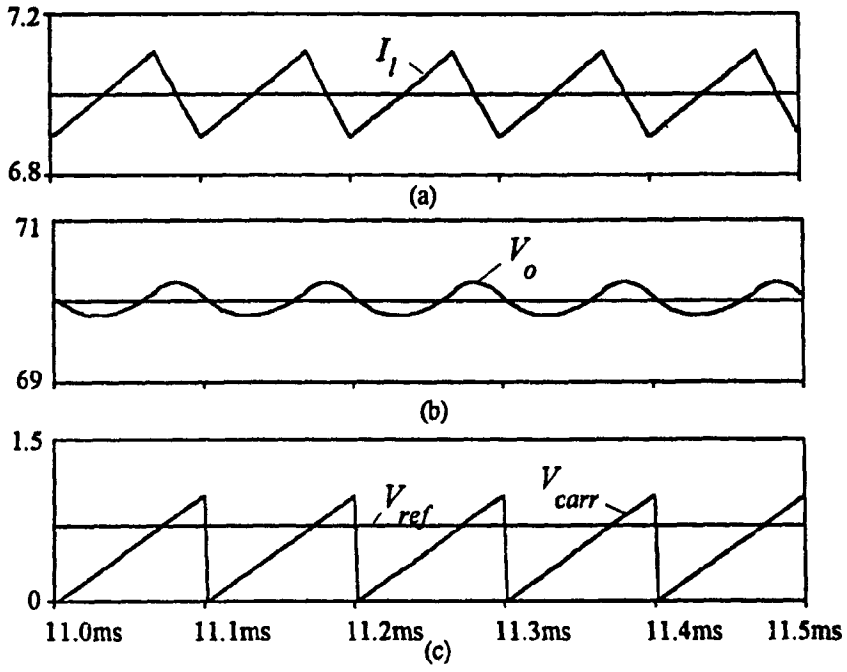


Fig. 3.8. Buck converter under open loop control. (a). Inductor current. (b) Output voltage. (c) Control waveforms.

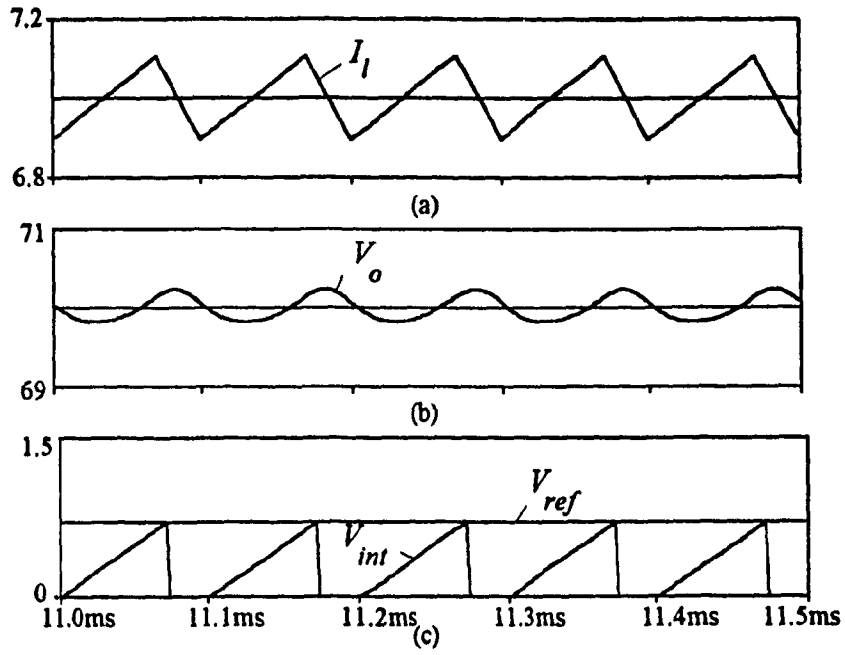


Fig. 3.9. Buck converter under Reset Integral Control. (a). Inductor current. (b) Output voltage. (c) Control waveforms.

3.3.3.2. Non-ideal dc bus

A non-ideal dc bus deteriorates the performance of the dc-dc converter by introducing low order harmonics in the output voltage. These harmonics are difficult to filter as their order is usually a small fraction of the switching frequencies used. A typical example is the 360 Hz, which is difficult to filter for a converter operating at 10 kHz. This is illustrated in input voltage spectrum in Fig. 3.11(a)

The small amount of harmonic in the output voltage is evident from the steady state results in Fig. 3.10(b) shown for one cycle of the input ripple voltage. With the converter operating with RIC, the harmonic is attenuated to a large extent (Fig. 3.11(b)), reducing the voltage distortion.

Thus the Reset Integral Control technique inherently compensates for the harmonic voltages in the dc bus and reduces the stress on the output filter and feedback loop design.

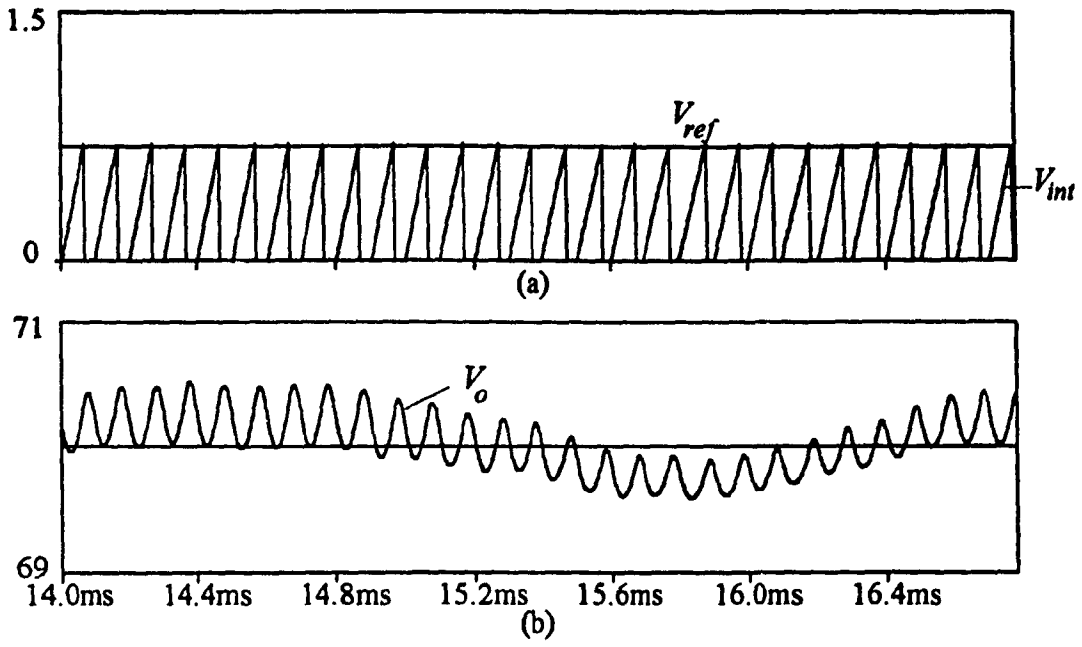


Fig. 3.10. Steady state results for a dc-dc converter operating under a non-ideal dc bus (a) Control waveforms. (b) Output voltage (detailed view)

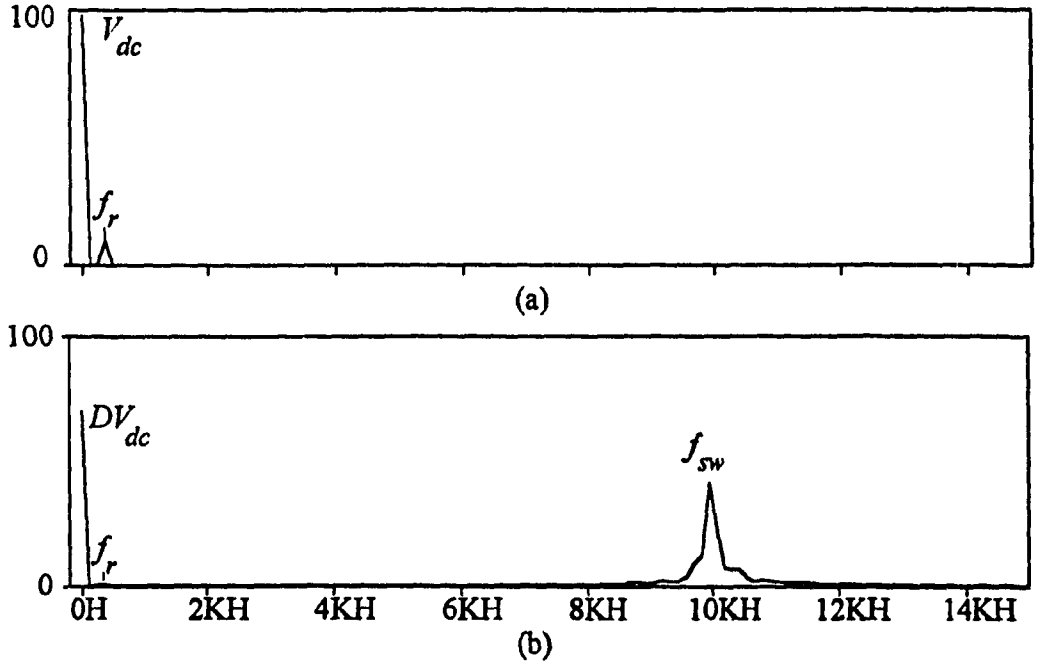


Fig. 3.11. Operation of dc-dc converter with a non-ideal dc bus. (a) Input voltage spectrum. (b) Output voltage spectrum (f_{SW}=10 kHz, D=0.7)

Although Reset Integral Control provides a constant dc output, its rejection to input source harmonics is dependent on the frequency of the source harmonic and the switching frequency. In order to evaluate the harmonic reduction of the integral loop quantitatively, a harmonic attenuation factor, K_h defined as the ratio of the output and input harmonic amplitudes is used.

To calculate the harmonic attenuation factor under Reset Integral Control, the switching function $f(t)$ (Appendix) is used. For a given input $V_d(t)$, the output voltage can be computed using:

$$V_{os}(t) = V_d(t) f(t) \tag{3.15}$$

The amplitude of the harmonic in the output voltage can be determined from (3.15) and K_h calculated. This factor is obtained as a function of the duty cycle and the ratio of source to switching frequency and is plotted in Fig. 3.12. It shows that the harmonic attenuation is better at lower duty cycle and at higher ratio of the input harmonic frequency to the switching frequency.

The attenuation can be also seen from Fig. 3.13 in which a 10% input harmonic was superimposed on the dc bus (k_r=0.1). The results are indicated for open loop, a conventional PI feedback, reset integral control and reset integral control with a feedback loop. As is clearly seen, reset integral control technique provides very good attenuation of the input source harmonic yielding a high quality output voltage.

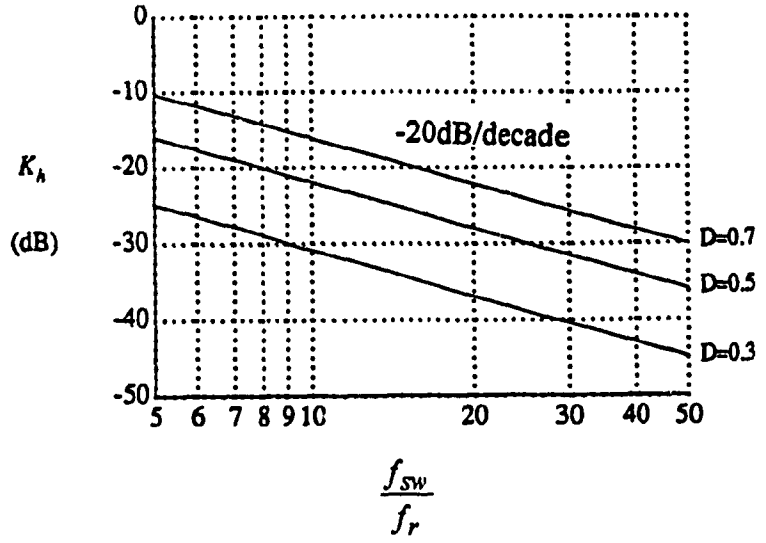


Fig. 3.12. Harmonic attenuation of reset integral control

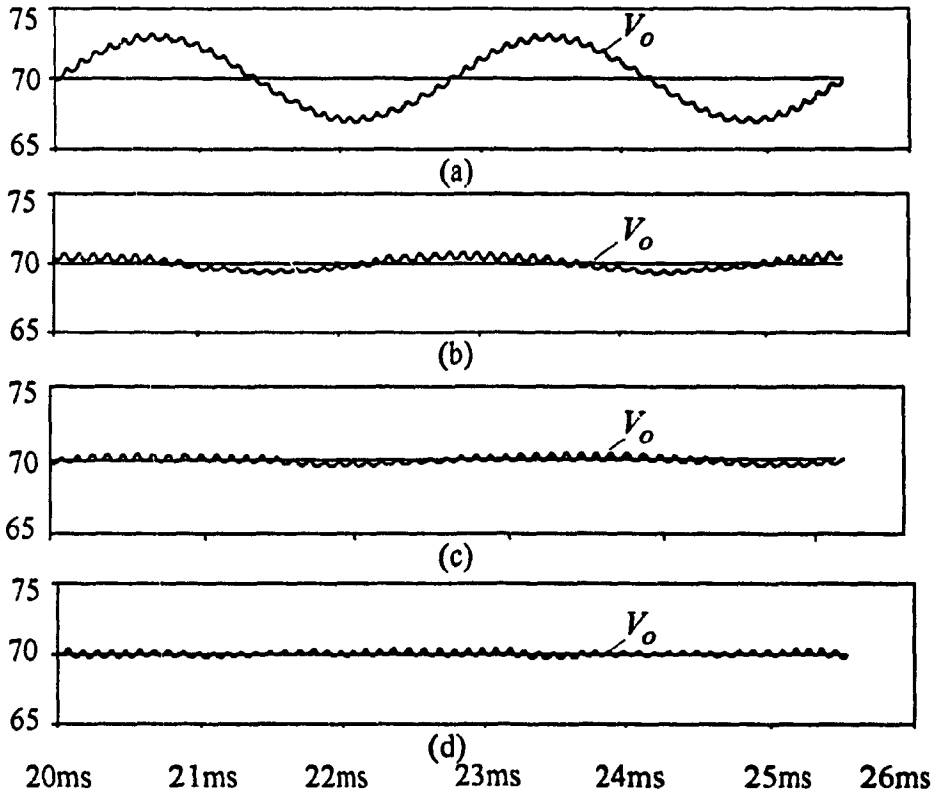


Fig. 3.13. Output voltage (detailed view) with 10% input source harmonic. (a) Open loop (b) Conventional feedback (c) Reset integral control (d) Reset integral control with feedback (k_f=0.1, f_r=360 Hz)

3.3.4. Dynamic response

The dynamic response of a dc-dc converter working under Reset Integral Control is illustrated by a step change in the input, whereby the input voltage is increased from 100 to 110 volts at t=14 ms as shown in Fig. 3.14. The controller reacts to the change in one switching cycle. Since the input voltage is higher, the rate of integration is faster. This results in narrower output voltage pulse following the disturbance and is evident from Fig. 3.14 (c). At the same time change in pulse width is such that the average output voltage remains the same and is determined by the reference voltage. Thus even after a large change in the input voltage, the output is maintained at the level prior to the disturbance, guaranteeing a high quality output voltage. This is shown in Fig. 3.14(d) in which output voltage is being maintained at 70 volts

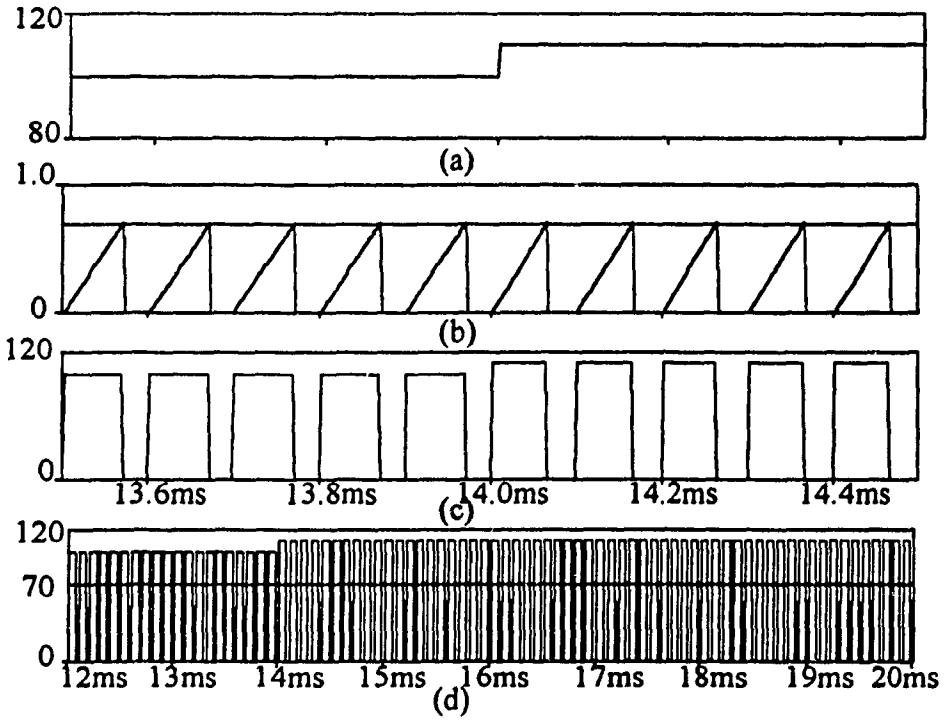


Fig. 3.14. Response of dc-dc converter for a 10% change in input voltage.(a) Input voltage. (b) Control waveforms. (c) Detailed view of output voltage (V_{OS}) and load voltage (V_O). (d) Output voltage (V_{OS}) and load voltage(V_O).

To improve the output voltage regulation, a feedback loop is included. The dynamic response of the system is studied by making a step change in the input and the reference voltage. The feedforward provides correction to the input disturbance in one cycle while the feedback loop ensures that the output tracks the reference change with zero steady state error. From simulation, two case studies for a 20% and 50% change in the input (at t=14ms) and 13% change in the reference (at t=20ms) are performed. The results are obtained for the conventional feedback system alone and the reset integral control with feedback control loop and shown in Fig. 3.15 and Fig. 3.16 respectively.

As clearly seen, RIC with a feedback loop gives a better performance in rejecting input source disturbance and has the same dynamics as the conventional feedback loop. While there is a distinct overshoot in the output voltage for an input change with feedback control, there is no visible change with the combined control strategy. Thus the input source disturbance is almost totally rejected in the output voltage, providing excellent voltage regulation for sensitive loads like computer power supplies.

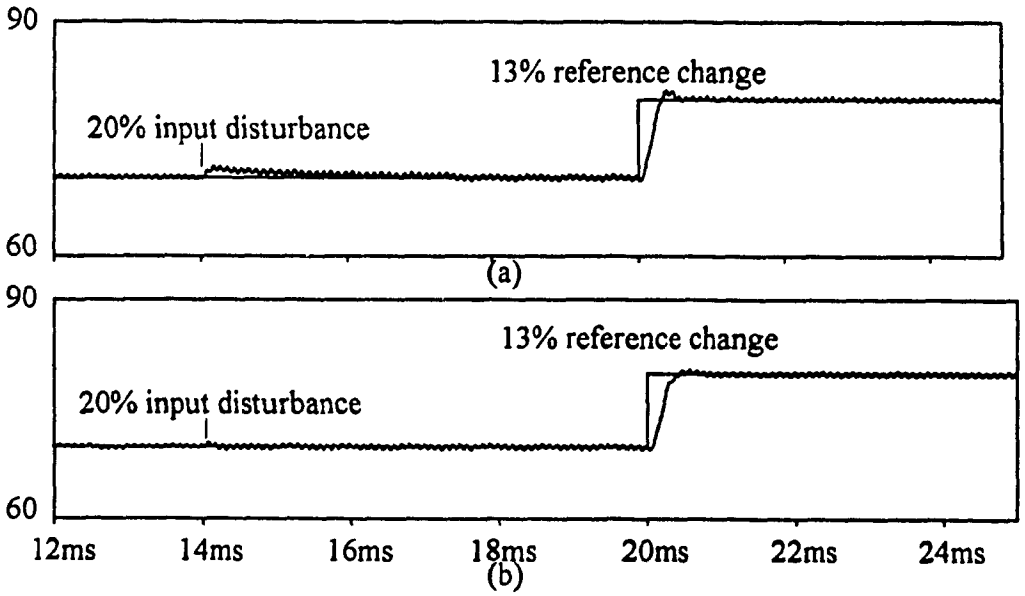


Fig. 3.15. Converter output voltage for a 20% change in input voltage and 13% change in reference. (a) Conventional feedback. (b) RIC with feedback loop.

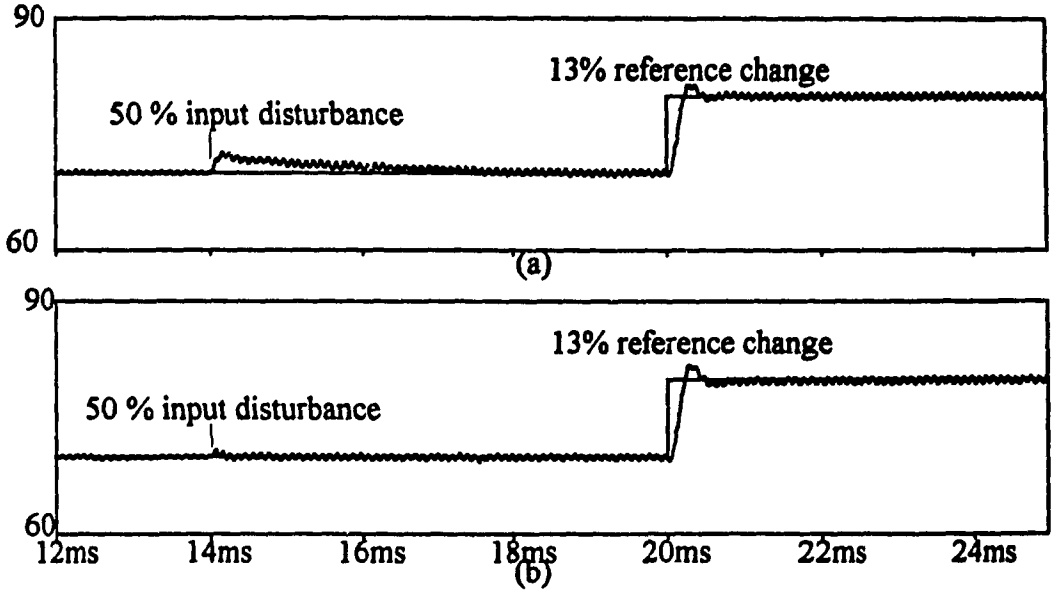


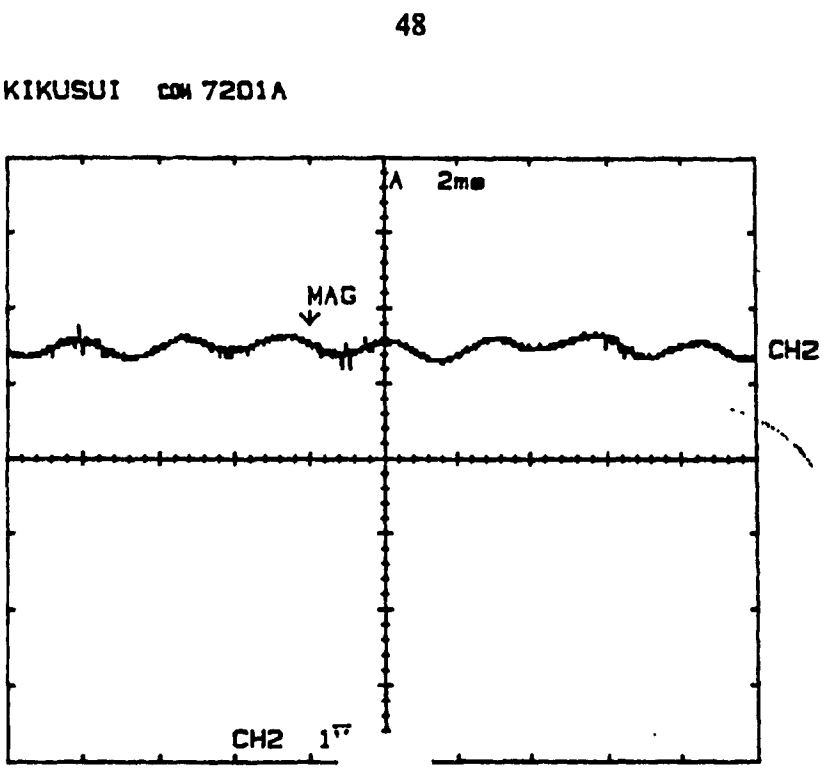
Fig. 3.16. Converter output voltage for a 50% change in input voltage and 13% change in reference. (a) Conventional feedback. (b) RIC with feedback loop.

3.3.5. Experimental results

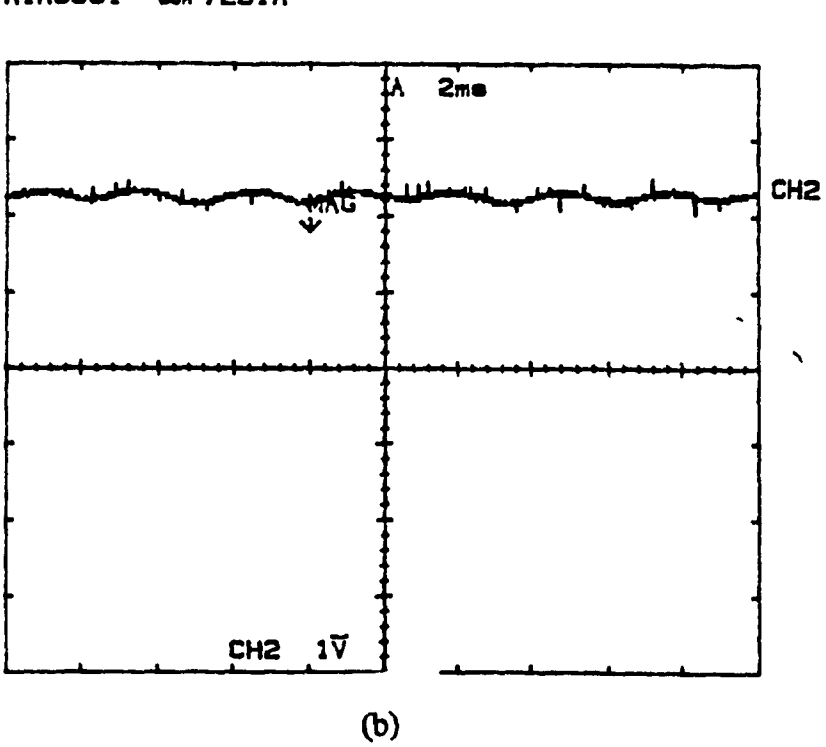
In order to verify the feasibility of the proposed schemes, a 1 kW, experimental prototype operating at 10 kHz ad 0.7 duty cycle is implemented. To incorporate the voltage drops across the output filter, a load voltage feedback loop was also included in the set-up.

In these schemes, the integral control acts as a feedforward loop and provides pre-regulation for the feedback loop. The system parameters include a resistive load of 6Ω and a integral time constant τ of 0.0765 ms. The PI controller parameters are k=1.44 and τ= 0.245ms. Experimental waveforms are shown in Figs. 3.17 through 3.20.

The complete load voltage waveforms are shown in Fig. 3.17. Fig. 3.18(a) shows the ac portion of the load voltage under openloop operating conditions. The waveform displays a dominant 360 Hz harmonic resulting from the diode bridge ac-dc conversion. Due to input source unbalances, 120 Hz is also present. techniques. Fig. 3.18(b) shows the voltage waveform when the load voltage feedback alone is incorporated.

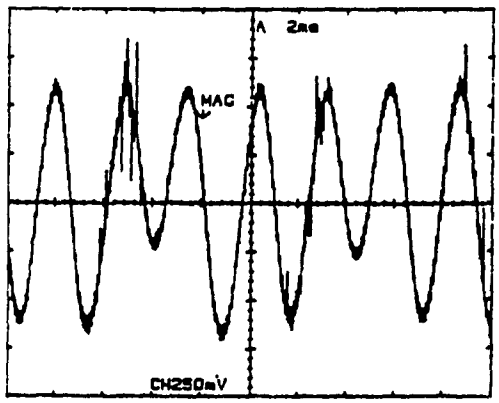


(a)

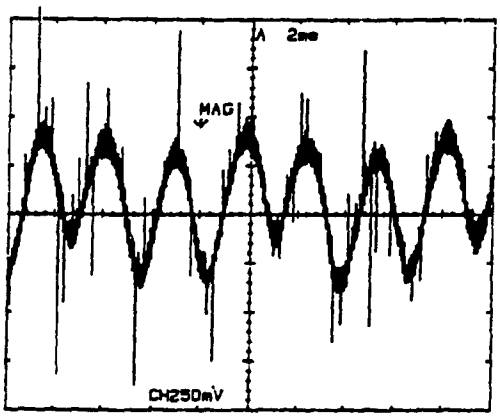


(b)

Fig. 3.17. DC output voltage (a) Open loop. (b) Feedback loop.



(a)



(b)

Fig. 3.18. AC component of dc output voltage. (a) Open loop. (b) Feedback loop

The integrator output and the switch gating signal under reset integral control are given in Fig. 3.19 (a) The load voltage waveform Fig. 3.19(b), shows a significant reduction in the ripple level as compared to the open-loop case. A further reduction is obtained with the combined reset integral control and feedback control strategy as shown in Fig. 3.19(c). The complete load voltage waveforms are shown in Fig. 3.20.

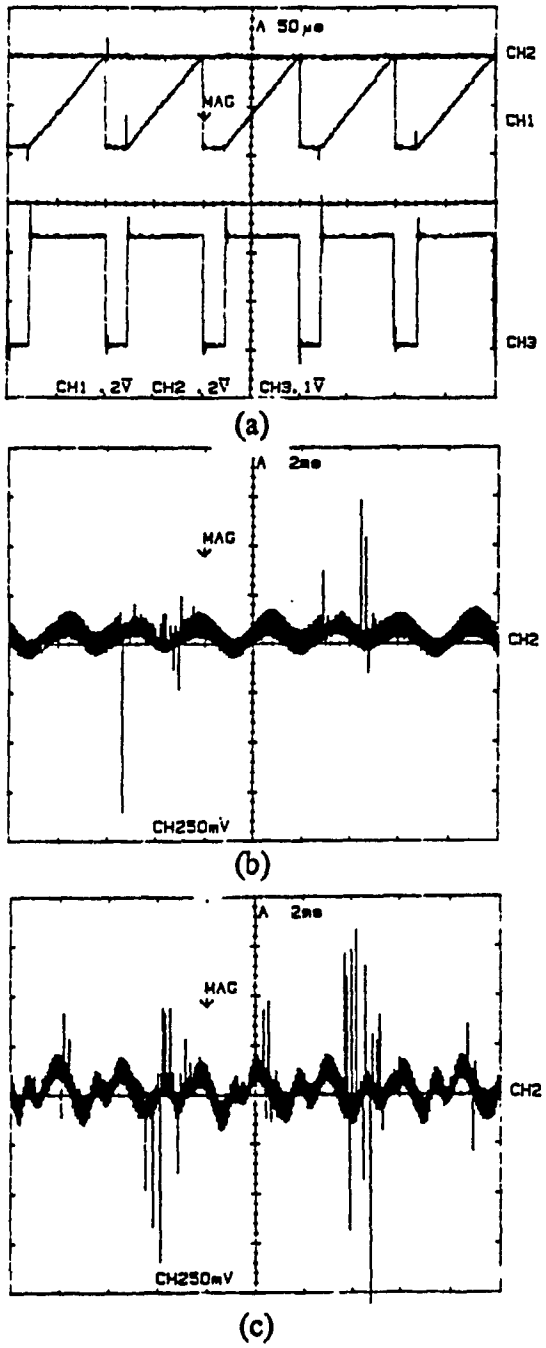


Fig. 3.19. Reset integral control. (a) Control waveforms. (b) AC component of the load voltage without feedback. (c) AC component of load voltage with feedback

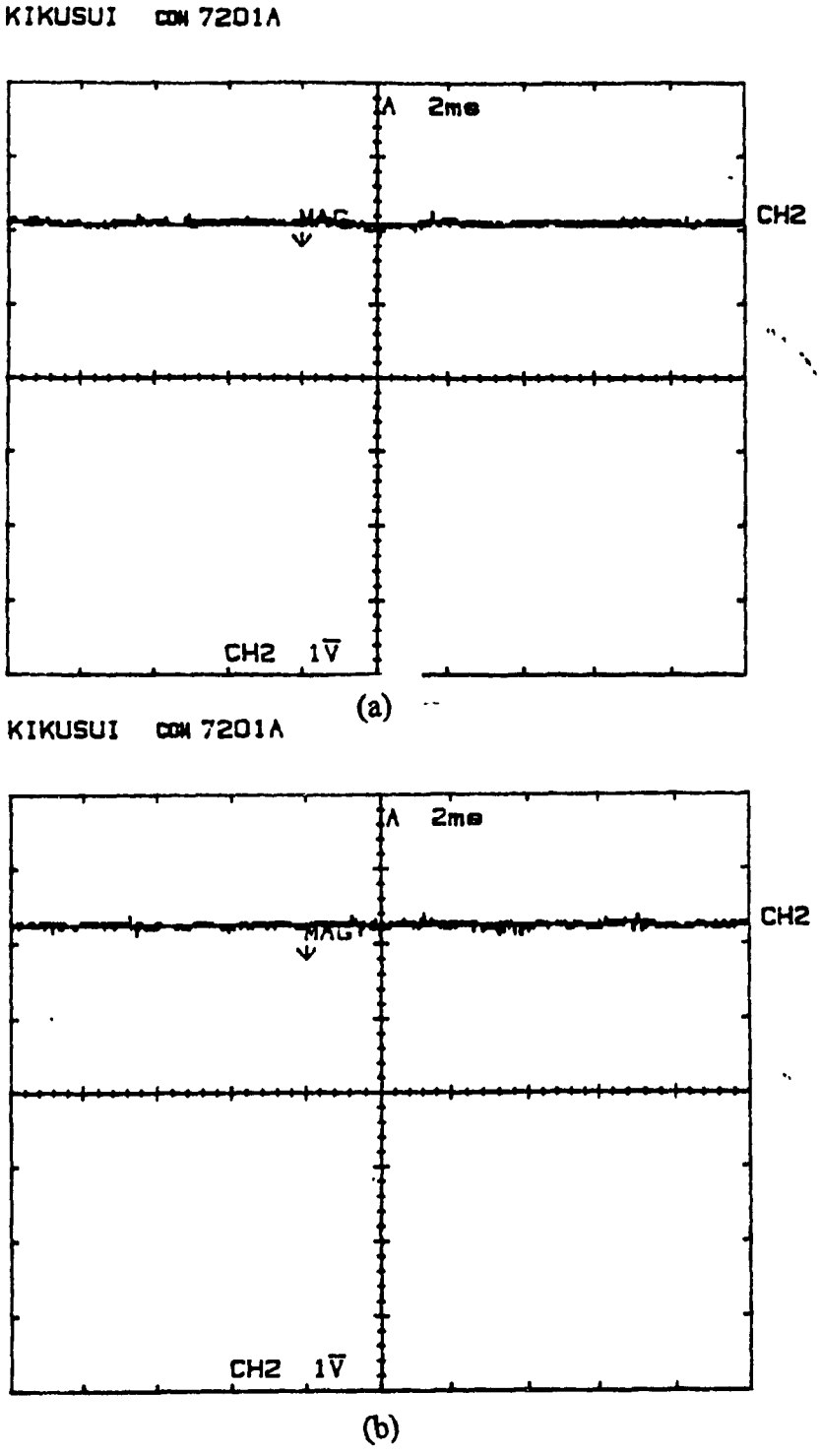


Fig. 3.20. Output voltage under reset integral control. (a) Without feedback. (b) With feedback.

3.4. Modulated Integral Control

Reset Integral Control technique works well as long as the switch is assumed to be ideal i.e. zero turn on and off delays. However in practice, switches have certain delays. As indicated in Table II section 1.2.2, turn off delays are greater than turn-on delays. This switching delay will introduce extra volt-seconds at the integrator output of the reset integral control, resulting in deviation of the output voltage away from the expected value This can have a significant effect on the performance of the converter especially when handling large output power.

To solve this problem, a Modulated Integral Control technique is proposed. The principle of the Modulated Integral Control was discussed in Chapter 2. Fig. 3.21 illustrates the complete schematic circuit diagram of the proposed Modulated Integral Control applied to a to a dc-dc buck converter.

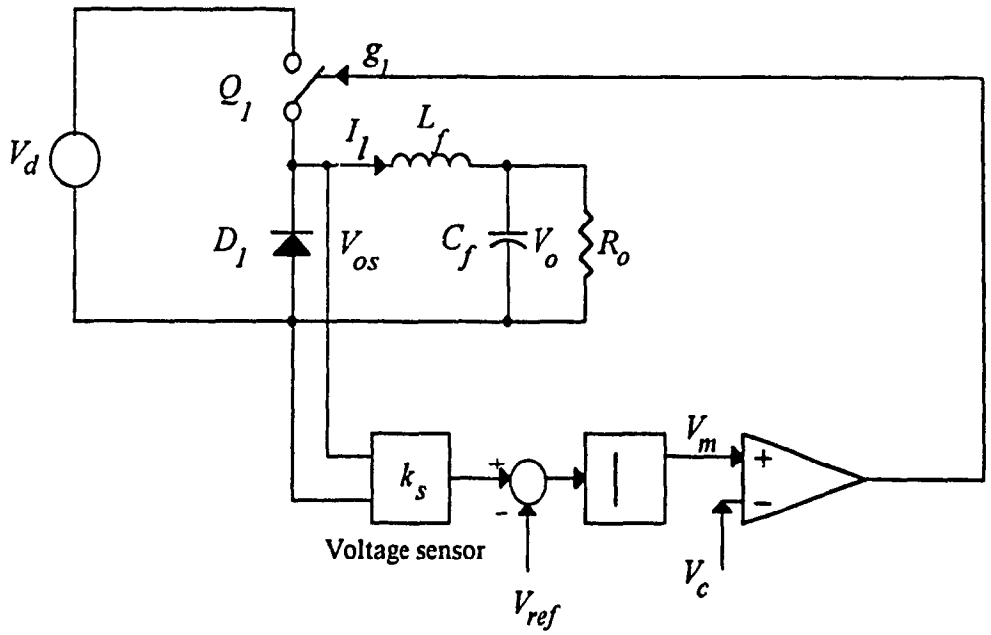


Fig. 3.21. Modulated Integral Control technique for a buck converter

3.4.1. Principles of operation

In Fig. 3.21, instead of integrating its output voltage V_{os} and resetting at the end of each period, the difference between the output voltage and the reference voltage is integrated. The integrator output is compared with a triangular carrier wave to generate the gating pulses. This is illustrated in Fig. 3.22.

While the switch is on, the integrator output has a positive slope. The intersection with the carrier waveform determines the turning off instant of the switch. Thereafter the slope of the integrator becomes negative and the intersection with the carrier waveform determines the turning on instant of the switch thus completing the switching cycle.

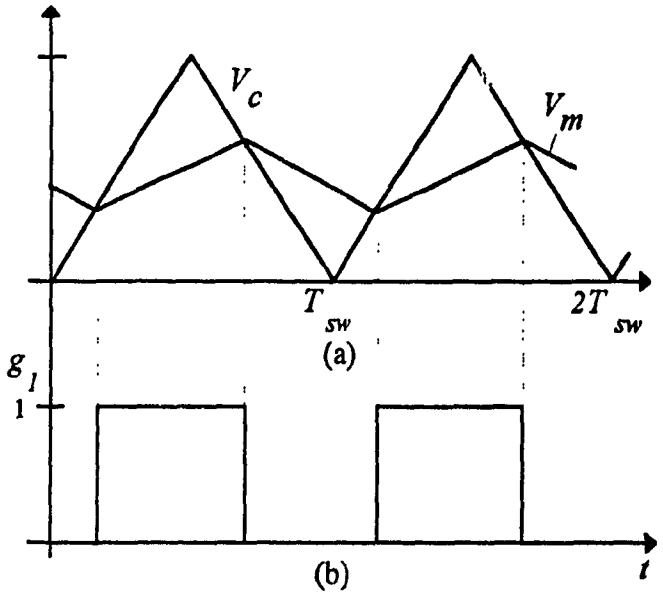


Fig. 3.22. Control waveforms for Modulated Integral Control technique

The major difference between this control technique and Reset Integral Control is that the integrator output is not reset in each period. Rather, the information from previous cycles is retained and utilized in the next period. In this way, any errors introduced by switching delays can be corrected. This is explained in detail in section 3.4.3.2.

3.4.2. Selection of the integrator time constant (τ)

This section outlines the design procedure for choosing the integrator time constant (τ). The design is carried out for an ideal dc bus and a non-ideal dc bus.

3.4.2.1. Ideal dc bus

As seen from the Fig. 3.22, the condition necessary to ensure constant frequency operation is that the slope of the carrier (m_c) must be greater than the rising (m_r) and falling (m_f) slopes of the modulation wave at all times.

The rising slope occurs when the switch is on and can be given by:

$$m_r = \frac{k_s V_{dc} - V_{ref}}{\tau} \tag{3.16}$$

The falling slope of the modulation occurs when the switch is off and can be expressed as:

$$m_f = \frac{V_{ref}}{\tau} \tag{3.17}$$

Let the amplitude of the carrier wave be V_c and frequency f_{sw}. The amplitude of the carrier is chosen such that :

$$V_c = k_s V_{dc} \tag{3.18}$$

The slope of the carrier is given by:

$$m_c = 2V_c f_{sw} \tag{3.19}$$

In order to satisfy the slopes conditions, we have

$$2V_c f_{sw} > \frac{k_s V_{dc} - V_{ref}}{\tau} \tag{3.20}$$

and

$$2V_c f_{sw} > \frac{V_{ref}}{\tau} \tag{3.21}$$

Let the converter operate at DC duty cycle D which is expressed as

$$D = \frac{V_{ref}}{k_s V_{dc}} \tag{3.22}$$

Using (3.22), eqns. (3.20) and (3.21) can then be written as:

$$\tau > \frac{1-D}{2f_{sw}} \tag{3.23}$$

and

$$\tau > \frac{D}{2f_{sw}} \tag{3.24}$$

The value of integrator time constant should thus satisfy the larger of (3.23) and (3.24).

3.4.2.2. Non-ideal dc bus

The non-ideal dc bus is given by (3.2). The presence of input harmonics affect the rising slope of the modulation slope. The maximum input voltage can now be written as $k_s V_{dc}(1+k_r)$. Substituting in the slope conditions and rearranging, (3.20) can then be written as:

$$\tau > \frac{1-D+k_r}{2f_{sw}} \tag{3.25}$$

The integrator time constant now is larger of the values given by (3.24) and (3.25). A dc-dc converter considered in section 3.3.2.3 is designed to operate under MIC. For a non-ideal dc bus with k_r=0.1 and operating at a duty cycle of 0.7, the value of integrator time constant satisfying (3.24) and (3.25) is

$$\tau > 35\mu\text{sec} \tag{3.26}$$

$$\text{Choose } \tau = 50\ \mu\text{sec} \tag{3.27}$$

3.4.3. Steady state results.

In this section steady state results are presented for a dc-dc converter operating under modulated integral control. The performance is indicated for ideal dc bus and non-ideal dc bus.

3.4.3.1. Ideal dc bus

From the design values obtained in the previous section, the converter in Fig. 3.21 was simulated and steady state results presented in Fig. 3.23. The results obtained are satisfactory and comparable with that obtained from open loop in Fig. 3.8.

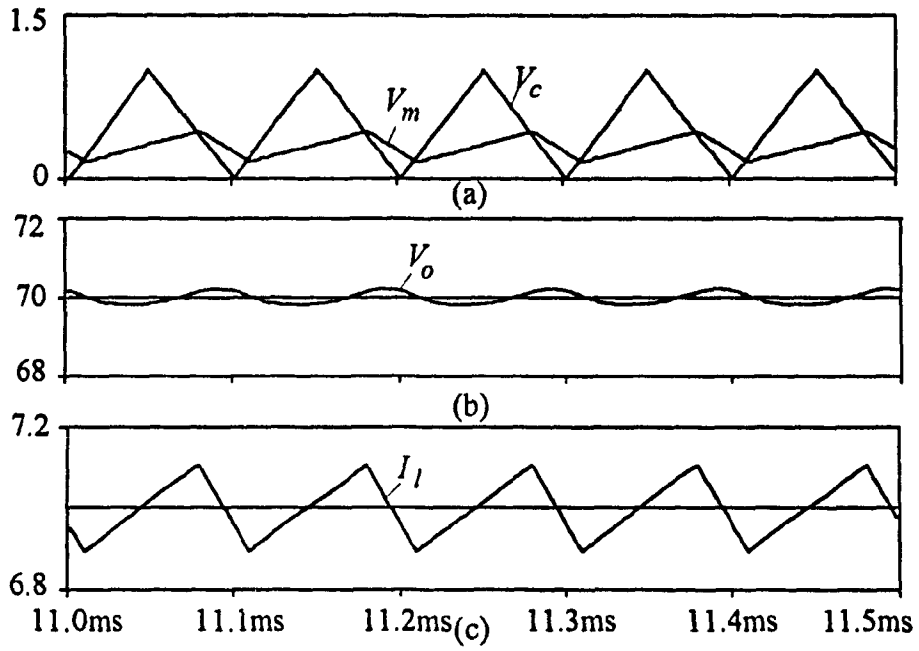


Fig. 3.23. Modulated Integral Control. (a) Control waveforms. (b) Load voltage. (c). Inductor current. (D=0.7)

3.4.3.2. Compensation of switching delays

In conventional feedforward control techniques only input voltages are measured and the behavior of switching devices is not taken into consideration in the

implementation. In particular switching delays can degrade the performance of feedforward control.

This is illustrated in Fig. 3.24 in which a buck converter under open loop conditions is simulated with a switching turn-off delay of 10μsec. This causes an increase in the output volts-sec resulting in a higher mean voltage which is undesirable.

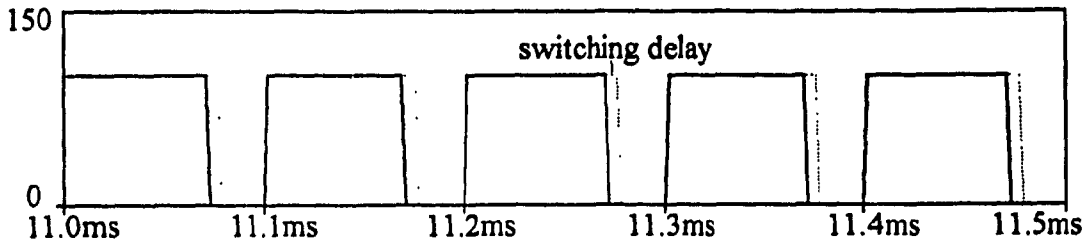


Fig. 3.24. Output voltage(V_{os}) with switching delay in open loop buck converter

The proposed Modulated Integral Control technique can easily solve this problem. This is seen from Fig. 3.25 and 3.26. Any switching delay causes an increase of the integrator output beyond its intersection with the carrier wave. Consequently the modulation wave is shifted upwards, giving a narrow pulse for the off pulse in the next half switching period. The overall effect is thus to shift the gating pattern with respect to the original pattern compensating the effect of the switching delay. The output voltage is undeviated from the original design, no matter how large the switching delay is. This results in a superior performance of the converter system.

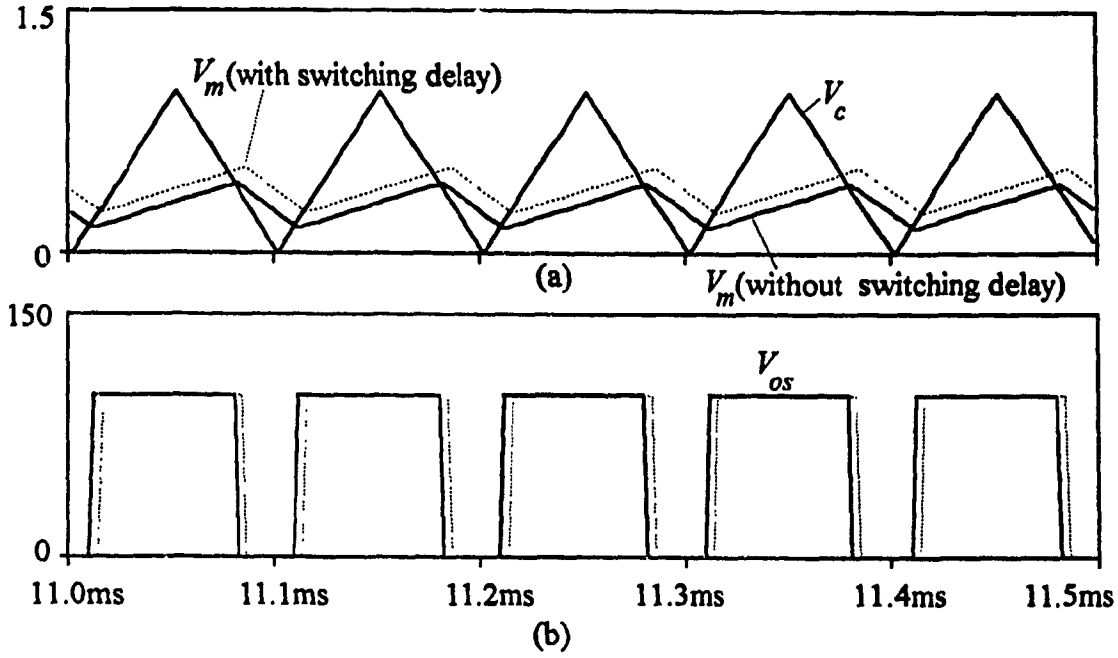


Fig. 3 25. Switching delay compensation using modulated integral control (a) Control waveforms (with and without delays).(b) Output voltage(V_{os})

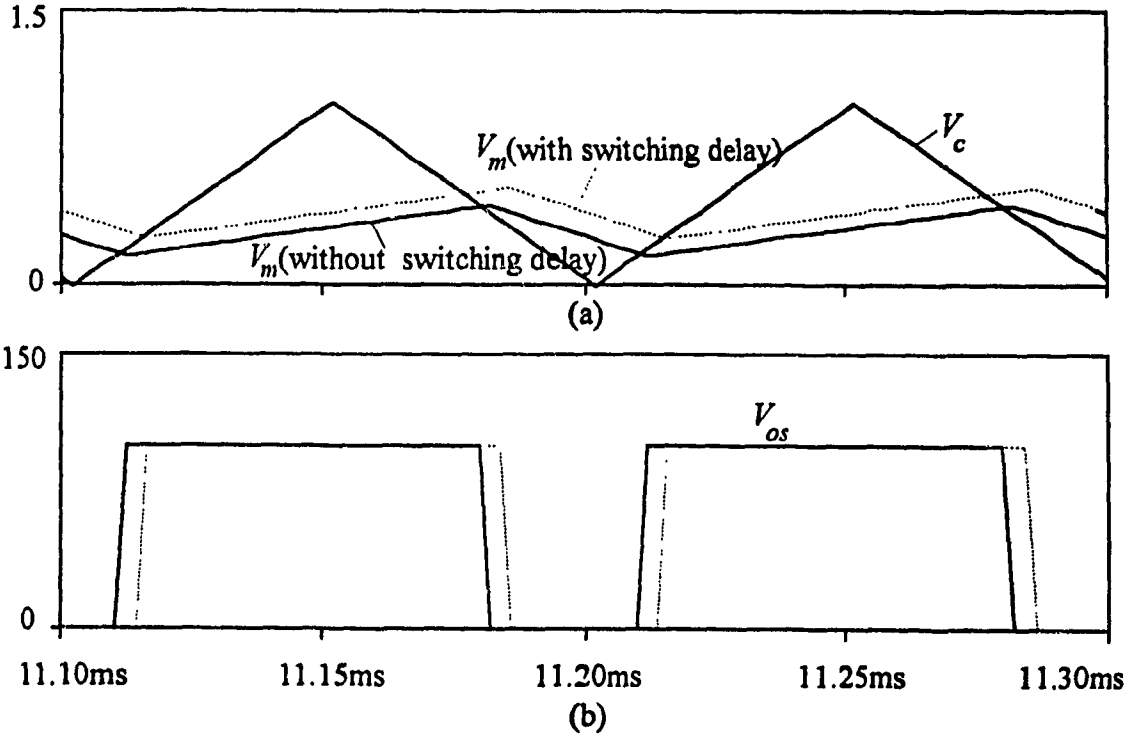


Fig. 3.26. Switching delay compensation using modulated integral control (detailed view) (a) Control waveforms (with and without delays).(b) Output voltage(V_{os})

3.4.3.3. Non ideal dc bus

A dc-dc converter designed in section 3.4.2.2. is simulated in PECAN under modulated integral control. The dc bus is assumed to have a single dominant harmonic at 360 Hz. Steady state results are presented in Fig. 3.27 The output voltage shows the appearance of harmonic in the output. However it is attenuated to a large extent and can be seen from the harmonic spectrum of the output voltage (Fig. 3.28).

Thus the modulated integral control technique provides good compensation for the harmonic voltages in the dc bus. However a comparison of Fig. 3.28(b) and Fig. 3.11(b) reveals that the RIC provides better harmonic attenuation than MIC.

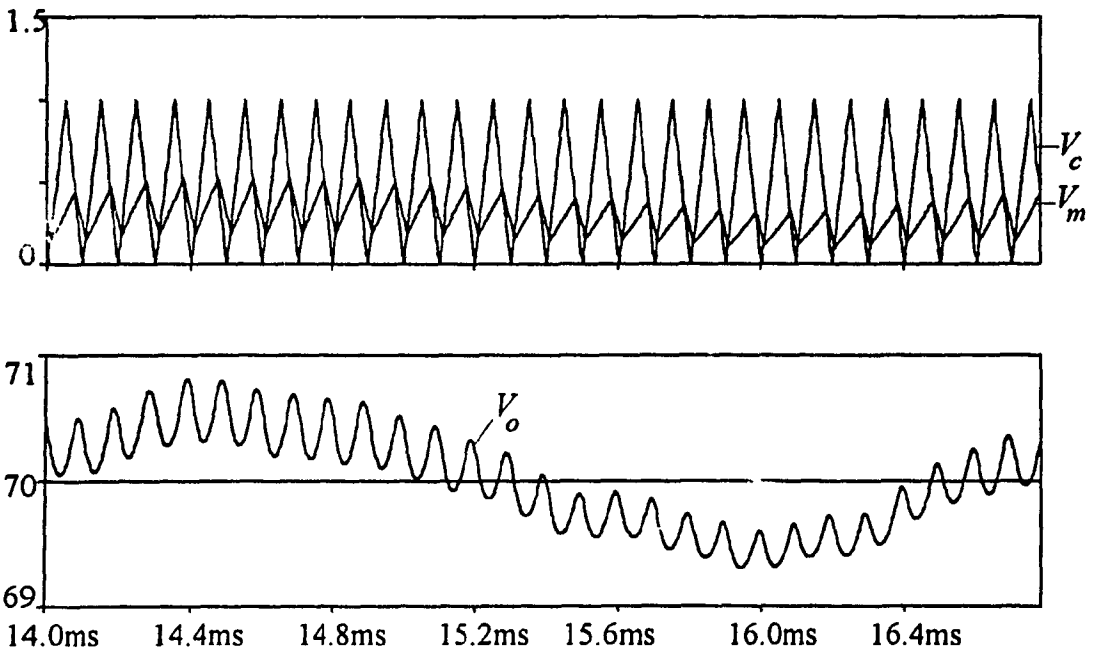


Fig. 3.27. Steady state results for a dc-dc converter operating under a non-ideal dc bus (a) Control waveforms. (b) Output voltage (detailed view)

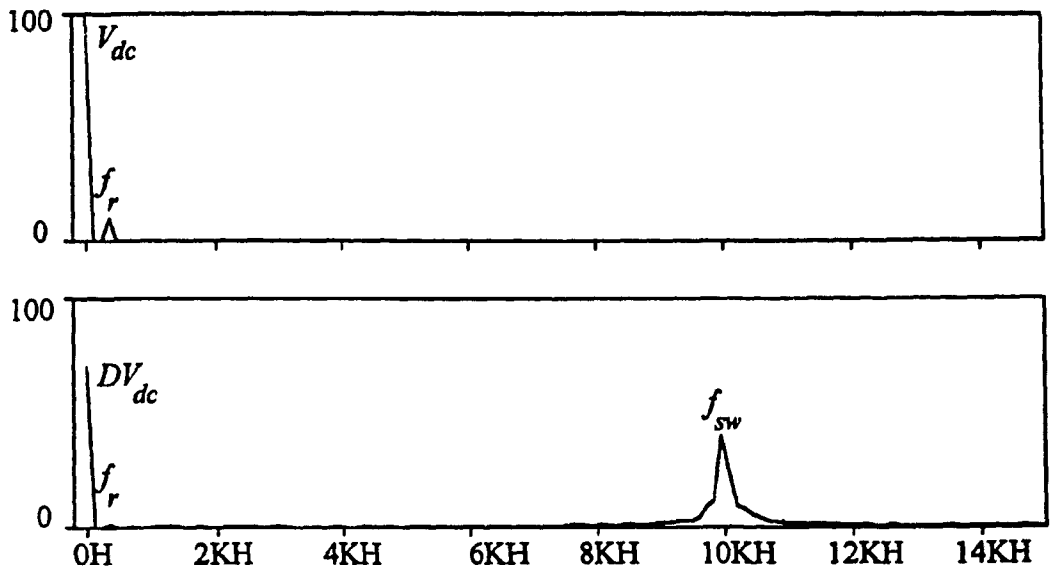


Fig. 3.28. Operation of dc-dc converter with a non-ideal dc bus. (a) Input voltage spectrum. (b) Output voltage spectrum (f_r=360 Hz, f_{SW}=10 kHz, D=0.7)

In order to evaluate the harmonic reduction of the modulated integral control quantitatively, a harmonic attenuation factor, K_h defined as the ratio of the output and input harmonic amplitudes is used.

To calculate the harmonic attenuation factor under modulated integral control, the switching function $f(t)$ (Appendix) is used. For a given input $V_d(t)$, the output voltage can be computed using (3.15) and K_h calculated.

This factor is obtained as a function of the duty cycle and the ratio of source to switching frequency and is plotted in Fig. 3.29. It shows that the harmonic attenuation higher as the ratio of the input harmonic frequency to the switching frequency increases.

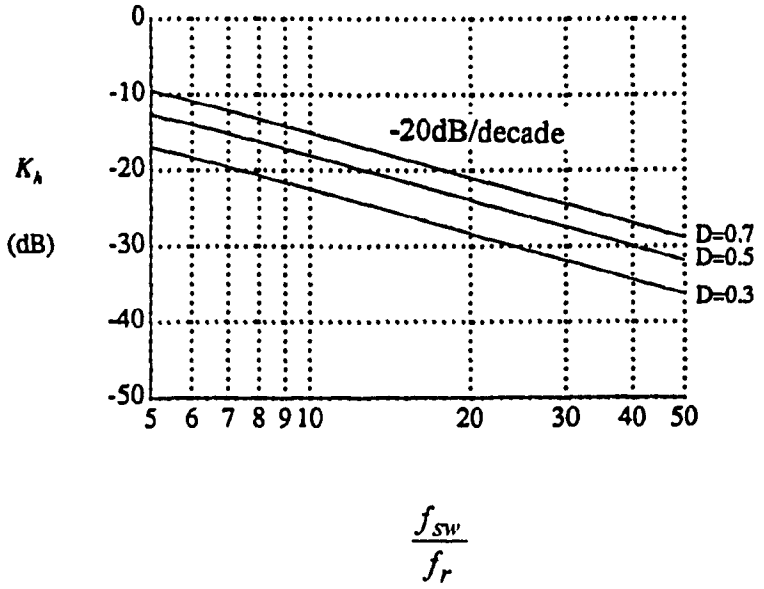


Fig. 3.29. Harmonic attenuation of modulated integral control

3.4.4. Experimental Results

Fig. 3.30(a) shows the carrier wave, the modulating wave and gating signals under the modulated integral control. With this scheme, the ac component of experimental output voltage with and without feedback is shown in Figs. 3.30(a)&(b). The dc load voltage waveforms are shown in Fig. 3.31.

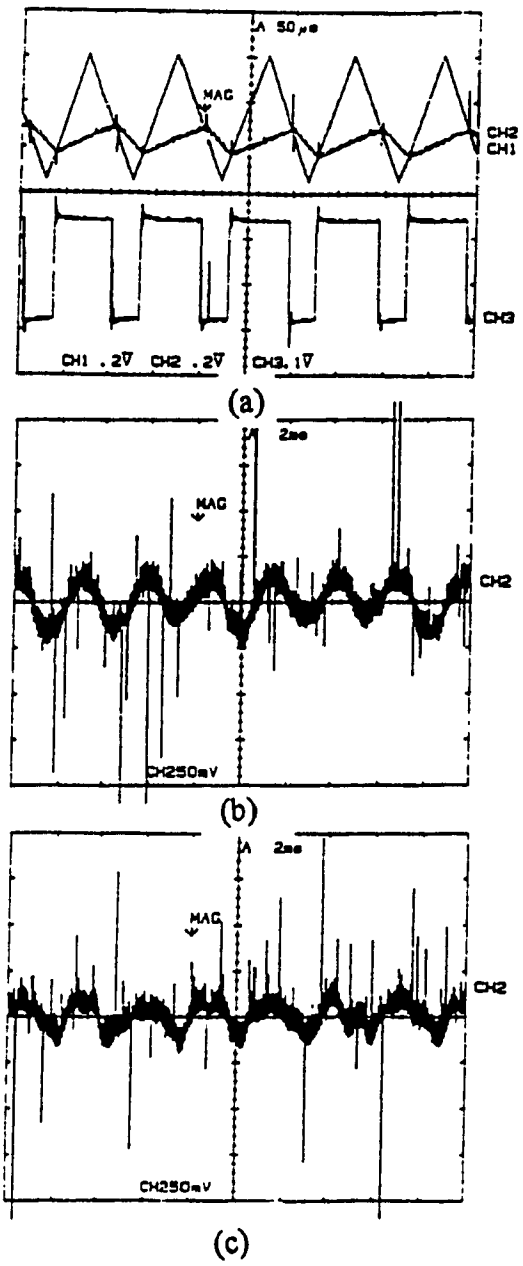


Fig. 3.30. Modulated integral control. (a) Control waveforms. (b) AC component of the load voltage without feedback. (c) AC component of load voltage with feedback

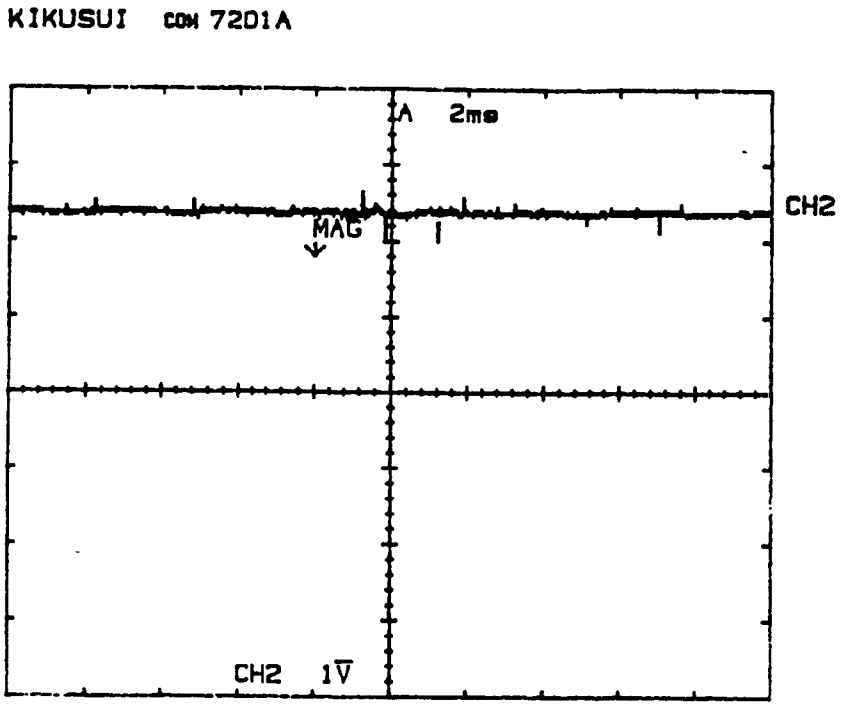


Fig. 3.31. Output voltage under modulated integral control with feedback.

3.5. Conclusions

In this chapter, two control techniques, reset integral control and modulated integral control have been analyzed for a dc-dc converter. Studies show that both techniques retain the advantages of the conventional feedforward technique. In addition they provide good output DC regulation with the ability to correct the errors due to the switch conduction drops. Furthermore, the modulated integral control also compensates for the errors in the output voltages due to the switching delays. Experimental results confirm the feasibility of the proposed techniques.

CHAPTER 4

PWM PATTERN GENERATORS FOR THREE PHASE VOLTAGE SOURCE INVERTERS

4.1. Introduction

Output harmonic minimization in standard PWM pattern generators is based on the assumption that the input dc bus voltage is ripple free and the semiconductor devices are ideal. However as discussed in detail in section 1.2, in a practical converter system it is difficult to realize an ideal dc bus and power switches. This deteriorates the quality of the inverter output voltage by introducing undesirable low order harmonics which are difficult to filter.

The output voltage integral control technique, introduced in the Chapter 2 and successfully implemented for a dc/dc converter in Chapter 3, is the basis of the PWM pattern generators proposed in this chapter. The purpose of these pattern generators is to inherently take into account the non-ideal conditions present in a switching converter and generate control signals for obtaining high quality sinusoidal output voltages. Based on either the reset integral or modulated integral control technique, two different pattern generators are analyzed and implemented. The principles of operation are explained. The features illustrated through simulation examples clearly bring forth the advantages as compared to the standard sinusoidal PWM (SPWM) output. Experimental results obtained on a 3kVA laboratory prototype confirm the feasibility and effectiveness of the proposed pattern generators.

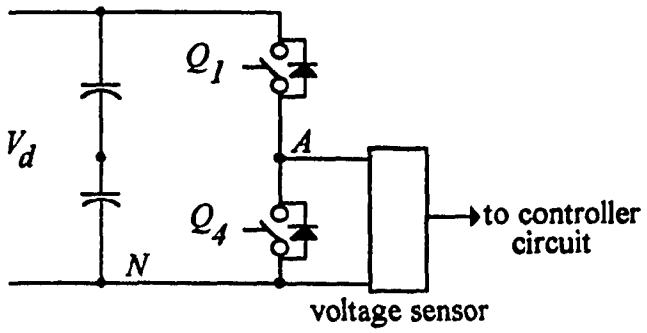


Fig. 4.1. Location of voltage sensor in dc/ac converters

4.2 Implementation aspects

There are two important aspects associated with the proposed pattern generators which need to identified before implementation:

1. Location of voltage sensor
2. Choice of reference voltage

4.2.1. Location of voltage sensor

In a dc-ac converter, the sensor can be placed across the dc bus and the gating signal generated through the pattern generator. Thus only one sensor is needed.

On examining the voltage across the bottom switch (Q_4), it is noted that when the top switch is on, it is the dc bus voltage less the conduction drop of the top switch i.e.

$$V_{AN} = V_d - V_{con,Q_1} \tag{4.1}$$

The voltage across the bottom switch has information regarding the dc bus ripple and one switch conduction drop can be taken into consideration and correction applied to the gating pattern.

Thus for a dc-ac converter the voltage across the bottom switch is identified to be the location of the sensor, Fig. 4.1. Also the harmonic spectra of the output voltage is related to that of the voltage across the bottom switch. This is illustrated in Fig. 4.2. The harmonics in the switch voltage are 0.577 times the line harmonics, with the harmonics at

switching frequency and multiples and certain side bands present. Thus by controlling the voltage across the bottom switch, one can regulate the output line voltage and justifies the location of the sensor.

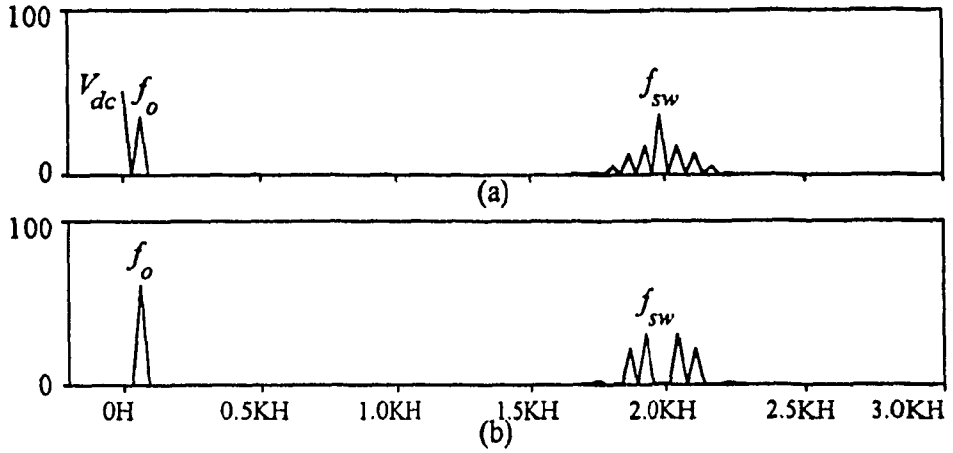


Fig. 4.2. Voltage harmonic spectra. (a) Voltage across bottom switch (b) Line voltage (f_{SW}=33pu M=0.7)

4.2.2. Choice of reference control voltage

The proposed techniques based on output voltage integral control require a reference control voltage. In a dc/dc converter a dc voltage was chosen as the reference. For a voltage source inverter since the desired output is a sinusoidal voltage and the voltage across the bottom switch is chosen as the controllable parameter, a sinusoidal voltage with a frequency equal to the fundamental frequency of the output (f_o) and having a dc bias (Fig. 4.3) is chosen as the reference i.e.

$$V_{ref} = V_{bias} + V_m \sin(2\pi f_o t) \tag{4.2}$$

The bias voltage can be chosen at will by the designer and is dependent only on the type of the analog/digital circuitry used for implementation. This aspect will be covered in detail in the design section.

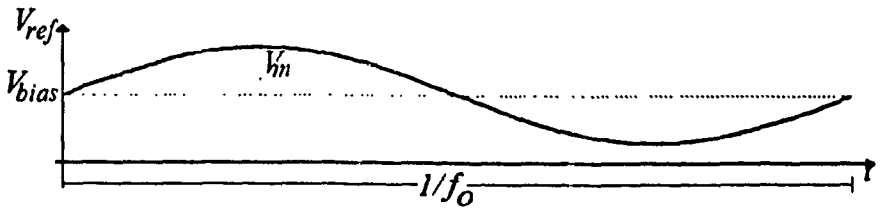


Fig. 4.3. Reference voltage for a dc/ac converter

4.3. Reset Integral controller

This section covers the performance of a three phase voltage source inverter gating signal for which are obtained from a PWM pattern generator based on reset integral control technique discussed in section 2.3. This technique is capable of compensating for dc bus harmonics by attenuating the low-order harmonics appearing in the output voltage.

4.3.1. Structure of the proposed pattern generator

The feasibility of the proposed pattern generator is first illustrated with a half bridge inverter. The three phase implementation is realized by independently controlling each inverter leg as a half bridge inverter.

4.3.1.1. Half bridge inverter

The proposed pattern generator in Fig. 4.4, has a closed loop structure and requires sensing of the instantaneous value of the voltage across the bottom switch. This voltage is applied to a resettable real-time integrator whose output is compared to a reference signal which is a sinusoidal voltage with a dc offset. As it reaches the reference, indicating that the output volt-sec has reached the desired value, switch Q_1 is turned off and the integrator output is reset. The bottom switch Q_4 is turned on thus inhibiting the input to the integrator whose output is clamped to zero until the end of the fixed switching period (T_{SW}). The gating signal for the bottom switch is complementary of the gating signal for the top switch. The waveforms are shown in Fig. 4.5.

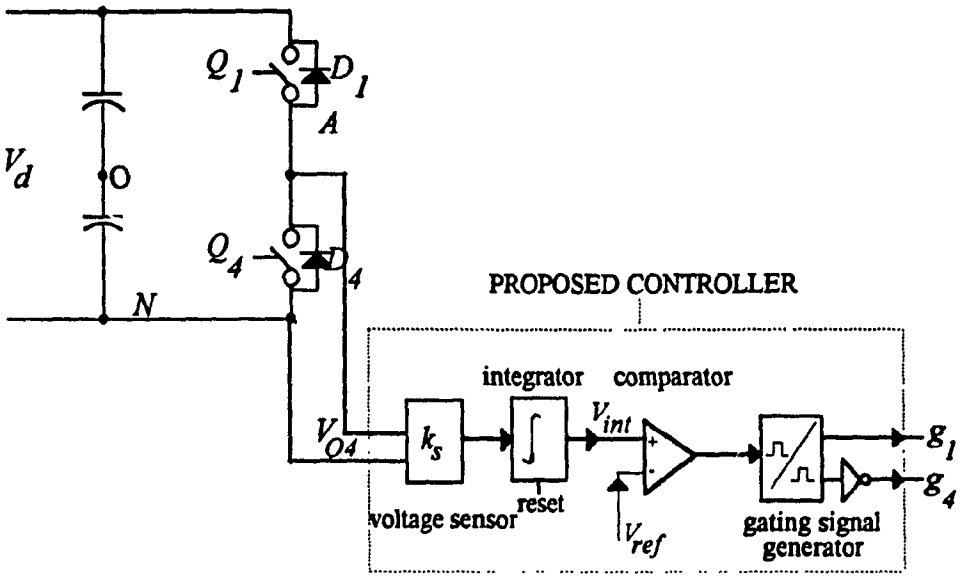


Fig. 4.4. Proposed pattern generator for half bridge configuration.

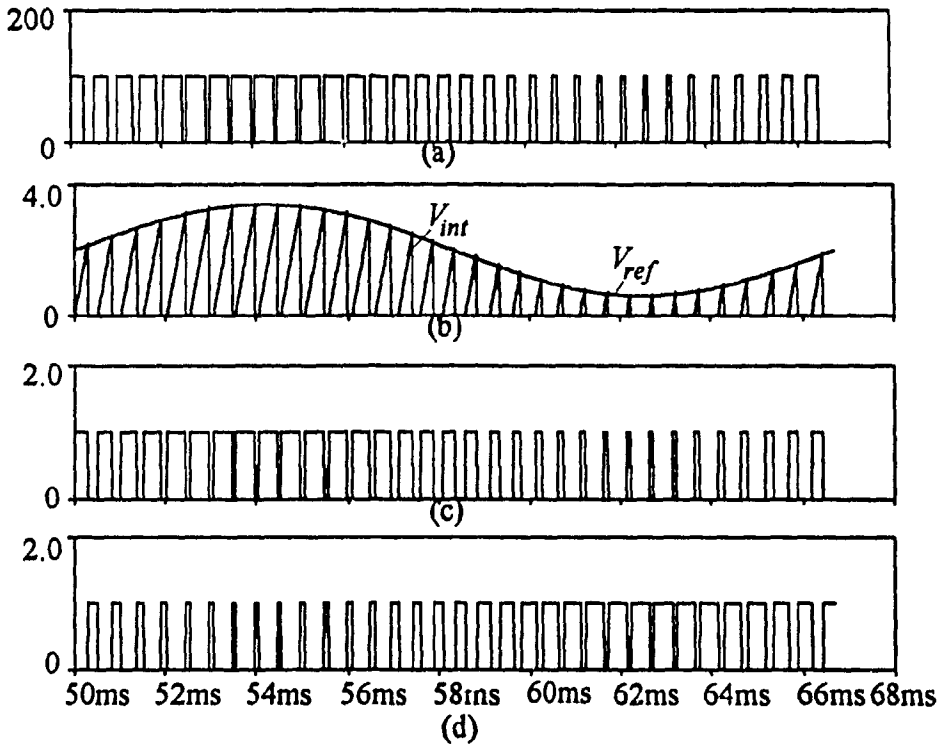


Fig. 4.5. Waveforms for a half bridge inverter. (a) Voltage across the bottom switch (V_{Q4}). (b) Integrator output (V_{int}) and control reference ($Vref$). (c) Gating signal for the top switch (g_1) (d) Gating signal for the bottom switch (g_4)

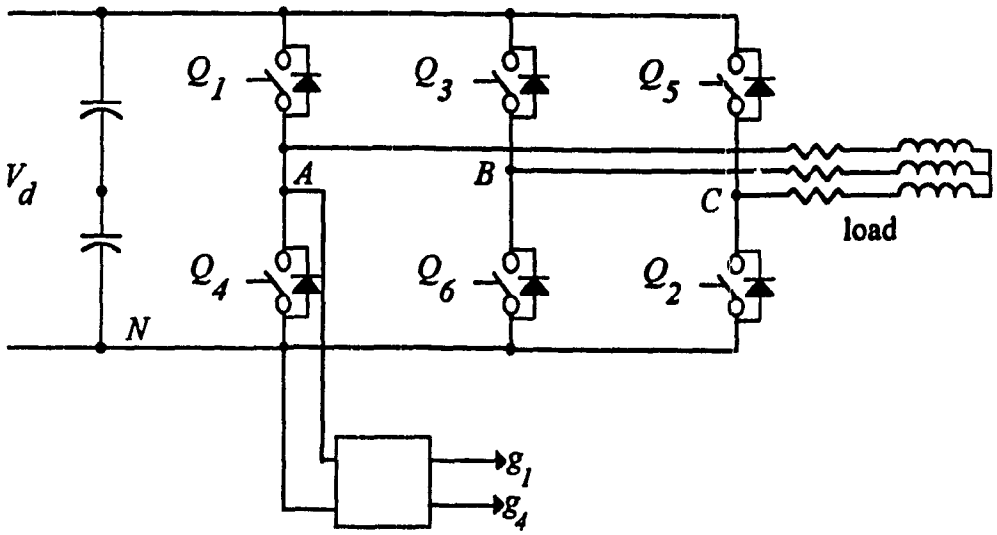


Fig. 4.6. Proposed pattern generator for a three-phase inverter.

4.3.1.2. Three phase operation

The proposed PWM pattern generator is implemented for a three phase voltage source inverter, Fig. 4.6. It comprises three independent modulators of Fig. 4.4 placed across the bottom switch of each inverter leg. Since in a three phase system, any two line voltages are phase shifted, three sinusoidal control references (V_{refa}, V_{refb}, V_{refc}) with a dc bias and phase shifted 120° are chosen.

As can be seen in Fig. 4.6, the voltage across the bottom switches (V_{AN},V_{BN},V_{CN}) are being controlled. The line voltage can be constructed as:

$$V_{XY} = V_{XN} - V_{YN} \tag{4.3}$$

where $X = A,B,C$; $Y = A,B,C$

Thus by controlling each phase independently and ensuring sinusoidal voltage, a high quality output line voltage can be guaranteed.

The waveforms associated with the proposed three-phase pattern generator are shown in Fig. 4.7.

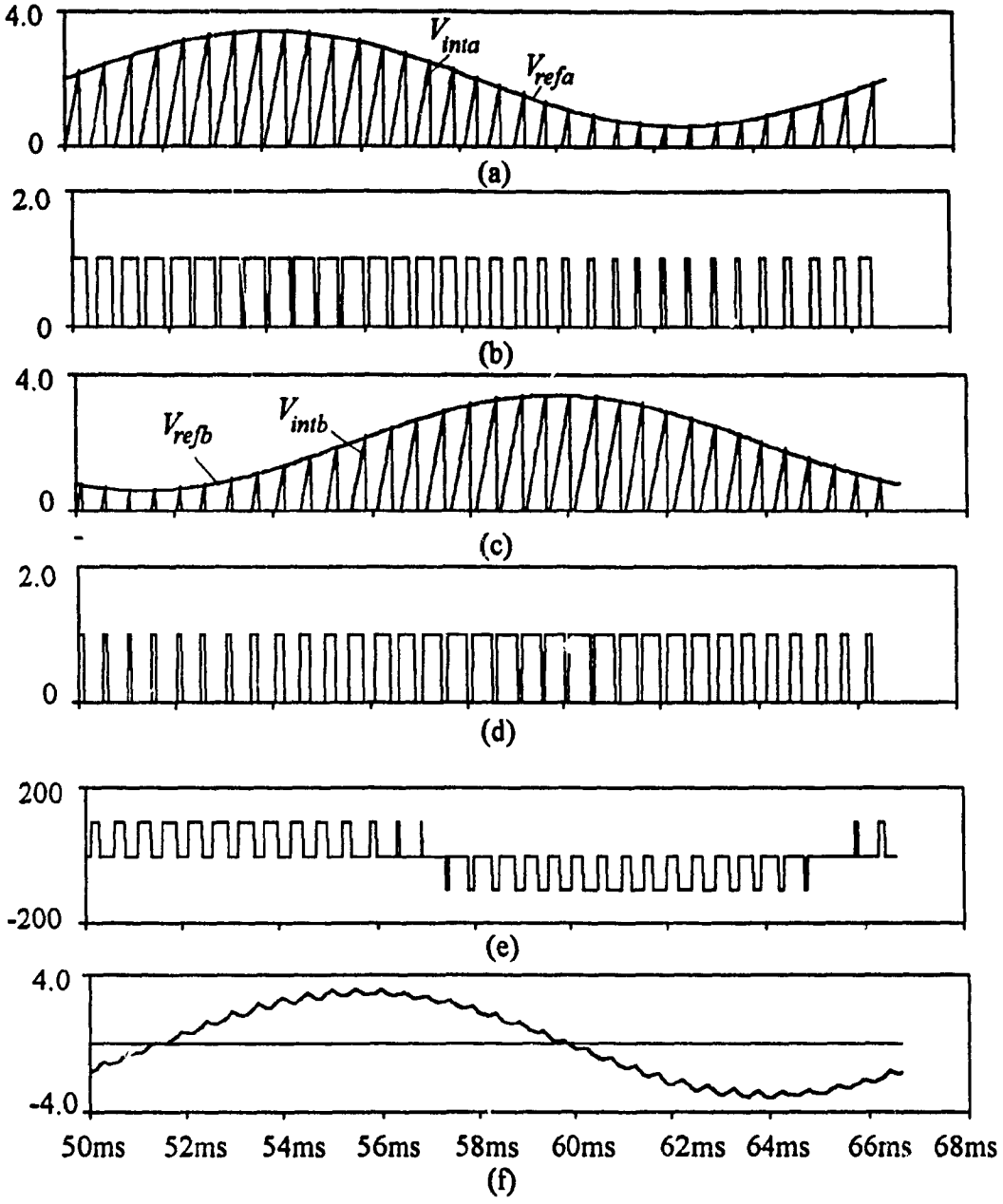


Fig. 4.7. Waveforms for three phase inverter. (a) Control waveforms for phase A. (b) Gating signal for switch Q_1. (c) Control waveforms for phase B. (d) Gating signal for switch Q_3. (e) Line voltage. (f) Line current.

(M=0.7, f_{sw}=33pu)

4.3.2. Principle of compensation

The voltage across the bottom switch is integrated at a constant frequency and is determined as:

$$\begin{aligned} V_{AN} &= V_d \quad \textit{top switch on} \\ &= 0 \quad \textit{bottom switch on} \end{aligned} \tag{4.4}$$

The voltage across the bottom switch being the input to the controller, the slope of integration is proportional to the instantaneous value of the input voltage. The integrator output is continuously compared with a sinusoidal control reference. Depending on the magnitude and frequency of the dominant ripple voltage, the input dc bus voltage varies in magnitude. When the input is higher, the rate of integration is faster and hence the integration value reaches the reference faster generating a narrow pulse width. On the other hand when the input is lower a wider pulse is generated. The PWM pattern generated by this on-line real time integration is a function of the non-ideal dc bus and the pulse width generated by virtue of comparison with a sinusoidal reference voltage, ensures a sinusoidal volt-sec distribution in the output voltage in each cycle. Thus the proposed modulator can inherently compensate for the ripple in the dc bus. This improves the performance of the VSI without resorting to complex control circuitry.

4.3.3. Design guidelines

This section develops the key design equations necessary in analyzing the performance and implementing the proposed pattern generator. A design example is presented and is used in simulation studies performed in PECAN.

4.3.3.1. Ideal dc bus

The key element in the proposed pattern generator is the integrator with a time constant τ, whose value is dependent on the system parameters. The dc bus is assumed to

be ideal, i.e. with no ripple. The compromise made in the performance with a non-ideal dc bus is discussed in detail in section 4.3.4.1.4. The input to the integrator being the voltage across the bottom switch, a sinusoidal reference with a dc offset (4.2) is chosen.

The modulation index (M) is then defined as

$$M = \frac{V_m}{V_{bias}} \tag{4.5}$$

Let f_{sw} be the switching frequency of the inverter and k_s the gain of the voltage sensor. The integrator output is given as:

$$V_{int} = \frac{k_s V_{dc}}{\tau} t \tag{4.6}$$

The time constant is selected so as to integrate to the maximum control voltage ($V_m + V_{bias}$) in one switching period ($T_{sw} = 1/f_{sw}$). Thus,

$$\frac{k_s V_{dc} T_{sw}}{\tau} = V_m + V_{bias} \tag{4.7}$$

Rearranging the above equation and choosing the worst case when $M = 1.0$, we obtain the integrator time constant as

$$\tau = \frac{k_s V_{dc} T_{sw}}{2 V_{bias}} \tag{4.8}$$

4.3.3.2. Design Example

In order to apply the design expressions obtained in the previous section, a three phase inverter is designed according to the following specifications:

- Input dc bus voltage V_{dc} = 100 volts
- Inverter output frequency, f_i= 60 Hz
- Voltage sensor gain, k_s= 1.0
- DC offset in the control reference, V_{bias} = 2 V

Using (4.8), the integrator time constant τ can be obtained as:

$$\tau = 25T_{sw} \tag{4.9}$$

Thus the integrator time constant is a function of the switching frequency. Since the performance of the inverter is evaluated at different frequencies, the design curve in Fig. 4.8 is used to choose the time constant for a given value of dc bus and control voltage. These values were then used to simulate the inverter in PECAN.

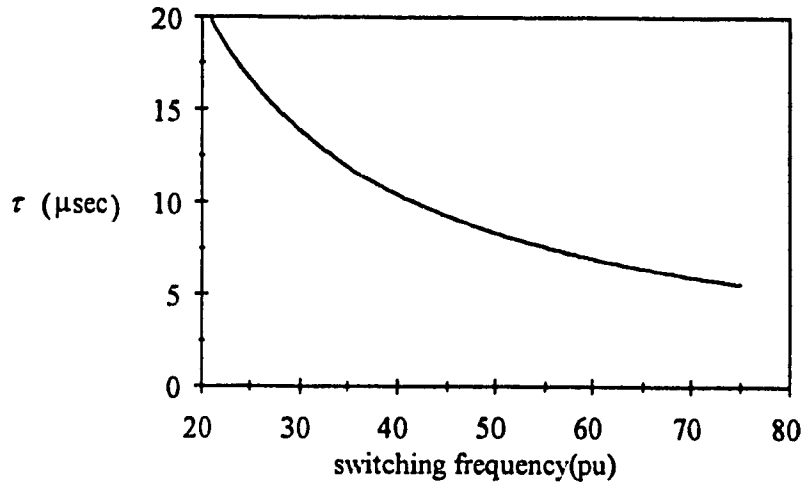


Fig. 4.8. Design curve. Integrator time constant (τ) versus switching frequency (fsw)

4.3.4. Performance analysis

This section provides an in-depth performance analysis of the proposed PWM pattern generator. The main objectives are to illustrate the feasibility and effectiveness of the pattern generator under steady state and transient conditions with ideal and non-ideal dc bus. In each case the comparison is done with the conventional and most widely used pattern generator based on sine pulse width modulation (SPWM) under similar conditions.

4.3.4.1. Steady State

The three phase inverter in Fig. 4.6 was simulated under steady state conditions. The performance assessment is done on the basis of the quality of the output fundamental voltage and current and voltage gain at different modulation indices.

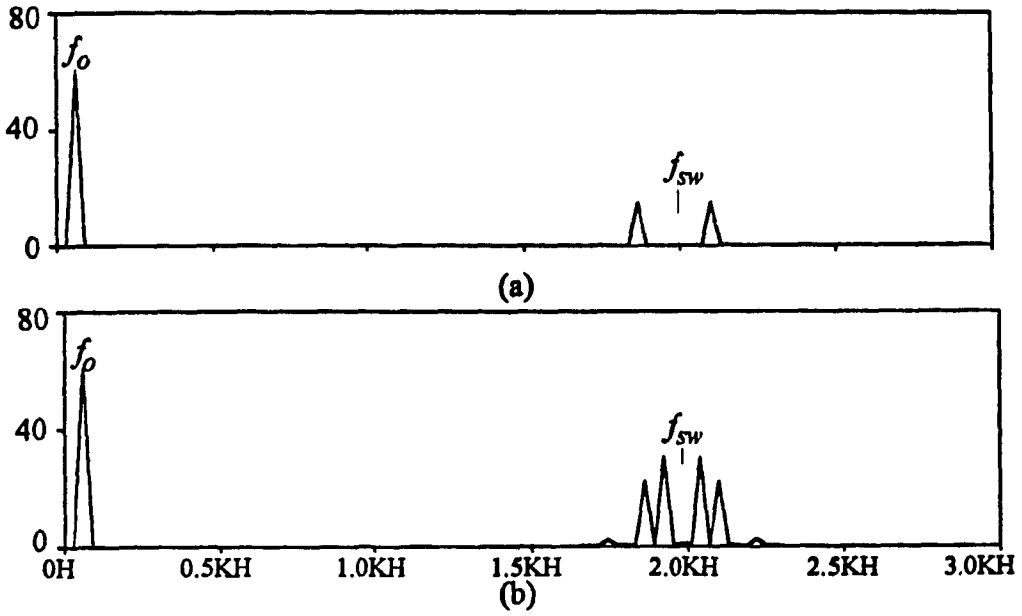


Fig. 4. 9. Output line voltage harmonic spectra under steady state with an ideal dc bus under (a) SPWM. (b) Integral control. (M=0.7 f_{sw}=33pu).

4.3.4.1.1. Quality of output voltage under ideal dc bus

The input dc bus is assumed to be ripple free. Fig. 4.9 shows the harmonic spectra of the line voltage for the two techniques in steady state.

The total harmonic distortion in line current (THD_i) defined in (4.10), is a performance index chosen to evaluate the performance of the proposed pattern generator. It is an indication of the filtering inherent in certain inverter loads e.g. an ac machine. It is the line current which is responsible for the torque developed by the machine and calls for minimum distortion in the current. A plot as a function of the switching frequency is shown in Fig. 4.10.

$$THD_i = \frac{\sqrt{(I_{rms})^2 - (I_{1rms})^2}}{I_{1rms}} \cdot 100\ \% \qquad (4.10)$$

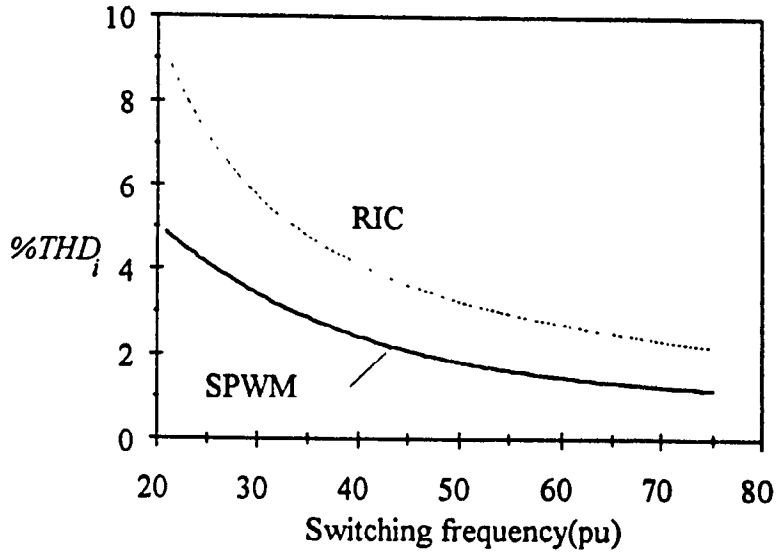


Fig. 4.10. THD_i with a typical inductive load (R_f=10Ω, L_f=16mH) as function of switching frequency with an ideal dc bus (M=0.7)

As noticed, the integral control technique produces a harmonic spectrum with a slightly higher distortion. This is because the correction is being applied only for a part of the time period. The gating pattern for the bottom switch is complementary of the top switch and not generated on-line.

4.3.4.1.2. Quality of output voltage under non-ideal dc bus

As discussed in section 1.2.1.2., with the inverter operating at a fundamental frequency f_o, the dominant harmonics of concern are at $f_r \pm f_o$. In this section simulation results are presented which exhibit the superiority of the reset integral control technique in attenuating these low order harmonics thus improving the quality of output voltage. The basis of comparison with a non-ideal dc bus is the harmonic rejection ability compared with the SPWM pattern generator in steady state.

Let the dc link voltage ripple be of dominant frequency f_r and magnitude $k_r V_{dc}$, where k_r is the dc bus ripple factor and V_{dc} the average dc bus voltage. The inverter input voltage can then be expressed as

$$V_d = V_{dc} + k_r V_{dc} \sin(2\pi f_r t) \tag{4.11}$$

Consider a ripple frequency of 2pu in the dc bus. With f_r=2pu, the dominant low order harmonic in the inverter line voltage is 3pu (Table I). This is shown in the harmonic spectra of Fig. 4.11 (b) obtained from the standard SPWM pattern generator. The same result with RIC is shown in Fig 4.11 (c)&(d) and it is evident that the harmonic is compensated for. The results are further substantiated by the line current waveform. As seen from Fig. 4.12 (a)&(b), there is a distinct distortion in line current obtained from SPWM. An improvement is observed with the RIC in Fig. 4.12 (c)&(d).

The harmonic attenuation capability is also illustrated by plotting the variation in current distortion (THD_i) as a function of switching frequency. It is shown in Fig. 4.13. The graph clearly shows an improvement with RIC at high switching frequencies.

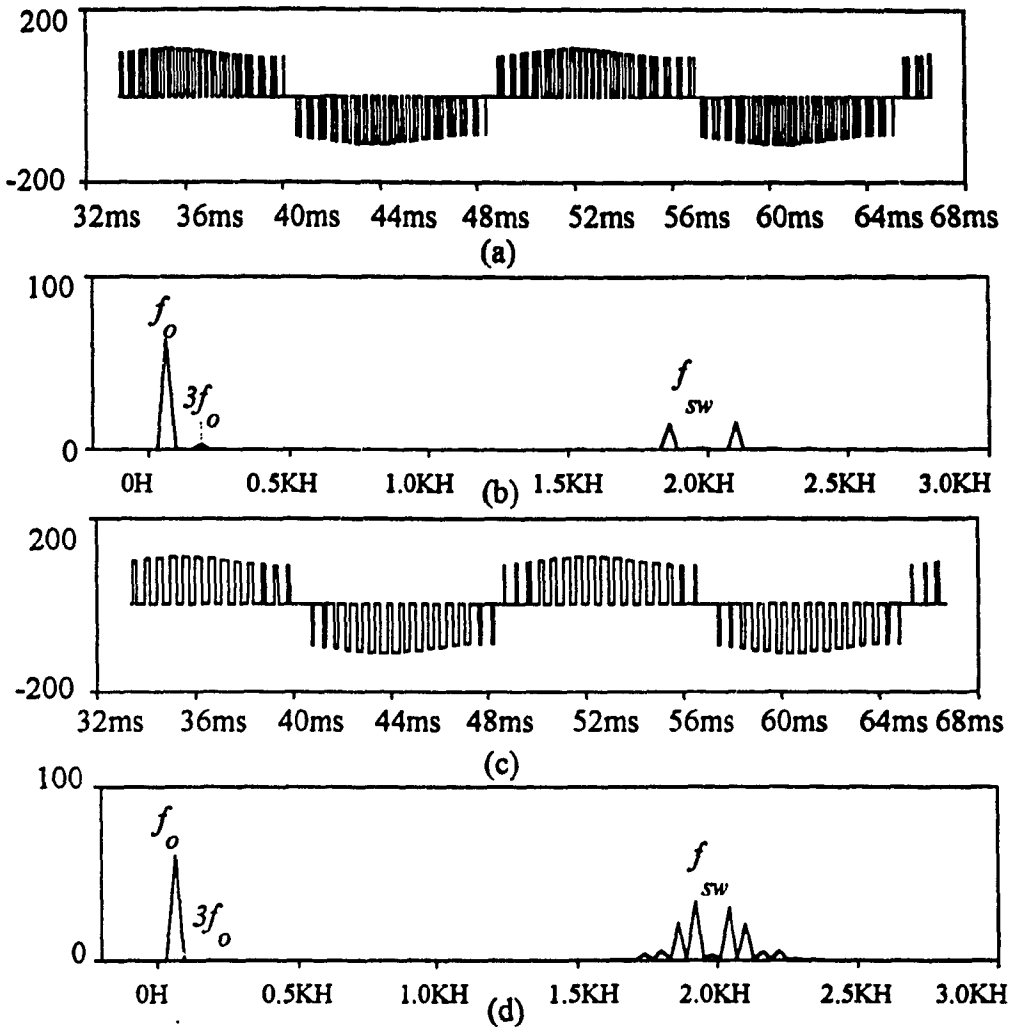


Fig. 4.11. Steady state operation of a three phase inverter with ripple in the dc bus (f_r=2pu). (a) Output voltage under SPWM. (b) Harmonic spectrum . (c) Output voltage under RIC. (b) Harmonic spectrum. (M=0.7, f_{sw}=33pu)

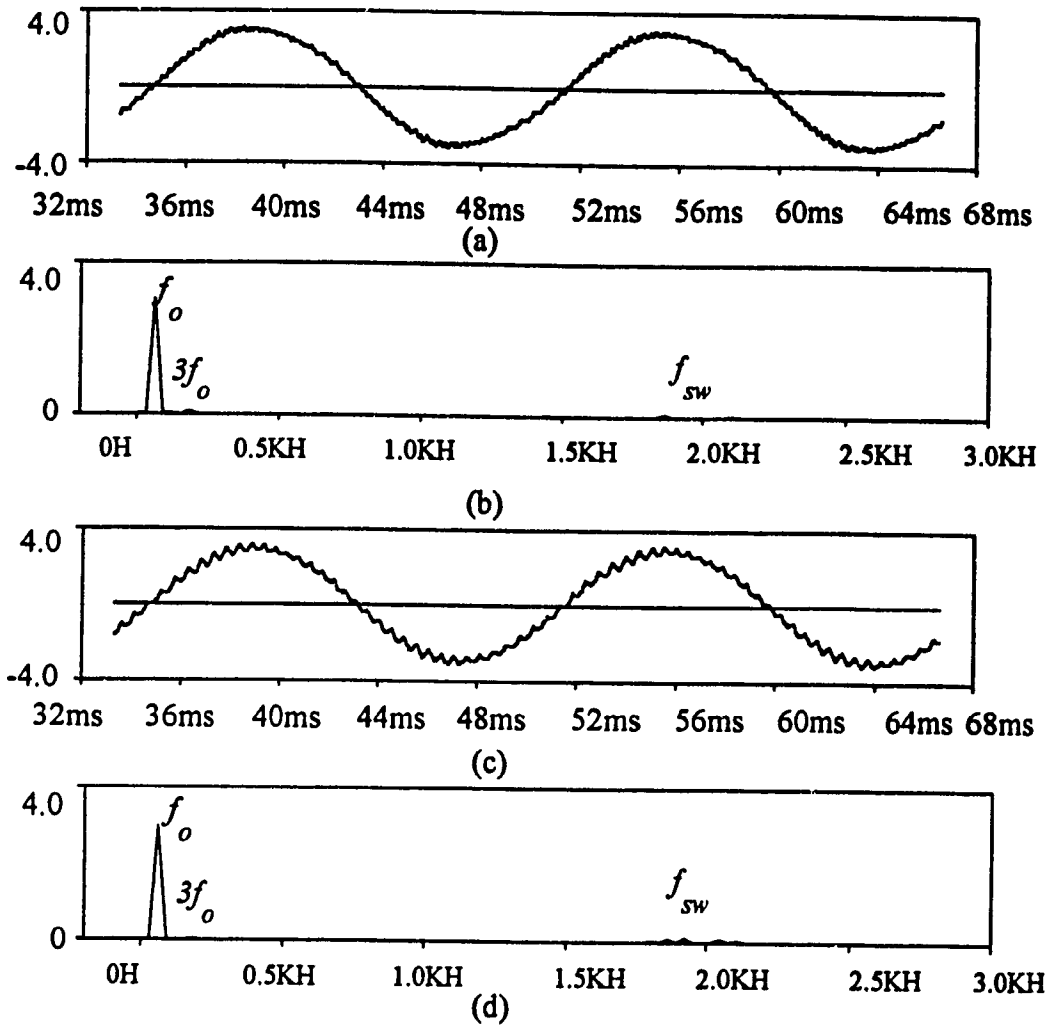


Fig. 4.12. Steady state operation of a three phase inverter with ripple in the dc bus (f_r=2pu). (a) Output current under SPWM. (b) Harmonic spectrum . (c) Output current under RIC. (b) Harmonic spectrum. (M=0.7, f_{SW}=33pu)

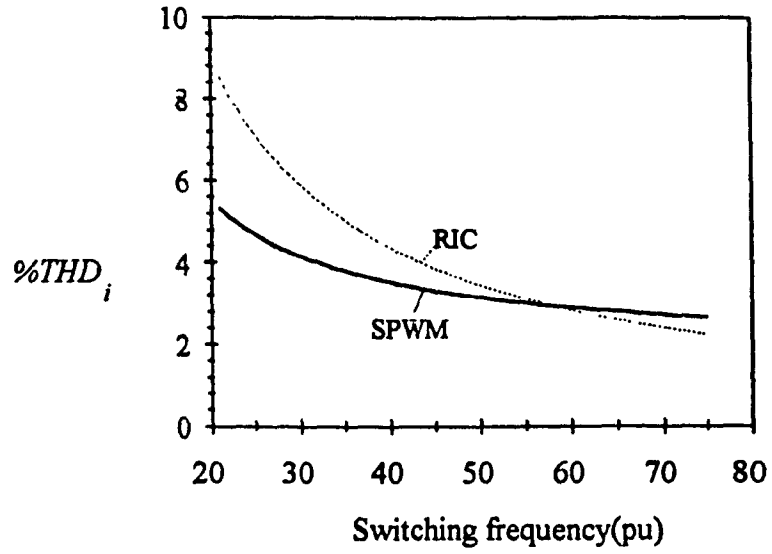


Fig. 4.13. Total current harmonic distortion (THD_i) versus switching frequency with 10% ripple (f_r=2pu). (a) Sine PWM. (b) Integral voltage control. (M=0.7)

A ripple of frequency 6pu is considered next. The dominant low order harmonics expected are the 5pu and 7pu. The results obtained from SPWM are compared with that obtained with RIC in Fig. 4.14. An improvement in harmonic attenuation is seen. Similarly Fig. 4.15 shows an improvement in current waveform with RIC.

The low order harmonic distortion (excluding the switching harmonics) is quantified by introducing a factor THD_{lv} and is defined as:

$$THD_{lv} = \frac{\sqrt{V_5^2 + V_7^2}}{k_r V_{dc}} \cdot 100\ \% \tag{4.12}$$

where V_5 and V_7 are the peak amplitudes of the low order harmonics respectively. The factor defined above is obtained at a modulation index of 0.7 and as a function of the switching frequency f_{sw}. The result is shown in Fig. 4.16. It is observed that while in SPWM, the attenuation of harmonics is independent of switching frequency, a better harmonic rejection is obtained with RIC. This is evident from Fig. 4.17 in which harmonic rejection results in low current distortion at higher frequencies.

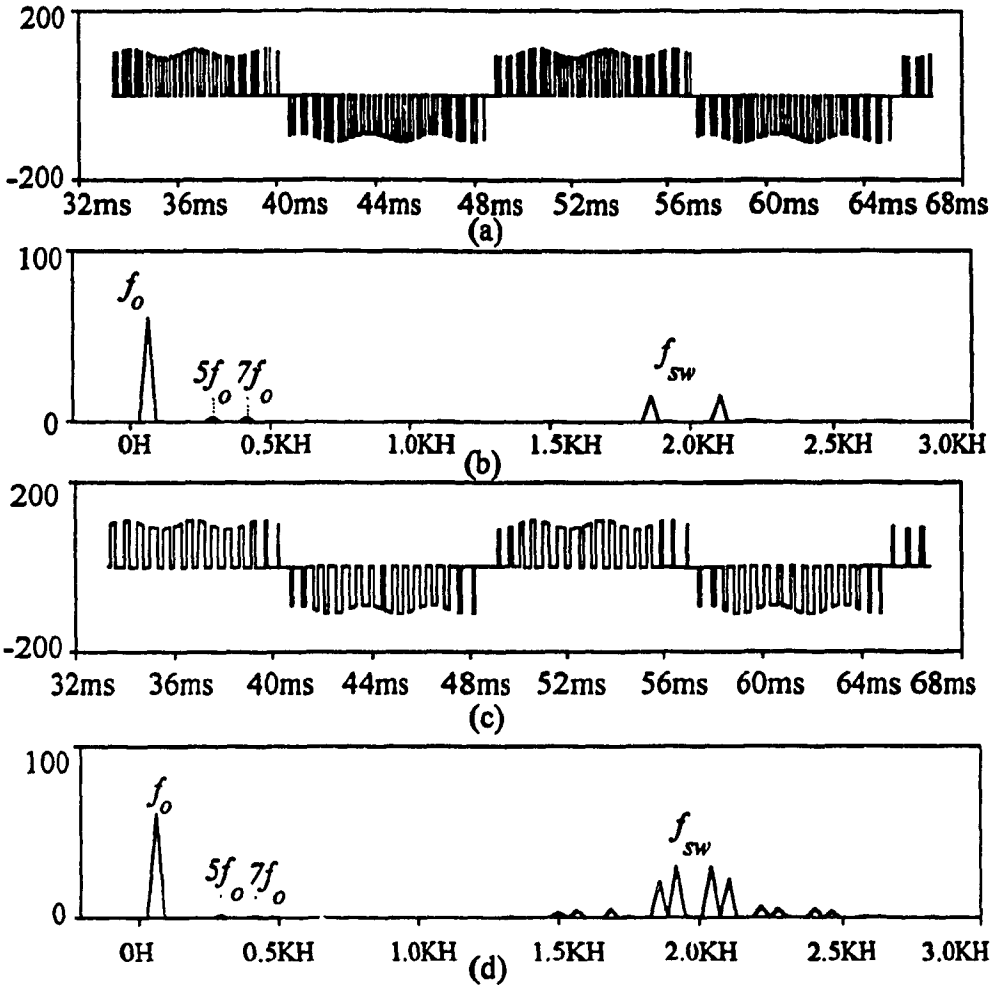


Fig. 4.14. Steady state operation of a three phase inverter with ripple in the dc bus (f_r=6 pu). (a) Output voltage under SPWM. (b) Harmonic spectrum. (c) Output voltage under RIC. (b) Harmonic spectrum. (M=0.7, f_{sw}=33pu)

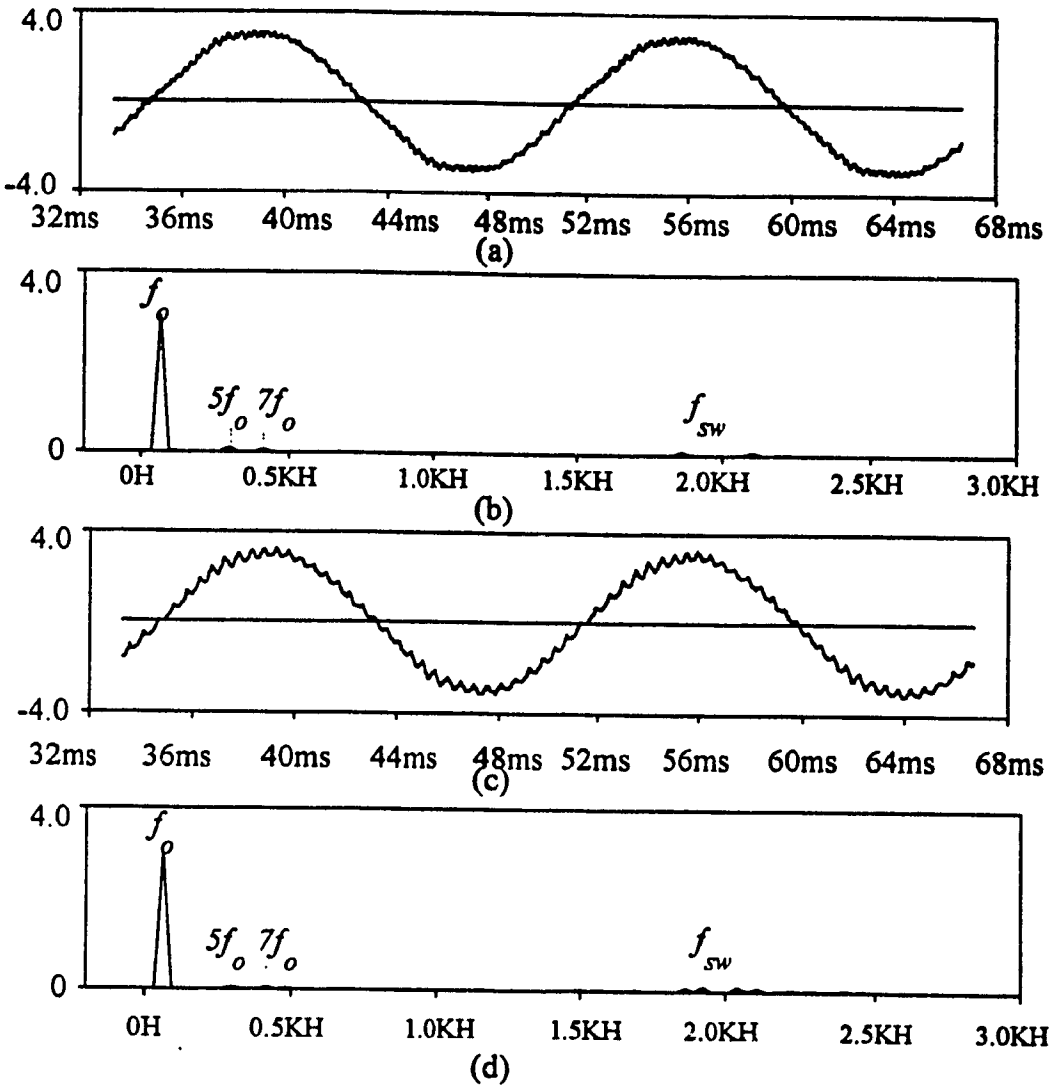


Fig. 4.15. Steady state operation of a three phase inverter with ripple in the dc bus (f_r=6 pu). (a) Output current under SPWM. (b) Harmonic spectrum . (c) Output current under RIC. (b) Harmonic spectrum. (M=0.7, f_{sw}=33pu)

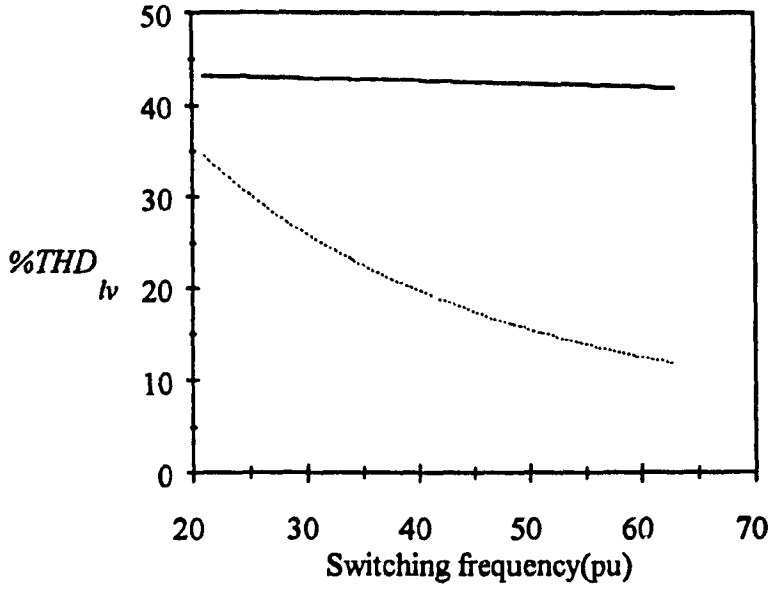


Fig. 4.16. Total low-order harmonic distortion versus switching frequency for (a) SPWM. (b) Integral voltage control. (M=0.2 and 0.7)

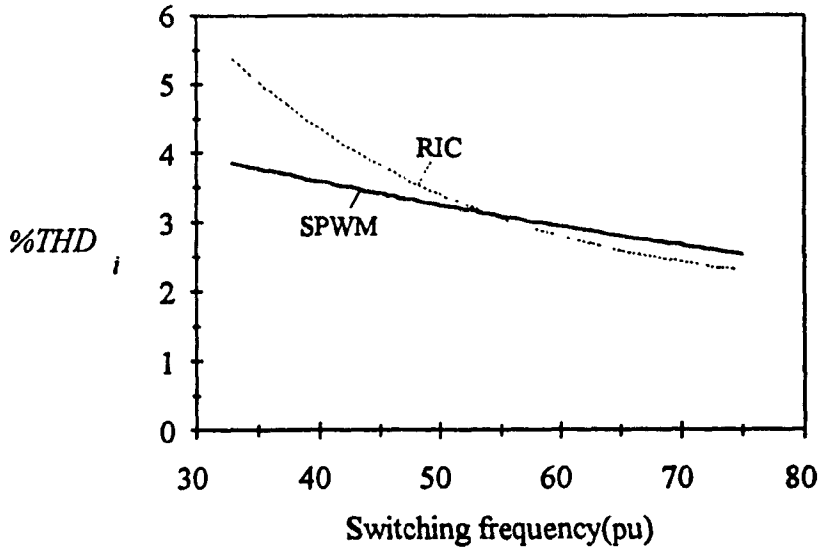


Fig. 4.17. Total current harmonic distortion ($\%THD_i$) versus switching frequency with 10% 360 Hz ripple. (a) Sine PWM. (b) Integral voltage control. (M=0.7)

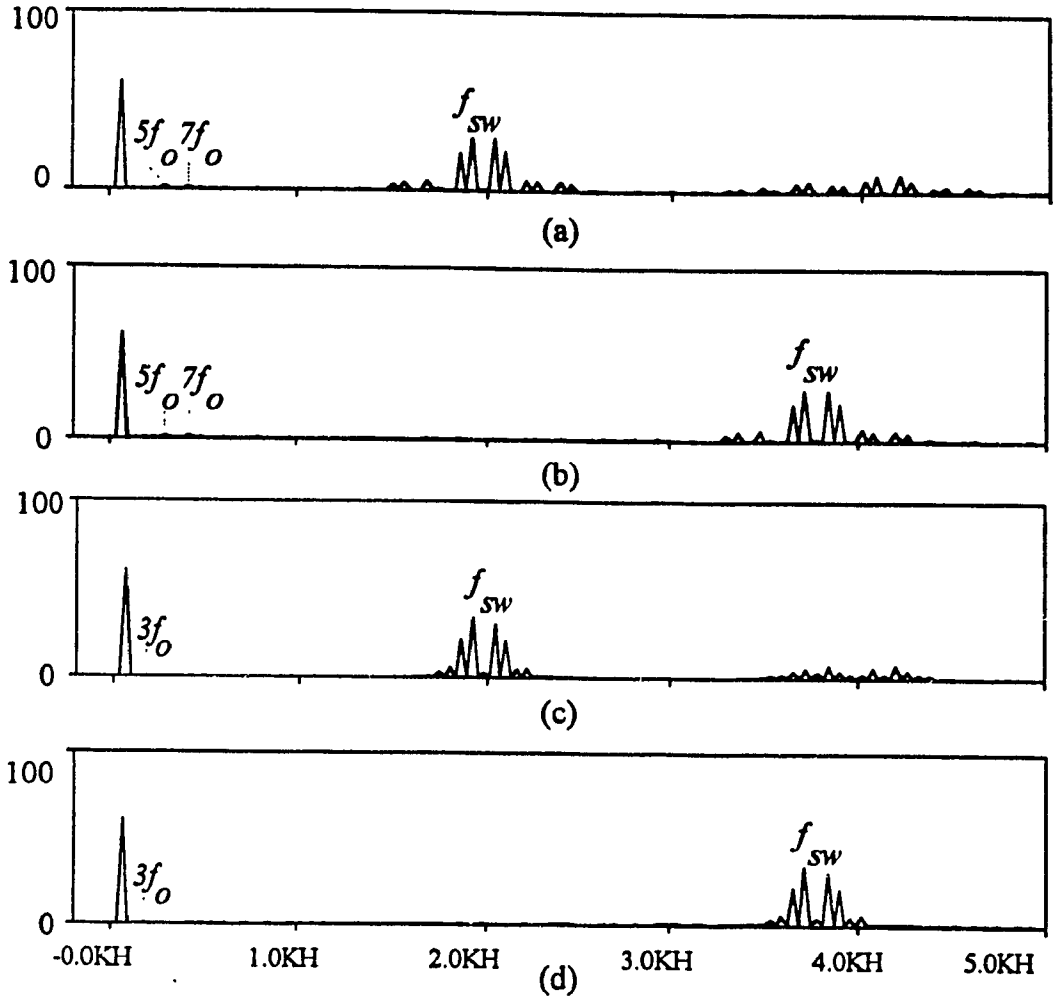


Fig. 4.18. Harmonic reduction with RIC as a function of switching frequency (a) f_r=6pu, f_{sw}=33pu (b) f_r=6pu, f_{sw}=63pu (c) f_r=2pu, f_{sw}=33pu (d) f_r=2pu, f_{sw}=63pu (k_r=0.1, M=0.7)

An improvement in harmonic attenuation of the lower order harmonics with increasing switching frequency for RIC is seen from the harmonic spectra of Fig. 4.18.

4.3.4.1.3. Output voltage gain under ideal dc bus

To obtain the transfer (input/output) characteristics in steady state, the rms fundamental output voltage($V_{LL1,rms}$) is obtained under different modulation indices given

by (4.5). Fig. 4.19 shows the plot of pu fundamental line voltage (rms) as a function of modulation index (M) with the proposed technique and standard SPWM. The graph shows that with the proposed technique the pu rms fundamental voltage varies linearly with the modulation index which is highly desirable feature. The ac gain obtained is identical to that obtained with SPWM technique.

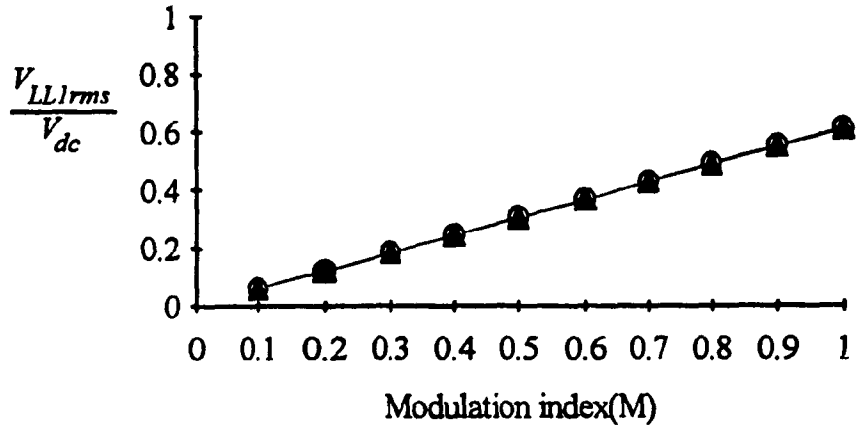


Fig. 4.19. Transfer characteristics for the proposed pattern generator and SPWM.

4.3.4.1.4. Reduction in gain with non-ideal dc bus

As seen from (4.8), the integrator time constant is designed for a ripple free dc bus. With the ripple on the dc bus, the integrator will not be able to integrate to the maximum control reference ($V_{bias}+V_m$) in one switching period (T_{sw}).(Fig. 4.20). This is because for a part of the input period, the dc bus voltage is less than the design value. If this occurs, the inverter operates with the maximum pulse width, irrespective of the control requirements and lower order harmonics are reintroduced. Thus the modulation index has to be decreased proportional to the input ripple, resulting in a loss in voltage gain. The voltage gain has been found from simulation studies to vary as:

$$K_{ac} = (1 - 2.k_r) \cdot K_{ac,ideal} \tag{4.13}$$

where $$K_{ac,ideal} = \frac{V_{ll,1}}{V_{dc}} = 0.866 \text{ (at } M = 1.0) \quad (4.14)$$

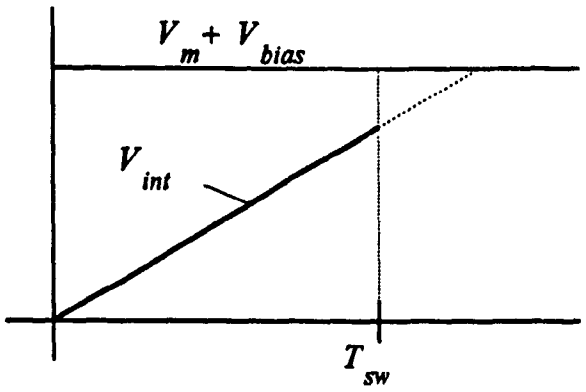


Fig. 4.20. Integrator output in a switching period with ripple in dc bus

In other words, with a ripple factor k_r, the maximum modulation index to which the inverter can be operated is given by the following equation

$$M_{max} = (1 - 2k_r) \quad (4.15)$$

This is illustrated in Fig. 4.21 and is the trade-off involved in applying the proposed controller for compensating the non-ideal DC bus. Such a limitation, inherent in compensation techniques is also reported in other schemes in the literature.

Thus with k_r=0.1, M_{max}=0.8.

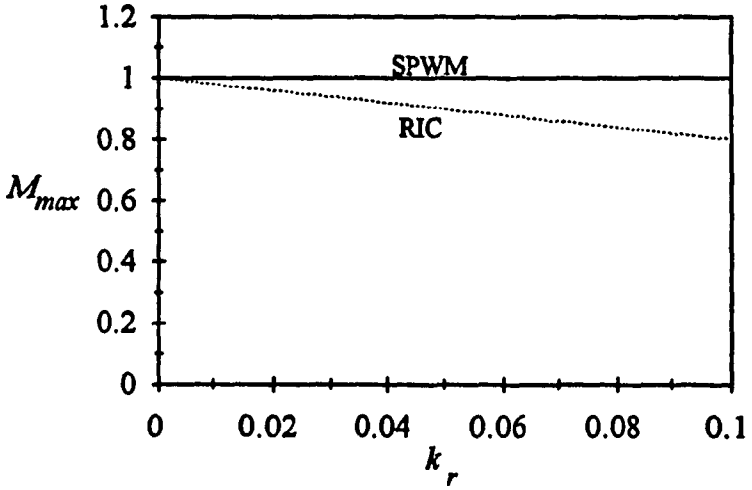


Fig. 4.21. Maximum modulation index (M_{max}) versus dc bus ripple factor.

4.3.4.2. Transient conditions

In this section the three phase inverter is studied under transient conditions. The criteria for evaluation is the ability of the controller to react to a change and maintain the desired output levels. The transient conditions considered are the change in (a) input dc bus and (b) reference control voltage.

4.3.4.2.1. Change in the input dc bus

The dc input voltage to the inverter is increased by 20% at time t=18ms. With the inverter operating at modulation index of 0.7, the desired output peak fundamental voltage is observed to be unaffected from the value prior to the disturbance. However with the SPWM technique, the output is found to increase by 20%. The simulation results are shown in Fig. 4.22.

4.3.4.2.2. Change in the reference

The reference is increased by 13% at time t=34ms, such that the inverter operates at a modulation index of 0.8. The controller reacts to the change in one switching cycle and allows a smooth transition in the operating point. This is achieved by adjusting the pulse width in output voltage. It is noticed in Fig. 4.23(c), that the pulse width in a half cycle of inverter output is larger than that prior to the change because it now takes longer for the integrator to touch the envelope of the reference voltage.

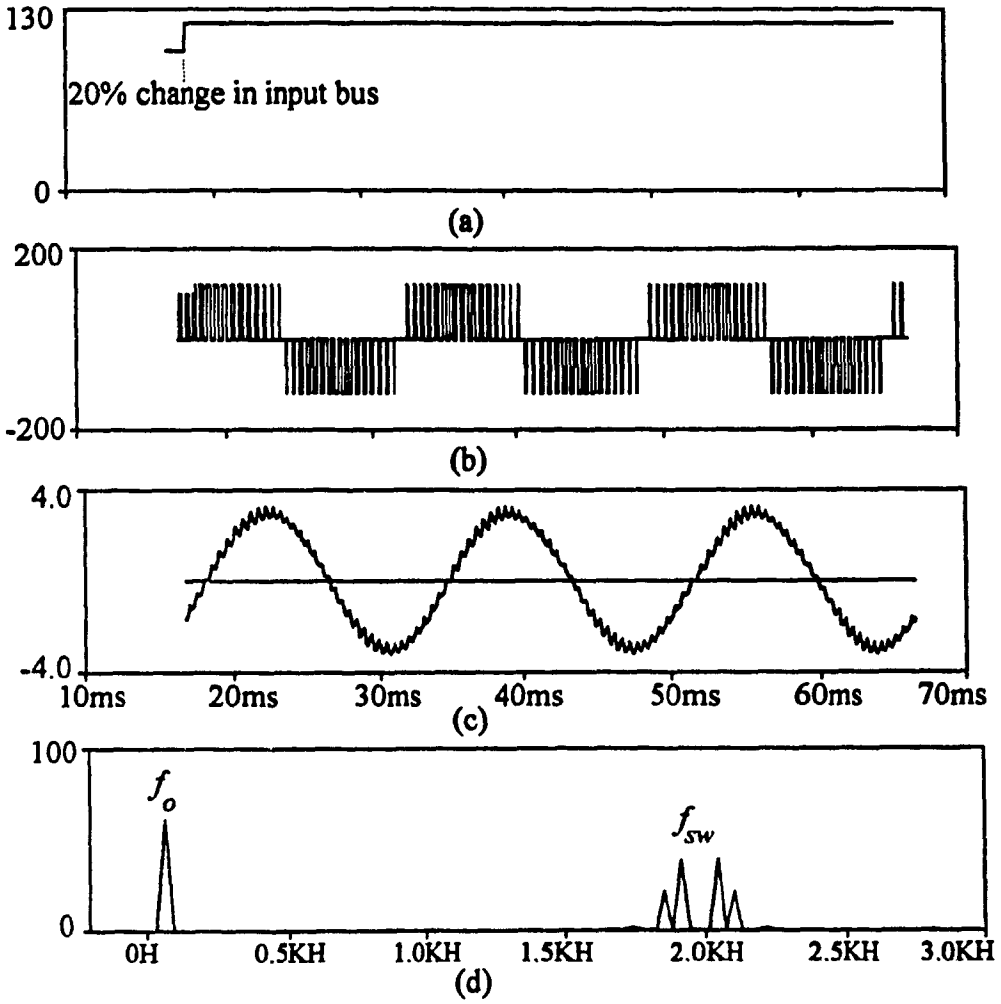


Fig. 4.22. Response of the converter to a change in the input dc bus. (a) Input dc bus. (b) Line voltage. (c) Line current. (d) Harmonic spectra of the line voltage.

(M=0.7, f_{sw}=33pu)

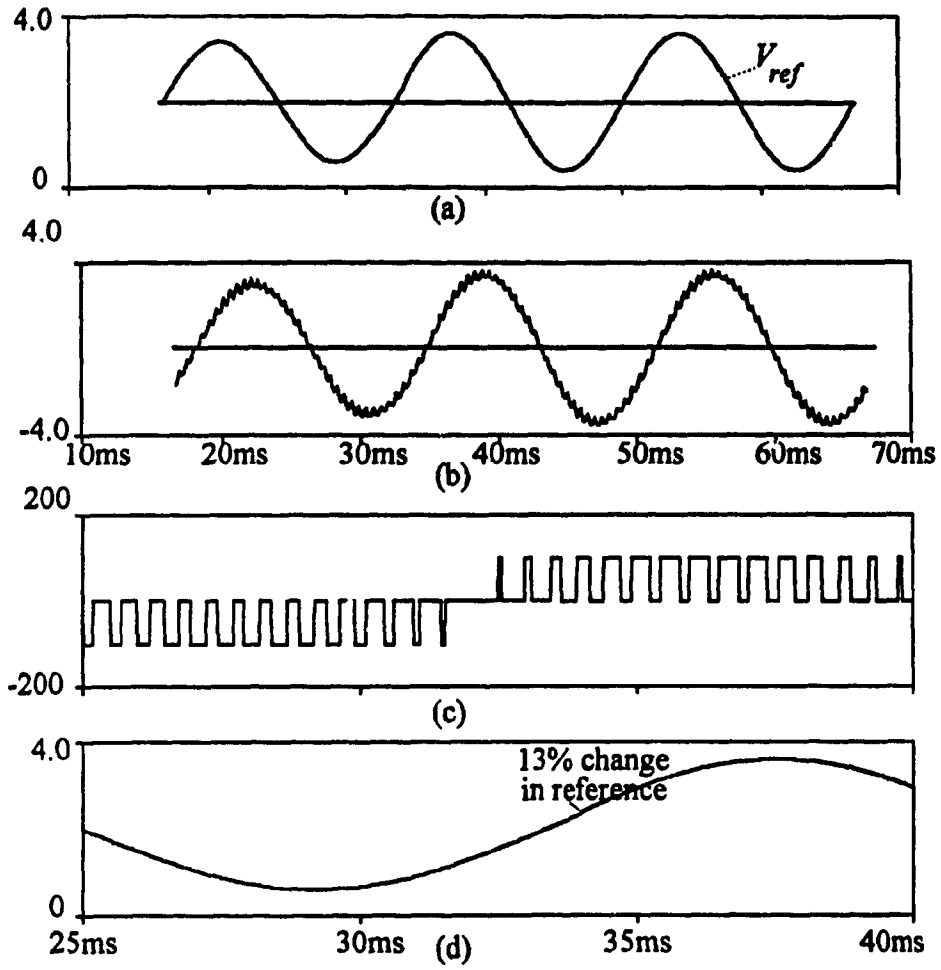


Fig. 4.23. Response of voltage source inverter to a change in control reference. (a) Control reference(V_{ref}). (b) Line current. (c). Detailed view of line voltage. (d). Detailed view of control reference (13% change at 34ms)

4.3.5. Experimental results

In order to verify the design procedure and the key simulation results, a 5 kVA experimental three-phase inverter was set up in the laboratory. The front end diode bridge was fed from a three-phase supply with unbalance capabilities.

Fig. 4.24(a) shows the sinusoidal control reference and the output of the real time resettable integrator. The integrator output is reset when it touches the envelope of the reference. Fig. 4.24(b) shows the gating signal for the switch Q_1 of the bridge inverter (Fig. 4.6).

Fig. 4.25(a) shows the dc link voltage with a dominant harmonic at 6 pu. This is inherent in diode bridge rectification. Fig. 4.25(b) and (c) show the experimental inverter output voltage(line to line) and line current. The corresponding frequency spectra are shown in Fig. 4.26. In particular Fig. 4.26(a) shows the dominant harmonic at 6 pu while Fig. 4.26(b) shows suppressed low order harmonics at 5 pu and 7 pu.

To study the performance of inverter under input unbalance conditions, one of the supply lines feeding the diode bridge was opened. Fig. 4.27(a) shows the resulting dc link voltage while Fig. 4.28(a) shows the corresponding frequency spectrum with the dominant harmonic at 2 pu. Fig. 4.27(b) shows the inverter line-line voltage and the corresponding frequency spectrum is as in Fig. 4.28(b) and clearly illustrates the effectiveness of the proposed pattern generator. The low order harmonic are almost suppressed improving the quality of the output voltage. The line current and its spectrum are shown in Fig. 4.27(c) and Fig. 4.28(c).

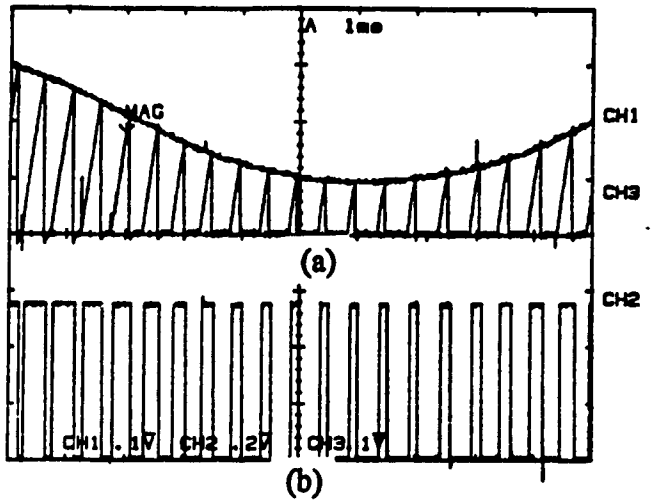


Fig.4.24. Control waveforms (a) Integrator output and control reference. (b) Gating signal for switch 1. (f_{SW}=33pu M=0.7)

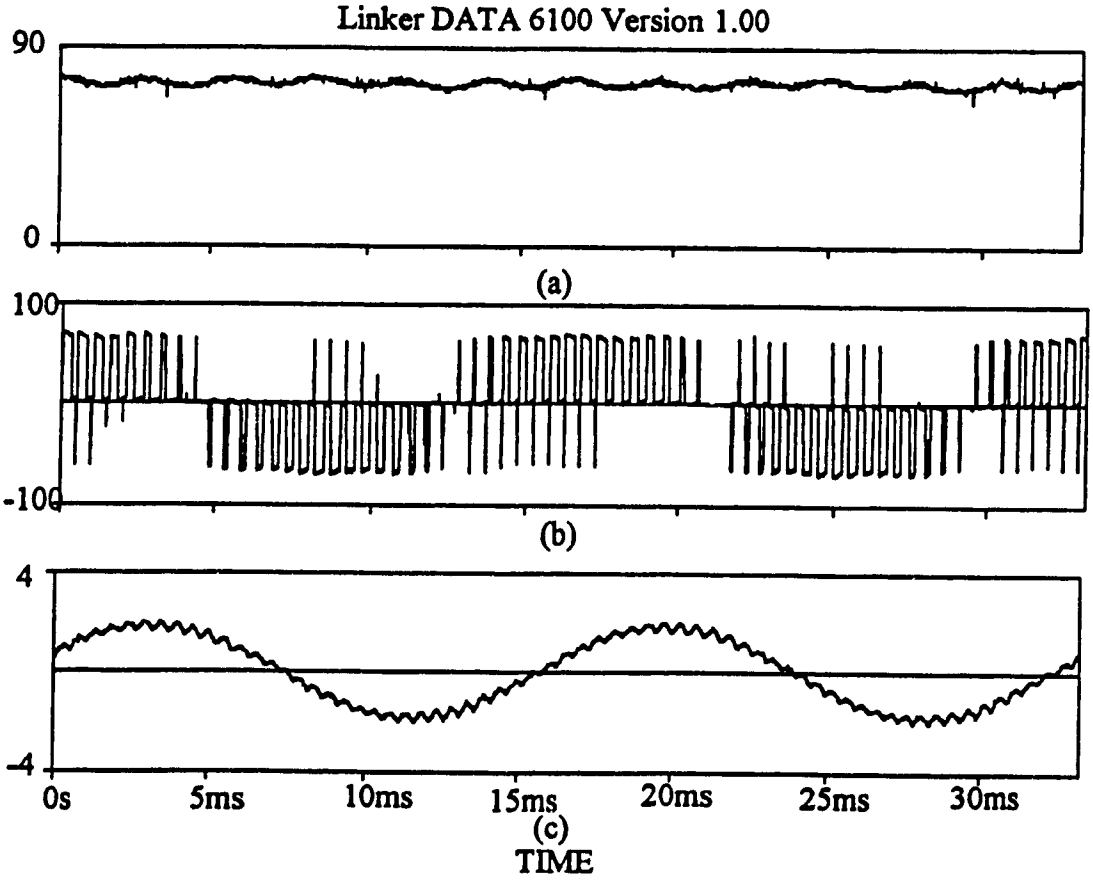


Fig.4.25. (a) Experimental DC link voltage. (b) Inverter output line-line voltage. (c) Line current (f_{SW}=33pu M=0.7)

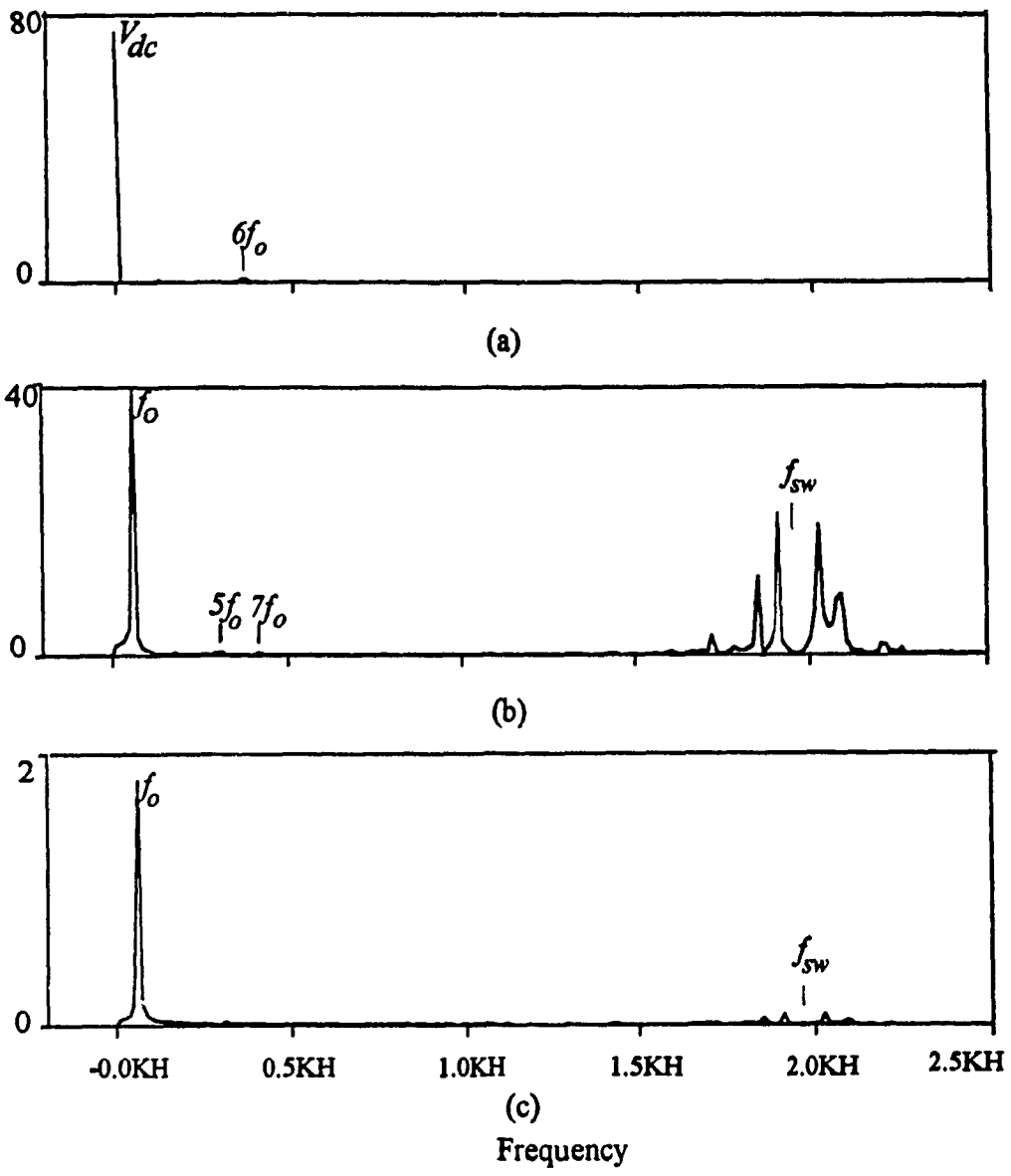


Fig. 4.26. Experimental frequency spectra. (a) DC link voltage. (b) Inverter output line-line voltage. (c) Line current. (f_{sw}=33pu M=0.7)

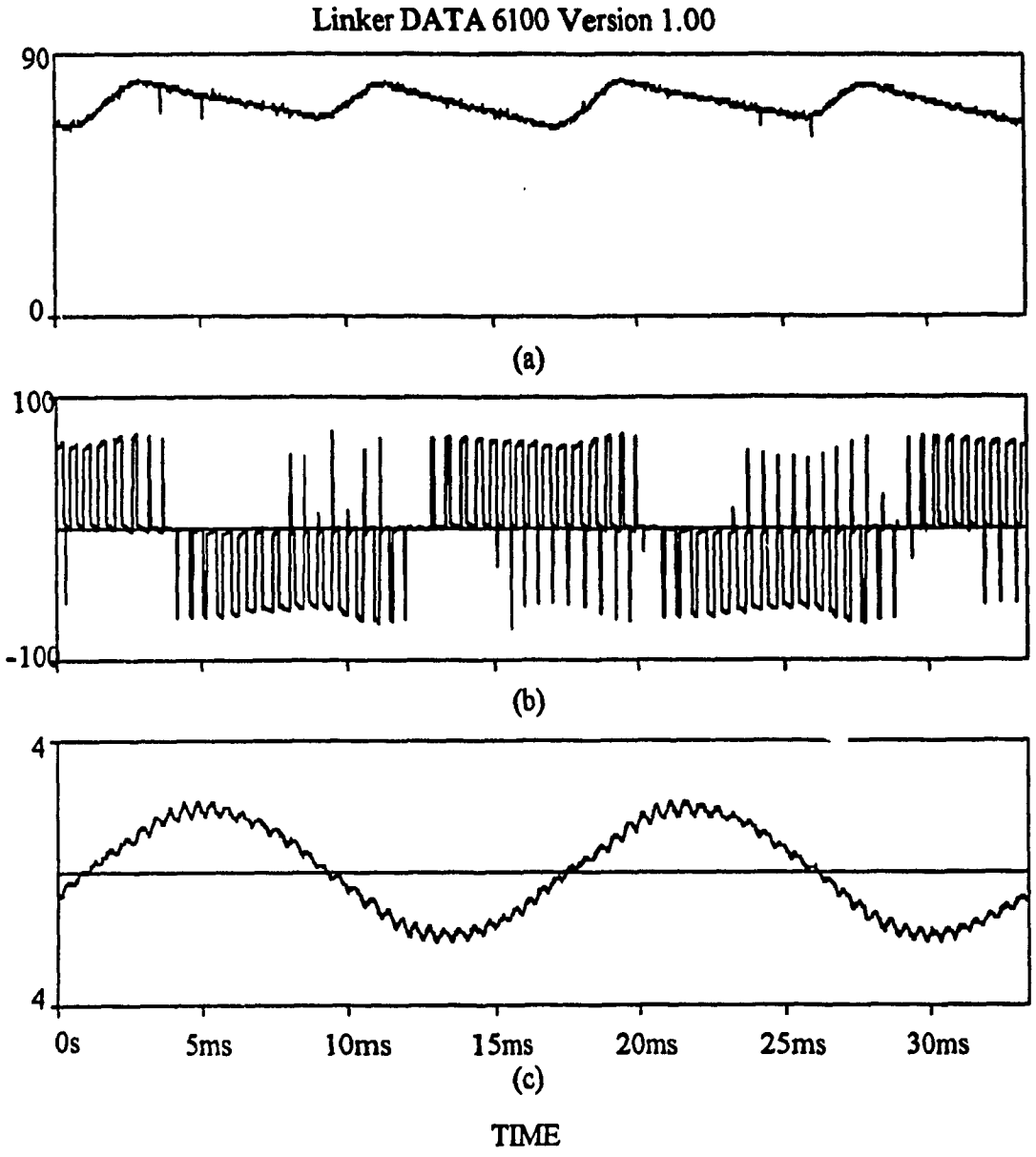


Fig. 4.27. (a) Experimental DC link voltage with unbalance in the input. (b) Inverter output line-line voltage. (c) Line current (f_{SW}=33pu M=0.7)

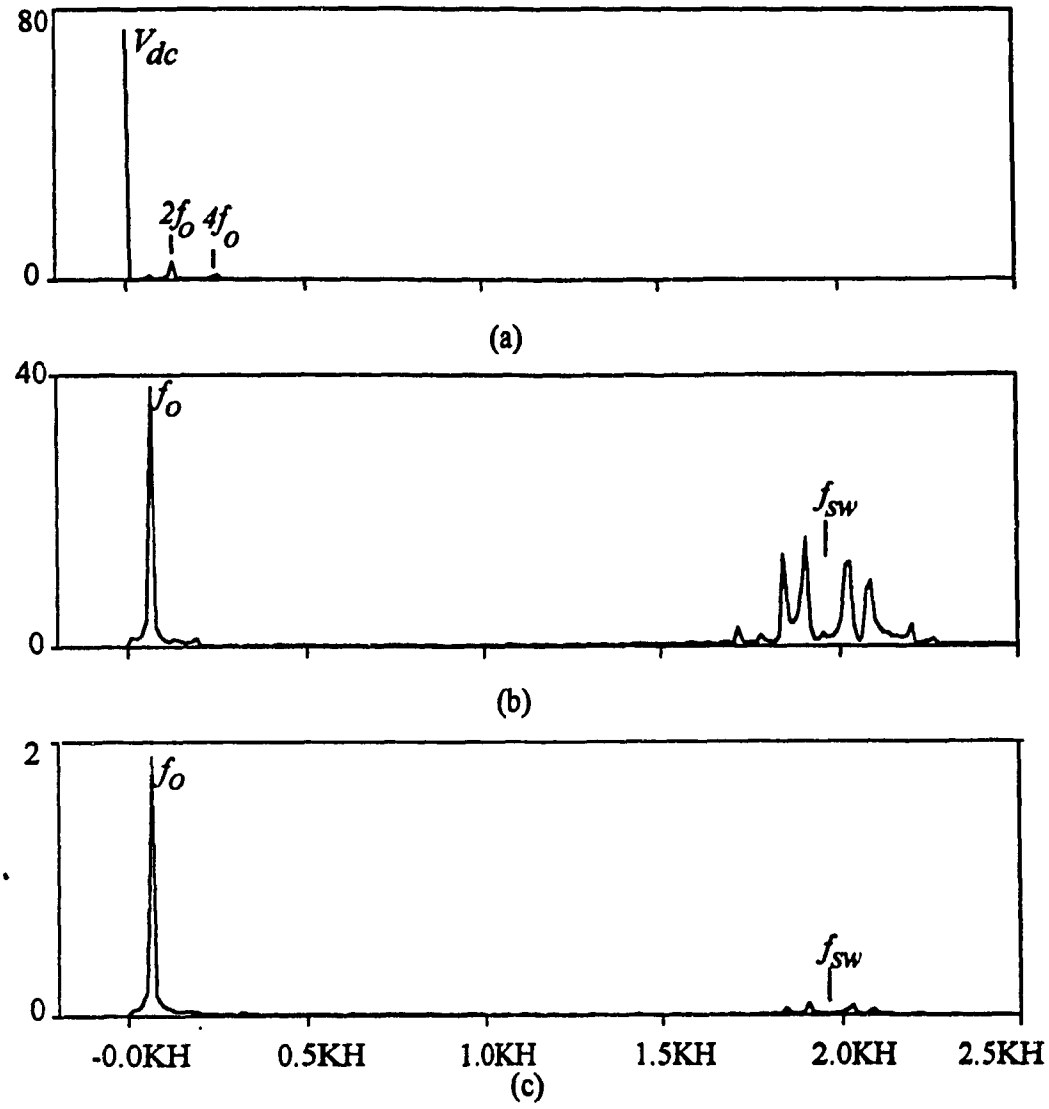


Fig. 4.28. Experimental frequency spectra. (a) DC link voltage. (b) Inverter output line-line voltage. (c) Line current. (f_{SW}=33pu M=0.7)

4.4. Modulated Integral Control (MIC)

This section discusses the improvement in the performance of dc-ac converters working under non-ideal conditions by applying the principle of modulated integral control introduced in chapter 2. This technique can provide compensation for dead times in the gating signals while rejecting the input harmonics.

4.4.1. Structure of the proposed controller

The modulated integral control technique is based on sensing the instantaneous output voltage of the inverter and generating the pattern from the error by using a carrier technique. The location of the sensor and the choice of the reference control voltage is the same as discussed in section 4.2.

4.4.1.1. Half bridge inverter

The pattern generator for a half bridge voltage source inverter is shown in Fig. 4.29. The structure of the proposed pattern generator is introduced with the help of a half bridge inverter and later extended for a three phase inverter. The basis for doing this is to realize independent control of the inverter legs.

4.4.1.2. Principles of operation

As seen from the Fig. 4.29, the instantaneous voltage across the bottom switch is sensed and brought to the controller. This voltage is proportional to the output line-line voltage as discussed in section 4.2. The error between this voltage and the control reference (e_{AN}) is integrated to generate the modulation waveform (V_m) and compared with a fixed frequency triangular carrier (V_{carr}) to generate the gating signals.

While the top switch (Q_1) is on, the integrator output has a positive slope. The intersection with the carrier determines the switching off instant. Thereafter the bottom switch is turned on (g_4). This forces the controller input to go to zero and the slope of the

integration becomes negative. At the next intersection with the carrier, the bottom switch is turned off and the top switch turned on (g_1) to repeat the switching cycle. The top and the bottom switch are thus switched in a complementary fashion. The complete control waveforms are shown in Fig. 4.30.

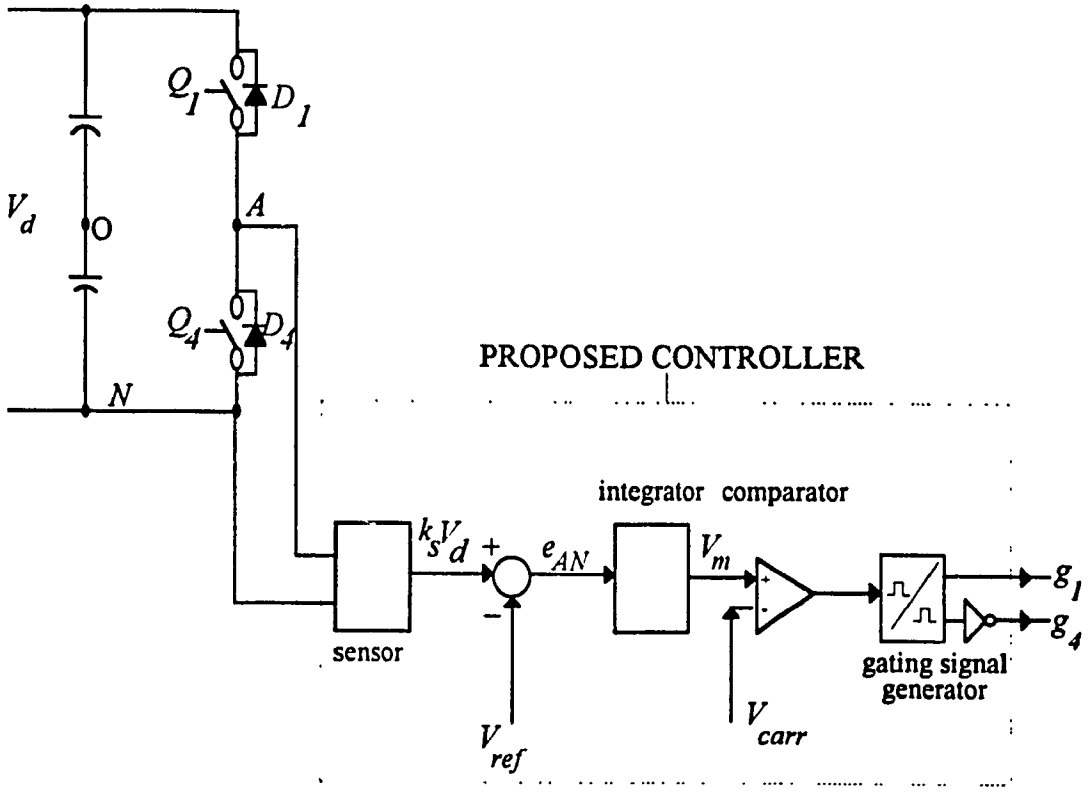


Fig. 4.29. The proposed controller for a half bridge voltage source inverter.

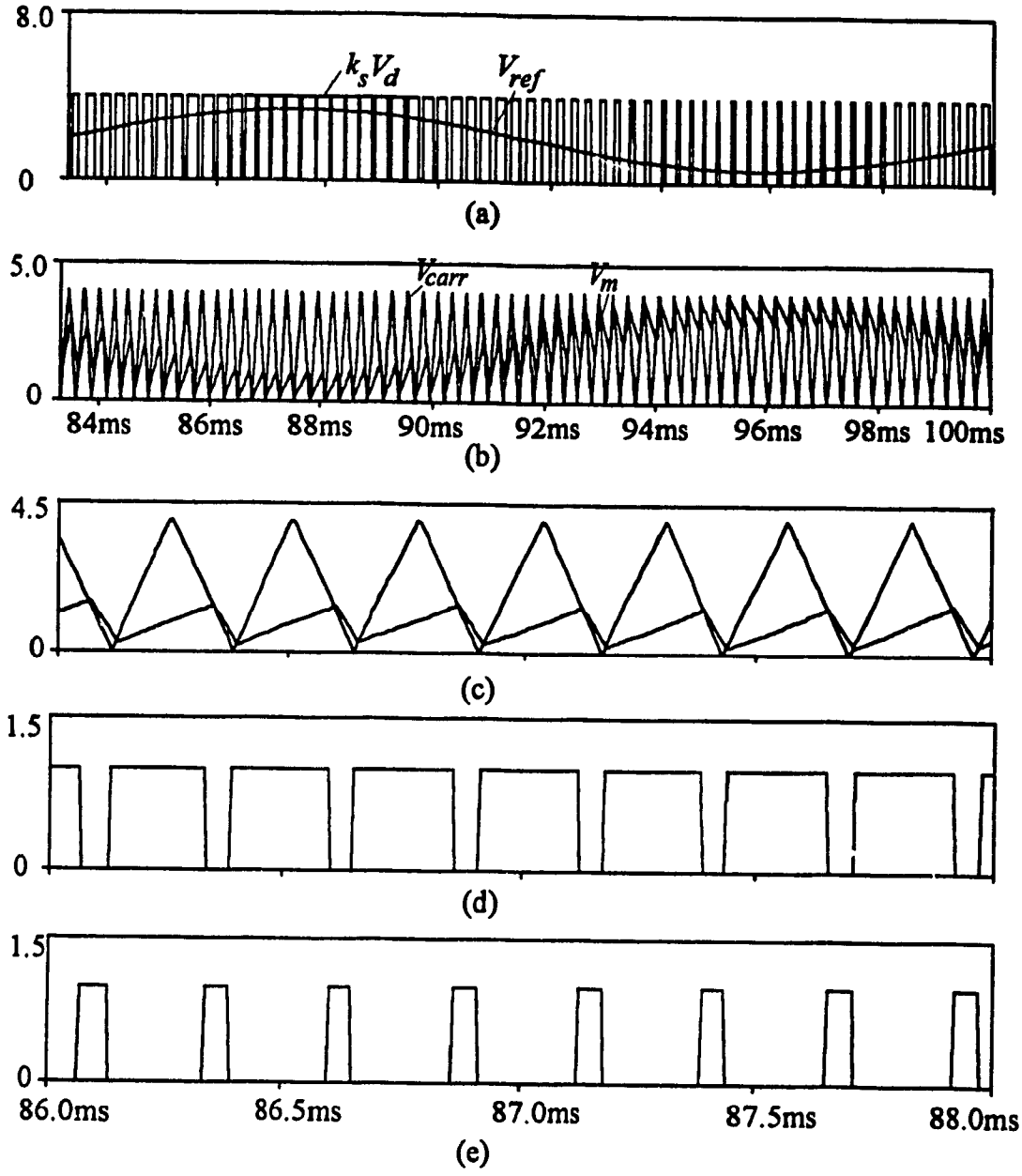


Fig 4.30. Waveforms of a half bridge inverter. (a) Controller input ($k_s V_d$) and reference voltage V_{ref}. (b) Modulation (V_m) and carrier(V_{carr}) waveforms. (c) Detailed view of the modulation and carrier waveform. (d) Gating signal for the top switch. (e) Gating signal for the bottom switch.

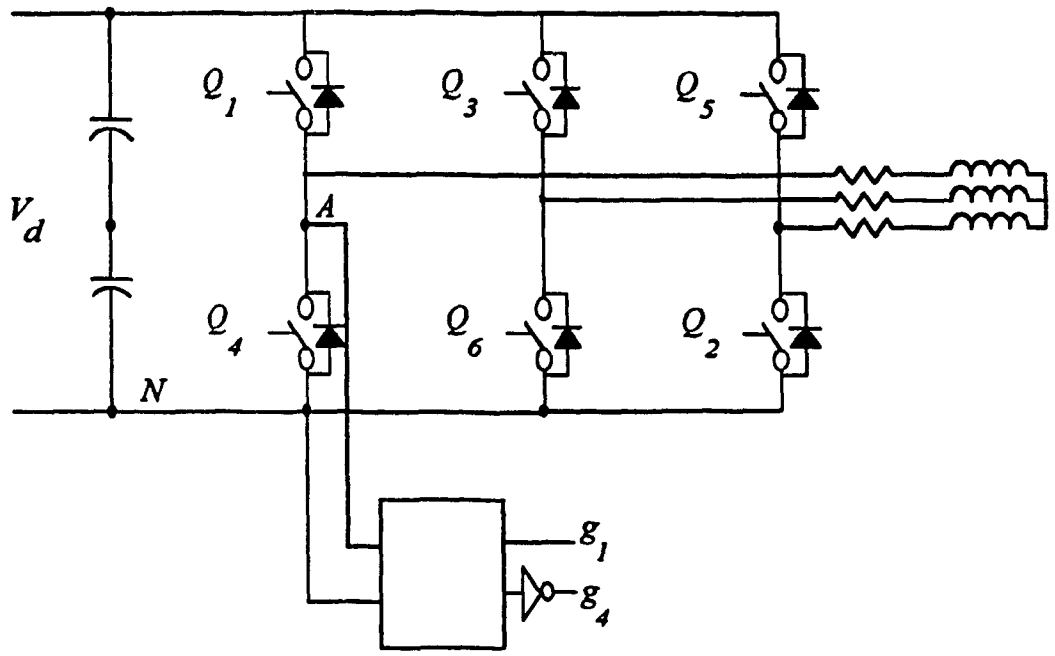


Fig. 4.31. Proposed pattern generator for a three-phase inverter.

4.4.1.3. Three phase inverter

The proposed pattern generator can be implemented for a three phase inverter by using three controllers of Fig. 4.29 across the bottom switch in each inverter leg. This requires three control references phase shifted 120°. The three phase implementation is shown in Fig. 4.31 and key waveforms are given in Fig. 4.32 and Fig. 4.33.

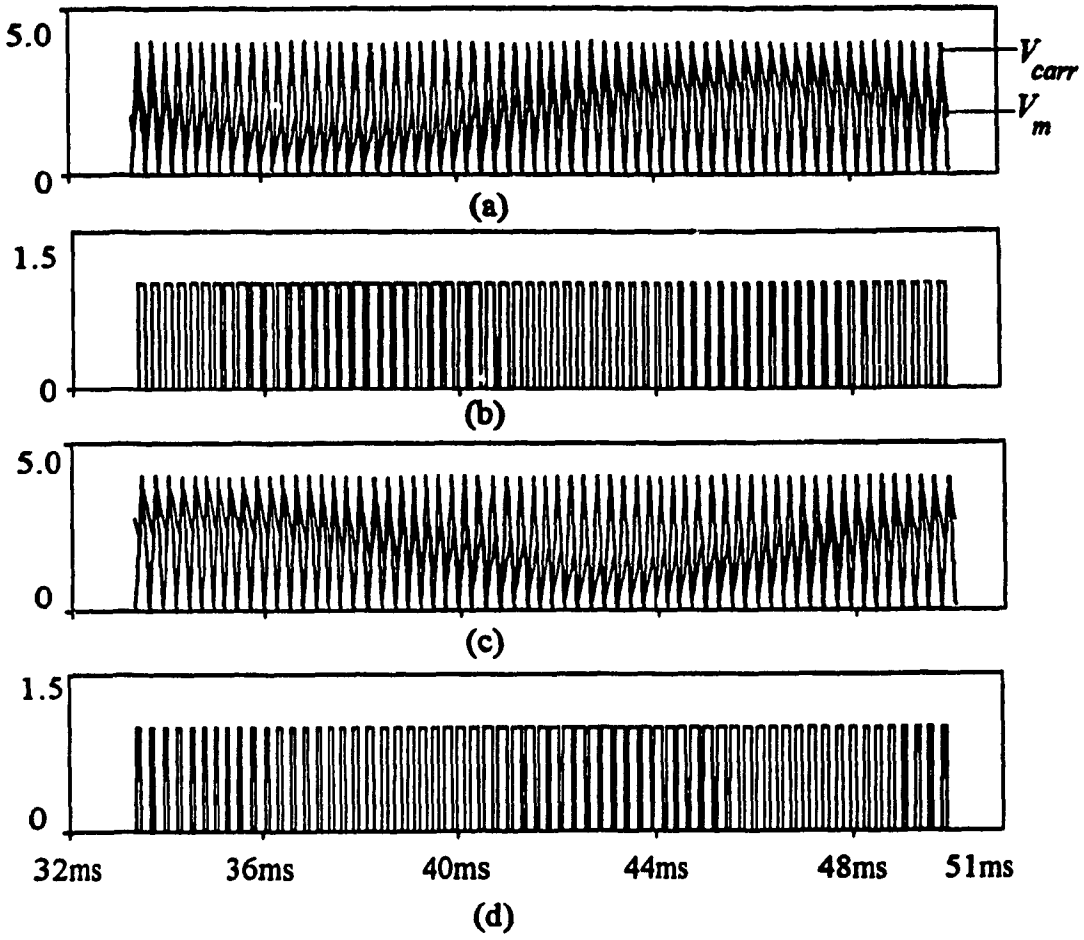


Fig. 4.32 Control waveforms. (a) Modulation and carrier waveform phase A. (b) Gating signal for switch Q_1. (c) Modulation and carrier waveform phase B. (d) Gating signal for switch Q_3.

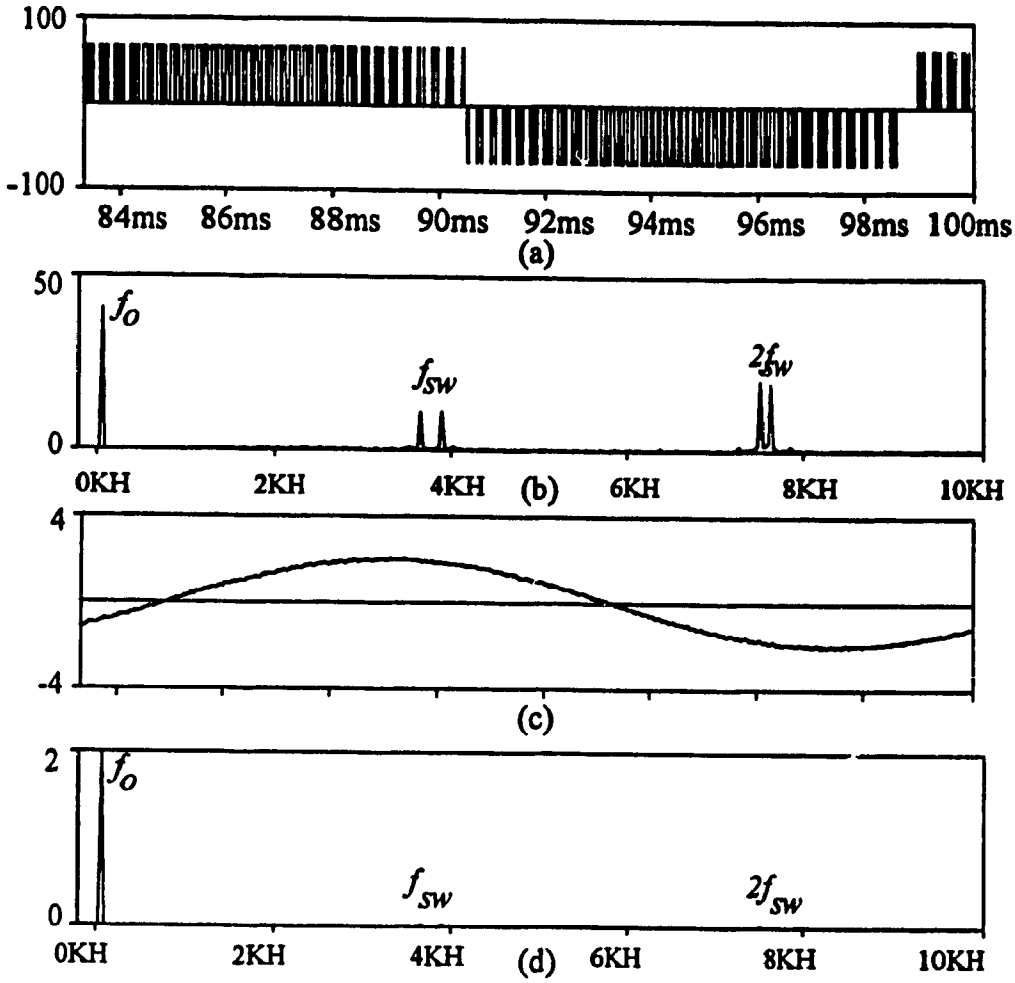


Fig. 4.33. Waveforms for the three phase pattern generator. (a) Line voltage (b) Spectrum of line voltage (c) Line current (d). Spectrum of line current. (M=0.7 f_{sw}= 3780 Hz)

4.4.2. Principles of compensation

Unlike the Reset Integral Control (RIC) technique in which the controller is deactivated for part of the switching period, here the integrator is not reset and tracks the sinusoidal reference (while the bottom switch is ON). The advantage with this is that the information from previous cycles is retained. This information is a function of the non-ideal conditions present in that switching half cycle and is used in the next half cycle to compensate for them. Thus errors introduced by switching delays and dead times can be

corrected. Also the slope of integration (while the top switch is ON) is proportional to the instantaneous value of the input voltage providing the basis of compensation for the source harmonics. These are discussed in detail in subsequent sections.

4.4.3. Design guidelines

The key parameter in the control loop is the integrator time constant τ which is dependent on the modulation index (M) and the dc link voltage. Thus the design is carried out for an ideal and a non-ideal dc bus.

4.4.3.1. Ideal DC Bus

Consider a ripple free dc bus with magnitude V_{dc}. The input to the controller is then given by:

$$V_{in} = k_s V_{dc} \tag{4.16}$$

Due to the offset present in the switch voltage, the control reference for a particular modulation index, M given by (4.5) can be rewritten as:

$$V_{ref} = V_{bias} + M\, V_{bias} \sin(2\pi f_o t) \tag{4.17}$$

As seen from Fig. 4.32(c), the necessary condition to be satisfied to ensure constant frequency operation is that the slope of the modulation wave be smaller than the carrier wave at all times.

The rising slope (when the top switch is ON) is given by:

$$m_r = \frac{(k_s V_{dc} - V_{ref})}{\tau} \tag{4.18}$$

while the falling slope (when the bottom switch is ON) is given by:

$$m_f = \frac{V_{ref}}{\tau} \tag{4.19}$$

From the above equations it is clear that the maximum rising slope occurs when the reference signal is minimal, while the maximum falling slope happens at the maximum reference voltage.

To satisfy the slope conditions, the following inequalities have to be satisfied, i.e.

$$\frac{2V_c}{T_{sw}} > \frac{k_s V_{dc} - V_{ref,min}}{\tau} \tag{4.20}$$

and

$$\frac{2V_c}{T_{sw}} > \frac{V_{ref,\max}}{\tau} \tag{4.21}$$

where Vc is the carrier amplitude and T_{sw} the switching time period.

At a given modulation index M and using (4.17), (4.20) can be rewritten as:

$$\frac{2V_c}{T_{sw}} > \frac{k_s V_{dc} - Vbias(1-M)}{\tau} \tag{4.22}$$

Let $$k_s V_{dc} = 2V_{bias} \text{ and } V_c = k_s V_{dc} \tag{4.23}$$

Equation (4.22)can be rewritten as:

$$\tau > \frac{V_{bias}(1+M)}{2V_c f_{sw}} \tag{4.24}$$

(4.21) also translates into the condition in (4.24).

This is graphically illustrated in Fig. 4.34 in which the integrator time constant as function of modulation index for various switching frequencies is plotted. To choose the integrator time constant, consider the worst case corresponding to M=1.0. (4.24) then reduces to

$$\tau_{min} = \frac{V_{bias}}{V_c f_{sw}} \tag{4.25}$$

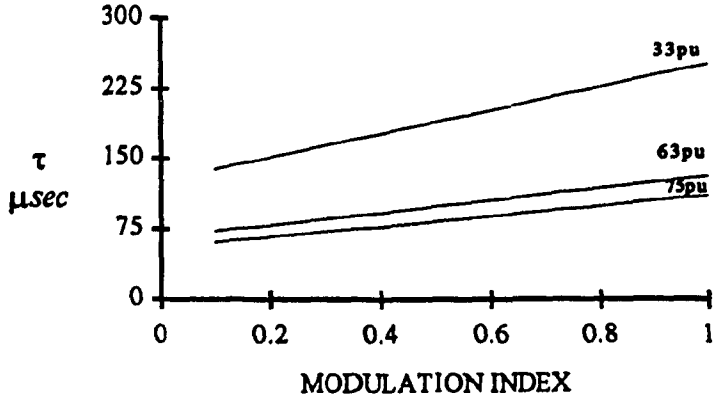


Fig. 4.34. Integrator time constant versus modulation index

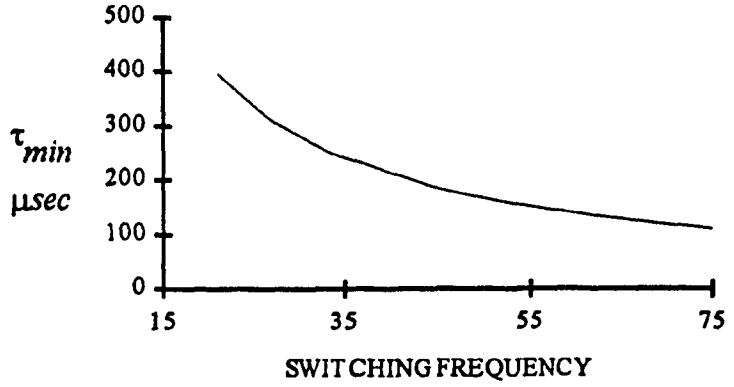


Fig. 4.35. Minimum recommended integrator time constant (for an ideal dc bus) versus switching frequency.

Using (4.23) the above equation can be rewritten as

$$\tau_{min} = 0.5\, T_{sw} \tag{4.26}$$

This is the key design equation and is plotted in Fig. 4.35.

4.4.3.2. Non-Ideal DC Bus

A non-ideal dc bus consists of a single dominant ripple frequency f_r and is given by (4.11). The ripple affects the rising slope of the integrator output.

The input to the controller is given by:

$$V_d = k_s (V_{dc} + k_r V_{dc} \sin(\omega_r t)) \tag{4.27}$$

Writing the condition for maximum rising slope (corresponding to maximum dc voltage and minimum reference voltage) and rearranging:

$$\tau > \frac{V_{bias}(1+M+2k_r)}{2V_c f_{sw}} \tag{4.28}$$

Choosing the worst case condition of M=1.0, and using (4.23), (4.28) can be rewritten as

$$\tau_{min} = \frac{(1+k_r)\, T_{sw}}{2} \tag{4.29}$$

(4.29) is graphically plotted in Fig. 4.36 for k_r=0.05 and 0.1.

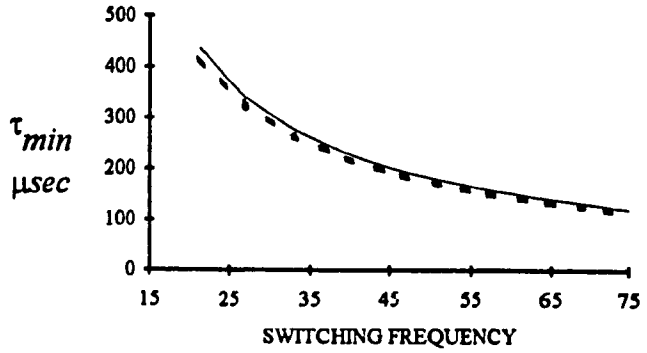


Fig. 4.36. Minimum recommended integrator time constant (for an non-ideal dc bus) versus switching frequency.

4.4.3.3. Design example

In order to apply the design equations developed in the previous section, a three phase inverter is designed according to the following specifications:

- input dc bus voltage, V_{dc}= 66.67V
- dc bus ripple frequency, f_r= 6 and 2pu
- dc bus ripple factor, k_r=0.1
- inverter fundamental output frequency, f_i=60 Hz or 1pu
- inverter switching frequency, f_{sw}=3780 Hz or 63pu

-voltage sensor gain= 0.06

The dc bus voltage after the voltage sensor can be written as

$$V_d = 4 + 0.4\sin(2\pi\ f_r t) \tag{4.30}$$

From (4.23) and (4.27),

$$V_c\text{=4v and } V_{bias}\text{=2 v.} \tag{4.31}$$

Substituting in (4.29) we have

$$\tau_{min} = 145.5\ \mu sec. \quad \text{Choose } \tau = 150\mu sec \tag{4.32}$$

4.4.4. Performance analysis

The performance of the proposed PWM technique is studied under (a) an ideal and (b) non-ideal dc bus and the results compared with standard SPWM outputs obtained under the same conditions.

4.4.4.1. Ideal DC Bus

The input DC bus is assumed to be ripple free, i.e. k_f=0 in (4.11). Fig. 4.37 shows a linear variation in the pu rms fundamental output voltage as a function of the modulation index. The gain is identical to that obtained with SPWM. Thus the two techniques give identical steady state results. The harmonic spectra of the line voltages obtained from the two techniques in Fig. 4.38 and are quite similar.

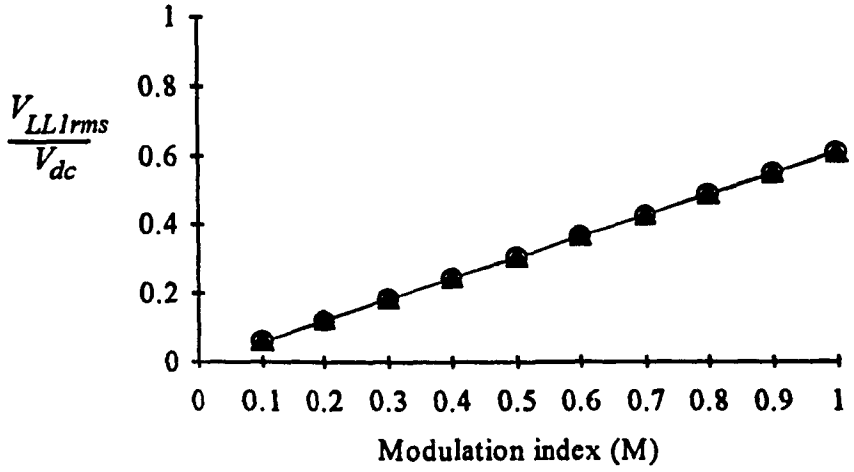


Fig. 4.37. Transfer characteristics for the proposed pattern generator and SPWM

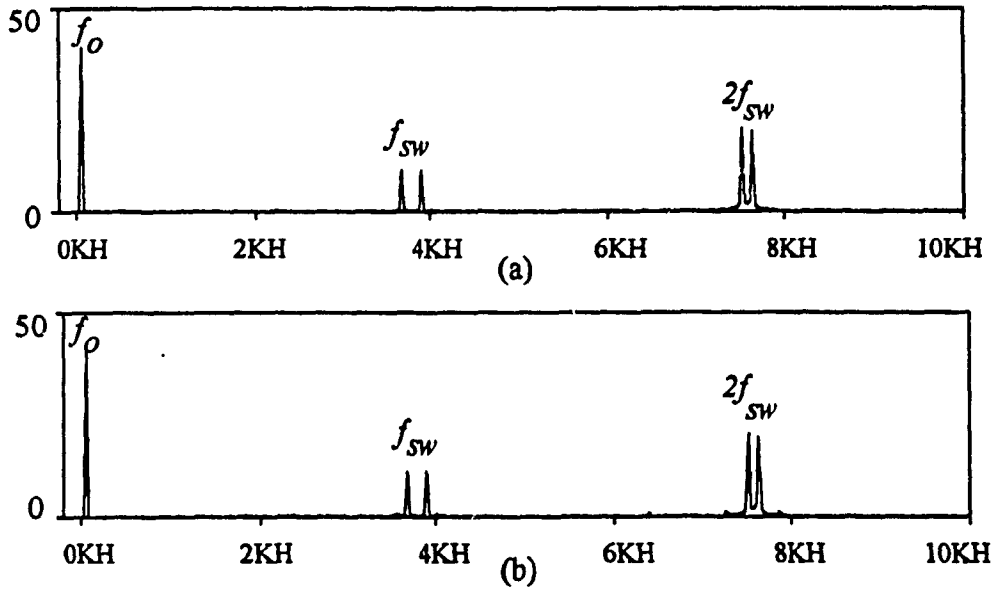


Fig. 4.38. Output line voltage harmonic spectra with an ideal dc bus under (a) SPWM. (b) Modulated Integral control . (M=0.7 f_{sw}= 63pu).

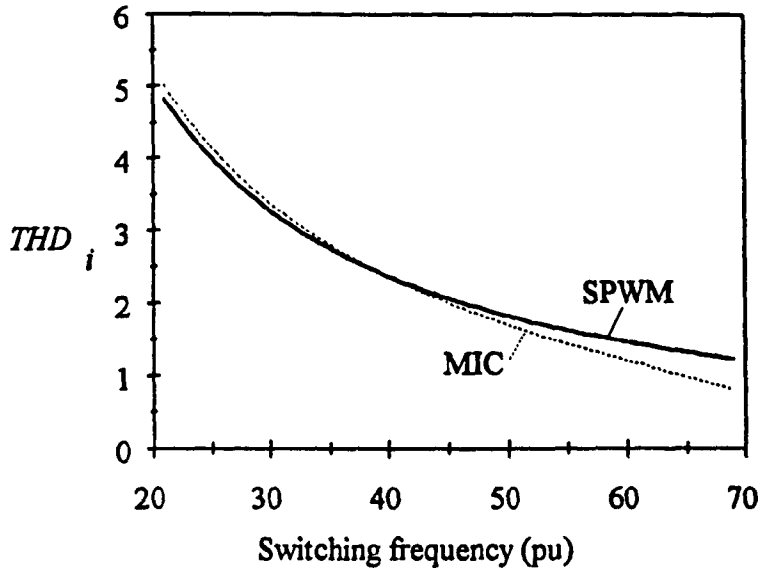


Fig. 4.39. % THD_i with a typical inductive load (R_f=10Ω, L_f=16mH) as function of switching frequency with an ideal dc bus . (M=0.7)

The total harmonic distortion in the line current (THD_i) (4.10) obtained as a function of the switching frequency was found to be comparable and even slightly better than SPWM at higher switching frequencies. This is shown in Fig. 4.39.

4.4.4.2. Dead time compensation

Power semiconductor devices like BJT or MOSFETS have finite switching times. In order to avoid shorting the dc bus, dead times are introduced in the gating signals. As reviewed in section 1.2.2.2, dead times deteriorate the quality of the output voltage. The proposed PWM pattern generator on the other hand has been found to give better results than SPWM while generating pattern on-line.

The results are obtained for a half bridge inverter with and without dead times. With a negative direction of current, the voltage input to the controller during the dead times is the dc bus voltage even though both switches in the inverter leg are off. The current now freewheels through the diode (D_1). This causes the integrator output to go

beyond the triangular wave. When the bottom switch is turned on, the output decreases with a negative slope, reducing the on time of the bottom switch. This is shown in Fig. 4.40. The dotted lines indicate the waveform without any deadtime.

With positive load current , during deadtimes, the current freewheels through the diode (D_4). This clamps the voltage input to the integrator to zero. The negative slope of the integrator output continues beyond the carrier wave and when the switch is turned on, the slope becomes positive, but reduces the on time thereby compensating for the delay. This is shown in Fig. 4.41.

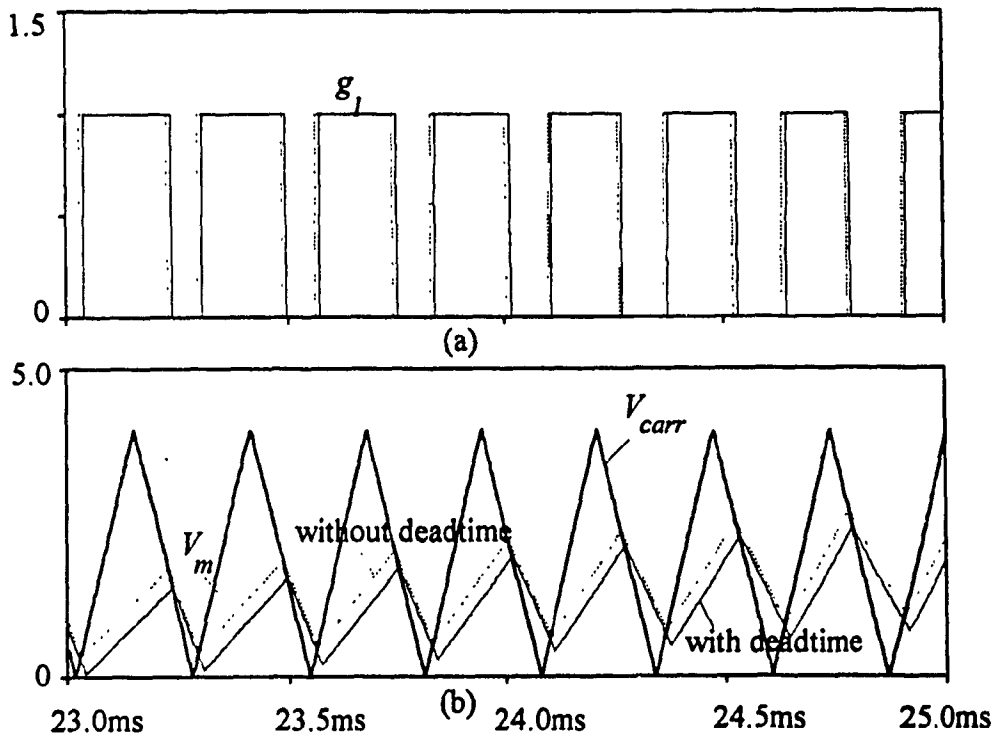


Fig. 4.40. Dead time effect for negative direction of load current. (a) Gating signal for top switch (with and without deadtimes). (b) Modulation (V_m) and carrier (V_{carr}) waveforms.

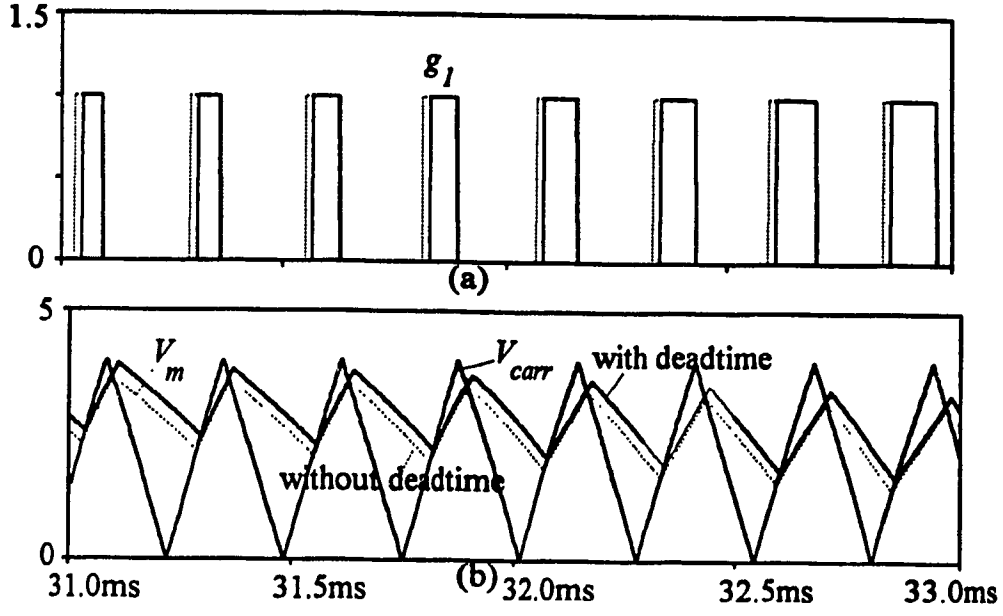


Fig. 4.41 .Dead time effect for positive direction of load current. (a) Gating signal for top switch (with and without deadtimes). (b) Modulation (V_m) and carrier (V_{carr}) waveforms.

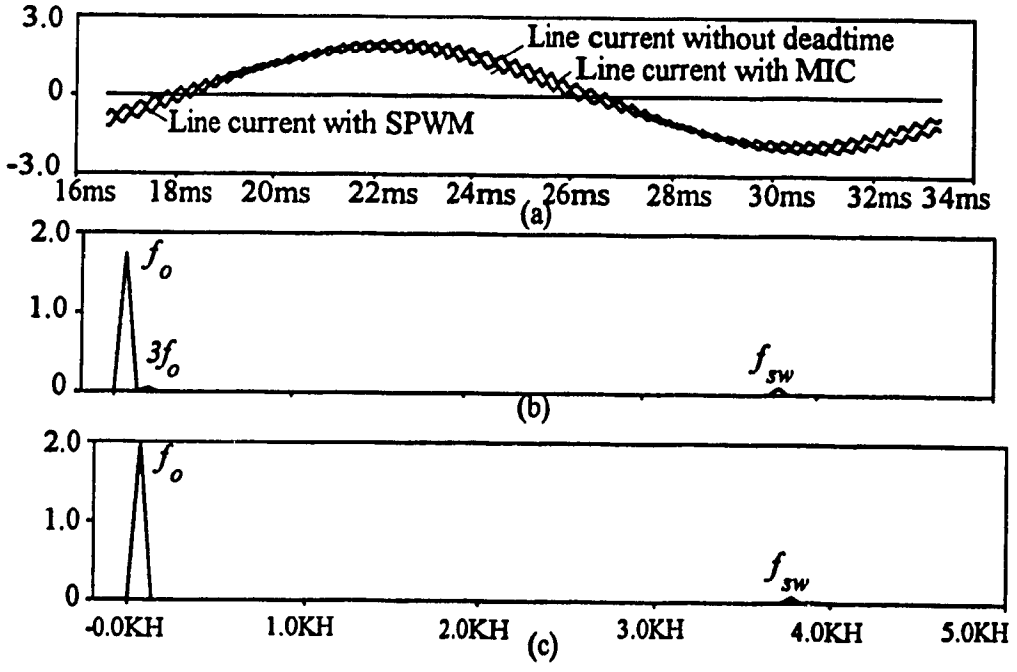


Fig. 4.42. Deadtime effect in line current of a half bridge inverter. (a) Line current (b) Harmonic spectrum of line current with SPWM. (b) Harmonic spectrum of line current under Modulated integral control (M=0.5, f_{SW}=63pu)

current obtained with the MIC for a half bridge inverter with a 10μsec deadtime is almost identical to the desired current without dead time. With SPWM technique, there is increased distortion and the current gain is reduced by 13%. This is illustrated in Fig. 4.42.

The effect in the three phase inverter is evident from the reduction in the line current distortion (Fig. 4.43) and reduction in lower order harmonics in the output line voltage(Fig. 4.44). It is also observed that the fundamental output voltage even with dead times introduced in the gating pattern is identical to the voltage obtained from a SPWM pattern without introducing dead times (Fig. 4.45). Thus this pattern generator gives a better performance than the conventional SPWM.

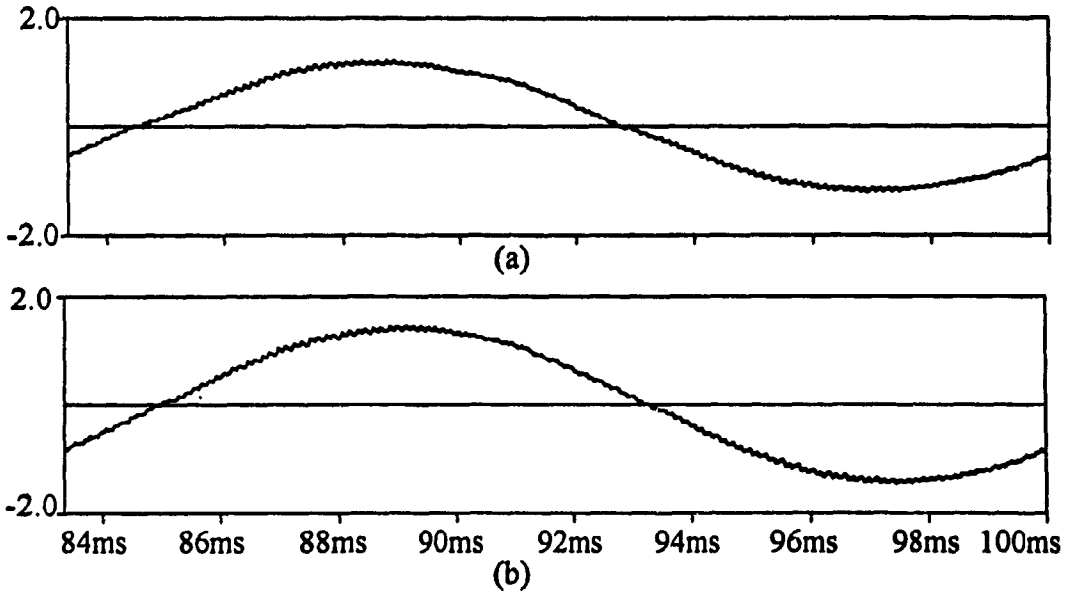


Fig. 4.43. Line current in three phase inverter with deadtime effects. (a) SPWM (b) Mod. Int. Control. (M=0.5, f_{SW}= 63pu, *deadtime* =10μsec)

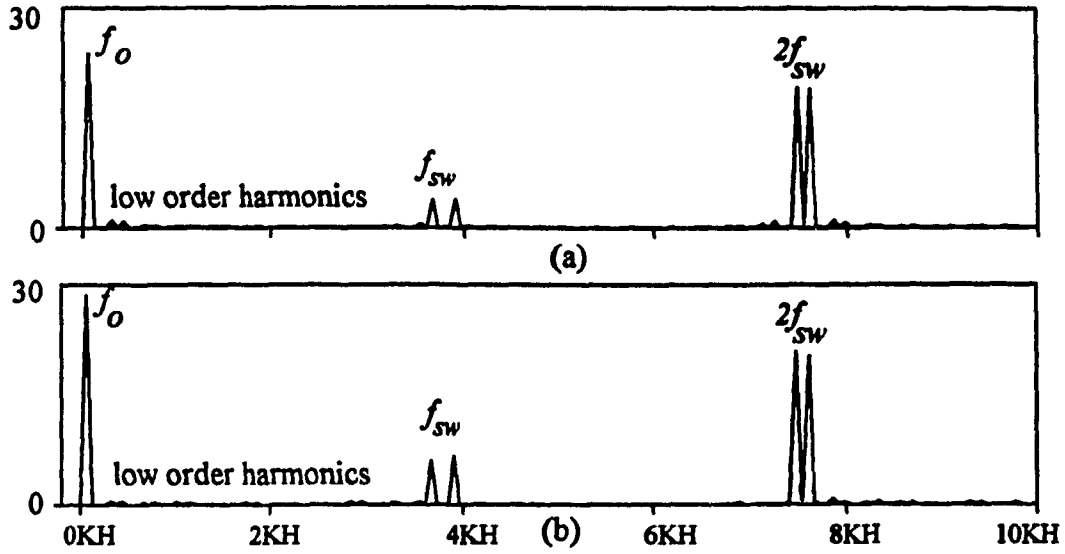


Fig. 4.44. Line voltage with deadtime effects. (a) SPWM (b) Mod. Int. Control. (M=0.5, f_{sw}= 63pu, *deadtime* =10μsec)

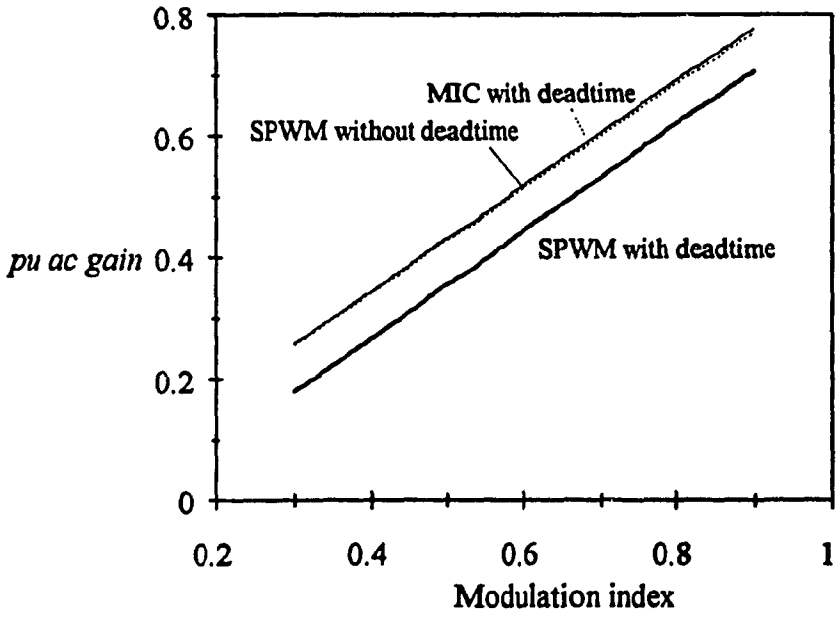


Fig. 4.45. pu ac gain versus modulation index (with and without dead time).

Thus with an ideal dc bus, the performance of the proposed pattern generator is satisfactory and comparable with the conventional SPWM pattern generator.

4.4.4.3. Non-ideal DC Bus

This section clearly brings out the advantage in using the proposed pattern generator. A better converter performance under non-ideal conditions is exhibited without much complexity in implementation. The dc bus is assumed to a have a single dominant harmonic at frequency f_r and is given by (4.11)

The effectiveness of the proposed pattern generator is evaluated by measuring the harmonic rejection ability in the output voltage. This study is carried out for dominant ripple frequencies of 6pu (360 Hz) and 2pu (120 Hz) with the inverter fundamental operating frequency of 1pu (60Hz).

With f_r= 6pu, the output low order harmonics (Table I) are the 5^{th} and 7^{th}. The harmonic rejection ability is measured quantitatively by the total low order harmonic distortion given by the following equation

$$THD_{lv} = \frac{\sqrt{V_5^2 + V_7^2}}{k_r V_{dc}} \tag{4.33}$$

This factor is a measure of only the low order harmonics (excluding switching harmonics). The effect is analogous to a single harmonic with the rms value given by the rms value of each of the individual harmonics. A plot as a function of switching frequency is obtained in Fig. 4.46 and better results are obtained with the proposed technique.

With f_r= 2pu, the dominant low order harmonic is 3pu (Table I). Thus the total low order harmonic distortion is defined as

$$THD_{lv} = \frac{V_3}{k_r V_{dc}} \tag{4.34}$$

(4.34) is plotted as a function of switching frequency in Fig. 4.47. Again a performance superior to the conventional SPWM was obtained with proposed technique.

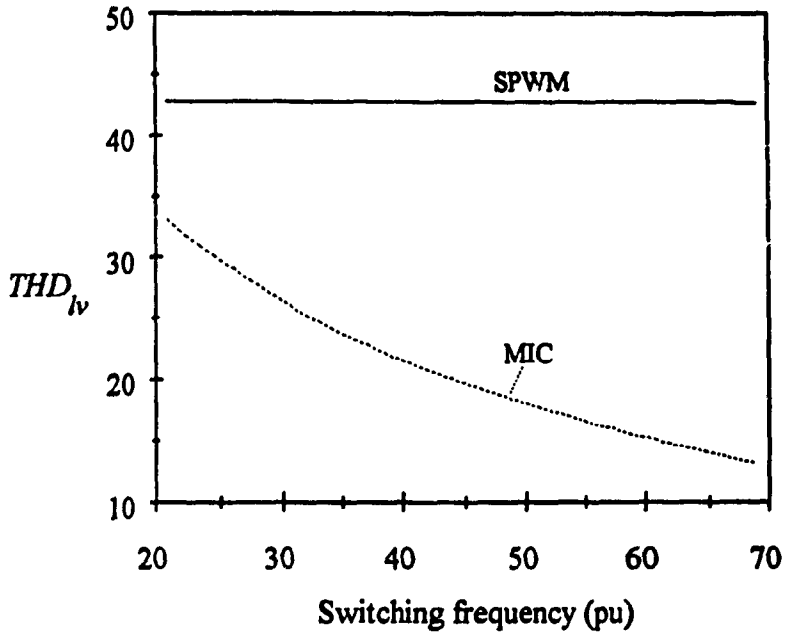


Fig. 4.46. Total low-order harmonic distortion ($\%THD_{lv}$) versus switching frequency. (M=0.7, f_r=6pu, k_r=0.1)

The harmonic distortion in line current (THD_i) (4.10) for f_r= 6pu and k_r=0.1 is found to be reduced with the proposed technique giving a high quality line current.(Fig. 4.48).

These results are also evident from the harmonic spectra of the line voltages in Fig. 4.49 in which better harmonic rejection is obtained with the modulated integral control technique. The results are compared with the standard SPWM. The line harmonics are suppressed to a greater extent yielding a better quality output voltage with the desired fundamental value.

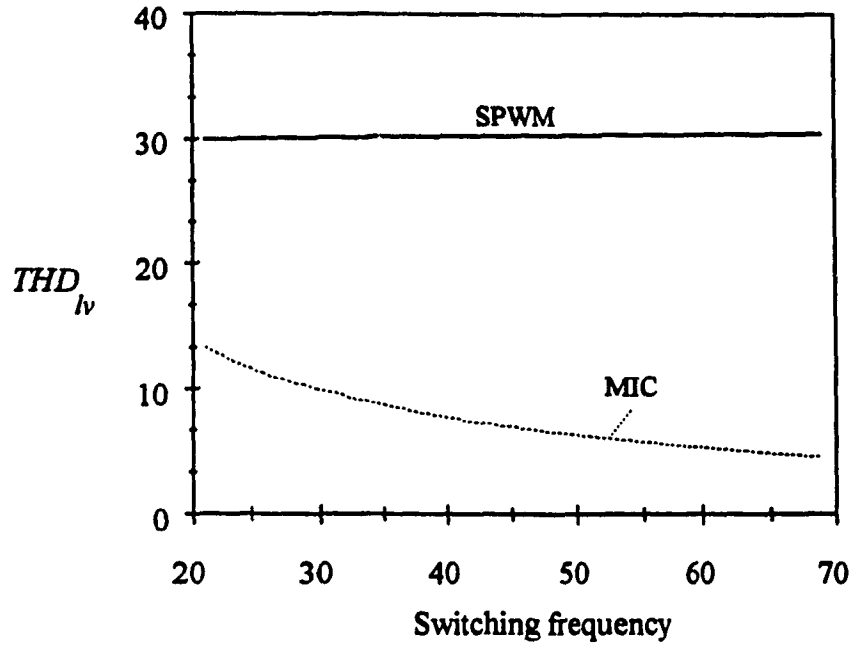


Fig. 4.47. Total low-order harmonic distortion ($\%THD_{lv}$) versus switching frequency. (M=0.7, f_r=2pu, k_r=0.1)

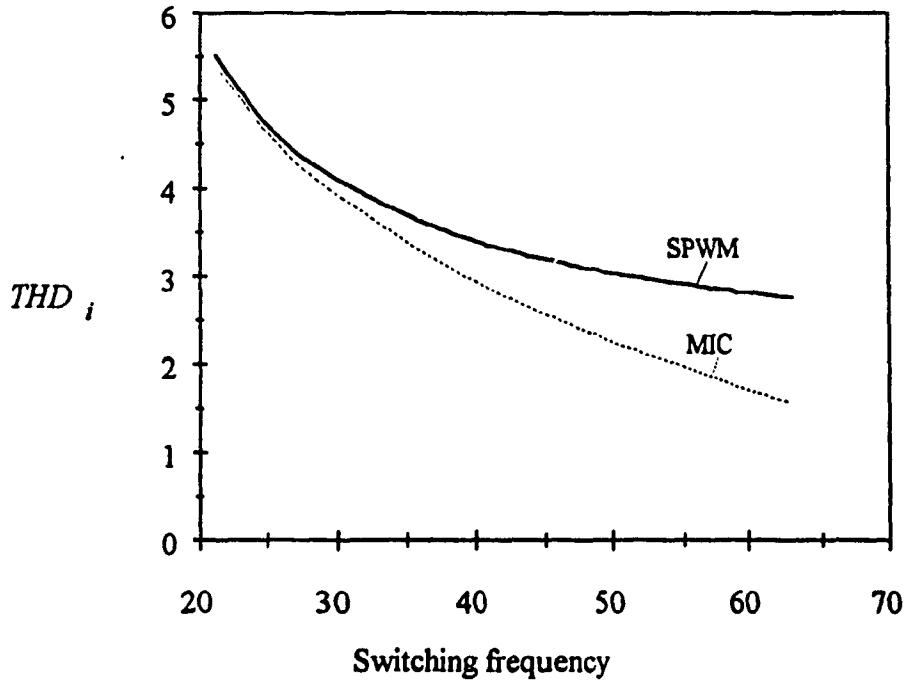


Fig. 4.48. Total current harmonic distortion ($\%THD_i$) versus switching frequency with 10% 360 Hz ripple (M=0.7)

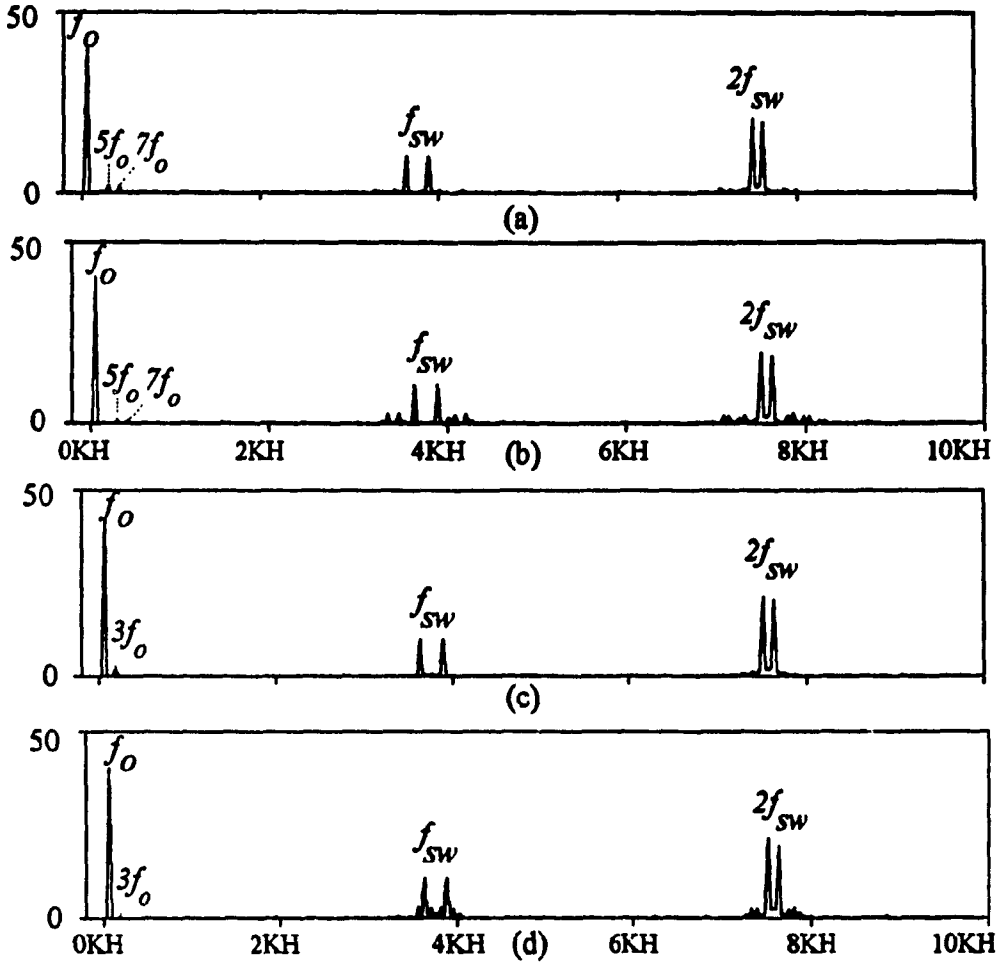


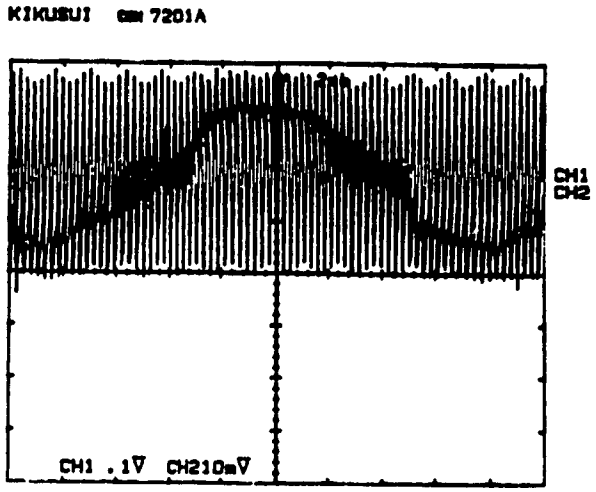
Fig. 4.49. Line voltage spectra under (a) Mod. Int. Control (f_r= 6pu) (b) SPWM (f_r=6pu). (c) Mod. Int. Control (f_r= 2pu) (d) SPWM (f_r= 2pu)

4.4.5. Experimental results

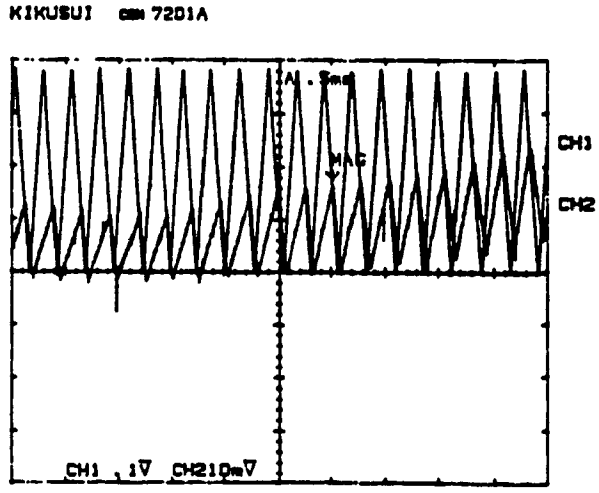
To verify the key simulation results, a 3kVA prototype was built in the laboratory. Key control waveforms are shown in Fig. 4.50. The intersections of the modulating wave with the carrier wave determine the switching instants.

With balanced input conditions the line voltage, its spectrum and line current are obtained in Fig, 4.51.

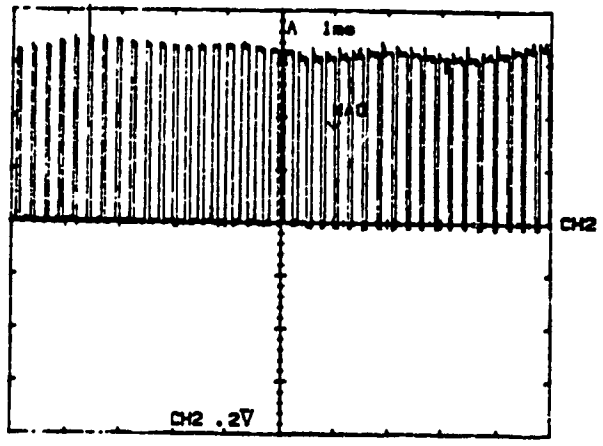
For unbalanced conditions, one of the inputs to the diode bridge was opened. The resulting line voltage, its harmonic spectrum and the line current are shown in Fig, 4.52.



(a)

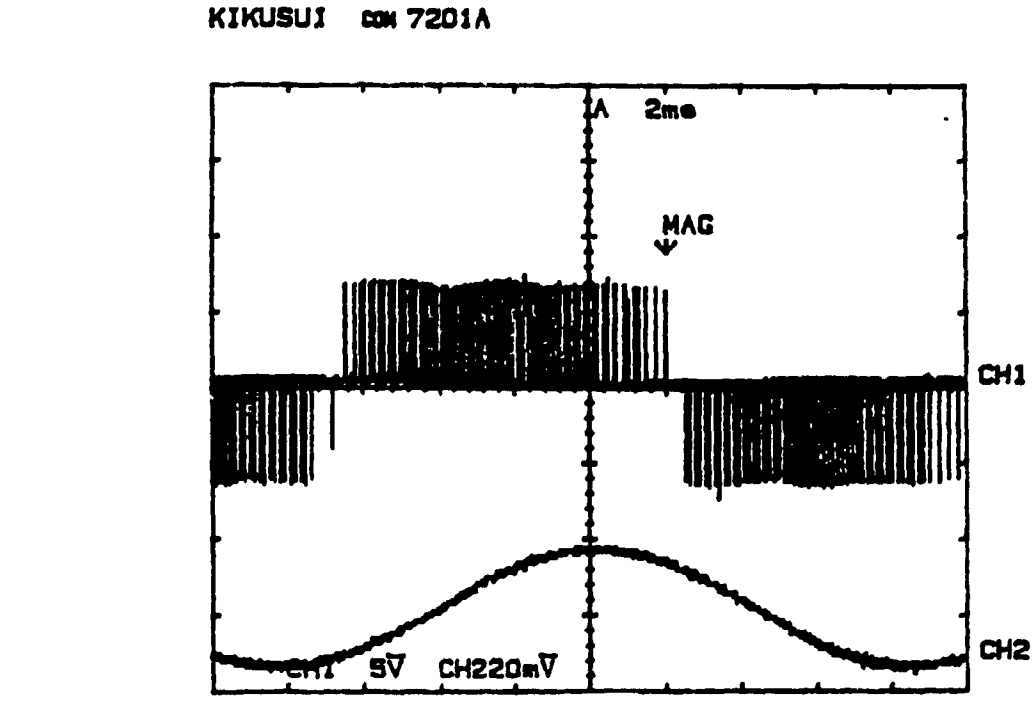


(b)

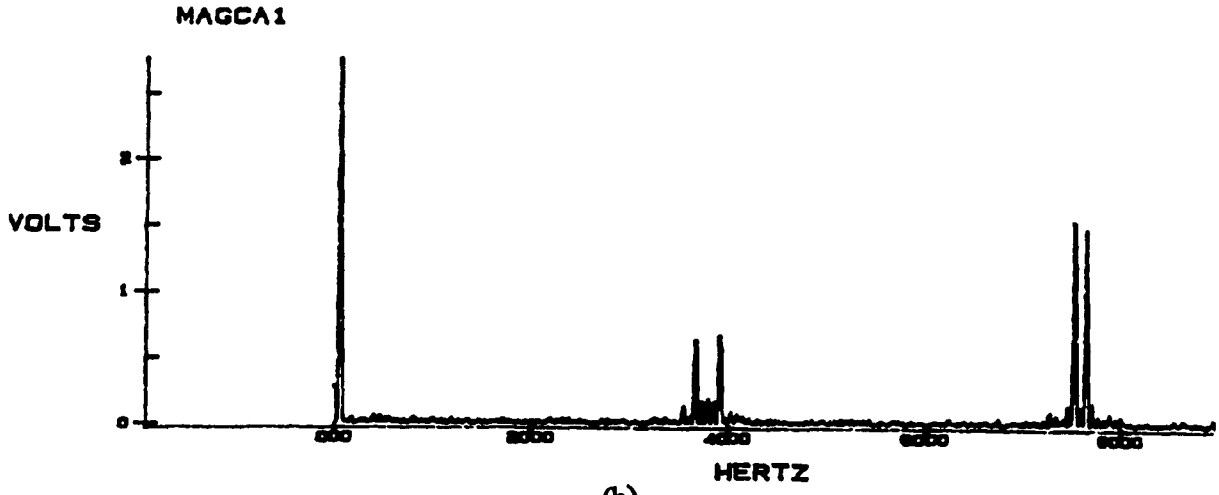


(c)

Fig. 4.50. Control waveforms for modulated integral control. (a). Triangular carrier and modulating waveform. (b) Detailed view of control waveforms. (c) Voltage across the bottom switch. (M=0.6, f_{sw}=3780 Hz)

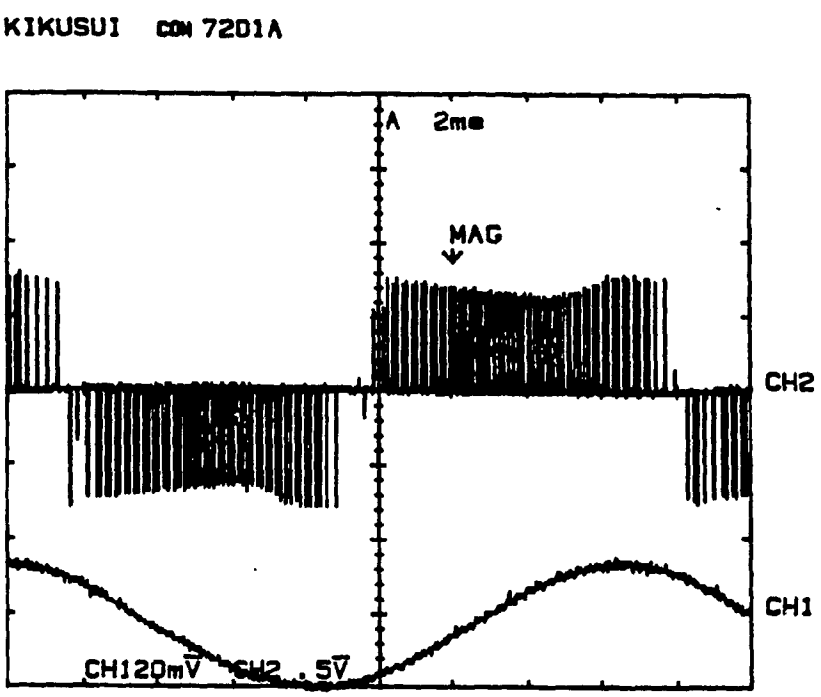


(a)

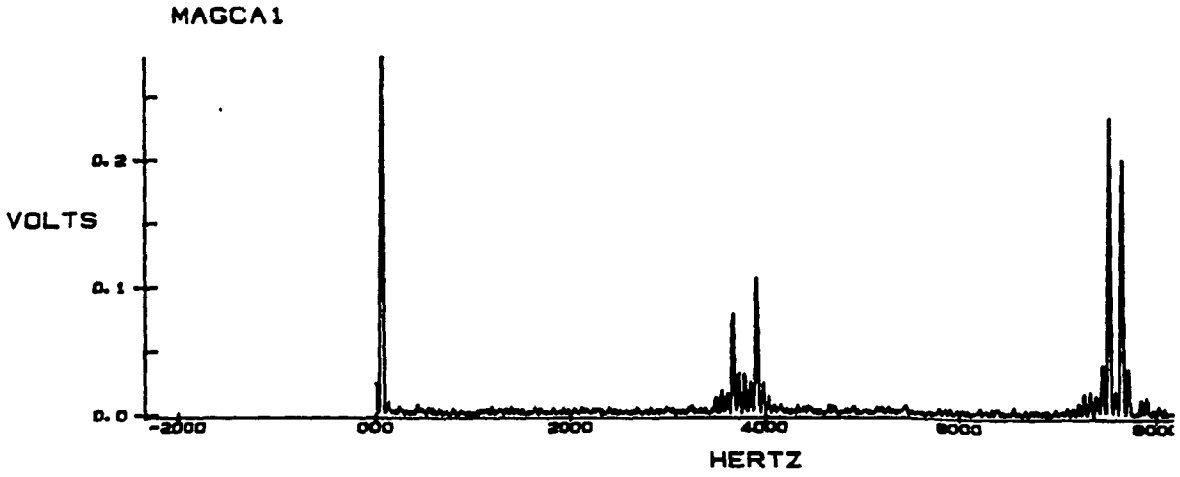


(b)

Fig. 4.51. Inverter waveforms for balanced operating conditions. (a) Line voltage and line current. (b). Harmonic spectrum of the line voltage.



(a)



(b)

Fig. 4.52. Inverter waveforms for unbalanced operating conditions. (a) Line voltage and line current. (b). Harmonic spectrum of the line voltage.

4.5. Conclusions

In this chapter two simple on-line pattern generators for voltage source inverters based on the concept of output voltage integral are analyzed and implemented. They minimize the effects of DC bus ripple and switch dead time and delays in the inverter output thus improving the quality of the output voltage. The techniques are easy to implement using digital and analog circuits. Experimental results on a 3 kVA prototype unit confirm the feasibility of the pattern generators.

CHAPTER 5

CONCLUSIONS

5.1. Conclusions

This thesis provides an insight into the problems of a non-ideal switching environment present in a converter system and justifies the need to carry out this work. The non-ideal conditions identified in this thesis are (a) presence of ripple voltage on the dc bus (b) switching delays and conduction drops accompanying a practical power device. There impact on the performance of the converter system is explained. The concept of output voltage integral control is further extended to identify two control schemes, Reset Integral Control and Modulated Integral Control with a potential of providing inherent compensation to the afore-mentioned non-ideal conditions. These control schemes are implemented in PWM pattern generators for dc-dc and dc-ac converters. The choice of the reference voltage helps in maintaining the desired output voltage. Moreover, the location of the voltage sensor in either case helps in compensating the switch conduction drops encountered in the power circuit.

In a dc-dc converter the proposed control schemes are identified to be feedforward in nature and found to provide very good performance especially under harsh switching environment. They can be used as voltage pre-regulators for feedback loop design.

In a dc-ac converter, two on-line pattern generators are implemented on the principle of output voltage integral control and found to provide better performance than conventional SPWM pattern generator. In particular the Reset Integral Control scheme is found to provide good input harmonic rejection while Modulated Integral Control is found to provide adequate compensation for switching delays while rejecting source harmonics.

Thus a superior performance with almost the same component count and complexity as the conventional pattern generators is realized. Performance features are illustrated through computer simulations. Experimental results obtained on laboratory prototypes confirm the feasibility of the pattern generators.

5.2. Suggestions for future research work

There is a scope of further research in this thesis. In particular:

- to increase the voltage gain, third harmonic voltage can be injected in the control reference voltage.

- a control scheme to extract phase information is implemented for a feedforward rectifier[42]. The same principle can be used in this controller. Each phase voltage can be reconstructed from line AB and line BC instead. Thus only two sensors are necessary. In addition by placing the sensors in the line, the conduction voltage drops for both switches can be taken into consideration, thus improving the performance further.

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APPENDIX

A.1. Power and control circuit diagrams

The layout of a dc-dc converter is shown in Fig. A.1 This converter can be controlled either by the reset integral controller (Fig. A.2) or the modulated integral controller.(Fig. A.3).

The schematic diagram of the dc-ac converter is shown in Fig. A.4. The dc-ac converter is operated to work either under reset integral control (Fig. A.5) or the modulated integral control (Fig. A.7). The reference voltage is shown for only phase A (Fig. A.6) and can be easily obtained for the phase B and C.

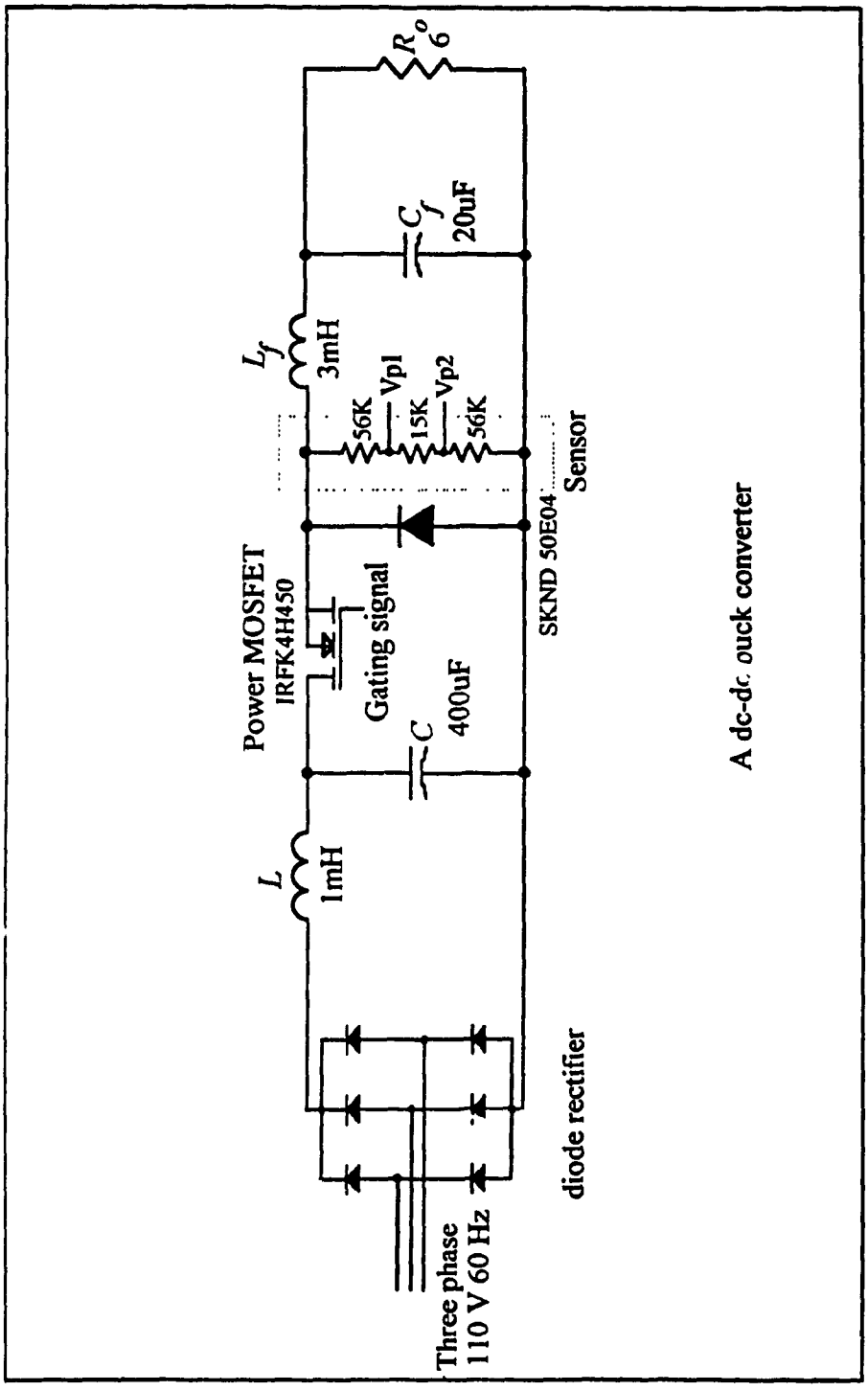


Fig. A.1. Power circuit of a dc-dc converter

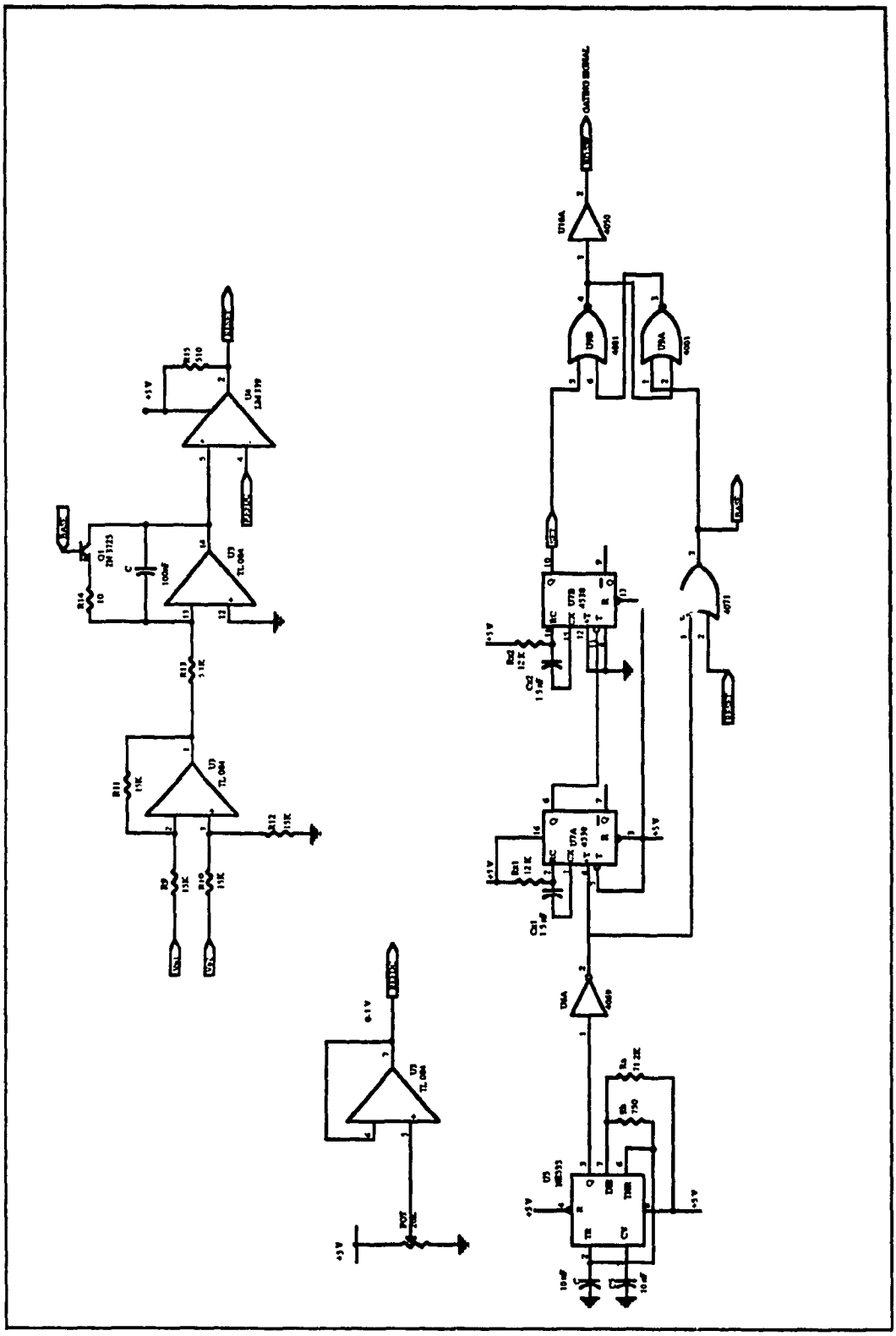


Fig. A.2. Reset integral control technique for dc-dc converter

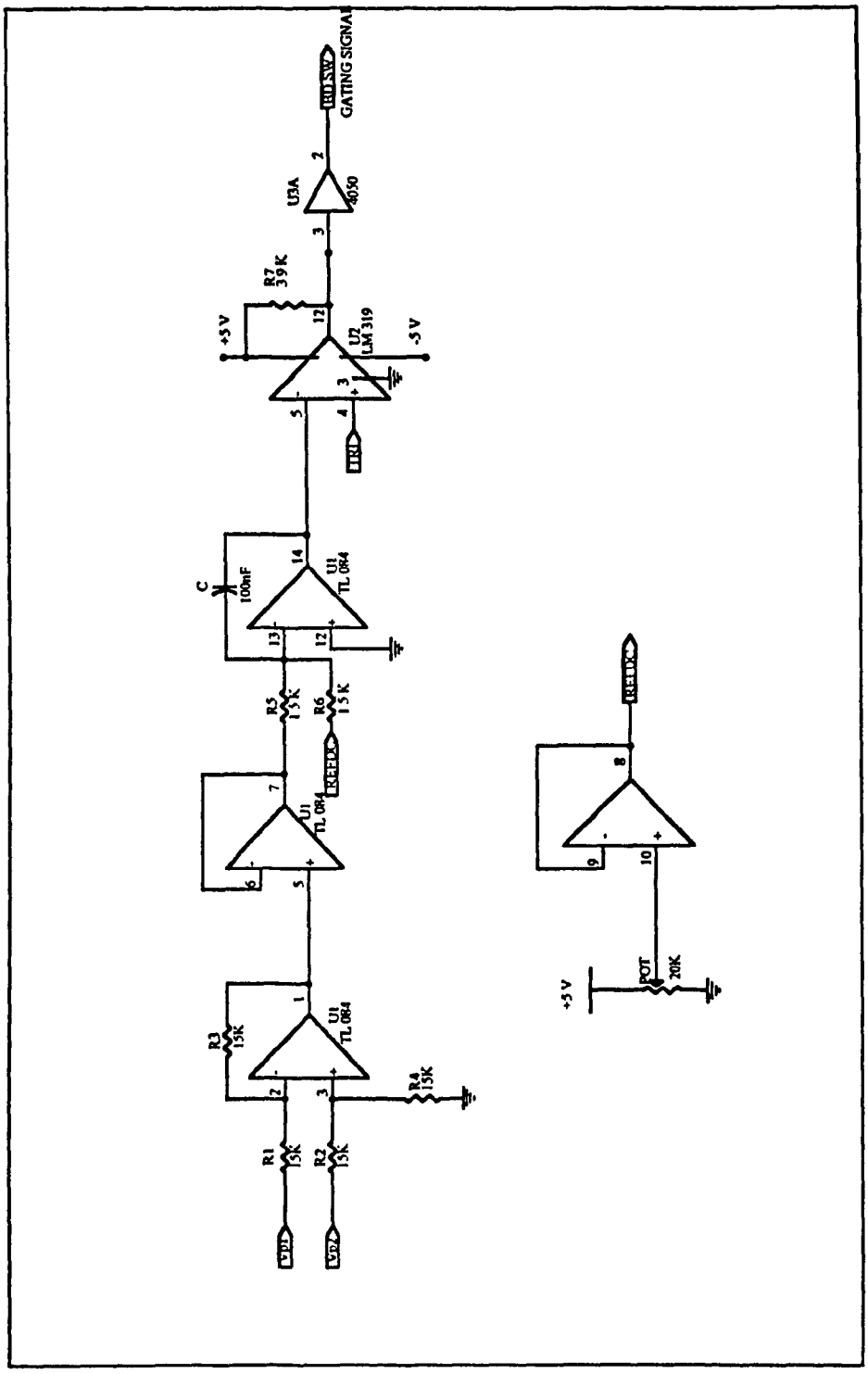


Fig. A.3. Modulated integral control technique for dc-dc converter

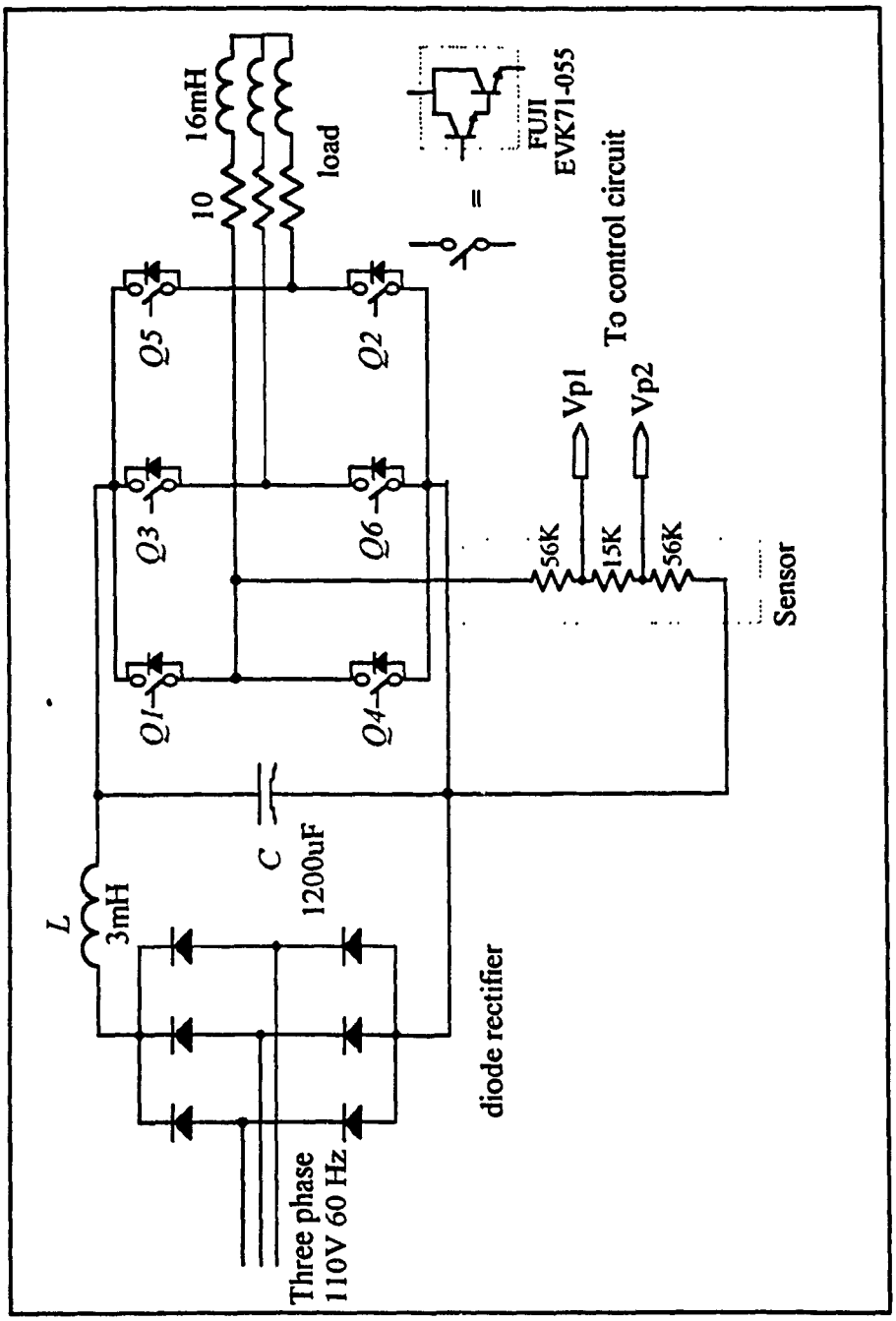


Fig. A.4. Power circuit of a dc-ac converter

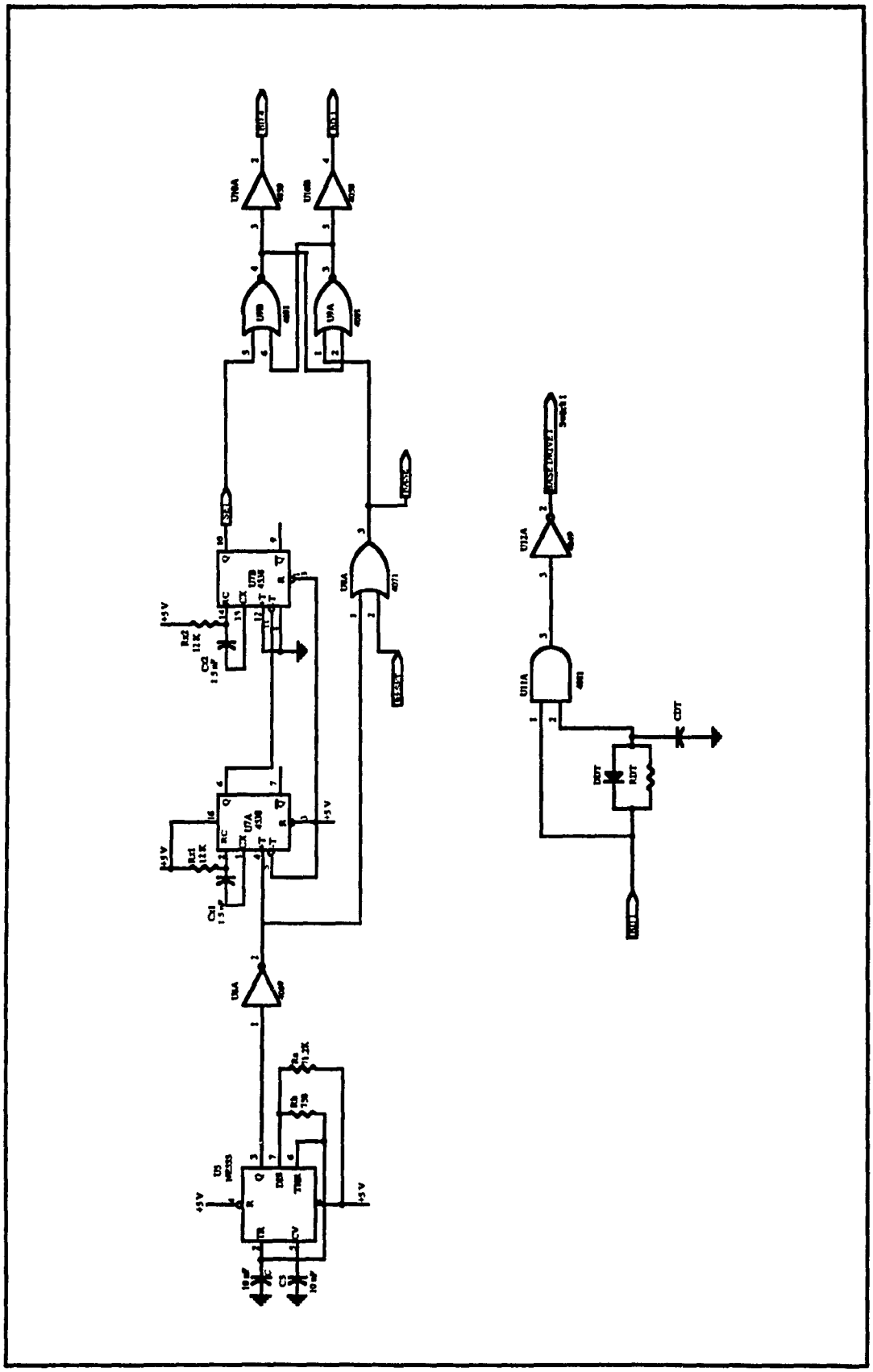


Fig. A.5. Generation of gating signal for a dc-ac converter using RIC(Phase A)

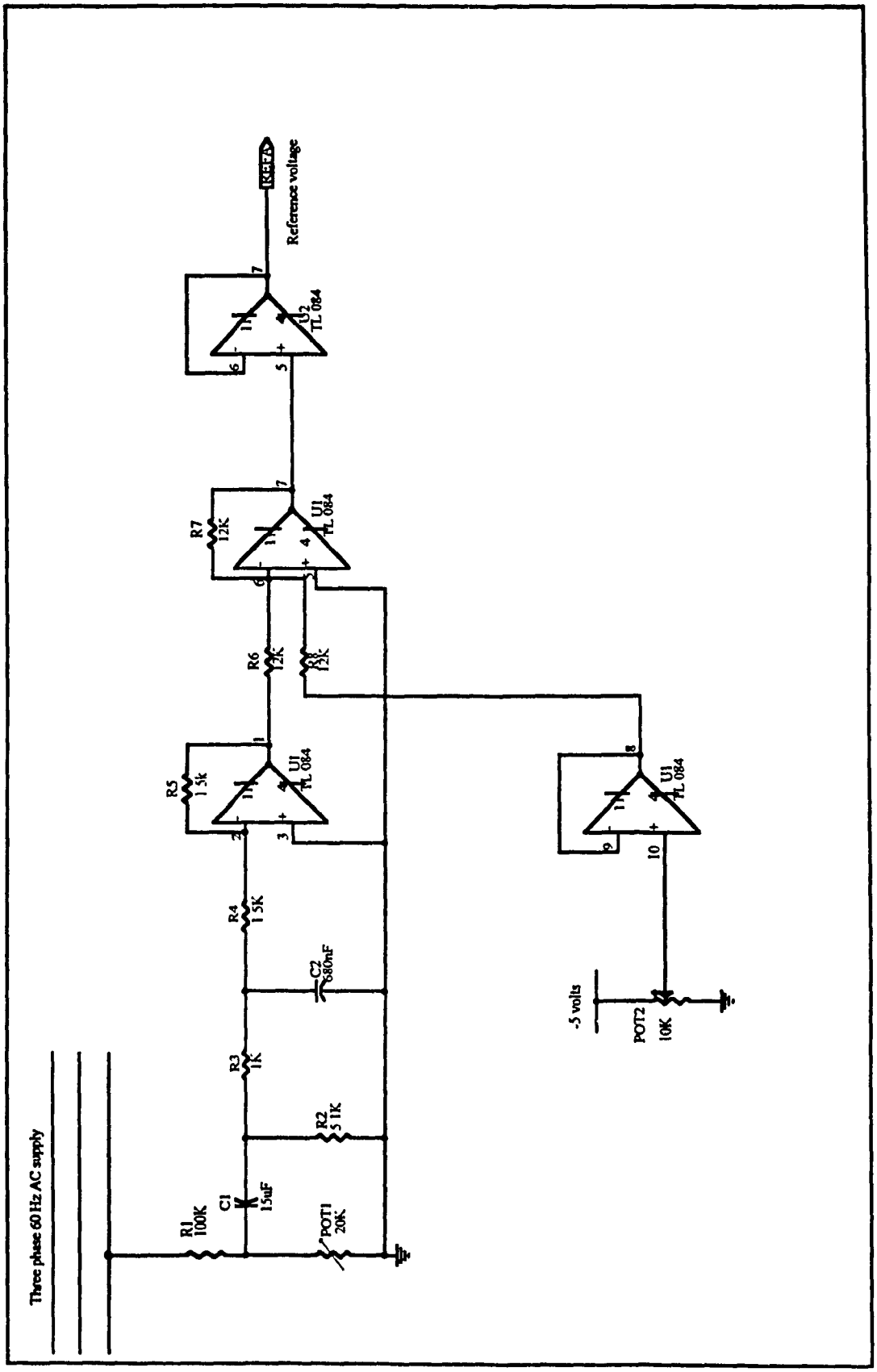
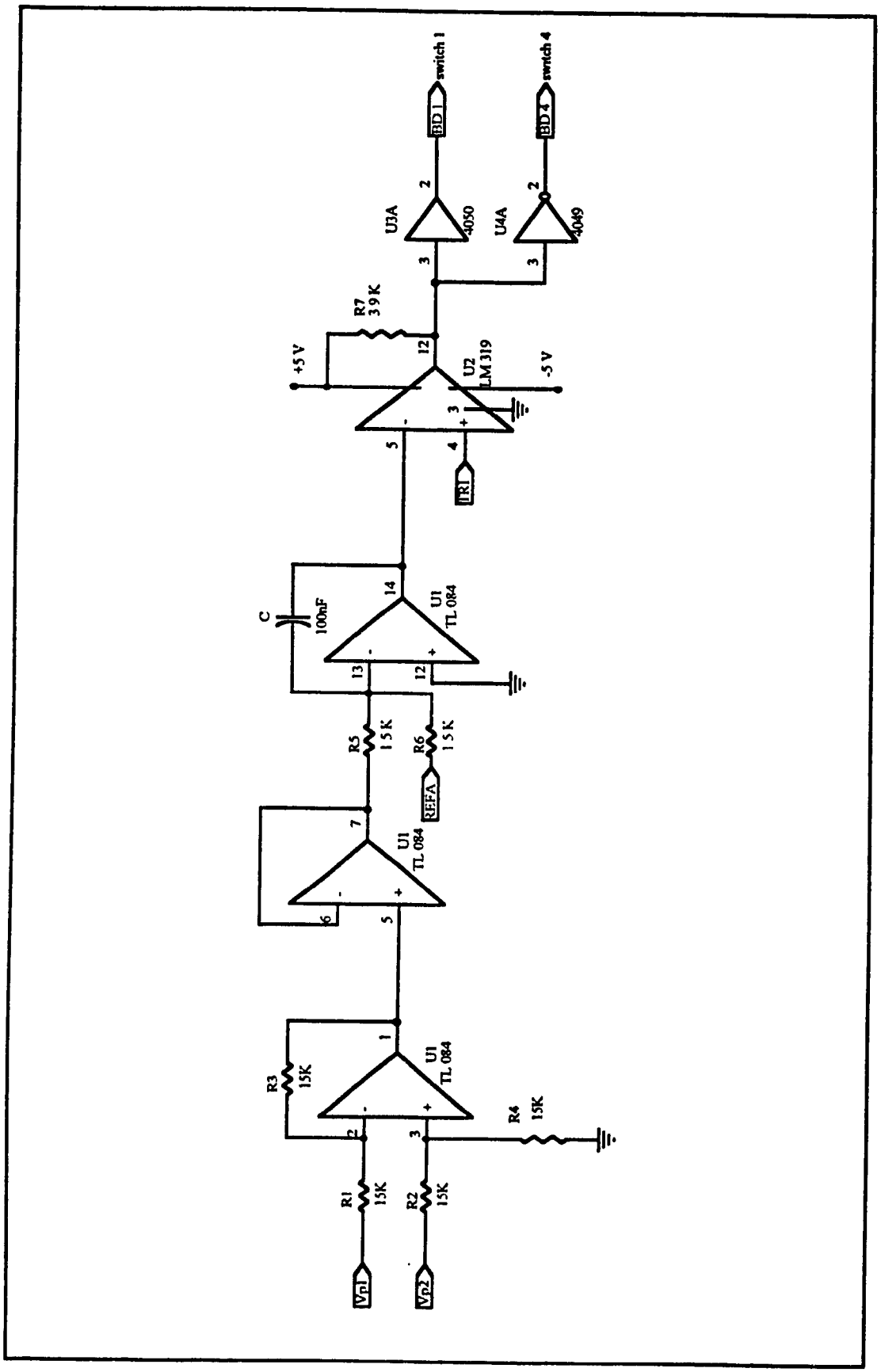


Fig. A.6. Generation of reference voltage for dc-ac converters



A.7. Generation of gating signals for dc-ac converter using MIC(Phase A)

A.2. Computation of the switching function for a dc-dc converter under reset integral control

In this section, the switching function of the output voltage under reset integral control is mathematically computed. This can be used in computing the harmonics in the output voltage for a given input voltage in (3.15)

The approach in computing the switching function is to represent each of the M pulses of the switching function in complex fourier series and then adding them, where M is the ratio of the switching(f_{sw}) to the ripple frequency(f_r). The first pulse can be drawn as:

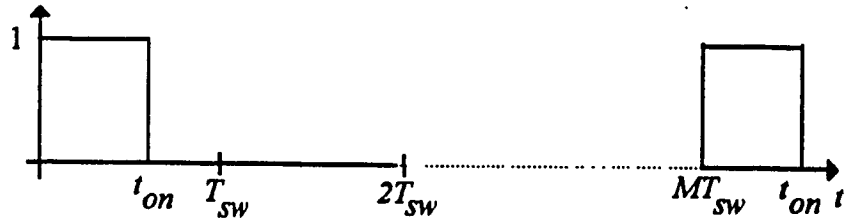


Fig. A.8. First pulse with periodicity of MT_{sw}

The pulse in any general k^{th} interval can be drawn as

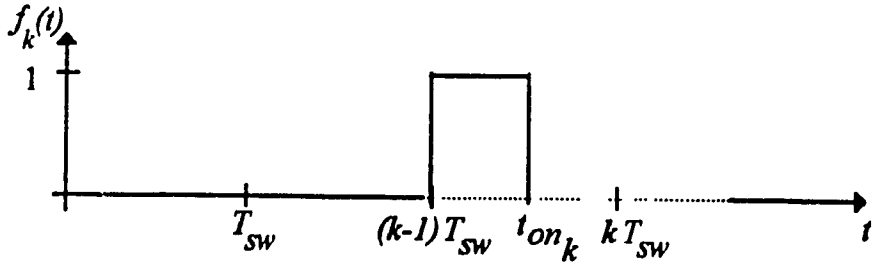


Fig. A.9. Pulse in the general k^{th} interval

The above function can be expressed in complex fourier series as:

$$f_k(t) = f_{1k} + \sum_{\substack{n=-\infty \\ n\neq 1}}^{n=+\infty} C_{n,k} e^{jn\omega_m t} e^{-j2\pi nK\omega(k-1)} \tag{A.1}$$

where

$$f_{1k} = \frac{\theta_{on_k}}{2\pi M} \quad \text{and}$$
$$C_{n,k} = \frac{1}{-j2\pi n}(e^{-jnK_f\theta_{on_k}} - 1) \tag{A.2}$$

where $$\omega_{sw}T_{sw} = 2\pi, \omega_{sw}t_{on_k} = \theta_{on_k} \text{ and } K_f = \frac{1}{M} \tag{A.3}$$

Thus the complete switching function can be expressed as:

$$f(t) = \sum_{k=1}^{M} f_{1k} + \sum_{k=1}^{M} \sum_{\substack{n=-\infty \\ n\neq 1}}^{n=+\infty} C_{n,k} e^{jn\omega_r t} e^{-j2\pi nK_f(k-1)} \tag{A.4}$$

To compute the expression for on time t_{on_k}, reference to Fig. A.10 is made.

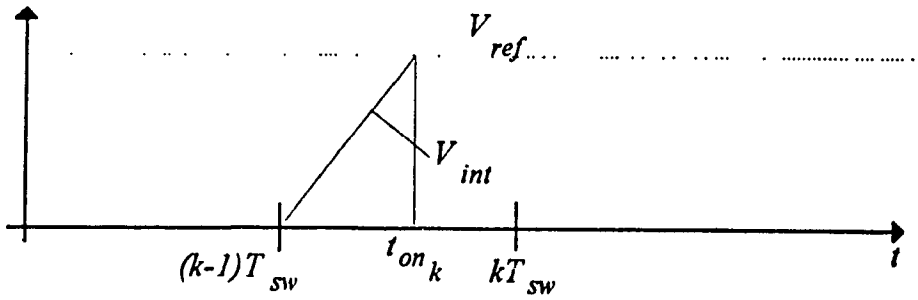


Fig. A.10. Output of integrator in any k^{th} interval to determine the on time(t_{on_k})

Let the input be dominant in one harmonic at a frequency ω_r, and be given by

$$V_d(t) = V_{dc} + k_r V_{dc} \sin(\omega_r t) \tag{A.5}$$

Integrator output in any general k^{th} interval is:

$$V_{int} = \frac{1}{\tau} \int_{(k-1)T_{sw}}^{(k-1)T_{sw}+t_{on_k}} V_d(t)\, dt \tag{A.6}$$

At the instant the integrator output touches the reference:

$$V_{ref} = \frac{1}{\tau} \int_{(k-1)T_{sw}}^{(k-1)T_{sw}+t_{on_k}} (V_{dc} + k_r V_{dc} \sin(\omega_r t))dt \qquad \text{(A.7)}$$

Solving the integral and transforming into angle domain we have:

$$V_{ref} = \frac{1}{\tau}\{V_{dc} t_{on_k} + k_r \frac{V_{dc}}{\omega_r}(\cos(K_f \omega_{sw} T_{sw}(k-1)) - \cos(K_f \omega_{sw}(T_{sw}(k-1) + t_{on_k})))\}$$

(A.8)

The equation can be rewritten as

$$\theta_{on_k} = 2\pi D - \frac{k_r}{K_f}[\cos(2\pi K_f (k-1)) - \cos(2\pi K_f (k-1) + K_f \theta_{on_k})] \qquad \text{(A.9)}$$

This expression for the on-time angle can then be substituted in eqns. (A.1) through (A.3) and the switching *f(t)* (A.4) computed.

A.3. Computation of the switching function for a dc-dc converter under modulated integral control

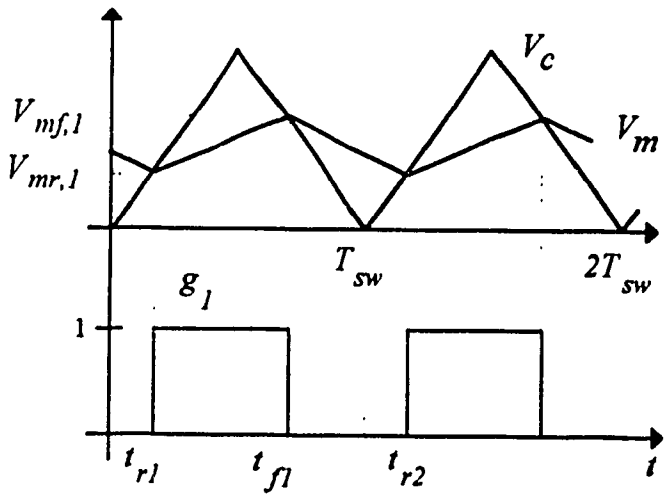


Fig. A.11. Computation of switching function for modulated integral control

The procedure for calculating the switching function under modulated integral control is similar to that in section A.1. The switching function can be expressed in the complex fourier series as:

$$f(t)=\frac{1}{2\pi M}\sum_{k=1}^{M}(\theta_{f,k}-\theta_{r,k})+\sum_{n=-\infty}^{\infty}\left(\sum_{k=1}^{M}C_{n,k}e^{-j2\pi nK_f(k-1)}\right)e^{jn\omega t} \quad (A.10)$$

$$\text{where } C_{n.k}=\frac{1}{-j2\pi n}(e^{-jnK_f\theta_{f,k}}-e^{-jnK_f\theta_{r,k}}) \quad (A.11)$$

The angles $\theta_{r,k}=\omega_{sw}t_{r,k}$ and $\theta_{f,k}=\omega_{sw}t_{f,k}$ can be obtained by inspection of Fig. A.11. Because of triangular wave modulation, an iterative procedure has to be adopted. Since $\omega_{sw}T_{sw}=2\pi$, the triangular wave is expressed as:

$$\begin{aligned} V_c(\theta)&=\frac{1}{\pi}\theta \qquad 0\le\theta\le\pi \\ &=1-\frac{\theta-\pi}{\pi} \quad \pi\le\theta\le 2\pi \end{aligned} \quad (A.12)$$

With an arbitrarily selected t_{r1}, the first intersection between triangular wave and carrier wave can be written as:

$$V_c(\theta_{r,1})=V_{mr,1}=\frac{\theta_{r,1}}{\pi} \quad (A.13)$$

The next intersection point governs the on time of the dc-dc converter and is determined by solving the following equation.

$$V_{mf,1}=V_{mr,1}+\frac{1}{\tau}\int_{t_{r,1}}^{t_{f,1}}((1-V_{dc})+V_{sh}\sin(\omega_r t)dt \quad (A.14)$$

where $V_{mf,1}$ can be expressed as

$$V_c(\theta_{f,1})=V_{mf,1}=1-\frac{\theta_{f,1}-\pi}{\pi} \quad (A.15)$$

Solving the integral in (A.14)

$$V_{mf,1}=V_{mr,1}+\frac{1}{\tau}(1-V_{dc})(t_{f,1}-t_{r,1})+\frac{V_{sh}}{\tau K_f\omega_{sw}}(\cos(K_f\theta_{r,1})-\cos(K_f\theta_{f,1})) \quad (A.16)$$

Substituting (A.15) yields the following equation

$$2\pi K_f K_\tau (2-\frac{\theta_{f,1}}{\pi}-V_{mr,1}) = K_f (1-V_{dc})(\theta_{f,1}-\theta_{r,1})+V_{sh}(\cos(K_f\theta_{r,1})-\cos(K_f\theta_{f,1}))$$

(A.17)

Rearranging (A.17) gives the equation to compute the switching angle

$$\theta_{f,1}= V_{sh}(\cos(K_f\theta_{f,1})-\cos(K_f\theta_{r,1}))+\frac{2\pi K_f K_\tau (2-V_{mr,1})+K_f(1-V_{dc})\theta_{r,1}}{K_f(1-V_{dc}+2K_\tau)}$$

(A.18)

This is a transcendental equation and can be solved for θ_{f1}.

To determine the off time of the converter, negative slope of the modulation wave is considered and the intersection with the triangular wave determines the turning on instant of the switch(t_{r2}) which is determined by the equation

$$V_{mr,2} = V_{mf,1}-\frac{1}{\tau}\int_{t_{f1}}^{T_{sw}+t_{r2}} V_{dc}\,dt \qquad \text{(A.19)}$$

Solving the integral in (A.19) yields

$$V_{mr,2} = V_{mf,1}-\frac{V_{dc}}{\tau}(T_{sw}+t_{r2}-t_{f1}) \qquad \text{(A.20)}$$

From (A.12), $V_{mr,2}$ is given as:

$$V_{mr,2} = \frac{\theta_{r,2}}{\pi} \qquad \text{(A.21)}$$

Substituting (A.21) in (A.20) yields:

$$\theta_{r,2} = \frac{-V_{dc}(2\pi-\theta_{f,1})+2\pi K_\tau V_{mf,1}}{2K_\tau+V_{dc}} \qquad \text{(A.22)}$$

This is used to calculate $\theta_{f,2}$ and the procedure repeated for a complete cycle at the end of which new$\theta_{r,1}$ will be calculated. The procedure is repeated till the value converges. The angles are then substituted in (A.10) through (A.11) to compute the switching function *f(t)*.

A.4. Computation of switching function under reset integral control for a dc-ac converter.

In this section, the line switching function is expressed mathematically. This can be used to theoretically confirm the harmonic rejection capability of the proposed control scheme.

The procedure involves computing the complex Fourier series for each of the pulses in the switching function and then adding them together to yield the complete switching function.

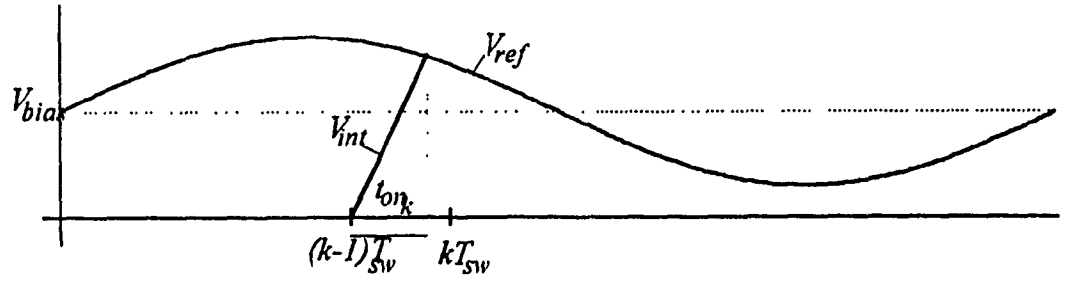


Fig. A.12. Determination of on time for a general pulse in the k^{th} interval

With reference to Fig. A.12 and considering the k^{th} interval, the on time (t_{on_k}) is determined by the intersection of the integrator output with the sinusoidal control reference. Thus for phase A:

$$\frac{1}{\tau}\int_{(k-1)T_{sw}}^{(k-1)T_{sw}+t_{on_k}} (V_{dc} + k_r V_{dc}\sin(\omega_r t)dt = V_{bias} + V_m \sin(\omega_o((k-1)T_{sw} + t_{on_k})) \quad \text{(A.23)}$$

Using (4.5)

$$\frac{1}{\tau}\int_{(k-1)T_{sw}}^{(k-1)T_{sw}+t_{on_k}} (V_{dc} + k_r V_{dc}\sin(\omega_r t)dt = V_{bias}(1 + M\sin(\omega_o((k-1)T_{sw} + t_{on_k})) \quad \text{(A.24)}$$

This expression can be simplified and rewritten as:

$$V_{dc}\frac{t_{on_k}}{\tau}+\frac{k_r V_{dc}}{\tau\omega_r}[\cos(\omega_r(k-1)T_{sw})-\cos(\omega_r((k-1)T_{sw}+t_{on_k}))]= V_{bias}(1+M\sin(\omega_o((k-1)T_{sw}+t_{on_k})) \quad \text{(A.25)}$$

Let $\omega_{sw}=M_f\omega_r$ and $\omega_{sw}=N\omega_o$.

Translating into the angle domain by the transformation:

$$\omega_{sw}T_{sw}=2\pi$$
$$\omega_{sw}t_{on_k}=\theta_{on_k} \quad \text{where } 0\le\theta_{on_k}\le 2\pi \quad \text{(A.26)}$$

(A.25) can be rewritten

$$V_{dc}\frac{t_{on_k}}{\tau}+\frac{k_r V_{dc}}{\tau K_m\omega_{sw}}[\cos(2\pi K_m(k-1))-\cos(2\pi(k-1)K_m+\theta_{on_k}))]= V_{bias}(1+M\sin(2\pi(k-1)K_n+\theta_{on_k})) \quad \text{(A.27)}$$

where $K_m=\frac{1}{M_f}$ and $K_n=\frac{1}{N}$.

Using (4.8) and rearranging, the above equation can be rewritten as:

$$\theta_{on_k}+\frac{k_r}{K_m}(\cos(2\pi(k-1)K_m)-\cos(2\pi(k-1)K_m+K_m\theta_{on_k})= \pi(1+M\sin(2\pi(k-1)K_n+K_n\theta_{on_k}) \quad \text{(A.28)}$$

The above equation is transcendental is nature and a computer program in FORTRAN using a numerical routine is used to solve for the on time angle in the k^{th} interval. The Fourier coefficients are then determined using the following equation:

$$C(n,k)=\frac{1}{-j2\pi n}(e^{-jnK_m\theta_{on_k}}-1) \quad \text{(A.29)}$$

The switching function for phase A, $f_a(t)$ can then be expressed as:

$$f_a(t)=\frac{1}{2\pi M_f}\sum_{k=1}^{k=M_f}\theta_{on_k}+\sum_{\substack{n=-\infty\\ n\neq 0}}^{n=+\infty}\left(\sum_{k=1}^{k=M_f}C(n,k)e^{-j2\pi nK_m(k-1)}\right)e^{jn\omega_r t} \quad \text{(A.30)}$$

Switching function for phase B($f_b(t)$) and phase C($f_c(t)$) can be obtained by phase shifting the reference voltage in (A.23) . The line switching function $f_{ab}(t)$ is then obtained as:

$$f_{ab}(t) = f_a(t) - f_b(t) \tag{A.31}$$

The output line voltage is computed as

$$V_{ab} = (V_{dc} + k_r V_{dc} \sin(\omega_r t)) \cdot f_{ab}(t) \tag{A.32}$$

The harmonic spectra of the switching function determined mathematically and from computer simulation are shown in Fig. A.13 and found to be a very good match. This validates the analysis performed.

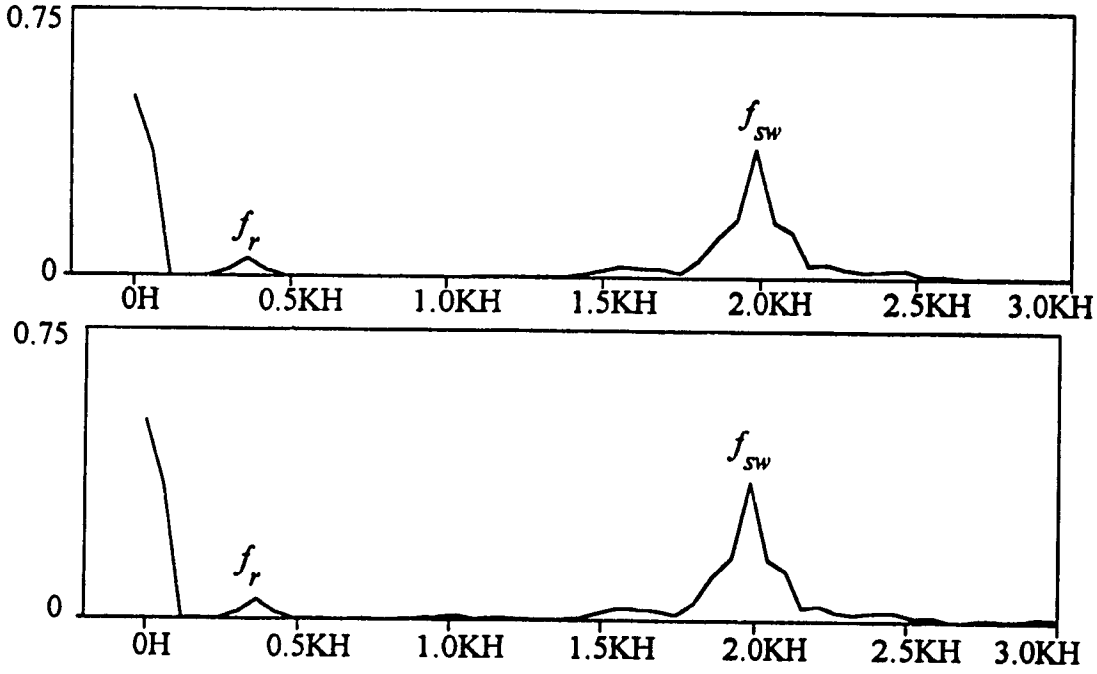


Fig. A.13. Switching function for phase A, $f_a(t)$. (a) Mathematically computed. (b) Computer simulation (f_{sw}=33pu, M=0.7)

A.5. Listing of FORTRAN programs used to compute the switching functions

A.5.1. Program to compute the switching function for a dc-dc converter working under reset integral control

```
C     LINE SWITCHING FUNCTION FOR A DC/DC CONVERTER WITH RIC
        DIMENSION BETA(100),THETA(1030),ASWCHF(2048)
      COMPLEX C(100,100),SWFP(100,100),SWCHF(1030)
      COMPLEX C1,J,SWCHFP,SWCHFN
      INTEGER RES
      REAL KM,KN,M
      OPEN(UNIT=23,FILE='FUNC.TXT')
      RES=256
      J=(0.0,1.0)
      VSH=10
      VS=100
      D=0.7
      NR=6
      NFSW=20
      FR=360
      FSW=NFSW*FR
      KM=1.0/REAL(NFSW)
      PI=3.14159
      WR=2*PI*FR
      SWCHF(1)=0
      WRITE(*,105)
105   FORMAT(1X,'THIS PROGRAM COMPUTES THE SWITCHING FUNCTION')
      WRITE(*,106)
106   FORMAT(1X'FOR A DC-DC CONVERTER')
      WRITE(*,108) NFSW,M
108   FORMAT(1X,'THE SWITCHING FREQUEMCY IS',I4,'MOD.INDEX=',F3.2)
      WRITE(*,107)
107   FORMAT(1X,'CALCULATING!! PLEASE DO NOT INTERRUPT')
      DO 500 ILOOP=0,RES-1
      THETA(ILOOP)=REAL(ILOOP)*2*PI/REAL((RES-1))
      DO 10 I=1,NFSW
      RD=PI/180
      P0=0
      P1=2*PI
      Q01=P0
      Q02=(VSH/(VS*KM))*(COS(2*PI*(I-1)*KM)-COS(2*PI*(I-1)*KM+KM*P0))
      Q03=-PI*2*D
      Q0=Q01+Q02+Q03
```

```
30   Q11=P1
     Q12=(VSH/(VS*KM))*(COS(2*PI*(I-1)*KM)-COS(2*PI*(I-1)*KM+KM*P1))
     Q13=-PI*2*D
     Q1=Q11+Q12+Q13
102  FORMAT(1X,F7.4,F7.4)
     PP=P1-Q1*(P1-P0)/(Q1-Q0)
     DELTA=(PP-P1)
     IF (ABS(DELTA) .GT. 0.0001) GOTO 40
     GOTO 50
40   P0=P1
     Q0=Q1
     P1=PP
     GOTO 30
50   BETA(I)=PP
10   CONTINUE
     SWFDC=0
     DO 15 K=1,NFSW
     SWFDC=SWFDC+1/(2*PI*NFSW)*BETA(K)
15   CONTINUE
     SWCHFP=0
     DO 200 N=1,100
     C1=0.0
     DO 300 K=1,NFSW
     C(N,K)=1.0/(-J*2*PI*REAL(N))*(EXP(-J*REAL(N)*KM*BETA(K))-1)
     SWFP(N,K)=C(N,K)*EXP(-J*2*PI*N*KM*(K-1))*EXP(J*N*THETA(ILOOP))
     C1=C1+SWFP(N,K)
300  CONTINUE
     SWCHFP=SWCHFP+C1
     SWCHFN=CONJG(SWCHFP)
200  CONTINUE
     SWCHF(ILOOP)=SWFDC+SWCHFP+SWCHFN
     ASWCHF(ILOOP)=REAL(SWCHF(ILOOP))
     ASWCHF(ILOOP+(RES-1))=ASWCHF(ILOOP)
     WRITE(*,201) ILOOP
500  CONTINUE
     DO 600 ILOOP=0,2*RES-1
     TIME=REAL((ILOOP))*2*PI/(WR*REAL((RES-1)))
     VDC=VS+VSH*SIN(WR*TIME)
     WRITE(23,103)TIME,ASWCHF(ILOOP),VDC
103  FORMAT(E15.6,1X,E15.6,1X,E15.6)
201  FORMAT(1X,I4)
600  CONTINUE
     STOP
     END
```

A.5.2. Program to compute the switching function for a dc-dc converter working under modulated integral control

```
C    SWITCHING FUNCTION FOR A DC/DC CONVERTER WITH MIC
     DIMENSION BETAR(100),BETAF(100),VMR(100),VMF(100)
     DIMENSION THETA(1030),ASWCHF(2048)
     COMPLEX C(100,100),SWFP(100,100),SWCHF(1030)
     COMPLEX C1,J,SWCHFP,SWCHFN
     INTEGER RES
     REAL KM,KT
     OPEN(UNIT=23,FILE='MFUNC.TXT')
     RES=256
     J=(0.0,1.0)
     VSH=0.1
     VDC=0.7
     NR=6
     NFSW=5
     FR=360
     FSW=NFSW*FR
     KM=1.0/REAL(NFSW)
     KT=0.4
     PI=3.1415927
     WR=2*PI*FR
     WRITE(*,105)
105   FORMAT(1X,'THIS PROGRAM COMPUTES THE SWITCHING FUNCTION')
     WRITE(*,106)
106   FORMAT(1X 'FOR A DC-DC CONVERTER WITH MODULATED INTEGRAL
CONTROL')
     WRITE(*,108) NFSW,VDC
108   FORMAT(1X,'THE SWITCHING FREQUEMCY IS',I4,'DUTY CYCLE=',F6.4)
     WRITE(*,107)
107   FORMAT(1X,'CALCULATING!! PLEASE DO NOT INTERRUPT')
     DO 500 ILOOP=0,RES-1
     THETA(ILOOP)=REAL(ILOOP)*2*PI/REAL((RES-1))
     BETAR(1)=PI/2
1     DO 10 I=1,NFSW
     VMR(I)=BETAR(I)/PI
102   FORMAT(1X,I3,3F9.4)
     RD=PI/180
     P0=PI
     P1=2*PI
     VAL=KM*(1.-VDC+2.*KT)
     Q01=P0
```

```
      Q02=-(2.*PI*KM*KT*(2.-VMR(I))+BETAR(I)*KM*(1.-VDC))/VAL
      Q03=-VSH*(COS(KM*P0)-COS(KM*BETAR(I)))
      Q0=Q01+Q02+Q03
30    Q11=P1
      Q13=-VSH*(COS(KM*P1)-COS(KM*BETAR(I)))
      Q1=Q11+Q02+Q13
      PP=P1-Q1*(P1-P0)/(Q1-Q0)
      DELTA=(PP-P1)
      IF (ABS(DELTA) .GT. 0.0001) GOTO 40
      GOTO 50
40    P0=P1
      Q0=Q1
      P1=PP
      GOTO 30
50    BETAF(I)=PP
      VMF(I)=2-BETAF(I)/PI
      BETAR(I+1)=(2*PI*KT*VMF(I)-VDC*(2*PI-BETAF(I)))/(2*KT+VDC)
2000  FORMAT(1X,I4,':',2F10.5)
10    CONTINUE
      DELTA=BETAR(I)-BETAR(1)
32    FORMAT(1X,I5,F8.5)
      IF (ABS((BETAR(I)-BETAR(1))).LE. 0.001) GOTO 3
      BETAR(1)=(BETAR(I)+BETAR(1))/2.0
      GOTO 1
202   FORMAT(1X,I4,2F9.4)
      STOP
3     SWFDC=0
      DO 15 K=1,NFSW
      SWFDC=SWFDC+1/(2*PI*NFSW)*(BETAF(K)-BETAR(K))
15    CONTINUE
      SWCHFP=0
      DO 200 N=1,100
      C1=0.0
      DO 300 K=1,NFSW
      C(N,K)=1.0/(-J*2*PI*REAL(N))*(EXP(-J*REAL(N)*KM*BETAF(K))
     R-EXP(-J*REAL(N)*KM*BETAR(K)))
      SWFP(N,K)=C(N,K)*EXP(-J*2*PI*N*KM*(K-1))*EXP(J*N*THETA(ILOOP))
      C1=C1+SWFP(N,K)
300   CONTINUE
      SWCHFP=SWCHFP+C1
      SWCHFN=CONJG(SWCHFP)
200   CONTINUE
      SWCHF(ILOOP)=SWFDC+SWCHFP+SWCHFN
      ASWCHF(ILOOP)=REAL(SWCHF(ILOOP))
      ASWCHF(ILOOP+(RES-1))=ASWCHF(ILOOP)
```

```
      WRITE(*,201) ILOOP
500   CONTINUE
      DO 600 ILOOP=0,2*RES-1
      TIME=REAL((ILOOP))*2*PI/(WR*REAL((RES-1)))
      VO=100+100*VSH*SIN(WR*TIME)
      WRITE(23,103)TIME,ASWCHF(ILOOP),VO
103   FORMAT(E15.6,1X,E15.6,1X,E15.6)
201   FORMAT(1X,I4)
600   CONTINUE
      STOP
      END
```

A.5.3. Program to compute the switching function for a dc-ac converter working under reset integral control

```
C     OUTPUT VOLTAGE OF A VOLTAGE SOURCE INVERTER WORKING
C       UNDER RIC
      DIMENSION BETA(100),THETA(1030),ASWCHF(1030)
      DIMENSION BSWCHF(1030),SWLL(1030)
      DIMENSION VDC(1030),VO(1030)
      COMPLEX C(100,100),SWFP(100,100),SWCHF(1030)
      COMPLEX C1,J,SWCHFP,SWCHFN
      INTEGER RES
      REAL KM,KN,M
      OPEN(UNIT=23,FILE='SWITCH',STATUS='OLD')
C     RESOLUTION OF THE PROGRAM
      RES=256
      J=(0.0,1.0)
      PI=3.14159
      VSH=10
      VS=100
      NR=6
      NFSW=33
      FO=60
      FR=NR*FO
      WR=2*PI*FR
      FSW=NFSW*FO
      KM=FR/FSW
      KN=FO/FSW
      M=0.7
      M120=RES/3
```

```
      M240=2*RES/3
      WRITE(*,105)
105   FORMAT(1X,'THIS PROGRAM COMPUTES THE OUTPUT VOLTAGE')
      WRITE(*,106)
106   FORMAT(1X'OF A THREE PHASE INVERTER')
      WRITE(*,108) NFSW,M
108   FORMAT(1X,'THE SWITCHING FREQUEMCY IS',I4,'MOD.INDEX=',F3.2)
      WRITE(*,107)
107   FORMAT(1X,'CALCULATING!! PLEASE DO NOT INTERRUPT')
      DO 500 ILOOP=0,RES-1
      THETA(ILOOP)=REAL(ILOOP)*2*PI/REAL((RES-1))
      DO 10 I=1,NFSW
      RD=PI/180
      P0=0
      P1=2*PI
      Q01=P0
      Q02=(VSH/(VS*KM))*(COS(2*PI*(I-1)*KM)-COS(2*PI*(I-1)*KM+KM*P0))
      Q03=-PI*(1+M*SIN(2*PI*(I-1)*KN+KN*P0))
      Q0=Q01+Q02+Q03
30    Q11=P1
      Q12=(VSH/(VS*KM))*(COS(2*PI*(I-1)*KM)-COS(2*PI*(I-1)*KM+KM*P1))
      Q13=-PI*(1+M*SIN(2*PI*(I-1)*KN+KN*P1))
      Q1=Q11+Q12+Q13
102   FORMAT(1X,F7.4,F7.4)
      PP=P1-Q1*(P1-P0)/(Q1-Q0)
      DELTA=(PP-P1)
      IF (ABS(DELTA) .GT. 0.0001) GOTO 40
      GOTO 50
40    P0=P1
      Q0=Q1
      P1=PP
      GOTO 30
50    BETA(I)=PP
10    CONTINUE
      SWFDC=0
      DO 15 K=1,NFSW
      SWFDC=SWFDC+1/(2*PI*NFSW)*BETA(K)
15    CONTINUE
      SWCHFP=0
      DO 200 N=1,100
      C1=0.0
      DO 300 K=1,NFSW
      C(N,K)=1.0/(-J*2*PI*REAL(N))*(EXP(-J*REAL(N)*KN*BETA(K))-1)
      SWFP(N,K)=C(N,K)*EXP(-J*2*PI*N*KN*(K-1))*EXP(J*N*THETA(ILOOP))
      C1=C1+SWFP(N,K)
```

```
300   CONTINUE
      SWCHFP=SWCHFP+C1
      SWCHFN=CONJG(SWCHFP)
200   CONTINUE
      SWCHF(ILOOP)=SWFDC+SWCHFP+SWCHFN
      ASWCHF(ILOOP)=REAL(SWCHF(ILOOP))
      WRITE(*,201) ILOOP
201   FORMAT(I5)
500   CONTINUE
      DO 600 I=0,RES-1
      LK=MOD(I+M120,RES-1)
      BSWCHF(I)=ASWCHF(LK)
600   CONTINUE
      DO 700 I=0,RES-1
      SWLL(I)=ASWCHF(I)-BSWCHF(I)
C     GENERATING THE INPUT DC BUS VOLTAGE
     TIME=REAL(I)/(60*REAL((RES-1)))
      VDC(I)=VS+VSH*SIN(WR*TIME)
C     OUTPUT VOLTAGE
      VO(I)=VDC(I)*SWLL(I)
      WRITE(23,103)TIME,VDC(I),VO(I)
103   FORMAT(E15.6,E15.6,E15.6)
700   CONTINUE
     STOP
      END
```