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Packet Execution: A New Concept in Multiprogramming

Angel Diez

A Technical Report

in

The Department

of

Computer Science

**Presented in Partial Fulfillment of the Requirements
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Montréal, Québec, Canada**

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ABSTRACT

Packet Execution: A New Concept in Multiprogramming

Angel Diez

This paper presents a new approach to achieve an improvement of the cost/performance ratio of a multiprogramming workload running on a single-CPU, via a multi-micro-processor system. The proposed approach is based on the partitioning of programs into blocks called packets. These packets travel in a multiprocessor network structure seeking the first idle micro-processor, where the code performs the required function (execution, I/O, storage, etc). Should the peak workload increase, the multiprocessor machine can easily be upgraded by adding processors in a modular fashion.

PREFACE

The completion of this report is due to three main and only factors. First, to the generation of a concept, brought to paper-life by stubbornness, belief and a reasonably broad experience with packet-switching processors used in data communications. Second, to the constant support of Dr. Bipin Desai. Without his positive influence, the concept of Packet Execution would probably have remained buried within the boundaries of my skull. Third, to the perseverance and support of my wife Linda, whose smile was the best medicine against the common frustrations encountered during the project.

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1.0 BACKGROUND.

The idea of distributing the power of a large CPU into a multitude of smaller processors that perform individual tasks, while offering a better performance as a whole, is not new. P. H. Enslow (ENS-1) identifies 63 multiprocessors of different kind commercially available. The multitude of smaller, experimental systems is much greater. Several well documented papers give an insight into the different aspects of multiprocessing. (FULL-1), (JEN-1), (DAV-1).

When distributing a computer system, several questions arise. How should the tasks executed in the uniprocessor be decomposed to run on a set of smaller processors?. Should the processors be loosely coupled or tightly coupled ?. What is the most efficient connection between processors: Bus, ring, crossbar ?. How can the synchronization of processes and overhead be controlled?. These and a multitude of other different questions have been addressed in the literature. Myers (MYE-1) among others stresses the need for matching the hardware structure with the software that is to be executed in it. S. I. Kartashev (KAR-1 &-2), for instance, addresses this problem by designing a dynamically variable multiprocessor system.

L. Svobodova (SVO-1) supplies logical reasons for a well organized set of requirements in a distributed system.

Simulation studies and theory of message passing systems can be found in (MON-1), (HAL-1), (BRY-1) and (JEN-2).

The type of network used to connect the processors has a strong influence

on the throughput capability of the multiprocessor system. General studies of network organizations are found in (ENS-1), (BAS-1 &-2), (BER-1), (DAV-1).

Following Švobodova (SVO-1) and Halstead (HAL-1) we have concentrated in this project on fully distributed systems where there is no centralized control. Group of processors having the same authority, decide, by message interchange, on issues that affect a different group of processors. One way of connecting processors in the same group is by a loop or ring. The advantage of this type of connection is that loop protocols are easy to implement and expand. Loop networks are analyzed in (JAF-1), (LIU-1), (PIER-1), (NEW-1).

In a fully distributed multiprocessor the operating system loses its identity as the control of resources is done by communications protocols rather than by central decision making. Most operating systems up to date have been built around a kernel and higher level processes that see the hardware in a synchronous and transparent fashion.

Synchronization of processes is vital to avoid deadlock situations. Operating systems that specifically stress this issue are the THE (MCK-1) and the RC-4000 (HAN-1). In this paper we emphasize synchronization by message passing.

Hierarchical structures are analyzed in (GOO-1) and (PAR-1). Implementation of distributed operating systems as a set of processors has been analyzed in (JEN-1), (BUH-1), (MYE-1), (PRO-1), (BRO-1) and (WUL-1). Most of the systems analyzed in these papers show a certain centralization of functions. We emphasize maximum decentralization in a fully distributed

BACKGROUND.

system.

Systems that have substantially influenced our thinking are the STAR-OS and MEDUSA operating systems, both running on the Cm* multiprocessor, (JON-1), (JON-2), (SWA-1), as well as the SYMBOL machine and operating system. (RIC-1). All these papers discuss the limitations encountered when trying to distribute functions in a multiprocessor. We feel that these constraints can be minimized with the concept of Packet Execution.

2.0 PACKET EXECUTION: BASIC CONCEPTS

In a typical data processing shop the main CPU is shared by programmers and users to test, edit and compile programs as well as to run production applications. At one point in time, many different programs are being scheduled and run by the centralized operating system and CPU. Bottlenecks occur during peak periods and the typical answer to heavy CPU loading is to acquire either another tightly-coupled CPU or a faster CPU. In both cases, the cost of upgrading is fairly high.

We could reduce the CPU load by providing each programmer with a stand-alone microcomputer so that the editing, compiling and testing of individual programs could be done on these units. Unfortunately, this approach is rarely cost-effective because testing of programs usually requires access to large, centralized code modules and data files. The amount of main memory and disk space associated with the individual microcomputers would, most likely, be prohibitive.

We could also reduce the CPU load by executing programs or portions of programs on a multitude of small processors. To achieve this task in an effective manner, the processors should operate asynchronously. This means that no dependencies should exist between the different execution units. More important, the programs have to be decomposed in blocks that are self-addressable. (We will call these blocks packets from now on.) In other words, the programs or parts thereof should be accessible to any processor in the machine regardless of their position in main memory or disk. In this way, centralized files and data bases are accessible to all the users, while the task of executing programs is uniformly shared by the dif-

ferent execution units.

These execution processors only require a fraction of the speed and operating system overhead of the centralized CPU. Naturally, the overhead associated with routing the individual packets to the different processors, increases. We feel, however, that this communications overhead can be minimized with an adequate design.

To illustrate our approach, let us consider programs and data files structured in the following way: (see Fig. 1)

The object code of program A is decomposed in blocks called Instruction Packets (IP). Each IP references variables, subroutines and data files whose descriptors are contained in Environment Packets (EP). Data files are also decomposed in Data Packets (DP). To run program A we start by loading the first IP and EP of the program as well as the data packets referenced in the EP. These are IP1A, EP1A, DP1 and DP2. This set of packets can run on a stand-alone execution processor and form a group called Packet Group.

To speed-up execution, we also want to load in memory all the packets that are most likely to be dispatched next. These are referenced in the EP1A packet: IP2A, EP2A, IP3A, EP3A, DP3 and DP4. This set of packets, together with IP1A, EP1A, DP1 and DP2, form the Packet Group Set of EP1A.

The abstract machine that can run programs decomposed in this fashion is illustrated in Fig. 2. We call it PACOS (Packetized Computing System). Processors are interconnected by a ring network. Vertical rings will be called Slices. Horizontal rings will be called Loops. When we refer to the function that each Loop performs, we will be talking about Levels. There are

four Levels in PACOS, each Level consisting of several peer processors.

1. The User Manager Level (UM Level), monitors (and controls on exceptions) the execution flow of each program. It consists of several User Manager Switches (UMS) and Processors (UMP).
2. I/O is controlled by the Device Manager Level. (DM Level) It consists of Device Manager Switches and Processors. (DMS-DMP)
3. The Memory Manager Level (MM Level), consists of several peer memory units, each one controlled by a Memory Manager Processor (MMP) and a Memory Manager Switch (MMS). Each Memory Manager can hold several self-addressable packets that may belong to different programs.
4. The execution unit consists of several peer Execution Manager Processors, each one executing a Packet Group at a time. A local memory holds the Packet Group under execution. Each EMP interfaces with PACOS via an EMS (switch).

The general processing flow of packets within PACOS is explained below, taking as an example the program A of Fig. 1. To simplify the description, a single Slice will be considered. (see Fig. 3). EP and DP packets are routed to the desired destination by means of Control Packets (CP). The switches. (UMS, DMS, MMS and EMS) scan the header of the arriving Control Packets and route them accordingly. Control Packet commands are explained in Section 5.3.

Initially, a user requests to run program A from a terminal attached to the DMP.

- 1.- The DMP translates this request into a CREATE(A) control packet that is sent to the UM Level.
- 2.- The UMP accepts the packet and sends a GET(EP1A, from UM to MM) control packet requesting EP1A from memory.
- 3.- As the EP1A packet does not exist in memory, the MMP retrieves it from disk by sending the stream: GET(PKT.GRP.SET of EP1A, from MM to DM)
- 4.- The DMP accepts the packet, retrieves the Packet Group Set of EP1A and generates the packet: STORE(PKT.GRP.SET of EP1A, to MM).
- 5.- The MMP stores all packets of the PKT.GRP.SET and sends the stream: SEND(EP1A,GLB.DP, to UM). GLB.DP is a DP packet holding all the global variables of program A. (See Section 6, p.42). This Global DP packet is only required once at creation of the program object.
- 6.- When the UMP receives EP1A plus the Data Packet that contains all the Global variables, it generates a request to commence the execution of the first Packet Group, by sending an imbedded SEND control packet: SEND(SEND(PKT.GRP.1A, to EM) to MM).
- 7.- The MMP accepts the packet and generates SEND(PKT.GRP.1A, to EM):
- 8.- The EMP accepts the Packet Group and executes it. Once execution is finished, the EMP generates the block: UPDATE(EP1A, to UM)
- 9.- The UMP accepts the block and updates the EP packet (which provides information about the current status of the program) as well as any global

variables that might have been affected, before sending the stream: UPDATE(EP,DP,PKTS, to MM) + SEND(SEND(PKT.GRP.2A, to EM) to MM) + GET(PKT.GRP.SET of EP2A, to MM).

10.-The MMP accepts the block, updates all EP, DP packets affected and sends the stream: SEND(PKT.GRP.2A, to EM). The second Packet Group is sent to the EM.Level for execution. If PKT.GRP.SET of EP2A does not exist in memory, the MMP retrieves it from disk by sending: GET(PKT.GRP.SET of EP2A, to DM).

11.-The EMP accepts PKT.GRP.2A and executes it.

12.-The DMP retrieves PKT.GRP.SET of EP2A, requested by the MMP in step 10, and Sends: STORE(PKT.GRP.SET of EP2A, to MM).

13.-When the PKT.GRP.2A has finished executing, the EMP sends: UPDATE(EP2A, to UM).

At this time the cycle repeats, going back to step 9, until the end of execution of program A is reached.

The packet flow has been described for a single Slice and a single program. Naturally, multiple slices will speed-up the execution of several jobs or tasks running in a multiprogramming environment. The transfer of packets is done via parallel buses, at very high speed. We figure that the overall performance of the machine will be quite high, as long as the delay caused by transferring packets remains a fraction of the time spent in processing chores such as: a) Execution of a Packet Group in the EMP. b) Storing/retrieving packets in the DMP. c) Storing/retrieving packets in

the MMP. A simulation of the packet flow will be quite useful in assessing the consistency of our thinking.

The proposed scheme offers several advantages:

1. Reliability: If any unit fails, the rest of the system continues working normally.
2. Modularity: As all units in one group (or level) are similar in construction, expansion and replacement of equipment is straight forward.
3. Cost: It is less costly to produce 1000 units of a VLSI circuit board than 10 larger systems of 100 circuit boards each.

The disadvantages of this structure are:

1. The partitioning of a large program into several packets that run on different processors in an efficient manner, is still a challenging area of research.
2. A great deal of care has to be placed in the design of the communications links and routing algorithms, in order to avoid a degradation in performance due to transmission delays.

Fig. 1.- THE PACKET GROUP

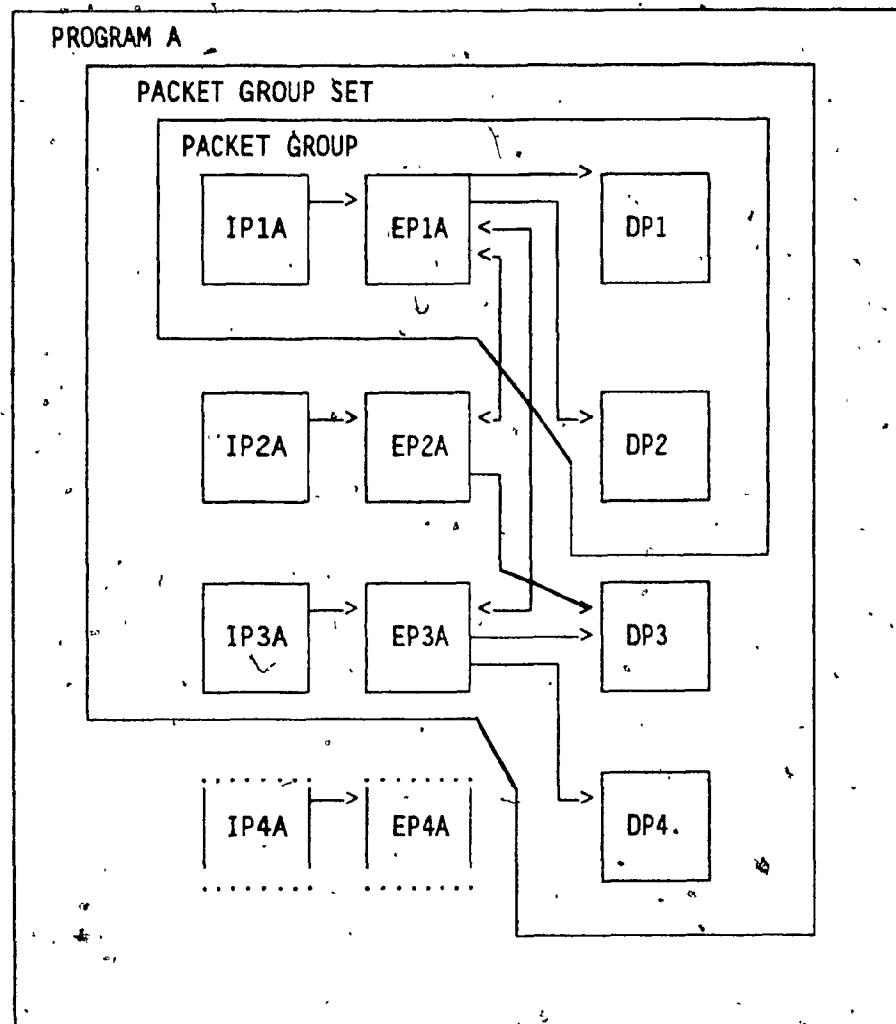


Fig. 2:- PACOS ARCHITECTURE

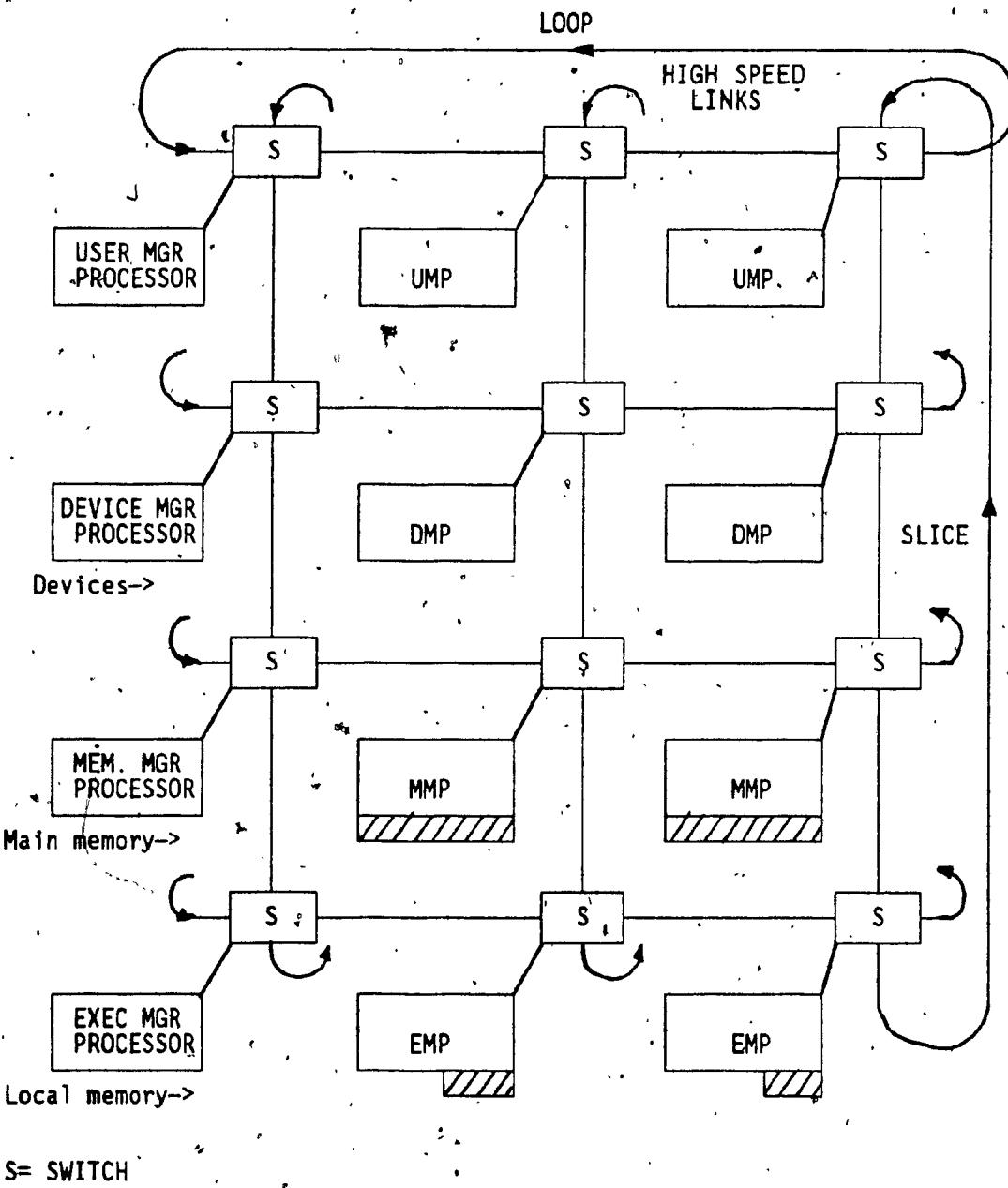
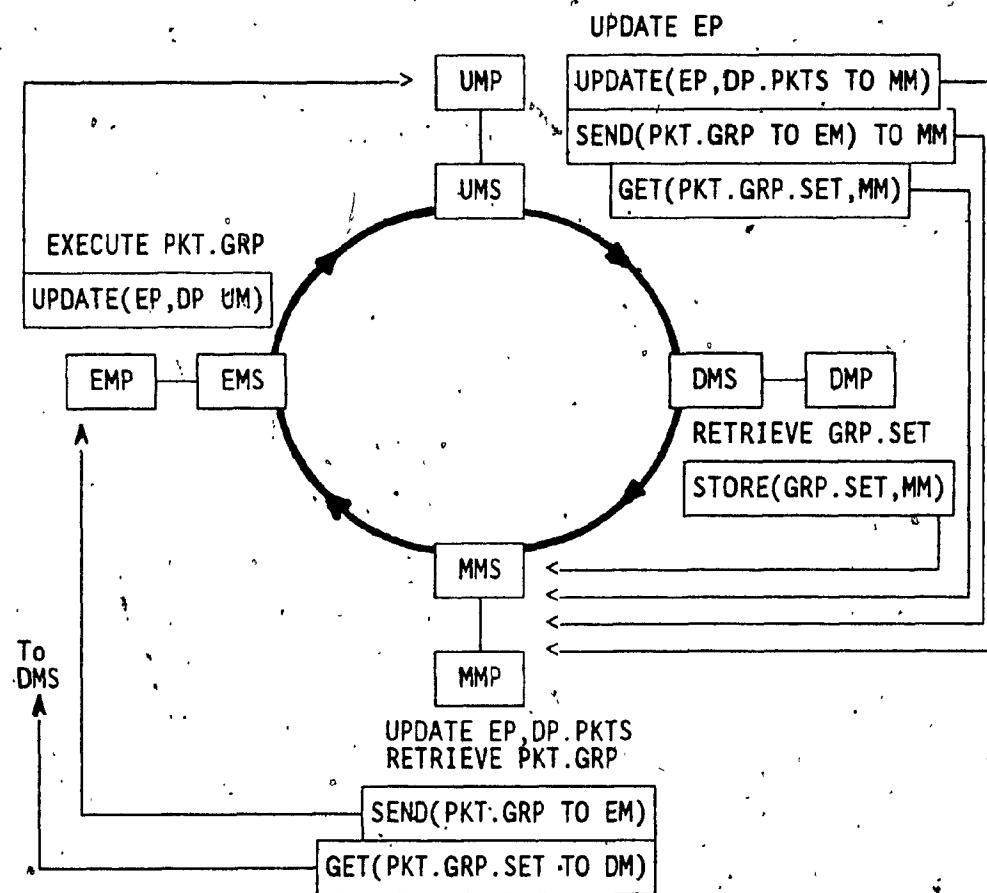


Fig. 3.- PACKET EXECUTION (ONE SLICE)



3.0 THE PACKET GROUP

A **Packet Group** is defined as the group of packets that execute in a single Execution Manager Processor. It consists of:

- One Instruction Packet (IP) that holds the object code.
- One Environment Packet (EP) that holds the variables, labels and data referenced in the code.
- One or more packets Data Packets (DP) that hold data.

Packets flow through the distributed machine by means of switches and commands inserted in Control Packets (CP).

Packets have a unique identifier that consists of the packet type, the object number and the packet number. For example, to uniquely identify the EP packet (code 01), number 15 of object number (00...01111101100000110) , we simply have to refer to the following packet ID:

0	2	32	48	63
01	00...	..01111101100000110	00..	01111

EP OBJECT NO. 30 bits PKT NO. 16 bits

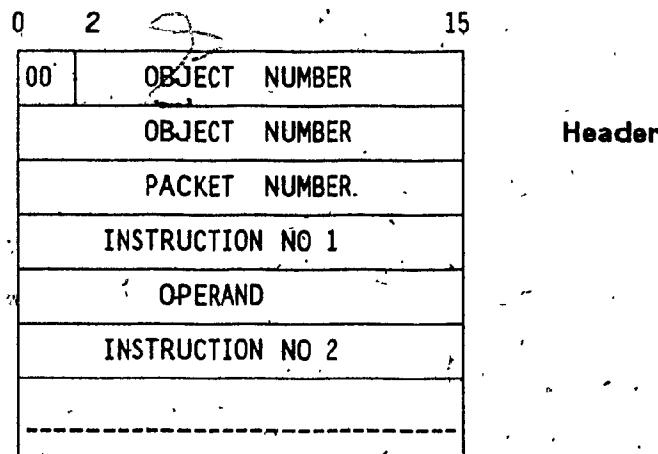
To illustrate the operation of PACOS, a specific machine organization will be analyzed.

We consider a machine that has the following addressing capabilities: Object address : 30 bits. (This gives one billion unique objects). Packet address: 16 bits. (This gives 64 kpackets/ object). IP memory size: 16 bits. (This gives a maximum of 64 kwords/packet). EP memory word size: 64 bits. Data memory word size: 64 bits. (six tag bits plus 58 value bits).

3.1 INSTRUCTION PACKET.

This type of packet is identified by the code 00. The packet has a header consisting of the packet type (00), the object number (30 bits) and the packet number (16 bits). The object code follows the packet header. Operation code occupies one word (16 bits) and operands occupy also one word (16 bits). As the machine is stack oriented, a maximum of one operand per instruction is necessary. The structure of the IP packet is shown in Fig 4.

Fig. 4.- Instruction Packet



3.2 ENVIRONMENT PACKET

This packet is identified by the code 01 and contains all references associated with the respective IP. Fig. 5 shows the structure of the EP. Every IP has a corresponding EP that holds all the variables referenced in the IP. One EP, however, can be associated with several DP's (Data Packets), depending on the data being referenced. The EP packet has a packet header that contains the type code (01), the object number (owner of the packet), the packet number and the starting address. The starting address is to be given to the EMP (execution manager) so that the related IP can start executing on the right local address.

Following the header, all references are inserted in the packet. Each reference is defined with two-64 bits words. The first word contains the name of the identifier (in a standard code such as ASCII). This information is important to notify the user dynamically of any errors during execution. The second word contains the Identifier Control Word.(ICW). The ICW contains all necessary information to locate the value of the identifier being addressed. Table 1 shows the structure of the ICW.

Fig 5.- Environment Packet

0	2	32	48	63
01	OBJECT NUMBER	PKT NUMBER	START ADDRESS	
	IDENTIFIER	NAME		
	IDENTIFIER CONTROL WORD* (ICW)			
	IDENTIFIER	NAME		
	IDENTIFIER CONTROL WORD (ICW)			

ICW

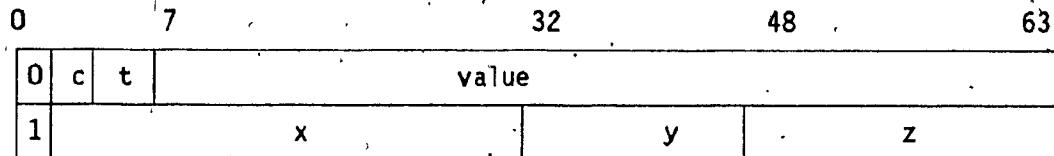


TABLE 1.- CONTENTS OF ICW

FIELD	BITS	VALUE	DESCRIPTION
h (home)	0	0	Value of identifier is contained in the ICW (bits 7-63)
		1	ICW contains descriptor to the identifier (bits 1-63)
c (class)	1-3	000 001 010 011 100 101 110	Global variable Local variable Array pointer Label Procedure Parameter Program segment
t (type)	4-6	000 001 010 011 100 101	Bit Boolean Character Fixed Float Subscript
x	1-31		Identifies the object number of the reference.
y	32-47		Identifies the Packet number of the referenced word.
z	48-63		Identifies the address of the referenced word inside the packet.

If the reference is local (bit 0=0) the value is contained in bits 7-63.

3.3 CONTROL PACKET

This type of packet is identified by the code 10 and contains commands, responses and notifications addressed to other processors. The header contains the type code (10), the control command, the object number of the originating process and the packet number originating the command. The destination level number, destination object number (30 bits) and the destination packet number (16 bits) complete the control packet. The originating object number of the control packet may differ from the originating object number of the packet in transit.

CP packets are attached to the header of IP, EP, and DP packets, to route them properly. Fig 6 shows a sample Control Packet.

Fig 6.- Control Packet

0	2	15
1	0	COMMAND
d		OBJECT NUMBER (dest)
		OBJECT NUMBER (dest)
		PACKET NUMBER (dest)
o		OBJECT NUMBER (origin)
		OBJECT NUMBER (origin)
		PACKET NO. (origin)
		PACKET IN TRANSIT

The destination field is described in Table 2.

TABLE 2.- Destination Level Number (Origin)

FIELD	BITS	VALUE	DESTINATION (ORIGIN)
d (o)	0-1	00	User Manager
		01	Device Manager
		10	Memory Manager
		11	Execution Manager

The different types of commands are explained below:

- GET.-Retrieves a certain packet from the destination layer, on behalf of the originating object.
- UPDATE.-Updates the original EP or DP packet according to the information attached to the CP packet.
- STORE.-Stores the EP, IP or DP attached to the control packet in any available MMP or device if the destination is a DMP.
- CREATE.-Creates a new object in the UM layer.
- CLEAR.-Clears the originating packet number from the MMP holder of the packet.
- SEND.-Transfers one or several packets, to the destination layer. This packet may contain imbedded control packets.

3.4 DATA PACKET (DP)

The packet header contains the type code (11), the object number (bits 2-31) and the packet number (bits 32-47). Data items (64 bits), follow the header. Each data item is qualified with a 6-bit Tag field as per Table 3. These tags are used when the data item is indirectly addressed by a descriptor in the ICW. The structure of the Data Packet is shown in Fig 7.

Fig 7. - Data Packet

0	2	32	48	63
11	OBJECT NUMBER	PKT NUMBER	not used	
c	t	DATA	ITEM	
c	t	DATA	ITEM	
c	t	DATA	ITEM	

Table 3.- Data Tags

TAG FIELD	BITS	VALUE	DESCRIPTION
c (class)	0-2	000	Global variable
		001	Local variable
		010	Array pointer
		011	Label
		100	Procedure
		101	Parameter
		110	Program segment
t (type)	3-5	000	Bit
		001	Boolean
		010	Character
		011	Fixed
		100	Float
		101	Subscript

4.0 PACOS ARCHITECTURE.

An abstract architecture of the PACOS machine that will execute a program submitted in packetized form is illustrated in Fig. 2.

The packet switching network is composed of switching processors connected by two half-duplex rings. Processors at the same level have similar characteristics and form a LOOP. Processors located on the same vertical ring form a SLICE. (In theory, we can build a PACOS computer with a single Slice, although it would be very inefficient).

Packets originally reside in mass-storage devices (At the DM Level). Upon request, packets are transferred to the Memory Manager Level where they remain until cleared by CLEAR commands. Execution of a Packet Group is performed asynchronously. The packets of the group are transferred to the Execution Manager Level (EML). The EP packet will actively seek an idle EMP by checking each EMS (switch) in the EML Loop. Once an EMP is found idle, the Packet Group will grab it and will execute in it. After execution this EMP becomes idle again. If one processor fails, automatic reconfiguration occurs and the machine continues processing normally.

The overall PACOS network resembles a toroid where information flows always in the same direction. The transmission of packets from node to node is done by 16 and 64-bit parallel buses, that accomodate the width of the different packet types. Buffers are used to hold the packets before they are released and after they are received by a switch. An additional signal in the inter-nodal bus serves as control line to indicate FREE or FULL BUFFER conditions.

4.1 THE USER MANAGER LEVEL.

The User Manager Level consists of several User Managers that are peer to each other both physically and logically. Each User Manager Processor (UMP) interfaces with the rest of the machine via a User Manager Switch (UMS). This switch is a routing unit that maintains routing algorithms for incoming and outgoing packets according to the status information supplied to or from the UMP illustrated in Fig 8. The basic interface is defined as follows:

1. OK.- This signal is supplied by the User Manager Switch (UMS) after having received approval from the other UMP's regarding scheduling priority and table updates of the object just created. If the object just created is a program, the UMP will initiate its execution.
2. UPDATE.- This signal has an initial OFF status and is turned ON as soon as a request for updating the EP or tables arrives. The signal is turned OFF as soon as the receiving UM has updated the appropriate EP packet and tables.
3. UPBUS.- This interface transfers packets between the UMP and the switch.

A picture of the UMP-UMS interface is shown in Fig 8. The dynamic behaviour of the UMP is described in pseudo-code form in the next page.

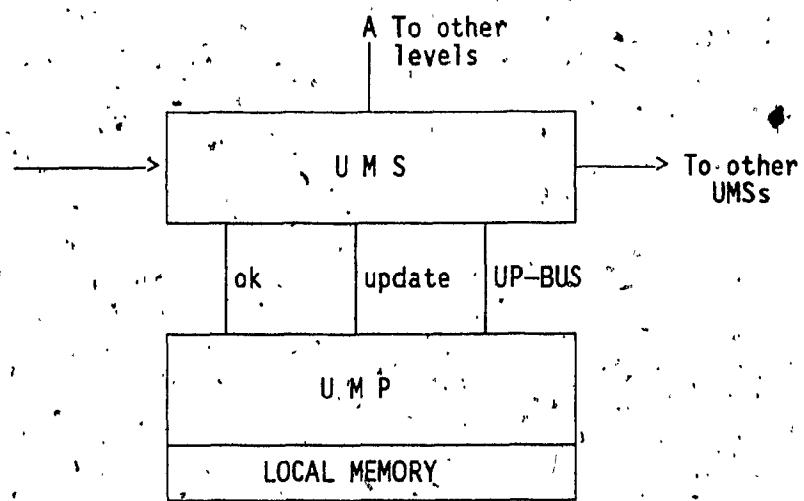
The UMS makes decisions based on the status of three tables: a) UMLTABLE maintains a record for all the existing objects in PACOS. b) UMPTABLE(n)

maintains a record for all the existing objects that have been created by the UMP number "n". c).UMSTABLE(n) maintains the routing tables for all incoming packets.

When an UPDATE command is received both UML and UMP table's are updated. When a packet arrives at the UMS its destination is checked and it is routed according to the UMSTABLE.

The operation of the UM is as follows: Initially, the UM is free to accept any objects for creation and dispatching (if object is a program to execute). As soon as a CREATE request is received, the UMS will decide whether the new object can be accepted by this UMP or not. If not accepted, the UMS will simply pass the CREATE request to the next UMS. If accepted, the UMS will send an UPDATE command to the other UMP's in order to update their UMP-UMLTABLES. The UPDATE command is returned to the UMP with the acceptance. At that time The UM switch sets the OK flag ON and the UMP requests execution of the first Packet Group by sending an imbedded SEND command to the Memory Manager, MM. The UMP also requests the next Packet Group Set from the DML with a GET command. This request is done in parallel with the execution of the current Packet Group. At program creation time, the DML will send to the UMP a special DP packet containing the Global variables of the program, GLB.DP. The UMP keeps on receiving EPs as Packet Groups get executed, and updating the EPs, DPs and global variables. When the last EP is received, the UMP sends an UPDATE command to the other UMs indicating that the just finished object will be removed from the UMP-UMLTABLES, if the other UMPs do not need this object. CLEAR commands are also sent to the MML to clear the memory space used by the terminated object.

Fig 8.— USER MANAGER



4.2 USER MANAGER DYNAMIC FLOW.-

USER MANAGER

Begin

Do forever

If CREATE= True then

 If object is accepted by UMS then

 Begin

 OK:= False

 SEND (UPDATE UML-UMPTABLES, next UMS)

 If OK= true then

 Begin

 GET(PKT.GRP.SET,MML) ** Get next pkt grp set from MM **

 SEND(SEND(PKT GRP, EML) MML)

 End

 End.

 If UPDATE= True then

 Begin

 Update(table or EP,DP) ** Table is updated by the UMP **

 If origin of Update is this UMP

 then OK:= True else ** Acknowledging returned Update *

 SEND (UPDATE, next UMS) ** Update passed to other UMs*

 UPDATE:= False

 If End-of PGRM= True then ** Process finished **

 SEND(CLEAR, object, MML)

 End

 End

4.3 THE DEVICE MANAGER LEVEL.

The DM Level consists of a group of peer Device Managers each consisting of a processor and a switch. Each DMP can handle several devices. The DMP (Device Manager Processor) interfaces with the DMS via flags and buses. It also interfaces with the devices via a data bus. The basic structure of the DM is shown in Fig. 9. The basic interface signals are described below.

1. IO(P).- This flag is set ON by the switch as soon as a request to read or write a packet is received.
2. MORE(n).- This signal is to indicate that the Device "n" cannot accept I/O requests other than for the file currently being accessed. It puts the device into a WAIT state and the device will not be FREE until the MORE flag is set OFF.
3. DPBUS.- This bus transfers packets between the DMS and the DMP.

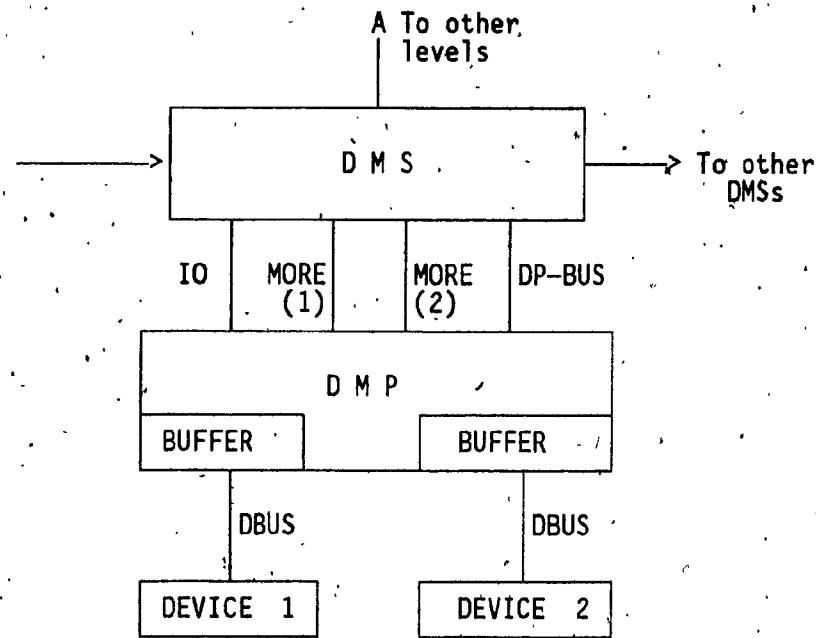
Devices are given a permanent, protected, object number at system generation time. Files are assigned an object number at creation time. Therefore writing (reading) to (from) devices, such as terminals, lines, printers, etc, or files is only a matter of mapping object number to physical location of the desired resource. This mapping is done by the DMLTABLE and the DMPTABLE, maintained by the DMS switches. The DMLTABLE maps object number, packet number, to DMP number. The DMPTABLE maps object number, packet number, to physical device and location within the device.

For instance, to print a block of data to a specific printer, the command

SEND(Dest= Printer object number) is sent with a Control Packet to the DML. The first DMS that receives the CP packet will scan its DMLTABLE and decide whether the printer device belongs to its DMP. If so, it will scan the DMPTABLE to identify the device; otherwise the DMS will pass along the CP packet to the next DMS.

Three basic states, FREE, WAIT and BUSY are assigned to each device. The device is considered FREE when it is ready to accept IO requests from ANY object. While in the BUSY state, the DM is transferring data to (from) the device. If the packet being read or written is part of a sequential transfer, that cannot be interrupted, (such as a print file), the MORE flag will be set and the device will switch from BUSY to WAIT state and viceversa until the IO request has been completed. At that time the device goes into the FREE state. If an IO request is received for a device that is in a BUSY or WAIT state, this request will either : a) Wait in the device queue until the device is available or b) Be passed to the next DMS. The dynamic flow of the DMP is explained below in pseudocode form.

Fig 9.- DEVICE MANAGER



4.4 DEVICE MANAGER DYNAMIC FLOW.

```

DEVICE MANAGER
Begin
Do forever
BUSY:= False
WAIT:= False
FREE:= True
Repeat
  If IO(P) = true then
    Begin
      WAIT:= False
      FREE:= False
      BUSY:= True
      DONE:= False
      DOIO          ** The IO, is being done **
      DONE:= True
      If MORE= true then ** Sequential transfer **
        Begin
          BUSY:= False
          WAIT:= true
        End
      End
    until MORE= False
  End.
End.

```

4.5 THE MEMORY MANAGER LEVEL.

The Memory Manager Level consists of several peer Memory Managers (MM) each one having a Memory switch and a processor (MMP). Each MMP has the responsibility of storing and retrieving packets of information stored in main memory. Each packet has self-addressing capabilities. Therefore, a file can be stored in different memories belonging to different MMs. Each MMP keeps status tables of the packets and files kept by all the MMs. The basic interface between the MMP and the MMS switch is shown in Fig. 10. While a common memory with interleaved MMP modules might have some advantages (particularly in the sharing of common data by different programs), a fully distributed memory approach was chosen. This was to take advantage of two important features of the PACOS architecture: easy expandibility and minimum level of inter-dependencies among processors.

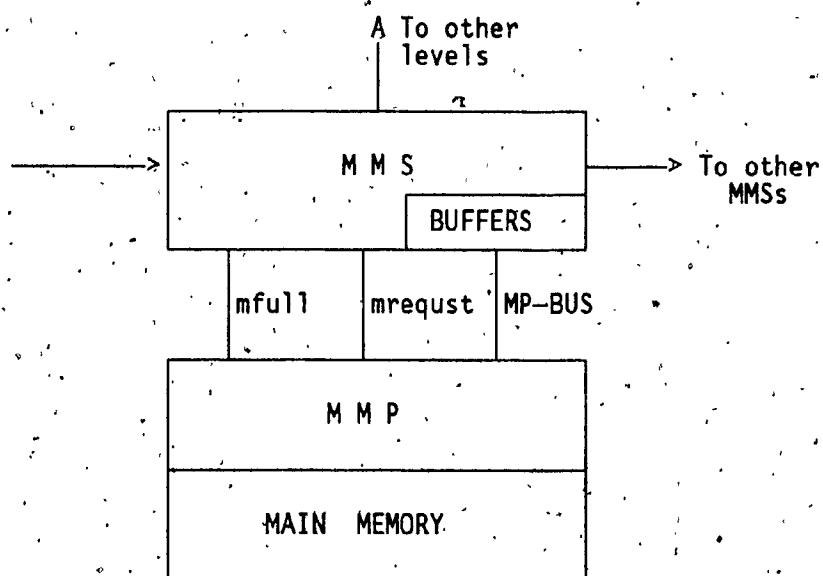
The interface signals and buses are described below:

1. MREQUEST.- This flag is set ON as soon as a request to the MM arrives to the switch. When the request has been honored, the flag is set OFF.
2. MFULL.- This flag is set ON when the storage capacity of the MMP has been reached. The flag will be set OFF as soon as a CLEAR(P) control packet is accepted by the MMP. The CLEAR packet deletes one packet of data from main memory.
3. MPBUS.- Bus used to transfer packets between the MMP and the MMS.

Initially, the MM has all main memory available and is ready to store

packets. The initial state is FREE. As soon as a request arrives to the switch, the MMS will check its tables to see if the arriving packet should be honored by the MMP. If the request is to update tables (from other MMs), then the MMS will update the appropriate table and will pass the request to the other MMs. If the request is a GET, the MMP will get the requested packet either from main memory or from the Device Manager. If the latter, a CP packet, requesting the packet, will be sent to the DM. If the request is a STORE, the MMP will first check if there is enough storage available. If not, the request will be passed on to other MMs. If the request is CLEAR, the MMS will update the MMPTABLE and will notify this to the other MMs. The cleared packet will no longer exist in this MM. The dynamic behaviour of the MM is described in the following page:

Fig 10.- MEMORY MANAGER



4.6 MEMORY MANAGER DYNAMIC FLOW

```
MEMORY MANAGER
Begin
FREE:= True
BUSY:= False
MAVAIL:= MSIZE
MFULL:= false
Begin
Do forever
If Dest= MML then
Case COMMAND of
    UPDATE: Begin
        Update MMPTABLE,MMLTABLE
        SEND(UPDATE, next MMS)
    End
    STORE: Begin
        If (MFULL or MREQUEST) then
            SEND(STORE, next MMS) else
                Begin
                    MREQUEST= True
                    Load packet ** The packet has been stored
                    MAVAIL= MAVAIL-1
                    MREQUEST= False
                    SEND(UPDATE,next MMS)
                End
    End
    GET: Begin
        If PKT not in MMLTABLE then
            SEND(GET, DML) else ** pass GET to Device Level **
        If PKT in MMPTABLE then
            Begin
                MREQUEST= True
                Read packet
                MREQUEST= False
                SEND(PKT, Origin level)
                SEND(UPDATE,next MMS)
            End else
                SEND(GET, next MMS) ** pass GET to next MMS **
        End
    End
    CLEAR: Begin
        If PKT not in MMLTABLE then ERROR else
        If PKT in MMPTABLE then
            Begin
                MREQUEST= True
                Clear Packet
                MAVAIL= MAVAIL+1
                MREQUEST= False
                SEND(UPDATE, next MMS)
            End
        else
            SEND(CLEAR, next MMS)
    End
End
```

4.7. THE EXECUTION MANAGER LEVEL

The Execution Manager Level consists of several Execution Managers (EMs) each one consisting of a switch and a processor. The processor also has a local memory to hold the packet group. The function of the EMP is to execute the IP packet once the corresponding EP and DPs have been received. The interface between the switch and the EMP is shown in Fig. 11 and consists of the following flags and buses:

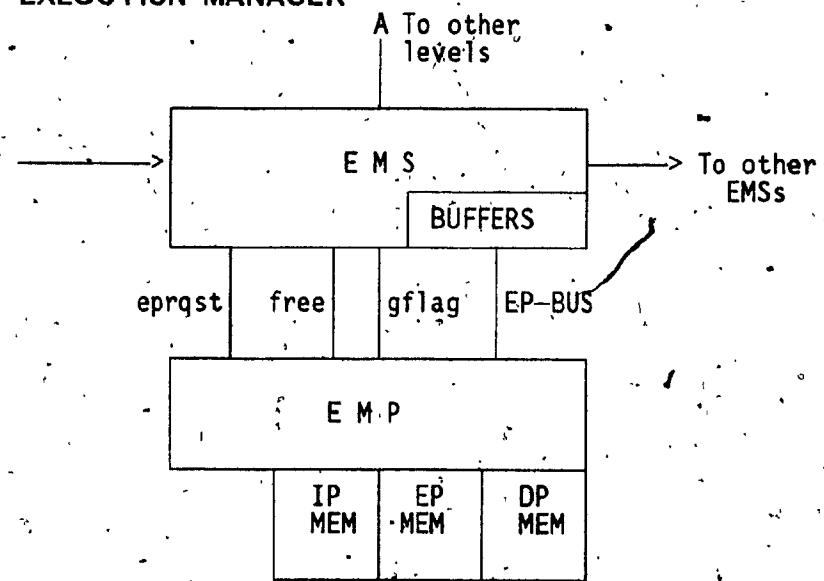
1. EPRQST.-This signal is set ON as soon as an EP packet arrives at the EM-switch and encounters the EMP free.
2. GFLAG.-This flag is set ON as soon as all the members of the Packet Group are found in the EMP's local memory.
3. FREE.-This flag is set ON as soon as the EMP is ready to accept a new Packet Group.
4. EPBUS.-This bus transfers packets between the EMP and the EMS.

Initially, the EMP is free to receive requests for execution from any User Manager. As soon as a request arrives, if the EMP is free, the switch will accept the EP by turning EPRQST flag ON. The EMP will go into a WAIT state until the IP and DPs forming the Packet Group of the particular EP are received by the switch. At that time, GFLAG is turned ON and the IP can start executing. The EMP goes into a BUSY state. At the end of the execution process, the EMP goes into the FREE state again by turning the FREE flag ON. If the EMP is busy when a request arrives, the EMS will pass the request to the

next EMS until one idle EMP is found.

The dynamic behaviour of the EM is described in the following page in pseudo-code format.

Fig 11.- EXECUTION MANAGER



4.8 EXECUTION MANAGER DYNAMIC FLOW

```
EXECUTION MANAGER
Begin
Do forever
FREE:= True
Case PKTTYPE of
    EP: Begin
        If FREE= True then
            Begin
                FREE= False
                EPRQST= True
                Load EP *** EP grabs the idle EMP ***
                WAIT= True
                End else
                SEND(PKT, next EMS)
            End
        IP,DP:Begin
            If FREE= False then
            If PKTGROUP(P)= PKTGROUP(IP,DP) then
                Begin
                    Load IP,DP*** Packet Group being collected **
                    If GFLAG= 1 then *** Packet Group ready ***
                    Begin
                        Run Packet Group
                        SEND(Update,EP,DP,PKTs, UML)
                        WAIT= False
                    End
                    else SEND(PKT, next EMS) ** PKT.GRP(P)<> PKT.GRP(IP,DP)
                End
            End
        End
    End
```

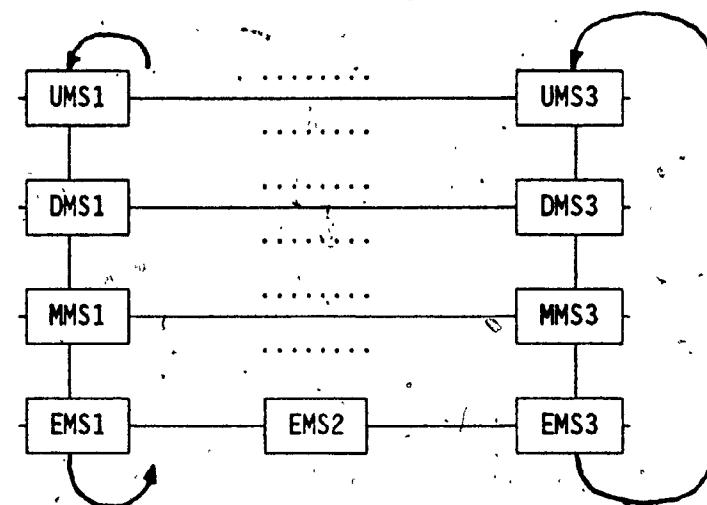
4.9 HARDWARE CHANGES IN THE PACOS ARCHITECTURE.

Although adding one Slice to PACOS is seen as the simple process of inserting a Slice PC board into a circular mother board and updating all the switching tables, it may happen that the reason for expansion is motivated by a very high utilization of only one level in PACOS. (e.g. the EML, but not the other levels). Therefore we should provide for modular units at the Switch-Processor scale, rather than at the Slice scale.

Fig. 12 illustrates a situation where only one EMS-EMP module has been inserted. (only switches are shown for simplicity). By inhibiting the non-used ports of the new switch, correct routing of incoming packets is guaranteed; i.e. packets are not routed to non-existing MMS2, DMS2 or UMS2.

To ensure uniformity, a zero value for table item "Slice 2" should be entered in the switch tables of the first three levels. By introducing hardware in this manner, optimum usage of resources is obtained. In a similar manner, Device Managers, Memory Managers or User Managers can be added when the need arises. In order to reflect the fact that EMS3 and EMS1 are now routing packets to other levels on behalf of EMS2, the routing algorithms would have to be changed.

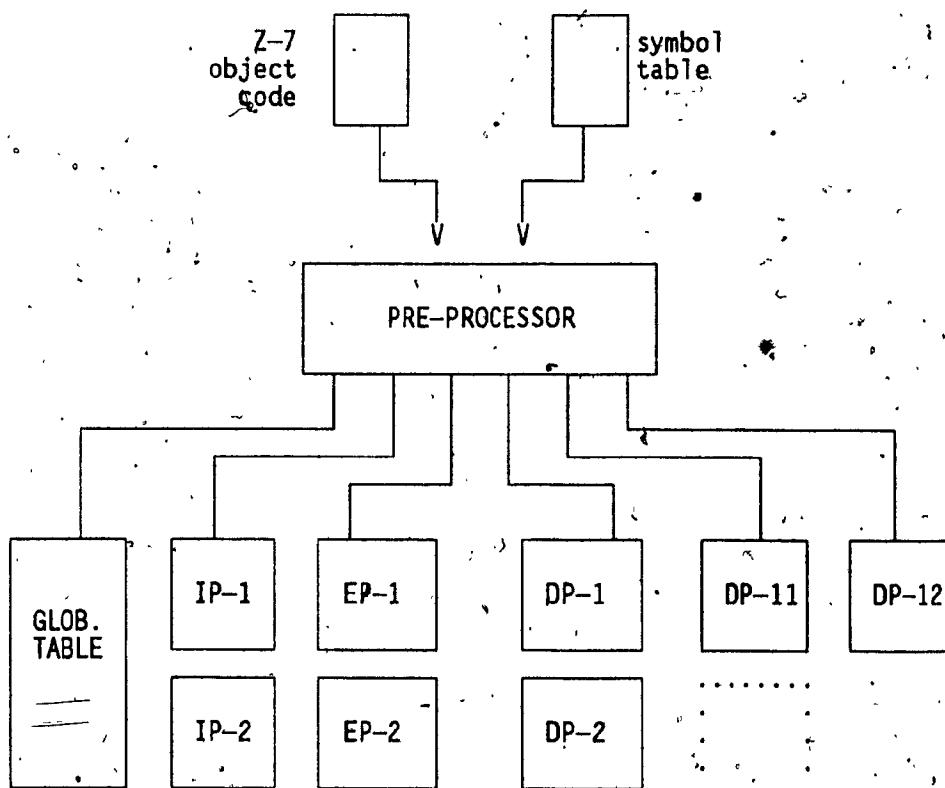
Fig. 12.- ADDING ONE EMS-EMP



5.0 THE PARTITIONING ALGORITHM.

To illustrate the basic concepts of packetizing a standard object code program, a basic machine language will be chosen. This is the stack-oriented language for the academic machine Z-7. (Ref. HOL-1). The main reason to choose this language has been simplicity. Programs written in Z-7 consist of a symbol table and several blocks of code; each block starting with a label entry and ending with an EXIT instruction. A program written in Z-7 language has to pass through a pre-processor that will generate the packets in a format that is understood by PACOS. See Fig 13.

Fig. 13.— PACOS PRE-PROCESSOR



The input to the pre-processor is a list of object code plus a symbol table. The output consists of packets and a table, GLOBTABLE, that references all global variables. Local variables are referenced in the EP packets. See Fig 14.

Fig.14.- PRE-PROCESSOR INPUT.- GLOBTABLE

Z-7 OBJECT CODE	SYMBOL TABLE	GLOBTABLE
0 OPCODE	OPERAND TYPE ADDR	OPERAND OBJECT PKT
1 OPERAND	OPERAND TYPE ADDR	OPERAND OBJECT PKT
2 OPCODE	OPERAND TYPE ADDR	OPERAND OBJECT PKT
3 OPERAND	OPERAND TYPE ADDR	OPERAND OBJECT PKT
4 OPCODE	OPERAND TYPE ADDR	OPERAND OBJECT PKT
5 OPERAND	OPERAND TYPE ADDR	OPERAND OBJECT PKT
6 OPCODE	OPERAND TYPE ADDR	OPERAND OBJECT PKT
7 OPERAND	OPERAND TYPE ADDR	OPERAND OBJECT PKT
.....
EXIT OPCODE
.....
EXIT

The algorithm of the pre-processor, necessary to produce PACOS executable code, is described below in pseudocode format.

The main program reads the object code and starts generating the IP, EP packets as well as initializing the GLOBTABLE. If the next word read is PUSH or ENTER or ALLOCATE, the procedure CHECK will read the following operand, and will write it onto the EP packet. If the variable is global, the table GLOBTABLE is also updated. If the variable is a substructure the procedure ICW will generate a DP packet that will contain working space for the allocation of the substructure. A new packet will be generated as soon

as EXIT or the maximum packet length has been reached.

PACKETIZING ALGORITHM. (Object SAMPLE is being packetized)

```
ICW: Procedure
Begin
If Word(I)=Global then          (* Known from the symbol table *)
If Word(I) not in GLOBTABLE then
Generate Word(I) entry in GLOBTABLE
If Word(I)= substructure then.
    Begin
        Create new DP packet header
        Allocate locations in DP (* Space is allocated for Word(I) *)
    End
End

CHECK: Procedure
Begin
I:=I+1
Read Word(I)                      (* Read operand *)
Write Word(I) onto IP
If Word(I) not in EP then
    Begin
        Write Word(I) onto EP
        ICW
    End
End

Begin (* Main program *)
OBJECTNAME:= SAMPLE
MAX:=Maximum Packet Length
Create GLOBTABLE Packet Header
While not EOF(SAMPLE) do
    Begin
        Create new IP Packet Header
        Create new EP Packet Header
        I:=0
        Read Word(I)
        While (I< MAX) or (Word(I)=EXIT) do
            Begin
                Write Word(I) onto IP
                If (Word(I) = PUSH) or ENTER) or ALLOCATE) then
                    CHECK
                I:=I+1
                Read Word(I)          (* Read opcode *)
            End
    End
End
```

A major research effort should be placed in identifying optimum algorithms

for a specific PACOS structure. Packet length, hardware design, program idiosyncrasies, etc. play an important role in this optimization. Because of this complexity, we are attempting to initially work with simple tools and algorithms, and further develop more accurate solutions, while progressing in our observations.

6.0 AN APPLICATION EXAMPLE.

The following program converts Fahrenheit degrees to Celsius. It is shown here in Pascal-like format for easy comprehension, although it runs in PACOS in the stack-oriented Z-7 language (see Ref. HOL-1), as indicated in Appendix A. The input file INFILE contains the number of data items plus the data values in Fahrenheit degrees. The output file OUTFILE contains the values in Celsius degrees.

```
Program CELSIUS (I=INFILE,O=OUTFILE)
Var I,M: integer
    TEMPF,TEMPC: Array(0..20) of integer

Procedure INPUT (* IP-1 Packet *)
Begin
  For I:=0 to M do
    Readln(INFILE,TEMPF(I))
  End

Procedure CONVERT (* IP-2 Packet *)
var I: integer
Begin
  for I:=0 to M do
    Begin
      TEMPc(I):= (TEMPF(I)-32)*5/9
      Writeln(OUTFILE,TEMPc(I))
    End
  End

Begin (* Main program, IP-3 *)
  Readln(INFILE,M)
  I:=0
  INPUT
  I:=0
  CONVERT
End
```

The PACOS pre-processor will partition the program CELSIUS into 3 IPs, 3 EPs and one GLOBTABLE (DP-0). The files INFILE and OUTFILE will be partitioned into one DP packet each.

Initially, a user requests to run CELSIUS. The starting address of CELSIUS,(IP3,19), is assumed to be known. The steps outlined in Section 2 of this report will be used to explain the flow of packets in PACOS.

1.-A CREATE(CELSIUS) control packet is sent to the UM Level.

2.-A UMP accepts the job and sends GET(EP3(CELSIUS), to MM).

3.-As EP3 does not exist in memory, the MMP will attempt to retrieve from disk not only EP3, but rather the complete Packet Group Set of EP3. The PKT.GRP.SET of EP3 consists of IP3,EP3,IP2,EP2,IP1,EP1,DP1(INFILE), DP1(OUTFILE) and GLOBTABLE. (In this case all the packets are in the same Packet Group Set.)

4.-PKT.GRP.SET is sent to MM.

5.-PKT.GRP.SET is stored in memory.

6.-UMP receives EP3 plus GLOBTABLE.

7.-MMP sends PKT.GRP.3 to EM.

8.-EMP executes the Packet Group starting at location 19. At location 20 it jumps to MAIN (IP3, location 0). At location 10 it jumps to INPUT (IP1,-location 0). At this time execution stops since IP1 is not locally available. The execution address at the start of a process or at the return from a subroutine, is stored in the START ADDRESS field of the EP header. In our case, the return address (11) is stored in the header of EP3. EMP sends UPDATE(EP3) to UM.

9.-UMP updates the EP packet as well as the GLOBTABLE values affected (In this case, I=0, M=7). A request is sent to update EP3 in memory. A request is also sent to execute PKT.GRP.1.

10.-MMP updates the EP3 packet and sends PKT.GRP.1 to EM Level.

11.-PKT.GRP.1 executes in one EMP until the EXIT instruction is reached.

12.-Not applicable in this example (Next PKT.GRP.SET does not exist)

13.-After execution, the EMP sends the EP1 packet to the UM for updating.

9.-UMP updates the EP packet as well as the GLOBTABLE values affected (TEMPF(I),I). It sends the EP packet to be updated at the MM. It also sends a request to execute PKT.GRP.3 (starting address 11).

The same process continues until STOP is encountered. At that time the UMP will be notified that the program CELSIUS has finished execution and it will be destroyed from the system.

While the process of packetizing a program is one more step in the development process, this should not be seen as an impediment for programmers. The objective is to ensure that production programs that are already in packetized format, such as compilers, utilities, applications, etc, run efficiently and at minimum cost. Automatic utilities that can compile and packetize a high level language, such as Pascal, are feasible and should be transparent to programmers.

PKT.GRP.1 (Celsius) + GLOBTABLE

0 IP-1 (Celsius) 15

00	Celsius	(1)
	Celsius	(1)
	Pkt.No.	(1)
0	PUSH	(5)
1	TEMPF	(0)
2	PUSH	(5)
3	I	(1)
4	FETCH	(6)
5	ADD	(8)
6	GET	(13)
7	STORE	(7)
8	PUSH	(5)
9	I	(1)
10	PUSH	(5)
11	I	(1)
12	FETCH	(6)
13	PUSH	(5)
14	1	(3)
15	ADD	(8)
16	STORE	(7)
17	PUSH	(5)
18	M	(2)
19	FETCH	(6)
20	PUSH	(5)
21	I	(1)
22	FETCH	(6)
23	SUBTRACT	(9)
24	REPEAT	(5)
25	EXIT	(4)

0 EP-1 (Celsius)

32 48 63

01	Celsius	Pkt. No.1	0
TEMPF			
1	INFILE	DP-1	1
I			
0000101	(value)	0	
M			
1	INFILE	DP-1	0
1			
00100111	(value)	1	

0 DP-1-INFILE

63

11	INFILE	1	0
M			
0	TEMPF	7	
1		23	
2		45	
3		52	
4		3	
5		75	
6		100	
7		65	

GLOBTABLE (Celsius)

0 63

11	Celsius	DPG-0	0
M	INFILE	DP-1	
M	CELSIUS	EP-1	
M	CELSIUS	EP-2	
I	CELSIUS	EP-1	
TEMPF	INFILE	DP-1	
TEMPF	CELSIUS	EP-1	
TEMPC	OUTFILE	DP-1	
TEMPC	CELSIUS	EP-2	

AN APPLICATION EXAMPLE.

42

PKT.GRP.2 (Celsius)

IP-2 (Celsius)
0 15

00	Celsius	(1)
	Celsius	(1)
	Pkt.No.	(2)
0	PUSH	(5)
1	K	(5)
2	PUSH	(5)
3	TEMPF	(0)
4	PUSH	(5)
5	I	(1)
6	FETCH	(6)
7	ADD	(8)
8	FETCH	(6)
	
	
	
62	ADD	(8)
63	FETCH	(6)
64	PUT	(4)
65	PUSH	(5)
66	I	(1)
67	PUSH	(5)
68	I	(1)
69	FETCH	(6)
70	PUSH	(5)
71	1	(3)
72	ADD	(8)
73	STORE	(7)
74	PUSH	(5)
75	M	(2)
76	FETCH	(6)
77	PUSH	(5)
78	I	(9)
79	FETCH	(5)
80	SUBTRACT	(9)
81	REPEAT	(3)
82	EXIT	(4)

EP-2 (Celsius)

32 48 63

01	Celsius	Pkt. No.2	0
TEMPF			
1	INFILE	DP-1	1
I			
0010101	(value)	0	
M			
1	INFILE	DP-1	0
1			
0010011	(value)	1	
TEMPC			
1	OUTFILE	DP-1	0

DP-1-INFILE

63

11	INFILE	1	0
M			
1	TEMPF	23	
2		45	
3		52	
4		3	
5		75	
6		100	
7		65	

DP-1-OUTFILE

63

11	OUTFILE	1	0
TEMPC			
1			
2			
3			
4			

AN APPLICATION EXAMPLE.

PKT.GRP.3 (Celsius)

0 IP-3 (Celsius) 15

00	Celsius (1)
	Celsius (1)
	Pkt. No. (3)
0	PUSH (5)
1	M {0}
2	GET (13)
3	STORE (7)
4	PUSH (5)
5	I {1}
6	PUSH (5)
7	0 {5}
8	STORE (7)
9	ENTER (1)
10	INPUT (2)
11	PUSH (5)
12	I {1}
13	PUSH (5)
14	0 {5}
15	STORE (7)
16	ENTER (1)
17	CONVERT (3)
18	EXIT (4)
19	ENTER (1)
20	MAIN (4)
21	STOP (12)

0 EP-3 (Celsius)

32

48

63

01	Celsius	Pkt. No.3	19
M			
1	INFILE	DP-1	0
I			
	0000101	(value)	0
INPUT			
1	CELSIUS	IP-1	0
CONVERT			
1	CELSIUS	IP-2	0
MAIN			
1	CELSIUS	IP-3	0
0			
	0010011	(value)	0

0 DP-1-INFILE 63

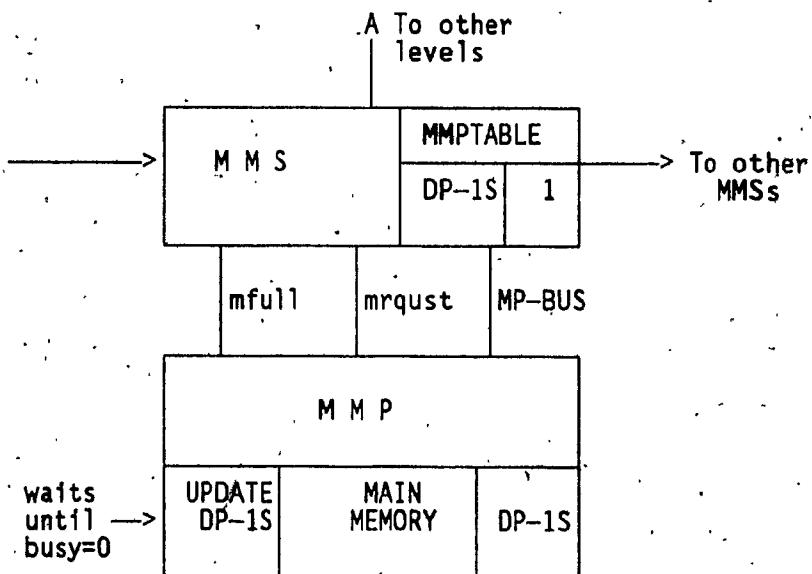
11	INFILE	1	0
M			
1	TEMPF	23	7
2		45	23
3		52	45
4		3	52
5		75	3
6		100	75
7		65	100

AN APPLICATION EXAMPLE.

7.0 SYNCHRONIZATION CONSIDERATIONS.

Synchronization in PACOS is obtained by a semaphore-like mechanism. To illustrate how a shared resource is accessed by several processes without danger of deadlock, we will use a shared DP packet as an example. The shared packet, DP-1S, resides in one MMP. (Refer to Fig. 15). The MMPTABLE, located in the MM switch, allocates one entry for this shared packet, that contains a "Busy bit". This bit will be set to 1 as soon as a request to update the shared packet arrives. If, while the bit is set to 1, another update request for the same packet arrives from a different program, this request will be queued in a FIFO queue. The arriving UPDATE packet will be temporarily allocated in a buffer until the "Busy bit" returns to 0. At that time, the waiting request will be honored by the MMP.

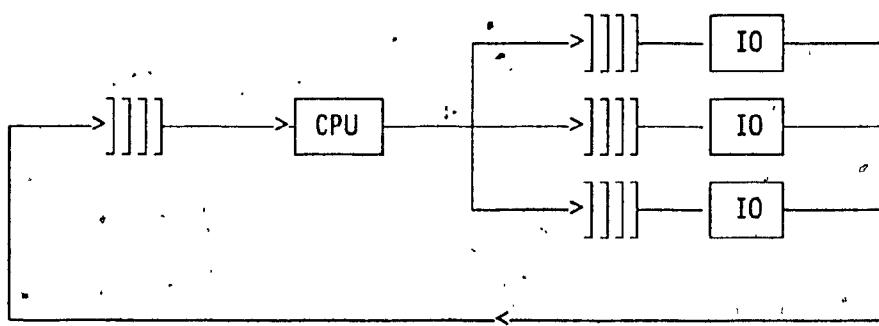
Fig 15.- SHARED PACKET



8.0 PERFORMANCE CONSIDERATIONS.

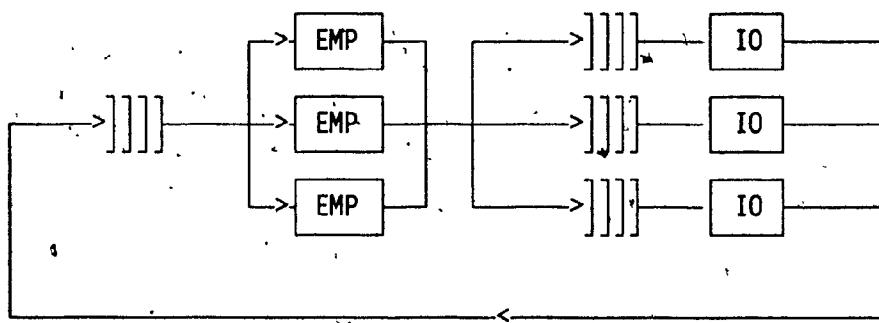
A single-CPU multiprogramming system can be simulated by a set of queues and servers as represented in Fig 16.

Fig. 16.- Single CPU system.



The multi-CPU multiprogramming system PACOS can be represented by a set of queues and servers as per Fig. 17

Fig. 17.- PACOS multi-server queueing model..



To calculate the number of EMP processors necessary to replace a single large processor CPU, the total throughput supplied by both machines will be equated. The same mixture of programs will be used.

A = Throughput of a single CPU. (instr/sec)

B = Throughput of a single EMP. (instr/sec)

TTIME = Average turnaround time per job (secs). It is equal to the average execution time plus the waiting time per job.

ETIME = Average execution time per job. (secs)

E(t_A) = Execution time of one page in a single-CPU system. E(t_B) = Execution time of one packet group in the EMP.

L = Number of instructions executed per packet group (or page).

n = Number of Slices in PACOS.

\bar{U}_A = Delay caused by memory fetch and data transfer of one page in the single-CPU system. \bar{U}_B = Delay of one packet group in PACOS.

φ_A = Delay caused by waiting time spent in the dispatch queue for a single-CPU system. φ_B = Waiting time spent until a free EMP is grabbed by a packet group.

ρ_A = Utilization of the CPU. ρ_B = Utilization of one EMP in PACOS.

In a multiprogramming environment, the average turnaround time of J jobs running concurrently on a single-CPU system will be compared to the average turnaround time of the same number of jobs running on PACOS. We will consider that packets and pages are of the same length.

Each job consists, on the average, of M executable pages or packet groups.

$$J \cdot TTIME = J \cdot M \cdot \left(\frac{L}{A} + \varphi_A + G_A \right) = J \cdot M \cdot \left(\frac{L}{B} + \varphi_B + G_B \right) \text{ or:}$$

$$\frac{L}{A} + \varphi_A + G_A = \frac{L}{B} + \varphi_B + G_B \quad (1)$$

Using standard queueing theory, (IBM-1, MAR-1), and assuming that the service time of execution processors follows the exponential distribution, we derive the average waiting times φ_A and φ_B .

$$\varphi_A = \frac{\rho_A \cdot E(t_A)}{1 - \rho_A} \quad (2)$$

where:

$$\begin{cases} E(t_A) = \frac{L}{A} \\ \rho_A = \text{CPU utilization} \end{cases}$$

$$\varphi_B = \frac{p_n(\mu) \cdot E(t_B)}{n \cdot (1 - \rho_B)} \quad (3)$$

where:

$$\begin{cases} \mu = n \cdot \rho_B \\ \rho_B = \text{EMP utilization} \end{cases}$$

$$p_n(\mu) = \frac{1 - r(\mu)}{1 - \rho_B \cdot r(\mu)}$$

$$r(\mu) = 1 - \frac{\mu^n}{n! \sum_{k=0}^n \frac{\mu^k}{k!}}$$

$$E(t_B) = \frac{L}{B}$$

Equation 2 indicates that when the utilization of the single-CPU becomes

close to 1, the degradation of waiting time can only be reduced by increasing the CPU processing speed, i.e. reducing the execution time $E(t_A)$. However, when the utilization of each EMP in PACOS becomes close to 1, we can reduce the waiting time by simply adding more slices (increasing "n"), which in most cases is simpler and less costly than upgrading the single-CPU processor.

Equation 1 becomes:

$$\frac{L}{A} \left(1 + \frac{\rho_A}{1 - \rho_A} \right) + U_A = \frac{L}{B} \left(1 + \frac{P_n(\mu)}{n*(1 - \rho_B)} \right) + U_B = K$$

where K is the specific cycle time (part of the turnaround time) per page or packet group to be used as a parameter reference. Substituting L as a function of K in the previous equation, we obtain:

$$\frac{A}{B} = n * \frac{(1 - \rho_B)}{(1 - \rho_A)} * \frac{(K - U_B)}{(K - U_A)} * \frac{1}{(n*(1 - \rho_B) + P_n(\mu))} \quad (4)$$

Equation 4 establishes the performance function of a single-CPU system (in multiples of the basic EMP speed) in relationship to the performance obtained by a PACOS machine of "n" slices while loading both systems with the same multiprogramming level.

Following A.V. Pohm (POH-I), the optimum level of service is obtained when the average execution time per job is equal to the average wait time per job. (memory access + routing delays + page fault timing). In other words, the optimum balance is obtained when neither resource, EMP or rest of the

machine, has to wait for the other to finish.

We define the Balance Ratio as :

$$BR = \frac{ETIME}{TTIME} \quad (5)$$

The optimum BR is 0.5. When $BR > 0.5$ then the EMP is the bottleneck. When $BR < 0.5$ then the wait-for-EMP, routing and memory fetching delays are the bottleneck.

From equations 4 and 5 we can derive the ratio of processing speeds of single-CPU versus single EMP as a function of the number of slices in PACOS, "n", in relationship to the optimum Balance Ratio of PACOS.

Although P_n is a function of "n", its absolute value oscillates between 0.5 and 1. Typical value is 0.6. (see IBM-1, pp. 34-40). Since the routing delays of a single-CPU system are in the order of microseconds while in PACOS are in the order of milliseconds, we can estimate that $G_B \gg G_A$. Other typical values, used in the simulation of PACOS in Section 11 are: $L=4,000$ instructions executed per packet group; $B=100,000$ instr/sec.; $G_B=2$ msecs. This delay is estimated based on the fact that a 4 Kbytes packet takes on average, four inter-nodal delays of 0.4 msecs to reach the EM level, plus 0.2 msecs to be fetched from memory, plus 0.2 msecs to update tables in the UM and MM levels.

With $BR=0.5$, we have: $K = TTIME/M = 2 * ETIME/M = 2*L/B$. where M is the average number of packet groups executed per job.

Using K as a parameter, we can plot equation 4, illustrated in Fig. 18. The

maximum value of A/B is obtained when $n \rightarrow \infty$, the result is $(A/B)_{\max} = 1/(1-\rho_A)$, as long as $K > G_A, G_B$. The maximum effective value of "n" is obtained when $A/B = n$ since, beyond this point, the relative performance of PACOS does not improve with the addition of more slices.

Let us consider an example with the following typical values:

$\rho_A = 0.99$; $\rho_B = 0.9$; $K = 0.08$ secs/packet group; $P_n = 0.6$. Substituting these values, we obtain:

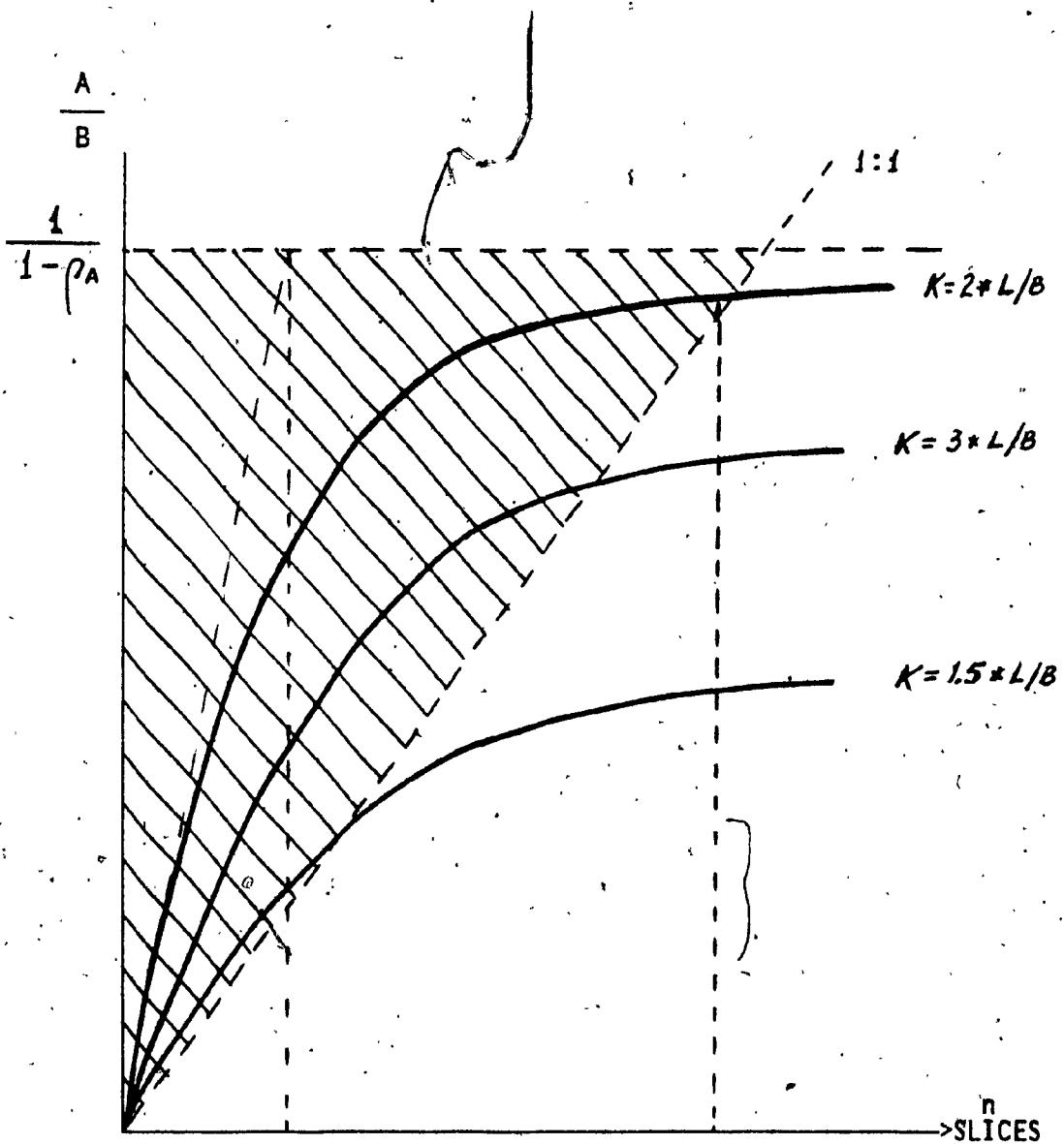
$$\frac{A}{B_{\max}} = 100 ; \quad n_{\max} = 94 \text{ slices} ;$$

Substituting the same values in equation 4 we obtain the CPU speed required to match the performance of a PACOS machine with "n" slices. For example:

For $n = 6$ slices, $A/B = 50$.

These results indicate that a PACOS machine used at the indicated EMP utilization level, will consistently outperform a single-CPU system having a speed ratio equal to the number of slices of PACOS. For 94 or more slices, PACOS' comparative performance will start degrading. The linear margin where PACOS outperforms the single-CPU system is, however, significant.

Fig. 18.- Processing ratio (CPU) vs. No. of Slices (PACOS)



$$n_a = \frac{P_n}{\frac{K-G_B}{K-G_A} (1-\rho_B)}$$

$$n_{max} = \frac{1}{1-\rho_A} \times \frac{K-G_B}{K-G_A} - \frac{P_n}{1-\rho_B}$$

PERFORMANCE CONSIDERATIONS.

Several conclusions can be obtained from these curves:

1. The performance curves flatten towards the asymptote $A/B = 1/(1 - \rho_4)$ when $K \gg \rho_A, \rho_B$; (usually this is the case). The higher the throughput (or CPU utilization), the higher is the range of operation of PACOS.
2. Since we are interested in achieving a performance which is equal or superior to the one provided by a single-CPU system, the effective area of operation of PACOS is the zone where $A/B > n$. Within this area, the PACOS machine outperforms a single-CPU system. For example, with $K = 2^* L/B$ (optimum Balance Ratio) and $\rho_4 = 0.99, \rho_B = 0.9$, only 6 slices are required to replace a CPU having an A/B value of 50,
3. The optimum curve is obtained for $K = 2^* ETIME/M = 2^* L/B$, as expected. For higher or lower values of K , the performance of PACOS degrades.

Equation 4 and the corresponding curves indicate that the performance of a PACOS machine, intended to replace a large single-CPU system, is almost linearly proportional to the number of slices, and outperforms the latter, within a large range of processor utilization. These theoretical results are very encouraging and will be compared with the simulation results in Section 11.

9.0 PACOS SIMULATOR

The abstract machine PACOS has been simulated in GPSS, according to the original specifications and the performance assumptions indicated in Section 8. The GPSS program is attached in Appendix C.

The first GENERATE block generates programs, one per GPSS transaction. This program transaction is later split into multiple transactions that, in reality, are packets. These packets move back and forth between PACOS levels until the end of the program execution is reached. At that time, turnaround time, execution time and other statistics of the program are saved for printing and further analysis. Packet transactions have been assigned the following fullword parameters:

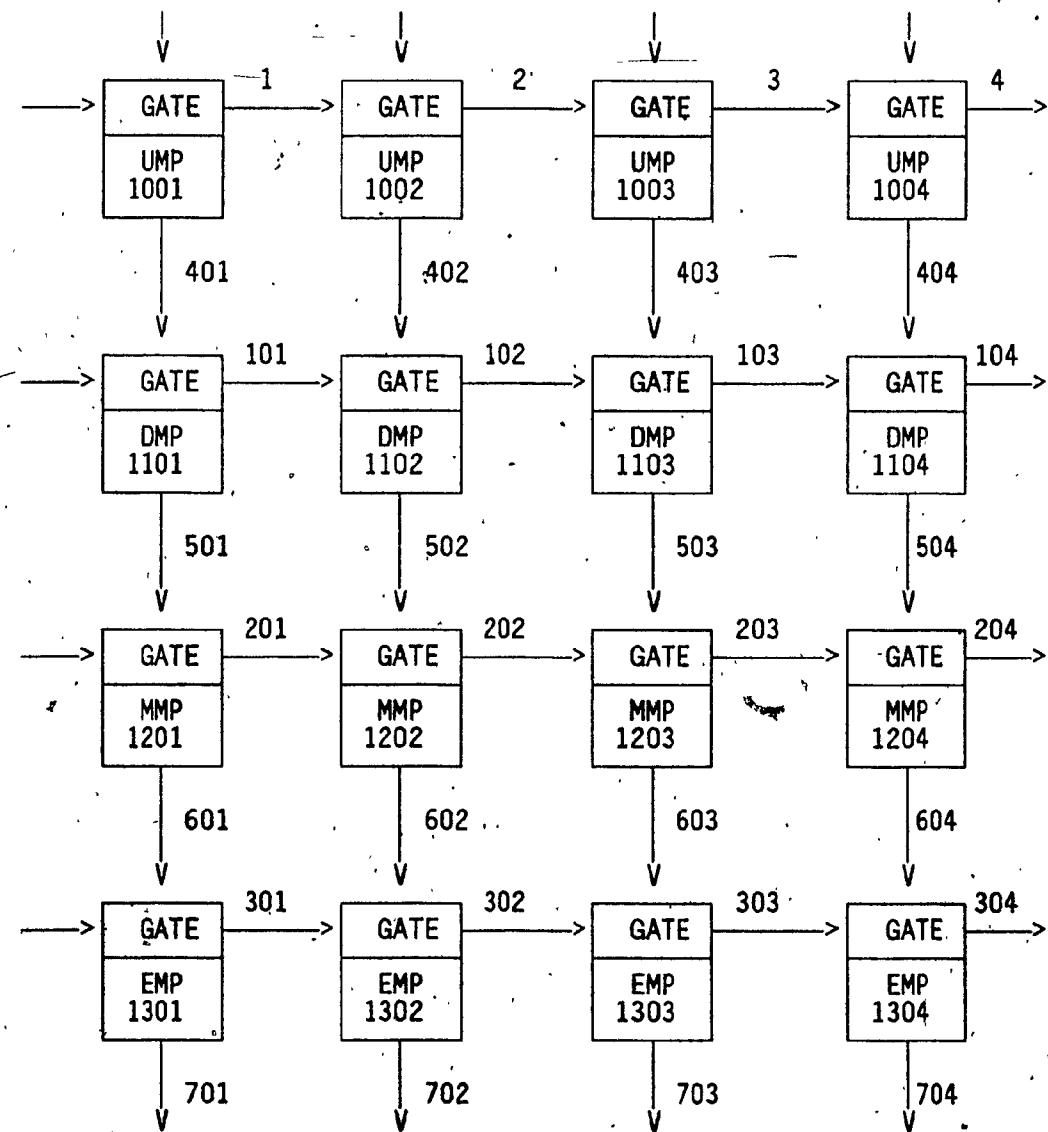
PARM. NO.	DESCRIPTION
1.-	Processor (or node) number where the packet resides at a specific time.
2.-	Program No.
3.-	Packet No.
4.-	Packet length (in bytes)
5.-	Destination Level. Levels of PACOS are: 0: User Manager 1: Device Manager 2: Memory Manager 3: Execution Manager
6.-	Type of Control Command. Commands in PACOS are:

- 1: GET
 - 2: UPDATE
 - 3: STORE
 - 4: CLEAR
 - 5: CREATE
 - 6: SEND
- 7.- Packet Type: 1(EP), 2(IP), 3(DP), 4(CP)
- 8.- Originating level (s e Parm. 5)
- 9.- Horizontal (Loop) communications link no. It is assigned the number of the processor (PF1) minus 1000 by variable LINK1.
- 10.- Vertical (Slice) communications link no. It is assigned the value of variable LINK1 plus 400 by variable LINK2..
- 11.- Holds the number of packets that belong to the same packet group.
- 12.- Program length. (Initially in number of packet groups executed)
- 13.- Holds the turnaround time of the job. Used for tabulation purposes.
- 14.- Holds the clock time of every Packet Group entering a free EMP.
- 15.- Accumulated number of Packet Groups called for execution.
- 16.- Holds the UMP number creator of the object.
- 17.- Holds the actual time that the job spent while executing in the Execution Manager Level.

9.1 SIMULATION OF THE SWITCHING NETWORK

Processors and links are GPSS facilities numbered as per Fig 19.

Fig. 19.- MEANING OF FACILITIES



The following limitations are applicable to this structure:

- a) The network is half-duplex, ring topology. Packets are transmitted in one direction only. Therefore Slice link no. 801 becomes automatically no.,401 and the last Loop link on level 0 becomes link no. 1.
- b) For simulation purposes, a maximum number of 100 slices is available.
- c) Packets are transmitted to the next switching processor as soon as the link (facility) is available. A transmission delay (V\$DEL) is assigned before reaching the next switching processor. The value of this delay is 100 microseconds for a packet size of 1 Kbytes. The speed of the links is 80 Mbps or 10,000 Kbytes/s. The transmission delay is proportional to the length of the packet.

9.2 SIMULATION OF PROGRAM BEHAVIOUR DURING EXECUTION

The concept of Packet Execution is based on the known "locality of access" characteristic of program behaviour. (MAD-1), (CAR-1). In simple words, it states that the probability of the CPU addressing the instruction previous or next to the current one is very high. Therefore it is advantageous to execute code while keeping in local memory a certain number of previous and subsequent instructions.

It is also known that an adequate design of the memory hierarchy, (cache, main memory, secondary memory) is vital to achieve an adequate optimization

of resources. If the memory hierarchy is properly designed, the timing involved in accessing packets from secondary storage (Device Manager), should not degrade the performance of the system since these accesses can be done in parallel with execution of packet groups. (The Packet Group Set is fetched in advance). (see POH-1, pp. 92-116, for a discussion on optimization of different memory hierarchies). Therefore, in simulating PACOS, we will assume that access to secondary storage is completely transparent to the system.

Since our main interest is to compare the performance of a single-CPU, virtual memory system with the one provided by PACOS, we will define "a priori" a packet length of 4,000 bytes, which is a standard page size in existing systems. The sample programs are short (average of 17 packet groups per program) to avoid lengthy GPSS simulation time. Since the same type of programs are run on both single-CPU and PACOS systems, we expect the results to be consistent regardless of program length.

In order to reflect the multiple characteristics of programs during execution, different functions have been defined. The following situations, that usually occur during program execution, will be considered.

- A jump to a loop or subroutine (N cycles). If the loop is outside the current packet, the calling IP will be brought in to execute N times.
- A jump to an instruction located in a different packet or I/O. (Execution of the current packet would stop)
- A jump to a subroutine located in a different packet. In this case execution stops, but the current IP will be called again to execute after

the subroutine has finished processing.

- Calls to subroutines or loops, (both inside or outside the current packet), may occur several times within one packet.

To simulate this behaviour we define the following GPSS functions:

- GEN.- Gives the number of packets that will compose a new packet group minus one. (EP is not counted). Usually, a Packet Group will consist of one IP, one EP and one or more DPs.
- PTIME.- Gives the basic execution time of an instruction packet of 1 Kbytes in size. (62 instructions). At a rate of 0.1 MIPS, the execution time will be 1.5 msecs.
- PLEN.- Program length in number of Packet Groups executed. Basic packet size is 4 Kbytes.
- CBND.- Gives the expected number of iterations encountered in a loop. This figure is, of course, very much program dependent. We will use an average of 6 (six) iterations per loop.
- LPPR.- Gives the probability of encountering a jump to an I/O, loop or subroutine located in a different packet.
- LPNO.- Gives the number of jumps to a different packet that the current packet will experience during execution.

We also define several variables. Two of them relate to program behaviour: SPAWN and CPUTM.

SPAWN is defined as the variance of the number of times, over a normalized packet size of 4,000 bytes, that a given IP will be dispatched for execution.

$$\text{SPAWN} = \text{LPPR} * \text{CBND} * \text{LPNO} * (4 - \text{NORM})$$

This variable reflects the fact that the number of packets executed per program decreases when the packet length increases.

We also define the variable CPUTM as the execution time used by one packet group.

$$\text{CPUTM} = \text{PTIME} * \text{CBND} * \text{NORM} / \text{CPTM}$$

where NORM is the normalized packet size in thousands and CPTM is the normalized EMP processing speed in multiples of the basic 0.1 MIPS. (value of B in Section 10)

The simulation program operates in the following way: A number of programs are generated, one every seven msecs. Since all these programs run concurrently in the machine, they represent the Multiprogramming Level, MPL, or load of the system. The GPSS clock runs in microseconds. Each program, at creation time, is assigned a User Manager Processor that will be responsible for monitoring the process. This allocation is done in a round-robin manner.

Each program, (a GPSS transaction), is sent to the Memory Manager Level in the form of the first Packet Group. It splits in several packets according

to the value of the function GEN. Each packet of the Packet Group is sent to the Execution Manager Level (Param. No.5= 3). The EP packet of the group searches for the first free EMP available (GATE NU PF1,OSW). This check is provided by the EMS, and if unsuccessful, the EP packet will get routed to the next EMS. After grabbing one EMP, the EP will wait for the rest of the Packet Group to arrive (ASSEMBLE block). Once the Group is complete, execution starts (ADVANCE CPUTM).

When execution of the packet group stops, due to one of the conditions previously mentioned, the original EP packet is routed to the UM level (Parm 5= 0), where the cycle is repeated. The end of the program will occur when the number of packet groups executed is equal to the initially assigned program length plus the accumulated value of the variable SPAWN (PF 15). Table TTIME stores all the values of the turnaround time for each program. Table ETIME stores all the values of the accumulated time that all the Packet Groups of each program spend executing in one EMP. Table NPAC stores all the values of the number of Packet Groups executed per program.

9.3 SIMULATION RESULTS

The first simulation run gives an indication of the variation of average turnaround time as a function of the number of Slices in PACOS. (see Fig. 20). Packet size is fixed at 4 Kbytes. CPTM (EMP processing speed) is fixed at 1 (0.1 MIPS). As indicated in Section 10, Performance Considerations,

the optimum Balance Ratio is obtained when the execution time, ETIME, is 50% of the turnaround time. For an MPL (multiprogramming level) of 10 programs, we notice that this situation occurs when the number of slices is four.

With one Slice, the EMP is constantly busy and packets spend most of the time waiting for the EMP to become free.

With eight and more Slices, most of the time is spent in execution of packets in the EMP. ($ETIME = 0.8 * TTIME$).

The second simulation run (results in Fig 21) gives an indication of the performance that a single-CPU system would provide, using the same load of programs as on the previous run. We simulate this situation by changing the following parameters:

- The inter-nodal delays are reduced to 20 microseconds/packet. (from 400 microseconds on the PACOS machine). This time roughly approximates the register-transfer delays involved in a single-CPU system.
- The memory access time per packet is reduced to 20 microseconds per packet (from 200 microseconds in PACOS). This is based on a memory cycle time of 0.1 microseconds per instruction, which is a typical value for a medium size mainframe. (POH-1, pp. 77-80)
- The speed of the single-slice CPU is increased by factors of 4, 8, 12, 16, 20, 24 and 32.

For CPTM = 4, the turnaround time is worse than having a PACOS machine with

four slices. This situation is caused by packets spending too much time waiting for the CPU to be free. The bottleneck clears up when CPTM is increased to 8. The Balance Ratio, however, still remains too low. ($ETIME = 0.2 * TTIME$)

Finally, Fig. 22 indicates the variation of performance of a single-CPU system versus a PACOS machine with "n", number of Slices. The turnaround time has been kept constant at the optimum level of the simulated PACOS system. ($BR = 0.5$ or $TTIME = 2.5$ secs.), as well as at lower and higher levels of $TTIME$. This chart is a combination of the results obtained on Figs. 20 and 21. The close-to-linear relationship demonstrates that the concept of Packet Execution can effectively provide a solution to the problem of upgrading large, general purpose, single-CPU systems.

The resulting values are consistent (allowing for simulation variances), with the theoretical results obtained in Section 10 (equation 4, Fig. 18).

Fig. 20.- Turnaround time vs. No. of Slices

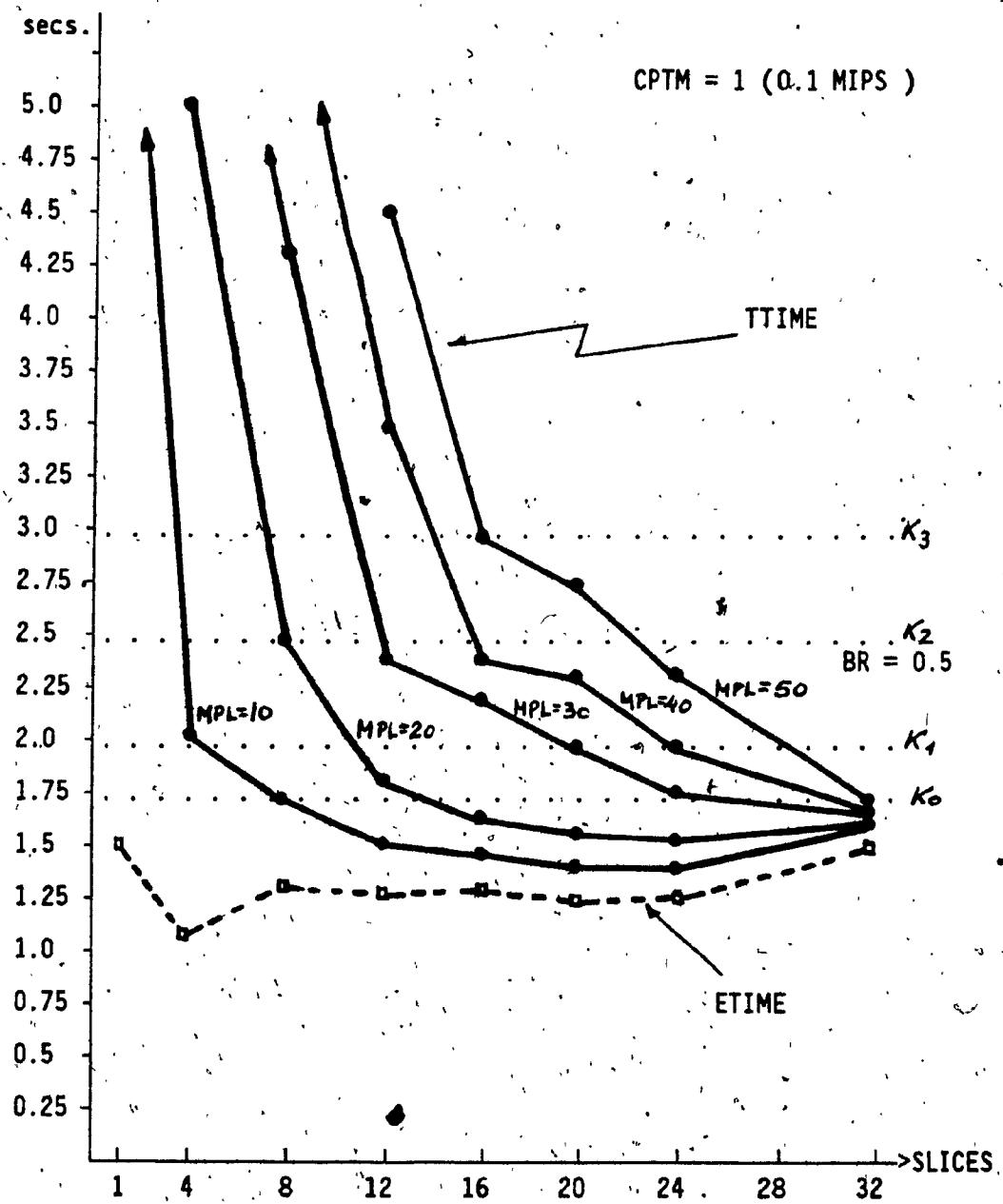


Fig. 21.- Turnaround time vs. EMP processing speed.(One Slice)

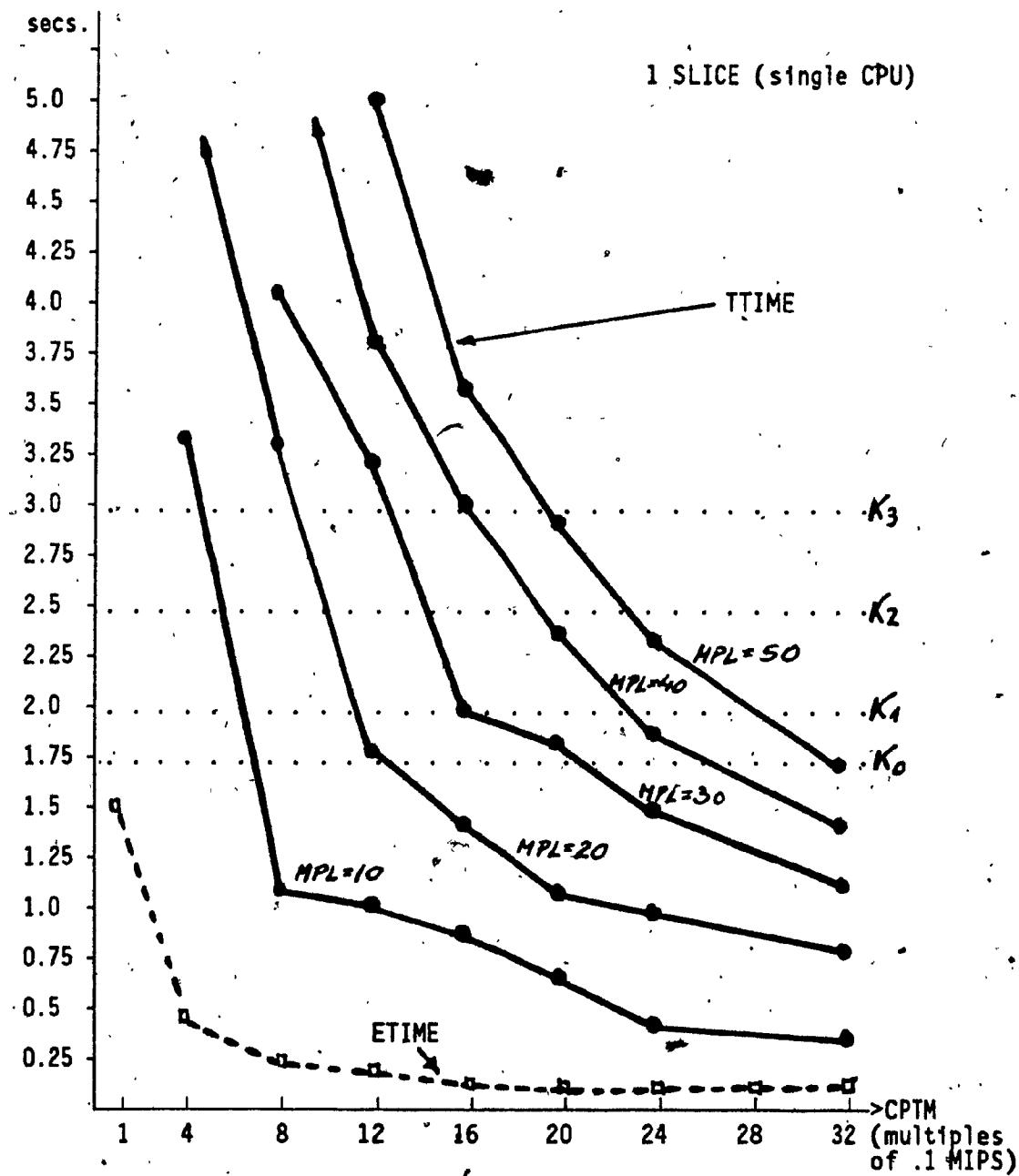
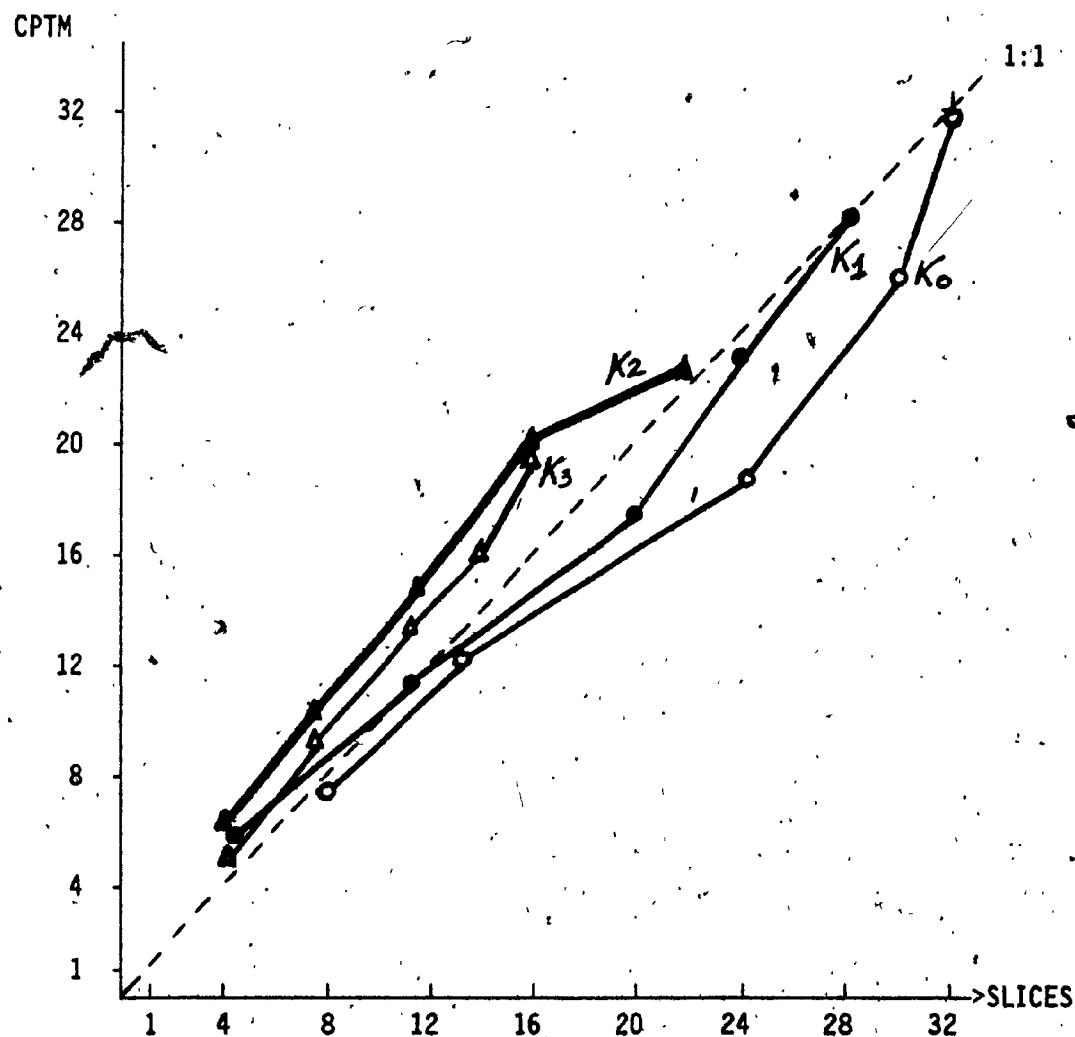


Fig. 22.- SINGLE CPU vs. PACOS.

TTIME = K (see Figs. 20,21)



10.0 CONCLUSION

The concept of Packet Execution attempts to replace a large, single-CPU multiprogramming system with a fully distributed architecture of smaller processors. While multi-processing is today a common approach used in distributing specific tasks, a fully distributed allocation of all tasks to all processors requires partitioning of programs in very specific ways. The Packet Group concept can be a cost-effective solution to the problem of generalizing the distribution of tasks among processors.

Simulation results indicate that the performance of PACOS does not degrade with the addition of subsequent slices. This is due to the multi-path structure of the packet architecture that avoids transmission bottlenecks by routing packets to the next free processor. As a result, the PACOS architecture can offer a very cost-effective solution to the expensive upgrading of heavily-loaded, single-CPU computer system.

The construction of a prototype of PACOS would be a most challenging project, that might open the doors to the replacement of massive and expensive single-CPU computer systems with modular, low-cost microprocessors.

11.0 APPENDICES

11.1 APPENDIX A.- Z-7 INSTRUCTION SET. CELSIUS PROGRAM

The Z7 user language is stack-oriented. There are sixteen different Z7 instructions, varying in length from one to three words. The instructions are:

OP CODE	MNEMONIC AND FORMAT
0	BRANCH <addr1> <addr2>
1	ENTER <addr>
2	RETURN
3	REPEAT
4	EXIT
5	PUSH <value>
6	FETCH
7	STORE
8	ADD
9	SUBSTRACT
10	MULTIPLY
11	DIVIDE
12	STOP
13	GET
14	PUT
15	ALLOCATE <value>

In the paragraphs that follow, the semantics of the various instructions are specified. Instructions with similar functions are grouped together. We use a simple notation to describe the instructions. The variables I and J are registeres local to the CPU. A left arrow (<-) denotes a stack operation. IP is the instruction pointer. STACK_PTR always addresses the word beyond the top of the stack; it is implicitly manipulated by most of the instructions.

ADD: J <- stack; I <- stack; stack <- I+J;
SUBSTRACT: J <- stack; I <- stack; stack <- I-J;
MULTIPLY: J <- stack; I <- stack; stack <- I*J;
DIVIDE: J <- stack; IF J=0 THEN trap 12;
ELSE DO: I <- stack; stack <- I/J; END;

STOP, GET, and PUT each produce traps. In the case of a GET instruction, the CPU places the contents of the IO address on top of the stack. In the case of a PUT instruction, the entry on the top of the stack is placed at the specific address.

STOP: trap 3;
GET: stack <- memory(data segment, IO_ADDR);
PUT: memory(data segment, IO_ADDR) <- stack;

ALLOCATE increases the stack pointer by the amount specified, in order to reserve space for variables. The instruction pointer must be incremented to the word following <value>.

ALLOCATE <value>:
STACK_PTR = STACK_PTR + <value>
IP = IP + 1; /* Bypass <value> */

PUSH, FETCH, and STORE each involve data transfers. PUSH places its operand on the top of the stack. FETCH removes the top entry from the stack, treats it as an address, and places the contents of that address on the top of the stack. STORE removes the entry on the top of the stack and places it at

the address specified by the second entry on the stack.

```
PUSH <value>:  
    stack <- <value>;  
    IP = IP + 1; /* Bypass value */  
FETCH: I <- stack; stack <- memory(data segment, I);  
STORE: J <- stack; I <- stack; memory(data segment, I) = J;
```

ENTER, BRANCH, EXIT, RETURN, and REPEAT affect the flow of control of Z7 programs and are self-explanatory.

11.1.1 JOB CELSIUS

M	EQU	0	VARIABLE M
K	EQU	1	VARIABLE K
I	EQU	2	VARIABLE I
TEMPF	EQU	3	ARRAY TEMPF 20
TEMPC	EQU	23	ARRAY TEMPC 20
INPUT	PUSH	TEMPF	BLOCK INPUT
	PUSH	I	GET TEMPF(I)
	FETCH		
	ADD		
	GET		
	STORE		
	PUSH	I	I=I+1
	PUSH	I	
	FETCH		
	PUSH	1	
	ADD		
	STORE		
	PUSH	M	REPEAT M-I
	FETCH		
	PUSH	I	
	FETCH		
	SUBTRACT		
	REPEAT		
	EXIT		
CONVERT	PUSH	K	END
	PUSH	TEMPF	BLOCK CONVERT
	PUSH	I	K=TEMPF(I)

FETCH		
ADD		
FETCH		
STORE		
PUSH	TEMPC	TEMPC(I)=K-32
PUSH	I	
FETCH		
ADD		
PUSH	K	
FETCH		
PUSH	32	
SUBTRACT		
STORE		
PUSH	TEMPC	TEMPC(I)=TEMPC(I)*5
PUSH	I	
FETCH		
ADD		
PUSH	TEMPC	
PUSH	I	
FETCH		
ADD		
FETCH		
PUSH	5	
MULTIPLY		
STORE		
PUSH	TEMPC	TEMPC(I)=TEMPC(I)/9
PUSH	I	
FETCH		
ADD		
PUSH	TEMPC	
PUSH	I	
FETCH		
ADD		
FETCH		
PUSH	9	
DIVIDE		
STORE		
PUSH	TEMPC	PUT TEMPC(I)
PUSH	I	
FETCH		
ADD		
FETCH		
PUT		
PUSH	I	I=I+1
PUSH	I	
FETCH		
PUSH	1	
ADD		
STORE		
PUSH	M	REPEAT M-I
FETCH		
PUSH	I	
FETCH		
SUBTRACT		
REPEAT		
EXIT		
MAIN		END
PUSH	M	BLOCK MAIN
GET		GET M

STORE	I	I=0
PUSH	0	
PUSH		
STORE		
ENTER	INPUT	ENTER INPUT
PUSH	I	I=0
PUSH	0	
STORE		
ENTER	CONVERT	ENTER CONVERT
EXIT		END
ALLOCATE	43	BEGIN MAIN
ENTER	MAIN	
STOP		

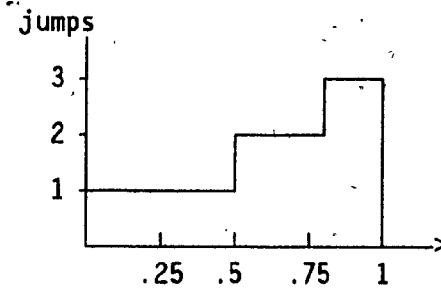
Data:

7 23 45 52 3 75 100 65

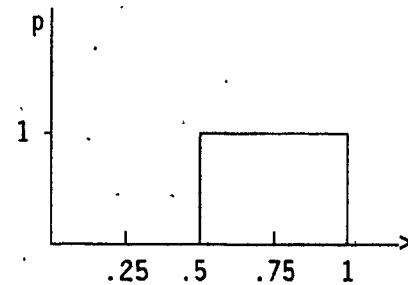
11.2 APPENDIX B.- GPSS SIMULATOR FUNCTIONS.

FUNCTION	DESCRIPTION	STRUCTURE
GEN	Gives the number of packets that will compose a new packet group (EP is not counted).	
PTIME	Execution time of one packet group (1 Kbytes)	
PLEN	Program length in number of packet groups executed.	
CBND	Number of iterations in a local loop. (Loop contained in the same packet)	

LPNO Number of jumps to subroutines or loops located in a different packet.



LPPR Probability of encountering a jump to subroutine or loop located in a different packet.



11.3 APPENDIX C.- GPSS PACOS SIMULATOR PROGRAM.- SAMPLE INPUT/OUTPUT.

CONCORDIA UNIVERSITY OPSL V/6000		CMN OPSL V/6000 VER. 2.0		B4/07/23 08:30:55	
BLOCK NUMBER	LOC	OPERATION	A, B, C, D, E, F, G, H, I, J	COMMENTS	CARD NUMBER
		REALLOCATE	FAC, 1400, GRP, 200, GUE, 1400, STO, 1400		34
		PSIZE	EQU 1,X		1
		SPEED	EQU 2,XXX		2
		PSIZE	EQU 3,XXX		3
		PACB2	EQU 4,XXX		4
		PNO	EQU 5,XXX		5
		LEVX	EQU 6,XXX		6
		MORX	EQU 7,XXX		7
		VERX	EQU 8,XXX		8
		PROX	EQU 9,XXX		9
		GENA	EQU 10,X		10
		CPTH	EQU 11,X		11
		LINK1	VARIABLE PF1-1000		12
		LINK2	VARIABLE VALNK1+400		13
		LEVEL	VARIABLE VALNK1/100		14
		Slice	VARIABLE VALNK1/100		15
		NORM	VARIABLE X1/1000		16
		DEL	VARIABLE XANORM/100		17
		CPUMT	VARIABLE FNMP TIME OF PROCESSOR=1000/X11		18
		SP AIN	VARIABLE FNALPPRREFNCBND=F-NLPLPD=(4-VNORM)		19
		INITIAL	X1, 4000	**** PACKET SIZE IN BYTES ****	20
		INITIAL	X2, 4000	*** SPEED ***	21
		INITIAL	X3, 50	*** SIZE IN PACKETS OF EACH MEMORY MANAGER ***	22
		INITIAL	X4, 4	*** NUMBER OF SLICES ***	23
		INITIAL	X9, 0	*** INITIALLY PROGRAM NO. 0 ***	24
		INITIAL	X11, 1	*** PROCESSING SPEED OF EACH PROCESSOR ***	25
		INITIAL	X12, 1001	*** USER MANAGER NO OF PROGRAM ***	26
		DEFN FUNCTION	RN1, D3	*** NUMBER OF PACKETS THAT FORM A NEW PACKET GROUP ***	27
		PTIME FUNCTION	RN1, D3	*** EXECUTION TIME OF ONE PACKET GROUP ***	28
		: 2, 17, 8, 2, 37, 1, 37			29
		PLEN FUNCTION	RN1, D4	*** PROGRAM LENGTH IN NO OF PKT. GROUPS ***	30
		: 1, 37, 2, 10, 7, 15, /, 8, 20, /, 9, 23, 1, 30,			31
		CMD FUNCTION	RN1, D3	*** NUMBER OF ITERATIONS IN A LOCAL LOOP ***	32
		: 4, 4, 0, 10, 1, 12			33
		LPPR FUNCTION	RN1, D3	*** NUMBER OF JUMPS TO DIFFERENT PACKETS ***	34
		: 5, 5, 0, 2, 1, 3, /			35
		LPPR FUNCTION	RN1, D2	*** PROB. OF FINDING A JUMP TO SURN. IN DIFFERENT PACKET ***	36
		: 5, 0, 1, 1,			37
		NEXTIP FUNCTION	RN1, D2	*** PROBABILITY OF PACKET GROUP FAULT IN MN ***	38
		: 7, 0, 1, 1,			39
		GENERATE MARK	7000, . 1, 20, . 26, F	*** GEN PROS. ONE EVERY 7 MSEC'S *** *** TURNAROUND TIME CLOCK STARTS ***	40
					41
					42
					43
					44
					45
					46
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					48
					49
					50
					51
					52
					53
					54

CONCORDIA UNIVERSITY. OPS6 V/6000				CRM OPS6 V/6000 VER. 2.0	84/07/23. 08 30. 55.
BLOCK NUMBER	BLDC	OPERATION	A, B, C, D, E, F, G, H, I, J	COMMENTS	CARD NUMBER
24		ASSIGN ASSIGN	1, X12 16, X12	** ABSION UMP PROCESSOR ** ABSION UMP PROGRAM CREATOR	55
25	TEST	UPLIST SAVE VALUE TRANSFER	1, VOL1NC 12, X12 12, X12-X4	** UPLIST VOL1NC ** INCREASE UMP NO BY ONE	56
26	UPLST	ULAST SAVE VALUE TRANSFER	1, VOL1NC 12, X12 12, X12-X4	** BACK TO FIRST SLICE ***	57
27	UREXT	UREXT SAVE VALUE ASSIGN	1, VOL1NC 12, X12 12, X12-X4	** NEW PROGRAM NUMBER ** ** SET ASSEMBLY GROUP NUMBER **	58
28	10	ASSIGN ASSIGN	1, VOL1NC 12, X12	** DESTINATION LEVEL - MH **	59
29	11	ASSIGN ASSIGN	1, VOL1NC 12, X12	** CONTROL COMMAND TO SET ** PACKET TYPE - EP	60
30	12	ASSIGN ASSIGN	1, VOL1NC 12, X12	** SET LOOP LINK NO **	61
31	13	ASSIGN ASSIGN	1, VOL1NC 12, X12	** SET SLICE LINK NO **	62
32	14	ASSIGN ASSIGN	1, VOL1NC 12, X12	** INITIALIZE PROGRAM LENGTH **	63
33	15	ASSIGN ASSIGN	1, VOL1NC 12, X12	** ASSIGN BASIC PROGRAM LENGTH **	64
34	16	ASSIGN ASSIGN	1, VOL1NC 12, X12	** INITIALIZE EXEC TIME COUNTER **	65
35	17	ASSIGN ASSIGN	1, VOL1NC 12, X12		66
36	18	ASSIGN ASSIGN	1, VOL1NC 12, X12		67
37	19	ASSIGN ASSIGN	1, VOL1NC 12, X12		68
38	20	DEVEL TEST E GRIND TEST NE TEST NE TEST NE	PF10 PF10 PF10 PF10	** DEVEL TEST E ** GRIND TEST NE ** TEST NE ** TEST NE	69
39	21	DEVEL TEST NE TEST NE TEST NE TEST NE	PF10 PF10 PF10 PF10	** DEVEL TEST NE ** TEST NE ** TEST NE ** TEST NE	70
40	22	DEVEL TEST NE TEST NE TEST NE TEST NE	PF10 PF10 PF10 PF10	** DEVEL TEST NE ** TEST NE ** TEST NE ** TEST NE	71
41	23	DEVEL TEST NE TEST NE TEST NE TEST NE	PF10 PF10 PF10 PF10	** DEVEL TEST NE ** TEST NE ** TEST NE ** TEST NE	72
42	24	DEVEL TEST NE TEST NE TEST NE TEST NE	PF10 PF10 PF10 PF10	** DEVEL TEST NE ** TEST NE ** TEST NE ** TEST NE	73
43	25	DEVEL SEIZE TRANSFER	PF10 PF9	** DEVEL SEIZE ** TRANSFER	74
44	26	DEVM SEIZE	PF9	** DEST IS ANOTHER SLICE ** GRAB LOOP LINK TO GO TO OTHER SWITCH ***	75
45	27	DEVM TRANSFER	AR1NO	** INTRA-NODAL DELAY ** ** LOOP LINK 16 RELEASED ***	76
46	28	AR1NO ADVANCE RELEASE DEPART	AR1NO V6DEL PF9 PF9	** AR1NO ** V6DEL ** PF9 ** PF9	77
47	29	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11	** IS THIS THE LAST SLICE ** ** INCREASE PROCESSOR NO. ** ** NEW LOOP LINK NO ** ** NEW SLICE LINK NO. ***	78
48	30	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		79
49	31	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		80
50	32	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		81
51	33	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		82
52	34	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		83
53	35	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		84
54	36	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		85
55	37	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		86
56	38	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		87
57	39	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		88
58	40	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		89
59	41	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		90
60	42	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		91
61	43	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		92
62	44	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		93
63	45	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		94
64	46	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		95
65	47	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		96
66	48	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		97
67	49	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		98
68	50	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		99
69	51	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		100
70	52	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		101
71	53	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		102
72	54	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		103
73	55	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		104
74	56	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		105
75	57	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		106
76	58	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		107
77	59	TEST O UPLIST SAVE VALUE ASSIGN	X4, VOL1NC PF11 PF11 PF11		108

CONCORDIA UNIVERSITY. OPSYS V/6000				CRTPSS V/6000 VER. 2.0	84/07/23. 08 30 55.
BLOCK NUMBER	BLDC	OPERATION	A, B, C, D, E, F, G, H, I, J	COMMENTS	CARD NUMBER
93		ASSIGN	11+, 1 X10, NEXT	** INCREASE NUMBER OF PACKETS BY ONE (EP) **	165
94		SPLIT	PF2	** GENERATE PACKET GROUP **	166
95		JOIN	5,3	** BELONG TO SAME ASSEMBLY SET **	167
96		ASSIGN	.CLEVL	** DEST- EN LEVEL **	168
97		TRANSFER	PF2		169
98		NEXT	JOIN		170
99		ASSIGN	5,3		171
100		ASSIGN	7,2	** THESE PACKETS ARE IP, DP, PACKETS **	172
101		TRANSFER	.CLEVL		173
102		STORE ENTER	PF1	** ACCESS MAIN MEMORY **	174
103		ADVANCE	K20	** STORAGE AND UPDATE OF TABLES **	175
104		LEAVE	PF1		176
105		TERMINATE			177
106		EXECUTION "MANAGER" LEVEL			178
107		TEST E	PF5, 3, OLEV	** CHECK FOR EM LEVEL **	179
108		TEST E	PF7, 1, OTHER	** CHECK FOR EP PACKET **	180
109		DATE NU	PF1, DBW	** IF EP IS IN USE, GO TO GET ANOTHER **	181
110		DATE NU	PF1	** ELSE, GET THIS EP **	182
111		SEIZE	PF1		183
112		TRANFER	PF2	** SET CONTROL SWITCH **	184
113		OTHER	PF2, DLV	** IF SWITCH NOT SET, WAIT A LITTLE **	185
114		DATE LS	PF2, DLV		186
115		ADVANCE	VDEI,	** WAIT BEFORE LOOKING FOR THE EP **	187
116		TRANSFER	DBW		188
117		GRP	REMOVE	** GATHER ALL THE MEMBERS OF THE PKT.GRP **	189
118		ASSEMBLE	PF1,1	** CANCEL GROUP NUMBER **	190
119		LOGIC R	PF2	** RESET SWITCH **	191
120		MARK	14	** COUNTS BEGINNING OF EXECUTION **	192
121		ADVANCE	VSCPUTH	** PKT.GRP EXECUTES IN EMP **	193
122		ASSIGN	15+, VSCPAM	** INCREASE PROGRAM LENGTH **	194
123		RELEASE	PF1		195
124		DEPART			196
125		TEST L	17+, TPI4	** ACCUMULATES EXEC TIME PER PROGRAM **	197
126		ASSIGN	12+, 1	** COUNTING PACKET GROUPS **	198
127		TEST L	PF12, PF13, OUT	** IF LIMIT REACHED, PROGRAM ENDS - **	199
128		TEST L	PF12, 50, OUT	** NO MORE THAN 50 PACKET GROUPS **	200
129		ASSIGN	2,0	** DESTINATION=USER MANAGER LEVEL **	201
130		ASSIGN	7,1	** PACKET TYPE = EP **	202
131		ASSIGN	6,2	** COMMAND= UPDATE **	203
132		TRANSFER	.OLEV		204
133	OUT	TABULATE	ETIME	** TURNAROUND TIME PER PROGRAM **	205
134		TABULATE	NPAC	** EXEC TIME PER PROGRAM **	206
135		TTIME TABLE	HP13, 0, 100, 20	** NUMBER OF PACKET GROUPS PER PROGRAM **	207

CONCORDIA UNIVERSITY. OPSS V/6000 CRM OPSS V/2000 VER. 2.0
 BLOCK NUMBER 8LOC OPERATION A,B,C,D,E,F,G,H,I,J
 3 ETIME TABLE PF17,0,100,20
 MAC TABLE PF12,0,5,8
 TERMINATE T

REPEAT X4,1
 REPORT ONE POLICE ***
 FAC TITLE FACILITIES
 TAB INCLUDE TABLES
 ENDREPORT T1-T471.2,3,4
 START 20,...,POLICE
 CLEAN X1-X3,X11-X12
 INITIAL X4,4
 START 20,...,POLICE
 CLEAN X1-X3,X11-X12
 INITIAL X4,8
 START 20,...,POLICE
 FOUR SLICES ***
 EIGHT SLICES ***

CONCORDIA UNIVERSITY OPBS V/4000		CRN OPSBS V/4000 VER. 2.0		84/07/23 08:32:55.	
FACILITY	AVERAGE UTILIZATION	NUMBER ENTRIES	AVERAGE TIME/TRAN	SELLING TRANS NO.	PREEMPTING TRANS NO.
010	0.010	125	400 000	100-13698	112
		112	400 000	110-13698	100
		100	400 000	111-13698	101
		100	400 000	111-13698	102
		100	400 000	111-13698	103
		100	400 000	111-13698	104
		100	400 000	111-13698	105
		100	400 000	111-13698	106
		100	400 000	111-13698	107
		100	400 000	111-13698	108
		100	400 000	111-13698	109
		100	400 000	111-13698	110
		100	400 000	111-13698	111
		100	400 000	111-13698	112
		100	400 000	111-13698	113
		100	400 000	111-13698	114
		100	400 000	111-13698	115
		100	400 000	111-13698	116
		100	400 000	111-13698	117
		100	400 000	111-13698	118
		100	400 000	111-13698	119
		100	400 000	111-13698	120
		100	400 000	111-13698	121
		100	400 000	111-13698	122
		100	400 000	111-13698	123
		100	400 000	111-13698	124
		100	400 000	111-13698	125
		100	400 000	111-13698	126
		100	400 000	111-13698	127
		100	400 000	111-13698	128
		100	400 000	111-13698	129
		100	400 000	111-13698	130
		100	400 000	111-13698	131
		100	400 000	111-13698	132
		100	400 000	111-13698	133
		100	400 000	111-13698	134
		100	400 000	111-13698	135
		100	400 000	111-13698	136
		100	400 000	111-13698	137
		100	400 000	111-13698	138
		100	400 000	111-13698	139
		100	400 000	111-13698	140
		100	400 000	111-13698	141
		100	400 000	111-13698	142
		100	400 000	111-13698	143
		100	400 000	111-13698	144
		100	400 000	111-13698	145
		100	400 000	111-13698	146
		100	400 000	111-13698	147
		100	400 000	111-13698	148
		100	400 000	111-13698	149
		100	400 000	111-13698	150
		100	400 000	111-13698	151
		100	400 000	111-13698	152
		100	400 000	111-13698	153
		100	400 000	111-13698	154
		100	400 000	111-13698	155
		100	400 000	111-13698	156
		100	400 000	111-13698	157
		100	400 000	111-13698	158
		100	400 000	111-13698	159
		100	400 000	111-13698	160
		100	400 000	111-13698	161
		100	400 000	111-13698	162
		100	400 000	111-13698	163
		100	400 000	111-13698	164
		100	400 000	111-13698	165
		100	400 000	111-13698	166
		100	400 000	111-13698	167
		100	400 000	111-13698	168
		100	400 000	111-13698	169
		100	400 000	111-13698	170
		100	400 000	111-13698	171
		100	400 000	111-13698	172
		100	400 000	111-13698	173
		100	400 000	111-13698	174
		100	400 000	111-13698	175
		100	400 000	111-13698	176
		100	400 000	111-13698	177
		100	400 000	111-13698	178
		100	400 000	111-13698	179
		100	400 000	111-13698	180
		100	400 000	111-13698	181
		100	400 000	111-13698	182
		100	400 000	111-13698	183
		100	400 000	111-13698	184
		100	400 000	111-13698	185
		100	400 000	111-13698	186
		100	400 000	111-13698	187
		100	400 000	111-13698	188
		100	400 000	111-13698	189
		100	400 000	111-13698	190
		100	400 000	111-13698	191
		100	400 000	111-13698	192
		100	400 000	111-13698	193
		100	400 000	111-13698	194
		100	400 000	111-13698	195
		100	400 000	111-13698	196
		100	400 000	111-13698	197
		100	400 000	111-13698	198
		100	400 000	111-13698	199
		100	400 000	111-13698	200

CONCORDIA UNIVERSITY OPSIS V/6000			CRM OPSIS V/6000 VER 2.0	PREEMPTING BEI 11 NO TRANS NO.	84/07/23. 08.32.55.
FACILITY	AVERAGE UTILIZATION	NUMBER ENTRIES	AVERAGE TIME/TRAN	TIME/TRAN	
1008	0.000	4	20.000	20.000	
1101	0.054	1	20000	20000	
1102	0.067	1	20000	20000	
1103	0.054	1	20000	20000	
1104	0.036	1	20000	20000	
1105	0.045	1	20000	20000	
1106	0.031	1	20000	20000	
1107	0.031	1	20000	20000	
1108	0.063	1	20000	20000	
1201	0.003	1	20000	20000	
1202	0.003	1	20000	20000	
1203	0.002	1	20000	20000	
1204	0.002	1	20000	20000	
1205	0.001	1	20000	20000	
1206	0.001	1	20000	20000	
1207	0.002	1	20000	20000	
1208	0.002	1	20000	20000	
1301	7.63	1	87.911	79.793	
1302	8.23	1	87.911	108.149	
1303	7.23	1	87.911	77.786	
1304	7.34	1	87.911	66.7	
1305	8.04	1	87.911	81.068	
1306	7.84	1	87.911	83.525	
1307	7.31	1	87.911	79.793	
1308	9.77	1	87.911	103.229	
TABLETTIME ENTRIES IN TABLE			MEAN ARGUMENT	STANDARD DEVIATION	
20		3011854.000		693222.905	
TABLETTIME ENTRIES IN TABLE			MEAN ARGUMENT	STANDARD DEVIATION	
20		1449600.000		331757.402	
TABLETNPAC ENTRIES IN TABLE			MEAN ARGUMENT	STANDARD DEVIATION	
20		16.000		5.992	
CLEAR INITIAL START			X1-X3, X11-X12 X4-X12 20...POLICE	1212 1213 1214 1215	

CONCORDIA UNIVERSITY OPSS V/6000

AVERAGE UTILIZATION

NUMBER ENTRIES

CRM OPSYS V/6000 VER 2.0

AVERAGE TIME/TRAN

PREEMPTING TRANS NO.

APPENDICES

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APPENDICES

CONCORDIA UNIVERSITY OP85 V/4000 **AVERAGE NUMBER OF ENTRIES** **CRM OPS V/4000 VER. 2.0 PREENTING TRANS NO.**

FACILITY UTILIZATION	NUMBER OF ENTRIES	AVERAGE TIME/TRAN	TIME/TRAN
1304	345	24	77358.333
1305	534	36	70557.692
1306	594	37	73066.667
1307	595	20	94718.000
1308	595	34	93897.000
1309	772	20	73459.412
1310	220	23	80072.174
1311	636	27	79101.481
1312	636	21	104587.619

TABLE #1 TIME ENTRIES IN TABLE **MEAN ARGUMENT** **STANDARD DEVIATION**

20	MEAN ARGUMENT	STANDARD DEVIATION
20	1293400.000	593886.637

TABLE #2 TIME ENTRIES IN TABLE **MEAN ARGUMENT** **STANDARD DEVIATION**

20	MEAN ARGUMENT	STANDARD DEVIATION
20	13.500	6.048

CLEAR INITIAL START **X1-X3, X11-X12** **** SIXTEEN SLICES ****

X4, 16, 20, . . . , POLICE	246
	247
	248
	249
	250
	251

SACRAMENTO STATE UNIVERSITY. OPS: V-6000
FACILITIES FACILITY AVERAGE UTILIZATION

CRM GPS V/4000 VER. 2.0
AVERAGE BEIZING PREEMPTIVE
TIME/TRANZ TRANS NO.
TRANZ NO.

84/07/23. 08 26. 31.

87

89

CONCORDIA UNIVERSITY <OPSS V/4000
ENTRIES IN TABLE> MEAN ARGUMENT

20 1467200.000

CRM OPSYS V/4000 VER. 2.0
STANDARD DEVIATION

529725.410

TABLE N_{AC}
ENTRIES IN TABLE

MEAN ARGUMENT

20

17.250

STANDARD DEVIATION

5.955

CLEAR X1-X13, X111-X12
INITIAL X4-X6
START X0, PINE, ICE

APPENDICES

CONCORDIA UNIVERSITY		OPSS V/6000	NUMBER ENTRIES	CNN OPSS, V/6000 VEN. SEIZING TRANS NO.	AVERAGE TIME/TRAN	2.0 PREEMPTING TRANS NO.	84/07/23 . 08:37:01.
616	617	618	619	620	621	622	623
702	703	704	705	706	707	708	709
709	710	711	712	713	714	715	716
716	717	718	719	720	721	722	723
723	724	725	726	727	728	729	730
730	731	732	733	734	735	736	737
737	738	739	740	741	742	743	744
744	745	746	747	748	749	750	751
751	752	753	754	755	756	757	758
758	759	760	761	762	763	764	765
765	766	767	768	769	770	771	772
772	773	774	775	776	777	778	779
779	780	781	782	783	784	785	786
786	787	788	789	790	791	792	793
793	794	795	796	797	798	799	800
799	801	802	803	804	805	806	807
807	808	809	810	811	812	813	814
814	815	816	817	818	819	820	821
821	822	823	824	825	826	827	828
828	829	830	831	832	833	834	835
835	836	837	838	839	840	841	842
842	843	844	845	846	847	848	849
849	850	851	852	853	854	855	856
856	857	858	859	860	861	862	863
863	864	865	866	867	868	869	870
870	871	872	873	874	875	876	877
877	878	879	880	881	882	883	884
884	885	886	887	888	889	890	891
891	892	893	894	895	896	897	898
898	899	900	901	902	903	904	905
905	906	907	908	909	910	911	912
912	913	914	915	916	917	918	919
919	920	921	922	923	924	925	926
926	927	928	929	930	931	932	933
933	934	935	936	937	938	939	940
940	941	942	943	944	945	946	947
947	948	949	950	951	952	953	954
954	955	956	957	958	959	960	961
961	962	963	964	965	966	967	968
968	969	970	971	972	973	974	975
975	976	977	978	979	980	981	982
982	983	984	985	986	987	988	989
989	990	991	992	993	994	995	996
996	997	998	999	999	999	999	999

CONCORDIA UNIVERSITY con

TABLE ETIME
ENTRIES IN TIME

1747520.00
BETWEEN
STATEMENT OF EXPENSES
AND STATEMENT OF REVENUE
670103.616

93

CONCORDIA UNIVERSITY 9888 9/6000
FACILITIES **AVERAGE**
FACILITY **EXTRA**

CRM OPS5 V/6000 VER. 2.0
NUMBER ENTRIES AVERAGE TIME/TRAN SEIZING TRAN. PREEMPTING TRANS. NO.

CRM OPSS V/6000 VER. 2.0 04/07/23. 08.37.20.

APPENDICES

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APPENDICES

CONCORDIA UNIVERSITY, OPSIS V/4000 CONCORDIA UNIVERSITY, OPSIS V/4000 06/07/23 09:37:21

APPENDICES

TABLES	TABLE TIME ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
1324	0.431	20	88920.000

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94/07/23 08:37:2

CONCORDIA UNIVERSITY OPSS V/6000 MEAN ARGUMENT CRM OPSS V/6000 VER. 2.0

ENTRIES IN TABLE 20 CRM STANDARD DEVIATION

17000000.0000

TABLE MPAC ENTRIES IN TABLE

MEAN ARGUMENT

19.500

20

END

264
265

Powers

CONCORDIA UNIVERSITY. QPS5 V/6000
 BLOCK NUMBER. #LDC OPERATION A,B,C,D,E,F,G,H,I,J COMMENTS
 2 ETIME TABLE PF17.0..100.20 ** EXEC TIME PER PROGRAM **
 NPAC TABLE PF12.0..5.6 ** NUMBER OF PACKET GROUPS PER PROGRAM **

RESET	X4.1	
INITIAL	X11.4	** CPU SPEED IS 0.4 MIPS **
REPORT	PPQDFR	
FAC TITLE	FACTLITIES	
TAB TITLE	TABLES	
INCLUDE	T1-T4/1,2,3,4	
ENDREPORT		
START	20...PPQDFR	

APPENDICES.

CONCORDIA UNIVERSITY OPSYS V/4000	AVERAGE UTILIZATION	NUMBER ENTRIES	CMM OPSYS V/4000 VER. 2.0	SEIZING TRANS NO.	PREEPTING TRANS NO.
1.61	0.947	390848	20.000		
1.01	0.002	390700	20.000		
1.21	0.001	449	20.000		
1.41	0.002	869	20.000		
1.61	0.001	340	20.000		
2.01	0.001	340	20.000		
2.21	0.219	588	20000		
2.41	0.001	340	20.000		
2.61	1.000	360	22348	444	

TABLES
TABLE ETIME
ENTRIES IN TABLE

TABLE ETIME ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
20	6315039.000	1224427.001

TABLE MPAC ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
20	378400.000	167464.183

TABLE MPAC ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
20	16.000	6.266
INITIAL	X1-X5,X12	CPU SPEED IS 0.9 MIPS
START	20...PPOWER	233
		237
		238

CONCORDIA UNIVERSITY. OPSIS V/6000

FACILITIES **AVERAGE** **CRM OPSIS V/6000 VER. -2.0**
UTILIZATION **NUMBER** **PREEMPTING**
ENTRIES **ENTRIES** **TRANS NO.**

61	0.961	194577	20.000
101	0.003	700	20.000
121	0.002	639	20.000
141	0.004	653	20.000
161	0.002	340	20.000
201	0.002	340	20.000
221	0.390	79	20.000
241	0.002	360	20.000
261	1.000	340	1124.222

**TABLES FAPC TIME
ENTRIES IN TABLE**

20 MEAN ARGUMENT

3200928.000

MEAN ARGUMENT

524327.542

**TABLE FETINE
ENTRIES IN TABLE**

20 MEAN ARGUMENT

329750.000

MEAN ARGUMENT

529758.400

**TABLE MPAC
ENTRIES IN TABLE**

20 MEAN ARGUMENT

18.000

STANDARD DEVIATION

3.712

239

210

241

242

CONCORDIA UNIVERSITY OPSS V/4000			CRM OPSS V/4000 VER. 2.0		
AVERAGE UTILIZATION		NUMBER ENTRIES	AVERAGE TIME/TRAN	SEIZING TRANS NO.	PREEMPTING TRANS NO.
41	0.938	114058	20.000		
101	0.005	449	20.000		
141	0.003	421	20.000		
161	0.007	817	20.000		
201	0.003	320	20.000		
221	0.003	320	20.000		
241	0.003	82	19.359	183	3333
241	1.000	340	20.000		
241	1.000	340	72.7	429	

TABLE ETIME ENTRIES IN TABLE			MEAN ARGUMENT	STANDARD DEVIATION
20			1824221.750	415431.996

TABLE MPAC ENTRIES IN TABLE			MEAN ARGUMENT	STANDARD DEVIATION
20			1202111.100	41165.063

CLEARN INITIATI START			11-16 X112	CPU SPEED IS 1.6 MIPS
20	...PPMER	20		243

CONCORDIA UNIVERSITY. QPS5 V/4000
FACILITIES UTILIZATION AVERAGE NUMBER
ENTRIES TIME SPAN PREEMPTING
TIME 121 NO. FRAME NO.

41	0.957	04491	20.000	
101	0.007	670	20.000	
121	0.004	440	20.000	
141	0.003	831	20.000	
161	0.003	325	20.000	
201	0.003	325	20.000	
221	0.970	19999	687	3343
241	0.003	345	20.000	
261	1.000	5734	493	

TABLES
ENTRIES IN TABLE

20 MEAN ARGUMENT
1330124.500

TABLES
ENTRIES IN TABLE

20 MEAN ARGUMENT
99937.900

TABLES
ENTRIES IN TABLE

20 MEAN ARGUMENT
17.250

INITIAL 11-14-X12
START 20...PPOWER ** CPU SPEED IS 2.0 MIPS ..

247
248
249
250

CONCORDIA UNIVERSITY. GPSS V/4000 CRM GPSS V/4000 VER. 2.0
FACILITY UTILIZATION AVERAGE NUMBER OF ENTRIES AVERAGE TIME/TRAN SEIZING NO. PREEMPT NO. TRANS NO.

61	0.930	65395	20.000		
101	0.009	610	20.000		
121	0.011	384	20.000		
141	0.004	742	20.000		
161	0.004	295	20.000		
201	0.004	295	20.000		
221	0.996	70	1997.429		
241	0.004	315	20.000		
261	1.000	315	4462.095		

TABLES TABLETTING ENTRIES IN TABLE

20	1037340.000	STANDARD DEVIATION	389308.926
TABLE ETIME ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION	
20	67190.000	STANDARD DEVIATION	30439.273

TABLE NPAC ENTRIES IN TABLE

20	15.790	STANDARD DEVIATION	6.939
CLEAR INITIAL START	X1-X4, X12 X1, 24, PPQ, ER 20,...,PPQ, ER	** CPU SPEED IS 2.4 MIPS **	
20			251

CONCORDIA UNIVERSITY OPSS V740000 CRM OPSS V/4000 VER. 2.0 84/07/23. 04 59. 20

FACILITY	AVERAGE UTILIZATION	NUMBER ENTRIES	AVERAGE TIME/TRAN	SEIZING IND.	PREEMPTING TRANS NO.
61	0. 967	70635	20. 000		
101	0. 006	720	20. 000		
121	0. 006	642	20. 000		
141	0. 012	911	20. 000		
161	0. 005	350	20. 000		
201	0. 005	350	20. 000		
221	0. 005	373	19809. 726		
241	0. 005	370	20. 000		
261	1. 000	370	3945. 773		
TABLE TIME ENTRIES IN TABLE					
			MEAN ARGUMENT	STANDARD DEVIATION	
	20		1042500. 600	287442. 384	
TABLE ETIME ENTRIES IN TABLE					
			MEAN ARGUMENT	STANDARD DEVIATION	
	20		88791. 430	31021. 374	
TABLE MPAC ENTRIES IN TABLE					
			MEAN ARGUMENT	STANDARD DEVIATION	
	20	10. 300	10. 708	6. 708	
			END	234	237

APPENDICES

CONCORDIA UNIVERSITY OPS6 V/6000

BLOCK NUMBER	LOC	OPERATION	A, B, C, D, E, F, G, H, I, J	COMMENTS	CARD NUMBER
2		ETIME TABLE	PF17, 0, 100, 20	** EXEC TIME PER PROGRAM **	220
		NPACK TABLE	PF12, 0, 5, 8	** NUMBER OF PACKET GROUPS PER PROGRAM **	221
3	125	TERMINATE			222

PPOWER

		CRM OPS6 V/6000 VER. 2.0	MPL = 50	84/07/30 16.03.1
RESET				
INITIAL	X4,1.	** CPU SPEED IS 0.4 MIPS **		
INITIAL	X11,4.			
REPORT	PPOWER			
FAC	FACILITIES			
TITLE	TABLES			
TAB	INCLUDE T1-T4/1,2,3,4			
TAB	ENDREPORT			
START	30,...,PPOWER			
CLEAR	X1-X4, X12	** CPU SPEED IS 0.8 MIPS **		
INITIAL	X11,8			
START	30,...,PPOWER			

APPENDICES

CONCORDIA UNIVERSITY		GPSS V/6000		CRM GPSS V/6000 VER 2.0		84/07/30 18:57:11	
FACILITIES	AVERAGE UTILIZATION	ENTRIES	AVERAGE TIME/TRAN	BEZING TRANS NO.	PREEPTING TRANS NO.		
61	0.995	448460	20 000				
101	0.004	1650	20 000				
124	0.003	1884	20 000				
141	0.004	2026	20 000				
161	0.002	800	20 000				
201	0.002	800	20 000				
221	0.497	234	20000	000			
241	0.202	850	20 000				
261	1.040	850	11000	793			
TABLES		MEAN ARGUMENT		STANDARD DEVIATION			
ENTRIES IN TABLE		7532126.400		1782297.167			
TABLE ETIME		MEAN ARGUMENT		STANDARD DEVIATION			
ENTRIES IN TABLE		178670.000		64062.439			
TABLE NPAC		MEAN ARGUMENT		STANDARD DEVIATION			
ENTRIES IN TABLE		50		6.308			
TABLE ETIME		17.000		6.308			
INITIAL		X1-X4-X12		CPU SPEED 16 1.2 MIPS			
START		X11-X12		PPDMER			
		50...		239			
		50...		240			
		50...		241			
		50...		242			

CONCORDIA UNIVERSITY' OPSS V/6000		CRM OPSS V/6000 VER. 2.0	
FACILITIES	AVERAGE UTILIZATION	NUMBER ENTRIES	AVERAGE TIME/TRAN
61	0.989	319546	20.000
101	0.003	1620	20.000
131	0.003	679	20.000
141	0.006	2031	20.000
161	0.002	790	20.000
201	0.002	231	1476.3
211	0.714	840	20.000
221	0.003	840	7689.451
261	1.000		

TABLE NPAC ENTRIES IN TABLE

MEAN ARGUMENT		STANDARD DEVIATION	
50	4947884.040	11224021.803	

TABLE ETIME ENTRIES IN TABLE		MEAN ARGUMENT		STANDARD DEVIATION	
50	120144.400	50	16.800	6.682	

TABLE NPAC ENTRIES IN TABLE		MEAN ARGUMENT		STANDARD DEVIATION	
50	120144.400	50	16.800	6.682	

CLEAR N1-N4-NH3		INITIAL X11,16		CPU SPEED IS 1.6 MIPS **	
START	50	16.800	16.800	243	243
				243	243
				243	243
				243	243

CONCORDIA UNIVERSITY. OPSS V/6000	FACILITIES	AVERAGE FACILITY	NUMBER ENTRIES	CRM OPS5 V/6000 VER 2 0	AVERAGE TIME/TRAN	SEIZING TRANS NO.	PREEPTING TRANS NO.
61	0.983	233789	20000	101	0.006	1150	20000

TABLES	TABLE	TABLE
121	1025	20000
141	1890	20000
161	750	20000
201	750	1946
221	226	681
241	800	20000
261	800	5950
	1	162

TABLE #	AC ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
ETIME	50	3544177.200	950114.442
ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION	
50	82390.000	39982.739	

247
248
249
250

CONCORDIA UNIVERSITY GPSS V/6000			CRM,GPSS V/6000 VER 2.0	84/07/30. 20:4
FACILITY UTILIZATION	AVERAGE NUMBER ENTRIES	AVERAGE TIME/TRAN	PREEMPTING TRANS NO.	
61	0.983	196874	20 000	
101	0.008	1530	20 000	
131	0.006	1987	20 000	
141	0.010	1924	20 000	
161	0.004	740	20 000	
201	0.004	740	20 000	
221	0.004	197	20000	
241	0.004	790	20 000	
261	1.000	790	3069 215	
TABLES TIME ENTRIES IN TABLE				
	30	MEAN ARGUMENT 29322724.000	STANDARD DEVIATION 781452.235	
TABLE ETIME ENTRIES IN TABLE				
	30	MEAN ARGUMENT 21644.000	STANDARD DEVIATION 33396.869	
TABLE NPAC ENTRIES IN TABLE				
	30	MEAN ARGUMENT 15.000	STANDARD DEVIATION 6.256	
				251
				252
				253
				254
				255
CLEAR INITIAL START				
		X1-X4,X12 X11-24 30,...,PPOWER	** CPU SPEED IS 2.4 MIPS **	

CONCORDIA UNIVERSITY OPSS V/6000
FACILITIES FACILITY AVERAGE UTILIZATION NUMBER ENTRIES

	AVERAGE UTILIZATION	NUMBER ENTRIES	AVERAGE TIME/TRAN	BEIZING TRANS NO.	PREEMPTING TRANS NO.	64/07/30 20:37:31
61	0.988	198563	20.000			
101	0.010	1610	20.000			
121	0.006	169	20.000			
141	0.012	1961	20.000			
161	0.005	780	20.000			
201	0.005	780	20.000			
221	0.997	160	19.997	262		
241	0.005	830	20.000			
261	1.000	830	38.64	964		

TABLE #1 TIME ENTRIES IN TABLE

TABLE #1 TIME ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
50	2072089.240	730287.875

TABLE #2 TIME ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
50	87334.860	29357.497

TABLE #3 AC ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION
50	16.600	7.918

	MEAN ARGUMENT	STANDARD DEVIATION
END		236 2.67

PPD 14 = 50 SC 14 = 3:2 N/P 5

HPL = 50 ~~PROBE R~~ CRM QSS V/6000 VER 200 CPDN = 3:2 NIPS 84/08/21 22.14.17.

CONCORDIA UNIVERSITY - OPSS V/6000

AVERAGE TIME/TRAN	SEIZING TRANS NO.	PREEMPT INC TRANS NO.
20.000		
20.000		
20.000		
20.000		
20.000		
20.000		
20.000		
20.000		
19925.430		4564
20.000		
20.000		
20.000		

3032.712	STANDARD DEVIATION 911762.282	STANDARD DEVIATION 21673.419
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STANDARD DEVIATION **6.999** **260**
 261

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CONCORDIA UNIVERSITY computer

APPENDICES

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