

DESIGN AND CONSTRUCTION OF A
SINGLE PHASE MODIFIED MCMURRAY INVERTER.

Dilip Mukhedkar

A Dissertation
in
The Department
of
Electrical Engineering

Presented in Partial Fulfillment of the Requirements
for the degree of Master of Engineering at
Concordia University
Montreal, Quebec, Canada

March 1979

©

Dilip Mukhedkar

March 1979

ABSTRACT

DESIGN AND CONSTRUCTION OF A SINGLE PHASE

MODIFIED MCMURRAY INVERTER

Dilip Mukhedkar

The concepts involved in the design and implementation of a single phase Modified McMurray inverter are presented and discussed. The operation of the inverter commutation circuit is explained and is analyzed. The procedure for the design of the power circuit is formulated and the practical design considerations are discussed. The protection circuits of the inverter are presented. A digital firing circuit of the inverter is designed permitting a precise inverter control. The circuit also implements an electronic 'Start-Stop' procedure. Based on the design described in this report, an 8 KVA Single Phase inverter was constructed and it was successfully tested for various operating conditions. The experimental results are also included in this report.

RÉSUMÉ

Conception et réalisation d'un onduleur monophasé
de type McMurray modifié

Dilip Mukhedkar

Ce text décrit les problèmes fondamentaux reliés à la conception et à la réalisation d'un onduleur monophasé de type McMurray modifié. Le circuit de commutation de l'onduleur est tout d'abord décrit. Par la suite, les diverses étapes de la conception du circuit de puissance ainsi que leurs implications pratiques sont expliquées. Un circuit digital d'allumage des thyristors permet d'obtenir un contrôle précis et une mise en route de l'onduleur. Finalement, les résultats expérimentaux obtenus avec un onduleur de 8 KVA, sous diverses conditions de charge, sont présentés.

ACKNOWLEDGEMENT

I wish to express my gratitude to Dr. V. R. Stefanovic for his valuable advice and expert guidance during my studies. I wish to acknowledge my deep sense of appreciation to Dr. P. D. Ziogas for his valuable suggestions and whole hearted co-operation during the preparation of this dissertation. The whole Electrical Engineering department has been most helpful and co-operative during the course of my entire study and especially I would like to acknowledge my gratitude to Dr. M. N. S. Swamy and Dr. A. Antoniou for providing me necessary facilities and help, which enabled me to complete my studies. -I am deeply indebted to Dr. V. Ramachandran for his valuable advice and guidance during my entire studies. I would like to thank Dr. J. F. Lindsay for his help and co-operation during my stay at this University. Heartfelt thanks are extended to my friends Subhash Rakeja, Alam Iftekar, Guy Oliver and Cris for their friendly co-operation and help.

I wish to record sincere appreciation of my dear friend Pradeep Bhagwat, who shared with me his insight and practical knowledge. Very special thanks to Mrs. Mohica Ewaroo for her excellent typing job when it was most needed. I am thankful to my brother Dinkar and my sister-in-law Usha for their valuable help and encouragement. Finally I wish to thank, in a very special way, my wife Kunda for her companionship, help, co-operation and uncomplaining patience throughout my studies.

TABLE OF CONTENTS

<u>TITLE</u>	<u>PAGE</u>
ABSTRACT	i
ABSTRACT	ii
ACKNOWLEDGEMENTS	iii
TABLE OF CONTENTS	iv
LIST OF FIGURES	viii
LIST OF TABLES AND APPENDIX	xiii
CHAPTER I - INTRODUCTION	
1.1 INTRODUCTION	1
1.2 VOLTAGE AND FREQUENCY CONTROL IN INVERTERS	2
1.2.1 VARIABLE DC LINK	2
1.2.2 FIXED DC LINK	4
1.2.3 COMPARISON OF VOLTAGE CONTROL TECHNIQUES	4
1.3 APPLICATION OF PWM INVERTERS	8
1.3.1 UPS APPLICATIONS	8
1.3.2 AC MOTOR DRIVES	8
1.4 INVERTERS SUITABLE FOR PWM	10
1.5 OBJECTIVES OF THE PROJECT	16
1.6 REVIEW OF THE PREVIOUS WORK	16
1.7 BRIEF OUTLINE OF THE PROJECT	18
CHAPTER II OPERATION AND ANALYSIS OF COMMUTATION CIRCUIT	20
2.1 INTRODUCTION	20

<u>TITLE</u>	<u>PAGE</u>
2.2 DESCRIPTION OF THE POWER CIRCUIT	20
2.3 BASIC INVERTER OPERATION	22
2.4 OPERATION OF COMMUTATION CIRCUIT WITH INDUCTIVE LOAD	22
2.5 ANALYSIS OF THE COMMUTATION CIRCUIT	37
CHAPTER III DESIGN OF POWER CIRCUIT	46
3.1 INTRODUCTION	46
3.2 REQUIREMENTS OF POWER CIRCUIT FOR PWM	47
3.3 SELECTION OF COMMUTATION CIRCUIT COMPONENTS	47
3.4 DESIGN SPECIFICATIONS AND CALCULATIONS	52
3.5 COMPONENT SELECTION	55
3.5.1 COMMUTATION CAPACITOR	55
3.5.2 COMMUTATION INDUCTOR	59
3.5.3 DAMPING RESISTOR	59
3.5.4 MAIN THYRISTORS	60
3.5.5 AUXILIARY THYRISTORS	62
3.5.6 FEED-BACK DIODES	64
3.5.7 CLAMPING DIODES	65
3.6 A NOTE ON INVERTER LOSSES	66

<u>TITLE</u>	<u>PAGE</u>
CHAPTER IV PROTECTION CIRCUITS	68
4.1 INTRODUCTION	68
4.2 THE PROTECTION OF THYRISTORS AGAINST EXCESSIVE dI/dt	68
4.3 PROTECTION OF THYRISTORS FROM EXCESSIVE dV/dt AND VOLTAGE SPIKES DUE TO SWITCHING TRANSIENTS	70
4.4 PROTECTION OF THYRISTORS FROM FAULT CURRENTS	75
CHAPTER V DESIGN AND IMPLEMENTATION OF THE FIRING CIRCUIT	77
5.1 INTRODUCTION	77
5.2 BASIC REQUIREMENTS	77
5.3 GUIDELINES FOR THE DESIGN	81
5.4 IMPLEMENTATION OF THE CIRCUIT	81
5.4.1 INTERFACE CIRCUIT	84
5.4.2 CONTROL CIRCUIT	87
5.4.3 OUTPUT CIRCUIT	92
CHAPTER VI EXPERIMENTAL RESULTS	97
6.1 INTRODUCTION	97
6.2 DESCRIPTION OF THE EXPERIMENTAL SET UP	98
6.3 EXPERIMENTAL PERFORMANCE	98

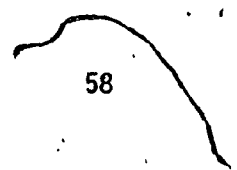
<u>TITLE</u>	<u>PAGE</u>
CHAPTER VII . CONCLUSIONS	122
REFERENCES	125
APPENDIX I	129
APPENDIX II	144
APPENDIX III	182

TABLE OF FIGURES

<u>FIGURE</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
CHAPTER I		
Figure 1.1	VOLTAGE CONTROL USING A PHASE CONTROLLED RECTIFIER	3
Figure 1.2	VOLTAGE CONTROL USING DC CHOPPER	5
Figure 1.3	VOLTAGE CONTROL USING PWM	6
Figure 1.4	SINGLE PHASE-HALF BRIDGE MCMURRAY INVERTER CIRCUIT	11
Figure 1.5	SINGLE PHASE-HALF BRIDGE MODIFIED MCMURRAY INVERTER CIRCUIT	12
Figure 1.6	SINGLE PHASE-HALF BRIDGE MODIFIED MCMURRAY BEDFORD INVERTER CIRCUIT.	13
Figure 1.7	SINGLE PHASE-HALF BRIDGE COMPLIMENTARY COMMUTATED INVERTER CIRCUIT	14
CHAPTER II		
Figure 2.1	POWER CIRCUIT OF MODIFIED MCMURRAY INVERTER	21
Figure 2.2	VOLTAGE AND CURRENT WAVEFORMS FOR DIFFERENT TYPES OF LOAD	23
Figure 2.3	GATING SIGNALS FOR THE INVERTER	24
Figure 2.4	EQUIVALENT CIRCUIT OF THE INVERTER DURING STARTING	25

<u>FIGURE</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
Figure 2.5	PATH DURING THE RETURN OF EXCESS CHARGE ON THE CAPACITOR C_c (DURING STARTING)	27
Figure 2.6	EQUIVALENT CIRCUIT DURING FIRST PORTION OF THE COMMUTATION CYCLE	28
Figure 2.7	NATURAL FIRING AND ADVANCED FIRING	30
Figure 2.8	COMMUTATION WAVEFORM FOR INDUCTIVE LOAD (NATURAL FIRING)	31
Figure 2.9	EQUIVALENT CIRCUIT OF INVERTER DURING SECOND PORTION OF COMMUTATION CYCLE	32
Figure 2.10	EQUIVALENT CIRCUIT DURING THE THIRD PORTION OF COMMUTATION CYCLE.	33
Figure 2.11	PATH DURING RETURN OF OVER CHARGE ON CAPACITOR	35
Figure 2.12	COMMUTATION WAVEFORM FOR INDUCTIVE LOAD [ADVANCE TRIGGERING]	36
Figure 2.13	RLC SERIES CIRCUIT WITH DC SOURCE E USED FOR ANALYSIS OF COMMUTATION CIRCUIT	38
CHAPTER III		
Figure 3.1	COMMUTATION CIRCUIT DESIGN CURVE	48
Figure 3.2	COMMUTATION CIRCUIT DESIGN CURVE	49
Figure 3.3	EQUIVALENT CIRCUIT OF A CAPACITOR	56

<u>FIGURE</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
Figure 3.4	APPROXIMATE CURRENT WAVEFORM OF CAPACITOR DISCHARGE CYCLE	58
Figure 3.5	CURRENT WAVEFORM FOR PURELY RESISTIVE LOAD	61
Figure 3.6	APPROXIMATE CURRENT WAVEFORM OF AUXILIARY THYRISTOR	63
CHAPTER IV		
Figure 4.1(a)	TRANSIENTS DUE TO REVERSE RECOVERY OF FEED BACK DIODES	72
Figure 4.1(b)	TRANSIENTS DUE TO REVERSE RECOVERY OF FEED BACK DIODES	73
CHAPTER V		
Figure 5.1	PWM WAVEFORM	78
Figure 5.2	PULSE TIMING DIAGRAM	82
Figure 5.3	BLOCK DIAGRAM OF FIRING CIRCUIT	83
Figure 5.4	INTERFACE CIRCUIT	85
Figure 5.5	INPUT AND OUTPUT WAVEFORM OF INTERFACE CIRCUIT	86
Figure 5.6	SCHEMATIC DIAGRAM OF CONTROL CIRCUIT	88
Figure 5.7	CONTROL CIRCUIT TIMING DIAGRAM	89
Figure 5.8	TIMING DIAGRAM OF MASTER CLEAR CIRCUIT	93
Figure 5.9	SCHEMATIC DIAGRAM OF OUTPUT CIRCUIT	94
Figure 5.10	CIRCUIT DIAGRAM OF PULSE AMPLIFIER	96



<u>FIGURE</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
CHAPTER VI		
Figure 6.1 & 2	EXPERIMENTAL SET-UP OF SINGLE PHASE MODIFIED MCMURRAY INVERTER	100
Figure 6.3 & 4	CLOSE-UP VIEW OF POWER CIRCUIT	101
<u>Figure 6.5 & 6</u>	INTERFACE & CONTROL CIRCUIT OUTPUT CIRCUIT (PULSE AMPLIFIER CIRCUIT)	102
Figure 6.7	CLOSE-UP VIEW OF SNUBBER CIRCUIT	103
Figure 6.8	FIRING SEQUENCE OF SINGLE PHASE MODIFIED MCMURRAY INVERTER FOR REGULAR OPERATION	104
Figure 6.9	OUTPUT OF PULSE AMPLIFIER CIRCUIT	105
Figure 6.10	COMMUTATION CAPACITOR CURRENT & VOLTAGE WAVEFORM	106
Figure 6.11	COMMUTATION CAPACITOR CURRENT & VOLTAGE WAVEFORM	107
Figure 6.12	VOLTAGE AND CURRENT WAVEFORM ACROSS LOAD	108
Figure 6.13	DV/DT ACROSS MAIN THYRISTOR T 1	109
Figure 6.14	DV/DT ACROSS AUXILIARY THYRISTOR TA 1	110
Figure 6.15	VOLTAGE & CURRENT WAVEFORM ACROSS LOAD	111
Figure 6.16	DV/DT ACROSS MAIN THYRISTOR T 1	112
Figure 6.17	DV/DT ACROSS AUXILIARY THYRISTOR TA 1	113
Figure 6.18	VOLTAGE & CURRENT WAVEFORM ACROSS LOAD	114
Figure 6.19	DV/DT ACROSS MAIN THYRISTOR T 1	115
Figure 6.20	DV/DT ACROSS AUXILIARY THYRISTOR TA 1	116

<u>FIGURE</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
Figure 6.21	DV/DT ACROSS MAIN THYRISTOR T 1	117
Figure 6.22	DV/DT ACROSS AUXILIARY THYRISTOR TA 1	118
Figure 6.23	COMMUTATION CAPACITOR VOLTAGE WAVEFORM	119
Figure 6.24	COMMUTATION CAPACITOR CURRENT WAVEFORM	120
Figure 6.25	COMMUTATION CAPACITOR CURRENT & VOLTAGE WAVEFORM	121
APPENDIX I		129
Figure [A]	SCHEMATIC DIAGRAM OF AMPLIFYING GATE THYRISTOR	131
Figure [B.1]	SNUBBER NETWORK	132
Figure [C.1]	GRAPH OF $\frac{I_{pk}(DC)}{I_{pk}(AC)}$ vs L/R	
Figure [C.2]	GRAPH OF $\frac{I_t^2(DC)}{I_t^2(AC)}$ vs L/R	

LIST OF TABLES

<u>TABLE</u>	<u>DESCRIPTION</u>	<u>PAGE</u>
CHAPTER I		
Table 1.1	COMPARISON TABLE FOR THREE METHODS OF VOLTAGE CONTROL	7
Table 1.2	GENERAL COMPARISON OF INVERTERS SUITABLE FOR PWM	15

LIST OF APPENDIX

APPENDIX I

A	AMPLIFYING GATE THYRISTORS	130
B	DESCRIPTION, OPERATION & SELECTION OF SNUBBER CIRCUIT	130
C	FUSE SELECTION PROCEDURE	136

APPENDIX II

	DETAIL SPECIFICATIONS OF THE COMPONENTS	144
--	---	-----

APPENDIX III

	COMPUTER PROGRAMME & FLOW CHART	182
--	---------------------------------	-----

CHAPTER I

INTRODUCTION

1.1 Introduction:

A new era in the field of Power Conversion started with the introduction of thyristor in 1957. Since then immediate attention was focussed on the application of thyristors in inverter circuits. In recent years, thyristor technology has made a significant progress, permitting the operation of sophisticated inverter circuits in variety of applications.

A thyristor cannot be switched off (commutated) by a gate control. In thyristor converters operating from AC voltage sources, the commutation is provided by the reversal of the applied voltage (phase commutation). When a thyristor converter operates from a DC supply, an additional circuit, called commutation circuit has to be generally provided to turn off thyristors (forced commutation). Consequently the thyristor inverters are very often classified according to the kind of the associated commutation circuit [1], [2], [3].

One should note that inverter applications require much better thyristor dynamic characteristics; such as short turn-off times, high dv/dt and di/dt capabilities etc; than in the case of phase commutated converters. However, Inverter graded thyristors are now commercially available, thus making possible increasingly sophisticated inverter operations.

1.2 Voltage and Frequency Control in Inverters

In many inverter applications, it is necessary to obtain an AC output voltage with variable frequency and amplitude. Frequency Control is readily accomplished by controlling the frequency at which various thyristors are turned "on" and "off" (i.e. fired and commutated). Several methods are available for controlling the output voltage of an inverter [4]. Most of these methods fall into one of the two broad categories, namely;

Variable DC Link and

Fixed DC Link.

1.2.1 Variable DC Link

For methods in this category, the output voltage is controlled indirectly by varying the level of the DC input. This is usually accomplished by one of the two following techniques; Controlled Rectifier and DC Chopper.

1.2.1. (a): Controlled Rectifier

Three phase AC supply is rectified by a controlled full wave, three phase rectifier which produces a variable DC level which is filtered and then fed to the Inverter [5]. The block diagram of this system is shown in Fig [1-1].

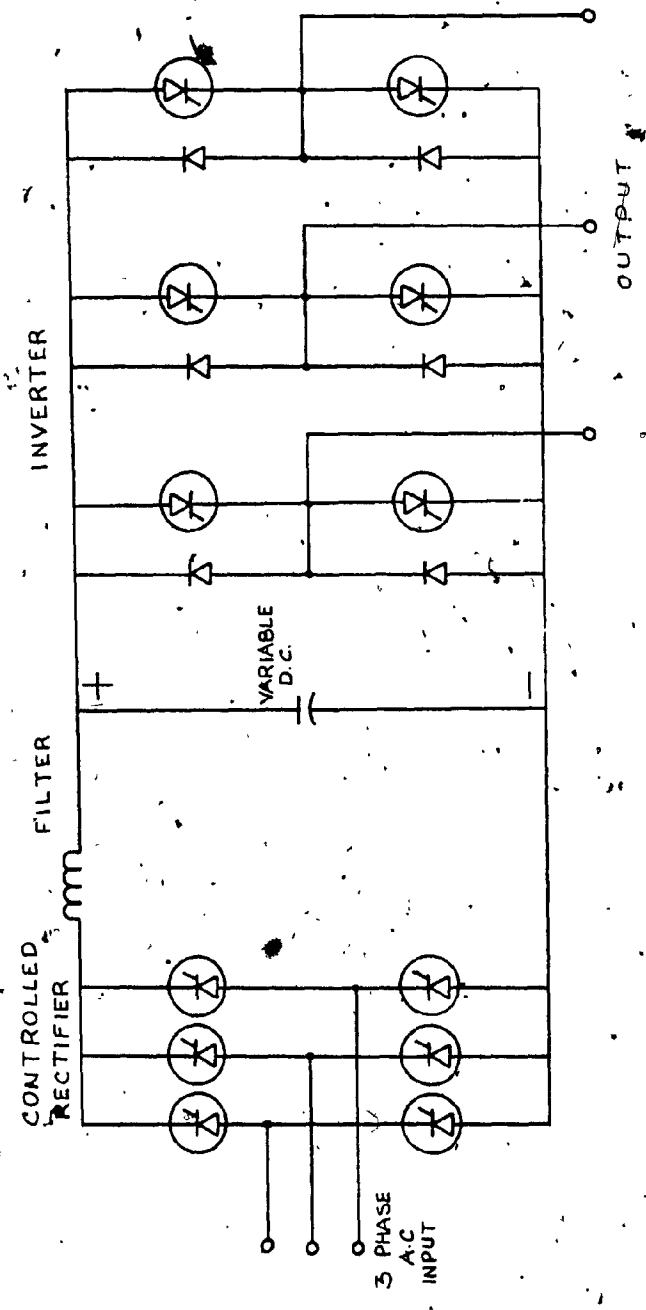


Fig [1.1] Voltage Control using a Phase Controlled Rectifier.

Note: The thyristor symbol enclosed in a circle represents a thyristor that may be turned "on" and, if necessary commutated by means of circuit elements not included in the diagram.

1.2.1. (b): DC Chopper:

A fixed DC voltage (from a battery, DC bus, or diode rectifier) is converted to a variable DC level by DC Chopper, which is filtered and then fed to an Inverter [5]. The block diagram of this system is shown in Fig. [1.2].

1.2.2. Fixed DC Link.

This category includes all methods in which both the amplitude and the frequency of the output voltage are controlled within the Inverter itself. The most commonly used method in this category is referred to as pulse width modulation or PWM. PWM, when applied to inverters, can be described as a method of controlling the amplitude of the output voltage by varying the interval during which the load is connected to supply. The result is that the output consists of a train of discrete pulses. The width of these pulses is controlled by varying the instants at which various thyristors are fired and/or commutated [6]. The block diagram of this system is shown in Fig [1.3].

1.2.3 Comparison of Voltage Control Techniques.

A comparison Table for the three methods of voltage control (mentioned above), indicating which of desirable characteristics are possible with each technique, is given in Table [1.1]. Thus, from this comparison, it can be seen that the PWM

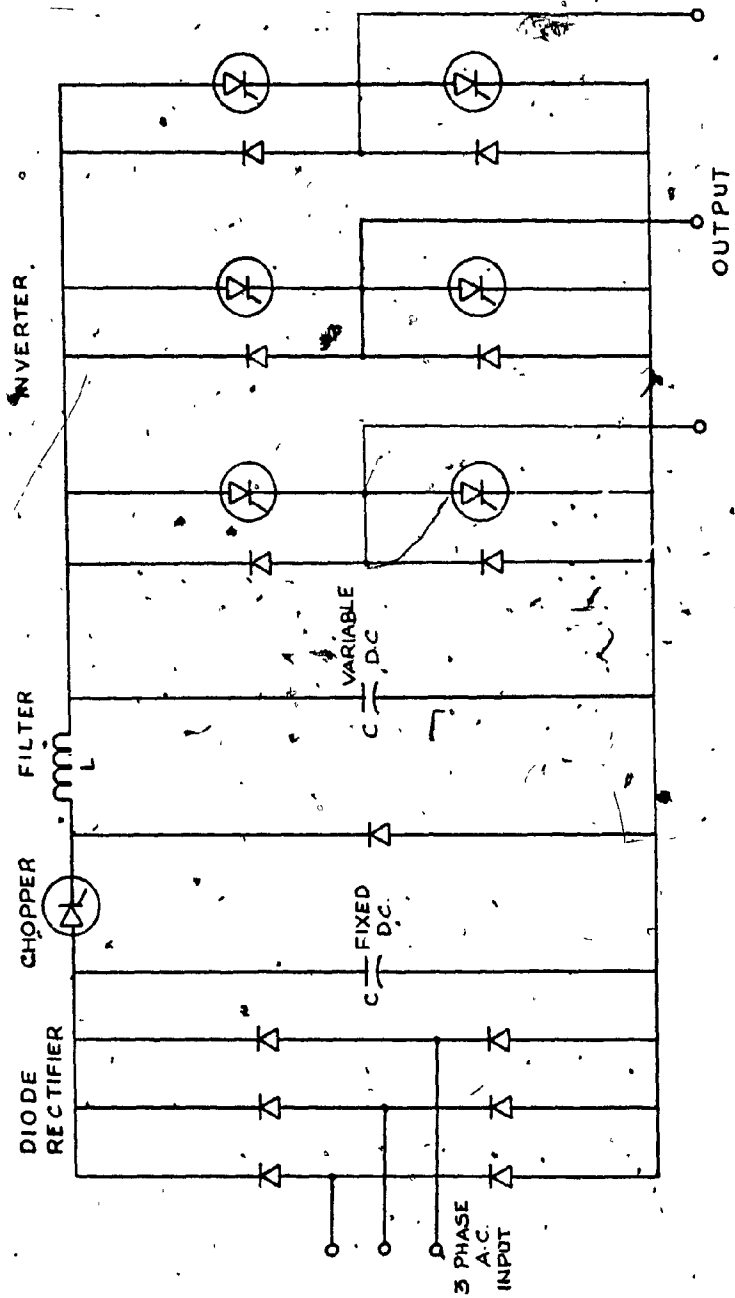


Fig. [1.2] Voltage Control using DC Chopper.
Note: Same as given in fig. [1.1].

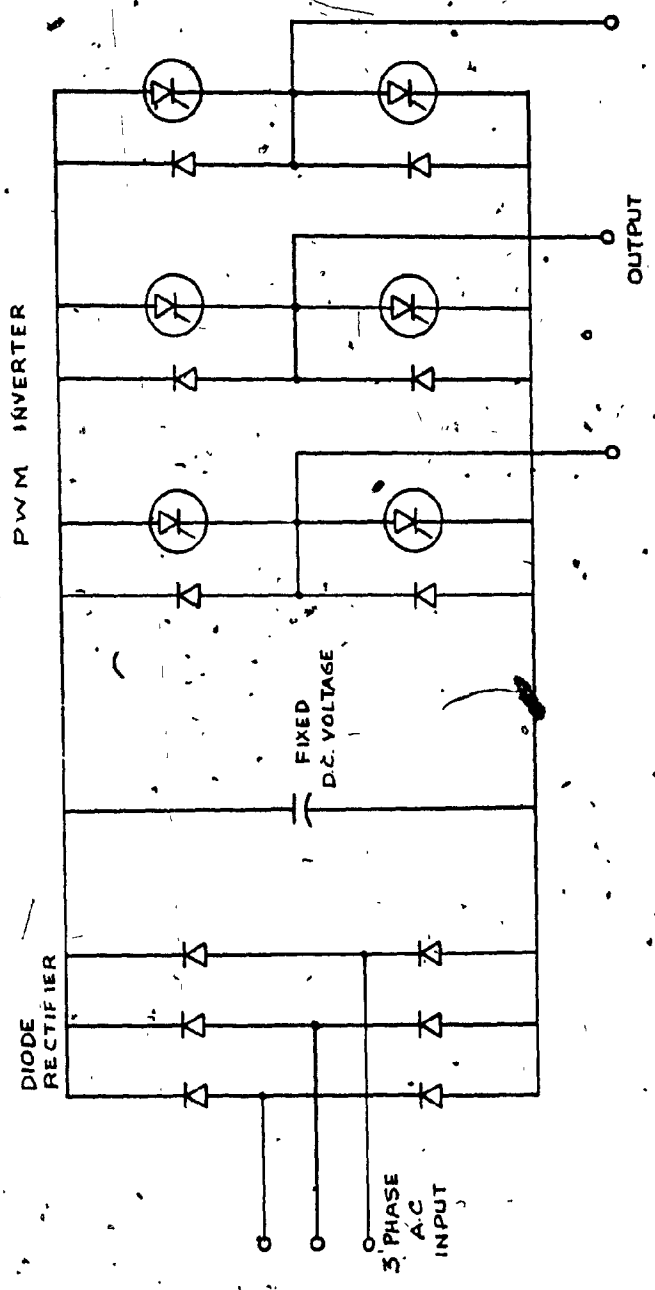


Fig. [1.3] Voltage Control using PWM.

Note: Same as in fig. [1.1].

TABLE 1.1

Comparison Table for three Methods of Voltage Control

S.No.	Desired Characteristics	Controlled Rectifier	DC Chopper	PWM
1	Good Input Power factor and Harmonics	No	Yes	Yes
2	Can be Fed by AC or DC	No	Yes	Yes
3	No Additional Components	No	No	Yes
4	Restriction on Design of Commutation Stage.	Yes	Yes	No
5	Low output harmonics	Yes	Yes	No
6	Minimum Number of Commutations per cycle.	Yes	Yes	No
7	Simple Control Circuitary	Yes	Yes	No

Note: Detailed explanation of above is given in [6].

Inverter system has advantages over other two systems. The distinct advantage is that the control of output voltage and frequency is achieved with one power controller and special control logic. The disadvantage of this system is that the control circuitry of this system is usually complex and is largely determined by the application requirements.

The availability of microprocessors is now making the control circuit design easier, resulting at the same time in controllers with an improved performance.

1.3 Application of PWM Inverters:

Main applications of PWM Inverters include the following:-

- 1) Uninterruptible power supplies (UPS) for stand by power sources for computers, medical equipment etc., where Inverter is controlled to provide constant output voltage and frequency.
- 2) AC motor drives where the variable voltage/variable frequency capability of PWM Inverters is utilized.

1.3.1. UPS Applications:

The following are the prime requirements of the Inverters used for UPS applications. The Inverter has to perform the basic conversion from DC to AC, eliminate unwanted harmonics, provide a stable output frequency, regulate

for load and line variations and include some means for protecting the Inverter from over loads on its output. Such a performance is extremely important. PWM Inverters offers such performance and in addition they have some distinct advantages over other types of Inverters used for the same purpose [7]. Therefore PWM Inverters are preferred for UPS applications.

1.3.2. AC Motor Drives:

The induction motor has been one of the most widely used motors in the industry. Before the advent of thyristor, Conventional methods (voltage variation, pole change, etc.) were used for its limited speed control. However its application was mainly limited to drives with constant or near constant speed. Whenever a process required a wide speed range, the dc motor was used. Now, with availability of thyristor Inverters, the speed of the induction motor can be effectively controlled by controlling the motor input frequency. The induction motor has advantages over dc motor in terms of mechanically robust construction, decreased maintenance, reduced cost, etc. Thus the use of induction motor in variable speed drive is gradually increasing. However, one should not conclude that the induction motor will entirely replace the dc motor in the foreseeable future. The main reason is that the cost of the accessories (like Inverters) associated with induction

motor drive is usually 2-3 times higher than the cost of power supplies for variable speed dc motors and in addition, the control circuitry of the induction motor drive is usually complex as compared to its dc counterpart. The AC motor drive will be selected only when a particular application makes it more economical [4], or, when critical performance requirements make the dc motor drive unsuitable.

Among the inverters suitable for AC motor drive applications, PWM Inverter is one of the often considered choice. It fulfills the drive requirements [5] and offers superior performance [8].

1.4 Inverters suitable for PWM

The selection of a particular type of Inverter for a PWM operation is largely dictated by the application requirements. Within PWM class of Inverters, there are different types available. Among those, the following are often considered:

- McMurray Inverter, fig. [1.4];
- Modified McMurray Inverter, fig. [1.5];
- Modified McMurray Bedford Inverter, fig. [1.6];
- Complimentary commutated Inverter (CCI), Fig. [1.7]
(This is similar to McMurray Bedford Inverter).

A general comparison of these inverters is presented in Table 1.2. This comparison is based on commutation component ratings, efficiency, number of components in the circuit, thyristor protection and complexity

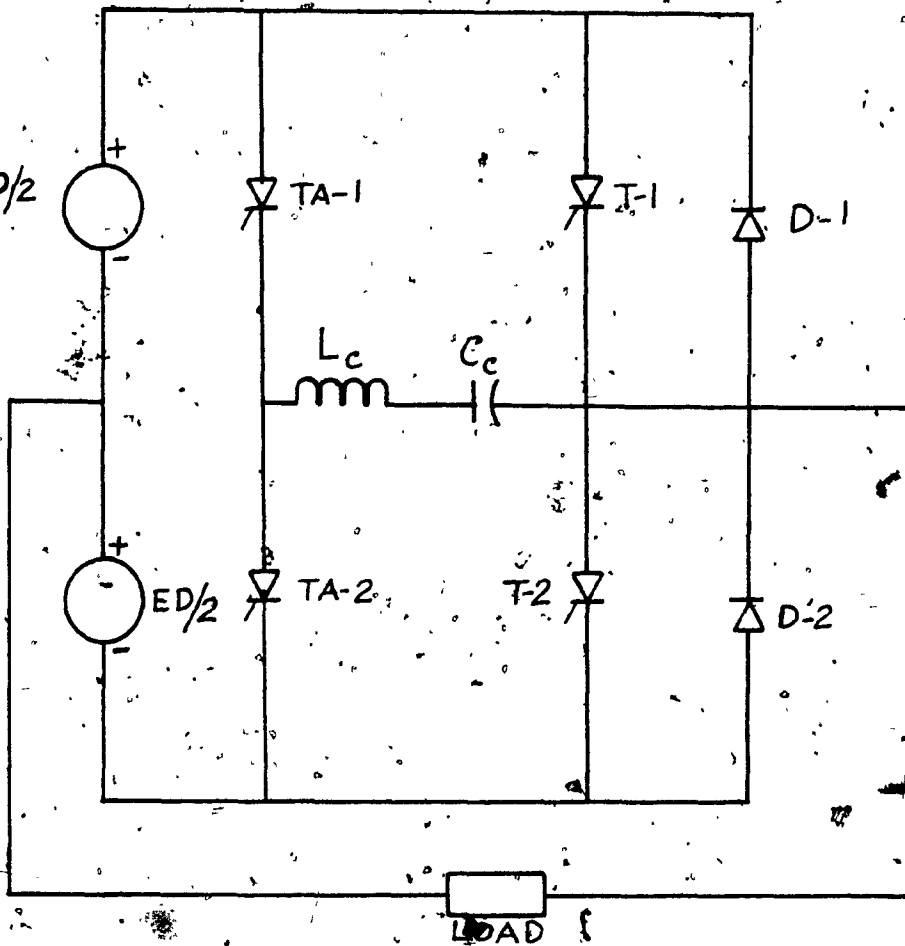


Fig. [1.4] Single Phase - Half Bridge McMurray Inverter Circuit

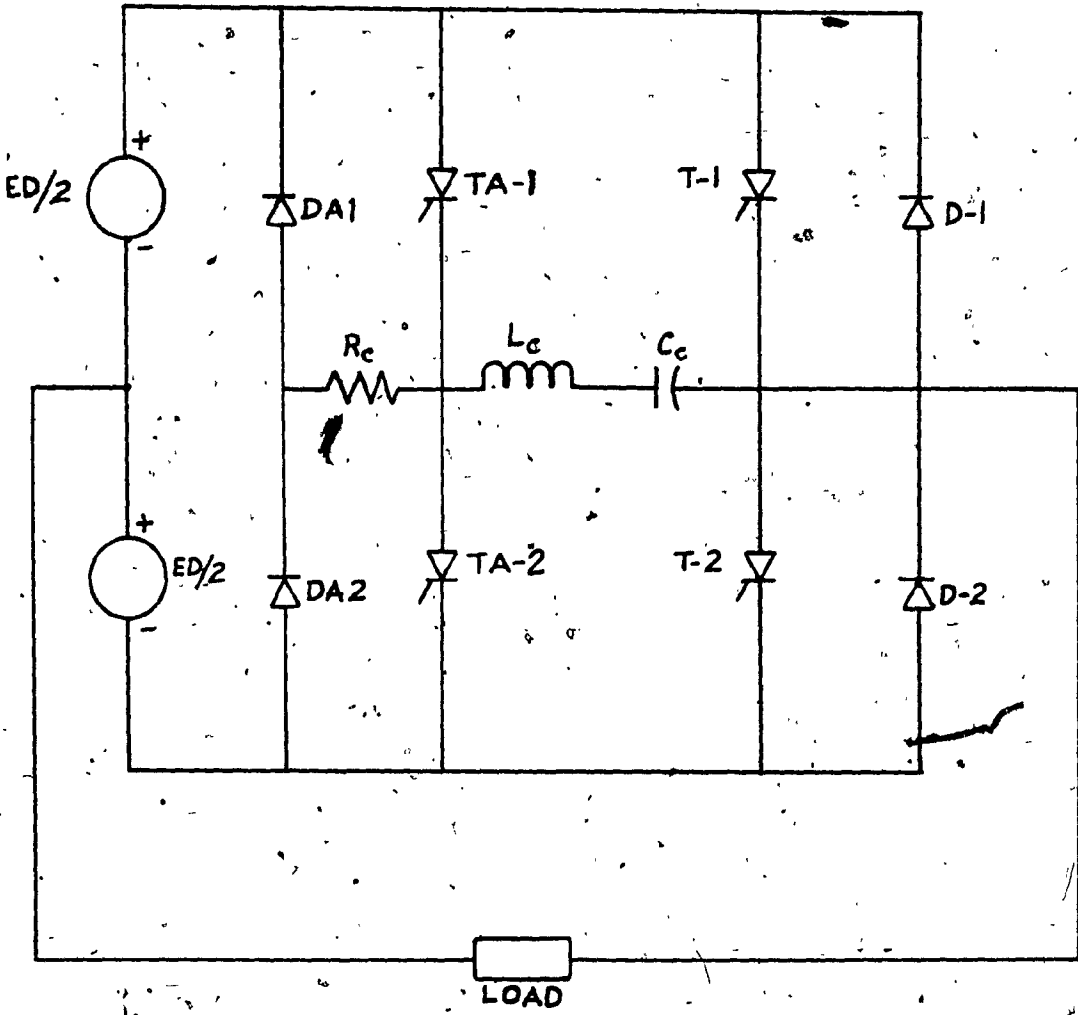


Fig. [1.5] Single Phase - Half Bridge Modified McMurray Inverter Circuit.

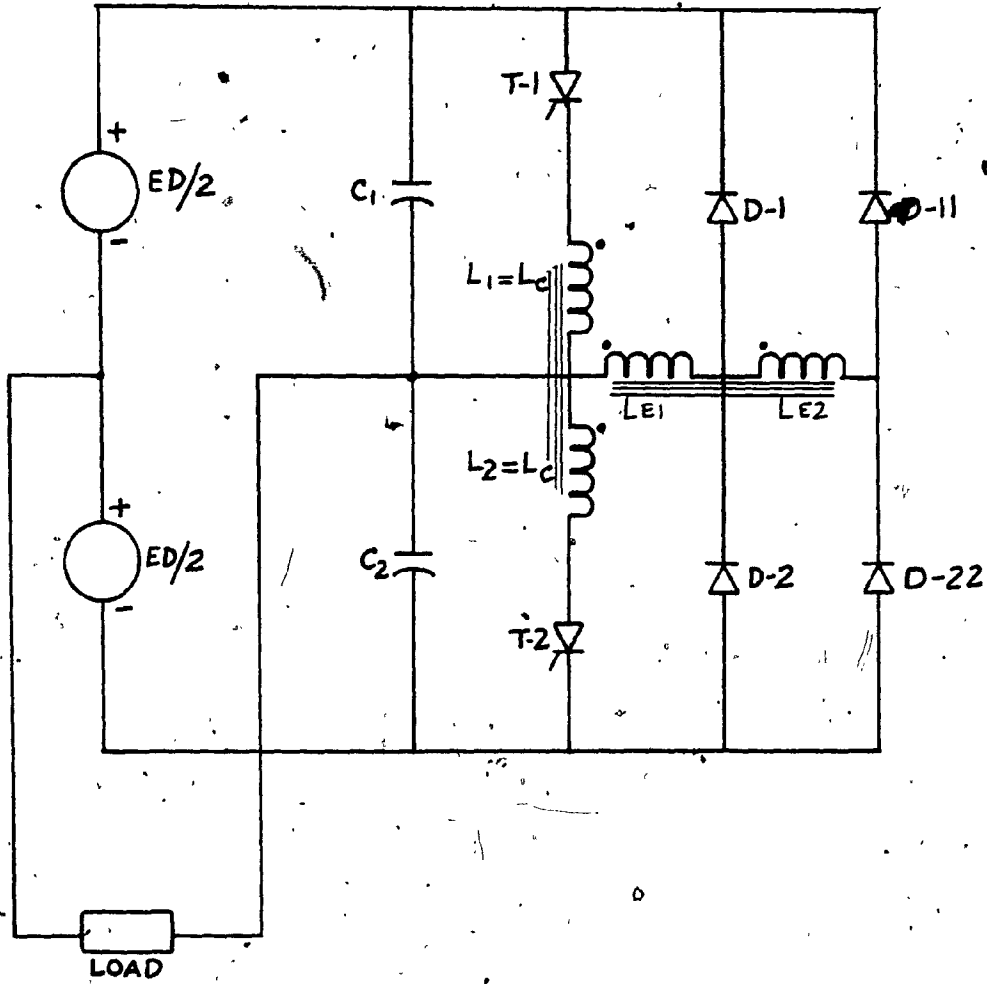


Fig. [1.6] Single Phase - Half Bridge Modified McMurray Bedford Inverter Circuit.

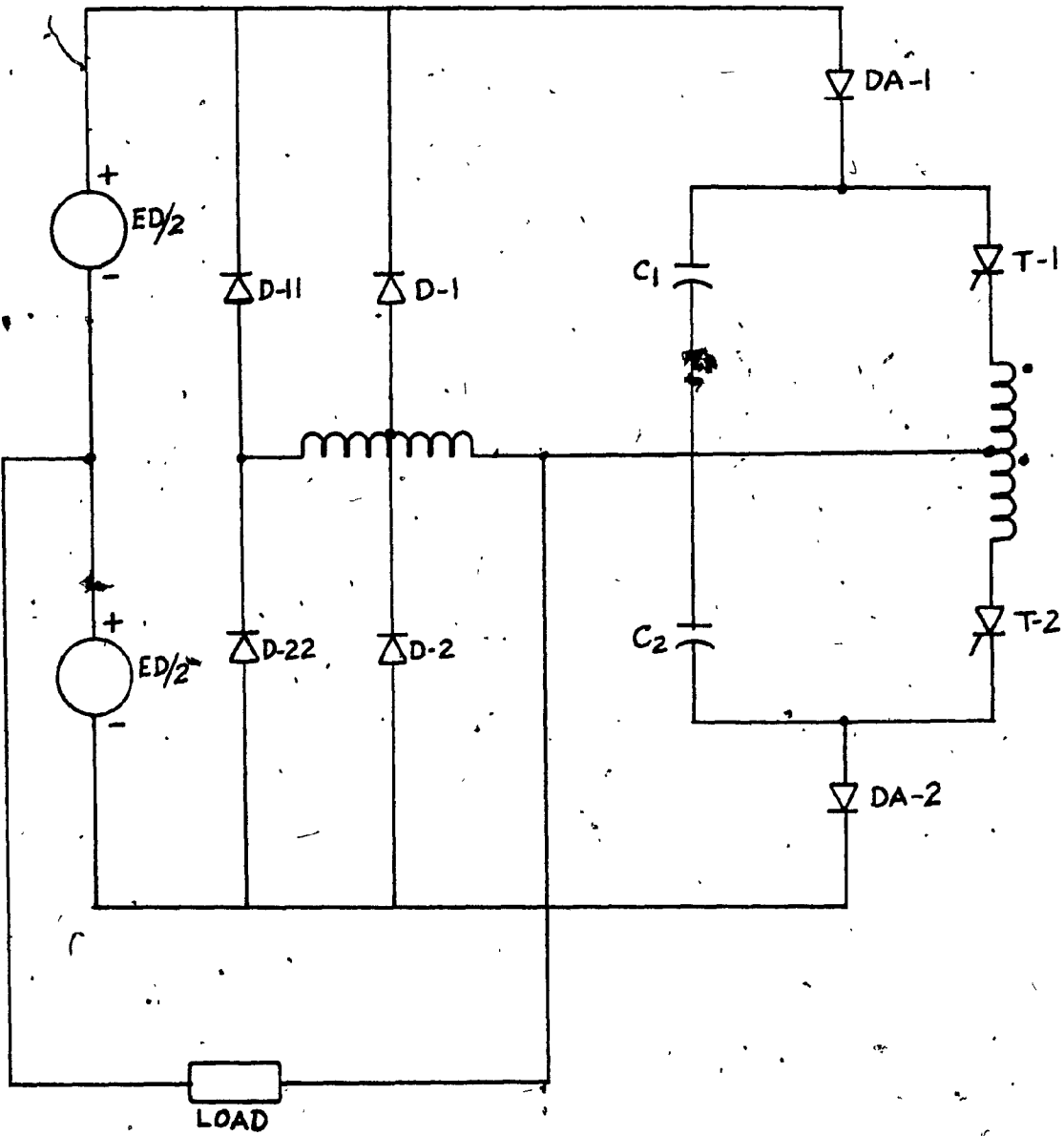


Fig. [1.7] Single Phase - Half Bridge Complimentary Commutated Inverter Circuit.

Table 1.2 General Comparison of Inverters suitable for PWM

Parameters	McMurray Inverter	Modified McMurray Inverter	Modified McMurray-Bedford Inverter	Complimentary Commutated Inverter (CCI)
Commutation Component ratings	Lowest	Next lower	Relatively higher	Relatively higher
Efficiency of Commutation circuit	Highest	Highest	Next Highest	Next Highest
No. of Components in the circuit	Lowest	Next lower	Relatively higher	Relatively higher
Voltages Stresses & dv/dt on thyristors	Highest	Next highest	Lower	Lower
di/dt in the thyristors	Highest	Next highest	Lower	Lower
Complexity of Control Circuitry	Complex	Complex	Relatively simpler	Relatively simpler

of control circuitry.

1.5 Objectives of the Project:

In many applications, the inverter is an important building block of the total system. The development of the power electronics laboratory requires several inverters, all to be used as building blocks in various drive applications. Therefore a single phase - half bridge modified McMurray Inverter was designed and fabricated. The modified McMurray Inverter was selected on the basis of its advantages over other inverters in terms of commutation component ratings, efficiency of commutation circuit, no of components etc. The design and fabrication of this inverter was the objective of this study and is reported here. Before presenting a brief outline of the project it will be appropriate to review the previous work.

1.6 Review of Previous work.

Research work on Inverter circuits started as early in 1920 when Alexanderson and Price in the United States announced the parallel Inverter (with which two alternating working thyratrons were turned off by a capacitor) [10], [11].

The research on inverters continued from this period onwards. The important research developments on Inverters from 1920 to 1957 are mentioned by Klemens Heumann [12]. Thus the basic theory for inverters was developed in the era of mercury arc devices [13].

The introduction of thyristor (silicon Controlled rectifier (SCR)) in 1957 gave a great impetus to Inverter technology. In 1961, McMurray and Shattuck published the first inverter circuit with thyristors [14].

Since then, the inverter technology progressed rapidly and now there are several efficient Inverter circuits available. McMurray's auxiliary impulse commutated Inverter circuit was reported in 1964 [15].

Later in 1970, Penkowski and Pruzinsky presented a modified version of McMurray's Inverter [16]. In 1977, Palaniappan et al presented a modified McMurray Inverter circuit with a pulse forming network [PFN] in the commutation circuit [17]. Klaassens has presented analysis of the commutation circuit of McMurray Inverter for design purposes [18].

Carlton et al have presented practical design considerations for this Inverter circuit [19].

Mokrytzki [9], Pollack [5] and many others have recognized the advantages of this Inverter for PWM.

Sahli reported the use of McMurray Inverter for traction applications [20]. Finally Plunkett and Plette reported the use of Modified McMurray Inverter in induction motor drive for transit cars. [21].

1.7 Brief Outline of the Project:

In this section, a brief outline of the project is presented.

The operation and analyses of commutation circuit is described in chapter 2. The operation of the commutation circuit for inductive load condition is explained. The triggering of the next main thyristor plays an important role in the commutation process and is explained here. Finally, the analysis of the commutation circuit is given and is used in sizing of the commutation components.

The design of the Inverter power circuit is described in chapter 3. Practical design considerations are discussed. Requirements of the power circuit for PWM are outlined. Then the selection of the values for the commutation circuit is presented. Finally the determination of the ratings of components and component selection are given.

The protection circuits for the inverter are described in chapter 4. The protection of thyristors against di/dt failures, excessive dv/dt and voltage spikes due to switching transient, and the protection of thyristors from fault currents are discussed. Then the solutions to the above problems are presented.

The firing circuit of the Inverter is described in chapter 5. The firing circuit generates the required triggering pulses to the thyristors and also controls the starting and stopping operation of the Inverter. The requirements for the design of the firing circuit are first outlined and the design implementation is presented.

The firing circuit is realized using digital scheme. The salient features of the firing circuit include the precise adjustment of delay between firing the auxiliary and the main thyristors; as well as the electronic 'start-stop' operation of the inverter.

The experimental performance of the Inverter is presented in chapter 6. The obtained results indicate a satisfactory inverter operation.

Finally, the conclusions are presented in chapter 7 .

CHAPTER II

OPERATION AND ANALYSIS OF COMMUTATION CIRCUIT

2.1 Introduction: The operation and analysis of the commutation circuit of the modified McMurray inverter is presented. This is an auxiliary impulse commutated circuit which is distinguished from the original McMurray inverter by the addition of two diodes and a resistor fig. [1.4] and [1.5]. They are used for the return of the overcharge on commutating capacitor to the DC voltage source. The circuit and its operation is described next followed by the analyses of the commutation circuit,

2.2 Description of the Power Circuit:

The power circuit of the single phase modified McMurray inverter is shown in fig. [2.1]. This circuit uses a centre tapped DC supply. T-1 and T-2 are the main thyristors which carry load current. D-1 and D-2 are the feedback diodes associated with T-1 and T-2 respectively. TA-1 and TA-2 are the auxiliary thyristors used to commutate T-1 and T-2. DA-1 and DA-2 are the clamping diodes, which are used for the return of the overcharge on the commutation capacitor (C_c) to the DC voltage source. They also serve to commutate the auxiliary thyristors TA-1 and TA-2. R_c is the damping resistor which controls the undershoot of the capacitor voltage. L_c is the commutation inductor and C_c is the commutation capacitor. L_1 is the inductor used for limiting rate of rise of load current (di/dt) in the thyristors.

F_1 and F_2 are high speed fuses C_F . C_F is the dc filter capacitor which is considered as a part of the dc supply.

2.3 Basic Inverter Operation:

The main thyristor T-1 and T-2 are gated to conduct during alternate half cycles. When the load is reactive, the feedback diodes D-1 and D-2 conduct during part of each half cycle to return the magnetic energy stored in the load inductance to the dc supply. Commutation of the main thyristors is accomplished by means of auxiliary thyristors TA-1 and TA-2 in conjunction with the capacitor C_c and the inductor L_c . The voltage and current waveshapes for different types of load are shown in fig. [2.2] while the gating signals for starting and regular operation are shown in fig. [2.3].

2.4 Operation of Commutation Circuit With Inductive Load.

Commutation process is explained on the assumption that the load current remains constant during the commutation process and commutation components are ideal.

The inverter is started by triggering thyristors T-1 and TA-2 simultaneously. T-1 starts conducting the current from the DC supply. This current consists of a load component (I_L) and an oscillatory current i_c . C_c starts to charge the commutation capacitor. When the capacitor gets fully charged (with y side positive fig. [2.4]) the i_c falls to zero. At that moment, capacitor is charged to voltage; $e_c = -2ED$ [See Sec. (2:5)] and TA2 turns off (as it becomes reverse.

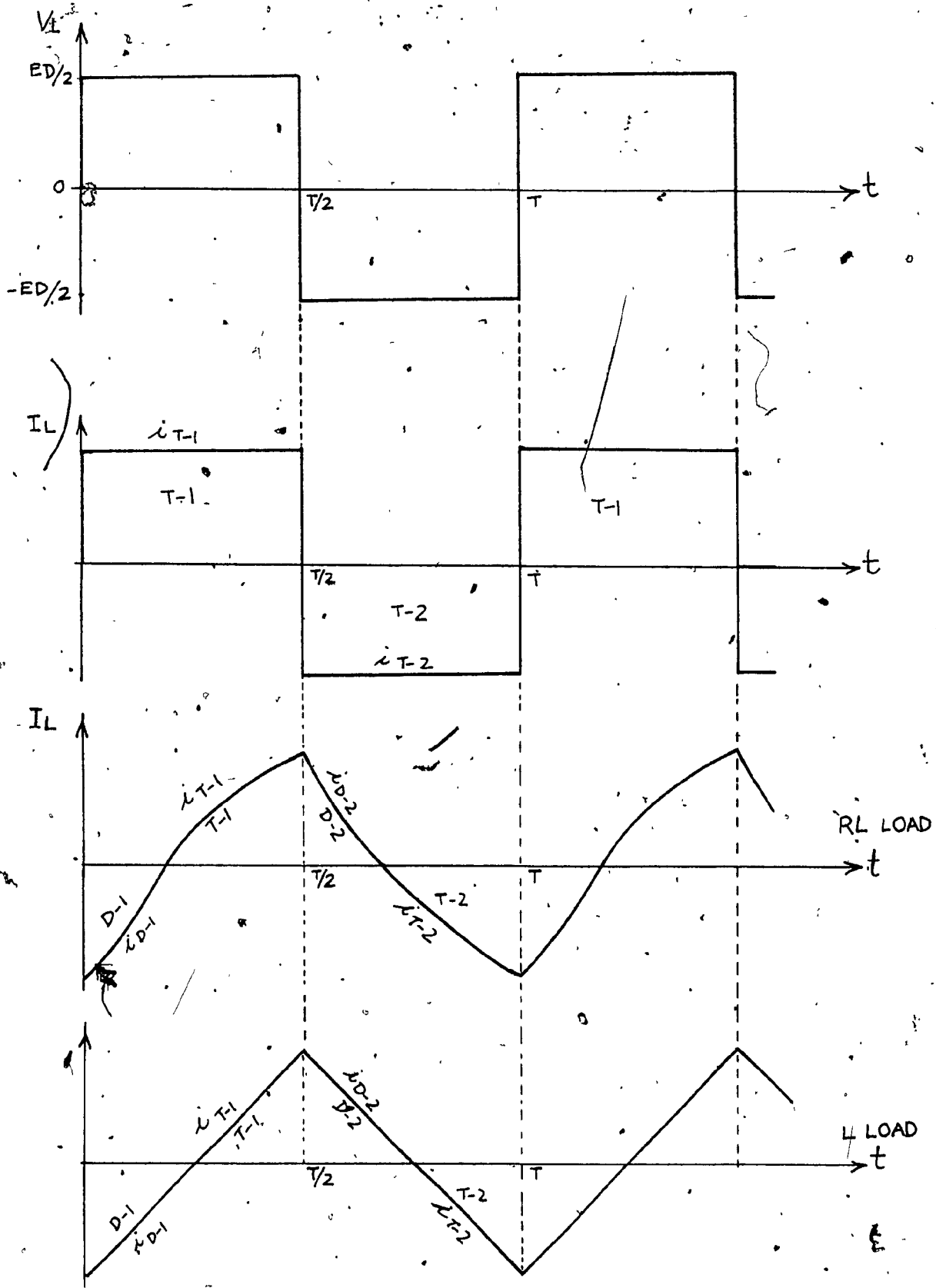


Fig. [2.2] Voltage and Current Waveforms for Different Types of Load.

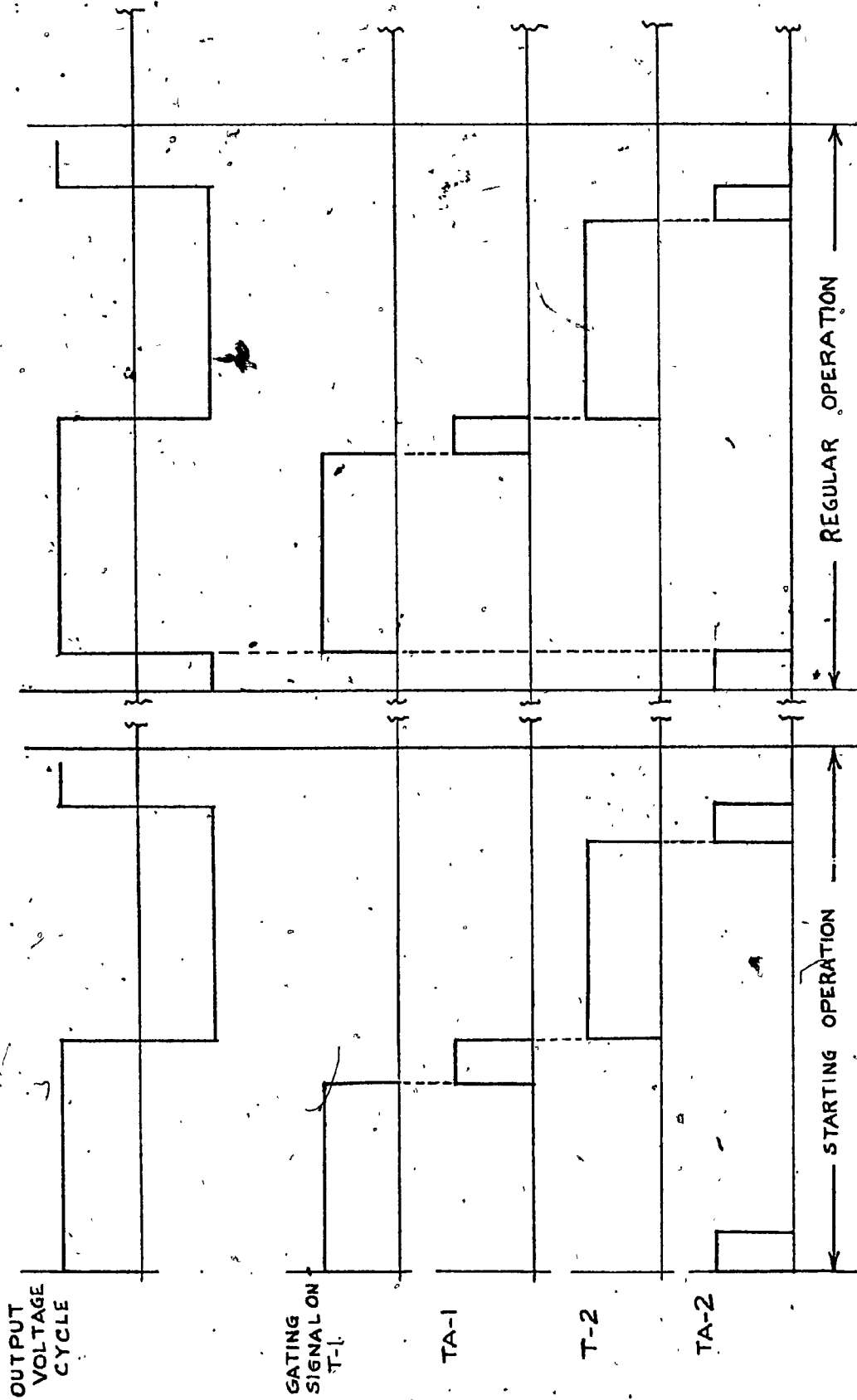


Fig. [2.3] Gating Signals for the Inverter.

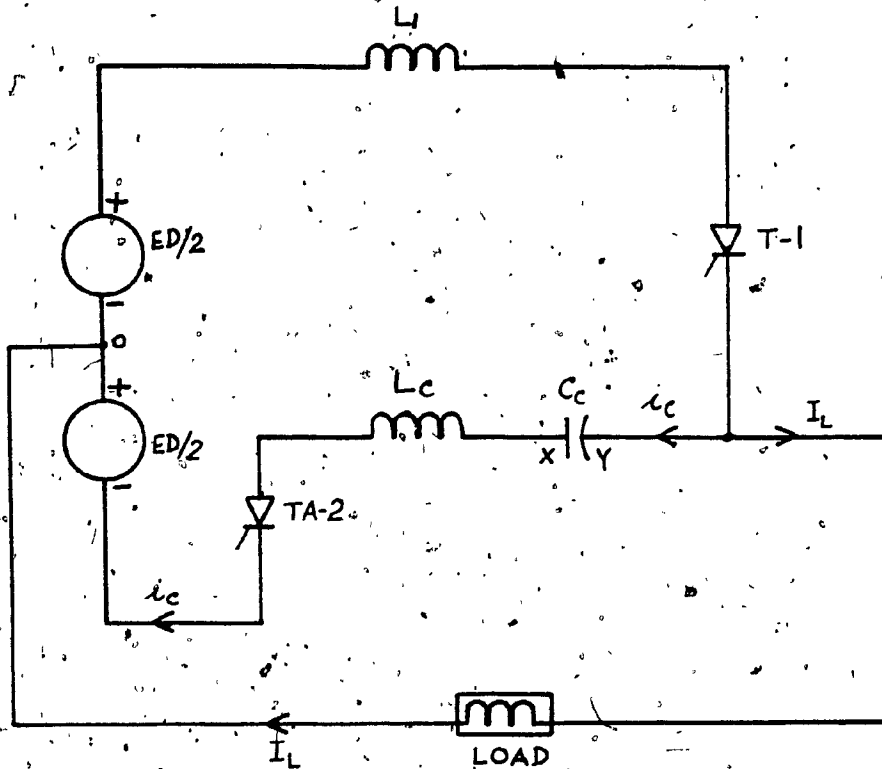


Fig. [2.4] Equivalent Circuit of the Inverter During Starting.

biased). The equivalent circuit for this interval is shown in fig. [2.4]. Since the capacitor voltage exceeds the supply voltage, the excess charge on the capacitor is fed back to the DC supply through the path shown in fig. [2.5]. The capacitor discharges to the level set by the DC bus [i.e. $e_c = -ED$]. The polarity of the capacitor voltage is such that it is ready to commutate T-1.

Commutation of T-1: In order to commutate T-1, TA-1 is triggered. The equivalent circuit of the inverter, after TA-1 has been fired, is shown in fig [2.6]. The capacitor (C_c) starts discharging. The discharge current i_c starts increasing sinusoidally through TA-1, L_c , C_c . Since I_L is assumed constant, the current through T-1 decreases as i_c is increasing. When i_c is equal to I_L , the current through T-1 is reduced to zero and the entire load current is transferred to TA-1. However, the capacitor current continues to increase and the excess of i_c over the load current I_L , now starts flowing through D-1, thereby putting a reverse voltage on T-1 (essentially equal to a forward diode drop). The discharge current i_c reaches its peak and starts decreasing thereby changing polarity of the voltage across C_c .

For safe circuit operation, T-1 must remain reverse biased for a time interval ($t_{o\min}$) larger or equal to the specified turnoff time T_q (i.e. $t_{o\min} \geq T_q$). T-2 can only be fired (turned 'on'), when reverse bias interval for T-1 equals or exceeds T_q .

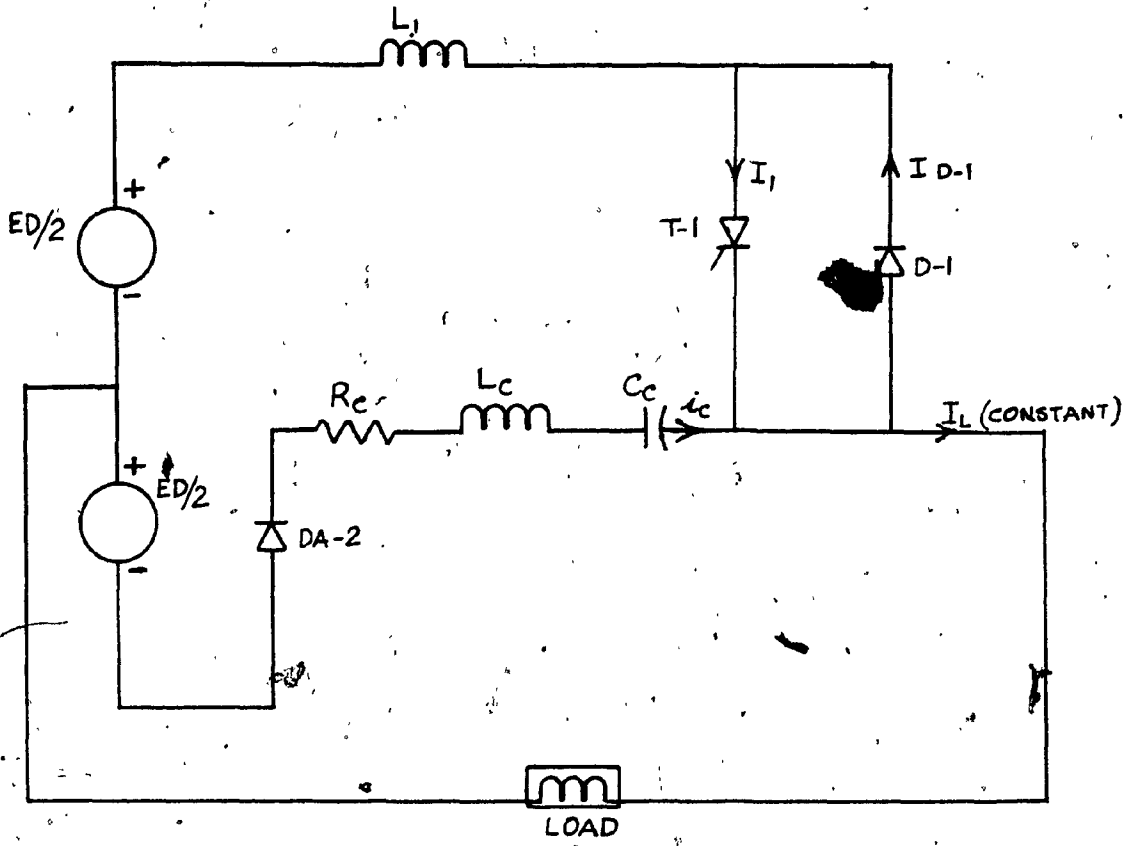


Fig. [2.5]. Path during the return of excess charge on the capacitor C_c (during starting).

Note: $I_1 = I_L - i_c$ for $i_c \leq I_L$ and $I_{D-1} = 0$

$I_{D-1} = i_c - I_L$ for $i_c \geq I_L$ and $I_1 = 0$

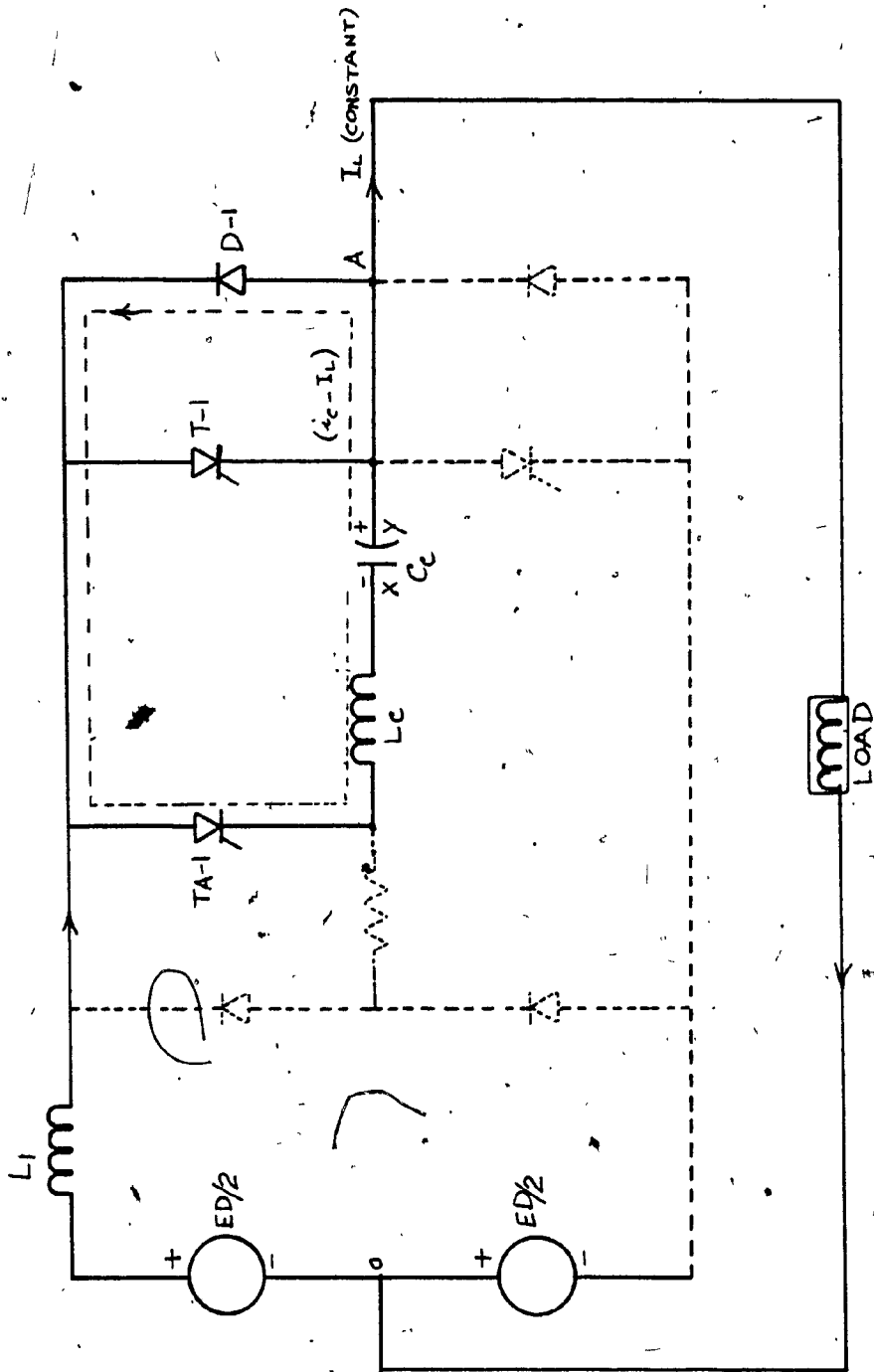


Fig. [2.6] Equivalent Circuit During First Portion Of The Commutation Cycle.

Here two different cases can occur, as follows:

Case I: T-2 can be fired $\pi\sqrt{L_C C_C}$ seconds after TA-1 is triggered (i.e. T-2 is fired at or about the time the i_C would fall to zero during the no load operation).

This is called Natural triggering [Fig. (2.7 a)].

Case II: T-2 can be fired, when i_C is equal to $I_{L \max}$ (where $I_{L \max}$ is the maximum load current, which the inverter can commute successfully). This is called Advanced firing: [fig. (2.7 b)].

Now considering Case I, one recalls that the capacitor discharge current i_C starts falling after reaching its peak, thereby changing the polarity of the voltage across C_C . In this process when i_C is equal to I_L , D-1 stops conducting and the commutation interval for T-1 ends [fig. [2.8]: I portion of commutation cycle].

Also, when i_C is equal to I_L , the capacitor voltage e_C is less than ED. D-2 now tends to conduct but it can not conduct unless e_C is equal to ED. Therefore the voltage on the capacitor is built at a constant current ($i_C = -I_L$) till e_C is equal to ED. [22]. [fig. (2.8): II portion of commutation cycle and fig. (2.9)].

When $e_C \geq ED$, D-2 conducts, the voltage across load changes polarity and i_C continues to decay sinusoidally through the path shown in fig [2.10] until it falls to zero. At this point e_C is greater than

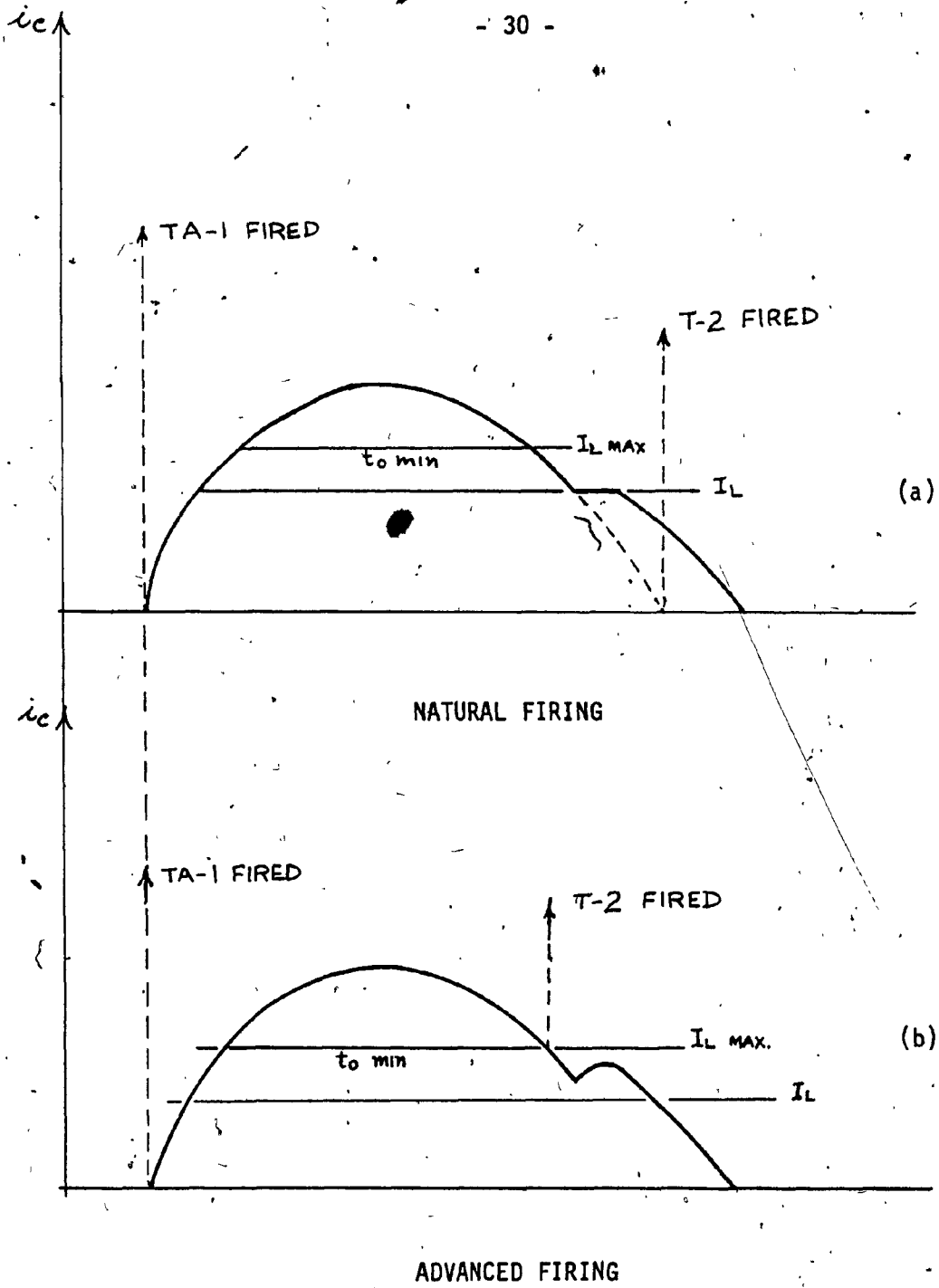


Fig [2.7]

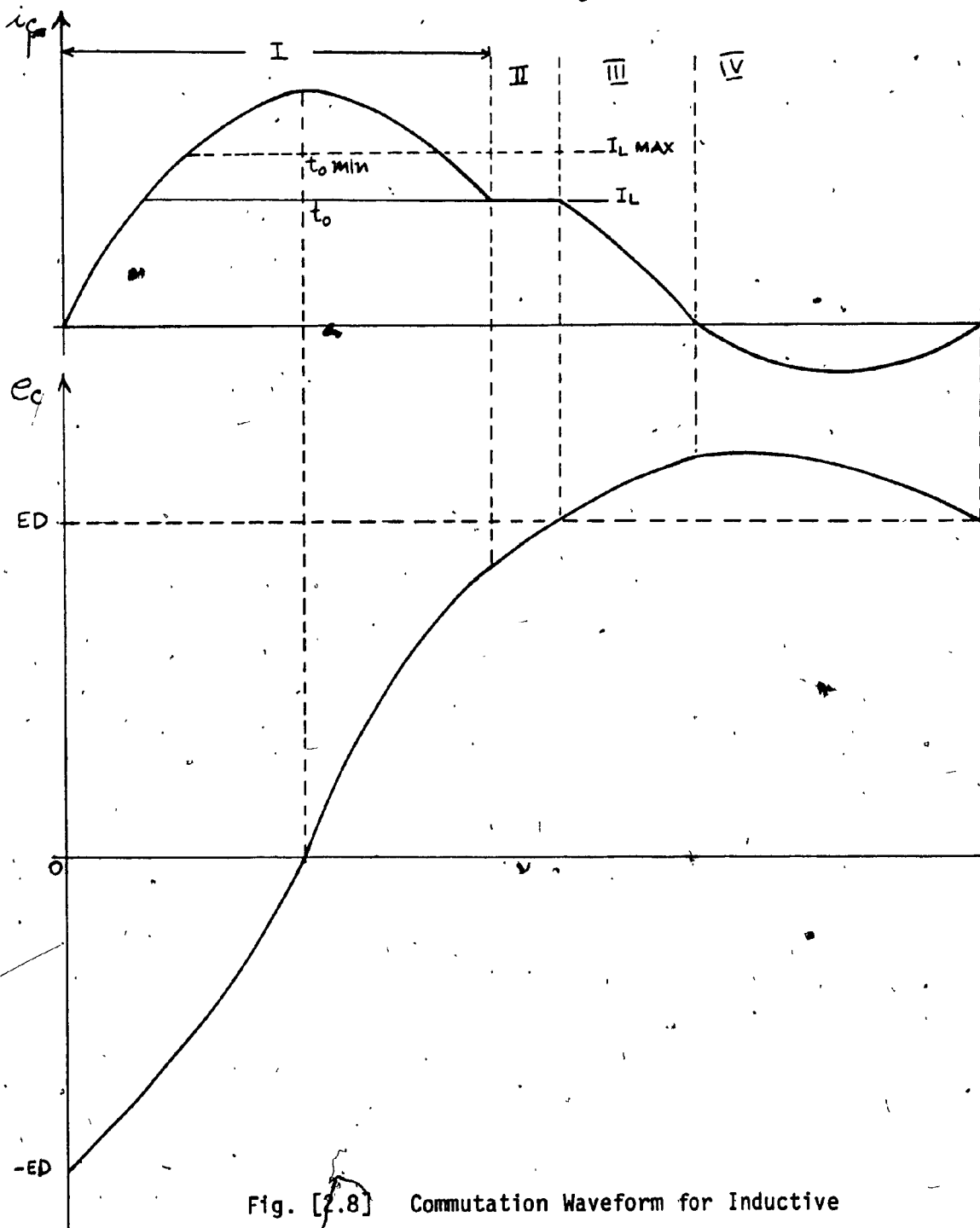


Fig. [2.8] Commutation Waveform for Inductive Load (Natural Firing).

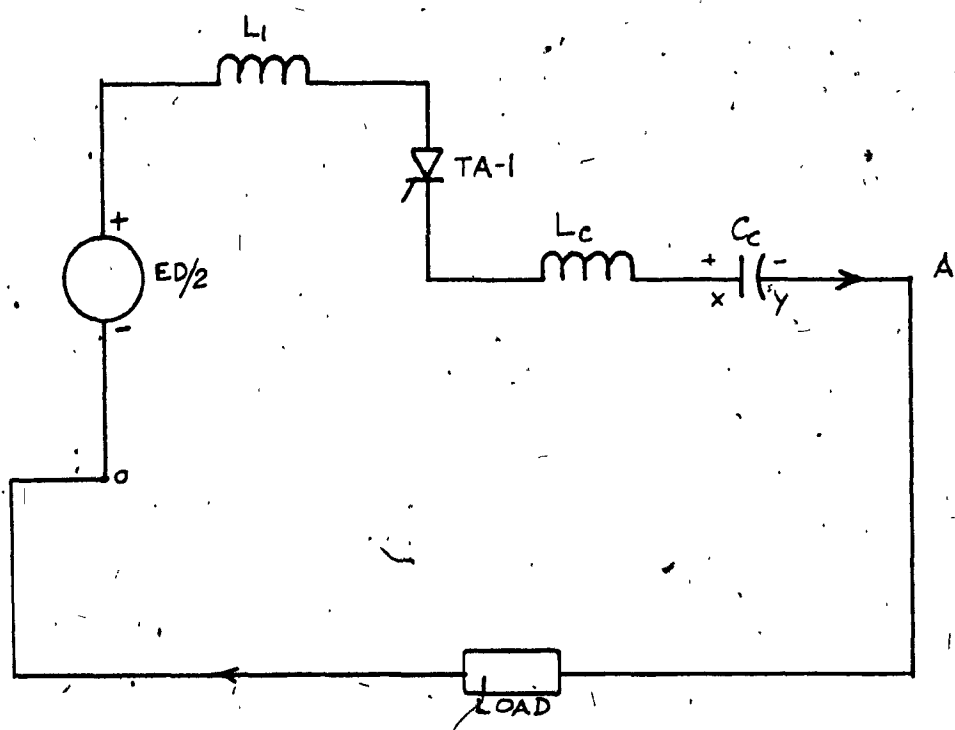


Fig [2.9] Equivalent Circuit of Inverter during second portion of commutation cycle. (Capacitor C_c is charged with constant current $i_c = I_L$).

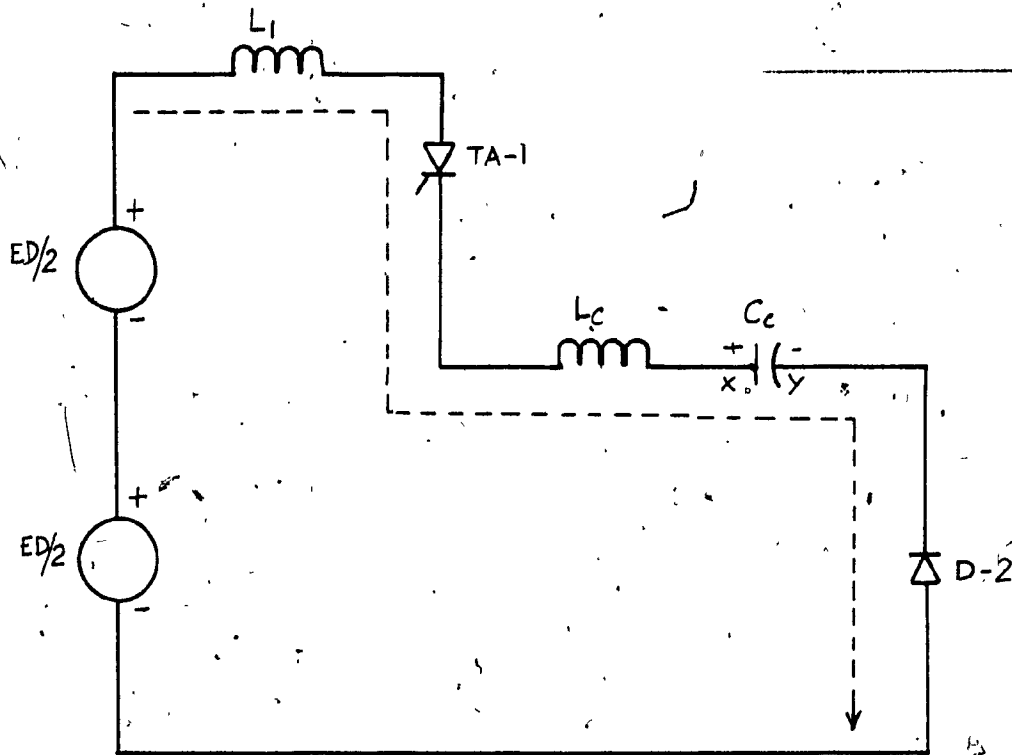


Fig. [2.10] Equivalent Circuit during the third portion of commutation cycle.

Note: Please note that net current in D-2 is in forward direction (i.e. $I_{D-2} = I_L - i_c > 0$).

ED because of the initial current in the inductance $(L_1 + L_c)$.

[fig. [2.8]: III portion of commutation cycle].

Since $e_c > ED$, the overcharge on the capacitor is fed back to the DC source through the path shown in fig [2.11] and in this process, the voltage drop across R_c and DA-1 reverse biases TA-1 and ensures its safe commutation. Finally the commutation process ends when exponentially decaying i_c falls to zero. [fig. (2.8): IV portion of commutation circle].

Now consider case II. As mentioned earlier, the capacitor discharge current i_c starts falling after reaching its peak, thereby changing the polarity of the voltage across C_c . With this scheme T-2 is fired when i_c falls to $I_{L \max}$. Since e_c is still smaller than ED (D-2 is reverse biased), T-2 starts conducting. Since D-1 would be still conducting at that moment for all load currents smaller than $I_{L \max}$, the current in D-1 is transferred to T-2. D-1 stops conducting when current in D-1 is fully transferred to T-2. Thus the commutation interval for T-1 ends [fig. 2.12: I portion of commutation cycle].

Since e_c is still less than ED, i_c starts increasing again through T-2 till e_c becomes equal ED. When e_c is equal to ED, i_c starts falling again while the capacitor voltage continues to build up. When i_c becomes equal to I_L , e_c is already greater than ED, so that D-2 starts conducting (thereby commutating T-2) [fig. 2.12 : II portion of commutation cycle]. From this point onwards, the operation

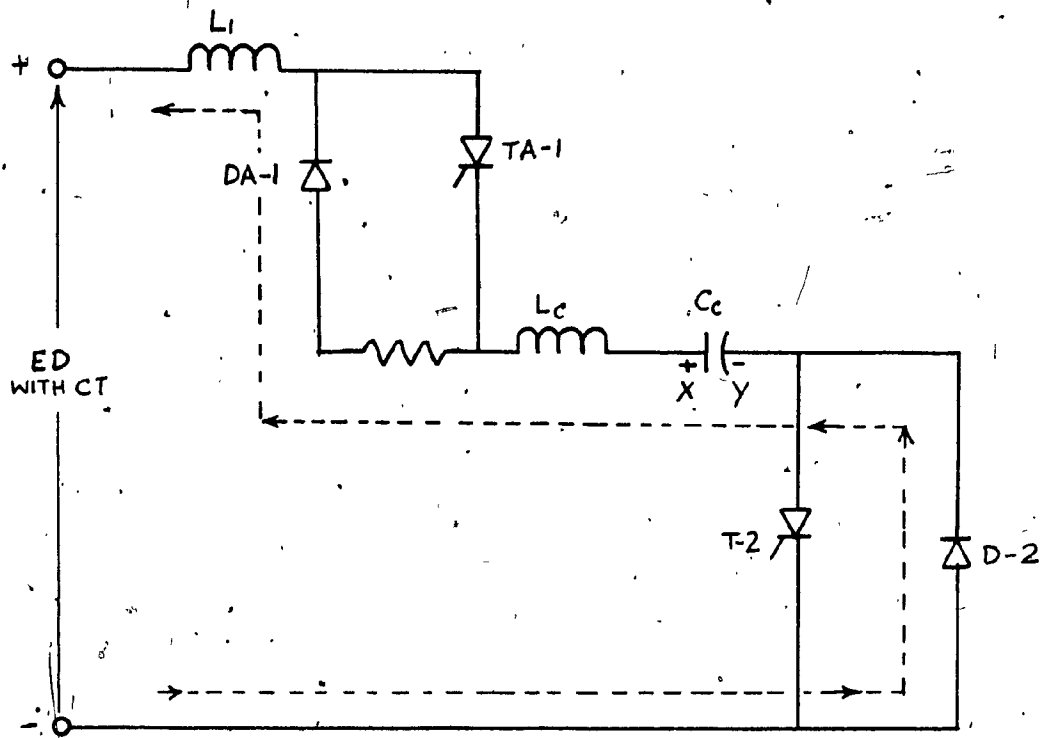


Fig. [2.11] Path during return of over charge on capacitor [IV portion of commutation cycle].

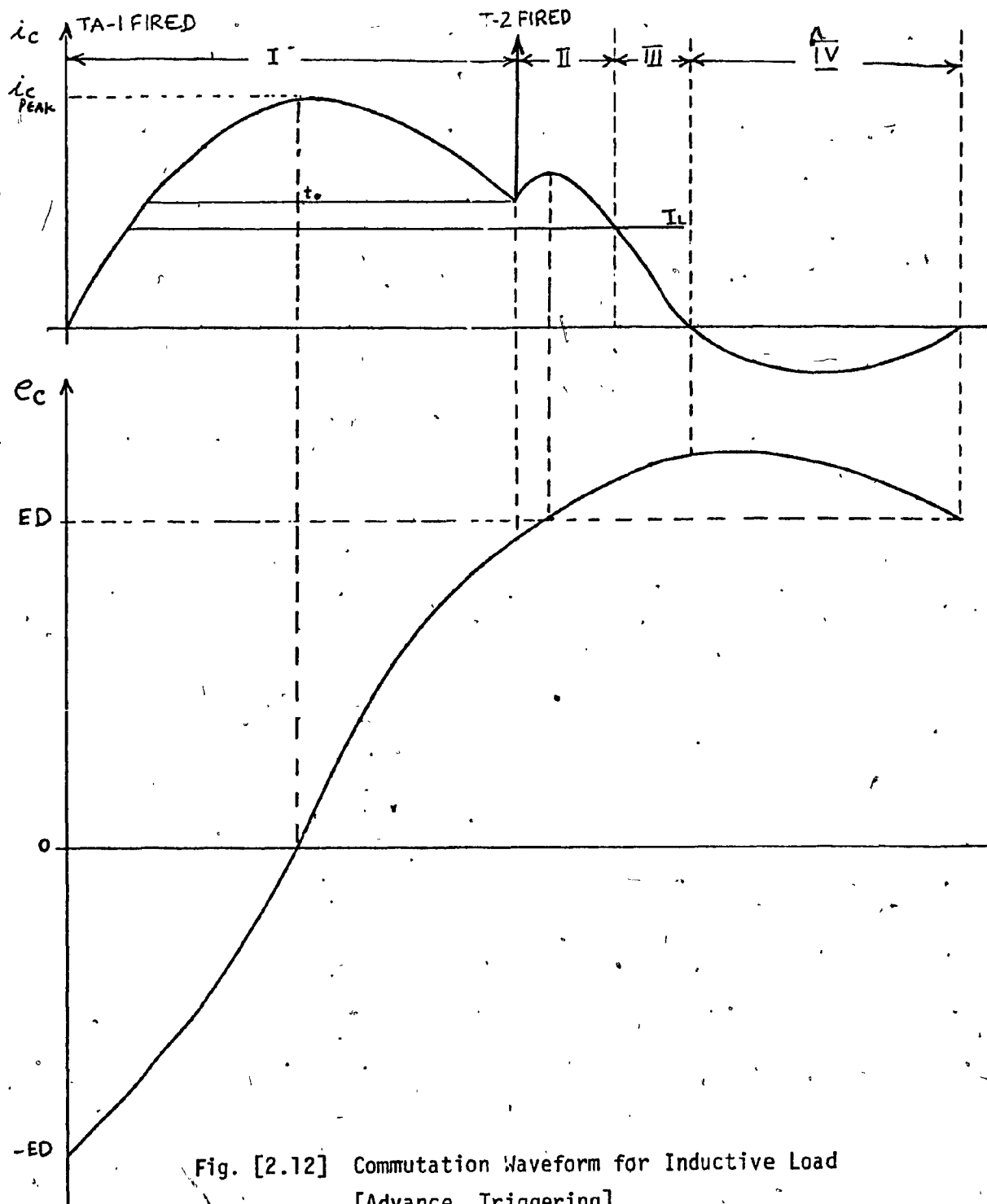


Fig. [2.12] Commutation Waveform for Inductive Load [Advance Triggering].

of the commutation circuit is identical to one described in case I and the commutation waveforms for third and fourth portion of the commutation cycle for this are given in fig. [2.12].

Thus, at the end of the commutation cycle for T-1, the polarity of the capacitor voltage is such that it is ready to commutate T-2 and the process of commutating T-2 is analogous to that described for T-1.

2.5. Analysis of the Commutation Circuit:

In the analysis of the commutation circuit, the capacitor voltage and current can be calculated at each instant during commutation. The analysis is useful for sizing of the commutation components.

For analysis purpose, the commutation circuit can be modeled as a RLC series circuit connected to a DC source E . The circuit is shown in fig. [2.13] and consists of a capacitor C , inductor L and resistor R (representing losses), Connected in series to a source of DC voltage E . The initial voltage on the capacitor is E_i and the initial current is I_i , with polarities as indicated in fig [2.13]. The differential equation for the circuit is given by

$$E = E_i + \frac{1}{C} \int_0^t i_c(t) dt + L \frac{d i_c}{dt} + R i_c \quad \text{Eqn. 2.1}$$

with initial condition $i_c(+0) = I_i$.

Using Laplace Transform, the Laplace transform of equation [2.1] is

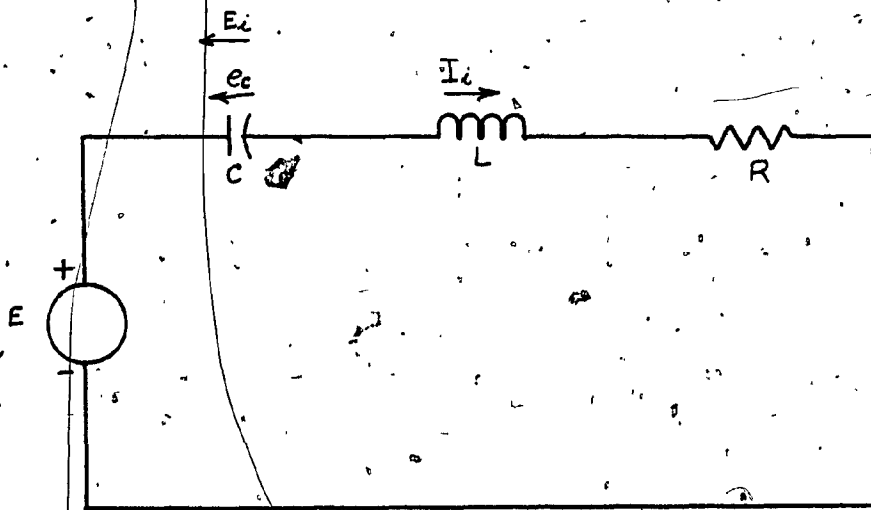


Fig. [2.13] RLC Series Circuit with dc source E used for analysis of commutation circuit.

given by

$$\frac{E - E_f}{s} = \frac{1}{sC} i_c(s) + L [s i_c(s) - I_f] + R i_c(s) \quad \text{Eqn. 2.2}$$

Solving the equation [2.2] for $i_c(s)$, the Laplace transform of $i_c(t)$,

$$i_c(s) = \frac{\frac{E - E_f}{L} + s I_f}{s^2 + \frac{R}{L} s + \frac{1}{LC}} \quad \text{Eqn. 2.3}$$

Assuming the oscillatory case the inverse transform of equation [2.3]

is

$$i_c(t) = \frac{E - E_f}{\omega L} e^{-\alpha t} \sin(\omega t) - I_f \frac{\omega_0}{\omega} e^{-\alpha t} \sin(\omega t - \phi) \quad \text{Eqn. 2.4}$$

where;

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad \text{or} \quad \omega_0^2 = \frac{1}{LC}$$

$$\alpha = \frac{R}{2L}$$

$$\omega^2 = \omega_0^2 - \alpha^2 > 0,$$

$$\phi = \text{Tan}^{-1} \left(\frac{\omega}{\alpha} \right) \quad \text{and we define}$$

$$x = \sqrt{L/C} \text{ and } Q = \frac{x}{R} \quad \text{Eqn. 2.5}$$

The expression for voltage e_c on capacitor C is obtained in a similar manner and is given by

$$e_c(t) = E - (E - E_i) \frac{\omega_0}{\omega} e^{-\alpha t} \sin(\omega t + \phi) + \frac{I_i}{\omega C} e^{-\alpha t} \sin(\omega t) \quad \text{Eqn. 2.6}$$

The equations [2.4] and [2.6] are valid for all modes of commutation cycle and only the initial conditions and some parameter values are different for each mode. These equations are now applied to the specific conditions of the commutation circuit of the inverter of fig [2.1] with inductive load (natural firing) and R_0 will represent the lumped resistance in the commutation circuit (i.e., R_0 is the equivalent total resistance of series combination of L_c and C_c).

During the starting of the inverter, the equivalent circuit of the inverter is shown in fig [2-4]. Here the initial conditions are

$I_i = 0$ and $E_i = 0$ and the parameters are

$$E = ED$$

$$L = L_1 + L_c$$

$$C = C_c$$

$$R = R_0$$

The capacitor voltage and current any time during this portion can be calculated using equations [2.6] and [2.4]. At the end of this portion, when i_c falls to zero, the final voltage on capacitor e_{c_1} (starting) will depend on Q [Eqn. 2.5] and will be approximately equal to twice the supply voltage [E_D].

Since capacitor voltage is greater than supply voltage, the excess charge on capacitor is fed back to the DC supply. The equivalent circuit of the inverter during this portion is shown in fig [2.5].

Here the initial conditions are

$$E_i = e_{c_1} \text{ (starting) and } I_i = 0 \text{ and the parameters are}$$

$$E = E_D$$

$$L = L_1 + L_c$$

$$C = C_c$$

$$R = R_o + R_c$$

The capacitor voltage and current any time during this portion can be calculated using equations [2.6] and [2.4]. At the end of this portion, when capacitor current falls to zero, the final voltage on capacitor e_{c_2} (starting) will depend upon Q [Eqn. 2.5] and will be slightly less than supply voltage. Now the polarity of the

capacitor voltage is such that it is ready to commutate T-1 .

In order to commutate T-1, TA1 is fired and the first portion of commutation cycle starts. The equivalent circuit of the inverter, after TA-1 has been fired, is shown in fig [2.6]. During this portion of the commutation cycle, the initial conditions are

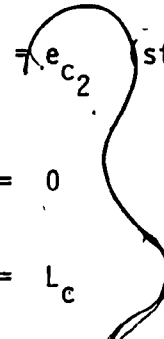
$E_i = e_{c2}$ (starting) and $I_i = 0$ and the parameters are

$E = 0$

$L = L_c$

$C = C_c$

$R = R_0$



The capacitor voltage and current any time during this portion can be calculated using equations [2.6] and [2.4]. The capacitor current i_c after reaching its peak value starts falling and when i_c is equal to load current (I_L), D-1 stops conducting. This marks the end of the first portion of commutation cycle. The capacitor voltage $e_c(t_1)$ at this time is less than the supply voltage [E_D] and the time t_1 (at which i_c is equal to I_L) depends on load current (I_L). During second portion of commutation cycle, since the capacitor voltage is less than the supply voltage, the capacitor starts charging through the load. The equivalent circuit of the inverter during this

portion of commutation cycle, the initial conditions are

$$E_i = e_c(t_1) \text{ and } I_i = I_L \text{ and the parameters are}$$

$$E = E_D$$

$$L = L_1 + L_C + L_L \text{ [} L_L \text{ is inductance in the load]}$$

$$C = C_C$$

$$R = R_0$$

The capacitor voltage any time during this portion can be calculated from equation [2.6]. This portion of commutation cycle ends when the capacitor voltage $e_c(t_2)$ is equal to supply voltage $[E_D]$. Since capacitor voltage is equal to supply voltage and capacitor current is equal to I_L , D-2 starts conducting and the third portion of commutation cycle starts. During this portion of commutation cycle, the equivalent circuit of the inverter is shown in fig [2.10]. Here the initial conditions are

$$E_i = e_c(t_2) = E_D \text{ and } I_i = I_L \text{ and the parameters are}$$

$$E = E_D$$

$$L = L_1 + L_C$$

$$C = C_C$$

$$R = R_0$$

The capacitor current i_c continues to decay through the path shown in fig [2.10]. When i_c falls to zero, this marks the end of this portion of commutation cycle. The capacitor voltage $e_c(t_3)$ at this time will depend on the load current and will be greater than supply voltage $[E_D]$. Since capacitor voltage $[e_c(t_3)]$ is greater than supply voltage $[E_D]$, the excess charge on the capacitor will be fed back to the DC supply and the fourth portion of commutation cycle starts. The equivalent circuit of the inverter during this portion of the commutation cycle is shown in fig [2.11]. Here the initial conditions are

• $E_i = e_c(t_3)$ and $I_i = 0$ and the parameters are

$$E = E_D$$

$$L = L_1 + L_C$$

$$C = C_C$$

$$R = R_O + R_C$$

Finally the whole commutation process will stop when capacitor current i_c falls to zero. The capacitor voltage $e_c(t_4)$ at this time will depend upon Q [Eqn. 2.5] and now the polarity of capacitor voltage is such that it is ready to commutate T-2 .

Thus the capacitor voltage and the current can be calculated at each instant during the entire commutation process.

CHAPTER III

Design of Power Circuit

3.1 Introduction: The principles involved in the design of the power circuit are presented in this chapter and practical design considerations are discussed. The power circuit [fig [2.1]] consists of the following components.

- Main thyristors T-1 and T-2
- Feedback diodes D-1 and D-2
- Auxiliary thyristors TA-1 and TA-2
- Clamping diodes DA-1 and DA-2
- Commutation capacitor C_c
- Commutation inductor L_c
- Damping resistor R_c

The determination of ratings of these components and the selection of these components are important for reliable, economic and efficient operation of the circuit. The packaging of the power unit is also an important part of the successful design [16]. It plays an important role in the efficient operation and maintainance of the inverter and therefore, it should be planned carefully. The location of the components and wire runs are important to minimize the noise pick up at high frequency. The requirements of power circuit meant for PWM are first outlined, then followed by the determination and selection

of the ratings of the components.

3.2 Requirements of Power Circuit for PWM (Pulse-Width Modulation).

The power circuit intended for pulse width modulation should satisfy the following requirements.

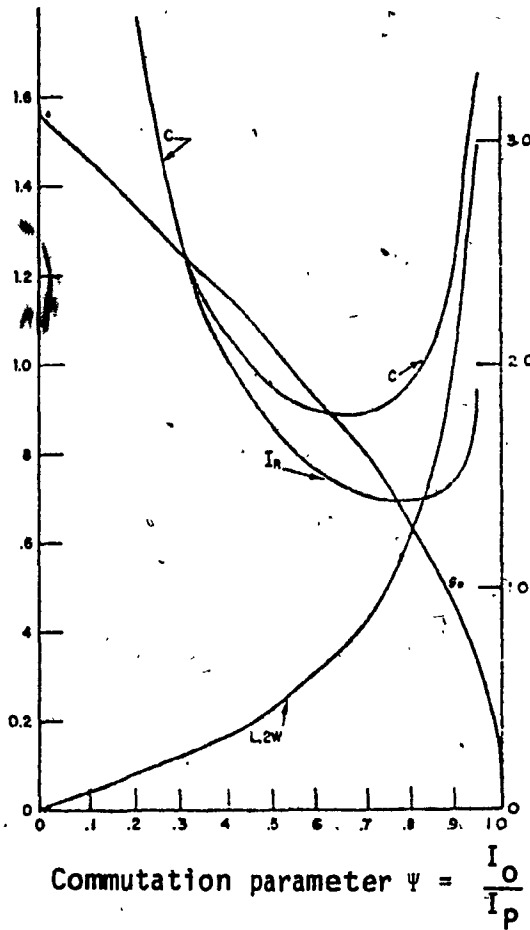
- 1) Low energy loss per commutation.
- 2) Low stored energy in the commutation capacitor.
- 3) Commutating ability is to be adequate at all operating conditions.
- 4) Have a low output impedance.

The first three requirements relate to commutation circuit, while the fourth one relate to power circuit.

3.3 Selection of Commutation Circuit Components.

This involves the determination and selection of the ratings of C_c , L_c and R_c . The commutation circuit is designed by assuming that commutation circuit has high quality factor (Q). For efficient design, Q should be at least equal to Ten [24]. As shown in section [2.4], the successful commutation of main thyristors require that the $L_c C_c$ discharge current should exceed load current for an interval which is longer than the turn-off time of the main thyristors. Selection of commutation circuit components is based on a set of design curves, given in fig [3.1] and fig [3.2], [16]. In fig [3.1], the independent

$$C_c \left(\frac{E_D}{I_0 t_0} \right), L_c \left(\frac{I_0}{E_D t_0} \right) \cdot M \left(\frac{1}{E_D I_0 t_0} \right)$$



$$\theta_0 = \omega_0 t_0, I_R \left(\frac{1}{I_0} \sqrt{\frac{I}{t_0}} \right)$$

Fig. [3.1] Commutation Circuit Design Curve.

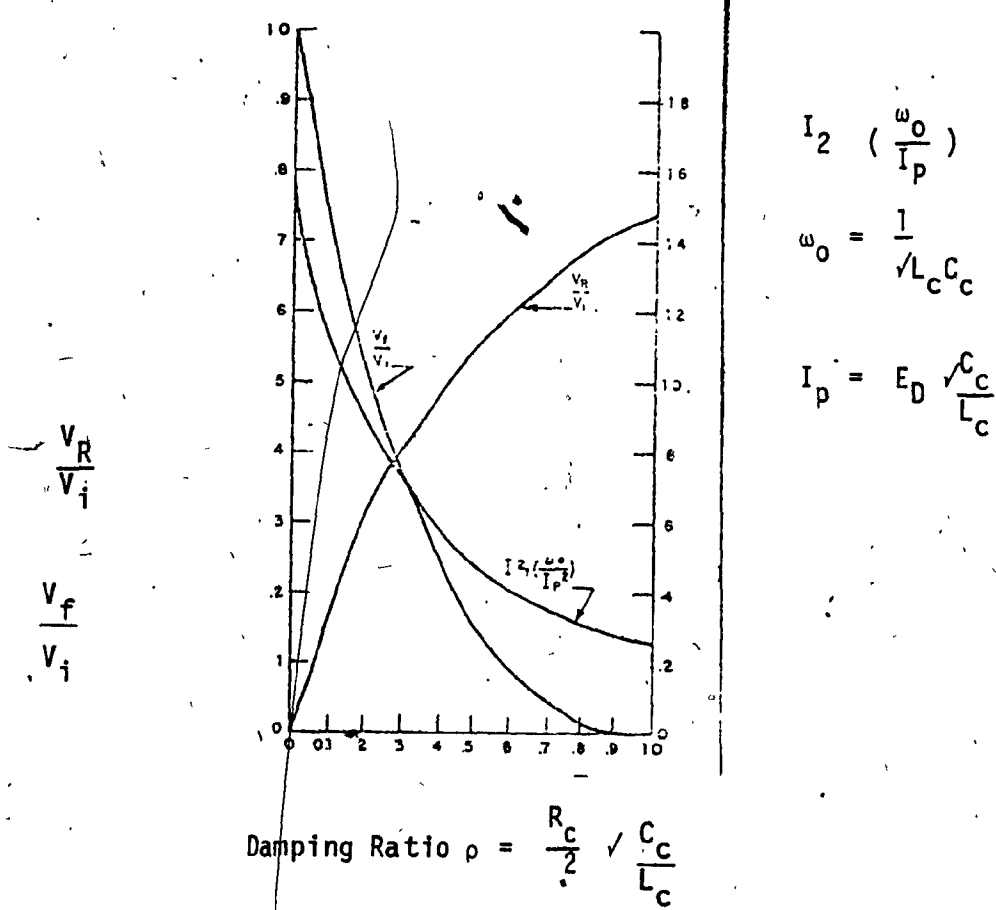


Fig. [3.2] Commutation Circuit Design Curve.

variable is the commutation parameter (ψ), which is defined as

$$\psi = \frac{\text{Maximum load current to be commutated}}{\text{Peak commutating current}} = \frac{I_o}{I_p} < 1$$

The dependent quantities are the value of L_c and C_c , the trapped (stored) energy (W) and the no load RMS current in the commutation thyristors (I_R). The RMS current in L_c and C_c is equal to $\sqrt{2} I_R$. One approach leading to efficient circuit design is to minimize energy stored in the commutation capacitor C_c . As illustrated in fig [3.1], this can be achieved by selecting ψ values corresponding to the minimum commutation capacitor value. Therefore a value of ψ equal to 0.7 is selected in this case.

From curves [fig [3.1]], for $\psi = 0.7$,

$$C_c \left(\frac{E_D}{I_o t_o} \right) = .9 \quad \text{Eqn. 3.1}$$

i.e. $C_c = \frac{.9 t_o I_o}{E_D} \quad \text{Eqn. 3.2}$

and

$$L_c \left(\frac{I_o}{E_D t_o} \right) = .4 \quad \text{Eqn. 3.3}$$

i.e. $L_c = \frac{.4 t_o E_D}{I_o} \quad \text{Eqn. 3.4}$

where the values of components are

C_C = Value of commutating capacitance in micro farad
(μF).

L_C = Value of commutating inductance in micro henries.
(μH).

E_D = Value of dc supply voltage in volts.

I_O = Value of Max. load current in Amps.

t_o = Value of circuit turn off time in microseconds
(μS)

The dc supply voltage E_D is fixed by the available power source; the maximum load current I_O is defined by operating conditions (over loads, harmonics etc.); ' t_o ', the available time for turn off (circuit turn off time) is determined by the 'turn-off' time (t_q) of the thyristor selected for the circuit. ' T ' is the period of switching frequency (chopping frequency). Knowing these quantities, C_C , L_C and I_R can be calculated. At this point, the currents, voltages and frequency needed for specifying the capacitor (C_C) and inductor (L_C) are known. Other considerations require that discharge path during fourth portion of commutation cycle [Section 2.4 & 2.5] be adequately damped so that the thyristors [Aux.] are not subjected to high voltages. The value of damping resistor R_C (in ohms) can be calculated from

$$P = \frac{R_C}{2} \sqrt{\frac{C_C}{L_C}}$$

Eqn. 3.5

where P is damping factor.

There are some trade offs to be made in the selection of R_C . Figure [3.2] is a graph of V_f/V_i and V_R/V_i as a function of the damping factor. The voltage V_i is the magnitude of the overshoot of the capacitor voltage e_C above E_D . V_f is the magnitude of the undershoot of capacitor voltage e_C below E_D . V_R is the peak voltage that appears across resistor R_C during the energy return portion of the commutation cycle. The curve (V_f/V_i) shows the effect of the voltage undershoot V_f as a function of V_i . The purpose of the resistor is to minimize the voltage undershoot. As the damping factor increases, the voltage (V_R) across the resistor R_C increases. This voltage adds directly to the supply voltage E_D , thereby increasing the forward voltage on the auxiliary thyristors. Also, as the damping factor increases, the time required for completion of the discharge portion of the commutation cycle also increases. For PWM operation, the inverter should complete a commutation cycle as rapidly as possible.

3.4 DESIGN SPECIFICATIONS AND CALCULATIONS.

Design Specifications:

- Single phase half bridge configuration.
- Rated output: 8 KVA

- Rated output voltage: 110 volts (RMS)
- Rated DC input voltage: $240 \pm 8\%$ volts
- Chopping Frequency: 2000 HZ [Max.]

Design Calculations

The design calculations can be done by assuming that the load is purely inductive. The inverter operating under this condition can then operate safely for any other type of load. For purely inductive load, the current waveform is triangular in shape [fig. 2.2]. Therefore for a 75 amps RMS continuous load current, the value of the peak load current is approximately 130 Amps [$\sqrt{3} \times 75$]. Now fixing the maximum commutating capability of the inverter taking into account the overload and a factor of safety 1.7, the inverter should be able to commute successfully a max load current of 225 Amps. i.e. $I_0 = 225$ Amps. Next step for design calculation is to fix ' t_0 ', the circuit turn off time. Thyristors for inverter applications having a guaranteed turn off time (t_0) of 20 microseconds are presently available in the market at a reasonable price. Therefore for reliable commutation, choose $t_0 = 25$ microseconds. This is because during commutation, the feed back D-1 and D-2 which are connected antiparallel with T-1 and T-2 limit the reverse voltage applied across thyristors T-1 and T-2 to its forward voltage drop and there by increases the turn off time of thyristors. Finally the value of E_D can be fixed. A DC power supply of 240 volts [$\pm 8\%$] with centre-tap is available. Since the commutation capability diminishes with input supply, the value of E_D can be fixed at minimum value of power supply. i.e. $E_D = 220$ volts.

Now the required values of C_c and L_c can be calculated from equations [3.2] and [3.4]. Therefore,

$$C_c = \frac{0.9 \times 25 \times 225}{220}$$
$$= 23.01 \mu F$$

and $L_c = \frac{0.4 \times 25 \times 220}{225}$

$$= 9.77 \mu H$$

Hence the values of C_c and L_c can be selected as follows:

$$C_c = 25 \mu F$$

and $L_c = 9 \mu H$

Now with these values of C_c and L_c selected, we can once again check for I_o . i.e.

$$I_o = \frac{C_c \times E_D}{.9 \times t_o} = \frac{25 \times 220}{0.9 \times 25}$$

$$= 244.44 \text{ Amps, and } I_o = \frac{0.4 \times t_o \times E_D}{L_c}$$

$$= \frac{0.4 \times 25 \times 220}{9} = 244.44 \text{ Amps.}$$

Thus, we are sure that, with selected values of C_c and L_c , we can commutate the required I_0 . Now keeping in view the trade offs mentioned for selection of the value of R_c , a damping factor of $P = 0.7$ is selected from curves [fig [3.2]]. This gives the value of R_c as 0.84 ohm.

In order to verify that the commutation time offered by the circuit (t_0) is within specified limit (i.e. $t_0 \geq t_q$), a computer programme was written. The selected values of L_c , C_c , R_c , E_D etc were used in the computer programme. The programme calculated the values of i_c and e_c at each instant during entire commutation. Programme results verified the suitability of selected values for above components. The computer programme is included in the appendix [III].

3.5 COMPONENT SELECTION

3.5.1 Commutation Capacitor.

For the selection of commutation capacitor, the following points are important. Fig [3.3] represents a simplified equivalent circuit of a capacitor where C is the capacitance of an ideal capacitor; R_1 is the ESR [Equivalent series resistance] of the plates, leads etc; R_2 is the insulation resistance sometimes measured by measuring a leakage current and L is the equivalent series inductance of the plates. Capacitors

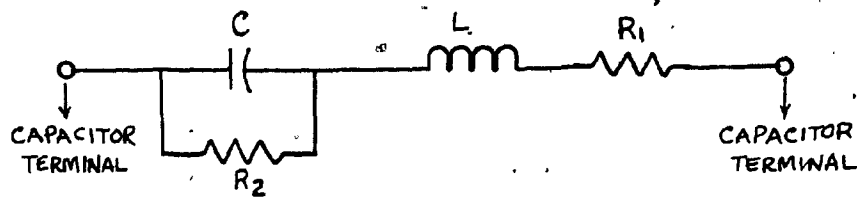


Fig. [3.3] Equivalent Circuit of a Capacitor.

used in commutation circuit should have minimum ESR and minimum L (Equivalent series inductance). The commutation losses depend on ESR thus to minimize the losses, ESR must be minimum. The ESR determines also the capacitor time constant RC and thus the speed by which a capacitor can discharge. Since for high frequency operation, commutation periods are short. One again should minimize the ESR. Therefore, when selecting capacitor for commutation, one has normally to select capacitors specially made for thyristor circuit applications. Hence commutation capacitors made by G.E. Co. (General Electric Company) were used in this design.

The following are the specifications of the commutation capacitor required:

Capacitance: 25 μ F (microfarad)

RMS Current: 105 Amps [Fig (3.4)]

Peak Current: 325 Amps

Peak voltage (AC): 600 volts

On the basis of the specifications for the commutation capacitor, two 10 μ F capacitors (G.E 28F5723FC) and one 5 μ F capacitor (G.E 28F5122FC) were selected for the purpose. The capacitors were connected in parallel to form a capacitor bank of 25 μ F with a capability of 150 Amps RMS.

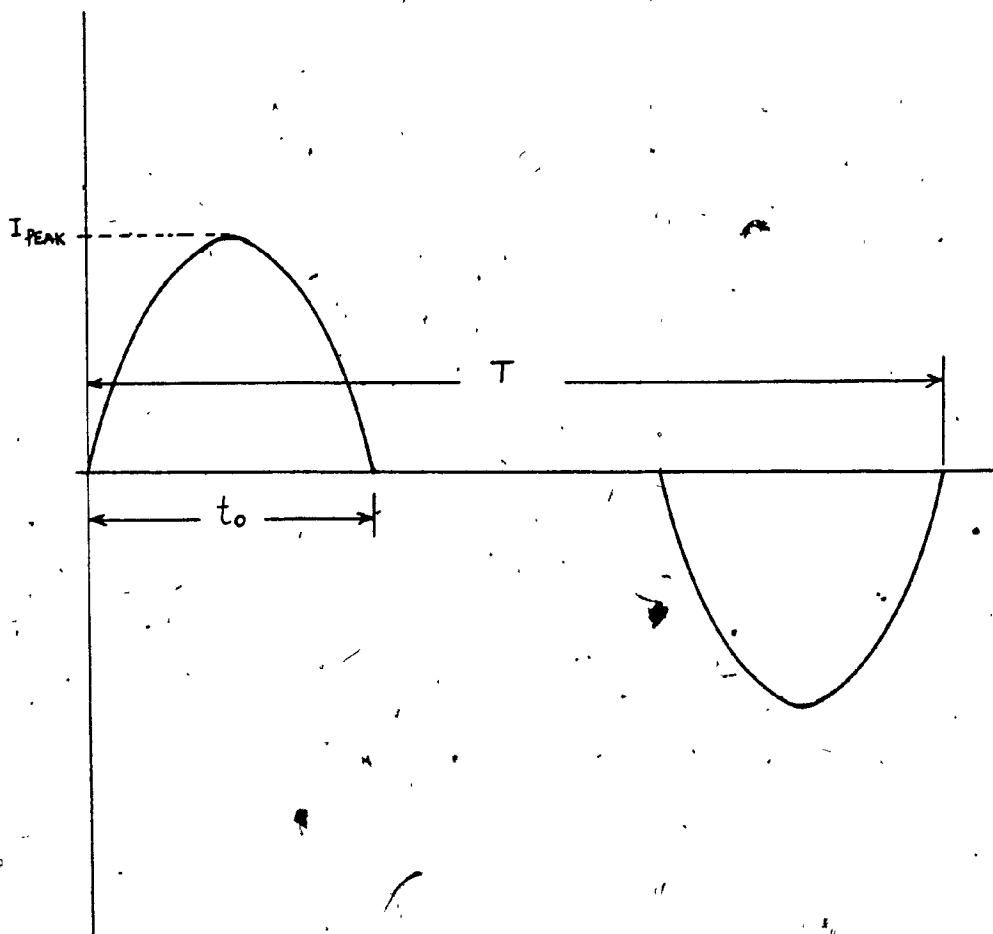


Fig. [3.4] Approximate Current Waveform of Capacitor Discharge Cycle.

$$I_{\text{peak}} = \frac{225}{.7} = 321.43$$
$$= 325$$

$$t_0 = \pi \sqrt{L_c L_c} = \pi \sqrt{25 \times 9} = 47.12 \mu\text{s}$$
$$= 50 \mu\text{s}$$

$$T = 500 \mu \text{ sec}$$

$$I_{\text{RMS}} = I_{\text{peak}} \sqrt{\frac{t_0}{T}} = 325 \cdot \sqrt{\frac{50}{500}} = 102.77$$
$$= 105 \text{ Amps RMS}$$

3.5.2 Commutation Inductor.

The commutation inductor operates at high frequency and carries commutation current. Commutation losses depend on Q of the inductor. In order to minimize losses, Q should be high (i.e. resistance of inductor should be low). The cable or wire used for inductor should be preferably stranded. This is to minimize the effective resistance at high frequency. Air core inductor wound with stranded wire was used in this design. The calculations showed that an inductor of 9 (nine) microhenries is required. The air core inductor was obtained by using a number 2 phillips cable. This cable has 1633 strands and can carry 160 Amps. of RMS current continuously. Two layers of 6 (six) turns in each layers on a 3 (three) inch diameter plastic core gave the value of 9 (nine) microhenries. While mounting this inductor, care should be taken so that no magnetic material is placed in the path of the inductance loop.

3.5.3 Damping Resistor.

From the calculations, the value of the damping resistance required is .84 ohms. An ohmite adjustable vitreous enameled resistor of one ohm (type 210) was

selected for this purpose.

3.5.4 Main Thyristors.

In addition to carrying the load current, the main thyristors carry also the current pulse for charging the commutation capacitor during the inverter starting. Under the maximum commutating capability, the main thyristor carries a current of 225 Amps plus the charging current of 325 Amps for about 50 microseconds [$\pi\sqrt{L_c C_c}$ seconds]. Thus, in this period the thyristor peak current is 550 Amps for about 50 micro seconds. The peak inverse voltage to which the thyristors will be subjected, is equal to e_c peak. In addition to this, we have to consider the repetitive reverse recovery transients which occur every time the feed back diode recovers [chapter 4]. With proper protection (Suppression), the peak reverse voltage of the main thyristors can be limited to 550 volts and therefore the thyristor PRV rating should be at least equal to 600 volts. The turn off time requirements of the thyristors is 20 microseconds. Under the worst case, the current waveform of a main thyristor is shown in fig [3.5].

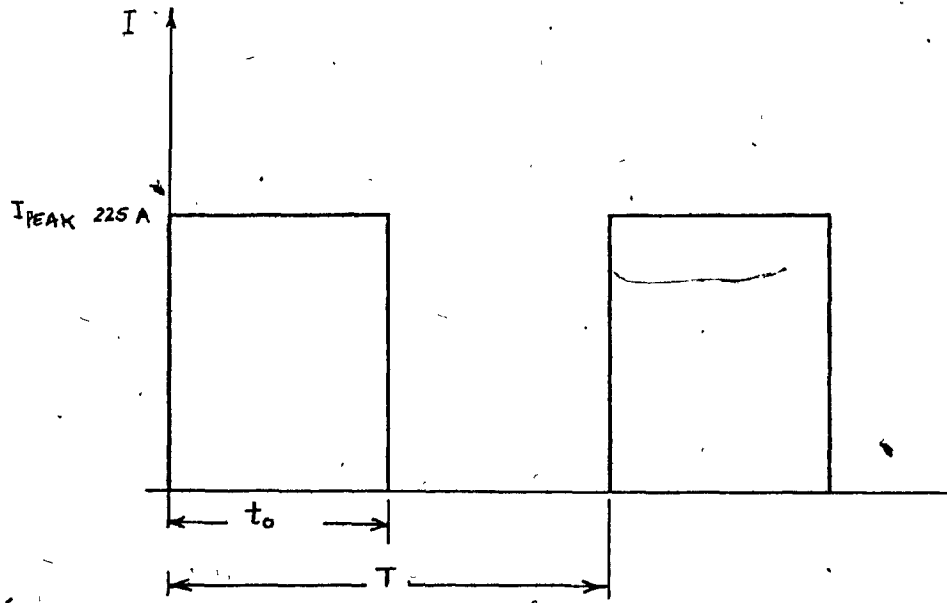


Fig. [3.5] Current Waveform for Purely Resistive Load.
(For Main Thyristor) duty cycle = 50%.

$$t_o = T/2$$

$$I_{\text{peak}} = 225 \text{ Amps}$$

$$I_{\text{av}} = I_{\text{pk}} \times \frac{t_o}{T}$$

$$= 225 \times 1/2 = 112.5 \text{ Amps}$$

$$I_{\text{RMS}} = I_{\text{pk}} \sqrt{\frac{t_o}{T}}$$

$$= 225 \sqrt{1/2} = 225 \times .707$$

$$= 160 \text{ Amps RMS.}$$

The following are the principal specifications for the main thyristors.

Peak reverse voltage = 600 volts.

Average current = 112.5 Amps.

RMS current = 160 Amps.

Peak (Max) Current = 550 Amps for 50 microseconds.

Turn-off time ' t_q ' = 20 microseconds.

On the basis of the above specifications, GE (General Electric Co.) C-365M Hockey Puck model was selected for the main thyristors (i.e. for T-1 and T-2). The detailed specifications of this thyristors are included in appendix [II].

3.5.5 Auxiliary Thyristors.

The auxiliary thyristors carry capacitor discharge current and load current during commutation. Figure [3.6] shows the current waveform of an auxiliary thyristor. The following points are important in the selection of the auxiliary thyristors.

The auxiliary thyristor conducts a high peak, narrow current pulse.

For successful PWM operation, the auxiliary thyristor should recover quickly and it should have low switching losses.

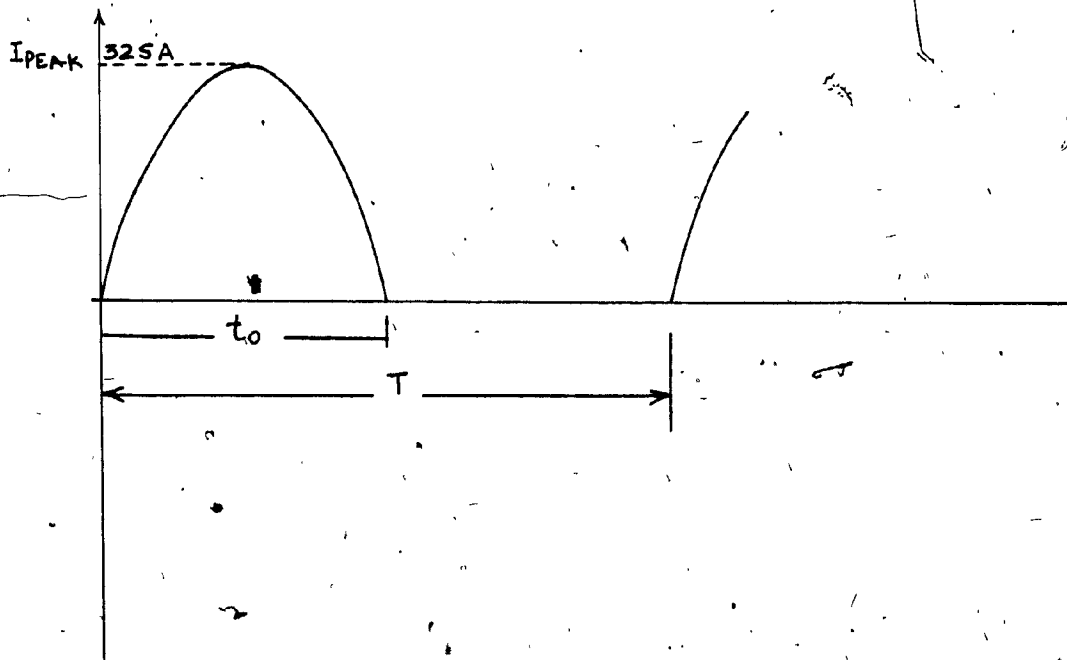


Fig. [3.6] Approximate Current Waveform Of Auxillary Thyristor:

$$t_o = 50 \mu \text{ sec.}$$

$$T = 5000 \mu \text{ sec. (} f_{\text{chop}} = 2000 \text{ Hz).}$$

$$I_{\text{RMS}} = I_{\text{pk}} \sqrt{\frac{t_o}{2T}}$$
$$= 75 \text{ Amps}$$

$$I \text{ Average} = \frac{2 I_P t_o}{\pi T}$$
$$= 25 \text{ Amps.}$$

Since the commutation circuit tends to ring, the auxiliary thyristors are often required to have a high voltage rating. Specially the blocking voltage requirement of the auxiliary thyristors is equal to the capacitor voltage e_c (peak). Normally a 30% safety margin is used for the thyristor voltage rating. Keeping above considerations in mind, the same thyristor model (GE C-365M) was selected for auxiliary thyristors. One of the main reason behind the selection is that the packaging of the complete (power) unit becomes more efficient and compact with both auxiliary and main thyristors having the same case (hockey puck case).

3.5.6 Feed Back Diodes.

During the commutation of a main thyristor, the feed back diode carries the difference between the commutation current i_c and the load current I_L [section 2.4]. When selecting a feed back diode, it is extremely important to specify those with short turn off time and with soft declination current characteristics. The reason for this is that the diode with short turn off time and soft declination current characteristics minimizes the transient

($L di/dt$) voltage in the external circuit, L being the inductance in the external circuit. By this way the transients and re-applied dv/dt to which thyristors are subjected is reduced to a great extent. A discussion on the need to use the fast recovery diodes in inverter circuits is well documented in [25] and [26]. Therefore a fast recovery diode with a blocking voltage of 600 volts and a current carrying capability of 100 Amps (average) at full load is required in this design. However, since a diode with this current rating is not available in a hockey puk case, a fast recovery diode with 400 Amp (average) has been selected. It has a voltage rating (blocking) voltage of 600 volts. By specifying a hockey puk case rather than a stud type, the inductance between the main thyristors and feed back diodes can be minimized. Further more, the consistency in the case type means the packaging of the entire assembly (power unit) much more compact.

3.5.7 Clamping Diodes.

During the fourth portion of commutation cycle [section 2.4], the over charge on the commutation capacitor is returned to the dc supply through the clamping diode. The current requirement of this

diode should be such that it can withstand I^2t of the maximum current pulse. At the same time such diodes should be of fast recovery type, so as to reduce the transients due to reverse recovery. The fast recovery diodes IR 12FL60 made by International Rectifier Co. was selected for this purpose. It has a current rating of 12 Amps (Ave.) and a blocking voltage of 600 Volts. This selection has been found to be satisfactory.

3.6 A Note on Inverter Losses.

The losses in the inverter are due to

- 1) Losses in the semiconductors.
- 2) Losses in the snubber circuit.
- 3) Losses in the commutation circuit.

1) Losses in the semiconductor: These losses are caused by thyristor switching, forward drop across the thyristors and diodes and by the reverse recovery of the solid state devices.

2) Losses in the snubber circuit: Each thyristor and diode has a snubber circuit connected across it for protection against dv/dt : [chapter IV] Losses

associated with snubber circuit are given by

$$P_{\text{snubber}} = f c E_c^2 \text{ where}$$

f = frequency of operation in HZ.

c = capacitance in the snubber circuit in farads.

E_c = Peak switching voltage in volts.

As the switching frequency increases, losses also increase. Losses in the snubber circuit can be reduced by optimizing the value of the snubber components. [chapter IV].

3) Losses in commutation circuit: Losses in the commutation circuit depends on quality factor Q of the commutation inductor. To minimize losses, Q should be high (i.e. resistance of the commutation inductor should be low).

NOTE: Specifications of components is included in appendix [II].

CHAPTER IV

PROTECTION CIRCUITS

4.1 Introduction: The protection circuits of the inverter are discussed in this chapter. The protection circuits can be grouped as follows:-

- 1) Protection of thyristors against excessive di/dt .
- 2) Protection of thyristors against excessive dv/dt and voltage spikes due to switching transients.
- 3) Protection of the thyristors from fault currents.

These are considered below.

4.2 The Protection of the thyristors against Excessive di/dt

Conduction of anode current in the thyristors commences in the immediate neighborhood of the gate connection and spreads from there across the whole area of the junction. Thyristors are so designed that the conduction area spreads as rapidly as possible, nevertheless if the current density at the gate junction during 'turn-on' is too high, local hot spots will be formed in the neighborhood of the gate connection. This localized heating may result in failure of the thyristors or, in the absence of failure, can cause a high switching loss. It is for this reason that the maximum value of ' di/dt ' below which the thyristor will not be damaged, is specified by manufacturer.

Di/Dt values may be limited to a safe range by adding a small inductance (di/dt inductance) in the anode circuit. Further more, the problem can be minimized by using fast rising, maximum amplitude (hard-drive) gate pulses to trigger a thyristor. Such pulses increase the speed by which the conduction spreads across the junction and thus minimize thyristor 'turn-on' time. The details regarding the design of hard-drive gate circuits are documented in [23]. Finally the di/dt problem can be further minimized by selecting a thyristor with an amplifying gate. Thyristors with an amplifying gate have a high built-in di/dt withstand capability. Further details on thyristors with an amplifying gate are documented in [2]. However a brief note on thyristors with an amplifying gate are included in appendix [I A].

All three di/dt protection measures mentioned above have been taken in this project. Both auxiliary and main thyristors have been selected with an amplifying gate structure, resulting in a very high allowed value for di/dt. Hard driving gate pulses, with a rise time of 0.1 microsecond and an amplitude of about 20 volts are used [chapter V]. Finally a small (5 μ H), saturable inductor is connected in the circuit as shown in fig [2.1]. The inductor is designed to saturate just below the rated current, so as to minimize the voltage drop during normal thyristor conduction [27]. Note also that this inductor contributes to the short circuit impedance and this plays an important role in the fuse co-ordination.

4.3 Protection of Thyristors from Excessive dv/dt and Voltage Spikes due to Switching Transients.

Thyristors are very sensitive to fast rising forward applied voltages either during turn-on or commutation interval. There is some inherent capacitance between junctions of the thyristor. A fast rising voltage impressed on this junction capacitance results in a current, $i = c \, dv/dt$. If this current is sufficiently large, a regenerative action may occur causing the thyristor to switch to the "ON" state. This regenerative action is similar to that which occurs when gate current is injected to turn the thyristor on. This is called dv/dt turn on and is explained in [2]. This dv/dt turn on is non-destructive but in certain circuits, may result in mal function of the circuit. This is especially true for the case of the inverter described in this project. Thyristors in this inverter circuit experience transients due to (fast) commutation and due to reverse recovery problem of feed back diodes.

Transients due to fast Commutation.

During commutation, when the capacitor (C_c) discharge current (i_c) exceeds the load current (I_L) and reaches peak, it starts decreasing there by changing its slope. If the stray inductance between main thyristor and (feed back) diode is significant, creates a steep rising positive voltage across the main thyristor. This voltage might turn on the thyristor again resulting in commutation

failure, there by causing short circuit across dc supply. Next the transients due to reverse recovery of feedback diodes are explained in the next paragraph.

Transients due to reverse, recovery of feed back diodes.

The transients due to reverse recovery of a semiconductor junction diode can be explained briefly as follows:- In a semiconductor junction diode, forward current is carried by minority carriers being injected from the junction. During the conduction, there is a certain amount of 'pile-up' of these carriers in the vicinity of the junction. This represents a stored charge. If the current was to stop flowing suddenly, the diode can not recover its reverse voltage blocking capability instantaneously because of this stored charge. Therefore a current flows in the diode in the reverse direction until all the stored charge is swept away. Depending on the circuit parameters and the amount of stored charge, the cessation of reverse recovery current may be very abrupt, in which case a very high di/dt induces large voltage transients across the inductances in the path of the reverse recovery current. This type of transients due to reverse recovery of the (feed back) diodes are experienced in this inverter circuit and this is explained in the next paragraph.

During the commutation of the main thyristor T-1, the difference between the capacitor (C_c) discharge current (i_c) and the load current (I_L) is carried by the feed back diode D-1. At a point, $i_c = I_L$; [fig (4.1a) and fig (4.1b)], the current in diode reduces to zero and diode momentarily conducts in reverse direction [fig [4.1b]].

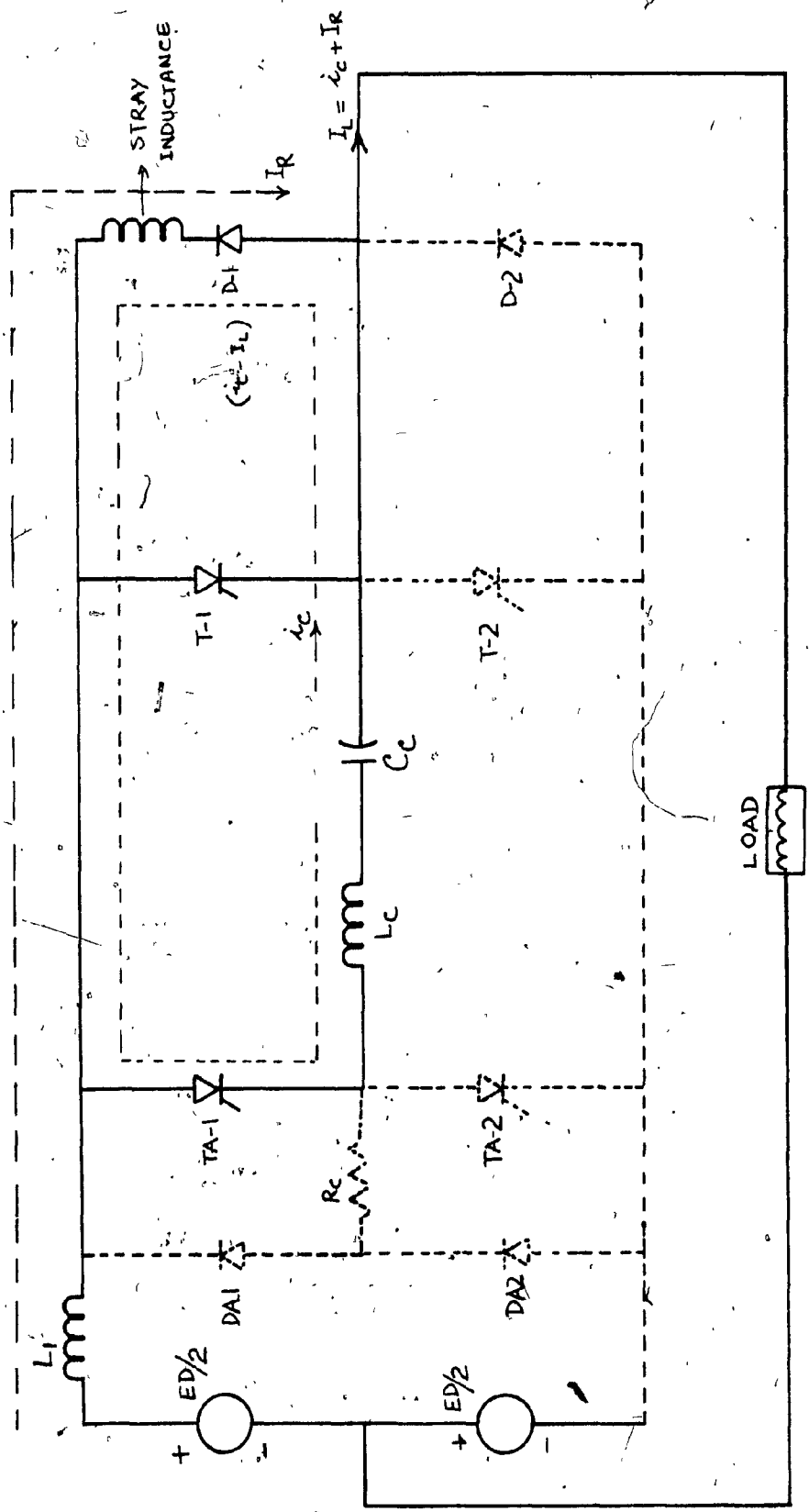


Fig. [4.1a] Transients due to reverse recovery of feed back diodes.

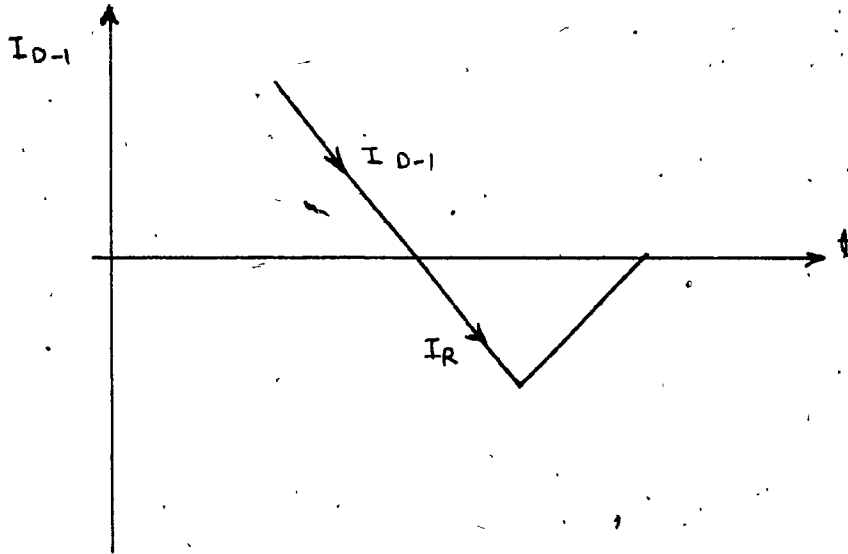


Fig. [4.Jb] Transients due to reverse recovery of feed back diodes.

Now $I_L = i_C + I_R$ where I_R is the recovery current. When I_R reaches its peak in the negative direction, it changes its slope and at that point the current $[i_C + I_R]$ drops to the value less than I_L . Therefore the load voltage changes its polarity.

$[L_{\text{stray}} \frac{d I_{D-1}}{dt}$ and $L_{\text{Load}} \frac{d I_L}{dt}]$ are applied across the main thyristor in a fraction of a microsecond. Such a high rate of rise of voltage (dv/dt) can cause a thyristor to turn on again resulting in a commutation failure which causes a direct short circuit of the dc supply.

It is also important to keep dv/dt of the thyristor as low as possible even when a thyristor may be capable of a much greater dv/dt value, since the fast rising voltages (dv/dt) represents a high powered noise signal which is coupled to low level signal circuitry through stray capacitances between the two circuits [28].

As a solution to dv/dt problem, it is generally necessary to connect a snubber circuit across a power diode and a thyristor to absorb the energy associated with the recovery current of the device and to limit dv/dt . Various snubber circuit configurations are available but the basic one consists of a series RC network. Another solution to dv/dt turn on problem is to select a thyristor with higher dv/dt capability. For example, thyristors with Shorted-Emitter structure have a high dv/dt withstand capability [2]. The dv/dt withstand capability of the thyristor can be also increased by applying a

a negative bias on the gate of thyristor. There are circuits which apply a negative gate bias only while dv/dt is being applied. The basic idea of these circuits is to differentiate the dv/dt applied to the anode, invert the polarity and then apply it to gate. The details of negative gate bias techniques are documented in [2] and [23].

Therefore, considering the above facts, the problem of reducing dv/dt on thyristors in this inverter circuit can be solved by using the RC network or negative bias. RC networks are excellent for dv/dt suppression at low switching frequencies but when the frequency is increased above 400 HZ, the losses become significant. Thus the RC network alone will not solve the problem effectively for frequencies above 400 HZ. In such cases the combination of RC network and the negative gate bias techniques can be employed. This protection method is employed for the inverter in this project. The circuit which combines both techniques is fully described in [29]. However both description, operation and selection of components for this circuit are included in appendix [I. B].

4.4 Protection of Thyristors from Fault Currents.

It is very important to protect thyristors from fault currents due to short circuit and commutation failure. Commutation failure can be due to dv/dt turn on or due to an overload beyond the stored energy capability of the commutation circuit. The thyristors will be carrying

a short circuit current and therefore they have to be protected by a proper fuse. It is a well known fact that semiconductor components have a relatively small thermal storage capacity and therefore they can not be overloaded beyond the maximum device ratings. Due to high values of a fault current, a non-uniform current distribution is formed at the junction of the semiconductor. The junction then gets damaged either because of these abnormal current densities or because of high junction temperature, which is proportional to the product I^2t . Because of this effect, very rapid removal of fault current is essential. This necessitates the use of high speed fuses. The basic function of these fuses is to limit the rated continuous current allowed to pass through the device and to interrupt, safely, very high prospective fault currents.

The protection to the thyristors from fault currents is provided by selecting fuses of proper rating. Details on fuse operation and selection are included in appendix [I C].

CHAPTER V

DESIGN AND IMPLEMENTATION OF THE FIRING CIRCUIT

5.1 Introduction: This chapter describes the design and implementation of the firing circuit. The firing circuit generates the required triggering pulses to thyristors and it also controls the starting and stopping operation of the inverter. The input signal (PWM waveform) comes to this firing circuit from a PWM controller. This waveform is timed and processed so as to generate the required triggering pulses. For design of the firing circuit, the basic requirements of the power circuit are first outlined and then the design implementation is presented.

5.2 Basic Requirements: The inverter power circuit is shown in fig. [2.1]. The commutation circuit operation is explained in chapter II. Referring to that figure (i.e., fig. (2.1)), Thyristor T-1 and T-2 are alternatively turned on to connect point 'A' to the positive or negative side of the DC supply. This inverter has then only two fully controllable states that can be utilized to generate an alternating voltage across the load. With thyristor T-1 'on' and thyristor T-2 'off', v_{A0} is positive and with thyristor T-1 'off' and thyristor T-2 'on', v_{A0} is negative. Thus this inverter can be used to generate any waveform consisting of only these two states. Fig. [5.1] shows a typical PWM waveform that can be generated by this inverter. Such a PWM output can be generated at power level by feeding the same PWM reference signal to

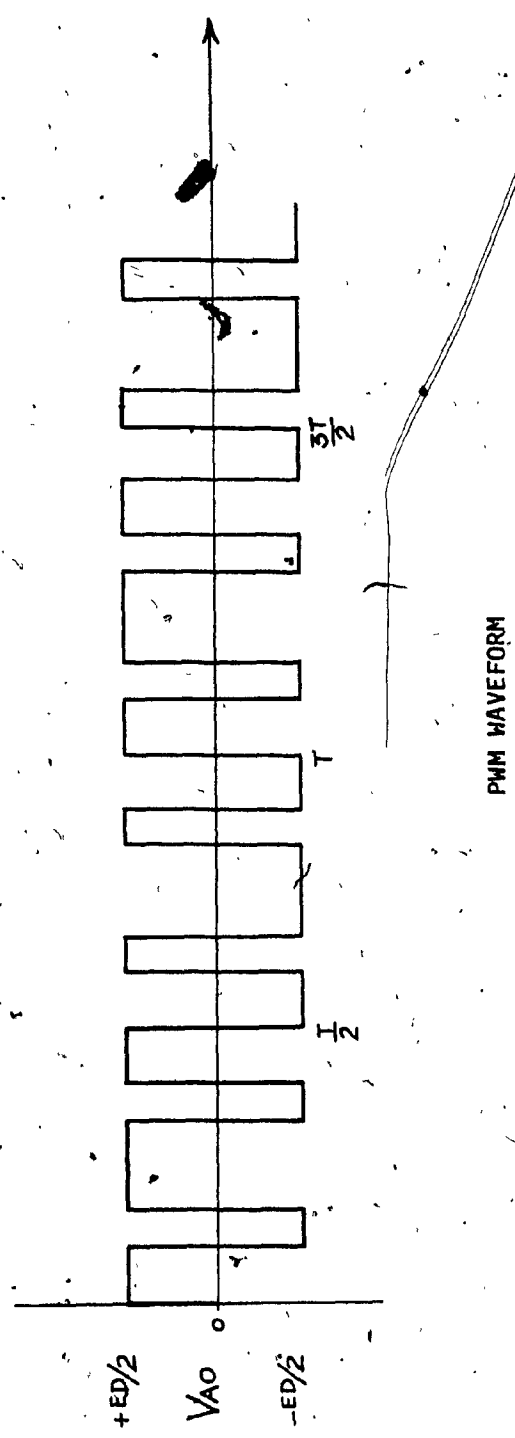


Fig. [5.1]

the input of the inverter firing circuit. This reference signal is provided by a PWM controller. After receiving the reference signal, the firing circuit has to perform three basic tasks.

They are as follows:

- Initiation of the operation (i.e., starting of Inverter)
- Regular (Sequential) operation.
- End of operation (i.e. stopping of Inverter).

Initiation of Operation: The inverter can be started at the beginning of the positive cycle of the reference waveform. When the 'start' command is given, the firing circuit waits to sense the beginning of the positive cycle of the reference waveform (i.e. it "catches" the first rising edge of the reference waveform, after 'start' command is given). Thus, the firing circuit senses the beginning of the positive cycle of the reference waveform and then sends the triggering pulses to thyristors T-1 and TA2 simultaneously. This ensures that the inverter starts always on the positive edge of the reference signal and that the commutation capacitor (C_c) is charged with correct polarity for commutation of T-1. Then the commutation of T-1 at the end of positive cycle (of reference waveform) and T-2 at the end of negative cycle (of reference waveform) during 'starting' operation is same as in regular operation which is given next.

Regular (sequential) Operation: In the regular (sequential) operation, when T-1 has to be commutated at the end of positive cycle (of the reference waveform), triggering pulse should be sent to thyristor TA-1 (i.e, the triggering pulse to TA-1 should be sent at the beginning of the negative cycle (of the reference waveform)). Then after the required delay, triggering pulses should be sent to thyristor T-2 so that T-2 can conduct on negative cycle (of the reference waveform). For commutation of T-2 at the end of negative cycle (of the reference waveform), triggering pulse should be sent to TA2 (i.e., the triggering pulse to TA-2 should be sent at the beginning of the next positive cycle (of the reference waveform)). Then after required delay, triggering pulses should be sent to thyristor T-1 so that T-1 can conduct on next positive cycle (of the reference waveform). Thus in this way, the inverter starts operating in regular mode.

End of operation: Since the inverter operation is started at the beginning of the positive cycle (of the reference waveform), the inverter operation can be terminated at the end of negative cycle (of the reference waveform) by commutating T-2 (i.e, it should be stopped by firing TA2 and afterwards no pulses should be sent to any other thyristors). When the 'stop' command is given, the firing circuit waits to sense the beginning of the positive cycle of the reference waveform (i.e., it "catches" the first rising edge of the reference waveform, after 'stop' command is given). Thus, the firing circuit senses the beginning,

of the positive cycle of the reference waveform and then sends triggering pulse to TA-2 only. Fig. [5.2] shows the timing diagram of the required pulses during starting, regular and stopping operation of the inverter.

5.3 Guidelines for the Design: A firing circuit which satisfies the requirements outlined above, can be realized either by analogue or digital scheme. However, the digital scheme has the following advantages over the analogue scheme.

- Immunity against noise
- High reliability

Therefore it was decided to use digital scheme in the design. The design of the firing circuit is simple and straight forward. While designing the circuit, the following criterion was kept in mind:

- The logic circuitry should be simple
- The circuit should be realized by using low cost standard IC chips.

5.4 Implementation of the Circuit: The block diagram of the digital firing circuit is shown in fig [5.3]. It consists of three basic functional blocks. They are

- Interface Circuit
- Control Circuit
- Output Circuit

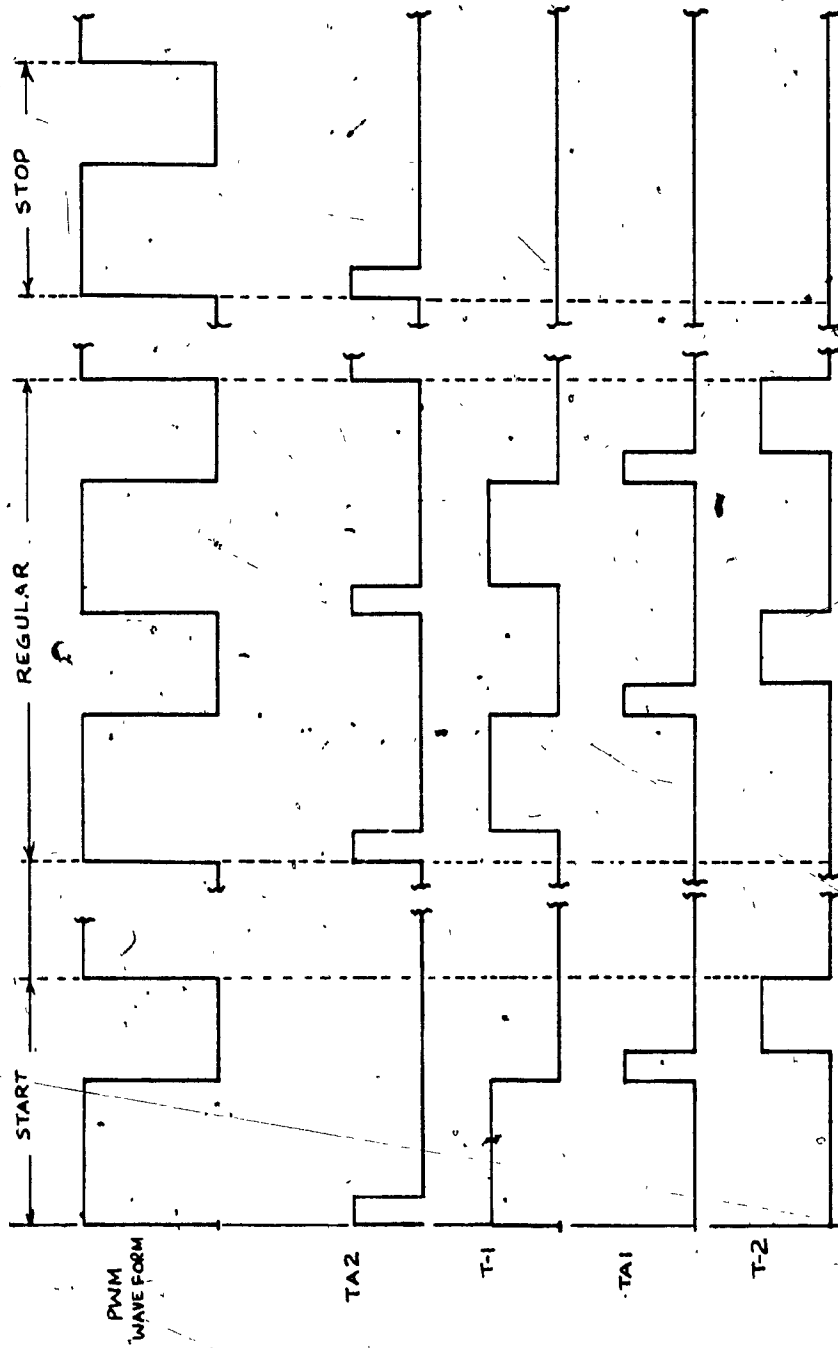


Fig. [5.2] Pulse Timing Diagram.

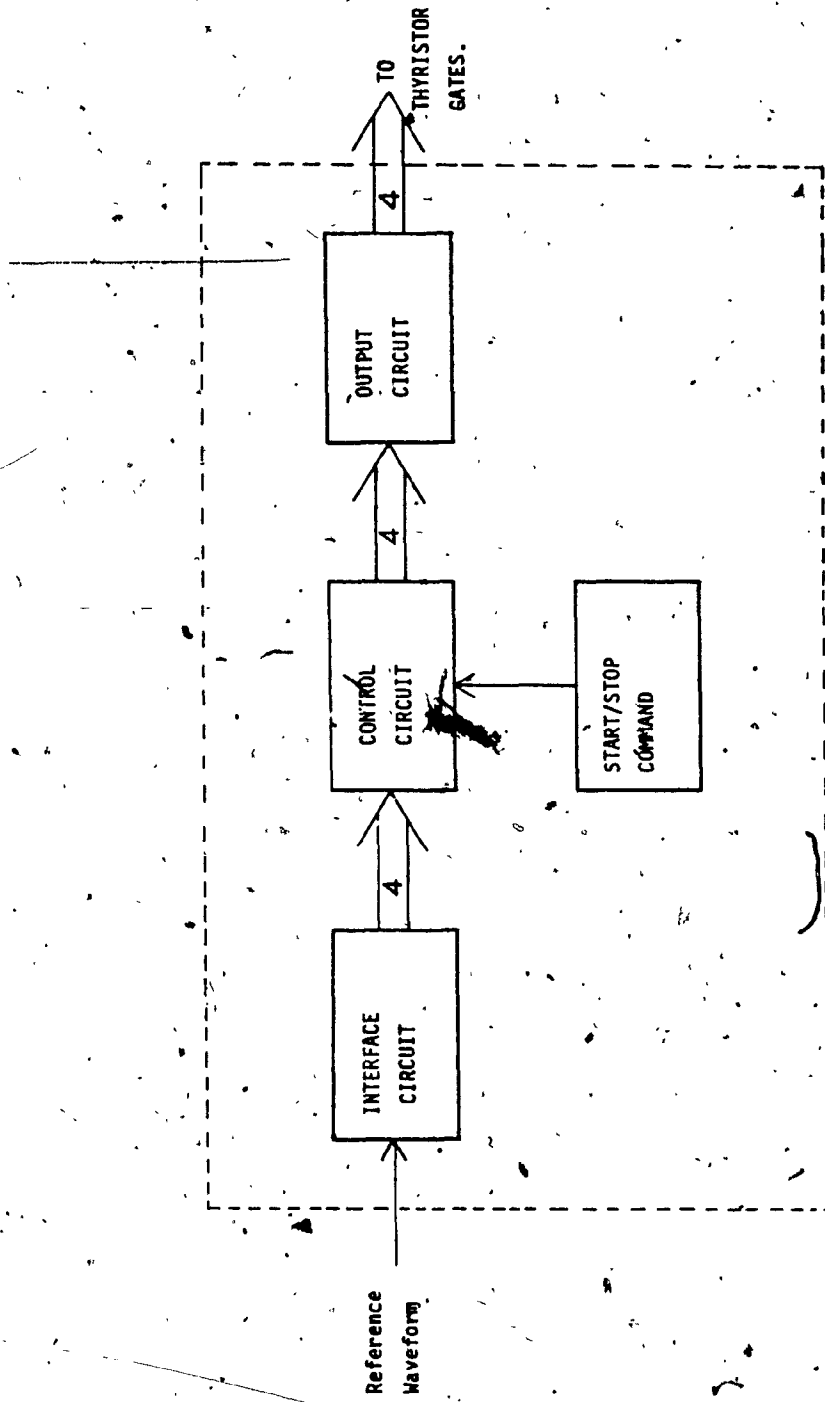


Fig. [5.3] Block Diagram of Firing Circuit.

The description and realization of each block is given below.

5.4.1 Interface Circuit:- The interface circuit is shown in fig. [5.4]. It receives the reference waveform (signal) and produces four output signals to be processed by the control circuit. The circuit is realized by using one inverter (7404) and two edge triggered mono. stable multivibrators (74123). They are connected as shown in fig. [5.4].

The first and second outputs are the non-inverted and inverted versions of the input waveform. These two signals serve also as the inputs to the two monostable multivibrators. The outputs of the monostable multivibrators (signal 3 and 4) are the adjustable duration pulses. In this application, the pulse duration can be varied between 25 and 50 microseconds by varying the connected 20 K ohms variable resistors, fig. [5.4]. The outputs from monostable multivibrators are used to trigger the auxiliary thyristors and to produce a required delay in triggering the main thyristors. Thus the triggering pulses are generated at either low to high or a high to low switching (transition) of the input waveform. The input and output waveforms for the interface circuit are shown in fig. [5.5].

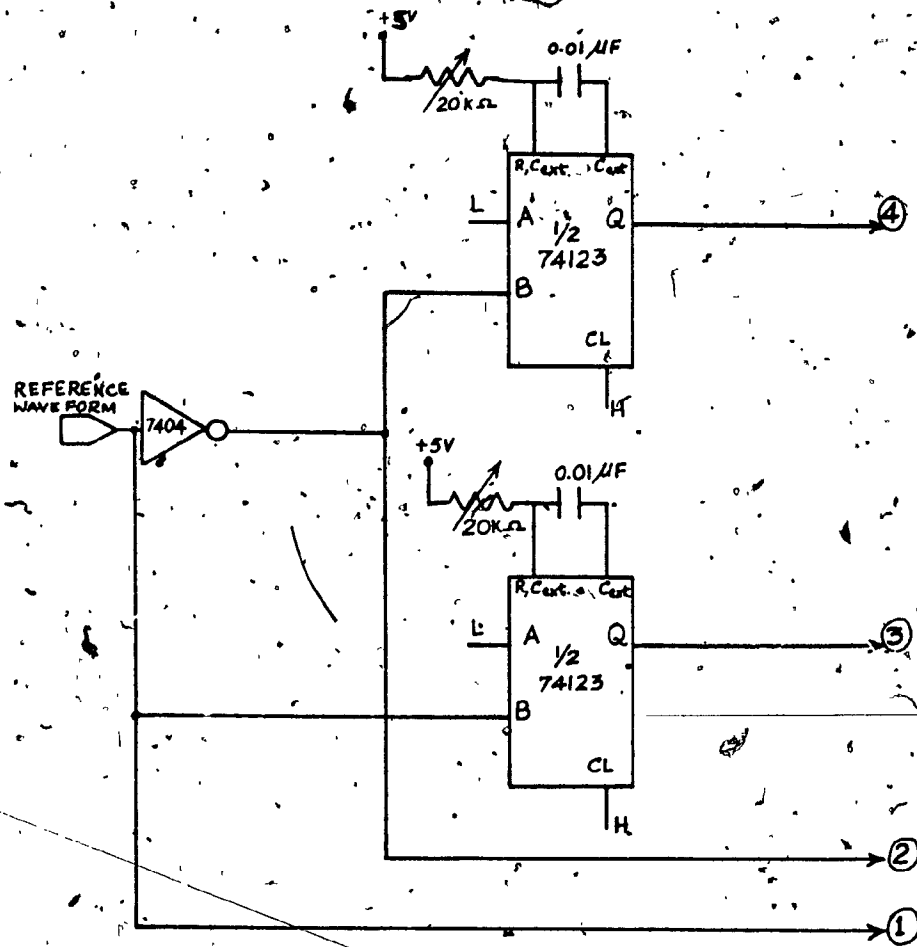


Fig. [5.4] Interface Circuit.

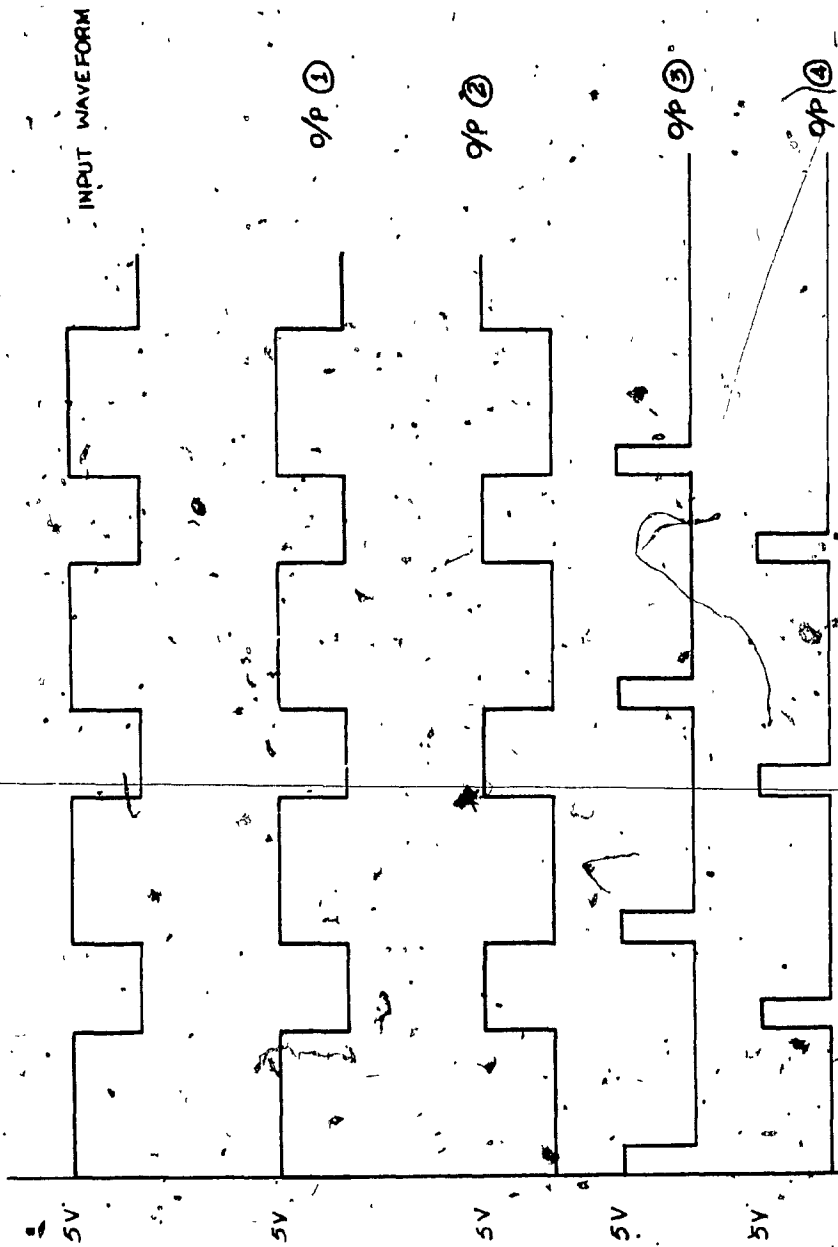


Fig. [5.5] Input and Output Waveforms of Interface Circuit.

5.4.2. Control Circuit: This circuit controls the firing of the main and the auxiliary thyristors. The schematic diagram of this circuit is given in fig. [5.6] while the timing diagram is shown in fig. [5.7]. The control circuit receives the input signals from the interface circuit, and creates the appropriate triggering pulses which are then processed by the output circuit. The control circuit is the heart of the system, fig. [5.6].

It is comprised of the following:

- (a) A start-stop switch with its debouncing circuit (gates 14, 15, 16, 17)
- (b) Two synchronizing Data flip flops.
- (c) Control logic (Gate no:1 to 13).
- (d) A master clear circuit.

The operation of these sections is as follows:

(a) A single pole, double throw switch is used to start and stop the entire operation. This switch is debounced by a latch consisting of gates 14, 15, 16 and 17. It gives a bounceless low to high transition at the output of gate 17, when the operation is started and a high to low transition when it is ended (stopped).

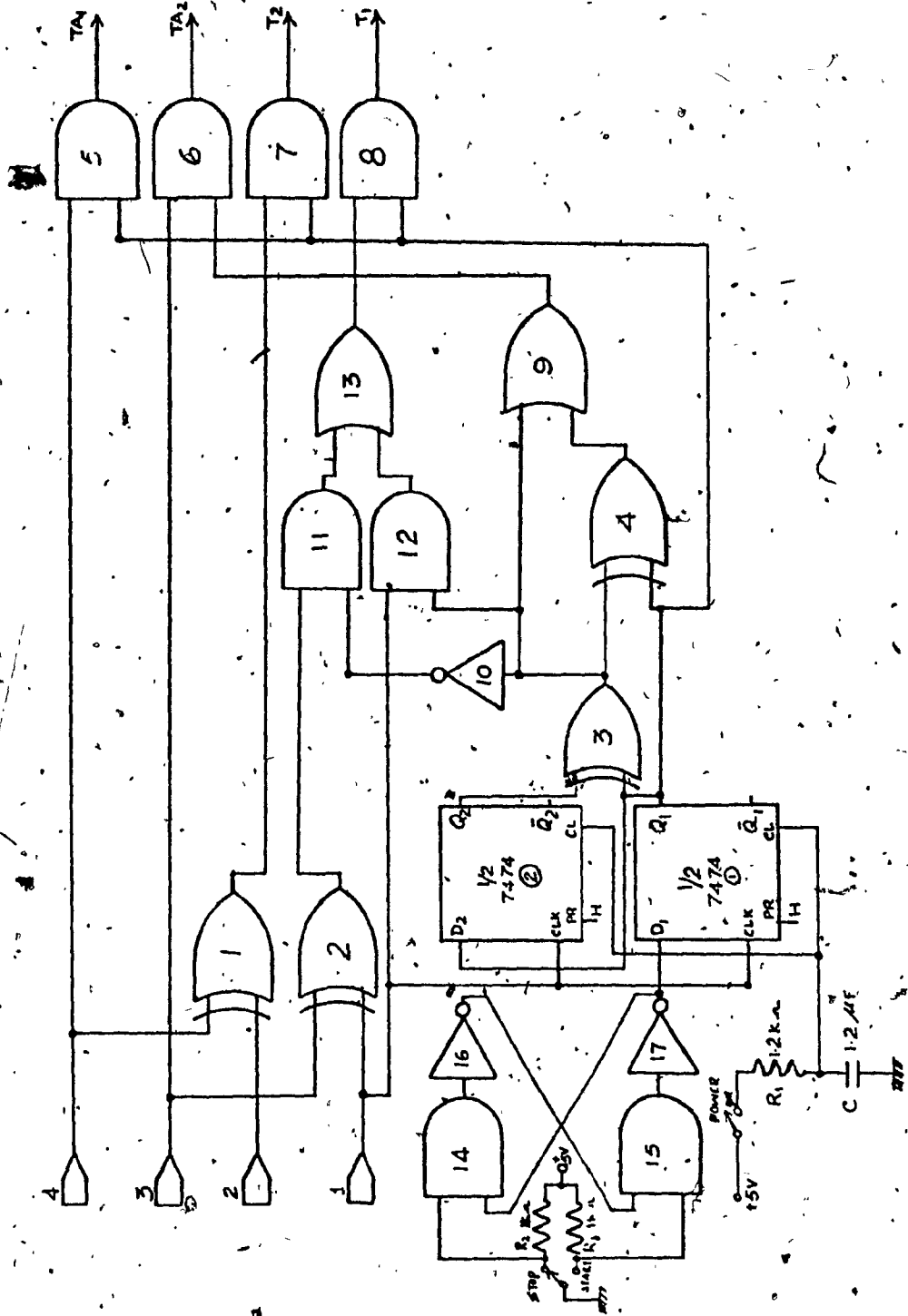


Fig. [5.6] Schematic Diagram of Control Circuit.

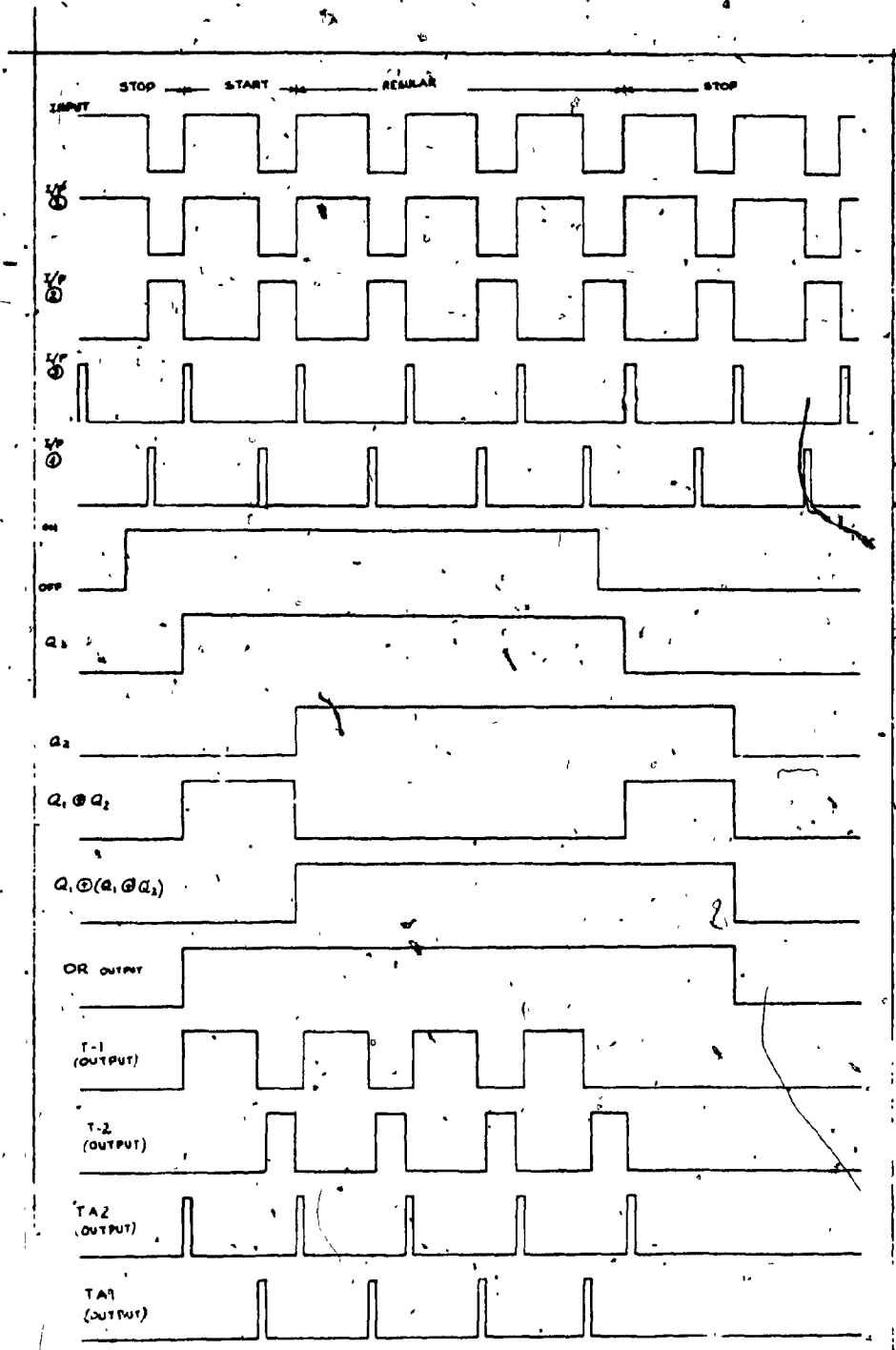


Fig. [5.7] Control Circuit Timing Diagram.

(b) The two positive edge triggered "D" flip flop (7474) are clocked with the reference waveform, which also forms the system clock. Flip-flop no:1 is synchronizing the asynchronous 'start-stop' waveform with the clock fig [5.6] and [5.7]. This means that it "catches" the first rising edge of the reference waveform after the operation has started and the first rising edge of the same waveform when it is ended (stopped). Flip flop no. 2 is clocked from the same clock but its "D" input is receiving data from the output of the first flip-flop. Thus it will "catch" the rising edge after one cycle of the reference waveform has elapsed. In other words, its output (Q 2) will be the same as the output of the first flip flop (Q 1) but it will be delayed by one clock period. These waveforms can be readily seen in the timing diagram, fig. [5.7].

(c) The control logic has the following triple task. First, when the operation starts and only for the first cycle (i.e., starting cycle), it has to trigger thyristors T-1 and TA-2 simultaneously. Second, during the regular operation, the four thyristors are fired, one after another, in the sequence - TA-2, T-1, TA-1, T-2. Third, when the operation stops and for the last cycle only, TA-2 has to be triggered while all other triggering pulses are disabled.

To fulfill the above requirements, the control logic operates in the following manner. Inputs 3 and 4 are passed straight to the

output circuit (through enabling gates 6, 5) to form the triggering pulses for thyristors TA-2 and TA-1 respectively. Inputs 2 and 4 are exclusive or'd (gate 1) to create the triggering pulse (through enabling gate 7) for thyristor T-2. Inputs 1 and 3 are exclusive or'd (gate 2) to create the triggering pulse for thyristor T-1 through the enabling gate 8. Thus, with the use of exclusive OR gates (1 and 2), the required delay in triggering thyristors T-2 and T-1 can be obtained. For example, if a delay of 25 microseconds in triggering the main thyristors T-2 and T-1 is required, then the widths of output pulses of monostable multivibrator [in interface circuit] should be adjusted to 25 micro seconds. Gates, 10, 11, 12, 13 form a multiplexing circuit which selects either, output of gate 2 during the regular operation, or input 1 during the start-stop operation [first and last cycles]. The selection signal to the multiplexer is the output Q 1, of the first flip-flop, exclusive or'd with the output Q 2 of the second flip-flop through gate 3. Gates 4 and 9 are controlling the output enabling gate 6 while Q 1 is controlling the other output gates (5, 7, 8). The purpose of this distinction in the control of the output gates is that gate 6 has to be disabled one clock period after the other gates are disabled. Thus, at the end of the operation, thyristor TA-2 will be triggered once more, while all others will not.

(d) The purpose of the master clear circuit is to clear the two "D" flip flops, when power is turned on. This is accomplished through a resistor-capacitor as shown in fig [5.6]. The timing waveform of this circuit is shown in fig [5.8]. When power is turned on, capacitor C behaves momentarily as a short circuit. Until it charges to about 3.5 V, it presents a logic low to the clear input of the flip flops and thus clearing them. When the capacitor voltage exceeds the value of 3.5 volts, it presents a logic HIGH to the clear inputs, and therefore does not affect flip flops any more.

5.4.3. Output Circuit: The schematic diagram of the output circuit is shown in fig [5.9]. The triggering pulses for thyristors TA-1 and TA-2 are directly fed to the pulse amplifier through the opto couplers while the triggering pulses for thyristors T-1 and T-2 are first converted into a train of pulses before being transferred to the pulse amplifiers through opto couplers. The necessity for passing a train of pulses on thyristors T-1 and T-2 was already explained in chapter II, while the need for pulse amplification arises from the fact that the triggering pulses from the control circuit are a TTL [5V logic] signals, obviously they do not have sufficient power to drive the thyristor gates, and the pulse amplification becomes necessary.



Fig. [5.8] Timing Diagram of Master Clear Circuit.

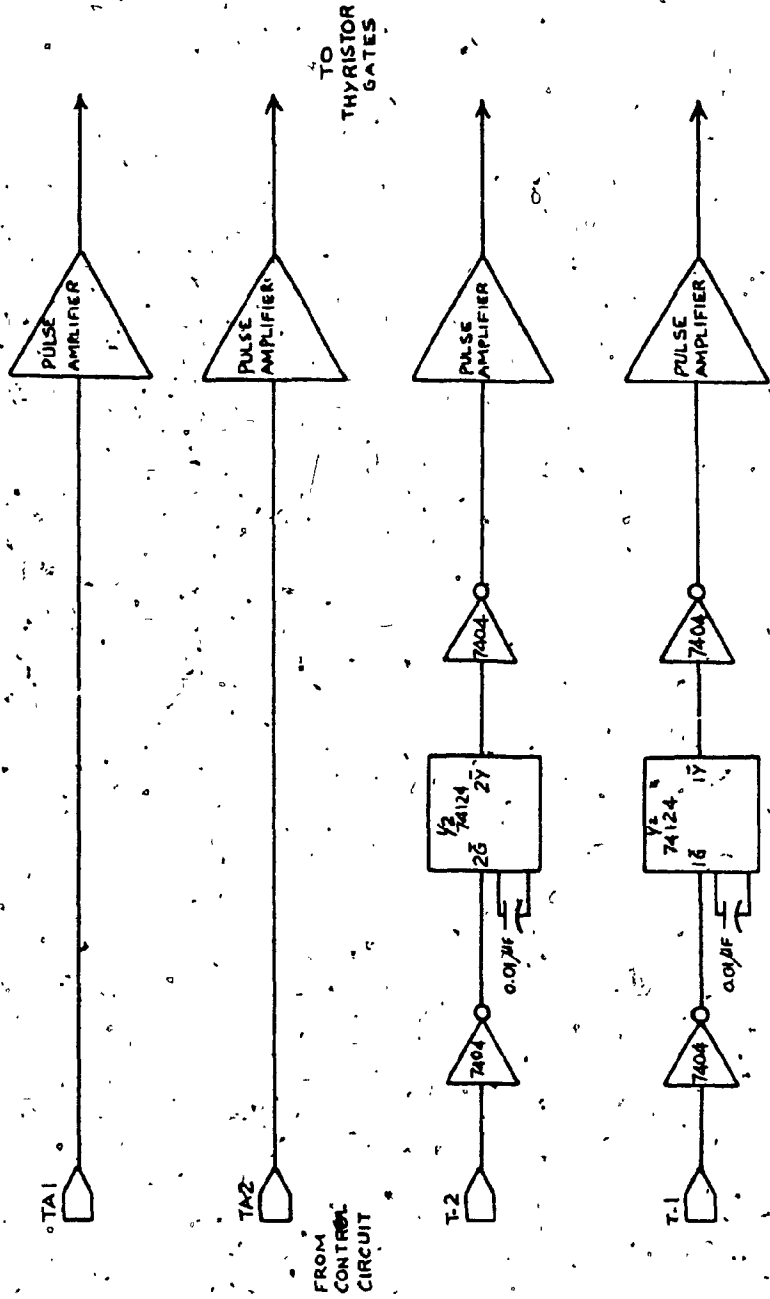


Fig. [5.9] Schematic Diagram of Output Circuit.

Opto-couplers are used to isolate the pulse amplifier from the control circuit. The reason is that the supply voltage required for the pulse amplifier is 20 volts while the control circuit is connected to 5 volt supply. In addition, opto couplers also minimize the noise propagation problem.

The required train of pulses [pulse-burst] for triggering T-1 and T-2 is obtained by using synchronous oscillator [74124]. The frequency of this oscillator is set at 50 KHz.

Fast rising gate pulses with high amplitude are generally used for proper triggering of thyristors. These type of pulses become essential requirement in case of high di/dt operation. There are various pulse amplification circuits available for obtaining such pulses [23] and the one used in this project is shown in fig [5.10]. It uses a direct amplification to obtain gate pulses with fast rise time and high amplitude. With this circuit, typically, gate pulses having a rise time of 0.1 microseconds or less and an amplitude of 20 volts, are obtained. The output of the pulse amplifier is fed to the thyristor gate.

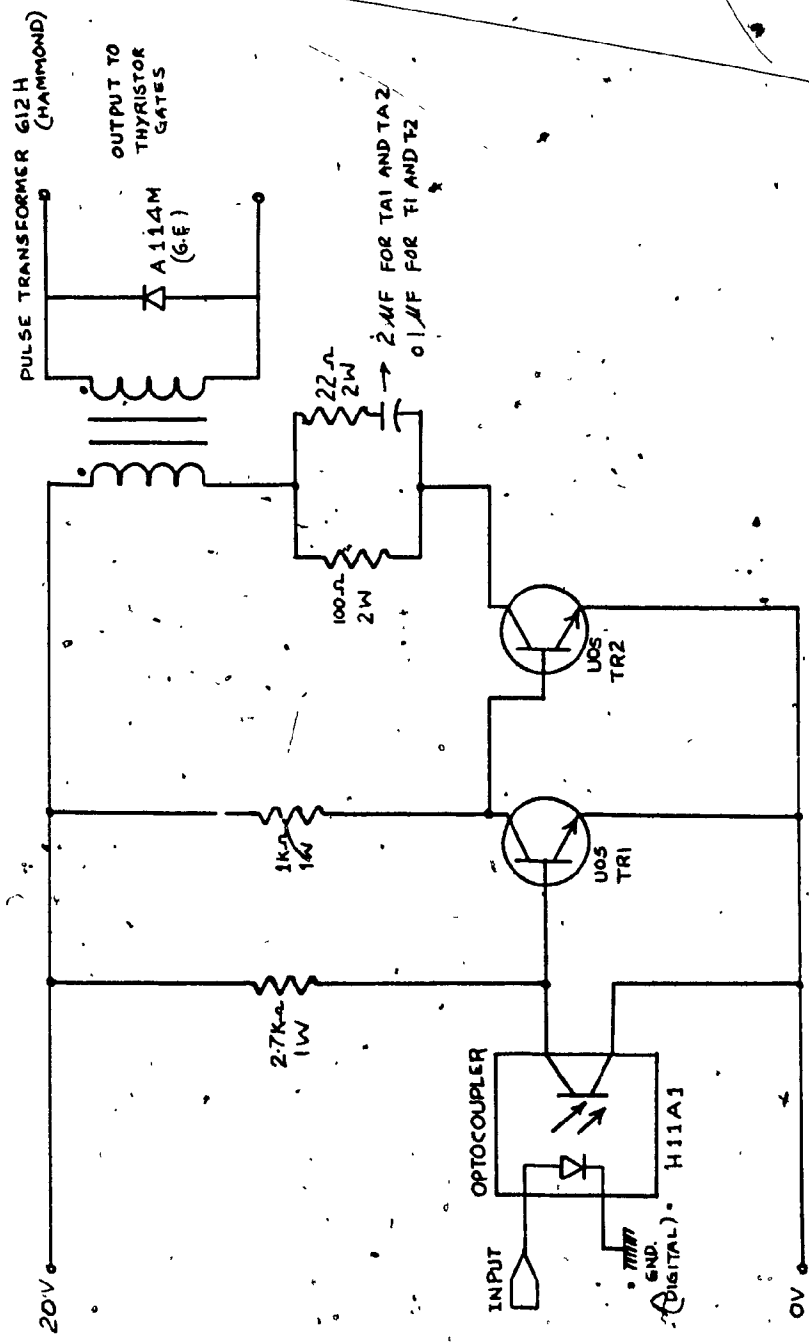


Fig. [5.10] Circuit Diagram of Pulse Amplifier.

CHAPTER VI

EXPERIMENTAL RESULTS

6.1 Introduction: A prototype of a modified McMurray inverter was actually built following the design outlined in chapter III. The inverter was subsequently tested for all types of passive loads (R, RL, L-loads), with a square wave supplied as the reference input to the firing circuit. The experimental results obtained during these tests are presented and explained in this chapter.

6.2 Description of the Experimental Set-up.

A DC supply of 220 volts with centre-tap was used for experimentation. Photographs 1 and 2 show the experimental set-up of the inverter. The details of the power circuit module are shown in photographs 3 and 4. The power circuit was built in a compact module form as explained in chapter 3. Firing circuit was assembled on bread boards and shielded cables between the logic circuit and the pulse amplifier circuit were used to avoid noise pick up. Photographs 5 and 6 show the details of the firing circuit. Photograph 8 shows the firing pulses during the inverter regular operation while photograph 9 shows the output of the pulse amplifier circuit (for thyristors T-1 and TA-2). RC snubber circuit combined with negative gate bias technique (as explained in chapter 4) was used for dv/dt protection. The details of the snubber circuit are shown in fig 7. Saturable inductors for di/dt protection and high speed

fuses for short circuit protection were used (Photograph 1). The performance of the protection circuits was satisfactory.

6.3 Experimental Performance.

The oscillograms recorded during the inverter testing are presented in this section (oscillograms 10 to 25) - oscillograms 10 and 11 show the commutation capacitor current and voltage waveform for no load (natural triggering) and inductive load (advance triggering). Oscillograms 12, 13, 14; 15, 16, 17; 18, 19, 20 show the waveforms of load voltage and current, dv/dt across main and auxiliary thyristor for different load conditions (L, RL, R load). Oscillograms 21, 22, 23 and 24 show the dv/dt across main thyristor, the dv/dt across auxiliary thyristor, commutation capacitor voltage and commutation current for no load. Finally oscillogram 25 shows commutation capacitor voltage and current waveform for no load (Advance triggering).

Under different load conditions, the load voltage (waveform) remains same (constant) while the current wave shape changes depending upon the nature of load (oscillograms 12, 15, 18). The calculated peak capacitor current was 325 Amps and the actual peak capacitor current (oscillogram 25) was approximately 330 Amps which closely corresponds to one calculated. The calculated peak capacitor voltage was about 390 volts and the actual capacitor voltage was approximately 360 volts. This difference can be attributed to the Q factor of the commutation inductor [18] [as explained in chapter 3 and Section 2.5]. Thus the inverter performance was.

satisfactory under all loading conditions.

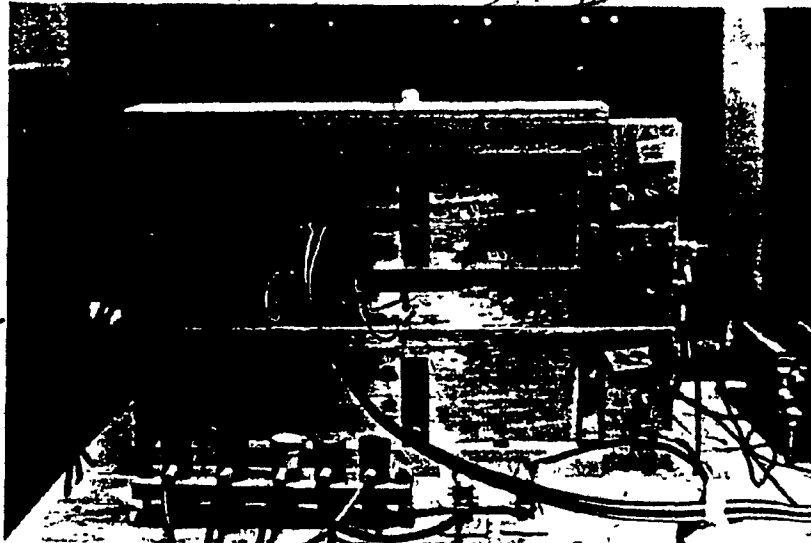
Note: The bottom traces in oscillograms 14, 16, 17, 19, 20, 21, 22
are capacitor current traces and they can be ignored.



1 & 2 : EXPERIMENTAL SET-UP OF
SINGLE PHASE MODIFIED MCMURRAY INVERTER

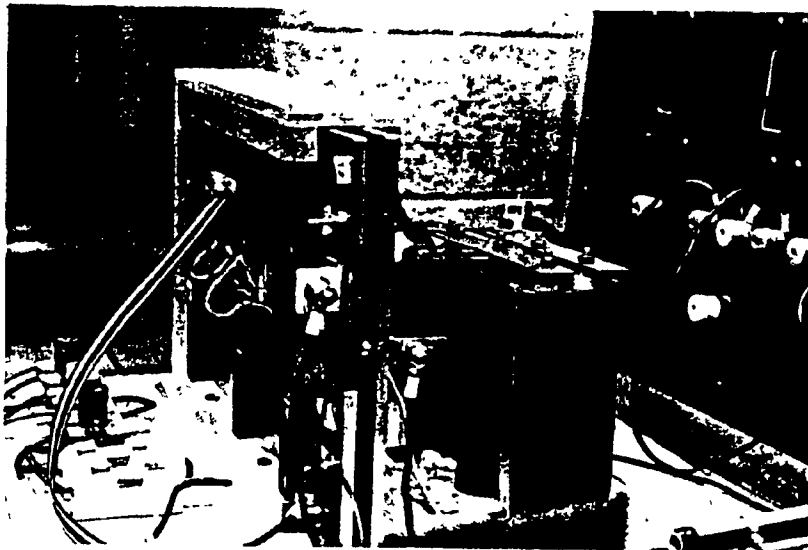


2



3

3 & 4: CLOSE-UP VIEW OF POWER CIRCUIT



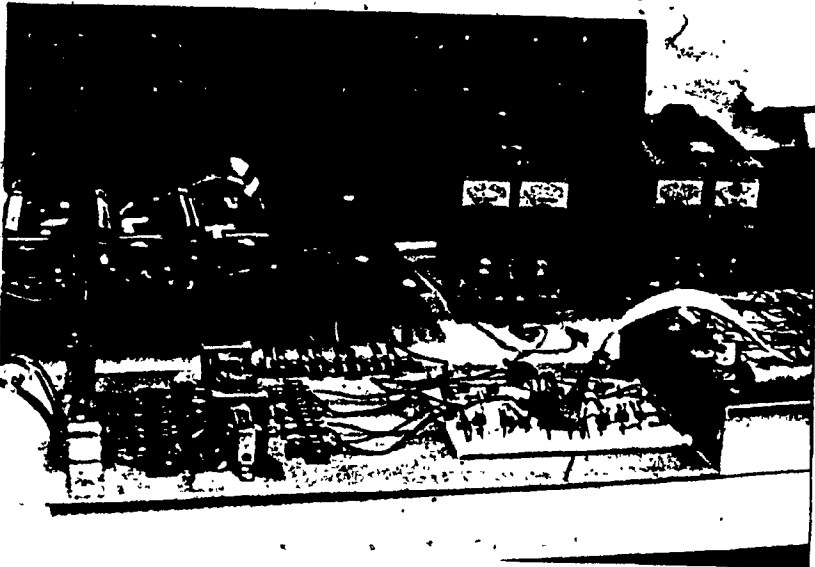
4

5 & 6: CLOSE-UP VIEW OF FIRING CIRCUIT.



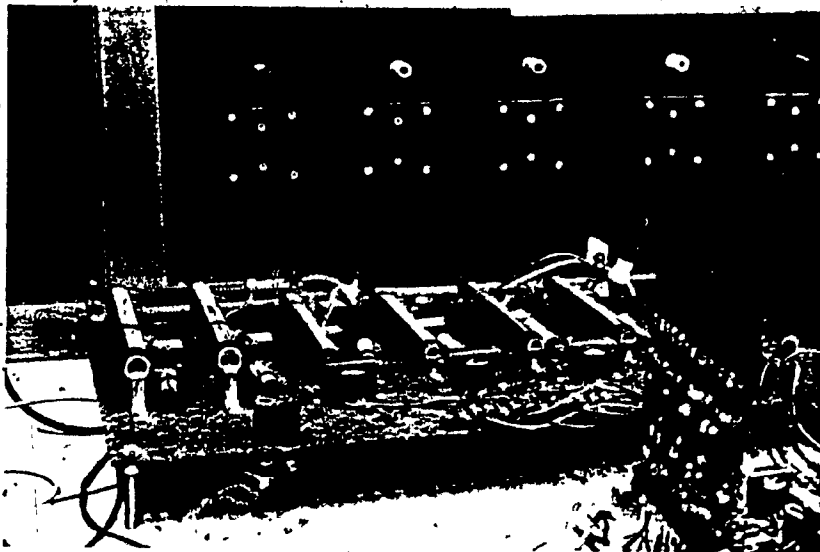
5

5: INTERFACE & CONTROL CIRCUIT.

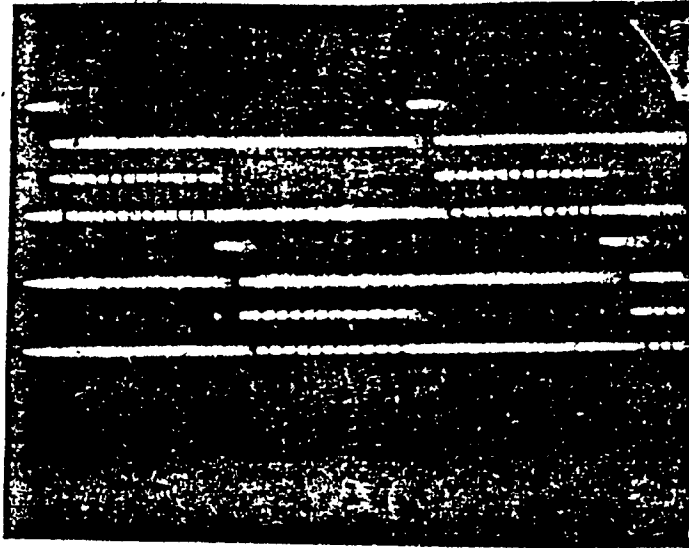


6

6: OUTPUT CIRCUIT (PULSE AMPLIFIER CIRCUIT).



7: CLOSE-UP VIEW OF SNUBBER CIRCUIT.



8

8: FIRING SEQUENCE OF SINGLE PHASE MODIFIED MCMURRAY
INVERTER FOR REGULAR OPERATION.

(OUTPUT OF CONTROL CIRCUIT):

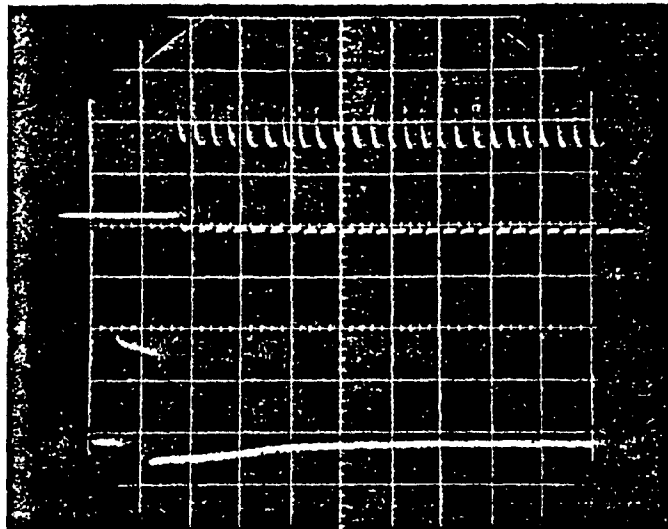
1st Trace from top: Pulse on TA 1.

2nd Trace from top: Pulse on T 2.

3rd Trace from top: Pulse on TA 2.

4th Trace from top: Pulse on T 1.

Scale: 5V/cm.



9: OUTPUT OF PULSE AMPLIFIER CIRCUIT.

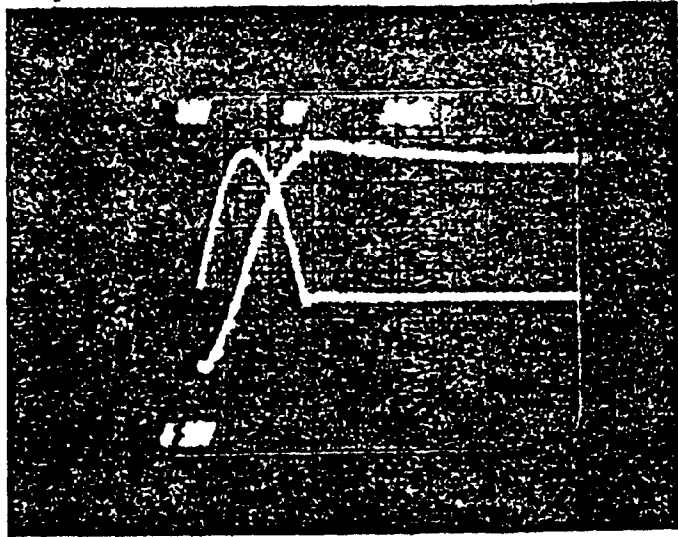
Top Trace: Pulse on T 1.

Bottom Trace: Pulse on TA 2.

Scale:

5 V/cm.

50 μ s/cm.



10

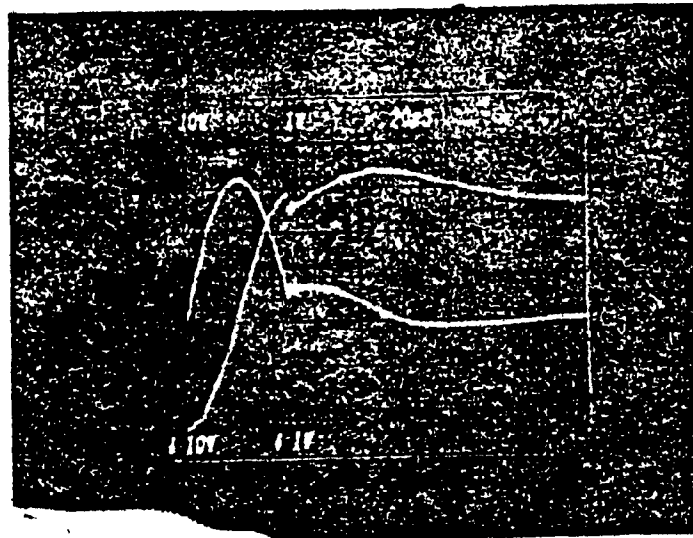
10:- COMMUTATION CAPACITOR CURRENT & VOLTAGE WAVEFORM
AT NO LOAD. ($f = 60 \text{ Hz.}$)

Scale:

100 A/cm.

100 V/cm.

20 $\mu\text{s/cm.}$



11

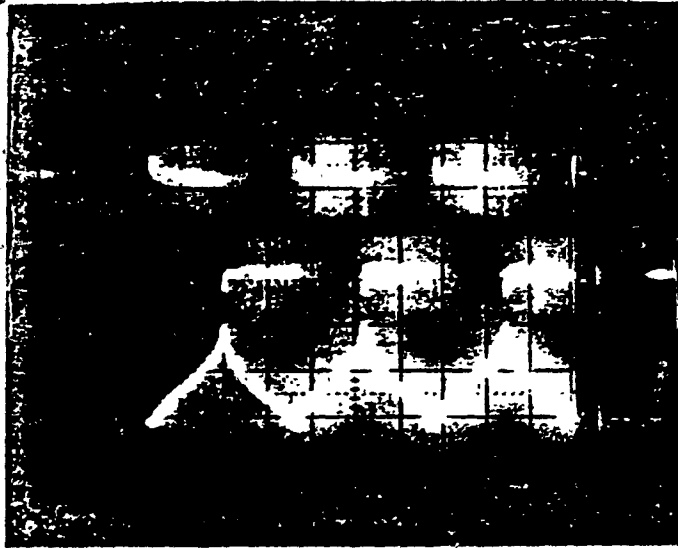
11: COMMUTATION CAPACITOR CURRENT & VOLTAGE WAVEFORM
FOR INDUCTIVE LOAD (30 A, rms.), ($F = 6\text{Hz.}$)

Scale:

100 A/cm

100 V/cm

20 $\mu\text{s/cm}$



12

12: VOLTAGE AND CURRENT WAVEFORM ACROSS LOAD.

INDUCTIVE LOAD. (10 A, rms.)

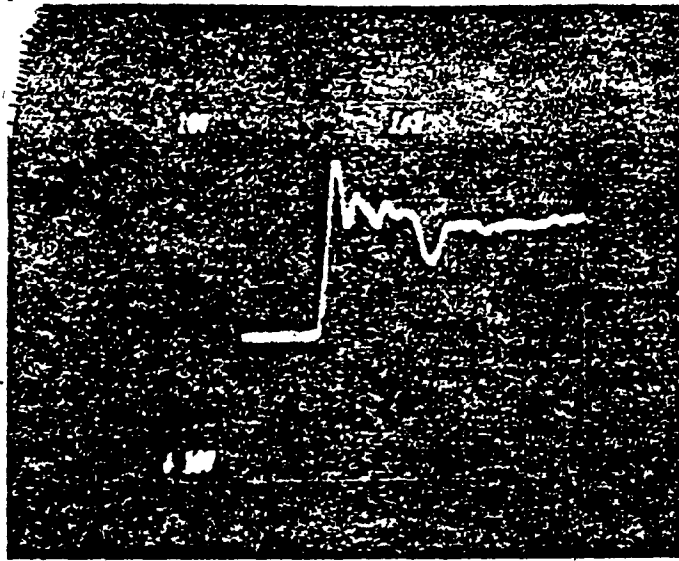
(f = 60 Hz).

Scale:

100 V/cm

10 A/cm

5 ms/cm



13

13: DV/DT ACROSS MAIN THYRISTOR T1

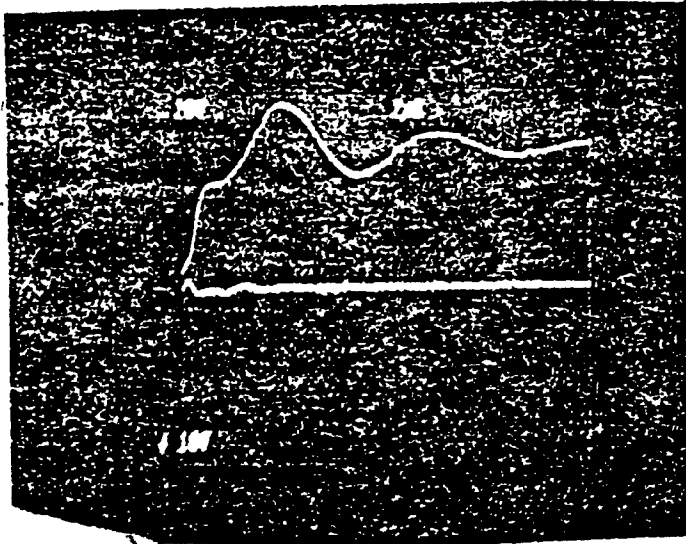
INDUCTIVE LOAD (20 A, rms.)

(f = 100 Hz).

Scale:

100 V/cm

1 μs/cm



14

14: DV/DT ACROSS AUXILIARY THYRISTOR TA 1 .

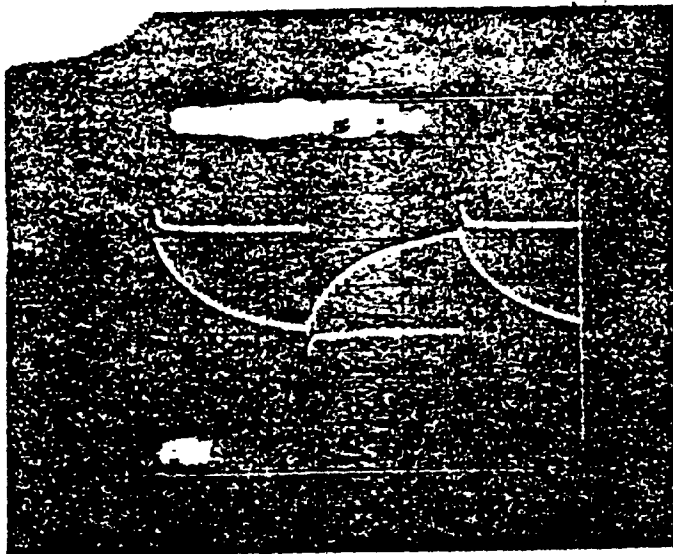
INDUCTIVE LOAD (20 A, rms.)

(f = 100 Hz.)

Scale:

100 V/cm

2 μ s/cm



15

15: VOLTAGE & CURRENT WAVEFORM ACROSS LOAD

(R, L LOAD.) (7 A, rms.)

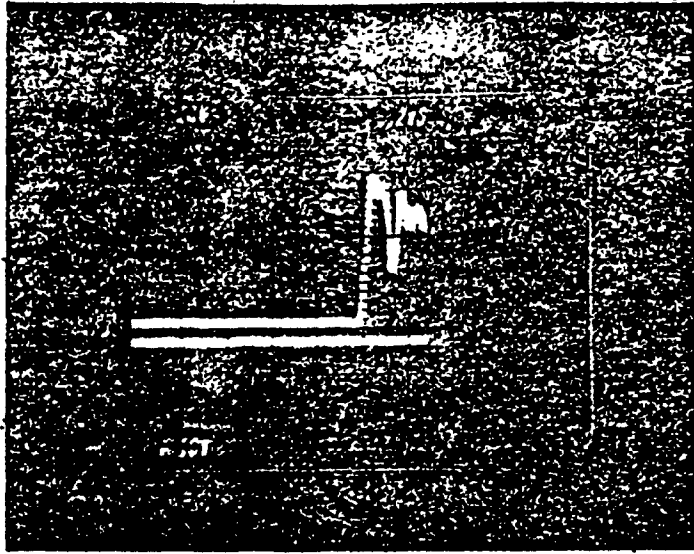
(f = 60 Hz.)

Scale:

100 V/cm

10 A/cm

2 ms/cm



16

16: DV/DT ACROSS MAIN THYRISTOR T 1 .

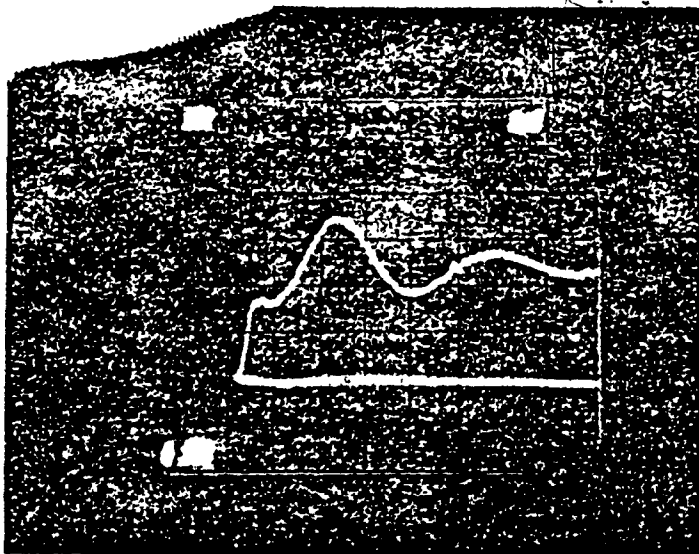
(R,L LOAD.) (7 A, rms.)

(f = 50 Hz.)

Scale:

100 V/cm

2 μ s/cm



17

17: DV/DT ACROSS AUXILIARY THYRISTOR TA 1 .

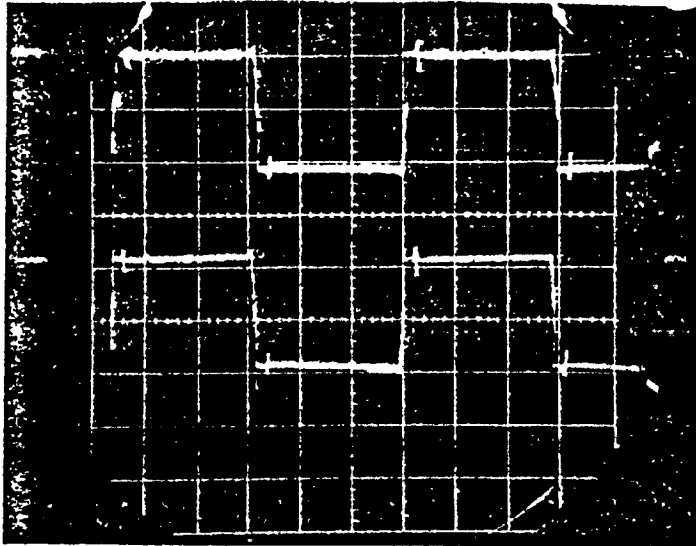
(R,L LOAD.) (7A, rms.)

(f = 60 Hz.)

Scale:

100 V/cm

2 μ s/cm



18

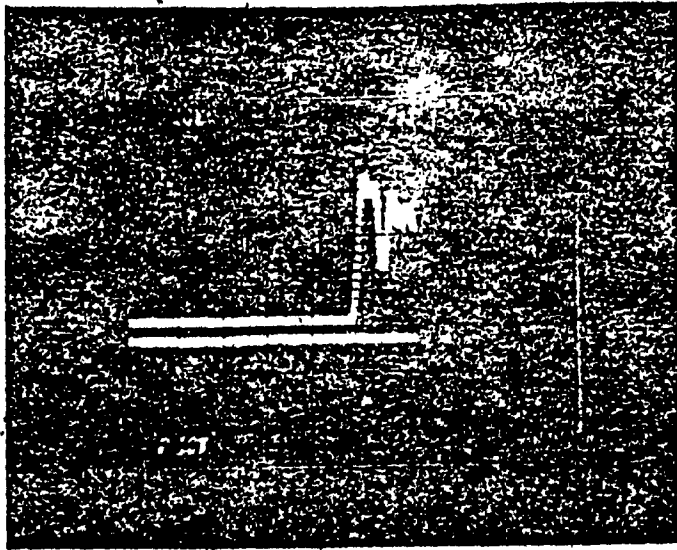
18: VOLTAGE & CURRENT WAVEFORM ACROSS LOAD.
RESISTIVE LOAD. (5 A).
(f = 100 Hz.)

Scale:

100 V/cm

5 A/cm

2 ms/cm



19

19: DV/DT ACROSS MAIN THYRISTOR T 1

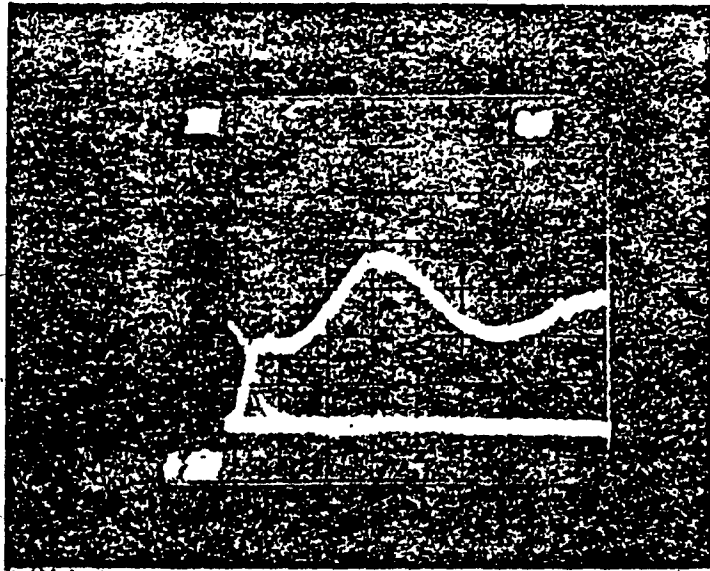
RESISTIVE LOAD. (5 A)

(f = 100 Hz).

Scale:

100 V/cm

2 μ s/cm



20

20: DV/DT ACROSS AUXILIARY THYRISTOR TA 1 .

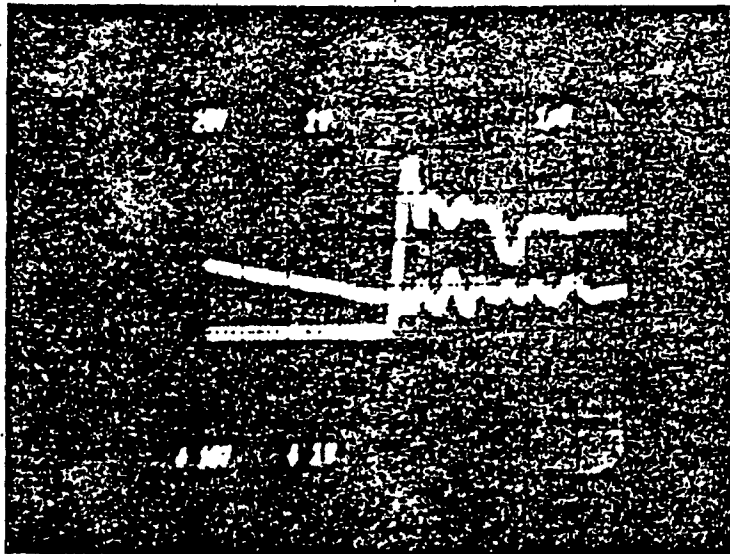
RESISTIVE LOAD. (5 A)

(f = 100 Hz.)

Scale:

100 V/cm

2. μ s/cm



21

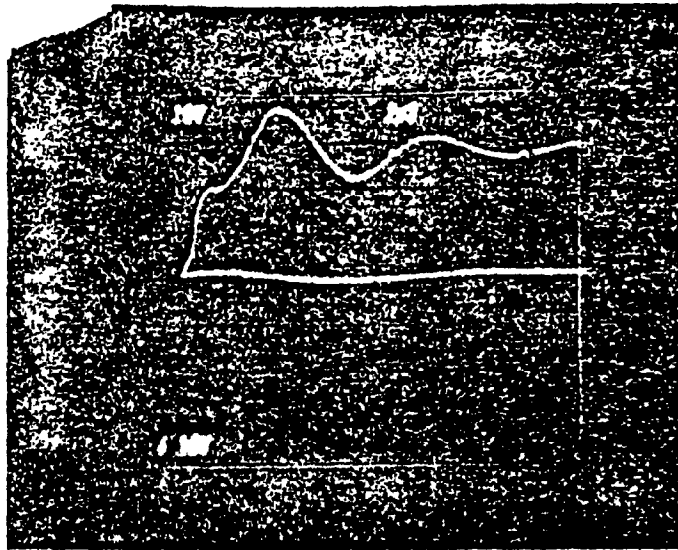
21: DV/DT ACROSS MAIN THYRISTOR T 1.

NO LOAD. (f = 100 Hz.)

Scale:

100 V/cm

1 μ s/cm



22

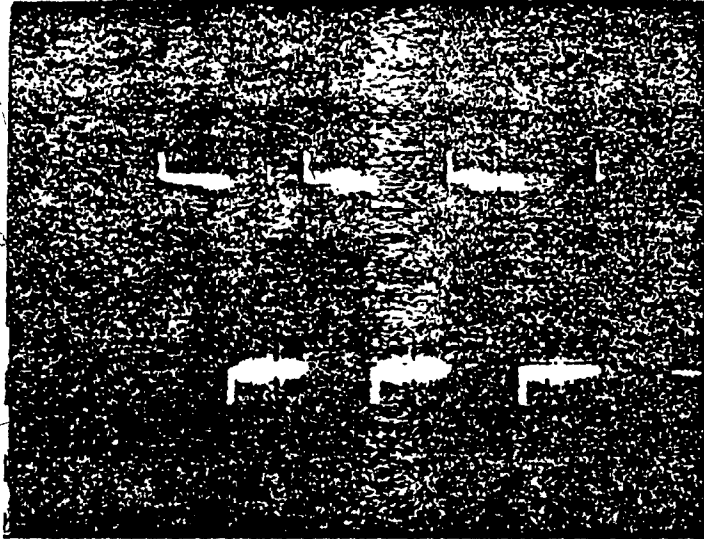
22: DV/DT ACROSS AUXILIARY THYRISTOR TA 1 -

NO LOAD ($f = 100 \text{ Hz.}$)

Scale:

100 V/cm

2 $\mu\text{s/cm}$



23

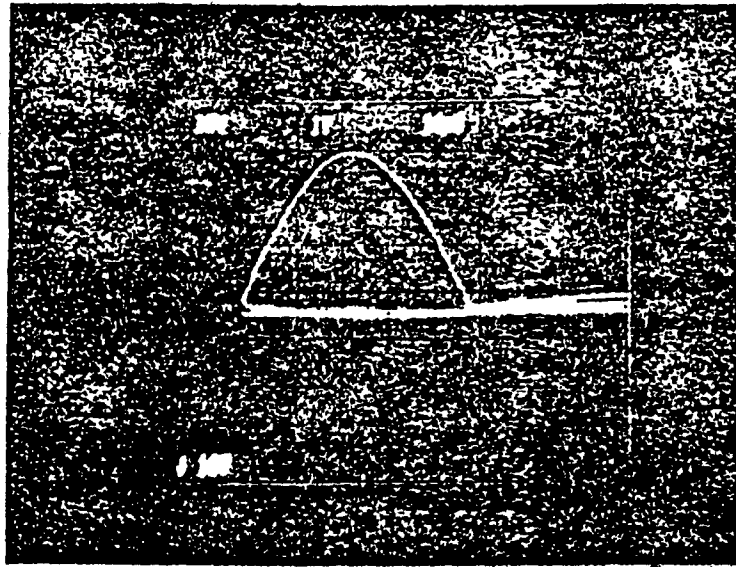
23: COMMUTATION CAPACITOR VOLTAGE WAVEFORM.

NO LOAD ($f = 60 \text{ Hz.}$)

Scale:

100 V/cm

5 ms/cm



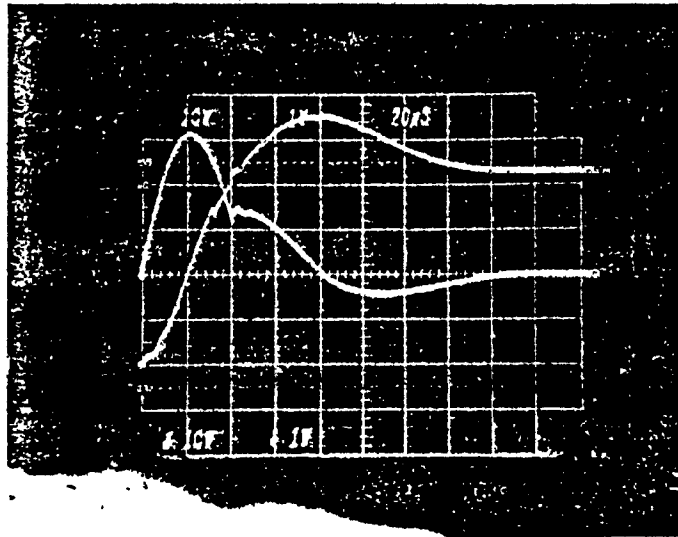
24

24: COMPUTATION CAPACITOR CURRENT WAVEFORM.
NO LOAD ($f = 100$ Hz.)

Scale:

100 A/cm

10 μ s/cm



25

COMMUTATION CAPACITOR CURRENT & VOLTAGE WAVEFORM
FOR ADVANCE TRIGGERING.

Scale:

100 A/cm

100 V/cm

20 μs/cm

CHAPTER VII

CONCLUSIONS

In recent years, the thyristor technology has made a significant progress and as a result thyristors with short turn-off times are commercially available. This has enabled the design of sophisticated thyristor inverters for a variety of applications. In applications requiring control of output voltage and frequency, PWM (pulse width modulated) control of inverters is used. In these inverters, regulation of output voltage and frequency is achieved within the same power controller by a special control logic. The power circuit of PWM inverters is simple but the control circuit is relatively complex. Main applications of PWM inverters include variable speed induction motor drives and uninterruptible Power Supplies (UPS).

The modified McMurray inverter described in this report is suitable for PWM. This inverter has the advantages in terms of low ratings of commutation components, minimum number of commutation components and high efficiency of circuit. However the dv/dt and di/dt stresses experienced in this inverter circuit are critical.

In the design of commutation circuit, the values of peak commutation capacitor voltage, peak commutation current, turn-off time of thyristors and the damping factor are important parameters. Commutation losses depend on Q factor of the commutating inductor.

Proper selection of components in the power circuit is essential for efficient, reliable operation of the circuit. The packaging of the power circuit is also one of the important parts of successful design.

When designing the inverter (thyristor) protection circuit, the following features were included.

The protection against di/dt failures is provided by connecting the necessary di/dt inductance in the anode circuit of the thyristor and selection of thyristors with amplifying gate structure ensures high di/dt withstanding capability.

The protection against excessive dv/dt and voltage spikes due to switching transients is provided by the snubber circuit. Since dv/dt stresses are critical in this inverter, combination of RC snubbers with dynamic negative gate bias provides the necessary protection.

The protection from fault current is provided by selecting proper high speed fuses.

The firing circuit of the inverter can be realized through analogue or digital scheme. The digital scheme which has advantages of higher immunity against noise, better accuracy of control and high reliability has been implemented in this design.

A prototype of the modified McMurray inverter was actually built following the design outlined in this report. The salient features of this prototype model are:

The compact modular form of the power circuit which simplifies maintenance, trouble-shooting and minimizes stray inductances in the path of main thyristors and feedback diodes.

The digital firing circuit which include the electronic 'start-stop' operation of the inverter as well as the precise adjustment of delay between triggering the auxillary and the main thyristors.

The inverter was subsequently tested for all types of passive loads (R, RL, L loads). The obtained results indicated satisfactory inverter operation.

Thus the prototype inverter becomes an important building block of the three phase inverter system. This report provides the necessary information and guide lines for the future designs of the modified McMurray type inverters.

References

- [1] Mapham N. W., "The Classification of SCR Inverter Circuits",
IEEE International Convention Record, part 4, pp. 99-105,
1964.
- [2] General Electric Co., "SCR Manual" - 5th Edition - pp. 351-399,
1972.
- [3] International Rectifier Co., "SCR Applications Hand Book",
1st Edition - pp. 283-309, 1974.
- [4] Pollack J. J., "Some Guide Lines for the Application of Adjustable-
speed AC Drives", IEEE Trans. on IA, vol. IA-9, no. 6, pp. 704-710,
Nov/Dec 1973.
- [5] Pollack J. J., "Advanced Pulse Width Modulated Inverter Techniques",
IEEE Trans on IA, vol IA-8, no. 2, pp. 145-154, Mar/April 1972.
- [6] Rosenberg "Pulse Width Control in PWM Inverters" - M.Sc.
Thesis University of Toronto 1970.
- [7] Peterson W. V.; Yohman E. J., "Pulse Width Modulated Inverters
for Uninterruptible AC Power System Applications", IEEE Trans.
on IECI, vol. IECI-17, no. 4, pp. 339-345, June 1970.
- [8] Stefanovic V. R., "Variable Frequency Induction Motor Drive
Dynamics", Ph.D. Theses, McGill University 1975.

- [9] Mokrytzki, B., "Pulse Width Modulated Inverters for AC Motor Drives", IEEE Trans on IGA, vol. IGA-3, no. 6, pp. 493-503, Nov/Dec 1967.
- [10] Alexanderson E. F. W., "System of distribution", U.S. patent 1800 002, 1923.
- [11] Prence D. C., "The Direct Current Transformer Utilizing Thyatron tubes", General Electric Rev., vol. 31, pp. 347-350, 1928.
- [12] Klemens Heumann, "Development Of Inverters with Forced Commutation for AC Motor Speed Control up to the Megawatt Range", IEEE Trans. on IGA, vol. IGA-5, no. 1, pp. 61-67, Jan/Feb 1969.
- [13] Rissik, H., "The Fundamental Theory of Arc Convertors", London, Chapman and Hall Ltd., Chapt. X, XI, XII, 1939.
- [14] McMurray, W. and Shattuck D. P., "A Silicon Controlled Rectifier Inverter with Improved Commutation", AIEE Trans. on Communications and Electronics, vol. 80, pp. 531-542, Nov. 1961.
- [15] McMurray, W., "SCR Inverter Commutated by an Auxiliary Impulse", IEEE Trans on Communication and Electronics, vol. 83, no. 75, pp. 824-829, Nov. 1964.
- [16] Penkowski, L. J. and Pruzinsky, K. E., "Fundamentals of a Pulse Width Modulated Power Circuit", IEEE Conference Record of Fifth Annual Meeting of Industry and General Applications Group, pp. 669-678, 1970.

- [17] R. Palaniappan, R. K. Abrol, S. K. Datta, J. Vithayathel,
"Modified McMurray Inverter with pulse forming Network
Commutation Circuits", IEEE Trans on IECI, vol. IECT-24,
no. 1, pp. 66-73, Feb. 1977.
- [18] Klaassens J. B., "Analyses of a Forced Commutation Circuit for
Design of a Class of Thyristor Inverters", IEEE Trans on IECI,
vol. IECT-20, no. 3, pp. 125-129, Aug. 1973.
- [19] Carlton E. G., Skogsholm E. A. and Volkmann W. K., "Practical
Design Considerations for Inverter Drives", IEEE Trans on I. A.,
vol. IA-9, no. 5, pp. 593-600, Sept/Oct. 1973.
- [20] Jalal T. Salihi, "An Inverter for Traction Application", IEEE Trans.
on IA, vol. IA-8, No.5, pp. 644-650, Sept/Oct. 1972.
- [21] Plunkett A. B., Plette D. L., "Inverter Induction Motor Drive
for Transit Cars", IEEE Trans. on IA, vol. IA-13, no. 1,
pp. 26-37, Jan/Feb. 1977.
- [22] Dewan S. B. and Straughen A., "Power Semiconductors Circuits",
A Book published by John Willey & Sons, Chapter VI.
- [23] Rice L. R., Editor, Second Edition, "Westinghouse, Silicon
Controlled Rectifier Designer's Handbook", Chapter VI, Sept. 1970.
- [24] Bedford B. D. & Hoft R. G., "Principles of Inverter Circuits",
A Book published by John Wiley & Sons Inc., Newyork, Chapter VII.

- [25] Von Zastrow E. E. & Galloway, "Commutation Behaviour of Diffused High Current Rectifier Diodes", G. E. application note: 200.42/(6/65).
- [26] Galloway J. H., "Application of Fast Recovery Rectifiers" G. E. application note: 200.38/(6/65).
- [27] Paice D. A., "Nonlinear Reactors as Protective Elements for Thyristor Circuits", IEEE Trans. on Magnetics, vol. MAG-3, no. 3, pp. 288-232, Sept. 1967.
- [28] Min B. J. & Wearsch H. W., "An improved Snubber Circuit for Power Semiconductors", IEEE, IAS Conference Record, pp. 1017-1022, 1977.
- [29] Cooper D., "The State of the Art in Power Thyristor Semiconductor Technology", International Rectifier Co., A. Handbook.
- [30] Wu S.J. "Analyses and Design of Optimized Snubber Circuit for dv/dt Protection in Power Thyristor Application" G. E. application note: 660-24/(2/71).
- [31] McMurray W., "Optimum Snubbers for Power Semiconductors", IEEE Conference Record of Sixth Annual Meeting of IAS Group, pp. 33-41, 1971.
- [32] "Semiconductor Fuse Applications Handbook", Editor: Glenn Geissinger, Published by: International Rectifier Co., II Edition, Jan. 1973.

APPENDIX I

APPENDIX I

A

AMPLIFYING GATE THYRISTOR

This type of thyristor has an internal arrangement for gate current amplification. Schematically the amplifying gate thyristor is shown in fig. [A]. This amplifying gate thyristor behaves like a main power handling thyristor triggered by a small 'pilot' thyristor. In this type of thyristors, double switching is employed i.e. the main thyristor portion switches immediately after conduction is initiated in the pilot portion of device. The anode current of the pilot portion of the device causes rapid turn on of a significant portion of the main current carrying portion of the device. Therefore to initiate 'turn-on', only a relatively small amount of gate current is required and thus, with this type of gate arrangement (construction), a high built in di/dt withstand capability is ensured to the thyristor.

B

DESCRIPTION AND OPERATION OF THE SNUBBER

NETWORK

The circuit diagram is shown in fig [B.1]. In this circuit, part no: 30 is the thyristor, which is to have the snubber network connected

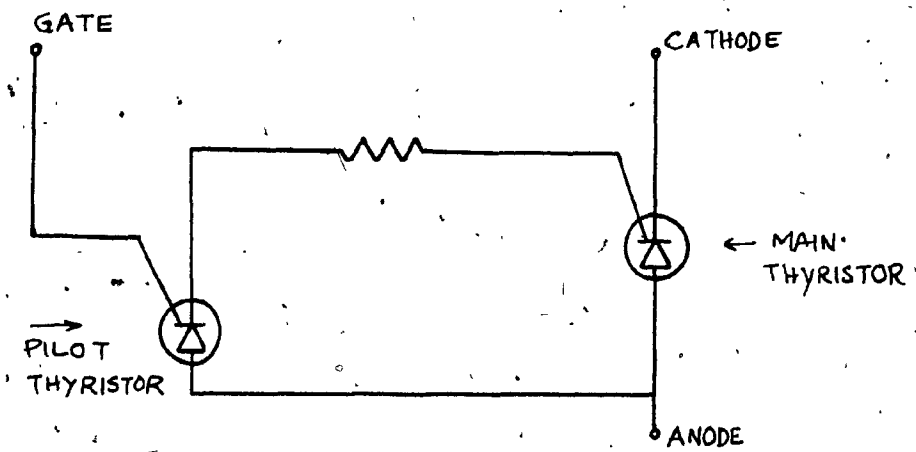


Fig. [A] Schematic Diagram of Amplifying Gate Thyristor.

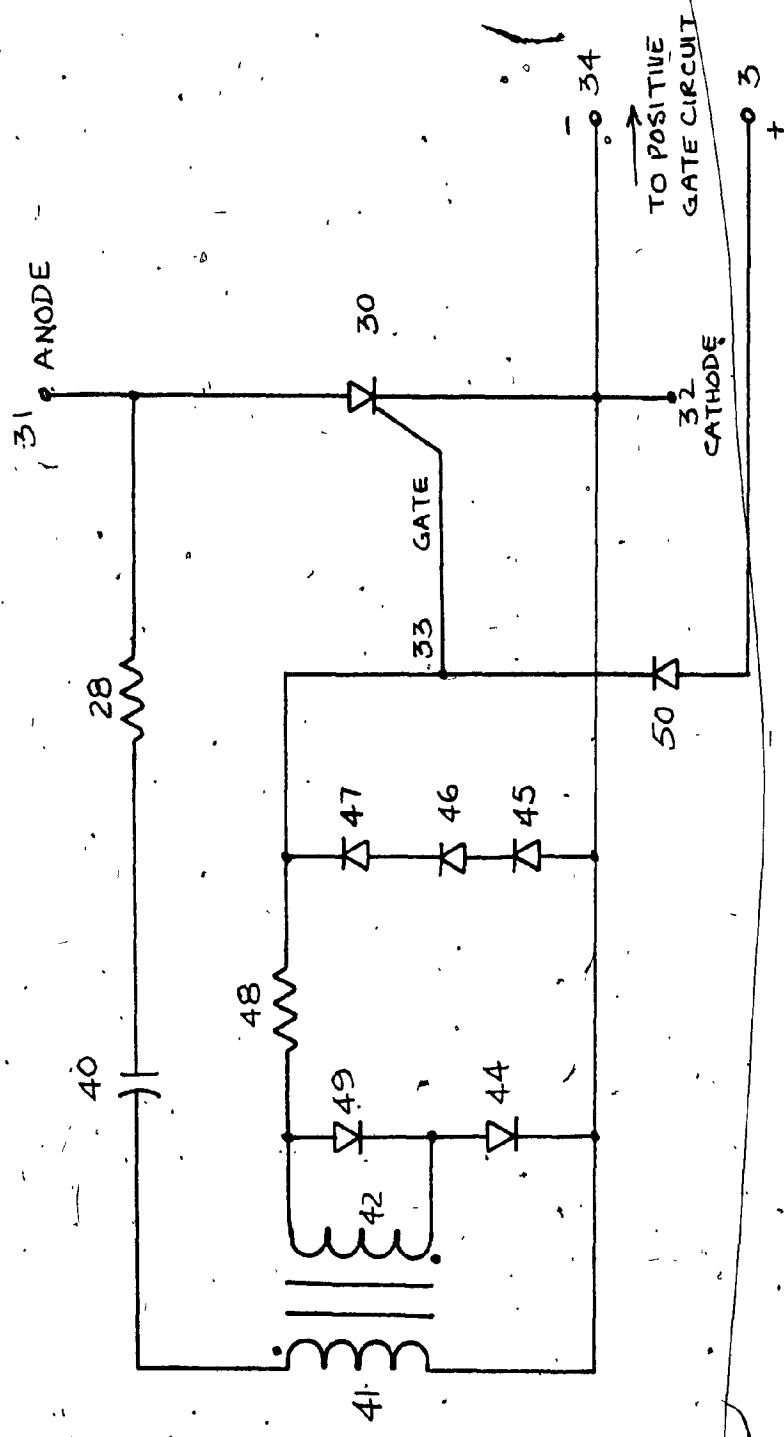


Fig. [B.1] Snubber Network.

across it. The points number 31, 32, 33 are its anode, cathode and gate terminals respectively. The normal gate signal to turn on thyristor is applied to terminals 34 and 35 through a fast recovery diode (part no. 50). Connected in series pointing from the cathode to gate of the thyristor is series of diodes (parts no. 45, 46, 47). These provide a clipping of the negative bias on the gate. Part no. 48 is simply a current limiting resistor to avoid any measurable gate current from flowing into the suppression network and to limit the current from the suppression network through diodes. Part no. 41 and 42 are the primary and secondary of a pulse transformer. Part no. 49 is a free wheeling diode connected across secondary of pulse transformer. Part no. 44, is a diode which blocks any positive signal from flowing out of the pulse transformer through the gate. Part no. 40 is a differentiating capacitor and part no. 28 is a damping resistor. They are connected in series with the primary of the pulse transformer across anode (31) and cathode (32) of the thyristor as shown in fig. [B.1].

OPERATION OF THE CIRCUIT

The circuit works as follows:- when there is a forward rising voltage across the thyristor (30), this voltage is differentiated by capacitor (40). The current flows into this capacitor being in series with winding (41) of the pulse transformer. Accordingly, a voltage is introduced in winding (42) of the pulse transformer. The voltage is proportional to the rate of rise of voltage (dv/dt) across the thyristor (30) and this voltage is then

applied to diode (44) across the diodes (45, 46, 47), which are in parallel with the gate circuit including terminals 32 and 33. Diode 44 is a fast recovery diode to prevent any reverse recovery current from triggering thyristor (30). Resistor (part no. 48) serves as a current limiting resistance in a closed circuit including pulse transformer winding (42) and diodes (44, 45, 46 and 47). The forward voltage drop across diodes (45, 46, 47) is then applied to gate (33) as a negative bias. As the positive dv/dt in the circuit increases and the demand for more negative gate current increases, the current applied by the circuit increases proportionately. When resistance (no. 48) is small, compared to the impedance of capacitor (40), the maximum available negative current is given by $I_{\max} (\text{snubber}) = c \, dv/dt$.

The volt-seconds applied to the transformer will be constant as the voltage increases at any particular rate to a specified voltage. The number of volt-seconds applied to winding (42) is proportional to the product of capacitance of capacitor (40), resistance of resistor (48) and change in voltage. It should be mentioned here that the selection of the pulse transformer is not critical [29].

Thus with this circuit, it is possible to negatively bias the gate of the thyristor in proportion to the dv/dt applied to the thyristor with no external power source.

SELECTION OF COMPONENTS

As it was not possible to obtain the necessary design procedure the values of the components used in this circuit were obtained by cut and try method. The starting values for the snubber circuit [R (part no. 28) and C (part no. 40)] were obtained by the guidelines given in [30] and [31]. The final values were chosen as R = 15 ohm and C = .1 μ F by experimentation. The pulse transformer used in this circuit is of type 612 H. made by Hammond Co. The diodes used in this circuit were of type A114 m [fast recovery type] made by G.E. Co. The value of current limiting resistor (part no. 48) used is 560 ohms. With these values, this snubber circuit showed satisfactory results. The specifications of components are included in appendix [II].

APPENDIX I

C

SOME IMPORTANT FACTORS IN FUSE

CO-ORDINATION UNDER DC OPERATION

In general, when operating from a DC supply, it is more difficult for the fuse to perform its intended function of current interruption following a short circuit because the current through the fuse is not inherently reduced to zero as it is when the applied voltage is AC. Whenever the voltage across the fuse reverses repetitively, the fuse can be considered to be operating on AC. Fuses intended for the protection of semiconductors may be used in both AC and DC circuits. On the other hand, most of the published information for thyristor fuses pertains to their performance in AC applications; very little published information pertains to operations on DC [32].

During the time, the fuse is clearing the fault, rapid interruption of large (fault) currents leads to creation of high overvoltages called arcing voltages. If a semiconductor is subjected to such a high overvoltage, it will fail due to breakdown phenomenon. Thus, while selecting a fuse, precaution should be taken to see that arcing voltage during fault interruption, should not exceed

the blocking voltage capability of the semiconductor.

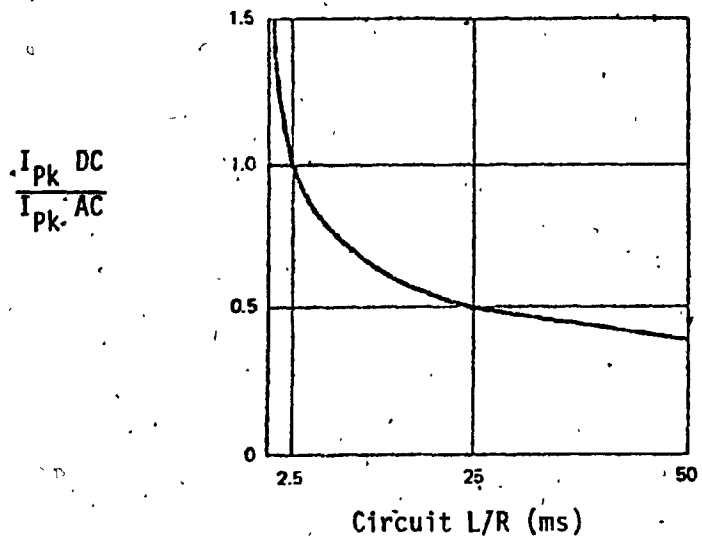
The major factor which determines how a fuse will operate in a dc circuit is the time constant (L/R) of the dc circuit [32].

The maximum voltage that can be applied to the fuse and still enable it to clear will be less in the case of dc operation. With many current limiting fuses designed for the protection of semiconductors, the dc voltage rating will be about 75 percent of the ac RMS voltage rating when the rate of rise of current through fuse is high (i.e. $\frac{L}{R}$ is small, (up to 20 milli-sec.)). For low rate of rise of current (i.e. $\frac{L}{R}$ is high (20 milli-sec or more)), the maximum voltage which the fuse can interrupt is still less.

Therefore, the maximum DC voltage rating of a fuse operating in a dc circuit depends on L/R of the circuit and the graph of circuit L/R verses DC voltage rating is usually supplied by the fuse manufacture.

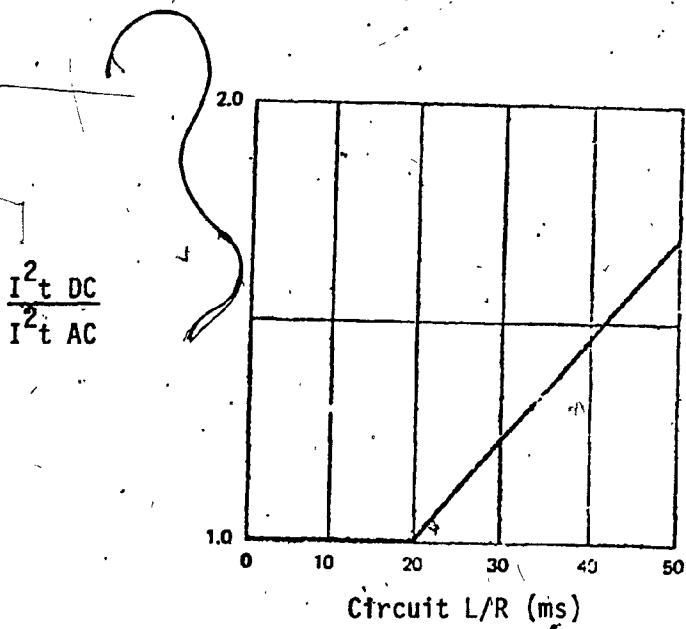
The instantaneous peak let through current for dc operation can be related to the value published for ac operation in a low power factor circuit and is dependent on the dc circuit L/R . This is shown in fig [C.1]. [This curve was supplied by fuse manufacturer]. The let-through I^2t for dc operation can also be related to the value published for ac operation and again shows dependency on the dc circuit L/R . This is shown in fig [C.2]. [This curve was also supplied by fuse manufacturer].

Thus, these curves [fig (C.1) and (C.2)] are useful for selection of fuse. Other information pertaining to fuse operation and selection



Ratio of Instantaneous Peak Let-Through Current for DC to AC Operation Vs. Circuit L/R.

Fig. [C.1]



Ratio of Let-Through I^2t for DC to AC Operation
Vs. Circuit L/R

Fig. [C.2]

is given in detail in [32].

Location of fuse in a circuit is also an important consideration in selection and co-ordination of fuses. The location of fuse is solely dependent on actual circuit configuration. The proper location of fuse in this inverter circuit is shown in fig [2.1].

STEP BY STEP APPROACH TO FUSE SELECTION

From the above considerations, a step by step approach to the fuse selection for this inverter is given below:

- A Determine the circuit inductance and resistance and find the ratio L/R .
- B Determine the prospective fault current.
- C From the graphs of L/R , V_s , $\frac{I_{PK} (DC)}{I_{PK} (AC)}$ and

$\frac{I^2_t (DC)}{I^2_t (AC)}$, given by fuse manufacturer, determine

the values of the above ratios. Using the ratio $\frac{I_{PK} (DC)}{I_{PK} (AC)}$

and $I_{PK} (DC)$ [which is prospective fault current], find the current $I_{PK} (AC)$ [which is the prospective (Equivalent) AC

fault current value].

- D From the above value of prospective AC fault current, find the value of I^2t (AC). From the value of I^2t (AC) and the ratio of $\frac{I^2t \text{ (DC)}}{I^2t \text{ (AC)}}$, find the value of I^2t (DC).

This value of I^2t (DC) is now compared with the 'let-through' I^2t of the semiconductor device. I^2t (DC) has to be less than I^2t of the device under all conditions. Similarly I_{PK} (DC) has to be less than peak 'let-through' surge current of the device.

- E Finally, from the curve of Peak Arc voltage versus supply voltage, supplied by the fuse manufacturer, check if the peak Arc voltage is less than the blocking voltage capability of the semiconductor device.

SELECTION OF THE FUSE

Thyristors used in this inverter circuit are GE C-365 m type. The subcycle surge rating and sub cycle I^2t verses pulsewidth data are given in its specification sheet, which is included in appendix [II].

The total circuit inductance and resistance of the circuit was estimated to 20 microhenries and .1 ohm . This gives the L/R ratio as .2 mili seconds. The prospective fault current was

estimated to 2200 Amps [$I_{\text{fault}} = \frac{E}{R}$]. For the value of

L/R = .2 m. sec, the ratio of $\frac{I_{\text{PK}} (\text{DC})}{I_{\text{PK}} (\text{AC})}$ is equal to 1.5 .

This gives $I_{\text{PK}} (\text{AC})$ as 1500 Amps (approximately), which is prospective AC fault current. Again for the value of

L/R = .2 m. sec, the ratio of $\frac{I^2 t (\text{DC})}{I^2 t (\text{AC})}$ is equal 1 .

Sub cycle $I^2 t$ V_s pulse width data was plotted on the graph of 'let through' $I^2 t$ verses prospective AC fault current.

From above, it was seen that for the given fault condition, fuse rating (current) could go as high as 175 Amp, because the 'let through' $I^2 t$ for 1500 Amps of fault current for 175 Amps fuse was far below the $I^2 t$ of the thyristors, under all conditions.

However, under normal (rated) operating condition, the inverter demands a (RMS) current of 75 Amps (approximately), therefore the current rating of the fuse can be 80 Amps. Similarly the operating voltage of the fuse can be 220 V (DC) and therefore AC

voltage rating can be 250 V (AC, RMS). Finally, the peak arc voltage for the fuse [for 250 V, AC rating] is below the blocking voltage capability of the thyristor.

Hence a high speed fuse [SF 25 x 80] manufactured by International Rectifier Co. is recommended for the purpose. It has a current rating of 80 Amps [RMS] and a voltage rating of 250 volts [AC, RMS]. The data sheet of the fuse is included in appendix [II].

APPENDIX II

SPECIFICATIONS OF COMPONENTS

HIGH SPEED Silicon Controlled Rectifier

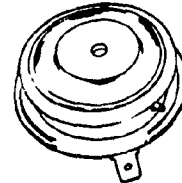
C364/C365

600 Volts

275 A RMS



The General Electric C364 and C365 Silicon Controlled Rectifiers are designed for power switching at high frequencies. These are all-diffused Press-Pak devices employing the field-proven amplifying gate.



FEATURES:

- Fully characterized for operation in inverter and chopper applications.
- High di/dt ratings.
- High dv/dt capability with selections available.
- Rugged hermetic glazed ceramic package.

MAXIMUM ALLOWABLE RATINGS

TYPES	REPETITIVE PEAK OFF-STATE VOLTAGE, V_{DRM}^1 $T_J = -40^\circ\text{C to } +125^\circ\text{C}$	REPETITIVE PEAK REVERSE VOLTAGE, V_{RRM}^1 $T_J = -40^\circ\text{C to } +125^\circ\text{C}$	NON-REPETITIVE PEAK REVERSE VOLTAGE, V_{RSM}^1 $T_J = +125^\circ\text{C}$
C364/C365A	100 Volts	100 Volts	200 Volts
C364/C365B	200	200	300
C364/C365C	300	300	400
C364/C365D	400	400	500
C364/C365E	500	500	600
C364/C365M	600	600	720
C365S	700	700	840
C365N	800	800	960

¹ Half sine wave waveform, 10 ms max. pulse width.

RMS On-State Current, $I_T(\text{RMS})$	275 Amperes
Peak One Cycle Surge (Non-Repetitive) On-State Current, I_{TSM} (60 Hz).....	1800 Amperes
Peak One Cycle Surge (Non-Repetitive) On-State Current, I_{TSM} (50 Hz).....	1700 Amperes
I^2t (for fusing) for times > 1.5 milliseconds.....	9,500 (RMS Ampere) ² Seconds
I^2t (for fusing) for times > 8.3 milliseconds.....	13,500 (RMS Ampere) ² Seconds
Critical Rate-of-Rise of On-State Current, Non-Repetitive.....	800 A/ μs †
Critical Rate-of-Rise of On-State Current, Repetitive.....	500 A/ μs †
Average Gate Power Dissipation, $P_{G(\text{AV})}$	2 Watts
Storage Temperature, T_{STG}	-40°C to +150°C
Operating Temperature, T_J	-40°C to +125°C
Mounting Force Required.....	.800 Lbs. \pm 10% 3.56 KN \pm 10%

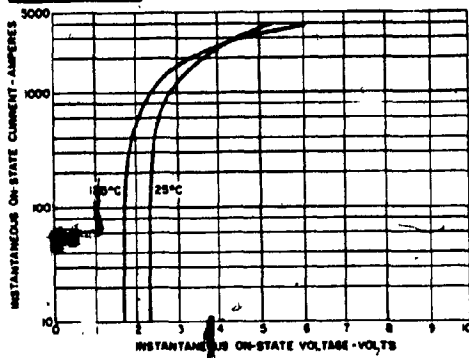
[†]di/dt ratings established in accordance with EIA-NEMA Standard RS-397, Section 5.2.2.6 for conditions of max. rated V_{DRM} : 20 volts, 20 ohms gate trigger source with 0.5 μs short circuit trigger current rise time.

CHARACTERISTICS

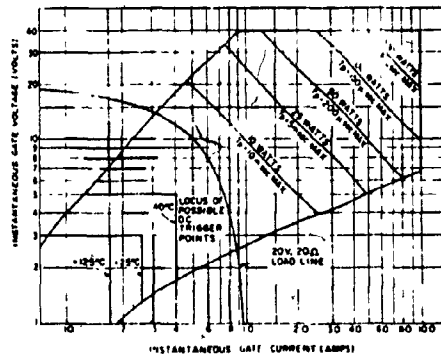
TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITION
Repetitive Peak Reverse and Off-State Current	I_{RRM} and I_{DRM}	-	5	12	mA	$T_J = +25^\circ C$ $V = V_{DRM} = V_{RRM}$
Repetitive Peak Reverse and Off-State Current	I_{RRM} and I_{DRM}	-	12	17	mA	$T_J = 125^\circ C$ $V = V_{DRM} = V_{RRM}$
Thermal Resistance	$R_{\theta JC}$	-	.12	.135	$^\circ C/Watt$	Junction-to-Case (Double-Side Cooled)
		-	.15	.26		Junction-to-Case (Single Side Cooled)
Critical Rate-of-Rise of Off-State Voltage (Higher values may cause device switching)	dv/dt	200	500	-	V/ μsec	$T_J = +125^\circ C$, Gate Open, V_{DRM} = Rated Linear or Exponential Rising Waveform Exponential $dv/dt = V_{DRM} (.632)/t$
Higher minimum dv/dt selections available - consult factory						
Holding Current	I_H	-	40	1000	mAdc	$T_C = +25^\circ C$, Anode Supply = 24 Vdc, Initial On-State Current = 2 Amps
DC Gate Trigger Current	I_{GT}	-	70	250	mAdc	$T_C = +25^\circ C$, $V_D = 6 Vdc$, $R_L = 3 Ohms$
		-	100	400		$T_C = -40^\circ C$, $V_D = 6 Vdc$, $R_L = 3 Ohms$
		-	25	175		$T_C = +125^\circ C$, $V_D = 6 Vdc$, $R_L = 3 Ohms$
DC Gate Trigger Voltage	V_{JT}	-	3	5	Vdc	$T_C = -40^\circ C$ to $0^\circ C$, $V_D = 6 Vdc$, $R_L = 3 Ohms$
		-	1.25	3.0		$T_C = 0^\circ C$ to $+125^\circ C$, $V_D = 6 Vdc$, $R_L = 3 Ohms$
		0.15	-	-		$T_C = 125^\circ C$, V_{DRM} , $R_L = 1000 Ohms$
Peak On-State Voltage	V_{TM}	-	1.9	2.6	Volts	$T_C = +25^\circ C$, $I_{TM} = 500 A.mps$, Peak Duty Cycle $\leq .01\%$
Turn-On Delay Time	t_d	-	0.5	-	μsec	$T_C = +25^\circ C$, $I_L = 50 Adc$, V_{DRM} , Gate Supply, 20 Volt Open Circuit, 20 Ohm, 0.1 μsec max. rise time, ††, †††
Conventional Circuit Commutated Turn-Off Time (with Reverse Voltage) Faster Maximum Turn-Off Times Available, Consult Factory	t_q	-	-	-	μsec	(1) $T_C = +125^\circ C$ (2) $I_{TM} = 150 Amps.$ (3) $V_R = 50 Volts Min.$ (4) V_{DRM} (Reapplied) (5) Rate-of-Rise of Reapplied Off-State Voltage = 200 V/ μsec (linear) (6) Commutation $di/dt = 5 Amps/\mu sec.$ (7) Repetition Rate = 1 pps. (8) Gate Bias During Turn-Off Interval = 0 Volts, 100 Ohms
	C364	-	8	10		
	C365	-	15	20		
Conventional Circuit Commutated Turn-Off Time (with Feedback Diode)	$t_{q(diode)}$	-	-	-	μsec	(1) $T_C = +125^\circ C$ (2) $I_{TM} = 150 Amps.$ (3) $V_R = 1 Volt$ (4) V_{DRM} (Reapplied) (5) Rate-of-Rise of Reapplied Forward Blocking Voltage = 200 V/ μsec (linear) (6) Commutation $di/dt = 5 Amps/\mu sec$ (7) Repetition Rate = 1 pps. (8) Gate Bias During Turn-Off Interval = 0 Volts, 100 Ohms.
	C364	-	15	†		
	C365	-	20	†		

† Consult factory for specified maximum Turn-Off Time.
 †† Delay time may increase significantly as the gate drive approaches the I_{GT} of the Device Under Test.
 ††† Current risetime as measured with a current probe, or voltage risetime across a non-inductive resistor.

C384/C385

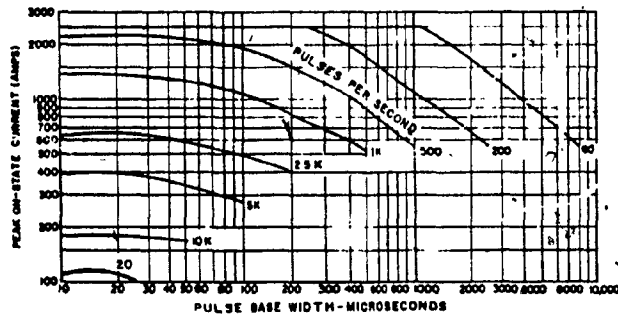


1. MAXIMUM ON-STATE CHARACTERISTICS

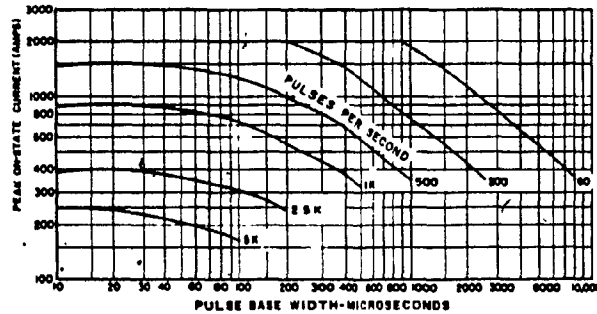


2. GATE TRIGGER CHARACTERISTICS AND POWER RATINGS

SINE WAVE CURRENT RATING DATA

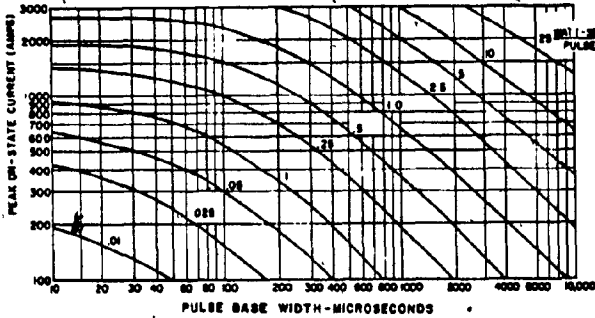


3. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH ($T_c = 65^\circ C$)



4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH ($T_c = 90^\circ C$)

C384/C365



B. ENERGY PER PULSE FOR SINUSOIDAL PULSES

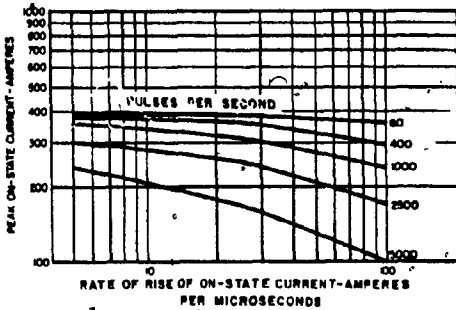
NOTES:

(Pertaining to Sine and Rectangular Wave Current Rating)

1. Switching voltage = 400 volts.
2. Reverse voltage applied = $V_R < 800$ volts.
3. Required gate drive:
20 volts, 65 ohms, 1 μ sec risetime for less than 100 amps/μsec.
20 volts, 20 ohms, .8 μ sec risetime for greater than 100 amps/μsec.
4. RC Snubber ckt. = 0.25 μ f, 5 Ω .
5. Double-Side Cooled.
6. Maximum energy dissipated during reverse recovery to be 15% of total W-S/P shown in W-S/P chart or 0.03 W-S/P, whichever is lesser.
7. Values of W-S/P are for $T_j = 125^\circ\text{C}$.

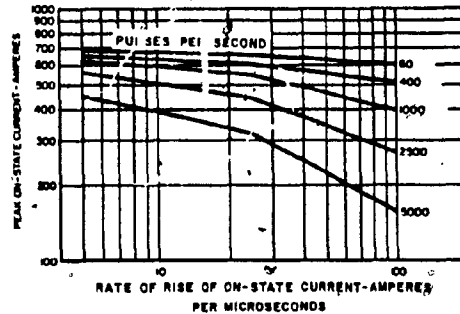
RECTANGULAR WAVE CURRENT RATING DATA

DUTY CYCLE - 50%

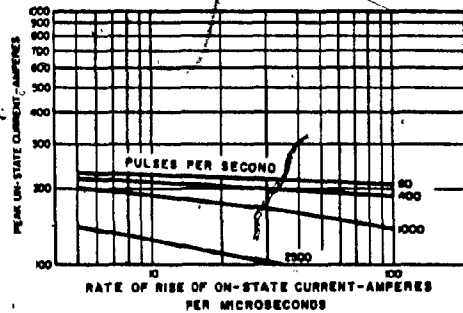


6. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. di/dt ($T_C = 65^\circ\text{C}$)

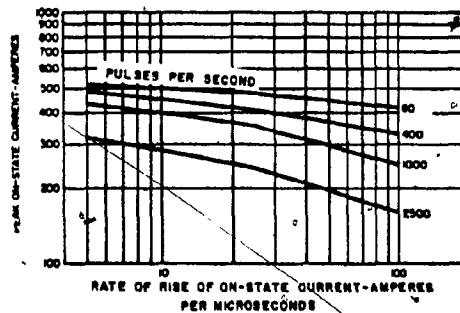
DUTY CYCLE - 25%



8. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. di/dt ($T_C = 65^\circ\text{C}$)



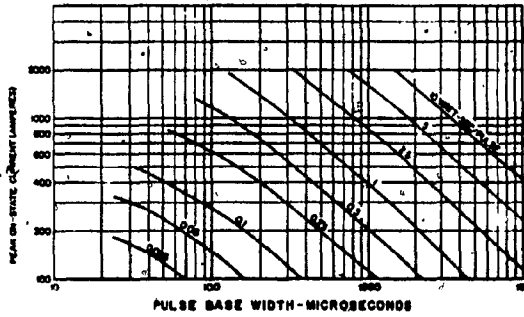
7. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. di/dt ($T_C = 90^\circ\text{C}$)



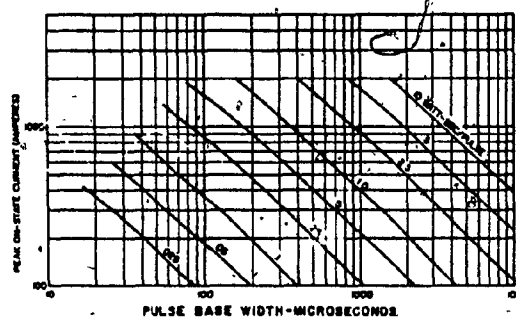
9. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. di/dt ($T_C = 90^\circ\text{C}$)

C364/C365

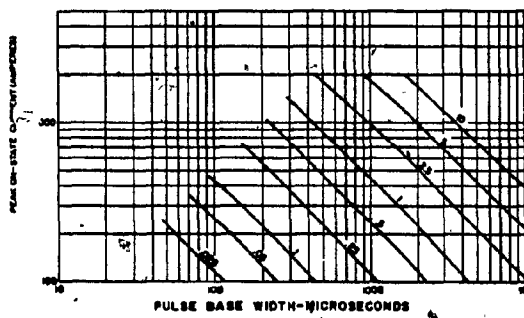
WATT-SECOND PER PULSE



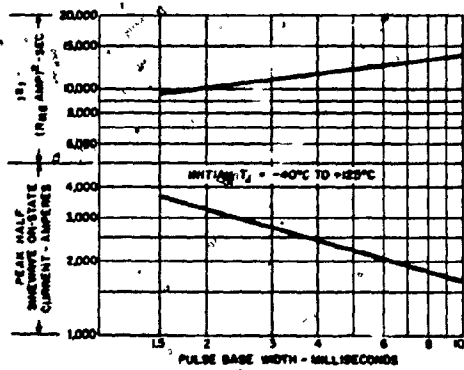
10. ENERGY PER PULSE VS. PEAK CURRENT AND PULSE WIDTH ($di/dt = 100 \text{ A}/\mu\text{sec}$)



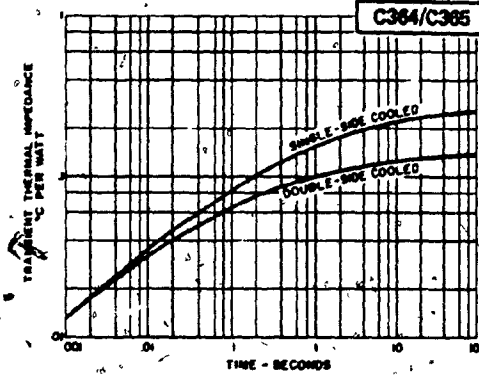
11. ENERGY PER PULSE VS. PEAK CURRENT AND PULSE WIDTH ($di/dt = 25 \text{ A}/\mu\text{sec}$)



12. ENERGY PER PULSE VS. PEAK CURRENT AND PULSE WIDTH ($di/dt = 5 \text{ A}/\mu\text{sec}$)



13. SUB-CYCLE SURGE (NON-REPETITIVE) ON-STATE CURRENT AND I^2t RATING



14. TRANSIENT THERMAL IMPEDANCE - JUNCTION-TO-CASE

OUTLINE DRAWING

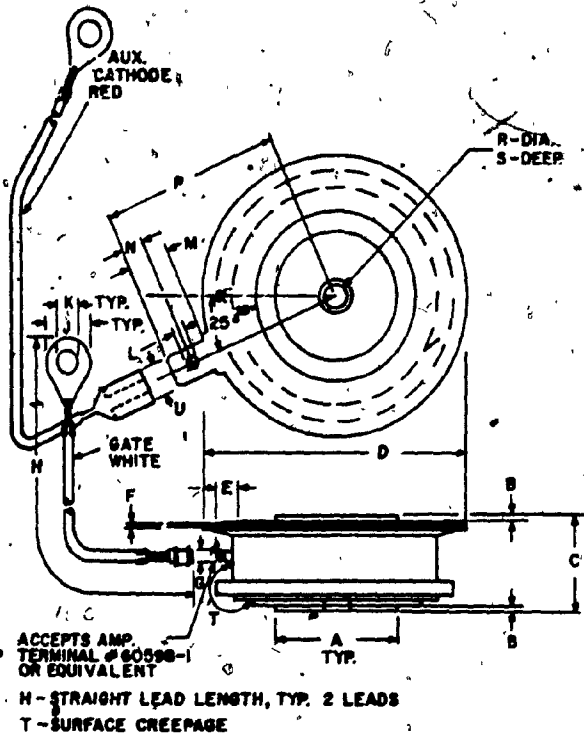


TABLE OF DIMENSIONS

Conversion Table

SYM	DECIMAL INCHES		METRIC MM	
	MIN.	MAX.	MIN.	MAX.
A	.744	.752	18.897	19.101
B	.030	.040	.762	1.524
C	.13	.565	13.081	14.351
D	1.800	1.856	40.84	42.06
E	.110	—	2.794	—
F	.031	.017	.330	.432
G	.057	.059	1.447	1.449
H	7.980	8.115	202.70	206.11
J	—	.300	—	7.620
K	.137	.153	3.479	3.886
L	.065	.070	1.651	1.778
M	.245	.260	6.223	6.604
N	.120	.140	3.048	3.556
P	1.080	1.125	27.69	28.55
R	.135	.146	3.429	3.683
S	.067	.063	1.701	2.108
T	.340	—	8.636	—
U	.186	.189	4.724	4.801

High Speed Fast Recovery Rectifier

A397

1500 Volts 400A Avg.

The A397 series is General Electric's highly reliable, all-diffused, Press-Pak, 400 ampere, fast recovery, silicon rectifier diode. These diodes are designed for use in high frequency applications or where a fast recovery diode is a necessity. These diodes provide a superior combination of speed, blocking voltage capability and soft recovery, which is required in such demanding applications as:

- Inverter Feedback Diode
- Free Wheeling Diode
- High Frequency Rectification
- Low EMI Power Supplies



FEATURES:

- Published Current Ratings Up To 20,000 Hz
- Soft Recovery With Low Recovery Charge
- All-Diffused
- Package Reversibility
- Rugged Glazed Ceramic Hermetic Package

MAXIMUM ALLOWABLE RATINGS AND SPECIFICATIONS

TYPE	REPETITIVE PEAK REVERSE VOLTAGE V_{RRM} $T_J = -40^\circ\text{C to } +125^\circ\text{C}$	NON-REPETITIVE ² PEAK REVERSE VOLTAGE, V_{RSM} $T_J = 25^\circ\text{C to } 125^\circ\text{C}$	DC REVERSE ² VOLTAGE, V_R $T_J = -40^\circ\text{C to } +125^\circ\text{C}$	REPETITIVE PEAK REVERSE CURRENT, I_{RRM} $T_J = 125^\circ\text{C}$
A397A	100 Volts	300 Volts	100 Volts	25 mA
A397B	200	300	200	25
A397C	300	400	300	25
A397D	400	500	400	25
A397E	500	600	500	25
A397M	600	720	600	25
A397S	700	840	700	25
A397N	800	950	800	25
A397T	900	1075	900	25
A397P	1000	1200	1000	25
A397PA	1100	1300	1100	25
A397PB	1200	1400	1200	25
A397PC	1300	1520	1300	25
A397PD	1400	1600	1400	25
A397PE	1500	1700	1500	25

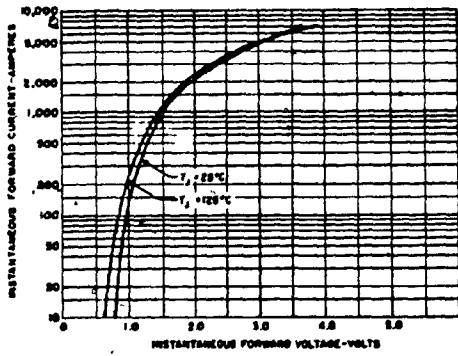
Peak Forward Current, I_{FM} ($T_C = +65^\circ\text{C}$, Half-Sine Wave Pulse Width = 8.3 msec., D.F. = 50%) 1200 Amperes
 Peak One-Cycle Surge (Non-Repetitive), Forward Current, I_{FSM} 5000 Amperes
 Minimum I^2t Rating (See Curve 11), $t \geq 1$ msec. (Non-Repetitive) 44,000 (RMS Ampere)² Seconds
 Thermal Resistance, $R_{\theta JC}$ (D.C.)095°C/Watt
 Storage Temperature, T_{stg} -40°C to +150°C
 Operating Junction Temperature, T_J -40°C to +125°C
 Mounting Force Required 800 Lbs \pm 10%
 3.56KN \pm 10%

NOTES:

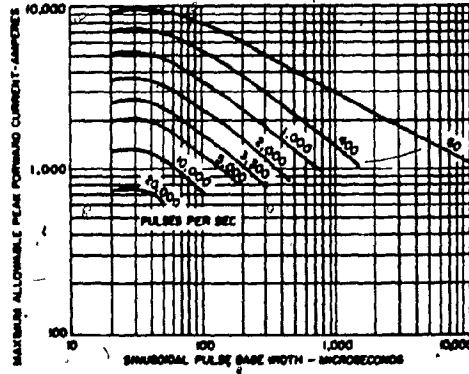
- ¹ Assumes a heatsink thermal resistance of less than 2.0°C/watt.
- ² Non-repetitive voltage and current ratings, as contrasted to repetitive ratings, apply for occasional or unpredictable overloads. For example, the forward surge current ratings are non-repetitive ratings that are used in fault coordination work.
- ³ Assumes a heatsink thermal resistance of less than 1.0°C/watt.

DEVICE SPECIFICATIONS

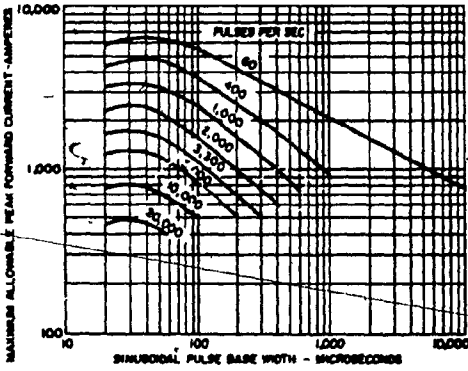
A397



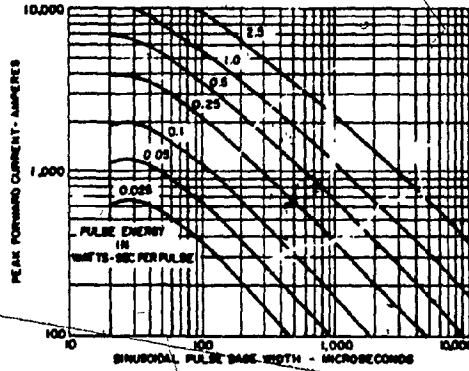
1. MAXIMUM FORWARD CHARACTERISTICS



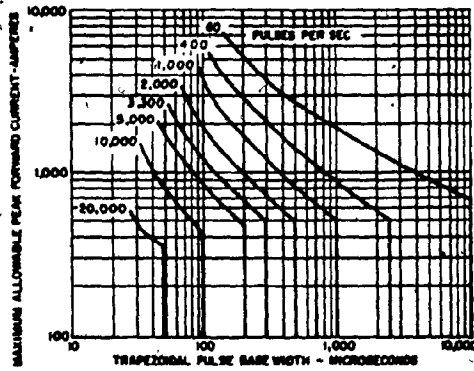
2. MAXIMUM ALLOWABLE PEAK FORWARD CURRENT SINUSOIDAL WAVEFORM ($T_c = 85^\circ\text{C}$) DOUBLE SIDE COOLED



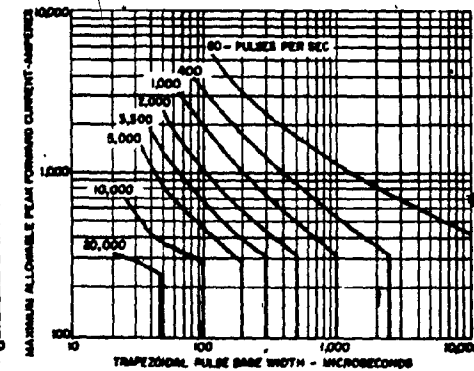
3. MAXIMUM ALLOWABLE FORWARD CURRENT SINUSOIDAL WAVEFORM ($T_c = 90^\circ\text{C}$) DOUBLE SIDE COOLED



4. SINUSOIDAL PULSE ENERGY ($T_j = 125^\circ\text{C}$)



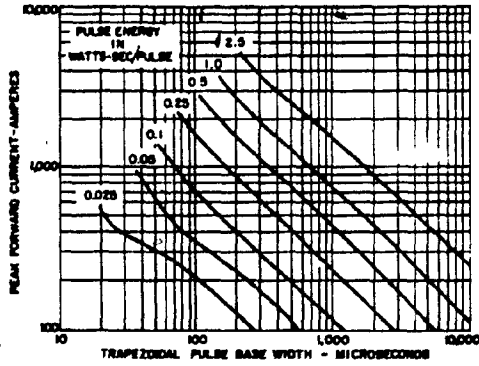
5. MAXIMUM ALLOWABLE PEAK FORWARD CURRENT TRAPEZOIDAL WAVEFORM ($T_c = 85^\circ\text{C}$) dI/dt (RISING & FALLING) = $100 \text{ A}/\mu\text{s}$ DOUBLE SIDE COOLED



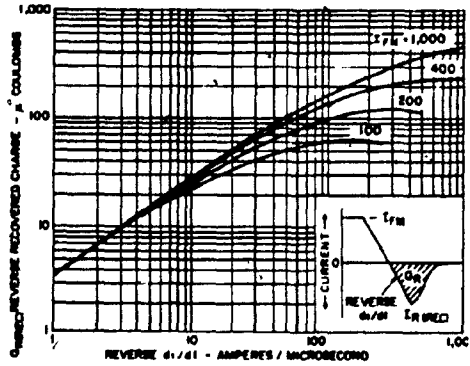
6. MAXIMUM ALLOWABLE PEAK FORWARD CURRENT TRAPEZOIDAL WAVEFORM ($T_c = 90^\circ\text{C}$) dI/dt (RISING & FALLING) = $100 \text{ A}/\mu\text{s}$ DOUBLE SIDE COOLED

DEVICE SPECIFICATIONS

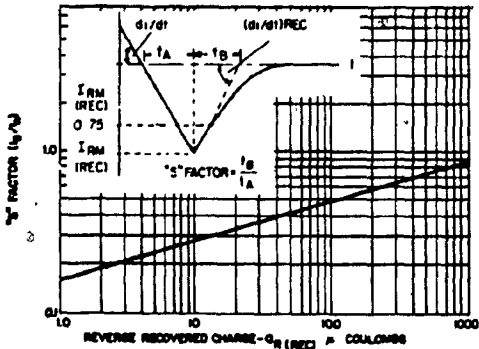
A387



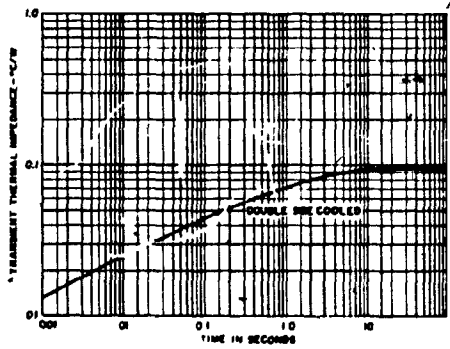
7. TRAPEZOIDAL PULSE ENERGY DI/DT (RISING & FALLING) = 100 A/μS (T_J = 125°C)



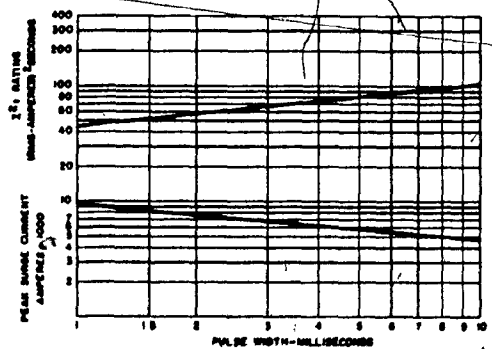
8. TYPICAL RECOVERED CHARGE (Maximum Recovered Charge Group 12) If maximum recovered charge group 12 is required, request A387 __ X9, e.g. A3878 X9, etc.



9. TYPICAL "S" FACTOR VERSUS RECOVERY CHARGE (T_J = 125°C)

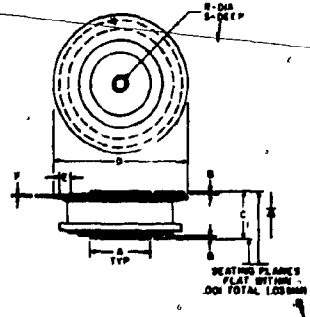


10. TRANSIENT THERMAL IMPEDANCE - JUNCTION-TO-CASE



11. SUB-CYCLE SURGE FORWARD CURRENT AND I²t RATING VERSUS PULSE TIME FOLLOWING RATED LOAD CONDITIONS

OUTLINE DRAWING TABLE OF DIMENSIONS



DIM	DECIMAL INCHES		METRIC MM	
	MIN	MAX	MIN	MAX
A	744	752	18.99	19.16
B	600	600	15	15.2
C	515	505	12.99	12.80
D	1.000	1.000	25.40	25.40
E	1.11		27.99	
F	821	817	20.80	20.65
G	126	140	3.17	3.54
H	651	653	16.53	16.58

SUGGESTED MOUNTING METHODS FOR PRESS-PAKS TO HEAT DISSIPATORS A397

When the Press-Pak is assembled to a heat sink in accordance with the following general instructions, a reliable and low thermal resistance interface will result

1. Check each mating surface for nicks, scratches, flatness and surface finish. The heat dissipator mating surfaces should be flat within .0005 inch/inch and have a surface finish of 63 micro-inches.
2. It is recommended that the heat dissipator be plated with nickel, tin, or silver. Bare aluminum or copper surfaces will oxidize in time resulting in excessively high thermal resistance.

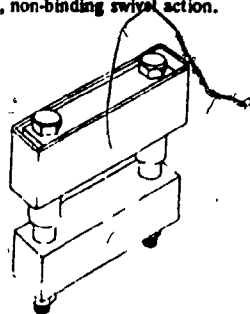
3. Sand each surface lightly with 600 grit paper just prior to assembly. Clean off and apply silicone oil (GF SF1154 200 centistoke viscosity) or silicone grease (GE G322L or Dow Corning DC 3, 4, 340 or 640). Clean off and apply again as a thin film. (A thick film will adversely affect the electrical and thermal resistance.)
4. Assemble with the specified mounting force applied through a self-leveling, swivel connection. The force has to be evenly distributed over the full area. Center holes on both top and bottom of the Press-Pak are for locating purposes only.

MOUNTING THE A397, ONE HALF INCH PRESS-PAK USING THE SERIES 1000 CLAMP

CLAMP FEATURES:

- *Hardened Steel Pivot* insuring constant pressure in rugged applications over long periods.
- One-piece phenolic insulator gives added 1/2" creep distance.
- Use of *special Force Indicator Gauge* eliminates need for torque wrenches, inaccurate "flex" gauges and guesswork.
- Various bolt lengths available to accommodate most mounting situations.
- No loose parts to complicate assembly.
- Stiffening *brace* to reinforce heat sink available upon request.

- Single-side cooling terminal available upon request.
- Positive, non-binding swivel action.



SERIES 1000

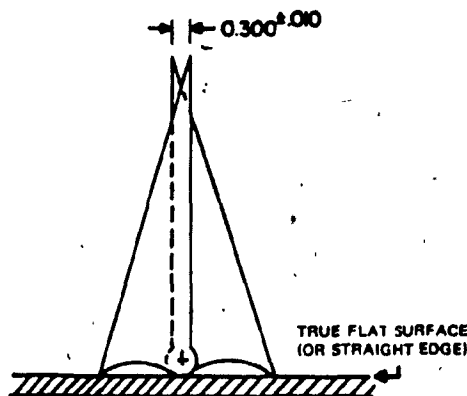
MOUNTING PROCEDURE:

With the semiconductor positively located in place on the heatsink(s), place the clamp in position with the bolts through the holes in the heatsink(s), and proceed as follows:

1. Refer to SCR Manual, Fifth Edition for Preparation of Mounting the Press-Pak SCR, 18.2.7.
2. Tighten the nuts evenly until finger tight.
3. Tighten each bolt 1/2 turn, using a 7/16 socket wrench on the bolt heads.
4. Place the Force Indicator Gauge firmly against the springs, as shown on the Outline Drawing, so that both ends and the middle are in solid contact with the springs. The holes of the gauge will then indicate the spring deflection, or force; correct mounting force is indicated when the holes coincide.

To Calibrate Force Gauge:

If the gauge is suspected of being out of calibration due to wear or damage, check it on a flat surface as shown below.



Examples:



Less than rated force. Tighten nuts alternately 1/4 turn at a time until points coincide.



Correct Force



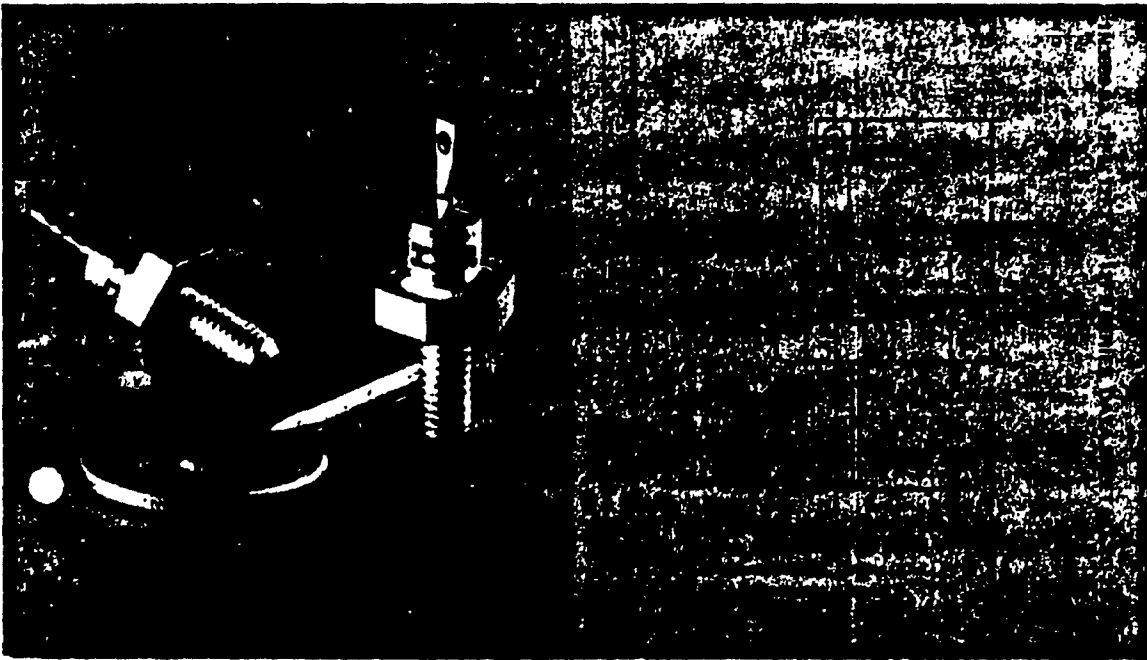
Excessive force. Loosen nuts and start over. NEVER try to adjust spring force by backing off the nuts, spring friction will produce false readings. Always start at Step 1.

If the points are not $0.300 \pm .010$ apart, calibrate the gauge by filing the bottom contact points.

1N3889-93, 12FL, 12FT & 12FV SERIES

12 Amp Fast Recovery Rectifiers

- Soft Recovery Characteristics
- For use in: Inverters, Sonar Power Supplies, Ultrasonic Systems and as Free-Wheeling Rectifiers
- Available to 1000 volts @ 350 nanosec
- Available to 600 volts @ 200 nanosec
- Data Sheet includes curves of recovery characteristics over wide range of operating conditions



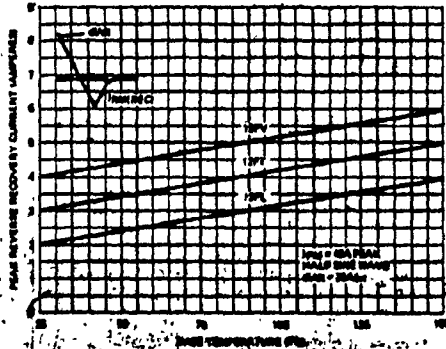


Fig. 7 - Typical Variation of Recovery Current with Temperature

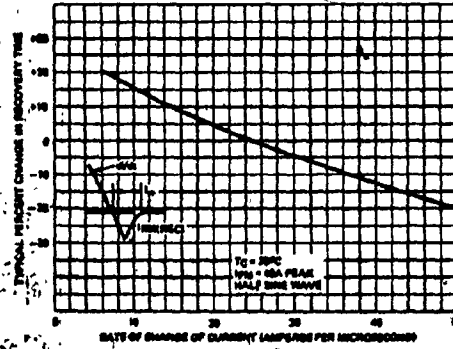


Fig. 8 - Typical Variation of Recovery Time with di/dt

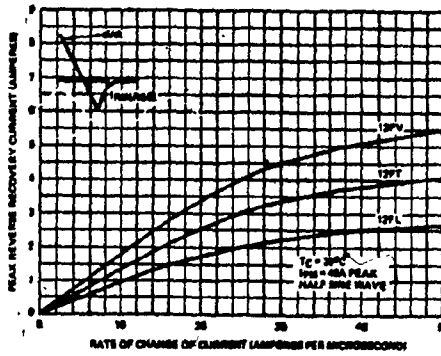


Fig. 9 - Typical Variation of Recovery Current with di/dt

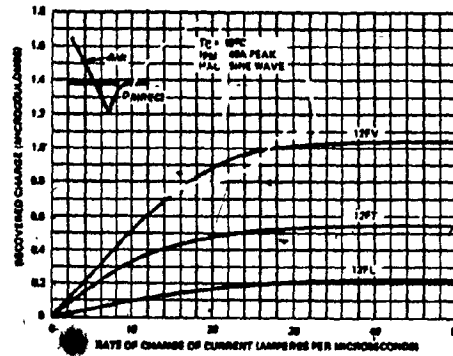


Fig. 10 - Typical Variation of Recovered Charge with di/dt

INTERNATIONAL RECTIFIER IOR

Semiconductor Division, 233 Kansas St., El Segundo, Calif. 90245 • Telex 67-4686 • Phone (213) 678-6281

Manufacturing facilities in United States, Canada, Great Britain, India, Italy and Japan. Sales offices and distributors in major cities throughout the world.

Printed in U.S.A. 3-73

INTERNATIONAL RECTIFIER **IR**

ELECTRICAL SPECIFICATIONS

	1N3888 12FL	12FT	12FV	UNITS	TEST CONDITIONS
$I_F(AV)$ Max. average forward current	12*	12	12	A	$T_C = 100^\circ C$, 1 phase operation
$I_{F(peak)}$ Max. peak one cycle non-repetitive	150*	150	150	A	60 Hz half sine wave following any rated load condition, non-repetitive
I^2t Max. I^2t for fusing (1)	93	93	93	A ² s	$t = 5$ to 8.3 msec
V_{FM} Max. peak forward voltage drop	1.4*	1.4	1.4	V	$I_F = 12A$ DC, $T_C = 25^\circ C$
	1.5*	1.5	1.5	V	$I_F = 12A$ average (37.8 A peak), $T_C = -65^\circ C$ to $100^\circ C$
$I_{R(AV)}$ Max. average reverse current, $V_R = 50$ to $800V$	5*	-	-	mA	$T_C = 100^\circ C$, V_{RM} = rated V_{RRM} , rated $I_F(AV)$, 1 phase operation
	-	10	10	mA	
I_R Max. DC reverse current, $V_R = 50$ to $800V$	3*	-	-	mA	V_R = rated dc value, $T_C = 100^\circ C$
	-	6	6	mA	
	25*	-	-	μA	V_R = rated dc value, $T_C = 25^\circ C$
	-	50	50	μA	
t_{rr} Max. reverse recovery time	200*	350	500	ns	$T_C = 5^\circ C$, $I_F = 1A$, $V_R = 30V$
	200	350	500	ns	$T_C = 25^\circ C$, $I_F = 40A$ peak, $dI/dt = 25A/\mu S$
$I_{RM}(REC)$ Max. peak reverse recovery current (recovery)	2*	3	4	A	$T_C = 25^\circ C$, $I_F = 1A$, $V_R = 30V$
	2	3	4	A	$T_C = 25^\circ C$, $I_F = 40A$ peak, $dI/dt = 25A/\mu S$

THERMAL MECHANICAL SPECIFICATIONS

T_J Junction operating temperature range	-65° to 150°C	
T_{stg} Storage temperature range	-65° to 175°C	
$R_{\theta JC}$ Max. thermal resistance, junction-to-case	2.0°C/W	DC operation
$R_{\theta CS}$ Thermal resistance, case-to-sink	0.6°C/W	Mounting surface flat, smooth, and greased
Mounting torque	Min. 12 lb-in. Max. 15 lb-in.	Non-lubricated threads
Approximate weight	% oz.	

VOLTAGE RATINGS

PART NUMBER†	V_{RRM} - Max. repetitive peak reverse voltage (V)	$V_R(RMS)$ - Max. RMS Reverse Voltage (V)	V_R - Max. DC Blocking Voltage (V)
1N3888 12FT5 12FV5	50*	35*	50*
1N3889 12FT10 12FV10	100*	70*	100*
1N3891 12FT20 12FV20	200*	140*	200*
1N3882 12FT30 12FV30	300*	210*	300*
1N3883 12FT40 12FV40	400*	280*	400*
12FL50 12FT50 12FV50	500	350	500
12FL60 12FT60 12FV60	600	420	600
- 12FT70 12FV70	700	490	700
- 12FT80 12FV80	800	560	800
- 12FT90 12FV90	900	630	900
- 12FT100 12FV100	1000	700	1000

(1) Multiply by 0.55 for $t = 1.5$ msec.

† Standard polarity - Stud is cathode. For reverse polarity, add "R" to base number: 1N3888R, 12FLRS.

* JEDEC registered value.

1N3888-83, 12FL, 12FT and 12FV Series, Data Sheet No. PD-2.030A

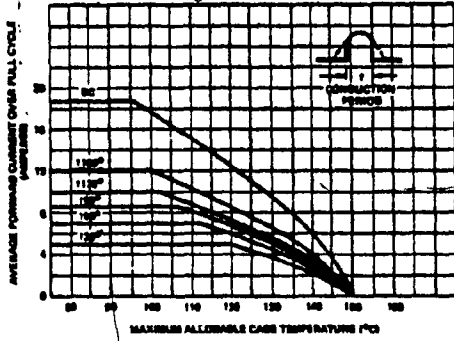


Fig. 1 - Average Forward Current Vs. Case Temperature

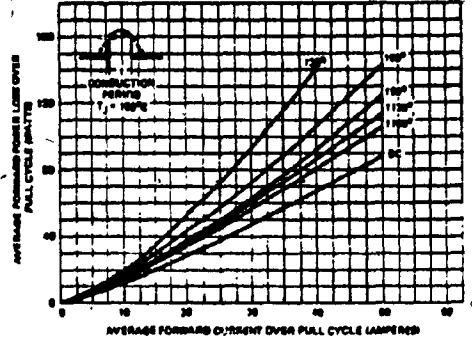


Fig. 2 - Maximum Average Forward Power Loss Vs. Average Forward Current

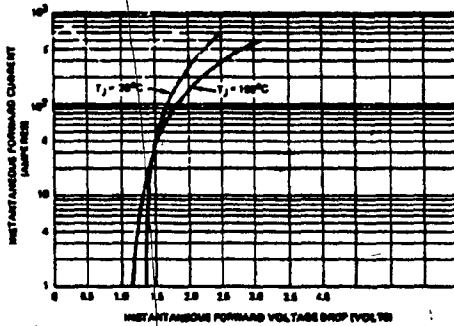


Fig. 3 - Maximum Instantaneous Forward Voltage Drop Vs. Instantaneous Forward Current

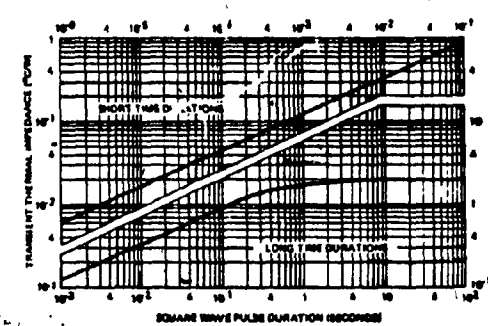


Fig. 4 - Maximum Transient Thermal Impedance, Junction to Case

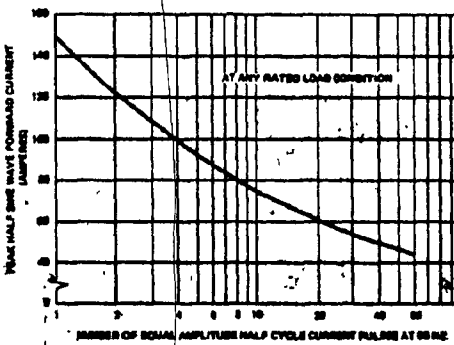


Fig. 5 - Maximum Non-Repetitive Surge Current

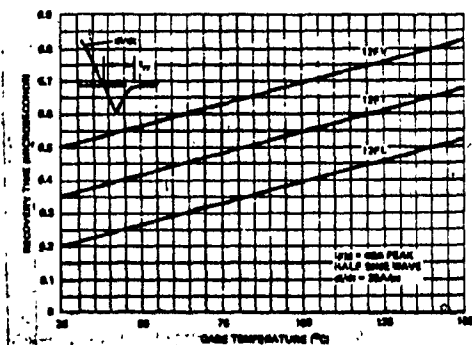


Fig. 6 - Typical Variation of Recovery Time with Temperature

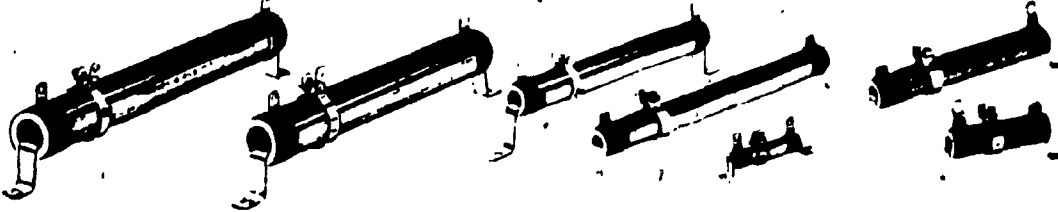


dividohm type 210 adjustable vitreous enameled resistors

"Dividohm" resistors make ideal voltage dividers for original equipment and replacement in transmitters, rectifiers and other apparatus. Such tapered "dividohms" are made by using one or more adjustable legs, or "dividers," which are also handy for adjusting and resistance values, for adjusting circuits, and for use on equipment which must be set to meet various line voltages.

"Dividohm" resistors are vitreous enameled resistors on which a narrow strip has been left uncoated to expose a section of each turn. Contact to any wire in this strip is made by an embossed contact on the adjustable leg (topical).

WATT RATING: The stated wattage rating applies only when the entire resistance is in the circuit. When the adjustable leg is set at an intermediate point, the wattage rating is reduced in proportion to the same proportion, i.e., if the leg is set at half the resistance, the wattage is reduced by one-half. A safe rule to follow is to make sure that the maximum rated current is not exceeded. This should be carefully checked particularly if the resistor will be used as a voltage divider with several adjustable legs. Resistance tolerance is $\pm 1\%$ for the total resistance value.



Resistor Value	12 WATT Core: 1 1/2" x 1/2" x 3/8" Mg. Cr. 71, 72, 73 Ar. Wt. 02 lb. Std. Mfg. Dist. No. 5			25 WATT Core: 2" x 1/2" x 3/8" Mg. Cr. 71, 72, 73 Ar. Wt. 03 lb. Std. Mfg. Dist. No. 9			50 WATT Core: 4" x 1/2" x 3/8" Mg. Cr. 71, 72, 73 Ar. Wt. 05 lb. Std. Mfg. Dist. No. 9			75 WATT Core: 6" x 1/2" x 3/8" Mg. Cr. 71, 72, 73 Ar. Wt. 07 lb. Std. Mfg. Dist. No. 9			100 WATT Core: 8" x 1/2" x 3/8" Mg. Cr. 71, 72, 73 Ar. Wt. 09 lb. Std. Mfg. Dist. No. 12			175 WATT Core: 8" x 1 1/2" x 3/8" Mg. Cr. 71, 72, 73 Ar. Wt. 13 lb. Std. Mfg. Dist. No. 14			225 WATT Core: 10" x 1 1/2" x 3/8" Mg. Cr. 71, 72, 73 Ar. Wt. 15 lb. Std. Mfg. Dist. No. 18		
	Cal. No.	Max. Amps.	Med. Ohm.	Cal. No.	Max. Amps.	Med. Ohm.	Cal. No.	Max. Amps.	Med. Ohm.	Cal. No.	Max. Amps.	Med. Ohm.	Cal. No.	Max. Amps.	Med. Ohm.	Cal. No.	Max. Amps.	Med. Ohm.	Cal. No.	Max. Amps.	Med. Ohm.
1	1000	3.46	0000	1.68	0000	7.87	3.21	0704	4.64	0000	10.8	1154	13.2	7.94	1004	15.08	10.10				
2	1000	2.43	0000	3.54	0000	5.00		0705	6.12	0000	7.01	4.68	1154	9.35	1004	10.64					
3	1000	2.00	0001	2.80	0000	4.87		0706	5.06	0000	5.77	4.00	1154	7.83	1004	8.67					
4	1000	1.54	0002	2.24	0000	3.14		0707	3.87	0000	4.47	3.00	1154	5.22	1004	6.72					
5	1000	1.25	0003	1.82	0000			0708	2.74	0000	3.16	4.30	1154	4.10	1004	4.74					
10	1000	1.00	0004	1.50	0001	2.23		0709	2.24	0000	2.00	3.00	1154	3.00	1004	3.00					
15	1000	0.90	0005	1.20	0002	1.41		0710	1.73	0000	1.80	2.50	1154	2.10	1004	2.10					
20	1000	0.80	0006	1.00	0003	1.00		0711	1.22	0000	1.41	2.00	1154	1.50	1004	1.50					
25	1000	0.75	0007	0.90	0004	0.90		0712	1.12	0000	1.20	1.80	1154	1.20	1004	1.20					
30	1000	0.70	0008	0.80	0005	0.80		0713	1.01	0000	1.00	1.60	1154	1.00	1004	1.00					
40	1000	0.65	0009	0.70	0006	0.70		0714	0.91	0000	0.90	1.40	1154	0.90	1004	0.90					
50	1000	0.60	0010	0.60	0007	0.60		0715	0.81	0000	0.80	1.20	1154	0.80	1004	0.80					
60	1000	0.55	0011	0.55	0008	0.55		0716	0.71	0000	0.70	1.00	1154	0.70	1004	0.70					
75	1000	0.50	0012	0.50	0009	0.50		0717	0.61	0000	0.60	0.90	1154	0.60	1004	0.60					
100	1000	0.45	0013	0.45	0010	0.45		0718	0.51	0000	0.50	0.80	1154	0.50	1004	0.50					
150	1000	0.40	0014	0.40	0011	0.40		0719	0.41	0000	0.40	0.70	1154	0.40	1004	0.40					
200	1000	0.35	0015	0.35	0012	0.35		0720	0.31	0000	0.30	0.60	1154	0.30	1004	0.30					
250	1000	0.30	0016	0.30	0013	0.30		0721	0.21	0000	0.20	0.50	1154	0.20	1004	0.20					
300	1000	0.25	0017	0.25	0014	0.25		0722	0.11	0000	0.10	0.40	1154	0.10	1004	0.10					
350	1000	0.20	0018	0.20	0015	0.20		0723	0.11	0000	0.10	0.30	1154	0.10	1004	0.10					
400	1000	0.18	0019	0.18	0016	0.18		0724	0.11	0000	0.10	0.20	1154	0.10	1004	0.10					
450	1000	0.17	0020	0.17	0017	0.17		0725	0.11	0000	0.10	0.15	1154	0.10	1004	0.10					
500	1000	0.16	0021	0.16	0018	0.16		0726	0.11	0000	0.10	0.10	1154	0.10	1004	0.10					
550	1000	0.15	0022	0.15	0019	0.15		0727	0.11	0000	0.10	0.08	1154	0.10	1004	0.10					
600	1000	0.14	0023	0.14	0020	0.14		0728	0.11	0000	0.10	0.06	1154	0.10	1004	0.10					
650	1000	0.13	0024	0.13	0021	0.13		0729	0.11	0000	0.10	0.05	1154	0.10	1004	0.10					
700	1000	0.12	0025	0.12	0022	0.12		0730	0.11	0000	0.10	0.04	1154	0.10	1004	0.10					
750	1000	0.11	0026	0.11	0023	0.11		0731	0.11	0000	0.10	0.03	1154	0.10	1004	0.10					
800	1000	0.10	0027	0.10	0024	0.10		0732	0.11	0000	0.10	0.02	1154	0.10	1004	0.10					
850	1000	0.09	0028	0.09	0025	0.09		0733	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
900	1000	0.08	0029	0.08	0026	0.08		0734	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
950	1000	0.07	0030	0.07	0027	0.07		0735	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
1000	1000	0.06	0031	0.06	0028	0.06		0736	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
1100	1000	0.05	0032	0.05	0029	0.05		0737	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
1200	1000	0.04	0033	0.04	0030	0.04		0738	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
1300	1000	0.03	0034	0.03	0031	0.03		0739	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
1400	1000	0.02	0035	0.02	0032	0.02		0740	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					
1500	1000	0.01	0036	0.01	0033	0.01		0741	0.11	0000	0.10	0.01	1154	0.10	1004	0.10					

Use "Screw Driver Type Adjustable Leg" is supplied with each unit. Legs with a silver contact button can be ground from the wire shown below.

MOVING THE LEGS MUST ALWAYS BE DONE AT LEAST TEMPORARILY BEFORE MOVING AND NOT MOVED GREAT WHILE THE CURRENT IS OFF IN ORDER TO PROTECT THE EXPOSED WIRE FROM MECHANICAL OR ELECTRICAL TAPPE AND TO PROTECT THE OPERATOR FROM DANGEROUS VOLTAGES.



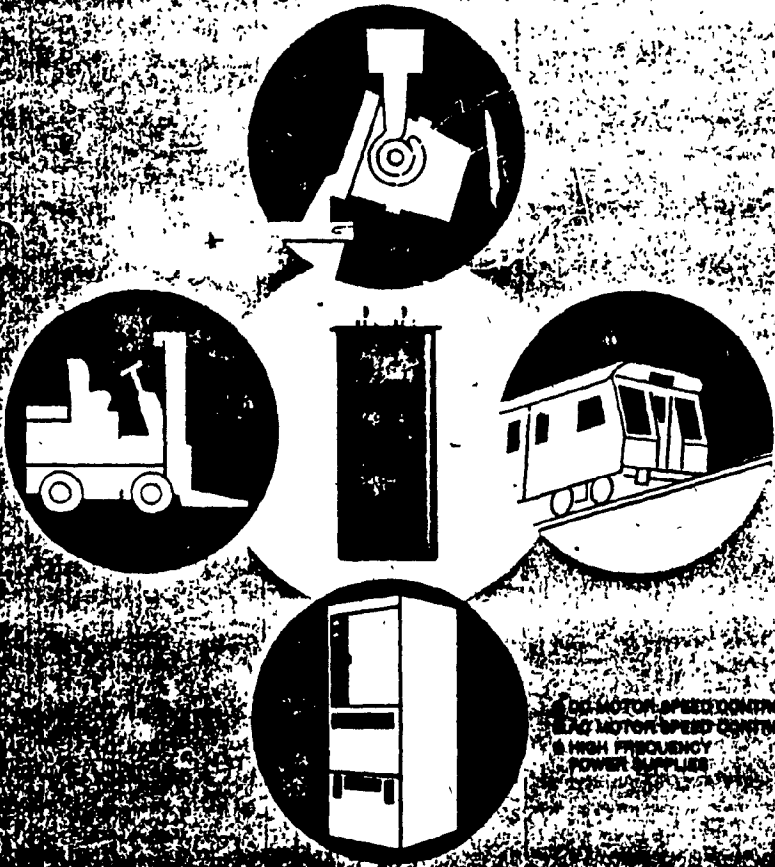
STANDARD				SILVER CONTACT BUTTONS			
Core Dist.	Core Dist.	Core Dist.	Core Dist.	Core Dist.	Core Dist.	Core Dist.	Core Dist.
1 1/2"	2"	4"	6"	8"	10"	12"	15"
0.01	0.02	0.05	0.10	0.15	0.20	0.30	0.40
0.02	0.04	0.10	0.20	0.30	0.40	0.60	0.80
0.05	0.10	0.20	0.30	0.40	0.60	0.80	1.00
0.10	0.20	0.30	0.40	0.60	0.80	1.00	1.50
0.20	0.30	0.40	0.60	0.80	1.00	1.50	2.00
0.30	0.40	0.60	0.80	1.00	1.50	2.00	3.00
0.40	0.60	0.80	1.00	1.50	2.00	3.00	4.00
0.60	0.80	1.00	1.50	2.00	3.00	4.00	6.00
0.80	1.00	1.50	2.00	3.00	4.00	6.00	8.00
1.00	1.50	2.00	3.00	4.00	6.00	8.00	10.00
1.50	2.00	3.00	4.00	6.00	8.00	10.00	15.00
2.00	3.00	4.00	6.00	8.00	10.00	15.00	20.00
3.00	4.00	6.00	8.00	10.00	15.00	20.00	30.00
4.00	6.00	8.00	10.00	15.00	20.00	30.00	40.00
6.00	8.00	10.00	15.00	20.00	30.00	40.00	60.00
8.00	10.00	15.00	20.00	30.00	40.00	60.00	80.00
10.00	15.00	20.00	30.00	40.00	60.00	80.00	100.00

This adjustable leg, which is threaded at both ends, features two adjustment — one at adjustment and one change of adjusting the resistance wire while making legs. Available for 1/2" core. Catalog No. 210B \$4.31

New 28F Series Capacitors For SCR Commutation Applications

STANDARD RATING RANGE FROM 25 TO 1000 A, 100 TO 5000 VOLTS MAX.

Amherst



DC MOTOR SPEED CONTROL
AC MOTOR SPEED CONTROL
& HIGH FREQUENCY
POWER SUPPLIES

GENERAL  ELECTRIC

Industry's most complete line of SCR capacitors

CAPACITOR SELECTION (Cont.) STANDARD RATINGS

2. Pulse width less than 50 μ sec. Given:
 Capacitance: 5 MFD = 10 percent
 Voltage: 65 VAC, 16.6 KHz continuous
 sine wave
 Current: 34 amps RMS
 Temperature: 80 C
- a. Select a 5 MFD unit with an 80 C
 current rating near 34 amps RMS.
 28F1248FC has a current rating of
 30.6 for 50 microseconds.
- b. The current multiplier for 16.6 KHz
 (pulse width = 30 microseconds) from
 Fig. 5 is 1.2.
- c. Allowable current for Cat. No. 28F-
 1248FC at 16.6 KHz is (1.2) (30.6) =
 36.7 amps RMS.
- d. Since the allowable current of 36.7
 amps is greater than the required
 value of 34 amps RMS, this unit is
 adequate.

The following two examples are typical
 of SCR commutating applications in-
 volving unidirectional or bidirectional
 square waveforms such as those found
 in variable AC and DC motor speed con-
 trols, power inverters and other low fre-
 quency applications with fast voltage
 rise times.

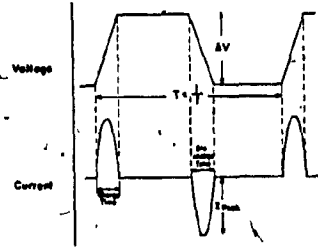


Fig. 4

1. Unidirectional square wave
 Given:
 Capacitance: 20 MFD = 10 percent
 Voltage: 600 Vpk square wave 200 Hz
 rep rate
 Current: Half sine wave pulses 60
 microseconds wide
 Temperature: 60 C ambient
- a. Determine RMS current:

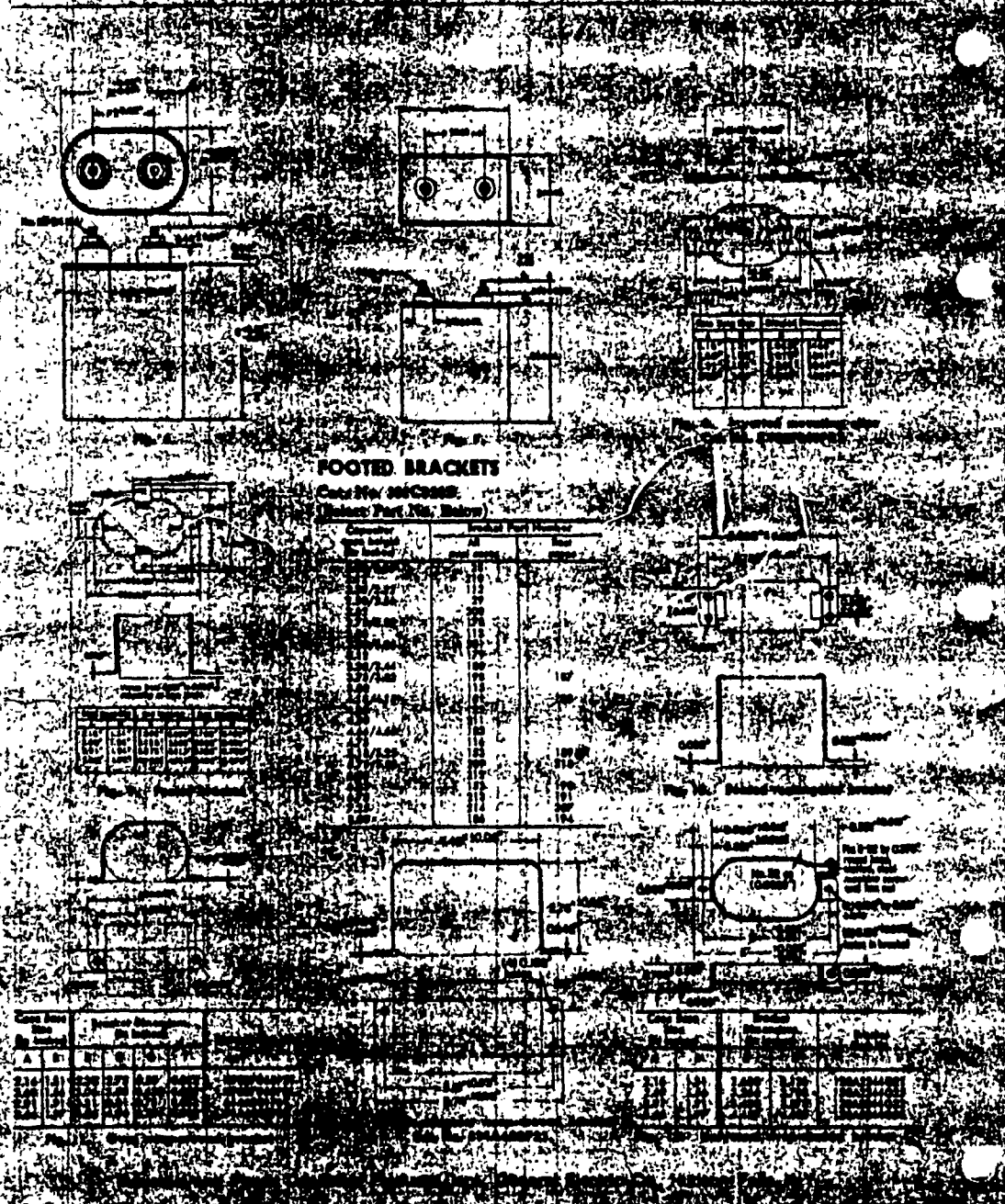
$$I_{RMS} = \frac{CAV}{0.64} \frac{(20)(600)}{(0.64)(60)} = 313 \text{ Amps}_{pk}$$

$$I_{RMS} = I_{pk} \sqrt{\frac{1}{2} \times f} = \frac{313 \sqrt{60 \times 10^{-6} \times 200}}{\sqrt{2}} = 34.2 \text{ amps RMS}$$

Dielectric	Manufacture Rating			Dimensions in inches			Fig. No.	Max. RMS (Amperes) At Max. Ambient Temp								
	Volts DC	μf	Catalog Number	A	B	C		60 C	70 C	80 C						
Paper	200	1	28F1010FC 28F1022FC 28F1033FC 28F1048FC 28F1077FC 28F1088FC	2.16	1.31	2.06	0.81	200	8.9	4.4	3.8 Δ					
	200	2						200	17.8	9.3	5.3					
	200	3						200	22.1	14.3	9.4					
	200	10						200	32.4	24.2	15.1					
	200	15						200	37.7	27.9	16.1					
	200	20						200	32.4	24.9	22.4					
	200	30						200	64.7	50.9	29.4					
	200	40						200	81.1	59.9	34.4					
	400	1						28F1109FC 28F1111FC 28F1122FC 28F1133FC 28F1148FC 28F1177FC 28F1188FC	2.16	1.31	2.06	0.81	400	7.3	5.4	3.1 Δ
	400	2											400	14.0	10.3	4.0
400	3	400	14.0	10.3	4.0											
400	10	400	26.6	19.7	11.4											
400	15	400	32.4	24.2	15.1											
400	20	400	44.9	34.6	20.0											
400	30	400	65.3	48.2	27.8											
400	40	400	87.1	64.0	35.0											
400	50	400	89.4	64.0	38.1											
Paper	600	1	28F1209FC 28F1211FC 28F1222FC 28F1233FC 28F1248FC 28F1277FC 28F1288FC	2.16	1.31	2.31	0.81						600	7.7	5.7	3.2 Δ
	600	2						600	10.4	7.7	4.2 Δ					
	600	3						600	5.6	11.5	6.7					
	600	10						600	17.3	20.2	11.7					
	600	15						600	39.0	28.9	24.4					
	600	20						600	49.2	34.3	21.0					
	600	25						600	59.2	44.0	25.4					
	600	30						600	71.1	52.5	29.3					
	600	40						600	79.1	54.9	33.7					
	600	50						600	93.8	70.8	40.8					
Paper	1000	1	28F1309FC 28F1311FC 28F1322FC 28F1333FC 28F1348FC 28F1377FC	2.16	1.31	2.06	0.81	1000	5.1	3.9	2.2 Δ					
	1000	2						1000	8.9	6.5	3.8 Δ					
	1000	3						1000	12.1	8.9	5.2					
	1000	5						1000	18.3	13.3	7.8					
	1000	10						1000	33.3	24.5	14.1					
	1000	15						1000	43.0	33.0	19.0					
Paper	1500	0.5	28F1411FC 28F1422FC 28F1433FC 28F1448FC	2.16	1.31	2.06	0.81	1500	3.6	2.7	1.5 Δ					
	1500	1						1500	6.3	4.6	2.7 Δ					
	1500	2						1500	11.0	8.2	4.7					
	1500	3						1500	15.0	11.1	6.4					
	1500	5						1500	23.5	17.3	10.0					
	1500	10						1500	37.3	27.4	15.9					
Paper	2000	0.25	28F1511FC 28F1522FC 28F1533FC 28F1548FC 28F1577FC	2.16	1.31	2.06	0.81	2000	2.6	1.9	1.1 Δ					
	2000	0.50						2000	4.0	3.0	1.7 Δ					
	2000	1						2000	6.6	4.9	2.8 Δ					
	2000	2						2000	11.9	8.9	5.1					
	2000	3						2000	16.8	11.7	6.8					
	2000	5						2000	25.6	18.9	10.9					
Poly-carbonate	2000	10	2000	41.2	30.4	17.8										
	400	1	28F1248FC 28F1277FC 28F1288FC 28F1299FC	2.16	1.31	2.06	0.81	400	21.0	15.3	9.0					
	400	2						400	34.0	23.3	14.8					
	400	3						400	33.0	23.0	19.5					
	400	5						400	72.0	52.0	30.6					
	400	10						400	120.0	89.3	57.0					
400	20	400						189.0	148.0	84.0						
Metallized Paper	200	25	28F1101FC 28F1102FC 28F1103FC 28F1107FC	2.49	1.56	2.12	0.81	120	12.5	9.7	4.7 Δ					
	200	50						120	20.4	15.8	7.7 Δ					
	200	100						120	34.9	26.8	13.0 Δ					
	200	150						120	43.3	33.3	16.3 Δ					

* See "Max. RMS Volts AC" column for a-c Rating.
 † Based on 50 microsecond pulse width.
 ‡ This number is given for purposes of derating only. In no case may capacitor be operated at currents in excess of 50 amps RMS.
 § This number is given for purposes of derating only. In no case may capacitor be operated at currents in excess of 12 amps RMS.
 ¶ This number is given for purposes of derating only. In no case may capacitor be operated at currents in excess of 20 amps RMS.
 Δ These designs use tinned copper straps instead of braided cable leads as the RMS current ratings make the use of cable unnecessary.

Standard Case Dimensions



GENERAL ELECTRIC

Fast Recovery Rectifier

2.0 Amps

200-600 Volts

A114B
A114C
A114D
A114E
A114M

THE GENERAL ELECTRIC A114 IS A 2.0 AMPERE, AXIAL-LEADED, FAST RECOVERY RECTIFIER. DUAL HEATSINK CONSTRUCTION PROVIDES RIGID MECHANICAL SUPPORT FOR THE PELLETT AND EXCELLENT THERMAL CHARACTERISTICS. PASSIVATION AND PROTECTION OF THE PN JUNCTION OF THE SILICON PELLETT ARE PROVIDED BY SOLID GLASS; NO ORGANIC MATERIALS ARE PRESENT WITHIN THE HERMETICALLY-SEALED PACKAGE.

absolute maximum ratings: (25°C unless otherwise specified)

	A114B	A114C	A114D	A114E	A114M	
Reverse Voltage (-65°C to +150°C, T _J)	200	300	400	500	600	Volts
Working Peak, V _{RM}	200	300	400	500	600	Volts
Repetitive Peak, V _{RM}	200	300	400	500	600	Volts
DC, V _M	200	300	400	500	600	Volts
Average Forward Current, I _F	←----- 1.0 -----→					Ampere
75°C ambient (see Rating Curves)						←----- 2.0 -----→
25°C "	←----- 40 -----→					
Peak Surge Forward Current, I _{FSM}						←----- 85 -----→
Non-rep., .0083 sec., half sine wave, Full load JEDEC method	←----- 3.5 -----→					
Non-rep., .001 sec., half sine wave, Full load @ +150°C, T _J						←----- -65°C to +150°C -----→
I ² t (for fusing), RMS	←----- -65°C to +175°C -----→					
.001 to .01 seconds						
Junction Temperature Range						
Operating, T _J						
Storage, T _{STG}						

Mounting: Any position. Lead temperature 290°C max. to 1/8" from body for 5 seconds max. during mounting.

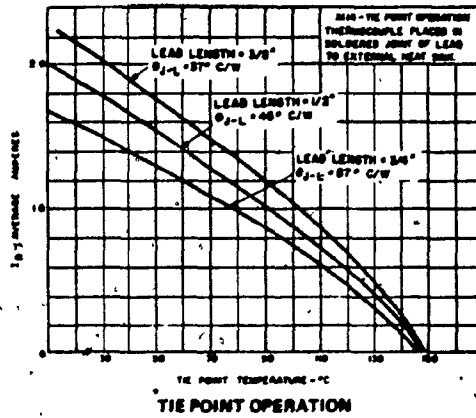
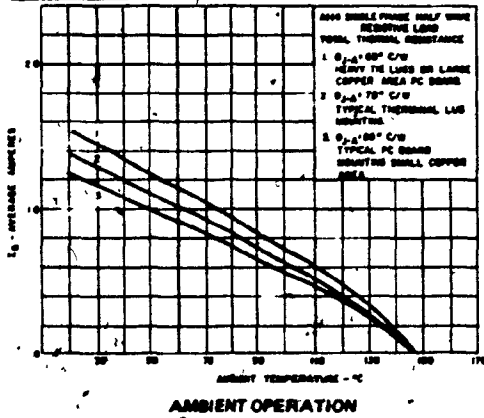
electrical characteristics: (25°C unless otherwise specified)

Maximum Forward Voltage Drop, V _{FM}	←----- 1.1 -----→					Volts
I _{FM} = 1.0A, T _A = +25°C						
Maximum Reverse Current, I _{RM} @ rated V _{RM}	5	5	5	5	5	Microamps.
T _J = +25°C	300	300	300	200	200	Microamps.
T _J = +150°C	1	1	1	1	1	Microamps.
Typical I _{RM} @ 25°C	←----- 140 -----→					Nanosecs.
Typical Reverse Recovery Time, t _r	←----- 200 -----→					Nanosecs.
Maximum Reverse Recovery Time, t _r						

Recovery circuit per MIL-S-19500/286C.

A114B
A114C
A114D
A114E
A114M

CIRCUIT DESIGN INFORMATION
MAXIMUM ALLOWABLE DC OUTPUT CURRENT RATINGS
SINGLE PHASE, RESISTIVE AND INDUCTIVE LOADS



CAPACITIVE LOADS

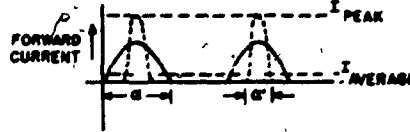
Current Densities (capacitive load)

Average forward current as specified under maximum ratings, page 1, and derating curves for high temperature operation, above, must be corrected for applications with capacitive loads. As the current conduction angle, α , is decreased, the peak current required to maintain the same average current increases, i.e., the peak-to-average current ratio increases from 3.14. Figure 3 gives the derating required based on this increase in peak to average current ratio for sine wave operation. For more complete information consult Application Note 200.30.

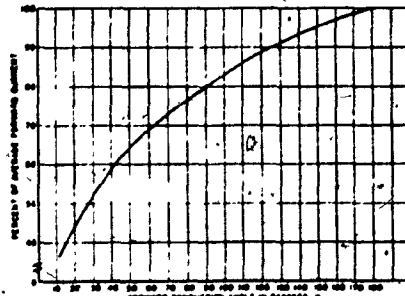
- METHOD:**
- Determine conduction angle α in degrees for particular circuit as designed.
 - Enter Figure 3 for the particular conduction angle and read corresponding percent of forward current per cell.
 - Multiply this value times average forward current for resistive load from figures 1 and 2 as given for the actual ambient or tie point temperature required.

See Typical Examples Below

TYPICAL EXAMPLES (25°C Ambient Temperature)					
	Example No. 1	Example No. 2	Example No. 3	Example No. 4	Units
Conduction Angle (α)	170	110	130	70	Degrees
Rated Average Current (Resistive Load)	1	1	1	1	Amp.
% of Average Current	0.98	0.86	0.92	0.73	%
Rated Average Current (Capacitive Load)	0.98	0.86	0.92	0.73	Amps.



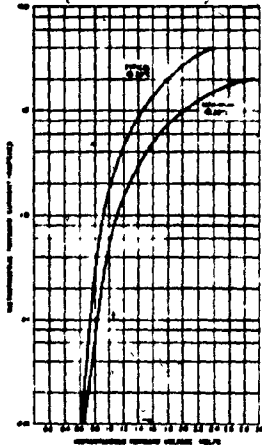
α = CONDUCTION ANGLE (DEG)
 α' = SHORTENED CONDUCTION ANGLE
OSCILLOSCOPE PRESENTATION



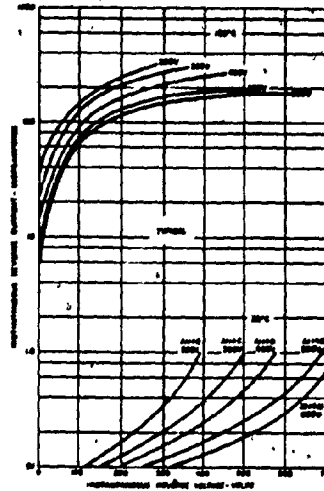
DERATING FOR SHORTENED CONDUCTION ANGLE

TYPICAL CHARACTERISTICS

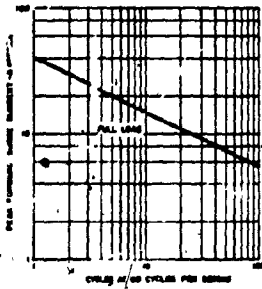
A114B
A114C
A114D
A114E
A114M



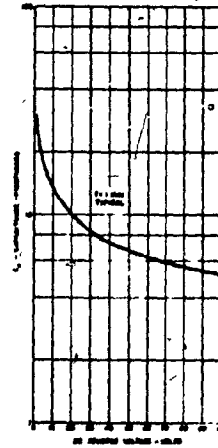
FORWARD CHARACTERISTICS



REVERSE CHARACTERISTICS

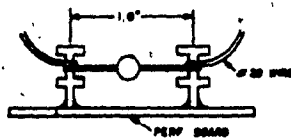


MAXIMUM NON-REPETITIVE MULTICYCLE FORWARD SURGE CURRENT

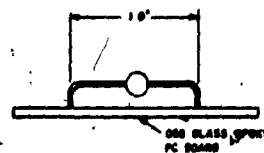


JUNCTION CAPACITANCE

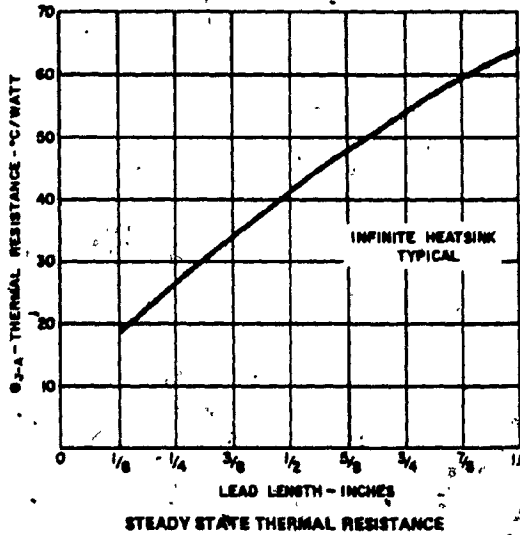
TYPICAL TIE LUG MOUNTS



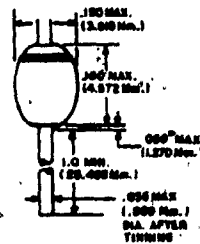
TYPICAL PC BOARD MOUNTING



A114B
A114C
A114D
A114E
A114M



Marking band to appear on cathode end.



ALL DIMENSIONS ARE IN INCHES AND (METRIC)
 *WELD AND SOLDER FLASH NOT CONTROLLED IN THIS AREA

OUTLINE DRAWING

HAMMOND PULSE TRANSFORMERS 610

- Available in 3 different mounting types.
- Rise times and insulation suitable for use in SCR firing circuits.
- Special types up to 100KV and high powers available on special order.

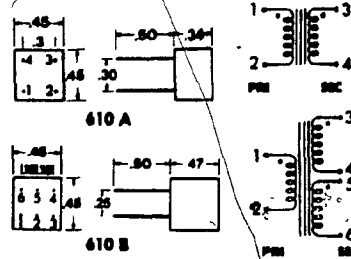
610 SERIES

- Epoxy cast with printed circuit pins.
- Weighs only 0.5 oz.
- These may be produced to MIL-T-27 on request.



Cat. No.	Ratio	Circuit Volts (max.)	L _p mH	D.C. Res. (Ω)		Insulation test (rms volts)	Wt. oz.
				R _p	R _{s2}		
610 A	1:1	250	5.2	3.4	3.9	1000	
610 B	1:1	250	4.8	2.1	1.85	2.3	1000

NOTE - 610 A is replacement for old part #64287 and 610 B for #70303.

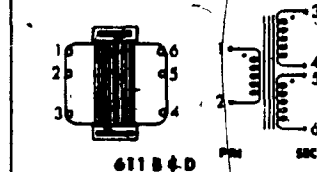
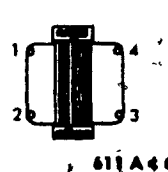
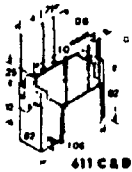


611 SERIES

Open bracket frame
with printed circuit
pins on 0.1 grid.

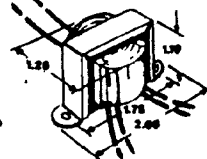
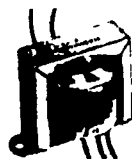


Cat. No.	Ratio	Circuit Volts (max.)	L _p mH	D.C. Res. (Ω)		Insulation test (rms volts)	Wt. oz.
				R _p	R _{s2}		
611 A	1:1	125	8.6	0.45	0.55	1000	0.7
611 B	1:1	125	17.2	1.26	1.0	1000	0.7
611 C	1:1	250	56	3.31	4.46	1500	1.2
611 D	1:1	250	17	1.73	1.31	1500	1.2

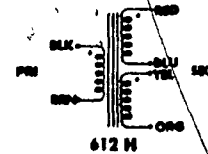
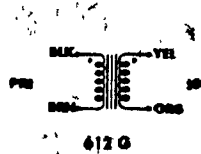


612 SERIES

Open horizontal bracket mounting with
4" flexible leads.



Cat. No.	Ratio	Circuit Volts (max.)	L _p mH	D.C. Res. (Ω)		Insulation test (rms volts)	Wt. oz.	
				R _p	R _{s2}			
612 G	1:1	600	6.6	0.87	0.87	4000	8.0	
612 H	1:1	600	1.5	0.45	0.42	0.49	4000	8.0



SUPERSEDES PREVIOUS ISSUE

WE RESERVE THE RIGHT TO REVISE THIS DESIGN WITHOUT PRIOR NOTICE

EFFECTIVE FEBRUARY 1974

HAMMOND MANUFACTURING COMPANY LIMITED

QUELPH, ONT. CAN. N1M 1E5

TELEPHONE • QUELPH (416) 822-2990 • TORONTO (416) 364-3267 • TELEFAX 066-58523

Data Sheet No. PD-8.002

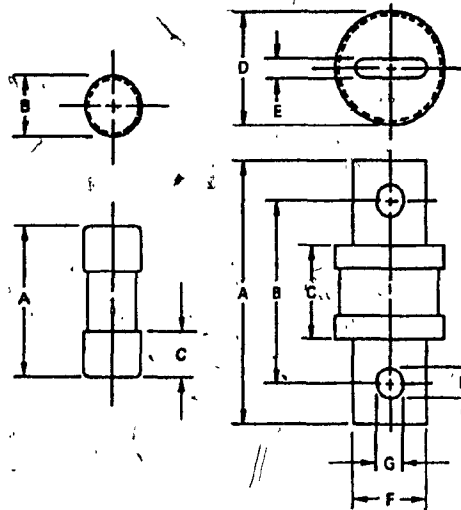
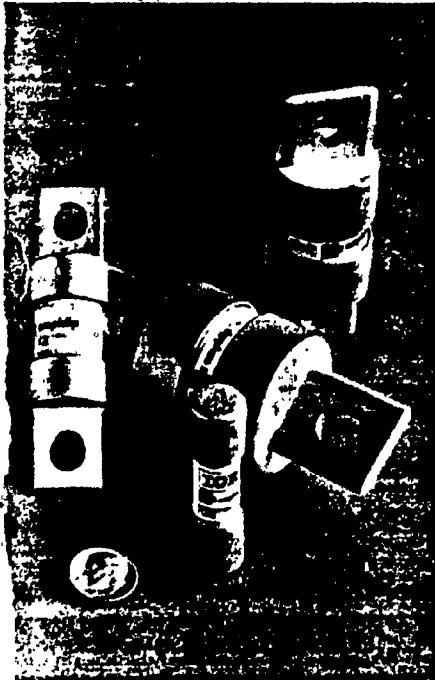
INTERNATIONAL RECTIFIER 

SF25X SERIES semiconductor fuses

250 Volt ampklip Semiconductor Fuses

Designed specifically to protect semiconductor devices

- 250 volts RMS, 10 to 600 amps RMS
- Ceramic body — can't burn
- Pure silver links
- Links welded to contacts
- Rated by semiconductor specialists



SF25X SERIES — ampklip SEMICONDUCTOR FUSES
DATA SHEET NUMBER PD-8.002

1B

SF25X10 to 30

SF25X40 to 800

SF25X Series, Data Sheet No. PD-8.002

Fuses are rated in RMS current. Rectifier circuit designs are often based on average current. During steady state operation the fuse must not be operated in excess of its maximum RMS current rating.

ELECTRICAL SPECIFICATIONS

SERIES	SF25X	UNITS
Maximum RMS voltage	250	V RMS
Maximum peak voltage	353	V
Maximum dc voltage (refer to Fig. 18)	210	V dc
Maximum arc voltage	410	V
Interrupting capacity	238,000	A Peak

THERMAL-MECHANICAL SPECIFICATIONS

Forced cooling current rating factor, 900 LFM	1.2	
Maximum ambient temperature	150	°C
Maximum deadweight axial loading	5	lbs

DEVICE RATINGS

PART NUMBER	NOMINAL RMS CURRENT RATING (A) ^①	FUSE RESISTANCE		MELTING I ² t ^② (A ² -sec)	CLEARING I ² t		MAX. TIGHTENING TORQUE (LB-FT)	WEIGHT (OZ)
		COLD ^③ (mΩ)	HOT ^④ (mΩ)		130V ^⑤ (A ² -sec)	250V ^⑥ (A ² -sec)		
SF25X10	10	23	34	7	16	19	—	0.9
SF25X15	15	11.5	17	19	34	60	—	0.9
SF25X20	20	7.7	11.5	38	70	120	—	0.9
SF25X25	25	5.7	8.5	60	140	180	—	0.9
SF25X30	30	4.3	6.5	100	180	240	—	0.9
SF25X40	40	2.8	4.4	200	350	500	7	2.0
SF25X50	50	2.0	3.5	290	480	800	7	2.0
SF25X60	60	1.7	3.0	400	680	1,150	7	2.0
SF25X70	70	1.0	1.7	550	1,000	1,800	7	6.2
SF25X80	80	0.87	1.5	740	1,300	2,200	7	6.2
SF25X100	100	0.68	1.15	1,000	2,000	3,300	7	6.2
SF25X150	150	0.45	0.77	2,500	5,000	7,200	7	6.2
SF25X200	200	0.34	0.53	4,000	8,000	12,000	7	6.2
SF25X250	250	0.26	0.45	6,500	13,000	22,000	17	11.0
SF25X300	300	0.22	0.37	10,000	20,000	32,000	17	11.0
SF25X350	350	0.20	0.35	12,500	24,000	39,000	17	11.0
SF25X400	400	0.17	0.30	17,000	35,000	55,000	17	11.0
SF25X500	500	0.14	0.24	30,000	47,000	90,000	17	11.0
SF25X600	600	0.11	0.175	40,000	60,000	120,000	17	11.0

① See Figures 5 and 6 for RMS current ratings vs. ambient temperature.

② ± 10% tolerance.

③ At maximum rating shown on Figures 5 and 6 @ T_A = 25°C.

④ Typical I²t values for normal circuit conditions. See maximum clearing I²t curves for values under specific operating conditions.

DIMENSIONS (See Drawing, Page 1)

PART NUMBER	A ^①		B ^①		C ^①		D ^①		E ^②		F ^②		G ^②		H ^②	
	IN.	MM.	IN.	MM.	IN.	MM.	IN.	MM.	IN.	MM.	IN.	MM.	IN.	MM.	IN.	MM.
SF25X10 to 30	2.000	50.8	2.438	61.9	0.609	15.5	—	—	—	—	—	—	—	—	—	—
SF25X40 to 60	3.188	80.9	2.488	63.0	1.562	39.6	0.812	20.6	0.125	3.2	0.719	18.3	0.344	8.7	0.406	10.3
SF25X70 to 200	3.125	79.5	2.375	60.3	1.625	41.3	1.218	30.9	0.188	4.8	1.000	25.4	0.344	8.7	0.406	10.3
SF25X250 to 600	3.844	97.5	2.781	70.7	1.988	50.5	1.531	38.8	0.250	6.3	1.000	25.4	0.406	10.3	0.488	11.9

① Tolerance is ± 0.062 inch (± 1.6mm)

② Tolerance is ± 0.016 inch (± 0.4mm)

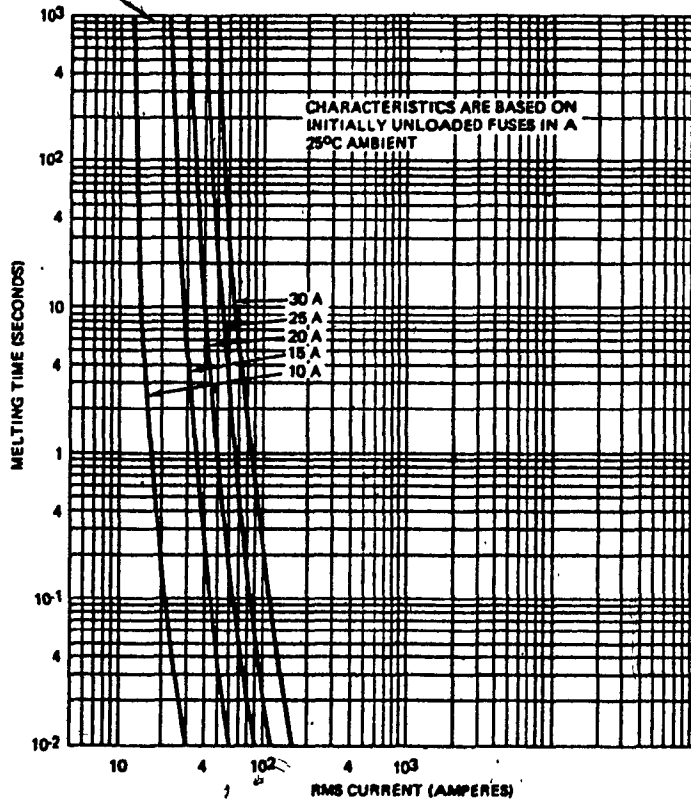


Fig. 1 - Melting Time Vs. Current - For Fuses Rated 10 to 30A

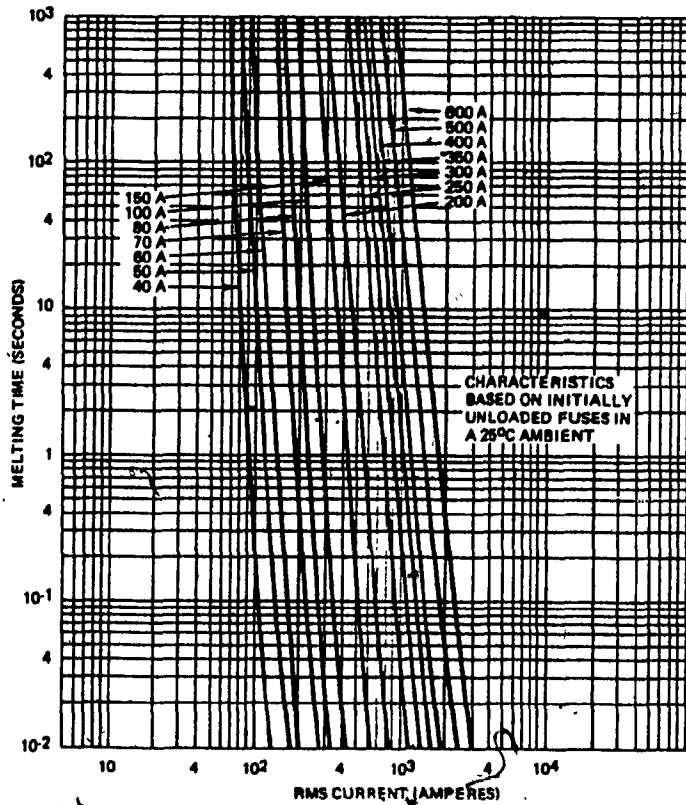


Fig. 2 - Melting Time Vs. Current - For Fuses Rated 40 to 600A

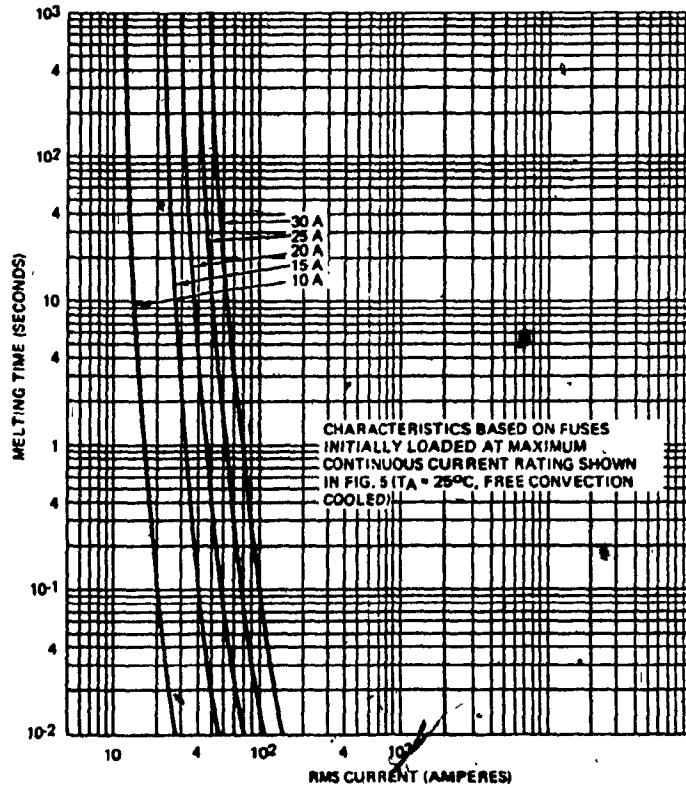
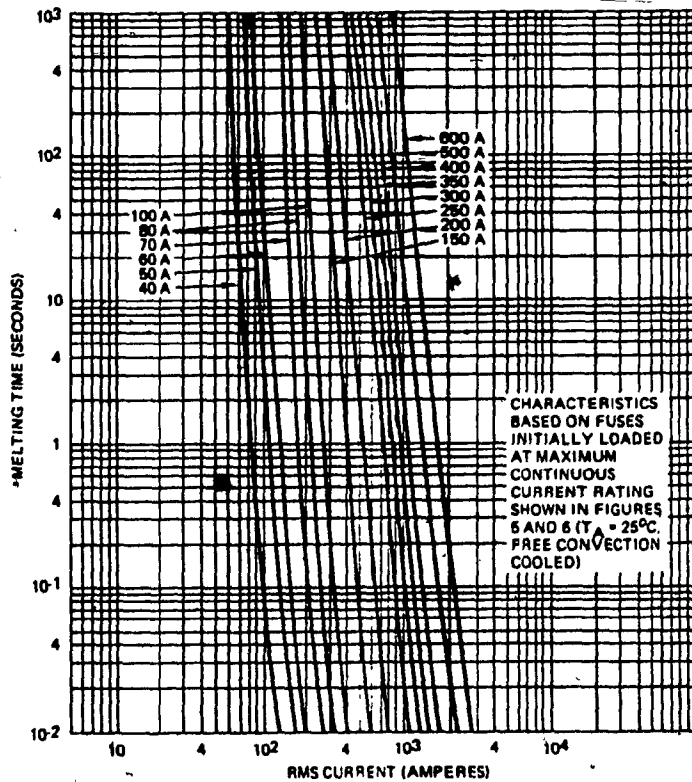


Fig. 3 - Pre-Loaded Melting Time Vs. Current - For Fuses Rated 10 to 30A



4B

Fig. 4 - Pre-Loaded Melting Time Vs. Current - For Fuses Rated 40 to 600A

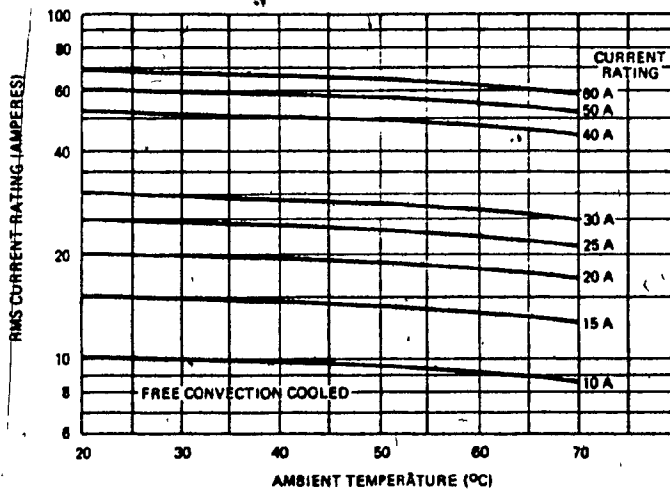


Fig. 5 - Maximum RMS Continuous Current Vs. Ambient Temperature - For Fuses Rated 10 to 60A

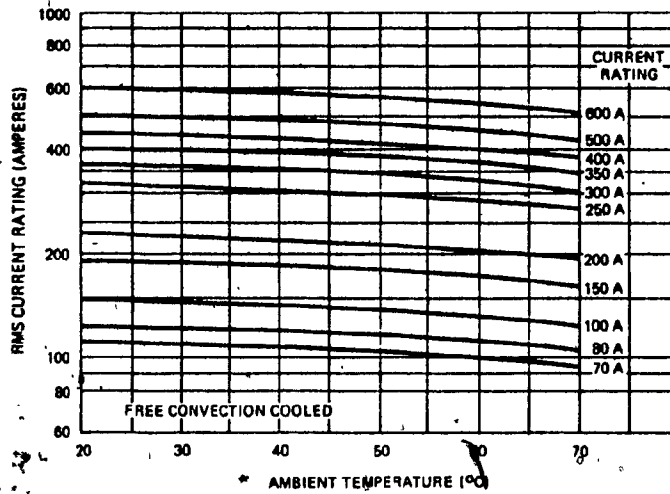


Fig. 6 - Maximum RMS Continuous Current Vs. Ambient Temperature - For Fuses Rated 70 to 600A

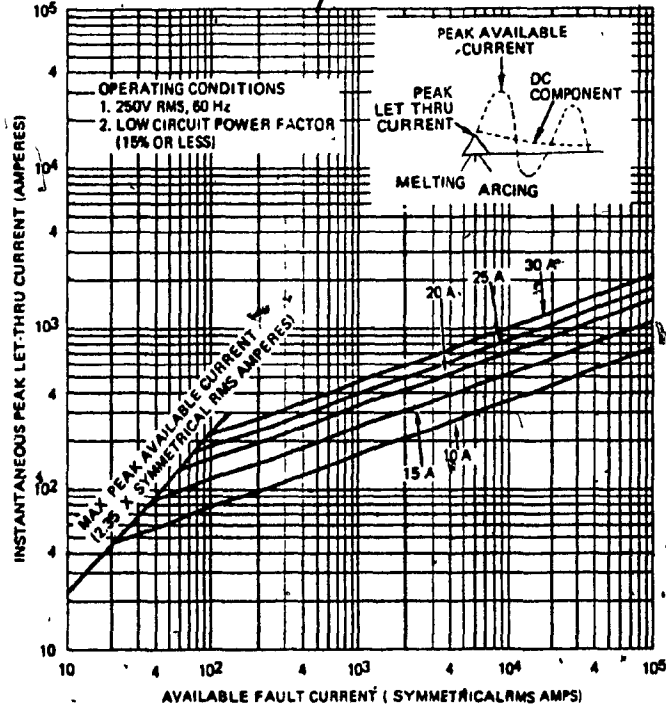


Fig. 7 - Peak Let-Through Current Vs. Fault Current - For Fuses Rated 10 to 30A

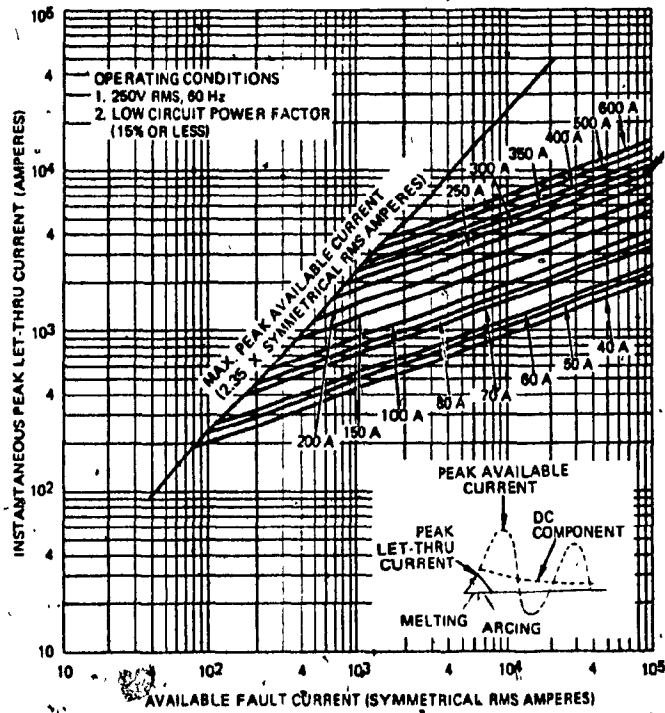


Fig. 8 - Peak Let-Through Current Vs. Fault Current - For Fuses Rated 40 to 600A

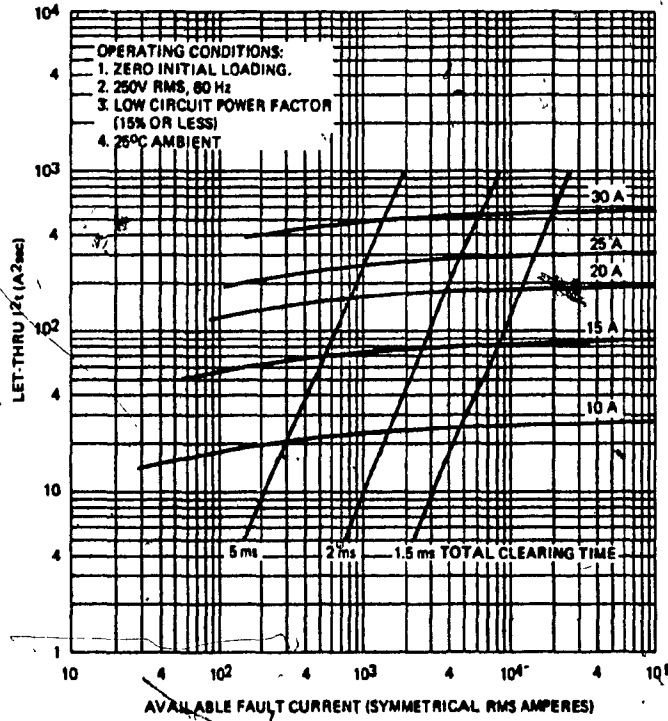


Fig. 9 - Maximum Clearing I^2t Characteristics - 250V Supply - For Fuses Rated 10 to 30A

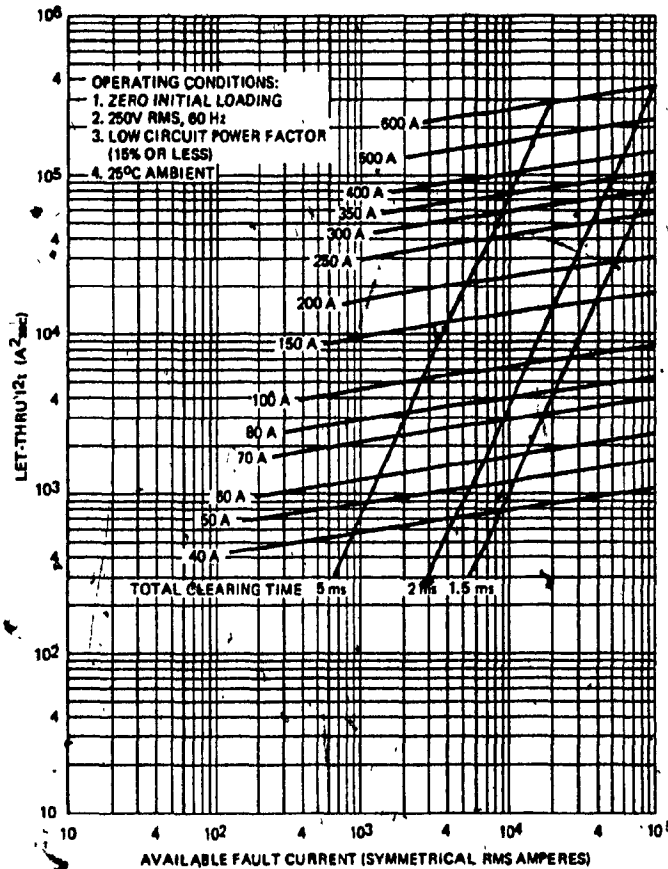


Fig. 10 - Maximum Clearing I^2t Characteristics - 250V Supply - For Fuses Rated 40 to 600A

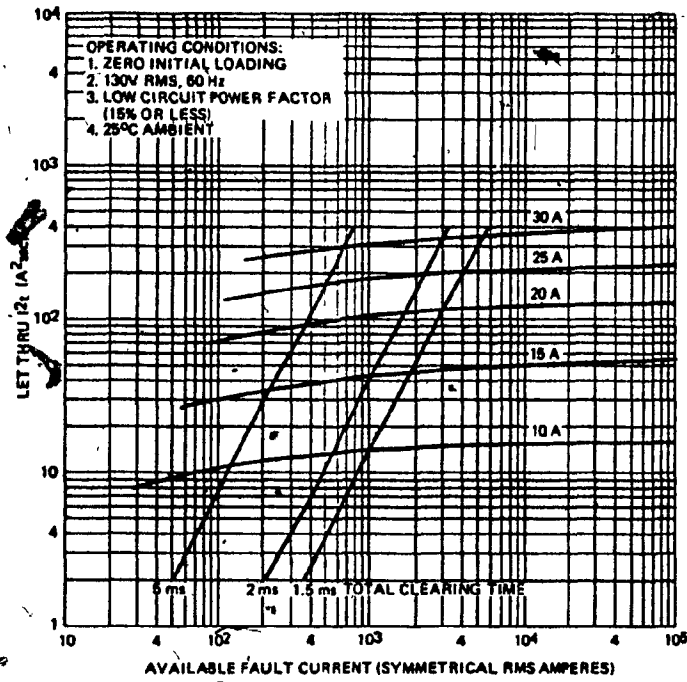
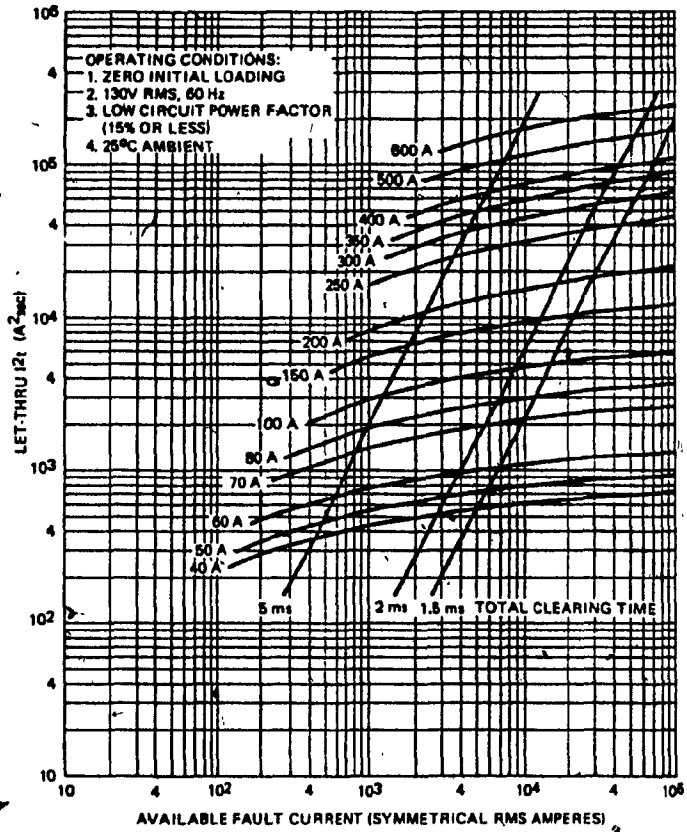


Fig. 11—Maximum Clearing I^2t Characteristics—130V Supply—For Fuses Rated 10 to 30A



8B

Fig. 12—Maximum Clearing I^2t Characteristics—130V Supply—For Fuses Rated 40 to 600A

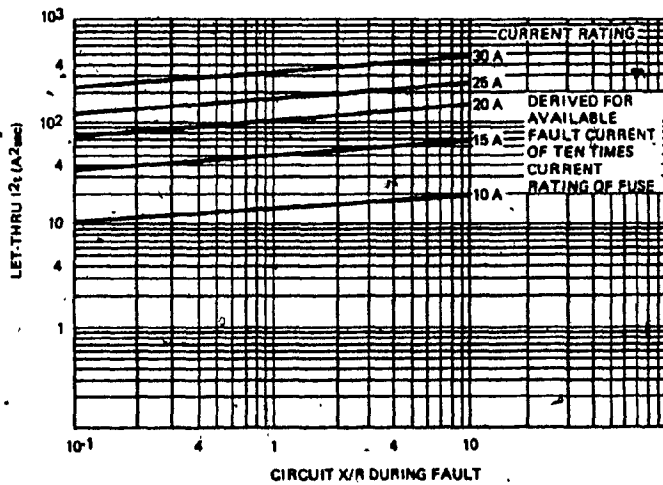


Fig. 13 - Clearing I^2t Characteristics Vs. Circuit X/R - For Fuses Rated 10 to 30A

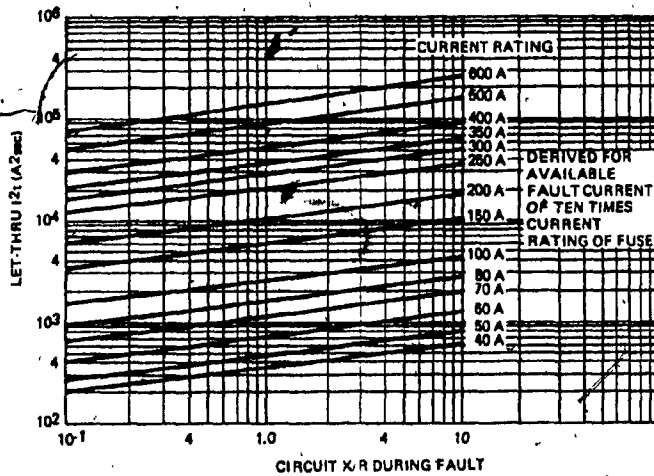


Fig. 14 - Clearing I^2t Characteristics Vs. Circuit X/R - For Fuses Rated 40 to 600A

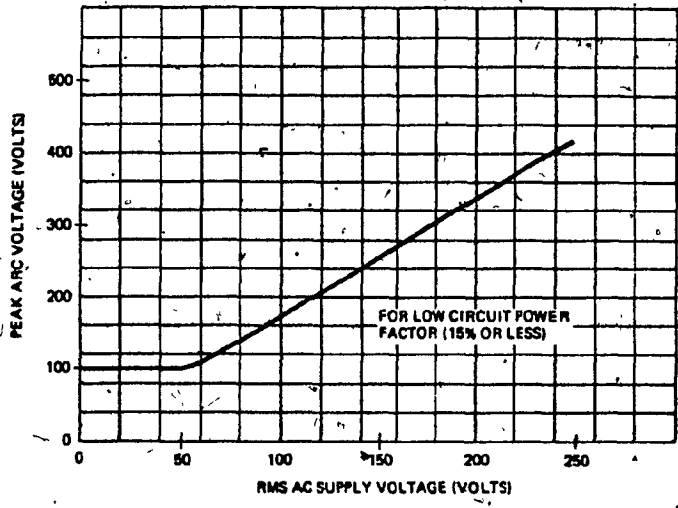


Fig. 15 - Maximum Arc Voltage Characteristic

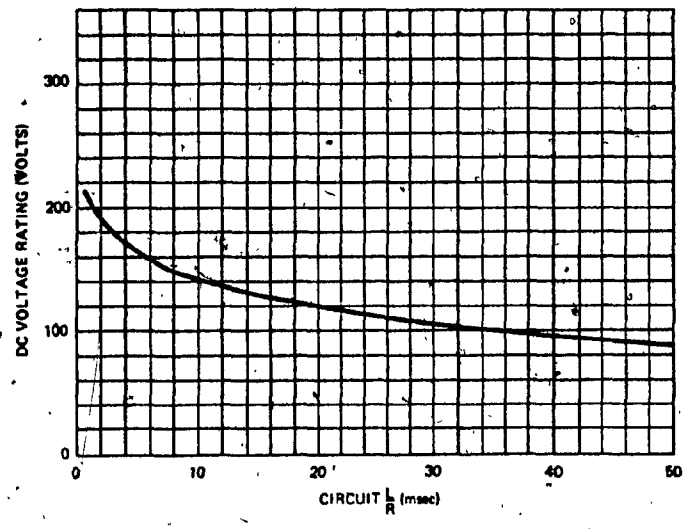


Fig. 16 - Maximum DC Voltage Rating Vs. Circuit L/R

MPS-U05 (SILICON) MPS-U06

NPN SILICON ANNULAR AMPLIFIER TRANSISTORS

... designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage -
 $V_{CE0} = 60 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc - MPS-U05}$
 $80 \text{ Vdc (Min) @ } I_C = 1.0 \text{ mAdc - MPS-U06}$
- High Power Dissipation - $P_D = 10 \text{ W @ } T_C = 25^\circ\text{C}$
- Complements to PNP MPS-U55 and MPS-U56

NPN SILICON AMPLIFIER TRANSISTORS



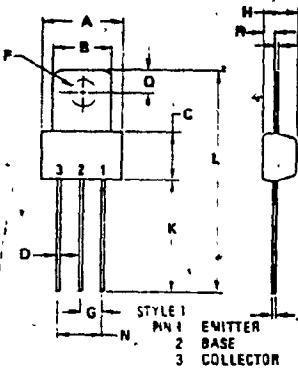
MAXIMUM RATINGS

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	V_{CE0}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	40		Vdc
Collector Current - Continuous	I_C	20		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	10	80	Watts mW/°C
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	10	80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA(1)}$	125	°C/W

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.14	8.53	0.320	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.98	0.53	0.038	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.006
M	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

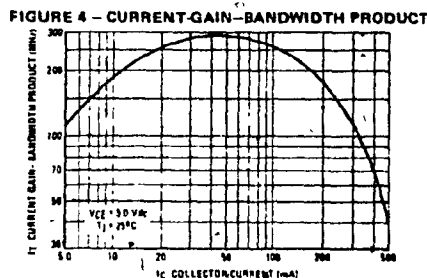
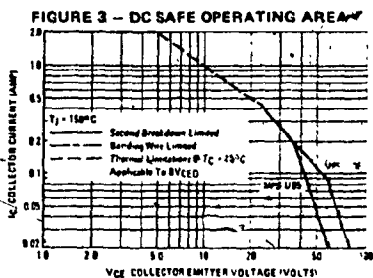
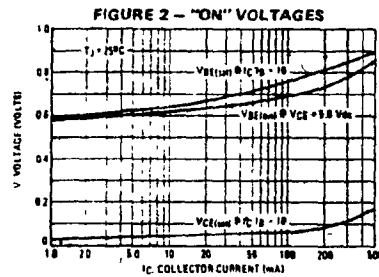
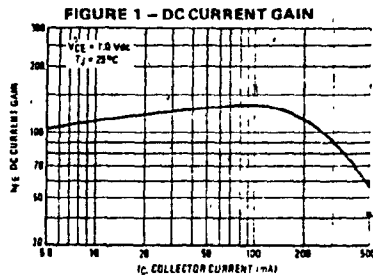
CASE 152-02

MPS-U05, MPS-U06 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I _C = 1.0 mA, I _B = 0)	BV _{CEO}	80	—	—	V _{dc}
Emitter-Base Breakdown Voltage (I _E = 100 μA, I _C = 0)	BVEBO	40	—	—	V _{dc}
Collector Cutoff Current (V _{CB} = 40 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0)	I _{CBO}	—	—	100 100	nA _{dc}
ON CHARACTERISTICS					
DC Current Gain (1) (I _C = 50 mA, V _{CE} = 1.0 Vdc) (I _C = 250 mA, V _{CE} = 1.0 Vdc) (I _C = 500 mA, V _{CE} = 1.0 Vdc)	h _{FE}	80 60 —	125 100 55	—	—
Collector-Emitter Saturation Voltage (1) (I _C = 250 mA, I _B = 10 mA) (I _C = 250 mA, I _B = 25 mA)	V _{CE(sat)}	—	0.18 0.1	0.4	V _{dc}
Base-Emitter On Voltage (1) (I _C = 250 mA, V _{CE} = 5.0 Vdc)	V _{BE(on)}	—	0.74	1.2	V _{dc}
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (1) (I _C = 200 mA, V _{CE} = 5.0 Vdc, f = 100 MHz)	f _T	50	170	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)	C _{ob}	—	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



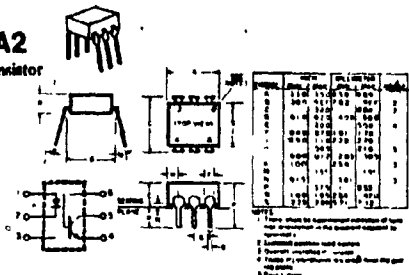
OPTOELECTRONICS



Photon Coupled Isolator H11A1-H11A2

Ga As Infrared Emitting Diode & NPN Silicon Photo-Transistor

The General Electric H11A1 and H11A2 are gallium arsenide infrared emitting diodes coupled with a silicon photo-transistor in a dual in-line package.



absolute maximum ratings: (25°C)

INFRARED EMITTING DIODE		
Power Dissipation	*100	milliwatts
Forward Current (Continuous)	60	milliamperes
Forward Current (Peak) (Pulse width 1 μsec 300 P Ps)	3	amperes
Reverse Voltage	3	volts

*Derate 1.33mW/°C above 25°C ambient

PHOTO-TRANSISTOR		
Power Dissipation	**150	milliwatts
V _{CEO}	30	volts
V _{CE0}	70	volts
V _{ECO}	7	volts
Collector Current (Continuous)	100	milliamperes

**Derate 2.0mW/°C above 25°C ambient

TOTAL DEVICE		
Storage Temperature	-55 to 150°C	
Operating Temperature	-55 to 100°C	
Lead Soldering Time (at 260°C)	10 seconds	
Surge Isolation Voltage (Input to Output)		
H11A1	2500V (peak)	1770V (RMS)
H11A2	1500V (peak)	1060V (RMS)
Steady-State Isolation Voltage (Input to Output)		
H11A1	1500V (peak)	1060V (RMS)
H11A2	950V (peak)	660V (RMS)

individual electrical characteristics (25°C)

INFRARED EMITTING DIODE	TYP.	MAX.	UNITS
Forward Voltage (I _F = 10 mA)	1.1	1.5	volts
Reverse Current (V _R = 3 V)	-	10	microamps
Capacitance (V = 0, f = 1 MHz)	50	-	picofarads

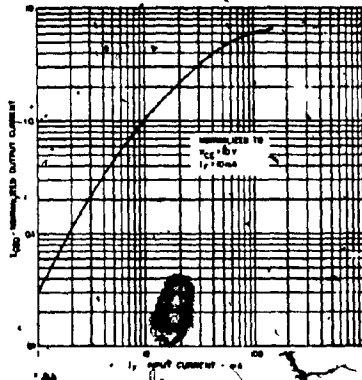
PHOTO-TRANSISTOR	MIN.	TYP.	MAX.	UNITS
Breakdown Voltage - V _{(BR)CEO} (I _B = 10mA, I _F = 0)	30	-	-	volts
Breakdown Voltage - V _{(BR)CBO} (I _C = 100mA, I _F = 0)	70	-	-	volts
Breakdown Voltage - V _{(BR)ECO} (I _F = 100μA, I _E = 0)	7	-	-	volts
Collector Dark Current - I _{C0} (V _{CE} = 10V, I _F = 0)	-	5	50	nanoamps
Capacitance (V _{CE} = 10V, f = 1MHz)	-	2	-	picofarads

coupled electrical characteristics (25°C)

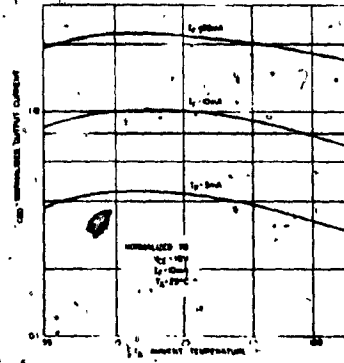
	MIN.	TYP.	MAX.	UNITS
DC Current Transfer Ratio (I _F = 10mA, V _{CE} = 10V)	50	-	-	%
Saturation Voltage - Collector to Emitter (I _F = 10mA, I _C = 0.5mA)	20	-	-	%
Isolation Resistance (Input to Output Voltage = 500V _{DC})	-	0.1	0.4	volts
Input to Output Capacitance (Input to Output Voltage = 0, f = 1MHz)	100	-	-	gigaohms
Switching Speeds:	-	-	2	picofarads
Rise/Fall Time (V _{CE} = 10V, I _{CE} = 2mA, R _L = 100Ω)	-	2	-	microseconds
Rise/Fall Time (V _{CE} = 10V, I _{CE} = 50μA, R _L = 100Ω)	-	300	-	nanoseconds

H11A1, H11A2

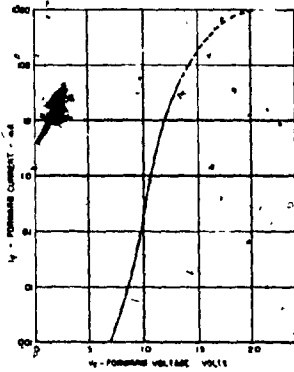
TYPICAL CHARACTERISTICS



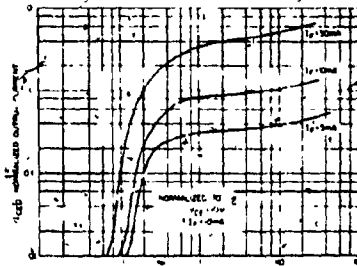
OUTPUT CURRENT VS INPUT CURRENT



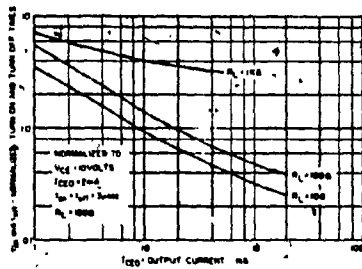
OUTPUT CURRENT VS TEMPERATURE



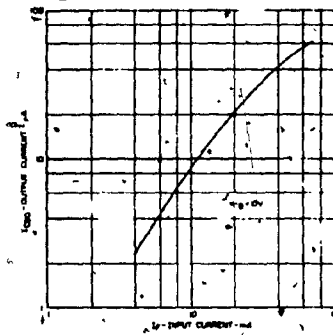
INPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS



SWITCHING TIMES VS OUTPUT CURRENT



OUTPUT CURRENT (I_{CBO}) VS INPUT CURRENT

APPENDIX III

COMPUTER PROGRAMME

and

FLOW CHART

PROGRAM INVERT(INPUT,OUTPUT)

ANALYSIS OF COMMUTATION CIRCUIT OF MODIFIED MCMURRAY
INVERTER CIRCUIT.

THIS PROGRAM CALCULATES THE INSTANTANEOUS VALUES OF
COMMUTATION CAPACITOR CURRENT AND VOLTAGE DURING ENTIRE
COMMUTATION PROCSS. IT ALSO CALCULATES THE TOTAL TIME FOR
CHARGING OF COMMUTATION CAPACITOR AND DISCHARGING OF EXCESS
CHARGE ON THE CAPACITOR DURING INVERTER STARTING AND THE
TOTAL COMMUTATION TIME FOR ENTIRE COMMUTATION PROCESS.

*****NOMENCLATURE*****

LC IS THE VALUE OF COMMUTATING INDUCTANCE IN MICRohenRIES.
LI IS THE VALUE OF DI/DT INDUCTANCE IN MICRohenRIES.
C IS THE VALUE OF COMMUTATING CAPCITANCE IN MICROFARADS.
R IS THE VALUE OF DAMPING RESISTANCE IN OHMS.
ED IS THE VALUE OF THE SUPPLY VOLTAGE IN VOLTS.
CIL IS THE VALUE OF MAXIMUM LOAD CURRENT TO BE COMMUTATED IN
AMPRES.
Q OF THE COMMUTATION INDUCTOR IS TAKEN AS 10.

DIMENSION TIME(S)
REAL LC,L,LI,XIST
READ *,LC,L,C,R
READ *,ED,CIL
K=1

L,RIC,RC,ALP1,ALP2,ALP3,W10,W20,W ARE CIRCUIT PARAMETERS.

L=LC*LI
RIC=SQRT(L/C)/10.
RC=SQRT(LC/C)/10.
ALP1=(R+RIC)/(2.*L)
ALP2=RIC/(2.*L)
ALP3=RC/(2.*L)
W10=1./SQRT(L*C)
W20=1./SQRT(LC*C)
E1=0.
T=0

STARTING CYCLE
INITIAL CONDITIONS AND PARAMETERS

GO TO(10,20,30,40,50),K
PRINT 11
FORMAT(1H1,30X,*, STARTING CYCLE *,//)
E1=0.
C11=0.
E=ED
W0=W10
ALP=ALP2
GO TO 60
PRINT 21

21 FORMAT(1H1,30X, 'RETURN OF EXCESS CHARGE ON CAPACITOR',//)

RETURN OF EXCESS CHARGE ON THE CAPACITOR
INITIAL CONDITIONS AND PARAMETERS

55 EI=EC1
ALP=ALP1
EC1=0.
GO TO 60

30 PRINT 31
31 FORMAT(1H1,30X, 'FIRST PORTION OF COMMUTATION CYCLE',//)

FIRST PORTION OF COMMUTATION CYCLE
INITIAL CONDITIONS AND PARAMETERS

75 E=0.
EI=-EC1
L=LC
W0=W20
ALP=ALP3
EC1=0.
GO TO 60

40 PRINT 41
41 FORMAT(1H1,30X, 'SECOND PORTION OF COMMUTATION CYCLE',//)

SECOND PORTION OF COMMUTATION CYCLE
INITIAL CONDITIONS AND PARAMETERS

85 E=ED
EI=EC1
CII=CIL
L=LC+LI
W0=W10
ALP=ALP2
EC1=0.
GO TO 60

50 PRINT 51
51 FORMAT(1H1,30X, 'THIRD PORTION OF COMMUTATION CYCLE',//)

THIRD PORTION OF COMMUTATION CYCLE
INITIAL CONDITIONS AND PARAMETERS

100 EI=EC1
CII=0.
ALP=ALP1
EC1=0.

CALCULATE W, PHI, CTC, (COMMUTATION CURRENT), EC (COMMUTATION
CAPACITOR VOLTAGE)

60 W=SQRT(W0**2.-ALP**2.)

PHI=ATAN(4/A_P)

PRINT 51

61 FORMAT(22X, 'TIME', 15X, 'CTC', 15X, 'EC', 15X, 'DIDT', 17X, 'DVDT',//)

70 CTC=((E-EI)/(W*L))*EXP(-ALP*TI)*SIN(W*TI)-CII*(W0/W)*EXP(-ALP*TI)
1*SIN(W*TI-2*PI)

EC=E-(E-EI)*(W0/W)*EXP(-ALP*TI)*SIN(W*TI-2*PI)/(W*L)

110

```
115      IEXP(-ALP*T)*SIN(W*T)
      DIOT=EXP(-ALP*T)*((E-ET)/(W*LI)+(W*COS(W*T)-ALP*SIN(W*T))-(CII*NO/W
110      LI*(ALP*SIN(W*T)+PHI)+W*COS(W*T)+PHI))
      DVDT=EXP(-ALP*T)*((E-ET)*(W/W)+(ALP*SIN(W*T)+PHI)-W*COS(W*T)+PH
111      II)-(CII/(W*C)*(W*COS(W*T)-ALP*SIN(W*T)))

120      CHECK FOR FINAL CONDITION
      GO TO(110,140,130,110,140),K

125      110 IF(CIC) 200,100,100
      130 IF(EC)100,100,400
      140 IF(CIC) 100,100,200
      400 IF(CIC-CIL) 200,200,100,0
      100 PRINT 71,T,CIC,EC,DIOT,DVDT
      71  FORMAT(20X,F5.2,10X,F10.5,10X,F10.5,10X,F10.5,/)

130      EC=EC
      T=T+.5
      GO TO 70
      200 TIME(K)=T
      K=K+1

135      IF(K,LE,51 GO TO 80

140      CALCULATE TOTAL TIME FOR CHARGING OF COMMUTATION CAPACITOR
      AND DISCHARGE OF EXCESS CHARGE ON CAPACITOR DURING INVERTER
      STARTING (KTST) AND TOTAL COMMUTATION TIME (TCT).

      KTST=TIME(1)+TIME(2)
      TCT=TIME(3)+TIME(4)+TIME(5)
      PRINT 201,KTST
      PRINT 202,TCT

145      201 FORMAT(30X,'CHARGING TIME OF CAPACITOR = ',F6.2,' MICRO SECONDS',/)
      202 FORMAT(30X,'TOTAL COMMUTATION TIME = ',F6.2,' MICROSECONDS',/)
      300 STOP
      END
```

ANALYSIS OF COMMUTATION CIRCUIT OF MODIFIED McMURRAY INVERTER

