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Electrical Characterization of Fluorinated And Oxynitrided Gate-Oxides

Tan Khai Nguyen

A Thesis

in

The Department

of

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Presented in Partial Fulfillment of The Requirements
For the Degree of Doctor of Philosophy at
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ABSTRACT

Electrical Characterization of Fluorinated And Oxynitrided Gate-Oxides

Tan Khai Nguyen, Ph.D.
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Many novel gate oxidation processes have been developed to meet the ongoing quest for thinner and higher- quality gate dielectric layers. Among these processes, fluorination and nitridation methods have emerged as promising techniques for ultra-large scale integrated circuit (ULSI) technology. Reported data in the literature is presented to show the advantages of these two processes. There are various ways to fabricate fluorinated and oxynitrided SiO_2 films. In this work, fluorination is done by shallow F-ion implantation through polysilicon gate, followed by thermal diffusion into the underlying gate oxide. Oxynitridation is done by a heat treatment in N_2O gas. The samples are fabricated as lot-splits of the Mitel 1.5 μm process.

As background, the mechanisms of generation of oxide trapped charges during hot carrier injection stress are discussed. In this light, the quality of fluorinated and oxynitrided gate-oxides are discussed, in comparison with control oxides. The dissertation also discusses methods used to characterize the electrical properties of oxides. According to the framework of DiMaria *et al*, gate voltage changes during Fowler-Nordheim stress are sensitive only to trapped charges located outside a tunneling distance from the cathode interface. The dissertation discusses how DiMaria's framework can be applied to obtain

information about trapped-charge generated in the bulk oxide and trapped charges generated at or near the SiO_2 interfaces outside or within a tunneling distance from the cathode interface. This technique will be used to do electrical characterization on gate oxides treated by fluorination or oxynitridation.

In this work, oxynitrides show convincingly better performance than the fluorinated and the conventional thermally-grown oxides under positive gate bias Fowler-Nordheim tunnelling injection stress. However, under negative gate bias Fowler-Nordheim tunnelling injection stress, only the lower-temperature oxynitrides show advantages, not the higher-temperature oxynitrides. Channel hot electron injection stress also confirms the feasibility of incorporating oxynitridation into sub-micrometer processes. The application of the developed electrical characterization technique helps to reveal the complex behaviors of charge components induced in gate oxides under Fowler-Nordheim stress.

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CHAPTER 1

INTRODUCTION

1.1 Fluorinated and Oxynitrided Thin Gate Dielectrics

Fabrication technologies for intergrated circuits of the future will demand very thin gate dielectric layers. Electrically-induced degradation effects in thin gate oxides need to be carefully understood.

Many novel processes have been developed in the quest for high-quality, thinner, lower-temperature-processed gate oxides. Methods used to grow oxides by plasma include plasma-enhanced chemical vapor deposition [1], remote plasma-enhanced chemical vapor deposition [2-3], excited plasma oxidation [4-5], and electron cyclotron resonance [6]. Thin gate oxides can be also created by aqueous electrochemical processes such as anodic oxidation [7]. Alternatively, thermal oxidation processes can be modified to include fluorination [8-14], or oxynitridation [15-16].

Among these novel and other processes, fluorination [8-14] and oxynitridation are particularly interesting techniques [15-18]. For fluorination, many aspects of the properties of the resulting dielectric layers have been studied. For example, such oxides have been found to be more resistant to ionizing radiation [9, 13-14, 19-22], Fowler-Nordheim (FN) tunnelling injection stress [8-10,14, 23-26], and channel hot electron stress [8, 11-14,

27-29]. Fluorination has also been shown to increase oxide growth rate, and provides a more relaxed oxide structure [30]. For oxynitrided gate dielectrics, several studies [16-18, 31-34] have specifically addressed the electrical and physical properties of the films. These studies all report that oxynitrides have better performance than thermal oxide in such aspects as channel hot carrier injection [17, 35-39], radiation impact-ionization [31], charge breakdown [37,40], Fowler-Nordheim stress [15-17, 31, 38, 40], and deep level transient spectroscopy [41].

While the techniques are clearly promising, there are many aspects of these techniques which remain not fully characterized or understood. This work aims to extend the understanding of these techniques by an enhanced electrical characterization strategy, with the goal of forming a more comprehensive view of the effects of these two techniques.

1.2 Overview of This Document

Critical measures of the reliability of fabricated oxides are the densities of trapped charges generated in the bulk oxide and at the interfaces during electrical stress. Failure criteria are commonly defined as the point at which a device can no longer perform its intended function, whether due to catastrophic breakdown or due to gradual degradation [42]. The study of defect generation in MOS oxides during electrical stress is very important.

Chapter 2 begins with discussion of oxide defects, and of the mechanisms of impact ionization and electron trap generation. These two types of traps are believed to be

generated under electrical stresses, usually from the Fowler-Nordheim tunnelling of hot electrons. The theoretical framework of DiMaria [43-44] is then applied to establish a method for measurement and study of charge components in MOS oxides. This tool allows deeper systematic electrical characterization of the special-process films considered in this work.

Also in Chapter 2, the prior literature on fluorinated and oxynitrided oxides is discussed. For fluorinated oxides, while there exist several oxide fluorination processes, the most practical process appears to be fluorination by ion implantation of F ions. This is the fluorination method studied in this work. Oxynitridation can be done from a variety of gaseous sources and processes. In this work, N_2O-oxynitridation is mainly studied.

After the above (more general), discussions of electrical characterization and of the two techniques, Chapter 3 maps the experimental and characterization plan for this work. The anticipated importance is also discussed in this chapter. The measurement set-up and procedures are also outlined.

Chapter 4 begins with detailed descriptions of the fluorinated and oxynitrided sample preparation lot splits. Then, because any variation in a complete process can be complex and subtle, an in-situ pilot study is done to confirm previously reported consequences of fluorination on Mitel's 1.5μm process. The electrical characterization techniques employed are constant-voltage Fowler-Nordheim hot carrier injection stress and constant-current Fowler-Nordheim hot carrier injection (CCFN) stress. Standard Capacitance-Voltage (C-V) measurements are also applied, to measure typical value of oxides such as flat-band voltage, interface state densities, oxide fixed charge, and threshold voltage.

An extensive study of fluorination is conducted in Chapter 5. In this section, both positive and negative gate biases of CCFN stresses are used. Many analyses are done to study the induced charges generated in the fluorinated oxides. Based on these analyses, conclusions about induced charge components are suggested, such as charge locations, charge trapping rates, the rate of change of charge trapping rate. Comparisons of the quality of the fluorinated and the control oxides are also made based on the obtained results.

Chapter 6 is devoted to oxynitridation. Following Chapter 5, positive and negative gate biases of CCFN are applied to the oxynitrides. Many analyses are done to study the induced charges generated in the oxynitrided oxides. Based on these analyses, conclusions about induced charge components are suggested such as charge locations, charge trapping rates, the rate of change of charge trapping rate. Comparisons of the quality of the oxynitrides and the control oxide are also made based on the obtained results.

Chapter 7 is a summary and comparison of the behavior of the fluorinated, oxynitrided and control cases. Numerical details in the obtained data are used to do comparisons between the fluorinated and the oxynitrided cases, which are both shown to be better oxides than the control case. The comparisons display advantages and disadvantages of the two processes. Overall, it turns out that the oxynitrides are "better" than the fluorinated and the control oxides. The work displays a relatively comprehensive and comparative view of the many effects of the fluorination and oxynitridation techniques.

Chapter 8 shows experimental data of channel hot electron injection stress on oxynitrides. Discussions suggest the suitability of oxynitridation for incorporation into sub-micrometer processes.

Chapter 9 summarizes the thesis and contributions, and suggests future work on the topic.

1.3 Industrial Relevance.

The samples under investigation in this project were fabricated in the 1.5 μm Mitel standard process. As well as a basic study of the effects of fluorine and nitrogen in thin gate oxides, the data obtained from the samples investigated can show whether these two oxide treatment techniques can be incorporated into submicron processes at companies such as Mitel Corporation.

1.4 Overall Goals of The Project

- Study effects of fluorine incorporated into gate oxide.
- Study effects of nitrogen incorporated into gate oxide.
- Achieve a more comprehensive understanding of the overall effects of these two techniques on the electrical behaviors of thin gate oxides.
- Compare advantages and disadvantages of these two techniques to see which technique can be employed in the future in Mitel Corporation fabrication processes.

● Formalize a characterization technique based on a variation of the DiMaria model, to allow detailed identification of the charge components in gate oxides, using positive gate bias and negative gate bias electrical stress tests.

CHAPTER 2

BACKGROUND

This chapter covers background material on two important bodies of knowledge:

- Oxide defects and electrical reliability characterization.
- Fluorinated and oxynitrided gate oxides.

2.1 Background On Oxide Defects And Electrical Reliability Characterization

2.1.1 Oxide Charges

Fig. 2.1 shows a model of oxide charges and defects caused by electrical stress proposed by Deal [45]. Symbols "+" and "-" show the sign of the charges as positive and negative respectively. The oxide charges and defects will be discussed from top to bottom (according to the Fig. 2.1).

First, mobile ionic charges are most commonly caused by the presence of ionized alkali metal atoms such as sodium or potassium. They are located either at the metal/SiO_2 interface where they originally, enter the oxide layer, or at the Si/SiO_2 interface, where

they have drifted under an applied field. The charge can be detected by the use of Bias Temperature Stress (BTS). However, these charges are not, commonly and presently, a problem due to the extreme cleanliness enforced on modern fabrication process.

Oxide trapped charges occur because of the existence of defects in the oxide bulk. They are often located near the interfaces. Oxide traps become charged when charges are injected (by electrical stress) through the oxide. They can also be generated by ion-implantation or ionizing radiation. The oxide trapped charges can be either positive or negative.

Oxide fixed charges, Q_f, are thought to be predominantly positive and exist approximately within 50Å of the interface. The oxide in the region near the Si/SiO_2 interface may also be a suboxide, where the chemical symbol is SiO_x, where $1<x<2$. The term "fixed charge" is given, because such charges are immobile under an applied electric field and do not exchange charge with silicon when the gate bias is varied. Since they are predominantly positive, the threshold voltage (V_{th}) is shifted in the negative direction under the effect of this type of charge. Since oxide fixed charge is caused by the fabrication process, and the sign of this type of charge is positive, then in the as-grown gate oxide the High Frequency Capacitance-Voltage (HFCV) curve will be shifted to the left. As it is named, the oxide fixed charge is fixed, therefore during an electrical stress, we expect the value of Q_f to remain constant.

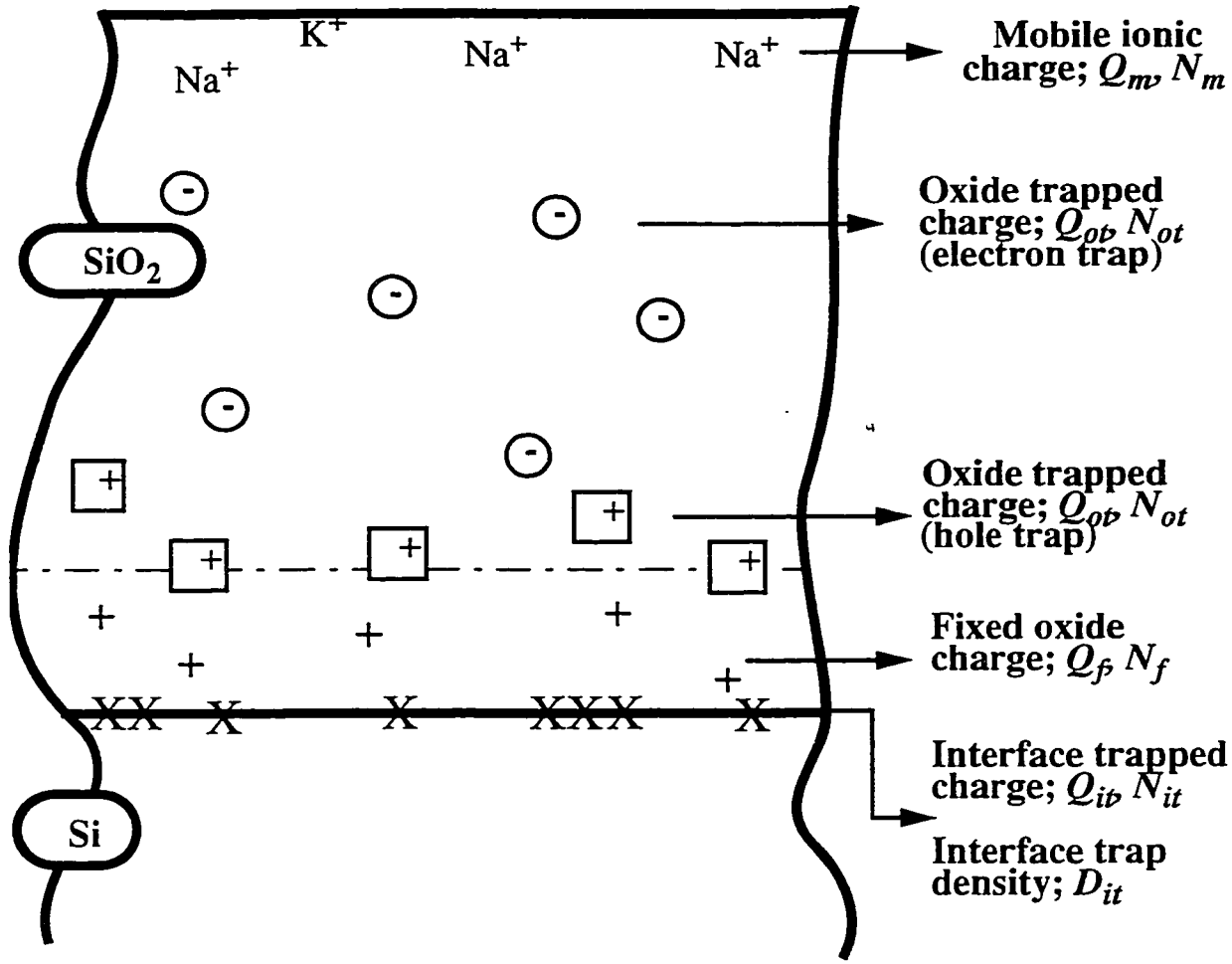


Fig. 2.1 - Oxide charges and defects [45].

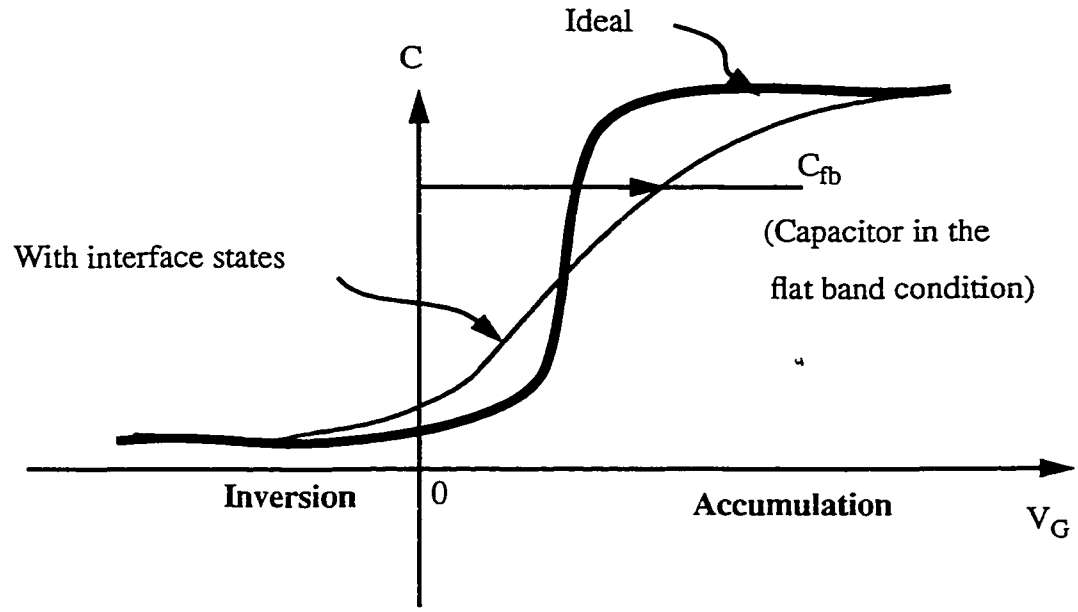
Interface trapped charges occur because of the existence of interface traps within about 10 Å of the Si/SiO_2 interface, which are energy levels distributed throughout the bandgap of the semiconductor at the Si/SiO_2 interface. The reason for these extra energy states is thought to be the abrupt termination of the periodic semiconductor crystal at the interface, which allows electronic energy levels to exist within the forbidden bandgap of silicon. These traps become charged by exchange of electrons or holes with the silicon when the gate bias is varied [45].

There are two types of interface traps: donor interface traps and acceptor interface traps. Donor interface traps are positive when empty, and neutral when full. Acceptor interface traps are negative when full, and neutral when empty. The effects of interface states are quite different from the effects of other oxide charge types. Charging and discharging in the interface states cause distortion (usually smear-out) in the HFCV curve. Fig. 2.2 illustrates this phenomenon.

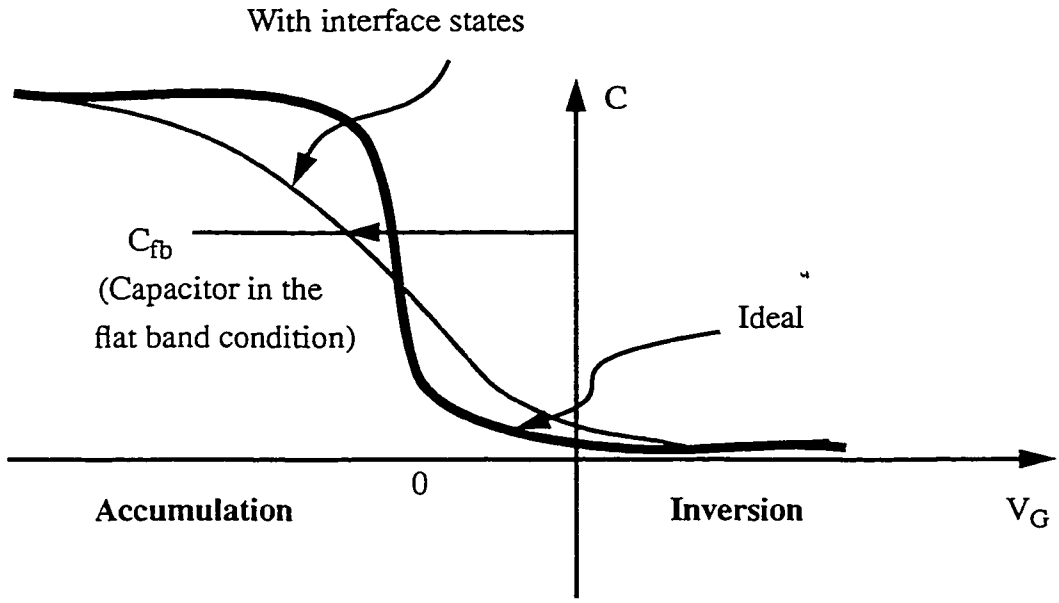
Theoretically, the distribution of the density of interface states, D_{it}, at an energy level is a summation of both donor and acceptor states:

$$D_{it}(\zeta_s) = D_{it}^{d}(\zeta_s) + D_{it}^{a}(\zeta_s) \tag{2.1}$$

Appendix A.2 contains the derivations associated with above equation. However, in practice it is quite impossible to distinguish which portion of D_{it} belongs to the donor or the acceptor types. According to Ref. 46, Wagner and Berglund showed a method to calculate the *total* interface state density by the combination of high and low frequency C-V curves (see Appendix A.5). From then on, Wagner and Berglund's method [46] became the most used method to extract the interface state density vs. silicon band gap energy.



(a) Typical Capacitance-Voltage curve of a MOS capacitor on n-type silicon.



(b) Typical Capacitance-Voltage curve of a MOS capacitor on p-type silicon.

Fig. 2.2 - High Frequency C-V characteristic curves of MOS capacitors showing the effect of interface states.

2.1.2 Theoretical Background of Electrical Measurements

2.1.2.1 Mechanism of Charge Trap Creation in The Bulk Oxide

Fig. 2.3 illustrates the model set up by DiMaria, Arnold and Cartier [43-44], to explain the mechanisms of how oxide traps are generated under positive gate bias. The mechanisms are compared in the schematic energy-band diagrams in Figs. 2.3a and 2.3b.

Trap creation (Fig. 2.3(a)), occurs for electrons possessing energies greater than 2eV. This model relates to the existence of hydrogen at the interfaces of SiO_2 [47-52]. In this mechanism, it is believed that hot electrons release hydrogen atoms from defect sites near the anode/oxide interface. This mobile species can then move to the cathode/oxide interface where it produces interface states and a distribution of electron traps. This process is thermally activated [43-44, 52], not dependent on oxide thickness (for films over 100Å) [43-44], and increases moderately with average fields above 1.5MV/cm and is measurable after the injection of $1x10^{-3}$ C/cm^2 on poly-Si-gate structures [43-44].

Fig. 2.3(b) describes how degradation can be caused by the impact ionization process. In this mechanism, mobile holes produced in the bulk oxide closer to the anode move under the applied field to the cathode/oxide interface, where some are trapped in as-fabricated energetically-deep sites (believed to be due to oxygen vacancies) [43-44]. Some of the injected electrons from the cathode combine with these trapped holes producing interface states and traps near the cathode. This process is weakly dependent on lattice temperature, has a strong oxide thickness dependence up to 500Å, occurs only when the fields exceed 7 MV/cm, and is measurable at injected fluences as low as $1x10^{-6}$ C/cm^2 [43-44].

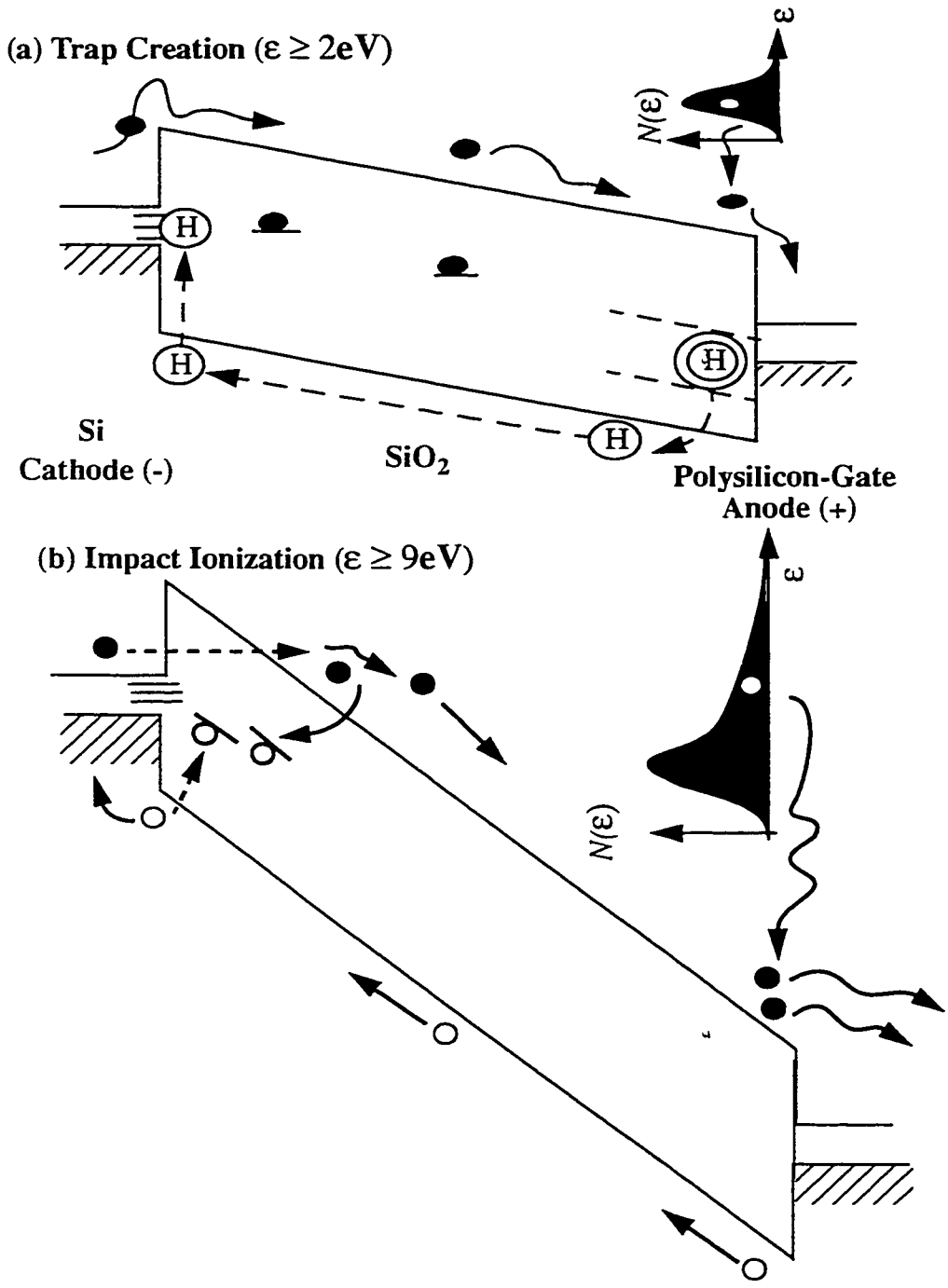


Fig. 2.3 - Schematic energy-band diagram showing for positive gate bias: (a) trap creation near the cathode caused by mobile hydrogen release from H-decorated sites near the anode, and (b) defect generation near the cathode caused by free electron/ trapped hole recombination where holes were generated in the oxide bulk by impact ionization [43-44].

Similarly to Figs. 2.3, in Fig.2.4 (a), under negative gate bias, the hot electrons release hydrogen atoms from defect sites near the anode/oxide interface. These mobile species then travel to the opposite interface and help to create interface states and a distribution of electron traps [43]. In Fig. 2.4(b), due to impact-ionization, mobile holes are produced in the bulk oxide close to the anode. These mobile species, then drift to the cathode/ oxide interface, where some are trapped in as-fabricated energetically-deep sites. Some of the injected electrons from the cathode combine with these trapped holes producing interface states and traps near the cathode [43].

Interfacial defect generation will occur at both interfaces of the bulk oxide. When the thickness of oxide is high (>130Å), the most-discussed problem is the interfacial states at the Si/SiO_2 interface. However, when the thickness of the gate oxide is smaller (<40Å) then the defects at both interfaces become important. By introducing these mechanisms, DiMaria [43] successfully explained the existence of the hole trapping, and the characteristic curve of trapped charges vs. injected fluence. Fluence is defined as injected current density multiplied by stressing time, or in cases where the current density varies, it is $\int_o^t j(\tau))d\tau$.

Also based on his model, DiMaria pinpointed the effect of hydrogen [43] at the interfaces of gate oxides. Thus the model suggests that replacing the Si-H chemical bond by some other species having higher-energy bonds could be expected to improve the reliability of gate oxides during hot carrier injection.

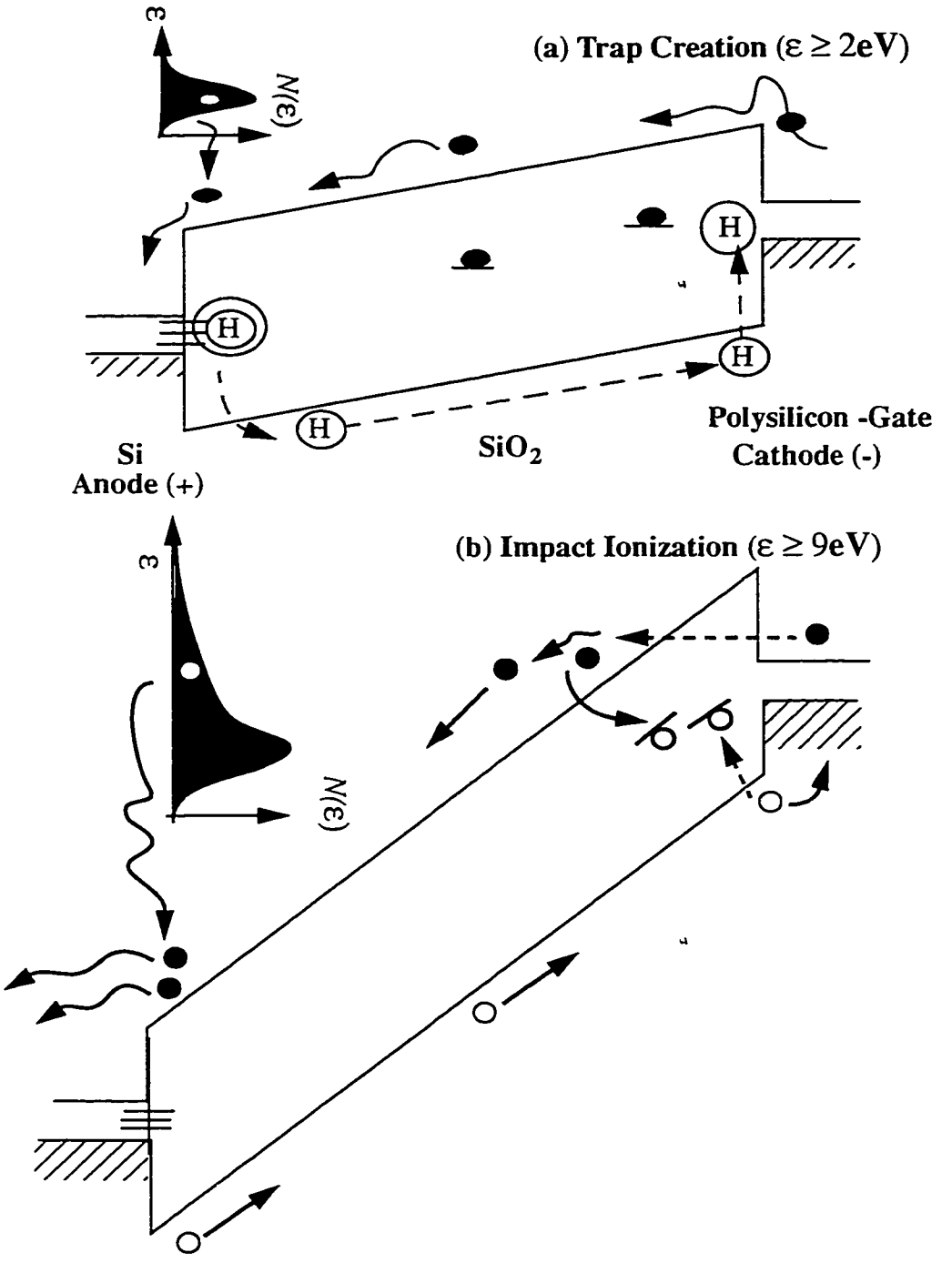


Fig. 2.4 - Schematic energy-band diagram showing for negative gate bias (a) trap creation near the anode caused by mobile hydrogen release from H-decorated sites near the anode, and (b) defect generation near the cathode caused by free electron/ trapped hole recombination where holes were generated in the oxide bulk by impact ionization.

2.1.2.2 The Sensitivity of Gate Voltage to Oxide Trapped Charges

Flatband voltages are sensitive to all charged defects including the ones located at the interface of Si/SiO_2. Because of this, the parameter of flatband voltage shift, ΔV_{fb}, can give the experimentalist only an overall result. Therefore, in order to study the components of charge in the bulk oxide, researchers must have ways to isolate the effects of charges at different locations in the oxide.

DiMaria [53] derived the following two equations:

$$\Delta V_g^{-} = \frac{1}{\varepsilon_{ox}}(L-\bar{x})Q \tag{2.2}$$

$$\Delta V_g^{+} = -\frac{1}{\varepsilon_{ox}}\bar{x}Q \tag{2.3}$$

Eq. 2.2 is for negative gate bias, while Eq. 2.3 is for positive gate bias, where L is oxide thickness, Q is trapped charge density, $\bar{x}$ is the centroid of charge, and V_g is the gate voltage which is required to maintain a constant current during a constant current Fowler-Nordheim stress. In these two equations, the metal-oxide interface is used as the origin of the coordinate x. Thus, for the gate voltage, according to DiMaria [43-44], Eqs. 2.2-2.3 can be interpreted as: the gate voltage is the most sensitive to charge trapping outside a tunneling distance away from the injecting cathode interface. The tunneling distance depends on the applied field. However, this distance never exceeds 50Å [43, 53-54]. This value is consistent with the upper bound of 50Å for the centroid measured using I-V charge-locating techniques [53-54]. Discussion of main possibilities associated with the biases is presented later in Section 3.1.

2.1.2.3 Constant-Voltage Fowler-Nordheim Stress, Also Called *j-t* Technique

The term "*j-t* technique" was first mentioned by DiMaria [44]. In this technique, a constant voltage (high enough to cause the Fowler-Nordheim tunneling phenomenon) is applied to the MOS capacitor, and the gate current is monitored. For an ideal MOS structure, the measured current would be constant with time. However, the change in gate oxide charge densities, due to the voltage and current flow, changes the characteristics of the original MOS structure and as a result the current may change. For example, when a positive voltage is applied on the gate, the creation of positive charges in the bulk oxide can increase the gate current, whereas the creation of electron trapped charges can reduce the current.

The Fowler-Nordheim current density relation with oxide field is (in Eq. 2.4),

$$j = AE^2 e^{-\frac{B}{E}} \tag{2.4}$$

where j is the current density, E is the field near the cathode, A (in unit of A/MV^2) is a constant, characteristic of a specific fabrication process, and B (in unit of MV/cm) is another constant, defined below, related to the energy barrier of silicon. One can derive the number of trapped charges generated in the bulk oxide outside of a tunneling distance from the cathode interface [43]. The number of traps generated in the bulk oxide during an electrical stress (after a time t) is (see Appendix A.1 for the derivation):

$$N(t) \equiv \frac{\varepsilon_{ox}(E_{ox}^{ave})^2 \ln\left(\frac{J(t)}{J(0)}\right)}{qB} \tag{2.5}$$

where B is a constant equal to:

$$B = \frac{4(2m_e^*)^{\frac{1}{2}}(\phi_b)^{\frac{3}{2}}}{3hq} \tag{2.6}$$

where h is Planck's constant divided by 2π, m_e^* is the effective mass of a tunneling electron (usually taken as 0.5 times the mass of a free electron), and ϕ_b is the cathodic energy barrier height (3.1eV for the Si/SiO_2 interface). Thus based on two equations, Eq. 2.5 & Eq. 2.6, one can calculate the charge defects generated during a constant voltage Fowler-Nordheim hot carrier injection stress. Eq. 2.5 is the main equation of the so-called *j-t* technique.

2.1.2.4 Constant-Current Fowler-Nordheim Stress

Similar to the *j-t* technique is the constant-current Fowler-Nordheim (CCFN) hot carrier injection stress. This method was used before the *j-t* technique was developed. It shares the same principle, that the defects generated in gate oxides are caused by the Fowler-Nordheim tunneling phenomenon. The electrical stress is applied as a constant current, such that the associated electric field is high enough to cause Fowler-Nordheim tunneling. During the electrical stress, the gate voltage is monitored. As trapped charges are generated in the oxide, the voltage at the gate must change to maintain a constant current. Thus the shift of the gate voltage will contain information about the trapped charges generated during constant current Fowler-Nordheim stress. Of course, the gate voltage shift, ΔV_g, is only sensitive to trapped charge farther than a tunneling distance away from the injecting cathodic interface [43, 55].

Eq. 2.7 is the main equation used to calculate the charge defects under a constant current Fowler-Nordheim stress. The trapped charge can be calculated as (see Appendix A.1):

$$\Delta V_g = \frac{\Delta QL}{\varepsilon_{ox}} \qquad (2.7)$$

2.1.3 Channel Hot Electron Injection Stress

Whereas the above techniques are used to characterize simple MOS capacitors, the impact of dielectric degradation on MOSFET function can be more directly evaluated by the technique of applying channel hot carrier injection stress. In this case the mechanism of degradation is: when electrons gain high enough energy and move to the drain under applied electric field, these high energy electrons will cause impact ionization at the drain region. The impact ionization then can be monitored by the substrate current, I_{sub} (see Fig. 2.5).

The degradations in device performance (threshold voltage shifts, (ΔV_{th}), and percentage reduction of transconductance, ($\Delta g_m(\%)$), resulting from hot carrier injection) are strongly related to the results of hot carrier impact ionization which induce substrate current [56-58]. Hu *et al* [58] and Takeda *et al* [59] suggest that by monitoring the substrate current, (I_{sub}), ΔV_{th}, and $\Delta g_m(\%)$ can be indicators of device lifetime or of process reliability.

The device lifetime, τ, is defined as the time for a certain threshold voltage shift, ΔV_{th}, or a certain reduction in transconductance, $-\Delta g_m/g_m(0)$, usually 50 mV or 10%,

respectively. The degradation in device may be caused by impact ionization which can be monitored via substrate current. Then the empirically-found variation [58] of device life-time versus I_{sub} is:

$$\tau \propto \left(\frac{I_{sub}}{W}\right)^{-1} \tag{2.8}$$

where W is the width of the MOSFET.

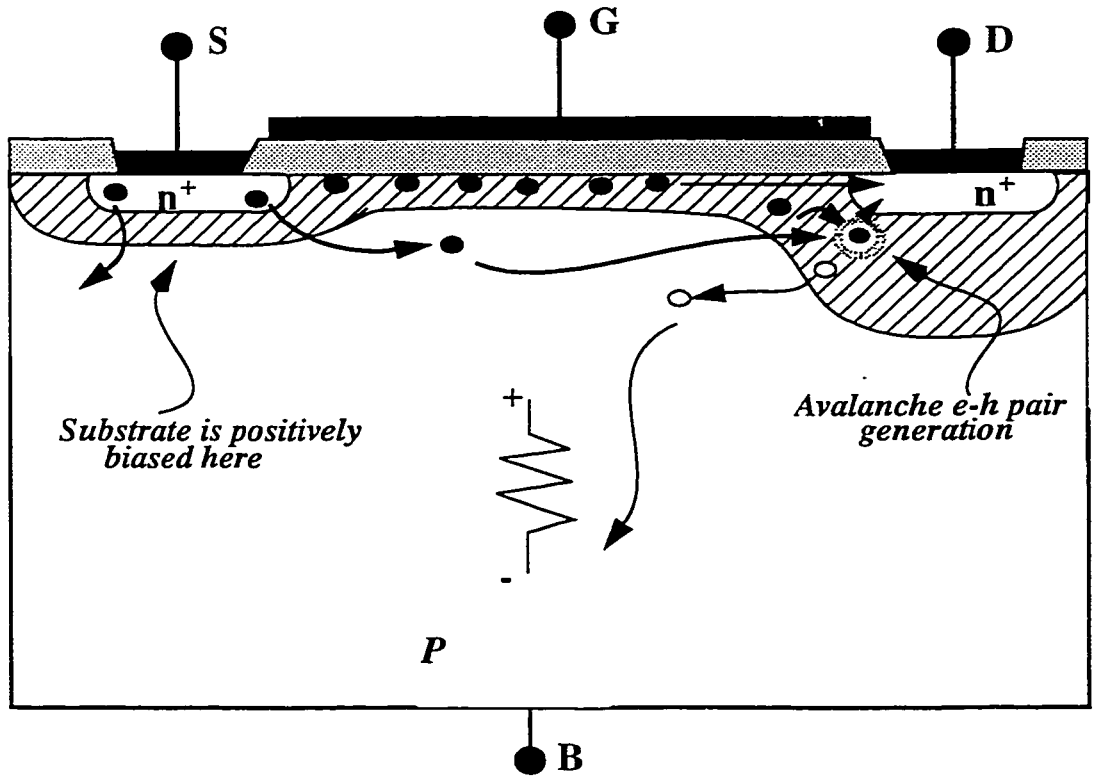


Fig. 2.5 - A MOSFET with impact ionization happening in the drain space charge region.

2.2 Background On Fluorinated And Oxynitrided Gate Oxides

2.2.1 Fluorination

2.2.1.1 Fabrication Processing

There are four reported ways to incorporate fluorine into gate-oxides:

1) HF-last cleaning treatment prior to thermal oxidation [25-23].

2) NF_3 -gas thermal growth of oxide with parts per million of NF_3 in the O_2 [28, 60-62].

3) Shallow fluorine-ion implantation into the poly-Si gate, followed by heat treatment to diffuse the fluorine into the underlying gate oxide [9, 13, 15, 19, 27].

4) F implant into the Si substrate, followed by the gate oxidation [63].

While the details vary, the results from these techniques are qualitatively very similar (i.e, an appropriate amount of fluorine gives rise to improvement in the the resistance to hot-carrier-induced or radiation-induced damage), Note, however, that either too little or too much fluorine does not cause the optimal improvements.

2.2.1.2 F-Build Up At The Si/SiO_2 Interface (or F Distribution Into Si)

According to Ma [14], if an oxide was thermally grown at 1000°C in ultra-dry O_2 on a Si wafer which had previously been immersed in a 2.5% aqueous HF solution for 5 min, then the amount of fluorine remaining in the oxidized sample is approximately

$3x10^{13}cm^{-2}$. This would not be enough to beneficially impact the resistance to hot carrier injection.

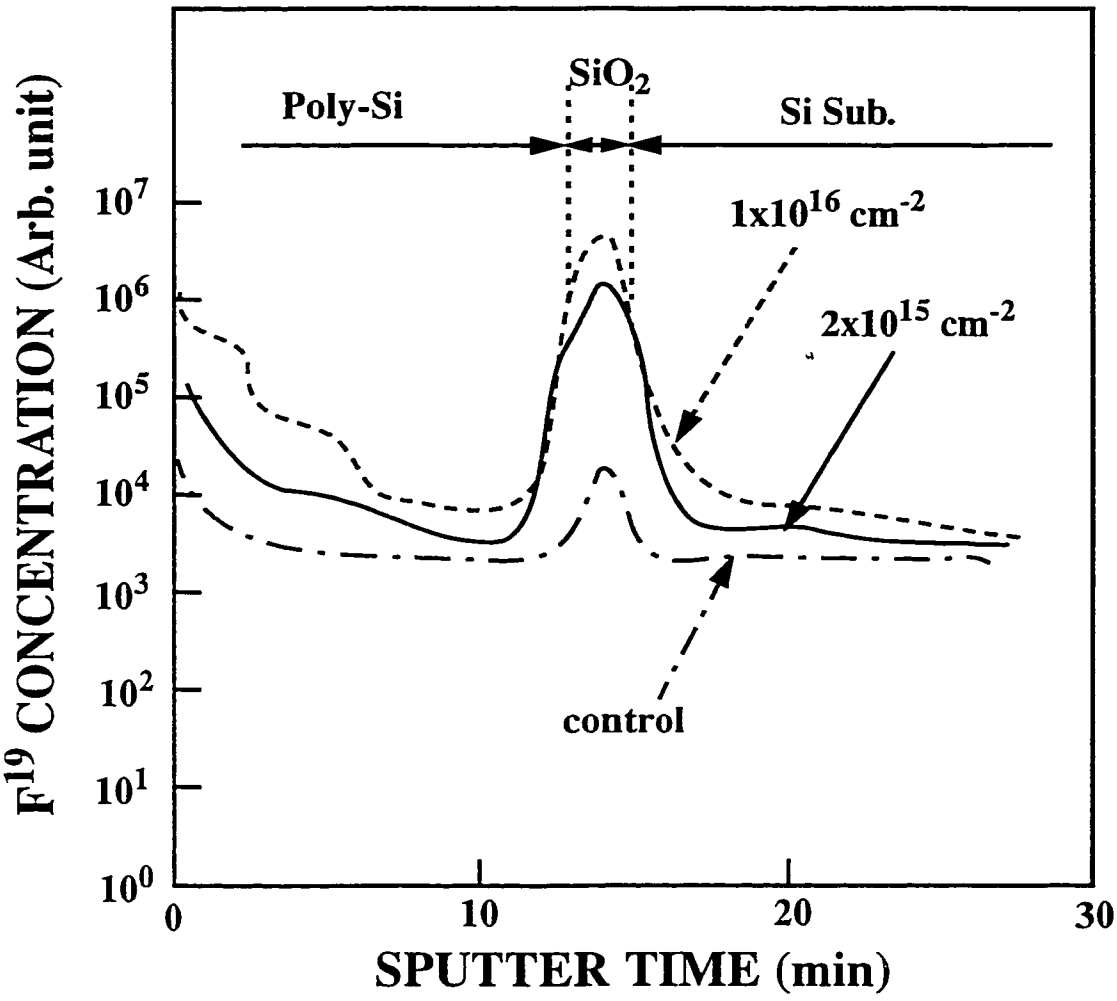


Fig. 2.6 - SIMS profiles of MOS structures after F implantation into the poly-Si gate followed by diffusion (at 950°C for 10min) i) control, ii) implant dose of $2x10^{15}$ cm^{-2}, iii) implant dose of $1x10^{16}$ cm^{-2} [14].

In many articles, SIMS profiles have shown that, by any method of fluorination, there is a significant amount of fluorine located in the bulk oxides [14-15, 25, 60]. Fig. 2.6 displays fluorine profiles when the ion implantation method is used. For this profile, again

a significant amount of fluorine is now located in the bulk oxide. In addition, Saraswat [15] reported further details in fluorine-ion implantation that while the fluorine is almost completely segregated into the oxide, the fluorine profiles show two peaks in the bulk oxide, and these two peaks are located at both interfaces of the SiO_2.

2.2.1.3 Electrical Characterization Data

In this section, some typical data will be reported, digested from a survey of numerous publications on the topic. In short, fluorinated oxides are usually better than the control oxides in the following cases:

◆ During CCFN and CVFN hot carrier stresses, less distortion is found in the HF C-V and LF C-V curves (see Fig. 2.8a) [14, 25]. This leads to less generated D_{it} (see Fig. 2.8b) [14, 25]. These curves also indicate that the shift of flatband voltage is less for fluorinated gate oxides.

◆ In 1989, Ma [14] showed that the resistance to hot carrier injection varied substantially with fluorine dose. Changes in flatband voltage and D_{it} were measured during FN hot-carrier stressing. Optimal implant conditions were found to be $2x10^{15}$ cm^{-2} at 25keV, for a 3500Å polysilicon gate on top of ~250Å of oxide [14], consistent with the data in Figs. 2.9 (a), (b) [9,15].

◆ Virdi *et al* [63] observed that the presence of fluorine reduced the interface state density. Xie and Young [64] further distinguished between fast and slow interface states, and found more complex behavior as a function of implant dose. Fluorine-dose was found

to critically influence fast state density and was found to suppress slow states. They suggested that a judgement of optimum implant conditions should take account of the impact of fluorine on both types of states.

◆ For fluorine-implanted samples, under channel hot carrier injection, the reported results also show less shift in threshold voltage and less change in transconductance (see Fig. 2.10) [9].

◆ Since fluorinated oxide (fluorine-ion implanted oxides), show less degradation in transconductance and less shift in threshold voltage, then fluorinated oxides are more reliable than the control [12]. Fig. 2.11 supports this statement.

2.2.1.4 Role of F

Two possibilities have been proposed to explain the reliability improvement of fluorinated oxides when an appropriate amount of fluorine is introduced into gate oxide [12, 14, 60]:

i) Formation of SiF bonds in place of SiH bonds at the Si/SiO_2 interface.

ii) Strain relaxation.

Fig. 2.7 is constructed to illustrate the above two hypotheses. Numbers in diamonds indicate chemical processes happening. The top (left) diagram shows the Si/SiO_2 interface before any chemical process has occurred. The bottom (right) diagram shows chemical bonds generated associated with the indicated numbers in the top diagram.

As shown in Fig. 2.7, the first possibility is that a fluorine atom can break a Si-H bond (process (2)), or a Si-OH bond, to form a Si-F bond (process (3)) in its place. Research in the field shows that fluorine in thermal SiO_2 tends to form the Si-F, not the Si-O-F, bond [14, 15, 60]. Because the Si-F bond (5.73eV) is stronger than the Si-H bond (3.18eV) and Si-OH bond [12, 60], fluorinated oxide is more resistant to hot carrier damage [14, 60]. This hypothesis may explain some of the results but not the cases where excessive amounts of fluorine actually cause degradation of the oxide reliability [14].

Ma [14], Wright and Saraswat [12] proposed that the essence of the strain relaxation model is: when a small amount of fluorine is incorporated, fluorine atoms terminate the Si dangling bonds (process (1)), break some strained bonds (process (4)) near the Si/SiO_2, interface and thus reducing the interface stress. However, when a fluorine atom breaks a strained Si-O-Si bond (near the Si/SiO_2 interface), this forms a Si-F bond and a non-bridging Si-O bond. Consequently, an excessive amount of incorporation induces a large amount of non-bridging oxygen centers, which are precursors of interface states [15, 60]. In other words, these non-bridging bonds may be harmful to the oxide reliability. Therefore, the optimum fluorine concentration corresponds to the situation at which the benefit of strain relaxation exceeds the opposite effect caused by the non-bridging oxygen bonds.

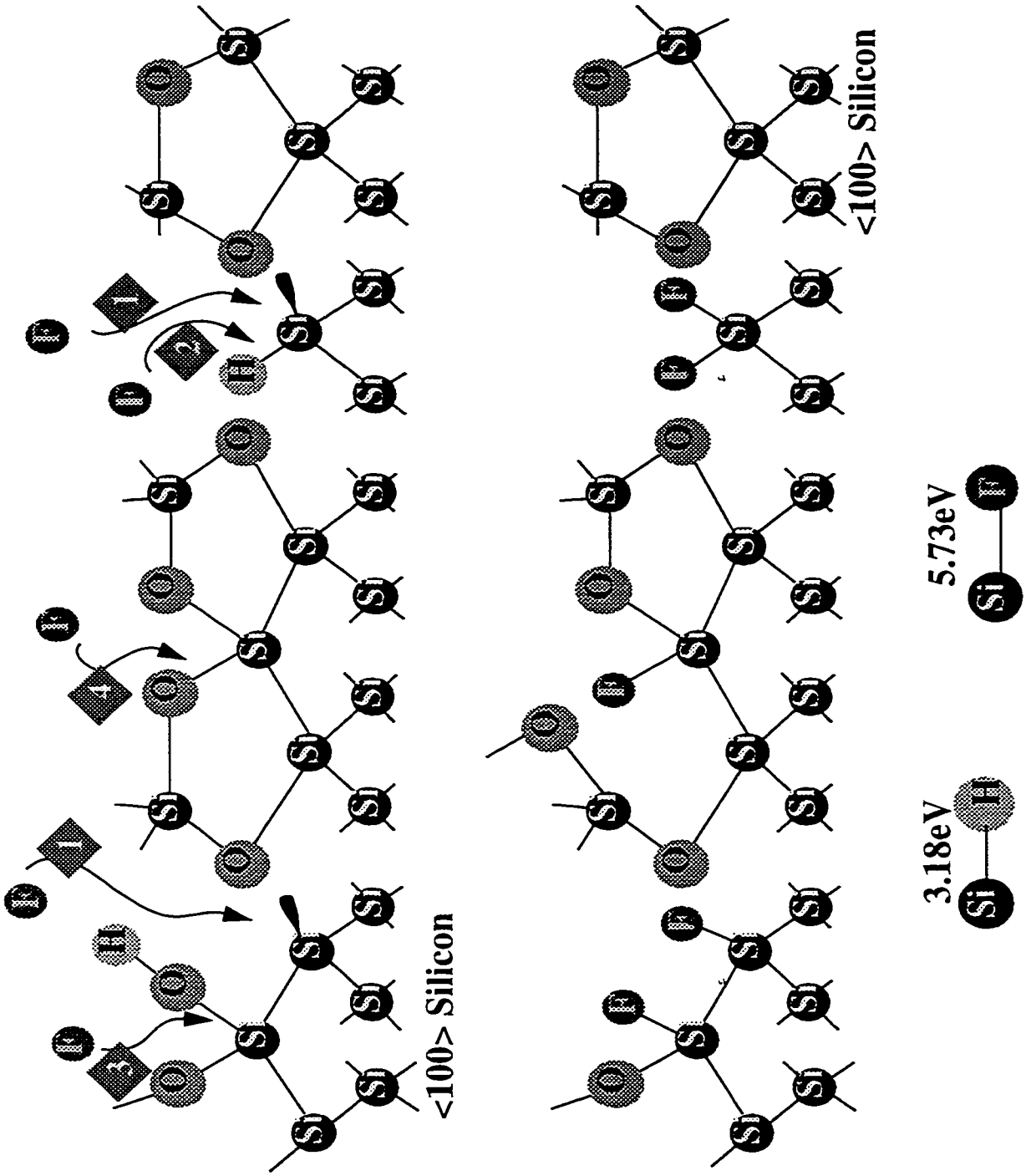


Fig. 2.7 - Proposed Possibilities used to explain why fluorination improves the quality/performance of gate oxides. Numbers in diamonds indicate chemical processes like: 1) Fluorine atom fills the dangling bond. 2)Fluorine atom replaces hydrogen to form Si-F bond. 3) Fluorine atom replaces OH group to form Si-F bond. 4) Fluorine atom breaks the strained bonds Si-O-Si to form a Si-F and a non-bridging Si-O bonds.

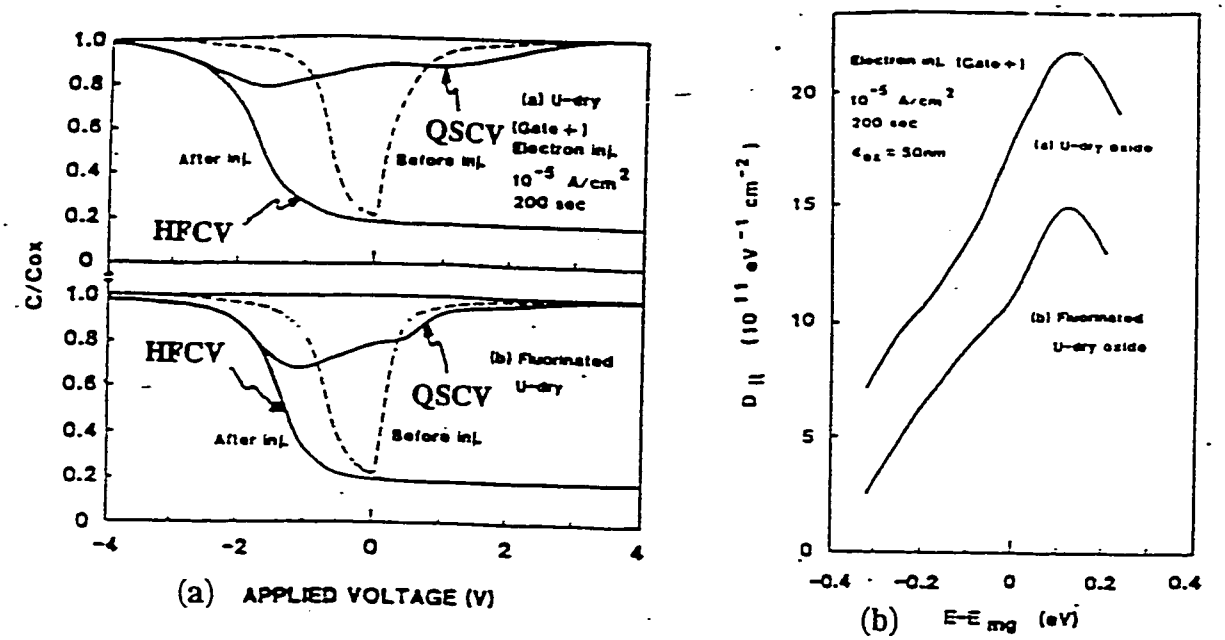


Fig. 2.8 - a) High Frequency and Quasi-Static CV curves before and after constant current electron injection. Samples were prepared by HF dip followed by dry-oxidation [14, 25]. b) Interface trap distribution after constant current electron injection in samples prepared as shown in Fig. 2.6 (a) [14, 25]

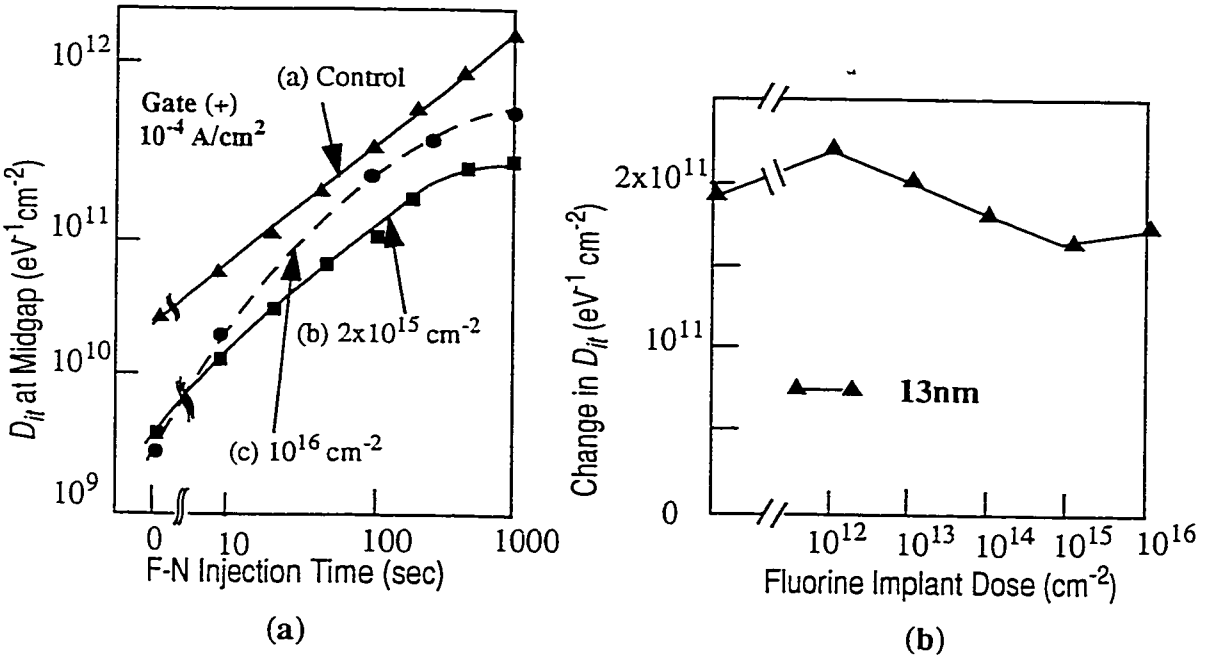


Fig. 2.9 - a) Increase of interface trap density for three sets of MOS capacitors as a function of FN electron injection time. Electrons were injected from silicon substrate at a constant rate of 10^{-4} A/cm^2 [9]. b) Change in D_{it} after a constant current stress of 10mA/cm^2 from the substrate into capacitors for a total charge of 0.1 C/cm^2. The samples were prepared as implanted with a dose of 10^{16} cm^{-2} at an energy of 90keV. The thickness of poly-Si is 2500Å. The annealing time is 30min at 900°C [15].

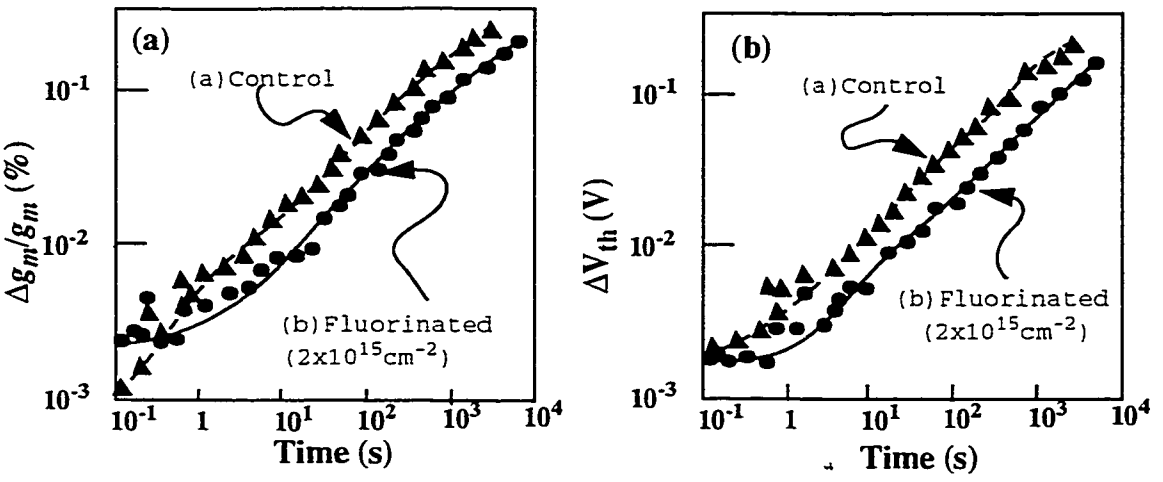


Fig. 2.10 - a) Transconductance (g_m) degradation and b) threshold voltage (V_{th}) shift for a set of fluorinated MOSFET's and a set of control MOSFET's as a function of hot carrier injection time. The stressing condition were: Gate bias V_g = 3V, Drain bias V_d = 7V, source and substrate bias V_s=V_b= 0V [9].

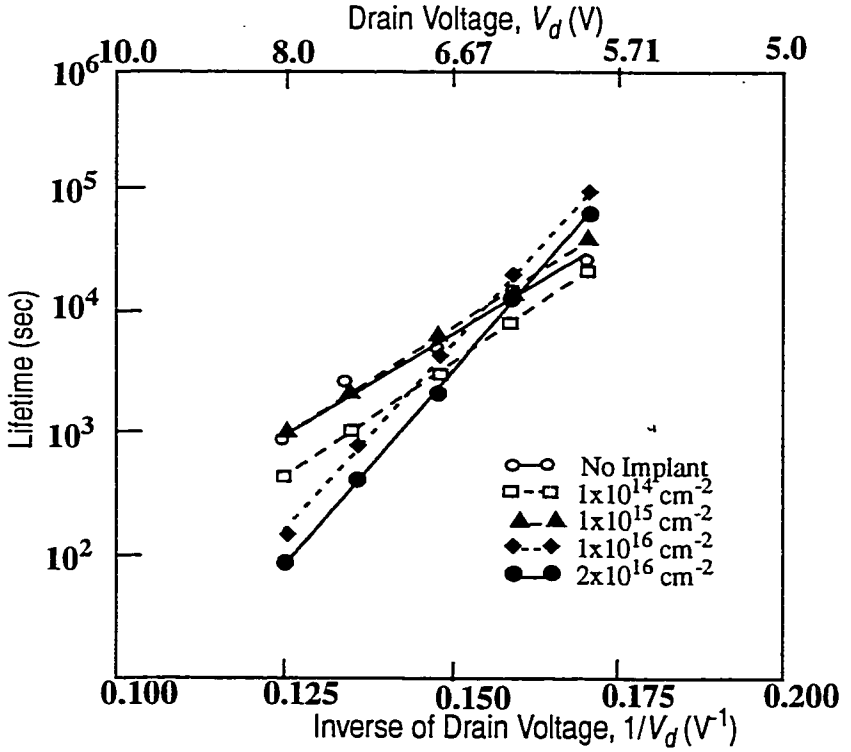


Fig. 2.11 - Reciprocal drain voltage dependence of hot carrier induced life time degradation until 10% reduction in g_m. Gate voltage was set to its value for peak substrate current [12].

2.2.2 Oxynitridation

2.2.2.1 Fabrication Technology

Oxynitridation is used as a variation of thermal oxidation. Nitrogen is introduced into the gate oxide by introducing gases such as NO (a toxic gas) [40] or N_2O (a harmless gas) [65], or by NH_3 [32] during or after the oxydation cycle. To do oxynitridation, the procedure can be either one-step oxidation [66], in which the oxide layer is grown in an ambient consisting of N_2O, NO or NH_3, or two-step oxidation [67], in which a conventional oxide layer is grown and then is subsequently treated in an ambient consisting of N_2O, NO or NH_3.

Grown by either method, oxynitrides have always been reported to have better quality than simple thermal oxides. Oxynitrides are widely considered to be the most promising technique for the future of CMOS technology [68].

2.2.2.2 N-Build-Up At The Si/SiO_2 Interface (or N Distribution Into Si)

Fig. 2.12 show that nitrogen atoms tend to relocated at the Si/SiO_2 interface after re-oxidation in a nitrogen-containing gas [65]. Fig. 2.12 also shows that the concentration of nitrogen at the Si/SiO_2 interface is a function of the oxidation temperature and the percentage of N_2O in the gas ambient. It is quite obvious from Fig. 3.7 that, for the same percentage of N_2O in the gas ambient, a higher re-oxidation temperature will give a higher concentration of nitrogen at the Si/SiO_2 interface [65].

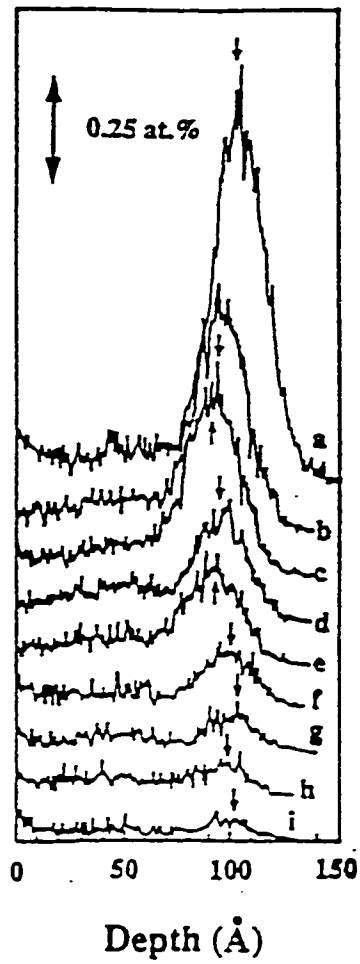


Fig. 2.12 - Nitrogen profiles determined by SIMS analysis. The arrow indicates the Si/SiO_2 interface. The thickness of oxynitrides is about 100Å. These oxynitride films were grown from a) 100% N_2O at 1100°C. b)75% N_2O at 1100°C. c)75% N_2O at 1050°C. d)50% N_2O at 1100°C. e)50% N_2O at 1050°C. f)50% N_2O at 1000°C. g)25% N_2O at 1100°C. h)25% N_2O at 1100°C. and i) 25% N_2O at 1000°C [65].

2.2.2.3 Electrical Characterization Data

◆ Several previous studies have shown that the oxynitrides have greater charge-to-breakdown, Q_{bd}, than thermal oxides. Okada *et al* [38] show that, the higher the concentration of N_2O in the oxynitridation ambient (in the range 0% to 100%), the higher the charge-to- breakdown, Q_{bd}, and that the Q_{bd} of oxynitrides is 2-4 times larger (0.5-0.9 C/cm^2) than the control (thermal) case (0.2-0.6 C/cm^2).

◆ According to Hwang *et al*, [69] if the oxynitridation temperature is high (1000°C-1200 °C), the shift of the interface trap density, D_{it}, under a constant current Fowler-Nordheim stress (CCFN) of 10 mA/cm^2, at high fluence (0.1-10 C/cm^2) is an order of magnitude lower than the control case. For example, for samples oxynitrided at 1000°C, 1100°C and 1200°C, at an injected fluence of charge of 1 C/cm^2, D_{it} at midgap are $4x10^{11}$, $2x10^{11}$ and $6x10^{11}$ $eV^{-1}cm^{-2}$ respectively, while the control has a D_{it} at mid-gap of $>1.5x10^{12}$ $eV^{-1}cm^{-2}$ (see Fig. 2.13) [69].

◆ Under Fowler-Nordheim hot carrier stress, oxynitrides exhibit less bulk charge trapping (see Fig. 2.14) [70].

◆ Oxynitridation shows higher reliability under channel hot carrier injection (see Fig. 2.15) [67].

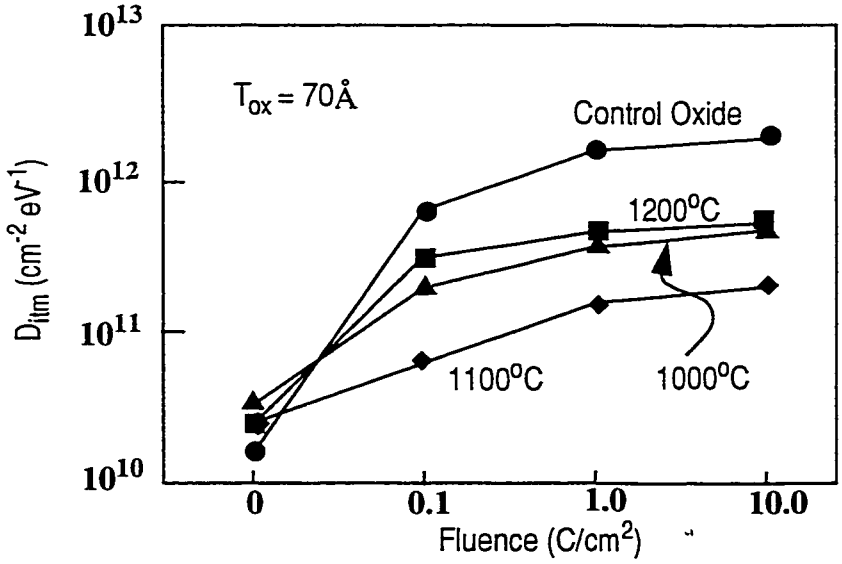


Fig. 2.13 - Calculated midgap interface states (D_{itm}) using HFCV - LFCV technique. Oxynitrides show much lower change in midgap interface states, ΔD_{itm}, under constant current stress (+10mA/cm^2) in comparison to control oxide. Oxynitrides grown at 1100°C show the least degradation [69].

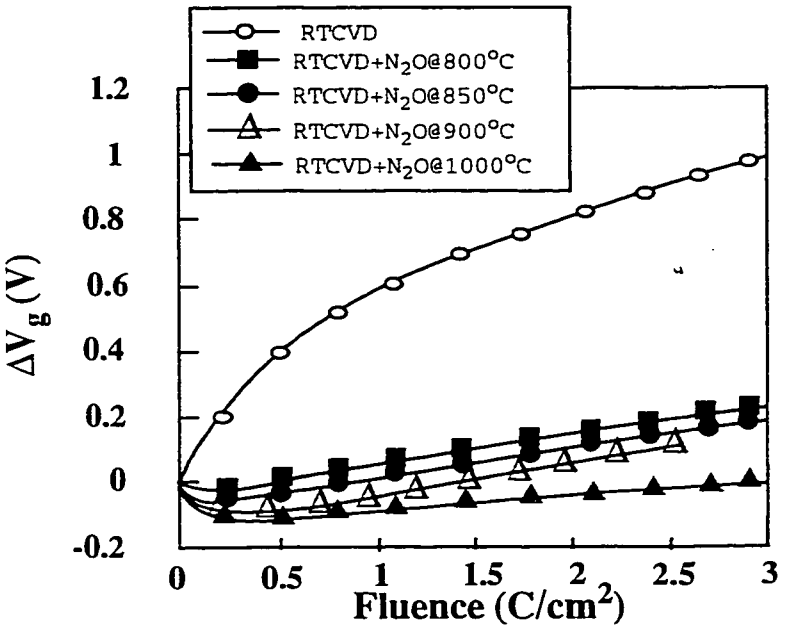


Fig. 2.14 - Gate voltage shifts vs. injected fluence. The plots show charge trapping for deposited films reoxidized in N_2O at different temperature. Hot electrons are injected from the substrate. Area = 2.5×10^{-5} cm^2, current density = 0.01 A/cm^2 [70].

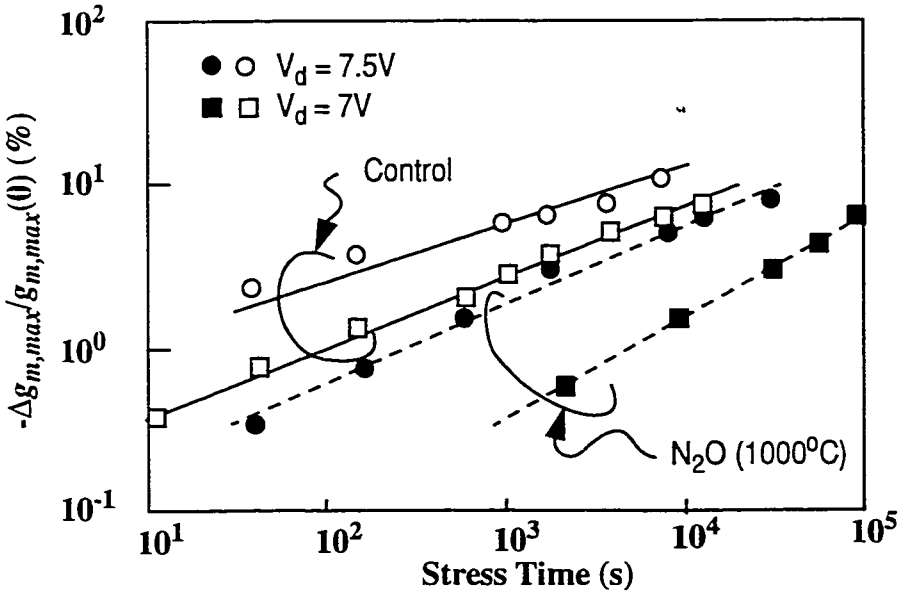


Fig. 2.15 - MOSFET transconductance degradation under channel hot electron stress. The stresses are applied at condition for stress is applied at maximum substrate current, where the oxynitrided gate oxide of devices was grown in N_2O at 1000°C for 8 min to a thickness of 61Å. The control oxide is 62Å [67].

2.2.2.4 Role of N

Similar to the role of F, nitrogen replaces the Si-H chemical bond to form the Si-N bonds. Recently (1997), Ellis, Carr and Buhrman [71] showed that nitrogen is bonded as $Si_3{\equiv}N$ near the interface and as $Si_2{=}N$- away from the interface, and that it is the $Si_3{\equiv}N$ species which is responsible for improved resistance to interface state generation. This $Si_3{\equiv}N$ bond is actually the chemical bond found in Si_3N_4.

Using Auger electron spectroscopy (AES), secondary ion mass spectroscopy (SIMS) and electrical characterization, Hori *et al* [31], have formed a semi-empirical formula to explain the dramatic reduction of flatband voltage shift, ΔV_{fb}, and D_{it} in oxynitrides during hot carrier stress. Hori *et al* suggest that the better electrical properties are caused by the presence of nitrogen atoms (N) at the Si/SiO_2 interface, and reduction in the concentration of more-active hydrogen atoms (H) at the interface.

While the above works concentrate on the defects at the Si/SiO_2 interface, the work of Fukuda *et al*, [72] considers bulk trapped charge in oxynitrided samples of 100Å thickness with oxynitridation temperature in the range of 1100-1200°C. According to Fukuda *et al*,[72] the replacement of Si-N, Si-OH and Si-O-Si bonds can result in lower (better) rate of oxide-trap creation, dV_g/df, where $V_g(f)$ is the gate voltage as a function of f, and f is cumulative injected charge, or fluence. Also, Fukuda *et al*, [72] show that the above-mentioned chemical replacements cause greater (better) charge-to-breakdown (Q_{bd}), and low D_{it}.

2.2.3 Fluorination- And Oxynitridation-Related Issues Addressed In This Thesis

2.2.3.1 Fluorination Related Issues

In general, and based on studies such as those mentioned above, F-implanted oxides are often believed to have higher quality than standard thermal SiO_2 films, as indicated by reduced ΔV_{fb} and D_{it}. This is usually thought to be because Si-H bonds at the Si/SiO_2 interface are replaced by Si-F bonds, which are stronger than Si-H bonds [15] leading to lower measured interface state density. However, the intepretation of D_{it} in the case of fluorinated oxides may be in question. Saraswat *et al* [15] mention that fluorine-implants may change interface state densities outside the Si bandgap. In particular, the state due to the stronger Si-F bond is likely to be more than 0.5eV outside the Si conduction band. Thus standard high-frequency and low-frequency C-V data may not be sensitive to the full effects of the fluorine-implant on the Si/SiO_2 interface.

In the view of the above, while V_{fb} and D_{it} are reasonably employed as *overall* indicators of oxide reliability, it appears that the detailed roles of fluorine incorporated into a MOS gate oxide remain unresolved. It is likely that there may be several effects, both in the bulk and at/near the interface, which may impact electrical measurements in complex ways.

This work aims to supplement the existing body of experimental research by investigating the roles of fluorine, both at the interface and in the bulk. By using the theoretical framework of DiMaria *et al* [43], we use C-V analysis and shifts of gate voltage during electrical stressing to determine variations of both bulk and interface charge components

with experimental conditions. In this way, we attempt to sort out the various components of induced charge in fluorinated gate dielectrics subjected to high-field hot-carrier injection. The results are then related to the existing body of experimental research on the topic.

2.2.3.2 Oxynitridation Related Issues

It is generally believed that oxynitrides have better reliability than many other oxides. However, there is not widespread agreement about the effect of oxynitridation on the bulk oxide. For example, according to V. Misra *et al*, [70] and A.Yankova *et al*, [18] while the incorporation of nitrogen into the Si/SiO_2 interface increases the hardness of the interface, the presence of nitrogen in the bulk can cause detrimental effects on the quality of bulk oxides.

Secondly, from the SIMS profile [31, 65], while nitrogen enhances the reliability of gate oxides by creation of $Si_3{\equiv}N_4$, at the Si/SiO_2 interface [71], it is not clear that oxynitridation can gain that advantage at the $poly/SiO_2$ interface. This conclusion can be made from the SIMS profile [31, 65], in which shows there is only the nitrogen built-up at the Si/SiO_2 interface, but not at the $poly/SiO_2$ interface.

This work aims to supplement the existing body of experimental research by investigating the roles of nitrogen, both at the interface and in the bulk. By using the theoretical framework of DiMaria *et al* [43], we use C-V analysis and shifts of gate voltage during electrical stressing to determine variations of both bulk and interface charge components with experimental conditions. In this way, we attempt to sort out the various components

of induced charge in oxynitrided gate dielectrics subjected to high-field hot-carrier injection. The results are then related to the existing body of experimental research on the topic.

CHAPTER 3

EXPERIMENTAL AND CHARACTERIZATION STRATEGIES

3.1 Importance of Studying Charge Components Generated During Fowler-Nordheim Injection Under Positive And Negative Gate Bias.

The study of the effect of either fluorine or nitrogen incorporation into the bulk of gate oxides has not been widespread. The framework of DiMaria *et al* [43-44], discussed in Section 2.1.2, has shown the difference between flatband voltage charge sensitivity and gate voltage charge sensitivity. Flatband voltage is sensitive to all trapped charges existing in the SiO_2 and at the Si/SiO_2 interface, and weighted by the centroid of the distance of the charges from the gate/ SiO_2. On the other hand, gate voltage is sensitive to changes in trapped charge, outside of a tunneling distance away from the injecting interface, and weighted by the centroid of the distances of those charges from the opposite, non-injecting interface. By employing these ideas, one can study in a systematic manner the locations of the charges induced in fluorinated and oxynitrided gate oxides.

The following table (Table 3.1) shows the main possibilities according to gate bias

	V_{fb}	V_g	V_{fb}-V_g
+ Gate bias	Senses all charges including ones at the SiO_2 interfaces	Senses only charges located outside a tunneling distance from the Si/SiO_2 interface	Senses charges located within a tunneling distance from the Si/SiO_2 interface.
- Gate Bias	Senses all charges including ones at the SiO_2 interfaces	Senses only charges located outside a tunneling distance from the poly-Si/SiO_2 interface	Senses charges located within a tunneling distance from the poly-Si/SiO_2 interface.

Table. 3.1 - Oxide charge sensitivity of V_g, V_{fb}, V_{fb}-V_g

Thus it is clear that the difference between flatband voltage shift, ΔV_{fb}, and gate voltage shift, ΔV_g, can give information about charges located within a tunneling distance of the injecting interface. By employing these concepts and measured and derived quantities, we can study charge components in thin oxides in some detail.

Under positive gate bias, the difference between total charge (calculated from ΔV_{fb}) and the bulk charge calculated from Eq. 2.5 or Eq. 2.7 will give us quantitatively the charge generated at/near the Si/SiO_2 interface (within a tunneling distance from the interface, see Table 3.1). This method has an advantage (compared to a D_{it} measurement) that, we can calculate the real density of trapped charges, rather than the distribution function of interface states, which are quite impossible to convert into density of actual charges. Another advantage is that we can evaluate the trapped charges generated in the bulk oxide (outside a tunneling distance form the Si/SiO_2 interface, see Table 3.1) during the Fowler-Nordheim stress. Such parameters as trapped charge generation rates can be calculated by this technique.

In addition, in very thin oxides, the traps generated at the other interface (poly-Si/ SiO_2) can play a role in the ULSI device function, For example, Fig. 3.1 displays the operational biases for an E^2PROM, invented at Toronto University [73]. In the reading cycle, the device works as a common MOSFET, and thus the most damage comes from low-field hot-electron injection and channel hot-electron injection. However, the mentioned stresses can only cause severe damage when the device operates for long periods of time, say years. For the writing (+12V gate bias) and erasing (-15V gate bias) cycles, now the tunnel oxide is subject to very high field hot-electron injections. Therefore, with a view to E^2PROM performance, one must pay close attention to the reliability of MOS structures in both bias configurations. By applying negative gate bias on MOS capacitors, now the difference between ΔV_{fb} and trapped charges calculated from either Eq. 2.5, or Eq. 2.7, gives us information about how the trapped charges are generated at/near the poly/SiO_2 interface (within a tunneling distance). This information also can help us to improve operation of flash E^2PROMs which are sensitive to the behavior and reliability of very thin SiO_2 films under both positive and negative gate biases as discussed.

Using a variation of the DiMaria framework, all of the above effects can be studied in an integrated manner, to derive a set of conclusions about fluorinated and oxynitrided oxides.

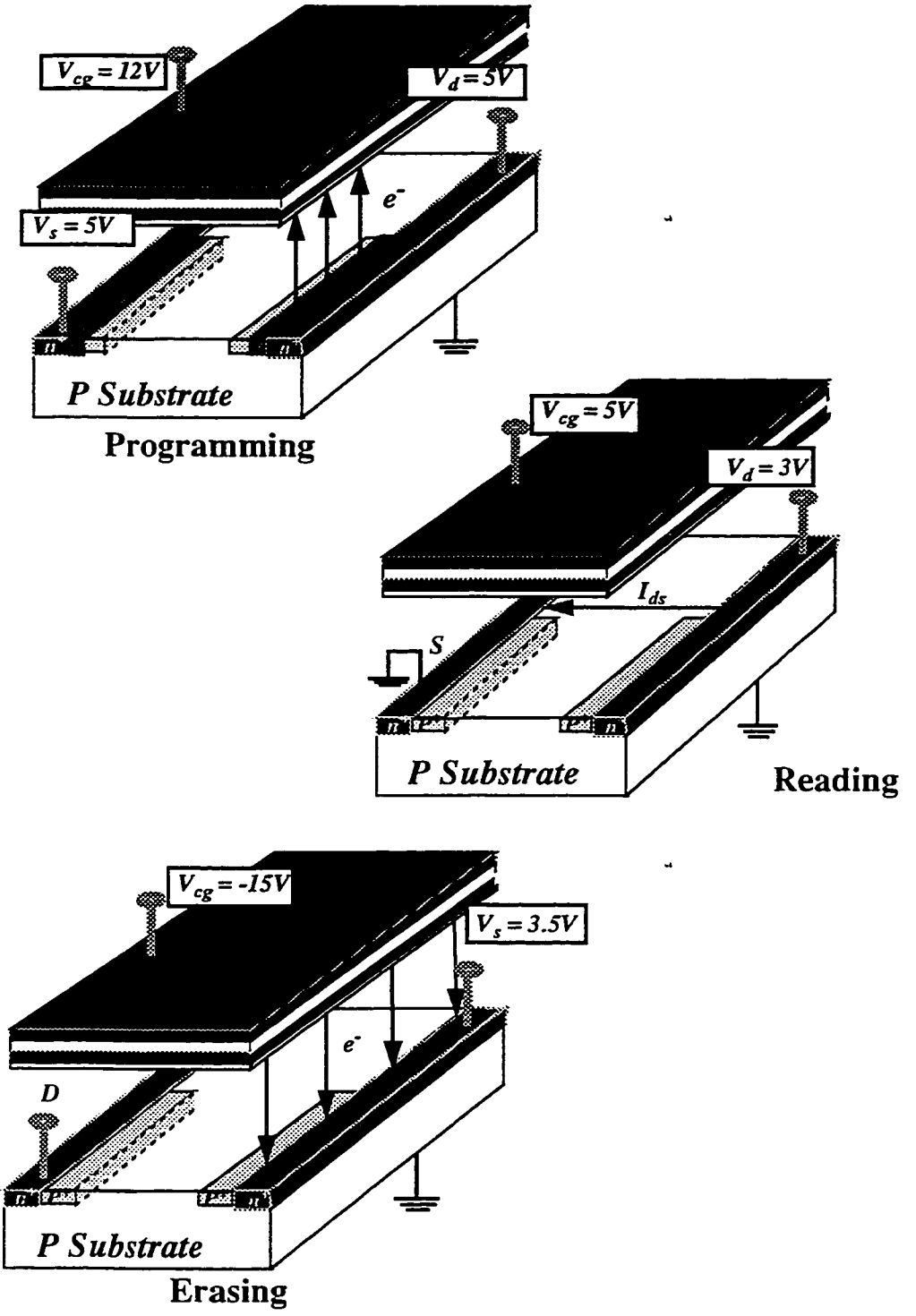


Fig. 3.1 - Schematic to show operational conditions of an E^2PROM [73] in the working cycles: Programming, Reading, Erasing. The thickness of the tunnel oxide is about 100Å.

3.2 Film Characterization Techniques

In this work, the induced charge components under high-field charge injection conditions are studied. Hot carriers are injected in the positive gate bias configuration. The flatband voltage shift, ΔV_{fb}, is a measure of built-up charge throughout the oxide layer including charging at/near both SiO_2 interfaces weighted by the centroid of the distance from the injected interface. On the other hand, gate voltage shift, ΔV_g, is not sensitive to induced charge within a tunneling distance from the injected interface. The information about charging at/near the interface (cathode or the injected interface) during CCFN stress then can be extracted from the difference between flatband voltage shifts and gate voltage shifts, both measured during CCFN.

3.2.1 Capacitance-Voltage (C-V) Measurement

In our experiments, C-V measurements are done by using a probe station enclosed in a dark shielded box with automated high-frequency C-V (HF) and low-frequency C-V (LF). The values of flatband voltages, $V_{fb}(t)$, are recorded via high frequency C-V measurements. From combined HF and LF C-V measurements, standard calculations [74] obtained interface trap density versus energy in the silicon bandgap, (D_{it} curves). Such HF and LF measurements are performed at various times during the experiments, including before and after CCFN injection stress.

From HF C-V measurements, standard calculations obtained V_{fb}, V_{th} and Q_f (nominally fixed oxide charge). The parameter of most concern between the two types of voltages usually is the flatband voltage rather than the threshold voltage. The reason is, if the

difference between $D_{it}(0)$ and $D_{it}(2\phi_B)$ is insignificant, then the relationship between V_{fb} and V_{th} is (see Appendix A.3 for the derivation):

$$V_T = V_{fb} + 2\phi_B \pm \frac{\sqrt{2q\varepsilon_s N_B[\pm 2\phi_B]}}{C_{ox}} \tag{3.1}$$

where ϕ_B is the Fermi level measured from the intrinsic level in the bulk, q is electronic charge, (+) for n-channel device, (-) for p-channel device, and N_B is either donor or acceptor doping concentration as appropriate. Therefore, it seems that the threshold voltage is the flatband voltage plus a constant (for Eq. 3.1).

Secondly, the so calculated Q_f, actually, is a total of fixed oxide charge, interface trapped charge at no band bending, and whatever trapped charge exists in the bulk oxide prior or post stress [75, 76], $(Q_f + Q_{it}(0) + Q_{ox})$, rather than merely Q_f (see Appendix A.4). From combined HF and LF C-V measurements, standard calculations obtain the midgap D_{it}, the density of interface states at midgap.

3.2.2 Fowler-Nordheim Stress

Hot electron Fowler-Nordheim tunneling stress can be carried out by either Constant voltage stress (also called *j-t* stress) or by constant current stress.

3.2.2.1 *j-t* Stress

This test is accomplished using a HP4145A parameter analyzer, with positive voltage applied to the poly gate. Then, the evolution of the current density with stressing time is monitored. Such *j-t* data sets are then transformed [43] to calculate normalized current density vs. injected charge (fluence). Normalized current density is computed as the ratio

of $J(t)/\ J(t=0)$. Then, based on Eqs. 2.5 & 2.6, oxide trapped charge density, Q_{ot}, more than a tunnelling distance away from the injecting electrode, is computed from normalized current density and plotted vs. fluence. The *j-t* technique was used in conjunction with C-V analysis to understand the post stress behavior of the control and fluorinated oxides.

3.2.2.2 Constant Current Fowler-Nordheim Stress

To apply CCFN injection stress, a constant current density is applied to the gate of the NMOS capacitor-structure by using the HP4145, and the same probe station and cabling as was used for the C-V measurements described above. Via the HP4145 SMU-based system, gate voltages were recorded as a function of stressing time (t). A constant current is injected into the gate. The associated electric field must be always below the catastrophic breakdown value.

3.2.3 Charging Curves Translated from ΔV_{fb}, ΔV_g and $(\Delta V_{fb} - \Delta V_g)$

3.2.3.1 Charging Curves

With recorded values of $V_{fb}(t)$, now values of flatband voltage shifts are calculated as $\Delta V_{fb}(t) = V_{fb}(t) - V_{fb}(0)$. Similarly, values of gate voltage shifts are calculated as $\Delta V_g(t) = V_g(t) - V_g(0)$. Both voltage shifts may be converted to equivalent densities of charged defects N (cm^{-2}) by the following equation, which can be derived from either Eq. 2.7 (or Eq. A.33 in Appendix A.4):

$$N = - C_{ox}\frac{\Delta V}{qA} \tag{3.2}$$

where C_{ox} is the measured oxide capacitance, q is electron charge, A is the gate area, and ΔV is either voltage shift. As noted in Ref. [43] and in Section 3.1, this equation gives the centroid-weighted charge.

The injected fluence, at constant current density, is $f = j \times t$, where j is the constant current density passing through the capacitor gate and t is the stressing time.

With raw data as described above, ΔV_{fb} and ΔV_g are numerically manipulated by the use of Eq. 3.2 to obtain (a) the induced charge throughout the oxide (including charging at the Si/SiO_2 interface) ($N_{\Delta Vfb}(f)$) and (b) the charge only in the bulk oxide (more than a tunnelling distance from the hot-electron injected interface) ($N_{\Delta Vg}(f)$). Then, the difference between these two charging curves is the induced charge near/at the injected interface ($N_{ic}(f)$). The charging curves for (ΔV_{fb} - ΔV_g) can be directly graphically calculated from $N_{\Delta Vfb}(f)$ and $N_{\Delta Vg}(f)$ or from (ΔV_{fb} - ΔV_g) via (Eq. 3.2). These calculated charging curves therefore contain information about interface trapped charge, and bulk oxide trapped charge of the stressed oxides.

Fig. 3.2 displays typical charging curves, extracted as explained above, under (+) gate bias FN stress. In Fig. 3.2, the charge calculated from ΔV_{fb} varies oppositely (from (+) to (-). The variation in trapped charge calculated from ΔV_g, generally, exhibits various stages: (i) an initial increase in trapped positive charge due to impact ionization, (ii) the attainment of a maximum net positive trapped charge, (iii) a shift from net positive to net negative trapped charge, as electron trapping (electron trap creation or filling of electron traps having small capture cross-section [55]), becomes dominant, (iv) increasing net negative trapped charge, which usually continues [43-44, 77] until breakdown. A feature

likely to be of some importance is the zero-crossing fluence. In some special cases as discussed later, the zero-crossing fluence can be used as an indicator to identify which oxides under investigation are more reliable [78, 79].

Fig. 3.3 displays typical charging curves, extracted as explained above, under (-) gate bias FN stress. The shape of ΔV_g charging curves in (-) gate-bias are similar to those of positive gate bias, but the ΔV_{fb} and (ΔV_{fb}-ΔV_g) charging curves are different. Under (-) gate bias, because the corresponding $N_{\Delta Vfb}(f)$[1] is considerably larger than the $N_{\Delta Vg}(f)$[2], then, the $N_{ic}(f)$ has a shape similar to $N_{\Delta Vfb}(f)$. In detail, ΔV_{fb} under (-) gate bias[3] is different from the ΔV_{fb} under (+) gate bias[4] charging curve in two aspects: the maximum positive net charge has a magnitude higher than the maximum point in ΔV_{fb}+, and the maxima are located at a higher fluence. In contrast to (ΔV_{fb}-ΔV_g) charging curves under (+) bias[5], which only contain negative charge, (ΔV_{fb}-ΔV_g) charging curves under (-) gate bias[6] display several stages: (i) an initial increase in trapped positive charge due to impact ionization, (ii) the attainment of a maximum net positive trapped charge, (iii) a shift from net positive to net negative trapped charge, as electron trapping (electron trap creation or filling of electron traps having small capture cross-section), becomes dominant, (iv) increasing net negative trapped charge [80]. There is only one special case, the oxynitride created from a treatment temperature of 1050°C, discussed later in Chapter 8 and Chapter 9, possesses only the two first stages: (i) and (ii).

---

1. Denoted $N_{\Delta Vfb}(f)$- and $N_{\Delta Vfb}(f)$+, for (-) and (+) gate biases, respectively
2. Denoted $N_{\Delta Vg}(f)$- and $N_{\Delta Vg}(f)$+, for (-) and (+) gate biases, respectively
3. Denoted ΔV_{fb}-
4. Denoted ΔV_{fb}+
5. Denoted as N_{ic}+
6. Denoted N_{ic}-

The dashed segments in Figs. 3.2-3.3, suggest the shapes of curves expected but not measured due to the limitations of the set-up of the experiments.

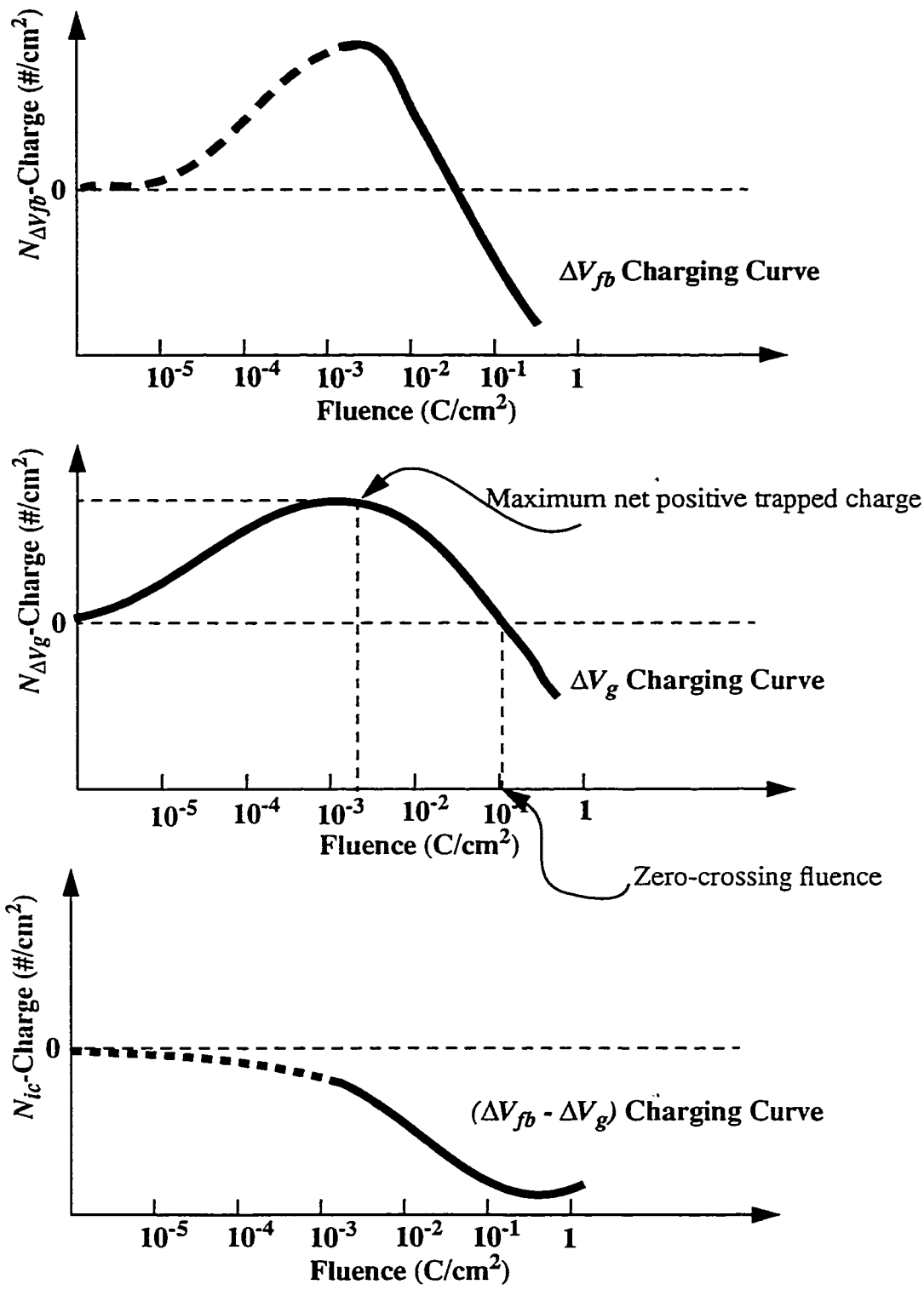


Fig. 3.2 - Typical charging curves, extracted from ΔV_{fb}, ΔV_g, and ΔV_{fb}-ΔV_g, under a (+) gate-bias Fowler-Nordheim Stress.

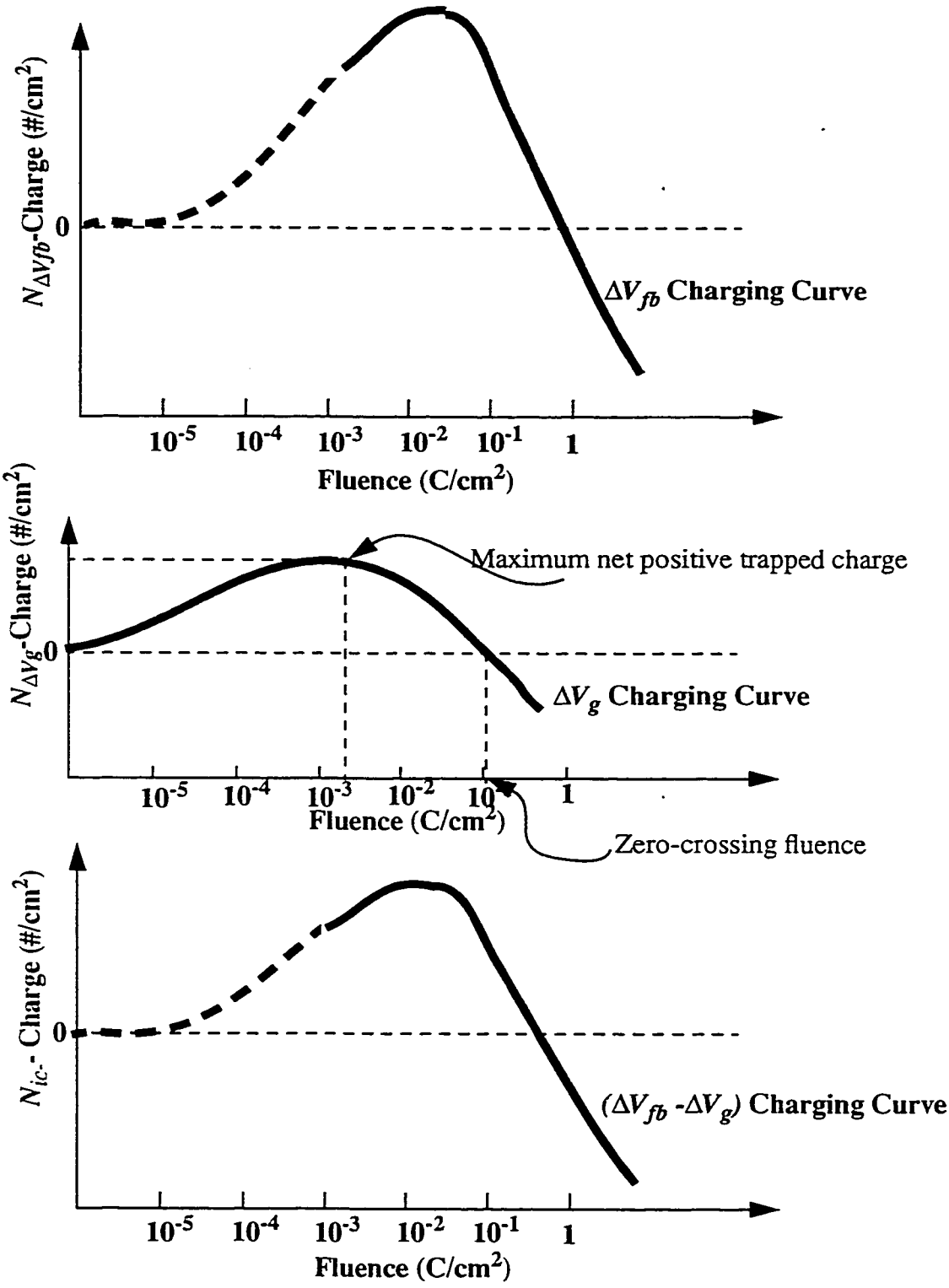


Fig. 3.3 - Typical charging curves, extracted from ΔV_{fb}, ΔV_g, and ΔV_{fb}-ΔV_g, under a (-) gate-bias Fowler-Nordheim Stress.

3.2.3.2 Graphical Model

In this section a graphical model is used to explain the meanings of the zero-crossing fluence and the saturated negative values of charge built up at/near the Si/SiO_2 interface under a (+) gate bias FN stress if anomalous charges are not taken into account [81].

The simplified graphical scheme is built (as shown in Fig. 3.4) based on observations from experimental data. Following is the list of definition of parameter in Fig. 3.4:

A: maximum positive value in $N_{\Delta Vg}+$

AF: Fluence at which the maximum positive value in $N_{\Delta Vg}+$ appears.

B or B': Saturated $N_{ic}+$, assuming there is no existence of anomalous charge

BF: Fluence at which the saturated $N_{ic}+$ is reached.

C or C': Zero-crossing fluence, the fluence at which $N_{\Delta Vg}(f)+= 0$.

This graphical model can help to compare the reliabilities of two or several gate oxides, in which, the values A, AF, BF are almost the same, or the differences are slight. In other words, if A, AF, BF are constant, the use of the proposed graphical model can roughly compare the reliabilities of oxides. Experimentally, this assumption is reasonable for fluorinated oxides (which are to be discussed in Chapter 7).

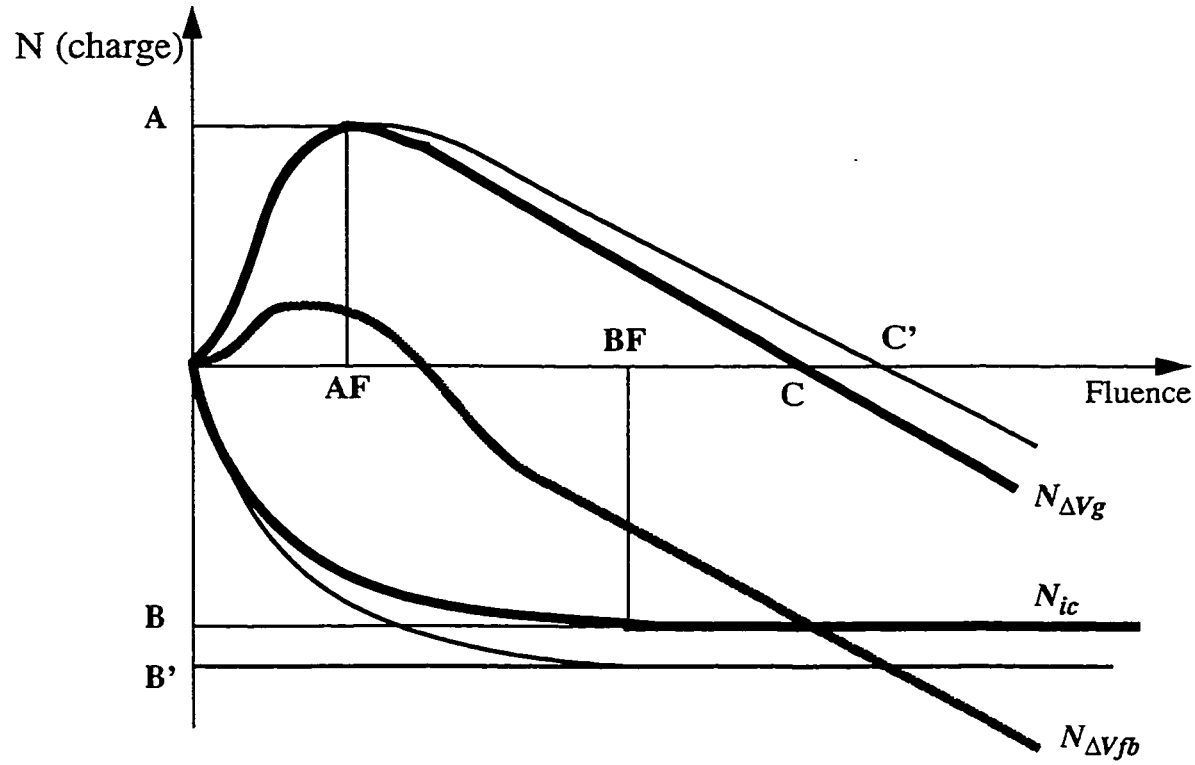


Fig. 3.4 - Schematic of the graphical technique to analyze the charge components induced into gate oxide during CCFN.

For example, under (+) gate bias CCFN, the maximum positive net charge $N_{\Delta Vg}$+ is around ~3.4 x10^{11} /cm^2 for most oxides [78, 79], and has a position on the fluence axis at around 2.3x10^{-3} C/cm^2 (see Table 5.1). These positions correspond to the values of A and AF in Fig. 3.4, respectively. In Figs. 5.5(b)-5.8(b) (see also Fig. 5.10), most of the fluorinated oxides and control oxide reach a saturation/maximum N_{ic}+ value at a fluence of between 8.0 and 9.0x10^{-2} C/cm^2. These are equivalent to the value BF in Fig. 3.4.

Based on the experimental data, it is reasonable to assume that, in Fig. 3.4, A, AF, BF are near constants, whereas saturated negative charge at/near the Si/SiO_2 interface, B,

and zero-crossing fluence, C, vary more substantially. Since $N_{\Delta Vfb} = N_{\Delta Vg} + N_{ic}$, then if C moves to C' while B does not change, the tail of the $N_{\Delta Vfb}$ curve must have a slope less steep than before. In other words, the $N_{\Delta Vfb}$ curve now shows a higher quality oxide during CCFN. Similarly, we can understand the meaning of the result for the case where C stays at the same location, while B moves to B'. In this case, although the slope of $N_{\Delta Vfb}$ curve does not change, an increase in (B-B') downwardly shifts the $N_{\Delta Vfb}$ curve. In other words, $N_{\Delta Vfb}$ curve now presents for an oxide whose quality is worse in high fluence. The effects are opposite if C' move to C, or B' move to B. For example, as shown in discussions in Chapter 7, sample B-2E15-10KeV and sample A-3E14-10KeV have N_{ic}+ almost the same (-4.11×10^{11} and 4.08×10^{11} /cm^2, respectively), but the zero-crossing fluence, are 9.22×10^{-2} and 7.89×10^{-2} C/cm^2, respectively. This would indicate that B-2E15-10KeV must be a better oxide.

A better oxide should have a higher zero-crossing fluence, C, or fewer saturation interface trapped charges, B, or both (best case). Consequently, the worst case only happens when an oxide has a lower C and a higher B. However, it is quite difficult to make a conclusion for a combination of a high B and a high C, or a low B and a low C. To summarize, all possibilities are tabulated in Table 3.2. Because of the trade off between two quantities B and C, the graphical model addresses the complexity of oxide reliability. If a process tries to improve the interface state problem (improve B), but neglects the effect in the bulk oxide (neglect C), this process could cause an overall worse effect instead of better.

		Zero-crossing fluence		
		>[i]	=[ii]	<[iii]
Saturation Interface Trapped Charge	>	Unknown	Worse	Worst
	=	Better	Same	Worse
	<	Best	Better	Unknown

i. > presents for higher
ii. = presents for unchanged or the same
iii. < presents for smaller or lower

Table. 3.2 - Oxide's quality evaluated from varying zero-crossing fluence and saturation interface trapped charge.

3.2.4 Trapping Rate

This is another parameter which can be used to better understand the complicated behavior of charging in the oxides under Fowler-Nordheim injection stress, the trapping rate. Information about the net trapping rate is available from charging curves. $N\Delta_{V_g}$ vs.f data are converted into trapping rate $\Delta N_{\Delta V_g}/\Delta f$. Fig. 3.5 shows the typical shape of the induced charging rate, which is plotted in log-log scale. Since the hole traps have a large capture cross section (in order of 10^{-15} cm^2 or greater) [43, 55], at the beginning (at fluence as small as 10^{-6} C/cm^2 [43, 55]) the charging rate has a large positive value. Then when the ΔV_g charging curve reaches the maximum value, the induced charging rate becomes zero. And after that, the rate becomes negative.

However as the experimental data shown, the log-log scale can not give a clear view to compare the initial net positive (hole) trapping rates at the beginning of each electrical stress [78]. For this, the linear-log scale is used. Fig. 3.6 displays a typical curve of induced charging rate vs. fluence. From Fig. 3.6, it is clear that the net charging rate has

evolved through several stages. i) high and relatively constant net positive trapping rate; ii) rapid reduction in net positive charging rate; iii) net charging rate approaches zero and crosses zero; and iv) the net charging rate is saturated. The linear-log format shows in all studied cases a straight line portion of each curve from about 10^{-4} to about $5x10^{-4}$ C/cm^2 [78-80.] This portion can be modeled as:

$$\frac{d}{df}\left(N_{\Delta V_g}\right) = K_1 log_{10}(f) + K_2 \tag{3.3}$$

where K_1 and K_2 <0.

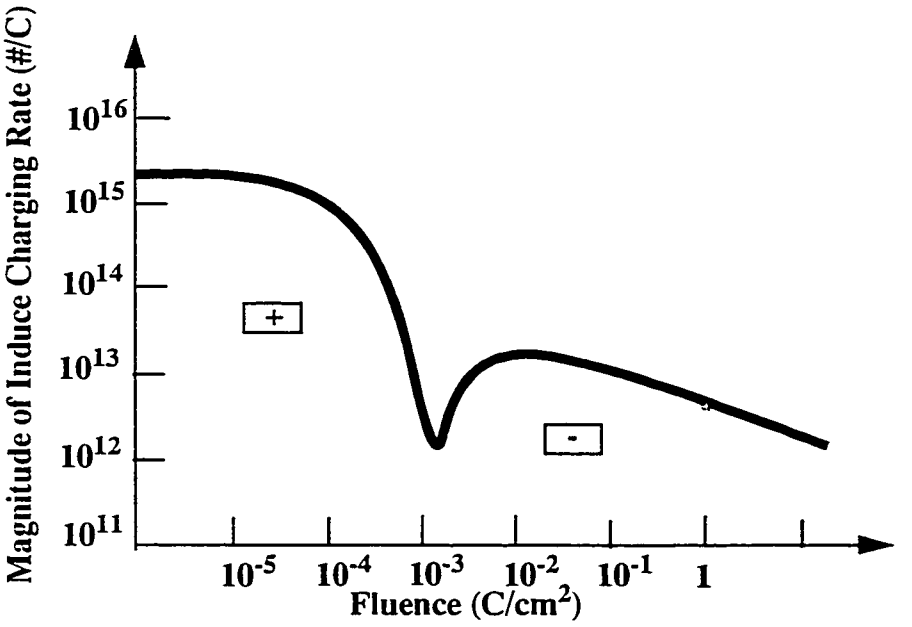


Fig. 3.5 - Magnitude of induced charging rate, which is extracted from ΔV_g charging curve. Typically, the curve starts with positive values, then drops to zero when the charging curve of ΔV_g reaches its maximum. After that the charging rate possesses a negative value.

As shown in Eq. 3.3 and Fig. 3.6, K_1 represents the slope of the curve $d(N_{\Delta Vg})/df$ in stage ii. Stage ii is where the induced charging rate decreases rapidly from net positive to approach zero, and then switch to net negative charging rate [78]. Therefore in Ref. 78, we

called K_1 *the rate of change of the electron trapping rate with respect to fluence.* K_2, as from Eq. 3.3, is the induced charging rate at an injected charge of 1C/cm^2. Practically, K_2 is the actual saturated value of the induced electron charging rate (at high fluence).

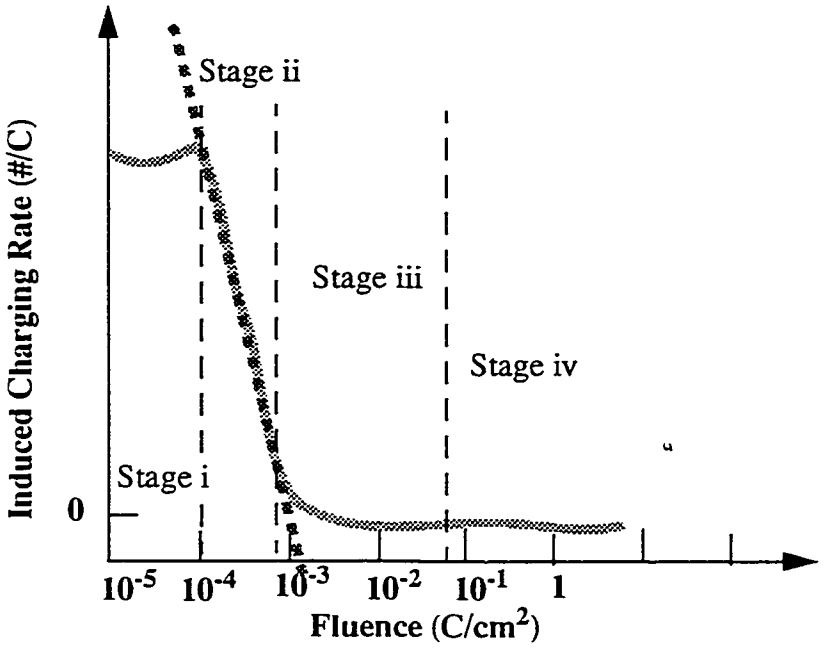


Fig. 3.6 - A typical curve of induced charging rate in linear-log scale. Stage ii is fitted by a straight line using the least-mean square method.

3.3 Electrical Characterization Equipment Set-Up

In order to characterize the fabricated samples, some experimental set ups are required. These set-ups are done in such a way that the measurements at Microelectronics and Fabrication Laboratory, Concordia University are re-producible at Mitel's Laboratory.

Note that the author spent several months to do electrical characterization at Fab2 at Mitel Corp., Bromont (Quebec). Later, based on the experiences gained, the author set

up the measurement environment at Concordia's Microelectronics and Fabrication Laboratory. The set up was calibrated with respect to measurements done in Fab2 at Mitel Corporation

The Set-up can help the user handle measurements such as:

- Obtain High Frequency and Low Frequency Capacitor-Curves on capacitors with poly-silicon gates fabricated at Mitel Corp. Based on these characteristic C-V curves, the interface states density can be extracted.

- Apply Constant Current Fowler-Nordheim stress or *J-t* Technique on MOS capacitors either in positive or negative gate bias.

- Apply Channel hot carrier injection stress on MOSFET with the whole requirement procedure as at Fab2, Mitel Corporation.

Appendix C shows connections and numerical details of the setup.

3.4 Measurement Procedures

3.4.1 Fowler-Nordheim Stress

For Fowler-Nordheim stress, the test structure is the MOS capacitor. In common, this type of electrical characterization is carried out by the following procedure:

i) HFCV and LFCV measurements are done: to get the initial parameters of the MOS capacitor such as V_{th}, V_{fb}, D_{it} at the midgap.

ii) Fowler-Nordheim stress is applied on the MOS capacitor for a certain period of time.

iii) HFCV and LFCV measurements are done: At this point, the after-stress parameters (V_{th}, V_{fb}, D_{it} at the midgap) are recorded/monitored.

iv) Steps ii) and iii) are sequentially repeated for higher and higher injected fluence.

Notice that the timing gap between step ii) and iii) is also important, since after the stress, the relaxation partially moves stressed-values back to the origin. The differences between before-stress and after-stress parameters, then, contain the information about the quality of the investigated gate dielectric.

To study the bulk trapped charge, the gate voltages or the gate currents are monitored in step ii). From the monitored values of I_g and V_g, then we can calculate the trapped charges generated outside a tunneling distance from the injecting cathode interface. In addition, the difference between the initial value of V_{fb} obtained in step i) and later monitored value of V_{fb} gives us the overall trapped charges. As previously discussed, now the difference between the overall charges and the bulk trapped charges shows quantitatively the trapped charges formed within a tunneling distance from the cathode interface.

3.4.2 Channel Hot Carrier Injection Stress

Before applying CHE stress, there are some preparation steps required such as:

- Verify gate leakage current, I_G. If I_G >1pA, the device is bad and must be rejected from the characterization.

♦ Verify at what V_{DS} the snapback phenomenon takes place. Record the V_{DS} value at which the snapback begins. Theoretically, the snapback phenomenon is expected to overestimate the device-lifetime. Therefore, this value of V_{DS} provides the limit of Drain voltage that could be applied to the MOSFETs.

♦ Record maximum substrate current at V_{DS} = 5.5V and maximum substrate current, I_{submax}, at the V_{DS} values which are applied for CHE stress. Record V_{GS} at which I_{submax}, associated with the applied V_{DS} occurs

After these measurements, the common procedure to apply channel hot electron injection stress is carried out by the following steps:

i) Measure the initial threshold voltage, V_{th0}, or the initial transconductance of MOSFET, g_{m0}.

ii) Apply CHE stress under a period of time, Δt, (in seconds).

iii) At intervals, stop CHE stress, and then measure the threshold voltage, V_{th}, or the transconductance of MOSFET, g_m. Calculate the difference between the initial V_{th0} or g_{m0} and just-measured V_{th} or g_m, respectively.

iv) A device lifetime is reached when ΔV_{th} = 50mV, or $\Delta g_m/g_{m0}$ = 10%.

Now, *one data point of I_{submax}/W versus lifetime is obtained.*

For a process, to plot a curve of lifetime vs. I_{submax}/W several MOSFETs are stressed at different values of I_{submax}. According to Eq. 2.8, the relation between the lifetime and the maximum substrate current density is linear. By extrapolation from the experimental plot, if the lifetime of an operational MOSFET (i.e., for Mitel 1.5 μm process, V_{DS}

= 5.5V) is greater than or equal to 10 years, then that process is qualified. Fig. 3.7 illustrates how to estimate the lifetime of a device working at an operational V_{DS}.

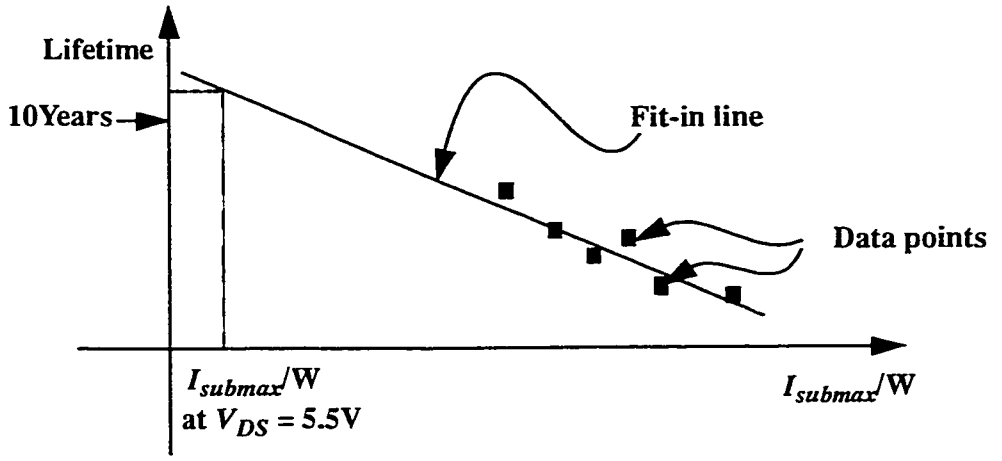


Fig. 3.7 - A typical plot of Lifetime vs. I_{submax}/W. The lifetime of a device working at operational V_{DS} is extrapolated from the fitted line.

All of the electrical measurements were done in standard laboratory conditions of $18^{o}C \leq T \leq 23\ ^{o}C$. For Fowler-Nordheim stress, 2 to 3 sites on each wafer were stressed at the same condition to check the reliabity of the test. For channel hot electron stress, the prior-stress tests were done on all devices under test in the same condition to check whether the results were repeatable. In reality, all fabricated samples on the same wafer display (almost) identical characteristics. The test results were also double-checked with experimental set-ups at Mitel. The check confirmed that both set-ups (at Mitel, and at Concordia University) produced the same results. Note that the equipment at Mitel is regularly calibrated every six months.

3.5 Overall Experimental And Electrical Characterization Strategy.

● Since the impact of any variation in a complete fabrication process can be both subtle and complex, first, a simpler pilot study is devised. Fluorine-ions are implanted into the gate oxide, and capacitors are tested by probing directly on the patterned poly (no full back-end metallization process needed). Both techniques, *j-t* and CCFN are used to study the effect of fluorine on gate oxides. The parameters of concern here are the changes in the bulk charges, D_{it}, after certain electrical stresses. These measurements serve to verify whether fluorination causes approximately the same effects in Mitel's 1.5 μm process as reported in literature. After the pilot study confirms the effects of fluorine in Mitel's 1.5 μm process, further intensive study is done on samples having the full Mitel's 1.5 μm process including the back-end metallization.

● Do Fowler-Nordheim hot carrier injection stress with positive gate bias on fluorinated samples. Analyze the obtained results. Based on the analysis, discussions about hole trap generation, electron trap generation, hole and electron charging rate, will be done. Because the tests under positive gate bias will disclose information about trapped charges generated within a tunneling distance from the Si/SiO_2 interface, discussion about charge at/near the Si/SiO_2 interface will be presented.

● Do Fowler-Nordheim hot carrier injection stress with negative gate bias on fluorinated samples. Analyze the obtained results. Based on the analysis, discussions about hole trap generation, electron trap generation, hole and electron charging rate, will be done. Because the negative gate bias will disclose the information of trapped charges gen-

erated within a tunneling distance from the poly-Si/SiO_2 interface, studies about charge at/near the poly-Si/SiO_2 interface will be conducted.

- Use the results of both (+) and (-) bias to discuss many effects of fluorination in the bulk, at/near the interface of Si/SiO_2, and at/near the interface of poly/SiO_2.

- Similarly, do Fowler-Nordheim hot carrier injection stress with positive gate bias on oxynitrided samples., and conduct similar analyses as described above for the fluorinated case.

- Similarly, do Fowler-Nordheim hot carrier injection stress with negative gate bias on oxynitrided samples. and conduct similar analyses as described above for the fluorinated case.

- Similarly, use the results of both (+) and (-) bias to discuss many effects of oxynitridation in the bulk, at/near the interface of Si/SiO_2, and at/near the interface of poly/SiO_2

- Compare results between fluorinated cases and oxynitrided cases.

- Do channel hot carrier injection stress on oxynitrided samples to further explore the impact of the oxynitridation technique.

3.6 Chapter 3 Contributions

A gate oxide characterization scheme was planned to study fluorinated and oxynitrided gate oxides. This scheme has been developed based on DiMaria's model of trapped

charge creation and the sensitivity of gate voltage during a Fowler-Nordheim stress. Note that while the scheme is developed here for the study of fluorination and oxynitridation, in practice the scheme could be applied to study any other kind of gate-oxides.

The discussion in Section 3.1 also emphasizes that the study of defects created in the negative gate bias FN stress is as important as those created under positive gate bias FN stress. The information obtained from both bias configurations could help the process engineer plan a good process, for example for E^2PROM fabrication.

Based on the charging curves obtained from ΔV_g, ΔV_{fb}, and ΔV_{fb}-ΔV_g, a graphical model was set up to estimate which oxide is more reliable where the net positive maxima are assumed to be located at the same location in the plots of $N_{\Delta Vg}$ vs. fluence. The model shows the physical meaning of the zero-crossing fluence, and the saturated interface charge values. Furthermore, the model emphasizes the importance of the charge created in the bulk, in addition to the more usual study of the Si/SiO_2 interface, in order to more fully understand oxide reliability.

To enhance the study of the trapping rate under a FN stress, an empirical equation (Eq. 3.3) was introduced. The rate of charge of the electron trapping rate with respect to fluence, K_1, is a novel parameter. By the use of this parameter, the transition between the net positive and net negative trapped charge (calculated from ΔV_g), can be better understood. Thus, K_1, can be used as an indicator to show how vulnerable an oxide is to the electron trap creation. Besides K_1, the induced charging rate at an injected charge of 1C/cm^2, K_2, was introduced as a parameter used to measure the saturated value of the induced electron charging rate (at high fluence).

The main contribution of this chapter is the development of this ensemble of techniques, all applied in a coherent manner to evaluate an oxide improvement process technique.

CHAPTER 4

SAMPLE PREPARATION AND PILOT STUDY

4.1 Sample Preparation

4.1.1 Chosen Techniques To Fabricate Fluorinated And Oxynitrided Oxides

Note that all samples in this project were fabricated in the 1.5 μm process at Mitel Corporation, Bromont, Quebec (see Appendix B for details on this process).

For fluorinated oxides, the technique employed is F-ion implantation into the poly-silicon gate, above the gate oxide. HF-last treatment prior to thermal oxidation is not chosen since we do not want to change Mitel's cleaning process. NF_3 gas treatment is not chosen for safety reasons. NF_3 is a very reactive gas, which can chemically react with H_2O for HF acid. In turn, HF will erode the thickness of any quartz furnace tube walls. Pre-oxidation F implant into Si, followed by gate oxidation is not chosen either, since the required implant energy is too high. The chosen technique is shallow F- ion implantation into the poly-silicon gate, followed by heat treatment to diffuse the F into the underlying gate oxide. This technique is also used because the change in overall device fabrication process

is minimal. In the Mitel 1.5 μm process, F-ion implantation is done after poly-Si deposition, and either before or after poly-Si patterning.

For oxynitrided oxides, the gas used is N_2O. NO is not used because of its toxicity. While NH_3 can be used to form oxynitrides, it introduces H atoms into SiO_2 film [38]. Thus, NH_3 is not a good candidate. N_2O is a good candidate which can be used to study oxynitridation.

4.1.2 Sample Preparation

4.1.2.1 Preparation of Fluorinated Samples

4.1.2.1.1 In-Situ MOS Capacitor Samples For Pilot Study

In order to study the effect of fluorination alone, without the potential complications caused by of the whole fabrication process, MOS Capacitor samples were prepared for a pilot study.

Lightly-doped (~ 10^{16} /cm^3), <100>, Czochralski-grown 2-4Ω-cm, N-type wafers were processed in a 1.5um standard CMOS process:

1) Pre-gate oxidation process.

2) Gate oxidation in dry O_2 to thickness of 265Å.

3) Gate in-situ doped polysilicon deposition.

4) Experimental F-implant [7](3 cases):

7. Using F ions seperated from BF_3

- Control Oxide (no implant)

- F-case-1: $6x10^{14}/cm^2$ @ 10Kev

- F-case-2: $2x10^{15}/cm^2$ @ 25Kev

5) Patterning of gate polysilicon by reactive ion etching.

6) F-cases are annealed at 900°C for 10 minutes. Most of the implanted fluorine is expected to diffuse into oxide [14-15], being located largely at the poly/SiO_2 and Si/SiO_2 interfaces after the anneal. The control oxide is not annealed.

7) Electrical characterization by probing directly on the poly gate. Gate capacitor areas used are $2.12x10^{-3}$ cm^2 and $4.02x10^{-4}$ cm^2.

4.1.2.1.2 Fluorinated Gate Oxides (Full Process)

Seventeen (17) wafers, phosphorous lightly-doped ($1.5x10^{15}$ cm^{-3}) <100> Czochralski grown 3 Ω-cm n-type, are used in this study. The wafers are dedicated to 17 experimental F-implant cases as follows:

- 1 Control oxide (no implant).

- 8 F-implant before poly-etch (families B -10 and B - 25).

- 8 F-implant after poly-etch (families A -10 and B - 25).

In a batch process, the wafers are subjected to front-end processing typical of a standard poly-gate CMOS process, as listed below:

1. Pre-gate oxidation process.

2. Gate oxidation in dry O_2 at 900°C to thickness of 265 Å.

3. Gate in-situ-doped polysilicon deposition to thickness of 3500 Å.

4. Experimental F-implants before poly-etch: (only families B -10 and B - 25 are implanted at this step).

- Family B-10, F-implanted at 10KeV with doses: $3x10^{14}$ /cm^2, $6x10^{14}$ /cm^2, $1x10^{15}$ /cm^2, and $2x10^{15}$ /cm^2
- Family B-25, F-implanted at 25KeV with doses: $6x10^{14}$ /cm^2, $1x10^{15}$ /cm^2, $2x10^{15}$ /cm^2, and $5x10^{15}$ /cm^2.

5. Patterning of gate polysilicon by reactive ion etching.

6. Experimental F-implants after poly-etch: (only families A-10 and A- 25 are implanted at this step).

- Family A-10, F-implanted at 10KeV with doses: $3x10^{14}$ /cm^2, $6x10^{14}$ /cm^2, $1x10^{15}$ /cm^2, and $2x10^{15}$ /cm^2.
- Family A-25, F-implanted at 25KeV with doses: $6x10^{14}$ /cm^2, $1x10^{15}$ /cm^2, $2x10^{15}$ /cm^2, and $5x10^{15}$ /cm^2.

7. All wafers are annealed at 900°C for 10 minutes in N_2. While the implanted fluorine is assumed to be predominantly within the poly gate before anneal, most of it is expected [14-15] to diffuse into the oxide, residing largely at the poly/SiO_2 and Si/SiO_2 interfaces, after the anneal. The control oxides are not annealed.

8. All 17 samples are then processed through the remainder of the 1.5μm standard process, including metallization.

9. Electrical characterization is done by probing on metal pads connected to the poly gate. The gate capacitor area used was 4.02×10^{-4} cm^2.

The reason for implanting in both cases, before and after poly-etch, is to study the effect of fluorine at the Si/SiO_2 interface. For a corresponding pair of before- and after-poly-etch samples (i.e same implantation dose, same implantation energy), we expect both of them to have same amount of fluorine in the bulk. However, by the lateral diffusion after F-ion implantation, the after poly-etch sample (in the corresponding pair) should have a higher amount of fluorine at or near the Si/SiO_2 interface by the capacitor perimeter.

4.1.2.2 Oxynitrided Samples

Five (5) <100> Czochralski-grown wafers, n-type phosphorus, 3 Ω-cm ($2x10^{15}$ cm^{-3}) are used in this study. In a batch process, the wafers are subjected to front-end processing typical of a standard poly-gate CMOS process. All gate oxide samples are grown at 900°C in pure dry O_2 and then are annealed at the same temperature for 20 minutes. After that, the wafers are separated into 4 cases, for experimental oxynitride formation. The oxynitridation time for all cases is 30 minutes in pure N_2O. The control wafers are simply annealed at 950°C in N_2 for 20 minutes. Below is the list of oxynitridation temperatures and corresponding oxide thicknesses.

⇨ Oxynitridation in N_2O:

- 1. At 850°C, final t_{ox}: 248 Å.
- 2. At 950°C, final t_{ox}: 250 Å.
- 3. At 1000°C, final t_{ox}: 265 Å.
- 4. At 1050°C, final t_{ox}: 268 Å.

Then the n^+ polysilicon gate is deposited by LPCVD. Then all wafers are subjected to the remainder of the standard 1.5 μm CMOS fabrication process including a post-metallization anneal at 425°C.

Electrical characterization of MOS capacitors is done by probing on metal pads connected to the poly gates. The gate capacitor area used is 4.02×10^{-4} cm^2.

In addition, nMOSFETs are fabricated with lightly-doped drain (LDD) and source structures. Channel widths in these devices are either 1.5μm or 50μm. The channel length of the wide devices (W = 50μm) is 1.5μm, while the channel length in narrow devices is varied from 1.5μm to 0.8μm.

4.2 In-situ Study Of Electrical Characterization Of Fluorine-implanted Gate Oxide Structures.

This section of the work aims to study the effects of fluorination on gate oxide before the samples were subjected to any post-poly-etch processes. It also aims to expand the study of the electrical properties of fluorinated gate oxides, by an approach combining both C-V analysis and *j-t* analysis. Both techniques, *j-t* and CCFN are used to study the effect of fluorine on gate oxides. The parameters of concern here are the changes in the bulk charges, D_{it}, after certain electrical stresses. These measurements serve to verify whether fluorination causes approximately the same effects in Mitel's 1.5 μm process as reported in the literature.

In this experiment the samples were fabricated as mentioned in section 4.1.2.1.1. The experimental F-implant cases are:

(i) Control oxide (no implant)

(ii) F-case-1: $6x10^{14}$ cm^{-2} at 10 keV, and

(iii) F-case-2: $2x10^{15}$ cm^{-2} at 25 keV (this case was chosen to be compatible with typical fluorine implant doses and energies [9, 14]).

Thus after the subsequent poly etch and anneal, the samples are not sent through the remainder of the process, but are subjected to electrical reliability stressing by two Fowler-Nordheim tunneling injection stress methods: constant current stress, and constant-voltage stress (*j-t* analysis [43]). The trends of evolution of flatband voltage (V_{fb}), midgap interface state density (D_{it}), and oxide trapped charge (Q_{ot}) are found, before and after such electrical stresses.

4.2.1 Measurement Procedures

Since the fabrication process stops at the step of poly etch, there is no metal pad to make the contact. However, for the n-type substrate, the front contact for a capacitor-characterization can be made by probing directly on the poly, while the back-contact comes from the substrate (which is connected to the chuck of the hot plate). Fig 4.1 shows the structure of an in-situ fluorinated capacitor, and how the electrodes (a probe and a hot-chuck) are connected to the structure.

4.2.1.1 C-V Measurements

Automated high frequency (HF) C-V (1MHz, -5 to +5V) and low frequency (LF) C-V (-5 to +5V, 200 mV/s sweep, 0.1 pF minimum resolution) measurements were done using a probe station enclosed in a dark shielded box. Such HF and LF measurements were performed at various times during the experiments, including before and after constant-current density stressing, and before and after *j-t* stressing, as described below.

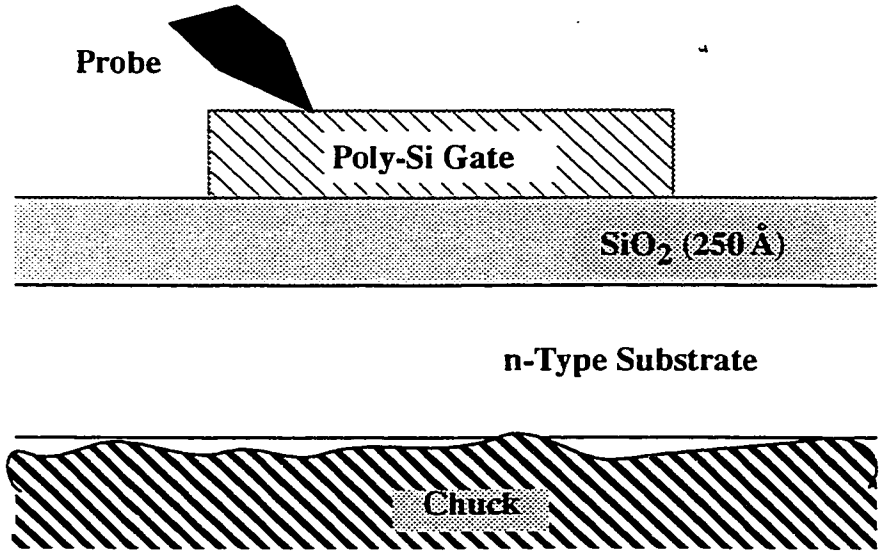
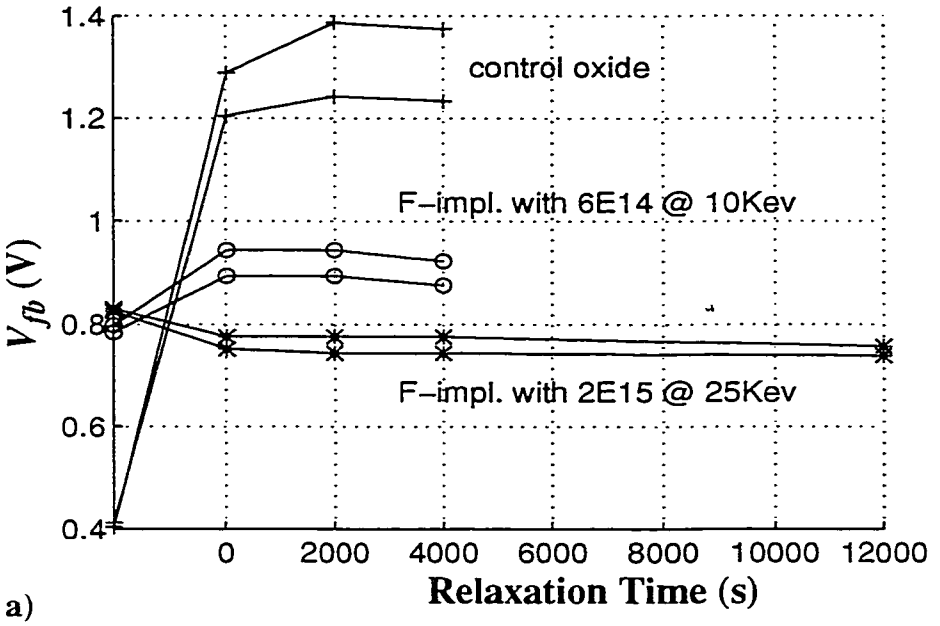


Fig. 4.1 - Structure of a MOS capacitor for in situ study. For a constant current stress, a current source is connected to the probe. For a constant voltage stress, a voltage source is connected to the probe. Note the surface of the chuck is rough.

4.2.1.2 Constant Current Density Tunnelling Stress

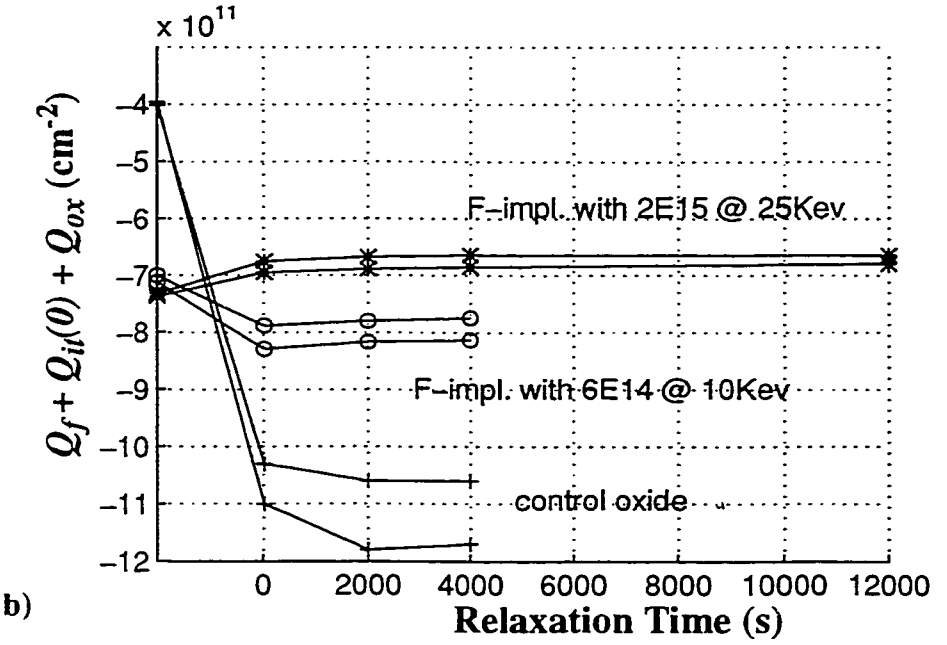
A constant DC current density was applied to the gate, using a Keithley SMU-based system, and the same probe station and cabling setup as used for the C-V measurements described above. After a constant current density of 2.36×10^{-4} A/cm^2 for 200sec (the applied voltage was >20V), the stressing current was terminated, and C-V analysis

was immediately (within 5 s) performed as described above. C-V analysis was subsequently repeated after further time intervals of 2000, 4000, and for one case, 12000 s. There was no stressing in between the subsequent measurements. Thus these measurements trace the time evolution of oxide properties after the release of a single 200s stress. Each complete set of HF and LF CV measurements took ~1440s, and the time delays include that required for the C-V measurements. The results of this sequence are shown in Figs. 4.2(a)- 4.2(c).



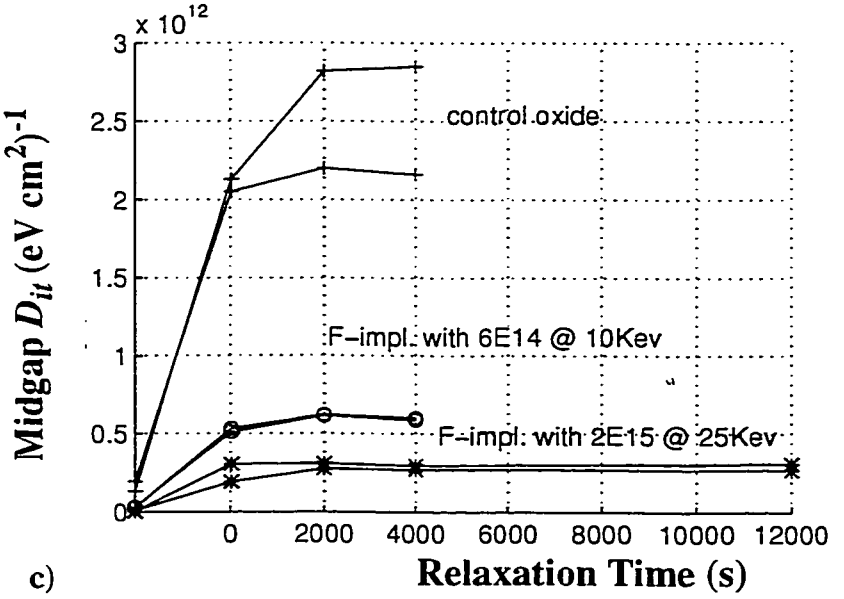
a)

Fig. 4.2 - (a) V_{fb}, vs. time after release of FN stress at 2.36 x10^{-4} A/cm^2 for 200s (fluence = 0.0472 C/cm^2). The values at the vertical axis were measured before any electrical stress.



b)

Fig. 4.2 - (b) Calculated ($Q_f + Q_{it}(0) + Q_{ox}$) vs. time after release of FN stress at 2.36 x10^{-4} A/cm^2 for 200s (fluence = 0.0472 C/cm^2). The values at the vertical axis were measured before any electrical stress.



c)

Fig. 4.2 - (c) Midgap D_{it} vs. time after release of FN stress at 2.36 x10^{-4} A/cm^2 for 200s (fluence = 0.0472 C/cm^2). The values at the vertical axis were measured before any electrical stress.

4.2.1.3 *j-t* Stress

This test was accomplished using a HP4145A parameter analyzer, with positive voltage applied to the poly gate. Fig. 4.3 presents a sample *j-t* curve, showing the evolution of the current density with stressing time. Such *j-t* data set are then transformed [43] to calculate normalized current density vs. injected charge (fluence). Normalized current density is computed as the ratio of *J(t)/ J(t=0)*. Then based on Eqs. 2.5 & 2.6, oxide trapped charge density, Q_{ot}, more than a tunnelling distance away from the injecting electrode, is computed from normalized current density and plotted vs. fluence. Examples of Q_{ot} vs. fluence can be seen in Fig. 4.4.

The *j-t* technique was used in conjunction with C-V analysis to understand the post-stress behavior of the control and fluorinated oxides.

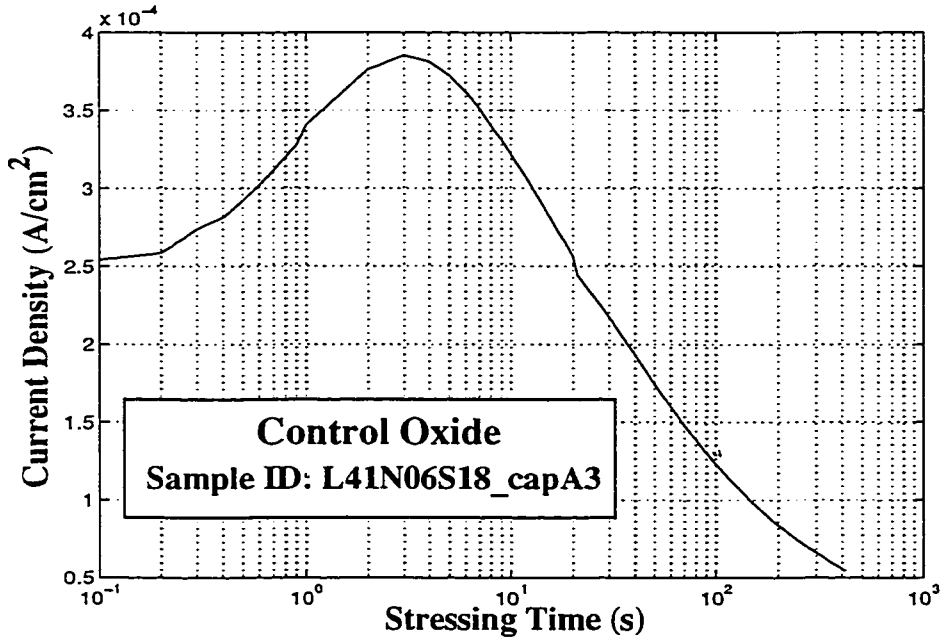


Fig. 4.3 - Current density injected through MOS gate vs. stressing time. The sample used was the control oxide and the stressing field was 8.87 MV/cm.

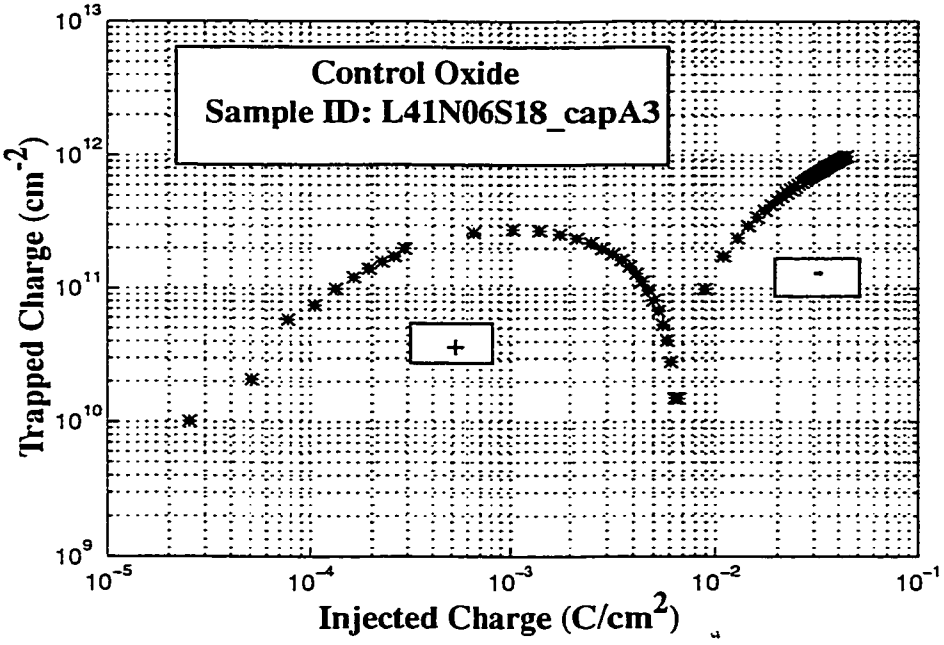


Fig. 4.4 - Calculated trapped charge vs. injected charge (fluence). The part of the curve to the left of 6.2×10^{-2} C/cm^2 indicates net positive trapped charge, while the part to the right indicates net negative trapped charge.

4.2.2 Results And Discussion

Figs. 4.2(a) and 4.2(b) show the evolution of V_{fb} and $(Q_f + Q_{it}(0) + Q_{ox})$ calculated from HF C-V measurements, before and after constant current stress. Before the stress, the fluorinated cases show more significant levels of oxide charge than the control oxide, (and therefore larger offset of V_{fb} from ideal values). However, after stress the control oxide showed very large shifts, (~6-7x10^{11} cm^{-2}) indicating a significant reliability hazard. The fluorinated cases, on the other hand, show much smaller shifts (<1.5x 10^{11} cm^{-2}). This is accord with the findings of [9, 10, 15, 25, 23]. Likewise in Fig. 4.2(c), the evolution of midgap D_{it}, calculated from HF C-V and LF C-V data demonstrates similar trends. The

fluorinated cases are more resistant to the constant-current stress as compared to the control case.

The results found are in accord with the usual findings [15, 25, 23] that such fluorination treatments are effective in improving MOS gate capacitor reliability. For example, for 250Å oxides, at 0.05 C/cm^2, Nishioka *et al* [9] found that midgap D_{it} for fluorinated oxide shifted by ~ $2x10^{11}$ eV^{-1} cm^{-2}, while the control oxide shifted by ~$7x10^{11}$ eV^{-1} cm^{-2} for a dose equivalent to the F-case-2. Similarly, for 130Å oxides, at 0.1 C/cm^2, Wright *et al* [15] found that midgap D_{it} for a fluorinated case shifted by ~$2.5x10^{11}$ eV^{-1} cm^{-2}.

However, the above stress tests at constant-current density only consider the oxide properties after application of one specific value of fluence, and thus may miss more complex behavior during evolution of that state. Furthermore, C-V analysis is affected by all of the charge defects throughout the thickness of the oxide, including those at the Si/SiO_2 interface. *j-t* analysis, on the other hand, is sensitive only to charge defects in the bulk oxide more than a tunneling distance away from the cathode, in this case is the Si/SiO_2 interface [43]. Indeed, a very powerful aspect of this technique is that it clearly shows the evolution of trapped charge in the bulk oxide, as a function of injected charge. Therefore, combination of C-V analysis with *j-t* analysis can provide a much more comprehensive assessment of MOS gate capacitor reliability.

Q_{ot} vs. fluence present (for example, consider the control sample in Fig. 4.4) several stages, representing different physical phenomena [43, 76]:

i) an initial increase in trapped positive charge due to impact ionization,

ii) the attainment of a maximum net positive trapped charge (at about $1x10^{-3}$ C/ cm^2 in Fig.4.4),

iii) a shift from net positive to net negative trapped charge attained at ~$6.2x10^{-3}$ C/ cm^2 (in Fig.4.4) as electron trap creation becomes dominant,

iv) increasing net negative trapped charge, which usually continues [43, 44, 76, 83] to increase until breakdown, and

v) charge breakdown.

While this particular curve was terminated before breakdown in order to perform post-stress C-V analysis, the test can readily be run until the catastrophic breakdown. Such catastrophic breakdown can occur in any regime (i)-(iv). While this describe the typical overall shape of oxide trapped charge, Q_{ot}, vs. fluence curves, the fluence levels at which phenomena (ii) and (ii) occur, and the maximum Q_{ot} level in stage (ii), all can vary dramatically depending on the quality of the dielectric.

Careful *j-t* tests were performed on the three cases, choosing the applied field such that the average current over the stressing duration would be as close as possible to the CCFN stress used in Figs. 4.2(a)- 4.2(c). The results for a fluence of 0.047C/cm^2, (same as the FN stressing fluence used in Figs. 4.2(a) - 4.2(c)) are summarized in Fig. 4.5 and Table 4.1.

First of all, the results shown in Fig. 4.2(b) and Fig. 4.5 agree with each other under the introduced electron trap mechanism (discussed in Section 2.1.2.1). Under the electron trap mechanism, the creation of electron traps is related to the existence of hydro-

gen at the SiO_2 interface [43, 44]. However, as we have discussed in Section 2.2.1.4, the incorporation of fluorine into gate oxides has replaced the chemical bond SiH by SiF, believed to require higher energy to be broken. The fluorination, therefore, reduces the creation of electron traps in the gate oxide. In Fig. 4.2(b), the obtained data support this idea, and also show a systematic tendency that, the more fluorine incorporated into the gate oxide, the fewer electrons are trapped by the constant current density Fowler-Nordheim (FN) stress. Fig. 4.5 further clarifies that under FN stress, during the evolution of trap creation, the trend is: while *the impact ionization may be unaffected (or only slightly affected) by the existence of hydrogen, the replacement of hydrogen atoms by fluorine atoms has dramatically suppressed the electron trap creation.*

A companion series of *j-t* tests was done at different stressing fields near to the chosen applied field. In each case, Q_{ot} at a fluence of 0.047C/cm^2 was found to be relatively insensitive to small variations in stressing field. The trapped charge densities at this level of fluence can be roughly compared with the changes in oxide charge shown in Fig. 4.2(b). The control oxide in both tests has the most significant net negative charge density. F-case-2 in both tests has the highest net positive charge density. In this way the two tests give relatively consistent judgements. The differences between the results of the two tests in Table 4.1 may potentially be explained by the presence of significant levels of charge within the tunneling length of the Si/SiO_2 interface (to which Q_{ot} is not sensitive). However, it should be noted that in the control case the difference is positive, while in F-case-1 and F-case-2 this difference is negative.

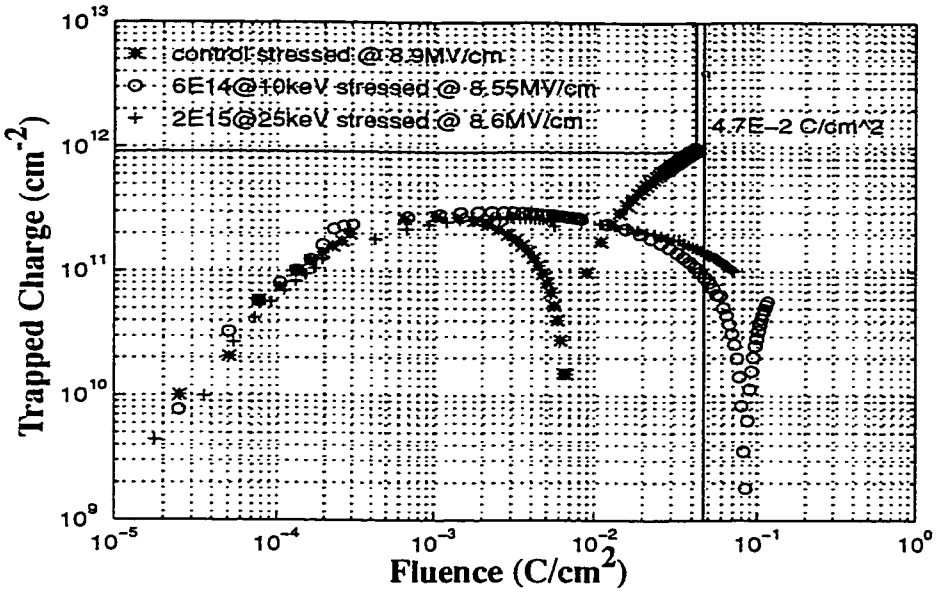


Fig. 4.5 - Trapped Charge vs. fluence for the three cases studied. The vertical line indicates a fluence of 0.047 C/cm^2.

Assuming that the value of Q_f is constant then most of the difference between the results of the two tests comes from $Q_{it}(0)$. In accord with Roh *et al* [55], and the findings of this thesis [78], the charge component (under positive gate bias) of the interface states is negative. Consequently, this explains how there is a negative difference for the fluorinated cases as shown in Table 4.1.

Gate Oxide Case	Average applied field (MV/cm)	Trapped Charge, Q_{ot} (/cm^2)	$\Delta(Q_f + Q_{it}(0) + Q_{ox})$ (see Fig. 4.2(b)) (/cm^2)
Control oxide	8.90	-1.0x10^{12}	-6.70x10^{11}
F-case-1: 6x10^{14}@10keV	8.55	+6.5x10^{10}	-1.03x10^{11}
F-case-2: 2x10^{15}@25keV	8.60	+1.4x10^{11}	+4.95x10^{10}

Table. 4.1 - Trapped charge from *j-t* analysis at a fluence of 0.047C/cm^2 and $\Delta(Q_f + Q_{it}(0) + Q_{ox})$ from CV measurement.

However, to explain the positive difference in the control case, another type of trapped charge should be taken into account: anomalous positive charge, APC. These anomalous charges are also called slow states since their existence can only observed at high fluence. APC behaves like a donor [48], is located near/at the Si/SiO_2 interface [48, 55], alternatively charges and discharges, and after a number of charge reversal the effect is damped. This damping phenomena is dependent on the temperature: the higher the temperature, the larger the damping effects is [55]. Regarding the variation of oxide parameters V_{fb} and D_{it} after the release of stress shown in Fig. 4.2(a) and Fig. 4.2(c), this is not the first time such phenomena have been observed. Roh *et al* [55] observed V_{fb} oscillatory behavior with magnitudes of ~4V and of ~ 1.75V associated with a period of 7500s, after FN stress at 4.4 $\mu A/ cm^2$, fluence = $0.13C/cm^2$. The post-stress voltage shifts and rates of shift observed in this work are smaller than those reported in [55], but they may stem from similar physical phenomena. Another piece of evidence to confirm that what is observed is APC, is that the oscillation is also obtained from D_{it} (see Fig. 4.2(c)). This information indicates that the anomalous charge, appearing in control samples, is actually located at / near the Si/SiO_2 interface. The anomalous charge has been observed in the control oxide (stressed at ~8.9 MV/cm, up to a fluence of $0.047\ C/cm^2$), while there is no such observation in the fluorinated cases.

Since oxide trapped charge varies in a complex manner as a function of oxide properties and applied fluence, simple FN stress at a single fluence level could yield misleading results [76]. To illustrate, Fig. 4.6 presents Q_{ot} vs. fluence for both control and fluorinated cases. In these *j-t* tests, the applied field was kept constant at 8MV/cm for all the three cases, and the stresses were terminated, before breakdown, near a fluence of 1.6 x

10^{-3} C/cm^2. The last Q_{ot} value for the control oxide reflected a net negative trapped charge of 5.9x10^9 C/cm^2. HF C-V measurements were performed immediately after termination of the stresses, and the results are tabulated in Table 4.2. The C-V results are quite different from those shown in Figs. 4.2. If one had simply applied a simple FN stress to approximately 1.4-1.6 x10^{-3} C/cm^2, instead of 0.047 C/cm^2, and at 8MV/cm instead of ~8.6-8.9MV/cm, one could have arrived at an entirely different conclusion about the reliability of the three cases. Indeed one could have erroneously concluded that the control oxide was the most reliable, since its ΔV_{fb} was by far the smallest.

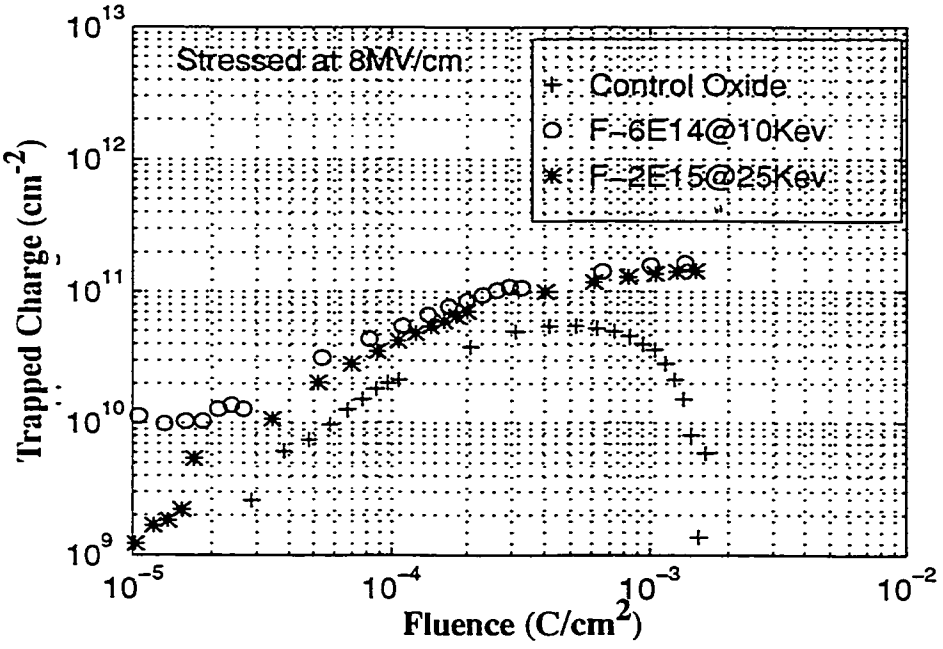


Fig. 4.6 - Trapped charge vs. fluence. For all three cases, the applied field was 8 MV/cm. Stresses were terminated as the fluence reached approx. 1.6x10^{-3} C/cm^2. The final value of Q_{of} for the control oxide is at 5.9x10^9 C/cm^2, rising after the minimum at 1.4x10^9 C/cm^2, indicating net negative trapped charge.

Gate Oxide Case	Fluence (C/cm2)	Before Stress (V)	After stress (V)	ΔV_{fb} (V)	$\Delta(Q_f + Q_{it}(0) + Q_{ox})$ (/cm^2)	Q_{ot} (/cm2)
Control oxide	$1.6\text{x}10^{-3}$	0.412	0.431	+0.019	$-1.55\text{x}10^{10}$	$-5.92\text{x}10^{9}$
F-case-1: $6\text{x}10^{14}$@10keV	$1.4\text{x}10^{-3}$	0.798	0.611	-0.187	$+1.52\text{x}10^{11}$	$+1.65\text{x}10^{11}$
F-case-2: $2\text{x}10^{15}$@25keV	$1.5\text{x}10^{-3}$	0.832	0.672	-0.160	$+1.30\text{x}10^{11}$	$+1.44\text{x}10^{11}$

Table. 4.2 - V_{fb}, ΔV_{fb}, $\Delta(Q_f + Q_{it}(0) + Q_{ox})$ obtained from HF CV, and Q_{ot} obtained from *j-t* measurements, all were measured at a after a fluence ~$1.5\text{x}10^{-3}$ C/cm^2.

In Table 4.2, since comparison between $\Delta(Q_f + Q_{it}(0) + Q_{ox})$, and Q_{ot} shows a consistent negative difference, this suggests that there exists no APC in the three oxide cases. Therefore, if an applied electric field of 8MV/cm is simply chosen to do FN stress, one can also not observe the effect of fluorination on the aspects of formation of anomalous charge.

These measurements, both constant current density and *j-t* stress, form a sufficiently consistent picture to address oxide reliability for the three cases studied here. As suggested by DiMaria *et al* [16, 43, 44], the evaluation of oxide reliability is a complex concern, depending on applied field and applied fluence. At low fluence, the fluorinated cases are *more* affected by impact ionization, as seen in Fig. 4.6, because the curves for F-case-1 and F-case-2 rise earlier than the curve for the control oxide. So in this low fluence regime (< $2\text{x}10^{-4}$ C/cm^2), the control oxide would have a lower shift in V_{fb}. At high fluence, on the other hand, the fluorinated oxides are found to be *less* affected by trap creation, since stages (iii) and (iv) of the curve appear to be attained at much higher fluences

than in the control oxide. The control oxide has a much earlier onset of trap creation (step (ii) and (iii)). Therefore, in the high fluence regime, the control oxide has higher shift in flatband (see Fig. 4.2a). Similarly, as seen in Fig. 4.5, the curve for F-case-2 (after Q_{ot} maximum) falls more slowly than that for F-case-1. This indicates that F-case-2 is more resistant to electron trap creation than F-case-1. All of these observations are consistent with the reported data in Section 2.2.1.3, and with the discussions about the role of fluorine in Section 2.2.1.4. In these sections, for the replacement of SiH by SiF and fluorine atoms filling as-deposited dangling bonds, fluorination enhances the resistance of gate oxide to electron trap generation.

As gate oxides become thinner and thinner, impact ionization becomes less and less important [43, 44], suggesting that electron trap creation at high fluence becomes relatively more and more important. Since fluorinated oxides are found to be more resistant to such electron trap creation, this suggests that fluorinated oxides offer the likelihood of better reliability for future CMOS technologies.

Furthermore, as discussed, the fluorinated cases have also, at least, reduced (if not suppressed) the creation of anomalous positive charge. This type of charge has a behavior of charging and discharging (unexplainable [55]), this adds more complexity in the scenario of charge components created under FN stress. APC is commonly believed to cause deleterious effects [55] in the reliability of gate structures. Thus by reducing APC defects, fluorination has improved the performance of gate oxides.

4.2.3 Conclusions

4.2.3.1 Reliability of In-Situ Fluorine Implanted Samples

In-situ fluorine-implanted gate oxide structures (two different doses and implant energies) were electrical characterized along with in-situ unimplanted controls. The usual device reliability indicators of Q_f, ΔV_{fb}, and midgap D_{it} are found to be improved, as compared to unimplanted controls. The fluorinated cases are found to be more resistant to constant-current Fowler-Nordheim stress as compared to the control case. Accordingly, *j-t* analysis corroborates that the fluorine cases exhibit improved-reliability over the control structures. The following are the key aspects which show that in-situ fluorine-implanted samples have more reliable performance:

- Fluorination reduces electron trap creation in gate oxide.

- Fluorination reduces or suppresses the creation of anomalous charges, which usually appear at high fluence.

- Fluorination shows more reliable performance in such usual measures as: ΔV_{fb}, ΔD_{it}, ΔQ_f or Q_{ot}.

4.2.3.2 The Combination of C-V And *j-t* Analysis

While the results of constant current tunnelling stress are found to be relatively consistent with the *j-t* analysis in this study, the combination of C-V and *j-t* analysis is found to offer a more comprehensive view of complex oxide variations, and is found to be more useful for the study not only of fluorinated oxides but any forming oxides.

The use of the combination of C-V and *j-t* measurements proved that a simple FN stress (apply a constant current or voltage on the gate at a specific time, then measure ΔV_{fb}, ΔD_{it}, etc....) can lead to mistaken conclusions about oxide reliability. Note that, at the time [75, 76] were published, simple FN stress was still used in industry and research laboratories to roughly test the reliability of novel processes.

The combination of C-V and *j-t* analysis also opens a new view to show that the mechanism of charge component generation in gate oxide under FN stress is more complicated. This combination offers also a tool to study charge at different locations in the gate oxide. For example, in this study, from Tables 4.1 and 4.2., the differences between two columns of $\Delta(Q_f + Q_{it}(0) + Q_{ox})$ and Q_{ot}, roughly give quantitative information about anomalous charges and areal charges trapped within a tunneling distance from the Si/SiO_2 interface.

4.2.4 Chapter 4 Contributions

- A combination of *j-t* and C-V techniques is used to characterize the quality of fluorinated and control oxides. The scenario of charge components induced by Fowler Nordheim stress is demonstrated to be quite complex.

- A simple FN stress test can lead to false-conclusions regarding the oxide reliability. Thus, for more accurate analysis, a more comprehensive plan must be enacted to characterize any oxide.

- The measurements of D_{it}, ΔV_{fb} verify that fluorine incorporation into gate oxides improves the oxide quality similarly to reports in the literature [9, 12-15].

- By the use of the *j-t* technique, the analysis shows that the electron trapped charges generated in the bulk are reduced when the fluorination process is employed.

- Comparison between Q_{ot} (calculated from *j-t* techniques) and $\Delta(Q_f + Q_{it}(0) + Q_{ox})$ (from C-V measurement) suggests that fluorination reduces or suppresses the creation of anomalous positive charge.

CHAPTER 5

FLUORINATION IN GATE OXIDES CHARACTERIZED BY FOWLER-NORDHEIM TUNNELLING INJECTION STRESS

5.1 Effects of Fluorine Implants on Induced Charge Components in Gate-Oxides Under Positive Gate Bias Constant-Current Fowler-Nordheim Stress.

The devices in this study were fabricated as described in Section 4.1.2.1.2. Note that the thickness of the oxides is 265Å, while the poly-thickness is 3500Å (see Appendix B). These values are near or the same as the values reported in Refs. [9, 14], thus there are good reasons to believe that the investigated oxides would have depth profiles similar to SIMS profiles reported in Fig. 2.6.

While in Chapter 6, the pilot in-situ study is reported, in this chapter, fluorination is studied more extensively according to the strategies outlined in Chapter 4.

Like previous studies, fluorinated gate oxides prove to have better performance in the aspects of overall flatband voltage shifts and interface trapped charge density. However, these advantages result from more complex combinations of effects. In this study,

comparisons of induced charging components between fluorinated and control gate oxides expose complicated variations of trapped charge generation in bulk and interface regions.

5.1.1 Measured And Calculated Results

In our experiments, C-V measurements are executed by using a probe station enclosed in a dark shielded box with automated high-frequency C-V (HF) (1MHz, -5V to +5V) and low-frequency C-V (LF) (-5V to +5V, 100mV/sec sweep, 0.1 pF minimum resolution). The values of flatband voltages were recorded via high frequency C-V measurements. From combined HF and LF C-V measurements, interface trap densities versus energy in the silicon bandgap, (D_{it} curves) are obtained.

To apply (+) CCFN injection stress, a constant current density was applied to the gate of the n-MOS capacitor-structure by using a HP4145, and the same probe station and cabling as was used for the C-V measurements described above. Via the HP4145 SMU-based system, gate voltages were recorded as a function of stressing time (t). A constant current of 95.4 nA was injected into the gate. This is equivalent to a constant current density of 2.36×10^{-4} A/cm^2. This was also the value employed in the previous in-situ fluorination study [76]. The associated electric field causing the injected current density was in the ranges of 8.5 to 8.7 MV/cm.

5.1.1.1 D_{it} Curves

Fig. 5.1(a) shows a typical distribution of interface traps across the bandgap of Si before any applied electrical stress, for implant family B-25. Near midgap, where these calculated results are most reliable, it is clear that the trap densities in the F-implanted

cases are generally below those of the control case. The higher the implant dose, the lower the density of interface traps at midgap. Figs. 5.1(b) and 7.1(c) present D_{it} vs. bandgap energy after certain injected fluences. The intermediate fluence, 0.07 C/cm^2, appears to have caused $\geq 10^{12}$ eV^{-1} cm^{-2} interface traps in each case in the family B-25. As in Fig. 5.1(a), the control oxide exhibits higher D_{it} than the F-implanted cases. At the very high fluence of 0.22 C/cm^2, however, the control oxide appears to have incurred more interface traps, while the F-implanted cases have not changed much since Fig. 5.1(b).

These D_{it} results are in general accord with the trends reported by previous researchers:

- The F-implanted cases have lower (better) pre-stress D_{it} than the control case [14-15, 26].

- While both control and F-implanted cases degrade to $>10^{12}$ /cm^2, after a high fluence of injected charge, the control oxide exhibits more degradation than the F-implanted cases [14-15, 26].

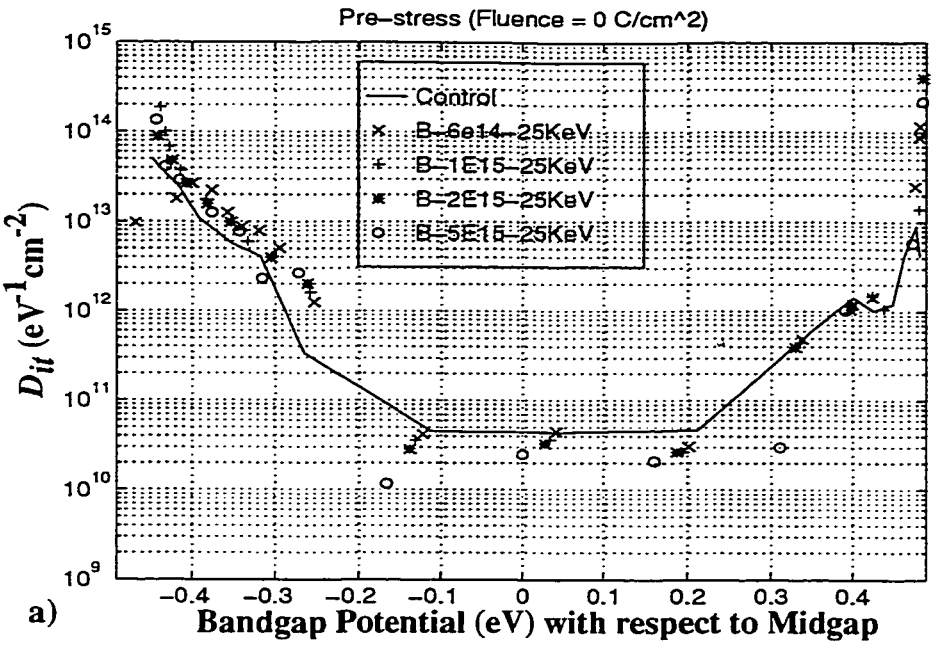


Fig. 5.1 - (a) Interface trap density measured vs. silicon band gap energy for family B-25 and for the control oxide Before the constant current Fowler-Nordheim stress.

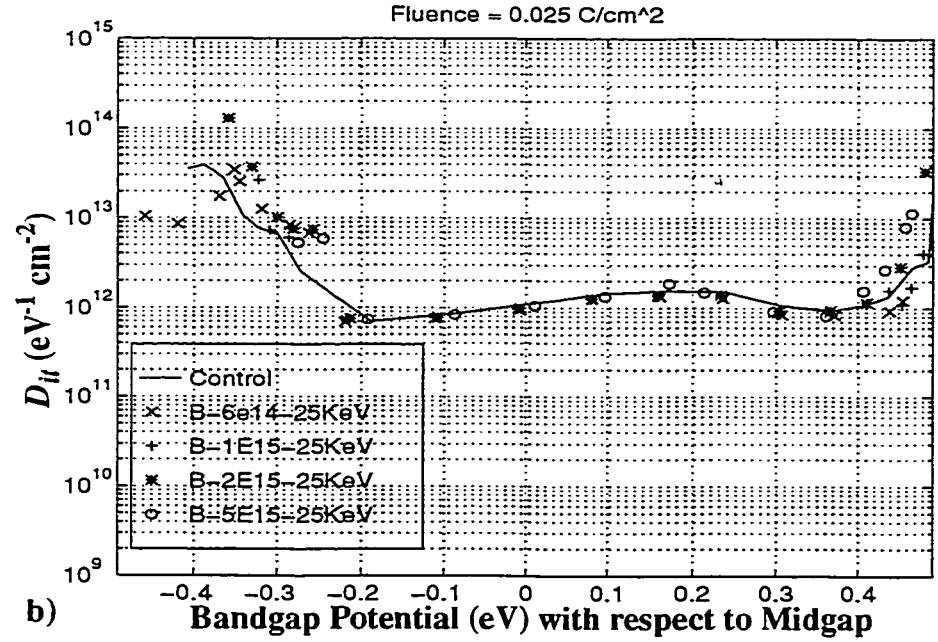


Fig. 5.1 - (b)Interface trap density measured vs. silicon band gap energy for family B-25 and for the control oxide after an injection of hot electrons to a fluence of 0.025 C/ cm^2.

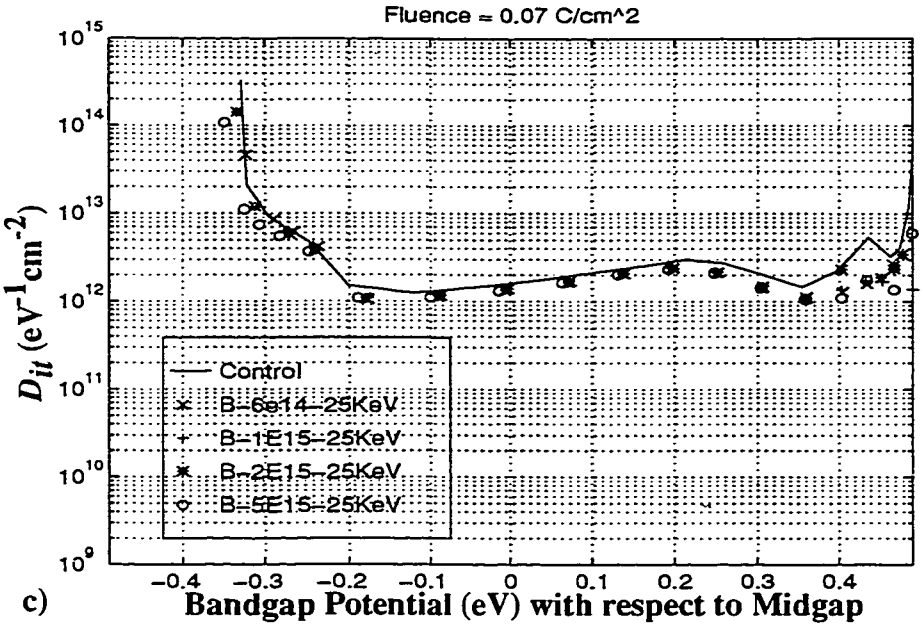


Fig. 5.1 - (c) Interface trap density measured vs. silicon band gap energy for family B-25 and for the control oxide after an injection of hot electrons to a fluence of 0.07 C/cm^2.

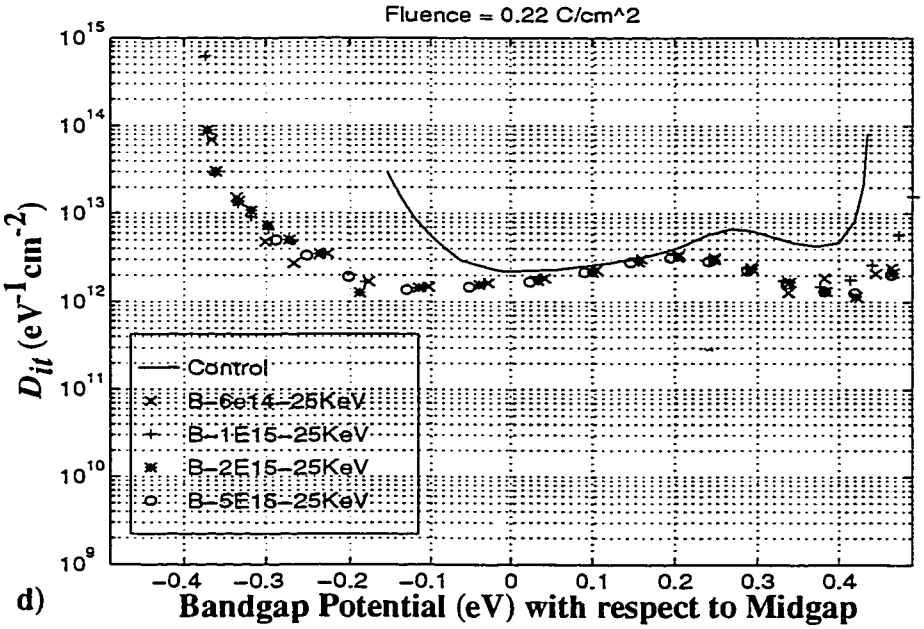


Fig. 5.1 - (d) Interface trap density measured vs. silicon band gap energy for family B-25 and for the control oxide after an injection of hot electrons to a fluence of 0.22 C/cm^2.

5.1.1.2 Flatband Voltage Shift, ΔV_{fb}

Figs. 5.2 show examples of the evolution of ΔV_{fb} for the four fluorinated families (and the control oxide), during a (+) CCFN stress. The constant current density was 2.36×10^{-4} A/cm^2. The ΔV_{fb} measurements were done at various intervals up to a total injected charge of 0.22 C/cm^2. For the all fluorinated families (B-10K, A-10K, B-25K, and A-25K), Figs. 5.2 (a), (b), (c), (d) show that while at low fluence (less than about 3×10^{-2} C/cm^2), it is difficult to distinguish the F-implanted cases from the control case, at high fluence the F-implanted cases exhibit noticeably lower ΔV_{fb}. The highest F-doses yield the lowest ΔV_{fb} in all of the fluorinated families.

Fig. 5.3 summarizes ΔV_{fb} for all families at a particular high fluence level, 0.1 C/cm^2. It can be seen that at this high fluence all of the F-implanted cases have lower ΔV_{fb} than the control oxide. Also, there is a rough trend that in general the higher doses give lower ΔV_{fb}. Figs. 5.2, 5.3 are again in general accord with the results of other researchers [14-15, 64].

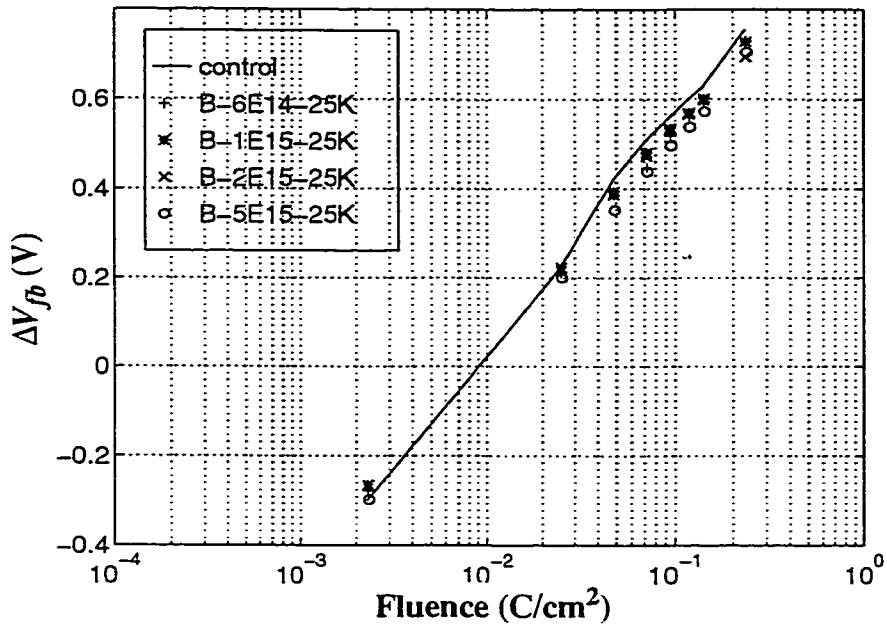


Fig. 5.2 - (a) Flatband voltage shifts, ΔV_{fb} vs. fluence of hot electrons injected from substrate. Control oxide ΔV_{fb} curve is included for comparison. Fluorinated oxides were implanted at 25KeV before poly -etch.

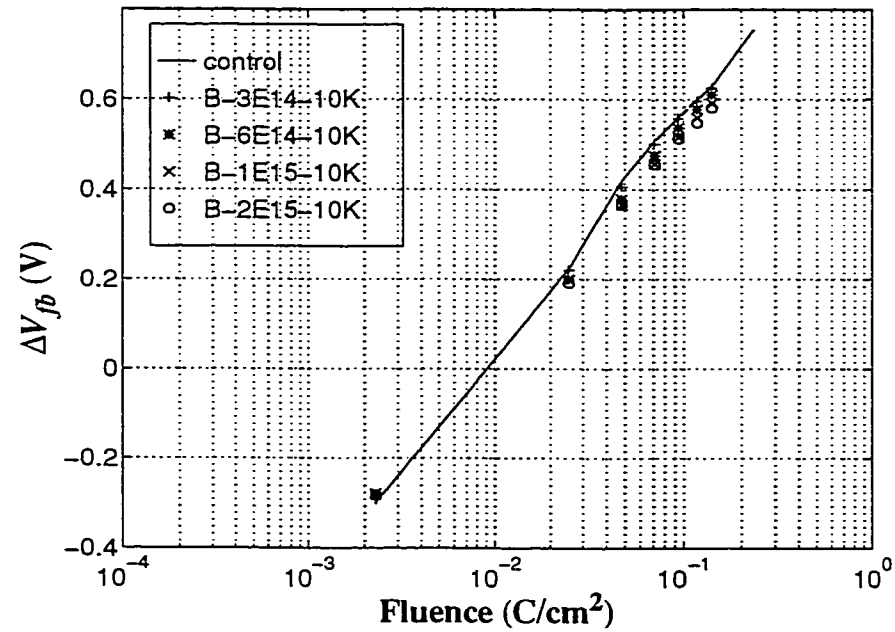


Fig. 5.2 - (b) Flatband voltage shifts, ΔV_{fb} vs. fluence of hot electrons injected from substrate. Control oxide ΔV_{fb} curve is included for comparison. Fluorinated oxides were implanted at 10KeV before poly -etch.

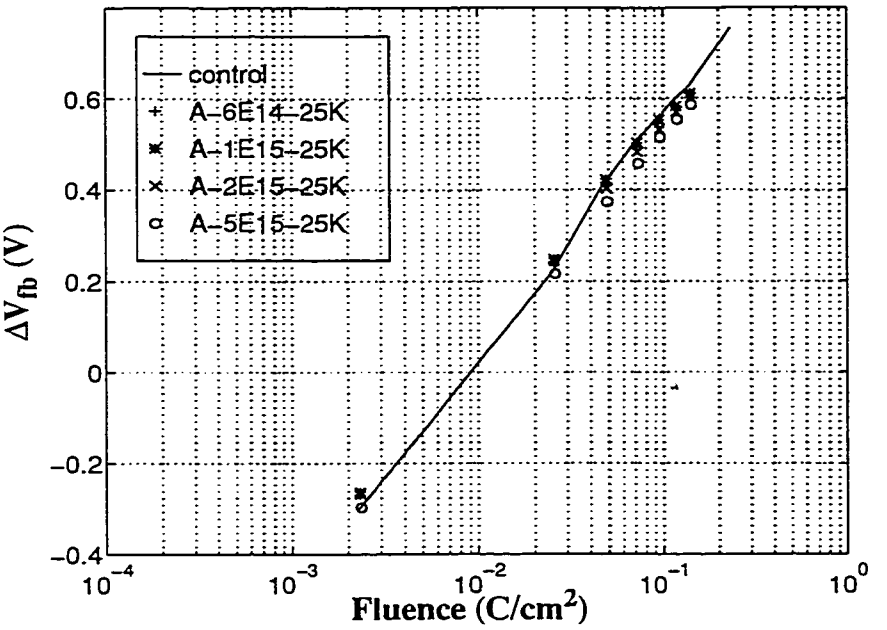


Fig. 5.2 - (c) Flatband voltage shifts, ΔV_{fb} vs. fluence of hot electrons injected from substrate. Control oxide ΔV_{fb} curve is included for comparison. Fluorinated oxides were implanted at 25KeV after poly -etch.

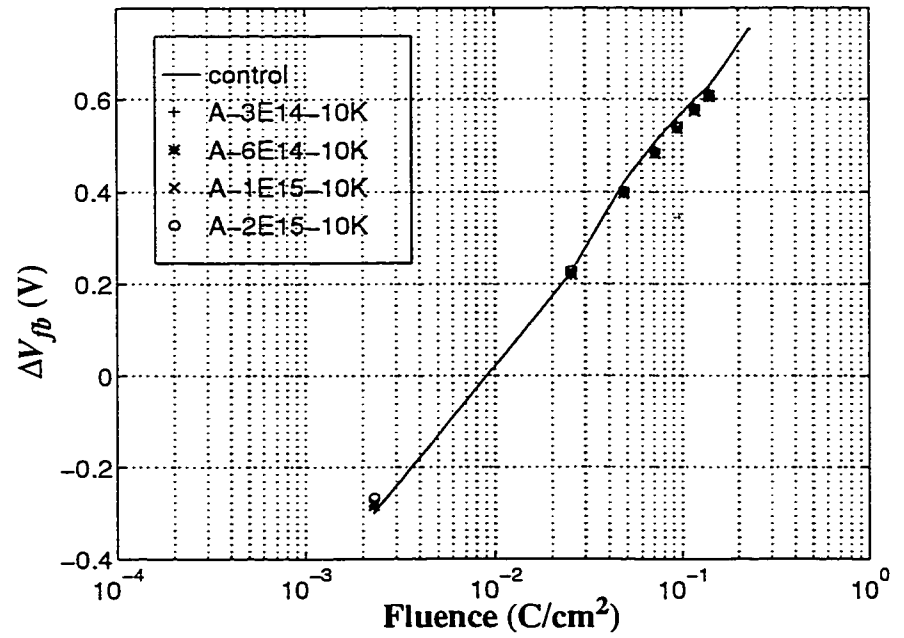


Fig. 5.2 - (d) Flatband voltage shifts, ΔV_{fb} vs. fluence of hot electrons injected from substrate. Control oxide ΔV_{fb} curve is included for comparison. Fluorinated oxides were implanted at 10KeV after poly-etch

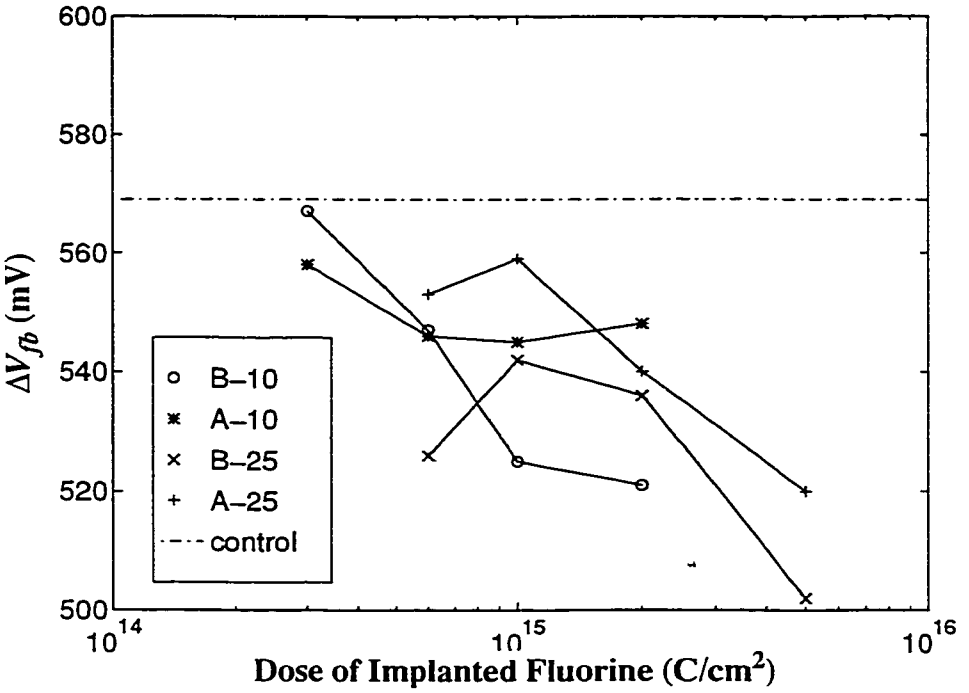


Fig. 5.3 - Flatband voltage shifts vs. F-dose for all samples studied, measured at 0.1 C/cm^2.

5.1.1.3 Gate Voltage Shift, ΔV_g

In Fig. 5.4, all samples (including the control case) exhibit a steadily negative gate voltage shift at low fluence, reach the maximum negative shift at a fluence around ~2.3x10^{-3} C/cm^2, then start to increase ΔV_g in the positive direction. Later, at high fluence, the gate voltage shift approaches zero (zero-crossing point) at a fluence of >6.7x10^{-2} C/cm^2 and then continues increasing positively.

In Fig. 5.4, all fluorinated samples, except B-5E15-25K and A-5E15-25K, have smaller maximum negative gate voltage shifts compared to the control case. Furthermore, except B-5E15-25K and A-5E15-25K, there are crossovers with respect to the control case

for all fluorinated oxides. The crossovers take place at a fluence around $2x10^{-2}$ C/cm^2. Because of the crossovers, all fluorinated oxides have $\Delta V_g = 0$ at higher fluences, including the two cases 5E15-25K and A-5E15-25K. In brief, the control sample demonstrates higher positive gate voltage shift at high fluence (say $f > 2x10^{-2}$ C/cm^2). This phenomenon, as discussed later, is converted to a higher zero-crossing fluence in all the fluorinated oxides, compared to the control oxide's zero-crossing fluence [78]. In addition, between the fluorinated oxides, themselves, the values of fluences at which $\Delta V_g = 0$, can only be clearly observed from higher fluorine-implanted energy families. In Fig. 5.4 (a) and (c), the figures show that the higher F-implanted doses lead to higher zero-crossing fluence.

Positive values in ΔV_g means a net negative trapped charge, and vice versa, in the bulk oxides outside a tunneling distance from the Si/SiO_2 interface. Thus, to summarize from the tails of ΔV_g curves in Figs. 5.4, the following trends can be observed regarding the evolution of electron traps generated in the bulk oxide outside of a tunneling distance from the Si/SiO_2 interface [81]:

a) Regarding the zero-crossing fluence, the fluorinated oxides maintain net positive charge longer than the control oxide (for $f > 2x10^{-2}$ C/cm^2).

b) Regarding how the zero-crossing fluence varies among fluorinated oxides, the higher the ion-implanted fluorine dose, the higher the zero-crossing fluence.

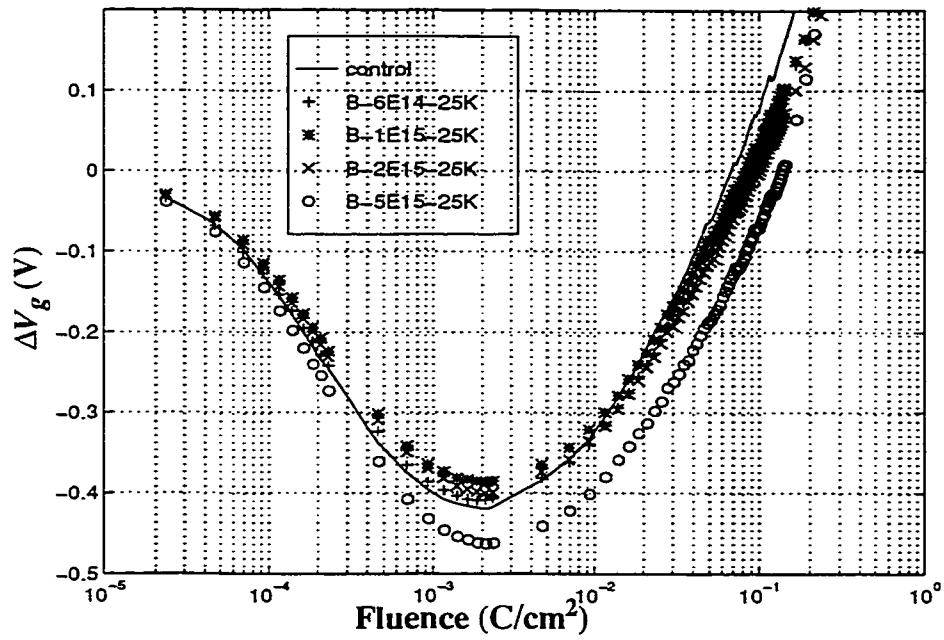


Fig. 5.4- (a) ΔV_g vs. fluence of hot electrons injected from substrate. Control oxide ΔV_g curve is included for comparison. Fluorinated oxides are implanted at 25KeV before poly-etch.

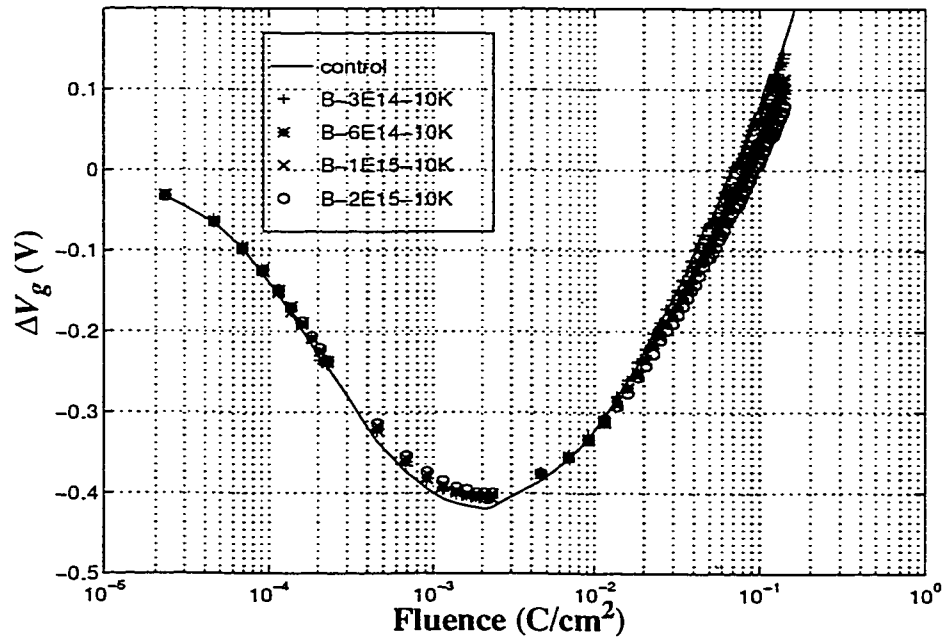


Fig. 5.4- (b) ΔV_g vs. fluence of hot electrons injected from substrate. Control oxide ΔV_g curve is included for comparison. Fluorinated oxides are implanted at 10KeV before poly-etch.

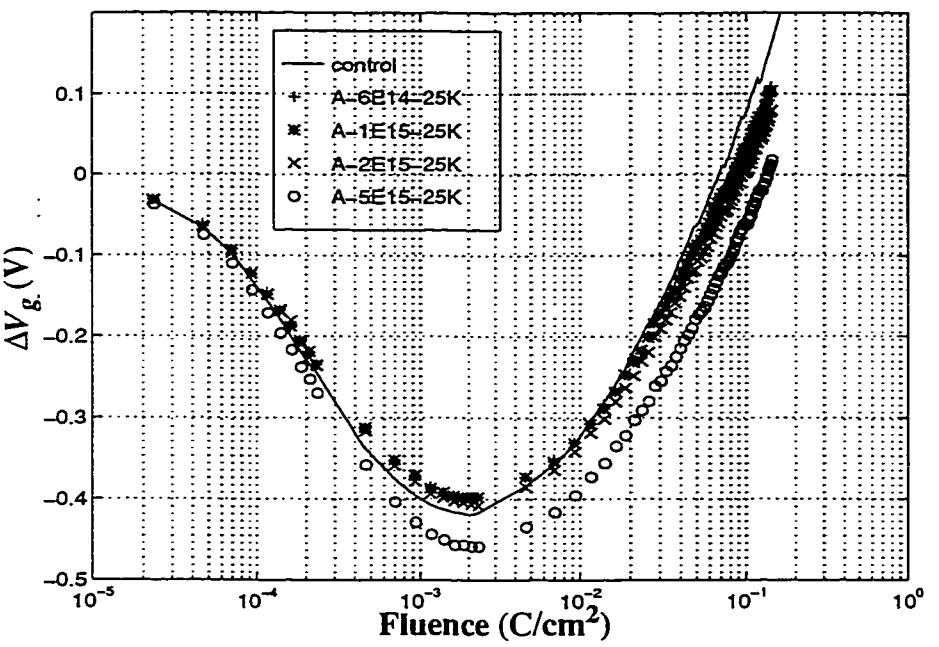


Fig. 5.4- (c) ΔV_g vs. fluence of hot electrons injected from substrate. Control oxide ΔV_g curve is included for comparison. Fluorinated oxides are implanted at 25KeV after poly-etch.

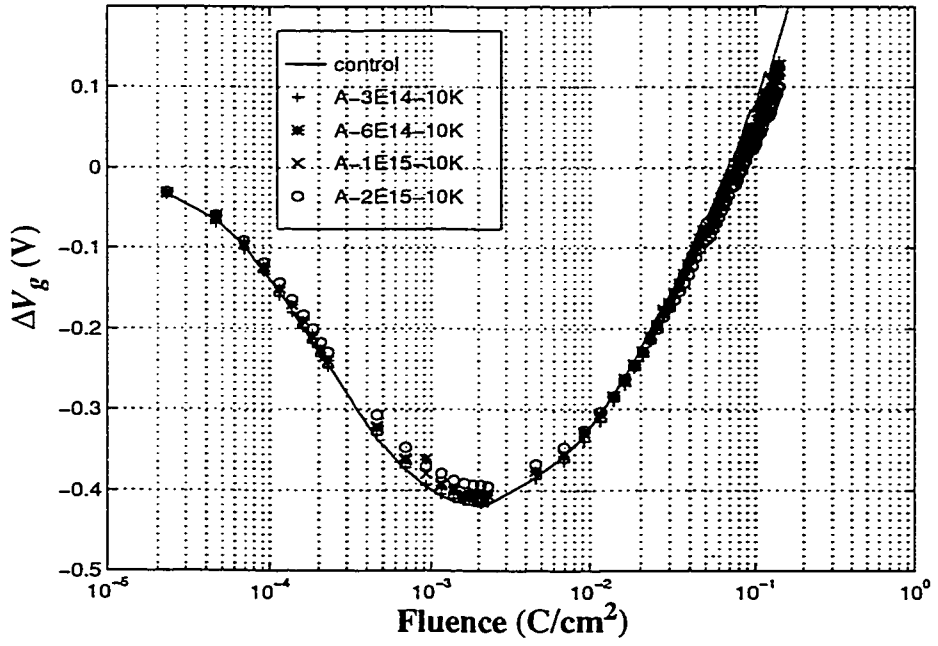


Fig. 5.4 - (d) ΔV_g vs. fluence of hot electrons injected from substrate. Control oxide ΔV_g curve is included for comparison. Fluorinated oxides are implanted at 10KeV after poly-etch.

5.1.1.4 Charging Curves from ΔV_{fb}, ΔV_g, and $\Delta V_{fb} - \Delta V_g$

Figs.5.5 (a), 5.6(a), 5.7(a), 5.8(a) show typical sets of charging curves, calculated from ΔV_{fb} and ΔV_g, for the families B-25, B-10, A-25 and, A-10, respectively. The charge calculated from ΔV_{fb} varies oppositely (from (+) to (-), than the data shown in Fig. 5.2, since *negative* V_{fb} shifts correspond to *positive* charge in the oxide.

The variation in trapped charge calculated from ΔV_g, generally, exhibits various stages. (i) an initial increase in trapped positive charge due to impact ionization, (ii) the attainment of a maximum net positive trapped charge (at about 2.3 $x10^{-3}$ C/cm^2), (iii) a shift from net positive to net negative trapped charge (attained at about 0.7-1.4$x10^{-1}$ C/cm^2 in Fig. 7.8a), as electron trapping (electron trap creation or filling of electron traps having low capture cross-section), becomes dominant, (iv) increasing net negative trapped charge, which usually continues [43, 44, 77] until breakdown. These tests were usually terminated before breakdown occurred [78]. A noteworthy feature in Figs.5.5 (a), 5.6(a), 5.7(a), 5.8(a), is the zero-crossing fluence, at which the ΔV_g net trapped charge starts changing the sign from positive to negative.The zero-crossing fluence is summarized in Fig. 5.9, and tabulated in Table 5.1. All fluorinated samples exhibit a higher zero-crossing fluence than the control (as also observed in Section 5.1.1.3).

Figs.5.5 (b), 5.6(b), 5.7(b), 5.8(b), for the families B-25, B-10, A-25 and, A-10, respectively, are calculated from the ($\Delta V_{fb} - \Delta V_g$) charging curves in Figs.5.5 (a), 5.6(a), 5.7(a), 5.8(a). They show the at/near Si/SiO_2-interface charge as a function of fluence, $N_{ic}(f)$. In each curve, the net interface charge is negative for all fluence levels tested. The higher F-implanted doses systematically lead to *more-negative* $N_{ic}(f)$. In each case, the net

interface charge becomes more negative with increasing fluence, until approximately 7 to $11x10^{-2}$ C/cm^2 is reached. At even greater fluences, N_{ic} levels off or becomes slightly more positive. For example, N_{ic} for the control oxide exhibits the greatest reversal (increase) in this high-fluence regime. The curve reaches its most negative position at about $-4x10^{11}$ /cm^2 at a fluence of $\sim 7x10^{-2}$ C/cm^2 (see Figs.5.5 (b), 5.6(b), 5.7(b), 5.8(b)) [78]. This observation is consistent with the existence of anomalous charge hypothesized from the in-situ studies in Chapter 6 [75, 76].

Fig.5.10 summarizes N_{ic} at 0.1 C/cm^2. In all cases, N_{ic} of fluorinated oxides has more negative induced charge than the control oxide. The magnitudes of N_{ic} at 0.1 C/cm^2 for the two families B-10 and A-10 are slightly higher than for the control oxide (around $0.15x10^{11}$ /cm^2). In families B-25 and A-25, the trend is more obvious, with higher F-implanted dose incurring more built-up net negative trapped charge N_{ic}. Overall, Fig. 5.10 shows that the higher F-implanted doses lead to *more-negative* $N_{ic}(f)$ [78]. The most substantial difference in $N_{ic}(f)$ compared to $N_{ic}(f)$ of the control, comes from the highest dose, $5x10^{15}$ /cm^2. These differences are: $\sim 0.65x10^{11}$ /cm^2 and $\sim 0.73x10^{11}$ /cm^2 for implants before and after poly-etch, respectively. It is also quite interesting to observe in Fig. 5.10 that, at most of the doses, (except at $6x10^{14}$ /cm^2), $N_{ic}(f)$ after poly-etch tends to be slightly more negative than $N_{ic}(f)$ before poly-etch.

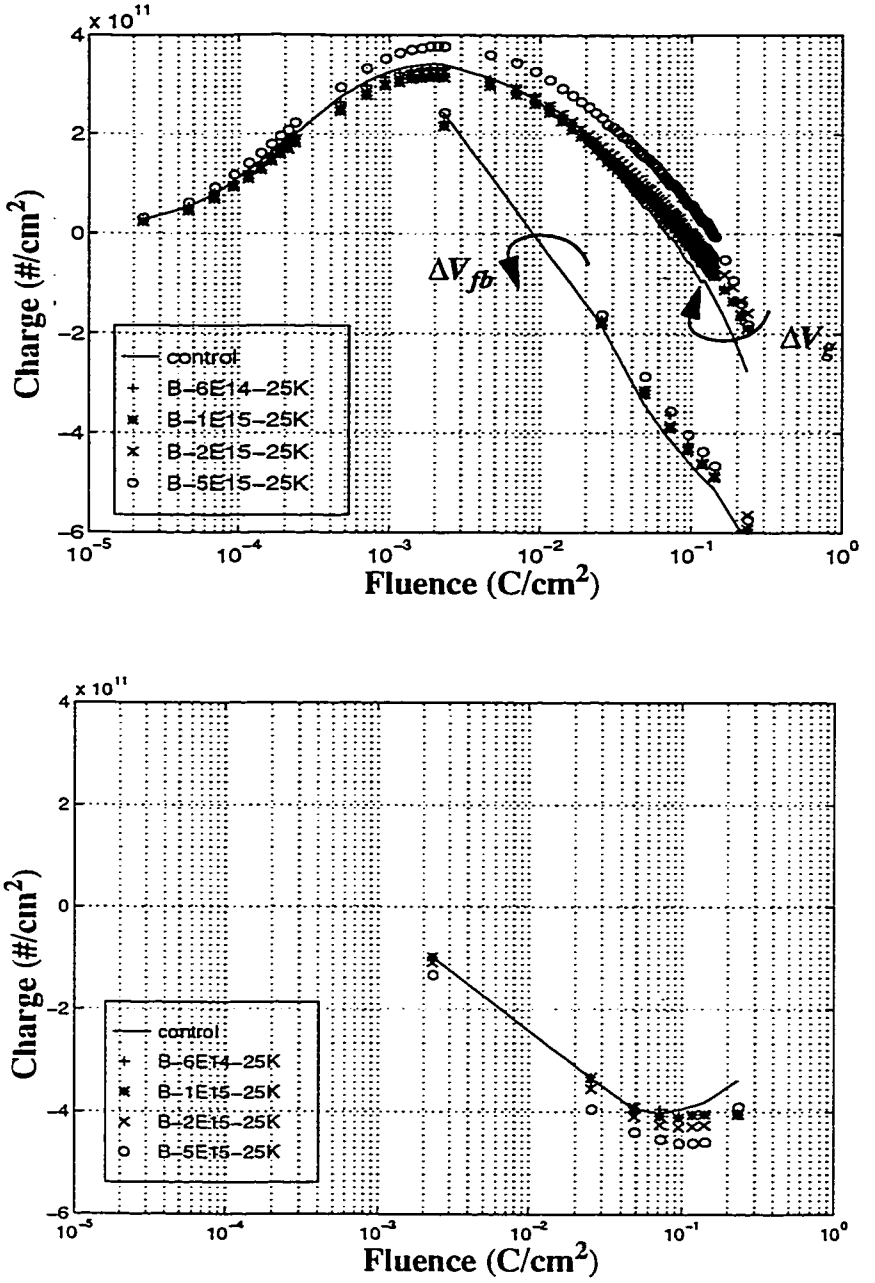


Fig. 5.5 - a) Set of charging curves plotted from ΔV_{fb} and ΔV_g of fluorinated-gate oxide family formed of F-implants at 25KeV before poly-etch. b) Set of charging curves plotted from the difference $\Delta V_{fb} - \Delta V_g$, describing build-up of interface charge during CCFN for the fluorinated gate oxides formed of F-implants at 25KeV before poly-etch.

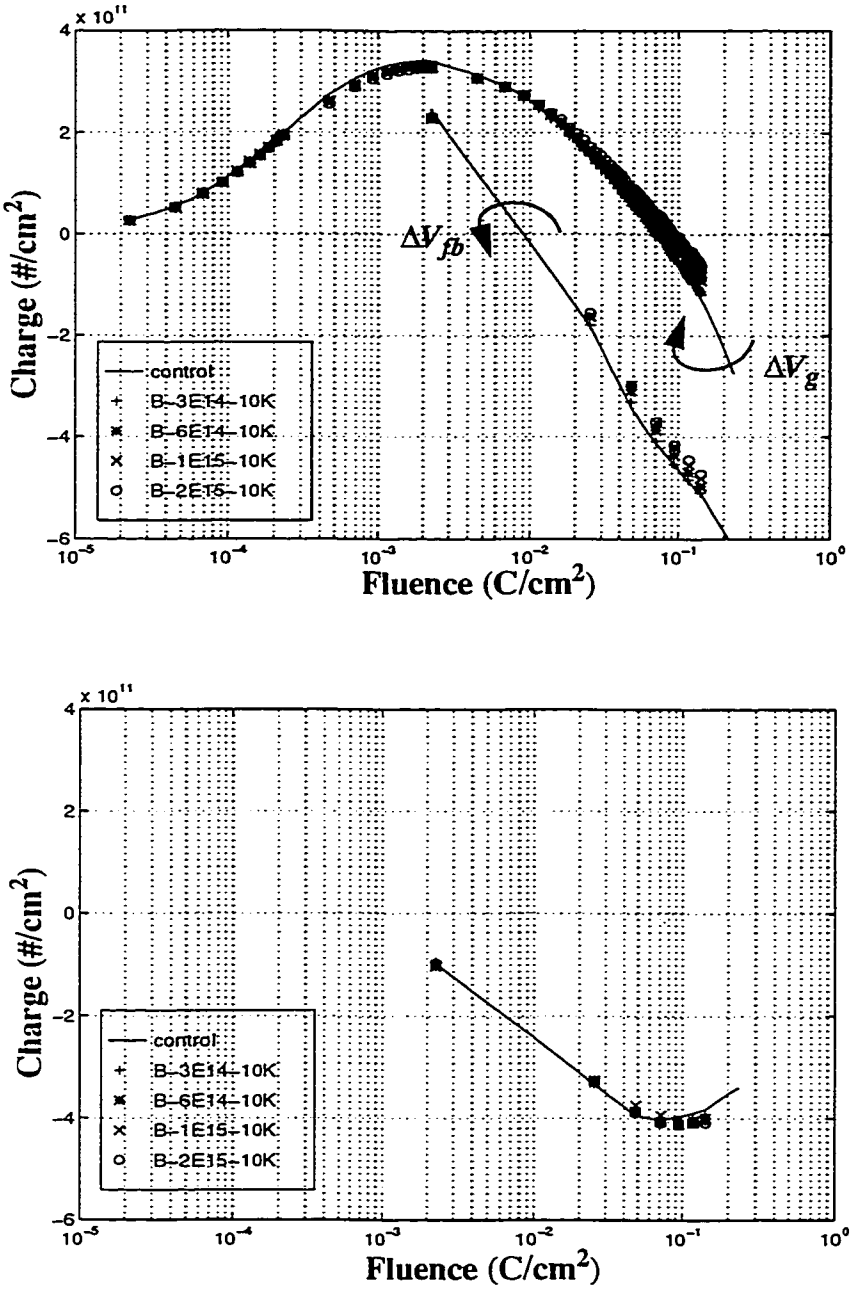


Fig. 5.6 - a) Set of charging curves plotted from ΔV_{fb} and ΔV_g of fluorinated-gate oxide family formed of F-implants at 10KeV before poly-etch. b) Set of charging curves plotted from the difference $\Delta V_{fb} - \Delta V_g$, describing build-up of interface charge during CCFN for the fluorinated gate oxides formed of F-implants at 10KeV before poly-etch.

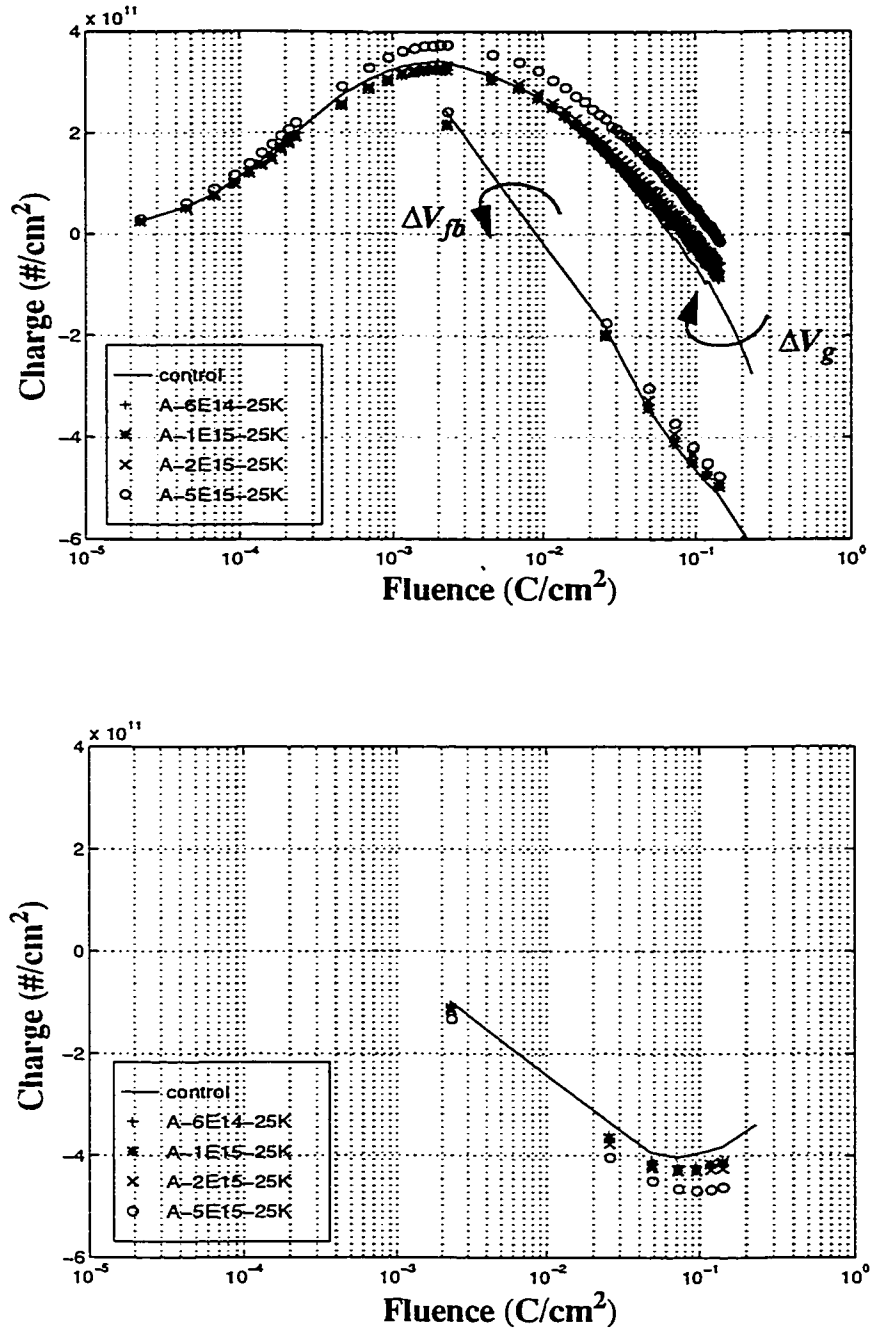


Fig. 5.7 - a) Set of charging curves plotted from ΔV_{fb} and ΔV_g of fluorinated-gate oxide family formed of F-implants at 25KeV after poly-etch. b) Set of charging curves plotted from the difference $\Delta V_{fb} - \Delta V_g$, describing build-up of interface charge during CCFN for the fluorinated gate oxides formed of F-implants at 25KeV after poly-etch.

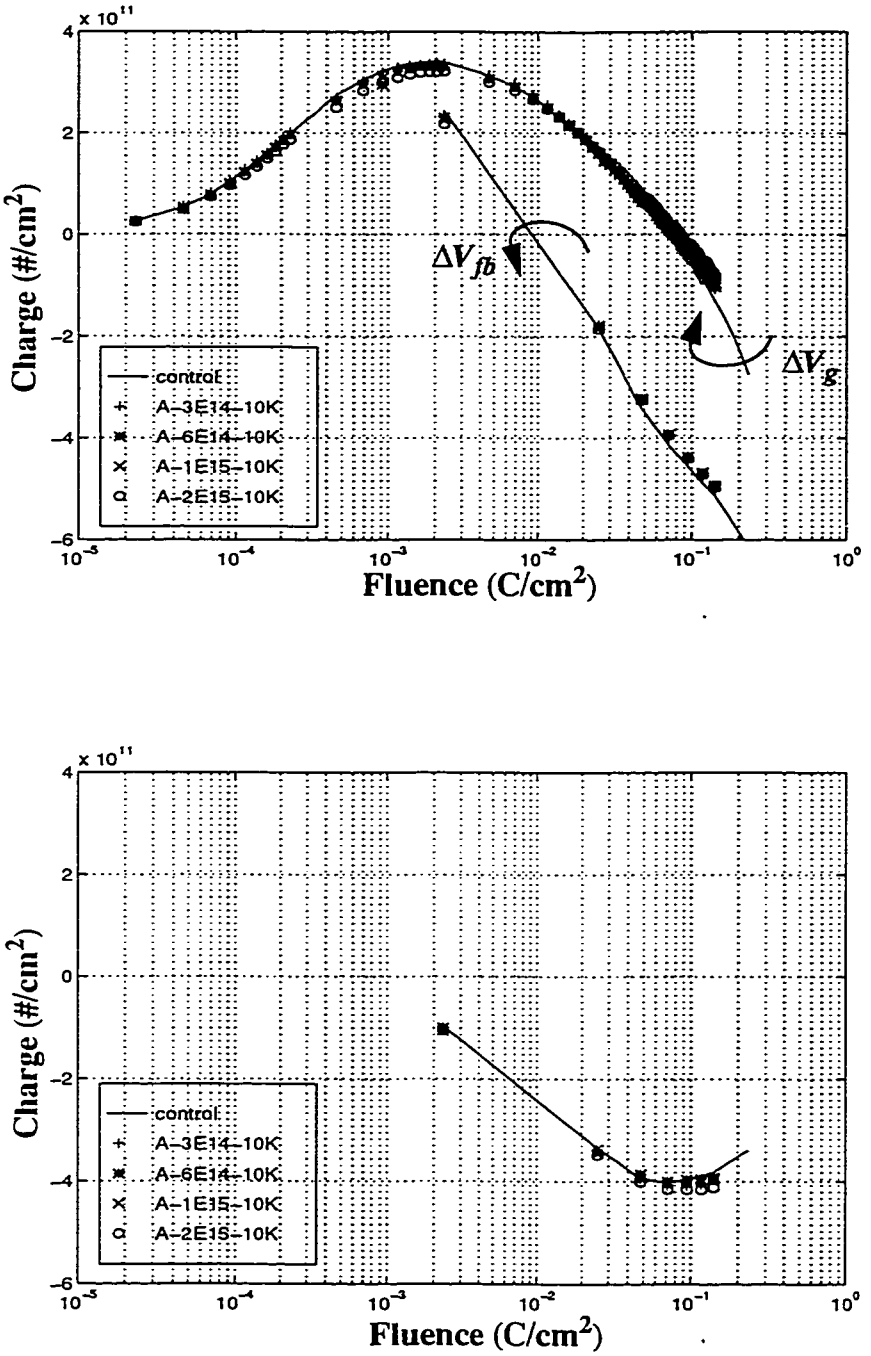


Fig. 5.8 - a) Set of charging curves plotted from ΔV_{fb} and ΔV_g of fluorinated-gate oxide family formed of F-implants at 10KeV after poly-etch. b) Set of charging curves plotted from the difference $\Delta V_{fb} - \Delta V_g$, describing build-up of interface charge during CCFN for the fluorinated gate oxides formed of F-implants at 10KeV after poly-etch.

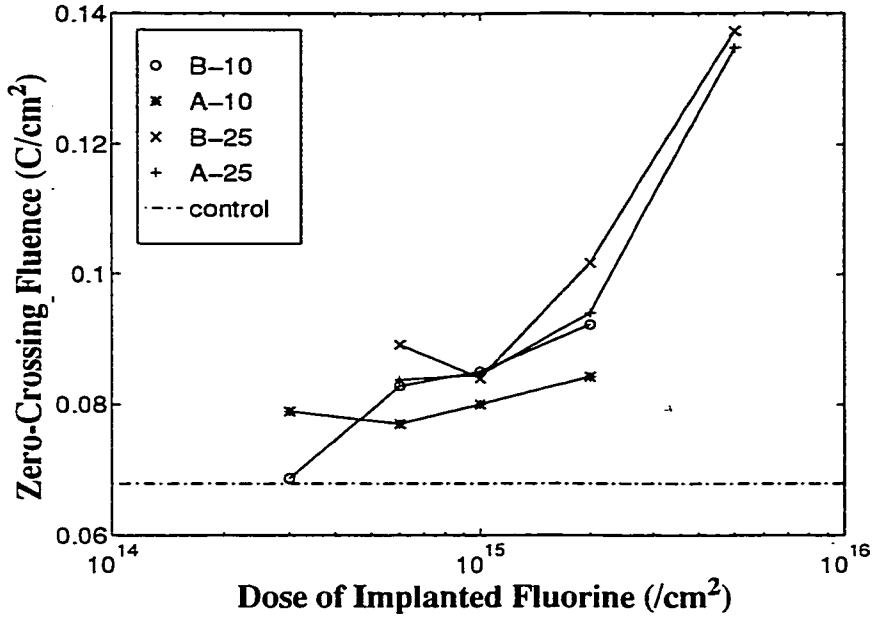


Fig. 5.9 - Zero-crossing fluences vs. implanted fluorine dose for all samples studied. The control oxide zero-crossing fluence is included for comparison.

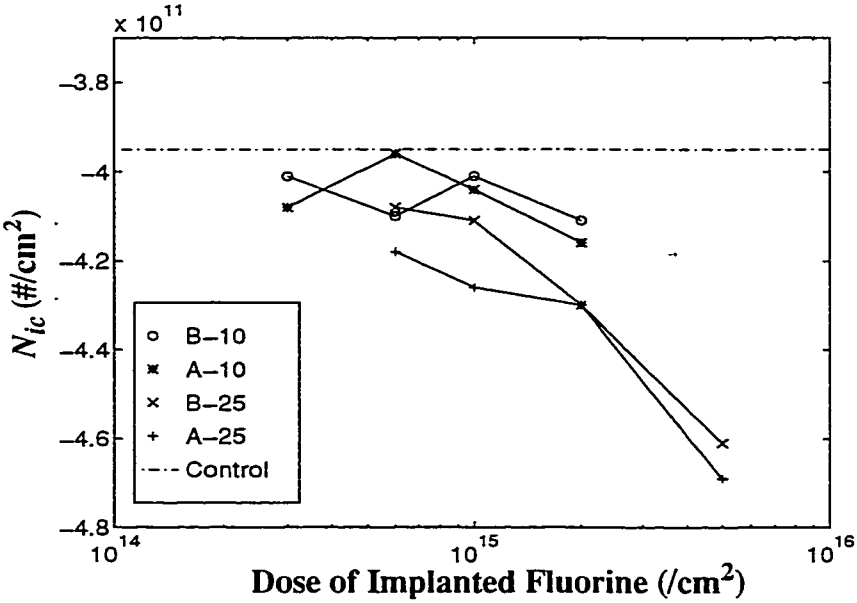


Fig. 5.10 - The near/at the Si/SiO_2 interface trapped charge, N_{ic}, measured at 0.1 C/ cm^2 vs. implanted fluorine dose for all samples studied. The control oxide's N_{ic} is included for comparison.

5.1.1.5 Trapping Rate

In addition to the above features, information about the net *trapping rate* is available from charging curves. $N_{\Delta Vg}$ vs. f data was converted into trapping rate $\Delta N_{\Delta Vfb}/\Delta f$ between successive pairs of data points. Fig. 5.11 shows derived curves for the entire B-25 family. Note that unsigned magnitudes are plotted in this log-log format, and that by comparing with Fig. 5.5a, the net trapping rate becomes negative at $f > 2.3 \times 10^{-3}$ C/cm^2. In this figure, it is impossible to distinguish between the curves in this graph, except that the control oxide may have a more negative trapping rate (higher electron trapping rate) at $f > 10^{-3}$ C/cm^2. The inset shows an expanded linear vs. log view of only the low fluence portion and allows determination of initial net positive (hole) trapping rates at the beginning of each electrical stress.

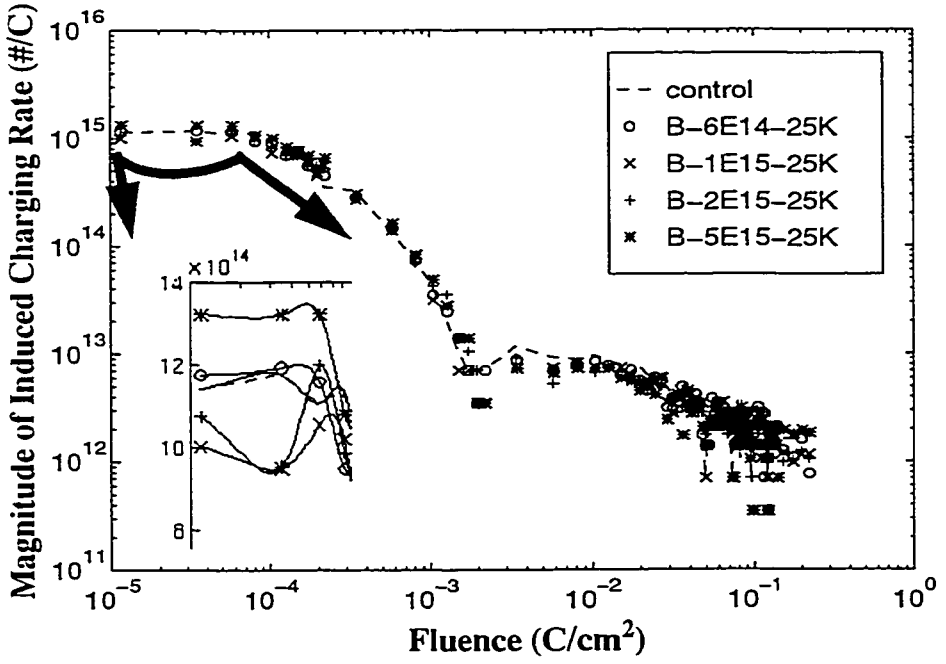


Fig. 5.11 - Magnitude of induced charging rate, extracted from ΔV_g charging curves in Fig. 5.5(a) of fluorinated oxides implanted at 25KeV before poly-etch. These curves indicate that the induced charging rates are functions of injected charge. The inset shows sections of curves at low fluence.

Since it is difficult to discuss differences between the different F-cases in any regime on this graph, Fig. 5.12 was prepared. Fig. 5.12 shows a typical semilog plot for the charging rate calculated from ΔV_g charging curves. As mentioned in section 3.2.4 Fig. 5.12 displays that the net charging rate has evolved through several stages. i) high and relatively constant net positive trapping rate; ii) rapid reduction in net positive charging rate; iii) net charging rate approaches zero and crosses zero; and iv) the net charging rate is saturated at about minus 10^{12} #/C. The linear-log format shows in all cases a straight line portion of each curve from about 10^{-4} to about $5\text{x}10^{-4}$ C/cm^2 [78]. This portion can be modeled using Eq. 3.3 (in Section 3.2.4):

$$\frac{d}{df}\left(N_{\Delta V_g}\right) = K_1 log_{10}(f) + K_2$$

where K_1 and $K_2 < 0$. The thus-extracted K_1, K_2 are also tabulated in Table 5.1.

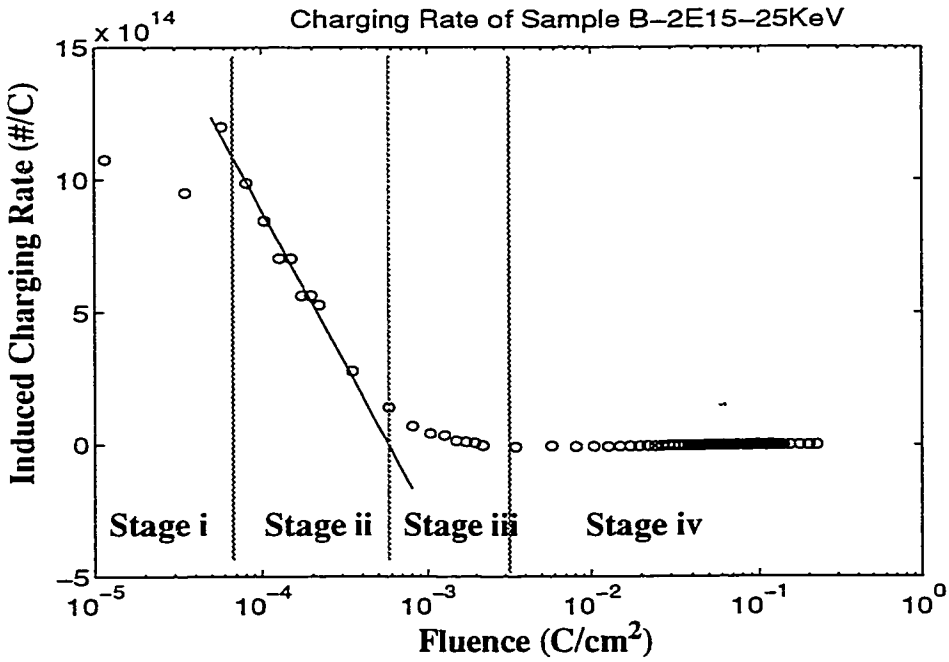


Fig. 5.12 - A typical curve of induced charging rate vs. fluence. Stage ii) is fitted by a straight line using the least-mean square method.

Oxide	Max + position (10^{-3}C/ cm^2)	Max + value (10^{11}/ cm^2)	Zero-Crossing Fluence (10^{-2} C/ cm^2)	Judgement from Zero-Fluence [i]	K_1 [ii] ($x10^{14}$)	K_2 ($x10^{14}$ #/ C)
Control	2.1	3.42	6.79	**Most L**	-15.6	-52.5
B-3E14-10KeV	2.3	3.31	6.87	**LLLL**	-12.9	-42.3
B-6E14-10KeV	2.3	3.31	8.28	**LLL**	-13.3	-44.2
B-1E15-10KeV	2.3	3.27	8.50	**LL**	-10.5	-33.4
B-2E15-10KeV	2.3	3.26	9.22	**L**	-10.4	-32.9
A-3E14-10KeV	2.1	3.39	7.89	**LLL**	-12.0	-38.7
A-6E14-10KeV	1.8	3.32	7.70	**LLLL**	-11.3	-36.0
A-1E15-10KeV	2.3	3.31	8.00	**LL**	-11.4	-36.5
A-2E15-10KeV	2.3	3.22	8.42	**L**	-11.2	-35.9
B-6E14-25KeV	1.9	3.33	8.91	**LLLL**	-11.1	-35.7
B-1E15-25KeV	2.3	3.14	8.40	**LLL**	-10.8	-34.6
B-2E15-25KeV	2.3	3.27	10.17	**LL**	-10.6	-33.9
B-5E15-25KeV	2.3	3.78	13.73	**L**	-12.4	-39.6
A-6E14-25KeV	2.3	3.25	8.37	**LLLL**	-11.6	-37.6
A-1E15-25KeV	2.3	3.24	8.45	**LLL**	-12.0	-39.0
A-2E15-25KeV	2.3	3.33	9.40	**LL**	-11.7	-37.9
A-5E15-25KeV	2.3	3.74	13.47	**L**	-13.7	-44.8

i. **L** refers to Left

ii. Note that the dimension of K_1 is #/C per decade of fluence.

Table. 5.1 - Parameters Derived from ΔV_g versus fluence Curves.

The following main trends can be observed in Table 5.1, and accompanying summary Figs. 5.9, 5.13, and 5.14:

• The maximum net (+) charge occurs at approximately the same fluence (1.8 - 2.3×10^{-2} C/cm^2), for all experimental cases.

• The net (+) charge maxima for the F-implanted cases are generally slightly lower than the control case (with isolated exceptions in the 25keV -implanted families). For the A-10 and B-10 families, the variation is systematic, with the highest dose leading to the lowest maximum (+) value. The two exceptions occur at the highest dose, 5×10^{15} cm^{-2}, and at the highest energy, 25keV.

• The zero-crossing fluences also tend to vary systematically, with only one exception. Fig.5.9 summarizes the zero-crossing results. For all the fluorinated cases, the zero crossings occur at higher fluence than the control oxide. Within each family of implanted cases, higher doses usually led to higher zero-crossing fluence. At a given F-implant dose, higher implant energy tended to give a higher zero-crossing. Comparing implants before poly-etch (B-families) to implants after poly-etch (A-families), the zero-crossings of B-families were usually slightly higher than those of A-families.

• K_1 and K_2 for all fluorinated oxides are substantially lower than K_1, and K_2 for the control case.

• Fig. 5.13 graphs hole trapping rate at a low fluence of ~2×10^{-5} C/cm^2 for all F-implanted cases. Except at the highest dose, 5×10^{15} cm^{-2}, it appears that there is no systematic order due to fluorine dose. However, most of the F-cases cause somewhat lower hole trapping rate than the control oxide, except at the highest dose, 5×10^{15}cm^{-2}.

• Fig.5.14 plots the trends in K_1 vs. F-implant dose. It is interesting to note the U-shaped tendency, indicating that at dose of 1-2x10^{15} cm^{-2}, the negative charging rate may be lowest.

As will be explained in the Discussion Section (5.1.2), these trends are consistent with the theoretical analyses of DiMaria *et al* [43], and are very revealing about the details of the effects of F-implants on oxide and interface quality.

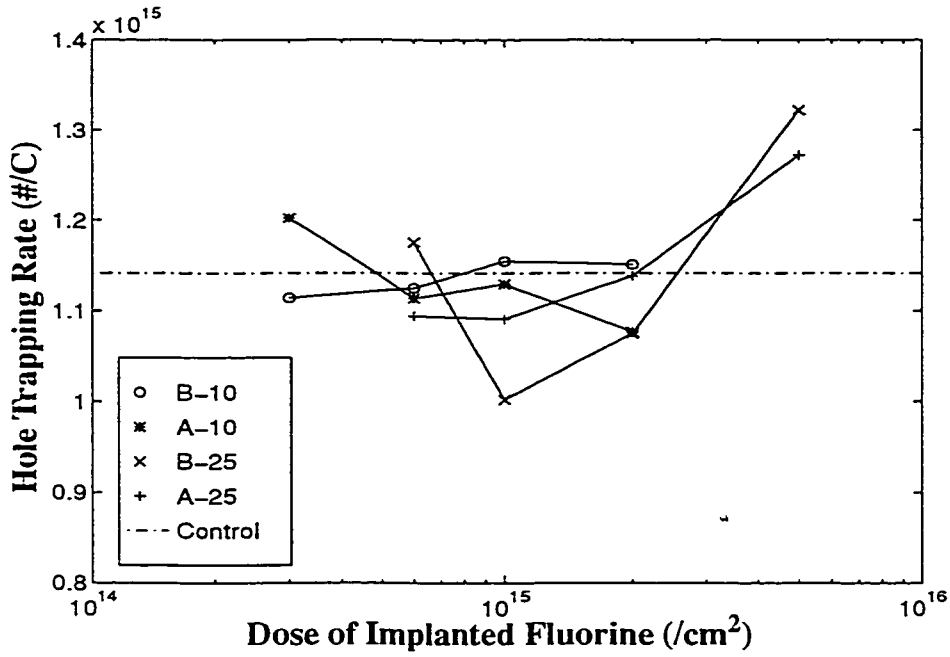


Fig. 5.13 - Average hole trapping rates, calculated from data points in the inset of Fig. 5.11 vs. F-dose for all samples studied. The control oxide average hole trapping rate is included for comparison.

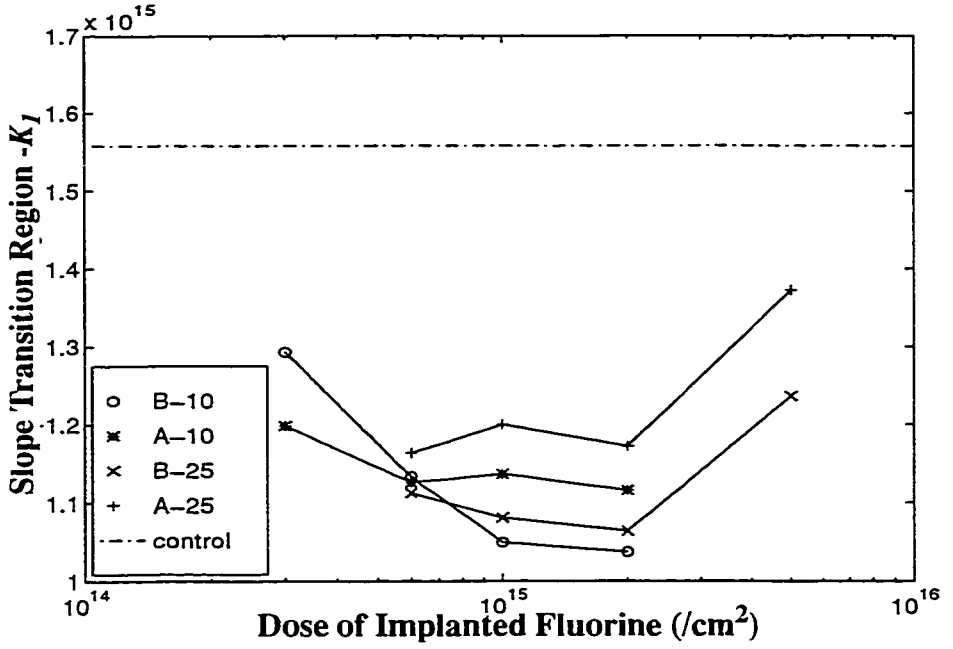


Fig. 5.14 - K_1 vs. F-dose for all samples studied, from the model of stage ii) of Fig. 5.12. These K_1 are calculated from equation: $\frac{d}{df}\left(N_{\Delta V_g}\right) = K_1 log_{10}(f) + K_2$.

5.1.2 Discussion

The analysis of the data focuses on issues of charged defects generated during CCFN stress. The behavior of charged defects in each family of fluorine-implanted oxides is compared to the control oxide. The analysis starts from comparisons of families of fluorinated oxides to the control oxide. Then the trends observed in charging curves, and the evolution of defects are discussed. Conclusions on the roles of fluorine in gate oxides are presented.

5.1.2.1 Interface State Density, D_{it}

The changes of interface state distribution, D_{it}, (in Figs.5.1a-c) are consistent with previous studies in that after a certain injected charge, D_{it} of fluorinated oxides is always smaller than D_{it} of the control oxide [9, 14-15, 26, 63]. In addition, Fig. 5.2 (flatband voltage shifts) and Fig. 5.3 (ΔV_{fb} at 0.1 C/cm^2) support the hypothesis that fluorination increases the overall resistance of gate oxide to FN tunnelling stress under positive gate bias. This agrees with references [14-15]. Except at a dose below 10^{15} cm^{-2} implanted at 25KeV, one could surmise from Fig. 5.3 that higher fluorine dose and higher implanted energy, yield a perhaps *better* gate oxide.

5.1.2.2 Compensation Between Higher Positive Bulk Charge And Higher Negative Interface Trapped Charge To Give A Better ΔV_{fb}

As discussed in Sections 3.2.3, the shift of flatband voltage, ΔV_{fb}, is actually composed of several induced charge components generated during FN tunnelling stress. The curves in Figs. 5.5(a)-5.8(a), 5.12 show that the generated charge in the bulk has compensated the charge near/at the Si/SiO_2 interface, to obtain better flatband voltage shifts in fluorinated oxides. In Figs. 5.5(a)-5.8(a), ΔV_g charging curves show that when $f < 1x10^{-3}$ C/cm^2, there is not much difference between fluorinated oxides and control oxides. But with fluence $>1x10^{-3}$ C/cm^2, the fluorinated oxides maintain a net positive charge longer than the control oxide. This leads to a greater shift left (more negative corresponding to more positive charges) in flatband voltage for the F-cases. Thus by the graphical model in Section 3.2.3.2, if the saturated value of N_{ic} is the same for every sample, then it would be simple to say the fluorinated cases have higher reliability.

However, (ΔV_{fb}–ΔV_g) charging curves (see Figs. 5.5(b)-5.8(b)) display a higher net negative charge built up at/near the Si/SiO_2 interface for every fluorinated oxide, more obvious in the B-25 and A-25 families. This higher net negative charge can be interpreted as a greater contribution to shift right (more positive) in flatband voltage. The overall result, graphically, is: *under positive gate bias CCFN, a more positive net charge in the bulk compensates a more negative net charge at/near the Si/SiO_2 interface to cause a lesser shift in flatband voltage for every case of fluorinated oxides* [78]. Each of these two phenomena is discussed below in greater detail.

5.1.2.3 Interface Trapped Charge

For each before-poly-etch sample (B-families), there is a corresponding after-poly-etch sample (A-families). Due to the fabrication process, a corresponding pair in A- and B- families should have the same amount of fluorine in the bulk oxide. But each A- sample should have a greater amount of fluorine at/near the Si/SiO_2 interface (exactly at/near the perimeter of the MOS capacitors).

Fig. 5.10 shows that in most cases (except for samples implanted with $6x10^{14}$ cm^{-2} at 10KeV), this greater amount of fluorine at the interface results in a more negative N_{ic} at 0.1 C/cm^2. Fig. 5.15, plotted to see the effect of the extra amount of fluorine incorporated into the Si/SiO_2 interface, shows that at a intermediate fluence, the "after" cases exhibit a higher N_{ic} than the corresponding "before" cases. This comparison between B- and A-families is a confirmation of the basic result found by (ΔV_{fb}- ΔV_g) charging curves: In general, *the higher the fluorine dose at/near the Si/SiO_2 interface, the greater the density of*

trapped charges at the interface when subjected to hot electron injection from the substrate [78]. This is in accord with previous reports [64, 85], and supports our use of the (ΔV_{fb}-ΔV_g) method.

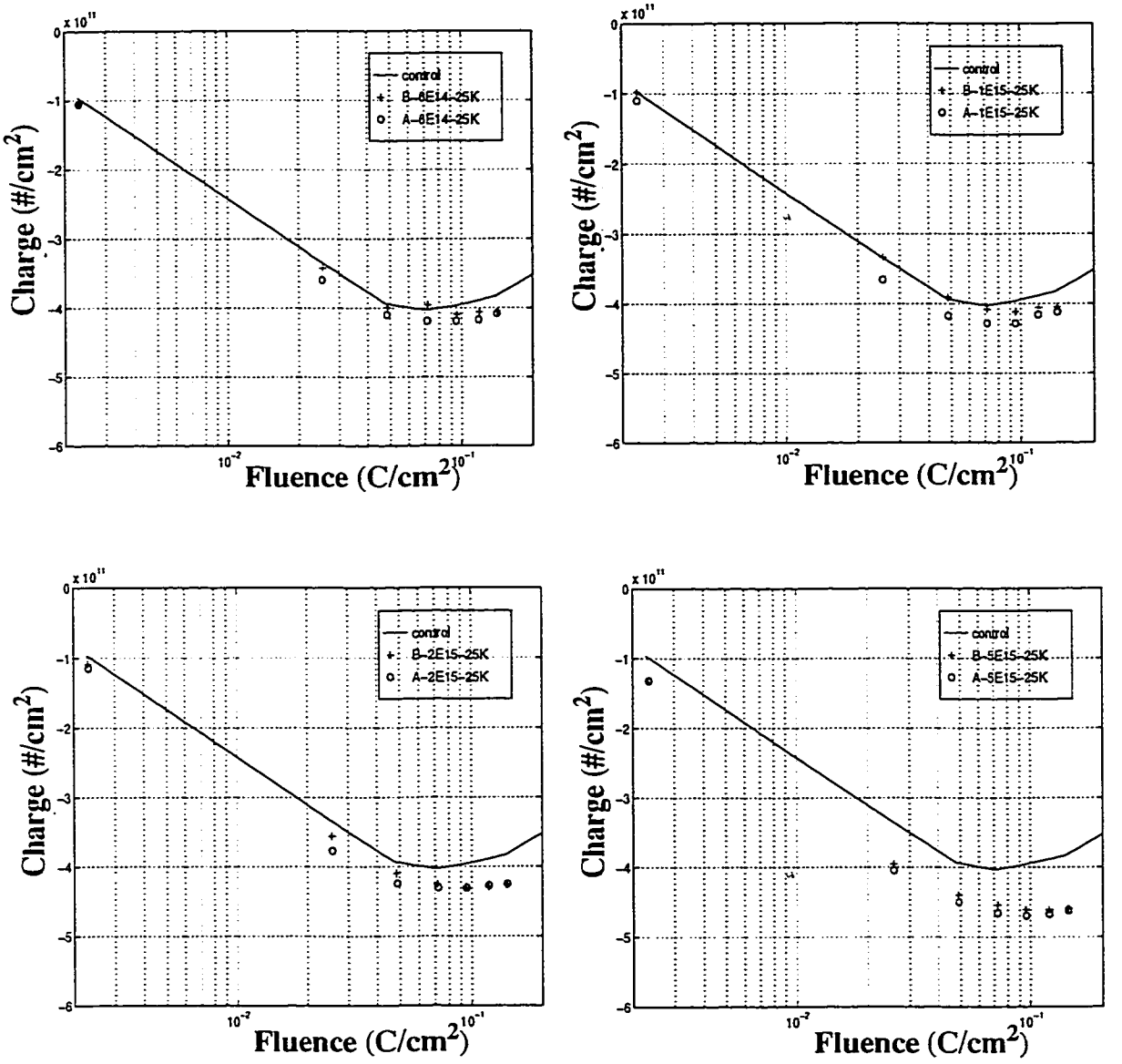


Fig. 5.15 - N_{ic} Curves for corresponding pairs from before and after poly etch of families, B-25K and A-25K.

The increase of the interface trapped charge in A-samples (compared to corresponding B- samples), actually, can be explained by the strain relaxation. As discussed by Ma [14], and Wright and Saraswat [12] (in Section 2.2.1.4), the existence of an excessive amount of fluorine at the Si/SiO_2 interface can cause undesired non-bridging Si-O bonds. By lateral diffusion, in every member of A-families there could be an excessive amount of fluorine introduced to at/near the Si/SiO_2 interface. And this amount of fluorine would be located in a vicinity of the perimeter of the MOS capacitor. Therefore, the fluorine atoms are highly condensed in a small area of the MOS capacitor's Si/SiO_2 interface. Consequently, the excessive amount of fluorine induces a large number of non-bridging Si-O bonds at/near the Si/SiO_2 interface in a vicinity of the perimeter of the MOS capacitor. This leads to higher negative trapped charge in A-samples than in corresponding B-samples. Thus, the before- and after- poly-etch pairs' obtained results support the validity of the strain-relaxation hypothesis.

5.1.2.4 Bulk Trapped Charge

Next, it should be noted that bulk charging observed in ΔV_g charging curves such as Figs.5.5(a) - 5.8(a) is affected by complicated phenomena, in accord with DiMaria *et al*'s model [43]. The net positive charge build-up at fluence $<10^{-3}$ C/cm^2 is evidence of hole trapping at low fluence. The subsequent reduction of net positive charge when fluence $> 2.3\text{x}10^{-3}$ C/cm^2, is an evidence of electron trapping. It is reasonable to hypothesize from stage (i) and (ii) of Fig. 5.12, that, (i) hole trapping begins immediately (likely due to large hole capture cross-section), and is relatively constant at least through $f = 10^{-4}$ C/cm^2 and

that (ii) electron trapping must only become significant by comparison after about 10^{-4} C/cm^2 (likely due to small electron trap capture cross section). Eventually, in stage (iv) of Fig. 5.12, electron trapping becomes slightly greater than hole trapping.

From a detailed look at Figs. 5.5(a) - 5.8(a), it is relatively clear that the variations in zero-crossing fluence among the F-implant cases (between 0.08 and 0.15 C/cm^2), are influenced much earlier in the test. The differences between the ΔV_g charging curves are stable and constant from about $f = 10^{-3}$ C/cm^2 through the zero-crossings. These differences are due to two factors: variations in initial net positive (hole) trapping (in stage (i) in Fig. 5.12), and variations in rapid rate of increase of negative (electron) trapping (in stage (ii) in Fig. 5.12). On the other hand, the control oxide in Fig. 5.5(a)-5.8(a) has a different charging rate at high fluence (~ 10^{-1} C/cm^2), likely due to a higher electron trapping rate in this regime.

Among the F-implant cases, while the zero-crossing fluences in Fig.5.9 appear to vary approximately monotonically with implanted dose, all at a fluence greater than that of the control oxide, a closer look at the factors which determine these zero-crossing fluences again shows more complex variations.

Figs.5.13-5.14 show that the variations of both of hole trapping rate and K_1 (rate of change of electron trapping rate) are not monotonic with dose. Instead, Fig. 5.14 indicates that the rate of change of electron trapping rate in stage (ii) has a minimum at a dose about $2\text{x}10^{15}$ cm^{-2}. This minimum may indicate an *optimal dose* at $2\text{x}10^{15}$ cm^{-2}, *as far as electron trapping in the bulk is concerned.* Also, while the control oxide exhibits the highest

K_1, Fig. 5.14 may suggest that a dose of fluorine above $5x10^{15}$ cm^{-2} could cause K_1 to rise toward that of the control oxide.

Further comparison of the zero-crossing fluences in Table 5.1 and Figs.5.16, between cases implanted before and after poly-etch may indicate another relatively systematic trend which relates fluorine at/near the SiO_2/Si interface to electron trapping in the bulk. Except at the lowest doses, *an excessive amount of fluorine at the Si/SiO_2 interface has led to a greater trapping rate of electrons in the bulk, when hot electrons are injected from the substrate* [78].

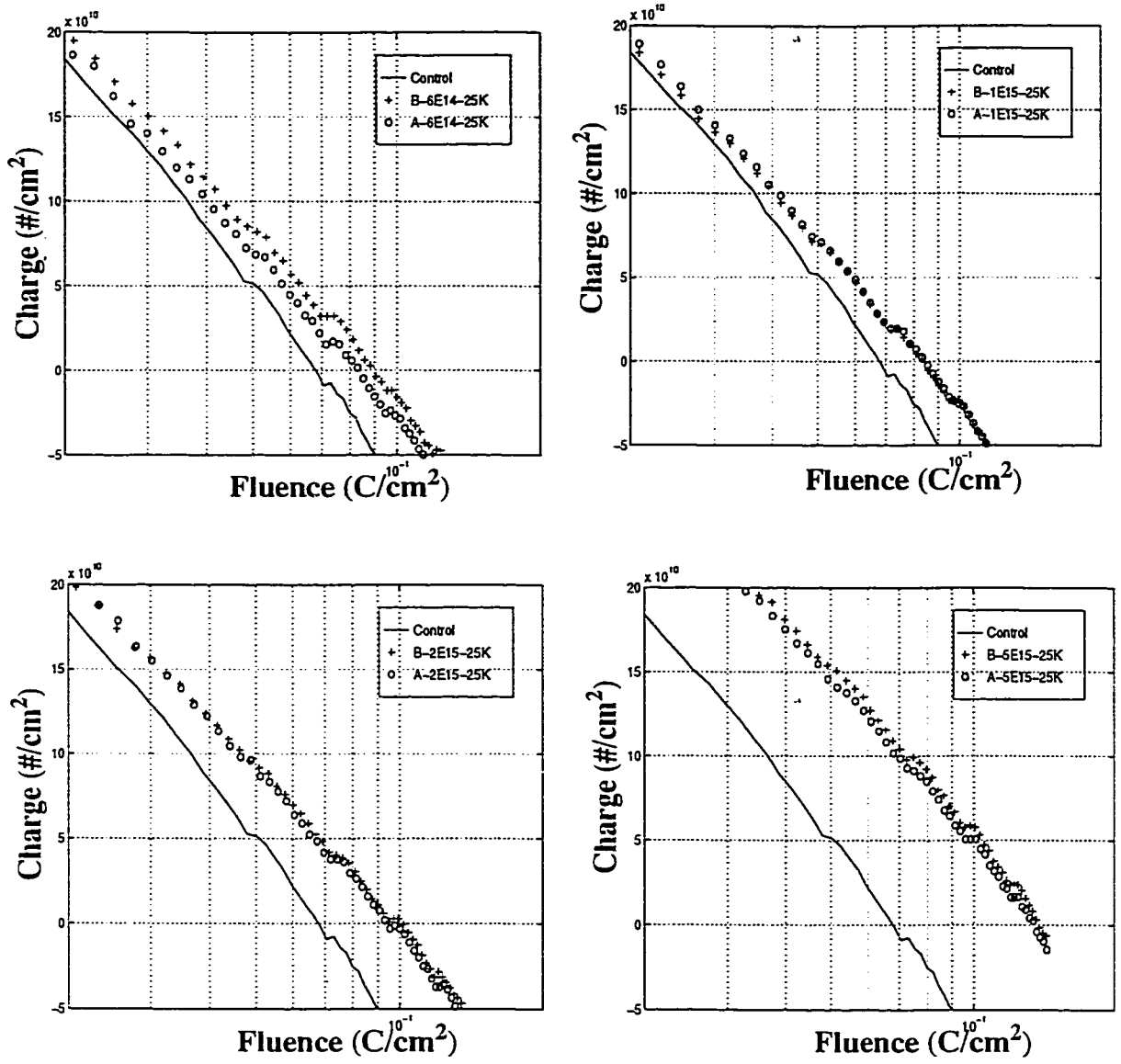


Fig. 5.16 - ΔV_g charging curves in Figs. 5.5(a) & 5.7(a) at high fluence of the corresponding pairs of before and after poly etch. Data from B-25K and A-25K families.

5.1.2.5 Anomalous Positive Charge In Fluorinated Oxides

In Figs. 5.5(b) - 5.8(b), and Fig. 5.15, the control sample shows clearly a turn-around in the at/near interface charging curve at $f \sim 6\text{x}10^{-2}$ C/cm^2. Above this fluence, the net negative charge at the interface and near the interface, is reduced, not greatly, but observably. This suggests the existence of *slow* donor states or anomalous positive charge

(APC) in the control oxide. Since the turn-around is less severe in the F-cases, one can hypothesize that *fluorine at/near the Si/SiO_2 interface, suppresses the generation of APC or slow donor state*s [76, 78]. Similar turnaround phenomena has been reported by other research such as [64, 55]. For example, based on flatband voltage shifts, Xie and Young [64] suggested that a F-dose of 10^{14}-$10^{15}cm^{-2}$ would be optimal dose for suppression of APC. The data in Fig. 5.5(b) are relatively consistent with this, in that the $6x10^{14}$ cm^{-2} and 10^{15} cm^{-2} curves are the flattest out to a fluence of 0.22 C/cm^2 [78].

In addition to the above discussion, the series of Figs. 5.15 show that with an extra amount of fluorine incorporated at the perimeter of MOS capacitor, there are more APC generated near/at the Si/SiO_2 interface. This supports again the suggestion of an optimal dose for APC suppression in fluorination process [64] if the strain relaxation is considered.

5.1.3 Summary of (+) Bias Data

By analysis of the charge components induced in gate oxides under CCFN stress, the roles of incorporated fluorine in gate SiO_2 films are found to be quite complex. By application of the models of DiMaria *et al* [43], it becomes clear that several compensating effects yield the overall changes in flatband voltage. The main effects found are summarized as follow:

- At low fluence, hole trapping in the bulk does not vary significantly due to fluorination.

• At high fluence, greater implanted F-dose leads to lower electron trapping in the bulk. An optimal dose is found, $2x10^{15}$ cm^{-2} at 25KeV, for the rate of change of electron trapping rate.

• Higher implanted F-dose leads to more negative trapped charges at the Si/SiO_2 interface. This agrees well with the strain relaxation theory.

• Slow donor states or APC appear at high fluence, with possible optimum dose consistent with previous research [64] in the range between $6x10^{14}$ cm^{-2} and 10^{15} cm^{-2}.

• When after poly-etch implants yield more fluorine at the interface, this leads to more electron trapping in the bulk (assuming a constant F concentration in the bulk for a corresponding before and after pair). These excessive amounts of fluorine appear to reduce the effect of fluorine suppressing APC.

5.2 Effects of Fluorine Implants on Induced Charge Components in Gate-Oxides Under Negative Gate Bias Constant-Current Fowler-Nordheim Stress.

After a full study (above, Section 5.1) of four fluorinated families, in this Section only the family B-25K is investigated under negative gate bias Fowler-Nordheim constant current injection stress. This is done because of the advantages observed from this family under (+) gate bias. Overall, the fluorinated oxides in B-25K family are better than the ones in A-25K, and B- or A-10K [78].

The measurement set-ups are as the same as the ones in section 5.1. The only difference is that, instead of a (+) polarity bias, now, a begative (-) gate bias is used with a constant current density of 2.36×10^{-4} A/cm^2.

5.2.1 Results and Discussion

5.2.1.1 D_{it} Curves

Fig. 5.17 shows the D_{it} vs. bandgap potential of samples in family B-25K after a negative gate bias constant current Fowler-Nordheim stress ($f = 0.025$ C/cm^2). The scales of the y and x axes in Fig. 5.17 are kept the same as the scales in Figs. 5.1 for later comparison between (+) and (-) gate bias. The figure does not show any dramatic advantages due to fluorination. The inset in Fig. 5.17, therefore, is introduced to get a closer picture of the effect of fluorine on the interface state density. The inset in Fig. 5.17 displays that in the oxides, the D_{it} varies from ~4-4.8x10^{11} eV^{-1}cm^{-2} to 6-7x10^{11} eV^{-1}cm^{-2} for the range of the bangap potential from -0.1 to 0.1 eV. In this range, the sample B-5E15 shows the highest induced D_{it}, which is always lightly higher than the control's D_{it}. However, the other three fluorinated oxides show less D_{it} in this range of bangap potential.

In the inset of Fig. 5.17, the variation between the fluorinated cases suggests a very shallow optimal dose, which may be near 2×10^{15} cm^{-2}. The non linear relationship of fluorine dose vs. D_{it} again supports the strain relaxation hypothesis, in which an optimal fluorine dose is predicted.

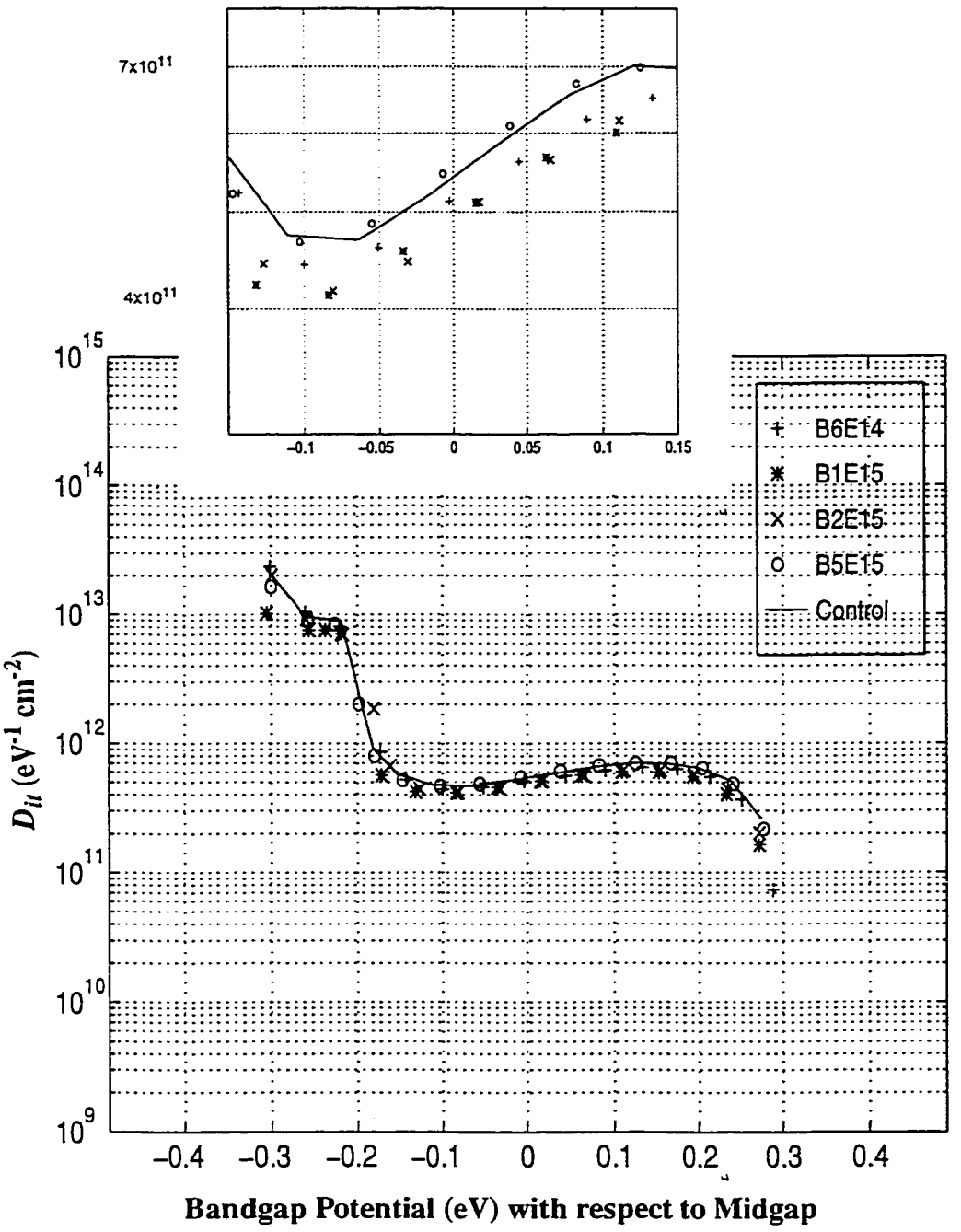


Fig. 5.17 - D_{it} Vs. bandgap potential for fluorinated oxides in family B-25K. The injected fluence is 0.023 C/cm^2.

Fig. 5.18 presents the D_{it} vs. bandgap potential of samples in family A-25K after a negative gate bias constant current Fowler-Nordheim stress ($f = 0.025 C/cm^2$). Similarly to Fig. 5.17, the fluorinated cases do not show any dramatic advantages in induced D_{it}. Again a zoomed inset is required to see the fluorination effect more clearly. Now, in the inset of Fig. 5.18, the D_{it} curve of sample B-5E15 is coincident with the control curve, and the D_{it} curve of A-1E15 shows the highest D_{it}. But sample A-2E15 again appears to have the optimal dose.

A closer look at the insets in Fig. 5.17 and Fig. 5.18 shows that, except for the pair A-B-5E15, all fluorinated A- and B- pairs show a higher D_{it} in the A-sample. For example, the midgap D_{it} of A-2E15 is higher than the midgap D_{it} of B-2E15 with a difference around 0.5×10^{11} $eV^{-1}cm^{-2}$.

Thus, in general, the data in Fig. 5.17 and Fig. 5.18 show a slight advantage can be gained from fluorination. As small as this advantage is, it is again cancelled out when an excessive amount of fluorine is introduced into at/near the Si/SiO_2 interface. It again supports the validity of the strain relaxation mechanism

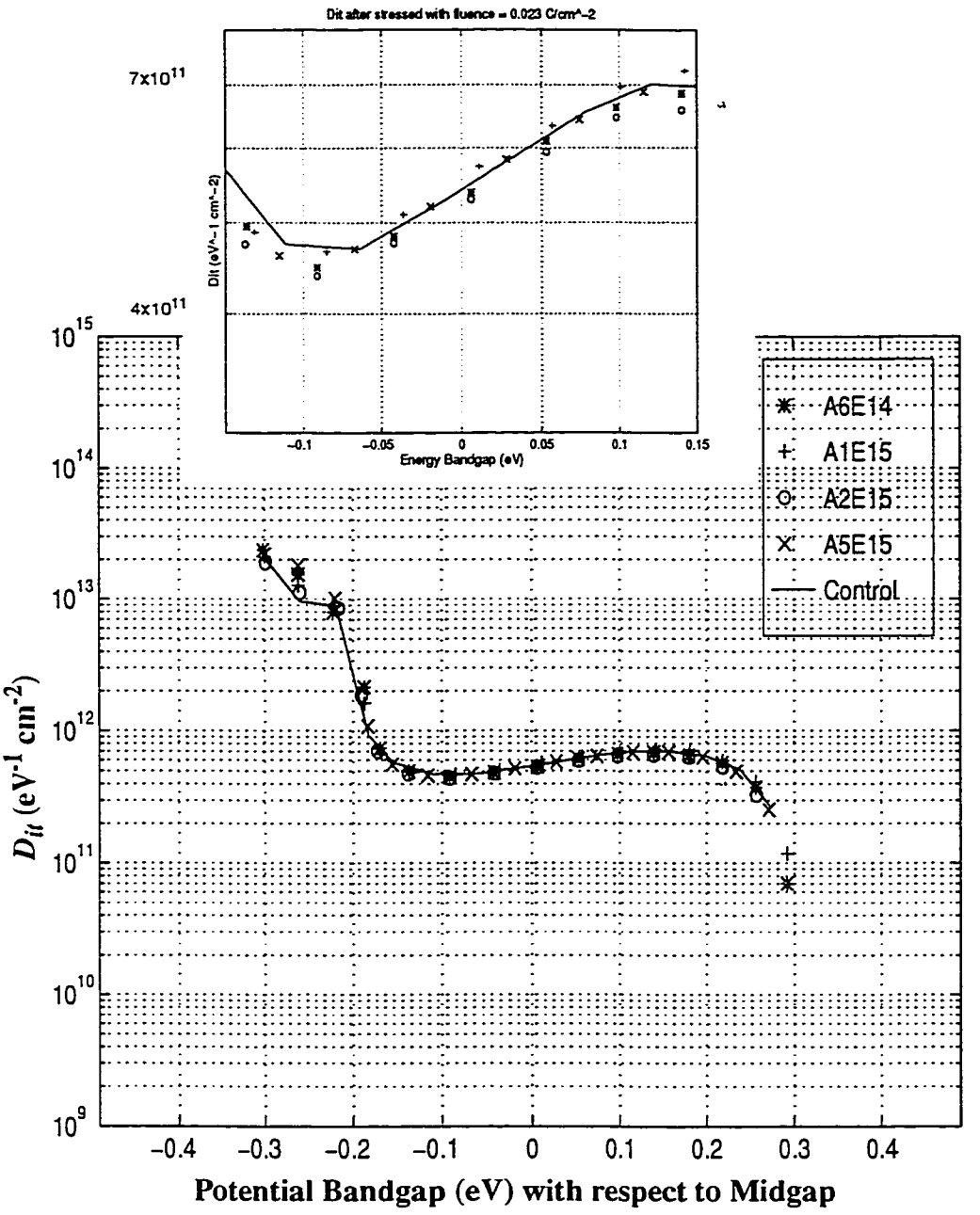


Fig. 5.18 - D_{it} Vs. bandgap potential for fluorinated oxides in family A-25K. The injected fluence is 0.023 C/cm^2.

5.2.1.2 ΔV_{fb} Charging Curves

Fig. 5.19 shows the ΔV_{fb} charging curves calculated from ΔV_{fb} in (-) CCFN. Fig. 5.19 displays that under (-) bias the overall net charge evolves through several stages: (i) build-up of the net positive trapped charge, (ii) attainment of a positive maximum at a fluence ~$2.3\text{x}10^{-2}$ C/cm^2, (iii) a shift from net positive to net negative trapped charge (attained about 1.8-$2.1\text{x}10^{-1}$ C/cm^2) as electron trapping (electron trap creation or filling of electron traps having low capture cross-section), becomes dominant, (iv) increasing net negative trapped charge, which usually continues [43] until breakdown. These tests were usually terminated before breakdown occurred [80].

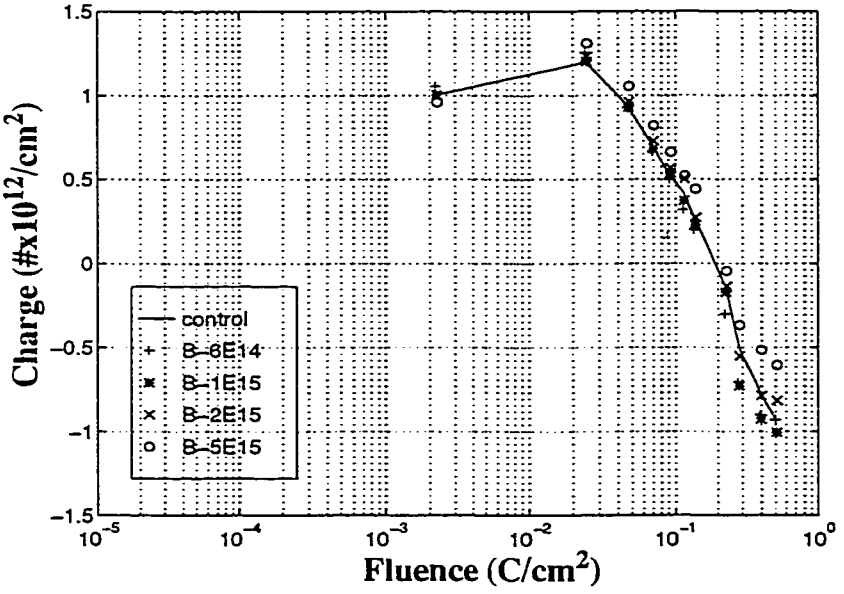


Fig. 5.19 - Charge Calculated from ΔV_{fb} under negative gate bias CCFN stress.

Some observations can be stated. B-5E15 has the highest positive maximum. Therefore, B-5E15 must have a higher hole trapping rate than the control and other fluorinated oxides. However, it is quite difficult to say whether every fluorinated oxide has higher hole trapping rate than control oxide, because the other three fluorinated oxides

have more hole trapped charges than the control oxide at both fluence, at $f = 2.3\text{x}10^{-3}$ C/cm^2 and at $f = 2.3\text{x}10^{-2}$ C/cm^2 (the positive maxima).

In the range of fluences from 5 to $8\text{x}10^{-1}$ C/cm^2, the control's charging curve intercepts the fluorinated oxide curves, except case B-5E15-25K's curve. These crossovers may indicate that the fluorinated oxides have higher electron trapping rate than the control. However, it is quite difficult to see the variation among the fluorinated curves.

5.2.1.3 ΔV_g Charging Curves

Fig. 5.20 displays the variations in charging in $N_{\Delta Vg}$ under (-) gate bias, $N_{\Delta Vg}$-. As discussed in Section 3.1, $N_{\Delta Vg}$- is sensitive to charging in the gate oxide excluding charging within a tunneling distance from the poly/SiO_2 interface. Fig. 5.20 shows that the charging due to ΔV_g evolved through several stages: (i) increasing of positive trapped charge at low fluence, (ii) reaching a positive maximum at $f \sim 2.3\text{x}10^{-3}$ C/cm^2, (ii) a shift from net positive to net negative trapped charge (attained at about $f = 1.6\text{-}4.0\text{x}10^{-1}$ C/cm^2 for most cases), as electron trapping (electron trap creation or filling of electron traps having low capture cross-section), becomes dominant, (iv) increasing net negative trapped charge until breakdown.

This $N_{\Delta Vg}(f)$- evolution is similar to $N_{\Delta Vg}(f)$+ evolution, discussed in Section 5.1.1.4. Table 5.2 tabulates the positive maxima, and the fluences at which the maxima occur, and N_{ic} (f) values. Both (-) and (+) values are included in Table 5.2 for later comparison in Section 5.3.

In Fig. 5.20, in stage (i) and (ii), $f = 0$ to 2.3×10^{-3} C/cm^2, the fluorinated oxides always expose fewer positive trapped charges. This might be evidence that the fluorination reduces hole trap generation in the gate oxide under (-) gate bias. The systematic variation between the fluorinated oxides in hole trap aspect can be observed in Fig. 5.20 and the column (-) bias max positive values: *the higher the implanted fluorine dose, the less the hole trap generation.* Note that $N_{\Delta Vg}$- consists of trapped charge generated in the bulk (a tunneling distance away from the poly/SiO_2 interface) and the charge located at the Si/SiO_2 interface. As discussed in Section 5.1.2.3, because fluorination increases the negative trapped charge at/near the Si/SiO_2 interface [78], there might be possibilities that this is the reason for reducing positive maxima values in the fluorinated oxide $N_{\Delta Vg}$ *(f)*-.

The aspect of electron traps, however, does not display clearly the same tendency as the observed in hole traps at low fluence. Fig. 5.20 exposes that, except case B-5E15-25K, the other fluorinated oxides have zero-crossing fluences lightly smaller than the control's zero-crossing fluence. Due to the tails of $N_{\Delta Vg}$ *(f)*- curves in Fig. 5.20, the zero-crossing fluences are varied between oxides (from high to low) as: control and B-1E15 (both seems sharing the same zero-crossing fluence), B-2E15, B-6E14 and B-5E15. Therefore, the variation in negative trapped charges is not systematic among the fluorinated oxides.

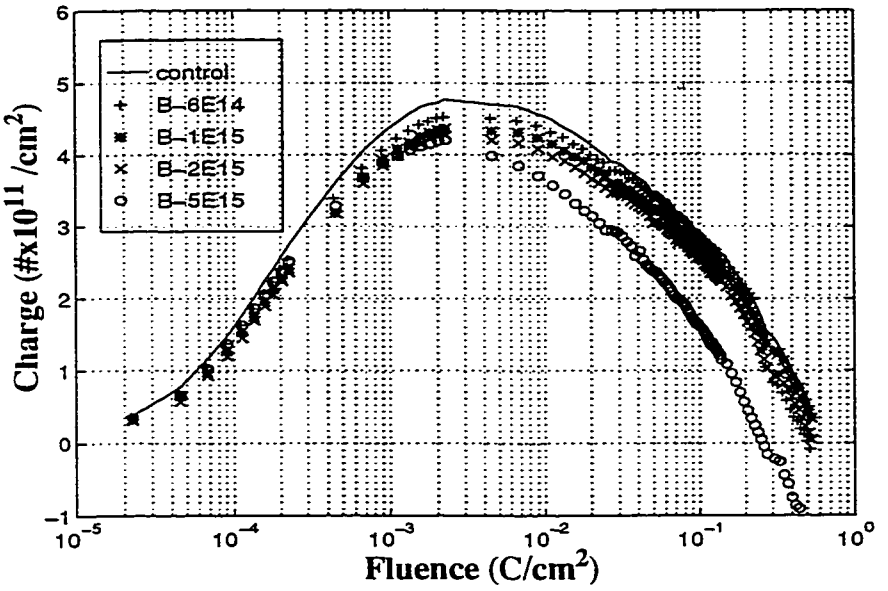


Fig. 5.20 - Charging curves calculated for B-25K from ΔV_g under a (-) gate bias FN stress.

Oxide	*(+)Bias* max + position (10^{-3} C/ cm^2)	*(-)Bias* max + position (10^{-3} C/ cm^2)	*(+) Bias* N_{ic} at 2.3×10^{-3} C/cm^2 (10^{11} / cm^2)	*(-)Bias* N_{ic} at 2.3×10^{-3} C/cm^2 (10^{11} / cm^2)	*(+)Bias* max + value (10^{11} / cm^2)	*(-)Bias* max + value (10^{11} / cm^2)	*(+) Bias* Total charge at 2.3×10^{-3} C/cm^2 (10^{11}/ cm^2)	*(-)Bias* Total charge at 2.3×10^{-3} C/cm^2 (10^{11} / cm^2)
Control	2.1	2.2	- 0.96	5.25	3.42	4.77	2.44	10.02
B-6E14-25K	1.9	2.2	- 1.06	6.00	3.33	4.53	2.27	10.05
B-1E15-25K	2.3	2.3	- 0.98	5.57	3.14	4.37	2.16	10.03
B-2E15-25K	2.3	2.3	- 1.09	5.70	3.27	4.28	2.18	9.98
B-5E15-25K	2.3	2.3	- 1.34	5.37	3.78	4.21	2.44	9.58

Table. 5.2 - Comparison of maximum values of positive maxima from charging curves in both set of (+) and (-) gate bias FN stress after an injected fluence of ~2.5×10^{-2}C/cm^2.

5.2.1.4 (ΔV_{fb}-ΔV_g) Charging Curves

Fig. 5.21 shows the extracted data from ΔV_{fb}-ΔV_g, measured under (-) gate bias. $N_{ic}(f)$- curves display the evolution of trapped charges at/near poly/SiO_2 interface through several stages: (i) build-up of the net positive trapped charge, (ii) attainment of positive maximum at a fluence ~$2.3x10^{-2}$ C/cm^2, (iii) a shift from net positive to net negative trapped charge (attained about 1.4 to $2.2x10^{-1}$ C/cm^2) as electron trapping (electron trap creation or filling of electron traps having small capture cross-section), becomes dominant, (iv) increasing net negative trapped charge., which usually continues until breakdown. This evolution is as same as the evolution observed in $N_{\Delta Vfb}(f)$- (discussed in Section 5.2.1.2).

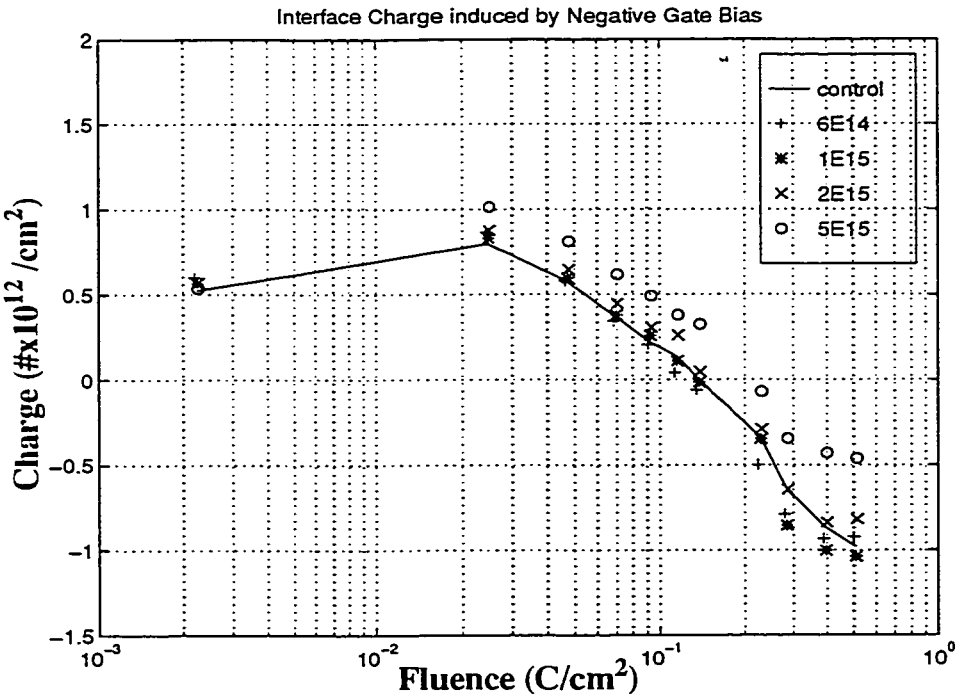


Fig. 5.21 - ΔV_{fb}-ΔV_g Charging Curves for the family B-25K under negative gate bias FN stress.

In Fig. 5.21, at low fluence (up to f~2.3x10^{-2} C/cm^2), all fluorinated oxides exhibit more hole trapped charges than the control. Especially, case B-5E15-25K shows the highest positive maxima at f ~2.3x10^{-2} C/cm^2. Thus fluorination increases the hole trapped charges at/near the poly/SiO_2 interface under (-) CCFN. Accordingly, the right-most column of Table 5.2 shows a trend that the higher implanted fluorine doses yield less hole trap generation.

However, Fig. 5.21 shows that, only the case B-5E15-25K might have less electron trapped charge than the control (at high fluence). In the other fluorinated $N_{ic}(f)$- curves, there are crossovers with the control 's curve. Thus, with a higher positive maximum (than the control), these crossovers indicate that the fluorinated oxides exhibit a higher electron trapping rate than the control. Perhaps, as happened at the Si/SiO_2 interface, at the poly/SiO_2 interface, fluorine atoms could cause some damage near the poly/SiO_2 interface. This might be the reason for more electron trapped charges in the fluorinated cases.

Table 5.2 shows that under (-) CCFN more defects are caused than in (+) CCFN (see the total charge columns). A rough estimate can show that most positive defects are located at/near the poly/SiO_2 interface. First, the $N_{\Delta Vfb}(f)$- values (see Fig. 5.19) are substantially larger than the charge contribution from the Si/SiO_2 interface. For instance, at f = 2.3x10^{-2} C/cm^2, the $N_{\Delta Vfb}$- is at least $2(D_{it}$-), this suggests that $N_{\Delta Vfb}$- contains substantial contributions either from positive trapped charges somewhat farther out in the oxide (such that they would not be seen in the D_{it}) or from near-interface positive traps outside of the silicon band gap [80]. Secondly, the $N_{\Delta Vfb}(f)$- values (see Fig. 5.19) are also larger than the $N_{\Delta Vg}(f)$- values (see Fig. 5.20). Therefore, this suggests that $N_{\Delta Vfb}$- contains substantial contributions from positive trapped charges *not* located in the bulk oxide. With

these discussions, only one possibility remains: that $N_{\Delta Vfb}$- contains substantial contributions from positive trapped charge located at/near the poly /SiO_2 interface. This conclusion is consistent with the DiMaria model, in which under negative gate bias CCFN, ΔV_g is not sensitive to the trapped charges which are created or located within a tunnelling distance from the poly/SiO_2 interface.

This new set of positive trapped charges (located at/near the poly/SiO_2 interface) yields positive trapped charge maxima at an injected f ~$2.3x10^{-2}$ C/cm^2 (see Fig. 5.19 and Fig. 5.21). However, the positive maxima in $N_{\Delta Vg}(f)$- occur at f~ $2.3x10^{-2}$ C/cm^2 (see Fig. 5.20 and Table 5.2). This indicates that the positive trapped charges at/near the poly/SiO_2 interface have smaller hole capture cross-section than the $N_{\Delta Vg}(f)$- hole capture cross-section.

5.2.1.5 Induced Charging Rate In The Bulk of Oxides

Figs. 5.22 (a) and (b) presents the induced charging rate calculated from $N_{\Delta Vg}(f)$-, via Eq. 3.2. Fig. 5.22(a) plots $\Delta N_{\Delta Vg}(f)$-/Δf vs. f in semilog scale, while Fig. 5.22(b) plots the magnitude of induced charging rate vs. f in log-log scale.

In Fig. 5.22(a), at low fluence, the hole trapping rate shows a non-linear dependence on fluorine-implant dose. The control case presents the largest value of the positive charging rate. All positive charging rates of the fluorinated oxides are lower than the control rate. The optimal dose is $2x10^{15}$ cm^{-2}.

In Fig. 5.22(b) the charging rate changes sign around $f = 2.3 \times 10^{-3}$ C/cm^2 (this corresponds to the zero-crossing fluence). The tails (right side of the figure) of charging rate curves vs. fluence show that the fluorinated cases have negative charging rates which are almost the same as the control rate, except for case B-5E15-25K [80].

Table 5.3 summarizes the values of K_1 and K_2 which are extracted from Fig. 5.22. The values of K_1 and K_2 in (+) CCFN also are included to compare the effects of fluorine in both bias configurations (discussed later). The two main parameters of interest are low-fluence hole trapping rate, and rate of change of trapping rate K_1^a. In these aspects, under (-) CCFN, 2×10^{15} /cm^2 appears to be again optimal dose (as in (+) bias).

Oxide	*(+) Bias* K_1[i] (10^{15})	*(-) Bias* K_1 (10^{15})	*(+) Bias* K_2 (10^{15} #/C)	*(-) Bias* K_2 (10^{15}#/C)	*(+) Bias* Hole Trapping Rate (10^{15})	*(-) Bias* Hole Trapping Rate (10^{15})
Control	-1.56	-1.67	-5.25	-5.43	1.17	1.72
B-6E14-25KeV	-1.11	-1.64	-3.57	-5.39	1.18	1.60
B-1E15-25KeV	-1.08	-1.57	-3.46	-5.16	1.00	1.44
B-2E15-25KeV	-1.06	-1.40	-3.39	-4.52	1.07	1.36
B-5E15-25KeV	-1.24	-1.80	-3.96	-5.99	1.32	1.50

i. Dimension of K_1 is #/C per decade of fluence

Table. 5.3 - K_1, K_2 and Hole Trapping Rate of members in family of B-25K, presented both in (+) and (-) FN stress.

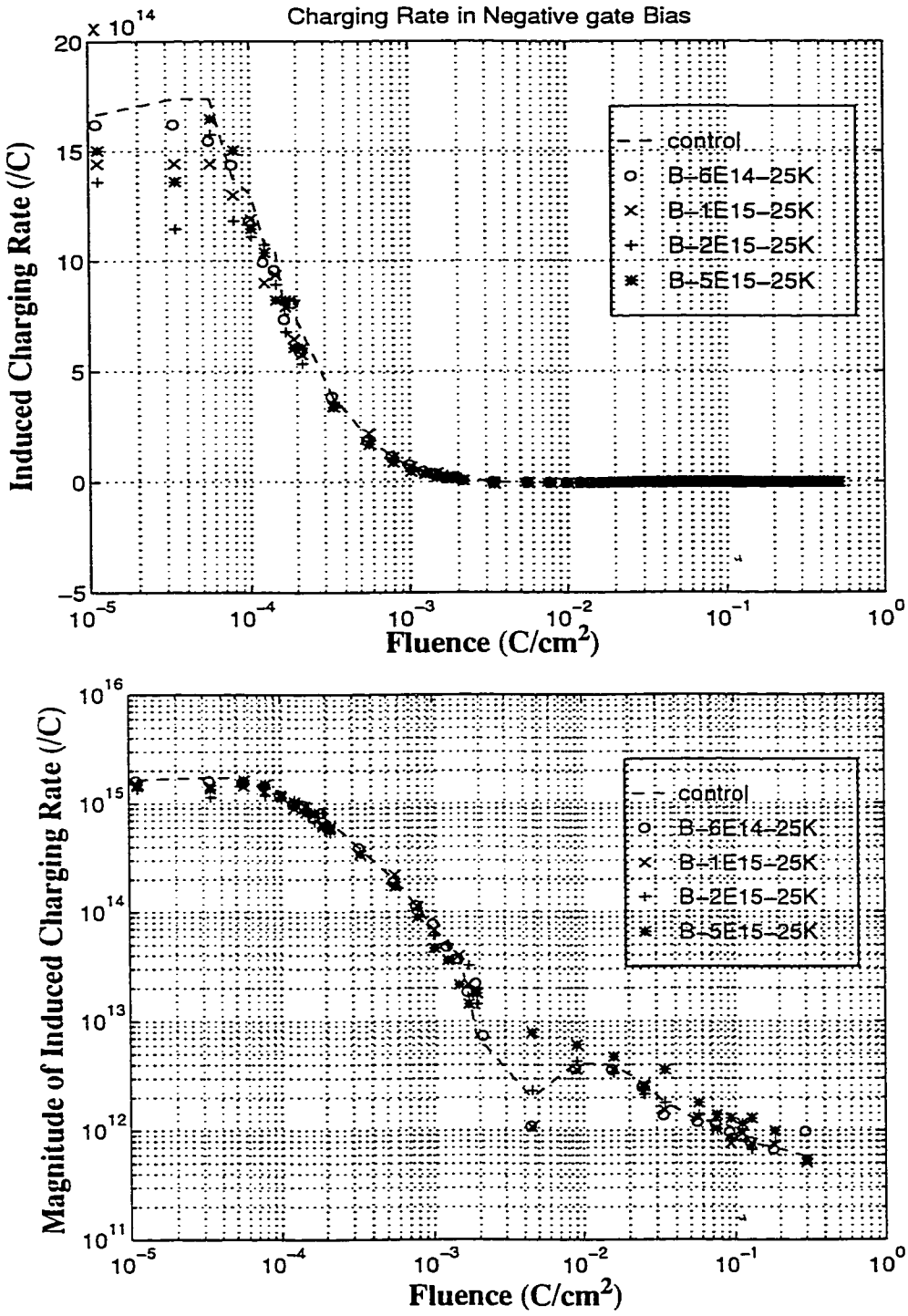


Fig. 5.22 - Induced Charging Rate of the Fluorinated samples under (-) FN stress, both in a) semilog plot, and b) log-log plot.

5.2.2 Summary of (-) Bias Data

Some conclusions can be drawn:

During (-) gate bias CCFN stress, the excessive amount of fluorine at the perimeter of MOS capacitors at the Si/SiO_2 interface appears to reduce the advantage of F-incorporation into the Si/SiO_2 interface. The results are consistent with the (+) gate bias results. The quality degradation caused by excessive fluorine atoms at/near the Si/SO_2 interface supports the strain relaxation hypothesis.

Under (-) gate bias CCFN, in $N_{\Delta V_g}(f)$-, fluorinated oxides show a tendency that the higher fluorine-implanted doses yield fewer hole traps at low fluence in the bulk oxide outside a tunnelling distance from the poly/SiO_2 interface.

Under (-) gate bias CCFN, in $N_{\Delta V_g}(f)$-, fluorinated oxides show fewer electron traps than the control at high fluence in the bulk oxide outside a tunnelling distance from the poly/SiO_2 interface. But the variation is not systematic among the fluorinated oxides.

A large amount of positive charge builds-up at/near the poly/SiO_2 interface under a (-) CCFN at low fluence. However, there is no systematic variation observed for electron trap generation. Perhaps, here is the disadvantage of fluorination under (-) CCFN.

In aspects of induced charging rate such as parameter K_1, K_2, hole trapping rate, the fluorinated cases are not always better than the control, except the dose $2x10^{15}$ /cm^2. The fluorine implant dose $2x10^{15}$ cm^{-2} at 25KeV appears to be an optimal dose.

5.3 (+) Bias vs. (-) Bias

5.3.1 The Si/SiO_2 Interface State Distribution

One noteworthy observation is that under (+) gate bias, in Fig. 5.1(b) (after a fluence of $2.5x10^{-2}$ C/cm^2), the values of midgap interface state densities are ~$1x10^{12}$ eV^{-1} cm^{-2} while under (-) gate bias, in Figs. 5.17 and 5.18 (after a fluence of $2.3x10^{-2}$ C/cm^2) the obtained values of midgap interface state densities are now around $5x10^{11}$ $eV^{-1}cm^{-2}$. We can say that (+) CCFN generates more interface states than (-) CCFN.

This observation might be explained by the DiMaria model. As shown in Fig. 2.3, under (+) bias CCFN, interface states are partly caused by the mechanism in which hydrogen atoms are released from the poly/SiO_2 interface to form interface states at the Si/SiO_2 interface. However, under (-) gate bias, (in Fig. 2.4), hydrogen atoms are now released from Si/SiO_2 interface to form states at the poly/SiO_2 interface states. Therefore, there should be a substantial reduction in the Si/SiO_2 interface states generated under (-) gate bias CCFN.

Next, the existence of two fluorine peaks in the SIMS profiles [15], discussed in Section 2.2.1.2, means that there is an increase in the number of Si-F bonds at both interfaces, which are more difficult to break. Therefore, less mobile (hydrogen) atoms are released from the anodes to form interface states at the cathodes. If this is true, then the fluorinated cases should show better performance than the control. Both Figs. 5.1(d) and 5.17 support this conclusion. Furthermore, the inset in Fig. 5.17 shows that there is an optimal dose, in this respect which is $2x10^{15}$ cm^{-2}.

Another interesting fact is that data from both (-) and (+) gate bias show that with an excessive amount of fluorine at the Si/SO_2 interface, the performance of fluorinated oxides is worse (see Section 5.1.2.3 and 5.2.1.1). Presented data for the Si/SiO_2 trapped charges and interface states in both (-) and (+) gate biases support the validity of the strain relaxation, proposed by Ma [14] and Wright and Saraswat[15].

5.3.2 ΔV_{fb} Charging Curves

ΔV_{fb} charging curves in Figs. 5.5(a) and 5.19, for fluorinated oxides, are used to compare the induced charges, $N_{\Delta Vfb}(f)$. In all cases, substantially more charges (~5 times more) are induced by (-) bias than by (+) bias. Also, overall positive charging regimes (corresponding to shifts to the left in ΔV_{fb}) extend to much higher fluences in the (-) bias cases than in the (+) bias cases. In (-) bias, the oxides are charging positively at $f > 10^{-2}$ C/cm^2, while in (+) bias they are already charging negatively at $f \sim 3\text{x}10^{-3}$ C/cm^2. These overall differences between the (-) and (+) bias cases are in general accord with the experimental observations of DiMaria *el al* [43] for thermal oxides. In both positive bias and negative bias, the data for the fluorinated cases is clustered near the data for the control oxide, with the highest F-dose yielding the maximum net positive charging [80].

5.3.3 ΔV_g Charging Curves

ΔV_g charging curves, in Figs.5.5 and 5.20, compare the charge $N_{\Delta Vg}(f)$, induced by positive [78] and negative [80] gate bias CCFN stressing in the fluorinated, and control cases. Similarly to Ref. [43], the differences between the positive and negative cases are rather subtle, less dramatic than differences in $N_{\Delta Vfb}(f)$. In this work, the negative-bias

cases generally reach somewhat greater positive charging maxima, and have somewhat higher zero-crossing fluences. However, all the positive charging maxima in both (-) and (+) bias occur at a fluence ~1.9-2.3x10^{-3} C/cm^2. This could indicate that the induced positive charge under both (+) and (-) bias mainly comes from a set of trapped charge (having the same hole capture cross-section).

5.3.4 Relations Observed From Both ΔV_{fb}, And ΔV_g Charging Curves

Since the maximum positive charging reached in $N_{\Delta Vfb}$-, is substantially greater (~ 2 times greater) than the maximum positive charging reached in $N_{\Delta Vg}$-, it can be concluded that most of the positive induced charge, indicated by the positive charging regimes in Fig. 5.19, must be nearer to the poly/SiO_2 interface. If this were not true, $N_{\Delta Vg}$- would be much higher than it is, since $N_{\Delta Vg}$- is less sensitive than $N_{\Delta Vfb}$- to charges near the poly/SiO_2 interface [43, 80]. Fig. 5.21 shows quantitatively the number of charge locating near/at the poly SiO_2 interface.

Also, in (-) bias, the $N_{\Delta Vg}$- curves all reach their maximum positive charging at fluences < 5x10^{-3} C/cm^2 (see Fig. 5.20), while the $N_{\Delta Vfb}$- curves all reach their maximum positive charging at fluences > 10^{-2} C/cm^2 (see ΔV_{fb} charging curves in Fig. 5.5(a)). This confirms that the positive charging observed in $N_{\Delta Vg}$- is not simply a less-sensitive result of the *same* positive charging as observed in $N_{\Delta Vfb}$-. Thus, the variations in $N_{\Delta Vfb}$- are likely to be due to variations in a different set of charges, probably nearer to the poly/SiO_2 interface, and perhaps having different (smaller) capture cross-sections [80]. This should be contrasted with the (+) bias results, where all the positive charge maxima occur at flu-

ences about $2x10^{-3}$ C/cm^2, likely since both $N_{\Delta Vg}$+ and $N_{\Delta Vfb}$+ are sensitive to charges created outside of a tunneling distance from the Si/SiO_2 interface [78, 80].

Also in Table 5.2, the total defects caused in (-) CCFN stress are slightly less than five times those generated in (+) CCFN. In (+) bias configurations, the optimal implanted-dose could be from $1\sim2x10^{15}$ cm^{-2}. The trends in (-) CCFN is that the higher fluorine-implanted dose, the fewer the hole traps generated at low fluence. Overall, the data in Table 5.2 (right-most column), suggest that while the fluorination process can give some advantages in the (+) bias case, these good effects are cancelled when hot electrons are injected from the gate ((-) bias), due to many trapped charges formed at/near the poly/SiO_2 interface.

5.3.5 Charging Rate Aspects

Figs. 5.11 and 5.22, and Table 5.3 summarize the derived charging rates. The magnitudes are greater in (-) bias. The optima (minima) in both positive and negative charging appear to be at slightly different doses (more clearly $2x10^{15}$ than in (+) bias).

The two main parameters of interest are low-fluence hole trapping rate, and rate of change of trapping rate K_1. For the control, the hole trapping rate at low fluence is significantly greater in (-) bias than in (+) bias. On the other hand, K_1 is only slightly more severe in (-) bias. For most of the fluorinated cases (-) bias values are more severe than (+) bias values. Note that, in either bias case, $2x10^{15}$ cm^{-2} is still maintained as the optimal dose [80].

This could be due to variation in the position of the fluorine in the SiO_2 layer. Ref. [15] showed that the implanted F may have a somewhat higher concentration near the poly/SiO_2 interface. The highest doses yield both the most severe K_I and a high hole trapping rate. This is consistent with the possibility that the higher doses of fluorine may end up with more fluorine-concentration near the poly/SiO_2 interface [80].

5.3.6 Summary of (+) And (-) Bias Comparisons

Negative bias CCFN yields fewer interface states at the Si/SiO_2 interface than positive bias. However, the study of the behavior of before- and after-poly-etch pairs in both positive and negative gate bias proves that the extra amount of fluorine introduced to the perimeter of MOS capacitor at the Si/SiO_2 interface is a source of degradation of the performance of gate oxides. This result supports strongly the strain relaxation hypothesis.

Negative bias CCFN stressing yields quite different charging behavior from positive bias, in the fluorinated and control oxides. Analyses of $N_{\Delta Vfb}$ and D_{it} in the (-) bias case show that enhanced positive charging in the control, and fluorinated cases is not represented in D_{it}, but is located at/near the poly/SiO_2 interface.

The set of negative bias induced positive charges generated near/at the poly/SiO_2 interface could have a smaller capture cross-section than the induced positive charges in the bulk ($N_{\Delta Vg}$-). This is contrasted with the positive bias results, where all the positive charge maxima occur at almost the same fluences, i.e the same capture cross-section for all positive induced charge in positive gate bias.

$2x10^{15}$ /cm^2 is still found to be the optimal dose [78, 80] for both positive and negative biases in the aspects of trapping rates. High fluorine doses may lead to somewhat degraded bulk charging characteristics. The variations are consistent with higher F-doses being found near to the poly/SiO_2 interface.

5.4 Chapter 5 Contributions

An extensive study of fluorine incorporation into gate oxides was planned and executed. The study was done using both positive and negative gate bias CCFN. The study showed the complex scenario of charge components generated in different locations in gate oxides in both (+) and (-) gate biases.

This study extends the knowledge base of fluorinated gate oxides in the following specific points:

- Under positive gate bias, hole trapping in the bulk oxide does not vary significantly due to fluorination. For electron trapping, greater implanted dose leads to lower electron trapping in the bulk.

- Under positive gate bias, higher implanted fluorine dose leads to more negative trapped charges at the Si/SiO_2 interface.

- In accord with the pilot study in Chapter 4, under positive gate bias, the slow donor states or anomalous positive charge are reduced or suppressed by the fluorination process. Possible optimum dose could be in the range between $6x10^{14}$ /cm^2 to 10^{15} /cm^2.

● After-poly-etch implants, while yielding more fluorine at the interface, lead to more electron trapping underpositive gate bias. The extra amount of fluorine reduced the suppression of the slow donor states in fluorination. This is evidence supporting the strain relaxation hypothesis, proposed by Ma [14] and Wright and Saraswat [15]

● Under negative gate bias, the study of the effect of fluorine on D_{it} proves that the appearance of more fluorine at the interface reduces the advantage of the fluorination process. And again this supports the strain relaxation hypothesis.

● Under negative gate bias CCFN, high fluorine dose leads to fewer hole traps which are located outside a tunnelling distance from the poly/SiO_2 interface. But electron traps located outside a tunnelling distance from the poly/SiO_2 interface, does not show a systematic variations.

● Under negative gate bias CCFN, a large amount of positive trapped charge is induced at/near the poly/SiO_2 interface. The set of negative bias induced positive charges generated near/at the poly/SiO_2 interface could have a smaller hole capture cross-section than the induced positive charges in the bulk ($N_{\Delta Vg}$-) [80]. This is contrasted with the positive bias results, where all the positive charge maxima occur at almost the same fluences, i.e the same capture cross-section for all positive induced charge in positive gate bias.

● $2x10^{15}$ /cm^2 is found to be the optimal dose [78, 80] for both positive and negative biases in the aspects of the rate of change of the charging rate, saturated charging rate, and induced charging rate.

However, in general, fluorinated samples still show advantages on the control sample. The effects usually do not show up as clearly as they have shown in the pilot study, in

Chapter 4. This confirms and reminds us of the truth that the impact of any variation on a complete fabrication process can be both subtle and complex. The advantages which fluorination gains in an abbreviated process can be at least partly cancelled out by steps in the back-end process.

CHAPTER 6

OXYNITRIDATION IN GATE OXIDES CHARACTERIZED BY FOWLER-NORDHEIM INJECTION STRESS

6.1 Electrical Characterization of Oxynitrided Gate Dielectrics Under Positive Gate Bias Constant Current Fowler-Nordheim Stress.

The devices in this study were fabricated as shown in Section 4.1.2.2. Note that the oxide thickness in this case varied monotonically with reoxidation temperature from 248Å to 268Å. In this Chapter, the electrical characterization plan is the same as the one used in Chapter 5. Analysis of oxide-traps during constant-current Fowler-Nordheim stress uncovers complex phenomena in oxide-trap creation. Several features of the data indicate an optimum at an oxynitridation temperature of 850°C-950°C; including initial net-positive oxide-trap creation, and changes in rates of oxide-trap creation.

Because the number of samples is fewer, the results and discussion are presented simultaneously. The order of presentation is the same as in Chapter 5, i.e starting from the interface state distribution, then $N_{\Delta Vfb}$, $N_{\Delta Vg}$, and N_{ic}.

6.1.1 Results And Discussion

6.1.1.1 Interface States Density, D_{it}:

Fig.6.1 shows the evolution of interface trap densities at midgap, as a function of injected fluence, for the oxynitride family and the control. Before any applied electrical stress (at $f = 0$), the trap densities in the oxynitrided cases are grouped, slightly above those of the control case (about 1-3x10^{10} $eV^{-1}cm^{-2}$ above the control). An injected fluence of 2.5x10^{-2} C/cm^2 causes >10^{11} $eV^{-1}cm^{-2}$ interface trap densities to be generated in all cases. However, it is obvious that the oxynitrided cases have incurred substantially less D_{it} than the control sample. Furthermore, it is clear that the oxynitrides follow a pattern: *the higher the oxynitridation temperature, the lower the interface trap density at midgap.* At the very high fluence of 2.2x10^{-1} C/cm^2, samples oxynitrided at temperatures ≥ 950°C still have midgap D_{it} less than 10^{12} $eV^{-1}cm^{-2}$, while the control has a midgap D_{it} greater than 2x10^{12} eV^{-1} cm^{-2}.

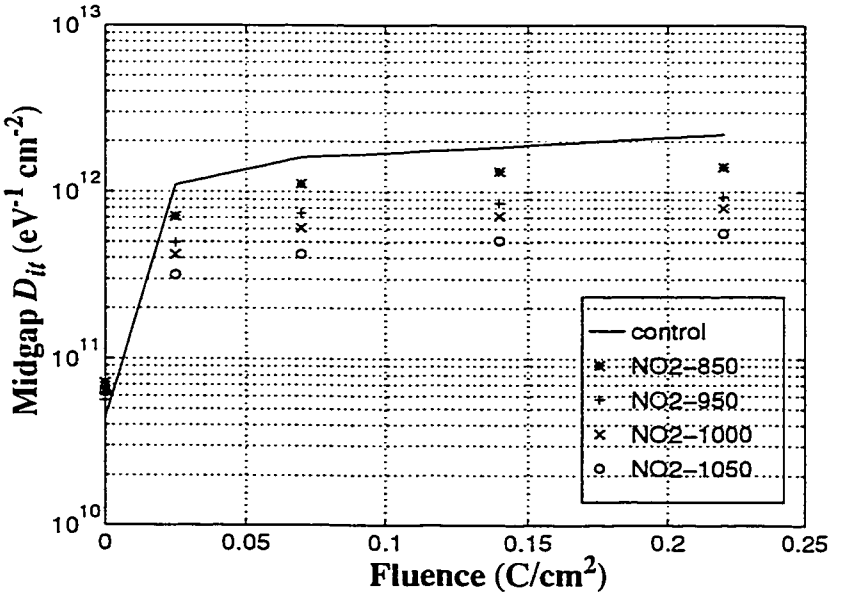


Fig. 6.1 - Interface trap density at midgap, for oxynitrides and control oxides, as a function of injected fluence.

Figs 8.2(a)-(e) chart the distributions of interface trap densities with increasing fluence, for the oxynitrided family. These distributions show that the control case incurs more and more interface traps with increasing fluence, while the distributions for the oxynitrided cases have not changed much after $f = 7.0 \times 10^{-2}$ C/cm^2. It should also be noted that, in the control case, the degradation is even worse, 0.1 - 0.3 eV below midgap, while this is not observed in the N-cases [79].

The behavior of interface state distribution, D_{it}, (in Fig. 6.1, before and after CCFN stress), is consistent with previous studies. Before any CCFN, the oxynitrides have a slightly higher D_{it} than the control oxide (see Fig. 8.2 (a)). This is in agreement with Yankova *et al* 's work [18]. After a certain injected charge, D_{it} of the oxynitrides is always smaller than D_{it} of the control oxide. [32, 33, 69]

The semi-empirical model of Hori *et al* [31] is applicable to explain these phenomena. According to the model [31], the nitrogen (N) atoms at the Si/SiO_2 interface[8], are likely to be inert and don't contribute significantly to trap generation during CCFN stress. On the other hand, the concentration of hydrogen (H) atoms at the Si/SiO_2 interface[9], are likely to be more active, and are related to the creation of large numbers of electron traps during CCFN stress [43, 70]. The model further asserts that the oxynitridation process reduces C_H and increases C_N. Further, the results of SIMS analysis from Hori *et al* [31] and Okada *et al* [65] show that higher oxynitridation temperatures and times lead to higher C_N and lower C_H.

8. Denoted C_N
9. Denoted C_H

Our results shown in Figs. 6.1 and 8.2 are consistent with the above described findings, since all of our oxynitridations had the same time of 30 minutes. At this constant process time, the higher the oxynitridation temperature, the lower the post-stress D_{it} of our oxides during CCFN stress, consistent with higher C_N and lower C_H (at the Si/SiO_2 interface).

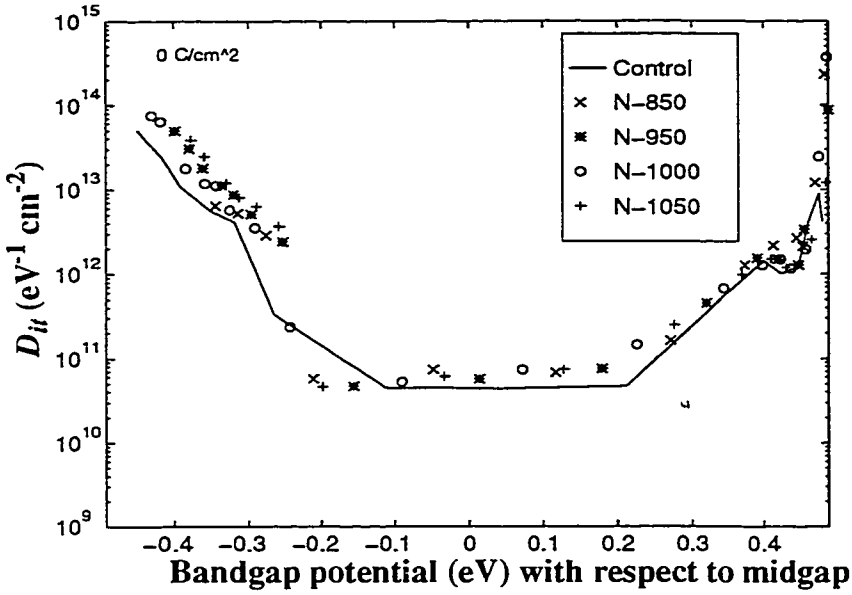


Fig. 6.2- (a) D_{it} vs. bandgap energy, at pre-stress, 0 C/cm^2.

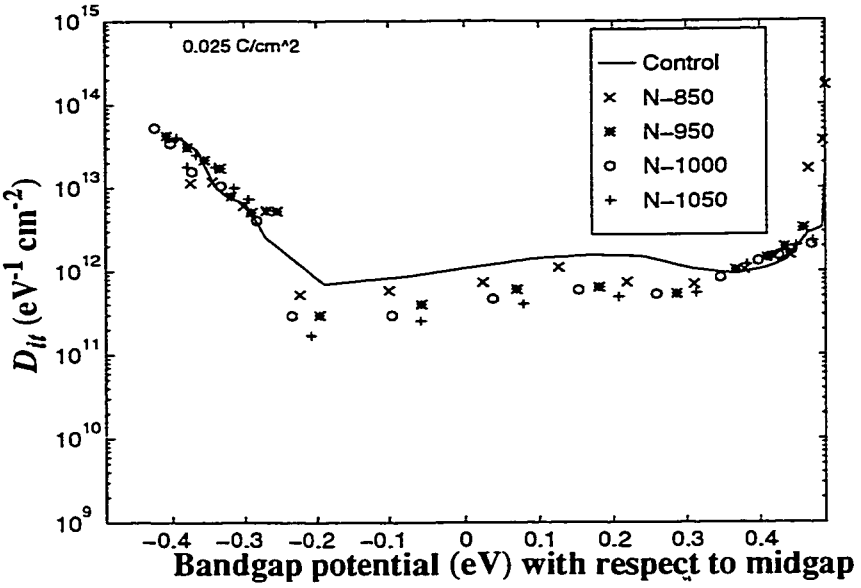


Fig. 6.2 - (b) D_{it} vs. bandgap energy after a positive gate bias FN stress, $f = 2.5 \times 10^{-2}$ C/cm^2.

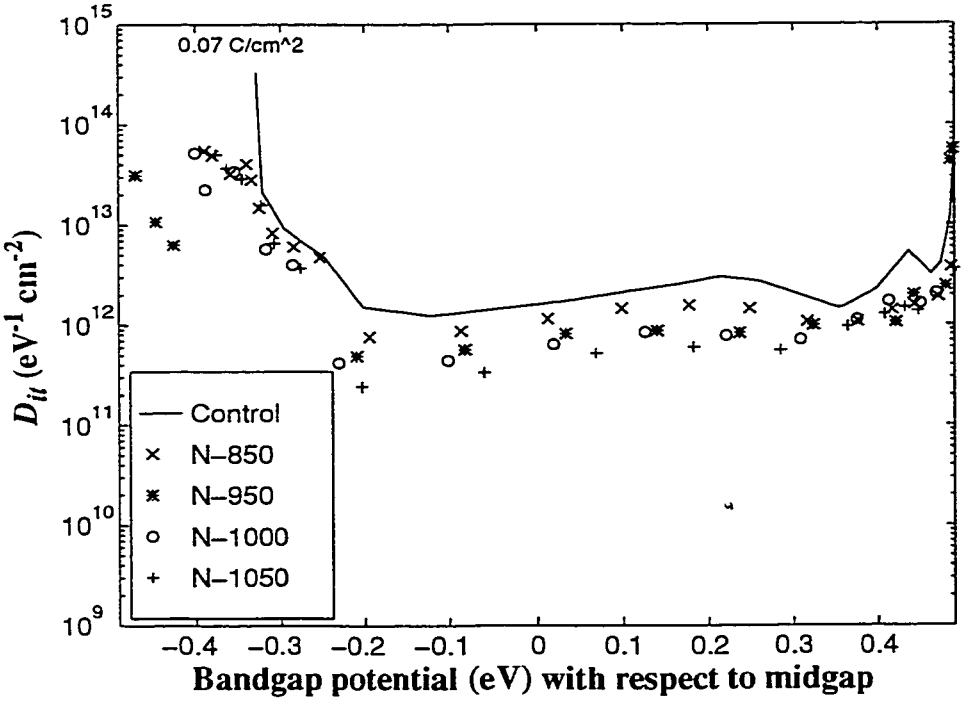


Fig. 6.2 - (c) D_{it} vs. bandgap energy after a positive gate bias FN stress, $f = 7.0 \times 10^{-2}$ C/cm^2.

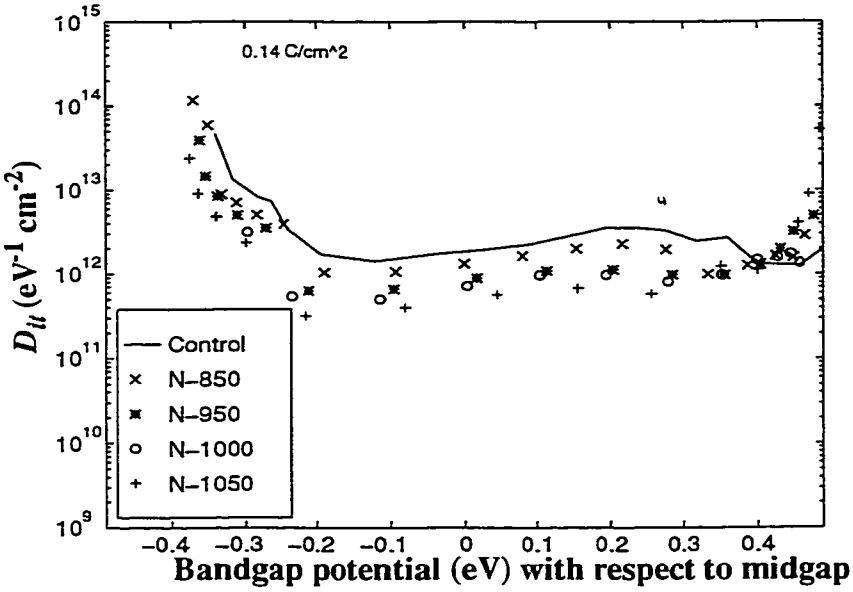
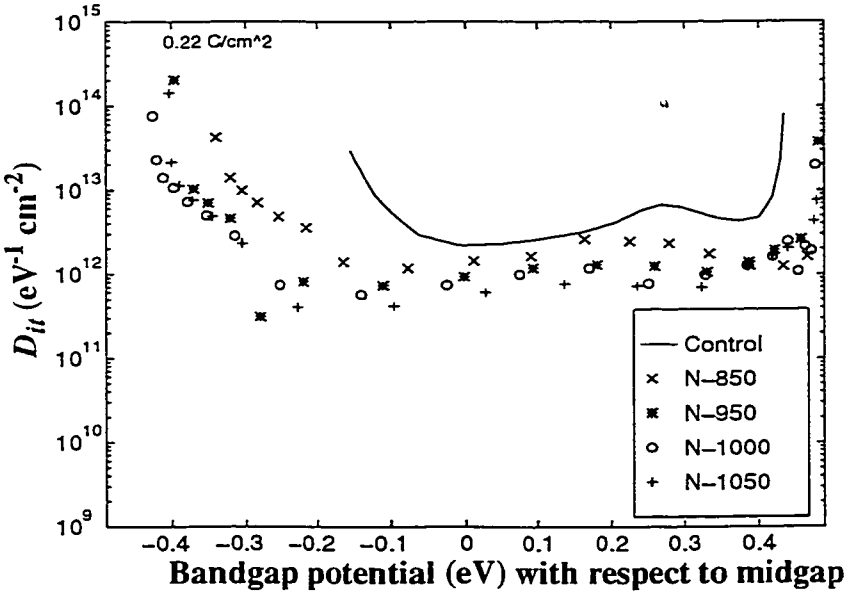


Fig. 6.2 - (d) D_{it} vs. bandgap energy after a positive gate bias FN stress, $f = 1.4 \times 10^{-1}$ C/cm^2.



(d) D_{it} vs. bandgap energy after a positive gate bias FN stress, $f = 1.4 \times 10^{-1}$ C/cm^2.

Fig. 6.2 - e) D_{it} vs. bandgap energy after a positive gate bias FN stress, $f = 2.2 \times 10^{-1}$ C/cm^2.

6.1.1.2 ΔV_{fb}, And ΔV_{fb} Charging Curves:

Fig. 6.3 shows examples of the evolution of ΔV_{fb} for the oxynitrided family and the control oxide, during a CCFN stress with a constant current density of 2.36×10^{-4} A/cm^2. The ΔV_{fb} measurements were done at certain intervals. While at low fluence (less than about 3×10^{-2} C/cm^2), it is difficult to distinguish the oxynitrided cases from the control case, at high fluence the oxynitrided cases exhibit noticeably lower ΔV_{fb}. The highest oxynitridation temperature clearly yields the lowest ΔV_{fb}. Fig. 6.3 is in general accord with the results of other researchers [31, 41]. Fig. 6.4 shows the set of charging curves, calculated from ΔV_{fb} in Fig. 6.3 for the oxynitrided family. The net charge calculated from ΔV_{fb} varies oppositely (from (+) to (-), from the data shown in Fig. 6.3, since *negative* V_{fb} shifts correspond to *positive* charge in the oxide.

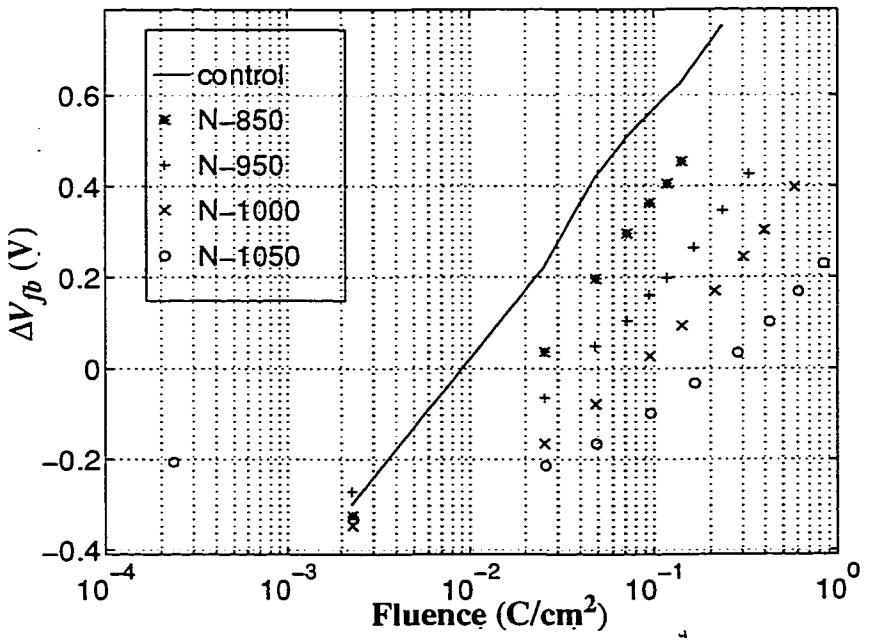


Fig. 6.3 - Flatband voltage shifts, ΔV_{fb}, for oxynitrides vs. fluence of hot electrons injected from the substrate. Control oxide ΔV_{fb} curve is included for comparison.

The highest flatband voltage shift of nearly 800 mV is observed in the control case when the fluence is about $2.2x10^{-1}$ C/cm^2. If ΔV_{fb} were used as an overall measure of reliability, the most reliable oxide of this set would be oxynitrided at 1050°C, which has a flatband voltage shift of only 220 mV at a fluence near 1 C/cm^2. In Figs.6.4 it is clear that, *the higher the oxynitridation temperature, the slower and the lower is the net negative charge build-up in oxynitrides.*

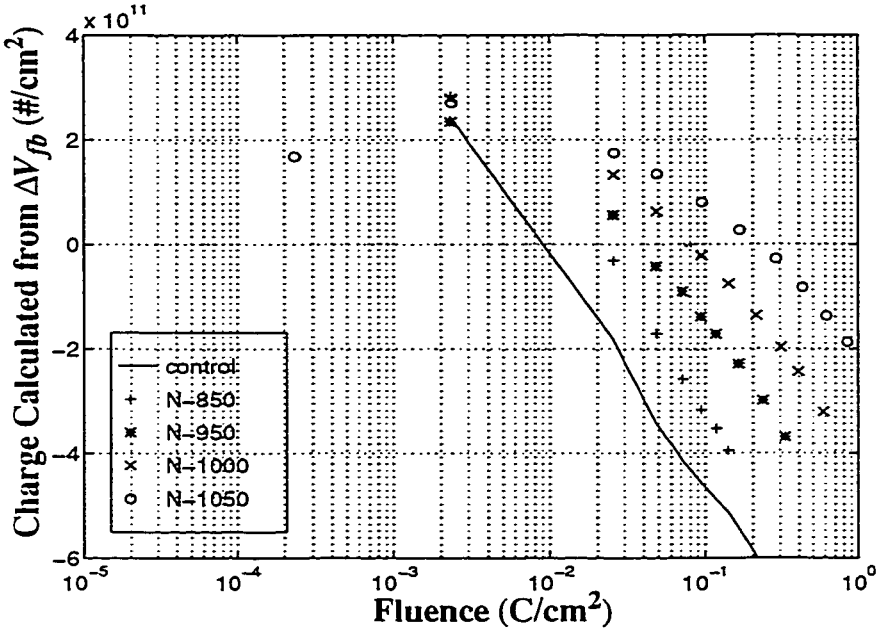


Fig. 6.4 - Set of ΔV_{fb} net charging curves, extracted from flatband voltage shifts (in Fig. 6.3) for oxynitrides (including the control oxide for comparison) under positive gate bias at a constant current density of $2.36x10^{-4}$ A/cm^2.

6.1.1.3 ΔV_g And Net Trapping Rate In The Bulk:

Fig. 6.5 shows charging curves calculated from ΔV_g. These represent charging in the bulk, more than a tunnelling distance away from the Si/SiO_2 interface. The variation in bulk trapped charge exhibits various stages: (i) an initial increase in trapped positive

charge, (ii) the attainment of a maximum net positive trapped charge (at about 2.2 - 2.3 $x10^{-3}$ C/cm^2), (iii) a shift from net positive to net negative trapped charge (attained at about $7x10^{-2}$ C/cm^2 for the control case and at about 0.1-1.0 C/cm^2 for the oxynitrided cases), as electron trap creation becomes dominant, (iv) increasing net negative trapped charge, which usually continues [43, 44, 77] until breakdown. These tests were usually terminated before breakdown occurred. The control case exposes the lowest maximum net positive charge, while the oxynitride with the lowest N_2O treatment temperature (850°C) exhibits the highest maximum net positive charge. Table 6.1 summarizes these variations. The zero-crossing fluence exhibits a systematic variation in that the higher the oxynitridation temperature, the higher the zero-crossing fluence.

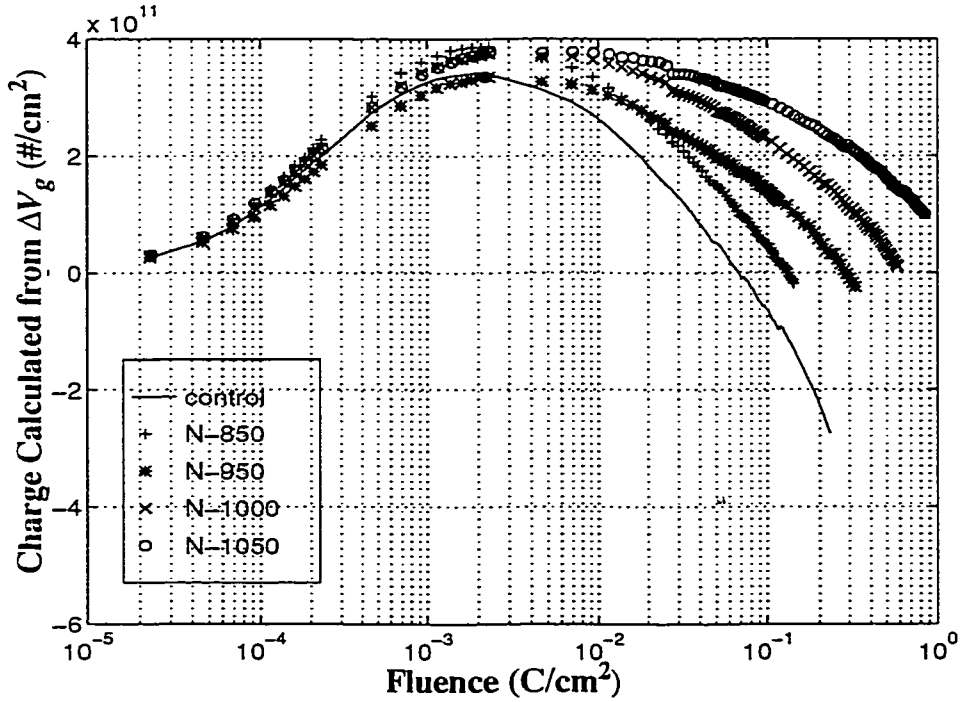


Fig. 6.5 - Set of ΔV_g net charging curves extracted from gate voltage shifts for oxynitrides (including the control oxide for comparison) under positive gate bias at a constant current density of $2.36x10^{-4}$ A/cm^2.

In addition to the above features, information about the net *trapping rate* is available from charging curves. $N_{\Delta V_g}$ vs. f data was converted into trapping rate $\Delta N_{\Delta Vfb}/\Delta f$ between successive pairs of data points. Fig. 6.6 shows derived curves for the entire oxynitride family. Note that unsigned magnitudes are plotted in this log-log format. Note also that the data has been smoothed in the range $f \geq 5\text{x}10^{-3}$ C/cm^2 to reduce noise and the other measurement artifacts [79].

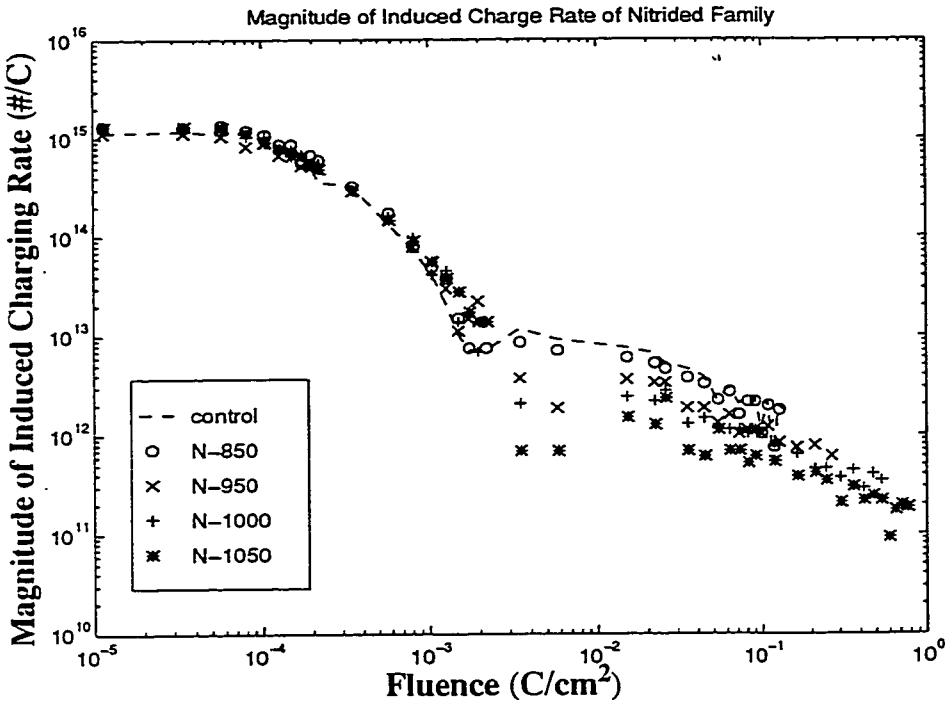


Fig. 6.6 - Unsigned magnitude of induced net charge rate, extracted from the Fig. 6.5 ΔV_g net charging curves for oxynitrides (including the control case). These curves indicate the induced net charging rates are functions of injected charge. Notice that the curves are smoothed at high fluence (f >5x10^{-3} C/cm^2)

Fig.6.7 and its inset were prepared to show typical semilog plots for the charging *rate* calculated from ΔV_g charging curves. From Fig. 6.7, it is clear that the net charging rate has evolved through the following stages. (i) high and relatively constant net positive

trapping rate, indicative of hole trapping dominance up to about 10^{-4} C/cm^2; (ii) rapid reduction in net positive charging rate, (this stage, from appr. 10^{-4} C/cm^2 to appr. $5x10^{-4}$ C/cm^2, indicates a rapid increase in electron trapping rate or a rapid decrease in hole trapping rate, or both); (iii) net charging rate approaches zero and crosses zero (from appr. $5x10^{-4}$ to appr. $3x10^{-3}$ C/cm^2); (iv) from the extreme of net negative charging rate at 1-10^{12} /C, the negative charging rate decreases; and (v) after about 10^{-1} C/cm^2, the net charging rate continues to decrease below 10^{12} #/C.

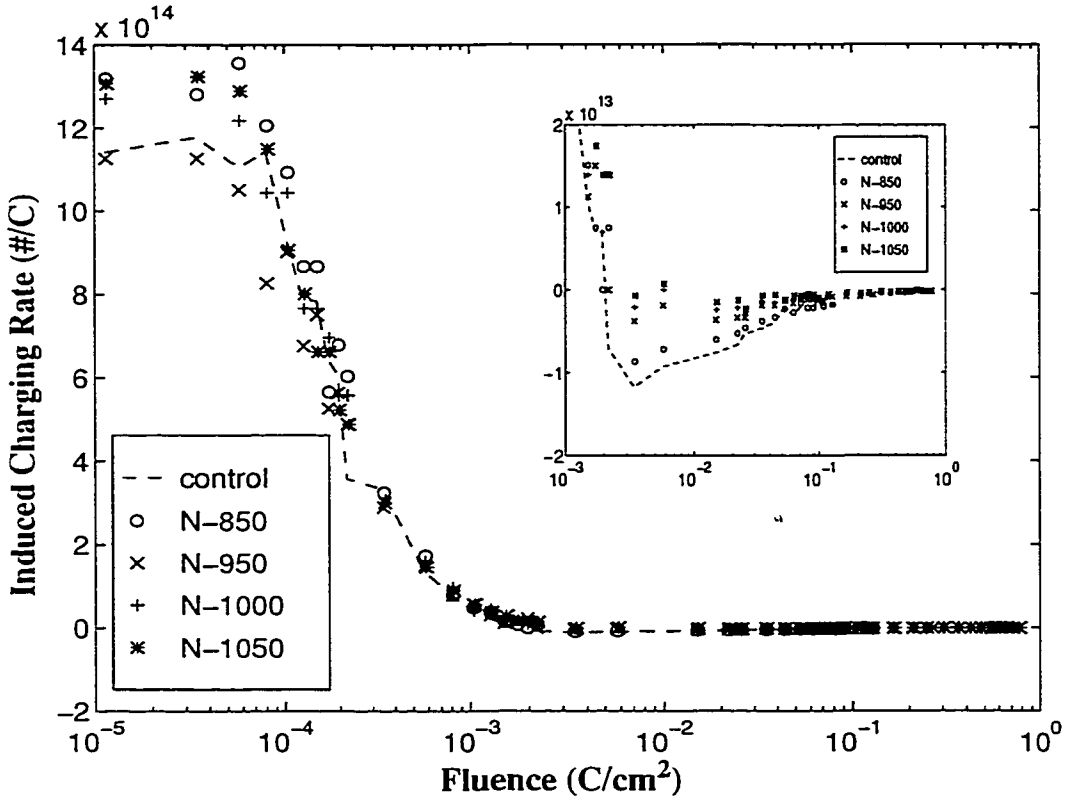


Fig. 6.7 - Semilog plots for net charging rate extracted from the Fig.6.5 ΔV_g net charging curves for oxynitrides (including the control case). The inset re-displays (magnified) the portion of the curves at high fluence, where the induced net charging rate switches from positive to negative.

The linear-log format shows in all cases a fairly straight-line portion of each curve from about 10^{-4} to about $5x10^{-4}$ C/cm^2. This portion can be modeled following Eq. 3.3 [78, 79]:

$$\frac{d}{df}\left(N_{\Delta V_g}\right) = K_1 log_{10}(f) + K_2$$

where K_1 and $K_2 < 0$. The thus-extracted K_1, K_2 are also included in Table 6.1. The curves for ΔV_g in Fig.6.5, and the derived trapping rates in Figs.6.6 and 6.7 and Table 6.1 deal with trap generation in the bulk oxide, more than a tunnelling distance away from the interface. In accord with DiMaria *et al*'s model [43], charging curves such as Fig. 6.5 are affected by complicated phenomena, in several stages, depending on the amount of injected charge [78, 79]. The net positive charge build-up at $f < 10^{-3}$ C/cm^2 is evidence of hole trapping at low fluence due to impact ionization. The subsequent reduction of net positive charge when $f > 2.2x10^{-3}$ C/cm^2, is evidence of a rapid increase in electron trapping or a rapid decrease in hole trapping, or both [79]. In this regime, the net trapping rate appears to be decreasing proportionally to the logarithm of the injected fluence, in accord with a first-order charging kinetic model of Roh *et al* [55]. This indicates an "*acceleration*" of electron trapping and/or a "*deceleration*" of hole trapping. If the model [55] is believed then hole trapping stays relatively constant, at $f > 10^{-4}$ C/cm^2 while electron trapping increases rapidly after this (in stage (ii)) of Fig. 6.7). Eventually, in stage (v) of Fig.6.7, electron trapping becomes slightly greater than hole trapping.

The following main trends can be observed in Table 6.1, and Figs. 6.5-6.7:

- The maximum net (+) charge occurs at approximately the same fluence (2.1-2.3x10^{-2} C/cm^2) for all cases.

• The net (+) charge maxima for the oxynitride cases are generally slightly higher than the control case (with isolated exception in the N-950 case). This suggests the possibility of an optimum N_2O treatment temperature, likely between 850°C-950°C, at which the lowest net (+) charge maximum might be obtained.

• Fig.6.7 shows that the hole trapping rate of every oxynitrided case, at a low fluence of ~$2x10^{-5}$ C/cm^2, is substantially higher than the control, except for the N-950 case. Thus in the range of 850°C-950°C, there is an oxynitridation temperature such that the low-fluence hole (positive) trapping rate is the lowest. Of course, this is consistent with the lowest net (+) charge extremum.

• The zero-crossing fluences also tend to vary systematically. In Fig. 6.5, for all the oxynitrided cases, the zero crossings occur at higher fluence than the control oxide. The tendency is: *the higher the N_2O treatment temperature, the higher the zero-crossing fluence.*

• Regarding the trapping rates, K_1 and K_2 for all oxynitrides are substantially lower than K_1 and K_2 for the control case. The sample N-950 has the lowest values of K_1 and K_2. This indicates that in the range of 850°C-950°C, there is an oxynitridation temperature such that the rate of change of (low-fluence) electron (negative) trapping rate in the bulk is the lowest.

• However, in stage (iv) of the evolution of the induced charging rate, there is no minimum or maximum at the 950 °C oxynitridation temperature. In this stage, the negative charging rate follows the simple pattern: *the higher the oxynitridation temperature, the less negative the net charging rate.*

Oxide	Max + position (10^{-3}C/ cm^2)	Max + value (10^{11}/ cm^2)	Zero-crossing Fluence (10^{-2} C/ cm^2)	Judgement from Zero-Fluence [i]	K_1 [ii] ($x10^{14}$)	K_2 ($x10^{14}$ #/C)	Hole Trapping rate at low fluence ($x10^{14}$#/ C)
Control	2.1	3.42	6.79	**Most L**	-15.6	-52.5	11.5
N-850	2.3	3.87	13.16	**LLLL**	-14.97	-49.2	13.5
N-950	2.3	3.35	28.48	**LLL**	-9.0	-27.9	11.2
N-1000	2.3	3.75	62.00	**LL**	-12.5	-40.5	13.0
N-1050	2.3	3.77	>100	**L**	-14.8	-49.2	13.3

i. **L** Refers to Left
ii. Dimension of K_1 is #/C per decade of fluence.

Table. 6.1 - Summary of Observations from ΔV_g vs. f curves.

6.1.1.4 (ΔV_{fb} - ΔV_g) Charging Curves:

Fig. 6.8 shows near-interface charge as a function of fluence, $N_{ic}(f)$, calculated from the curves in Figs. 6.4 -6.5 (ΔV_{fb} - ΔV_g). In each curve, the net interface charge is negative for all fluence levels tested. *The higher oxynitridation temperatures lead to less-negative $N_{ic}(f)$.* In each oxynitrided case, the net interface charge becomes more negative with increasing fluence. These features are consistent with the variations in D_{it} during CCFN (Figs. 6.1 and 8.2).

Another interesting feature of Fig. 6.8 is the turnaround in the control oxide curve at fluence greater than $6x10^{-2}$ C/cm^2. Only the control case exhibits such a turn around phenomenon, while the nitrided cases do not. The control curve reaches its most negative position at about $-4x10^{11}$ cm^{-2} at a fluence of ~$7x10^{-2}$ C/cm^2 (see Fig. 6.8). Such behavior

suggests the existence of "slow" donor states (donor states which become active after a relatively high fluence) or "anomalous positive charge" (APC) [55, 64, 76, 78]. These charges have been hypothesized to be caused by the presence of hydrogen atoms at the interface [43, 70]. Thus the reduction or elimination of the turnaround in the oxynitrided cases is again consistent with Hori *et al*'s model [31], where oxynitridation reduces hydrogen concentration at the Si/SiO_2 interface.

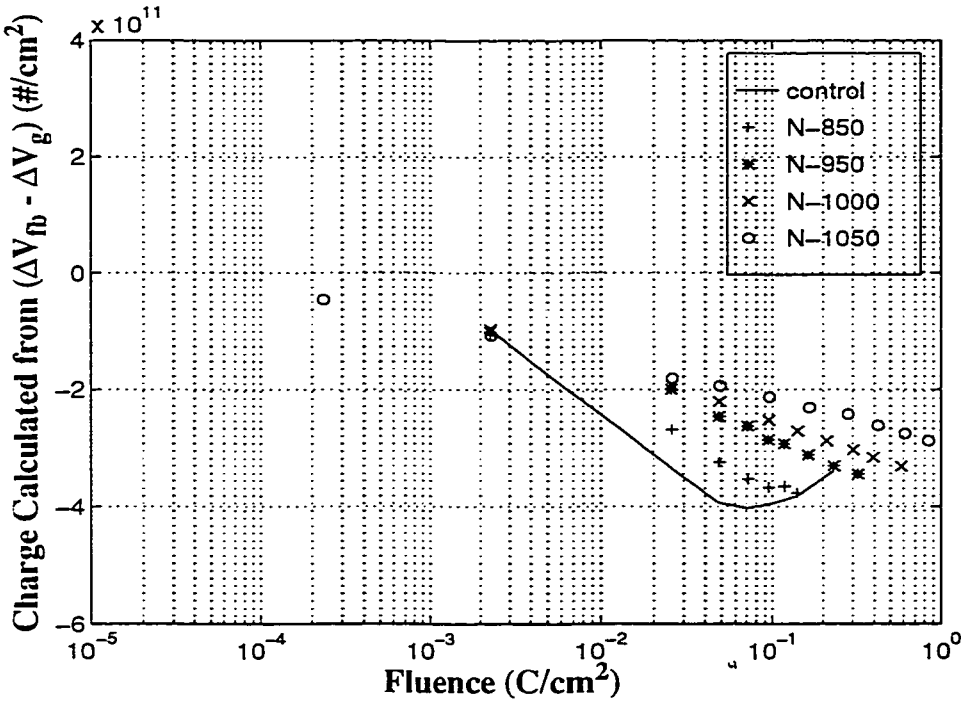


Fig. 6.8 - (ΔV_{fb} - ΔV_g) charging curves for oxynitrides calculated from the difference between flatband and gate voltage shifts.

Furthermore, in accord to this work, Belkouch *et al* [41] reported that the oxynitridation process enhances creation of trap levels at E_c-0.3eV and E_c-0.2eV at the Si/SiO_2 interface, while in the control case, there is only the existence of the trap level at E_c-0.3eV

at the interface. Ref. [41] shows that, the higher the oxynitridation temperature (i.e. higher nitrogen concentration at the Si/SiO_2), the higher the interface state density at the trap level E_c-0.2eV, while the interface states density at the trap level of E_c-0.3eV reduces. Thus according to Refs. [41] and [31], the accumulation of nitrogen at the Si/SiO_2 interface helps reduce the hydrogen concentration, (i.e reducing the interface state density at the trap level E_c-0.3eV); and helps increase the nitrogen concentration at the Si/SiO_2 interface,(i.e increase the interface state density at the trap level of E_c-0.2eV). The interface states at the trap level of E_c-0.2eV are less sensitive to electrical stress than the ones at the level of E_c-0.3eV [41]. This explains the systematic variation in oxynitridation in Fig. 6.8.

6.1.2 Summary of (+) Bias Data

By analysis of the charge components induced in gate oxides under (+) bias CCFN stress, a relatively comprehensive view of the dependences of oxynitrides on N_2O treatment temperature have been presented and discussed.

The occurrence of trap sites and interface trapped charge is reduced by N_2O treatment, especially at higher temperatures. This is found to be consistent with the semi-empirical model of Hori *et al* [31], related to the presence of hydrogen and nitrogen at the interface.

By application of the models of DiMaria *et al* [43], it becomes clear that several compensating effects in the bulk and interface yield the overall changes in flatband voltage. The main effects found are summarized as follows:

• Higher oxynitridation temperatures lead to fewer electron traps and lower electron trapping rate at the Si/SiO_2 interface. This is consistent with the D_{it}-based analysis above.

• Slow donor states (or "APC") appear at the interface at high fluence only in the control (thermal) case. There is no evidence to suggest that this phenomenon occurs in the oxynitrided cases.

• At low fluence, hole trapping in the bulk varies only moderately with oxynitridation temperature. Also, there may be an optimum oxynitridation temperature in the range of 850-950°C, in which the hole trapped charges and hole trapping rates are smallest.

• At low fluence, the rate of change of the electron trapping rate in the bulk appears to have an optimum at 850-950°C.

• At high fluence, higher oxynitridation temperatures are related to lower (better) electron trapping in the bulk, without any optimum at 850-950°C.

6.2 Electrical Characterization of Oxynitrided Gate Dielectrics Under Negative Gate Bias Constant Current Fowler-Nordheim Stress.

Following the same strategy as employed in Chapter 5, the measurement set-ups are the same as the ones in Section 6.1. However, for negative gate bias, a constant current density of -2.36×10^{-4} A/cm^2 is injected into the oxides from the gate.

6.2.1 Results and Discussion

6.2.1.1 The Interface State Densities, D_{it}

Fig. 6.9 shows the D_{it} vs. bandgap potential of samples in the oxynitrided family after a negative gate bias constant current Fowler-Nordheim stress. The plot proves that all the oxynitrided oxides have fewer generated interface states. It is also clear that the higher the re-oxidation temperature, the lower the density of interface states created. These results are consistent with Hori's model [31], for higher oxynitridation temperature has higher nitrogen concentration at the Si/SiO_2 interface.

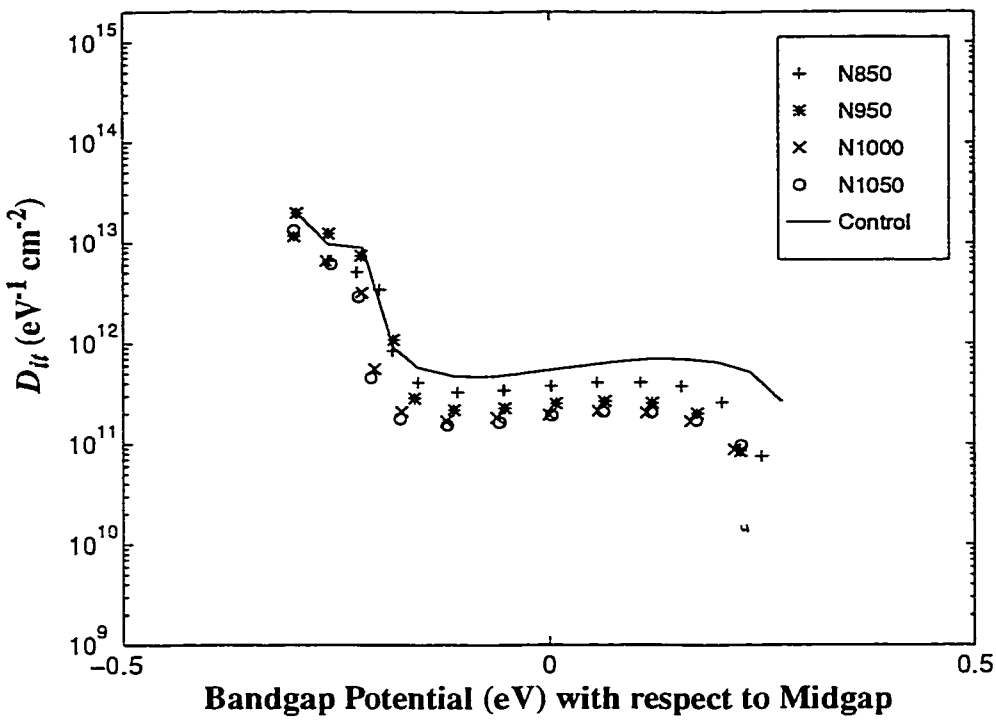


Fig. 6.9 - D_{it} vs. Bandgap potential for nitrided samples and the control oxides after an injected fluence of 2.3x10^{-2}C/cm^2 under (-) gate bias.

6.2.1.2 ΔV_{fb} Charging Curves

Fig. 6.10 shows the charging curves obtained from ΔV_{fb} in (-) CCFN. In Fig. 6.10, the evolution of overall charge is such that, at low fluence, net positive charge begins to build up, and reaches a net positive maximum at a fluence between 2x10^{-3} and 2x10^{-2} C/cm^2. Note that all the oxynitrided samples (compared to the control) exhibit lower net positive trapped charges at very low fluence (f~2.3x10^{-3} C/cm^2), but reach higher maxima at higher fluence (f~2.3x10^{-2} C/cm^2), except the N-1050 case. Thus, the low-fluence slopes of the evolution of trapped charge are steeper for the oxynitrided cases, indicating a higher positive trapping rate for all of the oxynitrided samples.

At fluences beyond the net charge maxima:

• The case N-850 has the steepest slope, (i.e. this sample has the most negative trapping rate).

• Cases, N-950 and N-1000, have very similar ΔV_{fb} charging curves, but demonstrate lower electron trapping rates than N-850 and control cases.

• The N-1050 case, however, maintains a net positive charge for a much greater range of fluence. In other words, the higher temperature (1050 ^{o}C) oxynitridation has dramatically reduced the electron trapping. The oxynitrided samples show a systematic variation in that, *the higher the re-oxidation temperature, the lower the electron trap creation.* Overall, N-1050 case is a very good oxide in terms of flatband voltage shifts.

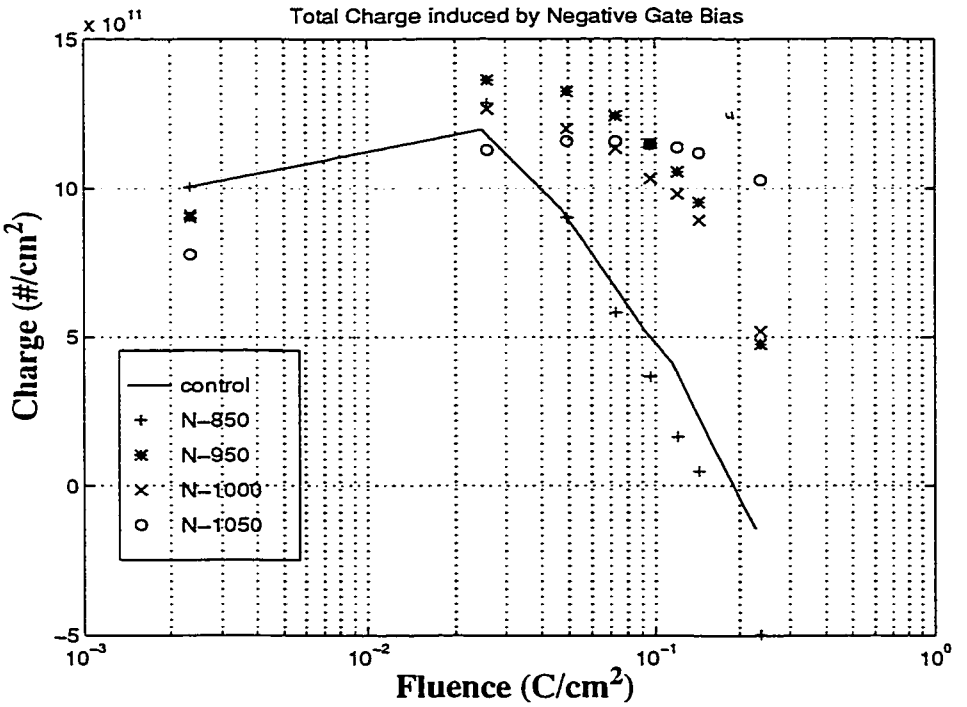


Fig. 6.10 - ΔV_{fb} Charging curves of oxynitrided oxides. Note that the induced charge maxima are in the order of 10^{12} /cm^2.

6.2.1.3 ΔV_g Charging Curves

Fig. 6.11 shows the ΔV_{fb} charging curves calculated from ΔV_{fb} in (-) CCFN. Fig. 6.11 displays that under (-) bias the overall net charge evolves through several stages: (i) build-up of the net positive trapped charge, (ii) attainment of positive maximum at a fluence ~2.3×10^{-2} C/cm^2, (iii) a shift from net positive to net negative trapped charge as electron trapping (electron trap creation or filling of electron traps having low capture cross-section), becomes dominant. These tests were usually terminated before breakdown occurred [80].

Fig. 6.11 displays the charging behavior in the bulk (excluding charges within a tunneling distance from the poly/SiO_2 interface). At low fluence ($f < 1 \times 10^{-3}$ C/cm^2) a systematic variation is observed among oxynitrided oxides. *The higher the re-oxidation temperature, the greater the hole trap creation.* Because the higher re-oxidation temperature implies that there is a higher nitrogen concentration in the bulk, and more at the Si/SiO_2 interface [31], the results might indicates that the oxynitridation is the cause for high induced hole traps in ΔV_g charging curves. However, the charging curve of the control is found between these oxynitrided curves (below N-1000, and above N-950). This indicates that lower oxynitridation temperatures are a better choice (than higher temperatures), if the oxynitridation is intended to improve hole trap creation in $N_{\Delta Vfb}$- (lower is better).

Fig. 6.11 shows that, after $f > \sim 8 \times 10^{-2}$ C/cm^2 the variation of electron trapped charges is systematic among oxynitrided cases. This may imply that higher oxynitridation temperature yields greater electron traps. However, the control curve is found between these oxynitrided curves (again, below N-1000, and above N-950).

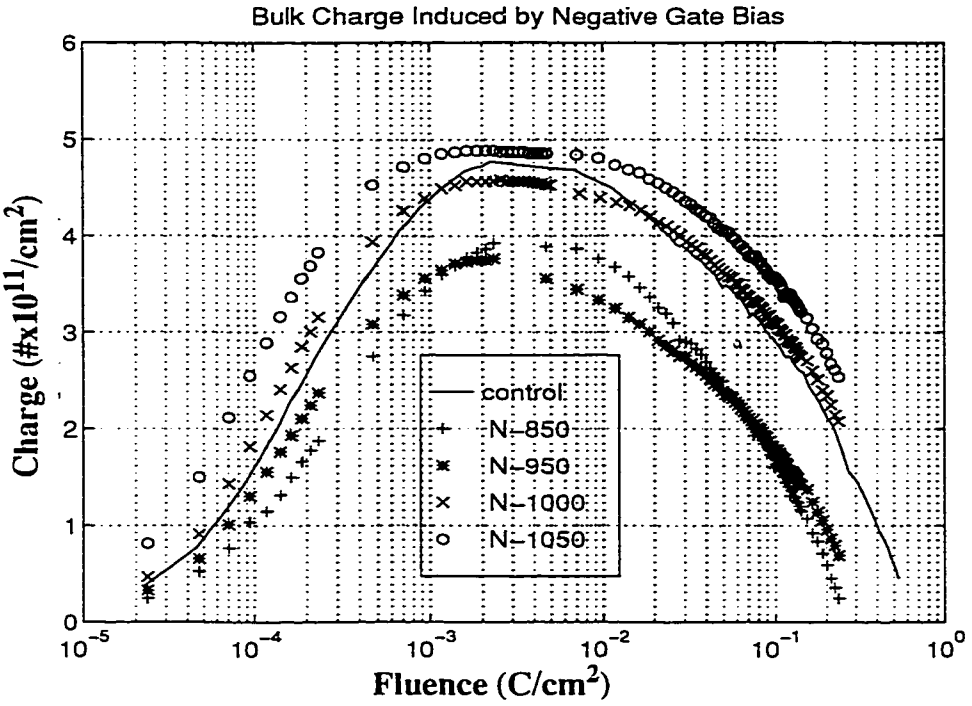


Fig. 6.11 - Charging curves calculated from ΔV_g for oxynitrides under a (-) gate bias FN stress.

6.2.1.4 ΔV_{fb}-ΔV_g Charging Curves

Fig. 6.12 shows the data extracted from ΔV_{fb}-ΔV_g. All oxynitrided cases have higher net positive maxima than the control. Some details are listed as follows:

- Case N-850 is almost coincident with the control case. This would indicate that, at the 850°C re-oxidation temperature, the oxynitridation process does not affect much the behavior of the oxide at the poly/SiO_2 interface.

- The N-950 and N-1000 cases show that, at these re-oxidation temperatures, the hole traps at the poly/SiO_2 interface are now enhanced. The N-950 case has the highest positive maximum. However, as shown in Fig. 6.12, we expect an intersection between charging curves of N-950 and N-1000 cases (at higher fluence f~2.5×10^{-1} C/cm^2). The

highest positive maximum and this anticipated intersection suggest the conclusion that N-950 has more electron traps than N-1000. Thus, between these two cases, the higher the re-oxidation temperature, the fewer electron traps generated.

• The above-discussed trend again appears in case N-1050. In Fig. 6.12, there is no indication that the case N-1050 has reached its maximum yet. This oxynitride might have dramatically suppressed the electron trapped charges. This result is consistent with the findings of Mazumder *et al* [88]. In Ref. 88, if a thick nitride layer (51Å) is deposited at an interface of the bulk oxide and the anode, then a high density of positive trapped charges is formed at the other interface. However, this phenomenon does not appear when the nitride layer is thinner (43Å) [88]. According to Ellis *et al* [71], in oxynitridation when nitrogen atoms congregate to the Si/SiO_2 interface, they form chemical bonds as $Si_3{\equiv}N$. This bond is actually the chemical bond found in nitride. According to Hori *et al*'s model [31], case N-1050 would have the highest nitrogen concentration at the Si/SiO_2 interface. Case N-1050, therefore, could have a thick nitride layer. This layer could be thick enough to entirely suppress the electron traps as reported by Mazumder *et al* [88].

Overall, there is no systematic variation in the aspect of hole traps. But *higher oxynitridation temperature leads to fewer electron traps.*

Like in the fluorinated cases, Table 6.2, shows that under (-) CCFN more defects are caused than in (+) CCFN. And as discussed above, Figs. 6.10, 6.12, and Table 6.2 summarize that most of these defects are located at/near the poly/SiO_2 interface. Data of (+) bias are included in Table 6.2 to be compared later in Section 6.3.

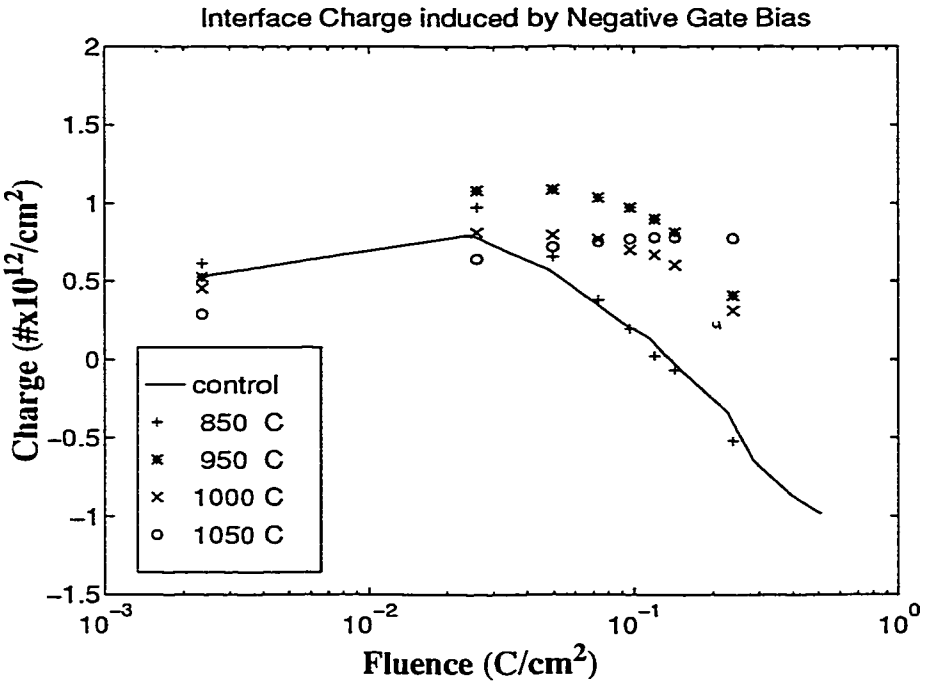


Fig. 6.12 - ΔV_{fb} -ΔV_g Charging Curves for the Oxynitrided family under the negative CCFN.

Oxide	*(+)Bias* Max + position (10^{-3}C/ cm^2)	*(-)Bias* Max +position (10^{-3}C/ cm^2)	*(+)Bias* N_{ic} at $2.3x10^{-3}$ C/cm^2 (10^{11}cm^2)	*(-)Bias* N_{ic} at $2.3x10^{-3}$ C/cm^2 (10^{11}cm^2)	*(+)Bias* Max + value (10^{11}cm^2)	*(-)Bias* Max + value (10^{11}/ cm^2	*(+)Bias* Total charge at $2.3x10^{-3}$ C/cm^2 (10^{11}cm^2)	*(-)Bias* Total charge at $2.3x10^{-3}$ C/cm^2 (10^{11}/ cm^2)
Control	2.1	2.2	- 0.96	5.25	3.42	4.77	2.44	10.02
N-850	2.3	2.4	-1.04	6.12	3.87	3.93	2.82	10.01
N-950	2.3	2.4	-1.01	5.25	3.35	3.76	2.34	9.02
N-1000	2.3	2.6	-0.96	4.55	3.75	4.58	2.78	9.11
N-1050	2.3	2.4	-1.07	2.90	3.77	4.89	2.70	7.79

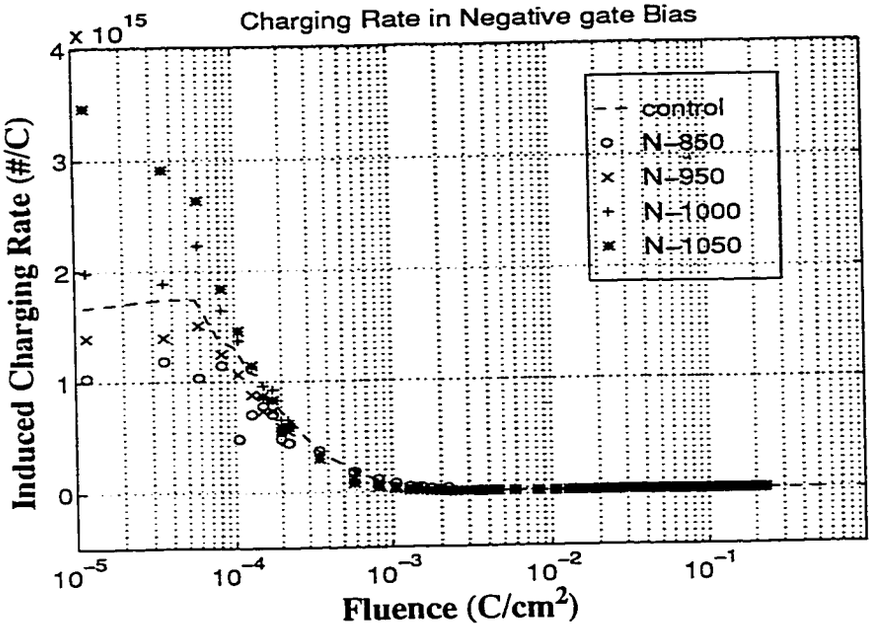
Table. 6.2 - Comparison of maximum values of positive maxima from charging curves in both set of (+) and (-) gate bias FN stress after an injected fluence of ~$2.5x10^{-2}$C/cm^2.

6.2.1.5 Induced Charging Rate In The Bulk Oxides

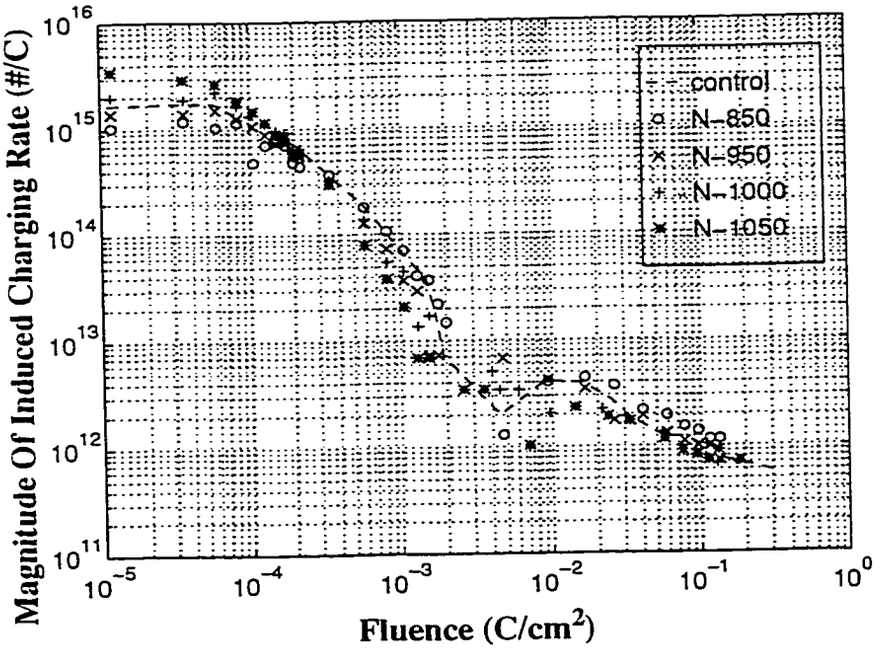
In Fig. 6.13(a), at low fluence, a systematic trend is observed in ΔV_g charging curves: that the higher the re-oxidation temperature, the higher the hole trapping rate. Again the control curve is found between the oxynitrided cases (below N-1000 and above N-950). The hole trapping rate of the N-1050 case is twice that of the control. These results prove that the low re-oxidation temperature, i.e. low nitrogen concentration at the Si/SiO_2 interface, might cause fewer hole traps in the bulk and at the Si/SiO_2 interface. However, a high re-oxidation temperature, i.e. high nitrogen concentration at the Si/SiO_2 interface, enhances the hole trap creation during a (-) CCFN.

Fig. 6.13(b) shows a clearer view of the view of electron trapping rate. With $f>10^{-3}$ C/cm^2 (in Fig, 6.13(b)), The N-850 case shows the largest induced negative charging rate.

Table 6.3 summaries the values of K_1 and K_2 which are extracted from the Fig. 6.13. The values of K_1 and K_2 in (+) CCFN are included to compare the effects of oxynitridation in both bias configurations later. The three (-) columns show a very interesting systematic variation that the higher the re-oxidation temperature, the greater the rate of change of the electron trap, and the grater the hole trapping rate. But whatever aspect, the control value is always stays between the two oxynitrided cases: below N-1000, and above N-950.



(a)



(b)

Fig. 6.13 - Induced Charging Rate of oxynitrided samples under (-) FN stress, in a) semilog plot, and b) log-log plot.

Oxide	*(+) Bias* K_1[i] (10^{15})	*(-) Bias* K_1 (10^{15})	*(+) Bias* K_2 (10^{15} #/C)	*(-) Bias* K_2 (10^{15}#/C)	*(+) Bias* Hole Trapping Rate (10^{15}#/C)	*(-) Bias* Hole Trapping Rate (10^{15}#/C)
Control	-1.56	-1.67	-5.25	-5.43	1.17	1.72
N-850	-1.49	-0.95	-4.92	-2.96	1.35	1.09
N-950	-0.90	-1.50	-2.79	-4.93	1.12	1.43
N-1000	-1.25	-2.11	-4.05	-7.04	1.30	2.03
N-1050	-1.48	-2.49	-4.92	-8.48	1.33	3.00

i. Dimension of K_1 is #/C per decade of fluence.

Table. 6.3 - Comparative K_1 & K_2, and Hole Trapping Rate in (+) and (-) bias for the oxynitrided family, including the control case.

6.2.2 Summary of (-) Bias Data

The Si/SiO_2 interface state distribution, like in (+) bias, under (-) CCFN shows a systematic variation in oxynitridation: the higher the re-oxidation, the fewer the interface states generated. And all of investigated oxynitrides, while they have higher interface state densities before any electrical stress, have a lower interface state densities than the control after an electrical stress.

Charges located in the bulk and the Si/SiO_2 interface show a systematic variation in the oxynitrided cases. The higher the oxynitridation temperature, the larger the number of hole traps generated. However, the control case is not the worst in this aspect. The control oxide has fewer hole traps created than the oxynitrided cases with higher oxynitridation temperatures (1000°C, and 1050°C), but has more hole traps created than the lower temperature oxynitridations (950°C, and 850°C).

There is also the same systematic variation for the rate of change of electron trapping rate in the bulk and at the Si/SiO_2 interface: the higher the oxynitridation temperature, the greater the rate of change of electron trapping rate. And like in hole trapping rate, the rate of change of electron trapping rate for the control is less than the higher temperature oxynitridation cases (1000°C, and 1050°C), but more than the lower temperature oxynitridation cases (950°C, and 850°C).

A large amount of positive charge is generated at/near the poly/SiO_2 interface at low fluence ($f < 2.3 \times 10^{-2}$ C/cm^2).

The variation in terms of induced charging rate, and the rate of change of the electron traps follows again the pattern observed in ΔV_g charging curves (charges located in the bulk and at the Si/SiO_2 interface). The pattern is the higher the oxynitridation temperature, the higher the hole trapping rate, and the higher the rate of change of the electron traps. And again the corresponding values for the control case are below N-1000 values and above N-950 values.

6.3 (+) Bias Vs. (-) Bias

6.3.1 The Si/SiO_2 Interface State Distribution

Fig. 6.2, and Fig. 6.9 are used for comparison of the two polarities. Table 6.4 summarizes the midgap interface state densities of oxynitrided and the control oxides under both (+) and (-) gate biases after an injected fluence of ~ 2×10^{-2} C/cm^2. Interface state densities varies following a pattern that the oxides formed by higher the temperature of oxyni-

tridation has less generated interface states in both bias configurations. The distribution of interface states under (-) CCFN stress is approximately a half of the D_{it} in (+) CCFN stress.

The explanation for this phenomenon is as discussed in Section 5.3.1. The results are consistent with DiMaria's model, for the moving of hydrogen atoms from the anode to form the interface states at the cathode [43]. In (-) gate bias, hydrogen atoms are released from the Si/SiO_2 interface to form states at the $poly/SiO_2$ interface. This explains why all oxides have fewer interface states under (-) gate bias than under (+) gate bias.

Oxides	(+) Bias Midgap D_{it} after an $f = 2.5x10^{-2}$ C/cm^2 (ev^{-1}cm^{-2})	(-) Bias Midgap D_{it} after an $f = 2.3x10^{-2}$ C/cm^2 (ev^{-1}cm^{-2})
Control	$1.09x10^{12}$	$0.54x10^{12}$
N-850	$0.71x10^{12}$	$0.38x10^{12}$
N-950	$0.49x10^{12}$	$0.26x10^{12}$
N-1000	$0.42x10^{12}$	$0.20x10^{12}$
N-1050	$0.32x10^{12}$	$0.19x10^{12}$

Table. 6.4 - Comparative midgap interface state densities of oxynitrided oxides under positive and negative gate biases.

6.3.2 ΔV_{fb} Charging Curves

Fig. 6.4 and Fig. 6.10 compare the induced charge, $N_{\Delta Vfb}(f)$, for oxynitrides. In both (+) and (-) bias cases, the data vary dramatically away from the control data at high fluence. The overall negative charging rate at high fluence is much lower for the higher

N_2O treatment temperatures. In (-) bias, the N-1050 case shows that, its net negative charging is drastically reduced (almost eliminated) until $f > 10^{-1}$ C/cm^2.

A closer view of $N_{\Delta Vfb}$ shows that there are crossovers in both sets of data (see Fig. 6.4 and Fig. 6.10). At low fluence the higher treatment temperatures yield *lower* positive charging, while at high fluence, the higher temperatures yield *slower* negative charging. Both are improvements over the respective control curves [79, 80]. In keeping with the general trends in the above discussion, the crossover occurs at substantially higher fluence in the (-) bias case (~$2.3\text{x}10^{-3}$ - 10^{-2} C/cm^2) than in the (+) bias case (~$2.3\text{x}10^{-3}$ C/cm^2). These improvements vs. the control are qualitatively consistent with the findings of Fukuda *et al* [72], and Misra *et al* [70], who show by secondary ion mass spectroscopy (SIMS) that N_2O oxynitridation leads to a pile-up of N atoms near/at the Si/SiO_2 interface.

Like the fluorinated cases, there are significantly more charges (~5 times more) induced by (-) bias than by (+) bias (see Table 6.2). Also overall positive charging regimes extend to much higher fluences in the (-) bias cases than in the (+) bias cases. In (-) bias the oxides are charging positively at fluences up to > 10^{-2} C/cm^2, while in (+) bias they are already charging negatively at ~$3\text{x}10^{-3}$ C/cm^2. These overall differences between the (-) and (+) bias cases are in general accord with the experimental observations of DiMaria *et al* [43] for thermal oxides.

6.3.3 ΔV_g Charging Curves And Trapping Rate Calculated From ΔV_g Charging Curves

Figs. 6.5 & 6.11 compare the (-) bias and (+) bias induced charge $N_{\Delta Vg}(f)$, for oxynitrides. Figs. 6.6, 6.7 & 6.13, and Table 6.3 summarize the derived charging rates.

Similarly to Ref. [43] and the results of fluorinated samples in Chapter 7, the differences between the positive and negative cases are rather subtle, less dramatic than differences in $N_{\Delta Vfb}(f)$. The negative bias cases generally reach somewhat greater positive charging maxima, and have somewhat higher zero-crossing fluences. However, as shown in Figs. 6.5 & 6.11, and Table 6.2, all the positive charging maxima in both (-) and (+) biases occur at a fluence ~2-2.6x10^{-3} C/cm^2.

Like in (+) bias, in (-) bias the maximum positive charge is almost attained at the same fluence for all treatment temperatures. But for the higher temperatures, 1000°C and 1050°C, in (-) bias it seems that the maxima values are maintained for a larger range of fluence (see Fig. 6.11). Although not very significant, the data in Table 6.2 show that the maximum-positive charge occurs at a slightly higher fluence under (-) bias (compared to (+) bias). Since $N_{\Delta Vg}$- consists of trapped charges in the bulk (outside of a tunnelling distance from the poly/SiO_2 interface) and trapped charges at the Si/SiO_2 interface, the characteristic behaviors of interface states at the Si/SiO_2 interface could be the cause of the difference. As discussed in Section 6.1.1.4, Belkouch *et al* [41] reported the appearance of two trap levels in oxynitrides: one is at E_c-0.3eV, and the other is at E_c-0.2eV. Higher oxynitridation temperature yields more states at E_c-0.2eV, and fewer states at E_c-0.3eV [41]. In addition, states at E_c-0.2eV level are insensitive to an electrical stress [41]. The Si/SiO_2 interface states at E_c-0.3eV possess a capture cross-section of 3.8x10^{-18} cm^{-2} [41], with which the interface states contribute observable trapped charges at fluences on the order of 10^{-3} C/cm^2 [55]. Because the positive maxima of $N_{\Delta Vg}$- occur around this order of magnitude (~2.4x10^{-3} C/cm^2), the reduction of the interface Si/SiO_2 states at E_c-0.3eV could be the cause for the slight increase of the maximum-positive fluence in $N_{\Delta Vg}$- (com-

pared to $N_{\Delta Vg}$+). The almost-flat (broader) peaks of $N_{\Delta Vg}$- curves of higher temperature oxynitrides (in Fig. 6.11) are evidence supporting the above-discussed hypothesis.

In (-) bias, the higher temperatures lead to more-rapid positive charging at low fluence (< 10^{-4} C/cm^2 as seen in Fig. 6.13(a), and summarized in Table 6.3). Next, Table 6.3 shows that at fluences of 10^{-4} - 10^{-3} C/cm^2, the rate of change of the electron trapping rate, K_I, is also most severe at high N_2O treatment temperatures under (-) CCFN. These are quite different from values of K_I observed under (+) CCFN. Positive bias data in Table 6.3 shows that, there is an optimal oxynitridation temperature to yield the smallest hole trapping rate and K_I. And this temperature should be in the range of 850°C-950°C. The contrast between these variations and those observed in both $N_{\Delta Vg}$- and $N_{\Delta Vg}$+ are consistent with oxynitridation affecting the bulk oxide quite differently near the two interfaces: (a) the effects on the variations in positive charging in the bulk oxide are more evident near to the poly/SiO_2 interface than near to the Si/SiO_2 interface (in N_{ic}-), and (b) higher N_2O treatment temperatures lead to reduce negative trapping near to the Si/SiO_2 interface (in N_{ic}+), but increase negative trapping near to the poly/SiO_2 interface under (-) bias (see (-) Bias K_I column in Table 6.3) [80]. Again, this is likely to be due to the presumed high N concentration near the Si/SiO_2 interface, and relatively low N concentration near the poly/SiO_2 interface [31, 80].

6.3.4 Relations Observed From ΔV_{fb}, ΔV_g, And ΔV_{fb}- ΔV_g Charging Curves

Like the fluorinated study, the positive charging maxima reached in (-) bias $N_{\Delta Vfb}$-, are substantially greater (> 2 times greater) than the positive charging maximum reached

in $N_{\Delta Vg}$- (see Figs. 6.10 and 6.11). It can be concluded that most of the positive induced charges, indicated by the positive charging regime in Fig. 6.10, must be nearer to the poly/SiO_2 interface. As discussed also in Chapter 5, if this were not true, $N_{\Delta Vg}$- would be much higher than it is, since $N_{\Delta Vg}$- is less sensitive than $N_{\Delta Vfb}$- to charges near the poly/SiO_2 interface [43, 80].

In addition, data in Table 6.4 show that, after an injected fluence of $2.3\text{x}10^{-2}$ C/cm^2 in (-) bias stress most of the oxynitrided and the control have (+) bias D_{it} about twice as great as (-) bias D_{it} at midgap. The difference between the behavior of $N_{\Delta Vfb}$ and D_{it} is striking. At $f = 2.3\text{x}10^{-2}$ C/cm^2, $N_{\Delta Vfb}$- is at least $2(D_{it})$, suggesting that $N_{\Delta Vfb}$- contains substantial contributions from positive trapped charges somewhat farther out in the oxide (such that they would not be seen in D_{it}). This conclusion is consistent with DiMaria model, in which under negative gate bias CCFN, ΔV_g does not sensitive to the trapped charges which are created or located within a tunnelling distance from the poly/SiO_2 interface [43].

Also, in (-) bias, the $N_{\Delta Vg}$- curves all reach their maximum positive charging at fluences $< 5\text{x}10^{-3}$ C/cm^2, while the $N_{\Delta Vfb}$- curves all reach their maximum positive charging at fluences $> 10^{-2}$ C/cm^2. This provides an evidence such that the positive charging observed in $N_{\Delta Vg}$- is not simply a less-sensitive result of the *same* positive charging as observed in $N_{\Delta Vfb}$- [80]. Thus, the variations in $N_{\Delta Vfb}$- are likely to be due to variations in a different set of bulk charges, probably nearer to the poly/SiO_2 interface, perhaps having smaller capture cross-sections. This should be contrasted with the (+) bias results, where all the positive charge maxima occur at fluences about $2\text{x}10^{-3}$ C/cm^2, likely since both

$N_{\Delta Vg}$+ and $N_{\Delta Vfb}$+ are sensitive to trapped charges near to the same Si/SiO_2 interface [79, 80].

6.3.5 Summary of (+)Bias Vs. (-) Bias Comparisons

Oxynitrides exhibit a pattern of higher oxynitridation temperatures causing fewer interface states in both (-) and (+) biases. And the control shows the highest interface state density. Moreover, (-) gate bias yields about half the interface state density as does (+) gate bias.

Negative bias CCFN stressing yields quite different charging behavior from positive bias, in both control and oxynitrides, Analyses of $N_{\Delta Vfb}$, $N_{\Delta Vg}$, and D_{it} in the (-) bias show that, enhanced positive charging is not presented at the Si/SiO_2 interface but at/near $poly/SiO_2$ interface. This set of charge could have a smaller ("slower") capture cross-section than the induced positive charge in the bulk, $N_{\Delta Vg}$-. This is contrasted with the positive bias results, where all the positive charge maxima occur at almost the same fluences, i.e the same capture cross-section for all positive induced charge in positive gate bias

While (+) bias show that higher temperature forms better oxynitrided oxides, this is not true in (-) bias. Higher temperature oxynitrides could have higher induced positive trapped charges, higher electron trapping rate. Overall, higher N_2O treatment temperatures lead to improvements vs. standard thermal oxide in charging near the Si/SiO_2 interface, consistent with SIMS [72,70] findings that nitrogen is piled up at that interface. On the other hand, bulk charging near the $poly/SiO_2$ interface is detrimentally affected.

6.4 Chapter 6 Contributions

An extensive characterization of oxynitrides is executed. The study is done on both positive and negative gate bias CCFN. The study disclosed the complex scenario of charge components generated into different locations in gate oxides in both (+) and (-) gate biases.

Under positive gate bias, positive trapped charges and hole trapping rate (at low fluence), in the bulk oxide ($N_{\Delta Vg}$+), shows a non-linear relationship to the oxynitridation temperature. The optimal temperature is found to be in the range of 850°C-950°C.

Under positive gate bias, higher oxynitridation temperatures lead to fewer electron traps in the bulk oxide ($N_{\Delta Vg}$+), and lower electron trapping rate at the Si/SiO_2 interface.

Under positive gate bias, while at low fluence the rate of change of electron trapping rate in the bulk appears to have an optimum at 850°C-950°C, at high fluence, higher oxynitridation temperatures are related to lower (better) electron trapping rate in the bulk, without any optimum at 850°C-950°C. This would tend to suggest that different phenomena govern electron trapping rates at high vs. low fluence [79].

The analyses of N_{ic}+ expose that slow donor states (APC) appear at high fluence only in the control oxide, but not in any of the oxynitrides. This suggests that oxynitridation significantly suppress this type of charge defects in gate oxides.

Under negative gate bias CCFN, higher oxynitridation temperature leads to more hole traps and higher hole trapping rates for charges (from $N_{\Delta Vg}$-), which are located outside a tunnelling distance from the $poly/SiO_2$ interface.

Also under negative gate bias, higher oxynitridation temperatures lead to fewer electron traps, and greater rates of change of electron trapping rate for charges (from $N_{\Delta Vg}$-), which are located outside a tunnelling distance from the poly/SiO_2 interface.

However, not all oxynitrided oxides show better performance than the control. In aspects as hole trapping rate, the rate of change of electron trapping rate, induced positive and negative charges, the analyses of $N_{\Delta Vg}$- show that, these values for the control are always smaller (better) than the high temperature oxynitrides (1000°C & 1050°C) and larger (worse) than the low temperature oxynitrides (850°C & 950°C).

Analyses of $N_{\Delta Vfb}$-, $N_{\Delta Vg}$-, N_{ic}-, and D_{it}- show a large amount of positive trapped charge induced at/near the poly/SiO_2 interface. This set of charge have smaller, "slower", trap capture cross-sections, comparing to the capture cross-sections of positive charges induced in the bulk under negative gate bias CCFN, or any positive charges induced under positive gate bias CCFN.

The study of the interface state density, D_{it}, show a systematic variation in oxynitrides oxides. Higher oxynitridation temperatures exhibit fewer interface states created in both (+) and (-) biases. These results are consistent with Hori's model [31] and the deep level transient spectroscopic study of these same oxynitrides by Belkouch *et al* [41].

CHAPTER 7

FLUORINATION Vs. OXYNITRIDATION

In this chapter, the data of fluorinated family B-25K, implanted at 25KeV before poly-etch, are compared and constrasted with the data of oxynitrided samples.

7.1 D_{it} Generated Under Positive And Negative Gate Biases

7.1.1 Common Behavior of Both Fluorinated And Oxynitrided Oxides In D_{it}

Under positive gate bias (see Fig. 5.1 and Fig. 6.2) and also under negative gate bias (see Fig. 5.17 and Fig. 6.9), there are several behaviors common to both fluorinated and oxynitrided oxides.

- Both the fluorinated and the oxynitrided cases show lower interface state densities generated under CCFN than interface state densities generated in the control oxides.

- Interface state densities generated under positive gate bias are approximately twice the magnitude of the interface state densities generated under negative gate bias. This is true of every case studied in this thesis. (see Table 7.1).

These results are consistent with the trends in the prior literature. They further confirm the plausibility of a mechanism involving replacement of Si-H chemical bonds by some other chemical bonds such as Si-F or Si-N, believed to require higher energy to be broken. This again supports the proposed mechanisms of trapped charge generated by hot electrons in DiMaria's model [76-80]. Overall, these results confirm that both fluorinated and oxynitrided oxides are of higher quality than control oxides in aspect of interface states density.

7.1.2 Numerical Difference In D_{it} Between Fluorinated And Oxynitrided Cases.

Table 9.1 summarizes the midgap D_{it} for (+) bias from Fig. 5.1 and Fig. 6.2, and for (-) bias from Fig. 5.17 and Fig. 6.9. Under positive gate bias, the worst case is the control which has the highest midgap D_{it} of $1.09\text{x}10^{12}$ $eV^{-1}cm^{-2}$ after a $f = 2.5\text{x}10^{-2}$ C/cm^2. Although smaller, the interface state densities of the fluorinated cases are only slightly smaller, and are in the range $0.98\text{-}1.03\text{x}10^{12}$ $eV^{-1}cm^{-2}$ after an injected $f = 2.5\text{x}10^{-2}$ C/cm^2. However, the interface state densities of the oxynitrides are more substantially lower. These values are in the range $0.32\text{-}0.71\text{x}10^{12}$ $eV^{-1}cm^{-2}$ after an injected $f = 2.5\text{x}10^{-2}$ C/cm^2. The higher oxynitridation temperatures have lower midgap interface densities.

Similar to (+) gate bias, under (-) CCFN, the exhibited D_{it} values of the fluorinated cases are not substantially smaller than the control's D_{it} ($0.54\text{x}10^{12}$ $V^{-1}cm^{-2}$ after an injected $f = 2.3\text{x}10^{-2}$ C/cm^2). The case B-5E15-25K displays a D_{it} higher than the control ($0.56\text{x}10^{12}$ $V^{-1}cm^{-2}$ after an injected $f = 2.3\text{x}10^{-2}$ C/cm^2). The oxynitrides have quite smaller D_{it} in the range of $0.19\text{-}0.38V^{-1}cm^{-2}$ after an injected $f = 2.3\text{x}10^{-2}$ C/cm^2. Again

the pattern of the higher oxynitridation temperature shows a lower interface state density generated.

Oxides	(+) Midgap D_{it} after an $f = 2.5\text{x}10^{-2}$ C/cm^2 (ev^{-1}cm^{-2})	(-) Midgap D_{it} after an $f = 2.3\text{x}10^{-2}$ C/cm^2 (ev^{-1}cm^{-2})
Control	$1.09\text{x}10^{12}$	$0.54\text{x}10^{12}$
B-6E14-25K	$0.98\text{x}10^{12}$	$0.52\text{x}10^{12}$
B-1E15-25K	$1.00\text{x}10^{12}$	$0.49\text{x}10^{12}$
B-2E15-25K	$1.02\text{x}10^{12}$	$0.48\text{x}10^{12}$
B-5E15-25K	$1.03\text{x}10^{12}$	$0.56\text{x}10^{12}$
N-850	$0.71\text{x}10^{12}$	$0.38\text{x}10^{12}$
N-950	$0.49\text{x}10^{12}$	$0.26\text{x}10^{12}$
N-1000	$0.42\text{x}10^{12}$	$0.20\text{x}10^{12}$
N-1050	$0.32\text{x}10^{12}$	$0.19\text{x}10^{12}$

Table. 7.1 - Comparative midgap D_{it}, for a) positive gate bias up to $f = 2.5\text{x}10^{-2}$ C/cm^2 and b) negative gate bias up to $f = 2.3\text{x}10^{-2}$ C/cm^2.

The pattern of variation of interface state densities in oxynitrides is consistent with the Hori *et al*'s model [31] in which higher oxynitridation temperature causes higher nitrogen concentration at the Si/SiO_2 interface. The discussion also shows that in both (+) and (-) biases, oxynitridation improves the interface state density of oxides more than the fluorination does.

7.2 Anomalous Positive Charge or Slow Donor States Generated

Two figures, Fig. 5.5(b) and Fig. 6.8, are used to discuss the performance of the control, fluorinated and oxynitrided oxides in the aspect of generation of anomalous positive charge (APC).

7.2.1 Common Behavior of Fluorinated And Oxynitrided Oxides Due To Anomalous Positive Charge.

The discussions in Section 5.1.1.4 and Section 6.1.1.4 show that the control has a turn-around at a fluence of ~$7x10^{-2}$ C/cm^2 after reaching an extremum of ~ -$4x10^{11}$ #/cm^2. This indicates the existence of APC at/near the Si/SiO_2 interface of the control oxide. The discussion also shows that there is reduction or suppression of APC in gate oxides in the fluorinated and the oxynitrided cases [78, 79].

7.2.2 Detailed Difference In APC Between The Fluorinated And Oxynitrided Cases

However, in fluorinated cases at even greater fluence (f>$7x10^{-2}$ C/cm^2) N_{ic} levels off or becomes slightly more positive. Fig. 5.5(b) illustrates this statement. The data points at $f = 2.2x10^{-1}$ C/cm^2 show that APC has been generated in the fluorinated cases. Thus, the fluorination partly suppresses APC at the Si/SiO_2 interface, but not entirely.

In Fig. 6.8, however, there is no turn around observed in the oxynitrided cases. Especially, in the N-1050 case, even at quite high fluence f~1 C/cm^2, there is no evidence

of APC. As a consequence, oxynitrides might entirely suppress APC in the gate oxide. By this, oxynitrides show better performance than the control (the worst) and than the fluorinated oxides in reducing/suppressing APC.

7.3 Trapped Charges Near The SiO_2 interfaces

A limitation of the DiMaria model is that, there is no possibility to study the trapped charge at both interfaces of bulk oxides under the same gate bias. Under (+) gate bias, the trapped charges calculated from (ΔV_{fb} - ΔV_g) only expose information about trapped charges created near/at the Si/SiO_2 interface within a tunneling distance from the Si/SiO_2 interface. Under (-) gate bias, the extracted charging curves from (ΔV_{fb} - ΔV_g) contain information only about the trapped charge at/near the poly/SiO_2 interface. Under (-) gate bias, some more analyses can be done for the interface state density, D_{it}, presenting defects at/near the Si/SiO_2 interface. The values of D_{it}, however, could not be converted into real trapped-charge numbers. Therefore, one can only make rough guesses what might be happening at the Si/SiO_2 interface under (-) gate bias stress.

7.3.1 Trapped Charges Generated Under (+) Gate Bias At/Near The Si/SiO_2 Interfaces

Table 7.2 summarizes the values of N_{ic}+ at f=0.1C/cm^2 of two oxide families, the oxynitrides and the B-25K fluorinated oxides (from Fig. 5.5(b) and Fig. 6.8). In Fig 5.5(b), all the fluorinated cases show more electron traps generated at/near the Si/SiO_2 interface

than in the control. In Table 7.2, the variation of the fluorinated cases is very systematic: higher fluorine dose causes more electron traps near/at the Si/SiO_2 interface.

However, the oxynitrides behave very differently. Fig. 6.8 shows that all of the oxynitrides have fewer induced electron traps than the control (and of course than the fluorinated oxides). The data in Table 7.2 show a systematic variation in oxynitrides: the higher oxynitridation temperatures cause fewer electron traps generated at/near the Si/SiO_2 interface. Especially, N_{ic}+ in the N-1050 case after $f = 0.1 C/cm^2$ is near half of the control's N_{ic}+ after the same injected fluence.

Oxides	N_{ic}+ at $f = 0.1 C/cm^2$ ($10^{11}/cm^2$)
Control	-3.95
B-6E14-25K	-4.08
B-1E15-25K	-4.11
B-2E15-25K	-4.30
B-5E15-25K	-4.61
N-850	-3.65
N-950	-2.84
N-1000	-2.56
N-1050	-2.11

Table. 7.2 - N_{ic} of the B-25K family and the oxynitrided family obtained at a $f = 0.1$ C/cm^2.

In short, the oxynitridation helps to reduce electron trapping at the Si/SiO_2 interface under positive gate bias CCFN. And the fluorination enhances electron trap creation at/near the Si/SiO_2 interface under positive gate bias CCFN.

7.3.2 Trapped Charges Generated Under (-) Gate Bias At/Near The $Poly/SiO_2$ Interfaces

7.3.2.1 Common Behaviors of Positive Trapped Charges Generated Under (-) Bias At/Near The $Poly/SiO_2$ Interfaces

As discussed in Sections 5.2.1.4, 5.3.4, 6.3.4, and 6.2.1.4, there are two types of trapped charge generated at/near $poly/SiO_2$ interface under negative gate bias. At low fluence, positive trapped charges appear. At high fluence, negative trapped charges appear.

For positive trapped charge there are some common behaviors, which can be listed for all oxides under investigation:

- High magnitude of positive maxima, (i.e a large amount of positive trapped charges are generated). For the control, it reaches the maximum of ~$8x10^{11}$ #/cm^2. All the fluorinated oxides (see Fig.5.21), and oxynitrides (see Fig. 6.12) have higher positive maxima than the control does.

- This set of positive trapped charges is different from that found in the bulk oxide. This set of positive trapped charge possesses a smaller capture-cross section than those in the bulk.

7.3.2.2 Differences Of Fluorination And Oxynitridation In Electron Traps At/Near The Poly/SiO_2 Interface Under (-) CCFN

There are two considered aspects here: electron traps, and electron trapping rates.

Most of the cases show the existence of electron traps. However, in the case N-1050, it seems that there is no evidence of electron traps. This was also reported by Mazumder *et al* [88]. One of their samples under negative gate bias, exhibits only a huge number of hole traps, but no electron traps. The curves in Fig. 6.12, under (-) bias, after the attainment of the positive maxima, show fewer electron traps generated in the oxynitrides than in the control, except in the N-850 case. For fluorinated oxides, the data in Fig. 5.21, under (-) bias, show that the B-5E15 case has slightly less electron traps, while the other fluorinated cases have around the same density of electron traps as the control. Thus overall, oxynitride (with temperature $\geq 950^{o}C$) has less electron traps than the control and fluorinated oxides.

To study the electron trapping rate, there are two points which may be important: the maximum positive value, and any crossover at higher fluence. In Fig. 5.21, some fluorinated samples have higher positive maxima, but there are also crossovers between their N_{ic}- and the control's N_{ic}- curves. This indicates that at high fluence, fluorinated oxides have higher electron trapping rate at/near the Si/SiO_2 interface than the control does. For convenience of comparison, averaged electron trapping rates of the oxynitrides and the fluorinated oxides in the B-25K family are estimated. An example of the estimation is: (trapping rate) = (trapped charge at $2.3x10^{-1}$ C/cm^2 - trapped charge at $2.3x10^{-2}$ C/cm^2) divided by ($2.3x10^{-1}$ C/cm^2 - $2.3x10^{-2}$ C/cm^2). The results are tabulated in Table 7.3.

The data in Table 7.3 show that the oxynitridation reduces the electron trapping rate, especially with higher oxynitridation temperature. In the fluorinated cases, the data in Table 7.3 show only the case B-5E15-25K having lower averaged electron trapping rate than the control. The other three fluorinated cases have higher electron trapping rate than the control.

Oxides	Approximate Electron Trapping Rate (#/C)
Control	-5.49×10^{12}
B-6E14-25K	-6.59×10^{12}
B-1E15-25K	-5.59×10^{12}
B-2E15-25K	-5.63×10^{12}
B-5E15-25K	-5.23×10^{12}
N-850	-7.22×10^{12}
N-950	-3.25×10^{12}
N-1000	-2.42×10^{12}
N-1050	0.63×10^{11}

Table. 7.3 - Electron trapping rates, averaged values calculated by ΔN_{ic}-/ Δf. Where fluence is from 2.3×10^{-2}C/cm^2 to 2.3×10^{-1} C/cm^2.

7.4 Trapped Charge, Charging Rates, The Rate of Change of Charging Rate In $N_{\Delta Vg}$

7.4.1 Common Behaviors In Hole Traps:

The data in Tables 5.2, and 6.2 show that the hole traps at the low fluence, under both (+) and (-) gate bias, have some common behaviors:

- The positive maxima are found at almost the same fluence. This information shows that these sets of charge share the same hole capture-cross section.

• Although the (-) gate-bias data always show higher positive maxima than the (+) gate-bias data, the difference between these two sets of data in most cases is about $1.2x10^{11}$ /cm^2. This difference could be due to the sensitivity of gate voltage of charges located at/near the injecting interfaces, since the two interfaces have different micro-structures, (the Si substrate possesses a crystalline structure, while the poly possesses a poly crystalline structure).

However, since the positive maxima are found at the same fluence, and have a value varied from a difference of ~$1.2x10^{11}$ /cm^2, this might indicate that the two observed sets of positive charges from $N_{\Delta Vg}$ - and $N_{\Delta Vg}$ + are actually the same sets of charges.

7.4.2 Considered Parameters In $N_{\Delta Vg}$+

Discussions in Chapter 5 and Chapter 6 reveal that:

• *Trapped Charges:* Fig. 5.5(a) and Fig. 6.5 show that the hole traps, in general, do not vary much due to fluorination or oxynitridation. However, both oxynitrided and fluorinated oxides have fewer electron traps than the control. Further details reveal that the zero-crossing fluences of the fluorinated cases are from ~$8x10^{-2}$ to ~$1.3x10^{-1}$ C/cm^2 (in Fig. 5.5(a)), while the oxynitrides' zero-crossing fluences are from ~$1.3\ x10^{-1}$ to greater than 1C/cm^2 (in Fig. 6.5). Note that the positive maxima do not vary much and are located almost at the same fluence. Therefore, if the graphical model in Section 3.2.3.2 is applied, then the oxynitrides have fewer electron traps than the fluorinated oxides (and of course fewer than the control oxides).

• *Induced Charging Rate:* First, for the hole trapping rate at low fluence, in Table 7.4, the best of the fluorinated cases is B-1E15 with a rate = $1x10^{15}$ #/C. For the oxynitrides the best is N-950 with a rate of $1.12x10^{15}$ #/C. The other oxynitrided cases have higher hole trapping rates than any member in B-25K family, and the control oxide (with a rate of $1.17x10^{15}$ #/C). In short, the fluorinated cases have lower hole trapping rates than the oxynitrides.

Secondly, for the electron trapping rate, compare the two figures, Fig. 5.11 and Fig. 6.6. Around f = 1-3x10^{-3} C/cm^2, the negative trapping rates of the fluorinated cases are obviously "smaller" than the control. But Fig. 6.6 shows that the electron trapping rates of oxynitrides are "significantly smaller" than the control's.

• *The rate of change of the trapping rate, K_I*: The column (+) K_I in Table 7.4 reveals that the control case has the largest K_I (- 1.56 x10^{15}). The best case of the B-25K family is the case B-2E25 with a K_I of -$1.06x10^{15}$. And the best of the oxynitrides is the N-950 case with a K_I of -$0.90x10^{15}$.

However, while the other K_Is in the fluorinated cases are from -$1.08x10^{15}$ to -$1.24x10^{15}$ the other oxynitrides' K_Is are from -$1.25x10^{15}$ to -$1.48x10^{15}$. Thus except for the optimal oxynitrided case (N-950), all other oxynitrides have higher rates of change of the electron trapping rate than the fluorinated cases.

Oxide	(+) Bias K_1 (10^{15})	(-) Bias K_1[i] (10^{15})	(+) Bias K_2 (10^{15} #/C)	(-) Bias K_2 (10^{15} #/C)	(+) Bias Hole Trapping Rate (10^{15} #/C)	(-) Bias Hole Trapping Rate (10^{15} #/C)
Control	-1.56	-1.67	-5.25	-5.43	1.17	1.72
B-6E14-25KeV	-1.11	-1.64	-3.57	-5.39	1.18	1.60
B-1E15-25KeV	-1.08	-1.57	-3.46	-5.16	1.00	1.44
B-2E15-25KeV	-1.06	-1.40	-3.39	-4.52	1.07	1.36
B-5E15-25KeV	-1.24	-1.80	-3.96	-5.99	1.32	1.50
N-850	-1.49	-0.95	-4.92	-2.96	1.35	1.09
N-950	-0.90	-1.50	-2.79	-4.93	1.12	1.43
N-1000	-1.25	-2.11	-4.05	-7.04	1.30	2.03
N-1050	-1.48	-2.49	-4.92	-8.48	1.33	3.00

i. Dimension of K_1 is #/C per decade of fluence.

Table. 7.4 - Comparative K_1 & K_2, and hole trapping rate in (+) and (-) bias for the B-25K family, and oxynitrided family, including the control case.

7.4.3 Considered Parameters In $N_{\Delta Vg}$-

Discussions in Chapter 5 and Chapter 6 under (-) gate bias, reveal that:

• *Trapped Charges:* Fig. 5.20 shows that hole trapping in all fluorinated oxides is less than in the control. Their positive maxima are all higher than $4x10^{11}$ #/cm^2. In Fig. 6.11, N-1050 shows a higher positive maximum than the control's. Case N-1000 has its maximum in the same range as the maxima of the fluorinated oxides. However, oxynitrides at lower temperatures, N-950 and N-850, have substantially lower positive maxima (smaller than $4x10^{11}$ #/cm^2). Between these two cases, N-950 has the lowest positive max-

imum. Thus the lower temperature oxynitridation reduces the hole traps at low fluence under (-) gate bias.

Since the variation of the positive maxima is quite large in the oxynitride family (from 3.8×10^{11} to 4.9×10^{11} /cm^2), it is quite difficult to compare the electron traps generated in these samples, based on only the zero-crossing fluences.

• *Induced Charging Rate:* For hole trapping rate at low fluence, in Table 7.4, the best of the fluorinated cases is B-2E15-25K with a rate = 1.36×10^{15} #/C. For the oxynitrides the best case is N-850 with a rate of 1.09×10^{15} #/C. However, all the fluorinated oxides have smaller rates than the control (1.72×10^{15} #/C). For the oxynitrides, N-950 with a rate of 1.43 $\times 10^{15}$ #/C is almost the same as the rate for B-1E15-25K. The other samples, having higher oxynitridation temperatures, have substantially higher positive trapping rates (>2×10^{15} #/C). In short, the lower-temperature oxynitridation is better, or might be the same as fluorination with respect to hole trapping-rate performance. But higher-temperature oxynitridation causes significantly higher hole trapping rate.

Secondly, for electron trapping rates, compare the two figures, Fig. 5.22(b) and Fig. 6.13(b).The tails of the $N_{\Delta V_g}$- curves do not show much difference between oxynitridation and fluorination. From discussions in Chapter 5, the lower fluorine-implanted doses may cause somewhat less electron trapping rates than the control, but not for the higher fluorine-implanted doses. A similar phenomenon happens in oxynitridation: while the two lower temperature oxynitrides have lower electron trapping rate than the control, the two higher temperature oxynitrides have higher electron trapping rate than the control.

• *The rate of change of the trapping rate, K_1*: The column (-) K_1 in Table 7.4 reveals that the best case is N-850 with a K_1 of -0.95x10^{15}. The best of the fluorinated cases is B-2E15-25K with a K_1 of -1.40x10^{15}. N-950 and other fluorinated oxides, have K_1s in a range from -1.50x10^{15} to -1.80x10^{15} in which the control's K_1 is included. The other two high-temperature oxynitrided oxides, N-1000 and N-1050, have quite high K_1s, -2.11x10^{15} to -2.49x10^{15}, respectively. Thus, while the lower temperature oxynitridation helps to decrease the rate of change of the trapping rate, the higher temperature oxynitridation increases the rate of change of the trapping rate.

7.5 Overall Performance Calculated From ΔV_{fb}

First of all, left or right shifts in ΔV_{fb} cause corresponding shifts in the threshold voltage. These are not desired effects. Second, although in many cases, a shift left in ΔV_{fb} first appears at low fluence, this is followed by a shift right in ΔV_{fb}. Finally, dielectric breakdown takes place at high fluence. However, recently, Mazumder *et al* [88] reported that, under negative gate bias (CCFN), as a thick nitride layer (51Å) is deposited at an interface of bulk oxide and which is the anode, then there is more holes are trapped at the other interface, and there is no evidence of electron trapping. They reported [88], that the more holes become trapped near the gate, the more rapid the breakdown that takes place. Based on the above discussions, the overall ranks of oxides are suggested in Table 7.5 based on the absolute ΔV_{fb}.

7.5.1 Positive Gate Bias

Table 7.5 is a summary of flatband voltage shifts of members of B-25K and oxynitride families after a (+) CCFN up to $f = 0.1 C/cm^2$. Further charging details of ΔV_{fb} of these two families can be seen in Fig. 5.5(a) and Fig. 6.4. The control is the worst case. The fluorinated oxides show a quite complex relationship of ΔV_{fb} or trapped charge vs. fluorine-implanted doses. And this complex behavior is discussed in detail in Chapter 5. For oxynitrides there is a simple relation between the oxynitridation temperature and quality: higher oxynitridation temperature leads to higher quality.

Oxide	ΔV_{fb} (mV)	Trap. Charge ($10^{11}/cm^2$)	Evaluation within family	Overall Rank
Control	569	-4.63		9 (Worst)
B-6E14-25KeV	526	-4.28	>>	6
B-1E15-25KeV	542	-4.41	>>>>	8
B-2E15-25KeV	536	-4.36	>>>	7
B-5E15-25KeV	502	-4.09	>	5
N-850°C	373	-3.24	>>>>	4
N-950°C	170	-1.47	>>>	3
N-1000°C	34	-0.28	>>	2
N-1050°C	- 95	+0.78	>	1 (Best)

Table. 7.5 - Overall Oxide Quality as judged by ΔV_{fb} at fluence of ~0.1 C/cm^2 under positive gate bias [81]

7.5.2 Negative Gate Bias

The detail data for this comparison are the two figures, Fig. 5.19 and Fig. 6.10. In these two figures, while the trapped charge generated in the fluorinated cases have values clustered around the control value, the oxynitrides show quite larger positive trapped charge generated than the control and fluorinated oxides, except N-850 case.

For convenience of comparison, Table 7.6 is similar table as one as Table 7.5. In Table 7.6, the rank is suggested based on the absolute value of the flatband voltage shift. Unlike Table 7.5, data of ΔV_{fb} in Table 7.6 show only the left shift (net positive trapped charge). Variation in the fluorinated cases follows a simple pattern: the smaller the fluorine-implanted dose, the better the quality. However, the oxynitrides under negative gate bias behave differently from the positive gate bias, showing a complex variations. Within the oxynitrided family, the rank is from the best (N-850) to the worst (N-1050).

Though the "best" case is an oxynitride, overall, the fluorinated oxides present better performance under (-) bias than the oxynitrides. Under (-) bias, the control and fluorinated oxides have very similar charging curves.

Oxide	ΔV_{fb} (mV)	Trap. Charge (10^{11}/cm^2)	Evaluation within family	Overall Rank
Control	-593	4.83		4
B-6E14-25KeV	-519	4.23	>	2
B-1E15-25KeV	-591	4.82	>>	3
B-2E15-25KeV	-672	5.48	>>>	5
B-5E15-25KeV	-759	6.18	>>>>	6
N-850°C	-385	3.35	>	1(*Best*)
N-950°C	-1316	11.36	>>>	8
N-1000°C	-1273	10.25	>>	7
N-1050°C	-1408	11.47	>>>>	9 (Worst)

Table. 7.6 - Overall Oxide Quality as judged by ΔV_{fb} at fluence of ~0.1 C/cm^2 under negative gate bias.

7.6 Threshold Adjustment

Any novel technique, when is introduced into a complete fabrication process, can cause effects on the other steps. In this work, the introduced step is gate oxidation. Because gate oxidation causes effects at the interfaces and also in the bulk of oxides, there are some changes in flatband voltage. As a result, for a production line, the threshold voltages of MOS structures are now shifted.

Table 7.7 summarizes the initial V_{fb} (flatband voltage before any electrical stress), and the required implanted charge to adjust the flatband voltage back to the control values.

Eq. 3.2 is used to obtain the required charges for the adjustment. According to the data in Table 7.7, *fluorination shifts the flatband voltage to the left*, and this is consistent with Refs [14, 15]. However, *oxynitridation shifts the flatband voltage to the right*, and this is consistent with Fukuda *et al* [72]. Consequently, fluorinated oxides require some n-type implantation such as phosphorous, or antimony, while the oxynitrides require boron implantation for threshold adjustment. Note that for oxynitridation the required dose is significantly higher than for fluorination.

Oxide	V_{fb} (mV)	Number of implanted charges required to restore to V_{fb} of the control
Control	576	
B-6E14-25KeV	589	-1.06×10^{10} #/cm^2
B-1E15-25KeV	593	-1.38×10^{10} #/cm^2
B-2E15-25KeV	607	-2.52×10^{10} #/cm^2
B-5E15-25KeV	646	-5.70×10^{10} #/cm^2
N-850°C	465	9.04×10^{10} #/cm^2
N-950°C	365	1.72×10^{11} #/cm^2
N-1000°C	319	2.09×10^{11} #/cm^2
N-1050°C	242	2.72×10^{11} #/cm^2

Table. 7.7 - Initial V_{fb}, and the required threshold adjustment to bring the V_{fb} back to the control values.

7.7 Conclusion

Some common behaviors appear in every oxide, regardless of what kind of gate-oxide fabrication process is applied. These behaviors are listed:

- Less D_{it} (around a half) is generated at the Si/SiO_2 interface under negative gate bias than under positive gate bias.

- The set of positive charge generated at/near the $poly/SiO_2$ interface under negative gate bias, is actually a set different from the set of positive charge generated in the bulk oxides. This set has a slower hole capture cross-section than the hole traps generated in the bulk

- Under both bias configurations, the induced hole traps, calculated from $N_{\Delta V_g}$, are likely to be from the same set of trapped charge defects.

Other differences between the three types of oxides are tabulated in the following Table 7.8. According to the summary, under (+) bias, oxynitridation is shown to be quite better than fluorination and control. However, under (-) gate bias, the data show that in many aspects, oxynitridation is not better than fluorination and/or even the control case, mostly, because of the dominance of a huge amount of positive trapped charges generated at/near the $poly/SiO_2$ interface. According to the study of Mazumder *et al* [88], the best solution is to use the lower oxynitridation temperature oxides, in which there might be only a thin nitride layer created at/near the Si/SiO_2 interface.

		(+) Gate Bias	(-) Gate Bias
Si/ SiO_2 Interface	D_{it}	$D_{it}^{N} < D_{it}^{F} < D_{it}^{ctrll}$	$D_{it}^{N} < D_{it}^{F} < D_{it}^{ctrl}$
	APC	$APC^{N} < APC^{F} < APC^{ctrl}$	
	e^{i}-trap	$e\text{-}trap^{N} < e\text{-}trap^{ctrl} < e\text{-}trap^{F}$	
Poly/ SiO_2 Interface	h^{ii}-trap		• $h\text{-}trap^{ctrl} < h\text{-}trap^{F}$ & $h\text{-}trap^{N}$ • $h\text{-}trap^{N} \cong h\text{-}trap^{F}$ (incomparable)
	e-trap		• No e-traps for N-1050°C • $e\text{-}trap^{N} < e\text{-}trap^{F}$ & $e\text{-}trap^{ctrl}$, except N-850°C
	e-rate		$e\text{-}rate^{N} < e\text{-}rate^{F}$ and $e\text{-}rate^{ctrl}$, except N-850°C
$N_{\Delta Vg}$	h-trap	• $h\text{-}trap^{N} \cong h\text{-}trap^{F} \cong h\text{-}trap^{ctrl}$	•$h\text{-}trap^{N\text{-}1050} > h\text{-}trap^{ctrl}$ •$h\text{-}trap^{N\text{-}1000} \cong h\text{-}trap^{F} < h\text{-}trap^{ctrl}$ •$h\text{-}trap^{N@lowT\ iii} < h\text{-}trap^{F}$
	h-rate	•Best of N is $h\text{-}rate^{N\text{-}950}$ •Best of F is $h\text{-}rate^{B\text{-}1E15}$ •$h\text{-}rate^{ctrl} > h\text{-}rate^{N\text{-}950} > h\text{-}rate^{B\text{-}1E15}$	•Best of F is $h\text{-}rate^{B\text{-}2E15}$ •Best of N is $h\text{-}rate^{N\text{-}850}$ •$h\text{-}rate^{N@lowT} < h\text{-}rate^{F} < h\text{-}rate^{ctrl}$ •$h\text{-}rate^{N@highT} > h\text{-}rate^{ctrl}$
	e-trap	$e\text{-}trap^{N} < e\text{-}trap^{F} < e\text{-}trap^{ctrl}$	Not comparable
	e-rate	$e\text{-}rate^{N} < e\text{-}rate^{F} \cong e\text{-}rate^{ctrl}$	•$e\text{-}rate^{N@lowT} < e\text{-}rate^{ctrl} < e\text{-}rate^{N@highT}$ •$e\text{-}rate^{F@lowD\ iv} < e\text{-}rate^{ctrl} < e\text{-}rate^{F@highD}$
	K_1	•The best is $K_1^{N\text{-}950}$ •$K_1^{ctrl} > K_1^{other\ N\ v} > K_1^{F}$	•$K_1^{N@lowT} < K_1^{ctrl} \cong K_1^{F} < K_1^{N@highT}$
ΔV_{fb}		N better F better Ctrl	N^{850} better F ≅ Ctrl better Other N
Threshold Adj.		• N needs threshold adjustment with p-type impurity: Boron • F needs threshold adjustment with n-type impurity: Phosphorous, Antimony	

i. e for electron
ii. h for hole
iii. N@lowT for lower oxynitridation temperature for two cases: N-850, and N-950. N@highT for higher temperature and presented for two cases: N-10000, and N-1050.
iv. F@lowD for lower implanted doses: B-6E14 and B-1E15. F@highD for higher implanted doses: B-2E15, and B-5E15
v. ^{Other} N, means except the case N-950

Table. 7.8 - Summary of comparison between fluorinated, oxynitrided, and conventional thermally-grown oxides.

7.8 Chapter 7 Contributions

The comparison the three different type of oxides, the fluorinated, the oxynitrided, and the control, provides conclusions about the characteristic response of the oxides under CCFN stress. The whole comparison exposes the differences between charge components generated under (+) bias and (-) gate biases. These differences are due to the unsymmetrical structure of MOS capacitor.

The comparison also shows common behaviors of oxides. There might be only one set of hole traps in the bulk oxide for both (+) and (-) gate bias. However, the set of positive charge at/near the poly/SiO_2 interface is different from the mentioned set of positive charge in the bulk. The clear evidence is the set of hole traps near the poly/SiO_2 interface possesses a "slower" hole-capture cross-section [80]. Also the interface state density created under (+) is twice as great as the interface state density created under (-) bias [80].

Under (+) gate bias, the oxynitrides are shown to be better than the control and the fluorinated oxides. However, under (-) gate bias, charging near the poly/SiO_2 interface is detrimentally affected. To benefit from the advantage of oxynitrides under (+) bias, one could use the lower temperature oxynitrides, which may avoid detrimental affects of oxynitridation under (-) bias.

If used, the fluorinated oxides would require n-type threshold adjustments, whereas the oxynitrides would require p-type threshold adjustments.

CHAPTER 8

Channel Hot Carrier Stress of Oxynitrided-Gate nMOSFETs

It is commonly believed that the degradation of devices under channel hot carrier stress is caused by impact ionization [27, 58]. In order to reduce damage at a drain region caused by channel hot electron (CHE) injection, graded drain structures such as double-diffused drain (DDD), lightly doped drain (LDD) and other variations, have been employed [56-57]. These structures can reduce the electric field in the drain space charge region and/or change the locations of impact ionization [57]. However, the main issue in CHE injection still concerns the dimension of devices being scaled down to sub-micrometer. The damage caused by CHE injection in short channel devices is still substantial, even when DDD, or LDD are used in the process [13, 56, 59]. Thus, one approach is the improvement of the quality of the gate oxide and of the Si/SiO_2 interface to reduce the trap centres during hot carrier injection.

This chapter investigates the effect of channel hot carrier stress on nMOSFET devices fabricated with oxynitrides as gate dielectrics. The same family of oxynitrides, N_2O-treated at temperatures from 850°C - 1050°C, are used as gate dielectrics in nMOSFETs having a range of dimensions (see Section 4.1.2.2). These are compared with devices made using thermally-grown control oxide.

8.1 Electrical Set-up For Measurements In Channel Hot Carrier Injection Stress.

The procedure to do CHE stress is listed as following:

• In order to avoid confusing measurements, only devices having low gate leakage were used for channel hot carrier tests. The devices were selected by a pre-test, where the drain (D), source (S), and body (B) were grounded, while a DC source of 5V was applied to the gate. Only devices with gate current under 1pA were used.

• Next, the snapback voltage (V_{SNB}), was obtained for each usable device. The curve g_m vs. V_{DS} (for V_G = 3V) was measured. V_{DS} was swept from 0-8.5V for devices with W = 50μm, and from 0-7V for devices with W = 1.5μm. The snapback voltage then was determined graphically as shown in Fig. 8.1. Since these voltage sweeps could potentially damage a device, a substatntial number of cases was re-verified after a sweep. In all cases, no degradation is observed due to this initial sweep.

• Device degradation characteristics were determined by the shift of threshold voltage (ΔV_{th}), and the reduction of transconductance (g_m). The standard technique used to measure the threshold voltage in the saturation region uses extrapolation of the linear region on $\sqrt{I_D}$ versus V_{GS} curves. To carry out this measurement, the gate and the drain are tied together, and swept from 0 to 1.5V in 0.1 volt increments.

• The maximum g_m was determined for each device, before and after 30,000 seconds of stress, by setting V_{DS} = 0.1V and V_{GS} = 3V. In this way, degradations in maximum g_m were observed.

• The stress condition (V_{GS} and V_{DS}) was determined from the plot of substrate current (I_{sub}) vs. V_{GS} for a given V_{DS} (which must be in the saturation region, but below V_{SNB}). The value of V_{GS} is chosen to obtain the maximum substrate current (I_{submax}). To obtain the plot of lifetime (τ) vs. I_{sub} or I_{sub} /W, devices were stressed at several different values of I_{submax}

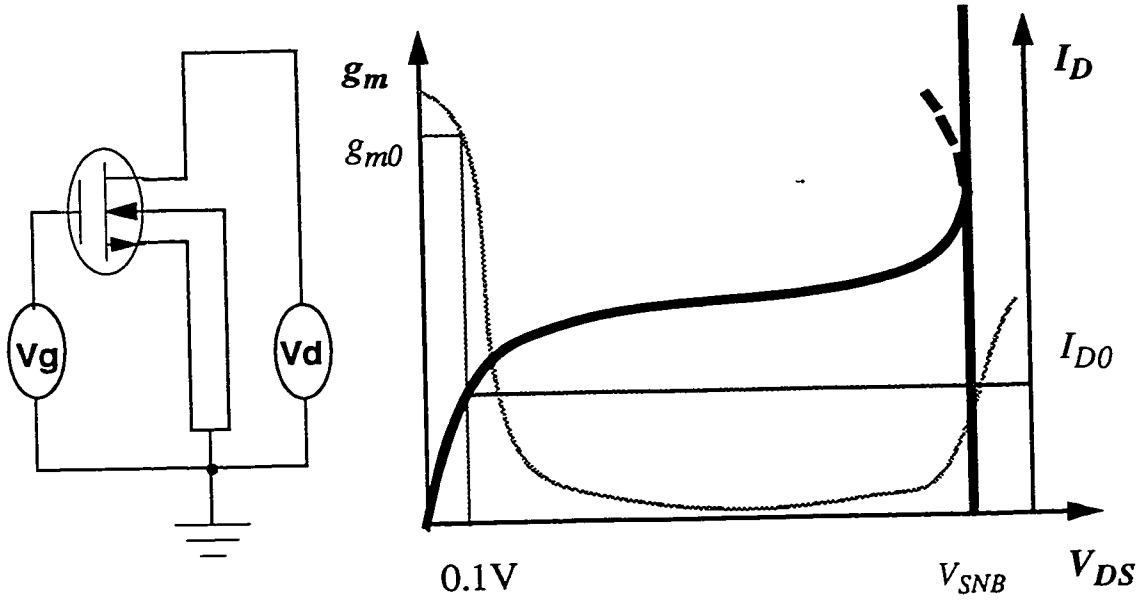


Fig. 8.1 - Circuit schematic used to measure g_m vs. V_{DS}. The graph at right illustrates how V_{SNB} is determined. g_{m0} is measured at V_{DS} = 0.1V, in the linear regime, and is used to track transconductance changes (reduction) as a function of stress.

8.2 Experimental Results

8.2.1 Pre-Stress Measurements:

In devices having W = 50μm, the values of V_{SNB} were found to be the same for all devices. In narrow devices (W = 1.5μm), with channel lengths larger than 1.0μm, no dif-

ferences in snapback voltage were observed between the different oxynitrided and control cases [82]. However, in narrow devices, with sub-micron channel length, different snapback voltages were observed in the different cases. Fig. 8.2(a) shows the variation of transconductance with respect to V_{DS} for devices with W = 1.5μm and L = 1.5 μm. Fig. 8.2(b) shows the same measurement for devices with W = 1.5 μm and L = 0.8μm. Table 8.1 shows snapback voltages estimated from g_m vs. V_D curves for devices with various channel lengths.

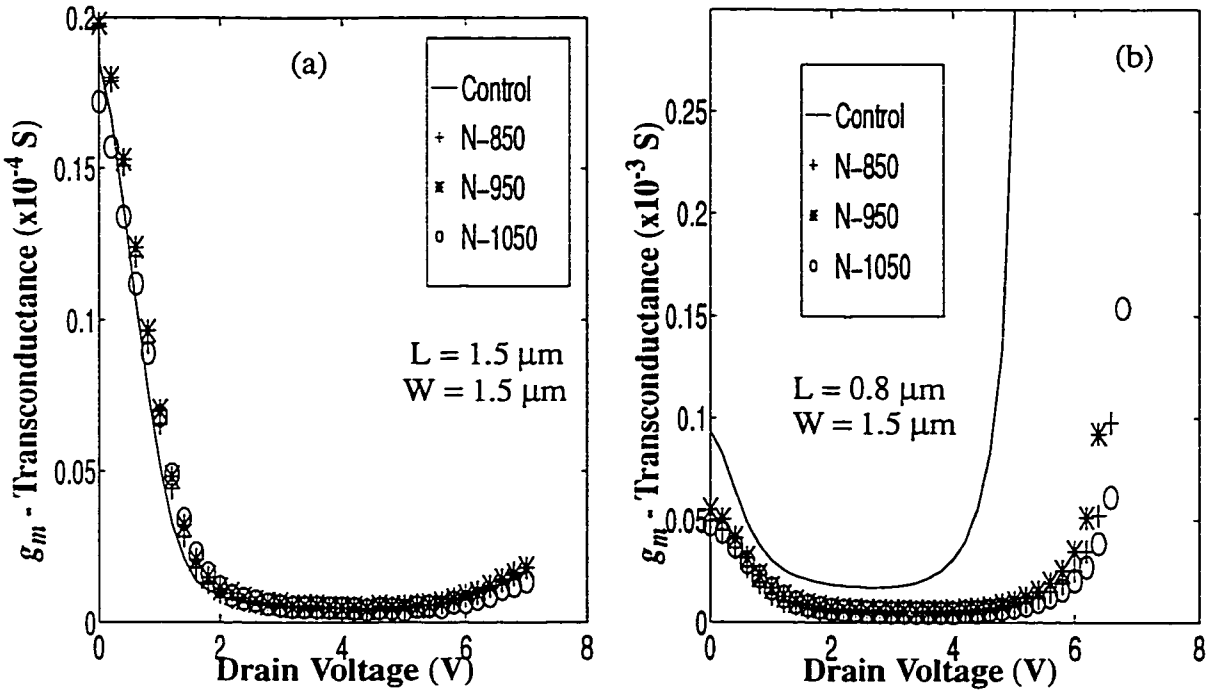


Fig. 8.2 - Variation of transconductance vs. V_{DS}. V_G = 3V, V_S =V_B = 0V. Two cases are shown: (a) L = 1.5μm, W = 1.5 μm; and (b) L = 0.8μm, W = 1.5 μm.

Gate Length	1.5 μm	1.2 μm	1.0 μm	0.8μm
Control	> 6.0V	> 6.0V	~ 5.2V	~ 4V
N-850°C	> 6.0V	> 6.0V	~ 5.8V	~ 5.5V
N-950°C	> 6.0V	> 6.0V	~ 5.8V	~ 5.5V
N-1050°C	> 6.0V	> 6.0V	~ 5.8V	~ 5.5V

Table. 8.1 - Graphically-estimated V_{SNB} vs. gate length, where W = 1.5.μm.

Figs. 8.3 show the maximum substrate current (I_{submax}) for devices of various channel widths and lengths (The substrate current is generated due to ionization of silicon atoms by hot electrons.). The maximum substrate current is reduced for the oxynitrided samples compared to the control samples. The reduction is greatest for the highest oxynitridation temperatures. This suggests that, *the impact ionization of silicon atoms due to hot electrons may be reduced for devices with oxynitrides* [82].

Fig. 8.4 shows V_{th} variations vs. channel length. As the figure shows, the short channel effect is much smaller for the oxynitrided devices than for the control devices. *Higher temperature oxynitrided devices have less-severe short channel effects.*

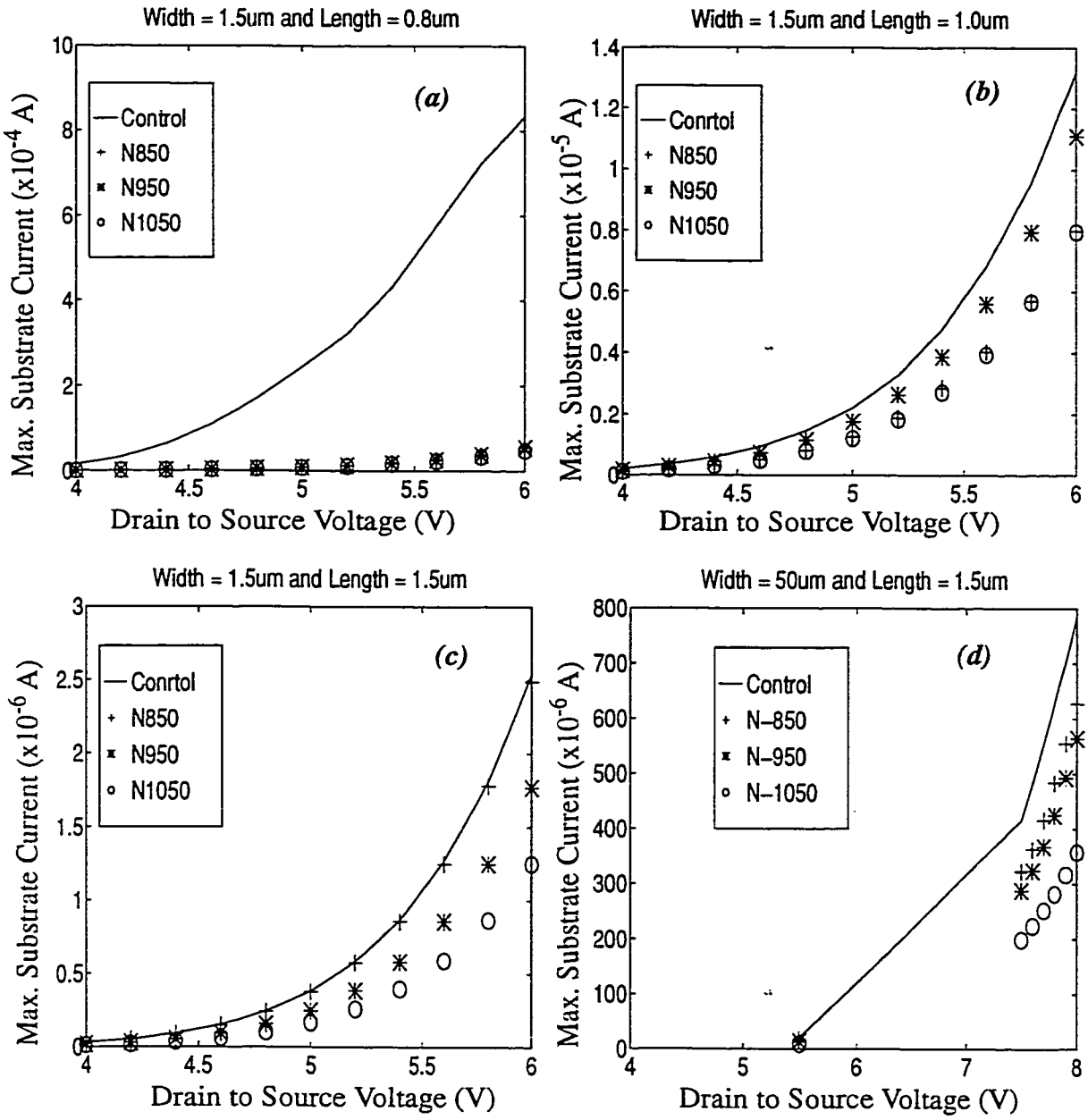


Fig. 8.3 - The maximum substrate currents of nMOSFET for: (a) L =0.8μm, and W = 1.5μm, (b) L =1.0μm, and W = 1.5μm, (c) L =1.5μm, and W = 1.5μm, (d) L =1.5μm, and W = 50μm.

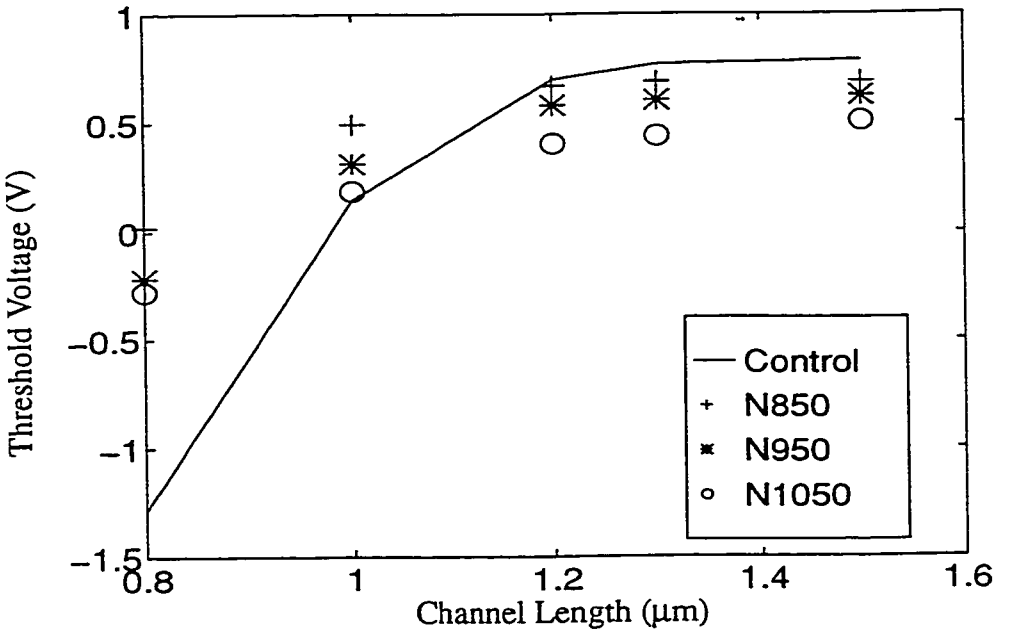


Fig. 8.4 - Threshold voltage vs. channel length.

8.2.2 Post-Stress Measurements:

Figs. 8.5 (a), (b) show the reduction in transconductance and threshold voltage shifts vs. channel lengths for devices with W = 1.5μm, after applying 30,000 seconds of channel hot electron stress. The stress condition for each device was chosen at a fixed V_{DS} while V_{GS} was applied at a value to give maximum substrate current, I_{submax}. The transconductance reduction and threshold voltage shift are most obvious in devices with channel length less than 1μm. The most severe degradations are seen in the control oxide. The smallest shifts are seen for the devices made with the highest N_2O treatment temperatures.

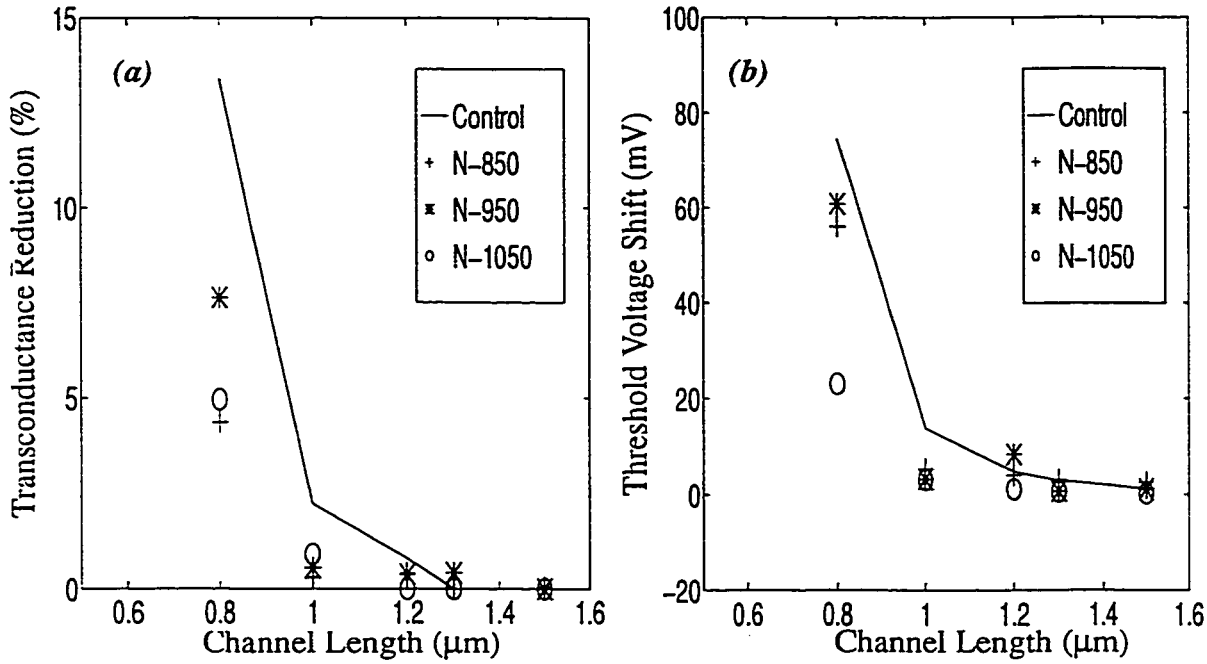


Fig. 8.5 - a) Reduction of Transconductance, g_m; and b) Threshold voltage shifts of n-MOSFET devices. Channel width W = 1.5μm. Stress duration = 30,000 sec. Applied V_D = 5V. $V_{G\ (Isubmax)}$ was chosen such that I_{sub} was at maximum for each tested sample. V_S = V_B = 0V. Transconductance values were measured at V_G = 3V, V_S=V_B = 0V, and V_D = 0.1V.

Fig. 8.6 shows device lifetimes, with respect to substrate current per unit width (I_{sub}/W) for various devices. The empirically-found variation [57-58] of device lifetime (τ) versus I_{sub} given as:

$$\tau \propto (I_{sub})^{-1} \tag{8.1}$$

The lifetime, τ, is defined as the time for a threshold voltage shift of 50 mV, at the device operating voltage. τ is estimated using accelerated testing, by measuring the time to a threshold voltage shift of 50 mV at higher stress voltages. The data for two of the oxynitrided cases is compared to the control in Fig. 8.6. Estimated slopes on this log-log graph are listed in Table 8.2.

In Fig. 8.6, the slope of τ vs. I_{sub}/W for N-950 devices, is higher than that of the control and N-850 devices, in agreement with Wright *et al*'s report [40]. Since τ is proportional to the inverse of I_{sub} (see Eq. 2.8) [58], the steeper slope for N-950 means these N-950 devices require higher minimum energy to create trapped charges in the Si/SiO_2 interface.

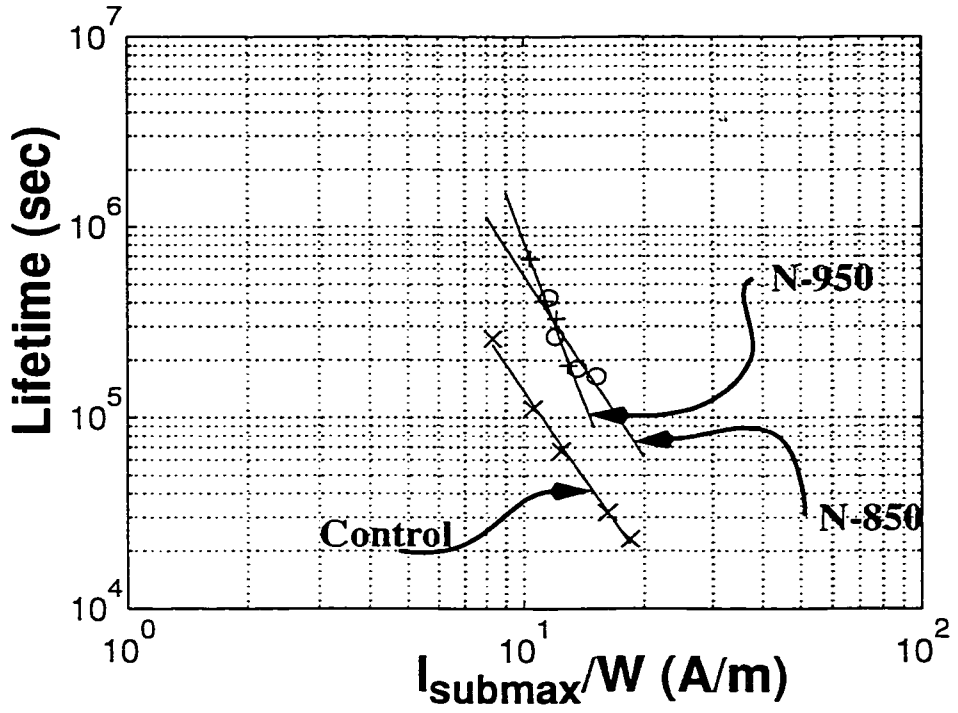


Fig. 8.6 - Dependence of device lifetime, defined as the time to ΔV_{th} = 50 mV, on I_{submax}/W.

Oxides	Slope
Control	-3.02
N-850°C	-3.16
N-950°C	-5.54

Table. 8.2 - Extracted slopes from Fig. 8.6.

8.3 Discussion

8.3.1 Pre-Stress:

In Fig. 8.4, for devices with L = 0.8μm the threshold voltage difference between nitrided cases and the control is about 1.0V. This difference, however does not show in devices having channel length greater than 1.5μm. Thus the short channel effect is more severe in the control than in nitrided oxides for sub-micron devices. There may be more impact ionization events occurring in the control device than in the nitrided devices. This may lead to a smaller snapback voltage in control devices compared to those with oxynitrided gates (Fig. 8.2) [82]. The high values of substrate current in the control devices (Fig. 8.3(a)) support this suggestion.

By employing the oxynitridation technique, the short channel effect is reduced in sub-micron nMOSFET devices. The device performance can thus be improved significantly by using oxynitrided gates.

8.3.2 Post-Stress:

Our measurements in Fig. 8.5 show that under CHE injection stress, nitrided devices degrade substantially slower than the control device in the short-channel (≤ 1μm) range. If the view is accepted that the degradation is caused by hot electrons injected into the oxide [43], causing charge trapping at the Si/SiO_2 interface (near to the drain) and in the bulk oxide, then the results in Fig. 8.5 are in accord with the findings of Refs. [13, 27, 31, 79], where the replacement of H by N atoms increases the resistance of thin MOS gate oxides to hot carrier injection stress.

Also, in Fig. 8.5 the degradation is approximately the same for all devices having length greater than 1μm. However, when the device length is 1μm or less, the degradation in the control case is larger than in the nitrided cases.

In Fig. 8.6, results for two nitrided devices show better reliability for nitrided devices in high field stress. Furthermore, the curves for N-850 and N-950 cross each other (Fig. 6). This can be interpreted to mean that, at low field more time is required for an N-950 device to degrade than an N-850 device.

8.4 Conclusions

In summary, the effects of oxynitridation on MOS device function include:

- The short channel effect is reduced.

- The resistance to channel hot carrier injection is enhanced, and fewer trapped charges are generated in the gate oxide.

8.5 Chapter 8 Contributions

A plan to study the effect of oxynitridation under channel hot carrier injection stress was executed. The results showed that the oxynitrided-gate oxide nMOSFETs possess better quality than the control samples.

From pre-stress data for short channel length devices (L = 0.8μm), the oxynitrided devices show that there was likely less impact-ionization. The oxynitridation also reduces

the short channel effect on nMOSFET devices. The pattern of the variation in impact-ionization and short channel length effect in oxynitrided devices is: devices with *higher oxynitridation temperature show better performance.*

The post-stress data show that oxynitrided devices possess better resistance to channel hot carrier injection. Oxynitridation is likely to enhance the reliability of CMOS devices if applied to a sub-micrometer process.

CHAPTER 9

SUMMARY OF CONTRIBUTIONS, AND SUGGESTION FOR FUTURE WORK

9.1 Over View

This study examined the characteristics of three different types of gate oxides: the control, fluorinated, and oxynitrided oxides. The main lines of this work as stated in Section 1.4, are:

- Development of an electrical characterization technique, based on a variation of the DiMaria framework.

- Study of fluorinated gate oxides.

- Study of oxynitrided gate oxides.

- Comparison of both techniques: oxynitridation and fluorination.

DiMaria's framework was employed to plan the electrical-characterization strategies using both (+) and (-) gate bias Fowler-Nordheim stress. By the use of this framework, charge components induced during Fowler-Nordheim stresses in the gate oxides were extensively investigated. The analysis of the obtained data demonstrate a complex

scenario of locally-induced charges in the gate oxides. To further investigate the effects of fluorine and nitrogen incorporated into the gate oxides, a graphical model was used to evaluate reliability of gate oxides. An empirical model was also suggested to study the rate of change of electron trapping rates.

For fluorination, the use of before- and after-poly-etch pairs provides substantial data to support the validity of the strain-relaxation model proposed by Ma [14], and Wright and Saraswat [12].

Under (+) gate bias, fluorinated and oxynitrided oxides showed better qualities than the conventional thermally-grown oxides in aspects such as: interface states densities (D_{it}), anomalous positive charge (APC), electron trapped charge, and electron trapping rate (see Table 7.8). However, the observed advantages in (+) gate bias of fluorinated and oxynitrided samples were compromised by the results in (-) gate bias. The main problem appearing in (-) gate bias came from the large amount of positive trapped charge which is generated at/near the poly/SiO_2 interface.

Similar phenomena are observed in the oxynitrided gate oxides. While the analysis of (+) gate bias data shows a substantial improvement using oxynitridation, the (-) gate bias analysis reveals some detrimental effects caused by oxynitridation, mostly located at/ near the poly/SiO_2 interface. This could be consistent with Hori *et al*'s model [31] and Ellis *et al*'s report [71], in the sense that, higher temperature oxynitridation could cause higher nitrogen concentration at the Si/SiO_2 interface. Higher nitrogen concentration at the Si/SiO_2 interface can cause a thicker nitride layer at the Si/SiO_2 interface. This can lead to a large amount of positive charge at the poly/SiO_2 interface [88].

Channel hot electron stress was carried out on nMOSFET devices which were formed with oxynitride gate oxides. The results are interesting and confirm that the oxynitrides are superior to the control oxides.

Overall, the comparison between three different types of gates oxides, the control, the fluorinated, and the oxynitrided, favors the use of oxynitridation. Oxynitrides are in every respect better than the fluorinated and the control oxides, under (+) gate bias. The drawback of oxynitrides under (-) gate bias can be alleviated by the use of lower oxynitridation temperatures.

9.2 Summary of Contributions

9.2.1 Formation of An Electrical Characterization Technique

Refer to Chapter 3:

- The main contribution of the developed electrical characterization technique in Chapter 3 is the ensemble of techniques, all applied in a coherent manner to evaluate an oxide improvement process technique. This electrical characterization technique covers all conventional oxide-reliability parameters such as flatband voltage shifts and the interface state density, and also reveals further detailed information about the induced charge generated in gate oxide under Fowler-Nordheim stress. The additional information can be tabulated in Table 9.1.

Information Containing Sources		Information obtained	
		Under (+) gate Bias	Under (-) gate bias
	$N_{\Delta Vg}(f)$ (calculated from ΔV_g via Eq. 3.2)	Trapped charge located outside a tunneling distance from the Si/ SiO_2 interface: • Hole trapped charge at low fluence • Electron trapped charge at high fluence	Trapped charge located outside a tunneling distance from the poly/ SiO_2 interface: • Hole trapped charge at low fluence • Electron trapped charge at high fluence
	$N_{ic}(f)$ (calculated from ΔV_{fb} - ΔV_g via Eq. 3.2)	Trapped charge located within a tunnelling distance from the Si/ SiO_2 interface: • Electron trapped charge • APC at high fluence	Trapped charge located within a tunnelling distance from the poly/SiO_2 interface: • Hole trapped charge at low fluence • Electron trapped charge at high fluence
	$d(N_{\Delta Vg}(f))/df$ (Applied only for $N_{\Delta Vg}(f)$)	• Hole trapping rate at low fluence • Electron trapping rate at high fluence	• Hole trapping rate at low fluence • Electron trapping rate at high fluence
	The rate of change of the trapping rate, K_1, in Eq. 3.3 (Used only for $d(N_{\Delta Vg}(f))/df$)	How fast the trapping rate decreased from the dominant region of hole trapping rate to the dominant region of electron trapping rate.	How fast the trapping rate decreased from the dominant region of hole trapping rate to the dominant region of electron trapping rate

Table. 9.1 - Information gained from the electrical characterization technique developed in Chapter 3.

• To evaluate the reliability of gate oxides under (+) gate bias, a graphical model is also developed, based on the above-mentioned electrical characterization technique (in Section 3.2.3.2). For oxides which have the positive maxima located almost at the same fluence in the plot of $N_{\Delta vg}(f)$ vs. f, reliabilities can be compared by this method. Some

parameters, like the zero-crossing fluence, and the saturation Si/SiO_2 interface trapped charges, then, can be used to discuss or compare reliabilities of oxides.

9.2.2 Study of Fluorine Incorporated Into Gate Oxides

Refer to Chapter 4:

- The results obtained agree with reported literature in:

  - ❒ Fluorination reduces the shift of interface state densities, D_{it} under a Fowler Nordheim stress. For example, for an injected fluence of 0.025 C/ cm^2, the shift in midgap D_{it} of fluorinated samples implanted with $2x10^{15}$ / cm^2 at 25KeV is around $2x10^{11}$ $eV^{-1}cm^{-2}$. This value was also found by Refs. [15, 25].

  - ❒ Fluorination decreases the flatband voltage shifts under a Fowler-Nordheim stress.

  - ❒ Fluorination decreases the shift in $\Delta(Q_f + Q_{it}(0) + Q_{ox})$, under a Fowler-Nordheim stress.

- By the use of combination of *j-t* and C-V techniques, the scenario of charge component induced by Fowler-Nordheim stress is demonstrated to be quite complex.

- Therefore, a simple FN stress test can lead to misconceptions about the oxide reliability. For more accurate analysis, a more comprehensive plan must be enacted to characterize any oxide.

• The *j-t* technique analysis shows that electron trapped charges generated in the bulk oxide are reduced when fluorination is employed.

• Analyses also show that there is the appearance of anomalous positive charge (APC) in the control oxide. But the generation of this type charge, APC, during Fowler-Nordheim stress is reduced or suppressed by fluorination.

Refer to Chapter 5:

• An extensive study of fluorination incorporation into gate oxides was planned and executed. The study was done using both positive and negative gate bias CCFN. The study showed the complex scenario of charge components generated in different locations in gate oxides in both (+) and (-) gate biases.

• In general, while fluorinated samples still show advantages over the control sample, the effects usually do not show up as clearly as they did in the pilot study, in Chapter 6. This confirms and reminds us that the impact of any variation on a complete fabrication process can be both subtle and complex. The advantages which fluorination gains in an abbreviated process can be at least partly cancelled out by steps in the back-end process.

This study extends the knowledge base of fluorinated gate oxides in the specific points which are tabulated in Table 9.2.

Aspects Analyzed		Detailed contributions from fluorination study[i]	
		Under (+) gate Bias	Under (-) gate bias
	D_{it}	• Generally, Fluorinated cases show less induced D_{it} than the control case. • However, the introduction of an excessive amount of fluorine to at/near the Si/SiO_2 interface reduces the good effect of fluorination at/near the Si/SiO_2 interface. This strongly support the strain relaxation hypothesis, proposed by Ma [14] and Wright and Saraswat [15]	
	$N_{\Delta Vg}(f)$	• Hole trapping does not vary significantly due to fluorination • Electron trapping shows a pattern: greater implanted dose leads to lower electron trapping in the bulk	• Higher fluorine dose leads to less hole traps. • Electron trapping dose not shows a systematic variation. Though all fluorinated oxides show less electron traps than the control case.
	$N_{ic}(f)$	• Higher implanted dose leads to higher electron trapped charges at/near the Si/SiO_2 interface. • Fluorination reduces or suppresses APC. Possible optimum dose could be in the range of $6x10^{14}$ /cm^2 to 10^{15} / cm^2 • Excessive amount of fluorine at/near the Si/SiO_2 interface reduces the suppression of APC.	• A large amount of positive trapped charge is induced at/near the poly/ SiO_2 interface. The set of positive charges could have a smaller hole capture cross-section than the induced positive charges in the bulk ($N_{\Delta Vg}$-).
	$d(N_{\Delta Vg}(f))/df$	• No systematic variation in hole trapping rate in the fluorinated samples. Most fluorinated cases have lower hole trapping rates than the control	• No systematic variation in fluorinated samples in hole and electron trapping rate. • Optimal dose is $2x10^{15}$ /cm^2
	K_1 & K_2,	• $2x10^{15}$ /cm^2 is confirmed as the optimal dose for both positive and negative biases in the aspects of the rate of change of the charging rate, saturated charging rate.	

i. Refers to Table 9.1 to see the location in the oxides and at what fluence, high or low, each type of charges taking places.

Table. 9.2 - Contributing information gained from the fluorination study.

9.2.3 Study of Oxynitridation In Gate Oxides

Refer to Chapter 6:

An extensive characterization of oxynitrides is executed. The study is done on both positive and negative gate bias CCFN. The study reveals the complex scenario of charge components generated into different locations in gate oxides in both (+) and (-) gate biases.

This study extends the knowledge base of oxynitrided gate oxides in the specific points which are tabulated in Table 9.3.

		Detailed contributions from oxynitridation study[i]	
		Under (+) gate Bias	Under (-) gate bias
Aspects Analyzed	D_{it}	• All oxynitrides show less generated D_{it} than the control oxide. • Higher temperature oxynitridation leads to less induced interface states density.	
	$N_{\Delta Vg}(f)$	•Positive trapped charges in the bulk oxide shows a non-linear relationship to the oxynitridation temperature. The expected optimal temperature is in the range of 850°C-950°C. • Higher oxynitridation temperature leads to fewer electron traps	• Higher temperature oxynitridation leads to more hole traps, and fewer electron traps. • Induced positive and negative charge of the control are always smaller (better) than the high temperature oxynitrides (1000-1050°C) and larger (worse) than the low temperature oxynitrides (850-950°C).
	$N_{ic}(f)$	• Higher temperature oxynitridation leads to less electron trapped charges at/near the Si/SiO2 interface. • Oxynitridation dramatically suppresses APC.	• A large amount of positive trapped charges is induced at/near the poly/ SiO_2 interface. These charges could have a smaller hole capture cross-section than the induced positive charges in the bulk ($N_{\Delta Vg}$-).
	$d(N_{\Delta Vg}(f))/df$	• Hole trapping rate, in the bulk oxide shows a non-linear relationship to the oxynitridation temperature. The expected optimal temperature is in the range of 850°C-950°C. • Higher temperature oxynitridation leads to lower electron trapping rate.	• Higher temperature oxynitridation leads to higher hole trapping rates. • Hole and electron trapping rates, of the control are always smaller (better) than high temperature oxynitrides (1000-1050°C) and larger (worse) than low temperature oxynitrides (850-950°C).
	K_1 & K_2,	• At low fluence the rate of change of electron trapping rate in the bulk appears to have an optimum at 850°C-950°C	• Higher temperature oxynitridation yields higher the rate of change of electron trapping rate in the bulk.

i. Refers to Table 9.1 to see the location in the oxides and at what fluence, high or low, each type of charges taking places.

Table. 9.3 - Contributing information gained from the oxynitridation study

9.2.4 Comparison Between Fluorination And Oxynitridation

Refers to Chapter 7:

• The comparison of the three different types of oxides, the fluorinated, the oxynitrided, and the control, provides conclusions about the characteristic response of the oxides under CCFN stress. The whole comparison exposes the differences between charge components generated under (+) and (-) gate biases. These differences are due to the asymmetrical structure of the MOS capacitor.

• The comparison also shows common behaviors of oxides. There might be only one set of hole traps in the bulk oxide for both (+) and (-) gate bias. However, the set of positive charge at/near the poly/SiO_2 interface is different from the mentioned set of positive charge in the bulk. The clear evidence is the set of hole traps near the poly/SiO_2 interface possesses a smaller, "slower", hole-capture cross-section [80]. Also the interface state density created under (+) is twice as great as the interface state density created under (-) bias [80].

• Under positive gate bias, the oxynitrides are proven to be better than the control and the fluorinated oxides. However, under (-) gate bias, charging near the poly/SiO_2 interface is detrimentally affected. To benefit from the advantage of oxynitrides under (+) bias, one could use the lower temperature oxynitrides, which may avoid detrimental affects of oxynitridation under (-) bias.

• If used, the fluorinated oxides would require n-type threshold adjustments, whereas the oxynitrides would require p-type threshold adjustments.

9.2.5 Oxynitrided Oxides Under Channel Hot Electron Injection Stress

Refers to Chapter 8

A plan to study the effect of oxynitridation under channel hot carrier injection stress was executed. The results showed that the oxynitrided-gate oxide nMOSFETs possess better quality than the control samples.

From pre-stress data for short channel length devices (L = 0.8μm), the oxynitrided devices suggest that there was less impact-ionization. The oxynitridation also reduces the short channel effect on nMOSFETs. The pattern of the variation in impact-ionization and short channel length effect in oxynitrided devices is: devices with *higher oxynitridation temperature show better performance.*

The post-stress data show that oxynitrided devices possess better resistance to channel hot carrier injection. This is could be due to the fact that oxynitridation reduces the density of trapped charges created/formed in the gate oxides both in the bulk and at/near the Si/SiO_2 interface. Oxynitridation is likely to enhance the reliability of CMOS devices if applied to a sub-micrometer process.

In summary, the effects of oxynitridation on MOS device function include:

- The short channel effect is reduced.
- The resistance to channel hot carrier injection is enhanced, and fewer trapped charges are generated in the gate oxide.

9.3 Suggestions For Future Works

The oxide thickness in these devices is 250-265 Å. In this range of thicknesses, the device degradation may be caused by hot electrons due to Fowler-Nordheim tunneling. The results obtained through this work can be applied to any device in which the degradation mechanism is related to hot electrons generated by Fowler-Nordheim tunneling. However, when the oxide thickness is smaller than 50 Å, the direct tunneling phenomenon dominates. And thus, only a part of the obtained results can be used.

Under direct tunneling, the degradation in the device may be caused by electrons which have low energy levels. Therefore, there is no impact-ionization. In other words, hole trap creation, requiring electrons with energy > 9eV, can be neglected. But electron trap creation, requiring electrons with energy > 2eV, might still exist. Consequently, the results obtained for electron trapping might be useful for processes with oxide thickness smaller than 50 Å.

For giga scale (GLSI) technology, the thickness of the gate oxide is as low as 15-25 Å. In these processes, the poly gate layer is replaced by silicide. And with a such small thickness (15-25 Å), the electron does not need to be "hot" to pass through the gate dielectric layer. Therefore, the obtained results could not be used.

9.3.1 Realize An E^2PROM Fabrication Process In A Sub-Micrometer Process

The main work of this dissertation can be directly applied to create the gate oxides and tunnel oxides of flash-E^2PROM (see Fig. 3.1). Below is a list of tasks relevant for study of behavior of oxynitrides when they are incorporated into a 0.8 μm process[10]:

❒ Since the tunnel oxide is thinner (i.e. 50-100 Å), information about the growth rate of oxynitride is needed at varied temperatures (because a thin oxide needs a low growth temperature).

❒ Since the lifetime of a flash-E^2PROM is dependent on the dielectric time dependent breakdown, study of charge breakdown and voltage breakdown must be carried out. Preparation for oxynitrides (in 0.8μm process) is planned and executed to test the value of charge breakdown and voltage breakdown, both under (-) and (+) gate bias.

❒ Since the E^2PROM structure has two oxide layers, the tunnel oxide and the gate oxide, the breakdown test should be executed for both. Oxynitridation could be a good candidates for these tests.

9.3.2 Other Suggestions

❒ To further study the effect of oxynitridation (also for fluorination) at/near the poly/SiO_2 interface, a poly-poly capacitor is a suitable structure. Applying the same characterization technique shown in Chapter 3, one can get more information from both poly/SiO_2 interfaces in a poly-poly capacitor structure.

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10. In 0.8 mm process, the oxide thickness is around 100 Å

❒ Applying a two-layer or multi-layer ellipsometric model to characterize the thickness, and refractive index of the oxynitrided/fluorinated layer formed by oxynitridation or fluorination. Accurate knowledge of the relative permeabilities of the layers is needed.

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APPENDIX A

RELEVANT DERIVATIONS

A.1 Calculation Of Oxide Trapped Charges Under Fowler-nordheim Hot Carrier Injection Stress

To manipulate the measurement data, first we start with Fowler-Nordheim current:

$$J = AF^2 e^{-\frac{B}{F}} \tag{A.1}$$

where J is current density, F is field near cathode, A (A/MV^2) is a constant characteristic of a specific fabrication processing; and B (MV/cm) is another constant related to the energy barrier of silicon [89]. Initially, there are no charge defects generated, and the field near the cathode interface is equal to the averaged oxide field (i.e. $F = E_{ox}{}^{ave}$, $\Delta Q = 0$). Then Eq. A.1 can be written as:

$$J(0) = A[E_{ox}{}^{ave}(0)]^2 \quad e^{-\frac{B}{E_{ox}{}^{ave}(0)}} \tag{A.2}$$

However, during the electrical stress, trapped charges are generated. Then the value of ΔQ will be changed (i.e. $\Delta Q \neq 0$). Note that $E_{ox}{}^{ave}$ is the averaged oxide field near the cathode (negative polarity). With the addition of an amount of charge, ΔQ, introduced to MOS oxide system at the time t, the field near the cathode will be:

$$E_{cathode} = E_{ox}{}^{ave}(t) - \frac{\Delta Q \bar{x}}{\varepsilon_{ox} L} \tag{A.3}$$

where $\bar{x}$ is the centroid of the just-introduced charge ΔQ, L is oxide thickness. The (-) sign presents for the meaning that the field near cathode is reduced if the added charge is positive; and the field near the cathode is increased if the added charge is negative. Because of the change of the field near cathode, now Eq. A. 2 will be written after a stressing time t, as:

$$J(t) = A\left(E_{ox}{}^{ave}(t) - \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}\right)^2 \quad e^{-\frac{B}{E_{ox}{}^{ave}(t) - \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}}} \tag{A.4}$$

Where $\bar{x}$ is the centroid of the bulk charge, L is the oxide thickness as in Eq. A. 3.

Since the gate bias is kept constant, $E_{ox}{}^{ave}$ = const. Dividing Eq. A.4 by Eq. A.2 on both sides, we then achieve the following equation:

$$\frac{J(t)}{J(0)} = \frac{\left(E_{ox}{}^{ave} - \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}\right)^2}{(E_{ox}{}^{ave})^2} \; e^{-\left\{\frac{B}{E_{ox}{}^{ave} - \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}} - \frac{B}{E_{ox}{}^{ave}}\right\}} \tag{A.5}$$

Practically,

$E_{ox}{}^{ave} \gg \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}$, then Eq.A.5 can be re-written as:

$$\frac{J(t)}{J(0)} \cong e^{-B\left\{\frac{\frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}}{(E_{ox}{}^{ave})^2}\right\}} \tag{A.6}$$

Taking the logarithm of both sides of Eq.A.6, we achieve

$$\ln\left(\frac{J(t)}{J(0)}\right) \cong \frac{B(\Delta Q\bar{x})}{(E_{ox}^{ave})^2(\varepsilon_{ox}L)} \tag{A.7}$$

Consequently,

$$\Delta Q \cong \frac{(\varepsilon_{ox}L)(E_{ox}^{ave})^2 \ln\left(\frac{J(t)}{J(0)}\right)}{B\bar{x}} \tag{A.8}$$

For the thick gate oxides, usually $L/\bar{x} \cong 1$, then Eq.A.8 will become

$$\Delta Q \cong \frac{\varepsilon_{ox}(E_{ox}^{ave})^2 \ln\left(\frac{J(t)}{J(0)}\right)}{B} \tag{A.9}$$

With the above derivation, in 1993, DiMaria [43] presented the following equation, which is actually the same as Eq.A.9. The number of traps generated in bulk oxide during an electrical stress (after a time t) is:

$$N(t) \cong \frac{\varepsilon_{ox}(E_{ox}^{ave})^2 \ln\left(\frac{J(t)}{J(0)}\right)}{qB} \tag{A.10}$$

where B is a process constant and is equal to:

$$B = \frac{4(2m_e^*)^{\frac{1}{2}}(\phi_b)^{\frac{3}{2}}}{3hq} \tag{A.11}$$

where h is Plank's constant divided by 2π, m_e^* is the effective mass of a tunneling electron (usually taken as 0.5 times the mass of a free electron), and ϕ_b is the cathodic energy barrier height (3.1eV for the Si/SiO_2 interface). Thus based on two equations, Eqs. A.10-11), one can calculate the charged defects generated during a Fowler-Nordheim con-

stant voltage hot carrier injection stress. The Eq. A.10, is the main equation of the so-called *j-t* technique.

Similar to the *j-t* technique is the constant current Fowler-Nordheim (CCFN) hot carrier injection stress. This method was used long before the *j-t* technique. However, CCFN and *j-t* have shared the same principle in that the defects generated in gate oxides are caused by the Fowler-Nordheim tunneling phenomenon. The aim of application of this technique is to monitor the oxide charge and Si/SiO_2 interface state densities. The charge defect is calculated by the shift of gate voltage instead of the logarithm of ratio of currents. From Eq.A.2 and Eq.A.4, since $J(0) = J(t)$ (for constant current stress), then

$$[E_{ox}{}^{ave}(0)]^2 \quad e^{-\frac{B}{E_{ox}{}^{ave}(0)}} = \left[E_{ox}{}^{ave}(t) - \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}\right]^2 \quad e^{-\frac{B}{E_{ox}{}^{ave}(t) - \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L}}} \tag{A.12}$$

In order to have both sides of Eq. A.12 equal to each other, the solution for this equation is:

$$E_{ox}{}^{ave}(0) = E_{ox}{}^{ave}(t) - \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L} \tag{A.13}$$

Because $E_{ox}{}^{ave}$ is the averaged oxide field near the cathode (negative polarity), then Eq. A.13 can be written as:

$$\frac{V_g(0)}{L} = \frac{V_g(t)}{L} + \frac{\Delta Q\bar{x}}{\varepsilon_{ox}L} \tag{A.14}$$

$$\text{or } \Delta V_g = -\frac{\Delta Q\bar{x}}{\varepsilon_{ox}} \tag{A.15}$$

The above Eq. A.15, is the main equation used to calculate the charge defects under a constant current Fowler-Nordheim stress. For a thick oxide, Eq.A.15 will become:

$$\Delta V_g = -\frac{\Delta QL}{\varepsilon_{ox}} \tag{A.16}$$

A.2 Density Of Interface Traps

First, we take a look at Fig. A.1. This plot shows the band bending vs. depth, with respect to the silicon surface. ψ_s is the energy difference between the surface and (deep in) the bulk of silicon. The Fermi level, a solid horizontal line, is a distance ϕ_B (in eV) above the intrinsic level in the bulk (dashed dotted line). An arbitrary energy level in the bulk (dashed line), shown by a distance ζ above the intrinsic level. This energy level at the silicon surface is located at a distance of ζ_s.

Thus the relation of ζ and ζ_s can be derived as follows:

$$\zeta_s = \zeta - \phi_B + \phi_s \tag{A.17}$$

$$\zeta_s = \zeta - \phi_B + (\psi_s + \phi_B) \tag{A.18}$$

$$\text{Then} \quad \zeta_s = \zeta + \psi_s \tag{A.19}$$

Now let $D_{it}(\zeta_s)$ be the *probability* per unit area that an interface trap level is present with energy (in eV) between ζ_s and $\zeta_s+d\zeta_s$. $D_{it}(\zeta_s)$ is commonly called the density of interface trap levels per unit area per electron volt [90].

With the use of Eq. A.Eq. 19, $D_{it}(\zeta_s) = D_{it}(\zeta+\psi_s)$. Thus, the interface trap charge density per unit area $Q_{it}(\psi_s)$ can be defined at any ψ_s. This definition depends on the

donor or acceptor nature of the interface traps [90]. Donor interface traps are positive when filled or neutral when empty. Therefore, for donor interface traps (superscript *d*):

$$Q_{it}^{d}(\psi_s) = q \int_{\left(\frac{E_v}{q}-\psi_s\right)}^{\left(\frac{E_c}{q}-\psi_s\right)} [1-f_o(\zeta-\phi_B)]\ D_{it}^{d}(\zeta+\psi_s)\ d\zeta \qquad \text{(A.20)}$$

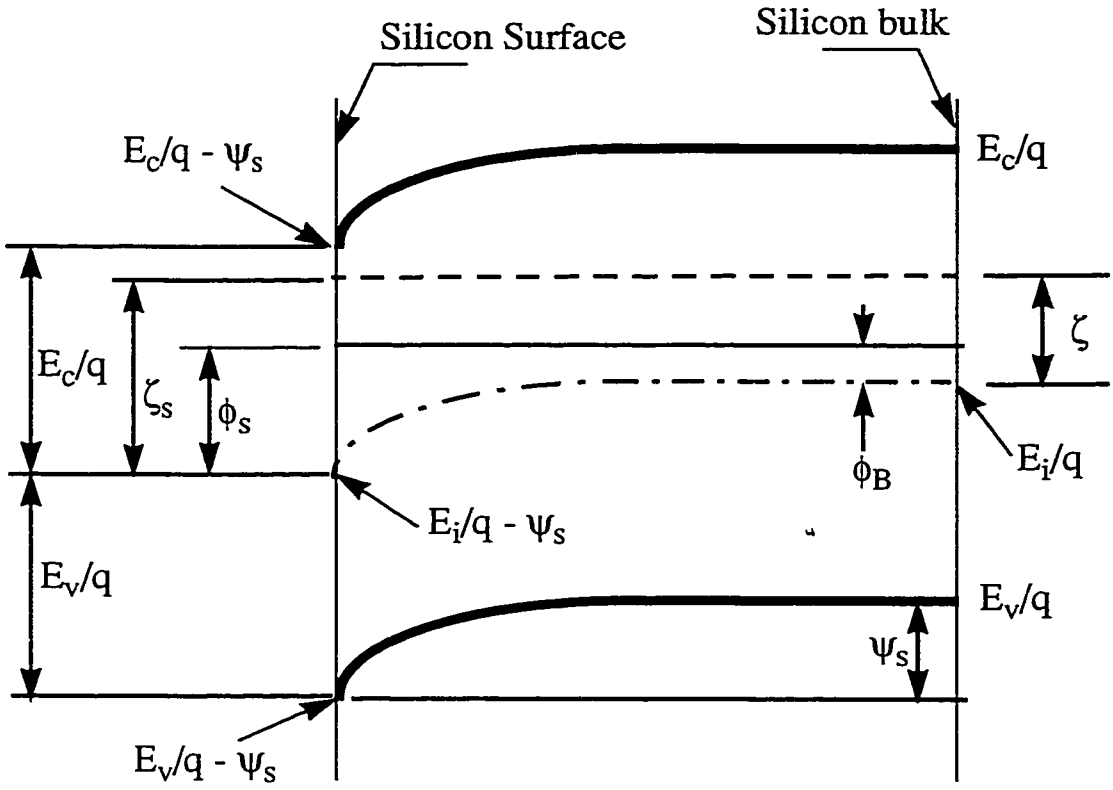


Fig. A.1 - Band bending versus depth from silicon surface illustrating the notation ζ_s and ϕ_s for energies measured from the intrinsic level at the silicon surface [90].

where, as shown in Fig. A.1, ϕ_B is the Fermi level measured from the intrinsic level in the bulk., $(E_c/q - \psi_s)$ and $(E_v/q - \psi_s)$ locate the band edges at the silicon surface

relative to the intrinsic level in the bulk silicon; and $f_o(\zeta - \phi_B)$ is the Fermi function as Eq. A.21.

$$f_o(E) = \frac{1}{1 + \exp[(q(E - \phi_B))/(kT)]} \tag{A.21}$$

And for acceptor interface traps, since they are neutral when empty and negative when filled, then the interface trap charge for acceptor (superscript *a*):

$$Q_{it}^{a}(\psi_s) = (-q) \int_{\left(\frac{E_v}{q} - \psi_s\right)}^{\left(\frac{E_c}{q} - \psi_s\right)} f_o(\zeta - \phi_B)\ D_{it}^{a}(\zeta + \psi_s)\ \ d\zeta \tag{A.22}$$

The net interface trap charge per unit area, $Q_{it}(\psi_s)$

$$Q_{it}(\psi_s) = Q_{it}^{d}(\psi_s) - Q_{it}^{a}(\psi_s)$$

$$Q_{it}(\psi_s) = q \int_{\left(\frac{E_v}{q} - \psi_s\right)}^{\left(\frac{E_c}{q} - \psi_s\right)} D_{it}^{d}(\zeta + \psi_s)\ d\zeta - q \int_{\left(\frac{E_v}{q} - \psi_s\right)}^{\left(\frac{E_c}{q} - \psi_s\right)} f_o(\zeta - \phi_B)\ \{D_{it}^{d}(\zeta + \psi_s) + D_{it}^{a}(\zeta + \psi_s)\} d\zeta \tag{A.23}$$

If the variable ζ under the integrals is changed to $\zeta s = \zeta + \psi_s$ (as Eq. A.19) then Eq. A.23 can be written as:

$$Q_{it}(\psi_s) = q \int_{\frac{E_v}{q}}^{\frac{E_c}{q}} D_{it}^{d}(\zeta_s)\ d\zeta_s - q \int_{\frac{E_v}{q}}^{\frac{E_c}{q}} f_o(\zeta_s - \phi_B - \psi_s)\ \{D_{it}^{d}(\zeta_s) + D_{it}^{a}(\zeta_s)\} d\zeta \tag{A.24}$$

Thus a very small incremental change in band bending $d\psi_s$ will cause a small change in Q_{it}, dQ_{it} (by taking the derivative of $Q_{it}(\psi_s)$ in Eq. A.24 with respect to ψ_s) [90]:

$$\frac{dQ_{it}}{d\psi_s} = q\int_{\frac{E_v}{q}}^{\frac{E_c}{q}}\left(\frac{kT}{q}\right)f_0(\zeta_s-\phi_B-\psi_s)[1-f_0(\zeta_s-\phi_B-\psi_s)]\times[D_{it}^{d}(\zeta_s)+D_{it}^{a}(\zeta_s)]d\zeta \qquad (A.25)$$

Where the following derivative has been used:

$$\frac{df_o(\zeta_s-\phi_B-\psi_s)}{d\psi_s} = \frac{-kT}{q}f_o(1-f_o) \qquad (A.26)$$

Thus, Eq. A.25 shows that the change in the interface trap charge is determined by the ***sum*** of probabilities for donor and acceptor interface traps. Experimentally, there is no technique to measure these two different types of interface traps. Therefore, the total probability density of interface trap energy levels, $D_{it}(\zeta_s)$ is a very important (and also popular) parameter in MOS characterization. The total probability density of interface trap energy levels is defined [90] as:

$$D_{it}(\zeta_s) = D_{it}^{d}(\zeta_s)+D_{it}^{a}(\zeta_s) \qquad (A.27)$$

A.3 High Frequency Capacitor Voltage Measurement And Low Frequency Capacitor Voltage Measurement

Fig. A.2(a) illustrates a set-up for doing either high frequency or low frequency C-V measurements. The voltage is swept in a range such that the substrate immediately

beneath the Si/SiO_2 is in accumulation, depletion or inversion. At each voltage, the value of capacitance is recorded.

Thus, based on the recorded capacitance and corresponding voltage such plots as ones (dashed curves) shown in Fig. A.2(b) can be experimentally obtained. The solid curves (in Fig. A.2(b)) present for HF C-V and LF C-V curves of an n-substrate MOS capacitor with a charge free oxide. Based on the amount and position of oxide charges the CV curves can be different from the ones of a MOS capacitor with a charge-free oxide. This difference may include change of horizontal position or/and some distortion (dashed curves in Fig. A.2), and is used to obtain information about oxide charges and Si/SiO_2 interface states.

The most important parameter extracted from the HF C-V curve is the flatband voltage. By the definition of flatband condition thus the band bending energy level, $\psi_s = 0$. And the calculation of V_{fb}:

$$V_{fb} = W_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(0)}{C_{ox}} - \frac{Q_s(0)}{C_{ox}} - \frac{Q_m}{C_{ox}} \tag{A.28}$$

where W_{ms} is the work function of metal and silicon, $Q_{it}(0)$ is the interface trapped charge at the band bending energy is zero, $Q_s(0)$ is the surface charge at the band bending energy is zero (a constant for each sample), and Q_f and Q_m are the oxide fixed charge and mobile ionic charge, respectively. Practically, $Q_s(0)$ does not need to be zero for non uniform doping profiles.

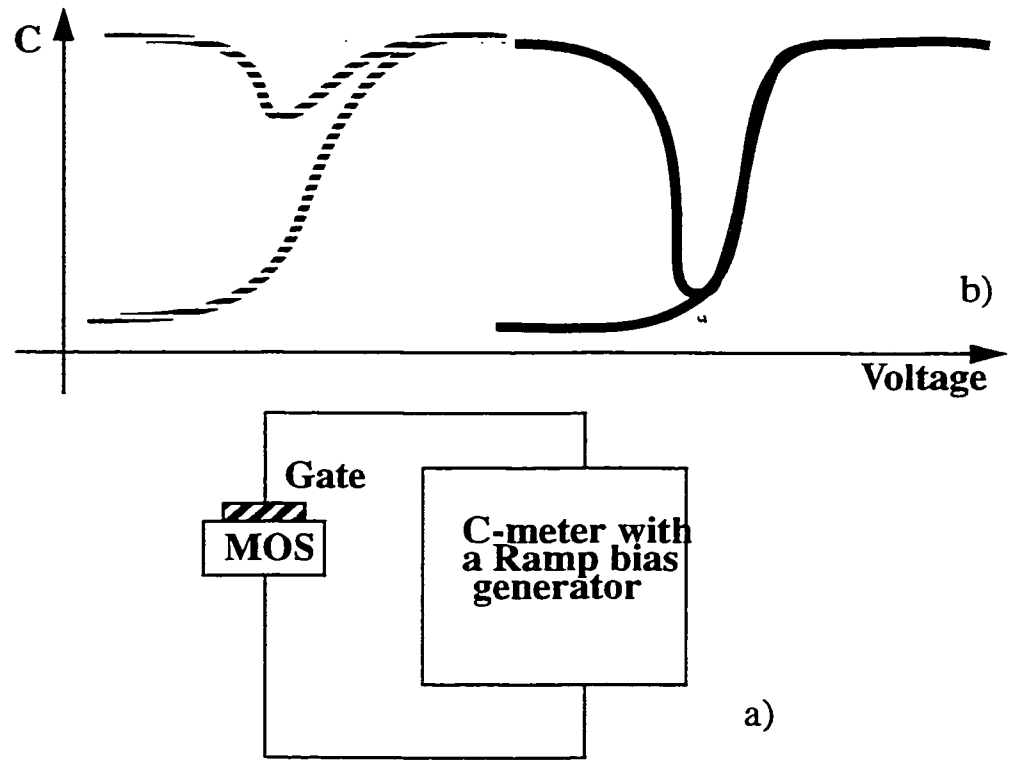


Fig. A.2 - a) Schematic setup; b) Display typical high frequency and low frequency C-V curves before (solid lines) and after (dashed lines) electrical stress.

In the case where mobile charges exist in the gate oxide, the Eq. A.28 can become:

$$V_{fb} = W_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(0)}{C_{ox}} - \frac{Q_s(0)}{C_{ox}} - \frac{Q_m \gamma_m}{C_{ox}} \qquad \text{(A.29)}$$

where $\gamma_m = 0$ when all mobile ionic charge moved to the interface of poly and SiO_2; and $\gamma_m = 1$ [91] when all mobile ionic charge stay near or at the interface of Si/SiO_2. However, note that the term $Q_s(0)$ can be omitted under the assumption that the doping profiles are uniform (i.e. $Q_s(0) = 0$). Eq. A.29 now can be written as:

$$V_{fb} = W_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(0)}{C_{ox}} - \frac{Q_m \gamma_m}{C_{ox}} \qquad \text{(A.30)}$$

The reason why we pay more attention to the flatband voltage rather than threshold voltage is because of the following relationship between flatband and threshold voltages. According to many textbooks [91-93], the threshold voltage was calculated at the condition that the inversion occurs or $\psi_s = 2\phi_B$, thus

$$V_T = W_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(2\phi_B)}{C_{ox}} - \frac{Q_m \Upsilon_m}{C_{ox}} + 2\phi_B \pm \frac{\sqrt{2q\varepsilon_s N_B |2\phi_B|}}{C_{ox}} \qquad \text{(A.31)}$$

where in Eq. A.31, (+) for n-channel device, (-) for p-channel device, and N_B is either donor or acceptor doping concentration as appropriate.

If Q_{it} changes little in going from $\psi_s = 0$ to $\psi_s = 2\phi_B$, a reasonably good approximation in well-made devices, then by using the value of V_{fb} in Eq. A.28, Eq. A.31 can be written as:

$$V_T = V_{fb} + 2\phi_B \pm \frac{\sqrt{2q\varepsilon_s N_B |2\phi_B|}}{C_{ox}} \qquad \text{(A.32)}$$

Then for a doping concentration and an oxide thickness, threshold voltage is approximately equal to the addition of flatband voltage and a constant. Consequently, the charge defects cause any change in flatband voltage, will cause the same change in threshold voltage. In other words, we can study the reliability of gate oxide by mainly concentrate to study the shift of flatband voltage instead of threshold voltage.

A.4 Charge Components in Calculated Q_f

The following deduction will show the value of "calculated Q_f", Q_{fcal}

By definition we have

$$V_{fb} = W_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(0)}{C_{ox}} - \frac{Q_s(0)}{C_{ox}} - \frac{Q_m}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{A.33}$$

where $Q_{it}(0)$ and $Q_s(0)$ is the interface trapped charge and the surface charge at zero-band bending condition, respectively. To extract the "*calculated* Q_f", the programmer usually assumes that the test structure is ideal, i.e. there is no Q_{it}, Q_s, Q_m, and Q_{ox}. Consequently,

$$Q_{fcal} = Q_f + Q_{it}(0) + Q_s(0) + Q_m + Q_{ox} \tag{A.34}$$

For current technologies, Q_m can be omitted. To simplify the problem, let the doping profile is uniform then $Q_s(0) = 0$, then the Eq. 34 can be rewritten as:

$$Q_{fcal} = Q_f + Q_{it}(0) + Q_{ox} \tag{A.35}$$

A.5 Interface Trap Density Extracted From HF-CV And LF-CV curves

The program used in our laboratory to calculate the trap density is followed by combined High-Low frequency capacitance method. The low frequency capacitance of the MOS capacitor is defined by:

$$C_{LF} = \frac{dQ_T}{dV_G} \tag{A.36}$$

Thus by manipulating the above equation, Nicollian [94] show:

$$C_{LF} = (C_s + C_{it})\frac{C_{ox}}{C_{ox} + C_s + C_{it}} \tag{A.37}$$

Based on the above equation, we have the equivalent circuit of the MOS capacitor, which shown in Fig. A.3(a). However, at high frequency, since the frequency is too high the interface traps to respond, then $C_{it} = 0$. As a result, we have the equivalent circuit of the MOS capacitor at high frequency as one shown in Fig. A.3(b).

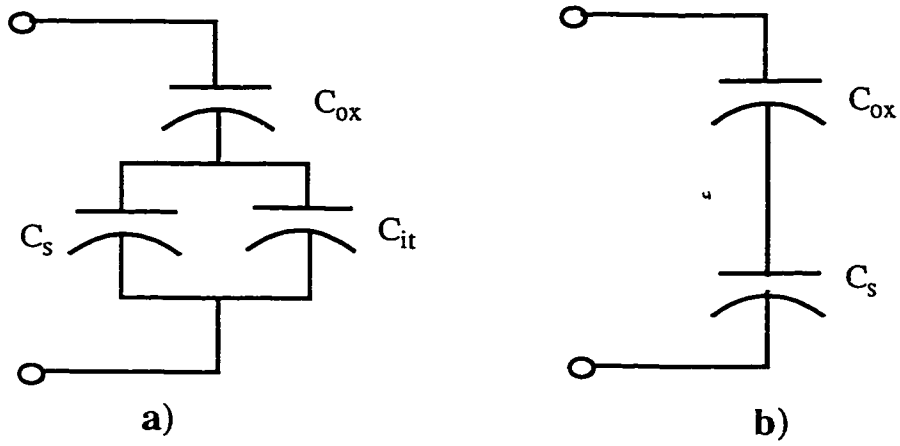


Fig. A.3 - Equivalent circuit of the MOS capacitor a) Low frequency; b) High frequency [94]

It is obvious that the difference between C_{LF} and C_{HF} contains the information of interface trap. From this idea, Wagner and Berglund [46] derived the following expression for D_{it}

$$D_{it} = \frac{C_{ox}}{q}\left[\left(\frac{1}{\Delta C/C_{ox} + C_{HF}/C_{ox}} - 1\right)^{-1} - \left(\frac{1}{C_{HF}/C_{ox}} - 1\right)^{-1}\right]$$

$$\text{or} \qquad D_{it} = \frac{\Delta C}{q}\left(1 - \frac{C_{LF}}{C_{ox}}\right)^{-1}\left(1 - \frac{C_{HF}}{C_{ox}}\right)^{-1} \tag{A.38}$$

Where $\Delta C = C_{LF} - C_{HF}$

By the use of Eq. A.38, we can extract the trap level density of interface trap at any gate bias voltage. Fig. A.4 shows how this method can be done graphically, and what parameters are needed to be monitored to get the interface trap level density.

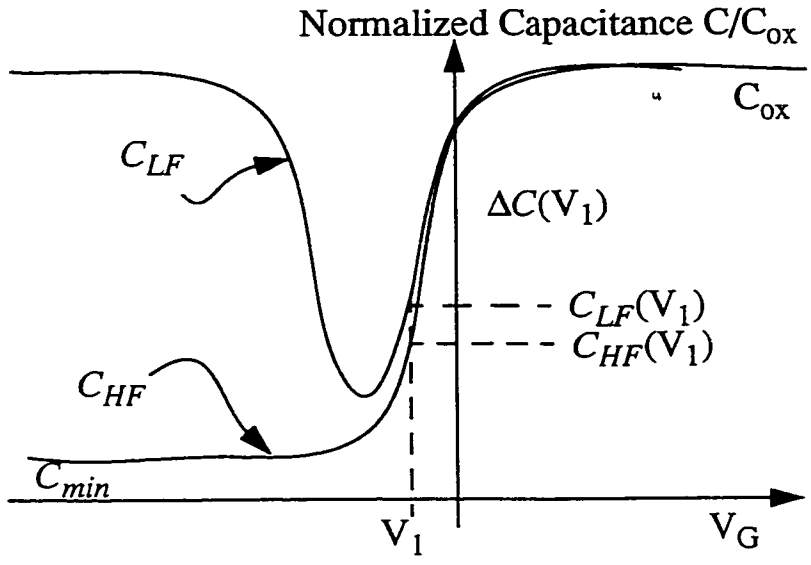


Fig. A.4 - High frequency capacitance and low frequency capacitance as functions of gate bias for a n-type MOS capacitor illustrating the parameters needed to graphically extracted interface trap level density using high-low frequency method.

APPENDIX B

MITEL 1.5 μm PROCESS OVERVIEW

In this chapter, the processing steps of the Mitel 1.5 μm process are presented within the bounds of Non-Disclosure Agreement between Mitel Corp. and Concordia uNiversity.

In following Sections, the typical Mitel process, CS150A, is used as reference to display about the changes in fabrication process. These changes are inevitable when a novel technique is employed, for examples fluorination into gate oxides.,

B.1 The Overall Properties of Mitel CS150A 1.5 μm Process

Overall, the Mitel 1.5μm process has the following properties:

◆ CMOS process with enhancement mode transistors for mixed signal applications.

◆ P-well based process.

◆ Single-Poly Single-Metal process.

◆ 11 masks as shown in table 1.

In this process, depending on the requirement of customers, the poly-2 and metal-2 are options which can be added into the process. In that case the name of process is changed. However, CS150A process is a 1.5μm single poly single metal. Because wafers

for this project were fabricated principally by the CS150A process, thus there are no poly-2 and metal-2 masks involved in the test-structures.

B.2 Wafers Used For CS150A Process

Since the process is p-well based, the starting silicon crystal must be n-type. Typical wafers for this process are 4", Czochralski <100>, 2-4 Ω-cm having a thickness of 525μm.

	Purpose
1)	P-well definition
2)	Active area definition
3)	Field boost implant
4)	Threshold voltage implant
5)	Poly 1 definition (gate and interconnect)
6)	N^- regions
7)	N^+ S/D regions
8)	P+ S/D regions
9)	Contact etch
10)	Metal 1 definition
11)	Bond pad etch

Table. B.1 - Masks & Masks' Purpose

B.3 Process CS150A Flow

The series of Figs. B is drawn to illustrate how n- and p- type MOS capacitors are built by the process CS150A. The Fowler-Nordheim hot carrier injection stresses were done on MOS capacitors. The left text column shows only technical steps done in the flow of process. These are written in a generic form.

❒ The process starts with N-type bulk wafers

❒ Initial Oxidation Procedure:

- Deposit wet oxidation layer and nucleation.
- Etch wet oxidation layer.
- Initial oxidation growth.

❒ P-well Procedure:

- Coat positive photoresist.
- Numbering.
- Align P-well definition mask.
- Develop positive photoresist.
- Verification by mark-laser.
- Etching of P^--well.
- Implantation of P^--well.
- Remove photoresist.

❒ Active Area definition Procedure:

- Etch oxide away
- Grow oxide under nitride.
- Nitride deposition.
- Coat positive photoresist.
- Align active area definition mask.
- Coat positive photoresist.
- Align active area definition mask.
- Development of photoresist.
- Etching of nitride.
- Remove photoresist.
- Clean.

❒ Field boost implant Procedure:

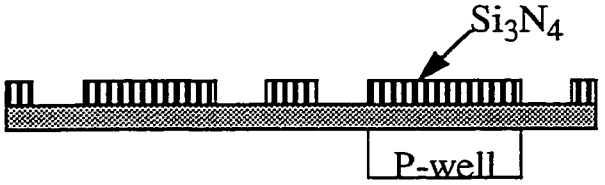
- Spin positive photoresist.
- Align field boost implant mask.
- Development of photoresist.
- Field Implantation P^-.
- Remove photoresist.
- Clean.

N-bulk

Fig B.1. - After Initial Oxidation Procedure done.

N-bulk

Fig. B.2. - After P-well procedure done.



N-bulk

Fig. B.3 After Active Area definition done.

- Field Implantation N^-.

❒ Field Oxide & Gate Oxide Procedure:
- Grow field oxide.
- Etch oxide.
- Remove nitride.
- Pre-Gate oxide growth.
- Etch oxide.
- Gate Oxide Growth.

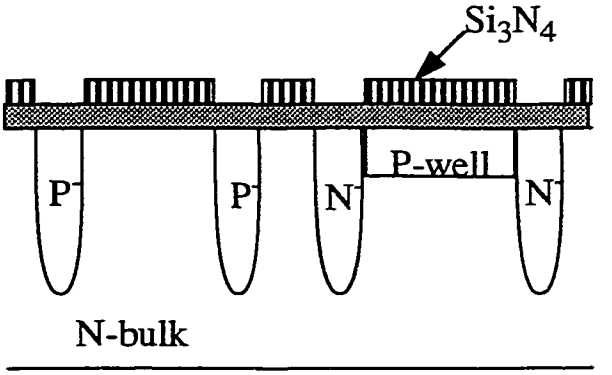


Fig. B.4 - After Field boost implant done.

❒ Threshold Voltage (V_T) Adjustment Procedure:
- V_{Tn} adjustment implantation.
- Coat positive photoresist.
- Align threshold voltage adjustment mask.
- Development of photoresist.
- Anti-burn out implantation.
- VT_p adjustment implantation
- Remove photoresist.

❒ Poly1 Deposition procedure:
- Deposit poly1.
- Spin negative photoresist.
- Remove unwanted poly1.
- Remove photoresist.

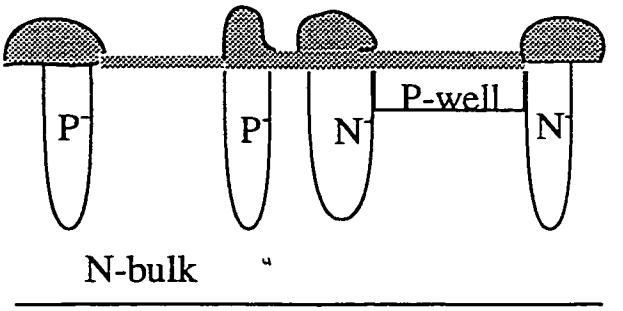


Fig. B.5 - After Gate Oxide grown

❒ Poly1 definition Procedure:
- Spin positive photoresist.
- Align poly1 definition mask.
- Development of photoresist.
- Inspection of the development.
- Poly Etch.
- Remove photoresist.
- Final inspection.
- Clean.

❒ Light doped drain (LDD) procedure:
- Spin positive photoresist.

- Align N^- region mask.
- Development of photoresist.
- Hard bake.
- Implant LDD N^- phosphorous.
- Remove photoresist.
- Clean.
- Etch oxide.
- Oxidation of implantation.

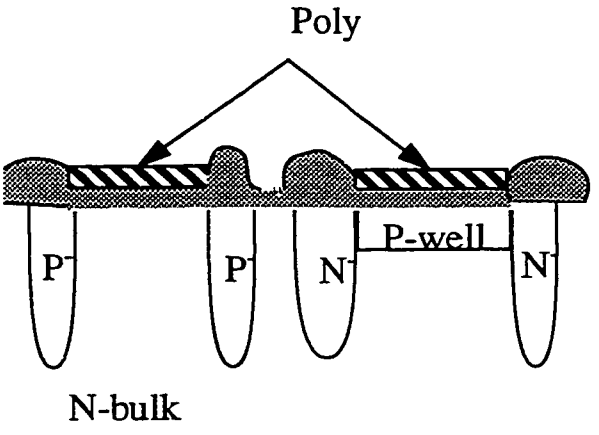


Fig. B.6 - After Poly1 etched.

❒ N^+ Source/Drain Region Procedure:
- Spin positive photoresist.
- Align N^+ Source/Drain Region mask.
- Development of photoresist.
- Hard bake.
- Implantation N^+ arsenic.
- Remove photoresist.
- Clean.

❒ P^+ Source/Drain Region Procedure:
- Spin positive photoresist.
- Align $^+$ Source/Drain Region.
- Development of photoresist.
- Implantation BF_2.
- Remove photoresist.
- Clean.

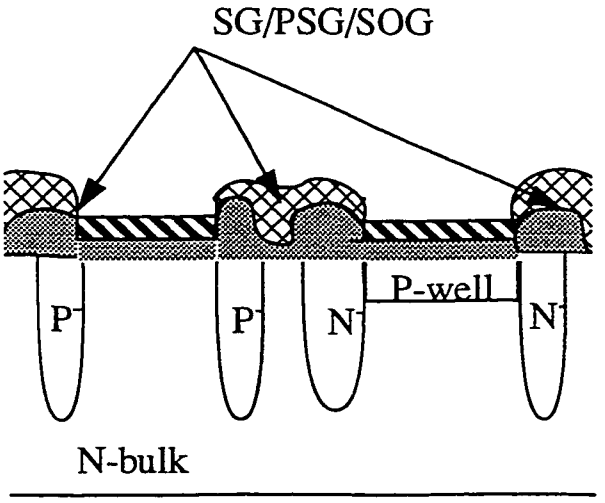


Fig. B.7 - After Contact etched

❒ Contact Etch Procedure:
- Coat SG/PSG/SOG.
- Spin negative photoresist.
- Remove flapping oxide.
- Remove photoresist.
- Clean.
- Spin positive photoresist.
- Align Contact definition mask.
- Development of photoresist.
- Plasma remove contact (SG/PSG/SOG).
- Remove photoresist.
- Clean.

❒ Metal1 Definition Procedure:
- Deposit Metal1.
- Spin positive photoresist.
- Align metal1 definition mask.
- Development of photoresist.
- Wet passivation.
- Remove photoresist.
- Plasma remove metal1.
- Rinse to remove residue.

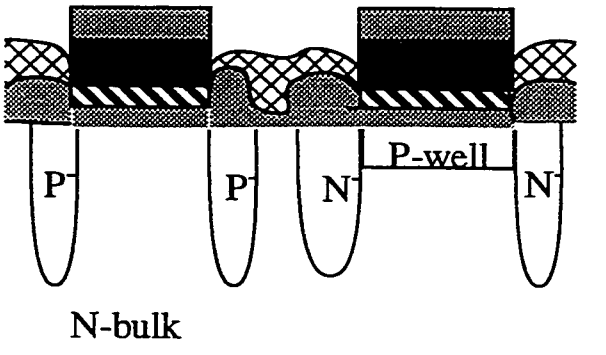


Fig. B.8 - After Metal1 definition

❒ Alloying Procedure:
- Dry alloy before the passivation
- Passivation growth.

❒ Bond Pad Etch Procedure:
- Spin positive photoresist.
- Align Bond Pad mask.
- Development of photoresist.
- Plasma etching
- Clean.

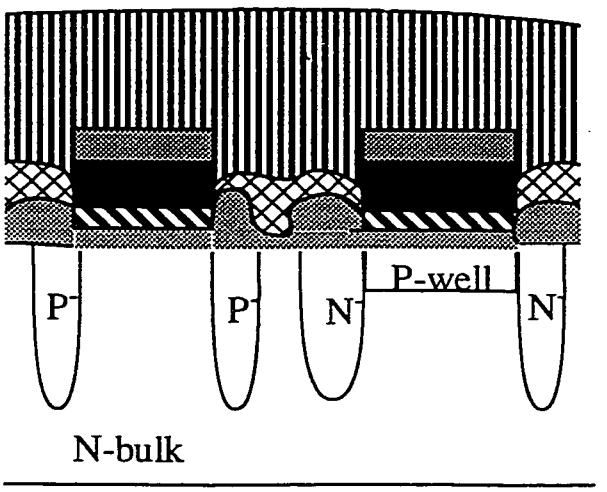


Fig. B.9 - Final Passivation Si_3N_4.

- Waiting for electrical characterization.

From the illustrations and summarized texts for process CS150A, Table B.2 can be set up. In this table, only the basic steps are mentioned. Also from this table, it is very convenient for reader to follow the splits of experimental samples. For example, ideas of before and after poly etch, are easily traced. For before-poly-etch samples, the fluorine

implantation is executed abruptly after the step 14, and before step 15 in Table B.2. For after-poly-etch samples, the fluorine implantation is done after step 15 and before step 16 in Table B.2. To do fluorinated samples there is no extra mask or modification in set of masks required. The oxynitridation request the change of gate oxidation in step 11 in Table B.2. And again there is no requirement for extra mask or mask modification for this technique.

Step	Description	Condition
1	Starting material N-type Bulk	2-4 Ω-cm
2	Initial Oxidation (and nucleation)	
3	P-well mask & implant	
4	P-well diffusion	
5	Sub Nitride Oxide	
6	Nitride deposition	
7	Active area mask & etch	
8	P^- field mask and implant	
9	N^- field implant and blanket	
10	Field oxidation	9000 Å
11	Gate oxidation	265 Å
12	V_{tn} Blanket implant	
13	V_{tp} adjust & punchthrough mask & implant	
14	Polysilicon gate deposition	3225 Å
15	Poly gate mask & etch	
16	LDD N^- mask & implant	
17	Implant oxide	
18	N^+ mask & implant	
19	P^+ mask & implant	
20	Dielectric deposition SG/PSG/SOG	1300/5000/1800 Å
21	Contact mask & etch	
22	Metallization 1	
23	Metal1 mask & etch	
24	Alloy	
25	Passivation: Oxide/Nitride	5000/5000 Å
26	Pads mask & etch	

Table. B.2 - Process CS150A flow over view.

APPENDIX C

EXPERIMENTAL SET UP FOR ELECTRICAL CHARACTERIZATION

Two different techniques are applied to characterize test structures: Fowler-Nordheim tunneling injection stress (on MOS capacitors) and channel hot carrier injection stress (on MOS transistors). With technical advice from engineers at the Semiconductor Division of Mitel Corp., the instruments were connected for electrical characterization at the Microelectronics Laboratory, Concordia University. Later, as the study developed, some modifications were done, but the original scheme was generally maintained.

In the first sections of this appendix, some parameters of the employed instruments will be shown. Then, relying on characteristics of instruments, discussions on modifications will be presented.

It should be noted that, before this work, there had been no such set up or electrical characterization experiments at Concordia University. A significant amount of time was devoted to build these set-ups.

C.1 Instruments Employed For Electrical Characterizations

C.1.1. Shielded Box

The shielded box is a black-painted box whose inside walls are covered by a thick copper sheet. Thus with the copper sheets, when the box is closed, there is no interference

caused by outside electromagnetic waves. A stage (called chuck) is centered inside the box. This stage can be heated up to 399°C [95]. The rise and fall of temperature of the stage is controlled by an IEEE 488 card [95]. However, all electrical characterization presented in this report was done at room temperature. The heating option was not used.

There are 4 co-axial connectors which allow up to 4 probe connections from inside to outside of the shielded box. To simplify the schematic, the shielded box can be drawn as in Fig. C.1

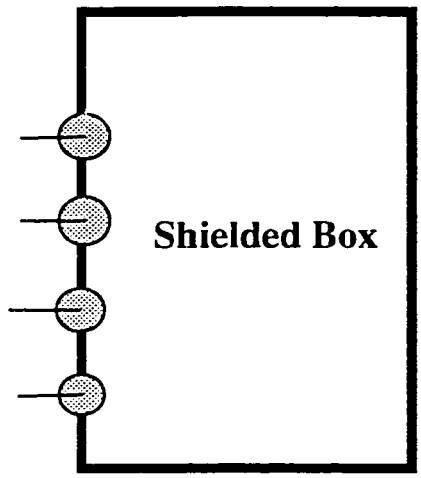


Fig. C.1 - - Diagram for the shielded box.

C.1.2. HP 4284A: Precision LCR Meter.

This is a HP-IB (Hewlett-Packard Interface Bus system) measurement instrument, which can provide voltage sources whose frequency range is from 20Hz to 1MHz [96]. In electrical characterizations done, HP 4284A was used as an 1 MHz voltage supply. In

addition, the program, which is used to execute the HF C-V measurement, switches the measurement mode to Cs-Rs (series capacitance, series resistance) [97].

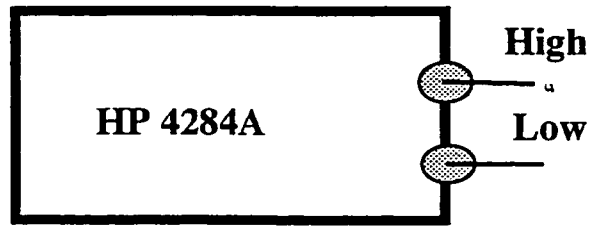


Fig. C.2 - Diagram for High Frequency, HP 4284A, LCR meter.

The input/output of the device consists of four terminals which are: high current, high potential, low current and low potential [98]. In tests, the high current and high potential terminals are connected together, while the low current and the low voltage are connected together. This method is called the two-terminal method [98]. These connectors are BNC coaxial cable. HP 4284A, in Fig. C.2, is drawn with two terminals named *high* and *low*.

C.1.3. HP 4140B: pA Meter/DC Voltage Source.

The HP 4140B is a very popular instrument. This instrument can measure very accurately in the sub-pA domain. The manufacturer, Hewlett-Packard, claims that the measurement range is $\pm 1 \times 10^{-15}$ A to $\pm 1.999 \times 10^{-2}$ A [99]. However, the range of pA is enough to satisfy the requirements/specifications of these tests.

The HP 4140B provides 2 voltage sources V_A: up to ±100V, a function generator/ programmable source, and V_B: up to ±100V, a programmable DC voltage source [100]. These two voltage sources (outputs) can be connected by coaxial connectors. But the input terminal, used to monitor the current, is a tri-ax connector.

In C-V measurements, the HP 4140B is used to obtain the quasi-static curves. The diagram of the HP 4140B can be shown as in Fig. C.3.

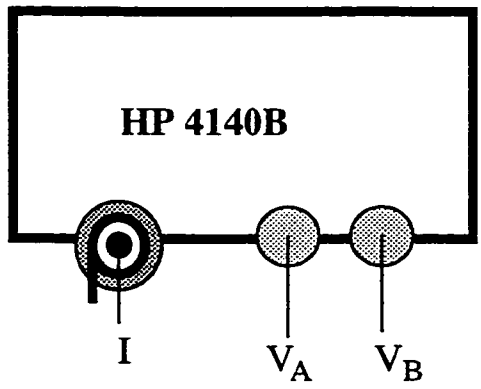


Fig. C.3 - Diagram of pA Meter/DC Voltage source HP 4140B.

C.1.4. HP 4145A: Semiconductor Parameter Analyzer.

The HP 4145A is an HP-IB operating instrument, which can provide researchers flexibility in monitoring signals through stimulus-measurement units (SMUs). HP 4145A supports the measurements by 4 SMUs and provides two voltage sources called VS1 and VS2. The diagram for this measurement unit can be displayed as the one in Fig. C.4. Notice that *in the HP4145A used in this study, SMU1 is non-functional.*

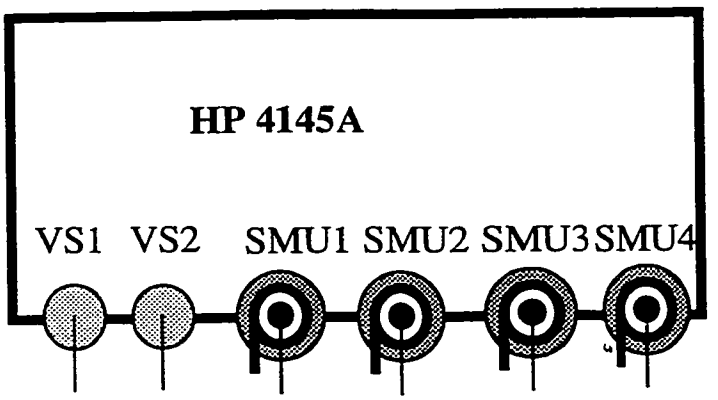


Fig. C.4 - Diagram of HP4145A

While the SMU is designed to gain advantages in low-current measurements, by itself, the guard-terminal can be used to reduced the effect of leakage currents (see Fig. C.5). An SMU has the voltage at the guard terminal held at the same potential as the SMU output voltage [101]. But, the same potential between the guard and SMU output terminal causes some inconveniences when connecting a SMU to coaxial BNC cables or connectors.

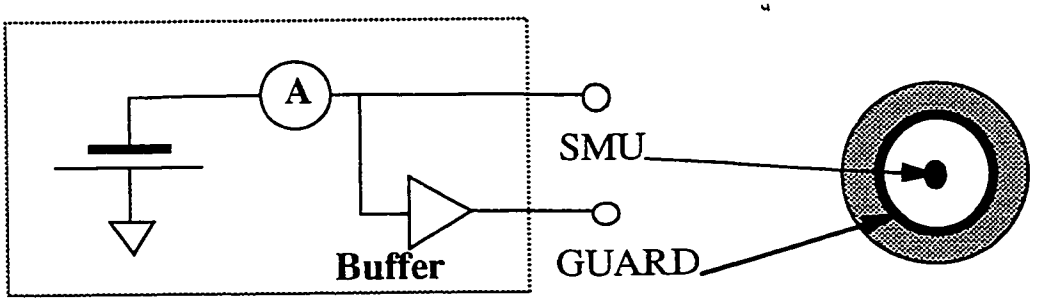


Fig. C.5 - Schematic of a SMU.

Without a (proper) triax-coax BNC adaptor, the guard voltage terminal in Fig. C.5 can be connected to the ground terminal (of any measurement instrument or the shielded box).To purchase these specific adaptors, the user must check with some small companies,

dealers and order the merchandise. This can take several months for ordering, fabrication and shipping, plus high prices. For example, an AD-BJ20-E1-PL75 would cost $45 US, or an AD-BJ20-E2-PL75 would cost to $75 US each [102]. Thus to get rid of this problem, an interface-box was built, based on the advice of Mr. M. Faucher, an engineer at Mitel Corp. The mentioned interfacial box can give the same results as triax-coax BNC adaptors, requires less budget, takes shorter time to posses and also gives the user more flexibility in switch-connections between different measurements on a same device under test.

C.1.5. Interfacial Box

This box was built by the author, when working as research assistant in the Microelectronics Laboratory, Concordia University. This utility allows the user to connect SMUs (triax BNC) to an ordinary (twinax BNC) coaxial cable without having the same potential between two terminals of a connected twinax coaxial cable. Moreover, since SMU1 is dead (as previously mentioned), a T connection was welded inside the interface box, as shown in Fig. C6, to supply voltage to a 4-terminal device, as MOSFET, in tests such as threshold voltage measurement. Fig. C6 also shows a schematic of how triax jacks were welded to coax jacks. Fig. C6 is used as a diagram for the interface box.

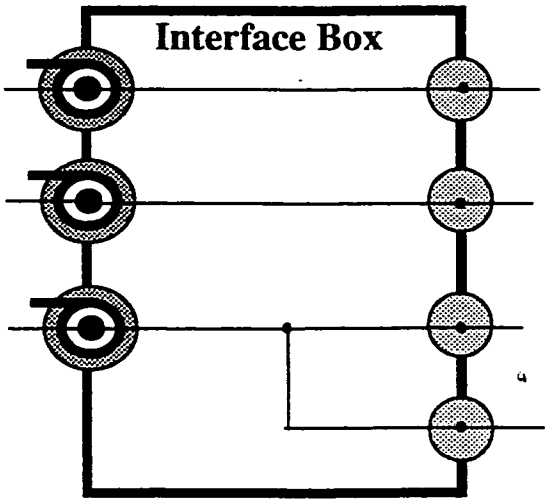


Fig. C.6 - Schematic of the interface box.

C.1.6. HP Series 300 Computer

A HP-IB computer operating was connected to HP-IB system. Via the computer, C-V measurements are automatically controlled by computer program. This package can also allow the user to measure I-V curves, C-V curves, time-dependent dielectric breakdown (TDDB), of any dielectric.

Under C-V characterization, the test structure is MOS capacitor. The program can give important outputs such as threshold Voltage, V_{th}, flatband Voltage, V_{fb}, summation of defect charge through out the dielectric. The combination of High and Quasi-Static C-V curves also provide the plot of interface trapped charge (D_{it}) versus bandgap energy of Silicon.

C.2 Set Up of Fowler-Nordheim Tunnelling Injection Stress.

C.2.1. Gate Leakage Current Detection

An eligible MOS capacitor for the test must have a low gate leakage current at low electric field. When a 5V bias applied on the gate, the device is considered defected for a gate current exceeding 1 pA. It is an obligation that, the defected devices must be rejected from the rest of the FN stress.

This test is always performed at the beginning of any electrical characterization to avoid errors come from defective devices. Through out hundreds of investigated devices, there were 2 or 3 devices suspected. Since the detected gate leakage current is very low, only the HP4140B can be used. The connection is very simple as shown in Fig. C.7.

To observe the leakage current, the set-up is done as:

- V_A is set manually to -5V constant.
- The measurement mode is set to *I-V.*
- And V_B *is used only for the guard ring* (P-type MOS capacitor).

Once the measured current is less than ±1 pA, the device under test is to be subjected to Fowler-Nordheim tunneling injection stress characterization.

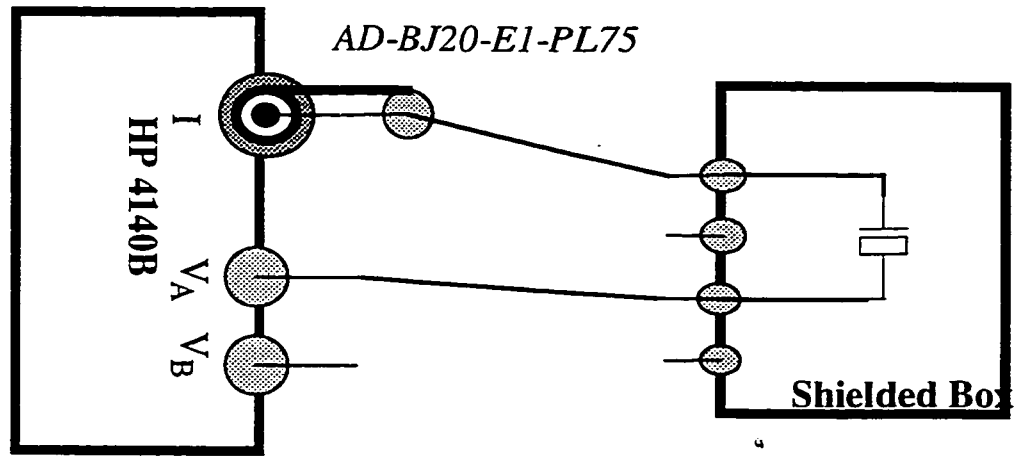


Fig. C.7 - Schematic for detection gate-leakage current of a MOS capacitor.

C.2.2. Fowler-Nordheim Hot Carrier Injection Stress Set-Up.

For Fowler-Nordheim stress the test structure is MOS capacitor. In common this type of electrical characterization is carried out by following procedure:

i) High & Low C-V measurement: to get the initial parameters of the structure such as V_{th}, V_{fb}, D_{it} at the midgap.

ii) Apply Fowler-Nordheim stress at a certain period of time.

iii) High & Low C-V measurement: At this point, the after-stress parameters are recorded/monitored.

Notice that the gap between step ii) and iii) is also important, since after the stress, material tends to release stress. The differences between before-stress and after-stress parameters, then, contain the information of the quality of the investigated gate-dielectric layers.

Fowler-Nordheim stress is applied following three main steps: First, high frequency C-V measurement; secondly, Quasi-static C-V curve; and thirdly the Fowler-Nordheim injection stress. Fig. C.8 shows a schematic for connections via which the three measurements and stress are apllied.

In Fig. C.8, the high of HP 4284A is connected to the gate of the MOS capacitor. Range of swept-voltage and range of frequency can be adjusted by the HP-IB computer. The MOS capacitor is connected to HP4140B via: the gate is connected to I-terminal, and the substrate is connected to V_A. The value of V_A is programmed by the computer. Note that, V_B is only employed when the MOS capacitor consists of guard ring (generally, for p-type MOS capacitor). All data obtained from measurements are feed through HP-IB bus/cable to a computer to compute required parameters.

At Microlectronics Laboratory, except the dead channel SMU1, the user can use any SMU. In Fig. C.8, SMU3 is connected to the substrate, while SMU2 to the gate of the device. Manually, SMU3 is set to a zero-constant voltage or a common ground, whereas SMU2 can be assigned either a constant current or a non-zero constant voltage. Thus, HP4145A can monitor current/voltage values at SMU2, SMU3 versus time (stressing time). These monitored data can be saved into 51/2 inch floppy disks or printed/plotted out.

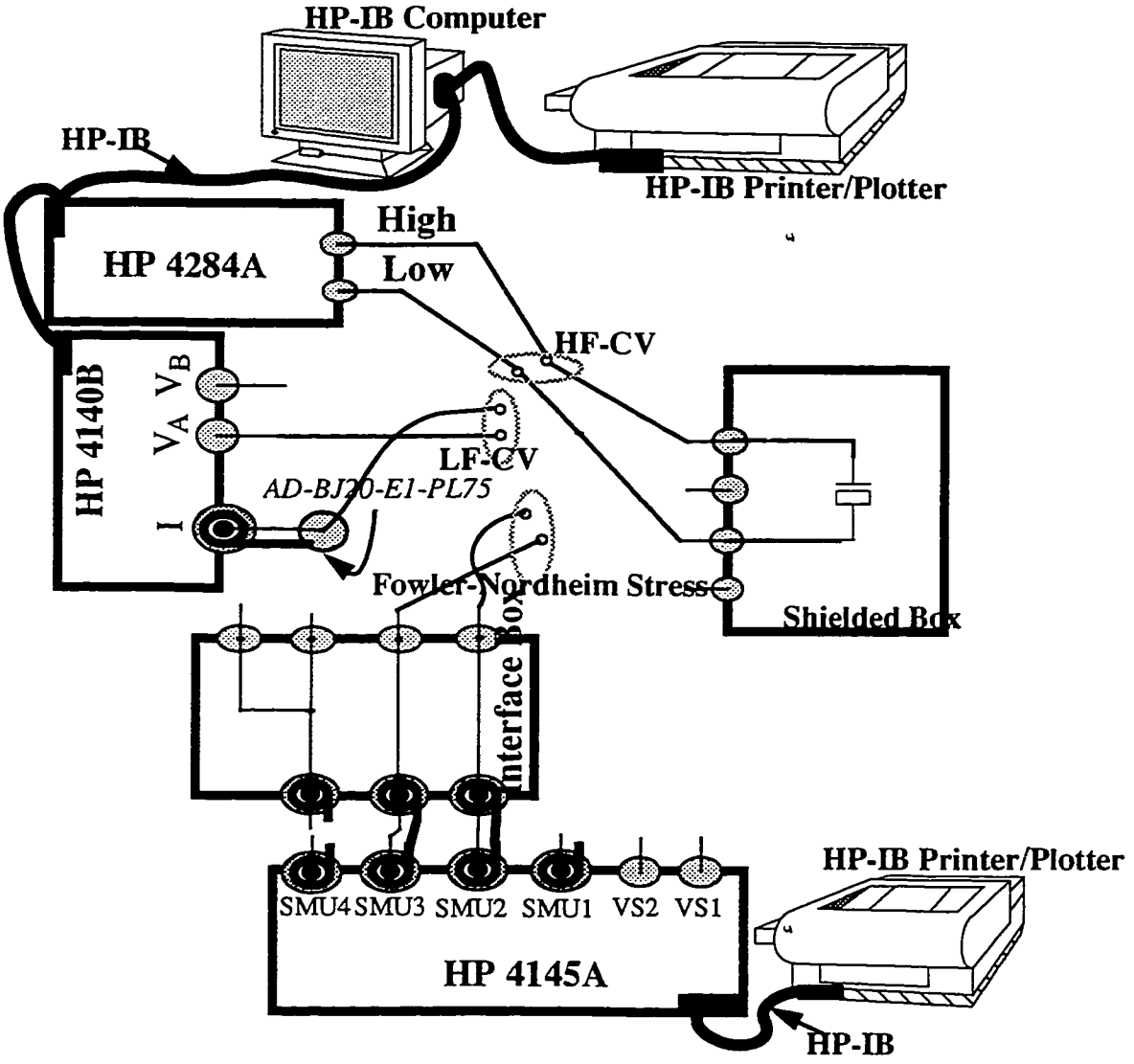


Fig. C.8 - Schematic for Fowler-Nordheim Stress set up.

C.3 Channel Hot Electron Injection (CHE) Stress Set-up.

This type of test uses a MOSFET structure (four-terminal structure) to monitor the damage in the device during hot electrons bombarding the channel of the MOSFET. The most damaged zone is the space charge region at/near the drain, because at this area the electric field is the highest. The damage can appear in the change of either threshold voltage or transconductance gain of the device.

Before apply CHE stress, there are some prepared steps must be done. such as:

♦ Verify gate leakage current, I_G. If I_G >1pA, the device is bad and must be rejected from the characterization.

♦ Verify where the snapback phenomenon taking place. Recorded V_{DS} value at which snapback beginning. From theory section snapback phenomenon is expected to give us overestimation of device-lifetime, therefore, this value of V_{DS} presenting the limitation of Drain voltage that could be applied on MOSFETs.

♦ Maximum substrate current at V_{DS} = 5.5V and Maximum substrate current, $I_{sub\text{-}max}$, at V_{DS} which will be applied for CHE stress.

After these measurements, the common procedure to apply Channel hot electron injection stress is carried out by following steps:

i) Measure the initial threshold voltage, V_{th0}, or the initial transconductance of MOSFET, g_{m0}.

ii) Apply CHE stress under a period of time Δt (seconds).

iii) Intervally, stop CHE stress, and then measure the threshold voltage, V_{th}, or the transconductance of MOSFET, g_m. Calculate the difference between initial V_{th0}/g_{m0} and just-measured V_{th}/g_m.

iv) A device lifetime is reached when ΔV_{th} = 50mV, or $\Delta g_m/g_{m0}$ = 10%.

Now, *one data point of I_{submax}/W versus lifetime is gained.*

C.3.1. Gate Leakage Current Verification Set-Up

When connected as shown in Fig. C.9, V_A is set to a constant voltage of -5V, while the current (I) terminal is used to measure the gate leakage current. The measurement mode is manually set to I-V mode. This set up is similar to the gate-leakage current measurement for an MOS capacitor, except that here the device under test is a four terminal one. If I_G is >±1pA, then the device is considered to be defective and is rejected from the test.

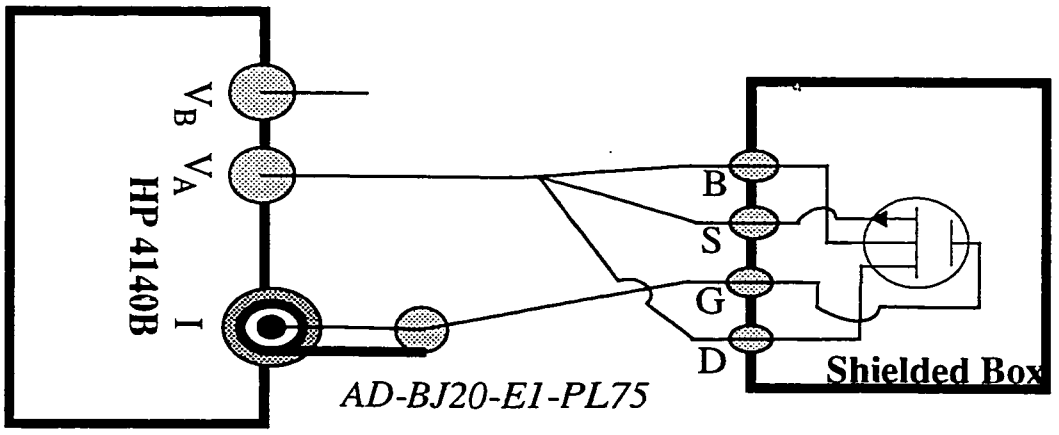


Fig. C.9 - Schematic of verification the gate leakage current.

C.3.2. Snapback Verification Set-Up.

Fig. C.10 is an experimental set-up to monitor the snapback verification, I_{submax}, V_{th}, and and to apply CHE stress. The values of V_G, V_D, V_B, and V_S are programmed by HP4145A. By a pre-defined auto sequence (ASQ), the data/plots are automatically recorded into 51/2 inch floppy disk.

For snapback measurement, 2 graphs are plotted (on the VCR of HP4145): first, I_D vs. V_{DS}, and secondly, g_m vs. V_{DS}. The set up for these measurements are:

:

	Name	Able Recorded	Source	Type	Range	compl.
SMU2	V_D	I_D	V	Var 1	0-8 V; Step 0.2 V	15 mA
SMU3	V_S	I_S	COM	Const	0 V	100mA
SMU4	V_B	I_B	COM	Const	0 V	100mA
VS1/VS2	V_G	-	V	Var 2	4-6V; Step 0.5 V	15 mA

Via either I_D vs. V_{DS} or g_m vs. V_{DS} plot, the snapback points can be deifined. V_{DS} in applying stres must be smaller than the snapback value. Practically, the high field near the snapback point can be used to reduce the stressing time.

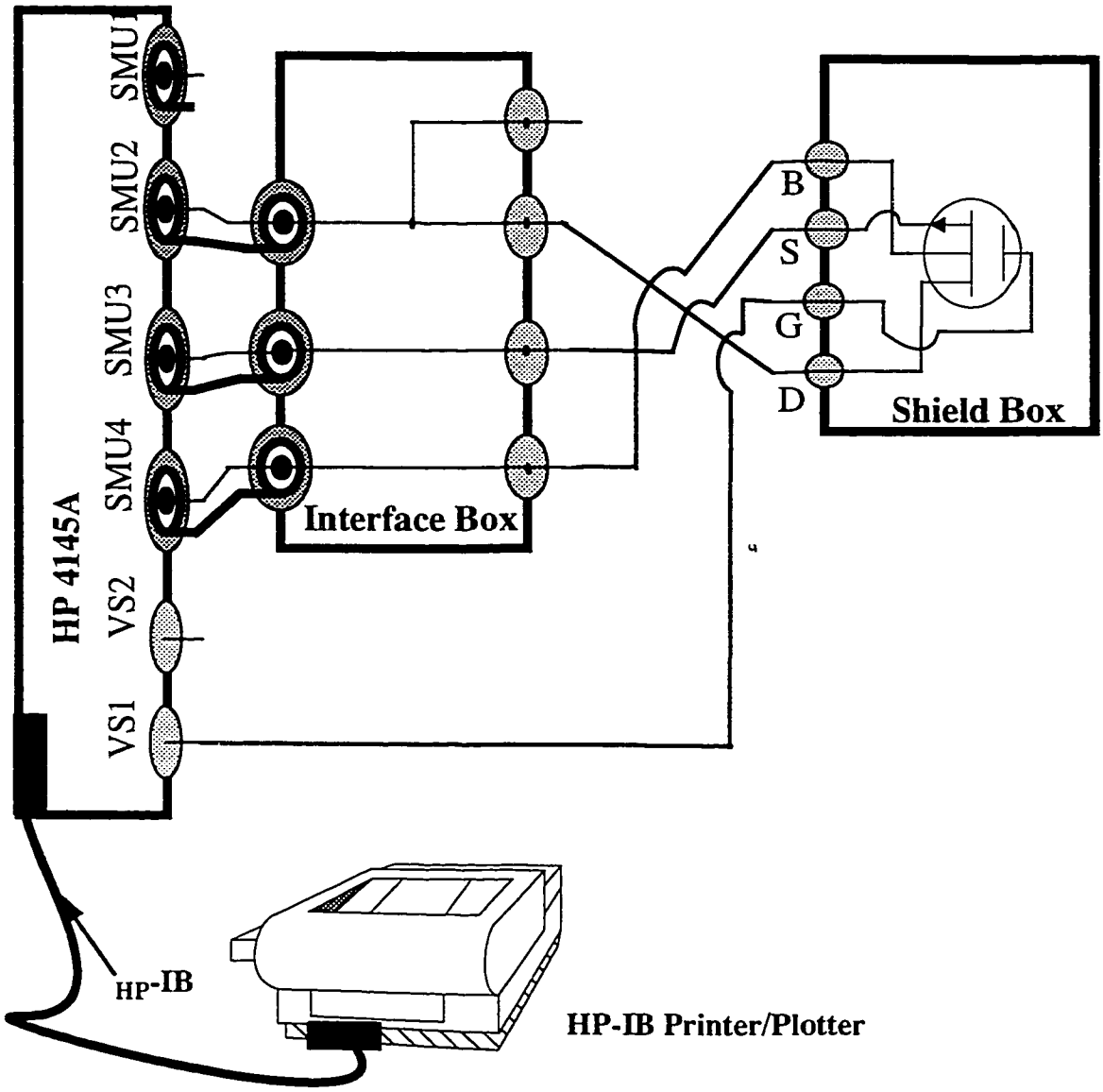


Fig. C.10 - Schematic for connection of Snapback verification, I_{submax} measurement, V_{th} measurement, and CHE stress application.

To measure transconductance, there are two schemes to do it:

1) Slope of I_D vs. V_G in linear region, not in saturation region, can be used as the transconductance of the device under test. For the Mitel 1.5μm process, V_G is set from 2.2 to 5 V, while V_D is fixed at 1 V. The slope of I-V curve is considered as g_m.

2) From "function definition" of HP4145A, a variable $\Delta g_m = \Delta I_D/\Delta V_G$ is defined. The data to be fed into this defined function are from the plot of $I_D$vs. V_{DS}. This scheme is applied to measure the transconductance at Microelectronics Laboratory. All of the set up of channel definition is stored in a file called SNAPBACK.

C.3.3. I_{submax} Measurements

At a fixed V_{DS}, there is one I_{submax} associated with a V_{GS}. Since there is a requirement to know I_{submax} measured at V_{DS} = 5.5 V, this value, therefore, must be measured. In addition to this required value, to obtain the plot of I_{submax}/W vs. lifetime, the values of I_{submax} at V_{DS} at which the CHE stress applied must be measured. To search for an appropriate I_{submax} in a stress, many associated-V_{GS}. for fixed V_{DS} should be measured before any CHE stress. In our experiment, the values of I_{submax}, and associated-V_{GS} at V_{DS} = 5.5, 7.5, 7.6, 7.7, 7.8, 7.9, and 8.0 V are measured.

While the connection is kept as shown in Fig. C.10, the set up for channel definition is changed as following:

	Name	Able Recorded	Source	Type	Range	compl.
SMU2	V_D	I_D	V	Var 2	5-8 V; Step 0.1 V	100mA
SMU3	V_S	I_S	COM	Const	0 V	100mA
SMU4	V_B	I_B	COM	Const	0 V	100mA
VS1/VS2	V_G	-	V	Var 1	0-4V; Step 0.1V	100mA

The values of I_{sub}, is denoted as I_B in the above table, is recorded, and from the plots of I_B versus V_{GS}, the required I_{submax} can be defined for a fixed V_{DS}. Then the

required values of I_{submax}, now, are stored for later calculation. All these set up are stored in a program called ISUB.

C.3.4. Threshold Voltage Measurement Set-Up.

To obtain V_{th}, the MOSFET must be configured in saturation mode, i.e. let $V_G = V_D$, while $V_B = V_S$. Thus again the connect is remained as Fig. C.10, but the channel definition, then, is:

:

	Name	Able Recorded	Source	Type	Range	compl.
SMU2	V_D	I_D	V	Var 1	0-2V; Step 0.01 V	100mA
SMU3	V_S	I_S	COM	Const	0 V	100mA
SMU4	V_B	I_B	COM	Const	0 V	100mA
VS1/VS2	V_G	-	V	Var '1	Follow Var 1	100mA

Then from the I-V curve of I_D vs. V_{DS}/V_{GS}, the values of threshold voltage is established as shown in theoretical section. To get the threshold voltage, the data points in the linear section of I_D vs. V_{DS}/V_{GS} is recorded. Based on these data, the threshold voltage is calculated by least means square method. The set up for threshold voltage measurement is stored in one program called VTH.

C.3.5. CHE Stress Applied Connection.

At the beginning of this project, HP4140B was employed to supply voltage sources for CHE stress. That took time to re-connect properly terminals to the probes.

However, HP4145A, also can supply same voltage sources as HP4140B. This gives more flexibility to arrange connections. A channel definition as shown in this section has an advantage that, with the same connection as Fig. C.10, the CHE stress still can be applied on samples without re-arrange/re-connect the probes and the terminals.

From I_{submax}s measured as presented in Section C.3.3, an appropriate I_{submax} is chosen. Since the values of V_{DS}, V_{GS} are known, it is easily to set up a channel definition to have a right chosen I_{submax}. For example, say at V_{DS} = 7.8V,a sample has an I_{submax} = 455 μA with V_{GS} = 3.15 V. Hence, the channel definition set up can be:

:

	Name	Able Recorded	Source	Type	Range	compl.
SMU2	V_D	I_D	V	Const	7.8 V	100mA
SMU3	V_S	I_S	COM	Const	0 V	100mA
SMU4	V_B	I_B	COM	Const	0 V	100mA
VS1/VS2	V_G	-	V	Const	3.15 V	100mA

Depend on chosen I_{submax}, the program of CHE stress must be changed for each measurement. And that the only program must be changed for every CHE stress, while other programs do not need to be changed after some initial probing measurements. In order to run auto sequence set up (ASQ), the programs of CHE stress would be saved under a name, say CHE, thus there is no need to change a readily-prepared ASQ. Or the names of CHE stress program can be saved in different names, but ASQ must be changed respectively (that is not the choice to be used).

To run automatically, there are 2 ASQ were set. The first ASQ is for the initial value measurements. A typical program for this ASQ is:

```
1 GET P SNAPBACK
2 SINGLE
3 SAVE D SNAPBACK
4 GET P ISUB
5 SINGLE
6 SAVE D SINGLE
7 GET P VTH
8 SINGLE
9 SAVE D VTH
```

Steps 3, 6, 9 can be replaced by command PAUSE if the user can get the measurement immediately. That could help the user to save space in floppy disk which has a limited memory.

The second ASQ, is set for CHE stress. Since the maximum stressing time can be employed up to 5000 seconds per SINGLE command, and there is a limit of 24 lines for an ASQ, then if there is a quest for a long stressing time, this ASQ must be recalled to repeat the steps. Note that the stored data file must be recorded or copied to new disks before re-run this ASQ. A typical program for this ASQ is:

```
1 GET P CHE
2 SINGLE
3 SINGLE
4 GET P VTH
5 SINGLE
6 SAVE D VTH1
7 GET P CHE
8 SINGLE
9 SINGLE
10 GET P VTH
11 SINGLE
12 SAVE D VTH2
13 GET P CHE
14 SINGLE
15 SINGLE
16 GET P VTH
17 SINGLE
18 SAVE D VTH3
19 GET P CHE
```

20 SINGLE
21 SINGLE
22 GET P VTH
23 SINGLE
24 SAVE D VTH4

With an ASQ as this one, the stress can last in 40,000 seconds. Note that most of the CHE stresses require around 100,000 to 200,000 seconds. Then, this ASQ must be repeated two, three, or more times.