Wide Frequency Range Superheterodyne Receiver Design and Simulation

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Abstract

Wide Frequency Range
Superheterodyne Receiver Design and Simulation

Chen-Yu Hsieh

The receiver is the backbone of modern communication devices. The primary purpose of a reliable receiver is to recover the desired signal from a wide spectrum of transmitted sources. A general radio receiver usually consists of two parts, the radio frequency (RF) front-end and the demodulator. RF front-end receiver is roughly defined as the entire segment until the analog-to-digital converter (ADC) placed before digital demodulation. Theoretically, a radio receiver must be able to accommodate several tradeoffs such as spectral efficiency, low noise figure (NF), low power consumption, and high power gain. The superheterodyne receiver consisting of double downconversion can well balance the tradeoffs required for the receiver design.

In this thesis, the RF front-end superheterodyne receiver design and implementation is presented. Instead of fixed radio frequency of system-on-chip (SOC) design which has been a popular research topic, a radio receiver operating in the wide frequency range of roughly 2.53 GHz to 2.83 GHz located in *IEEE* S-band is considered. The wide frequency range receiver is suitable for applications like Direct-to-Home satellite television systems, which allocates from 2.5 GHz to 2.7 GHz. This thesis is focusing on the off-chip receiver design for the objectives of processing a wider

frequency band while providing high linearity and power gain. The important active devices in a receiver which are low noise amplifiers (LNA), power amplifiers (PA), and mixers are designed and implemented. In this work, the two-stage LNA designed provides low NF and good input standing wave ratio (VSWR). The class-A PA is designed utilizing the load-pull method for maximum power transfer and highest possible power added efficiency (PAE). The mixer design adopts the double balance fully differentially (Gilbert) topology which is ideal for low port feedthrough, intermodulation distortion, and moderate conversion gain.

The self-built active devices (e.g. amplifiers and mixers) and band-pass filters (BPF) provided by Agilent EEsof Advance System Design (ADS) are combined into a double downconversion RF front-end receiver. The receiver sensitivity and selectivity is assessed and tabulated. Also, the operation in the wide frequency range of roughly 2.53 GHz to 2.83 GHz with the last intermediate frequency (IF) of 20 MHz is verified.

Acknowledgement

I would like to thank my supervisor, Dr. Yousef R. Shayan for his guidance throughout the development of this thesis and suggestions on this implementation-oriented design. He has been a constant source of valuable ideas and inspiration. Last but not the least, I would like to take this opportunity to thank my parents for their constant support for me to pursue the graduate study at Concordia University.

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List of Acronyms

Acronym	Expansion
ADS	Advance Design System
ADC	Analog-to-Digital Converter
ACPR	Adjacent Channel Power Ratio
AGC	Automatic Gain Control
BJT	Bipolar Junction Transistor
BSIM	Berkeley Short-channel IGFET Model
BPF	Band Pass Filter
BSF	Band Select Filter
CMOS	Complementary metal–oxide–semiconductor
CNM	Conjugate Noise Match
CPW	Grounded Co-planar Transmission line
CSF	Channel Select Filter
DUT	Device Under Test
DAC	Digital-to-Analog Converter
DECT	Digital Enhanced Cordless Telecommunications
DSL	Digital Subscriber Lines
DSP	Digital Signal Processing

FDD	Frequency-Division Duplexer
FET	Field-Effect Transistor
GaAs	Gallium Arsenide
GPS	Global Positioning System
HD	Harmonic Distortion
IF	Intermediate Frequency
IMDR	Intermodulation Distortion Ratio
IIP3	Input Third Order Intercept Point
IMD	Intermodulation Distortion
IMT	International Mobile Telecommunications
IP1dB	Input Referred 1 dB Gain Compression Point
IMC	Input Matching Circuit
LSC	Load Stability Circle
LNA	Low Noise Amplifier
M	Mismatch Factor
MEMS	Microelectromechanical Systems
MTI	Moving Target Indication
NF	Noise Figure
OIP3	Output Third Order Intercept Point
OMC	Output Matching Circuit
OP1dB	Output Referred 1 dB Gain Compression Point

OFDM	Orthogonal Frequency Division Multiplexing
OMDS	Output Minimum Detectable Signal
PCSNIM	Power Constrained SNIM
P1dB	1 dB Gain Compression Point
QPSK	Quadrature Phase Shift Keying
RF	Radio-Frequency
SAW	Surface Acoustic Wave
SFDR	Spurious Free Dynamic Range
SiGe	Silicon Germanium
SNIM	Simultaneous Noise and Impedance Match
SNR	Signal-to-Noise Ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
SSB	Single Side Band
SSC	Source Stability Circle
VCO	Voltage Controller Oscillator
VGA	Variable Gain Amplifiers
WCDMA	Wideband Code Division Multiple Access

Chapter 1

Introduction

1.1 Background

The receiver, having the primary purpose of reliably recovering the desired signal from a wide spectrum of transmitted sources, is backbone of the modern communication devices. The radio designer must understand each of several devices in a complete communication system from the modulator in the transmitter to the output of the demodulator placed in the receiver. Modern portable communication devices should be small and low in power consumption. To achieve this, both digital and RF devices should be placed on the same semiconductor die to form a so-called "system on a-chip" (SOC) which requires a high degree of integration [1-3]. Since the field-effect transistor (FET) provides smaller area and lower power consumption than bipolar junction transistor (BJT) devices, therefore FETs are widely used in the design of digital systems associated with modem development. Moreover, the integration of digital and RF/analog design leads to the SOC design primarily based on complementary metal–oxide–semiconductor (CMOS) process technology [2,3, 5].

While CMOS provides higher integration into SOC and lower power consumption, several advantages can be provided by BJT. Aside from being able to

provide higher gain (i.e. higher transistor transconductance), higher output impedances, and transition frequency (f_T), the noise is perhaps one of the major advantages of Silicon-Germanium (SiGe) based heterojunction bipolar transistor (HBT) over CMOS. The flicker and thermal noise are both higher in CMOS than in SiGe based HBT. To reduce noise, large size and large current are often required. Nowadays, design of power amplifiers (PA) in a cell-phone front-end have been more based on either SiGe or Gallium-Arsenide (GaAs) BJT for higher power amplification than CMOS based process technology. Therefore, the radio receiver deigned in this thesis, has focused on designing active devices such as low noise amplifier (LNA) and power amplifier (PA) based on BJTs. The mixer, that usually utilizes several transistors, is designed based on CMOS process technology for lower power consumption and more linear behavior [4-6].

Radio RF front-end receiver is roughly defined as the entire segment until the analog-to-digital converter (ADC) placed before digital demodulation. A generic multi-band (e.g. GSM and WLAN) RF front-end receiver consisting of two RF chains is shown in Figure (1.1) . The antenna picks up the electromagnetic waves from the environment and amplifies the signal within its bandwidth. The first component following the receiver antenna is usually the micro-electro-mechanical systems (MEMS) duplexer. The duplexer and voltage controlled oscillator (VCO) can be software configured by the digital signal processing (DSP) chip to switch from band to band and channel to channel between the several receiver chains. The MEMS devices have also been a popular research topic lately with the trend of software reconfiguring single radio front-end for different bands and standards [7-9]. In addition, on-chip MEMS tunable bandpass filter (BPF) has been

known to provide on-chip integration with low loss and high quality factor (Q) on the order of 100- 1000 [10].

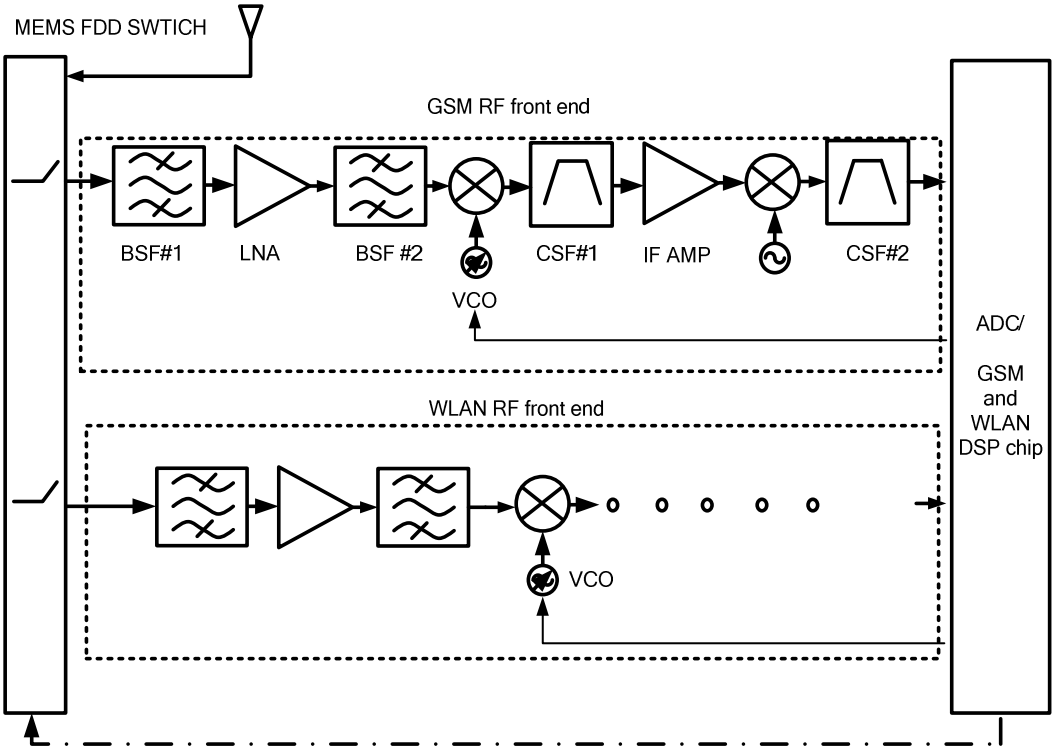


Figure 1.1 Multi-band radio architecture.

In this thesis, the design and implementation of the active devices have been focused on while considering the necessary passive band-select filters (BSF) and channel-select filters (CSF) in the path of frequency downconversion. The first BSF is often placed for preselecting the desired band of interest. However, the attenuation must be limited with the consideration of noise figure (NF), insertion loss, and group delay. The second BSF will serve the purpose of minimizing the mixer LO feedthrough, nonlinearities caused by the LNA, and further attenuating the image-band signals. The two CSF proceeding both mixers reflect the undesired IF such as LO harmonics and several intermodulation distortion (IMD) products back to the mixer. To mitigate this

problem, a double balanced active mixer has been proposed. The CSF can also be placed preceding the second mixer to reflect the undesired signal frequencies from entering. The IF amplifier (IF AMP) is designed with high reverse isolation to reduce the reflected frequency components.

Theoretically, a radio receiver must be able to accommodate several requirements such as spectral efficiency, low noise figure and low power. In this thesis, the receiver end design and implementation is presented. The general specifications of a modern RF front-end radio receiver must include the following:

- Selectivity
- Sensitivity
- Power gain
- Isolation

The most important aspect of designing a radio receiver would be the frequency planning. Carefully choosing the operating frequencies for the LNA, power amplifier (PA), and mixer in a double downconversion radio can balance the tradeoffs between receiver selectivity and sensitivity. A highly sensitive receiver can suppress the image band, which will also be downconverted to the same intermediate frequency (IF) after the mixing process. Having the image band relatively far from the desired band can ease off the shaping requirements (i.e. lower quality-factor) of the high operating frequency image-reject filter. However, having high IF can lead to lossy filters and unstable amplifiers. On the contrary, for high selectivity receivers, a low IF should be adopted. Having a relatively low IF can lead to optimum channel selection with minimum adjacent channel leakage and maximum intermodulation distortion (IMD) ratio.

1.2 Literature Survey and Motivation

Recently, there has been few published references [11-15] discussing the construction of the radio front-end receiver for different applications in short details. In [11], a dual-band RF front-end operating for both Wideband Code Division Multiple Access (WCDMA) and Global Positioning System (GPS) is implemented. This RF front-end includes two differential LNA, double-balanced mixers of two channels (i.e. in-phase and quadrature) and a voltage-controlled oscillator (VCO). The receiver utilizes two LNAs, mixers and multiphase VCO to reduce the hardware complexity. In [12], a dual-band RF front-end operating at 2.4 and 5.2 GHz is proposed. The dual-band RF front-end consists of a LNA and a switchable single balanced mixer between 2.4 and 5.2 GHz. In [13], a dual-band RF front-end employs the image reject mixer with two tuned RF stages and a common IF stage to allow operation with 1.8 GHz standards while using only two oscillators. In [14], the proposed RF front-end circuits consisting of a LNA using an on-chip transformer and a downconversion mixer using BJT have been implemented in 0.18 mm deep n-well CMOS process. In [15], the measurement results of LNA, PA and antenna switch for front-end 1.9 GHz Digital Enhanced Cordless Telecommunications (DECT) application based on SiGe HBT have been presented.

Based on the several references above, this thesis has been devoted on building all the widely implemented front-end active devices as seen in [11-15] such as LNAs, differential mixers, and power amplifiers. However, in this thesis, instead of fixed radio frequency of SOC designs, a radio receiver operating in the wide frequency range of roughly 2.53 GHz to 2.83 GHz located in *IEEE* S-band is considered. The wide frequency range receiver is suitable for applications like Direct-to-Home satellite

television systems, which allocates frequency range from 2.5 GHz to 2.7 GHz. Also, the Digital Subscriber Lines (DSL) adopts the similar Frequency Division Multiple Access (FDMA) scheme to divide the available frequency range into several frequency channels for downstream, upstream traffic, and access from multiple users.

In [16,17], the similar off-chip Moving Target Indication (MTI) radar receiver located in *IEEE* L-band operating from 1.22 to 1.35 GHz is designed, with an IF frequency of 30 MHz. The passive mixer implemented in radio receiver is designed for RF of 1.3 GHz and LO of 1.33 GHz. It consists of two Schottky diodes, directional coupler, and RF filter, while providing conversion loss of roughly 6 dB and port feedthrough of roughly 17 dB. In comparison to [16], this thesis is focusing on the receiver design with the objectives of processing wider frequency range while providing higher linearity, lower NF, lower power consumption and higher power gain. Above all, the mixers implemented in this thesis are able to provide better linearity and higher conversion gain. After completing this thesis, the author will gain the experience of designing wide frequency range RF front-end, which in future may be used in the development of SOC operating wide radio frequency range.

1.3 Thesis Objectives and Contributions

The objective of this thesis is design and implementation of essential active devices in the *IEEE* S-band double downconversion radio receiver such that it is able to downconvert different carrier frequencies in the desired frequency range of roughly 2.53

GHz to 2.83 GHz down to the fixed intermediate frequency of 20 MHz by tuning the VCO. The contributions of this thesis are as follows:

- A double-IF downconversion receiver in the frequency range of roughly 2.53 GHz to 2.83 GHz (located in *IEEE* S-band) is designed and simulated.
- The frequency plan of the receiver is given to balance the tradeoffs of the radio receiver sensitivity (e.g. NF) and selectivity (e.g. P1dB). Also, different receiver architectures have been compared and performance tradeoffs have been tabulated and discussed.
- A rarely seen methodology of designing a stable microwave LNA has been presented. The approach starts by first choosing the desired load reflection coefficient by plotting constant power gain circle and fixing an acceptable input mismatch factor (M). With the chosen M, the transducer gain can be obtained. With the desired load reflection coefficient, the input reflection coefficient can be calculated and the input VSWR can be plotted.
- The stable LNA integrated with image-band attenuation notch filter is able to provide low NF, moderate power gain, and good input VSWR.
- The class-A power amplifier (PA) using load-pull method is designed. The design procedures of the high power amplifier are somewhat different from that of small signal amplifier (e.g. LNA). The PA utilizes load-pull method to obtain the proper impedances at the input and output ports of the amplifier for maximum power transfer.

- The conventional conjugate matched and power matched amplifiers are cascaded for higher power gain and transfer.
- The double balanced fully differential (Gilbert) mixer is simulated based on SPICE3 0.5 μm CMOS process technology. It is able to provide low port feedthrough and eliminate even order intermodulation distortion (IMD) with moderate power gain and NF.
- All the active components built are cascaded for a series of signal assessments. The most important outcome of the radio receiver design is that it is able to downconvert the desired frequency range resulting the same last IF frequency (i.e. 20 MHz) with similar waveform amplitudes.
- Several important figure-of-merits indicating the receiver selectivity and sensitivity such as minimum detectable signal (MDS), spurious free dynamic region (SFDR), and third order intercept point (TOI) are tabulated.
- The receiver 1dB power compression point (P1dB), third order power intercept point (IP3), noise figure, and power gain are assessed.

1.4 Methodology of Design and Implementation

In this design, all of the active circuits are designed and simulated on Agilent EEsof Advance Design System (ADS). The software is the most adopted tool used for RF/ microwave circuits, m*onolithic microwave integrated circuit* (MMIC) and radio frequency integrated circuit (RFIC) design. The Agilent ADS is chosen over Cadence

SpectreRF to be the simulation tool for the receiver design because it is able to support design of schematic, layout, frequency and time domain circuit simulation, and electromagnetic field simulation without having to switch from one CAD tool to the other [18]. The summary of the simulations provided by ADS throughout this entire thesis are:

- *Curve tracer template* for accurate transistor DC- biasing.
- S-parameter simulation for the active devices under *Simulation-S_Param* palette.
- Harmonic Balance simulation for frequency and time domain signal assessment under *Simulation-HB* palette.
- The *Smith Chart Matching* and *Impedance Matching* palette allowing the designer to obtain accurate impedance matching while achieving wideband low-pass, high-pass, or band-pass filtering.
- The import of HSPICE, SPICE3, and BSIM based transistor model file provided by different vendors and conversion into netlist for mixer design.
- Quick measurements of figure-of-merits such as PA power added efficiency (PAE), IIP3, and OIP3 by correctly setting up the *PAE, IP3in, and IP3out* blocks under *Simulation-HB* palette.
- Simulation using templates provided by *RF-design guide* allowing the designer to simulate the required receiver figure-of-merits (e.g. P1dB and NF) as well as the individual devices.

1.5 Thesis Organization

In chapter 2, a double-IF downconversion radio receiver (superheterodyne) is presented. The performance tradeoffs of the radio receiver sensitivity and selectivity are

also discussed. Different receiver architectures are compared and performance tradeoffs have been calculated.

In chapter 3, the approach of designing a microwave LNA is shown. The small-signal LNA is able to provide moderate power gain, power consumption, low NF, and image-band attenuation integration. The load-pull method of designing a class-A power amplifier (PA) is explained as well. Load-pull method is essentially a process of varying the output impedance presented to the active component (e.g. amplifier transistor) while plotting the power and efficiency parameters on the Smith Chart. Having a larger constant output power contour on load reflection coefficient plane can ensure the amplifier transistor to be less sensitive to the output impedances. Therefore, it is desirable to be the buffer PA in a series of cascaded PAs.

In chapter 4, the fully differential (Gilbert) mixer is discussed and simulated. It is the most widely adopted topology existing in the modern radio receiver for the ability of providing low port feedthrough and intermodulation distortion (IMD).

In chapter 5, all active components built are cascaded for the verifying a series of assessments (e.g. last IF signal). The most important outcome in this radio receiver design is that it is able to downconvert the desired frequency range to the same last IF frequency (i.e. 20 MHz) only with slightly different waveform amplitudes.

Chapter 6 concludes the thesis by listing main contributions and details the future work which can be carried out in the Wireless Design Laboratory based on this thesis.

Chapter 2

Superheterodyne Receiver

In order to ease off the tradeoffs between image rejection and channel selection the superheterodyne receiver can accommodate multiple frequency conversion stages each followed by signal amplification and filtering. Therefore, filter quality factor must be considered. In order to find the perfect balance between the channel selection (selectivity) and image-rejection (sensitivity) of superheterodyne receiver, it is essential to quantify these two parameters from perspective of entire receiver other than individual component in the chain.

Selectivity is a measure of ability of the receiver to demodulate a desired small signal in presence of adjacent channel interference (blocker). Sensitivity indicates receiver's ability to demodulate a desired small signal in the presence of surrounding noise with acceptable signal-to-noise ratio (SNR).

In this chapter, we are going to discuss tradeoffs associated with single-IF (heterodyne) receiver. In addition, the superior performance of superheterodyne receiver has been illustrated.

2.1 Single-IF Tradeoff

Before illustrating the concept of superheterodyne (dual-IF) receiver it is best to look at the general tradeoff between selectivity and sensitivity of a single-IF (heterodyne)

receiver. The tradeoffs result from the selection of mixer intermediate frequency (IF) and ability of processing the desired channel while filtering strong blockers (adjacent channels). According to Equation (2.1) filtering for desired channel at high center frequency (f_o) with strong adjacent channel (blocker) will require extremely high filter quality factors (Q) given BW_{3dB} is the filter 3dB bandwidth.

$$Q = \frac{f_o}{BW_{3dB}} \tag{2.1}$$

A lossy circuit (high Q) magnifies the NF of the proceeding blocks by the attenuation factor [3,19]. Therefore, to reduce the filter Q the f_o should be reduced. A conventional heterodyne receiver is shown in Figure (2.1) .The tuned oscillator can be designed to be tunable for a certain bandwidth to mix with a band of radio frequencies (RF) to produce a fixed IF. The Q of band-select filter is usually very high due to operating at high frequencies, therefore, only very limited suppression can provide to the undesired image band.

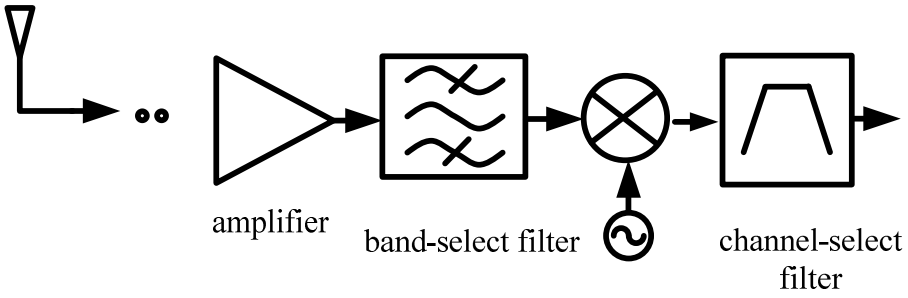


Figure 2.1 Conventional heterodyne receiver.

The Figure (2.2) shows the potential spectra of the frequency planning for single-IF (heterodyne) receiver. Proceeding the band-select filter the mixer performs frequency conversion by taking the two input frequencies, usually called radio frequency ($f_{RF\#1}$) and local oscillator ($f_{LO\#1}$) frequencies. After the mixing process the difference frequency (i.e. $f_{IF\#1}=|f_{RF\#1} - f_{LO\#1}|$) is generated, namely, "intermediate frequency" (IF). It is within ones instinct there will be two RF frequencies that will generate the same IF at the output of the mixer. With one RF frequency ($f_{RF\#1}$) being desired will set the other undesired RF frequency to be so called "image frequency" ($f_{image\#1}$).

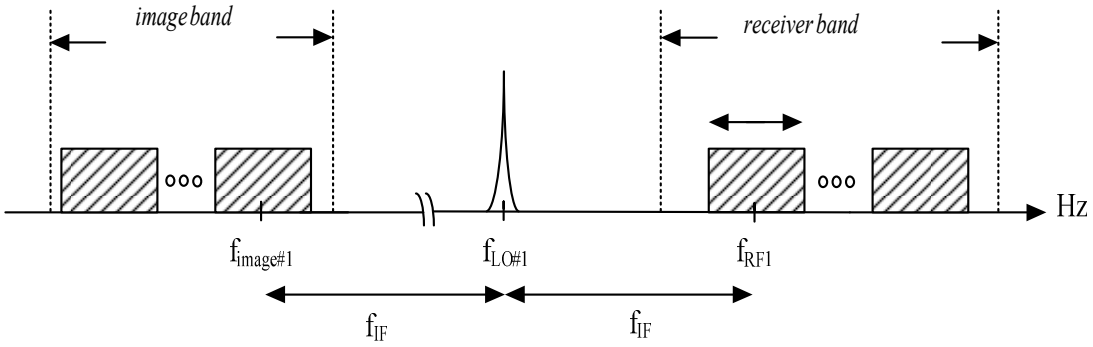


Figure 2.2 Heterodyne receiver with receiver and image band tradeoffs.

Frequency planning is extremely important for receiver design as several tradeoffs should be carefully considered. One can refer to Figure (2.3) for the compromise between receiver selectivity and sensitivity. The Figure 2.3 (a) shows low IF after the mixing process. Recall Equation (2.1) which defines the Q of a filter. With sufficient low IF, the Q of channel selection filter proceeding the mixer can be relatively high. Therefore, low IF allows great adjacent channel (blocker) suppressions with limited image frequency suppression. On the contrary, Figure 2.3 (b) indicates high IF leading to substantial rejection of the image frequency with poor channel selectivity (blocker) that results in adjacent channel leakage [3, 20].

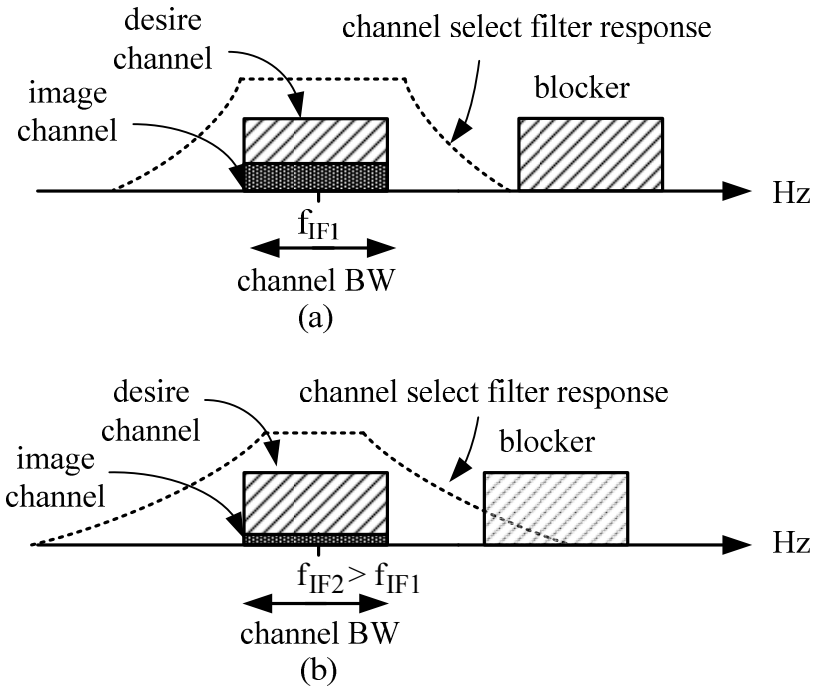


Figure 2.3 Heterodyne receiver (a) high selectivity (Low IF)
(b) high sensitivity (High IF).

It is apparent that the traditional single-IF (heterodyne) receiver exhibits a tradeoff between channel selection and image frequency rejection. Receiver with better channel selection exhibits better selectivity while better image frequency suppression indicates better sensitivity [3, 20].

In the next section, the detailed operation of superheterodyne receiver is discussed. With double frequency conversion, the balanced between the selectivity and sensitivity tradeoffs can be achieved with appropriate operation frequency chosen for devices in the receiver chain.

2.2 Superheterodyne Receiver

The radio receiver recovers the transmitted baseband data by essentially reversing the functions of the transmitter components. The basic block diagram of transceiver is shown in Figure (2.4) [20].

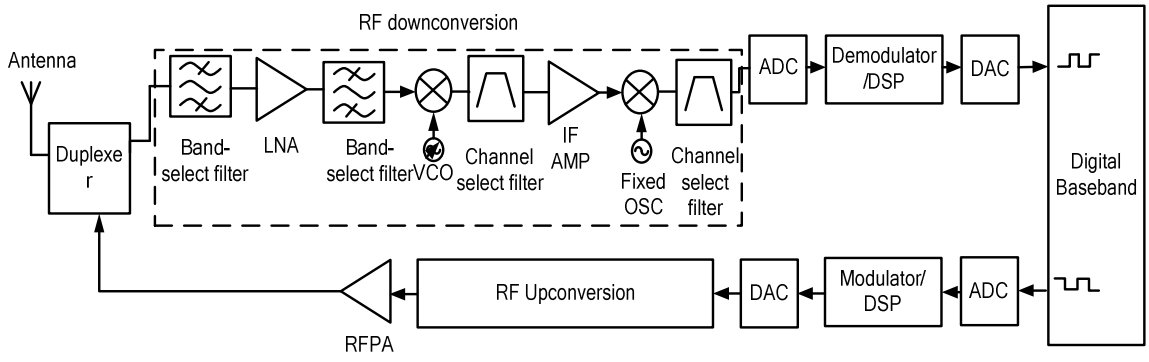


Figure 2.4 Basic transceiver block diagram.

The antenna that receives electromagnetic waves radiated from many source over a broad frequency range. After MEMS duplexer that allows bi-directional communication

over a single channel, the band-select filter (e.g. MEMS filter) selects the desired frequency band while suppresses the received signal at undesired frequency bands. Placing a band-select (image-rejection) filter reduces the possibility of signals at undesired frequencies from overloading the proceeding devices. The filter should have a low insertion loss. This implies that its stopband response will not be very sharp, so this filter generally does not provide much attenuation of image-rejection.

Low noise amplifier (LNA) has primary mission of amplifying the possibly weak received signal, while minimizing the added noise power. After the LNA, the first mixer is used to partially downconvert the signal frequency from RF to IF, which is generated by tuning voltage controller oscillator (VCO) to the necessary LO frequency. A channel-select filter, usually implemented by surface acoustic wave (SAW) filter is placed after the mixer to provide sharp cut-off response for undesired channel frequencies. A high gain IF amplifier compensates the losses of RF signal power up to the IF frequency at the RF downconversion stage before carrying out the second mixing process. After the second mixing process proceeds the last channel-select filter, setting the overall noise bandwidth of the receiver, as well as removing most unwanted mixer products. For example, harmonics of $f_{RF,}$ $f_{LO,}$ and other spurious response that may fall into receiver bandwidth (i.e. channel bandwidth). The baseband information is recovered by the combination of analog-to-digital (ADC) converter and digital signal processing (DSP) circuits. The digital-to-analog (DAC) converter is placed for possible recovering of voice information.

Comparing to single-IF (heterodyne) receiver, the superheterodyne topology can ease off the tradeoffs between band selection (sensitivity) and channel selection

(selectivity) .Superheterodyne receiver can accommodate multiple frequency conversion stages, to avoid problems due to LO stability, with each followed by signal amplification and filtering, therefore relaxing Q of the filters.

In this work, the RF double downconversion receiver front-end located in *IEEE* L-band shown in Figure (2.5) is simulated with the component operating frequencies shown in Table 2.1.With double frequency down-conversion the frequency assignments are carefully chosen to achieve the best balance between receiver selectivity and sensitivity.

Desire band (GHz)	2.53 to 2.83	Channel bandwidth (MHz)	5
Image band (GHz)	1.67 to 1.97	Channel spacing (MHz)	5
VCO tuning range (GHz)	2.1 to 2.4	Output of 1st mixer (MHz)	430
Fixed OSC (MHz)	410	Output of 2^{nd} mixer (MHz)	20

Table 2.2 Receiver frequency parameter.

The channelization of frequency division multiple access (FDMA) has been chosen for the superheterodyne receiver design. It uses an available system spectrum divided into individual frequency channels enabling access from multiple users.

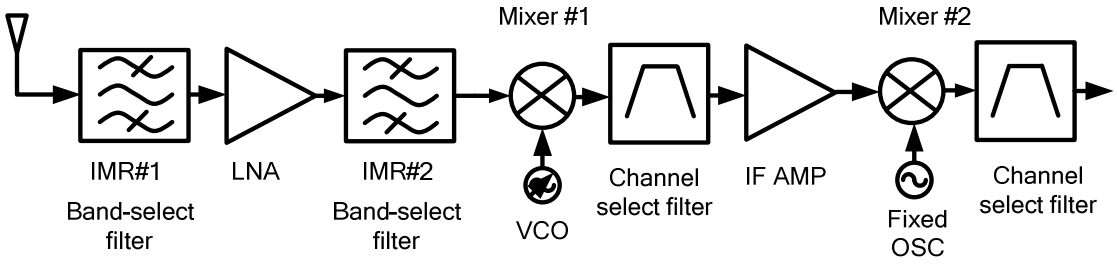


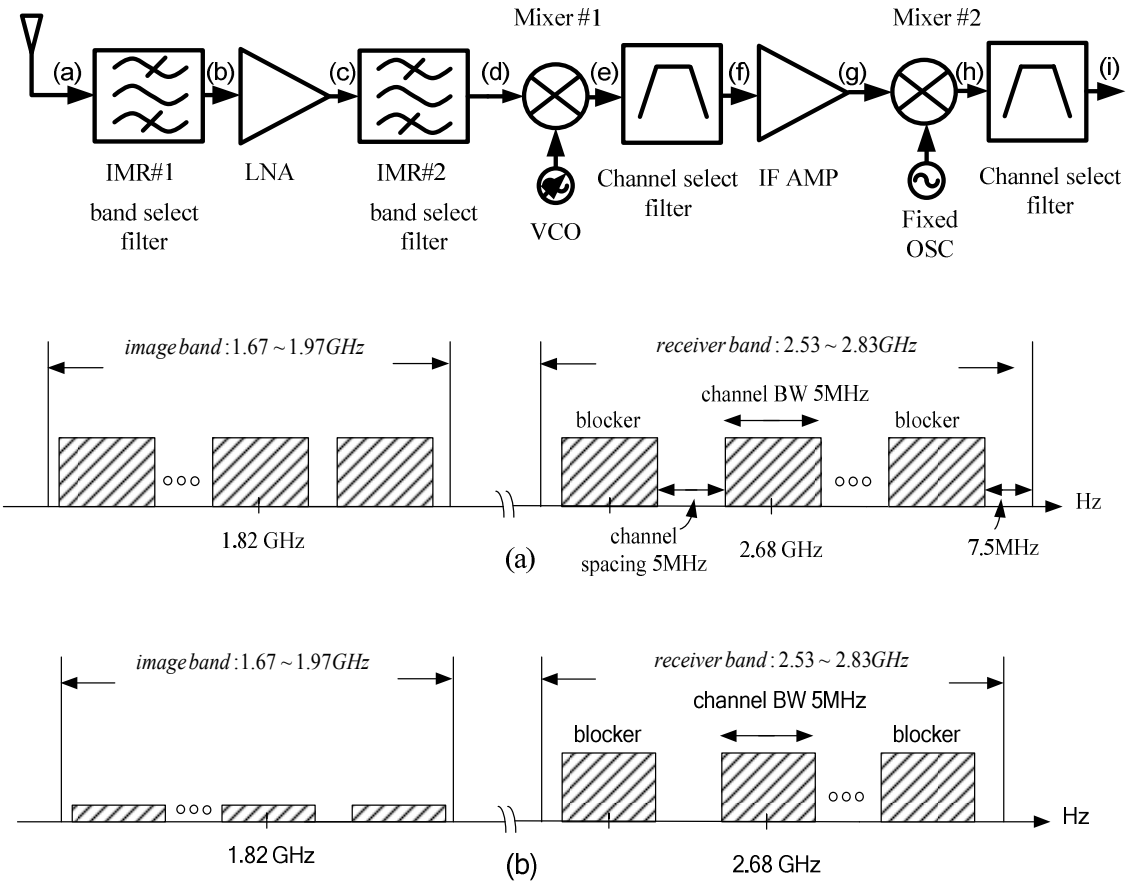
Figure 2.5 Structure of superheterodyne receiver.

The receiver is designed to process the desired signal band from 2.53 to 2.83 GHz with channel bandwidth of 5 MHz. In reality, the antenna receives signals in its bandwidth at different power levels. Above all, the unavoidable image band is particularly in designer's interest due to the mixing process in the receiver, therefore it should be attenuated by the band-select filters. The image band can be determined approximately spanning from 1.67 to 1.97 GHz by setting the IF of the first mixer equal to 430 MHz. In order to downconvert the entire signal band (i.e. 2.53 to 2.83 GHz), the first mixer is designed to be tunable from 2.1 to 2.4 GHz. For example, if one desires to access the channel at 2.68 GHz the first mixer should be tuned to frequency of 2.25 GHz and will output the first IF of 430 MHz. Any other IF frequency at the output of the first mixer will be seen as interferer and will be filtered by the following devices. Moreover, the *half-IF* spurs problem caused by nonlinearities of the mixer is also investigated [3, 20, 21]. For example, the *half-IF* problem can be caused by mixing the second harmonics of RF (e.g. 2 × 2.68 GHz) minus the half IF (i.e. 2 × 2.465 GHz) with the second harmonics

of the LO (i.e. -2 × 2.25 GHz) to produced the unwanted signal at the desired IF of 430 MHz. The easiest way to mitigate this problem is to maintain the duty cycle of the mixer LO signal to suppress the even order harmonics.

After the process of filtering and amplification, the second mixing process will take place to downconvert the 430 MHz signal leaving the last IF at 20 MHz with bandwidth of 5 MHz. One can refer to Figure (2.6) for more detailed signal spectra operation down the receiver chain. The antenna being the first device in the receiver will pick up the signals at all frequencies in the free-space. Out of all the interferences, the image band (1.67 to 1.97 GHz) shown in Figure 2.6 (a) is converted to the same IF as the desired signal band. The first device proceeds the antenna is usually a lossy band pass filter (BPF), which can partially suppress the image band signal (2.53 to 2.83 GHz) as shown in Figure 2.6 (b). Following the first band-select filter the LNA will amplify the weak received in-band signal, while minimizing the added noise power. The signal spectra at the input and output of the LNA shown in Figure 2.6 (c) may not differ much since the primary deign objective of the LNA is minimizing the noise power. Nonlinearity will take place at the output of active devices (e.g. LNA), therefore, in reality the signal spectra will be messier than shown. The purpose of the second band-select filter is to further suppress the out-of-band signals, shown in Figure 2.6 (d). In order to balance the receiver selectivity and sensitivity, the first IF of 430 MHz has been chosen. After the first mixer, the desired channel is located at 430 MHz with image channel in the out-of-band suppressed to a relatively low power level as illustrated in Figure 2.6 (e). At the center frequency of 430 MHz and bandwidth of 5 MHz, the first channel-select filter can band pass the desired channel with relatively relaxing Q (i.e. Q ≈

86) for the second mixing process. After several filtering and first mixing process the IF amplifier can provide high gain to raise signal power level at the desired frequency as shown in Figure 2.6 (g). The second mixer in the receiver chain is designed to be driven by a fixed LO of 410 MHz to output the desired IF of 20 MHz with bandwidth of 5 MHz as shown in Figure 2.6 (h). At the frequency of 20 MHz the last channel-select filter can reduce the blockers' power level close to the noise floor as seen in Figure 2.6 (i).



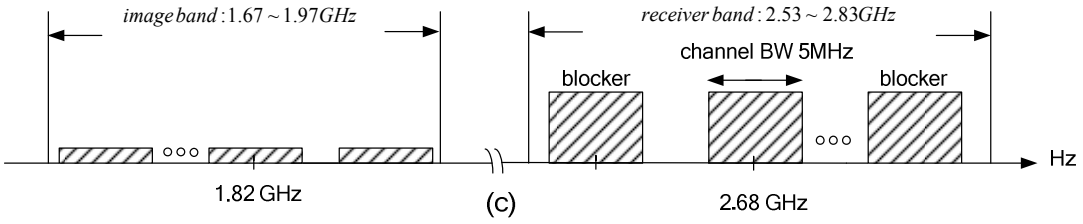


image band : 1.67 ~ 1.97GHz
receiver band : 2.53 ~ 2.83GHz
channel BW 5MHz
blocker
blocker
Hz
1.82 GHz
2.68 GHz

(c)

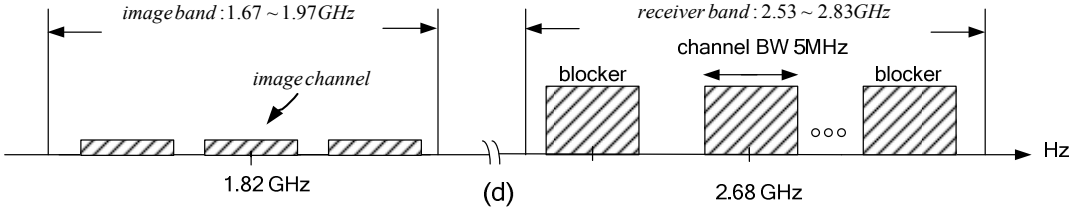
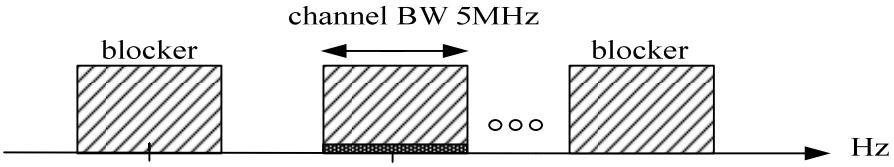
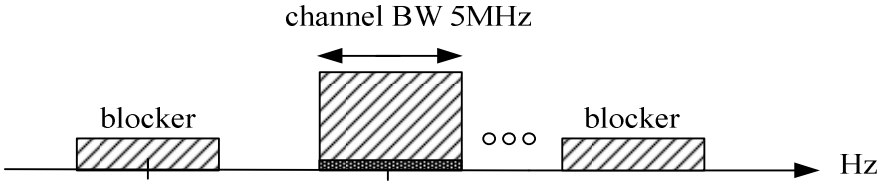


image band : 1.67 ~ 1.97GHz
receiver band : 2.53 ~ 2.83GHz
channel BW 5MHz
image channel
blocker
blocker
Hz
1.82 GHz
2.68 GHz

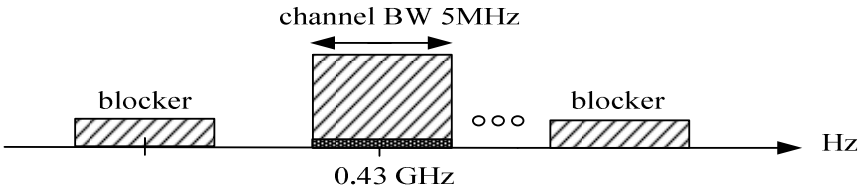
(d)


channel BW 5MHz
blocker
blocker
Hz
0.43 GHz

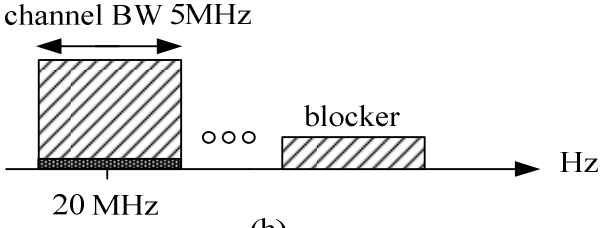
(e)


channel BW 5MHz
blocker
blocker
Hz
0.43 GHz

(f)


channel BW 5MHz
blocker
blocker
Hz
0.43 GHz

(g)


channel BW 5MHz
blocker
Hz
20 MHz

(h)

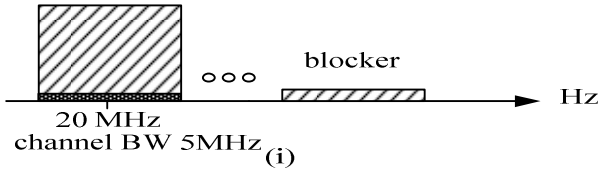


Figure 2.6 Superheterodyne receiver with simplified signal spectra.

2.3 Sensitivity

Nowadays, the receiver must be sensitive enough to detect signal levels as low as -110 dBm, while not overloaded by much stronger interferers [1, 3, 20]. The receiver sensitivity is an indication of the minimum detectable signal (MDS) with acceptable minimum SNR (SNR_{min}), which is set by the receiver's modulation and demodulation scheme, therefore, the receiver MDS can vary depending on required SNR_{min}.

2.3.1 Active Device Sensitivity

Noise figure (NF) defined in Equation (2.2) can be used to determine SNR degradation by components in the receiver. Due to the internally generated noise, the output SNR (SNR_{out}) is always less than the input SNR (SNR_{in}).

$$NF(dB) = 10\log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{2.2}$$

To explore the relation between receiver NF and sensitivity, which is indicated by $P_{i,MDS}$, one can refer to Equation (2.3).

$$P_{i,MDS} = NF(dB) + SNR_{\min} - 174dBm/Hz + 10\log BW \tag{2.3}$$

where BW is the channel bandwidth and $P_{i,MDS}$ is the minimum detectable input level that achieves minimum required output SNR (SNR_{min}), which is determined by the system modulation scheme. For low fundamental power levels, the third order intermodulation products are still well below the noise floor. However, as the fundamental power increases, the third-order intermodulation products start to appear above the noise floor at three times the rate that of fundamental. Another parameter called spurious-free dynamic range (SFDR) indicates the range between the fundamental power and the third-order power equal to the minimum detectable signal (MDS) power. The expression of SFDR is shown in Equation (2.4) with P_{IIP3} indicates the input third order intercept point and $P_{i,MDS}$ represents the input MDS.

$$SFDR = \frac{2}{3}(P_{IIP3} - P_{i,MDS}) \tag{2.4}$$

In RF design, the upper end of SFDR defines the maximum input level in a two-tone test for which the third-order intermodulation products do not exceed the noise floor [3,19, 20].

2.3.2 Receiver Sensitivity

The noise appearing at the receiver's output is the combination of the noise picked up by the antenna and the noise generated within the receiver. Consider the following receiver chain in Figure (2.7) the receiver sensitivity illustrated in Equation (2.5) can be determined by knowing NF of each cascaded block. One should note that the noise contributed by each block following the receiver chain decreases as the gain preceding the stage increases. This implies that to achieve the lowest F, the first and

second blocks in the receiver should be designed with lowest noise as their primary objectives.

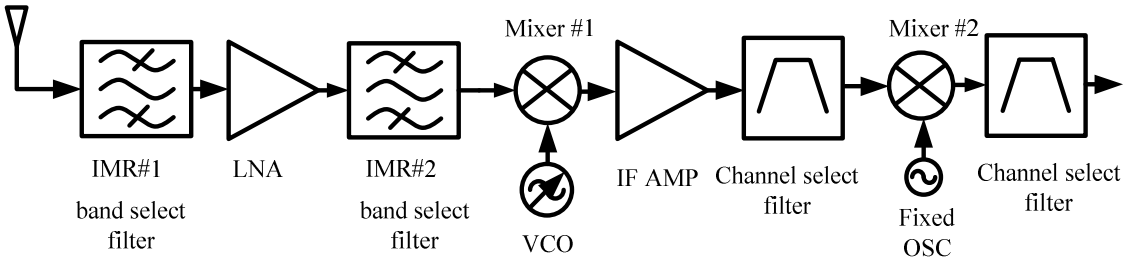


Figure 2.7 Typical receiver chain.

$$F = F_{IMR\#1} + \frac{F_{LNA} - 1}{G_{IMR\#1}} + \frac{F_{IMR\#2} - 1}{G_{IMR\#1} G_{LNA}} + \frac{F_{\text{Mixer}\#1} - 1}{G_{IMR\#1} G_{LNA} G_{IMR\#2}} + \ldots \tag{2.5}$$

2.4 Selectivity

The selectivity of radio receiver indicates the attenuation provided in the interferers and possible blockers adjacent to the desired channel. Selectivity is the property of a receiver that allows to separate a desired signal or signals at one frequency from those at all other undesired frequencies. Careful selection of receiver architecture and frequency plan can greatly relax the selectivity realization. For superheterodyne receiver it is more effective to achieve selectivity by downconverting a relatively wide RF bandwidth around the desired signal, and using a sharp-cutoff bandpass filter at the IF stage to select only the desired in-channel frequency band.

2.4.1 Active Device Selectivity

The small-signal S parameters are not useful for large-signal active devices such as highly efficient power amplifier (other than class-A operation) and mixer. Therefore, a set of large-signal parameters is needed to characterize the nonlinear active devices [1,3,19].

The effect of nonlinearities of the individual active component in the receiver is shown in Figure (2.8), which indicates the channel spectra at the input and output of a non-linear device (e.g. low noise amplifier). Up to the point, the in-band interferers are not attenuated by channel-select filter, therefore, the nonlinearity of the following stages, such as LNA, and any other nonlinear active devices are critical.

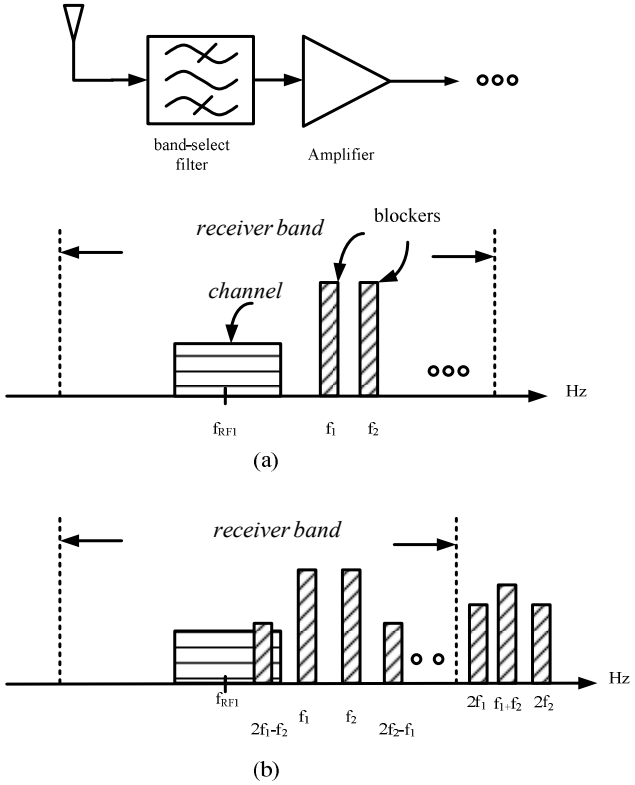


Figure 2.8 Signal spectra at (a) input and (b) output of front-end amplifier.

In general case, the output response (v_o) of a nonlinear circuit can be modeled by Taylor series expansion in terms of one-tone input signal voltages (v_i) with fundamental frequency of f_o as illustrated in Equation (2.6) below.

$$
\begin{aligned}
&One-tone: v_i = V_o \cos 2\pi f_o t \\
&One-tone: v_o = (a_0 + 0.5a_1 {V_o}^2) + (a_1 V_o + 0.75a_3 {V_o}^3)\cos 2\pi f_o t \\
&\qquad\qquad + (0.5a_2 {V_o}^2)\cos 4\pi f_o t + H.O.T \\
&Voltage\ gain: \frac{v_o(f_o)}{v_{i(f_o)}} = a_1 + 0.75a_3 {V_o}^2
\end{aligned}
\tag{2.6}
$$

The voltage gain expression above consists of Taylor coefficient a_1 and an additional term of a_3 proportional to the input signal amplitude V_0.In practical active devices the Taylor coefficient a3 will be less than zero, therefore the voltage gain can decrease with increasing value of input signal amplitude. Moreover, it is within one's instinct that highly linear active devices can suppress the Taylor coefficient a3 for higher voltage gain. With this gain saturation effect one can define the gain compression phenomenon for all the active devices. One can refer to Figure (2.9) for a typical active device response with output power versus input power.

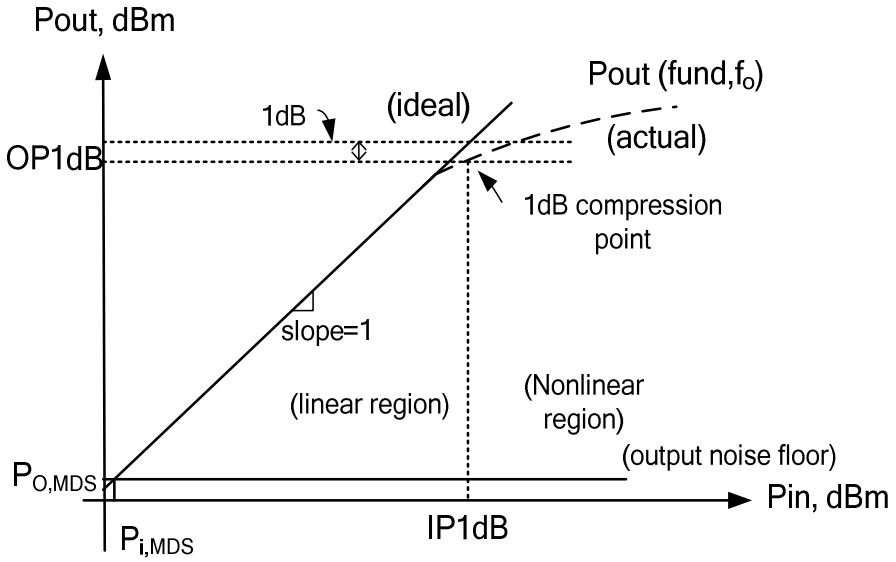


Figure 2.9 Active device 1dB compression point location.

For a perfectly ideal power amplifier, the plot of output power versus input power should be a straight line with slope of one unrestricted by the input power. However, due to the physical limit of power amplifier the output power will saturate at a certain level of input power. One can refer to Figure (2.9) for the 1dB compression point (P1dB), denoted by output power at fundamental frequency decreased by 1dB from the ideal extrapolated line. The P1dB has been widely used to denote upper power limit for an active device to behave in a linear fashion, it can be stated in terms of input referred power (IP1dB) and output referred power (OP1dB) for different active devices. Usually for amplifiers P1dB is specified as OP1dB while mixers are often specified as IP1dB.The two figures of merit can be related by the gain of the active device indicated in Equation (2.7).

$$OP1dB(dBm) = IP1dB(dBm) + G_A(dB) - 1 \tag{2.7}$$

where G_A is the small-signal linear available power gain. Moreover, note that the more linear the active device the higher input referred 1dB compression point (IP1dB) and output referred 1dB compression point (OP1dB) would be.

Recall Equation (2.6), which indicates that the output voltage of an active device consists of signals at fundamental (f_0) and harmonics frequency under one-tone excitation. Usually the harmonics generated at the output of active device will not lie in the desired operation bandwidth, therefore, will not impose significant amount of distortion on desired signal at fundamental frequency. Significant distortion can take place when active device is excited by two-tone input signal. In Equation (2.8), it is shown that output voltage consists several intermodulation products with decreasing amplitudes [3,20].

$$Two\,tone: v_i = V_o \cos 2\pi f_1 t + V_o \cos 2\pi f_2 t$$

$$\begin{aligned} Two\,tone: v_o = {} & a_0 + a_1 V_o(\cos 2\pi f_1 t + \cos 2\pi f_2 t) + \ldots \\ & 0.5 a_2 {V_o}^2 (1 + \cos 4\pi f_1 t) + 0.5 a_2 {V_o}^2 (1 + \cos 4\pi f_2 t) + \\ & a_2 {V_o}^2 (\cos[2\pi f_1 - 2\pi f_2]t + \cos[2\pi f_1 + 2\pi f_2]t) + \ldots \\ & a_3 {V_o}^3 (1.5 \cos 2\pi f_2 t + 0.75 \cos[4\pi f_1 - 2\pi f_2]t + 0.75 \cos[4\pi f_1 + 2\pi f_2]t) \end{aligned} \tag{2.8}$$

Depending on the active device, there are different output intermodulation frequencies products which the designer should consider. For example, when designing a mixer the desired output frequency will be the sum or difference of two input frequencies (f_1 and f_2).However, when it comes to amplifier design any other output frequencies other than f_1 and f_2 will be considered as distortions and needs to be filtered out. Out of so

many intermodulation distortions the third-order two-tone intermodulation products is in designers interest as they are located near f_1 and f_2 in operating bandwidth, thus, hard to filter out by lossy filters at high operating frequency.

Another important figure of merit called third-order intercept point (TOI) is also widely used to determine the active device linearity when fed by two-tone input signal . Recall Equation (2.8) as the input voltage V_o at fundament frequency increases, the voltages at the third-order product ($2f_1$-f_2) will increase at a rate of V_o^3. This can also imply that the ouput power of third-order product ($2f_1$-f_2) will increase with slope of three with the increasing input power at fundamental frequency (f_1). As seen in Figure (2.10) both power curves at both fundamental and third-order frequencies will saturate and inevitably intersect, therefore, it defines the TOI point. Note that the higher TOI indicates a highly linear active device [3,19].

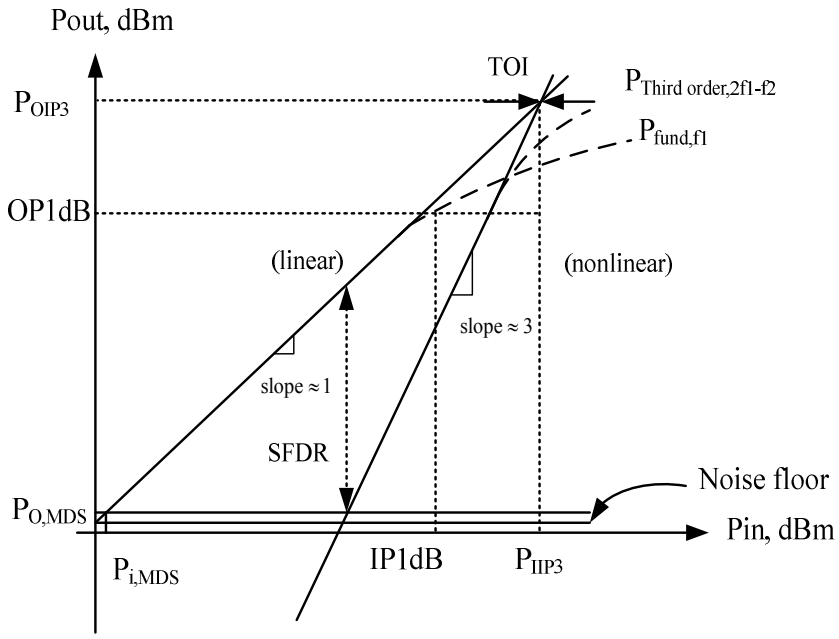


Figure 2.10 Active device IP3 point location.

2.4.2 Receiver Selectivity

After obtaining the knowledge of linearity of individual components in the receiver, the third order intercept point (TOI) can also indicate the receiver linearity. One can refer to Equation (2.9) for the cascaded input-referred third order intercept point (IIP3).

$$\frac{1}{P_{IIP3}} = \frac{1}{P_{IMR\#1}} + \frac{G_{IMR\#1}}{P_{LNA}} + \frac{G_{IMR\#1}G_{LNA}}{P_{IMR\#2}} + \ldots \tag{2.9}$$

From IIP3 expression above, it is observed that the tradeoffs between selectivity and sensitivity do exist. For example, to obtain a low receiver NF the LNA is often designed

with low NF and moderate power gain. However, increasing the power gain can reduce the receiver IIP3 and selectivity. Therefore, to relax the tradeoffs, the primary objective of designing a LNA should focus on lowering the NF.

In the receiver shown in Figure (2.11), the passive device such as band-select and channel-select filters are assumed to have infinity IP3 (e.g. $P_{IMR\#1} \approx \infty$), and those terms will go to zero in IIP3 equation. However, one will have to keep track of their gains (losses) [3].

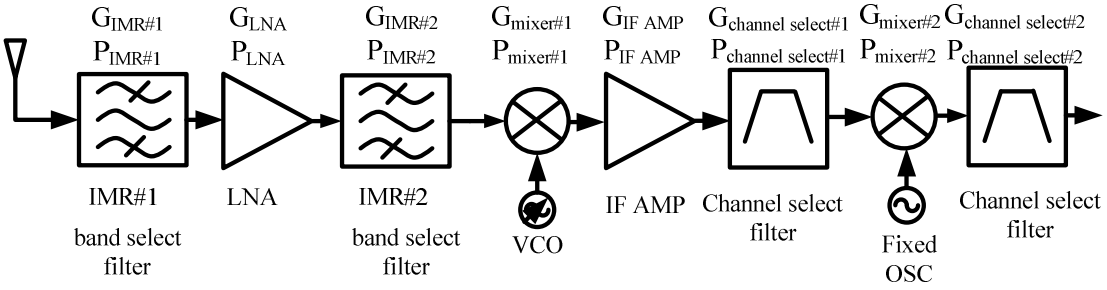


Figure 2.11 Receiver components with individual IIP3 and available gain.

2.5 Summary

In this chapter, the tradeoff between receiver selectivity and sensitivity is discussed. The superheterodyne receiver is shown to have achieved the balance between the two important figures of merit. Moreover, the operation frequencies for the active devices designed using Agilent EEsof EDA Advanced Design System (ADS) in the receiver chain have been initiated, which will be shown in the following chapters.

Chapter 3

Amplifier Design and Implementation

Amplification is a critical function in wireless receivers and transmitters. Nowadays, almost all microwave amplifiers utilize transistors based on compound material of silicon germanium (SiGe) and gallium arsenide (GaAs) for different purposes of either power consumption or hole mobility [22-23]. Ideally, a power amplifier (PA) is designed to fulfill a wide variety of specifications such as linearity, noise figure, power gain, output power, efficiency, and bandwidth. Often, these parameters are interdependent and tradeoffs are considered. Highly linear communication systems are capable of employing higher level modulation scheme which results in increasing channel capacity.

In this chapter two class-A amplifiers are introduced. The first being small-signal low noise amplifier (LNA) , where the input signal power is considered as small-signal that the transistor can be assumed to operate as a linear device .The function of LNA, plays an important role in receiver designs. The main function is to amplify extremely low signals while adding the lowest possible noise (e.g. thermal and shot noise for BJT

based LNA), thus preserving the required Signal-to-Noise Ratio (SNR) of the system at extremely low power levels.

The second amplifier designed being class-A common Emitter power amplifier (PA) suitable for low voltage and wideband system, utilizing load-pull method (power matching) for maximum output power transfer. In this design conjugate matching is not used because it does not result in maximum power transfer. Another reason of utilizing load-pull method is because conventional S-parameter is defined independent of input power level of transistor and assumed amplifier behaves linearly with signal power well below compression point. Therefore, the S-parameter design technique contradicts with the objective of maximum output power transfer, which deliberately operates near the compression region of the amplifier.

3.1 Amplifier Fundamentals

3.1.1 Gain Definitions

Almost all single stage microwave amplifiers with input matching and output matching circuit can be characterized as shown in Figure (3.1) . Input matching circuit (IMC) and output matching circuit (OMC) are placed in the circuit to reduce power reflections. Together with S-parameter and different reflection coefficients (Γ) ,the three different gain expressions of the microwave circuits are defined in Equation 3.1 from the power distributions in Figure (3.1) .Transistor modeling under high frequency using S-parameter has been adopted extensively because conventional open or short circuit test can be unrealizable and may cause circuit oscillations with the parasitic elements.

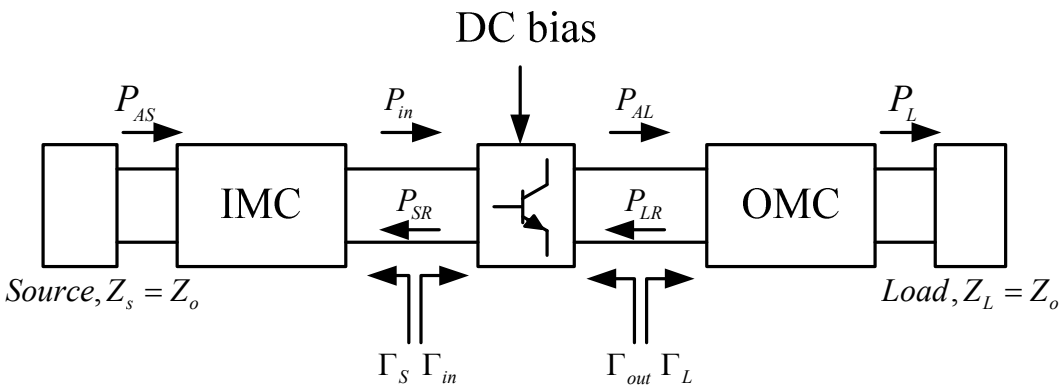


Figure 3.1 Power distribution of single stage amplifier.

$$G_T(Transducer\,Gain) = \frac{P_L}{P_{AS}}$$
$$G_P(Power\,Gain) = \frac{P_L}{P_{in}} \tag{3.1}$$
$$G_A(Available\,Gain) = \frac{P_{AL}}{P_{AS}}$$

One can obtain theoretical maximum power transfer when simultaneous conjugate match (SCM), $\Gamma^*_{in}=\Gamma_s$ and $\Gamma^*_{out}=\Gamma_L$, can be obtained. The Equation 3.2 shows that given a unconditionally stable circuit (Rollett stability factor, K >1 and |D|=|S11S22-S12S21|<1) no power is reflected (i.e. P_{SR} and P_{LR}=0 dB) thus providing maximum power transfer.

$$G_{T,\max} = G_P = G_A = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \tag{3.2}$$

However, most of the time the condition for SCM is not fulfilled and it is possible to optimize the power gain of the amplifier while $G_{T,\max}$ is not attainable. Source (input) mismatch factor (M) and voltage standing wave ratio (VSWR) defined in Equation 3.3 are two useful parameters to indicate maximum power transfer.

$$M_s = \frac{(1-|\Gamma_{in}|^2)\times(1-|\Gamma_S|^2)}{|1-\Gamma_S\Gamma_{in}|^2} = 1-\left[\frac{VSWR-1}{VSWR+1}\right]^2 \quad (3.3)$$

Having VSWR or M near unity (i.e. P_{SR}=0 dB) ensures that the amplifier absorbs most of the power available from the source. This can also lead to Equation 3.4 with both G_T and G_P in absolute units.

$$G_T = M_s \times G_P \quad (3.4)$$

The bottom line in designing small-signal amplifier is to have high power gain, G_P, and good input matching (i.e. M_S equals unity) to produce the maximum transducer gain (G_T). From [22-23], the constant input VSWR circle can be plot by choosing the value of Γ_L and M. Also, the Γ_{in} can be derived by value of Γ_L .This is extremely useful when it comes to designing low noise amplifier (LNA) since having control over both input VSWR and NF circle plot on Γ_S plane can ensure both low NF and amount of power available for the load.

3.1.2 Stability

An amplifier is a circuit designed to enlarge electrical signals. Stability of a circuit defined as having no output signal produced when there is no input signal**.** If the amplifier produces an output when there is no input present, the amplifier can behave as an oscillator. At high frequencies, the parasitic capacitances in a transistor may produce feedback at certain frequencies, resulting in potentially instability. Therefore, after DC

biasing the stability test of a transistor up to its transition frequency (f_T) must be carried out. Usually, a potentially unstable transistor can be made unconditionally stable by introducing negative feedback and additional resistive loading with the compromise of power gain [22-23]. Stability analysis is carried out by assuming small-signal amplifier, since the initial signal that causes oscillation is always small. Refer to Figure (3.2) where the shaded region indicates stability region where the load stability circle (LSC) and source stability circle (SSC) are both plotted assuming $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$,respectively.

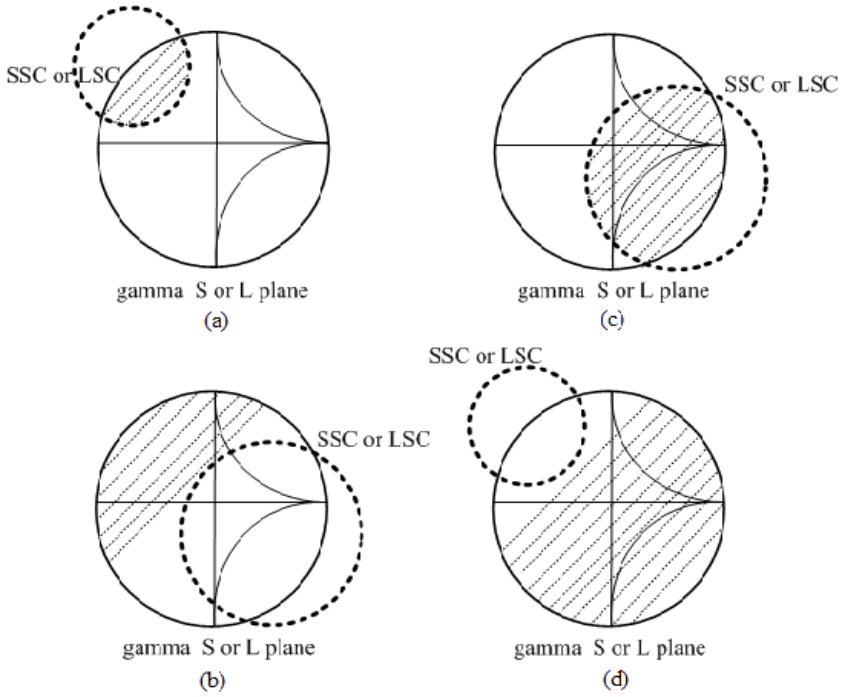


Figure 3.2 (a, b) Stability region (shaded) with $|S_{11}|$ or $|S_{22}|>1$ (c, d) $|S_{11}|$ or $|S_{22}|<1$.

The intuitive way of determining the stable region on the $|\Gamma_s|$ and $|\Gamma_L|$ plane depends on the value of $|S_{11}|$ and $|S_{22}|$, respectively. If the $|S_{11}|$ or $|S_{22}|$ are less than unity, the stable region has to include the center of the Smith Chart regardless of the size of the LSC or SSC, respectively. On the contrary, when the $|S_{11}|$ or $|S_{22}|$ are greater than unity the stable region must not include the center of the Smith Chart.

3.1.3 Conjugate and Power matching

Conjugate matching ensures maximum power gain, however, it does not provide maximum power transfer to the output in reality. One of the principal differences between linear microwave amplifier design and power amplifier design is that for optimum power, the output of the device is often not present with conjugate match impedance. This has been the subject of debate about the meaning of "conjugate matching" because the usual conjugate matching theory usually does not deliver as much power to the output as power matching [24]. Conjugate matching leads to maximum power transfer solely based on the source generator having no physical limits on both current and voltage while power (load-line) matching is a real-world compromise [24].

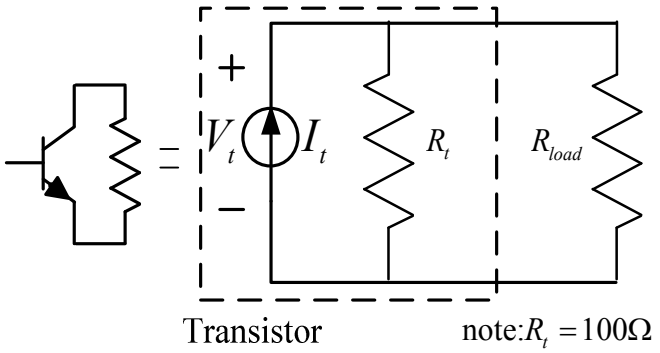


Figure 3.3 Maximum power transfer.

Referring to Figure (3.3) with current source and resistor in parallel imitating a transistor, one can easily distinguish between conjugate and power match. Assume I_t can supply maximum current of 1 A, under the conjugate matching condition the R_{load} should be set equal to R_t. The two resistors of 100 ohm in parallel will lead to an equivalent resistor of 50 ohm. This will lead to the terminal voltage, V_t, of 50 V assuming maximum

current utilized. However, this value is over the maximum allowable voltage swing, which is limit by the DC voltage supply. Moreover, the maximum terminal voltage can exceed even without utilizing maximum current of 1A.

In order to utilize the maximum current and voltage swing of the transistor, a lower value of load resistance, R_{load}, would need to be selected. The power matching involves choosing a R_{load} different than R_t with several tradeoffs such as gain, VSWR, and stability considered. It is necessary to extract the maximum power (it does not ensure maximum power gain) from RF transistors, voltage (or current) control current source, and at the same time accommodate maximum permissible current and voltage swing.

For linear class-A power amplifier with the transistor turned ON in the entire signal conducting period will present something close to its small-signal output impedance, represented by S-parameter to the proceeding device in the receiver chain. However, when it comes to highly efficient and non-linear type power amplifier (e.g. class-D biasing), which transistor can operate partially ON and OFF, an isolator or balanced configuration should be implemented to interface with the proceeding device.

3.1.4 Linearity

Depending on the modulation scheme the amplifier should exhibit good linearity to prevent spectral regrowth consists of odd-order distortions .Low spectral regrowth is an important aspect in modern communication system design because to use minimum

system bandwidth, channels are closely spaced and so any power leaking over from adjacent channels will cause an increase in adjacent channel interference.

The bandwidth efficient modulation scheme such as QPSK require linear PAs to minimize spectral regrowth and cross modulation. Several advanced PA linearity preservation techniques such as pre-distortion and feedforward are available [25]. However, some techniques are only suitable for certain classes of power amplifiers.

The intermodulation distortion (IMD) under two-tone (carrier) excitation with separation of Δf is an extension of harmonic distortion (HD), which is defined under one-tone excitation of power device under test (DUT), such as power amplifiers (PA). Having HD, the output of DUT contains multiple harmonics that are often out-of-band and easy to filter out. Nonlinearities of the DUT shown in Figure (3.4) is similar but third-order distortions at the output are often in the vicinity of the two carriers and are difficult to be filtered out.

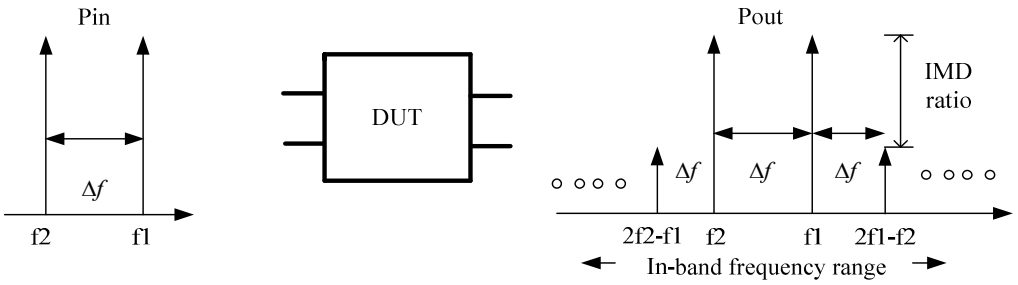


Figure 3.4 IMD representation of non-linear circuit (DUT).

Moreover, under a digital modulated system the linearity figure of merit called adjacent channel power ratio (ACPR) is often defined for IMD with the intermodulation bands stretch out to several times higher than the original modulation bandwidth. Among

several IMDs, the third-order is most concerned in a regulated communications band as it contributes the most amount of spectral leakage from desired to adjacent channel.

The output third order intercept point (OIP3) and input third order intercept point (IIP3) indicated in Figure (3.5) are obtained by extrapolation both first order and third order power, which are parameters assessing the IMD of the DUT. Usually, having higher IMD will lead to higher intercept point.

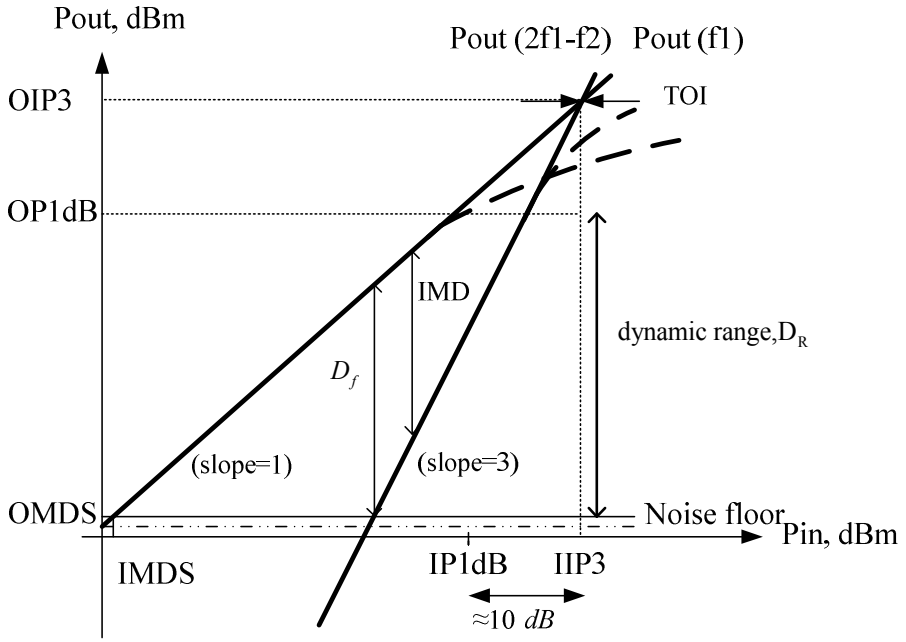


Figure 3.5 Input-output power relation of non-linear circuit.

Some input-output power rule-of-thumb can come in handy during the process of this simulation. One can approximate OIP3 from the output power spectrum of the two-tone (carrier) test, which is roughly defined as shown in Equation (3.5).

$$\begin{aligned} OIP3(dBm) &\approx P_{out,f1} + 0.5 \times IMD \\ &\approx 1.5P_{out,fundf1} - 0.5P_{out,third} \end{aligned} \tag{3.5}$$

With the above equation, it is possible to estimate the nonlinearities that can cause by the interferences in the receiver band. Suppose for a certain communication standard, the required SNR is 10 dB with the surrounded interferences. Suppose the desired input RF signal received has the power level of -100 dBm. The input third order IMD of the blocker in the desired frequency band must not be larger than -110 dBm to maintain the 10 dB margin to avoid overloading the receiver, since the channel filtering only happens until the first IF stage . If the input fundamental power of the blocker equals to -50 dBm, then according to Equation (3.5) the IIP3 will equal to -20 dBm (i.e. -50dBm+30 dB).

Also, refer to Figure (3.5), the IP1dB will be roughly -10 dBm. Therefore, the designer will be able to estimate the required IP1dB for the first device in the receiver (e.g. LNA), which in this case has to be larger than -10 dBm to avoid device saturation.

Spurious free dynamic range (SFDR) shown in Equation (3.6) is the region where the third order power is lower than the output minimum detectable signal (OMDS).

$$SFDR(dB) \approx \frac{2}{3}(OIP3 - OMDS) \tag{3.6}$$

Spurious free dynamic range is a useful figure-of-merit since within this range the third order power is less than the noise power, thus distortion can be negligible. Also, the SFDR can directly relate the device output sensitivity (OMDS) to selectivity (OIP3). In essence, a linear power amplifier should possess large SFDR, TOI, and dynamic range.

3.2 Low Noise Amplifier Design

The low noise amplifier (LNA) is a crucial device in the receiver as it should provide low NF, reasonable gain, and stability without oscillation over the entire useful frequency range, defined by unity current-gain frequency (f_T). To minimize the NF of the LNA, one can match the device to its noise matching impedance ($\Gamma_{s,opt}$), which is obtained at the impedance where the noise of the device is terminated. To minimize the noise seen by the output, one must perform noise matching at the IMC. Otherwise, the noise can be reflected back from the load to the transistor and amplified. However, both noise and gain matching are rarely obtained simultaneously. Moreover, as the gain of the device increases, the difficulty in obtaining a stable design becomes increasingly more challenging. Normally, a filter is placed in front of LNA to avoid overloading. Recall the receiver noise figure given in Equation (3.7). The receiver NF is mostly contributed by the NF of the first component in the receiver, given the gain provided by the proceeding devices are very large .

$$F_{receiver} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \tag{3.7}$$

In the design of LNA, the requirement of low noise performance often contradicts with achieving both highest available power gain and good input mismatch. There are several approaches to microwave/ RF LNA design, such as conjugate noise match (CNM) for off-chip design, simultaneous noise and impedance match (SNIM), and power constrained SNIM (PCSNIM) for on-chip design [26-28].

For the operating frequency and the transistor chosen, the CNM is able to achieve both low noise and moderate power gain (G_P). Therefore, the more complicated PCSNIM will not be needed in this specific case. CNM, the most widely adopted method, starts by choosing an optimum source reflection coefficient ($\Gamma_{S,opt}$) with lowest noise figure, moderate available gain, and perform conjugate (or power) matching at the output. However, choosing optimum source reflection coefficient does not allow full control over input VSWR, which is varied by load reflection coefficient (Γ_L).

In this design, the desired Γ_L is chosen by plotting constant optimum power gain (G_P) circle on Γ_L plane by fixing an acceptable input mismatch factor (M). With the chosen M, the transducer gain (G_T) can be obtained by recalling Equation (3.4). After obtaining the value of $\Gamma_{L,}$ the input reflection coefficient (Γ_{in}) can be calculated using Equation (3.8).

$$\Gamma_{in} = \frac{S_{11} - D\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.8}$$

With the help of Γ_{in}, the designer may plot the input VSWR circle [22-23]. Moreover, it is apparent that moving Γ_L can deviate Γ_{in}, thus, leading to the change of shape and location of the input VSWR circle. Therefore, this method gives the designer direct information on the "real" gain (G_T), NF, and M of the LNA before impedance matching. With a few iterations, the desired Γ_s is chosen overlapping the lowest possible constant NF and good input VSWR circles on the Γ_S plane. A more detailed design flow is shown in Figure (3.6).

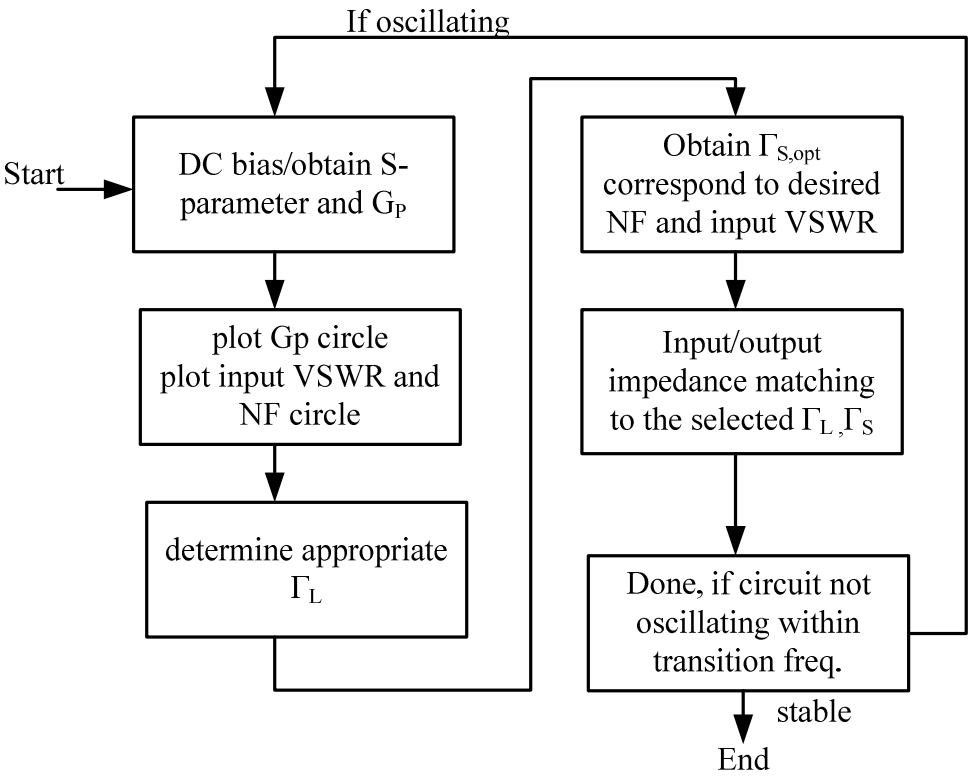


Figure 3.6 LNA design flow with CNM.

3.2.1 DC Bias and S-parameter Analysis

The primary goal of the LNA deigned is to provide lowest noise figure and moderate gain at the frequency range of 2.53 GHz to 2.83 GHz while suppressing the image frequency band ranging from 1.67 GHz to 1.97 GHz. First, the LNA designed in the center frequency of 2.68 GHz will be investigated. The silicon based NPN transistor *BFR520_19921214*, manufactured by Philips Semiconductor, is chosen for the simulation [29]. This is a wideband transistor capable of operating up to transition frequency of 9 GHz, which is suitable for this design since we are interested in the frequency range of 2.53 GHz to 2.83 GHz. A common Emitter DC biasing with ideal RF choke and DC block are shown in Figure (3.7) .

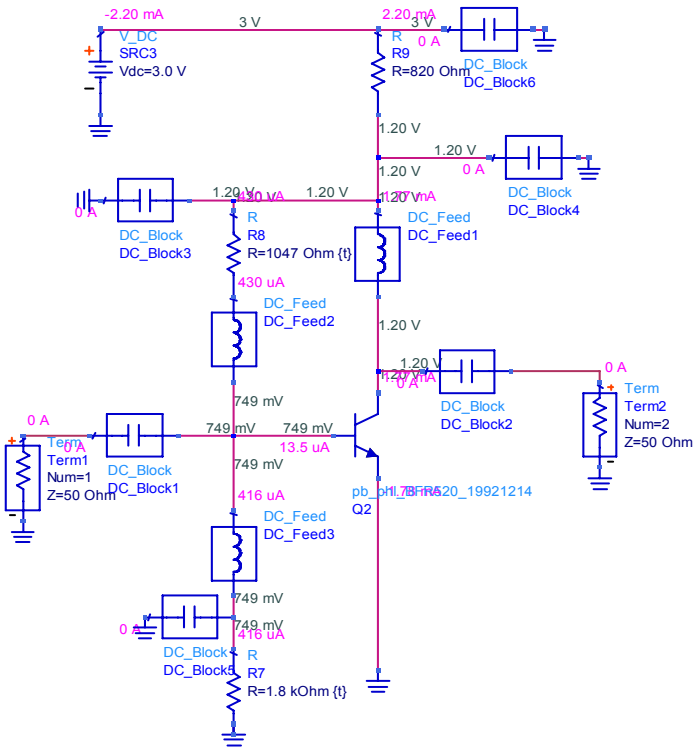


Figure 3.7 LNA DC self-bias with ideal decoupling.

The main purpose of BJT biasing is to ensure fixed Collector current regardless of any drift in the DC current gain. The passive biasing circuit employs resistor between Collector and Base junction, which imposes negative feedback for DC signal and helps to stabilize the bias point of the BJT [30]. Moreover, it provides Emitter current to be insensitive to variations of Collector-Emitter current gain (β) and transistor temperature by choosing $R_B/ (\beta+1) << R_C$ with R_B, R_C, β equals to 1.047 kΩ , 820 Ω, and ≈131 A/A, respectively. According to the data sheet of the transistor, the Collector terminal set at 1.2V DC can provide class-A voltage swing at the output given the supply DC voltage is set at 3V.

To provide additional linearity for the LNA the passive decoupling element such as DC Blocks and RF Chokes placed in the circuit for blocking DC and RF signals which are capacitors and inductors , respectively. The inductor value should mimic high

impedance (approximately 1 KΩ) at the operating frequency. The choice of capacitor is to short the RF signal or to open circuit DC voltages. Additional inductor, introducing negative feedback for RF signal, can be placed in the Emitter terminal (i.e. Emitter degeneration) for better linearity with the purpose of helping better noise matching and wider operation bandwidth [22-23, 30]. However, the side effects are reduction of device available power gain, degradation of reverse isolation (i.e. S12), and the increase of tendency for circuit oscillation [22-23, 30].

3.2.2 Notch Filter

A series resonant LC notch filter is shown in Figure (3.8) , which is eventually integrated with the LNA to provide sufficient attenuation at the image frequencies 1.67 GHz to 1.97 GHz.

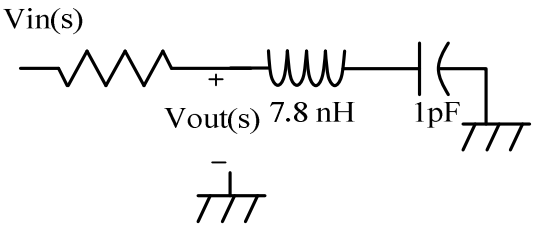


Figure 3.8 Notch Filter schematic.

In this design, the notch filter is implemented based on the frequency of maximum rejection illustrated in Equation (3.9).

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{3.9}$$

The center rejection frequency of roughly 1.8 GHz can be achieved by choosing values of both inductor and capacitor equal to 7.8nH and 1pF, respectively. Also, the magnitude and phase response is shown in Figure (3.9) with roughly 10 to 40 dB of the attenuation for the desired rejection frequency band (i.e. 1.67 GHz to 1.97 GHz) with the insertion loss of roughly 5 dB.

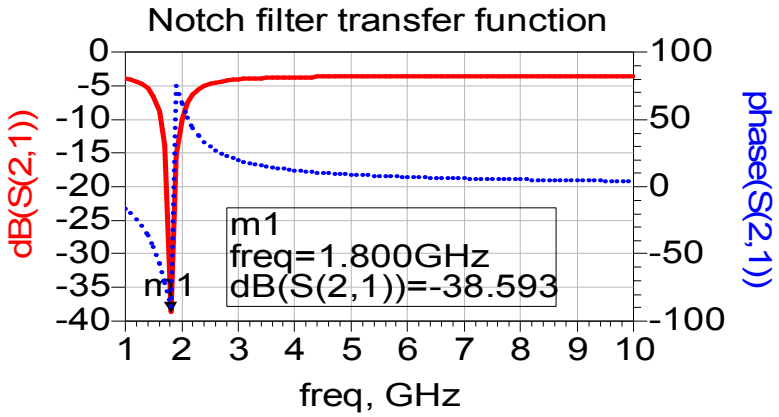


Figure 3.9 Notch filter frequency response.

The undesired frequency suppression is achieved by inserting a notch filter at the Collector terminal of the BJT. The designed LNA loaded with simple notch filter is found to be more linear with the compromise of power gain, NF and input VSWR as shown in the next section. The notch filter is kept as simple as a second-order LC circuit in order to avoid circuit oscillation (e.g. |S11|> 0 dB) as well as longer filter group delay, which is proportional to the order of the filter and inverse proportional to the filter bandwidth.

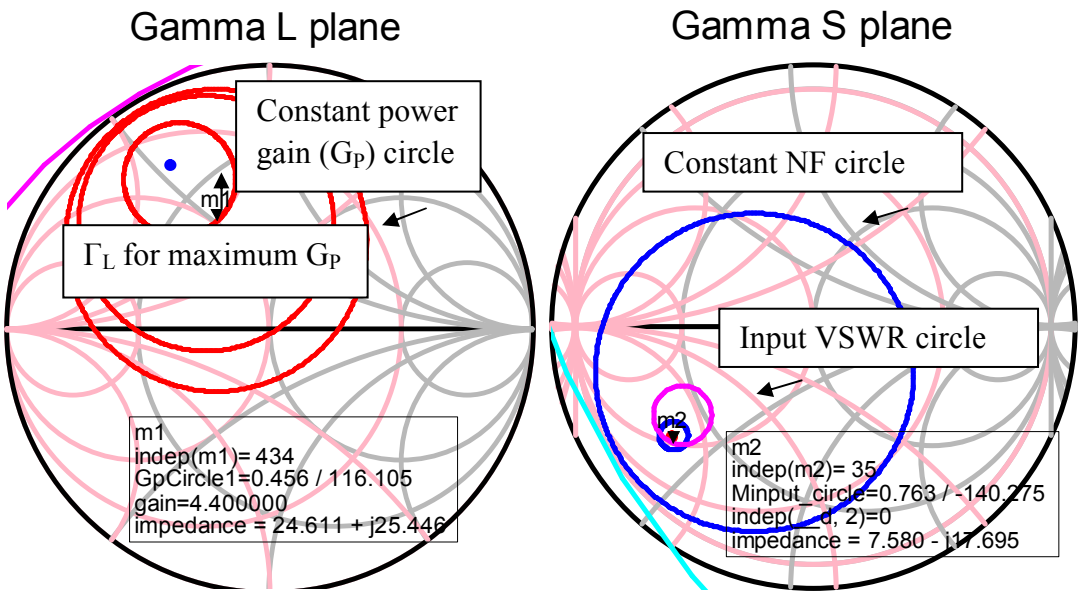
3.2.3 Low Noise and Input VSWR Matching

With the *S-parameter* simulation in ADS, the parameters in Table 3.1 indicate that the circuit is unconditionally stable at the operating frequency of 2.68 GHz with transducer power gain (i.e.|S21|) of 4.42 dB and NF_{min} of 0.45 dB, which is defined as the minimum noise figure when input is terminated with optimum source impedance.

Parameter	value	unit
Frequency	2.68	GHz
K	1.01	None
|D|	0.63	None
|S11|	-3.28	dB
|S22|	-6.20	dB
|S21|	4.42	dB
NF_{min}	0.45	dB
Optimum source impedance	7.58-j17.7	Ω

Table 3.1 LNA single frequency simulation before impedance matching.

According to design flow in Figure (3.6), the next step would be plotting constant power gain (G_P) circle on Γ_L plane with constant input VSWR and noise figure (NF) circle on Γ_S plane. Varying Γ_L can vary Γ_{in} thus changing the location of constant input VSWR circle on the Γ_S plane. In Figure 3.10 (a) below, the constant (G_P) circle of 4.4 dB indicates selection of $\Gamma_L=0.456/116.1^o$ (m1) on gamma-L plane leading to the corresponding input mismatch factor (M) of 0.95 (VSWR= 1.58) and noise figure of 0.46 dB (m2) on gamma- S plane in Figure 3.10 (b), which roughly equals to NF_{min} .



(a) (b)

Figure 3.10 (a) G_P circle and LSC (b) NF, VSWR circle, and SSC.

Lastly, the conjugate of $\Gamma_L=0.456/116.1^o$ and $\Gamma_S=0.76/-140.28^o$, as indicated by the markers on the Smith Chart, should present to the source and load of the transistor for low noise figure and moderate gain matching for the LNA. Moreover, for achieving higher linearity as the primary concern, different matching approaches can be followed. Envelope termination is widely adopted for linearity matching for better P1dB and TOI [31].In this design the matching of corresponding Γ_L approach (power matching) is followed as the gain is already significantly degraded by the selection of transistor and later on the integration of notch filter.

It is important to assess the LNA stability upon integrating the notch filter. In this design the circuit starts to oscillate (i.e. |S11| > 0 dB) in the vicinity of 4 GHz, therefore resistive loading is added to IMC for stabilizing the transistor at the expense of degrading the gain and noise performance. Given the LNA is stabilized up to transistor transition

frequency (i.e. 9 GHz) with the resistive loading, the S-parameter simulation with respect to frequency for the LNA with and without the notch filter is shown in the Figure (3.11) .

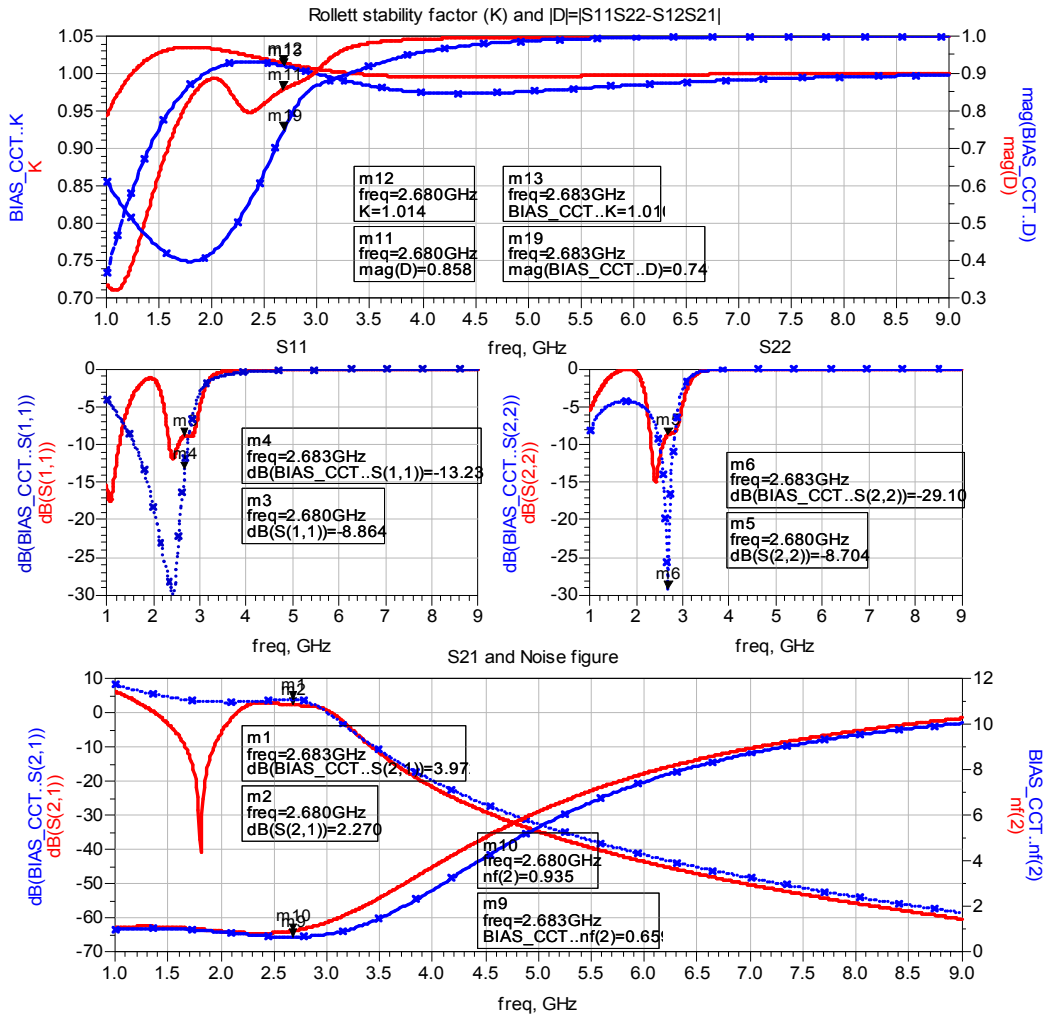


Figure 3.11 Simulated S-parameter of single-stage without (x) and with notch filter (solid).

The LNA integrated with notch filter is able to provide attenuation in the area of 1.8 GHz as well as the undesired band (1.67 GHz to 1.97 GHz) with approximately 2 dB power gain loss with only 0.3 dB NF degradation in the desired band (2.53 GHz to 2.83 GHz). In order to increase the power gain, a two-stage design is presented. Recalling Equation (3.7), two identical active circuits cascaded can give NF≈1.4 dB and $G_T \approx 4.5$ dB (i.e. 2.27dB + 2.27 dB). The same matching method is carried out while making sure

the circuit is unconditionally stable as described previously. The OMC in both stages is designed to match the conjugate Γ_L and the IMC is matched to low NF and good VSWR. The S-parameter simulation with respect to frequency for the two-stage LNA with notch filter and single-stage LNA without notch filter is shown in the Figure (3.12) .

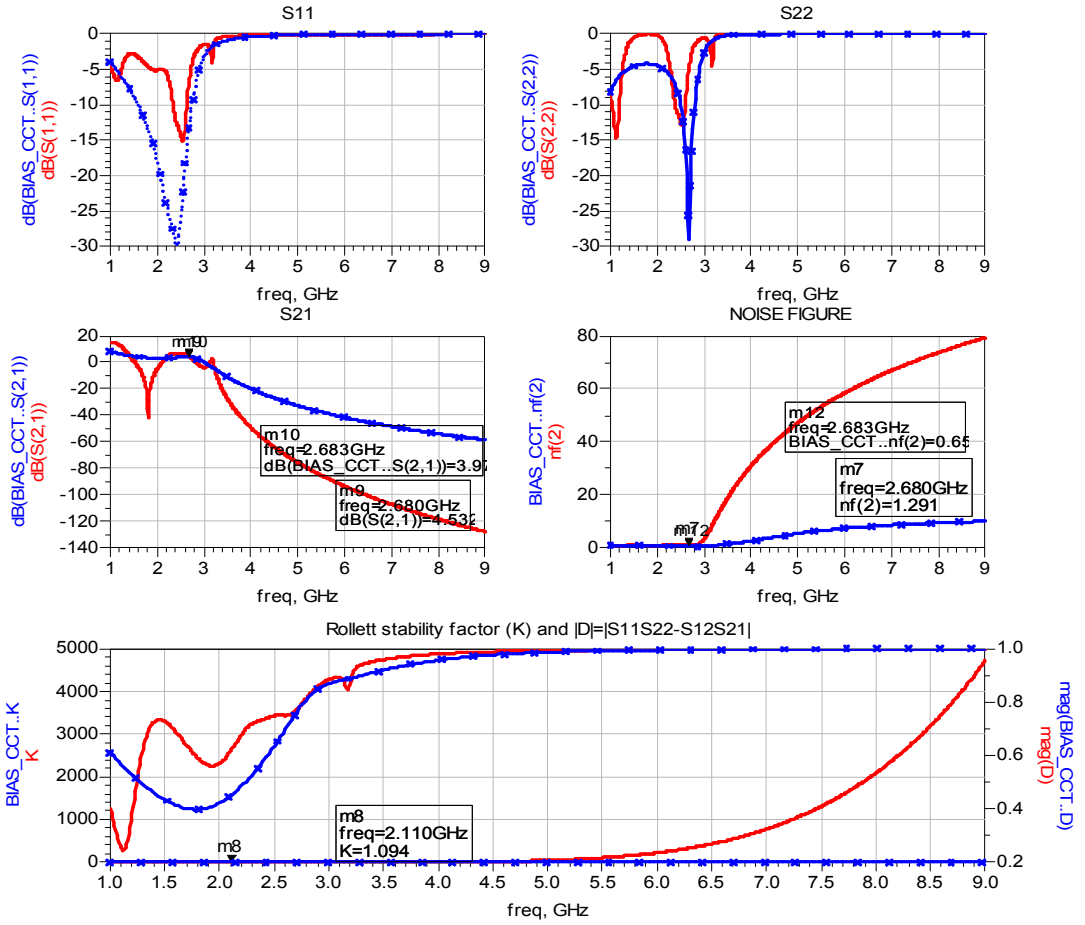


Figure 3.12 S-parameter of single-stage without notch filter (x) and two-stage with notch filter (solid).

3.2.4 Large-Signal Simulation

Upon simulating the transducer gain (G_T), some tuning is given to the components in the circuit to ensure stability. The Figure (3.13) showed the G_T of two-stage LNA (notch filter), single-stage LNA (notch filter) and single-stage LNA (no notch filter). The

single-stage LNA (no notch filter) is shown to have the smallest linear region, while the single-stage LNA (notch filter) shows the smallest power gain. The two-stage LNA (notch filter) is shown to have the largest linear operating region (i.e. highest IP1dB of ≈ 1 dBm) indicated by marker 3 (m3) at the same time achieving the highest power gain (i.e. ≈4.5 dBm) indicated by marker 7 (m7).

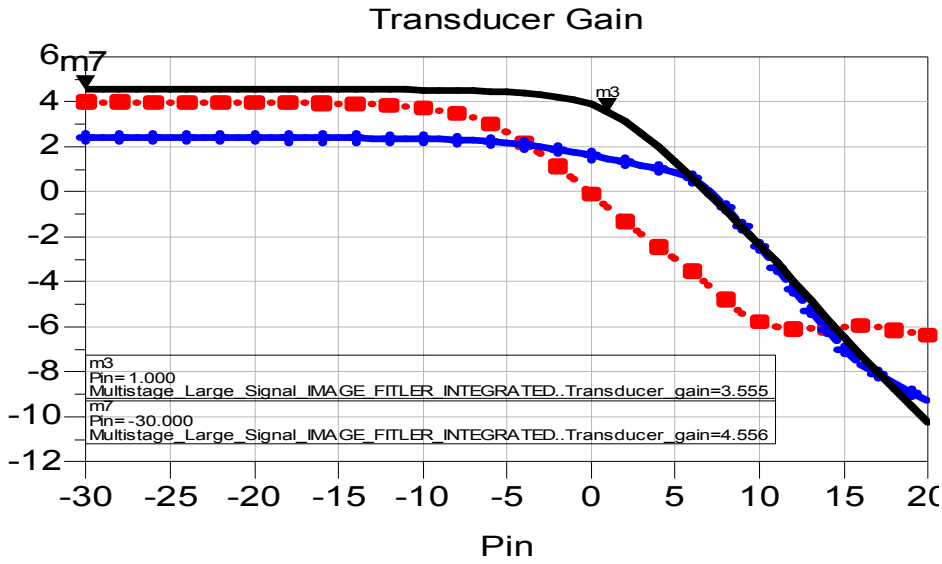


Figure 3.13 LNA G_T simulation.

It is possible to predict the IIP3 of the LNA under tow-tone simulation by observing the third order intercept as shown in Figure (3.14) .The IIP3 given by markers 1 (m1) produce an IIP3 of roughly -3.3 dBm. This is fairly close to the value generated by *IP3in* block under ADS *Simulation-HB*, which is -3.78 dBm.

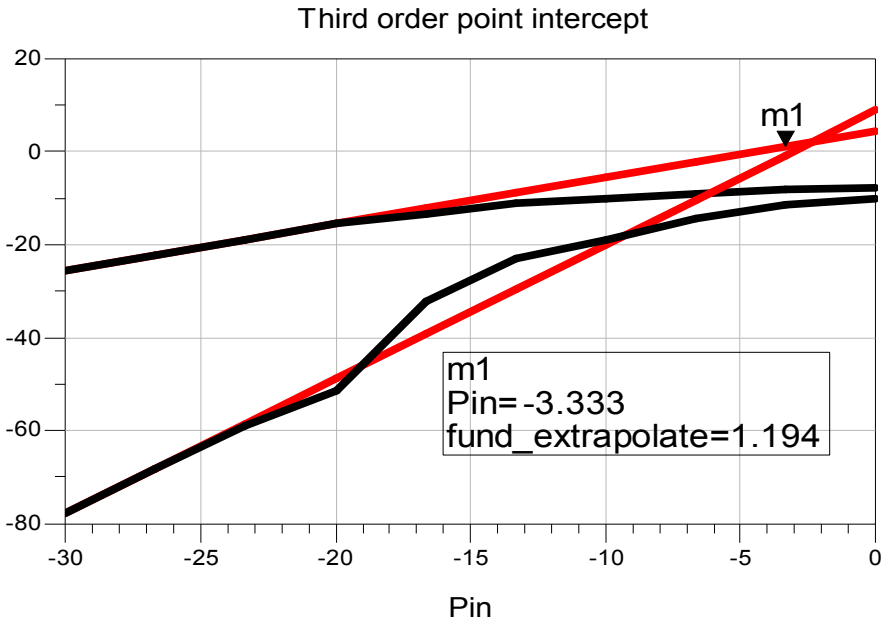


Figure 3.14 Third order incept of IP3 assessment.

The final results in Table 3.2 with single point RF power sweep at -30 dBm showed that compromises has to be taken depending on the primary objective (e.g. gain, linearity , noise figure, etc) of the LNA. It is noted that the results tabulated in the table are somewhat different than the ones shown in the figures above. However, the tradeoffs between the different topologies still exist. In this design a two-stage LNA with notch filter out performed the single-stage without notch filter in terms of linearity and power gain (G_T) only with the compromise of slight degradation on the noise figure (NF).

Parameter (*BFR520_19921214)*	Two-stage (Notch filter)	Single-stage (no Notch filter)	Units
Center frequency	2.68	2.68	GHz
NF	1.3	0.66	dB
|S11|	-6.9	-13.4	dB
|S22|	-4.78	-30	dB

|S12|	-10.54	-6.50	dB
G_T	4.55	4.0	dB
Input VSWR	2.66	1.54	N/A
IP1	≈-15	≈-18	dBm
IIP3	≈-5	≈-9.8	dBm
Power consumption	≈4.25	≈2.12	mW

Table 3.2 LNA simulation performance at 2.68 GHz.

Moreover, for single-stage LNA, the output return loss (e.g. |S22|) is better than input return loss (e.g. |S11|) as the output is matched to a high G_T and the input is mismatched to give a relatively low NF and good input VSWR. To remedy this problem, an isolator can be placed in front of the LNA to compromise for higher noise figure.

Before moving onto the circuit layout, a more accurate simulation must be carried out. The two-stage LNA with real off-the-shelf passive elements and edge discontinuities modeling are shown in Figure (3.15) with some component values purposely missing due to lack of space.

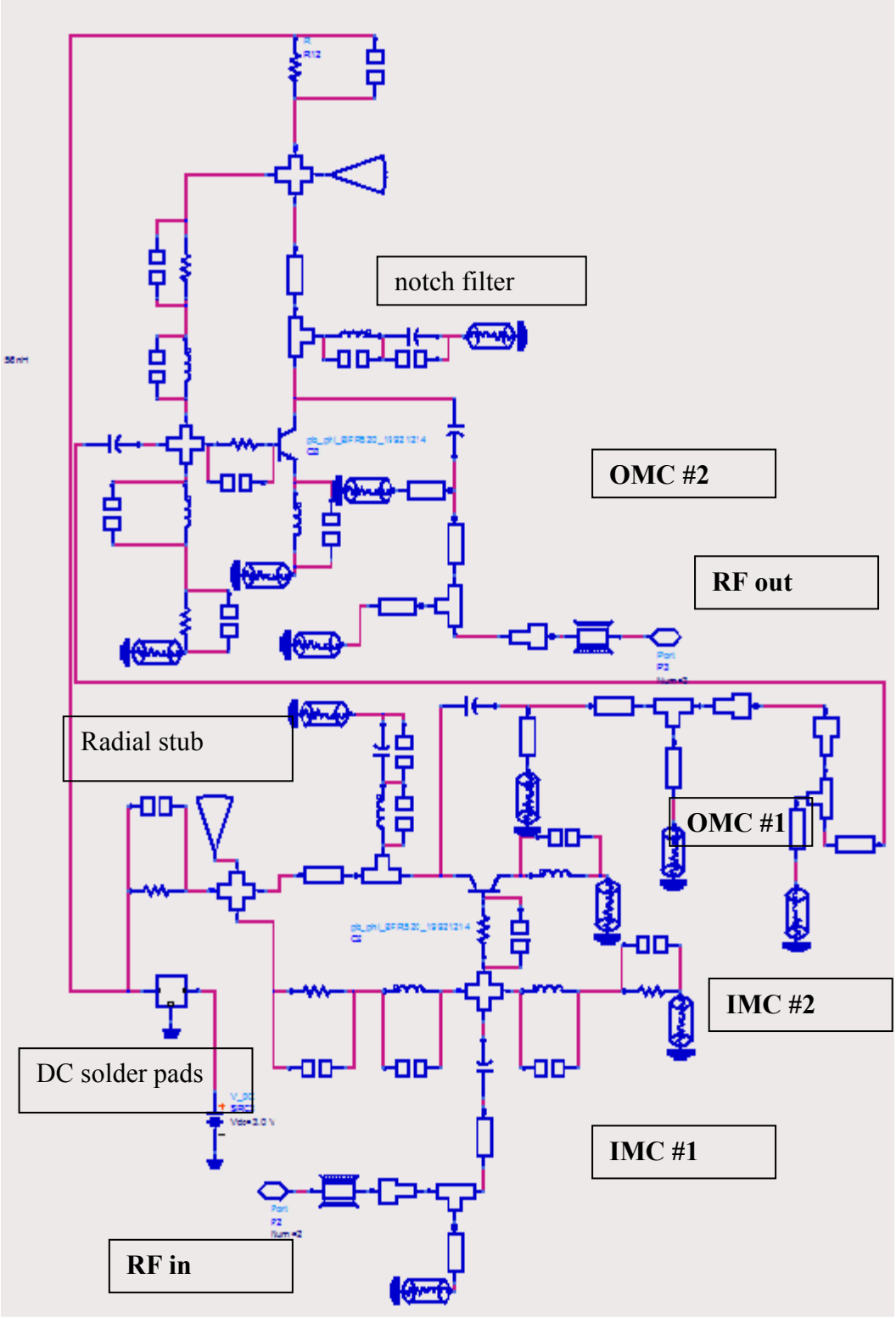


Figure 3.15 Two-stage LNA with notch filter and Emitter degeneration.

With the operating frequency in the range of 2 to 3 GHz, the IMC and OMC are constructed by microstrip lines converted from passive elements using *LineCalc* tool in ADS based on the *Rogers RO4000 series* substrates [32]. Moreover, the radial stub can achieve wider bandwidth short and open circuit effect for the RF and DC signals, respectively. To achieve the opposite, it is possible to combine a quarter-wavelength transmission line at the center operating frequency with a radial stub to obtain open and short circuit effect for RF and DC signals, respectively. The inductor in the Emitter junction chokes any RF signal and the capacitor shorts out any RF leakage through the inductor. To obtain higher simulation accuracies, the microstrip interconnecting patches, component solder pads, related microstrip width discontinuities, and stubs edge effects can also be included in the circuit [33-35]. Moreover, the grounded co-planar (CPW) transmission line, which can offer higher Q than conventional microstrip by adjusting its width and reduce substrate interaction, is added at the input and output signal path of the circuit.

3.3 Intermediate Frequency Power Amplifier

In this work, class–A high gain amplifiers operating at the intermediate frequency (IF) utilizing both conjugate matching and power matching are designed. Since one provides maximum power gain and the other shows maximum power transfer, thus two different approaches should be taken into considerations depending on the purpose of the amplifier.

3.3.1 Class-A PA Operation

In this work class-A PA with maximum power transfer utilizing load-pull method is introduced. Class-A operation is defined as 360^o conduction angle of the signal, which means the transistors in the amplifier is turned ON 100% of the time in the input signal period. Having the correct bias point should give an output voltage swing of V_{max} to V_{knee} with output current swing of I_{max} to zero theoretically shown in Figure 3.16 (a).

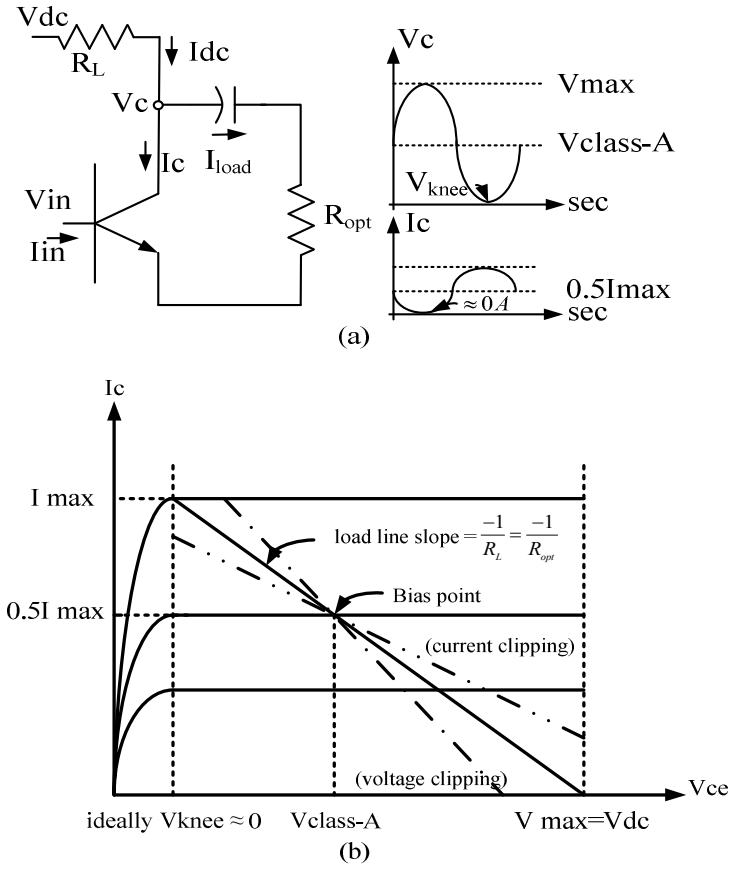


Figure 3.16 (a) Class-A signal conduction (b) and corresponding bias point.

For simplicity, an ideal transistor would present a loadline as a straight line instead of an ellipse assuming it is an ideal voltage (or current) control current source with no parasitic elements. Moreover, an ideal non-linear transistor model would give a

V_{knee} of zero. However, this is rarely the case in reality. In reality, the V_{knee} comes from the physical behavior of the transistor. The voltage $V_{class\text{-}A}$ is located approximately in the midway between V_{max} and V_{knee}. The V_{max}, chosen by the designer, has to be lower than the maximum allowable Collector voltage of the transistor. The a-priori value of R_L can be obtained from Equation (3.10), which is roughly a starting point of finding R_{opt}. This is when load-pull method comes into play to find a more accurate R_{opt} .

$$R_L = \frac{V_{\max} - V_{knee}}{\mathrm{I}_{max}} \approx R_{\mathrm{opt}} \tag{3.10}$$

Knowing the location of $V_{class\text{-}A}$ does not guarantee class-A operation. There are three load lines with different slopes shown in Figure 3.16 (b). In order to avoid clipping in either voltage or current waveform at the output of the transistor, the ideal load line should coincide coordinates (V_{knee}, I_{max}), ($V_{class\text{-}A}$, $0.5I_{max}$), and (V_{max}, 0). Therefore, the value of R_L needs to be iterated to make sure the load-line intersects with all three points.

Aside from the power gain or power transfer, a PA must also be low on power consumption and convert as much of the DC power drawn into usable RF power. Therefore, efficiency or power added efficiency (PAE) needs to be defined. PAE, which is the ratio of output power (Pout) minus the dissipated DC power (Pdc) fed by the DC voltage source over the available input power (Pin), is illustrated shown from Equation (3.11) to (3.14).

$$Pout = 0.5 \times Iload^2 \times R_{opt} \tag{3.11}$$

$$Pin = 0.5 \times re(Iin \times conj(Vin)) \tag{3.12}$$

$$Pdc = Idc \times Vdc \tag{3.13}$$

$$PAE(\%) = (Pout - Pin) / Pdc \leq 50\% \tag{3.14}$$

Theoretically, class-A operation can support maximum 50% PAE only if substantial nonlinearity is acceptable. However, this contradicts the general principle of class-A linear PA, leading to efficiencies of less than 40% in real design [36].

3.3.2 Class-A PA Simulation

3.3.2.1 Load Reflection Coefficient Sweep

After obtaining the vicinity of the optimum load, R_{opt}, one would need to undergo a more sophisticated load reflection coefficient sweeping on the Smith Chart. The Smith Chart is essentially a circle with a radius of one as shown in Figure (3.17) .

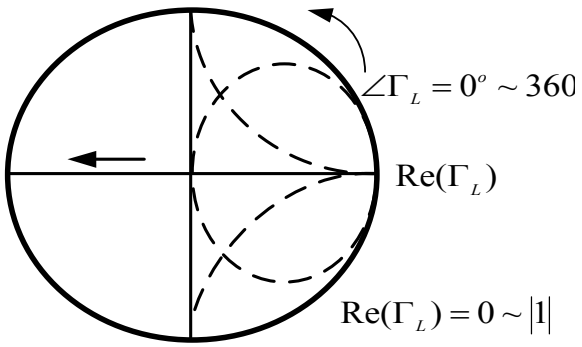


Figure 3.17 Load reflection coefficient sweeping for optimum load on Smith Chart

Therefore, in this work a two-dimensional magnitude (0 to 1) and phase (0 ^{o} to 360^{o}) sweeping of load reflection coefficients is initiated for the fundamental frequency of 430 MHz using the *Harmonic Balance* and *Parameter Sweep* simulation blocks provided by ADS. In this design, the contour of constant power at fundamental and harmonics frequencies as well as constant PAE contours are calculated and plot on Smith Chart for every load reflection coefficient swept.

3.3.2.2 DC Bias and Load-Pull Simulation

In this PA design, a silicon based NPN common emitter transistor BFR-92A with transition frequency (f_t) of 6 GHz manufactured by Philips is chosen for the ability of handling high DC voltage ratings at the CE terminal of the transistor. The maximum voltage and current at Collector junction are chosen to be 8V and 70mA, respectively, for safely operating under absolute maximum ratings [37]. The knee voltage is found to be approximately 0.7V. Therefore, the R_L would be roughly 120Ω. The DC bias circuit is shown in Figure (3.18) with roughly V_{CE}=3.5V and I_C=39.8mA as well as utilizing negative feedback to initiate class-A operation for the same reason as LNA design explained previously. It is possible to roughly estimate the output power by recalling Equation 3.14 before starting the simulation. Having the dissipated DC power of roughly 139.3mV, the output power should not exceed 69.7mW (i.e. 18.4dBm) for class-A maximum efficiency of 50%.

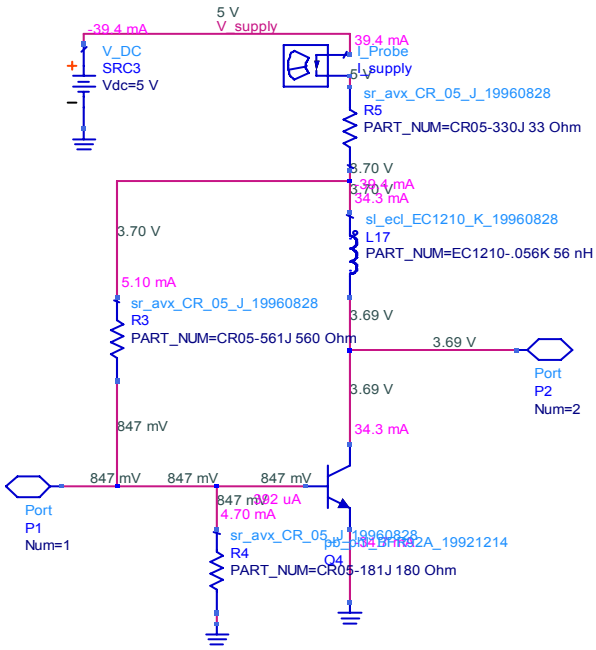


Figure 3.18 DC bias for Class-A PA.

In the simplest form, load-pull measurement indicates certain functional relationship between output powers, PAE and the calibrated output match [36, 38]. In this design, finding the optimum load impedance will be our primary goal for maximum power transfer to the load given the PA driving in the linear region. In the simulation, the source and load impedances are set to 50Ω from 430 MHz to 5th harmonics frequencies.

Recalling Equation (3.11) and (3.14) the outpour power at both PA fundamental and harmonics frequency as well as PAE can be calculated. Moreover, using the macro command of *contour* and *indep* will allow plotting constant fundamental and harmonics powers as well as PAE contours on the Smith Chart illustrated in Figure (3.19), by indexing the corresponding matrix to the desired frequency. It is worthy to mention that it is highly desirable to have larger fundamental power contour shown on the Smith chart, as this means that the power transfer ability of a PA is less susceptible to the change of Γ_L presented to the load. Therefore, this indicates that the load-line matched PA is an ideal

buffer that minimizes the impact on the PA coming from the proceeding devices in the receiver simulation.

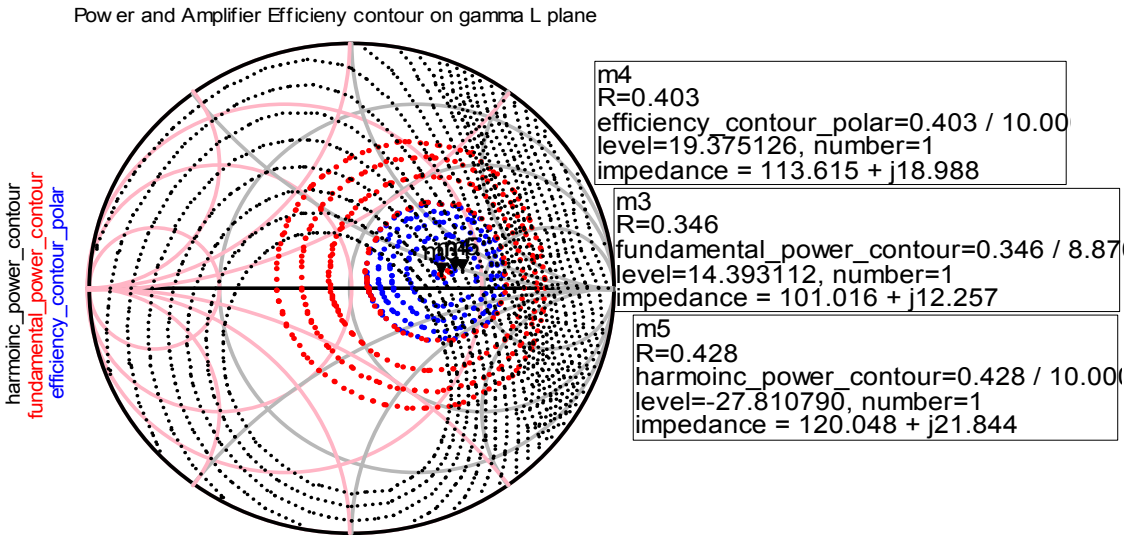


Figure 3.19 Power and PAE contour on Γ_L plane given available power of -4 dBm.

Refer to Table 3.3 as well as marker 3 and 5 (m3, m5) in Figure (3.19) , one can see the PA can deliver roughly 14.4 dBm (i.e. 27.5mV) at 430 MHz. In addition, the difference of the output power at fundamental frequency (430 MHz) and its harmonics, which is averaged from 2nd to 5th harmonics, is approximately 41 dB. With the significant difference, one can assume the amplifier is operating in linear mode (class-A) [36].

Parameter (BFR-92A)	Value	Units
Power at 430 MHz	14.4	dBm
Power at harmonics (Averaged)	-27.8	dBm
PAE	19.3	%

Table 3.3 Amplifier fundamental and harmonics output power and PAE.

Moreover, the dotted contour represent the amplifier PAE (m4 in Figure 3.19) with respect to different load reflection coefficients. From the theory of power amplifier,

once non-linear distortion sets in, the maximum power transferred at the fundamental frequency (i.e. 430 MHz) will cease to increase. Increasing the available power from the input to the amplifier will only convert power at the harmonics (860 MHz and so on).

Also, it is worthy to note that the larger the fundamental frequency output power contour the less sensitive the PA is to the load impedance. The PA can deliver constant power to a wide range of load with little change in output power level from its maximum. In this design, the optimum load of *101.02+j12.26* (or $\Gamma_L = 0.346/8.87^o$) is chosen as it is located near the efficiency contour of *19.38%* (with the highest efficiency of *19.48%)* given the available power of -4 dBm. Moreover, the power at the harmonic frequencies is not a concern as marker 5 (m5) showed that the power contributed by the harmonics frequency (up to 5th) is only around -28.8 dBm. After choosing the Γ_L, the conjugate matching at the input can be performed as shown in Figure (3.20) with the output matched to $\Gamma_L = 0.346/8.87^o$. One point worth noting is that pi-matching is chosen as it serves both purposes of wider bandwidth matching, low-pass filtering, and attenuations for harmonics generated by transconductive non-linearities for the PA.

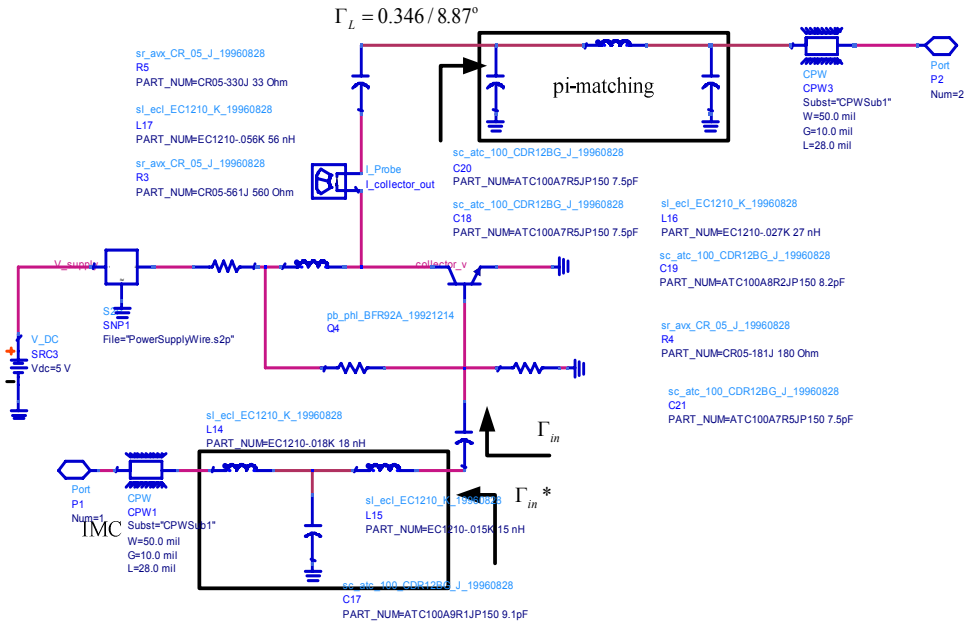


Figure 3.20 Raw PA circuit with input conjugate match and output load-line match.

The circuit shown in Figure (3.20) is inserted under *one-tone harmonic balance* and *two-tone harmonic balance* template in ADS to verify the initial simulation. There are few valuable outcomes worth mentioning. The current and voltage waveform shown in Figure (3.21) indicates the DUT under conditions of sinusoidal excitation and optimum loading.

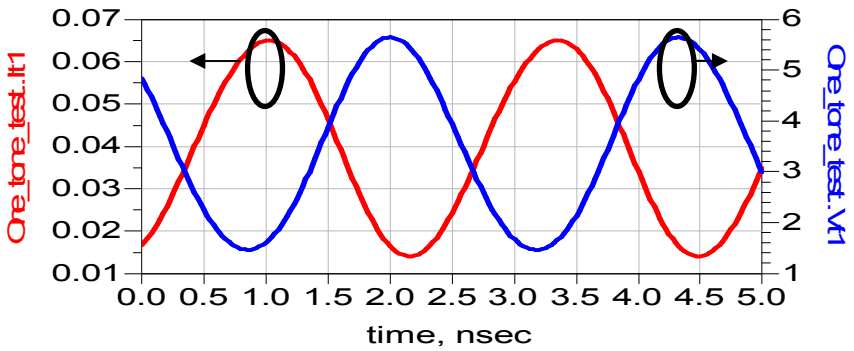


Figure 3.21 Class-A output voltage (right-Y) and current (left-Y) waveform.

Comparing the amplifier output voltage and current waveform in Figure (3.21) to class-A signal conduction shown in Figure (3.16), the voltage waveform swings from

V_{knee} to $2V_{DC}$ while the current waveform shows 360° conduction angle with peak-peak amplitude of I_{max}.

3.3.2.3 Large-Signal Simulation

In the large-signal simulation, the G_T and PAE of both conjugate and load-line matching with off-the-shelf passive components are compared in Figure (3.22) . The load-line matching is found to be slightly more linear than conjugate matching with the transducer gain (power gain) of approximately 18.6 dB and the IP1dB of approximately -1 dBm. The PAE of the class-A PA shows that the PAE obtained is roughly 14% with available RF power of -4 dBm. In addition, the maximum PAE is roughly 22.5% without being driven into compression region (i.e. Pa_dbm < -1dBm), which deviates from the theoretical maximum PAE of 50% for class-A operation.

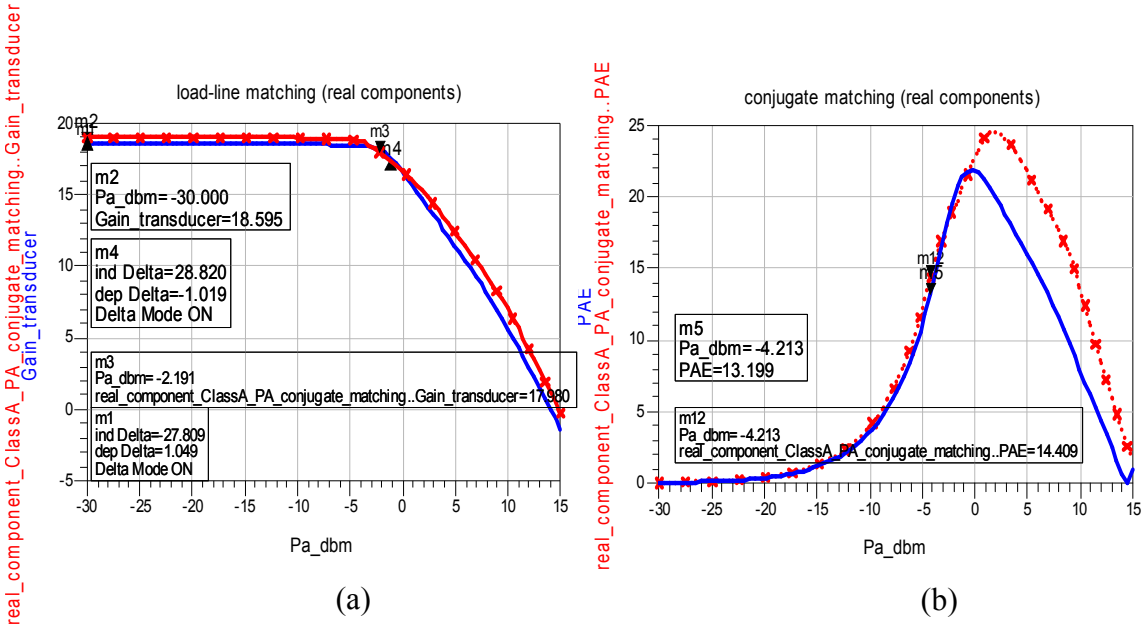


Figure 3.22 (a) G_T and (b) PAE vs. available power with load-line and conj. matching.

In order to obtain third order intercept point (TOI) the two-tone test is performed with f1=432.5 MHz and f2=427.5 MHz setting the tone separation of 5 MHz. The TOI is

defined by the intersection of extrapolating the output power curves of both fundamental (f1) and third order (2f1-f2) frequencies shown in Figure (3.23).

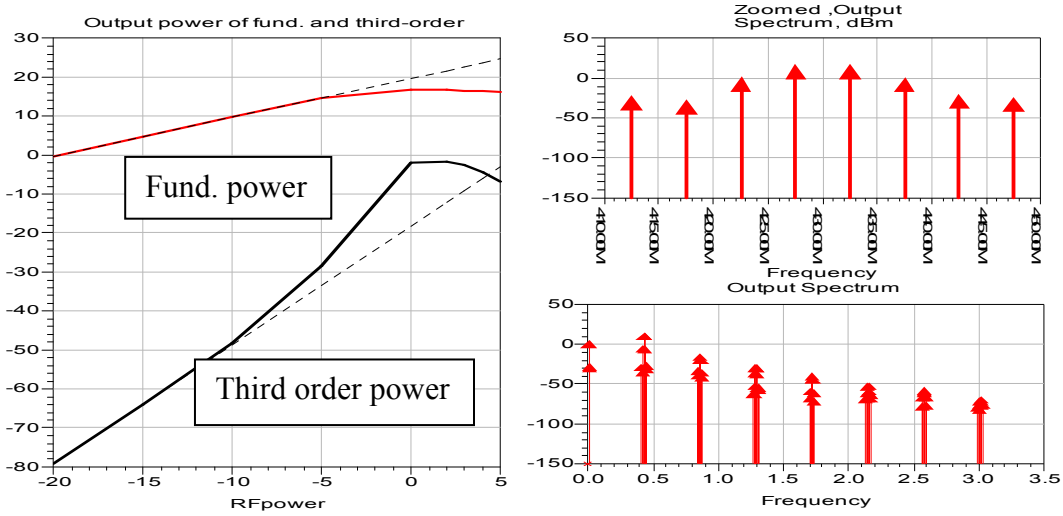


Figure 3.23 Output power and spectra.

However, the power sweep in this design did not converge, therefore the IIP3 and OIP3 are obtained by approximating the output voltage spectrum. During the simulation the third order tone of intermodulation was found not only contributed by the two fundamental tones (i.e. f1 and f2), but also the higher order terms (i.e. 5^{th} order) of intermodulation distortions. The output power spectrum in Figure (3.24) is driven by available power within the compression region. Assuming the PA operates in linear region, the IIP3 can be approximated to be roughly 13.5 dBm.

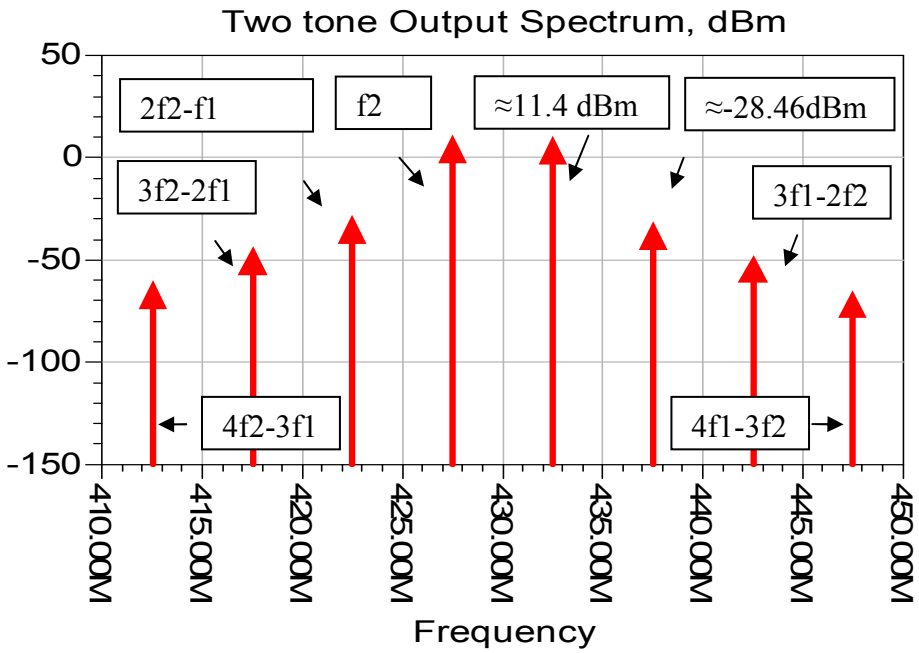


Figure 3.24 Spectrum of two-tone IMD (f1=432.5 MHz and f2=427.5 MHz).

The comparison of circuit performance between load-line match and conjugate match is shown in Table 3.4. It is shown that the load-lone match is able to achieve higher linear performance (e.g. high P1dB) while slightly degrading on the power gain and S22. The results are close to that of obtained by [36]. Similar to LNA, the performance tradeoffs should be considered when it comes to choosing the appropriate design technique for the desired outcome in the design process.

Parameter (BFR-92A)	Load-line match	Conjugate match	Unit
Frequency	430	430	MHz
R_{opt}	101.02+j12.26	51.41+j22.02	Ω
G_T	19.50	20.60	dB
IP1dB	-1.02	-2.2	dBm

IIP3	13.50	8.50	dBm
Noise figure (P_{in} of -2dBm)	4.95	3.07	dB
PAE (P_{in} of -2dBm)	19.03	19.05	%
Power consumption	≈126.57	≈126.57	mW

Table 3.4 Class-A PA parameter with load-line vs. conjugate match.

3.4 Summary

In this chapter, the design of the both LNA and PA placed in the receiver chain has been presented. Also, several performance tradeoffs are considered depending on the primary objective of the active devices. In the system-level receiver simulation, a two-stage LNA and PA consisted of conjugate match and load-line match will be implemented. In the next chapter, the double balanced active mixer, which is also an important part of the receiver design, will be discussed in detail.

Chapter 4

Mixer Design and Implementation

Modern superheterodyne receiver consists of several components down the chain including the mixer, which performs frequency transformation (upconversion or downconversion) from mixing the two input frequencies to provide output frequencies. Other than low power consumption, the modern communication equipments are designed to be high gain and high linearity. Among all the requirements, high linearity is the most difficult to achieve since the mixer is required to operate at low supply voltage and power consumption. Linear mixer circuit has been widely adopted in modern mixer design to reduce adjacent channel interferences and other types of possible interferences between various communication standards (e.g. IS-95 and WiMAX).

In the mixer design, the highest linearity would be the primary objective with optimum gain to be secondary as the power amplifiers in the receiver chain can compensate for it. In terms of noise figure, it can be minimized by carefully choosing the transistor in the mixer [1].

Among many proposed active mixers, the doubled-balanced fully differential mixer (e.g. Gilbert mixer) has been widely adopted since it can achieve good port-to-port isolation and rejection of even-order spurious responses, thus, providing the minimum power level at undesired frequencies at the output [1]. The differential pair topology of

the Gilbert mixer is the most adopted used building block in analog integrated circuit design given it is less sensitive to noise and interference (i.e. large common mode rejection ratio) than single-ended circuits. In this chapter, first the mixer fundamentals are discussed and different mixers available. Then, because of the advantages of double balanced mixer, we are going to use this type of mixer for design and simulation.

4.1 Mixer Fundamentals

Mixer is a non-linear device , which mixes the incoming radio-frequency (RF) signal with local oscillator (LO) signal and produces another signal, called "intermediate frequency " (IF) signal. One can refer to Equation (4.1) as the basic mixer operation [1,3]. The multiplication of both RF and LO in time domain will present frequency shifting in the frequency domain at IF port, which is at $|\omega_{RF} \pm \omega_{LO}|$.

$$\begin{aligned} & A_{RF}\cos\omega_{RF}t \times A_{LO}\cos\omega_{LO}t \\ &= \frac{A_{RF}A_{LO}}{2}\left[\cos\left(\omega_{RF}+\omega_{LO}\right)t+\cos\left(\omega_{RF}-\omega_{LO}\right)t\right] \\ &= \frac{A_{IF}}{2}\left[\cos\left(\omega_{RF}+\omega_{LO}\right)t+\cos\left(\omega_{RF}-\omega_{LO}\right)t\right] \end{aligned} \tag{4.1}$$

Depending on mixer up or downconversion operations, either frequency at $|\omega_{RF}+\omega_{LO}|$ or $|\omega_{RF}-\omega_{LO}|$ is desired, respectively.

4.1.1 Multiplier Mixer

Theoretically, active mixer operation shown in Figure (4.1) utilizes a square wave LO input signal with ideally 50% duty cycle. Ideal square wave signal has only odd harmonics with decreasing amplitudes, which is used to create frequency shifting by multiplying with the incoming RF signal. In this work, LO signal is a high frequency sinusoidal signal, which has a very steep slope, resembling a square wave signal.

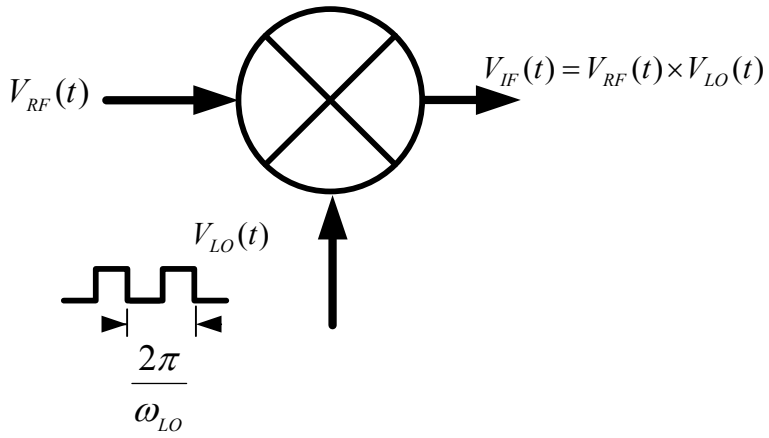


Figure 4.1 Active mixing operation.

Referring from Equations (4.2) to (4.5), the IF signal is produced by RF and LO signal multiplication and convolution in time and frequency domain, respectively. In frequency domain the IF output consists of several frequency components of $V_{RF}(f)$ vertically scaled by nf_{LO} as shown below [1, 3].

$$V_{RF}(t) = V_{RF}\cos(\omega_{RF}t) \tag{4.2}$$

$$V_{LO}(t) = \frac{4}{\pi}[(\cos(\omega_{LO}t) - \frac{\cos(3\omega_{LO}t)}{3} + \frac{\cos(5\omega_{LO}t)}{5} - ...] \tag{4.3}$$

$$
\begin{aligned}
V_{IF}(t) &= V_{RF}(t) \times V_{LO}(t) \\
&= \frac{2V_{RF}}{\pi}[(\cos(\omega_{diff}t) - \frac{\cos(\omega_{3.diff}t)}{3} + \frac{\cos(\omega_{5.diff}t)}{5} - ...] + \\
&\quad \frac{2V_{RF}}{\pi}[(\cos(\omega_{sum}t) - \frac{\cos(\omega_{3.sum}t)}{3} + \frac{\cos(\omega_{5.sum}t)}{5} - ...]
\end{aligned} \tag{4.4}
$$

$$
\begin{aligned}
V_{IF}(f) &= V_{RF}(f) * V_{LO}(f) \\
&= \sum_{n=-\infty}^{+\infty} \frac{\sin(n\pi/2)}{n\pi} V_{RF}(f - nf_{LO})
\end{aligned}
$$

where

$$
\begin{aligned}
&\omega_{LO} = 2\pi f_{LO} \\
&\omega_{IF} = \omega_{diff} = |\omega_{RF} - \omega_{LO}| \\
&\omega_{sum} = \omega_{RF} + \omega_{LO} \\
&\omega_{3.diff} = |\omega_{RF} - 3\omega_{LO}| \\
&\omega_{3.sum} = \omega_{RF} + 3\omega_{LO}
\end{aligned} \tag{4.5}
$$

Moreover, the image frequency signal, which resides at the same IF apart from the other side of the LO frequency can be problematic in channelized applications where channels are separated by fixed frequency. To mitigate this problem, a band-select filter can be placed in preceding stages of the receiver. In this receiver design the downconverted IF (i.e.| $\omega_{RF} - \omega_{LO}$ |) is desired, any other frequencies including the unconverted IF (i.e.| $\omega_{RF} + \omega_{LO}$ |) will be attenuated by filtering mechanism as much as possible.

4.1.2 Conversion Gain

Mixer conversion gain can be defined as the ratio of IF output to RF input. Recalling Equation (4.1) the conversion gain can be defined as half of the LO amplitude

(i.e. 0.5 A_{IF}). In this design both voltage and power conversion gains are considered. The voltage conversion gain is defined as the ratio of root mean square signal voltage at the output port to the root mean square signal voltage at the input port. The power conversion gain is defined as the power at the IF port to the available power driving the RF port. The voltage definition of conversion gain is less meaningful in this design because for Gilbert mixers, transformers/ Baluns are placed at the mixer three ports for balance-unbalance signal conversion, imposing changes to voltage levels while keeping the powers fixed.

Active mixers can often provide conversion gain greater than unity while passive mixers often provide the opposite, sometimes known as conversion loss. However, providing gain in the process of frequency transformation does not improve the sensitivity of the device. Often, the noise figures are also amplified. This makes passive mixer sometimes favored [3].

4.1.3 Linearity

The first downconversion mixer in the chain dominantly determines the receiver selectivity. Linearity performance is critical for mixer as it is often placed after the LNA in the receiver chain. Similar to amplifiers, the 1 dB gain compression (P1dB) point, which indicates upper power limit for an active device to behave in a linear fashion, defines the linearity of mixer.

When two signals with similar power level and in vicinity on the spectrum excite the weakly nonlinear device, mixer, intermodulation distortion can take place and several orders of distortion products can be generated. The third and fifth orders of distortion are

in the designer's interest particularly. Even order distortions are generally well out of band and can be filtered out easily. Figure (4.2) shows that in presence of two-tone input signals the third order of distortion will appear closest to the desired IF spectrum with the separation of Δf. Moreover, not only the lower IF frequencies but also the upper IF frequencies will be generated resulting from IMD under two-tone excitation at the mixer IF port. In this design, a filtering mechanism (i.e. tuned load) will be presented to suppress the effect of upper IF at the mixer IF port.

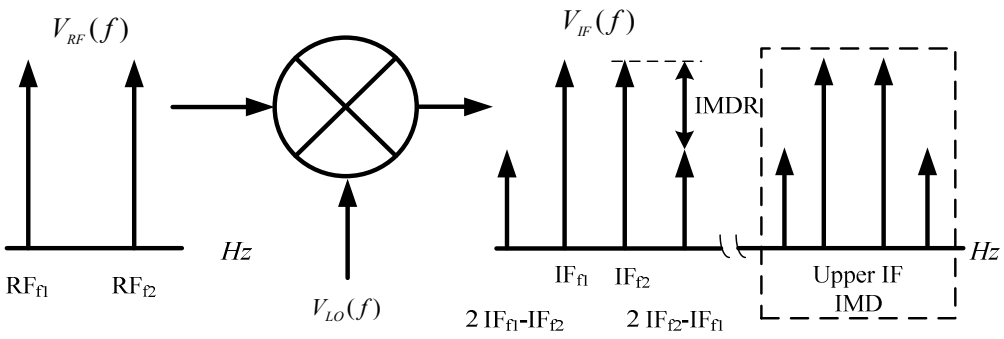


Figure 4.2 Simplified mixer two-tone test signal spectrum.

Another parameter called intermodulation distortion ratio (IMDR) also indicates the mixer linearity, which is the ratio between the desired IF signal and the third order distortion [3,39]. The higher the ratio the more linear the mixer is.

The third order intercept point (TOI) is used to determine linearity of the mixer when excited by two tones from the perspective of the adjacent channels. One should note that different from power amplifiers (PA) the output frequency (IF) may not be near the input frequency (RF) for mixer. It is worthy to note that the higher order distortions can be ignored when operating well below the compression level, but can become the

dominant contributors in the compression and saturation region. Thus, it is desired to obtain the P1dB point before conducting TOI test.

4.1.4 Isolation

Mixer isolation can be a great problem for singly active (e.g. BJT) mixer, the RF and LO feedthrough at the IF port can be significant as well as the reverse LO feedthrough at the RF port due to its' non-differential topology.

In this chapter, the Gilbert mixer is chosen in the receiver design since double-balanced mixer is known for great port isolation performance. The two unwanted feedthrough (i.e. LO to IF, RF to IF) components are reduced by including differential input signals at RF and LO ports.

Both forward and reverse isolations are of concern. The signal power of LO is generally large and it can cause forward feedthrough in the following signal processing components of the receiver. Reverse feedthrough can interfere to other receiver chains. The required isolation levels greatly depend on the environment in which the mixer is utilized.

4.2 Balanced Mixer

The "odd symmetry" response and time variant single-balanced active mixers in Figure (4.3) generally have a gain stage (M1, transconductor), a switching stage (M2/3, switching pair), and a differential IF output. The first stage of this mixer is the RF

transconductor (M1) that contributes to conversion gain and converts the RF signal into an amplified current-only output. Later, the current is sent to differential LO depending on the ON/OFF of M2/3. The load resistors, R_L, at the drain side of M2/3 form a current to voltage transformation. Also, it is worthy to mention that load resistors can also be an active load such as a current source with the tradeoffs of increasing flicker (1/f) noise. The resulting differential IF output is the RF signal multiplied by a square wave at the LO frequency. Thus, this active mixer behaves like a multiplier [40-41].

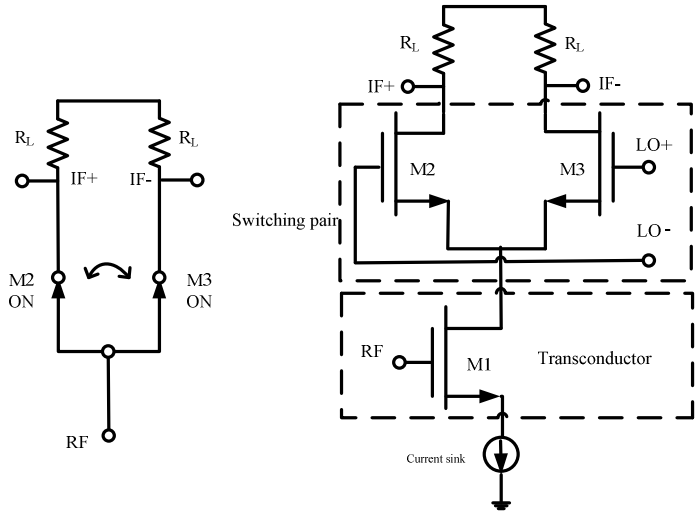


Figure 4.3 Single-balance Mixer.

Differential output at IF is preferred for higher gain and more immunity to RF to IF feedthrough comparing to single ended IF output [3, 41]. The circuit also provides good LO to RF feedthrough, which is depending on the symmetry of the circuit and the differential LO drives. The main drawback of single-balance mixer is high LO to IF feedthrough. That is, the LO signal could leak into the IF if the IF is not much lower than the LO frequency and desensitize the mixer. This can make the filter in the following stage hard to suppress the LO signal without interfering the IF. Also, RF to IF

feedthrough can take place if either the IF port is taken single-ended or LO switching mismatch.

Double-balanced mixers, also called Gilbert mixers are preferred over the single balanced implementations as it greatly attenuates LO-to-IF, and RF-to-IF feedthrough, which can increase linearity. The double-balanced mixer is defined as linear and time variant because it generates frequencies that do not exist in the input signal. Referring to Figure (4.4) the circuit topology is essentially two single-balanced circuits with the RF transistors in parallel and the LO switching pair in anti-parallel.

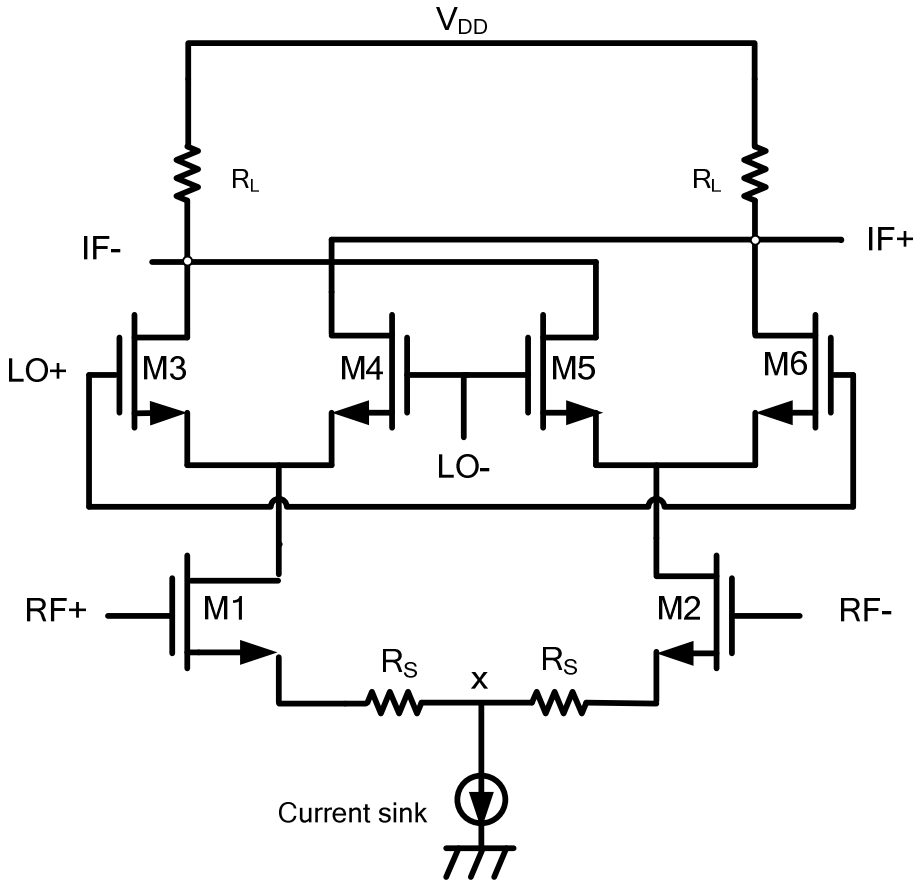


Figure 4.4 Double-balanced Mixer (Gilbert mixer).

The Gilbert mixer is a natural extension of the single-balanced topology. It replaces the common source RF driver stage (M1 in Figure 4.3) with a differential pair (M1 and 2 in Figure 4.4). Referring to Figure (4.5), the LO signal alternately turns on M3/6 shown in Figure 4.5 (a), then M4/5 shown in Figure 4.5 (b) with the arrows showing the direction of small signal RF current. The small RF signal sets the direction of small signal current flow. The IF output magnitude is proportional to RF input, but the IF polarities flip according to the ON and OFF of M3/4/5/6. The IF signal generated by either LO+ controlled transistors are 180 degrees out of phase with respect to the transistors turned ON by LO-. The differential output current of the RF driver stage is then commutated by a four-transistor (switch) drive by the LO. This circuit symmetry cancels both RF and LO signals at the IF output. The LO is also isolated from RF due to symmetry of differential LO, which is a significant advantage.

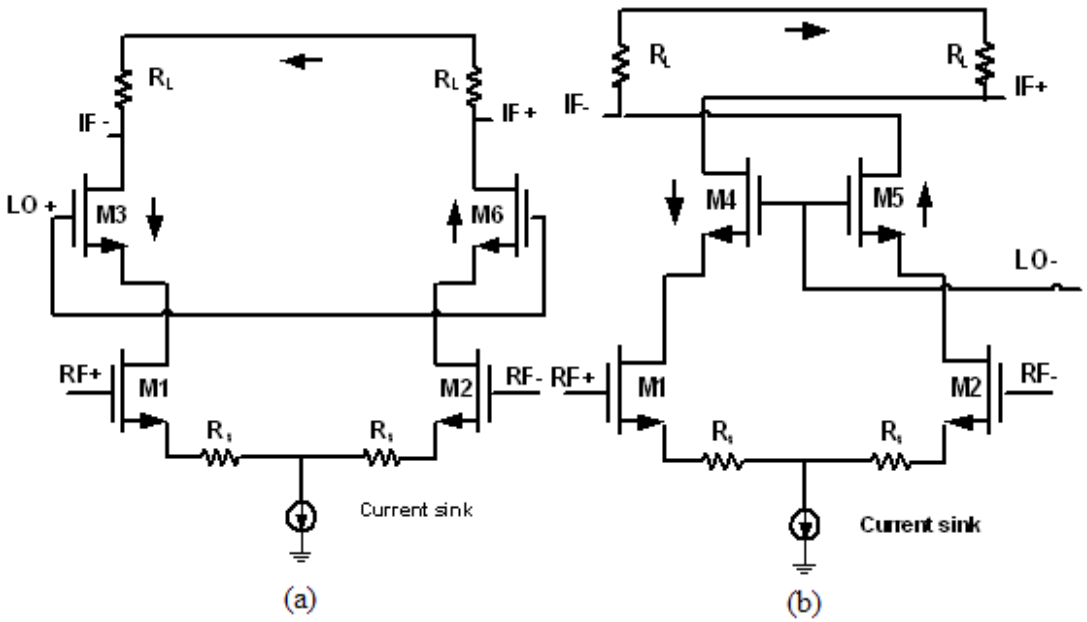


Figure 4.5 Analysis of LO signal alternately commutate between (a) M3/6 and (b) M4/5.

4.3 Design Procedure

In this design, the modeling of the MOSFETs are based on *SPICE3-level 3 0.5um fabrication process* [42]. Simulations based on the sophisticated MOSFET model files allows results obtained from the CAD tool very close to the performance exhibited by the fabricated circuits. The ADS allows importing of the ASCII MOSFET SPICE model file, provided by the user, into netlist using *NETLIST INCLUDE* block under *Data Items*. With the netlist converted, the MOSFETs obtained under *Devices-MOS* can fully exploit the desired transistor model given the correct model instance name is assigned. The default DC biasing curve tracer of the CMOS *SPICE3 0.5um* shown in Figure (4.6) with channel length (L) and width (W) of 2.5um and 100 um. It is seen that with early voltage effect the drain-source current (I_{DS}) is somewhat proportional to drain-source voltage (V_{DS}) while operating the MOSFETs in the saturation region [42].

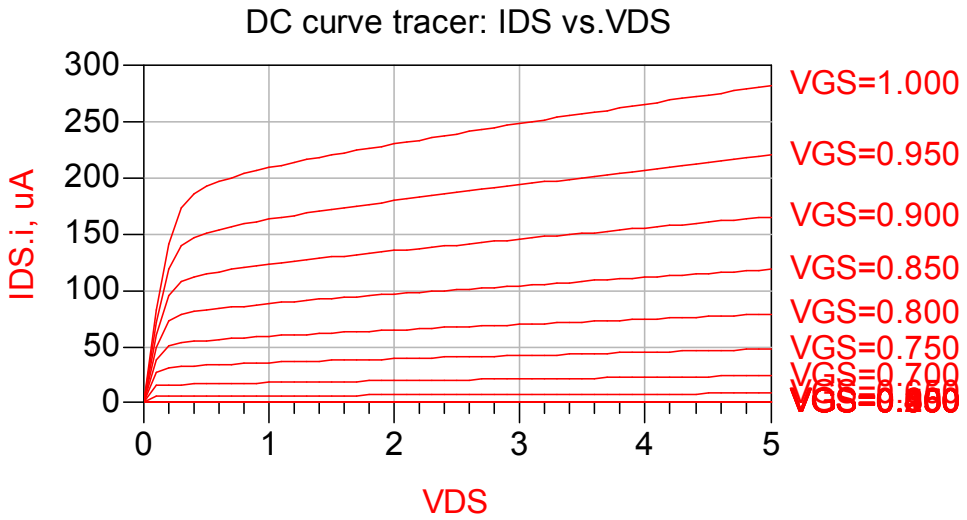


Figure 4.6 DC curve tracer of *FET* IDS vs.VDS.

The partial NMOS process parameters for DC biasing, and ports operating frequency are shown in Table 4.1. The equations for estimating the appropriate DC bias voltage levels will be presented. Also, note that the biasing for the Gilbert mixer with the optimum gain, linearity, and noise figure is an iterative process and should be constantly examined. Moreover, it is observed that there is a built-in redundancy in the SPICE3 MOSFET model parameters. For example, the design can choose to specify k_{nmos} instead of UO and TOX (i.e. $\approx 1.38\times10^{-8}$) separately, and vice versa.

SPICE3 0.5um parameter	value	unit	Port frequency	value	unit
k_{nmos}	56.3	$\mu A/V^2$	LO	2.25	GHz
V_{TO}	0.66	V	RF	2.68	GHz
L_{min}	0.5	μm	Desired IF	430	MHz
UO	456.56	$cm^2/(V\text{-}sec)$			
LAMBDA	0.01	V^{-1}			
PHI	0.7	V			
GAMMA	0.5	$V^{1/2}$			
Cox	2.5×10^{-3}	F/m^2			

Table 4.1 Partial parameters of SPICE3 0.5um CMOS process.

The fundamental equations shown below for modeling the behavior (e.g. DC biasing and conversion gain) of the transistors are referenced from [3, 5]. In saturation region, the MOSFET provides a drain current whose value is independent of the drain

voltage and is determined by the gate voltage roughly obeying the square-law illustrated in Equation (4.7).

$$i_D = \frac{1}{2} k_{nmos} (\frac{W}{L})(v_{GS} - V_t)^2 (1 + \frac{v_{DS}}{V_A}) \tag{4.7}$$

where the L and W are the gate length and width of the channel. The v_{GS} is greater than 0v assuming MOSFET is in enhancement-mode. The k_{nmos}, in the units of $\mu A/V^2$, is the intrinsic transconductance set by the process technology used to fabricate the NMOS transistors. The V_A is the early voltage, which is depended on the process technology and is defined as the inverse of LAMBDA given in Table 4.1. In addition, the threshold voltage, V_t, can vary from different SPICE parameters as it is proportional to PHI and GAMMA.

Assuming an infinite early voltage can lead to a drain current independent of the drain voltage, therefore, the saturated NMOS behaves as an ideal current source whose value is controlled by the difference of gate source voltage (v_{GS}) and threshold voltage (V_t). Moreover, the channel modulation effect can be minimized at the expense of transistor size by assuming three to five times of the minimum channel length (L_{min}) [5]. This provides reasonable starting point for DC biasing. However, channel modulation is important for the short-channel MOSFET, thus, it should be considered in the simulation.

Referring to Equation (4.8) the transconductance, g_m, as a function of k_{nmos}, varies from one CMOS fabrication process to the other. Moreover, the g_m can be adjusted by changing the value of aspect ratio (W/L) and overdrive voltage (i.e. V_{GS}-V_t). The overdrive voltage is a small-signal parameter, which varies with the DC bias of the MOSFET [5].

$$g_m \equiv \frac{i_d}{v_{gs}} = k_{nmos}(\frac{W}{L})(V_{GS} - V_t) \tag{4.8}$$

Note that one can increase the transconductance by increasing the overdrive voltage with the expense of reducing the allowable voltage swing at the drain. In addition, one can obtain larger transconductance by increasing the aspect ratio.

4.3.1 Differential RF stage

The first stage in a balanced Gilbert mixer is the source-coupled pair transconductance stage driving the RF signal. The design of the mixer is mostly focusing on linearization, which is dominantly determined by the design in the differential RF stage. The linearity of MOSFET can be improved by maintaining its' quiescent (Q) point stability. The instability of quiescent point and transconductance can be reduced by placing source degeneration resistors in the circuit at the expense of noise figure and conversion gain [1]. The Equation (4.9) indicates the ratio of gate source voltage (v_{gs}) and input small-signal voltage (vi) which is equal to the inverse of $1+g_mR_s$ representing the amount of negative feedback, where g_m is the transconductance of the transistor.

$$\frac{v_{gs}}{v_i} \approx \frac{1}{1+g_mR_s} \approx \frac{1}{1+g_m\left(2\pi f_{LO}L_s\right)} \tag{4.9}$$

Moreover, one can choose between source degeneration resistor (R_s) and inductor (L_S) to control the magnitude of the signal, v_{gs}, and make sure that the NMOS transistor stays in linear operation region (i.e. $v_{gs} << 2V_{OV}$).

The thermal noise and DC voltage drop caused by R_s can be eliminated by replacing it with degeneration inductance, L_S, to inductively degenerate the differential RF stage. Therefore, a larger load resistor can be placed to increase the conversion gain at the expense thermal noise. Also, since the inductor is frequency dependent it can place an impact on the input impedance of the mixer and contribute to circuit instability, therefore fine tuning on the Ls will be needed. Furthermore, inductors on CMOS circuits have low quality factor thus forming a parasitic resistance in series with the inductor.

The conversion gain (voltage gain) of the Gilbert mixer with source degeneration is defined in Equation (4.10) as follows [2],

$$G_{conv.} \approx \frac{2}{\pi} \frac{R_L}{(R_s + \frac{1}{g_m})} \approx \frac{2}{\pi} \frac{R_L}{(j\omega L_S + \frac{1}{g_m})} \tag{4.10}$$

where the $2/\pi$ coefficient comes from signal at the IF port evenly divided between the upper and lower IF frequencies. Also, throughout the simulation , it is noted that increasing R_L can achieve higher conversion gain, however, the thermal noise can significantly increase.

The transistors in the RF stage should be biased in saturation with enough headroom for small signal voltage swing. If one increases the overdrive voltage, V_{OV}, more headroom can be obtained for both gate-source voltage, $v_{GS,}$ and drain current, i_D, swings. Recall Equation (4.8), increasing the overdrive voltage and width of the channel while keeping length constant can increase the RF transconductance (gm). Yet, another useful expression for gm can be obtained as shown in Equation (4.11).

$$g_m \approx \frac{2I_D}{V_{GS}-V_t} = \frac{2I_D}{V_{OV}} \approx k_{nmos}\frac{W}{L}V_{OV} \approx \sqrt{2k_{nmos}I_D\frac{W}{L}} \tag{4.11}$$

According to Equation (4.11), given a fixed drain current (bias current), I_D, a higher overdrive voltage will lead to lower RF transconductance, thus decreasing the conversion gain as shown in Equation (4.10). However, better linearity can be achieved [43].

4.3.2 Differential LO stage

The switching LO can be considered as large-signal operation. Non-deal switching, can reduce the conversion gain and increase the noise figure. Ideal switching of the transistors completely turned on and off with sufficient LO power can mitigate the noise problem [3, 39]. According to MOSFET voltage transfer characteristics, increasing ν_{GS} without changing ν_{DS} can lead the transistor into triode region. This is contradicting to the rule of thumb of designing the differential LO stage in the Gilbert mixer, which is keeping the transistors in saturation ($\nu_{DS} \geq \nu_{GS}$-V_T). In order to make sure the transistors can switch between cutoff and saturation region elegantly, V_{GS} should be as close to V_T as possible but the difference cannot be zero. This implies that the aspect ratio (W/L) of LO MOSFET can be relatively large and can lead to the increase of drain and source capacitance. Moreover, with the strong LO signal pumping the circuit, the drain voltage of RF MOSFETs can vary and produce nonlinear transconductance (g_m) [42].

In this work, assuming voltage drop across LO (i.e. v_{DS}) roughly to be equal to 10% of the voltage drop across R_L can be an ideal starting point for finding LO biasing voltages [41- 42]. The Figure (4.7) demonstrates that the gate to source voltage approximately equal to threshold voltage along with sufficient voltage swing can offer proper switching of the transistor pairs.

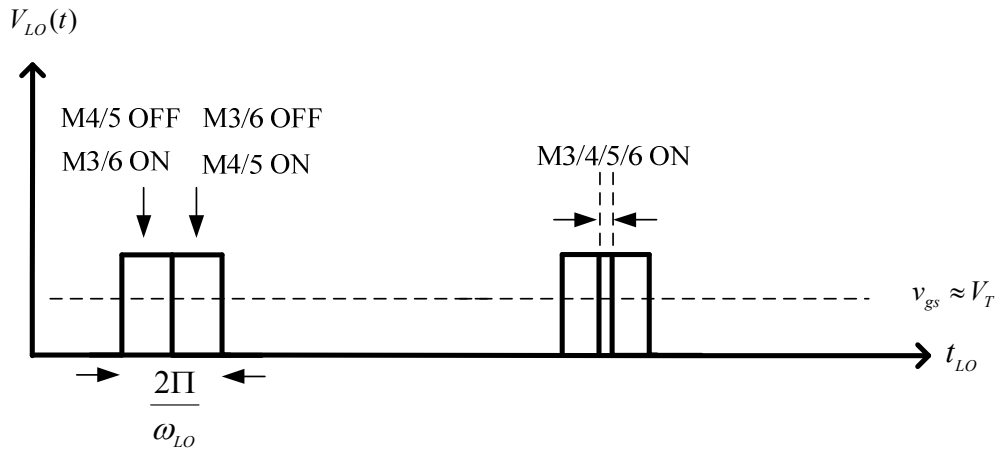


Figure 4.7 Ideal and non-ideal LO switching.

Moreover, it is noted that not only the RF current will be wasted but also the noise will be generated if ON time of two pairs of transistors M3/6 (driven by LO+) and M4/5 (driven by LO-) are overlapped. Minimizing the simultaneous conducting region can reduce the noise contribution in the LO stage.

4.3.3 Current Sink

The current source plays a major role in the IC design. It is often used in biasing the circuit and as an active load. The current mirror implemented in the Gilbert mixer as the biasing circuit has the advantage of generating a stable reference current as well as large output impedance. Therefore, the output current can be balanced even with the single-ended input signal (e.g. RF+= $AsinW_{RF}t$ and RF-=0) being fed to the mixer. This also implies that given the RF input signal is perfectly balanced the current sink/source can be neglected for better linearity. A simplified current mirror is shown in Figure (4.8). It is noted that under ideal differential RF signal excitation, the node x is a virtual signal ground.

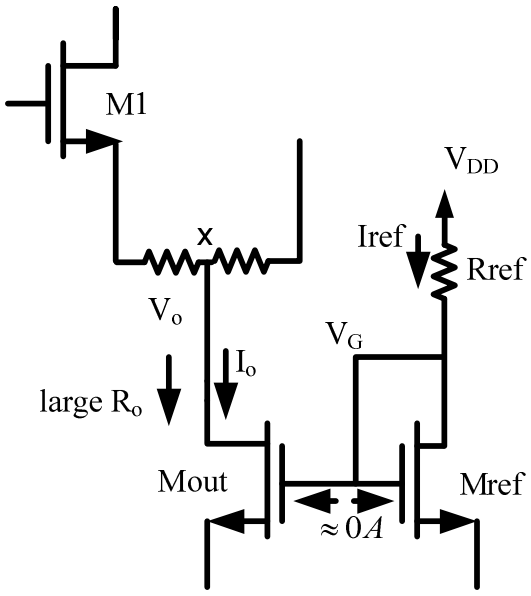


Figure 4.8 Constant current source/sink.

The source and gate end of transistor M_{ref} is shorted thus ensuring that the transistor is always operating in saturation region. According to Equation (4.7),

neglecting channel modulation (i.e. $|V_A|$ approaches infinity) can lead to reference current equal as follows.

$$I_{ref} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Mref}(v_{GS\,ref} - V_t)^2 = \frac{V_{DD} - V_G}{R} \tag{4.12}$$

It is worthwhile to mention that the output resistance, R_o, of the current source/sink equals to small-signal output resistance, $r_{o,Mout}$, which is usually few kilo ohms. Therefore, it is convincing to assume that only negligible amount of the small-signal RF current will enter the current source/sink even under non-ideal differential RF signal excitation. Moreover, cascoding the MOS current mirror (e.g. Wilson current mirror) can lead to a larger R_o and further suppress the current mirror early effect (i.e. larger $|V_A|$) [30].

In order to keep the transistor M_{out} in saturation region, the condition of $V_{ds} \geq V_{gs}$-V_T should still be satisfied. Recall the degeneration resistor (or inductor) from last section. Ideally, having a degeneration inductor will impose neither thermal noise to degrade the noise figure nor voltage drop thus giving higher voltage at the drain of transistor M_{out}. Given gate source voltage of the completely matched transistors M_{out} and M_{ref} are deliberately set equal, it is apparent that adjusting the channel width and length of transistors M_{out} and M_{ref} in Figure (4.8), can modify the current transfer ratio shown in Equation (4.13).

$$\frac{I_o}{I_{ref}} = \frac{(\frac{W}{L})_{Mout}}{(\frac{W}{L})_{Mref}} \tag{4.13}$$

Increasing the reference current, I_{ref}, can increase both conversion gain and linearity of the circuit with the expense of power consumption. The size of MOS will be too large to fabricate if the value of I_{ref} needed exceeds a certain maximum value depending on the process of the MOSFET. To remedy this problem one can connect the source end of each RF transistor to separate current sink/source [5]. However the two current sink/source should be well matched to avoid noise degradation.

When the small-signal input of the differential RF stage is perfectly balanced, the conventional current source/sink may not be necessary. A LC tank circuit shown in Figure (4.9) can replace the conventional current source/sink to achieve higher linearity [44].

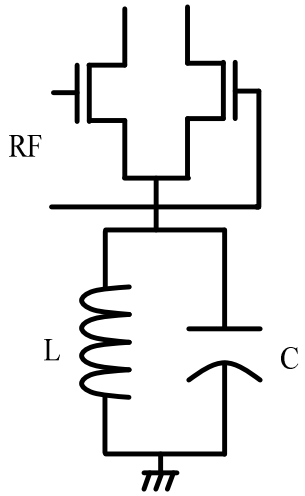


Figure 4.9 Half of the Gilbert mixer with tank circuit.

The inductor shorts the dc bias thus providing path to ground, therefore there are virtually no dc voltage drop across the current source. At resonance, the tank circuit exhibits high impedance to ground, imitating an ac current source [45]. Also, the tank circuit needs to be tuned at the resonance frequency, f_o, to ensure perfect balance at the RF stage fed single-ended or differentially.

4.3.4 Mixer Noise Analysis

The noise figure of the active balance mixer at IF frequency is mainly contributed by the RF stage [46]. A rough expression shown in Equation (4.14) can be used to define the noise of the Gilbert mixer at the IF port.

$$\begin{aligned} Noise_{IF} &= RF + Load + LO \\ &\approx 8kT\gamma g_m R_L^{\,2} + 8kTR_L + 16kT\gamma \frac{I_{bias}}{\pi A_{LO}} R_L^{\,2} \end{aligned} \tag{4.14}$$

The first term, which is the main contributor of the noise expression, is caused by the transconductance (g_m) in the RF-stage. The second term is the thermal noise contributed by the load resistor (R_L). The third term of the noise expression indicates the noise contributed by the LO switch, which depends on the biasing current (I_{bias}) and switching amplitude (A_{LO}).

4.3.5 Tuned Load

Replacing the source degeneration resistance with inductor at source end of both RF stage transistors does not impose DC voltage drop thus increasing headroom for voltage swings. Similar technique is introduced to the load resistance for linearity improvement. A tuned load, which is essentially a notch filter consisting of mixer load resistance, inductor, and capacitor in parallel, can be placed at the drain end of the LO stage transistors. It is noted that DC biasing may need to be slightly altered by placement of the tuned load with the short circuit of the inductor under DC excitation.

The designed Gilbert mixer will generate an upper (i.e. $|\omega_{RF}+\omega_{LO}|$) and lower IF (i.e. $|\omega_{RF}-\omega_{LO}|$) with approximately the same power level at the IF output. In this design, only the lower IF is desired, therefore, the tuned load shown in Figure (4.10) will be designed to attenuate the undesired upper IF (i.e. 4.93 GHz).

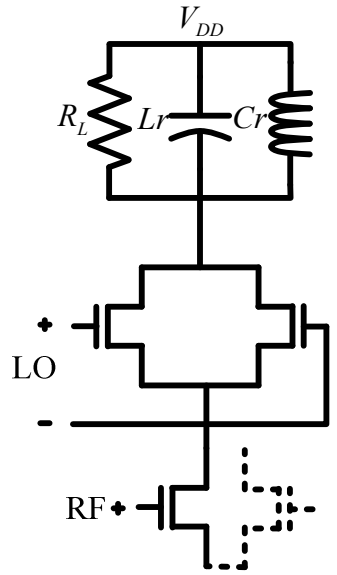


Figure 4.10 Position of tune load in the mixer circuit.

At the undesired upper IF (i.e. 4.93 GHz) the notch filter L_r and C_r will short out the load resistance leading to zero conversion gain of the mixer circuit. The equivalent admittance of the tuned load can be derived in Equation (4.15) as follows.

$$Y = \frac{1}{R_L} + jwC_r + \frac{1}{j2\pi f_r L_r} \tag{4.15}$$

where f_r represents the resonating frequency. At resonance, the imaginary part of equivalent admittance equals to zero, therefore, the resonating frequency shown in Equation (4.16) can be altered by adjusting the value of both L_r and C_r as follows.

$$f_r = \frac{1}{2\pi\sqrt{C_r L_r}} \tag{4.16}$$

4.4 Mixer Simulation

With several iterations incorporating Equations (4.7) to (4.19), the preliminary values of MOSFET sizes and passive elements for the optimum balance between power gain, linearity, and noise figure are shown in Table 4.1 and Figure (4.11). Several modifications can be made to increase the conversion gain, such as replacing the load resistance, R_L, to an active load. This will allow even higher conversion gain without using too much physical space on chip and voltage swing headroom. However, low IF active load can generate significant amount of flicker (1/f) noise that can degrade the

mixer SNR [46]. Moreover, increasing the bias current can improve the mixer conversion gain and linearity and carrying the value of Ls can be chosen to provide optimum noise matching.

Circuit parameter	value	unit	Circuit parameter	value	unit
V_{DD}	2.3	V	L_S	≈2	nH
Channel length (all)	1.6	μm	Lr	14	nH
Channel width M1/2	251	μm	Cr	10	pF
Channel width M3/4/5/6	381	μm	R_L	1000	Ω
I_O	30	mA	V_{SS}	-2.3	V

Table 4.2 Preliminary modeling parameter in the Gilbert mixer.

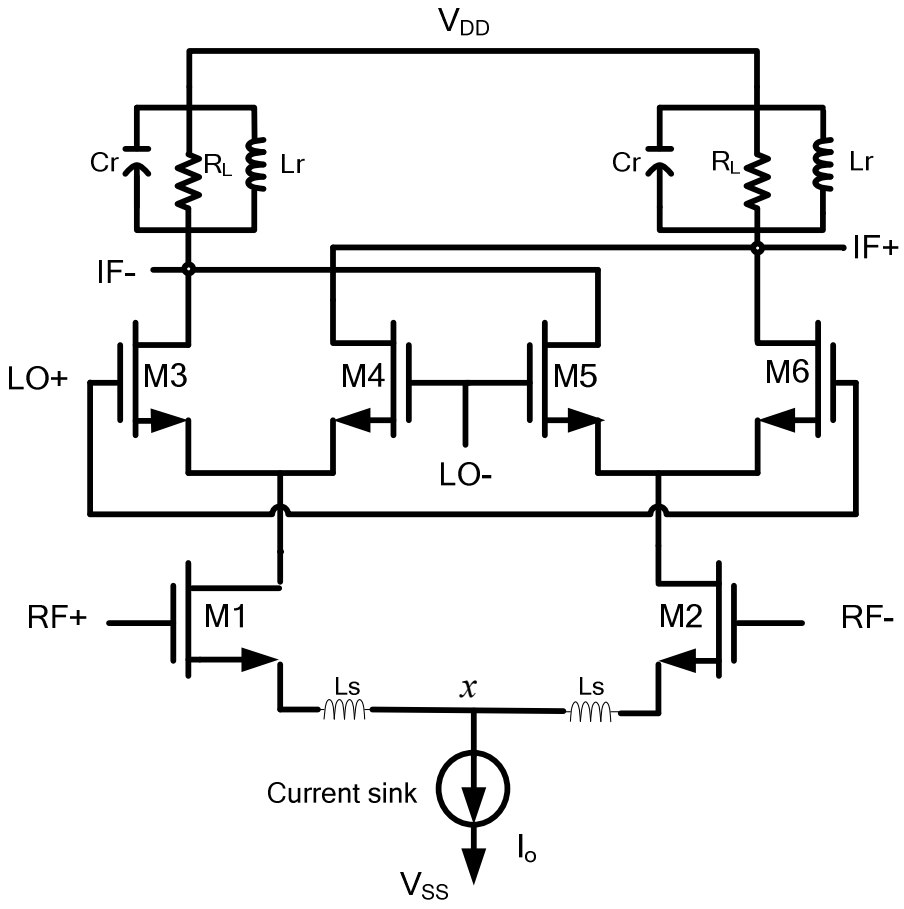


Figure 4.11 Topology of Gilbert mixer implemented.

With the parameter values provided in Table 4.2, the value of transconductance can be approximated as roughly 27.5 mA/V and conversion gain of 22 dB obtained by Equation (4.11) and (4.10), respectively.

During the simulation, most of the efforts are put into finding the best outcome for all the parameters since the trade-offs among gain, noise, linearity, and power dissipation are interdependent. For example, reducing the ratio of channel width and length while increasing the overdrive voltage can cause the gain to drop and the noise will increase with the benefit of improving the linearity. Higher gain and better linearity can be achieved by increasing the drive current through the RF stage, however power

consumption will be increased. In addition, the larger current will drop the voltage headroom especially if resistive loads are used. The larger amount of current through the LO switching stages will require larger LO drive, which is undesired because it is hard to achieve under high LO frequency. The summary of tradeoffs adjusting the circuit parameters are shown below in Table 4.3.

Circuit parameter	Performance summary
Current source/sink	Linearity, conv. gain vs. power consumption
R_S	Linearity vs. conv. gain
L_S	Linearity ,gain , and noise vs. operable frequency range
$(W/L)_{RF}$	Linearity vs. conv. gain
$(W/L)_{LO}$	Power consumption vs. conv. gain
R_L	Thermal noise vs. conv. gain

Table 4.3 Summary of performance tradeoffs.

The frequency of LO is chosen to be lower than RF (i.e. low-side mixer) in order to facilitate the oscillator design. The mixer input impedance has to match to the output impedance of the preceding device while the output impedance is set to match with the input impedance of the proceeding device, which is usually a filter. In the process of simulation, the input impedance is matched to 50Ω for measurements. This is done by terminating the RF port under the S-parameter simulation and measuring the input impedances. The load impedance is designed to be roughly 1000 Ω as it is rarely equal to the general characteristics impedances of 50Ω. Most off-chip passive IF filters operating in megahertz regions have an input impedance of roughly 500 Ω to 1000Ω [3,46].

Therefore, in this design the voltage conversion gain will not equal to power conversion gain. One can refer to Figure (4.12) and understand the basic operation of the Gilbert mixer in this design. The both inputs RF and LO port are driven single-ended and taken differentially by a Balun. As mentioned previously, the LO port should be turning on and off the two mixers in the circuit driven by the IF port differentially and later it is combined back to single-ended output for the component proceeding the mixer. The RF and LO signals taken differentially can provide superior port isolation therefore prevent possible LO leakage and RF feedthrough at the IF port. Moreover, the LO leakage at the RF port can also be minimized.

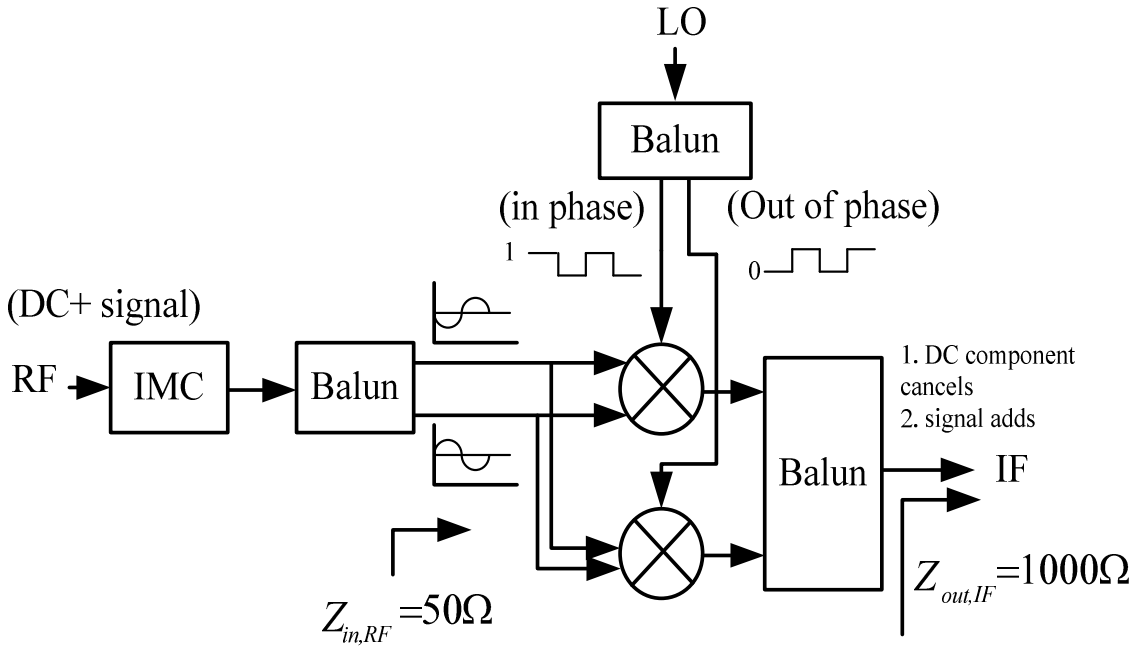


Figure 4.12 Gilbert mixer input/output impedance.

4.5 Mixer Performance

A source coupled Gilbert mixer utilizing tuned load and inductor degeneration is simulated in ADS. In this design, the single side band (SSB) noise figure taken as the appropriate NF since the image band is partially filtered by image reject filter. During the simulation, three major sources contributing the NF are the load resistances, LO and RF MOSFETs. Increasing LO signal amplitude along with increasing the RF MOSFET biasing can help reducing IF thermal noise. It is worthy to mention that the NF obtained is quiet low, this is because the simulation is based on a less accurate mode of SPICE3. More accurate of mixer performance can be provided by BSIM model files [47]. Moreover, one should note that the results in Table 4.4 are obtained by driving the Gilbert mixer with tuned load and inductor degenerations with LO and RF port of 20 dBm and -40 dBm, respectively. Also, note that the power consumption is calculated by multiplying the used current by DC supply voltage.

Parameters	ADS simulation results	unit
Conversion (Power) gain	9.46	dB
Conversion (Voltage) gain	16.63	dB
DC voltage supply	5	V
Noise figure (SSB)	5.78	dB
IP1dB	≈10	dBm
Source impedance	50	Ω

Power consumption	150	mW
Load impedance	1000	Ω
LO power	20	dBm
RF power	-40	dBm

Table 4.4 Simulation results of Gilbert mixer.

4.5.1 Port Transient Response

The RF and LO waveforms in Figure 4.13 (a) and (b) are indicating the periodic signal injected into the mixer for the desired IF signal waveform. One can observe the RF and IF waveform period to be approximately 0.35ns and 0.44ns, respectively. This shows the desired RF and IF frequencies of roughly 2.68 GHz and 2.25 GHz are fed into the mixer.

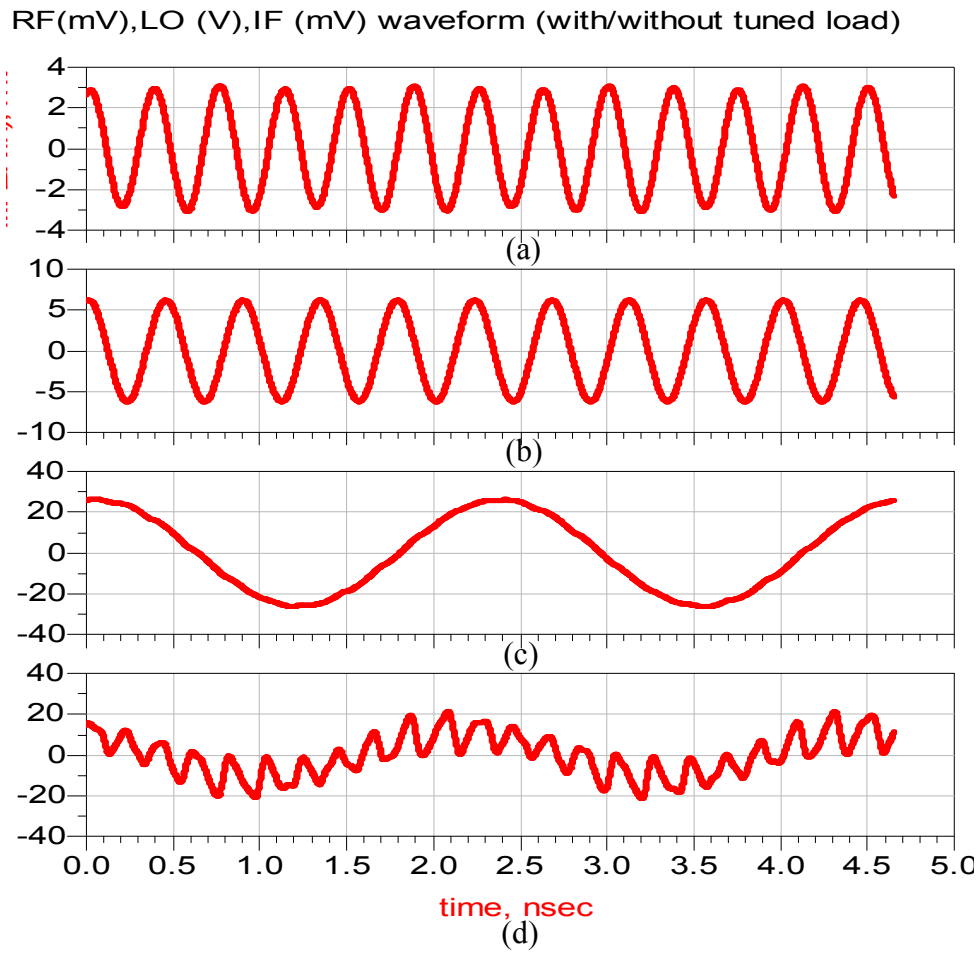


Figure 4.13 (a) RF (mV), (b) LO (V), (c) IF (mV) with tuned load (d) without tuned load.

Moreover, with the placement of appropriate tuned load in the mixer to filter out the undesired upper IF frequency of 4.93 GHz can result in a "clean" IF waveform shown in Figure 4.13 (c) with the period of roughly 2.3ns, which is the desired lower IF of 430 MHz. Moreover, with no placement of the tune load, the IF waveform shows a signal of 430 MHz superimpose another signal of 4.98 GHz.

As shown in Figure (4.14), aside from the unwanted mixer spurs created by the harmonics of RF and LO, the IF port frequency spectrum shows both the lower and upper IF frequencies. The lower IF frequency (desired) at 430 MHz indicated by m1 and the

upper IF frequency (undesired) at 4.93 GHz indicated by m2 is significantly attenuated by roughly 40 dB with tuned-load placed in the mixer. This is desirable as it reduces the power level of the undesired frequencies reflected back from the proceeding channel-select filter.

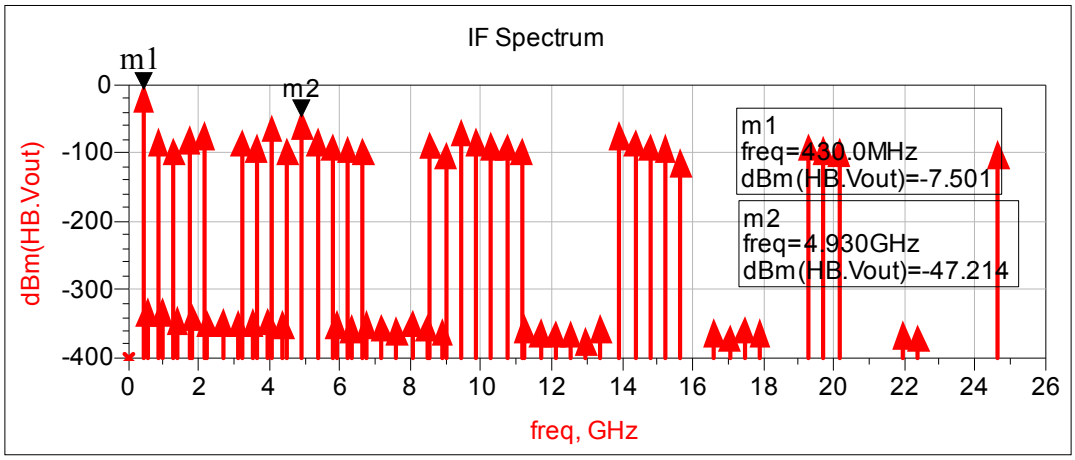


Figure 4.14 Gilbert mixer frequency spectrum of lower IF (m2) and higher IF (m1).

4.5.2 Conversion Gain and Gain Compression

Before the power compression test, the optimum LO power to switch on/off the switching stage should be determined, which is done by simulating the mixer conversion gain as a function of LO power. Degeneration resistance of 2 Ω and 50 Ω along with inductor degeneration 0.6 nH placed in the mixer are simulated. The conversion gain as a function of LO power is shown in Figure (4.15). It is seen that the gain difference between the 2 Ω degeneration resistance and 0.6nH inductor is negligible. For better comparison, an extreme case of degeneration resistance of 50 Ω is also simulated to show significant degradation of gain. However, it is shown later that it provides the highest linearity with the largest P1dB.

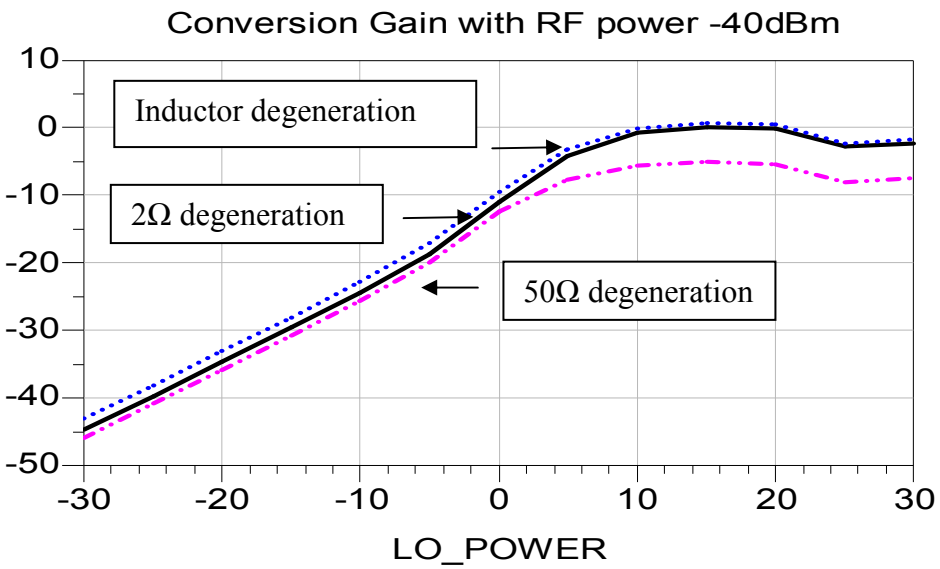
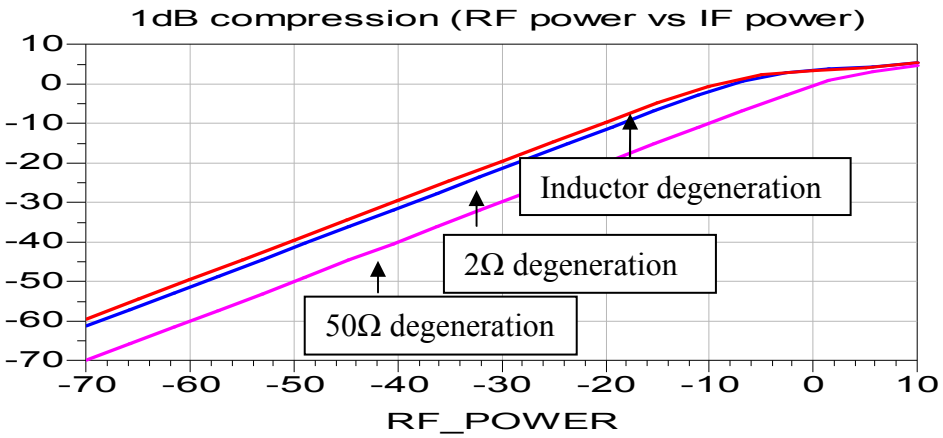


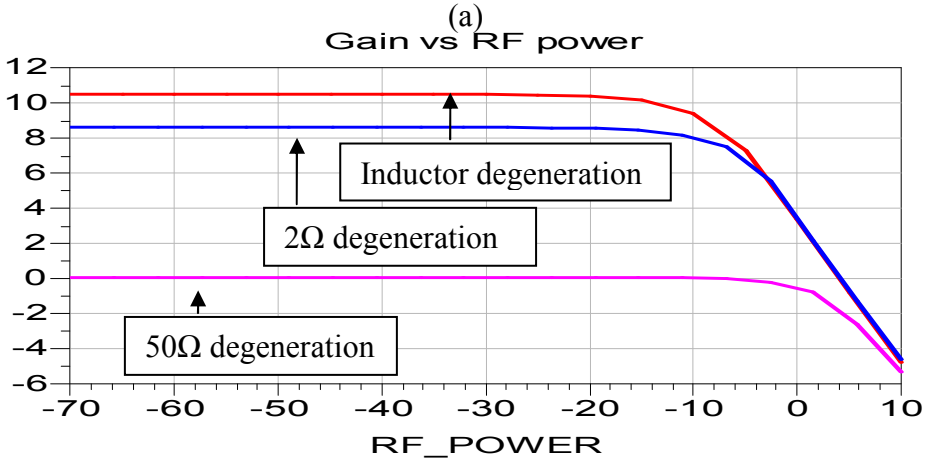
Figure 4.15 Conv. gain (dB) vs. LO Power with different degenerations.

In the mixer design, it is desired to have the IF signal to be directly proportional to the RF signal amplitude. However, in reality this will not be true beyond the physical limit of the circuit. The P1dB point is an indication of circuit dynamic range, which is determined by 1dB deviation of IF power from ideal extrapolated curve. Driving the RF input beyond the P1dB point will cause the mixer gain to deviate from the ideal power curve at IF port.

According to Figure (4.16), one can see the obvious tradeoffs between linearity and gain with the output power and P1dB of 50Ω degeneration intentionally shown. Also, it is seen that the inductor degeneration is able to provide highest conversion gain by sweeping the RF power with roughly the same P1dB as resistor degeneration. Moreover, the degeneration of 50Ω provides higher P1dB roughly of 6 dB comparing to inductor source degeneration with roughly 11 dB gain degradation. It is worthy to mention that the results in Figure (4.16) is to indicate the tradeoffs between gain and linearity. It does not indicate the final P1dB of this mixer design.



(a)



(b)

Figure 4.16 (a) Output power (b) Conv. Gain (dB) as function of RF power.

4.5.3 Third Order Intercept

The P1dB is an indication of a maximum allowable RF power that gives linear IF power at the mixer output .The third order intercept (TOI) point is an indication of the mixer linearity with adjacent channel interferences. The higher the TOI indicates there are less channel interferences after the frequency conversion by mixer. The TOI is determined by injecting two RF signals (two-tone) at slightly different frequencies and observe the extrapolated intersection of the fundamental and third order frequency

curves. In this design, the two tones are set at 2682.5 MHz and 2677.5 MHz with separation of 5 MHz .With mixing the two tones with the LO frequency of 2250 MHz will generate two fundamental IF frequencies at 427.5 MHz and 432.5 MHz with third order intermodulation frequencies of 422.5 MHz and 437.5 MHz. The IIP3 and OIP3 can be approximated with the two-tone test shown in Figure (4.17). One can see the power at both fundamental and third order intermodulation distortion frequencies as well as the intersection of the extrapolated lines showing the TOI

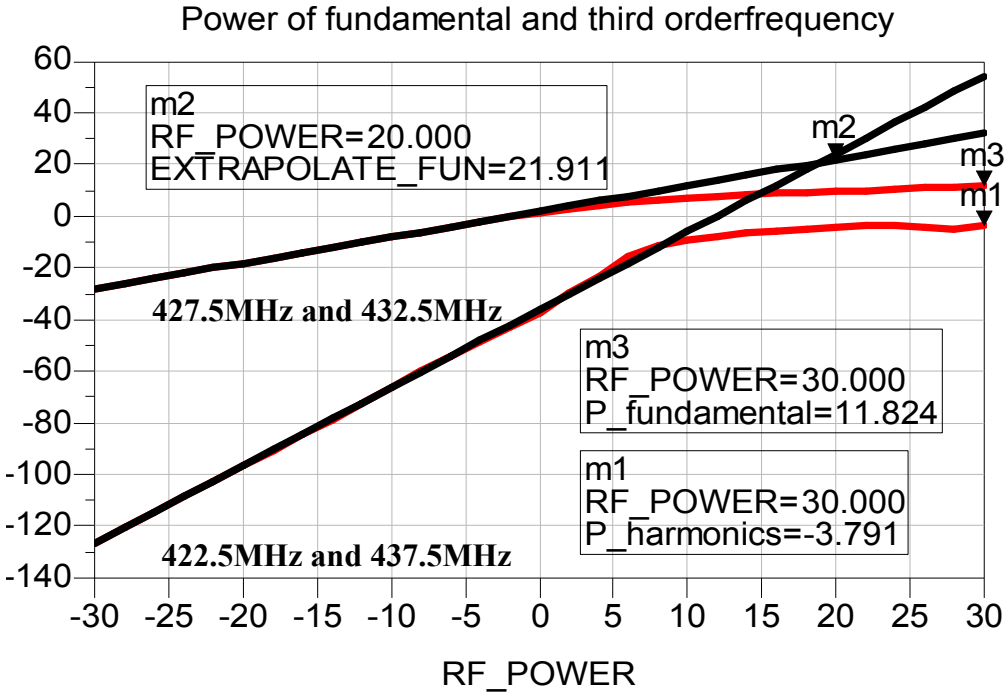


Figure 4.17 TOI with two-tone spacing of 5 MHz with LO power of 20 dBm.

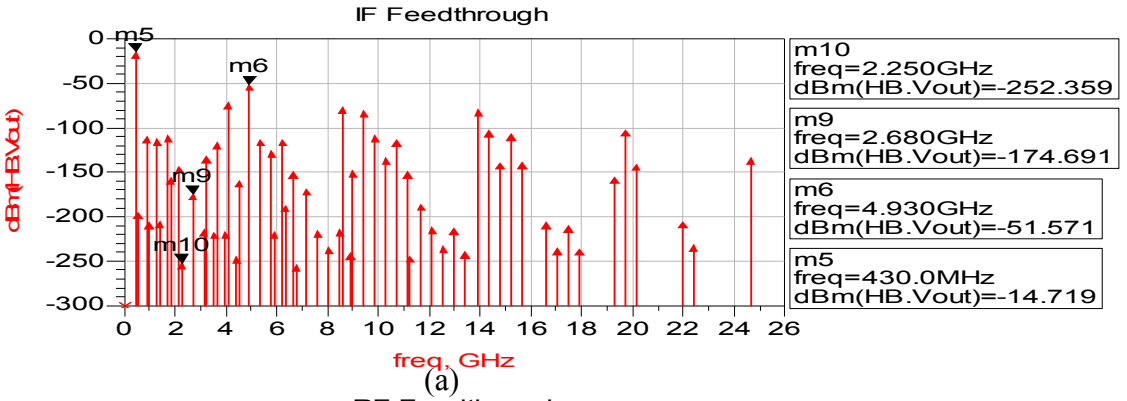
From TOI , one can determine the IIP3 and OIP3, which are roughly 20 dBm and 21.9 dBm, respectively. Also, the values are compared by *IP3OUT* block in ADS shown in Table 4.5 and they are fairly close.

Parameters	ADS simulation results	unit
Fundamental frequency	427.5 and 432.5	MHz
Third order frequency	422.5 and 437.5	MHz
IIP3	≈20	dBm
IIP3(IP3OUT block)	≈18.6	dBm
OIP3	21.9	dBm

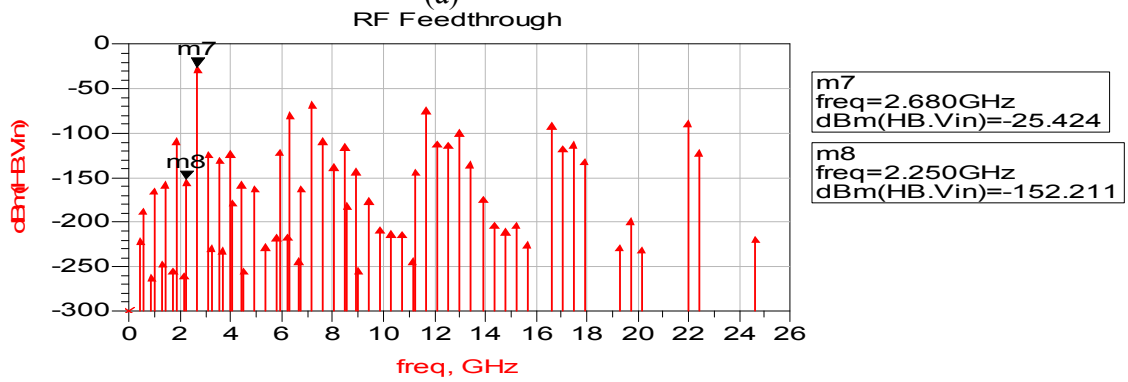
Table 4.5 IP3 of Gilbert mixer with tuned load, inductor degeneration.

4.5.4 Feedthrough

The approach taken to observe the mixer port feedthrough is to plot the spectrum of the signals at either port of the mixer. The feedthrough of both RF and LO at the IF port should be the primary concern as it can directly affect the component proceeding the mixer. Gilbert mixer being a fully differential topology can greatly eliminate the noise from RF and LO signal. From Figure 4.18 (a), the LO and RF signals are swept up to the fifth harmonic each and the voltage level of RF and LO frequency components appeared at the IF port are significantly attenuated by approximately 300 dB. In the figure, marker 9 (m9) and 10 (m10) are showing the voltage level of RF and LO frequencies, respectively.



(a)



(b)

Figure 4.18 (a) IF port feedthrough (b) RF port feedthrough.

LO signal leaking through the RF port also needs to be considered as well. In order to achieve high conversion gain in the Gilbert mixer, the power of LO are usually set on the order of 20 dBm. At such high power level, LO leakage can be significant thus creating problem for the preceding component, usually LNA. However, with the fully differential topology within the Gilbert mixer, the reverse leakage can be minimized. In Figure 4.18 (b), observe the LO voltage level (m8) at RF port (m7) attenuated by about approximately 128 dB. Moreover, it is possible to design the component preceding the mixer to have small reverse voltage gain (i.e. small |S12|) to further mitigate the LO leakage.

4.6 Summary

In this chapter, the design of a Gilbert mixer integrated with tune loads and source inductor degeneration has been presented. It has been shown that inductor degeneration provides the highest linearity and power gain, comparing to resistor degeneration. Also, with placing a tune load on the Drain terminal of the switching LO can successfully tune out the undesired output frequency component.

After the presentation of Gilbert mixer along with the design of LNA and PA in the previous chapter, it is desirable to cascade all the basic building blocks of a double-IF receiver while carefully considering the intermediate impedance matching. In the next chapter, the receiver undergoes a series of simulations and the valuable outcomes are shown.

Chapter 5

Test Results

In the previous chapters, the approaches taken to the mixer and amplifier design are discussed in detail. So far, only the transistor-level design and simulation has been presented. In this chapter, the system-level of the receiver chain will be shown and discussed. The receiver chain simulated in this work using ADS software is a double-IF topology, which means two mixers along the process of downconversion will be presented along with the necessary LNA, PA, and band-pass filter (BPF). Similar to previous chapters, several figures of merits (e.g. NF) defining the receiver's sensitivity and selectivity will also be shown. Also, it is worth mentioning that for easier convergence of the *HARMONIC BALANCE* simulator, the off-the-shelf passive elements in each of the receiver active devices have been replaced with ideal passive components under ADS *Lumped-Components* palette. Note that if off-the-shelf passive components are used, the simulation results would have been slightly different from the results obtained in this thesis.

5.1 Simulation Setup

The double-IF receiver discussed in chapter two shown in Figure (5.1) is implemented using the circuits designed and built in the last two chapters. Sometimes, inter-stage matching may not be necessary for SOC design given the wavelength of the operating frequency is shorter than the wire bonding of the on-chip large input impedances devices. The inter-stage matching in the off-chip design will be extremely important for minimum power reflection. In this work, almost all the devices built are purposely designed matching to the characteristics impedances of 50Ω, except the output of the first Gilbert mixer, which is purposely matched to ≈ 1000Ω. This is based on the passive BPF (e.g. Chebyshev filter) operating at the half gigahertz frequency is more commonly matched to high impedances in the range of 500 to 1000Ω.

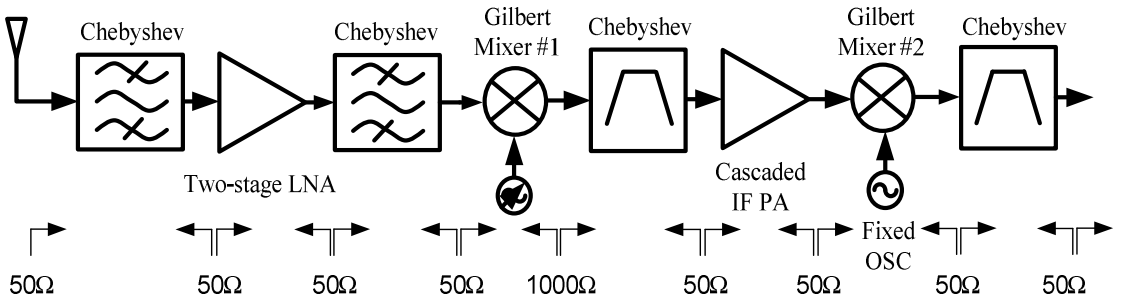


Figure 5.1 Double-IF receiver.

In this chapter, the test results of the receiver performance are simulated using the self-built active devices presented in the previous chapters and the band pass filters (BPF) provided by ADS under *Filters-Bandpass* palette. The BPF provided by ADS is able to offer constant-impedance that serves to minimize the disruptive reflection of IF signals at the output of the two mixers. Such filters attenuate the unwanted sum frequency signals

by absorption [35]. The required orders (n) of the filters in this design can be roughly obtained by Equation (5.1) [41].

$$n = \frac{2A(dB)}{20\log(\frac{2\Delta f}{f_{BW}})} \tag{5.1}$$

where the A(dB) is the desired filter attenuation in dB, Δf is the difference in hertz between the desired and image carrier frequency and f_{BW} is the bandwidth of the desired band , which should be slightly smaller than the filter passband bandwidth. It is noted that if a mixer IF port is terminated with a conventional passive IF filter, the undesired frequency signal (e.g. upper IF) will re-enter the mixer and generate IMD. To minimize the IMD, the IF filters proceeds the mixer are often designed to attenuate the undesired frequency by absorption. The double-IF receiver tested with frequency ranges shown in Table 5.1. The receiver is capable of receiving the desired band from 2.53 to 2.83 GHz and the corresponding image band from 1.67 to 1.97 GHz with the tuning range from 2.1 to 2.4 GHz injected into the first Gilbert mixer.

Desire band (GHz)	2.53 to 2.83	Second mixer fixed OSC (MHz)	410
Image band (GHz)	1.67 to 1.97	Output of 1st mixer (MHz)	430
First mixer tuning range (GHz)	2.1 to 2.4	Output of 2nd mixer (MHz)	20
channel bandwidth (MHz)	5	channel spacing (MHz)	5

Table 5.1 Receiver frequency specifications.

5.2 Time Domain Simulation

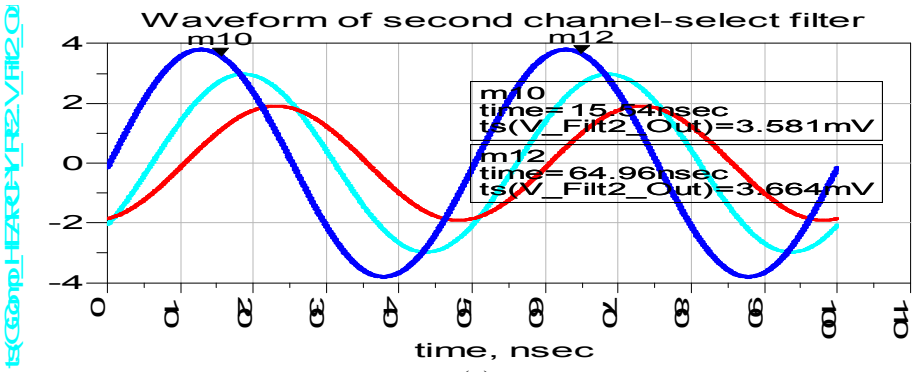
5.2.1 Last IF

The details of the last IF simulation is shown in Table 5.2. The receiver simulation is performed under ADS *Harmonic Balance* simulator, by sweeping the frequencies of input RF signal, the corresponding LO frequency signal, and the second fixed frequency LO signal. The RF frequency of 2.68 GHz as well as the two frequencies of 2.54 and 2.82 GHz located in the leftmost and rightmost channel inside the desired band is fed to the receiver for the purpose of observing the recovered 20 MHz signal at the output of the last channel-select filter. Also note that the power of the first and second LO as well as the available RF power are set at 20, 0, and -70 dBm, respectively, to avoid driving into saturation. Note that the power of image frequency is purposely set to be 30 dB higher than the RF power (i.e. -70 dBm) situated at the desired frequency channel. It is worthy to mention that to maintain consistency, the power level in Table 5.2 are kept constant throughout the entire single point sweep following. The ADS *Design Guide* - *RF System* template allows two-dimensional sweep of both available RF power and LO power for the assessment of the receiver P1dB [48].

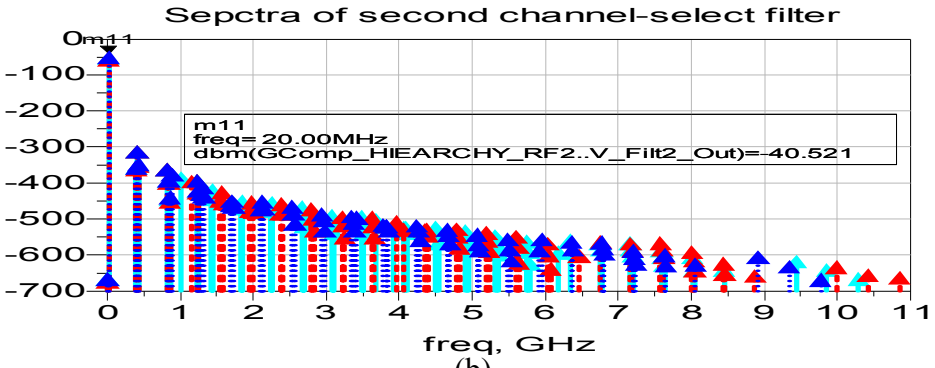
Available RF power (dBm)	-70	Second LO power (dBm)	0
Image frequency power (dBm)	-40	Image frequency harmonics	3
Tested RF frequencies (GHz)	2.54, 2.68 , 2.82	RF frequency harmonics	3
Image frequencies (GHz)	1.68, 1.82 , 1.96	Mixer LO harmonics	3
First LO power (dBm)	30	Maximum mixing order	4

Table 5.2 Last IF simulation specifications.

The second IF signal recovered at the output of the last channel-select filter with the input RF frequencies of 2.54, 2.68, and 2.82 GHz is shown in the Figure (5.2) below. According to Figure 5.2 (a), the three waveforms of the second IF signals showing different amplitudes (i.e. 2 to 4 mV) and phases with roughly the same signal periods of about 50 ns, which corresponds to 20 MHz.



(a)



(b)

Figure 5.2 Output at last channel-select filter.

Moreover, according to the frequency spectra, the marker 11 (m11) situated at 20 MHz was amplified from -70 dBm given to roughly power of -40 dBm, which is significantly higher comparing with many unwanted frequency components shown in Figure 5.2 (b). It is worthy to mention that the waveform and power level amplitudes decrease while RF input frequency increases. The power level of 20 MHz signal can be further amplified by cascading another PA. However, the linearity of the PA needs to be carefully considered, as the last building block down in the receiver front-end largely determines the overall linearity.

Choosing the IF frequency of 20 MHz should balance the noise problem result from low IF frequency and ADC clock jitters resulting from high IF frequency. Having a 20 MHz carrier signal with bandwidth of 5 MHz, the Nyquist criterion indicates that the sampling frequency of the analog-to-digital converter (ADC) proceeding needs to be at least 45 MHz. Therefore, if the ADC is sampling at a clock rate of 45 MHz, it would be enough to accommodate signal with maximum frequency of 22.5 MHz. Moreoever, it is desirable to present a constant signal level to the ADC for maintaining the proper ADC resolution . As a result, receive signal system typically use one or more variable gain amplifiers (VGA) to complete the automatic-gain-control (AGC) loop.

5.2.2 Mixer Operation

Mixer, a device that is both linear and inherently nonlinear produces several unwanted frequency components at its input and output. In particular, the most important signal frequencies (e.g. upper IF and feedthrough) that can cause severe nonlinearities at the input and output of the both mixers are indicated in Table 5.3. In addition, the available power used to sweep to RF and LO signals remain unchanged as indicated in Table 5.2. The signal waveform and spectra shown in Figure (5.3) indicates the mixing operation at the input and output of the first Gilbert mixer. Prior to the first mixer, the 6^{th} order band-select filter is placed in the receiver to partially attenuate the image band from the desired band. However, at gigahertz operating frequency, the extremely high filter Q is needed, therefore, attenuation is limited.

First mixer lower IF (MHz)	430	First mixer RF (GHz)	2.68
First mixer upper IF (GHz)	4.93	First mixer image (GHz)	1.82
Second mixer lower IF (MHz)	20	Second mixer RF (MHz)	430
Second mixer upper IF (MHz)	840	Second mixer image (MHz)	450
LO of 2^{nd} mixer (MHz)	410	LO of 1st mixer (GHz)	2.25

Table 5.3 Significant nonlinear frequency components.

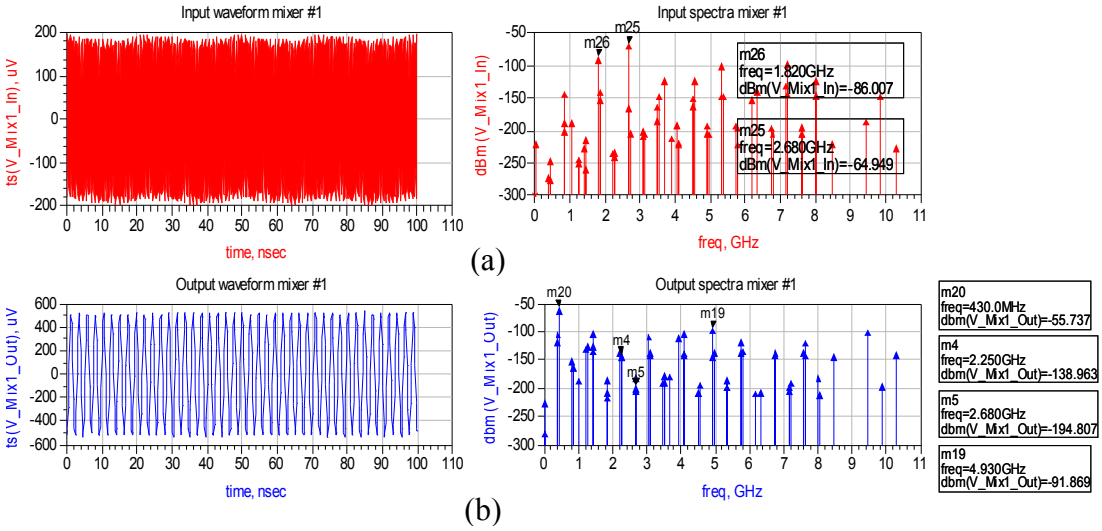


Figure 5.3 Signal waveform and spectra at (a) input and (b) output of first mixer.

To better explain the mixing operation, perhaps it is best to look at the frequency spectra. The frequency components shown in Figure 5.3 (a) indicates the mixer input, proceeding the first band-select filter, with both the desired RF and image frequencies of 2.68 and 1.82 GHz on the power level of -65 and -86 dBm, respectively. This is predictable for a typical lossy filter operating at gigahertz range. The IF and LO feedthrough at the RF port is nearly negligible with the power level of roughly -200 dBm.

Looking at the output signal of the first mixer shown in Figure 5.3 (b), the only desirable frequency component, indicated by marker 20 (m20), is the lower IF of 430 MHz with the power level of roughly -56 dBm. The upper IF frequency of 4.93 GHz, indicated by marker 19 (m19), is showing 35 dB lower with the tuned load placed in the mixer as explained in the previous chapter. The RF and LO feedthrough at the output are insignificant as both power levels are below -100 dBm indicated by markers 4 (m4) and 5 (m5). Similar to the first mixer, the mixing operation of the second mixer is shown in Figure (5.4) below. The LO feedthrough, indicated by marker 16 (m16), at the RF input of the second mixer is found to be significant with the power level of roughly -14 dBm.

Fortunately, this impact of reverse LO leakage can be minimized by lowering the reverse transmission gain (i.e. S12) of the preceding devices in the receiver. Recalling the Figure 5.3 (b), the power level of the reverse LO leakage of 410 MHz is roughly -100 dBm.

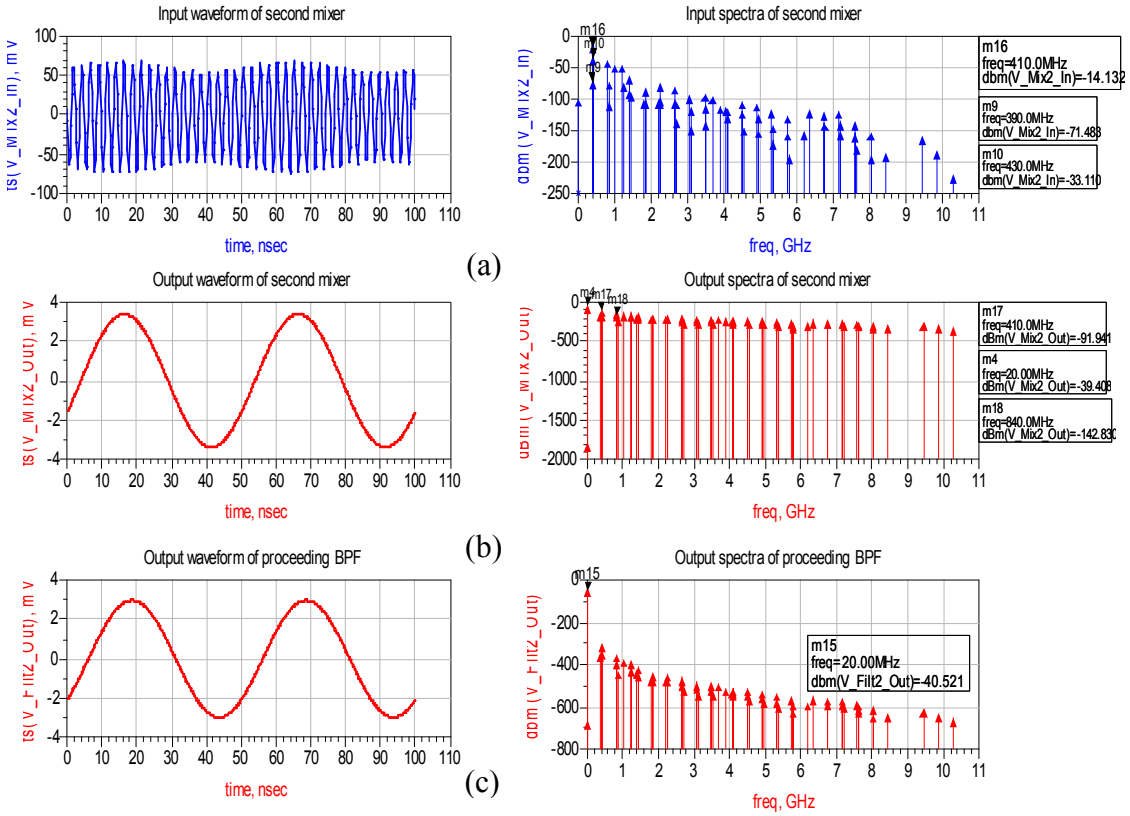


Figure 5.4 Signal waveform and spectra at (a) input, (b) output of second mixer, and (c) output of proceeding BPF.

The Figure 5.4 (b) shows the desired lower IF of 20 MHz , indicated by marker 4 (m4), with the power level of roughly -40 dBm. Similar to the first mixer, the power level of RF feedthrough (m2) and upper IF (m1) at the output of the second mixer are insignificant. Furthermore, waveform and spectra of the signal at the output of the last BPF proceeding the second mixer shows a “cleaner” 20 MHz signal by filtering out the unwanted frequency components as indicated by spectra in Figure 5.4 (c).

5.2.3 Cascaded PA

The cascaded IF PA in this work is constructed by cascading the conjugate matched PA with the proceeding load-line matched PA for high power gain/ power transfer. The time-domain signal waveforms at the input and output of the cascaded IF PA are shown below in Figure (5.5). From the markers 13 (m13) and 14 (m14) shown, the voltage amplitude is amplified by roughly 62 times (i.e. ≈ 68.4 mV / 1.1 mV) with a phase difference of almost 180 degrees.

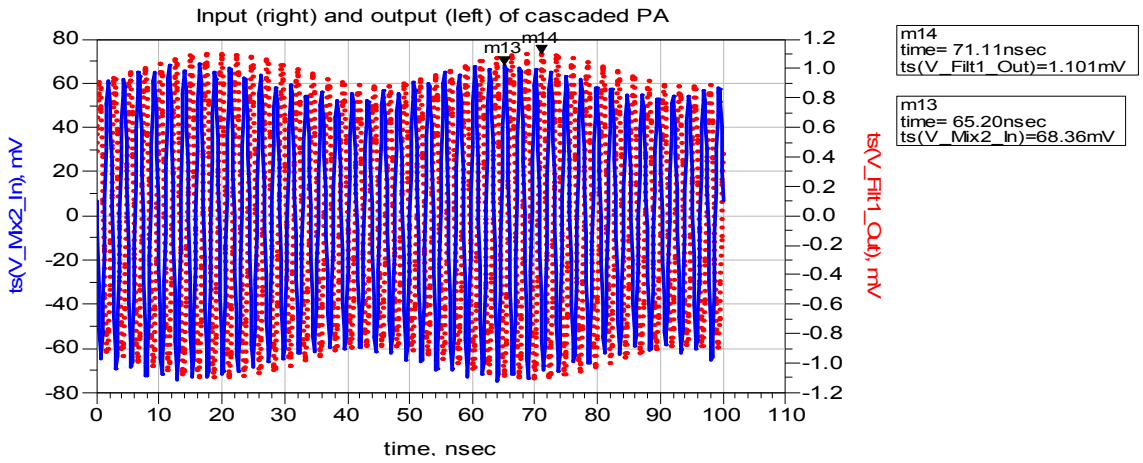


Figure 5.5 Input and output voltage waveform of the cascaded PA.

The output waveform shows out-of-phase with respect to the input waveform, which is predictable since the PA is constructed with transistors and passive components often leading to phase changes between the signals.

5.2.4 Receiver Selectivity

After assessing the details of signal operations in the individual segments in the receiver, it is desirable to cascade all the devices in order to calculate several important figure-of-merits that indicate the receiver selectivity and sensitivity. In order to observe the receiver's selectivity, the P1dB and TOI are both important indications as they represent the linear region where the active device can function.

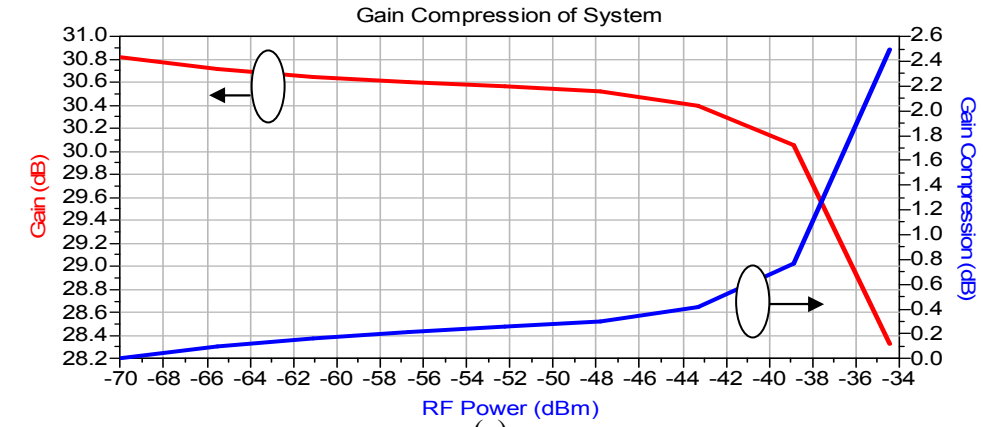
The details of the RF power sweep for obtaining receiver P1dB is given in Table 5.4. The frequency of 2.68 GHz was selected as the tested RF signal with the corresponding image frequency of 1.82 GHz to be twice the first IF (860 MHz) frequency apart. The power levels of both signals are considered up to 5^{th} harmonics with the maximum mixing order of 7 chosen under ADS *Harmonic Balance* simulation [49].

Available RF power (dBm)	-70 to -35	First LO power (dBm)	20
Image frequency power (dBm)	-40	Second LO power (dBm)	0
Tested RF frequencies (GHz)	2.68	Image frequency harmonics	5
Image frequencies (GHz)	1.82	RF frequency harmonics	5
Frequency spacing (MHz)	5	LO harmonics	1
Maximum mixing order	7		

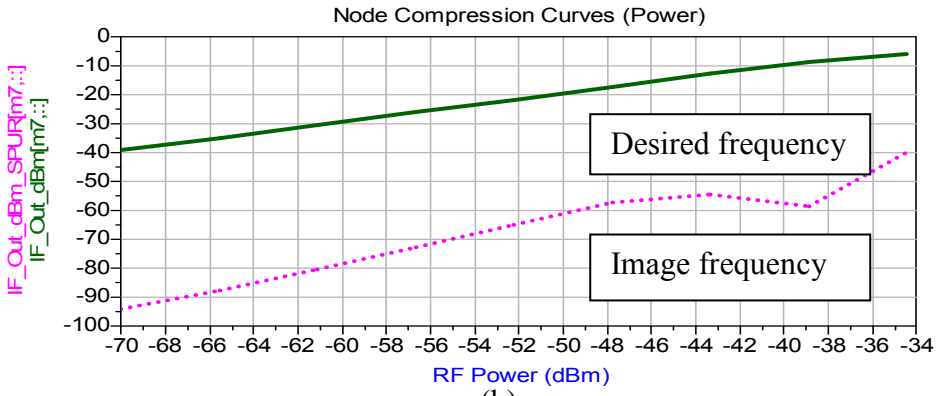
Table 5.4 Receiver P1dB and IP3 simulation details.

According to the left-Y axis in Figure 5.6 (a), the entire receiver is capable of providing roughly 30dB of gain up to the maximum RF power of roughly -38 dBm, which is the point of IIP1 indicated as seen on the right-Y axis. Moreover, both image

and desired frequency can be downconverted to the same IF, with one being attenuated in the process of frequency downconversion and the other amplified down the chain.



(a)



(b)

Figure 5.6 (a) Receiver P1dB and (b) output power.

It is apparent that according to Figure 5.6 (b), the signal at the image frequency stays at roughly 55 dB lower than the desired RF frequency signal by observing the power level at the output of last channel-select filter in the receiver. On the contrary, the desired signal frequency is being amplified as the output power follows the RF power with the slope of roughly one. The figure also indicates that even the receiver is gradually saturating above -34 dBm, it is still capable to differentiate between the signals at both image and desired RF frequency with the difference of roughly 35 dB.

Finding the IP3 and IMD also requires the sweeping of RF power and calculations based on the ADS *Design Guide* - *RF System* template for accurate assessments. It is noted that the power of both LO are kept constant as indicated in Table 5.4.

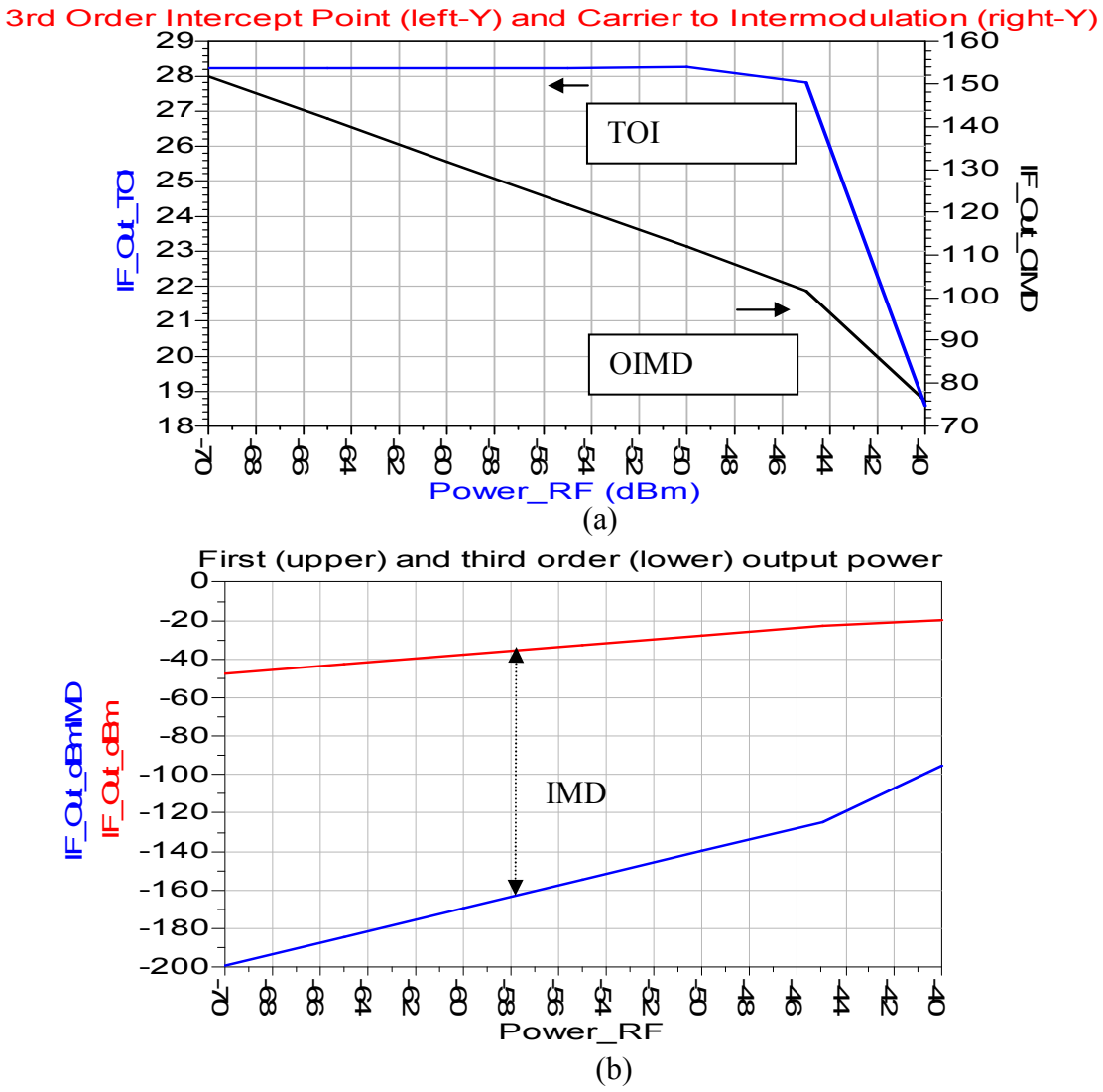


Figure 5.7 (a) OIP3 and IMD vs. RF power sweeping of last IF (b) Fund. and third order output power vs. RF power sweeping of last IF.

According to Figure 5.7 (a), the trace corresponding to the left y-axis indicates the receiver OIP3 while the right y-axis indicates the OIMD by probing the output of the last

device in the chain. The receiver remains relatively linear with the available RF power less than -50 dBm with the OIMD and OIP3 stayed nearly constant. As explained in the previous chapters, the higher the OIP3 and OIMD the more linear the receiver is, therefore leading to better selectivity. Moreover, the IMD simulation of the output power at the last IF frequency with the first order frequencies of 17.5 MHz, 22.5 MHz and third order frequencies of 12.5 MHz, 27.5 MHz, shown in Figure 5.7 (b). Note that the power difference between the two traces indicate the IMD with respect to the carrier, which is represented by the trace corresponding to the right-Y axis in Figure 5.7 (a).

5.2.5 Receiver Sensitivity

After determining the receiver's selectivity, it is desirable to obtain the sensitivity by calculating the noise figure, which demonstrates the SNR degradation along each of the devices along the chain. In this design, in order to obtain more accurate calculations of the receiver's performance, the numbers shown in the table below are obtained using the ADS *Design Guide* - *RF System* and the *Noise controller* with other self-built devices [48]. The cumulated noise figure, power gain, and device power at each node labeled in Figure (5.8) are provided in Table 5.5.

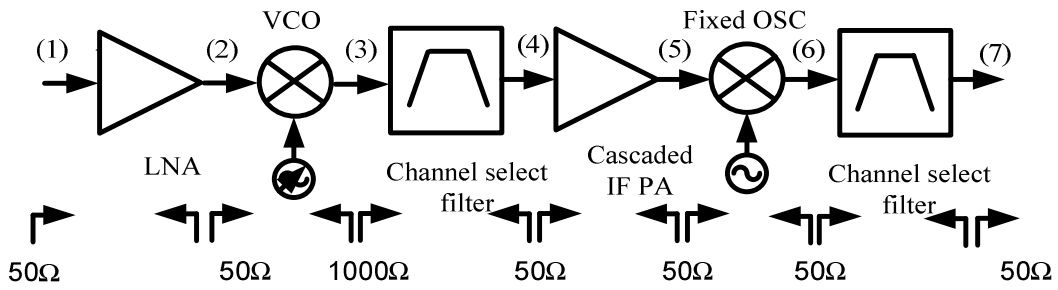


Figure 5.8 Nodes labeled in the double-IF receiver for power calculations.

Power at nodes (dBm)							
Node	(1)	(2)	(3)	(4)	(5)	(6)	(7)
	-64.48	-54.07	-56.06	-25.9	-19.26	-20.263	-0.263
Cumulated Noise Figure (dB)							
Node	(2)	(3)	(4)	(5)	(6)	(7)	System
	6.11	8.22	8.23	7.85	8.53	8.53	8.53
Cumulated Power Gain (dB)							
Node	(2)	(3)	(4)	(5)	(6)	(7)	System
	5.51	15.94	13.94	44.1	50.74	49.737	49.737
Noise temp	290 Kelvin						
Noise bandwidth	5 MHz						
Boltzmann constant	1.38×10^{-23} J/Kelvin						
Power consumption	≈557.4 mW						
Minimum detectable input	≈-95.4 dB						
SFDR	≈48.9 dB						
Available RF power (dBm)	-70						

Table 5.5 Level diagram of each node along the chain in Fig. 5.8.

It is worthy to mention that with the receiver NF of roughly 8.53 dB, the minimum detectable input level ($P_{i,MDS}$) can be approximately obtained as -95.4 dB given the minimum required SNR of 3 dB. Moreover, the spurious free dynamic range (SFDR) is roughly equal to 48.9 dB given the OIP3 of roughly 28 dBm as seen in Figure 5.7 (a). It is noted that the above results are obtained by simulating the desired RF frequency, first LO frequency, and second LO frequency, with the maximum order of five under ADS *HARMONIC BALANCE* [49]. Therefore, the results may vary depending on the numbers of harmonics taken by the designer.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis, a double-IF downconversion radio receiver located in the *IEEE* S-band is designed and simulated using Agilent EEsof Advance Design System (ADS). The wide frequency range radio receiver operating from 2.53 GHz to 2.83 GHz with the essential active components such as LNA, mixer, and PA haven been successfully design and simulated.

The tradeoffs of the radio receiver sensitivity and selectivity have been discussed in chapter 2 along with the frequency planning selected to balance the tradeoffs. Some figure-of-merits of the receiver and the active devices performances such as P1dB and power gain are assessed throughout the thesis. Moreover, several design templates under ADS *RF Design Guide* are utilized for obtaining higher accuracy of the performance assessments. The essential active devices existing in the receiver have been designed and implemented.

In chapter 3, a rarely seen methodology of designing a microwave low noise amplifier (LNA) has been presented. The approach taken is to start by first choosing the

desired Γ_L by plotting constant power gain circle and fixing an acceptable input mismatch factor (M). With the chosen M, the transducer gain (G_T) can be obtained. With the desired $\Gamma_{L,}$ the Γ_{in} can be calculated and the input VSWR can be plotted. With an iterative process, the "sweet" spot giving low NF, moderate gain, and good input VSWR can be obtained. Moreover, , a notch filter is integrated in order to attenuate the image band which is the same IF away from the LO frequency.

A single-stage LNA with and without notch filter as well as a two-stage LNA with notch filter have been designed. As a result, the two-stage LNA is able to provide the following:

- Lower NF.
- Good input VSWR.
- Moderate power gain.
- Image band attenuation.
- Low power consumption.

The second half of chapter 3 presented the approach of designing a class-A power amplifier (PA) using load-pull method. Load-pull method is essentially a process of varying the output impedance presented to the active component while plotting the output power and other parameters such as power added efficiency (PAE) on the Smith Chart. Both of the conventional conjugate matched and power matched PA are cascaded for high power gain and transfer to the receiver. The short summary of characteristics of the two-stage PA is as follows.

- Higher power gain.
- Load-Pull design.

- High P1dB and IIP3.

In chapter 4, the fully differential (Gilbert) mixer was simulated based on SPICE3 0.5 μm CMOS process technology. The Gilbert mixer is the most widely adopted topology existing in the modern radio receiver. It is able to provide low port feedthrough and eliminate even order intermodulation distortion (IMD) with the tradeoffs of noise figure and power consumption. The short summary of characteristics of the fully differential (Gilbert) mixer are as follows.

- Low port feedthrough.
- Linear with IP1dB.
- Moderate power gain.

In chapter 5, all the active components built are put together for verifying a series of assessments. The most important outcome of the radio receiver design is that it is able to downconvert the desired frequency band with similar waveform amplitudes. This is desirable as it eases off the requirements on the possible AGC and ADC. Also, the signal waveform and spectra of the input and output of each cascaded component (i.e. active devices and filters) in the receiver have been shown in detail. Lastly, the sensitivity (e.g. NF) and selectivity (e.g. IIP3) of the entire receiver as well as the individual active devices are presented.

6.2 Future Work

This thesis provides detailed information on building a RF front-end receiver. It can be used as a base for the possible ongoing projects in the Wireless Design Laboratory. Possible future work based on this thesis can be summarized as follows.

- It is desired to fully integrate the active devices implemented in the thesis such as LNA, mixer, and PA into RF front-end SOC. Integrating all system components into one chip in a single module can minimize the product size, improve reliability, increase fabrication process.
- To increase the Gilbert mixer conversion gain the folded mixer topology has also been widely adopted [50]. In the folded mixer topology the RF stage has been separated from the LO and IF stage. This implies that larger voltage drop can be placed across the load resistor. This can directly contribute to increase of conversion gain assuming current flowing through is a fixed constant.
- The main drawback of the Gilbert mixer is high power consumption due to having roughly twice the bias current and power consumption to replicate the linearity and conversion gain of the single-balance mixer. This can be mitigated by introducing a novel approach called bleeding technique [51] , which it allows only portion of the bias current through RF stage transistors appear at LO stage switching-transistors, thus reduce the drop in voltage headroom and transistor flicker noise (1/f) as well as improve switching efficiency. Therefore, a higher gain can achieve merely by increasing the output load resistance without additional power consumption.

Bibliography

[1] Lee,T.H., The Design of CMOS Radio Frequency Integrated Circuits, 2nd ed., Cambridge, UK:Cambridge University Press,2004.

[2] Abidi,A." RF CMOS Comes of Age",IEEE Microwave Mag., Dec.2003.

[3] Razavi, B., RF Microelectronics,Upper Saddle River,NJ:Prentice Hall,1998.

[4] Amir M. Sodagar., Analysis of Bipolar and CMOS Amplifiers , CRC Press,2007.

[5] A. S. Sedra and K. C. Smith, Microelectronic Circuits. 5th ed., New York: Holt, Rinehart and Winston, 2004.

[6] Skotnicki, T.; Hutchby, J.A.; Tsu-Jae King; Wong, H.-S.P.; Boeuf, F.; , "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *Circuits and Devices Magazine, IEEE* , vol.21, no.1, pp. 16- 26, Jan.-Feb. 2005.

[7] M. el Hassan; C. P. Moreira; A. A. Shirakawa; E. Kerherve; Y. Deval; D. Belot; A. Cathelin; , "A Multistandard RF Receiver Front-End Using a Reconfigurable FBAR Filter," *Circuits and Systems, 2006 IEEE North-East Workshop on* , vol., no., pp.173-176, June 2006.

[8] Reines, I.; Park, S.-J.; Rebeiz, G. M.; , "Compact Low-Loss Tunable -Band Bandstop Filter With Miniature RF-MEMS Switches," *Microwave Theory and Techniques, IEE Transactions on* , vol.58, no.7, pp.1887-1895, July 2010.

[9] Diamantis, S.; Ahmadi, M.; Jullien, G.A.; Miller, W.C.; , "A programmable MEMS bandpass filter," *Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on* , vol.1, no., pp.522-525 vol.1, 2000.

[10] C. Nguyen: "MEMS Technology for Timing and Frequency Control," IEEE Trans. Ultrason., Ferroelect., Freq. Contr., vol. 54, no. 2, pp. 251–270, Feb. 2007.

[11] Min-Yi Wang; Sheen, R.R.-B.; Chen, O.T.-C.; Tsen, R.Y.J.; , "A dual-band RF front-end for WCDMA and GPS applications," *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on* , vol.4, no., pp. IV-113- IV-116 vol.4, 2002.

[12] Dao, Vu Kien; Choi, Byoung Gun; Park, Chul Soon; , "A Dual-band CMOS RF Front-end for 2.4/5.2 GHz Applications," *Radio and Wireless Symposium, 2007 IEEE* , vol., no., pp.145-148, 9-11 Jan. 2007.

[13] Wu, S.; Razavi, B.; , "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *Solid-State Circuits, IEEE Journal of* , vol.33, no.12, pp.2178-2185, Dec 1998.

[14] Lee, J.; Nam, I.; Cho, S.; Lee, K.; , "Highly linear and low noise 2.4 GHz RF front-end circuits using transformer and vertical NPN BJT," *Electronics Letters* , vol.43, no.2, pp.103-105, January 18 2007.

[15] Gotzfried, R.; Beisswanger, F.; Gerlach, S.; , "Design of RF integrated circuits using SiGe bipolar technology," *Bipolar/BiCMOS Circuits and Technology Meeting, 1997. Proceedings of the* , vol., no., pp.51-56, 28-30 Sep 1997.

[16] Migowski, G.O.; Santos, J.C.A.; , "Designing an RF front end radio receiver for educational purposes," *Microwave and Optoelectronics Conference, 2003. IMOC*

2003. Proceedings of the 2003 SBMO/IEEE MTT-S International , vol.1, no., pp. 497- 502 vol.1, 20-23 Sept. 2003.

[17] R. R. Pantoja, "*Osciladores de microondas atransistores sintonizados a varactor",* M. Sc. Thesis, Rio de Janeiro, May 1986.

[18] "Agilent EEsof EDA Design & Simulation Software" , Internet: www.home.agilent.com/agilent/product.jspx?cc=CA&lc=eng&ckey=1475688&nid=-3360.0.00&id=1475688 (visited 24, Jan, 2011).

[19] G. Gonzalez, "Microwave transistor amplifiers - analysis and design", 2nd Edition 1997, Prentice-Hall.

[20] Xiaopeng Li, Mohammed Ismail, "Multi-Standard CMOS Wireless Receivers: Analysis and Design " Springer Netherlands, 2002.

[21] R.C. Sagers, "Intercept Point and Undesired Responses," IEEE Trans. Vehicular Tech., Vol.32,pp.121-133, February 1983.

[22] D.M. Pozar, "Microwave engineering", 3rd Edition, 2005 John-Wiley & Sons.

[23] D.M. Pozar, "Microwave and RF Design of Wireless Systems", 2001 John-Wiley & Sons.

[24] S. C. Cripps, "RF power amplifier for wireless communications", 1999, Artech House.

[25] Kondoh, H., "FET Power Performance Prediction Using a Linearized Device Model", Proc. IEEE Intl.Microw Symp.,MTT-S,1989,pp.567-572.

[26] Van der Heijden, M.P.; De Vreede, L.C.N.; Burghartz, J.N.; , "On the design of unilateral dual-loop feedback low-noise amplifiers with simultaneous noise,

impedance, and IIP3 match," *Solid-State Circuits, IEEE Journal of* , vol.39, no.10, pp. 1727- 1736, Oct. 2004.

[27] Voinigescu, S.P.; Maliepaard, M.C.; Schroter, M.; Schvan, P.; Harame, D.L.; , "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design ," *Bipolar/BiCMOS Circuits and Technology Meeting, 1996., Proceedings of the 1996* , vol., no., pp.61-64, 29 Sep-1 Oct 1996.

[28] "ELEC 483-Microwave and RF Circuits and Systems- Low Noise Amplifier Design", Internet: <http://bmf.ece.queensu.ca/elec483/slides/LNA_design.pdf > (visited 24, Jan, 2011).

[29] "BFR520 plastic surface-mounted package", Internet: <http://www.nxp.com/documents/data_sheet/BFR520.pdf> (visited 24, Jan, 2011).

[30] Gray P. R., Meyer R. G., "Analysis and design of analog integrated circuits", 3rd Edition, 1993, John-Wiley & Sons.

[31] Kondoh, H., "FET Power Performance Prediction Using a Linearized Device Model", Proc.IEEE Intl.Microw Symp.,MTT-S,1989,pp.567-572.

[32] "RO4000® Series High Frequency Circuit Materials", Internet: <http://www.rogerscorp.com/acm/products/16/RO4000-Series-High-Frequency-Circuit-Materials-Woven-glass-reinforced-ceramic-filled-thermoset.aspx> (visited 24, Jan, 2011).

[33] M. Goldfarb and R. Pucel. "Modeling Via Hole Grounds in Microstrip," *IEEE Microwave and Guided Wave Letters* , Vol. 1, No. 6, June 1991, pp. 135-137.

[34] S. A. Maas, “Nonlinear microwave circuits”, 1988, Artech House.

[35] C. W. Sayre, “Complete wireless design”, 2001, McGraw-Hill.

[36] S. C. Cripps, “RF power amplifier for wireless communications”, 1999, Artech House.

[37] “BFR92A plastic surface-mounted package”, Internet: <http://www.nxp.com/#/pip/pip=[pip=BFR92A_N]|pp=[t=pip,i=BFR92A_N]> (visited 24, Jan, 2011).

[38] Cripps,S., “A Method for the Prediction of Load-Pull Power Contours in GaAs MESFETs” proc.IEEE Intl.Microw Symp.,MTT-S,1983,PP.221-223.

[39] Ludwig. R and Bogdanov. G, RF Circuit Design. Pearson Education, 2nd edition,2000.

[40] Gilbert, B., "A precise four-quadrant multiplier with subnanosecond response," *Solid-State Circuits, IEEE Journal of* , vol.3, no.4, pp. 365- 373, Dec 1968.

[41] Rogers J, Plett C,”Radio Frequency Integrated Circuit Design”, Artech House, 2003.

[42] Caverly R,”CMOS RFIC Design Principles”, Artech House,2007.

[43] Stephen Yue, “Linearization techniques for mixers”,Analog circuit design Course, 2000.

[44] Voinigescu, S.P.; Maliepaard, M.C.; , "5.8 GHz and 12.6 GHz Si bipolar MMICs," *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International* , vol., no., pp.372-373, 488, 6-8 Feb 1997.

[45] E.Abou-Allam, J.Nisbet,”Low-Voltage 1.9-GHz Front-End Receiver in 0.5-u CMOS technology”,IEEE,2001.

[46] “ECEN 665CMOS RF Integrated Circuits”,

Internet: <www.ece.tamu.edu/~kentesar/ELEN665/ELEN665_7.pdf > (visited 24, Jan, 2011).

[47] “Website of BSIM”,

Internet: < http://www-device.eecs.berkeley.edu/~bsimsoi/ > (visited 24, Jan, 2011).

[48] “Advanced Design System (ADS) Core”**,**

Internet: < http://www.home.agilent.com/agilent/product.jspx?nid=-34346.804581.00&lc=eng&cc=CA> (visited 24, Jan, 2011).

[49] “Harmonic Balance Basics”**,**

Internet: < www.edocs.soco.agilent.com/display/ads2009/Harmonic+Balance+Simulation> (visited 24, Jan, 2011).

[50] Kihwa Choi; Dong Hun Shin; Yue, C.P.; , "A 1.2-V, 5.8-mW, Ultra-Wideband Folded Mixer in 0.13-μm CMOS," *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE* , vol., no., pp.489-492, 3-5 June 2007.

[51] S. -G. Lee, et al, “ Current-reuse bleeding mixer”, Electronics Letters, Vol.36, No 8, April.2000.