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THE PARALLEL CONNECTION OF SINGLE PHASE DC TO AC POWER CONVERTERS

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ABSTRACT

THE PARALLEL CONNECTION OF SINGLE PHASE

DC TO AC POWER CONVERTERS

Joseph Woods

Electrical power converter subsystems are placed between an ac-mains bus and a load in order to condition the power being transferred, to protect the load and the ac source, and to provide uninterruptible power supply (UPS) features. One method of providing the required interface in, low to medium power applications (1.0 to 150 kVA), is to connect multiple converter modules in parallel. This approach has the advantages of increased reliability, due to the redundancy of the system, and flexibility, since modules can be added or removed as needed.

The successful performance of a parallel-connected system depends on i) the modularity of the individual converter units, ii) their response characteristics, and iii) the quality of the power they produce. A single-phase converter module and a parallel connection circuit is proposed that meets these three objectives by using a fast control circuit for each converter, insulated-gate bipolar transistors (IGBTs), a high switching frequency (10 kHz to 20 kHz), and a frequency modulated (FM) communication scheme. Thus, the modularity is enhanced by using an FM signal in order to eliminate the wiring normally required to share the converter output current control parameters.

DEDICATION

This Thesis is dedicated to the memory of the late Dr. P. D. Ziogas, with whom the author began the studies that culminated in the production of the following work. The author also wishes to acknowledge the support and aid given by his supervisors, Dr. G. Joos and Dr. P. Jain and his colleagues including, Mr. Jose Espinoza, Mr. Humberto Pinhiero, and Mr. Donato Vincenti at the P. D. Ziogas Memorial Power Electronics Laboratory. Finally, appreciation is due to the authors family, wife Dorsey and son Denis for their support and patience.

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1. INTRODUCTION

1.1. The Origin of The Parallel Converter Topology

It can be argued that the 'post industrial' society is characterized as much by its ever growing dependence on the reliable operation of a wide range electrically powered technologies as by any other feature [1]. The performance and reliability levels expected of the computer and telecommunications industries, for example, approach 100 percent. For their convenience, the consuming public expects that their telephones, cable television networks, and banking machines will work every time they are needed. In locations housing businesses and small to medium-sized industrial plants (10 - 150 kVA), there are pieces of computing, communication, and production equipment that are very important to the success of the operations they serve. The reliability of these 'critical' loads depends in turn on the equipment and circuits used to protect their sources of power. One method of ensuring the operation of these important low-power circuits is to attach them to a separate power supply bus and to install power conditioning circuits as a connection between the isolated bus and the mains or utility bus. If the reliability, flexibility, and power capacity of the critical bus must be increased, then a strategy is required that will expand the power conditioning interface efficiently and easily. A system of identical power converter modules connected in parallel is one means of achieving this goal.

1.1.1. Power Converters and Power Conditioning

Invariably, an electronic or electrical device draws the power it needs from a utility

bus which does not match the voltage or current requirements of the device. The failure of the mains bus to provide the power required by any piece of sophisticated electrical equipment has two modes:

i) There is a complete loss of power resulting in total failure.

ii) The quality of the power is so poor that the equipment malfunctions.

Unfortunately, both modes are aided by the development of smaller, lighter, and cheaper models of many classes of electrical circuits. Moreover, the quest for higher performance and lower cost has created a situation where the circuits are more sensitive to the low quality power they themselves produce. This is so because the trend towards compact electrical devices has led to the proliferation of nonlinear switching power supplies which pollute their source of power by reflecting noise back into the utility bus. Since there is a practical and economical limit to the amount of protective circuitry that the designer can incorporate in his power supply design, there is a need for a class of circuit which can protect and condition the power required by the low-power, single-phase, high performance load and its associated bus.

Protection of sensitive loads in a single location can be achieved by connecting them to a common critical bus which is fed by a power conversion circuit such as an uninterruptible power supply (UPS) or a power factor correction circuit (PFC) [2] [3]. A typical installation is shown in Fig. 1.1 where the converter acts to protect the critical bus from disturbances caused by large loads such as welders or motors. These loads may normally require 5 per-cent of the maximum current allowed by the utility bus. However, the operating cycle of the nonlinear load may instantly switch on and switch off 90 per-cent of

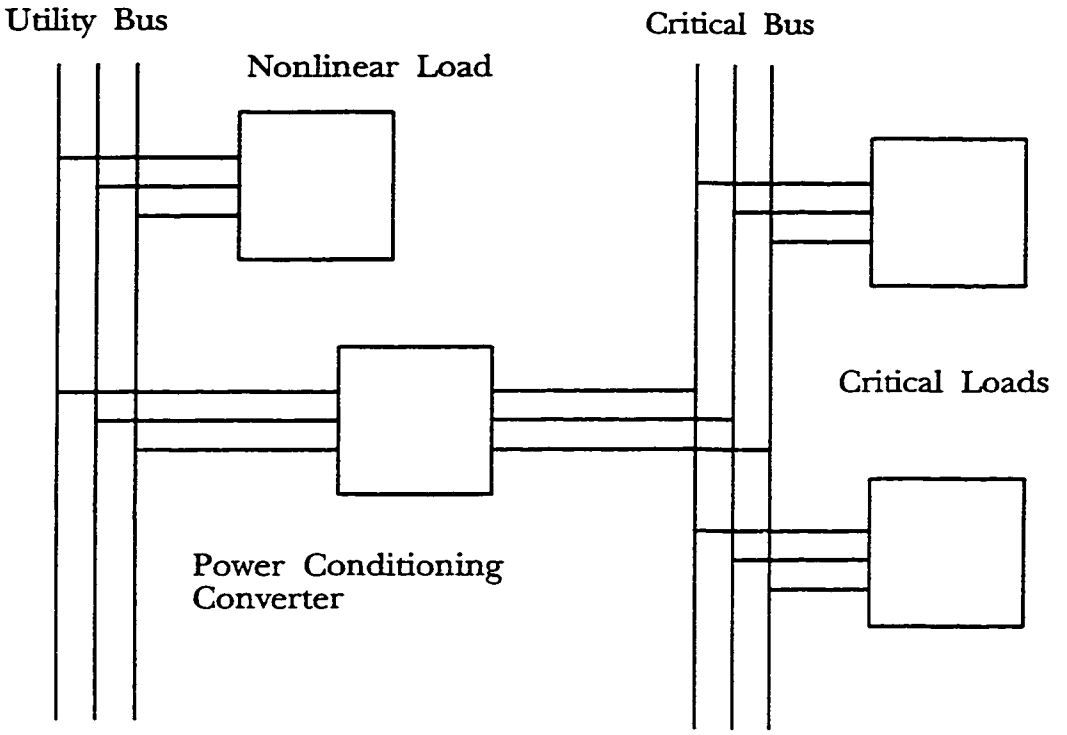


Fig. 1.1. A power conditioning converter placed between a utility bus and a sensitive load.

the current capacity of the bus. If the critical loads require only 2 per-cent of the maximum current, the utility bus is not overloaded but the current transients and resulting harmonic distortion may cause the more sensitive loads to malfunction. In addition to maintaining the quality of the power delivered , the conditioning converter can be connected to a battery and used to supply power when the utility bus fails. In this case the interface converter is referred to as a UPS. Thus, a power conditioning converter can supply the critical bus with clean, and consistent power without requiring the installation of a second isolated utility bus.

1.1.2. The Parallel Power Converter Circuit

Regardless of the type of power converter employed, the client system of critical

loads can be expected to experience a need to expand. At this point the engineer can either replace the existing converter with one of higher capacity or add another in parallel with the original. The addition of converter modules in parallel is attractive since it is economical (the original equipment investment is not lost) and more reliable (redundancy is increased). However, this strategy leads to a system of much greater complexity and with a wider range of design and performance criteria.

The diagram in Fig. 1.2 shows the basic configuration of the parallel converter structure required to meet the needs of the expanded critical bus. The converters themselves could be UPS modules, or ac - ac converters as drawn in Fig. 1.3. As shown, this system does not indicate how the power processed by the converters is to be controlled. Thus, circuits are required to provide for power sharing between modules, synchronization between converters, and shutdown in case of individual converter failure. Further, there is a variety of ways in which the loads can be connected to the protected bus. Since there are many possible combinations of converters, loads, and connection schemes, a review of the contemporary literature is required in order to identify the design approaches that can be applied to power conditioning applications.

1.2 Existing Parallel Converter Designs

The initial motivation for creating circuits composed of parallel converters was to obtain structures with a very high power output. Since it is difficult to extend the current capacity of switching converters by paralleling the switches themselves (Thyristors, Transistors), efforts were made to incorporate the switches into larger circuits that could be

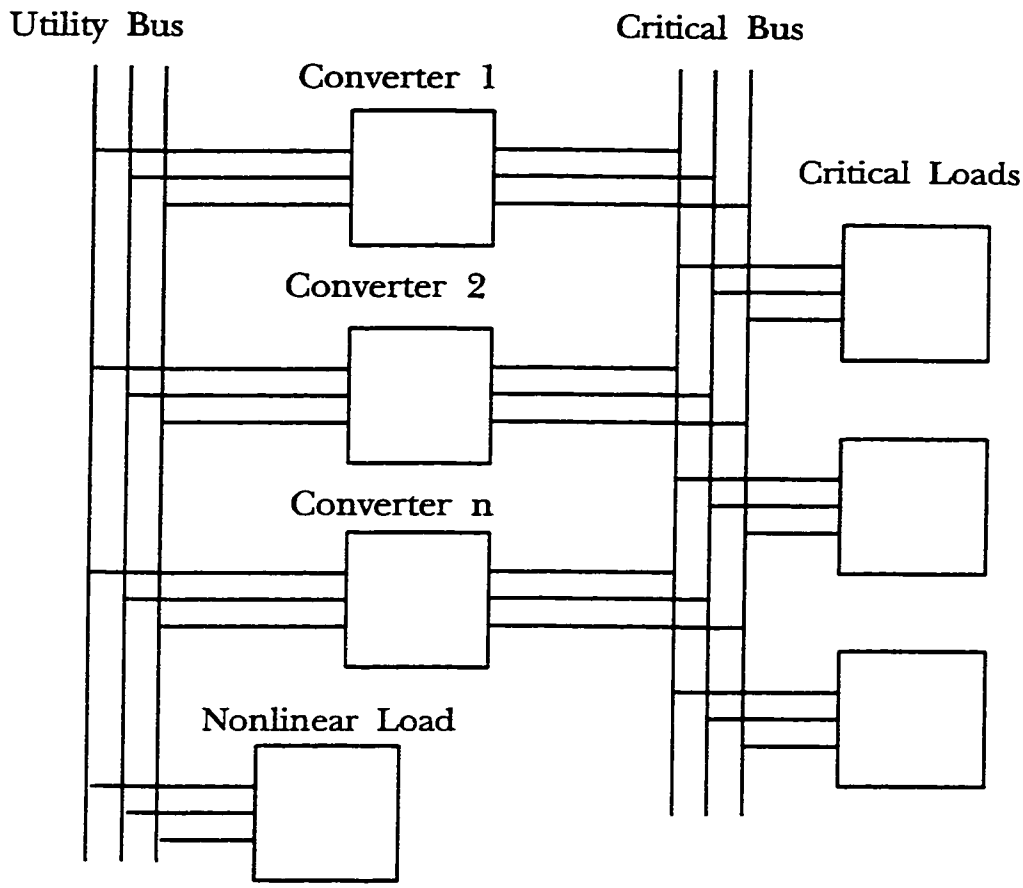


Fig. 1.2. The expanded system with multiple paralleled converters.

paralleled more easily. Immediately however, enhanced reliability was recognized as a desirable and exploitable product of the inherently redundant parallel configuration [4]. Reed and Sharma discuss both objectives and detail the basic reliability calculations [5]. Both of these sources are concerned with a parallel system composed of UPS converter modules. The UPS based system is a natural choice for the basic converter of the proposed topology and is given more attention by Fontaine [6]. Other types of power circuits can be paralleled however, and the research literature includes the complete range of conversion subcircuit categories.

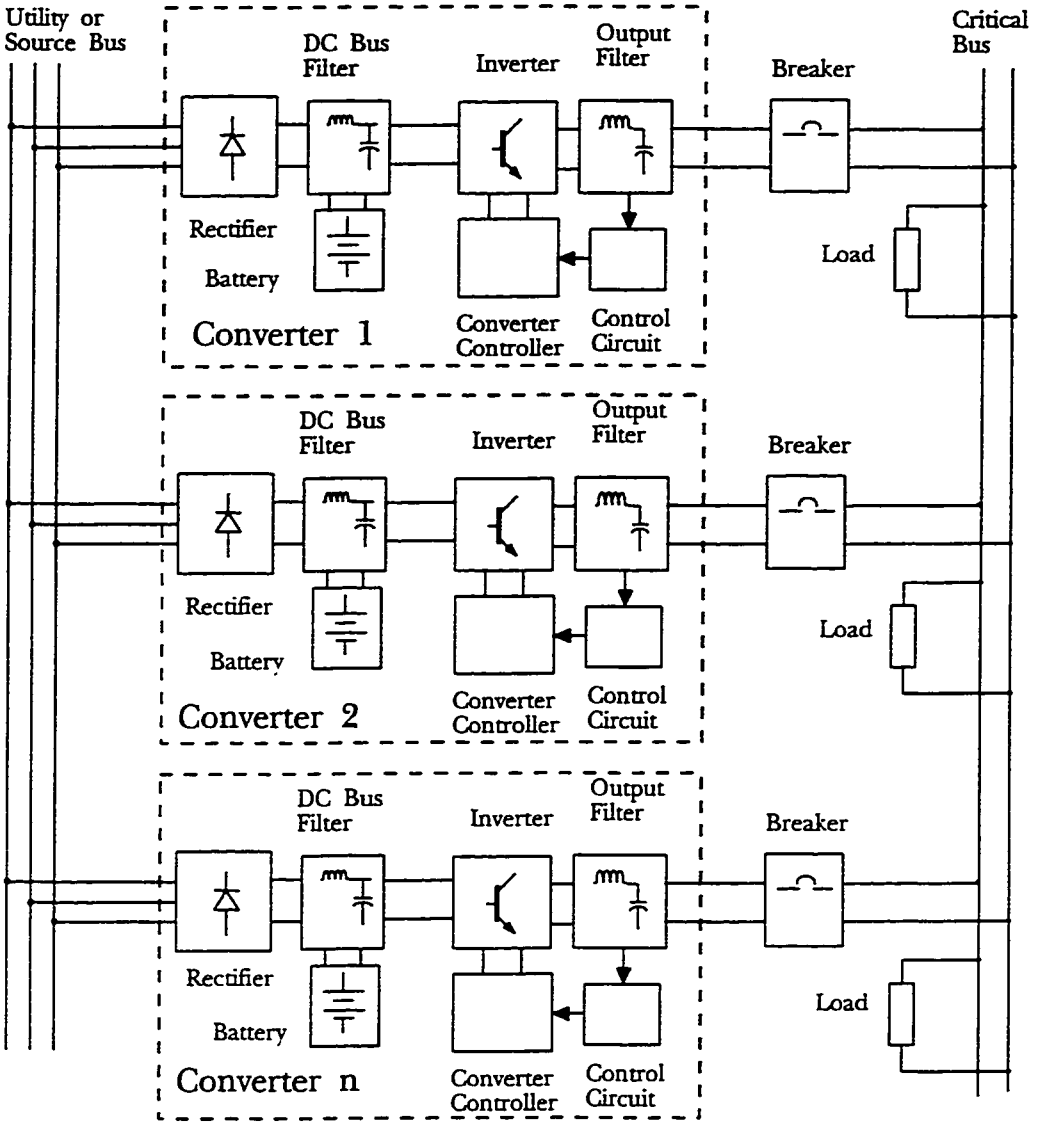


Fig. 1.3. Uninterruptible power supply modules connected in parallel.

1.2.1 Converter Circuits in Parallel Topologies

Converter modules used in parallel schemes correspond to the four categories of power processors: 1) ac-ac, 2) ac-dc, 3) dc-ac, and 4) dc-dc. In general, the ac-ac converters are represented by UPS circuits with a variety of control and bus connection schemes [7] [8]. High power rectifiers have been studied in parallel arrangements [9]. High power ac inverters using gate turn-off thyristors (GTO's) have been combined to drive large ac motors

[10] [11]. Much attention has been devoted to the problem of connecting dc-dc power supplies in parallel [12] [13]. Regardless of the type of converter module used, an effort is almost always made to present the analysis in a generalized fashion. In this way some aspects of the design of one type of converter can be applied to the other classes. Since the focus of this work is on mains-to-critical bus applications, research done in the area ac-ac power conversion is most relevant.

1.2.2. AC to AC Converters Connected in Parallel

Generalized ac-ac converters consisting of four stages: a rectifier and a dc-link filter, a voltage source inverter (VSI) and an output filter , a controller, and a breaker (static transfer switch) have been investigated with respect to control strategies, reliability, and power quality [14] [15]. This converter package is shown in Fig. 1.3 in a parallel configuration that can be used as a baseline for comparison with other approaches. Since this converter is to represent the basic approach to the paralleling problem in a low-power environment, it is modeled as a three-phase to single-phase circuit. The ideal circuit shown does not include any control elements which operate between the individual converters, hence, the parallel system is built using discrete converter modules. Also, this system is structurally flexible. Ideally, converter units can be added or removed as the total load on the critical bus is changed. Finally, since it is easy to add one more module than is necessary, the inherent reliability of the system is enhanced. The basic parallel-converter circuit then should exhibit three characteristics:

1) The system should be modular.

2) The proposed system should be expandable.

3) The reliability of the system should be greater than for a single module.

Tabisz, Jovanovic, and Lee [16] discuss additional characteristics of distributed power systems (DPS). Thermal management is easier to achieve on a per-converter basis since each power processor handles only a small part of the total load. Maintainability is another advantage of a parallel system that is due to the redundancy of the circuit. Converters that fail can be replaced without turning off the entire system. Finally, size reduction is possible because the smaller converter modules can use higher switching frequencies and smaller, lighter filter elements. The success of a system of parallel connected power converter units can be judged based on how well the scheme meets these criterion.

Holtz, Lotzkat, and Werner [7] have proposed a high-power (220 V, 300 A) multi-inverter scheme which features a single dc bus and a shared output transformer as shown in Fig.1.5 . This circuit, while being a parallel-based system, is not truly modular and the expandability is restricted by the presence of a common output transformer and a common dc bus. The use of the single transformer means that the output voltages of the individual converters must be in phase. A small phase difference between the output voltages will produce circulating currents with dc components. Since the primary winding of the transformer has a very low resistance (milliohms), a small dc voltage will produce large currents that can drive the transformer into saturation. Hence, the control scheme emphasizes a very fast inner voltage control loop and a magnetizing-current controller as a means of avoiding saturation of the transformer. The complete multivariable control system includes loops to control instantaneous output voltage, rms output voltage, and active and

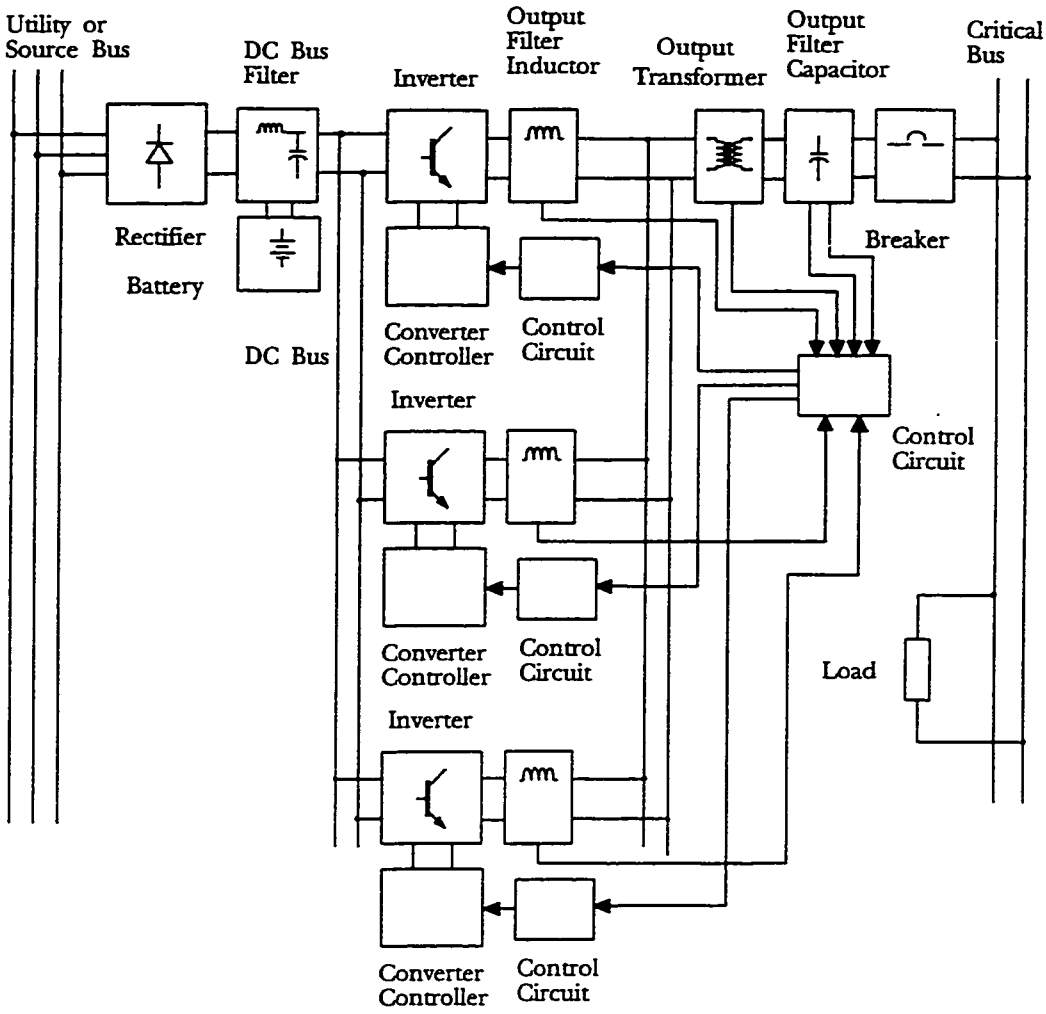


Fig. 1.4. Paralleled converters using a common dc bus and output transformer.

reactive load distribution.

To process the high power levels, the inverter circuit proposed by Holtz et al uses Darlington bipolar switches and a slow switching frequency of 1 kHz. Thus, control of the system is slowed, the filters must be larger, and the harmonics in the output waveforms require a more sophisticated multivariable control approach. Finally, since the system is subject to heating losses, the sensitivity of the system as a whole to the performance of certain components is increased. This circuit is essentially a design that is an extension of

the strategy of increasing the current-handling capabilities of bipolar transistors by paralleling them. Moreover, since the transistors themselves cannot be easily connected in parallel, single-phase full-bridge inverter modules can be used instead. A parallel connected system composed of independent converters has been described by Chandorkar, Divan, and Adapa [17]. The circuit is shown in Fig. 1.5 and can be characterized by three features:

1) There are independent dc sources for each converter.2) There is no control system intercon

3) The system requires a stiff output bus.

A stiff ac bus is defined as one where the ratio $\Delta P/\Delta f$ is between 2000 and 5000 MW per Hertz [18][19]. The authors show that by altering the frequency (droop) of each CM, the power angle can be controlled. A second independent quantity, the fundamental output voltage, is also used to produce a system that requires no communication between CM's. The requirement for a high power system indicates that this design may need adaptation for use in a low power environment with a weak load bus.

The scheme offered by the authors is important in that it offers a solution to the problems posed by the spatial distribution of the CM's and the loads attached to the critical bus. Moreover, communication is a problem when the converters and the loads are not located adjacent to one another and the distributed parameters of the transmission line must be taken into account. The modularity of this improved scheme is further enhanced by the use of independent dc sources fed by separate utility busses. However, the presence of these sources in weak ac systems may create harmonics and control problems.

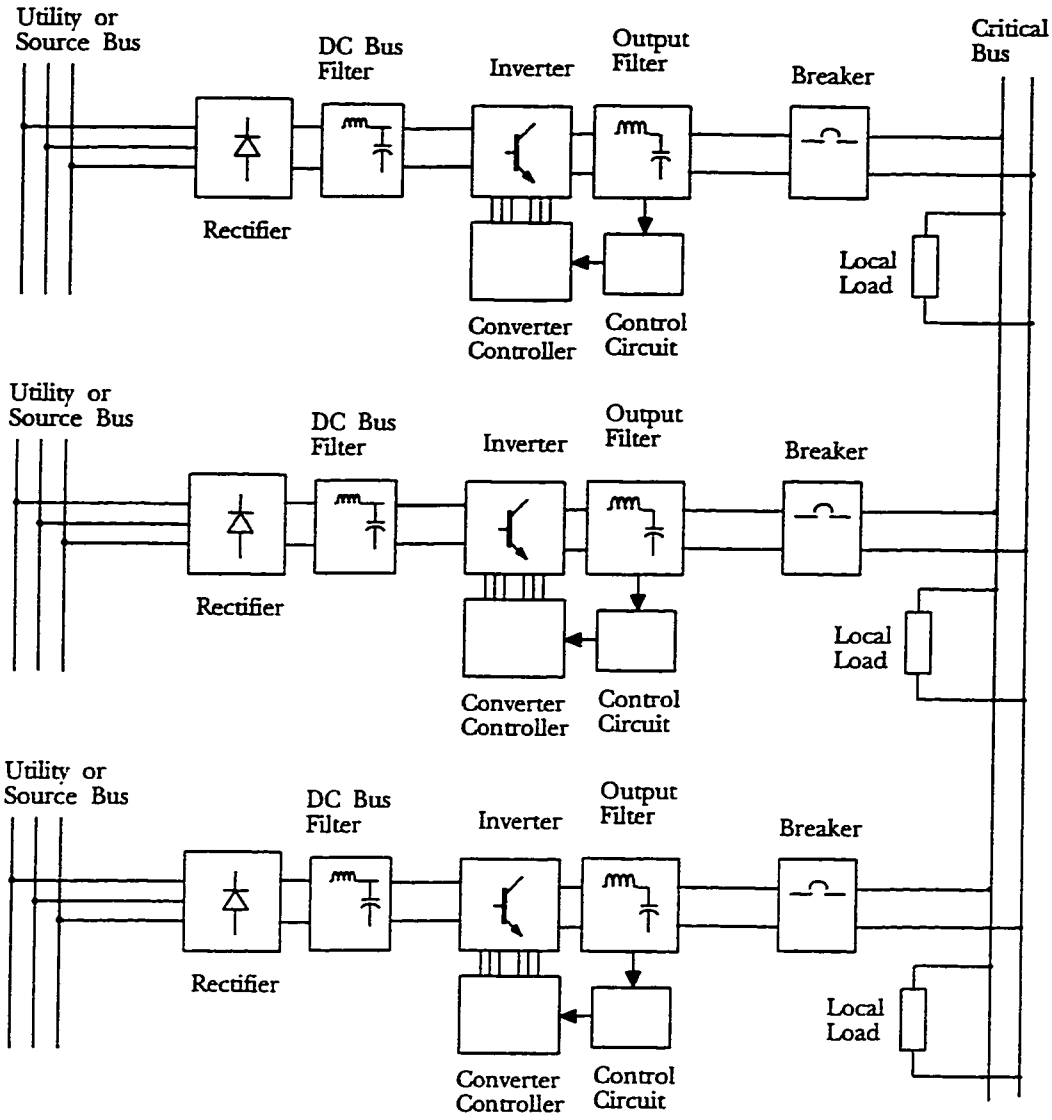


Fig. 1.5. Paralleled converters with independent dc sources, output filters and transformers. The transformers are included in the output filter block.

The modularity of the individual converters is maximized when the only connection between CM's is the load bus. Thus, a control strategy such as the one proposed above has the advantage of not requiring a separate 'third wire' for the control system. Perreault, Selders, and Kassakian have investigated the use of a frequency modulated (FM) signal that is broadcast on the load bus [20]. This technique makes it possible for the CM controllers

to have equal access to one or more important system parameters such as the total current delivered carried by the load bus or the voltage on the load bus. Although the authors restrict their investigation to a system of parallel connected dc-dc converters, they indicate that the method can be applied to ac - ac converter systems. Thottuvelil and Verghese have also researched the problem of paralleling dc-dc converters with current sharing and provide stability analysis for "democratic" and "master-slave" current sharing techniques[21]. Byungcho Choi discusses three approaches to paralleling dc to dc converters with defferent degrees of flexibility [22]. The most expandable system uses individual voltage references and exhibits the problem of sensitivity to this parameter. Of these sources the work of Perreault, Selders, and Kassakian offers a direct application to dc to ac converter systems since high voltage ac power systems commonly use their transmission lines as a communication channel [23] [24].

Parallel systems of dc to ac power converters using the signal injection method to pass control parameters between modules are discussed by Tuladhar, Jin, Unger, and Mauch [25]. The authors use the droop method of controlling the connected inverters, an approach common to high -power ac systems. In this approach, the frequency of the PWM is varied slightly to alter the real and reactive components of the power output of each CM. Finally, the problem of modeling single phase inverters with respect to their choice of control parameters (output current, output voltage, capacitor current) and control strategies are the subject of papers by Ryan and Lorenz, and Abdel-Rahim and Quaicoe [26] [27] [28].

1.2.3. Problems Associated with Parallel-Connected Converter Systems

Systems of parallel-connected UPS-based converters are compromised by a well recognized array of degenerative conditions [29] [30]. These abnormal characteristics include: i) circulating currents, ii) voltage source imbalances, iii) higher harmonic crosscurrents, iv) ripple in the dc bus and poor input power factor, v) magnetizing currents, vi) resonant conditions, and vii) dc bus overvoltages caused by converter regeneration. Moreover, component drift and differences in voltage and current references can cause voltage imbalance, frequency differences, and phase differences between the outputs of the interconnected converters. Kawabata and Higashino discuss the means of dealing with these conditions by using a variety of control schemes including a circuit that uses a combined minor-current loop and an outer voltage-loop. This approach offers overcurrent protection, load sharing, and fast output voltage control. The design and testing of a candidate system of converters must account for these potentially destructive conditions.

1.3. The Scope and Contents of the Thesis

Many low or medium-power sensitive loads are installed in locations where there is a need for a protected bus. At these sites a critical bus can be assembled by paralleling a large number of UPS type converters and placing them between the utility mains and a secondary power supply circuit. In this case the UPS CM's should have as little interconnection as possible while sharing the power equally and providing acceptable output voltage and current waveforms for a standard range of load types. The design of the basic CM should be as simple as possible while exploiting the performance capabilities of state-of-the-art components and operating modes. This Thesis will describe the design, analysis, and

performance of a system of parallel-connected modules that emphasizes three features:

1) The converters will use switches that can operate at high frequencies (20 kHz).

2) The system will have a minimum of interconnections between modules.

3) The system will use frequency-modulation (FM) in the current control loop.

Recent advances in the fabrication of high power switching semiconductors have pushed the upper switching frequency to 25 kHz [31]. The insulated-gate bipolar transistor (IGBT) and the metal-oxide semiconductor field-effect transistor (MOSFET) are two high switching-speed power devices whose performance characteristics are suitable for use in medium power converter circuits. In particular, the IGBT can switch up to 600 Amperes at 575 Volts with a switching frequency of 25 kHz. The proposed circuit will use a switching frequency of 10 kHz to 20 kHz.

The concept of modularity is important in terms of reliability, installation, expansion, and servicing of the paralleled CM's. Modularity is enhanced if the number of interconnections between modules can be held to a minimum. The scheme advocated will use only the input and output power lines to complete the control and power subcircuits. In order to eliminate the need for a 'three-wire' control communication arrangement, an FM signal will be used to regulate the current sharing between modules.

1.3.1. General Description of the Proposed System

The design of the candidate CM is approached by outlining the output power requirements, the available input power, the required transient response, the topology, and the anticipated stresses caused by the parallel connection of the individual CM's. To

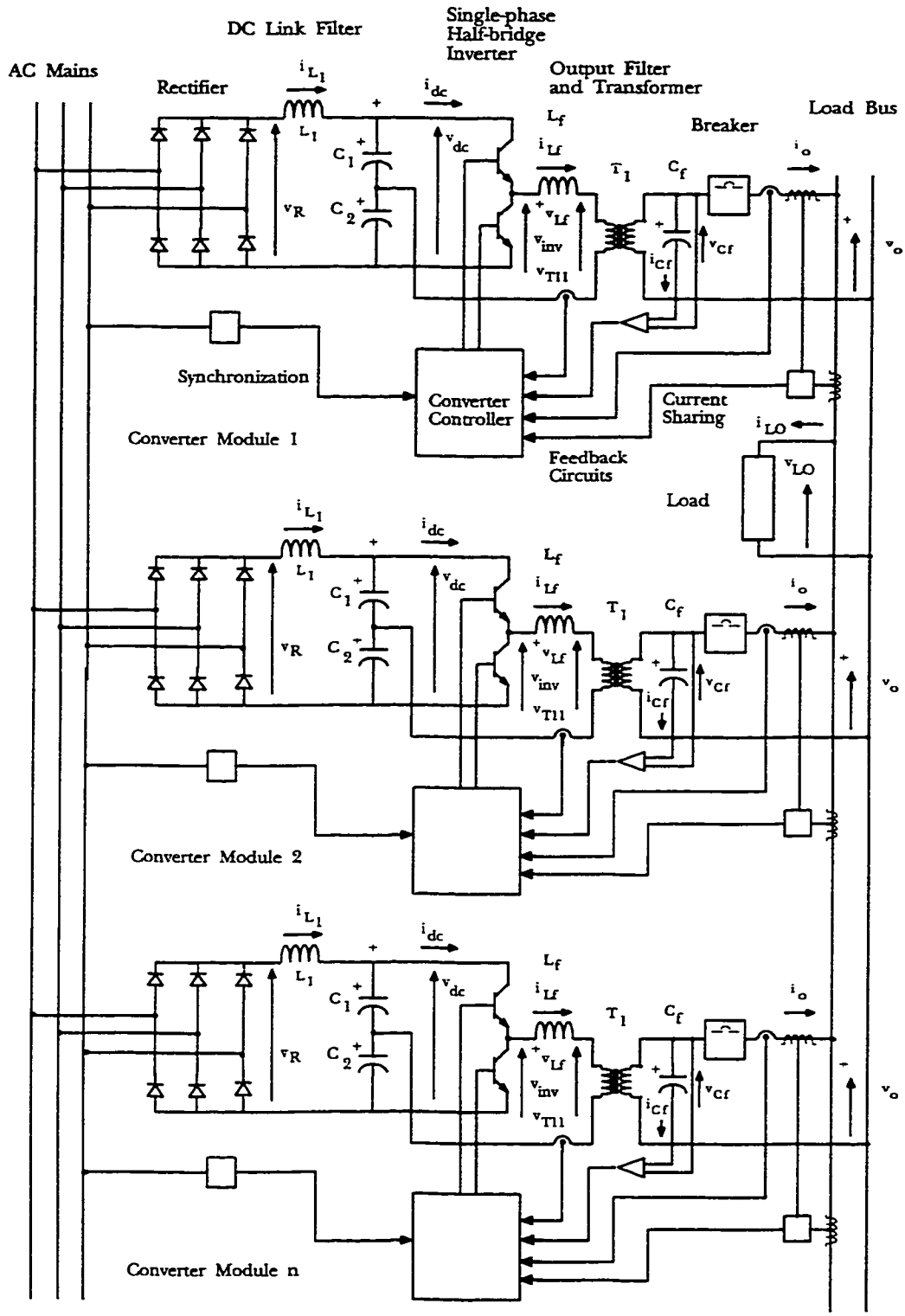


Fig. 1.6. The proposed system of parallel connected converters.

investigate the strategy of paralleling UPS type converters operating in the low-power (less than 10 kVA) to medium-power (10-150 kVA)range, a candidate system is constructed as shown in Fig 1.7. This basic system is composed of a number of modules placed between a three-phase mains (208 V rms phase-phase) and a single-phase load bus (120 V rms phase-neutral). Each converter section is expected to deliver 500 VA to the load bus. Thus, the per-unit (pu) values referred to output of the individual converters are chosen to be 500 VA for 1 pu output power, 120 Vac rms is the per unit output voltage, and the per unit load current is 4.17 A rms. This topology is typical of an installation expected to be found in a low-to-medium power environment. Since the power units are simply UPS modules without the batteries, their performance and design specifications are based on the standards of the UPS industry [32] [33] [34]. Thus, the converter is expected to draw its power from a three-phase three-wire bus. Since enhanced modularity is a goal of the candidate design, the CM's are equipped with individual rectifier sections although they share a common mains bus and are not to be classified as 'stand alone systems'.

Converters of this type are expected to recover to within five percent of the rated load voltage in a period not greater than one-half cycle (8.33 ms) for a load application or removal of 100 percent. The loads are separate and have a range of linear and nonlinear operating characteristics.

If the paralleled converters are to share the load equally, then their respective output voltages and currents must be identical. Since the output voltages share the same critical or load bus, they will tend to assume the same magnitudes and phase. The individual output currents of the converters, however, will not fall into synchronism and must have a template

that will provide a current reference with respect to the average amplitude and phase required of all the converters sharing the output bus. The proposed circuit will include a frequency modulated communication scheme that will sample the individual currents amplitude and phase, determine the average amplitude and phase, and present this information to each converter as the current reference. The proposed current sharing technique will enhance the modularity of the system because it requires no interconnection between the converter modules other than the output bus.

1.3.2. Specifications of the Proposed System

The study of the fundamental properties of a system of parallel connected converters is carried out using a CM consisting of four components:

1). A full-bridge rectifier is coupled to a dc bus filter.

2). A single-phase half-bridge inverter is connected to an output filter and a step-up isolation transformer.

3). A control circuit operates on both the CM and the system level and a frequency modulated scheme is used to communicate between converters.

4). A static transfer switch connects the CM to the load bus.

A converter module of the type to be tested is shown in Fig 1.6 . The individual converters and their respective controllers are designed to take advantage of a switching frequency of 10 kHz and the harmonic characteristics of the half-bridge inverter. Although the circuit is modeled as a UPS system, the battery and the elements needed for connection with an alternate power source, such as a generator, are not included. Moreover, the prototype

system is chosen to test the characteristics of power processors connected in parallel and not the full range of UPS performance issues.

1.3.2.1. The rectifier and dc filter

Since the system under test is one that would be used as an interface between a three-phase bus and a single-phase load, the rectifier is a full bridge type with a low-pass dc bus filter. Typically, the rectifier assembly and filter specifications require a dc bus with less than 5.0% THD and dc regulation ± 1% for ± 10% ac voltage change, for ± 5% input frequency change, or for 10 - 100% load variations [32, 37]. Moreover, the dc supply must be stable enough for the inverter section to attain its performance objectives.

1.3.2.2. The inverter and output filter

The advantage of the single-phase half-bridge inverter is that there is no dc component in the output current since the bus capacitors pass only the ac components. Moreover, this allows the designer to neglect the leakage inductance in the isolation transformer and to have less concern for transformer heating and saturation. A further advantage is gained by using a switching frequency of 10 kHz. A higher switching frequency extends the bandwidth (BW) of the output filter and allows the designer to use smaller filter components. When the power requirements of a single-phase inverter are large, a full-bridge configuration is preferred so that the load current can be shared by two switches rather than one. However, since the CM is intended for low to medium-power range applications, current stresses on the switches do not pose a problem. The switches can simply be chosen

so that their ratings are 150% to 200% of the required capacity.

The output filter of the converter includes a transformer for isolation and voltage matching. Since the candidate system is chosen to reflect the performance of a basic UPS configuration, the presence of the transformer in the output stage is required to investigate the effects on the total system performance.

1.3.2.3. The control circuit

The control circuit emphasizes a very fast response characteristic and a simple structure. The controller employs two types of control mechanisms - a combination of two current-control loops and an outer voltage-loop. A basic sinusoidal pulse-width-modulation (PWM) scheme is to be used to control the switching elements. In order to improve the dynamic response of the system, a switching frequency of 10 kHz is to be used. This control approach will serve as a base-line for the evaluation of the control design with respect to response time, power quality, and load sharing. In order to enhance the modularity of the proposed scheme, the current sharing parameters will be passed between the individual converter controllers by means of frequency modulated signals on the output bus.

1.3.2.4. The static transfer switch and load

The CM is connected to the critical bus by a static transfer switch (breaker). A standard transfer switch consists of two pairs of silicon controlled rectifiers (SCR's) connected in a parallel back-to-back configuration. One terminal of the switch is usually connected to the critical bus and the other to the CM output. In the test circuit, the standard

static switch has been replaced by one which consists of a diode bridge and a semiconductor switch. The switch must be evaluated with respect to its sensitivity to noise and its response time. The choice of semiconductor switch could be either MOSFET or IGBT. The loads typically have power factors in the range of 1.0 to 0.8 -lagging power factor. Although this criterion is assumes that the load is linear, there are other performance standards which reflect the need for a UPS to compensate for the switch-mode power supplies usually found in computers. Such a requirement is that the converter provide a better than three-to-one crest-to-rms single phase load current at 70% to 80% rated power.

1.4. Contributions of the Thesis

This Thesis combines three techniques found in the field of power and power electronics and uses them to provide an original approach to the design of parallel dc to ac converter circuits:

1) The scheme exploits high-frequency switches (IGBT) and carrier PWM.

2) An FM communication scheme is used in the current sharing control loop.

3) Inter-converter control parameters are communicated over the output bus.

To the best of the authors knowledge this approach has not been described previously in the literature and represents a useful contribution to the problem of devising modular paralleled converter systems. Circuits composed of parallel-connected stand-alone power conditioning converters including UPS converters, are attractive because they are expandable, they offer more reliability as a result of their redundancy, and they can process higher levels of power. In order to realize these advantages, the modularity and performance of the individual

converters and the integrated systems should be emphasized. The proposed circuit configuration shown in Fig. 1.6 is used to investigate the advantages of operating a UPS-type single-phase half-bridge inverter based converter at a 10 kHz switching frequency using IGBT switches and an FM communication scheme to transmit the current sharing signal over the output power bus. Such a system offers the advantage of i) modularity because the need for added control wiring is eliminated and ii) better performance because the higher switching frequency reduces the need for filtering components and improves the response of the control circuits.

1.4.1. The Development Strategy of the Thesis

This Thesis investigates the performance of a converter circuit and a multi-converter parallel connection scheme. Thus, the contribution of this work is based on the integration of three design elements into a single modular converter that can be paralleled easily:

1) The CM is based on a single-phase half-bridge topology using a simple control scheme with an independent dc bus and input and output filters.

2) IGBT switches are operating at a switching frequency of 10 kHz - 20 kHz.

3) An FM communication scheme is used to form a control loop for current sharing.

This approach yields both a simplified solution to the problem of connecting low power converters in parallel and a benchmark for comparison with more complex circuits and control strategies.

The feasibility of the proposed scheme is established by calculation of the basic circuit parameters and by computer simulation of the control circuits, the CM, and a

paralleled system. Finally, a prototype system is built and used to demonstrate the operation of the proposed scheme and the validity of the performance predicted by the simulation software.

1.4.2. The Contents of the Thesis

This Thesis is composed of seven chapters and an appendix. Each chapter represents a discreet step in the process of designing and testing a system of modular ac power converters:

1) The proposed system is introduced.

2) The power system is designed.

3) The basic converter module controller is designed.

4) The FM scheme and system controller are designed.

5) The basic converter is tested using computer simulation.

6) The system of converters is tested by simulation and a prototype circuit.

7) The process is summarized.

The first chapter introduces the topic of paralleled power converter structures and gives examples of previous work done in the field. At the conclusion of this chapter a CM and a general parallel connection scheme are proposed. The three step design process begins in Chapter 2 which describes the requirements of the basic power circuit and the expected performance of the single-phase half-bridge converter that is the core of the CM. The third chapter includes the calculation of the control circuit parameters and a computer simulation of the performance of the converter controller using PC based software (MATLAB). Chapter

4 details the design of the converter modules connected in a parallel system including the implementation of the FM communication scheme. The third stage of the design process is done in Chapter 5 and Chapter 6 where the CM and the complete system are simulated using software designed for power applications (PSIM). The construction of the experimental test circuit and the results of the testing are also given in Chapter 6. Finally, Chapter 7 summarizes the complete work, compares the experimental results with the predicted performance and suggests areas for future work. The Appendix gives the details of the construction of the prototype circuit.

2. DESIGN AND OPERATION OF THE DC TO AC INVERTER

2.1 The Initial Design Stages

The design of a system of paralleled converters is done in three steps and begins by first considering the nature of the power circuit which is the basic system unit. Secondly, the individual converter module (CM) design is completed, then the discussion of the CM and system-level control can proceed. Finally, the operation of the entire system is analyzed and the performance of the control circuits investigated. This chapter shows how the first stage is accomplished. The operating elements of the basic CM are described and the design and performance of each CM subsection is detailed.

2.2. Design of the Basic Converter Module

The individual CM to be used is a single-phase half-bridge inverter as shown in Fig. 2.1 . The CM is composed of four subcircuits:

1) The rectifier and dc-bus filter section.

2) An inverter stage with switching controls.

3) An output filter and transformer.

4) The static transfer switch and load.

The design of each of these subsections is based on the objective of a modular, simplified, yet effective paralleling scheme.

2.2.1. Fundamental Circuit Ratings

The per-unit (pu) values are defined for a CM that delivers 500 VA to the load bus at 120 Vac rms. Other circuit and system operating parameters are referred to those common to the UPS industry. The output power factor, the filter component ratings, and the input power factor should be included in the evaluation of the CM. Although the design procedure described here does not treat the matter of input power factor, the parameter is an important one and is discussed by other authors [33]. The efficiency of the individual modules will fall in the range of 75% to 85% for operation with loads of 50% to 100% (0.5 pu to 1.0 pu). Typically, the output power factor will be 1.0 to 0.8 lagging and the input power factor should be less than 0.9 for loads of 0.5 pu to 1.0 pu . The basic operating parameters for each CM are summarized in Table 2.1 below.

2.2.2. Component Selection

The elements which are included in the rectifier, the input filter, the output filter, the inverter, the transformer, and the sensing circuits are chosen so that each section of the CM can perform its function under worst-case conditions. Essentially, this means that each inverter can operate at 1.50 pu load conditions while the voltage and current ratings of the switches, inductors, and capacitors are sized to accommodate transients caused by load switching and load generated harmonics. The worst-case conditions for each circuit section and the subsequent component size calculation will be noted as each circuit is designed.

2.2.3. Auxiliary Subcircuits

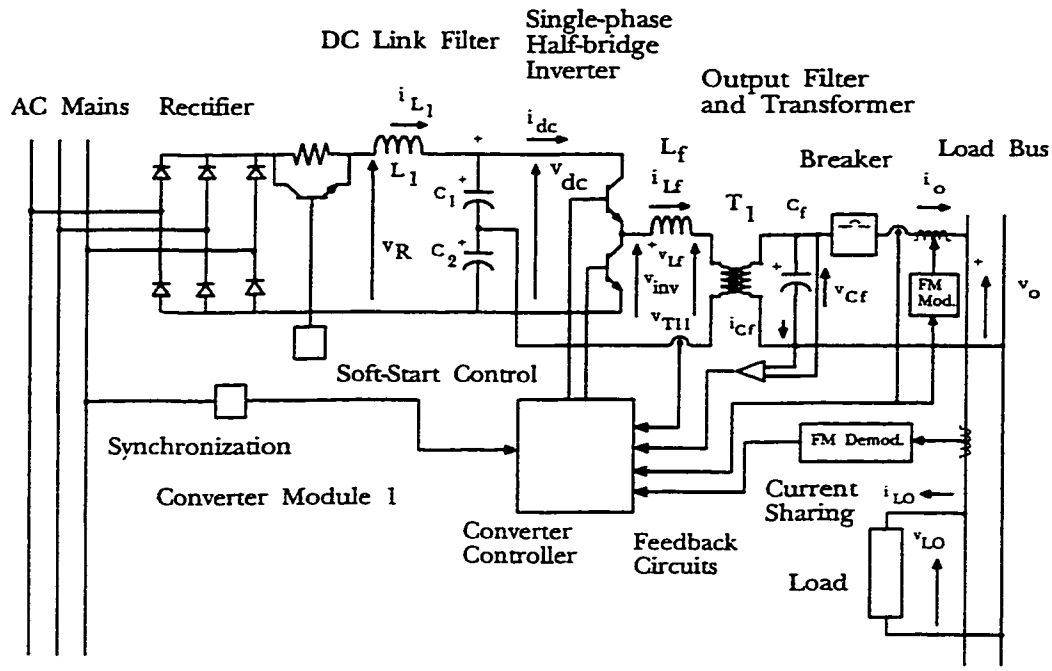


Fig. 2.1. The converter module.

The auxiliary circuits include the soft-start or walk-in circuit, individual switch fuses, the synchronization circuit, and the solid-state transfer switch. These elements are not developed as part of this research, however, they are required for the circuit used in the software simulation as well as the experimental prototype. The design of each of these elements will be noted as required for the general control scheme. The designs will conform to the standards of the UPS industry and no special designs will be incorporated for this research [32].

2.3. The Rectifier and DC Bus Filter

The three-phase rectifier and filter shown in Fig. 2.2 are designed to serve each CM to be connected in parallel. The first decision is to choose either a common dc-bus for all of the paralleled CM sections or an independent dc-source for each converter. A single dc

Table 2.1. THE CONVERTER MODULE PARAMETERS

Specification	Value
Output Frequency	60 Hz
Efficiency	75% to 85%
Normal Load Operating Range	0.5 to 1.0 pu (64% nominal)
Input Power Factor	Less than 0.9
Output Power Factor	1.0 to 0.8 Lagging
Switching Frequency	10 kHz

bus minimizes the possibility of phase variations between the paralleled converters and simplifies the construction of the prototype circuit and the analysis of the system as a whole. However, the modularity of the entire system is reduced since the number of converter sections is limited by the capacity of the single rectifier. Alternatively, the use of individual rectifier sections allows each CM to operate as a more independent section. Thus, each CM is equipped with its own dc source having the same characteristics in terms of ripple and harmonic spectra. This is accomplished at the cost of a larger filter for the dc bus.

2.3.1. The Input Filter

The input filter is designed to maintain a low input power factor (1.0 to 0.9) when the load is inductive since this creates the poorest input current waveforms. The filter consists of an inductor placed in series with each phase of the input ac source. This inductor is set to be equal to the value of the dc filter inductance. Although the value is very large and does not represent an optimal approach to the problem of input power factor control, the use of

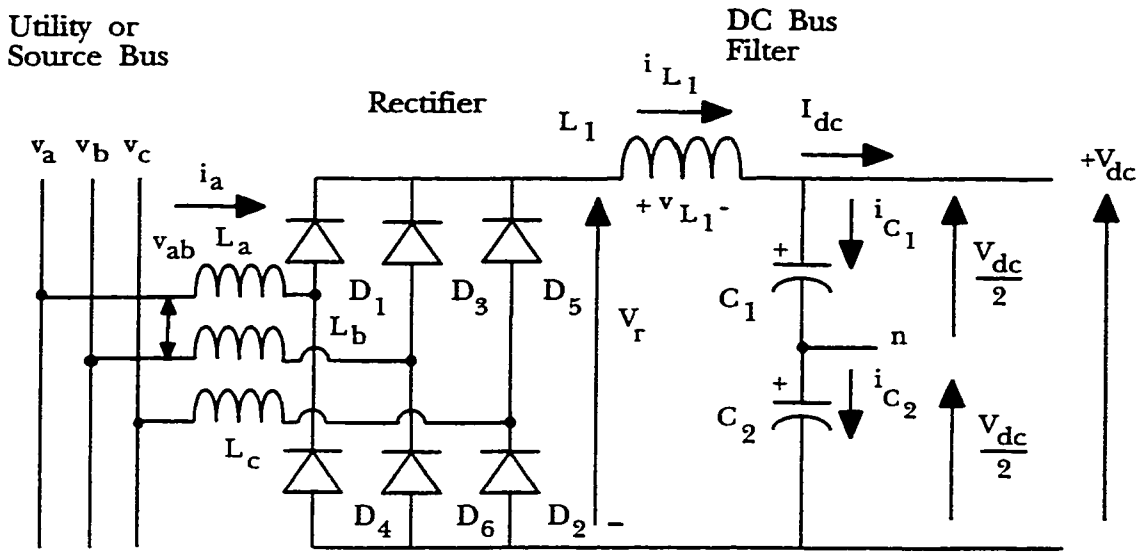


Fig. 2.2. The rectifier and dc bus.

a large input filter inductor ensures that the control scheme will function as planned using a basic input ac filter.

2.3.2. The Rectifier and DC Filter

The rectifier is a full-bridge three-phase type with a second order LC filter. The average output voltage with no load is

$$V_{do} = \frac{3}{\pi} V_{max} \tag{2.1}$$

where V_{max} is the maximum value of the phase-to-phase voltage v_{ab} in Table 2.1 [35]. The six-pulse rectifier produces an even output waveform with only the cosine terms present in the Fourier representation of the no-load voltage V_r. The cosine terms are given by

$$a_m = \frac{1}{\pi / q} \int_{-\pi/q}^{\pi/q} V_{max} \cdot \cos \omega t \cdot \cos m \omega t \, d\omega t \qquad \textbf{(2.2)}$$

where

q is the pulse number of the rectifier (6),

n is given by 0, 1, 2, ...,

m is the product nq,

V_{max} is the maximum value of the line-to-line voltage v_{ab} , Fig. 2.2

This integral can be reduced to

$$a_m = \frac{2 q V_{max}}{\pi (m^2 - 1)} \left[- \sin \frac{\pi}{q} \cdot \cos \frac{m \pi}{q} \right] \qquad \textbf{(2.3)}$$

$$V_{do} = \frac{q}{\pi} \sin \frac{\pi}{q} V_{max} \qquad \textbf{(2.4)}$$

Note that the dc component $V_{do} = \frac{a_0}{2}$ is found by letting m = 0.

The voltage for harmonic n is given as

$$v(\omega t) = V_{max} \frac{q}{\pi} \sin \frac{\pi}{q} \left[\frac{2}{m^2 - 1} \right] \left[- \cos m \frac{\pi}{q} \right] \qquad \textbf{(2.5)}$$

The 6-pulse rectifier has harmonics whose number is a multiple of 6. The values of the 6th, 12th, and 18th harmonics are given in Table 2.2 below. The total RMS harmonic content (THD) is .0418 V_{do} for the 6-pulse rectifier [36].

Table 2.2. AMPLITUDES OF THE RECTIFIER HARMONICS

Harmonic Number, *n*	Harmonic Amplitude
6	.0571 V_{do}
12	.0140 V_{do}
18	.0062 V_{do}

The dc bus filter shown in Fig. 2.2 is designed to keep the lowest order harmonic (LOH) to at a value which will ensure that the THD is below 5%. Since the amplitudes of the harmonics decrease rapidly as *n* increases, the THD can be approximated using the value of the 6th harmonic. Assuming that the commutation and rectifier device losses are not greater than 1% of V_{do}, then V_{do} is taken to be the actual dc component of V_r. The ratio of the amplitude of the 6th harmonic component of the rectifier filter output voltage, V_{dc} to the 6th harmonic component of V_{do} yields

$$\frac{V_{dc6}}{V_{do6}} = \frac{1}{\omega_h^2 LC - 1} \tag{2.6}$$

Where ω_h is the frequency in radians of the harmonic of interest (2242 rad/sec). The product of the inductor and capacitor values is

$$LC = \frac{1}{\omega_h^2}\left[\frac{V_{do6}}{V_{dc6}} + 1\right] \tag{2.7}$$

The product LC can be used to find the break frequency, ω_n, of the filter where

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{2.8}$$

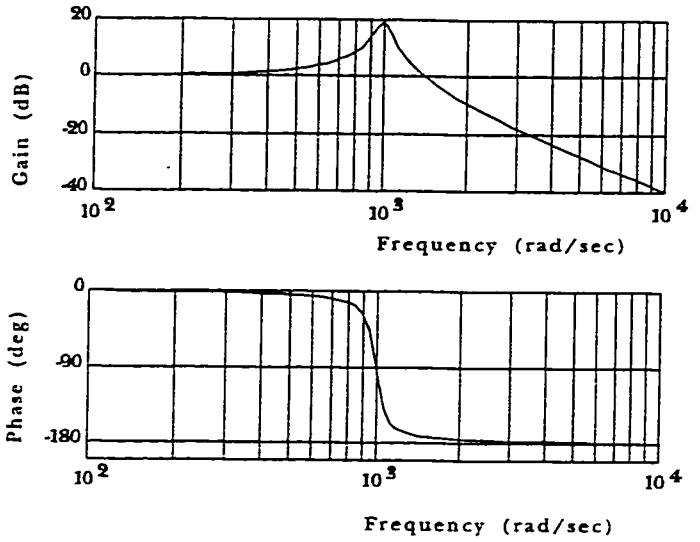


Fig. 2.3. The simulated output of the rectifier circuit.

The value of *LC* is found from (2.7) and the break frequency can be verified from (2.8). The combination of the filter elements can now be analyzed to determine the relative values of the inductor and the capacitor impedances.

2.3.3. Rectifier and DC Bus Component Values

In order to reduce the THD of the dc bus voltage from 5.7% to 1.7%, the ratio V_{dc6}/V_{do6} is set to 1/3. The value of the product LC is then found using **(2.7)**. The series combination of the capacitors C_1 and C_2 is given by C where $C_1 = C_2 = 2C$. C is chosen so that X_C is to be approximately .1 per-unit (pu) and the impedance, X_L, of the filter inductor L_1 is .01 pu. This combination of values yields a filter with an attenuation of -10 dB at the frequency of the 6th harmonic (2242 rad/sec). The frequency response of this filter is shown in Fig. 2.3. The break frequency of this filter is approximately 1.0 k rad/sec. The design of this filter is based on the performance of the rectifier when attached to a 1.05 pu

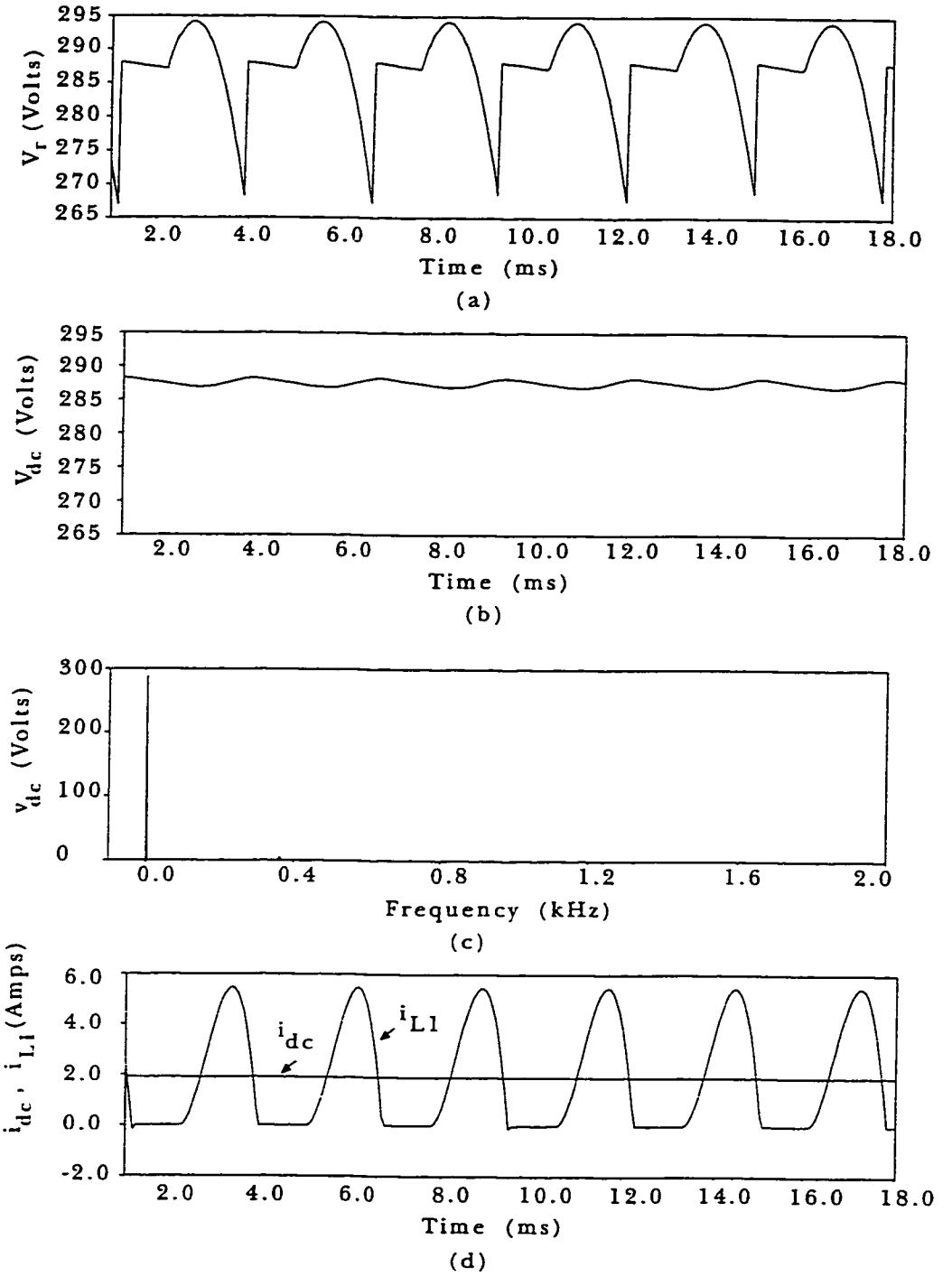


Fig. 2.4. The rectifier and dc filter waveforms. (a) The rectifier voltage. (b) The dc filter voltage. (c) The dc voltage spectrum. (d) The dc currents.

load with a unity power factor (PF). Such a load is the equivalent of the inverter operating at 95% efficiency and a 1.0 pu resistive load. The choice of a large filter capacitor is usually

made since the capacitor controls V_{dc} directly.

2.3.4. Simulated dc source performance

The performance of the rectifier and the dc filter are simulated using a personal computer (PC) based simulator. The results of the simulation are shown in Fig.2.4 . The output waveform for the filtered dc bus voltage, V_{dc}, indicates that the ripple has been reduced to 0.5% . The harmonic spectra indicate that, if the THD of the dc voltage is taken as the amplitude of the 6th harmonic, then the THD is 0.1%.

2.3.5. Construction of the DC Source

The important parameters for the design of the rectifier and the dc filter are: the diode current ratings, the filter inductor current rating , and the filter capacitor voltage and current rating. The discontinuous nature of the rectifier current shown in Fig. 2.4 indicates that the rectifier diodes should be rated at 2.5 to 3.0 pu amps in order to ensure that they will be able to withstand the transients created by reactive loads. The filter inductor should have a similar current rating of 2.5 to 3.0 pu. The voltage rating of the filter capacitor should be on the order of 4.0 to 5.0 pu voltage to handle overvoltage conditions at start-up.

2.4. The Inverter and the Switching Control

The important circuit elements to be decided in the CM are the switches and the PWM switching pattern. Thus, the inverter section chosen for this scheme is a single-phase half-bridge inverter driven by a sine pulse-width-modulation (SPWM) switching scheme.

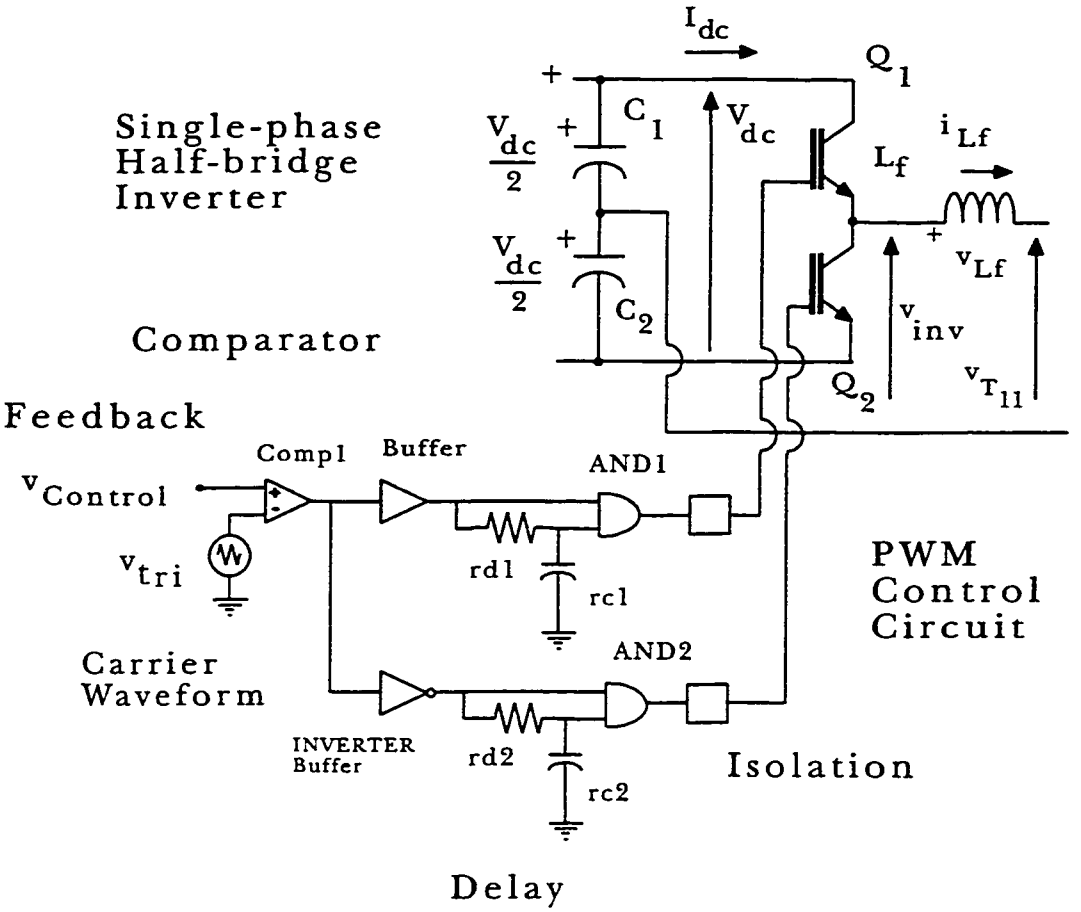


Fig. 2.5. The inverter and PWM switching circuit.

The half-bridge configuration is used for its simplicity, its low parts-count, and because the circuit can be used as a base-line for comparison with more sophisticated designs. The SPWM switching scheme is also chosen for its base-line characteristics - it is the simplest approach that can produce the required output waveforms.

2.4.1. The Model of the Inverter and Switching Circuit

The circuit of Fig. 2.6 shows how the inverter and the switching circuit are connected. The complete circuit is shown in Appendix I . The circuit is composed of a single-phase half-bridge inverter that uses two IGBT switches. Isolation of the PWM controller from the

power circuit (switches Q1, Q2) can be done by pulse transformer, opto-isolator, or an integrated circuit (IC) specifically designed to drive MOS gated power switches such as the IGBT. The input to the PWM control circuit is from the feedback circuits described in Chapter 3. The feedback signal is compared with a carrier waveform and the modulated output is sent to the switches through two paralleled inversion and delay sections. The half-bridge topology has the advantage that the arrangement of the capacitors in the dc bus filter will block the dc component in the output current. This feature is useful in designing the control circuit (Chapter 3) since there is less chance that the output isolation transformer will saturate on the primary side.

2.4.2 The PWM Switching Scheme

The IGBT switches feature a maximum combined turn-on and turn-off time of less than 5 μs. At 10 kHz a 30 V peak-peak triangular wave allows a 10 μs pulse at 80% modulation (12V). This indicates that the IGBT switches are capable of delivering a switching pulse in 10 μs (turn-on to turn-off) and can be used for a 10 kHz switching scheme. The feedback signal, $v_{control}$, is essentially a 60 Hz sine wave that is taken from the control circuit. Thus, the PWM switching pattern used by the power switches is developed by comparing the modulating signal, $v_{control}$, from the control circuit with the carrier signal, a 10 kHz triangular waveform, v_{tri}. The carrier or switching frequency is identified as f_s and the modulating frequency is f_1 which is the fundamental of the output voltage of the inverter section. The amplitude modulation ratio, m_a, is defined as

Table 2.3. HARMONIC CONTENT OF INVERTER OUTPUT

Harmonic, h ($m_a = 0.6$)	Frequency, f_h, Hz	$V_{inv\,h}$ /($V_{dc}/2$)	$V_{inv\,h}$, Vpk
1	60	0.6	61.09
m_f - 2	9.88 k	0.131	13.339
m_f, 167th	10 k	1.006	102.434
m_f + 2	10.12 k	0.131	13.339
2 m_f - 3	19.82 k	0.071	7.229
2 m_f -1	19.94 k	0.370	37.675
2 m_f	0.0	0.0	0.0
2 m_f +1, 334th	20.06 k	0.370	37.675
2 m_f +3	20.18 k	0.071	7.229
3 m_f - 4	29.76 k	0.047	4.786
3 m_f - 2	29.88 k	0.203	20.67
3 m_f, 500th	30 k	0.083	8.451
3 m_f +2	30.12 k	0.203	20.67
3 m_f +4	30.24 k	0.047	4.786

$$m_a = \frac{V_{control}}{V_{tri}} \tag{2.9}$$

where $V_{control}$ and V_{tri} are the peak amplitudes of the modulating and carrier waveforms. Also, the frequency modulation ratio m_f is given by

$$m_f = \frac{f_s}{f_1} \tag{2.10}$$

where f_s and f_1 are the carrier frequency and the fundamental of the modulating frequency. The desired voltage at the load is 120 V rms (169.7 V pk) and the turns ratio of the transformer is 1:2. This means that the required fundamental component of the voltage output by the inverter is 60 V rms. Using these values, the modulation index of the PWM scheme can be found from

$$m_a = V_{inv} \cdot \frac{2}{V_{dc}} \tag{2.11}$$

Since m_f is very large, the PWM scheme is classified as asynchronous and for $m_a = 0.6$ the harmonics can be calculated from

$$V_{inv\ rms\ h} = \frac{1}{\sqrt{2}} \cdot \frac{V_{dc}}{2} \cdot \frac{V_{inv\ \max\ h}}{\frac{V_{dc}}{2}} \tag{2.12}$$

The values of the first 13th terms of $V_{inv\ rms}$ and the values of the normalized harmonic coefficient are given in Table 2.4 for $m_f = 167$. Note that for the m_f given, the possibility of subharmonic currents exists for certain loads such as large ac motors [37].

2.4.3 Inverter Component Values

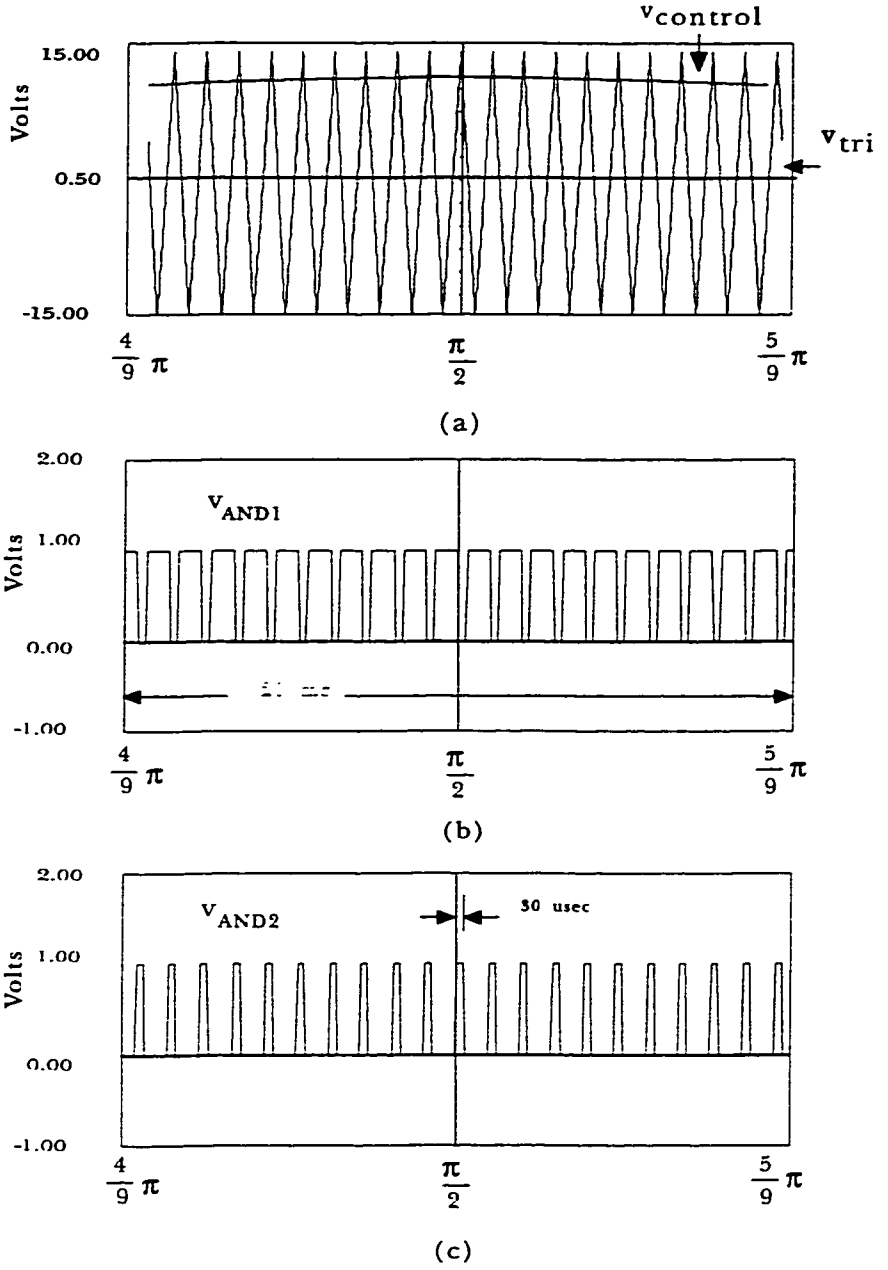


Fig. 2.6. The inverter switching pattern. (a) The modulation and carrier voltages. (b) Detail of the upper switch gating signal. (c) The lower switch gating signal.

The inverter ratings must take into account the rms and peak currents of the switches and the accompanying thermal stresses. The single-phase half-bridge topology places added stresses on the switches and the high switching frequency increases the commutation losses.

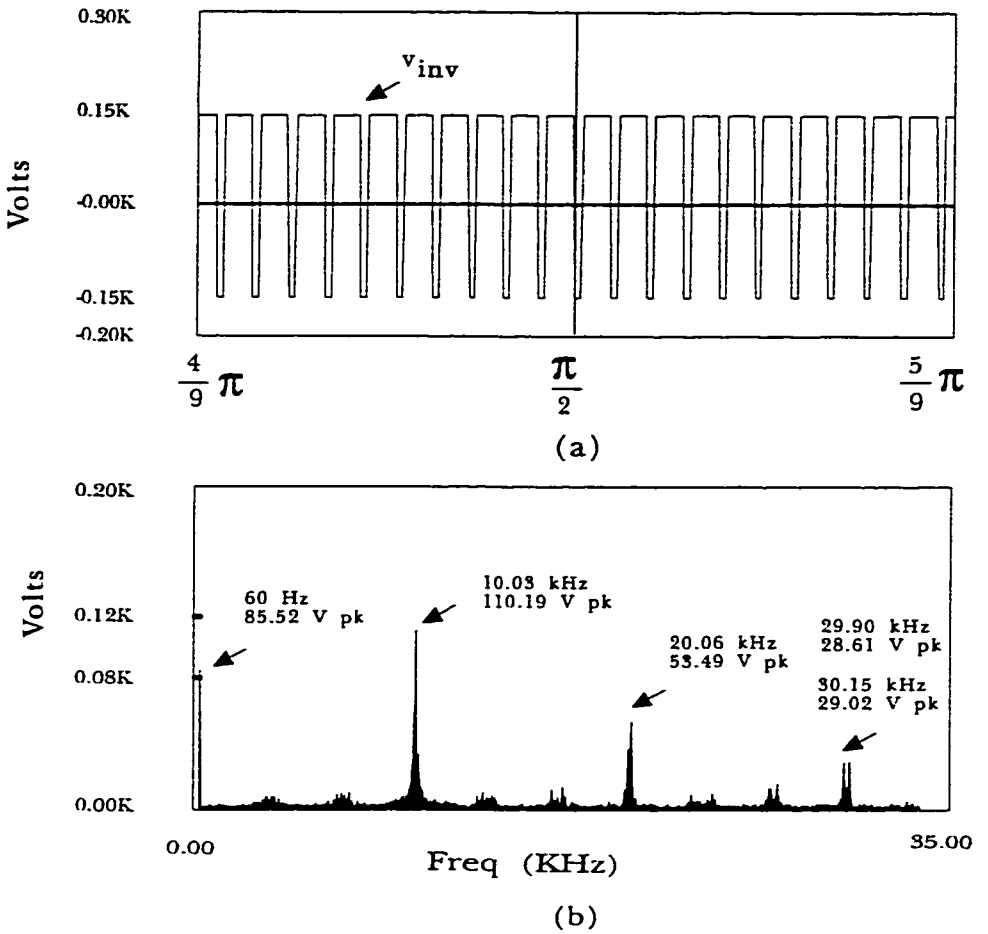


Fig. 2.7. The inverter output voltage. (a) The unfiltered output waveform. (b) The harmonic spectra.

The rms voltage appearing across each switch is equal to $V_{dc}/2$, the dc bus voltage and the rms current in the steady state is the output current i_{inv}. Therefore, by rating the switches for 1.5 to 2.0 pu voltages and currents, the inverter will be able to accommodate large transients with less reliance on the performance of the filters, transformer, and control circuits.

2.4.4 Simulated Inverter Performance

The idealized inverter and PWM section performance can be observed through simulation. The results of the simulation are shown in Fig.2.6 and Fig. 2.7 . The detail of

the generation of the PWM signals sent to the switches is shown in Fig. 2.6a. This Figure spans a period of 2.0 ms and is centered at $\pi/2$ radians, the point where the PWM pattern has the narrowest pulse widths and the shortest transition times for the lower switch. By symmetry the same conditions exist for the upper switch at $\pi 3/2$ radians. Figs. 2.6b, and 2.6c show the gating signals sent to the upper and lower switches as drawn in Fig. 2.6. The minimum on-time for the lower switch is shown to be 30 μs which is within the performance tolerances of the IGBT switches. The detail of the unfiltered inverter output is shown in Fig. 2.7 and is centered about $\pi/2$ radians. The pulse train is also taken over a period of 2.0 ms and again indicates that the maximum pulse on-time is 70 us and the off-time 30 us. Both times are also within the performance specifications of the IGBT switches. The harmonic spectra of the inverter output voltage confirms the results shown in Table 2.4. The dominant harmonic appears at 10 kHz with other major harmonic terms centered at 20 kHz and 30 kHz. Also, subharmonics appear at multiples of 3.3 kHz.

2.4.5 Construction of the Inverter and the Switching Control

The choice of the switches is based on a 2.0 pu voltage and current rating. This specification will protect the inverter during transient conditions that will be encountered under load conditions. The components used to generate the control and carrier signals can be CMOS integrated circuits, this dictates the amplitude of the carrier voltage.

2.5. The Output Filter and Transformer

The output filter and isolation transformer are shown in Fig. 2.8. This configuration

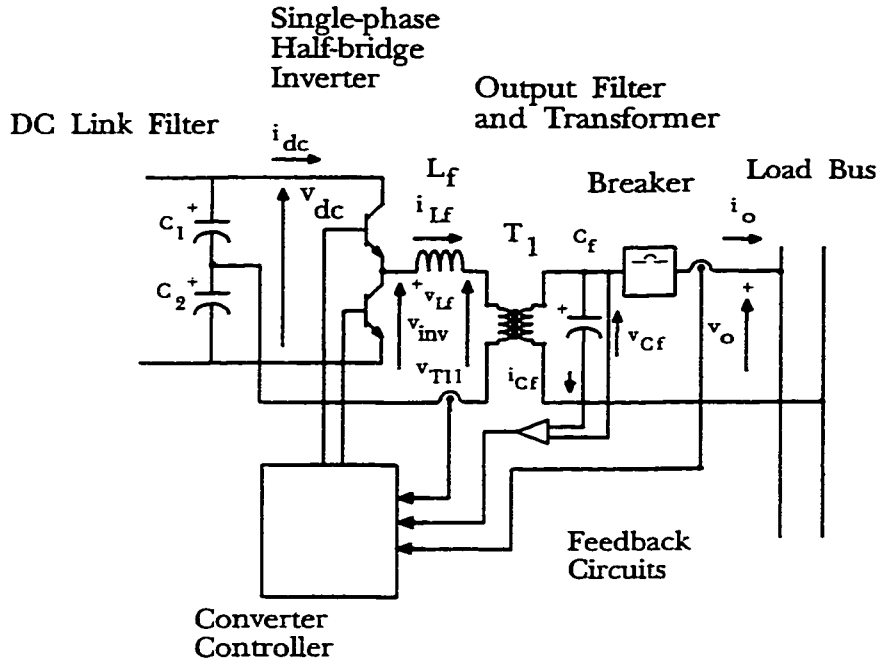


Fig. 2.8. The output filter and transformer.

places the transformer between the filter inductor, L_f, and the output capacitor, C_f, so that the inductor can limit current transients at the inverter output and the capacitor can support the voltage at the output bus. The design of the output filter is related to the choice of the PWM switching pattern. Once the type of switching pattern is determined then the filter design can

proceed on the basis of the predetermined dominant harmonic. A value in the range 0.1 to 0.25 pu can be expected if the switches are rated from 1.50 - 2.0 pu.

2.5.1. The model of the output filter

The transformer and filter combination shown in Fig. 2.8 are modeled in Fig. 2.9. The transformer used is the low-frequency model which includes the leakage resistances and magnetizing inductance. For power transformers, this model is useful up to 6.0 k rad/sec

when the magnetizing inductance becomes so large that only the leakage resistances remain.

2.5.2. Output filter component values

A second-order LC filter is used and the design is based on the assumption that at a modulation index of 0.6 the dominant harmonic is the 166th. The carrier frequency is 166 pu (10.0 kHz, 62.8 k rad/sec) and the break frequency of the filter can be found from **(2.13)** below

$$\omega_n = N_{hd} \times \left(\frac{magnitude_{(h1)} \times 0.3}{magnitude_{(hd)}} \right)^{\left(\frac{1}{\delta}\right)} \qquad \textbf{(2.13)}$$

where

ω_n	is the pu filter break frequency,
N_{hd}	is the pu order of the dominant harmonic (166),
$magnitude_{h1}$	is the pu peak magnitude of the fundamental harmonic,
$magnitude_{hd}$	is the pu peak magnitude of the dominant harmonic,
δ	is the filter order (2 in this case).

The estimated break frequency is found to be at 68.4 pu. Assuming that the filter inductor is to be large enough to limit the current transients then a value of .001 pu is chosen and the value of the capacitor can be found using

$$C = \frac{1}{L \omega_n^2} \qquad \textbf{(2.14)}$$

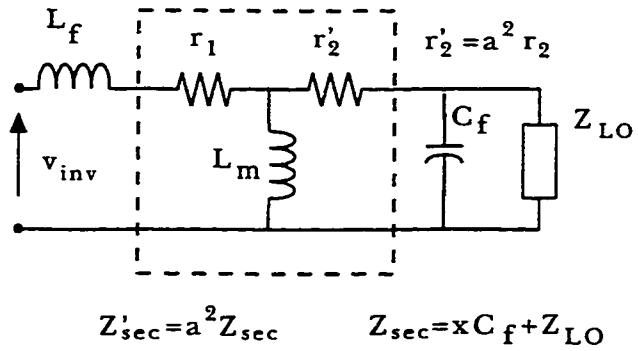


Fig. 2.9. The low-frequency transformer model and output filter.

The value of C_f is found to be 1.0 pu. The model of the transformer to be used is shown in Fig. 2.9 as part of the output filter. The low-frequency model is used since the performance at frequencies below 6.0 k rad/sec is of primary importance. The transformer leakage resistances and the magnetizing inductance are found from the results of open-circuit and short-circuit tests performed on industry standard products. The leakage resistances are found to be .005 pu, and the magnetizing inductance is approximately 100 pu.

2.5.3. Simulated output filter performance

The frequency response of the unloaded output filter is shown in Fig.2.10 . Three curves are taken corresponding to the filter capacitor values of 1.0 pu, 0.1 pu, and 0.01 pu. The smallest value has a break point at approximately 10 k rad/sec.

2.5.4. Construction of the output filter

The current rating of the output filter inductance and the voltage rating of the output filter capacitor are placed at 2.0 pu. This value gives sufficient margin for the limited

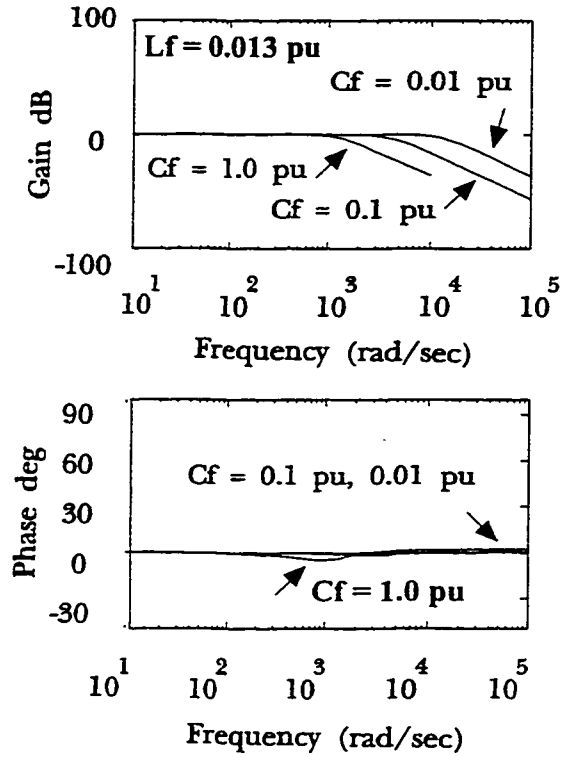


Fig. 2.10. The frequency response of the output filter including the transformer magnetizing inductance.

overload and transient conditions allowed by the control module. The transformer, which is often mandated as an isolating element as well as a step-up or step-down voltage adjustment, is less flexible with respect to the ratings and the model parameters such as magnetizing inductance and leakage resistance. The VA rating of the transformer implies a range of electrical values and size and weight constraints which can only be over come by using more sophisticated switching patterns (Harmonic Injection PWM, or Selective Harmonic Injection PWM) or transformerless circuit topologies.

2.5.5. The Interconnection and Supply of Converter Modules

There are four issues which must be considered that deal with the interface of the

CM with the supply and load busses: 1) resonant frequencies between converters, 2) load switching, 3) soft start capability and dc bus control, and 4) current sharing between multiple converters connected in parallel. The possibility of resonances between converter modules is minimized by the use of isolation transformers and output filters. The dc bus is considered an ideal source for the purposes of this research. The load switching and current sharing capabilities of the converters will be investigated in Chapters 3.0 and 4.0.

2.6. Summary

In order to investigate the feasibility of the proposed system of converters and the control scheme, a CM is designed that will use advances in power semiconductor technology as well as serve as a baseline for comparison with more advanced techniques. The CM is based on a single-phase half-bridge inverter supplied by its own rectifier and dc bus filter. The inverter uses IGBT switches operating at 10 kHz using a SPWM switching pattern The output of each inverter is sent to a transformer and output filter and is connected to the load bus by a breaker. Each CM uses a static rectifier at the input with a passive input filter which is designed to protect the utility bus but is not optimized for performance and size. The rectifier output filter is a passive second order designed to maintain a dc voltage level with less than 0.3% THD and 0.5% ripple.

The inverter section of the CM is presented with an output filter and an isolation transformer that are designed to filter harmonic components above 1.0 k rad/sec. The converter is synchronized to the utility bus by means of a phase-locked loop (PLL) circuit which represents a standard industry design. A separate circuit is required for each CM in

order to control the output voltage and current. Also, a circuit must be designed to balance the load currents between the individual converter units. These control functions will be designed in Chapter 3.0.

3. DESIGN AND PERFORMANCE OF THE CONVERTER CONTROL SYSTEM

3.1. Control Strategy for the Proposed System of Converter Modules

The CM is designed to promote the modularity and the output-quality of the complete system of paralleled converters. Thus, the interconnections between the individual units are minimized and each module is expected to control its respective output voltage and current. In order to do this without generating undesirable voltage and current components on the critical bus, it is important that the output voltages at each CM be as close as possible in amplitude and in phase. To accomplish this, very fast circuits are used to control the output of each inverter. The amplitude of each converter's output current is determined by an inner current-control loop that acts as a limiting device. The voltage is governed by an outer voltage-control loop which matches the converter output to that of the critical bus. In addition to the requirement that the output of each CM be matched, the power delivered to the load must be shared equally between the converters. This power sharing strategy is implemented by incorporating a third, outer current-share control loop that ensures that each converter contributes its portion of the total load current. The current sharing parameters, amplitude and phase, are transmitted to the controllers of each converter by means of a frequency modulated (FM) communication scheme. The FM signals are decoded so that the average amplitude and phase of all the individual converter currents is determined and a

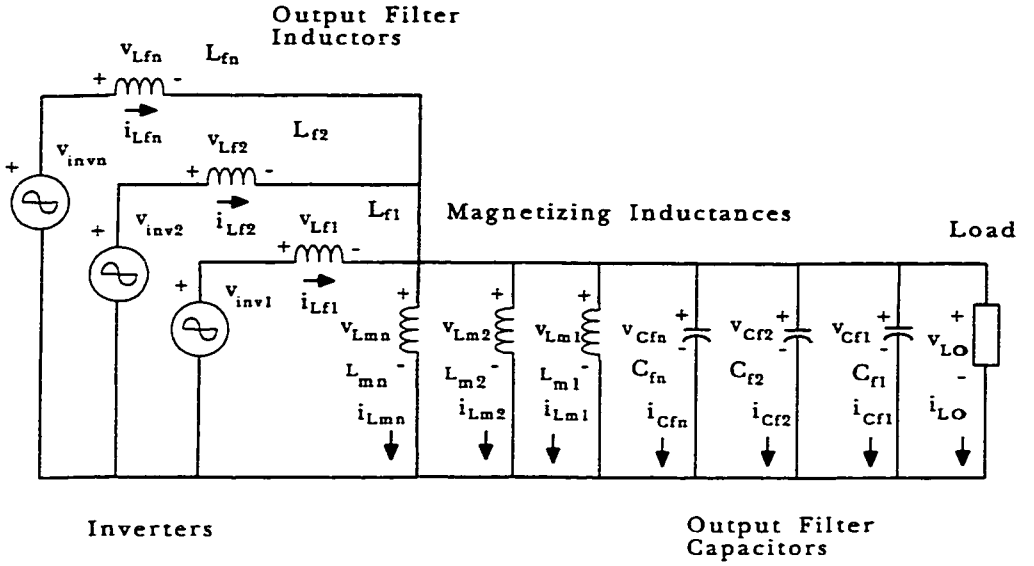


Fig. 3.1. The equivalent circuit of n paralleled converters.

common current reference template is available to converter controllers.

3.1.1. The Model of the CM System

The equivalent circuit of the system of *n* paralleled converters is shown in Fig. 3.1. The individual rectifiers and inverters are reduced to identical ac sources which are assumed to be in phase and with identical output voltage amplitudes. The individual module output transformers are reduced to their respective magnetizing and leakage reactances. The magnetizing inductances, L_{mn} , are referred to the primary coils of the transformers and the leakage reactances, are added to the respective filter inductors, L_{fn} . The parallel arrangement of the CM's indicates that the basic control strategy will be a current control scheme.

3.1.1.1. The model equations

The currents of the circuit of Fig. 3.1 can be described by

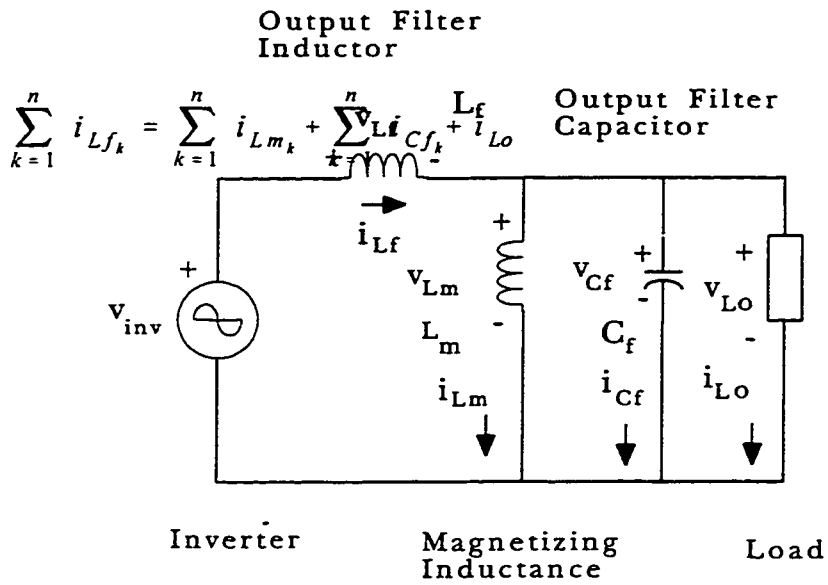


Fig. 3.2. The equivalent circuit of the converter module.

where

i_{Lfk} is the current through the kth filter inductor and leakage inductance,

i_{Lmk} is the current through the kth magnetizing inductance,

i_{Cfk} is the current through the kth output-filter capacitor,

i_{Lo} is the load current.

The voltages are defined as

$$v_{inv1} = v_{inv2} = v_{invn} \tag{3.2}$$

where

$v_{inv1} \cdots v_{invn}$ are the per-unit inverter voltages,

Note, that the voltage sources represent the same quantity if they are ideal, are in phase, and

have the same amplitude.

3.1.1.2. The reduced equivalent circuit

The magnetizing inductances and the filter capacitors of the individual CM's can be combined to form a single inductor and capacitor. Thus, the circuit of Fig. 3.1 can be reduced to the circuit of Fig. 3.2. This simplified equivalent circuit represents a single CM with an output filter and a transformer connected to a 1 pu load. Following the standard derivation given by Holtz et al [7], the circuit equations are given as

$$v_{inv} = v_{Lf} + v_{Cf} \tag{3.3}$$

where

$$v_{Cf} = v_{Lm} = v_{Lo} \tag{3.4}$$

The currents are given by

$$i_{Lf} = i_{Lm} + i_{Cf} + i_{Lo} \tag{3.5}$$

The voltage and current relationships for the reactive elements are defined as

$$v_{Lf} = L_f \frac{d i_{Lf}}{d t} \tag{3.6}$$

The current of the output-filter capacitor is given by

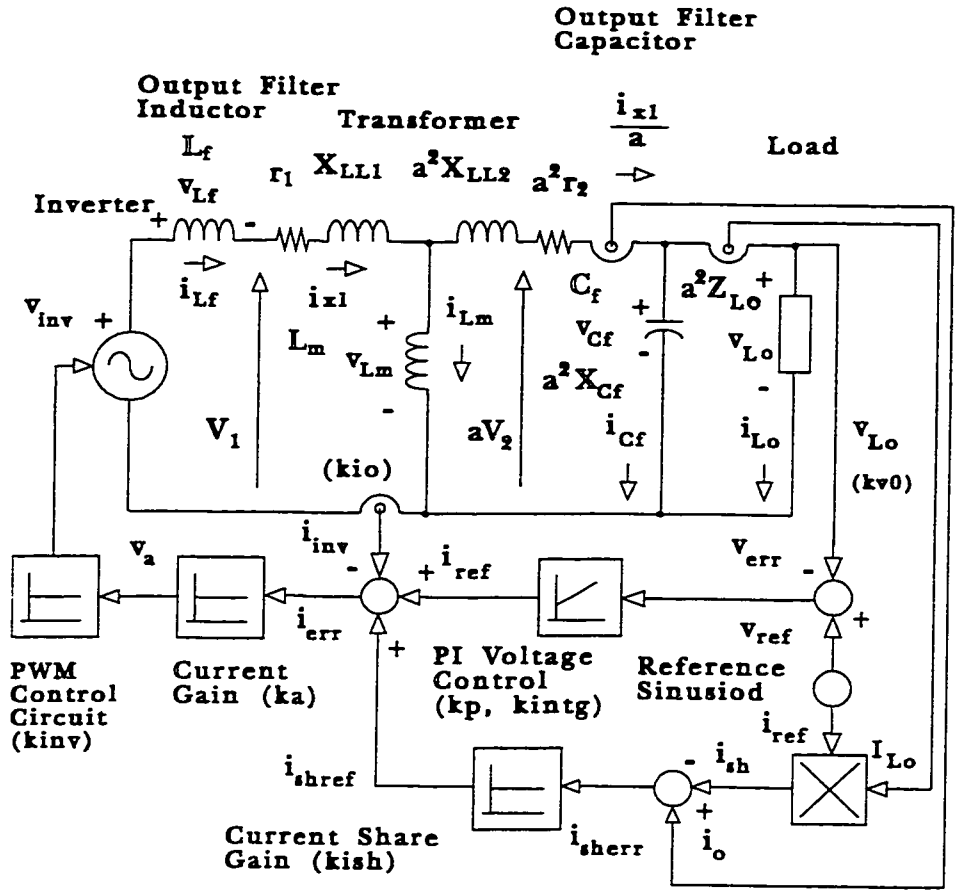


Fig. 3.3. The converter module control scheme.

$$i_{Cf} = C_f \frac{dv_{Cf}}{dt} \tag{3.7}$$

$$v_{Lm} = L_m \frac{di_{Lm}}{dt} \tag{3.8}$$

Table 3.1. CONTROL CIRCUIT PERFORMANCE CRITERIA

Circuit Performance Parameter	Control System Parameter
Response to Load Application	Response Time, 8.33 ms
Response to Load application	Settling Time, 100 ms
Overvoltage	Overshoot, 10%

These fundamental circuit relationships form the basis for analyzing and designing the CM control mechanisms and the system as a whole.

3.1.2. The Basic CM Control Circuit

Control of the individual converters requires two fundamental control loops that emphasize speed of response in order to minimize the effects of unwanted components in the output voltages and currents. An inner current controller has the added function of protecting the inverter from damaging current surges. The outer voltage control circuit is designed to monitor the load voltage and to contribute to the over all power sharing strategy between the CM's. The diagram of Fig. 3.4 shows how the control circuit is attached to the CM. This circuit will be used in the following sections to analyze the action of the control circuit. Note that the circuit incorporates the output transformer developed in section 2.5 and Fig. 2.9.

The inner current-control circuit must have a fast response to changes in the total converter output current. Since the desired total response time for both control loops is limited to one cycle, at 60 Hz the maximum time limit is 16.67 ms. In order to achieve 1:10 ratio in the response times of the inner to the outer loop, the objective is to design an inner

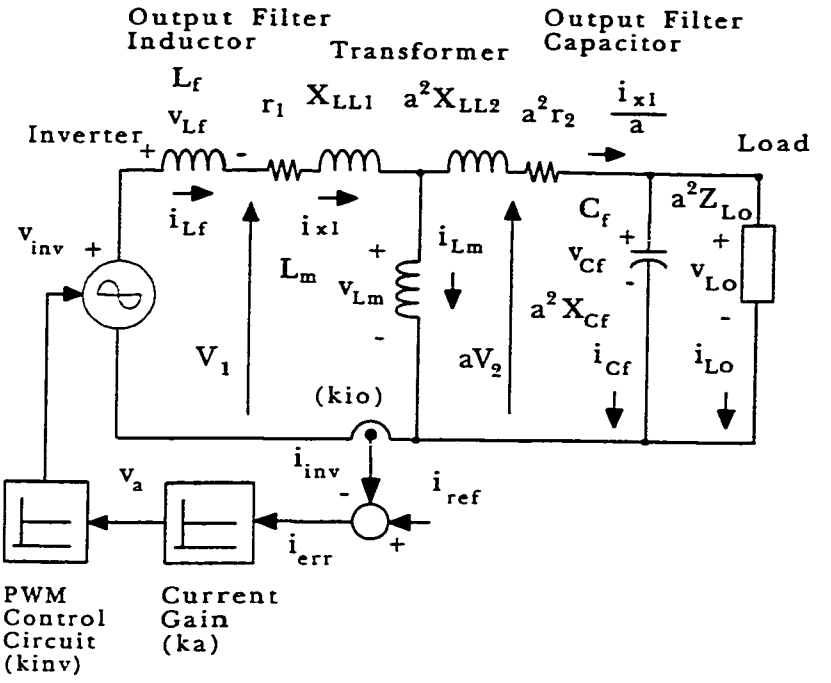


Fig. 3.4. The inner current control loop.

current loop that can react in 1.67 ms. The outer voltage controller then has a much longer response time and can incorporate a proportional-integral (PI) control mechanism.

3.1.3. Control System Design Criteria

Each CM must have a controller that can meet specific requirements for maximum overshoot, settling time, and steady-state error. Parameter sensitivity is also of interest since circuit elements can change with temperature or vary due to manufacturing inconsistencies. Also, these performance criteria are related to the power quality. The settling time, t_s, of the

complete control system must be less than 16.66 ms. This will ensure that associated power-quality parameters such as flicker, voltage sag, and surge are minimized. The performance criteria associated with the CM are summarized in Table 3.1.

3.2. The Current Control Circuit

There are three components of the inverter output current which are possible control variables. The transformer magnetizing current, the output-filter capacitor current, and the current output to the critical bus are parameters that could be used to manage the output of the converter module. The first will be neglected in the strategy to be used here. Thus, the current to the capacitor and to the load will provide the information necessary to control the voltage and the power delivered by the CM. The first circuit parameter to be encountered is the current through the output filter inductor, i_{Lf}. This value represents the total CM current and is the basis for the inner current loop.

3.2.1. The Inner Current Control Loop

The speed response of the inner current-control loop is met by placing a cascade proportional controller in a feedback circuit as shown in Fig. 3.5. The reference current is a sinusoid which is generated by the voltage control loop. The transfer function of this loop is given by

$$T(s) = \frac{i_{Lf}}{i_{ref}} = \frac{k_a \cdot k_{inv} \cdot G(s)}{1 + k_{io} \cdot k_a \cdot k_{inv} \cdot G(s)} \qquad \textbf{(3.9)}$$

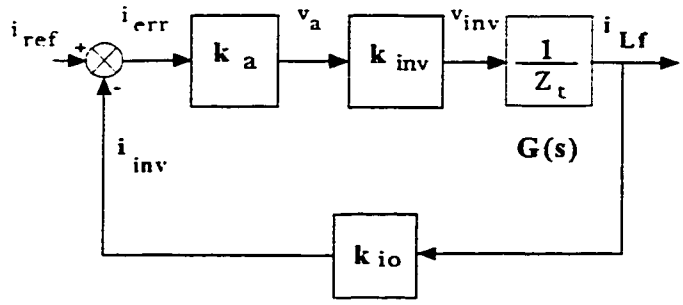


Fig. 3.5. The inner current loop block diagram.

where k_a, k_{inv}, and k_{io} are gain constants shown in Fig.3.5 . The value of k_a is determined from the step response of the circuit and the Bode plot. The constant k_{io} is the gain of the current sensor and k_{inv} is the inverter gain. As described in Chapter 2.3, K_{inv} is found from the amplitude of the carrier and the dc bus as

$$K_{inv} = \frac{V_{dc}}{2 \cdot V_{carrier}} \tag{3.10}$$

The function $G(s)$ is given by

$$G(S) = K_1 \cdot \frac{s^2 + K_2 \cdot s + K_3}{s^3 + K_4 \cdot s^2 + K_5 \cdot s + K_6} \tag{3.11}$$

The constants are

$$K_1 = \frac{k_a \cdot k_{inv} \cdot k_{io}}{L_f} \tag{3.12}$$

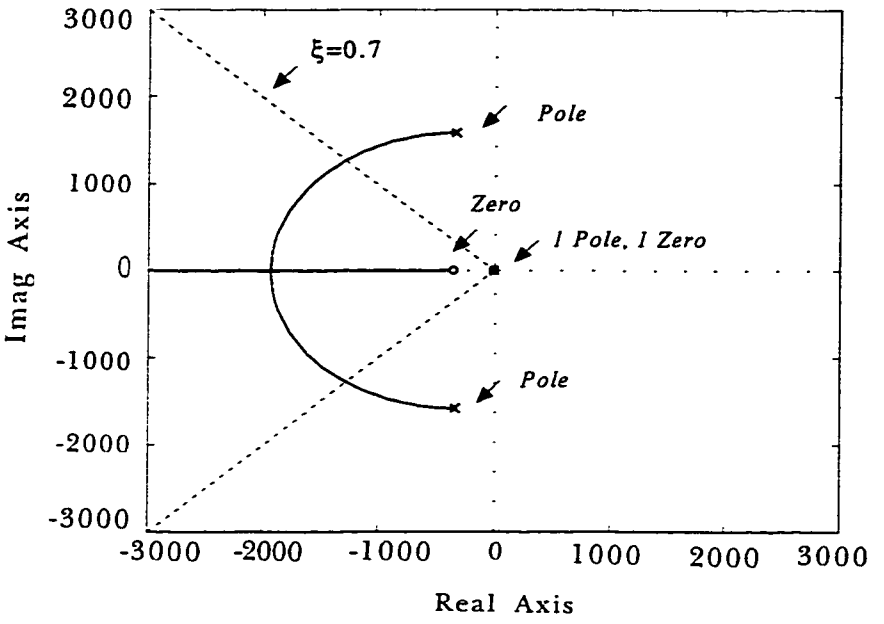


Fig. 3.6. The Root Locus of the inner current loop.

$$K_2 = \frac{L_m + R_a \cdot C_f}{R_{Lo} \cdot L_m \cdot L_f} \tag{3.13}$$

$$K_3 = \frac{R_b}{R_{Lo} \cdot L_m \cdot C_f} \tag{3.14}$$

$$K_4 = \frac{L_m \cdot L_f + L_f \cdot R_a \cdot C_f + r_1 \cdot R_{Lo} \cdot L_m \cdot C_f + R_a \cdot L_m \cdot C_f}{R_{Lo} \cdot L_m \cdot L_f \cdot C_f} \tag{3.15}$$

$$K_5 = \frac{R_b \cdot L_f + L_m \cdot r_1 + r_1 \cdot R_a \cdot C_f + R_b \cdot L_m}{R_{Lo} \cdot L_m \cdot L_f \cdot C_f} \tag{3.16}$$

$$K_6 = \frac{r_1 \cdot R_b}{R_{Lo} \cdot L_m \cdot L_f \cdot C_f} \tag{3.17}$$

The damping terms are $R_a = a^2 r_2 R_{lo}$, and $R_b = a^2 r_2 + a^2 R_{lo}$. These values represent a minimum amount since the resistances associated with the filter components L_f and C_f, and the physical connections are not represented.

3.2.2. The Performance of the Inner Current Controller

The Root Locus diagram in Fig.3.6 shows that the inner current control is stable and by choosing a point on the locus a value for the open loop gain K_I can be found. The amplifier gain K_a is then derived using (3.12). The step response of the inner current controller is shown in Fig 3.7 for three values of K_a although a gain of approximately 5.0 is more than sufficient to ensure a response within the required 1.67 ms.

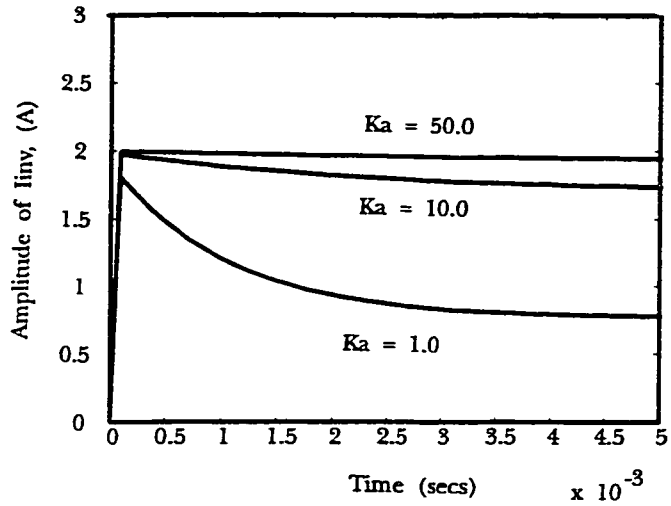


Fig. 3.7. The step response of the inner current control loop.

3.2.3. The Transformer Magnetizing and Filter Capacitor Currents

The current components of Fig. 3.2, that correspond to the transformer magnetizing current, i_{Lm}, and the filter capacitor current, i_{Cf} are not included directly in the control scheme. The magnetizing current is not controlled because the half-bridge configuration reduces the possibility of saturation by eliminating dc current components. The capacitor current is controlled indirectly through the output voltage using the voltage control loop.

3.2.4. Control of Load Sharing

The load current, i_{Lo}, shown in Fig. 3.2 is used as a control variable as part of the current sharing circuit to be described in Section 3.5. The presence of the load current as a single central control variable allows the voltage control of each CM to be adjusted independently. In addition, the signal that represents the load current variable can be transmitted to the individual modules through the output bus thereby eliminating the 'third'

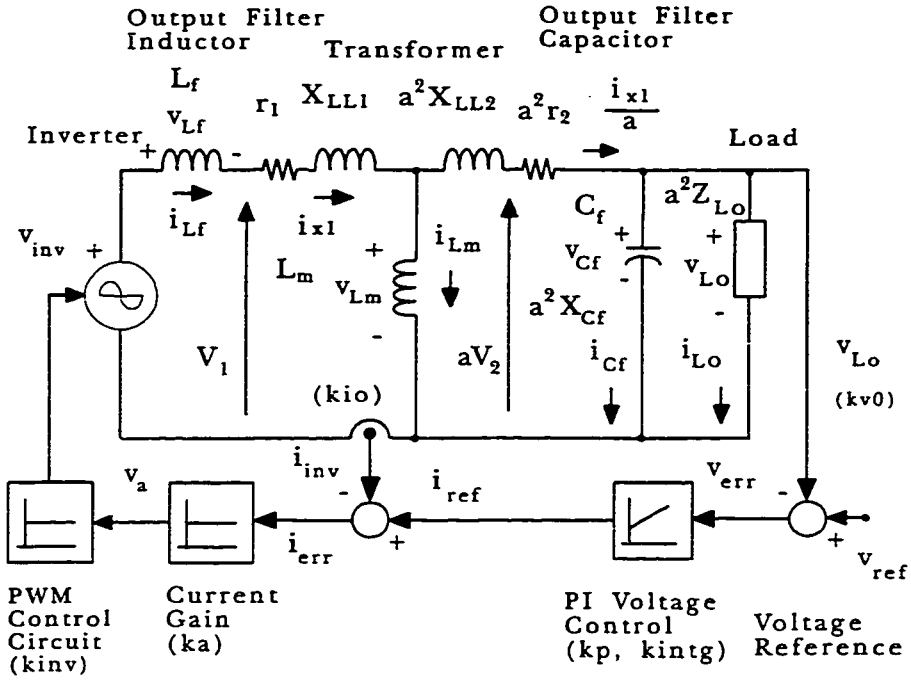


Fig. 3.8. The inner current and outer voltage control loops.

wire for communication.

3.3. The Voltage Control Circuit

The outer control loop is the voltage control circuit shown in Fig. 3.8. The circuit consists of a proportional-plus-integral control element that uses a signal generated by the utility bus or a synchronization circuit as the reference. The feedback signal is the voltage, v_{Lo}, which is taken from the output filter capacitor. The PI circuit is added to reduce the steady-state error and to provide a pair of dominant complex poles.

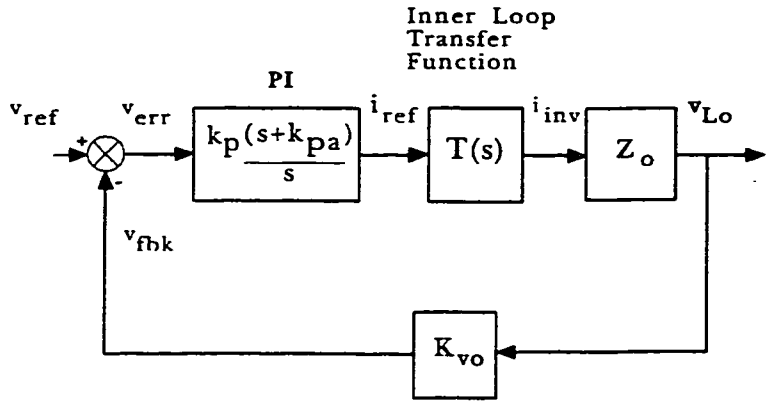


Fig. 3.9. Block diagram of the outer voltage control loop.

3.3.1. The Outer Voltage Control Loop

The transfer function of the outer voltage loop, Fig. 3.9, is given by

$$T_v(s) = \frac{v_{Lo}}{v_{ref}} = \frac{k_p \cdot k_s \cdot k_x \cdot G_v(s)}{1 + k_{vo} \cdot k_p \cdot k_s \cdot k_x \cdot G_v(s)} \tag{3.18}$$

where k_p is the proportional gain of the PI circuit and

$$k_s = \frac{k_a \cdot k_{inv}}{L_f} \tag{3.19}$$

$$k_x = \frac{a^2}{C_f} \tag{3.20}$$

The open loop transfer function $G_v(s)$ of Fig. 3.9 is given by

$$G_v(s) = \frac{s^3 + K_{v1} \cdot s^2 + K_{v2} \cdot s + K_{v3}}{s^5 + K_{v4} \cdot s^4 + K_{v5} \cdot s^3 + K_{v6} \cdot s^2 + K_{v7} \cdot s + K_{v8}} \tag{3.21}$$

where

$$K_{v1} = \frac{L_m + (a^2 \cdot r_2 \cdot r_{Lo} \cdot C_f)}{r_{Lo} \cdot L_m \cdot C_f} + K_{pa} \tag{3.22}$$

$$K_{v2} = \frac{a^2 \cdot r_2 + a^2 \cdot r_{Lo}}{r_{Lo} \cdot L_m \cdot C_f} + K_{pa} \cdot \frac{L_m + (a^2 \cdot r_2 \cdot r_{Lo} \cdot}{r_{Lo} \cdot L_m \cdot C_f} \tag{3.23}$$

$$K_{v3} = K_{pa} \cdot \frac{a^2 \cdot r_2 + a^2 \cdot r_{Lo}}{r_{Lo} \cdot L_m \cdot C_f} \tag{3.24}$$

$$K_{v4} = a_1 \cdot a_{11} \tag{3.25}$$

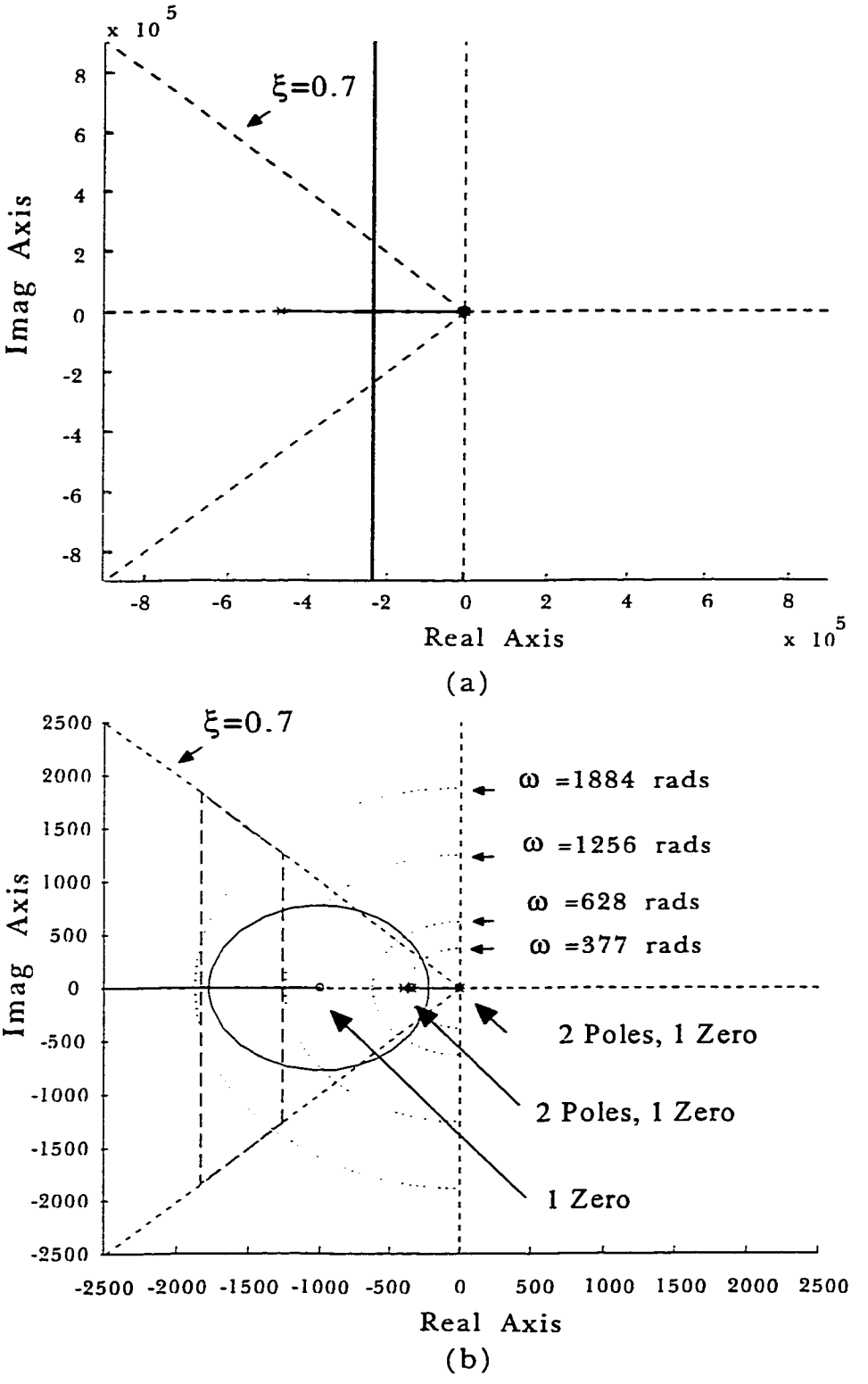


Fig. 3.10. The root locus of the current and voltage control loops. (a) The complete root locus. (b) The detail of the root locus around 1.5 k rad/sec.

$$K_{v5} = a_2 + a_{11} \cdot a_1 + a_{22} \tag{3.26}$$

$$K_{v6} = a_3 + a_{11} \cdot a_2 + a_{11} \cdot a_2 \tag{3.27}$$

$$K_{v7} = a_{22} \cdot a_3 \tag{3.28}$$

$$a_1 = \frac{\begin{array}{c} L_m \cdot L_f + L_f \cdot r_a \cdot C_f + r_1 \cdot r_{Lo} \cdot L_m \cdot C_f \\ + r_a \cdot L_m \cdot C_f + K_2 \cdot r_{Lo} \cdot L_m \cdot C_f \end{array}}{L_f \cdot r_{Lo} \cdot L_m \cdot C_f} \tag{3.29}$$

$$a_2 = \frac{\begin{array}{c} r_b \cdot L_f + r_1 \cdot L_m + r_1 \cdot r_a \cdot C_f \\ + r_b \cdot L_m + K_2 \cdot L_m + K_2 \cdot r_a \cdot C_f \end{array}}{L_f \cdot r_{Lo} \cdot L_m \cdot C_f} \tag{3.30}$$

$$a_3 = \frac{r_1 \cdot r_b + K_2 \cdot r_b}{r_{Lo} \cdot L_m \cdot C_f \cdot L_f} \tag{3.31}$$

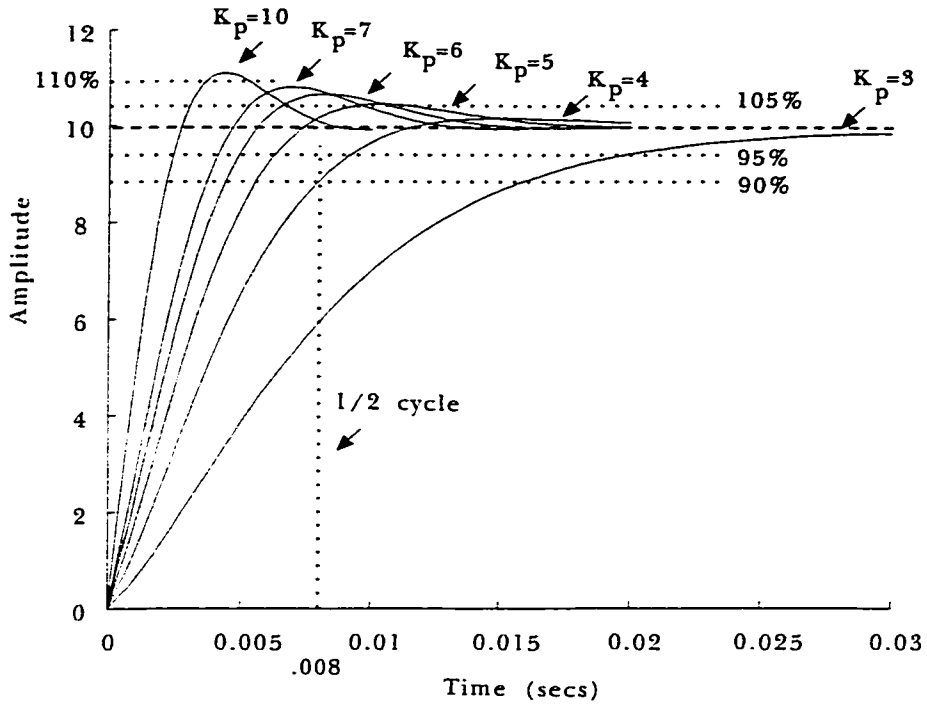
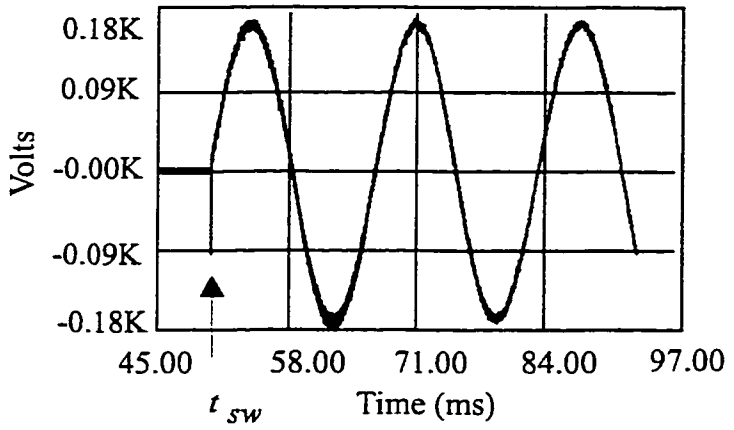


Fig. 3.11. The step response of the inverter voltage control loops for values of k_p, the proportional gain constant of the PI controller.

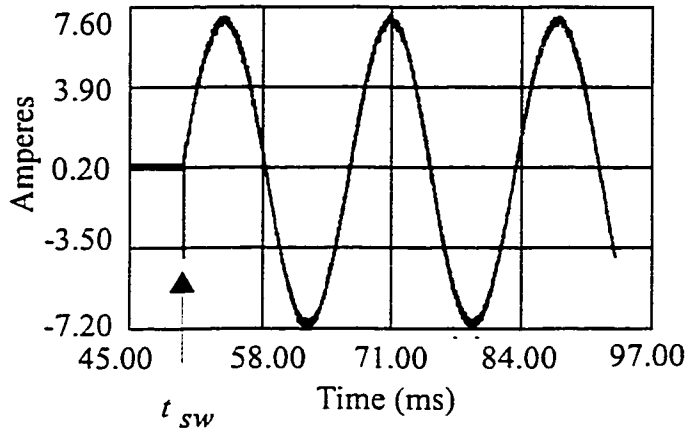
$$a_{11} = \frac{L_m + r_b \cdot C_f}{r_{Lo} \cdot L_m \cdot C_f} \tag{3.32}$$

$$a_{22} = \frac{r_b}{r_{lo} \cdot L_m \cdot C_f} \tag{3.33}$$

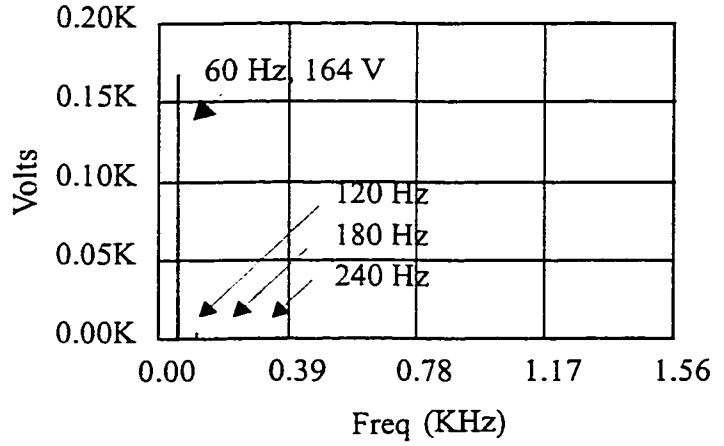
where $r_a = \alpha^2 r_2 r_{Lo}$, $r_b = \alpha^2 r_2 + \alpha^2 r_{Lo}$, $K_1 = K_a K_{inv}$, and $K_2 = K_{io} K_a K_{inv}$.



(a)



(b)



(c)

Fig. 3.12. The simulated response of the inverter to a 1.25 pu load, 1 PF, $k_p = 5.0$, $t_{sw} = 50$ ms. (a) The load voltage. (b) The load current. (c) The load voltage spectrum.

The root locus of this system is shown in Fig. 3.10. The complete root locus diagram indicates that the combination of the inner and outer loops is stable and that the cascade PI controller contributes pair of complex poles and a damping constant. The detail of the root locus contains an enclosed region around 1.5 k rad/sec that can be used to find the loop gain constant, K_v, and the proportional gain, K_p. These values are derived from (3.18) where

$$K_v = k_{vo} \cdot k_p \cdot k_s \cdot k_x \qquad \textbf{(3.34)}$$

Since k_s and k_x are known and the feedback constant k_{vo} is determined by the voltage transducer, the root locus can be used to find range of values for k_p. By choosing values of the open loop gain constant, K_v, that lie within the dashed lines of Fig. 3.13 a value can be found which corresponds to the time constant of the outer control loop.

3.3.2. The Performance of the Voltage Control Circuit

The step response of the voltage control circuit is shown in Fig.3.11. If the gain of 5.0 is used, then the response of the inverter will be within 10% of the final value within a half cycle as required by the published specifications and the objectives of Table 3.1.

3.3.3. The Simulation of the Voltage Controller

The simulated response of the inverter is shown in Fig. 3.12. The waveforms show the response of a single inverter circuit to the application of a 1.25 pu load of 1.0 PF. Also

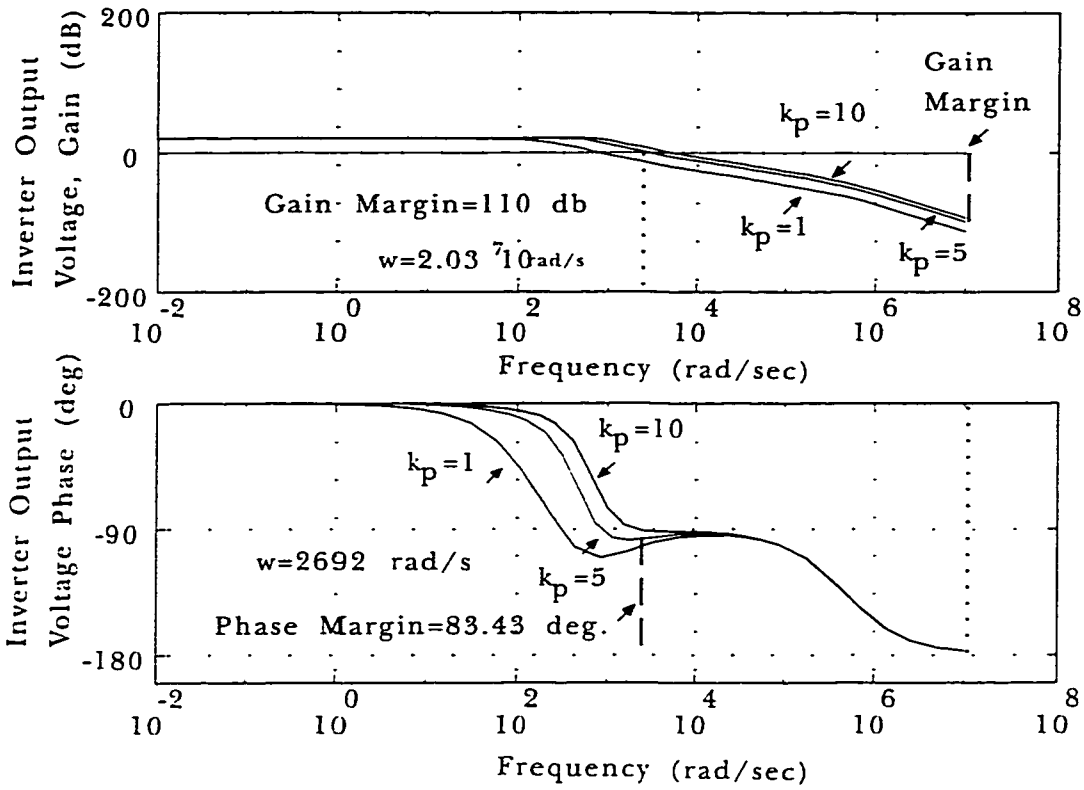


Fig. 3.13. The Bode diagram of the inverter output voltage.

shown in Fig. 3.12 is the spectrum of the output voltage. The Bode plot in Fig. 3.14 shows that the output voltage is stable to 2.03×10^7 radians (3.2×10^6 Hz) and the cutoff frequency for the harmonics is approximately 2700 radians.

3.4. Summary

As a first step in the design of a control scheme for a system of parallel connected converters, the controller for the single CM is developed. The equivalent circuit of the converter including the transformer and load is chosen, three loops are connected and the transfer function is evaluated. The control variables to be used are the voltage at the output filter capacitor (V_{out}), the output current, I_{out}, and the total current output by the inverter, the

filter inductor current, I_{Lf}. Table 3.1 shows the response characteristics that the basic converter must exhibit. To obtain the desired 8.33 ms response (current and voltage) the Root Locus diagram of the CM is identified and the closed loop gain constant is evaluated. Since there are constraints on the gains of the two current loops, the gain of the PI element associated with the voltage loop plays the most important role. Figure 3.11 establishes the range of values for the gain of the PI block as well as the stability of the CM controller. The Root Locus diagram of Fig. 3.10 shows that the basic converter module is stable for the range of values and the circuit topology chosen.

4. THE FM CURRENT-SHARING COMMUNICATION SCHEME

4.1. Control of Multiple Converter Modules

The interconnection of the system of inverter modules requires the addition of two more elements to complete the entire control scheme. First, a power-sharing current control loop is added to the ensure that each converter contributes an equal share of the total load current. Secondly, a FM communication scheme is to be added that will permit the current sharing feedback signal to be transferred over the load bus. The use of the load bus as a communications channel will eliminate the need for a separate control bus thereby simplifying the installation of the entire system.

4.2. The Model of the Paralleled System of Converters

The diagram of Fig. 3.1 is the equivalent circuit of n converters in a parallel configuration. This topology is used as the basis for the diagram of Fig. 4.1 where a basic system composed of two modules is presented without any connection between their respective controllers. In this case there are three ways the two inverter sections, although identical, can produce nonidentical output voltages and currents:

1) The inverter loop gains are different.

2) The voltage references are different.

3) The impedances of the output bus between modules is different.

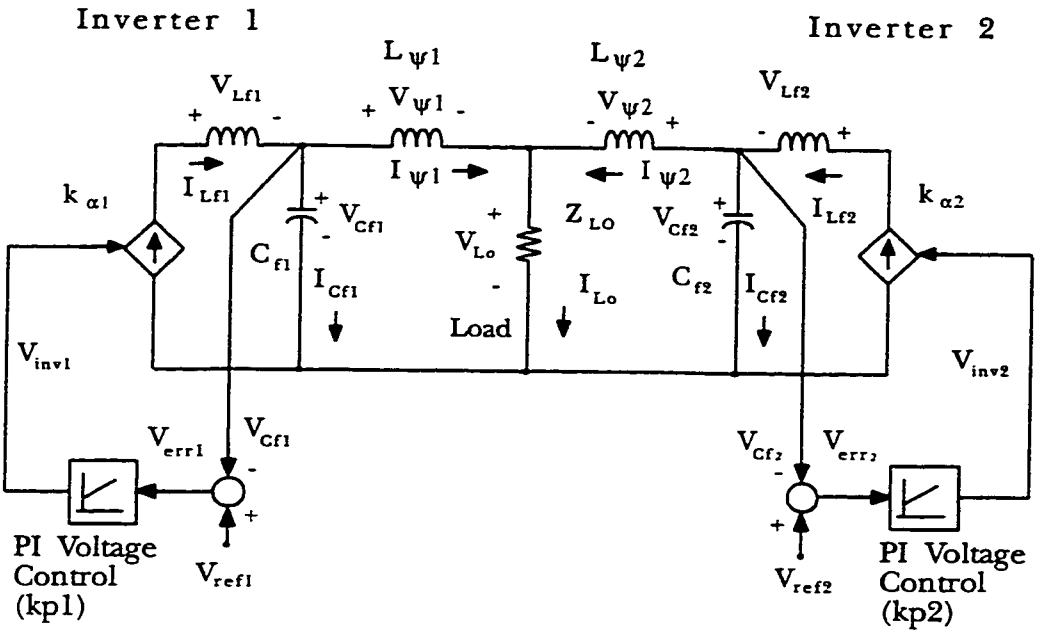


Fig. 4.1. The model used to evaluate the effect of the voltage-reference imbalance on a system of two converters connected in parallel.

The current balance controller to be added to the previously developed current and voltage control loops will modulate the voltage references therefore, the differences in the loop gains and the individual currents at the load will be compensated. Thus, the importance and the characteristics of the effect that the voltage reference unbalance has on the complete system must be modeled and evaluated.

The differences in the voltage references can be determined from Fig. 4.1 where each CM is modeled as a current source. The magnetizing inductances are neglected and an inductive impedance has been added to each CM to simulate the connection between the module and the load. The analysis proceeds on the basis that all quantities are phasors operating at 1 pu radian frequency and that the operating parameters in both inverters are the same except for the respective voltage references. The voltage references differ in peak amplitude only and all sinusoidal voltages and currents are in phase. In this way the net

imbalance between the load currents of each inverter, $I_{\psi 1}$ and $I_{\psi 2}$ can be observed. At the output of each CM the voltages and currents are given by

$$\begin{aligned} V_{cf1} &= -j\, I_{cf1} \cdot X_{cf1} \\ V_{cf2} &= -j\, I_{cf2} \cdot X_{cf2} \end{aligned} \tag{4.1}$$

$$\begin{aligned} I_{cf1} &= k_{\alpha 1} \cdot V_{inv1} - I_{\psi 1} \\ I_{cf2} &= k_{\alpha 2} \cdot V_{inv2} - I_{\psi 2} \end{aligned} \tag{4.2}$$

Here $k_{\alpha 1}$ and $k_{\alpha 2}$ represent the gain of the inner current control loop and $I_{\psi 1}$ and $I_{\psi 2}$ are the currents through the sections of the output bus connecting the respective inverters to the load. Also, it is assumed that $I_{\psi 1} + I_{\psi 2} = V_{Lo} / Z_{Lo}$ and $I_{cf1} = I_{cf2}$. The voltages developed at the inverters are

$$\begin{aligned} V_{inv1} &= V_{err1} \cdot -j \cdot k_{p1} \\ V_{inv2} &= V_{err2} \cdot -j \cdot k_{p2} \end{aligned} \tag{4.3}$$

where k_{p1} and k_{p2} are the gains of the PI control blocks. The voltage error in each case is

$$\begin{aligned} V_{err1} &= -V_{cf1} + V_{ref1} \\ V_{err2} &= -V_{cf2} + V_{ref2} \end{aligned} \tag{4.4}$$

The reference voltages are phasors and

$$\begin{aligned} V_{ref1} &= V_{pk,\,ref1}\angle 0 \\ V_{ref2} &= (V_{pk,\,ref2} + \Delta V_{ref})\angle 0 \end{aligned} \tag{4.5}$$

By substituting (4.5) into (4.4) V_{err} is expressed as a function of $V_{cf1,2}$ and $V_{ref1,2}$.

$$\begin{aligned} V_{err1} &= -V_{cf1} + V_{pk,\,ref1}\angle 0 \\ V_{err2} &= -V_{cf2} + (V_{pk,\,ref2} + \Delta V_{ref})\angle 0 \end{aligned} \tag{4.6}$$

By substituting (4.3) into (4.6) the inverter voltage gain is

$$\begin{aligned} V_{inv1} &= (-V_{cf1} + V_{pk,\,ref1}\angle 0) \cdot -j \cdot k_{p1} \\ V_{inv2} &= (-V_{cf2} + (V_{pk,\,ref2} + \Delta V_{ref})\angle 0) \cdot -j \cdot k_{p2} \end{aligned} \tag{4.7}$$

Since $I_{cf1} = I_{cf2}$, (4.7) can be substituted into (4.2) and the relation between the capacitor currents is

$$\begin{aligned} & k_{\alpha 1} \cdot (-V_{cf1} + V_{pk,\,ref1}\angle 0) \cdot (-j \cdot k_{p1}) - I_{\psi 1} \\ &= k_{\alpha 2} \cdot (-V_{cf2} + (V_{pk,\,ref2} + \Delta V_{ref})\angle 0) \cdot (-j \cdot k_{p2}) - I_{\psi} \end{aligned} \tag{4.8}$$

Let $V_{cf1} = V_{cf2} = V_{Lo} = I_{Lo} \cdot Z_{Lo}$ in the steady state and

$$\begin{aligned} \Delta I_{\psi} &= I_{\psi 1} - I_{\psi 2} \\ I_{Lo} &= I_{\psi 1} + I_{\psi 2} \end{aligned} \tag{4.9}$$

By replacing V_{cf1} and V_{cf2} with the load voltage V_{Lo} and by adding $I_{\psi 2}$ to (4.8) the expression to evaluate becomes

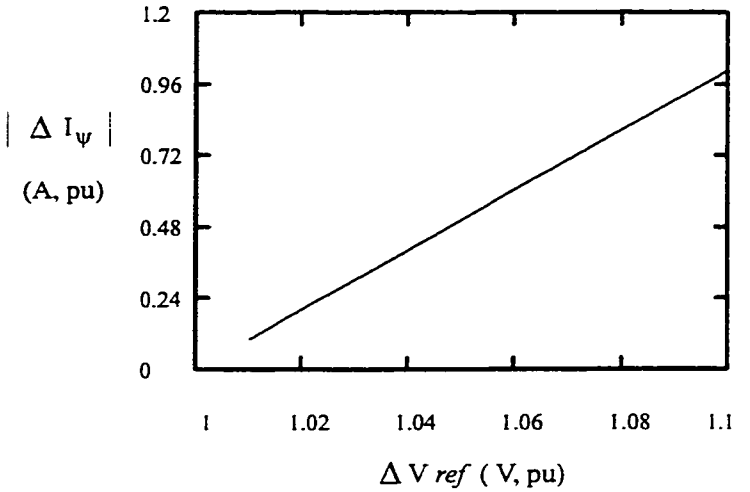


Fig. 4.2. Output current imbalance due to reference voltage difference.

$$k_{\alpha 1} \cdot (-(I_{Lo1} \cdot Z_{Lo1} + V_{pk.\,ref1} \angle 0) \cdot (-j \cdot k_{p1}) - \Delta I_{\psi} = k_{\alpha 2} \cdot (- I_{Lo\,2} \cdot Z_{Lo\,2} + (V_{pk.\,ref2} + \Delta V_{ref}) \angle 0) \cdot (-j \cdot k_{p2} \quad \textbf{(4.10)}$$

The magnitude of the current imbalance is given in Fig. 4.4. where

$k_{\alpha 1}$, $k_{\alpha 2}$ =0.25

k_{p1}, k_{p2} =0 + 14i, 1 pu

V_{ref1}, V_{ref2} =12+0i, 0.1 pu

Z_{Lo} =14.4+0i, 0.5 pu

The current imbalance is a linear function of the difference between the voltage references.

4.3. The Stability of the Proposed Control Scheme

The stability of the interconnected system of paralleled converters and the proposed control scheme can be investigated using a state space realization of a circuit composed of

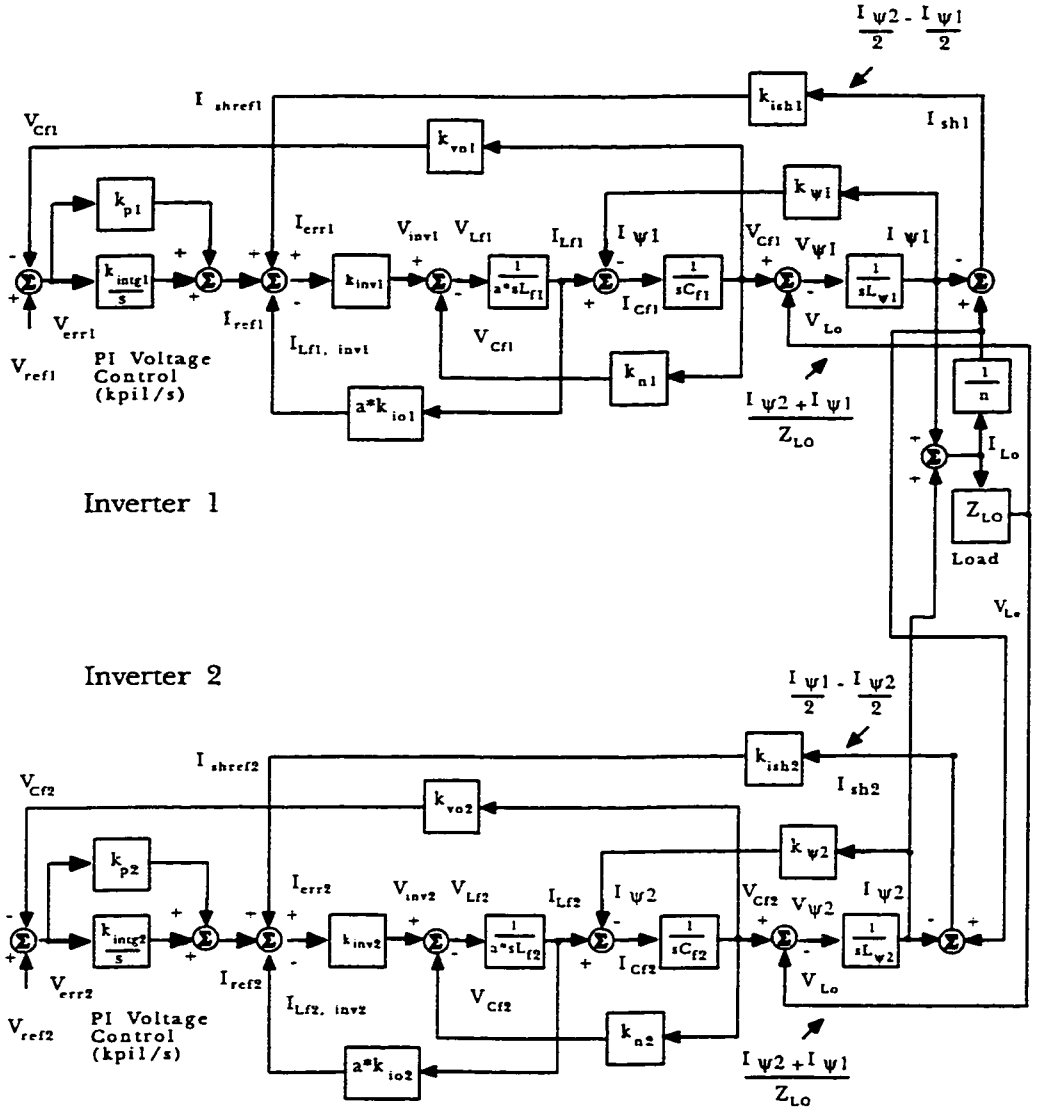


Fig. 4.3. The equivalent circuit with two converters and the current sharing controller.

two converters (MATLAB) as well as a PC- based mixed-mode circuit simulator (PSIM, PSPICE). Thus, the stability of the system will be assessed from reduced order models that can be compared with the performance results obtained from the power-circuit simulation software.

The circuit of Fig. 4.4 shows two CM's connected in parallel with the current sharing control loop in place. The state space description of this system is

$$\begin{aligned} \dot{x} &= A\,x + B\,u \\ y &= C\,x + D\,u \end{aligned} \tag{4.11}$$

where the state variables are i_{Lf1}, i_{Lf2}, v_{Cf1}, v_{Cf2}, $i_{L\psi 1}$, $i_{\psi 2}$, k_{PI1}, and k_{PI2}. The state vector is given by

$$\dot{x} = \left| \dot{k}_{PI1}\ \dot{i}_{Lf1}\ \dot{v}_{Cf1}\ \dot{i}_{L\psi 1}\ \dot{k}_{PI2}\ \dot{i}_{Lf2}\ \dot{v}_{Cf2}\ \dot{i}_{L\psi 2} \right|^{T} \tag{4.12}$$

The state matrix, A, of the system is given by

$$A = \begin{vmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{vmatrix} \tag{4.13}$$

The submatrices A_{11} and A_{22} are

$$A_{11},\ A_{22} = \begin{vmatrix} 0 & 0 & a_{jk13} & 0 \\ a_{jk21} & a_{jk22} & a_{jk23} & a_{jk24} \\ 0 & a_{jk32} & 0 & a_{jk34} \\ 0 & 0 & a_{jk43} & a_{jk44} \end{vmatrix} \tag{4.14}$$

where j = k and j,k = 1 ... m, n. Note that m = n since the system matrix is square. The elements of the state submatrix Ai,j corresponding to the n th converter are

$$a_{13} = -k_{von} \cdot K_{intgn}$$

$$a_{21} = \frac{k_{invn}}{L_{fn}}$$

$$a_{22} = -k_{ion} \cdot \frac{K_{invn}}{L_{fn}}$$

$$a_{23} = \frac{-k_{von} \cdot k_{pn} \cdot k_{invn} - 1}{L_{fn}}$$

$$a_{24} = \frac{-k_{invn}}{n \cdot L_{fn}}$$

$$a_{32} = \frac{1}{a \cdot C_{fn}}$$

$$a_{34} = \frac{-1}{a \cdot C_{fn}}$$

$$a_{43} = \frac{1}{L_{\psi n}}$$

$$a_{44} = \frac{-Z_{Lo}}{L_{\psi n}}$$

The off-diagonal submatrices, in this case A_{12} and A_{21} contain the inter-module transmission parameter, the output current from the n - 1 other converters. These submatrices are given by

$$A_{12}, A_{21} = \begin{vmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & a_{jk_{24}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & a_{jk_{44}} \end{vmatrix}$$

where

$$a_{j,k_{24}} = \frac{k_{imvn}}{N \cdot L_{fn}}$$

and N is the number of converters in the system, n is the corresponding diagonal submatrix with p representing the output current of the CM associated with that column of the system matrix, $p \neq n$.

The eigenvalues of the state matrix are negative for values of the proportional gain kp ≥ 1.0. This is consistent with the models of the CM developed earlier. Figure 4.4 shows the root locus plot of the output of each converter with respect to a step input at the reference voltage. Also, the effect of the output current of the other N modules is shown. The step

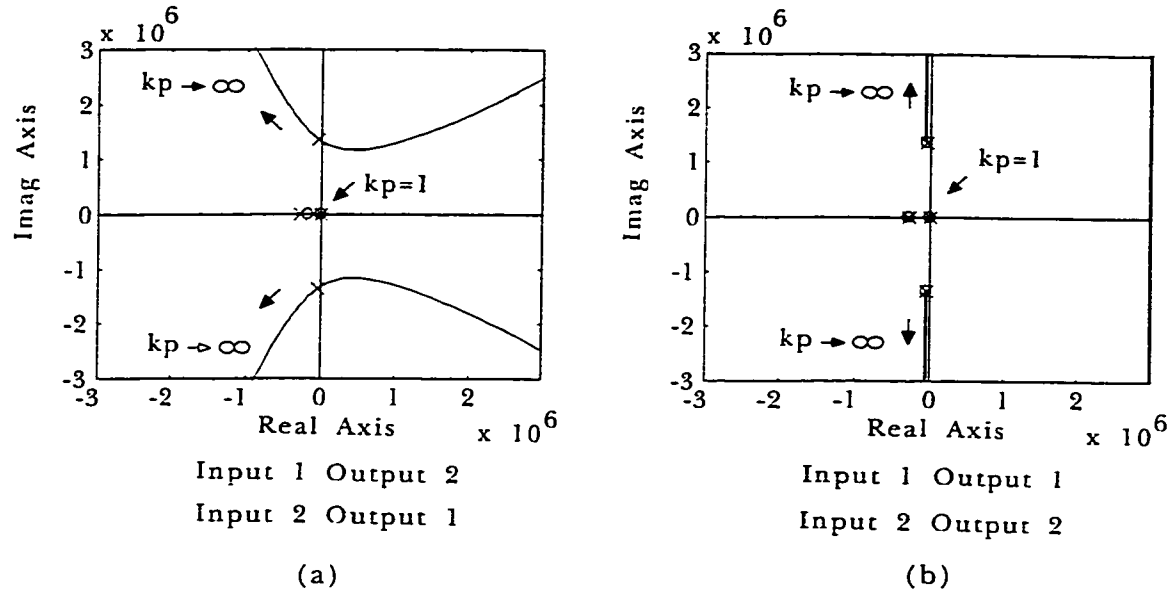


Fig. 4.4. The root-locus plot of the two-converter system. (a) The effect of the current share signal on the output of each converter. (b) The response of each converter due to the voltage reference.

response curves for the two converter system are shown in Fig. 4.5. These curves are also consistent with the performance of the individual CM. The results of the root locus, step response, and eigenvalue analysis indicate that the system of two parallel connected converters will be stable and that the performance can be extended to systems consisting of any number of parallel connected modules having the same design specifications and characteristics as those presented here. Thus, with a preliminary assessment of the stability of the system completed, the simulation software can be used to investigate the performance of larger systems of converters

4.4 The Current Sharing Control Circuit

The current sharing signal can be transmitted to the individual modules through a dedicated carrier or communication channel or through the critical output bus. The use of

the output power line as a communications channel is common in the electric power industry and can be adapted for use with the proposed system [20] [23] [24]. The strategy is to have each CM generate two frequency-modulation (FM) signals. One signal corresponds to the amplitude of the current that is being supplied by that CM and the other represents the phase angle between the output voltage of the converter and the output current. Thus, on the output bus, there will appear $2n$ individual FM signals where n is the number of paralleled modules. The signals for each current parameter will be transmitted in separate frequency ranges. The value of the output current amplitude for all modules on the critical bus could be broadcast in the range of 1 kHz to 5 kHz with 1 kHz representing 0 A rms and 5 kHz representing a maximum rms current value. Similarly, the phase angles could be broadcast in the range of 6 kHz to 10 kHz. To decode the total FM signal, each module will include two demodulators which will receive the FM signals of all CMs on the bus in the two bands and determine the correct share of the total current required by each CM as well as the average phase angle.

4.4.1. The Description of the Current Sharing Controller

As shown in Fig. 4.6 each of the two sending units of every CM's current sharing controller (CSC) consists of a peak-to-rms converter and a voltage controlled oscillator (VCO). In addition, the phase angle circuit includes a subcircuit that detects the power angle and produces a dc quantity. The current amplitude circuit converts the output current to an rms quantity which determines the frequency of oscillation of the VCO over a linear range as shown in Fig. 4.7. The FM current signal from the VCO is then injected into the critical bus. The receiving circuit of the CSC collects the aggregate FM signal and produces a

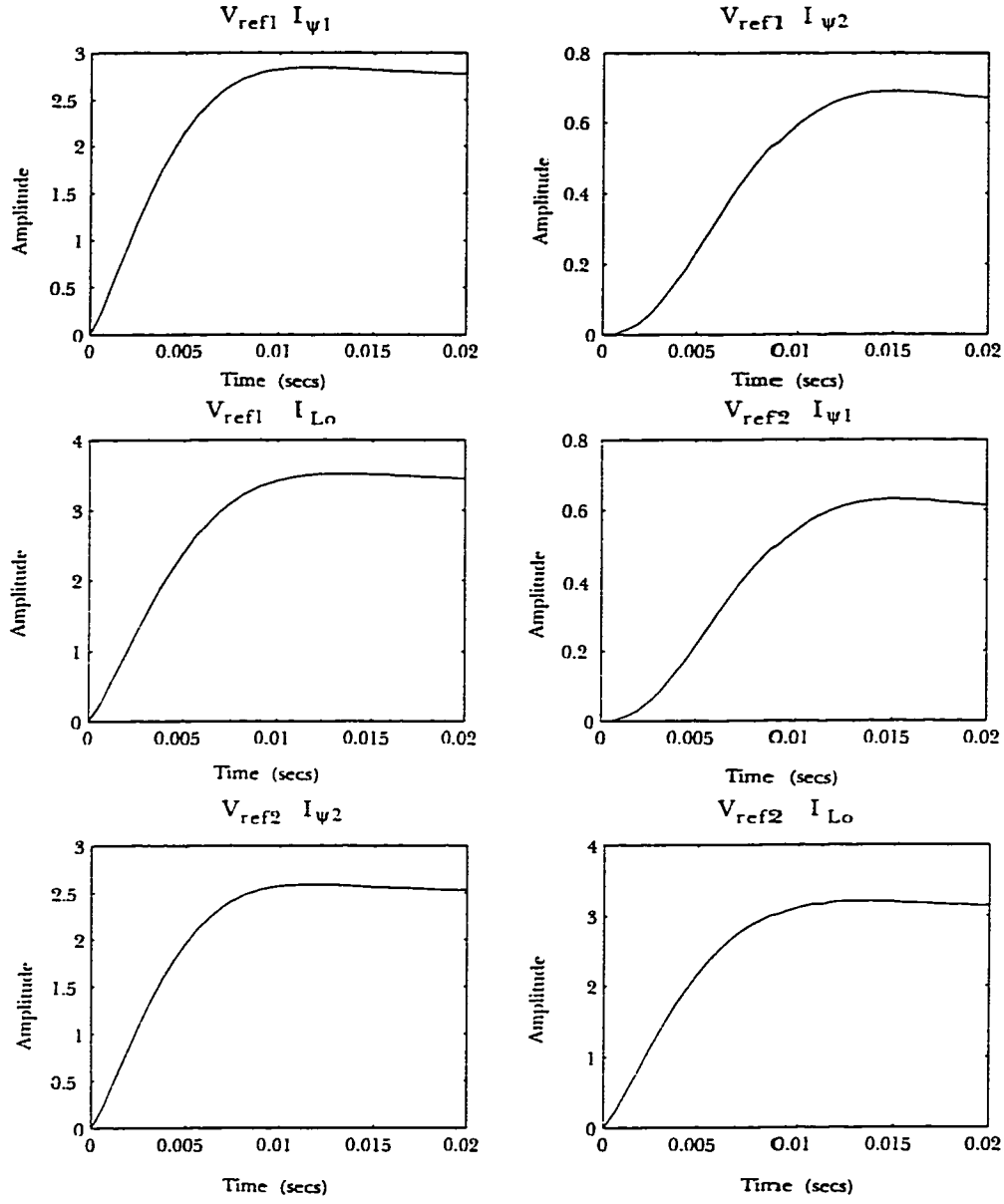


Fig. 4.5. The step response of a system composed of two converters with a 1.0 pu, resistive load.

weighted frequency estimate that corresponds to the ideal current to be supplied by each CM.

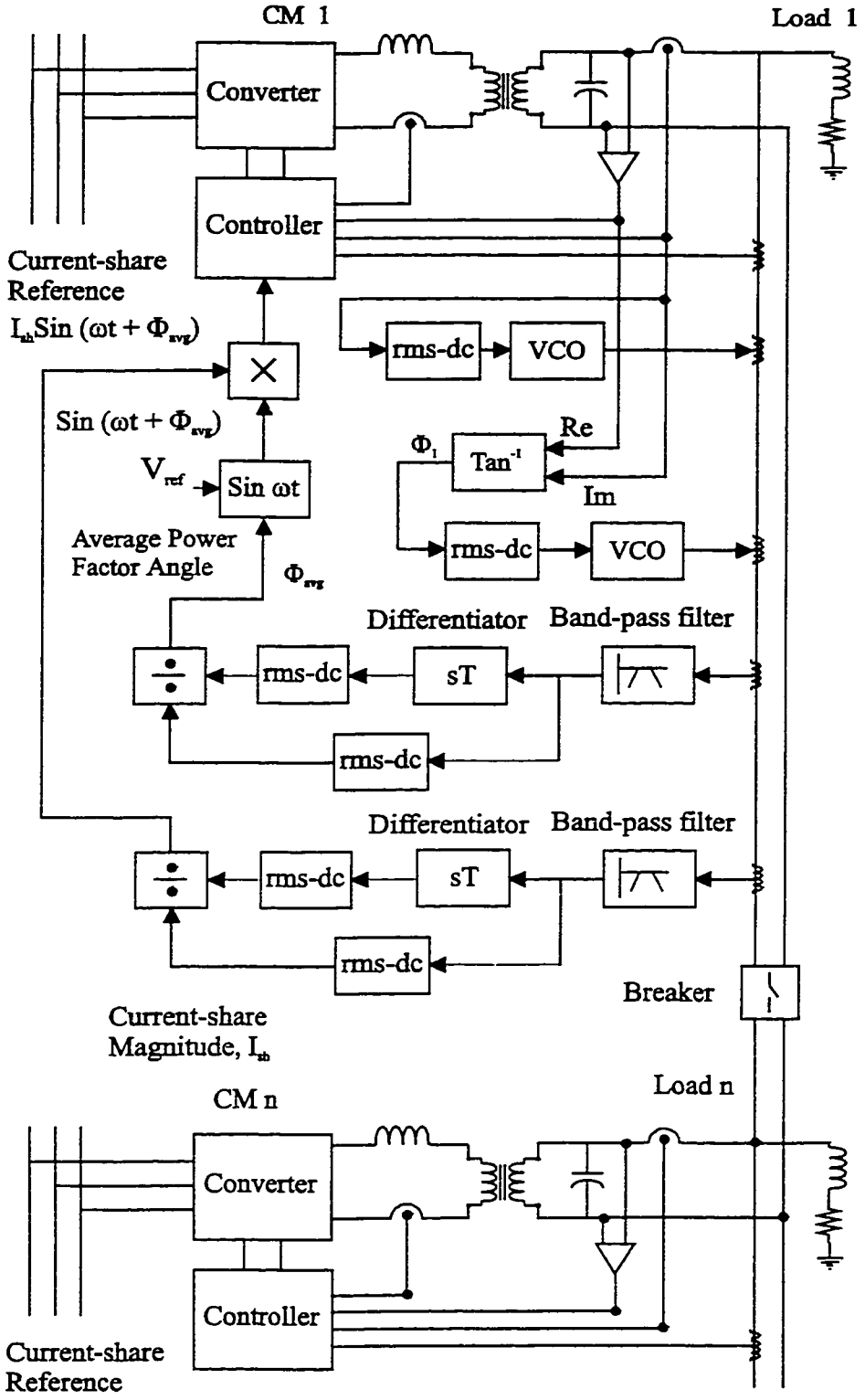


Fig. 4.6. The current share control circuit with the amplitude and phase communication circuits.

4.4.2. The Frequency Modulated Communication Scheme

Following the analysis of Perreault, et al., the aggregate signal is a sinusoid *x(t)* which is made up of *n* sinusoids of frequencies ω_k where $k = 1...n$ as shown in Fig. 1.6 . Note that each frequency represents the rms output current of a particular converter. This aggregate signal is filtered and resolved into two components which are divided to produce the final frequency estimate ω_{rms}. The first component is the power spectrum of x(t) which is given by

$$S_x(\omega) = 2\pi \sum_{k=1}^{N} \frac{1}{2} |X_k|^2 [\delta(\omega - \omega_k) + \delta(\omega + \omega_k)] \tag{4.26}$$

The second component is the power spectrum of x(t) after it has been passed through a filter H (ω) and is given by

$$S_x(\omega) = 2\pi \sum_{k=1}^{N} \frac{1}{2} |X_k|^2 |H(\omega_k)|^2 [\delta(\omega - \omega_k) + \delta(\omega + \omega_k)] \tag{4.27}$$

The rms values of the two power spectrum signals are

$$x_{rms} = \sqrt{\frac{1}{2\pi} \int_{-\infty}^{+\infty} S_x(\omega)\, d\omega} \tag{4.28}$$

and

$$x_{rms} = \sqrt{\sum_{k=1}^{N} |X_k|^2} \tag{4.29}$$

Similarly

$$y_{rms} = \sqrt{\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_y(\omega)\, d\omega} \tag{4.30}$$

and

$$y_{rms} = \sqrt{\sum_{k=1}^{N} |X_k|^2 |H(\omega_k)|^2} \tag{4.31}$$

The frequency which corresponds to the required current is found by dividing 4.31 by 4.29.

$$\omega_{rms} = \frac{\sqrt{\sum_{k=1}^{N} |X_k|^2 |H(\omega_k)|^2}}{\sqrt{\sum_{k=1}^{N} |X_k|^2}} \tag{4.32}$$

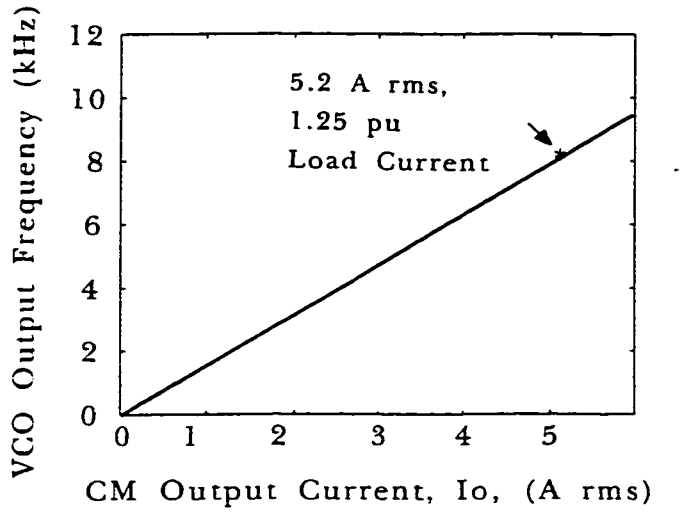


Fig. 4.7. The relationship between the output current magnitude and the VCO generated signal.

Thus ω_{rms} is the demodulated FM signal which is used in the separate controllers (current amplitude and phase) as components that are combined to produce the current share reference signal shown in Fig. 4.6.

4.4.3. The Simulation of the Frequency Modulation Controller

The circuit required to send and receive the FM current sharing information can be modeled using software designed for power circuits. The circuit used to simulate the current sharing loop is shown in Figs. 4.8. The circuit is composed of two parts, each with two subcircuits, (i) the upper section which sends and receives the amplitude of the output current signal and (ii) the lower section which calculates the average phase angle of the current-

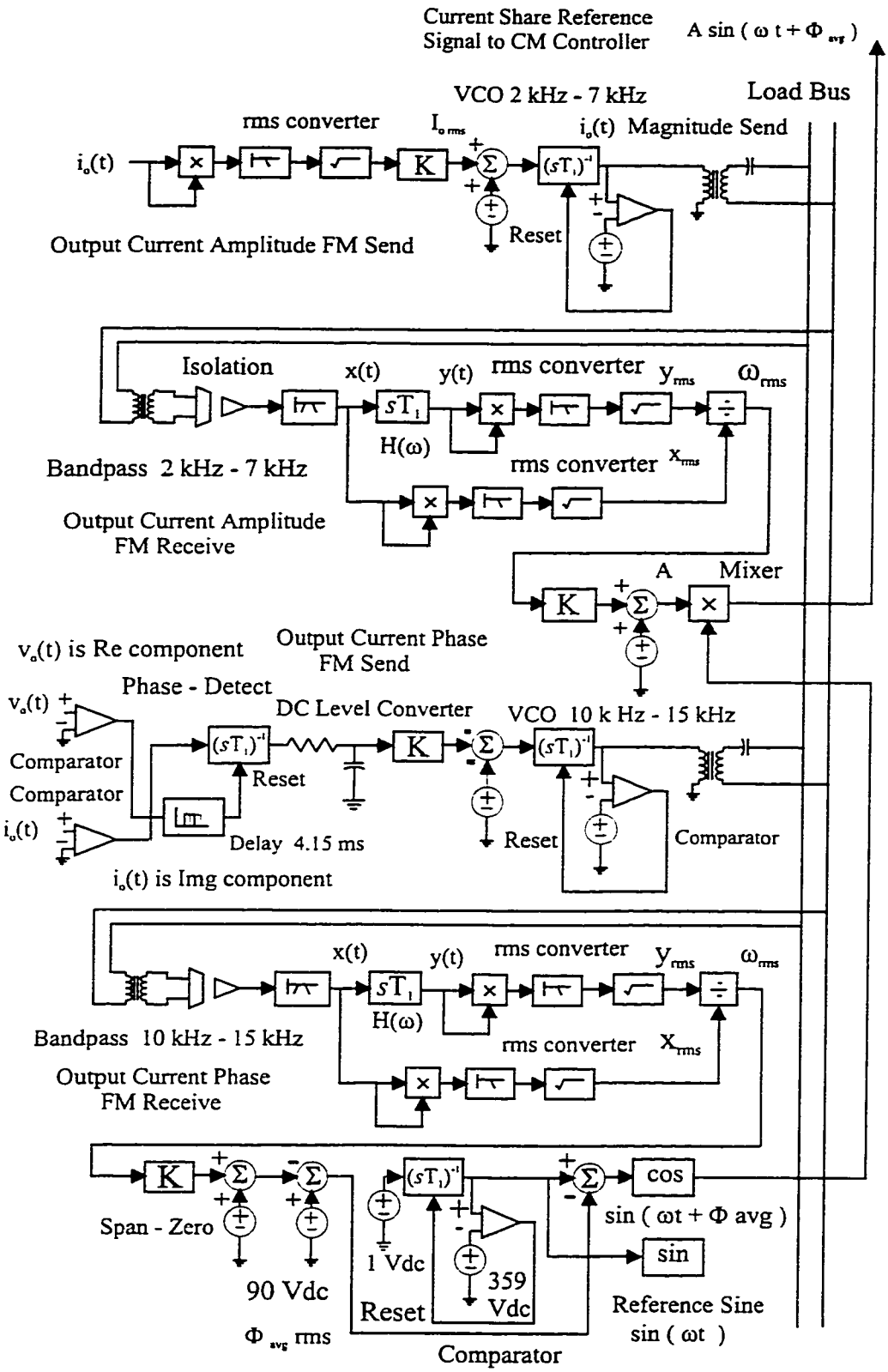


Fig. 4.8. The simulation circuit of the current share amplitude and phase modulation and demodulation subcircuits.

share reference.

In the first subcircuit the individual CM current is sensed at the output of the filter and sent to an rms converter which provides the input signal to the VCO. This FM signal is amplified and transferred to the critical bus. Thus, the rms value of the amplitude component of the output current $i_o(t)$ of each CM is broadcast in a particular frequency range (2 kHz to 8 kHz in the example given). By controlling the amplitude of the injected current, the magnitude of the harmonic which eventually appears on the bus voltage can be limited to an acceptable level.

Beneath the output current modulating subcircuit is the demodulating circuit that senses the combined input of all of the FM current-amplitude signals on the bus. This circuit accepts the filtered aggregate of the desired bandwidth and passes this signal, x(t), through two channels. The one channel, y(t), is weighted by passing through a highpass filter and then the rms value is found, y_{rms}. The rms value of x(t) is found and x_{rms} becomes the divisor while y_{rms} is the numerator. The quotient, ω_{rms}, is a dc quantity that represent the desired average value of the amplitude of the current share template. This division effectively allows the demodulation circuit to divide the total current output of the converters on the bus by the total number of converters on the bus. Finally, the amplitude signal is sent to a multiplier where it is combined with the signal from the current-share phase angle demodulator.

The signal that quantifies the average phase angle as required by the current-share template is determined in the CM phase angle modulation and demodulation sections. The output voltage, $v_o(t)$, and current, $i_o(t)$ of each converter unit is passed through a phase detection circuit. The detector produces a dc pulse whose width is transformed into a dc

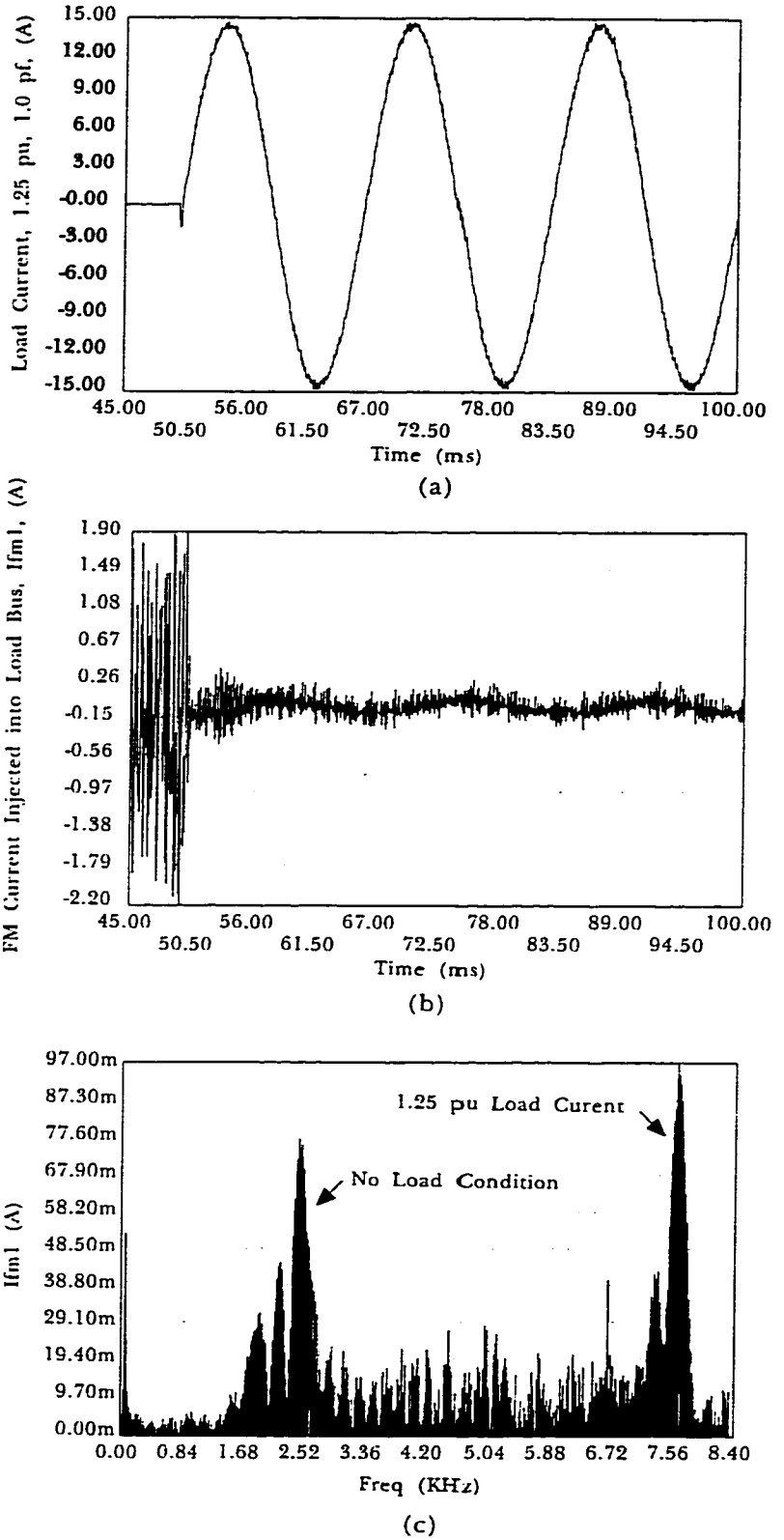


Fig. 4.9. The simulation of the current-share circuit. (a) The load current. (b) The injected current. (c) The spectrum of the injected current for three cycles.

signal that varies in amplitude as the power phase angle (and pulse width) varies from 90 degrees leading to 90 degrees lagging. As before, the dc quantity is sent to a VCO operating over a different frequency range (11 kHz to 15 kHz) from the one used by the current-amplitude circuit presented above.

The last of the four subcircuits is the average phase-angle demodulation section. As with the current-amplitude demodulator, the combined FM signals of all contributing CMs are filtered in a dedicated bandwidth (10 kHz to 15 kHz). The output signal ω_{rms} is phase shifted and compared with the ouput of a VCO. The difference is a dc signal, Φ_{avg}, that represents the average power angle of all the converters tied to the output bus. This signal can now be passed to a signal generator that produces the current-share sinusoid, sin ($\omega t + \Phi avg$). The phase-adjusted sinusoid with unit amplitude is now multiplied by the amplitude A determined previously in the current-amplitude demodulation subcircuit. The results of the simulation of the FM current-share circuit are shown in Fig. 4.9 and Fig. 4.10.

4.5. Summary

The control circuit of a converter module that is to be part of a system of n identical, parallel connected converters is presented and the design is developed at two levels i) the individual CM and ii) the complete system. The basic CM control scheme is based on the need to determine three currents in the CM circuit. First, the total current at the output of the inverter is monitored to prevent overcurrent surges. A second outer control loop determines the voltage at the filter capacitor and hence the output voltage. The capacitor voltage is translated into the capacitor current by means of a PI controller. The third current loop is the

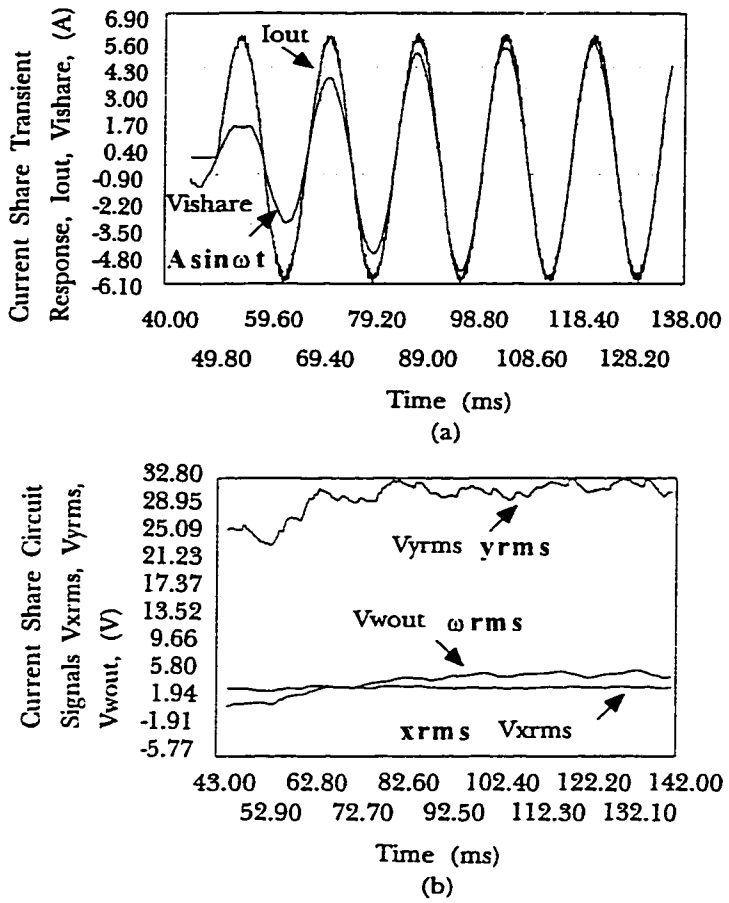


Fig. 4.10. The waveforms produced by the FM current-share circuit (amplitude subcircuit). (a) The output current and current share template, Asin ωt. (b) The rms outputs of bandpass filter, highpass filter, and rms division

output current that is delivered to the ac bus. This parameter is a current sharing element that forces each CM to limit its output to a proportion determined by the number of converters connected to the ac bus. Finally, a frequency modulation communication technique is proposed so that the current sharing reference can be transmitted to every CM without requiring a separate communication channel. To accomplish this, each CM broadcasts two signals, each signal in its own frequency band. One signal corresponds to the amplitude of

the output current and the other signal is the phase with respect to the output voltage. Each CM then receives, over the output bus, the composite of the output-current amplitude and phase signals contributed by all the converters on the bus. Each converter then decodes the composite signals in their respective bandwidth and determines the average output current amplitude and phase angle. The two current-share template components are then multiplied in each CM and returned to the control circuit as the output current reference. At the system level, a state-space model of the complete circuit is presented in order to establish the fundamental stability of the control scheme. The presentation of the results of the testing of the system is developed in the following chapter.

5. PERFORMANCE OF THE CONVERTER MODULES

5.1. Testing The Converters

In order to test the effectiveness of the design of the power system, the control subcircuit, and the converter module, the converters are tested by simulating their performance using a computer software package. A PC-based simulation program designed for power and power electronic circuits, PSIM, is used to examine the response of the unit CM and the system before the final testing is done using the experimental prototype. The test procedures are based on the published standards (IEC, IEEE) and practices common to the UPS and power quality sectors of the electrical industry. The results of the computer based testing are compared to performance criteria offered by these same bodies. The simulation includes the power subcircuit and the FM current share scheme. Both transient and steady-state characteristics are observed as needed in order to establish the feasibility of the paralleling strategy. Examples of the circuit processed by the simulator are included in this section (and the Appendix) as well as results of all testing.

5.2. Design Criteria and Performance Objectives

There are two classes of criterion that will be used establish the performance of the individual CM and the total system: i) the transient response requirements and ii) the steady state characteristics including harmonic distortion. Performance standards relating to the

operation of UPS's and power conditioning circuits in general are developed by the following bodies:

i. Institute of Electrical and Electronics Engineers (IEEE)

ii. American National Standards Institute (ANSI)

iii. National Fire Protection Agency (NFPA)

iv. National Equipment Manufacturers Association (NEMA)

v. International Organization for Standardization (ISO)

vi. International Electrotechnical Commission (IEC)

The values used for performance testing of the proposed system are drawn from the IEEE/ANSI and ISO/IEC published standards, in particular, IEEE Std. 519-1992, IEEE 446 (IEEE Orange Book), and IEC 1000-3-2 [38][39][40][33]. Table 5.1 gives the harmonic standards for the voltage and the current output waveforms.

The transient response of the individual CM's as well as the response of the system is given by IEEE Std 446-1987. The range of power factor for the load is given as 1.0 PF to 0.8 PF lagging. However, this range could be expanded to include 0.8 PF leading and a wider range of nonlinear loads. The normal industrial voltage recovery specifications state that:

i. The voltage must return to within 5% after ½ cycle (0.0833 s) for 100% load application or removal.

ii. The maximum deviation of the voltage is 10% average per ½ cycle for 100% load application or removal.

This specification can be expanded to include a step change of 125% load application or

Table 5.1.. THE STEADY STATE PERFORMANCE SPECIFICATIONS

PARAMETER	SPECIFICATION
Harmonic Distortion, Voltage Waveform	Maximum of 5% Total Harmonic Distortion, THD, (Maximum of 3% THD for Special Applications, Hospitals and Airports.) Individual Voltage Distortion Less than 3%, IEEE Std 519-1992, pp. 85.
Notch-Depth, Voltage Waveform	Maximum of 20% for General Systems, Maximum of 10% for Hospitals and Airports, IEEE Std 519- 1992 pp. 77. (d/v * 100)
Notch Area, Voltage waveform	Maximum 22, 800 (usec*V) for General Systems. Maximum 16,400.0 for Hospitals and Airports, Ieee Std 519-1992, pp 77.
Current Distortion Limits	Total Demand Distortion (TDD) For Odd Harmonics, h<11,< 4% Iload, 11<= h<17 , < 2%, 17<=h<23, <1.5%, 23<=h<35, <0.6%, 35<=h, ,0.3%. IEEE Std 519-1992 pp. 78.
Current Harmonic Limits	Maximum Currents for h=3, 2.3A, h=5, 1.14A, h=7, 0.77A, h=9, 0.40A, h=11, 0.33A, h=13, 0.21A 15<=h= 39, 2.25/h, for h=2, 1.08A, h=4,0.43A, h=6,0.3A, 8<=h<=40, 1.84/h. IEC 1000-3-2.
Current Harmonic Limits	Maximum THD Current 5%, IEEEStd 446-1887.

removal. These requirements apply equally to both the individual converter and the system as a whole.

In addition to the normal performance tests, other failure modes can be evaluated through

simulation. This nondestructive testing has the advantage of safety and repeatability. Essentially, this is testing for recovery of the system from a loss of synchronization of one or more of the CM's. The abnormal modes can be classified as shown in Kawabata et al [23]. The effects of voltage amplitude imbalance, voltage phase imbalance, and voltage frequency imbalance can be investigated and the resulting circulating currents, higher harmonic crosscurrents, ripple in the dc bus, magnetizing currents, resonant conditions, and potential dc bus overvoltages can be documented.

5.2.1. The Selection of Power System Components

The elements that are used to construct both the simulation and the prototype circuits can be described as per unit quantities where necessary. The use of per unit values allows direct comparison between the results obtained from the software simulation and the experimental circuit. This is necessary because the simulation is based on an idealized CM and interconnected system while the test circuit is modified to accommodate the availability of components and the limitations of the breadboard circuit construction.

The base quantities are the output power (P_{base}, W) and the voltage at the output bus (V_{base}, V_{rms}). From these values the base current (I_{base}, A_{rms})and the base impedance (Z_{base}, Ohms) are derived. The base frequency is 60 Hz or 376.9 rad/s. The components to be considered in both the simulation and the prototype circuits are divided into seven classes by circuit subsection:

1). The pre-rectifier input filter.

2). The dc bus filter.

3). The power switches and snubber components.

4). The inverter output filter and the transformer.

5). The static switch.

6). The load impedance.

7). The FM circuit.

The values of the subcircuits processing ac currents and voltages are based on the per-unit impedance while the dc bus components and the switches are based on the value of the voltage or current they must carry.

5.2.2. The FM Communications Scheme

The effectiveness of the FM communications scheme must be examined with respect to the contribution of the modulated signal to the voltage and current THD. Also, the possibility that interaction between the inherent system resonances and the FM program can be investigated. It is assumed that if the standard limits are placed on i) the value of the voltage and current THD and ii) the values of the individual harmonics then the FM signal will not create radio frequency interference (RFI).

5.3. The Simulated Techniques for the Converter Modules

The performance of the individual CM's, their subcircuits and a system composed of three converters is simulated with PC-based software packages. Waveforms are produced for steady-state and transient circuit operation at both the CM and the system level. The simulation packages offer a limited prediction of the capability of the individual converters

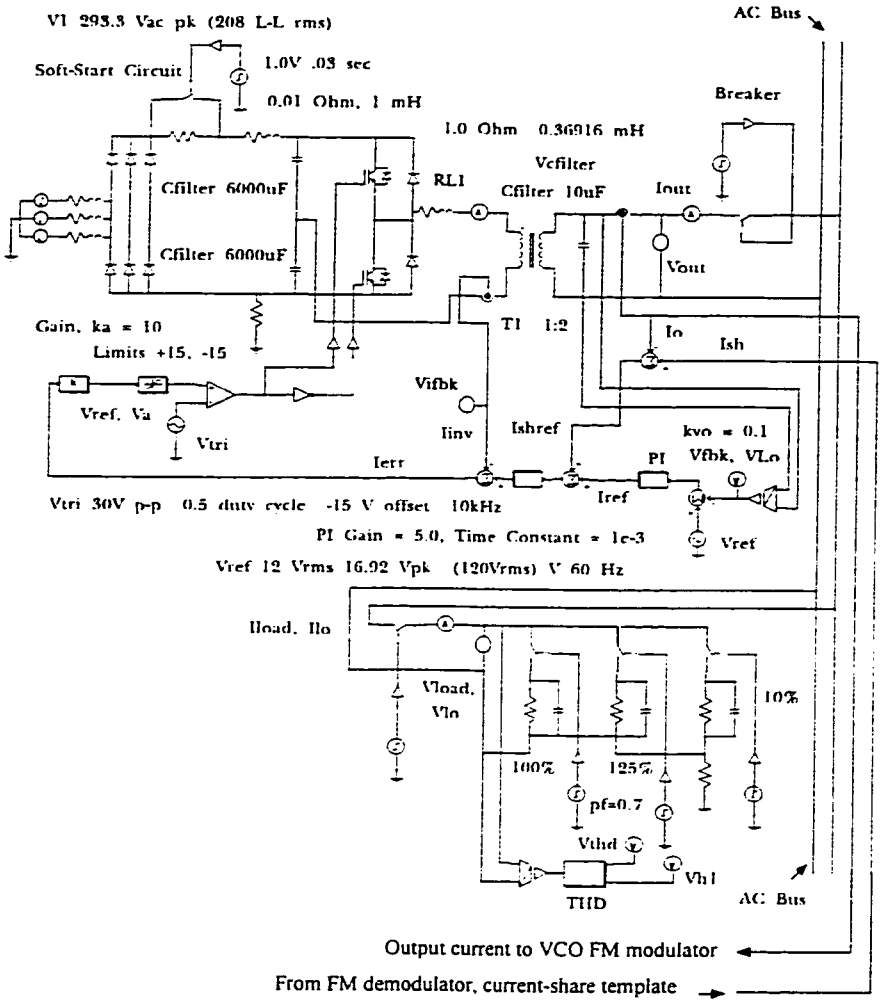


Fig. 5.1. The simulation software model of the inverter and controller sections of an individual basic converter module.

and the performance of the system as a whole. Also, the output from the software packages can validate the previous analysis with respect to system stability .

5.3.1. The Simulation Software and Circuit Models

The proposed strategy for the control of the individual converters and the system as a whole is tested using two simulation packages, PSpice and PSIM [41][42]. PSpice is a device-oriented simulation package which has the advantage of approximating the

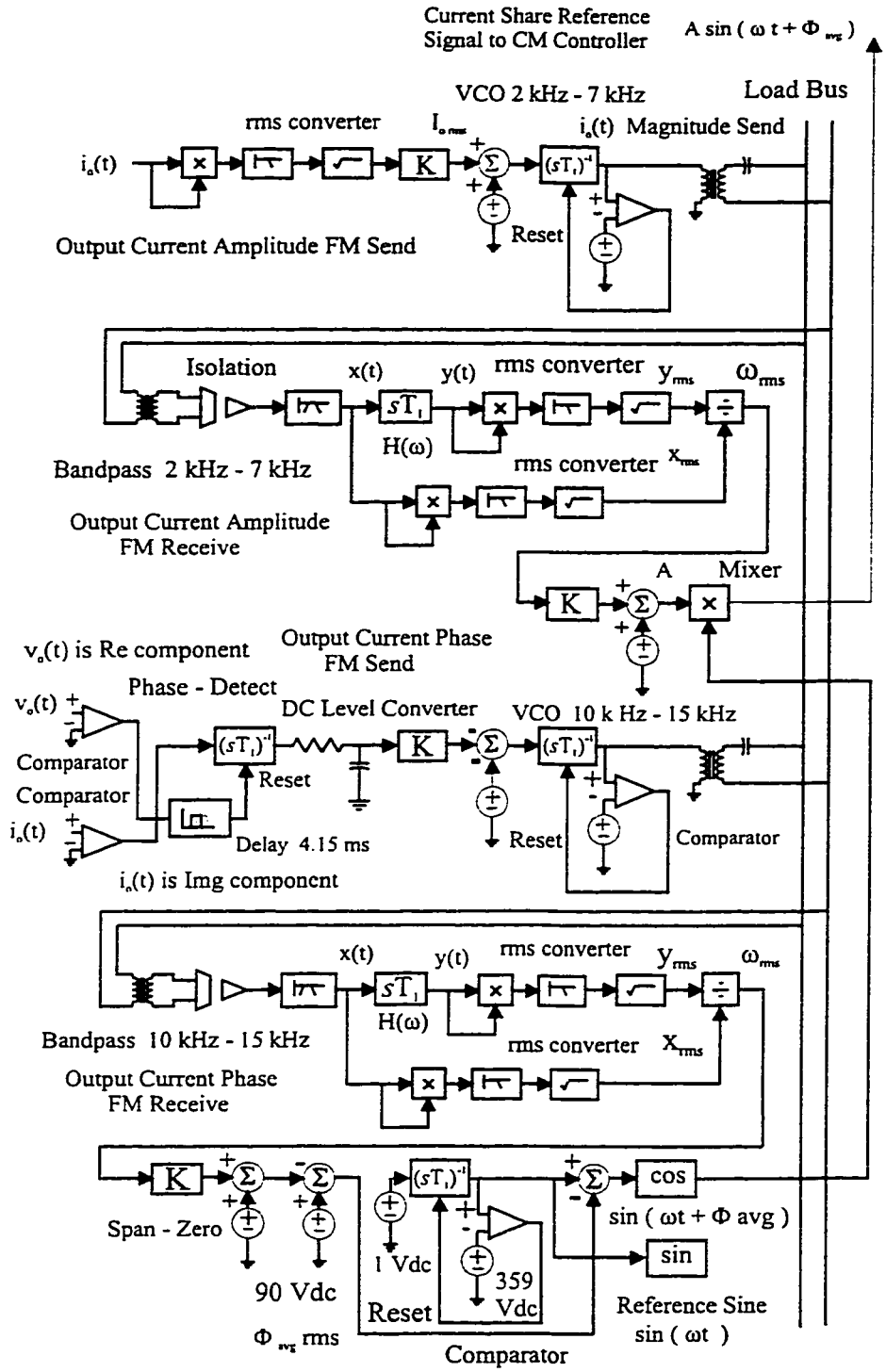


Fig. 5.2. The current-share template circuit used for simulation.

performance of specific electronic components. There is a disadvantage, however, in that simulation of large circuits is time consuming and convergence is not assured for nonlinear

circuits (diodes). PSIM is a mixed-mode, analog and function-block simulation package that can accommodate nonlinear power-circuit components and circuits and simulate their performance quickly. However, convergence is still a problem and many common circuits cannot be modeled easily if the function is not included in the software.

The strategy employed here is to use the PSIM software where speed is important and the component models are available. PSpice is used to confirm the performance of specific subcircuits using manufacturers component models while PSIM is used to determine the response of the system as a whole.

5.3.2. The Simulation software schematic

The PSIM schematic of the basic converter is shown in Fig.5.1 and Fig.5.2. These two sections represent a single module which is repeated as necessary to obtain the required total current required by the load. Figure 5.1 includes the CM power components, the load, and control section and Fig. 5.2 represents the FM load-current sharing controller. The input to the power section is the connection to the three-phase utility or mains bus through an input filter that consists of three inductors L_a, L_b, and L_c. The output of the CM is the connection to the critical bus (I_{out}, V_{out}) and the control signals I_o, V_{Lo}, and I_{inv}. The inputs to the CM control section are the signals I_o, V_{Lo}, and I_{inv} as well as the current share signal, I_{sh}. These signals correspond to the control loops developed in Chapter III. The signal V_{ref}, generated by an independent source, could also be a PLL fed from the utility or mains bus. Also shown in Fig. 5.1 is the load arrangement, in this case 0.7 PF leading, in three stages (0.1, 1.0, and 1.25 pu).

Figure 5.2 shows the FM current-share controller circuit. This circuit is composed of two sections, the load current-to-frequency converter subcircuit and the current-share reference-signal generator subcircuit. The input to the current-to-frequency converter is the current output by an individual CM, I_o, and the output of this section is the output from the VCO that is actually a frequency modulated current which is injected into the critical load bus, I_{fm}. The FM demodulation circuit that is used to generate the current-share reference accepts, as an input, the voltage of the critical bus. The output of this section is the current sharing signal, I_{sh}. To test the performance of the proposed system, three converters were connected and the characteristics of the units and the system were observed.

The simulation circuit components are based on a 500 W load, P_{base}, and a load bus voltage of 84.87 V_{rms} (120 V_{peak}). Thus, the base current is given by

$$I_{base} = \frac{P_{base}}{V_{base}} \tag{5.1}$$

and the base impedance is

$$Z_{base} = \frac{V_{base}}{I_{base}} \tag{5.2}$$

The per-unit values of the circuit inductances and capacitances are found by dividing their respective impedances by the base impedance. The inductors used for the input filter to the rectifier are chosen to be a .026 pu and the rectifier filter components are rated based on the output voltage and current. Thus, the dc filter inductance is rated at 10 A or 170% and the

Table 5.2. VALUES OF THE MODEL OUTPUT TRANSFORMER

Parameter	Value
Turns Ratio	1:2
Primary Resistance, Ohms	0.16
Primary Leakage Inductance, mH	0.5
Secondary Resistance, Ohms	0.64
Secondary Leakage Inductance, mH	2.0
Magnetizing Inductance, H	8.0

filter capacitor is 350 V or 413% of the output voltage.

5.3.3. The model of the inverter

The inverter section of the simulation circuit is supplied by a three-phase ac bus and a diode rectifier. A soft-start circuit has been added in order to speed the calculation of the of the dc bus voltage. The rating of the switches in per-cent of the load parameters does not apply in the case of the simulation but the output filter components and the transformer can be expressed as per-unit values.

5.3.4 The transformer, filter elements and the loads

The transformer characteristics are derived from tests done on three single-phase transformers ranging from 500 VA to 3000 VA. The PSIM model of the transformer uses the resistance of the primary and secondary coils, the leakage inductance of the same coils, the magnetizing inductance, and the turns ratio. The values assigned are given in Table 5.2.

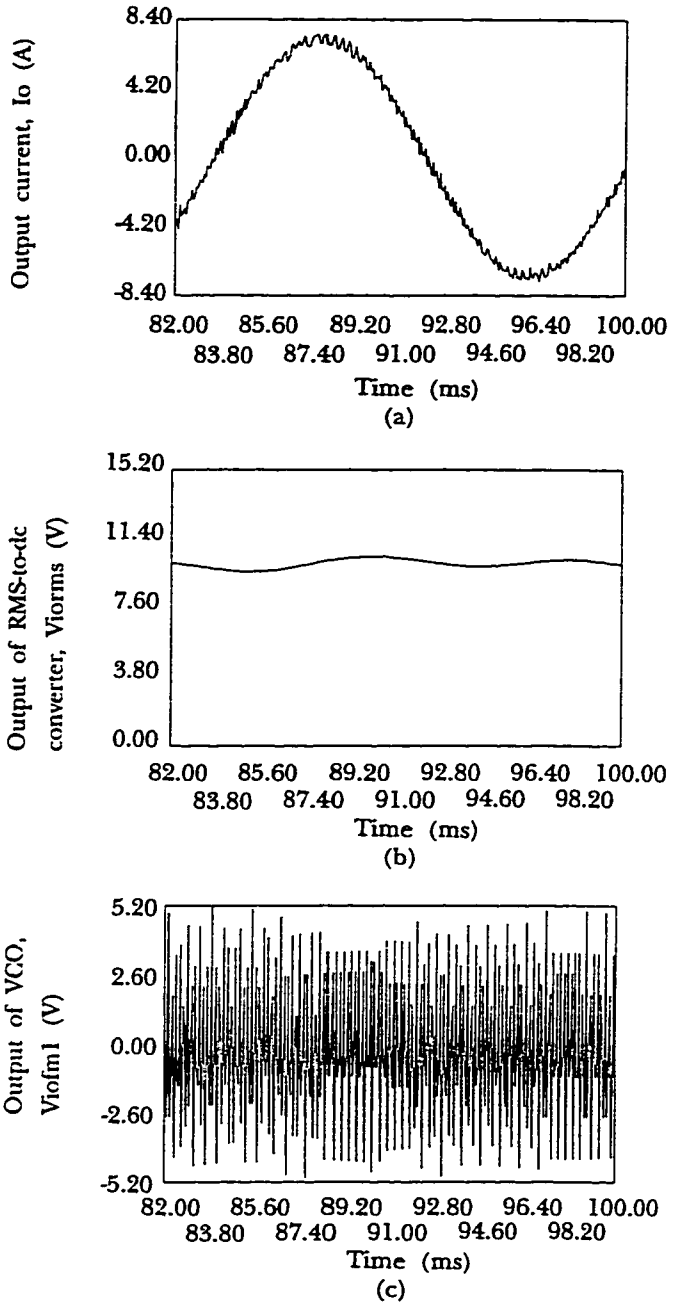


Fig. 5.3. The current-share subcircuit signal-injection for 1.25 pu and 1.0 PF load current. (a) The output current. (b) The rms-to-dc output. (c) The VCO output.

The filter is a second order LC type as described in Chapter 2.4. The curves shown in Fig. 2.10 and Fig. 3.13 mean that essentially there is a range of possible values for the

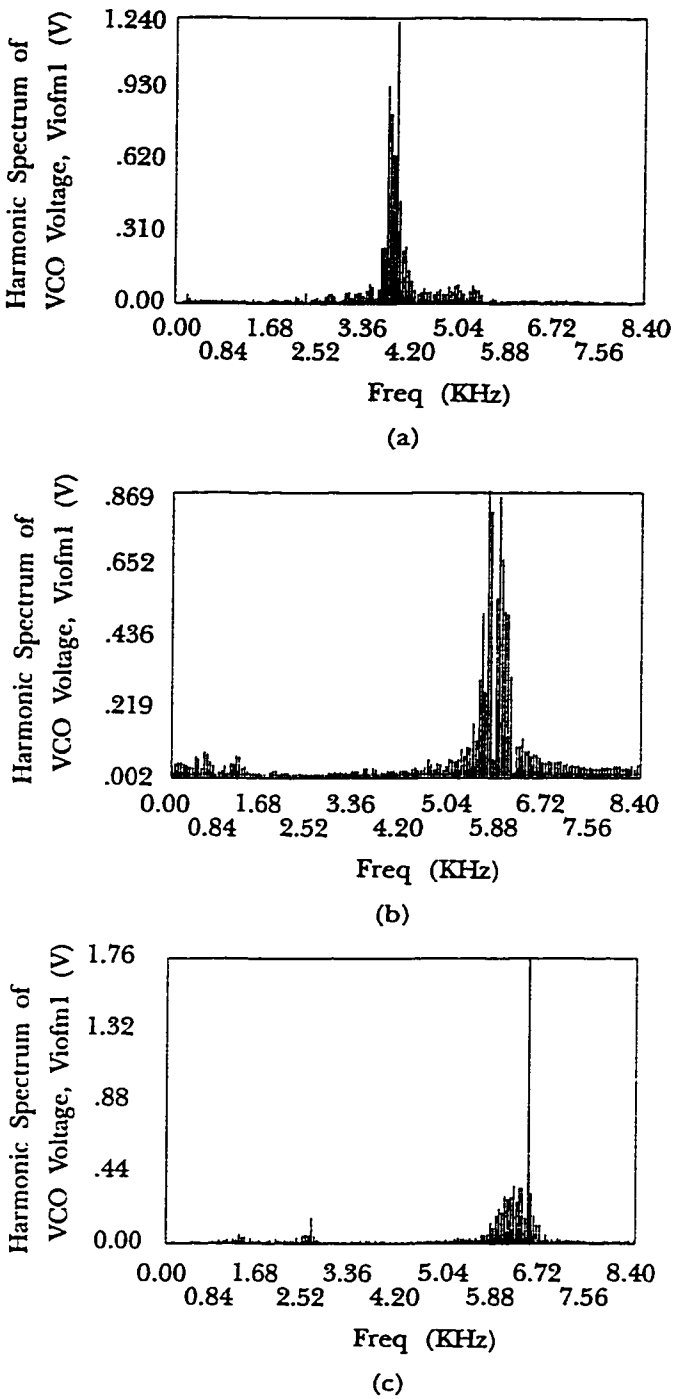


Fig. 5.4. Spectra of the broadcast current-share signals. (a) 0.1 pu load current. (b) 1.0 pu load current. (c) 1.25 pu load current.

Filter capacitor. By neglecting the effects of the transformer, the break points of the LC filter

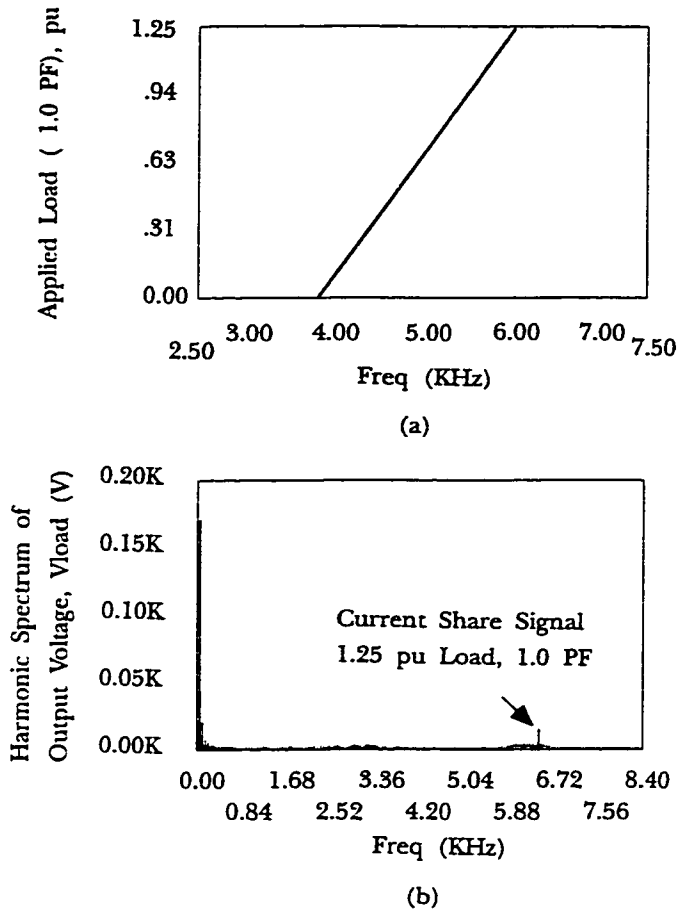


Fig. 5.5. The output of the current-share amplitude signal. (a) The frequency range corresponding to a range of loads. (b) The effect of the injected signal on the output voltage.

elements can be placed between 500 Hz and 1.6 kHz. Since these break points may represent a resonant amplitude peak, they mark the lower limit of the useful frequency range that can be reserved for the FM communication channels. Assuming that the filter inductor, L_f, is 1 mH, then the filter capacitors fall in the range of 10 uF to 100 uF. The output filter capacitor with a value of 100 uF or 0.9 pu (VA_{base} = 500) represents a break point of 500 Hz with the filter inductor at 1.0 mH is .013 pu. The 10 uF filter capacitor (9.2 pu) has a break frequency at 1.59 kHz (10 k rad/s) and both options are well below the 10 kHz switching

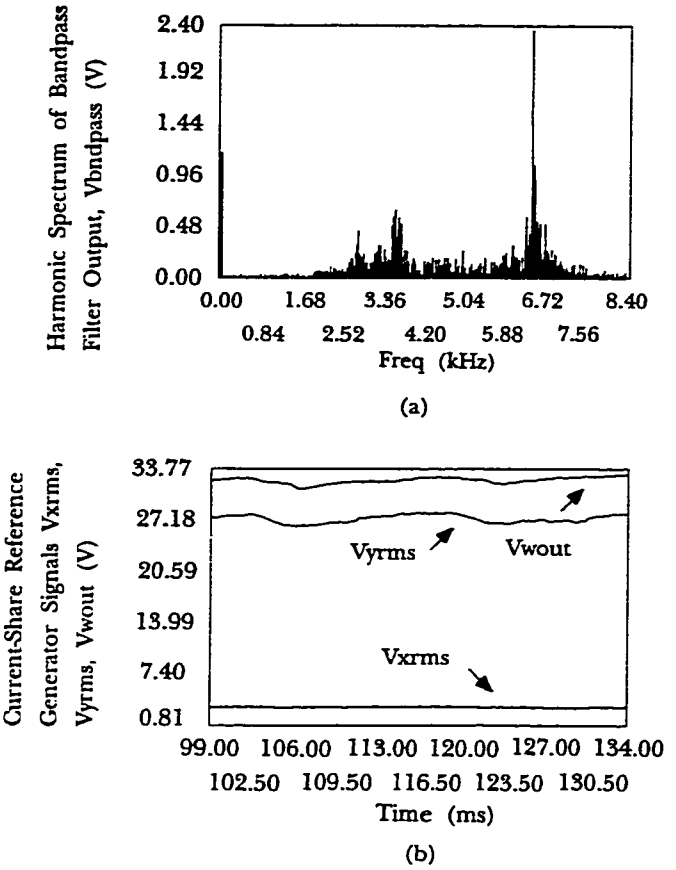


Fig. 5.6. The current-share amplitude voltages for one CM at 1pu and 1 PF load. (a) The bandpass filter output, x_{rms} . (b) The rms current division signals.

frequency. However, the lower value capacitor may create problems for the bandpass filters of the FM demodulation circuits which will have fewer decades to take advantage of the -40 dB/decade attenuation offered by the filter.

5.3.5. The control circuit

The complete control circuit includes the inner current and outer voltage control loops (Fig. 5.1) and the FM current sharing circuit shown in Fig. 5.2. The output voltage

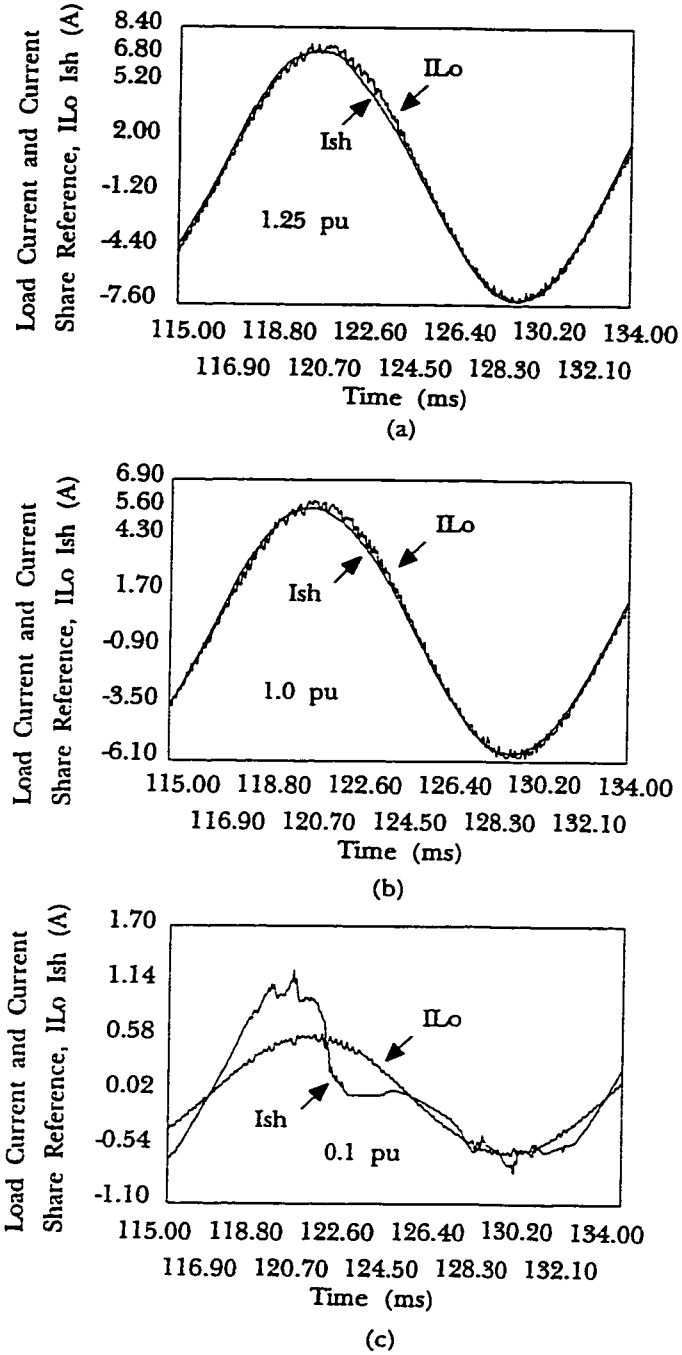


Fig. 5.7. Currents and the current-share amplitude reference waveforms. (a) 1.25 pu load. (b) 1.0 pu load. (c) 0.1 pu load.

of the CM, V_{out} or $V_{cfilter}$, is sensed as V_{Lo} and forms a negative feedback loop that is compared with the reference voltage, V_{ref}. The result of the comparison, V_{fbk}, is sent to a PI

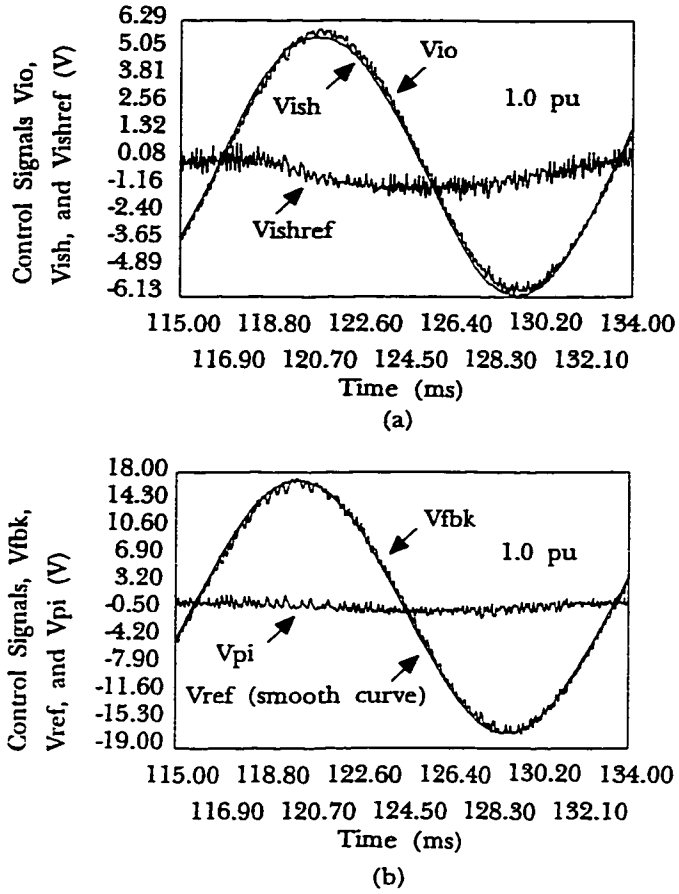


Fig. 5.8. Control circuit waveforms. (a) The current-share summing junction. (b) The outer voltage loop junction.

controller block with a gain of 5.0 and a time constant of 1.0 msec. The output of the PI section becomes the current reference, I_{ref}.

5.4. The Simulated Steady-State Response of the CM

In order to demonstrate the simulated performance of an individual CM (including the current-sharing controller), the combined circuit of Fig.5.1 and Fig. 5.2 is tested for both steady-state and transient operating conditions. In each case loads are 0.1 pu, 1.0 pu, and 1.25 pu and 1.0 PF (resistive).

5.4.1. The steady-state response of the control and current-sharing subcircuits

In the steady-state mode, the behavior of the control variables can be traced by starting with the outer current loop and by following the control action as it continues through the current share module and the inner loops. The action of the current injection module of the CM is shown in Fig 5.3. Here, the CM output current, Io, the rms value of the current, Viorms, and the output of the VCO section, Viofm1, are shown for a 1.25 pu load. The ripple associated with the rms-to-dc converter represents a trade-off with respect to the response time of the converter. The ripple shown (13%), requires three cycles (50. ms) to stabilize. The spectrum of the injected signal, Viofm1, is shown in Fig. 5.4 for 0.1, 1.0, and 1.25 pu loads. Note that the frequency of the noise injected into the critical bus increases linearly as the output current, Io, increases. This is shown in Fig. 5.5 (a). Finally, Fig. 5.5 (b) shows the spectrum of the output voltage and the contribution of the current-share signal to the total noise carried by the critical bus.

The aggregate of all the FM output current signals sent to the output bus is detected by the second half of the current share subcircuit and converted into a voltage which represents the ideal current to be output by the CM, I_{sh}. The spectrum of the current share signal that is taken from the bus and sent to the bandpass filter, Vbndpass, is shown in Fig. 5.6 (a). Since there is only one CM there is a large spectral component at the frequency corresponding to a1.25 pu load current (6.0 kHz). The signal produces two components, V_{yrms} and V_{xrms}, that are divided, scaled, and multiplied by a sinusoid to form the current share reference signal $I_{sh}(t)$. The voltages V_{xrms} and V_{yrms} are shown in Fig. 5.6 (b). The parameter

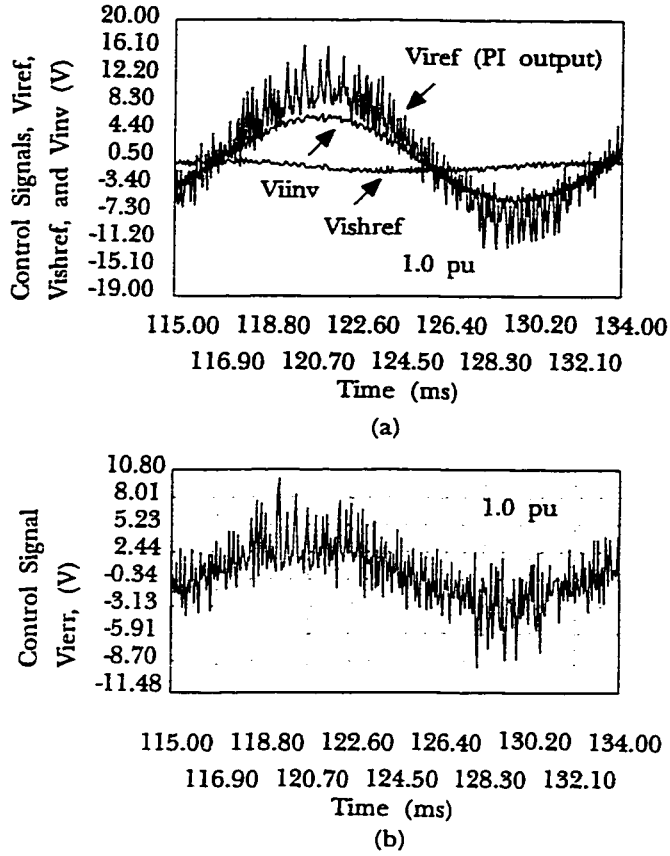


Fig. 5.9. The inner current loop summing junction. (a) The input control variables. (b) The output to the PWM comparator.

$I_{sh}(t)$, that is returned to the main control circuit is plotted with the actual output current in Fig.5.7 for 0.1 pu, 1.0 pu, and 1.25 pu loads and 1.0 PF.

The desired current is returned to the main control circuit as the parameter $I_{sh}(t)$ where it is compared with the output current of the CM, Io. This loop and the error signal, Ishref, are shown in Fig. 5.8 (a) for a 1.0 pu resistive load. The voltages representing the variables of the outer voltage loop, Vfbk, Vref, and the input to the PI section are shown in Fig. 5.8 (b).

The output of the PI controller block, Viref, and the inner current feedback junction parameters, Viinv, and Vishref are plotted in Fig. 5.9 (a). For clarity, the output of this

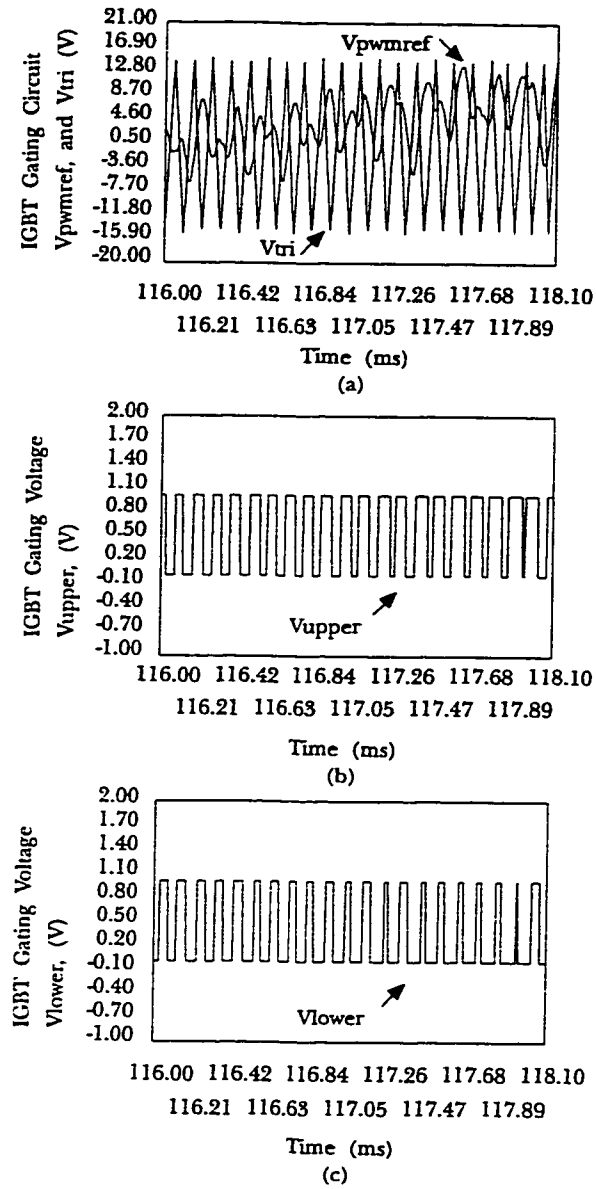


Fig. 5.10. The PWM waveforms for 1/4 cycle (45 deg.). (a) The comparator input. (b) The upper switch gating signal. (c) The lower switch gating signal.

summation, Vierr, is shown for one cycle and is represented in Fig. 5.9 (b). The carrier, Vtri, a triangle waveform, and the gating pulses to the upper and lower switches, Vupper and ,

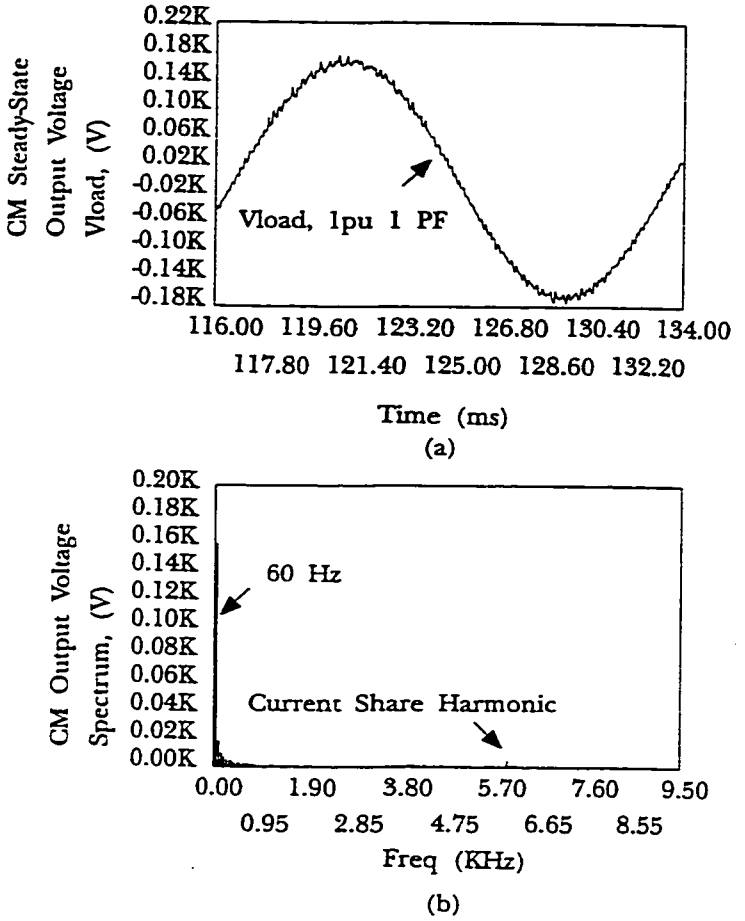


Fig. 5.11. The steady state output voltage of a single CM. (a) The voltage waveform. (b) The harmonic content for 1.0 pu and 1 PF.

Vlower, are shown in Fig.5.10(a), Fig. 5.10 (b) and 5.10 (c). Their output is restricted to a range of 45 degrees.

5.4.2. The steady state response of the power subcircuit

The output voltage and currents are given in Fig. 5.11 and Fig. 5.12 for a single converter. The load is 1.0 pu, and 1.0 PF. The THD for the voltage is 0.26 %. The response of the CM to unity and lagging 0.8 PF loads will be demonstrated as part of the simulation of

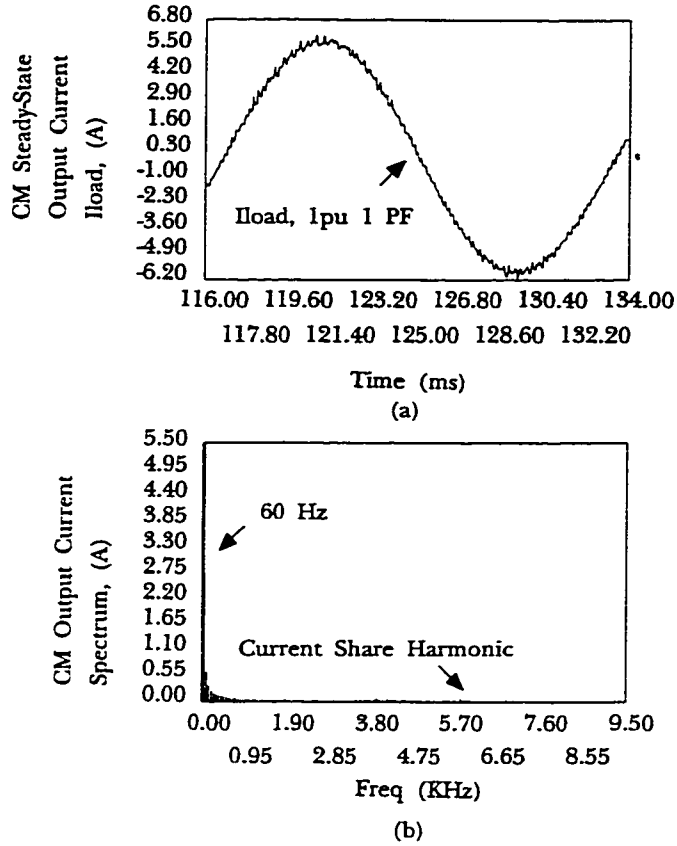


Fig. 5.12. The steady state output current of a single CM. (a) The voltage waveform. (b)The harmonic content for 1.0 pu and 1.0 PF.

the transient behavior of the circuit.

The effect of the application and removal of loads on the critical ac bus can be monitored by using the simulation software. The control variables that are of the most interest are those that determine the current sharing characteristics while the settling time and the harmonic content of the voltage and current waveforms are critical to the output of the power circuit.

5.5 The transient response of the CM control and current-sharing subcircuits

The single CM can be used to illustrate the behavior of the of the rms-to-dc converters in the current -share signal generator subcircuit. The step response of the current share subcircuit to a load of 1.0 pu at 1.0 PF is shown in Fig 5.13. The circuit variable Vioshare1 is plotted with the actual output current Iout. The load is applied at 50 ms and the waveforms converge after 5 cycles.

5.5.1. The transient response of the single-CM power subcircuit

The transient response of a single CM is evaluated in Fig. 5.14 for resistive loads of 0.1 pu and 1.25 pu. The output voltages and currents are within 5% of their final value within one half-cycle or 8.33 ms.to a load of 1.0 pu at 1.0 PF is shown in Fig. 5.14. The circuit variable Vioshare1 is plotted with the actual output current Iout. The load is applied at 50 ms and the waveforms converge after five cycles.

5.5.2. The Simulated Response to an Abnormal Operating Conditions

Degenerative conditions include changes in the reference voltage and changes in circuit parameters including the dc bus, the inverter, the control circuit, and the output bus impedance. The effect of a reference voltage imbalance was presented in section 3.4 and will be reviewed again in the context of a multi-converter system in section .3.4.

5.6. Summary

The computer software simulation of the single converter module demonstrates the

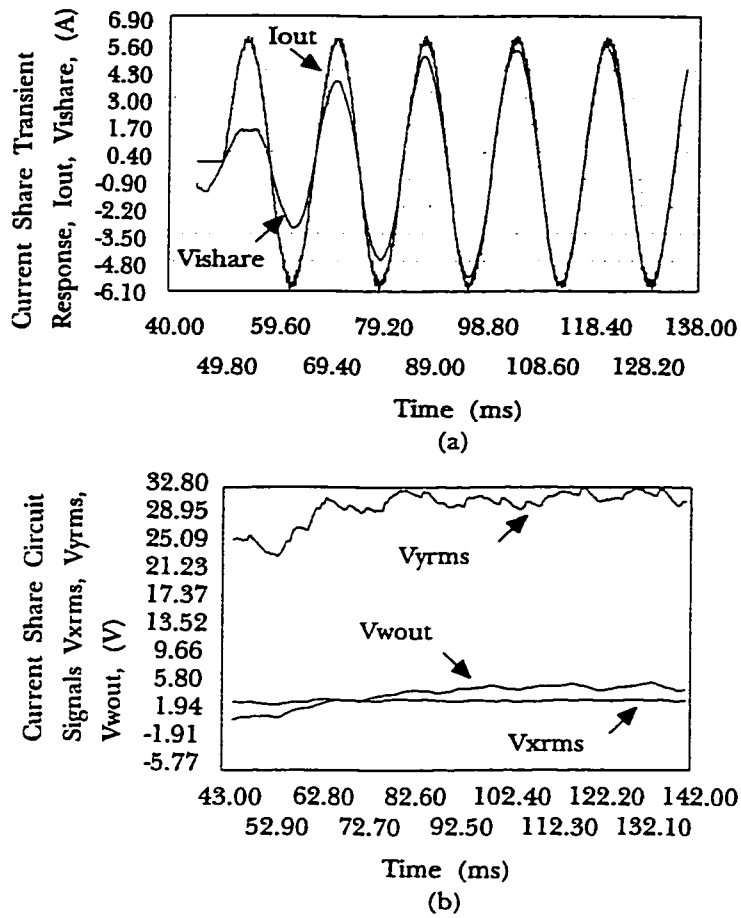


Fig. 5.13. The transient response of the current share controller to a 1.0 pu, 1.0 PF load. (a) The response of the current share reference signal, Vishare. (b) The response of the rms based signals.

action of circuits of Fig. 5.1 and Fig. 5.2. The results obtained in this chapter and for the remaining chapters are to be compared with the industry standards summarized in Table 5.1. For the purposes of this research, the goals for the transient testing are achieved if the output voltage stabilizes in 8.33 ms after switching and the steady-state voltage has a THD less than 5%.

In order to aid in the explanation of the FM scheme, Figs. 5.3 to 5.6 give details of the signals developed in Figs. 5.1 and 5.2. Figures 5.7 and 5.8 show that the current share

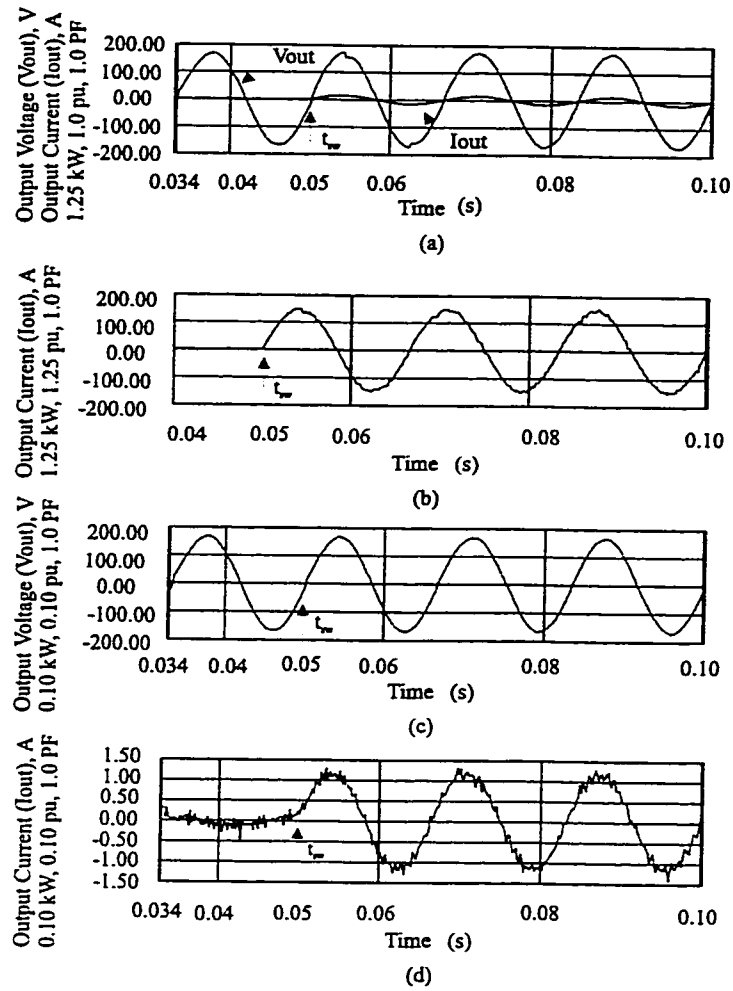


Fig. 5.14. The transient response of a single CM loaded at 50 ms. (a) The output Voltage and current at 1.25 pu and 1.25 kW. (b) Detail of the output current at 1.25 pu. (c) The output voltage at 0.1 pu and 0.1 kW. (d) Detail of the output current at 0.1 pu.

reference signals and the important signals associated with the operation of the power circuit. The steady state output voltage and current waveforms of Figs. 5.11 and 5.12 establish that the proposed CM is capable of meeting the performance objectives of 5% THD despite the presence of the FM signals. Finally, Figs. 5.13 and 5.14 show that the single converter is stable under transient conditions. The computer simulation of the single CM operation provides a useful reference in that it gives some indication of what the circuit performance

and internal waveforms will be before further work begins on the multi-converter system.

6. IMPLEMENTATION AND SYSTEM PERFORMANCE

6.1. The Performance of the System of Converters Connected in Parallel

The performance testing of the system of converters should confirm the results predicted by the theoretical calculations and give additional insight to the operation of the interconnected modules. In particular, the operation of the power subcircuit, the control circuit, the filters, and the frequency modulated communication scheme must be validated with respect to their performance as part of an integrated system. The testing is done using software simulation and an experimental prototype and both transient and steady-state modes of operation are observed. The simulation of a system consisting of two and three CMs is required to show that the controller can maintain the output voltages and currents to the specified values without undesirable interaction between the paralleled units. Finally, experimental results of testing on a laboratory circuit must demonstrate the effectiveness of the current-sharing control strategy.

6.2. The Software Models of the Circuit

The software and the circuit models used for the system of three CMs are the same as those used in Section 5.2. A single CM is a combination of the subcircuits shown in Fig. 5.1 and Fig. 5.2, where each subcircuit is joined to the other through the ac bus, the output current sensor (Iout1,2,3), and the current-share reference connection (Vioshare1,2,3). The

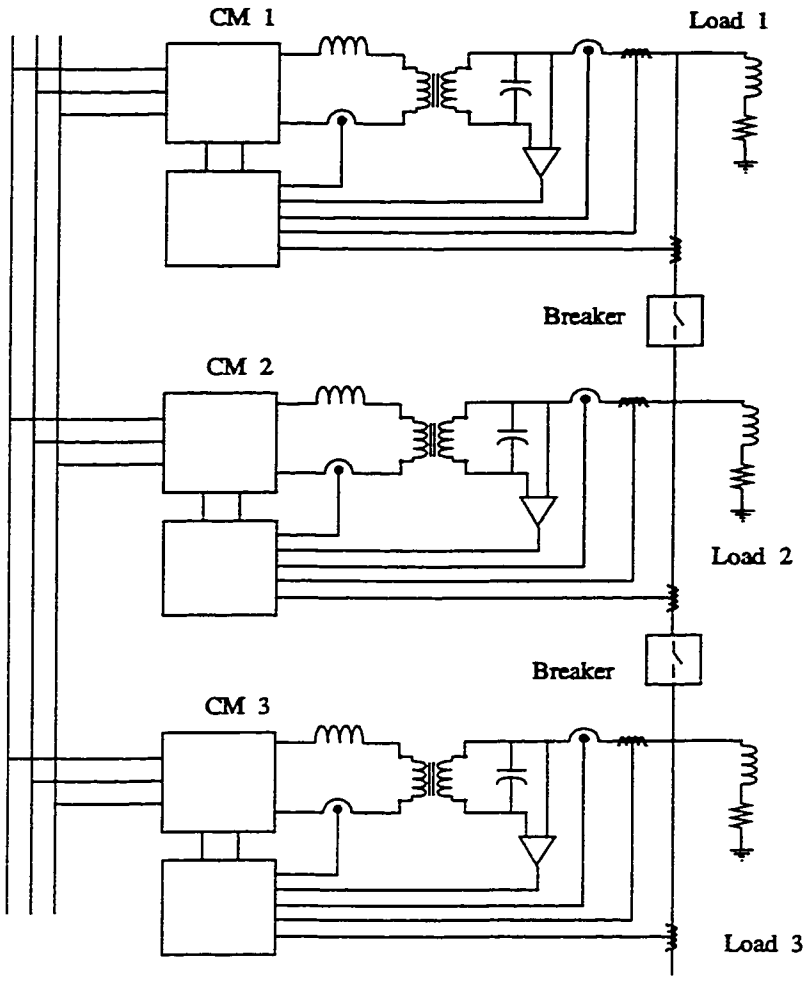


Fig. 6.1. The CM connection scheme for testing the transient response of the system of paralleled converters.

basic CM is repeated and the only connection between the modules is the critical ac bus. The complete system is shown in Fig. 6.1. The THD is measured by the software simulation package using the definition

$$THD = \frac{\sqrt{V_{rms}^2 - V_1^2}}{V_1} \tag{6.1}$$

The variable V_1 is the rms value of the fundamental and Vrms is the total rms value of the

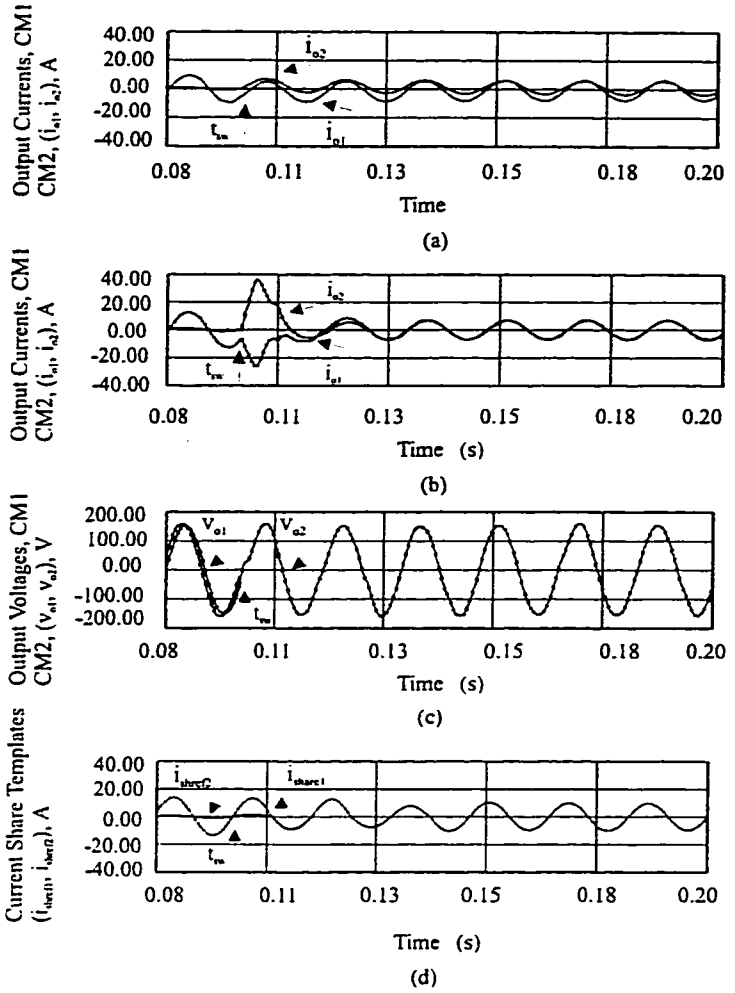


Fig. 6.2. The simulated transient response of a two CM system. (a) The current share reference removed. (b) The current share reference added. (c) The output and bus voltages. (d) The current share reference signals.

voltage or current waveform being measured. Also, the steady-state output waveforms can be investigated for evidence of dc components and subharmonic ripple. The remaining parameters found in Table 5.1, notch-depth and notch-area, can also be evaluated.

6.2.1. The Simulated Transient Response of the Parallel Connected System

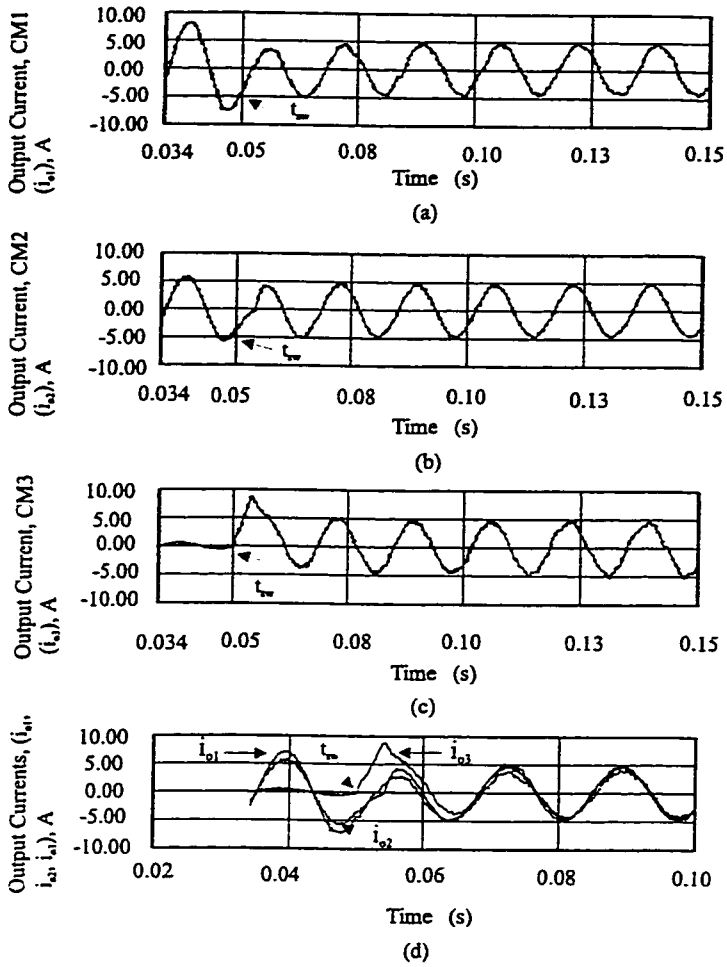


Fig. 6.3. The simulated transient response of a three CM system. (a) Output current of CM1, 1.25 pu, 0.8 PF lagging. (b) Output current of CM2, 1.0 pu, 0.8 PF lagging. (c) Output current of CM3, 0.1 pu, 0.8 PF lagging. (d) The output currents superimposed.

The simulated transient response of the proposed system is demonstrated using a system composed of two and three converters each with an individual reactive load as shown in Fig. 6.1. This system represents a collection of medium power CMs. Each module can deliver 1 kW of power where the per-unit output voltage is 120 Vac rms (169.2 V peak) and the per-unit current is 4.17 A rms (5.88 A peak). The converters act independently supplying

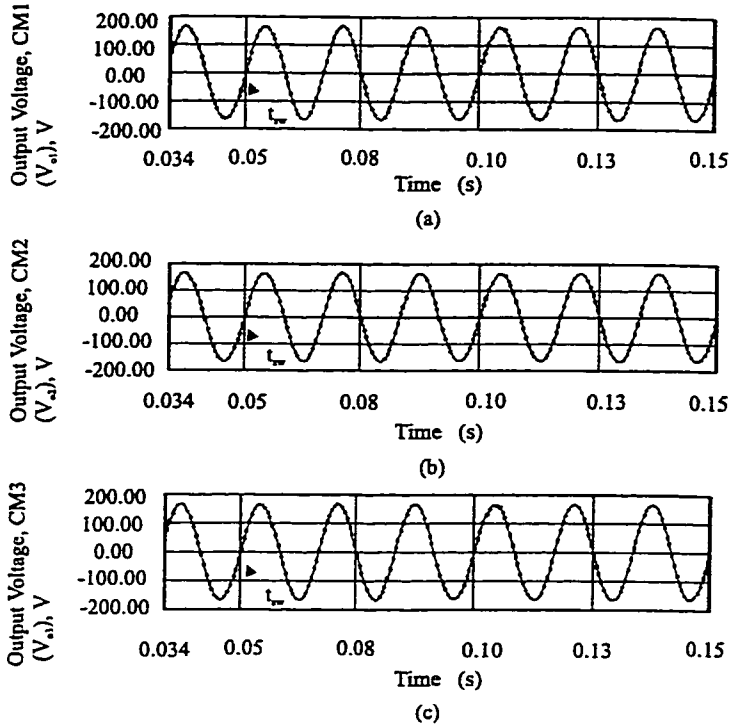


Fig. 6.4. The output voltages of the simulated three converter system. (a) The output voltage of CM1. (b) The output voltage of CM2. (c) The output voltage of CM3.

loads of 0.1, 1.0, and 1.25 pu and 0.8 lagging power factor until the instant when both breakers are closed.

6.2.2. The simulated transient response of a two-CM system

Figure 6.2 shows the simulated transient response of a system consisting of two converters connected to loads of 0.1 pu, 1.0 PF and 1.25 pu, 1.0 PF respectively. Part (a) of Fig. 6.2 shows the response of the system when the current share feedback signal from the control system is removed. At the switching instant, t_{sw} (100 ms), the output currents

associated with CM1 and CM2 ($i_{o1}(t)$, $i_{o2}(t)$) absorb the current imbalance and redistribute it as a dc component that is added to each. After 20 ms the converters are not sharing the total current equally and they are passing a large dc current between them.

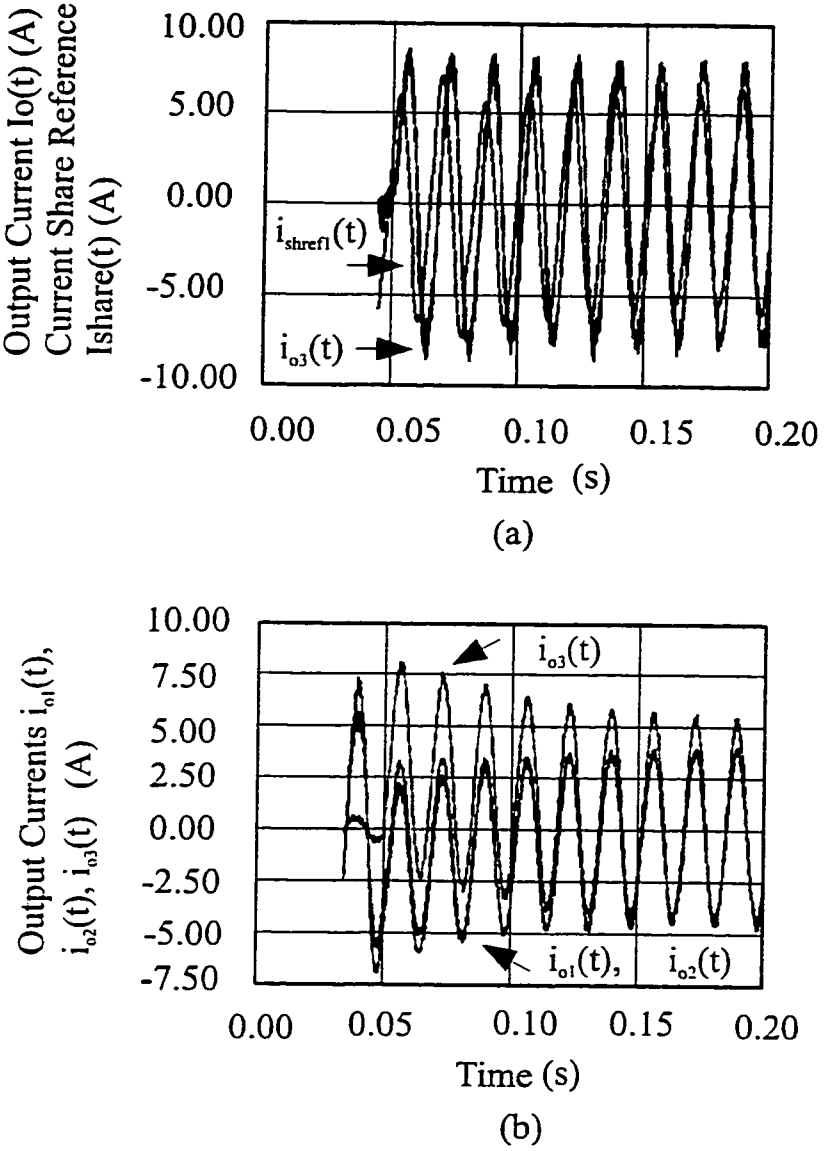


Fig. 6.5. Simulation of the three-converter system. (a) The synchronization time after application of 1.0 pu 0.8 PF load. (b) The effect of the removal of the current share reference signal.

The behavior of the same system with the current-share feedback signal connected has

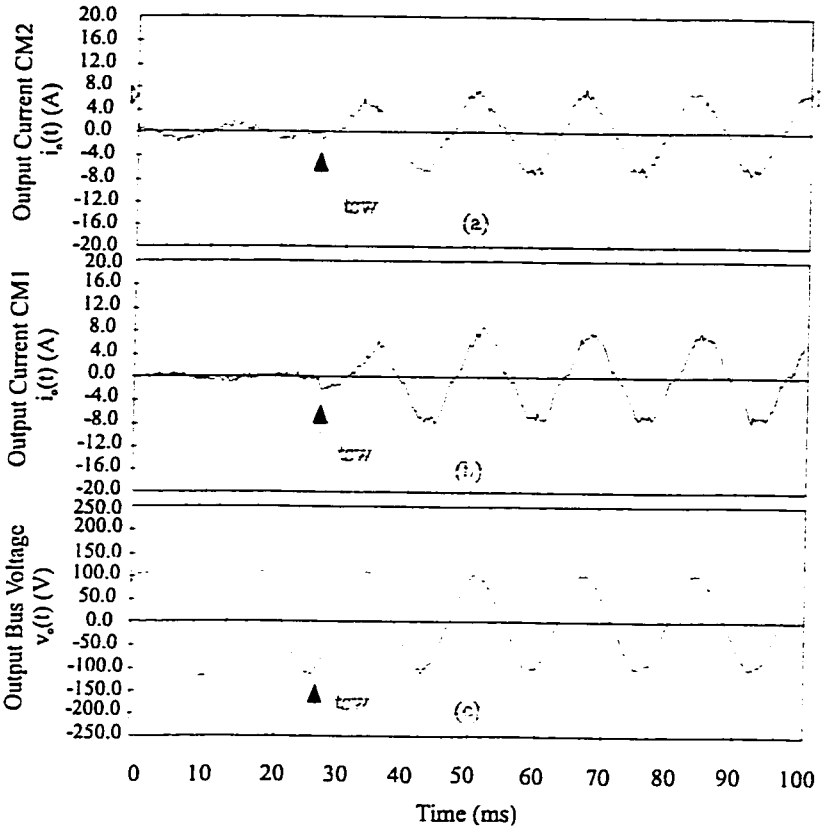


Fig. 6.6. The experimental results from a two converter system. (a) The output current of CM 2. (b) The output current of CM1. (c) The output bus voltage.

two important differences. First, in Fig.6.2 (b), at the switching instant there is now a large transient (3.0 pu) that is eliminated after one cycle (16.67 ms). Second, the currents converge and share after two cycles and there is no longer a dc component. Figure 6.2 (c) shows the output voltages of the respective modules, $v_{o1}(t)$ and $v_{o2}(t)$. The bus voltage shown has a THD of 2 percent and no other distortion. The current reference share signals are shown in Fig. 6.2 (d). The signals converge immediately after the switching instant and stabilize after three cycles.

6.2.3. The transient response of a three converter system

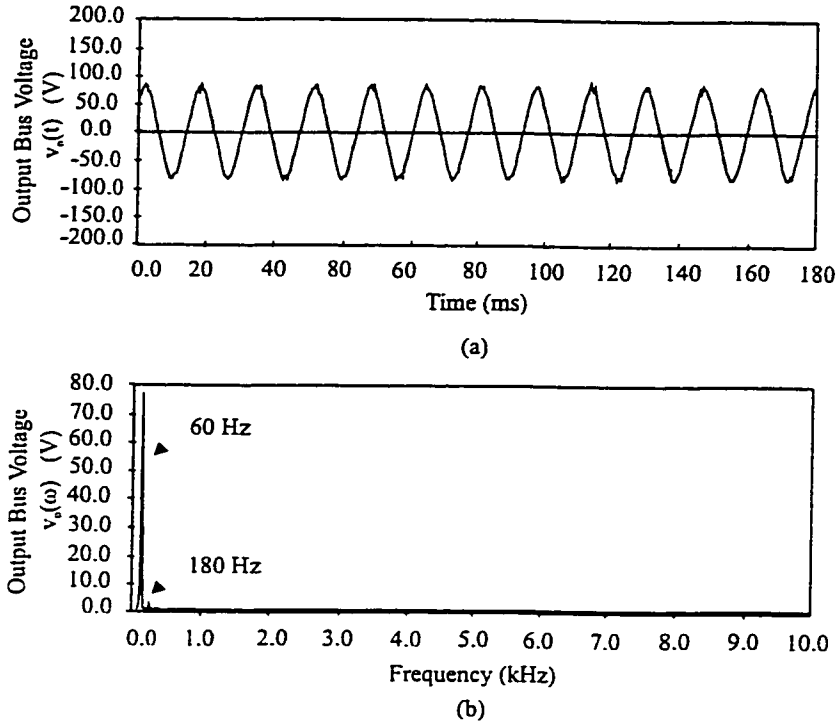


Fig. 6.7. The experimental results from the two converter system. (a) The output bus voltage, $v_{o1}(t)$ and $v_{o2}(t)$ combined. (b) The spectrum of the output bus voltage

The transient response of three converters that are connected to the critical bus at 50 ms is shown in Fig. 6.3 and Fig. 6.4. Initially the converters supply loads of 1.25 pu, 0.8 PF lagging, 1.0 pu, 0.8 PF lagging and 0.1 pu, 0.8 PF lagging. Figures 6.3 (a), (b), and (c) show that the individual converters are able to respond to the changing load in three cycles. Part (d) of Fig. 6.3 shows the three currents superimposed. The three currents are shared after two cycles.

The waveforms shown in Fig. 6.5 demonstrate two phenomena associated with the three-converter circuit. Part (a) shows the time required for the current share reference signal to lock in phase with the output current of a single CM. The combined delay of the FM send and receive circuits is eight cycles (133.36 ms, 8.0 pu). After this time the current reference

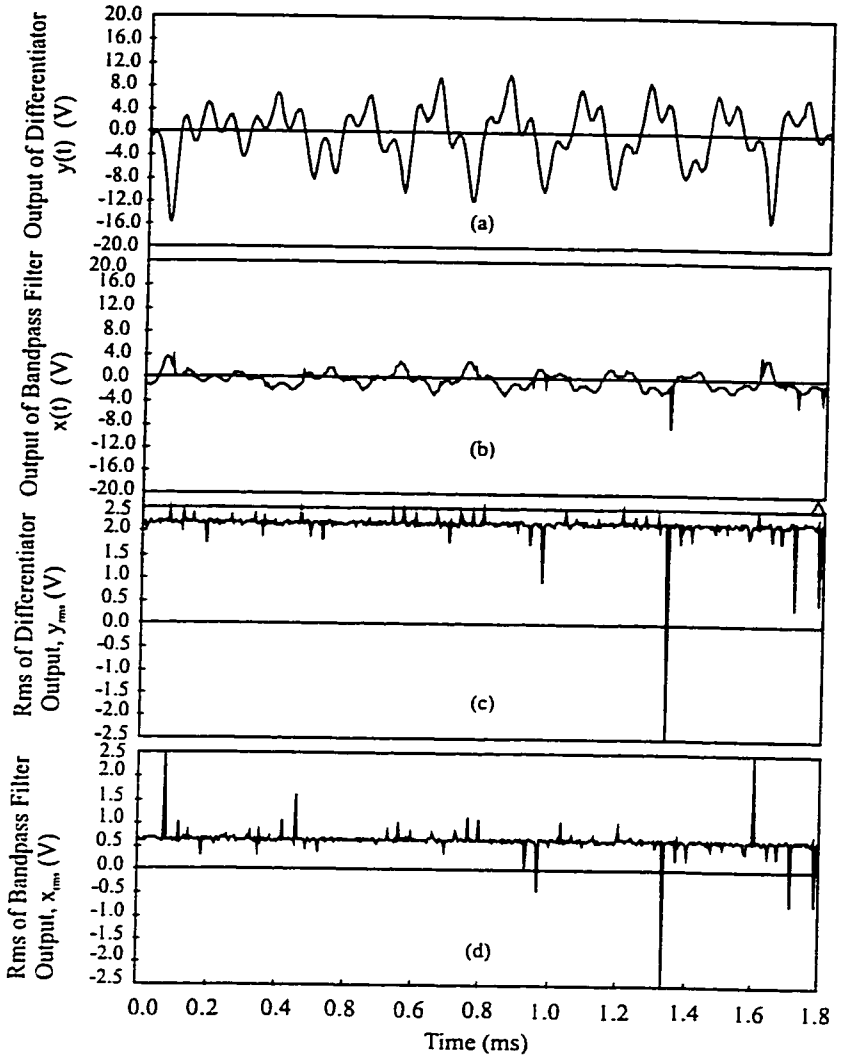


Fig. 6.8. The experimental current-amplitude FM demodulator waveforms. (a) The output of the high-pass filter. (b) The aggregate of the received current-amplitude signals from the bandpass filter. (c) The rms value of (a). The rms value of (b).

including the average load phase angle and the CM output current are synchronized. The effect of the removal of the current sharing template is given in Fig. 6.5 (b). The output current of the converter with the smallest load (0.1 pu, 0.8 PF) before the breaker is closed, shows an initial overshoot and subsequently maintains a dc bias.

6.3. Construction and Performance of the Experimental Test Circuits

A system of two CMs was constructed in order to test the effectiveness of the proposed converter design and current sharing scheme. The test circuit was operated at 60Vac rms, 1 pu voltage, and 4.0 A rms, 1 pu current. The connection of the converters, loads and breakers is described in Section 6.2 and Fig. 6.1. The initial objective of the experimental testing is to show that the CM control circuit and the FM communication scheme are capable of being built and functioning as predicted by the computer simulation. The assignment of the bandwidth for the FM channel and the control of the noise in the converter output waveforms and the FM demodulation subcircuit are two areas that also must be assessed.

In order to accomplish these objectives, the test circuit is limited to two converters each with a single current-share amplitude control subcircuit. Thus, the load is 1.0 PF and the average phase-angle FM control circuit is not used. The switching frequencies used were 10 kHz and 15 kHz.

6.3.1. Construction of the Prototype Circuits

The prototype circuit was constructed according the scheme shown in Fig 5.1 and the upper sections of Fig.5.2 identified as the output-current amplitude FM send and FM receive subcircuits. The interconnection of the converters is as shown in Fig. 6.1 for two modules. The schematic diagrams of the circuits are shown in the Appendix. The realization of the circuit depends on the use of discrete integrated circuit (IC) components available from a number of manufacturers. Thus, the rms-to-dc conversion, multiplication, and division functions are accomplished with single parts (Analog Devices) that are easily installed and

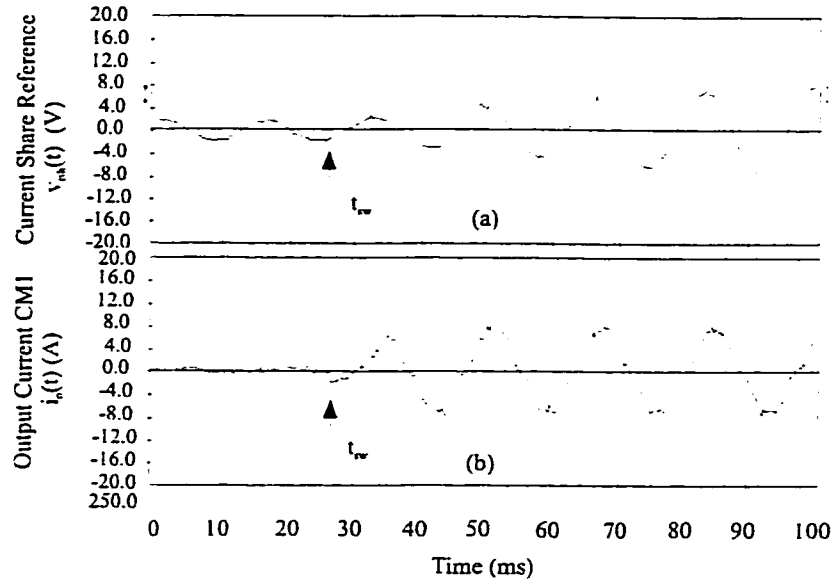


Fig. 6.9. The transient response of the experimental circuit for the transition from 0.1 pu to 1.0 pu load. (a) The current-share reference . (b) The output current of CM1.

perform reliably with minimal design effort.

6.3.2. The Transient Operation of the Prototype System

The response of two converters to the application of a full load, 1.0 pu, from a no-load, 0.1 pu state is shown in Fig. 6.6 (a) and (b). The output currents of the two converters, $i_{o1}(t)$ and $i_{o2}(t)$ converge after one cycle. Fig. 6.6 (c) shows the output bus voltage.

6.3.3. The Steady State Response of the Experimental System

The voltage on the critical bus is shown in Fig. 6.7(a) and the harmonic spectrum is shown in Fig. 6.7 (b). The bus voltage and the spectra show no effects from the presence of the FM control signals. However a third harmonic component is present as a product of the PWM and the output filter.

The performance of the FM communication scheme can be demonstrated by observing

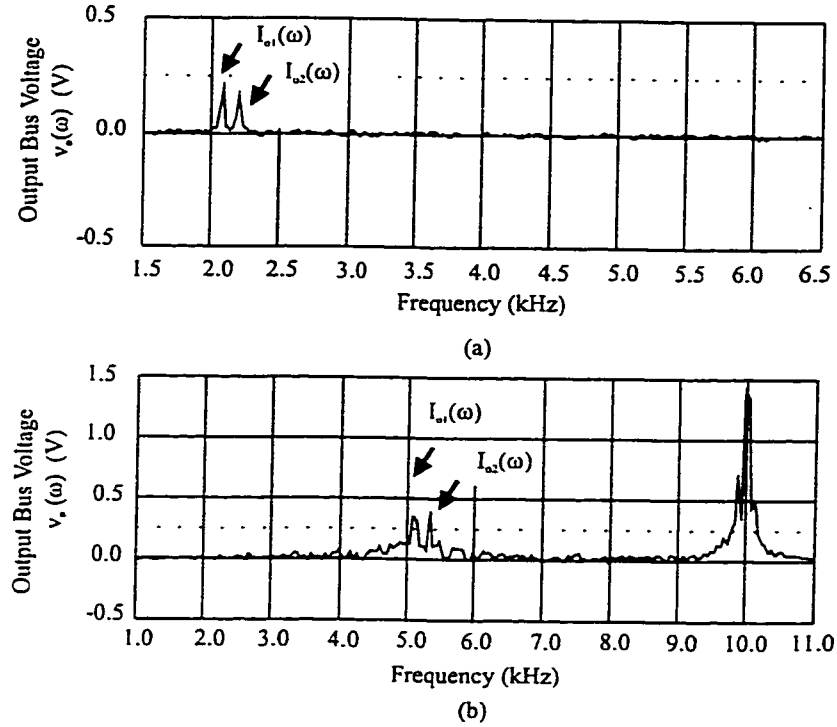


Fig. 6.10. The FM current amplitude signals on the output bus. (a) The output currents at 0.1 pu load. (b) The output currents at 1.0 pu load. Carrier (switching) frequency is at 10 kHz.

the signals x(t), y(t), x_{rms}, and y_{rms}. These control voltages are shown in Fig. 6.8 for 1.0 pu load and 1.0 PF operating conditions. Part (a) shows the filtered signal x(t) that represents the combined FM signals broadcast by the two converters current amplitude VCOs. Part (b) shows the result of passing x(t) through a high-pass filter thus producing the voltage y(t). These two components are then processed by rms-dc converters and the result is shown in Fig. 6.8 (c) and (d). The value of y_{rms} is divided by x_{rms} and the result is scaled to represent the amplitude of the current-share template. The template is then multiplied by a unit reference sinusoid to form the current-share reference signal, $v_{shref}(t)$. Note that these signals correspond to the simulated result of Fig. 5.13 (b). The template waveform is shown in Fig. 6.9 (a) with

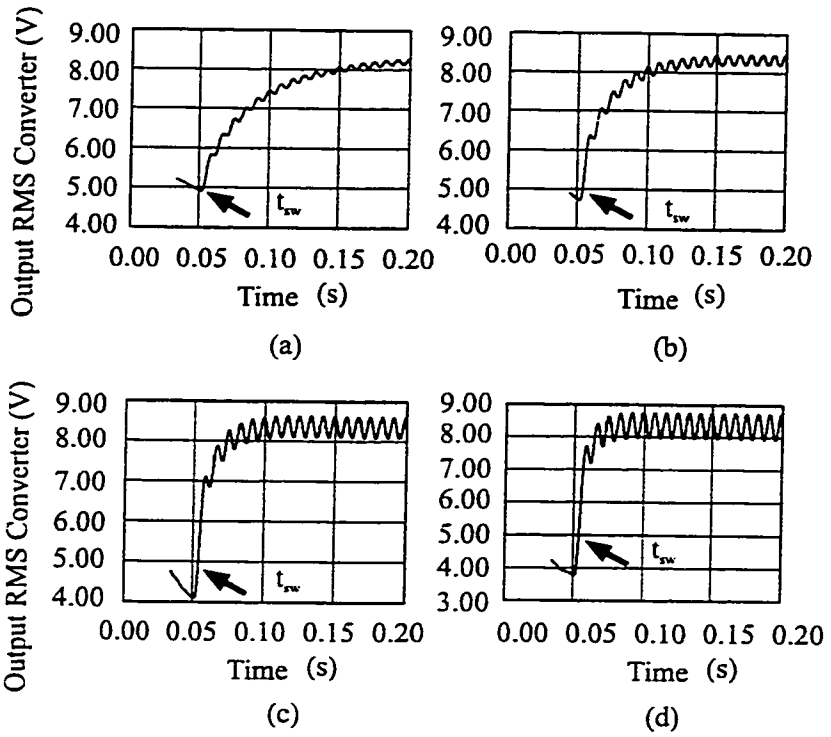


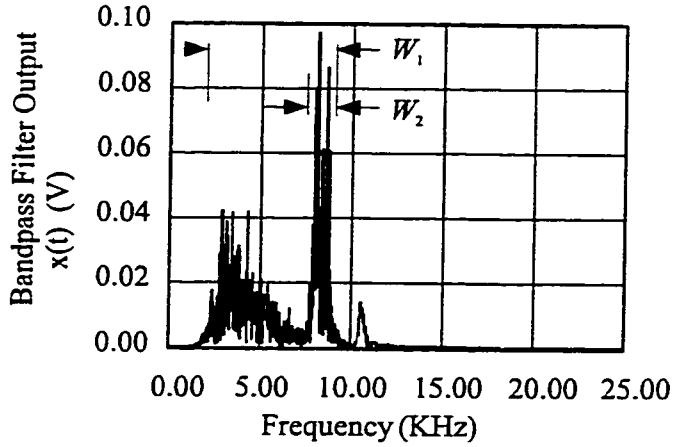
Fig. 6.11. The simulated response characteristics of the rms converters (1 pu = 16.67ms). (a) τ = 1 pu, e = .032 pu, Ts = 9.0 pu. (b) τ = 0.5 pu, e = .05 pu, Ts = 6.0 pu. (c) τ = 0.25 pu, e = .077 pu, Ts = 4.0 pu. (d) τ = 0.167 pu, e = .125 pu, Ts = 2.0 pu.

a corresponding CM output current in Fig. 6.9 (b).

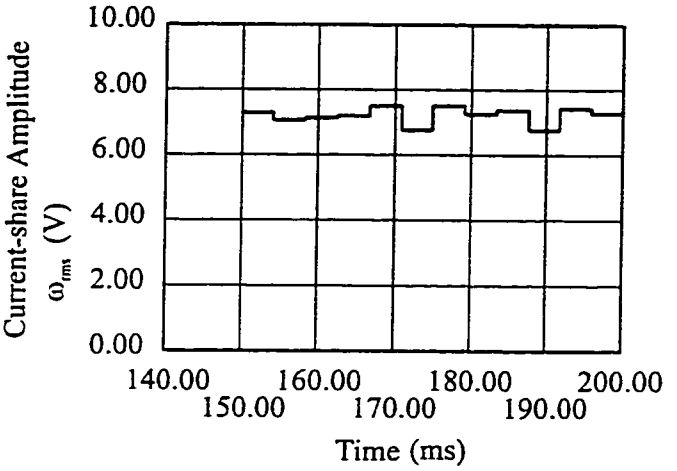
The FM signals representing the frequency coded values of the output currents are shown on Fig. 6.10. Part (a) shows the two converter output currents $i_{o1}(t)$ and $i_{o2}(t)$ represented as 2.1 kHz and 2.25 kHz frequencies respectively for nominal no-load values of 0.1 pu . Figure 6.10 (b) shows the same currents for the 1.0 pu load condition where 4.0 A rms is represented by frequencies of 5.1 kHz and 5.25 kHz.

6.4. Performance and Design Considerations

The design and performance of the proposed system depends on three factors that have



(a)



(b)

Fig. 6.12. The simulated error associated with the rms converter ripple. (a) The bandwidth of the error on the output bus. (b) The cumulative error in the current-share amplitude signal.

an interlocking influence on the circuit response. First, the rms-dc converters introduce an error in the FM scheme as their response time is reduced. Next, the voltage reference must be virtually the same for each CM. Finally, the assignment of the frequency ranges that are assigned to the output filter, the FM signals, and the PWM carrier are hardware (switch and filter) dependent. The choice of components for the realization of the circuit depends on these

factors.

6.4.1. The Effect of the RMS Circuits

The rms converters in each of the FM sending subcircuits can contribute a significant error in the determination of the amplitude and the phase of the current share template. Fig. 6.11 shows how the rms output ripple increases as the response time decreases. Thus Figs. 6.11 (a), (b) , (c), and (d) will transfer errors of .032 pu, .05 pu, .075 pu, and .125 pu respectively to the VCO. As shown in Fig. 6.12 (a) the 0.125 pu error at the VCO is transferred to the output bus as bandwidth W_2 where W_1 is the total operating range, no-load to full-load. The error is finally decoded as ripple in either the amplitude or the phase angle component of the current share reference, Fig. 6.12 (b). In this case, the rms converter response shown in Fig. 6.12 (b) with a six cycle settling time and .05 pu error is chosen as the best performance compromise.

6.4.2. The Effect of Error in the Voltage Reference

The effect of a difference in the voltage references has a twofold effect on the output currents. In a two converter simulation, as the difference increases the amplitudes and the phases of the output currents change. A 1.0 per cent difference will produce an error of 8.6 percent in the current amplitudes and a 17 degree phase shift. A difference of 5 percent in the voltage references will produce 90 degree phase shift and an 85 percent difference in the output currents. Thus, the strategy for implementing the voltage reference must take into account the sensitivity of the control circuit to this parameter.

6.4.3. The Assignment of the Signal Bandwidth on the Output Bus

Since the converter controller and power section are required to share the output bus, some consideration must be given to the placement of the resonance points of the output filter and the carrier frequency. The proposed control strategy uses the ability of the IGBT switch to operate at frequencies above 10 kHz as a means of providing enough bandwidth between the break point of the output filter (500 Hz to 1 kHz) and the noise produced at the switching frequency of 20 kHz in the simulation and the 10 kHz and 15 kHz frequencies used in the prototype. Moreover, the presence of multiple sources of noise implies that the bandpass filters of the FM receiving subcircuits be 3rd order or higher and that notch filter sections may be required to control persistent harmonic components at specific frequencies.

6.5. Summary

Before construction of the prototype of the proposed system, the results of the power section and control circuit design are implemented on a PC based software simulation package. The simulation circuit is composed of three converter modules each supplying an inductive load. The CM sections include a controller that uses an FM communication scheme to enhance the modularity of the overall system by using the output bus to pass the signals that determine the phase and the amplitude of the current-share reference. The results of the simulated performance of a single converter module are shown in Figs. 5.3 to 5.14, while the dual and triple converter systems are shown in Figs. 6.2 to 6.5. In particular, in Fig. 6.3 and Fig. 6.4 the results of the steady-state and the transient tests show that a CM can be put into service that will switch 0.1 pu to 1.25 pu loads over a range of 1.0 PF to 0.8 lagging PF with a one to three

cycle response time and a 1.5 pu overshoot for the current waveforms. The voltage waveforms show a response of less than one-half cycle with no overshoot, no notch effect, and a THD of less than 5% for a switching frequency of 20 kHz.

The experimental results confirm the behavior of the FM communication circuit and the current sharing circuit for a single channel operation (current amplitude) using a system of two converters. The waveforms of Fig. 6.6 show that the loads can be switched from 0.1 pu to 1.0 pu and that the converters will share the load equally. Also, the voltage waveform of Fig. 6.6 and Fig. 6.7 shows that the output voltage is stable through the transient and that the presence of the FM signals on the output bus does not contribute to excessive harmonic distortion.

7. CONCLUSIONS

7.1. Summary

There are three advantages associated with low-to-medium capacity, power-conditioning systems consisting of individual converter modules connected in parallel configurations. Systems such as the one shown in Fig 1.16, can be used to provide sensitive loads with a high quality, reliable source of power through a critical bus. Also, parallel connected converter module arrangements are flexible in terms of expansion and installation and finally, they are easier to maintain. In order to study the fundamental operating characteristics of this type of multi-module circuit, a basic configuration of single-phase half-bridge inverters connected in parallel was proposed and investigated. The objectives of the research were realized by designing a modular system with a minimum of interconnections and a control circuit that uses a direct approach to solving the problem of providing fast response characteristics. Specifically, the supporting research shows that it is possible to construct and operate a system of parallel converters with four features:

1) Each CM is single-phase half-bridge with an output filter and transformer.

2) The switching frequency is 10 kHz to 20 kHz.

3) The control circuit uses two current loops and an outer voltage loop.

4) Current sharing is enforced by a FM based current template.

Further, the modularity of the system is enhanced by using a FM communication scheme in

order to pass the control parameters related to the current-share template between the modules on the critical bus.

In Chapter I the origins and types of the parallel-connected systems are presented and a candidate system is introduced as the subject of this Thesis. The objectives of the design are to produce a CM that has a basic design that can meet the standards of the UPS and power quality industry as well as various regulating bodies (IEEE, IEC). To meet these objectives a circuit model presented in Chapter I has a fast response time (half-cycle or less), (ii) has a modular construction with minimal interconnections between individual units, and (iii) is based on a half-bridge single-phase design. The proposed scheme is shown in Fig. 1.6 and is characterized by the placement of n converters with individual rectifier sections, inverters, output filters, control circuits, and transformers. For the purposes of this work, the converters are asssumed to be identical and they share a common voltage reference. Further, the magnitudes and the phases of the output currents are passed to all the converters simultaneously on the output bus using FM signals (Fig. 3.22). Each converter then decodes the information found on the bus and forms a current-share template that is used to ensure that the individual output currents are balanced.

In Chapter II the design of the power section of the CM is completed and the performance of the rectifier, the inverter, and the filter sections are determined. In Chapter III the control section of the CM is designed and the essential stability of the paralleled system is demonstrated (Fig. 3.18). The performance of the scheme is investigated through computer simulation and experimentation in Chapter IV. The simulated results of the steady-state and transient responses of a single CM and systems of two and three converters show that the

proposed system and control circuit are capable of responding to step load changes from 0.1 pu to 1.25 pu in 0.5 cycles for output voltage and three cycles or less for output current (Fig. 4.17, Fig. 4.18). The same performance was demonstrated experimentally for a 1.0 PF load (Fig. 4.20).

7.2. Feature and Advantages of the Proposed Topology

The proposed parallel configuration of single-phase converters is designed to make use of the modularity, flexibility, and reliability offered by a system of identical modules each sharing a small part of a large load. The proposed circuit has four advantages that make it attractive:

1) The modules are isolated units that can placed anywhere on the output bus.

2) The system capacity can be expanded or reduced by adding or removing units.

3) Converters can be serviced without disturbing the entire system.

4) The inverter and control circuits use basic design strategies.

Since the converters are not directly linked by an isolated control bus, there is less limitation as to their location on the output bus. In this way existing power distribution wiring can be used to create a protected bus and the converters can be conveniently placed for connection to it. The modularity of the proposed system means that CMs can be added or removed easily for maintenance or to change the power level of the system. Finally, the CM, including the control circuit and the power circuit, employs a design that can be expanded to include more sophisticated converter theories and topologies.

The research also shows some limitations which are inherent in the adopted CM design.

There are five areas that place constraints on the application and performance of the proposed system:

1) The switching frequency and current ratings require an IGBT switch.

2) The control circuits are sensitive to variations in the reference voltage.

3) The scheme requires that all converters be identical.

4) The FM communication circuits need additional components.

5) A high switching frequency is necessary.

The enhanced modularity of the candidate circuits depends upon the adoption of the FM approach to implement current-sharing. This in turn means that sufficient bandwidth (10 kHz to 15 kHz) must be available to accommodate the two current related signals, amplitude and phase. Thus, the high switching frequency is required so that it can be placed higher than the FM channels where it will not interfere with the control action of the CMs. To accommodate the need for operation above 10 kHz, the choice of switches is limited at present to the MOS-gated devices, the IGBT and the MOSFET. Finally, the current requirements of the proposed single-phase topology can be best met by using the IGBT switch.

7.2.1 Performance of the Proposed System

Through computer simulation and the performance of a prototype system composed of two CMs, the proposed scheme is validated with respect to eight parameters:

1) The converters successfully use a single-phase half-bridge topology.

2) The switching frequency is in the range of 10 kHz to 20 kHz.

3) The system works for loads of 1.0 PF to 0.8 PF lagging.

4) The system performance is stable for step load changes of 0.1 pu to 1.25 pu.

5) The THD is less than 5%. (The voltage notch is negligible).

6) The step response of the system is half-cycle for output voltage.

7) The step response of the system is three cycles or less for output current.

8) The FM based current-sharing scheme is functional.

The bridge topology chosen uses two switches which means that stresses are increased on each switch. The system is designed, however, for low power applications and switches are available that allow 2.0 pu to 3.0 pu current and voltage overrating. Thus for nominal ranges of 15 A rms and 120 V rms, IGBT devices can be ordered with 60 A rms and 600 V rms specifications. The product of the simulation, Figs 4.16 through 4.19, and the experimental results, Figs 4.20 to 4.24 indicate that the converters and the system are stable for step load changes and that the output voltages and currents meet the transient response requirements of Table 4.1 and IEEE Std 446-1987 (Chapter 4.1.1).

7.2.2. Design of the Proposed System

The design of the candidate system of converter modules including the FM communication sections requires a preliminary plan involving six circuit parameters:

1) The power level of the system must be evaluated.

2) An appropriate converter topology is identified.

3) The PWM switching strategy (Sine PWM, Harmonic Injection) is chosen.

4) The resonant frequencies of the system must be identified.

5) The switching frequency of the converter must be decided.

6) The bandwidth of the FM signals must be assigned.

The bandwidth of the FM signals must be wide enough so that the rms ripple is not a significant part each channel (Chapter 4.5.1). Next, the frequency ranges assigned to the current sharing scheme should be placed between the resonant frequencies of the output filter and the PWM carrier frequency. Finally the design of the filters is done so that the attenuation due to the output LC filter and the transformer is compensated in the bandpass filters of the FM subcircuits.

The FM sending and receiving subcircuits of both the current amplitude and the current phase sections will require bandpass filters that are third order or higher. The additional filtering at the output of the VCO of the sending circuits may be required to prevent unwanted noise from being recycled on the output bus. Also, the bandpass filters of the FM demodulation circuit may not be able to control unforseen system resonances. In, this case the addition of high-q band stop filters should be viewed as a design option. Finally, the method of providing the voltage reference is very important due to the sensitivity of the circuits to this parameter. In this research the voltage reference is assumed to be taken from the utility bus, however, such a signal could also be broadcast as another FM signal on the system output.

7.3. Future Work

The prototype system developed and tested in this Thesis represents a benchmark or baseline that can be used for comparison with more sophisticated and more complex schemes. Since the approach is restricted to a CM that is a single-phase half-bridge inverter supplied by

an ideal dc source , the opportunity exists for further study and improvement in three areas: (i) power quality, (ii) FM modulation, demodulation, and weighting schemes, and (iii) the use of other converter and UPS circuits and topologies.

Moreover, the focus of this Thesis is on the modularity of the paralleled system, the performance of the controller, and the FM current share structure. Thus, issues such as dc bus control and input-power factor have been neglected as well as the application of more advanced control schemes. There are three areas where continued experimental work would extend the results and improve the performance of the prototype circuit:

1) Improve the efficiency and power quality of the system.

2) Improve the FM communication scheme.

3) Extend the basic converter to include UPS circuits.

The power quality improvement can be studied by investigating the effect of advanced PWM switching patterns, the use of alternative control schemes (DQ, droop, digital), and assignments of the bandwidths on the output bus. The signals used for the transfer of the current share template could be encoded as narrow band FM with the center frequency f_o placed in the middle of the BWs now assigned to the current share elements, amplitude and phase. Finally, the proposed scheme should be expanded to include the range of UPS topologies available in the literature as well as three-phase applications. The present work provides the basis for continued research predicated on the advantages of flexibility and reliability offered by the use of paralleled converter circuits.

REFERENCES

1. N. G. Hingorani and Karl E. Stahlkopf, "High Power Electronics," *Scientific American*, vol. 269, no. 5, November, 1993, pp 78 - 85.

2. M. C. Chandorkar, D. M. Divan, Y. Hu, and B. Banerjee, "Novel Architectures and Control for Distributed UPS Systems," *IEEE Ninth Annual Applied Power Electronics Conference and Exposition, APEC '94*, pp 683 - 689.

3. G. T. Heydt, *Electric Power Quality*, Stars in a Circle Publications, West LaFayette, Indiana, 1991, pp. 484 - 497.

4. Kenneth M. Watkins, "The Application of High-Power Inverter Systems," *IEEE Trans. Ind. and Genrl. Appl.*, vol IGA-5, no. 5, pp. 588 - 593, Sept./Aug. 1969.

5. John Reed, and Naresh Sharma, "Large Parallel UPS Systems Utilizing PWM Technology," in *Conf. Proc. IEEE International Telecommunications Energy Conference, INTELEC 1984*, pp. 282 - 289.

6. Clement Fontaine, "On The Paralleling of UPS Systems," in *Conf. Proc. 1986 IEEE International Telecommunications Energy Conference, INTELEC '86*, October 19-22, 1986, Toronto, Canada, pp. 651 - 655.

7. Joachim Holtz, Wolfgang Lotzkat, and Karl-Heinz Werner, "A High-Power Multitransistor-Inverter Uninterruptible Power Supply System," *IEEE Trans. Power. Elec.*, vol. 3, no. 3, July 1988, pp. 278 - 285.

8. Shinzo Tamai and Masahiro Kinoshita, "Parallel Operation of Digital Controlled UPS System," in *Conf. Proc. IEEE 1991 International Conference on Industrial Electronics, Control and Instrumentation, IECON '91*, October 28 - November 1, 1991, Kobe, Japan, pp. 326 - 331.

9. Juan Dixon and Boon T. Ooi, "Series and Parallel Operation of Hysteresis Current-Controlled PWM Rectifiers," *IEEE Trans. Ind. App.*, vol. 25, no. 4, Jul./ Aug. 1989, pp. 644 - 651.

10. M. Honbu, Y. Matsuda, K. Miyazaki, and Y. Jifuku, "Parallel Operation Techniques of GTO Inverter Sets for Large AC Motor Drives," in *Conf. Rec. IEEE Industrial Applications Society Annual Meeting, IAS 1982*, October 4 - 7, 1982, San Francisco, CA, pp. 657 - 662.

11. S. Okuma, K. Iwata, and K. Suzuki, "Parallel Running of GTO PWM Inverters," in *IEEE Power Electronics Specialists Conference, PESC 1984*, pp. 111 - 120.

12. K. Siri and C. Q. Lee, "Current Distribution Control of Converters Connected in Parallel," in *Conf. Rec. 1990 IEEE Industry Applications Society Annual Meeting, IAS 1990*, Seattle, Washington, pp. 1274 - 1280.

13. B. Choi, B. H. Cho, R. B. Ridley and F. C. Lee, "Control Strategy for Multi-Module Parallel Converter Systems," in *21st Annual IEEE Power Electronics Specialists Conference, PESC '90 Record*, pp. 225 - 234.

14. P. Dobrovolny, J. Woods and P. D. Ziogas, "A Phase-Locked-Loop Synchronization Scheme for Parallel Operation of Modular Power Supplies," in *20th Annual IEEE Power Electronics Specialists Conference, PESC '89 Record*, vol. II, pp. 861 - 870.

15. J. Woods, P. D. Ziogas and G. Joos, "Transient Behavior of Converter Modules Connected in Parallel," *16th Annual Conference of IEEE Industrial Electronics Society, IECON '90*, vol. II, pp. 1105 - 1111.

16. Wojciech Tabisz, Milan Jovanovic, and Fred Lee, "Present and Future of Distributed Power Systems," in *Conf. Proc. IEEE 1992 Seventh Annual Applied Power Electronics Conference and Exposition, APEC '92*, February 23-27, 1992, Boston, Massachusetts, pp. 11 - 18.

17. M. C. Chandorkar, D. M. Divan, and R. Adapa, "Control of Parallel Connected Inverters in Standalone ac Supply Systems," *IEEE Trans. Ind. App.*, vol. 29, no. 1, Jan./Feb. 1993, pp. 136 - 143.

18. B. M. Weedy, *Electric Power Systems*, John Wiley and Sons, New York, 1972, pp. 120.

19. A. R. Bergen, *Power Systems Analysis*, Prentice Hall, Inc., Englewood Cliffs, New Jersey, 1986, pp. 265.

20. David J. Perreault, Robert L. Selders, Jr., John G. Kassakian, "Frequency-Based Current-Sharing Techniques for Paralleled Power Converters." in *27th Annual IEEE Power Electronics Specialists Conference*, PESC 1996, Bavino, Italy, June 23-27, 1996, pp. 1073 - 1079.

21. V. Joseph Thottuvelil, George C. Verghese, "Analysis and Control Design of Paralleled DC/DC Converters with Current Sharing," *IEEE Trans. Power Elec.*, vol. 13, no. 4, Jul. 1998, pp. 635-644.

22. Byungcho Choi, "Comparative Study on Paralleling Schemes of Converter Modules for Distributed Power Applications," *IEEE Trans. Ind. Elec.*, vol. 45, no. 2, Apr. 1998, pp. 194 - 199.

23. E. Taylor, *Power System Communications*, George Newnes Limited, London, 1957.

24. Heinrich-Karl Podszeck, *Carrier Communication over Power Lines*, Springer-Verlag, New York, 1972.

25. A. Tuladhar, H. Jin, T. Unger, and K. Mauch, "Parallel Operation of Single Phase Inverters with no Control Interconnections," in *IEEE Applied Power Electronics Conference and Exposition*, APEC'97, vol. 1, pp. 94 - 100.

26.Michael J. Ryan, William E. Brumsickle, and Robert D. Lorenz, "Control Topology Options for Single-Phase UPS Inverters," in *IEEE PEDES Conference Record 1996*, vol. 1, pp 553 - 558.

27. Michael J. Ryan and Robert D. Lorenz, "A Synchronous-Frame Controller for a Single-Phase Sine wave Inverter," in *Conf. Proc. Twelfth Annual Applied Power Electronics Conference and Exposition. APEC'97*, vol. 2, pp. 813 - 819.

28. Naser M. Abdel-Rahmin and John E. Quaicoe, "Analysis and Design of a Multiple Feedback Loop Control Strategy for Single-Phase Voltage-Source UPS Inverters," *IEEE Trans. Power Elec.*, vol. 11, no. 4, Jul. 1996, pp. 532 - 541.

29. Takao Kawabata and Shigenori Higashino, "Parallel Operation of Voltage Source Inverters," *IEEE Trans. Ind. App.*, vol. 24, no. 2, March/April, 1988, pp. 281 - 287.

30. Richard G. Hoft and Myung Youn, "Analysis of Parallel Operation of Inverters," *IEEE Industry Applications Society, IAS Annual Meeting*, 1976, Chicago, Illinois, October 11-14, 1976, pp 951-958.

31. C. S. Mitter, "Introduction to IGBTs," *PCIM Power Conversion and Intelligent Motion*, vol. 21, no.12, December, 1995, pp. 32.

32. David C. Griffith, *Uninterruptible Power Supplies*, Marcel Dekker, Inc., New York, 1989, pp. 403.

33. Mike Boost, "High Performance Medium Power UPS," *PhD Thesis*, Concordia University, Montreal, 1989, pp. 11.

34. *IEEE Recommended Practice for Emergency Standby Power Systems*, IEEE Std 446-1974, The Institute of Electrical and Electronics Engineers, Inc., 1974, pp. 92.

35. Johannes Schaefer, *Rectifier Circuits: Theory and Design*, John Wiley and Sons, New York, 1965.

36. R. W. Lyle, *Power Converter Handbook*, Canadian General Electric Company Ltd., Peterborough, Ontario, Canada, 1976.

37. N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics, Converters, Applications, and Design*, John Wiley and Sons, New York, 1989, pp 109.

38. Wilson E. Kazibwe and Musoke H. Sendaula, *Electric Power Quality Control Techniques*, Van Nostrand Reinhold, New York, 1993.

39. IEEE, *IEEE Recommended Practices and requirements for Harmonic Control in Electrical Power Systems*, IEEE Std 519-1992, The Institute of Electrical and Electronics Engineers, Inc., New York, 1993.

40. International Electrotechnical Commission, *Draft Proposal for Harmonic Mains Current Standard for Information Technology Equipment*, IEC TC 74/WG 9, Geneva, Switzerland, 1994.

41. MicroSim Corporation, *Pspice Circuit Analysis Software*, MicroSim Corporation, Irvine California, 1996.

42. Powersim Technologies Inc., *PSIM Software, Version 2.1*, Powersim Technologies Inc., Vancouver, British Columbia, 1996.

APPENDIX

Fig. A.1. The circuit of the converter module used for the simulation (PSIM).

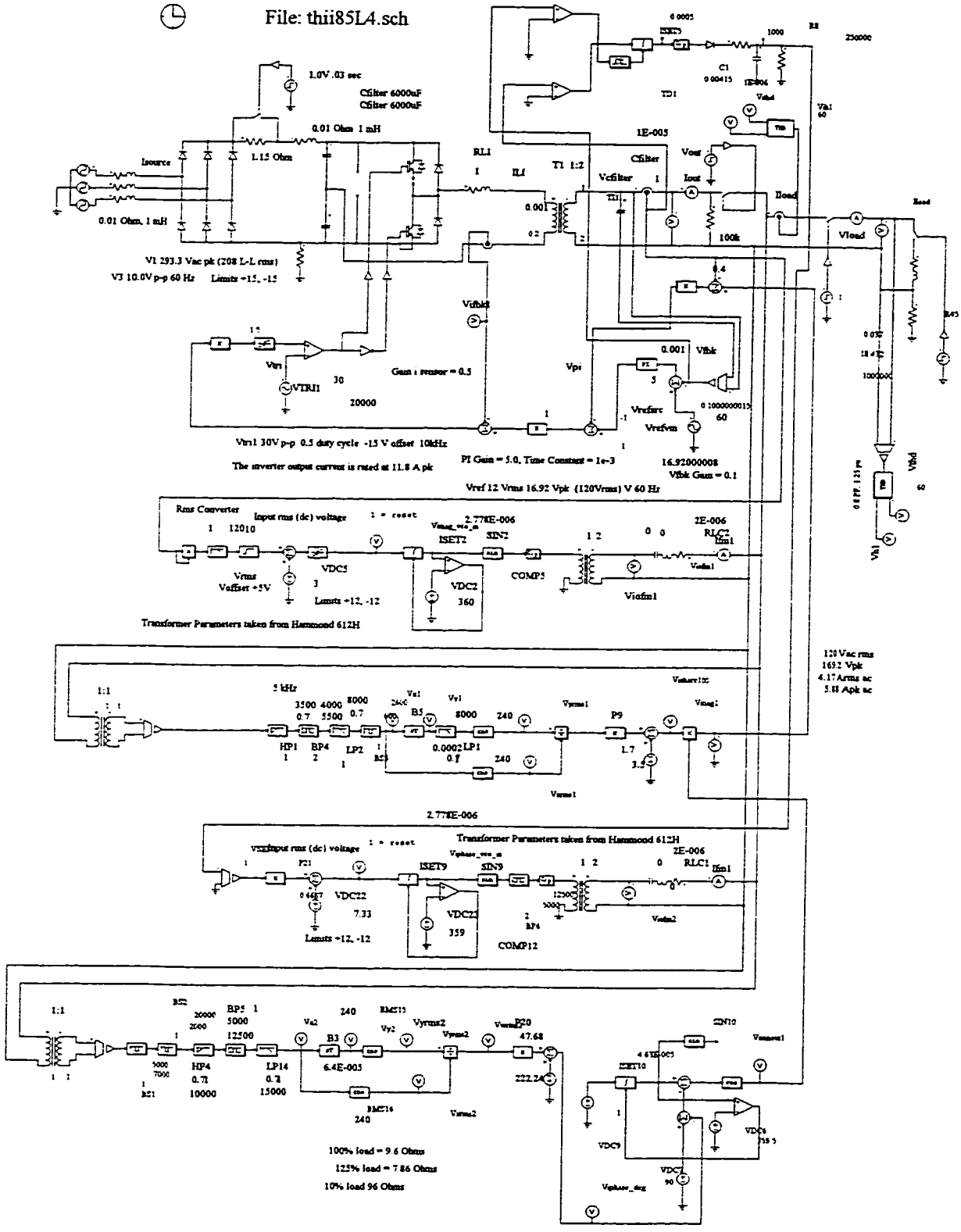


Fig. A.2. The current-share FM conversion subcircuit.

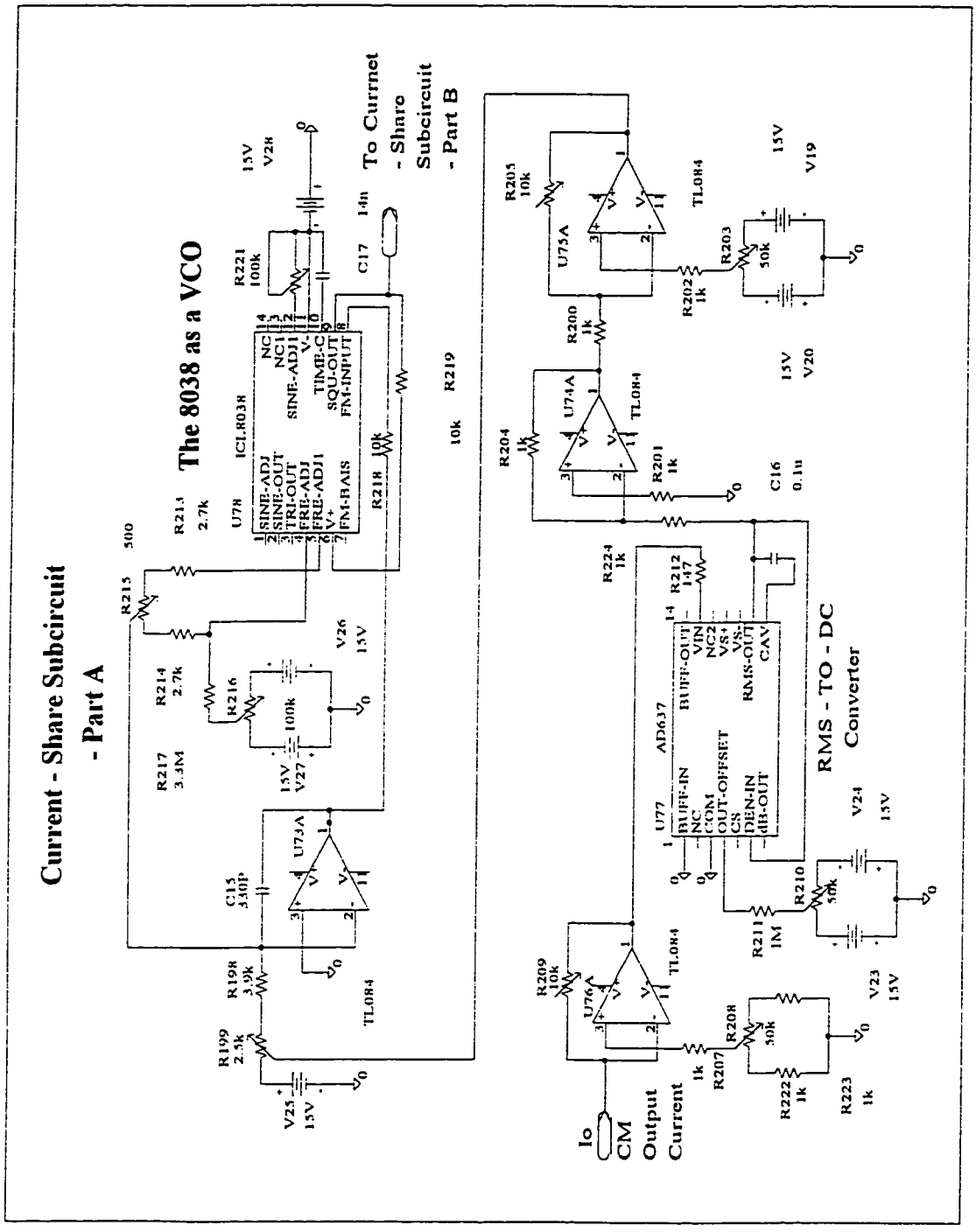


Fig. A.3. The current-share FM signal injection subcircuit.

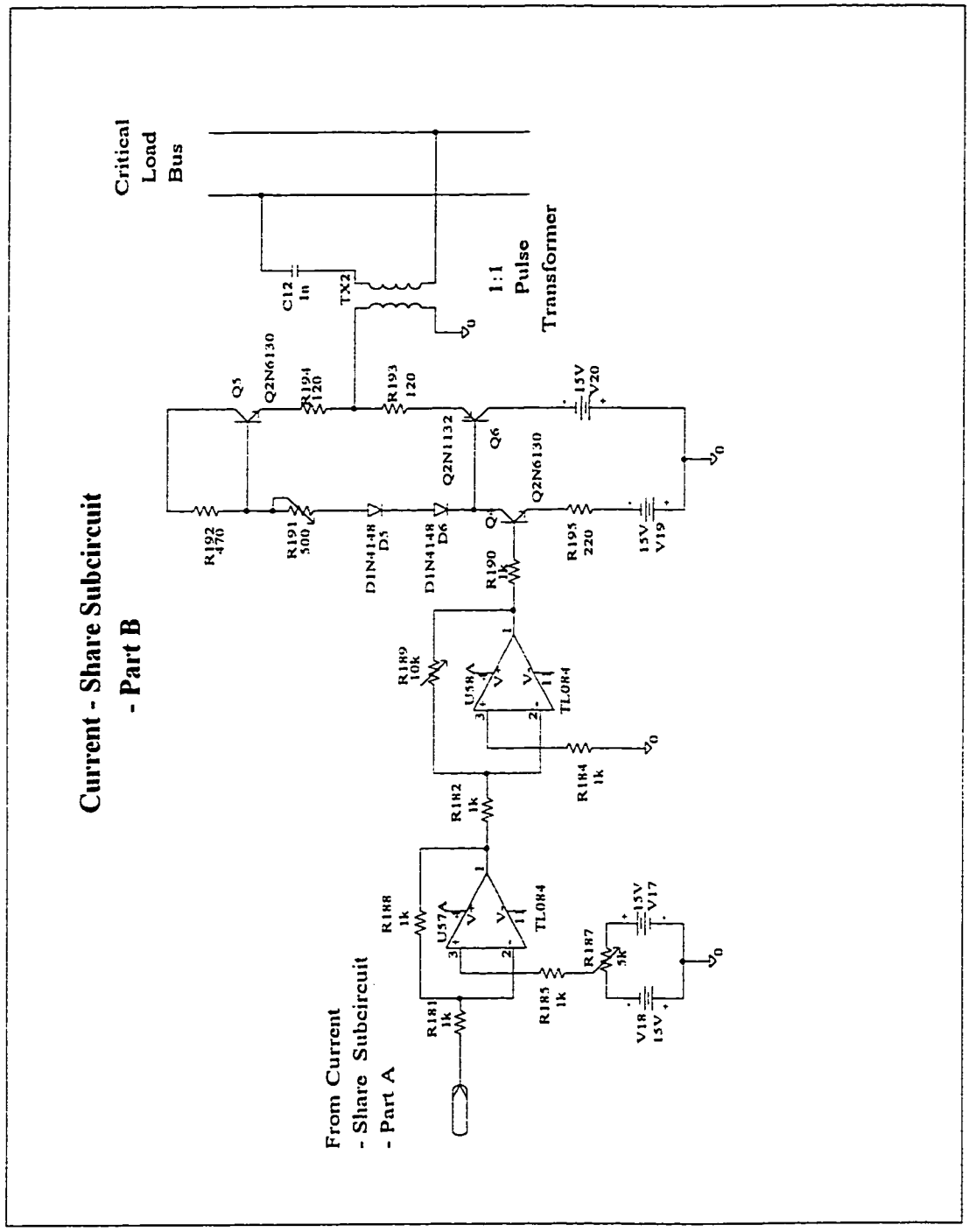


Fig. A.4. The current-share FM detection-subcuit bandpass filter.

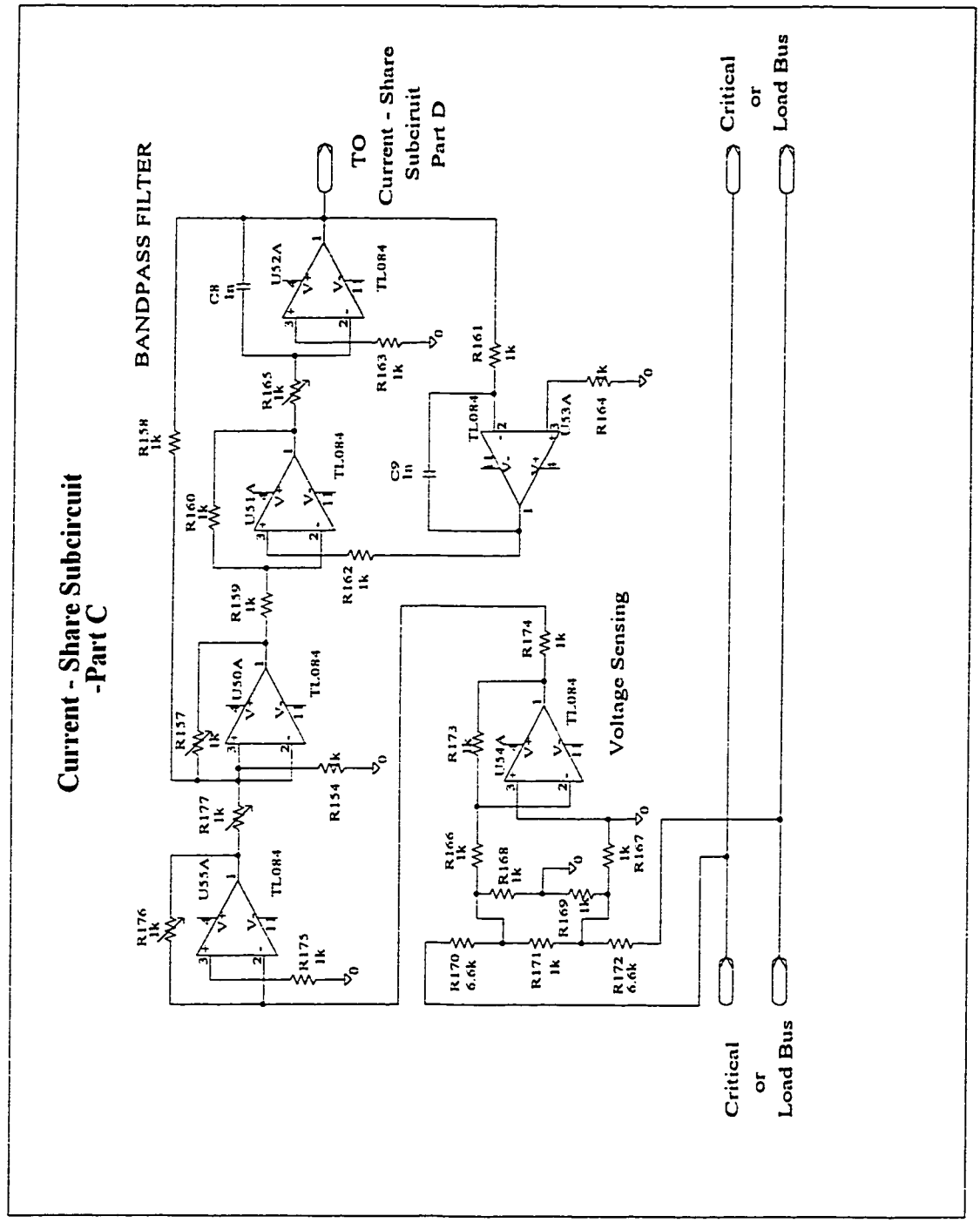


Fig. A.5. The current-share FM detection weighting and division subcircuit.

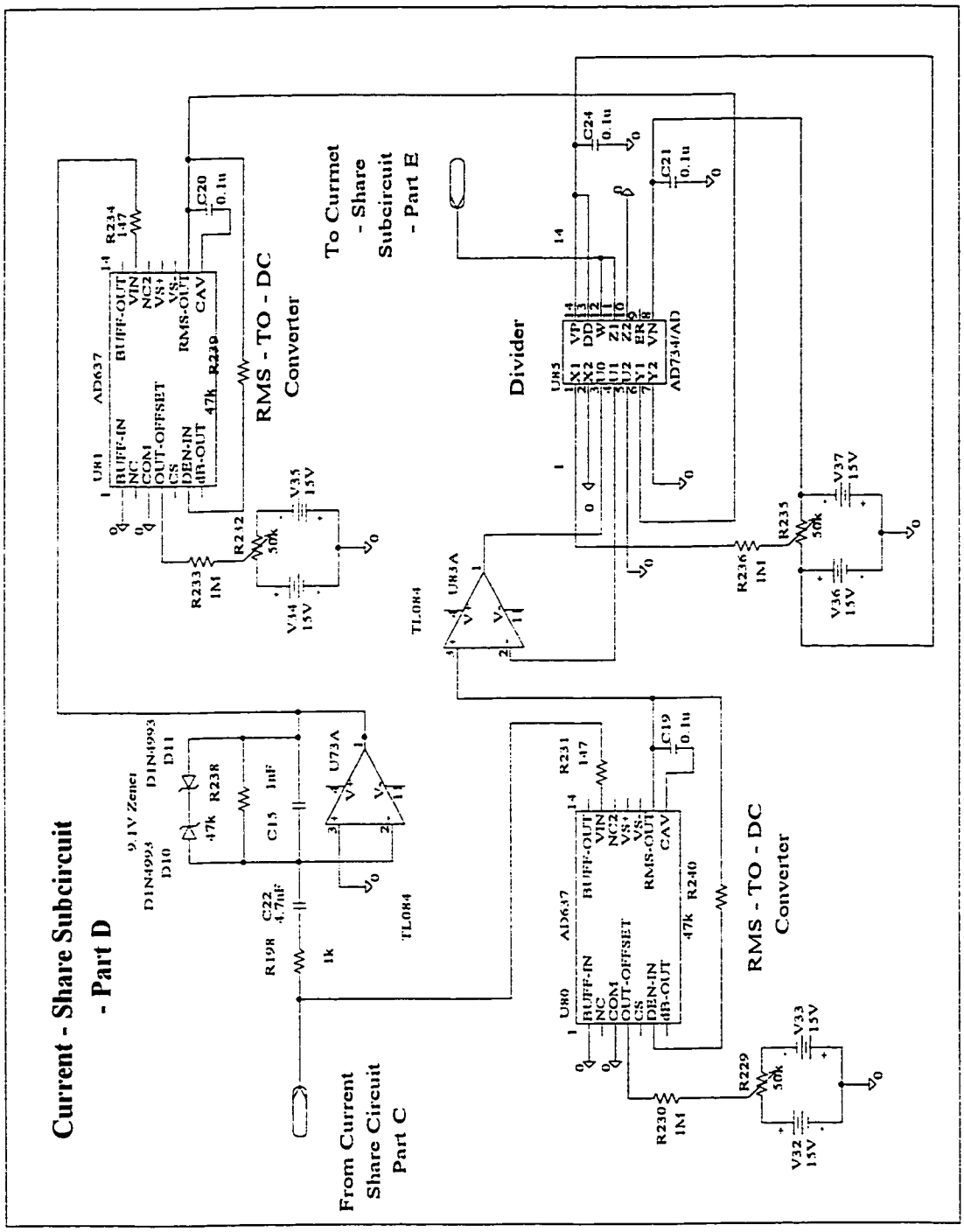


Fig. A.6. The current-share FM synchronization subcircuit.

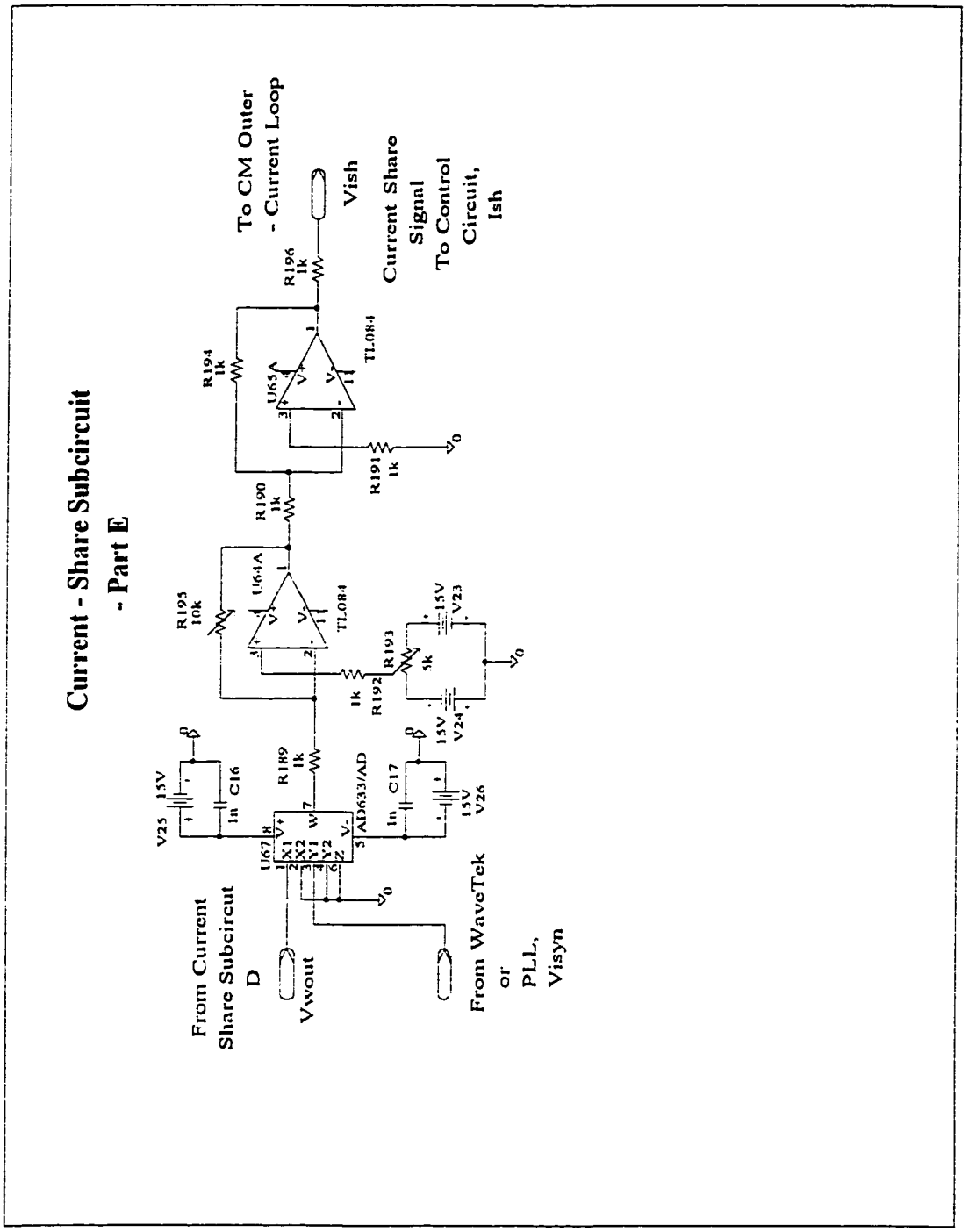


Fig. A.7. The CM voltage control loop.

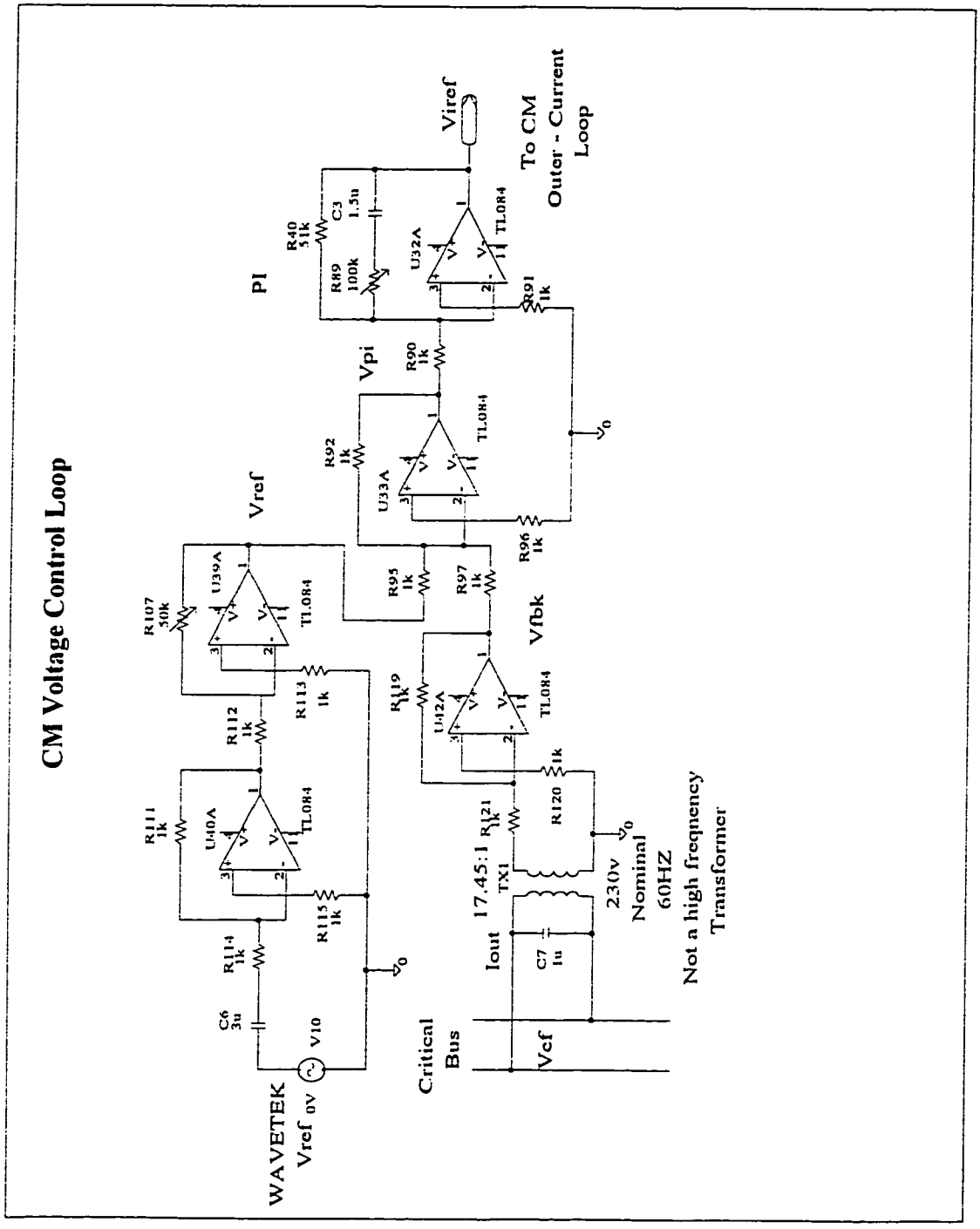


Fig. A.8. The CM outer current loop.

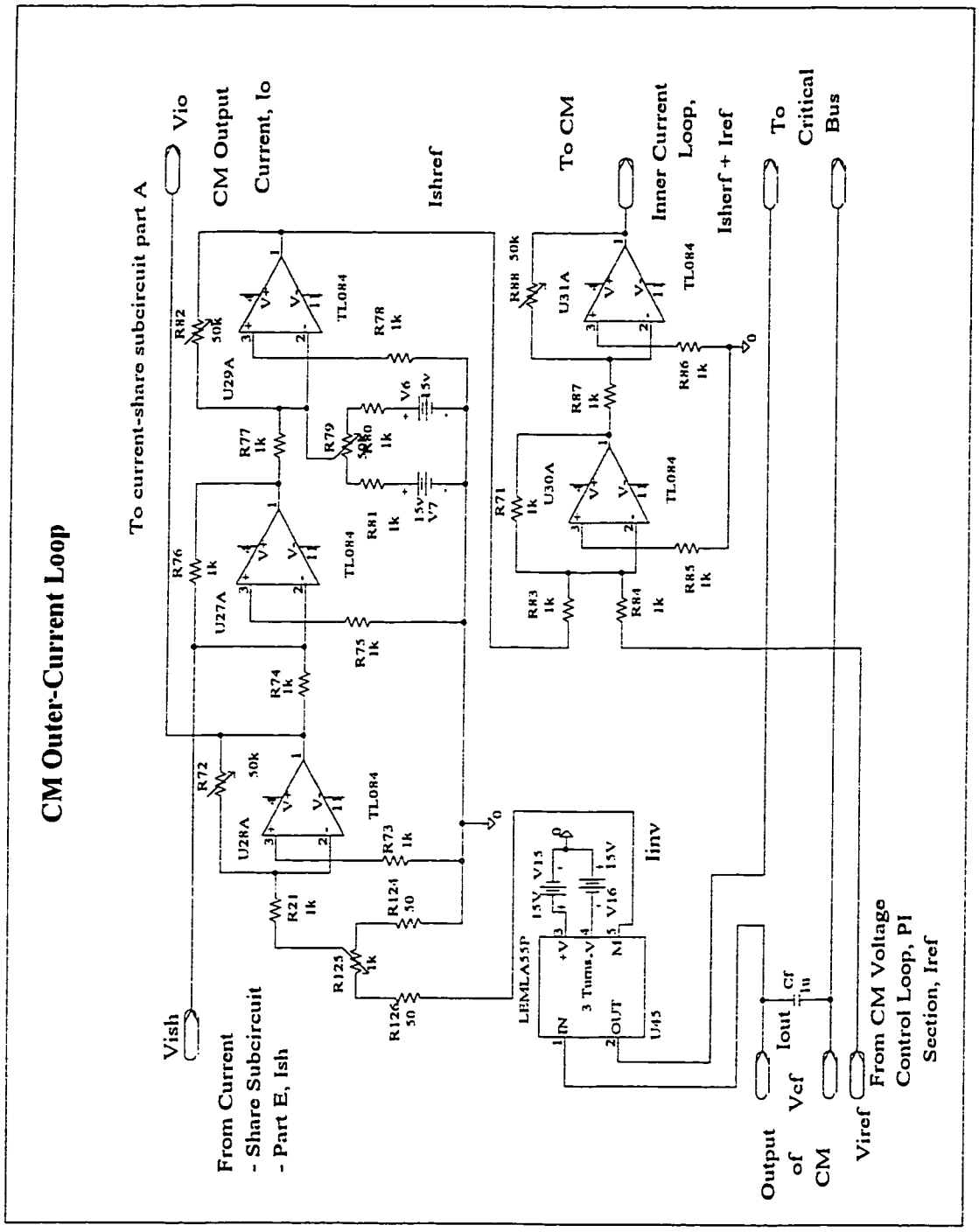


Fig. A.9. The CM inner current loop.

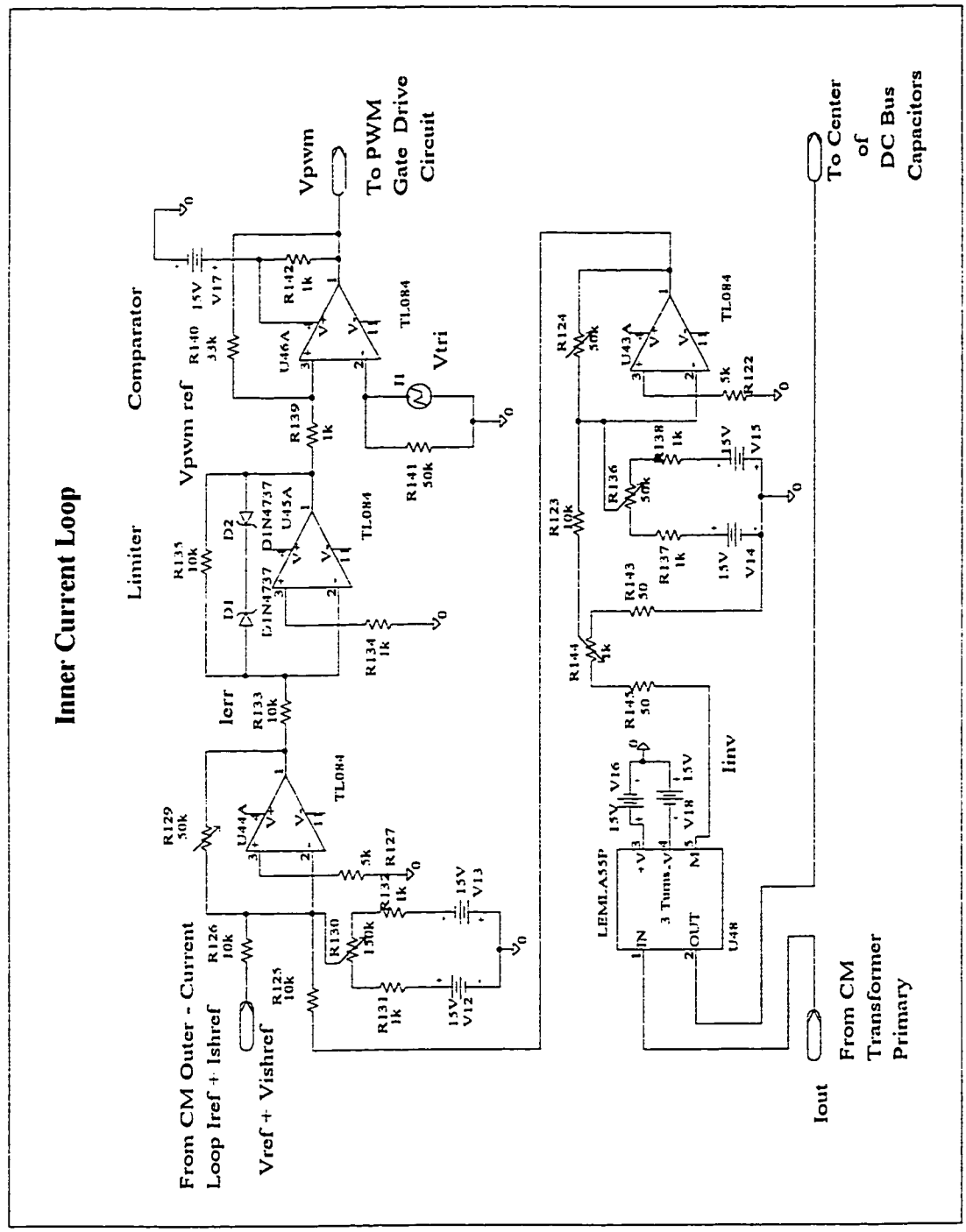


Fig. A.10. The gate-drive circuit.

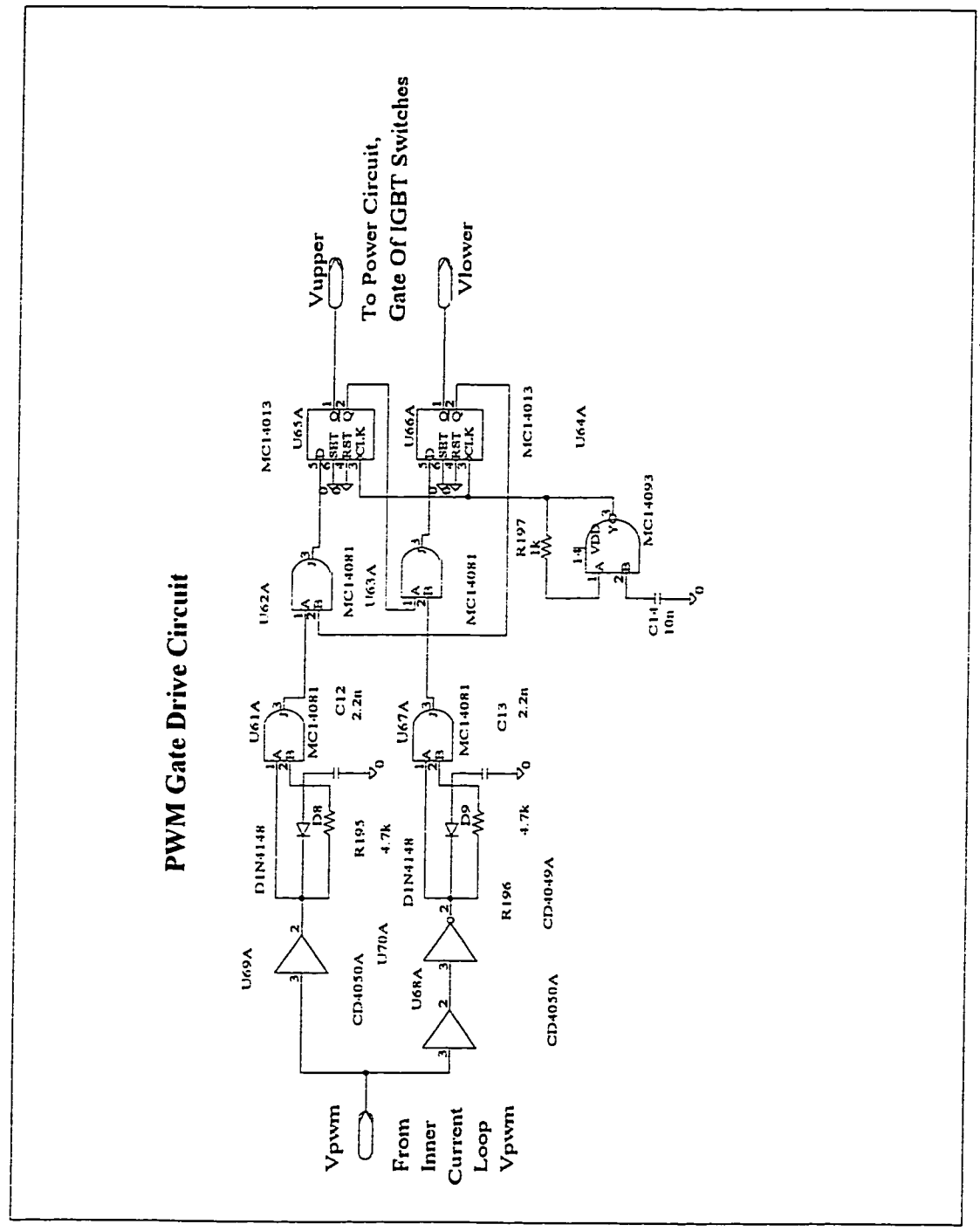


Fig. A.11. The CM power circuit.