# A Feedback Control Technique to Compensate for the Temperature Dependence of the Transconductance of CMOS Transistors and Its Application in $g_m$-C Filters

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# Abstract

## A Feedback Control Technique to Compensate for the Temperature Dependence of the Transconductance of CMOS Transistors and Its Application in $g_m$-C Filters

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Transconductance-C ($g_m$-C) filters are suitable solutions to perform a variety of signal processing tasks. Operational Transconductance Amplifiers (OTAs) are main components of $g_m$-C filters, and variable transconductance gain ($g_m$) has a detrimental effect on the performance of $g_m$-C filters. One principal factor to cause such variations of the transconductance ($g_m$) values is the change in environment temperature. In this thesis, a new negative feedback technique is applied to stabilize changes in the transconductance of CMOS OTA with temperature variation over the industrial temperature range of –30°C to +85°C. Stabilized transconductance will bring stability in the frequency and quality factor of the filters built from these OTAs. To validate this notion, several types of second-order $g_m$-C filters have been built with the temperature stabilized OTAs. Furthermore, a second-order $g_m$-C band-pass filter with the negative feedback control system has been implemented using TSMC 0.18 μm CMOS technology, and fabricated through the facilities of Canadian Microelectronics Corporation (CMC). The experimental results show good agreement with the theoretical expectation.

# Acknowledgements

I would like to express my sincere gratitude to my thesis supervisor, Dr. R. Raut, for his insightful guidance, valuable advice and continued assistance throughout the course of this work. His great generosity and kindness provided me with ample freedom to pursue my academic goal.

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Finally, I want to thank my beloved husband and daughter who really give me the perspective I need the most for my future.

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# List of Symbols and Abbreviations

| | |
|---|---|
| APF | All-pass Filter |
| BPF | Band-pass Filter |
| BW | Bandwidth |
| C | Capacitor |
| CMOS | Complementary Metal Oxide Semiconductor |
| CTM | Capacitor Top Metal |
| dB | Decibel |
| DIP | Dual In-line Package |
| DAC | Digital Analog Converter |
| HPF | High-pass Filter |
| HPN | High-pass Notch |
| H(s) | Transfer Function |
| I | Current |
| IC | Integrated Circuit |
| L | Channel Length of a MOS Transistor |
| LPF | Low-pass Filter |
| LPN | Low-pass Notch |
| MOS | Metal Oxide Semiconductor |

MOSFET Metal Oxide Semiconductor Field Effect Transistor

OTA Operational Transconductance Amplifier

OP-AMP Operational Amplifier

Q Quality Factor

R Resistor

S/H Sample-and-Hold

T Temperature

V Voltage

VDD Positive Supply Voltage

VSS Negative Supply Voltage

$V_{th}$ Threshold Voltage of a MOS Transistor

VLSI Very Large Scale Integration

VCO Voltage-Controlled Oscillator

W Channel Width of a MOS Transistor

$\mu$ Mobility of Carrier

$\omega$ Frequency in Radians

$g_m$ Transconductance

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# Chapter 1

# Introduction and Motivation

Analog filters are essential in many different systems. Even signal-processing systems that appear to be entirely digital often contain one or more analog continuous-time filters internally or as interface with the analog world [1]. With the arrival of VLSI, a filter built with discrete components will be unacceptably bulky when compared to the remaining parts of a system that are being increasingly implemented in fully integrated form. Also, counting hand assembly, manual tuning, and wire interconnection, a discrete design may be too expensive or unreliable. Therefore, considerable effort is being devoted to design of filter circuits that consist only of components that are conveniently realizable on an integrated circuit chip.

There are two main techniques for realizing integrated analog filters. One

technique is the use of switched-capacitor circuits. A switched capacitor circuit, although its signal remains continuous in voltage (i.e., it is never quantized), is, in fact, a discrete-time filter since it requires sampling in the time domain. Because of this time-domain sampling, the clock rate must always be at least twice the highest frequency being processed to eliminate aliasing. In fact, typically the clock rate is much greater than twice the signal bandwidth, to reduce the requirements of an anti-aliasing filter. As a result, switched-capacitor filters are employed to process low frequency signals. Presently, the second most popular technique for realizing integrated analog filters is continuous-time filters. As their name suggests, continuous-time filters have signals that remain continuous in time and that have analog signal levels. Since no sampling is required, continuous-time filters have a significant speed advantage over their switched-capacitor counterparts [2].

Integrated continuous-time filters are suitable solutions to perform a variety of signal processing tasks. Two main approaches to design such filters that are fully compatible with current CMOS technologies are MOSFET-C active filters and transconductance-C ($g_m$-C) filters. MOSFET-C active filters are similar to fully differential active RC filters, except that the resistors are replaced with equivalent MOS transistors operating in triode region. Because all active filters include one or more operational amplifiers that generally limit the frequency range of filters, MOSFET-C active filters are often applied to low to intermediate frequency range.

Transconductance-C ($g_m$-C) filters don't contain operational amplifiers and obtain the required gain from transconductance amplifiers. These filters consist only of transconductance amplifiers and capacitors and are referred to as the transconductance-C ($g_m$-C) filters. $g_m$-C filters are particularly advantageous at high frequencies because it is easier to design a transconductor capable of driving a capacitor at high frequencies than to design the high frequency amplifier required by other methods.

The critical problem in the design of integrated $g_m$-C filters is their need for some sort of tuning circuitries because the filter coefficients are determined by the ratio of two dissimilar elements, such as capacitance and transconductance values. If no tuning is performed, one might expect large deviation of the absolute value for the $g_m/C$ ratio due to process variations and operating conditions (i.e., environment temperature). To guarantee accurate performance, automatic tuning is very desirable in an integrated $g_m$-C filter.

## 1.1 Common Automatic Tuning Methods

A variety of approaches based on phase-locked loops [2][3][4][5], adaptive signal processing [6], magnitude-locked loops [1], and envelop detection [7][8] techniques have been proposed and used for automatic tuning in $g_m$-C filters. A brief review of these techniques is presented below.

### 1.1.1 Phase-locked Loop Technique

The general scheme of a standard phase-locked loop technique is shown in Figure 1-1. The operation proceeds as follows. The phase detector, which is an analog multiplier, compares the external reference clock with the output of the VCO. The VCO is realized

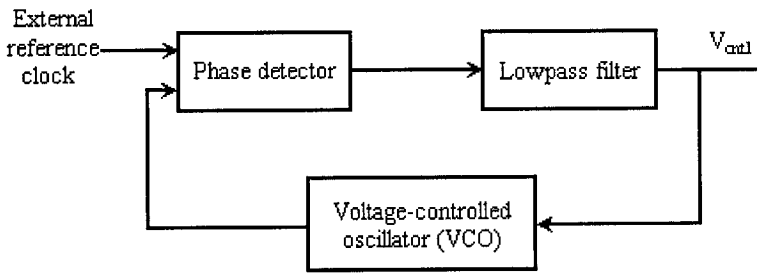


Figure 1-1: Phase-locked loop frequency tuning scheme

by using operational transconductance amplifier (OTA) based integrators that are tuned to adjust the VCO's frequency. The output of the phase detector produces a raw error signal, which is low-pass filtered to eliminate all undesirable high-frequency components. The cleaned error signal is applied to the VCO frequency control terminal. Once the VCO output is locked to the external reference signal, the $g_m/C$ ratio of the VCO is set to a desired value, and the control voltage, $V_{cntl}$, can be used to tune the integrated filter. It should be noted that choosing the external reference clock involves a trade-off because it affects both the tuning accuracy as well as the tuning signal leakage into the main filter. It is best to choose the reference frequency that is equal to the filter's upper passband edge. However, noise gains for the main filter are typically the largest at the filter's upper

passband edge, and therefore the reference-signal leak into the main filter's output might be too severe. As one moves away from the upper passband edge, the matching will be poorer. Another problem with this approach is that, unless some kind of power-supply-insensitive voltage control is added to the VCO, any power-supply noise will inject jitter into the control signal, $V_{cntl}$. If the additional amplitude control is needed for this case, it is quite complex.

### 1.1.2 Adaptive Signal Processing Technique

The adaptive signal processing technique [6] attempts to tune a continuous-time integrated filter by adjusting all the poles and zeros of the tunable filters. The system diagram is shown in Figure 1-2. During tuning, the input to the tunable filter is a

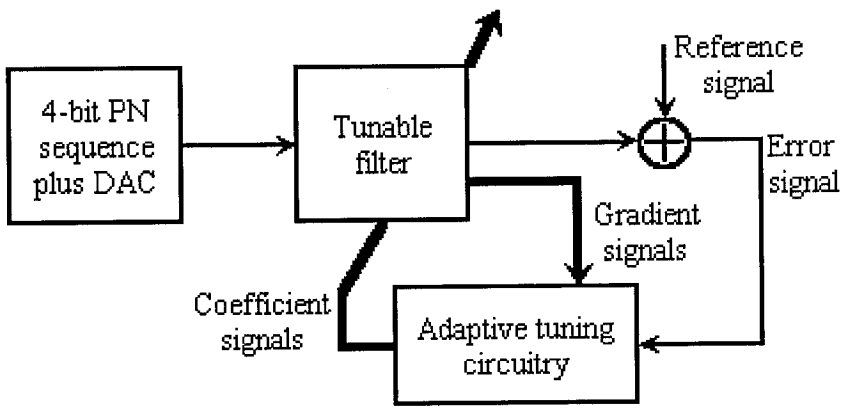


Figure 1-2: Adaptive signal processing technique tuning scheme

predetermined output from a pseudorandom(PN) 4-bit sequence and a D/A converter. Since the input is known and repetitive, the ideal output from a desired transfer function can be precalculated (or simulated) and used as a reference signal for the adaptive system. Then, the output of the tunable filter is compared with the reference signal to get the error signal, while the adaptive tuning circuitry minimizes this error signal. After adaptation, the transfer function of the tunable filter should match that of the desired filter, and, by freezing the coefficients (assuming they are digitally controlled), the tunable filter can be disconnected from the tuning circuit and used for the desired operation. With this approach, it is possible to tune all the poles and zeros of the tunable filters to better match the desired transfer function. Although the adaptive tuning circuitry simply consists of comparators, analog multiplexers, and integrators, this adaptive tuning scheme has not yet been fully integrated or experimentally verified in a high-frequency application.

### 1.1.3 Magnitude-locked Loop Technique

The magnitude-locked loop technique relies on peak detection. For $g_m$-C filters, the main problem is to realize accurately the time constant $C_U/g_m$ where $C_U$ is a unit capacitor. The magnitude-locked loop technique tunes this time constant by varying $g_m$. The circuit is shown in Figure 1-3. The two components, an OTA of value $g_m$ loaded by a capacitor $C_U$, form an integrator. Assuming a reference voltage $v_1(t) = V_1 \sin \omega_{ref} t$, where

$\omega_{ref}$ = $g_m/C_U$, is applied to the integrator, the output of the integrator shall be:

$$v_2(t) = -V_1 \frac{g_m}{\omega_{ref} C_U} \cos \omega_{ref} t = -V_2 \cos \omega_{ref} t \qquad (1\text{-}1)$$

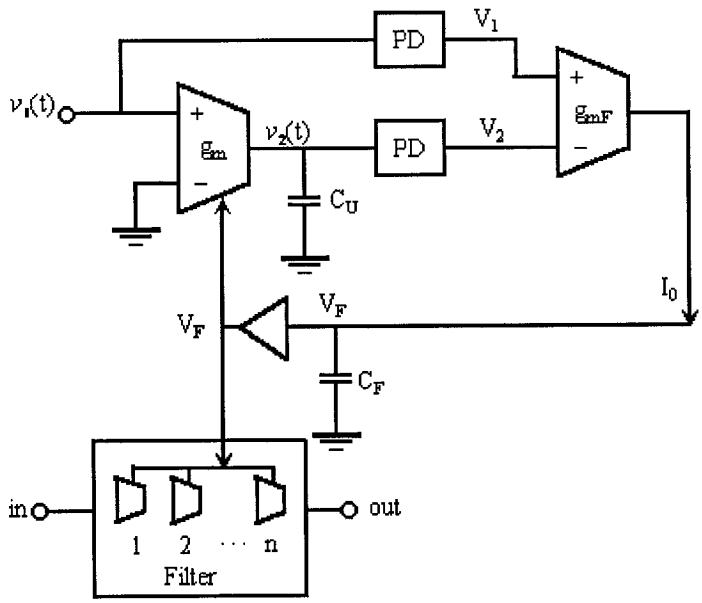


Figure 1-3: Magnitude-locked loop technique frequency tuning scheme

From this equation we see that $V_1 = V_2$ if $\frac{g_m}{C_U} = \omega_{ref}$. Sending both the reference voltage $v_1(t)$ and the output voltage $v_2(t)$ of the integrator through two identical peak detectors PD, the two dc outputs $V_1$ and $V_2$ are compared in an OTA with gain $g_{mF}$ that generates a current $I_0=g_{mF}(V_1-V_2)$. The current $I_0$ is integrated in a capacitor $C_F$ to generate a bias voltage. The values $g_{mF}$ and $C_F$ are not critical. $V_F$ is buffered and applied to the tuning terminal of the OTA whose transconductance value $g_m$ increases with rising

$V_F$. If now $V_1<V_2$, $g_m$ is too small, $I_0$ is positive, and the bias voltage $V_F$ increases so that $g_m$ becomes larger. If $V_1>V_2$, $g_m$ is too large, $I_0$ is negative, and the bias voltage $V_F$ decreases so that $g_m$ reduces. As soon as $V_1=V_2$, $I_0=0$, that is to say, $\frac{g_m}{C_U} = \omega_{ref}$. At this point the bias voltage is adjusted such that the transconductance $g_m$ is tuned so that the time constant is correct. Since capacitor ratios are realized accurately, the ratio of any capacitor $C_i$ to the unit capacitor $C_U$, $C_i/C_U$, can be implemented with very small error. Thus, all OTAs in the filter are tuned to the value $g_m$ by applying the buffered $V_F$ to their bias terminals. However, any DC offset voltage in the transconductance $g_m$ will translate into an incorrect peak value of $V_2$. This is interpreted by the comparator as an incorrect value of $g_m$ and will result in mistuning. Careful offset cancellation is necessary; therefore, differential design is beneficial so that offset voltages are subtracted out.

### 1.1.4 Envelope Detection Technique

Envelope detection technique has been proposed for high frequencies (around 150 MHz) and high quality factor of the filters. This technique uses envelope detection to obtain the filter magnitude response and to detect the center frequency. The magnitude response of a filter can be obtained by sweeping the input signal frequency and measuring the corresponding output magnitudes. Instead, in this scheme, a signal at a fixed reference frequency $\omega_{ref}$ is applied to the filter while the frequency control voltage

$V_{cntl}$ of the filter is swept to vary $g_m$. The time-domain envelope of the filter output reflects the filter's magnitude response, and the maximum value of the filter's magnitude response in time-domain is obtained when $g_m/C=\omega_{ref}$, which is the same as in frequency domain analysis (i.e., keeping $g_m$ constant and varying $\omega$). Figure 1-4 shows the block diagram for envelope detection technique frequency tuning. The first block, which consists of a differential full-wave rectifier, a level shifter and a buffer, is connected to the filter, and completes envelope detection. The second block is the envelope delay circuit. In order to detect a voltage value slightly below the peak level, the envelope is delayed and compared with its original such that $V_{fast}$ and $V_{slow}$ intersect at some point after the peak value. Through track-hold block, detection of the voltage corresponding to the center frequency, $V_{cntl}$, is carried out. However, this tuning scheme uses mixed mode analog-digital circuits, and the circuits are relatively complex. No experimental verification is available yet.

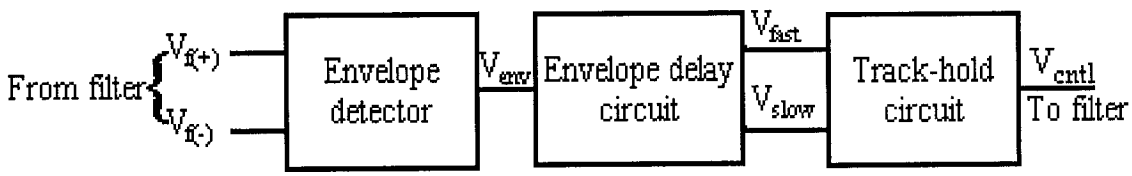


Figure 1-4: Block diagram of frequency tuning using envelope detection technique

## 1.2 Motivation

The basic principle of all of the above tuning schemes is to adjust the ratio of $g_m/C$ to meet the $g_m$-C filters' specification, and the tuning systems are complex. As was mentioned in the previous section, the variation of $g_m/C$ ratio in integrated circuits can be very large (i.e., up to 30-percent) without tuning. However, integrated capacitance tolerance, mainly due to process variations, typically accounts for about 10-percent variations [2]. Thus, in applications where a 10-percent variation can be permitted, it may be sufficient to set only the $g_m$ value near constant. In the case where 10-percent accuracy is not enough, clearly one must attempt to maintain $g_m/C$ as constant as possible. For the high precision capacitor, one way is using external capacitors that have very accurate values, and another way is to undertake initial tuning of elements via a laser trimming procedure to eliminate the effect of processing variations. But, because the transconductance gain ($g_m$) of OTAs changes not only with process variations, but also with operating conditions, the initial tuning techniques can not assure that the transconductance gain ($g_m$) of OTA remains stable when operating conditions, such as environmental temperatures, change.

In this thesis, a novel technique using simple negative feedback to stabilize the transconductance gain of an OTA against temperature variations is introduced, and its applications to several second-order $g_m$-C filters are illustrated.

One of OTAs' attractive features is that its transconductance can be controlled by changing the external DC bias voltage or current. The transconductance gain of OTAs is a nonlinear function of temperature. In our work, a negative feedback technique is applied to produce a temperature dependent control voltage (bias voltage) for the OTA to maintain the stability of $g_m$ against the temperature variation over the range of –30°C to +85°C, that is to say, this OTA has constant transconductance gain over the temperature range common in industrial environment. Furthermore, this control voltage is simultaneously applied to the OTAs in several second-order $g_m$-C filters. Thus, the center (cut-off) frequency and Q-factor of the $g_m$-C filters, which depend on the transconductance gain ($g_m$), are stabilized.

## 1.3 Thesis Outline

The thesis begins with an overview on the current tuning technology choices for continuous-time filters. In Section 1.1 above, the basic principles have been presented, and the advantage and limitation of each technique have been highlighted. Then a simple negative feedback technique to counteract the transconductance gain ($g_m$) change with temperature variation has been proposed.

In what follows, Chapter 2 provides a brief review of the basic theory related to the proposal of the thesis. The temperature behavior of a MOS transistor and

transconductance gain ($g_m$) of the OTA are discussed. Furthermore, the models for several kinds of second-order $g_m$-C filters (i.e., low-pass, band-pass, and notch filter) are presented.

In Chapter 3, the proposed technique of using simple negative feedback to stabilize the transconductance gain ($g_m$) of an OTA over the range of –30°C to +85°C is introduced. First, a block diagram of the system that ensures a near constant $g_m$ despite variations in the environmental temperature is described. Then the implementation aspect of every building block in the system is discussed. Finally, the overall control mechanism to counteract the effect of temperature variation is provided. As a practical example, the application of the technique to a second-order $g_m$-C filter is illustrated.

System implementation based on a modern CMOS integrated circuit technology (TSMC 0.18 μm) is considered in Chapter 4. Implementation methods for large resistors and capacitors in CMOS technology are illustrated. Layout techniques to minimize the side effects of transistor pair mismatch and parasitics are discussed. Pre-layout and post-layout simulation results are presented.

Chapter 5 presents the experimental results and discussion for an integrated system implemented using the fabrication facilities of Canadian Microelectronic Corporation. The tests over several temperatures have been carried out in the thermal

chamber facilities of CMC Electronics Inc. (Courtesy Mr. Alok Bhattacharya, Senior Metrologist).

The thesis concludes with a summary of the work done and suggestions for future work in Chapter 6.

## 1.4 Objectives

The following is a summary of the objectives of this thesis.

* Propose a new simple negative feedback technique to stabilize changes in the transconductance of the OTA with temperature variation over the range of –30°C to +85°C.

* Validate the proposed feedback technique by realizing several types of second-order $g_m$-C filters with the temperature stabilized OTAs.

* Implement a second-order $g_m$-C band-pass filter with feedback control system using TSMC 0.18 μm CMOS technology, and fabricate through the facilities of Canadian Microelectronics Corporation (CMC).

In summary, the system proposed in this thesis is very suitable for implementation in a modern CMOS technology, and may prove to be a suitable alternative to the techniques proposed so far in terms of power and area overhead requirements in an IC technological environment.

# Chapter 2

# Basic Principles

In this chapter, the temperature behavior of a MOS transistor is addressed. This is then followed by a detailed derivation of the expression for transconductance ($g_m$) of the OTA, and the equation reveals that the characteristics of the transconductance ($g_m$) depend on the temperature nonlinearly. Furthermore, several kinds of second-order $g_m$-C filters, for example, low-pass, high-pass, band-pass, all-pass and notch filters, are examined. The results display that if the transconductance $g_m$ values are stabilized against temperature variations, the center (cut-off) frequency and Q-factor, which depend upon the transconductance gain ($g_m$) of the OTAs, are also stabilized.

## 2.1 Temperature Behavior of a MOS Transistor

The OTAs are built from MOS transistors. MOS transistors have three regions of operation: cut-off, triode, and saturation region. In the CMOS OTA structure, to be introduced shortly, all transistors operate in the saturation region. The first-order equation [9] describing the behavior of an NMOS device in the saturation region (Although this simplified equation is not its accurate model for TSMC 0.18 μm technology since the second-order effects are ignored, it can give some guidance for the design of circuits.) is:

$$I_d = \mu \frac{\varepsilon_{ox}}{t_{ox}} (W/2L)(V_{gs} - V_{th})^2 \qquad 0 < V_{gs} - V_{th} < V_{ds} \qquad (2\text{-}1)$$

μ — carrier mobility in the channel,

$\varepsilon_{ox}$ — permittivity of the silicon oxide,

$t_{ox}$ — thickness of the oxide layer.

The primary temperature dependent parameters are the mobility 'μ' and the threshold voltage '$V_{th}$'. The temperature dependence of the carrier mobility μ is given as [10]:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^n \qquad (2\text{-}2)$$

where T is absolute temperature in Kelvin's degrees (°K), $T_0$ is room temperature (300 °K), and the exponent n is between -1.09 and –2.17 dependent on the size [11] of a NMOS transistor based on TSMC 0.18 μm technology. Thus, for a 100°C temperature

increase, mobility may decrease by as much as 21.1% to 37.7%. In turn, the current consumption of a complete circuit may decrease considerably at high temperature. We shall use:

$$K(T) = \mu(T)\frac{\varepsilon_{ox}}{t_{ox}} \qquad (2\text{-}3)$$

For a particular technology, the permittivity of the silicon oxide $\varepsilon_{ox}$ and thickness of the oxide layer $t_{ox}$ are constant, so:

$$K(T) = K(T_0)\left(\frac{T}{T_0}\right)^n \qquad (2\text{-}4)$$

The temperature dependence of the threshold voltage can be approximated by the following expression [12]:

$$V_{th}(T) = V_{th}(T_0) + \alpha\left(\frac{T}{T_0} - 1\right) \qquad (2\text{-}5)$$

This expression is valid over the range of 200° ~ 400° K, with α depending on the substrate doping level and the implant dose used during fabrication. Here α is between –0.20 and –0.24 [11] dependent on the size of a NMOS transistor based on TSMC 0.18 μm CMOS process. When temperature is increased, the decrease in $V_{th}$ gives rise to a corresponding increase in drain current. However, since μ decreases with temperature and its effect is a dominant one, the overall observed effect of a temperature increase is a decrease in drain current. Therefore, the ac transconductance ($g_m$) of a MOS transistor changes with temperature in accordance with:

$$g_m(T) = \sqrt{2K(T)(W/L)I_d(T)} \qquad (2\text{-}6)$$

## 2.2 Properties of Operational Transconductance Amplifier

Operational Transconductance Amplifier (OTA) is a very useful building block in analog systems design. Since the transconductance gain of OTAs is electronically variable, they are widely applied in continuous-time integrated filters, analog multipliers, nonlinear circuits and closed loop applications mainly for switched-capacitor circuits.

### 2.2.1 Models of the OTA

The circuit symbol and the small signal equivalent circuit of an ideal operational transconductance amplifier are shown in Figure 2-1. An ideal OTA is a voltage controlled current source described by

$$i = g_m(v_+ - v_-) \qquad (2\text{-}7)$$

whose input and output impedances are both infinite, as illustrated in the diagram of Figure 2-1(b). In many designs, the transconductance ($g_m$) is variable by setting a control

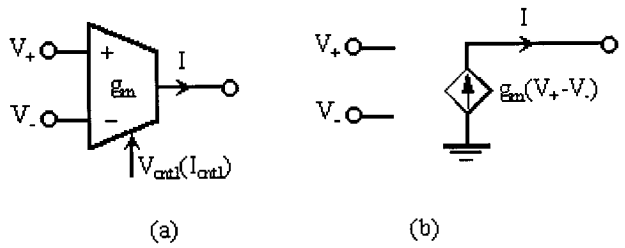


Figure 2-1: (a) Circuit symbol of an OTA, (b) the ideal model of an OTA

bias voltage or current, $V_{cntl}$ or $I_{cntl}$. But, the real OTA has finite input and output impedances that can be modeled as shown in Figure 2-2. Note the impedances from the inverting and noninverting input terminals to ground are assumed to be equal, and any impedance between the input terminals is neglected. The transconductance gain ($g_m$) has a finite bandwidth. However, in this thesis, the ideal model of an OTA will be applied to simplify the analysis.

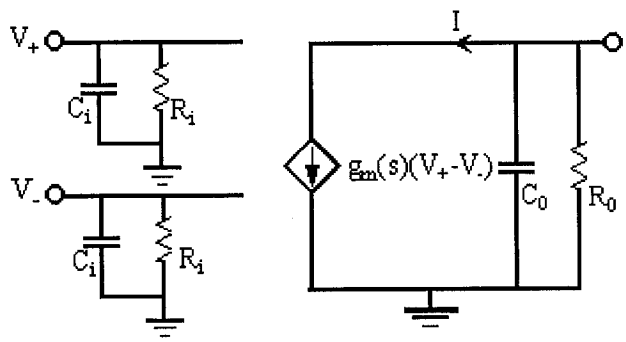


Figure 2-2: Real OTA model with frequency dependent $g_m$

## 2.2.2 Characteristics of OTA

Two of the key attractive properties of OTAs are: (1) operation at higher frequencies in comparison with conventional OP-AMPs, and (2) tunability of the transconductance using a bias voltage or current. The wideband of the OTA is due to, in part, the fact that their internal nodes are low impedances. However, the main limitation of a practical OTA are: (1) limited linear input voltage range, (2) finite output

impedance, and (3) the transconductance ($g_m$) is temperature sensitive. In this thesis, we shall consider OTAs built from MOS transistors. Several techniques have been employed to increase the linear range at the input. These involve: (a) attenuation, (b) nonlinear terms cancellation, and (c) source degeneration. Some details can be found in [13]. The output impedance can be increased using cascode structures at the expense of reduced output signal swing. In this thesis, design of a high performance OTA has not been considered. The main concern is to produce a temperature dependent control voltage to stabilize the transconductance gain ($g_m$) of an OTA against temperature variation. So, a simple common source differential pair, as shown in Figure 2-3, is chosen as an OTA. As regards design of OTAs with high output impedance and high linearity, several circuits are available in the literature [14], [15].

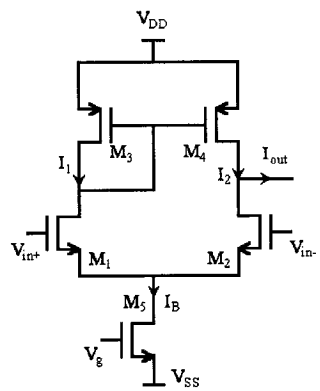


Figure 2-3: Differential pair OTA

This OTA has a differential input pair $M_1$, $M_2$, a current mirror load $M_3$, $M_4$, and a constant current $I_B$ for biasing, derived from $M_5$. The output current for the small signal operation is:

$$i_{out} = g_m(v_{in+} - v_{in-}) \tag{2-8}$$

When all transistors work in saturation region, and the temperature variation is considered, using the square law I-V equation, we can derive:

$$g_m(T) = K(T)\sqrt{\frac{W_4 W_5}{2L_4 L_5}}\left(V_g - V_{ss} - V_{th}(T)\right) \tag{2-9}$$

From this equation, it is obvious that the transconductance ($g_m$) of the OTA changes with temperature. To illustrate what equation (2-9) really means, we have done a simulation experiment. An OTA with a particular transconductance gain at room temperature (i.e., 314 μ mho at 27°C) using the above structure is built based on TSMC 0.18 μm CMOS technology. The simulation result, as shown in Figure 2-4, displays that the transconductance gain ($g_m$) is a nonlinear function of temperature when the bias voltage

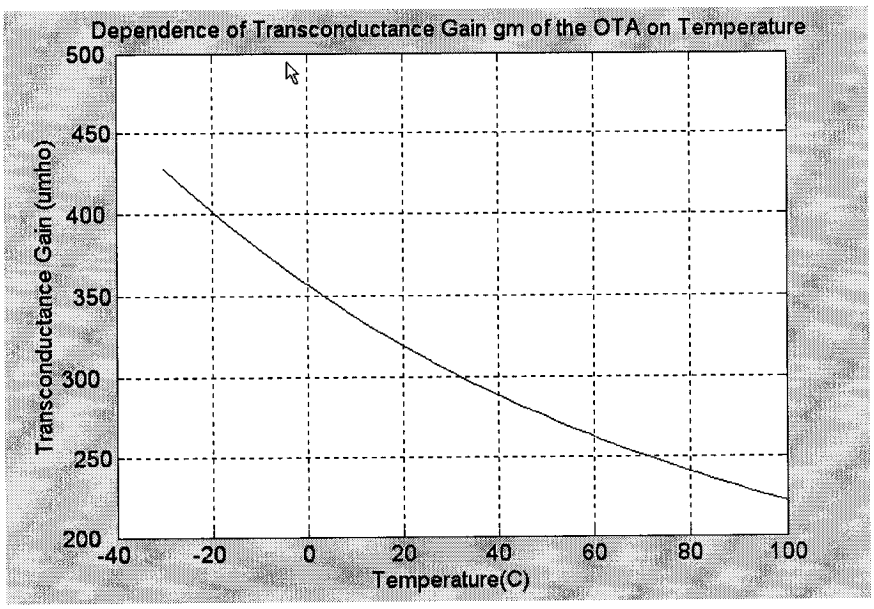


Figure 2-4: Dependence of transconductance gain ($g_m$) of the OTA on temperature

$V_g$ is fixed. This causes the characteristics of the OTA-based circuit to be strongly dependent on the temperature.

On the other hand, equation (2-9) indicates that the only way to keep the transconductance gain ($g_m$) of the OTA constant at different temperatures will be to adjust the bias voltage $V_g$ with temperature variation. The transconductance gain ($g_m$) of the OTA is controlled by the voltage $V_g(T)$ according to the expression:

$$g_m(T)\mid_{V_g(T)} = K(T)\sqrt{\frac{W_4 W_5}{2L_4 L_5}}\left(V_g(T) - V_{ss} - V_{th}(T)\right) \qquad (2\text{-}10)$$

At room temperature $T_0$,

$$g_m(T_0)\mid_{V_g(T_0)} = K(T_0)\sqrt{\frac{W_4 W_5}{2L_4 L_5}}\left(V_g(T_0) - V_{ss} - V_{th}(T_0)\right) \qquad (2\text{-}11)$$

In order to meet the requirement of $g_m(T)\mid_{V_g(T)} = g_m(T_0)\mid_{V_g(T_0)}$ at different temperatures, the control voltage $V_g(T)$ has to be adjusted as:

$$V_g(T) = \frac{K(T_0)\left(V_g(T_0) - V_{ss} - V_{th}(T_0)\right)}{K(T)} + V_{ss} + V_{th}(T) \qquad (2\text{-}12)$$

It is obvious that $V_g(T)$ is a nonlinear function of temperature. In Chapter 3, a novel negative feedback technique will be proposed to obtain a temperature dependent control voltage so that the transconductance ($g_m$) of the OTA is held close to $g_m(T_0)$ over a wide temperature range.

## 2.3 Mathematical Models of Filters

Filters as linear systems can be easily analyzed and synthesized using network transfer functions in frequency domain. In continuous-time domain, Laplace transform technique can be used to model the transfer functions. Referring to Figure 2-5, the


Figure 2-5: Schematic representation of a filter system

schematic representation of a filter system, in continuous-time domain, the filter transfer function can be defined in terms of Laplace-transformed excitation *X(s)* and the zero-state response *Y(s)*:

$$H(s) = \frac{L[y(t)]}{L[x(t)]} = \frac{Y(s)}{X(s)} = \frac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_0} = \frac{N(s)}{D(s)} \tag{2-13}$$

where $m \leq n$ for any realizable physical network. N(s) and D(s) are the numerator and denominator polynomials, respectively, and $n$ is the order of the filter.

In normal case for filters, Y(s) and X(s) in equation (2-13) are voltage transforms

[i.e. $V_{out}$ (s) and $V_{in}$ (s), respectively], $H(s) = V_{out} / V_{in}$ is referred to as the voltage transfer function.

Filters are typically categorized according to the filtering function performed. If magnitude (gain, attenuation) requirements are of primary importance, the filters are classified as low-pass, high-pass, band-pass, or band-stop (low-pass, high-pass notch) networks. In some applications, if one is mainly concerned with phase or delay specifications with no change in magnitudes, the filters typically will be either all-pass networks or delay equalizers.

Table 2-1 on next page presents the analytical expressions for standard biquad filter transfer functions. It may be noted that the denominator function D(s) is same for all five filter types, while the numerator function N(s) changes depending upon the specific type of the filter.

**Table 2-1 Standard Biquad Transfer Functions**

[Note: $H(s)=\frac{N(s)}{D(s)}$, with $D(s)=s^2+(\omega_p/Q_p)s+\omega_p{}^2$, for all filters]

| Type of filter | $N(s)$ |
|---|---|
| Low-pass (LPF) | $H_0\omega_p{}^2$ |
| Band-pass (BPF) | $H_0(\omega_p/Q_p)s$ |
| High-pass (HPF) | $H_0 s^2$ |
| All-pass (APF) | $s^2-(\omega_p/Q_p)s+\omega_p{}^2$ |
| Low-pass, High-pass Notch (LPN, HPN) | $H_0(s^2+\omega_n{}^2)$ |

In the above table $\omega_p$ is known as the pole frequency and $Q_p$ as the quality factor (pole-Q) of the filter. In the notch filter when $\omega_n$ is less than $\omega_p$, the filter is known as a high-pass notch (HPN). If $\omega_n$ is higher than $\omega_p$, the filter is known as a low-pass notch (LPN) filter. The poles of the transfer function are given by:

$$p_0=\sigma_0\pm\omega_0=-\frac{\omega_p}{2Q_p}\pm j\frac{\omega_p}{2Q_p}\sqrt{4Q_p{}^2-1} \qquad (2\text{-}14)$$

For a highly selective filter $Q_p$ shall be very high which implies that the real part of the pole will have a small magnitude. As long as the real part is negative and $Q_p$ is positive, the filter represents a stable network. It is also understood that, for a complex pole pair, the quantity $4Q_p{}^2-1$ must be positive, i.e., $Q_p$ must be higher than 0.5.

### 2.3.1 Transconductance-C (or $g_m$-C) Filters

Analog continuous-time filters are a basic building block in many electronic systems. The trend in modern integrated circuits is to incorporate as many system blocks as possible in a single chip with the motivation towards a complete system on a chip.

$g_m$-C filters are very amenable to monolithic implementation. This design method generally uses only operational transconductance amplifiers and capacitors and is referred to as the transconductance-C (or $g_m$-C) filter. With OTAs having $g_m$ of few hundred micro mhos and on-chip capacitors of few picofarads, the operation can be extended to applications at hundreds of megahertz. $g_m$-C filters are preferred specifically for application at high-frequencies. Nevertheless, the critical problem in the design of this kind of filters is their need for some sort of tuning circuitry. Phase locked loop technique [3][4][5] has been popular for low frequency. Envelope detection technique using mixed mode analog-digital circuits has been proposed for frequencies around 150 MHz [7][8]. There are additional challenges for high frequency $g_m$-C filters. Thus, parasitic capacitance and finite bandwidth of the $g_m$ of the OTA can affect the filter performance.

OTAs are main components of $g_m$-C filters, and environmental effect, such as temperature variation, has a detrimental effect on the performance of $g_m$-C filters. Temperature change affects the $g_m$ of the OTA. The dependence of transconductance gain

($g_m$) of a typical OTA on temperature has been shown in Figure 2-4 in Section 2.2.2.

## 2.3.2 Mathematical Models of Second-order $g_m$-C Filters

In the following, several structures and corresponding transfer functions for second-order $g_m$-C filters are presented.

### 2.3.2.1 A Second-order Band-pass $g_m$-C Filter

The schematic diagram of a typical second-order $g_m$-C band-pass filter and the associated ac equivalent circuit are shown in Figure 2-6.

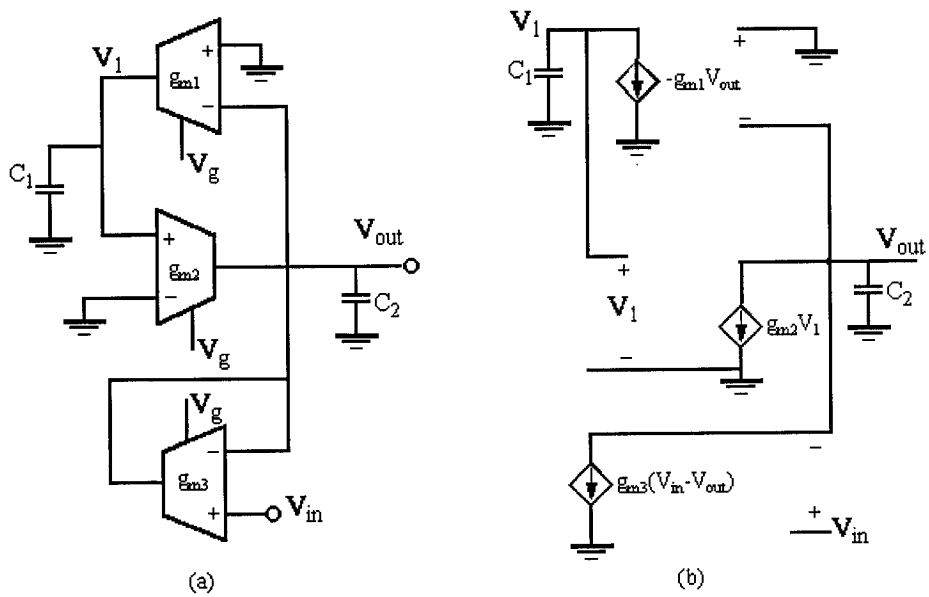


Figure 2-6: (a) The schematic diagram of a second-order $g_m$-C band-pass filter,

(b) The associated ac equivalent circuit.

Using nodal analysis, the transfer function of this filter is [1]:

$$H(s)=\frac{V_{out}}{V_{in}}=\frac{(g_{m3}/C_2)s}{s^2+(g_{m3}/C_2)s+g_{m1}g_{m2}/C_1C_2} \qquad (2\text{-}15)$$

The transfer function of standard BIQUAD band-pass filters based on Table 2-1 is:

$$H(s)=\frac{H_0(\omega_p/Q_p)s}{s^2+(\omega_p/Q_p)s+{\omega_p}^2} \qquad (2\text{-}16)$$

Comparing (2-15) with (2-16), the expressions of the center frequency and Q-factor are, respectively:

$$\omega_p=\sqrt{g_{m1}g_{m2}/C_1C_2} \qquad (2\text{-}17)$$

$$Q_p=\frac{\omega_p}{g_{m3}/C_2}=\frac{\sqrt{g_{m1}g_{m2}/C_1C_2}}{g_{m3}/C_2} \qquad (2\text{-}18)$$

From these formulas, it is obvious that the center frequency and Q-factor are dependent on the transconductance gain ($g_m$). Furthermore, the equation (2-9) and the Figure 2-4 reveal the transconductance gain ($g_m$) of the OTA is a nonlinear function of temperature. That is to say, if the transconductance ($g_m$) values are stabilized against temperature variations, the center frequency and Q-factor will be also stabilized.

This second-order band-pass filter structure has been adopted for this thesis work. To simplify the circuit, all OTAs in this $g_m$-C band-pass filter have been arranged to have the same transconductance value and same capacitance, i.e., $g_{m1}= g_{m2}= g_{m3}=g_m$, $C_1=C_2=C$. Thus:

$$\omega_p = \frac{g_m}{C} \qquad (2\text{-}19)$$

$$Q_p = 1 \qquad (2\text{-}20)$$

Taking $g_m$=314 μ mho and C =5 pF, the design value of center frequency is 10 MHz with $Q_p$=1.

### 2.3.2.2 A General Biquadratic $g_m$-C Filter

Figure 2-7(a) presents a structure, which can be used to realize any of the five standard biquadratic transfer functions. It consists of five OTAs, and the analysis can be carried out using the ac equivalent circuit as shown in Figure 2-7(b). Thus,

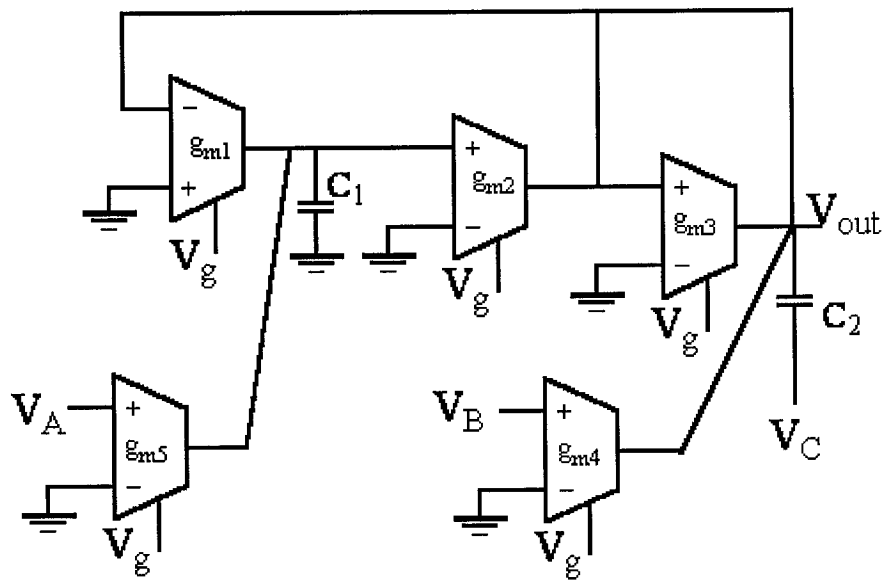


Figure 2-7: (a) General biquadratic structure

By inspection, one can write:

$$i_{C_1} = -g_{m5}V_A + g_{m1}V_o \tag{2-21}$$

$$V_x = \frac{i_{C_1}}{sC_1} = \frac{g_{m1}V_o - g_{m5}V_A}{sC_1} \tag{2-22}$$

KCL at node $V_y$ leads to:

$$g_{m2}V_x + g_{m4}V_B + g_{m3}V_o + sC_2(V_o - V_C) = 0 \tag{2-23}$$

Substituting $V_x$ from equation (2-22), yields:

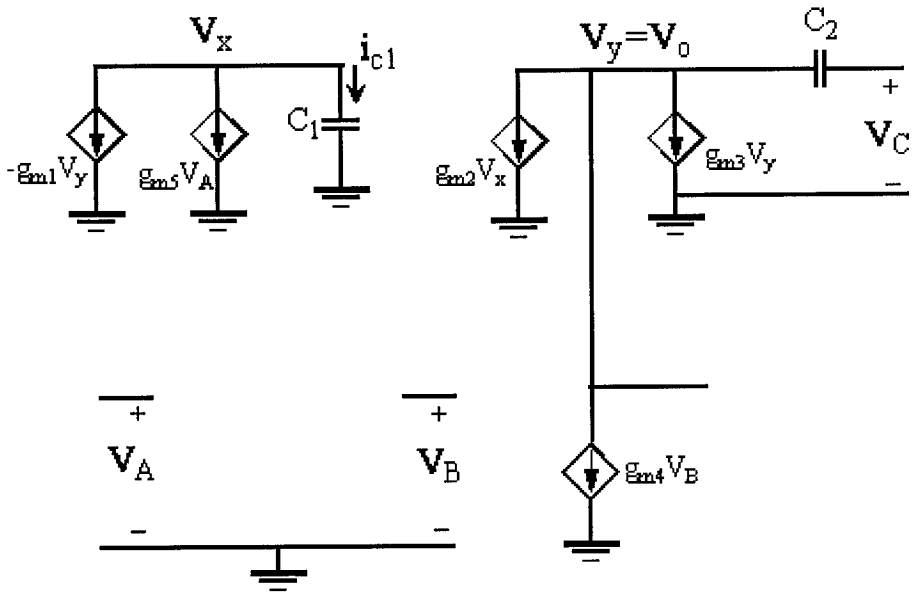


Figure 2-7: (b) Small signal equivalent circuit

$$g_{m2}\frac{g_{m1}V_o - g_{m5}V_A}{sC_1} + g_{m4}V_B + g_{m3}V_o + sC_2(V_o - V_C) = 0 \tag{2-24}$$

Simplifying and rearranging:

$$V_o = \frac{s^2 C_1 C_2 V_C - s g_{m4} C_1 V_B + g_{m2} g_{m5} V_A}{s^2 C_1 C_2 + s C_1 g_{m3} + g_{m1} g_{m2}} \quad (2\text{-}25)$$

The denominator of equation (2-25) has the standard form with

$$\omega_p = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \quad (2\text{-}26)$$

$$\frac{\omega_p}{Q_p} = \frac{g_{m3}}{C_2} \quad (2\text{-}27)$$

So that

$$Q_p = \frac{1}{g_{m3}} \sqrt{\frac{g_{m1} g_{m2} C_2}{C_1}} \quad (2\text{-}28)$$

By examining equation (2-25), it turns out that one needs to suitably choose signal voltage $V_A$, $V_B$, and $V_C$ to produce the different transfer functions. Thus:

For LPF, choose $V_i=V_A$, and $V_B=V_C=0$

For HPF, choose $V_i=V_C$, and $V_A=V_B=0$

For BPF, choose $V_i=V_B$, and $V_A=V_C=0$

For Notch filter, choose $V_i=V_A=V_C$ and $V_B=0$

For APF, choose, $V_i=V_A=V_B=V_C$, $g_{m3}=g_{m4}$ and $g_{m1}=g_{m5}$

In practical circuits, the points $V_{A(B,C)}=0$ should be grounded to reduce the noise interference.

From the equations (2-26) and (2-28), one can easily understand that if the transconductance ($g_m$) values are stabilized against temperature variations, the pole frequency $\omega_p$ and pole Q of the general biquadratic $g_m$-C filter will also be stabilized.

## 2.4 Summary

In this chapter, the temperature behavior of a MOS transistor has been discussed. The expression for transconductance gain ($g_m$) of the differential pair OTA reveals that the $g_m$ is a nonlinear function of temperature. The mathematical models for several kinds of second-order $g_m$-C filters (i.e., low-pass, high-pass, band-pass, all-pass and notch filter) have been presented, and these models reveal that the pole frequency and pole Q of $g_m$-C filters are dependent on the transconductance gain ($g_m$). That is to say, if the transconductance ($g_m$) values are stabilized against temperature variations, the pole frequency and pole Q will also be stabilized.

# Chapter 3

# The Proposed Negative Feedback System

In Chapter 2, we have discussed the temperature dependence of the transconductance ($g_m$) of an OTA. The impact of this effect on the pole-frequency ($\omega_p$) and pole-Q ($Q_p$) of typical second-order $g_m$-C filters has been highlighted. In this chapter we introduce the proposed negative feedback system, which will reduce the change in transconductance due to temperature variations substantially. In Section 3.1, we present the block diagram of the control system, and the principle of operation is explained. Analysis and design aspects of the various subsystems using a modern CMOS technological process (TSMC 0.18 μm CMOS technology) are addressed in Section 3.2. Results obtained by simulation are included to validate the design goals. The overall control mechanism is explained in Section 3.3.

## 3.1 Block Diagram of the Control System

Figure 3-1 shows the block diagram of the control system. The function of the slave subsystem is to provide a temperature dependent control voltage $V_g(T)$ to the master subsystem to stabilize the transconductance of the OTAs in the master subsystem against temperature variation. The master subsystem could be, for example, a second-order $g_m$-C band-pass filter.

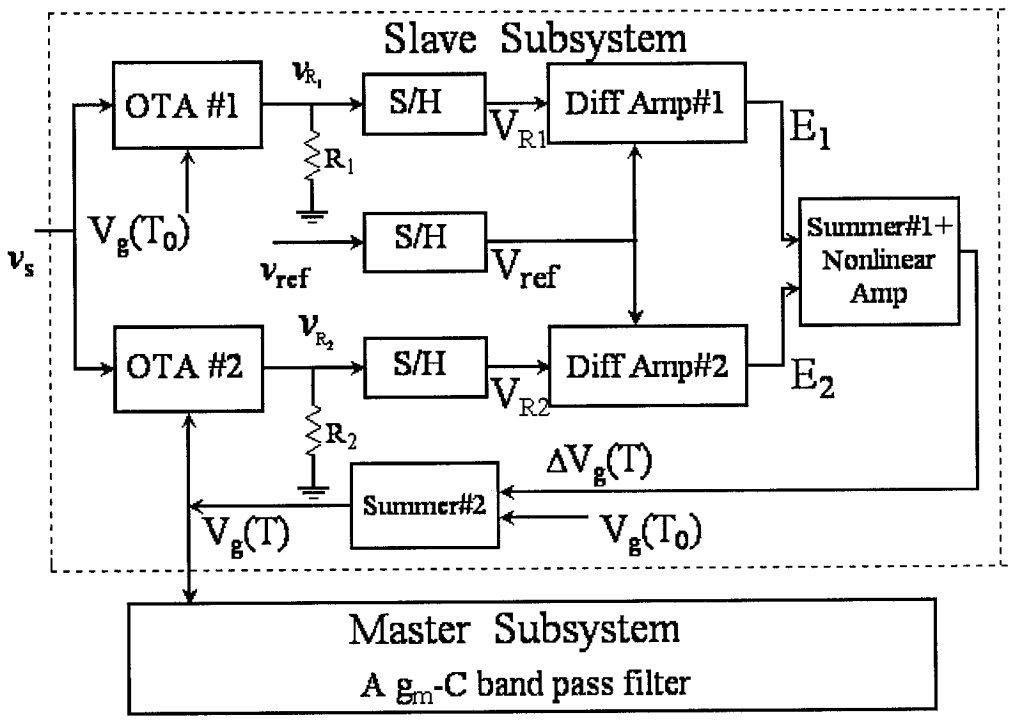


Figure 3-1: The block diagram of the control system

The slave subsystem includes two forward paths and one feedback path. In the

forward paths, the resistors $R_1$ and $R_2$ at the outputs of OTA#1 and OTA#2 are used to measure the $g_m$ values of the OTAs, that is to say, the voltage drop across the resistors depends on the transconductance ($g_m$) of the OTAs. The sample-and-hold (S/H) circuits hold the peak instantaneous voltage values to process them further. The difference amplifiers #1 and #2 compare the standard voltage $V_{ref}$ (the output voltage of the OTA at room temperature) with the output voltages $V_{R1}$ and $V_{R2}$ respectively. The outputs of these difference amplifiers produce the static error signal $E_1$ and dynamic error signal $E_2$. E1 and E2 are amplified and added together using the nonlinear amplifier and summer #1, whose gain changes with temperature variation, to produce the error control voltage $\Delta V_g(T)$ at a temperature T. In the feedback path, through summer#2, $\Delta V_g(T)$ and a fixed bias voltage $V_g(T_0)$ are summed to produce the temperature dependent control voltage $V_g(T)$. This control voltage is applied to OTA#2 to close the control loop. $V_g(T)$ is also simultaneously applied to the OTAs in the master subsystem to stabilize the respective transconductance ($g_m$) values.

## 3.2 Analysis and Design Aspects of the Subsystems

### 3.2.1 The Operational Transconductance Amplifier (OTA)

We have selected a simple differential pair as the OTA to establish our control strategy. The OTA schematic is shown in Figure 3.2.

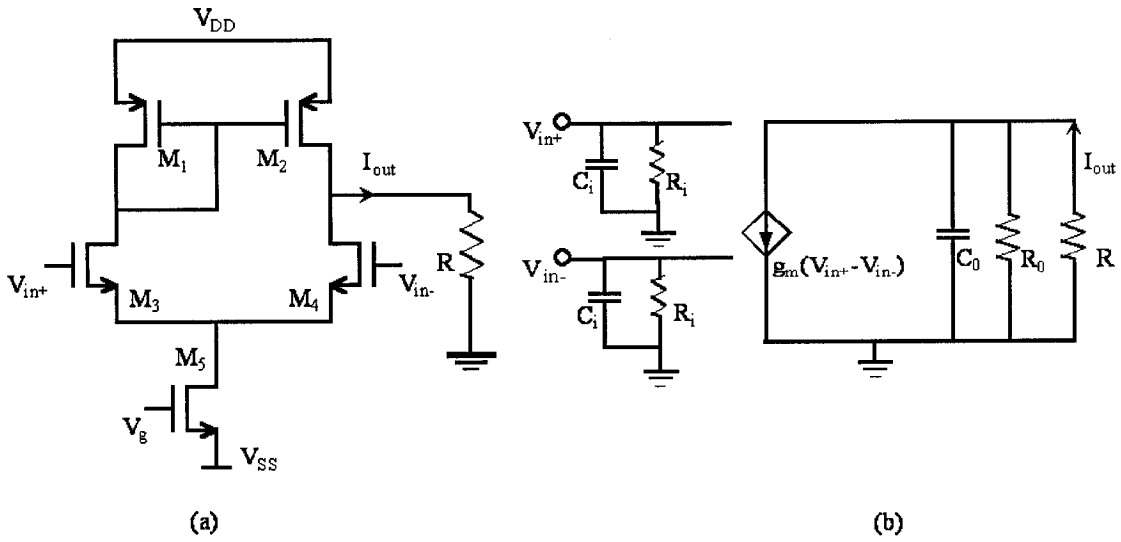


Figure 3-2: The differential pair OTA (a) schematic, (b) small signal equivalent circuit

### 3.2.1.1 Design Data for the OTA

The differential pair shown in Figure 3-2 is used as the OTAs in the whole system. The sizes of the transistors and the DC supply values are shown in Table 3-1.

**Table 3-1 Design Data for the Differential Pair OTA**

| Transistor | $M_1$ and $M_2$ | $M_3$ and $M_4$ | $M_5$ | |
|---|---|---|---|---|
| (W/L)* ratio | 11.39/1.44 | 0.95/1.44 | 1.4/2.88 | |
| Power supply (V) | VDD | +1.8 | VSS | -1.8 |
| Reference voltage (V) | $V_g$ | -0.5 | | |

Note: * W and L are in microns each (L: Length, W: Width).

In this thesis, all implementations are based on TSMC 0.18 μm CMOS technology. The nominal transconductance of the OTA (at 27°C) is 314 μ mhos.

### 3.2.1.2 Measurement for the Transconductance of OTA

The basic idea in the control system is to derive an error voltage signal proportional to the difference of the transconductance gain ($g_m$) of the OTA at 27°C and at any other given temperature. In this system, we apply a resistor R (=$R_1$=$R_2$ in Figure 3-1) at the output of the OTA to develop a voltage, which will change with temperature variations. For the OTA, the output is taken from the drain terminals, which have high output resistance. If the load resistor R has a small value, for example, 1KΩ, the output voltage will be

$$v_R = i_{out} R \qquad (3\text{-}1)$$

However, $i_{out} = g_m (v_{in+} - v_{in-})$, thus:

$$v_R = g_m (v_{in+} - v_{in-}) R \qquad (3\text{-}2)$$

The measurement results for the differential pair OTA, obtained by simulation, are tabulated in Table 3-2. The output resistances and transconductance gain ($g_m$) with fixed bias voltage $V_g$ (i.e. -0.5V) at the different temperatures are listed in column 2 and column 3. Column 4 is the calculated peak voltage drop across the 1 KΩ load resistor R based on equation (3-2) and column 3. The input signal to the OTA is a sinusoidal signal

with 50 mV magnitude and 10 MHz frequency. Column 5 is the measured peak value of the voltage drop across the 1 KΩ load resistor R. The small differences between the values in column 4 and 5 are due to a finite output resistance of the OTA.

**Table 3-2 Measured vs Calculated Transconductance of the OTA**

| Temperature | Output Resistance (KΩ) | $g_m$ Value with Fixed $V_g$ (μ mho) | Calculated Output Voltage Drop (mV) | Measured Output Voltage Drop (mV) |
|---|---|---|---|---|
| 85°C | 1089 | 239.5 | 11.98 | 11.59 |
| 27°C | 856.7 | 314 | 15.7 | 14.98 |
| 0°C | 750.4 | 364.4 | 18.22 | 17.22 |
| -30°C | 634.6 | 438.5 | 21.93 | 20.53 |

### 3.2.2 Sample-and-Hold Circuit

The sample-and-hold (S/H) circuit is a key block for many applications, such as analog to digital or digital to analog converters, analog multiplexers, and data acquisition system. Its basic function is to transform a continuous time signal into a step wise signal for further processing. In our system, the sample-and-hold block retains instantaneous voltage outputs from the OTA at specific time points. The output of the S/H circuit

resembles a DC voltage, proportional to the $g_m$ of the OTAs at a given temperature. Two important requirements for the sample-and-hold circuit are: (1) ease of implementation using CMOS process, (2) relatively high precision. Some simple sample-and-hold circuits will be described first, followed by discussion on some improved sample-and-hold circuits. Finally, a simple and feasible sample-and-hold circuit is proposed.

### 3.2.2.1 The Basic Sample-and-Hold Circuit

One basic circuit configuration commonly used to implement monolithic sample-and-hold circuit is shown in Figure 3-3 (a). This architecture potentially offers the

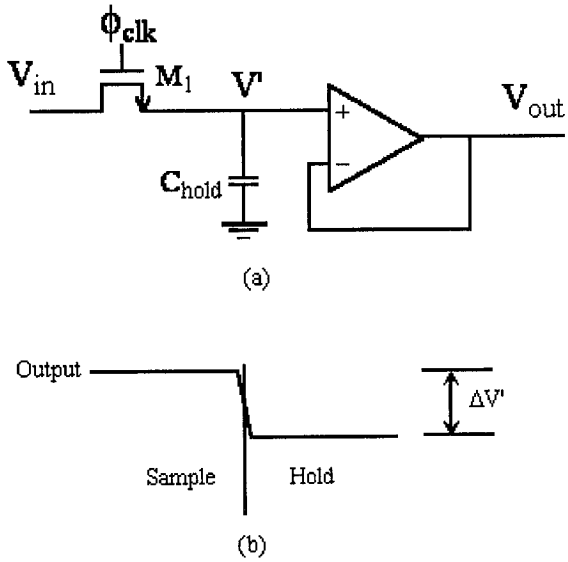


Figure 3-3: Basic sample-and-hold architecture

fastest implementation of the sampling function. The simplest sample-and-hold circuit consists of a switch, shown implemented with MOS pass transistor $M_1$, which samples the input onto a hold capacitance $C_{hold}$. A high-input-impedance unity-gain amplifier buffers the hold capacitance and provides a low-impedance output node that drives the follow-up circuitry. When $\phi_{clk}$ is high, V' follows $V_{in}$. When $\phi_{clk}$ goes low, V' will ideally hold the value of $V_{in}$ at that instance. Unfortunately, V' will have a negative going hold step, which is an error that occurs each time a sample-and-hold goes from sample mode to hold mode. This hold step, as illustrated in Figure 3-3 (b), is caused by charge injection. When $M_1$ conducts, a finite amount of mobile carriers are stored in the channel. However, when $M_1$ turns off, the channel charge exits through the source and drain electrodes. The charge transferred to the data node during the transistor turning-off period superposes an error component to the sampled voltage. In addition to the charge from the intrinsic channel, the charge associated with the feed-through effect of the gate-to-diffusion overlap capacitance also enlarges the error voltage after the transistor turns off. Since this charge is negative, it will cause the junction voltages to have negative glitches [16].

The circuit schematic corresponding to the general case of switch charge injection is shown in Figure 3-4. Also shown in Figure 3-4 are the parasitic capacitances, $C_{gs}$ and $C_{gd}$, caused by gate-drain and gate-source overlap capacitors. Capacitance $C_L$ is the lumped capacitance at the data-holding node. Resistance $R_S$ could be the output resistance of the preceding stage, while capacitance $C_S$ could be the lumped capacitance

associated with the output node of the preceding stage.

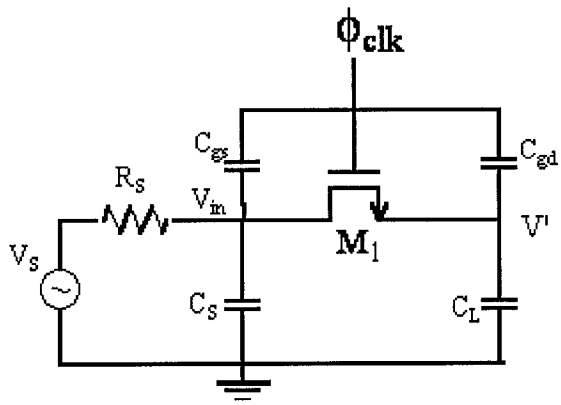


Figure 3-4: Circuit for analysis of switch charge injection

The change in the voltage V' due to charge injection effect is given by [2]:

$$\Delta V' = -\frac{C_{ox}WL(V_{DD} - V_{th} - V_{in})}{2C_{hold}} \qquad (3\text{-}3)$$

Notice that $\Delta V'$ is linearly related to $V_{in}$, which results in a gain error for the overall sample-and-hold circuit. However, more importantly, $\Delta V'$ is also linearly related to $V_{th}$, which is nonlinearly related to the input signal, $V_{in}$, due to variations in the source-substrate voltage. Assuming the substrate is tied to $V_{SS}$, the $V_{th}$ is given by:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|V_{in} - V_{SS}| + \varphi} - \sqrt{\varphi}\right) \qquad (3\text{-}4)$$

$V_{th0}$ is threshold voltage for zero source-substrate voltage, $\gamma$ the body effect parameter, and $\varphi$ the Fermi potential. This nonlinear relationship with $V_{in}$ results in distortion of the overall sample-and-hold circuit.

There is also an additional change in V' due to the gate overlap capacitance. This can be calculated using the capacitor-divider circuit shown in Figure 3-5. The charge in $V_{out}$ due to a charge in $V_{in}$ is given by [2]:

$$\Delta V_{out} = \Delta V_{C2} = \frac{\Delta Q_{C2}}{C_2} = \frac{\Delta V_{in} C_1}{C_1 + C_2} \tag{3-5}$$

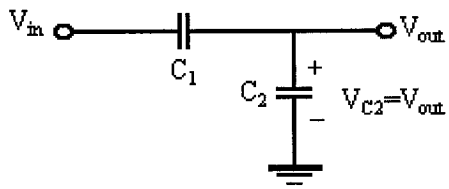


Figure 3-5: A capacitor divider

This formula can be applied to the circuit of Figure 3-4 to calculate the change in V' due to the overlap capacitance of M1 when it turns off. For this case, we have $C1=C_{gd}$, $C_2=C_{hold}$, and $\Delta V_{in}= -V_{DD}$. The change in V' due to the overlap capacitance is then given by

$$\Delta V' = \frac{-V_{DD} C_{gd}}{C_{gd} + C_{hold}} \tag{3-6}$$

Approximately, we have

$$\Delta V' = -\frac{C_{ox} W L_{ov} V_{DD}}{C_{hold}} \tag{3-7}$$

This change is normally less than that due to the change caused by the channel charge

since $L_{ov}$ is small. The component appears simply as an offset since it is signal independent. The offset can be removed in our system when the sampled data in two paths are compared in the differential amplifier.

For our case reduction of the switch charge injection is very important. The Miller hold capacitance technique [17] may be used to achieve the goal. In this approach, the input is sampled onto an equivalent hold capacitance that is small during the sampling mode, but is electrically increased during the hold mode by means of Miller feedback.

The Miller capacitance sample-and-hold circuit is shown in Figure 3-6. In this

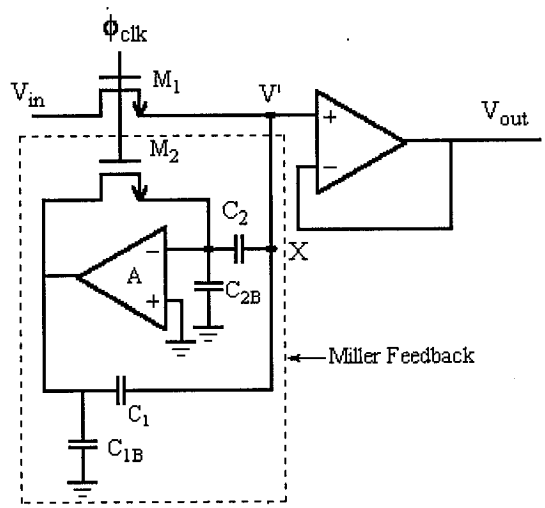


Figure 3-6: Sample-and-hold circuit using a Miller hold capacitor

circuit, the equivalent hold capacitance is formed by a combination of capacitors $C_1$ and $C_2$, the MOS pass transistor $M_2$, and an inverting amplifier with gain A. $C_{1B}$ and $C_{2B}$ represent the parasitic bottom-plate capacitances associated with $C_1$ and $C_2$, respectively.

When the circuit of Figure 3-6 is in the sample mode, both $M_1$ and $M_2$ are conducting. The switch $M_2$ bypasses the amplifier, and the bottom plates of both $C_1$ and $C_2$ are thus connected to the output of the amplifier, which has low output impedance. $M_2$ also maintains the amplifier at the threshold point of its transfer characteristic, i.e., the input and output are fixed at around one half of the power supply voltage $V_{DD}$. With sampling switch $M_1$ closed, the input voltage is sampled onto capacitors $C_1$ and $C_2$ at the hold node X.

During the transition from the sample mode to the hold mode, the rapid turn-off of transistors $M_1$ and $M_2$ results in the injection of channel charge and the capacitive coupling of the clock signal onto node X and the bottom plate of capacitor $C_2$. Since the drain and source of $M_2$ are at the threshold point of the amplifier transfer function during the sample mode, the charge injected from its turn-off is essentially independent of the input. The drain and source of $M_1$ are at the input potential during sampling; thus the charge injected during turn-off has a large input dependence and is a potential source of sampling error. If the coupling between the two switch transistors during turn-off is assumed to be minimal, then the charge injection and capacitive coupling can be modeled

as two independent current source charge injections as shown in Figure 3-7.

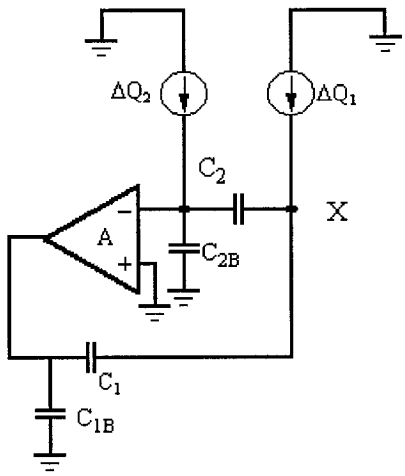


Figure 3-7: Equivalent model of Miller-effect sample-and-hold circuit during transition to hold mode

Analysis shows that in this system the charge injection due to switch M2 creates a fixed offset while one due to the signal bearing switch $M_1$ is attenuated by virtue of Miller effect. This technique, however, require big substrate area.

### 3.2.2.2 Proposed Sample-and-Hold Circuit

In order to satisfy the requirements of high sampling speed and high sampling precision, we have used an arrangement using dummy switches, as shown in Figure 3-8.

Switching two dummy switches with the inverted gate voltage $\overline{\phi_{clk}}$, opposite charges are provided to compensate the charge injection from the sampling switch. Since the drain

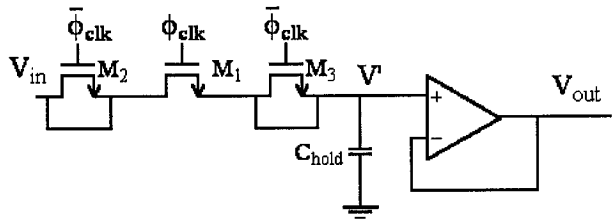


Figure 3.8: Sample-and-hold circuit with two dummy switches

and source terminals of the dummy transistor are connected together, it acts simply as voltage dependent MOS capacitors which couple the drain and source nodes with an inverted gain voltage source [18]. Frequently the dummy is designed half as wide as the sampling switch which results in its parasitic gate capacitance equals to half value of the sampling switch's parasitic gate capacitance. Consequently, perfect cancellation is achieved with the half-width dummy transistors in the following two cases:

* If the impedances on the drain and source side of the switch are identical. This means that the sampling switch pushes exactly half of its stored channel charge into each side, where it can be completely compensated by the dummy transistors.
* If the switching time is in the order of the intrinsic transit time of the switch.

The compensation is guaranteed even for unsymmetrical source and drain impedances, since no carriers flow through the open switch to equalize the potential on both sides.

In all other cases where the switch is still temporarily conductive during the turn-off transient, and equalization of the injected charges may not occur. Therefore, no 1:1 partitioning of the channel charge occurs and half size dummy transistors cannot fully compensate the charge injection. That is to say, in practice, it is difficult to achieve perfect cancellation. Nevertheless, because this sample-and-hold circuit is easily implemented using CMOS technology, requires less area, and has relatively high precision, it has been adopted in our design.

#### 3.2.2.3 The Design Data and Performance of the Sample-and-Hold Circuit

The design data for the proposed sample-and-hold circuit are tabulated in Table 3-3. The design data of the output buffer are given in Section 3.2.3. Table 3-4 provides the schematic simulation results of the proposed sample-and-hold circuit at the different temperatures when the sampled signal is a sinusoidal signal with 15mV magnitude and 10 MHz frequency. Column 2 is the output of the sample-and-hold circuit shown in Figure 3-8 when the two dummy switches are removed. Column 3 is the output of the sample-and-hold circuit shown in Figure 3-8. Comparing column 2 with column 3, one

**Table 3-3 Design Data for the Sample-and-Hold Circuit**

| Transistor | $M_1$ | $M_2$ | $M_3$ | |
|---|---|---|---|---|
| (W/L)* ratio | 1.7/0.72 | 0.78/0.72 | 0.78/0.72 | |
| Power supply (V) | VDD | +1.8 | VSS | -1.8 |
| Hold capacitance (pF) | $C_{hold}$ | 0.5 | | |
| Gate voltage (V) $\phi_{clk}$ | Voltage 1 | 0 | Voltage 2 | 1.8 |
| | Period | 100ns | Pulse wide | 2ns |
| | Delay time | 23ns | Rise/Fall time | 1ns |
| Gate voltage (V) $\overline{\phi_{clk}}$ | Voltage 1 | 0 | Voltage 2 | 1.8 |
| | Period | 100ns | Pulse wide | 96ns |
| | Delay time | 26ns | Rise/Fall time | 1ns |

Note: * W and L are in microns each (L: Length, W: Width).

can find that the hold step is reduced dramatically using the dummy switch compensation technique. From these simulation results, we find that the hold step is about 0.13% of the sampled value at 27°C, and the worst case (at -30°C) hold step is approximately 0.8% of the sampled value. However, the output voltage change of the above OTA across a resistance load over the range of -30°C to 85°C is 59.7% of its output voltage at 27°C. So, the precision of this sample-and-hold circuit is considered good enough for the operation of the overall system.

**Table 3-4 Simulation Results of the Sample-and-Hold circuit**

| Temperature | Output without dummy switches (mV) | Output with dummy switches (mV) |
|---|---|---|
| 85°C | 5.423 | 14.99 |
| 27°C | 5.621 | 15.02 |
| 0°C | 5.739 | 15.06 |
| -30°C | 5.887 | 15.12 |

### 3.2.3 The Operational Amplifier (OP-AMP)

In the negative feedback control system, the sample-and-hold circuit, the nonlinear amplifier, the difference amplifiers and summer are achieved using the OP-AMP. In these blocks, the OP-AMP will process very slowly varying signals, so high bandwidth is not a stringent requirement. The closed-loop offset and output impedance of the OP-AMP should be small. Two further concerns are the voltage gain and the CMR. The voltage gain should be high over the range of –30°C to +85°C, and the negative CMR should be lower than the lowest value of the required $V_g(T)$ as indicated in Figure 3-1. That is to say, the negative CMR should be lower than -0.704V, -0.5V, and -0.245V at -30°C, 27°C, and 85°C, respectively. In Chapter 4, we shall explain the reason for

these requirements. The schematic diagram of the proposed two-stage OP-AMP is shown in Figure 3-9. It consists of four parts: a bias circuit, a differential input stage, a second gain stage, and a class AB output stage. Capacitor $C_c$ is included to ensure stable operation of the OP-AMP under external negative feedback.

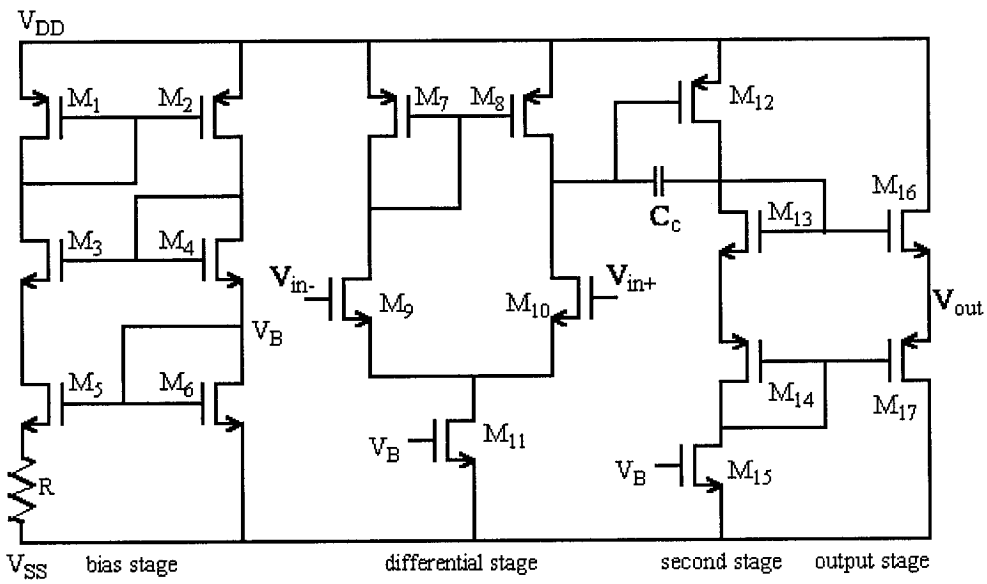


Figure 3-9: Schematic diagram of the OP-AMP

### 3.2.3.1 Bias Circuit Structure

In this system, the OP-AMP must maintain a high gain over a wide range of temperature. To this purpose, the voltage or current references should minimize their dependence on temperature. In the proposed bias circuit, the transconductance of $M_6$ is determined by [2]:

$$g_{m6} = \frac{2\left[1 - \sqrt{\frac{(W/L)_6}{(W/L)_5}}\right]}{R} \qquad (3\text{-}8)$$

So, it depends on geometric ratios only, independent of power-supply voltages, process parameters, temperature, or any other parameters with large variability. For the special case of $(W/L)_5 = 4(W/L)_6$, we have simply

$$g_{m6} = \frac{1}{R} \qquad (3\text{-}9)$$

Note that, not only is $g_{m6}$ stabilized, but all other transconductances are also stabilized since all transistor currents are derived from the same biasing network, and, therefore, the ratios of the currents are mainly dependent on geometry. We thus have, for all n-channel transistors,

$$g_{mi}\big|_{NMOS} = \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_6 I_{D6}}} \times g_{m6} \qquad (3\text{-}10)$$

and for all p-channel transistors

$$g_{mi}\big|_{PMOS} = \sqrt{\frac{\mu_p (W/L)_i I_{Di}}{\mu_n (W/L)_6 I_{D6}}} \times g_{m6} \qquad (3\text{-}11)$$

It should be noted here that the preceding analysis has ignored many second-order effects such as the transistor output impedance and the body effect. The body effect will modify the equation slightly, but the relationship will still depend primarily on geometry alone. The major limitation is due to the transistor output impedance. This effect can be made of little consequence by replacing the simple current mirrors with cascode mirrors.

### 3.2.3.2 Differential Input Stage

The most commonly used input stage for operational amplifiers is a differential input stage. The principal advantages are (1) elimination of common mode signals (such as noise) and (2) reduction of harmonic distortion. In our OP-AMP, the differential input single-ended output stage, as shown in Figure 3-10, consists of a N-channel input pair $M_9$-$M_{10}$ and a current-mirror $M_7$-$M_8$, providing a differential to single-ended conversion.

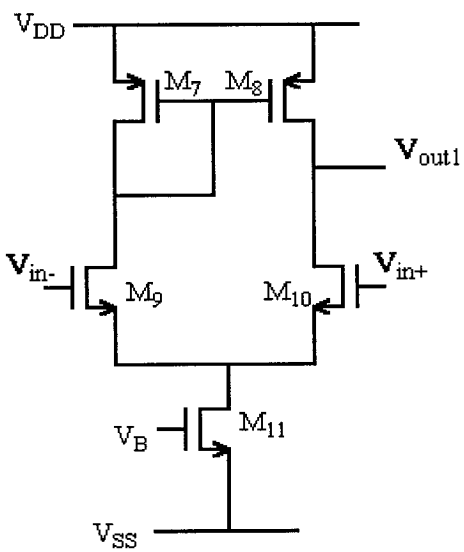


Figure 3-10: A differential input, single-ended-output gain stage

Standard nodal analysis produces the voltage gain at low frequency as (defining the differential input voltage as $v_{in} = v_{in-} - v_{in+}$):

$$A_{v1} = \frac{v_{out1}}{v_{in}} = \frac{g_m}{g_{ds8} + g_{ds10}} \qquad (3\text{-}12)$$

From this expression, the magnitude of the gain depends on the transconductance and output impedance.

### 3.2.3.3 Second Gain Stage

The second stage, as shown in Figure 3-11, appears as a common source amplifier with a PMOS ($M_{12}$) input stage and an NMOS ($M_{15}$) current source load. The uncommon part is the existence of two series connected transistors ($M_{13}$, $M_{14}$), which are configured like active resistors (drain-gate connected).

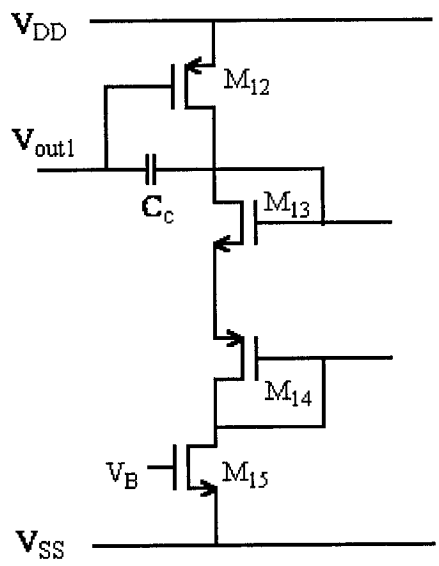


Figure 3-11: The second gain stage

For low frequency analysis one can then consider this stage as a common source amplifier where the load of the PMOS ($M_{12}$) stage is $r_{ds}$ of $M_{15}$ plus the resistances of the drain-gate connected transistors ($M_{13}$, $M_{14}$). The gain of the second stage will then be:

$$A_{v2} = -g_{m12}(r_{12} \| r_{15}) \qquad (3\text{-}13)$$

where $r_{12} = r_{ds12} + \frac{1}{g_{m13}}$ and $r_{15} = r_{ds15} + \frac{1}{g_{m14}}$. For the two-stage OP-AMP, the overall voltage gain is $A_{v1}A_{v2}$.

### 3.2.3.4 Output Stage

An important function of the output stage is to provide the amplifier with a low output resistance so that it can deliver the output signal to the load without loss of gain. The most challenging requirement in the design of the output stage is that it delivers the required amount of power to the load in efficient manner. This requires a high ratio between the maximum signal current that can be delivered to the load and the quiescent current of the output stage.

To reduce any distortion and have reasonably high conversion efficiently, we choose a Class AB output stage. The output stage is shown in Figure 3-12. A bias voltage $V_{BB}$ is applied between the gates of $M_N$ and $M_P$, and provides a small, non-zero quiescent current. In practice, the battery sources are simulated using gate-drain connected MOS

transistors as shown in Figure 3-11. In that figure, $M_{13}$ and $M_{14}$ provide this function. For small $V_{in}$, both MOS transistors conduct, and as $V_{in}$ is increased or decreased, one of the two MOS transistors takes over the operation.

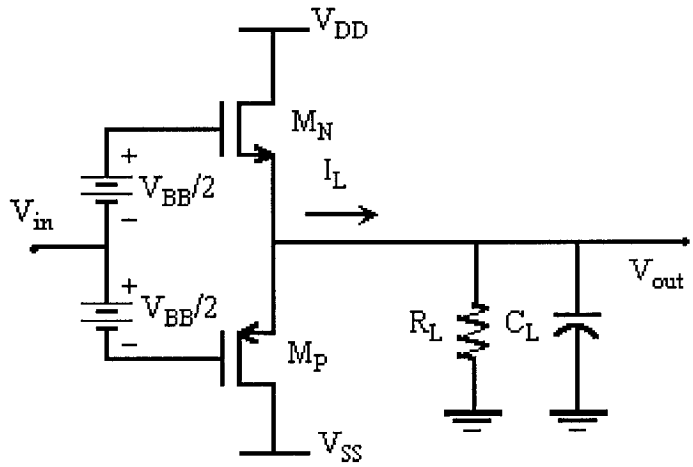


Figure 3-12: Class AB output stage

### 3.2.3.5 Design Data and Performance Parameters of the OP-AMP

The design data and main performance parameters at different temperatures of the OP-AMP are tabulated in Table 3-5 and Table 3-6, respectively. From the data sheet in Table 3-6, one can find the voltage gain, bandwidth, phase margin, and CMR can meet the requirements of the system over the range of temperature variation. However, the output offset voltage can change substantially with temperature variation, thanks to the negative feedback technique, which can absorb this variation in the error control voltage

and make the overall error very small.

**Table 3-5 Design Data for the OP-AMP**

| | | | | |
|---|---|---|---|---|
| Transistor (W/L) * ratio | $M_1$ and $M_2$ | $M_3$ and $M_4$ | $M_5$ | $M_6$ |
| | 0.88/0.87 | 0.88/6.679 | 8.968/0.72 | 2.242/0.72 |
| | $M_7$ and $M_8$ | $M_9$ and $M_{10}$ | $M_{11}$ | $M_{12}$ |
| | 4.372/1.2 | 0.88/3.12 | 2.236/0.72 | 12.898/0.72 |
| | $M_{13}$ | $M_{14}$ | $M_{15}$ | $M_{16}$ |
| | 27.036/0.72 | 86.78/0.72 | 12.023/2.00 | 25.38/0.72 |
| | $M_{17}$ | | | |
| | 82.4/0.72 | | | |
| Power supply (V) | VDD | +1.8 | VSS | -1.8 |
| Compensation-C (pF) | $C_c$ | 1 | | |
| Resistor (kΩ) | R | 4.583 | | |

Note: * W and L are in microns each (L: Length, W: Width).

**Table 3-6 Performance Parameters of the OP-AMP**

| Parameter | Value | | | | Unit |
|---|---|---|---|---|---|
| | -30°C | 0°C | 27°C | 85°C | |
| Voltage gain | 69.92 | 75.55 | 74.85 | 70.25 | dB |
| Unity gain bandwidth | 5.384 | 5.142 | 4.851 | 4.183 | MHz |
| Phase margin | 79.1 | 79.3 | 79.4 | 80.35 | deg |
| Positive CMR | 0.55 | 0.63 | 0.7 | 0.86 | V |
| Negative CMR | -0.73 | -0.66 | -0.64 | -0.48 | V |
| Output resistance | 553.4 | 561.1 | 570.1 | 592.8 | Ω |
| Output offset voltage | -405.3 | -183.7 | 5.53 | 310.2 | mV |
| Power dissipation | 0.379 | 0.411 | 0.434 | 0.470 | mW |

### 3.2.4 Nonlinear Amplifier

The OP-AMP is applied to realize the nonlinear amplifier, the difference amplifier, summer, and voltage follower in the slave subsystem. For the configurations of difference amplifier, summer, and voltage follower, one can refer to [19]. This section will concentrate on the configuration of nonlinear amplifier.

Since the temperature dependent control voltage $V_g(T)$ is a nonlinear function of

T, a nonlinear device is included in the whole control system. The nonlinear amplifier is shown in Figure 3-13. An NMOS transistor M is applied to realize a feedback resistor, and is biased in the triode region. The classical model equation for an n-channel transistor operating in the triode region is given by:

$$I_d = K(T)\left(\frac{W}{L}\right)\left[(V_{gs} - V_{th}(T))V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad V_{ds} < V_{gs} - V_{th} \quad (3\text{-}14)$$

If a small drain-source voltage, $V_{ds}$, is used, we can model the resistance of the transistor by the equation:

$$r_{ds} = \left(\frac{\partial i_d}{\partial V_{ds}}\right)^{-1} \quad (3\text{-}15)$$

which results in a small-signal resistance of

$$r_{ds} = \frac{1}{K(T)\left(\frac{W}{L}\right)(V_{gs} - V_{th}(T) - V_{ds})} \quad (3\text{-}16)$$

Thus, the gain of the amplifier is given by:

$$A'(T) = -\frac{r_{ds}}{R_3} = -\frac{L/W}{K(T)R_3(V_{gs} - V_{th}(T) - V_{ds})} \quad (3\text{-}17)$$

From the above equation, one can see that the gain of this nonlinear amplifier is a nonlinear function of temperature.

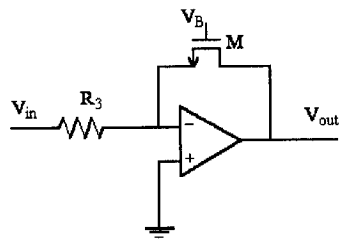


Figure 3-13: Nonlinear gain amplifier

## 3.3 Overall Control Mechanism

After having presented the various blocks of the overall control system in Section 3.2 of this chapter, we are in a better position to explain the mechanism by which the transconductance ($g_m$) is controlled as the temperature changes. The control system includes two forward paths and one feedback path as shown in Figure 3-1. Assume that the two OTAs in slave subsystem are driven by the same sinusoidal signal with small amplitude $V_s$. The signals developed across the two resistors $R_1$ and $R_2$ (each equal to R, say) at the output of the OTAs are, respectively:

$$V_{R1}(T) = g_m(T)\,|_{V_g(T_0)} V_s R \qquad (3\text{-}18)$$

$$V_{R2}(T) = g_m(T)\,|_{V_g(T)} V_s R \qquad (3\text{-}19)$$

The resistance of R is assumed small compared with the output resistance of the OTAs. These two resistors will be placed outside of the chip, so we can choose resistances with low temperature sensitivity (small temperature coefficient of resistance). Therefore, we assume that the change in R is small over the temperature range. This assumption is not critical for success of the method, but it will keep the mathematical expressions simpler. Assume that

$$V_{ref}(T_0) = g_m(T_0)\,|_{V_g(T_0)} V_s R \qquad (3\text{-}20)$$

For the upper forward path, the error $E_1(T)$ is given by:

$$E_1(T) = V_{R1}(T) - V_{ref}(T_0)$$
$$= V_s R \sqrt{\frac{W_4 W_5}{2L_4 L_5}} \left[ K(T)\left(V_g(T_0) - V_{ss} - V_{th}(T)\right) - K(T_0)\left(V_g(T_0) - V_{ss} - V_{th}(T_0)\right) \right] \quad (3\text{-}21)$$

The error $E_1$ will be zero at $T=T_0$ (i.e., =27°C, say). Since the slave OTA#2 needs to furnish the nominal $g_m$, i.e., $g_m(T_0)$, a bias voltage $V_g(T_0)$ is employed in summer#2 to maintain this condition at $T=T_0$. This will render $E_2=0$ at $T=T_0$. When the temperature will change from $T_0$, the error $E_1$ will assume non-zero value and produce the correction voltage $\Delta V_g(T)$. This correction voltage, together with $V_g(T_0)$ will produce $V_g(T)$ at the output of summer#2. The resulting $V_g(T)$ should in principle be same as that given in equation(2-12) and will be able to maintain $g_m(T)=g_m(T_0)$ for the slave OTA#2. As a consequence, we can see that $E_2$ will remain close to zero. If for some reason $E_2$ departs substantially from zero (making $g_m(T)$ similarly different from $g_m(T_0)$), the two error voltages $E_1$ and $E_2$ will combine to change $\Delta V_g(T)$ substantially to force $E_2$ to become close to zero again.

The above scenario also justifies the requirement of two error voltages $E_1$ and $E_2$ in the system. If only OTA#1 were used with $V_g(T)$ fed to OTA#1, the error voltage $E_1$ will alternately swing between zero and some finite value at each temperature T not equal to $T_0$. For any such temperature, as $V_g(T)$ assumes the value according to equation(2-12), the voltage $V_{R1}$ and $V_{ref}$ will become equal, rendering $E_1$ to zero value. This situation will thus bring up an oscillatory phenomenon in the control system and is not desired especially because a steady $g_m$ equal to $g_m(T_0)$ is required for all the time at any

temperature. Since at a fixed temperature $E_1$ provides a steady control voltage, this will be termed as the static component of the error. Similarly, $E_2$ will be termed as the dynamic component of the error voltage. The dynamic error voltage is given by:

$$\begin{aligned} E_2(T) &= V_{R2}(T) - V_{ref}(T_0) \\ &= V_s R \sqrt{\frac{W_4 W_5}{2L_4 L_5}} \left[ K(T)\left(V_g(T) - V_{ss} - V_{th}(T)\right) - K(T_0)\left(V_g(T_0) - V_{ss} - V_{th}(T_0)\right) \right] \end{aligned} \tag{3-22}$$

Consider the following nonlinear processing to achieve $V_g(T)$:

$$V_g(T) = A(T)\left(E_1(T) + BE_2(T)\right) + C \tag{3-23}$$

Where, A(T) is a temperature dependent voltage gain, B is a constant gain, and C is a DC offset voltage. When the dynamic error $E_2(T)$ approaches zero, we can get:

$$V_g(T) = A(T)E_1(T) + C \tag{3-24}$$

On setting $C = V_g(T_0)$ and substituting equations (2-12) and (3-21) into (3-24), we get:

$$A(T) = -\frac{1}{K(T)V_s R \sqrt{\frac{W_4 W_5}{2L_4 L_5}}} \tag{3-25}$$

From this formula, we see the voltage gain of A(T) is a nonlinear function of T. Comparing (3-25) with (3-17), one can match A(T) and A'(T) as close as possible by adjusting the size of the NMOS transistor M, the value of resistor $R_3$, and its gate voltage in Figure 3-13. So this temperature dependent voltage gain can be achieved approximately using a nonlinear amplifier shown in Figure 3-13.

When the dynamic error $E_2(T)$ is not equal to zero, the dynamic correction term A(T)B $E_2(T)$ is added to feedback voltage $V_g(T)$ to speed up the process of rendering

$g_m(T)$ approach $g_m(T_0)$. Since both $E_1(T)$ and $E_2(T)$ have similar expressions (see equation (3-22) and (3-21)), it may be convenient to process the two error signals through a common nonlinear amplifier as shown in Figure 3-1. Figure 3-14 illustrates the nature of variations of $E_1(T)$ and $E_2(T)$ during a control cycle when the environment temperature is at -30°C.

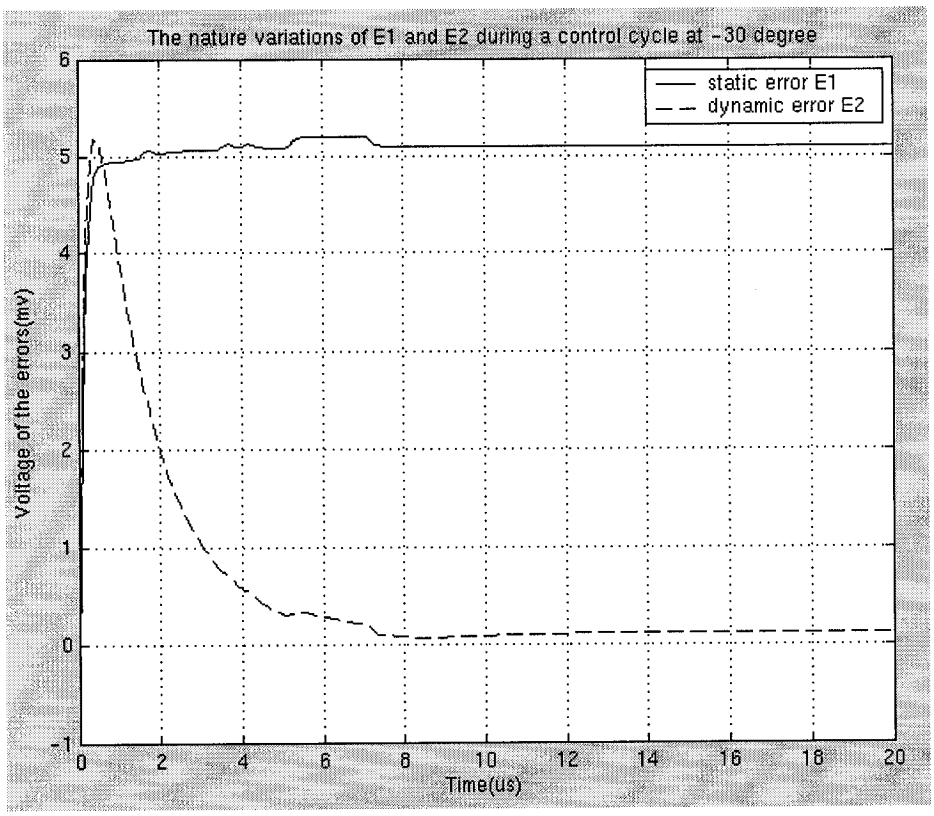


Figure 3-14: The nature of variations of $E_1(T)$ and $E_2(T)$ during a control cycle at -30°C

The above analysis explains how the variation of the transconductance of the slave-OTA#2 over the temperature range will be stabilized using this control circuit. If

the $V_g(T)$ terminal of slave-OTA#2 and the master OTAs are made common, the $g_m$ values of the master OTAs will become similarly invariant with temperature changes. Then the filter characteristics dependent upon the $g_m$ of the master OTAs will remain unaltered despite temperature variations. We have assumed that all the OTAs in the master subsystem are of same $g_m$ value.

When the filter characteristics depend on several distinct $g_m$ values, ideally, the slave subsystem has to be replicated to stabilize each of these $g_m$ values against temperature variations because $V_g(T)$ depends on both temperature and the size of transistors in the OTA. However, since temperature effect is a dominant one, from the point of view of engineering, we can apply one slave subsystem to adjust the different $g_m$ values against temperature variation.

## 3.4 Summary

This chapter introduces a novel technique using simple negative feedback to stabilize the transconductance gain of an OTA over the range of –30°C to +85°C. The block diagram of the whole system is described, and each basic building block is analyzed in detail. The design data for every block are tabulated in this chapter. Finally, the overall control mechanism against temperature variation is provided.

# Chapter 4

# System Implementation and Simulation Results

Chapter 3 provided the block diagram of the control system for stabilizing the transconductance gain of an OTA. There, we provided theoretical analysis and conceptual insight pertaining to the overall control mechanism. The detailed circuits for the slave subsystem have been described. In this chapter, the case of implementation of the system as shown in Figure 3-1 based on TSMC 0.18 μm technology is addressed. It is a one-poly-six-metal CMOS technological process. In Section 4.1, we present implementation methods for big resistors and capacitors in this technology, and consider the layout techniques in order to minimize the side effects of transistor pair mismatch and parasitics. Then, in Section 4.2, the results of numerical simulation of the proposed control strategy are presented to validate the theoretical predictions. Finally, pre and post layout simulation results are provided in Section 4.3.

## 4.1 Physical Design

The schematic diagram of the slave subsystem is shown in Figure 4-1. OA#1, OA#2 and OA#3 realize three voltage followers for three sample-and-hold blocks. Comparing Figure 4-1 with Figure 3-1 (it is included here again), OA#4, OA#5 and resistors $R_5$ constitute the difference amplifier #1 and #2. The summer #1 and the

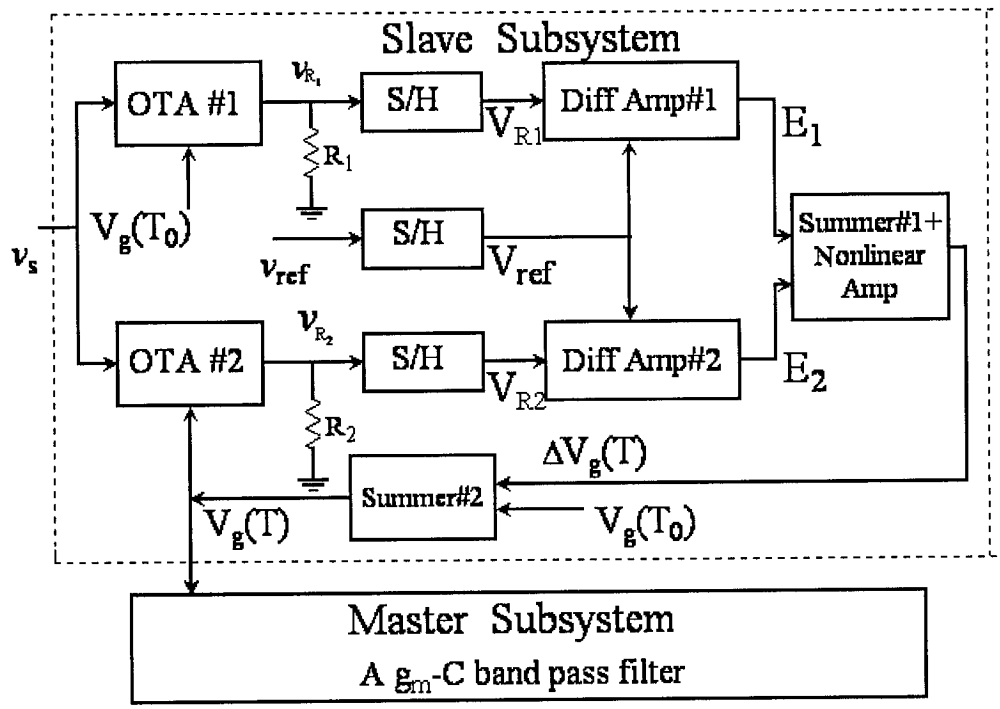


Figure 3-1: The block diagram of the control system

nonlinear amplifier are implemented by OA#6, resistors $R_3$, $R_4$ and NMOS transistor M. OA#7 and resistors $R_6$ produce summer #2. The inverter implemented by OA#8 makes

the polarity of the control voltage $V_{control}$ meet the requirement, and the control voltage $V_{control}$ is connected to the $V_g$ terminals of the OTAs in master subsystem. The design data of the components in Figure 4-1 are tabulated in Table 4-1. The gate voltages of the sample-and-hold circuit are same as the gate voltages cited earlier in Table 3-3. Resistors $R_1$, $R_2$, $R_3$ and $R_4$ are outside of the fabricated chip, and are replaced by high-precision resistors to reduce the effect of temperature variation on the resistance.

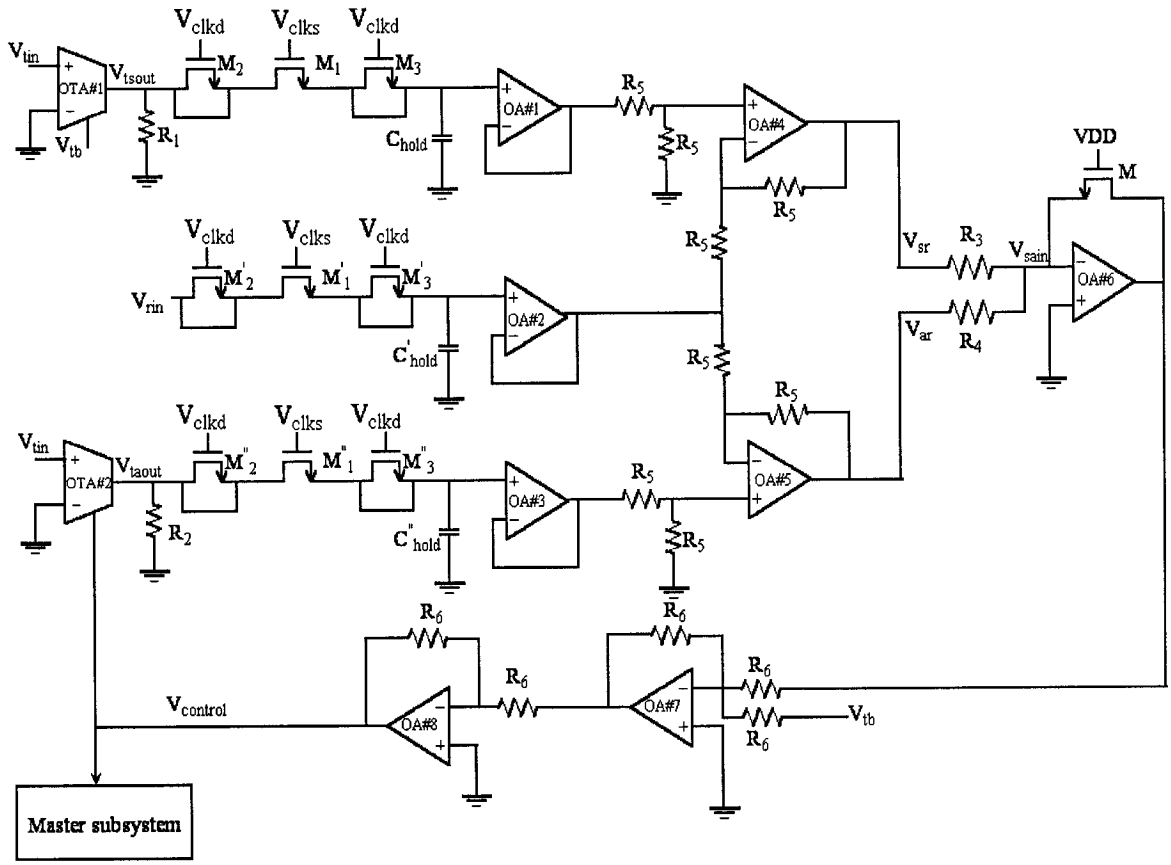


Figure 4-1: Schematic of the slave subsystem

**Table 4-1 Design Data for Slave Subsystem**

| Transistor | $M_1$, $M_1'$, and $M_1''$ | $M_2/M_2''$ | $M_2'$ | M |
|---|---|---|---|---|
| (W/L)* ratio | 1.7/0.72 | 0.85/0.72 | 0.87/0.72 | 0.88/5.65 |
| Power supply (V) | VDD | +1.8 | VSS | -1.8 |
| Input Voltage (V) | $V_{tin}$ | 50mV/10MHz | $V_{rin}$ | 15mV/10MHz |
| Bias Voltage (V) | $V_{tb}$ | -0.5 | $V_{opb}$ | -1.15 |
| Hold Capacitor (pF) | $C_{hold}$ | 0.5 | | |
| Resistor (kΩ) | $R_1/R_2$ | 1 | R3 | 0.5 |
| | $R_4$ | 2 | $R_5$ | 2 |
| | $R_6$ | 60 | | |

Note: * W and L are in microns each (L: Length, W: Width).

In Table 4-1, we see that the slave subsystem includes high valued resistors, and some of them are required to match with each other. In addition, in the master subsystem, there are few big capacitors (i.e., 5 pF).

The following sections will introduce the implementation consideration for big resistors and capacitors and some layout techniques that reduce the sources of noise and errors in the fabricated circuit. These strategies include the common-centroid layout for the differential pair to minimize mismatching effects; large size transistors are done in

fingered style to reduce the junction capacitance; capacitors and resistors are arranged in N-Well and shielded with VDD-ring to minimize the interference from substrate noise.

### 4.1.1 Matching and Noise Considerations

To realize high-quality analog circuits, one should consider several important layout issues. These issues can be broadly divided into two categories—matching and noise.

When integrated components are realized using lithographic techniques, a variety of two-dimensional effects can cause the effective sizes of the components to differ from the sizes of the glass layout masks [2]. Some examples of these effects are illustrated in Figure 4-2. For example, Figure 4-2 (a) shows how an effective well area will typically

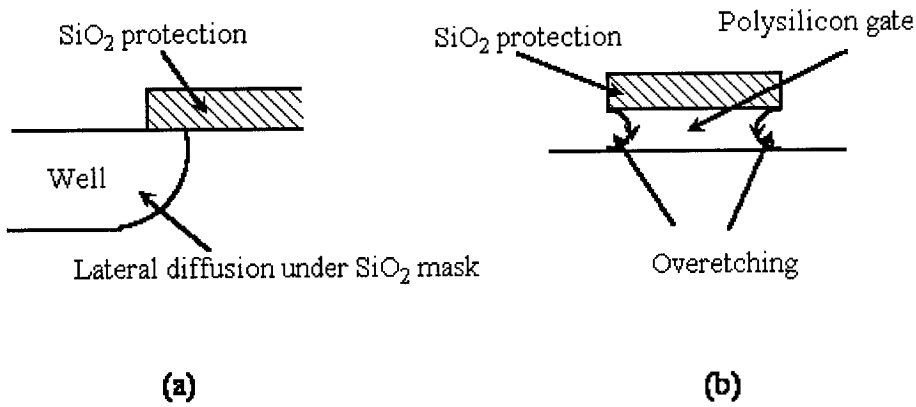


Figure 4-2: Two-dimensional effects causing sizes of realized microcircuit components to differ from sizes of layout masks

be larger than its mask due to the lateral diffusion that occurs not just during ion implantation but also at a later stage, such as annealing. Another effect, known as overetching, occurs when layers such as polysilicon or metal are being etched. Figure 4-2 (b) shows overetching that occurs under the $SiO_2$ protective layer at the polysilicon edges and causes the transistor polysilicon layer to be smaller than the corresponding mask layout. The examples shown illustrate typical sizing effects, but many other second-order effects influence the realized component sizes. These other effects include those caused by boundary conditions of an object, the size of the opening in a protective layout through which etching occurs, and the unevenness of the surface of the microcircuit. For these reasons, the absolute sizes of microcircuit components can seldom be accurately determined. Matching second-order size error effects is done mainly by making larger objects out of several unit-sized components connected together. Also, for best accuracy, the boundary conditions around all objects should be matched, even when this means adding extra unused components; objects to be matched should be placed next to one another because of the spatial variation in the process parameters.

Some layout issues help minimize noise in analog circuits [2]. Most of these issues either attempt to minimize noise from adjacent digital circuits getting coupled to the substrate or analog power supplies, or try to minimize substrate noise that affects analog circuits.

In the slave subsystem, the sample-and-hold circuits include clock signals. NWELL shields are placed under the clock lines to minimize substrate noise. In addition, the circuits with the clock signals should be placed as far from the analog circuits as possible to prevent the switching noise from affecting the analog circuitry.

### 4.1.2 Transistor Layout

The OTA and the OP-AMP we used in this system contain common source differential pairs that are needed to match precisely. To minimize large errors caused by gradient effects across a microcircuit, such as the temperature or the gate-oxide thickness changing across the microcircuit, the differential common source pairs are realized using common-centroid layout technique [2]. An example of a common-centroid layout of two identical matched transistors whose sources are connected is shown in Figure 4-3.

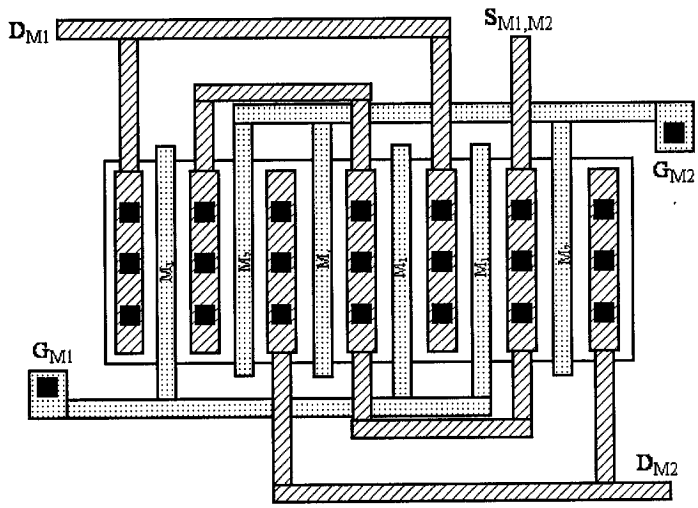


Figure 4-3: A common-centroid layout for a common source differential pair

For the layout of larger transistors in this system, we use several smaller transistors connected in parallel like fingers. A simplified layout illustrating this approach is shown in Figure 4-4 [2], where four transistors that have a common gate and share drain and source junctions are connected in parallel. This reduces the parasitic junction capacitances of the transistors, which are quite critical for high frequency operations.

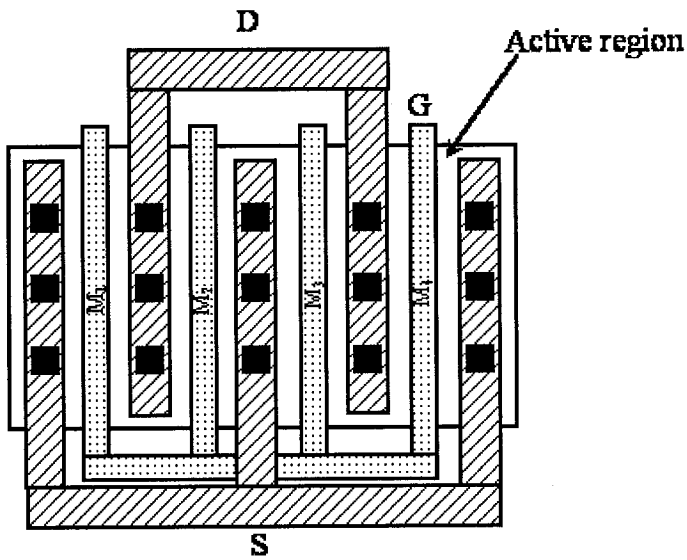


Figure 4-4: A fingered transistor

### 4.1.3 MiM Capacitor

The capacitors are realized using MiM capacitor in 0.18 μm CMOS technological process from TSMC. The metal to metal capacitor can be processed by CTM (Capacitor Top Metal Definition) to Metal 5, where the CTM layer is an additional layer between the

top two metal layers. The CTM layer is an optional layer forming the top plate for the MiM capacitor. If a system does not require a MiM capacitor, we simply ignore this layer. An example of the cross-section of a MiM capacitor is shown in Figure 4-5. Figure 4-6 displays a sample of the capacitor layout view. An N-Well with a VDD-ring, as shown in Figure 4-6, is placed under the MiM capacitor to minimize the noise interference from the common substrate. The shielding of the bottom plate is especially important because the coupling into the substrate from any interfering circuits can cause excursions of the voltage on the bottom plate [22].

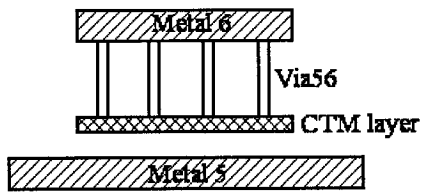


Figure 4-5: An example of the cross-section of a MiM capacitor

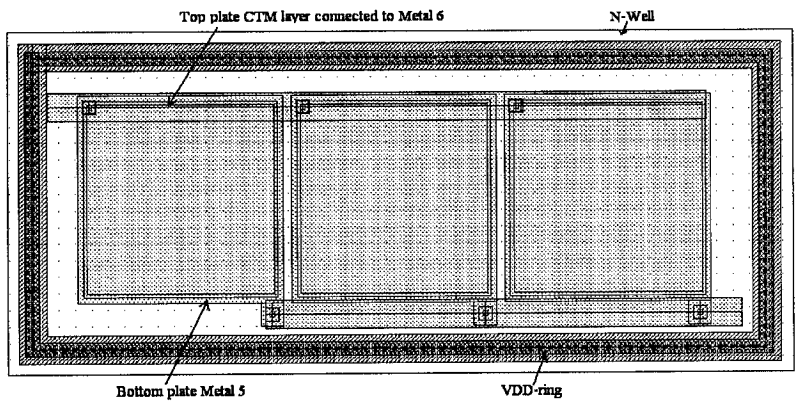


Figure 4-6: A MiM capacitor layout diagram

### 4.1.4 N+ non-silicided poly Resistor

Integrated resistors can be realized using a wide variety of materials. A popular choice is polysilicon. Other choices include diffused or ion-implanted regions such as junctions, wells, or base regions. TSMC 0.18 μm CMOS technological process provides P+ non-silicided and N+ non-silicided polysilicon to implement large resistors. Their sheet resistances can reach 341Ω/sq and 278Ω/sq [23], respectively. For example, for a resistor of 60 KΩ, it includes around 216 squares. Although the tolerance of any particular integrated resistor is relatively poor (±30%), the tracking between matched pairs of integrated resistors is excellent (±1%) [24]. In our system, the integrated resistors $R_5$ and $R_6$ are all matched pair as shown in Figure 4-1.

In order to realize a more accurate, but larger, resistor ratio which can be expressed as a ratio of integer values, we use the layout architecture as shown in Figure 4-7 [2]. The resistor consists of several fingers connected at their ends using

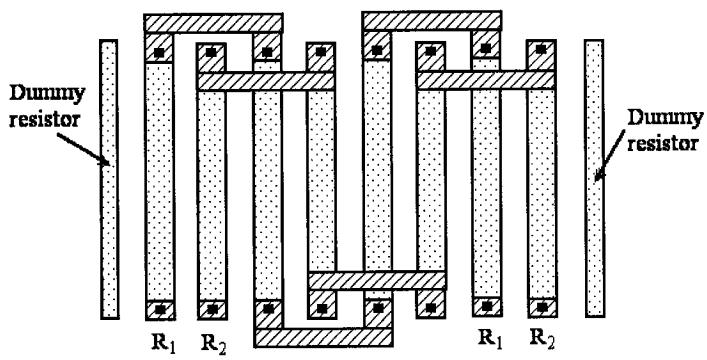


Figure 4-7: A layout for a more accurate and larger resistor pair

low-resistivity metal. This approach matches errors caused by the contact impedance between $R_1$ and $R_2$. Also, two dummy fingers have been included to match boundary conditions. In our system, all matched resistor pairs use the architecture shown in Figure 4-7. Because these resistors are implemented using N+ non-silicided polysilicon, the resistors are arranged in N-Well. The N-Well shielded with VDD-ring can minimize the interference from substrate noise.

### 4.1.5 The Whole System Layout

As mentioned in Chapter 2, the second-order $g_m$-C band-pass filter as the master subsystem is built in the fabricated chip to validate the proposed negative feedback technique. Figure 4-8 shows the layout of the filter chip with all control circuitry based on TSMC 0.18 μm CMOS technological process. The whole die area is 1 $mm^2$ inclusive of the pad frame.

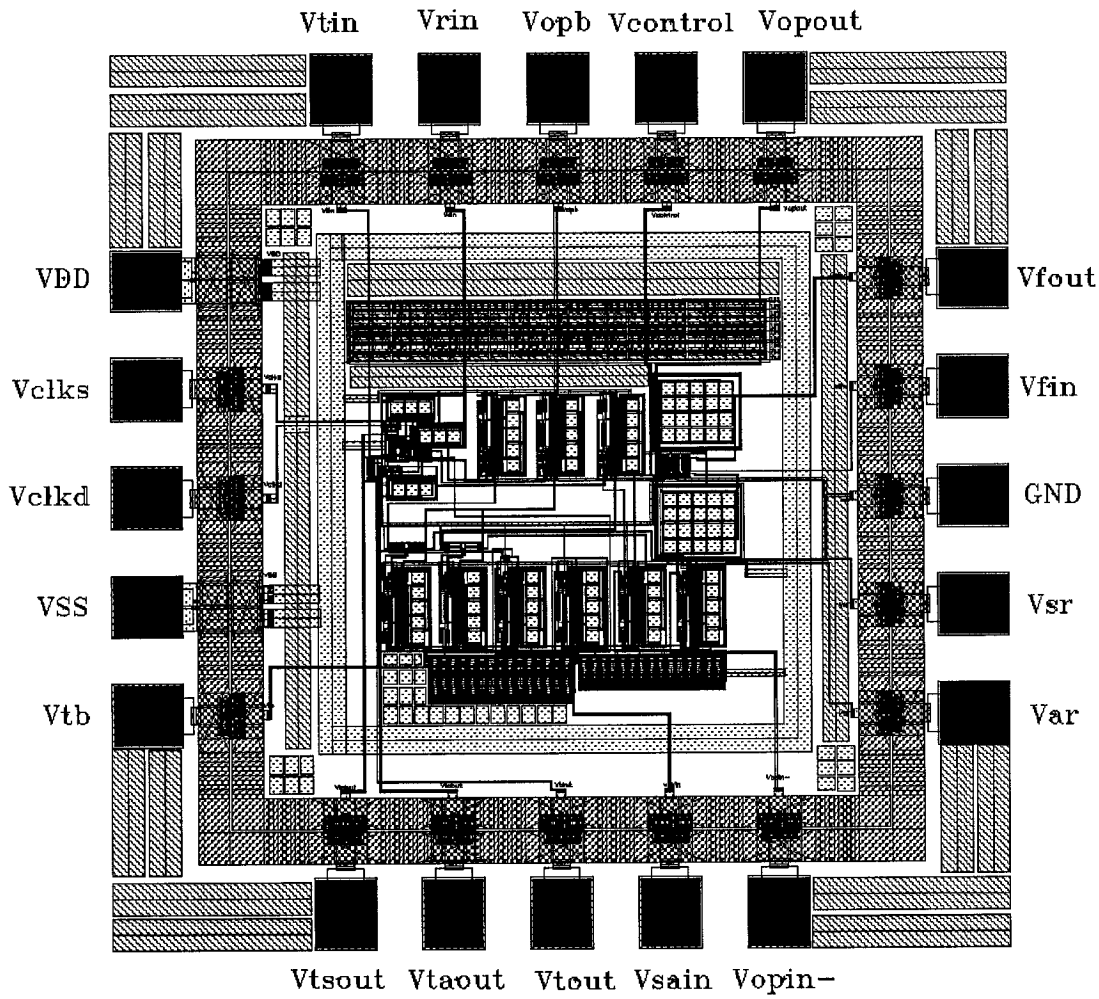


Figure 4-8: The layout view of the whole system

## 4.2 Numerical Simulation

In order to verify the proposed control strategy, a numerical simulation using MATLAB tools is done, based on the theoretical analysis in Chapter 3. Substituting equations (2-4) and (2-5) into (2-12), we get the expression of the required control

voltage $V_g(T)$:

$$V_g(T)=\left(\frac{T}{T_0}\right)^{-n}\left(V_g(T_0)-V_{ss}-V_{th}(T_0)\right)+V_{ss}+V_{th}(T_0)+\alpha\left(\frac{T}{T_0}-1\right) \qquad (4\text{-}1)$$

If we replace all parameters in (4-1) by actual circuit values based on TSMC 0.18 μm CMOS technology (which are tabulated in Table 4-2) and the temperature T is in Kelvins (absolute), equation (4-1) changes to:

$$V_g(T)=\left(\frac{T}{300}\right)^{1.59}\times 0.862-1.362-0.225\left(\frac{T}{300}-1\right) \qquad (4\text{-}2)$$

The relevant parameters of the TSMC process are shown in Table 4.2. From the equations (2-4), (2-5), (3-17) and (3-24), the actual control voltage at the different temperatures using the proposed feedback technique is derived as:

$$\begin{aligned} V_g'(T) &= A'(T)E_1(T)+C \\ &= -\frac{V_g(T_0)-V_{ss}-V_{th}(T_0)-\alpha\left(\frac{T}{T_0}-1\right)-\left(\frac{T}{T_0}\right)^{-n}\left(V_g(T_0)-V_{ss}-V_{th}(T_0)\right)}{V_{gs}-V_{th}'(T_0)-\alpha\left(\frac{T}{T_0}-1\right)-V_{ds}} \\ &\quad \times V_s\frac{RL}{R_3W}\sqrt{\frac{W_4W_5}{2L_4L_5}}+V_g(T_0) \end{aligned} \qquad (4\text{-}3)$$

Where $V_{gs}$, $V_{th}'(T_0)$ and $V_{ds}$ are relative to the transistor M in Figure 3-13 (page 58), and $V_{th}'(T_0)$ is threshold voltage considering body effect. Similarly, taking actual circuit values in Table 4-2 for all parameters in (4-3), the practical control voltage can be given by:

$$V_g'(T) = -0.906 \times \frac{0.637 + 7.50\times10^{-4} - 0.862\left(\frac{T}{300}\right)^{1.59}}{0.75 + 7.5\times10^{-4}T} \qquad (4\text{-}4)$$

The numerical simulation results according to the equations (4-2) and (4-4) from -30°C to 100°C using MATLAB are shown in Figure 4-9. There is very little disparity between $V_g(T)$ and $V_g'(T)$. That is to say, the numerical simulation results prove the potential of the proposed control strategy towards stabilizing the $g_m$ values against temperature variation.

**Table 4-2 Values of the Transistors and Other Parameters in TSMC 0.18 μm CMOS Technology**

| | | | | | |
|---|---|---|---|---|---|
| n | -1.59 | $V_{th}(T_0)$ | 0.438 V | $R_3$ | 0.5 kΩ |
| α | -0.225 | $V_s$ | 0.05 V | R | 1 kΩ |
| $T_0$ | 300 K | $V_{gs}$ | 1.8 V | (W/L)* | 1.4/2.88 |
| $V_{ss}$ | -1.8 V | $V_{th}'(T_0)$ | 0.825 V | $(W_4/L_4)$* | 11.39/1.44 |
| $V_g(T_0)$ | -0.5 V | $V_{ds}$ | 0 V | $(W_5/L_5)$* | 1.4/2.88 |

Note: * W and L are in microns each (L: Length, W: Width).

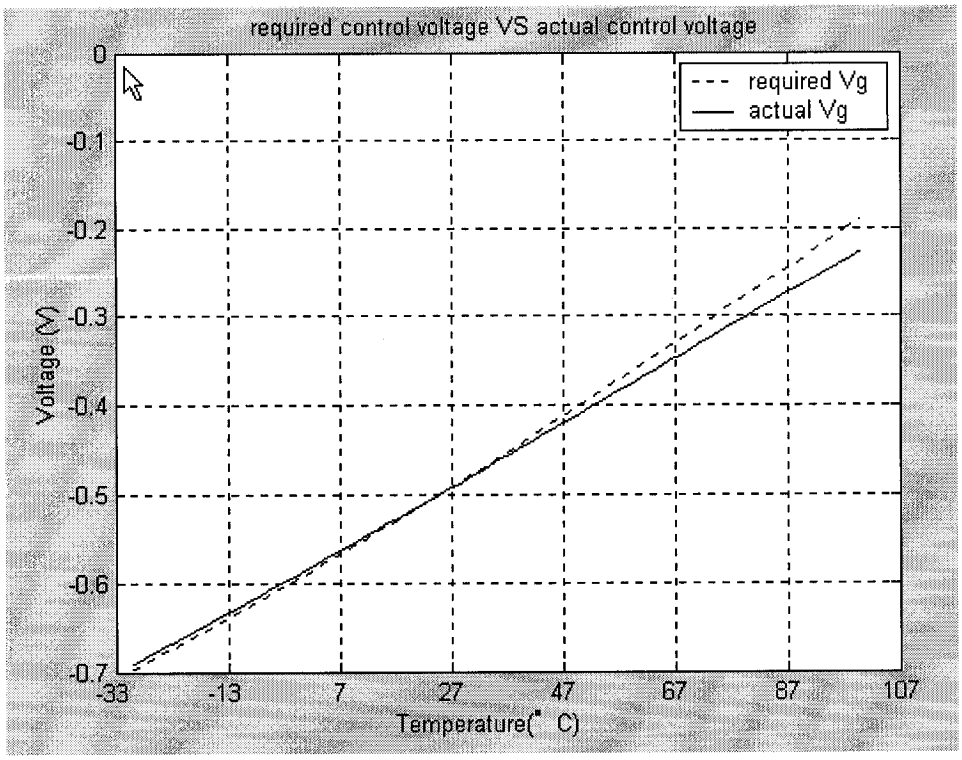


Figure 4-9: Numerical simulation of equations (4-2) and (4-4)

## 4.3 Network Simulation

The following subsections summarize the post layout simulation results of the transconductance of the OTA and the characteristics of the fabricated filter chip with the control system. In order to verify the feedback control strategy further, the pre layout simulation results for low-pass and notch filters with the architecture of a general biquad $g_m$-C filter as shown in Chapter 2 are demonstrated. The simulation is done using Spectre simulator under Cadence environment based on the TSMC 0.18 μm CMOS technology. The MOS device models are typical model (TT model) for both NMOS and PMOS in

level 49.

### 4.3.1 Results for the Transconductance ($g_m$) of the OTA and the Slave Subsystem

The test bench of measuring transconductance gain of the OTA is shown in Fig 4-10. The AC analysis is conducted using an ac input signal of amplitude of 1V, fed in $V_{in+}$ terminal. The output voltage response at the output terminal is same as the output current response because the output of the OTA is terminated in a resistor of 1Ω. In fact, the output current is the transconductance gain of the OTA.

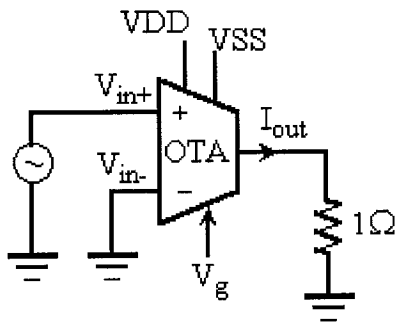


Figure 4-10: Test bench for the transconductance gain of OTA

In order to ensure the correct transconductance gain ($g_m$) of the OTA with the negative feedback control system at different temperatures, we should get the control voltage $V_g$ ($V_{control}$) at different temperatures through testing the slave subsystem. The test

bench of the slave subsystem for control voltage $V_{control}$ ($V_g$) is shown in Figure 4-11. The definitions of terminals are same as that of Figure 4-1.

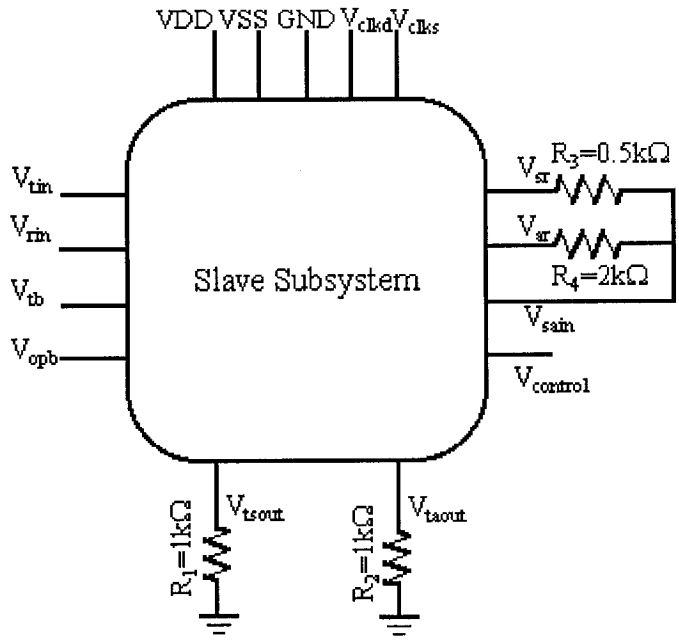


Figure 4-11: Test bench of slave subsystem

The simulation results for the proposed common source differential pair OTA ($g_m$=314 μ mhos) are summarized in Table 4-3. In Table 4-3, column 1 shows the temperature range of investigation. Column 2 shows the transconductance ($g_m$) variation of the OTA in absence of feedback as the temperature changes while $V_g$ is held at a fixed value of –0.5 volts. Column 3 presents the $V_g$ values that will be required to hold the $g_m$ constant at the nominal value at the room temperature (i.e., 314 μ mhos at 27°C). Column 4 shows the values of $V_g(T)$ achieved in closed loop, and these values are extremely close

to the desired values as shown in column 3. Column 5 shows the $g_m$ value achieved in closed loop condition at the different temperatures. The $V_g(T)$ values in column 4 are used to the control terminals of the OTAs in master subsystem. The values in column 5 display that by employing the proposed control scheme the variation in $g_m$ has been reduced from 61.8% to 2.4% over the range of –30°C to +85°C.

**Table 4-3 Simulation Results for the OTA and Slave Subsystem**

| Temperature | $g_m$(μ mhos) $V_g$ fixed | Desired $V_g$(mV) | Practical $V_g$(mV) | $g_m$(μ mhos) $V_g$ tuned |
|---|---|---|---|---|
| -30°C | 438.5 | -704 | -690.6 | 322.8 |
| 0°C | 364.4 | -604 | -600.7 | 315.1 |
| 27°C | 314 | -500 | -497.6 | 315 |
| 85°C | 244.3 | -245 | -247 | 315.2 |

### 4.3.2 Characteristics of the Control Voltages for OTAs with Different Transconductance Gains

In this section, we shall address the question if only one slave subsystem, as discussed so far, could be effective to control several different values of transconductance gain of different OTAs. Simulation results will be presented to establish the case.

To investigate this matter, four OTAs with four distinct transconductance gains are built using the same architecture as shown in Figure 2-3. In order to be used in the same $g_m$-C filter, all OTAs must have the same input and output DC quiescent points. Furthermore, we keep the DC quiescent points of all these OTAs same as the reference (as in Figure 2-3) OTA. The design data for the five different OTAs including the reference OTA are shown in Table 4-4.

For convenience, the expressions of control voltage $V_g(T)$ and related factors as derived in Chapter 2, are rewritten below,

$$V_g(T) = \frac{K(T_0)(V_g(T_0) - V_{ss} - V_{th}(T_0))}{K(T)} + V_{ss} + V_{th}(T) \qquad (4\text{-}5)$$

And

$$K(T) = K(T_0)\left(\frac{T}{T_0}\right)^n \qquad (4\text{-}6)$$

$$V_{th}(T) = V_{th}(T_0) + \alpha\left(\frac{T}{T_0} - 1\right) \qquad (4\text{-}7)$$

Here the exponent n is between -1.09 and –2.17 dependent on the size of an NMOS transistor based on TSMC 0.18 μm process. The value of α is between –0.20 and –0.24 dependent on the size of a NMOS transistor based on TSMC 0.18 μm technology. Table 4-5 shows the desired control voltages at different temperatures for the different OTAs. The $V_g$ values in this table are required control voltages to hold the respective $g_m$ values constant at different temperatures.

**Table 4-4 Design Data of OTAs with Five Distinct Transconductance ($g_m$) Values**

| Transconductance gain of OTA (at 27°C) | Transistor (W/L)* ratio | | |
|---|---|---|---|
| $g_m$=78 μ mhos | $M_1$ and $M_2$ | $M_3$ and $M_4$ | $M_5$ |
| | 2.963/1.44 | 0.95/6.32 | 1.4/11.9 |
| $g_m$=157 μ mhos | $M_1$ and $M_2$ | $M_3$ and $M_4$ | $M_5$ |
| | 5.76/1.44 | 0.95/3.045 | 1.4/5.84 |
| **$g_m$=314 μ mhos | $M_1$ and $M_2$ | $M_3$ and $M_4$ | $M_5$ |
| | 11.39/1.44 | 0.95/1.44 | 1.4/2.88 |
| $g_m$=628 μ mhos | $M_1$ and $M_2$ | $M_3$ and $M_4$ | $M_5$ |
| | 23.35/1.44 | 1.832/1.44 | 1.4/1.41 |
| $g_m$=1256 μ mhos | $M_1$ and $M_2$ | $M_3$ and $M_4$ | $M_5$ |
| | 23.35/0.672 | 3.44/1.44 | 2.61/1.41 |

Note: * W and L are in microns each (L: Length, W: Width).

** Reference OTA

In Table 4-5, column 1 shows the temperature range of investigation. Columns 2, 3, 4, 5, and 6 present the $V_g$ values that will be required to hold $g_m$ constant (i.e., equal to the respective value at 27°C) at different temperatures. Comparing column 4 with

**Table 4-5 Control Voltages for Different OTAs at Different Temperatures**

| T | Desired $V_g$ (mV) ($g_m$=78μ @27°C) | Desired $V_g$ (mV) ($g_m$=157μ @27°C) | Desired $V_g$ (mV) ($g_m$=314μ @27°C) | Desired $V_g$ (mV) ($g_m$=628μ @27°C) | Desired $V_g$ (mV) ($g_m$=1256μ @27°C) | Practical $V_g$(mV) (depending on $g_m$=314μ @27°C) |
|---|---|---|---|---|---|---|
| -30°C | -708 | -707.7 | -704 | -701 | -695.5 | -690.6 |
| 0°C | -604.8 | -604 | -604 | -601.5 | -598.5 | -600.7 |
| 27°C | -500 | -500 | -500 | -500 | -500 | -497.6 |
| 85°C | -244 | -243 | -245 | -251 | -258 | -247 |

columns 2, 3, 5, and 6, we find that control voltages $V_g$ change with the temperature and sizes of transistors in OTA. However, the changes across the temperature range are dominant, while the changes caused by varying sizes of the transistors are small. Column 7 is same as the column 4 of Table 4-3. That is to say, these values of $V_g$ are produced by the slave subsystem operating using the reference OTA. From Table 4-5, one can find these practical values are very close to the desired values as shown in columns 2, 3, 4, 5 and 6. If these practical control voltages are applied to the different OTAs at different temperatures, it will not result in substantial error. Therefore, if the transconductance gains of the OTAs in $g_m$-C filter are not too different (the largest value of $g_m$ is 8 times of the smallest one in the above example), the same slave subsystem can be used to control

distinct $g_m$. This will facilitate saving of substrate area.

### 4.3.3 Results for the Band-pass Filter

The schematic of the band-pass filter is shown in Figure 2-6. As mentioned in Chapter 2, the second-order $g_m$-C band-pass filter, as a master subsystem, has been fabricated on chip to validate the proposed technique. The OTAs in the filter network, as shown in Figure 2-6, have been arranged to have the same transconductance value (i.e. 314 μ mhos), so the terminal $V_g(T)$ for each OTA will be connected to output terminal $V_{control}$ of slave subsystem. Because the parasitic capacitors are considered in post layout simulation, the values of the capacitors $C_1$ and $C_2$ were changed to 4.5 pF and 4.4 pF, respectively, from the nominal value of 5 pF. However, because the analog pads, which are provided by Canadian Microelectronics Corporation (CMC), in our chip include some black-boxes, the associated parasitic could not be extracted. The effects of parasitic capacitance from the pads are not considered in the post layout simulation results. The AC analysis test bench for the second-order band-pass filter is shown in Figure 4-12.

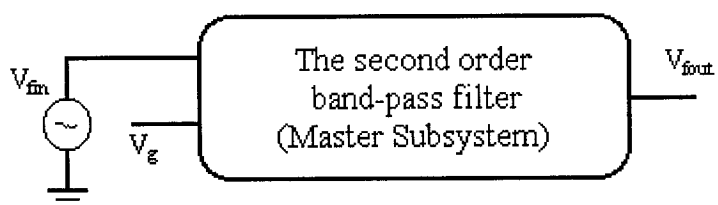


Figure 4-12: Test bench of the second-order band-pass filter

When the $V_g$ is fixed at –0.5V, different temperatures produce the results without feedback. However, when the $V_g$ is changed with temperature as the values in Table 4-3, one can get the AC response of the filter with feedback at different temperatures. Table 4-6 shows the variation in center frequency and bandwidth of the band-pass filter as the temperature is changed. It is obvious that the frequency and bandwidth variations are reduced considerably when the control voltage $V_g(T)$ is applied to the master OTAs, This is revealed by the data in columns 4 and 5 of Table 4-6 . The variation of center frequency improves roughly 12 times over the range of temperature.

**Table 4-6 The Simulation Results on the Band-pass Filter**

| Temperature | Without feedback | | With feedback | |
|---|---|---|---|---|
| | Band edges(MHz) | $f_p$(MHz) | Band edges(MHz) | $f_p$(MHz) |
| -30°C | 8.50 ~ 23.81 | 13.87 | 6.35 ~ 17.62 | 10.39 |
| 0°C | 7.07 ~ 19.69 | 11.68 | 6.19 ~ 17.14 | 10.07 |
| 27°C | 6.14 ~ 17.01 | 9.99 | 6.16 ~ 17.07 | 10.01 |
| 85°C | 4.80 ~ 13.19 | 7.85 | 6.09 ~ 16.78 | 9.89 |

The three curves in Figure 4-13 are AC responses at -30°C, 27°C, and 85°C of this band-pass filter in absence the proposed feedback. The three curves in Figure 4-14 show the cases with the proposed feedback.

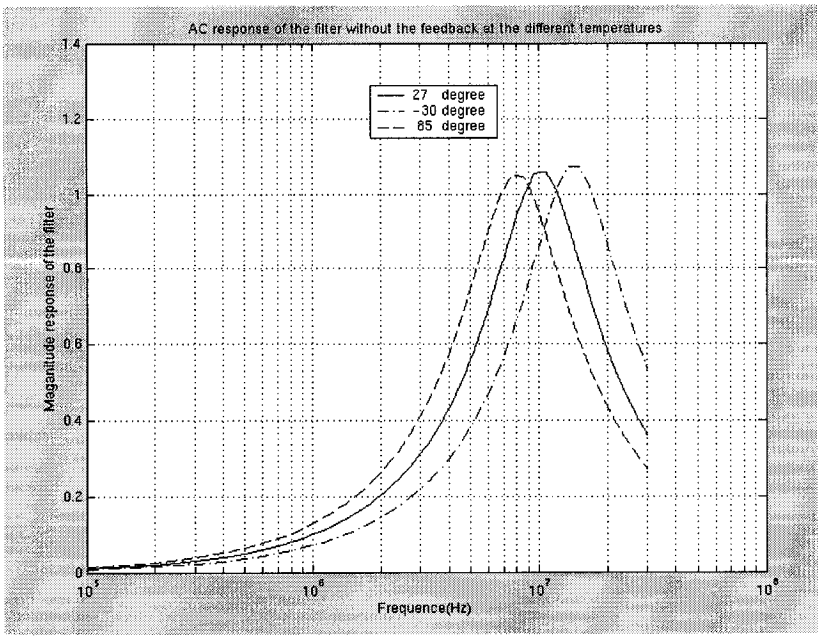


Figure 4-13: AC responses of the band-pass filter without the proposed feedback

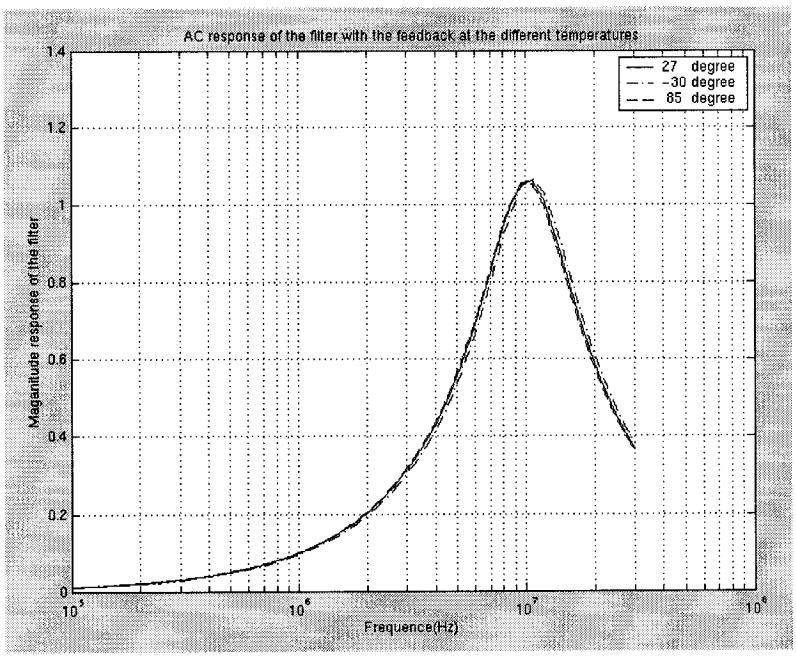


Figure 4-14: AC responses of the band-pass filter with the proposed feedback

The test bench for the transient response of the band-pass $g_m$-C filter can be achieved by combining the set ups in Figure 4-11 and Figure 4-12 together. That is to say, when $V_g$ and $V_{control}$ are made identical, one gets the transient response of the filter with feedback at different temperatures. The transient response of the band-pass $g_m$-C filter without and with feedback at -30°C, 27°C, and 85°C are shown in Figure 4-15 and Figure 4-16, respectively. The input signal for the filter is sinusoidal signal with 10 MHz frequency and 50mV magnitudes. Comparison of Figure 4-15 with Figure 4-16 proves that this scheme is very effective in stabilizing the center frequency and Q-factor of filters against temperature variations.

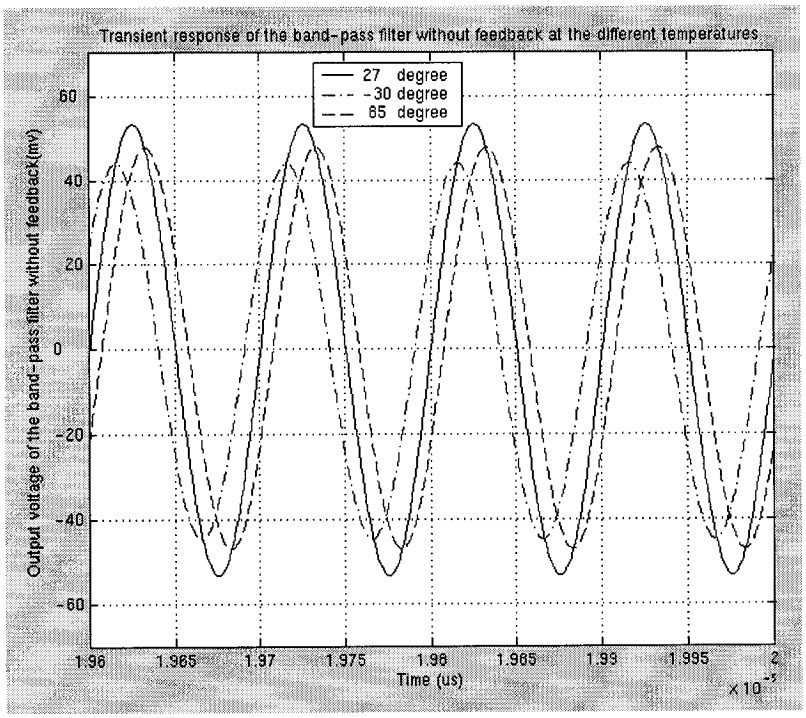


Figure 4-15: Transient response of the filter without the feedback at different temperatures

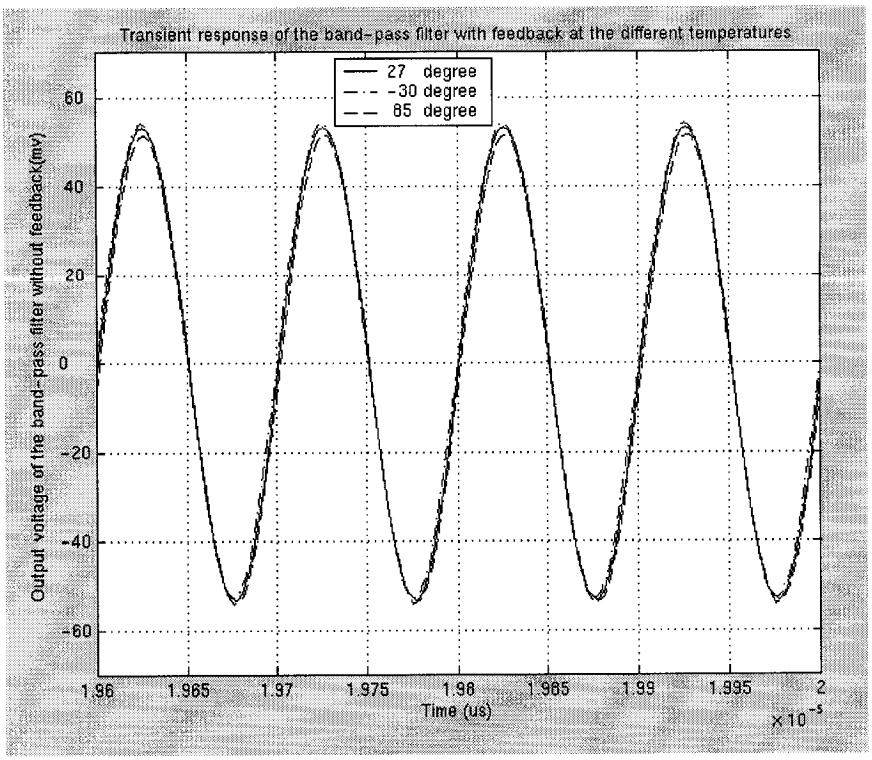


Figure 4-16: Transient response of the filter with the feedback at different temperatures

### 4.3.4 Results for the Low-pass and Notch Filter

In order to verify the feedback control strategy further, we applied this strategy to the low-pass and notch filter to prove its universality. The low-pass network with the architecture of a general biquad $g_m$-C filter is shown in Figure 4-17, and the transfer function of this filter is:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2}g_{m5}/C_1C_2}{s^2 + s\,g_{m3}/C_2 + g_{m1}g_{m2}/C_1C_2} \qquad (4\text{-}8)$$

Similarly, to simplify the circuit, all OTAs in the general biquadratic $g_m$-C low-pass filter have been arranged to have the same transconductance value and same capacitance, i.e., $g_{m1}= g_{m2}= g_{m3}=g_{m5}=g_m=314$ μ mhos, $C_1=C_2=C=5$ pF. Thus the cut-off frequency of this low-pass filter is 10 MHz with $Q_p=1$.

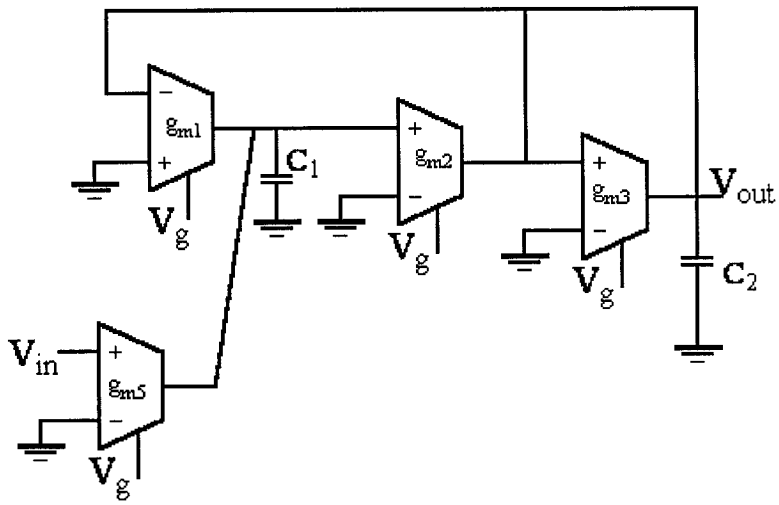


Figure 4-17: Low-pass general biquad $g_m$-C filter

Considering the effects from the parasitic capacitance, in the pre-layout simulation, we take $C_1=C_2=4.9$ pF. Table 4-7 shows the variation in cut-off frequency of the low-pass filter as the temperature is changed. When the control voltage $V_g(T)$ is applied to the OTAs in the low-pass filter, the cut-off frequency variations are reduced about 13 times over the temperature range from –30°C to 85°C. The three curves in Figure 4-18 are AC responses at -30°C, 27°C, and 85°C of this low-pass filter in absence of the proposed feedback. The three curves in Figure 4-19 show the case with proposed

feedback present.

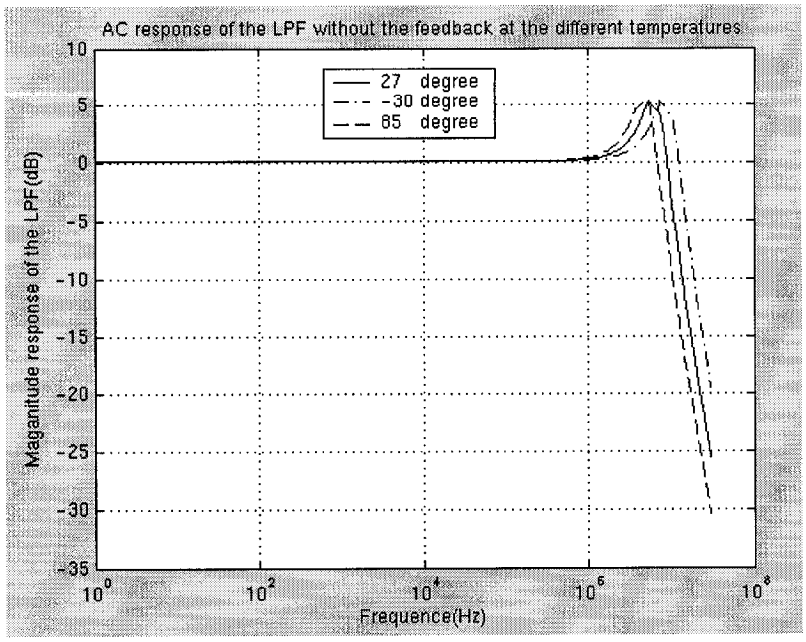


Figure 4-18: AC responses of the low-pass filter without the proposed feedback

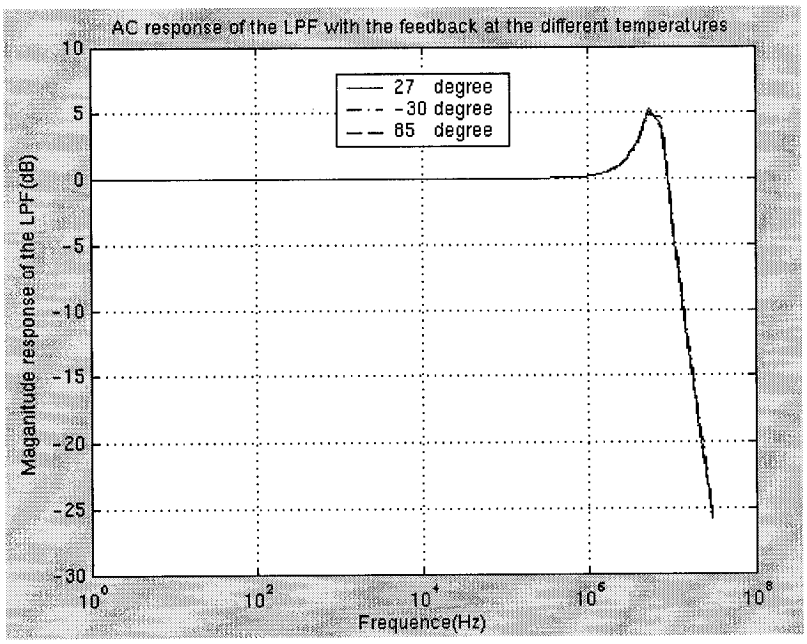


Figure 4-19: AC responses of the low-pass filter with the proposed feedback

**Table 4-7 The simulation results on the LPF and Notch filters**

| Temperature | Cut-off frequency of LPF (MHz) | | Center frequency ($\omega_n$=$\omega_p$) of Notch filter (MHz) | |
|---|---|---|---|---|
| | Without feedback | With feedback | Without feedback | With feedback |
| -30°C | 13.86 | 10.36 | 14.13 | 10.47 |
| 27°C | 10.02 | 10.05 | 10.00 | 10.00 |
| 85°C | 7.70 | 9.93 | 7.76 | 9.90 |

The general biquad $g_m$-C notch filter is shown in Figure 4-20, and the transfer function of this filter is:

$$\frac{V_{out}}{V_{in}} = \frac{s^2 + g_{m2}g_{m5}/C_1C_2}{s^2 + s\,g_{m3}/C_2 + g_{m1}g_{m2}/C_1C_2} \qquad (4\text{-}9)$$

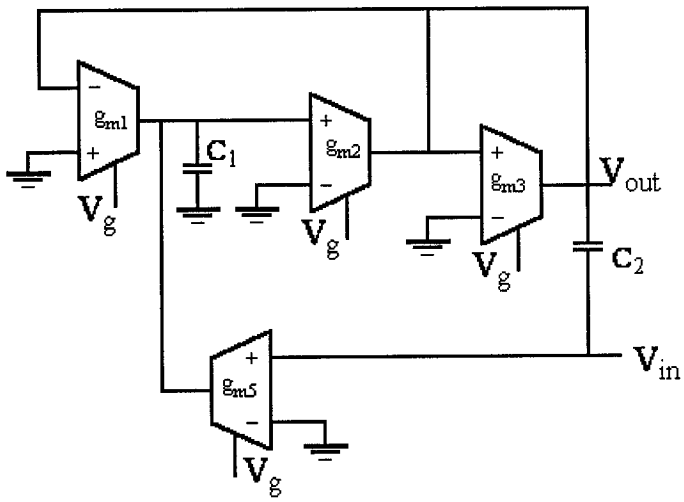


Figure 4-20: Notch general biquad $g_m$-C filter

When we take all OTAs in the general biquadratic $g_m$-C notch filter having the same transconductance value and same capacitance, i.e., $g_{m1}=g_{m2}=g_{m3}=g_{m5}=g_m=314$ $\mu$ mhos, $C_1=C_2=C=5$ pF. Thus, the center frequency $\omega_p$ (and $\omega_p=\omega_n$) of this notch filter is 10 MHz with $Q_p=1$.

In the pre-layout simulation, we take $C_1=C_2=4.8$ pF after considering the effects from the parasitic capacitance. Column 4 and column 5 in Table 4-7 display the variations in center frequency of the notch filter as the temperature is changed. Comparing column 4 with column 5, the center frequency variations of the notch filer are reduced 11 times over temperature variations. The three curves in Figure 4-21 are AC responses at -30°C, 27°C, and 85°C of this notch filter without the proposed feedback. The three curves in Figure 4-22 show the case with the proposed feedback.

Comparison of Figure 4-13, Figure 4-18 and Fig 4-21 with Figure 4-14, Figure 4-19 and Figure 4-22, respectively, it is obvious that the proposed feedback is very effective in stabilizing the center frequency and Q-factor of filters against temperature variations. And all these are in close agreements with the theoretical expectation.

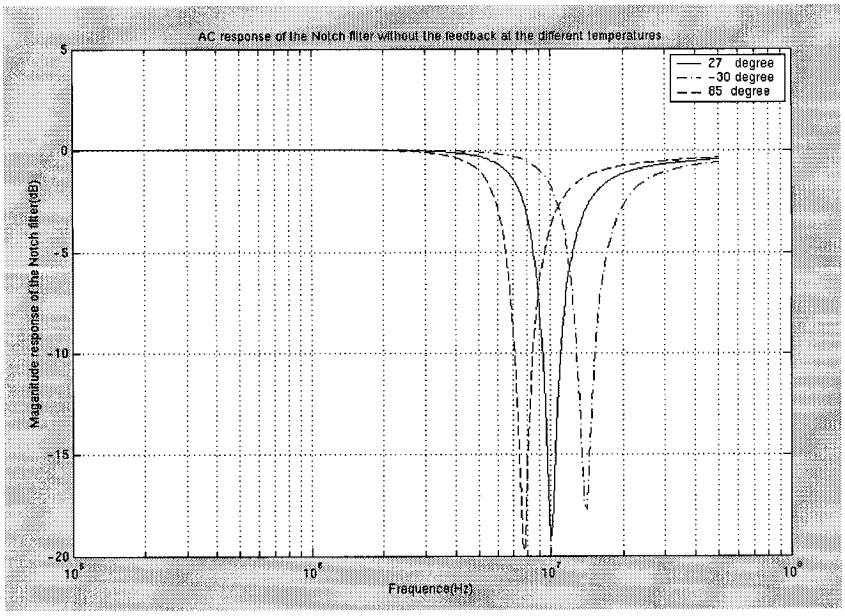


Figure 4-21: AC responses of the notch filter without the proposed feedback

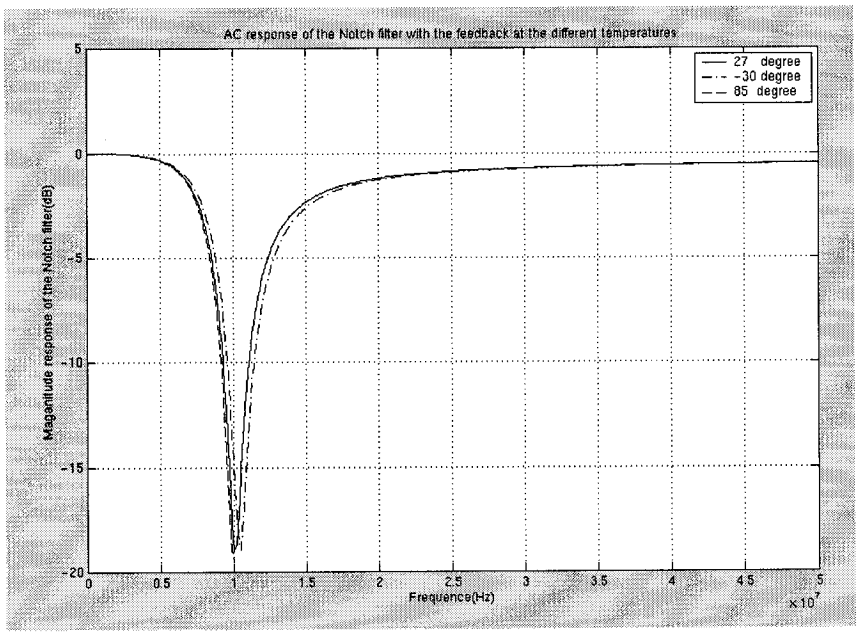


Figure 4-22: AC responses of the notch filter with the proposed feedback

## 4.4 Summary

This chapter presented the implementation of the whole system based on TSMC 0.18 μm CMOS process technology. Large resistors and capacitors are implemented using MiM capacitor and N+ non-silicided poly resistor, respectively. Layout techniques used in the system implementation to minimize the side effects of transistor pair mismatch and parasitics have been discussed.

The numerical simulation results of the proposed control strategy prove its effectiveness theoretically. Pre and post layout simulation results demonstrate that the proposed negative feedback technique is practically effective in stabilizing the transconductance gain ($g_m$) of OTAs and pole frequency and pole Q of filters against temperature variations. In the following chapter experimental results on the system fabricated using TSMC 0.18 μm CMOS process will be presented and discussed.

# Chapter 5

# Experimental Results and Discussion

This chapter presents measurement set-up and results on the fabricated chip. The experimental results confirm the functionality of proposed feedback technique. The deviation from the expected outcome is discussed.

## 5.1 Measurement Setup

The slave subsystem and the master subsystem, which consists of the second-order $g_m$-C band-pass filter, have been fabricated in TSMC 0.18 μm CMOS process through the facilities of the Canadian Microelectronics Corporation (CMC). Figure 4-8 shows the layout of the whole chip. The whole die area is $1mm^2$ inclusive of the pad frame, and the package is selected with 40 pins of DIP (Dual In-Line Package) architecture. The pin enumeration mapping is shown in Table 5-1, and the pin meanings

of the slave subsystem refer to the schematic of subsystem as shown in Figure 4-1(it is included here for convenience). The master subsystem has only the input terminal $V_{fin}$ and the output terminal $V_{fout}$.

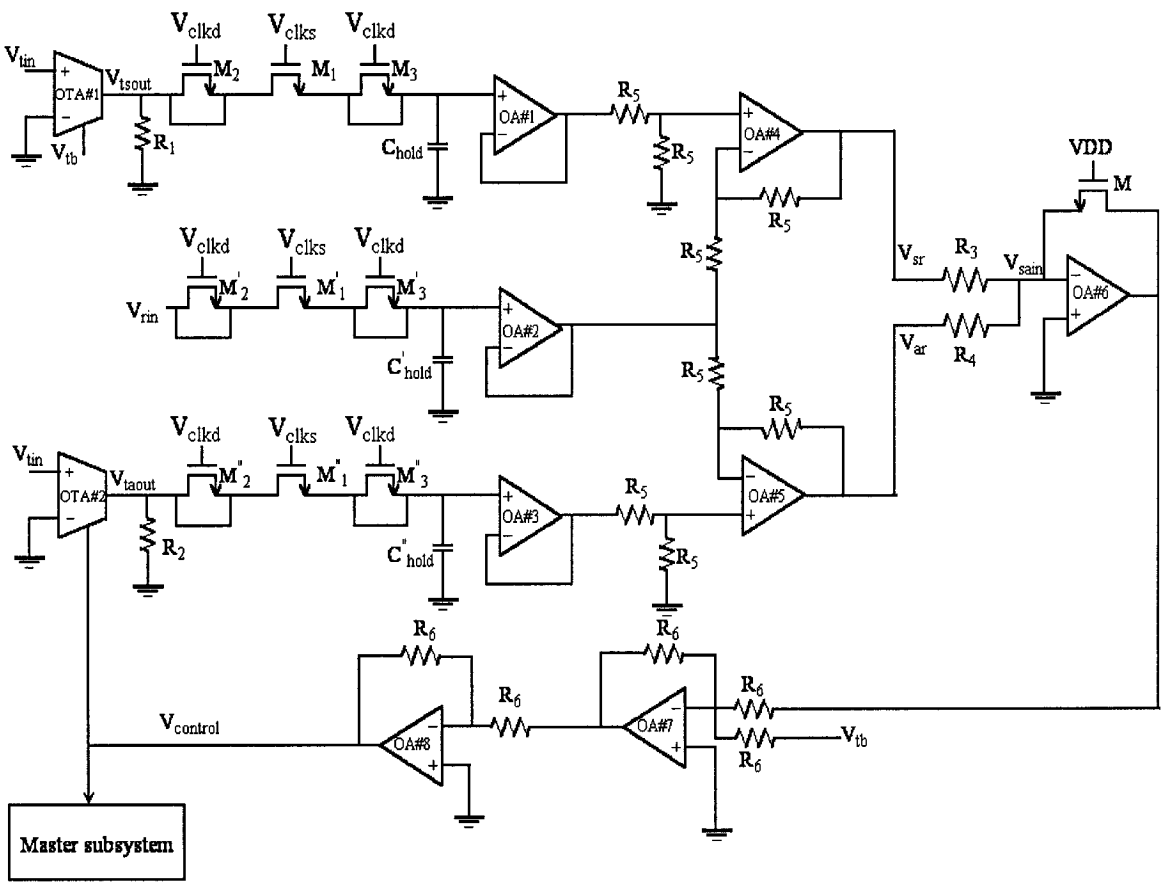


Figure 4-1: Schematic of the slave subsystem

**Table 5-1 Pin Enumeration of the Fabricated Chip**

| Pin Name | Pin Number | Pin Name | Pin Number |
|---|---|---|---|
| VDD | 38 | $V_{rin}$ | 32 |
| VSS | 1 | $V_{tin}$ | 33 |
| GND | 20 | $V_{opb}$ | 31 |
| $V_{clks}$ | 34 | $V_{control}$ | 30 |
| $V_{clkd}$ | 40 | $V_{sr}$ | 19 |
| $V_{tb}$ | 2 | $V_{ar}$ | 18 |
| $V_{tsout}$ | 8 | $V_{fin}$ | 21 |
| $V_{taout}$ | 9 | $V_{fout}$ | 22 |
| $V_{sain}$ | 11 | | |

The test bench for AC characteristics measurement is given in Figure 5-1. A sweeping AC sinusoidal voltage signal with 50 mV magnitude, which is provided by a signal generator, is applied to the input terminal $V_{fin}$ of the filter, and the output terminal $V_{fout}$ is probed by the oscilloscope. The test board with the chip was put into the thermal chamber, and all signal lines were connected to outside equipment through a hole of the thermal chamber (Model: Thermotron F-32CHV - ECA - AD). Then, the hole was filled using sponge.

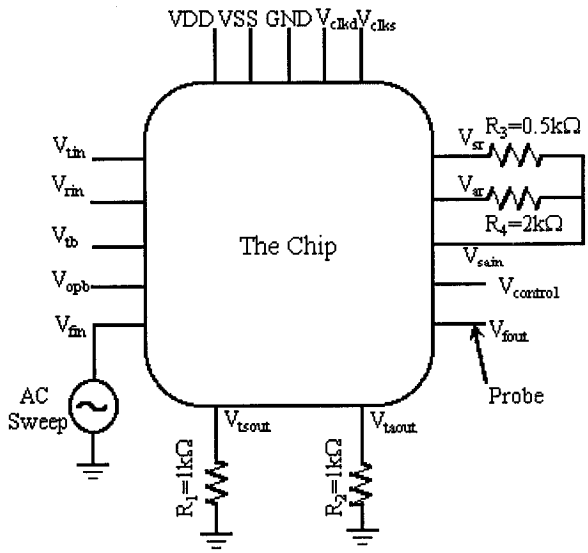


Figure 5-1: Measurement setup

The measurement is separated into two steps. The first step is to test the center frequency of the second-order band-pass $g_m$-C filter without the proposed feedback circuitry at different temperatures. In this case, VDD, VSS, and GND are provided; on the other hand, a fixed bias voltage of -0.5V is connected to $V_{control}$ terminal. At every testing temperature, through sweeping the input signal frequency, one records the output amplitude of the filter. The frequency of the input signal corresponding to the maximum output amplitude is considered as the center frequency of the band-pass filter at this temperature.

The next step is to measure the center frequency of the second-order band-pass $g_m$-C filter with the proposed feedback at different temperatures. The voltages, i.e., VDD,

VSS, $V_{tb}$, $V_{clks}$, $V_{clkd}$, $V_{opb}$, $V_{tin}$, $V_{rin}$, are all activated as shown in Figure 5-1. Using similar test approach as described in the proceeding paragraph, we get the center frequency of the filter with the control system at different temperatures.

## 5.2 Measurement Results

Since the thermal chamber was not available in the departmental laboratory, we sought help from an external agency, i.e., CMC Electronic Inc.(Courtesy Mr. Alok Bhattacharya). The time allotment for use of equipment was limited, so only one chip could be tested completely. The experimental results for the center frequency of the $g_m$-C band-pass filter at different temperatures are tabulated in Table 5-2.

**Table 5-2 The Experimental Results on the Band-pass Filter**

| Temperature | Without feedback | With feedback |
|---|---|---|
| | $f_p$(MHz) | $f_p$(MHz) |
| -30°C | 3.54 | 2.47 |
| -10°C | 3.02 | 2.16 |
| 0°C | 2.77 | 2.02 |
| 27°C | 1.91 | 2.14 |
| 60°C | 1.23 | 2.08 |
| 85°C | 1.01 | 1.96 |

Comparing column 2 with column 3 in Table 5-2, it is obvious that the center frequency variations of the $g_m$-C band-pass filter with the negative feedback over the range of -30°C to 85°C are improved roughly 5 times. That is to say, the feedback control system works as our theoretical expectation. But, there exists around 7.8 MHz of center frequency deviation at room temperature. Such large disparity could arise from several reasons. Some of these are discussed below.

## 5.3 Discussion of Experimental Results

The center frequency deviation of the chip filter is caused by two reasons. The main reason for this is that a buffer was not added at the output of the filter. A buffer should be connected at the output of the filter to separate the filter from the loading caused by the test equipment and parasitic capacitances from the pads and the package. Otherwise, the input impedance of the test equipment and parasitic capacitances of the pads and the package are directly added to the output of the filter, and this amounts to an increase in the design value of capacitor $C_2$ of the filter as shown in Figure 2-6(a). Since the center frequency of the $g_m$-C band-pass filter is proportional inversely to the value of the capacitor, the center frequency of the filter will be decreased accordingly.

In this test case, the TDS 3000 Series Digital Phosphor Oscilloscopes is used to detect the output of the filter. The input impedance of this oscilloscope [25] is 1MΩ±1%

in parallel with 13 pF ± 2 pF. For the parasitic capacitance of the bonding pads, some searches [26][27] indicated a value of approximately 1.5 pF. Although the author did her best to search the parasitic capacitance of the 40-DIP package used in this experiment, but no specific value could be known. As a rule of thumb, the parasitic capacitance from 40-DIP package can be estimated around 2 pF. When all these elements are considered at the output of the filter as shown in Figure 5-2, simulation results display the center frequency of the $g_m$-C band-pass filter without the feedback is decreased to 3.801 MHz at room temperature.

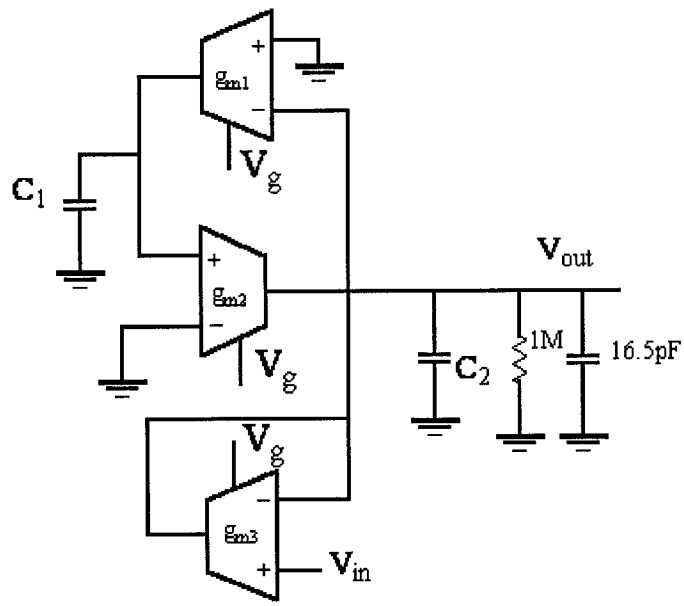


Figure 5-2: The equivalent schematic diagram of the band-pass filter

On the other hand, in this negative feedback control system the main focus has

been towards reducing the temperature effects on the transconductance gain ($g_m$) of the OTAs. In reality, the values of the transconductance ($g_m$) and capacitors in the $g_m$-C band-pass filter are affected by process variations. However, as CMOS IC fabrication technology becomes more and more advanced, the control of process variation and manufacturing uncertainty becomes more and more critical. The circuit yield loss caused by the process and device parameter variation has been more pronounced than before [28]. Due to difficulty in controlling the variation in different fabrication steps such as gate oxide growth, channel and source/drain implants, photolithography and etching etc in modern technologies, the variation in device parameters will become larger compared with older technology. The capacitors in the filter are implemented using MiM capacitor as mentioned in chapter 4, and the capacitance value of a MIM capacitor is sensitive to variation in the thickness of dielectric and geometry of metal plates. In general, the variation in MiM capacitors can be larger than 20%[28].

On assuming 20% process variation, that is to say, the values of capacitors $C_1$, $C_2$ and $g_m$ change 20% with process variation, we repeated the simulation. The stray effects of the measuring equipment were also counted in. The simulated center frequency of the $g_m$-C band-pass filter changed to 1.909 MHz, which is very close to the experimental result of the filter without feedback at room temperature.

The above analyses demonstrate the experimental results are quite reasonable

when all the perturbing factors are considered. Simulation data reveal the power consumption of the filter and the control system to be about 0.44 mW and 4.49 mW, respectively.

## 5.4 Summary

In this chapter, measurement results on the fabricated chip have been presented and discussed. The experimental results reveal that the proposed feedback functions properly if the input impedance of the test equipment, parasitic capacitance of the pads and package, and process variations are considered. Through testing the chip and analyzing the experimental results, a great amount of hands-on experience about analog IC design has been gathered.

# Chapter 6

# Conclusion

This chapter summarizes the key contributions in design of the OTA with a temperature insensitive transconductance and its application in $g_m$-C filters, and gives suggestions for the future work.

## 6.1 Conclusion

The key contributions of this project are claimed as follows:

* The mathematical model for transconductance gain ($g_m$) of the CMOS OTA has been formulated, and it reveals that the transconcuctance gain of OTA is a nonlinear function of temperature.

* A new simple negative feedback technique has been applied to produce the temperature dependent control voltage (bias voltage) for the OTA to maintain the stability of transconductance gain ($g_m$) against the temperature variation over the industrial range of –30°C to +85°C, and the derivation of the overall control mechanism is provided.

* Several types of second-order $g_m$-C filters with temperature stabilized OTAs, have been built to validate the proposed feedback control system. The pole frequency and pole Q of the $g_m$-C filters depend on the transconductance gain ($g_m$). So the stabilized transconductance gain ($g_m$) against temperature variation will bring stability in the frequency and quality factor of the filters built from these OTAs.

* The test chip has been implemented using TSMC 0.18 μm CMOS technology, and fabricated through the facilities of Canadian Microelectronics Corporation (CMC).

* The post layout simulation results reveal that the OTA transconductance gain variation has been reduced from typically 61.8% to 2.4% over the range of –30°C to +85°C. The variation in the center frequency of the $g_m$-C filter is reduced from 60.2% (without feedback control) to 5% (with feedback control)

over the same temperature range.

In conclusion, this system is very suitable for implementation in a modern CMOS technology, and may prove to be competitive to the techniques proposed so far in terms of power and area overhead requirements in an IC technological environment.

## 6.2 Future Work

A chip with the test buffer at the output of the filter may be fabricated and tested again.

During the filter tests, some noise signals have been observed. Most likely, these noises may be reduced through building a differential structure filter. Since the substrate area granted by CMC was limited, the differential structure could not be employed.

Another interesting work would be to find the characteristics of the integrated capacitor with temperature variation, since the pole frequency and pole Q of the $g_m$-C filter not only depend on transconductance ($g_m$) of the OTAs, but also are determined by the values of capacitors. If the temperature effects of the transconductance ($g_m$) and capacitances are considered together, the control efficacy for the frequency and quality factor of $g_m$-C filters is expected to improve.

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# REDUCING THE TEMPERATURE EFFECT ON A CMOS TRANSCONDUCTANCE AND ITS APPLICATION IN $g_m$-C FILTERS

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## Abstract

*A new negative feedback technique is applied to stabilize changes in the transconductance of a CMOS Operational Transconductance Amplifier (OTA) with temperature variations over the industrial range of –30°C to +85°C. Since OTAs are used as the basic building blocks in various $g_m$-C filters, stabilizing the transconductance will bring stability in the frequency and quality factor of the filters built from these OTAs. To validate this notion, a second order band-pass filter with 10MHz center frequency has been built with the temperature stabilized OTAs. The whole system has been implemented in TSMC 0.18μm CMOS technology available through the Canadian Microelectronics Corporation (CMC) and tested in the laboratory. The experimental results show close agreement with the theoretical expectations.*

***Keywords:*** *Temperature effect; Transconductance; CMOS; $g_m$-C band-pass filter.*

## 1. INTRODUCTION

Integrated continuous-time filters are suitable solutions to perform a variety of signal processing tasks. A popular approach to the design of such filters, that is fully compatible with current CMOS technologies, is the transconductance-C ($g_m$-C) filters. The critical problem in the design of this kind of filters is necessity for some sort of tuning circuitry. Phase locked loop technique [1] using master slave system has been popular for low frequency. Envelope detection technique using mixed mode analog-digital circuits has been proposed for frequencies around 150 MHz [2]. OTAs are main components of $g_m$-C filters, and variable $g_m$ has a detrimental effect on the performance of $g_m$-C filters. One principal factor to cause such variations of the transconductance ($g_m$) values is the changes in environment temperature.

In this paper, a novel technique using simple negative feedback to stabilize $g_m$ of an OTA against temperature variations is introduced, and a practical application to a second-order $g_m$-C band-pass filter is illustrated.

In the following, a block diagram of the system that ensures a nearly constant $g_m$ despite variations in the environmental temperature is described first. Design considerations for the various subsystems are addressed next. This is followed by some analyses pertaining to the overall control mechanism against temperature variations. Simulation and experimental results for the system implemented with TSMC 0.18μm CMOS process are presented to establish the efficacy of the proposed negative feedback technique.

## 2. OVERALL SYSTEM

Fig.1 shows the block diagram of the whole system. The slave subsystem includes two forward paths and one feedback path. It produces the temperature dependent control voltage $V_g(T)$, and this control voltage is simultaneously applied to the OTAs in the master subsystem of the $g_m$-C filter to stabilize their $g_m$-values so that the filter has stable center frequency and Q-factor over the range of –30°C to +85°C.

### 2.1 Design of the Slave Subsystem

The parameters of a MOS transistor in a CMOS process display temperature dependence. In the square law model of I-V equation:

$$I = K(W/2L)(V_{gs} - V_{th})^2 \quad (1)$$

The 'K' and '$V_{th}$' parameters are temperature dependent functions and are given by [3]:

$$K(T) = K(T_0)\left(\frac{T}{T_0}\right)^n \text{ and } V_{th}(T) = V_{th}(T_0) + \alpha\left(T/T_0 - 1\right) \quad (2)$$

If we consider the OTA built from a typical common source differential pair as shown in Fig.2, the $g_m$ of the OTA is dependent upon the voltage $V_g(T)$ according to:

$$g_m(T)\big|_{V_g(T)} = K(T)\sqrt{\frac{W_4W_5}{2L_4L_5}}\left(V_g(T)-V_{ss}-V_{th}(T)\right) \quad (3)$$

In order to meet the condition of $g_m(T)\big|_{V_g(T)} = g_m(T_0)\big|_{V_g(T_0)}$ at the different temperatures, the control voltage $V_g(T)$ must change with temperature as:

$$V_g(T) = \frac{K(T_0)\left(V_g(T_0) - V_{ss} - V_{th}(T_0)\right)}{K(T)} + V_{ss} + V_{th}(T) \quad (4)$$

It is obvious that $V_g(T)$ is a nonlinear function of T, and it is to be obtained from the control circuit shown in Fig.1. Then the $g_m$ of the OTA will be held close to $g_m(T_0)$ over the temperature range.

The control circuitry includes four principal components: sample-and-hold circuit, difference amplifier, summer, and nonlinear amplifier. The proposed sample-and-hold circuit with two dummy switches, operational amplifier (OP-AMP), and nonlinear amplifier are shown in Fig.3, Fig.4, and Fig. 5, respectively.

In the nonlinear amplifier, a NMOS transistor M is used as a feedback resistor. The gain of the amplifier is given by:

$$A'(T) = -\frac{L/W}{K(T)R\left(V_{gs}-V_{th}(T)-V_{ds}\right)} \quad (5)$$

Where $V_{gs}$, $V_{th}(T)$ and $V_{ds}$ are relative to the transistor M. Since K(T) and $V_{th}(T)$ are nonlinear function of T, the gain will be a nonlinear function of T.

## 2.2 Overall Control Mechanism

Assume that the two OTAs in slave subsystem are driven by the same sinusoidal signal with small amplitude $V_s$. The signals developed across the two resistors $r_1$ and $r_2$ (Fig.1) are, respectively:

$$V_{r1}(T) = g_m(T)\big|_{V_g(T_0)} V_s r_1 \quad (6)$$

$$V_{r2}(T) = g_m(T)\big|_{V_g(T)} V_s r_2 \quad (7)$$

Where $r_1=r_2=r$. $r$ is assumed small compared with the output resistance of the OTAs. These two resistors are outside of the chip, so we can choose temperature insensitive resistors. Therefore, the change in $r$ will remain small over the temperature range. This assumption is not critical for success of the method, but it simplifies expressions. Assume:

$$V_{ref}(T_0) = g_m(T_0)\big|_{V_g(T_0)} V_s r \quad (8)$$

For the upper forward path, the error $E_1(T)$ is given by:

$$E_1(T) = V_{r1}(T) - V_{ref}(T_0)$$

$$= V_s r\sqrt{\frac{W_4W_5}{2L_4L_5}}\left[K(T)\left(V_g(T_0)-V_{ss}-V_{th}(T)\right) - K(T_0)\left(V_g(T_0)-V_{ss}-V_{th}(T_0)\right)\right] \quad (9)$$

The error $E_1$ will be zero at $T=T_0$ (i.e., =27°C, say).

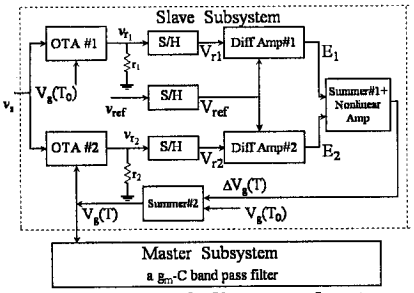


Fig. 1. **The block diagram of system**

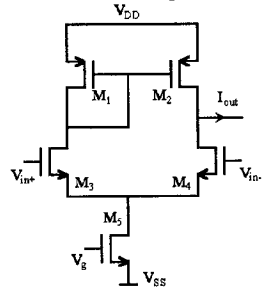


Fig. 2. **Differential pair OTA**

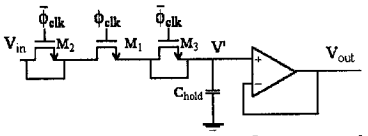


Fig. 3. **S/H circuit with two dummy switches**

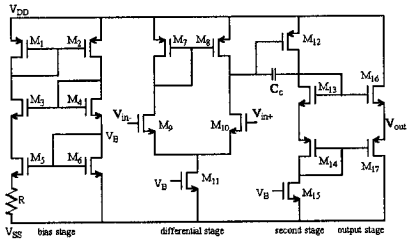


Fig. 4. **The schematic diagram of the OP-AMP**

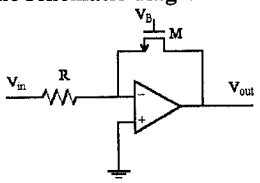


Fig.5. **Nonlinear amplifier**

The dynamic error voltage is given by:

$$E_2(T) = V_{r2}(T) - V_{ref}(T_0) \quad (10)$$

$$= V_s r\sqrt{\frac{W_4W_5}{2L_4L_5}}\left[K(T)\left(V_g(T)-V_{ss}-V_{th}(T)\right) - K(T_0)\left(V_g(T_0)-V_{ss}-V_{th}(T_0)\right)\right]$$

Consider the following nonlinear processing to

achieve $V_g(T)$ in eq. (4):

$$V_g(T) = A(T)(E_1(T) + BE_2(T)) + C \quad (11)$$

Where, A(T) is a temperature dependent voltage gain, B is a constant gain, and C is a DC offset voltage. When the dynamic error $E_2(T)$ approaches zero, we can get:

$$V_g(T) = A(T)E_1(T) + C \quad (12)$$

Setting $C = V_g(T_0)$ and substituting (4) and (9) into (12) yields:

$$A(T) = -1 \Big/ \left( K(T)V_s r \sqrt{\frac{W_4 W_5}{2L_4 L_5}} \right) \quad (13)$$

From this formula, we see that the voltage gain of A(T) is a nonlinear function of T. Comparing (13) with (5), one can match A(T) with A'(T) as close as possible by adjusting the size of the NMOS transistor M, the value of resistor R, and its gate voltage. That is to say, the temperature dependent control voltage $V_g(T)$ can be achieved approximately using the above slave subsystem.

## 3. SIMULATION RESULTS

The simulation has been done using Spectre simulator under Cadence environment based on the TSMC 0.18μm CMOS technology.

### 3.1 Results for $g_m$ of the OTA

The simulation results are summarized in Table 1. Column 2 shows $g_m$ variation of the OTA in absence of feedback as the temperature changes while $V_g$(in Fig.2) is held at –0.5 volts. Column 3 presents the $V_g$ values that will be required to hold the $g_m$ constant at the nominal value at the room temperature (i.e., 314 μ mho at 27°C). Column 4 shows the values of $V_g(T)$ achieved in closed loop, and these values are extremely close to the desired values as shown in column 3. Column 5 shows the $g_m$ value achieved in closed loop condition at the different temperatures. With the proposed control scheme the variation in $g_m$ has been reduced from 61.8% to 2.4% over the range of –30°C to +85°C.

Table 1 **Simulation results for OTA**

| T | $g_m$(μmho) $V_g$ fixed | desired $V_g$(mV) | practical $V_g$(mV) | $g_m$(μmho) $V_g$ tuned |
|---|---|---|---|---|
| -30°C | 438.5 | -704 | -690.6 | 322.8 |
| 0°C | 364.4 | -604 | -600.7 | 315.1 |
| 27°C | 314 | -500 | -497.6 | 315 |
| 85°C | 244.3 | -251 | -247 | 315.2 |

### 3.2 Results for the Band-Pass Filter

A second-order $g_m$-C band-pass filter (Fig.6) has been used to validate the proposed technique. All OTAs in this filter have been arranged to have the same $g_m$ value, so the terminal $V_g(T)$ for each OTA will be connected to the terminal $V_g(T)$ of slave-OTA#2 (see Fig. 1). The design value of center frequency is 10MHz with $Q_p$=1. Table 2 shows that the variations in center frequency and bandwidth of the band-pass filter with temperature changes. These are reduced about 12 times by virtue of the feedback. Fig.7 and Fig.8 are AC responses of this band-pass filter without and with the proposed feedback, respectively.

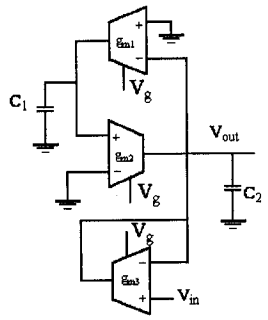


Fig. 6. **A second-order $g_m$-C band-pass filter**

Table 2. **The simulation results on the band-pass filter**

| T | Without feedback | | With feedback | |
|---|---|---|---|---|
| | Band edge (MHz) | $f_p$ (MHz) | Band edge (MHz) | $f_p$ (MHz) |
| -30°C | 8.50 ~ 23.81 | 13.87 | 6.35 ~ 17.62 | 10.39 |
| 0°C | 7.07 ~ 19.69 | 11.68 | 6.19 ~ 17.14 | 10.07 |
| 27°C | 6.14 ~ 17.01 | 9.99 | 6.16 ~ 17.07 | 10.01 |
| 85°C | 4.80 ~ 13.19 | 7.85 | 6.09 ~ 16.78 | 9.89 |

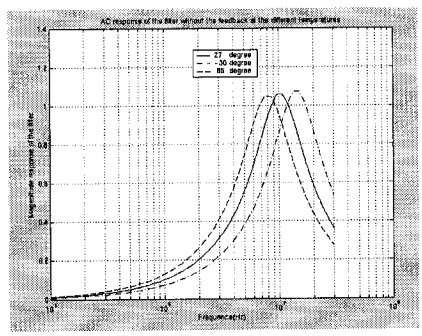

Fig.7 **AC responses of the filter without the feedback**

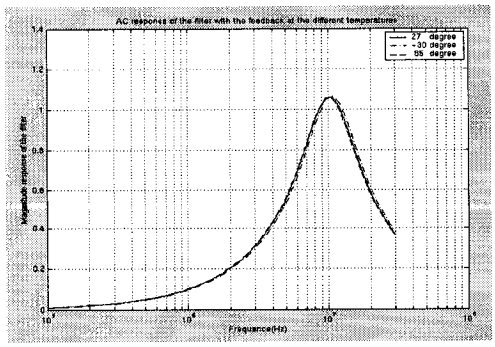

Fig. 8 **AC responses of the filter with the feedback**

## 4. EXPERIMENTAL RESULTS AND DISCUSSION

The system has been fabricated in TSMC 0.18μm CMOS process with 1 $mm^2$ die area inclusive of the pad frame. The experimental results for center frequency of the $g_m$-C band-pass filter at the different temperatures are tabulated in Table 3. In arriving at these results, correction factors due to the loading effects of the test equipment have been considered. Column 3 signifies substantial improvement regarding the stability of the center frequency of the band-pass filter. But, there exists a deviation of about 1.66MHz in the center frequency relative to the theoretical expectation at room temperature. In reality, the capacitors in the $g_m$-C band-pass filter also changes with temperature and with process variations. The MiM capacitors used to implement the filter could vary as much as 20%[4] due to variations in the thickness of the dielectric and geometry of metal plates. In our procedure, such variations were not considered. Therefore, the experimental results appear quite reasonable.

Table 3. **The experimental results on the filter**

| T | Without feedback | With feedback |
|---|---|---|
| | $f_p$(MHz) | $f_p$(MHz) |
| -30°C | 9.74 | 8.67 |
| 0°C | 8.97 | 8.22 |
| 27°C | 8.11 | 8.34 |
| 85°C | 7.21 | 8.16 |

Because of the several functional blocks on the test chip, unrelated to the filter system, accurate measured data of power consumption are not available; but, from simulation results, the power consumption for the overall filter is approximately 4.93mW.

## 5. CONCLUSIONS

A simple negative feedback technique has been proposed to stabilize $g_m$ of an OTA against temperature variations. The technique has been validated using TSMC 0.18μm CMOS technology. The OTA transconductance gain variation has been reduced from typically 61.8% to 2.4% over the range of –30°C to +85°C. As an application, a $g_m$-C band-pass filter has been designed, simulated, and tested. The post layout simulation results display that the variation in the center frequency of the $g_m$-C filter is reduced from 60.2% (without feedback control) to 5% (with feedback control) over the temperature range –30°C to +85°C. The experimental results except for the deviation due to process variational components agree well with the simulation results. The resistors and capacitors in this system are realized using poly without silicide and MiM capacitor, respectively. So, this system is very suitable for implementation in a modern CMOS technology, and may prove to be competitive to the techniques proposed so far [1][2] in terms of power and area overhead requirements in an IC technological environment.

## Acknowledgements

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