HIGH FREQUENCY AC DISTRIBUTED POWER SYSTEM FOR DESKTOP COMPUTER APPLICATIONS

Mei Qiu

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High Frequency AC Distributed Power System for Desktop Computer Applications

Mei Qiu, Ph.D.
Concordia University, 2004

ABSTRACT

The continual increasing performance of the desktop personal computer (PC) benefited from the advances in semiconductor technology presents increasing challenges for the power demands, such as higher power density, lower supply voltage with very tight tolerance, and higher supply current with very high slew rate (di/dt).

The existing dc distributed power system (DC DPS) suffers from low efficiency and poor transient response. This thesis introduces a new power architecture – high frequency ac distributed power system (HFAC DPS). In this power architecture, the front-end inverter generates sinusoidal voltage and current distribution for the ac bus; and then on board AC voltage regulator module (AC VRM) converts the intermediate ac voltage to a specific low dc voltage to power the load.

The objective of this thesis is to develop and implement HFAC DPS for the application of desktop computers. To achieve this objective, an asymmetrical pulse-width-modulated (APWM) resonant inverter and a PWM series resonant converter are proposed as the front-end inverter and AC VRM respectively. These two topologies both employ new control schemes to meet the future power requirements. Based on these two proposed topologies, HFAC DPS is implemented for a dual output application.

In this thesis, at both system level and circuit level for each proposed topology, detailed steady-state and dynamic analyses are performed, performance characteristics are presented, and the design procedures are generated. Simulation and experimental results are obtained from the prototype circuits to demonstrate the proof-as-concept.

The results obtained from this thesis present the following features of HFAC DPS: reduced power conversion stages, soft switching in each stage, high voltage and low current distribution, independent and tight voltage regulation at the point of load and excellent response against large transient signals in both dc input voltage and load current.

All these features indicate that HFAC DPS has potentially better power delivery quality and easier thermal management than the existing DC DPS. Therefore, HFAC DPS can be considered as an alternative solution to powering the new generations of desktop personal computers.

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To my parents

To my husband Djilali

and my daughter Myriam

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LIST OF ACRONYMS

AC	Alternative Current
APWM	Asymmetrical Pulse-Width-Modulated
ASIC	Application-Specific integrated circuit
CPU	Central Processing Unit
DC	Direct Current
DPS	Distributed Power System
EA	Error Amplifier
EMI	Electromagnetic Interference
ESL	Equivalent Series inductance
ESR	Equivalent Series Resistance
FF	Feedforward
FB	Feedback
HF	High Frequency
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LF	Low Frequency
LTI	Linear Time Invariant
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPU	Microprocessor Unit
PC	Personal Computer
PCB	Printed Circuit Board
PFC	Power Factor Correction

PWM	Pulse-width-modulation
RMS, rms	Root Mean Square value
SR	Synchronous Rectifier
THD	Total Harmonic Distortion
ZVS	Zero Voltage Switching
VLSI	Very Large Scale Integrated circuit
VRM	Voltage Regulator Module

LIST OF PRINCIPLE SYMBOLS

In this thesis, for instantaneous voltage and current that are functions of time, the symbols used are lowercase letters v and i respectively. The uppercase symbols V and I refer to their values computed from their instantaneous waveforms. They generally refer to an average value in dc quantities and a rms value in ac quantities. The peak values are indicated by the symbol "^" on top of the uppercase letters. The small disturbance from its nominal value is indicated by the symbol "~" on top of the lowercase letters. In this list, for voltages and currents, only their instantaneous symbols are listed.

α	Control angle of S_2 in phase-shift modulation (VRM)
α_n	Intermediate angle to calculate ϕ_n (Inverter)
β	Phase difference between the fundamental input current and transformer primary side voltage (VRM)
θ	Phase difference between the fundamental input voltage and current (VRM)
θ_n	Phase angle of the voltage v_{S2_ac} (Inverter)
ϕ_n	Phase difference between current i_r and voltage v_{S2_ac} (Inverter)
γ_n	Phase difference between voltage v_{S2_ac} and voltage v_p (Inverter)
	Phase difference between the harmonic input voltage and current (VRM)
τ	Integral time constant (Inverter)
ω_{eq}	Resonant frequency of the equivalent series resonant branch
ω_o	Operating frequency
ω_p	Resonant frequency of the parallel resonant branch

ω_s	Resonant frequency of the series resonant branch
η	Efficiency of the inverter or VRM
η_{rec}	Target rectification efficiency
$a_n, b_n, A_n, B_n, C_n, D_n, E_n, F_n$	Coefficients used in the expression of Fourier Series
C_2	Capacitor of 2nd harmonic trap
C_3, C_4	Capacitors in the error amplifier
C_{eq}	Equivalent series resonant capacitance (VRM)
C_f	Capacitor of input filter
C_p	Parallel resonant capacitor
C_s	Series resonant capacitor
C_{sn1}, C_{sn2}	Snubber capacitors of S_1 and S_2 of the inverter respectively
D	Duty cycle of switch S_1 of the inverter
d	Duty cycle of the PWM signal of the AC VRM
F_{co}	Cross-over frequency of the overall open loop
F_p	Pole frequency
F_z	Zero frequency
f_i	Resonant frequency of the input filter
f_o	Operating frequency of the inverter or VRM
G_{EA}	Required amplifier gain at the cross-over frequency
i_2	Current flowing through the 2nd harmonic trap
i_{Lp}, i_{Cp}	Currents through the parallel resonant inductor and capacitor respectively
i_{Lm}	Transformer magnetizing current (VRM)

i_r	Input resonant current flowing through series resonant branch (Inverter)
	Input resonant current (VRM)
i_{Req}	Current flowing through the equivalent load resistance (VRM)
i_{S1}, i_{S2}	Currents flowing through switch S_1 and S_2 respectively (Inverter)
i_{SR1}, i_{SR2}	Currents flowing through SR switches
$I_{s1\_turn\text{-}off}$	Turn-off current of switch S_1 (Inverter)
$I_{s2\_turn\text{-}off}$	Turn-off current of switch S_2 (Inverter)
k_{Lm}	Magnetizing inductance factor (VRM)
K_s	Sampling constant in the inverter feedback loop
k_s, k_p	Tuning factor of the series and parallel resonant branch
k	Interval number of switching period
L_s	Series resonant inductor
L_p	Parallel resonant inductor
L_2	Inductor of 2nd harmonic trap
L_f	Inductor of input filter
L_{lk}	Sum of transformer secondary leakage inductance and parasitic interconnect
	inductance of SR switches reflected to the primary side (VRM)
L_m	Transformer magnetizing inductance
M	Desired phase margin
N	Transformer turns ratio
N_p	Transformer primary winding turns
N_s	Transformer secondary winding turns
N_{SR}	Numbers of paralleled SR switches

n	Order of the harmonic component
P	Phase shift of the control-to-output transfer function
P_{in}	Input power
P_o	Output power
Q_2	Quality factor of the 2nd harmonic trap
Q_{eq}	Quality factor of the equivalent series resonant branch (VRM)
Q_s, Q_p	Quality factor of the series and parallel resonant branch (Inverter)
R_1, C_1	Output filter components of the rectifier in the feedback loop
R_2, R_3	Resistors in the error amplifier
R_{eq}	Equivalent load resistance reflected to the transformer primary side
$R_{ds(on)}$	ON-resistance of MOSFET
R_{load}	Load resistance
S_1, S_2	Chopper switches of the APWM resonant inverter
	Bidirectional ac switches of AC VRM
S	Total active switch stress
SR_1, SR_2	Synchronous rectifier (SR) switches
T_1	Control-to-output transfer function
T_{EA}	Transfer function of the error amplifier
T_{int_pwm}	Transfer function of the integrator and pulse-width modulator
T_p	Transfer function of the power stage
T_{RC}	Transfer function of the feedback sampling network and rectifier
T_s	Switching period
t_{charge}	Charging time of C_{ds} (VRM)

$t_{d(on)}$	Switching turn-on delay time
$t_{d(off)}$	Switching turn-off delay time
t_f	Switching turn-off fall time
t_{on}	ON-time of the gating pulse
U	Total active switch utilization
v_{ac_sw}	Voltage across the ac switch of the AC VRM
v_{ae}	Output voltage of the error amplifier
v_c	Triangular carrier wave in PWM control circuit
V_d	Input dc voltage of the inverter
v_{Ls}, v_{Cs}	Voltage across the series resonant inductor and capacitor respectively
v_{L2}, v_{C2}	Voltage across the inductor and capacitor of 2nd harmonic trap respectively
v_{Ceq}	Voltage across the equivalent series resonant capacitor (VRM)
V_{dc}	Output voltage of the rectifier in the inverter feedback loop
V_{diode}	Voltage drop when the body-diode of the MOSFET is conducting
V_{drop_SR}	Allowable maximum voltage drop across SR
v_{in}	Input ac voltage of the AC VRM
v_{int}	Output voltage of the integrator in the inverter feedforward loop
v_o	Output voltage of the APWM resonant inverter
V_o	Output voltage of the AC VRM
v_p	Voltage across the transformer primary side
V_{ref}	Reference voltage in PWM control circuit
v_{S1}, v_{S2}	Voltage across switch S_1 and S_2 respectively
v_{S2_ac}	AC component of voltage across switch S_2 (Inverter)

V_{S2_ac1}	RMS value of the fundamental component of voltage v_{S2}
V_{sn}	RMS value of the n^{th} harmonic component of voltage v_{S2}
v_{SR}	Voltage across SR switch due to the on-resistance $R_{ds(on)}$ of the switch
Z_s	Impedance of the equivalent series resonant branch (VRM)
Z_{sn}	Impedance of the series resonant branch (Inverter)
Z_p	Total impedance of the magnetizing inductance and equivalent resistance (VRM)
Z_{pn}	Total impedance of the parallel branches including parallel resonant branch, 2^{nd} harmonic trap and equivalent resistance (Inverter)

CHAPTER 1

INTRODUCTION

1.0 INTRODUCTION

The applications of a desktop personal computer (PC) are legion and hardly need elaborating today. Fig. 1- 1 shows the motherboard components of the desktop PC in a block diagram form [1-3].

The main functional units of a computer motherboard include a central processing unit (CPU) module, memory module and I/O interface (or peripheral) modules. These functional blocks can be constructed on a single printed circuit board (PCB, namely as motherboard), or in the limit, within a single Integrated Circuit (IC) package. The CPU is usually contained within a single very large scale integrated (VLSI) circuit, the memory within a bank of VLSI (or LSI) chips, and the I/O interface within a couple of large scale (and/or medium scale) ICs. In addition, the expansion slots allow the installation of some advanced application cards, such as graphic cards and modems. The information is transferred between these functional units by means of the system data bus. All the ICs and VLSI (and/or LSI) chips in each functional unit are powered by the power supplies, and they are all named as loads of the power supplies in this thesis.

Such a computer system has gone through dramatic changes in the last decade to obtain much higher speed, larger capability and more advanced functions. As an indispensable part of such systems, the power aspect in terms of power quality, conversion efficiency, reliability, density and cost is becoming an increasingly important

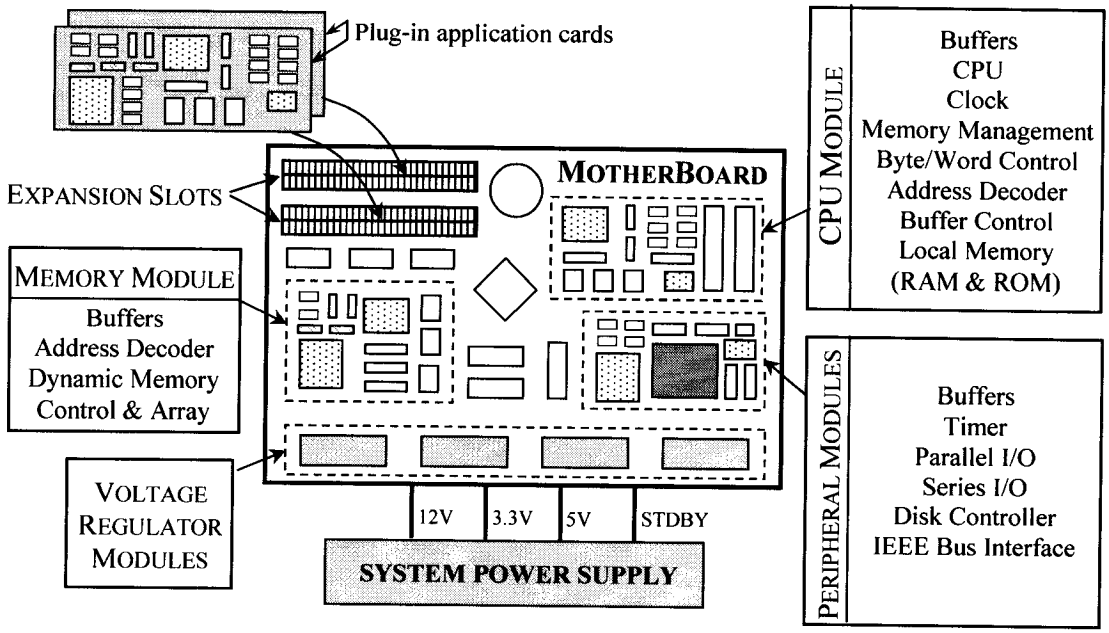


Fig. 1- 1: Block diagram of a desk-top computer motherboard

issue to attain the advanced performance goals of the entire system. The research work of this thesis is based on such motivation.

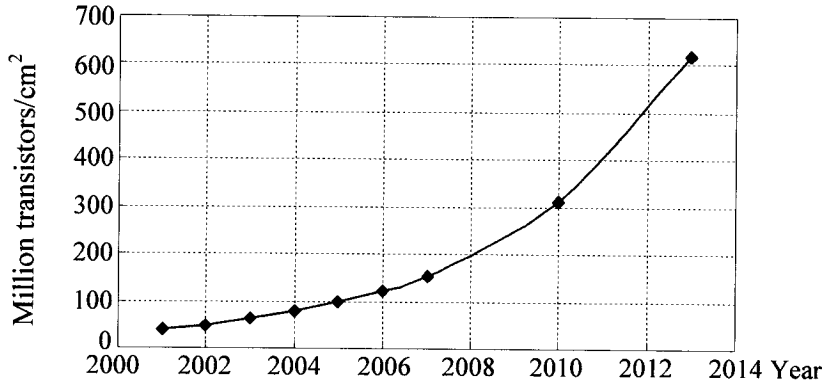
The goal of this chapter is to demonstrate the necessity of developing new power distribution approaches to solve the computer power problems. It starts with the introduction of the growing trends in the semiconductor technology in section 1.1, which bring the new challenges for the power demand presented in section 1.2. Then this chapter explores the drawbacks of the existing dc distributed power system (DC DPS) in section 1.3 and introduces the alternative solution – high frequency ac distributed power system (HFAC DPS) in section 1.4. The introduction of the HFAC DPS includes the architecture description and review of the front-end inverter and the AC voltage regulator module (AC VRM) topologies. The advantages of HFAC DPS over the DC DPS are illustrated in section 1.5. Finally the objectives of this thesis can be concluded in section 1.6, and the outline of this thesis is given in section 1.7.

1.1 GROWING TRENDS IN SEMICONDUCTOR TECHNOLOGY

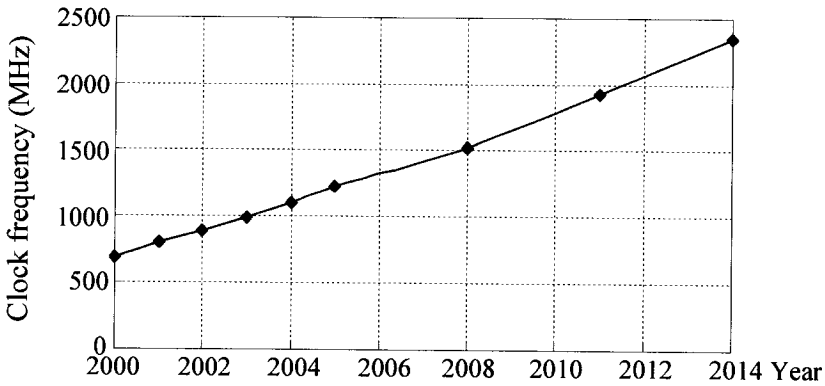
To meet rapid growing demands in data processing capability and data transfer bandwidth, the high performance microprocessors, memories, and application-specific integrated circuits (ASICs) have been benefited from the continuous advances in the semiconductor technology [4-7]. A review of the evolution of the semiconductor technology in the past two decades and a projection into the near foreseeable future shows that the semiconductor technology continues to match the propheey of Moore's law [4].

In this section, only the trends in semiconductor technology relevant to the power issues are discussed, and they are functions/cm^2 (defined as logic transistor density on a single monolithic chip) and ICs internal clock frequency. According to the International Technology Roadmap for Semiconductors (ITRS) 2002 update [5], the trends of these two technology characteristics particularly for the generations of the cost-performance microprocessor unit (MPU) are shown in Fig. 1- 2. It can be seen that in about 10 years, the transistor density in the microprocessor can be up to 620 million/cm^2, and their operating clock frequency will be raised to a few Giga Hertz.

The continuous increasing performance trends in semiconductor technology place significant challenges for thermal management, power delivery, interconnect density, and integration. In this thesis, the technology of power distribution is of the most concern.



(a) Functions/cm^2 (Transistor density)

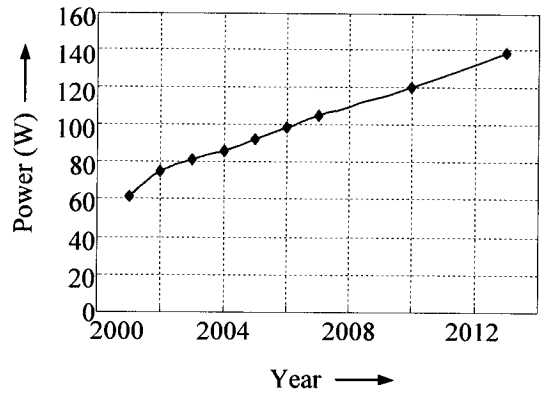


(b) Clock frequency

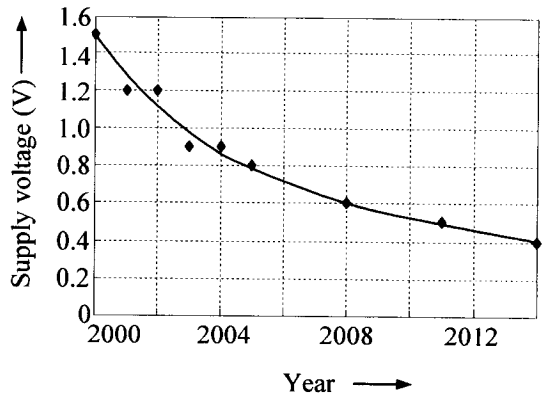
Fig. 1- 2: Growing trends of semiconductor technology (ITRS 2002 update [5])

1.2 NEW CHALLENGES FOR THE POWER DEMAND

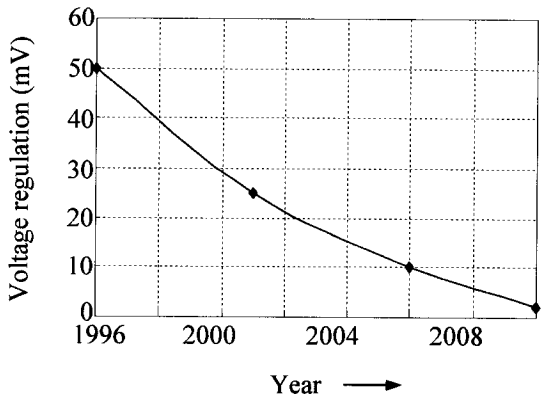
The advances in the semiconductor technology have impacted computer power supply industry significantly. The large growing trends presented in the previous section bring new challenges for the power system and power supply designers [8-23, 39-42]. As shown in Fig. 1- 3, the challenges are from the following six issues: (i) Higher power density; (ii) Lower supply voltage; (iii) Higher power quality; (iv) More multiple regulated supply voltage; (v) Higher supply current; (vi) Very large load transient with very high slew rate (di/dt).



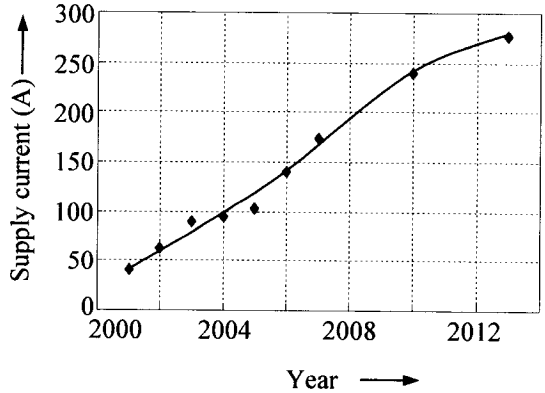
(a) Power consumption



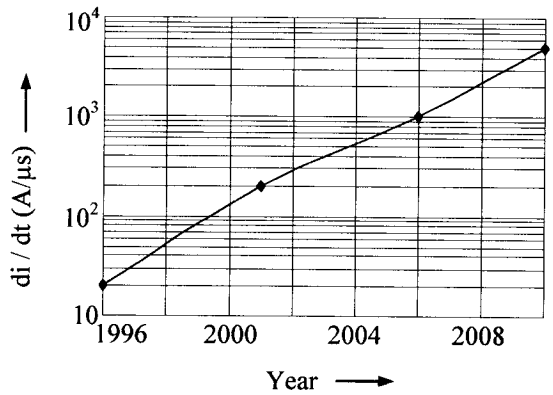
(b) Supply voltage



(c) Power quality



(d) Supply current



(e) Load current slew rate

Fig. 1- 3: Recent trends of the power demand

1.2.1 Higher Power Density

In order to increase PC performance, computer architects increase the clock frequency and increase the number of instructions by adding more parallel execution branches at the cost of increasing power consumption. More transistors increase capacitance and higher operating frequency increases charging and discharging currents. Despite voltage scaling, the net effect is an increase in power consumption over new generations of processors. A look at the trend line shown in Fig. 1- 3 (a), the power doubles approximately every 36 months over the past decade, which is approximately half the pace of the increase in the number of transistors. However, the future trend becomes more moderate.

The cost of higher power consumption associated with packaging, cooling and power delivery has jumped to the forefront in the computer industry. A lot of techniques have been used to reduce the power consumption in microprocessors, such as voltage scaling, clock gating, system power management, and so on. The research work of this thesis focuses on the power delivery approach.

1.2.2 Lower Supply Voltage

As indicated in Fig. 1- 3 (b), the power supply voltage is continuously decreasing. This trend is mainly derived from the consideration of power dissipation. The major source of power dissipation in the processor is the dynamic power loss P_D of all the active gates at any instant-of-time. This power loss is proportional to the product of the clock frequency f_{clk}, gate output capacitance C_{gate} and the square of supply voltage V_{dd}.

Currently, due to the dramatic increase in clock frequency and transistor count, a reduction in supply voltage is the most effective method for reducing dynamic power

loss. This technique is referred to as "voltage scaling". It also allows a reduction of the transistor channel length and a higher reliability of gate dielectrics [2].

1.2.3 Higher Power Quality

In order to ensure the accuracy of high speed data transition, voltage scaling technique requires much tighter tolerance on the power supply under both the steady-state and transient conditions, as shown in Fig. 1- 3 (c). Higher power quality could limit the noise margin in the steady state and voltage drop in the transient response, and eventually prevent ICs from malfunctioning.

1.2.4 More Multiple Regulated Supply Voltages

This power issue is to provide more multiple regulated supply voltages for a circuit board which may use different ICs operating under different supply voltages, or for most advanced ICs, their digital cores may operate at a lower voltage while their I/O and the analog sections operate with a higher supply voltage.

1.2.5 Higher Supply Current

Increased power consumption at lower supply voltages increases the magnitude of the supply current drawn by the CPU, as shown in Fig. 1- 3 (d).

1.2.6 Very Large Load Transient With Very High Slew Rate (di/dt)

To reduce the thermal dissipation in the PC, two approaches are currently being taken to minimize the power consumption. One is to continuously scale down the supply voltage as discussed in section 1.2.1. The second is so called processor "power management". This approach controls a processor into a high or low power stages according to the needs of different applications. Although this approach saves the average

power dissipation of a processor, it imposes an additional requirement of very fast transient response.

The most dramatic load transient occurs in the processor transition from the sleep mode (typical load current ≤1A) to the active mode (typical load current ≥10A) and vice versa. Because of higher operating frequency and higher supply current, this load transient could present much higher slew rate, around 0.5 ~1.0 A/ns currently in a Gaga Hertz circuit, as indicated in Fig. 1- 3 (e).

Typically, there are two voltage drop spikes under transient conditions. The first spike is due to quick power state transition of the processor, on-die power pitch design and processor package parasitic. In this case, local decoupling is absolutely necessary. The second voltage drop, which is concerned in this thesis, is dependent on the local voltage regulator module in terms of topology, switching frequency and control loop design.

In a summary, although the power dissipation in microprocessors has increased steadily over the past decades, future designs are unlikely to continue this trend. In addition, power delivery requirements, such as low supply voltage with tight voltage tolerance and high supply current with large di/dt transients, have also increased steadily. Future trends in this regard may very well continue even if the overall growth in power dissipation becomes more moderate.

Unfortunately, as discussed in the next section, the existing power distribution architecture and power supplies are not always able to follow the roadmap of the PC power demands. Alternative power delivery approaches have to be developed to satisfy the future power requirements.

1.3 PRESENT DC DISTRIBUTED POWER SYSTEM

1.3.1 System Description

The present distributed power system for the desktop computer is in dc domain [13-17]. Its power system block diagram and on-board power configuration are shown in Fig. 1- 4.

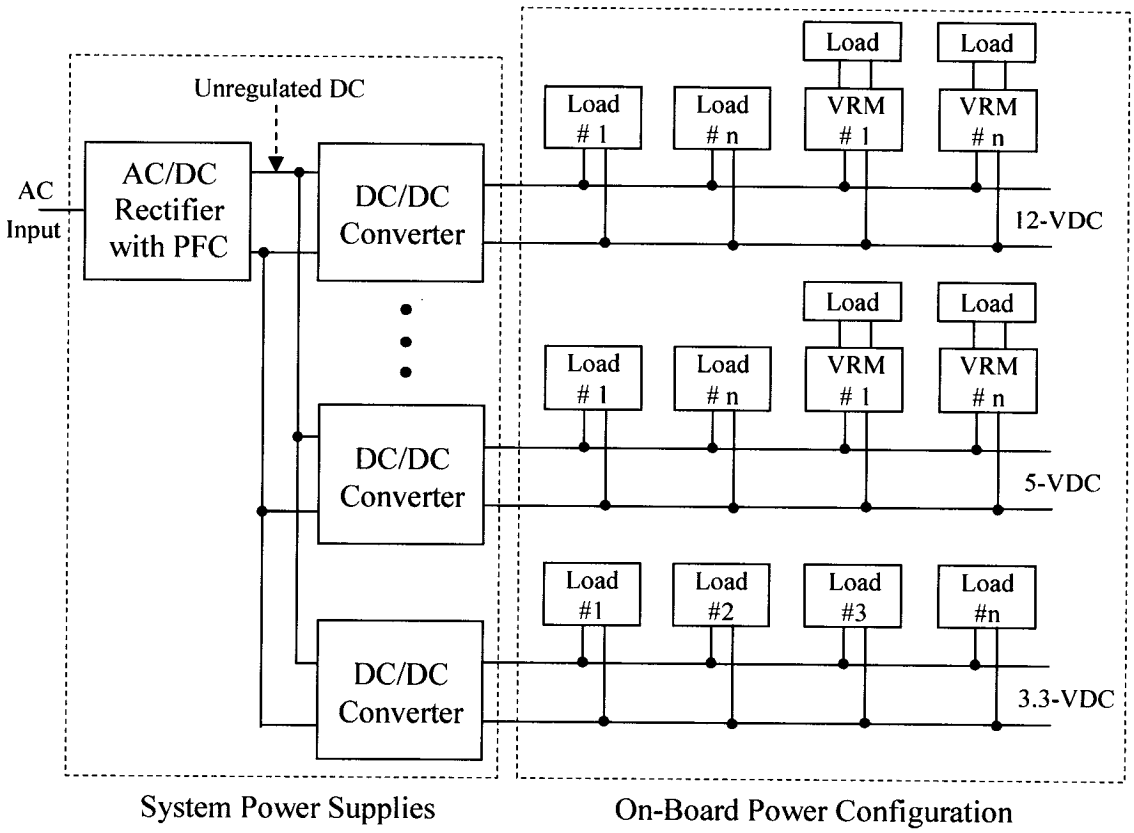


Fig. 1- 4: The existing power distribution frame in the desktop computer

In Fig. 1- 4, the system power supplies perform the following functions:

(i) Line rectification and filtering to generate an unregulated dc voltage;

(ii) Power factor correction (PFC) and input line current harmonic reduction;

(iii) Step-down dc/dc conversion to generate regulated multiple output voltages for the following purposes: (a) provide power for the disk drives that requires 5-V or 12-

V supply and some data processing circuits that require 5-V or 3.3-V supply; (b) provide dc bus distributed on the motherboard. This bus voltage is used as the input voltage of the local (on-board) voltage regulator modules (VRMs) to generate lower dc supply voltage (such as 1.2V, 1.5V, 1.8V, 2.5V) to power microprocessor, memories, and other loads.

The on-board power configuration of Fig. 1- 4 is developed based on the following two considerations:

(i) Lower supply voltages with very tight regulation are required to minimize the power consumption and narrow the noise margin as mentioned in section 1.2.2 and section 1.2.3. Therefore, besides the system power supplies, several voltage regulator modules (VRMs) are very necessary to be distributed in the system to provide lower finely regulated dc supply voltage to the load.

(ii) A major problem for the power distribution is the large load transients with very high slew rate (di/dt) as presented in section 1.2.6. During these large load transients, parasitic impedance of the connection between power supply and its load has a dramatic effect on the power supply output voltage. If this impedance is not low enough, the supply voltage may lose the regulation during the transient and cause the load to shut down or malfunction or even damage the load. As a result, VRMs must be located close to the load. This is known as on-board conversion. A number of decoupling capacitors are also required to provide noise decoupling and to reduce electromagnetic emissions.

1.3.2 Circuit Level Implementation

The circuit level description of the typical complete power system for the desktop computer of Fig. 1- 4 is shown in Fig. 1- 5.

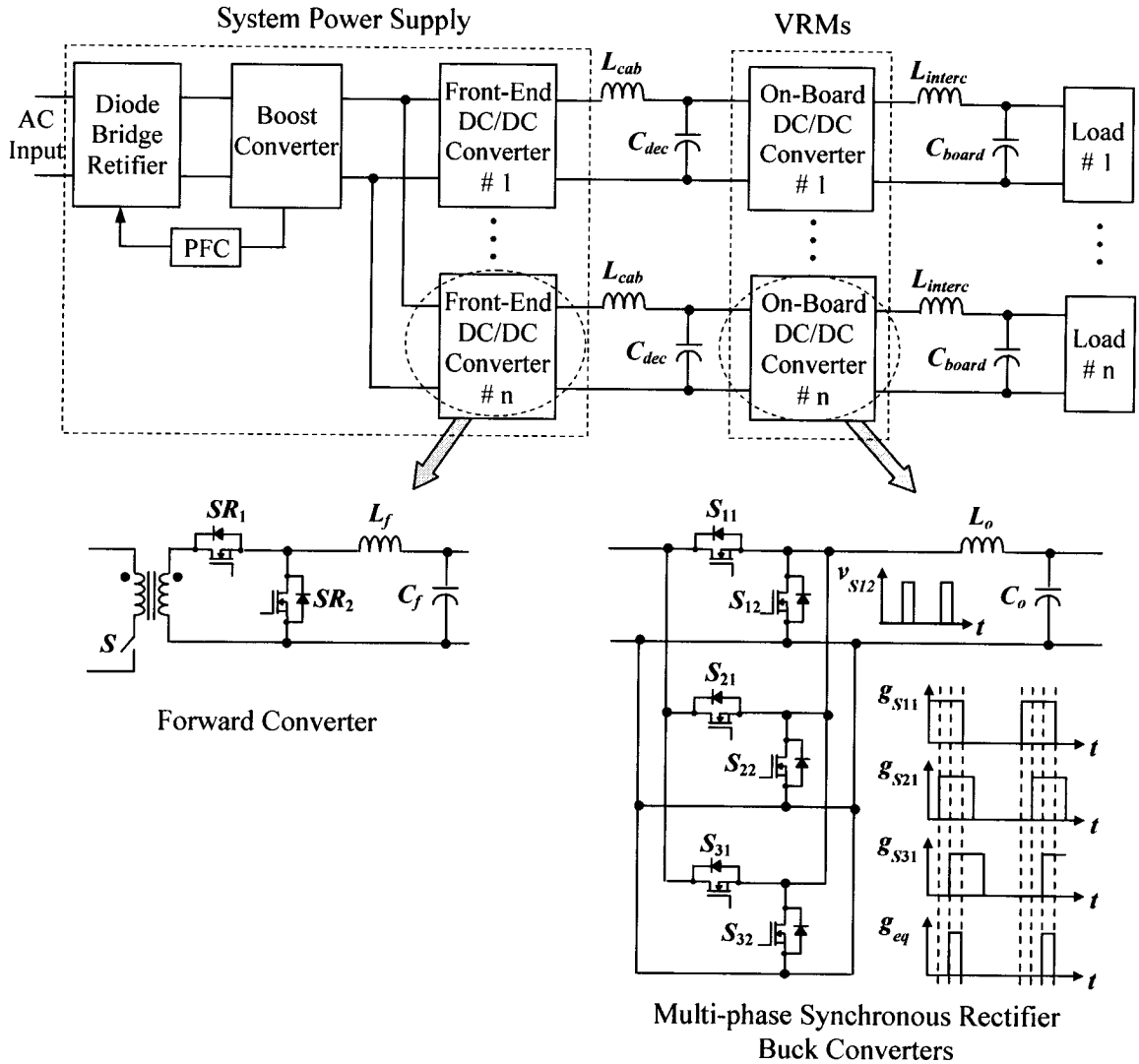


Fig. 1- 5: Circuit level description of the typical complete PC power system in dc domain

In Fig. 1- 5, the system power supply consists of a single-phase diode bridge rectifier to perform the line rectification, a boost converter to provide PFC, and front-end dc/dc converters to generate regulated multiple output voltages. Usually, the power level of the front-end dc/dc converter is below 250W, hence the modified forward topologies with soft switching and simplified transformers are preferred for its implementation [25-30]. Several forward converters are paralleled to provide multiple output voltages to be distributed.

Since the system power supply is connected to the motherboard by relatively long cables, its inductance L_{cab} is decoupled with capacitor C_{dec}. As explained in the section 1.3.1, the interconnect inductance L_{interc} between VRM and the load needs to be decoupled with on-board capacitance C_{board}.

Since the galvanic isolation is provided by the transformer of the system power supply, on-board VRMs do not need to be isolated. Consequently the simplest non-isolated step-down topology – the buck converter [25] can be used to implement the VRMs. Most of today's VRMs use synchronous rectifier buck topology [17, 31-37], as shown in Fig. 1- 5, to improve the converter efficiency at full load. However, the buck converter must operate with very small duty cycle to supply low voltage and high current, and the instantaneous peak power dissipated in the MOSFET becomes very high. Therefore, in Fig. 1- 5, several multi-phase synchronous rectifier buck converters need to be paralleled to form one VRM. The top switches (S_{11}, S_{21}, and S_{31} in Fig. 1- 5) are sequenced to turn on with relatively high duty cycle, but the effective duty cycle is small.

1.3.3 System Features

In the early days, time of Intel486^{TM} processor for example, the lowest supply voltage level of any component in a desktop PC was 5V. With low current demand (about 1A), it was not a problem to directly power the processor, memories and other circuit boards with centralized power system. Then in 90s, the dc distributed power system took over. Because of the low level voltage ($\leq$3.3V) required by the PC system components, local VRMs have to be added to a system platform.

Compared with the old centralized power system, the existing distributed power system has the following advantages:

(i) Heat produced by the power conversion is distributed through the whole system;

(ii) Voltage regulation for the on-board load provided by the local VRM is excellent;

(iii) The distribution losses are minimized since lower current is distributed, and the motherboard also becomes simple because of removal of high current rails;

(iv) There is less noise to disturb sensitive circuits due to the absence of the large ground loop existing in the centralized architecture;

(v) The failure group is the smallest, as a failed VRM does not affect the operation of other loads.

However, the present power distribution architecture still can not satisfy the future power demands for the desktop PC application due to the following reasons:

(i) Multiple dc/dc conversion stages (dc/ac/dc) must be used in the front-end converters resulting in low overall efficiency. This problem is even worse when multi modules are used to provide multiple outputs.

(ii) Distributed input filters are required for isolation from converter interaction and they are sensitive to impedance instability.

(iii) Current limiting circuit in each converter is needed.

(iv) More components, filters and converters add a high cost to the system, take a large board space, and lower the system efficiency and reliability, especially when more multiple supply voltages are required.

Furthermore, the VRM topologies employed in the existing distributed power system have the following major disadvantages for the future application:

(i) Several multi-phase synchronous rectifier buck converters need to be paralleled to form one VRM. For the future application with the demand of higher output

power, lower output voltage and higher current, even more multi-phase buck converters are required to be paralleled to form one VRM. This solution becomes very inefficient. The only efficient way to perform the power conversion with a large step-down ratio is to use a topology with a step-down transformer. Then again, multiple dc/dc conversion stages (dc/ac/dc) must be involved in the isolated VRM.

(ii) The low pass LC filter at the output of the VRM cannot meet the stringent dynamic regulation requirements. The output inductor becomes an open circuit facing to the large load transient with very high slew rate, and slow down the circuit transient response. Consequently, more output capacitors and decoupling capacitors are needed to maintain the output voltage during the transient. However this choice is very limited by the precious on-board space.

(iii) The synchronous rectifier buck converter has low efficiency at light load. However, with the system power management, VRMs are expected to further reduce the power consumption at light load in order to extend the battery operation time in the portable systems or to facilitate the compliance with various "energy star" ("green" power) requirements in the office systems.

Therefore, many research works have been done for an improved power distribution scheme, which could provide all the advantages of the existing dc power distribution, but at fewer components, lower cost, smaller size, higher efficiency and higher reliability. A new technique, high frequency ac power distribution, was introduced in [39] as an alternative solution for powering the new generations of computer system.

1.4 ALTERNATIVE HIGH FREQUENCY AC DISTRIBUTED POWER SYSTEM

1.4.1 System Architecture

The concept of high frequency AC distributed power system (HFAC DPS) was first proposed by NASA some 30 years ago for space applications [38]. Since then a number of industry have been working on this new powering scheme for other applications [39-46]. The basic configuration of the HFAC distributed power system is shown in Fig. 1- 6.

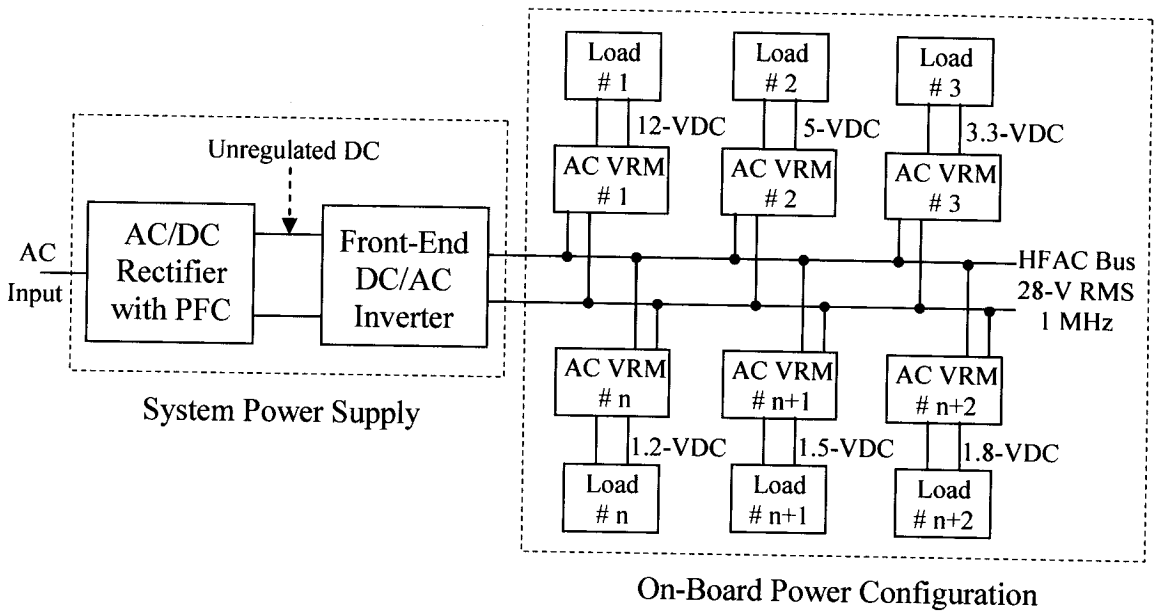


Fig. 1- 6: High frequency AC power distribution

In Fig. 1- 6, the system power supply performs the following functions:

(i) Line rectification and filtering to generate an unregulated dc voltage;

(ii) PFC and input line current harmonic reduction;

(iii) Low frequency ac to high frequency ac conversion to generate HFAC distribution.

Since the power stages of line rectification with PFC are the same as the present distributed power system in dc domain, they will not be discussed in the following sections. The input of the ac distributed power system will be seen as dc voltage.

In HFAC power distribution architecture of Fig. 1- 6, the front-end inverter converts the dc input voltage to high frequency (hundreds KHz to a few MHz) and high ac voltage (28 Vrms) to be distributed on the PC motherboard. Then on-board AC VRMs convert this ac voltage to the specific dc voltage to power the microprocessor, memories, and I/Os. When the supply voltage of 12-V DC or 5-V DC is required to power I/O loads, a simplified AC VRM without voltage regulation circuit – a series resonant converter with diode rectifier can be used [40]. However, when low level voltage (1.1V-1.8V DC) with very tight voltage regulation is required to power microprocessor and memories, the AC VRM must be implemented with a voltage regulation circuit. This type of AC VRM and the front-end inverter are the research objects of this thesis.

1.4.2 Selection of the High Frequency Front-End Inverter

To satisfy the power demands for the future desktop PC applications, the high frequency front-end inverter is expected to have the following features:

(i) High conversion efficiency from low-load to full-load;

(ii) Tight output voltage regulation under the steady-state and dynamic conditions;

(iii) Very low total harmonic distortion (THD) at the output;

(iv) Constant operating frequency;

(v) Low EMI.

A number of different topologies have been reported, but they appear to fail to satisfy all the requirements simultaneously [47, 48], or require complicated power and

control circuitry [49, 50]. Only the resonant inverter [51-53], as shown in Fig. 1- 7, can achieve all the design objectives with simple control method.

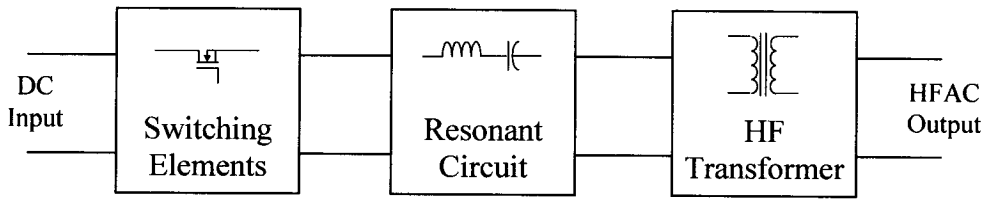


Fig. 1- 7: Circuit block diagram of the high frequency front-end inverter

This resonant inverter consists of three basic functional blocks: switching elements, resonant circuit and high frequency transformer. The switching elements are controlled by the pulse-width-modulated (PWM) gating signals. They can be full-bridge to generate quasi-square wave voltage for medium-to-high power applications, or a chopper circuit to generate unidirectional voltage for low power applications. Then this voltage is fed to a resonant circuit to generate resonating sinusoidal voltage and/or current. In the resonant circuit, to form a voltage type distribution, a parallel resonant branch must be used. To achieve high conversion efficiency from low-load to full-load, the series-parallel resonant circuit is preferred. At the output of the inverter, a high frequency transformer is used to provide output voltage matching and isolation.

1.4.3 Selection of the AC Voltage Regulator Module (AC VRM)

The on-board AC/DC converters, known as AC VRM, are used to convert high frequency ac voltage to the specific low dc voltage. To satisfy the power demands for the future desktop PC applications, the main design objectives for these converters are:

(i) High conversion efficiency from low-load to full-load;

(ii) Output voltage control from no-load to full-load;

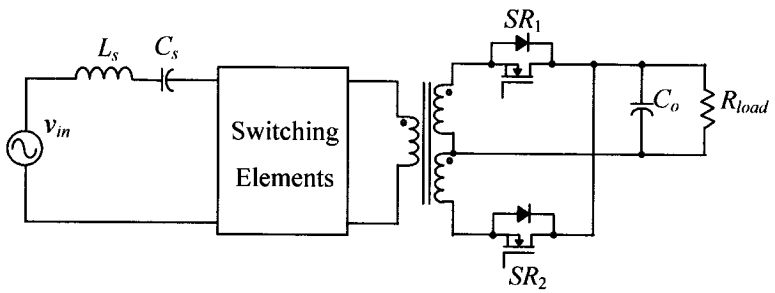
(iii) Tight output voltage regulation under steady-state and dynamic conditions;

(iv) Close-to-unity power factor (PF) and low THD in the input current;

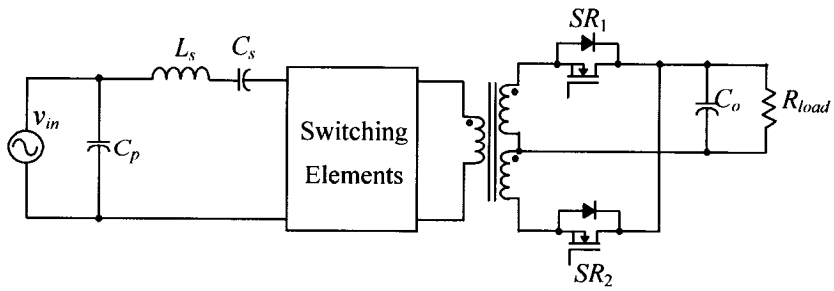
(v) Low mass and volume;

(vi) Low EMI.

To achieve objective (i), synchronous rectifier is used in the rectification stage, and all the switches employed in the VRM must operate with soft switching. To achieve objective (ii), the operating frequency must be constant, which allows voltage regulation at no-load with a proper control scheme [55-57]. To achieve objective (iii), especially to keep the output voltage regulation under the large load transient with very high slew rate (di/dt), only the simplest capacitive filter is allowed. To achieve objective (iv), a resonant circuit must be added between the ac voltage source and the rectifier [54]. According to these design considerations, two HFAC VRM topologies are currently available. The circuit block diagrams are shown in Fig. 1- 8.



(a) Series resonant VRM



(b) Parallel-series resonant VRM

Fig. 1- 8: Circuit block diagrams of the AC VRM topologies

The topology shown in Fig. 1- 8 (a) can be referred as series resonant VRM, and the topology shown in Fig. 1- 8 (b) can be referred as parallel-series resonant VRM. Both topologies have the following main advantages:

(i) Voltage regulation from no-load to full-load. Control techniques with constant operating frequency permit voltage regulation at no-load;

(ii) High conversion efficiency from low-load to full-load;

(iii) Fast transient response but with the trade-off of high current ripple in the output capacitor;

(iv) Input current with close-to-unity PF and low THD;

However, as compared to the series resonant VRM, the parallel-series resonant VRM has circulating current, and besides, higher no-load current (no-load current is zero in the series resonant VRM) and component count. Consequently, lower efficiency and higher total volt-ampere rating are resulted in the parallel-series resonant VRM topology. Therefore, the series resonant VRM topology is the preferred candidate for AC VRM in most HFAC DPS applications, as desktop computer for example.

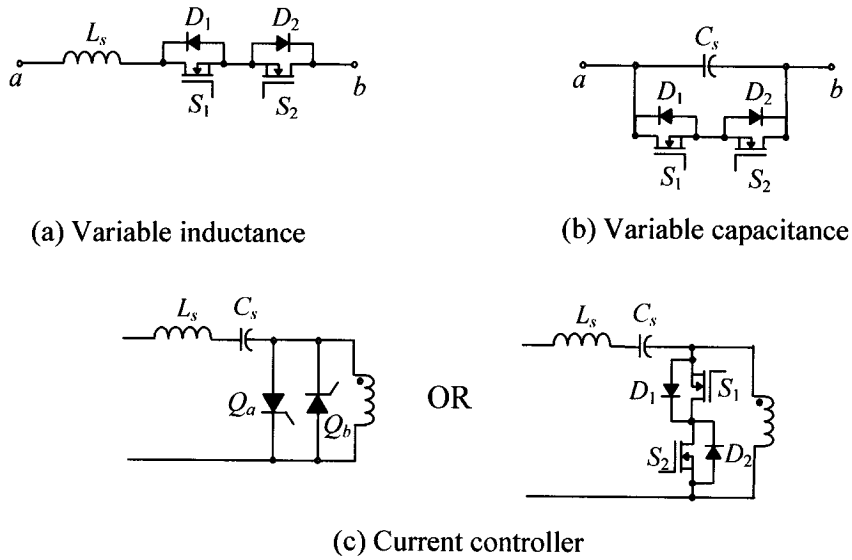
The parallel-series resonant VRM topology is only preferred in the applications with very sensitive equipment, because it has better performance in terms of PF and THD of the input current drawn from the ac bus. This advantage minimizes the harmonic currents injected into the ac bus, and thereby minimizing the electromagnetic interference with the sensitive equipments.

To implement the switching elements in Fig. 1- 8 to achieve the voltage regulation at the output of the series resonant VRM, three control approaches with constant operating frequency have been proposed [58-64]:

(i) Changing resonant frequency with variable inductance [58, 60, 61];

(ii) Changing resonant frequency with variable capacitance [58, 59];

(iii) Controlling the amount of the rectified current with a current controller [62-64].



(a) Variable inductance

(b) Variable capacitance

(c) Current controller

Fig. 1- 9: Control methods of the series resonant VRM

In approach (i), the variable inductance can be implemented by controlling the amount of the current flowing through the inductor, which requires a bidirectional switch connected in series with the inductor, as shown in Fig. 1- 9 (a). The control signal of S_1 is synchronized with the voltage v_{ab} with a control angle α varied from $\pi/2$ to π, and the control signal for S_2 is the complement of that for S_1. Although the switches operate with soft switching, it still has the following two main drawbacks:

(1) Discontinuous input current results in higher THD and lower PF;

(2) Due to the complementary gating signals of S_1 and S_2, full input current has to flow through either diode D_1 or diode D_2. This fact results in more conduction losses and consequently the lower efficiency.

In approach (ii), the variable capacitance can be implemented by connecting a bidirectional switch in parallel with the capacitor, as shown in Fig. 1- 9 (b). The control signal of S_2 is synchronized with the input current i_{ab} with a control angle α varied from $\pi/2$ to π, and the control signal for S_1 is the complement of that for S_2. Although this approach has the advantage of continuous input resonant current over the approach of the variable inductance, and the switches operate with soft switching, it still suffers from the following two main drawbacks:

(1) The gating signals are synchronized with the input current which is highly distorted at light load and it needs additional current sensing transformer;

(2) The same as drawback (2) of variable inductance approach.

Approach (iii) can be implemented by connecting a bidirectional switch as a current controller in parallel with the primary winding of the transformer, as shown in Fig. 1- 9 (c). However, the main disadvantage of this approach is that the phase-angle-controlled switches operate with hard switching, witch is not tolerable for the applications of very high operating frequency.

Therefore a new control approach with the following features is desired for the applications of very high frequency series resonant VRMs:

(i) Soft switching can be achieved from low-load to full-load;

(ii) The gating signals are synchronized with the input voltage of the VRM, which is assumed to be a pure sinusoidal voltage source;

(iii) Less conduction time for the anti-parallel diodes of the bidirectional switches, which results in less conduction losses;

(iv) Continuous input resonant current.

1.5 COMPARISON OF DISTRIBUTED POWER SYSTEM IN DC DOMAIN AND AC DOMAIN

The high frequency ac distributed power system (HFAC DPS) has been introduced for the applications of the desktop PCs. This alternative power solution not only possesses the advantages of the existing dc distributed power system (DC DPS) but also brings new features which are technically impossible in dc domain. The main advantages of this HFAC DPS over the present DC DPS are discussed as follows.

(i) Reduced number of components and reduced power conversion stages as shown in Fig. 1- 10.

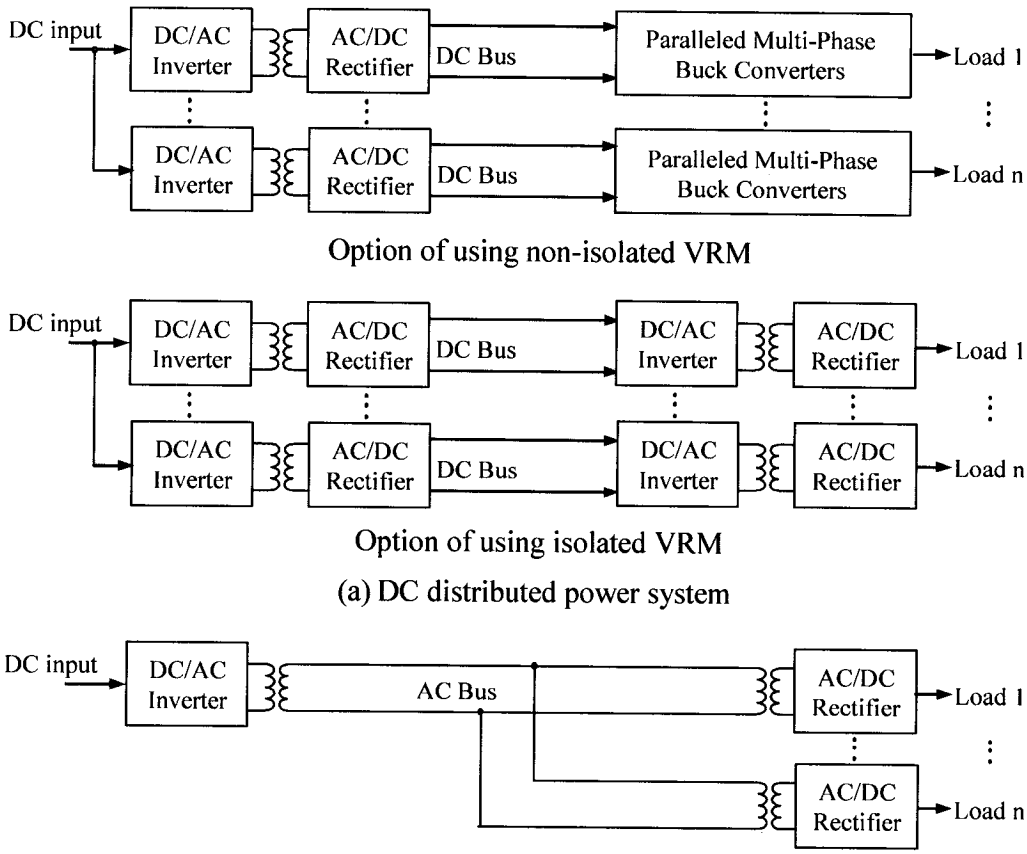


Fig. 1- 10: Power conversion stages in the distributed power system

For the front-end converter, the rectification step in the front-end dc/dc converter of DC DPS can be eliminated in AC DPS. For the VRMs, if non-isolated multi-phase buck converters are used in DC DPS, DC VRM has much higher components count than the AC VRM. If the isolated dc/dc converter is used as DC VRM, the rectification step in the DC VRM can be eliminated in AC VRM. Therefore the HFAC DPS has potentially higher efficiency, lower cost, smaller size, and better reliability.

(ii) Excellent transient response.

For a properly designed wide-bandwidth feedback control, the large-signal transient response of VRM is mainly determined by the response of output filter [17]. Because of no low-pass LC filter presented at the output of the AC VRM and very high operating frequency, the feedback loop in ac domain can be closed at much higher frequency than in the case of dc domain. Compared to the conventional VRM, the AC VRM could have the transient recovery time (t_{trans}) and the output capacitance (C_o) reduced by at least a factor of 10 respectively (t_{trans} =a few ten to a few hundred μs and C_o = 5000 to 8000 μF in DC VRM, and t_{trans} = a few to a few ten μs and C_o = 500 to 800 μF in AC VRM). This feature can improve the voltage regulation under the dynamic conditions and power density of the VRM significantly.

(iii) High efficiency from low-load to full-load.

The series-parallel resonant tank employed in the front-end inverter and the series resonant tank employed in the AC VRM all have the advantage of maintaining high efficiency independently of load conditions. This feature is essential for the PCs with system power management.

(iv) Simple current limit.

The resonant circuits which are incorporated in both front-end inverter and AC VRM provide inherent short-circuit protection at the power interface (fuse-less protection) and limited power transfer to the load (elimination of fire hazard). In other applications of the telecommunication systems and mainframe-level computer systems, the inrush current can be limited without any other additional circuits if "hot insertion" of the system card is required.

(v) Active energy steering.

The energy corresponding to the positive load current step must be provided by the power delivery system. During the negative current step, however, energy could be either stored and or damped. Damping, which is the only solution for the DC VRM, is technically the simplest but results in poor efficiency. In HFAC DPS, the excess energy can easily be steered to high frequency bus side to be stored in the resonant tank, and then be re-used when needed.

(vi) Reduction of thermal stress.

This is because less power conversion stages are required, and higher voltage and lower current are distributed through the ac bus. This feature may allow the system to operate with convection cooling rather than the forced air cooling, and increase the system reliability as well.

1.6 THESIS OBJECTIVES AND METHODOLOGIES

The high frequency ac distributed power system has been introduced in this chapter for the applications of the desktop PCs. The main objective of this thesis is to develop and implement such a power system, and it can be detailed as:

(i) To develop an improved series-parallel resonant inverter topology to be used as the front-end inverter;

(ii) To develop an improved series resonant converter topology to be used as the on-board AC VRM;

(iii) To present the system performance with the implementation of the proposed front-end inverter and on-board AC VRMs.

The proposed topologies must possess the desired features defined in sections 1.4.2 and 1.4.3 for inverter and AC VRM respectively. To achieve the main objectives, the following methodologies are used for developing each topology:

(i) Perform steady-state and dynamic analyses;

(ii) Present performance characteristics under both the steady-state and dynamic conditions;

(iii) Develop design procedures;

(iv) Provide simulation and experimental results for the proof-of-concept.

1.7 THESIS OUTLINE

The outline of the rest part of this thesis is as follows.

Chapter 2 presents an asymmetrical pulse-width-modulated (APWM) inverter to be used as the front-end inverter. The proposed topology could operate in three distinct modes, and the preferred mode of operation is derived. The steady-state analysis is carried out to illustrate the significant performance characteristics. The dynamic properties of the proposed inverter are investigated as well. Based on the dynamic analysis, a control scheme made with the combination of the modulated integral

feedforward control and the feedback control is employed. The simulation and experimental results are presented to verify the theoretical analysis.

Chapter 3 presents a series resonant converter topology to be used as an AC VRM. This topology employs a new control approach with the desired features which can overcome all the drawbacks of the existing control approaches described in section 1.4.3. The main switch in this topology can be controlled by either phase-shift-modulation or pulse-width-modulation (PWM). The steady-state analysis shows that the pulse-width-modulated AC VRM is expected to have higher efficiency than the phase-shift-modulated AC VRM. Therefore, the dynamic analysis is performed only for the pulse-width-modulated AC VRM. The simulation and experimental results are presented to provide the proof-of-concept.

Chapter 4 develops the design procedure for the APWM resonant inverter and the series resonant AC VRM based on the analyses of Chapter 2 and Chapter 3. Besides this, the design considerations from the system point of view are also discussed. Furthermore, the system implementation using the proposed APWM resonant inverter and the series resonant AC VRMs is presented. As a result, the system performance under both the steady-state and dynamic conditions is simulated, and the simulation results prove the analyses, design and implementation.

In Chapter 5, conclusions and contributions of this thesis are summarized, and the suggestions for the future work are proposed.

CHAPTER 2

AN ASYMMETRICAL PULSE-WIDTH-MODULATED (APWM) RESONANT INVERTER

2.0 INTRODUCTION

This chapter presents an asymmetrical pulse-width-modulated (APWM) resonant inverter to provide sinusoidal voltage and current distribution for HFAC distributed power system applications. This inverter includes a chopper to convert the dc input voltage to a high frequency unidirectional ac voltage, which in turn is fed to a high-frequency transformer through a series-parallel resonant circuit. The output voltage of the inverter is controlled at a desired level against any input line and output load variation. This inverter exhibits very low total harmonic distortion at the sinusoidal output, and near-zero voltage switching losses while operating at constant and very high frequency.

In this chapter, to understand the performance of the proposed APWM inverter, detailed analyses are carried out. The contents of this chapter can be outlined as:

In section 2.1, the APWM inverter topology is proposed. The circuit diagram and the operating principles are described.

In section 2.2, the steady-state analysis of the APWM inverter is performed to present: (i) output voltage control; (ii) harmonic analysis of the input current and output voltage; (iii) voltage and current of the main circuit variables.

In section 2.3, the performance curves for the APWM inverter are developed for the design purposes.

In section 2.5, a control scheme including feedforward and feedback control for the proposed inverter is derived, and the dynamic performance of the proposed APWM inverter is presented.

Finally, simulation and experimental verification of the theoretical analyses are given in section 2.6.

2.1 PROPOSED APWM RESONANT INVERTER TOPOLOGY AND ITS OPERATION

In this section, an APWM inverter topology is proposed. The circuit diagram is described in section 2.1.1. This inverter could operate in three distinct operation modes depending on the relationship of the resonant frequency to the operating frequency. The preferred operation mode is derived in section 2.1.2, and its operating principle is illustrated in section 2.1.3.

2.1.1 Proposed APWM Resonant Inverter Topology

The circuit diagram of an APWM resonant inverter and its variable designations are shown in Fig. 2- 1. The proposed APWM inverter consists of a chopper, a series-parallel resonant circuit, a 2^{nd} harmonic trap, and a high-frequency transformer.

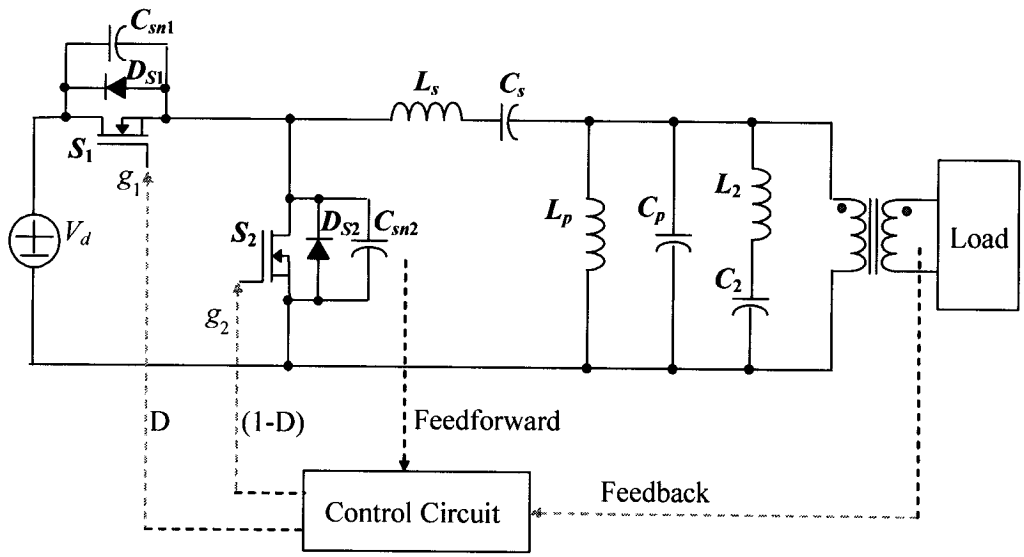
The chopper converts input dc voltage into a high frequency unidirectional voltage at its output. The resonant circuit, which consists of a series branch and a parallel branch, has the following functions:

(i) It converts the unidirectional voltage into resonating series current and parallel voltage;

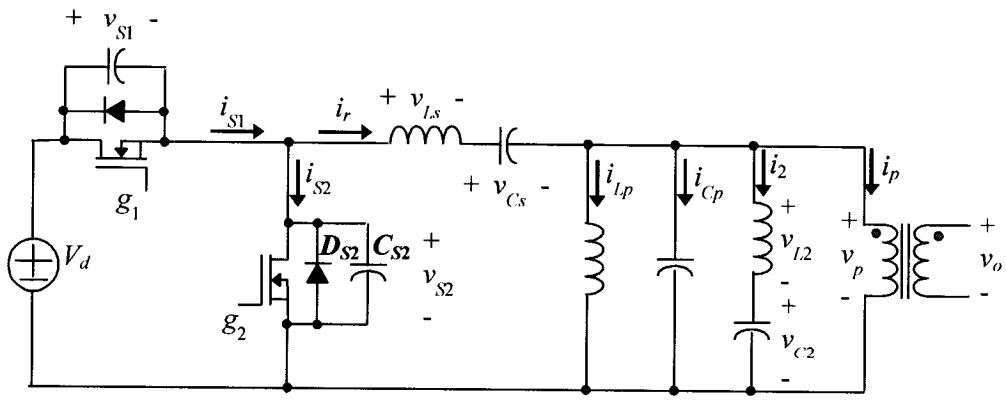
(ii) It provides zero-voltage switching (ZVS) for the inverter switches, and

(iii) It blocks dc component of the unidirectional voltage from passing to the high-frequency transformer.

The high-frequency transformer provides matching and isolation for the output of the inverter. The feed-forward and feedback control loops are employed to achieve fast transient response against the line and load variations.



(a) Circuit diagram



(b) Circuit variable designations

Fig. 2- 1: The proposed APWM resonant inverter

2.1.2 Modes of Operation

The proposed APWM inverter operates at constant frequency. To achieve maximum power transfer, the series resonant branch is tuned at the operating frequency of the inverter, so that this branch provides zero impedance at the operating frequency. The parallel resonant branch can be either tuned or off-tuned at the operating frequency. Therefore, depending on the relationship of the resonant frequency of the parallel branch ω_p to the operating frequency of the inverter ω_o, there are three distinct operation modes:

(a) Mode A: $\omega_p = \omega_o$,

(b) Mode B: $\omega_p < \omega_o$, and

(c) Mode C: $\omega_p > \omega_o$.

2.1.2.1 Mode A: $\omega_p = \omega_o$

The operating waveforms of this mode of operation are shown in Fig. 2- 2. At the beginning of interval II, the current is transferred from diode D_{s2} to switch S_2 resulting in turn-on switching under zero voltage. At the beginning of interval III, the current is transferred from switch S_2 to diode D_{s2} resulting in turn-off switching under zero voltage. But at the beginning of interval IV, the current is transferred from diode D_{s2} to switch S_1 resulting in turn-on switching under full input voltage. The turn-off for switch S_1 at the beginning of interval I can be under near-zero-voltage if large snubber capacitor is placed across it and enough dead time is allowed between the gating signals of S_1 & S_2. In addition, the circulating current flowing through the switches is minimized since both the series and parallel resonant branches are tuned at the operating frequency, which results in low conduction losses.

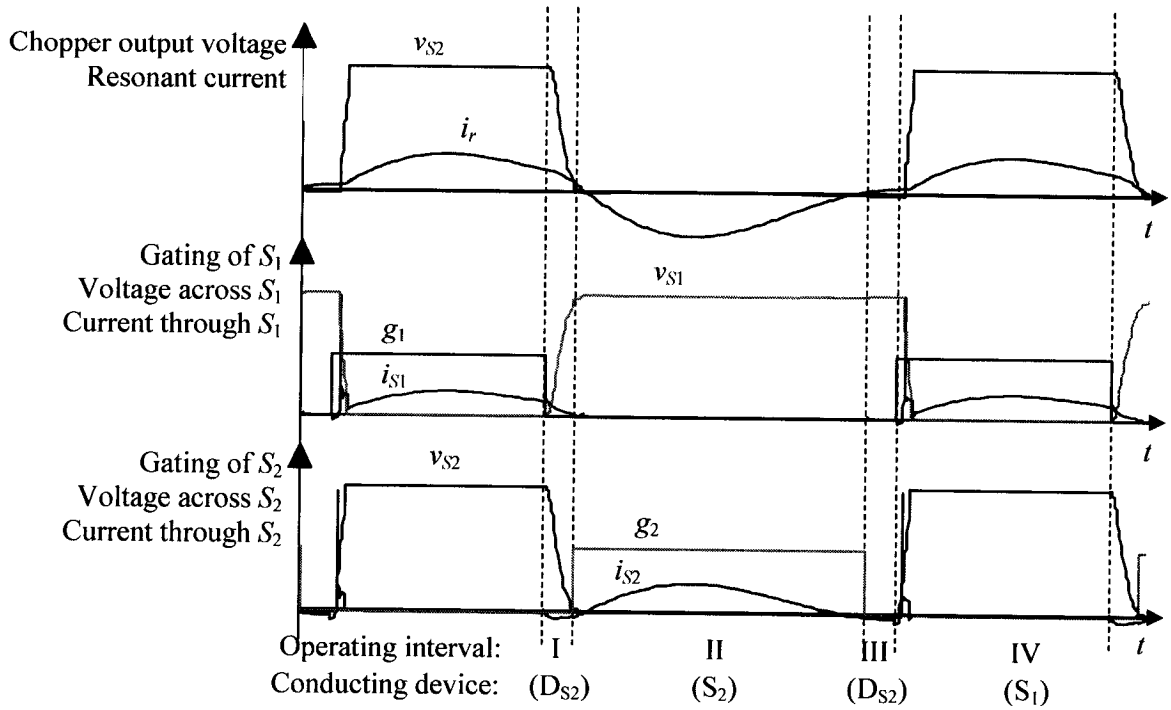


Fig. 2- 2: Operating waveforms of Mode A

2.1.2.2 Mode B: $\omega_p < \omega_o$

In this mode of operation, the parallel resonant branch presents a capacitive impedance at the operating frequency, and the resonant current leads the output voltage of the chopper. As shown in Fig. 2- 3, at the beginning of interval II and interval IV, the current is always transferred from the switch to its own body diode resulting in turn-off switching under zero voltage. But at the beginning of interval I and interval III, the current is always transferred from the body-diode of one switch to another switch resulting in turn-on switching under full input voltage. Meanwhile the circulating current flowing through the switches is high increasing both switching losses and conduction losses.

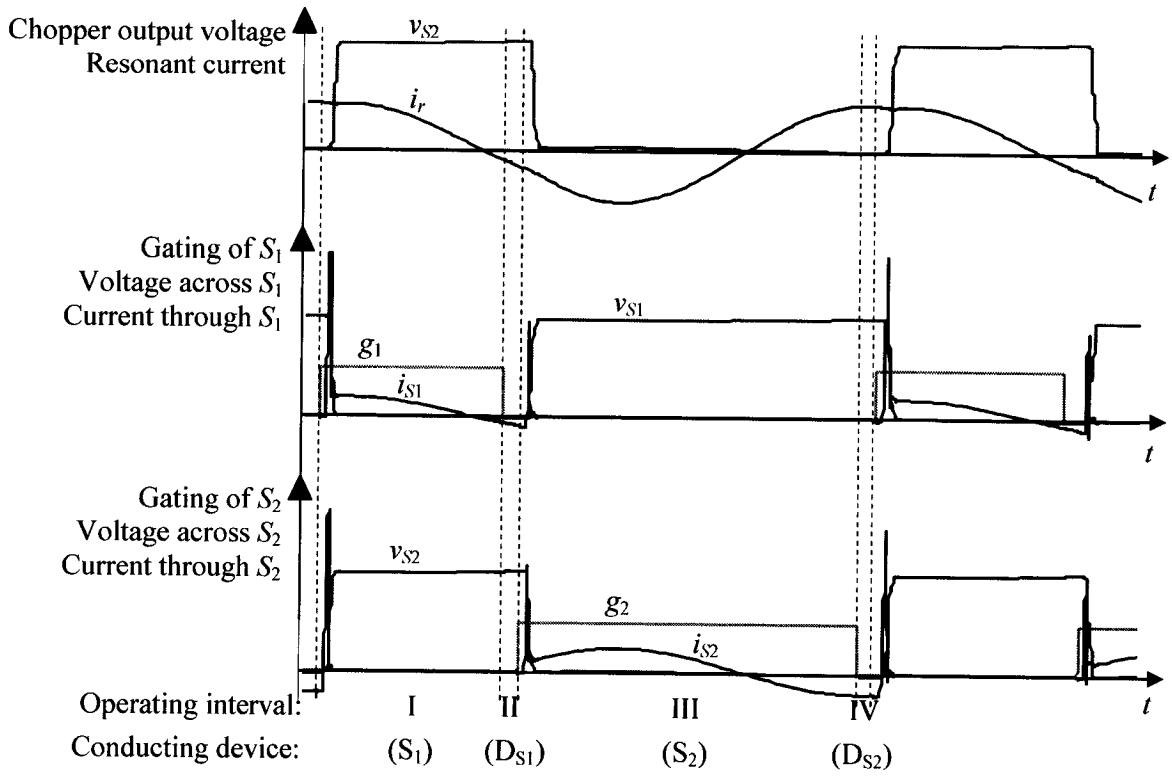


Fig. 2- 3: Operating waveforms of Mode B

2.1.2.3 Mode C: $\omega_p > \omega_o$

In this mode of operation, the parallel resonant branch provides an inductive impedance at the operating frequency, and the resonant current lags the output voltage of the chopper. This feature allows ZVS at turn-on for both switches S_1 and S_2 because the current is always transferred from the body diode to the switch. Furthermore, ZVS can also be achieved at turn off for both switches if large snubber capacitors are placed across the switches and enough dead time is allowed between the complementary gating signals of these two switches. Detailed operating principle will be explained in the next section.

From the above discussion, it is clear that the operation of mode B is very inefficient and the inverter should never be designed to operate in this operation mode. Operation of mode A has the minimum conduction losses and soft switching of one

switch. However, there is always turn-on loss for another switch. For the application of HFAC distributed power systems, the operating frequency is in the range of MHz where frequency dependent losses are dominant. Therefore, operating mode C is preferred since it has near zero switching losses for both switches employed in the chopper.

2.1.3 Operating Principle of the Preferred Operation Mode

Fig. 2- 4 shows the key operating waveforms of the proposed inverter of Fig. 2- 1. For each switching cycle, the inverter operates in the following 4 intervals. The active current path in each interval is shown in Fig. 2- 5.

Interval I:

The active current path during interval I is shown in Fig. 2- 5(a). At the beginning of this interval, switch S_2 is turned off. Because of the negative resonant current, capacitor C_{sn1} starts to discharge into the resonant circuit. Once the voltage across C_{sn1} reaches zero, the negative resonant current forces the anti-parallel diode D_{S1} to conduct.

Interval II:

The active current path during interval II is shown in Fig. 2- 5(b). At the beginning of this interval, switch S_1 is turned on under zero voltage and a positive voltage V_d appears at the output of the chopper. Power flows from dc input to the resonant circuit and to the output load.

Interval III:

The active current path during interval III is shown in Fig. 2- 5(c). At the beginning of this interval, switch S_1 is turned off. Because of the positive resonant current, capacitor C_{sn2} starts to discharge. Once the voltage across capacitor C_{sn2} reaches zero, the positive resonant current forces the anti-parallel diode D_{S2} to conduct.

Interval IV:

The active current path during interval IV is shown in Fig. 2- 5(d). At the beginning of this interval, switch S_2 is turned on under zero voltage and the output voltage of the chopper is clamped to zero. The energy stored in the resonant circuit during interval II now freewheels through S_2 and keeps supplying power to the load.

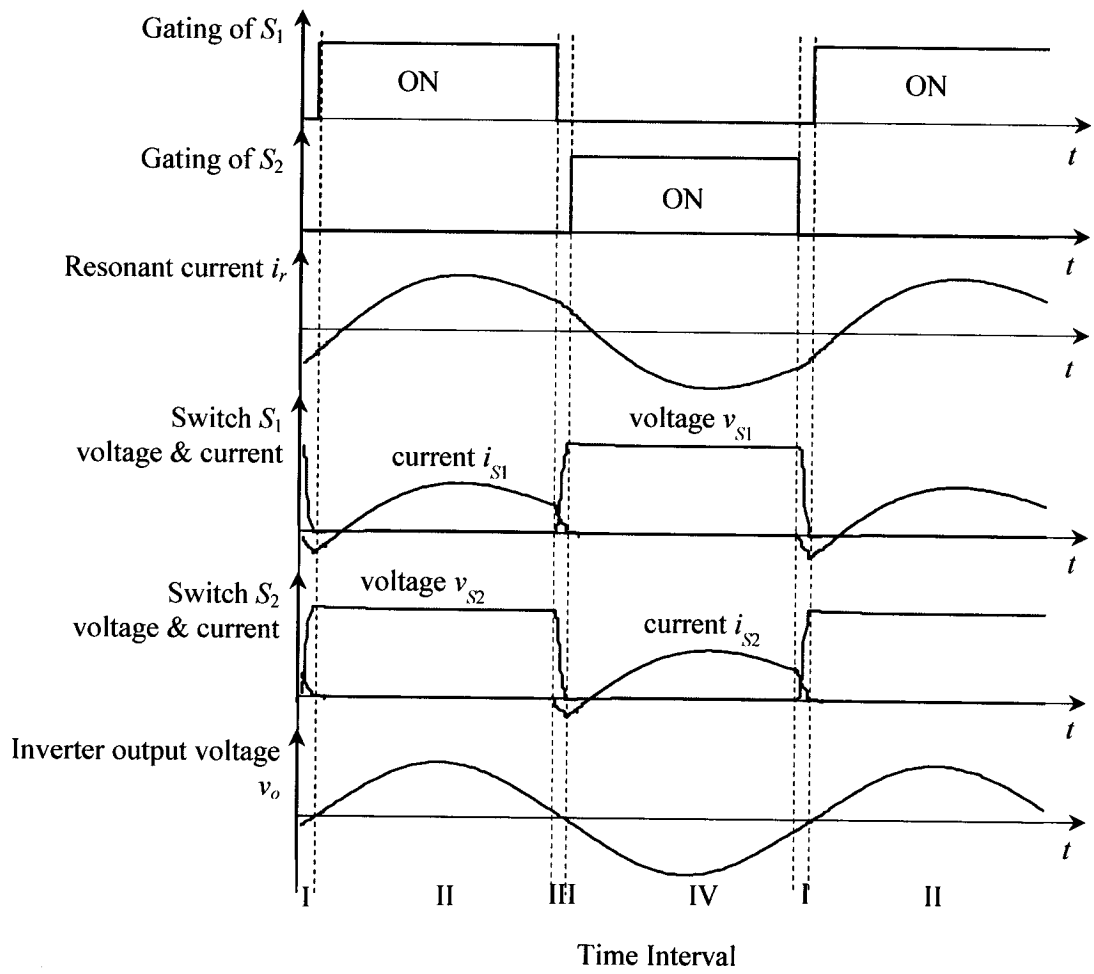


Fig. 2- 4: Operating waveforms of the proposed inverter

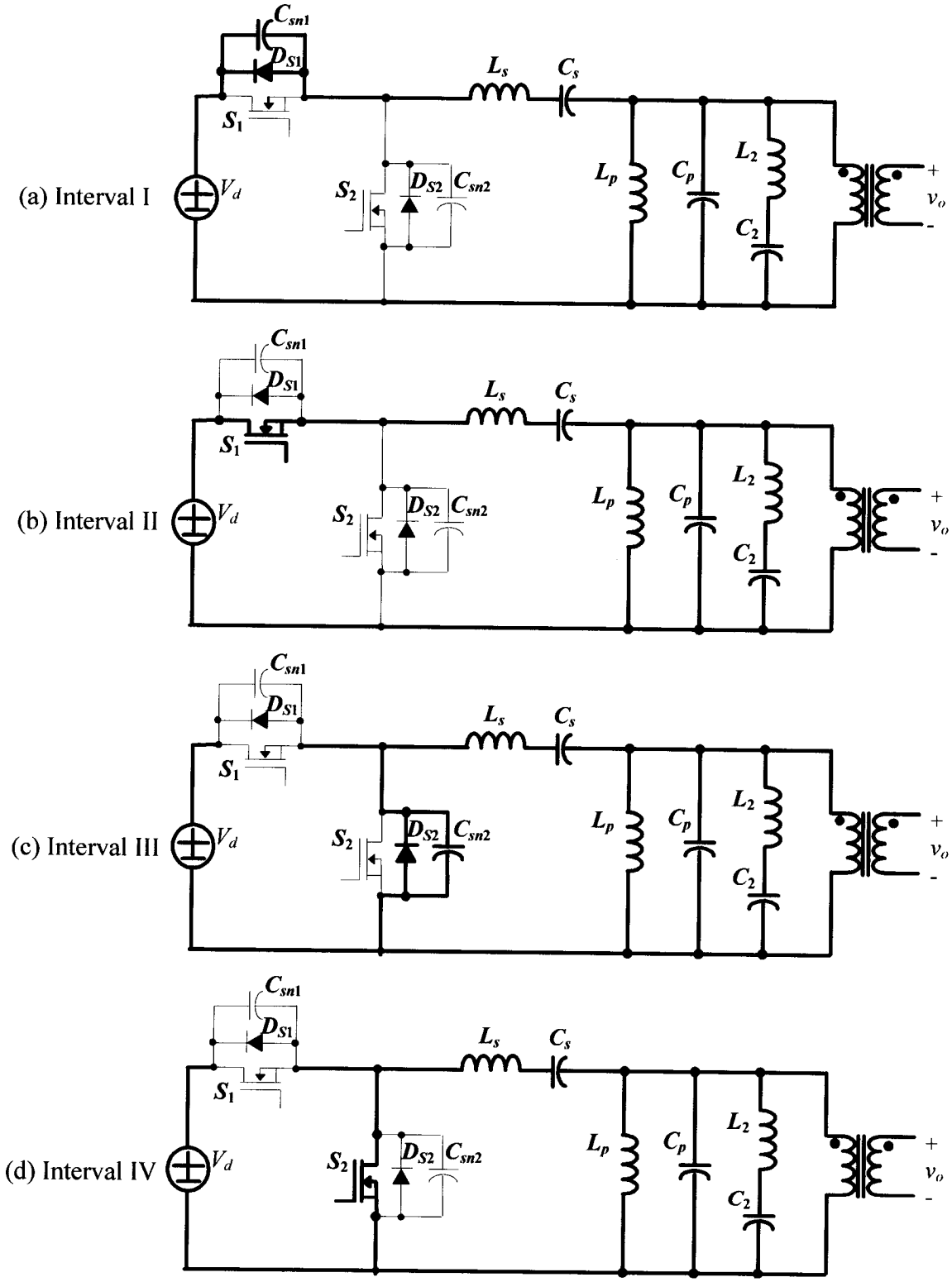


Fig. 2- 5: Active current path of the inverter in each operating interval

The above description of the inverter operation reveals that:

(i) Turn-on switching losses are zero since the anti-parallel diode always conducts prior to the switch,

(ii) The drain-to-source losses are eliminated since the capacitor across the switch always discharges into the resonant circuit,

(iii)Turn-off switching losses can be much reduced by using a large snubber capacitor across the switch, which provides a slow rise of the voltage across the switch.

2.2 STEADY-STATE ANALYSIS OF THE APWM RESONANT INVERTER

In this section, the steady-state analysis of the APWM inverter is presented. Section 2.2.1 makes the simplifying assumptions on which the analysis is based. The circuit parameters are normalized in section 2.2.2. In section 2.2.3, equations are derived to explain the output voltage control. The harmonic trap is added into the inverter circuit based on the harmonic analysis of the output voltage given in section 2.2.4. Then the time-varying expressions of voltage and current of the circuit variables are derived in section 2.2.5 to describe the inverter steady-state behavior. In section 2.5.6, the inverter input current harmonics are investigated to provide design guidelines for the input filter.

2.2.1 Simplifying Assumptions

The steady-state analysis of the proposed APWM inverter is carried out using the following assumptions:

(i) The input dc voltage of the inverter is constant;

(ii) The power semiconductor devices offer either zero or infinite impedance to the current flowing through them;

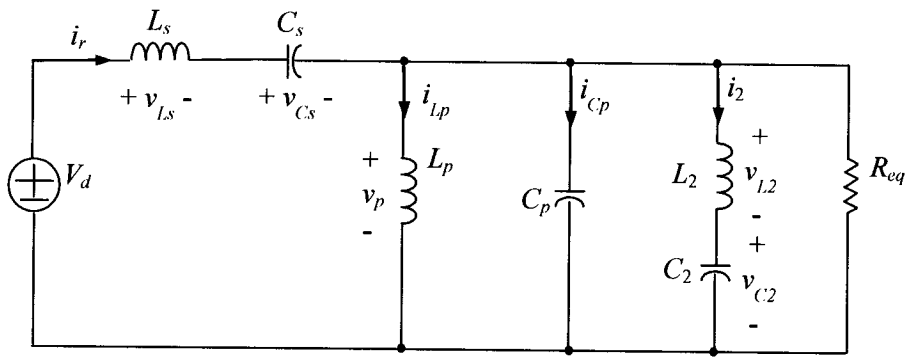
(iii) The effect of snubber capacitors is considered separately;

(iv) The magnetizing current of the matching transformer is negligible;

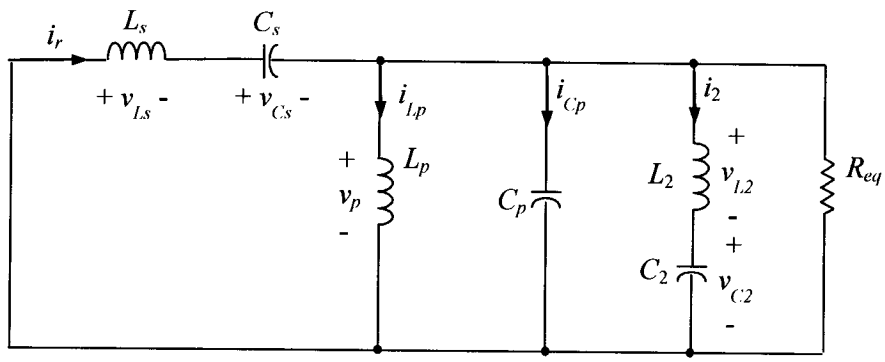
(v) The transformer winding resistance is lumped with the load, and the winding inductance is lumped with the resonant inductance;

(vi) The dead time between two complementary gating signals is negligible.

With the above assumptions, the operating intervals described in section 2.1.3 can be simplified into two intervals. The output stage of the inverter including the high-frequency transformer and the load can be presented by an equivalent resistance. Thus, the equivalent circuit in each simplified operating interval is shown in Fig. 2- 6.



(a) Simplified interval I: S_1 is on and S_2 is off $(kT_s \le t < kT_s+DT_s)$



(b) Simplified interval II: S_1 is off and S_2 is on $(kT_s+ DT_s \le t < (k+1)T_s)$

Fig. 2- 6: Equivalent circuit in each simplified operating interval

($k = 0, 1, 2, \ldots$, T_s is the switching period, and D is the duty cycle of S_1)

2.2.2 Normalization of the circuit parameters

The circuit parameters are normalized to make the analysis results obtained generally valid over a wide range of specified input and load conditions.

In the analysis, the input voltage V_d of the inverter is chosen as the base voltage:

$$1 \text{ p.u. volt} = V_d \tag{2- 1}$$

The equivalent resistance seen from the primary side of the transformer is taken as the base impedance:

$$1 \text{ p.u. impedance} = R_{eq} = N^2 R_{load} \tag{2- 2}$$

Where N is the transformer turns ratio, and R_{load} is the load impedance.

The operating frequency ω_o is taken as the base frequency:

$$1 \text{ p.u. rad/s} = \omega_o \tag{2- 3}$$

Therefore, the base current, power, inductance, and capacitance are expressed as:

$$1 \text{ p.u. current } I_B = V_d / R_{eq} \tag{2- 4}$$

$$1 \text{ p.u. power } P_B = I_B^2 R_{eq} \tag{2- 5}$$

$$1 \text{ p.u. inductance } L_B = R_{eq} / \omega_o \tag{2- 6}$$

$$1 \text{ p.u. capacitance } C_B = 1 / (\omega_o R_{eq}) \tag{2- 7}$$

Quality factors of the series-parallel resonant circuit are defined as:

$$Q_s = \omega_o L_s / R_{eq} \tag{2- 8}$$

$$Q_p = R_{eq} / (\omega_o L_p) \tag{2- 9}$$

Quality factor of the 2nd harmonic trap is defined by:

$$Q_2 = \omega_o L_2 / R_{eq} \tag{2- 10}$$

Where L_s, L_p, and L_2 are the values of the series resonant inductance, parallel resonant inductance and the inductance of the 2nd harmonic trap respectively.

2.2.3 Output Voltage Control

For APWM control technique [52], the complementary gating signals are applied to switches S_1 and S_2. The per-unit voltage at the output of the chopper can be represented by the following Fourier series:

$$v_{s2} = D + \sum_{n=1}^{\infty} \frac{\sqrt{2}\sqrt{1-\cos 2n\pi D}}{n\pi} \sin(n\omega_o t + \theta_n) \tag{2- 11}$$

where D is the duty cycle for switch S_1, and

$$\theta_n = \arctan\left(\frac{\sin 2n\pi D}{1-\cos 2n\pi D}\right) \tag{2- 12}$$

Because of the dc-block capacitor C_s, the ac component of v_{s2}, which causes the resonant current to flow, is given by:

$$v_{s2\_ac} = \sum_{n=1}^{\infty} \frac{\sqrt{2}\sqrt{1-\cos 2n\pi D}}{n\pi} \sin(n\omega_o t + \theta_n) \tag{2- 13}$$

Since the series resonant circuit is tuned and the parallel resonant circuit is slightly off-tuned at the operating frequency, only the ac fundamental component of v_{s2_ac} is considered to explain output voltage control. Its RMS value is given in (2- 14).

$$V_{s2\_ac1} = \frac{1}{\pi}\sqrt{1-\cos 2\pi D} \tag{2- 14}$$

Fig. 2- 7 shows the RMS output voltage as a function of the duty cycle D. This figure shows that the output voltage of the inverter can be controlled by changing the duty cycle D either from 0 to 0.5 (minimum-to-maximum output voltage) or from 0.5 to 1.0 (maximum-to-minimum output voltage). However, in the practical application, the isolation transformer used in the driver of S_1 will be saturated at $D = 1.0$. Therefore, duty cycle D from 0 to 0.5 is chosen for the complete output voltage control.

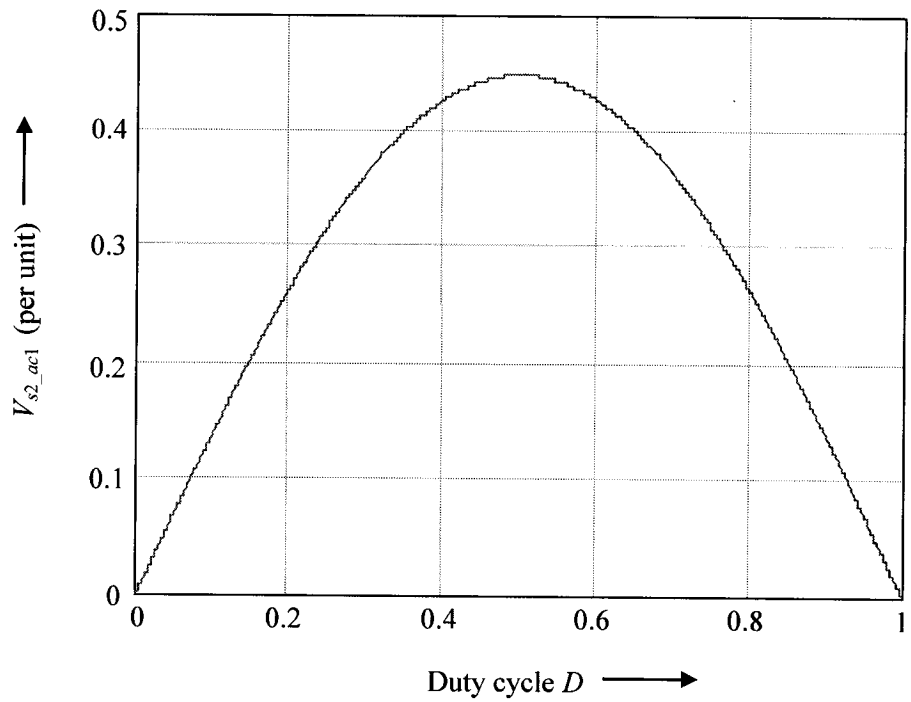


Fig. 2- 7: Output voltage control of the proposed inverter

2.2.4 Harmonic Analysis of the Output Voltage

A per unit nth harmonic equivalent circuit, as shown in Fig. 2- 8, is used to carry out further steady-state analysis of the proposed APWM resonant inverter.

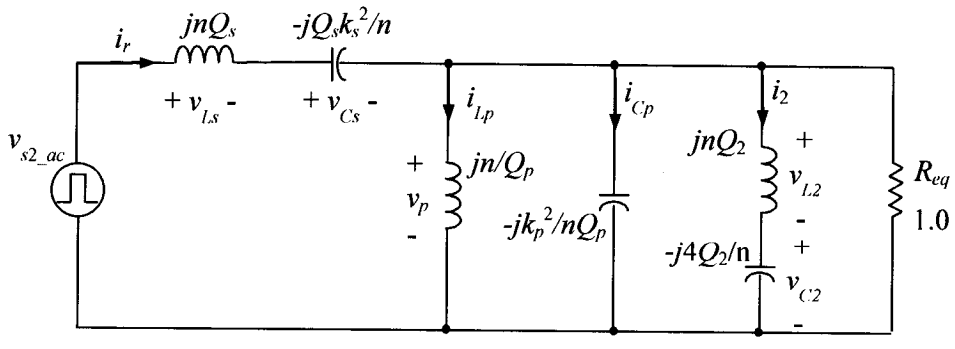


Fig. 2- 8: nth harmonic equivalent circuit of the proposed inverter

In Fig. 2- 8, the voltage source v_{s2_ac} (given by (2- 13)) replaces the input stage of the inverter including the input voltage source and the chopper circuit. The equivalent resistance R_{eq} represents the output stage of the inverter including the matching transformer and the load. The inductance and capacitance of the series-parallel resonant circuit and the 2nd harmonic trap are expressed in terms of the quality factors and the tuning factors.

The tuning factors are defined as:

$$k_s = \omega_s / \omega_o = 1 \tag{2- 15}$$

and

$$k_p = \omega_p / \omega_o > 1 \tag{2- 16}$$

Where ω_o is the operating frequency; ω_s and ω_p are resonant frequencies. Subscription "s" and "p" denote the quantities for the series and parallel resonant branches respectively.

For the APWM inverter without any harmonic trap, the per unit output voltage (rms) at the primary side of the high-frequency transformer is given by:

$$V_{pn} = V_{sn} \Big/ \left| 1 + Z_{sn} / Z_{pn} \right| \tag{2- 17}$$

where, V_{sn} is the rms value of the n^{th} harmonic of v_{s2_ac} given by (2-13), and

$$Z_{sn} = jQ_s (n - k_s^2 / n) \tag{2- 18}$$

$$Z_{pn} = 1 \Big/ \left(1 + jQ_p (n / k_p^2 - 1/n) \right) \tag{2- 19}$$

The corresponding harmonic profile of the output voltage is shown in Fig. 2- 9.

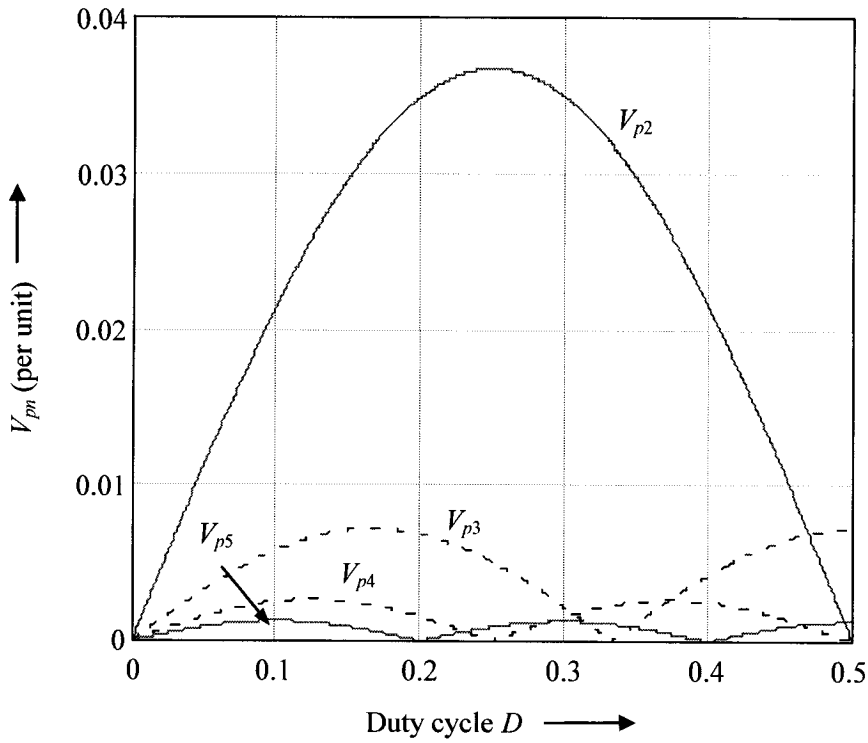


Fig. 2- 9: Harmonic profile of the APWM inverter

It can be seen that the most dominant harmonic is the 2nd harmonic. Therefore, a 2nd harmonic trap is employed in the proposed APWM inverter, as shown in Fig. 2- 1.

2.2.5 Inverter Circuit Voltages and Currents

From the equivalent circuit of Fig. 2- 8, the per-unit inverter circuit voltages and currents describing the steady-state behavior of the proposed APWM inverter are presented as follows.

(i) The per unit output voltage at the primary side of the high-frequency transformer is given by:

$$v_p = \sum_{n=1}^{\infty} \frac{\hat{V}_{s2\_ac,n}}{\left|1+\frac{Z_{sn}}{Z_{pn}}\right|} \sin(n\omega_o t + \theta_n - \gamma_n) \qquad (2\text{-}20)$$

Where $\hat{V}_{s2\_ac,n}$ is the maximum value of the nth harmonic component of voltage v_{s2_ac} given by (2- 13). Z_{sn} is the same as (2- 18), and

$$Z_{pn} = \frac{1}{1 + jQ_p(n/k_p^2 - 1/n) + 1/j(nQ_2 - 4Q_2/n)} \tag{2- 21}$$

$$\tan\gamma_n = \frac{Q_s(n - 1/n)}{1 - Q_s(n - 1/n)\left[Q_p\left(\frac{n}{k_p^2} - \frac{1}{n}\right) - \frac{1}{nQ_2 - 4Q_2/n}\right]} \tag{2- 22}$$

(ii) The per unit time-varying resonant current is given by:

$$i_r = \sum_{n=1}^{\infty} \frac{\hat{V}_{s2\_ac,n}}{|Z_{sn} + Z_{pn}|} \sin(n\omega_o t + \theta_n - \phi_n) \tag{2- 23}$$

Where

$$\phi_n = a\sin\left(\frac{|Z_{sn}| - |Z_{pn}| \cdot \sin(\alpha_n)}{|Z_{sn} + Z_{pn}|}\right) \tag{2- 24}$$

$$\alpha_n = a\tan\left(Q_p n/k_p^2 - Q_p/n - 1/(nQ_2 - 4Q_2/n)\right) \tag{2- 25}$$

(iii) The voltages and currents of the series resonant branch:

The current flowing through the series resonant branch is equal to the resonant current given by (2- 23).

The per unit time-varying voltage across the series resonant capacitor C_s is given by (2- 26), and its dc component is equal to the dc component at the output of the chopper.

$$v_{Cs} = D - Q_s \sum_{n=1}^{\infty} \frac{\hat{V}_{s2\_ac,n}}{n|Z_{sn} + Z_{pn}|} \cos(n\omega_o t + \theta_n - \phi_n) \tag{2- 26}$$

The per unit time-varying voltage across the series resonant inductor L_s can be derived from the equivalent circuit of Fig. 2- 6.

$$v_{Ls} = \begin{cases} 1 - v_p - v_{Cs} & \text{when} \quad kT_s \le t < kT_s + DT_s \\ -v_p - v_{Cs} & \text{when} \quad kT_s + DT_s \le t \le (k+1)T_s \end{cases} \tag{2- 27}$$

Where v_p is given by (2- 20), and v_{Cs} is given by (2- 26). $k = 0, 1, 2, \ldots$.

(iv) The voltages and currents of the parallel resonant branch:

The voltage across the parallel resonant branch is the same as the voltage at the primary side of the high-frequency transformer given by (2- 20).

The current flowing through the parallel resonant capacitor is given by:

$$i_{Cp} = \frac{Q_p}{k_p^2} \sum_{n=1}^{\infty} \frac{n\hat{V}_{s2\_ac,n}}{\left|1 + \frac{Z_{sn}}{Z_{pn}}\right|} \cos(n\omega_o t + \theta_n - \gamma_n) \tag{2- 28}$$

The current flowing through the parallel resonant inductor is given by:

$$i_{Lp} = -Q_p \sum_{n=1}^{\infty} \frac{\hat{V}_{s2\_ac,n}}{n\left|1 + \frac{Z_{sn}}{Z_{pn}}\right|} \cos(n\omega_o t + \theta_n - \gamma_n) \tag{2- 29}$$

(v) The voltages and currents of the 2nd harmonic trap:

The voltage and current of the 2nd harmonic trap are expressed by the sum of three components: (a) fundamental component, (b) 2nd harmonic, and (c) higher harmonics.

The current flowing through the 2nd harmonic trap is given by:

$$i_2 = i_{2\_a} + i_{2\_b} + i_{2\_c} \tag{2- 30}$$

Where

$$i_{2\_a} = \frac{\hat{V}_{s2\_ac,1}}{3Q_2}\cos(\omega_o t + \theta_1 - \gamma_1) \tag{2- 31}$$

$$i_{2\_b} = \frac{\hat{V}_{s2\_ac,2}}{\left|Z_{s2} + Z_{p2}\right|}\sin(2\omega_o t + \theta_2 - \gamma_2) \tag{2- 32}$$

$$i_{2\_c} = \sum_{n=3}^{\infty} \frac{-\hat{V}_{s2\_ac,n}}{Q_2(n - 4/n)\left|1 + \frac{Z_{sn}}{Z_{pn}}\right|}\cos(n\omega_o t + \theta_n - \gamma_n) \tag{2- 33}$$

Where $\hat{V}_{s2\_ac,1}$ and $\hat{V}_{s2\_ac,2}$ are the maximum value of v_{s2_ac} given by (2- 13) when n=1 and n=2 respectively. θ_1/θ_2 and γ_1/γ_2 are the values of θ_n and γ_n given by (2- 12) and (2- 22) respectively when n=1 and n=2.

The voltage across the capacitor of the 2nd harmonic trap is given by:

$$v_{C2} = v_{C2\_a} + v_{C2\_b} + v_{C2\_c} \tag{2- 34}$$

Where

$$v_{C2\_a} = \frac{4\hat{V}_{s2\_ac,1}}{3}\sin(\omega_o t + \theta_1 - \gamma_1) \tag{2- 35}$$

$$v_{C2\_b} = -2Q_2\frac{\hat{V}_{s2\_ac,2}}{\left|Z_{s2} + Z_{p2}\right|}\cos(2\omega_o t + \theta_2 - \gamma_2) \tag{2- 36}$$

$$v_{C2\_c} = \sum_{n=3}^{\infty} \frac{-\hat{V}_{s2\_ac,n}}{(n^2 - 4)\left|1 + \frac{Z_{sn}}{Z_{pn}}\right|}\sin(n\omega_o t + \theta_n - \gamma_n) \tag{2- 37}$$

The voltage across the inductor of the 2nd harmonic trap is given by:

$$v_{L2} = v_{L2\_a} + v_{L2\_b} + v_{L2\_c} \tag{2- 38}$$

Where

$$v_{L2\_a} = -\frac{\hat{V}_{s2\_ac,1}}{3}\sin(\omega_o t + \theta_1 - \gamma_1) \tag{2- 39}$$

$$v_{L2\_b} = 2Q_2 \frac{\hat{V}_{s2\_ac,2}}{\left|Z_{s2} + Z_{p2}\right|}\cos(2\omega_o t + \theta_2 - \gamma_2) \tag{2- 40}$$

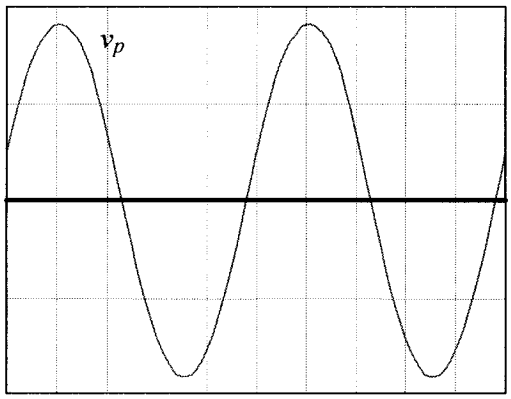
$$v_{L2\_c} = \sum_{n=3}^{\infty} \frac{\hat{V}_{s2\_ac,n}}{\left(n^2 - 4\right)\left|1 + \frac{Z_{sn}}{Z_{pn}}\right|}\sin(n\omega_o t + \theta_n - \gamma_n) \tag{2- 41}$$

(vi) The voltages and currents of the chopper circuit:

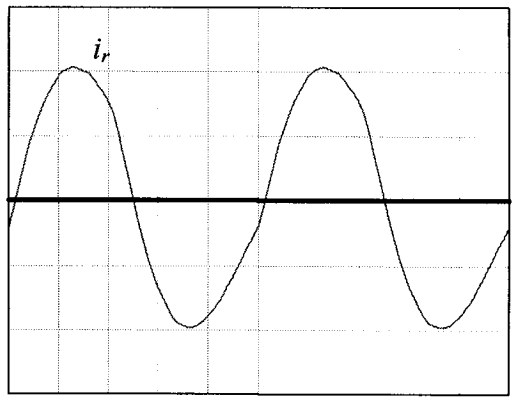
When switch S_1 is on and S_2 is off (interval I in Fig. 2- 6), the current flowing through S_1 is the resonant current given by (2- 23), and the current flowing though S_2 is zero. The voltage across S_1 is zero, and the voltage across S_2 equals the input voltage V_d.

When switch S_1 is off and S_2 is on (interval II in Fig. 2- 6), the current flowing through S_1 is zero, and the current flowing though S_2 is the resonant current given by (2- 23). The voltage across S_1 equals the input dc voltage V_d, and the voltage across S_2 is zero.

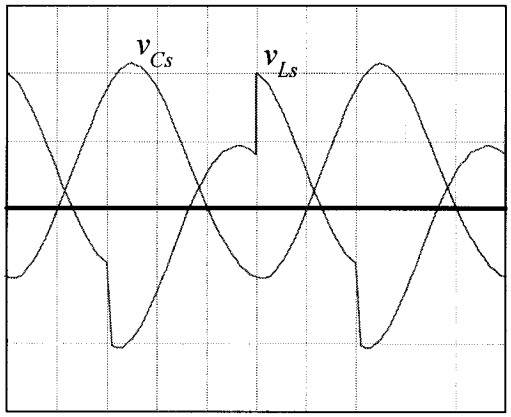
The waveforms of the circuit variables through two steady state cycles are shown in Fig. 2- 10. These waveforms are obtained from the above theoretical derivation for the inverter with V_d = 60V, $Q_s = Q_p$ = 2, k_p = 1.15, P_o = 160 W (80% load), V_o = 28 Vrms. The simulation results for the same inverter are shown in Fig. 2- 11 for the purpose of verification. It can be seen that the theoretical predictions and the simulation results have a good agreement, except some slight differences arising from the fact that the theoretical results are based on ideal circuit parameters, while the simulation model uses more realistic ones. Therefore, the steady-state analysis made in this section is valid and applicable to a real circuit.



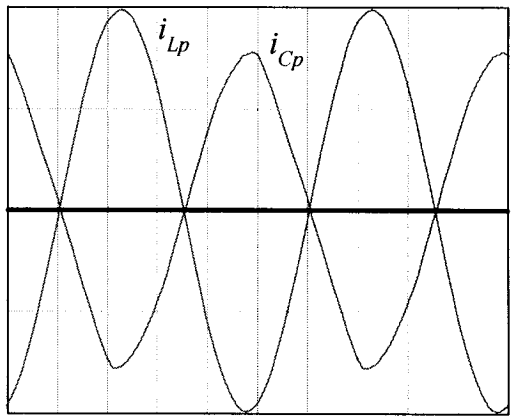
(a) Transformer primary voltage v_p(20V/div)



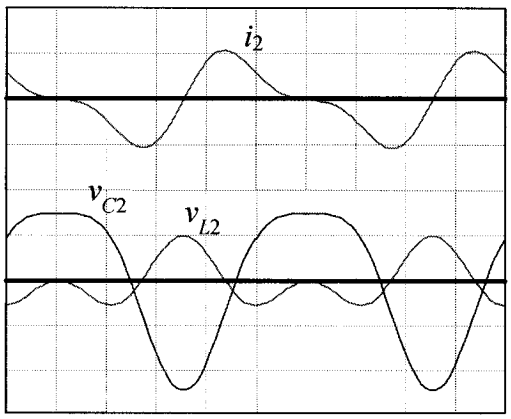
(b) Resonant current i_r (5A/div)



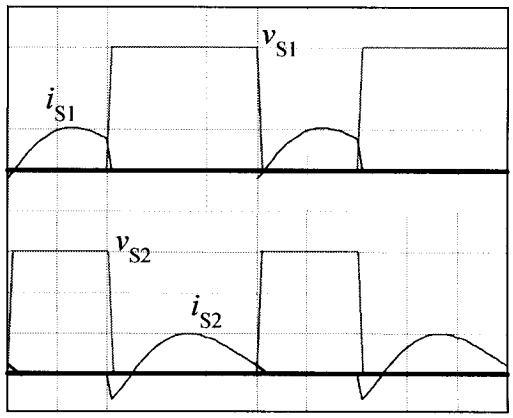
(c) Voltage of series resonant tank v_{Cs} and v_{Ls} (50V/div)



(d) Current of parallel resonant tank i_{Cp} and i_{Lp} (10A/div)

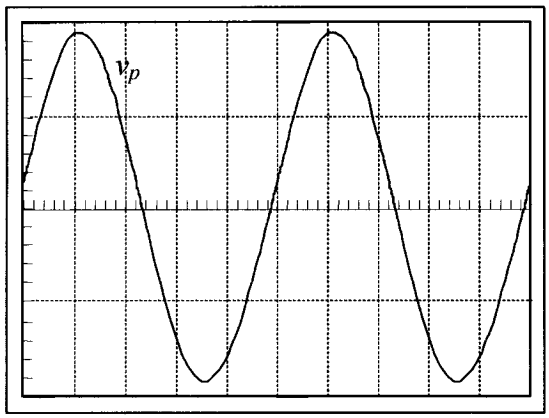


(e) Voltage and current of 2nd harmonic trap i_2 (2A/div), v_{C2} (25V/div), and v_{L2} (25V/div)

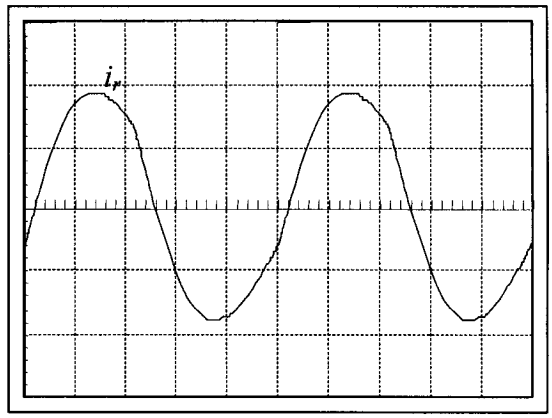


(f) Voltage and current of chopper switches v_{S1} & v_{S2} (20V/div), i_{S1} & i_{S2} (10A/div)

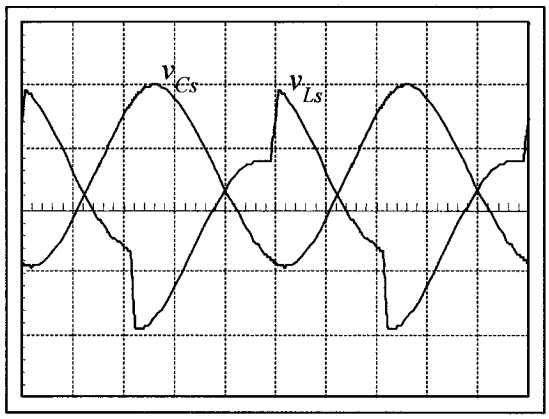
Fig. 2- 10: Theoretical waveforms of the inverter circuit variables (Horizontal time scale: 0.2 μs/div; Vertical voltage and/or current scales are indicated in subtitle)



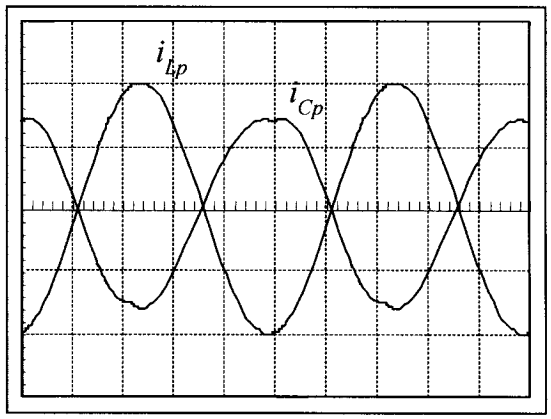
(a) Transformer primary voltage v_p(20V/div)



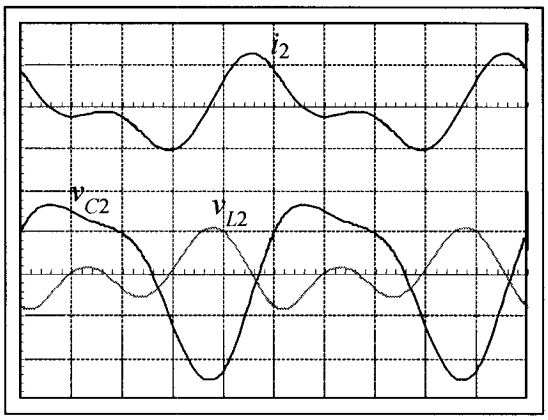
(b) Resonant current i_r (5A/div)



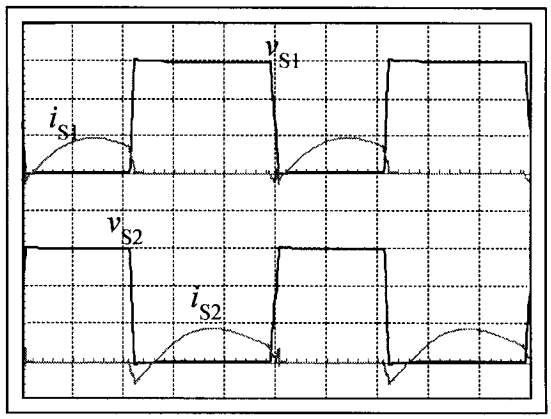
(c) Voltage of series resonant tank v_{Cs} and v_{Ls} (50V/div)



(d) Current of parallel resonant tank i_{Cp} and i_{Lp} (10A/div)



(e) Voltage and current of 2nd harmonic trap i_2 (2A/div), v_{C2} (25V/div), and v_{L2} (25V/div)



(f) Voltage and current of chopper switches v_{S1} & v_{S2} (20V/div), i_{S1} & i_{S2} (10A/div)

Fig. 2- 11: Simulation waveforms of the APWM inverter circuit variables (Horizontal time scale: 0.2 μs/div; Vertical voltage and/or current scales are indicated in subtitle)

2.3 PERFORMANCE CURVES FOR THE APWM RESONANT INVERTER

In this section, the RMS values of the inverter circuit variables are presented as a function of the tuning factor k_p for various values of the quality factors Q_s and Q_p. The inverter performance such as the total harmonic distortion of the output voltage and zero voltage switching is studied as a function of the duty cycle for various values of k_p, Q_s, and Q_p. Then the effect of the quality factor Q_2 on the performance of the 2nd harmonic trap is studied. Finally the switch stress and utilization are presented. The performance curves presented in this chapter are used in Chapter 4 to design the APWM inverter.

2.3.1 RMS Voltages and Currents of the Inverter

The time-varying expressions of the inverter circuit variables obtained in section 2.2.5 are used in this section to derive the RMS values of the circuit variables.

The information obtained in this section is used in Chapter 4 for design purpose. For a given set of parameters (Q_s, Q_p, and k_p), the maximum per unit ratings of the circuit components are determined when the duty cycle $D = 0.5$. Therefore, in this section, the RMS values of circuit variables are studied as a function of the tuning factor k_p and the circuit quality factors Q_s and Q_p ($Q_2 = 2$) when duty cycle is a constant of 0.5.

(i) The RMS value of the voltage across the primary side of the high-frequency matching transformer is given by (2- 42) and plotted as a function of k_p for various values of Q_s and Q_p in Fig. 2- 12(a):

$$V_p = \sqrt{\sum_{n=1}^{\infty}\left(\frac{V_{sn}}{\left|1 + Z_{sn}/Z_{pn}\right|}\right)^2} \qquad (2\text{- }42)$$

Where

$$V_{sn} = \frac{\sqrt{1-\cos(2\pi nD)}}{n\pi} \tag{2-43}$$

Fig. 2- 12(a) shows that, for different values of Q_s and Q_p, when k_p is varied within a very small range, V_p is close to a constant value equal to the fundamental component of V_{sn} regardless of the parameters of the resonant components. This fact can be explained by (2- 42) and (2- 43) as follows:

(a) When $n = 1$, $Z_{sn} = 0$, V_p is simply equal to the fundamental component of V_{sn};

(b) When $n = 2$, because of the 2nd harmonic trap, V_p is equal to zero;

(c) When $n > 2$, for each harmonic component, V_{sn} given by (2- 43) is less than 1, and the value of $|Z_{sn}|$ is much higher than the value of $|Z_{pn}|$. Therefore, V_p is approximately equal to zero.

(ii) RMS value of the resonant current is given by:

$$I_r = \sqrt{\sum_{n=1}^{\infty}\left(\frac{V_{sn}}{|Z_{sn}+Z_{pn}|}\right)^2} \tag{2-44}$$

The dominant contribution to I_r is its fundamental component, whose value is only dependent on the component values of the parallel resonant branch since the fundamental series resonant impedance is equal to zero. Therefore, as shown in Fig. 2- 12(b), I_r is a function Q_p and k_p regardless of Q_s.

(iii) RMS voltages of the series resonant components:

The RMS value of the voltage across the series resonant capacitor is given by (2- 45) and plotted as a function of k_p for various values of Q_s and Q_p in Fig. 2- 12(c):

$$V_{cs} = Q_s\sqrt{\sum_{n=1}^{\infty}\frac{V_{sn}^2}{n^2|Z_{sn}+Z_{pn}|^2}} \tag{2-45}$$

The RMS value of the voltage across the series resonant inductor is given by (2-46) and plotted as a function of k_p for various values of Q_s and Q_p in Fig. 2- 12(d):

$$V_{Ls} = \sqrt{\frac{1}{T_s}\left[\int_0^{DT_s}(1 - v_p - v_{Cs})^2 dt + \int_{DT_s}^{T_s}(-v_p - v_{Cs})^2 dt\right]} \qquad (2\text{-}46)$$

(iv) RMS currents of the parallel resonant components:

The RMS value of the current flowing through the parallel resonant capacitor is given by (2- 47) and plotted as a function of k_p for various values of Q_s and Q_p in Fig. 2-12(e):

$$I_{Cp} = \frac{Q_p}{k_p^2}\sqrt{\sum_{n=1}^{\infty}\left(\frac{nV_{sn}}{\left|1 + Z_{sn}/Z_{pn}\right|}\right)^2} \qquad (2\text{-}47)$$

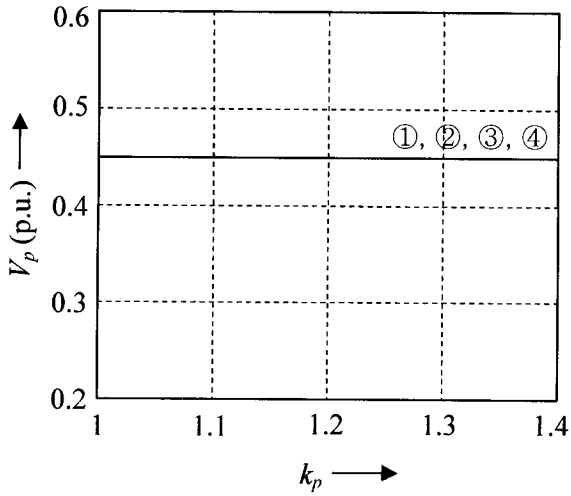
The RMS value of the current flowing through the parallel resonant inductor is given by (2- 48) and plotted as a function of k_p for various values of Q_s and Q_p in Fig. 2-12(f):

$$I_{Lp} = Q_p\sqrt{\sum_{n=1}^{\infty}\left(\frac{nV_{sn}}{\left|1 + Z_{sn}/Z_{pn}\right|}\right)^2} \qquad (2\text{-}48)$$

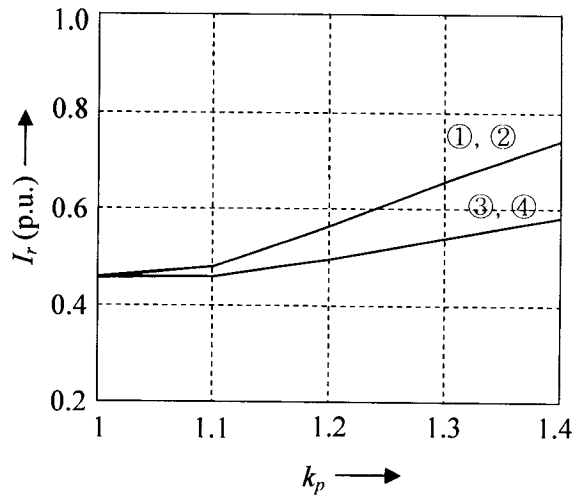
(v) RMS currents of the switches in the chopper circuit:

The RMS value of the current flowing through the switch S_1 is equal to that flowing through the switch S_2 when D = 0.5, and is given by (2- 49) and plotted as a function of k_p for various values of Q_s and Q_p in Fig. 2- 12(g):

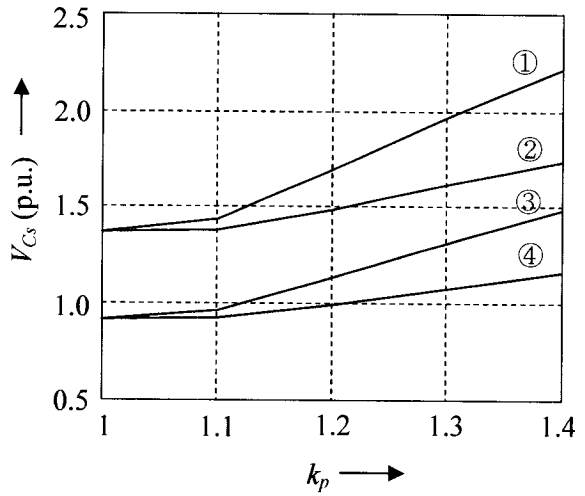
$$I_{S1} = I_{s2} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(\sum_{n=1}^{\infty}\frac{\hat{V}_{s2\_ac,n}}{\left|Z_{sn} + Z_{pn}\right|}\sin(n\omega_o t + \theta_n - \phi_n)\right)^2 dt} \qquad (2\text{-}49)$$



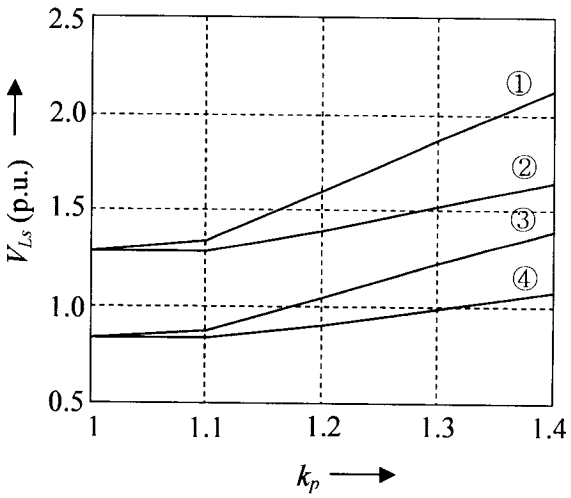
(a) RMS value of the voltage across the primary side of the transformer (①: Q_s=Q_p=3, ②: Q_s =3, Q_p =2, ③: Q_s =2, Q_p =3, ④: Q_s = Q_p =2)



(b) RMS value of the resonant current (①: Q_s = Q_p =3, ②: Q_s =2, Q_p =3, ③: Q_s =3, Q_p =2, ④: Q_s = Q_p =2)



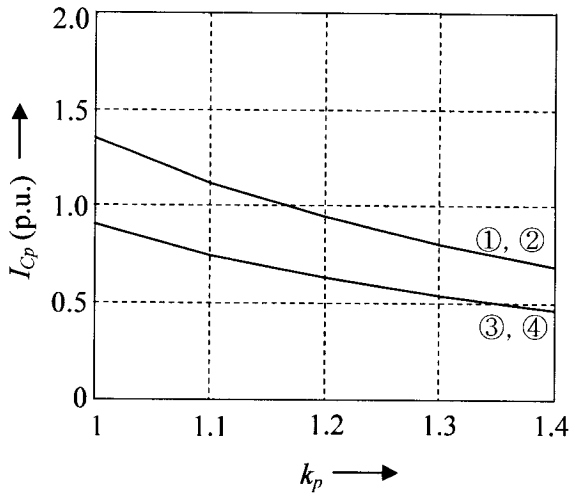
(c) RMS value of the voltage across the series resonant capacitor (①: Q_s = Q_p =3, ②: Q_s =3, Q_p =2, ③: Q_s =2, Q_p =3, ④: Q_s = Q_p =2)



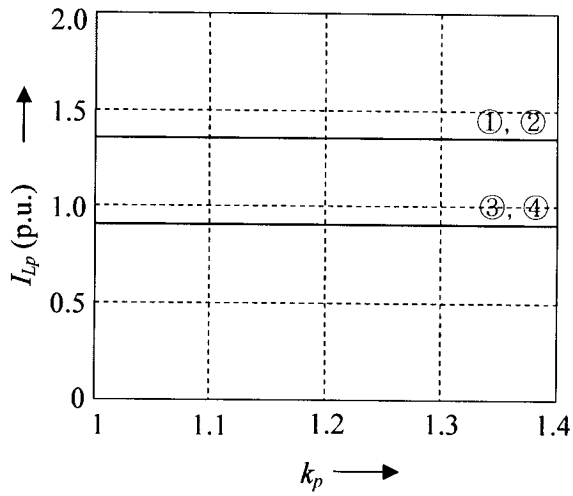
(d) RMS value of the voltage across the series resonant inductor (①: Q_s = Q_p =3, ②: Q_s =3, Q_p =2, ③: Q_s =2, Q_p =3, ④: Q_s = Q_p =2)

Fig. 2- 12: RMS voltages and currents of the proposed APWM inverter

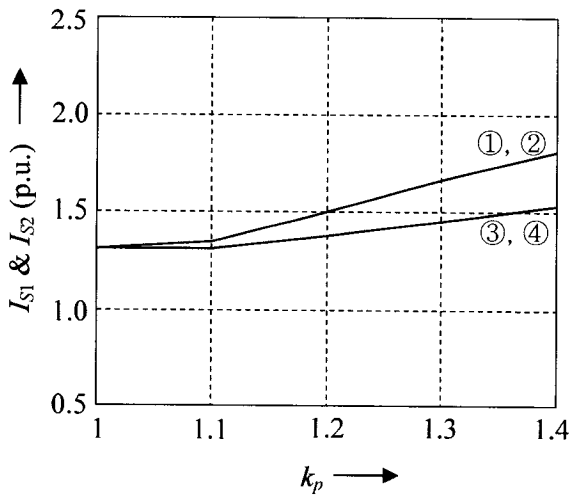
(to be continued)



(e) RMS value of the current flowing through the parallel resonant capacitor (①: Q_s=Q_p=3, ②: Q_s =2, Q_p =3, ③: Q_s =3, Q_p =2, ④: Q_s = Q_p =2)



(f) RMS value of the current flowing through the parallel resonant inductor (①: Q_s = Q_p =3, ②: Q_s =2, Q_p =3, ③: Q_s =3, Q_p =2, ④: Q_s = Q_p =2)



(g) RMS value of the current flowing through the chopper switches (①: Q_s = Q_p =3, ②: Q_s =2, Q_p =3, ③: Q_s =3, Q_p =2, ④: Q_s = Q_p =2)

Fig. 2- 12: RMS voltages and currents of the proposed APWM inverter

(continued)

2.3.2 Significant Characteristics of the APWM Resonant Inverter

In this section, the total harmonic distortion (THD) of the output voltage of the inverter and the conditions to achieve zero voltage switching (ZVS) are studied as the function of duty cycle with respect to the quality factors of the inverter (Q_s, Q_p) and the tuning factor k_p. Q_2 equal to 2 is assumed in this section.

2.3.2.1 Total harmonic distortion of the inverter output voltage

The THD of the output voltage of the proposed APWM inverter is calculated by:

$$\%THD = 100 \times \frac{\sqrt{\sum_{n=2}^{\infty} V_p}}{V_{p1}} \tag{2- 50}$$

Where V_p is the RMS value of v_p given by (2- 20), and V_{p1} is the RMS value of the fundamental component of v_p (n=1).

For different values of Q_s, Q_p and k_p, THD of the inverter output voltage is shown in Fig. 2- 13. It can be seen that the THD is not only highly depending on the circuit parameters, but also the range of the operating duty cycle, which is decided by the input voltage and load conditions.

2.3.2.2 Zero voltage switching

In Fig. 2- 14 and Fig. 2- 15, the current at turn-off instant of each switch of the chopper circuit is calculated to provide information on the region of ZVS for the complementary switch at turn-on. Derived from (2- 23), the per unit values of current at turn-off of switch S_1 and switch S_2 are given by (2- 51) and (2- 52) respectively:

$$I_{s1\_turn-off} = \sum_{n=1}^{\infty} \frac{\sqrt{2}\sqrt{1-\cos(2n\pi D)}}{n\pi \left| Z_{sn} + Z_{pn} \right|} \sin(2\pi nD + \theta_n - \phi_n) \tag{2- 51}$$

$$I_{s2\_turn-off} = \sum_{n=1}^{\infty} \frac{\sqrt{2}\sqrt{1-\cos(2n\pi D)}}{n\pi\left|Z_{sn}+Z_{pn}\right|}\sin(\theta_n - \phi_n) \qquad (2\text{-}52)$$

To achieve ZVS, the direction of the resonant current should be such that it forces the anti-parallel diode to conduct prior to the turn-on of the switch. Therefore, $I_{s1\_turn-off}$ should be positive to turn on S_2 under zero voltage, and $I_{s2\_turn-off}$ should be negative to turn on S_1 under zero voltage.

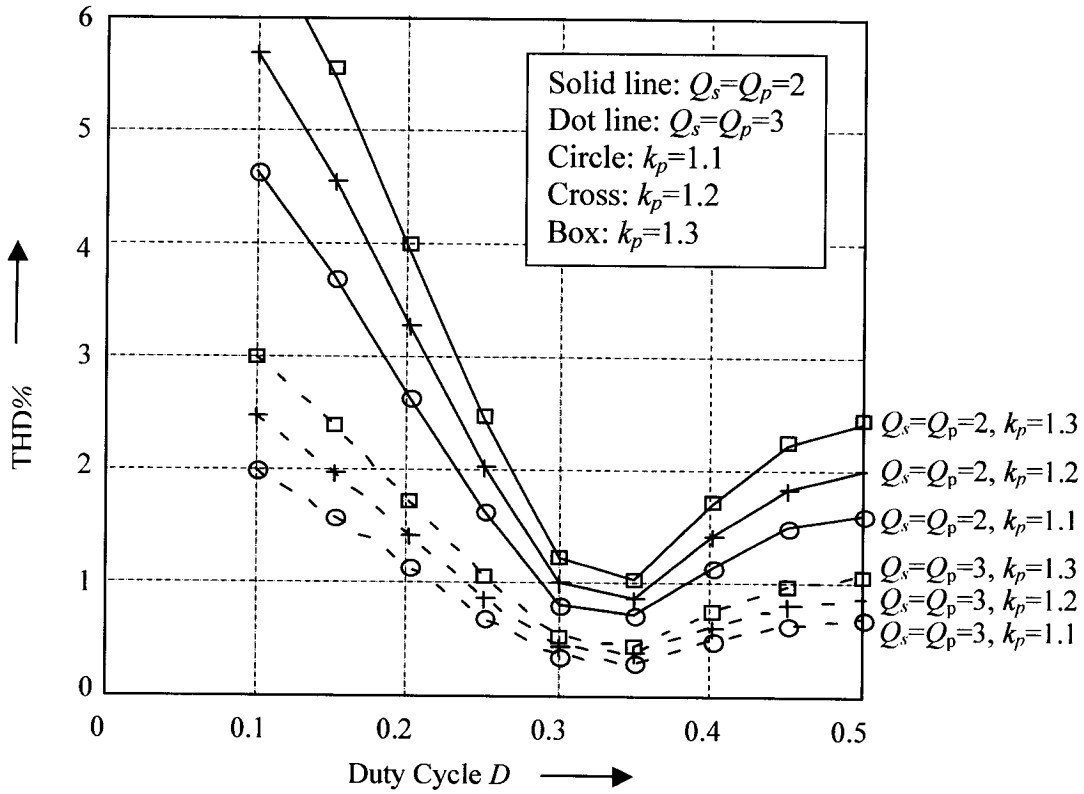


Fig. 2- 13: THD of the inverter output voltage

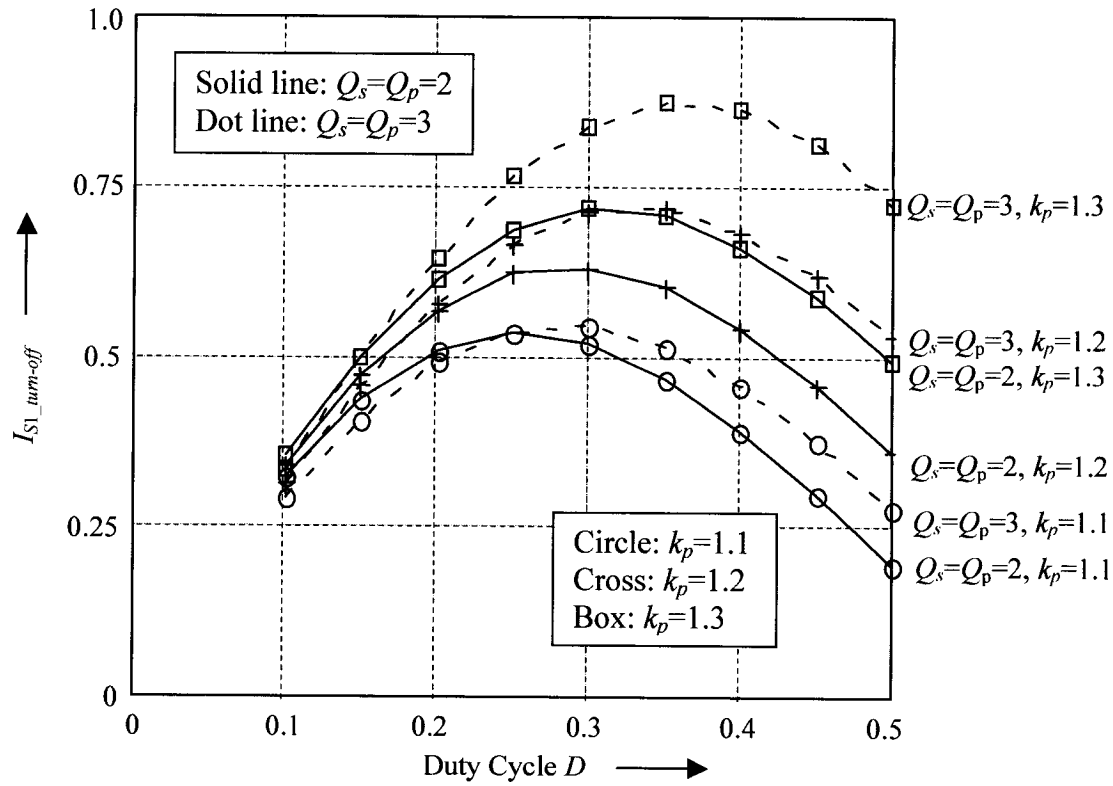


Fig. 2- 14: Region of turn-on ZVS for switch S_2: $I_{S1\_turn\text{-}off}>0$

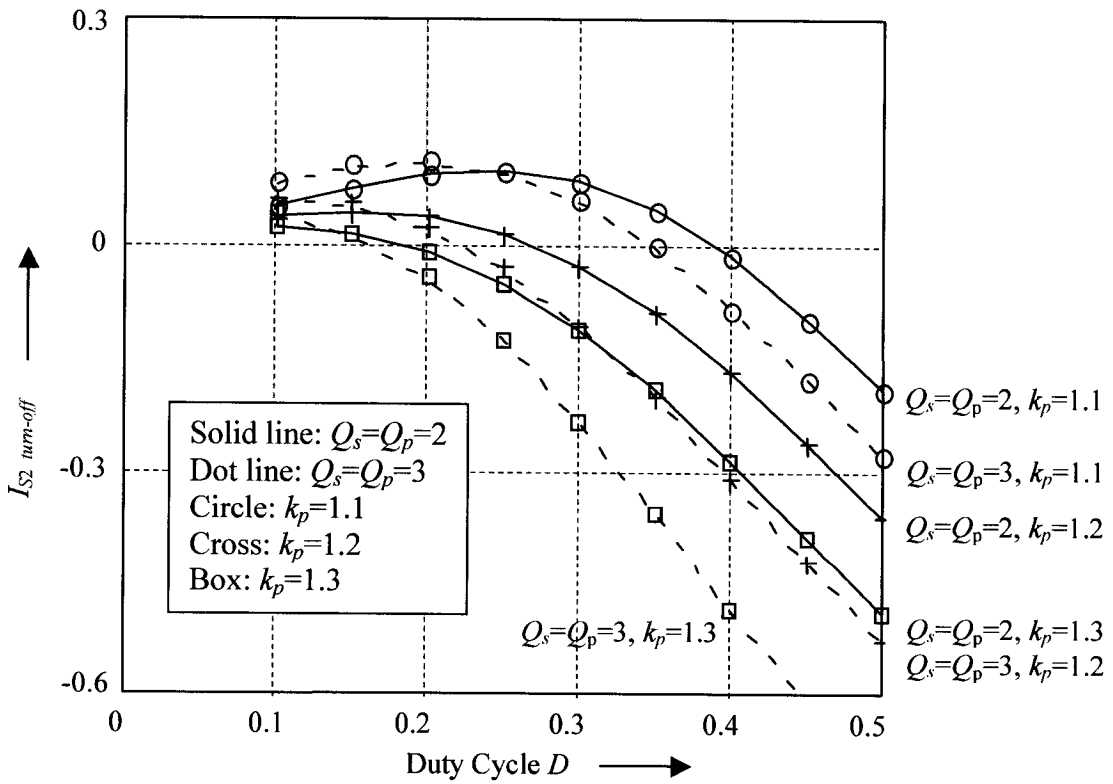


Fig. 2- 15: Region of turn-on ZVS for switch S_1: $I_{S2\_turn\text{-}off}<0$

2.3.3 Performance Curves of the Second Harmonic Trap

In this section, selection of the quality factor of the 2nd harmonic trap to achieve ZVS operation is described. The RMS values of the voltage and current of the 2nd harmonic trap are presented as a function of the quality factor Q_2. With respect to the duty cycle of switch S_1 and the quality factor Q_2, characteristics of the 2nd harmonic trap such as (i) the contribution of the 2nd harmonic trap on the attenuation of the 3rd harmonic, and (ii) effect of the tuning precision on the harmonic elimination, are studied.

2.3.3.1 Selection of the quality factor

As explained in section 2.1.2, in the preferred operation mode, the resonant current must lags the output voltage of the chopper at the operating frequency to achieve ZVS operation. Therefore, the parallel resonant branch and the 2nd harmonic trap together have to present an inductive impedance at the operating frequency.

The impedance of the parallel resonant branch and the 2nd harmonic trap at the operating frequency can be obtained from (2- 21) when n=1:

$$Z_{p1} = \frac{1}{1 + j\left[Q_p(1/k_p^2 - 1) + 1/(3Q_2)\right]} \tag{2- 53}$$

The imaginary part of Z_{p1} has to be positive to present an inductive impedance. Thus the quality factor of the 2nd harmonic trap should be limited by:

$$Q_2 > \frac{1}{3Q_p(1 - 1/k_p^2)} \tag{2- 54}$$

The minimum value of Q_2, Q_{2_min}, is plotted in Fig. 2- 16 as a function of Q_p for different values of k_p.

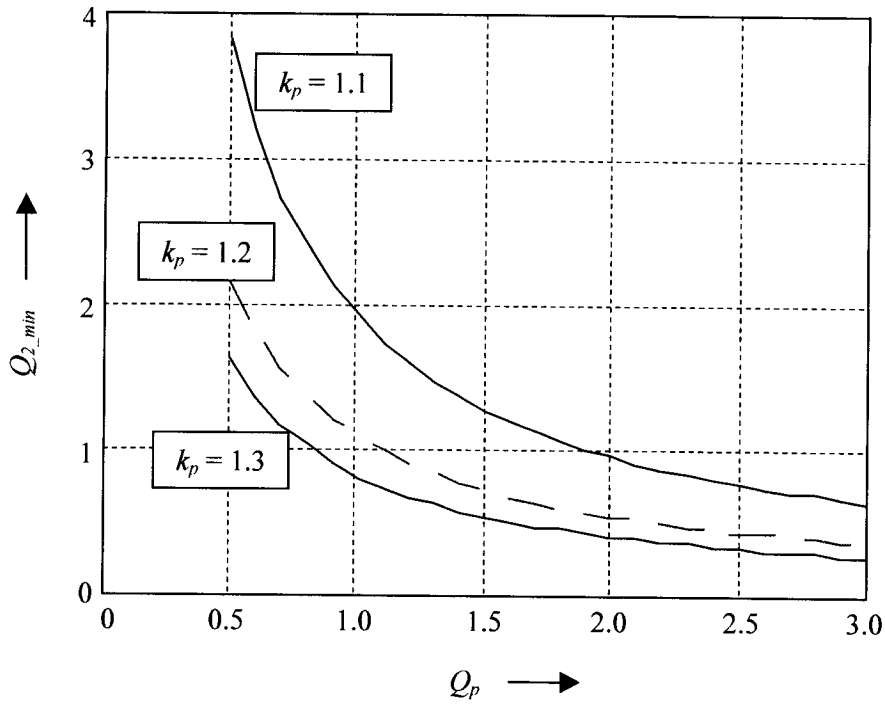


Fig. 2- 16: Minimum value of Q_2 as function of Q_p and k_p

2.3.3.2 *RMS values of voltage and current of the 2nd harmonic trap components*

The RMS current through the 2nd harmonic trap is given by (2- 55) and plotted as a function of Q_2 for various values of duty cycle D in Fig. 2- 17(a):

$$I_2 = \sqrt{\left(\frac{V_{sn1}}{3Q_2}\right)^2 + \left(\frac{V_{sn2}}{\left|Z_{s2} + Z_{p2}\right|}\right)^2 + \sum_{n=3}^{\infty}\left(\frac{V_{sn}}{Q_2\left(n - 4/n\right)\left|1 + Z_{sn}/Z_{pn}\right|}\right)} \qquad (2\text{- }55)$$

Where V_{sn1} and V_{sn2} are given by (2- 37) when n=1 and n=2 respectively.

The RMS value of the voltage across the capacitor of the 2nd harmonic trap is given by (2- 56) and plotted as a function of Q_2 for various values of D in Fig. 2- 17(b):

$$V_{C2} = \sqrt{\left(\frac{4V_{sn1}}{3}\right)^2 + \left(\frac{2Q_2V_{sn2}}{\left|Z_{s2} + Z_{p2}\right|}\right)^2 + \sum_{n=3}^{\infty}\left(\frac{V_{sn}}{\left(n^2 - 4\right)\left|1 + Z_{sn}/Z_{pn}\right|}\right)} \qquad (2\text{- }56)$$

The RMS value of the voltage across the inductor of the 2nd harmonic trap is given by (2- 57) and plotted as a function of Q_2 for various values of D in Fig. 2- 17(c):

$$V_{L2} = \sqrt{\left(\frac{V_{sn1}}{3}\right)^2 + \left(\frac{2Q_2 V_{sn2}}{\left|Z_{s2} + Z_{p2}\right|}\right)^2 + \sum_{n=3}^{\infty}\left(\frac{V_{sn}}{\left(n^2-4\right)\left|1 + Z_{sn}/Z_{pn}\right|}\right)} \qquad (2\text{- }57)$$

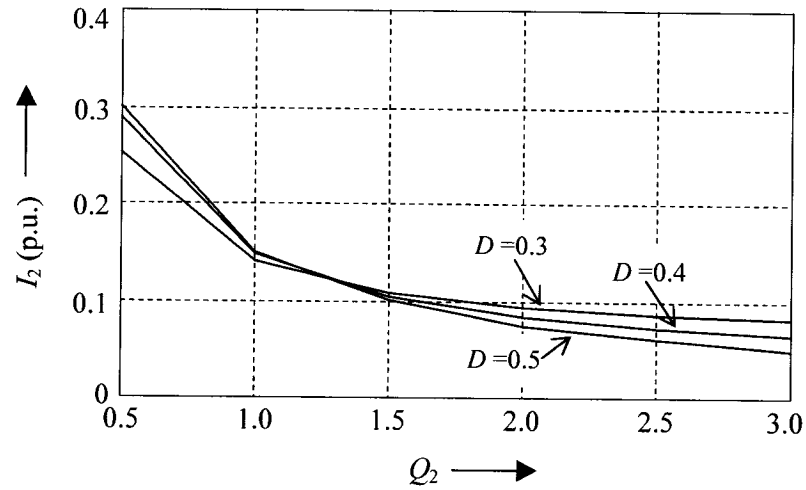
In Fig. 2- 17(b) and Fig. 2- 17(c), the RMS values of the voltage across the trap capacitor and inductor when $D = 0.5$ are constant regardless of the value of Q_2. This fact can be explained as follows. The most contributions to the RMS values are from the fundamental component and the 2nd harmonic. Since V_{sn2} is equal to zero when $D = 0.5$, in (2- 56) and (2- 57), the second item in the root operator is then equal to zero. The RMS values of the voltage across the trap capacitor and inductor when $D = 0.5$ are therefore only dependent on V_{sn1}:

$$V_{C2} \cong \frac{4V_{sn1}}{3} = 0.6 \qquad (2\text{- }58)$$

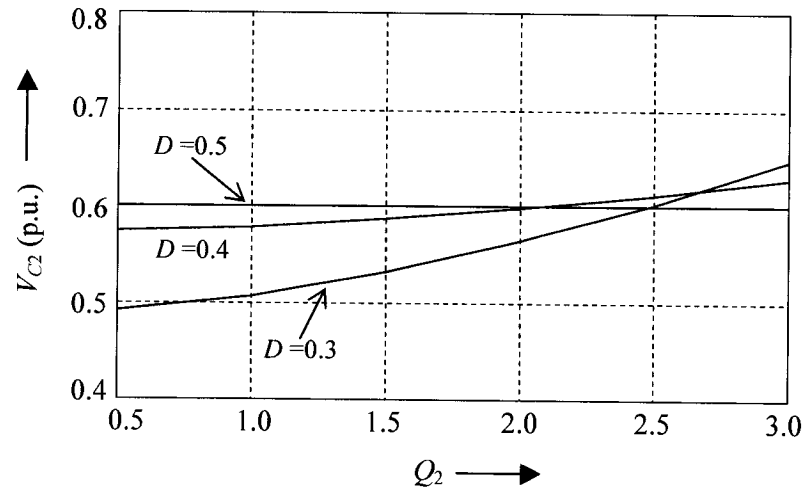
$$V_{L2} \cong \frac{V_{sn1}}{3} = 0.15 \qquad (2\text{- }59)$$

2.3.3.3 Contribution on the attenuation of the 3rd harmonic component

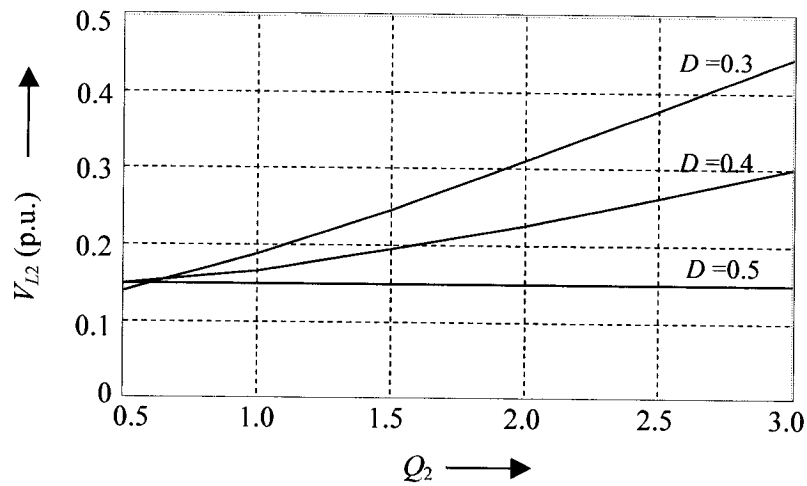
The 2nd harmonic trap has contribution on the attenuation of the 3rd harmonic component. As shown in Fig. 2- 18, the higher value of Q_2 provides more harmonic suppression when the duty cycle is close to 0.5. However, this suppression becomes less effective when Q_2 is greater than 2.



(a) RMS value of the current flowing through the 2nd harmonic trap



(b) RMS value of the voltage across the trap capacitor



(c) RMS value of the voltage across the trap inductor

Fig. 2- 17: RMS values of voltage & current of the 2nd harmonic trap components

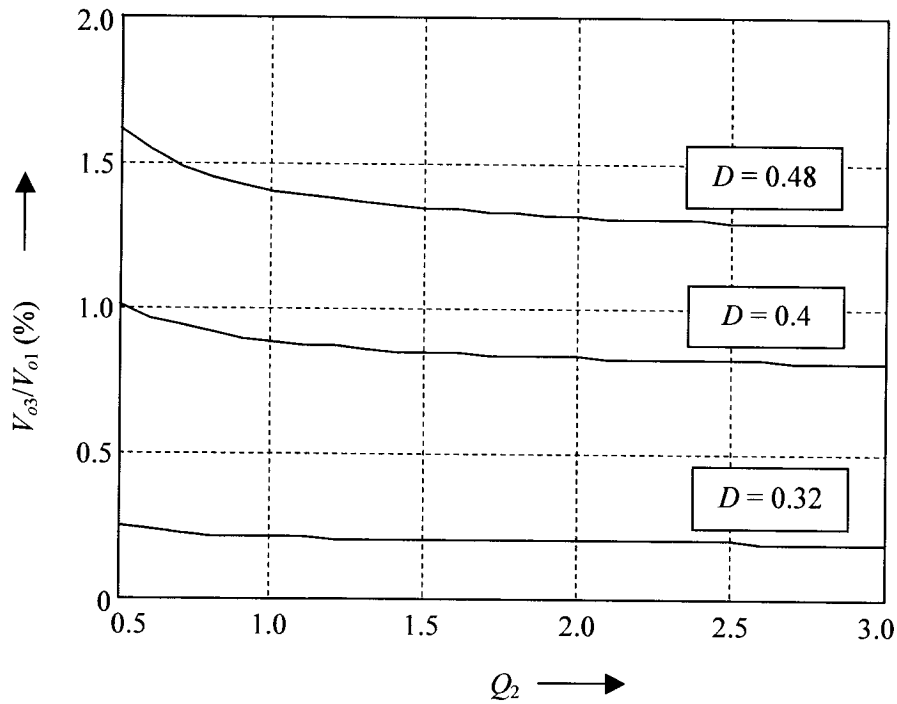


Fig. 2- 18: Effects of the 2nd harmonic trap on the attenuation of the 3rd harmonic

2.3.3.4 Effect of the tuning precision on the harmonic elimination

The 2nd harmonic cannot be eliminated completely because L_2 and C_2 cannot be tuned exactly at twice of the operating frequency. Theoretically, in the per unit system, the value of C_2 is given by:

$$C_2 = \frac{1}{4\omega_o Q_2} + e \qquad (2\text{- }60)$$

Where, $e = 0$. If a reasonable error of $e = 0.2\times10^{-9}$ is introduced into (2- 60), the 2nd harmonic component of the output voltage is re-calculated and plotted as a function of Q_2 in Fig. 2- 19. It can be seen that this harmonic component becomes significant at small duty cycle and at a higher value of Q_2.

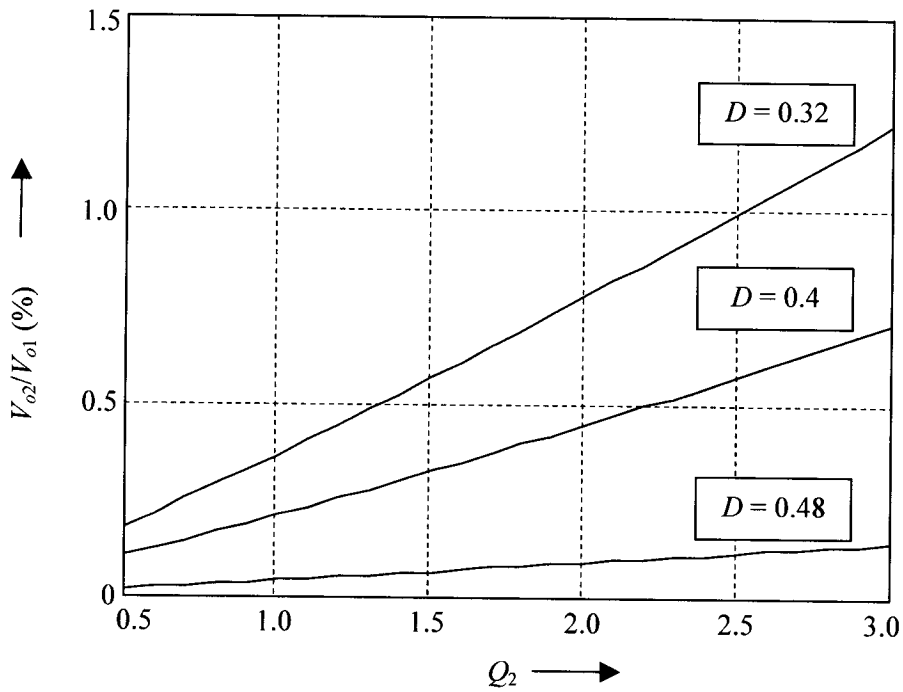


Fig. 2- 19: Normalized 2nd harmonic when its trap is not tuned exactly

2.3.4 Switch Stress and Utilization

Generally, the largest single cost in a converter is the cost of the active switches. Also, the conduction and the switching losses associated with the active switches often dominate the converter losses. Therefore, it is useful to calculate the total active switch stress and active switch utilization of the converter. To minimize the total silicon area required to realize the power devices of the converter, the total switch stress should be minimized and the switch utilization should be maximized.

In the proposed APWM inverter, there are two active switches employed in the chopper circuit. The total switch stress is defined as:

$$S = \hat{V}_{S1} I_{S1} + \hat{V}_{S2} I_{S2} \qquad (2\text{-}61)$$

Where, $\hat{V}_{S1}$ and $\hat{V}_{S2}$ are the peak voltage applied to the switch S_1 and switch S_2 respectively, which are equal to the dc input voltage V_d. I_{S1} and I_{S2} are the RMS current applied to the switch S_1 and switch S_2 respectively, which are given by (2- 49).

The switch utilization is defined as:

$$U = P_o / S \tag{2- 62}$$

Where P_o is the output load power.

The total switch stress and switch utilization of the proposed APWM inverter are plotted as a function of duty cycle D for different values of Q_s, Q_p and k_p in Fig. 2- 20 and Fig. 2- 21 respectively.

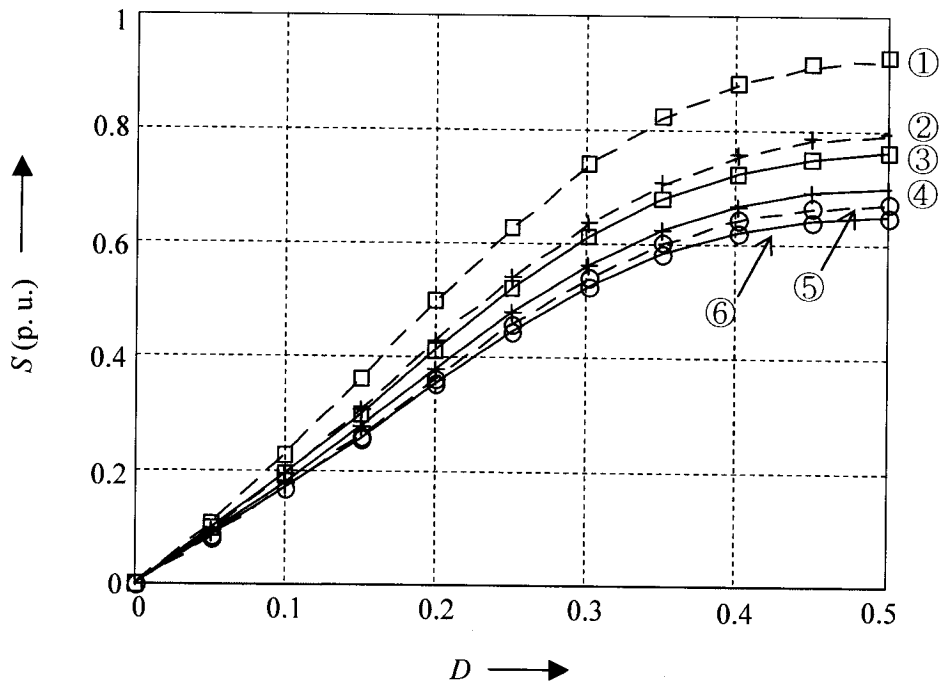


Fig. 2- 20: Total switch stress of the APWM inverter

(①: Q_s=Q_p=3, k_p=1.3, ②: Q_s=Q_p=3, k_p=1.2, ③: Q_s=Q_p=3, k_p=1.1,

④: Q_s=Q_p=2, k_p=1.3, ⑤: Q_s=Q_p=2, k_p=1.2, ⑥: Q_s=Q_p=2, k_p=1.1)

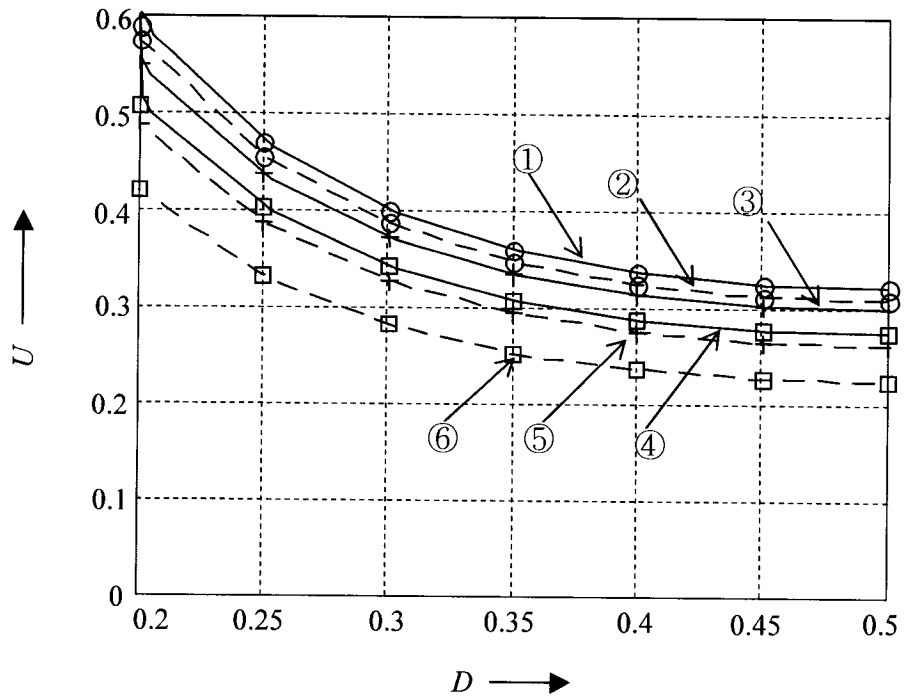


Fig. 2- 21: Switch utilization of the APWM inverter

(①: Q_s=Q_p=2, k_p=1.1, ②: Q_s=Q_p=3, k_p=1.1, ③: Q_s=Q_p=2, k_p=1.2,

④: Q_s=Q_p=2, k_p=1.3, ⑤: Q_s=Q_p=3, k_p=1.2, ⑥: Q_s=Q_p=3, k_p=1.3)

2.4 INVERTER INPUT CURRENT HARMONICS

In this section, the input current harmonics of the inverter are determined. The harmonic content of the input current determines the size of the inverter input filter for a specified percentage ripple superimposed on the dc voltage and current. The harmonic profile of the input current obtained in this section is used in Chapter 4 to design the input filter of the inverter.

Since the total harmonic distortion of the inverter output voltage is very low (less than 2%), only the fundamental component of the resonant current is considered to calculate the inverter per-unit input current:

$$i_{in} = \begin{cases} \dfrac{\hat{V}_{s2\_ac,1}}{|Z_{s1} + Z_{p1}|}\sin(\omega_o t + \theta_1 - \phi_1) & when \quad kT_s \le t < kT_s + DT_s \\ 0 & when \quad kT_s + DT_s \le t < (k+1)T_s \end{cases} \tag{2- 63}$$

Where

$$\hat{V}_{s2\_ac,1} = \frac{\sqrt{2}\sqrt{1-\cos(2\pi D)}}{\pi} \tag{2- 64}$$

$$Z_{s1} = jQ_s(1 - k_s^2/1) = 0 \tag{2- 65}$$

$$Z_{p1} = \frac{1}{1 + jQ_p(1/k_p^2 - 1) + j/(3Q_2)} \tag{2- 66}$$

$$\theta_1 = \arctan\left(\frac{\sin(2\pi D)}{1-\cos(2\pi D)}\right) \tag{2- 67}$$

$$\phi_1 = -\arctan\left(\frac{Q_p}{k_p^2} - Q_p + \frac{1}{3Q_2}\right) \tag{2- 68}$$

The input current of (2- 63) can be expressed by its Fourier series:

$$i_{in} = a_0 + \sum_{n=1}^{\infty}\left[a_n\cos(n\omega_o t) + b_n\sin(n\omega_o t)\right] \tag{2- 69}$$

Where

$$a_0 = -\frac{1}{2\pi}\frac{\hat{V}_{s2\_ac,1}}{|Z_{p1}|}\left[\cos(2\pi D + \theta_1 - \phi_1) - \cos(\theta_1 - \phi)\right] \tag{2- 70}$$

$$a_1 = \frac{1}{2\pi}\frac{\hat{V}_{s2\_ac,1}}{|Z_{p1}|}\left[2\pi D\sin(\theta_1 - \phi_1) - \frac{1}{2}\left(\cos(4\pi D + \theta_1 - \phi_1) - \cos(\theta_1 - \phi_1)\right)\right] \tag{2- 71}$$

$$a_n = \frac{1}{2\pi}\frac{\hat{V}_{s2\_ac,1}}{|Z_{p1}|}\left(A_n + B_n\right) \qquad n = 2, 3, 4\ldots \tag{2- 72}$$

$$A_n = -\frac{1}{n+1}\left(\cos(2\pi(n+1)D + \theta_1 - \phi_1) - \cos(\theta_1 - \phi_1)\right) \tag{2- 73}$$

$$B_n = -\frac{1}{1-n}\left(\cos(2\pi(1-n)D + \theta_1 - \phi_1) - \cos(\theta_1 - \phi_1)\right) \quad (2\text{-}74)$$

$$b_1 = -\frac{1}{2\pi}\frac{\hat{V}_{s2\_ac,1}}{|Z_{p1}|}\left[-2\pi D\cos(\theta_1 - \phi_1) + \frac{1}{2}\left(\sin(4\pi D + \theta_1 - \phi_1) - \sin(\theta_1 - \phi_1)\right)\right] \quad (2\text{-}75)$$

$$b_n = -\frac{1}{2\pi}\frac{\hat{V}_{s2\_ac,1}}{|Z_{p1}|}(C_n + D_n) \qquad n = 2, 3, 4\ldots \quad (2\text{-}76)$$

$$C_n = \frac{1}{n+1}\left(\sin(2\pi(n+1)D + \theta_1 - \phi_1) - \sin(\theta_1 - \phi_1)\right) \quad (2\text{-}77)$$

$$D_n = -\frac{1}{1-n}\left(\sin(2\pi(1-n)D + \theta_1 - \phi_1) - \sin(\theta_1 - \phi_1)\right) \quad (2\text{-}78)$$

Equation (2- 69) shows that the input current contains dc component and harmonics. The RMS value of the nth harmonic content is given by:

$$I_{in}(1) = \frac{1}{\sqrt{2}}\sqrt{a_1^2 + b_1^2} \quad (2\text{-}79)$$

and

$$I_{in}(n) = \frac{1}{2\sqrt{2}\pi}\frac{\hat{V}_{s2\_ac,1}}{|Z_{p1}|}\sqrt{A_n^2 + B_n^2 + C_n^2 + D_n^2} \quad (2\text{-}80)$$

Fig. 2- 22 shows the first five harmonic components (n = 1, 2, 3, 4, and 5 respectively) of the inverter input current for Q_s = 2, Q_p = 2, k_p = 1.2. It can be seen that the first harmonic component (n = 1) is dominant. Fig. 2- 23 shows the RMS value of this component as a function of the duty cycle for different values of Q_p and k_p.

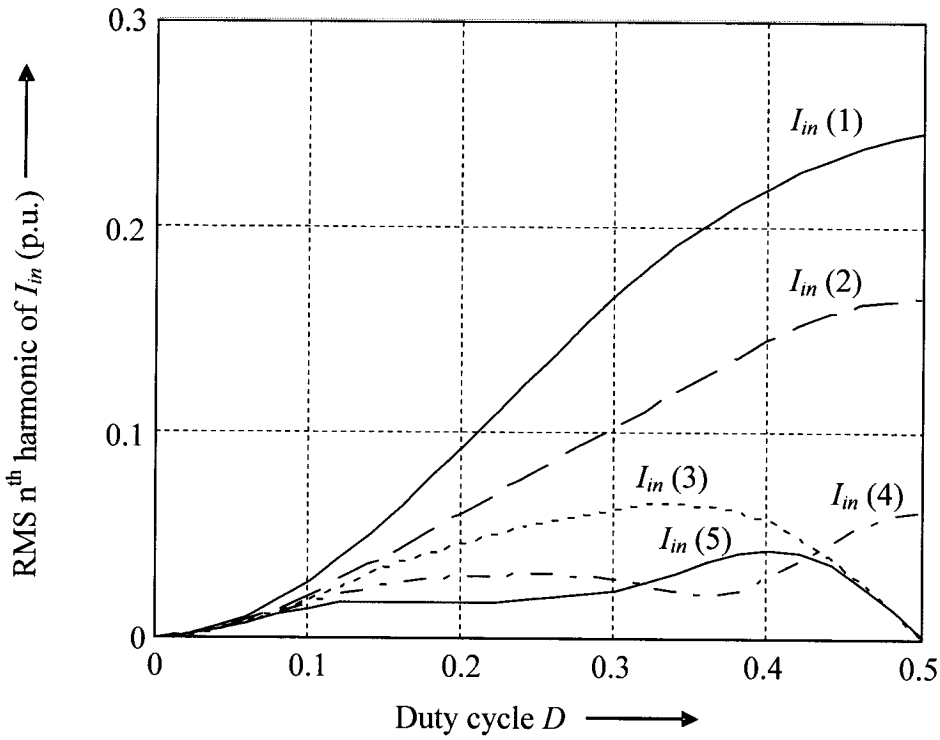


Fig. 2- 22: RMS harmonic components of the inverter input current

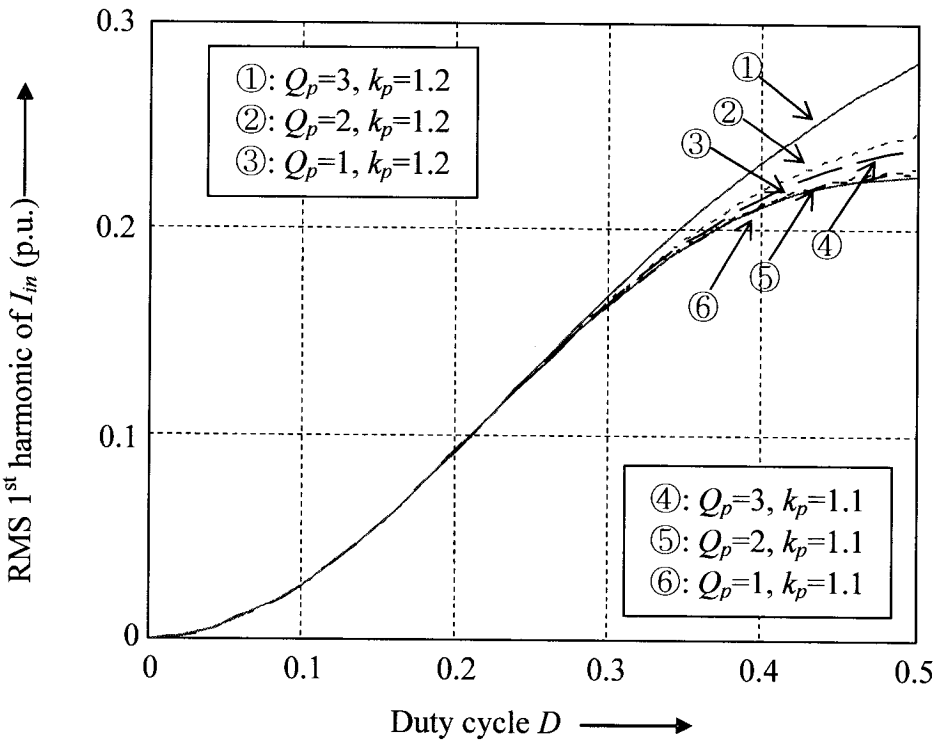


Fig. 2- 23: RMS harmonic component $I_{in}(1)$ of the inverter input current

2.5 DYNAMIC ANALYSIS OF THE APWM RESONANT INVERTER

In this section, the feedforward control techniques are first reviewed. Among these techniques, the modulated integral control is found to be the best choice for the feedforward control employed in the APWM resonant inverter. The implementation and operation principle of the modulated integral control are described in section 2.5.1. However, as shown in section 2.5.2, the inverter dynamic performance cannot achieve excellent transient response against the line and load variation with a single control loop (either feedforward loop or feedback loop alone). Therefore, a control scheme which consists of both feedforward and feedback control is proposed in 2.5.3. Then some design and stability considerations are illustrated in 2.5.4. Finally in 2.5.5, the simulation results of the inverter dynamic performance with the proposed control scheme are presented as design verification.

2.5.1 Feedforward Control Using Modulated Integral Control Technique

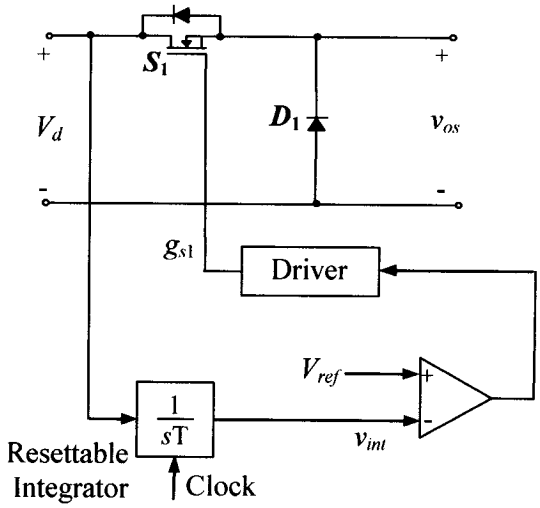
2.5.1.1 Review of the Feedforward Control

Voltage feedforward control techniques have been used in switch mode power converters to suppress the effect of input line harmonics and disturbances [65-67]. Conventionally, voltage feedforward control can be implemented by measuring the input voltage and integrating it through a resettable integrator. The implementation circuit is shown in Fig. 2- 24(a) and its key operating waveforms are shown in Fig. 2- 24(b).

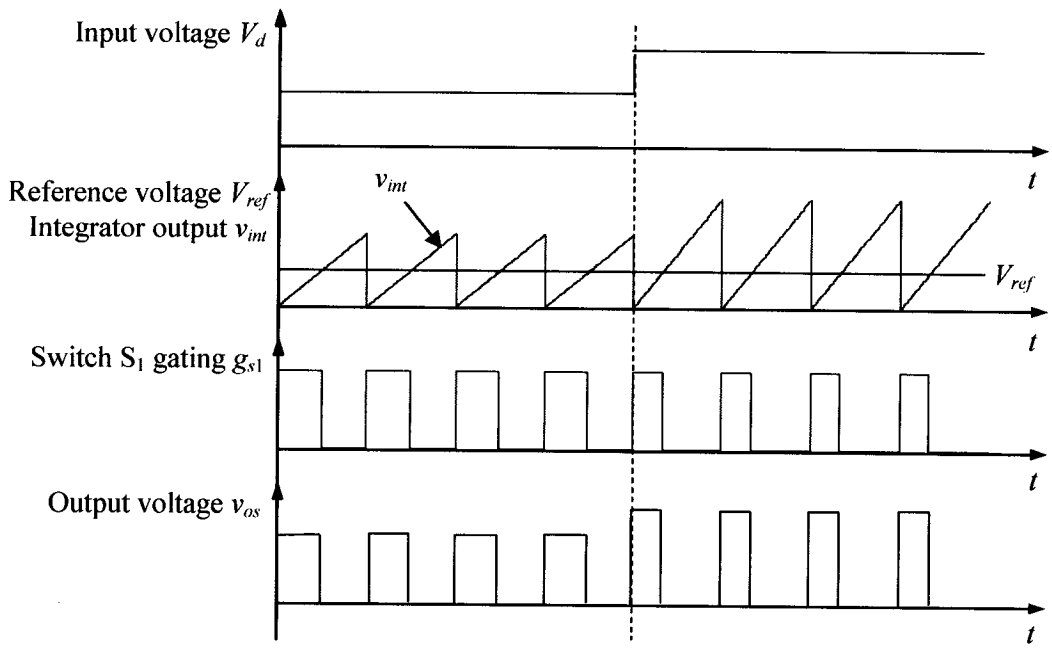
The on-time of the gating pulse is governed by:

$$t_{on} = \frac{V_{ref}}{V_d}\tau \qquad (2\text{-}81)$$

Where τ is the integral time constant, V_d is the DC input voltage, and V_{ref} is the amplitude of the reference voltage. The feedforward effect can be illustrated by (2- 81): As the input voltage increases, the on-time decreases and the output of the chopper should keep the same against the line variations.



(a) Circuit diagram



(b) Operating waveforms

Fig. 2- 24: Conventional feedforward control – circuit and waveforms

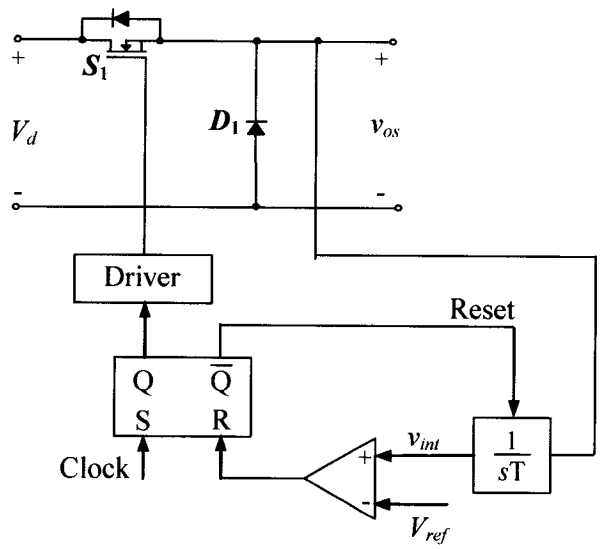
However, this technique does not consider the switch imperfections. To overcome this drawback, one-cycle control is proposed in early 90's [67]. This control technique is derived from the concept of keeping the average value of the chopper output voltage constant against the line variation. In this control scheme, as shown in Fig. 2- 25, the chopper output voltage is integrated and compared with a control reference. As soon as the integrator output reaches the reference, the switch is turned off and the integrator is reset to zero.

Compared to the conventional feedforward control, the voltage drop due to the switch conduction losses is inherently taken into account in the one-cycle control, because it is the output voltage of the chopper who is being integrated. However, the switch delays will still introduce extra volt-seconds at the integrator output, which results in a small deviation of the chopper output voltage away from the expected value.

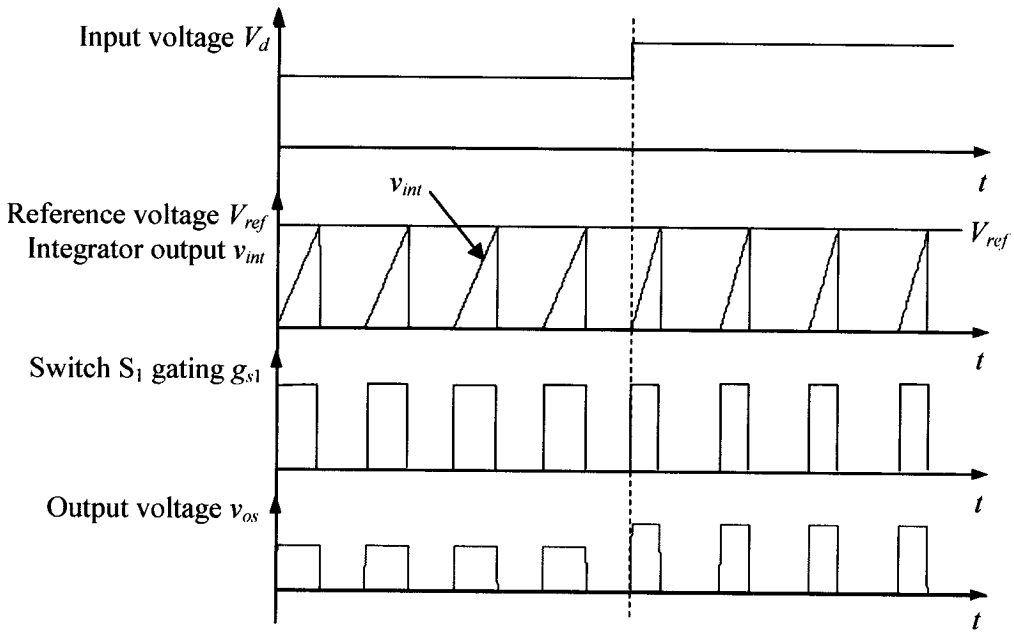
To minimize the influence of input voltage source and switch imperfections (including switch conduction losses and delays) on the chopper output voltage, a feedforward loop using modulated integral duty-cycle control is introduced in the next section.

2.5.1.2 Implementation and operation principle of the modulated integral control

Fig. 2- 26 shows the feedforward loop of the APWM resonant inverter under modulated integral control [68-69]. In Fig. 2- 26, only the chopper circuit of the APWM inverter is redrawn because only the feedforward loop is discussed in this section.



(a) Circuit diagram



(b) Operating waveforms

Fig. 2- 25: One-cycle control – circuit and waveforms

In the proposed feedforward loop, as shown in Fig. 2- 26, the difference between the output voltage of the chopper and the reference voltage is integrated. The integrator output is then compared with a triangular carrier wave to generate the gating pulses.

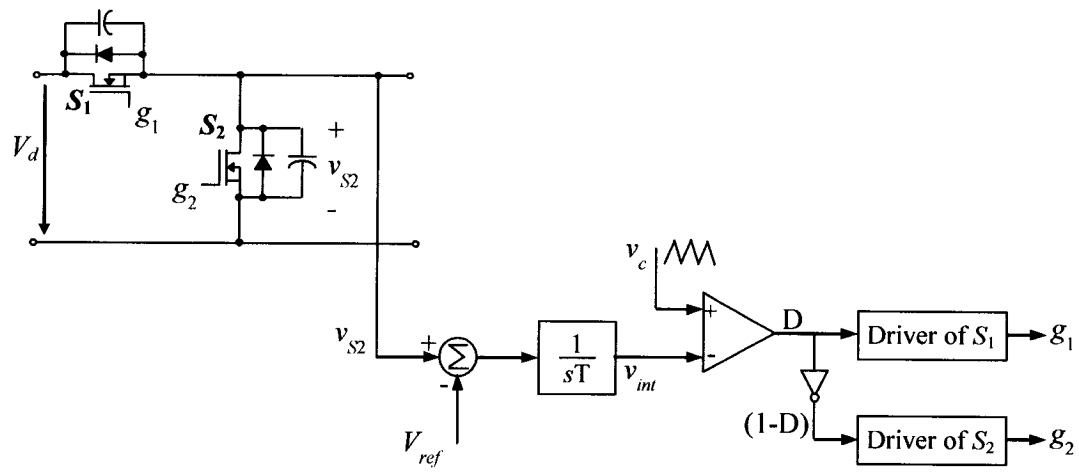


Fig. 2- 26: Proposed feedforward loop using modulated integral control technique

The major difference between this control technique and the one-cycle control is that the integrator is not reset at each cycle. Rather, the information from previous cycles is retained utilized in the next cycle. In this way, any errors introduced by the switch imperfection can be corrected.

In a summary, compared to other control techniques (such as typical voltage feedback control or current-mode control), modulated integral duty-cycle control has the following additional advantages:

(i) It has the advantages similar to the conventional feedforward control technique, i.e. simple implementation and good dynamic response.

(ii) The control loop is stable and is insensitive to noise.

(iii) It provides good pre-regulation since the errors introduced by the switch conduction losses and delays can be corrected.

The operating principles of the modulated integral control can be illustrated by the circuit waveforms shown in Fig. 2- 27. When the input voltage is increased (or the

switching delay is increased), the volt-seconds of the chopper output will increase. This results in the increase of the integrator output beyond its previous intersection with the carrier waveform. Consequently, the modulation wave v_{int} is shifted upward to give a small duty cycle for the next switching cycle, so that the line variation and the switching delay are compensated.

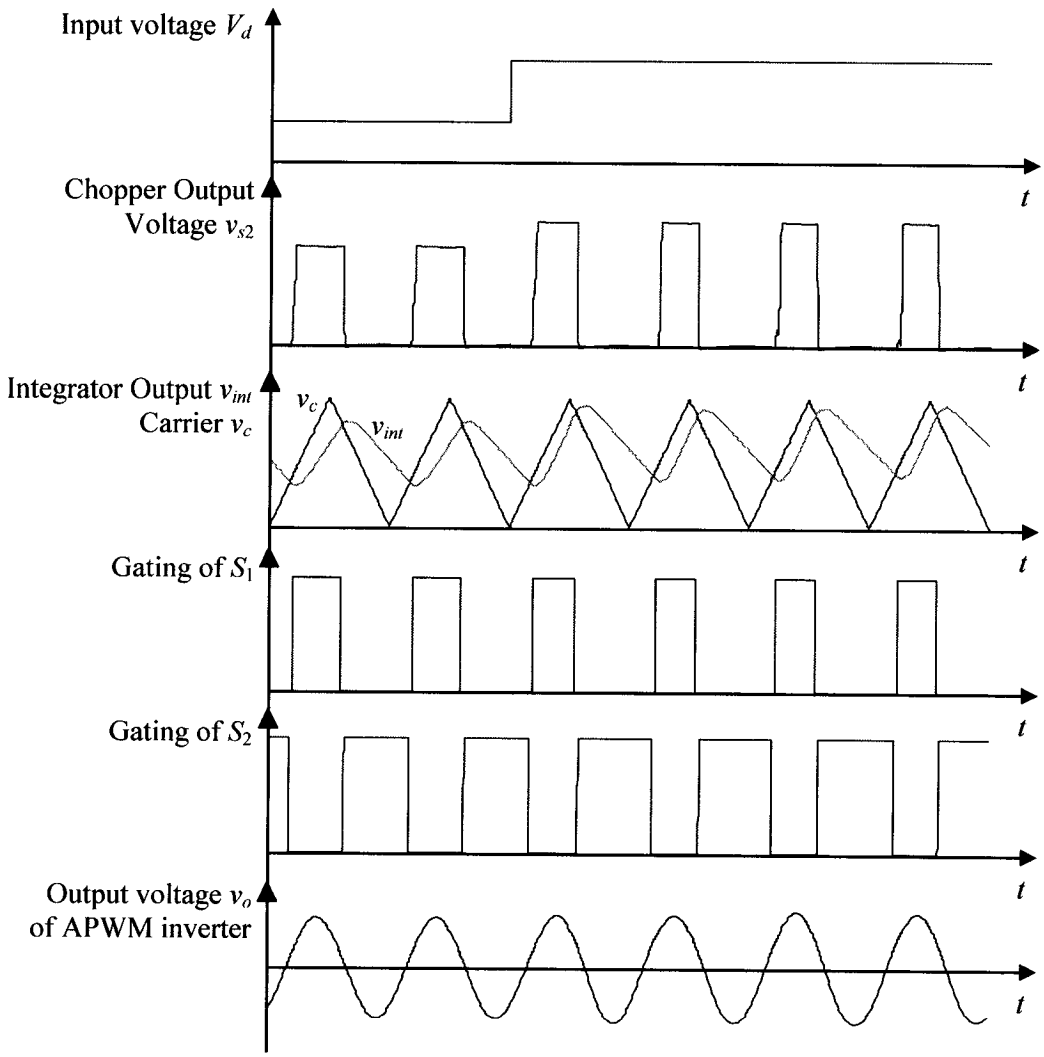


Fig. 2- 27: Operating waveforms of the modulated integral control

2.5.2 Inverter Performance with a Single Control Loop

The performance of the proposed feedforward control – modulated integral control is investigated by using the simulation tool PSPICE. To simulate the inverter response against the line variation, the DC piecewise linear voltage source at the input of the inverter has an initial value of 60V, and steps up to 75V at certain time. The key operating waveforms of the inverter during the transient is shown in Fig. 2- 28.

To compare the transient response of the inverter using only feedforward control with the inverter using only feedback control, a feedback loop including a feedback rectifier and a type-II error amplifier (EA) is used at the output of the inverter to generate the gating signals. The simulation results are shown in Fig. 2- 29.

By comparing Fig. 2- 28 with Fig. 2- 29, the following points can be concluded:

(i) The feedforward control has faster transient response. When the line variation occurs, the gating signals (duty cycle) change exactly and immediately in one cycle. The instantaneous control of the average value of the chopped voltage is achieved. The output voltage is disturbed because of the dynamics of the resonant circuits. However,

(ii) The feedforward modulated integral control has big steady-state error (10%) due to the conduction losses of the resonant circuits and the matching transformer.

(iii) The feedback control has slower transient response (The output of EA takes about 8 cycles to be stable). But,

(iv) The steady-state error using feedback control can be well corrected.

To achieve fast transient response against the line and load variation, and meanwhile, eliminate the steady-state error completely, a combined feedforward modulated integral control with the feedback control is proposed in the next section.

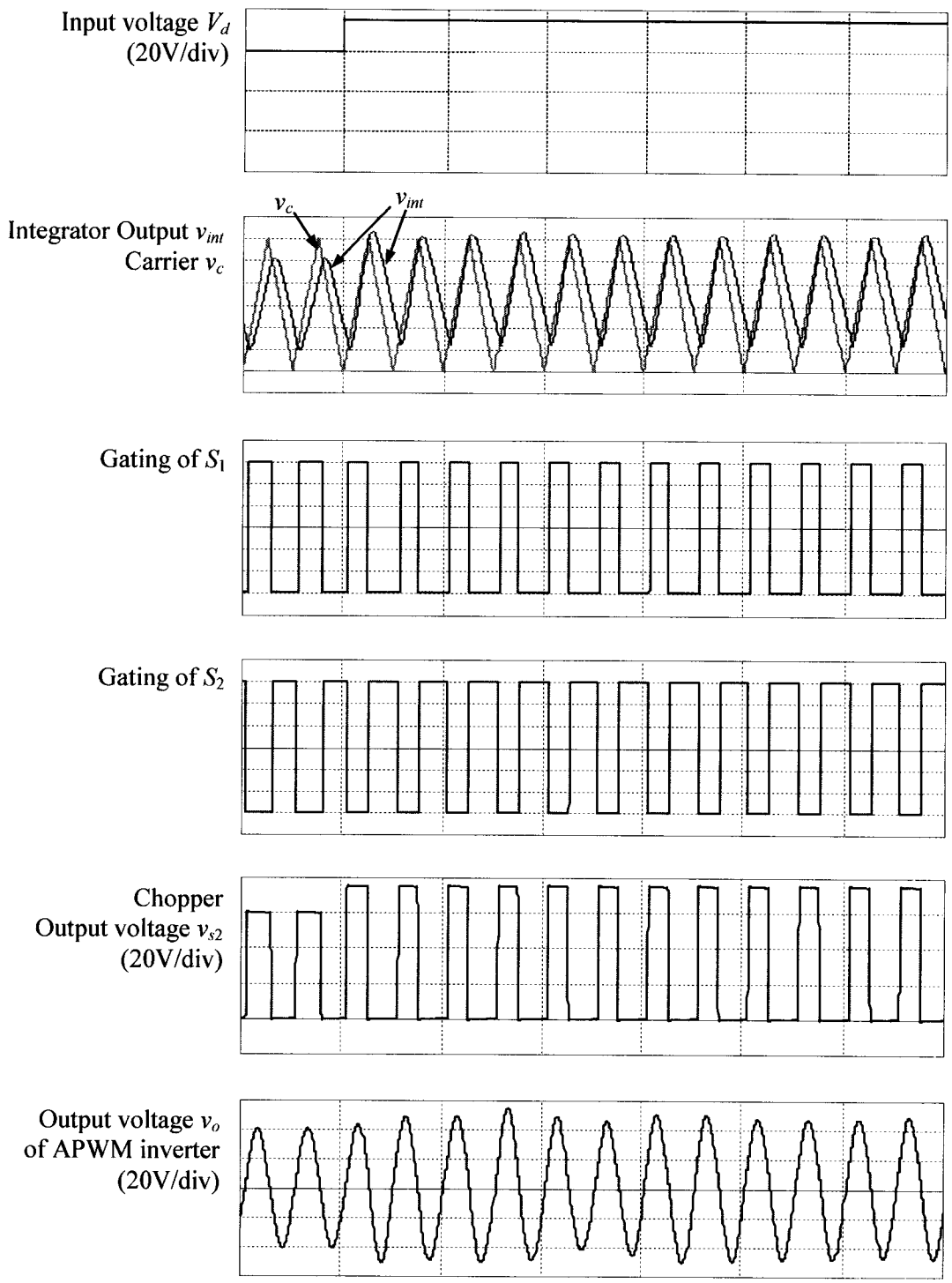


Fig. 2- 28: Operating waveforms of the APWM inverter with only feedforward control when input voltage steps up from 60V to 75V (Time scale: 2μs/div)

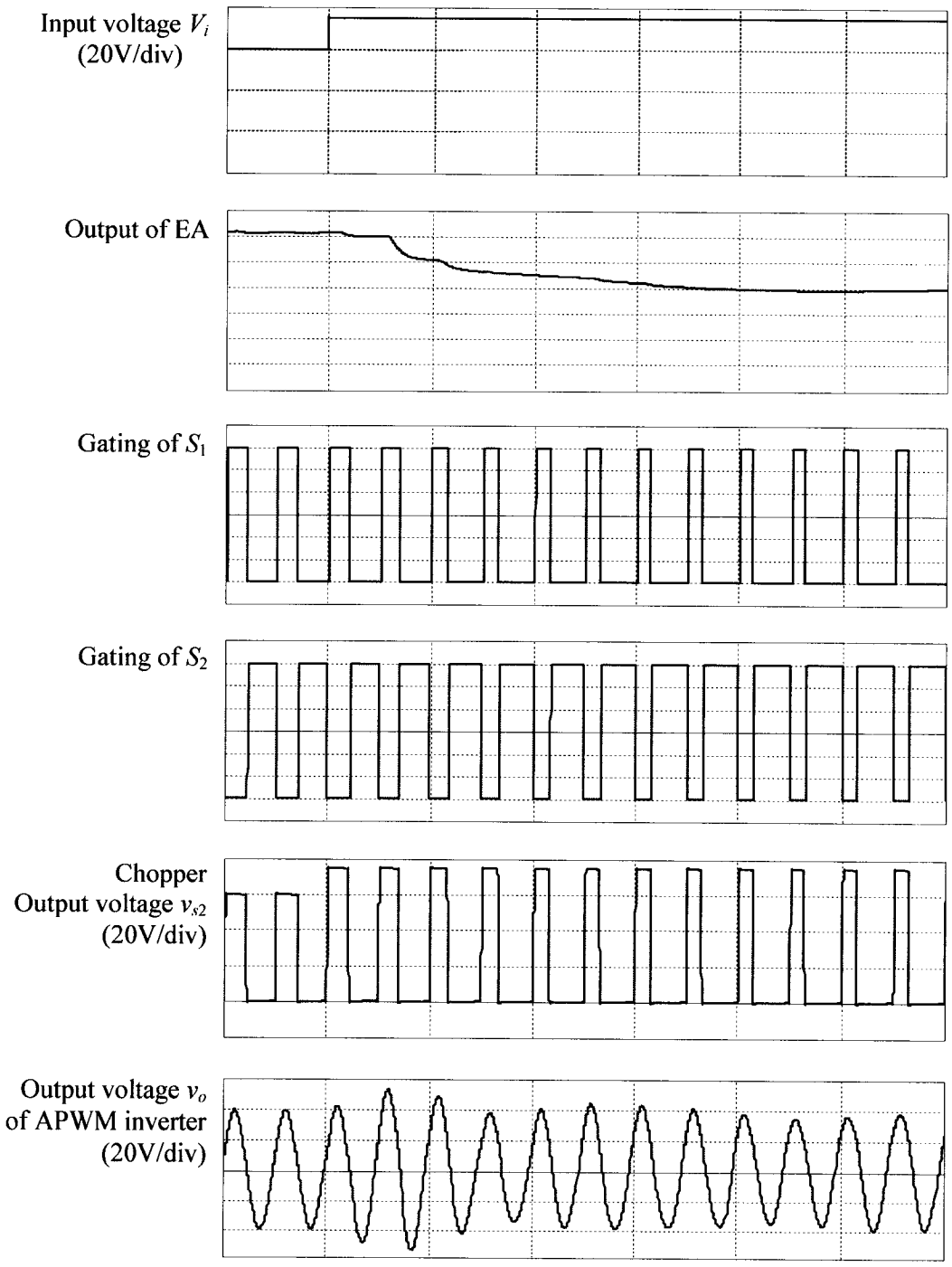


Fig. 2- 29: Operating waveforms of the APWM inverter with only feedback control when input voltage steps up from 60V to 75V (Time scale: 2μs/div)

2.5.3 Proposed Control Scheme – Combination of Feedforward and Feedback Control

The proposed control scheme of the APWM resonant inverter is shown in Fig. 2-30. In this control scheme, the feedforward loop uses modulated integral control to provide pre-regulation for the feedback loop. The feedback loop consists of a sampling network K_s, a rectifier and a type-II error amplifier (EA) which is designed to compensate the resonant tanks of the inverter and the output filter of the feedback rectifier.

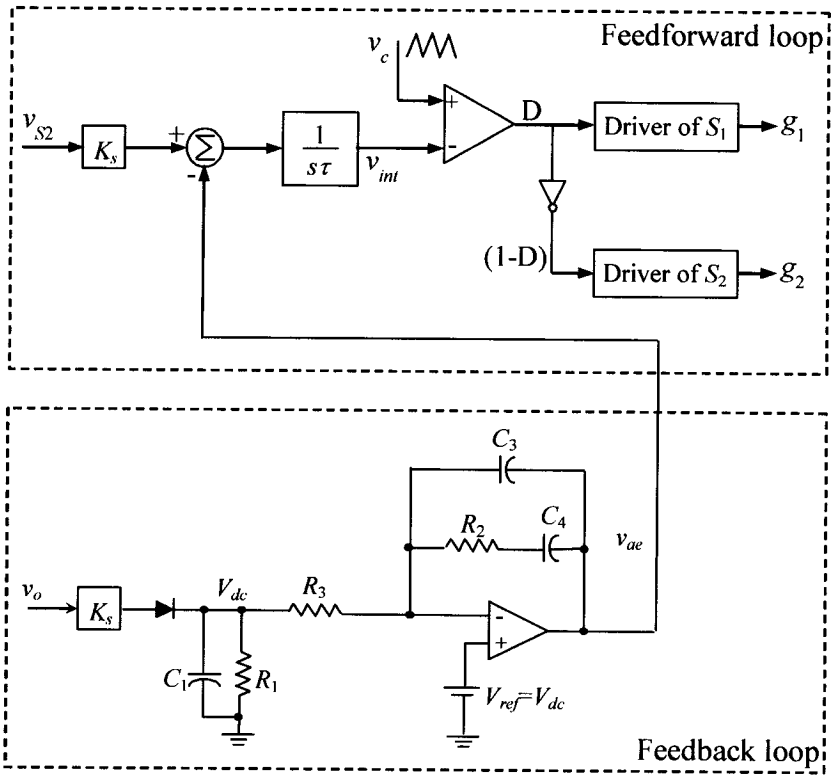


Fig. 2- 30: Proposed control scheme of the APWM resonant inverter

The difference between the proposed control loop and the modulated integral control introduced in section 2.5.1 is that: instead of using a constant DC voltage as the reference signal, the output of the error amplifier of the feedback loop is used to correct the steady-state error.

2.5.4 Design Considerations and Stability of the Proposed Control Scheme

The design considerations and stability of the proposed control scheme are illustrated on the base of the following design example:

Input voltage of the inverter: V_d = 60 V – 75 V

Output of the inverter: V_o = 28 Vrms, P_o = 200 W

Turns ratio of the transformer: N = 0.9

Circuit parameters: L_s = 1.2 μH, C_s = 21.1 nF (Q_s = 2)

L_p = 0.29 μH, C_p = 66.2 nF (Q_p = 2, k_p = 1.15)

L_2 = 1.2 μH, C_2 = 5.28 nF (Q_2 = 2)

2.5.4.1 Selection of the modulated integral time constant

The selection of the integrator time constant τ is based on the principle that the rising and falling slopes of the modulation wave (output of the integrator v_{int}) must be smaller than those of the carrier wave v_c. If the carrier wave is scaled such that its peak value equals the product of the DC input voltage V_d and the sampling gain K_s, the rising and falling slopes of the carrier wave will be $2K_sV_d/T_s$ (T_s is the switching period). On the other hand, the rising and falling slopes of the modulation wave are $(K_sV_d\text{-}v_{ae})/\tau$ (rising) and v_{ae}/τ (falling). Therefore, the integral time constant τ is limited by (detailed derivation is illustrated in Appendix A):

$$\frac{v_{ae}}{\tau} < \frac{2K_sV_d}{T_s} \tag{2- 82}$$

and

$$\frac{K_sV_d - v_{ae}}{\tau} < \frac{2K_sV_d}{T_s} \tag{2- 83}$$

Considering the duty cycle of switch S_1 is $D = v_{ae} / (K_s V_d)$, (2- 82) and (2- 83) become:

$$\tau > \frac{D}{2} T_s \tag{2- 84}$$

and

$$\tau > \frac{1-D}{2} T_s \tag{2- 85}$$

According to the output voltage control derived in section 2.2.3, the maximum value of the duty cycle is D_{max} = 0.5 when V_{d_min} = 60V. When V_{d_max} = 75V, the minimum value of the duty cycle D_{min} can be derived from (2-14):

$$D_{\min} = \frac{\arccos\left[1-\left(\sqrt{2}V_{d\_min}/V_{d\_max}\right)^2\right]}{2\pi} \tag{2- 86}$$

Which is D_{min} = 0.3.

Substituting D_{max} into (2- 84) and D_{min} into (2- 85) respectively, the minimum value of the integral time constant should be greater than the larger value of (2- 84) and (2- 85), which is τ > 0.35 μs. Therefore, τ = 0.4 μs is used in the simulation and experimental setups.

2.5.4.2 Design of the feedback loop

(1) Sampling network and feedback rectifier

Because most frequently used error amplifier cannot tolerate more than 3 V at its reference input, a sampling network with gain K_s = 0.1 is needed to reduce the inverter output voltage from 28 V to 2.8 V (RMS value). Then this voltage is rectified to a DC voltage to be fed to the error amplifier.

The output filter of the feedback rectifier consists of a capacitor C_1 and a discharging resistor R_1. Selection of the values of C_1 and R_1 should satisfy: (i) The corner frequency $f_{RC} = 1/(2\pi R_1 C_1)$ should be as high as possible (>200 kHz, which is the one-fifth of the switching frequency) to maintain a wide bandwidth of the control loop. (ii) The time constant R_1C_1 should be high enough to maintain a sufficient DC value at the output of the rectifier. In this design, C_1 and R_1 are chosen as: $C_1 = 0.1$ μF and $R_1 = 5$ Ω.

(2) Error amplifier

The mathematical tool – the K factor is used to synthesize an error amplifier (EA) [70-71]. The procedure is described as follows.

Step 1: Make a Bode plot of the control-to-output transfer function

To determine the appropriate compensation in the feedback loop for the desired steady-state and transient response, the linearized dynamic model of the APWM inverter with the proposed control scheme is developed, as shown in Fig. 2- 31.

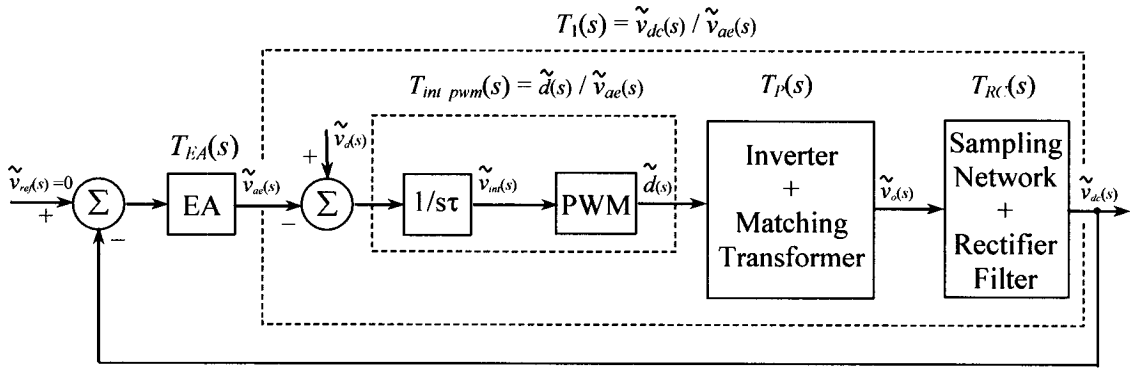


Fig. 2- 31: Dynamic model of the APWM inverter with the proposed control scheme

The control-to-output transfer function is defined as the transfer function between the output of the feedback rectifier and the output of the error amplifier:

$$T_1(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{v}_{ae}(s)} \tag{2- 87}$$

As derived in Appendix B, the frequency characteristics of the control-to-output transfer function are illustrated in Fig. 2- 32.

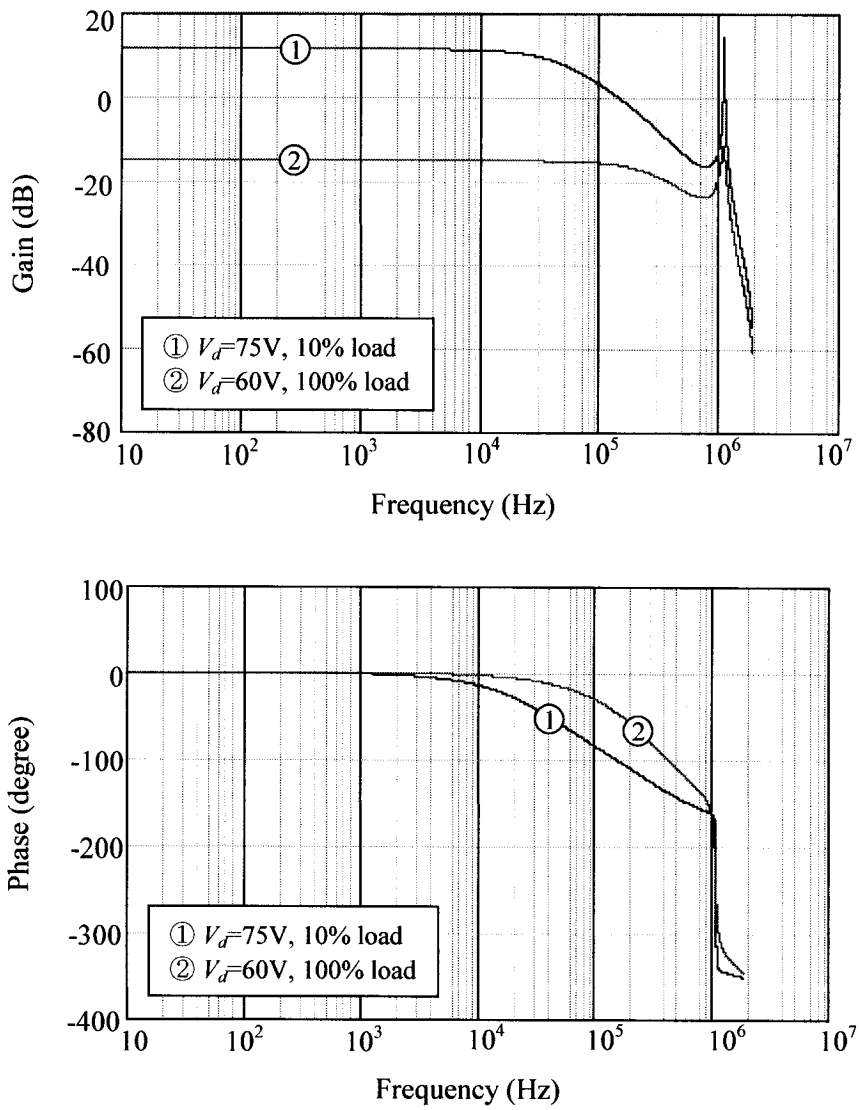


Fig. 2- 32: Bode plot of the control-to-output transfer function of the inverter

The Bode plot of Fig. 2- 32 shows that at low frequency zone, the original pole introduced by the feedforward integrator and original zero introduced by the APWM resonant inverter make the horizontal gain slope. At high frequency zone, the control-to-output transfer function has a pole at frequency of 318 kHz which is introduced by the filter of the feedback rectifier, and two pairs of poles at frequency around 1 MHz which are introduced by the series-parallel resonant tanks of the APWM inverter.

Step 2: Choose a crossover frequency:

As seen from the Bode plot of the control-to-output transfer function (Fig. 2- 32), the loop gain and the phase shift are different for various line and load conditions. The error amplifier is designed considering the worst-case operation (V_d=75 V, 10% load). The overall crossover frequency F_{co} is chosen at 150 kHz and the frequency characteristic of the error amplifier will be shaped to provide the total open loop gain slope of –1 and the desired phase margin (between 30° to 90°) at the crossover frequency. For the nominal operation case (V_d =60 V, 100% load), the same stability criteria will be verified.

Step 3: Choose the desired phase margin:

Since very large load transient is expected for the APWM resonant inverter, a desired phase margin of 50° under the worst case operation is chosen to yield well-damped load transient response.

Step 4: Determine the required amplifier gain:

This gain G_{EA} is the required amplifier gain at the crossover frequency and must equal the control-to-output loss under the worst case operation. When expressed in decibels, G_{EA} is simply the negative of the control-to-output gain which is -0.35 dB in Fig. 2- 32. Therefore, in this design, G_{EA} = 0.35 dB (or 1.04 in numerical value).

Step 5: Calculate the required phase boost:

The amount of phase boost at the crossover frequency required from the zero-pole pair of the amplifier is given by:

$$Boost = M - P - 90° \tag{2-88}$$

Where M is the desired phase margin which is 50°, and P is the phase shift of the control-to-output transfer function which is –99° under the worst case operation from Fig. 2- 32. Therefore, in this design, $Boost = 60°$.

Step 6: choose the error amplifier type:

Since the required phase boost is less than 90°, type-II error amplifier is chosen, and its circuit diagram is shown in Fig. 2- 30.

Step 7: Calculate the K factor:

The K factor can be calculated using (2- 89):

$$K = \tan\left(\frac{boost}{2} + 45\right) \tag{2-89}$$

Therefore $K = 4.0$ is used in this design.

Step 8: Calculate the circuit parameters of the error amplifier:

The type-II error amplifier has a zero at frequency F_z ($F_z = F_{co} / K = 37.5$ kHz), and a pole at frequency F_p ($F_p = K \cdot F_{co} = 600$ kHz). Its transfer function is given by:

$$T_{EA}(s) = \frac{1 + sR_2C_4}{sR_3(C_4 + C_3)(1 + sR_2C_3)} \tag{2-90}$$

If R_3 is arbitrarily taken as 1 kΩ, the parameters in (2- 90) are found out as:

$$R_2 = G_{EA}R_3 = 1.0 \quad k\Omega \tag{2-91}$$

$$C_4 = \frac{1}{2\pi F_z R_2} = 4.2 \quad nF \tag{2-92}$$

$$C_3 = \frac{1}{2\pi F_p R_2} = 265 \quad pF \tag{2-93}$$

Following the above steps, the Bode plot of the total open loop (T(s) = T_1(s)T_{EA}(s)) is finally presented in Fig. 2- 33.

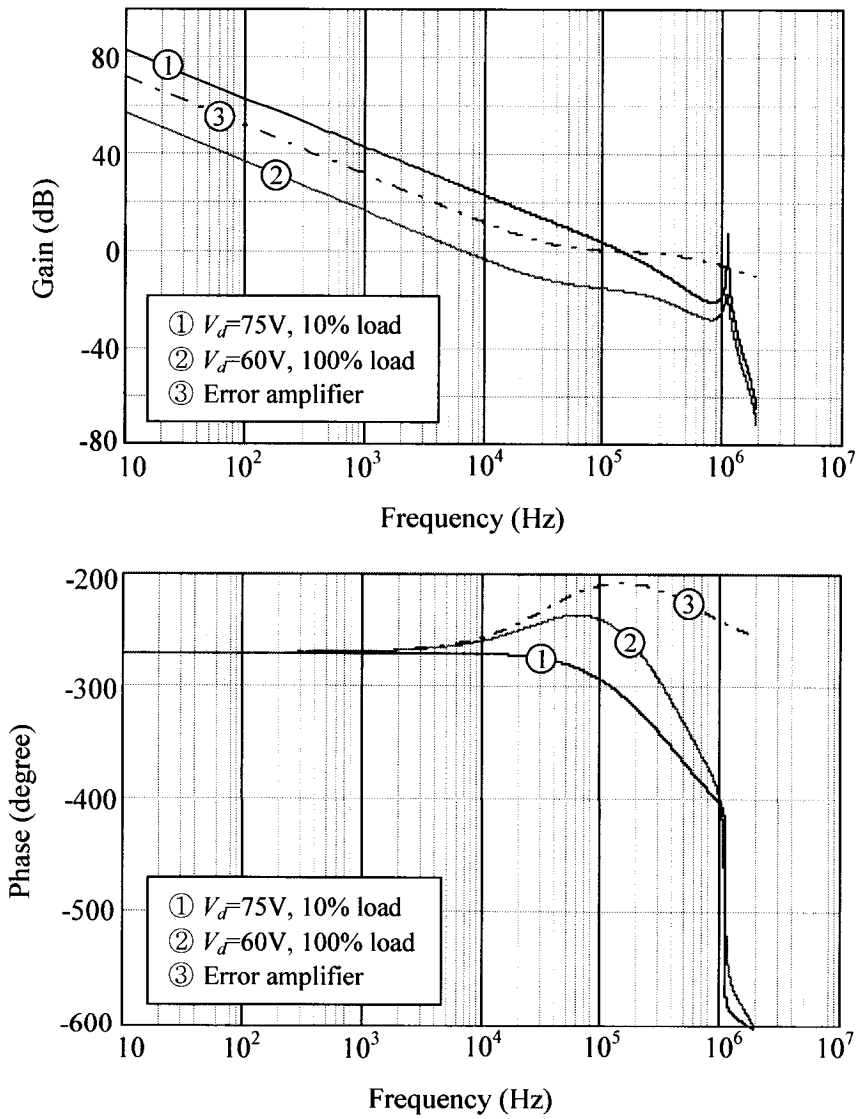


Fig. 2- 33: Bode plot of the EA and overall open loop circuit

It can be seen that the feedback loop satisfies the following criteria:

(i) The slope of the overall open loop gain at the crossover frequency is –20 dB/decade for either the worst or the nominal operation condition;

(ii) Phase margin of 53° for the worst operation condition and phase margin of 56° for the nominal operation condition are all within the range of safe value to yield well-damped transient response.

Therefore, the overall circuit stability and good transient response should be achieved. The closed-loop stability and transient response against the line and load variation will be examined in the next section.

2.5.5 Dynamic Performance of the APWM Resonant Inverter with the Proposed Control Scheme

Usually, for the HFAC distributed power system in the desktop computer, any disturbance or noise from the dc source and/or power management of the motherboard may cause large signal transients in both input voltage and load current. The proposed control scheme is employed in the APWM resonant inverter and its dynamic performance against the line and load variation is investigated by using the simulation tool PSpice. The simulation circuit (PSpice model of the APWM resonant inverter) is shown in Appendix D, and has the same circuit parameters as those used in section 2.5.4. The simulation results are shown in Fig. 2- 34 and Fig. 2- 35.

In Fig. 2- 34, thanks to the feedforward control loop, the input voltage perturbations can be completely rejected within very few switching cycles. During the line variation, the envelope of the output voltage has negligible change.

Fig. 2- 35 shows that the proposed control scheme provides good response to the large load transients. In Fig. 2- 35 (a) and (b), when the load changes from 50% load to full load and vice versa, the output voltage can reach the steady state within 4 cycles. In Fig. 2- 35 (c) and (d), when the load changes from 10% load to full load, the output voltage takes about 4 cycles to go back to the steady state. When the load changes from full load to 10% load, the output voltage takes about 10 μs to be stable again.

In Fig. 2- 35, the energy corresponding to the positive load current change is sourced by the dc source and the energy stored in the resonant circuit. During the negative load current change, the energy is partly stored in the resonant circuit and partly damped through the load resistance. Therefore, the following phenomena can be noticed in Fig. 2- 35:

(i) The recovery time during the positive load current change is almost same, either from 10% to full load or from 50% to full load;

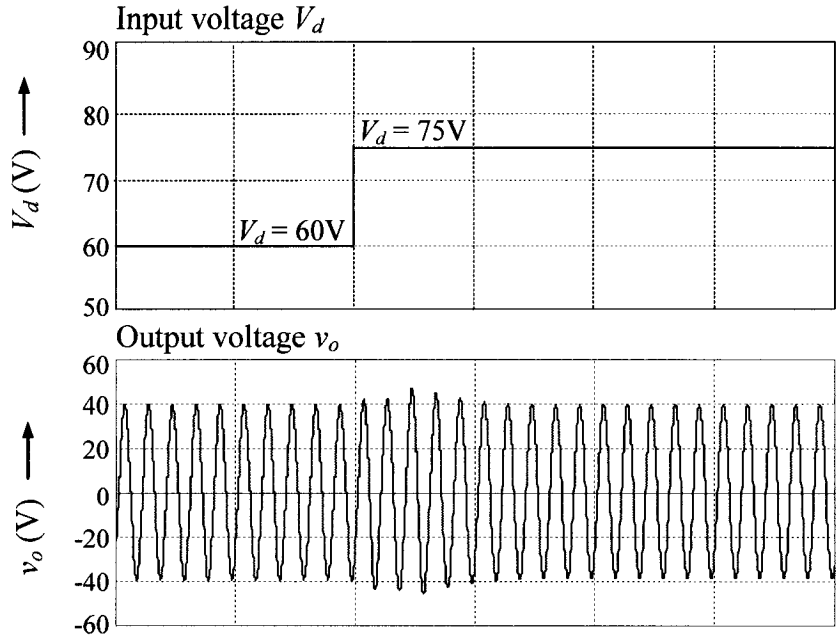
(ii) Under the very large load transient, from 10% to full load and vice versa, the recovery time during the positive load current change is much faster than that during the negative load current change. The lighter the load is, the longer recovery time the inverter takes.

After all, the proposed control scheme presents the desired dynamic performance:

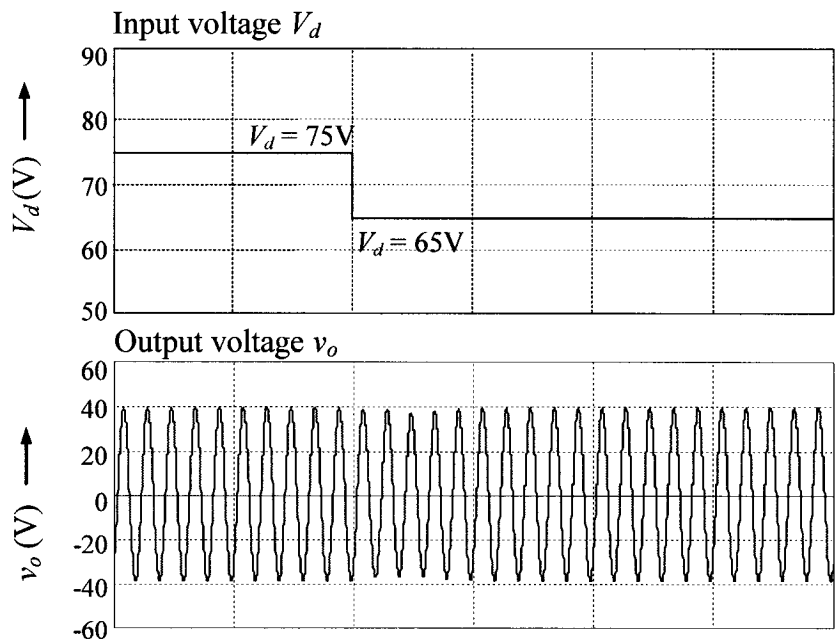
(i) The inverter operation is stable under large signal transients;

(ii) The feedforward loop provides pre-regulation for the feedback loop to speed up the transient response;

(iii) The feedback loop corrects the steady-state error completely.

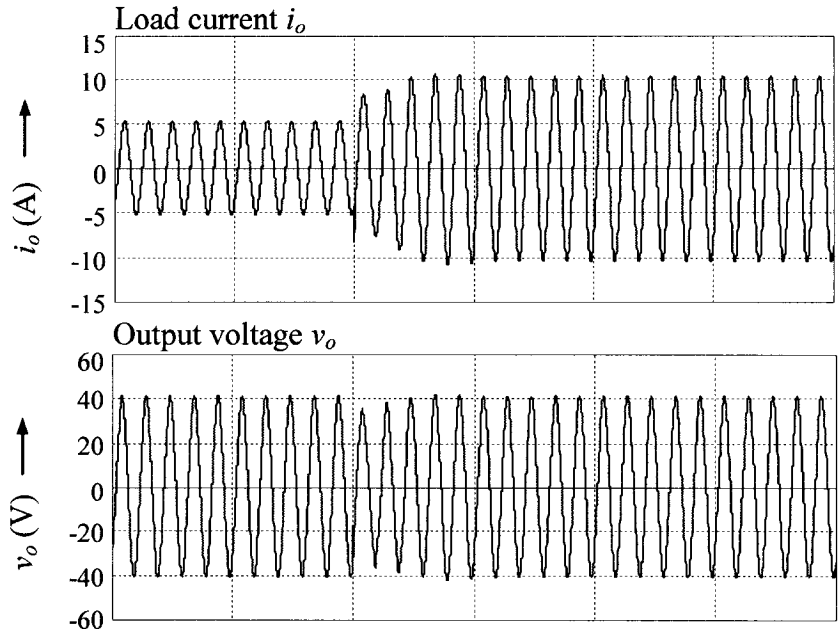


(a) Input voltage has step change from 60V to 75V (Horizontal time scale: 5μs/div)

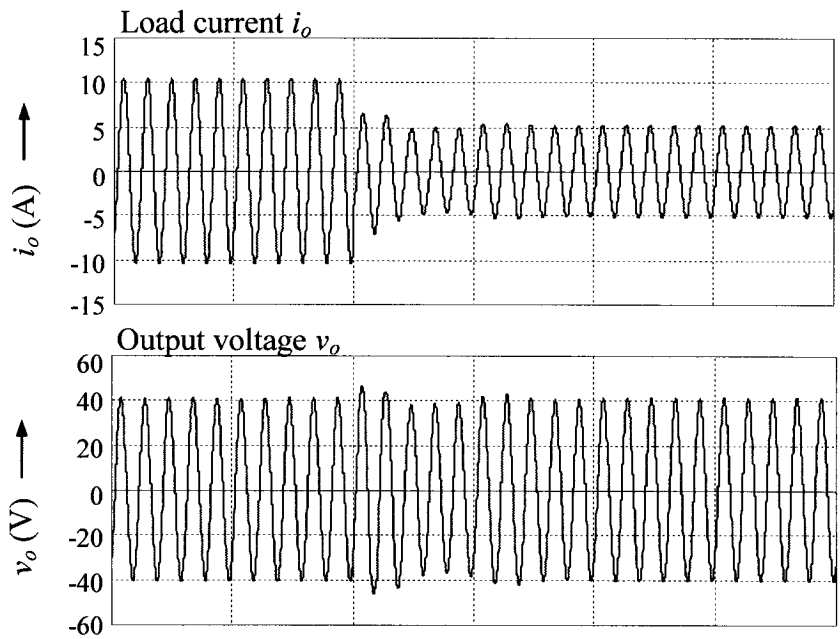


(b) Input voltage has step change from 75V to 65V (Horizontal time scale: 5μs/div)

Fig. 2- 34: Transient response of the APWM inverter against the line variation



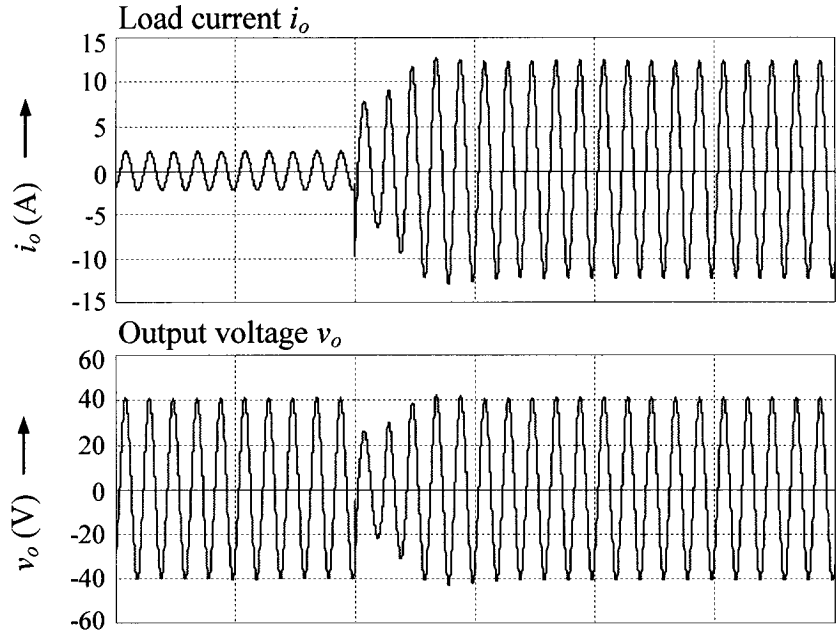
(a) Output load changes from 50% load to full load (Horizontal time scale: 5μs/div)



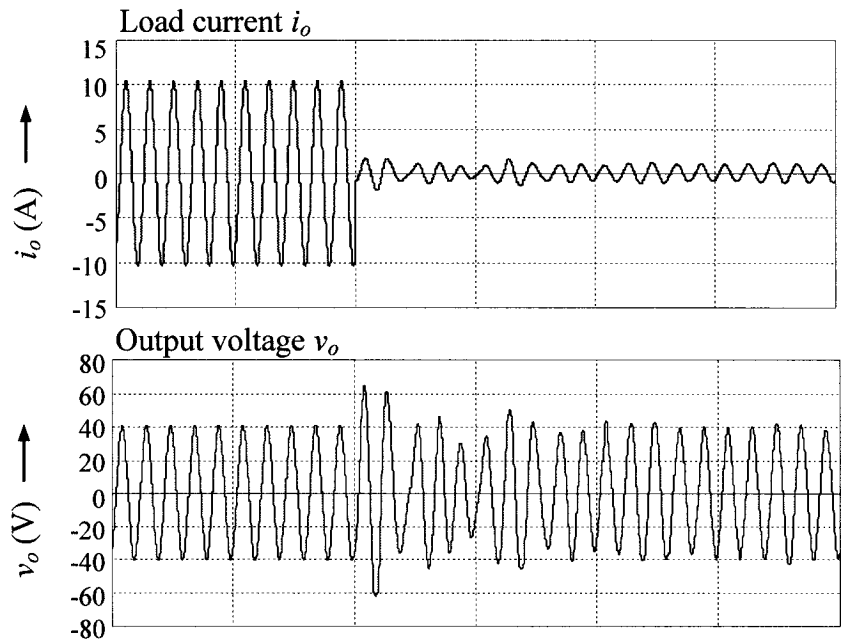
(b) Output load changes from full load to 50% load (Horizontal time scale: 5μs/div)

Fig. 2- 35: Transient response of the APWM inverter against the load variation

(to be continued)



(c) Output load changes from 10% load to full load (Horizontal time scale: 5μs/div)



(d) Output load changes from full load to 10% load (Horizontal time scale: 5μs/div)

Fig. 2- 35: Transient response of the APWM inverter against the load variation

(continued)

2.6 PERFORMANCE OF THE APWM RESONANT INVERTER – SIMULATION AND EXPERIMENTAL VERIFICATION

In this section, simulation and experimental results are presented to verify the theoretical steady-state and dynamic analyses performed in this chapter.

Fig. 2- 36 shows the prototype APWM resonant inverter. It is built to operate at 1 MHz under an input voltage range of 60 to 75 Vdc, and the output voltage is 28 Vrms sinusoidal waveform with a rated load of 200 W. The principle parameters of the simulation circuit and the experimental setup are shown in Table 2-1 and Table 2-2 respectively.

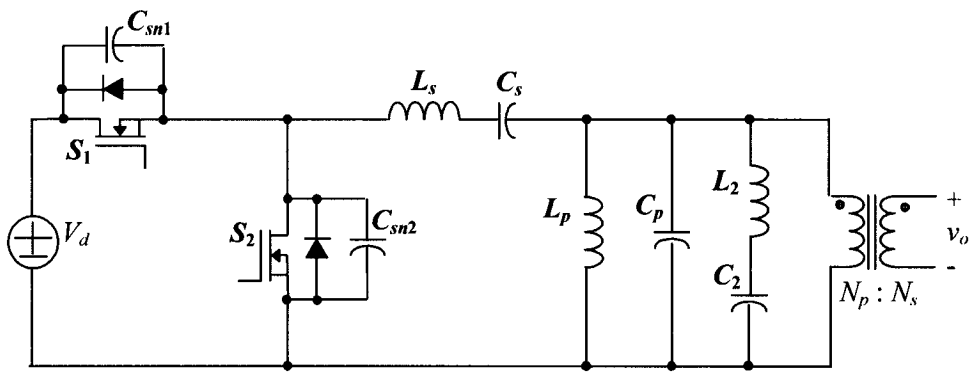


Fig. 2- 36: The prototype inverter of the proposed APWM resonant inverter

Table 2-1: Principle parameters of the simulation circuit

Resonant Components	L_s = 1.2 μH, C_s = 21 nF, L_p = 0.29 μH, C_p = 66.2 nF, L_2 = 1.2 μH, C_2 = 5.3 nF
Transformer	$N_p : N_s$ = 0.9, L_{leak}=0.01 μH, R_{loss}=2 mΩ
Switches	S_1 & S_2: IRF540

Table 2-2: Principle parameters of the experimental setup

Components	Values	Selections
L_s	1 μH	*Magnetics 55381-A2*
C_s	26.8 nF	*Wima FKP*
L_p	0.25 μH	*Magnetics 55381-A2*
C_p	76.7 nF	*Wima FKP*
L_2	1 μH	*Magnetics 55381-A2*
C_2	6.3 nF	*Wima FKP*
C_{sn1} & C_{sn2}	720 pF & 130 pF	*TDK X7R*
Transformer	$N_p : N_s$ =19:22, L_m=0.01μH	*TDK PC44LP22/13*
S_1 & S_2	IRF540	Appendix E

2.6.1 Simulation Results

The simulation is carried out by using the simulation tool PSpice. The PSpice model of the proposed APWM resonant inverter is shown in Appendix D.

2.6.1.1 Steady-state waveforms

Previously, the simulation results of the inverter steady-state waveforms have been presented in Fig. 2- 11 in section 2.2.5 for the verification of the waveforms (Fig. 2- 10) derived from the theoretical analyses. Fig. 2- 10 and Fig. 2- 11 show a good agreement between the theoretical predictions and the simulation results.

The harmonic spectrum of the inverter output voltage is shown in Fig. 2- 37. It shows that, at rated load, the proposed inverter generates near sinusoidal voltage waveform at the output, which has about 1.6% and 1.3% THD when the minimum (60V)

and maximum (75V) input voltage is applied respectively. This fact is expected because the 3rd harmonic component reaches its maximum value when the minimum input voltage is applied according to the harmonic profile shown in Fig. 2- 9. This simulation result also has a good agreement to the theoretical THD presented in Fig. 2- 13.

Fig. 2- 38 shows the harmonic spectrum of the inverter input current. Comparing this figure with the theoretical harmonic profile presented in Fig. 2- 22, the first ac component has very good agreement (5.72 A when V_d = 60 V in both figures), while the higher harmonics have some differences. This is because only the fundamental resonant current is considered to derive the input current harmonics in Fig. 2- 22.

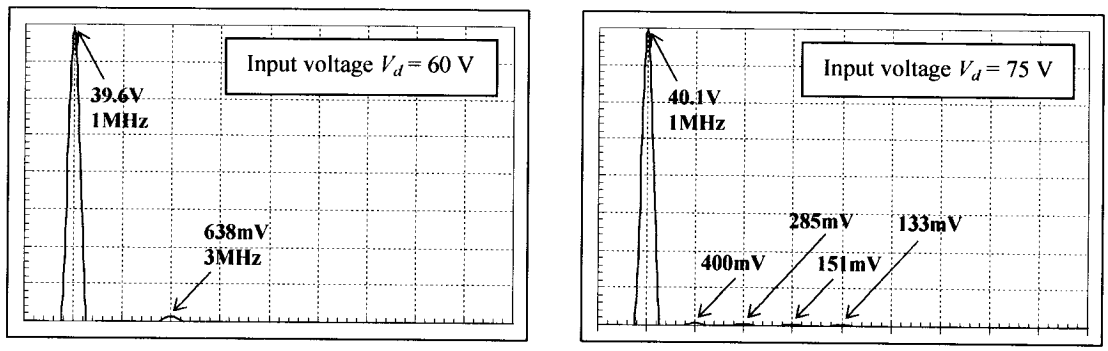


Fig. 2- 37: Harmonic spectrum of the inverter output voltage
(Horizontal scale: Frequency – 1 MHz/div; Vertical scale: Voltage - 10 V/div)

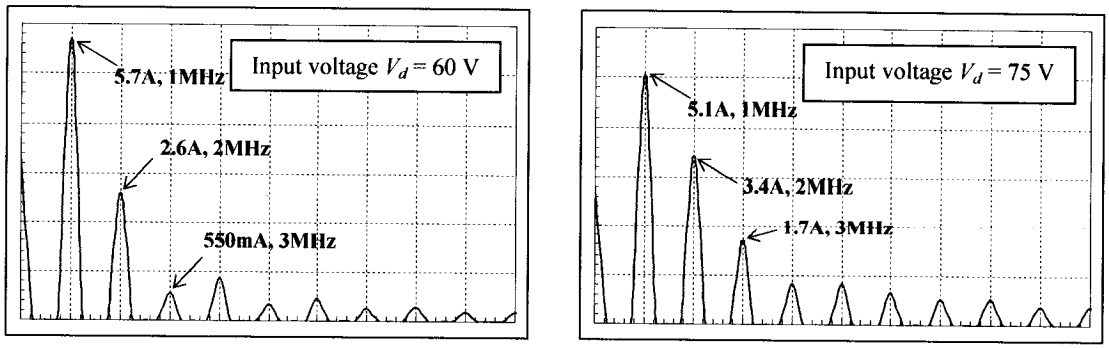
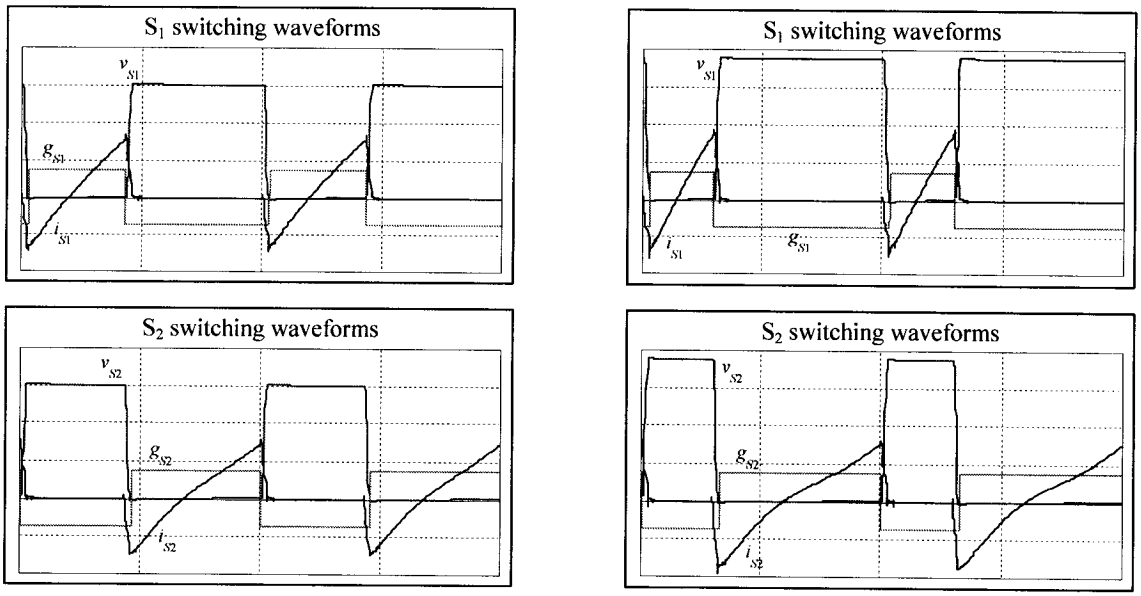


Fig. 2- 38: Harmonic spectrum of the inverter input current
(Horizontal scale: Frequency – 1 MHz/div; Vertical scale: current - 1 A/div)

2.6.1.2 *Zero-voltage-switching operation*

Operating waveforms of Fig. 2- 4 shows ZVS operation under the nominal operating condition (V_d= 60V and 100% load). Simulation results of Fig. 2- 39 show that ZVS operation is still maintained at light load for the whole input voltage range.



(a) Input voltage = 60V (b) Input voltage = 75V

Fig. 2- 39: ZVS operation of the proposed inverter at 10% load
(Horizontal scale: Time - 0.5μs/div; Vertical scale: Voltage - 20V/div, Current - 4A/div)

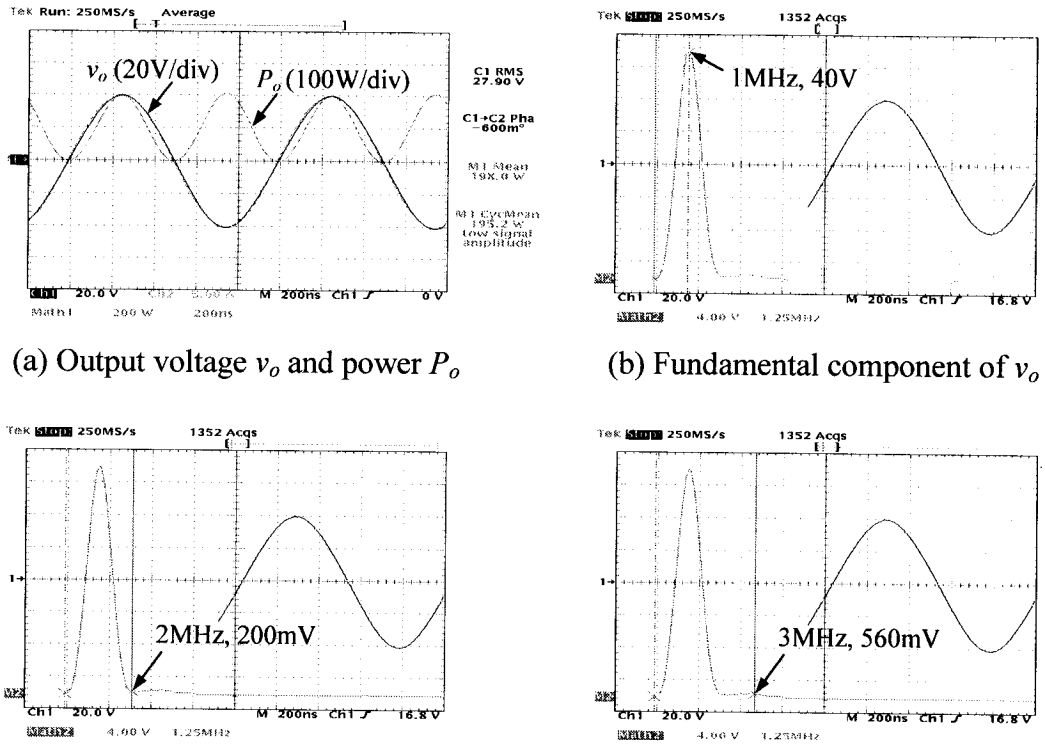
2.6.1.3 *Large transient response*

Due to the limitation of the available test facility (for example, no dc source is available to make step change in the input voltage), simulation is used to investigate the inverter dynamic performance under large transients in both input voltage and load current. Fig. 2- 34 and Fig. 2- 35 presented in section 2.5.5 show that the APWM resonant inverter with the proposed control scheme is stable and has fast response under the large signal transients in both input voltage and load current.

2.6.2 Experimental Results

2.6.2.1 Steady-state waveforms

The output voltage of the APWM resonant inverter and its harmonic components are presented in Fig. 2- 40. When V_d = 60 V and P_o = 200 W, the total harmonic distortion of output voltage is about 1.6%.



(a) Output voltage v_o and power P_o

(b) Fundamental component of v_o

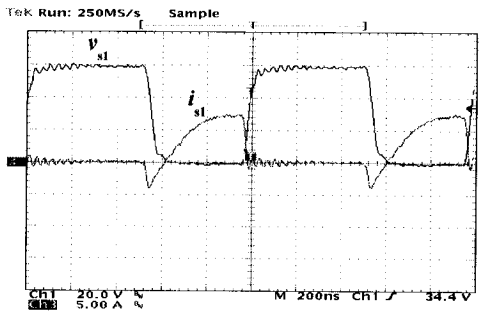
(c) 2nd harmonic component of v_o

(d) 3rd harmonic component of v_o

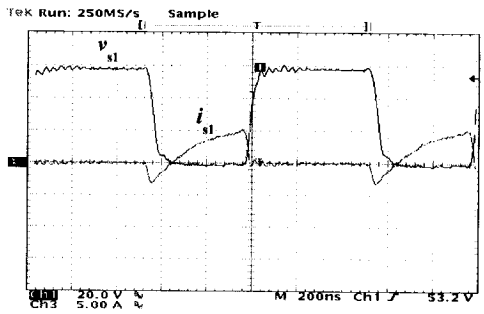
Fig. 2- 40: Experimental waveforms of the inverter output voltage

2.6.2.2 Zero-voltage-switching operation

Fig. 2- 41 (a) and (b) show the voltage and current of switch S_1 operating at 60% and 30% of the full load respectively. Similarly Fig. 2- 42 (a) and (b) show the voltage and current of switch S_2 operating at 60% and 30% of the full load respectively. These figures clearly show the zero voltage switching at both turn-on and turn-off.

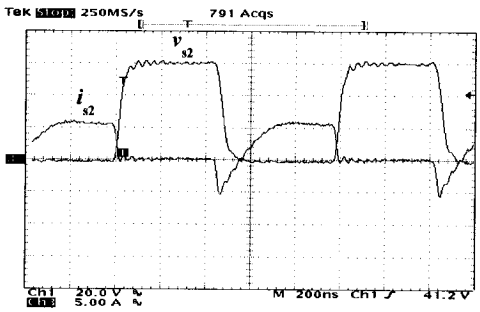


(a) Output current = 4.1A (60% load)

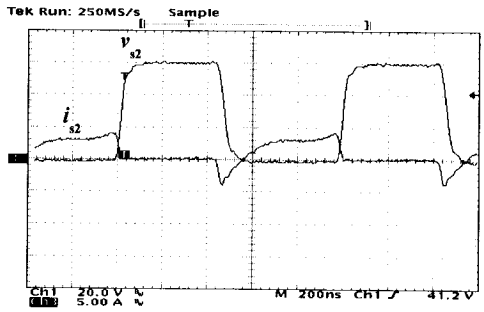


(b) Output current = 2.1A (30% load)

Fig. 2- 41: Experimental results of ZVS operation of switch S_1



(a) Output current = 4.1A (60% load)

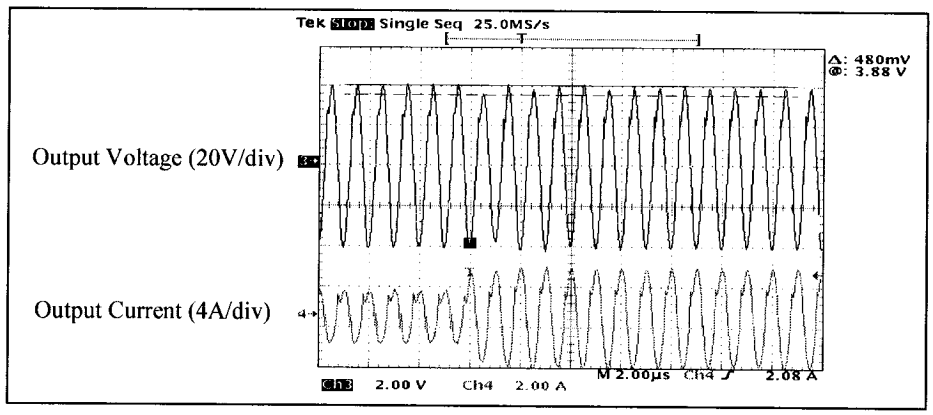


(b) Output current = 2.1A (30% load)

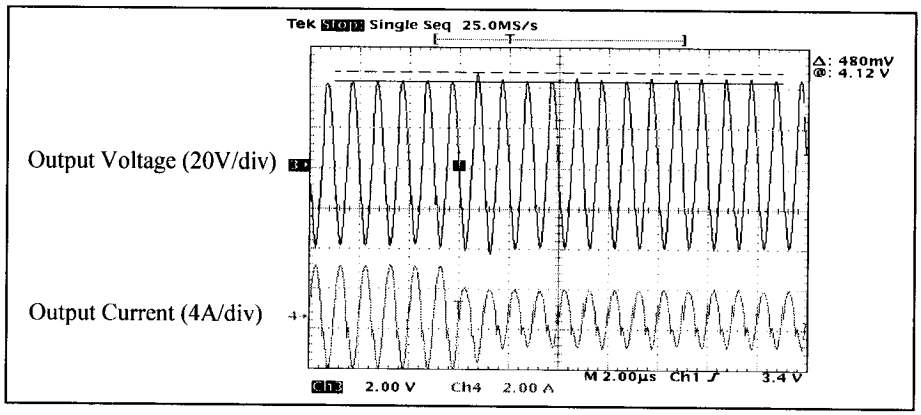
Fig. 2- 42: Experimental results of ZVS operation of switch S_2

2.6.2.3 Large transient response

Fig. 18 shows the transient response of the APWM inverter against the load variation. When the output is changed from 50% load to full load or vice versa, the output voltage can go back to steady state within 6 cycles, and its envelope has only some negligible change.



(a) Load changes from 50% load to full load



(b) Load changes from full load to 50% load

Fig. 2- 43: Transient response of the APWM inverter against the load variation

2.6.2.4 Efficiency

The overall efficiency of the proposed APWM resonant inverter as a function of the output power is shown in Fig. 2- 44. This figure shows that the efficiency is almost constant between 90% to 93% when the load decreases from 100% to about 50% of the full load. This fact can be explained as follows. Because the circuit achieves soft switching from full load to very light load, the major losses in the circuit are from (i) conduction losses in the power circuit and, (ii) losses in the control and drive circuits.

When the load decreases, the current in the power circuit decreases resulting in less conduction losses in the power circuit, and the losses in the control and drive circuit (which is almost constant) is only an ignorable part of the total losses. This yields an almost constant efficiency. However, when the load decreases further, the losses in the control and drive circuits become significant and cause the efficiency to decrease dramatically.

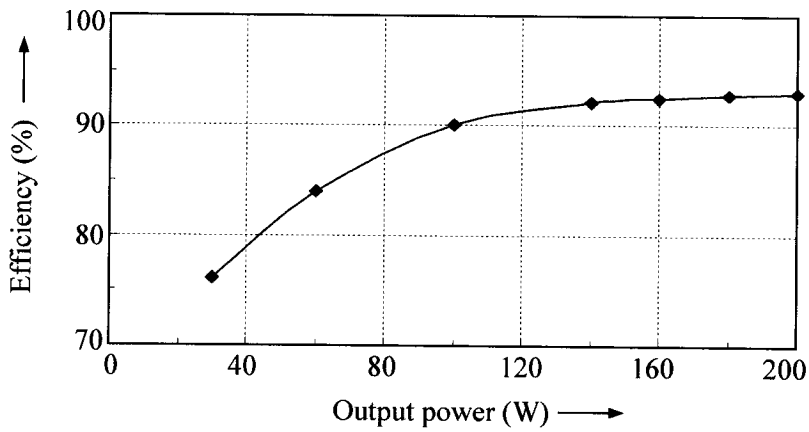


Fig. 2- 44: Efficiency of the proposed inverter vs. output power

2.7 SUMMARY

In this chapter, an asymmetrical pulse-width-modulated resonant inverter has been proposed. This topology uses a chopper, series-parallel resonant bank, a harmonic trap, and a high frequency transformer to generate a sinusoidal voltage with very low THD (<2%) at the output. A combination of feedforward and feedback control loop is employed in the inverter to achieve fast transient response against large input and load variation. The steady-state and dynamic behavior of the inverter have been analyzed and verified with simulation and experimental results.

In a summary, the proposed APWM resonant inverter is a very attractive candidate for the front-end inverter in the HFAC distributed power system applications because it has the following features:

(i) Providing sinusoidal voltage and current distribution resulting in low EMI;

(ii) Very low THD at the output under all line conditions (less than 2% at rated load);

(iii) Guaranteed ZVS operation independent of the operating conditions;

(iv) Fast transient response against large input voltage and load variation;

(v) High overall efficiency from full-load to reduced-load;

(vi) Inherent current limit due to the resonant circuit employed in the inverter.

The proposed APWM inverter will be designed as the front-end inverter employed in the HFAC distributed power system in Chapter 4, and furthermore, the system performance will be investigated in Chapter 5.

CHAPTER 3

AC VOLTAGE REGULATOR MODULE (AC VRM)

3.0 INTRODUCTION

A few topologies proposed in [58-64] could be the implementation of AC voltage regulator module (AC VRM). Most of them are resonant rectifier with phase-shift control, and they suffered from one of the following problems:

(i) It is difficult to control the output voltage for a wide range of load [60, 61];

(ii) Phase-angle-control switches operate with hard switching [60, 62-64];

(iii) Since the gating signals for the inverse-seriesed MOSFETs are complementary, the input current carried by one switch must flow through the anti-parallel diode of the complementary switch, which results in higher conduction losses [58, 59];

(iv) Gating signals are synchronized with the input resonant current which is highly distorted under light load, and additional current sensing transformer is needed [58, 59, 64];

(v) High voltage and/or current stress of the switch [58-64].

To overcome the above drawbacks, this chapter presents a series resonant converter as the AC VRM for the HFAC distributed power system applications. In this converter, to control the output voltage, an ac switch is connected in series with a resonant tank. The ac switch with its own drain-to-source capacitor is therefore used as a switch-controlled capacitor to change the resonant frequency while the operating frequency is fixed.

The ac switch of this resonant converter can be controlled by two different control techniques: phase-shift-modulation and pulse-width-modulation (PWM). Operating principles, steady-state analysis and performance curves of the proposed AC VRM using these two control techniques are presented in this chapter. Comparing these two control techniques, it is found that most advantages of the proposed converter topology can be achieved by either PWM control or phase-shift control. However, the proposed converter with PWM control is expected to have less voltage stress and higher overall efficiency under certain load conditions. Therefore, the PWM control is chosen as the optimal control technique for the proposed AC VRM, and its dynamic performance is studied in this chapter.

The contents of this chapter can be outlined as follows:

In section 3.1, the pulse-width-modulated AC VRM is presented including the circuit description, operating principle, steady-state analysis and the performance curves.

In section 3.2, the phase-shift-modulated AC VRM is presented including the circuit description, operating principle, steady-state analysis and the performance curves.

In section 3.3, the converter steady-state performance is compared between the pulse-width-modulated AC VRM and the phase-shift-modulated AC VRM.

In section 3.4, the dynamic analysis of the pulse-width-modulated AC VRM is presented.

Finally in section 3.5, the performance of the proposed AC VRM is verified by the simulation and experimental results.

3.1 PULSE-WIDTH-MODULATED AC VRM

In this section, a pulse-width-modulated AC VRM is presented. The circuit diagram and the operating principle are described in section 3.1.1 and 3.1.2 respectively. The steady-state analysis is carried out to derive the output voltage control and the time-varying expressions of the circuit variables in section 3.1.3. The performance curves showing the characteristics of the input current, and the voltage/current stress of the switches and the resonant tank components are presented in section 3.1.4.

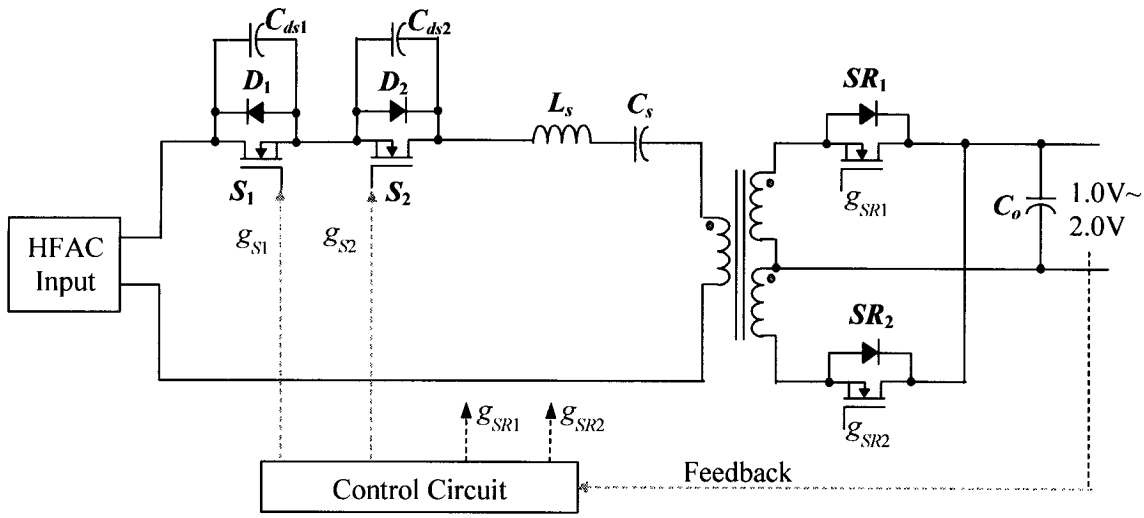
3.1.1 Circuit Description

Fig. 3- 1 shows a circuit diagram and its variable designations of the proposed high frequency pulse-width-modulated AC VRM.

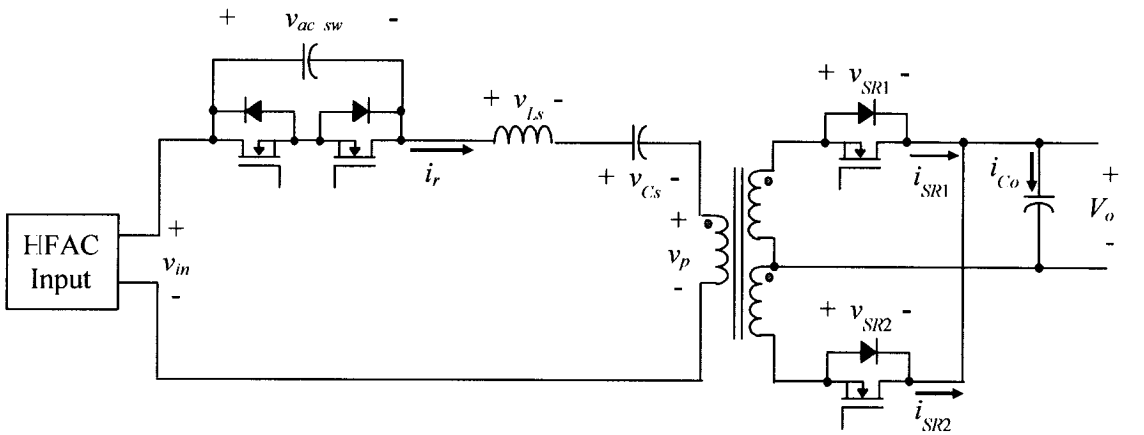
The primary side circuit consists of a series resonant tank and an ac switch composed of two inverse-seriesed MOSFETs. The ac switch with its drain-source capacitance, C_{ds}, acts as a switch-controlled capacitor. Therefore, the ac switch has the effect of switching the resonant point around so that the output voltage is controlled even though the operating frequency is fixed.

The secondary side circuit consists of a synchronous rectifier (SR) and a simple capacitor output filter.

An AC VRM topology, which has similar power circuit, was also proposed in [39]. The difference in the proposed circuit as compared to the circuit of [39] is in the PWM control technique. As it will be explained in the subsequent section, the control technique presented here maintains ZVS for both switches S_1 and S_2 under all load conditions.



(a) Circuit diagram



(b) Circuit variable designations

Fig. 3- 1: Pulse-width-modulated AC VRM

3.1.2 Principle of Operation

Fig. 3- 2 shows the key operating waveforms of the pulse-width-modulated AC VRM of Fig. 3- 1. For each switching cycle, depending on the operation of the ac switch, the converter operates in the following 6 intervals.

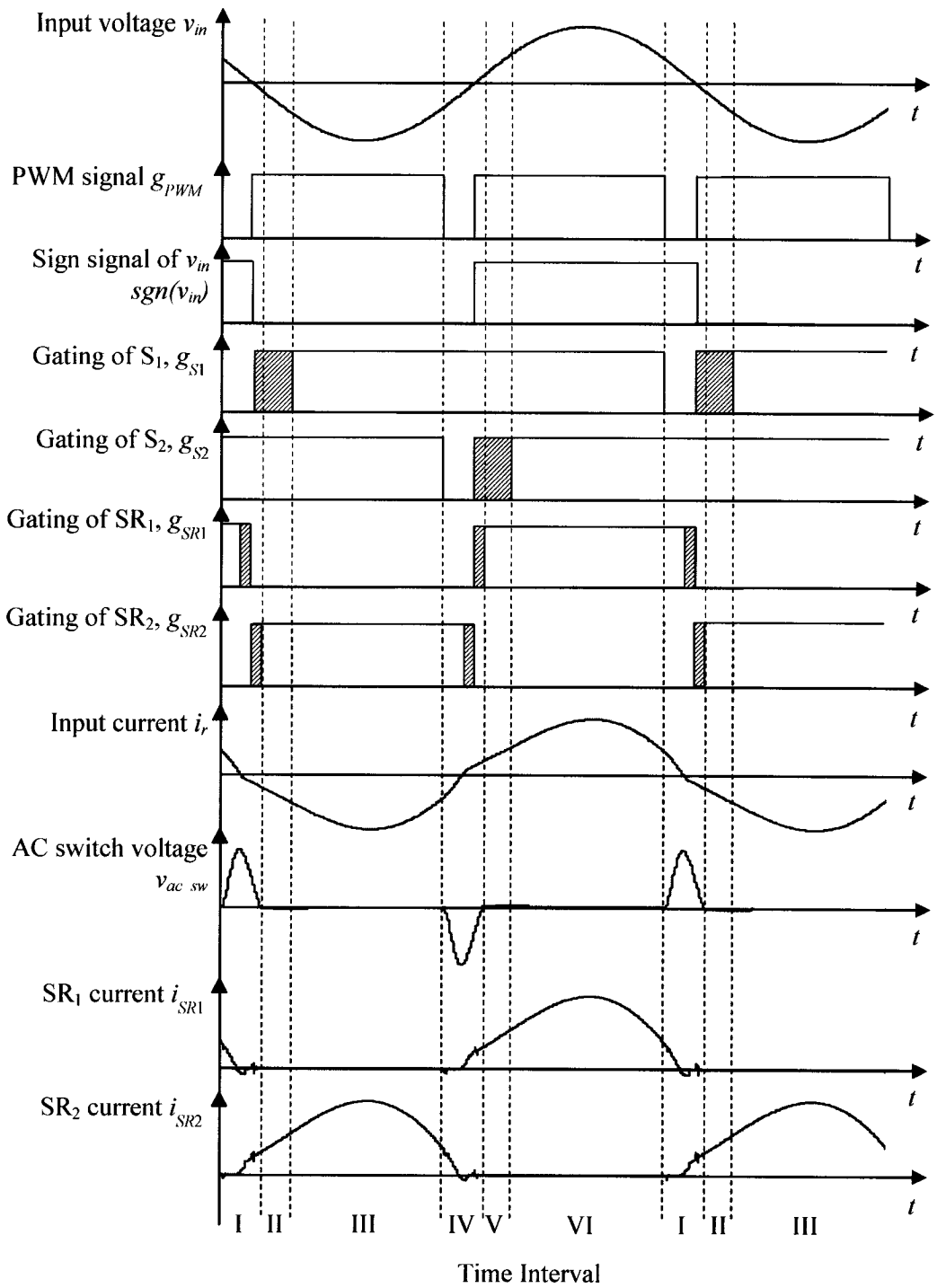


Fig. 3- 2: Operating waveforms of the pulse-width-modulated AC VRM

(Shaded area represents the delayed turn-on and advanced turn-off)

Interval I

At the beginning of this interval, switch S_1 is turned off and S_2 is kept on. The resonant current is shunted into the capacitor C_{ds1} of S_1 to charge and discharge it. Meanwhile, C_{ds1} acts as a lossless snubber to reduce the turn-off loss for switch S_1.

Interval II

At the beginning of this interval, the voltage across C_{ds1} reaches zero and will be kept zero since S_2 is still on. Now the negative resonant current is carried by D_1 and S_2.

Interval III

At the beginning of this interval, switch S_1 is turned on under zero voltage, and the negative current is now flowing through the ac switch S_1 and S_2.

Interval IV

At the beginning of this interval, switch S_2 is turned off and S_1 is kept on. The resonant current is shunted into the capacitor C_{ds2} of S_2 to charge and discharge it. Meanwhile, C_{ds} acts as a lossless snubber to reduce the turn-off loss for switch S_2.

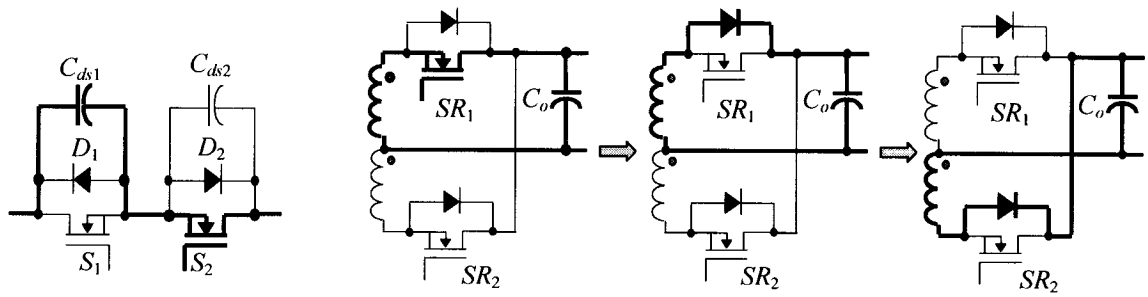
Interval V

At the beginning of this interval, the voltage across C_{ds2} reaches zero, and it will be kept zero since S_1 is still on. Now the positive resonant current is carried by D_2 and S_1.

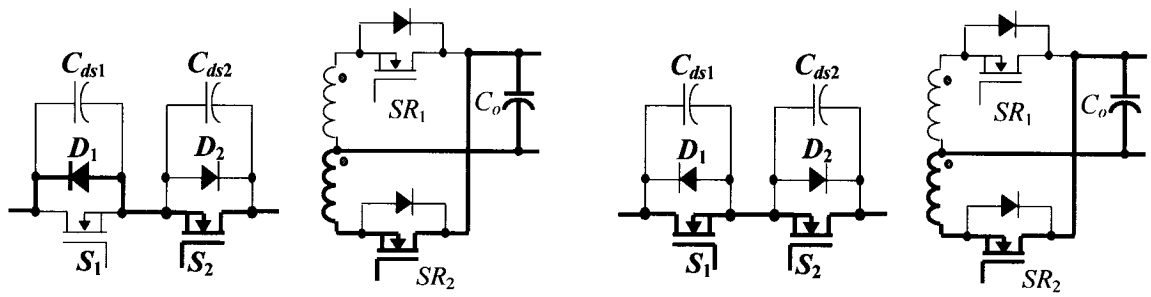
Interval VI

At the beginning of this interval, switch S_2 is turned on under zero voltage, and the positive current is now flowing through the ac switch S_1 and S_2.

The active current path of the converter in each interval is shown in Fig. 3- 3. Since the current path of the passive components is the same in each interval, only the active current path of the ac switch and SR switches are drawn in Fig. 3- 3.

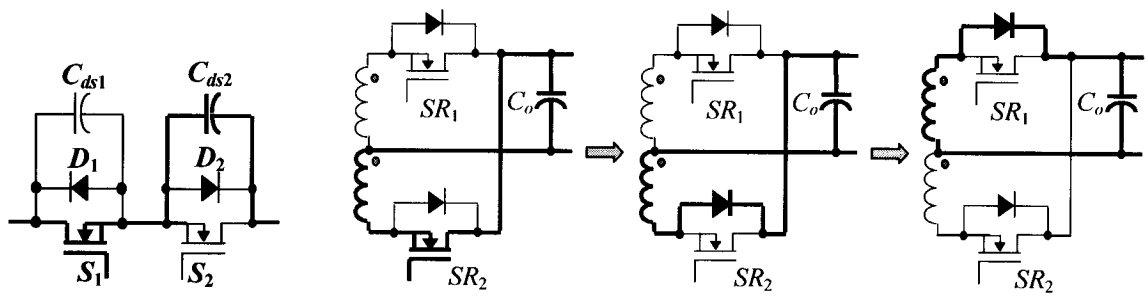


(a) Interval I

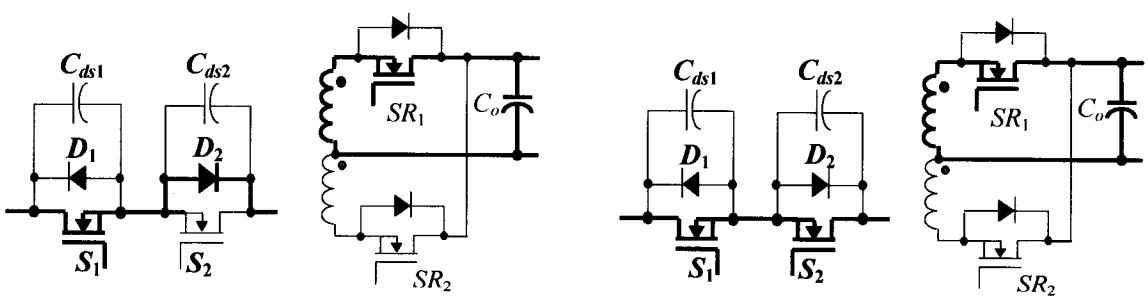


(b) Interval II

(c) Interval III



(d) Interval IV



(e) Interval V

(f) Interval VI

Fig. 3- 3: Active current path of the ac switch and SR switches of the PWM AC VRM in each operating interval

The following points can be noticed from Fig. 3- 2 and Fig. 3- 3:

(i) Turn-on ZVS of the primary side ac switch can be achieved under any load condition as long as the turn-on delay of the switch is set to be large enough. The turn-off loss of the ac switch is close to zero, since its drain-source capacitor acts as a lossless snubber.

(ii) The switching losses of SR are also zero. The body diode always conducts prior to the switch, which allows a turn-on ZVS. At the instant of turn-off, the current is transferred from the switch to its body diode till the current becomes zero. Therefore, a turn-off ZVS and smooth current transfer can also be achieved.

(iii) The resonant current is carried by both switches S_1 and S_2 in interval III and interval VI, which results in lower conduction losses compared to the case that complementary gating signals are applied (as mentioned in section 3.0). Therefore, the proposed pulse-width-modulated AC VRM is expected to have higher efficiency.

3.1.3 Steady-State Analysis of the Pulse-Width-Modulated AC VRM

In this section, the steady-state analysis is carried out on the base of some simplifying assumptions, and some considerations of non-ideal factors of the transformer and synchronous rectifier (SR). The output voltage control and the time-varying expressions of the circuit variables are derived. These equations are used in the next section (section 3.1.4) to plot some performance curves of the PWM AC VRM.

3.1.3.1 Simplifying assumptions

The steady-state analysis of the pulse-width-modulated AC VRM is carried out using the following assumptions:

(i) The input voltage of the converter is a pure sine wave;

(ii) The output capacitor is so large that the dc output voltage is constant;

(iii) The switches of the ac switch offer either zero or infinite impedance to the current flowing through them;

(iv) The inherent drain-source capacitance C_{ds} of the ac switch is considered as a constant external capacitance across the ideal switch;

(v) The on duration of the ac switch (sum of intervals II & III, and sum of intervals V & VI in each half switching cycle in Fig. 3- 2) is equal to the pulse width of the PWM signal;

(vi) The time duration of interval II and interval V is negligible;

(vii) The transformer primary winding leakage inductance is lumped with the resonant inductance;

(viii) The dead time between the gating signals for SR switches is negligible;

(ix) The load of the AC VRM is a resistance.

With the above assumptions, the simplified equivalent circuit of the converter in each operating interval is shown in Fig. 3- 4. In Fig. 3- 4, the inductance L_s is the sum of the resonant inductance and the transformer primary winding leakage inductance. The inductance L_{lk} represents the sum of the following inductance reflected to the primary side of the transformer: (i) Leakage inductance of the transformer secondary winding; and (ii) Parasitic interconnect inductance of the SR switches. The inductance L_m represents the magnetizing inductance of the transformer. The output rectification stage is represented by an ac equivalent resistance at the primary side of the transformer.

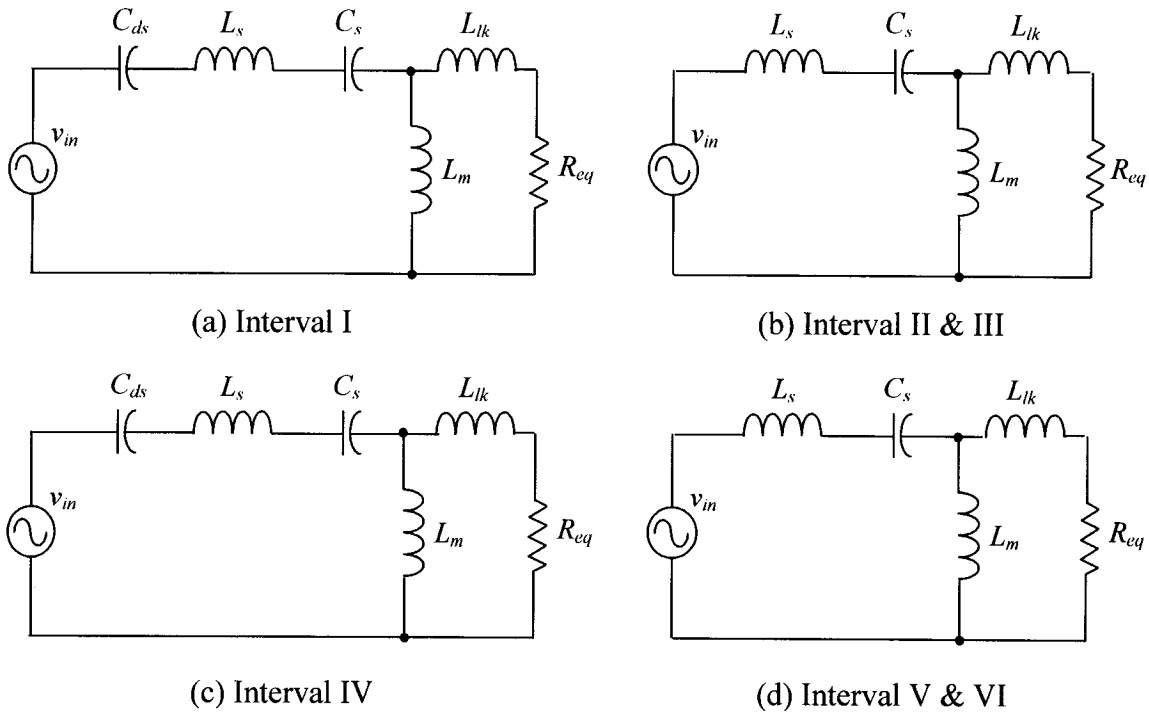


Fig. 3- 4: Simplified equivalent circuit of the PWM converter in each operating interval

3.1.3.2 Equivalent resonant frequency

As described in the operating principle, two inverse-seriesed MOSFETs act as an ac switch. When the switch is on, as shown in the equivalent circuit of Fig. 3- 4 (b) and (d), the series resonant capacitance is given by C_s. When the switch is off, as shown in the equivalent circuit of Fig. 3- 4 (a) and (c), the series resonant capacitance is given by the series connection of C_s and C_{ds}. Therefore, the ac switch can also be viewed as adjusting the average value of the series resonant capacitance over a cycle, which is named as equivalent resonant capacitance and given by:

$$C_{eq} = C_s \cdot d + \frac{C_s \cdot C_{ds}}{C_s + C_{ds}} \cdot (1-d) \qquad (3\text{- }1)$$

Where, d is the duty cycle of the PWM signal, which is defined as the high duration of the signal over half the switching period.

The equivalent resonant capacitance is, therefore, controlled by the duty cycle. Fig. 3- 5 shows the normalized equivalent capacitance as a function of duty cycle.

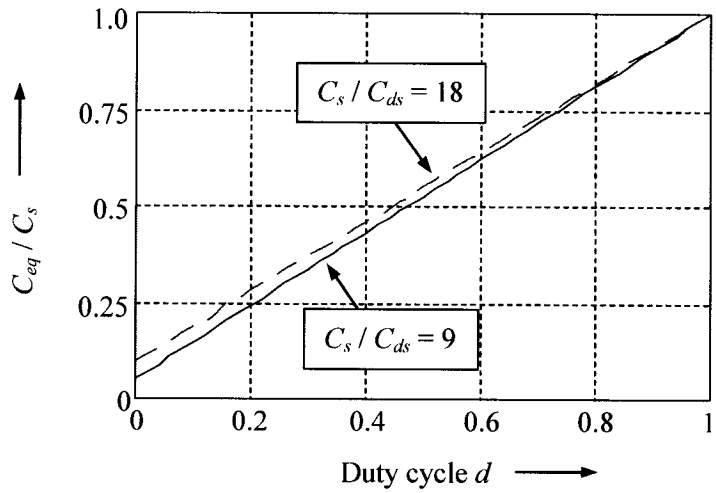


Fig. 3- 5: Normalized equivalent capacitance as a function of duty cycle

By replacing the series connection of the ac switch and the resonant capacitor with the equivalent series resonant capacitor, the equivalent circuit of the proposed converter is shown in Fig. 3- 6, and will be used to perform the steady-state analysis of the converter.

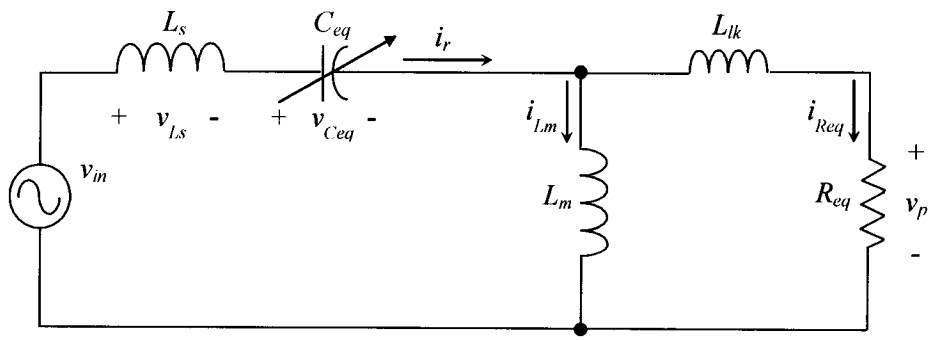


Fig. 3- 6: Equivalent circuit of the PWM AC VRM

In Fig. 3- 6, the following quantities are defined as:

AC-bus voltage:

$$v_{in} = \hat{V}_{in} \cdot \sin(\omega_o t) \tag{3- 2}$$

Equivalent load resistance:

$$R_{eq} = 8N^2 R_{load} / \pi^2 \tag{3- 3}$$

Where, N is the turns ratio of the transformer, and R_{load} is the load resistance.

Other quantities used in the steady-state analysis are defined as:

Equivalent quality factor:

$$Q_{eq} = \omega_o L_s / R_{eq} \tag{3- 4}$$

Magnetizing-inductance factor:

$$k_{Lm} = L_s / L_m \tag{3- 5}$$

The normalized equivalent resonant frequency:

$$\omega = \frac{\omega_{eq}}{\omega_o} = \frac{1}{\omega_o \sqrt{L_s C_{eq}}} \tag{3- 6}$$

As shown in Fig. 3- 7, changing duty cycle has the effect of changing the normalized equivalent resonant frequency, and therefore, the output voltage regulation can be achieved. The transfer function of the output voltage is derived as a function of duty cycle after considering some non-ideal factors of the transformer and the synchronous rectifier.

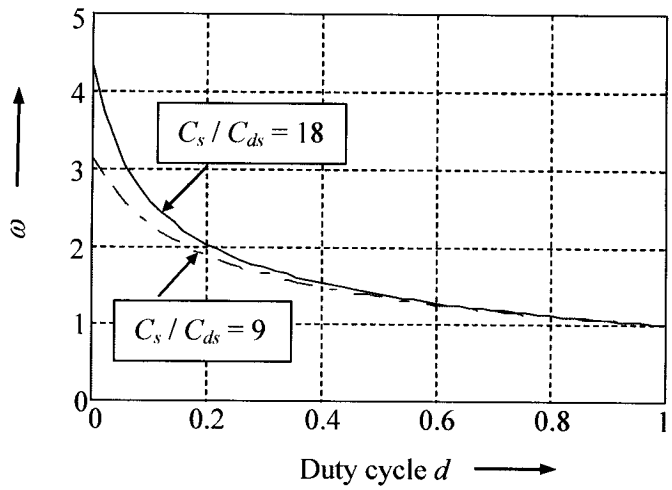


Fig. 3- 7: The Normalized equivalent resonant frequency as a function of duty cycle

3.1.3.3 Consideration of the non-ideal factors of the transformer and synchronous rectifier

When an ideal transformer and an ideal SR are considered, the voltage across the primary side of the transformer v_p can be represented by (3- 7) and its Fourier series (3- 8), and its waveform is shown in Fig. 3- 8(a).

$$v_p = \begin{cases} NV_o & 0 \le t \le T_s/2 \\ -NV_o & T_s/2 < t < T_s \end{cases} \tag{3- 7}$$

$$v_p = \frac{4NV_o}{\pi} \sum_{n=1}^{\infty} \frac{1}{2n-1} \sin((2n-1)\omega_o t) \tag{3- 8}$$

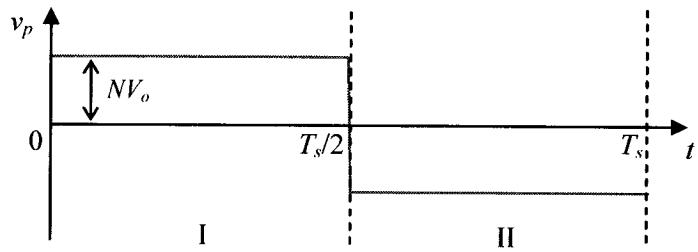
However, when the converter is operating at very high frequency, some non-ideal factors of the transformer and SR have significant effects on the converter performance characteristics. In this section and next section, as shown in Fig. 3- 4, the following four main non-ideal factors are considered:

(i) Leakage inductance of the transformer primary winding lumped with the resonant inductance represented by L_s in Fig. 3- 4;

(ii) Leakage inductance of the transformer secondary winding and Parasitic interconnect inductance of SR switches together represented by L_{lk} in Fig. 3- 4;

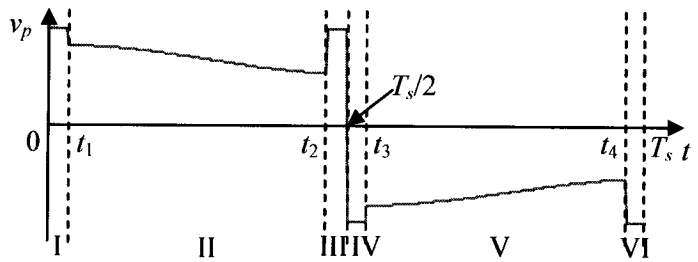
(iii) Magnetizing inductance of the transformer represented by L_m in Fig. 3- 4;

(iv) The forward voltage drop across the body diodes of SR switches.



Conducting device:
Interval I: SR_1
Interval II: SR_2

(a) Ideal transformer and SR



Conducting device:
Interval I: Diode of SR_1
Interval II: SR_1
Interval III: Diode of SR_1
Interval IV: Diode of SR_2
Interval V: SR_2
Interval VI: Diode of SR_2

(b) Non-ideal transformer and SR

Fig. 3- 8: Waveform of the voltage across the primary side of the transformer

When non-ideal factors (i), (ii) and (iv) are considered, voltage v_p can be determined by (3- 9), and its waveform is shown in Fig. 3- 8(b).

$$v_p = \begin{cases} N \cdot (V_{diode} + V_o) & 0 \le t < t_1 \\ N \cdot (L_{\sec} \cdot \dfrac{dNi_{r1}}{dt} + V_o) & t_1 \le t < t_2 \\ N \cdot (V_{diode} + V_o) & t_2 \le t < \dfrac{T_s}{2} \\ -N \cdot (V_{diode} + V_o) & \dfrac{T_s}{2} \le t < t_3 \\ N \cdot (L_{\sec} \cdot \dfrac{dNi_{r1}}{dt} - V_o) & t_3 \le t < t_4 \\ -N \cdot (V_{diode} + V_o) & t_4 \le t < T_s \end{cases} \quad (3\text{- }9)$$

Where V_{diode} is the voltage drop across SR switch when its body diode is conducting. L_{sec} is the sum of leakage inductance of the secondary side of the transformer and the parasitic interconnect inductance of SR. i_{r1} is the fundamental input resonant current.

Equation (3- 9) can be represented by its Fourier series (3- 10). Detailed derivation of (3- 9) and (3- 10) is presented in Appendix C.

$$v_p = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left[a_n \cos(n\omega_o t) + b_n \sin(n\omega_o t)\right] \tag{3- 10}$$

Where

$$b_n = \frac{2}{\pi}\frac{N}{n}(V_o + V_{diode})(1-\cos(n\pi)) + \frac{2}{\pi}\frac{N}{n}V_{diode}(\cos(n\alpha)-\cos(n\beta)) \tag{3- 11}$$

$$(\alpha = 2\pi f t_1,\ \beta = 2\pi f t_2,\ n = 1,2,3\ldots)$$

$$a_1 = A\cdot k\cdot(E_1 + F_1) \tag{3- 12}$$

and

$$a_n = A\cdot k\cdot(E_n + F_n) \qquad n = 0, 2, 3, 4, 5, \ldots \tag{3- 13}$$

Where

$$A = \frac{-\hat{V}_{in}\omega^2 C_{eq}}{\omega_o^4 L_s^2 C_{eq}^2 + \omega_o^2 R_{eq}^2 C_{eq}^2 - 2\omega_o^2 L_s C_{eq} + 1} \tag{3- 14}$$

$$k = \frac{2}{\pi}N^2 L_{\sec} \tag{3- 15}$$

$$E_1 = -\frac{1}{4}B(2\alpha - 2\beta + \sin(2\alpha) - \sin(2\beta)) \tag{3- 16}$$

$$F_1 = \frac{1}{4}C(\cos(2\alpha) - \cos(2\beta)) \tag{3- 17}$$

$$E_n = \frac{B}{2}\left[\frac{1}{n+1}(-\sin(n\alpha+\alpha) + \sin(n\beta+\beta)) + \frac{1}{n-1}(-\sin(n\alpha-\alpha) + \sin(n\beta-\beta))\right] \tag{3- 18}$$

$$F_n = \frac{C}{2}\left[\frac{1}{n+1}(\cos(n\alpha+\alpha)-\cos(n\beta+\beta))+\frac{1}{n-1}(-\cos(n\alpha-\alpha)+\cos(n\beta-\beta))\right] \quad (3\text{-}19)$$

$$B = -\omega_o C_{eq} R_{eq} \quad (3\text{-}20)$$

$$C = 1-\omega_o^2 L_s C_{eq} \quad (3\text{-}21)$$

3.1.3.4 Output voltage control

The voltage transfer function of the equivalent circuit of Fig. 3- 6 is defined as:

$$M = \frac{NV_o}{\hat{V}_{in}} = \frac{\pi}{4}\cdot\frac{\hat{V}_{p1}}{\hat{V}_{in}} \quad (3\text{-}22)$$

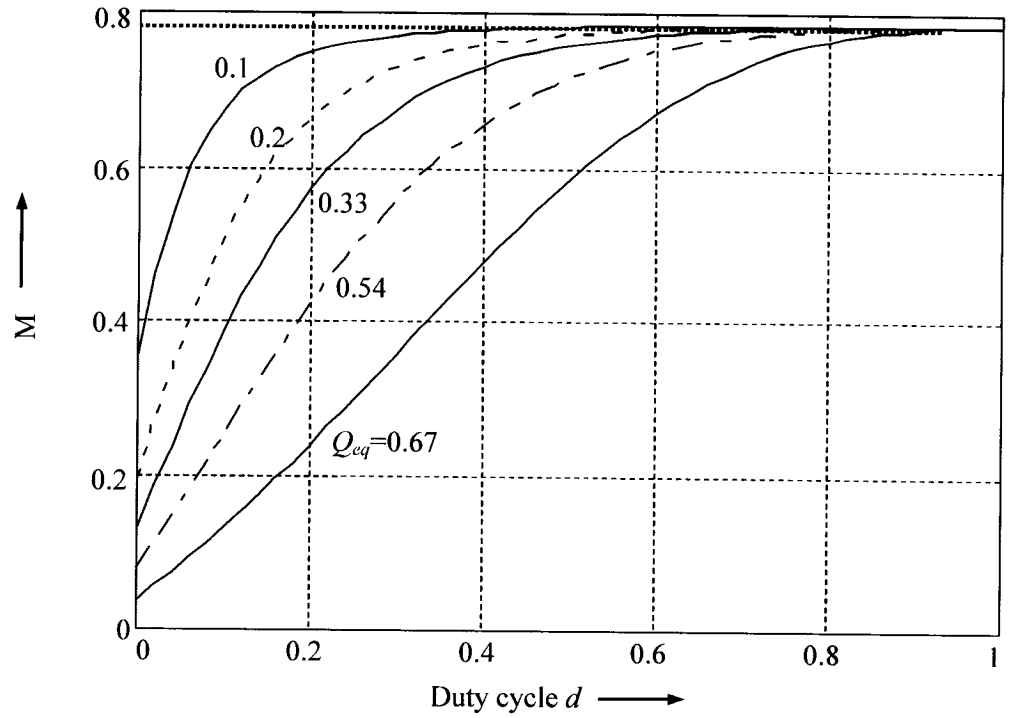
Where V_o is the dc output voltage of the AC VRM; $\hat{V}_{p1}$ is the peak value of the fundamental voltage across the transformer primary side.

According to Fig. 3- 6, the voltage transfer function can be derived as (assume that $R_{eq}>>\omega L_{lk}$, which is normally the case):

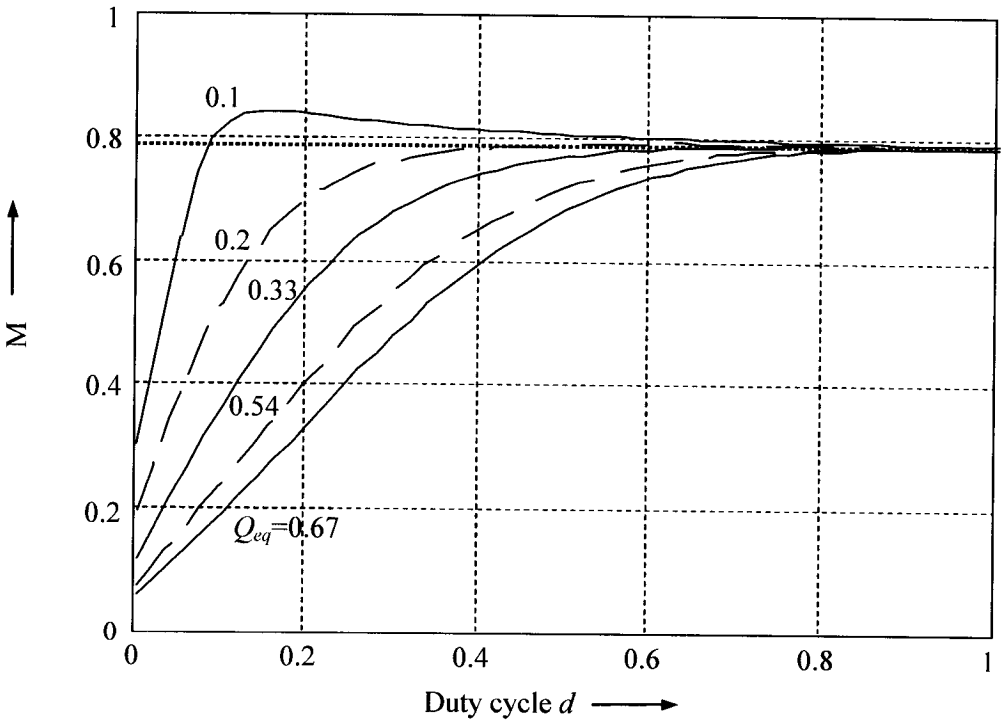
$$M = \frac{\pi}{4}\cdot\frac{1}{\sqrt{(1+k_{Lm}(1-\omega^2))^2+Q_{eq}^2(1-\omega^2)^2}} \quad (3\text{-}23)$$

For an ideal transformer, k_{Lm} = 0, the voltage transfer function versus the duty cycle variation is shown in Fig. 3- 9(a). The horizontal dotted line in Fig. 3- 9(a) shows the maximum gain of π/4 that the output voltage can achieve by changing the duty cycle.

Taking into account the magnetizing inductance of the transformer, for a value of k_{Lm} = 0.05, the voltage transfer function versus the duty cycle variation is shown in Fig. 3- 9(b). It can be seen that with decreasing Q_{eq}, the peak value of the voltage conversion ratio increases. To achieve the same voltage regulation, the required variation of duty cycle is wider, as compared with Fig. 3- 9(a).



(a) proposed converter with ideal transformer



(b) Proposed converter with non-ideal transformer

Fig. 3- 9: Output voltage control of the PWM AC VRM

3.1.3.5 Circuit voltages and currents

(i) Input resonant current

The expression of the input resonant current is the sum of its fundamental component and its harmonics. The fundamental component of the input resonant current can be found by Fig. 3- 6 (assuming that $R_{eq}>>\omega L_{lk}$):

$$i_{r1} = \frac{\hat{V}_{in}}{|Z_s + Z_p|}\sin(\omega_o t - \theta) \tag{3- 24}$$

where

$$Z_s = j\omega_o L_s - j/(\omega_o C_{eq}) \tag{3- 25}$$

$$Z_p = 1/(1/R_{eq} + 1/j\omega_o L_m) \tag{3- 26}$$

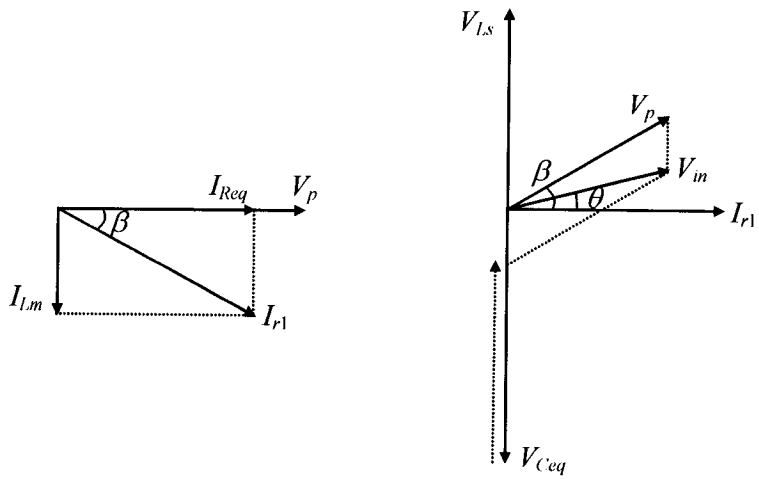


Fig. 3- 10: Phasor diagram of the equivalent circuit of Fig. 3- 6

(The magnitude of the phasors are represented by their RMS values)

The phase angle θ is derived from the phasor diagram, Fig. 3- 10, of the equivalent circuit of Fig. 3- 6. In Fig. 3- 10:

$$V_p \cos\beta = V_{in} \cos\theta \tag{3- 27}$$

Where

$$V_p = I_{r1}|Z_p| \tag{3- 28}$$

$$\cos\beta = I_{Req}/I_{r1} \tag{3- 29}$$

$$I_{Req} = \frac{V_{in}}{R_{eq}|1 + Z_s/Z_p|} \tag{3- 30}$$

Substituting (3- 28), (3- 29), and (3- 30) into (3- 27) gives:

$$\cos\theta = \frac{|Z_p|}{R_{eq}|1 + Z_s/Z_p|} \tag{3- 31}$$

The harmonic components of the input resonant current can be derived by the aid of the *n*th harmonic equivalent circuit shown in Fig. 3- 11(a), which is the sum of the fundamental equivalent circuit of Fig. Fig. 3- 11(b) and harmonic equivalent circuit of Fig. 3- 11(c).

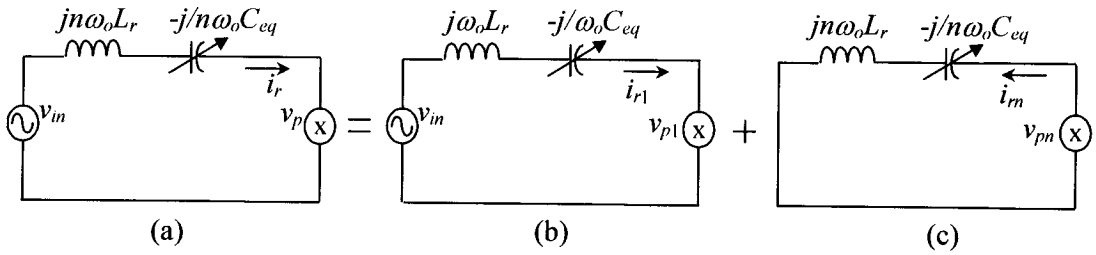


Fig. 3- 11: *n*th harmonic equivalent circuit of the proposed converter

In Fig. 3- 11(c), the harmonic components of the input resonant current are given by:

$$i_{rn} = \sum_{n=2}^{\infty} \frac{\sqrt{a_n^2 + b_n^2}}{\left| n\omega_o L_s - \frac{1}{n\omega_o C_{eq}} \right|} \sin(n\omega_o t - \gamma_n - \frac{\pi}{2}) \tag{3- 32}$$

Where a_n and b_n are given by (3- 13) and (3- 11) respectively, and γ_n is given by:

$$\tan\gamma_n = -a_n/b_n \qquad \text{n} = 2, 3, 4, \ldots \tag{3- 33}$$

Therefore, the expression of the input resonant current is given by (3- 34) according to Fig. 3- 11:

$$i_r = i_{r1} - i_{rn} \tag{3- 34}$$

(ii) Voltage and current of the resonant tank

The current flowing through the resonant tank is the input resonant current. The voltage across the resonant inductor is given by:

$$v_{Ls} = \frac{\hat{V}_{in}\omega_o L_s}{|Z_s + Z_p|}\cos(\omega_o t - \theta) - \sum_{n=2}^{\infty}\frac{n\omega_o L_s\sqrt{a_n^2 + b_n^2}}{\left|n\omega_o L_s - \dfrac{1}{n\omega_o C_{eq}}\right|}\cos(n\omega_o t - \gamma_n - \frac{\pi}{2}) \tag{3- 35}$$

The voltage across the resonant capacitor is given by:

$$v_{Cs} = \frac{-\hat{V}_{in}\cos(\omega_o t - \theta)}{\omega_o C_s|Z_s + Z_p|} + \sum_{n=2}^{\infty}\frac{\sqrt{a_n^2 + b_n^2}\cos(n\omega_o t - \gamma_n - \dfrac{\pi}{2})}{n\omega_o C_s\left|n\omega_o L_s - \dfrac{1}{n\omega_o C_{eq}}\right|} \tag{3- 36}$$

(i) Voltage and current of the ac switch

According to the operating waveforms shown in Fig. 3- 2, the current flowing through each switch of the ac switch is equal to the resonant current given by (3-34).

The voltage across each switch of the ac switch is equal to zero when it is on, and is given by (3- 37) when it is off.

$$v_{sw} = \frac{-\hat{V}_{in}\cos(\omega_o t - \theta)}{\omega_o C_{ds}|Z_s + Z_p|} + \sum_{n=2}^{\infty}\frac{\sqrt{a_n^2 + b_n^2}\cos(n\omega_o t - \gamma_n - \dfrac{\pi}{2})}{n\omega_o C_{ds}\left|n\omega_o L_s - \dfrac{1}{n\omega_o C_{eq}}\right|} \tag{3- 37}$$

(ii) Voltage and current of the synchronous rectifier

The gating signals of the synchronous rectifier are synchronized with the input voltage. During the positive half cycle of the input voltage, the top switch S_{SR1} is conducting, and during the negative half cycle of the input voltage, the bottom switch S_{SR2} is conducting. The voltage and the current of each switch are given by:

$$v_{SR1} = \begin{cases} 0 & \text{when} \quad kT_s \le t < (2k+1)T_s/2 \\ v_p/N - V_o & \text{when} \quad (2k+1)T_s/2 \le t < (k+1)T_s \end{cases} \tag{3- 38}$$

Where v_p is the voltage across the primary side of the transformer given by (3- 10), N is the turns ratio of the transformer, and constant $k = 0, 1, 2, 3, \ldots$

$$i_{SR1} = \begin{cases} Ni_r & \text{when} \quad kT_s \le t < (2k+1)T_s/2 \\ 0 & \text{when} \quad (2k+1)T_s/2 \le t < (k+1)T_s \end{cases} \tag{3- 39}$$

$$v_{SR2} = \begin{cases} -v_p/N - V_o & \text{when} \quad kT_s \le t < (2k+1)T_s/2 \\ 0 & \text{when} \quad (2k+1)T_s/2 \le t < (k+1)T_s \end{cases} \tag{3- 40}$$

$$i_{SR2} = \begin{cases} 0 & \text{when} \quad kT_s \le t < (2k+1)T_s/2 \\ -Ni_r & \text{when} \quad (2k+1)T_s/2 \le t < (k+1)T_s \end{cases} \tag{3- 41}$$

Where i_r is the input resonant current given by (3- 34).

If only the fundamental component of the resonant current is considered, the rectifier current, which is the sum of i_{SR1} and i_{SR2}, can be represented by its Fourier series:

$$i_{SR} = \frac{2}{\pi}\hat{I}_{SR} - \frac{4}{\pi}\hat{I}_{SR}\sum_{n=1}^{\infty}\frac{1}{4n^2-1}\cos(2n\omega_o t) \tag{3- 42}$$

Where $\hat{I}_{SR}$ is the peak value of the rectifier current:

$$\hat{I}_{SR} = \frac{N\hat{V}_{in}}{|Z_s + Z_p|} \tag{3- 43}$$

The dc component of i_{SR} flows though the output load, and the ac components of i_{SR} flows through the output capacitor.

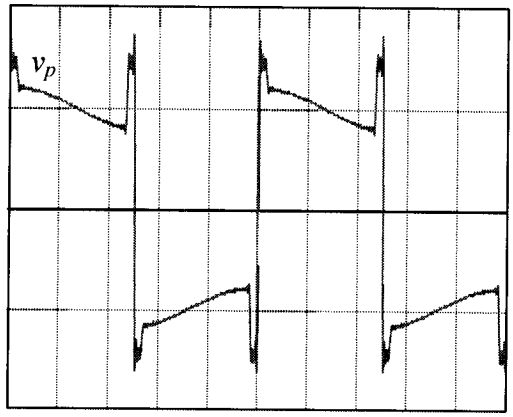
(iii) Voltage and current of the output capacitor

Since the output capacitor is assumed to be very large, the voltage across it is the constant ripple-free dc voltage V_o. For simplicity, assuming that only the fundamental component of the input resonant current is considered, the current flowing though the output capacitor is equal to the ac component of the rectifier current given by:

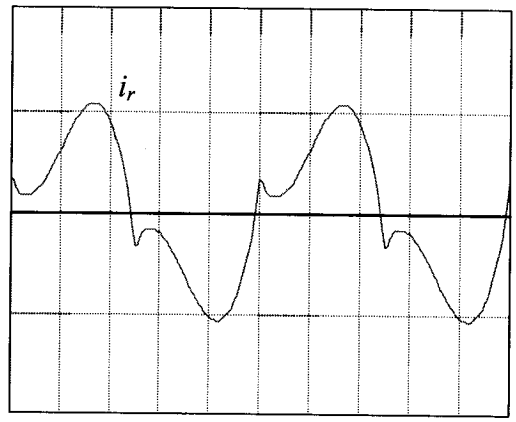
$$i_{Co} = -\frac{4}{\pi}\hat{I}_{SR}\sum_{n=1}^{\infty}\frac{1}{4n^2-1}\cos(2n\omega_o t) \qquad (3\text{-}44)$$

The waveforms of the circuit variables through two steady state cycles are shown in Fig. 3- 12. These waveforms are obtained from the above theoretical derivation for the converter with V_{in} = 28 Vrms, C_{ds}=1500 pF, L_s = 2.53 μH, C_s = 10 nF, N = 20, V_o = 1.5 V, and P_o = 15 W (50% load). Fig. 3- 12(a) is generated by using (3-10) considering the range of n from 1 to 100. Very high frequency ringings in Fig. 3- 12(a) are caused by harmonics higher than the order of 100 in (3-10).

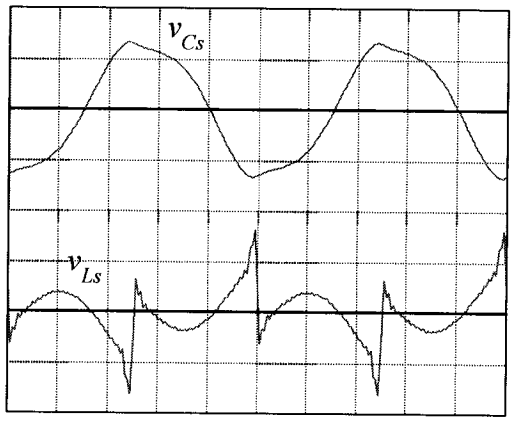
The simulation results for the same converter are shown in Fig. 3- 13 for the purpose of verification. Some high frequency ringings seen in the simulation waveforms are caused by the resonance between the transformer leakage inductance and the inherent drain-to-source capacitors of the SR switches. In a real circuit, a small snubber across the transformer primary side may be required to damp the ringings. Except this, the theoretical predictions and the simulation results have a good agreement in both shape and value. Therefore, the steady-state analysis made in this section is valid and applicable to the real circuit.



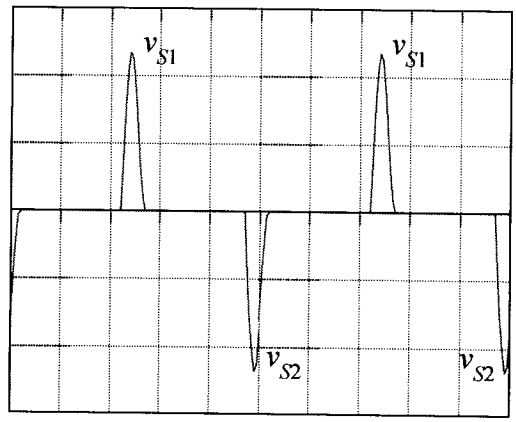
(a) Transformer primary voltage v_p(30V/div)



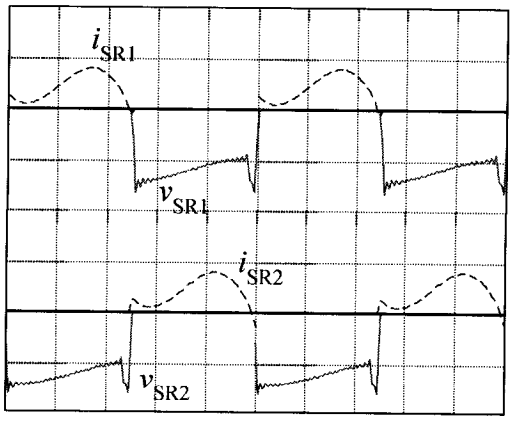
(b) Input resonant current i_r (1A/div)



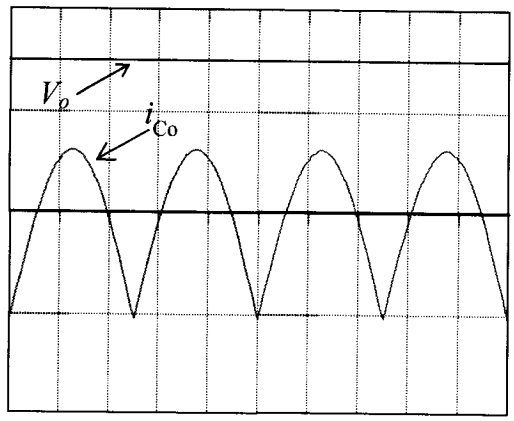
(c) Voltage of the resonant circuit v_{Cs} (10V/div) and v_{Ls} (40V/div)



(d) Voltage of the ac switch v_{S1} (5V/div) and v_{S2} (5V/div)

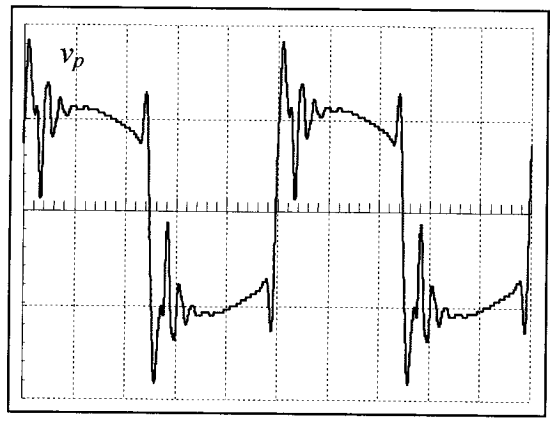


(e) Current and voltage of SR: i_{SR1} and i_{SR2} (25A/div), v_{SR1} and v_{SR2} (2.5V/div)

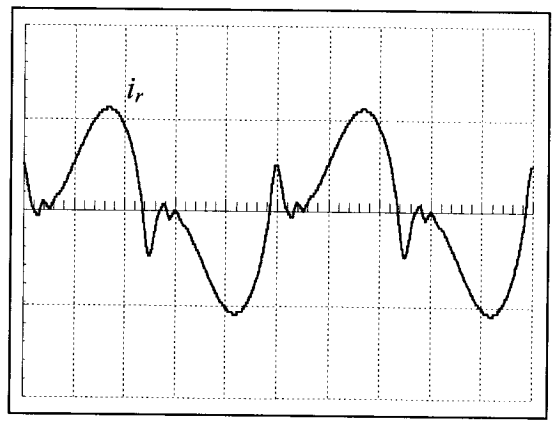


(f) Current and voltage of output capacitor i_{Co} (20A/div) and V_o (1V/div)

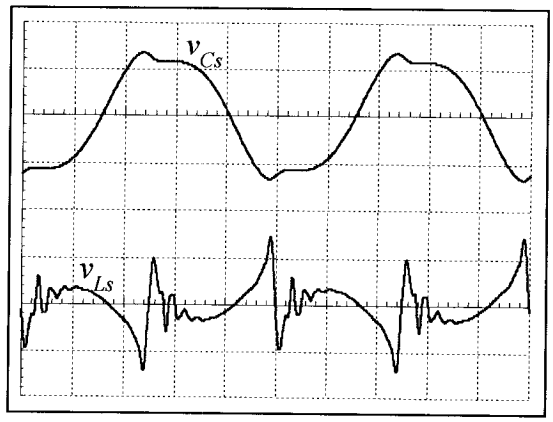
Fig. 3- 12: Theoretical waveforms of the circuit variables (Horizontal time scale: 0.2 μs/div; Vertical voltage and/or current scales are indicated in subtitle)



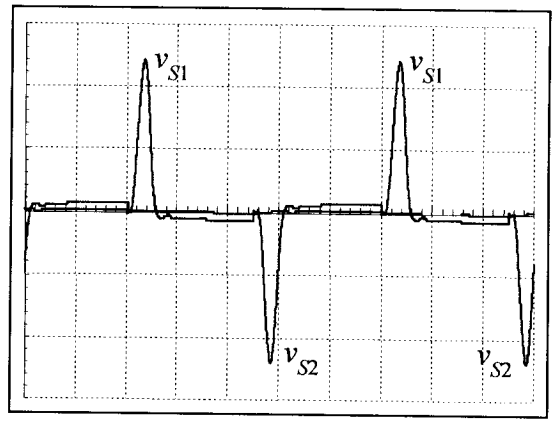
(a) Transformer primary voltage v_p(30V/div)



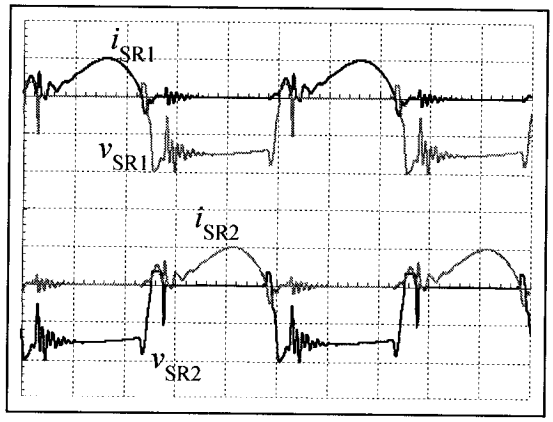
(b) Input resonant current i_r (1A/div)



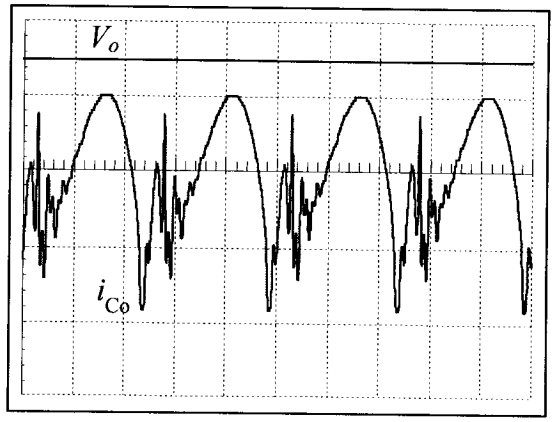
(c) Voltage of the resonant circuit v_{Cs} (10V/div) and v_{Ls} (40V/div)



(d) Voltage of the ac switch v_{S1} (5V/div) and v_{S2} (5V/div)



(e) Current and voltage of SR: i_{SR1} and i_{SR2} (25A/div), v_{SR1} and v_{SR2} (2.5V/div)



(f) Current and voltage of output capacitor i_{Co} (10A/div) and V_o (1V/div)

Fig. 3- 13: Simulation waveforms of the converter circuit variables (Horizontal time scale: 0.2 μs/div; Vertical voltage and/or current scales are indicated in subtitle)

3.1.4 Performance Curves for the Pulse-Width-Modulated AC VRM

In this section, the characteristics of the input resonant current, such as the displacement power factor, the total harmonic distortion, and the power factor are studied for the same converter example in the previous section. The RMS values of the voltages and current of the resonant tank are calculated. The voltage and current stress of all the switches employed in the circuit as ac switch and synchronous rectifier are presented. All the performance curves are presented as a function of duty cycle for different values of the quality factor, and they are used in Chapter 4 for the design purpose.

3.1.4.1 Characteristics of the input resonant current

(i) Displacement power factor

The displacement power factor (*DPF*) of the input resonant current is defined as:

$$DPF = \cos\theta \tag{3-45}$$

Where θ is the phase difference between the input voltage and current, and $\cos\theta$ is given by (3- 31).

Using (3- 4), (3- 5), and (3- 6) to simplify (3- 31), the expression of *DPF* is found to be:

$$DPF = 1/\sqrt{(1+k_{Lm}^2/Q_{eq}^2)\cdot[(1+k_{Lm}(1-\omega^2))^2+Q_{eq}^2(1-\omega^2)^2]} \tag{3-46}$$

Where Q_{eq}, k_{Lm}, and ω are defined by (3- 4), (3- 5), and (3- 6) respectively.

For different values of Q_{eq}, *DPF* of the input resonant current is plotted in Fig. 3-14 as a function of duty cycle.

(ii) Total harmonic distortion

The total harmonic distortion (*THD*) of the input resonant current is calculated by:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{rn}^2}}{I_{r1}} \tag{3- 47}$$

Where, I_{r1} is the RMS value of i_{r1} of (3- 24) and is given by (3- 48). I_{rn} is the RMS value of i_{rn} of (3- 32) and is given by (3- 49):

$$I_{r1} = \frac{V_{pk}}{\sqrt{2}\left|Z_s + Z_p\right|} \tag{3- 48}$$

Where Z_s and Z_p are given by (3- 25) and (3- 26) respectively.

$$I_{rn} = \frac{1}{\sqrt{2}} \sqrt{\frac{a_n^2 + b_n^2}{\left(\left|n\omega_o L_s - \frac{1}{n\omega_o C_{eq}}\right|\right)^2}} \tag{3- 49}$$

Where a_n and b_n are given by (3- 13) and (3- 11) respectively.

THD of the input resonant current is plotted in Fig. 3- 15 as a function of duty cycle for different values of Q_{eq}.

(iii) Power factor

From (3- 46) and (3- 47), the power factor (*PF*) of the input current can be found by (3- 50), and plotted in Fig. 3- 16 as a function of duty cycle.

$$PF = \frac{DPF}{\sqrt{1 + THD^2}} \tag{3- 50}$$

It can be seen that the input current has close-to-unit *PF* at the rated load, and above 0.9 at 50% load.

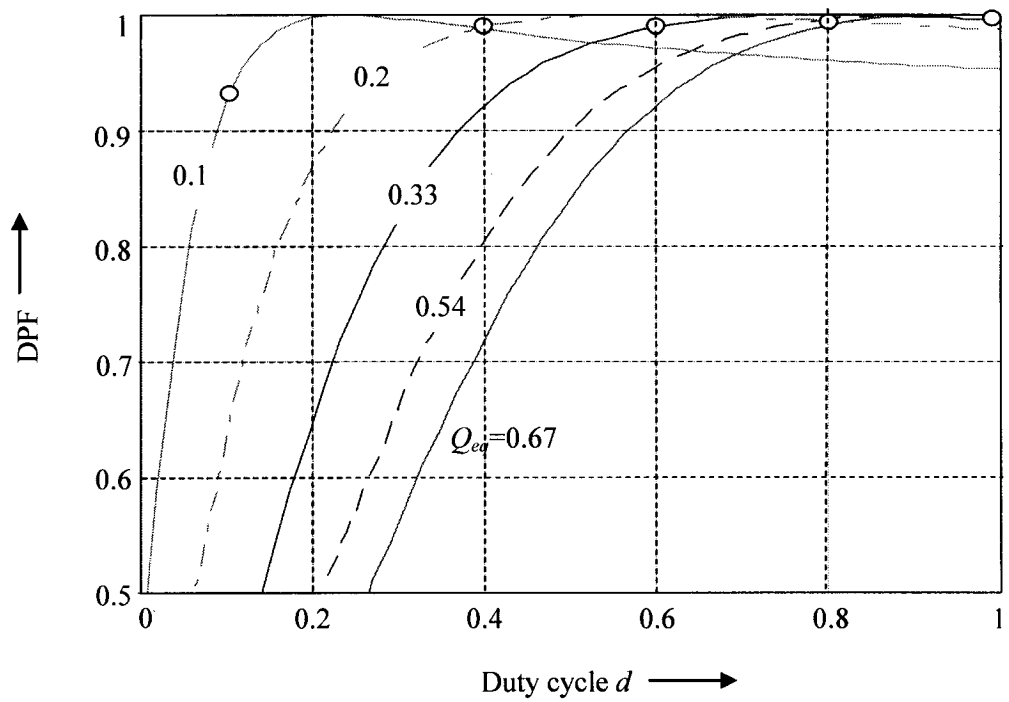


Fig. 3- 14: *DPF* of the input resonant current as a function of duty cycle

("Circle" denotes the operating point obtained from Fig. 3- 9 (b).)

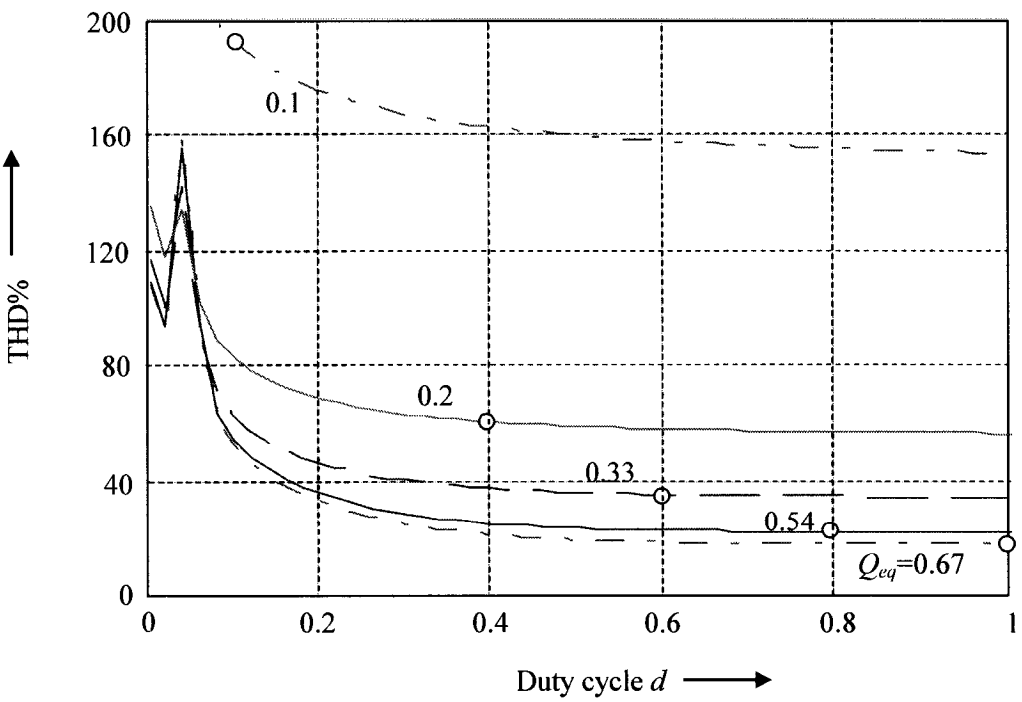


Fig. 3- 15: *THD* of the input resonant current as a function of duty cycle

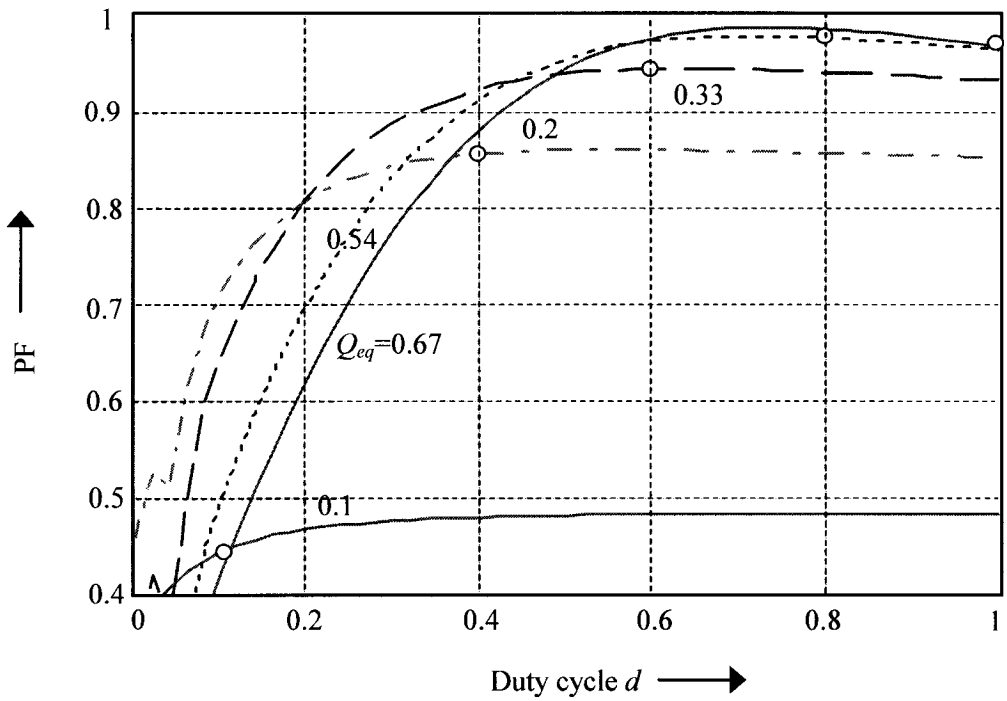


Fig. 3- 16: *PF* of the input resonant current as a function of duty cycle

It is noticed that there is resonant phenomenon in Fig. 3- 15 and Fig. 3- 16. The same phenomenon will be seen in Fig. 3- 18 to Fig. 3- 20, and Fig. 3- 22 as well. This is because that the equivalent second harmonic impedance of the series resonant branch including the ac switch has a resonant point around the operating point of d = 0.05, as shown in Fig. 3- 17.

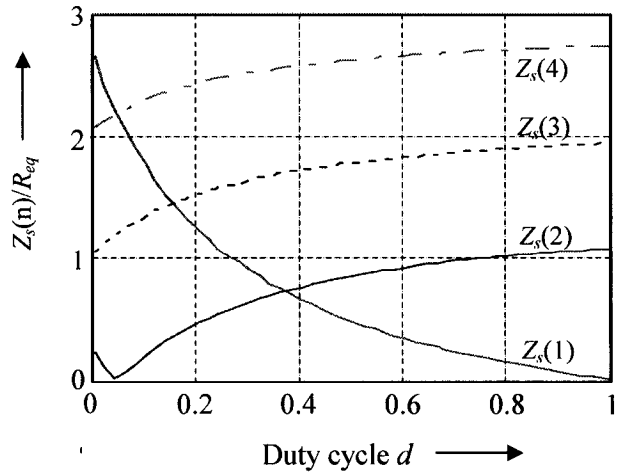


Fig. 3- 17: Equivalent impedance of the series resonant branch including ac switch

3.1.4.2 *RMS voltages and current of the resonant tank*

The RMS value of the voltage across the resonant inductor and capacitor, and the RMS value of the resonant current can be calculated by (3- 51), (3- 52) and (3- 53) respectively and plotted in Fig. 3- 18, Fig. 3- 19 and Fig. 3- 20 respectively as a function of duty cycle for different values of Q_{eq}.

$$V_{Ls} = \frac{1}{\sqrt{2}}\sqrt{\left(\frac{V_{pk}\omega_o L_s}{|Z_s + Z_p|}\right)^2 + \sum_{n=2}^{\infty}\left(\frac{n\omega_o L_s\sqrt{a_n^2 + b_n^2}}{|n\omega_o L_s - 1/(n\omega_o C_{eq})|}\right)^2} \tag{3- 51}$$

$$V_{Cs} = \frac{1}{\sqrt{2}}\sqrt{\left(\frac{V_{pk}}{\omega_o C_s|Z_s + Z_p|}\right)^2 + \sum_{n=2}^{\infty}\left(\frac{\sqrt{a_n^2 + b_n^2}}{n\omega_o C_s|n\omega_o L_s - 1/(n\omega_o C_{eq})|}\right)^2} \tag{3- 52}$$

$$I_r = \sqrt{I_{r1}^2 + \sum_{n=2}^{\infty} I_{rn}^2} \tag{3- 53}$$

Where I_{r1} and I_{rn} are given by (3- 48) and (3- 49) respectively.

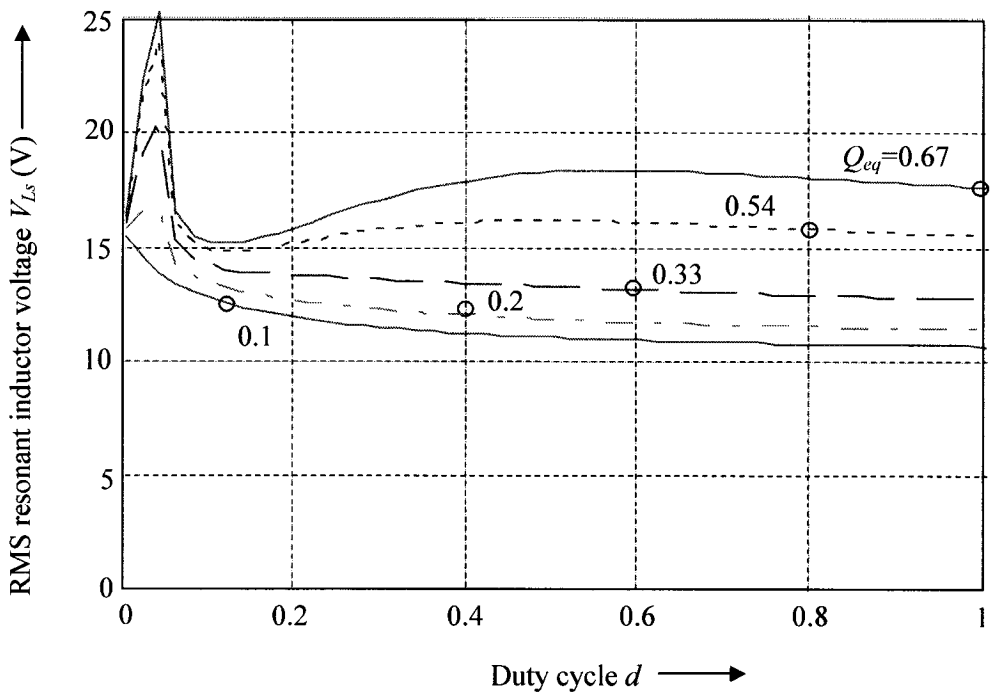


Fig. 3- 18: RMS voltage across the resonant inductor as a function of duty cycle

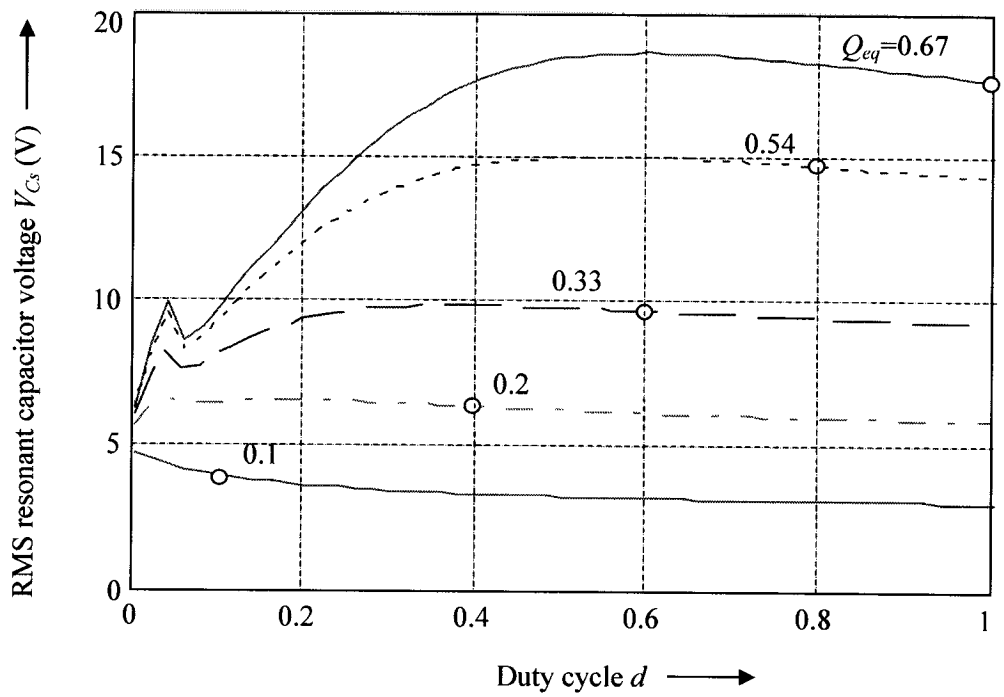


Fig. 3- 19: RMS voltage across the resonant capacitor as a function of duty cycle

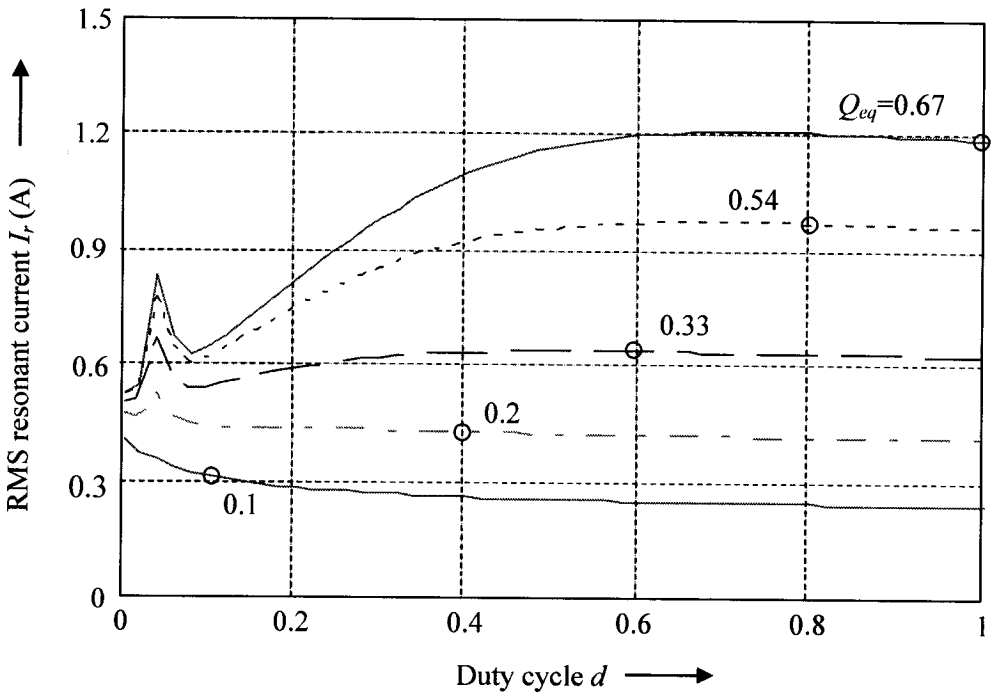


Fig. 3- 20: RMS resonant current as a function of duty cycle

3.1.4.3 *Voltage and current stress of the ac switch*

Since the current flowing through the ac switch is equal to the input resonant current flowing through the resonant tank, its RMS value is the same as (3- 53).

Assume that only the fundamental component of the resonant current charges and discharges the drain-source capacitor of the ac switch C_{ds}, the voltage across C_{ds} can be derived as:

$$v_{ac\_sw} = \frac{1}{C_{ds}} \int_0^t i_{r1} dt = \frac{\hat{V}_{in}}{\omega_o C_{ds} |Z_s + Z_p|} [\cos\theta - \cos(\omega_o t - \theta)] \qquad (3\text{- }54)$$

The peak value of v_{ac_sw} occurs at $t = (1-d)\pi / 2\omega_o$. However, the voltage stress of the ac switch is highly dependent on its drain-to-source capacitance C_{ds}, which is not constant but varies with the voltage across itself. Fig. 3- 21 only conceptually shows the normalized peak value of v_{ac_sw} as a function of the duty cycle.

It can be seen that at the rated load, the voltage across the ac switch is only the voltage drop due to the on resistance of the switch. When the load reduces, the peak value of v_{ac_sw} becomes higher, but will not exceed the peak value of input voltage.

3.1.4.4 *Voltage and current stress of the synchronous rectifier*

The peak value of the voltage across SR top (or bottom) switch appears when the body diode of SR bottom (or top) switch is conducting. It is given by:

$$\hat{V}_{SR} = 2V_o + V_{diode} = 3.8V \qquad (3\text{- }55)$$

The RMS current through each synchronous rectifier switch is calculated by (3- 56) and plotted in Fig. 3- 22 as a function of duty cycle.

$$I_{SR} = NI_r / \sqrt{2} \qquad (3\text{- }56)$$

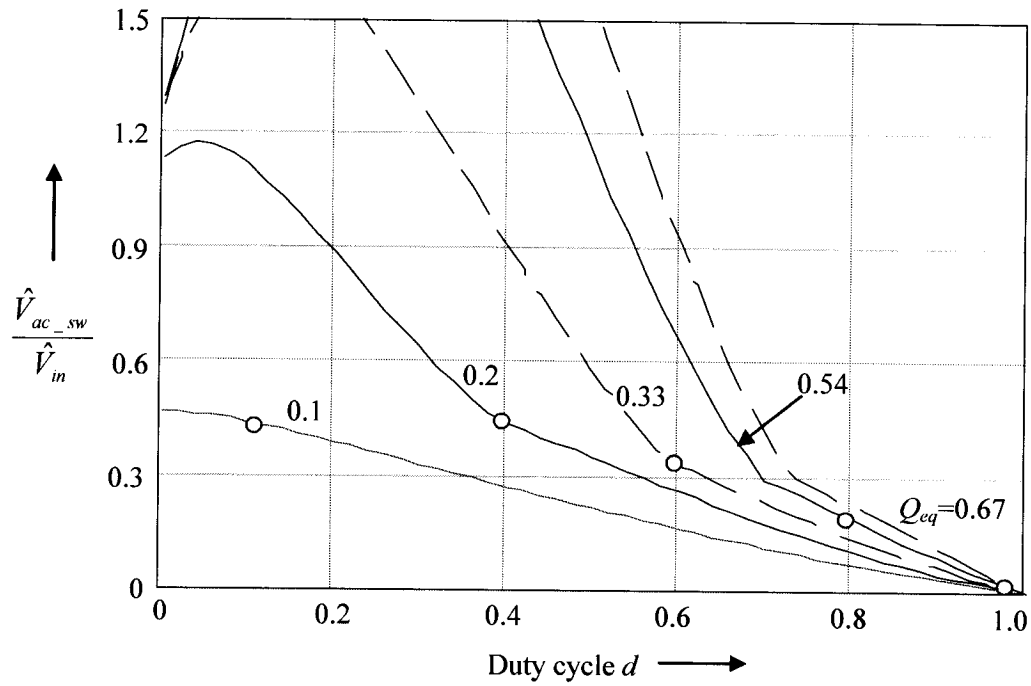


Fig. 3- 21: Voltage stress of the ac switch as a function of duty cycle

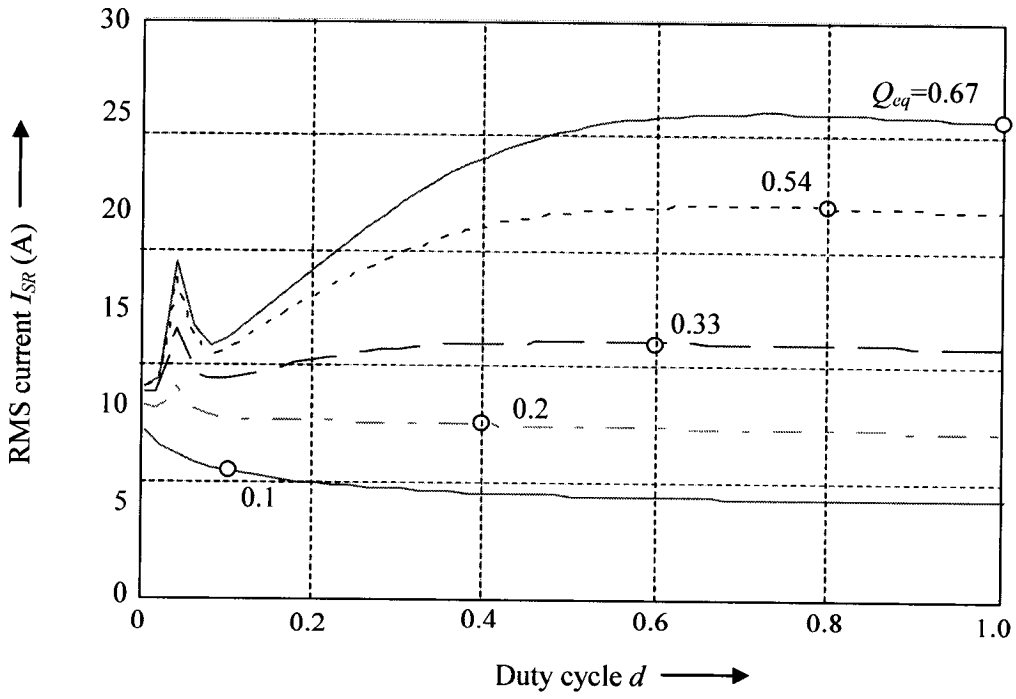


Fig. 3- 22: RMS current through each SR switch as a function of duty cycle

3.2 PHASE-SHIFT CONTROLLED AC VRM

In this section, a phase-shift-modulated AC VRM is presented. The circuit diagram and the operating principle are described in section 3.2.1 and 3.2.2 respectively. The steady-state analysis to derive the output voltage control and the expressions for the circuit voltages and currents is carried out in section 3.2.3. The performance curves showing the characteristics of the input current, such as the displacement power factor, the total harmonic distortion and the power factor, and the voltage/current stress of the switches and the resonant tank components are presented in section 3.2.4.

3.2.1 Circuit Description

The circuit diagram of the phase-shift-modulated AC VRM is shown in Fig. 3-23. It has the same topology as the pulse-width-modulated AC VRM presented in section 3.1.1. The only difference between these two converters is the control method. In Fig. 3-23, the ac switch of this converter is controlled by phase-shift modulation instead of pulse-width modulation in Fig. 3- 1.

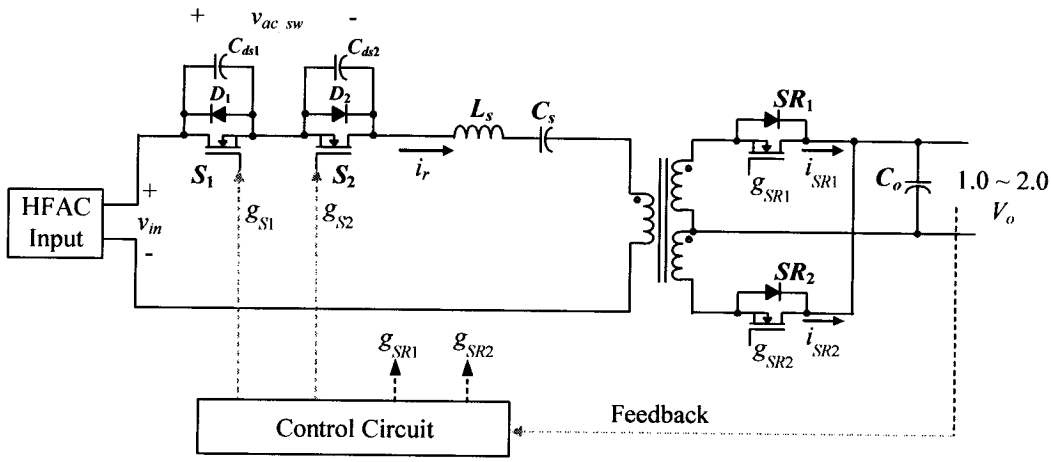


Fig. 3- 23: Phase-shift-modulated AC VRM

3.2.2 Principle of Operation

Fig. 3- 24 shows the key operating waveforms of the converter controlled by phase-shift modulation. The gating signal of S_2 is synchronized with the input voltage at a control angle α, which can be varied from $\pi/2$ to π. The gating signal for S_1 is the complement of that for S_2.

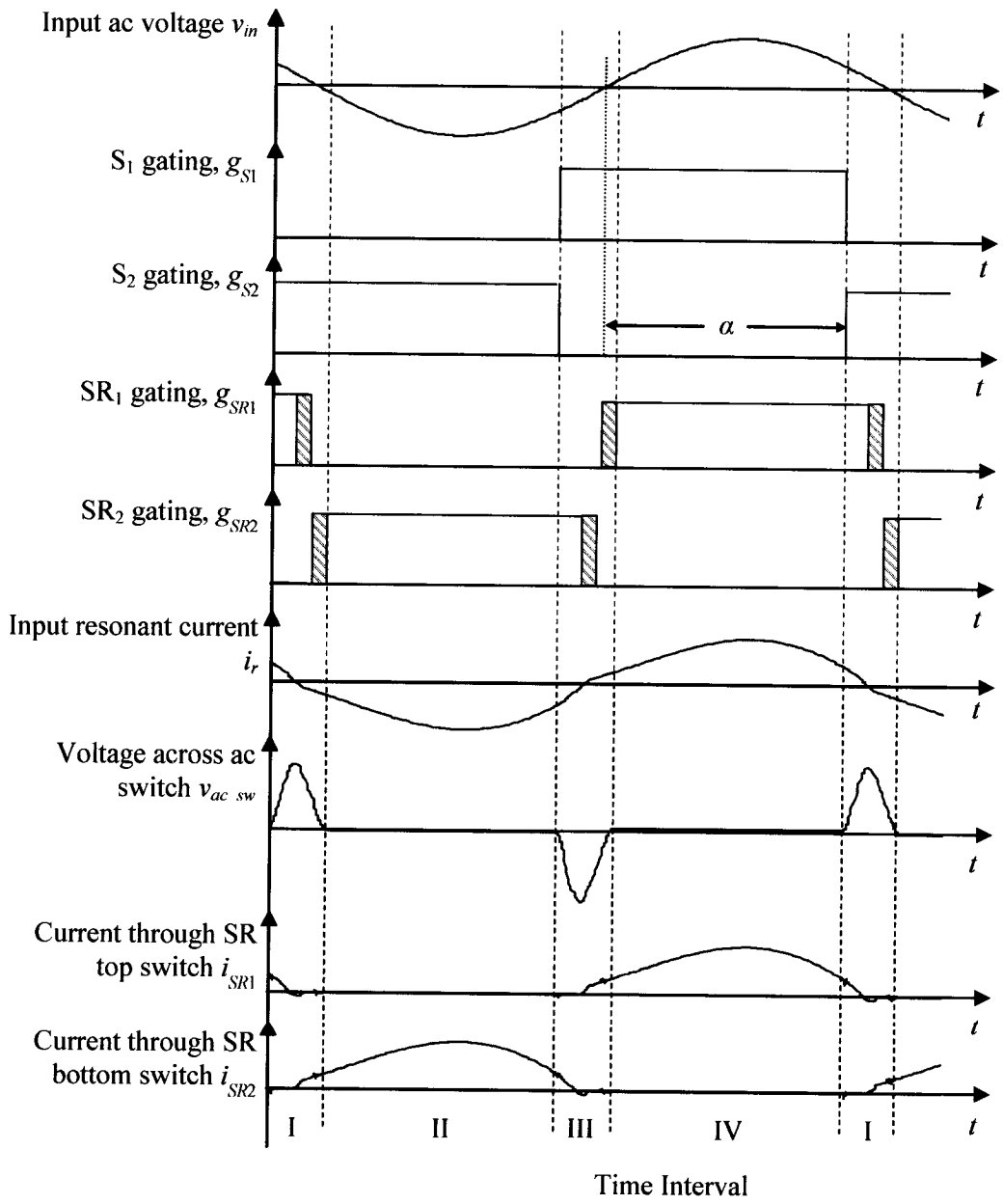


Fig. 3- 24: Operating waveforms of the phase-shift-modulated AC VRM

For each switching cycle, depending on the operation of the ac switch, the converter operates in the following 4 intervals.

Interval I:

At the beginning of this interval, switch S_1 is turned off and S_2 is turned on under zero voltage. The resonant current is shunted into C_{ds1} to charge and discharge it.

Interval II:

At the beginning of this interval, the voltage across C_{ds1} reaches zero, and it will be kept zero since S_2 is still on. The negative resonant current is carried by D_1 and S_2.

Interval III:

At the beginning of this interval, switch S_1 is turned on under zero voltage, and the negative resonant current is shunted into the capacitor C_{ds2}. Meanwhile, C_{ds2} acts as a lossless snubber to reduce the turn-off loss for switch S_2.

Interval IV:

At the beginning of this interval, the voltage across C_{ds2} reaches zero, and it will be kept zero since S_1 is still on. Now the positive resonant current is carried by S_1 and D_2, so that S_2 can be turned on under zero voltage at the beginning of the next interval.

The active current path of the ac switch in each interval is shown in Fig. 3- 25. The current path of the SR switches in each interval is the same as the corresponding interval in Fig. 3- 3 for PWM AC VRM.

It can be seen from Fig. 3- 24 and Fig. 3- 25 that ZVS of the primary side ac switch can be achieved under any load condition. SR switches operate with ZVS at both turn-on and turn-off due to the same reasons as explained for the PWM AC VRM in section 3.1.2.

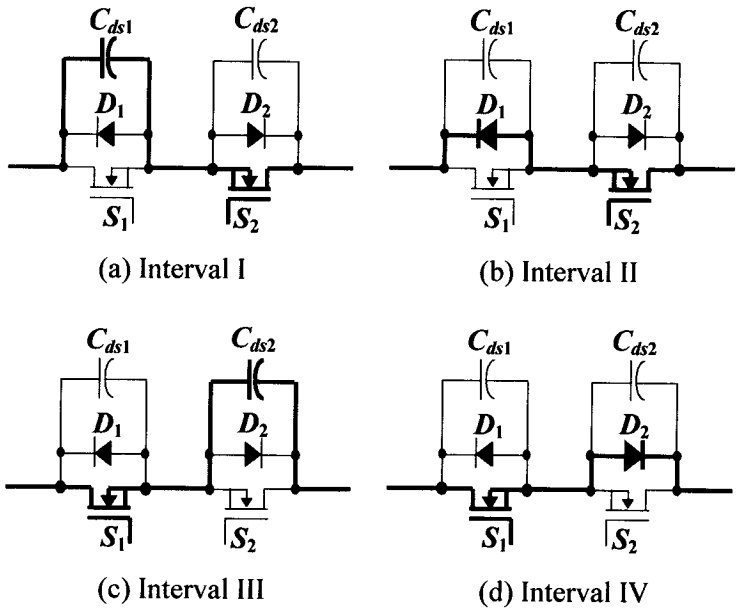


Fig. 3- 25: Active current path through ac switch of the phase-shift-modulated AC VRM in each operating interval

3.2.3 Steady-State Analysis of the Phase-Shift-Modulated AC VRM

In this section, the steady-state analysis is carried out on the base of some simplifying assumptions made in section 3.2.3.1. The output voltage control is derived as a function of the control angle α in section 3.2.3.2. The time-varying expressions of the circuit voltages and currents are presented in section 3.2.3.3.

3.2.3.1 Simplifying assumptions

The steady-state analysis of the phase-shift-modulated AC VRM is carried out using the following assumptions:

(i) The input voltage of the converter is a pure sine wave;

(ii) The output capacitor is so large that the dc output voltage is constant;

(iii) The dead time between the gating signals is negligible;

(iv) The switches of the ac switch offer either zero or infinite impedance to the current flowing through them;

(v) The inherent drain-source capacitance C_{ds} of the ac switch is considered as a constant external capacitance across the ideal switch;

(vi) The transformer primary winding leakage inductance is lumped with the resonant inductance.

With the above assumptions, the simplified equivalent circuit of the converter in each operating interval is shown in Fig. 3- 26. In Fig. 3- 26, L_m is the transformer magnetizing inductance. L_{lk} represents the sum of the transformer secondary leakage inductance and parasitic interconnect inductance of SR switches reflected to the primary side of the transformer. The output rectification stage is represented by an ac equivalent resistance at the primary side of the transformer.

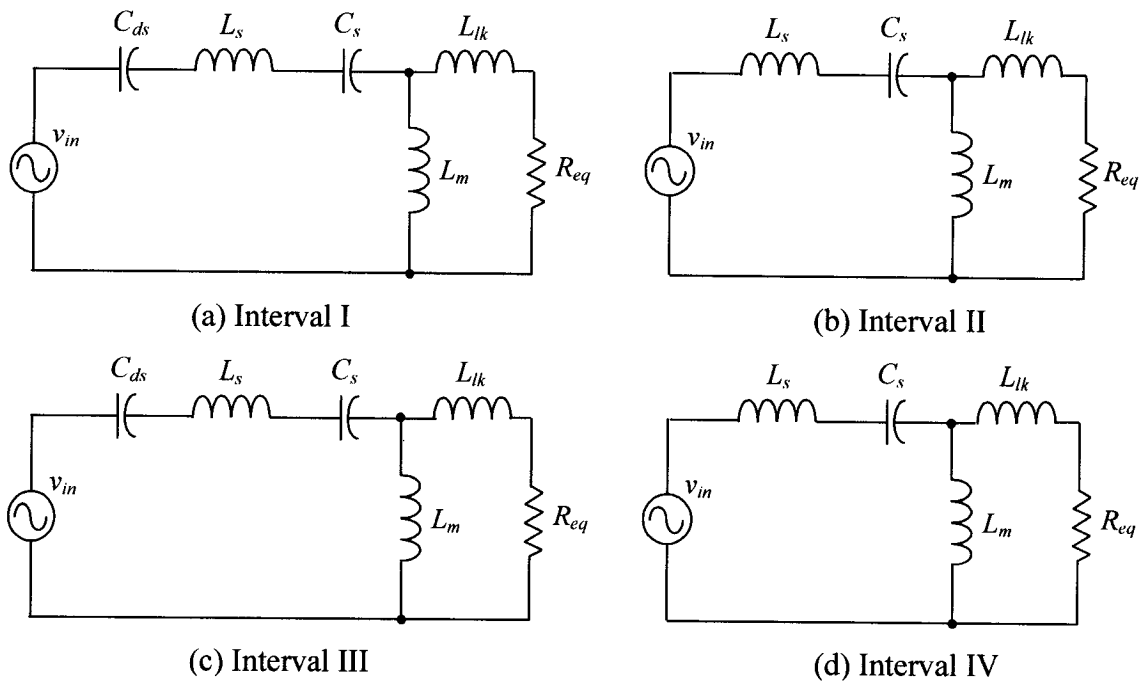


Fig. 3- 26: Simplified equivalent circuit of the phase-shift controlled converter in each operating interval

3.2.3.2 *Output voltage control*

As described in the operating principle, the ac switch with its drain-to-source capacitor C_{ds} can be seen as a switch-controlled capacitor C_{sw}. The equivalent circuit of the converter is drawn in Fig. 3- 27.

To derive the output voltage control, the principle waveforms of the converter are redrawn in Fig. 3- 28.

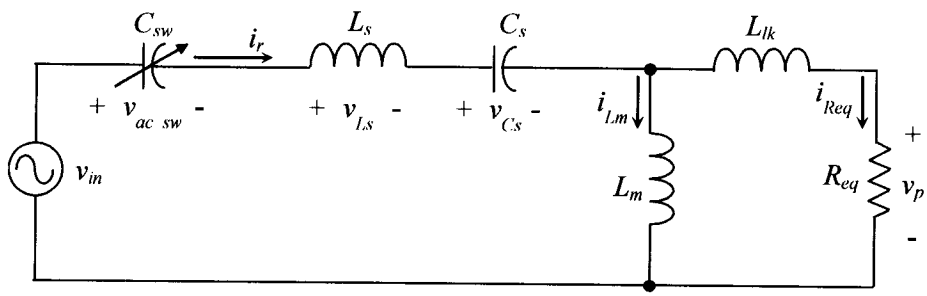


Fig. 3- 27: Equivalent circuit of the phase-shift-modulated converter

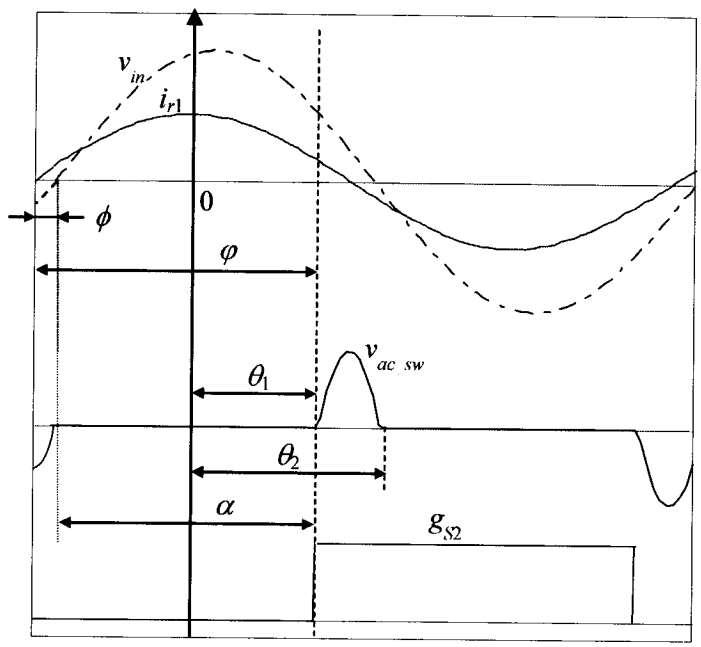


Fig. 3- 28: Principle waveforms to derive phase-shift output voltage control

In Fig. 3- 28, only the fundamental component of the resonant current, which leads the input voltage v_{in} by ϕ, is considered to charge and discharge the drain-to-source capacitor C_{ds}. The current flow is governed by:

$$i_{r1} = \frac{\hat{V}_{in}}{|Z_{in}|}\cos(\omega_o t) \tag{3- 57}$$

Where Z_{in} is the fundamental input impedance seen from the input, and $\hat{V}_{in}$ is the peak value of the input voltage.

Then the voltage across the drain-to-source capacitor can be derived as:

$$v_{ac\_sw} = \frac{1}{C_{ds}}\int_{\theta_1/\omega_o}^{t} i_{r1}dt = \frac{\hat{V}_{in}}{\omega_o C_{ds}|Z_{in}|}\left(\sin(\omega_o t) - \sin(\theta_1)\right) \tag{3- 58}$$

Where

$$\theta_1 = \varphi - \pi/2 \tag{3- 59}$$

$$\varphi = \alpha + \phi \tag{3- 60}$$

At θ_2, voltage v_{ac_sw} is discharged to be zero. Therefore,

$$\theta_2 = \pi - \theta_1 = 3\pi/2 - \varphi \tag{3- 61}$$

The waveform of v_{ac_sw} is an odd function as shown in Fig. 3- 28. Using Fourier series expansion, the fundamental component of v_{ac_sw} can be expressed as:

$$v_{ac\_sw1} = b_1 \sin(\omega_o t) \tag{3- 62}$$

Where

$$b_1 = \frac{\hat{V}_{in}}{\omega_o C_{ds}|Z_{in}|}\left[2 - \frac{1}{\pi}\left(2\varphi - \sin(2\varphi)\right)\right] \tag{3- 63}$$

Comparing (3- 57) and (3- 62), the equivalent switch-controlled capacitance can be obtained as:

$$C_{sw} = \frac{C_{ds}}{2 - \frac{1}{\pi}(2\varphi - \sin(2\varphi))} \tag{3- 64}$$

In (3- 64), the angle φ can be expressed by (3- 60) in terms of the control angle α and the phase angle ϕ, which is approximately given by:

$$\phi = \frac{\theta_2 - \theta_1}{2} = \pi - \varphi \tag{3- 65}$$

Substituting ϕ in (3- 60) by (3- 65), the angle φ can be expressed by only the control angle α:

$$\varphi = \alpha/2 + \pi/2 \tag{3- 66}$$

Therefore, the equivalent switch-controlled capacitance can be given as a function of the control angle α:

$$C_{sw} = \frac{C_{ds}}{1 - (\alpha + \sin(\alpha))/\pi} \tag{3- 67}$$

As a result, the equivalent series resonant capacitance, which is the series connection of the switch-controlled capacitor C_{sw} and the resonant capacitor C_s, is also a function of the control angle α given by (3- 68), and is plotted in Fig. 3- 29.

$$C_{eq} = \frac{C_{sw} \cdot C_s}{C_{sw} + C_s} \tag{3- 68}$$

Therefore, the ac switch has the effect of changing resonant frequency around, as given by (3- 69), while the operating frequency is fixed, as shown in Fig. 3- 30.

$$\omega_{eq} = 1/\sqrt{L_s C_{eq}} \tag{3- 69}$$

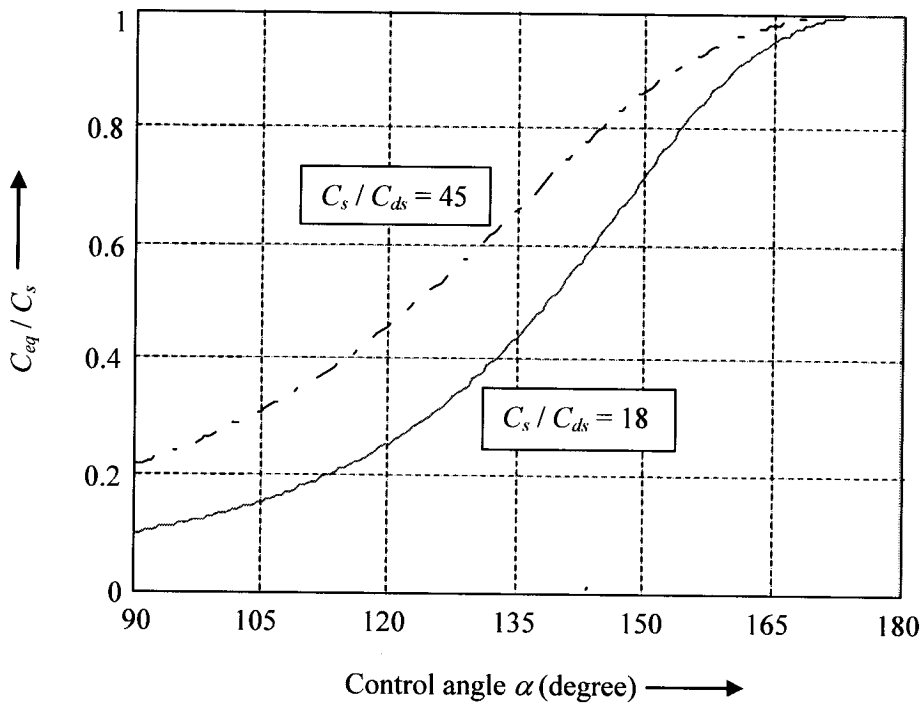


Fig. 3- 29: Normalized equivalent capacitance as a function of control angle α

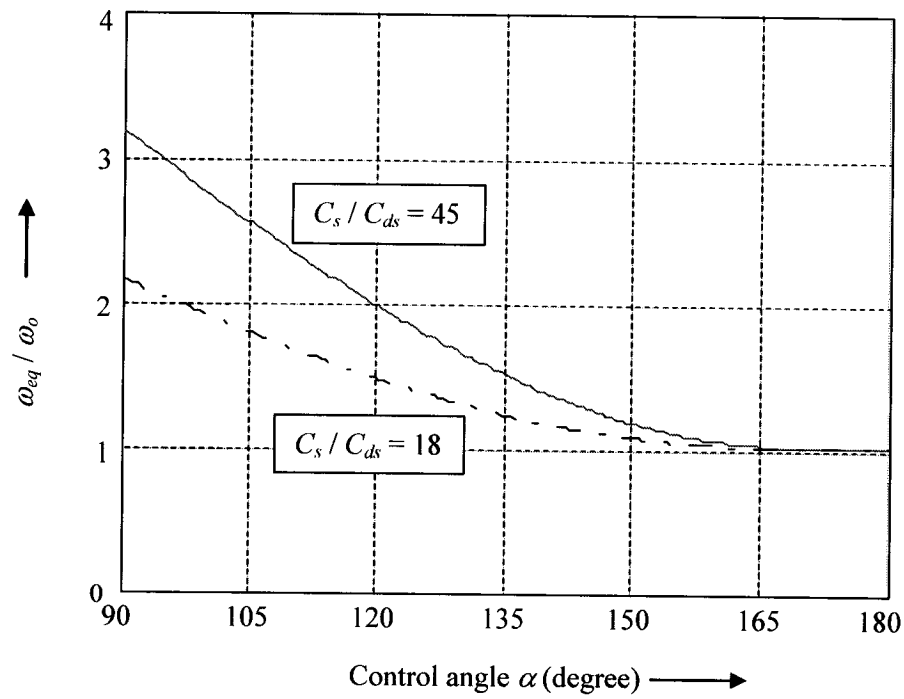


Fig. 3- 30: Normalized equivalent resonant frequency as a function of control angle α

From the equivalent circuit of Fig. 3- 27, the voltage transfer function can be derived as:

$$M = \frac{NV_o}{\hat{V}_{in}} = \frac{\pi}{4} \cdot \frac{1}{\sqrt{(1 + k_{Lm}(1-\omega^2))^2 + Q_{eq}^2(1-\omega^2)^2}} \qquad (3\text{- }70)$$

Taking into account the magnetizing inductance of the transformer, for a value of $k_{Lm} = 0.05$, the voltage transfer function versus the control angle α variation is shown in Fig. 3- 31.

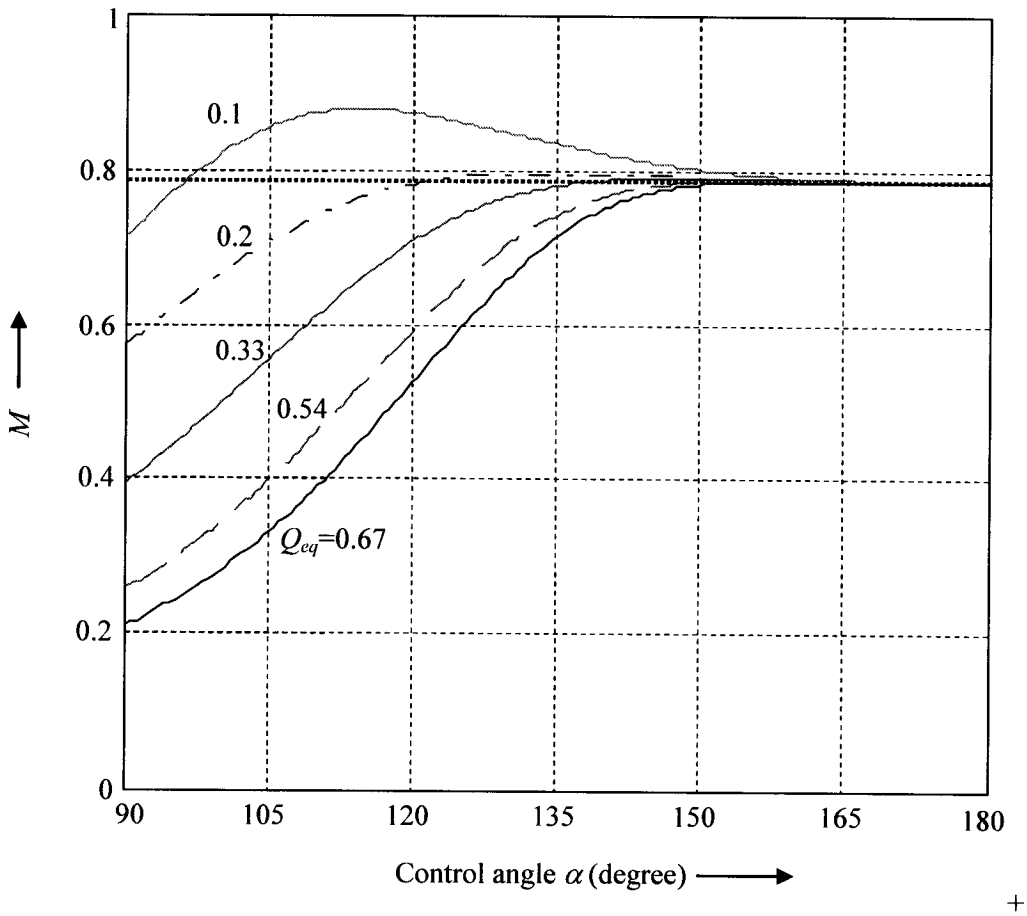


Fig. 3- 31: Phase-shift output voltage control with non-ideal transformer

3.2.3.3 Circuit voltages and currents

Since the phase-shift-modulated AC VRM has the same circuit topology as the pulse-width-modulated AC VRM, all the equations for the time-varying circuit variables derived in section 3.1.3 for the pulse-width-modulated AC VRM are also valid for the phase-shift-modulated AC VRM, except replacing the expression of C_{eq} with (3- 68). At 50% load, the theoretical and simulation waveforms of the circuit variables for the phase-shift-modulated AC VRM are very similar to those presented in Fig. 3- 12 and Fig. 3- 13 for the pulse-width-modulated AC VRM. These contents are not repeated here.

3.2.4 Performance Curves for the Phase-Shift-Modulated AC VRM

In this section, the characteristics of the input resonant current, such as the displacement power factor, the total harmonic distortion, and the power factor are studied. The RMS values of the voltages and current of the resonant tank are calculated. The voltage and current stress of all the switches employed in the circuit as ac switch and synchronous rectifier are presented. By using C_{eq} given by (3- 68), all the equations derived in section 3.1.4 for the pulse-width-modulated AC VRM are still valid in this section and are used to plot all the performance curves as a function of control angle for different values of the quality factor.

3.2.4.1 Characteristics of the input resonant current

The displacement power factor (*DPF*), the total harmonic distortion (*THD*) and the power factor (*PF*) of the input resonant current as a function of control angle are plotted in Fig. 3- 32, Fig. 3- 33, and Fig. 3- 34 respectively.

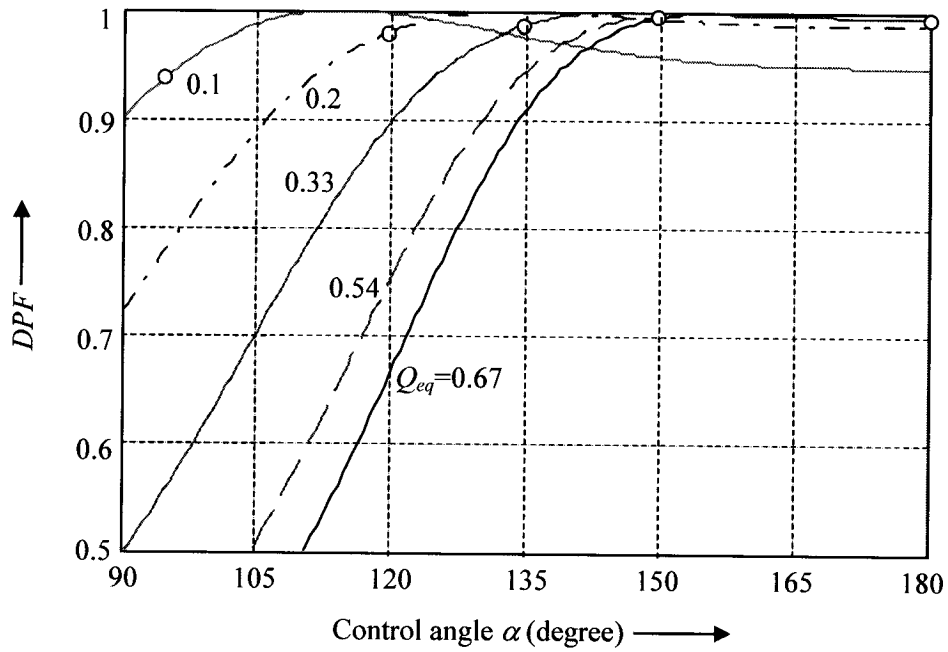


Fig. 3- 32: DPF of the input resonant current as a function of control angle α

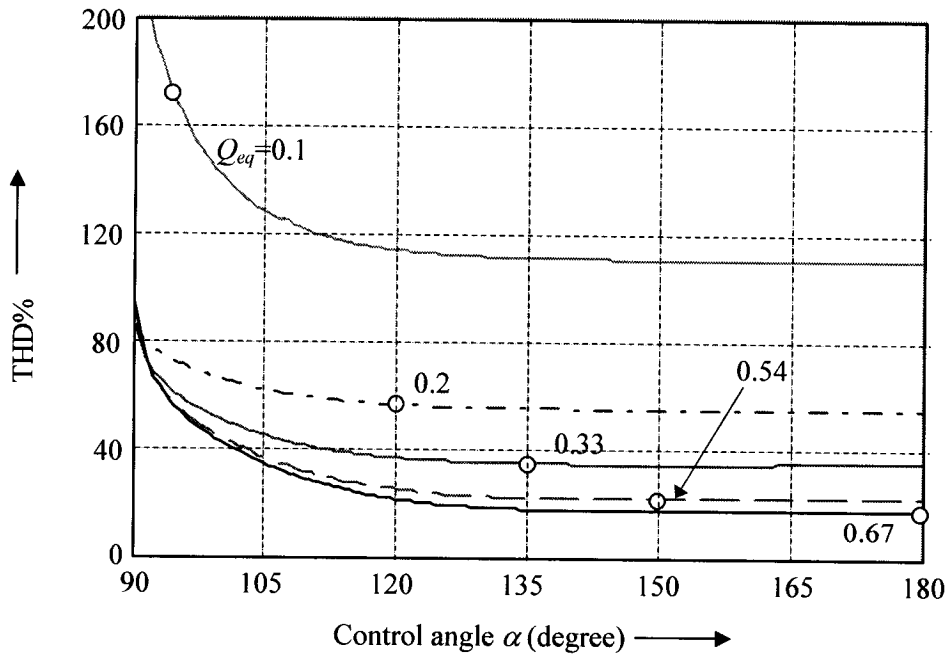


Fig. 3- 33: THD of the input resonant current as a function of control angle α

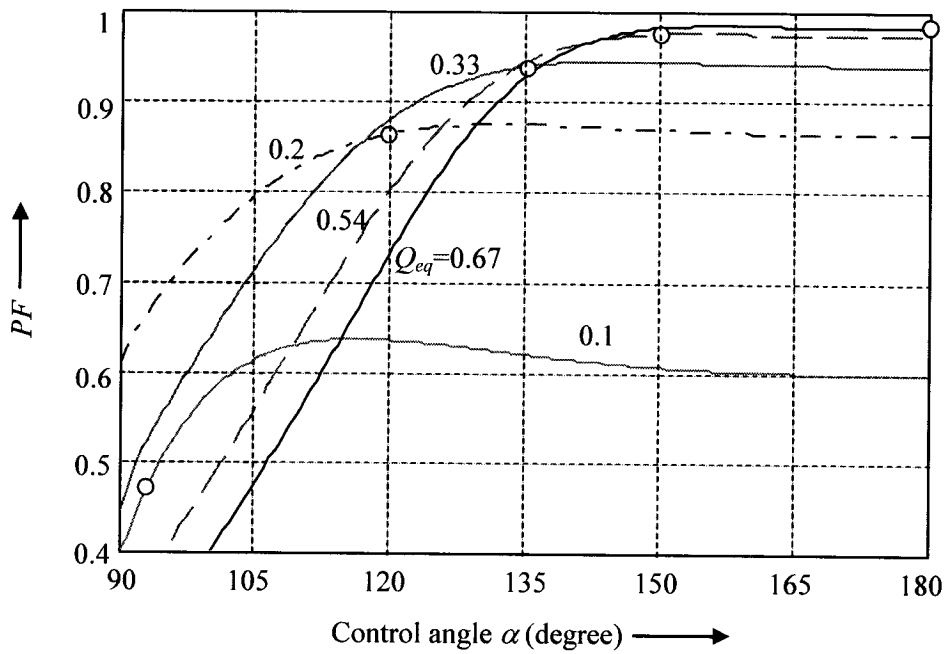


Fig. 3- 34: PF of the input resonant current as a function of control angle α

3.2.4.2 RMS voltages and current of the resonant tank

The RMS value of the voltage across the resonant inductor and capacitor are plotted in Fig. 3- 35 and Fig. 3- 36 respectively. The RMS value of the current flowing through the resonant tank is plotted in Fig. 3- 37.

3.2.4.3 Voltage and current stress of the ac switch

The ac switch has the same current stress as the resonant tank, as shown in Fig. 3- 37. The peak voltage across each switch of the ac switch is plotted in Fig. 3- 38.

3.2.4.4 Voltage and current stress of the synchronous rectifier

The peak value of the voltage across each switch of the synchronous rectifier is given by (3- 55), which is equal to 3.8 V, and the RMS current through each SR switch is plotted in Fig. 3- 39.

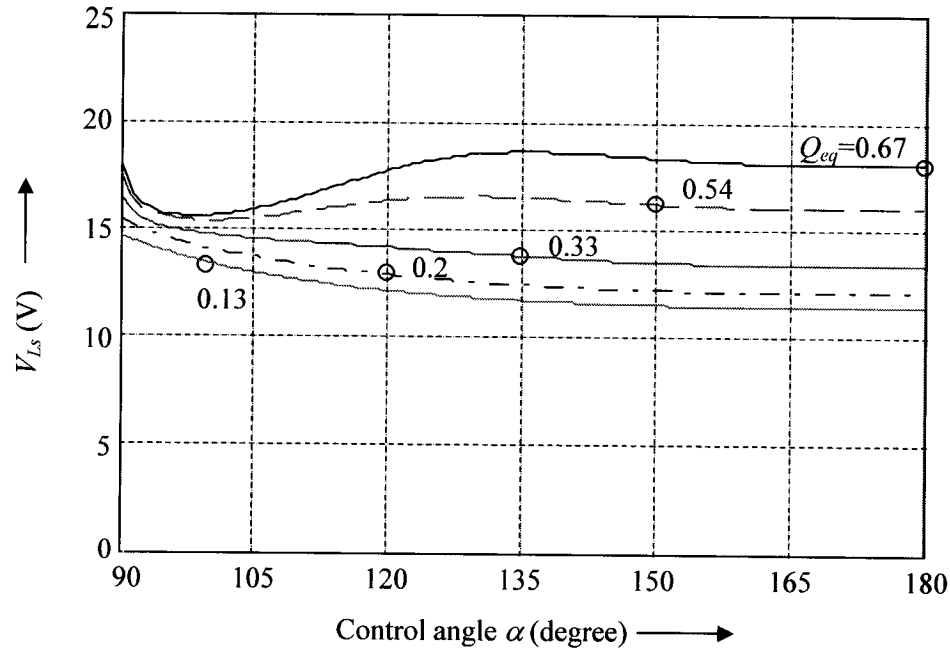


Fig. 3- 35: RMS voltage across the resonant inductor as a function of control angle

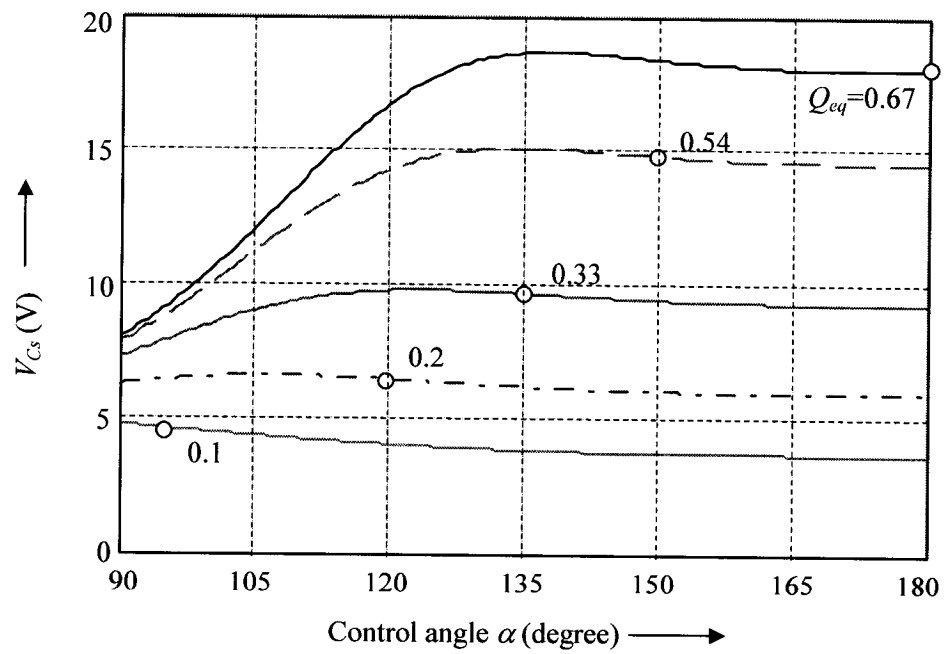


Fig. 3- 36: RMS voltage across the resonant capacitor as a function of control angle

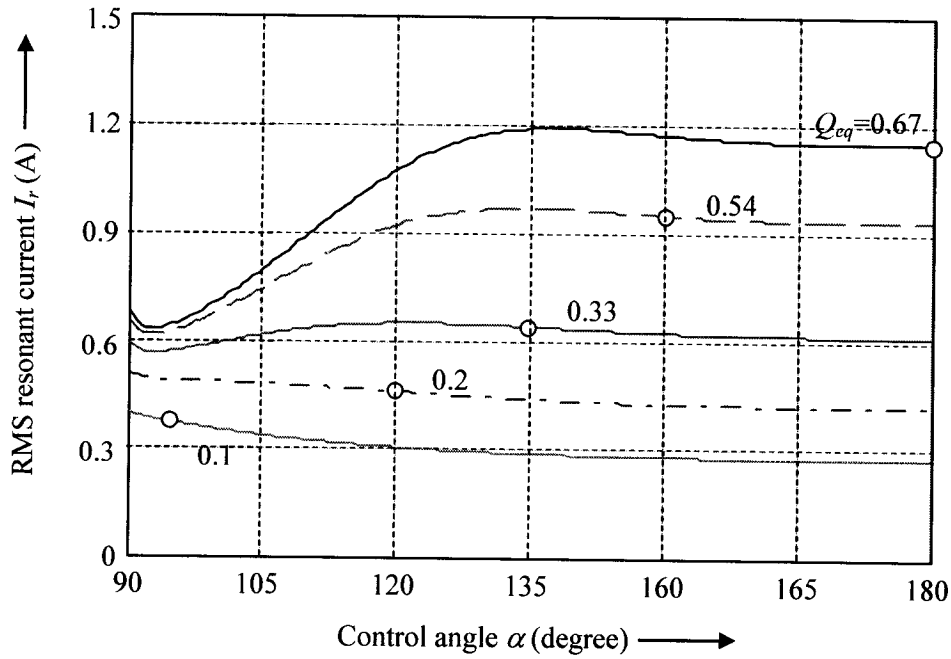


Fig. 3- 37: RMS resonant current as a function of control angle α

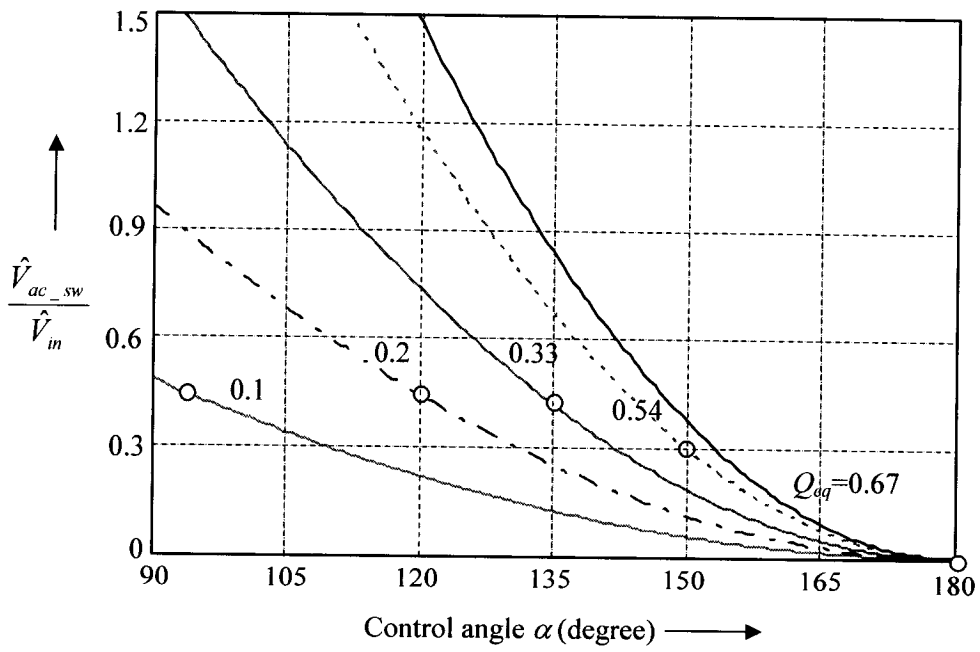


Fig. 3- 38: Voltage stress of the ac switch as a function of control angle α

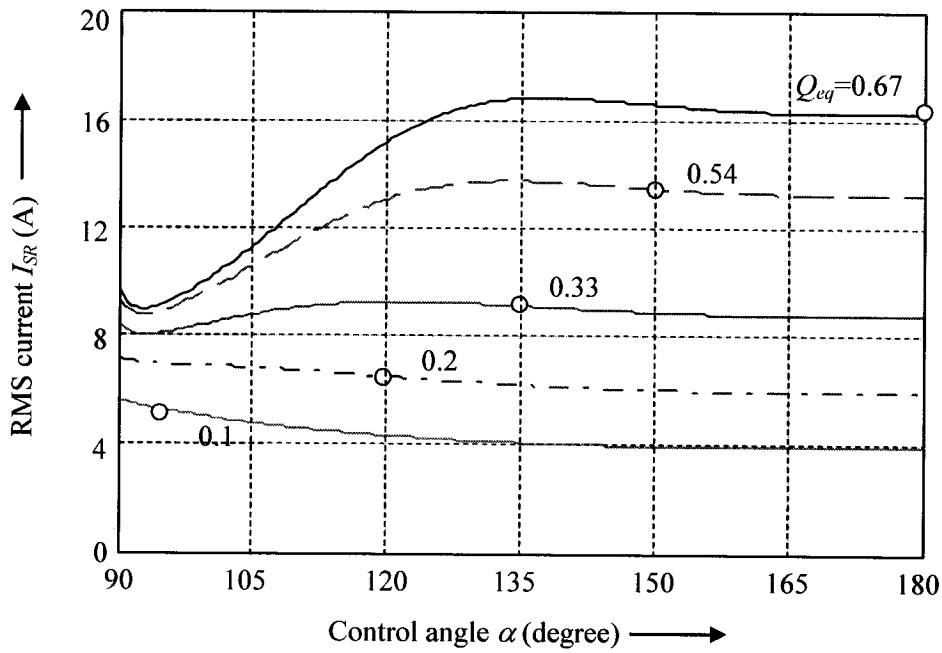


Fig. 3- 39: RMS current through each SR switch as a function of control angle α

3.3 Performance Comparison of the Pulse-Width-Modulated AC VRM and Phase-Shift-Modulated AC VRM

In this section, performance curves of AC VRM obtained from section 3.1.4 for PWM control and from section 3.2.4 for phase-shift control are used to compare the converter's performance. Simulation results obtained from PWM control and phase-shift control respectively are presented to show (i) operating waveforms, and (ii) operation of zero-voltage switching. Finally, an optimum control method is chosen for this AC VRM application.

3.3.1 Characteristics of the Input Resonant Current

The RMS value, the total harmonic distortion and the power factor of the input resonant current with two different modulation techniques are shown in Fig. 3- 40, Fig. 3- 41 and Fig. 3- 42 respectively.

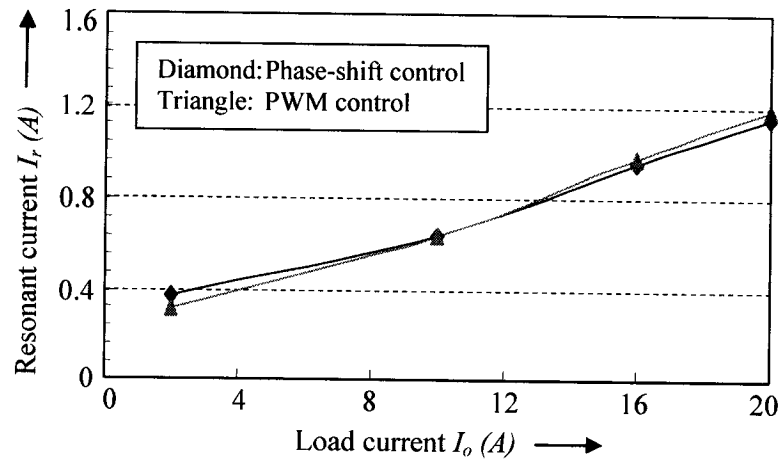


Fig. 3- 40: RMS resonant current under different load conditions

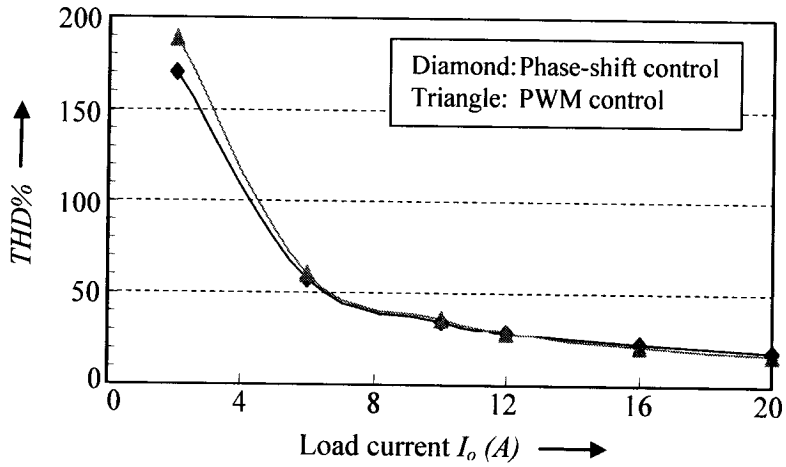


Fig. 3- 41: THD of the input current under different load conditions

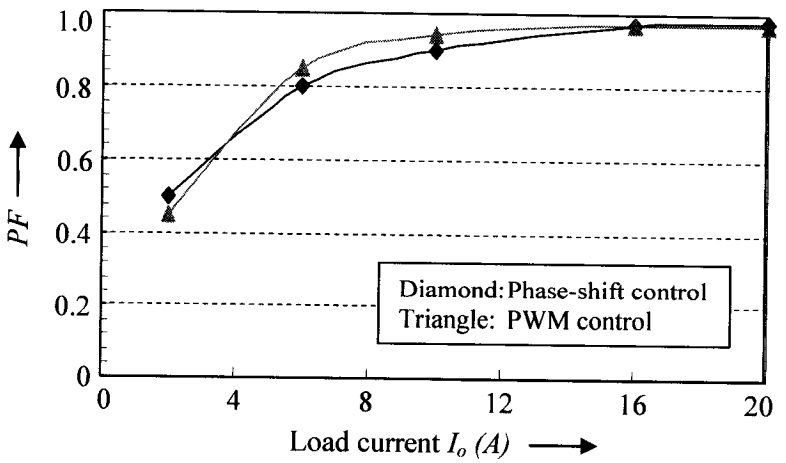


Fig. 3- 42: PF of the input current under different load condition

3.3.2 Voltage and Current Stress of the Resonant Tank

The voltage stress across the resonant capacitor and inductor with two different modulation techniques are shown in Fig. 3- 43 and Fig. 3- 44 respectively. The current stress is the same as Fig. 3- 40.

3.3.3 Voltage and Current Stress of the Switches

The voltage stress of the ac switch is shown in Fig. 3- 45, and the current stress is the same as Fig. 3- 40. The voltage stress of the rectifier is shown in Fig. 3- 46, and the current stress is shown in Fig. 3- 47.

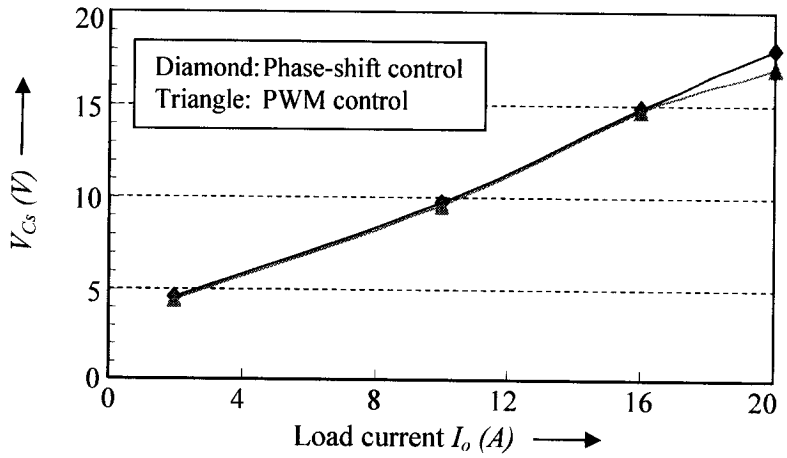


Fig. 3- 43: RMS voltage across the resonant capacitor under different load conditions

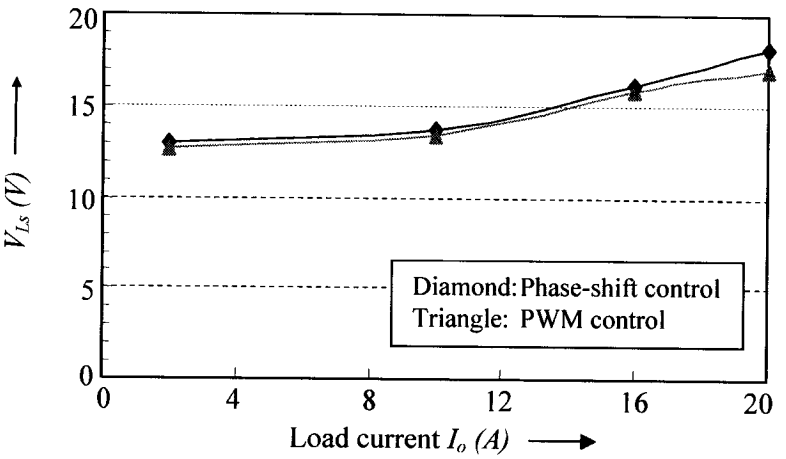


Fig. 3- 44: RMS voltage across the resonant inductor under different load conditions

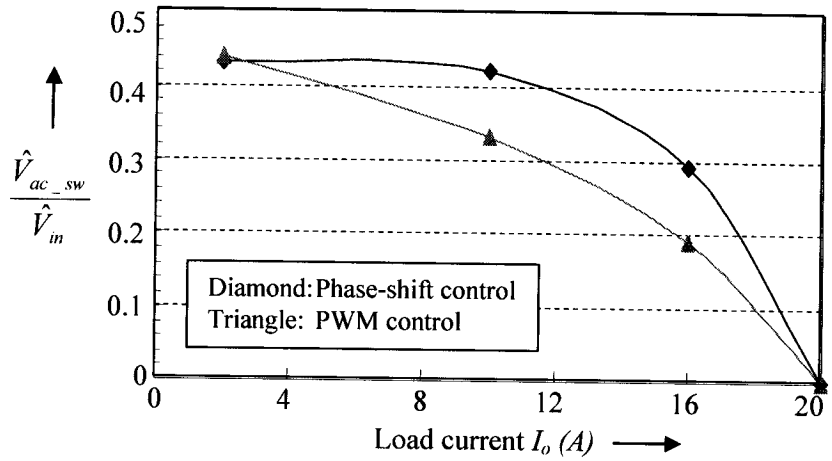


Fig. 3- 45: Voltage stress of the ac switch under different load conditions

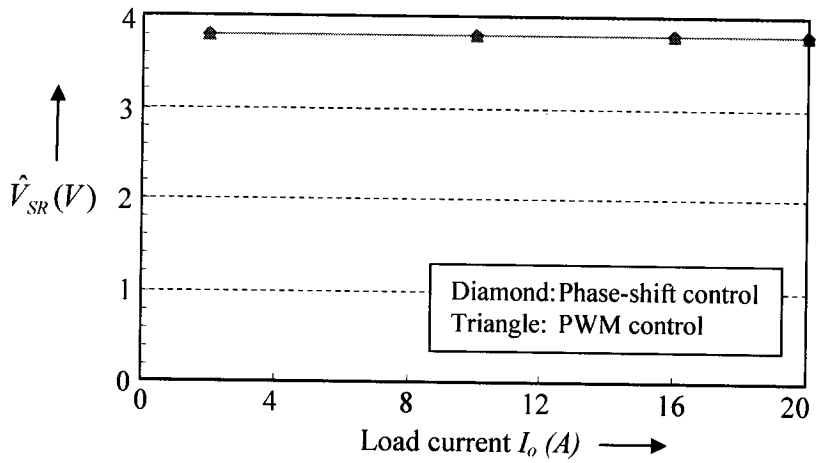


Fig. 3- 46: voltage stress of each SR switch under different load conditions

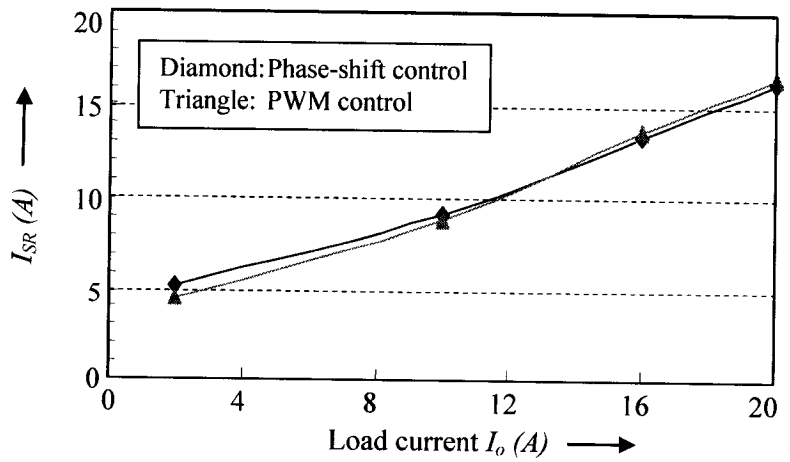


Fig. 3- 47: RMS current through SR switch under different load conditions

Comparing the performance curves of these two control techniques, it can be seen that:

(i) From Fig. 3- 42, Fig. 3- 43 and Fig. 3- 45, at the rated load, the proposed AC VRM topology has close-to-unity power factor, low total harmonic distortion in input current, and low voltage stress of the active ac switch (close-to-zero for PWM control and 0.7 V for phase-shift control) by using either PWM control or phase-shift control method.

(ii) From Fig. 3- 40 and Fig. 3- 43 to Fig. 3- 47, the voltage and current stress of the ac switch, the resonant tank, and the synchronous rectifier are the same by using either PWM control or phase-shift control.

(iii) As shown in Fig. 3- 45, the converter with PWM control close to full load has lower voltage stress of the active ac switch due to less charging and discharging time for C_{ds}. However, at light load, the voltage stress of the active ac switch of PWM control becomes similar to the phase-shift control. This fact is because that the gating signals of PWM, as shown in Fig. 3- 2, are very similar as of the phase-shift control at reduced load since intervals III and VI in Fig. 3- 2 when both switches S_1 and S_2 are conducting becomes very short.

3.3.4 Simulation Results

The operation of the proposed AC VRM with the phase-shift control or PWM control is simulated by using the simulation tool PSpice. The PSipice models of the phase-shift-modulated AC VRM and the pulse-width-modulated AC VRM are shown in Appendix D. The specifications and parameters of the simulation circuit are list in Table 3-1.

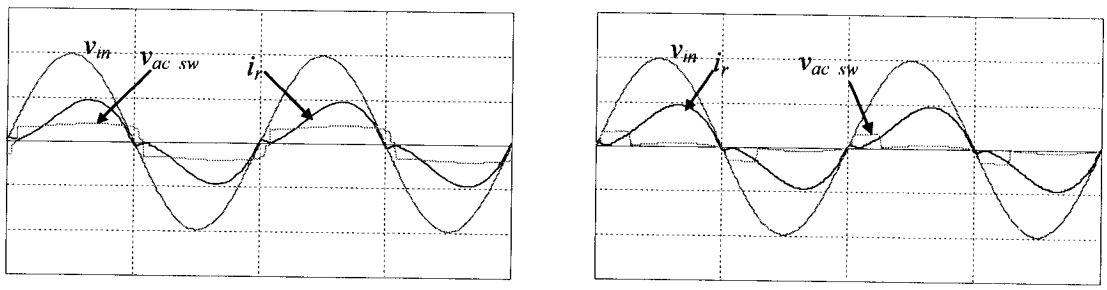
Table 3-1: Specifications and parameters of the simulation circuit of AC VRM

Specifications	V_{in} = 28Vrms, 1MHz	P_o = 30W, V_o = 1.5V, I_o = 20A
Parameters	L_s = 2.5μH, C_s = 10nF, C_o = 500μF Transformer turns ratio: N = 19.7	
Switches	S_1 & S_2: IRFP150	SR_1 & SR_2: 4 IRL3803 in parallel

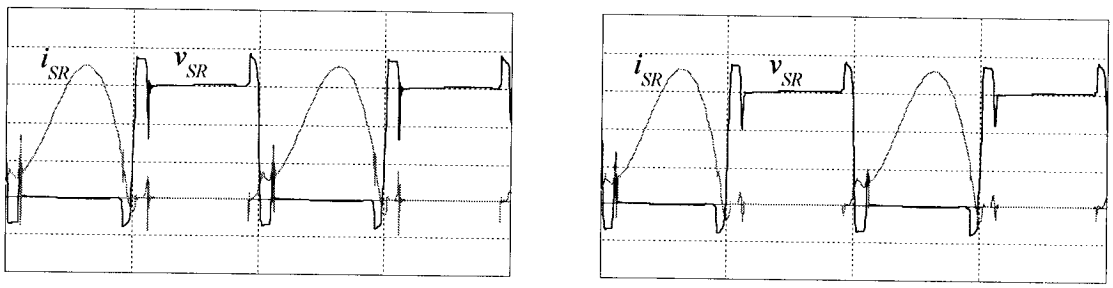
3.3.4.1 Main operating waveforms

The main operating waveforms of the primary side and the synchronous rectifier under different load conditions are shown in Fig. 3- 48, Fig. 3- 49, and Fig. 3- 50. It can be seen that the operating waveforms have only slight differences by using two different control techniques. The input current is highly distorted at light load because of the superimposed magnetizing current which becomes significant at light load.

Input voltage v_{in} (20V/div), Input current i_r (2A/div), Voltage across ac switch $v_{ac\ sw}$ (2V/div)



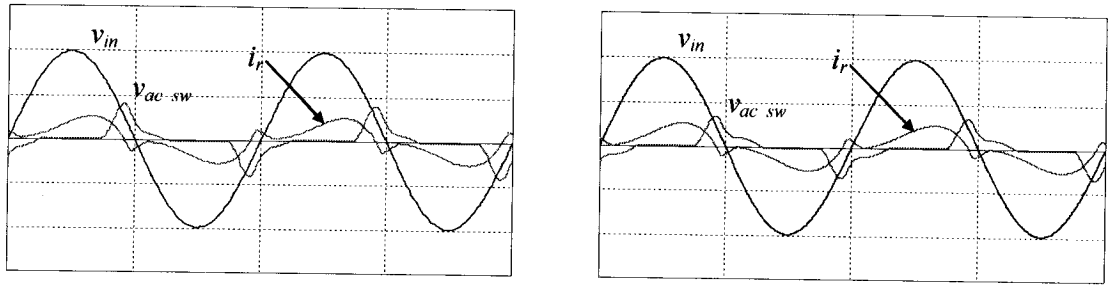
Voltage v_{SR} (1V/div) and current i_{SR} (10A/div) of the top switch of SR



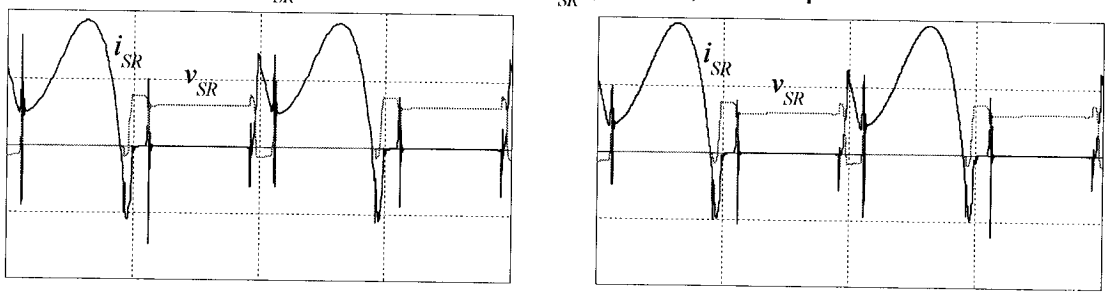
(a) Phase-shift control (b) PWM control

Fig. 3- 48: Simulation waveforms at full load (Horizontal time scale: 0.5μs/div)

Input voltage v_{in} (20V/div), Input current i_r (2A/div), Voltage across ac switch $v_{ac\ sw}$ (20V/div)



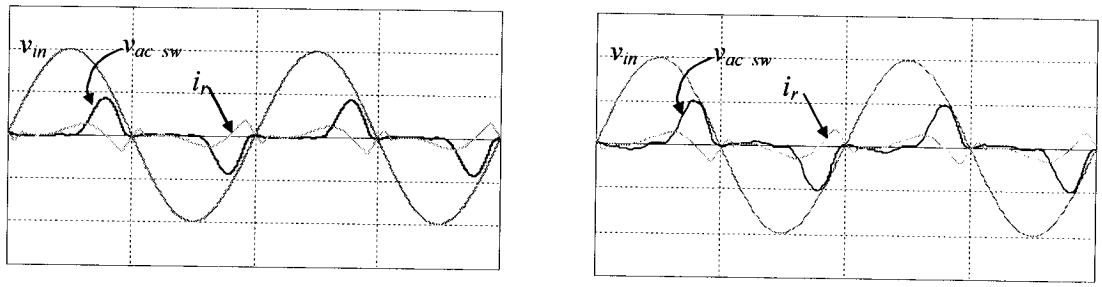
Voltage v_{SR} (5V/div) and current i_{SR} (10A/div) of the top switch of SR



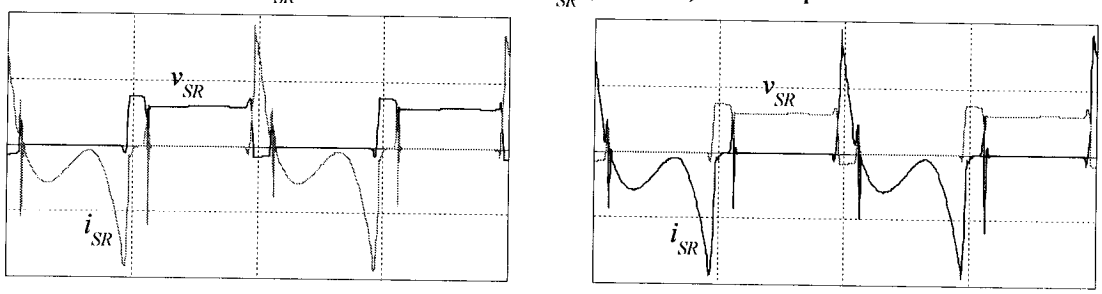
(a) Phase-shift control (b) PWM control

Fig. 3- 49: Simulation waveforms at 50% load (Horizontal time scale: 0.5μs/div)

Input voltage v_{in} (20V/div), Input current i_r (1A/div), Voltage across ac switch $v_{ac\ sw}$ (20V/div)



Voltage v_{SR} (5V/div) and current i_{SR} (10A/div) of the top switch of SR



(a) Phase-shift control (b) PWM control

Fig. 3- 50: Simulation waveforms at 10% load (Horizontal time scale: 0.5μs/div)

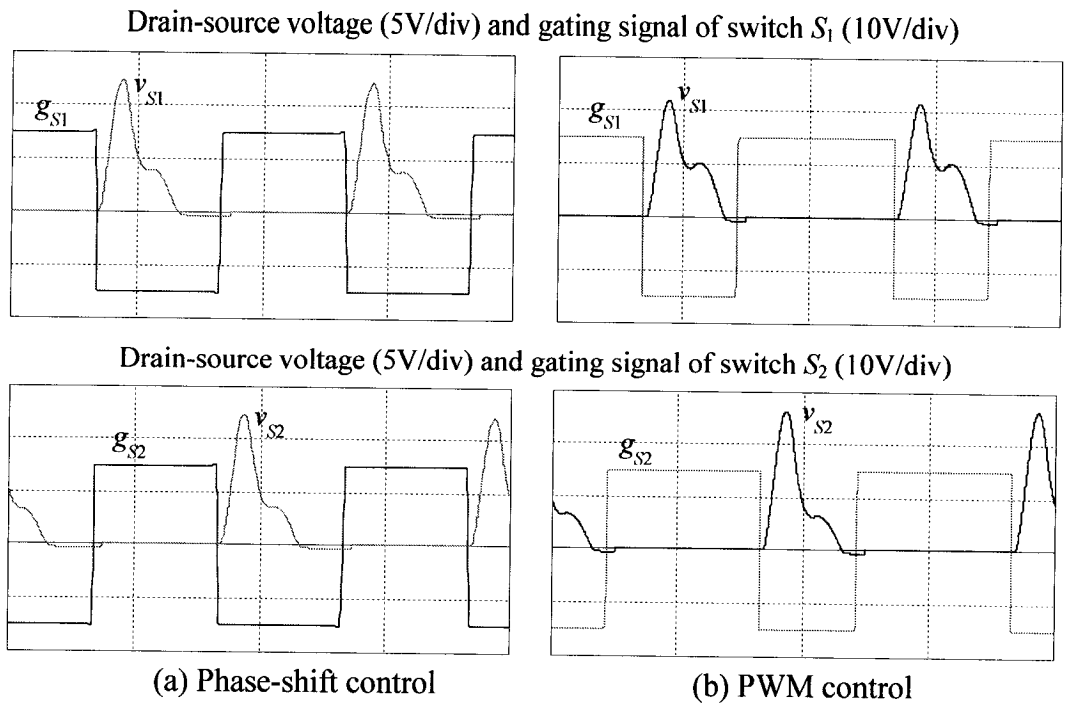


Fig. 3- 51: ZVS operation of the ac switch at 50% load (Horizontal time scale: 0.5μs/div)

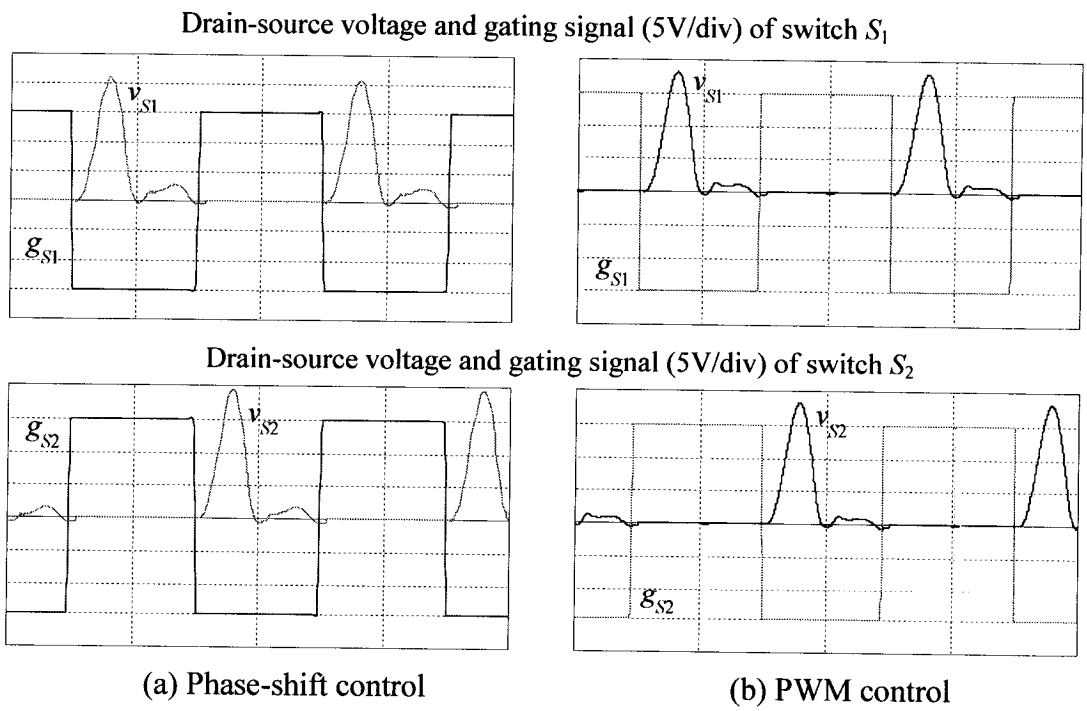


Fig. 3- 52: ZVS operation of the ac switch at 10% load (Horizontal time scale: 0.5μs/div)

3.3.4.2 Operation of zero-voltage-switching

As it is explained in the operating principle, the proposed converter should achieve ZVS at rated load and reduced load as well. The simulation results shown in Fig. 3- 51 and Fig. 3- 52 prove that both control techniques could allow the converter operate with ZVS under all load conditions.

3.3.5 Efficiency

The efficiency of the proposed series resonant converter can be defined as (except control and gate drive losses):

$$\eta = \frac{P_o}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} = 1 - \frac{P_{loss\_1}}{P_{in}} - \frac{P_{loss\_2}}{P_{in}} \tag{3- 71}$$

In (3-71), P_{in} and P_o are the input power and output power of the converter respectively. The losses of the converter, P_{loss}, can be divided into two parts. The first part, P_{loss_1}, is the losses dissipated in the transformer, synchronous rectifier, and the resonant circuit. The control method of the ac switches does not affect this part of losses. The second part, P_{loss_2}, is the losses of the primary side ac switches. Since ac switches operate with soft switching, this part of losses is considered to be only the conduction losses which are determined by the modulation method.

In PWM control, at the rated load, two MOSFETs of the ac switch are both turned on and conducting the input current, and the conduction losses of the switches can be evaluated by (3-72). In phase-shift control, the input current flowing through one MOSFET must flow through the body-diode of another MOSFET due to the complementary gatings, and the conduction losses of the switches can be given by (3-73).

$$P_{loss\_2\_pwm} = 2 \times 1.8 I_r^2 R_{ds(on)} = 0.19W \tag{3- 72}$$

$$P_{loss\_2\_phase} = 1.8I_r^2 R_{ds(on)} + V_{diode} I_r = 0.93W \qquad (3\text{-}73)$$

Where, I_r is the RMS current flowing through the ac switch, and is equal to 1.2 A under the rated load. $R_{ds(on)}$ is the on-state resistance of the MOSFET, and is equal to 0.036 Ω if IRFP150 is used. The factor 1.8 takes into account the thermal effect of $R_{ds(on)}$. V_{diode} is the voltage drop when the body-diode of the MOSFET is conducting, and equals to 0.7V.

Therefore, at the rated load, the efficiency of the PWM controlled converter is expected to be higher than the efficiency of the phase-shift controlled converter by:

$$\Delta\eta = \frac{P_{loss\_2\_phase}}{P_{in}} - \frac{P_{loss\_2\_pwm}}{P_{in}} = \frac{0.93W - 0.19W}{30W} \times 100\% = 2.5\% \qquad (3\text{-}74)$$

At very light load, the gating signals of PWM, as shown in Fig. 3- 2, are almost complementary since intervals III and VI in Fig. 3- 2 when both switches S_1 and S_2 are conducting becomes very short. Consequently, the efficiency of PWM controlled converter becomes similar to the phase-shift controlled converter at very light load.

In a summary, according to the comparison done in this section, it can be concluded that most advantages of the proposed AC VRM can be achieved by using either PWM control or phase-shift control. However, the converter with PWM control is expected to have higher efficiency at and/or close to the rated load.

In the distributed power system, high efficiency is one of the most critical issues required by the high-density on-board converters. Therefore, in the following sections, only pulse-width-modulation is chosen as the control method for the proposed AC VRM.

3.4 DYNAMIC ANALYSIS OF THE PULSE-WIDTH-MODULATED AC VRM

In this section the dynamic characteristics of the pulse-width-modulated AC VRM is analyzed to achieve fast transient response against the load variation. First of all, a circuit diagram of generating the gating signals is described in section 3.4.1. From the description, there is only one control variable to regulate the converter, which is the duty cycle of the PWM signal generated by a voltage feedback loop. Then the feedback loop using a type-II error amplifier is designed based on the dynamic model of the AC VRM derived in section 3.4.2. Finally, the stability and desired transient response are proved by the simulation results presented in section 3.4.3.

3.4.1 Implementation of the Control Circuit

The block diagram of Fig. 3- 53 shows the control circuit to generate the gating signals for the pulse-width-modulated AC VRM. The converter output voltage is fed back through an error amplifier and a pulse-width modulator to generate the PWM signal g_{PWM}. Then this signal is combined with the sign signal of the ac input voltage logically to generate the gating signal for each switch of the ac switch.

The gating signals for the synchronous rectifier are synchronized with the input voltage without any modulation.

Therefore, from control point of view, the duty cycle of the PWM signal is the most important control variable to regulate the output voltage, and the feedback loop design in the next section can determine the dynamic characteristics of the PWM AC VRM.

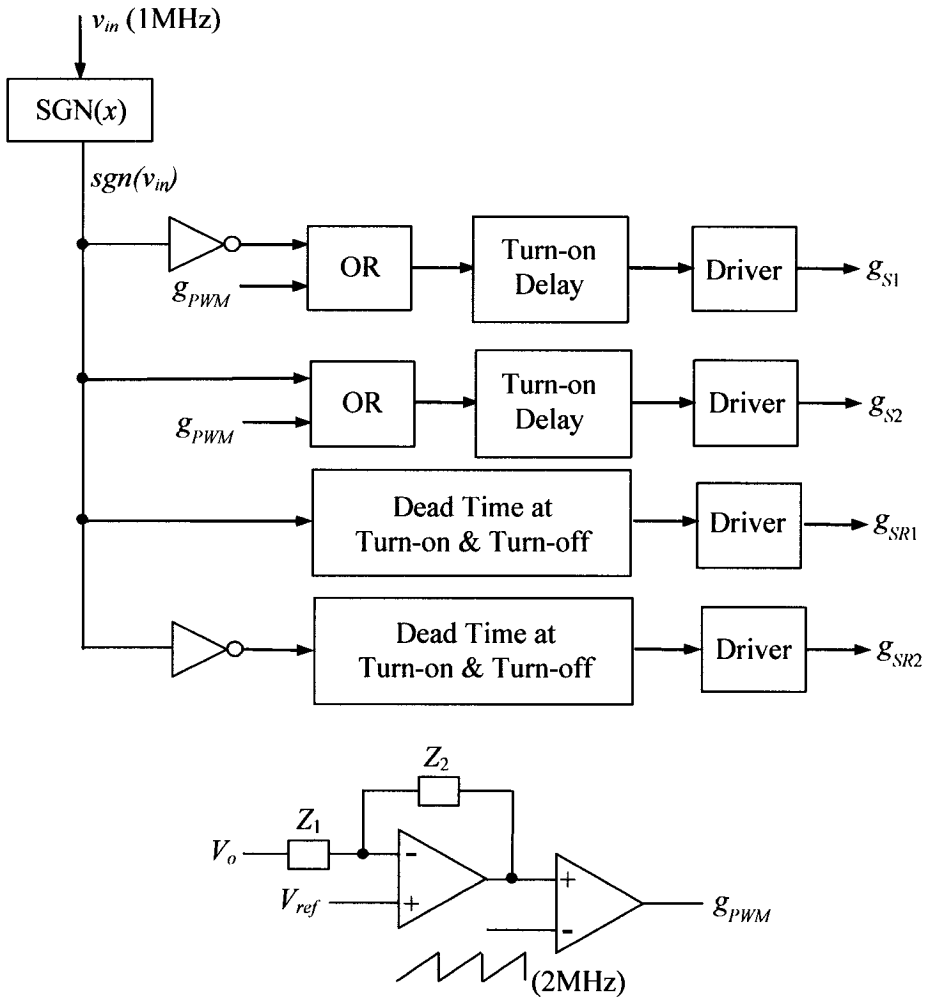


Fig. 3- 53: Gating signal generator of the pulse-width-modulated AC VRM

3.4.2 Feedback Loop Design of the PWM AC VRM

The feedback loop design of the PWM AC VRM is illustrated on the base of the following design example:

Input voltage of the converter: V_{in} = 28 Vrms

Output of the converter: V_o = 1.5 Vdc, P_o = 30 W

Turns ratio of the transformer: N = 20

Circuit parameters: L_s = 2.5 μH, C_s = 10 nF, C_{ds} = 1500 pF, C_o = 500 μF

To reduce the power dissipation on the equivalent series resistance (ESR) of the output capacitor, and to have higher corner frequency (beyond 10 MHz) introduced by ESR and equivalent series inductance (ESL) of C_o, the output capacitor is a capacitor bank which consists of the following capacitors in parallel: (i) 4 capacitors of 100 μF each with a ESR of 1.5 mΩ and an ESL of 1.25 nH, and (ii) 10 capacitors of 10 μF each with a ESR of 0.11 mΩ and an ESL of 0.025 nH. In this case, the ESR and ESL of the output capacitor are ignored in the voltage feedback loop design.

3.4.2.1 Dynamic model of the AC VRM

The power stage of the proposed converter of Fig. 3- 1 including the output filter can be linearized around its steady-state operating point, then the Bode plots can be used to determine the appropriate compensation in the feedback loop for the desired steady-state and transient response. The linearized feedback control circuit is illustrated in Fig. 3- 54. Each block in Fig. 3- 54 can be presented by a transfer function derived as follows.

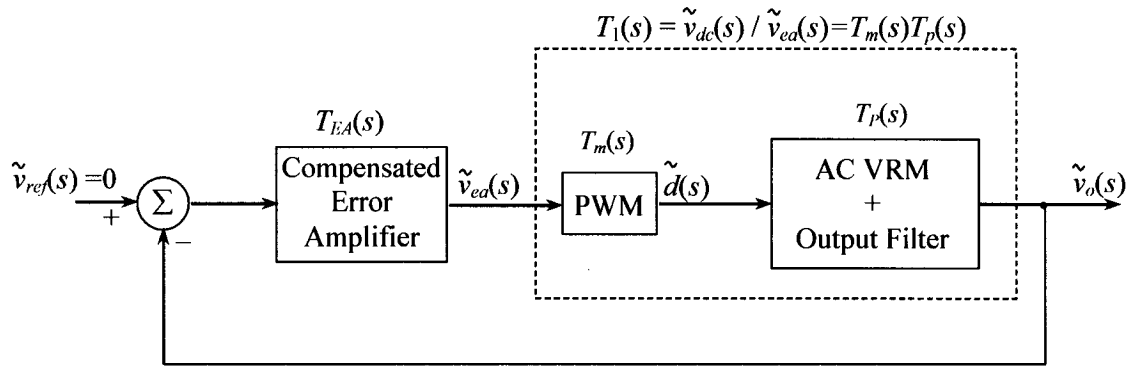


Fig. 3- 54: Linearized feedback control circuit of AC VRM

(1) Transfer function of the power stage $T_p(s)$

To derive the dynamic model of the AC VRM, the equivalent circuit of the proposed converter is drawn in Fig. 3- 55.

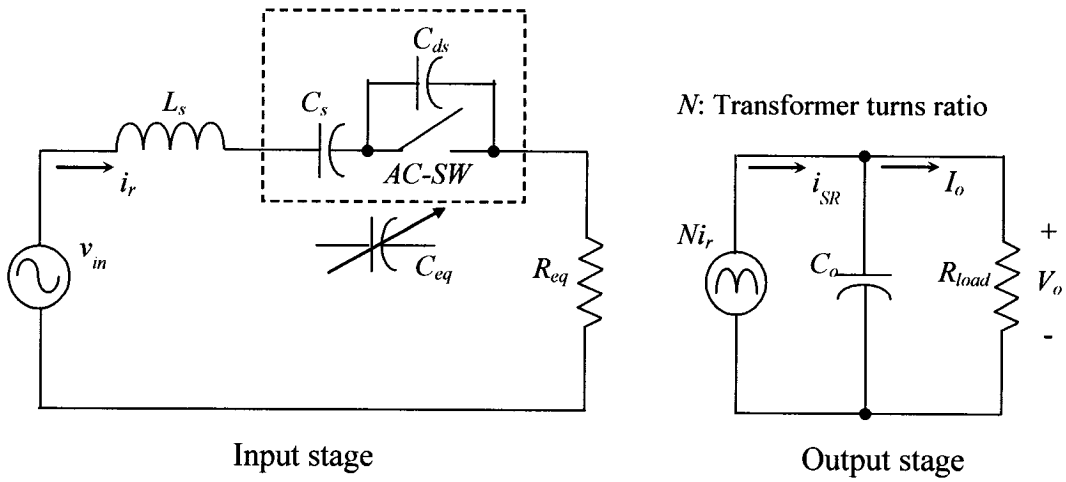


Fig. 3- 55: Equivalent power circuit of the proposed AC VRM

In the output stage of the equivalent circuit, assume that the value of the output capacitor is very high so that all the dc component of the rectifier current (i_{SR}) flows through the output load and the ac component through the capacitor. The output voltage in the steady state can be given as:

$$V_o = I_o R_{load} = \frac{2}{\pi} \hat{I}_{SR} R_{load} \tag{3- 71}$$

Where $\hat{I}_{SR}$ is the peak value of the rectifier current and derived from the input stage of Fig. 3- 55:

$$\hat{I}_{SR} = \frac{N\hat{V}_{in}}{\sqrt{R_{eq}^2 + \left(\omega_o L_s - \frac{1}{\omega_o C_{eq}}\right)^2}} \tag{3- 72}$$

It can be seen that $\hat{I}_{SR}$ is a function of the equivalent resonant capacitance which is a function of duty cycle. Recall (3- 1):

$$C_{eq} = C_s \cdot d + \frac{C_s \cdot C_{ds}}{C_s + C_{ds}} \cdot (1 - d) \tag{3- 73}$$

Assuming for simplicity that the input voltage is a pure sine wave without any disturbance ($\hat{V}_{in}$ is constant), now let the duty cycle be perturbed from its nominal value D to $d(t) = D + \tilde{d}(t)$, where $\tilde{d}(t)$ is assumed to be a small sinusoidal signal of frequency f_n. This will cause a sinusoidal modulation in amplitude of the rectifier current:

$$\hat{I}_{SR}(t) = \hat{I}_{SR} + \tilde{\hat{I}}_{SR}(t) \tag{3- 74}$$

The superscript ~ denotes a perturbation from the nominal value. Correspondingly the output voltage becomes:

$$v_o(t) = V_o + \tilde{v}_o(t) \tag{3- 75}$$

Where V_o is given by (3- 71), and $\tilde{v}_o(t)$ is given in its Laplace transform:

$$\tilde{v}_o = \frac{R_{load}}{1 + sC_oR_{load}} \tilde{\hat{I}}_{SR} \tag{3- 76}$$

Linearizing the item $\tilde{\hat{I}}_{SR}$ by its Taylor series expansion up to linear terms:

$$\tilde{\hat{I}}_{SR} = f'(D) \cdot \tilde{d} \tag{3- 77}$$

The derivative $f'(D)$ in (3- 77) is evaluated at the nominal solution:

$$f'(D) = \left(\frac{\partial \hat{I}_{SR}}{\partial C_{eq}} \cdot \frac{\partial C_{eq}}{\partial d} \right)\Bigg|_{d=D} \tag{3- 78}$$

The partial derivatives in (3- 78) are obtained from equations (3- 72) and (3- 73) respectively:

$$\frac{\partial \hat{I}_{SR}}{\partial C_{eq}} = -N\hat{V}_{in} \frac{\omega_o L_s - 1/(\omega_o C_{eq})}{\omega_o C_{eq}^2 \left[R_{eq}^2 + (\omega_o L_s - 1/(\omega_o C_{eq}))^2 \right]^{3/2}} \tag{3- 79}$$

$$\frac{\partial C_{eq}}{\partial d} = C_s - \frac{C_s \cdot C_{ds}}{C_s + C_{ds}} = K_c \tag{3- 80}$$

Thus the transfer function of the power stage including the output filter, which is the dynamic model of the proposed converter, can be found by:

$$T_p(s)=\frac{\tilde{v}_o}{\tilde{d}}=\frac{R_{load}}{1+sC_oR_{load}}\frac{-N\hat{V}_{in}\left[\omega_oL_s-1/(\omega_oC_{eq})\right]}{\omega_oC_{eq}^2\left[R_{eq}^2+(\omega_oL_s-1/(\omega_oC_{eq}))^2\right]^{3/2}}K_c \qquad (3\text{-}81)$$

(2) Transfer function of the direct duty cycle pulse-width modulator $T_m(s)$

The theoretical transfer function $T_m(s)$ is simply given by (3- 82) [25] without any time delays:

$$T_m(s)=\frac{\tilde{d}(s)}{\tilde{v}_{ea}(s)}=\frac{1}{\hat{V}_r} \qquad (3\text{-}82)$$

Where $\hat{V}_r$ is the peak value of the repetitive saw-tooth waveform (also named carrier wave) at the input of the pulse-width modulator.

However, the time delay associated with the comparator can lead to a delay in the real modulator response.

Finally, the control-to-output transfer function $T_1(s)=T_p(s)T_m(s)$ can be obtained by (3- 81) and (3- 82), and its Bode plot is illustrated in Fig. 3- 56.

3.4.2.2 Design of an error amplifier

Based on the dynamic model of the AC VRM, an error amplifier is designed to provide desired compensation to achieve overall stability and good transient response.

To avoid large–amplitude switching frequency ripple at the dc output under all load conditions, the crossover frequency of the total open-loop gain is chosen at 150 kHz, and the error amplifier is designed under the load condition around 50% load.

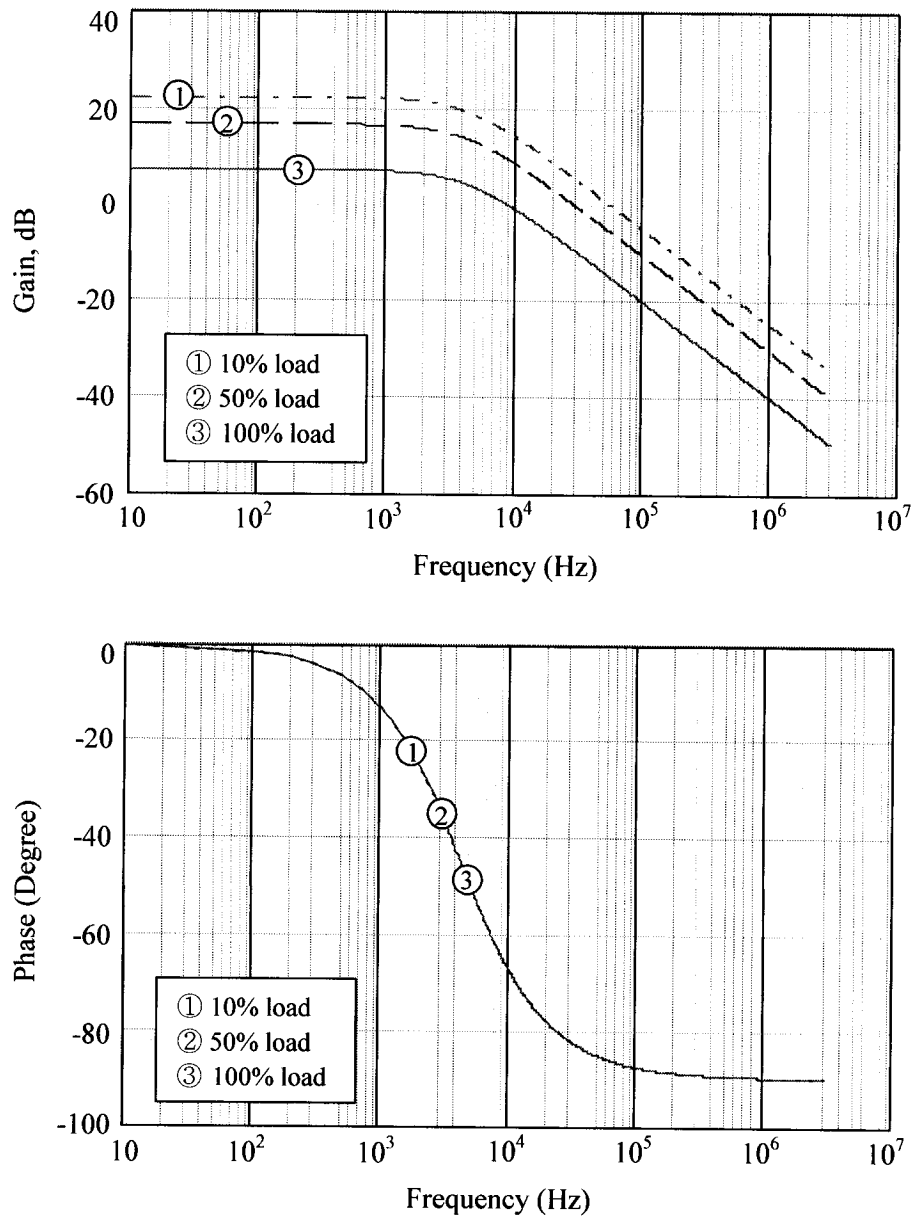
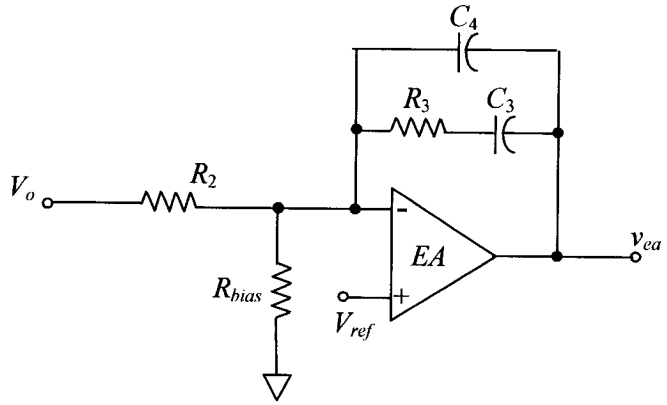
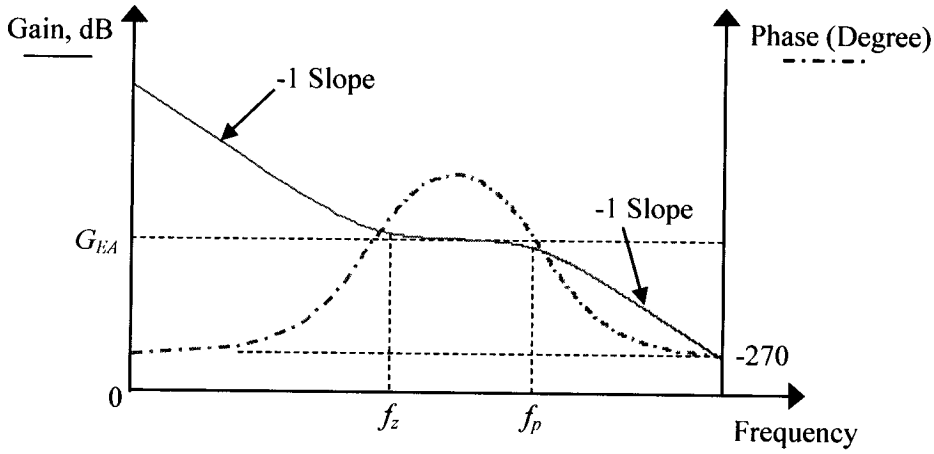


Fig. 3- 56: Bode plot of the control-to-output transfer function

According to the Bode plot of the control-to-output transfer function of the converter shown in Fig. 3- 56, a type-II error amplifier (its circuit diagram and Bode plot are shown in Fig. 3- 57) could shape the total open loop frequency characteristics to have a -1 gain slope and the desired phase margin (between 40° to 60°) at the crossover frequency.



(a) Circuit diagram



(b) Bode plot

Fig. 3- 57: Type-II error amplifier

In the design of a type-II error amplifier, the amplifier gain and the K factor are the most important factors to be determined.

(1) Amplifier gain

The amplifier gain of the type-II amplifier, G_{EA}, is equal to the gain loss of the control-to-output gain at the crossover frequency. From the Bode plot of Fig. 3- 56, G_{EA} = 14 dB (or 5.0 in numerical) in this design.

(2) K Factor

K factor is given by:

$$K = \tan\left(\frac{M - P - 90^\circ}{2} + 45^\circ\right) \tag{3- 83}$$

Where M is the desired phase-margin of 60° to yield well-damped load transient response. P is the phase shift of the control-to-output transfer function which is -90° in Fig. 3- 56. Therefore, $K = 4$ in this design.

(3) Calculate the circuit parameters of the error amplifier:

The type-II error amplifier has a zero at frequency F_z ($F_z = F_{co} / K = 37.5$ kHz), and a pole at frequency F_p ($F_p = K \cdot F_{co} = 600$ kHz). Its transfer function is given by:

$$T_{EA}(s) = \frac{1 + sR_3C_3}{sR_2(C_3 + C_4)(1 + sR_3C_4)} \tag{3- 84}$$

If R_2 is arbitrarily taken as 1 kΩ, the parameters in (3- 84) are found out as:

$$R_3 = G_{EA}R_2 = 5.0 \quad k\Omega \tag{3- 85}$$

$$C_3 = \frac{1}{2\pi F_z R_3} = 850 \quad pF \tag{3- 86}$$

$$C_4 = \frac{1}{2\pi F_p R_3} = 53 \quad pF \tag{3- 87}$$

The Bode plots of the designed type-II error amplifier and the overall loop are shown in Fig. 3- 58.

It can be seen that the control loop satisfies the stability criteria:

(i) The slope of the overall loop gain at the crossover frequency is –20 dB;

(ii) The phase margin between 56° to 63° under all load conditions is safe to yield well-damped large load transient response.

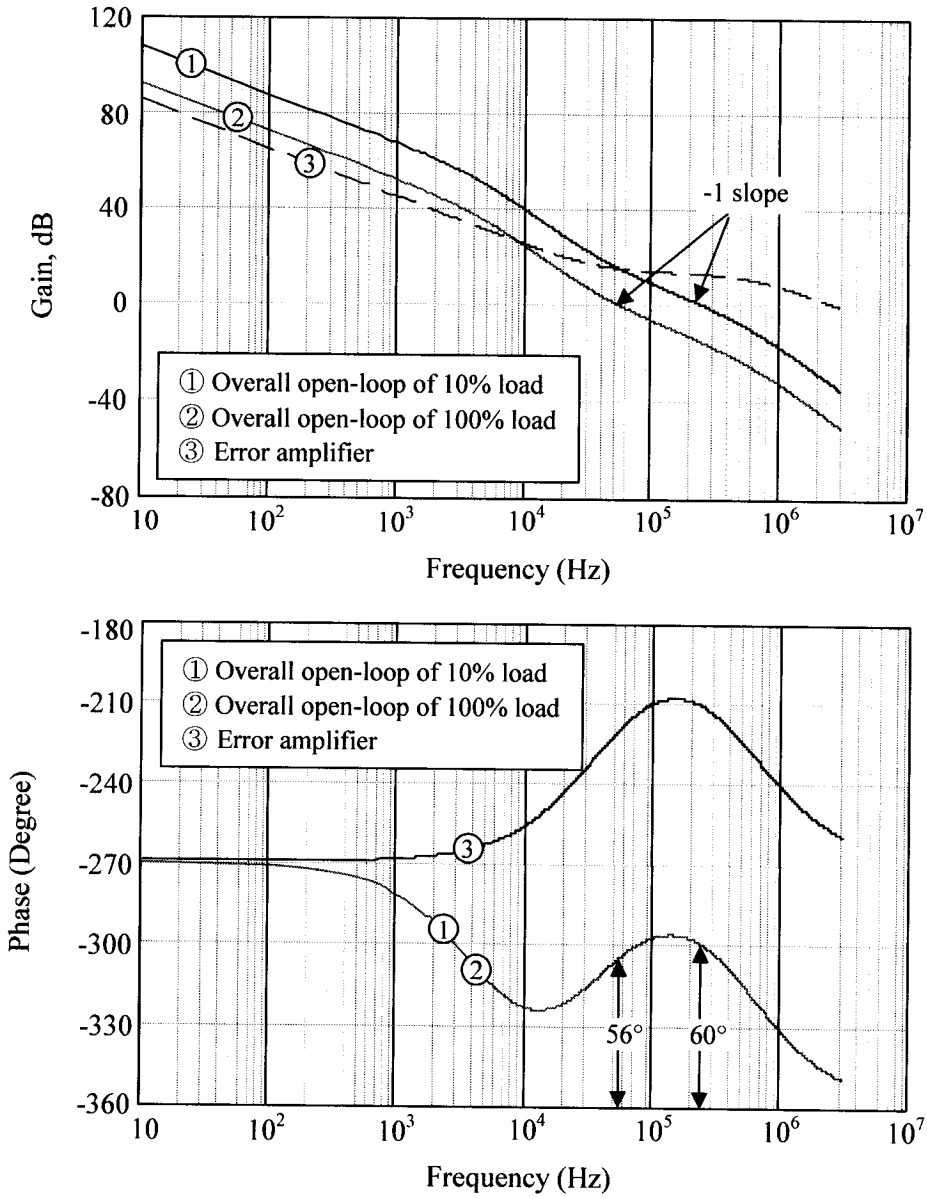


Fig. 3- 58: Bode plot of the type-II error amplifier and the overall loop

3.4.3 Dynamic Performance of the PWM AC VRM

The designed type-II error amplifier is employed in the proposed PWM AC VRM, and the closed-loop stability and load transient response are examed by using the simulation tool Pspice. The simulation circuit has the same circuit parameters as those used in the feedback loop design, and is shown in Appendix D.

The load transients caused by the power management of the processor board are normally with very high slew rate. In the simulation, the step change is applied to the output load current at the slew rate di / dt = 1000 A/μs. The simulation results are shown in Fig. 3- 59 and Fig. 3- 60, presenting the dramatic load transients occurring in the processor transient from the sleep mode (2A, 10% load) to the active mode (20A, 100% load) and vice versa.

Fig. 3- 59 shows the deviation of the output voltage when the output load current is changed from 10% load to full load. The large undershoot spike of 170 mV is caused by ESRs and ESLs of the output capacitor bank. This spike can be limited by some decoupling capacitors with very low ESLs in the real circuit. The slower undershoot portion following the spike is about 45 mV (3% of the nominal value). This is because the resonant inductor becomes virtually an open circuit at such high slew-rate (di/dt), and only the output capacitor provides the total load current. The whole recovery time during such a large step load transient is about 10 to 15 μs.

Fig. 3- 60 shows the deviation of the output voltage when the output load current is changed from full load to 10% load. Similarly, the output voltage has initial overshoot and undershoot spikes about 1V. The slower overshoot portion following the spike is about 45 mV (3% of the nominal value). The whole recovery time during such a large step load transient is about 25 μs.

The simulation results show that the compensated AC VRM is stable during the very large load transients. The output voltage deviation is limited within 3% against the large load current transient with a very high slew-rate (di/dt).

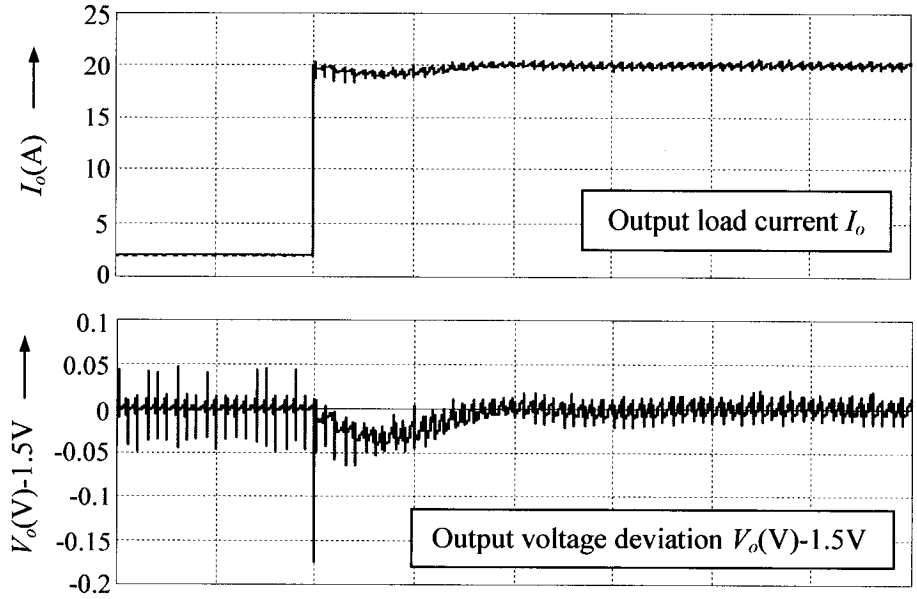


Fig. 3- 59: Transient response of VRM when output changes from 10% to full load

(Horizontal time scale: 5μs/div)

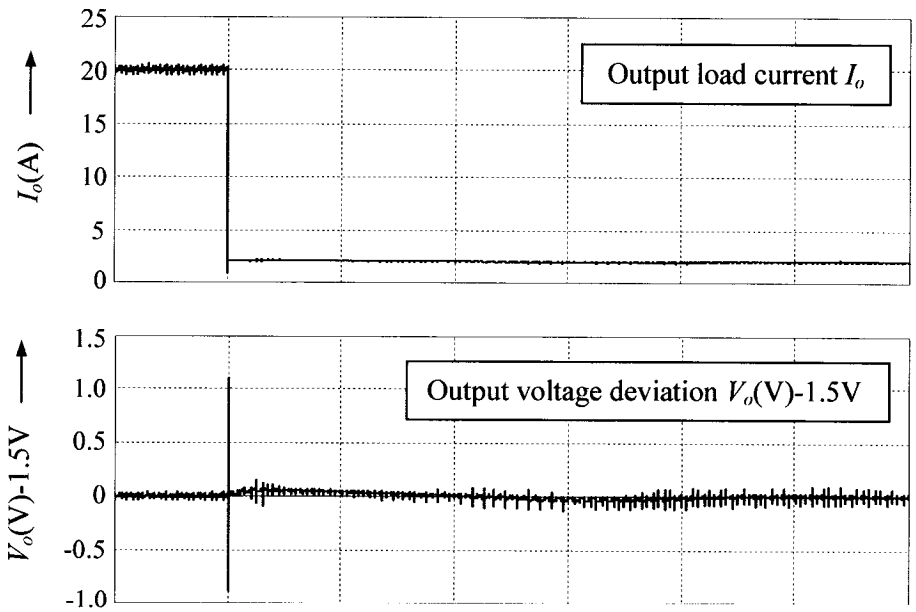


Fig. 3- 60: Transient response of VRM when output changes from full load to 10% load

(Horizontal time scale: 10μs/div)

3.5 PERFORMANCE OF THE PULSE-WIDTH-MODULATED AC VRM – SIMULATION AND EXPERIMENTAL VERIFICATION

In this section, simulation and experimental results are presented to verify the theoretical steady-state and dynamic analyses made in this chapter.

Fig. 3- 61 shows the prototype PWM AC VRM. It is built to operate at 1 MHz under a sinusoidal input voltage of 28 Vrms, and the output voltage is 1.5 Vdc with a rated load of 30 W. The principle parameters of the simulation circuit and the experimental setup are shown in Table 3-2 and Table 3-3 respectively.

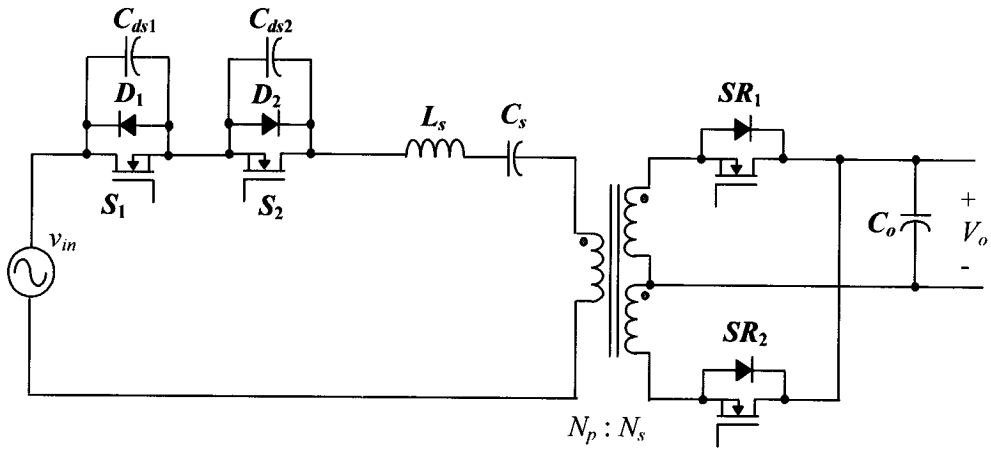


Fig. 3- 61: The prototype inverter of the proposed APWM resonant inverter

Table 3-2: Principle parameters of the simulation circuit

Resonant Components	L_s = 2.5 μH, C_s = 10 nF	
Output capacitor	C_o = 500 μF (Four 100μF capacitor with ESR=1.5mΩ and ESL=1.25nH and ten 10μF capacitor with ESR=0.11mΩ and ESL=0.025nH in parallel	
Transformer	$N_p : N_s$ = 20	
Switches	S_1 & S_2: IRFP150	SR_1 & SR_2: 4 IRL3803 in parallel

Table 3-3: Principle parameters of the experimental setup

Components	Values		Selections
L_s	2.5 μH		*Magnetics 55381-A2*
C_s	10 nF		*Vima FKP*
C_o	500 μF	Four 100μF with ESR=1.5mΩ and ESL=1.25nH	*TDK X7R*
		ten 10μF with ESR= 0.11mΩ and ESL=0.025nH	*TDK X7R*
Transformer	$N_p : N_s$ =19.8 , L_m=85 μH		*TDK PC5 0EPC17*
S_1 & S_2	IRFP150		Appendix E
SR_1 & SR_2	Two IRF 7822 in parallel		Appendix E

3.5.1 Simulation Results

The simulation is carried out by using the simulation tool PSpice. The PSpice model of the proposed PWM AC VRM is shown in Appendix D.

Previously, the simulation results of the converter steady-state waveforms have been presented in Fig. 3- 13 in section 3.1.3 for the verification of the theoretical waveforms, and in Fig. 3- 47 to Fig. 3- 49 in section 3.3.4 under different load conditions. These figures show a good agreement with the theoretical predictions.

The simulation results of zero-voltage-switching under different load conditions are presented in Fig. 3- 50 and Fig. 3- 51 in section 3.3.4.

Simulation results of Fig. 3- 59 and Fig. 3- 60 in section 3.4.3 show that the PWM AC VRM with well-designed control loop is stable and has fast response under the large signal transients with very high slew rate di/dt in the load current.

3.5.2 Experimental Results

3.5.2.1 Steady-state characteristics

The experimental waveforms of the input voltage, input current and voltage across the ac switch under different load conditions are shown in Fig. 3- 62. The output voltage ripple (4.48 mV, peak-to-peak) at full load is shown in Fig. 3- 63.

Some important steady-state characteristics are compared quantitatively in Table 3-4 between the experiment, simulation and theoretical prediction.

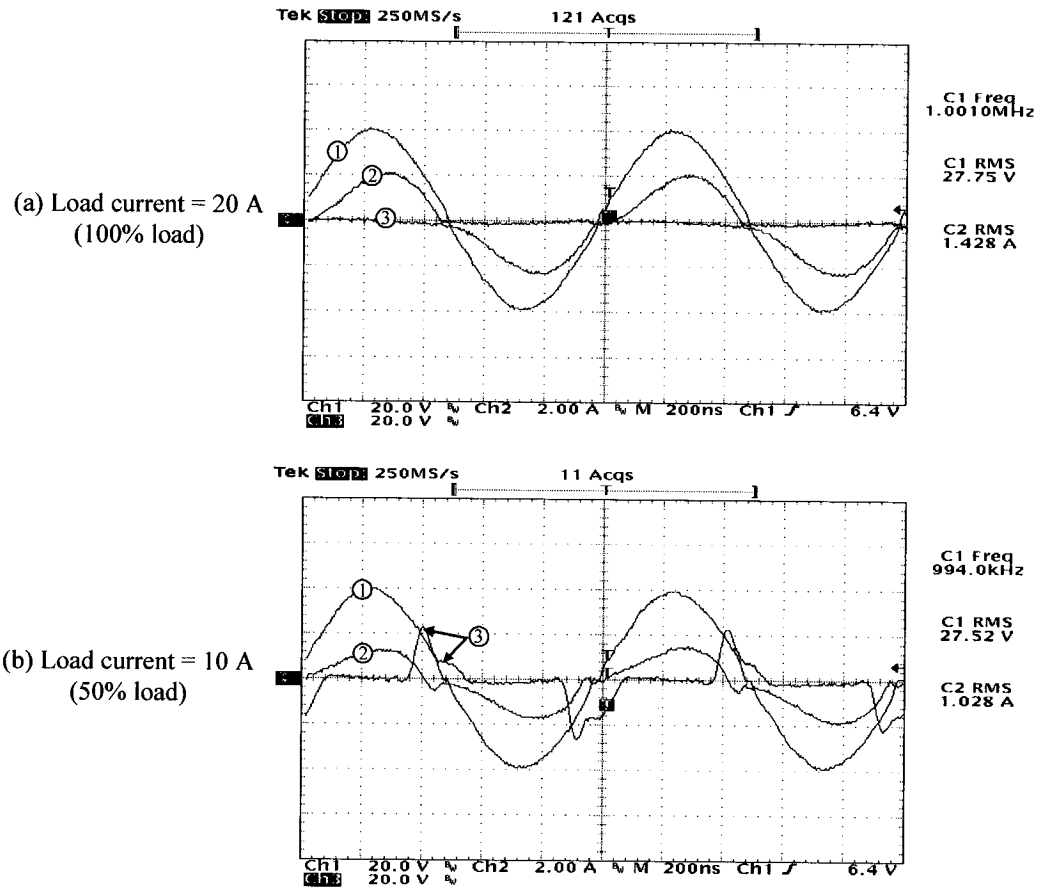


Fig. 3- 62: Main steady-state experimental waveforms (Time: 0.2μs/div)

(Trace ①: Input voltage (20V/div), Trace ②: Input current (2A/div),

Trace ③: Voltage across the ac switch (20V/div))

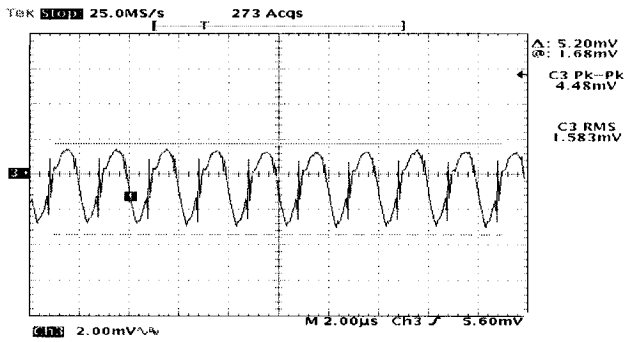


Fig. 3- 63: Experimental waveform of the output voltage ripple at full load

Table 3-4: Comparison of theoretical, simulation, and experimental steady-state characteristics

Comparison		Duty Cycle	Input current			ac switch peak voltage
			RMS	THD	PF	
100% Load	Theoretical	1.0	1.22A	18%	0.97	0.7V
	Simulation	0.9	1.25A	20%	0.97	0.7V
	Experimental	0.9	1.25A	20%	0.97	0.7V
50% Load	Theoretical	0.6	0.65A	35%	0.92	13V
	Simulation	0.67	0.69A	38%	0.90	13V
	Experimental	0.65	0.68A	43%	0.89	22V
10% Load	Theoretical	0.1	0.31A	192%	0.45	20V
	Simulation	0.44	0.32A	185%	0.43	20V
	Experimental	0.4	0.31A	187%	0.44	34V

Table 3-4 shows that the theoretical, simulation, and experimental steady-state properties have a good agreement on the characteristics of the input resonant current. However, in terms of the duty cycle of the PWM signal and the peak voltage across the

ac switch, good agreements are achieved under certain load conditions. These observations can be explained as follows.

(i) Duty cycle.

In the theoretical steady-state analysis, it is assumed that the on-duration of the ac switch equals the pulse-width of the PWM signal. This assumption is valid for a wide range of load conditions. However, at light load (lower than 30% of the full load), the actual operation of the ac switch has smaller on-duration than the pulse-width of the PWM signal. This fact increases the duty cycle in the actual operation dramatically in order to transfer the same amount of power compared to the theoretical analysis.

In addition, the simulation and experimental duty cycle at rated load less than one, which is the theoretical value, can provide maximum modulation during the large transients from light load to full load so that the transient recovery can be fast.

(ii) The voltage stress across ac switch.

In the theoretical analysis, drain-source capacitance C_{ds} is assumed to be a constant external capacitance (C_{ds} = 1500 pF) across an ideal switch. In the simulation, the model of a MOSFET switch has also a constant C_{ds}. However, in the actual operation, C_{ds} of the switch decreases when the drain-to-source voltage v_{ds} increases [25], as shown in Fig. 3- 64 (detailed data are referred to Appendix E).

In Fig. 3- 64(a), C_{ds} is a series combination of gate-drain capacitance C_{gd} and gate-source capacitance C_{gs}. Capacitance C_{gs} can be assumed constant. The most significant change in capacitance occurs in C_{gd} because the voltage change across it ($v_{dg} \approx v_{ds}$) is much larger than the voltage change across C_{gs}. Capacitance C_{gd} decreases when

v_{ds} increases at small duty cycle. The change in C_{gd} can be as large as a factor of 10 to 100 in Fig. 3- 64(b).

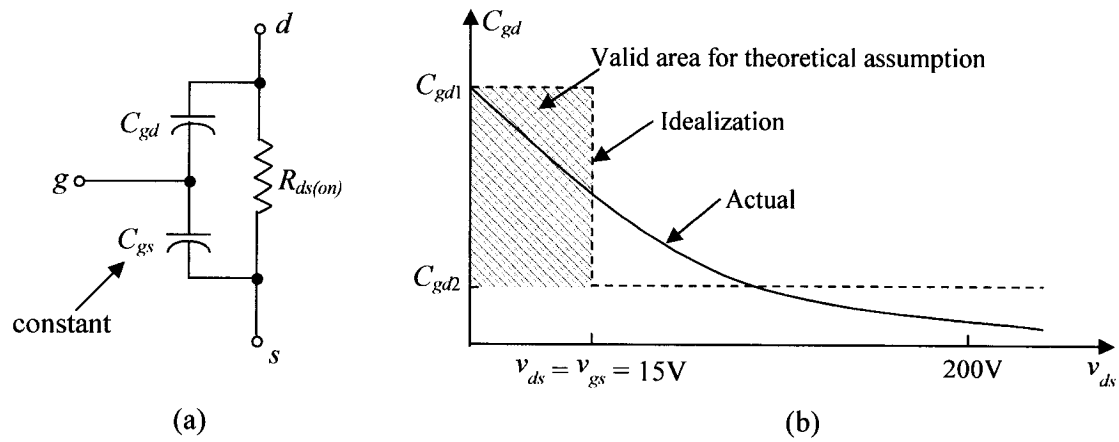


Fig. 3- 64: Circuit model and parameters for MOSFETs: (a) MOSFET equivalent circuit; (b) Variation in gate-drain capacitance with drain-source voltage.

For the proposed PWM AC VRM, the ac switch is composed of MOSFET IRFP150. C_{ds} = 1500 pF is its drain--source capacitance when its v_{ds} is around 7V. In Table 3-4, the theoretical and simulation results show that the peak voltage across the ac switch reaches 14V under 50% load condition. In this case, C_{ds} should be less than 1500 pF, and thereby increasing the voltage stress of the switch further, as shown in the experimental result. The same explanation can be applied to Table 3-4 under light load condition (10% of full load).

(iii) Input resonant current.

The assumption of constant value of C_{ds} in the theoretical analysis and simulation also introduces an error in calculating the impedance of the equivalent series resonant branch:

$$\Delta Z_s = \left|\omega_o L_s - \frac{1}{\omega_o C_{eq,real}}\right| - \left|\omega_o L_s - \frac{1}{\omega_o C_{eq,ideal}}\right| \qquad (3\text{-}88)$$

Where, $C_{eq,ideal}$ is the assumed constant value, and $C_{eq,real}$ is the real value of the equivalent series resonant capacitance.

This error of the impedance (ΔZ_s) increases when the load decreases. However, compared to the parallel impedance Z_p of the magnetizing inductance and the equivalent load resistance R_{eq} (referred to Fig. 3-6), error ΔZ_s is much less. At 10% load, for example, ΔZ_s is about 10Ω, and Z_p is about 90Ω. Therefore, this error has little contribution on calculating the input current.

This is the reason why the theoretical, simulation, and experimental results have a good agreement on the characteristics of the input resonant current under all load conditions in Table 3-4.

3.5.2.2 Zero-voltage-switching

ZVS operation of the proposed converter is proved under all load conditions. Fig. 3- 65 shows the switching characteristic waveforms of switch S_1 from full load to light load. It can be seen that at 12% load, although the switch voltage is distorted due to the highly distorted input current, ZVS operation is still maintained. The same ZVS operation can also be achieved by switch S_2.

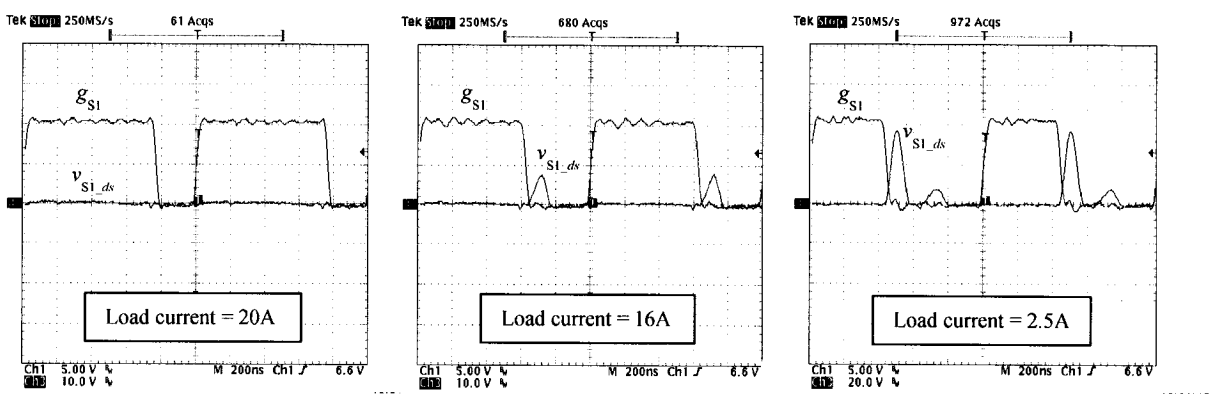


Fig. 3- 65: Experimental results of ZVS operation

3.5.2.3 Large load transients

The transient response of the proposed AC VRM against the load variation (from 0 A to 20 A and vice versa) is shown in Fig. 3- 66. The step change is applied to the output load at the slew rate (di/dt) of 1000 A/μs. When the output is changed from no-load to full-load, the output voltage drops about 3% and takes around 30 μs to get steady state. When the output is changed from full-load to no-load, the output voltage only takes 20 μs to be stable again. Compared to the simulation results, the initial spikes in the output voltage during the transients are much reduced because of the decoupling capacitors.

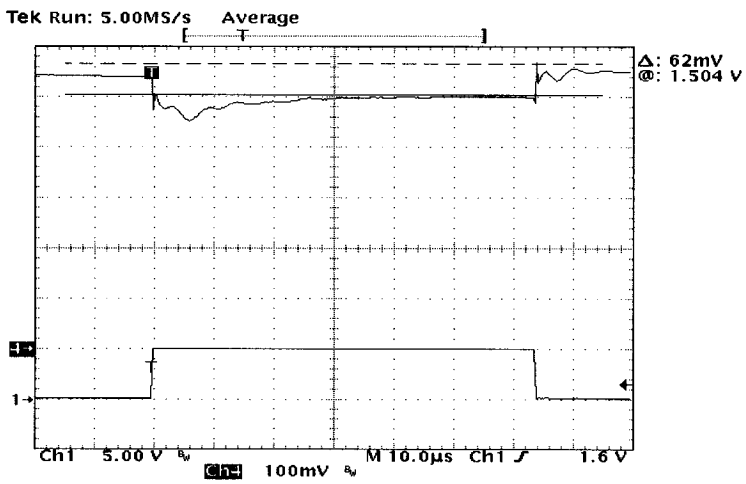


Fig. 3- 66: Transient response of the proposed AC VRM against the load variation

3.5.2.4 Efficiency

The proposed AC VRM's overall efficiency is shown in Fig. 3- 67. This figure shows that the efficiency of the converter is almost constant between 85% to 87% when the load decreases from 100% to about 50% of the full load. This constant high efficiency is benefited from the soft switching of all the switches employed in the converter, and the

major losses, which are the conduction losses, decrease when the load decreases. However, when the load decreases further, the losses in the control and drive circuit become significant and cause the efficiency to decrease.

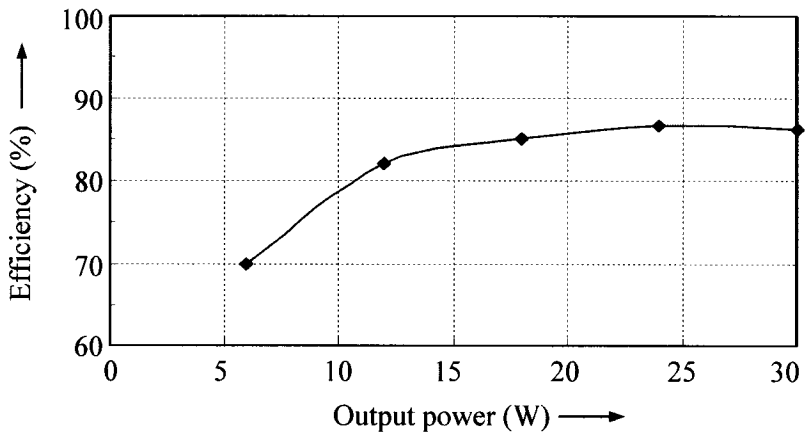


Fig. 3- 67: Efficiency of the PWM AC VRM vs. output power

3.6 SUMMARY

In this chapter, a series resonant converter has been proposed as the AC VRM in the HFAC distributed power system applications. This topology uses (i) an ac switch as a switch-controlled capacitor and a series resonant tank at the primary side to change the resonant frequency, (ii) a synchronous rectifier at the secondary side to reduce the conduction losses in the rectification, and (iii) a capacitor as the output filter to smooth the output voltage and achieve much faster transient response than any low-pass LC filter.

The ac switch can be controlled by either the pulse-width-modulation or the phase-shift-modulation so that the equivalent resonant frequency of the converter can be changed, and therefore the output voltage regulation can be achieved.

The steady-state and dynamic characteristics of the converter have been analyzed and verified with simulation and experimental results. They can be concluded as:

(i) Very tight voltage regulation at the output (1% ripple, and 3% during transient);

(ii) Close-to-unity rated power factor and low total harmonic distortion in the input current;

(iii) Guaranteed zero-voltage switching under all load conditions;

(iv) Low voltage stress of the active switches;

(v) Fast response against large load transient with very high slew rate (di/dt);

(vi) High overall efficiency;

(vii) Inherent current limit due to the resonant circuit employed in the converter.

All these features of the proposed AC VRM can be achieved by either PWM control or phase-shift control. However, the converter with PWM control is expected to have 3% higher efficiency at and/or close to the rated load. Therefore, PWM control is chosen as the optimum control technique for the proposed AC VRM.

The design procedure of the proposed pulse-width-modulated AC VRM to be employed in the HFAC distributed power system is shown in Chapter 4, and furthermore, the system performance will be investigated in Chapter 5.

CHAPTER 4

DESIGN, IMPLEMENTATION AND PERFORMANCE OF HFAC DISTRIBUTED POWER SYSTEM

4.0 INTRODUCTION

To overcome the drawbacks of the existing DC distributed power system for the desktop computer, Chapter 1 presented the concept of the alternative high frequency AC distributed power system (HFAC DPS) architecture. In this architecture, the functional blocks to convert low frequency ac line input into low regulated dc voltage to power the load are shown in Fig. 4- 1.

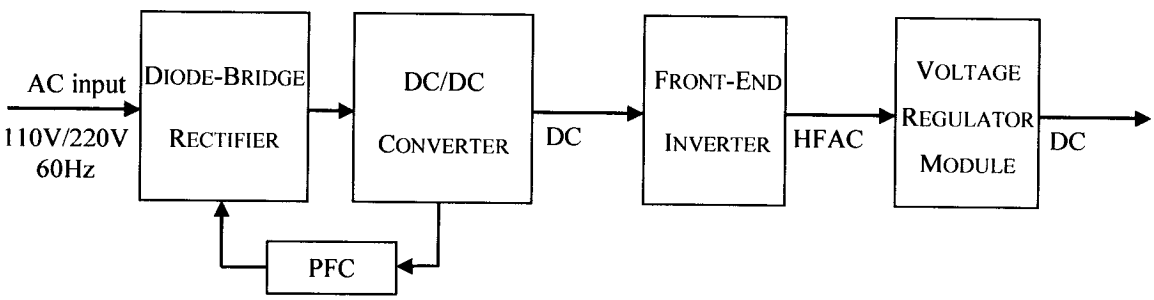


Fig. 4- 1: Block diagram of the power conversion stages of the HFAC DPS

In Fig. 4- 1, a diode bridge rectifier converts the ac input voltage into an unregulated dc voltage. Then a dc/dc converter is used to regulate this dc voltage and perform power factor correction (PFC) at the same time to improve the harmonic distortion of the input line current. A sinusoidal bus voltage is generated by a front-end inverter to be distributed on the motherboard, and on the local board, an AC VRM converts the ac bus voltage to the specific dc voltage to power the load, such as microprocessors, I/Os and memories of the desktop computer.

Since the rectification stage with PFC is technically mature, this chapter will focus on the design, implementation and performance of the system as related to the last two conversion blocks – front-end inverter and AC VRM.

This chapter firstly presents the issues of system design. The design requirements of HFAC DPS are specified, and design examples are presented to illustrate the design procedures of the front-end inverter and AC VRM individually.

Well designed front-end inverter and AC VRM are employed in the HFAC DPS, detailed system implementation and operating principles are presented. Finally, the system performance in the steady state and under the large transient signals, in both input voltage and output load, are investigated.

The outline of this chapter is as follows.

The first part of this chapter is the system design. In section 4.1, the design considerations of HFAC DPS are given. In section 4.2, the design of the APWM resonant inverter used as a front-end inverter is presented by a design example of 200 W inverter operating at 1 MHz. In section 4.3, the design of the PWM series resonant converter used as an AC VRM is illustrated by a design example of 30 W converter operating at 1 MHz.

The second part of this chapter is the system implementation. The conceptual and detailed implementation of the HFAC DPS is presented in section 4.4, and the system operating principles are discussed in section 4.5.

The third part of this chapter is the system performance. In section 4.6, the system steady-state performance in different operating mode is presented. In section 4.7, the system dynamic performance against input voltage and load variations is investigated.

Finally some conclusions of the HFAC DPS are summarized in section 4.8.

4.1 DESIGN CONSIDERATIONS OF THE HFAC DISTRIBUTED POWER SYSTEM

In general, the following factors have to be taken into account in the design of the HFAC distributed power system:

(i) The system should be capable of operating within the limits of the voltage and current ratings of the system components;

(ii) The system should be capable of delivering the required power to the output under various line and load conditions;

(iii) The system should have high overall efficiency from low-load to full-load;

(iv) The system should be self protecting under the various fault conditions;

(v) The system should have low electromagnetic interference (EMI).

Furthermore, a good design of a HFAC distributed power system involves a number of trade-offs and choices related to the selection of the distribution bus, optimization of the front-end inverter and on-board load VRMs, and integration of the system. These factors can be described as follows.

4.1.1 Bus Voltage Selection

Selection of the bus characteristics is an important step in the system design because it affects all power system components. The major considerations in the selection of the ac bus are:

(i) Power level

To minimize the distribution losses, the bus voltage should be sufficiently high to reduce the distribution current. However, the voltage level must be limited within the safety-defined level of 30V RMS [72]. Bus voltage of 28 (±5%) V RMS is selected.

(ii) Bus frequency

In general, the ac bus frequency could be in the range of 20 KHz to 2 MHz. For the application of the desktop computer, high bus frequency over 500 KHz is preferred due to the advantages of miniaturization and fast transient response. Bus frequency of 1 MHz is selected in this design based on the following considerations:

(a) The bus frequency is limited by the switching speed of the MOSFET. The operating frequency of the MOSFETs employed in the front-end inverter and AC VRMs is the same as the bus frequency. The switching delays (turn-on delay time + rise time + turn-off delay time + fall time) are usually in the range of 150 – 200 ns. These delays limit the maximum modulated duty cycle of the switches at very high operating frequency, thus limiting the ability of power transfer and the speed of transient response.

(b) At very high frequencies, the special bus cabling increases the cost and complexity, and the skin-effect increases the bus resistance and thereby the distribution losses.

(c) The speed of the converter transient response cannot be proportional to the bus frequency without any limit. In fact, it is limited by the compensation components in the control loop and the switching speed of the MOSFETs employed in the converters.

(iii) Bus voltage waveform shape

There are mainly two choices – sinusoidal wave and trapezoidal wave. As shown in Appendix F, the inverter with trapezoidal output is a half-bridge circuit, and two switches operate at fixed duty cycle close to 50%. This inverter can provide controlled

rising and falling edges of the output voltage waveform resulting in significantly reduced EMI. However, the output voltage of this inverter cannot be controlled, but highly depends on its input voltage which is the regulated output voltage of the dc/dc converter in Fig. 4- 1. In this design, sinusoidal wave is selected due to its very low EMI and easy implementation of its power and output control circuits.

4.1.2 Front-End Inverter

The front-end inverter, which is also named as system power supply, should be designed to have the following features:

(i) Very low total harmonic distortion at the rated output under all line conditions (less than 2% is specified in this design);

(ii) Zero-voltage-switching under all line and load conditions to achieve high efficiency;

(iii) Fast transient response.

The APWM resonant inverter developed and analyzed in Chapter 2 can meet all the general requirements for the system and all the features of the front-end inverter. In section 4.2, the detailed design steps are illustrated based on the equations and performance curves derived in Chapter 2.

4.1.3 On-Board AC VRMs

The main design objectives for the on-board load AC VRM can be concluded as:

(i) High efficiency (zero-voltage-switching and low conduction losses);

(ii) Close-to-unity power factor and low total harmonic distortion of the input current;

(iii) Fast transient response and very tight output voltage regulation;

(iv) Low mass and volume.

The PWM series resonant converter developed and analyzed in Chapter 3 can meet all the general requirements for the system and all the design objectives of the AC VRM. In section 4.3, the detailed design steps are illustrated based on the equations and performance curves derived in Chapter 3.

4.1.4 System Integration and Dynamic Interactions

The system integration techniques can improve the electrical performance and power density. The potential sources of the dynamic interactions in a distributed power system are related to paralleling and cascading of converter modules. EMI filters and de-coupling capacitors are required to reduce the problems related to the dynamic interactions. These issues are also primary concerns associated with the application of the HFAC distributed power system. However, it is out of the scope of this thesis and is not discussed in detail.

4.2 Design of the Front-End Inverter – APWM Resonant Inverter

In this section, the design of APWM resonant inverter of Fig. 4- 2 is illustrated by a design example. Section 4.2.1 gives the specifications on which the design is based. Section 4.2.2 gives the base quantities used in the design. Section 4.2.3 presents the selection of principle components and parameters, including the input filter (L_f and C_f), chopper circuit (switches and snubber capacitors), series-parallel resonant tank (L_s, C_s, L_p, C_p), 2nd harmonic trap (L_2 and C_2), and the output transformer. The performance curves and equations derived in Chapter 2 are used to develop the design procedure.

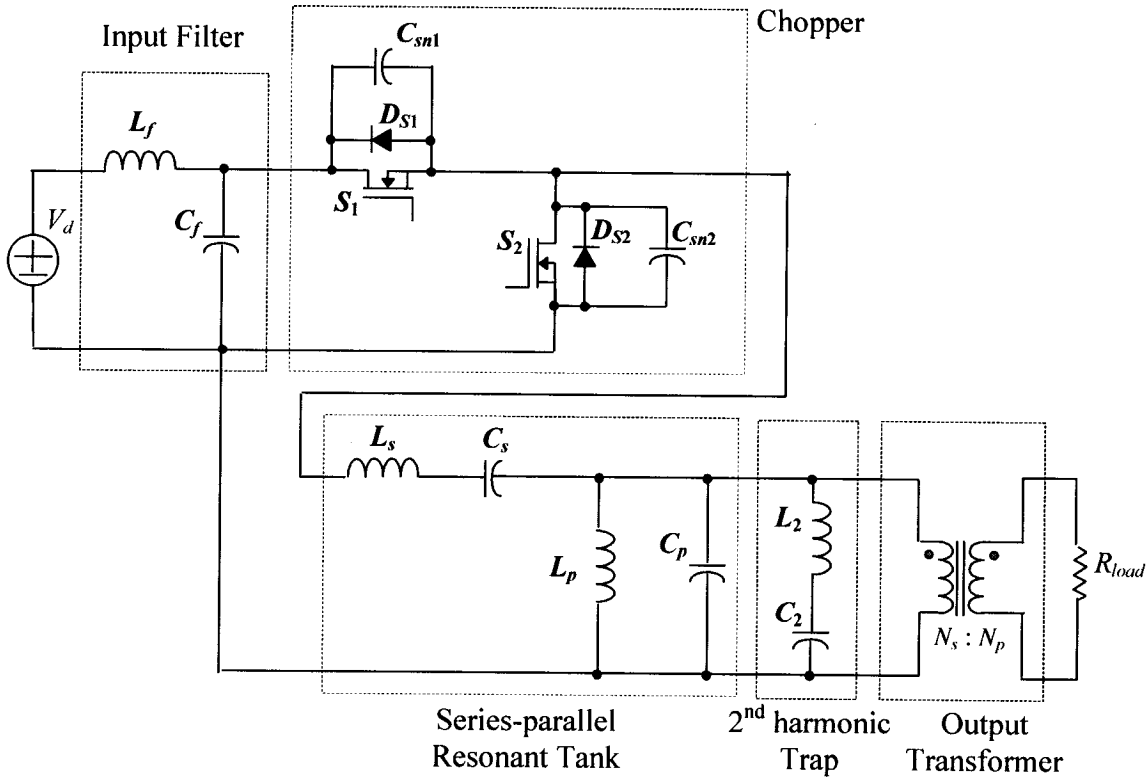


Fig. 4- 2: The proposed APWM resonant inverter

4.2.1 Specifications

In this design example, the following specifications are given:

(i) Input dc voltage: 60 V to 75 V;

(ii) Output voltage: 28 V (RMS), THD < 2%;

(iii) Rated output power: 200 W;

(iv) Constant operating frequency: 1 MHz.

4.2.2 Base Quantities

In Chapter 2, the circuit parameters are normalized in section 2.2.2, and the steady-state analysis results are obtained in per unit expression. In this design example, the following base quantities are defined:

Base voltage is the minimum input voltage of the inverter:

$$V_B = 60 \text{ V} = 1 \text{ p.u.} \tag{4- 1}$$

Base frequency is the operating frequency:

$$f_B = 1 \text{ MHz} \tag{4- 2}$$

Base impedance is given by:

$$R_B = N^2 R_{load} = N^2 V_o^2 / P_o = 3.7\ \Omega \tag{4- 3}$$

Base current:

$$I_B = V_B / R_B = 16.2 \text{ A} \tag{4- 4}$$

Base power:

$$P_B = V_B I_B = 973 \text{ W} \tag{4- 5}$$

4.2.3 Selection of Principle Components and Parameters

4.2.3.1 Second harmonic trap

As discussed in section 2.3.3, the following factors have to be considered to select the quality factor Q_2:

(i) To achieve ZVS operation, Q_2 has the minimum value given by (2-54) to guarantee that the parallel resonant branch and the 2nd harmonic trap together present an inductive impedance at the operating frequency;

(ii) Fig. 2-18 shows that higher value of Q_2 provides more contribution on the attenuation of the 3rd harmonic component at the inverter output;

(iii) Fig. 2-19 shows that higher value of Q_2 makes the negative effect of the tuning precision on the harmonic elimination, especially at small duty cycle.

Therefore, Q_2 = 2 is a good choice to satisfy (2-54), and meanwhile give good compromise between factor (ii) and factor (iii). Then the component parameters of the 2nd harmonic trap, L_2 and C_2, can be calculated by the definition of Q_2 given by (2-10), and their current and voltage ratings are given in section 2.3.1 by (2-55), (2-56) and (2-57) respectively.

4.2.3.2 Series-parallel resonant components

Generally, the quality factor of the resonant circuit is selected as small as possible to minimize the voltage and current stress on the resonant components and speed up the transient response against the load and input voltage variations. The minimum value of the quality factor is usually determined by the particular design specifications. Besides, in this proposed inverter, the series resonant branch is tuned at the operating frequency, while the parallel resonant branch is off-tuned. Therefore, in this design, three key parameters – quality factors Q_s & Q_p, and tuning factor k_p, are selected based on the following considerations:

(i) The total harmonic distortion of the inverter output voltage is less than 2% at the rated load for the whole input voltage range;

(ii) Zero-voltage-switching can be achieved under any operating conditions.

For this particular design example, the corresponding duty cycle control for the rated load ranges from 0.294 to 0.5. According to Fig. 2-13, Fig. 2-14, and Fig. 2-15 in section 2.3.2, $Q_s = Q_p = 2$ and $k_p = 1.15$ are found to be a good choice to satisfy the design requirement specifications. Finally the component parameters of the series-parallel

resonant circuit, L_s, C_s, L_p and C_p, can be calculated by the definition of Q_s, Q_p, and k_p given by (2-8), (2-9), and (2-16) respectively.

The voltage and current ratings of these components are given in section 2.3.1 by (2-42) to (2-48).

4.2.3.3 The output transformer

The output transformer provides safety isolation and matching for the inverter output. Thus the turns ratio of the transformer can be calculated as:

$$N = \frac{N_p}{N_s} = \frac{V_p}{V_o} \tag{4- 6}$$

Where V_p is the rms value of the transformer primary side voltage given by (2-42), and V_o is the rms value of the output voltage. In this design example, V_p = 0.45 p.u.= 27V, and V_o = 28V. Considering the voltage drop due to the winding resistance of the resonant inductor and the transformer, N can be selected between 0.86 to 0.9.

Selection of the power transformer core and magnetizing inductance can follow the conventional design procedure.

4.2.3.4 Input filter

As discussed in section 2.4, the inverter input current has a substantial ripple component at the operating frequency. Therefore, an input filter is necessary to smooth the current drawn from the unregulated dc line.

A simple LC input filter (L_f and C_f) is used in this design example, as shown in Fig. 4- 2. The expressions for the ripple current (I_{Lf}) in the inductor and the ripple voltage (V_{Cf}) across the capacitor are given by [73]:

$$I_{lf} = \sqrt{\sum_{n=1}^{\infty}\left(\frac{I_{in}(n)}{n^2(f_o/f_i)^2 - 1}\right)^2} \tag{4- 7}$$

$$V_{Cf} = \sqrt{\sum_{n=1}^{\infty}\left(\frac{2n\pi f_o I_{in}(n) L_f}{n^2(f_o/f_i)^2 - 1}\right)^2} \tag{4- 8}$$

Where $I_{in}(n)$ is the RMS n^{th} input harmonic (ripple) current of the inverter; f_o is the inverter operating frequency, and f_i is the resonant frequency of the input filter given by:

$$f_i = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{4- 9}$$

From Fig. 2-22, $I_{in}(1)$ is the dominant ripple in the input current, and reaches its maximum value at $D = 0.5$. For $Q_p = 2.0$ and $k_p = 1.15$, the maximum value of $I_{in}(1)$ is calculated by (2-79):

$$I_{in}(1) = 0.236 \quad \text{p.u.} \quad = \quad 3.82 \quad A \tag{4- 10}$$

Assume that the voltage ripple across the filter capacitor is 5% and the ripple current flowing through the inductor is 2%. From (4- 7) and (4- 8):

$$\frac{V_{cf}}{I_{lf}} = 2\pi n f_o L_f \tag{4- 11}$$

Thus

$$L_f = \frac{V_{cf}}{2n\pi f_o I_{lf}} = \frac{0.05 \times 60}{2 \times 1 \times \pi \times 10^6 \times 0.02 \times 3.82} = 6 \quad \mu\text{H} \tag{4- 12}$$

From (4- 7), when n = 1,

$$0.02 = \frac{1}{(f_o/f_i)^2 - 1} \tag{4- 13}$$

Therefore,

$$f_i = f_o/7.14 = 140 \quad \text{kHz} \tag{4- 14}$$

The value of C_f can be determined by:

$$C_f = \frac{1}{(2\pi f_i)^2 L_f} = 215 \quad \text{nF} \tag{4- 15}$$

4.2.3.5 Chopper circuit

(1) Maximum duty cycle of switch S_1

As discussed in section 2.2.3, to avoid saturation of the isolation transformer used in the driver of S_1, and maximize the switch utilization shown in Fig. 2-21, Maximum duty cycle of switch S_1 is chosen as 0.5.

(2) Voltage and current ratings of the switches

The voltage rating of the switch is equal to the maximum dc input voltage, 75V. The rms value of the current flowing through each switch is given by (2-49) in section 2.3.1, and is equal to 1.35 p.u. (22 A) from Fig. 2-12(g).

(3) Snubber capacitors

Turn-off current of the switch given by (2-51) and (2-52) in section 2.3.2 are used to calculate the value of its parallel snubber capacitor to minimize the turn-off switching loss. The absolute value of the snubber capacitor can be calculated as ($I_{S1\_turn\text{-}off}$ and $I_{S2\_turn\text{-}off}$ are renamed as $I_{S\_turn\text{-}off}$):

$$C_{sn} = \frac{t_{ar}}{2V_{d\ \max}} \cdot I_{s\_turn-off} \cdot I_B \tag{5-6}$$

Where, t_{ar} is the allowable time for the switch voltage to reach the maximum input voltage, and should be less than the specified dead time (around 15 ns) between the gating signals of those two complementary switches. The maximum value of $I_{S1\_turn\text{-}off}$

from Fig. 2-14 is 0.55 p.u. (9 A), and the maximum value of $I_{S2\_turn\text{-}off}$ from Fig. 2-15 is 0.1 p.u. (1.6 A).

Finally, the principle components and parameters of this given inverter design example are given in Table 4-1.

Table 4-1: Principle components and parameters of the inverter design example

Components	Values	Selections
V_d	60 V – 75 V dc	
V_o	28 V rms	
p_o	200 W	
f_o	1 MHz	
L_s	1.2 μH	*Magnetics 55381-A2*
C_s	21 nF	*Wima FKP*
L_p	0.29 μH	*Magnetics 55381-A2*
C_p	66.2 nF	*Wima FKP*
L_2	1.2 μH	*Magnetics 55381-A2*
C_2	5.3 nF	*Wima FKP*
L_f	6 μH	*Magnetics 55381-A2*
C_f	215 nF	*Wima FKP*
C_{sn1}	720 pF	*TDK X7R*
C_{sn2}	130 pF	*TDK X7R*
Transformer	$N_p : N_s$ =19:22, L_m=0.01μH	*TDK PC44LP22/13*
S_1 & S_2	IRF540	Appendix E

4.3 DESIGN OF THE ON-BOARD AC VRM – PWM SEIRES RESONANT CONVERTER

In this section, the design of the pulse-width-modulated AC VRM (shown in Fig. 4- 3) is illustrated by a design example. Section 4.3.1 gives the specifications on which the design is based. Section 4.3.2 presents the selection of principle components and parameters, including the output transformer, series resonant tank (L_s, C_s), output capacitor (C_o), the primary side ac switch and the synchronous rectifier. The performance curves and equations derived in Chapter 3 are used here to develop the design procedure.

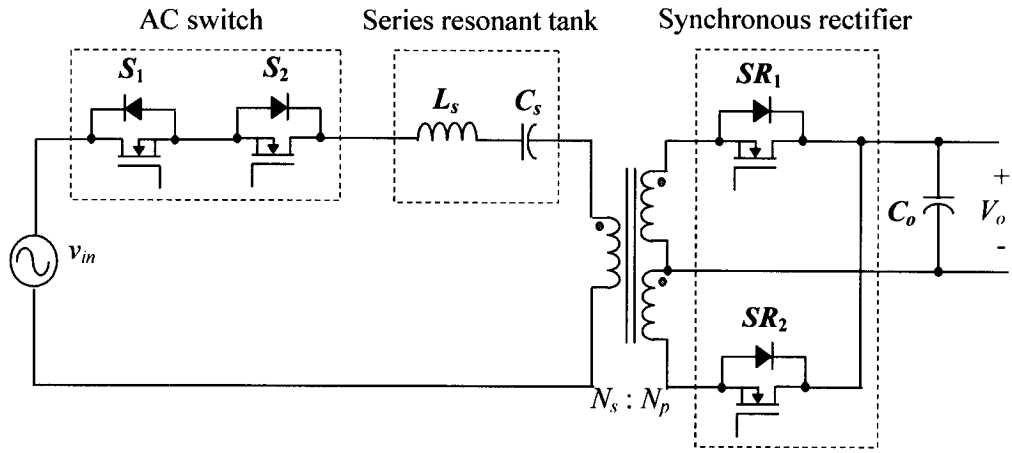


Fig. 4- 3: The proposed pulse-width-modulated AC VRM

4.3.1 Specifications

In this design example, the following specifications are given:

(v) Input ac voltage: 28 V rms, 1MHz, sinusoidal waveform;

(vi) Output voltage: 1.5 V dc;

(vii) Output voltage regulation: 1% in the steady-state and 3% in the transient);

(viii) Rated output power: 30 W;

(ix) Constant operating frequency: 1 MHz.

4.3.2 Selection of Principle Components and Parameters

4.3.2.1 The output transformer

At full load, the ac switch is on continuously and the transformer magnetizing current is negligible. Assuming that ideal transformer is considered, its primary side voltage is given by (3-8). Its fundamental component should equal the input voltage:

$$\frac{2\sqrt{2}}{\pi}(V_o + V_{SR})N = V_{in} \tag{4- 16}$$

Where, N is the transformer turns ratio, V_{in} is the RMS value of the input ac voltage. V_o is the output dc voltage, and V_{SR} is the RMS value of the voltage drop on the synchronous rectifier due to the on-resistance $R_{ds(on)}$ of the switch (about 0.075 V).

Therefore, in this design, the transformer turns ratio can be selected as N = 19.7. Selection of the power transformer core and magnetizing inductance can follow the conventional design procedure.

4.3.2.2 The series resonant tank

Since the large load transient with very high slew rate (di/dt) is a critical issue for the AC VRM, the quality factor of the series resonant circuit should be selected as small as possible to speed up the transient response. However, as shown in Fig. 3-16, the input current has very poor power factor at rated load if the quality factor is too low. According to the steady-state characteristics of the input current analyzed in section 3.2.4.1, and the dynamic analysis presented in section 3.4, quality factor equal to 0.6 can provide fast transient response and close-to-unity rated power factor as well. The values of the resonant components can be calculated accordingly, and their voltage and current ratings

are given by (3-51), (3-52), and (3-53) when duty cycle is equal to 1 (refered to Fig. 3-18, Fig. 3-19 and Fig. 3-20).

4.3.2.3 The output capacitor

The output capacitor is selected to minimize the output noise voltage and to guarantee regulation during load transients. These two goals are all important for the AC VRM design.

A. Selecting based on minimizing the output voltage ripple

The value of the output capacitor is calculated by considering the waveforms shown in Fig. 4- 4. Assuming that all the ripple components in the rectifier current flow through the output capacitor, the minimum value of the output capacitance can be determined by the conventional criteria: $C_o \geq \Delta Q/\Delta V_o$ (ΔQ and ΔV_o are defined in Fig. 4- 4). If the percentage ripple in the output voltage is specified to be 1% in this design, the output capacitance should be greater than 480 μF.

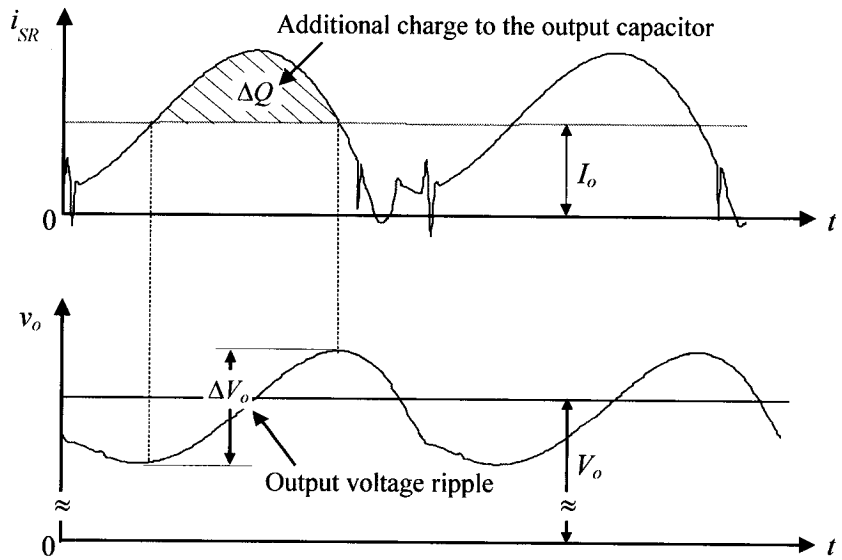


Fig. 4- 4: Output voltage ripple of the proposed AC VRM

B. Selecting based on load transient response

Usually, in the system with power management, when the load transition from the sleep mode to the active mode and vice versa, the slew rate of the transient load current is much higher than the VRM can support. As an example, when the load transition from sleep mode to active mode occurs, the load current I_{load} required at that instant is temporarily provided from the output capacitor awaiting for the VRM output current I_o to catch up, which results in the undershoot in the output voltage. The required output capacitance is calculated according to Fig. 4- 5 to hold-up the output voltage during such large load transient.

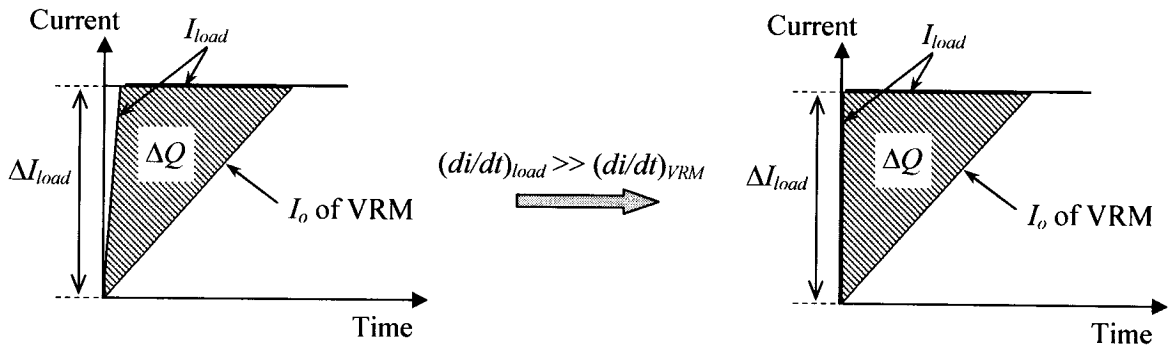


Fig. 4- 5: Load current transient from sleep mode to active mode

In Fig. 4- 5, assuming linear current rising for simplicity, the amount of charge provided by the output capacitor during the transient is approximately calculated by:

$$\Delta Q \approx \frac{\Delta I_{load}^2}{2(di/dt)_{VRM}} \tag{4- 17}$$

The current slew rate of the AC VRM, $(di/dt)_{VRM}$, is limited by the series resonant inductor L_s:

$$\frac{di_r}{dt} = \frac{v_{Ls}}{L_s} \tag{4- 18}$$

Thus, the value of the output capacitor can be evaluated as:

$$C_o = \frac{\Delta Q}{V_{o,drop}} = \frac{\Delta I_{load}^2 L_s}{2Nv_{Ls}V_{o,drop}} \quad (4\text{-}19)$$

Where, N is the transformer turns ratio (=19.7 in this design); ΔI_{load} is the change in the load current from sleep mode to active mode (=18A); L_s is equal to 2.5 μH; $V_{o,drop}$ (=0.045V) is the allowed maximum voltage drop determined by the voltage regulation (3% during the transient); v_{Ls} is the voltage across the series resonant inductor, which could be as low as 1V in the sleep mode. Therefore, the output capacitance should be greater than 460 μF in this design.

Considering selection A and selection B, the output capacitor in this design is chosen as 500μF.

C. Selecting capacitor types

When selecting capacitors, power loss, size, and circuit noise are primary concerns. Especially for a capacitor placed at the output, the value and type of capacitor also influences the loop bandwidth and load transient response of the converter.

Common capacitor types used in the converter with low output voltage are aluminum electrolytic, tantalum, and ceramic. Ceramic type is chosen in this design due to its satisfied performance characteristics with respect to size, ripple performance, and relative cost.

The same ceramic type with different packages could have very different ESR and ESL. Its selection is dependent on the function of the capacitor in a cost-effective way. The output capacitor of 500 μF in this design is a capacitor bank which consists of two types of capacitors in parallel. One type is ceramic capacitor with very low ESR

(0.11mΩ) and ESL (0.025nH) to guarantee the voltage regulation during the large load transients. Another type is ceramic capacitor with relatively high ESR (1.5mΩ) and ESL (1.25nH) to minimize the output noise voltage.

4.3.2.4 The priamry side ac switch

(1) Determination of turn-on delay

As discussed in section 3.1.2, zero-voltage-switching of the primary side ac switch can be achieved under any load condition as long as the turn-on delay of the switch is set to be large enough. The delay time can be determined refering to Fig. 4- 6. This figure shows the switching waveforms corresponding to the maximum charging and discharging time of the drain-source capacitor C_{ds}.

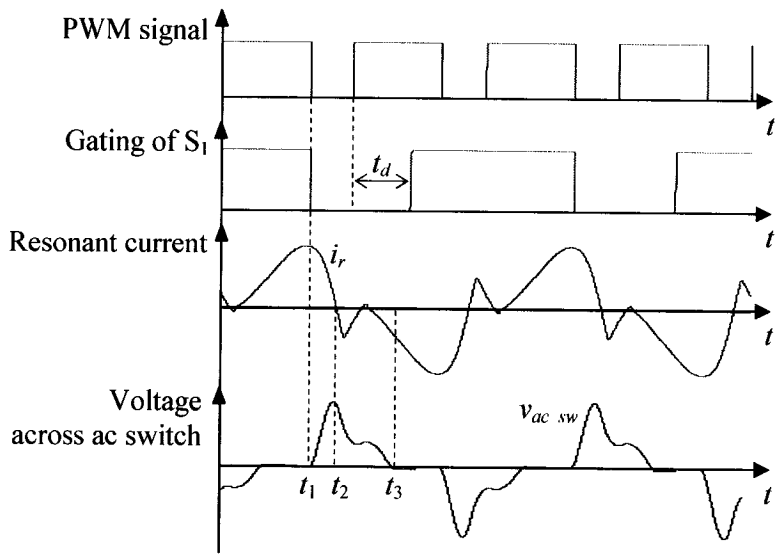


Fig. 4- 6: Switching waveforms of switch S_1 in the ac switch

In Fig. 4- 6, the charging time for the capacitor C_{ds} can be approximately determined by:

$$t_{charge} = t_2 - t_1 = \frac{2C_{ds}\hat{V}_{ac\_sw}}{I_{off}} \tag{4- 20}$$

Where, I_{off} is the turn-off current of switch S_1 calculated by (3-34) when $t = d/(2f_o)$. I_{off} is about 1 A at reduced load. C_{ds} is the inherent drain-source capacitance of the candidate switch when its drain-source voltage around 10V. $\hat{V}_{ac\_sw}$ is two times of the theoretical value calculated from (3-53).

Since the charging and discharging of C_{ds} is not symmetrical due to the distorted resonant current, assuming that the discharging time is 3 times of the charging time, the total charging and discharging time for C_{ds} thus becomes $4t_{charge}$. To achieve zero-voltage-switching, the turn-on delay time must satisfy:

$$t_{d(on)} \geq 4t_{charge} - \frac{1-d}{2f_o} \tag{4- 21}$$

Equation (4- 21) gives $t_{d(on)} \geq 0.2\mu s$ for this given design example.

(2) Other considerations

Although the ac switch is soft-switched, it still suffers from the so-called $\frac{1}{2}CV^2$ losses due to its inherent drain-source capacitance C_{ds}. This parameter, meanwhile, has dramatic effect on the switch voltage stress at reduced load. The switch selection should provide good compromise between these two factors. On the other hand, the trade-off in the switch selection should be also made between the least inherent capacitance and the least on-resistance to result in the least total losses in the ac switch.

The current rating of the ac switch is given by (3-53) when duty cycle is equal to 1 (Fig. 3-20). Its voltage rating should be able to handle the peak value of (3-54) at

reduced load, which is approximately equal to the peak value of the ac input voltage with some margin.

4.3.2.5 Sychronous rectifier (SR)

The target rectification efficiency, η_{rect}, limits the allowable maximum voltage drop across the SR, V_{drop_SR}, by:

$$V_{drop\_SR} \le (1-\eta_{rect})V_o \tag{4- 22}$$

Thus the total resistance of the SR switch shall be limited by:

$$R_{SR} < \frac{V_{drop\_SR}}{2.8I_{SR}} \tag{4- 23}$$

Where, I_{SR} is the rms value of the rectifier current given by (3-56) when duty cycle is equal to 1 (Fig. 3-22), and the factor 2.8 takes into account the thermal effects of $R_{ds(on)}$ and the PCB trace impedance.

The number of MOSFETs to be paralleled to form one SR switch is thus given by:

$$N_{SR} \ge \frac{R_{ds(on)}}{R_{SR}} \tag{4- 24}$$

Where, $R_{ds(on)}$ is the on-resistance of the candidate MOSFETs to be employed. However, large number of N_{SR} should be avoided. Otherwise, the costs, the circuit size and the gate-drive power would be unnecessarily increased.

The candidate SR switches should meet voltage rating given by:

$$V_{SR\_max} = 2\hat{V}_{SR} \tag{4- 25}$$

Where, the factor of 2 takes into account the voltage overshoot due to the effect of the transformer leakage inductance. $\hat{V}_{SR}$ is equal to 3.8 V given by (3-55).

The RMS current shall refer to (3-56) and Fig. 3-22.

To avoid cross-conduction (short circuit) of the SR switches, and to achieve zero-voltage switching as well, there is a dead time (t_{dd}) between the gating signal for the top switch and the gating signal for the bottom switch. This dead time is given by:

$$t_{dd} = t_{d(off)} + t_f \tag{4- 26}$$

Where, $t_{d(off)}$ and t_f are the turn-off delay time and fall time respectively of the candidate SR MOSFETs.

Finally, the principle components and parameters of this AC VRM design example are given in Table 4-2.

Table 4-2: Principle components and parameters of the AC VRM design example

Components	Values		Selections
L_s	2.5 μH		*Magnetics 55381-A2*
C_s	10 nF		*Vima FKP*
C_o	500 μF	Four 100μF with ESR=1.5mΩ and ESL=1.25nH	*TDK X7R*
		ten 10μF with ESR= 0.11mΩ and ESL=0.025nH	*TDK X7R*
Transformer	$N_p : N_s$ =19.6 , L_m= 145 μH		*TDK PC5 0EPC17*
S_1 & S_2	IRFP150		Appendix E
SR_1 & SR_2	Two IRF 7822 in parallel		Appendix E

4.4 IMPLEMENTATION OF THE HFAC DISTRIBUTED POWER SYSTEM

In this section, the APWM inverter designed in section 4.2 is employed in HFAC DPS to generate sinusoidal voltage and current distribution. Paralleled PWM resonant converters designed in section 4.3 are connected to the output of the inverter to produce multiple independently regulated outputs. Furthermore, the operating principles of such a system are discussed under different operation modes.

4.4.1 Conceptual Implementation

Fig. 4- 7 shows the conceptual implementation of the proposed high frequency AC distributed power system (HFAC DPS) for a two-output application. More outputs can be easily added by paralleling additional secondary circuits in the same manner.

In the HFAC DPS, the primary circuit is a simple DC/AC inverter with feedforward and feedback control to provide high-quality sinusoidal bus voltage against any input and secondary load variation. The secondary circuit is paralleled AC VRMs. Each AC VRM employs switch-controlled resonant tank to achieve output regulation and synchronous rectifier to improve the efficiency of the rectification stage.

4.4.2 Detailed Implementation

The detailed implementation of the conceptual architecture of Fig. 4- 7 is shown in Fig. 4- 8. The primary circuit is the APWM resonant inverter developed in Chapter 2 and designed in section 4.2. The only difference is the implementation of the feedback control loop. Instead of feeding back the voltage from the transformer secondary side, the primary side voltage is fed back. Such a feedback loop avoids any control loop that crosses over the isolation boundary between the primary and secondary side.

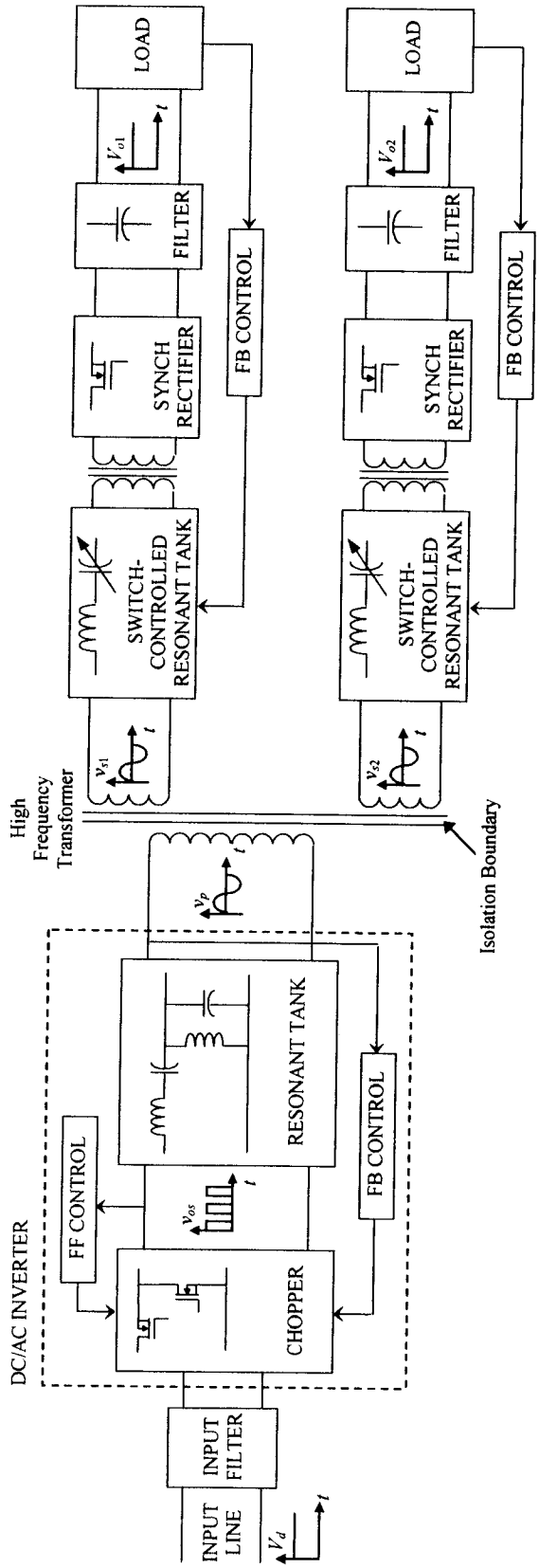


Fig. 4-6: The conceptual block diagram of the HFAC DPS for the two-output application

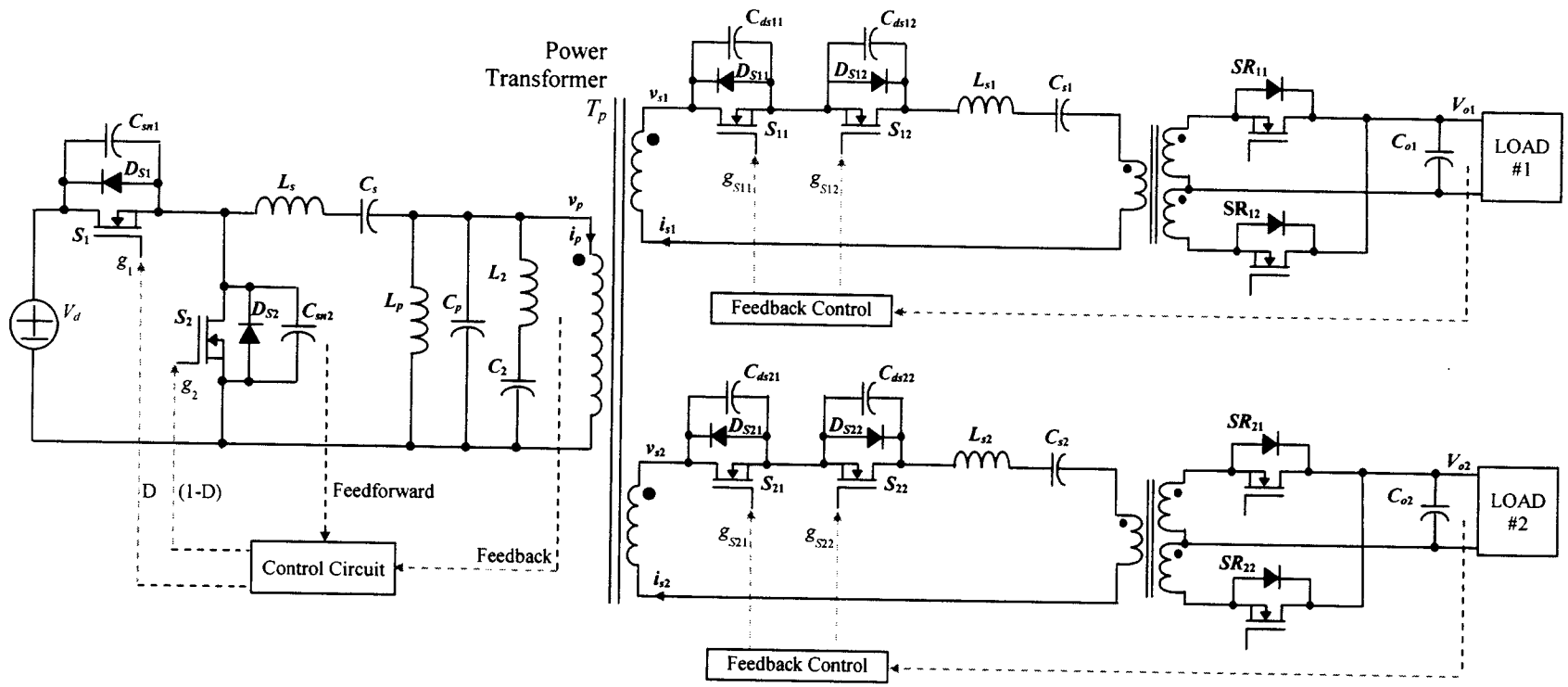


Fig. 4-7: Detailed implementation of the HFAC DPS for the two-output application

The secondary circuit consists of multiple AC VRMs using the PWM series resonant converter topology developed in Chapter 3 and designed in section 4.3. The feedback control loop is the same as the one designed in section 3.4.

4.4.3 Advantageous Features

Compared with the existing DC distributed power system, the HFAC DPS has all the advantageous features introduced in Chapter 1. The most remarkable features referring to Fig. 4- 8 are:

(i) Reduction of number of components due to less power conversion stages required. This feature results in higher frequency, higher reliability, lower cost and smaller size.

(ii) Excellent transient response because of C filter instead of LC filter at the AC VRM output.

(iii) Soft-switching in both front-end inverter and AC VRMs.

(iv) Isolated multiple AC VRMs, and no control loop that crosses over the isolation boundary between the primary and secondary side. This feature permits complete and reliable isolation for the power distribution.

(v) Independent feedback control of each AC VRM, hence providing precise regulation of each output voltage.

(vi) Inherent current limiting due to the resonant tank incorporated in both front-end inverter and AC VRMs. This feature makes the output short-circuit-proof easy.

(vii) Low EMI due to sinusoidal voltage and current distribution.

4.5 SYSTEM OPERATING PRINCIPLE

The HFAC DPS of Fig. 4- 8 operates in the following modes: (i) power transfer mode; (ii) no-load mode; and (iii) short-circuit mode. The equivalent circuits of the system during each operation mode are shown in Fig. 4- 9.

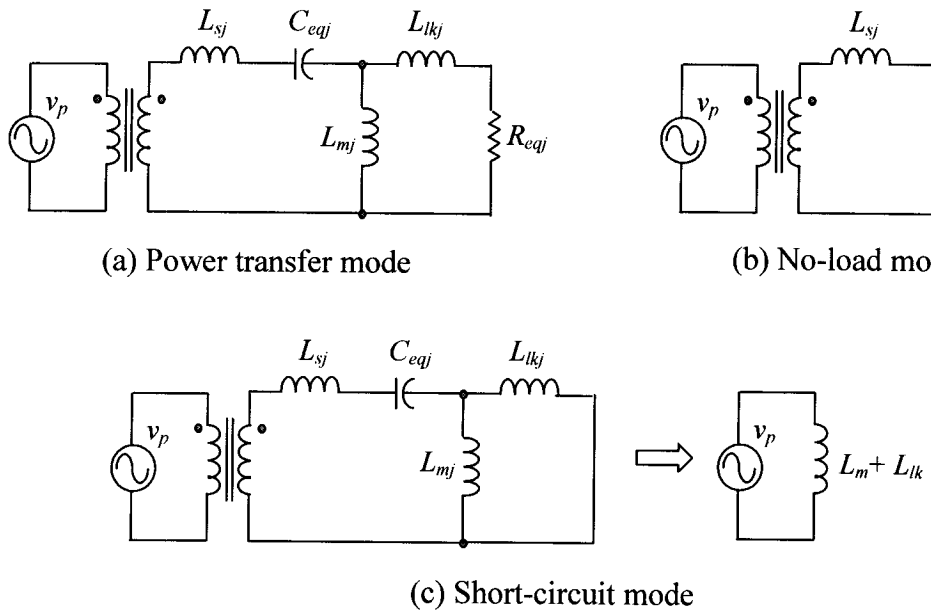


Fig. 4- 9: Equivalent circuits of HFAC DPS during each operation mode

4.5.1 Power Transfer Mode

In this mode of operation, as shown in Fig. 4- 9(a), the primary circuit is equivalent to a sinusoidal voltage source. It operates in the same way as described in Chapter 2 to achieve ZVS and output voltage regulation. The feedforward control combined with feedback control can provide instantaneous output regulation against the input voltage variation. This combination can also provide fast output regulation against vary large secondary load variation.

On the secondary side, only the equivalent circuit of the arbitrary j^{th} AC VRM is shown in Fig. 4- 9(a). The rectification stage is represented by its equivalent ac resistance. L_{mj} is the magnetizing inductance of the transformer in the rectification stage of the j^{th} AC VRM. The primary side leakage inductance is lumped with the series resonant inductance, and the secondary side leakage inductance seen from the primary side is represented by L_{lkj}. Each AC VRM operates in the same way as described in Chapter 3. ZVS is achieved independent of the load condition in both ac switch and the synchronous rectifier. Each AC VRM is controlled independently, and has fast response against large transient signal with very high slew rate in the output.

4.5.2 No-Load Mode

This mode of operation occurs when the secondary load is not connected, and the equivalent circuit is shown in Fig. 4- 9(b). In this mode of operation, the quality factor of the series resonant circuit of the AC VRM is close to zero. The output voltage control curves of Fig. 3- 8 show that the output voltage still can be regulated at its nominal value by a very small duty cycle. The no-load current drawn at the primary side is only a fraction of the nominal current.

4.5.3 Short-Circuit Mode

When a short circuit occurs at the output of the j^{th} AC VRM, the current drawn by the AC VRM would rise to a high value as a result of the substantially increased quality factor of the series resonant circuit. The ac switch of AC VRM will be shut down when the current reaches a limit value. Then the short-circuited AC VRM presents an open-circuit load for the inverter, as shown in Fig. 4- 9 (c). In such an equivalent circuit, the

sum of the magnetizing inductance and the leakage inductance of the main transformer is typically high (approximately 20 times the equivalent rated output resistive load), and the no-load current drawn at the primary is only a fraction of the nominal value.

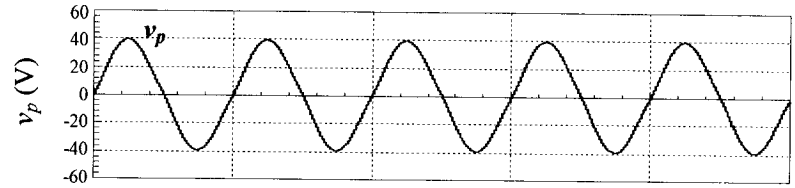
Making the AC VRM output short-circuit-proof is relatively easy because the series resonant inductance and the transformer leakage inductance make the current take a few resonant cycles to rise. This fact allows considerable time for the control circuit to take action. Consequently, the voltages across all the windings of the main transformer T_p do not collapse.

4.6 SYSTEM STEADY-STATE PERFORMANCE

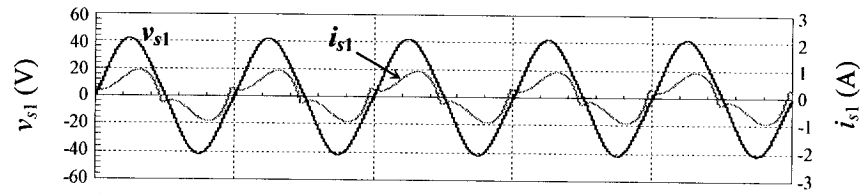
The steady-state performance of the HFAC DPS for a two-output application of Fig. 4- 8 is simulated by using the simulation tool PSpice.

During the power transfer operating mode, assume that the 1st AC VRM is operating under the full load, and the 2nd AC VRM is operating under 50% load, the main operating waveforms are shown in Fig. 4- 10. The designations of the variables are referred to Fig. 4- 8. All the spikes in the output voltage of the AC VRM are due to the ESRs and ESLs of the output capacitor. The amplitude of these spikes is much reduced by adding decoupling capacitors at the output of AC VRM in the real circuit, as shown in the experimental output voltage ripple of Fig. 3- 64.

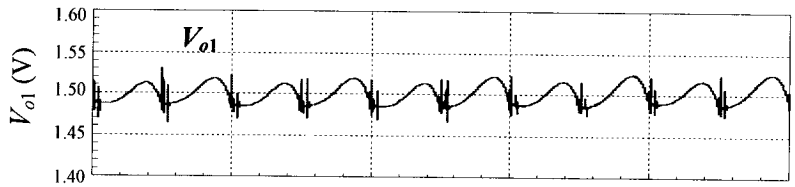
Fig. 4- 10 shows that, in the power transfer mode, the output voltage of the inverter is a very clean sinusoidal waveform, and all the AC VRMs are regulated independently. The steady-state characteristics of the inverter and AC VRM derived from Chapter 2 and Chapter 3 respectively can be applied.



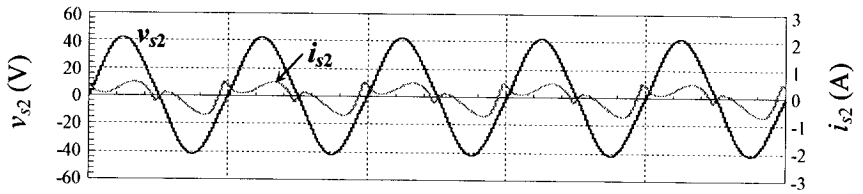
(a) Inverter output voltage v_p (20V/div)



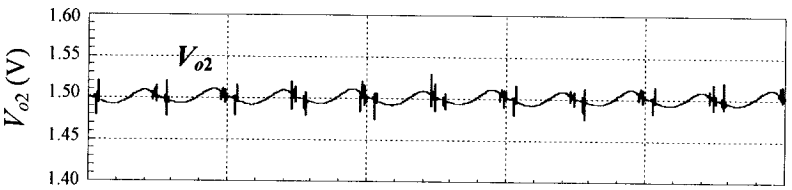
(b) 1st AC VRM input voltage v_{s1} (20V/div) and current i_{s1} (1A/div)



(c) 1st AC VRM output voltage V_{o1} (50mV/div)



(d) 2nd AC VRM input voltage v_{s2} (20V/div) and current i_{s2} (1A/div)



(e) 2nd AC VRM output voltage V_{o2} (50mV/div)

Fig. 4- 10: Steady-state operating waveforms during power transfer mode

(Horizontal time scale: 1μs/div)

The harmonic spectrum of the current drawn from the dc input line is shown in Fig. 4- 11 (a) and (b) for input voltage equal to 60 V and 75 V respectively when both AC VRMs are operating under the rated load. As compared with Fig. 2- 38, the

harmonics contained in the input current of the inverter are effectively attenuated by the input filter. The design of the input filter in this chapter is therefore verified.

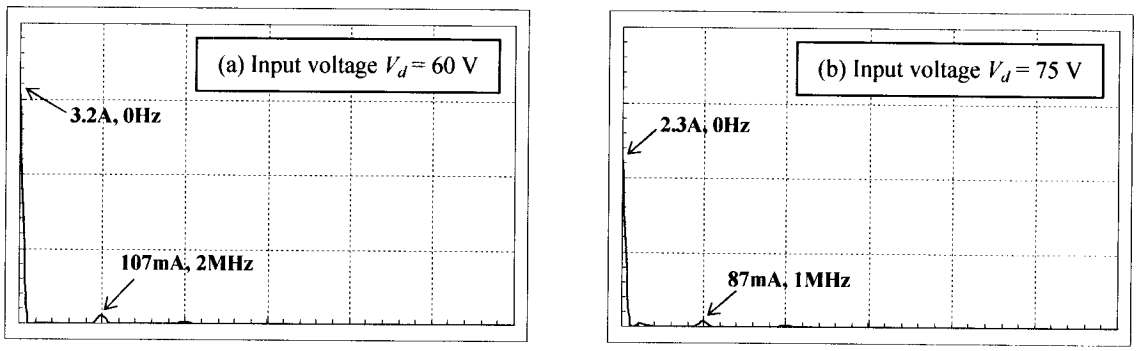
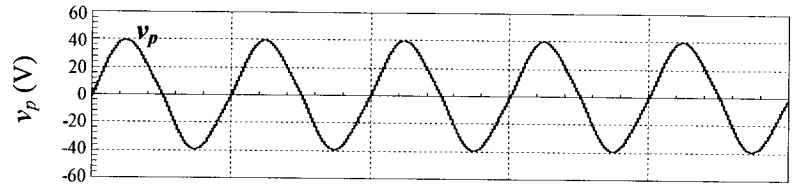


Fig. 4- 11: Harmonic spectrum of the system input current

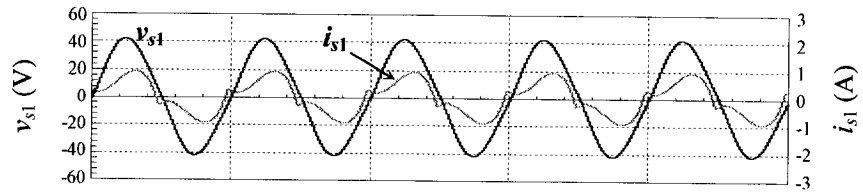
(Horizontal scale: Frequency 1MHz/div; Vertical scale: current 1A/div)

During the no-load operating mode, assuming that the 1st AC VRM is operating under the full load and the 2nd AC VRM has no load, the main operating waveforms are shown in Fig. 4- 12. The output voltage of the 2nd AC VRM is regulated at 1.5 V. The current drawn by the 2nd AC VRM is highly distorted, and less than the nominal value. The output of the inverter (bus voltage) and the operation of the 1st AC VRM in the steady state are not affected in this operating mode.

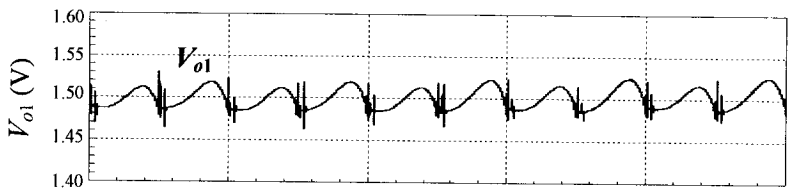
During the short-circuit operating mode, assuming that the 1st AC VRM is operating under the full load and the 2nd AC VRM has a short-circuited output. The ac switch of the 2nd AC VRM is shut down because of the excessive current. The main operating waveforms are shown in Fig. 4- 13. It can be seen that the output-short-circuited 2nd AC VRM has no effect on the steady-state operation of the 1st AC VRM. The power is transferred from the inverter to the 1st AC VRM as if the 2nd AC VRM does not exist. The voltages across all the windings of the main transformer T_p do not collapse.



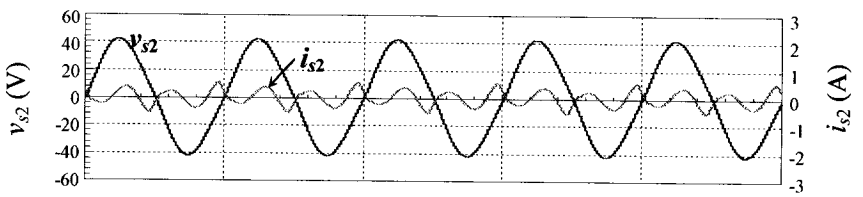
(a) Inverter output voltage v_p (20V/div)



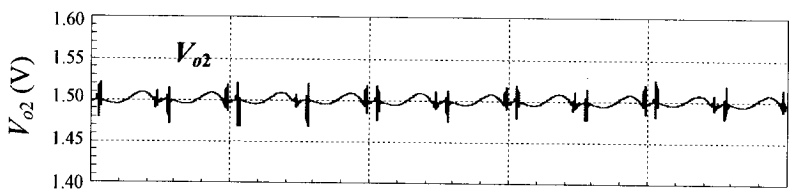
(b) 1st AC VRM input voltage v_{s1} (20V/div) and current i_{s1} (1A/div)



(c) 1st AC VRM output voltage V_{o1} (50mV/div)



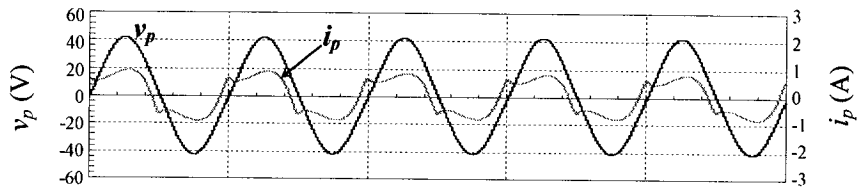
(d) 2nd AC VRM input voltage v_{s2} (20V/div) and current i_{s2} (1A/div)



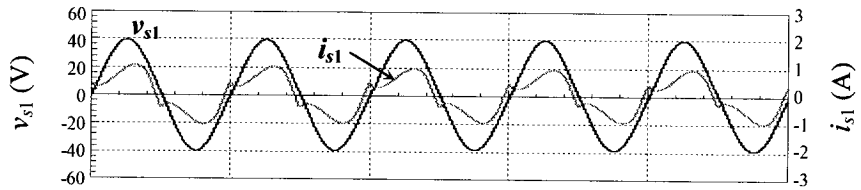
(e) 2nd AC VRM output voltage V_{o2} (50mV/div)

Fig. 4- 12: Steady-state operating waveforms during no-load mode

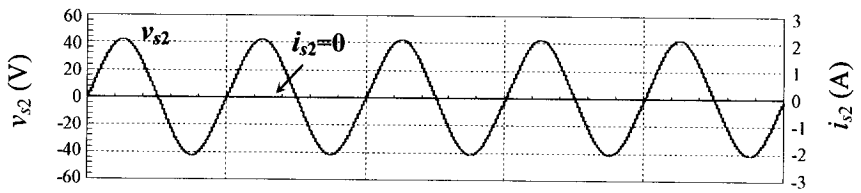
(Horizontal time scale: 1μs/div)



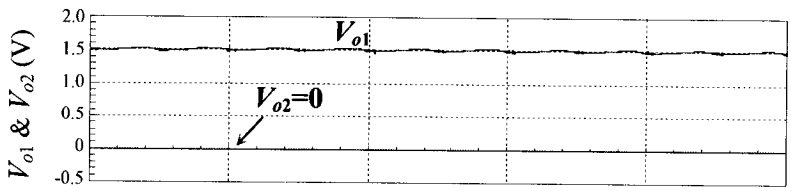
(a) Inverter output voltage v_p (20V/div) and current i_p (1A/div)



(b) 1st AC VRM input voltage v_{s1} (20V/div) and current i_{s1} (1A/div)



(c) 2nd AC VRM input voltage v_{s2} (20V/div) and current i_{s2} (1A/div)



(d) Output voltage of AC VRMs V_{o1} & V_{o2} (500mV/div)

Fig. 4- 13: Steady-state operating waveforms during short-circuit mode

(Horizontal time scale: 1μs/div)

4.7 SYSTEM DYNAMIC PERFORMANCE

In this section, the following system dynamic performance is investigated by simulating the HFAC DPS of Fig. 4- 8:

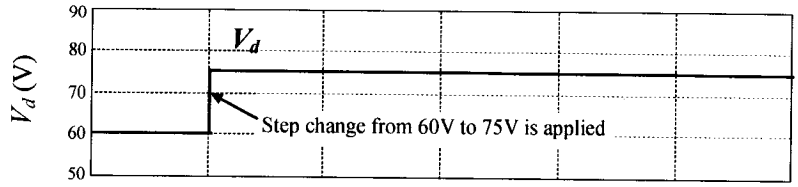
(i) The system response against the line variation (Fig. 4- 14);

(ii) The system response when one AC VRM's load operates from sleep mode to active mode (Fig. 4- 15);

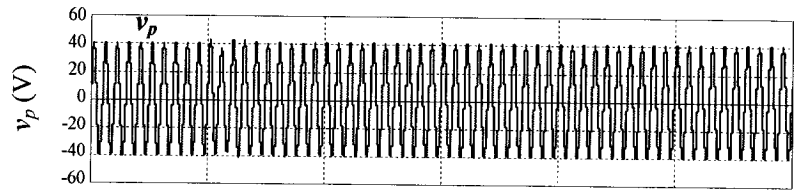
(iii) The system response when one AC VRM's load operates from active mode to sleep mode (Fig. 4- 16);

(iv) The system response when one AC VRM is short-circuited (Fig. 4- 17).

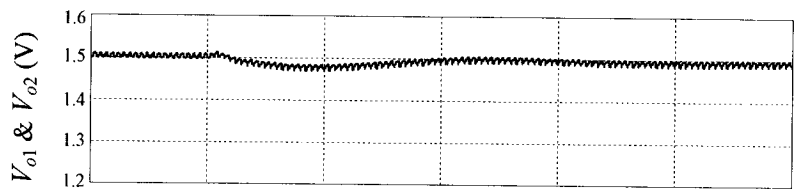
In Fig. 4- 14, the input dc voltage has a step change from 60 V to 75 V, and two AC VRMs are operating under full load. The inverter output voltage takes about 4 cycles to be stable again. The output voltage of the AC VRMs drops about 2%, and takes about 20 μs to go back to its steady state.



(a) Input voltage of the inverter V_d (10V/div)



(b) Inverter output voltage v_p (20V/div)

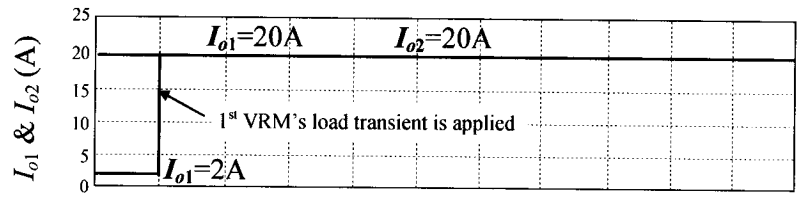


(d) Output voltage of AC VRMs V_{o1} & V_{o2} (100mV/div)

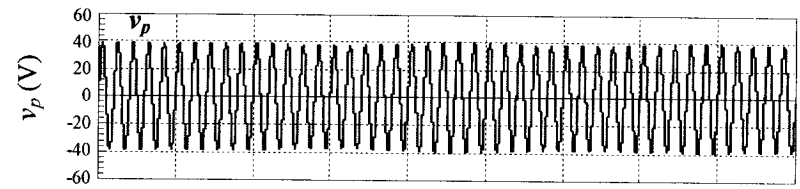
Fig. 4- 14: The system response against the line variation

(Horizontal time scale: 10 μs/div)

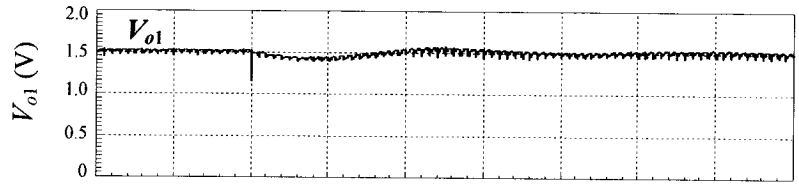
Fig. 4- 15 shows the system response when the load of the 1st AC VRM is suddenly changed from sleep mode to active mode. The slew rate (di/dt) of 1A/ns is applied. The output voltage of the inverter is hardly affected, and the output voltage of the 2nd AC VRM has very little variation (about 2%) from its steady state. The output voltage of the 1st AC VRM drops about 4% and takes 10μs to come back to its nominal value. The first undershoot spike of the 1st AC VRM in Fig. 4- 15 is caused by the ESLs of the output capacitor. This spike is even more severe in the real circuit due to the interconnect inductance L_{interc} between VRM and the load. Therefore it is necessary to add decoupling capacitors with very low ESL across the load to limit this spike.



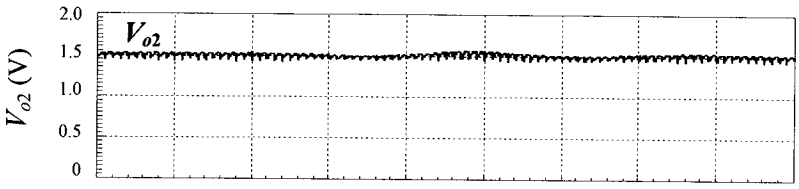
(a) AC VRMs output current I_{o1} & I_{o2} (5A/div)



(b) Inverter output voltage v_p (20V/div)



(c) 1st AC VRM output voltage V_{o1} (500mV/div)

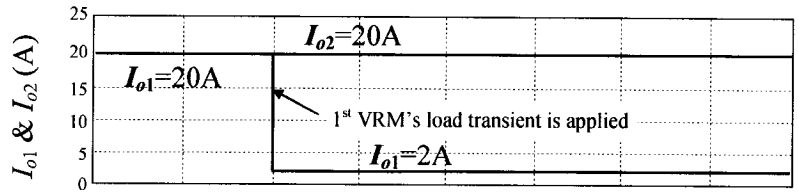


(d) 2nd AC VRM output voltage V_{o2} (500mV/div)

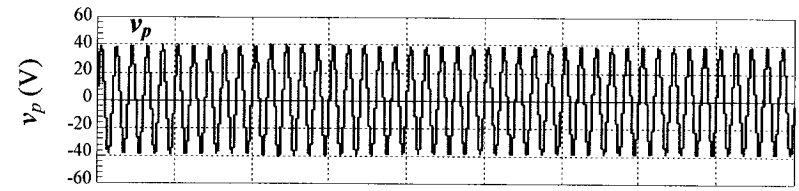
Fig. 4- 15: The system response when one AC VRM's load operating from sleep mode to active mode (Horizontal time scale: 5 μs/div)

Fig. 4- 16 shows the system response when the load of the 1st AC VRM is suddenly changed from active mode to sleep mode to save power. The slew rate (di/dt) of 1A/ns is applied. The output voltage of the inverter has negligible variation, and the output voltage of the 2nd AC VRM has less than 2% deviation from its steady state. The output voltage of the 1st AC VRM has an overshoot about 4% and takes 10μs to come back. Again, the initial voltage spikes at the output of the 1st AC VRM can be minimized

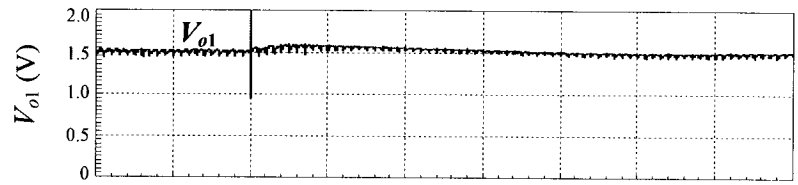
by adding additional ceramic capacitors with very low ESL. The absolute elimination of the cross-regulation under dynamic conditions is not achievable, because the input voltage of the AC VRM is coupled from the output of the inverter, which is not an ideal voltage source.



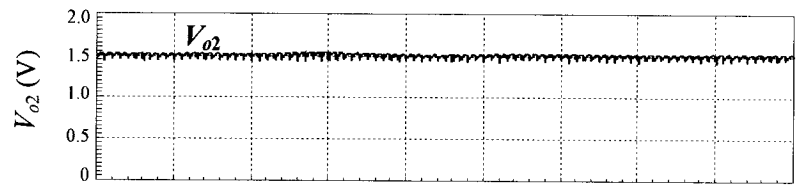
(a) AC VRMs output current I_{o1} & I_{o2} (5A/div)



(b) Inverter output voltage v_p (20V/div)



(c) 1st AC VRM output voltage V_{o1} (500mV/div)



(d) 2nd AC VRM output voltage V_{o2} (500mV/div)

Fig. 4- 16: The system response when one AC VRM's load operating from active mode to sleep mode (Horizontal time scale: 5 μs/div)

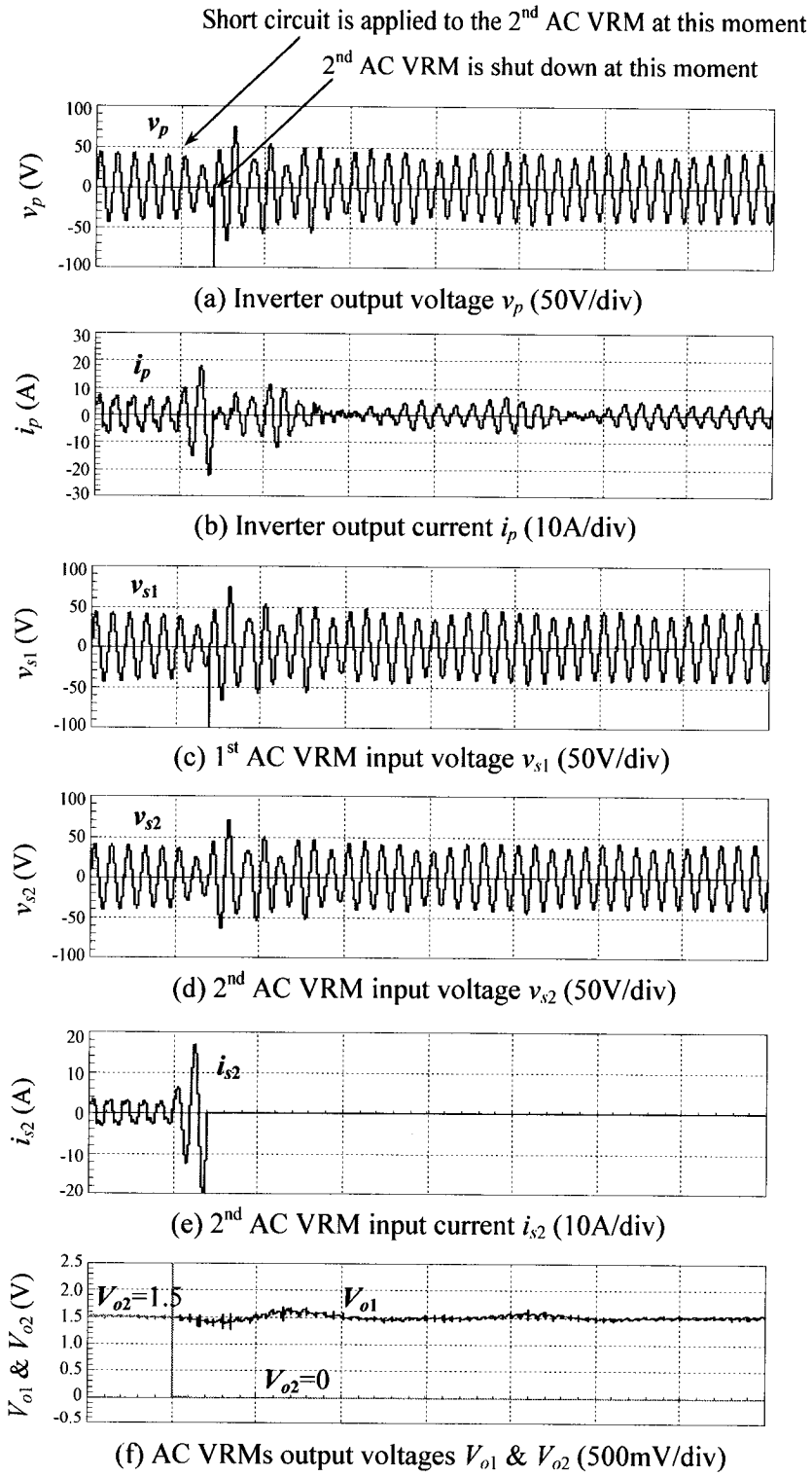


Fig. 4- 17: The system response when one AC VRM is output-short-circuited

(Horizontal time scale: 5μs/div)

Fig. 4- 17 shows the system response to the short circuit condition at the 2nd AC VRM output. When a short circuit is applied to the output of the 2nd AC VRM, the current drawn by this VRM starts to rise, but no large current spike with very high slew-rate appears due to the series resonant inductance. The ac switch of the 2nd AC VRM is turned off after 2 switching cycles (2 μs). During the transient, the voltages across all the windings of the main transformer T_p do not collapse. The output voltage of the 1st AC VRM has 5% deviation from its nominal value. The whole system takes about 25 μs to resume the steady-state operation.

The large under-shoot spikes in the output voltages of the inverter and the output voltage of the 1st AC VRM are caused because, in the simulation, the ac switch of the 2nd AC VRM is not turned off at zero-crossing of the series resonant current.

4.8 SUMMARY

In this chapter, the design procedure of the HFAC DPS has been illustrated by design examples. The implementation for a two-output application has been given. The operating principles of the power transfer mode, no-load mode, short-circuit mode have been explained. Finally, the concepts and design of the HFAC DPS have been verified by the simulation. The system performance in the steady state and under the large transient signals in both input voltage and output load have been investigated.

Besides the advantageous features of the HFAC DPS summarized in section 4.4.3, some features of the system performance can be concluded as:

(i) The system can operate in power transfer mode, no-load mode, and short-circuit mode;

(ii) In the steady-state operation, all the steady-state characteristics derived in Chapter 2 and Chapter 3 are validly applicable to the front-end inverter and AC VRM respectively;

(iii) In the steady-state operation, there is no output cross-regulation between AC VRMs, even when they are operating under different load conditions. However, under dynamic conditions, the output cross-regulation is inevitable;

(iv) Excellent system transient response against the line variation;

(v) The front-end inverter and AC VRMs keep good voltage regulation during the large load transition from sleep mode to active mode and vice versa which are usually encountered in the system with power management;

(vi) Inherent current limiting due to the resonant tank incorporated in both front-end inverter and AC VRMs can make the output short-circuit-proof easy;

With all the system features presented in this chapter together with advantageous steady-state characteristics of the front-end inverter and AC VRM presented in Chapter2 and Chapter 3 respectively, the HFAC DPS opens a new horizon for power solutions for the future desktop computer application.

CHAPTER 5

CONCLUSIONS

5.1 SUMMARY

This thesis has presented an alternative solution – high frequency ac distributed power system to powering the future applications of the desktop computers. The motivation of this research work has been driven by the new challenges of the power demand in the future, such as higher power density, lower supply voltage with very tight tolerance, higher supply current with very high slew rate (di/dt). These powering challenges arise from the fast growing trends in semiconductor technology which can benefit the computer system for higher speed, larger capacity and more advanced functions.

Based on the review of the present technology of DC DPS in desktop PCs, HFAC DPS has been introduced in Chapter 1 because this power architecture is capable of providing some features which are technically impossible in dc domain. Study and research have been carried out to achieve the objectives of this thesis - development and implementation of HFAC DPS for the applications of future desktop computers.

This thesis has dealt with two main power conversional blocks in HFAC DPS architecture – front-end inverter and AC VRM. An APWM resonant inverter has been proposed in Chapter 2 as the front-end inverter. This topology employs a chopper, a series-parallel resonant circuit, a 2^{nd} harmonic trap, and a high frequency transformer to provide sinusoidal voltage and current distribution with very low THD. A series resonant converter with a new control approach has been proposed as AC VRM in Chapter 3. In

the new control approach, an ac switch is used as a switch-controlled capacitor taking advantage of its own drain-source capacitor. This ac switch is connected in series with a series resonant tank so that the resonant frequency can be changed to achieve the output voltage control. In addition, synchronous rectifier is used to improve the efficiency of the rectification stage, and a simple capacitor bank is used as the output filter to speed up the transient response. Each chapter has provided the following information: (i) Description of topology and its operating principles; (ii) Steady-state and dynamic analyses; (iii) Performance characteristics under both steady-state and dynamic conditions; (iv) Simulation and experimental results to verify the concept.

By implementing HFAC DPS with the proposed APWM resonant inverter and the PWM series resonant converter, the design procedure, system implementation and performance have been given in Chapter 4. In the design procedure, the design considerations from the system point of view have been discussed, and the components selection of the circuit level has been illustrated by some design examples. In the system implementation, the system structure and operating principles have been described. Finally the system performance of HFAC DPS under both steady-state and dynamic conditions has been presented to prove the analyses, design and implementation.

5.2 CONTRIBUTIONS

Although the concept of HFAC DPS was proposed some 30 years ago, only little work had been done for the detailed system implementation on the circuit level, especially for the applications of very high operating frequency and low power. Therefore, the main contribution of this thesis is the development and implementation of

HFAC DPS to satisfy very challenging power demands for the future generations of desktop PCs.

The main contribution includes the following details:

(i) An improved APWM resonant inverter topology with the desired performance features has been developed as the front-end inverter;

(ii) An improved PWM series resonant converter topology with the desired performance features has been developed as the on-board AC VRM;

(iii) Steady-state and dynamic analyses of each topology have been performed;

(iv) Steady-state and dynamic performances of each topology have been proved by simulation and experimental results;

(v) Design procedure of each topology has been generated;

(vi) The system implementation by using the proposed topologies has been given;

(vii) The system performance under both steady-state and dynamic operating conditions has been evaluated.

5.3 CONCLUSIONS

In a conclusion, the main advantages of the HFAC DPS over the present DC DPS are: (i) Potentially high efficiency due to reduced power conversion stages; (ii) Very fast transient response due to the absence of low-pass output LC-filter and very high operating frequency; and (iii) Low EMI. Some detailed conclusions can be obtained from each part of the thesis as follows.

1. The proposed APWM resonant inverter is an attractive candidate for the front-end inverter in HFAC DPS because it has the following features:

(1.1) The proposed topology is capable of providing sinusoidal voltage and current distribution with low EMI.

(1.2) The proposed topology could operate in three distinct modes, and the preferred mode of operation is achieved when the series resonant branch is tuned at the operating frequency, and the parallel one is tuned slightly above the operating frequency. By carefully selecting the quality factors of the resonant circuit and harmonic trap, and the tuning factor of the parallel resonant branch, zero-voltage switching can be achieved independent of the input and load conditions in this preferred mode of operation.

(1.3) Very low THD (<2%) of the output voltage under various line conditions by adding a 2^{nd} harmonic trap.

(1.4) Overall efficiency can be kept constant around 90% from 50%-load to full load.

(1.5) A control scheme combined the modulated integral feedforward control with the feedback control provides fast transient response against large input voltage and load variation.

2. The proposed series resonant converter is an attractive candidate for the AC VRM in HFAC DPS because it has the following features:

(2.1) The new control approach has the advantages of soft switching under all load conditions, synchronous gating signals with the input voltage, continuous input current, and low voltage stress of the switches.

(2.2) Close-to-unity rated power factor and low total harmonic distortion in the input current.

(2.3) A relatively small output capacitor with a simple feedback control loop can provide very tight voltage regulation at the output (≤1% in the steady-state, and ≤3% during transient).

(2.4) The ac switch used in the new control approach can be controlled by either phase-shift modulation or pulse-width modulation to achieve the above features. However, PWM resonant converter is expected to have higher efficiency (2.5% higher) at rated load, because the gating signals are not complementary resulting in less conduction losses. Overall efficiency of PWM resonant converter can be kept constant around 85% from 50% load to full-load.

(2.5) The synchronous rectifier operates with zero-voltage-switching, and its gating signals are synchronized with the input voltage with fixed pulse-width which approximately equals to half cycle of the operating frequency.

3. HFAC DPS implemented by the proposed front-end inverter and AC VRMs could operate in one of the following modes of operation: (i) Power transfer mode; (ii) No-load mode; and (iii) Short-circuit mode.

4. Simulation of the system performance shows that:

(4.1) In the steady state operation, there is no output cross-regulation between AC VRMs, even when they are operating under different load conditions. However, under dynamic conditions, the output cross-regulation (≤2%) is inevitable.

(4.2) Excellent system transient response against the line variation.

(4.3) The front-end inverter and AC VRMs keep good voltage regulation during the large load transition from sleep mode to active mode and vice versa which are usually encountered in the system with power management.

(4.4) Inherent current limiting due to the resonant tank incorporated in both front-end inverter and AC VRMs can make the output short-circuit-proof easy. In the incident of short-circuit on board, the voltages across all the windings of the main transformer do not collapse.

5.4 SUGGESTIONS FOR FUTURE WORK

Today, HFAC DPS cannot be widely accepted in desktop PC applications because some potential problems have not been solved. To make HFAC DPS more viable and attractive, more research works are required on the following issues.

(i) System integration. A systematic design must be developed to optimize the high frequency power distribution layout, so that its electrical performance and power density can be maximized, and meanwhile, the dynamic interactions between the converter modules can be minimized.

(ii) Paralleling of the front-end inverter. In order to provide a redundant power system, the front-end inverter can be replaced by the paralleled inverter modules. However, this is difficult to be implemented in the ac bus environment due to the requirement of precise synchronization and impedance matching.

(iii) Advanced AC VRM topology. Instead of using the input ac switch to regulate the output voltage, research can be focused on developing a new topology using the synchronizing switches to perform output regulation and rectification at the same time. This new topology can reduce the component counts, thereby increasing the system efficiency and reliability, and resulting in more real-estate on the PCB.

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APPENDIX A

APWM RESONANT INVERTER: EQUATIONS USED TO SELECT THE INTEGRAL TIME CONSTANT OF THE FEEDFORWARD CONTROL LOOP

In order to derive the equations in section 2.5.4, which are used to select the integral time constant of the feedforward control loop of the APWM resonant inverter, the modulation wave (output of the integrator v_{int}), the carrier wave v_c, and the corresponding gating signal of switch S_1 are redrawn in Fig. A-1.

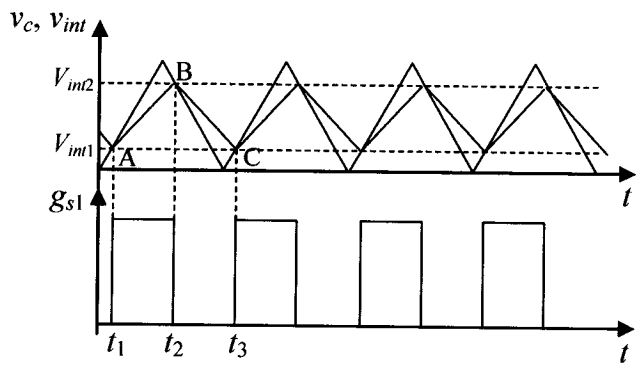


Fig. A-1: Modulation wave, carrier wave, and gating signal

According to the feedforward control loop diagram shown in Fig. 2-30, the modulation wave v_{int} can be expressed as:

$$v_{int} = \frac{1}{\tau}\int_{t_0}^{t}(K_s v_{s2} - v_{ae})dt + V_{int,0} \qquad \text{(A-1)}$$

Where τ is the time constant of the integrator, v_{s2} is the output of the chopper, and v_{ae} is the output of the type-II error amplifier. $V_{int,0}$ is the initial value of v_{int} at time $t = t_0$.

Therefore, the value of v_{int} at time $t = t_2$ and $t = t_3$ respectively can be found by (A-2a) and (A-2b):

$$V_{int2} = V_{int1} + \frac{1}{\tau}(K_s V_d - v_{ae})DT_s \tag{A-2a}$$

$$V_{int1} = V_{int2} + \frac{1}{\tau}(-v_{ae})(1-D)T_s \tag{A-2b}$$

Where D is the duty cycle of switch S_1 and T_s is the switching period.

On the other hand, curves AB and BC can also be expressed by the linear equations (A-3a) and (A-3b) respectively:

$$V_{int2} = V_{int1} + K_1(t_2 - t_1) \tag{A-3a}$$

$$V_{int1} = V_{int2} - K_2(t_3 - t_2) \tag{A-3b}$$

Where K_1 and K_2 are the absolute values of the slopes of curves AB and BC respectively.

Compare (A-2) and (A-3), K_1 and K_2 can be found out as:

$$K_1 = \frac{K_s V_d - v_{ae}}{\tau} \tag{A-4a}$$

$$K_2 = \frac{v_{ae}}{\tau} \tag{A-4b}$$

To derive the expression of duty cycle D, rearrange (A-2):

$$V_{int2} - V_{int1} = (K_s V_d - v_{ae})DT_s / \tau \tag{A-5a}$$

$$V_{int2} - V_{int1} = v_{ae}(1-D)T_s / \tau \tag{A-5b}$$

Then,

$$(K_s V_d - v_{ae})D = v_{ae}(1-D) \tag{A-5c}$$

Therefore, the duty cycle D can be defined as:

$$D = \frac{v_{ae}}{K_s V_d} \tag{A-6}$$

APPENDIX B

APWM RESONANT INVERTER: DERIVATION OF CONTROL-TO-OUTPUT TRANSFER FUNCTION

To determine the appropriate compensation in the feedback loop for the desired steady-state and transient response, the dynamic model of the circuit is developed as shown in Fig. 2-31, redrawn as Fig. B-1.

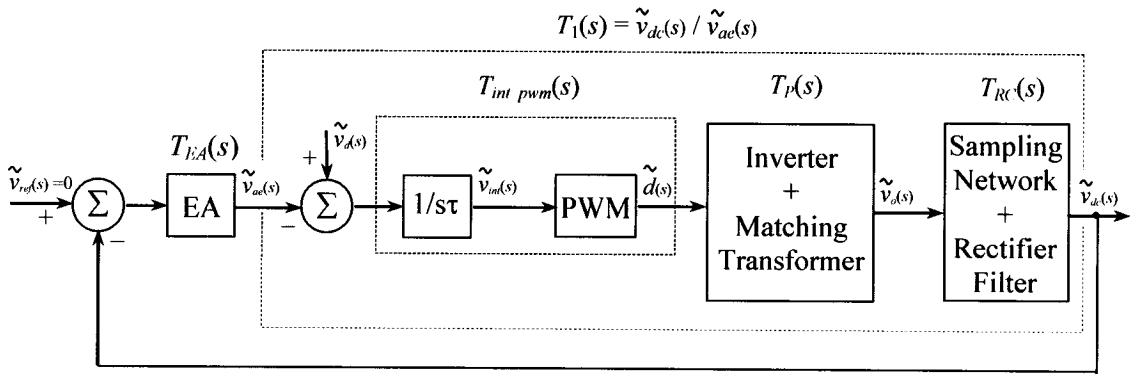


Fig. B-1: Dynamic model of the APWM inverter

In Fig. B-1, each block can be represented by a transfer function. The overall open-loop transfer function is:

$$T_{OL}(s) = T_{EA}(s)T_1(s) \tag{B-1}$$

Where $T_{EA}(s)$ is the transfer function of the compensated error amplifier, and $T_1(s)$ is the control-to-output transfer function of the inverter, which is defined as the transfer function between the output of the feedback rectifier v_{dc} and the output of the error amplifier v_{ae}:

$$T_1(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{v}_{ae}(s)} \tag{B-2}$$

Where the superscript "~" denotes a small perturbation from the nominal.

As seen from Fig. B-1, $T_1(s)$ consists of three dynamic function blocks:

$$T_1(s) = T_{int\_pwm}(s)T_p(s)T_{RC}(s) \tag{B-3}$$

Where $T_{int\_pwm}(s)$ is the transfer function of the feedforward integrator and the pulse-width-modulator. $T_p(s)$ is the transfer function of the APWM inverter including the matching transformer. $T_{RC}(s)$ is the transfer function of the sampling network and the feedback rectifier including the output RC filter. The derivation of each transfer function is described as follows.

B.1 TRANSFER FUNCTION OF THE POWER STAGE OF THE APWM INVERTER

To derive the transfer function of the power stage of the APWM resonant inverter, the power circuit of the APWM inverter is redrawn in Fig. B-2.

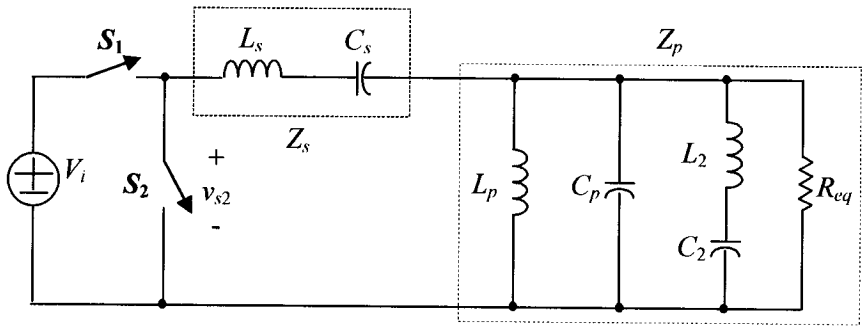


Fig. B-2: Power circuit of the APWM resonant inverter

In Fig. B-2, the output voltage of the inverter is given by:

$$v_o = \frac{v_{s2}}{N}\frac{Z_p}{Z_s + Z_p} \tag{B-4}$$

Where N is the turns ratio of the high frequency matching transformer. v_{s2} is the chopper output voltage, which is a function of the DC input voltage V_d and duty cycle D given by (2-11). Z_s is the impedance of the series resonant tank. Z_p is the total impedance of the

parallel resonant tank and the equivalent load resistance. The impedance of the 2nd harmonic trap can be ignored because it has contribution on the circuit frequency characteristics only around 2 MHz.

Now let the duty cycle be perturbed from D to $d(t) = D + \tilde{d}(t)$, but assume for simplicity that the input voltage V_d is constant. The goal of the feedforward control is to keep the average value of v_{s2} (which is equal to DV_d) constant against any disturbance by changing duty cycle D. Thus the dynamic model of the feedforward-controlled chopper can be expressed as:

$$\tilde{v}_{s2}(s)/\tilde{d}(s) = V_d \tag{B-5}$$

Since the resonant tanks and second harmonic trap are LTI (linear time invariant), their dynamic model can be expressed directly by their Laplace form. Therefore, the desired transfer function of the power stage of the inverter can be written as:

$$T_p(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_d}{N}\frac{1}{1 + Z_s(s)/Z_p(s)} \tag{B-6}$$

The Bode plot of (B-6) is shown in Fig. B-3 ① and ②.

B.2 TRANSFER FUNCTION OF THE SAMPLING NETWORK AND FEEDBACK RECTIFIER

The sampling network has a gain K_s equal to 0.1. The output filter of the feedback rectifier, which consists of a capacitor C_1 and a discharging resistor R_1, introduces a pole at frequency $f_{RC} = 1/(2\pi R_1 C_1) = 318$ kHz, and has the DC gain equal to 1.

Therefore, the transfer function of the sampling network and feedback rectifier is:

$$T_{RC}(s) = \frac{K_s}{1 + sR_1C_1} \tag{B-7}$$

The Bode plot of (B-7) is shown in Fig. B-3 ③.

B.3 TRANSFER FUNCTION OF THE FEEDFORWARD INTEGRATOR AND PWM

The transfer function of the integrator is known as $1/(\tau s)$. The gain of the pulse-width-modulator (PWM) is defined by $G_{pwm} = \tilde{d}(s)/\tilde{v}_{\text{int}}(s)$.

As derived in Appendix A, the rising slope of the output of the integrator is $K_1 = (K_s V_d - v_{ae})/\tau$, and the duty cycle D can be defined as $D = v_{ae}/(K_s V_d)$. Thus the small perturbation of K_1 can be written as:

$$\tilde{K}_1 = -\frac{\tilde{v}_{ae}}{\tau} = -\frac{K_s V_d \tilde{d}}{\tau} \tag{B-8}$$

Therefore, the perturbation at the output of the integrator can be found out by (A-3a) as:

$$\tilde{v}_{\text{int}} = \tilde{K}_1 D T_s = -\frac{K_s V_d \tilde{d}}{\tau} D T_s \tag{B-9}$$

Rearrange (B-9), the transfer function G_{pwm} can be obtained:

$$G_{pwm} = -\frac{1}{K_s V_d} \frac{\tau}{D T_s} \tag{B-10}$$

Because of the simplified assumption of constant input voltage V_d, $\tilde{v}_d(s)$ in Fig. B-1 is equal to zero. Therefore, the transfer function $T_{int\_pwm}(s)$ is given by:

$$T_{\text{int\_ pwm}}(s) = \frac{\tilde{d}(s)}{\tilde{v}_{\text{int}}(s)} \cdot \frac{\tilde{v}_{\text{int}}(s)}{-\tilde{v}_{ae}(s)} = -\frac{G_{pwm}}{\tau s} \tag{B-11}$$

The Bode plot of $T_{int\_pwm}(s)$ is shown in Fig. B-3 ④ and ⑤.

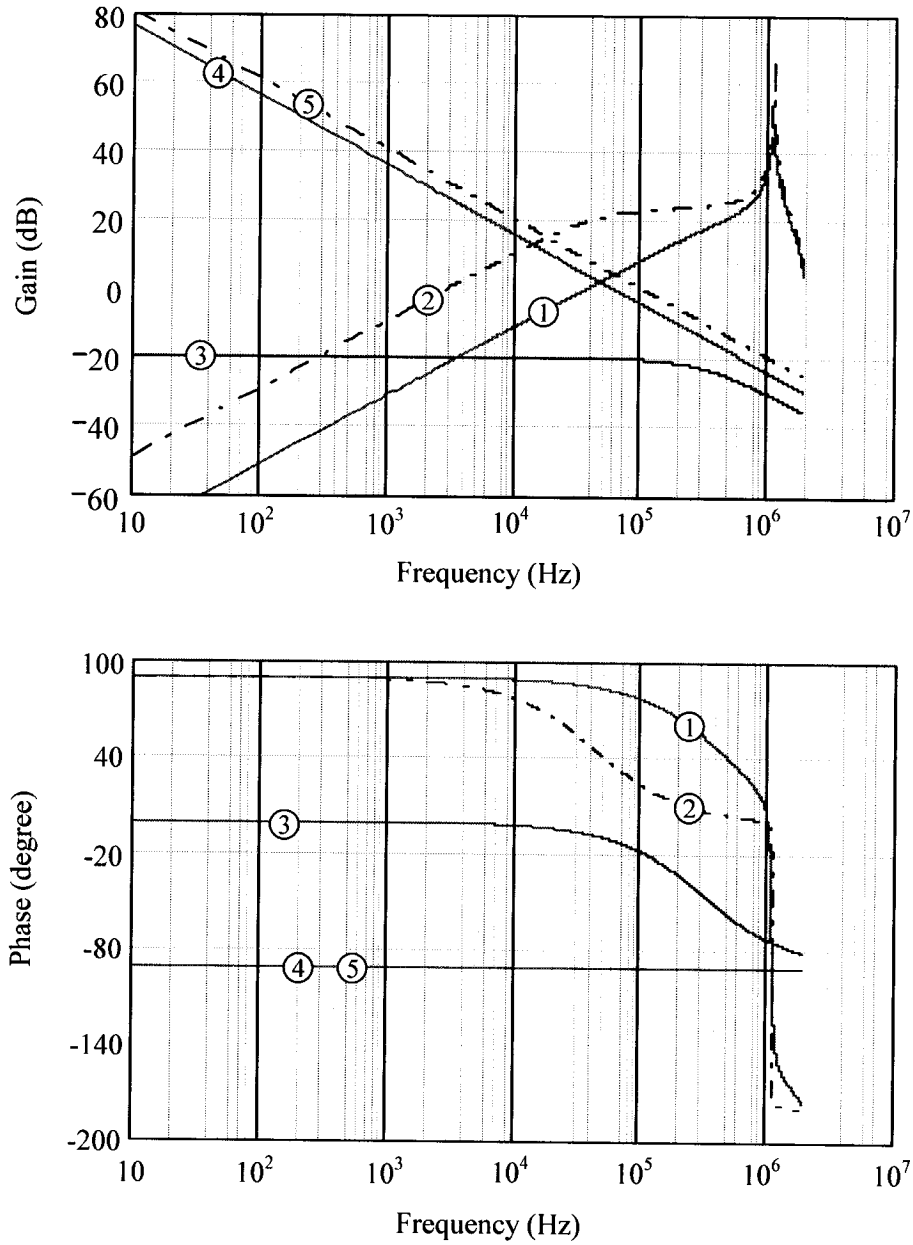


Fig. B-3: Bode plots of $T_p(s)$, $T_{RC}(s)$, and $T_{int\_pwm}(s)$

Traces:

①: $T_p(s)$ when V_d=60V & 100% load; ②: $T_p(s)$ when V_d=75V & 10% load;

③: $T_{RC}(s)$;

④: $T_{int\_pwm}(s)$ when V_d=60V & 100% load; ⑤: $T_{int\_pwm}(s)$ when V_d=75V & 10% load)

APPENDIX C

AC VRM: TRANSFORMER PRIMARY SIDE VOLTAGE WHEN NON-IDEAL TRANSFORMER AND SR ARE CONSIDERED

This Mathcad spread sheet is created to derive the transformer primary side voltage a its Fourier series when non-ideal transformer and SR are considered. The non-ideal factors taken into account in this derivation are listed in section 3.1.3.

C.1. Voltage waveform at the primary side of the transformer

Input voltage: $v_{in} := V_{pk}\cdot\sin(w_o\cdot t)$

Circuit parameters:

$V_{pk} := 28\cdot\sqrt{2}$ $V_o := 1.5$ $I_o := 5, 10..20$ $R_{load}(I_o) := \frac{V_o}{I_o}$

$w_o := 2\cdot\pi\cdot 10^6$ $d := 0, 0.02..1$ $N := \frac{\pi}{4}\cdot\frac{V_{pk}}{V_o + 0.075}$ $N = 19.746$

$L_s := 2.5\cdot 10^{-6}$ $C_s := 10\cdot 10^{-9}$ $C_{ds} := 2000\cdot 10^{-12}$

$R_{eq}(I_o) := \frac{8}{\pi^2}\cdot N^2\cdot R_{load}(I_o)$ $C_{eq}(d) := \frac{C_{ds}\cdot C_s}{C_{ds} + C_s}\cdot(1 - d) + C_s\cdot d$

$L_m := 75\cdot 10^{-6}$ $V_d := 0.7$ $L_{leak} := 1.5\cdot 10^{-9}$ $L := L_s + N^2\cdot L_{leak}$

$u := 10^{-6}$ $t := 0, 0.003\cdot u..1\cdot u$ $j := \sqrt{-1}$

$t_1 := 0.032\cdot u$ $t_2 := 0.468\cdot u$ $t_3 := 0.532\cdot u$ $t_4 := 0.968\cdot u$

Fundamental impedance:

$$Z_1(I_o, d) := \frac{j\cdot R_{eq}(I_o)\cdot w_o\cdot L_m}{R_{eq}(I_o) + j\cdot w_o\cdot L_m} + j\cdot\left(w_o\cdot L - \frac{1}{w_o\cdot C_{eq}(d)}\right)$$

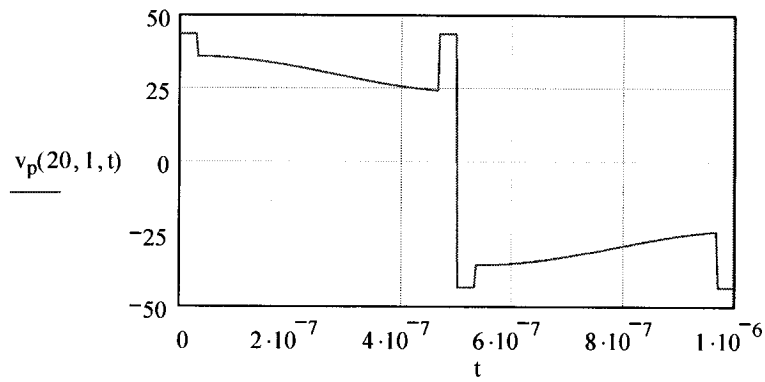
Fundamental resonant current in time domain:

$$DPF(I_o, d) := \frac{Re(Z_1(I_o, d))}{|Z_1(I_o, d)|} \qquad \alpha(Io, d) := \text{acos}(DPF(Io, d))$$

$$i_{r1}(I_o, d, t) := \frac{V_{pk}}{|Z_1(I_o, d)|}\cdot\sin(w_o\cdot t - \alpha(I_o, d))$$

Voltage at the primary side of the transformer:

$$v_p(I_o,d,t) := \begin{cases} N\cdot(V_d + V_o) & \text{if } 0 \le t < t_1 \\ N\cdot\left[L_{leak}\cdot\frac{d}{dt}\left(i_{r1}(I_o,d,t)\cdot N\right) + V_o\right] & \text{if } t_1 \le t < t_2 \\ N\cdot(V_d + V_o) & \text{if } t_2 \le t < 0.5\cdot u \\ -N\cdot(V_d + V_o) & \text{if } 0.5\cdot u \le t < t_3 \\ N\cdot\left[L_{leak}\cdot\left[\frac{d}{dt}\left(i_{r1}(I_o,d,t)\cdot N\right)\right] - V_o\right] & \text{if } t_3 \le t < t_4 \\ -N\cdot(V_d + V_o) & \text{if } t_4 \le t \le 1\cdot u \end{cases}$$

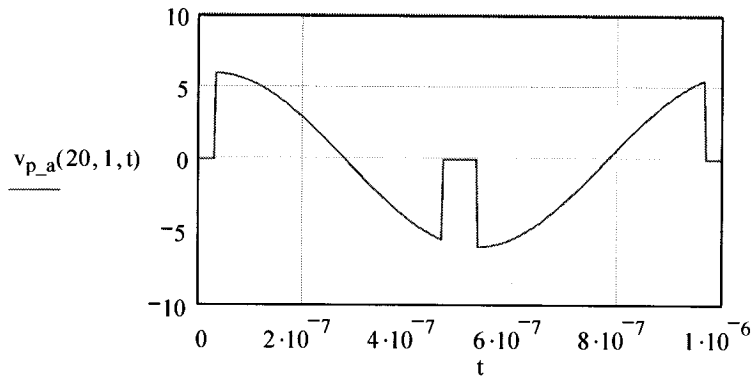


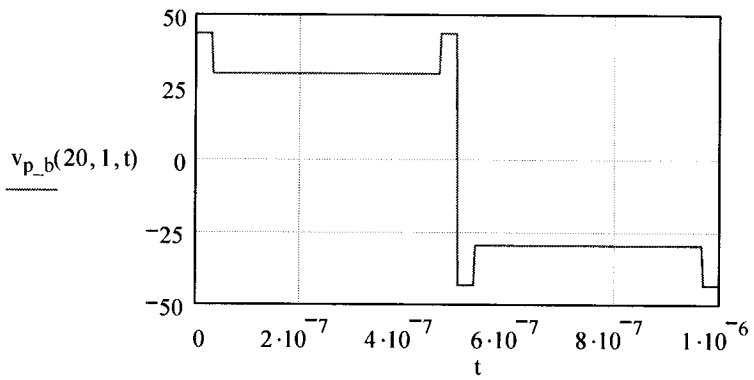
C.2. Representation of v_p by its Fourier Series

Equation of v_p can be seen as the sum of an even function v_{p_a} and an odd function v_{p_b}:

$$v_{p\_a}(I_o,d,t) := \begin{cases} 0 & \text{if } 0 \le t < t_1 \\ N\cdot\left[L_{leak}\cdot\left[\frac{d}{dt}\left(i_{r1}(I_o,d,t)\cdot N\right)\right]\right] & \text{if } t_1 \le t < t_2 \\ 0 & \text{if } t_2 \le t < 0.5\cdot u \\ 0 & \text{if } 0.5\cdot u \le t < t_3 \\ N\cdot\left[L_{leak}\cdot\left[\frac{d}{dt}\left(i_{r1}(I_o,d,t)\cdot N\right)\right]\right] & \text{if } t_3 \le t < t_4 \\ 0 & \text{if } t_4 \le t \le 1\cdot u \end{cases}$$

$$v_{p\_b}(I_o,d,t) := \begin{cases} N\cdot(V_d + V_o) & \text{if } 0 \le t < t_1 \\ N\cdot(V_o) & \text{if } t_1 \le t < t_2 \\ N\cdot(V_d + V_o) & \text{if } t_2 \le t < 0.5\cdot u \\ -N\cdot(V_d + V_o) & \text{if } 0.5\cdot u \le t < t_3 \\ N\cdot(-V_o) & \text{if } t_3 \le t < t_4 \\ -N\cdot(V_d + V_o) & \text{if } t_4 \le t \le 1\cdot u \end{cases}$$





C.2.1 The Fourier Transform of the voltage v_{p_a}:

$$v_{p\_a} = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cdot \cos(n \cdot x)$$

Where $x = w_o \cdot t$ $\qquad an = \frac{2}{\pi} \cdot \int_0^{\pi} f(x) \cdot \cos(n \cdot x)\, dx$

$$a_n = \frac{2}{\pi} \cdot \int_a^b \left(N^2 \cdot L_{leak} \cdot \frac{d}{dt} i_{r1} \right) \cdot \cos(n \cdot x)\, dx = k \cdot \int_a^b \left(\frac{d}{dt} i_{r1} \right) \cdot \cos(n \cdot x)\, dx$$

Where

$a := 0.064 \cdot \pi$ $\qquad b := 0.936 \cdot \pi$ $\qquad k := \frac{2}{\pi} \cdot N^2 \cdot L_{leak}$

Assume that $\qquad \frac{d}{dt} i_{r1} = A \cdot (B \cdot \cos(x) + C \cdot \sin(x))$

Then

$$A(I_o,d) := \frac{-V_{pk}\cdot w_o^{\,2}\cdot C_{eq}(d)}{R_{eq}(I_o)^2\cdot C_{eq}(d)^2\cdot w_o^{\,2} + w_o^{\,4}\cdot L^2\cdot C_{eq}(d)^2 - 2\cdot w_o^{\,2}\cdot L\cdot C_{eq}(d) + 1}$$

$$B(I_o,d) := -w_o\cdot C_{eq}(d)\cdot R_{eq}(I_o) \qquad C(d) := 1 - w_o^{\,2}\cdot C_{eq}(d)\cdot L$$

Furthermore, $\int_a^b \left(\frac{d}{dt} i_{r1}\right)\cdot\cos(n\cdot x)\,dx$ can be written as:

$$\int_a^b (B\cdot\cos(x) + C\cdot\sin(x))\cdot\cos(n\cdot x)\,d(x) = E + F$$

$$E(I_o,d,n) := \frac{B(I_o,d)}{2}\cdot\left[\frac{1}{n+1}\cdot(\sin(n\cdot b + b) - \sin(n\cdot a + a)) + \frac{1}{n-1}\cdot(\sin(n\cdot b - b) - \sin(n\cdot a - a))\right.$$

$$F(d,n) := \frac{C(d)}{2}\cdot\left[\frac{1}{n+1}\cdot(\cos(n\cdot a + a) - \cos(n\cdot b + b)) + \frac{1}{n-1}\cdot(\cos(n\cdot b - b) - \cos(n\cdot a - a))\right]$$

Therefore, a_n (n=0,2,3,4,5...) can be found as:

$$K(I_o,d) := A(I_o,d)\cdot k$$

$$a_n(I_o,d,n) := K(I_o,d)\cdot(E(I_o,d,n) + F(d,n))$$

When n=1, a_n is derived by:

$$E_1(I_o,d) = \lim_{n\to 1}\frac{B}{2}\cdot\left[\frac{1}{n+1}\cdot(\sin(n\cdot b + b) - \sin(n\cdot a + a)) + \frac{1}{n-1}\cdot(\sin(n\cdot b - b) - \sin(n\cdot a - a))\right]$$

$$E_1(I_o,d) := \frac{-1}{4}\cdot B(I_o,d)\cdot(-\sin(2\cdot b) + \sin(2\cdot a) - 2\cdot b + 2\cdot a)$$

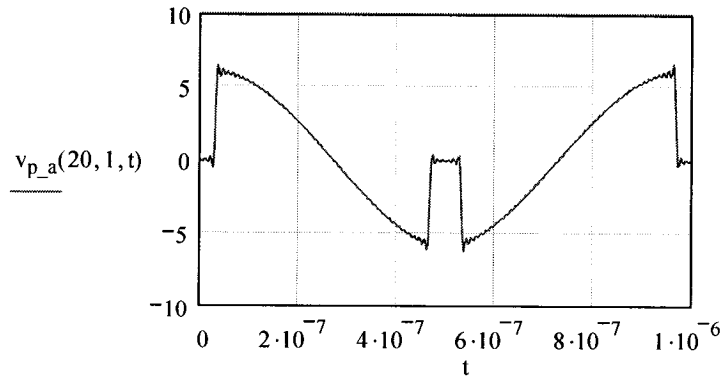
$$F_1(d) = \lim_{n\to 1}\frac{C}{2}\cdot\left[\frac{1}{n+1}\cdot(\cos(n\cdot a + a) - \cos(n\cdot b + b)) + \frac{1}{n-1}\cdot(\cos(n\cdot b - b) - \cos(n\cdot a - a))\right]$$

$$F_1(d) := \frac{1}{4}\cdot C(d)\cdot(\cos(2\cdot a) - \cos(2\cdot b))$$

$$a_1(I_o,d) := K(I_o,d)\cdot(E_1(I_o,d) + F_1(d))$$

Finally, the voltage v_{p_a} can be expressed by its Fourier series as:

$$v_{p\_a}(I_o, d, t) := \frac{a_n(I_o, d, 0)}{2} + a_1(I_o, d)\cdot\cos(w_o\cdot t) + \sum_{n=2}^{100} a_n(I_o, d, n)\cdot\cos(n\cdot w_o\cdot t)$$



C.2.2 The Fourier Transform of the voltage Vp_b:

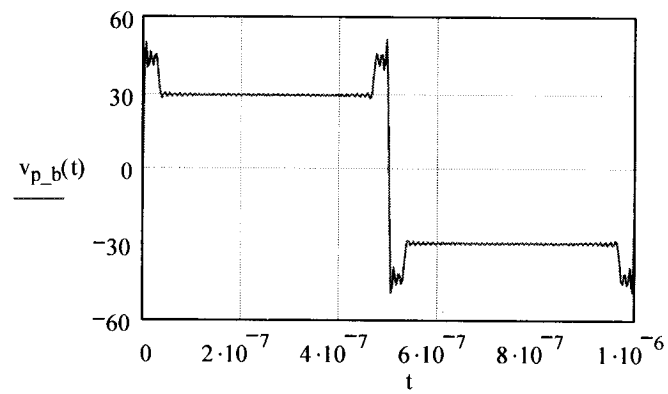
$$v_{p\_b} = \sum_{n=1}^{\infty} b_n\cdot\sin(n\cdot x)$$

Where $$b_n = \frac{2}{\pi}\cdot\int_o^{\pi} f(x)\cdot\sin(n\cdot x)\,dx$$

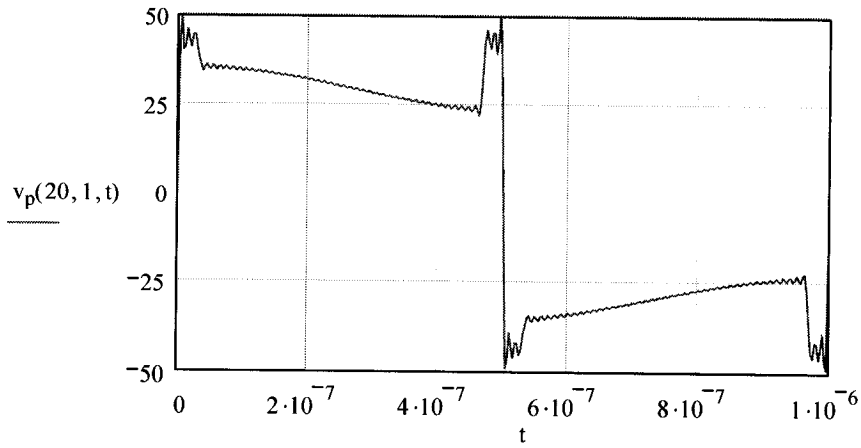
$$b_n = \frac{2}{\pi}\cdot\left[\int_0^a N\cdot(V_d + V_o)\cdot\sin(n\cdot x)\,dx + \int_a^b N\cdot V_o\cdot\sin(n\cdot x)\,dx + \int_b^{\pi} N\cdot(V_d + V_o)\cdot\sin(n\cdot x)\,dx\right]$$

$$b_n(n) := \frac{2}{\pi}\cdot\frac{N}{n}\cdot(V_o + V_d)\cdot(1 - \cos(n\cdot\pi)) + \frac{2}{\pi}\cdot\frac{N}{n}\cdot V_d\cdot(\cos(b\cdot n) - \cos(a\cdot n))$$

$$v_{p\_b}(t) := \sum_{n=1}^{100} b_n(n)\cdot\sin(n\cdot w_o\cdot t)$$



$$v_p(I_o,d,t) := v_{p\_a}(I_o,d,t) + v_{p\_b}(t)$$



C.3. Waveform of the resonant current

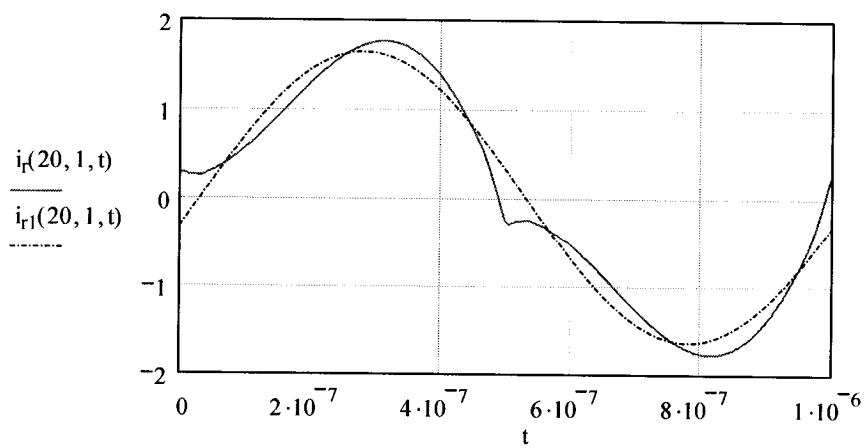
Therefore, the harmonics of the resonant current can be derived as:

$$\beta(n,t) := n\cdot w_o\cdot t - \frac{\pi}{2}$$

$$i_n(I_o,d,t) := \sum_{n=2}^{50} \frac{1}{\left| n\cdot w_o\cdot L - \frac{1}{n\cdot w_o\cdot C_{eq}(d)} \right|} \cdot \left(a_n(I_o,d,n)\cdot\cos(\beta(n,t)) + b_n(n)\cdot\sin(\beta(n,t))\right)$$

The waveform of the resonant current at the rated load:

$$i_r(I_o,d,t) := -i_n(I_o,d,t) + i_{r1}(I_o,d,t)$$



APPENDIX D

PSPICE MODELS

D.1 PSpice model of the APWM resonant inverter

The PSpice circuit schematic of the proposed APWM resonant inverter is shown in Fig. D-1. In Fig. D-1, the transformer is modeled by two coupled inductors. The dynamic load is modeled by a switch in series with a resistance, so that this part of load can be connected or disconnected at any certain time. The dynamic input dc voltage is modeled by a piecewise-linear voltage source. The error amplifier is modeled by a voltage-controlled-voltage source with a gain of 10^{20}. The PSpice models of all the components and simulation settings in Fig. D-1 are described following the circuit schematic.

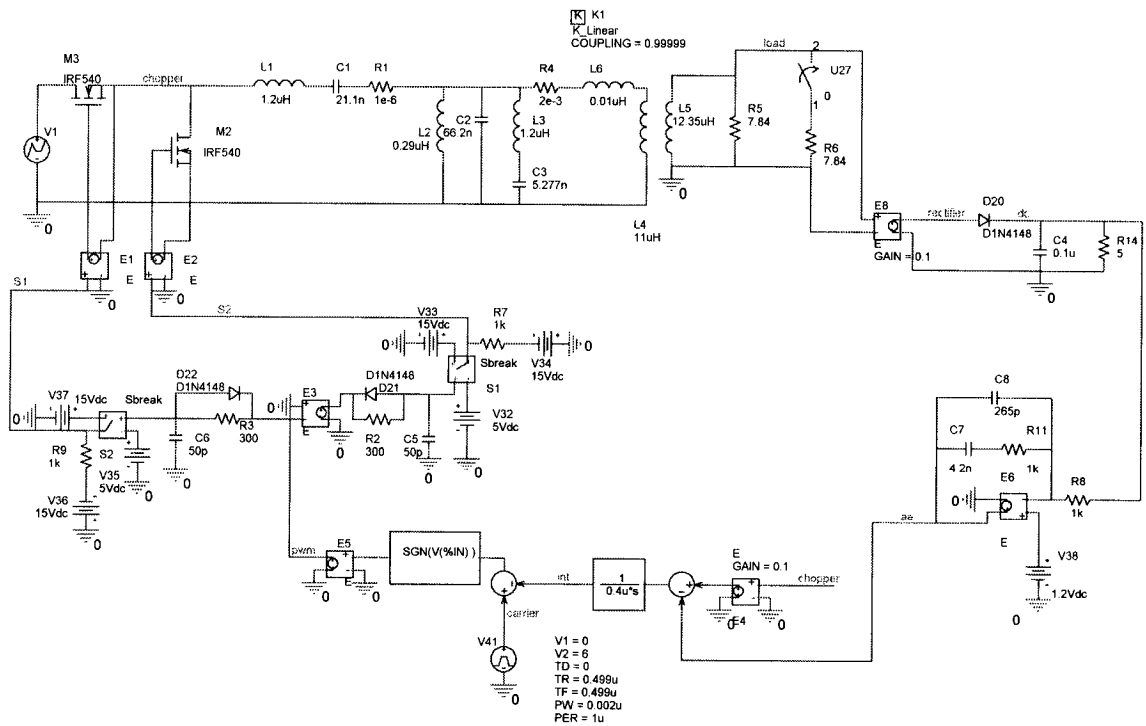


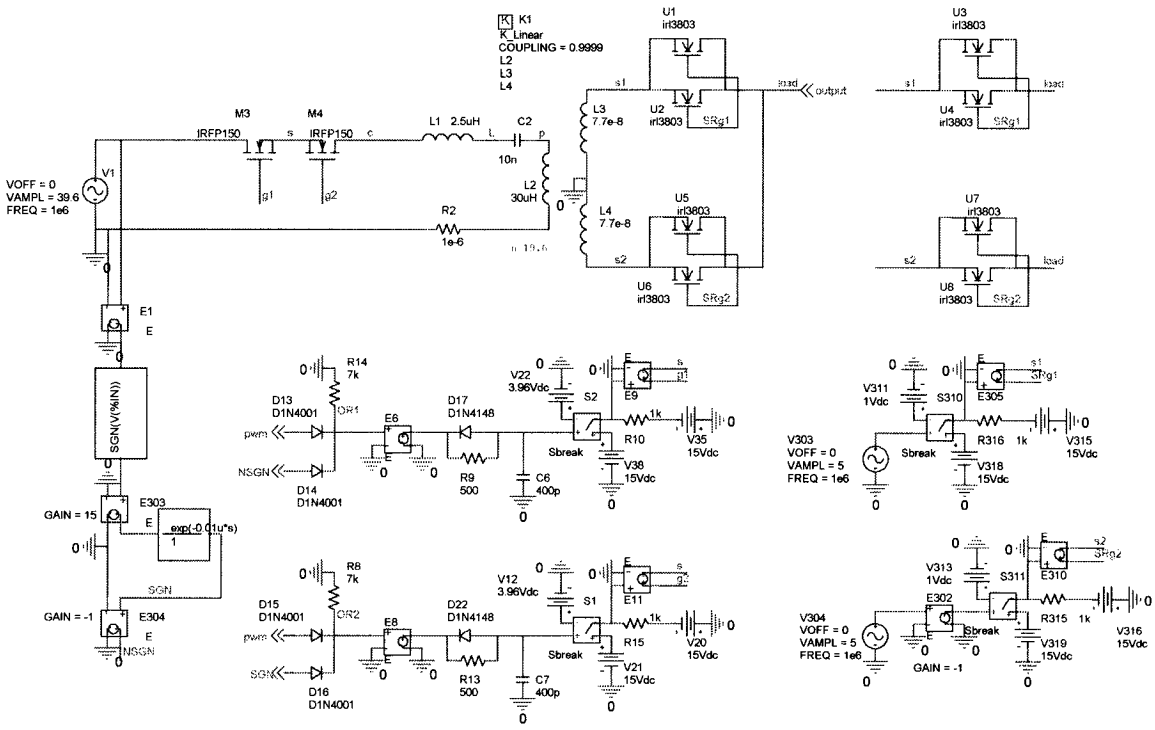
Fig. D-1: PSpice circuit schematic of the APWM resonant inverter

```
**** 10/18/03 05:22:12 ******** PSpice 9.2.3 (Jan 2002) ******* ID#
251265024

 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\modulatedint-schematic1-trans.sim ]

 ****     CIRCUIT DESCRIPTION
******************************************************************************
** Creating circuit file "modulatedint-schematic1-trans.sim.cir"
** WARNING: THIS AUTOMATICALLY GENERATED FILE MAY BE OVERWRITTEN BY
SUBSEQUENT SIMULATIONS

*Libraries:
* Local Libraries :
* From [PSPICE NETLIST] section of
E:\Cadence\Orcad_9.2.3\tools\PSpice\PSpice.ini file:
.lib "E:\Cadence\Orcad_9.2.3\tools\capture\library\pspice\mymos.lib"
.lib "nom.lib"

.subckt SCHEMATIC1_S1 1 2 3 4
S_S1         3 4 1 2 Sbreak
RS_S1         1 2 1G
.ends SCHEMATIC1_S1

.subckt SCHEMATIC1_S2 1 2 3 4
S_S2         3 4 1 2 Sbreak
RS_S2         1 2 1G
.ends SCHEMATIC1_S2

**** RESUMING modulatedint-schematic1-trans.sim.cir ****
.END

**** 10/18/03 05:22:12 ******** PSpice 9.2.3 (Jan 2002) ******* ID#
251265024
 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\modulatedint-schematic1-trans.sim ]
 ****     Diode MODEL PARAMETERS
******************************************************************************
               D1N4148
          IS    2.682000E-09
           N    1.836
         ISR    1.565000E-09
         IKF     .04417
          BV  100
         IBV  100.000000E-06
          RS     .5664
          TT   11.540000E-09
         CJO    4.000000E-12
          VJ     .5
           M     .3333
**** 10/18/03 05:22:12 ******** PSpice 9.2.3 (Jan 2002) ******* ID#
251265024

 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\modulatedint-schematic1-trans.sim ]
 ****     MOSFET MODEL PARAMETERS
******************************************************************************
```

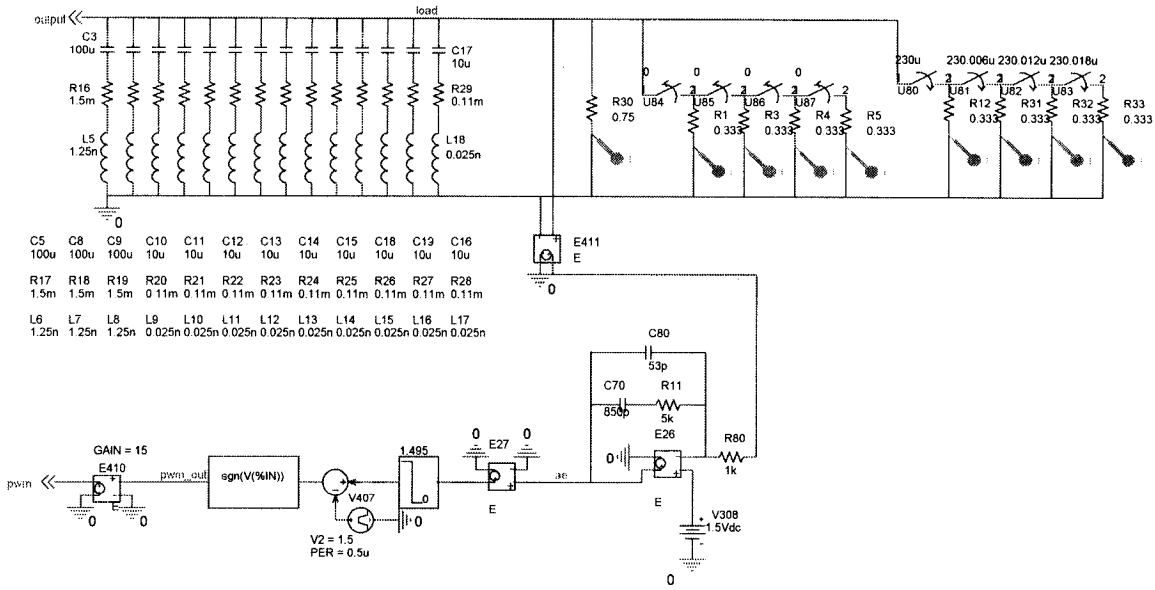
```
            IRF540
            NMOS
      LEVEL    3
          L    2.000000E-06
          W     .94
        VTO    3.136
         KP   20.710000E-06
      GAMMA    0
        PHI     .6
     LAMBDA    0
         RD     .02252
         RS     .02134
         RG    5.557
        RDS  444.400000E+03
         IS    2.859000E-12
         JS    0
         PB     .8
       PBSW     .8
        CBD    2.408000E-09
         CJ    0
       CJSW    0
         TT  142.000000E-09
       CGSO    1.153000E-09
       CGDO  445.700000E-12
       CGBO    0
        TOX  100.000000E-09
         XJ    0
      UCRIT   10.000000E+03
      DELTA    0
        ETA    0
     DIOMOD    1
        VFB    0
       LETA    0
       WETA    0
         U0    0
       TEMP    0
        VDD    0
      XPART    0

**** 10/18/03 05:22:12 ******** PSpice 9.2.3 (Jan 2002) ******* ID#
251265024

 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\modulatedint-schematic1-trans.sim ]

 ****     Voltage Controlled Switch MODEL PARAMETERS
*******************************************************************************
               X_U27.Smod      Sbreak
        RON    1.000000E-06    1
       ROFF    1.000000E+06    1.000000E+06
        VON    1               1
       VOFF    0               0
*******************************************************************************
```

D.2 PSpice model of the PWM AC VRM

The PSpice circuit schematic of the proposed PWM AC VRM is shown in Fig. D-2. Fig. D-2(a) shows the circuit schematic of the input stage, synchronous rectifier, and the control circuits of the ac switch and SR. The center-tapped transformer is modeled by three coupled inductors. Fig. D-2(b) shows circuit schematic of the output stage including output capacitor bank, dynamic load, and feed back control loop. The di/dt slew rate of the dynamic load is determined by the settings of the switches which connect or disconnect the parallel load resistance. The PSpice models of all the components and simulation settings in Fig. D-2 are shown following the circuit schematic.



(a) Circuit schematic of the input stage and synchronous rectifier



(b) Circuit schematic of the output stage

Fig. D-2: PSpice circuit schematic of the PWM AC VRM

```
**** 10/18/03 06:02:35 ******** PSpice 9.2.3 (Jan 2002) ******* ID#
251265024
 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\pwmclose-schematic1-trans.sim ]
 ****     CIRCUIT DESCRIPTION
******************************************************************************
** Creating circuit file "pwmclose-schematic1-trans.sim.cir"
** WARNING: THIS AUTOMATICALLY GENERATED FILE MAY BE OVERWRITTEN BY
SUBSEQUENT SIMULATIONS

*Libraries:
* Local Libraries :
* From [PSPICE NETLIST] section of
E:\Cadence\Orcad_9.2.3\tools\PSpice\PSpice.ini file:
.lib "E:\Cadence\Orcad_9.2.3\tools\capture\library\pspice\mymos.lib"
.lib "nom.lib"

.subckt SCHEMATIC1_S311 1 2 3 4
S_S311          3 4 1 2 Sbreak
RS_S311          1 2 1G
.ends SCHEMATIC1_S311

.subckt SCHEMATIC1_S2 1 2 3 4
S_S2          3 4 1 2 Sbreak
RS_S2          1 2 1G
.ends SCHEMATIC1_S2

.subckt SCHEMATIC1_S310 1 2 3 4
S_S310          3 4 1 2 Sbreak
```

```
RS_S310         1 2 1G
.ends SCHEMATIC1_S310

.subckt SCHEMATIC1_S1 1 2 3 4
S_S1         3 4 1 2 Sbreak
RS_S1         1 2 1G
.ends SCHEMATIC1_S1

**** RESUMING pwmclose-schematic1-trans.sim.cir ****
.END
**** 10/18/03 06:02:35 ******** PSpice 9.2.3 (Jan 2002) ******* ID#
251265024
 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\pwmclose-schematic1-trans.sim ]

 ****     Diode MODEL PARAMETERS
********************************************************************************
               D1N4001          D1N4148          X_U1.MD          X_U1.MD1
          IS   14.110000E-09     2.682000E-09     1.167120E-09     0
           N    1.984            1.836            1.29042         50
         ISR                     1.565000E-09
         IKF   94.81              .04417
          BV   75               100               30
         IBV   10.000000E-06    100.000000E-06   250.000000E-06
          RS     .03389           .5664            4.017390E-03
          TT    5.700000E-06     11.540000E-09
         CJO   25.890000E-12     4.000000E-12     3.471910E-09
9.079660E-09
          VJ     .3245            .5               2.9757           .5
           M     .44              .3333             .625265
.617379
          FC
10.000000E-09
          EG                                       1.2
         XTI                                       3.24829
               X_U1.MD2         X_U1.MD3         X_U2.MD          X_U2.MD1
          IS  100.000000E-12   100.000000E-12     1.167120E-09     0
           N     .4               .4               1.29042         50
          BV                                      30
         IBV                                     250.000000E-06
          RS    3.000000E-06                       4.017390E-03
         CJO                                       3.471910E-09
9.079660E-09
          VJ                                       2.9757           .5
           M                                        .625265
.617379
          FC
10.000000E-09
          EG                                       1.2
         XTI                                       3.24829

**** 10/18/03 06:02:35 ******** PSpice 9.2.3 (Jan 2002) ******* ID#
251265024

 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\pwmclose-schematic1-trans.sim ]
```

```
 ****     MOSFET MODEL PARAMETERS
******************************************************************************
               IRFP150          X_U1.MM          X_U2.MM          X_U6.MM
               NMOS             NMOS             NMOS             NMOS
       LEVEL    3                1                1                1
           L    2.000000E-06  100.000000E-06  100.000000E-06
100.000000E-06
           W    2             100.000000E-06  100.000000E-06
100.000000E-06
         VTO    3.15             2.32277          2.32277          2.32277
          KP   20.790000E-06  104.12           104.12           104.12
       GAMMA    0                0                0                0
         PHI     .6               .6               .6               .6
      LAMBDA    0                0                0                0
          RD     .01737
          RS     .02003
          RG    6.223
         RDS  444.400000E+03
          IS    2.843000E-12     0                0                0
          JS    0                0                0                0
          PB     .8               .8               .8               .8
        PBSW     .8               .8               .8               .8
         CBD    4.541000E-09
          CJ    0                0                0                0
        CJSW    0                0                0                0
          TT  145.000000E-09
        CGSO    1.498000E-09   46.711200E-06   46.711200E-06
46.711200E-06
        CGDO  367.000000E-12   15.415500E-09   15.415500E-09
15.415500E-09
        CGBO    0                0                0                0
         TOX  100.000000E-09     0                0                0
          XJ    0                0                0                0
       UCRIT   10.000000E+03   10.000000E+03   10.000000E+03
10.000000E+03
       DELTA    0
         ETA    0
      DIOMOD    1                1                1                1
         VFB    0                0                0                0
        LETA    0                0                0                0
        WETA    0                0                0                0
          U0    0                0                0                0
        TEMP    0                0                0                0
         VDD    0                0                0                0
       XPART    0                0                0                0

        **** 10/18/03 06:02:35 ******** PSpice 9.2.3 (Jan 2002) *******
ID# 251265024
 ** Profile: "SCHEMATIC1-trans"  [ E:\mei\thesis\Appendix\PSpice
model\pwmclose-schematic1-trans.sim ]


 ****     Voltage Controlled Switch MODEL PARAMETERS
******************************************************************************
               X_U86.Smod       X_U83.Smod       X_U80.Smod
X_U87.Smod
```

RON	1.000000E-06	1.000000E-06	1.000000E-06	
1.000000E-06				
ROFF	1.000000E+06	1.000000E+06	1.000000E+06	
1.000000E+06				
VON	1	1	1	1
VOFF	0	0	0	0

	X_U81.Smod	X_U84.Smod	X_U85.Smod	
X_U82.Smod				
RON	1.000000E-06	1.000000E-06	1.000000E-06	
1.000000E-06				
ROFF	1.000000E+06	1.000000E+06	1.000000E+06	
1.000000E+06				
VON	1	1	1	1
VOFF	0	0	0	0

The PSpice circuit schematic of the proposed phase-shift-controlled AC VRM is shown in Fig. D-3. In Fig. D-3, the control angle is determined by a Laplace transfer function. The PSpice models of all the components and simulation settings are the same as those in Fig. D-2.

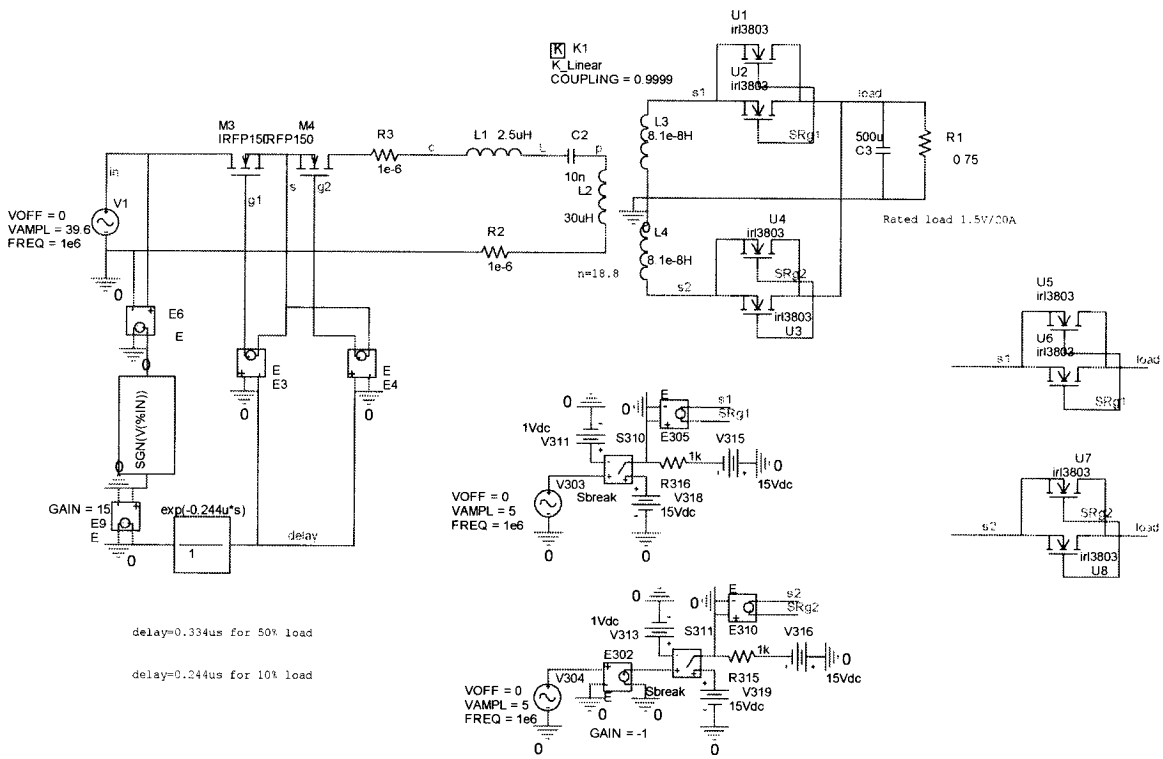


Fig. D-3: PSpice circuit schematic of phase-shift-controlled AC VRM

D.3 PSpice model of the HFAC distributed power system

The PSpice circuit schematic of the HFAC distributed power system of two-output application is shown in Fig. D-4. In Fig. D-4, the primary side is the power circuit of the APWM resonant inverter with an input filter. The sub-circuit of generating the gating signals of the chopper is the same as shown in Fig. D-1. The secondary side is two paralleled AC VRM. The sub-circuit of each AC VRM is the same as that shown in Fig. D-2, except that the input sinusoidal voltage source is replaced by the signal VRM1 or VRM2. The PSpice models of all the components and simulation settings are the same as those for Fig. D-2 and Fig. D-3.

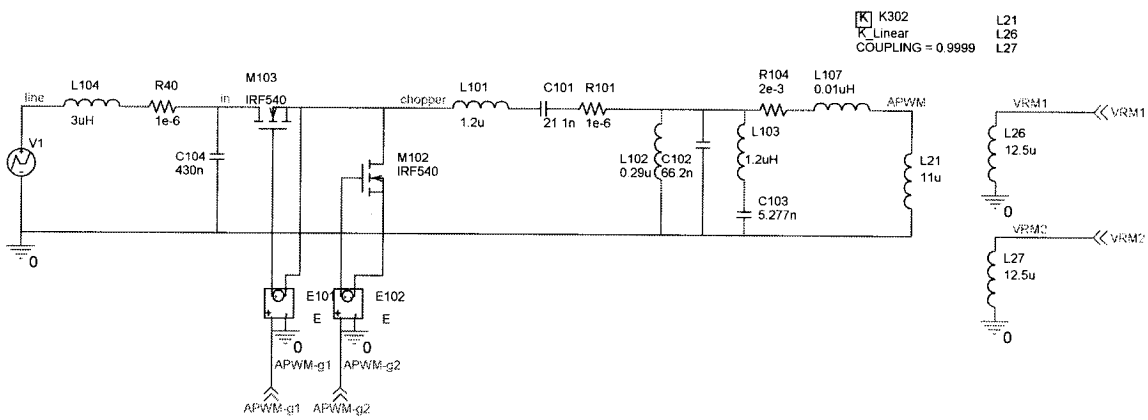


Fig. D-4: Circuit schematic of the HFAC DPS

APPENDIX E

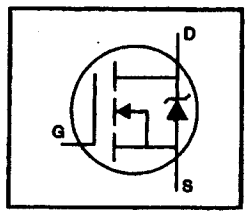
SPECIFICATIONS OF THE POWER SEMICONDUCTOR DEVICES

International IOR Rectifier

IRF540

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 100V

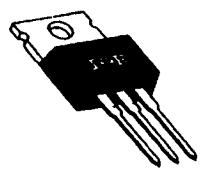
$R_{DS(on)}$ = 0.077Ω

I_D = 28A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	28	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	20	
I_{DM}	Pulsed Drain Current ①	110	
P_D @ T_C = 25°C	Power Dissipation	150	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	230	mJ
I_{AR}	Avalanche Current ①	28	A
E_{AR}	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.13	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.077	Ω	V_{GS}=10V, I_D=17A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	8.7	—	—	S	V_{DS}=50V, I_D=17A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=100V, V_{GS}=0V
		—	—	250		V_{DS}=80V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	72	nC	I_D=17A
Q_{gs}	Gate-to-Source Charge	—	—	11		V_{DS}=80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	32		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD}=50V
t_r	Rise Time	—	44	—		I_D=17A
$t_{d(off)}$	Turn-Off Delay Time	—	53	—		R_G=9.1Ω
t_f	Fall Time	—	43	—		R_D=2.9Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1700	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	560	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	120	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	28	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	T_J=25°C, I_S=28A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	180	360	ns	T_J=25°C, I_F=17A
Q_{rr}	Reverse Recovery Charge	—	1.3	2.8	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=25V, starting T_J=25°C, L=440μH R_G=25Ω, I_{AS}=28A (See Figure 12)

③ I_{SD}≤28A, di/dt≤170A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤175°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

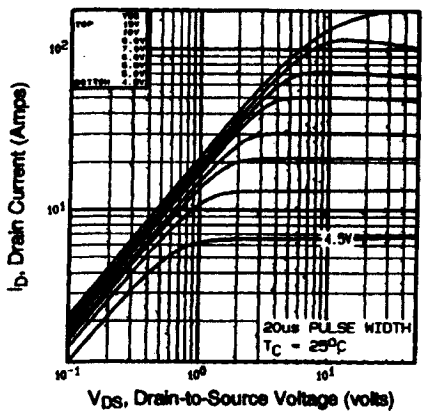


Fig 1. Typical Output Characteristics, T_C=25°C

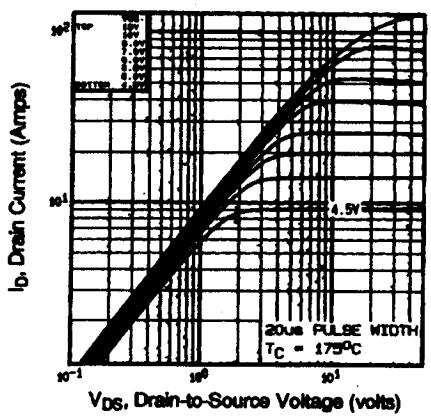


Fig 2. Typical Output Characteristics, T_C=175°C

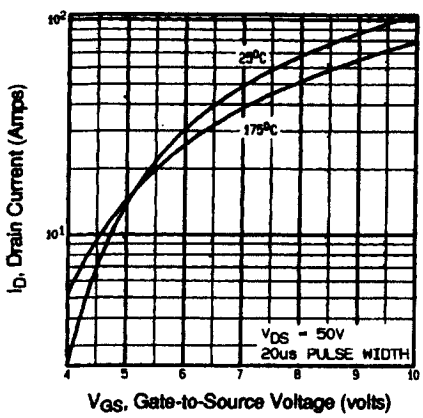


Fig 3. Typical Transfer Characteristics

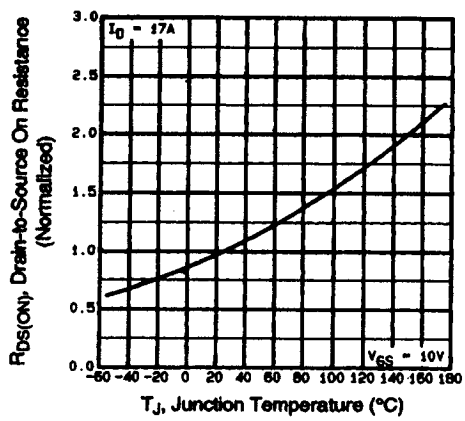


Fig 4. Normalized On-Resistance Vs. Temperature

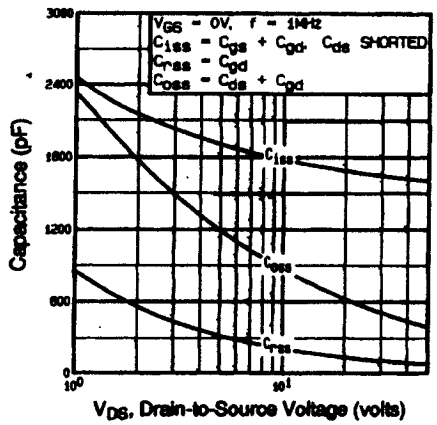


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

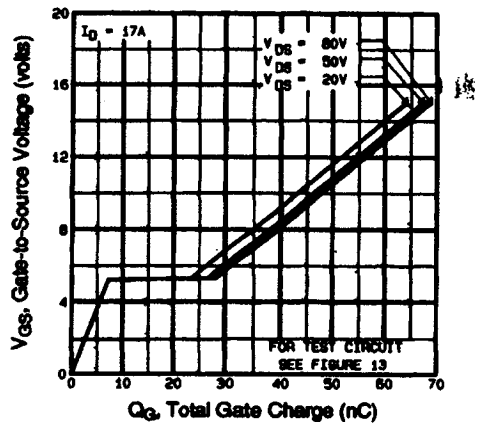


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

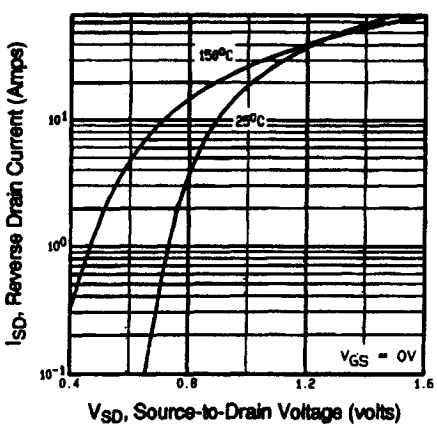


Fig 7. Typical Source-Drain Diode Forward Voltage

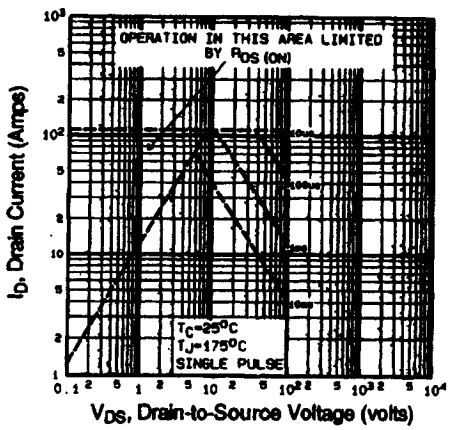


Fig 8. Maximum Safe Operating Area

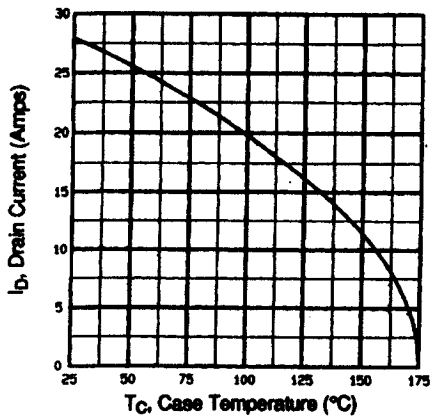


Fig 9. Maximum Drain Current Vs. Case Temperature

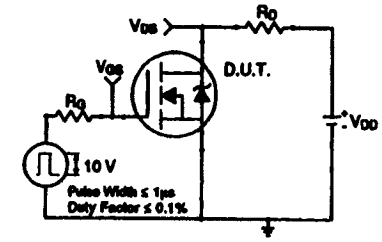


Fig 10a. Switching Time Test Circuit

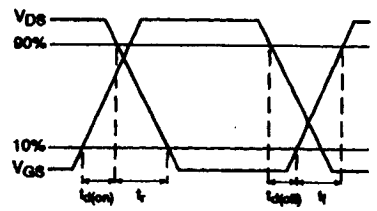


Fig 10b. Switching Time Waveforms

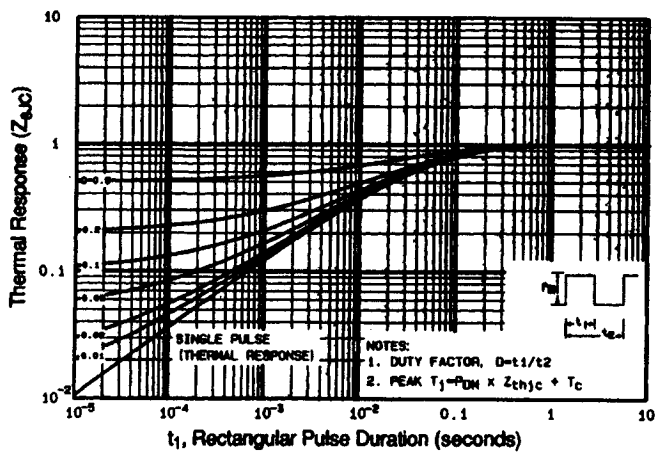


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

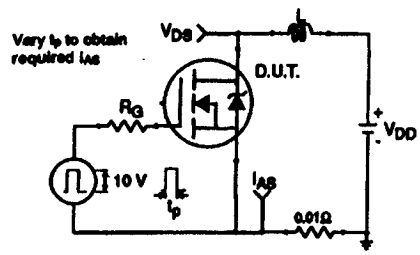


Fig 12a. Unclamped Inductive Test Circuit

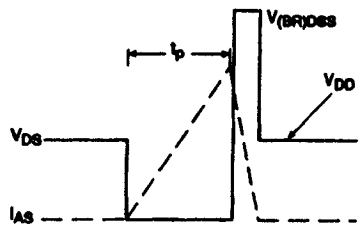


Fig 12b. Unclamped Inductive Waveforms

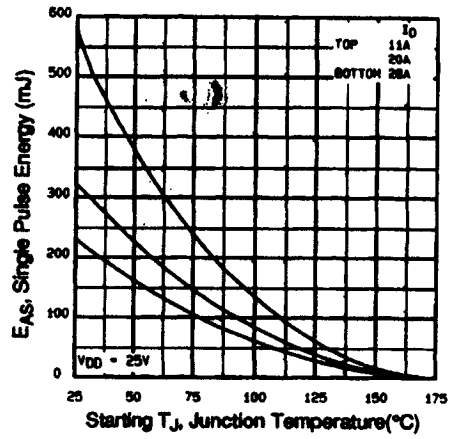


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

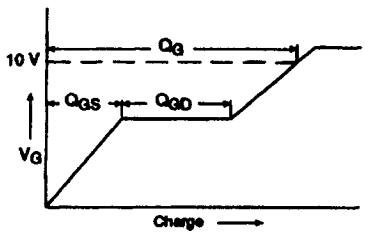


Fig 13a. Basic Gate Charge Waveform

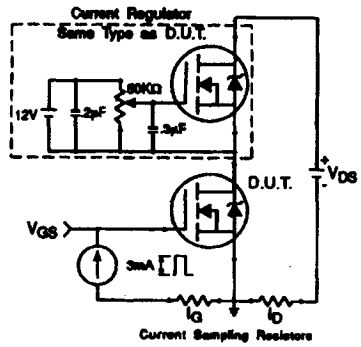


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

International IOR Rectifier

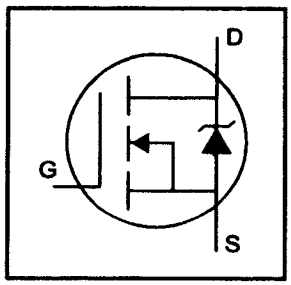
International
IOR Rectifier

PD - 91503D

IRFP150N

HEXFET® Power MOSFET

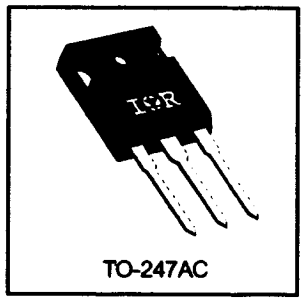
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 100V

$R_{DS(on)}$ = 0.036Ω

I_D = 42A



TO-247AC

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	42	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	30	
I_{DM}	Pulsed Drain Current ①⑤	140	
P_D @T_C = 25°C	Power Dissipation	160	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	420	mJ
I_{AR}	Avalanche Current①⑤	22	A
E_{AR}	Repetitive Avalanche Energy①	16	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.95	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I_D = 1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.036	Ω	V_{GS} = 10V, I_D = 23A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	14	—	—	S	V_{DS} = 25V, I_D = 22A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	110	nC	I_D = 22A
Q_{gs}	Gate-to-Source Charge	—	—	15		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	58		V_{GS} = 10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD} = 50V
t_r	Rise Time	—	56	—		I_D = 22A
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		R_G = 3.6Ω
t_f	Fall Time	—	40	—		R_D = 2.9Ω See Fig. 10 ④⑤
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	1900	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	450	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	230	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	140		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S =23A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	180	270	ns	T_J = 25°C, I_F = 22A
Q_{rr}	Reverse RecoveryCharge	—	1.2	1.8	µC	di/dt = 100A/µs ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 1.7mH
R_G = 25Ω, I_{AS} = 22A. (See Figure 12)

③ I_{SD} ≤ 22A, di/dt ≤ 180A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF1310N data and test conditions.

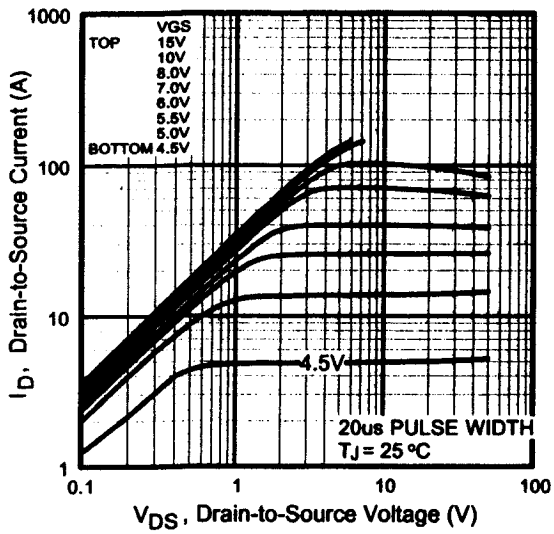


Fig 1. Typical Output Characteristics

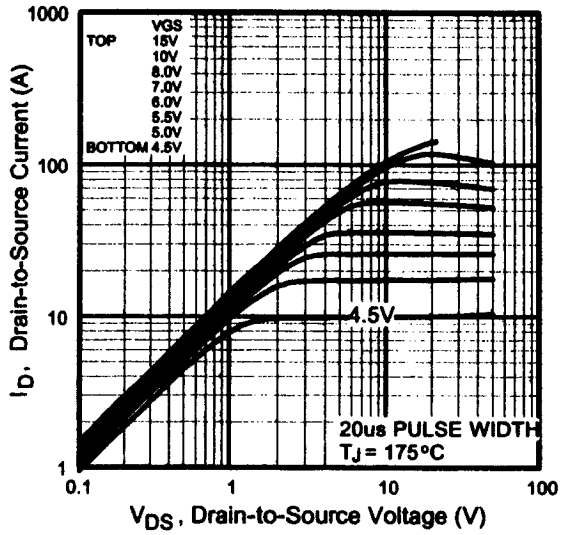


Fig 2. Typical Output Characteristics

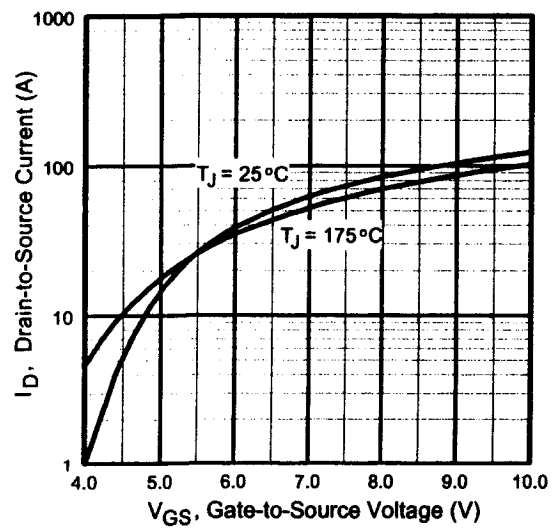


Fig 3. Typical Transfer Characteristics

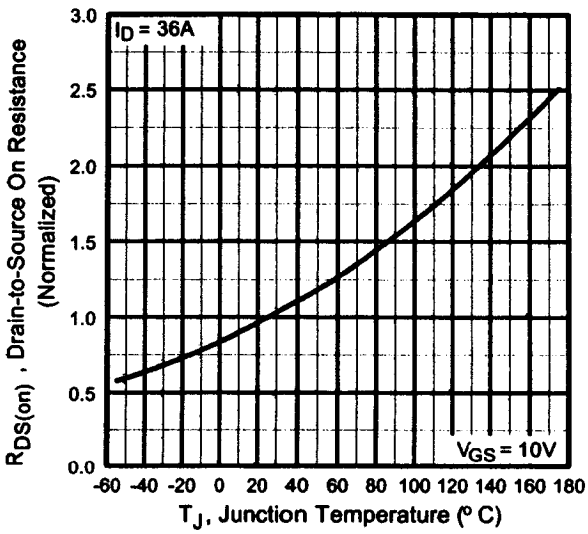


Fig 4. Normalized On-Resistance Vs. Temperature

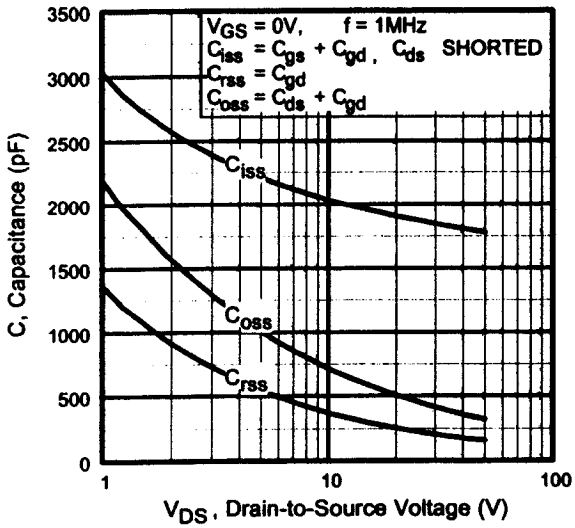


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

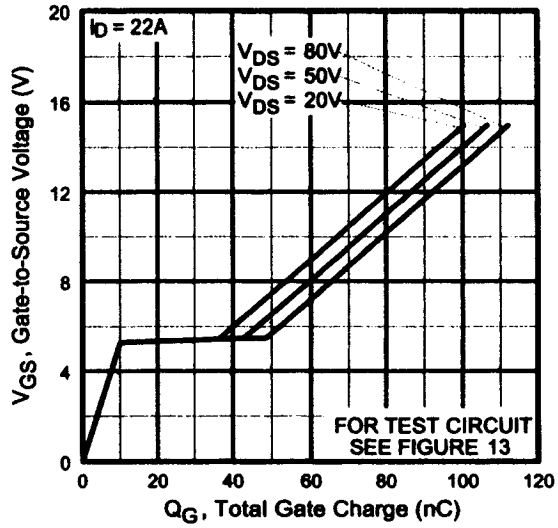


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

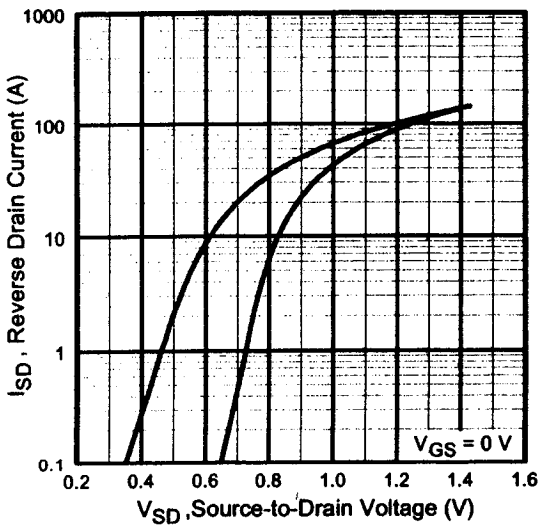


Fig 7. Typical Source-Drain Diode Forward Voltage

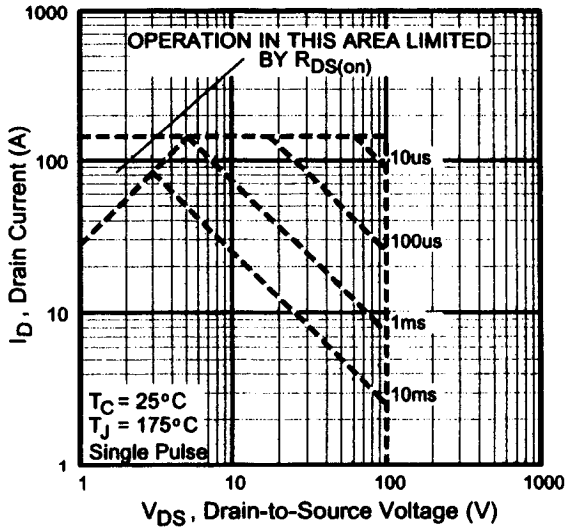


Fig 8. Maximum Safe Operating Area

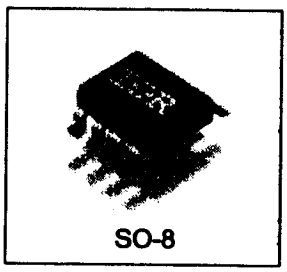
International
IOR Rectifier

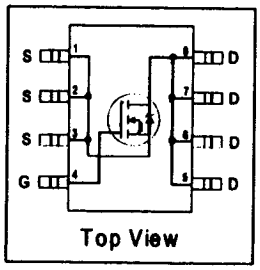
PD - 94279

IRF7822

HEXFET® Power MOSFET for DC-DC Converters

- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses


SO-8



Top View

Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRF7822 has been optimized for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and Cdv/dt-induced turn-on immunity. The IRF7822 offers particulary low $R_{DS(on)}$ and high Cdv/dt immunity for synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 3W is possible in a typical PCB mount application.

DEVICE CHARACTERISTICS⑤

	IRF7822
$R_{DS(on)}$	5.0mΩ
Q_G	44nC
Q_{sw}	12nC
Q_{oss}	27nC

Absolute Maximum Ratings

Parameter		Symbol	IRF7822	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain or Source Current ($V_{GS} \geq 4.5V$)	T_A = 25°C	I_D	18	A
	T_A = 70°C		13	
Pulsed Drain Current①		I_{DM}	150	
Power Dissipation	T_A = 25°C	P_D	3.1	W
	T_A = 70°C		3.0	
Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Continuous Source Current (Body Diode)		I_S	3.8	A
Pulsed Source Current①		I_{SM}	150	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	40	°C/W
Maximum Junction-to-Lead	$R_{\theta JL}$	20	°C/W

Electrical Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30	–	–	V	V_{GS} = 0V, I_D = 250µA
Static Drain-Source on Resistance	$R_{DS(on)}$		5.0	6.5	mΩ	V_{GS} = 4.5V, I_D = 15A②
Gate Threshold Voltage	$V_{GS(th)}$	1.0			V	V_{DS} = V_{GS}, I_D = 250µA
Drain-Source Leakage Current	I_{DSS}			30	µA	V_{DS} = 24V, V_{GS} = 0
				150		V_{DS} = 24V, V_{GS} = 0, Tj = 100°C
Gate-Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±12V
Total Gate Chg Cont FET	Q_G		44	60	nC	V_{GS}=5.0V, I_D=15A, V_{DS}=16V
Total Gate Chg Sync FET	Q_G		38			V_{GS} = 5.0V, V_{DS}< 100mV
Pre-Vth Gate-Source Charge	Q_{GS1}		13			V_{DS} = 16V, I_D = 15A
Post-Vth Gate-Source Charge	Q_{GS2}		3.0			
Gate to Drain Charge	Q_{GD}		9.0			
Switch Chg(Q_{gs2} + Q_{gd})	Q_{sw}		12			
Output Charge	Q_{oss}		27			V_{DS} = 16V, V_{GS} = 0
Gate Resistance	R_G		1.5		Ω	
Turn-on Delay Time	$t_{d(on)}$		15		ns	V_{DD} = 16V, I_D = 15A
Rise Time	t_r		5.5			V_{GS} = 5.0V
Turn-off Delay Time	$t_{d(off)}$		22			Clamped Inductive Load
Fall Time	t_f		12			
Input Capacitance	C_{iss}	–	5500	–	pF	V_{DS} = 16V, V_{GS} = 0
Output Capacitance	C_{oss}	–	1000	–		
Reverse Transfer Capacitance	C_{rss}	–	300	–		

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}			1.0	V	I_S = 15A②, V_{GS} = 0V
Reverse Recovery Charge④	Q_{rr}		120		nC	di/dt ~ 700A/µs V_{DS} = 16V, V_{GS} = 0V, I_S = 15A
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$		108		nC	di/dt = 700A/µs (with 10BQ040) V_{DS} = 16V, V_{GS} = 0V, I_S = 15A

Notes:
① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 400 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board
④ Typ = measured - Q_{oss}
⑤ Typical values of R_{DS}(on) measured at V_{GS} = 4.5V, Q_G, Q_{SW} and Q_{OSS} measured at V_{GS} = 5.0V, I_F = 15A.

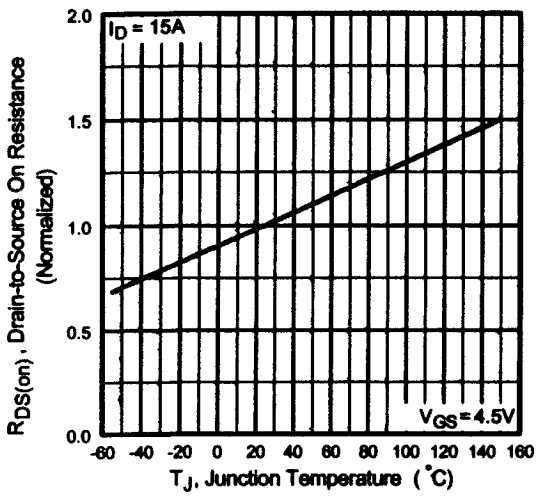


Fig 1. Normalized On-Resistance Vs. Temperature

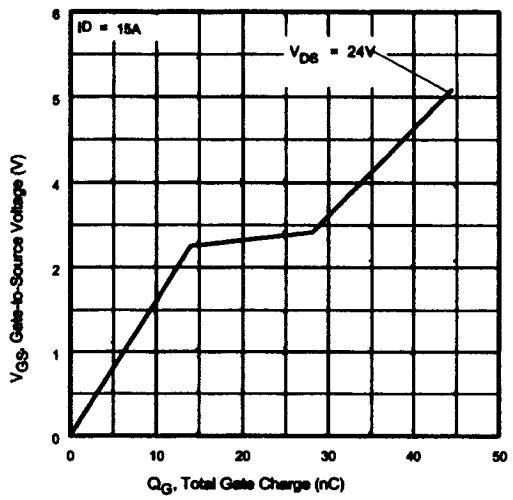


Fig 2. Typical Gate Charge Vs. Gate-to-Source Voltage

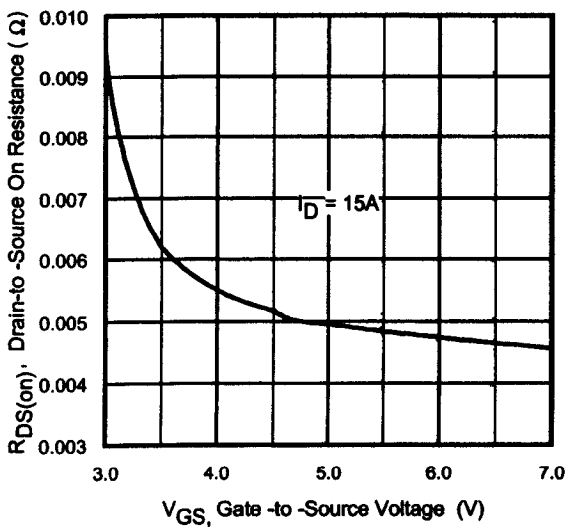


Fig 3. On-Resistance Vs. Gate Voltage

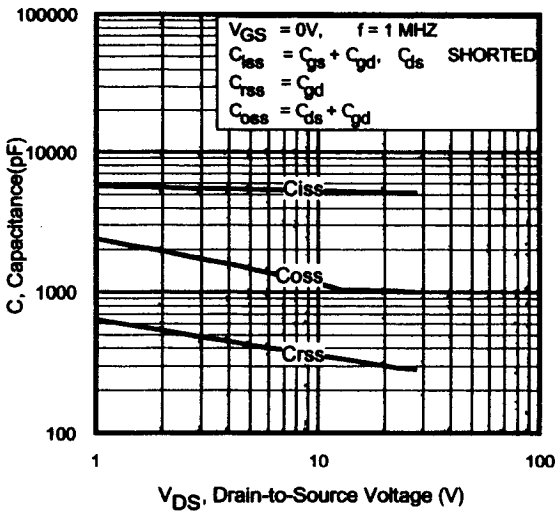


Fig 4. Typical Capacitance Vs. Drain-to-Source Voltage

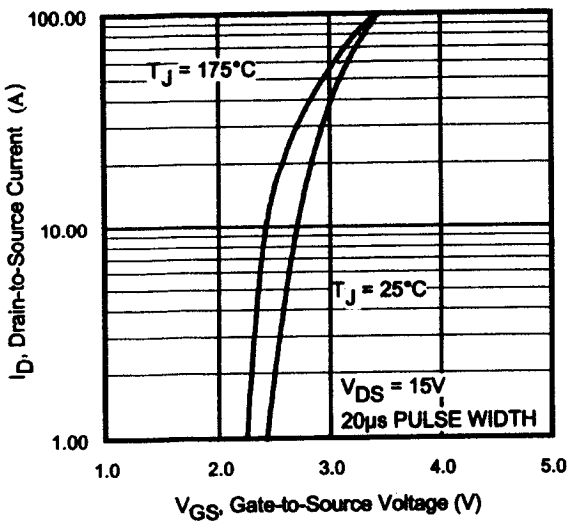


Fig 5. Typical Transfer Characteristics

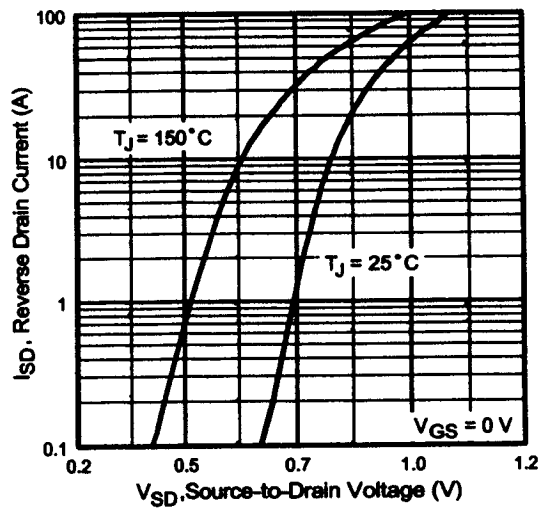


Fig 6. Typical Source-Drain Diode Forward Voltage

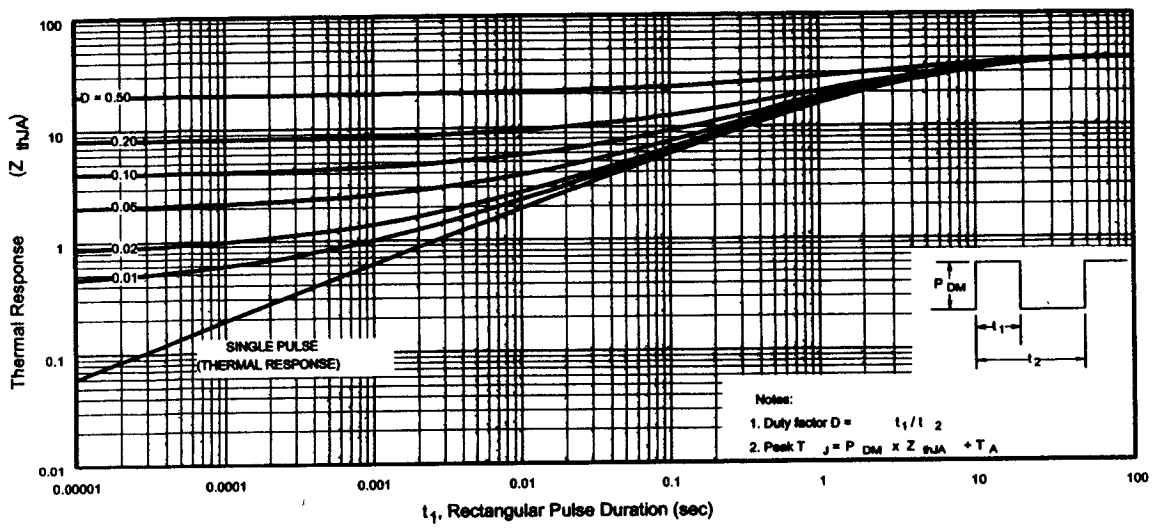


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

APPENDIX F

LINE AC TO HIGH FREQUENCY AC CONVERTER WITH TRAPEZOIDAL OUTPUT VOLTAGE

C.1 CIRCUIT DESCRIPTION

Fig. C-1 shows a circuit diagram of a low frequency ac (LFAC) to high frequency ac (HFAC) with trapezoidal output voltage waveform.

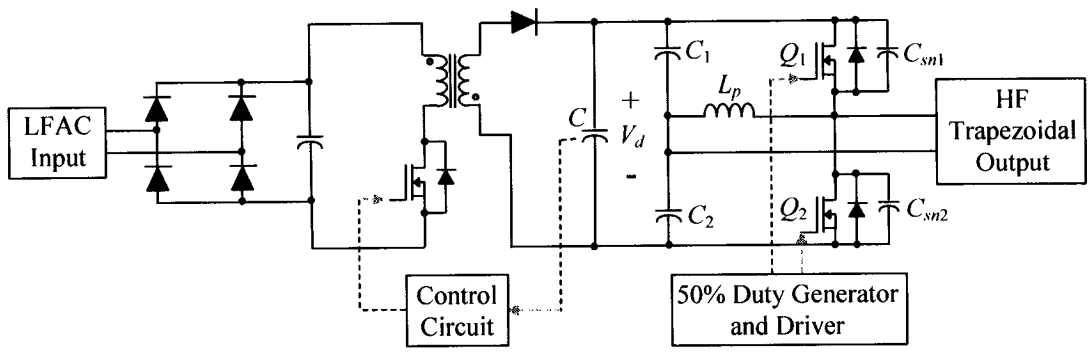


Fig. C-1: LFAC/HFAC converter with trapezoidal output voltage

This circuit consists of a conventional ac/dc switching power converter, an energy storage capacitor C and a dc/ac inverter. The ac/dc converter provides a constant and essentially ripple free voltage to the dc/ac inverter. The dc/ac inverter is a half-bridge circuit that consists of two capacitors C_1 and C_2 to form a center tap dc, two MOSFETs Q_1 and Q_2, two commutation capacitors C_{sn1} & C_{sn2}, and a commutation inductor L_p. Both switches Q_1 and Q_2 operate at a constant frequency with close to 50% duty cycle. The gating signals for the switches are complementary with a predetermined dead time. The values of dead time, commutation inductor L_p and capacitors C_{sn1} & C_{sn2} are designed in such a way that (i) a relatively constant slope is obtained for both rising and falling edges

of the output voltage waveform, and (ii) zero voltage switching is achieved for both switches during turn-on and turn-off under all load conditions.

C.2 OPERATING PRINCIPLE

The main operating waveforms of the inverter in Fig. C-1 are shown in Fig. C-2, and the brief operating principle of the inverter is given below:

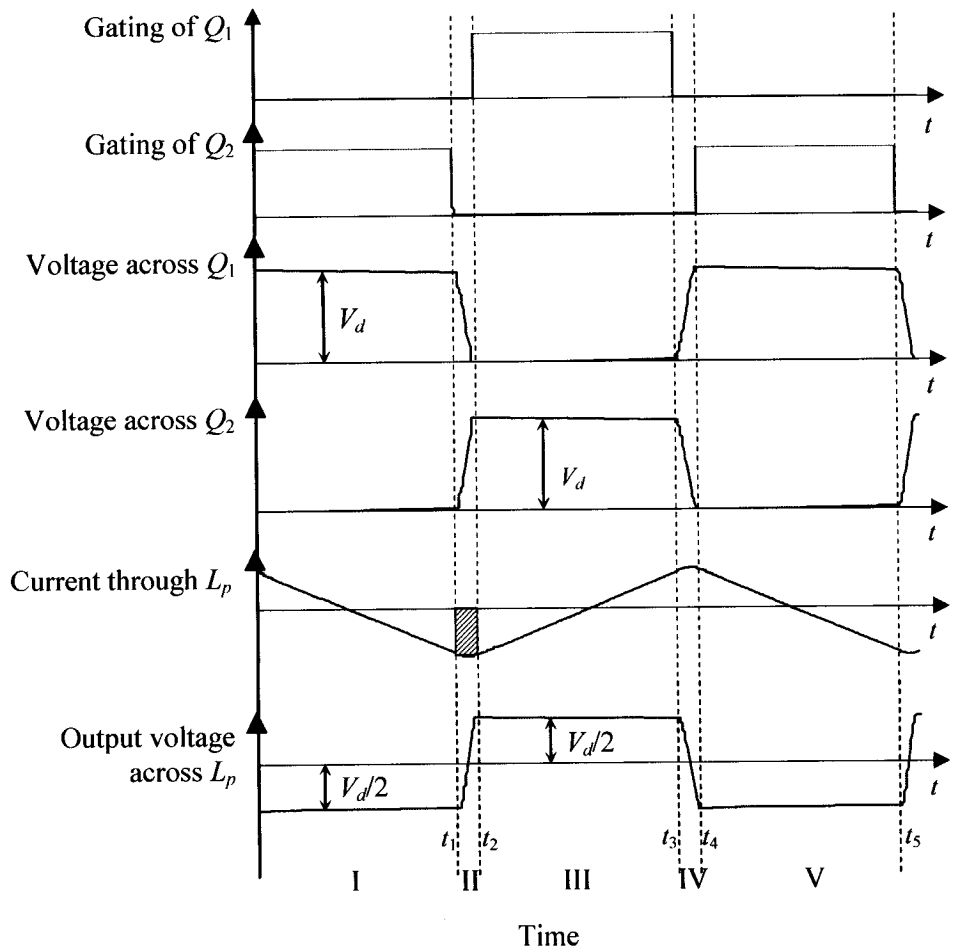


Fig. C-2: Operating waveforms of DC/HFAC inverter with trapezoidal output voltage

(i) Interval I

When Q_2 is conducting, a negative voltage equal to $V_d/2$ is appearing across the commutation inductor L_p and current following through L_p is governed by:

$$i_p(t) = \frac{V_d}{4L_p}(PW + \frac{t_r}{2}) - \frac{V_d}{2L_p}t \tag{C-1}$$

Where PW and t_r is the pulse width and rising time of the output trapezoidal waveform respectively.

At the end of this interval, current through L_p is equal to:

$$i_p(t_1) = -\frac{V_d}{4L_p} \cdot PW \tag{C-2}$$

(ii) Interval II

Now Q_2 is turned off and Q_1 has not been turned on yet (dead time), the negative inductor current now discharges the capacitor C_{sn1} from V_d to 0, and charges capacitor C_{sn2} from 0 to V_d.

At time $t = t_1 + t_r/2$, current through L_p reaches its peak value given by:

$$i_{p,\max} = \frac{V_d}{4L_p}(PW + \frac{t_r}{2}) \tag{C-3}$$

Assuming that the inductor current splits equally between the two commutation capacitors, the shaded area of i_p in Fig. C-2 represents the sum of charge Q to C_{sn2} and discharge Q from C_{sn1}. Therefore, the commutation capacitance can be calculated from:

$$C_{sn1} = C_{sn2} = \frac{Q/2}{V_d} = \frac{t_r}{8L_p}(PW + \frac{t_r}{4}) \tag{C-4}$$

(iii) Interval III

When capacitor C_{sn1} discharges to 0, the negative inductor current forces body diode D_1 to conduct. At this time, switch Q_1 can be turned on under zero voltage, thereby eliminating the switching losses. Once switch Q_1 is conducting, voltage $V_d/2$ is appearing across the inductor L_p and positive current is building up in L_p.

(iv) Interval IV

After close to 50% duty cycle, switch Q_1 is turned off, and Q_2 has not been turned on yet (dead time), the positive inductor current now discharges the capacitor C_{sn2} from V_d to 0, and charges capacitor C_{sn1} from 0 to V_d.

(v) Interval V

When capacitor C_{sn2} discharges to 0, the positive inductor current forces the body diode D_2 to conduct. At this time, switch Q_2 can be turned on under zero voltage, thereby eliminating the switching losses. Once switch Q_2 is conducting, negative voltage $V_d/2$ is appearing across L_p and once again negative current is building up in the inductor and the whole cycle repeats.

C.3 MAJOR FEATURES

(a) Provide controlled rising and falling edges of the output voltage waveform witch can significantly reduce EMI problem;

(b) Operate with zero voltage switching under all load conditions.