DSP-BASED CONTROL OF STATIC POWER QUALITY COMPENSATORS IN INDUSTRIAL POWER SYSTEMS

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ABSTRACT

DSP-BASED CONTROL OF STATIC POWER QUALITY COMPENSATORS IN INDUSTRIAL POWER SYSTEMS

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The increased use in industry of sensitive power electronics-based equipment resulted in concerns about power quality in distribution systems. This has led to the proposal of more stringent requirements regarding power quality, in terms of current harmonics, as reflected in standards such as IEEE-519, and in terms of voltage faults. By exploiting recent advances made in power electronics and digital control circuits, this thesis develops new power conditioning solutions based on the PWM voltage source converter, with emphasis on their dynamic response. The proposed compensators include four-switch and six-switch based series and shunt configurations. The proposed control strategies implement state-space feedback control of the series compensator, direct power control of the shunt compensator and unified deadbeat control of the combined series-parallel compensator. These control algorithms present a number of advantages such as dealing with time varying control references in series compensation, integrating multiple control variables into one control loop in shunt compensation, and unified control of the combination of series-parallel converters. The improvements cover the global control functions as well as direct converter control and PWM functions. Simulation and experimental results from laboratory prototypes confirm the theoretical considerations.

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LIST OF SYMBOLS

Voltage and Current Vectors

$[v_s]_{abc}$: Three-phase supply voltages, $[v_s]_{abc} = [v_{sa}\ v_{sb}\ v_{sc}]^T$

$[v_L]_{abc}$: Three-phase load voltages, $[v_L]_{abc} = [v_{La}\ v_{Lb}\ v_{Lc}]^T$

$[v_m]_{abc}$: Three-phase converter voltages, $[v_m]_{abc} = [v_{ma}\ v_{mb}\ v_{mc}]^T$

$[v_{inj}]_{abc}$: Three-phase injected voltages, $[v_{inj}]_{abc} = [v_{inj,a}\ v_{inj,b}\ v_{inj,c}]^T$

$[i_s]_{abc}$: Three-phase supply currents, $[i_s]_{abc} = [i_{sa}\ i_{sb}\ i_{sc}]^T$

$[i_L]_{abc}$: Three-phase load currents, $[i_L]_{abc} = [i_{La}\ i_{Lb}\ i_{Lc}]^T$

$[i_m]_{abc}$: Three-phase converter currents, $[i_m]_{abc} = [i_{ma}\ i_{mb}\ i_{mc}]^T$

$[i_{inj}]_{abc}$: Three-phase injected currents, $[i_{inj}]_{abc} = [i_{inj,a}\ i_{inj,b}\ i_{inj,c}]^T$

$[m]_{abc}$: Three-phase converter modulation index, $[m]_{abc} = [m_a\ m_b\ m_c]^T$

Voltage, Current and Power

V_{dc} : Converter dc-bus voltage

i_{dc} : Converter dc-bus current

V_{4sw} : Four-switch converter voltage space vector associated with $[v_m]_{abc}$

V_{6sw} : Six-switch converter voltage space vector associated with $[v_m]_{abc}$

$S_{af,h}$: Apparent power for load harmonics compensation only

$S_{af,h+q}$: Apparent power for harmonics and reactive power compensation

p_L : Instantaneous active power drawn by the load

q_L : Instantaneous reactive power drawn by the load

p_{inj} : Instantaneous active power injected by the compensator

q_{inj} : Instantaneous reactive power injected by the compensator

Modulating and Filter Parameters

G_c : Converter Modulating ac gain

α_z : Converter ac-link inductor voltage drop coefficient

L_{af} : Active filter ac-link inductor

γ_n : Turns ratio of the series coupling transformer

L_f : Converter LC filter inductor

C_f : Converter LC filter capacitor

r_f : Converter LC filter damping resistor

ξ_0 : Damping constant of the LC filter

Frequency and Period

f_s : Utility frequency (60 Hz)

f_h : Load harmonic frequency

f_f : Converter LC filter resonance frequency

f_{sw} : PWM switching frequency

ω_s : Supply angular frequency ($\omega_s = 2\pi f_s$)

ω_h : Load harmonic angular frequency ($\omega_h = 2\pi f_h$)

ω_f : Break frequency of the LC filter

T_s : Controller sampling time

T_{sett} : Settling time of the closed-loop control system

T_d : System modeling discretization time

T_{sw} : PWM switching period

LIST OF ACRONYMS

APLC	: Active Power Line Conditioner
ASD	: Adjustable Speed Drive
BJT	: Bipolar Junction Transistor
CSC	: Current-Source Converter
CSI	: Current-Source Inverter
CSR	: Current-Source Rectifier
DG	: Distributed Generation
DPC	: Direct Power Control
DSP	: Digital Signal Processor
DVR	: Dynamic Voltage Restorer
EMI	: Electromagnetic Interference
EPRI	: Electric Power Research Institute
FACTS	: Flexible AC Transmission Systems
FPGA	: Field Programmable Gate Array
GTO	: Gate-Turn-Off Thyristor
HVDC	: High Voltage DC
IGBT	: Insulated-Gate-Bipolar Transistor
IGCT	: Integrated Gate Commutated Thyristor
MOSFET	: Metal-Oxide-Semiconductor Field Effect Transistor
PCC	: Point-of-Common-Coupling

PWM	: Pulse Width Modulation
SCR	: Silicon Controlled Rectifier
SMES	: Superconducting Magnetic Energy Storage
SSC	: Static Series Compensator
STATCOM	: Static Synchronous Compensator
SVM	: Space Vector Modulation
THD	: Total Harmonic Distortion
UPFC	: Unified Power Flow Controller
UPQC	: Unified Power Quality Conditioner
UPS	: Uninterruptible Power Supply
VHSIC	: Very High Speed Integrated Circuit
VHDL	: VHSIC Hardware Description Language
VSC	: Voltage-Source Converter
VSI	: Voltage-Source Inverter
VSR	: Voltage-Source Rectifier

CHAPTER 1

INTRODUCTION

1.1 GENERAL INTRODUCTION

In typical power distribution systems, the proliferation of power electronics-based equipment results in deterioration of the quality of electric power supply. Both high power industrial loads and domestic loads may generate harmonics in the power networks [1][2]. At the same time, the equipment causing the disturbances is itself quite sensitive to the deviation of the supply voltage from the ideal sinusoidal voltage waveform [3][4]. Therefore, power quality problems may originate in the distribution system or may be caused by the power consumers themselves.

Great compatibility gaps were developed among power electronics manufacturers, power producers and power users, in that many of these systems are too sensitive to the electrical environment in which they are being placed. A safe, reliable and clean power supply to these industries is becoming a prerequisite to their profitable operation. This has led to the proposal of more stringent requirements regarding power quality [5][6][7][8], and standards such as IEEE-519 reflect these preoccupations.

Conventional equipment has been proven insufficient for mitigation of today's power quality problems [10]. Passive LC or LCR filter banks were traditionally used to limit the flow of harmonic currents and correct the power factor in distribution systems. However their performance depends upon the system parameters and they may cause parallel

resonances with the network impedance. They also tend to be bulky and the design is complex, particularly as the number of harmonic components to be canceled increases.

Uninterruptible power supply (UPS) systems are used to obtain a high quality power for sensitive loads. A UPS system consists of a rectifier, a battery system and an inverter. The batteries provide backup power during momentary power interruptions or severe voltage sags. However, the battery maintenance at high power levels, high capital costs and minimal utilization under normal operating conditions are some of its drawbacks. The UPS system also contains transfer switches whose operation is critical for supplying continuous power to sensitive loads.

In some cases, the back-up generation system based on rotating machines is used as an alternative to UPS system to provide power during temporary interruptions in power network. However, it has a slower response time and depends on automatic transfer switches for a change over between power sources in case of power quality faults. During the transfer between the main supply and the back up, there may be a loss of continuity of power to the load and hence the system may not be able to meet the required power quality indices.

With improvements in power electronics and control circuits, the static power quality compensator is now becoming more established in industry. Compared to the UPS system, which generates a new power source, the static power quality compensator compensates the faults of the existing power supply by voltage or current injection, and supplies a compensated power source to sensitive loads. In many cases, the static power quality compensator is a more economical solution to ensure a required level of power quality that is deemed satisfactory to the customers [11].

1.2 POWER QUALITY ISSUES

The concept of power quality implies supply availability and voltage quality, and is assessed by the user's perception of the attributes of the input voltage [12]. A voltage quality problem relates to any failure of equipment due to deviations of the line voltage from its nominal characteristics [13]. Fig. 1.1 shows the general power quality issues that may originate within the end-user power system such as harmonics, or in the power distribution system such as lightning.

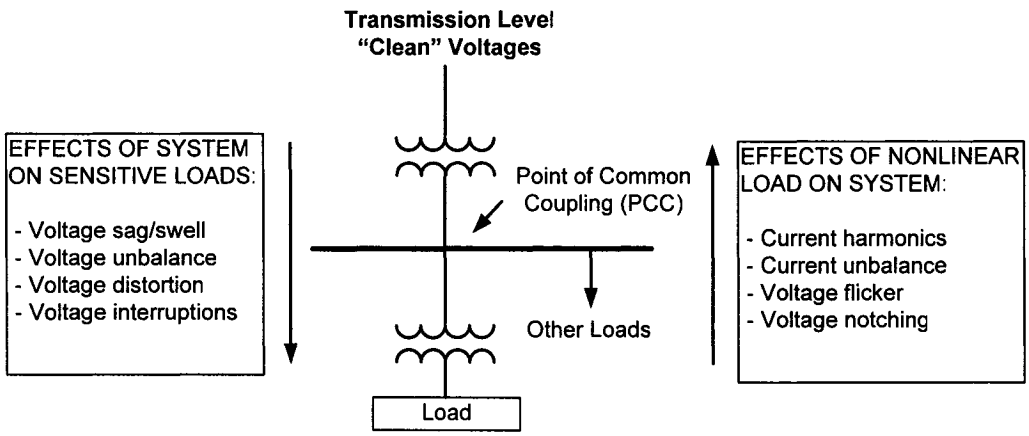


Fig. 1.1. The common power quality problems and their origins.

This thesis addresses several of the more common power quality problems, in particular voltage sags and harmonic currents. Together they account for over 90% of the power quality disturbances affecting most commercial and industrial customers.

1.2.1 Voltage Sags in Distribution Systems

Transmission-level bulk power in North America is extremely reliable, but the physical nature of the distribution network makes voltage sags and momentary interruptions inevitable [14]. Lightning, tree branch or animal contact, and insulation failures or human activity can create single-line-to-ground (SLG) or line-to-line fault paths, and rarely a 3-phase to ground fault. The relatively few customers near the fault will see a deep voltage sag. But the vastly larger community of customers on other distribution feeders, and also those connected through the transmission system, will see a voltage sag. The magnitude of the sag is determined by the customer's distance to the fault location, and its duration is determined by the characteristics of the utility's circuit protection devices.

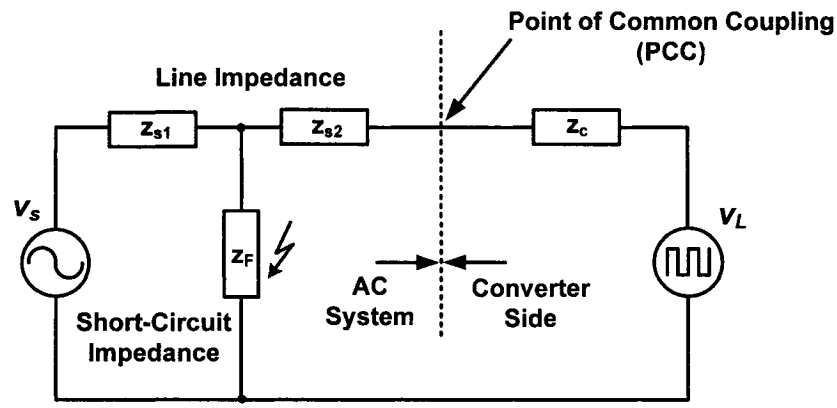


Fig. 1.2. The supply voltage sag caused by a short-circuit fault.

A distribution system power quality study was carried out from 1993 to 1995 [15]. Approximately 300 power quality monitors were installed in locations across the United States, resulting in over 6 million power quality events being recorded. The cumulative data indicates that most faults are single-line-to-ground (SLG) fault, where 92% of all

faults correspond to voltage sags with the remaining amplitude down to 40-50% of nominal value, and that most of these faults last for less than 2 seconds. Longer-term interruptions (2 seconds to 10 minutes) proved to be rare, accounting for an additional 4% of all faults. Similar data have also been recorded in a survey of Canadian power systems in 1997 [16]. Fig. 1.3 presents the number of voltage sags of a particular magnitude and duration expected in one year at a typical industrial site. It shows that the greatest numbers of faults are of short duration, less than one second, and leaves 50% to 90% of voltage remaining.

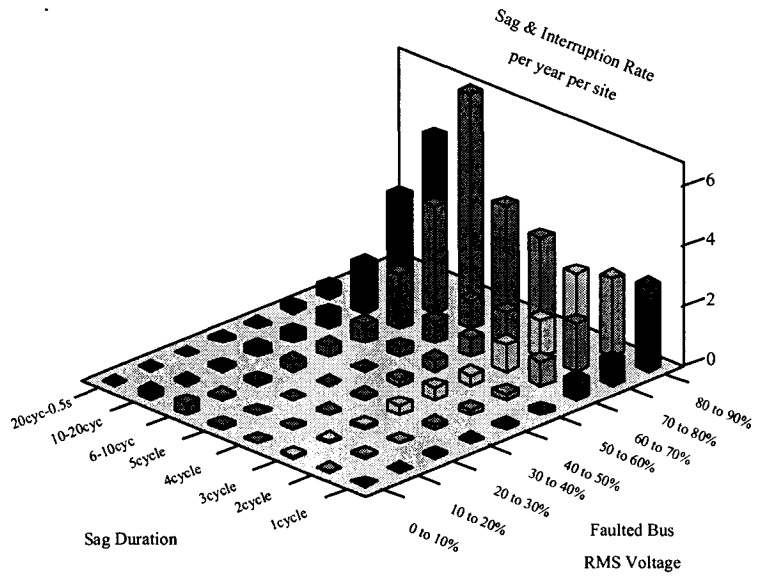


Fig. 1.3. Number of voltage sags at a typical industrial site.

Switching power supplies, industrial control relays, contactors, solenoids, adjustable-speed motor drives and thyristor controlled rectifiers are all susceptible to short term voltage sags [17][18]. IEEE standard 1346-1998 [5], "Recommended practice for evaluating electric power system compatibility with electronic process equipment", has been proposed to help industrial equipment users evaluate the impact of voltage sags at their plants. It provides the input voltage fault-duration curves that the electronic process

equipment should tolerate. In addition, IEEE standard 446-1987 [9], "Recommended practice for emergency and standby power systems for industrial and commercial applications", lists the typical ranges of input power supply disturbances that are considered acceptable by major computer manufacturers. In case of critical applications where a power failure is unacceptable, a backup to the utility grid has to be provided by means of the UPS system or power quality compensator.

1.2.2 Harmonics Drawn by Non-Linear Loads

Non-linear loads typically draw non-linear currents when fed from the ac supply [19]. A common non-linear load is an ac induction motor drive, in which the most significant harmonic currents injected into the ac supply include the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics. In addition to harmonic currents, non-linear loads may also draw a significant amount of reactive power [20].

When source inductance is taken into account, circulation of harmonic currents in the ac system results in voltage distortion at various points in the ac system. The reactive power also has a detrimental effect on the voltage of the ac system, resulting in additional voltage drops. The distorted voltage waveform affects the operation of both the non-linear load and other linear and non-linear loads connected to the same bus, or PCC, or adjacent buses, as Fig. 1.4 shows.

IEEE standard 519-1992 [8], "Recommended practices and requirements for harmonic control in electric power systems", proposes to designers of industrial plants the harmonic limits at the PCC. Summaries of the main requirements are given in Table 1.1 and Table 1.2.

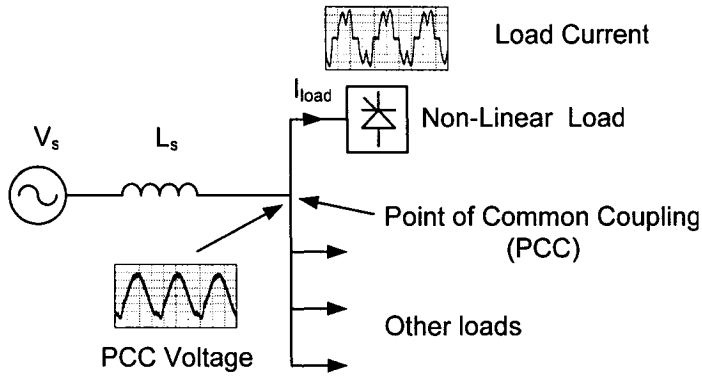


Fig. 1.4. Harmonic propagation in a power system due to the non-linear load.

Table 1.1. IEEE-519 Odd Harmonic Current Distortion Limits

Percent Limits of Harmonic Currents (Bus Voltage at the PCC < 69 KV)

I_{sc}/I_l	h<11	11<h<17	17<h<23	23<h<35	35<h	THD_i
<20	4.0	2.0	1.5	0.3	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Notes: 1. I_{sc} is the maximum short-circuit current at the PCC

2. I_l is the maximum fundamental frequency load current at the PCC

Table 1.2. IEEE-519 Voltage Distortion Limits

Bus Voltage @ PCC	HD_v (%)	THD_v (%)
< 69 kV	3.0	5.0

Notes: 1. HD_v = Individual harmonic voltage distortion

1.3 SOLUTIONS TO POWER QUALITY PROBLEMS

The analysis and mitigation of power quality problems are becoming an integral part of power system studies. In some cases, power quality compensation is incorporated into new plant installations. For existing installations, power quality compensators may have to be added. On the other hand, dynamic power conditioning can be applied to the entire facility, to small loads or to groups of critical equipment, depending on how concentrated or diverse the critical equipment location is within the facility. Each has advantages and disadvantages. However, the economics are usually better when the focus is on protecting the loads that are most critical to the overall process and the loads that are most sensitive to disturbances.

The power quality marketplace has a wide variety of products to solve the ever-growing list of power quality problems, most of them are designed to handle only one specific type of power abnormality. The UPS system is the traditional solution for protecting individual loads and groups of loads within a facility [21], and it is a full solution of all power quality problems by isolating the faulted main power source and supplying a backup power source. However, the cost of a UPS system, especially the cost for battery maintenance and replacement, makes the UPS solution less than ideal in many industrial environments. The new power conditioning technology is based on voltage and current injection instead of generation of a new power source, which merely corrects the deviations of the power supply from its ideal waveform, thus demands a lower capital cost. Table 1.3 shows the types of power quality problems that the static power quality compensator can address based on how it is configured.

Table 1.3. Solutions to Power Quality Problems based on Static Compensators.

Compensator Topologies	Power Quality Problems Addressed	
	Caused by Power Supply	**Caused by Load**
Series Compensator	- Voltage sag compensation - Blocking of voltage distortion - Phase voltage balancing	
Shunt Compensator		- Harmonic filtering - Reactive power compensation - Load balancing - Flicker reduction
Combined Series-Parallel Compensator	- Voltage sag compensation - Blocking of voltage distortion - Phase voltage balancing - Voltage swell compensation	- Harmonic filtering - Reactive power compensation - Load balancing - Flicker reduction

1.3.1 Series Configuration for Voltage Injection

Figure 1.3 illustrates how to configure the PWM converter in a series connection with the supply system through series injection transformers. The static series compensator (SSC) or the so-called dynamic voltage restorer (DVR) plays the role of a controllable voltage source. This configuration is most appropriate for protecting loads sensitive to supply voltage sags [30]. It can also compensate the harmonic distortion of the supply voltage [31].

The power rating of the series compensator is only a fraction of that of the load and the control response is in the order of milliseconds, thus ensuring a secure voltage supply under transient power network conditions [32]. In case of supply voltage fault, the energy needed for voltage compensation is supplied by the reduced source voltage through a diode bridge, as shown in Fig. 1.5. The series compensator is capable of feeding a certain amount of active power to the load via the dc-link, which takes the active power at the same time through the diode-bridge front-end. However the diode-bridge cannot send the

extra power back to the ac system, and the dc-link capacitor has a limited capacity to storage the active power. Therefore, the series compensator cannot compensate for voltage swells. In this case, a combined series-parallel compensator must be used.

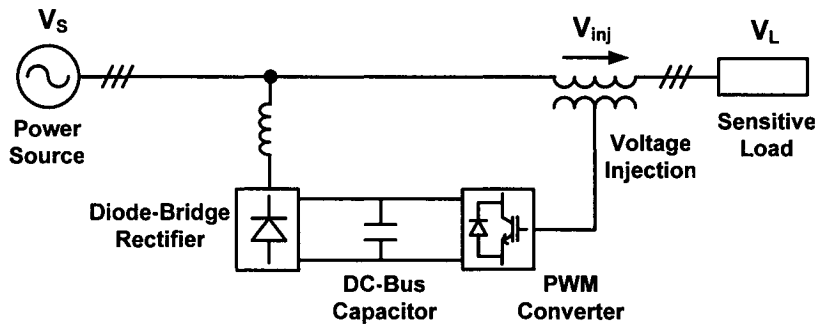


Fig. 1.5. The series-connected power quality compensator.

1.3.2 Shunt Configuration for Current Injection

Figure 1.4 shows the power circuit of the PWM converter when it is connected in parallel to the power supply and the load. This configuration is often called active filter or static synchronous compensator (STATCOM). It plays the role of a controllable current source, and is appropriate for compensation of the harmonic currents drawn by a nonlinear load [33].

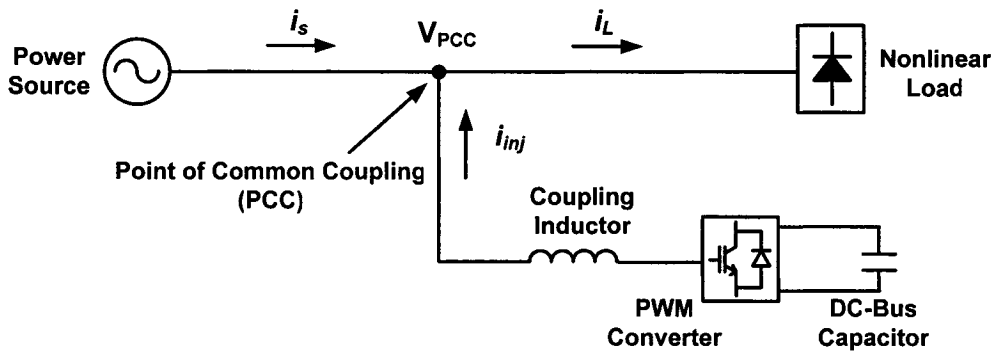


Fig. 1.6. The shunt-connected power quality compensator.

The shunt compensator injects currents into the PCC, and the selection of the control system depends on its compensation objective. There are two modes of operation: *standard mode* and *flicker mode*.

1.3.2.1 Standard mode

The current, flowing from the PCC to the load, is measured and separated into fundamental and harmonic components. The parallel compensator injects currents such that the harmonic currents are exchanged exclusively between the compensator and the load, and therefore do not flow into the power network. If designed with a large power rating, the parallel compensator can also inject reactive current, in both capacitive and inductive modes, to improve the displacement power factor [34].

1.3.2.2 Flicker mode

Flicker is caused by sudden, stochastic load current peaks, and it may cause voltage fluctuation at the PCC if not properly compensated. The flicker producing loads include arc furnaces, welding machines and tooling machines. When operating in flicker mode, the parallel compensator focuses on one or two harmonics and provides stepless reactive power injection and load balancing [35][36].

1.3.3 Unified Configuration for both Voltage and Current Correction

This configuration is similar to the series configuration, but it uses a parallel PWM converter to replace the diode-bridge front-end, and move the parallel converter to the downstream of the series converter in most applications, as Fig. 1.7 shows. The combined

series-parallel power quality compensator results in the unification of both types of protection and acts as both a controllable current source and a controllable voltage source. The unified configuration shows advantages if the load is a significant source of harmonics and sensitive to supply voltage variations at the same time [37].

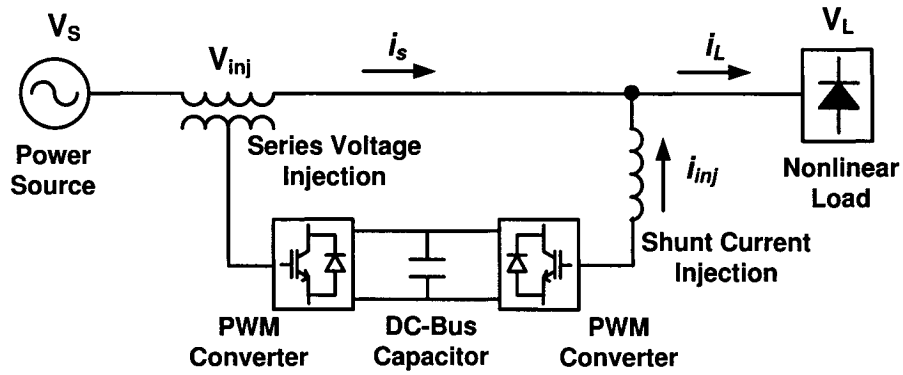


Fig. 1.7. The combined series-parallel power quality compensator.

1.4 PREVIOUS WORK

This thesis draws on work done in the area of power quality compensators and in the complementary area of modern drives. In recent years, significant improvements have been achieved, which allow a higher quality power to be supplied to critical loads. The review of the previous work is divided into three categories according to the three converter configurations: series, shunt and combined.

1.4.1 Static Series Compensators

A static synchronous series compensator was presented in [30] for power quality compensation on power transmission lines. The paper was aimed to enhance the stability in transmission systems, and the proposed control scheme was designed for thyristor or GTO based converters applied at high power level, in which the switching frequency is limited to less than 500 Hz.

A series of applications of the static series compensator using high switching frequency IGBT converters were firstly reported in [39][40][41]. Work [39] claims that it is possible to regulate the load voltage using only reactive power injection and no real power is then required from the compensator and the dc bus. It also presented the use of series compensators to improve the power factor for reactive loads, as a by-product of voltage regulation. The principle of operation was extended and improved in more recent works [42][43]. However, it was found that the control methods for power improvement significantly increased the compensator's power rating and severely restricted the range of voltage sags that can be compensated.

In [40], a static series compensator, consisting of three single-phase voltage source inverters, is proposed for unbalanced three-phase voltage compensation. The use of high switching frequency PWM converters results in fast dynamic response. Also because of the high switching frequency used, the compensator sees a considerable reduction in the size of the output LC filter.

A different compensator topology, as an alternative to [40], is presented in [41]. It uses a three-phase PWM converter to reduce the number of IGBT power switches, and operates with unbalanced switching functions.

A number of fast control algorithms for voltage fault compensation in distribution systems, including three-phase four-wire systems, are proposed in [44]. The proposed reference generation scheme is robust under various fault conditions and not computational intensive. A control scheme has also been proposed to use only two single-phase voltage source inverters for the three-phase unbalanced voltage fault compensation in three-phase three-wire power systems.

A control scheme based on three-phase current source converter was reported in [45] for series compensation, in which the supplemental modulation index control method is used to obtain high compensation performance.

A series var compensator using multi-level voltage source inverters was presented in [46] without the use of series coupling transformers. By using cascaded multilevel inverters, fast dynamic response is achieved with low switching frequencies, and the self-controlled dc-bus voltage simplified the implementation.

The constraint on response time of voltage compensation leads to most reported control strategies using open-loop feed forward control. Literatures [47][48][49] show

that the open-loop control produces a poorly damped response with the presence of the switching harmonic LC filter connected at the converter output side, and it is unclear how errors in the system (such as parameter variations, saturation of the series injection transformer, PWM blanking time effects, quantization effects) can affect the performance of the series compensator.

Closed-loop control permits active damping of the LC filter, and a closer tracking of the reference load voltage. Many control structures have been tried. However, to date few papers on closed-loop feedback control were reported [50]. Multi-loop PI feedback control was comprehensively investigated in [51] in terms of stability margins, frequency response and damping performance. But multi-loop PI control has difficulties meeting the fast dynamic response requirement due to the dynamic separation of the cascaded outer voltage control loop and inner current control loop.

A selective harmonic closed-loop feedback control for voltage harmonic compensation was proposed recently in [52]. However, the selective harmonic controllers (such as 5th and 7th resonant controllers) are stacked into the existing voltage sag controller, and the selective harmonic controller itself is limited to voltage harmonic compensation. Since the selective harmonic controller assumes a constant control reference (null value), while the control reference is time varying for three-phase unbalanced voltage fault compensation in synchronously rotating *d-q* coordinates, which is different from other power conversion applications [53].

Closed-loop feedback control of the static series compensator has attracted considerable attention in recent years, in which the improvement of the dynamic performance is of great importance.

1.4.2 Static Shunt Compensators

A general description of the static synchronous shunt compensator (STATCOM) was presented in [68][69], which described the operational principles and advantages of STATCOM. One of the outstanding advantage of STATCOM is that power storage component is not required in principle. While the two papers were designed for high power applications using thyristor or GTO power switches that generates a large amount of harmonics because of the slow switching frequency.

A STATCOM based on high switching frequency PWM converter was proposed in [70], in which the system is in a closed-loop control fashion, and a proportional-integral controller has been designed and implemented. Theoretical analysis of the power stage and the controller was presented and the system transfer functions were also derived.

A similar control scheme was also applied to STATCOM based on multilevel inverters [71]. In addition, a per-phase based instantaneous *d-q* transformation and the phase-shifted control of the dc-bus voltage were also proposed.

STATCOM is mainly used for reactive power compensation. In recent years, STATCOM is also used to reduce the level of harmonics in distribution systems [72][73], and is also called as active filter in medium and low power level applications. By a similar argument, STATCOM is also applied to voltage flicker mitigation [74].

A detailed design procedure for active filters was presented in [75]. The active filter focuses on compensating harmonics generated by non-linear loads. This paper presented comprehensive analysis and design procedures for the PI controller and the triangular-carrier PWM pattern generator.

A closed-loop selective harmonic compensation algorithm for active filters was proposed in [76]. And a number of high performance control strategies for active filter applications have been reported in recent years.

Multi-loop PI control is the most commonly used control strategy for STATCOMs and active filters that installed in industrial sites. The control system comprises of two cascaded control loops, an inner current control loop and an outer dc-bus voltage control loop. Typically, the inner current loop is fast, whereas the outer voltage loop is much slower (in the order of ten times or more) because of the dynamic separation requirement of the two cascaded loops. A new control structure based on the instantaneous power theory [77][78], called as direct torque control [79][80][81][86], was proposed for motor drive applications. Then the control structure was extended to the synchronous rectifier applications [88][89], in which it controls simultaneously the instantaneous active power and reactive power, and is called direct power control (DPC). DPC is a promising control strategy, however, extending the DPC control structure and applying to the active filter and STATCOM application has not been attempted so far.

A new three-phase active filter topology based on reduced four-switch voltage source converter was proposed in [99]. The paper analyzed the impact of the reduced switch count on power circuit design, and investigated the dc-bus voltage requirement of the four-switch compensator for load harmonics filtering. The paper demonstrated that, compared to its six-switch counterpart, the four-switch compensator is a viable alternative with a lower cost.

1.4.3 Combined Series-Parallel Compensators

Applying the combined series-parallel compensator to deal with fundamental frequency components in ac systems at high power level, such as reactive power compensation, power flow control and voltage regulation, was presented in a number of papers [105][106][107]. In these applications, the combined series-parallel compensator is called the Unified Power Flow Controller (UPFC). To control the UPFC, the power terms based on the product of rms voltage and current are used. The process of calculating rms values of the voltage and current degrades the dynamic performance of the UPFC during transients. The alternative method uses the *d-q* frame transformation as reported in [108][109][110]. However, this method is subject to the limitation of implicitly considering only the positive sequence component of the voltage. The difficulty here is the development of controllers that are capable of dealing with unbalanced and distorted voltages.

More general control capability enables the PWM converters to perform not only the function of a UPFC, but also the function of active filtering of harmonics. In this case, the unified series-parallel compensator is called the Unified Power Quality Conditioner (UPQC). The functions of the UPQC are grouped into two classes: (a) fundamental power compensation, such as power flow control and voltage regulation, and (b) harmonic power compensation. The control structure of UPQC determines its compensation characteristics.

Since the control of the UPQC is performed in *d-q* frame, a fast Phase Locked Loop is essential for algorithm implementation. This scheme works well in steady state, but its dynamic response is limited by the delay of instantaneous *d-q* transformation. Besides,

any improper allocation of the parameters during *d-q* decoupling calculation may introduce system oscillation in transients. The similar control scheme was also applied to UPQC based on multilevel voltage-source converters [111].

In [112], a general control algorithm for UPQC is proposed based on the instantaneous real and imaginary power theory. High-pass filters and PI controllers are used for error extraction and amplification. The series converter uses a triangular carrier PWM generator and the shunt converter uses a hysteresis PWM generator. Since the instantaneous power is extracted based on the product of voltage and current, the performance of this scheme is detrimentally affected by unbalanced supply voltage faults.

In [113], a combined series-parallel converter system is applied successfully in single-phase power systems. Unlike the aforementioned control schemes, the series converter is used for current control and the shunt converter is used for voltage control. This initiates a different way to control the series-parallel converter systems. In this paper, the PI control structure is still kept. The PI controller may encounter difficulties when the control references are time varying ac quantities.

The deadbeat control provides very fast transient response, and much research work has been done in recent years, especially oriented to motor drive, UPS and active filter applications. In literature [114], a deadbeat controller for the three-phase PWM converter with an output LC filter is presented based on the synchronously rotating *d-q* frame. The algorithm includes a current minor loop and a voltage control loop. The *d-q* components are cross-coupled, and the paper has developed two decoupled deadbeat controllers for the *d* and *q* components respectively. In [115], a disturbance-observer based deadbeat controller is proposed for UPS applications. The pole placement of the state observer and

that of the disturbance observer are chosen separately, in which the dynamics of the disturbance observer is faster than that of the state variable observer. This scheme shows advantages in terms of system robustness, in addition, the system model is based on the stationary α–β coordinates and therefore, the state variables are not cross-coupled. In [116], the performance of the deadbeat controller for a three-phase inverter under no load and various load conditions are investigated. In [117], a deadbeat current controller is proposed with an improved line voltage estimation technique for active filter applications. It has investigated the stability margins of the algorithm with respect to parameter mismatches. In [118], a deadbeat adaptive hysteresis current controller is presented to achieve the fixed PWM switching frequency of the converter. The system is digitally implemented with minimal external analog circuits. In [119], a deadbeat controller for line current detection type active filters is proposed by using the capacitor voltage as control intermediate, the output current of the active filter is regulated exactly equal to the current reference at the next sampling instant.

In [120][121], the concept of unified deadbeat control is proposed for the combinations of the series-parallel converters. The series-parallel converters are operated in the way similar to that in [113], and the control system provides a fast dynamic response. In terms of hardware design, two microprocessor control boards have been used to provide a high controller sampling frequency and a high PWM switching frequency that are essential to implement the deadbeat control law. It is possible to reduce the computational burden of the controller by changing the operation modes of the two converters, the system modeling approach and the PWM scheme. This will lead to the

simplification of the hardware structure and the improvement of the system performance in case of control saturation.

1.4.4 Technology Trends

There have been significant recent developments in motor drives, mostly ac induction motor drives. These developments have led to the optimization of the following components:

(i) Power circuits: two-level converters are standard units for low and medium voltage drives, up to about 1 MW, with three-level IGBT or IGCT converters used for larger power (up to 5 MW). Multi-pulse converters have also been implemented, based on stacked single-phase converters.

(ii) Control circuits: microprocessor and DSP based controllers have been developed, with special features such as field oriented control (*dq* decoupling), direct torque control and sensorless control.

(iii) The common configuration uses a diode rectifier front-end with a PWM inverter to supply the induction motor. Active front-end rectifiers are becoming more standard.

(iv) Most of the power converter topologies used today are based on the voltage source converter structure. This is the result of technological developments in switches (reverse blocking switches are less available), the advantages of the voltage source converter structure (capacitors are more readily available than inductors and losses are lower), and the flexibility provided by a voltage source type energy storage.

All these developments have significantly reduced the cost and increased the reliability of power converters used in medium and high power applications. The use of the technology in power quality applications has therefore been, for drive manufacturers, a natural extension of this technology. Most drive manufacturers are now proposing power quality compensation equipment, based on their drive technologies. These include static var compensators, active harmonic filters and series compensators.

Although ac drives can be reconfigured to serve as power quality compensation devices, a number of significant modifications must be made to the basic control system configuration. In many cases, the complete control scheme must be modified. In addition, a system approach must be used to optimize power quality compensation devices: the rectifier used in a typical drive, particularly an active front-end drive, can have many more functions in a combined series-parallel power quality compensator.

The static power quality compensator uses the DSP-based controller to implement advanced control algorithms and hence improve the steady state, and especially the dynamic performance. The new generation of DSP controllers greatly improves the prospects for applying power electronics to new power conditioning applications, and the new design methodologies have greatly enhanced the quality of implementation. In the thesis, the proposed control algorithms are implemented using the MATLAB/Simulink programming platform, and the application-specific C language and script language M-files which are integrated into the Simulink modules in form of user-defined S-functions.

1.5 THESIS SCOPE AND CONTRIBUTIONS

The scope of this thesis is to propose, analyze, design, and verify by simulation and experiments, high performance power quality compensators. It deals with three-phase power distribution systems, particularly the unbalanced and distorted systems, and provides solutions to most prevalent power quality problems. The enhancements cover the global control functions as well as direct converter control and PWM functions. To the best of the knowledge of the author, the contributions of the thesis are:

(i) A reduced switch-count compensator topology is proposed based on the four-switch three-phase voltage source converter. Since there are only two degrees of freedom available for control in a three-phase three-wire ac system, the four-switch converter is adequate to regulate two of the three line-to-line voltages or currents. The specified control strategies are proposed for voltage or current injection, and the resulting performance of the power quality compensator has not been degraded with the four-switch converter topology (Chapter 2 and Ref. [127]).

(ii) A classification method is developed that catalogues all voltage faults into three types in power distribution systems with delta-wye, delta-delta, wye-delta or wye-wye connected transformers. Three control reference generation options are proposed for voltage fault compensation, which choose to synchronize the control reference with the pre-fault voltage, the phase-*a* of the post-fault voltage or the positive sequence of the post-fault voltage respectively. The thesis proves that a minimum amount of voltage injection is required in most cases by taking the third

option, in which the control reference is synchronized with the positive sequence of the post-fault voltage (Chapter 3 and Ref. [129]).

(iii) A state feedback control algorithm is developed for the static series compensator that deals with time varying control references. It provides a better performance, in particular a faster dynamic response for voltage sags compensation, compared to the existing open-loop and closed-loop control algorithms that have been reported so far (Chapter 3 and Ref. [130][131]).

(iv) Appropriate active and reactive power terms are reformulated for load harmonics and reactive power compensation, and the characteristics of the corresponding power terms are derived (Chapter 4 and Ref. [135]).

(v) A direct power control algorithm is developed for the static shunt compensator. Specific PWM switching functions are obtained based on power flow control, and the control of multiple variables (three-phase line currents and dc-bus voltage) is integrated into one control loop to obtain a simple control structure and a fast dynamic response (Chapter 4 and Ref. [136][137]).

(vi) A unified deadbeat control algorithm is proposed for the combined series-parallel compensator. The two converters are modeled as a single multi-input and multi-output system to accomplish unified control of the two converters, and two identical deadbeat controllers are implemented for the two first-order equivalent systems. In addition, the inherent computing time delay caused by the deadbeat control algorithm is compensated by the proposed control strategy (Chapter 5 and Ref. [138][139]).

1.6 THESIS OUTLINE

The thesis is organized as follows.

Chapter 2 proposes two topologies of the static power quality compensator based on four-switch three-phase voltage source converter for voltage fault compensation and harmonic current filtering. Compared to the commonly used six-switch counterpart, the four-switch converter saves two power switches, at the same time, the four-switch converter incurs two times as high as the dc-bus voltage requirement, and the asymmetry in power circuit structure. Consequently, the four-switch converter produces larger dc-bus voltage ripples and is more sensitive to the unequal sharing of dc-bus voltages between the split capacitors. These issues have been addressed during the corresponding control system design. The experimental results indicate that the proposed four-switch converter is a viable alternative to the conventional six-switch counterpart with a lower cost and without compromising of performance.

Chapter 3 presents a state feedback control algorithm for the static series compensator. Most of the reported control strategies use open-loop feed forward control for voltage compensation, since the industrial equipment is generally sensitive to voltage sags and requires a fast dynamic response of the series voltage compensator. However, the open-loop control produces a poorly damped response with the presence of the LC filter. Closed-loop control permits active damping of the LC filter, but the commonly used multi-loop PI feedback control has difficulties meeting the fast dynamic response requirement due to the dynamic separation of the two cascaded control loops. The proposed state feedback control algorithm removes the inner current control loop that included in the multi-loop PI control structure, instead, the converter output current and

its derivative are used to reflect the load changes and to increase the dynamic response of the control system. In addition, a software based current observer is accomplished to obtain the instantaneous values of the output current and its derivative. The theoretical considerations are verified through simulation and experimental tests.

Chapter 4 develops a direct power control structure for active filters and static var compensators. The instantaneous active and reactive power terms are appropriately reformulated, and the proposed controller directly uses the instantaneous power terms as control variables to replace the current and voltage variables that are used in multi-loop PI control structures. It provides a systematic approach to derive the specific PWM switching functions based on the instantaneous power flow regulation, and demonstrates that full control of the active filter, including the line current and the dc-bus voltage, can be accomplished within an integrated power control loop. The advantages of the proposed control strategy are illustrated by experimental results on a 2 kVA laboratory prototype.

Chapter 5 proposes a unified deadbeat control algorithm for the combined series-parallel compensator. The combination of the two converters is modeled as a single multi-input and multi-output system, and the unified controller regulates the line current and load voltage simultaneously. The control algorithm decouples the three-phase ac system into two single-phase systems through abc-$\alpha\beta$ transformation, and two identical deadbeat controllers are implemented for the two first-order equivalent systems. In addition, the inherent time delay caused by the DSP controller for deadbeat algorithm computation is compensated by the proposed control strategy. Compared to other control schemes based on individual control of the two converters, simulation and experimental

results confirm that the unified control achieves deadbeat response of the overall system and demonstrates good disturbance rejection characteristics.

Chapter 6 contains the conclusions and suggestions for further study.

CHAPTER 2

STATIC COMPENSATORS BASED ON FOUR-SWITCH CONVERTER STRUCTURE

2.1 INTRODUCTION

The three-phase four-switch PWM voltage source converter is receiving more attention recently. However, its current applications are mainly aimed at ac induction motor drives and brushless dc motor drives [83]. Most of the reported control and PWM modulation algorithms in conjunction with four-switch converters are implemented to produce the desired dynamic and static speed-torque characteristics for motor drives. In particular, a four-switch inverter specific space vector modulation strategy (voltage controlled PWM) was presented in [95], and a direct current controlled PWM method was presented in [96]. The developments indicate that a four-switch converter could be a good alternative to the conventional six-switch counterpart with a lower cost and without compromising of performance.

This chapter extends the advances made in motor drives to the power quality compensation applications based on the four-switch converter topology. These include the dynamic voltage restorer (DVR) for series compensation, and the active filter for shunt compensation. Since there are only two degrees of freedom available for control in a three-phase three-wire system, the four-switch converter is adequate to regulate two of the line-to-line voltages or currents. The disadvantages of the four-switch converter have also been investigated in this chapter. As mentioned in the previous work [97], the main

drawbacks of the four-switch converter include its higher dc-bus voltage requirement and the asymmetry in circuit structure. Consequently, the four-switch converter produces larger dc-bus voltage ripples than its six-switch counterpart and is more sensitive to the unequal sharing of dc-bus voltage between the split capacitors. These issues have been addressed to enhance the power conditioning performance.

For dynamic voltage sag compensation, the four-switch three-phase converter is configured as a DVR. It provides line voltage support by inserting a voltage in series between the supply and the load. In normal configuration with six-switch converters, the DVR acts as a controllable three-phase voltage source. With four-switch converter topology, the two phase voltages connected to the converter legs are controllable, whereas the voltage of the third phase comes from the midpoint of the split-capacitor bank, and its value is uncontrollable. Therefore, series voltage compensation based on the four-switch converter leads to the requirement of modifying the power circuit configuration and the associated control algorithms. The four-switch series compensator has been investigated in [98]. This chapter proposes an improved voltage balancing and regulating algorithm, which minimizes the compensation errors caused by the dc-bus voltage variation and the series coupling transformer.

For load harmonic current compensation, the four-switch three-phase converter is configured as an active filter. It injects a controllable amount of current into the power feeder such that the harmonics produced by the nonlinear load can be cancelled out. With four-switch converter topology, one phase is connected to the midpoint of the dc-link split capacitor bank through an inductor, and the current of this phase is uncontrolled, instead, the resultant currents of the other two phases flow through this phase. This

imposes a limitation on the controller design. A three-phase active filter topology based on four-switch converter was presented in [99], and a reduced hysteresis controller for a four-switch three-phase ac/dc rectifier was proposed in [100]. However, the performance of these control algorithms depends on the fast signal processing capability of the controller to extract the high frequency load current harmonics in each sampling period. This chapter proposes a more practical solution that doesn't require a high sampling frequency of the controller. It is based on supply current reaction paradigm, which simply forces the supply current to be sinusoidal and gets rid of the load harmonic current extraction requirement. Furthermore, this chapter also indicates that the current controller is preferred to be per-phase based, where phase-*a* and phase-*b* currents are sensed and controlled independently. This helps blocking of the influence of dc-bus voltage unbalance between the split dc-link capacitors. Simulation and experimental tests on laboratory prototypes confirm the viability of the theoretical considerations.

2.2 POWER CIRCUIT ANALYSIS

The power circuit of the DVR based on four-switch converter topology is shown in Fig. 2.1. In this configuration, no voltage is injected to the third line, and the supply voltage is directly applied across the load. The three-phase four-switch converter is decoupled into two single-phase converters, and the midpoint of the dc-bus split capacitors serves as a return wire. The output of the converter is connected to a low-pass LC filter, to eliminate high frequency harmonics caused by the switching actions of the converter.

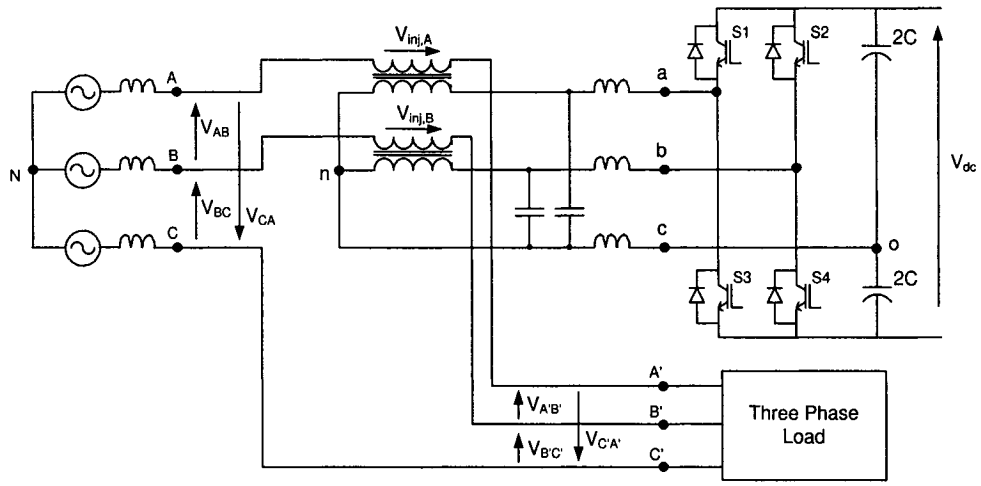


Fig. 2.1. Power circuit of the DVR based on four-switch voltage source converter.

The power circuit of the proposed active filter based on four-switch converter is shown in Fig. 2.2. In three-phase three-wire systems, control of two line currents gives full control over all three line currents. Therefore, the current in the third phase is controlled according to Kirchhoff's current law.

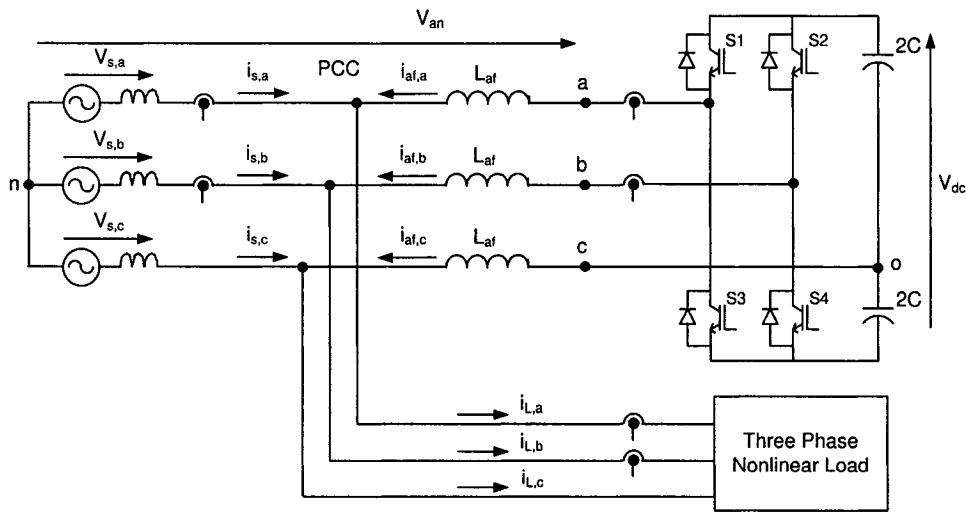


Fig. 2.2. Power circuit of the active filter based on four-switch converter.

It is shown that at the heart of the series and shunt compensators is a four-switch three-phase voltage source converter, and the converter output voltage can be obtained by writing the Kirchhoff's equations as

$$\begin{aligned} v_{an} &= v_{ao} + v_{on} \\ v_{bn} &= v_{bo} + v_{on} \\ v_{cn} &= v_{on} \end{aligned} \tag{2.1}$$

By summing the three equations, we obtain,

$$v_{on} = -\frac{(v_{ao} + v_{bo})}{3} \tag{2.2}$$

Substituting (2.2) in (2.1), we obtain,

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} \\ -\frac{1}{3} & -\frac{1}{3} \end{bmatrix} \cdot \begin{bmatrix} v_{ao} \\ v_{bo} \end{bmatrix} \tag{2.3}$$

In the four-switch configuration, there are four switching modes defined as (0,0), (0,1), (1,0) and (1,1). By the definition, "0" represents the lower switch is turned on and "1" the upper switch is turned on. The two switches on the same converter leg never turn on or off simultaneously. Based on the switching modes S_a and S_b listed in Table 2.1, the converter output voltage is derived as follows.

$$\begin{bmatrix} V_{ao}(k) \\ V_{bo}(k) \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} 2S_a - 1 \\ 2S_b - 1 \end{bmatrix} \tag{2.4}$$

Substituting (2.4) in (2.3) yields,

$$\begin{bmatrix} V_{an}(k) \\ V_{bn}(k) \\ V_{cn}(k) \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} S_{wa}(k) \\ S_{wb}(k) \\ S_{wc}(k) \end{bmatrix} \tag{2.5}$$

where

$$\begin{bmatrix} S_{wa}(k) \\ S_{wb}(k) \\ S_{wc}(k) \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} \\ -\frac{1}{3} & -\frac{1}{3} \end{bmatrix} \cdot \begin{bmatrix} 2S_a - 1 \\ 2S_b - 1 \end{bmatrix} \tag{2.6}$$

To facilitate the further analysis, the three-phase voltage is transformed into α–β plane. The transformation is defined as,

$$\mathbf{V}_{4sw}(k) = \begin{bmatrix} V_{4sw,\alpha}(k) \\ V_{4sw,\beta}(k) \end{bmatrix} = \mathbf{T} \cdot \begin{bmatrix} V_{an}(k) \\ V_{bn}(k) \\ V_{cn}(k) \end{bmatrix} \tag{2.7}$$

where

$$\mathbf{T} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2.8}$$

Table 2.1. Switching Modes and Voltage Vectors of the Four-Switch Converter.

Mode (k)	S_a	S_b	$V_{an}(k)$	$V_{bn}(k)$	$V_{cn}(k)$	$V_{4sw}(k)$
1	0	0	$-V_{dc}/6$	$-V_{dc}/6$	$V_{dc}/3$	$\frac{V_{dc}}{3} e^{-\frac{j2\pi}{3}}$
2	1	0	$V_{dc}/2$	$-V_{dc}/2$	0	$\frac{V_{dc}}{\sqrt{3}} e^{-\frac{j\pi}{6}}$
3	1	1	$V_{dc}/6$	$V_{dc}/6$	$-V_{dc}/3$	$\frac{V_{dc}}{3} e^{\frac{j\pi}{3}}$
4	0	1	$-V_{dc}/2$	$V_{dc}/2$	0	$\frac{V_{dc}}{\sqrt{3}} e^{\frac{j5\pi}{6}}$

There are four voltage space vectors in the α–β plane for the four-switch converters. With the help of graphical representation, these four voltage vectors form a parallelogram, as shown in Fig. 2.3. For the purpose of comparison, the voltage space vectors of a six-switch PWM converter is also presented in Fig. 2.4.

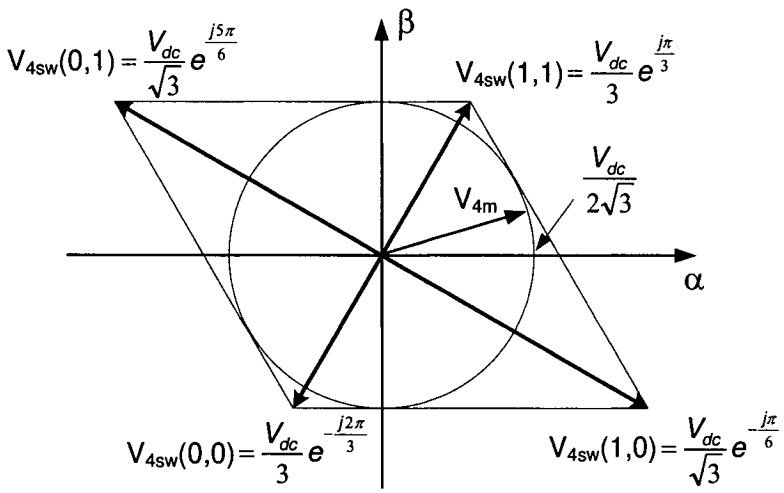


Fig. 2.3. The voltage space vectors of the four-switch converter.

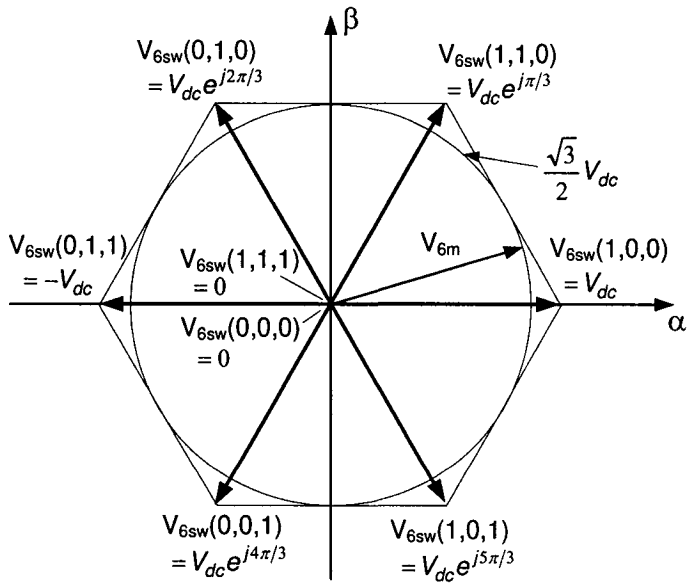


Fig. 2.4. The voltage space vectors of the six-switch converter.

By applying the virtual flux concept of the PWM voltage source converter, the four output voltage vectors of the four-switch converter generate a mean voltage vector $\mathbf{V_{4m}}$. In each switching period T_{sw}, $\mathbf{V_{4m}}$ generates a converter flux increase $\Delta\psi_4$ that is given as

$$\Delta\psi_4(T_{sw}) = \int_{t_0}^{t_0+T_{sw}} V_{4m} \cdot dt \tag{2.9}$$

To obtain a sinusoidal converter flux, it is necessary that the trajectory of the mean voltage vector is a circular path. If over modulation is not considered, the critical condition happens when the circle is inside tangent to the parallelogram. This boundary condition represents the maximum value of the mean voltage vector that is $V_{dc}/2\sqrt{3}$. Compared to Fig. 2.4, it is shown that the asymmetric voltage space vectors have reduced the maximum obtainable mean voltage to 1/3 of that of its six-switch counterpart.

From another point of view, it is found that the maximum obtainable peak voltage of four-switch converters is reduced to 1/2 of that of the six-switch counterpart, which is explained as follows. Due to the circuit configuration of the four-switch converter, the maximum obtainable peak value of the line-to-line voltage equals to $V_{dc}/2$. With the six-switch converter under the same condition, the maximum obtainable peak value of the line-to-line voltage reaches V_{dc}.

As a conclusion, in order to support a same load, the four-switch converter requires the dc-bus voltage to be controlled to a much higher level, usually two times as high as that of its six-switch counterpart.

Another disadvantage of the four-switch converter is the increased switching losses. Although the number of switches is reduced by 1/3 with the four-switch converter, its dc-

bus voltage is doubled compared to the six-switch counterpart, and it consumes approximately 1/3 extra switching losses when feeding the same current to a load.

Despite these drawbacks, a cost reduction is still achieved by using a four-switch converter to replace the six-switch counterpart in many power conditioning applications.

2.3 CONTROL ALGORITHMS FOR LINE VOLTAGE COMPENSATION

When the four-switch converter is acting as a DVR for line voltage compensation, the output voltage of the converter is injected to line *a* and line *b*, via series coupling transformers, as shown in Fig. 2.1. The voltage of the third line is directly supplied from the ac system to the load without any compensation.

The injected voltage is capable of performing a number of functions, such as voltage sags compensation and power factor control. The algorithm presented in this chapter focuses on amplitude regulation and unbalance compensation. Feed forward control is used to achieve fast compensation characteristics. There are two schemes for control reference generation: (a) Extraction of sequence components. This technique may result in slow dynamic response, since sequence component extraction requires appreciable processing time for signal filtering and computation. (b) Synthesis of the voltage reference from the available voltages. The magnitude is set arbitrarily, however, the phase angle should be set so as to minimize the voltage injection from the compensator. The difficulty exists in the fact that under fault conditions, one or more phase voltages may drop to zero. A synchronization voltage, available under all operating conditions, must be produced.

The proposed control algorithm ensures the availability of control reference under all fault conditions. In typical industrial power systems, the line voltages $v_{ab}(t)$ and $v_{ca}(t)$ never go to zero at the same time. The synchronization signal is extracted based on two of the line-to-line voltages, and tracks the phase *a* of supply voltage. It is written as,

$$v_{syn}(t) = \frac{v_{ab}(t) - v_{ca}(t)}{3} = V_a \cdot \sin(\omega t + \varphi_a) \tag{2.10}$$

In order to get the instantaneous phase angle of the reference voltage, a fast algorithm is presented to derive the phase angle φ_a based on sensed data in a short time window using two samples of the signal $v_{syn}(t)$. Let $v_{syn}(k+1)$ and $v_{syn}(k)$ represent the signals at instant t_{k+1} and t_k respectively, the instantaneous phase angle is given by the following equation:

$$\varphi_a = \tan^{-1}\left[\frac{v_{syn}(k)\cdot\sin(\omega t_{k+1}) - v_{syn}(k+1)\cdot\sin(\omega t_k)}{v_{syn}(k+1)\cdot\cos(\omega t_k) - v_{syn}(k)\cdot\cos(\omega t_{k+1})}\right] \tag{2.11}$$

This signal is then used to generate the three-phase line-to-line voltage reference for the voltage balancing and regulating algorithm, as Fig. 2.5 shows,

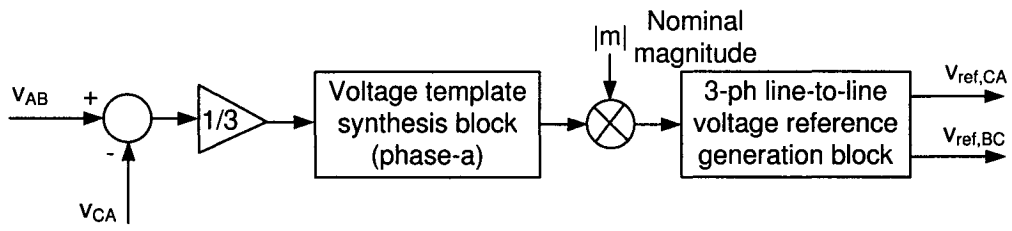


Fig. 2.5. Block diagram of the DVR control reference generation system.

The triangular carrier PWM technique is used to generate the modulating signals of the voltage source converter. The dc-bus voltage of the converter is supplied by a diode-bridge rectifier. Any of the voltage variations in the ac mains may cause the dc-bus voltage ripple. In order to eliminate the influence of dc-bus voltage variation, the dc bus

voltage is sensed and sent to the DVR controller. The required compensating voltage is divided by the sensed dc-bus voltage to calculate the modulating signals. The modulation signal of the converter is given by (2.12). As the dc-bus voltage drops, the modulation index increases.

$$V_{\mathrm{mod},a} = -\frac{V_{ref,CA} - V_{CA}}{(1+\alpha_z)\cdot\gamma_n \cdot G_c \cdot V_{dc}}$$
$$V_{\mathrm{mod},b} = \frac{V_{ref,BC} - V_{BC}}{(1+\alpha_z)\cdot\gamma_n \cdot G_c \cdot V_{dc}} \qquad (2.12)$$

Where G_c is the converter ac gain, which is defined as the required *pu* value of the modulation signal to obtain an unity modulation. α_z is the coefficient to compensate the voltage drop on converter ac-link inductors, and γ_n is the turns ratio of the series transformer. The control of DVR is based on a feed forward technique, and the block diagram of the control system is shown in Fig. 2.6.

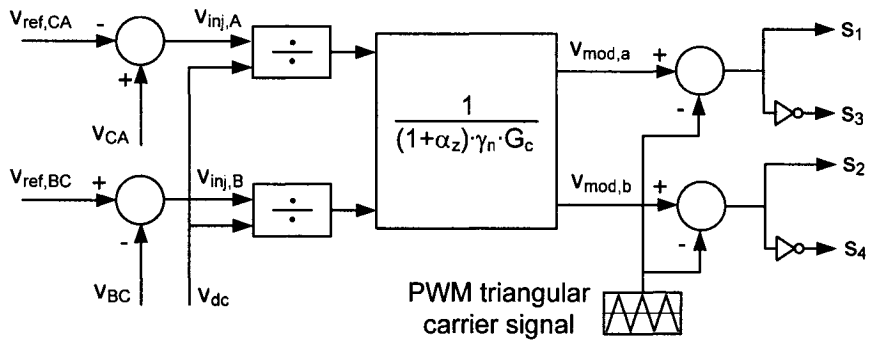
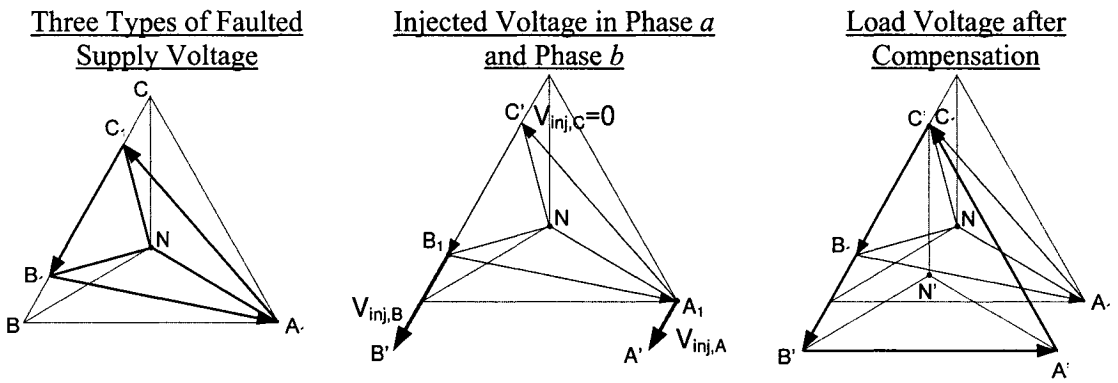


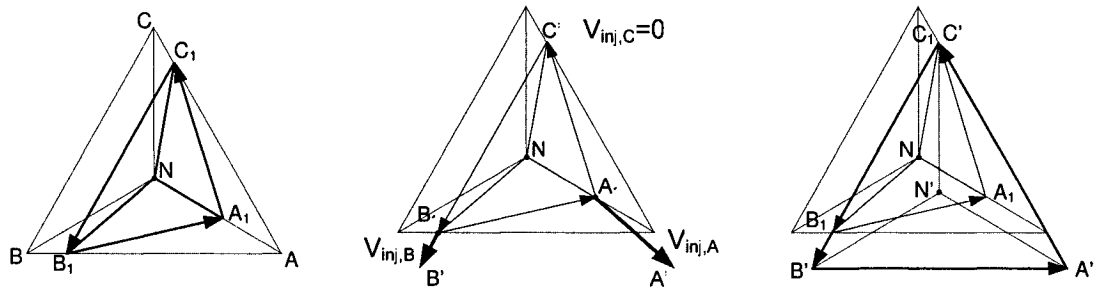
Fig. 2.6. Block diagram of the proposed DVR voltage control system.

In typical three-phase three-wire distribution systems with Y/Y, Y/Δ, Δ/Δ or Δ/Y distribution transformers, the voltage sags can be classified into three types [59]. The three types of supply voltage faults are shown in Fig. 2.7 when the phase angle jump is not considered, and the load voltages after compensation are also illustrated based on the proposed two phases voltage injection scheme. If a phase jump is associated with

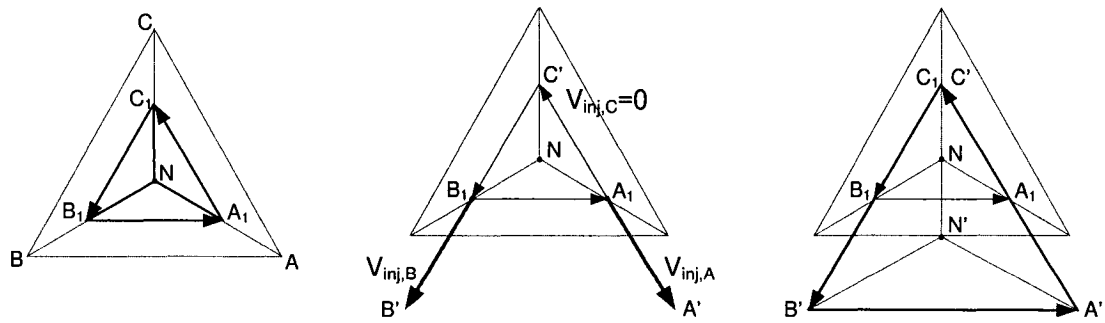
corresponding voltage faults, the faulted supply voltage vector should rotate a certain angle from its current position, and the similar compensation results can be concluded. It is shown that the line-to-line load voltages are three-phase balanced and of nominal amplitude after compensation.



(a) Compensation for a non-symmetrical two-phase voltage fault.



(b) Compensation for a non-symmetrical three-phase voltage fault.



(c) Compensation for a symmetrical three-phase voltage fault.

Fig. 2.7. Two-phase voltage injection vector diagrams for the compensation of three-phase supply voltage faults.

2.4 CONTROL ALGORITHMS FOR LOAD HARMONICS COMPENSATION

The active filter based on four-switch converter injects two phases (phase *a* and phase *b*) of harmonic current into the point-of-common-coupling (PCC), and the current in phase *c* is automatically controlled according to Kirchhoff's current law. Most of the active filters established in industrial sites directly use load current control algorithm, in which the controller senses the harmonic current drawn by the nonlinear load, and the active filter injects a same amount of harmonic current to supply the load, therefore, the supply current remains sinusoidal. However, the load harmonics sensing technique requires a fast processing capability of the controller to reduce the time delay caused by sampling A/D conversion. The sampling delay introduces phase shift errors of the load harmonics, and results in line current spikes. In practical implementations, the analog controller is generally used to implement the load harmonic current sensing technique, so as to minimize the sampling A/D conversion time delay.

An alternative control algorithm based on supply current reaction paradigm is presented in this section that is well suited for digital control implementation. The controller senses the fundamental frequency supply current, and forces the supply current to be a three-phase 60 Hz sinusoidal signal. Since the DSP controller does not have to sense the high frequency load harmonics, the relatively slow sampling frequency of the DSP controller will not degrade the harmonic filtering performance.

2.4.1 Load Current Sensing Scheme with Analog Control

The analog controller provides fast signal processing capability that is required for high frequency harmonics filtering. The load current sensing control structure consists of

an inner current control loop and an outer voltage control loop, and the control reference is obtained through load harmonic current sensing, as Fig. 2.8 shows.

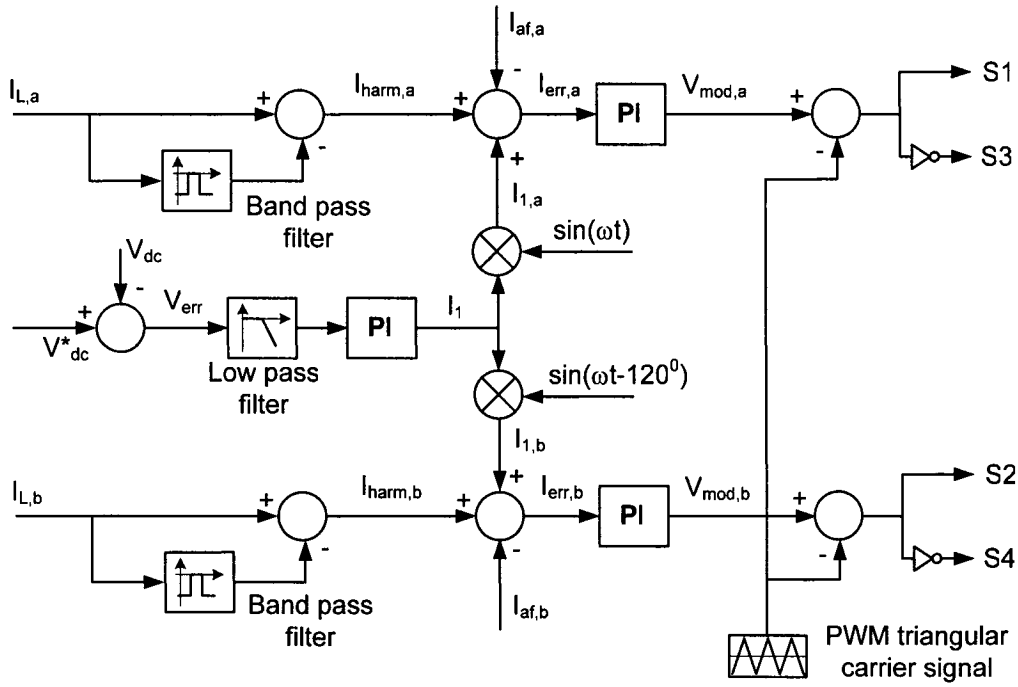


Fig. 2.8. Block diagram of the control system based on load current sensing.

The inner current control loop possesses very fast dynamic response. The harmonic components of the load current are obtained by extracting the fundamental component through a band-pass filter, then subtracting this fundamental component from the load current. A fixed switching frequency triangular carrier PWM generator is used in this implementation.

The dc-bus voltage control loop adjusts a small amount of real power flowing into the dc capacitor, thus to maintain a constant dc bus voltage and compensate the converter losses. The dc-bus voltage error is multiplied by a sine-wave template to synthesize a small fundamental frequency current component. This component is then added to the current control reference.

The analog controller is focused on compensating harmonic currents produced by the nonlinear load. Generally, the active filter does not inject fundamental frequency reactive current into the distribution system (for power factor improvement). Therefore, the power rating of the active filter can be reduced to just a fraction of that of the non-linear load.

2.4.2 Supply Current Sensing Scheme with Digital Control

Digital control is attractive because of the applicability of versatile control algorithms. In the area of active filter applications, the main constraint to digital control is the relatively slow sampling frequency of DSP controller. The appreciable processing time causes delay of the sampling A/D conversion, and the absence of sensible effects produces line current spikes.

In order to handle the high frequency load harmonics by using a relatively slow DSP controller, a practical solution is presented in this section, in which the control algorithm is based on supply current reaction. The digital controller simply forces the supply current to be sinusoidal, regardless of the load current. The reference current magnitude is derived from the dc-bus voltage regulation loop, and it is then modulated into a three-phase 60 Hz signal based on PCC voltage template. The proposed digital control algorithm is quite different from that of the analog control. The current reference in digital controller is a three-phase fundamental frequency sinusoidal signal, whereas the current reference in analog controller is high frequency harmonics that are mainly comprised of 5^{th}, 7^{th} and 11^{th} components.

Why the digital controller based on supply current sensing could eliminate line current spikes? Selecting the sampling time of the DSP controller at 50 μs as an example, the corresponding phase delays are 7.56° for 7^{th} harmonic sensing, 5.4° for 5^{th} harmonic

sensing, and merely 1.08° for 60 Hz supply current sensing. In addition, both the supply current and the current reference are 60 Hz sinusoidal signals, the phase delay caused by supply current sensing will not degrade the resulting line current waveform, instead, it only causes a small reactive power absorption.

The operational principle of the proposed supply current sensing algorithm is explained as follows taking phase *a* as an example. The load current in phase *a* drawn by the nonlinear load is written as

$$i_{load,a} = I_{Lp,a} \sin \omega t + I_{Lq,a} \cos \omega t + \sum_{h=5,7,11} I_{Lh,a} \sin\left(h\omega t + \varphi_{h,a}\right) \tag{2.13}$$

Where $I_{Lp,a}$ is the amplitude of the in-phase component of the load current, $I_{Lq,a}$ is the amplitude of the quadrature component of the load current, and $I_{Lh,a}$ is the amplitude of the harmonic component (5^{th}, 7^{th}, 11^{th}, etc.).

For the proposed control algorithm, the supply current is sensed and controlled. Assuming the load harmonics are completely compensated by the active filter, the supply currents in phase *a* is expressed as,

$$i_{s,a} = I_{sp,a} \sin \omega t + I_{sq,a} \cos \omega t \tag{2.14}$$

Where $I_{sp,a}$ is the amplitude of the in-phase component of the supply current and $I_{sq,a}$ is the amplitude of the quadrature component.

It indicates that the active filter injects harmonic current to supply the nonlinear load even though the load harmonic current is not sensed. The active filter injected current is derived as,

$$
\begin{aligned}
i_{af,a} &= i_{load,a} - i_{s,a} \\
&= (I_{Lp,a} - I_{sp,a})\sin\omega t + (I_{Lq,a} - I_{sq,a})\cos\omega t + \sum_{h=5,7,11} I_{Lh,a}\sin(h\omega t + \varphi_{h,a}) \qquad (2.15) \\
&= I_{afq,a}\cos\omega t + \sum_{h=5,7,11} I_{Lh,a}\sin(h\omega t + \varphi_{h,a})
\end{aligned}
$$

The active filter does not inject or absorb the active current component if the associated losses of the active filter are neglected. The active filter injects reactive current $I_{afq,a}$ to improve the power factor, and injects harmonic components $I_{Lh,a}$ (5^{th}, 7^{th}, 11^{th}, etc.) to compensate the load current harmonics. Currents in phase *b* and phase *c* can be presented in similar formats with a ±120 degree phase shift respectively.

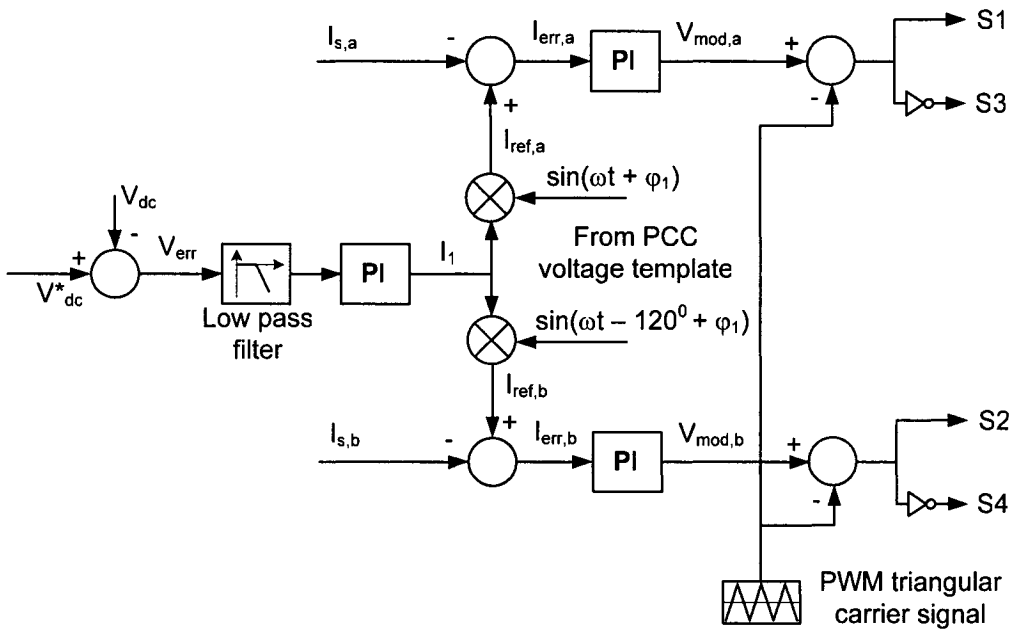


Fig. 2.9. Block diagram of the control system based on supply current sensing.

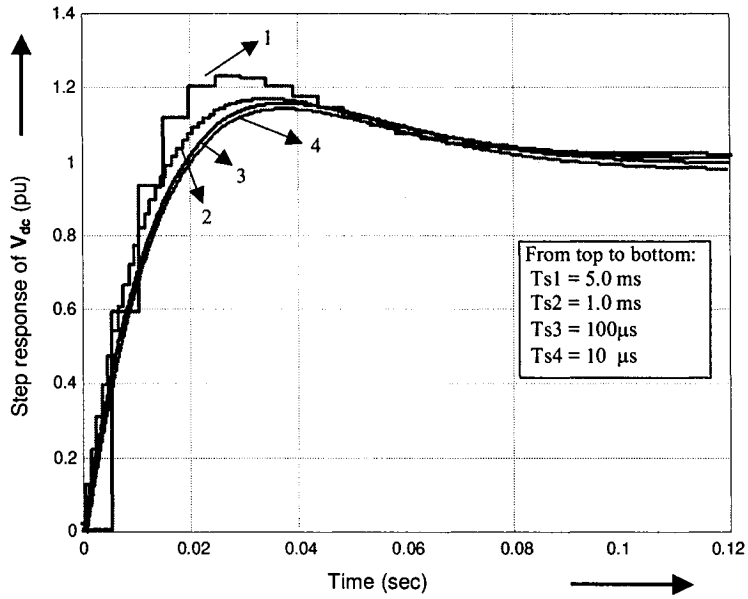


Fig. 2.10. Simulated results of the step response of the dc-bus voltage control loop with four different sampling time settings of the DSP controller.

The block diagram of the proposed control system based on supply current sensing scheme is shown in Fig. 2.9. The performance of the digital control system is affected by the sampling frequency of the DSP controller, since the controller delay introduces phase shift in the feed-back control loop, and changes the phase margin of the closed-loop control system. Fig. 2.10 investigates the step response of the dc-bus voltage control loop with four different DSP sampling time settings. The results illustrate that the overshoot of the dc-bus voltage deteriorates proportionally to the increase of the DSP sampling time.

2.4.3 Comparison of Load and Source Current Sensing Schemes

The load current sensing scheme compensates only the harmonic components of the load current, and imposes the least power rating requirement of the active filter. While the controller requires a fast data processing capability to extract the current harmonics instantaneously, and analog controllers are commonly used in the implementations to meet the fast signal processing requirement.

On the other hand, the source current sensing scheme doesn't have to extract the current harmonics, and compensates both the harmonics and the reactive power at the same time. As a result, the power rating requirement of the active filter is increased when the load displacement power factor decreases, while a relatively slower controller is applicable for the source current sensing scheme.

The vector representation of the associated power components is shown in Fig. 2.11, in which $S_{af,h}$ represents the power rating of the active filter compensating only the load harmonics, and $S_{af,h+q}$ represents the associated power rating for both load harmonics and reactive power compensation.

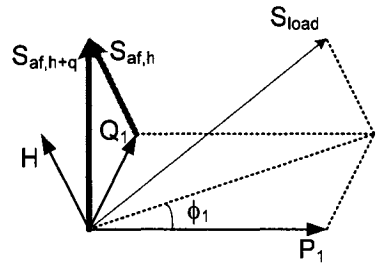


Fig. 2.11. Vector representation of the power components of the active filter.

If the three-phase supply voltage of ac mains is ideal, by applying the definition of the total harmonic distortion factor of load current as $THD_i = \sqrt{\sum_{h=3}^{\infty} I_h^2} \Big/ I_1$, the power rating requirement of the active filter is calculated in (2.16) as a function of the load power components.

$$\frac{S_{af,h+q}}{S_{load}} = \frac{\sqrt{Q_1^2 + H^2}}{\sqrt{P_1^2 + Q_1^2 + H^2}} = \frac{\sqrt{(\sin\varphi_1)^2 + THD_i^2}}{\sqrt{1 + THD_i^2}} \tag{2.16}$$

The normalized power rating requirement of the active filter (S_{load} = 1.0 pu) is shown in Fig. 2.12 in function of the total distortion factor of the nonlinear load. The advantages

and drawbacks of the two current sensing schemes, based on load current and source current sensing respectively, are derived in Table 2.2.

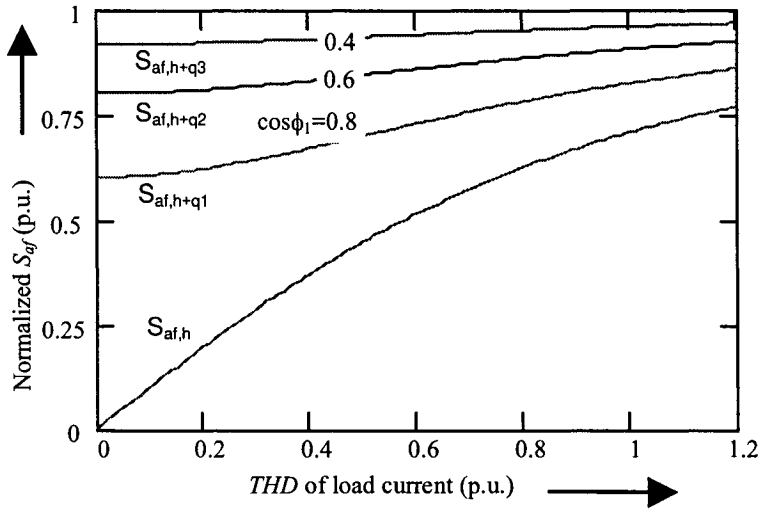


Fig. 2.12. Power rating requirement of the active filter in function of the load current THD_i.

Table 2.2. Comparison of Load and Supply Current Sensing Schemes

	Load Harmonic Current Sensing Scheme	**Supply Sinusoidal Current Sensing Scheme**
Controller selection	Analog Control	Digital Control
Number of current sensors	Four sensors for both the three-phase load current and active filter output current sensing.	Two sensors for three-phase supply current sensing.
Power rating	The active filter requires only a fraction of the load power rating	Generally need 0.5 to 1.0 pu of load power rating for both harmonics and reactive power compensation.
PCC voltage template dependence	Inaccurate voltage template increases the reactive power absorption slightly.	Inaccurate voltage template greatly increases the reactive power flow of the active filter. The system may lose its stability if the power rating of the active filter is not enough.

2.5 SIMULATION AND EXPERIMENTAL RESULTS

Laboratory prototypes of both the series voltage compensator and the shunt-connected active filter have been built based on the four-switch three-phase voltage source inverter. The proposed series and shunt compensators are designed at 2 kVA power rating. For series voltage compensation, the nominal phase voltage is selected at 40 V. Whereas for shunt harmonics compensation, the nominal phase voltage is chosen at 120 V, to test the compensator performance with different dc-bus voltage settings. The parameters of the series and shunt compensators are summarized in Table 2.3.

Table 2.3. Parameters of the Four-Switch Three-Phase Compensator

L_f	: Series compensator LC filter inductor	0.5 (mH)
C_f	: Series compensator LC filter capacitor	300 (μf)
r_f	: Series compensator LC filter damping resistor	0.8 (Ω)
γ_n	: Turns ratio of series coupling transformer	96/92
L_{af}	: Active filter ac-link inductor	1.5 (mH)
2C	: DC-bus split capacitor	900 (μf)
T_s	: DSP controller sampling time	50 (μs)
f_{sw}	: PWM switching frequency	5-10 (kHz)

The design principle for the parameters of the switching harmonic LC filter is extended from [39][134]. It is assumed that all of the switching harmonic currents pass through the filter inductor and capacitor. By setting a 10% total harmonic distortion factor for the output current THD_i and the LC filter capacitor voltage THD_v of the series converter, and selecting a break frequency of the LC filter about ten times lower than that of the PWM switching frequency, the values of the filter inductor and capacitor are determined. For the proposed system, the PWM switching frequency is 5 kHz, and the

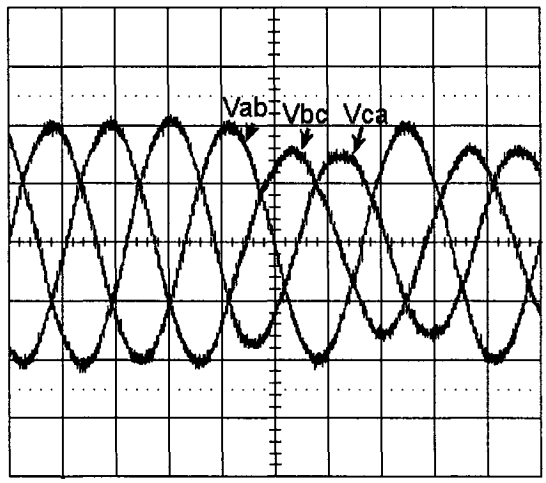
break frequency of the LC filter is chosen at 411 Hz. The parameters of the filter are L_f = 0.5 mH, C_f = 300 μf and the damping resistor r_f = 0.8 Ω.

The design of the dc-bus capacitor is based on the previous work [75][127]. The value of the dc-bus energy-storage capacitor is determined based on the permitted ripple range of the dc bus voltage. If the value of the capacitor is too small, then it is not capable of storing enough energy required for harmonics compensation, and the dc-bus voltage fluctuates. But a large dc-bus capacitance, along with a high voltage blocking rating, increases the cost of the compensator. The dc-bus capacitor is calculated by equalizing the instantaneous input power to the instantaneous output power of the static compensator, and selecting a 2% dc-bus voltage regulation ratio, the size of the dc-bus capacitor is obtained. With the proposed compensator, the size of the capacitor is load dependent, and the designed capacitance of 900 μf satisfies the voltage regulation ratio requirement on a 2 kVA power range.

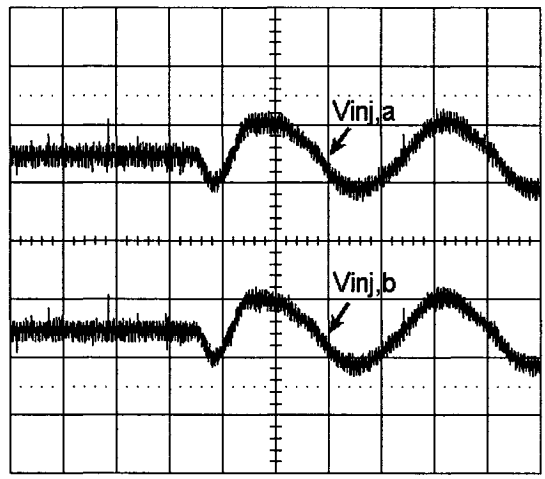
2.5.1 Performance of the Series Compensator with Feed Forward Control

A 2 kVA laboratory set-up was built to test the performance of the proposed series voltage compensator. The ac system passes through a wye-wye connected transformer and supplies a three-phase balanced resistive load. Fig. 2.13 illustrates the voltage compensation for a non-symmetrical supply voltage sag, and Fig. 2.14 gives results for a symmetrical supply voltage fault compensation. The results indicate that the series voltage compensator based on a four-switch converter is capable of maintaining the load voltage balanced and regulated. In addition, the high switching frequency harmonics are effectively reduced by the LC filter. The load voltage distortion factor THD_v is less than 3% with a PWM switching frequency of 5 kHz.

a) Three-phase line-to-line supply voltages with a 20% voltage sag in two phases. Volt: 50 v/div and time: 5 ms/div.



b) Injected voltages for phase *a* and phase *b*. Volt: 50 v/div and time: 5 ms/div.



c) Three-phase line-to-line load voltages after compensation. Volt: 50 v/div and time: 5 ms/div.

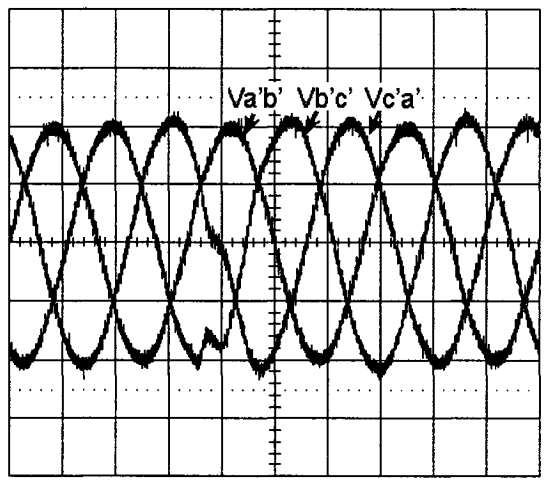
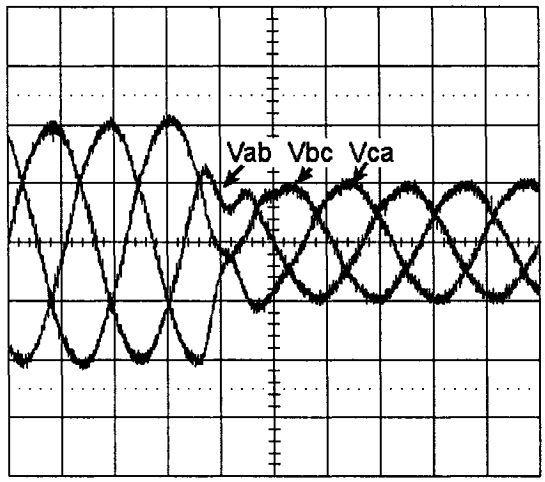


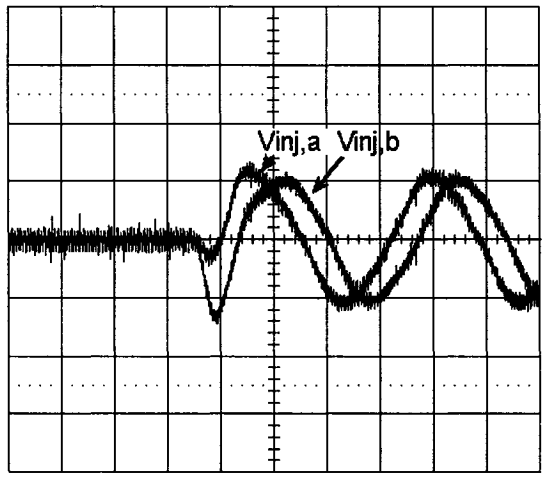
Fig. 2.13. Simulation performance of the four-switch series compensator for a non-symmetrical voltage fault compensation.

a) Line-to-line supply voltages with a 20% voltage sag in two phases. **b)** Compensator injected voltages for phase *a* and *b*. **c)** Load three-phase line-to-line voltages after compensation.

a) Three-phase line-to-line supply voltages with a 50% symmetrical voltage sag. Volt: 50 v/div and time: 5 ms/div



b) Injected voltages for phase *a* and phase *b*. Volt: 50 v/div and time: 5 ms/div.



c) Three-phase line-to-line load voltages after compensation. Volt: 50 v/div, time: 5 ms/div.

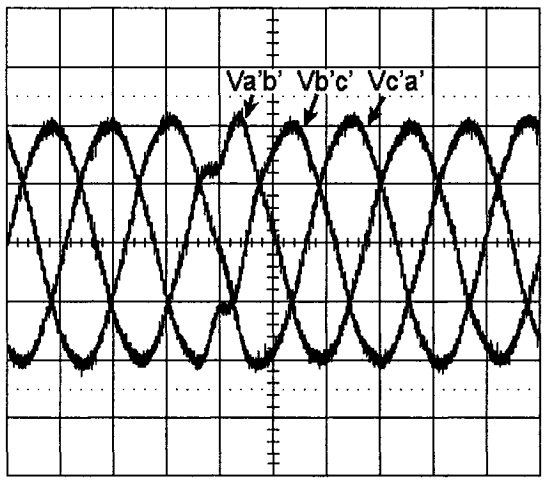


Fig. 2.14. Simulation performance of the four-switch series compensator for a 50% symmetrical three-phase voltage fault compensation.

a) Supply voltages with a 50% symmetrical voltage sag. **b)** Compensator injected voltages for phase *a* and *b*. **c)** Load three-phase line-to-line voltages after compensation.

2.5.2 Performance of the Active Filter Based on Load Current Sensing

The operation of the proposed four-switch active filter is verified on a 2 kVA experimental set-up, where it compensates harmonics generated by an adjustable-speed motor drive system having a diode rectifier at front-end. The switching frequency of the PWM converter is selected at 10 kHz to ensure that the active filter has fast dynamic response for load harmonics filtering.

The experimental set-up is evaluated in this section with the analog controller based on load current sensing. The supply voltage at the PCC is three-phase balanced and its peak phase voltage amplitude is 170 V. According to the power circuit of the four-switch active filter in Fig. 2.2, the condition for a successful current tracking of the active filter is mainly dependent on the di_L/dt of the load harmonic current, which can be expressed as following:

$$\left|\mathbf{V}_{4sw}(\mathbf{k})\right| \geq \left|\mathbf{V}_{pcc} + \mathbf{L}_{af}\frac{\mathbf{di}_L}{\mathbf{dt}}\right| \tag{2.17}$$

As Fig. 2.3 shows, the mean voltage vector $\mathbf{V}_{4m}$ is of an amplitude of $V_{dc}/2\sqrt{3}$. In the experimental setup, a minimum dc-bus voltage of 589 V is required for the active filter to synthesis a three-phase output voltage to follow the PCC bus voltage and without any load current tracking capability (di_L/dt = 0). A dc-bus voltage of 600 V allows the active filter to track the load current up to di_L/dt = 2.1 kA/sec. And a dc-bus voltage of 800 V gives the active filter a current tracking capability up to di_L/dt = 40.6 kA/sec.

The active filter has been tested with 800 V and 600 V dc bus voltages respectively, to compare the harmonic filtering performance under enough and insufficient dc-bus voltage conditions and to verify the boundary conditions for successful current tracking.

The performance of the active filter is presented in Fig. 2.15. The load current di_L/dt = 8 kA/sec and the THD_i of the load current is 37% before compensation. The supply current THD_i is 8.5 % after compensation with an 800 V dc bus voltage (current tracking capability di_L/dt = 40.6 kA/sec), and 15 % with a 600 V dc bus voltage (current tracking capability di_L/dt = 2.1 kA/sec).

a) Current waveforms with a dc-bus voltage V_{dc} = 800 V (current tracking capability di_L/dt = 40.6 kA/sec). Current: 10 A/div, time: 5 ms/div.

b) Current waveforms with a dc-bus voltage V_{dc} = 600 V (current tracking capability di_L/dt = 2.1 kA/sec). Current: 10 A/div, time: 5 ms/div.

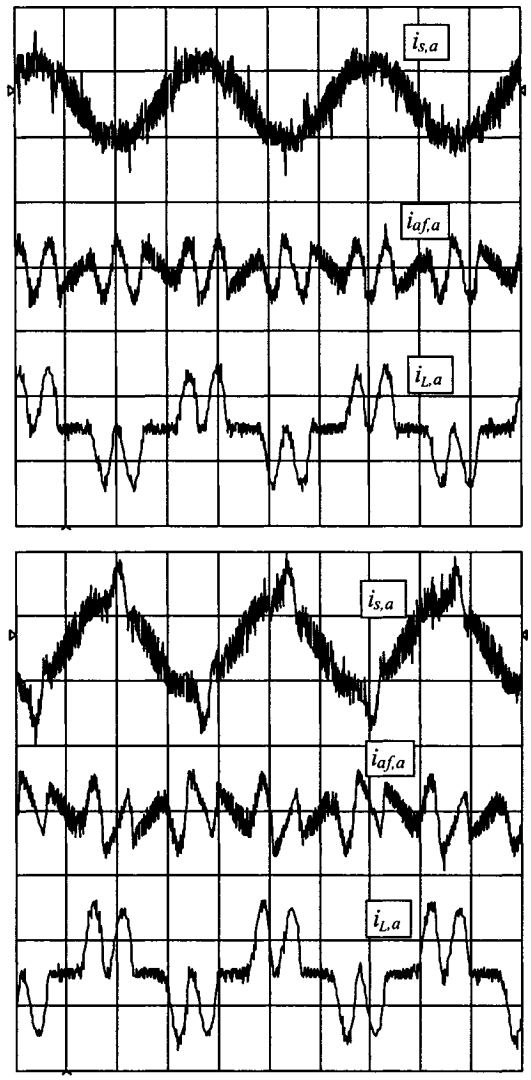


Fig. 2.15. Experimental performance of the four-switch active filter with load current sensing scheme.

The supply current, injected current and load current waveforms in phase *a*. **a)** With a dc bus voltage V_{dc} = 800 V (current tracking capability di_L/dt = 40.6 kA/sec). **b)** With a dc bus voltage V_{dc} = 600 V (current tracking capability di_L/dt = 2.1 kA/sec).

Fig. 2.16 compares the injected currents with 800 V and 600 V dc-bus voltages respectively. The results verify that the dc-bus voltage affects the current tracking capability of the active filter. Without enough dc bus voltage, the injected current cannot successfully track the load harmonics. As a result, the injected current with 600 V dc bus voltage, Fig. 2.16 **b)**, changes slower than that in Fig. 2.16 **a)** with 800 V dc-bus voltage.

a) Injected current with a dc-bus voltage V_{dc} = 800 V. Current: 10 A/div, time: 10 ms/div.

b) Injected current with a dc-bus voltage V_{dc} = 600 V. Current: 10 A/div, time: 10 ms/div.

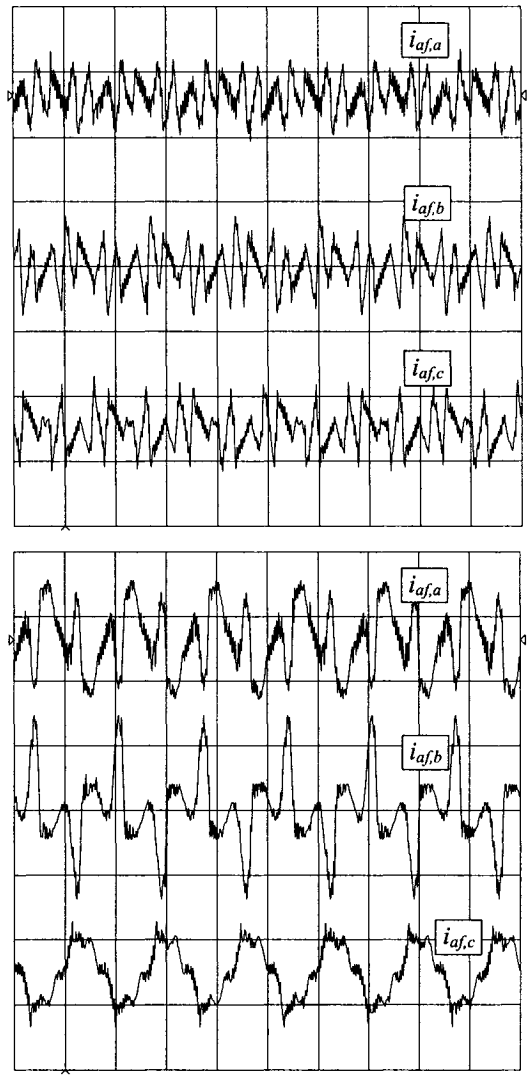
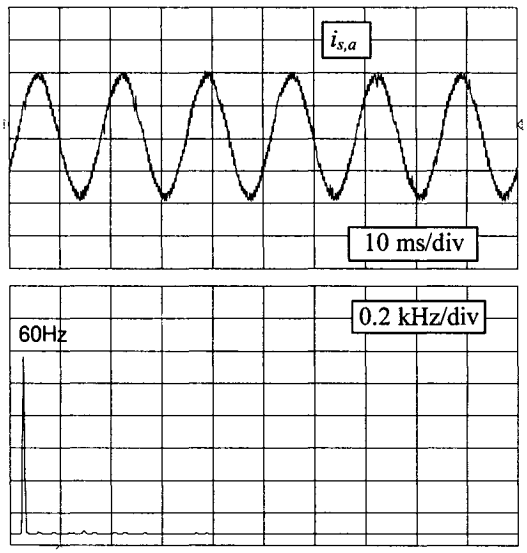


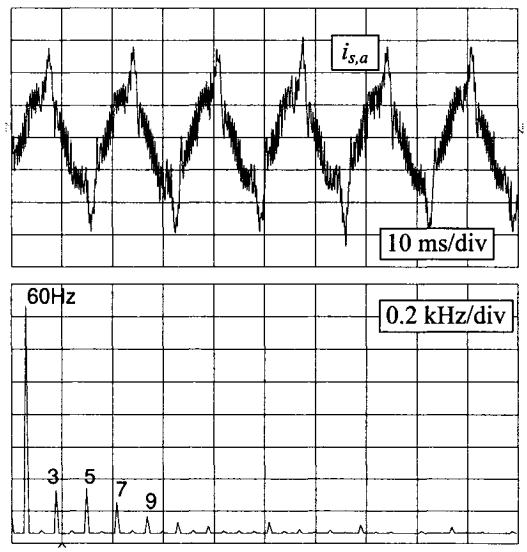
Fig. 2.16. Experimental results of the current tracking capabilities of the active filter with two dc bus voltage settings.

a) With V_{dc} = 800 V (current tracking capability di_L/dt = 40.6 kA/sec). **b)** With V_{dc} = 600 V (current tracking capability di_L/dt = 2.1 kA/sec).

Fig. 2.17 shows the current spectrum of the active filter. As expected, the active filter injects harmonic currents into ac mains to feed the nonlinear load. After compensation, the waveform of the supply current is sinusoidal with 800 V dc-bus voltage. If the dc-bus voltage drops to 600 V, the waveform of the supply current deteriorates, and includes noticeable harmonics.



a) Supply current with a dc-bus voltage V_{dc} = 800 V. Current: 5 A/div, time: 10 ms/div.



b) Supply current with a dc-bus voltage V_{dc} = 600 V. Current: 5 A/div, time: 10 ms/div.

c) Injected current with a dc-bus voltage V_{dc} = 800 V. Current: 5 A/div, time: 10 ms/div.

d) Load current with a dc-bus voltage V_{dc} = 800 V. Current: 5 A/div, time: 10 ms/div.

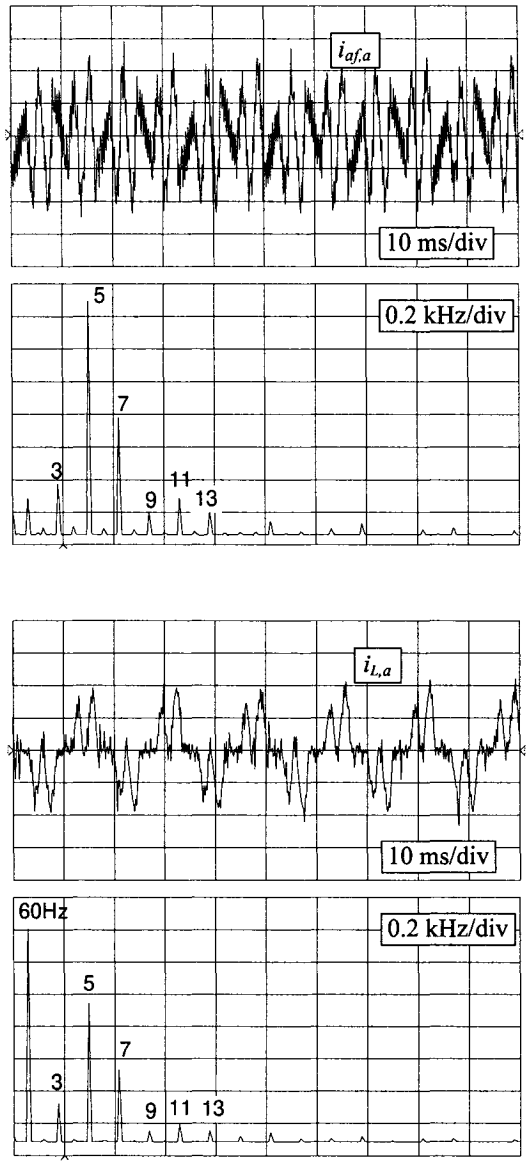


Fig. 2.17. Experimental results of the current spectra based on load current sensing scheme.

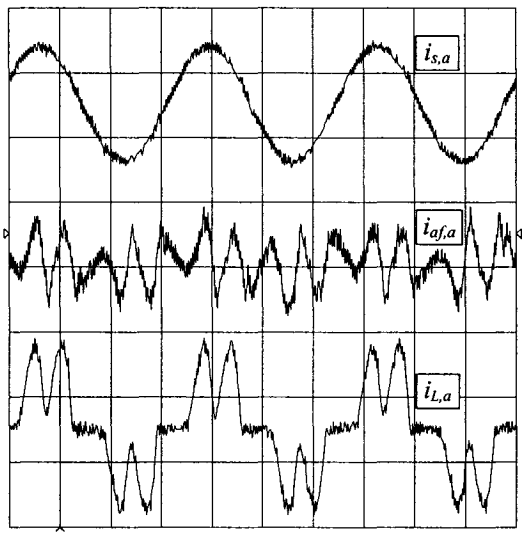
a) Spectrum of supply current i_{sa} with 800 V dc bus voltage. **b)** Spectrum of supply current i_{sa} with 600 V dc bus voltage. **c)** Harmonic spectrum of injected current $i_{af,a}$. **d)** Harmonic spectrum of load current $i_{L,a}$.

2.5.3 Performance of the Active Filter Based on Supply Current Sensing

The experimental prototype is then evaluated in this section with the digital controller based on supply current sensing control scheme. The sampling period of the DSP controller is selected as 50 μs.

The performance of the active filter is presented in Fig. 2.18. The load current di_L/dt = 8 kA/sec and the THD_i of the load current is 23% before compensation. The supply current THD_i is reduced to 4.5 % after compensation with an 800 V dc bus voltage (current tracking capability di_L/dt = 40.6 kA/sec), and 12 % with a 600 V dc bus voltage (current tracking capability di_L/dt = 2.1 kA/sec).

a) Current waveforms with a dc-bus voltage V_{dc} = 800 V (current tracking capability di_L/dt = 40.6 kA/sec). Current: 10 A/div, time: 5 ms/div.



b) Current waveforms with a dc-bus voltage V_{dc} = 600 V (current tracking capability di_L/dt = 2.1 kA/sec). Current: 10 A/div, time: 5 ms/div.

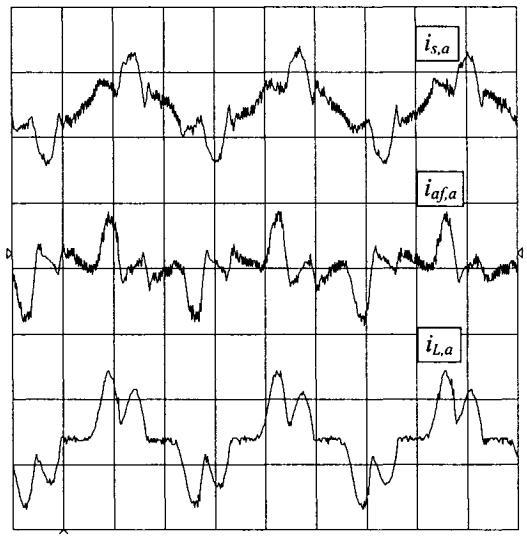


Fig. 2.18. Experimental performance of the four-switch active filter based on supply current sensing scheme.

The supply current, injected current and load current waveforms in phase *a*. **a)** With a dc bus voltage V_{dc} = 800 V (current tracking capability di_L/dt = 40.6 kA/sec). **b)** With a dc bus voltage V_{dc} = 600 V (current tracking capability di_L/dt = 2.1 kA/sec).

Fig. 2.19 demonstrates the transient performance of the active filter in the case of load fluctuation. The nonlinear load step-increases from 0.85 kVA to 1.8 kVA, and the response of the active filter is almost instantaneous. The injected current of the active filter successfully tracks the sudden change of the load current, and the supply current remains a slow changing sinusoidal current, therefore, the impact of load perturbation to the power system is reduced to minimum. The settling time of the dc bus voltage control loop is less than 30 ms, and the active filter shows an overshoot of 12% in dc bus voltage regulation.

Current waveforms with a load step-increase. The dc-bus voltage V_{dc} = 800 V (current tracking capability di_L/dt = 40.6 kA/sec). Current: 10 A/div, time: 5 ms/div.

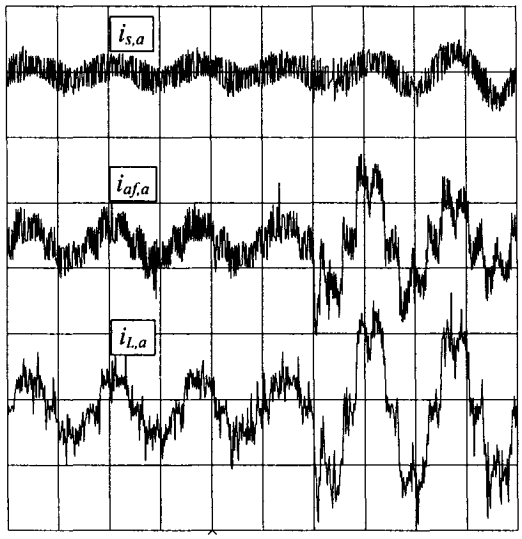


Fig. 2.19. Experimental results of the load perturbation response of the four-switch active filter based on supply current sensing scheme.

From the obtained waveforms, it is found that the experimental results in steady state coincide with the simulation results, in terms of voltage and current waveforms and the total harmonic distortion factors. When the control system is transient state, there are high-order harmonics presented in experimental waveforms, which are caused by the relatively slow sampling frequency of the DSP controller setting at 20 kHz. As discussed in Section 2.4.2, the appreciable processing time causes compensation delay, and produces line current spikes.

2.6 CONCLUSIONS

This chapter demonstrates the power conditioning capabilities of the static series and shunt compensators based on the four-switch voltage source converter, which indicates that the performance of the proposed compensator has not been degraded with the four-switch converter. The most significant drawback is the requirement of two times as high

as the dc-bus voltage, compared to its six-switch counterpart. In addition, due to the asymmetrical circuit structure of the four-switch converter, it is common to experience the unequal sharing of dc-bus voltage between the split capacitors.

For series voltage compensation, a modified power circuit configuration has been used and a control algorithm has been implemented to compensate three-phase line-to-line voltages based on two-phase voltage injection. For load harmonics compensation, both the load current sensing scheme and the supply current sensing scheme have been implemented. As an advantage of the supply current sensing scheme, the extraction of the high frequency load harmonic current is avoided, consequently, the detrimental effects caused by the sampling time delay of A/D conversion are alleviated. Therefore, the supply current sensing scheme is more suited for digital implementation than the commonly used load current sensing scheme. Simulation and experimental results confirm that the static compensator based on a four-switch voltage source converter structure is a viable alternative to the existing power quality solutions with a lower cost and without compromising of performance.

CHAPTER 3

STATE FEEDBACK CONTROL OF STATIC SERIES COMPENSATOR

3.1 INTRODUCTION

Voltage sags are the most prevalent type of power quality disturbances, and the static series compensator or so called dynamic voltage restorer (DVR) provides load voltage support with a power rating of only a fraction of that of the load [32][38]. A number of circuit configurations and control algorithms have been investigated, some implemented in industry, and most of them accomplish a compromise between steady state error and dynamic response.

Dynamic performance is a critical consideration. Many industrial loads such as electric drives and manufacturing processes are sensitive to interruptions as short as a few milliseconds. The constraint on response time leads to most reported DVR control strategies using open-loop feed forward control. While literature [47][49] shows that the open-loop control produces poorly damped response due to the presence of the switching harmonic LC filter. As shown in Fig. 3.1, the inductor at the output of the converter causes voltage drops proportional to the magnitude of the output current, and the interaction between the inductor and the capacitor introduces oscillation in transients. In addition, it is unclear how errors in the system (such as parameter variations, saturation of the series injection transformer, PWM blanking time effects and quantization effects) can affect the performance of the DVR with open-loop control schemes.

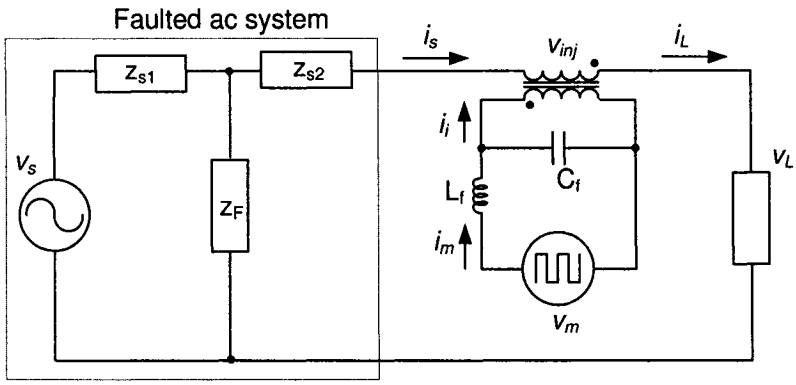


Fig. 3.1. Simplified equivalent circuit of the DVR.

Closed-loop control permits active damping of the LC filter, and a closer tracking of the reference load voltage. A number of control structures were tried. However, few papers on DVR closed-loop feedback control have been reported so far [50]. The multi-loop PI feedback control structure was comprehensively investigated in [51] in terms of stability margins, frequency response and damping performance. But multi-loop PI control has difficulties meeting the fast dynamic response requirement due to the dynamic separation of the two cascaded control loops for voltage and current regulation respectively. A recent work in [52] also proposed a selective harmonic closed-loop feedback control for voltage harmonics compensation. However, the selective harmonic controllers (such as 5th and 7th resonant controllers) are stacked into the existing fundamental-frequency voltage sag controller, and the selective harmonic controller itself is limited to voltage harmonics compensation. Since the selective harmonic controller assumes a constant control reference (null value), whereas the control reference of the fundamental-frequency voltage sag is usually time varying for three-phase unbalanced voltage fault compensation in synchronously rotating *d-q* coordinates. This makes the

DVR control system design different from that of the other power conversion applications [53].

This chapter is aimed at improving the dynamic response of the DVR. Steady-state compensation-capability curves are presented, and a closed-loop state variable feedback control strategy is proposed through modern treatment of classical control theory. The proposed control method provides a fast dynamic voltage sag compensation capability and is insensitive to the type of voltage faults and disturbances presented in the power network. The design of the proposed control system is based on the state-space model of the DVR system, but it removes the inner current control loop that is included in the multi-loop PI control structure. Instead, the inverter output current and its derivative are used to reflect the instantaneous load changes and to increase the dynamic response of the control system. Furthermore, a software based full-order current observer is developed to estimate the output current and its derivative, which can not be sensed directly by current transducers and is required in the proposed control algorithm. The theoretical considerations have been verified by simulation and experimental tests.

3.2 FAULTED DISTRIBUTION SYSTEMS

Power system studies show that over 90% of the power quality problems are associated with short-term voltage sags, dips and interruptions [14], which have the remaining magnitude in the range of 50% - 90% of nominal voltages and last for less than 2 seconds. In addition, by considering the short circuit impedance, which is the impedance between the point-of-common coupling (PCC) and the fault, a voltage fault also commonly associates with a phase-angle jump [59].

The vector diagrams of the common voltage faults are shown in Fig. 3.2 with Δ/Y, Δ/Δ, Y/Δ or Y/Y connected transformers, and assuming a zero phase-angle jump in the utility side for simplicity.

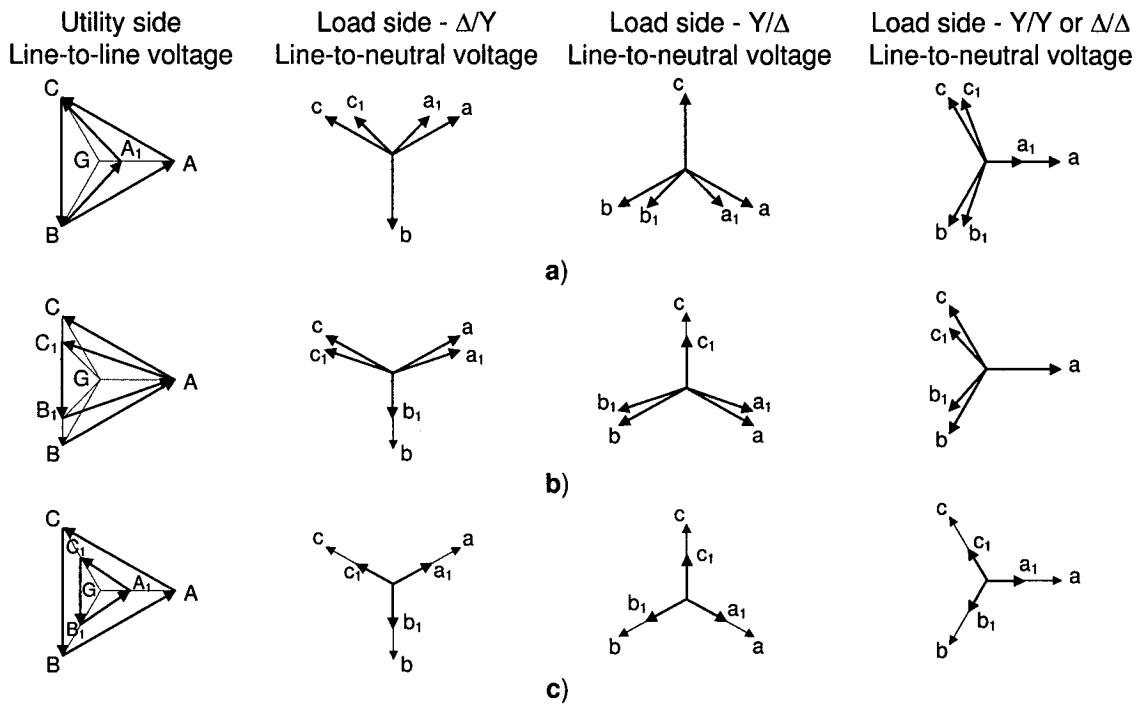


Fig. 3.2. Vector diagrams of supply voltage faults with Δ/Y, Δ/Δ, Y/Δ and Y/Y connected distribution transformers.

a) Single-phase voltage fault. **b)** Phase-to-phase voltage fault. **c)** Three-phase voltage fault.

Further studies conclude that, at the secondary side of the distribution transformers, all kinds of voltage sags can be classified into three categories, representing with a "*characteristic voltage*" $\vec{V}$ [64]. Type *1* is a non-symmetrical voltage fault with one phase voltage (*e.g.* phase *a*) unaffected and is expressed as,

$$\begin{aligned}\vec{V}_a &= 1 \\ \vec{V}_b &= -\frac{1}{2} - \frac{1}{2} j\vec{V}\sqrt{3} \\ \vec{V}_c &= -\frac{1}{2} + \frac{1}{2} j\vec{V}\sqrt{3}\end{aligned} \tag{3.1}$$

Type *II* is a non-symmetrical voltage fault experiencing voltage drops in three phases, which is written as,

$$\begin{aligned}\vec{V}_a &= \vec{V} \\ \vec{V}_b &= -\frac{1}{2}\vec{V} - \frac{1}{2} j\sqrt{3} \\ \vec{V}_c &= -\frac{1}{2}\vec{V} + \frac{1}{2} j\sqrt{3}\end{aligned} \tag{3.2}$$

Type *III* is a symmetrical voltage fault in three phases and is expressed as,

$$\begin{aligned}\vec{V}_a &= \vec{V} \\ \vec{V}_b &= -\frac{1}{2}\vec{V} - \frac{1}{2} j\vec{V}\sqrt{3} = \vec{V} \cdot \alpha^2 \\ \vec{V}_c &= -\frac{1}{2}\vec{V} + \frac{1}{2} j\vec{V}\sqrt{3} = \vec{V} \cdot \alpha\end{aligned} \tag{3.3}$$

The vector diagrams of the three fault types are shown in Fig. 3.3. The vectors named by *a, b, c* represent the voltages under normal operating conditions, the vectors named by a_1, b_1, c_1 represent those under faulted conditions that the *characteristic voltage* $\vec{V}$ drops to 0.5 pu and without any phase-angle jump, while the vectors named by a_2, b_2, c_2 represent those under faulted conditions that the *characteristic voltage* $\vec{V}$ drops to 0.5 pu and jumps -30^0 in phase-angle. It should be noted that most power distribution systems consist of inductive impedance, and indicate a negative phase angle jump associated with a voltage fault, *i.e.* the post-fault voltage lags the pre-fault voltage.

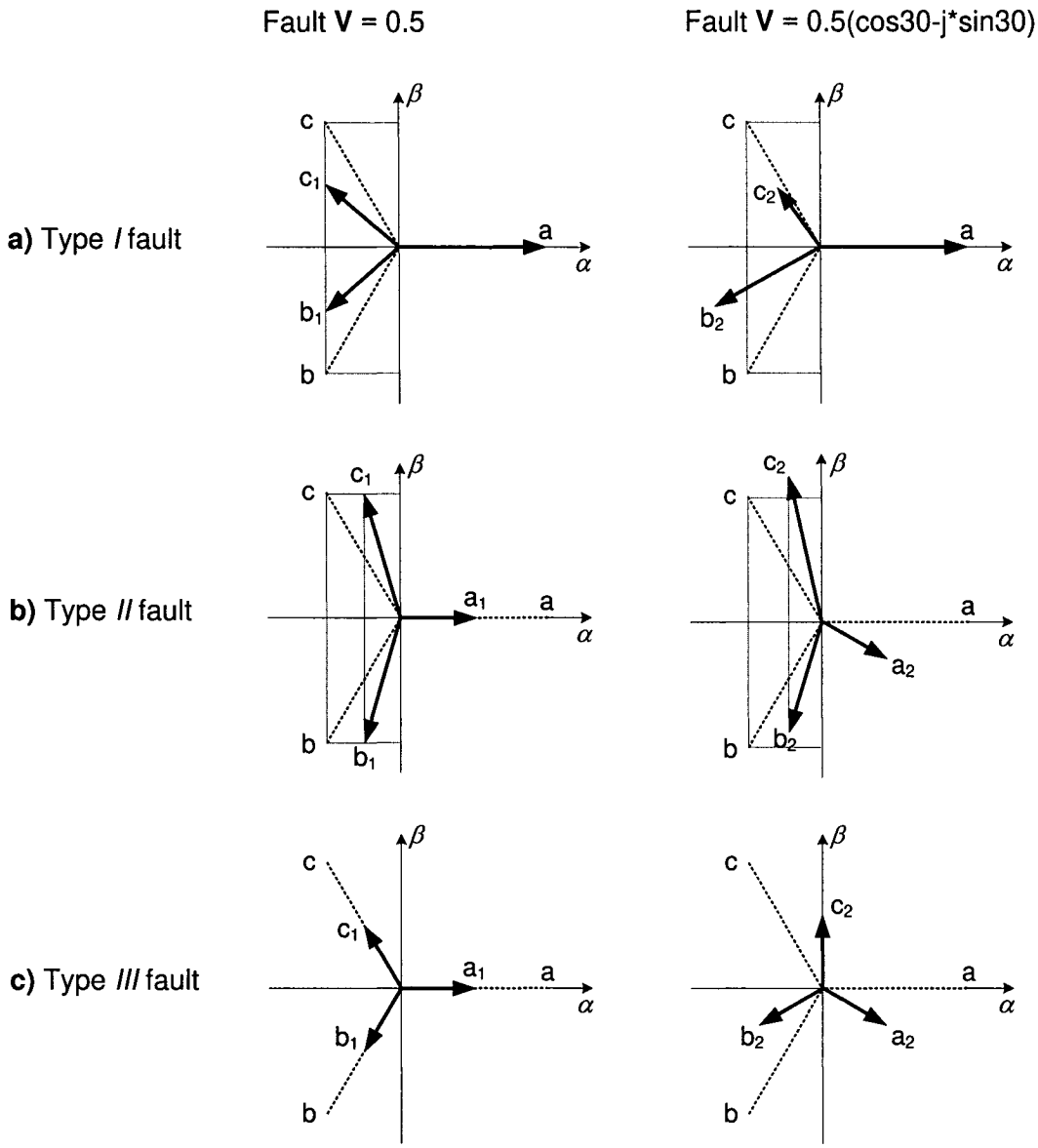


Fig. 3.3. Generalized three types of supply voltage faults in a typical three-phase distribution system.

In order to quantify the magnitude of a voltage sag and the unbalance among three phases, two factors are introduced known as the unbalance factor $\vec{\eta}$ and the magnitude factor $\vec{\rho}$.

According to the definition of the International Electro-technical Commission (IEC), the unbalance factor $\vec{\eta}$ is the ratio between the negative sequence of PCC bus line-to-line voltage $\vec{V}_n$ and the positive sequence of PCC bus line-to-line voltage $\vec{V}_p$.

$$\vec{\eta} = \frac{\vec{V}_n}{\vec{V}_p} = |\vec{\eta}| \angle \varphi_\eta \tag{3.4}$$

The unbalance factors under various fault conditions are shown in Fig. 3.4. It is shown that: (a) the non-symmetrical voltage faults, both type *I* and type *II*, result in the same unbalance factor curves as a function of the *characteristic voltage*; (b) the unbalance factor curve changes along with the change of the associated phase-angle jump of a non-symmetrical voltage fault; (c) the unbalance factor is zero for all three-phase symmetrical voltage faults (type *III*).

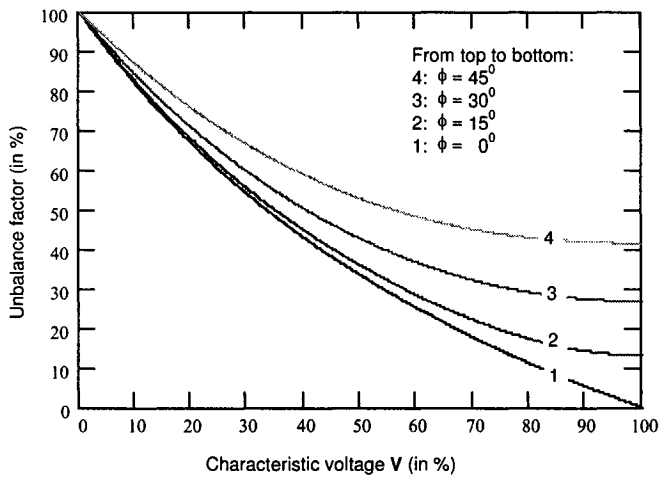


Fig. 3.4. Unbalance factor of the three-phase nonsymmetrical voltage faults.

The magnitude factor $\vec{\rho}$ is defined as the ratio of the positive sequence of PCC bus line-to-line voltage $\vec{V}_p$ to the nominal line-to-line voltage $\vec{V}_{ref}$.

$$\vec{\rho} = \frac{\vec{V}_p}{\vec{V}_{ref}} = |\vec{\rho}| \angle \varphi_\rho \tag{3.5}$$

The magnitude factors under various fault conditions are shown in Fig. 3.5. It is shown that: (a) the non-symmetrical voltage faults, both type *I* and type *II*, result in the same magnitude factor curves in function of the *characteristic voltage*; (b) the magnitude factor curve changes along with the change of phase-angle jump for non-symmetrical voltage faults; while (c) the magnitude factor curve for a symmetrical voltage fault (type *III*) doesn't change along with the change of phase-angle jumps.

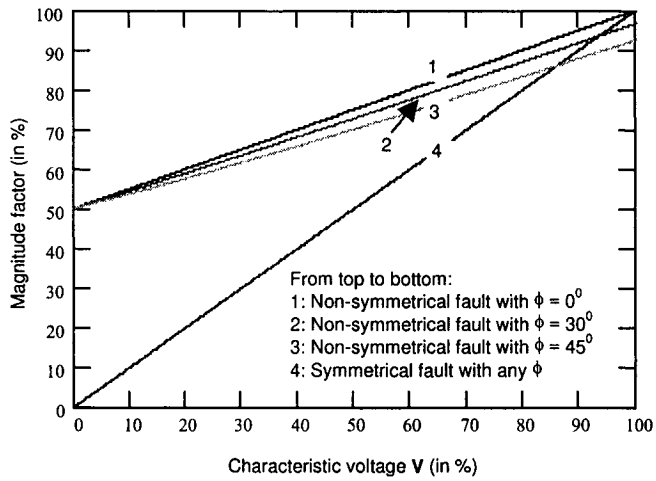


Fig. 3.5. Magnitude factor of the symmetrical and non-symmetrical voltage faults.

3.3 POWER CIRCUIT STRUCTURE OF THE STATIC SERIES COMPENSATOR

At the heart of a static series compensator is essentially a power converter that converts the dc-link voltage into an adjustable three-phase ac voltage. The power circuit configuration of a static series compensator can be implemented in a number of ways.

3.3.1 Configuration with a Three-Phase Voltage Source Converter

A three-phase converter connected to a three-phase series coupling transformer with either delta or wye connected windings on the converter side, and the line side windings are independently connected to the distribution system, as Fig. 3.6 shows. The power converter operates with three-phase unbalanced PWM switching functions. As discussed in Chapter 2, it is possible to replace the six-switch converter with a four-switch converter to reduce the number of IGBT power switches in three-phase three-wire ac systems. In that case, the corresponding power circuit is illustrated in Fig. 2.1.

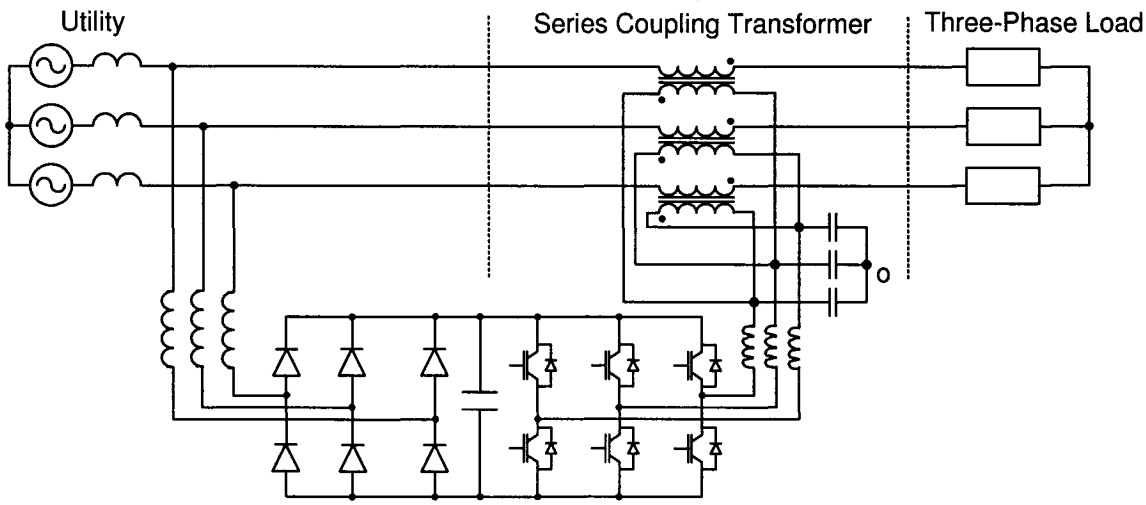


Fig. 3.6. Series compensator based on a three-phase voltage source converter.

3.3.2 Configuration with Three Single-Phase Full Bridge Converters

Three single-phase full bridge converters are coupled to the ac system by means of three independently connected transformers, and the three single-phase converters are connected to the same dc-bus, as shown in Fig. 3.7. Control of the system can be treated as three decoupled single-phase systems.

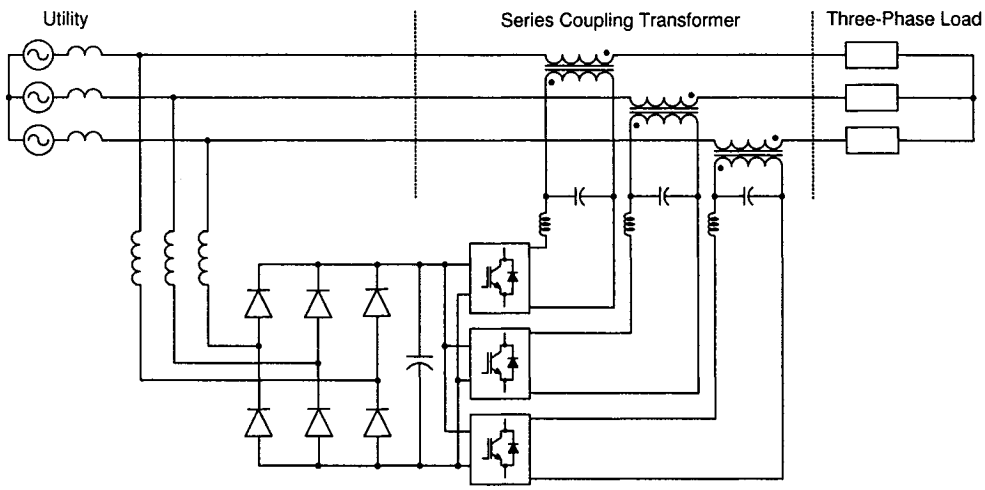


Fig. 3.7. Series compensator based on three single-phase full bridge converters.

3.3.3 Configuration with Three Single-Phase Half Bridge Converters

Three single-phase half bridge converters share a common dc-bus consisting of split capacitors. The windings of the transformers are wye connected on the converter side, and the line side windings are independently connected to the ac system as Fig. 3.8 shows. The midpoint of the split capacitors serves as a common point. It is connected to the 4^{th} wire of the windings and decouples the three converter legs. It should be noted that in three-phase three-wire power systems, the injected voltages add up to zero, which eliminates the necessity to decouple the three phases. Therefore, the midpoint connection of Fig. 3.8 can be removed and the power circuit configuration can be reduced to a conventional six-switch converter that is the same as in Fig. 3.6.

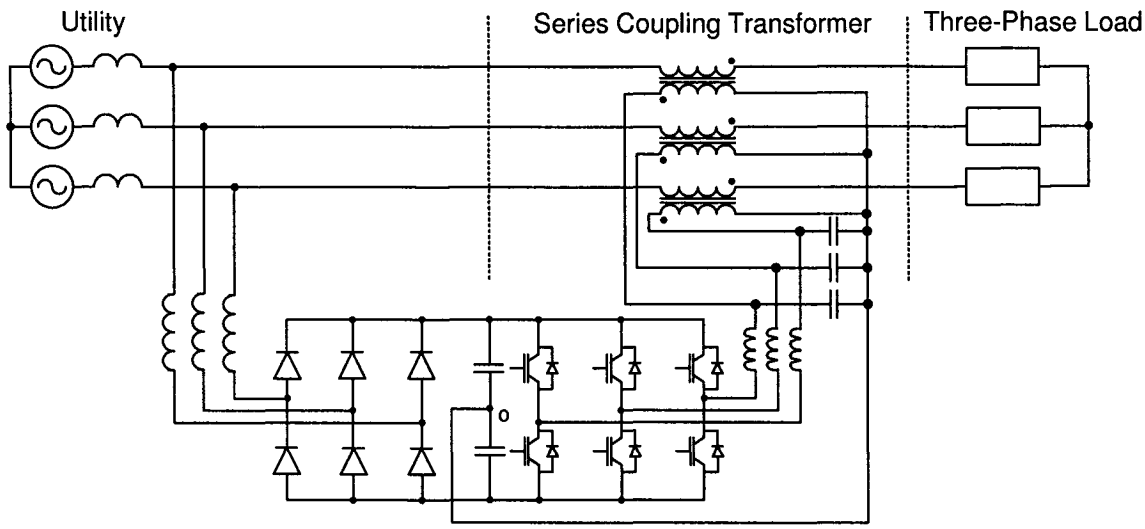


Fig. 3.8. Series compensator based on three single-phase half bridge converters.

In all three configurations, the output of the power converter is connected to a second order LC filter, thus to reduce the injection of high frequency harmonics caused by switching actions of the converter. The LC filter and the series coupling transformer carry the load current continuously when in operation. Compensation of the voltage drop in the LC filter and in the transformer can be implemented by introducing a correction voltage term with amplitude proportional to that of the load current.

The dc bus is powered by a diode bridge rectifier connected to the ac supply. Energy to the dc bus is provided on a continuous basis, but the amount of dc bus voltage is limited by the voltage available on the feeder, particularly under supply voltage fault conditions. Regulating the dc bus by means of a chopper can enhance the compensation capability. In addition, there have been suggestions to use the newer super capacitor technologies to increase energy storage in dc-bus, thus increasing the time duration in which the load voltage can be supported.

3.4 STEADY-STATE COMPENSATION CAPABILITIES

The static series compensator injects ac voltages with controllable magnitude and phase angle, and in series with the source and the load. The injected voltage can be considered essentially as a synchronous ac voltage source, and the line current flowing through this voltage source results in real and reactive power exchanging between the compensator and the ac system. The active power of the series compensator injected at the ac terminal is supplied by the dc-bus energy storage capacitors. The reactive power of the series compensator exchanged at the ac terminal is generated and absorbed internally by the power converter. The voltage injection capabilities of the series compensator are illustrated as follows based on phasor analysis.

3.4.1 Voltage Compensation with Only Reactive Power Injection

It is possible to regulate the load voltage using only reactive power injection, and the active power is then not required from the dc bus. The minimization of the use of active power leads to the reduction of the size and cost of the dc-bus power supply or the dc-bus energy-storage unit.

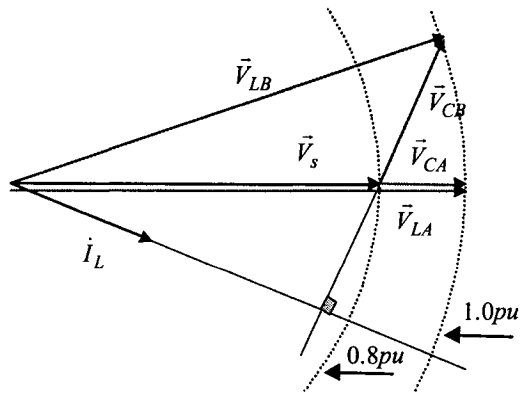


Fig. 3.9. Vector diagrams of the series compensator with minimum apparent power injection (V_{CA}) and with only reactive power injection (V_{CB}).

Fig. 3.9 shows that the reactive power injection scheme (V_{CB}) significantly increases the amount of the injected voltage and then severely restricts the range of voltage sags that can be compensated by the series compensator with a certain voltage injection capability [42]. The availability of real power removes the restrictions on the phase relation between the injected voltage and the line current. The following sections aim at control algorithms requiring minimum voltage injection and only the spare capacities of the series compensator are used for power factor improvement through reactive power injection.

3.4.2 Three Algorithms for Voltage Reference Generation

A critical issue in the selection of control algorithms for voltage fault compensation is to choose an optimal voltage reference generation scheme. The decision affects many aspects, such as the power rating requirement of the compensator, the calculation complexity, the reference availability, etc. Ideally the required voltage injection should be of minimum amplitude to reduce the voltage rating, therefore the power rating, of the compensator. The current rating is the line current in the ac system. Three reference selection schemes are studied as follows.

3.4.2.1 Reference synchronizing with the pre-fault voltage (scheme 1)

The three-phase supply voltage is sensed and a Phase Locked Loop is used to extract the phase angle of the supply voltage. During voltage sags, the Phase Locked Loop is switched into the freeze mode, and the voltage reference is synthesized using the nominal amplitude and the phase angle of the pre-fault voltage, as shown in Fig. 3.10.

The vectors named by a_1, b_1, c_1 represent the three-phase pre-fault voltage, the vectors named by a', b', c' represent the three-phase faulted supply voltage, and the vectors named by $V_{inj,a}$, $V_{inj,b}$, $V_{inj,c}$ represent the injected voltage for voltage fault compensation.

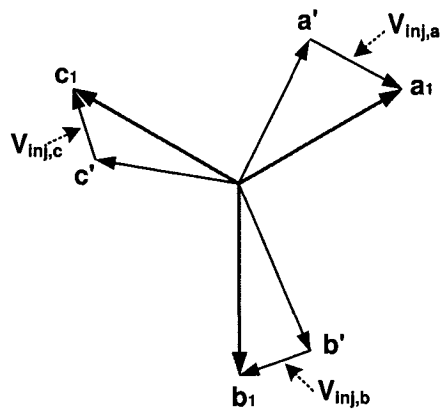


Fig. 3.10. Reference synchronizing with the pre-fault voltage (scheme 1).

3.4.2.2 Reference synchronizing with phase a of the post-fault voltage (scheme 2)

This scheme generates a synthetic voltage that is available under all voltage fault conditions. The magnitude of the voltage reference is set to the nominal amplitude, and the phase angle is synchronized to the phase a of the post-fault supply voltage. The algorithm is written as,

$$\vec{V}_{sync} = \frac{\vec{V}_{ab} - \vec{V}_{ca}}{3} = \vec{V}_a \tag{3.6}$$

The synthetic signal represents the voltage of phase a and is obtained from two of the line-to-line supply voltages. It is shown that for Y/Y, Y/Δ, Δ/Δ and Δ/Y connected transformers, $\mathbf{V}_{sync}$ never collapses to zero even if one phase is solidly grounded in the faulted ac systems. As Fig. 3.11 shows, the vectors named by a_1, b_1, c_1 represent the

three-phase pre-fault voltage, the vectors named by *a'*, *b'*, *c'* represent the three-phase faulted supply voltage, the vectors named by a_2, b_2, c_2 represent the three-phase voltage control reference, and the vectors named by $V_{inj,a}$, $V_{inj,b}$, $V_{inj,c}$ represent the injected voltage for voltage fault compensation.

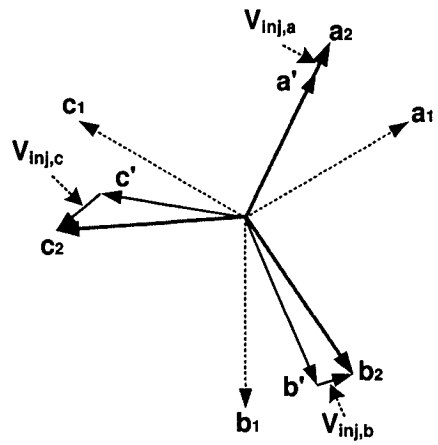


Fig. 3.11. Reference synchronizing with phase *a* of the post-fault voltage (scheme 2).

3.4.2.3 Reference synchronizing with the positive sequence of post-fault voltage (scheme 3)

The generation of the reference voltage synchronizing with the positive sequence of the post-fault voltage demands more computational efforts in order to extract the instantaneous sequence components. But this technique imposes the smallest voltage injection requirement. The advantage is much clearer when a large phase jump is associated with the voltage sag. As Fig. 3.12 shows, the vectors named by a_1, b_1, c_1 represent the three-phase pre-fault voltage, the vectors named by *a'*, *b'*, *c'* represent the three-phase faulted supply voltage, the vectors named by a_3, b_3, c_3 represent the three-

phase voltage control reference, and the vectors named by $V_{inj,a}$, $V_{inj,b}$, $V_{inj,c}$ represent the injected voltage for voltage fault compensation.

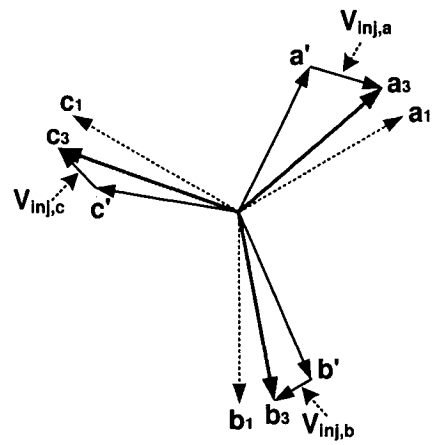


Fig. 3.12. Reference synchronizing with the positive sequence of post-fault voltage (scheme 3).

3.4.3 Voltage Injection Requirement of the Series Compensator

The series compensator is designed to insert the "missing" voltages into the ac system through the series coupling transformer. The injected voltage does not simply equal to the magnitude difference between the reference voltage and the supply voltage, but equal to the complex difference between them, in which the phase angle must be taken into account. The standard procedures for load voltage compensation include three steps, and are explained as follows.

3.4.3.1 Extraction of the sequence components

The three-phase supply voltage is decomposed into two balanced three-phase ac components, and a zero sequence component, by using the symmetrical components transformation:

$$\begin{bmatrix} \vec{V}_0 \\ \vec{V}_p \\ \vec{V}_n \end{bmatrix} = \mathbf{A} \cdot \begin{bmatrix} \vec{V}_{ab} \\ \vec{V}_{bc} \\ \vec{V}_{ca} \end{bmatrix} \tag{3.7}$$

where $\vec{V}_0$, $\vec{V}_p$ and $\vec{V}_n$ are the zero, positive and negative sequence voltage components respectively. If there is no neutral path in the ac system as in the three-phase three-wire ac system, the zero sequence component $\vec{V}_0$ is of null value. The transformation matrix **A** is defined as,

$$\mathbf{A} = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \quad \mathbf{A}^{-1} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \tag{3.8}$$

and $\alpha = e^{j(2\pi/3)}$.

3.4.3.2 Cancellation of the negative sequence component

The compensator injects a set of voltages to cancel out the negative sequence component of the supply voltage. Using the unbalance factor $\vec{\eta}$ and the magnitude factor $\vec{\rho}$ as defined in the previous section, the amount of the injected phase (line-to-neutral) voltages are given by,

$$[\vec{V}_{n,inj}]_{abc} = -\vec{\eta} * \vec{\rho} * \vec{V}_{ref} * \frac{[T_2]}{1-\alpha} \tag{3.9}$$

where $[T_2] = [1 \ \alpha \ \alpha^2]^T$.

3.4.3.3 Regulating the positive sequence component to the nominal amplitude

The compensator injects a set of voltages to regulate the magnitude of the positive sequence component of the supply voltage to 1.0 pu. The injected phase (line-to-neutral) voltages are given by,

$$[\vec{V}_{p,inj}]_{abc} = \frac{1-\vec{\rho}}{1-\alpha^2} * \vec{V}_{ref} * [T_1] \tag{3.10}$$

where $[T_1] = [1 \ \alpha^2 \ \alpha]^T$.

Based on the sum of (3.9) and (3.10), the total injected phase voltages are written as,

$$[\vec{V}_{inj}]_{abc} = \frac{\vec{V}_{ref} * [T_1]}{1-\alpha^2} - \vec{\rho} * \vec{V}_{ref} * (\frac{[T_1]}{1-\alpha^2} + \frac{\vec{\eta} * [T_2]}{1-\alpha}) \tag{3.11}$$

3.4.3.4 Comparison of injected voltages of the three reference generation schemes

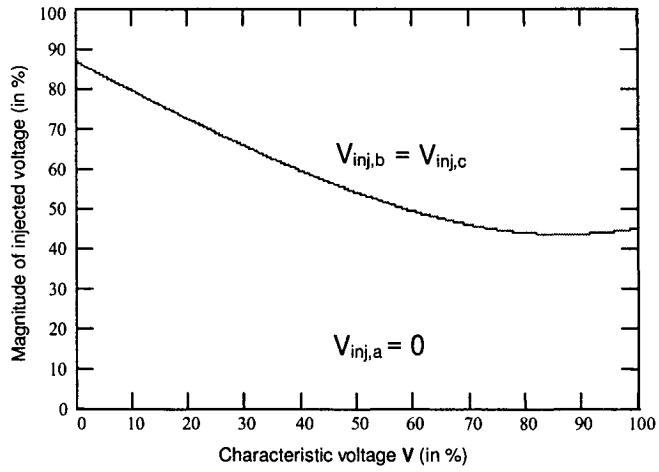
Selecting the magnitude of the pre-fault supply voltage to be 1.0 *pu* with zero initial phase angle, and considering with the three types of voltage faults in function of the *characteristic voltage* $\vec{V}$ as described in Section 3.2, the compensation quantities are summarized in Table 3.1 based on the three reference generation schemes, with the reference voltage synchronizing with the pre-fault voltage, the phase *a* of the post-fault voltage and the positive sequence of the post-fault voltage respectively. The table covers all types of voltage faults encountered in a typical three-phase three-wire distribution system. The compensator injected voltages under different fault conditions can be computed using the formulas provided in Table 3.1, and the resulting compensation capability-curves are plotted as follows.

Fig. 3.13 compares the injected voltages of the three control reference generation schemes for the type *I* fault with a phase angle jump of -30^0, in which schemes 1 and 2 result in the same compensation characteristics. Fig. 3.14 plots the injected voltages for type *II* fault compensation with the same phase angle jump of -30^0. Fig. 3.15 gives the injected voltages for type *III* fault compensation, in which the magnitudes of the injected voltages are the same in three phases and the associated phase angle jump has no influence on schemes 2 and 3. The results demonstrate that control scheme 3, synchronizing with the positive sequence of the post-fault voltage, leads to the smallest amount of voltage injection in most of the fault cases.

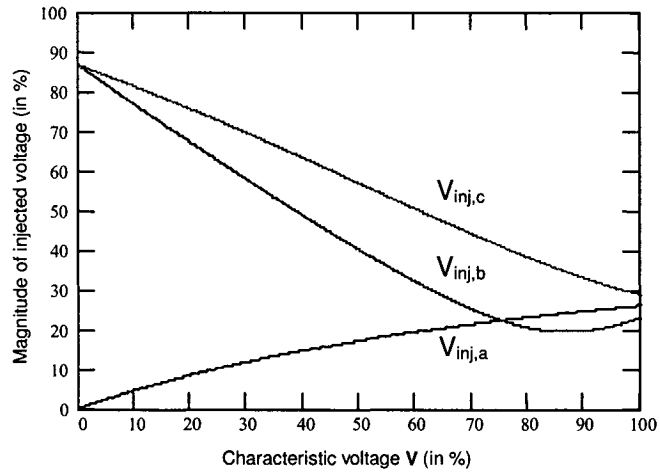
Table 3.1. Comparison of the Three Voltage Reference Generation Schemes.

Fault Type	Scheme 1 (Prefault voltage)			Scheme 2 (Postfault - phase *a*)			Scheme 3 (Postfault-positive sequence)		
	Volt Ref.	Unbal. Factor	Magn. Factor	Volt Ref.	Unbal. Factor	Magn. Factor	Volt Ref.	Unbal. Factor	Magn. Factor
Type *I*	1	$\frac{1-\vec{V}}{1+\vec{V}}$	$\frac{1}{2}+\frac{1}{2}\vec{V}$	1	$\frac{1-\vec{V}}{1+\vec{V}}$	$\frac{1}{2}+\frac{1}{2}\vec{V}$	$\frac{1+\vec{V}}{\lvert 1+\vec{V}\rvert}$	$\frac{1-\vec{V}}{1+\vec{V}}$	$\left\lvert\frac{1}{2}+\frac{1}{2}\vec{V}\right\rvert$
Type *II*	1	$\frac{\vec{V}-1}{1+\vec{V}}$	$\frac{1}{2}+\frac{1}{2}\vec{V}$	$\frac{\vec{V}}{\lvert\vec{V}\rvert}$	$\frac{\vec{V}-1}{1+\vec{V}}$	$\frac{1+\vec{V}}{2\vec{V}}\cdot\lvert\vec{V}\rvert$	$\frac{1+\vec{V}}{\lvert 1+\vec{V}\rvert}$	$\frac{\vec{V}-1}{1+\vec{V}}$	$\left\lvert\frac{1}{2}+\frac{1}{2}\vec{V}\right\rvert$
Type *III*	1	0	$\vec{V}$	$\frac{\vec{V}}{\lvert\vec{V}\rvert}$	0	$\lvert\vec{V}\rvert$	$\frac{\vec{V}}{\lvert\vec{V}\rvert}$	0	$\lvert\vec{V}\rvert$

a) Injected voltages with scheme 1 and scheme 2.



b) Injected voltages with scheme 3.



c) Maximum injected voltages of schemes 1 and 2 (dotted line), and scheme 3 (solid line).

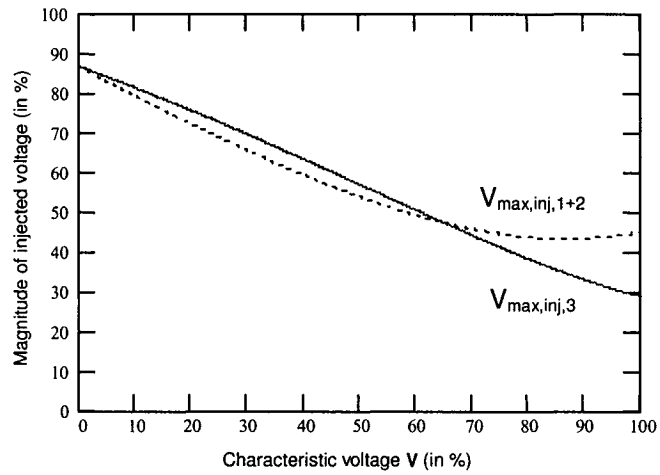
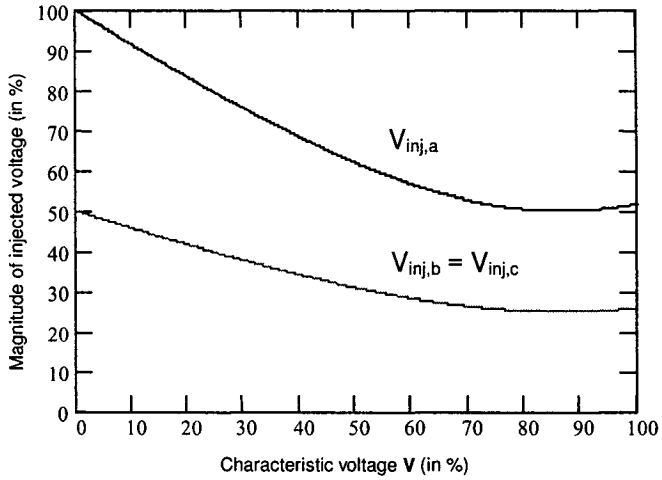
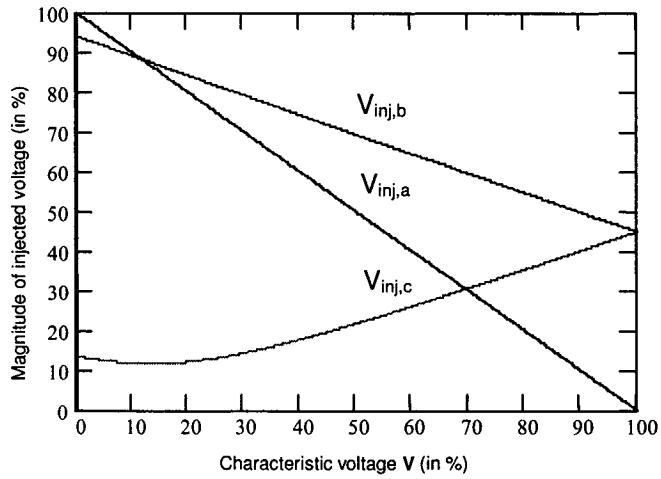


Fig. 3.13. Comparison of injected voltages with control schemes 1, 2 and 3, type *I* fault having a 30^0 of phase-angle jump.

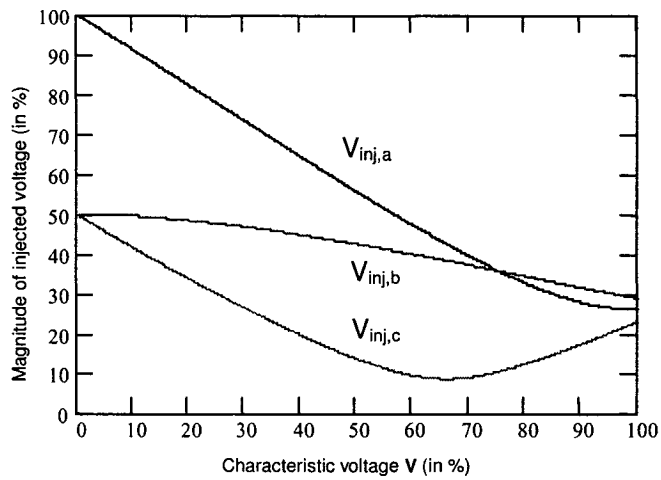
a) Injected voltages with scheme 1.



b) Injected voltages with scheme 2.



c) Injected voltages with scheme 3.



d) Maximum injected voltages of scheme 1, (dotted line), scheme 2, (dashed line) scheme 3 (solid line).

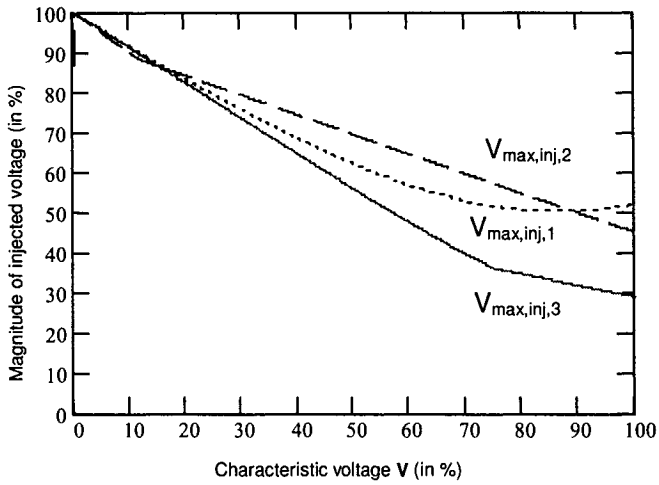


Fig. 3.14. Comparison of injected voltages with control schemes 1, 2 and 3, type *II* fault having a 30^0 of phase-angle jump.

Symmetrical three-phase injected voltages of scheme 1 (dotted line), scheme 2 and 3 (solid line).

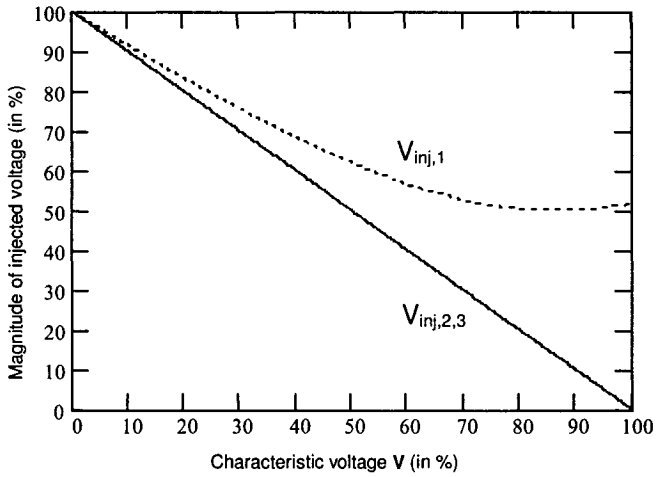


Fig. 3.15. Comparison of injected voltages with control schemes 1, 2 and 3, type *III* symmetrical three-phase voltage fault having a 30^0 of phase-angle jump.

3.5 DESCRIPTION OF THE PROPOSED POWER CIRCUIT

The proposed static series compensator is based on a three-phase voltage source converter, as shown in Fig. 3.16, having a similar power circuit structure as described in Fig. 3.6.

The output of the three-phase converter is connected to a three-phase series coupling transformer with wye connected windings on the converter side, and the line side windings are independently connected to the distribution system. The power converter operates with three-phase unbalanced PWM switching functions.

The PWM power converter consists of a second order LC filter on the ac side, to cancel out the high frequency harmonics caused by switching actions of the converter. The LC filter and the series coupling transformer carry the load current continuously when in operation. Compensation of the voltage drop caused by the LC filter and the series coupling transformer has been addressed by the proposed control algorithm.

In the following analysis, the three-phase power converter and the output LC filter are treated as one system. This allows the control system to provide active damping of the LC components and remove the loss-associated damping resistor from the LC filter. However, the number of state variables is increased in the resulting system model.

The dc bus is powered by a diode bridge rectifier connected to the ac supply. Energy to the dc bus is provided on a continuous basis, but the amount of dc bus voltage is limited by the voltage available from the feeder, particularly under fault conditions. Regulating the dc bus by means of a chopper can enhance the compensation capability.

The compensator inserts voltages in series with the ac system and the load. The space vector modulation method is used for the PWM switching converter, and the switching frequency of the converter is in the medium frequency range (5.2 kHz, or 87 pu).

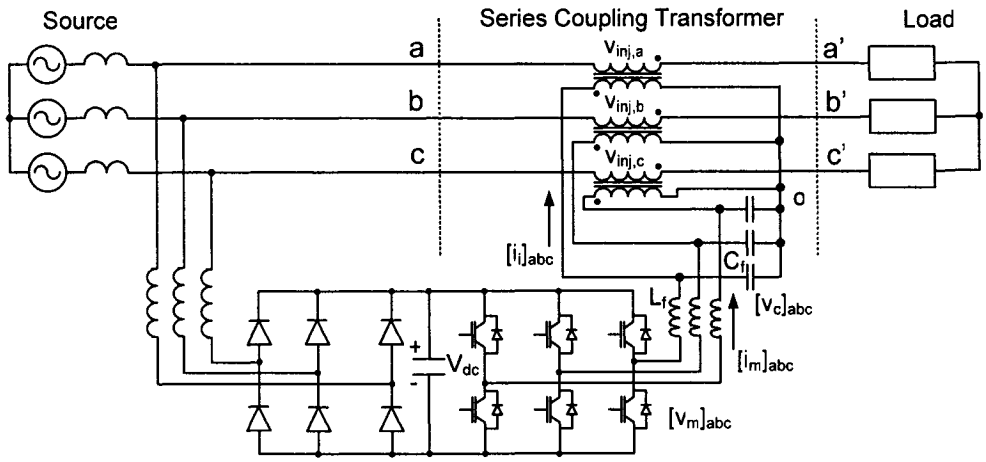


Fig. 3.16. Power circuit of the proposed series compensator.

Based on the PWM duty ratio and the cycle-by-cycle average model, the state-space model of the three-phase voltage source converter is derived and shown in Fig. 3.17.

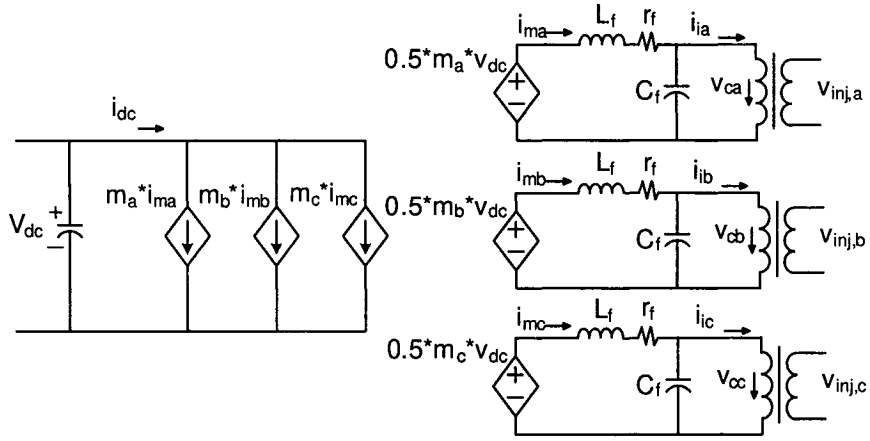


Fig. 3.17. Average model of the three-phase converter in stationary *abc* frame.

In order to derive the system equations, the involved state variables include the supply voltage $[V_s]_{abc}$, load voltage $[V_L]_{abc}$, series injected voltage $[V_{inj}]_{abc}$, LC filter capacitor voltage $[V_c]_{abc}$, inverter output voltage $[V_m]_{abc}$ and output current $[i_m]_{abc}$, series injected current $[i_i]_{abc}$ and dc-bus voltage V_{dc}. The series injected voltage $[V_{inj}]_{abc}$ is

related to the L-C filter capacitor voltage $[V_c]_{abc}$ based on the turns ratio γ_n of the voltage matching transformer.

The converter output voltage $[V_m]_{abc}$ is obtained in terms of the modulation index $[m]_{abc}$ and the dc-bus voltage V_{dc} as,

$$[V_m]_{abc} = [m]_{abc} \cdot V_{dc}/2 \tag{3.12}$$

By applying the Kirchhoff's current and voltage laws, the following system equations are obtained,

$$\begin{aligned} C_f \frac{d}{dt}[V_c]_{abc} &= [i_m]_{abc} - [i_i]_{abc} \\ L_f \frac{d}{dt}[i_m]_{abc} &= \frac{1}{2} \cdot [m]_{abc} \cdot V_{dc} - [V_c]_{abc} - r_f \cdot [i_m]_{abc} \end{aligned} \tag{3.13}$$

It is preferred to transform the system equations from stationary *a-b-c* coordinates into synchronously rotating *d-q* frame. The transformation allows the design of the controller to use dc dynamic models in balanced three-phase ac systems, and simplifies the analysis process. In three-phase three-wire systems as shown in Fig. 3.16, the zero sequence component of the state variable is of null value. Thus, the *dq* transformation of the system equations in (3.13) yields,

$$\begin{aligned} \frac{d}{dt}[V_c]_{dq} &= \omega\Phi[V_c]_{dq} + \frac{1}{C_f}[i_m]_{dq} - \frac{1}{C_f}[i_i]_{dq} \\ \frac{d}{dt}[i_m]_{dq} &= \omega\Phi[i_m]_{dq} - \frac{r_f}{L_f}[i_m]_{dq} + \frac{V_{dc}}{2L_f}[m]_{dq} - \frac{1}{L_f}[V_c]_{dq} \end{aligned} \tag{3.14}$$

where $\Phi = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$, and ω represents the angular frequency of the ac system.

3.6 THE PROPOSED CONTROL ALGORITHM

The proposed control strategy exploits modern treatment of classical control theory, based on the state space approach. It introduces a control variable to change the system behavior into the desired direction. The input variables are defined as the modulation indices $[m]_{dq}$. The output variables are defined as the capacitor voltages $[V_c]_{dq}$ of the LC filter that are associated with the injected voltages on the power line side of the series coupling transformer through the transformer turns ratio γ_n. The other state variables include the dc-bus voltage V_{dc}, converter output ac current $[i_m]_{dq}$ and the compensator injected current $[i_i]_{dq}$.

The resulting system is a multiple-input and multiple-output (MIMO) type of system. The inputs and outputs are *d-q* cross-coupled, and the output variables are implicitly expressed by the multiplication of input variables $[m]_{dq}$ and the state variable of V_{dc}. An input-output decoupling method has been reported in [65] for current-source rectifier applications, and the control principle is extended in this chapter to voltage-source converter systems after properly redefinition of the state variables. The LC filter damping resistor is removed from Fig. 3.17 ($r_f = 0$) to achieve active damping of the LC filter. The input-output simplification and decoupling process is performed in the following steps.

3.6.1 Expression of the Output Variables by Input Variables

In the system *dq* model (3.14), the output variables $[V_c]_{dq}$ are implicitly expressed by the input variables $[m]_{dq}$. The input-output decoupling method proposes to differentiate the output variables as many times as necessary, until one or more input variables appear explicitly. After differentiating (3.14) once, the following equation appears,

$$\frac{d^2}{dt^2}[V_c]_{dq} = -\left(\omega^2 + \omega_f^2\right)[V_c]_{dq} + \frac{2\omega}{C_f}\Phi[i_m]_{dq} - \frac{\omega}{C_f}\Phi[i_i]_{dq} + \frac{\omega_f^2 V_{dc}}{2}[m]_{dq} - \frac{1}{C_f}\frac{d}{dt}[i_i]_{dq} \quad (3.15)$$

where $\omega_f = 1/\sqrt{L_f C_f}$, the cut-off frequency of the second order L-C filter.

In the resulting equation (3.15), the output variables $[V_c]_{dq}$ are expressed directly by the input variables $[m]_{dq}$, therefore, the differentiation operation stops here. The resulting equation (3.15) can be written in the following standard state-space matrix format,

$$\mathbf{V}(t) = \mathbf{A}(t) \cdot [m]_{dq} + \mathbf{B}(t) \quad (3.16)$$

where $\mathbf{V}(t) = \frac{d^2}{dt^2}[V_c]_{dq}$, $\mathbf{A}(t) = \omega_f^2 V_{dc}/2$ and

$$\mathbf{B}(t) = -\left(\omega^2 + \omega_f^2\right)[V_c]_{dq} + \frac{2\omega}{C_f}\Phi[i_m]_{dq} - \frac{\omega}{C_f}\Phi[i_i]_{dq} - \frac{1}{C_f}\frac{d}{dt}[i_i]_{dq}.$$

3.6.2 Simplified Expression of the Outputs by a New Set of State Variables

The second step is to define a new set of state variables $[u]_{dq} = [u_d \; u_q]^T$, and to suppose that a linear and decoupled relationship exists between the output variables $[V_c]_{dq}$ and the new set of state variables $[u]_{dq}$, which is written as,

$$k_3 \cdot [u]_{dq} = \frac{d^2}{dt^2}[V_c]_{dq} + k_1 \cdot \frac{d}{dt}[V_c]_{dq} + k_2 \cdot [V_c]_{dq} \quad (3.17)$$

3.6.3 Transformation between the Inputs and the New Set of State Variables

The input-output decoupling and simplification can be achieved if a transformation matrix exists between the input variables $[m]_{dq}$ and the new set of state variables $[u]_{dq}$. Therefore, the output variables can be expressed by the decoupled input variables multiplying with the transformation matrix.

Combining equations (3.15) and (3.17), the input transformation is derived as,

$$[m]_{dq} = \mathbf{A}^{-1}(t) \cdot \left\{ k_3 \cdot [u]_{dq} + \mathbf{D}(t) \right\} \tag{3.18}$$

where $\mathbf{A}^{-1}(t) = 2/\omega_f^2 V_{dc}$ and

$$\mathbf{D}(t) = -k_1 \frac{d}{dt}[V_c]_{dq} + \left(\omega^2 + \omega_f^2 - k_2\right)[V_c]_{dq} - \frac{2\omega}{C_f}\Phi[i_m]_{dq} + \frac{\omega}{C_f}\Phi[i_i]_{dq} + \frac{1}{C_f}\frac{d}{dt}[i_i]_{dq}.$$

It can be seen that the input transformation is always available, except for one working point where the dc-bus voltage V_{dc} drops to zero. In practical applications, the dc-bus voltage is regulated to maintain a near constant value by using an ac/dc rectifier and an energy storage capacitor. Therefore, the proposed algorithm is always applicable during normal compensation operations. In addition, the input transformation (3.18) can be further simplified as,

$$[m]_{dq} = d_0 \left(\begin{array}{c} d_1[u]_{dq} + \begin{bmatrix} d_2 & -d_3 \\ d_3 & d_2 \end{bmatrix}[V_c]_{dq} + \begin{bmatrix} -d_4 & -d_5 \\ d_5 & -d_4 \end{bmatrix}[i_m]_{dq} \\ + \begin{bmatrix} d_4 & d_5/2 \\ -d_5/2 & d_4 \end{bmatrix}[i_i]_{dq} + d_6 \frac{d}{dt}[i_i]_{dq} \end{array} \right) \tag{3.19}$$

The parameters are defined as,

$$d_0 = 2/\omega_f^2 \cdot V_{dc}, \quad d_1 = k_3, \quad d_2 = \omega^2 + \omega_f^2 - k_2, \quad d_3 = k_1\omega, \quad d_4 = k_1/C_f, \quad d_5 = 2\omega/C_f$$

and $d_6 = 1/C_f$.

3.6.4 Dynamic Response of the Proposed Control System

By using Laplace Transform, the relation between the output variables $[V_c]_{dq}$ and the new set of state variables $[u]_{dq}$ cab be considered as a second-order low-pass system. Based on equation (3.17), the transfer function is expressed as,

$$\frac{V_{cd}(s)}{U_d(s)} = \frac{V_{cq}(s)}{U_q(s)} = \frac{k_3}{s^2 + k_1 s + k_2} \tag{3.20}$$

According to the prior analysis, the block diagram of the proposed state feedback control system is shown in Fig. 3.18.

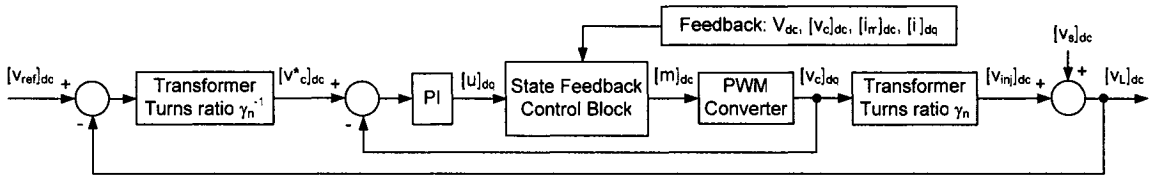


Fig. 3.18. Block diagram of the proposed control system.

In the proposed control system, the controller regulates the PWM modulation indices of the power converter, thus to maintain the load voltage with the nominal amplitude and tracking the positive sequence component of the supply voltage in phase angle. The inserted PI regulator is used to minimize the state steady error of the load voltage to be zero, even in the case of parameter mismatch during the system modeling. The PI regulator uses the form of $1/\tau_{dq}s$ to reflect a slow correction of compensation error, which is caused by parameter mismatch. The control system can be further simplified to Fig. 3.19 based on the compensator simplified equivalent circuit. The transfer function of the closed-loop control system is written as,

$$\frac{V_{cd}(s)}{V_{cd}^*(s)} = \frac{V_{cq}(s)}{V_{cq}^*(s)} = \frac{k_3/\tau_{dq}}{s^3 + k_1 s^2 + k_2 s + k_3/\tau_{dq}} \tag{3.21}$$

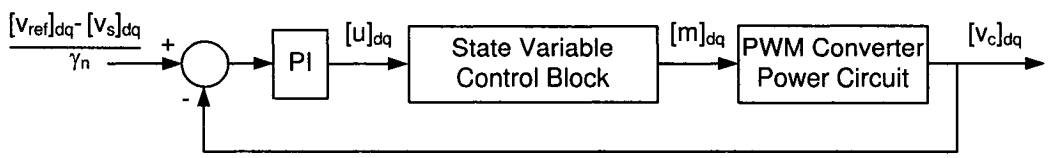


Fig. 3.19. Simplified block diagram of the proposed control system.

For the determination of the control parameters, the speed of response is an important criterion in the design of the system. The performance index of the proposed system takes the Integral of Time-Multiplied Absolute Error (ITAE) criterion, which is expressed as $\int_0^\infty t \cdot \left| \left[V_c^*\right]_{dq} - \left[V_c\right]_{dq} \right| \cdot dt$, and the parameters in equation (3.21) are chosen to minimize the integral. A number of parameter optimization methods have been presented in modern control theory, and an optimum third order transfer function based on ITAE criterion was proposed and successfully applied for the current source converter application [65]. The same optimum third order transfer function is used in the proposed control system design based on voltage source converter, which is written as:

$$\frac{(7.5418/T_{sett})^3}{s^3 + 1.75(7.5418/T_{sett})s^2 + 2.15(7.5418/T_{sett})^2 s + (7.5418/T_{sett})^3} \tag{3.22}$$

where T_{sett} is the designed settling time of the control system that is the time required for the eventual settling down of the load voltage to be within 2% of its value in steady state.

Therefore, the coefficients of the proposed controller are given by:

$$k_1 = 1.75\frac{7.5418}{T_{sett}}, \quad k_2 = k_3 = 2.15\left(\frac{7.5418}{T_{sett}}\right)^2, \quad \tau_{dq} = 2.15\frac{T_{sett}}{7.5418}.$$

In terms of implementation, the power rating of the series compensator is designed based on Table 3.1, thus it is capable of providing the required injected voltages under various fault conditions. In addition, the dc-bus voltage of the PWM converter is regulated to prevent the PWM synthesis from over-modulation and the consequent switching harmonics. Within the operating region, the proposed state variable feedback control system illustrates an improved steady state and dynamic performance over the open-loop control and the multi-loop PI feedback control schemes.

3.6.5 Dynamic Response of the Existing Control Schemes

As an extension of the analysis reported in [51], it is found that the open-loop control of static series compensators results in poor system damping following a voltage sag due to the presence of the LC filter. In the open-loop control system, the voltage on the power source side of the DVR is compared to the load voltage reference and the voltage difference is injected by the PWM converter. With the presence of the switching harmonic LC filter connected at the output of the PWM converter, the transient response of the DVR behaves like a second-order system following a voltage sag, and the capacitor voltage of the LC filter, which is injected into the power line through the series coupling transformer, can be written as,

$$V_{c,k}(t) = \left(1.0 - \frac{1}{s_2 - s_1}\left(s_2 e^{s_1 t} - s_1 e^{s_2 t}\right)\right) \cdot V_{r,k}(t) \tag{3.23}$$

Where k represents phase a, b or c, and $V_{r,k}(t)$ is the required injecting voltage calculated by the DVR controller. For the second-order system consisting of the LC filter, the natural frequency ω_f and the damping constant ξ_0 are given by

$$\omega_f = \frac{1}{\sqrt{L_f C_f}}, \qquad \xi_0 = \frac{r_f}{2L_f} \tag{3.24}$$

The eigenvalues of the characteristic equation are obtained as,

$$s_{1,2} = -\xi_0 \pm \sqrt{\xi_0^2 - \omega_f^2} \tag{3.25}$$

If the LC filter damping resistor r_f is zero, the eigenvalues s_1 and s_2 are a pure imaginary conjugate pair, the capacitor voltage oscillates without any damping. In practical implementations, a small damping resistor r_f is used, and the eigenvalues s_1 and s_2 are a complex conjugate pair with the magnitude of the imaginary part greater than that

of the real part. This results in an under-damped second-order system. It should be noted that a large damping resistor deteriorates the harmonics filtering performance of the LC filter and causes heating losses as well, which is not used in power converter applications. The analysis reveals that the damping performance of the series compensator is usually unsatisfactory with the open-loop control, and the damping performance is very much dependent on the damping resistance of the LC filter.

On the other hand, the closed-loop feed-back PI control is capable of providing active damping of the LC filter, in which the damping resistor is removed. As Fig. 3.20 shows, due to the cross-coupling of the *d-q* components of the voltage and current, most of the PI control schemes are based on the multi-loop control structure [51], including an inner current control loop and an outer voltage control loop. The performance of outer voltage control loop is limited to a slow dynamic response.

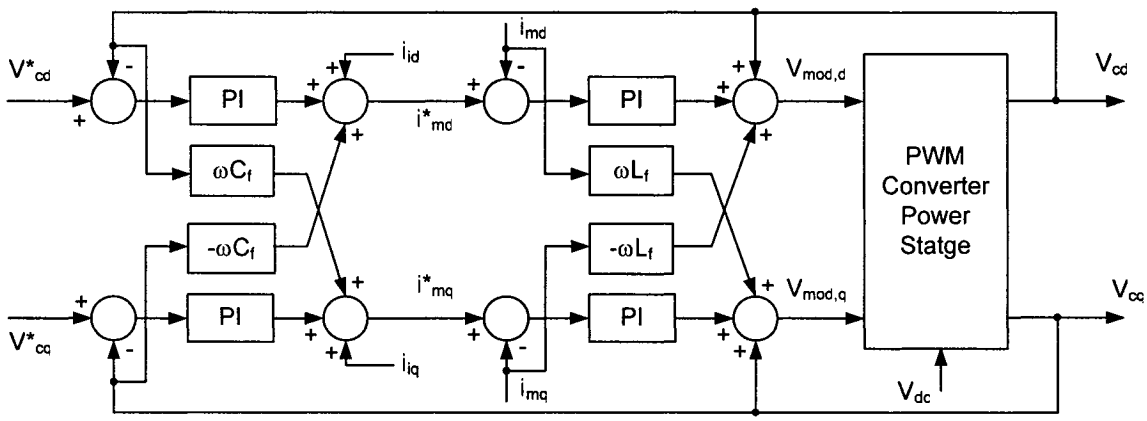


Fig. 3.20. Block diagram of the multi-loop PI control system.

According to the dynamic separation requirement of the cascaded two loops, the dynamic performance of the outer voltage control loop is much slower than that of the inner current control loop.

As an improvement, the proposed state feedback control algorithm removes the inner current control loop. Instead, the compensator injected current $[i_i]_{dq}$ and its derivative $d[i_i]_{dq}/dt$ are used to reflect the instantaneous load changes and to increase the dynamic response of the control system. Therefore, the proposed state variable feedback control algorithm is capable of providing faster dynamic response than that of the multi-loop PI control method.

3.7 FULL-ORDER CURRENT OBSERVER

The injected current $[i_i]_{dq}$ of and its derivative $d[i_i]_{dq}/dt$ are used in the proposed control scheme to reflect the instantaneous load changes. In practice, the current derivative cannot be sensed directly, and the differentiation computation usually introduces noise. A software based full-order current observer is constructed in this section, which estimates the injected current and its derivative at the same time.

The operational principle of the full-order current observer [66] is to guess the injected current $[i_i]_{dq}$ based on other known quantities such as $[i_m]_{dq}$ and $[V_c]_{dq}$, and to reduce the approximation error continuously by using feedback loops, as shown in Fig. 3.21.

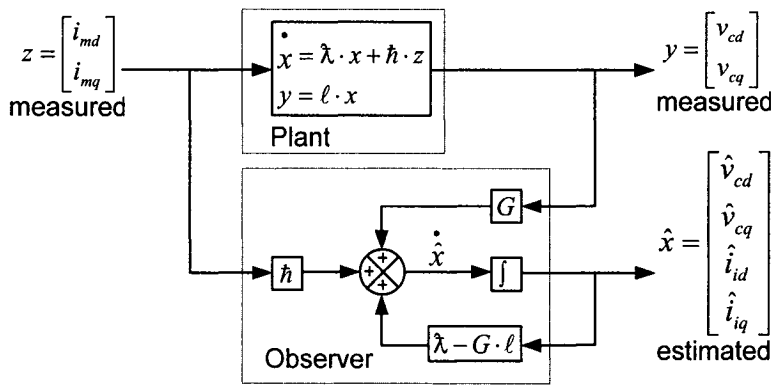


Fig. 3.21. Block diagram of the full-order current observer.

The construction of the current observer is based on the state-space model of the series compensator power circuit. The state variables of interest are $\boldsymbol{x} = [V_{cd}\ V_{cq}\ i_{id}\ i_{iq}]^T$, the output is defined as the sensed capacitor voltage $\boldsymbol{y} = [V_{cd}\ V_{cq}]^T$ and the perturbation is defined as the sensed converter output ac current $\boldsymbol{z} = [i_{md}\ i_{mq}]^T$.

$$\begin{aligned} \dot{\mathbf{x}} &= \lambda \cdot \mathbf{x} + \hbar \cdot \mathbf{z} \\ \mathbf{y} &= \ell \cdot \mathbf{x} \end{aligned} \tag{3.26}$$

where $\lambda = \begin{bmatrix} 0 & \omega & -1/C_f & 0 \\ -\omega & 0 & 0 & -1/C_f \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$, $\hbar = \begin{bmatrix} 1/C_f & 0 \\ 0 & 1/C_f \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$ and $\ell = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$.

The initially guessed values of i_{id} and i_{iq} are not accurate. But the variables V_{cd}, V_{cq}, i_{md} and i_{mq} are measured quantities, the current observer will correct the guessing errors automatically through continuous feedback compensation. The observer equation has the form of

$$\dot{\hat{\mathbf{x}}} = \mathbf{F} \cdot \hat{\mathbf{x}} + \mathbf{G} \cdot \mathbf{y} + \hbar \cdot \mathbf{z} \tag{3.27}$$

where $\hat{\mathbf{x}} = \begin{bmatrix} \hat{V}_{cd} & \hat{V}_{cq} & \hat{i}_{id} & \hat{i}_{iq} \end{bmatrix}^T$ represents the estimated values, **G** is the user-designed gain matrix of the full-order current observer. Based on the proposed power circuit, the gain matrix **G** has the form of

$$\mathbf{G} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \\ g_{31} & g_{32} \\ g_{41} & g_{42} \end{bmatrix} \tag{3.28}$$

F is the feedback matrix of the full-order observer that is computed based on the gain matrix **G** and the system model of the power circuit. It is expressed as,

$$\mathbf{F} = \lambda - \mathbf{G} \cdot \ell = \begin{bmatrix} f_{11} & 0 & f_{13} & 0 \\ 0 & f_{22} & 0 & f_{24} \\ f_{31} & f_{32} & 0 & 0 \\ f_{41} & f_{42} & 0 & 0 \end{bmatrix} \tag{3.29}$$

The derivation of the gain matrix **G** is based on the following design procedures:

i) Check the observability of the series compensator system. In this case, the number of linearly independent rows and columns of the observability matrix is 4, and the system is observable.

ii) Construct the dual system with $\lambda 1 = \lambda'; \hbar 1 = \ell'; \ell 1 = \hbar'$.

iii) Select the observer closed-loop poles **P**, and compute the feedback gain matrix **K** such that the eigenvalues of $(\lambda 1 - \hbar 1 * \mathbf{K})$ are the values specified in vector **P**.

iv) Obtain the full-order observer gain matrix **G** = **K'**.

The key step in the design of the full-order current observer is the selection of the pole placement vector **P**. These poles ought to be located in a way such that the dynamics of the current observer is five to ten times faster than that of the state feedback control system, to ensure the stability of the closed-loop control system.

The characteristic equation of the current observer is of forth-order and there are four poles. These poles should be placed in complex conjugate pairs with the magnitude of the imaginary part less than that of the real part, such that the observer exhibits a damping ratio greater than 0.707 and avoids any possible resonance.

The design of the full-order observer is implemented using MATLAB Control System Toolbox. The toolbox provides off-the-shelf mathematical functions for control

system design and optimization. Once the gain matrix **G** and the feedback matrix **F** have been defined, the derivative of the estimated current is computed instantaneously based on the following equation:

$$\begin{aligned} d\hat{i}_{id}/dt &= f_{31}\cdot\hat{V}_{cd} + f_{32}\cdot\hat{V}_{cq} + g_{31}\cdot V_{cd} + g_{32}\cdot V_{cq} \\ d\hat{i}_{iq}/dt &= f_{41}\cdot\hat{V}_{cd} + f_{42}\cdot\hat{V}_{cq} + g_{41}\cdot V_{cd} + g_{42}\cdot V_{cq} \end{aligned} \tag{3.30}$$

3.8 Simulation and Experimental Results

The proposed control strategy is firstly simulated in the MATLAB/SIMULINK environment. Then the same control algorithm is downloaded to the DSP set-up consisting of the MATLAB Real Time Workshop (RTW) and the dSPACE DS1103 PPC controller board to drive the laboratory prototype for experimental tests. The experimental implementation flowchart is shown in Fig. 3.22. The power circuit of the series compensator is also modeled as state-space matrixes to replace the laboratory prototype for real-time simulation.

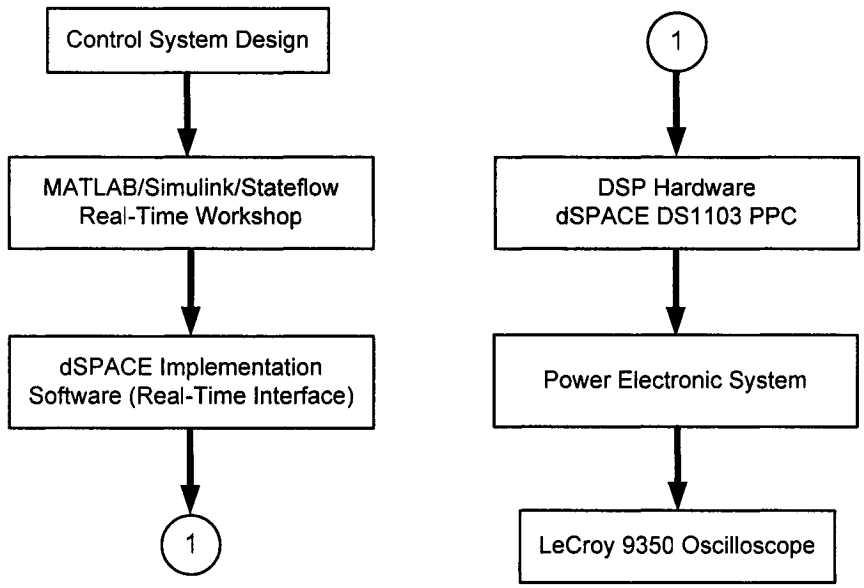


Fig. 3.22. The laboratory prototype implementation flowchart.

The proposed series compensator is designed at 2 kVA power rating. The nominal amplitude of the three-phase line-to-line voltage is selected at 70 V, and the dc-bus voltage is regulated to 200 V.

The parameter design of the switching harmonic LC filter is extended from [39][134]. It is assumed that all of the switching harmonic currents pass through the filter inductor and capacitor. By setting a 10% total harmonic distortion factor for the output current THD_i and the filter capacitor voltage THD_v of the series converter, and selecting a break frequency of the LC filter that is about ten times lower than that of the PWM switching frequency, the sizes of the filter inductor and capacitor are determined. For the proposed system, the frequency of the three-phase ac system is 60 Hz (1.0 pu) and the PWM switching frequency is 5.2 kHz (87 pu). The break frequency of the LC filter is chosen at 375 Hz (6.2 pu) and the parameters of the filter are set as L_f = 3 mH and C_f = 60 μf without the use of the damping resistor.

The proposed state variable feedback controller is designed to obtain a 4.2 ms settling time (T_{sett} = 4.2 ms) for load voltage compensation. Based on equation (3.22), the parameters of the controller are: k_1 = 3142, k_2 = 6932500 and τ_{dq} = 0.0012. As a result, the bandwidth of the overall closed-loop control system is around 715 rad/sec (1.9 pu). The bandwidth of the state feedback control block, which has been modeled as a second-order low-pass system in equation (3.20), is around 2630 rad/sec (6.9 pu).

As for the pole placement of the full-order current observer, the poles are chosen to tune the dynamic response of the current observer five times faster than that of the state feedback control system. As a result, the proposed four poles of the current observer are selected as -15189±j7130 and -20050±j12320 respectively. Based on equations (3.28)

and (3.29), the gain matrix **G** and the feedback matrix **F** of the current observer are calculated as:

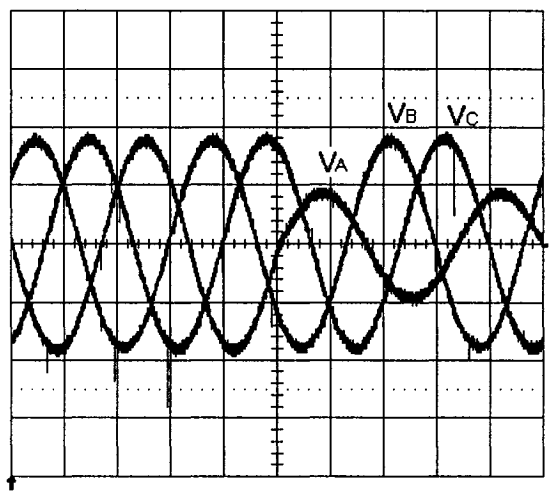
$$\mathbf{G} = 10^4 \times \begin{bmatrix} 4.01 & 0.038 \\ -0.038 & 3.036 \\ -3.32 & 0 \\ 0 & -1.69 \end{bmatrix}, \quad \mathbf{F} = 10^4 \times \begin{bmatrix} -4.01 & 0 & -1.67 & 0 \\ 0 & -3.03 & 0 & -1.67 \\ 3.32 & 0 & 0 & 0 \\ 0 & 1.69 & 0 & 0 \end{bmatrix}.$$

The sampling frequency of the DSP controller is selected at 16.7 kHz (278 pu), to accomplish the proposed control algorithms. Simulation and experimental results are obtained to verify the theoretical considerations.

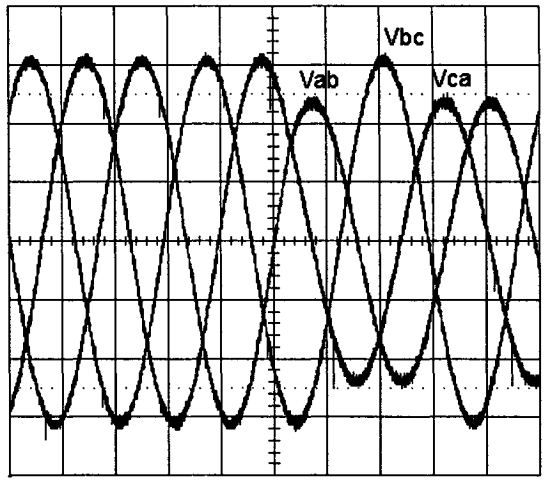
3.8.1 Voltage Fault Types with Y/Y and Y/Δ Connected Transformers

Most of the voltage sags encountered in distribution ac systems are single-line-to-ground fault. Fig. 3.23 shows that such a single-line-to-ground fault on the primary side of the distribution transformer causes a type *I* voltage fault on the secondary side of a Y/Y connected transformer, and a type *II* voltage fault on the secondary side of a Y/Δ connected transformer. The results verified the vector diagrams shown in Fig. 3.2.

a) Line-to-neutral voltage at the primary side of the transformer with the phase *a* voltage drops to 50% of the nominal amplitude. Volt: 50 V/div and time: 5 ms/div.



b) Line-to-line voltage at the secondary side of a Y/Y connected transformer. Volt: 50 V/div and time: 5 ms/div.



c) Line-to-line voltage at the secondary side of a Y/Δ connected transformer. Volt: 50 V/div and time: 5 ms/div.

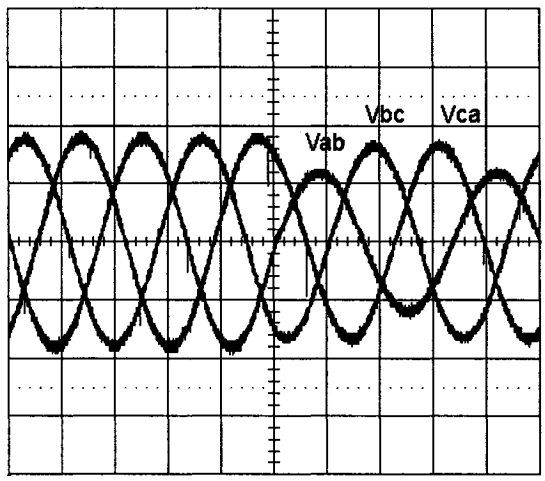


Fig. 3.23. Experimental results of the faulted supply voltage waveforms with Y/Y and Y/Δ connected transformers.

3.8.2 Performance with DC-Bus Voltage Fluctuation

This section tests the influence of the dc-bus voltage variation to the voltage compensation performance of the proposed control scheme. The output voltage of the PWM converter is tested without the use of the series coupling transformer for the sake of simplicity and the PWM converter is supplying a three-phase inductive load. Fig. 3.24 shows the performance of the converter with a dc-bus voltage fluctuation from 200 V to

180 V (10 %). Since the dc-bus voltage is sensed and fed to the controller for the calculation of the modulation index $[m]_{dq}$, the dc bus voltage variation only changes the modulation signals, whereas the converter output voltage is not affected by the disturbance. The result shows that the response of the converter is instantaneous.

The three-phase output voltage waveforms of the converter.

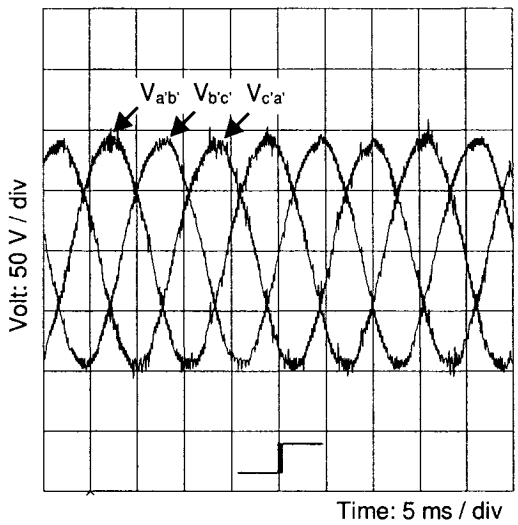


Fig. 3.24. Experimental results of the converter output voltages with a 10% dc-bus voltage step decrease.

3.8.3 Performance with Control Reference Step-Increase

This section tests the transient response of the voltage control system following a step change of the control reference. The output voltage of the PWM converter is tested without the use of the series coupling transformer and the converter is supplying a three-phase inductive load directly. Fig. 3.25 **a)** illustrates that the output voltage of the PWM converter gives a fast response following a step increase of the voltage reference, from 75 V increased to 100 V (25%). In addition, Fig. 3.25 **b)** shows that the *d-q* components of the output voltage have been decoupled and the proposed control scheme is capable of regulating the *d-q* components of the output voltage separately.

a) Output voltage of the converter with a 25% step increase.

b) The *d* component of the output voltage with a 25% step increase. The *q* component remains unchanged.

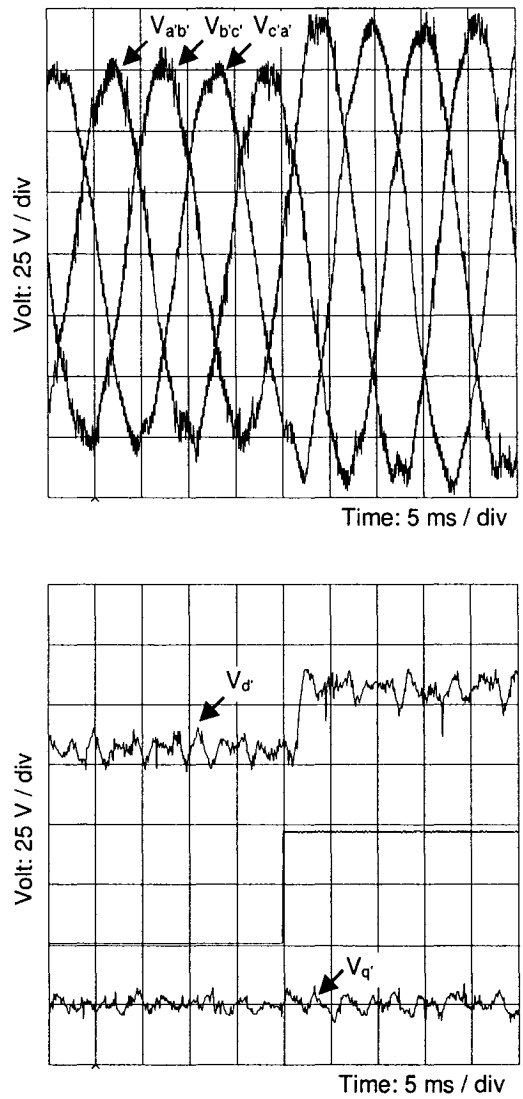


Fig. 3.25. Experimental results of the converter output voltages following a 25% control reference step-increase.

3.8.4 Dynamic Performance of the Series Compensator

Fig. 3.26 demonstrates the dynamic performance of the series compensator. The compensator injects three phase voltages into the ac system following a non-symmetrical voltage sag, and the load voltage is regulated to the nominal amplitude. Results illustrate that the transient response of the voltage control loop is fast, and the three phase voltages

at the load side are restored to the nominal amplitude after 4 ms following a non-symmetrical voltage fault in the ac system.

a) The faulted three-phase line-to-line supply voltages. One phase drops to 50%, and the other two phase drop to 75% of the nominal amplitude.

b) The three-phase line-to-line load voltages after compensation.

c) The injected voltages of the series compensator.

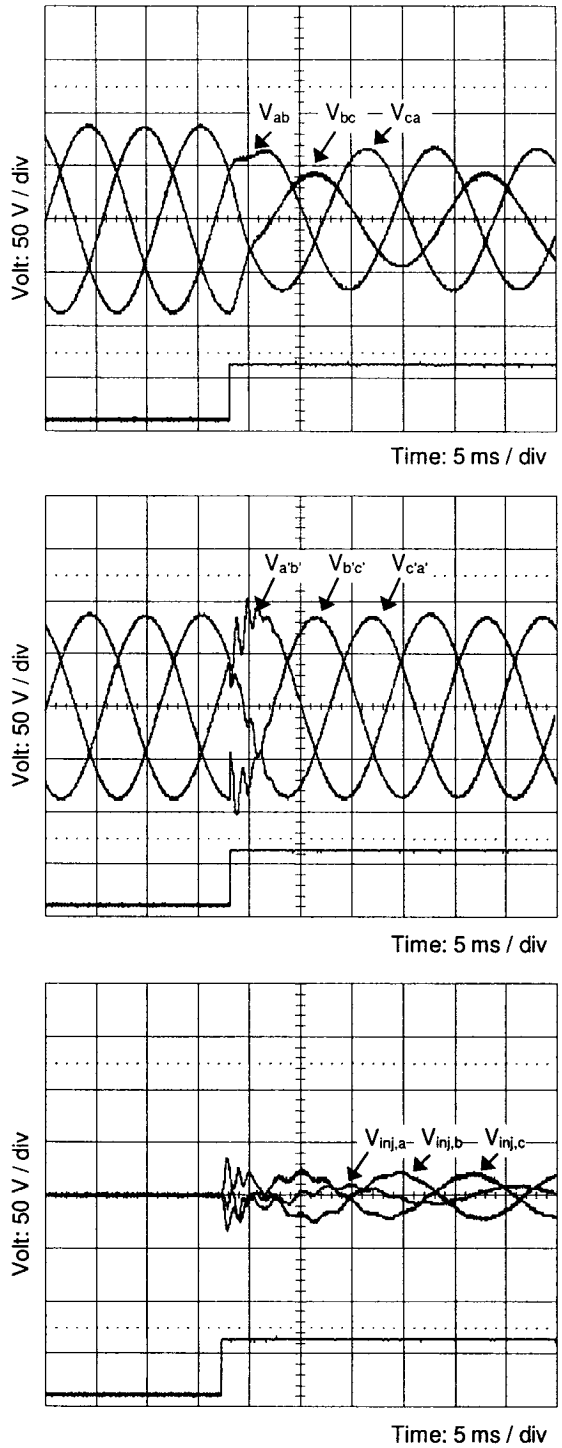


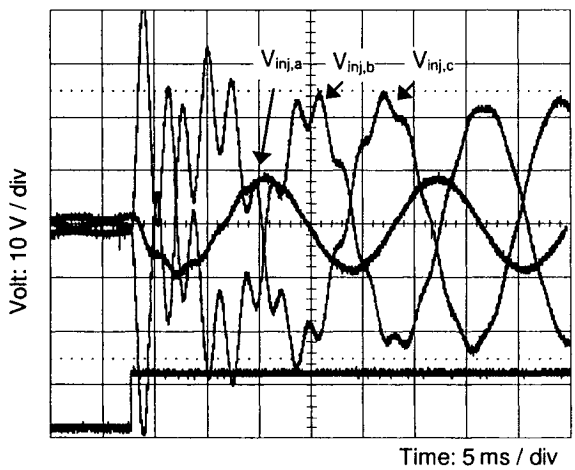
Fig. 3.26. Simulated results of the series compensator for a non-symmetrical supply voltage fault compensation.

3.8.5 Damping of the Oscillations Caused by the L-C Filter

Fig. 3.27 **a)** illustrates that the system damping is unsatisfactory for the series compensator with an open-loop controller. The parameters of the LC filter are $L_f = 3$ mH, $C_f = 60$ μf and the damping resistor $r_f = 0.8$ ohm. The series compensator injected voltage oscillates following the supply voltage sag, and the voltage oscillation is caused by the interaction of the inductor L_f and the capacitor C_f connected at the output of the PWM converter. A damping resistor r_f has to be inserted between the L_f and C_f components to damp the oscillation, but the damping resistor introduces heating losses.

In the proposed closed-loop control system, active damping of the LC filter is accomplished by the control algorithm and the damping resistor r_f is removed. Fig. 3.27 **b)** shows that the damping performance of the compensator injected voltage is improved with the proposed state variable feedback control scheme. It is noted that the voltage oscillation could not be compensated in the first 2 ms following a dynamic voltage sag, this is caused by the saturation of the PWM power converter.

a) Injected voltages with the open-loop feed forward control, and with a damping resistor of 0.8 ohm.



b) Injected voltages with the proposed state feedback control, and without the damping resistor.

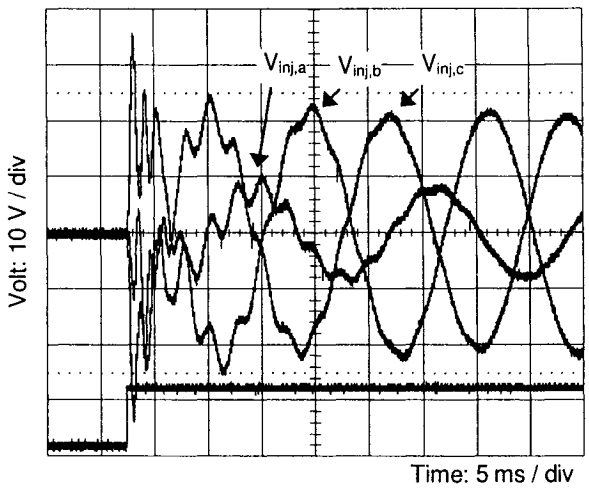
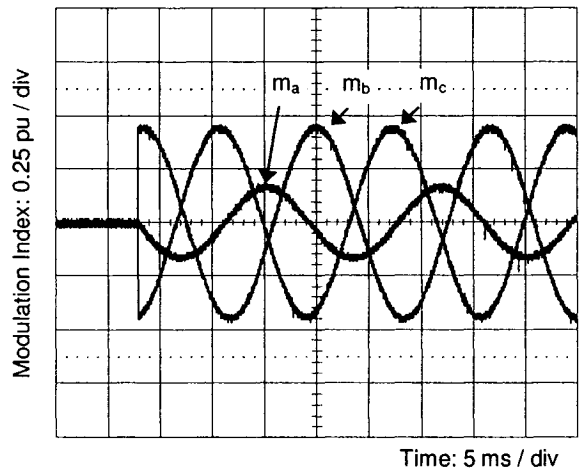


Fig. 3.27. Simulated results of the injected voltages with the open-loop control and the proposed state variable closed-loop control.

In addition, Fig. 3.28 **a)** illustrates that the modulation indices of the PWM converter is pure sinusoidal with the open-loop feed-forward control, whereas Fig. 3.28 **b)** shows the modulation indices of the converter contains sinusoidal and harmonics components with the proposed state feedback control scheme. This illustrates that the proposed state variable feedback controller acts actively to eliminate the output voltage oscillation caused by the interaction of the inductor and capacitor components of the LC filter.

a) Modulation indices with the open-loop feed forward control.



b) Modulation indices with the proposed state feedback control.

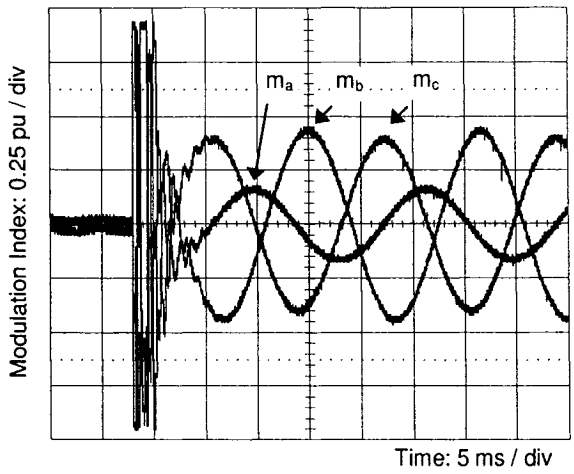
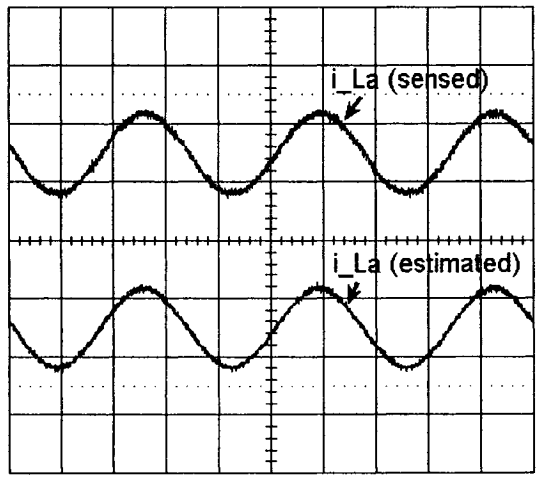


Fig. 3.28. Simulated results of the modulation indices generated by the open-loop controller and the proposed state feedback controller.

3.8.6 Performance of the Current Observer

Fig. 3.29 **a)** shows the phase *a* current obtained by using a current sensor and the proposed current observer respectively. The waveform of the estimated current is consistent with that of the sensed current. In addition, Fig. 3.29 **b)** shows the derivative of phase *a* current, which is obtained at the same time by using the proposed current observer. These are the steady state waveforms, and the current observer produces guessing errors during transients, which last for about 15 ms.

a) Phase *a* current obtained by the sensor (upper) and the proposed observer (bottom). Curr: 5 A/div and time: 5 ms/div.



b) Phase *a* current (5 A/div) and its derivative (500 A/sec/div) obtained by the proposed observer. Time: 5 ms/div.

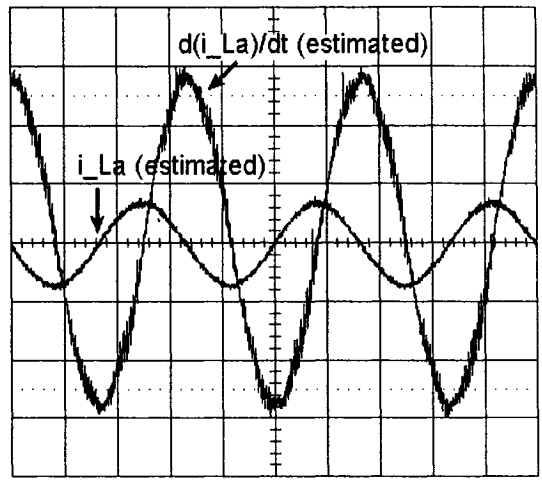


Fig. 3.29. Experimental results of the injected current waveforms obtained by the current sensor and the proposed current observer.

The capacitor C_f of the converter output LC filter is involved in the construction of the current observer. Any of the parameter mismatches detrimentally affects the accuracy of the current observer. Fig. 3.30 shows the estimation errors caused by the capacitor parameter mismatch on the calculation of rms values of the injected current and its derivative in a balanced three-phase ac system.

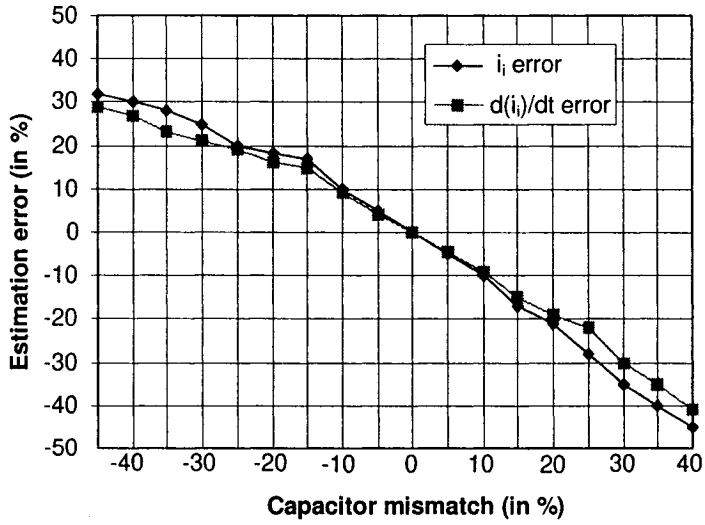


Fig. 3.30. Simulated results of the estimation errors of the current observer caused by the capacitor parameter mismatch.

3.9 CONCLUSIONS

Dynamic performance is a critical consideration in the control system design of the static series compensator, and is challenging the industry. The commonly used open-loop control scheme produces poorly damped response with the presence of the LC filter. On the other hand, the multi-loop PI feedback control structure has difficulties meeting the fast voltage compensation requirement due to the dynamic separation of the two cascaded control loops.

The proposed state feedback control strategy exploits the modern treatment of classical control theory, based on state space approach. It introduces a new control variable to change the system behavior into the desired direction, and then derives the transformation between the new control variable and the PWM modulation index. As a result, the proposed control system is capable of reducing the response time for dynamic voltage sag compensation, and providing active damping of the LC filter. The software-based current observer estimates the injected current and its derivative accurately under various fault conditions. Simulation and experimental results confirm the theoretical considerations.

CHAPTER 4

DIRECT POWER CONTROL OF STATIC SHUNT COMPENSATOR

4.1 INTRODUCTION

The shunt-connected var compensator or so called the active filter is used in industrial fields at medium and low power levels to compensate the harmonics and improve the power factor associated with unbalanced and nonlinear loads. Literature [85] shows that most of the active filters are designed based on the current control method with a cascaded multi-loop control structure. The inner current loop compensates harmonics and reactive power, and the outer voltage loop regulates the dc bus voltage. The current controller either injects the current harmonics consumed by the nonlinear load or forces the line current to be sinusoidal. Typically, the dynamic response of the inner current loop is fast and that of the outer voltage loop is slower, and the dc-link capacitor must have a sufficient energy storage capability to maintain a stable dc bus voltage during transients. In addition, an appropriate pulse width modulation scheme should be used for the power converter.

A number of new techniques have recently been proposed to improve the control of PWM converters for a number of applications. Issues addressed are the reduction of the number of sensors, alternate modulation schemes and the integration of control and modulation functions. The latter schemes have the advantage of faster transient response and the possibility of controlling simultaneously more than one variable. Among these schemes, the direct torque control (DTC) has been successfully applied in high

performance induction motor drives, for both the wound rotor [86] and the cage rotor [87] configurations. These methods of control are computationally simple and do not require rotor position sensors. The control schemes for synchronous rectifiers similar to the induction motor DTC, so called as Direct Power Control (DPC), have also been explored [88][89][90]. In these schemes, the instantaneous active and reactive power are directly controlled in a manner analogous to torque and flux control in induction motor, and the controllers are associated with the implementation of sensorless operation. However, the application of such a technique to the control of STATCOMs and active filters has not been reported so far. In addition, the regulation of PWM switching frequency has not been considered in most of the reported applications, instead, the PWM gating signals were fed directly from the hysteresis controllers. The reported papers on fixing the switching frequency of the PWM converter [91][94] were designed based on the specific motor parameters, and limited to motor drive applications.

This chapter develops the direct power control structure for active filters and shunt-connected var compensators. It derives the characteristics of the instantaneous active and reactive power terms based on the previous work [77][78], and reformulates the appropriate power terms. The specific PWM switching functions are derived systematically based on instantaneous power flow control, and the proposed controller adjusts dynamically the bandwidths of the two hysteresis comparators, so as to control the average PWM switching frequency. This leads to the elimination of short switching pulses and reduction of switching losses. In addition, since the phase information of the PCC voltage is used for the selection of switching states, this chapter also presents an algorithm to identify the sector where the voltage vector is currently located. The

proposed voltage phase tracking algorithm only involves simple algebraic and logical computations, and avoids intensive trigonometric functions as well as consequent approximation errors.

Compared to the multi-loop control structure, the proposed DPC control directly uses power terms as control variables and integrates control and modulation functions. Therefore, the cascaded control loops, the *abc-dq* co-ordinates transformation and the separately implemented PWM modulator that have been included in multi-loop control are no longer required in the proposed DPC control. Compared to the other DPC control applications that have been reported in the previous work, the proposed DPC scheme is reformulated and oriented to load harmonics and reactive power compensation, in which, the PWM switching functions are re-defined and the bandwidths of the two hysteresis comparators are dynamically adjusted to regulate the average switching frequency. The proposed DPC control system is tested on a 2 kVA laboratory prototype for load harmonics filtering and load fluctuation compensation respectively. Simulation and experimental results confirm that the proposed DPC control is insensitive to load conditions and provides good dynamic and steady state performance.

4.2 THE INSTANTANEOUS POWER TERMS IN THREE-PHASE AC SYSTEMS

In general, the active and reactive power terms in three-phase power systems are defined on the basis of average value under steady state condition. The theory of instantaneous power was developed in [77][78]. These papers provided a generalized definition of instantaneous active and reactive power, which is valid for sinusoidal or non-sinusoidal, balanced or unbalanced, three-phase power systems.

To deal with the instantaneous voltage and current in three-phase ac systems, it is convenient to analyze in the orthogonal α–β co-ordinates. In a typical three-phase three-wire ac system, the zero-sequence component is always zero, and the three-to-two phase transformation matrix is of the form as

$$\begin{bmatrix} v_\alpha & v_\beta \end{bmatrix}^T = \mathbf{M} \cdot \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}^T \tag{4.1}$$

where $\mathbf{M} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}$, and the factor $\sqrt{2/3}$ is for power equivalence between the three-phase and two-phase ac systems.

The instantaneous active power in the electrical system is defined as,

$$p = v_\alpha i_\alpha + v_\beta i_\beta = v_a i_a + v_b i_b + v_c i_c \tag{4.2}$$

The instantaneous reactive power is defined as,

$$q = v_\beta i_\alpha - v_\alpha i_\beta = -\frac{1}{\sqrt{3}}\left(v_a(i_b - i_c) + v_b(i_c - i_a) + v_c(i_a - i_b)\right) \tag{4.3}$$

In a balanced three-phase power system, the numerical value (magnitude) of the instantaneous active power is a constant, and is equal to three times of the steady-state active power per phase. The numerical value (magnitude) of the instantaneous reactive power is also a constant and equal to three times of the steady-state reactive power per phase. However, in terms of physical meaning, the instantaneous active power is the instantaneous power flowing between the source and the load. The instantaneous reactive power circulates among the three phases, and makes no contribution to the instantaneous power flowing from the source to the load. But the reactive power indeed increases the magnitude of the three phase currents and the losses in power lines.

In an unbalanced three-phase power system, or a distorted three-phase ac system with non-linear loads, neither the instantaneous active power nor the instantaneous reactive power is constant, and the harmonic ripples are introduced as

$$p = \bar{p} + \tilde{p} \qquad q = \bar{q} + \tilde{q} \tag{4.4}$$

Table 4.1. Characteristics of the Instantaneous Power Terms

Power Terms	Characteristics
$\bar{p}$	The average active power delivered from the source to the load, and it represents the active power generated by the positive-sequence voltage and current.
$\bar{q}$	The average reactive power circulating among the three phases and generated by the positive sequence voltage and current. It does not contribute to any power flowing from the source to the load, but it increases the line current amplitude and the associated losses.
$\tilde{p}$	The power ripples caused by negative sequence component and other harmonics. It corresponds to power oscillation between the source and the load, and its average is zero.
$\tilde{q}$	The power ripples caused by negative sequence component and other harmonics. It corresponds to power oscillation among three phases, and its average is zero.

The following two important conclusions are noticed:

i) To compensate the instantaneous reactive power ripple $\tilde{q}$, there is no power drawn from the dc-link energy storage capacitor to the ac system, since the power ripple circulates among the three phases. Taking this fact into account, the dc-link capacitor is not required theoretically to compensate the reactive current and harmonics.

ii) To compensate the instantaneous active power ripple $\tilde{p}$, an energy-storage capacitor is required in the dc-bus of the voltage source converter to absorb or supply the ripple of power. In the design of an active filter, the capacitor is determined based on the allowable ripple tolerance of the dc-bus voltage and the dynamic response of the dc-bus voltage regulation loop. Since DPC control

provides fast dynamic response, a small capacitor could be enough to maintain a stable dc-bus voltage during transients and ensure a good harmonic filtering capability.

4.3 DESCRIPTION OF THE PROPOSED SHUNT COMPENSATOR

The shunt-connected var compensator is based on a standard three-phase two-level voltage source converter as Fig. 4.1 shows. For the proposed DPC control scheme, four state variables, including the instantaneous active and reactive power drawn by the nonlinear load and those injected by the var compensator, are computed continuously. The power terms of the nonlinear load are used to generate the control reference, and those of the var compensator are fed back to compare with the control reference. Two hysteresis comparators are used for control purpose and the PWM gating signals are generated based on the output of the comparators. The output of the dc-bus voltage regulation loop is transformed and treated as an instantaneous active power quantity, which is added to the corresponding active power control reference. The dynamic separation of the control system is based on the fact that the response of the dc-bus voltage regulation block is slower than that of the instantaneous power control block (for harmonic and reactive power compensation). The DPC control structure results in averaged waveform synthesis, and the instantaneous power injected by the compensator varies within the hysteresis band. During each switching action, a voltage vector is chosen to force the compensator injected power following the control reference.

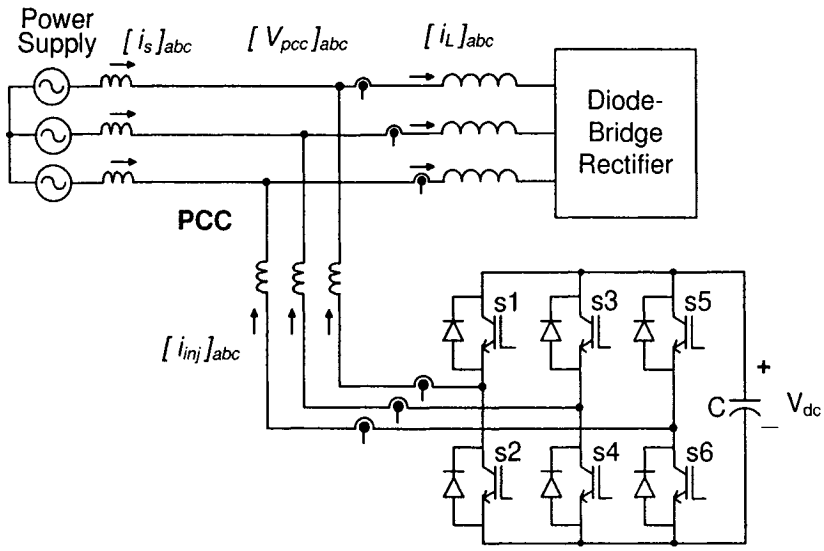


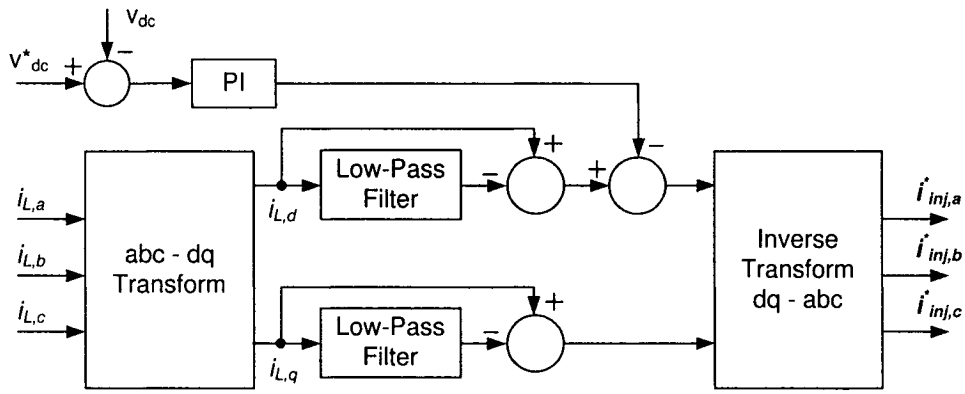
Fig. 4.1. Power circuit of the shunt-connected var compensator.

The entire control algorithm is carried out in the stationary *abc* co-ordinates, without the need of *abc-dq0* transformation. The instantaneous power terms used in this chapter are similar to those reported in [92]. However, in the previously reported work, the instantaneous power control is implemented through a current control method based on *abc-dq0* transformation. Therefore, the forward and backward transformation between the current and the power has to be performed in [92], which is based on current control. The proposed DPC method directly uses power quantities as control variables and results in simple control architecture. For comparison purpose, the control reference generation schemes, based on the current control method and the direct power control method respectively, are shown in Fig. 4.2, and the two control loop structures are illustrated in Fig. 4.3.

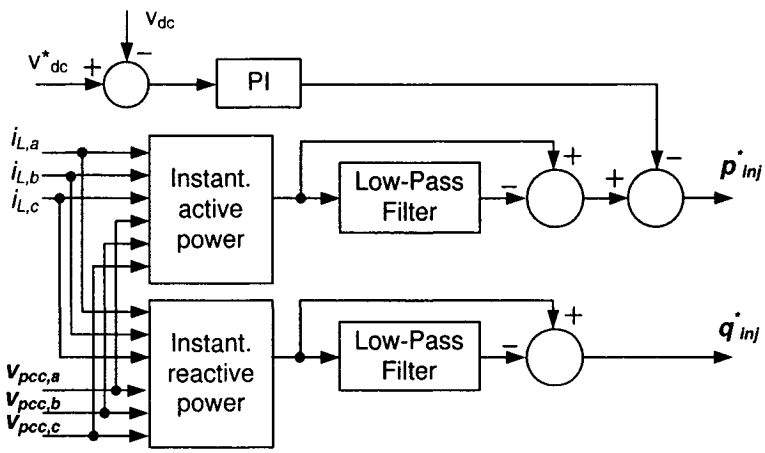
The commonly used control method is based on current control scheme. It senses and compensates the distorted load current to eliminate current harmonics from the line

current. The dc-bus capacitor voltage is regulated through fundamental frequency current injection to charge or discharge the dc-bus energy storage capacitor.

On the other hand, the proposed direct power control extracts the load power ripples as control references. It regulates the injected power flows of the converter and eliminates the intermediate step of regulating the injected current. The dc-bus voltage is also regulated based on power requirement of the energy storage capacitor. In addition, the control and PWM functions are integrated into one loop.

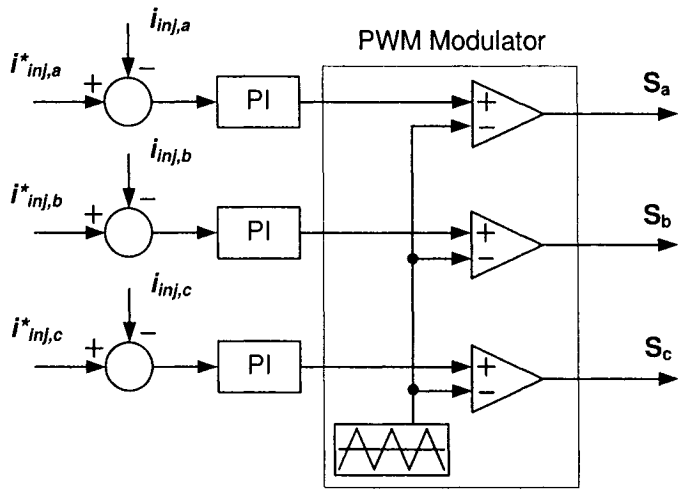


a) Current reference generation scheme for the current control method.

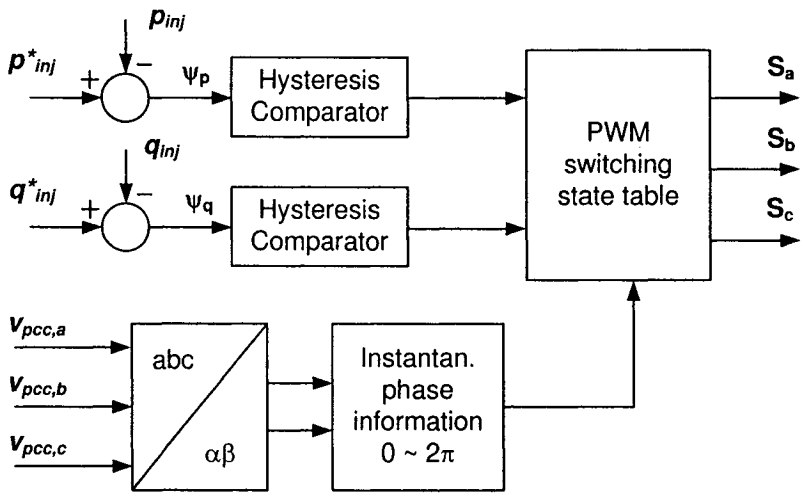


b) Instantaneous power reference generation scheme for the DPC control method.

Fig. 4.2. Control reference generation schemes of the current control method and the DPC control method.



a) Current control loop and PWM modulator for the current control method.



b) Instantaneous power control loop and switching state table for the DPC control method.

Fig. 4.3. Control structures and PWM methods of the current control method and the DPC control method.

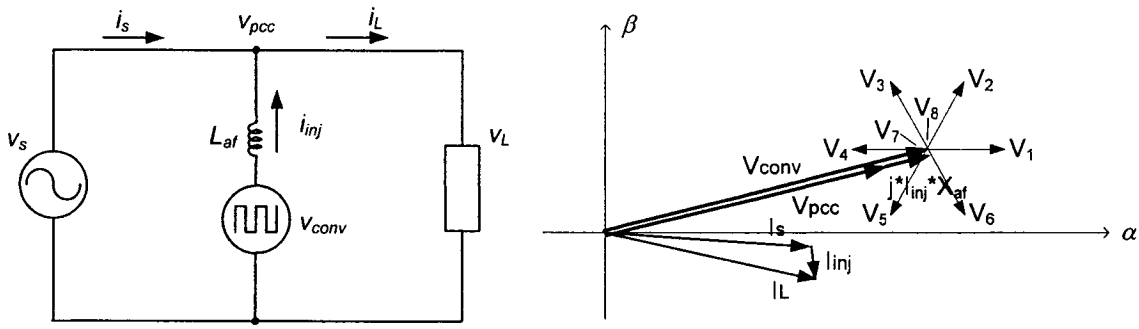
As a result, the proposed direct power control compensates the power ripples drawn by the nonlinear load, and forces the instantaneous active power p and reactive power q to be constant on the power input side. The power system only supplies sinusoidal currents, as if it was supplying a three-phase balanced linear load. The DPC control requires a high sampling frequency of the DSP controller to minimize the switching time

error and to prevent the injected power of the converter from exceeding the hysteresis boundaries. But the average switching frequency of the converter based on the DPC control stays at the same range as that based on the conventional current control strategy and using standard PWM modulation.

4.4 THE SELECTION OF PWM SWITCHING FUNCTIONS

With the DPC control scheme, the injected active power and reactive power of the var compensator are regulated by two hysteresis comparators to limit the instantaneous power ripples drawn from the power system. This type of control leads to an averaged waveform synthesis of the PWM converter.

The simplified equivalent circuit of the var compensator and the corresponding vector diagram are illustrated in Fig. 4.4. During each switching action, one switching vector is selected based on the instantaneous power injection requirement and the sector in which the PCC voltage vector is currently residing.



a) Simplified equivalent circuit of the var compensator.

b) Vector diagram illustrating the selection of switching vectors.

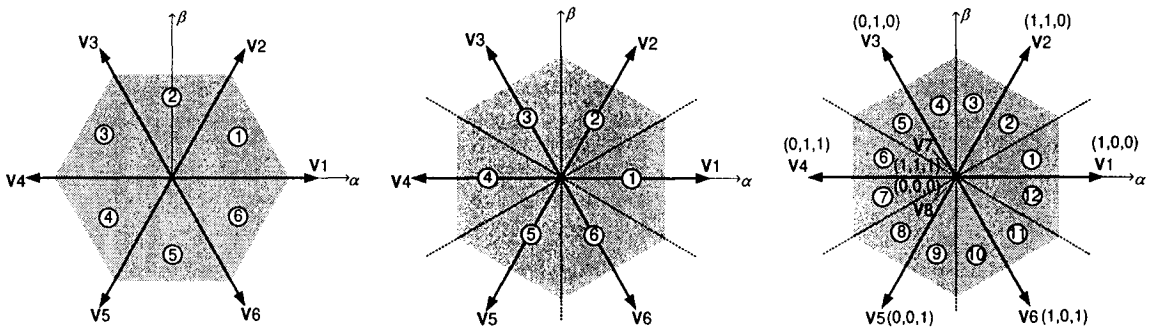
Fig. 4.4. Simplified diagrams of the var compensator with DPC control.

As Fig. 4.4 **b)** shows, by choosing voltage vector V_1, both the injected active power and the injected reactive power of the var compensator are increased. On the other hand, by choosing voltage vector V_2, the injected active power of the var compensator is

increased while the injected reactive power is reduced at the same time. If voltage vector V_3 is chosen, both the injected active power and the injected reactive power are reduced. It should be noted that the influence of the voltage vectors to the power flow of the var compensator depends on the sector number where the V_{pcc} voltage is currently allocated.

4.4.1 Sector Division Methods

One of the sector division methods divides the α–β plane into six sectors separated by the six voltage space vectors, as shown in Fig. 4.5 **a)**. This kind of division forms an hexagon with six non-zero voltage space vectors ($\mathbf{V_k}$, k= 1, 2, ..., 6), there are two zero vectors ($\mathbf{V_7}$, $\mathbf{V_8}$) at the origin of the plane. This method is used in the widely applied space vector modulation for voltage synthesis, and the best tracking is obtained when two of the non-zero space vectors adjacent to the reference voltage and one of the zero vectors are selected to synthesize the reference voltage. In direct power control applications, the control reference is the instantaneous power terms instead of the voltage vectors, and the synthesis method used for space vector modulation could not be used directly to provide instantaneous power regulation.



a) The six sectors divided by the voltage space vectors.

b) The six sectors centered with the voltage space vectors.

c) The twelve sectors by combining method **a)** and **b)**.

Fig. 4.5. Three schemes for the sector division in α–β plane.

However, this kind of sector division technique can be extended to track the instantaneous power reference with modified switching functions. This is based on the fact that controlling the magnitude and phase angle of the converter output voltage regulates the output power of the converter as well.

Another sector division method is to separate the six sectors to centre with the six voltage space vectors, as shown in Fig. 4.5 **b)**. This kind of division gets the same instantaneous power control performance as the first method.

A more effective way is to divide the plane into twelve portions, as shown in Fig. 4.5 **c)**. It combines the advantages of the two six-sector division methods. Considering the inherent symmetry, the phase angle ranges of the twelve sectors in the stationary α–β co-ordinates are expressed as

$$(\pi/6)(n-1) < \Theta_n \le (\pi/6)n \qquad n = 1,2,...,12 \tag{4.5}$$

4.4.2 Derivation of the Switching State Table

In direct power control, the instantaneous active power command p^* is generated based on the instantaneous active power ripples drawn by the non-linear load, plus the power requirement of the dc-bus voltage control loop. The instantaneous reactive power command q^* equals to the instantaneous reactive power ripples consumed by the non-linear load. The power terms of the nonlinear load are expressed as,

$$\begin{aligned} p_L &= v_{pcc,a} i_{L,a} + v_{pcc,b} i_{L,b} + v_{pcc,c} i_{L,c} \\ q_L &= -\left(v_{pcc,a}\left(i_{L,b} - i_{L,c}\right) + v_{pcc,b}\left(i_{L,c} - i_{L,a}\right) + v_{pcc,c}\left(i_{L,a} - i_{L,b}\right)\right)/\sqrt{3} \end{aligned} \tag{4.6}$$

The power references are obtained by extracting the ripples from the load power terms. On the other hand, the instantaneous power terms injected by the var compensator are defined as,

$$p_{inj} = v_{pcc,a} i_{inj,a} + v_{pcc,b} i_{inj,b} + v_{pcc,c} i_{inj,c}$$
$$q_{inj} = -\left(v_{pcc,a}\left(i_{inj,b} - i_{inj,c}\right) + v_{pcc,b}\left(i_{inj,c} - i_{inj,a}\right) + v_{pcc,c}\left(i_{inj,a} - i_{inj,b}\right)\right)/\sqrt{3} \quad (4.7)$$

After compensation, the ac system provides only the balanced and average power portion drawn by the nonlinear load, and the var compensator supplies the instantaneous power ripples drawn by the nonlinear load. If the var compensator has spare power injection capability, it can also inject all of the reactive power required by the load, including both the average reactive power component and the reactive power ripples, and a unity power factor is accomplished at the utility side in this case.

The block diagram of the direct power control system is shown in Fig. 4.6. The instantaneous power terms of the nonlinear load and those of the var compensator are inputs to the hysteresis comparators. After a two-to-four decoder, the comparator output determines the row value of the switching table. The column value is the sector number where the voltage vector is currently residing and is divided into 12 segments.

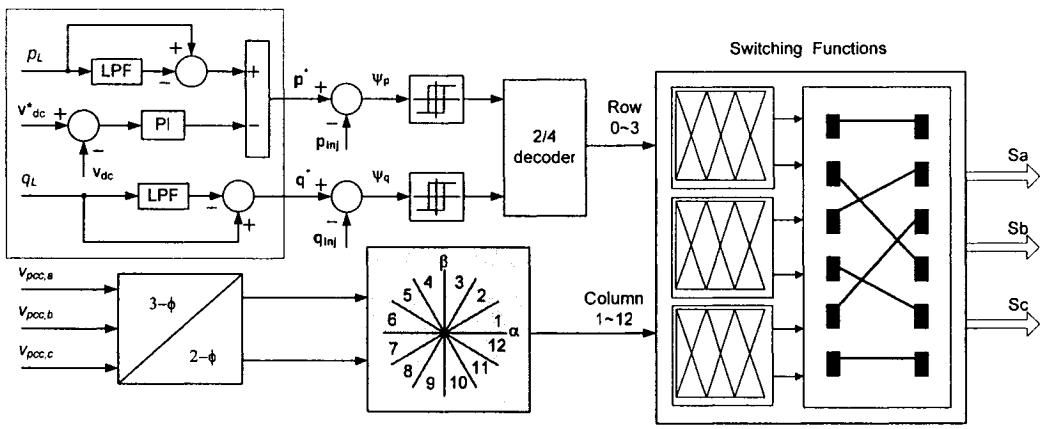


Fig. 4.6. Block diagram of the proposed direct power control system.

By applying an appropriate switching vector to the PWM power converter, the change of the converter instantaneous power can be driven to the desired direction. The voltage space vector can be taken from one out of eight possible positions (including six

non-zero vectors and two zero vectors). The influence of each voltage vector ($\mathbf{V_1}$ - $\mathbf{V_8}$) on the instantaneous active and reactive power flow is different, and results in different control dynamics. Assuming the PCC voltage vector is located in sector 1 as illustrated in Fig. 4.5 **c)**, the general selection criteria of the converter switching vectors is summarized in Table 4.2.

Table 4.2. Principles for Switching Vector Selection

Power errors	Criteria for the choosing of voltage space vectors	Application examples (in sector 1)
$\psi_q \geq 0$	Select the voltage vector that forces the converter output current lag in phase.	Choosing $\mathbf{V_1}$ (1,0,0) or $\mathbf{V_6}$ (1,0,1) in the case of $\psi_p \geq 0$.
		Choosing $\mathbf{V_7}$ (1,1,1), $\mathbf{V_8}$ (0,0,0) or $\mathbf{V_5}$ (0,0,1) in the case of $\psi_p < 0$.
$\psi_q < 0$	Select the voltage vector that forces the converter output current lead in phase.	Choosing $\mathbf{V_2}$ (1,1,0) in the case of $\psi_p \geq 0$.
		Choosing $\mathbf{V_7}$ (1,1,1), $\mathbf{V_8}$ (0,0,0), $\mathbf{V_3}$ (0,1,0) or $\mathbf{V_4}$ (0,1,1) in the case of $\psi_p < 0$.
$\psi_p \geq 0$	Select the voltage vector that drives the converter output current increase.	Choosing $\mathbf{V_1}$ (1,0,0) or $\mathbf{V_6}$ (1,0,1) in the case of $\psi_q \geq 0$.
		Choosing $\mathbf{V_2}$ (1,1,0) in the case of $\psi_q < 0$.
$\psi_p < 0$	Select the voltage vector that drives the converter output current decrease.	Choosing $\mathbf{V_7}$ (1,1,1), $\mathbf{V_8}$ (0,0,0) or $\mathbf{V_5}$ (0,0,1) in the case of $\psi_q \geq 0$.
		Choosing $\mathbf{V_7}$ (1,1,1), $\mathbf{V_8}$ (0,0,0), $\mathbf{V_3}$ (0,1,0) or $\mathbf{V_4}$ (0,1,1) in the case of $\psi_q < 0$.

Table 4.3. Switching Functions Based on Instantaneous Power Comparison

Row		Column											
		θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
0	$\psi_p < 0$ $\psi_q < 0$	0,1,0	0,1,1	0,1,1	0,0,1	0,0,1	1,0,1	1,0,1	1,0,0	1,0,0	1,1,0	1,1,0	0,1,0
1	$\psi_p < 0$ $\psi_q \geq 0$	0,0,1	1,0,1	1,0,1	1,0,0	1,0,0	1,1,0	1,1,0	0,1,0	0,1,0	0,1,1	0,1,1	0,0,1
2	$\psi_p \geq 0$ $\psi_q < 0$	1,1,0	1,1,0	0,1,0	0,1,0	0,1,1	0,1,1	0,0,1	0,0,1	1,0,1	1,0,1	1,0,0	1,0,0
3	$\psi_p \geq 0$ $\psi_q \geq 0$	1,0,0	1,0,0	1,1,0	1,1,0	0,1,0	0,1,0	0,1,1	0,1,1	0,0,1	0,0,1	1,0,1	1,0,1

By applying the operation principle to all twelve sectors in general cases, a two-dimensional switching state table is derived and listed in Table 4.3. During the implementation, the switching functions S_a, S_b and S_c are obtained based on the look-up table.

4.5 CALCULATION OF THE SECTOR NUMBER

The implementation of DPC control requires the calculation of the sector number where the PCC voltage vector is currently residing in α–β plane. Usually, the calculation of the sector number requires computing the phase angle θ of the voltage vector at every sampling instant. The computation uses the trigonometric functions and is usually an approximation by means of interpolation based on a look-up table stored in memory.

$$\theta = \tan^{-1}(V_{pcc,\beta} / V_{pcc,\alpha}) \tag{4.8}$$

This section proposes a new algorithm to compute the sector number. The algorithm only uses simple algebraic and logical computations. Therefore, it saves the DSP processing time for other important tasks such as PWM switching frequency control.

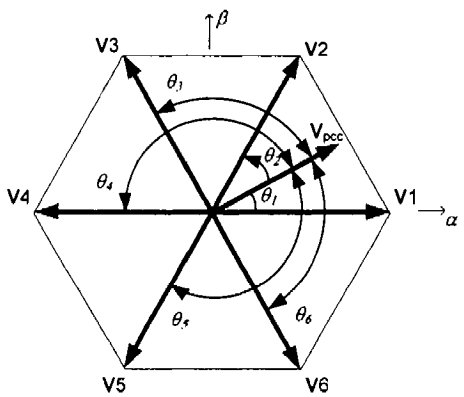


Fig. 4.7. Relations between the sector number and the value of $|V_k| \cdot |V_{pcc}| \cdot \cos\theta_k$.

By observing Fig. 4.7, it can be induced that the two adjacent vectors (V_i and V_{i+1}) of the output voltage vector V_{pcc} correspond to the two largest components among the six values of $|V_k|\cdot|V_{pcc}|\cdot\cos\theta_k$, k = 1,2,...,6.

After some mathematical manipulation, the calculation of the numerical values of $|V_k|\cdot|V_{pcc}|\cdot\cos\theta_k$ is transformed to simple algebraic computations. Taking k = 2 as an example,

$$\begin{aligned}
|V_2|\cdot|V_{pcc}|\cdot\cos\theta_2 &= \begin{bmatrix} V_{2,\alpha} & V_{2,\beta} \end{bmatrix}\cdot\begin{bmatrix} V_{pcc,\alpha} \\ V_{pcc,\beta} \end{bmatrix} \\
&= \begin{bmatrix} \frac{1}{2}V_{dc} & \frac{\sqrt{3}}{2}V_{dc} \end{bmatrix}\cdot\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\cdot\begin{bmatrix} V_{pcc,a} \\ V_{pcc,b} \\ V_{pcc,c} \end{bmatrix} \\
&= (0.5\cdot V_{pcc,a} + 0.5\cdot V_{pcc,b} - V_{pcc,c})\cdot V_{dc}
\end{aligned} \tag{4.9}$$

Applying the same principle to all of the six vectors, the following equations are obtained,

$$\begin{aligned}
n_1 &= |V_1|\cdot|V_{pcc}|\cdot\cos\theta_1 = (V_{pcc,a} - 0.5\cdot V_{pcc,b} - 0.5\cdot V_{pcc,c})\cdot V_{dc} \\
n_2 &= |V_2|\cdot|V_{pcc}|\cdot\cos\theta_2 = (0.5\cdot V_{pcc,a} + 0.5\cdot V_{pcc,b} - V_{pcc,c})\cdot V_{dc} \\
n_3 &= |V_3|\cdot|V_{pcc}|\cdot\cos\theta_3 = (-0.5\cdot V_{pcc,a} + V_{pcc,b} - 0.5\cdot V_{pcc,c})\cdot V_{dc} \\
n_4 &= |V_4|\cdot|V_{pcc}|\cdot\cos\theta_4 = -n_1 \\
n_5 &= |V_5|\cdot|V_{pcc}|\cdot\cos\theta_5 = -n_2 \\
n_6 &= |V_6|\cdot|V_{pcc}|\cdot\cos\theta_6 = -n_3
\end{aligned} \tag{4.10}$$

It should be noted that the voltage vectors of interest ($V_{pcc,a}, V_{pcc,b}, V_{pcc,c}$) are the instantaneous PCC bus voltage vectors at the axis *a*, *b* and *c* respectively. In the case of balanced three-phase ac systems, the instantaneous voltage vector can be obtained directly from the sensed three-phase voltages, and equation (4.10) is further simplified as,

$$
\begin{aligned}
n_1(k) &= 1.5 \cdot v_{pcc,a}(t_k) \cdot V_{dc} \\
n_2(k) &= -1.5 \cdot v_{pcc,c}(t_k) \cdot V_{dc} \\
n_3(k) &= 1.5 \cdot v_{pcc,b}(t_k) \cdot V_{dc}
\end{aligned}
\tag{4.11}
$$

Whereas in unbalanced and distorted three-phase ac systems, the aforementioned algorithm is not applicable. This limits the applicability of the proposed algorithm to the power systems with good quality voltage supply, such as the applications of active filter or power quality compensator with a series device to compensate the line voltage and a shunt device to compensate the line current.

Now the problem of computing sector number is transformed into the process of finding the largest element n_i and the second largest element n_j at every sampling time interval.

$$
n_i(k), \quad n_j(k) = \max\{n_1(k) \quad n_2(k) \quad n_3(k) \quad n_4(k) \quad n_5(k) \quad n_6(k)\} \tag{4.12}
$$

There are limited possibilities for the values of i and j, and the sector number is determined based on the flowchart as,

```
IF( j>i )
 {IF (i==1&& j==6) n=12; ELSE n=2i-1;}
ELSE
 {IF(i==6&& j==1) n=11; ELSE n=2i-2;}
```
(4.13)

4.6 CONTROL OF THE PWM SWITCHING FREQUENCY

In practical implementation, the highest switching frequency of the IGBT power devices should be limited to a certain range according to its power rating. A method is investigated in this section by using variable bandwidth of the hysteresis comparators.

Some algorithms were reported in literatures [104][118] to fix the switching frequency of the current-controlled converter with a hysteresis controller. The reported algorithm calculates an appropriate hysteresis bandwidth of the current at every sampling instant based on the pre-selected switching time interval. Whereas in direct power control, the control variables are power terms that are product of voltage and current. It is computational intensive to predict a proper hysteresis bandwidth at every sampling instant to obtain a constant switching frequency, and the estimation errors may cause the system to oscillate. Different from the previously reported algorithms, the proposed method is aimed at limiting the average switching frequency of the converter, thus to eliminate the short switching pulses and to reduce the switching losses. The method is developed as following:

i) The setting range of the hysteresis bandwidth is determined based on the observation of steady state performance of the var compensator. For the specific experimental prototype implemented in this chapter, the hysteresis bandwidth is set between 2 to 5 var, which represents a tolerance of power errors from 4 to 10 var or 0.04 to 0.09 pu, and the resulting PWM switching frequency varies between 5 kHz to 8 kHz. Choosing a hysteresis bandwidth larger than 5 var or a switching frequency lower than 5 kHz may introduce severe harmonics.

ii) A small hysteresis bandwidth causes unnecessary short switching pulses and additional switching losses, while a large bandwidth increases harmonic contents. During the transient state, a large bandwidth is used to limit the switching frequency within 8 kHz. When the system enters into steady state, the hysteresis bandwidth is adjusted to a small value to reduce the switching harmonics.

iii) The switching frequency is calculated based on the number of rising edges of the switching pulse in half a cycle time (8.3 ms). If the switching frequency is higher than 7.5 kHz (63 pulses), the bandwidth is increased. When the switching frequency is lower than 6.5 kHz (54 pulses), the bandwidth is decreased.

These design guidelines are implemented with the DSP controller. After design optimization of the proposed control system, the DSP controller has enough processing time for PWM quality improvement. The proposed flowchart for switching frequency control is shown in Fig. 4.8.

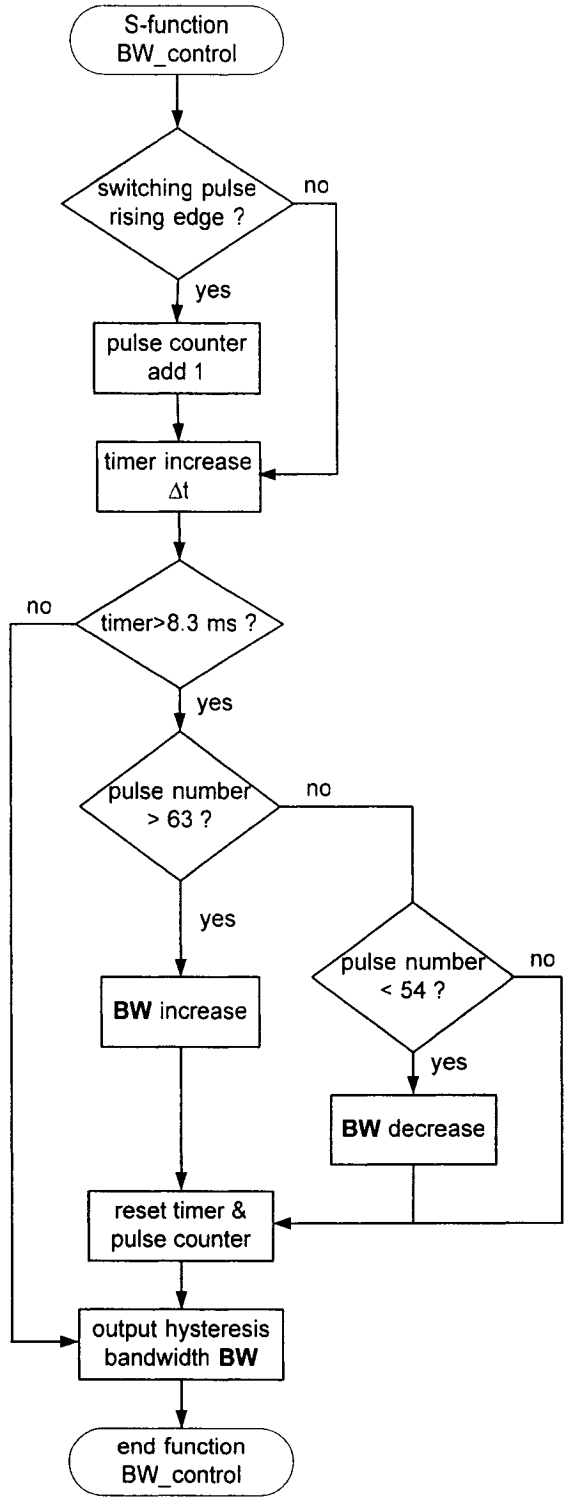


Fig. 4.8. Flowchart for PWM switching frequency control based on dynamic adjustment of the two hysteresis bandwidths.

Besides the limitation of the PWM switching frequency, another important issue in PWM implementation is to introduce a certain blanking time between the upper and lower IGBT power devices of the three converter legs, to prevent possible short through. The following logic is implemented to control the delay-on of IGBT power switches.

$$y(t_n) = x(t_n) * x(t_{n-1}); \tag{4.14}$$

For the PWM waveforms as shown in Fig. 4.9, the computed PWM switching signals in Fig. 4.9 **a)** is regulated to the waveforms of Fig. 4.9 **b)** and **c)** for upper and lower power switches respectively on the same converter leg. It is shown that the switch-on command is delayed by a user-defined time interval, which is tunable according to PWM switching frequency. Whereas the switch-off command is executed immediately without any delay.

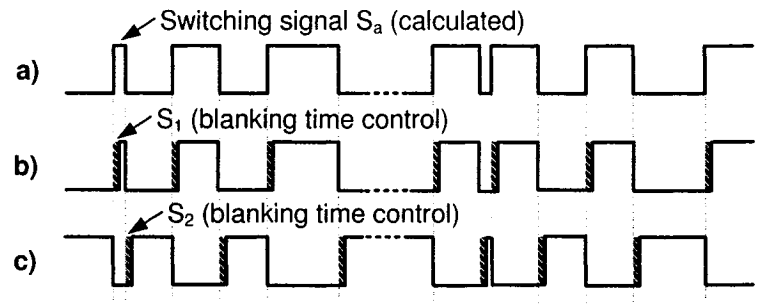


Fig. 4.9. Switching patterns for PWM blanking time control in phase-*a*.

a) Calculated PWM switching command, **b)** upper-switch pulses with PWM blanking time control, **c)** lower-switch pulses with PWM blanking time control.

4.7 Simulation and Experimental Results

A laboratory prototype of the proposed shunt compensator is built at 2 kVA power rating. The nominal amplitude of the three-phase line-to-line voltage is selected at 104 V, and the dc-bus voltage is regulated to 300 V. The shunt-connected var compensator is

coupled to the ac system in parallel to handle the unbalanced and nonlinear loads. The power source supplies the average power portions drawn by the nonlinear load and consumed by the var compensator for switching losses compensation. The var compensator supplies the instantaneous power ripples consumed by the nonlinear load.

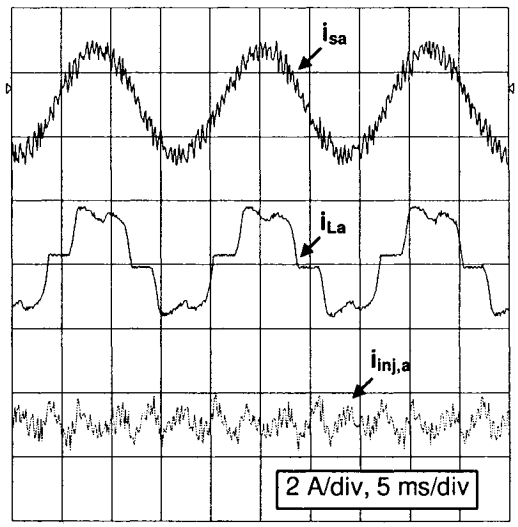
The DSP sampling frequency is much higher than the average PWM switching frequency in the proposed DPC control. For load harmonics compensation, the average switching frequency is 7 kHz, and the DSP sampling frequency is 50 kHz in order to filter out the current harmonics and keep the line current sinusoidal. For load fluctuations compensation, the average switching frequency is 3 kHz, and the DSP sampling frequency is chosen between 30 to 50 kHz in order to track the load power ripples. The reason for the high sampling frequency requirement of the DSP controller comes from the fact that the high performance of the DPC control is dependent on the capability of the DSP controller to react at the exact moment to switch on or off the converter IGBT power devices based on the comparison of instantaneous power terms. A high DSP sampling frequency allows effective reduction of the switching time errors and ensures the var compensator to inject the exact amount of instantaneous power to the ac system.

4.7.1 Nonlinear Load Compensation

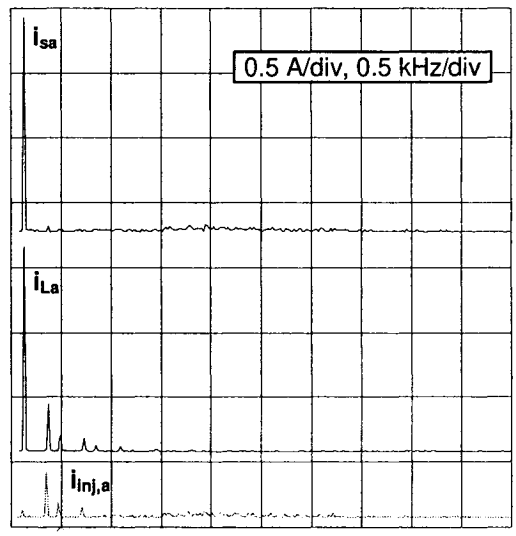
The experimental results are presented in Fig. 4.10 for filtering out the harmonic current caused by a diode-bridge rectifier load. The three-phase line-to-line voltage at the PCC is balanced and of an amplitude of 104 V. The ac-link inductor of the PWM converter is chosen at 3 mH and the dc-bus capacitor is of 500 μf. Fig. 4.10 **a)** shows that the load current is distorted, while the power supply input current remains sinusoidal after compensation, and the var compensator injects the harmonics drawn by the non-linear

load. Fig. 4.10 **b)** shows the spectra of the corresponding currents. The main harmonic contents of the load current include 5^{th}, 7^{th} and 13^{th} components. And the spectrum in bottom indicates that the var compensator injects the corresponding harmonic components. Fig. 4.10 **c)** shows instantaneous power ripples injected by the var compensator. The power ripples include multiple frequency components and the majority of them are 5^{th} and 7^{th} components.

a) Input current (upper), load current (middle), and injected current (lower). x-axis: 5 m/div, y-axis: 2 A/div.



b) Harmonic spectra of input current (upper), load current (middle) and injected current (lower). x-axis: 0.5 kHz/div, y-axis: 0.5 A/div.



c) Injected instantaneous power p (upper) and q (lower), the ripple is around 300 Hz ~ 420 Hz. x-axis: 5 ms/div, y-axis: 150 VA/div.

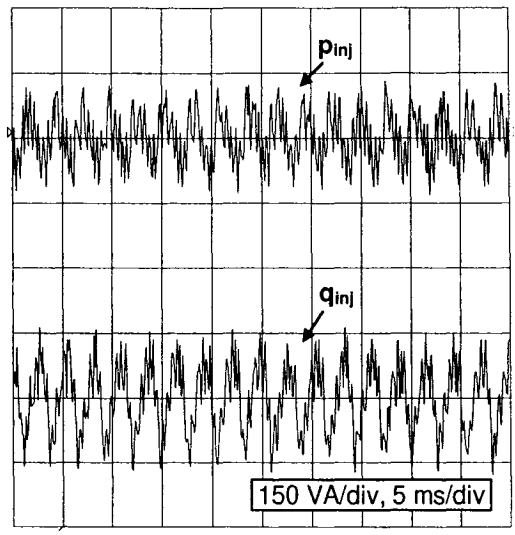
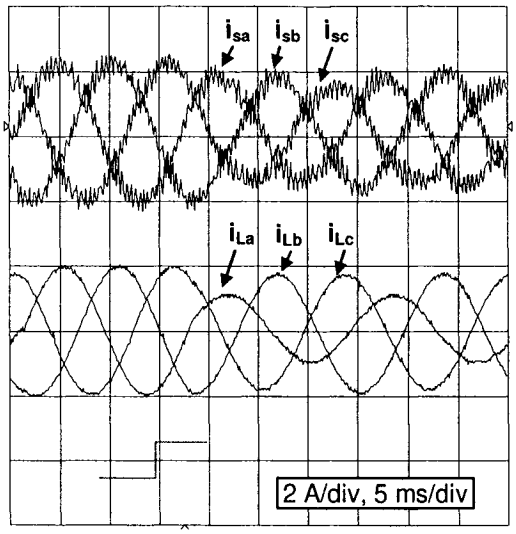


Fig. 4.10. Experimental performance for harmonic current filtering.

4.7.2 Load Fluctuation Compensation

The load fluctuation causes sudden, stochastic line current variation, which may introduce voltage fluctuation at the PCC. The time varying loads include furnaces and welding machines. In order to test the performance of the proposed DPC controller, the experiment of the compensator working with load fluctuation is performed. As initial conditions, the power system is stable, and the three-phase supply voltage at the PCC is balanced and of an amplitude of 104 V line-to-line voltages. The three-phase resistive load is balanced and linear, drawing a current of 0.7 A per phase. Then the load in one phase is suddenly reduced to 50 %, consequently, the total load is unbalanced and reduced. Fig. 4.11 **a)** shows the three-phase load current is unbalanced and reduced, while the three-phase line current is balanced after compensation. Fig. 4.11 **b)** shows that the injected instantaneous power is almost zero when the three-phase system is balanced, and a power ripple of 120 Hz is injected when the load is unbalanced. The settling time for line current compensation is around 7 ms.

a) The three-phase supply current (upper) and load current (lower) with load in phase-*a* reduced to 50 %. x-axis: 5 m/div, y-axis: 2 A/div.



b) The injected instantaneous power p (upper) and q (lower), the ripple is of 120 Hz, x-axis: 5 ms/div and y-axis: 150 VA/div.

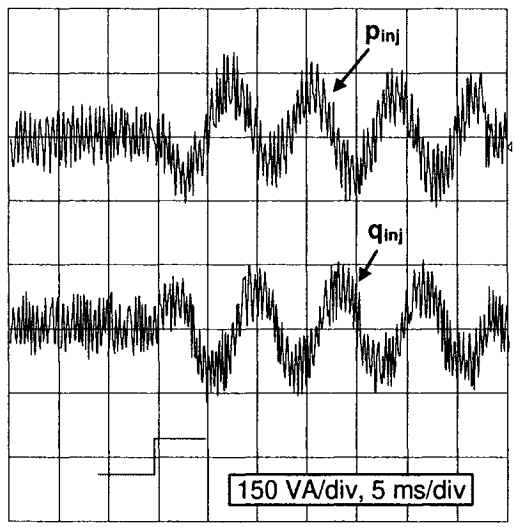


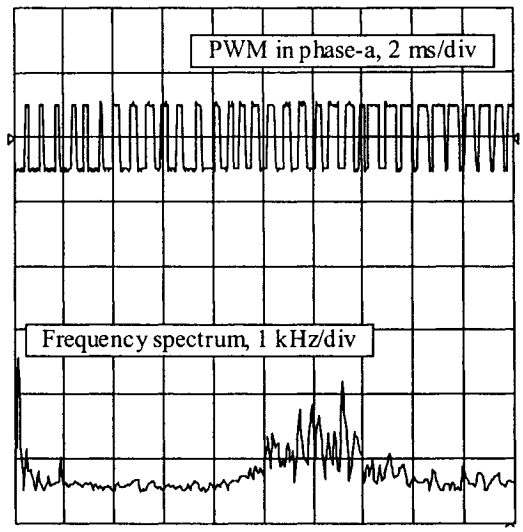
Fig. 4.11. Experimental performance for load fluctuation compensation.

4.7.3 PWM Switching Patterns

From the PWM patterns and the associated harmonic spectra as shown in Fig. 4.12 **a)**, it can be seen that the switching harmonics are distributed in a range from 5.5 to 7 kHz. Therefore, the switching frequency is not fixed, and the individual switching action depends on the output status of the hysteresis comparator. The converter switching frequency would change following the change of the harmonic contents of the load

current as well as the bandwidth of the hysteresis comparator. But the converter switching frequency varies around a certain range when the system is stable. For the specific var compensator investigated in this chapter, the average switching frequency is 7 kHz for nonlinear load compensation, and the average switching frequency is 3 kHz for unbalanced linear load compensation.

a) PWM switching pulses (upper) and harmonic spectrum (lower). The switching frequency is not fixed and distributed in a range from 5.5 ~ 7 kHz.



b) PWM switching pulses in phase-*a* with blanking time control. The switching-on moments are delay by 10 μs with an average switching cycle time of 167 μs (switching frequency of 6 kHz).

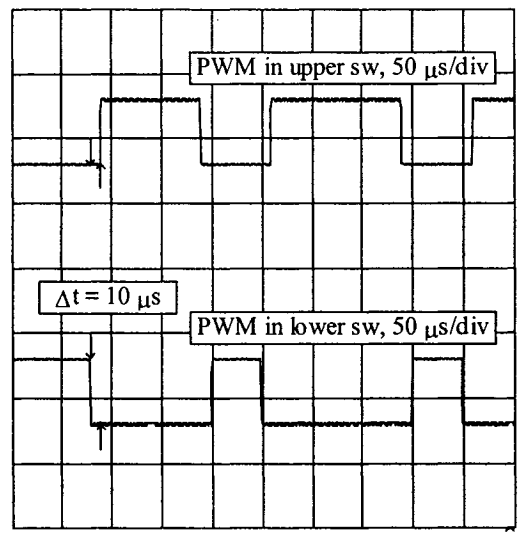


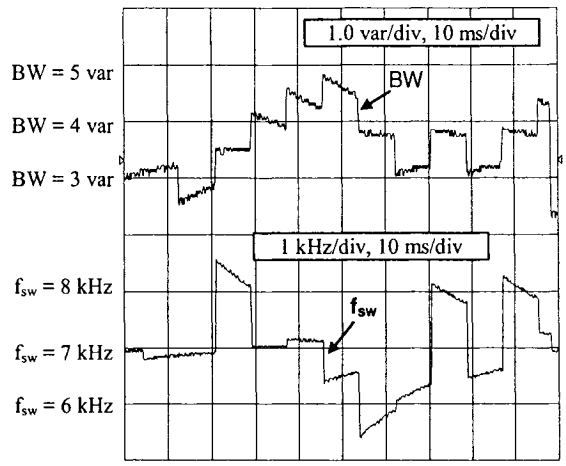
Fig. 4.12. Experimental results of PWM switching patterns with DPC control.

In Fig. 4.12 **b)**, a blanking time is introduced to the PWM gating signals, to prevent short through in the converter legs. Every switch-on action is delayed by 10 μs using external FPGA circuit, to wait for the other switch in the same leg to be fully turned off, based on an average switching cycle time of 167 μs (switching frequency of 6 kHz) in the experiment. Large blanking time causes switching harmonics. Therefore, a small and variable blanking time should be inserted based on the switching frequency.

4.7.4 Regulation of the Average PWM Switching Frequency

In order to control the average IGBT switching frequency, the band windows of the two hysteresis comparators are regulated according to the counted numbers of the switching pulses in every half a cycle time (8.3 ms). Fig. 4.13 **a)** shows the response of the varying switching frequency by regulating the comparator bandwidth. It is seen that the DSP controller reduces the bandwidth gradually when the switching frequency is less than 7 kHz, as a consequence, the switching frequency increases accordingly. On the other hand, the bandwidth is tuned to increase when the switching frequency is higher than 8 kHz, so as to force the switching frequency to decrease. The change of the PWM switching frequency always follows the regulation of the bandwidth. Results show that the switching frequency is controlled in the range from 5.5 to 8.5 kHz by using the variable bandwidth between 2 to 5 var. Fig. 4.13 **b)** lists the average switching frequency as a function of the comparator bandwidth for harmonic current compensation. When the bandwidth is larger than 12 var, the converter switching frequency fluctuates. It's hard to define the average switching frequency under this condition, and large amounts of harmonics are injected into the power system.

a) The variable comparator bandwidth (upper) and the response of the PWM switching frequency (lower).



b) The average switching frequency as a function of the comparator bandwidth.

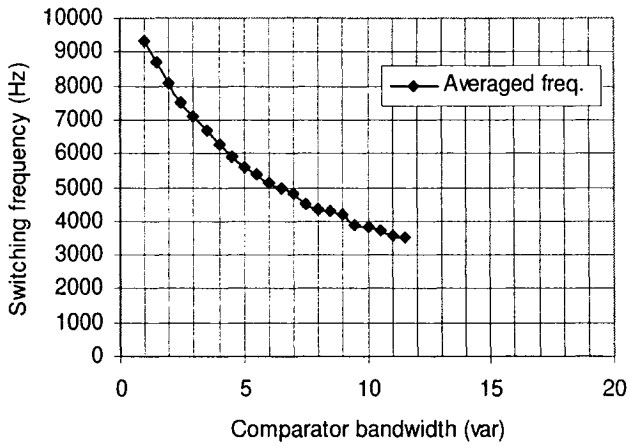


Fig. 4.13. Experimental results for average PWM switching frequency regulation.

4.8 CONCLUSIONS

In this chapter, a direct power control structure has been proposed and implemented for shunt-connected var compensators. The direct power control is extended from the direct torque control of motor drives and significant modifications have been made, including the re-definition of the appropriate power terms and the selection of PWM switching functions. With DPC control, the instantaneous active and reactive power

terms are directly used as control variables and the ac current and the dc-bus voltage control blocks are integrated into a single control loop. Therefore, the multi-loop control structure is avoided in DPC control and the dynamic response is increased. Aimed at practical implementation, the regulation of average PWM switching frequency, PWM blanking time control as well as the high sampling frequency requirement of the DSP controller have also been addressed during the control system design. In addition, since the instantaneous phase information of the PCC voltage has to be sent to the DPC controller in every sampling time interval, an algorithm is proposed to identify the sector in which the voltage vector is currently residing. The proposed method only uses simple algebraic and logical computations in stead of the trigonometric functions, as a result, it is free of approximation errors and saves the processing time of the DSP controller. Simulation and experimental results verify the theoretical analysis.

CHAPTER 5

UNIFIED DEADBEAT CONTROL OF THE COMBINED SERIES-PARALLEL COMPENSATOR

5.1 INTRODUCTION

The combined series-parallel converter topology has been investigated and reported in literatures aiming at power quality control, such as the unified power quality conditioner (UPQC) [37] and the universal active power line conditioner (UPLC) [112]. Both UPQC and UPLC have a similar power circuit structure based on the integration of the series and the parallel power converters that share a single dc link. Usually, the parallel converter is connected downstream of the series converter, and an alternative configuration is also presented in [37], where the parallel converter is connected upstream of the series converter. The proposed system in this chapter shares the similar power circuit structure, but is different in operation modes and control functions compared to the previously reported series-parallel converter systems, in which a unified deadbeat control method is developed to control the two converters combination simultaneously.

It has been noted that the deadbeat control provides very fast transient response, and much research work has been done in recent years, especially oriented to motor drives, UPS and active filter applications. In literature [114], a deadbeat controller for the three-phase PWM converter with an output LC filter is presented based on the synchronously rotating *d-q* frame. The algorithm includes a current minor loop and a voltage control

loop. The *d-q* components are cross-coupled, and two decoupled deadbeat controllers have been developed for the *d* and *q* components respectively. In [115], a disturbance-observer based deadbeat controller is proposed for UPS applications. The pole placement of the state observer and that of the disturbance observer are chosen separately, in which the dynamics of the disturbance observer is faster than that of the state variable observer. This scheme shows advantages in terms of system robustness, in addition, the system model is based on the stationary α–β coordinates and therefore, the state variables are not cross-coupled. In [116], the performance of the deadbeat controller for a three-phase inverter under no load and various load conditions are investigated. In [117], a deadbeat current controller is proposed with an improved line voltage estimation technique for active filter applications. The paper investigated the stability margins of the algorithm with respect to parameter mismatches. In [118], a deadbeat adaptive hysteresis current controller is presented to achieve a fixed PWM switching frequency of the converter. The system is digitally implemented with minimal external analog circuits. In [119], a deadbeat controller for the line current detection type active filter is proposed by using the capacitor voltage as an intermediate, the output current of the active filter is regulated exactly equal to the current reference at the next sampling time instant. In [121], a system model of the series-parallel converters combination is presented and the concept of unified deadbeat control of the combination of the two converters is initiated.

Based on the previous work, this chapter extends the analysis of the problems, originally presented in [121], and proposes significant modifications in operation modes and control functions of the series-parallel converters as well as the relocation of the harmonic LC filter. In [121], the parallel converter regulates the load voltage to be

sinusoidal with nominal amplitude, and the series converter regulates the line current to be sinusoidal. As a result, the dynamics of the parallel converter dominate the performance of combined system. A similar operation mode of the series-parallel converter was also proposed in [113] for single-phase ac systems. In the proposed system of this chapter, the control function of the series converter and that of the parallel converter are reversed. The series converter eliminates supply voltage sags, imbalance and flicker from the load voltage, whereas the parallel converter compensates current harmonics and reactive power produced by the nonlinear load, the dc bus voltage is also regulated by the parallel converter. The dynamics of the series converter dominates the system performance and the advantage of the proposed operation mode comes from the fact that the control system remains stable and robust even in the case of control saturation and loss of deadbeat response.

Generally, the deadbeat controller is sensitive to mismatches of the system model and uncertainties or variations of the model parameters. In addition, the control system has a tendency to become unstable if the dynamic response of the state variable observer and that of the disturbance observer are designed in the same range. Compared to the previous work in [121], the power circuit has been modified in this chapter, in which the location of the harmonic L-C filter is changed from the output of the shunt converter to that of the series converter, and there isn't any observer required in the proposed control scheme. A second-order prediction method is used to estimate the sudden changes of the supply voltage for feed forward compensation of the voltage disturbance. In addition, the discretization time of the state-space system model is selected twice the sampling time of the DSP controller to compensate the computing time delay required for the deadbeat

algorithm computation. Thus the deadbeat controller samples the control variables and executes the control routines twice in one discretization-time period, and the PWM signals are independently decided in the two successive control intervals. As a result, the load voltage is regulated to track the control reference with a delay of a single discretization time period. These theoretical considerations have been verified by means of simulation and experimental tests.

5.2 DESCRIPTION OF THE PROPOSED SYSTEM

The power circuit of the proposed series-parallel compensator is shown in Fig. 5.1. The series-connected converter and the shunt-connected converter share a common dc-link that consists of the energy storage capacitor or backup batteries.

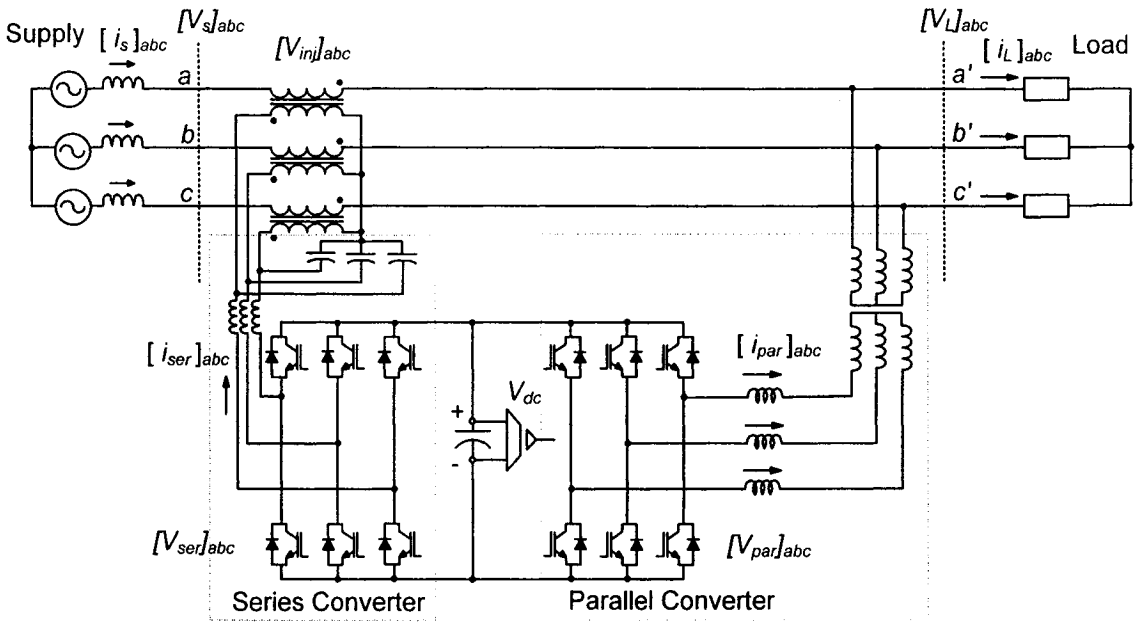


Fig. 5.1. Power circuit of the combined series-parallel compensator.

The series converter eliminates voltage sags, imbalance and flicker from the load terminal voltage. The shunt converter injects harmonics and reactive current to supply the

nonlinear load. It also performs dc link voltage regulation, thus leading to a significant reduction of the size of the dc-bus energy storage capacitor.

Taking one phase as an example, the combined system can be thought conceptually as shown in Fig. 5.2, and the equivalent circuits of the other two phases are identical. The effects of the harmonic LC filter should be carefully considered in control system design, since the dynamic behavior of the control system changes due to the presence of the LC filter. The capacitor component, in fact, is not accounted for in many applications, in which only the voltage drop across the ac-link inductor is considered. But this approach introduces a model mismatch and the consequent errors. In the proposed control system, the influence of the filter capacitor is considered, and the LC filter is properly damped by the controller to avoid possible resonant oscillations, especially during transient states.

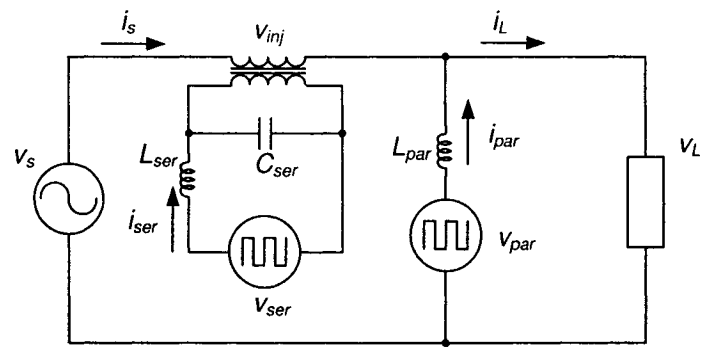


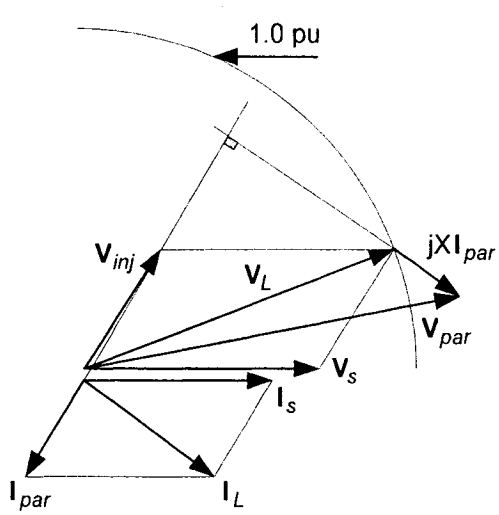
Fig. 5.2. Simplified equivalent circuit in phase *a*.

More than 90% of power quality faults are related to single-line-to-ground voltage sags. The unbalanced three-phase ac system can be decomposed into two balanced components, named positive and negative sequence components, and into a neutral point offset, named zero sequence component in three-phase four-wire configurations. The negative sequence component of the input voltage is isolated from the output by injecting a same amount of voltage component with opposite direction from the series converter

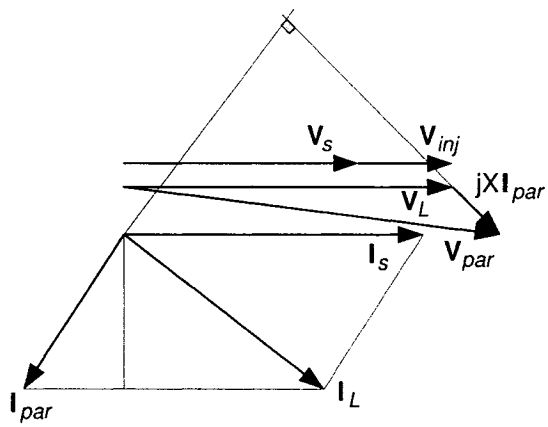
into the power line, in which only reactive power is associated. For the positive sequence component compensation, the phasor diagrams are shown as following. In Fig. 5.3 **a)**, the series converter injects voltages for load voltage support as well as line impedance compensation, and the shunt converter compensates harmonics and reactive power consumed by the load. In Fig. 5.3 **b)**, the series converter injects the minimum amount of voltages, by properly selecting the voltage reference, thus the power rating of the series converter can be reduced. The shunt converter provides reactive power compensation. In Fig. 5.3 **c)**, the series converter seeks to inject the minimum amount of voltages and the shunt converter doesn't provide reactive power compensation, instead, the shunt converter only absorbs a small amount of active current to compensate the switching losses and maintain a stable dc-bus voltage. As a result, the associated power rating requirement is greatly reduced.

It is found that in all of the voltage sag cases, the series converter injects active power to the ac system. The shunt converter absorbs active power from the ac system and passes it to the series converter to maintain a balanced power flow. At the same time, the shunt converter also takes a small amount of active power to compensate the switching losses of the converters.

a) The series converter provides load voltage support and line impedance compensation. The shunt converter provides reactive power compensation.



b) The series converter seeks minimum voltage injection. The shunt converter provides reactive power compensation.



c) The series converter seeks minimum voltage injection and the shunt converter doesn't provide reactive power compensation. This scheme imposes the minimum power rating requirement.

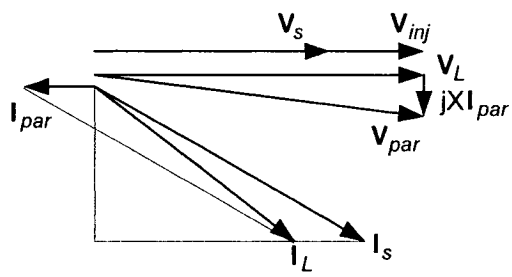


Fig. 5.3. Phasor diagrams of the combined series-parallel compensator.

The power flows of the series-parallel converters are shown in Fig. 5.4. The ac system supplies all of the real power consumed by the load, and some of the real power is circulating between the series and shunt converters. The shunt converter absorbs the harmonics produced by the nonlinear load, and provides reactive power compensation if

it has spare power injection capability. The series converter absorbs reactive power if the injected voltage isn't in phase with the input current.

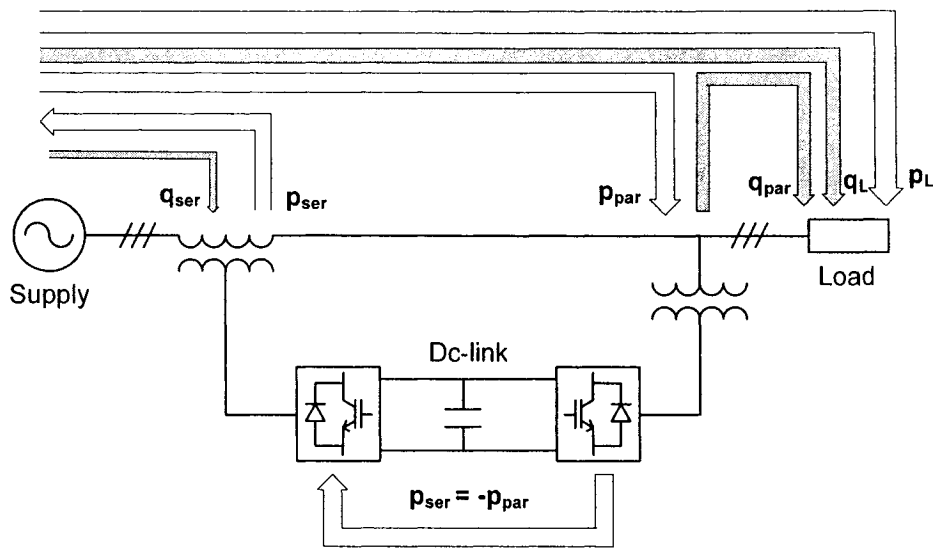


Fig. 5.4. Active and reactive power flow of the combined series-parallel compensator for voltage sag compensation.

5.3 MODELING OF THE COMBINED SERIES-PARALLEL COMPENSATOR

The series-parallel converters combination is treated as a single multi-input and multi-output system, which regulates the line current and load voltage simultaneously. In order to derive the system equation, the involved state variables include the load voltage $[V_L]_{abc}$, supply voltage $[V_s]_{abc}$, series converter output voltage $[V_{ser}]_{abc}$, shunt converter output voltage $[V_{par}]_{abc}$, power supply line current $[i_s]_{abc}$, series converter output current $[i_{ser}]_{abc}$, shunt converter output current $[i_{par}]_{abc}$ and dc-bus voltage V_{dc}. The series injected voltage $[V_{inj}]_{abc}$ is related to the capacitor voltage of the LC filter based on the turns ratio γ_n of the voltage matching transformer. By applying the Kirchhoff's current and voltage laws, the following system equations are obtained,

$$
\begin{aligned}
-\frac{C_{ser}}{\gamma_n}\cdot\frac{d}{dt}[V_L]_{abc} &= [i_{ser}]_{abc} + \gamma_n\cdot[i_s]_{abc} - \frac{C_{ser}}{\gamma_n}\cdot\frac{d}{dt}[V_s]_{abc} \\
L_{ser}\cdot\frac{d}{dt}[i_{ser}]_{abc} &= [V_{ser}]_{abc} + \frac{1}{\gamma_n}\cdot[V_L]_{abc} - \frac{1}{\gamma_n}\cdot[V_s]_{abc} \\
L_{par}\cdot\frac{d}{dt}[i_{par}]_{abc} &= [V_{par}]_{abc} - [V_L]_{abc}
\end{aligned}
\tag{5.1}
$$

5.3.1 State Space Model in Three-Phase ac System

Selecting the proper state variables, the model of the combined series-parallel compensator is expressed by the following standard state-space format,

$$
\dot{\mathbf{x}}_{abc} = \mathbf{A}_1\cdot\mathbf{x}_{abc} + \mathbf{B}_1\cdot\mathbf{u}_{abc} \tag{5.2}
$$

where $\mathbf{A}_1 = \begin{bmatrix} \mathbf{0} & -\frac{\gamma_n}{C_{ser}}\cdot\mathbf{I}_3 & \mathbf{0} \\ \frac{1}{\gamma_n\cdot L_{ser}}\cdot\mathbf{I}_3 & \mathbf{0} & \mathbf{0} \\ -\frac{1}{L_{par}}\cdot\mathbf{I}_3 & \mathbf{0} & \mathbf{0} \end{bmatrix}$,

$$
\mathbf{B}_1 = \begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{I}_3 & \mathbf{0} & -\frac{\gamma_n^2}{C_{ser}}\cdot\mathbf{I}_3 \\ \frac{1}{L_{ser}}\cdot\mathbf{I}_3 & \mathbf{0} & \mathbf{0} & -\frac{1}{\gamma_n\cdot L_{ser}}\cdot\mathbf{I}_3 & \mathbf{0} \\ \mathbf{0} & \frac{1}{L_{par}}\cdot\mathbf{I}_3 & \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}.
$$

The state variables are defined as,

$$
\mathbf{x}_{abc} = [V_{L-a} \quad V_{L-b} \quad V_{L-c} \quad i_{ser-a} \quad i_{ser-b} \quad i_{ser-c} \quad i_{par-a} \quad i_{par-b} \quad i_{par-c}]^T
$$

$$
\begin{aligned}
\mathbf{u}_{abc} = [&V_{ser-a} \quad V_{ser-b} \quad V_{ser-c} \quad V_{par-a} \quad V_{par-b} \quad V_{par-c} \\
&\dot{V}_{s-a} \quad \dot{V}_{s-b} \quad \dot{V}_{s-c} \quad V_{s-a} \quad V_{s-b} \quad V_{s-c} \quad i_{s-a} \quad i_{s-b} \quad i_{s-c}]^T
\end{aligned}
$$

and $\mathbf{I}_3$ is a (3×3) unit matrix.

5.3.2 Decoupled Two Single-Phase Systems by *abc*-$\alpha\beta$ Transformation

The three-phase system model of the combined series-parallel compensator can be converted into two decoupled single phase systems in α–β coordinates [115]. Performing the three-to-two phase transformation, and assuming a three-phase three-wire system, the above three-phase system model (5.2) is transformed to:

$$\dot{\mathbf{x}}_{\alpha\beta} = \mathbf{A}_2 \cdot \mathbf{x}_{\alpha\beta} + \mathbf{B}_2 \cdot \mathbf{u}_{\alpha\beta} \tag{5.3}$$

where $\mathbf{A}_2 = \begin{bmatrix} \mathbf{A}_{21} & \mathbf{0} \\ \mathbf{0} & \mathbf{A}_{22} \end{bmatrix}$ and $\mathbf{B}_2 = \begin{bmatrix} \mathbf{B}_{21} & \mathbf{0} \\ \mathbf{0} & \mathbf{B}_{22} \end{bmatrix}$.

$$\mathbf{A}_{21} = \mathbf{A}_{22} = \begin{bmatrix} 0 & -\dfrac{\gamma_n}{C_{ser}} & 0 \\ \dfrac{1}{\gamma_n \cdot L_{ser}} & 0 & 0 \\ -\dfrac{1}{L_{par}} & 0 & 0 \end{bmatrix},$$

$$\mathbf{B}_{21} = \mathbf{B}_{22} = \begin{bmatrix} 0 & 0 & 1 & 0 & -\dfrac{\gamma_n^2}{C_{ser}} \\ \dfrac{1}{L_{ser}} & 0 & 0 & -\dfrac{1}{\gamma_n \cdot L_{ser}} & 0 \\ 0 & \dfrac{1}{L_{par}} & 0 & 0 & 0 \end{bmatrix}.$$

The state variables are decoupled as,

$$\mathbf{x}_{\alpha\beta} = \begin{bmatrix} V_{L-\alpha} & i_{ser-\alpha} & i_{par-\alpha} & V_{L-\beta} & i_{ser-\beta} & i_{par-\beta} \end{bmatrix}^T$$

and

$$\mathbf{u}_{\alpha\beta} = [V_{ser-\alpha} \quad V_{par-\alpha} \quad \dot{V}_{s-\alpha} \quad V_{s-\alpha} \quad i_{s-\alpha} \quad V_{ser-\beta} \quad V_{par-\beta} \quad \dot{V}_{s-\beta} \quad V_{s-\beta} \quad i_{s-\beta}]^T.$$

The equation in (5.3) indicates that the two-phase system consists of two orthogonally decoupled systems in α-axis and β-axis respectively, the control of each of the two

systems can be performed as treating a single-phase system. The resulting two single-phase equivalent systems are identical first-order systems.

5.4 UNIFIED DEADBEAT CONTROL ALGORITHM

The deadbeat response can be obtained for first-order systems, where the output lags the control reference by one discretization time interval. In this section, the single-phase system model is used to develop the two identical deadbeat controllers for α-axis and β-axis systems respectively.

5.4.1 Discrete-Time State Space Equations

Based on (5.3), the state-space equations describing the two identical equivalent single-phase systems are written as,

$$\begin{aligned} \dot{\mathbf{x}}_{1p} &= \mathbf{A}_{1p} \cdot \mathbf{x}_{1p} + \mathbf{B}_{1p} \cdot \mathbf{u}_{1p} \\ \mathbf{y}_{1p} &= \mathbf{C}_{1p} \cdot \mathbf{x}_{1p} \end{aligned} \tag{5.4}$$

where $\mathbf{A}_{1p} = \mathbf{A}_{21} = \mathbf{A}_{22}$, $\mathbf{B}_{1p} = \mathbf{B}_{21} = \mathbf{B}_{22}$ and $\mathbf{C}_{1p} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}$.

The state variables include $\mathbf{x}_{1p} = \begin{bmatrix} V_L & i_{ser} & i_{par} \end{bmatrix}^T$, $\mathbf{u}_{1p} = \begin{bmatrix} V_{ser} & V_{par} & \dot{V}_s & V_s & i_s \end{bmatrix}^T$ and $\mathbf{y}_{1p} = \begin{bmatrix} V_L & i_{par} \end{bmatrix}^T$. These variables represent the single-phase (α-axis or β-axis) components of the corresponding three phase voltages and currents.

Selecting a small discretization time interval T_d, the state variables are assumed to stay unchanged at the sampled values during each discretization time period. Incorporating a ZOH conversion, the approximate discrete-time system model becomes:

$$\begin{aligned}\mathbf{x}_{1p}(k+1) &= \mathbf{F}\cdot\mathbf{x}_{1p}(k)+\mathbf{H}\cdot\mathbf{u}_{1p}(k)\\ \mathbf{y}_{1p}(k+1) &= \mathbf{C}\cdot\mathbf{x}_{1p}(k+1)\end{aligned} \tag{5.5}$$

where $\mathbf{F}=e^{\mathbf{A}_{1p}\cdot T_d}$, $\mathbf{H}=\mathbf{A}_{1p}^{-1}\cdot\left(e^{\mathbf{A}_{1p}\cdot T_d}-\mathbf{I}_3\right)\cdot\mathbf{B}_{1p}$, $\mathbf{C}=\mathbf{C}_{1p}$.

The matrix calculation is performed using MATLAB tools. For the proposed system, the results are obtained as,

$$\mathbf{F}=\begin{bmatrix} f_{11} & f_{12} & 0\\ f_{21} & f_{22} & 0\\ f_{31} & f_{32} & 1\end{bmatrix},\ \mathbf{H}=\begin{bmatrix} h_{11} & 0 & h_{13} & h_{14} & h_{15}\\ h_{21} & 0 & 0 & h_{24} & h_{25}\\ h_{31} & h_{32} & 0 & h_{34} & h_{35}\end{bmatrix} \tag{5.6}$$

5.4.2 The Deadbeat Control Law

Since two identical deadbeat controllers are used for the α-axis and β-axis systems respectively, the subscript of ***1p*** is removed in the following sections for the sake of simplicity, where **X**(k) will be used to replace $\mathbf{X_{1p}}$(k), and **u**(k) to replace $\mathbf{u_{1p}}$(k).

In addition, the vector **u**(k) is separated into two parts. The first part includes the control inputs of the two converters (the demanded synthesis voltages), and defined as $\mathbf{m}(k)=\left[V_{ser}(k)\quad V_{par}(k)\right]^T$. The second part includes the system disturbances, defined as $\xi(k)=[\dot{V}_s(k)\quad V_s(k)\quad i_s(k)]^T$. Therefore, the system model (5.5) can be rewritten as,

$$\begin{aligned}\mathbf{x}(k+1) &= \mathbf{F}\cdot\mathbf{x}(k)+\mathbf{L}\cdot\mathbf{m}(k)+\mathbf{N}\cdot\xi(k)\\ \mathbf{y}(k+1) &= \mathbf{C}\cdot\mathbf{x}(k+1)\end{aligned} \tag{5.7}$$

where $\mathbf{L}=\begin{bmatrix} h_{11} & 0\\ h_{21} & 0\\ h_{31} & h_{32}\end{bmatrix}$ and $\mathbf{N}=\begin{bmatrix} h_{13} & h_{14} & h_{15}\\ 0 & h_{24} & h_{25}\\ 0 & h_{34} & h_{35}\end{bmatrix}$.

Inverting the system model in (5.7), the control inputs of the combined series-parallel compensator are given in matrix format as follows,

$$\mathbf{C}\cdot\mathbf{L}\cdot\mathbf{m}(k)=\mathbf{y}(k+1)-\mathbf{C}\cdot\mathbf{F}\cdot\mathbf{x}(k)-\mathbf{C}\cdot\mathbf{N}\cdot\xi(k) \tag{5.8}$$

where $\mathbf{y}(k+1)$ represents the control system output, including the expected load voltage and shunt injected current of the next discretization time instant.

Based on (5.8), the control inputs of the two converters are derived as,

$$\begin{aligned}\mathbf{m}(k)&=(\mathbf{C}\cdot\mathbf{L})^{-1}\cdot\{\mathbf{y}(k+1)-\mathbf{C}\cdot\mathbf{F}\cdot\mathbf{x}(k)-\mathbf{C}\cdot\mathbf{N}\cdot\xi(k)\}\\&=\mathbf{Q}\cdot\mathbf{y}(k+1)+\mathbf{S}\cdot\mathbf{x}(k)+\mathbf{T}\cdot\xi(k)\end{aligned} \tag{5.9}$$

where $\mathbf{Q}=\begin{bmatrix}q_{11} & 0\\ q_{21} & q_{22}\end{bmatrix}$, $\mathbf{S}=\begin{bmatrix}s_{11} & s_{12} & 0\\ s_{21} & s_{22} & s_{23}\end{bmatrix}$ and $\mathbf{T}=\begin{bmatrix}t_{11} & t_{12} & t_{13}\\ 0 & 0 & t_{23}\end{bmatrix}$.

The equation (5.9) indicates that, replacing the system outputs (load voltage and injected current) at the next discretization time instant with control references, the control inputs are expressed as a linear combination of the control references, the sensed state variables as well as the disturbances. The deadbeat controller applies the control inputs to power converters through pulse-width modulation, and drives the system outputs to track the control references after one discretization time T_d delay. The block diagram of the proposed control system is shown in Fig. 5.5, and the state space model of the proposed deadbeat controller is illustrated in Fig. 5.6.

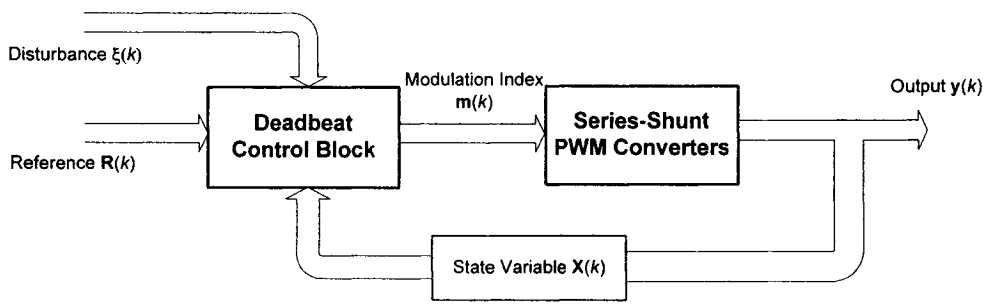


Fig. 5.5. Block diagram of the proposed deadbeat control system.

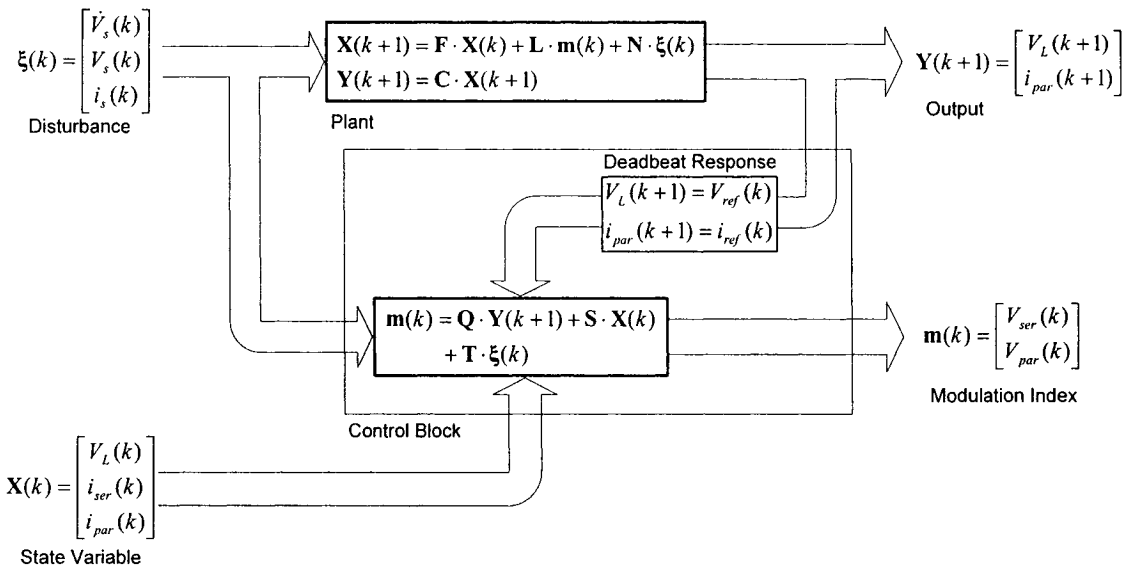


Fig. 5.6. State-space representation of the proposed control algorithm.

In real-time implementation, it is preferred to expend the computation equations to element format. For the series converter, the following demanded output voltage is derived for PWM modulation:

$$V_{ser}(k) = q_{11} \cdot V_{ref}(k) + s_{11} \cdot V_L(k) + s_{12} \cdot i_{ser}(k) + t_{11} \cdot \dot{V}_s(k) + t_{12} \cdot V_s(k) + t_{13} \cdot i_s(k) \tag{5.10}$$

For the parallel converter, the following demanded output voltage is derived for PWM modulation:

$$V_{par}(k) = q_{21} \cdot V_{ref}(k) + q_{22} \cdot i_{ref}(k) + s_{21} \cdot V_L(k) + s_{22} \cdot i_{ser}(k) + s_{23} \cdot i_{par}(k) + t_{23} \cdot i_s(k) \tag{5.11}$$

It is shown that the control of the series converter does not look up to the output of the parallel converter, while the control of the parallel converter is influenced by that of the series converter. In addition, the state variable regarding the dc-bus voltage is associated with the PWM modulation of both the series and the parallel converters.

5.4.3 Generation of Control References

For the proposed series-parallel compensator, the deadbeat controller tries to correct any deviation of the control outputs from the control references at the next discretization-time instant. The realization of the deadbeat response depends on a number of conditions such as the control is not saturated, the demanded converter output voltage is synthesizable through PWM modulation, and the availability of the reference signals.

The control references are generated as shown in Fig. 5.7. A Phase Locked Loop is used to keep the load voltage synchronized continuously. There are three options: synchronizing with the pre-fault supply voltage, the phase-*a* of the post-fault voltage, or the positive sequence of the post-fault voltage. The proposed control system synchronizes the voltage reference with the positive sequence of the post-fault voltage, since it leads to the smallest voltage injection [129]. The current reference of the shunt converter aims at supplying the harmonics and reactive power drawn by the nonlinear load. The shunt converter also absorbs a small amount of active power to compensate the switching losses of the PWM converters and maintain a stable dc-bus voltage.

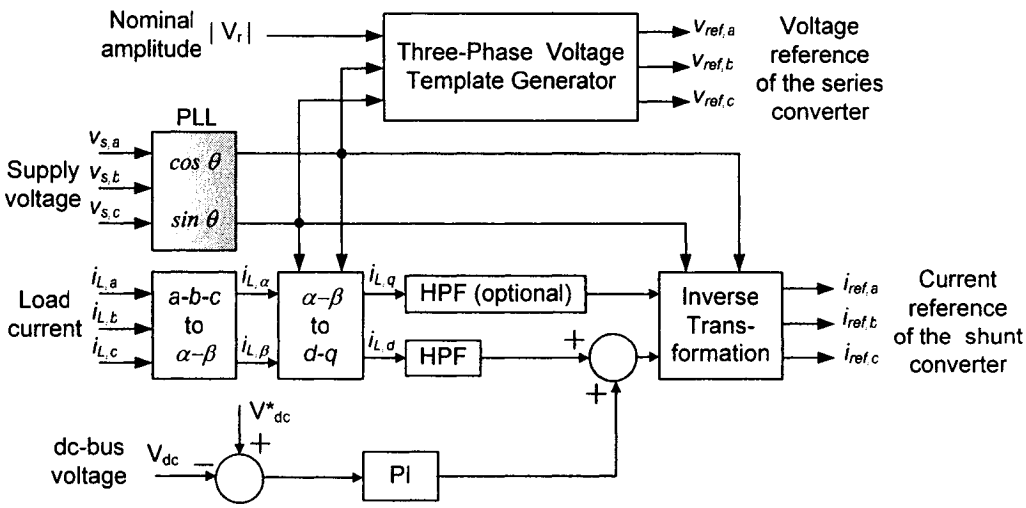


Fig. 5.7. Block diagram of the control reference generation system.

5.5 COMPENSATION OF ALGORITHM COMPUTING TIME DELAY

The inherent delay caused by the calculation time of the controller is a source of error in deadbeat control schemes. If the state variables are measured at the k-th time instant, since a certain amount of computing time is needed for the calculation of (5.10) and (5.11), it is short of time to implement the control law at the k-th time period.

In order to compensate the computing time delay, one of the commonly used solutions is to use observers, and estimate the values of state variables and disturbances at the k-th time instant based on their previous values at the (k-1)-th time instant [115]. Fig. 5.8 shows the timing chart of this strategy, where $\hat{X}(k)$ is the estimated state variables for the k-th time instant, and U(k) is the commanded modulation index for the k-th time instant. The pole placement of the state variable observer and that of the disturbance observer should be chosen separately to reduce detection noises.

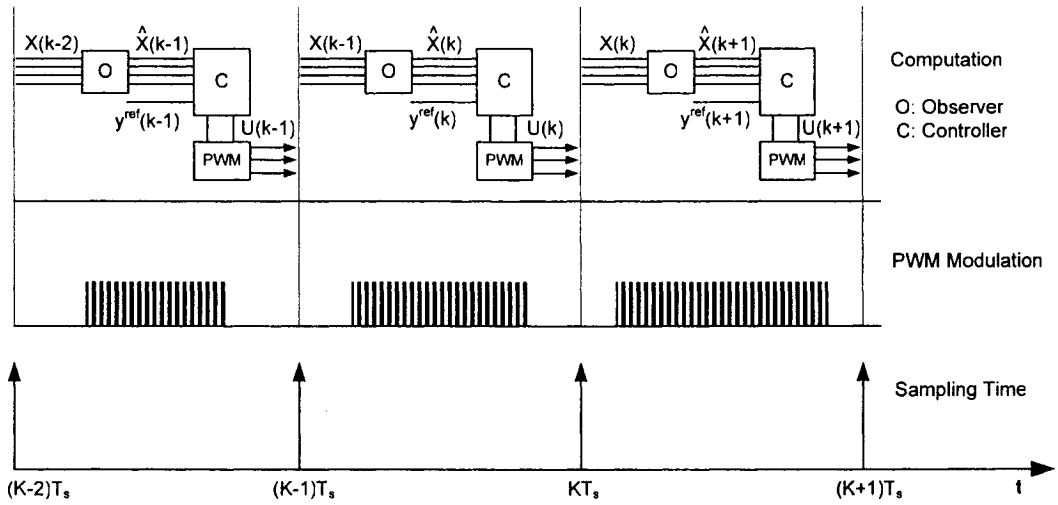


Fig. 5.8. Timing chart of the control scheme based on state variable observers.

An alternative method is proposed in this section to compensate the computing time delay [114]. There isn't any of the state variable observer and the disturbance observer used in the proposed system, instead, the discretization time T_d of the state space system model is selected twice the sampling time T_s of the DSP controller, in addition, a second order prediction method is used to estimate the supply voltages for feed forward compensation of any disturbances. The deadbeat controller samples the control variables and executes the control routines twice in one discretization-time step, and the PWM signals are independently decided in the two successive control intervals.

Fig. 5.9 shows the operation principles for the compensation of algorithm computing time delay. A single discretization time step $kT_d - (k+1)T_d$ is divided into two sampling time intervals as $nT_s - (n+1)T_s$ and $(n+1)T_s - (n+2)T_s$. The calculated converter output voltage for the time period $nT_s - (n+1)T_s$ is obtained as $V_{conv}(n)$ based on the state variables measured at the sampling time instant $(n-1)T_s$, and the corresponding modulation index $U(n-1)$ is sent to PWM modulator to drive the power converter. Then, the desired converter output voltage for the time period $(n+1)T_s - (n+2)T_s$ is computed as $\hat{V}_{conv}(n)$ based on the state variables measured at the sampling time instant nT_s. As shown by the dashed line (ka – kb) in Fig. 5.9, the area S_{ka} is the shortage of the converter voltage during the last sampling time period, and the shortage is compensated during the next sampling time period by an adjusted converter voltage $V_{conv}(n+1)$, which compensates S_{ka} by S_{kb}. As a consequence, the load voltage is regulated to track the control reference in a delay of a discretization time T_d period.

$$V_{conv}(n+1) = 2 \cdot \hat{V}_{conv}(n) - V_{conv}(n) \tag{5.12}$$

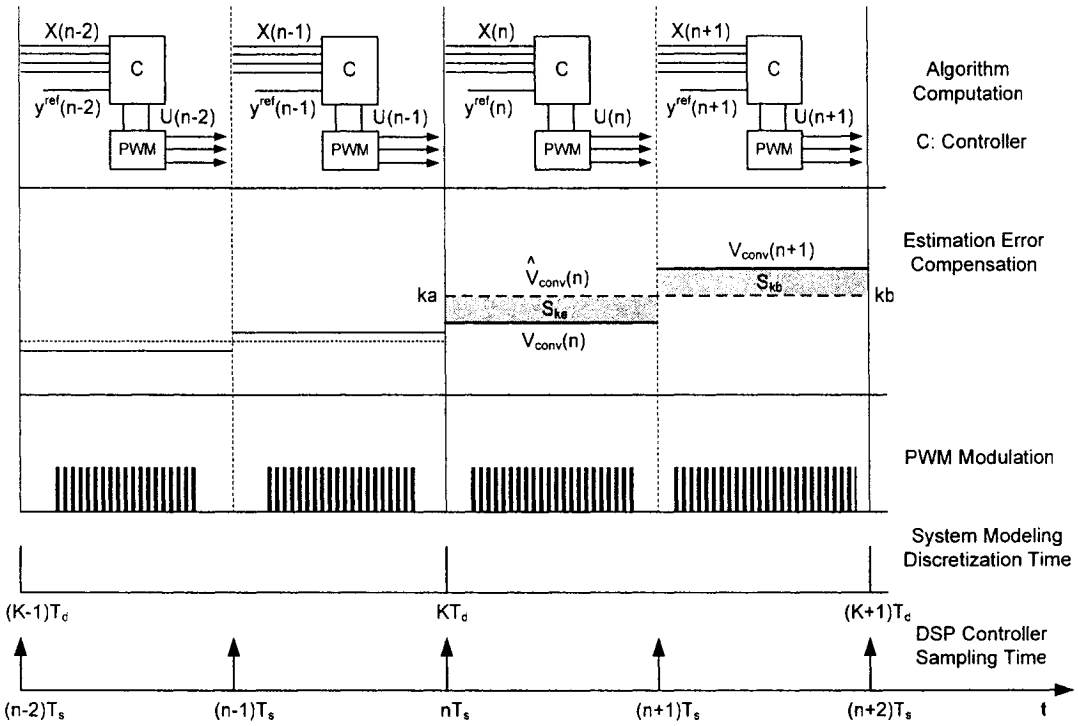


Fig. 5.9. Timing chart of the proposed method for compensation of algorithm computing time delay.

The variation of the three-phase supply voltage is predicted for feed forward compensation of the voltage disturbance. A second order prediction method [114] is presented in the proposed system. Referring to Fig. 5.10, the supply voltage at the sampling time instant nT_s is of a measured value of $V_s(n)$, while the predicted value of $\hat{V}_s(n)$ is used in the deadbeat controller to replace $V_s(n)$. The voltage estimation at the time instant nT_s is based on the last three measurements of the supply voltage that are $V_s(n)$, $V_s(n-1)$ and $V_s(n-2)$ respectively. The prediction calculation is written as,

$$\hat{V}_s(n) = 6 \cdot V_s(n) - 8 \cdot V_s(n-1) + 3 \cdot V_s(n-2) \tag{5.13}$$

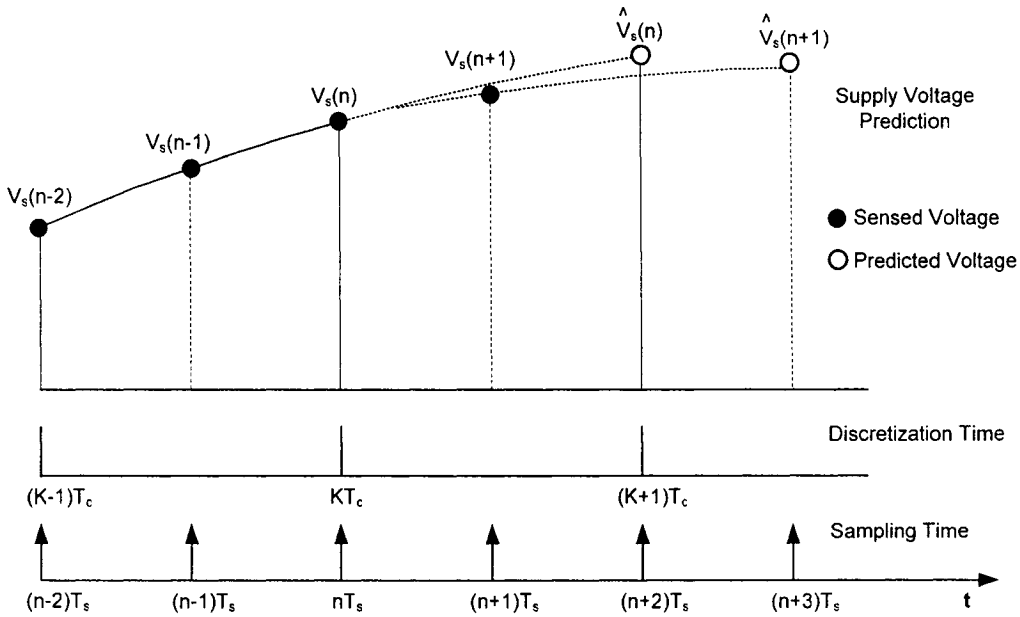


Fig. 5.10. The second order prediction method for supply voltage estimation.

By using the supply voltage prediction scheme, it is shown that the series-parallel compensator is capable of injecting an appropriate amount of voltage to the ac system following a dynamic voltage sag to effectively compensate the disturbance caused by a supply voltage fault.

5.6 IMPLEMENTATION OF SYMMETRICAL SPACE VECTOR MODULATION

The PWM power converter is used to synthesize the output voltages commanded by the deadbeat controller. It is desirable to keep the switching frequency fixed, which simplifies the design of the harmonic LC filter. The symmetrical space vector modulation strategy is well suited for the digital implementation, and is adopted in the proposed system.

The objective of space vector modulation is to synthesize a commanded voltage vector $\mathbf{V}_{conv}$ by a combination of switching patterns chosen from the basic space vectors (V_1 to V_8) [132]. The synthesis looks to the sector i in α–β plane where the voltage vector $\mathbf{V}_{conv}$ is currently residing, and the converter output voltage is synthesized as a linear combination of two adjacent vectors (V_i and V_{i+1}) and one of the zero vectors (V_7 or V_8). The on-duration of the switching vectors are computed as,

$$\begin{aligned} t_i &= \frac{2 \cdot T_{sw}}{\sqrt{3}} \cdot \frac{V_{conv}}{V_{dc}} \cdot \sin(60° - \theta_{conv}) \\ t_{i+1} &= \frac{2 \cdot T_{sw}}{\sqrt{3}} \cdot \frac{V_{conv}}{V_{dc}} \cdot \sin(\theta_{conv}) \\ t_0 &= T_{sw} - t_i - t_{i+1} \end{aligned} \tag{5.14}$$

where T_{sw} is the PWM switching cycle time, V_{dc} is the amplitude of the dc-bus voltage, V_{conv} is the amplitude of the demanded converter output voltage vector and θ_{conv} is the angle between the vector $\mathbf{V}_{conv}$ and the closest clockwise space vector (V_1 to V_6).

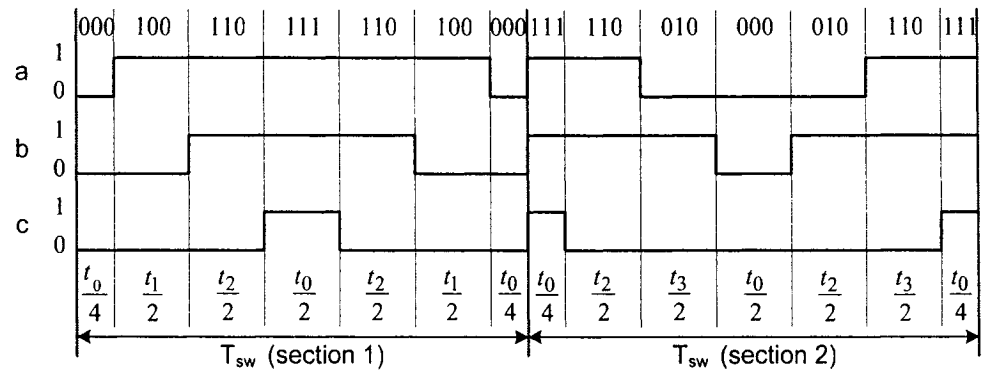
Symmetrical space vector PWM method is implemented essentially by separating each switching pulse into two parts symmetrically, as shown in Fig. 5.11 for PWM patterns in section 1 to 6 respectively. The purpose of the symmetrical pulse division is to reduce the THD_v of the synthesized output voltage without increasing the switching frequency of the converter.

The states of the gating patterns are provided by a two-dimensional look-up table, as shown in Table 5.1. The column value represents the time intervals, which are divided to $T_0/4$, $T_i/2$, $T_{i+1}/2$, $T_0/2$, $T_{i+1}/2$, $T_i/2$ and $T_0/4$ in every switching cycle. The row number represents the sector number in which the commanded voltage vector is currently residing. The look-up table is stored in the memory of the PWM modulator.

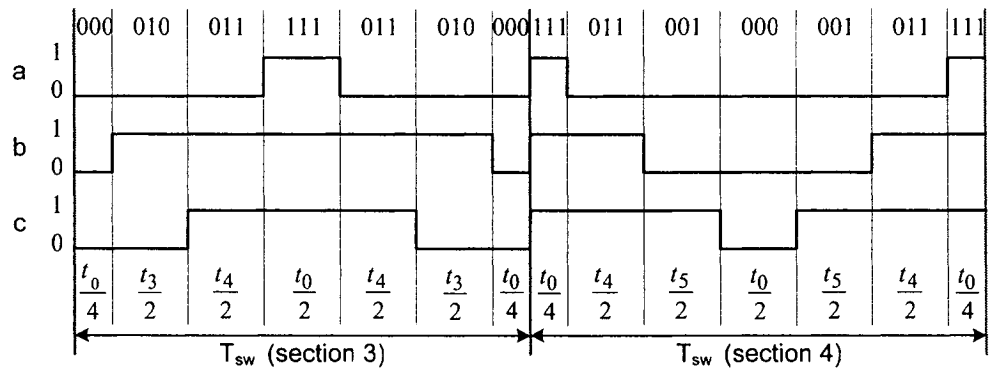
Table 5.1. Switching Patterns of the Symmetrical Space Vector Modulation

	Time	$T_0/4$	$T_i/2$	$T_{i+1}/2$	$T_0/2$	$T_{i+1}/2$	$T_i/2$	$T_0/4$
Sector	1	(0,0,0)	(1,0,0)	(1,1,0)	(1,1,1)	(1,1,0)	(1,0,0)	(0,0,0)
	2	(1,1,1)	(1,1,0)	(0,1,0)	(0,0,0)	(0,1,0)	(1,1,0)	(1,1,1)
	3	(0,0,0)	(0,1,0)	(0,1,1)	(1,1,1)	(0,1,1)	(0,1,0)	(0,0,0)
	4	(1,1,1)	(0,1,1)	(0,0,1)	(0,0,0)	(0,0,1)	(0,1,1)	(1,1,1)
	5	(0,0,0)	(0,0,1)	(1,0,1)	(1,1,1)	(1,0,1)	(0,0,1)	(0,0,0)
	6	(1,1,1)	(1,0,1)	(1,0,0)	(0,0,0)	(1,0,0)	(1,0,1)	(1,1,1)

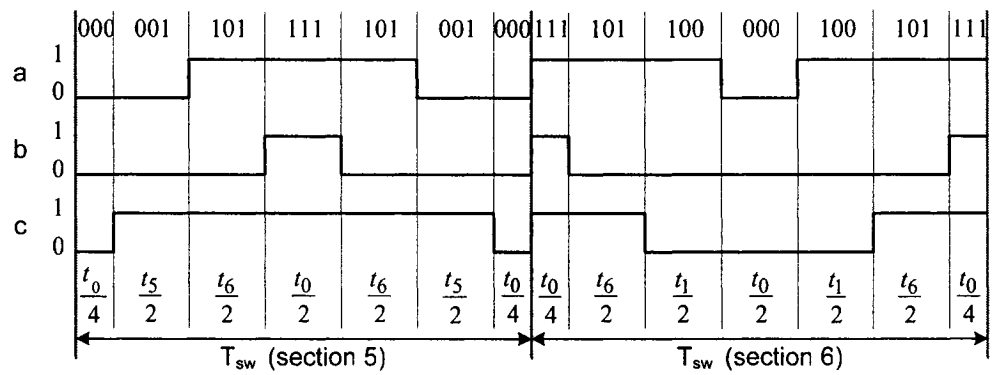
By observing Fig. 5.11, it is found that there is a total of six switch commutations at every switching cycle period T_{sw}, and the switch commutation numbers are the same from section 1 to section 6. But the actual switching action of each of the six power switches (T_{a+}, T_{a-}, T_{b+}, T_{b-}, T_{c+} and T_{c-}) remains only once. Considering the facts that a larger number of switch commutations helps to reduce the THD_v of the converter output voltage and a smaller number of switching actions of the IGBT power switch leads to a lower switching loss, it can be concluded that the proposed symmetrical space vector modulation is capable of accomplishing a low THD_v of the converter output voltage and maintaining the same amount of switching losses as other PWM methods based on triangular carrier PWM modulation.



a) PWM patterns in section 1 and 2.



b) PWM patterns in section 3 and 4.



c) PWM patterns in section 5 and 6.

Fig. 5.11. PWM patterns of the six sections in α–β plane with the proposed symmetrical space vector modulation.

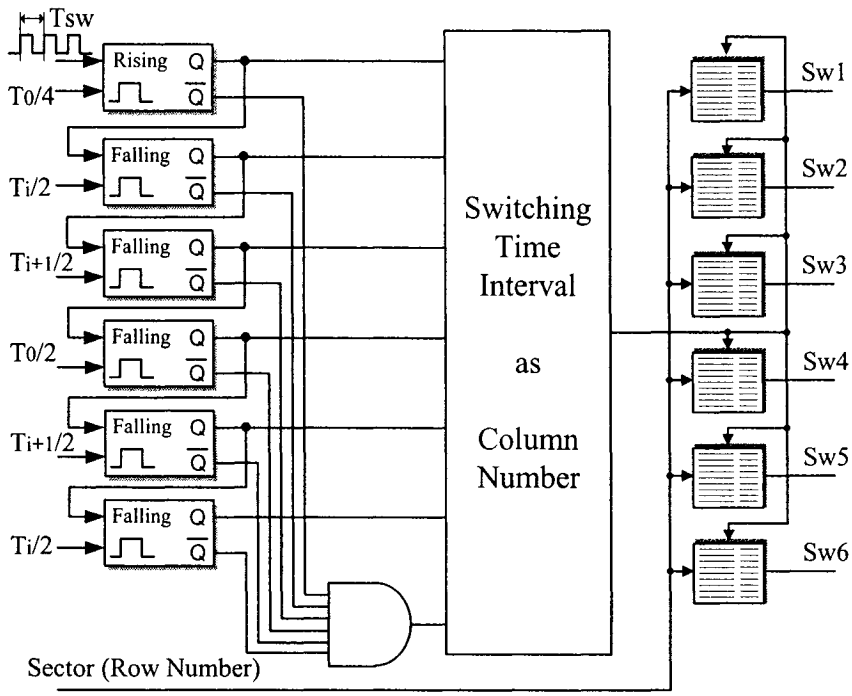


Fig. 5.12. The proposed PWM pattern generator based on monostable multi-vibrators.

The key component to implement the proposed symmetrical space vector modulation is the six monostable multi-vibrators, as shown in Fig. 5.12, which function as software timers to control the width of the switching pulses. The sampling frequency of the software timer determines the resolution of the gating signals, and has great impact on the quality of the PWM output waveforms, especially in high switching frequency applications. There are two input ports in each monostable unit. At input 1 (upper), the rising or falling edge signal triggers the monostable. At input 2 (lower), the input data determines the on-time pulse width. The multi-vibrators can be implemented by the DSP controller, or the FPGA circuit [132]. As a result, a series of pulses, with dynamically specified pulse-width, are generated at the output of the PWM modulator.

5.7 SIMULATION AND EXPERIMENTAL RESULTS

A laboratory prototype of the combined series-parallel compensator is built to verify the proposed control algorithms. Table 5.2 lists the system parameters for simulation and experimental tests. The discretization time for system modeling is selected at 200 μs, which is twice of the sampling time of the DSP controller, set as 100 μs, in order to compensate the time delay caused by the proposed deadbeat algorithm computation.

The parameter design of the switching harmonic LC filter is extended from [39][134]. It is assumed that all of the switching harmonic currents pass through the filter inductor and capacitor. By setting a 10% total harmonic distortion factor for the inductor current THD_i and the capacitor voltage THD_v of the series converter, and selecting a break frequency of the LC filter that is about ten times lower than that of the PWM switching frequency, the values of the filter inductor and capacitor are determined. For the proposed system, the PWM switching frequency is 6 kHz and the break frequency of the LC filter is chosen at 411 Hz. The parameters of the filter are $L_f = 3$ mH and $C_f = 50$ μf without the use of the damping resistor.

The design of the dc-bus capacitor is based on the previous work [75][127]. The dc-bus capacitor is calculated by equalizing the instantaneous input power to the instantaneous output power of the static compensator, in which the energy fluctuation magnitude of the capacitor is a function of the size of the capacitor, the dc-bus voltage and the dc-bus voltage variation across the capacitor. By selecting a 2% dc-bus voltage regulation ratio, the size of the capacitor is load dependent, and the designed capacitor value of 1800 μf satisfies the dc-bus voltage regulation ratio requirement in a 2 kVA power range.

Based on the designed parameters of the series-parallel compensator, the coefficients of equations (5.10) and (5.11) are obtained and two identical deadbeat controllers are used to compute the demanded output voltages of the series-parallel converters for the α and β components respectively. The outputs of the two controllers are then transformed into three-phase voltages through *αβ-abc* transformation, and sent to the corresponding PWM modulators of the two converters. After the simplification, the deadbeat control equations are derived as,

$$V_{ser,n}(k) = -7.35 \cdot V_{ref,n}(k) + 6.39 \cdot V_{L,n}(k) - 29.33 \cdot i_{ser,n}(k) + 0.001 \cdot \dot{V}_{s,n}(k) + 0.96 \cdot V_{s,n}(k) - 30.6 \cdot i_{s,n}(k)$$

$$V_{par,n}(k) = 0.34 \cdot V_{ref,n}(k) + 15 \cdot i_{ref,n}(k) + 0.66 \cdot V_{L,n}(k) - 0.7 \cdot i_{ser,n}(k) - 15 \cdot i_{par,n}(k) - 0.73 \cdot i_{s,n}(k)$$

where n represents the α and β components respectively.

Table 5.2. Parameters of the Combined Series-Parallel Compensator

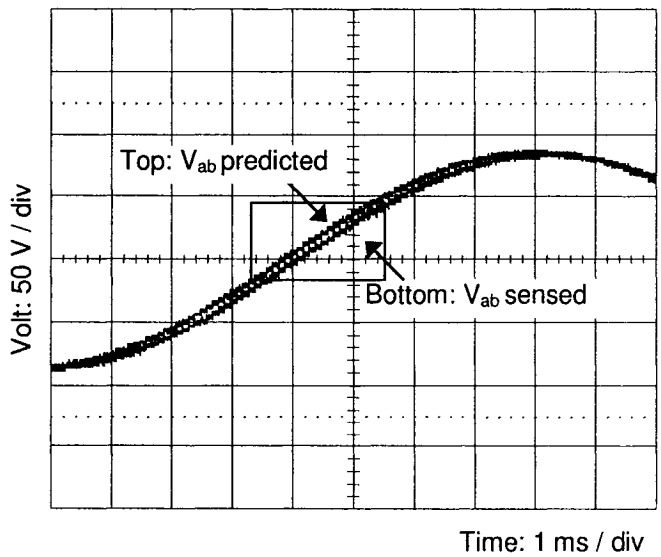
L_{ser}	: Filter inductance of the series converter	3.0 (mH)
C_{ser}	: Filter capacitance of the series converter	50 (μf)
L_{par}	: Inductance of the parallel converter	3.0 (mH)
γ_n	: Turns ratio of series coupling transformer	96/92
C_{dc}	: Dc-bus capacitor	1800 (μf)
V_{ref}	: Reference peak phase voltage	85 (V)
V_{dc}	: Dc-bus voltage	190 (V)
T_s	: Sampling time	100 (μs)
T_d	: Discretization time	200 (μs)
f_{sw}	: Switching frequency	6 (kHz)

The proposed series-parallel compensator is designed at 2 kVA power rating, and the nominal amplitude of the three-phase line-to-line voltage is selected at 60 V. A number of tests have been performed to verify the performance of the unified deadbeat controller.

The control algorithm is implemented through extensive use of available MATLAB toolboxes and simulated in the MATLAB/SIMULINK environment. The same algorithm is then downloaded to the DSP set-up consisting of the MATLAB Real Time Workshop (RTW) and the dSPACE DS1103 PPC controller board with the sampling frequency of the DSP controller set at 10 kHz. The power circuit of the series-parallel compensator is also modeled as state-space matrixes for real-time simulation. Simulation and experimental results are obtained to verify the theoretical considerations.

5.7.1 Prediction of Supply Voltages

Fig. 5.13 shows the performance for supply voltage estimation with the proposed second order prediction method. The results indicate that the predicted voltage equals to the sensed voltage in advance of two sampling time intervals. By using the predicted supply voltage in the deadbeat controller, it helps to compensate the supply voltage disturbances.



a) Waveforms of the predicted supply voltage (upper) and the sensed voltage (lower).

b) The relationship between the predicted voltage and the sensed voltage.

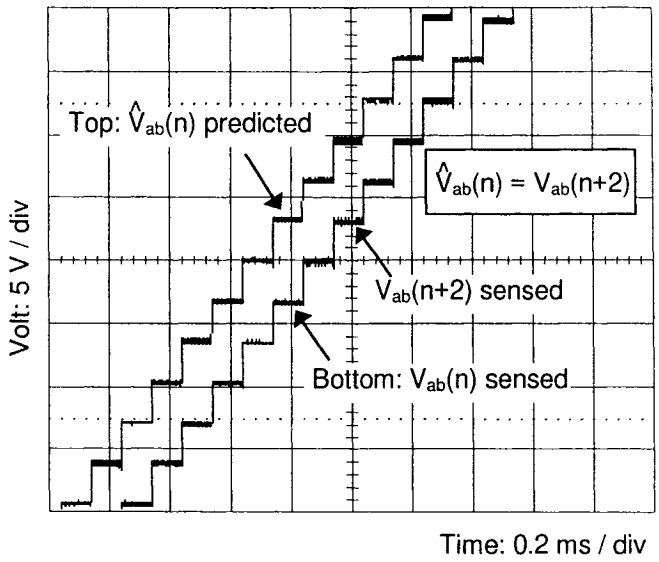


Fig. 5.13. Experimental results of the predicted voltage and the sensed voltage.

5.7.2 Compensation of Algorithm Computing Time Delay

Fig. 5.14 illustrates the mechanism of the deadbeat controller for compensation of the algorithm computing time delay. As explained in Fig. 5.9, the discretization time of the system model is selected twice of the sampling time of the DSP controller. In every discretization time period, the converter modulation index calculated at the second sampling time instant is regulated to compensate the shortage of the converter output voltage during the first sampling time period.

The converter modulation index with computing time delay compensation (V_{conv}) and without compensation ($\hat{V}_{conv}$).

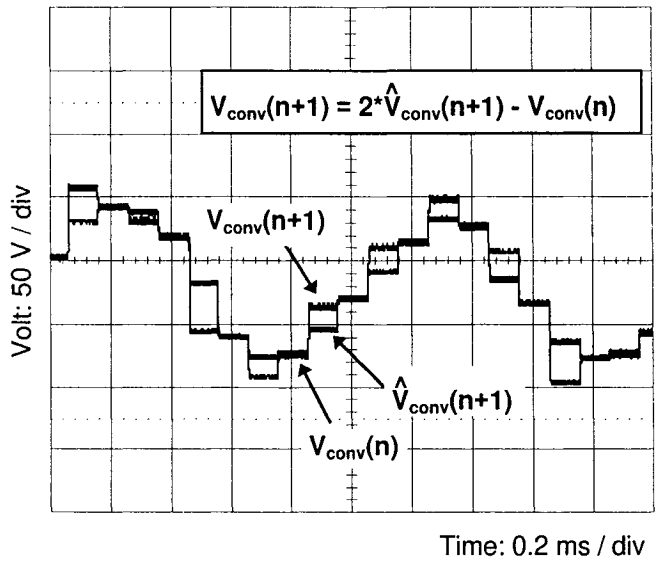
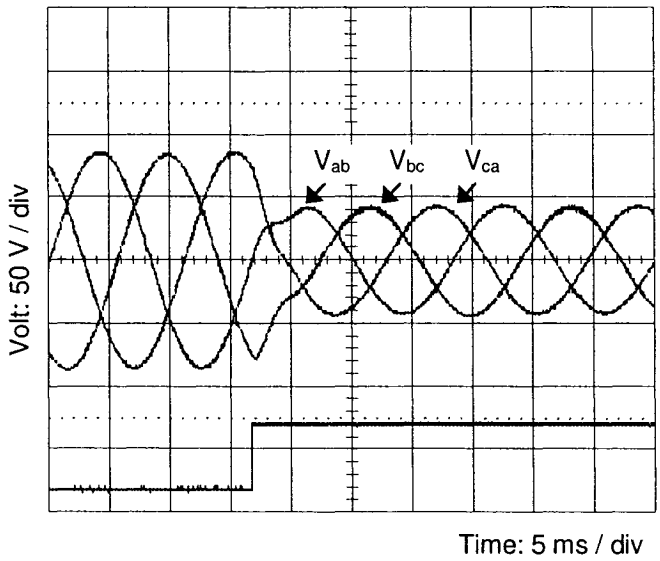


Fig. 5.14. Experimental results for compensation of the algorithm computing time delay.

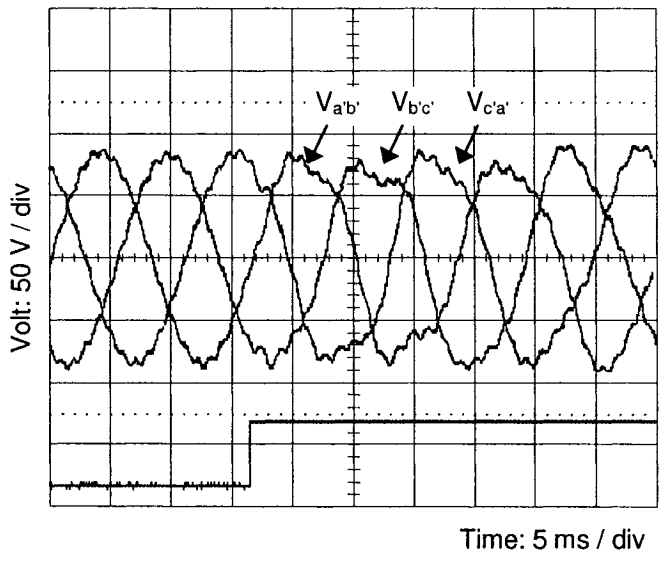
5.7.3 Compensation of a Symmetrical Voltage Fault

In Fig. 5.15, the performance of the proposed deadbeat controller is recorded for compensating a symmetrical three-phase voltage fault. Fig. 5.15 **a)** shows the faulted three-phase supply voltage with a 50% symmetrical voltage sag, Fig. 5.15 **b)** records the three-phase load voltage in transient state when the voltage fault is detected, and Fig. 5.15 **c)** indicates that the three-phase load voltage is regulated to the nominal amplitude in steady state. Fig. 5.15 **d)** gives the injected voltage of the series converter for voltage fault compensation. Fig. 5.15 **e)** shows the absorbed current of the shunt converter after the voltage fault. The shunt converter absorbs a certain amount of active power from the ac system and passes them to the series converter through the dc-link. Then the series converter feed back the active power into the ac system during series voltage injection.

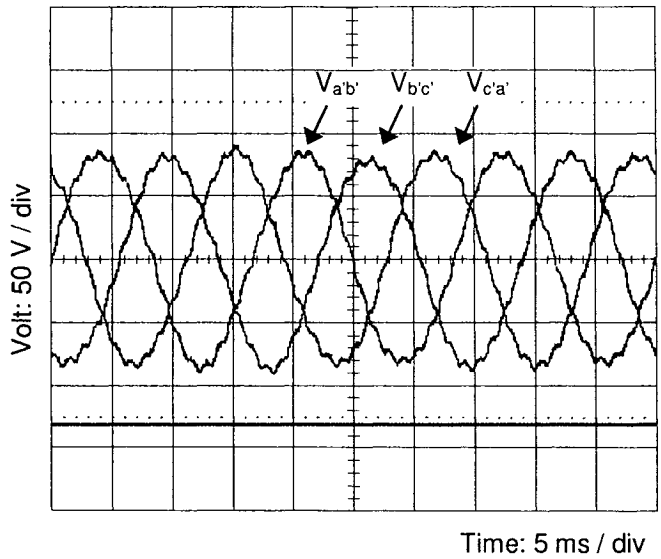
a) Supply voltage with a 50% symmetrical three-phase voltage fault.



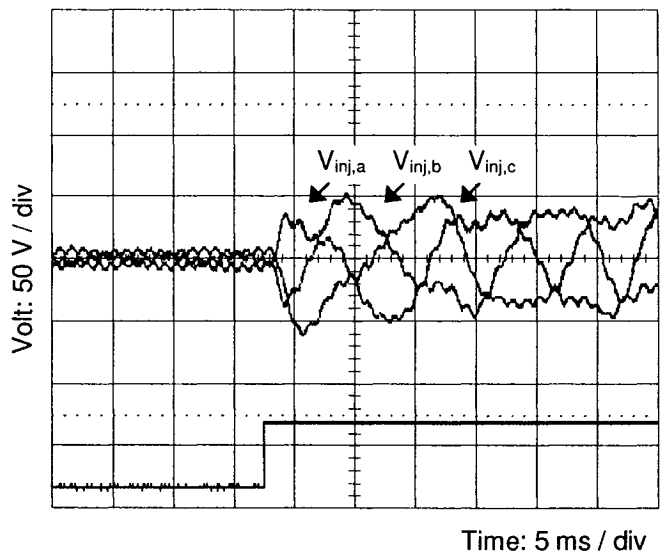
b) Load voltage in transients.



c) Load voltage in steady state.



d) Series converter injected voltage.



e) Shunt converter absorbed current with the voltage fault.

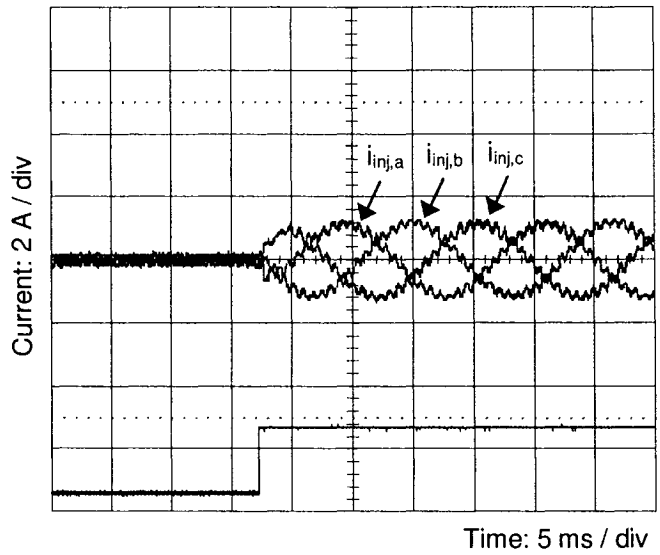
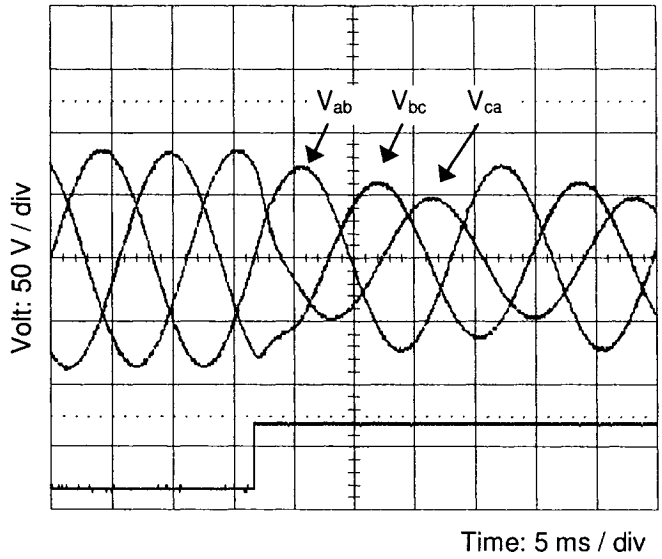


Fig. 5.15. Simulation performance for compensation of a 50% three-phase symmetrical voltage fault.

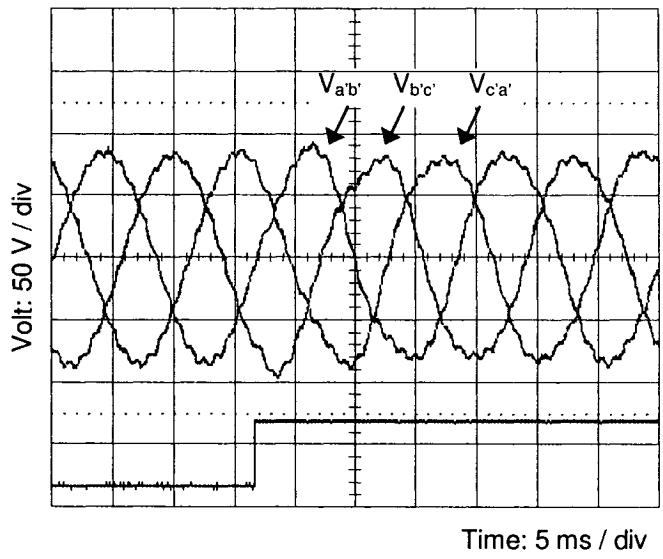
5.7.4 Compensation of a Non-Symmetrical Voltage Fault

The three-phase unbalanced voltage fault accounts for more than 90% of power interruptions encountered in industrial power systems. The performance of the proposed series-parallel compensator is tested for compensation of a non-symmetrical voltage sag with the three phase line voltages dropping to 80%, 67% and 53% of the nominal amplitude respectively. Fig. 5.16 **a)** shows the faulted supply voltage, Fig. 5.16 **b)** indicates that the regulated load voltage is of nominal amplitude after compensation, and Fig. 5.16 **c)** shows the injected voltage of the series converter for the voltage fault compensation.

a) Supply voltage with the three phase line voltages dropping to 80%, 67% and 53% of the nominal amplitude.



b) Load voltage after compensation.



c) Series converter injected voltage.

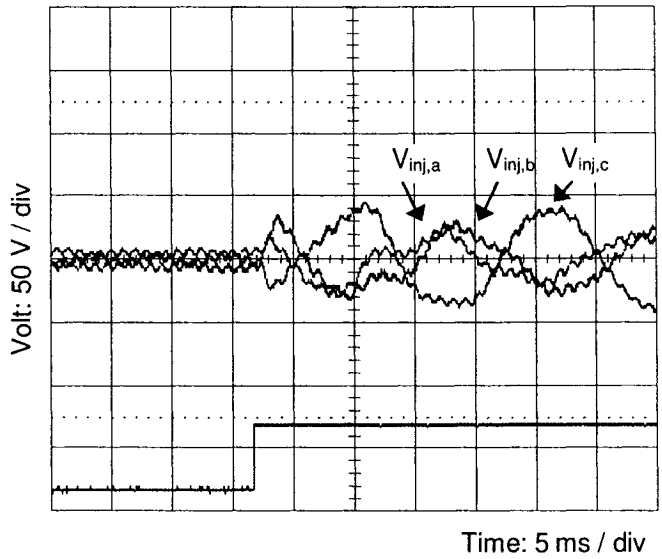


Fig. 5.16. Simulation performance for compensation of a three-phase non-symmetrical voltage fault.

5.7.5 Input and Output Currents of the Compensator

In Fig. 5.17, the input voltage drops from 1.0 pu (60 V) to 0.8 pu (48 V) with a three-phase symmetrical voltage fault, and the load voltage is compensated to 1.0 pu (60 V). As a result, the amplitude of the input current (top trace) is larger than that of the output current (bottom trace) under the voltage fault condition. This verifies the input-output current relationship illustrated by vector diagrams in Fig. 5.3. Since the active power of the input side and that of the output side are of the same quantities while the amplitude of the supply voltage is less than that of the compensated load voltage during a voltage sag.

Fig. 5.18 compares the sinusoidal line current with the distorted load current when the series-parallel compensator is feeding a three-phase nonlinear load (a diode-bridge rectifier). The result verifies that the shunt converter compensates the load current harmonics produced by the nonlinear load, as illustrated in Fig. 5.4.

The input current (upper) and the load current (lower) waveforms.

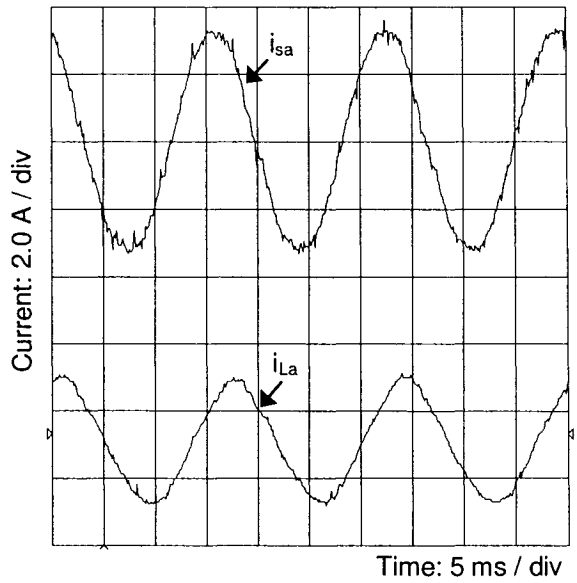


Fig. 5.17. Experimental results of the input current and the load current with a 20% three-phase symmetrical supply voltage fault.

The input current (top) and the load current (bottom) waveforms with a diode-bridge rectifier load.

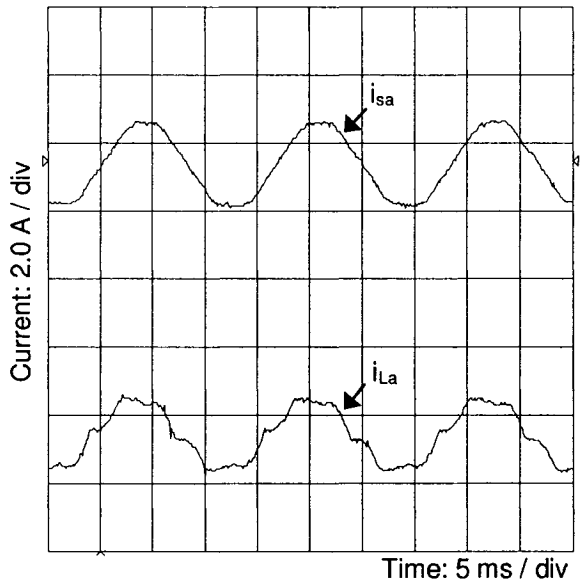


Fig. 5.18. Experimental results of the input current and the load current with a diode-bridge rectifier load.

5.8 CONCLUSIONS

This chapter proposes a unified deadbeat control strategy for the combined series-parallel compensator. It exploits the unified control of the two converters combination, by modeling the series-parallel converters as a single multi-input and multi-output system, and develops two identical deadbeat controllers for the two decoupled single-phase equivalent systems in α- and β-axis respectively. In addition, the computing time delay caused by the control algorithm calculation, an inherent source of error in deadbeat control, is also compensated by the proposed control strategy, in which the discretization time of the system model is selected twice the sampling time of the deadbeat controller. Therefore, the deadbeat controller samples the control variables and executes the control routines twice in a discretization-time step, and the PWM signals are independently decided in the two successive control intervals.

Compared to the commonly used control methods based on individual control of the series-parallel converters, the proposed unified control structure treats the two converters as a single unit, which leads to an accurate system model and a simpler control structure. On the other hand, the proposed deadbeat control algorithm provides a fast dynamic response, in which the compensated load voltage tracks the control reference with a delay of one discretization time period. Simulation and experimental results verify the theoretical considerations.

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 SUMMARY

Control and modulating techniques of static series and shunt compensators for power quality enhancement in industrial power systems are investigated in this thesis. Specifically, the following aspects are studied:

(i) Two power quality compensator topologies based on the four-switch voltage source converter are proposed, which include a dynamic voltage restorer for series compensation, and an active power filter for shunt compensation. The power circuit configurations and control algorithms based on the four-switch converter are modified from their six-switch counterparts to reflect the fact that the third phase comes directly from the midpoint of the split-capacitor bank and the corresponding voltage and current are uncontrollable. In addition, a practical digital control strategy is proposed and implemented for harmonic current compensation, the proposed control method uses the supply current reaction paradigm to replace the commonly used load current sensing scheme, which simply forces the supply current to be sinusoidal and doesn't sense and extract the load harmonic current.

(ii) The control issues of the static series compensator are investigated to reduce the critical response time for dynamic voltage sag compensation. The steady-state compensation-capability curves are derived, and three control reference generation schemes are proposed and compared to each other. A state feedback control strategy in

closed-loop control fashion and insensitive to the types of voltage faults presented in the power network, is proposed. The proposed control system design is based on the same system state-space model as that used in multi-loop PI control structure, but it removes the inner current control loop included in the multi-loop PI control, instead, the injected current and its derivative are used as control variables to reflect the load changes. In addition, a software based current observer is designed to estimate the current and its derivative at the same time.

(iii) The instantaneous active and reactive power terms are reformulated for the implementation of direct power control. In addition, specific switching functions are derived systematically based on instantaneous power flow control. Since the phase information of the PCC voltage is used in the proposed DPC control, an algorithm is proposed to identify the sector where the voltage vector is currently located. The proposed algorithm only involves simple algebraic and logical computations, and avoids intensive trigonometric functions as well as the consequent approximation errors. Furthermore, the DPC controller adjusts dynamically the bandwidths of the two hysteresis comparators and limits the PWM switching frequency in extreme noisy cases. The proposed DPC control has been tested for load harmonics filtering and load fluctuation compensation respectively.

(iv) A unified deadbeat control algorithm for the combined series-parallel compensator is proposed. It models the two converters as a single multi-input and multi-output system, and transforms the three-phase ac system into two decoupled single-phase systems through abc-$\alpha\beta$ coordinates transformation. Two identical deadbeat controllers are implemented for the two first-order equivalent systems respectively. The control

algorithm is accomplished through matrix computation. In order to compensate the algorithm computing time delay caused by the DSP controller, the discretization time of the system model is selected twice the sampling time of the digital controller. The deadbeat controller samples the control variables and executes the control routines twice in a discretization-time step, and the PWM signals are independently decided in the two successive control intervals. In addition, a second-order prediction method is used to estimate sudden changes of the supply voltage for feed forward compensation. The system equations are programmed in a way to reduce the computation time and are downloaded to the dSPACE DS1103 controller board for real-time implementation.

6.2 CONCLUSIONS

Laboratory prototypes of the 2 kVA range have been implemented to verify the feasibility of the proposed power quality compensators and their control schemes. Based on the simulation and experimental results, the following conclusions have been reached:

(i) Since there are only two degrees of freedom available for control in a three-phase three-wire ac system, the performance has not been degraded for the power quality compensator based on four-switch voltage source converter structure. The main drawback comes from the requirement of two times as high as the dc-bus voltage, compared to its six-switch VSI counterpart. Due to the asymmetrical circuit structure of four-switch converters, they are more sensitive to dc-bus voltage variations. The current control is preferred to be per-phase based for active filters using the four-switch converter, where phase-*a* and phase-*b* currents are sensed and regulated independently.

This leads to the blocking of the influence of dc-bus voltage unbalance between the split dc-link capacitors.

(ii) Dynamic performance is a critical consideration for static series compensators, since many industrial loads such as electric drives and manufacturing processes are sensitive to power interruptions as short as a few milliseconds. The multi-loop PI control structure has difficulties meeting the fast voltage compensation requirement due to the dynamic separation of the two cascaded control loops. On the other hand, the open-loop feed-forward control produces poorly damped response with the presence of the LC filter, and introduces errors in steady state. Simulation and experimental tests demonstrate that the proposed state feedback control is a better solution for dynamic voltage sag compensation, which leads to the reduction of the dynamic response time compared to the other control schemes, and near zero steady state compensation errors.

(iii) The proposed direct power control of the shunt-connected var compensator provides a simple and robust control structure that directly uses power terms as control variables and integrates control and modulation functions into one loop. Compared to the multi-loop PI control structure, the proposed DPC control has removed the cascaded control loops, and the separately implemented PWM modulator. Compared to DPC control methods that have been reported and implemented for other applications, the proposed DPC control is oriented to power quality compensation, in which the switching functions are re-defined, the bandwidths of the two hysteresis comparators are dynamically adjusted to eliminate short switching pulses, consequently, the average PWM switching frequencies are regulated. The proposed DPC controller is insensitive to load conditions and provides good steady state and dynamic performance.

(iv) The unified deadbeat control of the combined series-parallel compensator shows a number of advantages over the commonly used individual control of the two converters. The concept of unified control leads to an accurate and simple control structure by combining the two converters in system modeling. Two decoupled single-phase ac systems equivalent to the three-phase ac system are available through abc-$\alpha\beta$ coordinates transformation, and the deadbeat response is feasible for the two first-order equivalent systems. After compensation, the three-phase load voltage follows the reference voltage in a delay of one discretization time period, and the control system remains stable even in the case of control saturation.

6.3 Suggestions for Future Work

As an extension to this study of static power quality compensators in industrial power systems, the following topics are suggested:

(i) Develop a control algorithm to equalize the dc-bus voltages between the split capacitors of the four-switch voltage source converter.

(ii) Analyze and mitigate the effects of saturation of voltage coupling transformers in static series compensators.

(iii) Extend the direct power control technique to multi-level voltage source converters.

(iv) Develop a digital deadbeat controller based on FPGA circuits to provide a high sampling frequency for control algorithm implementation and PWM pattern generation.

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