Some Design Techniques for Low Power Low Noise CMOS Amplifier with Noise Optimization for Wireless Application in GHz Frequencies

M. Zamin Khan

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Abstract

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Zamin Khan

In recent years, there have been growing demands for bandwidth, for both voice and data communications. This has increased the need for high speed systems. The Radio Frequency integrated circuit (RFIC) and wireless market has suddenly expanded to unimaginable dimensions. Devices such as pagers, cellular and cordless phones, cable modems, and RF identification tags are rapidly penetrating all aspects of our lives, evolving from luxury items to indispensable tools.

Historically, RFIC's are implemented in III-V compounded semiconductors or in bipolar technologies. The DSP circuits, on the other hand, require small feature sizes to guarantee high speed of operation with low power consumption, hence the use of Complementary Metal-Oxide Semiconductor (CMOS) technologies. CMOS technologies are beginning to satisfy the needs of high-speed analog design, providing the drive for the quest for a complete commercial CMOS transceiver. Driven by the needs for low power, small size and low cost, CMOS RFIC design becomes main stream in modern wireless communication.

The challenges are not only to design RF transceivers in CMOS processes, but also to establish design methodologies for their building blocks. This thesis is concerned with one of the main building blocks, namely the Low Noise Amplifier (LNA). Several low Voltage LNA's have been successfully implemented in a standard 0.18 um CMOS

technology, operating in the 2.4-5 GHz frequency band. A new and very simple low voltage common source-common gate topology is suggested for low power consumption. The simulated results show the proposed topology is to be the choice in today's low power design with good performance in all aspects, when compared to other topologies.

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List of Symbols and Abbreviations

BJT	Bipolar junction Transistor
BW	Band width
C	Capacitor
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibel
DSP	Digital Signal Processing
g_m	Transconductance
I	Current
IC	Integrated Circuit
IIP3	Third Order Intercept Point
L	Inductance
LNA	Low Noise Amplifier
MOS	Metal Oxide Semiconductor
N.F	Noise Figure
Q	Quality factor
R	Resistor
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
S11	Input Matching
S22	Output Matching
S21	Power Gain
SNR	Signal to Noise Ratio

T	Temperature
V	Voltage
VCO	Voltage Controlled Oscillator
VDD	Positive Supply Voltage
VLSI	Very Large Scale Integration
VSS	Negative Supply Voltage
V_{th}	Threshold Voltage of a MOS Transistor

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Chapter 1 Introduction

1.1 Introduction

Historically, IC and RF designers have used different design methodologies, tools, and practices. Traditional analog designers have enjoyed an integrated front-to-back IC design system. On the other hand, RF designers with a discrete design background have used board-level computer-aided design (CAD) tools.

Traditional wireless system design was carried out at somewhat disjointed levels of abstraction: communication theorists created the modulation scheme and base band signal processing; RF system experts planned the transceiver architecture; circuit designers developed each of the building blocks; and manufactures "glued" the circuits and other components together. In fact, architectures were often planned according to the available off-the-shelf components, and circuits were designed to serve as many architectures as possible, leading to a great deal of redundancy at both system and device levels.[1]

The need for "modularity" in traditional RF design introduced many limitations at circuit and architecture level. In fact, the prevailing design mentality was to minimize the number of active devices because of their cost, inevitably requiring many passive components in each block. Designed and optimized as a stand-alone circuit, each building block would need to operate with standard interface impedance, usually 50 ohms, thus consuming substantial power.

Another attribute of traditional RF design was the use of trial and error rather than CAD tools. The lack of accurate device models and efficient simulation programs necessitated iterations at the board level to achieve an acceptable performance. Manual "tuning" used to be an integral part of RF system, a practice inherited to some extent in today's RF power amplifier design.

In recent years, RF design has undergone a paradigm shift, as more and more RF functions have been integrated on a chip and the number of discrete components has decreased. Traditional discrete designs are quickly reaching the physical limits of size, parasitic, and electrical performance. While in the past the wireless market was dominated by the relatively slow-growing military and cable television industries, its new consumer nature forces designers to seek more integrated solutions as opposed to the bulky, expensive, and power-hungry ones previously developed. [2]

This trend is more evident in the low-power segment of the wireless communication market, which includes handsets for cordless and cellular phones, pagers, and the more recent Bluetooth standard, where more compact and power-saving solutions are needed to accommodate the ever-growing demand for lighter and cheaper products.

Even though RF designs contain fewer devices compared to digital chips, they are inherently more challenging as very little automation is available for the design process. Moreover, RF devices are typically pushed to their performance limits; thus, all the nonlinearities and second-order effects need to be taken into account.

Nowadays, driven by an insatiable commercial demand for low cost and higher bandwidth with enhanced digital functionality in RF transceivers, RF designs are moving

towards high integration, low power, and low cost, while operating at higher frequencies (i.e. in the GHz range).[3]

1.2 Present Status of RF Design

Over the past two decades, RF systems have made remarkable progress, evolving from bulky, power-hungry boxes to miniature cellular phones and pager watches. RF transceivers have gone from simple voice communications to supporting data, electronic mail, and facsimile.

In addition to familiar wireless products such as pagers and cellular phones, RF technology has created many other markets that display a great potential for rapid growth, each presenting its own set of challenges to RF designers. Several such systems are discussed below.

WLAN [4]. Communication among people or pieces of equipment in a crowed area can be realized through a wireless local area network (WLAN). Using frequency bands around 900 MHz and 2.4 GHz, WLAN transceivers can provide mobile connectivity in offices, hospitals, factories, etc., obviating the need for cumbersome wired networks. Portability and reconfigurability are prominent features of WLANs.

GPS [4]. The use of GPS to determine one's location as well as obtain directions becomes attractive to the consumer market as the cost and the power dissipation of GPS receivers drop. Operating in the 1.5-GHz range, such systems are under consideration by

automobile manufactures, but they may be available as low-cost hand-held products sometime in near future.

RF IDs [4]. RF identification systems, simple called "RF IDs," are small, low-cost tags that can be attached to objects or persons so as to track their position. Applications range from luggage in airports to troops in military operations. Low power consumption is especially critical here as the tag's lifetime may be determined by that of a single small battery. RF ID products in the 900-MHz and 2.4-GHz range have recently appeared in the market.

Home Satellite Network [4]. The programs and services available through satellite television have attracted many consumers to home satellite networks. Operating in the 10-GHz range, these networks require the addition of a dish antenna and a receiver to a television set and directly competes with cable TV.

1.3 IC Technologies in RF Designs

The viable IC technology for RF circuits continues to change. Performance, cost, and time to market are three critical factors influencing the choice of technologies in the competitive RF industry.

The analog front-end was traditionally implemented using high performance technologies that can achieve high gains and low noise at high frequencies, such as Gallium Arsenide (GaAs) and Bipolar Junction Transistors (BJT's). The DSP circuits, on the other hand, require small feature sizes to guarantee high speed of operation with low power consumption, hence the use of Complementary Metal-Oxide Semiconductor (CMOS)

technologies. CMOS technologies are beginning to satisfy the needs of high-speed analog design, providing the drive for the quest for a complete commercial CMOS transceiver. As the minimum feature size of CMOS devices decreases, the RF performance (e.g. f_T) continues to improve to the point where they become comparable to those of GaAs and SiGe processes. A deep sub-micron CMOS device with f_T's exceeding 100 GHz. Rapid technology advances, coupled with the overwhelming dominance of CMOS in the digital arena, is making Si CMOS the best candidate for a single-chip solution for modern RF transceivers.

1.4 Motivation

A typical analog front-end employs four kinds of RF blocks, excluding any needed on-chip buffers, as shown in Figure 1.1: a low-noise amplifier (LNA), a mixer, a voltage-controlled oscillator (VCO), and a power amplifier (PA). The surface acoustic passive filters (SAW) are off-chip high-selectivity filters: Their narrowband performance is currently impossible to achieve using monolithic devices.

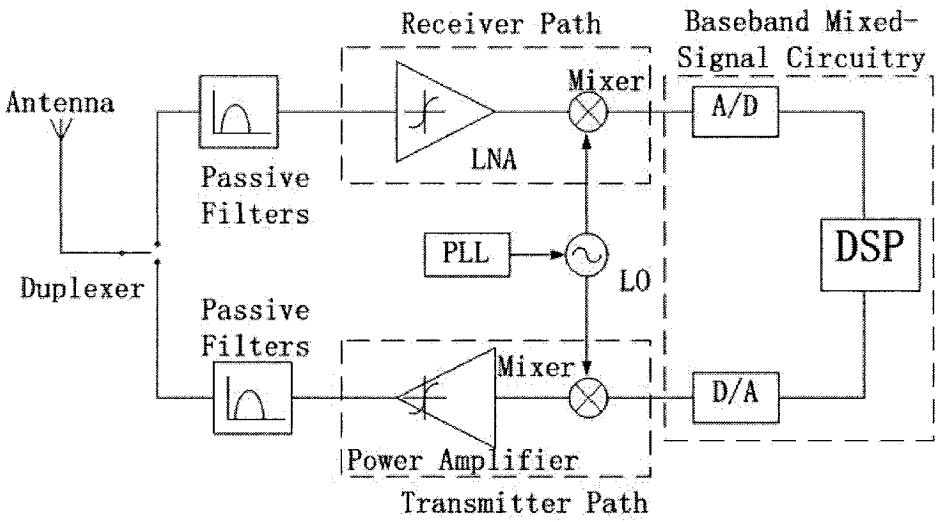

Figure 1.1 The conceptual block diagram of a typical RF transceiver.

The design of low-power RF ICs is strongly influenced by several factors. At the wireless communication system design level, the choice of frequency band, modulation scheme, transmitter power, and duty cycle has a major bearing on power consumption (the availability of frequency bands is governed by regulatory bodies). For a given system design, the radio architecture, IC process technology, and good circuit design all play a role in minimizing power consumption.

Cellular technology is a large market for RF ICs, and some consideration of the power requirements is worthwhile. Low cellular handset power consumption provides more talk time and /or smaller batteries, and is an important differentiating factor for competing ICs.

While the low cost and low power advantages of the CMOS technology are the dominant driving forces in the digital sector, the analog front-end become the bottlenecks in today's RF transceiver designs. Mainstream CMOS technologies are optimized for digital applications.

Over the last few years, wireless applications were developed for 900 MHz and 1.8 GHz bands, followed by current 2.4 GHz Bluetooth applications, then the 5-6 GHz bands for wireless LAN systems (e.g. IEEE 802.11a and HIPERLAN). Future technological advances and demand anticipate the use of CMOS technologies, operating at higher frequency bands (e.g. 5-10 GHz), for next-generation wireless communications applications.

The LNA is a critical building block in communications system as shown in Figure 1.1. It is usually the first active circuitry in the signal path in a receiver, which is supposed to amplify the weak RF signals received, while introducing as little noise as possible. The performance of the LNA affects the overall performance of a receiver, such as its sensitivity.

In general, wireless communication receivers demand low power consumption for portability and long battery life, while at the same time requires low noise figure, optimum gain, and high linearity. Several work on LNA's at 1- 5GHz have been reported in tables 1.1, 1.2 and 1.3, but little research has been done for decreasing the power consumption. Lowering the supply voltage (V_{DD}) is one of the most effective ways to decrease the power consumption. The bottle-neck for the low voltage design is the limitation of threshold voltages as it is not anticipated to decrease much below what is available today. The design of LNA is full of trade-offs between optimum gain, lowest noise figure, high linearity and low power consumption.

In this thesis, a CMOS low noise amplifier using proposed topology of common-source inductive source generation followed by common-gate is introduced, and several successful implementations of high frequency low-voltage integrated CMOS LNA's are

presented, demonstrating their performance and proving that the proposed topology is suitable for low power applications.

Table 1.1: Comparison of Several Reported LNAs in 5 GHz Band

Reference	[5]	[6]	[7]	[8]	[9]
Tech(um)	0.35	0.25	0.18	0.18	0.18
Freq.(GHz)	5.2	5.2	5.2	5.2	5.8
NF(dB)	2.45	2.1	2.0	1.4	2.5
S21(dB)	19.3	17	15.5	16.6	13
S11(dB)	N/A	-10	-11	-13	-5.3
S22(dB)	N/A	N/A	-10	N/A	-10.3
IIP3(dBm)	N/A	N/A	-4.3	0.6	N/A
Supply(V)	3.3	N/A	1.8	1.8	1
Power(mw)	26	N/A	10.4	16.2	22

Table 1.2: Comparison of Several Reported LNAs in 2.4GHz Band

Reference	[10]	[11]	[12]	[13]	[14]
Tech(um)	-	0.5	0.18	0.18	0.3
Freq.(GHz)	2.4	2.4	2.4	2.4	2.4
NF(dB)	1.8	2.4	1.6	4.0	2.0
S21(dB)	15	19	25	12	19
IIP3(dBm)	-	-	-8	-2	-
Supply(V)	5.0	3.0	1.5	1.8	-
Power(mw)	-	9	16	14.3	40.8

Table 1.3: Comparison of Several Reported LNAs in 1GHz Band

Reference	[15]	[16]	[17]	[18]	[19]
Tech(um)	0.35	0.5	0.8	1.0	0.5
Freq.(GHz)	0.9	0.9	0.9	1.0	1.0
NF(dB)	2.0	2.5	6.0	3.5	2.7
S21(dB)	17.5	9	17	22	12.2
IIP3(dBm)	-6.0	-4.7	-14	12	-21
Power(mw)	-	10	78	27	17

1.5 Thesis Outline

The thesis begins with an overview on the current technology choices in RF applications, for an LNA design. The challenges and the need for integrated CMOS LNA's operating in the 1-5 GHz frequency band, with a strong emphasis on low power design topologies are motivated.

Chapter 2 provides a brief review of the basic theory related to the proposal of the thesis. The basic theory and important parameters such as noise performance and distortion in RF designs are reviewed.

In chapter 3, different LNA topologies, which are suitable for low-voltage (sub 1V) application, are presented. Trade offs, in term of noise performance, gain and linearity are described. Finally, a new common-source inductive source generation followed by common-gate topology is proposed to be the choice in today's low power design with good performance in all aspects, when compared to other topologies.

In chapter 4, the layout issues and techniques are discussed. Lay out is another step in optimizing high frequency design. Poor layout could result into a non-working circuit. In this chapter, the layout techniques adopted in this work are addressed.

In chapter 5, different successful CMOS LNA implementations are presented and verified by simulation results. In this section, post layout simulation results are presented. All LNA implementation are designed with a low supply voltage (sub1V). Finally, a summary of all implementations, together with a comparison to other designs from the literature, is presented.

In chapter 6, the thesis concludes with a summary of the work done and with the results obtained, suggestion for future work, ending up with the contribution of this thesis in different Conferences and Journals.

Chapter 2 CMOS Low Noise Amplifer Basics

2.1 Introduction

The first stage of a receiver is commonly a Low Noise Amplifier (LNA), whose main function is to provide enough gain to suppress the additive noise of subsequent stages (e.g. mixer and image rejection filter). The noise characteristics of the LNA limit the sensitivity of the entire receiver. An LNA should add as little noise as possible and accommodate large signal without distortion.

In this chapter, some basic parameters such as noise and distortion in RF circuits are discussed. This is followed by a detailed design equations behind the most common CMOS LNA topology used at RF, which is suitable for low voltage (i.e. volt < 1V).

2.2 Noise Fundamentals [20]

2.2.1 Thermal Noise

The thermal noise is a white noise, i.e. it has a constant power spectral density throughout the frequency spectrum. It is caused by the random thermally excited vibrations of charge carriers in a conductor. The available thermal noise power of a resistor is defined as "the power that can be supplied by this resistive source to a matched but noiseless resistor."

For a given frequency bandwidth, Δf, the available noise power of one ohm resistor is proportional to its absolute temperature T expressed in Kelvin's:

$$N_{av} = kT\Delta f \tag{2.1}$$

Where k=1.38*10^{-23} J/K is the Boltzman constant. At room temperature (T=290°K), for a 1Hz bandwidth, the noise power expressed in dBm is -174 dBm. For circuit analysis, it is usually convenient to replace a 'noise' resistor with a noiseless resistor in conjunction with a root-mean-square (rms) noise source. The mean square noise power delivered to a load resistor R' is easily derived to be (Figure 2.1a):

$$N_{R'} = \overline{V_n^2} \cdot \frac{R'}{(R+R')^2} \tag{2.2}$$

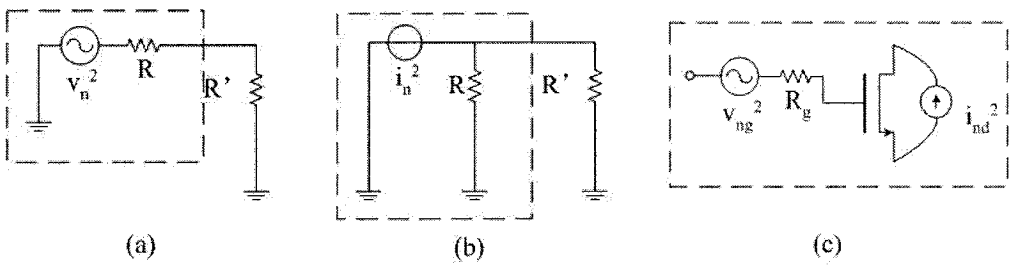

Figure 2.1 (a) Noise voltage (b) Noise current models for resistors thermal noise (c) MOS transistor noise sources.

If we set R=R', the above noise power will become the available noise power:

$$N_{R'=R} = N_{av} = kT\Delta f = \frac{\overline{v_n^2}}{4R} \tag{2.3}$$

This allows us to derive an expression for the mean square noise voltage in a resistance:

$$\overline{v_n^2} = 4RN_{av} = 4kTR\Delta f \tag{2.4}$$

In a similar fashion, the equivalent mean square noise current source can be derived to be (Figure 3.1b):

$$\overline{i_n^2} = \frac{4kT\Delta f}{R} \tag{2.5}$$

2.2.2 Shot Noise

Shot noise occurs due to the direct flow of current in diodes and transistors. It is due to the random drifting of charge carriers across the PN-junction, which results in current fluctuation (i.e. shot noise) around the average current value. The shot noise current is expressed as:

$$\overline{i_{sn}^2} = 2qI_D\Delta f \tag{2.6}$$

Where $\overline{i_{sn}^2}$ is the RMS noise current, q = 1.602*10^{-19} C is the electron charge, I_D is the average DC current, and Δf is the noise bandwidth.

From equation 2.6, the shot noise can be reduced by minimizing the bias current of an active device.

2.2.3 Flicker Noise (1/f Noise)

Flicker noise is due to random trapping of charge carriers associated with contaminations and defects in crystal lattices, which gives rise to a noise power dominated at low frequencies.

Similar to shot noise, flicker noise $\overline{i_{fn}^2}$ occurs in the presence of direct current flow, and is given by:

$$\overline{i_{fn}^2} = K\frac{I^a}{f^b}\Delta f \qquad (2.7)$$

Where K is a device-specific empirical parameter, I is the average DC current, Δf is again the noise bandwidth, "a" is a constant ranging from 0.5 to two, and "b" is another constant of about unity.

In LNA applications, RF signals are amplified in a narrowband fashion with a typical bandwidth of few hundreds of MHz around the center frequency of 2.4 to 5 GHz. Hence, flicker noise does not play an important role in LNA applications, because it only dominates at low frequencies. However, it becomes an important noise source when considering a complete transceiver where frequency translation is performed. On the receiver side, excessive flicker noise will corrupt the down-converted RF signals at base-band. On the transmitter side, flicker noise can be up-converted to the RF band where it interfaces with the desired RF signals. Nonetheless, flicker noise is a bigger concern in oscillator designs, for example, compared to the main focus of our work.

2.2.4 MOS Transistor Noise Sources [20]

Two major noise sources come into play at RF when dealing with MOS transistors.

A. Channel thermal noise

Modeled by a noise current source:

$$\overline{i_{nd}^2} = 4kT\gamma g_m \qquad (2.8)$$

Where g_m is the transistor transconductance, and γ is a layout-dependent constant, found to be 2/3 for long-channel devices. In short-channel devices, however, measurements

have revealed that this constant can be much higher. The above equation can be interpreted as the noise current of a drain resistance of value:

$$R_{Drain} = \frac{1}{\gamma g_m} \tag{2.9}$$

B. Gate resistance noise

This noise is the channel noise injected into the gate due to the physical distributed gate resistance:

$$R_g = \frac{R_{sq} W}{12 n^2 L} \tag{2.10}$$

Where R_{sq} is the sheet resistance of ploysilicon, W the total gate width of the device, L is the channel length, and n the number of gate fingers used. The 1/12 factor assumes that both ends of the transistor gate are shorted (otherwise this term becomes 1/3). By choosing a large number of gate fingers, R_g can be minimized and rendered negligible.

2.2.5 Noise Figure

The standard definition of the noise factor is the degradation of the SNR due to the circuit at hand [4], usually an amplifier or a frequency-translating circuit:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in} / N_{in}}{S_{out} / N_{out}} \tag{2.11}$$

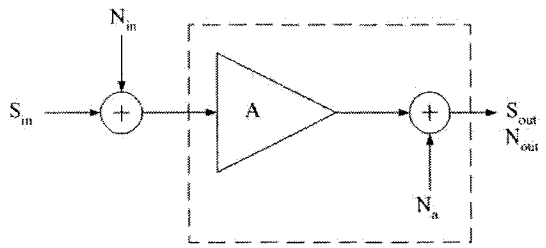

Figure 2.2 Noise-equivalent block diagram of a practical amplifier.

where S, N, and SNR are the signal power, noise power, and signal-to-noise ratio respectively. The subscripts denote whether the quantity considered is at the input or at the output. The input-injected noise power is usually the thermal noise of the driving source impedance, R_s, such as a 50 Ω antenna. If the input impedance of the circuit is matched to R_s, the input-injected noise power becomes the available noise power from R_s:

$$N_{in} = N_{av,R_s} = kT\Delta f \tag{2.12}$$

A more commonly used noise parameter is the noise factor F expressed in decibels, and known as the Noise Figure:

$$NF = 10 \cdot \log_{10} F = SNR_{in}(dB) - SNR_{out}(dB) \tag{2.13}$$

The ideal limit is that of a noiseless amplifier, which leads to F=1 and NF=0dB. Practical implementations can never provide such a low value.

Considering an amplifier with power gain A^2, the input-output relationships can be expressed as (Figure 2.2):

$$S_{out} = A^2 \cdot S_{in} \tag{2.14}$$

$$N_{out} = A^2 \cdot N_{in} + N_a \tag{2.15}$$

Where N_a is the available noise power of the amplifier. This power will be completely supplied to a subsequent stage only if there is perfect impedance match at the output of the amplifier. Equation (2.11) can then be rewritten in its more popular form:

$$F = \frac{A^2 N_{in} + N_a}{A^2 N_{in}} = 1 + \frac{N_a}{A^2 N_{in}} \tag{2.16}$$

Thus, the noise factor can be viewed as the ratio of the total output noise power, to the component of the output noise power that is due to the input-injected noise, N_{in}:

$$F = \frac{total \quad output \quad . \quad noise \quad power}{output \quad noise \quad power \quad due \quad to \quad input \quad source} \tag{2.17}$$

Or alternatively,

$$F = 1 + \frac{output \quad noise \quad power \quad due \quad to \quad circuit \quad noise}{output \quad noise \quad power \quad due \quad to \quad input \quad source} \tag{2.18}$$

Dividing both the numerator and denominator of (2.17) by the power gain of the amplifier, we obtain a similar and useful expression:

$$F = \frac{total \quad input \quad equivalent \quad noise \quad power}{input \quad injected \quad noise \quad power} \tag{2.19}$$

Given the noise factor F and the gain A of an amplifier, the available noise power of the amplifier can be easily derived from (2.15) to be:

$$N_{out} = A^2 (F - 1) N_{in} \tag{2.20}$$

2.2.6 Cascaded Noise Figure[21]

Considering a cascade of n matched amplifiers of gains A_k and noise factors F_k, (Figure2.3), the equivalent noise contribution of stage k when viewed at the input of the system can be expressed as:

$$N_{k,in} = \frac{N_{ak}}{A_k^2 A_{k-1}^2 \cdots A_1^2} \tag{2.21}$$

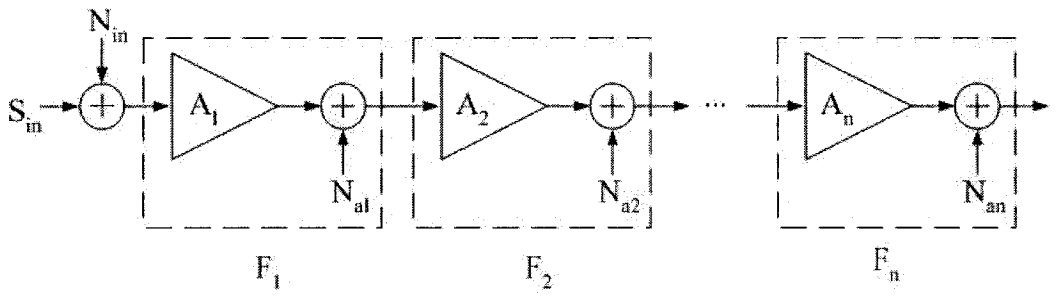

Figure 2.3 Cascade of 'noise' amplifier.

Replacing N_{ak} by Equation (2.21), we obtain:

$$N_{k,in} = \frac{(F_k - 1)N_{in}}{A_{k-1}^2 \cdots A_1^2} \tag{2.22}$$

Finally, the noise factor of the cascade can be derived using Equation (2.22):

$$F = \frac{N_{in} + \sum_{k=1}^{n} N_{ai,k}}{N_{in}} = F_1 + \frac{F_2 - 1}{A_1^2} + \frac{F_3 - 1}{A_1^2 A_2^2} + \ldots \tag{2.23}$$

The above equation, known as the Friis' formula, shows that the first stage has the most pronounced effect on the noise figure of the amplifier cascade. Thus, the first stages in a cascade of amplifiers have to display both a low noise figure and a high gain in order to minimize the noise figure of the entire cascade.

2.3 Distortion

2.3.1 Non-linearity

The behaviour of many analog and RF circuits can be approximated by a linear model represented in the form of a small signal response. As the input signal power increases to a level beyond the small signal approximation, non-linear effects become prominent. In circuit, these non-linearities are mainly due to the characteristics of the transistors.

To account for the non-linear effects, consider a practical system with a transfer function:

$$y(t) \approx \alpha_1 x_{in}(t) + \alpha_2 x_{in}^2(t) + \alpha_3 x_{in}^3(t) + \ldots \qquad (2.24)$$

Where α_1 is the linear gain factor of the system and $\alpha_n > 1$, for $n > 1$, is the non-linear gain factor.

By applying a single-tone input, $x_{in}(t) = A \cdot \cos(\omega t)$, and using common trigonometric identities, we are able to obtain a useful expression for the higher frequency harmonics: [4]

$$y_{out}(t) = \frac{\alpha_2 A^2}{2} + \left[\alpha_1 A + \frac{3}{4}\alpha_3 A^3\right]\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) + \ldots \quad (2.25)$$

The latter will be discussed in more details in the following sections.

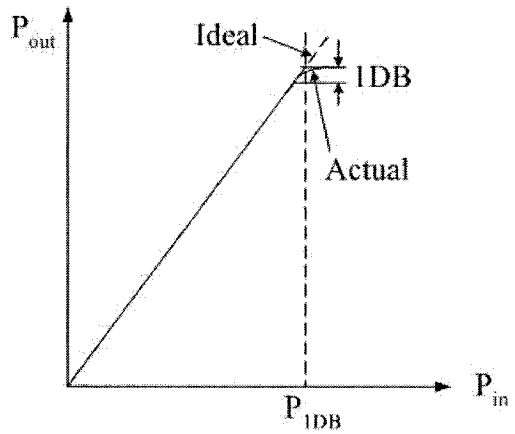

Figure 2.4 1dB Compression point.

2.3.2 Gain Compression

The first test or measure of non-linearity is how "compressive" or "saturating" the output is, as a function of the input. Indeed, the gain of practical amplifiers (and systems in general) decreases as the input amplitude increases beyond a certain limit until the output saturates, as shown in Figure 2.4. The common compression measure is the 1-dB compression point, which is defined as the point where the actual output is 1 dB lower than the expected output.

To express it mathematically, we only need to consider the gain seen by the fundamental harmonic in Equation (2.25):

$$y_{fund}(t) \approx \left[\alpha_1 A + \frac{3}{4}\alpha_3 A^3\right]\cos(\omega t) \qquad (2.25)$$

In order for the gain to decrease, i.e. output compression α_3 needs to be negative. The 1-dB compression point in the case is the point where the practical gain, $G_{prcatical} = \alpha_1 + \frac{3}{4}\alpha_3 A^2$, becomes 1 dB lower than the ideal gain, $G_{ideal} = \alpha_1$:

$$20\log_{10}\left|\alpha_1+\frac{3}{4}\alpha_3 A_{1dB}^2\right| = 20\log_{10}|\alpha_1| - 1dB \tag{2.26}$$

Leading to:

$$A_{1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.27}$$

2.3.3 Intermodulation Distortion

Another performance metric used to evaluate the distortion of a system is to measure how "multiplicative" the distortion is, by applying an input with multiple-tones and measuring the system response. A common measure used is the Intermodulation distortion in a "two-tone" test, and is quantified by the input and output third-order intercepts IIP_3 and OIP_3, respectively. [29]

When two adjacent tones, separated by a frequency of $2\Delta\omega$ are applied to the input of a non-linear system, the output generally exhibits some frequency components that are not direct harmonics of the input frequencies, appear at the output. These are called Intermodulation (IM) products.

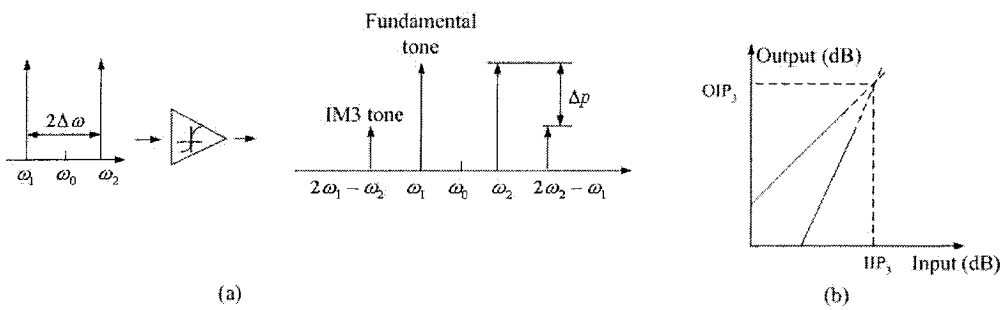

Figure 2.5 (a) Intermodulation in a non-linear system (b) Third-order intercept.

This happens due to the mixing of the two input tones as shown in Figure (2.5a).

Consider the input signal [4] $x(t) = G\cos(\omega_1 t) + G\cos(\omega_2 t)$, where $\omega_1 = \omega_0 - \Delta\omega$, and $\omega_2 = \omega_0 + \Delta\omega$, and ω_0 is the center frequency. The output spectrum, as given by Equation 2.18, becomes:

$$y(t) = \alpha_1[G\cos(\omega_1 t) + G\cos(\omega_2 t)] + \alpha_2[G\cos(\omega_1 t) + G\cos(\omega_2 t)]^2 + \alpha_3[G\cos(\omega_1 t) + G\cos(\omega_2 t)]^3 \ldots \quad (2.28)$$

By expanding Equation 2.25, the third order IM products (IM_3) can be obtained as:

$$\omega = 2\omega_1 - \omega_2; y_{IM3} = \frac{3\alpha_3 G^3}{4}\cos[(2\omega_1 - \omega_2)t] = \frac{3\alpha_3 G^3}{4}\cos[(\omega_0 - 3\Delta\omega)t] \quad (2.29)$$

$$\omega = 2\omega_2 - \omega_1; y_{IM3} = \frac{3\alpha_3 G^3}{4}\cos[(2\omega_2 - \omega_1)t] = \frac{3\alpha_3 G^3}{4}\cos[(\omega_0 + 3\Delta\omega)t] \quad (2.30)$$

From Equation 2.26 and 2.27, it can be easily seen that the third order IM products increase in proportion to G^3, whereas the fundamental tone increases linearly with G. On a logarithmic scale, the magnitude of the IM products grows at three times the rate at which the main tone increases. The IIP_3 and OIP_3 are defined as the point where the powers of the fundamental tones (i.e. $\alpha_1 G$) equal the powers of the third order Intermodulation products (i.e. $\frac{3\alpha_3 G^3}{4}$), as shown in Figure 2.5b. Mathematically, it can be expressed as:

$$\alpha_1 IIP_3 = \frac{3\alpha_3 (IIP_3)^3}{4} \quad (2.31)$$

Hence,

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}(dB) \quad (2.32)$$

And alternatively, the IIP_3 can be expressed in dBm and given by:

$$IIP_3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm} \tag{2.33}$$

Where P_{in} is the input power level in dBm, and ΔP is the difference in the power level in dB between the fundamental and the IM_3 tones, as shown in Figure 2.5a.

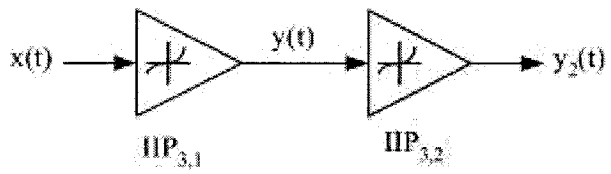

Figure 2.6 Cascade of two non-linear stages.

2.3.4 Cascaded Non-linearities

Consider two non-linear stages in cascade as shown in Figure 2.6, with input-output characteristics express as:

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.34}$$

$$y_2(t) = \beta_1 y_{in}(t) + \beta_2 y_{in}^2(t) + \beta_3 y_{in}^3(t) \tag{2.35}$$

Then, be only considering the first and third order terms, it can be easily shown that the overall transfer function of a cascade system is given by:

$$y_2(t) = \alpha_1\beta_1 x(t) + (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3)x^3(t) + \ldots \tag{2.36}$$

Thus, similar to Equation 2.29, the overall IIP_3 of two non-linear stages in cascade is:

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_1\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3}\right|}(dB) \tag{2.37}$$

Alternatively, by manipulating Equation 2.34, we can write:

$$\frac{1}{IIP_3^2} = \frac{3}{4} \cdot \frac{|\alpha_1\beta_1| + |2\alpha_1\alpha_2\beta_2| + |\alpha_1^3\beta_3|}{|\alpha_1\beta_1|} = \frac{1}{IIP_{3,1}^2} + \frac{3\alpha_2\beta_2}{2\beta_1} + \frac{\alpha_1^2}{IIP_{3,2}^2} \qquad (2.38)$$

Where $IIP_{3,1}$ and $IIP_{3,2}$ are the input IP_3 of the first and second stages, respectively.

For n cascaded non-linear stages, the overall IIP_3 of the system can be derived by generalizing Equation 2.36 and is expressed as:

$$\frac{1}{IIP_3^2} \approx \frac{1}{IIP_{3,1}^2} + \frac{\alpha_1^2}{IIP_{3,2}^2} + \frac{\alpha_1^2\beta_1^2}{IIP_{3,3}^2} + \ldots + const. \qquad (2.39)$$

As can be seen from Equation 2.36, the non-linearity of the latter stages have a bigger impact on the overall non-linearity of the system, since the IP_3 of each stage is effectively degraded by the total gain preceding that stage.

2.4 LNA Performance Metrics

Many performance metrics are used to evaluate the behaviour of an LNA (Table 2.1), most important of which are its noise figure and gain. [4]

Table 2.1 LNA performance metrics

NF	2dB
S21	10dB
S11	-10 dB
S12	-20 dB
Power	10mW
VCC	1.5-3V

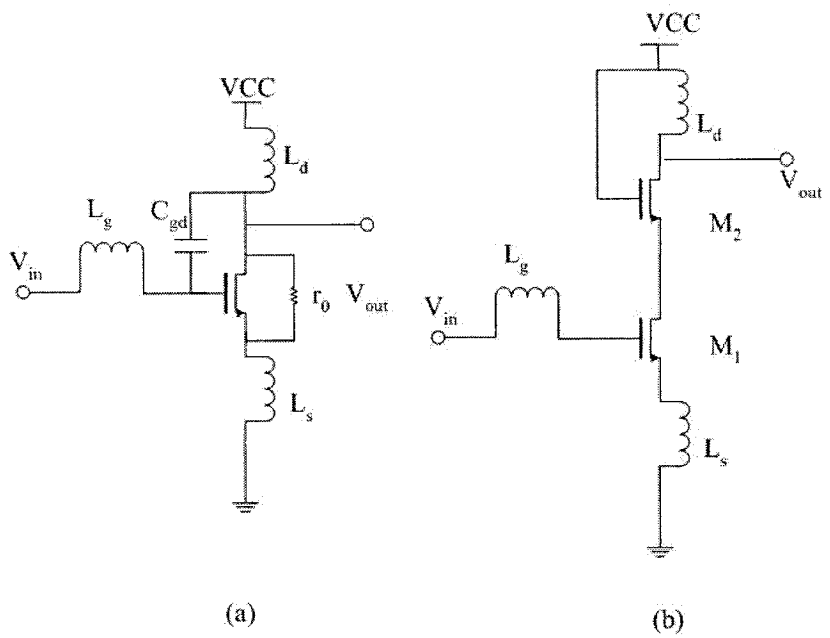

Figure 2.7 Common-source LNA topologies: (a) single transistor (b) cascode.

Those metrics should always be viewed in the context of the entire receiver with the goal of optimizing the entire system's performance, rather than that of this single component:

- The LNA's noise figure should be minimized as it directly affects the sensitivity of the entire receiver.
- Increasing the forward gain, S21, would also improve the receiver's noise figure, but at the expense of the non-linearity of the receiver.
- The LNA's linearity is less critical for the receiver, as subsequent stages' behaviour provides the bulk of the receiver's distortion. This relaxes the design a bit, as the amplifier's distortion can be traded-off to minimize power consumption.
- Finally, keeping with the low-power trend, modern receiver implementations need to be able to function with low voltage supplies, adding further to the design challenges.

2.5 CMOS LNA Fundamentals

The most common topology for RF CMOS LNA's is the common-source amplifier with inductive load and inductive degeneration. Two variants of this topology exist, (Figure 2.7), and both make heavy usage of inductors. At high-frequencies, inductors are usually on-chip, as integration becomes extremely desirable to eliminate package and bonding parasitics. A major drawback, however, is the strong dependence of the LNA's performance on the quality of those inductors, which are rather low in integrated form.

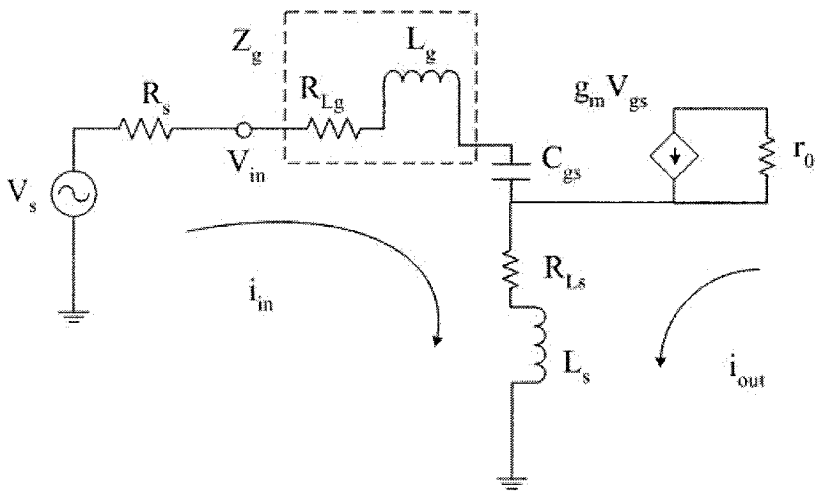

Figure 2.8 Equivalent circuits at the input.

The single-transistor LNA can be adequate at low frequencies. At higher frequencies, this circuit presents little reverse-isolation, due to the feedback path created by the gate-drain capacitance, C_{gd} (Figure 2.7a). This complicates the tuning of the amplifier, and may

render this circuit to potentially unstable. The more common cascode configuration solves this problem, while providing the same functionality (Figure 2.7b).

2.5.1 Input Matching

Using the equivalent circuit at the input of the LNA (Figure 2.8), we can write the following KVL Equation using the mesh currents i_{in} and i_{out}:

$$V_{in} = i_{in}(Z_g + Z_s) + i_{out}Z_s + V_{gs} \tag{2.40}$$

If we ignore the transistor channel-length modulation impedance, r_o, the mesh current i_{out} will become equal to the drain current $g_m V_{gs}$.

The input impedance can be found to be:

$$Z_{in} = \frac{V_{in}}{i_{in}} = Z_g + Z_s + \frac{1}{sC_{gs}} + \frac{g_m}{sC_{gs}}Z_s \tag{2.41}$$

By ignoring the resistivities of the inductors, we rewrite the above equation as:

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}}L_s \tag{2.42}$$

If the reactive components are made to resonate at the required center-frequency ω_0, the real term will be left unaffected:

$$\omega_0^2 = \frac{1}{(L_g + L_s)C_{gs}} \tag{2.43}$$

$$Z_{in}(\omega = \omega_0) = \frac{g_m}{C_{gs}}L_s = \omega_T L_s \tag{2.44}$$

Where ω_T is the unity-gain frequency of the transistor.

By making the appropriate device sizing and inductor choice, the input tank can be made to resonate and provide the required real input impedance:

a. L_s controls the value of the input impedance.

b. L_g is chosen to cancel the capacitive effect of C_{gs} and force resonance at the desired center frequency.

While these equations provide grounds for physical intuition, the series resistances of the inductors will also affect Z_{in}, resulting in:

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}}(1 + g_m R_{L_s}) + \omega_T L_s + R_{L_s} + R_{L_g} \quad (2.45)$$

As the inductors' resistances and inductance values are correlated, the inductors' layouts should be manually optimized to maximize matching. Reasonable starting values can be obtained from Equation (2.44) and (2.45).

2.5.2 Noise Figure

In practical, inductor L_g and L_s resistances have a non negligible contribution to the Noise Figure. The noise figure is given by [22], [23]

$$F = 1 + \gamma \frac{1}{R_s g_m Q_{in}^2} \quad (2.46)$$

Where Q_{in} is the quality factor of the entire input network. R_s is the source impedance.

2.6 Conclusion

In this chapter, we have discussed the main theory behind the LNA's design and circuit analysis. In next chapter, all different LNA topologies and proposed topology will be discussed.

Chapter 3 CMOS LNA Circuit Topologies

In this chapter, different CMOS LNA design topologies are described. This is then followed by a proposed design topology, which is suitable for low-voltage (sub 1 volt) applications.

3.1 Review of Topologies

Apart from the low noise characteristics targeted in LNA designs, input matching and power gain are also two important performance metrics. Input impedance matching is essential in an LNA design because the device has to provide a 50 Ω termination for the transmission line delivering the RF signal from off-chip. It should be noted that often the performance of the preceding filter (e.g. band selection filter) depends heavily on the quality of the terminating impedance. The power gain of an LNA is also critical, since higher gain translates into an improvement in the overall receiver noise figure, at the expense of higher non-linearity for the subsequent stages. In this section, detailed different design topologies of LNA are presented.

The first topology is classical Noise matching. In this topology, the LNA is designed for minimum NF by adding a matching circuit between the source and input of the amplifier

in Figure 3.1, to provide a 50ohms impedance matching at the input port. There are several disadvantages in using this technique: The extra resistor contributes its own thermal noise to the output, which equals the noise contribution of the source resistance. This means that there would be an immediate 3dB increase in the noise figure. Furthermore, the input signal is attenuated by the resistor termination before reaching the active device, which causes a reduction in gain. Thus, one cannot obtain both input matching and minimum NF simultaneously. The large noise penalty due to the use of resistive termination is the limitation of the classical noise matching.

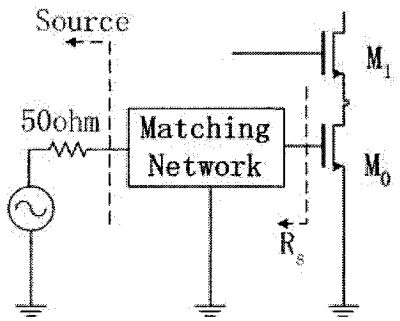

Figure 3.1 Cascode LNA topology used to apply classical noise matching technique.

The second topology, shown in Figure (3.2), uses the source of a common gate stage as the input termination. Appropriate transistor sizing and biasing is chosen such that the impedance looking into the source of the transistor (i.e. $1/g_m$) equals the characteristic impedance of 50 ohms. It can be shown that the lower bounds on the noise factor of this topology in a CMOS technology is given by: [4]

$$F = 1 + \frac{\gamma}{\alpha} \geq \frac{5}{3} \Rightarrow NF = 2.2dB \qquad (3.1)$$

And

$$\alpha \equiv \frac{g_m}{g_{d0}} \tag{3.2}$$

Where γ is a bias-dependent factor of the channel thermal noise, g_m is the device transconductance, and g_{d0} is the zero-bias drain conductance. The computed minimum noise figure of 2.2 dB in equation (3.1) is based on the assumption of long channel devices with parameters $\gamma = 2/3$ and $\alpha = 1$. In today's deep sub-micron CMOS devices, γ can be as high as two-to-three, which is due to the hot electrons effect, and α can be less than one. The theoretical minimum achievable noise figure for short channel devices in this topology is around 3dB, which doesn't satisfy today's low noise requirements.

The third topology is popular due to its inherent good noise performance. It employs inductive source degeneration, as shown in Figure (3.2b), to present real impedance at the input terminal. [24]

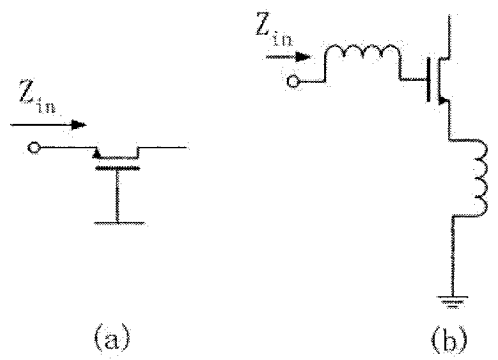

Figure 3.2 LNA matching topologies (a) $1/g_m$ degeneration (b) Inductive degeneration.

3.1.1 Low Voltage LNA Topologies

The development of wireless portable electronics is moving towards smaller and lighter devices with longer operating time, which requires compact low-voltage and low-power design topologies. Furthermore, the general trend of semiconductor device scaling has lead to reduced voltage requirements in order to avoid breakdown effects. For example, by migrating from a 0.35 μm to a 0.18 μm CMOS process, the typical turn-on voltage of an NMOS transistor is decreased from 0.7V to 0.5V, while the core supply voltage is reduced from 3.5V to 1.8V. These trends dictate that future RF frond-ends will have to operate with low voltages (i.e. <1V). under the reduced voltage supply, many common circuit topologies in RF designs, such as the conventional cascade structure and the Gilbert-cell structure, can no longer be employed because of the stacking constrains of transistors between the supply rails.

With the targeted voltage supply down to 1V there are limited numbers of suitable LNA topologies. Some amplifier implementations which can operate at sub-1V, along with the conventional cascode amplifier, are shown in Figure 3.3. Due to the superior noise performance of the common-source configuration with inductive degeneration in LNA designs, all the topologies presented in this thesis are based on this configuration.

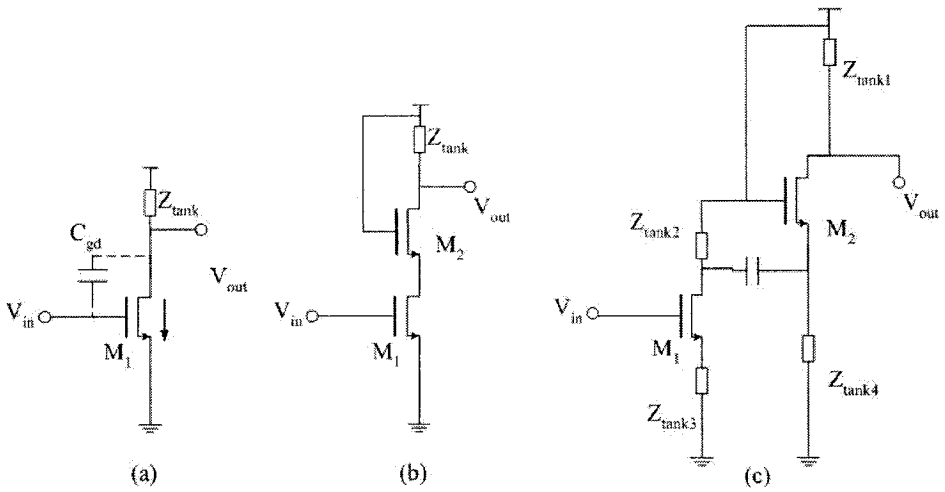

Figure 3.3 LNA topologies: (a) Single transistor (b) conventional cascode (c) proposed common-source common-gate.

3.1.2 Single Transistor LNA Topology

Consider the single transistor amplifier shown in Figure (3.3a). The minimum voltage headroom for this topology equals the voltage required to set the transistor into saturation (i.e. $V_{ds\text{-}sat}$). Since only a single supply is used in an actual implementation, the absolute minimum voltage equals the threshold voltage of the transistor (i.e. V_{th}), which is typically greater than $V_{ds\text{-}sat}$. Despite meeting the sub-1V design requirement, there remain many challenges with using this topology, which make it not desirable as the choice for low-voltage RF architecture. The main disadvantage of this topology is that it is very susceptible to instability problems as the frequency of operation increases. This is mainly due to the gate-to-drain parasitic capacitance (C_{gd}) which provides a low impedance feedback signal path at RF. Furthermore, following Miller transformation [25], the equivalent input capacitance (C_{in}) of the transistor becomes:

$$C_{in} = C_{gs} + (1 - A_v)C_{gd} \tag{3.3}$$

Where A_v is the voltage gain across the gate-to-drain capacitance of the common-source transistor. This setup further complicates the input impedance and noise matching, since the input reactance becomes not only dictated by C_{gs}, as can be seen in Equation 3.3, but is also a function of A_v and C_{gd}. Hence, it is rare to see implementations using this topology in modern fully integrated high frequency RF design.

3.1.3 Conventional Cascode LNA Topology

In order to alleviate the potential instability problems in a signal transistor amplifier, a common approach is to use the cascode configuration shown in Figure (3.4). This topology, together with the common-source configuration, has proven to be popular with excellent gain and noise performance in LNA designs. Substantial researches have been invested in LNA designs based on this topology. One of the main drawbacks of this structure is the need for relatively high supply voltage headroom, since it involves a minimum of two transistors stacking, which is not quite suitable for sub-1V applications.

3.1.4 Cascode LNA Topology

To achieve lower noise and higher gain, one cascode with the inductor degeneration topology is shown in Figure 3.4:

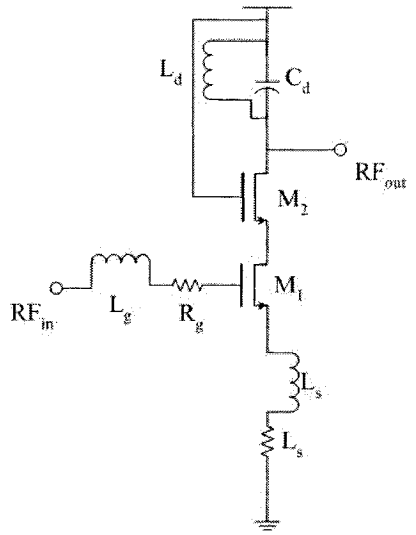

Figure 3.4 Schematic of a cascode topology with inductor degeneration.

The equivalent circuit of cascode topology scheme for small signal at the input of the LNA is shown in Figure 3.5.

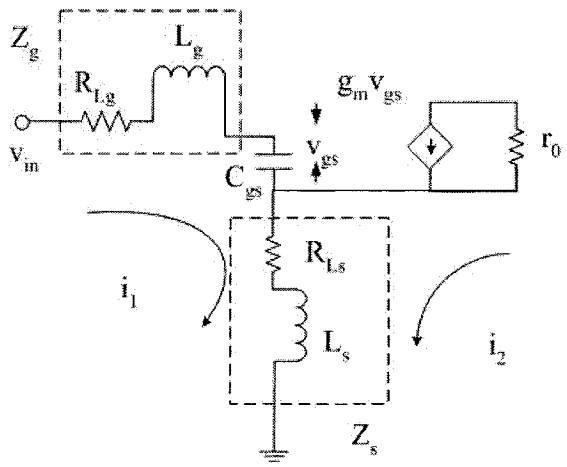

Figure 3.5 Small signal equivalent circuits at the input of LNA.

3.2 Design with Proposed New Topology

For LNA design, inductive source degeneration is used to achieve good input matching without adding thermal noise introduced by real resistor. The cascode topology shown in Figure 3.4 is a popular configuration for LNA design but it is not suitable for low voltage supply applications.

The proposed topology is shown in Figure 3.6, which works for low power supply applications such as 1V. Inductive source degeneration is also used to achieve good input matching and reduce noise figure. The first stage is inductively degenerated common-source amplifier formed by transistor M_0. Followed by a common-gate configurated transistor M_1, the value of LC tank of M_0 is carefully chosen to achieve a resonance frequency and is required to have a much higher impedance than that of the input impedance looked at the source of M_1. It provides a DC bias current path for M_0 and a high impedance branch to force the RF signal to flow into the source of M_1 through a big DC coupling capacitance C_s.

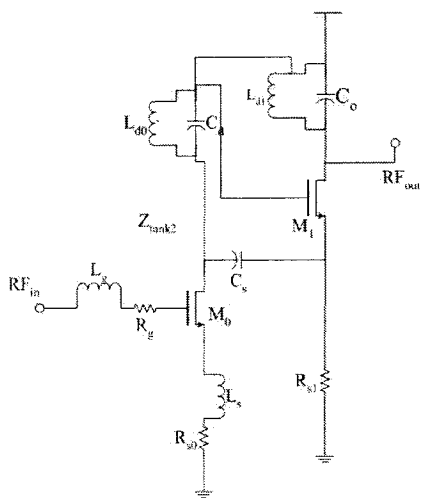

Figure 3.6 Common source common gate topology.

The input impedance of the LC tank (L_d, C_d) is

$$Z_d = R_d + \frac{\omega^2 L_d^2}{R_d} = \frac{\omega^2 L_d^2}{R_d} = R_d Q_d^2 \tag{3.4}$$

Then,

$$g_{m1} \rangle\rangle \frac{1}{R_d Q_d^2} \tag{3.5}$$

Where R_d and Q_d are the resistance and the quality factor associated with the inductor L_d.

The input impedance at the source of the common gate transistor M_1 is:

$$R_i = \frac{1}{g_{m1} + g_{mb1}} = \frac{1}{g_{m2}} \tag{3.6}$$

Where g_{mb} is the bulk transconductance

3.2.1 Threshold voltage control

The bottle-neck for the low voltage design is the limitation of threshold voltage because it is not anticipated to decrease much below what is available today. A solution to the threshold voltage problem comes from the well-know relationship as given: [25]

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}) \tag{3.7}$$

Where V_{th0} is the value of V_{th} with $V_{BS} = 0$, Υ is the bulk threshold parameter and Φ is the strong inversion surface potential of the MOSFET. For n-channel transistor voltage can be decreased. To reduce the threshold voltage as much as possible, we want the bulk bias V_{BS} as high as possible. This will however, forward bias the bulk-source diode or the base-emitter diode of the associated parasitic bipolar transistor (BJT) as shown in Figure 3.7, thereby turning on this BJT and an undesired bulk current increases significantly.

Thus, to keep the bulk current low, the parasitic BJT should be off i.e., bulk-source voltage should be smaller than 0.7V.

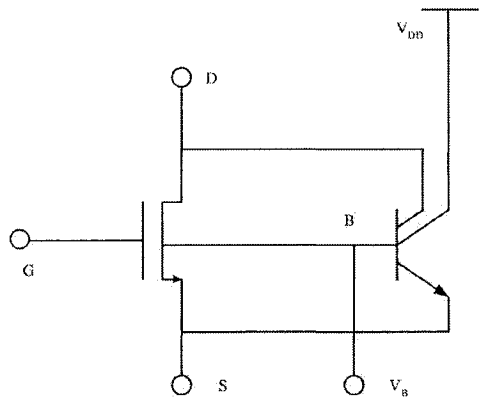

Figure 3.7 NMOS transistor with parasitic BJT

3.2.2 Bulk Source Biasing

To make the cascode LNA function, the well-source junction of the NMOS transistors are forward biased as shown in Figure 3.8 which causing the threshold voltage to decrease. By applying a voltage on V_{BS}, we can control the threshold voltage V_T and thus the polarization if the transistor. Once the threshold is reduced, the value of Vgs for the same current is less.

In 2.4 GHz LNA design, the VT decreased from 0.5 V to less than 0.4 V when 0.5V supplied to bulk and the value of current through bulk is 40 uA although this current is undesirable. The bulk current remains below 40 uA for bulk-source voltages as high as 0.5 V.

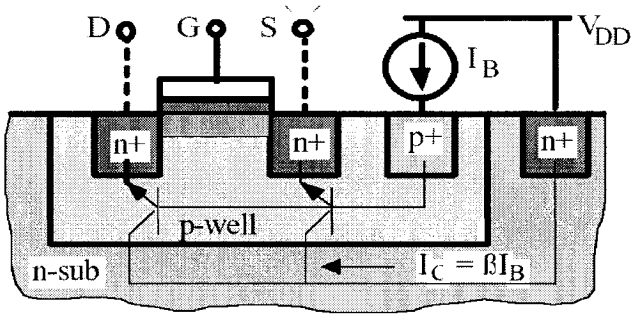

Figure 3.8 Cross-Section of a forward-biased NMOS transistor.

3.2.3 Input matching

Most RF instruments and coaxial cables have standardized impedances of 50 ohms, thus the input stage of the LNA is required to match to 50 ohms to have no power reflection. Without adding thermal noise introduced by real resistor, the common-source input transistor with inductive source degeneration is often employed and shown in Figure 3.9 Neglecting the gate drain capacitances, the input impedance is:

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{C_{gs} s} + s(L_s + L_g) + R_g \qquad (3.8)$$

Where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_1, respectively. L_g and L_s are the gate and source inductors and R_s is the effective gate resistance of M_1 given by $R_g=R_0/(3n^2L)$ where R_0 is the sheet resistance of the gate ploysilicon, W and L are the gate width and length of the transistor M_1 respectively and n is the number of fingers.

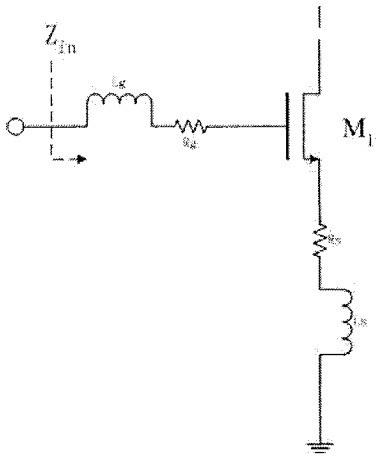

Figure 3.9 Common Source Input Stage with inductor degeneration.

At the resonant operating frequency (ω_0), the input matching criteria requires that:

$$Z_{in} = R_s = \omega_T L_s \qquad (3.9)$$

The C_{gs} source degeneration inductance L_s is chosen together with $?_T$ to provide the desired input resistance R_s (50 ohms), the real term can be made equal to 50 ohms without the existence of a real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met. As technology improves, ω_T increases this leads to a reduction in inductor L_s size, making the system more suitable for on-chip integration. The value of L_s is about 1nH and it is implemented on chip.

3.2.4 Minimum Noise Figure Design

An LNA determines the performance of the communication systems. It needs higher linearity and sufficient gain to overcome the next stage noise but not to overload. In our circumstances, F_1 is the noise factor of the LNA and G_1 is the gain of the LNA which

implies that higher gain and lower noise of LNA will lower the total noise of the system. Noise figure represents how much the given system degrades the signal-to-noise ratio. The minimum noise figure is achieved according to: [24]

$$F_{\min} = 1 + \frac{\omega}{\omega_t}\sqrt{\gamma\delta\xi(1-|c|^2)} \tag{3.10}$$

If δ were zero, the minimum noise figure would be 0dB.

3.2.5 Proposed Common-Source Common-Gate topology

The cascode topology with inductive source degeneration is a popular configuration for LNA design, but has problem working for very low voltage supply applications because the power supply must satisfy the following requirement:

$$V_{DD} + |V_{SS}| \geq 2V_{thn} \tag{3.11}$$

Where V_{DD} and V_{SS} are the positive and negative power supply, respectively and V_{thn} is the threshold voltage of the each of the NMOS transistor in fig 3.4.

To remove the factor 2 in Equation (3.11), cascode topology is replaced by single transistor configuration. Therefore, two single transistor cascaded stages with inductive source degeneration are designed for the LNA as shown in fig 3.9. The proposed cascade common-source common-gate topology offers a lower power supply than that of cascade LNA while the gain can be maintained.

The proposed common-source common-gate LNA is shown in fig 3.10. In the first stage of complete schematic, the size of common-source transistor M_1, off-chip inductance and on-chip input gate inductance L_{g1} at the source are used to achieve optimum input

matching and noise figure. The LC tank (L_{d1}, C_{d1}) of M_1 is set to achieve a resonance frequency and provide a DC bias current path and a high impedance branch to force the RF signal to flow into the source of the common-gate transistor M_2 through a big DC coupling capacitance. L_{s2} are connected to the source to improve the noise figure and stability. However, the S_{11} gets worse when L_{s2} increases. Source-follower buffer M_3 is employed for measurement purpose to drive an external 50 ohms load. The LNA output matching uses on-chip resistor R_{g3}, R_{s3} and metal-to-metal capacitor C_{s3}. Transistor M_0 with R_b for ac blocking forms the biasing circuitry. A bulk-source voltage V_{BK} is employed to forward-bias the well-source junction of transistors M_1 and M_2. The threshold voltage of the transistors decreased and the undesired bulk current remains below 100uA.

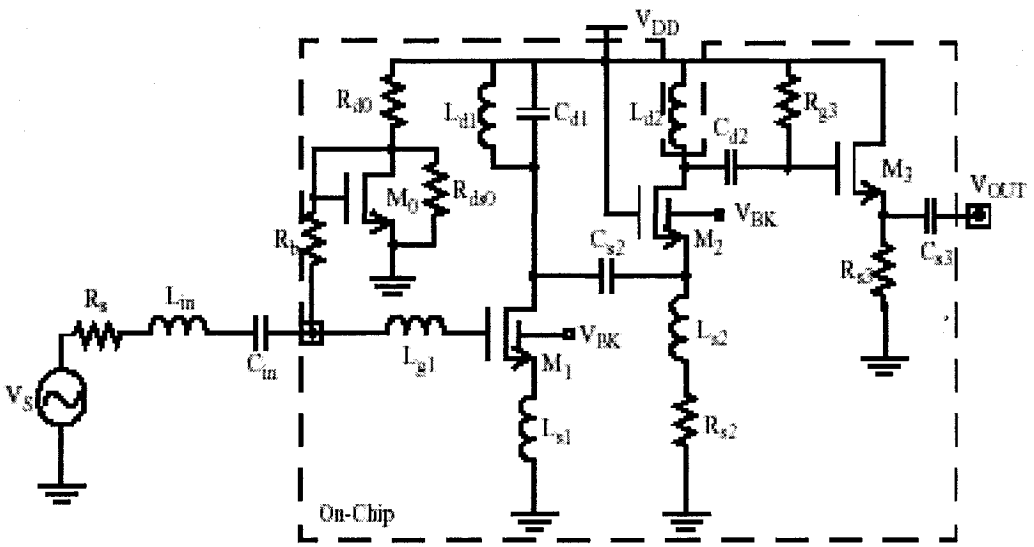

Figure 3.10 Complete schematic of proposed common-source, common-gate LNA

3.3 Conclusion

In this chapter, the popular cascode design is presented and analyzed. Then, some low voltage topologies are presented. Different topologies of signal transistor and conventional cascode are described to show the improvements of proposed design. Finally, a simple common-source common-gate topology is proposed to be the choice of low voltage designs with good performances in all aspects, when compared to other architectures.

Chapter 4 RF Layout Issues and Techniques

This chapter provides the layout techniques for RF design. All important layout issues are discussed.

Designing CMOS RF circuits operating at frequencies greater than 1 GHz in a standard CMOS process requires the following:

i) Proper modeling of high quality passive components.

ii) Good RF layout techniques, in order to minimize performance degradation.

In this chapter, the layout techniques adopted in this work are addressed. Detailed measurement results of sub-1V CMOS LNA's are presented, including a frequency and gain tuneable LNA.

4.1 Layout Techniques

Apart from proper modeling of integrated passives, layout is another important step in optimizing high frequency designs. Poor layout could result in large discrepancies between the actual and expected performance. The layout of a 5GHz CMOS LNA is shown in Figure 4.1, and is used to illustrate the RF layout techniques used in this work.

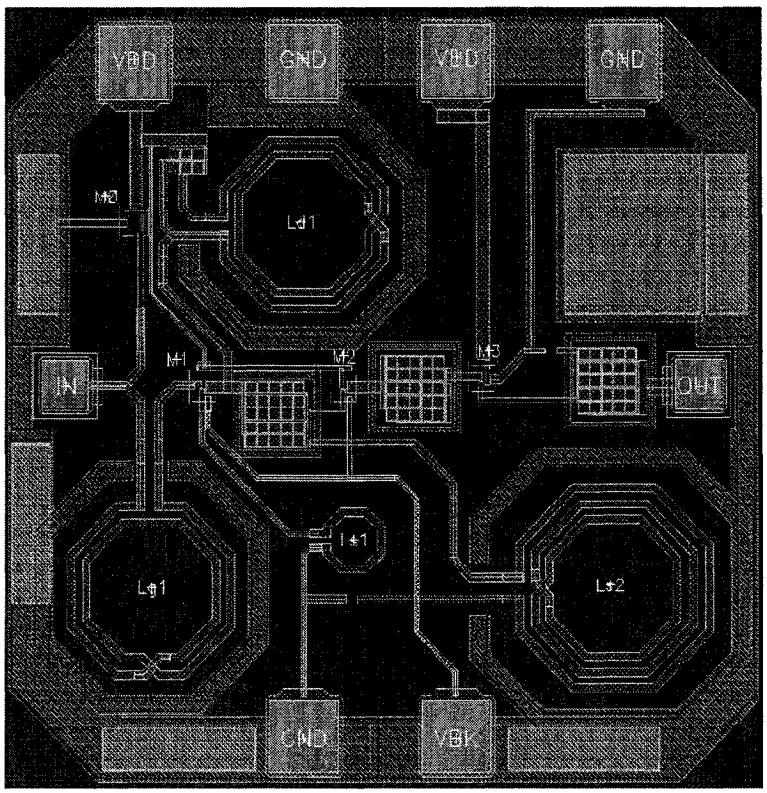

Figure 4.1 Layout of LNA for 5GHz amplifier.

The layout is done in a uni-directional fashion, i.e. no signal returns close to its origin, in order to avoid coupling back to the input. The RF input and output ports are placed on opposite sides of the chip to improve port-to-port isolation. Since on-chip probing is used to measure the performance of this LNA, standard Ground-Signal-Ground (GSG) probes are used at both the input and output RF ports. The signal pads (i.e. RF input and output) are implemented using the top metal layer only, attempting to reduce the impact of their parasitic capacitors on the RF performance. In order to minimize the effect of substrate noise on the system, a solid ground plane constructed using a low resistivity metal-1 material is placed between the signal pads (metal-6) and the substrate.

Since the operation of inductors involves magnetic fields, they can affect nearby signals and circuits, and cause interference. Therefore, inductors are placed far apart from each other, as well as from the main circuit components, with reasonable distance. Furthermore, traces connected to all inductors are made wide enough to minimize the series parasitic resistances and inductances, and thus avoid inductor Q degradation. Ideally, all interconnections should be as short as possible in order to minimize their impact. However, this is not always possible, especially due to the large geometrical structure of the inductors when compared to other components such as transistors and resistors. When long interconnects become unavailable in the layout, an in-house high frequency modeling routine is used in order to accurately estimate the parasitic introduced. The main purpose of this routine is to increase the accuracy between the simulated and measured RF performances, by incorporating unexpected layout dependent parasitics (e.g. inductances and resistances) [26]. Finally, line widths are set according to RF design guidelines, keeping DC traces thin to present high impedances to RF signals, and AC connections wide and as short as possible. "Round" corners are used, instead of sharp ones, for interconnects in order to minimize signal reflections at RF, as illustrated in Figure 4.1.

4.2 Design of RF Passive Components [24]

RF circuits generally have many passive components. Passive components such as inductors and capacitors play an integral part in the performances of circuit building

blocks in a transceiver, especially at high frequencies. In particular, passive devices are used for impedance and noise matching LNA designs, which are the main focus of this thesis.

4.2.1 Passive Devices in Si CMOS Technologies

An important parameter to consider when discussing passive devices is the quality factor (Q). The quality factor is generally defined as:

$$Q = 2\pi \frac{E_{store}}{E_{diss}} \tag{4.1}$$

Where E_{store} is energy stored in per cycle, and E_{diss} is the energy dissipated per cycle in a device.

The higher the Q factor, the lower the loss of a passive device. This definition is the most relevant when discussing inductors and capacitors, as such devices are meant to store energy, while dissipating little to no energy in the process. Thus, ideal inductors and capacitors having zero energy loss would have infinite Q's, whereas practical devices normally have finite Q's.

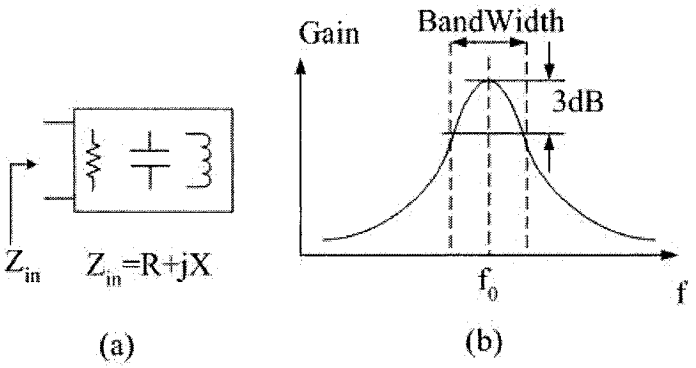

Figure 4.2 (a) Input impedance of a practical passive device (b) Quality factor of an LC resonant tank.

Based on the definition in Equation 4.1, the quality factor of a practical inductor can be expressed as:

$$Q = \frac{X_{ind}}{R_{ind}} = \frac{\omega L}{R} = \frac{2\pi fL}{R} \tag{4.2}$$

And the quality factor of a practical capacitor can be expressed as:

$$Q = \frac{X_{cap}}{R_{cap}} = \frac{1}{\omega CR} = \frac{1}{2\pi fCR} \tag{4.3}$$

Where X is the reactive component of a passive device storing energy, and R is the resistive component of a passive device dissipating energy (Figure 4.2(a)).

Apart from measuring the performance of a passive device, the quality factor can also measure the selectivity of a resonant circuit. Due to the band-pass nature of a resonant tank, the quality factor of an LC-tank can be expressed as follows (among several other possible definitions):

$$Q = \frac{f_0}{BW_{3dB}} \tag{4.4}$$

Where f_0 is the resonant frequency and BW_{3dB} is the 3 dB bandwidth of the response, as shown in Figure 4.2(b).

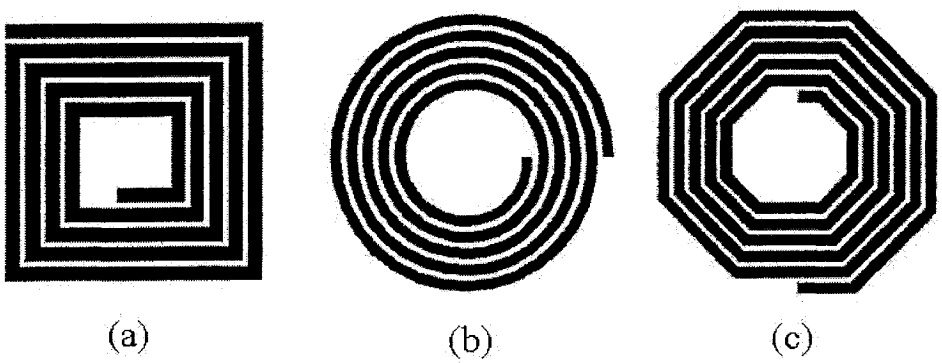

Figure 4.3 Inductor geometries (a) square (b) spiral (c) octagonal.

4.2.2 Common Inductor Layout Topologies

The common inductor layout geometries include square, octagonal, and circular inductors [24], as shown in Figure 4.3. In addition to the layout geometry, some variants have been shown to improve performance, such as inductors with lower ground plane, usually a broken polysilicon plane (Figure 4.3a), and symmetric layouts whenever 2-port inductors are needed (Figure 4.3b).

The integrated inductor exhibits the capacitive and resistive parasitics. For simulation purpose a simplified model as shown if Figure 4.3 was used: R is total parasitic series resistance, R_s is parasitic resistance to substrate, C is the total parasitic capacitance to substrate and L is inductance. Their values are given by ASITIC calculation tool provided by UC. Berkeley.

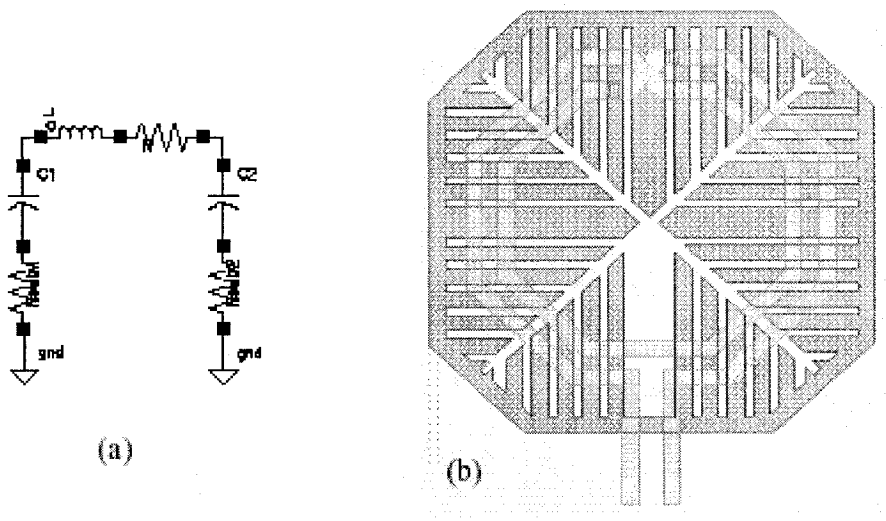

Figure 4.6 Inductor model: (a) simplified model (b) hollow patterned ground-shield inductor.

4.2.3 Asitic Technology [27]

Asitic is used for analysis and simulation of spiral inductors and transformers for ICs. It is CAD tools that aid the RF circuit designer to optimize and model spiral inductors, transformers, capacitors, and substrate coupling. The conductive substrate plays an integral part in determining the quality factor and self-resonance frequency of monolithic passive devices. ASITIC calculations include the electrically induced losses and coupling as well as the magnetically induced eddy current losses. Skin effect and proximity effects, or eddy currents in the metallization, are also included. We use asitic tool to design inductor in our LNA design.

4.3 On-chip RF-isolation Technology

On-chip isolation is becoming increasingly important due to higher integration levels, higher frequencies, and tighter specifications for next-generation products. Higher integration not only results in more transistors switching, and subsequently more noise creation, but it also puts noisy and sensitive components together on the same chip that, in the past, were on separate chips. At higher frequencies, noise now couples more easily from place to place. Isolation provided by wells is reduced, and package inductance becomes critical. The package impedance at GHz frequencies may cause on-chip AC grounds to appear to float. When the tighter specifications of next generation products, such as 3G cellular, are added to the picture, the RF designer must be both knowledgeable and creative to find an effective solution. An understanding of the impact of the process technology, grounding effects, and guard rings, shielding, decoupling, and package inductance is necessary to optimize isolation.

4.3.2 Technology Impacts

Most silicon-based RF chips are fabricated in bipolar, BiCMOS, SiGe, or CMOS processes using a lightly doped bulk, p-type substrate. Heavily doped substrates, most commonly used for large digital designs, such as microprocessors, where latch-up concerns dominate isolation and the extra wafer cost can be justified, will not be covered in this article. A lightly doped substrate is highly resistive, which typically means a resistivity of around 12 Ohm-cm or a doping concentration around $4x10^{14}$ cm^{-3} for a p-

type substrate. Experienced designers will often be able to achieve a few more dB of isolation using a lightly doped substrate rather than a heavily doped substrate.

The buried layers and sinker are roughly four orders of magnitude more conductive than the bulk substrate. If the sinker and buried layer are connected to a low-impedance AC ground, they may form a shield and draw carriers away from devices located inside the region. However, buried layers may also provide a low-impedance path for noise to travel into a sensitive area. In this case, the buried layer must be broken to increase the isolation.

In Figure 4.7, the break in the buried layer combined with the addition of a double guard ring provided a 20 times improvement in the isolation.

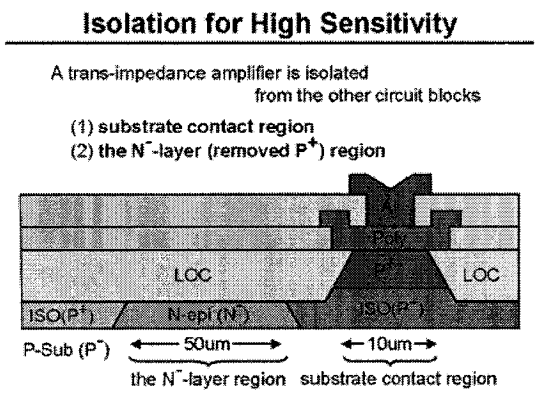

Figure 4.7 Example of breaking the buried layer to reduce coupling through the ISO (P+) region.

4.3.2 Grounding Effects

It is common practice among analog designers to have separate supplies for analog and digital sections of the chip to isolate the analog circuitry from the switching noise

introduced on the digital supplies. The same technique is useful to isolate different RF blocks. Dividing a chip into sections with different substrate grounds will attenuate noise coupling from area of a chip to another.

Although a seal ring is not typically grounded and is therefore not a grounding effect, it can decrease the isolation achieved by separating supplies. In some fabrication processes, a metallized ring contacting the substrate is placed around the outside of the chip to seal the edge from alkali ions that may enter the field oxide and affect the yield. This ring may act as a low-impedance path for noise coupling between different regions on the chip. If design guidelines allow the edge seal to be broken, the ring should be severed where it provides a coupling path between different supply regions.

4.3.3 Guard Ring

In a lightly doped substrate, as contrasted with a heavily doped substrate, guard rings typically provide effective isolation—this assumes that care has been taken to ensure that the guard ring is connected to a quiet supply. Guard rings around a sensitive circuit help to decouple noise from the circuit and ensure that noise will couple equally into both sides of a differential design. Guard rings around a noise source provide a low-resistance path to AC ground for the noise and help minimize the amount of noise injected into the substrate [24]. The efficiency of guard rings depends on the noise frequency and package inductance.

Backside connections to the substrate can be viewed, in a very simplistic manner, as a type of guard ring. The effectiveness of the backside connection will depend on the

inductance value between the backside and ideal ground, and on the frequency of the noise. Certain packages provide a very low inductance path from the backside of the chip to the board ground. In these cases, a conductive connection to the backside of the chip can add considerable isolation. However, if the package is such that a backside connection is grounded through down-bonds to the paddle and significant inductance exists in the package, the backside connection may make matters worse. At higher frequencies, the backside connection will then act as a floating conductor to spread noise across the ship.

Guard-ring width also affects isolation. In some cases, the width of the guard ring is similar to the depth of the substrate, and the package provides a very low impedance path to ground.

4.3.4 Shielding

Proper shielding for sensitive signal lines and passive components is an integral part of effective analog/RF IC layout. The challenge is to determine the appropriate shield layer, bias potential, and layout pattern. Sensitive signal buses are often laid out with alternating signal and shield lines to prevent crosstalk through lateral and fringing electric fields. To isolate the signal lines from the substrate, n-well or diffusion layers can be placed under the lines to prevent noise coupling.

In general, shielding increases parasitic capacitance, since the field lines from the signal wires terminate at a closer distance on the shielding before they reach another signal line or the substrate. The bias potential of the shield should be tied to the reference of the

signals. The effectiveness of shielding also depends on the signal operating frequency. In general, there is a trade-off between a lower shield parasitic capacitance and a higher series resistance. As frequency increases, a large series resistance causes the shield to be ineffective.

Passive components such as inductors and capacitors occupy substantial die area and thus are susceptible to coupling through the substrate. In a p-type substrate, the n-well can be placed under capacitors, inductors, or bond pads to provide a low-capacitance shield. However, the well resistance, typically on the order of 1K Ohm/sq., may be too large to be effective at high frequencies. To lower shield resistance, you can use a diffusion or polysilicon layer. Inductors are a special case, since the magnetic field will induce eddy currents in a conductive shield beneath the inductor. Inserting a pattern of slots in the shield perpendicular to the inductor traces, shown in Figure 4.8, will prohibit the eddy current by creating a "patterned ground shield"[28].

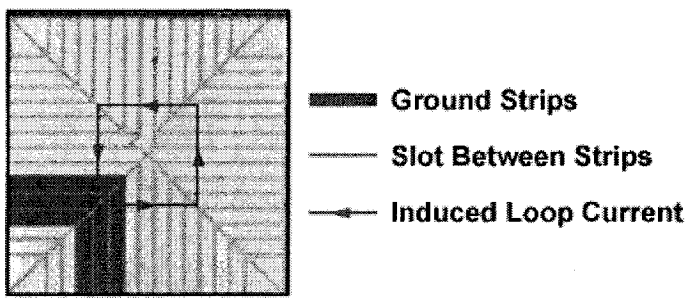

Figure 4.8 Close-up photo of a patterned ground shield.

4.3.5 On-Chip Decoupling

Decoupling capacitance is not always thought of as something that increases the isolation between two points, but it serves the same role. Isolation is desirable to attenuate noise coupling from one portion of a chip to another. If decoupling capacitance can reduce the amount of noise created by supplying local charge for nearby switching and thus lowering the peak current drawn across the package inductance, careful use of this capacitance essentially isolates a sensitive circuit that no longer sees the same supply and substrate noise levels.

Meeting the specifications of the next generation RF products requires an experienced designer who understands a variety of isolation techniques. Process technology options, grounding strategies, guard rings, shielding, decoupling capacitance, and package parasitics all play an important role in isolation. However, it is the combination of these factors that ultimately determines whether the final design will meet the product specifications.

4.4 Conclusion

In this chapter, the RFIC layout issues are discussed. Layout is a very important step in optimizing high frequency designs. Poor lay out could result into a non-working circuit. Guidelines for RF layout techniques towards successful LNA implementations are presented.

Chapter 5 Simulation Results and Discussion

This chapter provides the detailed simulation results and comparisons of different CMOS LNA. The simulation results confirm the functionality of proposed common source common gate cascade topology.

5.1 A 0.65V, 2.4GHZ CMOS Low-Noise Amplifiers Design with Noise Optimization

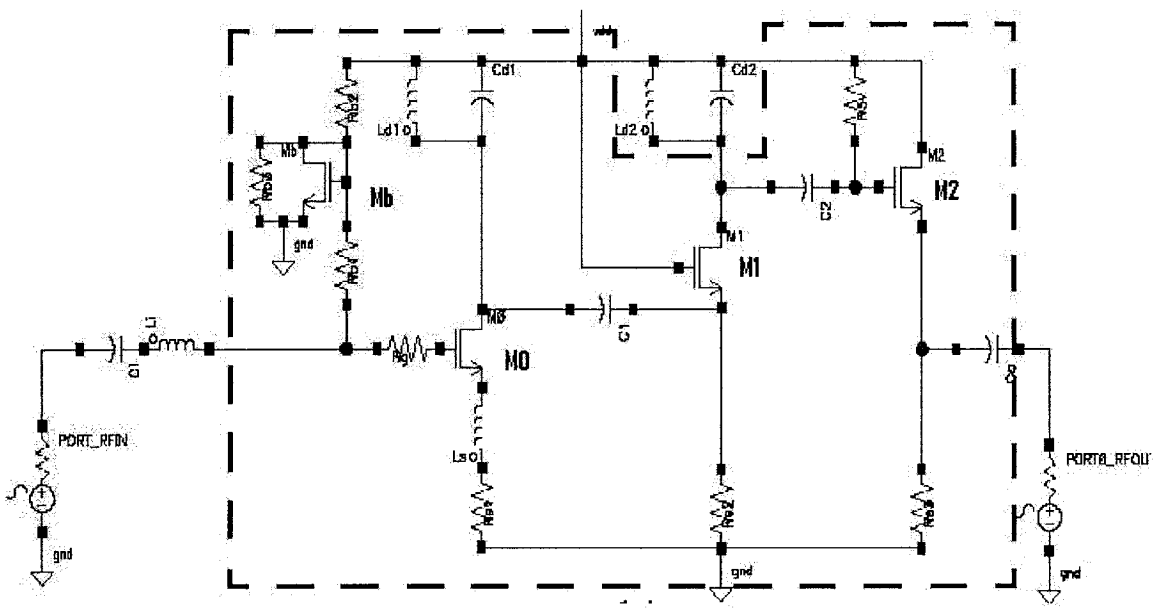

Figure 5.1 Complete schematic of proposed cascaded common-source, common-gate 0.65V, 2.4GHz LNA

The complete circuit is shown in Figure 5.1. The LNA first stage M_0 is inductively

degenerated representing the common-source amplifier followed by M_1 configured as common-gate device. M_b sets the dc bias for M_0. M_2 is configured as the buffer stage for LNA output matching. C_1 between M_0 and M_1 is acting as a coupling capacitance to block DC and provides ac path to let RF signal flow into the source of common-gate transistor M_1. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip. As shown in Figure 5.1 only the framed components are on-chip.

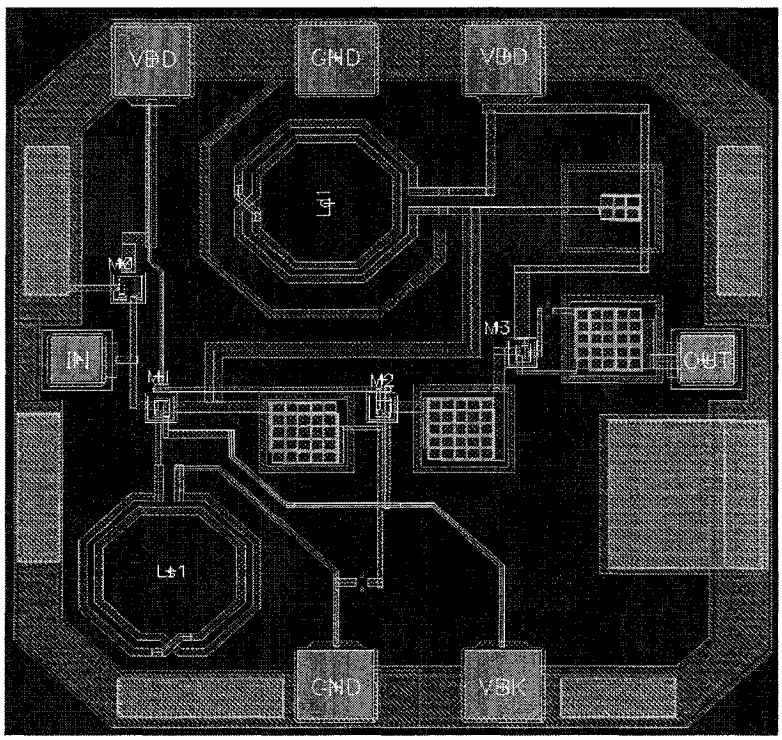

Figure 5.2 Layout of proposed LNA for 0.65V 2.4G amplifier.

The layout of the LNA is shown in Figure 5.2. The chip area is 0.9mm x 0.9mm. Figure 5.3 shows a forward gain (S21) of 27 dB at 2.4GHz. A low noise figure of 1.1 dB at 2.4 GHz is achieved after noise optimization in Figure 5.4. The S-parameters of the LNA are illustrated in Figure 5.5 and 5.6. The input matching S11 is -12dB. The S22 shows a good

output match with the output buffer which achieves -30.7dB, this maximizes the power transfer from the LNA to the 50 ohms input impedance of the next stage. The IIP3 simulation result of the LNA is shown in Figure 5.7. A two-tone signal, which is chosen close to each other, has been applied to the input port. The input-referred third-order intercept points (IIP3) is -30.0dBm.

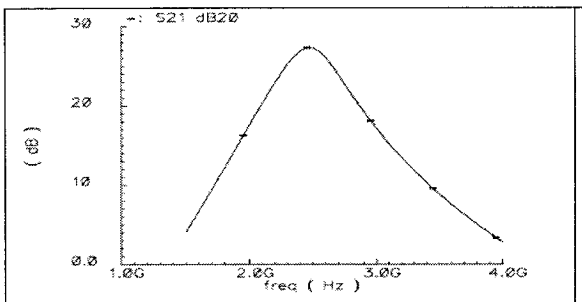

Figure 5.3 Power gain of proposed LNA

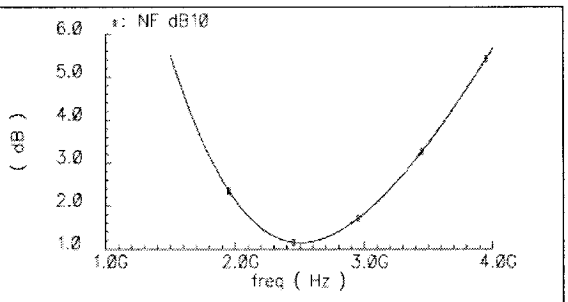

Figure 5.4 Noise figure of proposed LNA

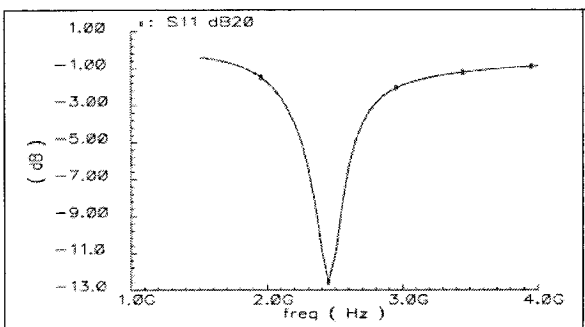

Figure 5.5 S11 of proposed LNA

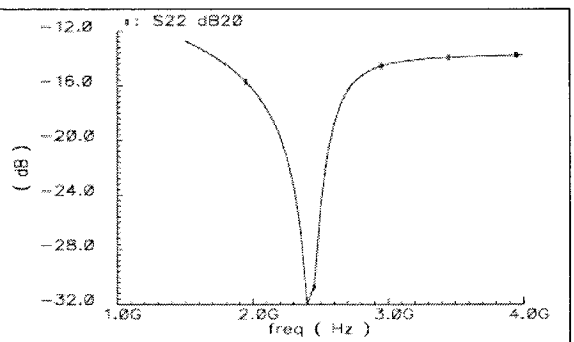

Figure 5.6 S22 of proposed LNA

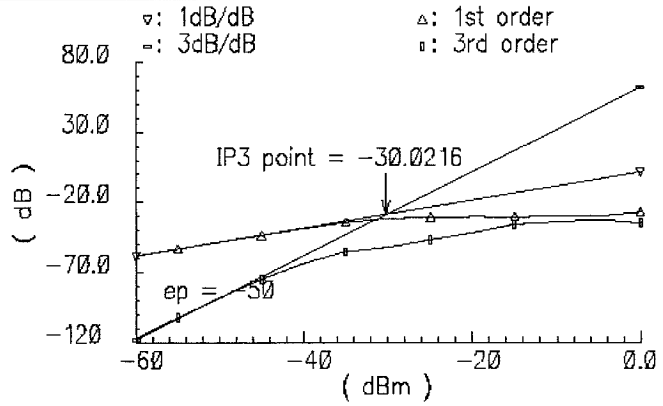

Figure 5.7 IIP3 of proposed LNA

Table 5.1 shows that the performance of the proposed LNA clearly excels over other work in terms of low voltage, low power, and low noise figure operation.

Table 5.1: Performance summary of 2.4GHz LNA

Reference	[10]	[11]	[12]	[13]	[14]	[proposed]
Tech(um)	-	0.5	0.18	0.18	0.3	0.18
Freq.(GHz)	2.4	2.4	2.4	2.4	2.4	2.4
NF(dB)	1.8	2.4	1.6	4.0	2.0	1.1
S21(dB)	15	19	25	12	19	27
IIP3(dBm)	-	-	-8	-2	-	-30
Supply(V)	5.0	3.0	1.5	1.8	-	0.65
Power(mw)	-	9	16	14.3	40.8	4.6

5.2 Comparison of cascode and proposed 2.4GHz LNA

The comparison of the simulation results of the proposed and *cascode LNA* configuration and the proposed cascade structure are discussed through Figures 5.8 to Figure 5.12. From these figures, the proposed circuit achieves a power gain that is 10dB higher than the *cascode LNA*. The proposed LNA consumes 4.6mw but the *cascode LNA* consumes 5.6mw. In the 2.4GHz band the proposed circuit has better performance than the *cascode LNA*.

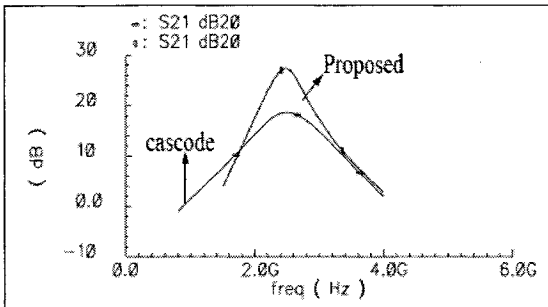

Figure 5.8 Power gain of proposed LNA vs Cascode LNA

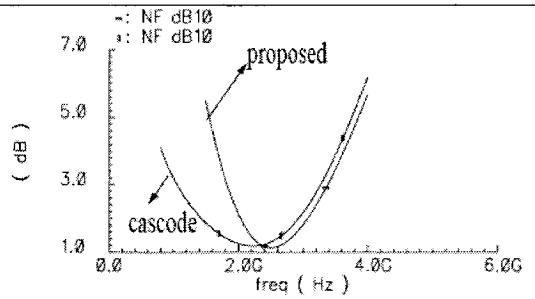

Figure 5.9 Noise figure of proposed LNA vs Cascode LNA

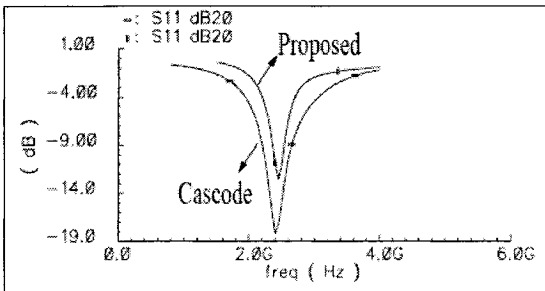

Figure 5.10 S11 of proposed LNA vs Cascode LNA

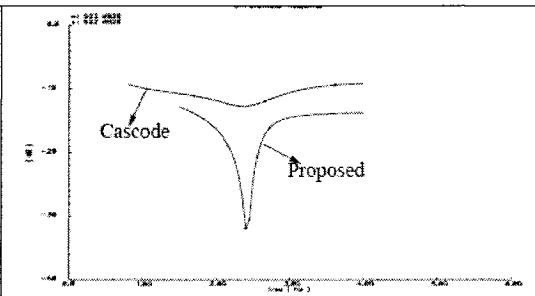

Figure 5.11 S22 of proposed LNA vs Cascode LNA

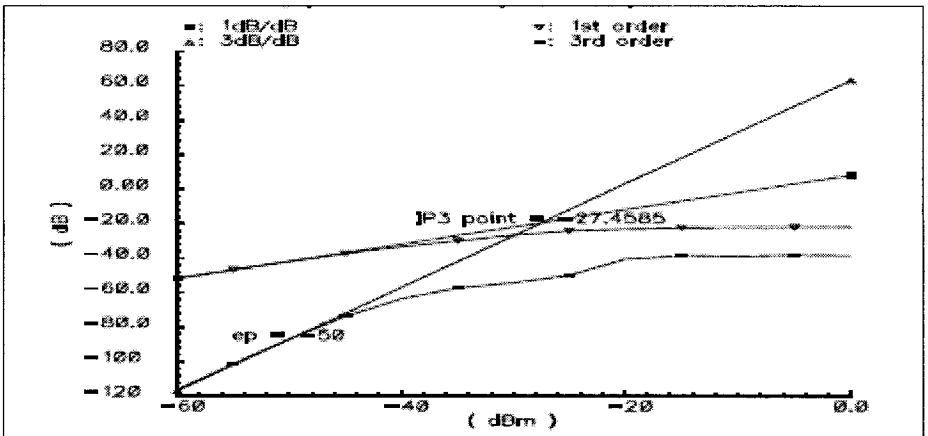

Figure 5.12 IIP3 of Cascode LNA

5.3 A 0.65 V CMOS Low-Noise Amplifier Design for 5GHz RF Applications

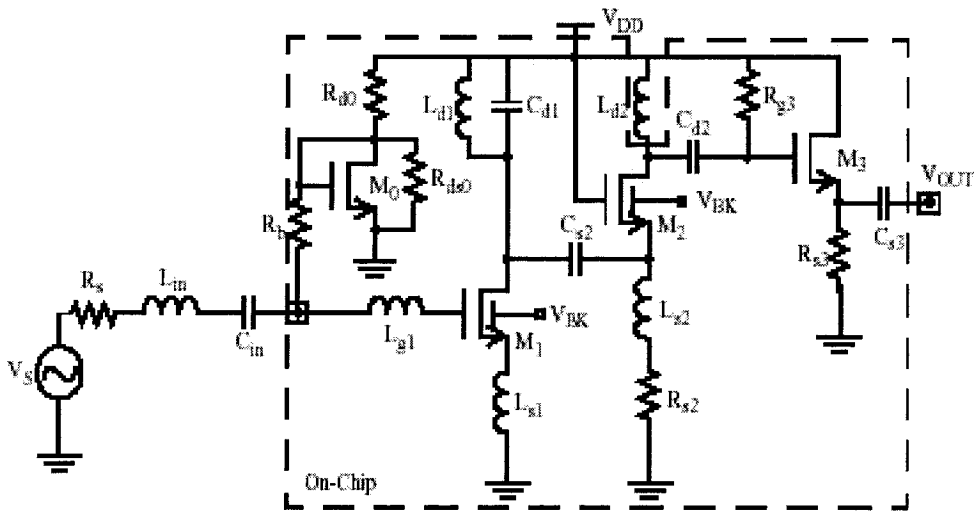

Figure 5.13 Complete schematic of proposed common-source, common-gate LNA for 0.65V amplifier at 5GHz.

For 5 GHz band, the 0.18um TSMC analog/RF CMOS process was used for implementation of the design. A deep N-well process, depicted in Figure 5.14, is employed to provide separate substrate connections and offering increased isolation from substrate noise for NMOS transistors. In addition, the bulk voltage can be forward-biased to reduce the threshold voltage of the NMOS transistors.

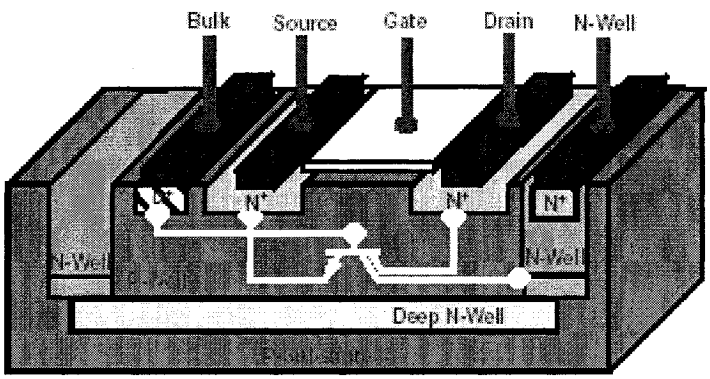

Figure 5.14 Cross section of a deep N-well

Several layout issues have been taken care of. First, grounded-shield plane is laid under the inductor to minimize the magnetic coupling to the substrate. Second, hollow inductor is used to reduce parasitic capacitance and resistance. Third, grounded guard rings with substrate connections surround each capacitor, transistor and three inductors. Moreover, each transistor has an extra N-well guard ring with V_{DD} connection surrounding the grounded guard ring. Forth, a quiet N-well under the input and output signal pads was placed to isolate the RF signals from the substrate.

The proposed circuit is shown in Figure 5.13 In the first stage, the size of common-source transistor M_1, off-chip inductance (L_{in} = 16 nH) and on-chip input gate inductance L_{g1} at the drain are properly chosen to tune the LNA to the desired band and match real

part of input impedance to 50Ω source impedance. In addition, L_{s1} at the source is used to achieve optimum input matching and noise figure. The LC tank (L_{d1},C_{d1}) of M_1 is set to achieve a resonance frequency at 5GHz and provide a DC bias current path and a high impedance branch to force the RF signal to flow into the source of the common-gate transistor M_2 through a big DC coupling capacitance (C_{s2} = 5 pF). L_{s2} are connected to the source to improve the noise figure and stability. However, the S_{11} gets worse when L_{s2} increases. This effect limits the amount of inductance (L_{s2} = 2 nH). Source-follower buffer M_3 is employed for measurement purposes to drive an external 50Ω load. The LNA output matching uses on-chip resistor R_{g3}, R_{s3} and metal-to-metal capacitor C_{s3}. Transistor M_0 with 20KΩ resistor R_b for ac blocking forms the biasing circuitry. A bulk-source voltage V_{BK} is employed to forward-bias the well-source junction of transistors M_1 and M_2. The threshold voltage of the transistors decreased from 0.54V to around 0.4V and the undesired bulk current remains below 100uA for bulk-source voltages as high as 0.65V. The layout is shown in Figure 5.15. The chip area is 1mm x 1mm.

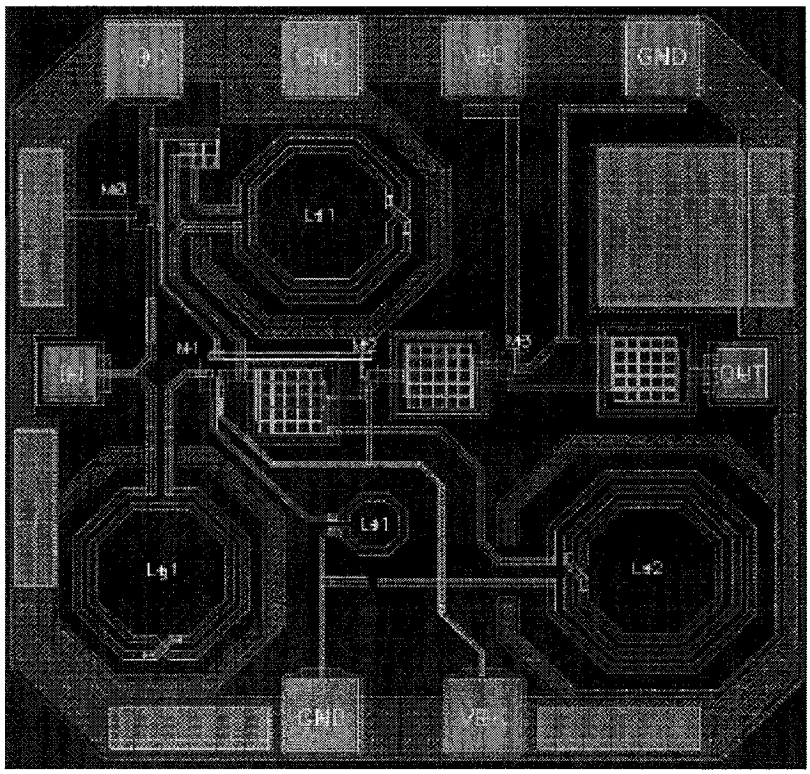

Figure 5.15 Layout of LNA for 0.65V 5G amplifier.

The input and output reflections (S_{11}, S_{22}) are presented in Figures 5.18 and 5.19 respectively. The S_{22} shows a good output match with the output buffer for both LNAs which achieves below -20dB. With the same input stage configuration for both circuits, the S_{11} are similar and less than -10dB. Figure 5.16 depicts a power gain of 20dB. The noise figure shows in figure 5.17 is 1.4dB. A two-tone signal of 5GHz with 20 KHz difference has been applied to the LNA input port. The IIP3 simulation result of the LNA is shown in Figure 5.20. A two-tone signal which is chosen close to each other has been applied to the input port. The input-referred third-order intercept points (IIP3) is -29dBm. This work is placed alongside with other reported 5GHz LNA in Table 5.2.

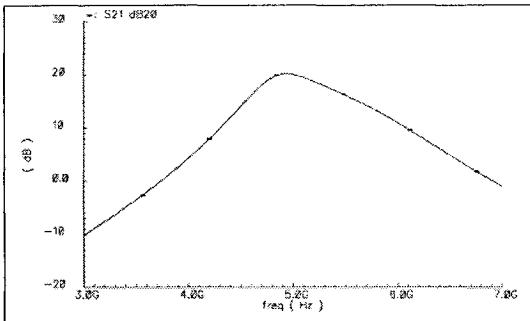

Figure 5.16 Power gain of proposed LNA

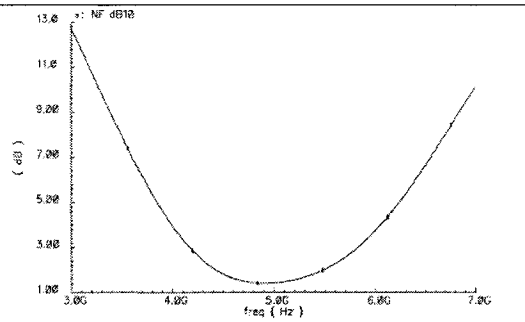

Figure 5.17 Noise figure of proposed LNA

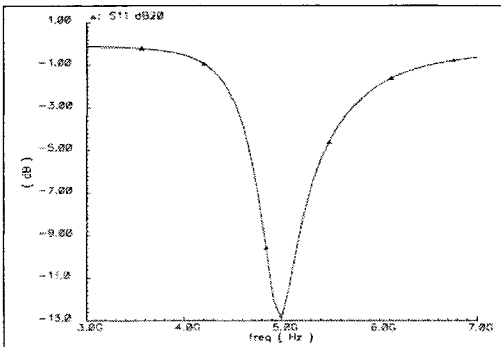

Figure 5.18 S11 of proposed LNA

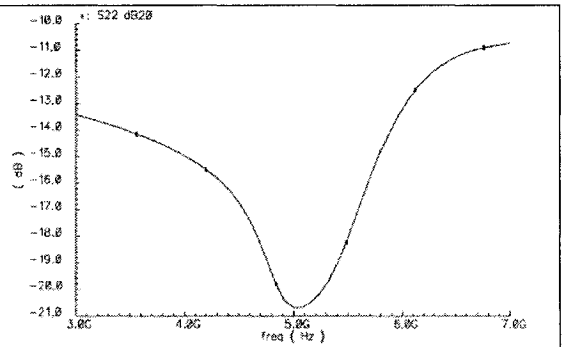

Figure 5.19 S22 of proposed LNA

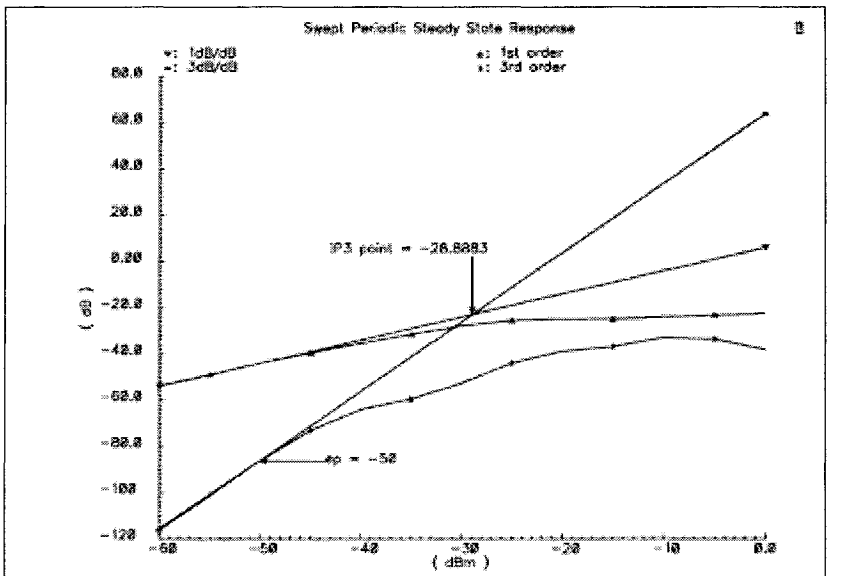

Figure 5.20 IIP3 of proposed LNA

Table 5.2: Performance summary of 5GHz LNA

Reference	[5]	[6]	[7]	[8]	[9]	[Proposed]
Tech(um)	0.35	0.25	0.18	0.18	0.18	0.18
Freq.(GHz)	5.2	5.2	5.2	5.2	5.8	5.0
NF(dB)	2.45	2.1	2.0	1.4	2.5	1.4
S21(dB)	19.3	17	15.5	16.6	13	20
S11(dB)	N/A	-10	-11	-13	-5.3	-15
S22(dB)	N/A	N/A	-10	N/A	-10.3	-21
IIP3(dBm)	N/A	N/A	-4.3	0.6	N/A	-29
Supply(V)	3.3	N/A	1.8	1.8	1	0.65
Power(mw)	26	N/A	10.4	16.2	22	1.9

5.4 Comparison of the proposed and cascode 5GHz LNA

The comparison of the simulation results of the cascode and proposed circuits are shown in Figure 5.20 to 5.24. From these figures, the proposed circuit has a higher power gain of 2dB than the cascode circuit. The proposed circuit noise figure is 0.2dB less than the cascode LNA circuit. The proposed circuit achieves the lowest voltage supply and power consumption. The proposed circuit consumes only 1.9mw from 0.65v power supply.

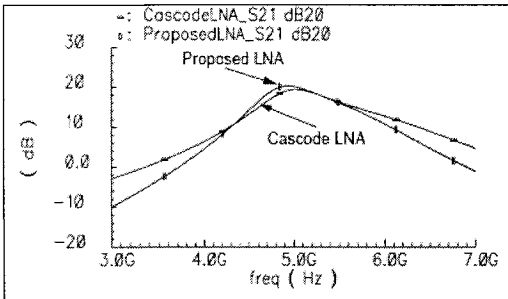

Figure 5.20 Power gain of cascode and proposed LNAs

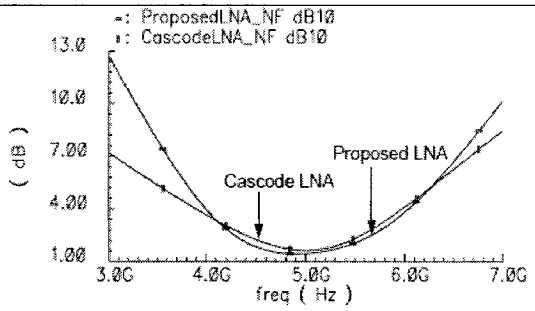

Figure 5.21 Noise figure of cascode and proposed LNAs

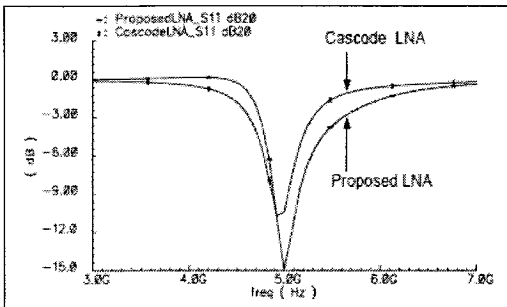

Figure 5.22 S11 comparison of cascode and proposed LNAs

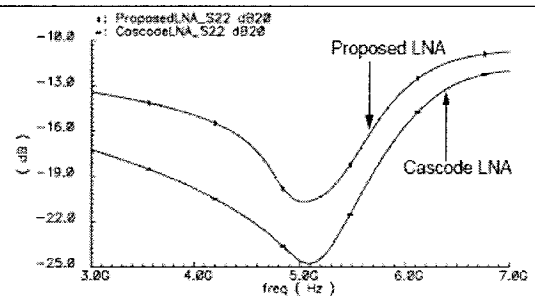

Figure 5.23 S22 comparison of cascode and proposed LNAs

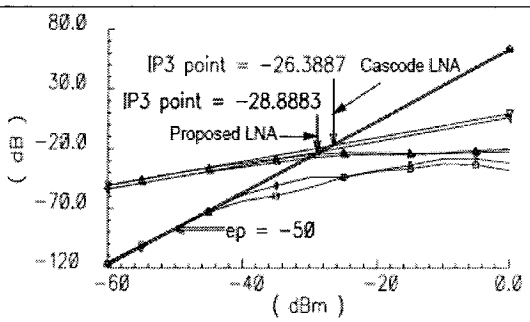

Figure 5.24 IIP3 comparison of cascode and proposed LNAs

5.5 Conclusion

In this thesis, a CMOS low noise amplifier using common-source inductive source degeneration followed by common-gate configurations is proposed. Spectre simulation using 0.18um CMOS technology shows a noise figure of 1.1dB, high power gain of 27dB at 2.4 GHz and a proposed topology is suitable for low poser supply application and works good at 0.65V voltage supply. The results show a low noise figure of 1.4 dB, high power gain of 20 dB and low power consumption of 1.9 mW from 0.65 V power supply at 5GHz.

Chapter 6 Conclusions

This chapter summarizes the performances of the CMOS LNA's in this work, and gives suggestions for the future work.

6.1 Achievements

In this work, a new topology for very low voltage high gain low-noise-amplifier (LNA) design has been proposed. This achieved better performance than other various topologies. Most of LNA designs have aimed at low power and high gain based on LNA fundamentals. By analyzing noise figure, non-linear distortion, input matching and gain compression, optimized solution has been reached after several iterations. The proposed design uses two stages of common source and common gate. Using this topology, various parameters of the circuit are designed to achieve high gain LNA RF performance at low voltage (sub 1 volt) with different frequencies with low power. Also, layout techniques and proper modeling based on high frequency CMOS RF circuits has been discussed to optimize the design of the circuits. Using these techniques, the LNA circuits are designed to provide high gain, low noise, and low power dissipation and low voltage power supply amplifiers. Tables 6.1 and 6.2 summarize the performances of CMOS LNA's reported in this work

The CMOS low noise amplifiers (LNA' s) using 0.65V power supply at 2.4GHz and 5 GHz respectively, achieved (by simulation) noise figure less than 1.1dB, and power

dissipation less than 4.6mw. The LNA can be used in systems such as blue tooth, wireless local networks, home satellite, and voice communication cell phones.

Table 6.1: Complete Performance summary of 5GHz LNA

Reference	[5]	[6]	[7]	[8]	[9]	[Cascode]	[Proposed]
Tech(um)	0.35	0.25	0.18	0.18	0.18	0.18	0.18
Freq.(GHz)	5.2	5.2	5.2	5.2	5.8	5.0	5.0
NF(dB)	2.45	2.1	2.0	1.4	2.5	1.6	1.4
S21(dB)	19.3	17	15.5	16.6	13	18	20
S11(dB)	N/A	-10	-11	-13	-5.3	-11	-15
S22(dB)	N/A	N/A	-10	N/A	-10.3	-25	-21
IIP3(dBm)	N/A	N/A	-4.3	0.6	N/A	-26	-29
Supply(V)	3.3	N/A	1.8	1.8	1	0.85	0.65
Power(mw)	26	N/A	10.4	16.2	22	3.2	1.9

Table 6.2: Complete Performance summary of 2.4GHz LNA

Reference	[10]	[11]	[12]	[13]	[14]	[Cascode]	[Proposed]
Tech(um)	-	0.5	0.18	0.18	0.3	0.18	0.18
Freq.(GHz)	2.4	2.4	2.4	2.4	2.4	2.4	2.4
NF(dB)	1.8	2.4	1.6	4.0	2.0	1.2	1.1
S21(dB)	15	19	25	12	19	19.5	27
IIP3(dBm)	-	-	-8	-2	-	-27.4	-30
Supply(V)	5.0	3.0	1.5	1.8	-	0.8	0.65
Power(mw)	-	9	16	14.3	40.8	5.6	4.6

6.2 Future work

- The CMOS low noise amplifier may be fabricated and tested.
- The proposed common source and common gate topology maybe used to design in different CMOS processes to get adequate performance for RF Circuit operating at 1-5 GHz.
- A very low power LNA maybe designed by using proposed topology in a weak inversion mode (sub threshold MOS operation) for wireless sensor networks and numerous other wireless applications that require very low power consumption.

6.3 Publications Originating from This Thesis

This thesis has been contributed to the following publications.

1. "A very low voltage, 1Ghz CMOS Low-Noise Amplifiers", World scientific and engineering academy and society (WSEAS2005), accepted for Journal publication, November 2005
2. "A 0.85V CMOS Low-Noise-Amplifier Design for 5GHz RF Applications", Midwest Symposium on Circuit and System (MWCAS2005), accepted for publication, August 2005.
3. "A 0.7V, 1GHz CMOS Low-Noise Amplifiers", World Multiconference on Systemics, Cybernetics and Informatics 2005 (WMSCI 2005), accepted for publication, July, 2005.
4. "A 0.8v, 2.4GHz, 1.2dB Noise Figure CMOS Amplifier for Application in Blue Tooth Systems ", World Multiconference on Systemics, Cybernetics and Informatics 2005 (WMSCI 2005), pp.66-69, July, 2005
5. "A 0.65V, 2.4GHz CMOS Low-Noise Amplifiers Design with Noise Optimization", Canadian Conference on Electrical and Computer Engineering 2005 (CCECE2005), accepted for publication, May, 2005.
6. "Comparison of Different CMOS Low-Noise Amplifier Topologies for Bluetooth Applications ", Wireless and Microwave Technology Conference 2005 (WAMICON2005), pp100-103, April, 2005.

7. "Noise Optimization Techniques For 1V 1GHz CMOS Low-Noise Amplifiers Design", International Journal of Signal Processing 2004 (IJSP2004), pp.232-235, Dec., 2004.

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Appendix A: Integrated Inductor Losses

The monolithic inductor characteristics deviate even further from the simple RF model, and require more elaborate modeling. Two common RLC-II-models are used [30] (Figure A.1), and most of the other RLC models are variants of these two. The narrowband models emulate the behaviour of the inductor within two to three decades of frequency, but usually fail beyond the resonance frequency of the inductors. The wideband model can cover a much wider range, specifically at higher frequencies. Often, several II-sections are cascaded to increase the model's accuracy at higher frequencies.

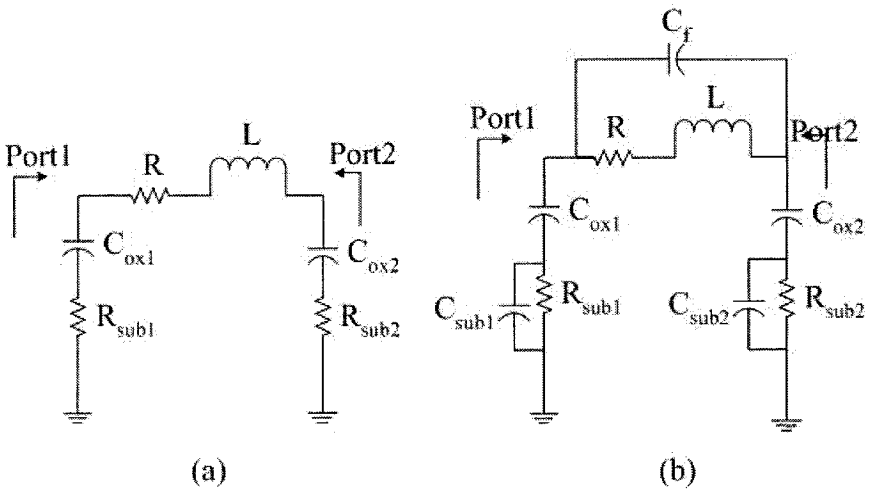

Figure A.1 Inductor two-port II- models.

The most dominant high-frequency losses can be grouped into the following three major categories:

1. Conductor losses:

a. Series ohmic losses due to conductor resistivity.

b. Skin effect.

2. Substrate losses:

a. Electrically (displacement) and magnetically (Eddy) induced substrate currents.

b. Dielectric losses (mostly capacitive).

3. Radiation (air and substrate).

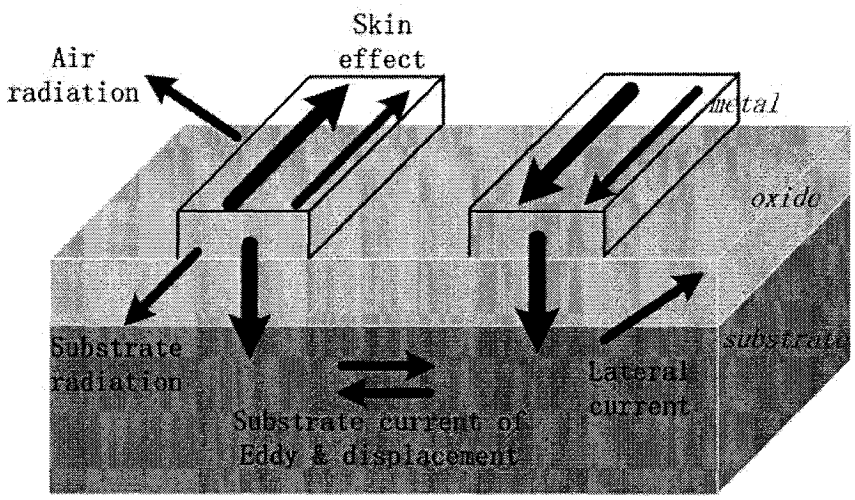

Figure A.2 Losses of Si microstrips at RF.

At low frequency, the ohmic resistances of the conductor are the dominant sources of losses. As such, the shape of the quality factor follows that of an RL section as shown in Figure A.1.b. As the operating frequency increases, the remaining sources of losses result in a decrease in Q, as they provide alternative parasitic components for energy storage besides *L*.

The various loss factors introduced in items 1-3 above are discussed further in the following. [28] [31]

A. Skin Effect

The skin effect arises at high frequency, when the conductor is thicker than the skin effect depth δ, defined as:

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma}} \qquad \text{(A.1)}$$

where μ_0 is the magnetic permeability of the conductor, and σ is the conductivity of the signal-carrying medium. Under these circumstances, only the regions close to the conductor surface carry the RF signal, resulting in an increase in the "*effective impedance*" at high frequency.

B. Bulk Eddy Currents

The rapidly-varying electromagnetic field (EMF) in the conductor results in an induced current in the substrate. This current is larger for substrates with low resistivity. This induction, according to Lenz' law, would have the effect of reducing the effective inductance, which in turn results in a reduction of the quality factor (Equation A.1).

To avoid this problem without using extra processing steps, the resistivity of the substrate can be increased by using a high-resistivity ground plane placed beneath the inductor, as will be explained in the next subsection.

C. Dielectric and Substrate Capacitive and Ohmic Losses

The high resistivity of the oxide dielectric (typical resistivity of SiO_2 is 10^{10} ohm*cm) make its resistance too large to affect the inductor's performance, as it essentially behaves as an open circuit. The remaining effect of the dielectric is mostly capacitive,

where the top plate is the metal conductor and the bottom-plane is the dielectric substrate boundary.

The substrate on the other hand is a source of ohmic losses due to its finite resistivity (typical p-bulk resistivity is 15-20 ohm*cm), and a source of capacitive leakage, where the bottom plate is the conducing ground plane usually residing beneath the die.

The substrate is the most serious source of losses for Si inductors, in particular for CMOS substrates which have fairly low resistivities. Extra processing steps to etch away the dielectric and substrate beneath the inductors would result in a considerable increase in quality factor. A common and more viable approach is to try to terminate the RF electric field, and consequently the resulting magnetic field, through the use of a polysilicon ground plane. This plane should not provide a closed path for the induced Eddy currents, and should therefore be broken.

D. Radiation

Radiation is the transformation of part of the signal power to an electromagnetic wave. The reduction of the power stored in L has the undesirable effect of reducing Q. With the current conductor sizes (a few hundred micrometers of outside length) and frequencies dealt with (few GHz), this is not a serious problem. The effective lengths of the strips are much smaller than the wavelengths of the RF signals considered (at 1GHz, the wavelength is λ=0.3m), and therefore, these strips do not behave as good antennas. This will become a problem as technologies become capable of supporting higher frequencies, specifically with the appearance of mutual radiations between adjacent strips.

Appendix B: Published Articles

A 0.85 V CMOS Low-Noise Amplifier Design for 5GHz RF Applications

M. Zamin Khan
Victhom Human Bionics,
Saint-Augustin-de-Desmaures
Quebec G3A 2J9
Canada
zamin.khan@victhom.com

Yanjie Wang
Dept. of ECE
Concordia University
Montreal, QC H3G 1M8
Canada
yanjie@ece.concordia.ca

R. Raut
Dept. of ECE
Concordia University
Montreal, QC H3G 1M8
Canada
rabinr@ece.concordia.ca

***Abstract*-A 0.85 V, 5 GHz low noise amplifier (LNA) has been designed, laid out and simulated using Spectre simulator in a standard TSMC 0.18um CMOS technology. The proposed cascode LNA achieves a gain of 20 dB, a noise figure of 1.6 dB, power dissipation of 3 mW from a 0.85 V power supply.**

I. INTRODUCTION

The growing number of users and demand for high speed wireless communications made the designers to work towards higher frequency bands. Wireless local area network (WLAN) operating in 5 GHz frequency band is expected to be a widely used system for the multimedia wireless applications. In general, wireless communication receivers demand low power consumption for portability and long battery life, while at the same time requires low noise figure, optimum gain, and high linearity. Several LNAs work at 5GHz have been reported [1]-[5] but little research has been done for decreasing the power consumption. Lowering the supply voltage (V_{DD}) is one of the most effective ways to decrease the power consumption. The bottleneck for the low voltage design is the limitation of threshold voltages as it is not anticipated to decrease much below what is available today [6].

The design of LNA is full of trade-offs between optimum gain, lowest noise figure, high linearity and low power consumption. Casecode topology is one of the most popular topologies used for CMOS LNA design, which provides high gain and low noise figure at the desired frequency. In this paper, we present the bulk bias technique to reduce threshold voltage so as to lower down voltage supply to 0.85V and ultimately decrease the power consumption. The consideration for noise optimization and input matching of LNAs illustrated in Section II. Design approach for o.85v LNA is illustrated in section III. Spectre simulation results and comparison with other reported LNAs are presented in section IV. Section V concludes the paper.

II. NOISE FIGURE AND INPUT MATCHING

A. Noise Figure

An LNA determines the performance of the communication systems. Noise figure represents how much the given system degrades the signal-to-noise ratio, which is defined as:

$$NF = 10\log\frac{TotalOutputNoisePower}{OutputNoisePowerBySourceImpedance} \quad (1)$$

CMOS LNA design provides high level of integration at low cost but it is a big challenge to achieve low noise performance because of the noisy nature of MOS device. The dominant noise source in MOS devices is channel noise:[7]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \quad (2)$$

Where g_{do} is the zero-bias drain conductance of the device. γ is a bias dependent factor which, for long channel device satisfies $\frac{2}{3} \le \gamma \le 1$,but for short channel devices can be as large as two or three, depending on bias condition. Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying with noise generator, which results in:

$$\overline{v_{rg}^2} = 4kT\delta r_g \Delta f \quad (3)$$

where δ is the coefficient of gate noise, normally equal to 4/3 for long channel devices and r_g is the gate resistance. The gate resistance can be minimized through interdigitation without the need of increased power dissipation, thus it is rendered insignificant [7]. If the sizes of the MOS transistors are carefully chosen, the optimum W_t which is simply a ratio of g_m/C_{gs} can be obtained. Therefore, the minimum noise figure can be achieved according to [8]:

$$F_{min} = 1 + \frac{w}{w_t}\sqrt{\gamma\delta\zeta(1-|c|^2)} \quad (4)$$

If δ were zero, the minimum noise figure would be 0dB.

B. Input Matching

To achieve lower noise and higher gain, the Cascode with the inductor generation topology is employed and shown in Figure 1.

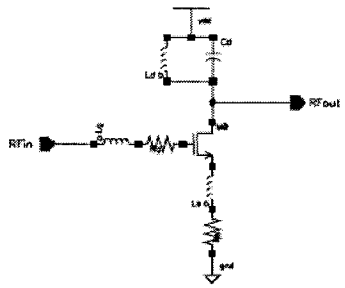

Figure 1. Inductively source degenerated common source amplifier

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Figure1 is:

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{C_{gs} S} + S(L_S + L_g) + R_g \quad (6)$$

where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_0 respectively. L_g and L_s are the gate and source inductors and R_g is the effective gate resistance of M_0 given by $R_g = R_0 / \left(3_n^2 L\right)$ where R_0 is the sheet resistance of the gate polysilicon, W and L are the gate width and length of the transistor M_0 respectively and n is the number of fingers [7].

At the resonant operating frequency(w_0), the input matching area requires that:

$$Z_{in} = R_s = \omega_t L_s \quad (7)$$

The C_{gs} source degeneration inductance L_s is chosen together with W_t to provide the desired input resistance Rs (50ohm), the real term can be made equal to 50 ohm without the existence of a real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met.

III. DESIGN APPROACH

A popular configuration for LNA design is cascode topology with inductive source degeneration to achieve good input matching without adding thermal noise introduced by real resistor as shown in Figure 2. But it has problem working for low voltage supply applications because the power supply must satisfy the following requirement

$$V_{DD} + |V_{SS}| \geq 2V_{thn} \quad (8)$$

where V_{DD} and V_{SS} are the positive and negative power suppl respectively and V_{thn} is the threshold voltages of the each of the NMOS transistor. A solution to the threshold voltage problem comes from the well-know relationship as given

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|}\right) \quad (9)$$

where V_{th0} is the value of V_{th} with $V_{BS} = 0$, γ is the bulk threshold parameter and ϕ is the strong inversion surface potential of

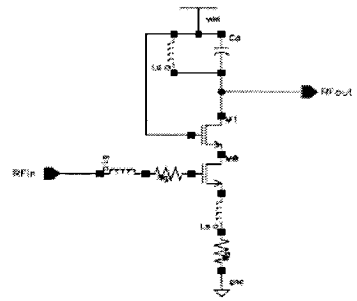

Figure 2. Cascode topology

the NMOS. By applying a voltage on V_{BS}, we can control the threshold voltage V_{th} and thus the polarization of the transistor. Once the threshold is reduced, the value of Vgs for the same current is less. In this LNA design ,the V_{th} decreased from 0.5 V to less than 0.4 V when 0.5V supplied to bulk and the value of current through bulk is 40 uA although this current is undesirable.The bulk current remains below 40 uA for bulk-source voltages as high as 0.5 V.

The simplified schematic of proposed cascode LNA is shown in Figure 3, The first stage is a cascode amplifier formed of M_1

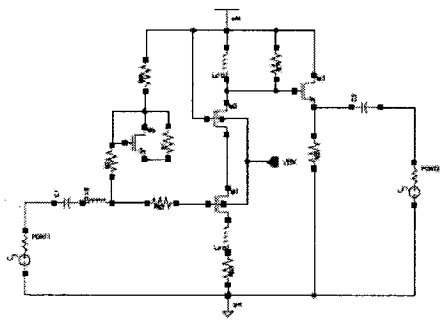

Figure 3. Simplified schematic of proposed cascode topology

and M_2. L_s and L_g are for input matching. M_3 is configured as the buffer stage for LNA output matching. output stage. common-gate device. M_b sets the dc bias for M_0. C_1 is used as a DC blocking capacitor. In our case, it is designed to be 10 pF. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip.

IV. LAYOUT ISSUES AND SIMULATION RESULTS

A. Layout Issues

The integrated inductor exhibits the capacitive and resistive parasitics. For simulation purpose a simplified model as shown in Figure 4 was used: R is total parasitic series resistance, R_s is parasitic resistance to substrate, C is the total parasitic capaci-

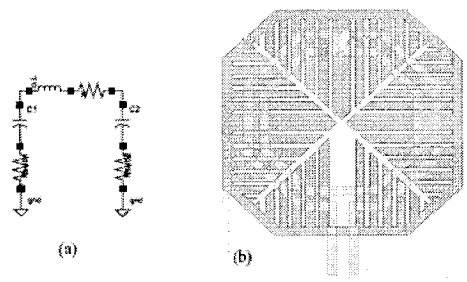

Figure 4. Inductor model: (a) simplified model (b) hollow patterned ground-shield inductor.

tance to substrate and L is the inductance. Their values are given by ASITIC calculation tool provided by UC. Berkeley.

A 0.18um TSMC analog/RF CMOS process was used for implementation of the design. A deep N-well process, depicted in Figure 5, is employed to provide separate substrate connec-

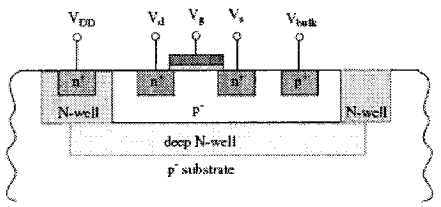

Figure 5. A cross section of a deep N-well

tions and offering increased isolation from substrate noise for NMOS transistors. In addition, the bulk voltage can be forward-baised to reduce the threshold voltage of the NMOS transistors.

Several layout issues have been taken care of. First, grounded-shield planed is laid under the inductor to minimize the magnetic coupling to the substrate. Second, hollow inductor is used to reduce parasitic capacitance and resistance. Third, grounded guard rings with substrate connections surround each capacitor, transistor and three inductors. Moreover, each transistor has an extra N-well guard ring with V_{DD} connection surrounding the grounded guard ring. Forth, a quiet N-well under the input and output signal pads were placed to isolate the RF signals from the substrate.

B. Simulation Results

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process with analog/RF MOSFET model BSIM3. The input and output matching are optimized and power supply of 0.85V is fed to the cascode LNA. Figure 6 depicts a power gain of 20dB at 5GHz for cascode LNA. The noise figure of the cascode LNA as shown in Figure 7.

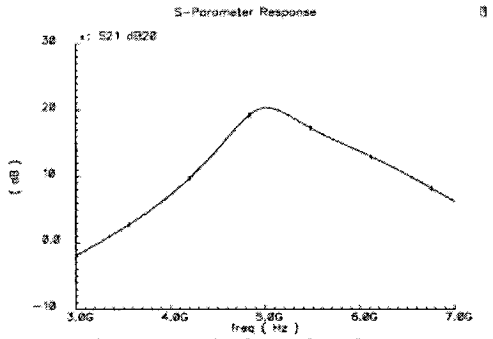

Figure 6. Power gain of proposed cascode LNAs

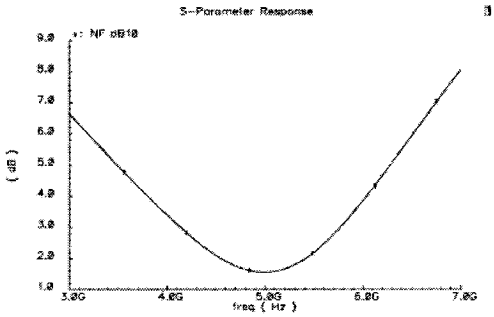

Figure 7. Noise figure of proposed cascode LNAs

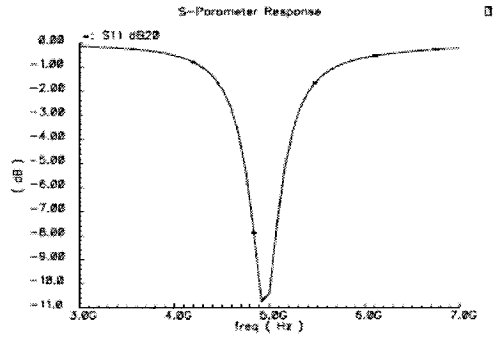

Figure 8. S_{11} of proposed cascode LNAs

The input and output reflections (S_{11}, S_{22}) are illustrated in Figure 8 and Figure 9 respectively. The S_{22} shows a good output match with the output buffer for LNA which achieves below -20dB. A two-tone signal of 5GHz with 20KHz difference has been applied to the LNA input port. The IIP3 simulation result of the LNA is shown in Figure 10. The input-referred third-order intercept points (IIP3) is -26dBm.

The layout of the LNA is shown in Figure 11. The chip area is 1mm x 1mm. This work is placed alongside with other recent

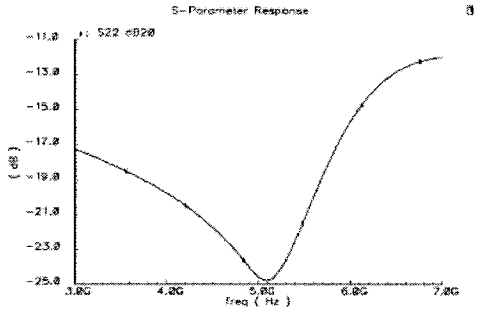

Figure 9. S_{22} of proposed cascode LNAs

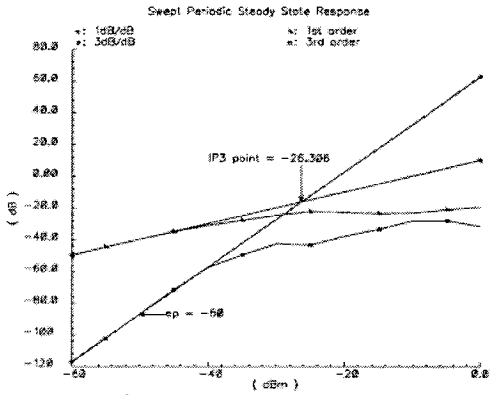

Figure 10. IIp3 of proposed cascode LNAs

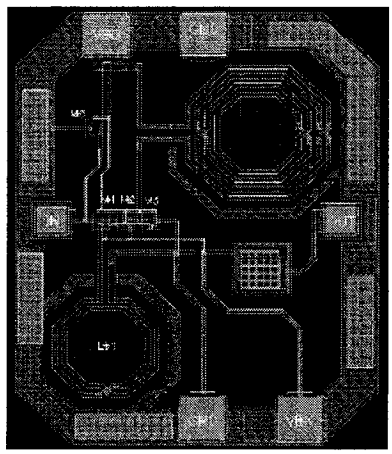

Figure 11. Layout of the proposed LNA

reported 5GHz LNA in Table I. It shows that the proposed LNA achieves the lowest voltage supply and power consumption.

TABLE I
Comparison of Various Recent Reported LNAs

Reference	[1]	[2]	[3]	[4]	[5]	Cascode LNA
Tech(um)	0.35	0.25	0.18	0.18	0.18	0.18
Freq.(GHz)	5.2	5.2	5.2	5.2	5.8	5
NF(dB)	2.45	2.1	2.0	1.4	2.5	1.6
S_{21}(dB)	19.3	17	15.5	16.6	13	20
S_{11}(dB)	N/A	-10	-11	-13	-5.3	-11
S_{22}(dB)	N/A	N/A	-10	N/A	-10.3	-25
IIP_3(dBm)	N/A	N/A	-4.3	0.6	N/A	-26
Supply(V)	3.3	N/A	1.8	1.8	1	0.85
Power(mw)	26	N/A	10.4	16.2	22	3

V. CONCLUSIONS

In this paper, a CMOS low noise amplifier using cascode configurations is proposed. Spectre simulation using 0.18μm CMOS technology shows a low noise figure of 1.6 dB, high power gain (S_{21}) of 20 dB and low power consumption of 3 mW from 0.85 V power supply.

VI. ACKNOWLEGEMENT

The authors greatfully acknowledge the support of Victhom Human Bionics. The research was also supported by a grant awarded to Dr. R. Raut by the Natural Science and Research Council (NSERC) of Canada.

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A Very Low Voltage Design for Different CMOS Low-Noise Amplifier Topologies at 5GHz

M Zamin Khan and Yanjie Wang
Department of Electrical and Computer Engineering
Concordia University
Montreal, QC H3G 1M8
Canada
mz_khan@ece.concordia.ca

R. Raut
Department of Electrical and Computer Engineering
Concordia University
Montreal QC H3G 1M8
Canada
rabinr@ece.concordia.ca

***Abstract*-A very low-voltage design for two different low noise amplifier (LNA) topologies at 5 GHz has been designed, laid out and simulated using Spectre simulator in a standard TSMC 0.18um CMOS technology. The proposed LNA topology achieves better performance than conventional cascode topology and are confirmed by simulation results. The LNA provides a high gain of 20 dB, a noise figure of 1.4 dB, power dissipation of 1.9 mW from a 0.65 V power supply. To the best of author's knowledge this is the lowest voltage supply CMOS LNA design reported to date.**

I. INTRODUCTION

Wireless communication is developing rapidly into one of the most important factors for the next-generation in information technology. Demanding for low power, small size and low cost, CMOS radio frequency integrated circuits (RFICs) design becomes main stream in modern portable wireless communications. Commonly a low noise amplifier (LNA) is a key component in RF front-end receiver which poses a challenge in terms of meeting high gain, low noise figure, good linearity and low power consumption requirement. Several LNAs work at 5GHz have been reported [1]-[5] but little research has been done for low voltage application. Decreasing the supply voltage is one of the efficient way to cut power dissipation. The voltage of the dry cell is 0.9 V and a single solar cell is about 0.5 V. The design of LNA capable of working within such ultra low voltage (0.9V ~ 0.5V) would be very attractive for portable wireless market.

While the continued scaling of silicon technology goes a long way towards reducing the size and power dissipation of the components, achieving the required very low power dissipation level requires innovations from the system architecture down to the circuit level. As such, this paper introduces a very low voltage LNA design using cascode topology and the proposed topology for the operation at 5GHz. The low voltage design for cascode and proposed LNAs is analyzed in Section II. Layout issues are discussed in Section III. Spectre simulation results and a comparison with other reported LNAs are presented in Section IV.

II. LOW VOLTAGE LNA TOPOLOGY

the most widely used topology for LNA design is cascode topology, which requires a high supply voltage (>1 V), since it employs two transistors stacked between the supply rails. With the ultra low voltage supply (0.9 V ~0.5 V), the number of suitable LNA topologies is very limited.

A. Threshold Voltage Control

The bottle-neck for the low voltage design is the limitation of threshold voltages because it is not anticipated to decrease much below what is available today [6]. A solution to the threshold voltage problem comes from the well-know relationship as given

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}\right) \quad (1)$$

where V_{th0} is the value of V_{th} with $V_{BS} = 0$, γ is the bulk threshold parameter and ϕ is the strong inversion surface potential of the MOSFET. For n-channel transistor, by biasing bulk-source voltage $V_{BS} > 0$ V, the threshold voltage can be decreased. To reduce the threshold voltage as much as possible, we want the bulk bias V_{BS} as high as possible. This will however, forward bias the bulk-source diode or the base-emitter diode of the associated parasitic bipolar transistor (BJT) as shown in Figure 1 , thereby turning on this BJT and an undesired bulk current increases significantly. Thus, to keep the bulk current low, the parasitic BJT should be off i.e., bulk-source voltage should be smaller than 0.7V.

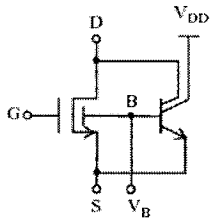

Figure 1. NMOS transistor with parasitic BJT

B. Input Matching

Most RF instruments and coaxial cables have standardized impedances of 50 Ω, thus the input stage of the LNA is required to match to 50 Ω to have no power reflection. Without adding thermal noise introduced by real resistor, the common-source input transistor with inductive source degeneration is often employed and shown in Figure 2. Neglecting the gate drain

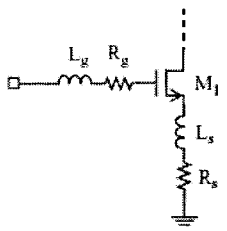

Figure 2. Inductively source degenerated common source input stage

capacitances, the input impedance is:

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{C_{gs} S} + S(L_S + L_g) + R_g \quad (2)$$

where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_1 respectively. L_g and L_s are the gate and source inductors and R_g is the effective gate resistance of M_1 given by $R_g = R_0 / \left(3n^2 L\right)$ where R_0 is the sheet resistance of the gate polysilicon, W and L are the gate width and length of the transistor M_1 respectively and n is the number of fingers [7].

At the resonant operating frequency (w_0), the input matching area requires that:

$$Z_{in} = R_s = \omega_t L_s \quad (3)$$

The C_{gs} source degeneration inductance L_s is chosen together with W_t to provide the desired input resistance Rs (50Ω), the real term can be made equal to 50 Ω without the existence of a real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met.

C. Cascode Topology

The cascode topology with inductive source degeneration is a popular configuration for LNA design, but it has problem working for very low voltage supply applications because the power supply must satisfy the following requirement

$$V_{DD} + |V_{SS}| \geq 2V_{thn} \quad (4)$$

where V_{DD} and V_{SS} are the positive and negative power supply, respectively and V_{thn} is the threshold voltages of the each of the NMOS transistor. The simplified low voltage design schematic of cascode topology is shown in Figure 3. The minimum supply voltage can be reached to 0.85 V, but bulk-source voltage

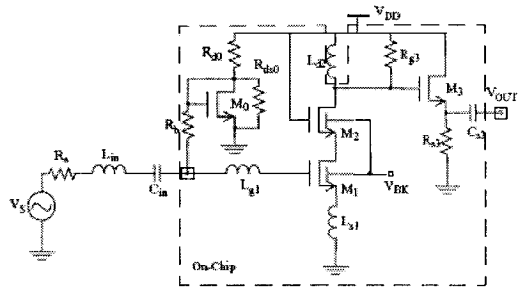

Figure 3. Simplified schematic of cascode topology

must kept smaller than 0.7 V to avoid the undesired bulk current increase significantly.

D. Proposed Common-source Common-gate Topology

To remove the factor of 2 in equation (4), cascode topology is replaced by single transistor configuration. Therefore, two single transistor cascaded stages with inductive source degeneration are designed for the LNA. The simplified schematic of proposed cascaded common-source common-gate topology is shown in Figure 4, which offers a lower power supply than that

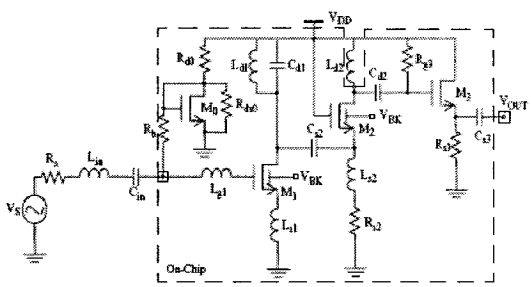

Figure 4. Simplified schematic of proposed common-source common-gate topology

of cascode LNA while the gain can be maintained. In the first stage, the size of common-source transistor M_1, off-chip inductance (L_{in} = 16 nH) and on-chip input gate inductance L_{g1} at the drain are properly chosen to tune the LNA to the desired band and match real part of input impedance to 50Ω source impedance. In addition, L_{s1} at the source is used to achieve optimum input matching and noise figure. The LC tank (L_{d1},C_{d1}) of M_1 is set to achieve a resonance frequency at 5GHz and provide a DC bias current path and a high impedance branch to force the RF signal to flow into the source of the common-gate transistor M_2 through a big DC coupling capacitance (C_{s2} = 5 pF). L_{s2} are connected to the source to improve the noise figure and stability. However, the S_{11} gets worse when L_{s2} increases. This effect limits the amount of inductance (L_{s2} = 2 nH). Source-follower buffer M_3 is employed for measurement purposes to drive an

external 50Ω load. The LNA output matching uses on-chip resistor R_{g3}, R_{s3} and metal-to-metal capacitor C_{s3}. Transistor M_0 with 20KΩ resistor R_b for ac blocking forms the biasing circuitry. A bulk-source voltage V_{BK} is employed to forward-bias the well-source junction of transistors M_1 and M_2. The threshold voltage of the transistors decreased from 0.54V to around 0.4V and the undesired bulk current remains below 100uA for bulk-source voltages as high as 0.65V.

III. LAYOUT ISSUES

The integrated inductor exhibits the capacitive and resistive parasitics. For simulation purpose a simplified model as shown in Figure 5. was used: R is total parasitic series resistance, R_s is

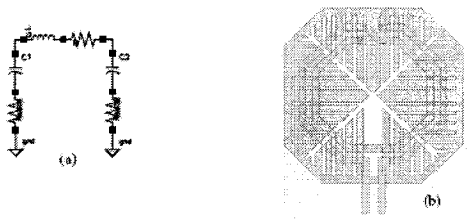

Figure 5. Inductor model: (a) simplified model (b) hollow patterned ground-shield inductor.

parasitic resistance to substrate, C is the total parasitic capacitance to substrate and L is the inductance. Their values are given by ASITIC calculation tool provided by UC. Berkeley.

A 0.18um TSMC analog/RF CMOS process was used for implementation of the design. A deep N-well process, depicted in Figure 6, is employed to provide separate substrate connec-

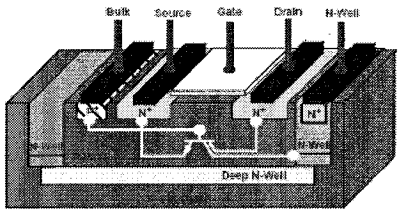

Figure 6. A cross section of a deep N-well

tions and offering increased isolation from substrate noise for NMOS transistors. In addition, the bulk voltage can be forward-biased to reduce the threshold voltage of the NMOS transistors.

Several layout issues have been taken care of. First, grounded-shield planed is laid under the inductor to minimize the magnetic coupling to the substrate. Second, hollow inductor is used to reduce parasitic capacitance and resistance. Third, grounded guard rings with substrate connections surround each capacitor, transistor and three inductors. Moreover, each transistor has an extra Nwell guard ring with V_{DD} connection surrounding the grounded guard ring. Forth, a quiet Nwell under the input and output signal pads were placed to isolate the RF signals from the substrate.

IV. SIMULATION RESULTS

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process with RF MOSFET model BSIM3. For comparison purpose, the transistor sizes are the same for both circuits, input and output matching are optimized and power supply of 0.85V and 0.65V are fed to the cascode and proposed LNAs respectively. Figure 7 depicts a power gain of

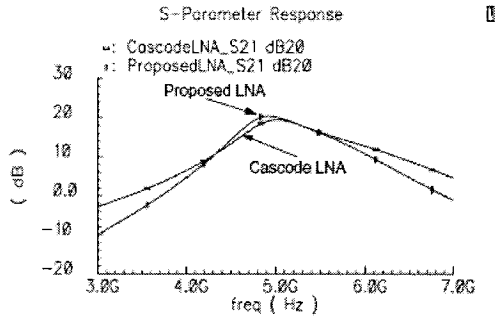

Figure 7. Power gain comparison of cascode and proposed LNAs

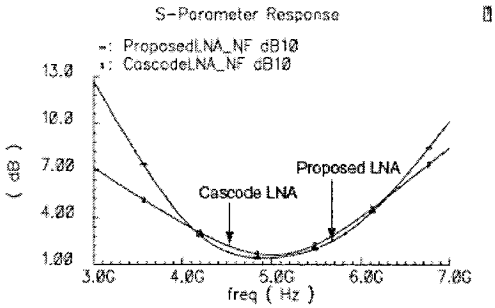

Figure 8. Noise figure comparison of cascode and proposed LNAs

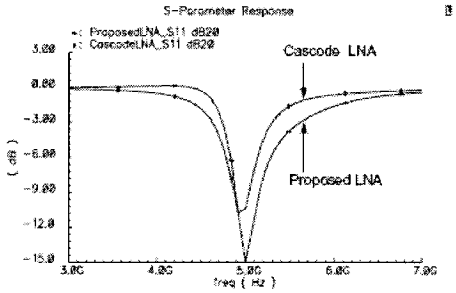

Figure 9. S_{11} comparison of cascode and proposed LNAs

20dB at 5GHz for proposed LNA, which is 2dB higher than the cascode LNA. This should thank to the source degeneration

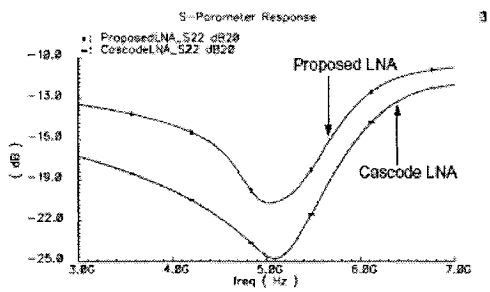

Figure 10. S_{22} comparison of cascode and proposed LNAs

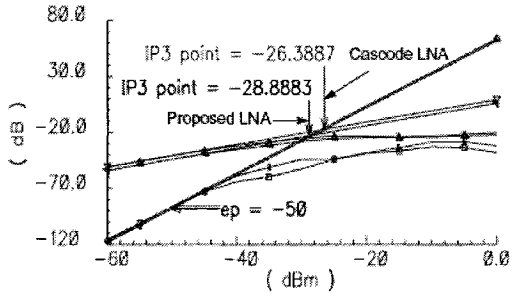

Figure 11. IIp3 comparison of cascode and proposed LNAs

inductance L_{s2}, which also offers a 0.2dB less noise figure than the cascode LNA as shown in Figure 8.

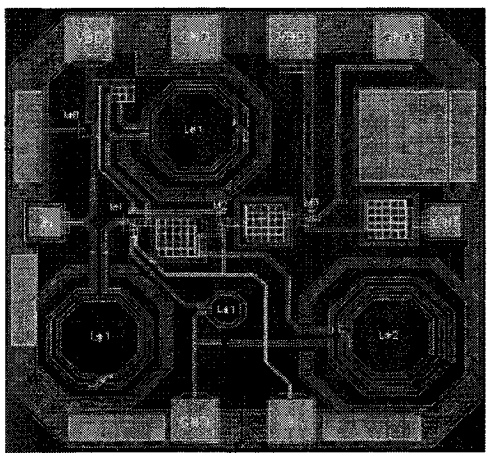

Figure 12. Layout of the proposed LNA

The input and output reflections (S_{11}, S_{22}) are illustrated in Figure 9 and Figure 10 respectively. The S_{22} shows a good output match with the output buffer for both LNAs which achieves below -20dB. With the same input stage configuration for both circuits, the S_{11} are similar and less than -10dB. A two-tone signal of 5GHz with 20KHz difference has been applied to the LNA input port. The IIP3 simulation result of the LNA is shown in Figure 11. A two-tone signal which are chosen close to each other has been applied to the input port. The input-referred third-order intercept points (IIP3) is -29dBm.

The layout of the LNA is shown in Figure 12. The chip area is 1mm x 1mm. This work is placed alongside with other recent reported 5GHz LNA in Table I. It shows that the proposed LNA achieves the lowest voltage supply and power consumption.

TABLE I
COMPARISONS OF RECENT REPORTED LNAs

Reference	[1]	[2]	[3]	[4]	[5]	Cascode	Proposed
Tech(um)	0.35	0.25	0.18	0.18	0.18	0.18	0.18
Freq.(GHz)	5.2	5.2	5.2	5.2	5.8	5	5
NF(dB)	2.45	2.1	2.0	1.4	2.5	1.6	1.4
S_{21}(dB)	19.3	17	15.5	16.6	13	18	20
S_{11}(dB)	N/A	-10	-11	-13	-5.3	-11	-15
S_{22}(dB)	N/A	N/A	-10	N/A	-10.3	-25	-21
IIP_3(dBm)	N/A	N/A	-4.3	0.6	N/A	-26	-29
Supply(V)	3.3	N/A	1.8	1.8	1	0.85	0.65
Power(mw)	26	N/A	10.4	16.2	22	3.2	1.9

V. CONCLUSIONS

In this paper, Two different CMOS LNA designs for low voltage supply operating at 5GHz is presented. A LNA using common-source common-gate topology working with 0.65 V supply is proposed. Spectre simulation using 0.18μm CMOS technology shows a low noise figure of 1.4 dB, high power gain (S_{21}) of 20 dB and low power consumption of 1.9 mW from 0.65 V power supply.

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A 0.8V, 2.4GHz, 1.2 dB Noise Figure CMOS Amplifier for Appliation in Blue Tooth Systems

M. Zamin Khan and Yanjie Wang
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: mz_khan@ece.concordia.ca
w_yanjie@ece.concordia.ca

R. Raut
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: rabinr@ece.concordia.ca

Abstract-**A 0.8 V, 2.4 GHz low noise amplifier (LNA) has been designed and simulated using Spectre simulator in a standard TSMC 0.18um CMOS technology. With low power and noise optimization techniques, the amplifier provides a gain of 19.5 dB, a noise figure of only 1.2 dB, power dissipation of 5.6 mW from a 0.8 V power supply.**

I. INTRODUCTION

Wireless communications receivers demand low power consumption for portability and long battery life, while at the same time requires low noise figure, optimum gain, and high linearity. one very important area in this context is personal wireless communication devices. Bluetooth is one of technology to require such condition, short range, 2.4GHz wireless standard for connecting various communications devices such as mobile phone wireless headsets, and desktop and note book computer. The primary constraint on bluetooth application is power consumption, decreasing power consumption of RFIC circuit is one of the key design issues. Lowering the supply voltage (V_{DD}) is the most effective way to decrease the power consumption. The primary role of the LNA is to lower the overall noise figure of the entire RF front-end, noise optimization is considered as one of the most critical steps in the LNA design procedure. The LNA determines the overall system's noise performance because it is the first block after the antenna[1].

Casecode topology is one of the most popular topologies used for CMOS LNA design, which provides high gain and low noise figure at the desired frequency. In this paper, we present the bulk bias technique to reduce threshold voltage so as to lower down voltage supply to 0.8V and ultimately decrease the power consumption.The consideration for noise optimization, design approach and the proposed LNA is suitable for o.8v are illustrated in section II. Spectre simulation results and comparison with other reported LNAs are presented in section III. Section IV concludes the paper.

II. DESIGN APPROACH FOR LNA

To achieve lower noise and higher gain, the casecode with the inductor degeneration topology is employed and shown in Figure 1.

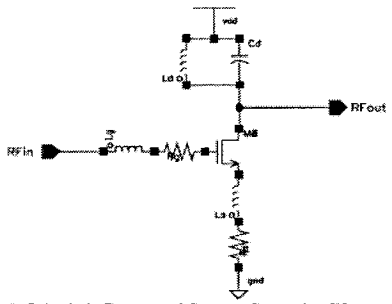

Figure 1. Inductively Degenerated Common Source Amplifier

II A: Input Matching

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Figure1 is:

$$Z_{in} = \frac{g_{mL_s}}{C_{gs}} + \frac{1}{C_{gs}S} + S(L_S + L_g) + R_g \qquad (1)$$

where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_0 respectively. L_g and L_s are the gate and source inductors and R_g is the effective gate resistance of M_0 given by $R_g = R_0/\left(3n^2L\right)$ where R_0 is the sheet resistance of the gate polysilicon,W and L are the gate width and length of the transistor M_0 respectively and n is the number of fingers [2].

At the resonant operating frequency(w_0), the input matching requires that:

$$Z_{in} = \frac{g_m}{C_{gs}} = \omega_t L_s \qquad (2)$$

The C_{gs} source degeneration inductance L_s is chosen together with ω_t to provide the desired input resistance Rs, the real term can be made equal to 50 ohm without the existence of a

real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met. As technology improves, ω_t increases this leads to a reduction in inductor L_s size , making the system more suitable for on-chip integration. The value of L_s is about 1nH and it is implemented on chip.

II B: Minimum Noise Figure Design

An LNA determines the performance of the communication systems. It needs higher linearity and sufficient gain to overcome the next stage noise but not to overload. A system noise factor is defined as:

$$F_{total} = F_1 + \frac{F_1 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \ldots \quad (3)$$

where F_n (n=1,2,3,....) is the noise factor of each stage, G_n(n=1,2,3,...)is the gain of each stage. In our circumstances, F_1 is the noise factor of the LNA and G_1 is the gain of the LNA which implies that higher gain and lower noise of LNA will lower the total noise of the system. Noise figure represents how much the given system degrades the signal-to-noise ratio, which is defined as:

$$NF = 10\log \frac{TotalOutputNoisePower}{OutputNoisePowerSourduetoImpedance} \quad (4)$$

Therefore, the minimum noise figure can be achieved according to [3]:

$$F_{min} = 1 + \frac{w}{w_t}\sqrt{\gamma\delta\zeta(1-|c|^2)} \quad (5)$$

If δ were zero, the minimum noise figure would be 0dB.

C Bulk Source Biasing

To make the Cascode LNA works at 0.8V, the well-source junction of the NMOS transistors are forward biased as shown in Fig. 2 which causing the threshold voltage to decrease. The threshold voltage with body effect is based on the following expression.

$$V_T = V_{TO} + \gamma[\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}] \quad (6)$$

which,V_{TO} is the intrinsic threshold voltage, γ is the body effect coefficient,ϕ_f the surface inversion potential of silicon and V_{BS} is the bulk-source voltage. By applying a voltage on V_{BS}, we can control the threshold voltage V_T and thus the polarization of the transistor. Once the threshold is reduced, the value of Vgs for the same current is less. In this LNA design ,The V_T decreased from 0.5 V to less than 0.4 V when 0.5V supplied to bulk and the value of current through bulk is 40 uA although this current is undesirable.The bulk current remains below 40 uA for bulk-source voltages as high as 0.5 V.

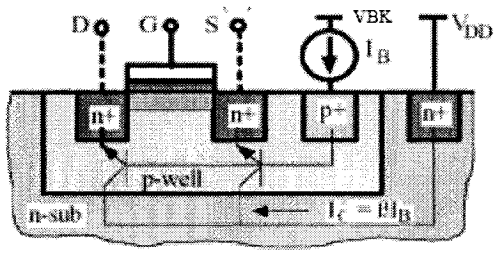

Figure 2. Cross-Section of a forward-biased NMOS transistor

III. Simulation Results

The complete schematic circuit is shown in Figure 3. The first

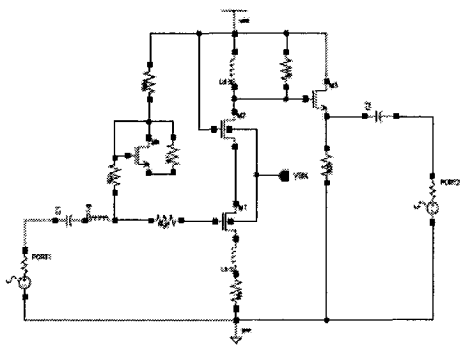

Figure 3. Complete shcematic of proposed common-scure, common-gate LNA

stage is a cascode amplifier formed of M_1 and M_2. L_s and L_g are for input matching. M_3 is configured as the buffer stage for LNA output matching. output stage. common-gate device. M_b sets the dc bias for M_0. C_1 is used as a DC blocking capacitor. In our case, it is designed to be 10 pF. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip.

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process. After noise optimization a low noise figure of 1.2 dB at 2.4 GHz is achieved and shown in Figure 6.

The S-parameters of the LNA illustrated in Figures 4,5,7,8 show a forward power gain (S21) of 19.5 dB at 2.4 GHz. A good input match of -16.8dB in Figure 7. A good output match with the output buffer which achieves -15dB in Figure 4. The S12 shows a low reverse transmission -59dB as shown in Figure 8. The IIP3 simulation result of the LNA is shown in Figure 9 A two-tone signal which are chosen close to each other has been applied to the input port. The input-referred third order inter-

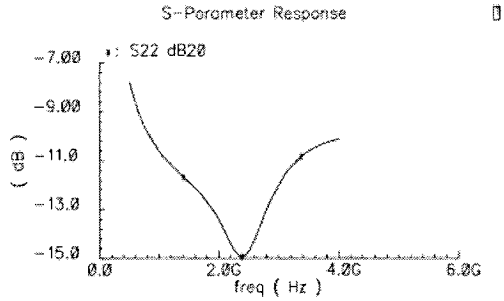

Figure 4. S22 of proposed LNA

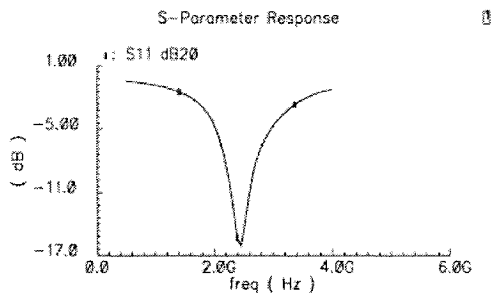

Figure 7. S11 of proposed LNA

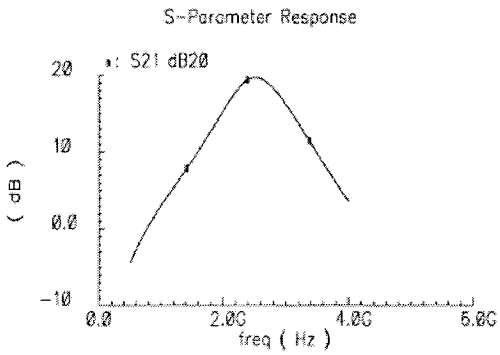

Figure 5. Power gain of proposed LNA

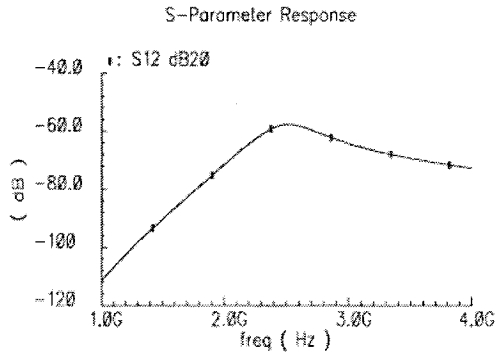

Figure 8. S12 of proposed LNA

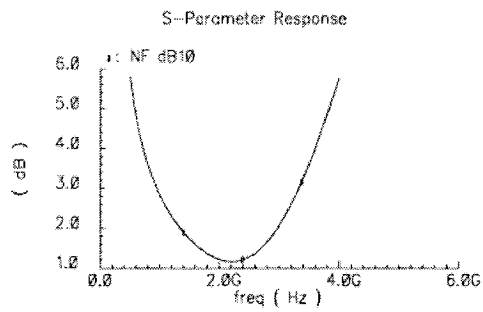

Figure 6. Noise figure of proposed LNA

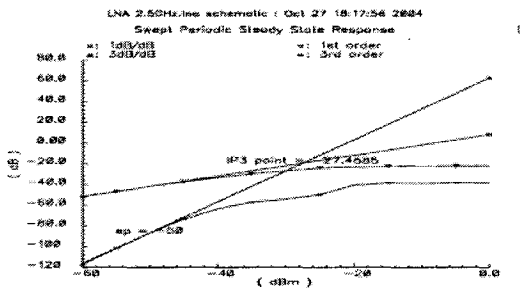

Figure 9. IIp3 simulation of the proposed LNA

cept points (IIP3) is -27.4dBm. The layout of the LNA is shown in Figure 10 , The chip area is 0.74mm x 0.94mm.

Table 1: Comparison of Various Recent Reported LNAs

Reference	[7]	[6]	[5]	[4]	[3]	This Work
Freq.(GHz)	2.4	2.4	2.4	2.4	2.4	2.4
NF(dB)	1.8	2.4	1.6	4.0	2	1.2
S_{21}(dB)	15	19	25	12	19	19.5
$IIP_{3(dBm}$	-	-	-8	-2	-	-27.4
Supply (v)	5	3	1.5	1.8	-	0.8
Power(mw)	-	9	16	14.3	40.8	5.6
Tech(um)	-	0.5	0.18	0.18	0.3	0.18

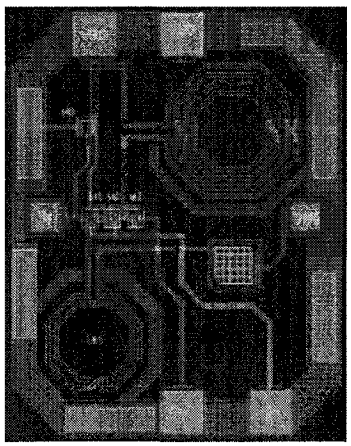

Figure 10. Layout of the proposed LNA

optimization techniques the proposed LNA achieves a much lower noise figure than other LNAs.

IV. CONCLUSIONS

In this paper, a new CMOS low noise amplifier using cascode topology with bulk biasing. The proposed topology is suitable for low power supply application and works well at 0.8 V voltage supply. Spectre simulation using TSMC 0.18µm CMOS technology shows a low noise figure of 1.2 dB, high power gain (S21) of 19.5 dB and low power consumption of 5.6 mW from 0.8 V power supply.Table 1. shows a comparison of the present work with similar work reported in the literature.The present work clearly exceeds the other work in terms of low voltage, low power, and low noise figure operation.

ACKNOWLEDGEMENT

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A 0.65V, 2.4GHZ CMOS LOW-NOISE AMPLIFIERS DESIGN WITH NOISE OPTIMIZATION

M. Zamin Khan, Yanjie Wang
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: mz_khan@ece.concordia.ca

R. Raut
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: rabinr@ece.concordia.ca

Abstract-**A 0.65 V, 2.4 GHz low noise amplifier (LNA) has been designed and simulated using Spectre simulator in a standard TSMC 0.18um CMOS technology. With low power and noise optimization techniques, the amplifier provides a gain of 27 dB, a noise figure of only 1.1 dB, power dissipation of 4.6 mW from a 0.65 V power supply.**

I. INTRODUCTION

The tremendous growth in the portable wireless application is pushing for cost-effective and low-power solutions. Among this bigger and bigger market, one of the most attracting fields lies in personal wireless communication development. Bluetooth is one of technology to meet such condition, short range, 2.4GHz wireless standard for connecting various communications devices such as mobile phone wireless headsets, desktop and note book computer. The primary constraint on bluetooth application is power consumption, decreasing power consumption of RFIC circuit is one of the key design issues. Lowering the supply voltage (V_{DD}) is the most effective way to decrease the power consumption. CMOS radio frequency integrated circuits (RFICs) design becomes main stream in modern portable wireless communications. Commonly a low noise amplifier (LNA) is a key component in RF front-end receiver which poses a challenge in terms of meeting high gain, low noise figure and linearity requirement at sub 1 volt power supply (such as 0.65 V). The primary role of the LNA is to lower the overall noise figure of the entire RF front-end, noise optimization is considered as one of the most critical steps in the LNA design procedure.

The design of LNA is full of trade-offs between optimum gain, lowest noise figure, high linearity and low power consumption. Casecode topology is one of the most popular topology used for CMOS LNA design, which provides high gain, low noise, but it is not suitable for low power supply. As such, this paper discusses the design implementation for a low voltage supply (0.65V). The consideration for noise optimization of LNA is illustrated in Section II. The design approach of proposed LNA is presented in Section III. Spectre simulation results and a comparison with other reported LNAs are shown in Section IV. Section V concludes the paper.

II. NOISE FIGURE AND OPTIMIZATION

CMOS LNA design provides high level of integration at low cost but it is a big challenge to achieve low noise performance because of the noisy nature of MOS device. The dominant noise source in MOS devices is channel noise:[2]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \tag{1}$$

Where g_{do} is the zero-bias drain conductance of the device. γ is a bias dependent factor which, for long channel device satisfies $\frac{2}{3} \le \gamma \le 1$,but for short channel devices can be as large as two or three, depending on bias condition. Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying with noise generator, which results in:

$$\overline{v_{rg}^2} = 4kT\delta r_g \Delta f \tag{2}$$

where δ is the coefficient of gate noise, normally equal to 4/3 for long channel devices and r_g is the gate resistance. The gate resistance can be minimized through interdigitation without the need of increased power dissipation, thus it is rendered insignificant [1]. If the sizes of the MOS transistors are carefully choose, the optimum W_t which is simply a ratio of g_m/C_{gs} can be obtained. Therefore, the minimum noise figure can be achieved according to [2]:

$$F_{min} = 1 + \frac{w}{w_t}\sqrt{\gamma\delta\zeta(1-|c|^2)} \tag{3}$$

If δ were zero, the minimum noise figure would be 0dB[3]

To achieve lower noise and higher gain, the common source with the inductor degeneration topology is employed and shown in Figure 1.

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Figure1 is:

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{C_{gs}S} + S(L_S + L_g) + R_g \tag{4}$$

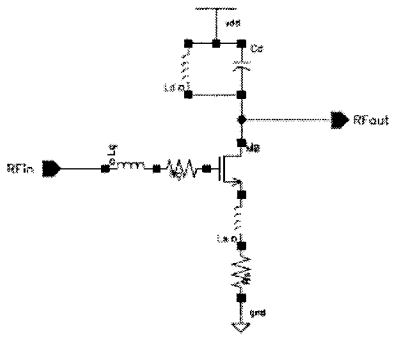

Figure 1. Inductively degenerated common Source Amplifier

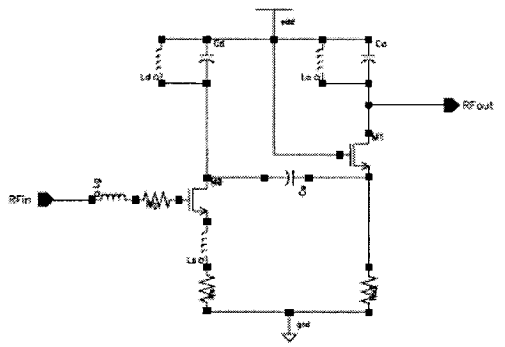

Figure 2. Common source common gate topology

where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_0 respectively. L_g and L_s are the gate and source inductors and R_g is the effective gate resistance of M_0 given by $R_g = R_0/(3n^2L)$ where R_0 is the sheet resistance of the gate polysilicon,W and L are the gate width and length of the transistor M_0 respectively and n is the number of fingers [1].

At the resonant operating frequency(w_0), the input matching area requires that:

$$Z_{in} = R_s = \omega_t L_s \tag{5}$$

The C_{gs} source degeneration inductance L_s is chosen together with W_t to provide the desired input resistance Rs, the real term can be made equal to 50 ohm without the existence of a real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met.

III. LNA DESIGN APPROACH

For LNA design, inductive source degeneration is used to achieve good input matching without adding thermal noise introduced by real resistor. The cascode topology is a popular configuration for LNA design but it is not suitable for low voltage supply applications.

The proposed topology is shown in Figure 2, which works for sub 1 volt, in our case it is 0.65V. Inductive source degeneration is also used to achieve good input matching and reduce noise figure. The first stage is inductively degenerated common-source amplifier formed by transistor M_0. Followed by a common-gate configurated transistor M_1. The value of LC tank of M_0 is carefully chosen to achieve a resonance frequency of 1GHz and is required to have a much higher impedance than that of the input impedance looked at the source of M_1. It provides a DC bias current path and a high impedance branch to force the RF signal to flow into the source of M_1 through a big DC coupling capacitance C_s.

The input impedance of the LC tank (L_d,C_d) is

$$Z_d = R_d + \frac{\omega^2 L_d^2}{R_d} \approx \frac{\omega^2 L_d^2}{R_d} = R_d Q_d^2 \tag{6}$$

Then,

$$g_{m1} \approx \frac{1}{R_d Q^2 d} \tag{7}$$

where R_d and Q_d are the resistance and the quality factor associated with the inductor L_d.

The input impedance at the source of the common gate transistor M_1 is:

$$R_i = \frac{1}{g_{m1} + g_{mb1}} \approx \frac{1}{g_{m2}} \tag{8}$$

where g_{mb} is the bulk transconductance.

A forward bias on this junction will cause the threshold voltage to decrease.The body effect feedback is based on the following expression.

$$V_T = V_{TO} + \gamma[\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}] \tag{9}$$

with,V_{TO} the intrinsic threshold voltage, γ the body effect coefficient, ϕ_f the surface inversion potential of silicon and V_{BS} the bulk-source voltage.In order to design LNA works at 0.65V By applying a voltage on V_{BS} we can control the threshold voltage V_T and thus the polarization of the transistor.

IV. Simulation Results

The complete circuit is shown in Figure 3. The LNA first stage M_0 is inductively degenerated representing the common-source amplifier followed by M_1 configured as common-gate device. M_b sets the dc bias for M_0. M_2 is configured as the buffer stage for LNA output matching. C_1 between M_0 and M_1

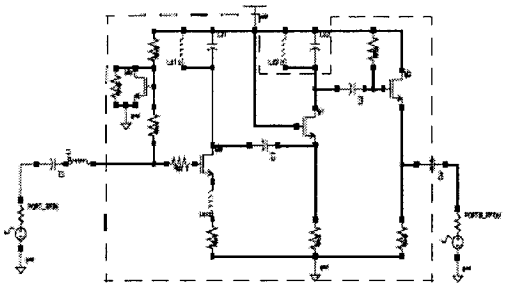

Figure 3. Complete shcematic of proposed common-soure, common-gate LNA

is acting as a DC coupling capacitance to block DC and provides ac path to let RF signal flow into the source of common-gate transistor M_1. In our case, it is designed to be 10 pF. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip. As shown in Figure 3 only the framed components are on-chip.

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process . After noise optimization a low noise

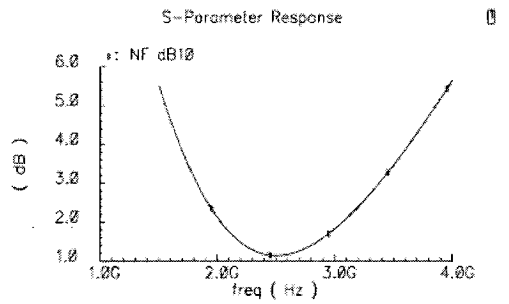

Figure 4. Noise figure of proposed LNA

figure of 1.1 dB at 2.4 GHz is achieved and shown in figure 4.

The S-parameters of the LNA are illustrated in Figure 5,6, and 7. Figure 6 shows a forward gain (S21) of 27 dB at 2.4GHz. The input matching S11 is -12dB.The S22 shows a good output match with the output buffer which achieves -30.7dB,this maximizes the power transfer from the LNA to the 50 ohms input impedance of the next stage. The IIP3 simulation result of the LNA is shown in Figure 8. A two-tone signal which are chosen close to each other has been applied to the input port. The input-referred third-order intercept points (IIP3) is -30.0dBm.

The layout of the LNA is shown in Figure 8. The chip area is 1mm x 1mm. This work is placed alongside with other recent

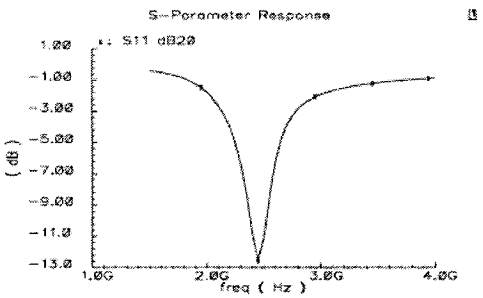

Figure 5. S11 of proposed LNA

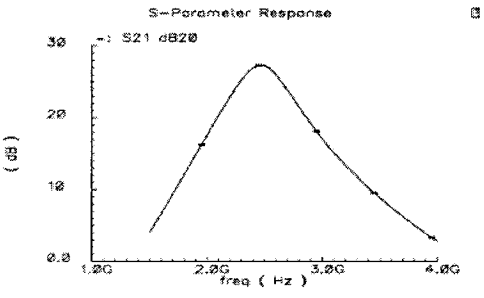

Figure 6. Power gain of proposed LNA

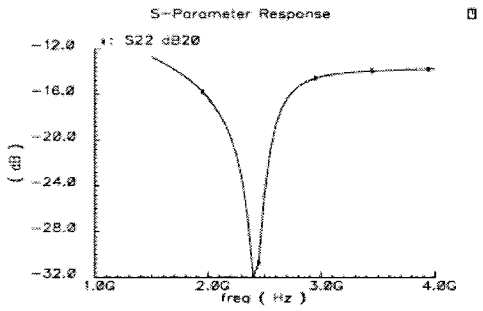

Figure 7. S22 of proposed LNA

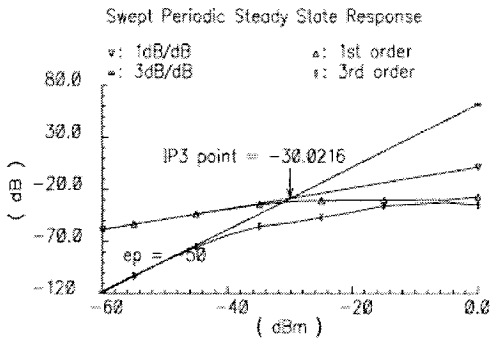

Figure 8. IIp3 simulation of the proposed LNA

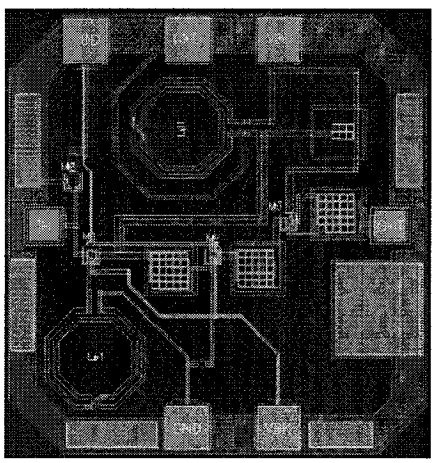

Figure 9. Layout of the proposed LNA

reported LNA in Table 1. It shows that with the noise optimiza-

Table 1: Comparison of Various Recent Reported LNAs

Reference	[8]	[7]	[6]	[5]	[4]	This Work
Freq.(G Hz)	2.4	2.4	2.4	2.4	2.4	2.4
NF(dB)	1.8	2.4	1.6	4.0	2	1.1
S_{21}(dB)	15	19	25	12	19	27
IIP_{3dBm}	-	-	-8	-2	-	-30
Supply Voltage	5	3	1.5	1.8	-	0.65
Power(mw)	-	9	16	14.3	40.8	4.6
Tech(um)	-	0.5	0.18	0.18	0.3	0.18

tion techniques the proposed LNA achieves a much lower noise figure than other LNAs.

V. CONCLUSIONS

In this paper, a new CMOS low noise amplifier using common-source inductive source degeneration followed by common-gate configurations is proposed. The proposed topology is suitable for low power supply application and works good at 0.65 V voltage supply. Spectre simulation using TSMC 0.18μm CMOS technology shows a low noise figure of 1.1 dB, high power gain (S21) of 27 dB and low power consumption of 4.6 mW from 0.65 V power supply.

ACKNOWLEDGEMENT

The research was supported by a grant awarded to Dr. R. Raut by the Natural Science and Research Council (NSERC) of Canada

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COMPARISON OF DIFFERENT CMOS LOW-NOISE AMPLIFIERS TOPOLOGIES FOR BLUETOOTH APPLICATIONS

M. Zamin Khan and Yanjie Wang
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: mz_khan@ece.concordia.ca
w_yanjie@ece.concordia.ca

R. Raut
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: rabinr@ece.concordia.ca

Abstract-**A 0.65 V, 2.4 GHz low noise amplifier (LNA) has been designed and simulated using Spectre simulator in a standard TSMC 0.18nm CMOS technology. With low power and noise optimization techniques, the amplifier provides a gain of 27 dB, a noise figure of only 1.1 dB, power dissipation of 4.6 mW from a 0.65 V power supply. The proposed LNA achieves superior performance over conventional cascode topology and are confirmed by simulation results.**

I. INTRODUCTION

The tremendous growth in the portable wireless application is pushing for cost-effective and low-power solutions. Among this bigger and bigger market, one of the most attracting fields lies in personal wireless communication development. Bluetooth is one of technology to meet such condition, short range, 2.4GHz wireless standard for connecting various communications devices such as mobile phone wireless headsets, and desktop and note book computer. The primary constraint on bluetooth application is power consumption, decreasing power consumption of RFIC circuit is one of the key design issues.Lowering the supply voltage (V_{DD}) is the most effective way to decrease the power consumption.CMOS radio frequency integrated circuits (RFICs) design becomes main stream in modern portable wireless communications. Commonly a low noise amplifier (LNA) is a key component in RF front-end receiver which poses a challenge in terms of meeting high gain, low noise figure and linearity requirement at sub 1 volt power supply (such as 0.65 V). The primary role of the LNA is to lower the overall noise figure of the entire RF front-end, noise optimization is considered as one of the most critical steps in the LNA design procedure.

The LNA determines the overall system's noise performance because it is the first block after the antenna[1]. The design of LNA is full of trade-offs between optimum gain, lowest noise figure, high linearity and low power consumption. Casecode topology is one of the most popular topology used for CMOS LNA design, which provides high gain, low noise, but it is not suitable for low power supply. As such, this paper discusses the design implementation for a low voltage supply (0.65V). This paper presents an LNA structure suitable for ultra low voltage and compared to widely used conventional cascode topology. The consideration for noise optimization of LNA is illustrated in Section II. The design approach of proposed common-source (CS) and common-gate(CG) cascade LNA with bulk-biased technique is presented in Section III. Spectre simulation results and a comparison with cascode and other reported LNAs are shown in Section IV. Section V concludes the paper.

II. NOISE FIGURE AND OPTIMIZATION

CMOS LNA design provides high level of integration at low cost but it is a big challenge to achieve low noise performance because of the noisy nature of MOS device. The dominant noise source in MOS devices is channel noise:[2]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \tag{1}$$

Where g_{do} is the zero-bias drain conductance of the device. γ is a bias dependent factor which, for long channel device satisfies $\frac{2}{3} \le \gamma \le 1$, but for short channel devices can be as large as two or three, depending on bias condition. Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying with noise generator, which results in:

$$\overline{v_{rg}^2} = 4kT\delta r_g \Delta f \tag{2}$$

where δ is the coefficient of gate noise, normally equal to 4/3 for long channel devices and r_g is the gate resistance. The gate resistance can be minimized through interdigitation without the need of increased power dissipation, thus it is rendered insignificant [2]. If the sizes of the MOS transistors are carefully chosen, the optimum W_t which is simply a ratio of g_m/C_{gs} can be obtained. Therefore, the minimum noise figure can be achieved according to [3]:

$$F_{min} = 1 + \frac{w}{w_t}\sqrt{\gamma\delta\zeta(1-|c|^2)} \tag{3}$$

If δ were zero, the minimum noise figure would be 0dB[4]

To achieve lower noise and higher gain, the casecode with the inductor generation topology is employed and shown in Figure 1.

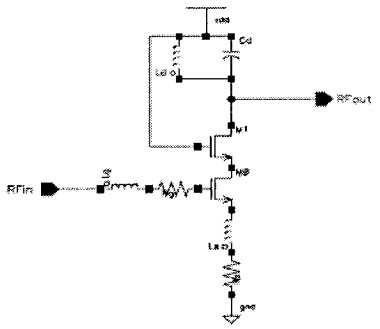

Figure 1. Schematic of a cascode topology with inductively degenerated .

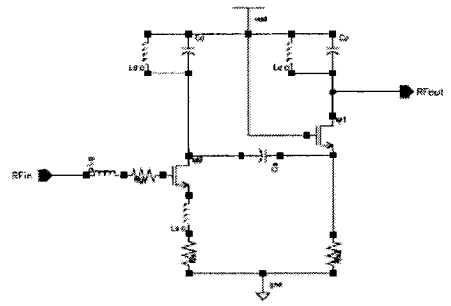

Figure 2. Common Source Common Gate Topology

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Figure1 is:

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{C_{gs} S} + S(L_S + L_g) + R_g \quad (4)$$

where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_0 respectively. L_g and L_s are the gate and source inductors and R_g is the effective gate resistance of M_0 given by $R_g = R_0 / \left(3_n{}^2 L\right)$ where R_0 is the sheet resistance of the gate polysilicon, W and L are the gate width and length of the transistor M_0 respectively and n is the number of fingers [2].

At the resonant operating frequency(w_0), the input matching area requires that:

$$Z_{in} = R_s = \omega_t L_s \quad (5)$$

The C_{gs} source degeneration inductance L_s is chosen together with W_t to provide the desired input resistance Rs, the real term can be made equal to 50 ohm without the existence of a real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met.

III. LNA DESIGN APPROACH

For LNA design, inductive source degeneration is used to achieve good input matching without adding thermal noise introduced by real resistor. The cascode topology is a popular configuration for LNA design but proposed topology offers a power supply less than that of cascode LNA .

The proposed topology is shown in Figure 2, which works for sub 1 volt low power supply applications, in our case it is 0.65V. Inductive source degeneration is also used to achieve good input matching and reduce noise figure. The first stage is inductively degenerated common-source amplifier formed by transistor M_0. Followed by a common-gate configurated transistor M_1. The value of LC tank of M_0 is carefully chosen to achieve a resonance frequency of 2.4GHz and is required to have a much higher impedance than that of the input impedance looked at the source of M_1. It provides a DC bias current path and a high impedance branch to force the RF signal to flow into the source of M_1 through a big DC coupling capacitance C_s .

The input impedance of the LC tank (L_d, C_d) is

$$Z_d = R_d + \frac{\omega^2 L_d{}^2}{R_d} \approx \frac{\omega^2 L_d{}^2}{R_d} = R_d Q_d^2 \quad (6)$$

Then,

$$g_{m1} \approx \frac{1}{R_d Q^2 d} \quad (7)$$

where R_d and Q_d are the resistance and the quality factor associated with the inductor L_d.

The input impedance at the source of the common gate transistor M_1 is:

$$R_i = \frac{1}{g_{m1} + g_{mb1}} \approx \frac{1}{g_{m2}} \quad (8)$$

where g_{mb} is the bulk transconductance.

To make the cascode LNA works at 0.65V, the well-Source junction of the NMOS transistors are forward biased as shown in Fig. 2 which causes the threshold voltage to decrease. The body effect feedback is based on the following expression.

$$V_T = V_{TO} + \gamma \left[\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}\right] \quad (9)$$

which,V_{TO} the intrinsic threshold voltage, γ the body effect coefficient, ϕ_f the surface inversion potential of silicon and V_{BS} the bulk-source voltage. By applying a voltage on V_{BS} we can control the threshold voltage V_T and thus the polarization of the transistor. Bulk-source operation is important because the threshold is reduced, the value of Vgs for the same current is less.

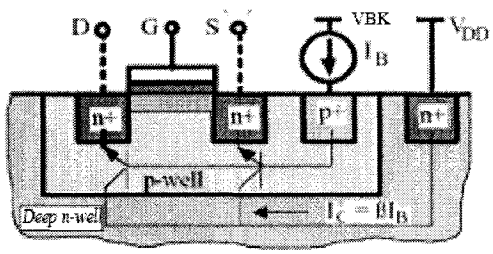

Figure 3. Cross-Section of a forward-biased NMOS transistor

IV. Simulation Results

The complete circuit is shown in Figure 4. The LNA first

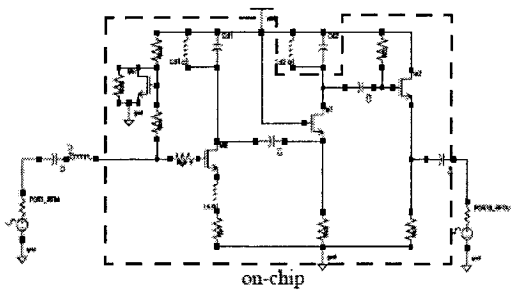

Figure 4. Complete shcematic of proposed common-soure, common-gate LNA

stage M_0 is inductively degenerated representing the common-source amplifier followed by M_1 configured as common-gate device. M_b sets the dc bias for M_0. M_2 is configured as the buffer stage for LNA output matching. C_1 between M_0 and M_1 is acting as a DC coupling capacitance to block DC and provides ac path to let RF signal flow into the source of common-gate transistor M_1. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip. As shown in Figure 4 only the framed components are on-chip.

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process. After noise optimization a low noise figure of 1.1 dB at 2.4 GHz is achieved and shown in Figure 6.

The S-parameters of the LNA are illustrated in Figure 5-8. Figure 5 shows a forward power gain (S21) of 27 dB at 2.4 GHz. The S11 shows a good input match at -11dB.The S22 shows a good output match with the output buffer which achieves -32dB. The IIP3 simulation result of the LNA is shown in Figure 9. A two-tone signal which are chosen close to each other has been applied to the input port. The input-referred

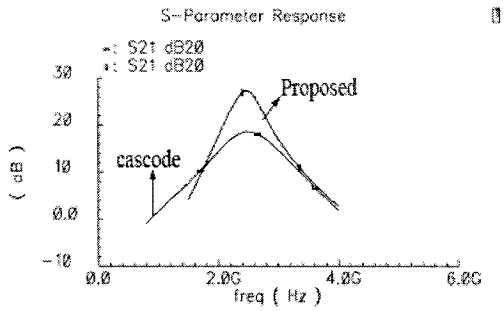

Figure 5. Power gain of proposed LNA vs Cascode LNA

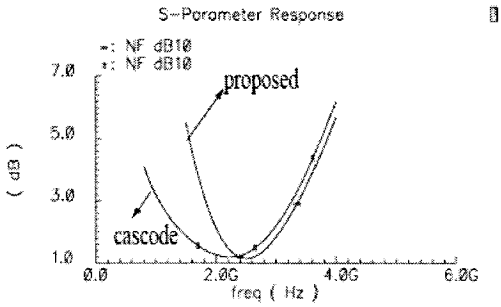

Figure 6. Noise figure of proposed LNA vs Cascode LNA

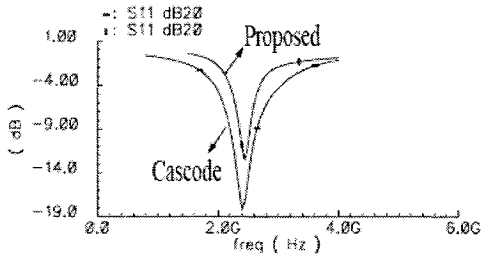

Figure 7. S11 of proposed LNA vs Cascode LNA

third-order intercept points (IIP3) is -30dBm. The final comparison of two topologies is shown in table 1.

The layout of the LNA is shown in Figure 9. The chip area is 0.9mm x 0.9mm. This work is placed alongside with other recent reported LNA in Table 1.It shows that with the noise optimization techniques the proposed LNA achieves a much lower noise figure than other LNAs.

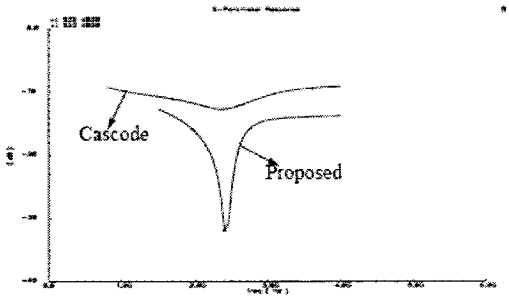

Figure 8. S22 of proposed LNA vs Cascode LNA

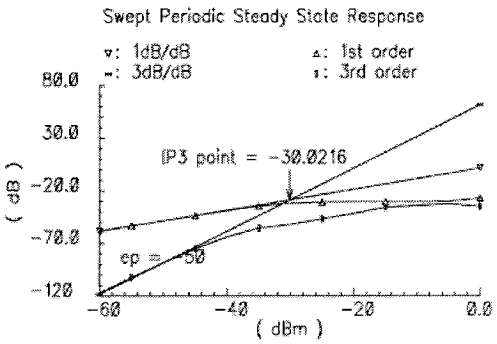

Figure 9. IIP3 simulation of the proposed LNA

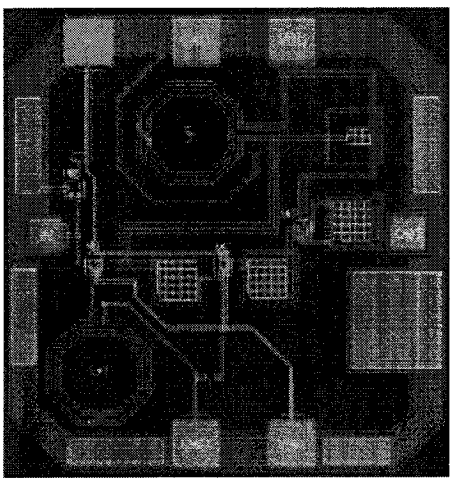

Figure 10. Layout of the proposed LNA

V. CONCLUSIONS

In this paper, a new CMOS low noise amplifier using common-source inductive source degeneration followed by common-gate configurations is proposed. The proposed topology is suitable for low power supply application and works good at 0.65 V voltage supply. Spectre simulation using TSMC 0.18μm CMOS technology shows a low noise figure of 1.1 dB, high power gain (S21) of 27 dB and low power consumption of 4.6 mW from 0.65 V power supply.

ACKNOWLEDGEMENT

The research was supported by a grant awarded to Dr. R. Raut by the Natural Science and Research Council (NSERC) of Canada

Reference	[7]	[6]	[5]	[4]	cascode	proposed
Freq.(G Hz)	2.4	2.4	2.4	2.4	2.4	2.4
NF(dB)	2.4	1.6	4.0	2.0	1.2	1.1
S_{21}(dB)	19	25	12	19	19.5	27
IIP_3(dBm)	-	-8	-2	-	-27.4	-30.0
Supply Voltage(v)	3	1.5	1.8	-	0.8	0.65
Power(mw)	9	16	14.3	40.8	5.6	4.6
Tech(um)	0.5	0.18	0.18	0.3	0.18	0.18

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A VERY LOW VOLTAGE, 1GHz CMOS LOW-NOISE AMPLIFIERS

M. Zamin Khan
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: mz_khan@ece.concordia.ca

R. Raut
Department of Electrical and Computer Engineering
Concordia University
Montreal, Canada
H3G 1M8
e-mail: rabinr@ece.concordia.ca

Abstract-**A 0.7 V, 1 GHz low noise amplifier (LNA) has been designed and simulated using Spectre simulator in a standard TSMC 0.18um CMOS technology. With low power and noise optimization techniques, the amplifier provides a gain of 23 dB, a noise figure of only 1.1 dB, power dissipation of 8.4 mW from a 0.7 V power supply.**

I. INTRODUCTION

Recently there has been much interest in using CMOS for Rf ICs operating in the 900MHz to 2.5Ghz rang.This frequency range is used by cellular phone applications such as GSM(Global system for Mobile Communication), and cordless application such as DECT(Digital Enhanced Cordless Telecommunication). Commonly a low noise amplifier (LNA) is a key component in RF front-end receiver which poses a challenge in terms of meeting high gain, low noise figure and linearity requirement at sub 1 volt power supply (such as 0.7 V). The primary role of the LNA is to lower the overall noise figure of the entire RF front-end, noise optimization is considered as one of the most critical steps in the LNA design procedure.

The noise figure (NF) of LNA should not exceed a 3 dB, assuming it has a gain more than 10 dB [1]. The design of LNA is full of trade-offs between optimum gain, lowest noise figure, high linearity and low power consumption. Casecode topology is one of the most popular topology used for CMOS LNA design, which provides high gain, low noise, but it is not suitable for low power supply. The consideration for noise optimization of LNA is illustrated in Section II. The proposed LNA design suitable for sub 1V power supply is analyzed in Section III. Spectre simulation results and a comparison with other reported LNAs are presented in Section IV. Section V concludes the paper.

II. NOISE FIGURE AND OPTIMIZATION

A. Noise Figure

An LNA determines the performance of the communication systems. It needs higher linearity and sufficient gain to overcome the next stage noise but not to overload. A system noise factor is defined as:

$$F_{total} = F_1 + \frac{F_1 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} + \ldots \quad (1)$$

where F_n (n=1,2,3,....) is the noise factor of each stage.G_n(n=1,2,3,...)is the gain of each stage. In our circumstances, F_1 is the noise factor of the LNA and G_1 is the gain of the LNA which implies that higher gain and lower noise of LNA will lower the total noise of the system. Noise figure represents how much the given system degrades the signal-to-noise ratio, which is defined as:

$$NF = 10\log\frac{TotalOutputNoisePower}{OutputNoisePowerBySourceImpedance} \quad (2)$$

CMOS LNA design provides high level of integration at low cost but it is a big challenge to achieve low noise performance because of the noisy nature of MOS device. The dominant noise source in MOS devices is channel noise:[2]

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \quad (3)$$

Where g_{do} is the zero-bias drain conductance of the device. γ is a bias dependent factor which, for long channel device satisfies $\frac{2}{3} \le \gamma \le 1$,but for short channel devices can be as large as two or three, depending on bias condition. Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying with noise generator, which results in:

$$\overline{v_{rg}^2} = 4kT\delta r_g \Delta f \quad (4)$$

where δ is the coefficient of gate noise, normally equal to 4/3 for long channel devices and r_g is the gate resistance. The gate resistance can be minimized through interdigitation without the need of increased power dissipation, thus it is rendered insignificant [2]. If the sizes of the MOS transistors are carefully chosen, the optimum ω_t which is simply a ratio of g_m/C_{gs} can be obtained. Therefore, the minimum noise figure can be achieved according to [3]:

$$F_{min} = 1 + \frac{w}{w_t}\sqrt{\gamma\delta\zeta(1-|c|^2)} \quad (5)$$

If δ were zero, the minimum noise figure would be 0dB[4].

B. Noise Optimization

To achieve lower noise and higher gain, the Common-source with the inductor degeneration topology is employed and shown in Figure 1.

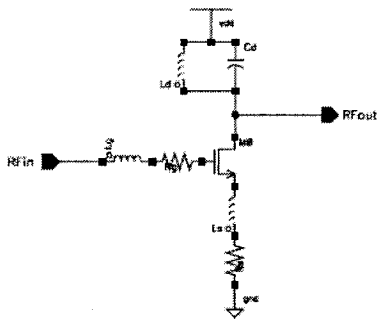

Figure 1. INDUCTIVE LY DEGENERATED COMMON SOURCE AMPLIFIER

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Figure1 is:[4]

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{C_{gs} S} + S(L_S + L_g) + R_g \qquad (6)$$

where g_m and C_{gs} are the transconductance and the gate-to-source capacitance of the input device M_0 respectively. L_g and L_s are the gate and source inductors and R_g is the effective gate resistance of M_0 given by $R_g = R_0 / \left(3_n^2 L\right)$ where R_0 is the sheet resistance of the gate polysilicon,W and L are the gate width and length of the transistor M_0 respectively and n is the number of fingers [2].

At the resonant operating frequency(w_0), the input matching requires that:

$$Z_{in} = R_s = \omega_t L_s \qquad (7)$$

The C_{gs} source degeneration inductance L_s is chosen together with ω_t to provide the desired input resistance Rs, the real term can be made equal to 50 ohm without the existence of a real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met.

III. DESIGN APPROACH

To make the LNA works at 0.7V, the well-Source junction of the NMOS transistors are forward biased which causing the threshold voltage to decrease. The threshold voltage with body effect is based on the following expression.

$$V_{TO} + \gamma[\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}] \qquad (8)$$

which, V_{TO} the intrinsic threshold voltage, γ the body effect coefficient, ϕ_f the surface inversion potential of silicon and V_{BS} the bulk-source voltage. By applying a voltage on V_{BS} we can control the threshold voltage V_T and thus the polarization of the transistor. In this LNA design, the V_T canbe decreased from 0.5V to 0.4V and the value of current through bulk is 10 uA although this current is undesirable.

For LNA design, inductive source degeneration is used to achieve good input matching without adding thermal noise introduced by real resistor. The proposed topology is shown in Figure 3, which works for sub 1 volt low power supply applications, in our case it is 0.7V. Inductive source degeneration is used to achieve good input matching and reduce noise figure. The first stage is inductively degenerated common-source amplifier formed by transistor M_0. Followed by a common-gate configurated transistor M_1. The value of LC tank of M_0 is carefully chosen to achieve a resonance frequency of 1GHz and is required to have a much higher impedance than that of the input impedance looked at the source of M_1. It provides a DC bias current path and a high impedance branch to force the RF signal to flow into the source of M_1 through a big DC coupling capacitance C_s.

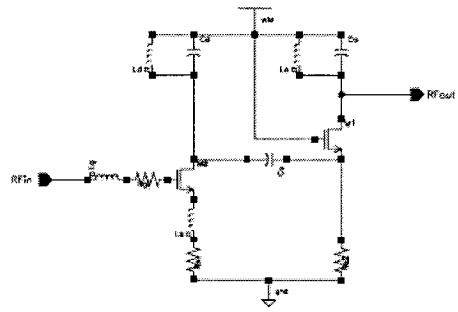

Figure 2. COMMON SOURCE COMMON GATE TOPOLOGY

The input impedance of the LC tank (L_d,C_d) is

$$Z_d = R_d + \frac{\omega^2 L_d^2}{R_d} \approx \frac{\omega^2 L_d^2}{R_d} = R_d Q_d^2 \qquad (9)$$

Then,

$$g_{m1} \approx \frac{1}{R_d Q^2 d} \qquad (10)$$

If $R_L << r_{ds}$, where R_d and Q_d are the resistance and the quality factor associated with the inductor L_d.
The input impedance at the source of the common gate transistor M_1 is:

$$R_i = \frac{1}{g_{m1} + g_{mb1}} \approx \frac{1}{g_{m2}} \quad (11)$$

where g_{mb} is the bulk transconductance.

IV. Simulation Results

The complete circuit is shown in Figure 3. The LNA first

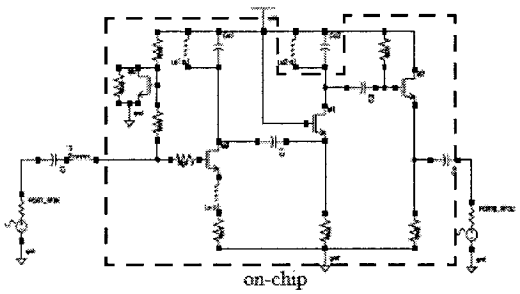

Figure 3. Complete shcematic of proposed common-soure, common-gate LNA

stage M_0 is inductively degenerated representing this common-source amplifier followed by M_1 configured as common-gate device. M_b sets the dc bias for M_0. M_2 is configured as the buffer stage for LNA output matching. C_1 between M_0 and M_1 is acting as a DC coupling capacitance to block DC and provides ac path to let RF signal flow into the source of common-gate transistor M_1. In our case, it is designed to be 10 pF. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip. As shown in Figure 3 only the framed components are on-chip.

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process. After noise optimization a low noise figure of 1.1 dB at 1 GHz is achieved and shown in Figure 5.

The S-parameters of the LNA are illustrated in Figure 4,6, and 7. Figure 4 shows a forward power gain (S21) of 23 dB at 1 GHz. The S11 shows a good input match at -13.5dB.The S22 shows a good output match with the output buffer which achieves -21dB.The IIP3 simulation result of the LNA is shown in Figure 8. A two-tone signal which are chosen close to each other has been applied to the input port. The input-referred third-order intercept points (IIP3) is -29dBm.

The layout of the LNA is shown in Figure 8. The chip area is 0.9mm x 0.9mm. This work is placed alongside with other

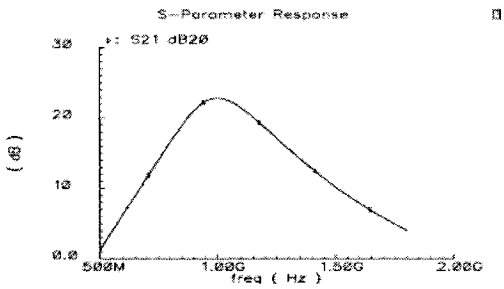

Figure 4. Power gain of proposed LNA

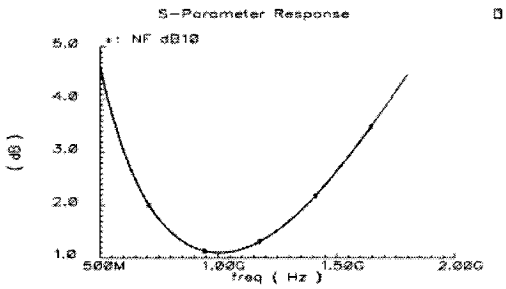

Figure 5. Noise figure of proposed LNA

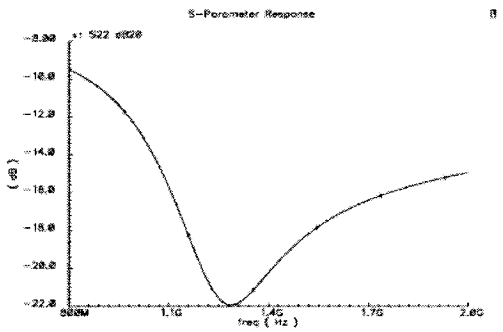

Figure 6. S22 of proposed LNA

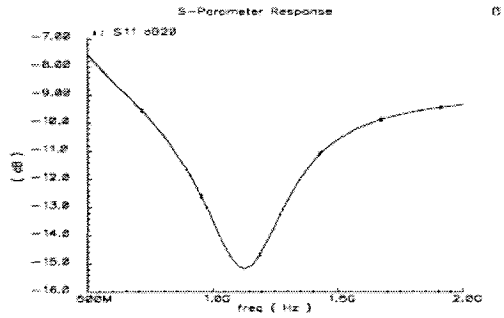

Figure 7. S11 of proposed LNA

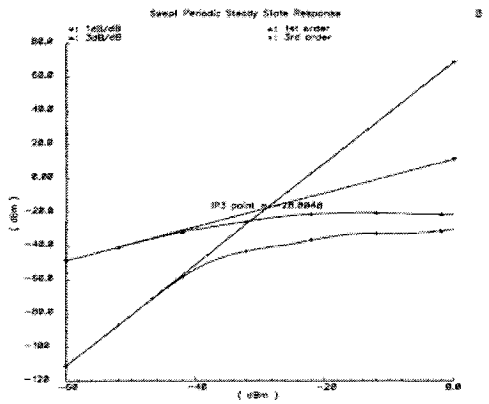

Figure 8. IIp3 simulation of the proposed LNA

recent reported LNA in Table 1. It shows that with the noise

Table 1: Comparison of Various Recent Reported LNAs

Reference	[5]	[6]	[7]	[8]	[1]	This Work
Freq(G Hz)	0.9	0.9	0.9	1	1	1
NF(dB)	2	2.5	6	3.5	2.7	1.1
S_{21}(dB)	17.5	9	17	22	12.2	23
$IIP_{3(dBm)}$	-6	-4.7	-14	12	-21	-29
Power(mw)	-	10	78	27	17	8.4
Tech(um)	0.35	0.5	0.8	1.0	0.5	0.18

optimization techniques the proposed LNA achieves a much lower noise figure than other LNAs.

V. CONCLUSIONS

In this paper, a new CMOS low noise amplifier using common-source inductive source degeneration followed by com-

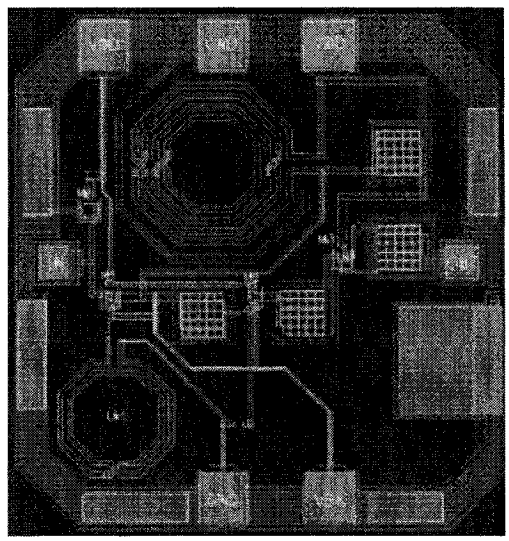

Figure 9. Layout of the proposed LNA

mon-gate configurations is proposed. The proposed topology is suitable for low power supply application and works good at 0.7 V voltage supply. Spectre simulation using TSMC 0.18μm CMOS technology shows a low noise figure of 1.1 dB, high power gain (S21) of 23 dB and low power consumption of 8.4 mW from 0.7 V power supply.

ACKNOWLEDGEMENT

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