Simulation of Controller Configurations for Static Synchronous Series Compensators & Interline Power Flow Controllers with EMTP-RV

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Abstract

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This thesis deals with Flexible AC Transmission Systems (FACTS) based on Voltage Source Converters (VSC). In particular, the emphasis is on series-connected VSC into transmission lines, known as Static Synchronous Series Compensator (SSSC) and Interline Power Flow Controller (IPFC). These are modern series compensators with fast response and high performance.

The SSSC and IPFC applications are simulated with the help of EMTP-RV software, where detailed models of the power system and controllers are implemented and the dynamic performances are considered.

The proposed VSC is based on a 3-level Neutral-Point-Clamped (NPC) VSC employing PWM techniques to generate firing pulses for the VSC switches. The VSC main circuit configuration, function and operating principles are first described.

The proposed VSC is used as the major building block of the SSSC. The detailed model of SSSC (with two different control strategies) is then presented. The controllers are designed to regulate the transmission line impedance by injecting a set of 3-phase voltages with controllable magnitude and phase angle. The stability of the proposed SSSC under various system conditions is investigated and the two different control strategies are compared.

Finally, two SSSCs with a common DC-link are used to configure an IPFC. The proposed IPFC is applied to two parallel transmission lines to regulate their impedances. The validity of the proposed control techniques under various system conditions is also investigated.

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List of Acronyms

CSC:	Current Source Converter
EMTP-RV:	Electro Magnetic Transients Program Restructured Version
FACTS:	Flexible AC transmission System
FC:	Fixed Capacitor
GTO:	Gate Turn-off Thyristors
GUPFC:	Generalized Unified Power Flow Controller
IEGT:	Injection Enhanced Gate Transistor
IGBT:	Insulated Gate Bipolar Transistor
IGCT:	Integrated Gate-commutated Thyristor
IPFC:	Interline Power Flow Controller
NPC:	Neutral Point Clamped
PWM:	Pulse width Modulation
SSSC:	Static Synchronous Series Compensator
STATCOM:	Static Synchronous compensator
SVC:	Static Var Compensators
TCR:	Thyristor Controlled reactor
TCSC:	Thyristor-controlled Series Capacitor
TSC:	Thyristor Switched capacitor
TSSC:	Thyristor Switched Series Capacitor
UPFC:	Unified Power Flow Controller
VSC:	Voltage Source Converter

Chapter 1

Introduction

1.1 General

Over the past few years, improving the traditional power transmission systems to utilize the maximum apparatus capacities as well as maintaining reliability and security of power systems have become important concerns. The rising electrical energy demand, both in developing and developed countries, is pushing transmission systems closer to their thermal and stability limits. Furthermore, the conventional transmission systems are not able to manage the control requirements of today's complex and vastly interconnected grid. Thus, fierce competition in the power market is now a reality, since deregulation has occurred in many countries. More profitable operation, as well as improved security and reliability in power systems, are demanded by shareholders and consumers. The conventional solutions of developing the power systems by constructing new transmission lines, substations, and power plants are both expensive and difficult to justify. In the past years, different approaches such as series/shunt compensation and phase shifting have been applied to increase the load-ability and consequently the security of the power systems. These devices were mechanically controlled so they were relatively slow to damp out dynamic and transient oscillations and were only useful in steady state operation. Therefore, transmission systems were designed with large stability margin as a protection against dynamic and transient problems.

The development of high power semiconductor switches opened up a new era of control techniques in power transmission systems. These applications with advanced control technology were introduced as alternatives to improve the utilization of the existing power systems and improve their operational reliability. Known as Flexible AC Transmission Systems (FACTS), these power electronic-based equipments provide cost-effective solutions to new operating requirements of modern power systems.

Power electronics technology was first applied in power systems compensation in the 1970's with the introduction of high power semiconductor diodes and thyristors [2]. Some of the first applications were in High Voltage DC (HVDC) transmission systems. In parallel, Static Var Compensators (SVC) using solid-state switches were employed in AC systems for var compensation. Hingorani first defined the concept of FACTS in 1988 as High power electronics and flexible AC transmission system [7]. At first, Thyristor Controlled Reactor (TCR) and Thyristor Switched Capacitor (TSC) were developed and installed individually or together with conventional capacitors [3],[4]. The rapid development of solid-state switches, with higher voltage/current ratings, and turn-off ability (i.e. GTOs and IGBTs), facilitated the production of a new generation of FACTS controllers based on converter topology.

1.2 Flexible AC Transmission System (FACTS)

The FACTS devices represent a relatively new technology for power transmission systems. They provide the same benefits as conventional compensators with mechanical switches (circuit breakers) in steady-state power system operation; in addition, they improve the dynamic and transient performance of the power system. This is achieved by fast switching time and repeatable operation of solid-state switches as compared to

mechanical switches. The switching time of a solid-state switch is a portion of a periodic cycle; and this is much faster than that of a circuit breaker with a switching time of a number of cycles. In addition, the other advantages of FACTS controllers are their smooth control and repeatable operation [7][8]. Recent advances in semiconductor technology have introduced solid-state switches with higher voltage and current for thyristors (8.5 kV and 4.5 kA), and for Gate turn-off thyristors (GTOs) (6 kV and 6 kA). Also, Insulated Gate Bipolar Transistors (IGBTs) are used for converters with lower rating range, but with higher switching frequencies in the range of up to 3-10 kHz [9].

FACTS controllers can be categorized into two major groups:

- Thyristor-controlled FACTS controller
- Converter-based FACTS controller

Thyristor-controlled FACTS controllers operate by switching a capacitor/reactor in series/shunt to the power system. They provide rapid, continuous control of reactive power over the selected lagging/leading power factor range. Several units have been installed since 1991; one of the first installations was a Thyristor Switched Series Capacitor (TSSC) on a series capacitive compensated 345 kV transmission lines in West Virginia[3].

In converter-based FACTS controllers, either a Voltage Source Converter (VSC) or a Current Source Converter (CSC) is used to generate an appropriate current or voltage, and inject it into the power transmission line. Converter-based FACTS controllers include the Static Synchronous Compensator (STATCOM) for shunt reactive power compensation, the Static Synchronous Series Compensation (SSSC) for series reactive compensation, the Unified Power Flow Controller (UPFC) with unique capability of

independently controlling both the active and reactive power flow in the line, and the Interline Power Flow Controller (IPFC) to control active and reactive power flow in parallel lines. In 1991, the first ± 80 Mvar Static synchronous Compensator (STATCOM) was installed at the Inuyama switching station in Japan [5], [6].

The following definitions for FACTS and FACTS controllers are defined by IEEE Power Engineering Society (PES) Task Force of FACTS working group [10]:

- ***Flexible AC Transmission System (FACTS):*** Alternating current transmission systems incorporating power electronic-based and other static controllers to enhance controllability and increase power transfer capability.
- ***FACTS Controller:*** A power electronic-based system and other static equipment that provide control of one or more AC transmission system parameters.

1.3 Power transmission system constraints

The three major factors that limit the loading capability of transmission lines can be categorized as thermal limits, voltage drop limits and stability limits [11]. Thermal limit is a function of ambient temperature, wind condition, conductor loading, and ground clearance. Voltage drops are limited by designed tolerance (about 10% over-voltage), besides the transient over voltage. From the stability point of view, the following items limit the transmission line capability:

- Transient stability
- Dynamic stability
- Steady-state stability
- Frequency collapse

- Voltage collapse
- Subsynchronous Resonance (SSR)

The load-ability of a short length line (less than 80 km) is determined by its thermal limit. For a medium length line (less than 300 km), the voltage drop is the limiting factor. And in long transmission lines (over 300 km), the stability is the main concern in load-ability of the line [11].

In the past, power systems were protected against dynamic changes of power flow by using appropriate stability margins. Devices such as shunt/series capacitors, used to increase the line loading and security of the power system were controlled mechanically. Therefore, they were only suitable for steady state operation in power systems [11].

1.4 Basic principle of active and reactive power flow control

A basic model of a power transmission system is shown in Figure 1-1. The two voltage sources could be two power systems which contain generators and loads. V_s and V_R are the sending-end and receiving-end voltages respectively, while δ is the phase angle between these voltages. The line resistance is neglected, and the transmission line impedance can be represented by its reactance X.

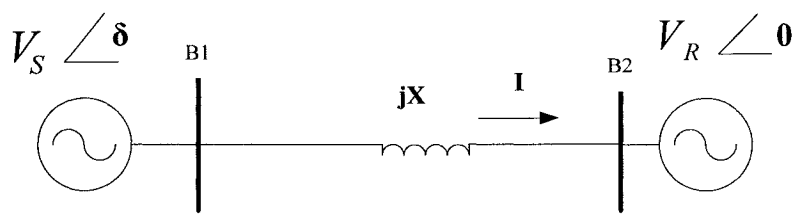

Figure 1-1: Power transmission line model

Figure 1-2 shows the voltage phasor diagram of such a system. The line current is perpendicular to the voltage drop $(V_s - V_R)$ in the transmission line. The active and reactive components of the transmission line current at the sending end are:

$$I_{ps} = \frac{(V_R \sin\delta)}{X}$$
$$I_{qs} = \frac{(V_s - V_R \cos\delta)}{X} \qquad (1\text{-}1)$$

And similar equations for transmission line current at the receiving end are:

$$I_{pR} = \frac{(V_s \sin\delta)}{X}$$
$$I_{qR} = \frac{(V_R - V_s \cos\delta)}{X} \qquad (1\text{-}2)$$

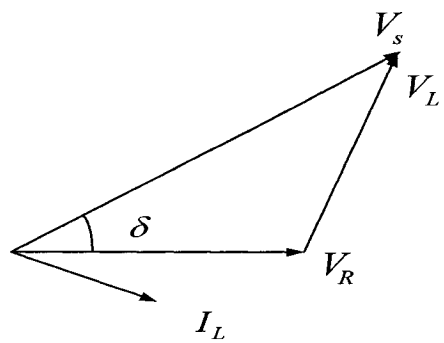

Figure 1-2: Voltage phasor diagram of the transmission line

Hence, the active and reactive power in the sending-end and the receiving-end can be obtained. Since the active power loss in the transmission line in Figure 1-1 is zero, the sending-end and receiving-end active powers are equal (i.e. $P_S=P_R$). Therefore, the active power at the sending-end and receiving-end is:

$$P = \frac{V_s * V_R}{X} \sin \delta \tag{1-3}$$

where δ is the angle between the two voltage sources.

The reactive power at the sending-end is:

$$Q_s = \frac{V_s(V_s - V_R \cos \delta)}{X} \tag{1-4}$$

and the reactive power at the receiving-end can be found from:

$$Q_R = \frac{V_R(V_S \cos \delta - V_R)}{X} \tag{1-5}$$

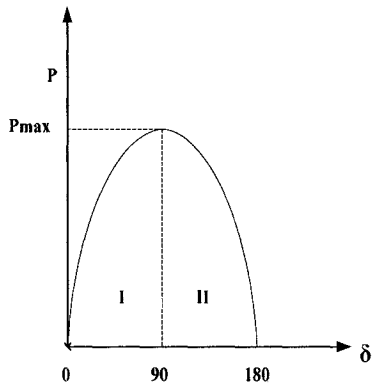

Figure 1-3: Power angle curve

Equations (1-2) to (1-5) show that controlling the voltage, angle and/or impedance of the power system can regulate the active and reactive power. Impedance control is more effective in active power flow control. Regulating sending-end and receiving-end voltages is more effective in reactive power flow control. Figure 1-3 demonstrates the power angle curve of the system shown in Figure 1-1. The maximum active power occurs

at $\delta = 90$ degrees, but the system is only stable if the derivative $\frac{dP}{d\delta}$ is positive and operates in Area I of Figure 1-3. In order to keep the power system stable from dynamic and transient oscillations, an adequate margin must also be maintained. In practice, the transmission angle is kept below 45 degrees [14].

1.5 Compensation in AC transmission lines

Reactive power compensators have been applied in power systems to increase steady-state power transmission by regulating voltage profile along the transmission lines. Conventionally, fixed or mechanically switched reactors/capacitors have been used for this purpose. Besides this, rotating synchronous condensers have been also employed in transmission lines for reactive shunt compensation. They have high capacitive output current at low system voltages and do not generate harmonics that resonate with the grid. However, they are vulnerable to rotating instability and have slow response with low short circuit impedance, and high maintenance cost [12]. The new generation of compensators is based on power electronic devices. They are suitable for fast reactive power compensation in power systems. Therefore, they are effective in dynamic compensation and real time control of power flow in power systems. These compensators are used in series, shunt or a combination of them in power transmission lines for different purposes. In the following sections, the concepts of shunt and series compensation are briefly reviewed.

1.5.1. Shunt compensation

Basically, shunt compensators are used to regulate the voltage in a transmission line; this is achieved by exchanging reactive power with the transmission line. Shunt reactors are used to reduce the line over-voltage under light loads, and shunt capacitors are applied to keep voltage at the desired level under heavy load conditions [1].

In Figure 1-4, a simple model of a transmission line is shown in which a shunt compensator is connected at the midpoint of the transmission line. Sending-end and receiving-end voltages are assumed equal (i.e. $V_s = V_R = V$), and an inductor (X_L) represents the line impedance.

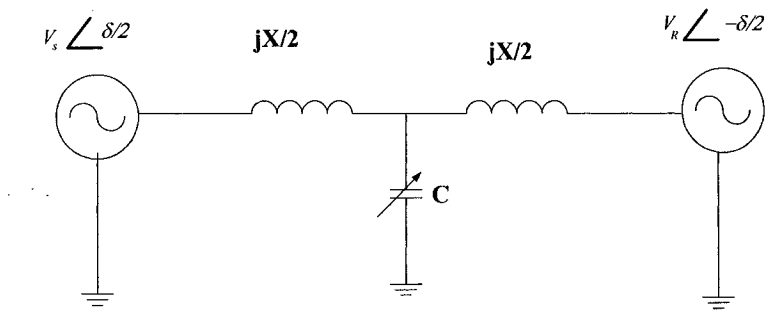

Figure 1-4: Power transmission line model with shunt compensation

While the transmission line is lossless, the active power at the sending-end and receiving-end are identical and can be obtained from the following equation:

$$P_c = 2\frac{V^2}{X_L}\sin\frac{\delta}{2} \qquad (1\text{-}6)$$

where δ is the phase angle between sending-end and receiving-end voltages. The reactive power is:

$$Q_c = 4\frac{V^2}{X_L}(1-\cos\frac{\delta}{2}) \qquad (1\text{-}7)$$

Figure 1-5 shows the P_c (active power with an ideal midpoint compensator), P (active power without compensator) versus δ characteristic of the shunt compensation model (Figure 1-4). The transmitted power is significantly increased compared to an uncompensated line.

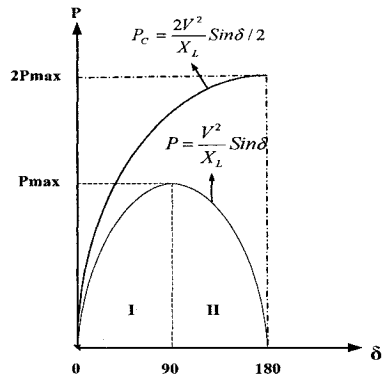

Figure 1-5: Active power versus transmission line angle

The thyristor-based FACTS controllers are well known and widely used in power system compensation since the late 70s. Generally, a combination of thyristor-based FACTS controllers with fixed capacitors is used. Figure 1-6 shows two typical configurations of Static Var Compensators (SVC). In Figure 1-6a, the SVC consists of a TCR, a TSC and fixed capacitor (FC). Figure 1-6b shows a TCR and FC together. By controlling the firing angles of the thyristors, reactive power compensation can be adjusted to the desired value. One of the first SVCs, with 40 Mvar rating, was installed at the Shannon substation in Minnesota Power and Light system in 1978 [13].

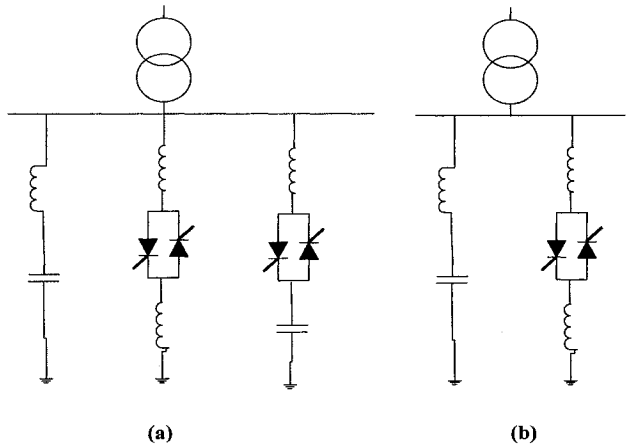

Figure 1-6: Static var compensator (a) TCR, TSC, and FC (b) TCR, and FC

A FACTS shunt compensation scheme, called STATCOM, is shown in Figure 1-7. A STATCOM generates a set of 3-phase voltages in phase with the transmission line voltages, and is capable of exchanging reactive power with the line. By regulating the STATCOM voltage, V_{inj}, the direction of the reactive power can be controlled [14].

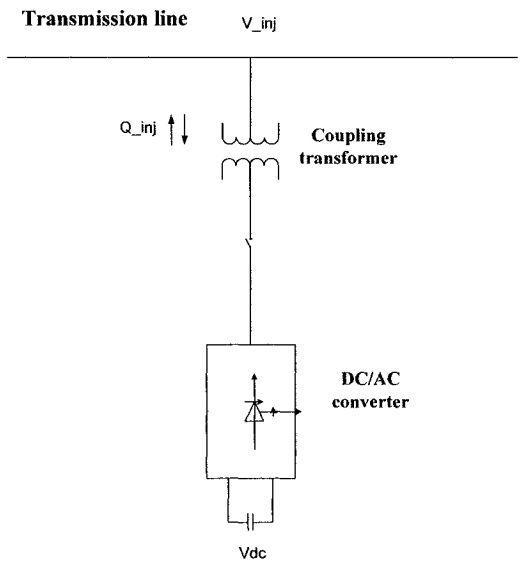

Figure 1-7: Schematic of STATCOM

1.5.1 Series compensation

The purpose of series compensation in power transmission lines is to control the reactive line impedance. In fact, by adding a series compensator such as a capacitor, a series voltage in opposition to the transmission line voltage drop is injected; thereby, the voltage drop across the transmission line and the effective line impedance are reduced. Consequently, the transmission line current increases. The drawbacks of series compensators are the need for protection devices that must be installed for protecting against high currents during fault periods and also the possibility of subsynchronous resonance exists that may damage generator shafts [1],[3].

Figure 1-8a shows a simple model of a power system with a capacitor in series. Figure 1-8b shows the corresponding phasor diagram.

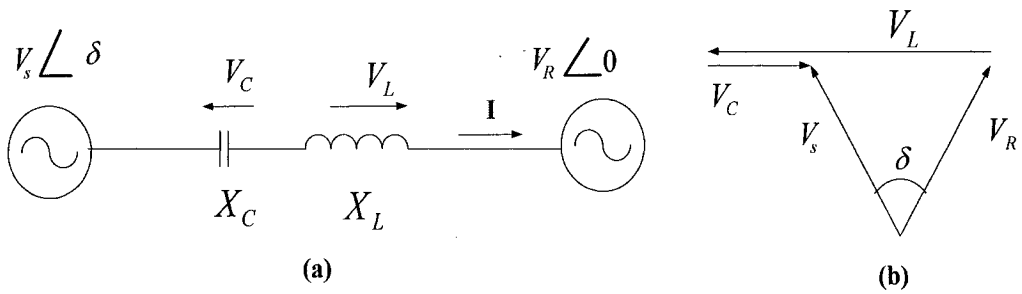

Figure 1-8: (a) Model of a power system with series compensation (b) Phasor diagram

Figure 1-9 shows a Thyristor-Controlled Series Capacitor (TCSC), which is a thyristor-based series FACTS controller. It is employed in transmission lines for rapid control of line reactance; by controlling the firing angle of the thyristors, the effective reactance value is changed.

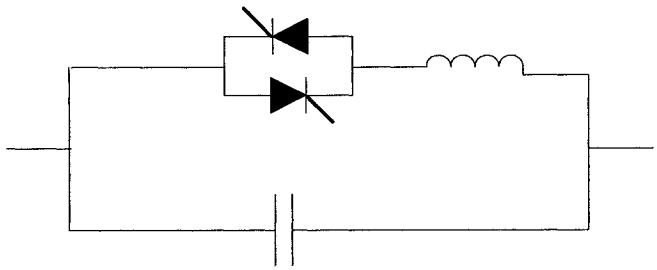

Figure 1-9: Schematic of TCSC

In converter-based FACTS controllers the same objective is achieved by adding a desired voltage in series with the transmission line. Figure 1-10 demonstrates a synchronous AC voltage source, whose output is equivalent to the voltage of the series capacitor ($V_{inj} = V_c = -jX_C I$). The Static Synchronous Series Compensator (SSSC) emulates the same functional behavior of a conventional series capacitor; in addition the following benefits are achieved by applying SSSC in a power transmission line [1].

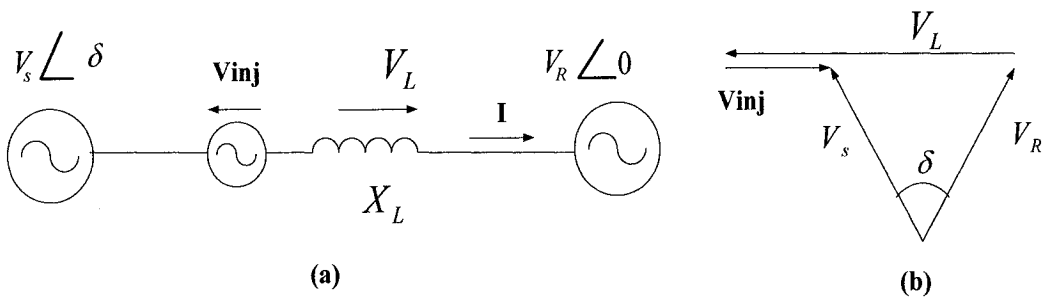

Figure 1-10: (a) Model of a power system with a synchronous voltage source in series (b) Phasor diagram

- **Transmitted power versus transmission angle characteristics**

The voltage across the capacitor is proportional to the line current i.e. a function of the angle between the sending-end and receiving-end voltages (transmission angle). By assuming $V_S = V_R$, the real transmitted power can be found from:

$$P = \frac{V_S V_R}{(1-k)X_L}\sin\delta = \frac{V^2}{(1-k)X_L}\sin\delta \qquad (1\text{-}8)$$

where $k = \frac{X_c}{X_l}$ is the degree of series compensation.

The transmitted power versus transmission angle is shown is Figure 1-11. By increasing the degree of compensation the transmitted power can be increased.

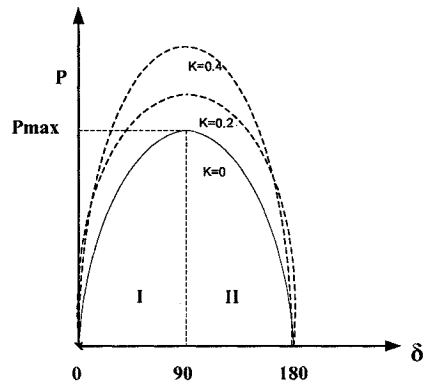

Figure 1-11: Transmitted power versus angle with various degrees of compensation

In SSSC, the series compensation degree is independent of the line current, and the transmitted power can be found from the following equation:

$$P = \frac{V^2}{X_L}\sin\delta + \frac{V}{X_L}V_{inj}\cos(\delta/2) \qquad (1\text{-}9)$$

Where the injected voltage, V_{inj}, is in quadrature with the line current. The transmitted powers versus transmitted angle curves are plotted in Figure 1-12.

As is shown in Figure 1-11 and 1-12, the transmitted power in the series capacitor increases by a fixed transition angle, but in SSSC the maximum transmitted power increases independently of the transmitted angle in the important range of $0 \leq \delta \leq 90°$ [1].

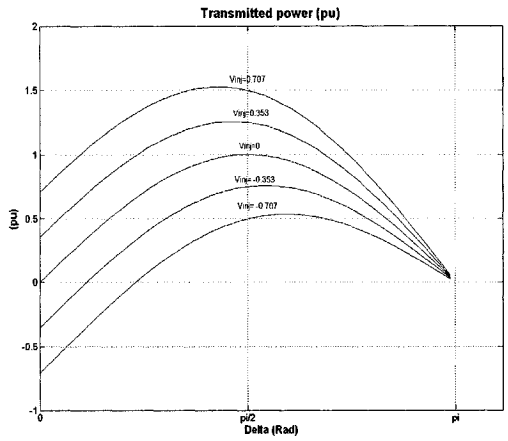

Figure 1-12: Transmitted power versus angle in SSSC

Also, the SSSC is capable of operating in both capacitive and inductive modes; therefore, it is able to operate as a reactor to decrease the line current.

- **Capability of active power compensation**

An important requirement in series compensation is to keep the ratio X/R high enough (over 10). A low ratio of X/R could gradually increase the reactive power demand, which results in line losses and voltage collapse. A SSSC, with the availability of an energy source, is able to exchange both reactive and active power with the transmission line. Therefore, SSSC is able to regulate both R and X in transmission lines in order to keep the X/R ratio high.

- **Immunity to subsynchronous resonance**

Series capacitors are vulnerable to subsynchronous resonance, but the fast response of a SSSC makes it capable of damping subsynchronous resonance.

1.6 Literature review

Since the focus of this thesis is on series connected VSC-based FACTS controllers, a brief literature review on this topic is presented below.

Gyugyi first proposed the converter-based, solid-state series compensator in 1979 [15]. Schauder and Mehta developed a mathematical model of a VSC with direct and indirect controllers by using Park's transformation in 1991[16]. In[17], Ooi et al reported a laboratory-based research on a series converter-based FACTS controller by using VSC and CSC topologies. They used a 1 kVA bipolar transistor converter with a 2-level Pulse Width Modulation (PWM) controller as the laboratory model. Gyugyi presented the application of a synchronous voltage source implemented by a multi-pulse GTO in AC transmission lines for series compensation in 1989[18] and introduced SSSC in 1996 [19]. Sen, Schauder, and Gyugyi first introduced the IPFC for multi-line transmission systems in 1999 [20]. A few papers on IPFC have been published that investigated the basic model and steady state operation of an IPFC [21], [22]. In [23], the ability of an IPFC in power flow control and damping system oscillation was considered. Much research has been done after developing the basic theory of a series converter-based FACTS controller. Several articles on SSSC have been published [24], [25], [28], and [44] to investigate the controller function and increase the efficiency of the converter's power circuit in order to reduce the losses and improve the quality of output voltage. IPFC is a relatively new topology and less published research is available on it [21], [22], [23]. Unlike STATCOM and UPFC, SSSC and IPFC have not been installed and utilized as yet in any transmission systems. More research is required in this area before practical use in power transmission systems.

1.7 Problem definition

This thesis investigates the theory and design of series converter-based FACTS controllers such as SSSC and IPFC. Both these applications use the VSC as the basic building block. The operating principles and design of the VSC are, therefore, first presented.

The thesis objective is to study the steady state and dynamic operation of VSCs in series with transmission systems. More precisely, the applications of SSSC and IPFC are considered. Both direct and indirect control methods in SSSC application are studied. Two SSSCs, with a common DC-link, are used to build an IPFC application. The models of the power system and the controllers are implemented using the EMTP-RV simulation package and results are obtained.

1.8 Thesis contributions

The Static Synchronous Series Compensator (SSSC) and the Interline Power Flow Controller (IPFC) are designed and implemented in EMTP-RV. The SSSC with direct and indirect controllers is presented and the dynamic performance of the two controllers is studied and compared. Several tests are conducted to validate the operation of the SSSC and the IPFC to compensate the impedance and limiting the fault current in the transmission line.

1.9 Thesis outline

Chapter 2 gives a general introduction to modeling, operating principles and passive component design of a 3-level Neutral Point Clamped (NPC) VSC. Also, the method to generate switching pulses for the converter is described. And finally, the VSC topologies in FACTS controllers are presented.

Chapter 3 concentrates on the application of a VSC in series with a power transmission line. This series connected VSC is called Static Synchronous Series Compensator (SSSC). The operating principle and control strategies that are used are explained. The simulation results, with an EMTP-RV model that includes a detailed representation of a 3-level PWM-controlled SSSC are given in this chapter.

Chapter 4 describes the operating principles and controller design of an Interline Power Flow Controller (IPFC). The theory and control function of the IPFC are explained, and the simulation results with EMTP-RV are presented.

Chapter 5 presents the conclusions and future direction of the research in this thesis.

1.10 Summary

This chapter gives a basic principle of series/ shunt compensation in transmission systems and the potential advantages of converter based FACTS controller for series/shunt compensation. Also it provides an overview of the thesis objectives, and methodology.

Chapter 2

Voltage Source Converter (VSC) and FACTS topologies

2.1 Introduction

Switch mode power converters are a major building block of converter-based FACTS controllers. A converter is capable of generating a set of 3-phase sinusoidal voltages with controllable magnitude and phase angle. In this chapter, the design fundamentals and basic operating principles of a 3-level Pulse Width Modulation (PWM) Voltage Source Converter (VSC) are explained. This PWM-controlled VSC is the basic building block of SSSC and IPFC that will be used for digital simulation in later chapters.

2.2 High power switch-mode converters

Voltage Source Converters (VSCs) and Current Source Converters (CSCs) are two major groups of power converters that are employed in FACTS devices. They are connected in series or shunt with the power transmission lines, and inject voltage or current with appropriate magnitude and phase angles. CSCs operate as a current source, and their DC side contains a current source such as a charged inductor. The DC current in CSC always has one polarity and power reversal takes place through a reversal of DC voltage polarity. Therefore, semiconductor switches with bi-directional voltage blocking must be used in CSCs. VSCs operate as a voltage source, and they have an energy source such as a charged capacitor on the DC side. In VSCs, the DC voltage always retains one polarity, and power reversal takes place through reversal of DC current polarity. So VSCs

require semiconductor switches with an ability of unidirectional voltage blocking. In FACTS applications, VSCs are preferred because of better performance and economical reasons. In this thesis, only VSCs are discussed and used for DC/AC conversion in FACTS controllers.

2.3 Power switches

Semiconductor switches that are suitable for high power FACTS applications include the Insulated Gate Bipolar Transistor (IGBT), the Gate Turn-off Thyristors (GTO), Injection Enhanced Gate Transistor (IEGT), and the Integrated Gate-Commutated Thyristor (IGCT). GTO and IGBT are likely to be replaced by new generation devices like the IGCT and IEGT respectively, because of their advantages [38]. IGCT and IEGT do not require individual snubber circuits. Also, an IGCT has better turn-off characteristics with lower switching and conducting losses when compared to a GTO and an IGBT. The maximum rating of an IEGT is presently 4.5kV/1.5 kA [39]. The maximum rating of an IGCT reaches 5.5-kV/1.8 kA for a reverse-conducting IGCT, and 4.5 kV/ 4 kA for an asymmetrical IGCT [40].

The cost of semiconductor switches for a 100 MVA installation is typically 1% of the total project cost [38]. However, it influences on the performance and, therefore, on the capital and operational cost of the applications. The following factors must be considered for selecting semiconductor switches:

1. Low cost
2. High reliability
3. Simple maintenance and assembly
4. Low dv/dt and di/dt

5. High voltage and current rating
6. Low losses (switching and conducting)
7. Fast switching
8. High frequency operation

2.4 Modeling of a 3-phase VSC

A VSC can be represented by a synchronous sinusoidal voltage source with controllable magnitude and phase angle. The scheme of a 3-phase VSC is shown in Figure 2-1. The series inductance "X_t" in the AC side of the VSC accounts for the leakage of the coupling transformer, and the series resistance "R_t" represent the transformer and VSC losses. The DC side of the VSC consists of a DC capacitor and a shunt resistance "R_{dc}" that represents the switching losses of the VSC.

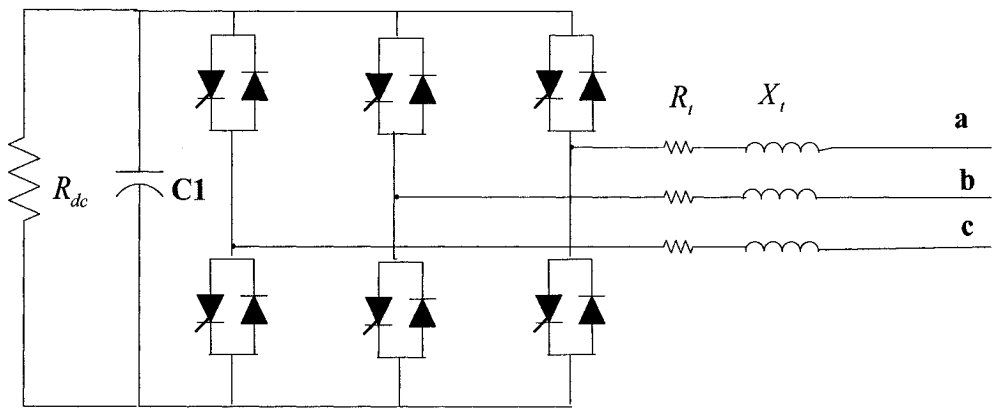

Figure 2-1: Diagram of a 3-phase VSC

It is assumed that the 3-phase output voltages of the VSC are balanced for a 3-wire system, and free of harmonics. The AC side and DC side equivalent circuit are shown in Figure 2-2.

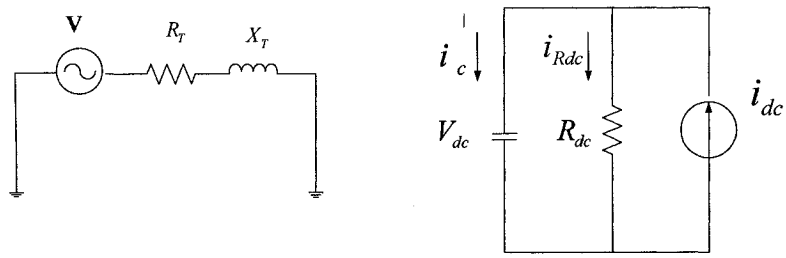

Figure 2-2 (a) AC side equivalent of VSC (b) DC side equivalent of VSC

The mathematical model of the VSC in terms of instantaneous variables in the AC side can be written as:

$$\begin{cases} L\dfrac{di_a}{dt} = U_a - V_a - R_a i_a \\ L\dfrac{di_b}{dt} = U_b - V_b - R_b i_b \\ L\dfrac{di_c}{dt} = U_c - V_c - R_c i_c \end{cases} \tag{2-1}$$

where U_a is the transmission line voltage and V_a is the VSC output voltage. The DC side of the VSC from Figure 2-2 (b) is defined by:

$$C\frac{dV_{dc}}{dt} = i_{dc} - \frac{v_{dc}}{R_{dc}} \tag{2-2}$$

By transforming eq. (2-1) in the a-b-c reference frame into the d-q-0 synchronous rotating reference frame, as explained in Appendix A, the following equations are obtained:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} -\dfrac{R\omega}{L} & -\omega & 0 \\ \omega & -\dfrac{R\omega}{L} & 0 \\ 0 & 0 & -\dfrac{R\omega}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \frac{\omega}{L}\begin{bmatrix} (U_d - V_d) \\ (U_q - V_q) \\ (U_0 - V_0) \end{bmatrix} \tag{2-3}$$

where ω is the angular frequency.

Using the same method from a-b-c frame to d-q-0 frame, the power balance between AC and DC side of the converter (assuming no losses) gives the following equation:

$$v_{dc} i_{dc} = \frac{3}{2}\left(u_d i_d + u_q i_q + u_0 i_0\right) \tag{2-6}$$

where:

$$\begin{aligned} u_d &= m_a v_{dc} \cos(\Phi) \\ u_q &= m_a v_{dc} \sin(\Phi) \end{aligned} \tag{2-5}$$

and m_a is the modulation index of the VSC, and Φ is the phase angle between the injected voltage and the line current.

Therefore, from eqs. (2-2), (2-4), and (2-5), the DC side equation of VSC in d-q-0 frame will be:

$$\frac{dv_{dc}}{dt} = \frac{3}{2C}\left(m_a \cos(\Phi) i_d + m_a \sin(\Phi) i_q\right) - \frac{v_{dc}}{CR_{dc}} \tag{2-6}$$

By combining eqs. (2-3) and (2-6), the mathematical model of VSC is obtained:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \\ v_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R\omega}{L} & \omega & 0 & -\frac{m_a}{L}\cos(\Phi) \\ -\omega & -\frac{R\omega}{L} & 0 & -\frac{m_a}{L}\sin(\Phi) \\ 0 & 0 & -\frac{R\omega}{L} & 0 \\ \frac{3m_a}{2C}\cos(\Phi) & \frac{3m_a}{2C}\sin(\Phi) & 0 & -\frac{1}{CR_{dc}} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \\ v_{dc} \end{bmatrix} + \begin{bmatrix} \frac{\omega}{L} & 0 & 0 & 0 \\ 0 & \frac{\omega}{L} & 0 & 0 \\ 0 & 0 & \frac{\omega}{L} & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} U_d \\ U_q \\ U_0 \\ 0 \end{bmatrix} \tag{2-7}$$

Since it is assumed that the 3-phase voltages are always balanced, the zero sequence component is zero, and only d-q components exist. In reality, this is far from the truth. Consequently, the zero sequence will be considered for DC-link voltage balancing separately in Chapter 3. The d-q-0 transformation is briefly explained in Appendix A.

2.5 3-level Neutral Point Clamped (NPC) VSC

VSCs, through a proper switching algorithm, convert DC voltage into a set of 3-phase AC voltages or currents with controllable amplitude and phase angle at fixed frequency equal to transmission line frequency (50 or 60 Hz). The converter DC terminals are connected to DC capacitors or a DC voltage source, while the AC side is connected to a power system through a coupling transformer. The DC capacitors must be large enough to maintain constant DC voltage during DC current changes. The coupling transformer connects the VSC to the power system. The transformer inductance protects the DC capacitor against short-circuits and sudden discharge.

Regulating the DC-link voltage or varying AC to DC gain of the converter can be used to control the AC voltage magnitude. In the first method, known as indirect control [1], the DC voltage is regulated in order to provide the desired amplitude in the AC side and the converter's AC to DC gain is kept constant. The disadvantage of this method is that the AC voltage range is limited due to the size of the DC side capacitor. In the second method of controlling the converter's AC to DC gain, the AC side voltage amplitude is regulated while the DC voltage is fixed (Direct control method). Both control methods are presented in this thesis for AC voltage regulation. The VSC has the capability to operate either as an inverter or a rectifier, and exchange active power with the power system; this is achieved by regulating the phase angle of the AC side voltage.

Several configurations for DC/AC converters exist, such as multi-pulse converters, and PWM converters [43]. PWM techniques offer lower harmonic components, with excellent dynamic response. Two-level PWM topology is the simplest and most commonly used, but it has the drawback of generating high switching-frequency

harmonics, and high dv/dt due to synchronous commutation of series devices. Multi-level PWM VSCs have the advantage of lower voltage stresses and generating lower harmonic components; also, they operate at a lower switching frequency [26].

An m-level converter (where $m \geq 3$), typically consists of m-1 capacitors in the DC-link and generates m-levels of voltages. Here, for simplicity, a 3-level PWM VSC is studied in detail and used for simulation. Figure 2-3 shows the schematic diagram of a 3-phase Neutral Point diode Clamped (NPC), 3-level VSC; the circuit consists of twelve valves and two DC capacitors. Each valve consists of a solid-state switch with turn-off capability and an anti-parallel diode. The anti-parallel switches ensure the bidirectional current flow, so that the converter is capable of operating in both rectifier and inverter modes.

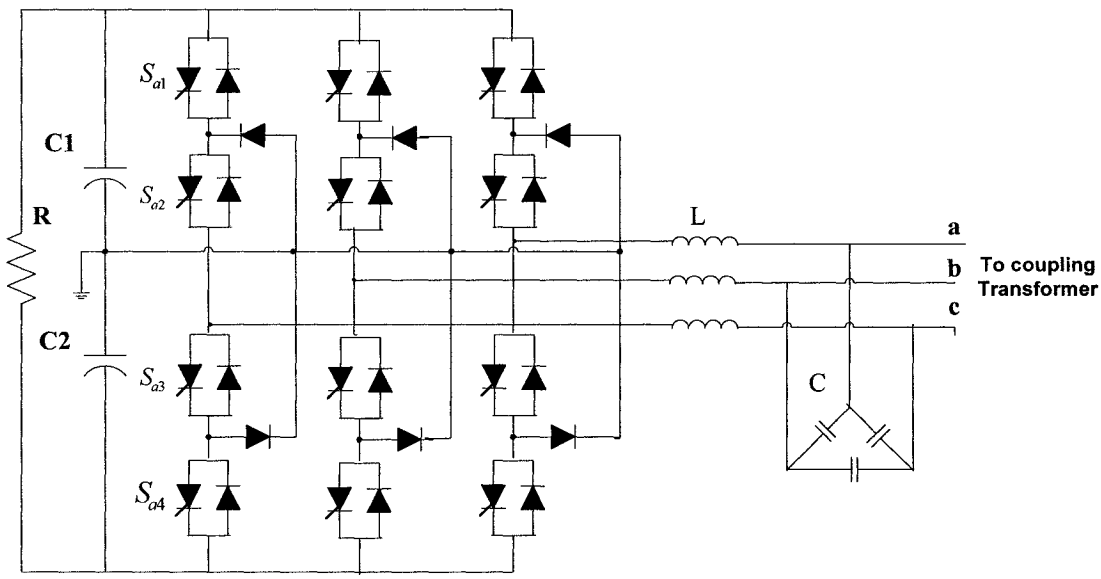

Figure 2-3: Schematic of a 3-level Neutral Point Clamped VSC

2.5.1 Sinusoidal Pulse Width Modulation (SPWM) technique

In SPWM technique, a reference sinusoidal waveform is compared with a triangular carrier wave. The frequency of the triangle carrier is selected to be much higher than the reference waveform. These two signals are compared, and when the sinusoidal wave is greater than the carrier, the SPWM trigger signal is high; otherwise it is at the low level. In a 3-phase converter, similar to the converter shown in Figure 2-1, a set of 3-phase balanced waveforms must be compared with a triangular carrier wave to generate appropriate firing pulses for the converter's switches. Consequently, the output voltage of the converter has the same frequency as the reference sinusoidal waveform, and the magnitude of the generated voltage is proportional to the modulation index that is defined by the ratio of the amplitude of the reference wave over the maximum value of the carrier. Figure 2-4 shows how the switching pulses are generated in a conventional 2-level SPWM converter.

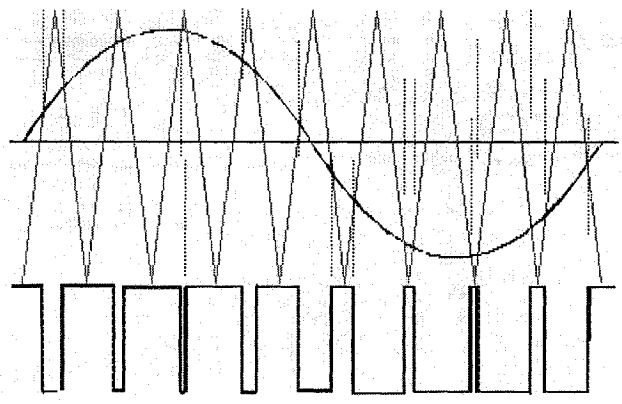

Figure 2-4: Modulation wave of 2-level PWM

In an m-level PWM converter, m-1 carrier waves are required to generate the switching pulses. Figure 2-5 shows the schematic for one phase of a 3-level PWM. The

3-level PWM uses two carrier waves, and the 3-level output waves are made with the following rules for the scheme shown in Figure 2-5:

- If Va> V_{tri-H}, S_{a1} is ON else S_{a1} is OFF.
- If Va> V_{tri-L}, S_{a2} is ON else S_{a2} is OFF.
- Only two series devices can be turned ON at the same time so:
    - S_{a1} and S_{a3} have opposite functions.
    - S_{a2} and S_{a4} have opposite functions.

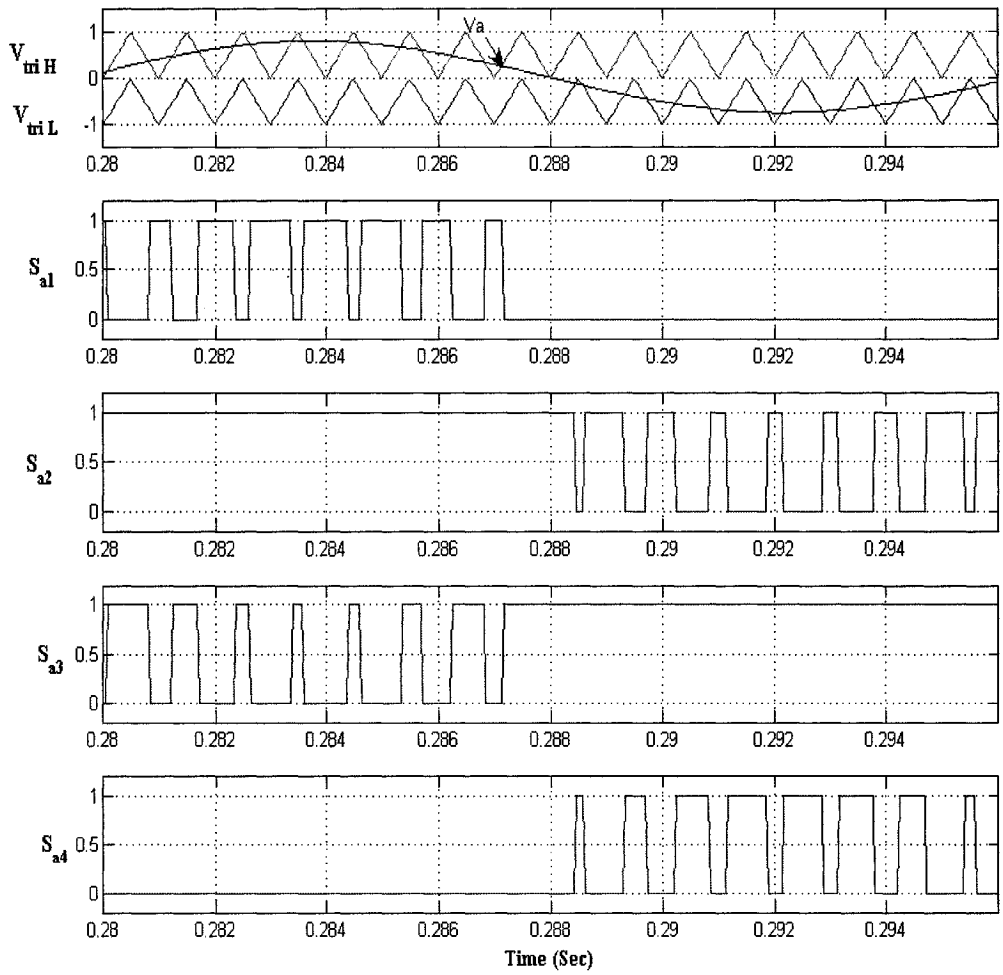

Figure 2-5 : Modulation wave and switching signals of a 3-level PWM

2.5.2 Operating principle of a 3-level NPC VSC

Figure 2-6 shows one pole of the 3-phase, 3-level NPC VSC, and the corresponding switching pattern is shown in Table 2-1. In a 3-level NPC VSC, the output voltage of the converter is made of 3-level voltages ($+V_{dc}/2$, 0, $-V_{dc}/2$).

There are three switch combinations to make a 3-level voltage in the output, namely:

- For $V_a = +V_{dc}/2$, upper switches S_{a1} and S_{a2} are ON.
- For $V_a = -V_{dc}/2$, two lower switches S_{a3} and S_{a4} are ON.
- For $V_a = 0$, S_{a2} and S_{a3} are ON.

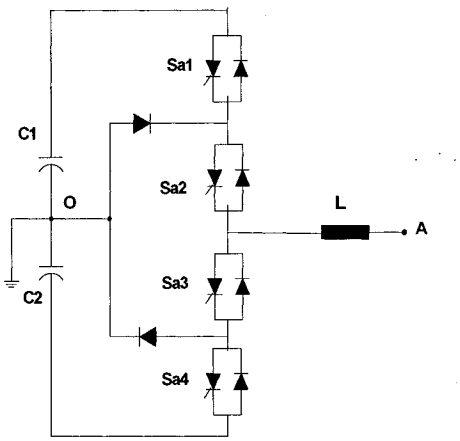

Figure 2-6: One pole of 3-level NPC VSC

Table 2-1: Switching pattern of one pole of a NPC VSC

Switching State	S_{1a}	S_{2a}	S_{3a}	S_{4a}	V_{an}
Positive	1	1	0	0	Vdc/2
Zero	0	1	1	0	0
Negative	0	0	1	1	Vdc/2-

In Table 2-1, the voltage levels and related switching states are shown. State "1" indicates that the switch is ON and state "0" indicates that the switch is OFF. Switches S_{a1}, S_{a3} and S_{a2}, S_{a4} are complimentary, i.e. if a switch is "ON" the other switch is "OFF" and vice versa. Figure 2-7 shows the output waveform of the 3-level VSC.

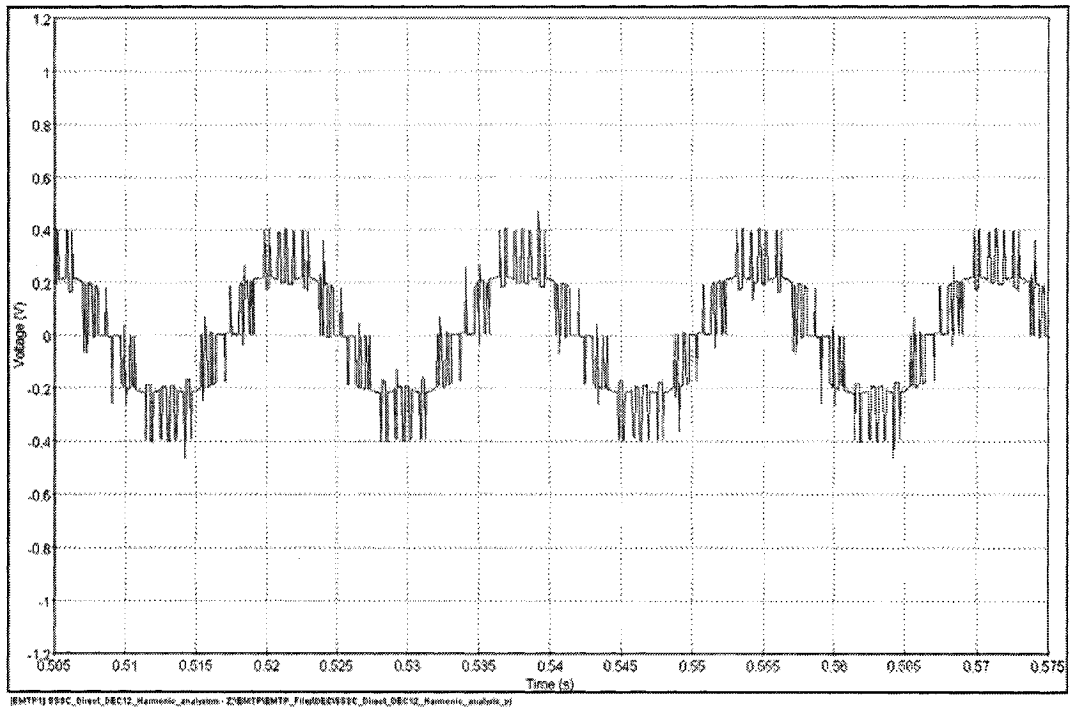

Figure 2-7: Output waveform of 3-level NPC VSC

2.6 Snubber circuit

Snubber circuits are used in a VSC to protect semiconductor switches from electrical stresses during the switching operations. In semiconductor switches, the over voltages during switch-off and turn-on currents during switch-on must be limited. Hence, these switches require turn-on and turn-off snubber circuits. Figure 2-8 shows the model of a switch with snubber circuits that are used in the converter model.

The equivalent switch identified as "GTO" and the anti-parallel diode D are represented as ideal switches in EMTP-RV. The small resistor r, in series with GTO and anti-parallel diode, represents the switch conduction losses and assists in avoiding any singularity on the inversion of the conductance matrix of circuit.

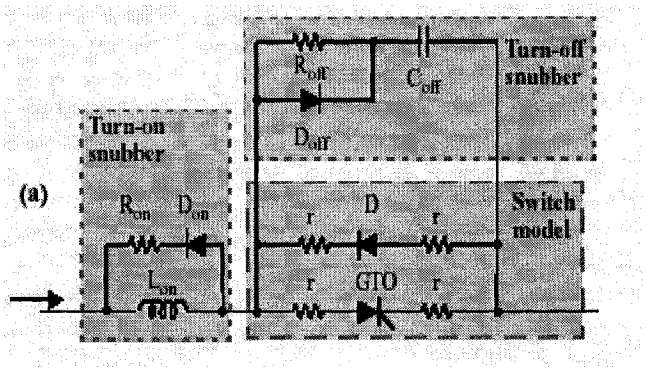

Figure 2-8: Model of the switch with snubber circuits

The polarized parallel R-L turn-on snubber circuit limits the rise rate of current, and the polarized R-C circuit limits the over-voltage during switch turn-off. An approximate value of the snubber circuit can be obtained from the following equations [30]:

$$\begin{cases} R_{on} = \dfrac{\Delta V_{CE}}{I_o} \\ \Delta V_{CE} = 10\% U_d \\ L_{on} = \dfrac{\Delta V_{CE} * t_{ri}}{I_o} \\ C_{off} = \dfrac{I_O * t_{fi}}{2 * U_d} \\ R_{off} = \dfrac{5 * U_d}{I_O} \end{cases} \tag{2-8}$$

where

t_{ri}: is the current rise time of the switch when the anode voltage falls from 90% to 10%

t_{fi} :is the current fall time of the switch when the anode current falls from 90% to 10%.

ΔV_{CE} : is the voltage drop across the switch during turn-on.

R_{off}: is the resistor in the turn-off snubber.

L_{on}: represents the inductor in the turn-on snubber.

2.7 Passive component design

2.7.1 DC-link capacitor

- **Balancing the DC-link voltages**

In a 3-level converter topology, the unequal voltage charging of the DC-link capacitors due to the circuit behavior may eventually damage the semiconductor switches. Since the charging and discharging time of the capacitors are not the same, an accumulating unbalance voltage may cause a high voltage on the semiconductor switches and surpass the switch rating [31] and may destroy the switches. Several methods, such as using separate DC voltage sources [32], or modified PWM patterns and voltage vector selections [33] can be used as solutions. To balance the voltages, a simple algorithm from [31] is applied that is based on zero sequence current. The unbalanced voltage is sensed and amplified by a PI controller, and compared to the zero sequence component of the converter output current to feed forward to the PWM. The same method is used here for DC-link voltage balancing and it will be discussed in more detail in Section 3.4.1

- **Design of DC capacitor**

The DC capacitor of VSCs has a major impact on the system operation. By using a large capacitor, the DC voltage ripple will be reduced, but the system will have a slower response to DC voltage regulation. Also the capacitor cost will be higher. Therefore, a capacitor with minimum capacity that satisfies the DC waveform quality is desired [41]. In this section, the optimum capacitor size with the respect to the DC voltage ripple is investigated.

If the parallel resistor with the DC-link capacitors (representing the converter losses) and the stored line inductor energy is neglected, by applying KCL:

$$C_{dc}\frac{dV_{dc}}{dt}+\frac{V_{dc}}{R_{dc}}=S^{T}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2-9}$$

where S is the switching function and can be defined by:

$$S=\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}=m_a\begin{bmatrix} \sin(\omega t) \\ \sin(\omega t+120^{\circ}) \\ \sin(\omega t+240^{\circ}) \end{bmatrix} \tag{2.10}$$

It is assumed that the harmonic components caused by the switching action are neglected. For simplicity, one pole of the 3-level converter is considered to determine the minimum capacitor size.

$$\begin{aligned} S^{T}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} &= m_a\begin{bmatrix} \sin(\omega t) \\ \sin(\omega t+120^{\circ}) \\ \sin(\omega t+240^{\circ}) \end{bmatrix}\begin{bmatrix} I_m\cos(\omega t+\phi) \\ I_m\cos(\omega t+\phi+120^{\circ}) \\ I_m\cos(\omega t+\phi+240^{\circ}) \end{bmatrix} \\ &= \frac{m_a I_m}{2}\begin{bmatrix} \sin 2(\omega t+\phi) \\ \sin 2(\omega t+\phi+120^{\circ}) \\ \sin 2(\omega t+\phi+240^{\circ}) \end{bmatrix} \end{aligned} \tag{2-11}$$

At any instant ($S_a i_a+S_b i_b+S_c i_c$) is equal to one of the AC phase current with value of $\frac{I_m m_a}{2}$. In steady-state, the DC voltage has a small ripple that is defined as the difference between the maximum and minimum value of DC voltage $\Delta V_{dc}=V_{dc\max}-V_{dc\min}$, with average value of $V_{dc,ave}$. By considering a short period of time that DC-link voltage is

charged from $V_{dc\min}$ to $V_{dc\max}$, the variation of DC voltage can be shown with $\frac{\Delta V_{dc}}{\Delta t}$.

Therefore, eq. (2-9) becomes:

$$C_{dc}\frac{\Delta V_{dc}}{\Delta t}+\frac{V_{dc}}{R_{dc}}=\frac{I_m m_a}{2} \tag{2-12}$$

Hence, the minimum value of the DC-link capacitor can be defined by the following equation:

$$C_{dc}=\frac{\left(\frac{I_m m_a}{2}-\frac{V_{dc,ave}}{R_{dc}}\right)*\Delta t}{\Delta V_{dc}}=\frac{\frac{I_m m_a}{2}-\frac{V_{dc,ave}}{R_{dc}}}{\Delta V_{dc}*f_s} \tag{2-13}$$

where f_s is the converter's switching frequency, and ΔV_{dc} is the acceptable ripple in the DC-link.

2.7.2 AC side filter design

It is important to keep the harmonics on the AC side of the converter at an acceptable level. In a practical scheme, either 4 or 8 multiple converters with a transformer arrangement are used to reduce the generated harmonics, and produce a very high quality sinusoidal output waveform with 24 or 48 steps. Therefore, in these cases, no output filter will be required [34]. A high power PWM converter generates high order harmonics on the AC side of the converters because of finite and limited switching frequency. Figure 2-9 shows the harmonic spectrum of the designed 3-level NPC VSC. A low-pass filter is, therefore, applied to keep the harmonics at an acceptable level.

- ***Total Harmonic Distortion (THD)***

The AC voltage generated by PWM is given by:

$$V(t) = \sum_{i}^{\infty} V_i Sin(2\pi f_i t + \phi_i) \qquad (2\text{-}14)$$

If the ratio of the switching frequency over fundamental frequency is very high, the current harmonics are independent of the load, and only depend on the switching frequency f_s, DC-link voltage, the modulation index m_a, and number of levels. Figure 2-9 shows the harmonic spectrum of the designed 3-level NPC VSC with 900 Hz switching frequency.

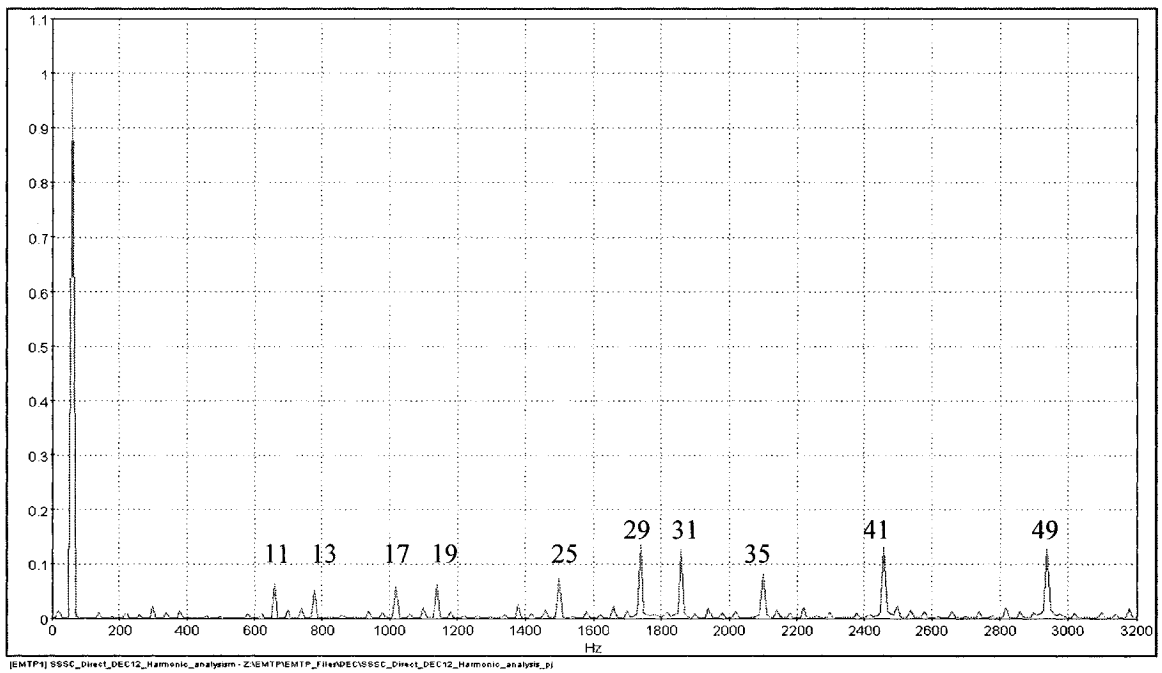

Figure 2-9: Harmonic spectrum of 3-level NPC VSC

The performance of the switching converter topologies can be evaluated by Total Harmonic Distortion (THD) of the voltage and current at the output of the converter. The THD factor indicates how closely the PWM generated voltage resembles the reference sinusoidal waveform with fundamental frequency. THD is defined as:

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} V_n^2}{V_1^2}} \tag{2-15}$$

Where V_n is the RMS value of the harmonic n, and V_1 is the RMS value of the fundamental voltage. Note that THD is independent of the frequency.

- ***Weighted Total Harmonic Distortion (WTHD)***

Weighted Total Harmonic Distortion (WTHD) is another indicator to evaluate the converter's performances. Like THD, WTHD is based on the sum of the squared harmonics over fundamental frequency component; in addition, the order of the harmonics is considered.

$$WTHD = \sqrt{\frac{\sum_{n=2}^{\infty} (V_n / i)^2}{V_1^2}} \tag{2-16}$$

In [37], an analytical approach is presented to determine THD and WTHD for multi-level PWM converters. The following equations are obtained for a 3-level PWM converter:

$$THD = \sqrt{\frac{1}{m}\left(\frac{4}{\pi} - m\right)} \tag{2-17}$$

$$WTHD = \sqrt{\left(\frac{2}{m^2}\left(\frac{f_1}{f_s}\right)\frac{\pi}{3}\left[\frac{m^2}{2} - \frac{8m^3}{3\pi} + \frac{3m^4}{8}\right]\right)} \tag{2-18}$$

Where m is the modulation index of the PWM converter.

- ***Low Pass Filter design***

PWM harmonics are defined in [37] for 3-level PWM converters. The harmonics are:

$nm_f \pm k$

$$where \begin{cases} n = 1,3,\ldots & \text{and } k = 0,2,4,\ldots \\ n = 0,2,4,\ldots & \text{and } k = 1,3,\ldots \end{cases}$$

For 900 Hz switching frequency, m_f=15 and consequently the first set of harmonics are: 15, 15±2, 15±4 …

In [35], the low-pass filter design for a 3-level PWM converter is defined. The filter performance is determined by its resonant frequency. The best filter performance is reached when the resonant frequency of the filter is well below the lower harmonic frequency caused by the PWM, and much higher than the fundamental frequency. Since, in high power PWM converters, switching frequency is limited around 1kHz, so the filter resonant frequency must be chosen between 60 Hz and 1 KHz. The resonant frequency of the filter is defined based on the pulse frequency of the converter. The following equation is used in [35] to select an appropriate low-pass filter for a 3-level high power PWM converter:

$$f_r = 0.8 * \left(\frac{f_p}{2} \right) \tag{2-19}$$

where f_r is the resonant frequency, and f_p is the pulse frequency.

The pulse frequency in a 3-level PWM is twice the switching frequency. Therefore, for a 900Hz 3-level PWM converter, the resonant frequency will be $f_r = 720$. From knowledge of the resonant frequency, the L and C values of the low-pass filter can be determined by:

$$\omega_r = \frac{1}{\sqrt{L_f C_f}} \tag{2-20}$$

There are several choices for selecting L_f and C_f, but it should be noted that the capacitor is usually the cheaper device. Sufficiently high value for the inductor must be selected in the order to limit the current that the converter carries to charge the filter capacitors. Figure 2-10 shows the harmonic spectrum of the VSC output voltage after filtering.

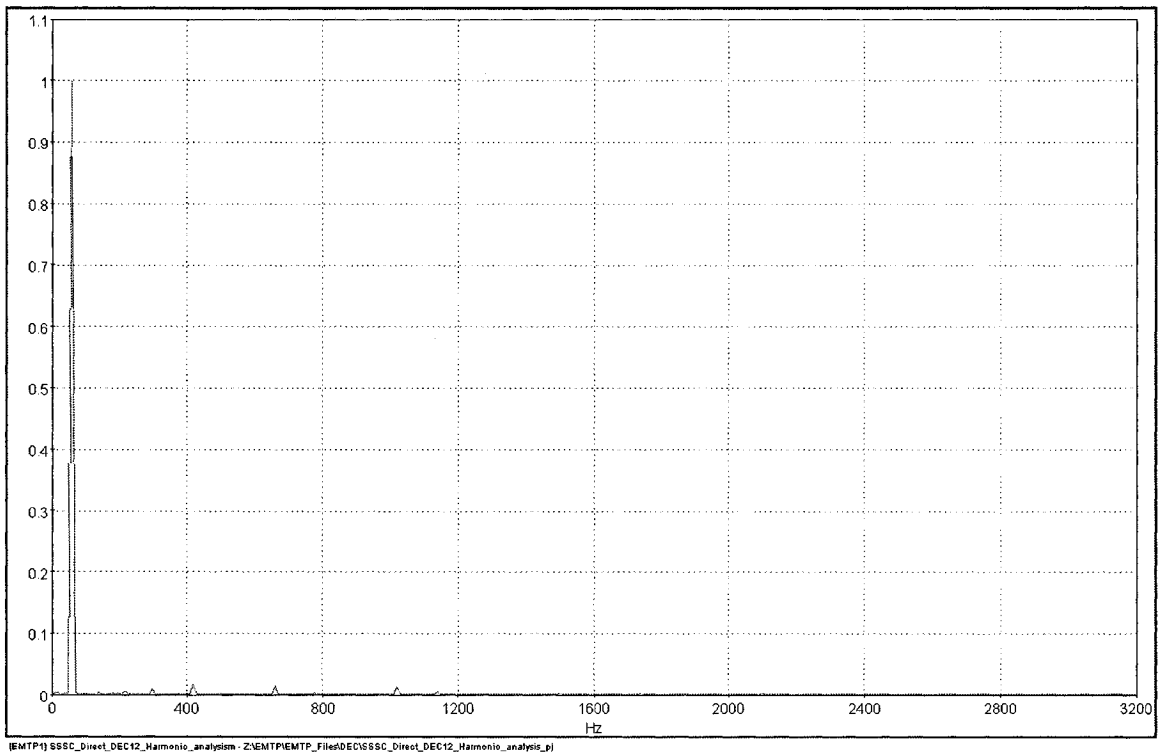

Figure 2-10: Harmonic spectrum of 3-level NPC VSC output voltage after filtering

2.8 Reference Wave Generator

The transmission line voltages and currents can be severely distorted by harmonics, and unbalance in the system. Therefore, one of the major concerns in controller design is providing an appropriate reference signal from the transmission system to synchronize the controller. A Reference Wave Generator (RWG) is used to extract the fundamental

waveforms from the distorted line voltages or currents, and generates the reference waveform. The designed RWG is based on [36]. This method when compared to the conventional phase-looked-loop (PLL) [42] has very fast response to any distortion and is almost without any transient delay.

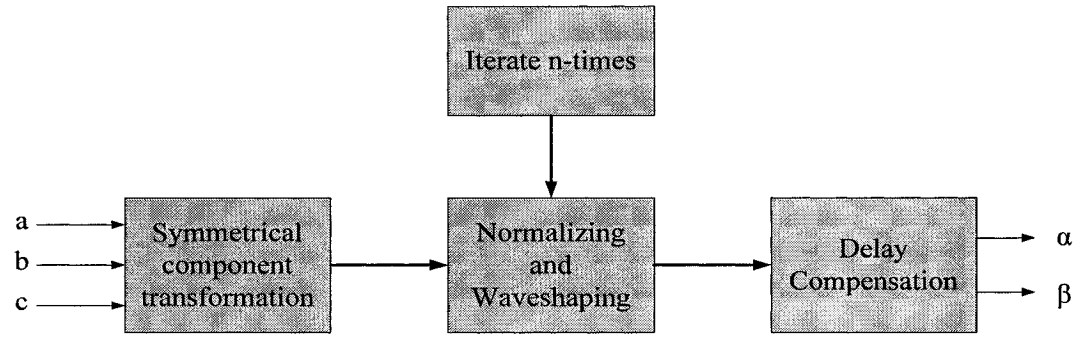

Figure 2-11: Block diagram of Reference Wave Generator (RWG) [36]

The 3-phase transmission line currents (i_a, i_b, and i_c) are used as the reference signals by the controller to generate either leading or lagging voltages by 90 degrees. Figure 2-11 shows the block diagram of the RWG. The 3-phase transmission line currents are transformed into positive, negative and zero sequence components (a-b-c coordinates to α-β-0 coordinates), as indicated in the following equation:

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (2\text{-}21)$$

While the 3-phase currents are sinusoidal and balanced, i_α and i_β become sinusoidal and orthogonal, and the zero sequence become equal to zero. In case of any distortions or

harmonics, i_α and i_β sinusoidal waveforms and 90 degrees phase angle will be changed. In order to keep i_α and i_β waveforms sinusoidal and perpendicular, a normalizing block and band-pass filter is applied.

The normalizing and wave-shaping block must be iterated several times to obtain a set of two sinusoidal waveforms with a 90 degrees phase shift. Hence, a time delay occurs that depends on the number of iterations and time step of the simulation. The time delay can be calculated as:

$$\phi_{Delay} = nt_s(2\pi f) \tag{2-22}$$

where n is the number of iteration and t_s is the time step, and f is the utility frequency. The time delay caused by iteration is compensated by using the following equation:

$$\begin{bmatrix} V_{\alpha ref} \\ V_{\beta ref} \end{bmatrix} = \begin{bmatrix} \cos\phi_{Delay} & -\sin\phi_{Delay} \\ \sin\phi_{Delay} & \cos\phi_{Delay} \end{bmatrix} \begin{bmatrix} V'_{\alpha} \\ V'_{\beta} \end{bmatrix} \tag{2-23}$$

The generated reference waveform has a unit value. Figure 2-12 shows a comparison between a conventional PLL and RWG. The graph demonstrates the angle between the input and output of the PLL and RWG. RWG has almost no oscillations with a very fast settling time.

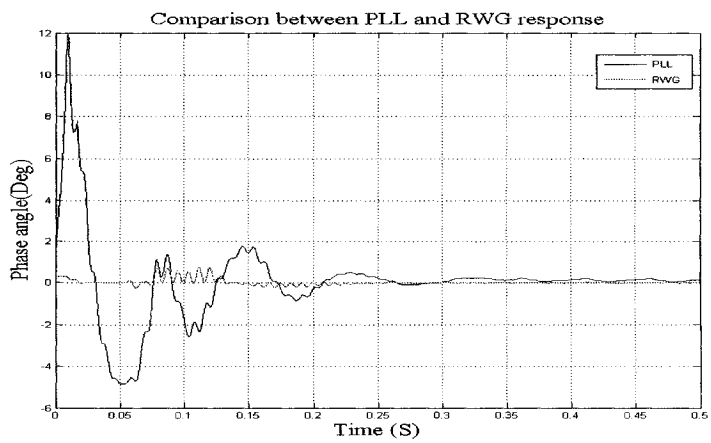

Figure 2-12: Comparison of a conventional PLL and RWG

2.9 VSC topologies

VSCs can be connected in series, parallel or a combination of them into the transmission lines. They can be used for power flow control in a single as well as multiple transmission lines. STATCOM and SSSC are the most commonly used topologies in converter-based FACTS controllers; other less popular topologies include UPFC, IPFC and GUPFC.

2.9.1 STATCOM

A Static Synchronous Compensator (STATCOM) is a shunt connected power converter that exchanges reactive power with the transmission line. The capability of the STATCOM is analogous to a rotating synchronous compensator, and can be used for dynamic compensation of power systems, increasing transient stability and providing voltage support. The IEEE definition of the STATCOM is[10]:

Static Synchronous Compensator (SSC or STATCOM): *" A static synchronous generator operated as a shunt-connected static var compensator whose capacitive or inductive output current can be controlled independent of the AC system voltage."*

The schematic diagram of a STATCOM is shown in Figure 2-13. The DC voltage V_{dc} is converted to a set of 3-phase AC voltages with controllable amplitude and phase angle. By regulating the output voltage amplitude into the transmission line the reactive power exchange can be controlled. The phase angle between injected voltage V_{inj} and bus voltage V_T is controlled in order to regulate the active power exchange with the transmission line. If the converter's losses are neglected, the injected voltage and bus

voltage are in phase, and the STATCOM output current is in quadrature with the bus voltage. Hence, the STATCOM output current can be found by the following equation:

$$|I_{inj}| = \frac{V_{inj} - V_T}{X_{Statcom}} \tag{2-24}$$

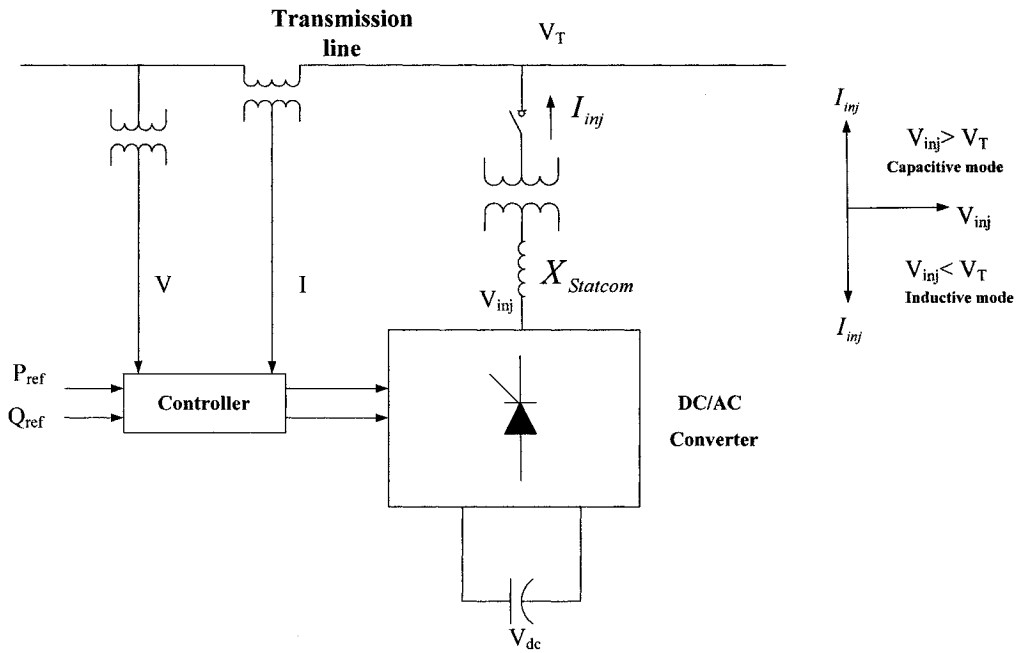

Figure 2-13: Diagram of STATCOM

If the magnitude of $V_{inj} > V_T$, the STATCOM operates in capacitive mode and supplies reactive power to the transmission line, and if $V_{inj} < V_T$, the STATCOM operates in inductive mode and absorbs reactive power from the transmission line.

2.9.2 SSSC

A Static Synchronous Series Compensator (SSSC) is a power converter connected in series with the transmission line and it injects a voltage in quadrature with the line current to emulate a series capacitive or inductive reactance into the transmission line. A SSSC

equipped with energy storage system and/or absorbing devices is also able to exchange real power with the power system.

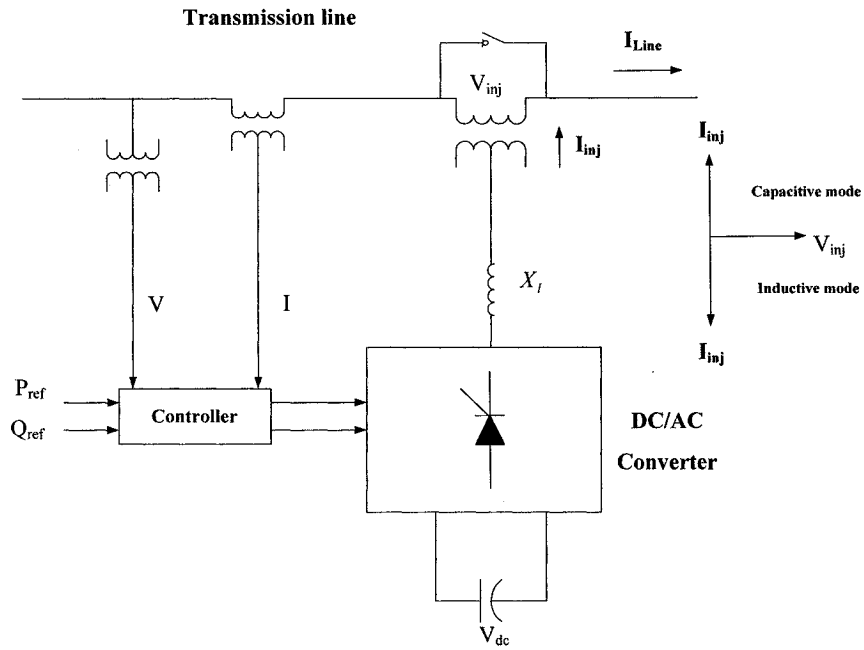

Figure 2-14: Diagram of SSSC

The diagram of SSSC is shown in Figure 2-14. Similar to a STATCOM, reactive power exchange is controlled by the magnitude of the injected voltage to the transmission line, and angle control is used to regulate the active power exchange. The inductive or capacitive mode of operation is set by the injected voltage phase angle with respect to the transmission line current. When injected voltage is leading the line current, reactive power is absorbed and SSSC operates in inductive mode. In capacitive mode, injected voltage is lagging the line current and injects reactive power to the transmission line.

2.9.3 UPFC

A Unified Power Flow Controller (UPFC) consists of a SSSC and a STATCOM connected together in a back-to-back arrangement through their DC-link. Figure 2-15

shows the block diagram of an UPFC. The UPFC is capable of exchanging reactive power with the power system through both series and shunt connections. In addition it is able to exchange active power through the DC-link.

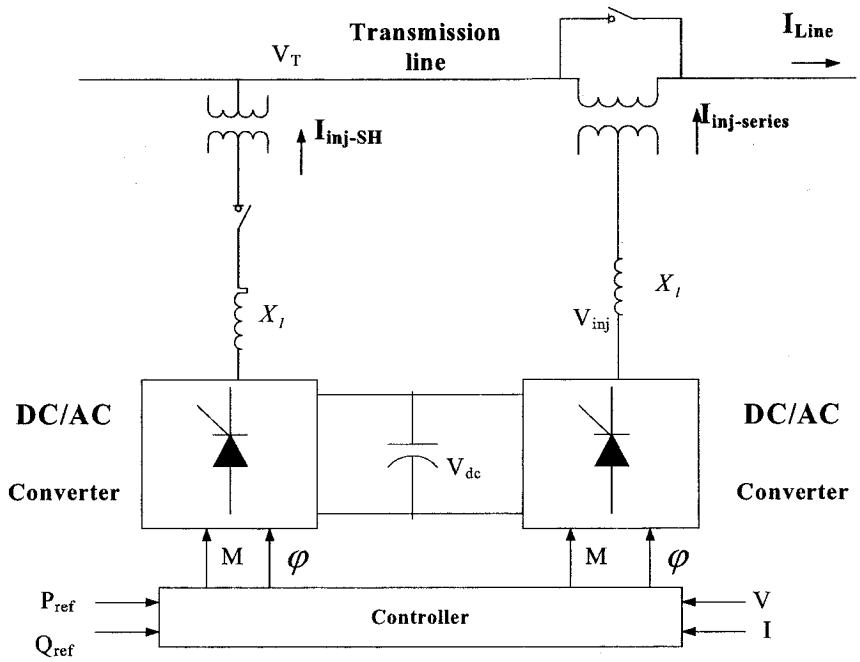

Figure 2-15: Schematic of UPFC

The shunt connection is used to maintain a constant voltage on the DC- link while regulating the active power in the series connection. However, the shunt connection is only used to exchange reactive power with the transmission line.

2.9.4 IPFC

An Interline Power Flow Controller (IPFC) consists of two or more SSSCs that share a common DC-link, and are used to control power flows of multi-lines or a sub-network. Each SSSC has the capability of exchanging reactive power with the transmission lines. Furthermore, active power can also be transferred through the DC-link between SSSCs.

However, the active power that is injected by one SSSC to the transmission line must be equal to the active power taken away from the other transmission lines (neglecting the losses).

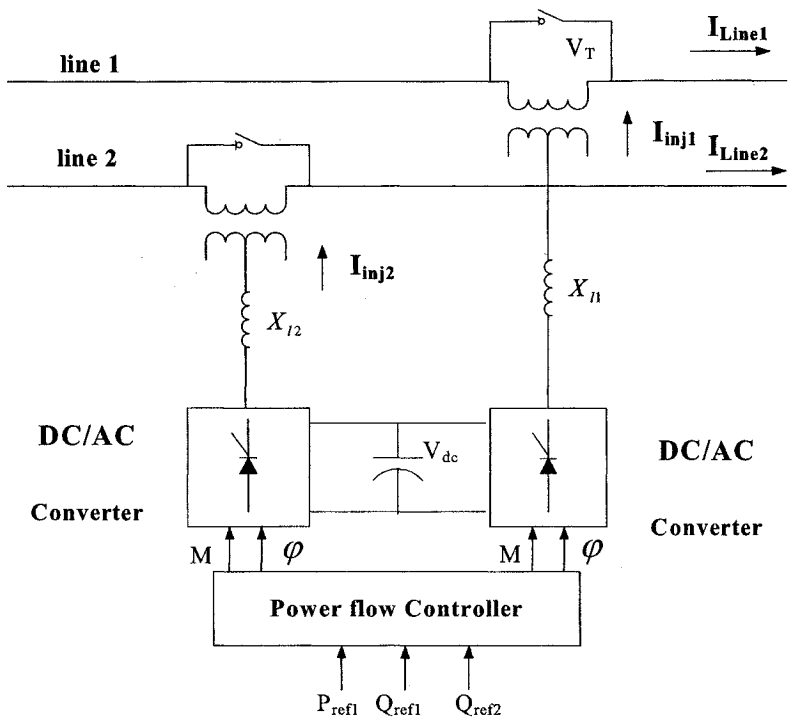

Figure 2-16: Schematic of IPFC

An IPFC with a multi-converter configuration is shown in Figure 2-16. IPFC can be used to equalize active and reactive power between transmission lines, and transfer power from overloaded lines to lines that are under-loaded. One series branch has one degree of freedom but the remaining branches have two degrees of freedom and provide both active and reactive compensation.

2.9.5 GUPFC

A Generalized Unified Power Flow Controller (GUPFC) is composed of a shunt power converter and several series converters with a common DC-link. Similar to IPFC, a GUPFC can be used to control power flow of several transmission lines.

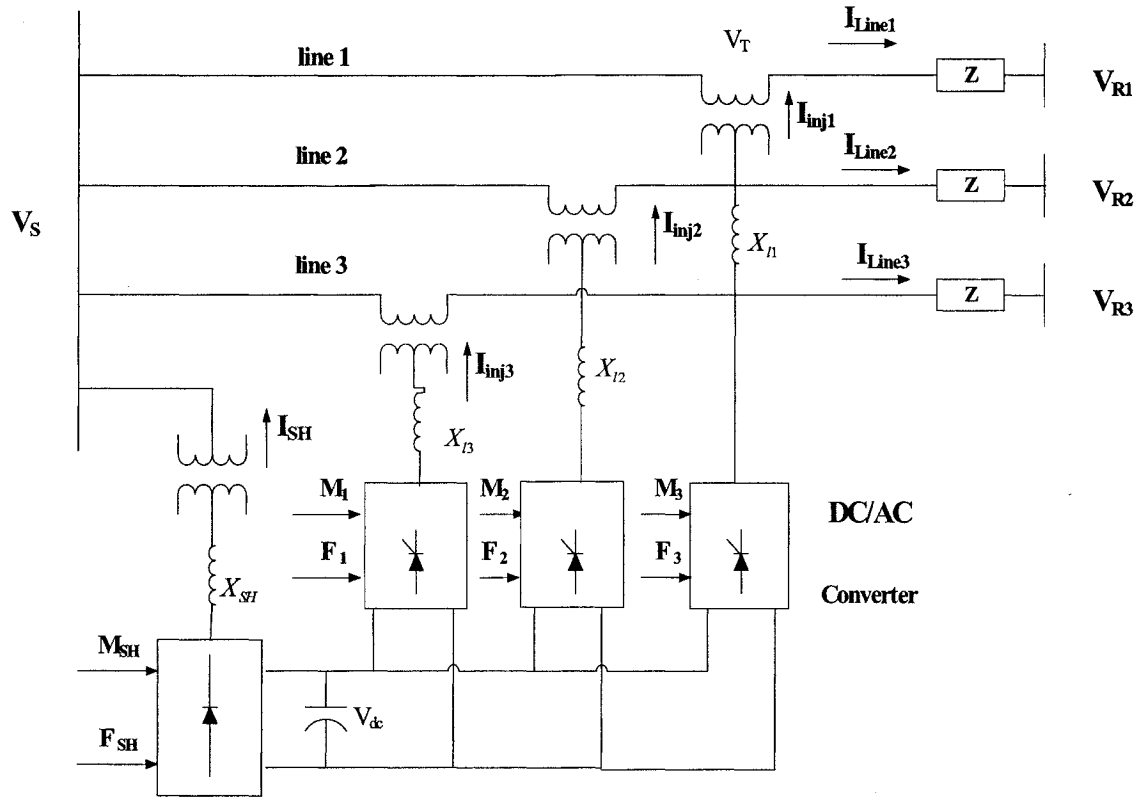

Figure 2-17: Schematic of GUPFC

The series converters control active and reactive power flow in the transmission lines, and the shunt converter (with one degree of freedom) supports the real power requirement of the series converters via the common DC-link. A GUPFC is shown in Figure 2-17.

2.10 Summary

This chapter has discussed the fundamental of 3-phase VSC that is used as the basic building block for SSSC and IPFC in the next chapters. The mathematical model of VSC is presented; and the operation principle of a 3-level NPC VSC is explained.

The design of snubber circuits and passive component in the VSC is discussed. The guidelines for designing DC capacitors and the AC side filter for the VSC are presented.

A fast synchronizing method for generating reference waveforms are explained. All possible topologies for converter based FACTS applications are presented.

Chapter 3

Modeling and Controller Design of Static Synchronous Series Compensator (SSSC)

3.1 Introduction

This chapter presents the operation and control strategies of the SSSC. For this purpose, a dynamic model is developed by linearizing equations at fundamental frequency. Both direct and indirect controllers of SSSC are proposed. The accuracy of the mathematical model is verified by the results obtained from time-domain simulations with EMTP-RV.

3.2 Power circuit of the SSSC

A Static Synchronous Series Compensator (SSSC) consists of a VSC connected in series with the transmission line through a coupling transformer. The VSC generates a set of 3-phase voltages with controllable magnitude and phase angle at the desired frequency; thus, a SSSC is analogous to a synchronous sinusoidal voltage source. A detailed 3-phase diagram of the SSSC is given in Figure 3-1. Where V_s and V_r are voltages at the sending-end and receiving-end of the transmission line, and R_{line} and X_{line} are transmission line resistance and reactance respectively. The phase angle between V_s and V_r is δ. The coupling transformer primary windings are star-connected and the secondary windings are connected in series with each phase of the transmission line. The

turn's ratio of the coupling transformer is 1:1. R_t and X_t are the internal resistance and leakage inductance of the coupling transformer. V_{inj-a}, V_{inj-b}, and V_{inj-c} are output voltages of VSC that are injected in series into the transmission line. The transmission line currents are i_a, i_b, i_c. The voltage across the DC-link of VSC is V_{dc}.

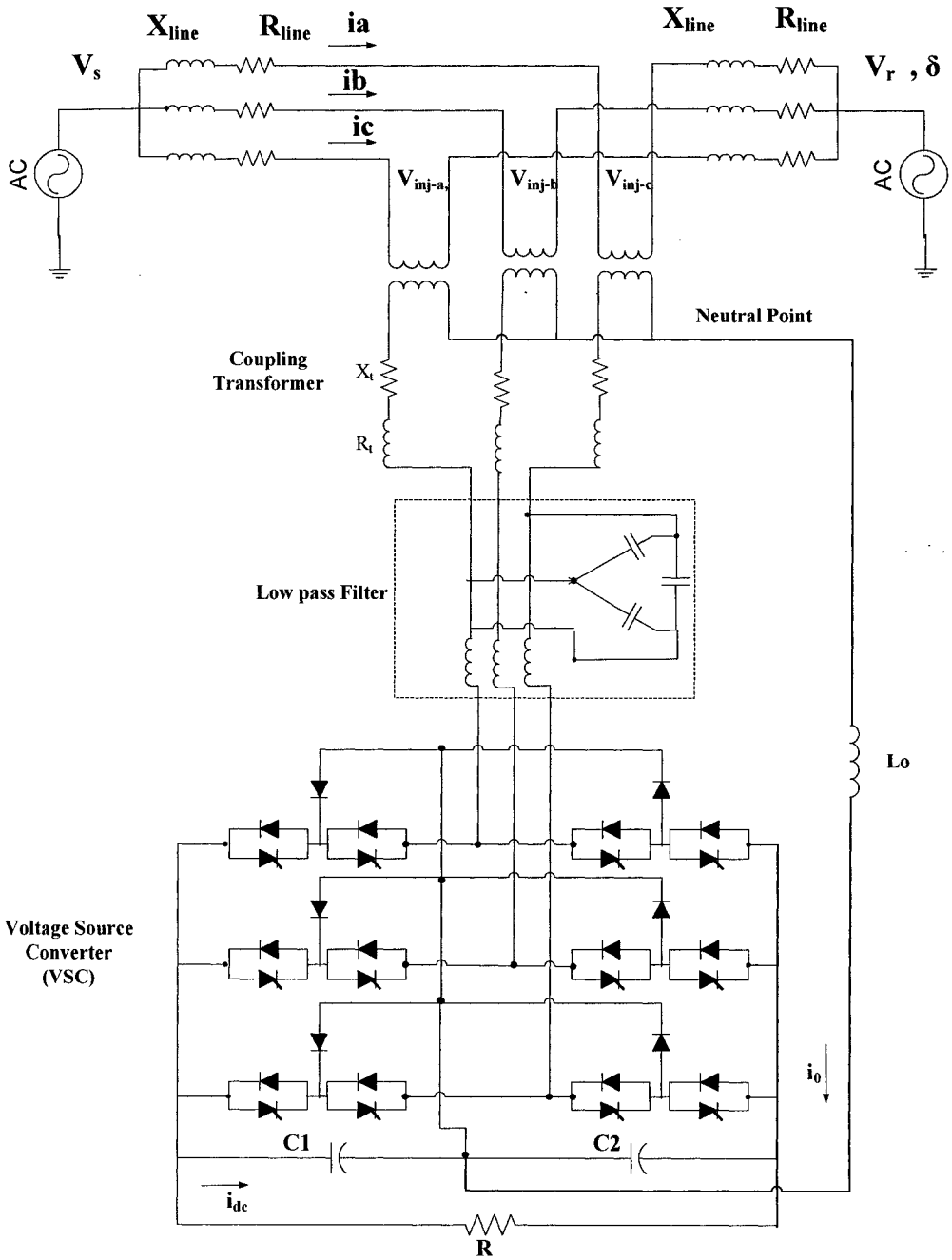

Figure 3-1: SSSC power circuit

3.3 Operating principle of the SSSC

Basically, a SSSC generates on its output terminals a sinusoidal voltage, with controllable amplitude, in quadrature (nearly) with the transmission line current. Consequently, the injected voltage emulates either a capacitive or an inductive reactance in series with the transmission line that increases or decreases the total transmission line reactance. As a result, the power flow will change in the line. Hence, the SSSC is a powerful device to control transmission line impedance, and therefore the power flow, independent of the line current.

In fact, reactive power exchange is controlled by the magnitude of the injected voltage to the transmission line, and angle control is used to regulate the active power exchange. The inductive or capacitive mode of operation is set by the injected voltage phase angle with respect to the transmission line current. When the injected voltage is leading the line current, reactive power is absorbed and the SSSC operates in inductive mode; in capacitive mode, injected voltage is lagging the line current and injects reactive power into the transmission line.

Only a SSSC equipped with an Energy Storage System (ESS) is able to exchange active power with the transmission line. Figure 3-2 shows the phasor diagram of a SSSC equipped with an ESS. The line current phasor is used as the reference phasor. Theoretically, the SSSC voltage phasor can operate in all four quadrants of the circle, by setting the phase angle of the SSSC output voltage V_{inj} with respect to the transmission line current. There are, however, some practical limitations in power systems, i.e. voltage range in the receiving-end which must be kept between 0.95 p.u. to 1.05 p.u., and the magnitude of injected voltage of SSSC in capacitive mode must be less than the voltage

drop across the transmission line $V_{inj} < V_{line}$. Otherwise the power flow in the line will be reversed and that is not desired.

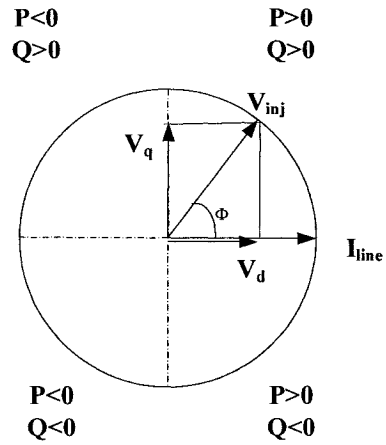

Figure 3-2: Phasor diagram of SSSC

The active (P) and reactive (Q) power exchange between SSSC and the transmission line are:

$$P = V_{inj} * I_{line} \cos\Phi$$
$$Q = V_{inj} * I_{line} \sin\Phi \qquad (3\text{-}1)$$

3.4 SSSC control strategies

In this thesis, the SSSC is designed in order to control the impedance characteristic of the transmission line. The main function of the controller is to generate appropriate firing pulses for the VSC's switches in order to produce the required output voltages. This is achieved by computing the required magnitude and phase angle of the output voltage from the reference signals. The output voltages of VSC in synchronous frame are:

$$V_d = kV_{dc}\cos(\Phi)$$
$$V_q = kV_{dc}\sin(\Phi) \tag{3-2}$$

where k is the gain of the converter that relates the DC-side voltage to the peak value of output phase voltage at the converter AC-side and Φ is the phase angle between injected voltage and transmission line current.

Two control methods, known as direct and indirect control methods [1] can be applied to regulate the output voltage of the VSC. In indirect control method, k is kept constant and the only available control input is the angle Φ of the VSC. In direct control method, both k and Φ are varied for control purposes and the DC-link voltage of VSC is kept constant and sufficiently high. Both direct and indirect methods are used for SSSC controller design in this thesis and the results are compared together.

As mentioned in Section 2.7.1, balancing the voltages between two DC-link capacitors is an important concern in the 3-level converter. Uneven voltage charging on upper and lower DC-link capacitors may apply destructively high over-voltages on switching devices and DC-link capacitors. In order to maintain equal voltages in the DC-link capacitors, the neutral point must be kept balanced. Here zero sequence current is used to equalize voltages in upper and lower capacitors in the DC-link. Since the output voltage of the VSC is regulated based on the total DC-link voltage, balancing the voltage of DC-link's capacitors has negligible effect on the injected voltage of the SSSC in both direct and indirect control methods. Since the DC-link voltage balancing controller algorithm is common in both direct and indirect control methods, it will be presented first.

3.4.1 DC-link Balancing Controller

The zero sequence current can be used to balance the voltages of the DC-link capacitors in a 3-level Neutral-Point-Clamped (NPC) VSC [31]. This is achieved by connecting the neutral points of the coupling transformer and the DC-link of the VSC through inductor L_0, as shown in Figure 3-1. The power balance eq. (2-4) of a 3-level VSC, with two capacitors in the DC-link is defined by the following equation:

$$v_{dc} i_{dc} = \frac{3}{2}\left(u_d i_d + u_q i_q\right) = V_{dc2} i_{dc} + V_{dc1}(i_{dc} + i_0) \tag{3-3}$$

where V_{dc2} and V_{dc1} are DC-link voltages of C1 and C2 capacitors respectively and i_0 is the zero sequence current and i_{dc} is the DC-link current of the VSC.

The neutral points of the coupling transformer and DC-link are connected with a large inductor to reduce the switching ripple in the zero sequence current. A PI controller and a proportional controller are employed for Balancing Controller such that:

$$i_{0-ref} = (V_{dc2} - V_{dc1})(K_{p-vb} + \frac{K_{i-vb}}{S}) \tag{3-4}$$

$$i_0^{'} = (i_{0-ref} - i_0)(K^{'}_{p-vb}) \tag{3-5}$$

If the DC-link capacitors are unbalanced, a zero sequence current is generated and amplified by the PI controller as shown in eq. (3-4). The generated zero sequence current $i_{0\text{-ref}}$ is compared to the actual zero sequence current of the converter's output i_0 (neutral points of the coupling transformer), and amplified by a proportional controller as shown in eq. (3-5). The zero sequence current $i_0^{'}$ is regulated by the PWM controller that controls the output zero sequence voltage of the VSC. Depending on the direction of the

zero sequence current, the upper or lower DC-link capacitor is charged and since the whole DC-link voltage is kept constant, by charging a capacitor the other capacitor is discharged, and the DC-link capacitor voltages will be even. Figure 3-3 and 3-4 show the block diagrams of the voltage balancing controllers in the SSSC with the indirect and direct controllers respectively.

3.4.2 Indirect controller

This method is described in [1] and also used in [24], [25]. As mentioned earlier, in indirectly controlled converters, only the phase angle of the output voltage is controllable and the magnitude remains proportional to the DC-link voltage. However, the DC-link voltage can be varied by regulating the angular position of the output voltage. In this situation, real power is exchanged with the transmission line to charge or discharge the DC-link capacitors to the desired level. If the VSC losses are neglected in steady-state operation, the injected voltage is in quadrature with the transmission line current (capacitive or inductive mode). Therefore, a small phase displacement $\Delta\delta$ is required for real power exchange. A positive phase displacement ($90^\circ + \Delta\delta$) causes real power flow from SSSC to the transmission line, and as a result the DC-link capacitors will be discharged. A negative phase displacement ($90^\circ - \Delta\delta$) lets the SSSC absorb real power from the transmission line, and the DC-link capacitors will be charged.

A small-signal model of the indirectly controlled SSSC is proposed in [16]. Here the large signal model of eq. (2-7) is recalled to present the model of indirectly controlled SSSC.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R\omega}{L} & \omega & -\frac{m_a}{L}\cos(\Phi) \\ -\omega & -\frac{R\omega}{L} & -\frac{m_a}{L}\sin(\Phi) \\ \frac{3}{2C}m_a\cos(\Phi) & \frac{3}{2C}m_a\sin(\Phi) & -\frac{1}{CR_{dc}} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} + \begin{bmatrix} \frac{\omega}{L} & 0 & 0 \\ 0 & \frac{\omega}{L} & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} U_d \\ U_q \\ 0 \end{bmatrix} \quad (3\text{-}6)$$

By linearization of the above equation around an operating point, the following equation can be obtained:

$$\frac{d}{dt}\begin{bmatrix} \Delta i_d \\ \Delta i_q \\ \Delta v_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R\omega}{L} & \omega & -\frac{m_a\omega}{L}\cos(\Phi_\circ) \\ -\omega & -\frac{R\omega}{L} & -\frac{m_a\omega}{L}\sin(\Phi_\circ) \\ \frac{3}{2C}m_a\omega\cos(\Phi_\circ) & \frac{3}{2C}m_a\omega\sin(\Phi_\circ) & -\frac{\omega}{CR_{dc}} \end{bmatrix}\begin{bmatrix} \Delta i_d \\ \Delta i_q \\ \Delta v_{dc} \end{bmatrix} +$$

$$\begin{bmatrix} \frac{\omega}{L} & 0 & -\frac{m_a\omega}{L}\sin(\Phi_\circ) \\ 0 & \frac{\omega}{L} & -\frac{m_a\omega}{L}\cos(\Phi_\circ) \\ 0 & 0 & -\frac{3}{2C}m_a\omega(i_{d0}\sin(\Phi_\circ) + i_{q0}\cos(\Phi_\circ)) \end{bmatrix}\begin{bmatrix} \Delta U_d \\ \Delta U_q \\ \Delta\Phi \end{bmatrix} \quad (3\text{-}7)$$

The frequency domain analysis is used to obtain the transfer function of eq. (3-7). For simplicity, the converter power losses are neglected (i.e. R=0, R_{dc}=0). So the equivalent transfer function that relates Δi_q and $\Delta\Phi$ can be found as follows:

$$\frac{\Delta i_q}{\Delta\Phi} = \frac{\frac{m_a\omega}{L}\left(S^2 + \frac{3m_a^2\omega^2C}{2L}\right)V_{dc\circ} + \left(\frac{3m_a^2\omega^3C}{2L}\right)i_{q\circ}}{S\left(S^2 + \omega^2 + \frac{3m_a^2\omega^2C}{2L}\right)} \quad (3\text{-}8)$$

The block diagram of an indirect controller for SSSC is given in Figure 3-3. The 3-phase injected voltages, ($V_{inj\text{-}a}$, $V_{inj\text{-}b}$, and $V_{inj\text{-}c}$) generated by the converter, the

transmission line AC voltages, (V_a, V_b and V_c) and transmission line currents (i_a, i_b and i_c) are sensed and fed into the Blocks 1, 2 and 3 respectively.

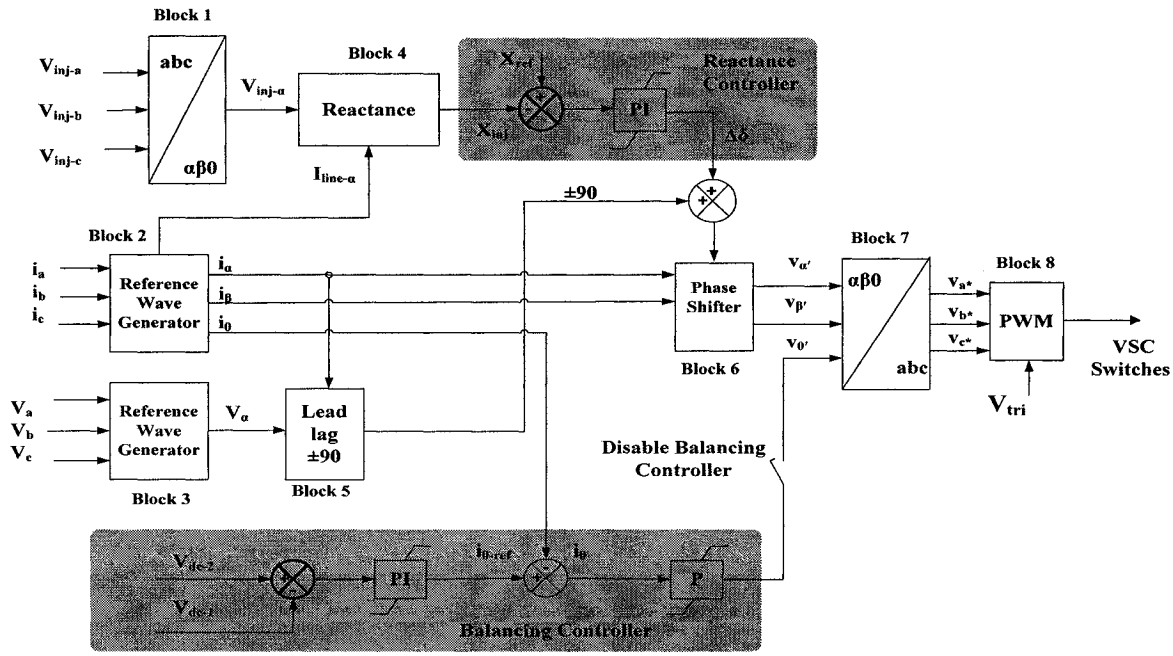

Figure 3-3: Indirect control block diagram of SSSC

Block 1 is used to transform the 3-phase injected voltages (V_{inj-a}, V_{inj-b}, and V_{inj-c}) to the α-β-0 coordinates domain and obtain the positive sequence voltage V_{inj-a}.

$$\begin{bmatrix} V_{inj-\alpha} \\ V_{inj-\beta} \\ V_{inj-0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{inj-a} \\ V_{inj-b} \\ V_{inj-c} \end{bmatrix} \quad (3\text{-}9)$$

Block 2 is used to transform the 3-phase line currents (i_a, i_b and i_c) to the α-β-0 domain using RWG block; this block was described in more detail in Section 2.8. The i_α

and i_β components are fed to the phase shifter (Block 6) while the zero sequence component i_0 is fed the Balancing Controller. For generating reference waveforms for control purposes the 3-phase currents are transformed from a-b-c to α-β-0 coordinates, by using eq. (3-10).

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (3\text{-}10)$$

If the 3-phase current waveforms in a-b-c coordinates are balanced, then i_α and i_β components are sinusoidal and orthogonal, and i_0 represents the zero sequence component.

Block 3 is used to transform the 3-phase line voltages V_a, V_b and V_c to the V_α, V_β and V_0 domain using another RWG block with a similar transformation equal to eq. (3-9). Only the V_α component of this block is fed to the Lead/Lag Block (Block 5); the two other outputs V_β and V_0 are not required.

Block 4 receives the positive sequence voltage $V_{inj\text{-}\alpha}$ from Block 1 and the positive sequence of the line current $I_{line\text{-}\alpha}$ from Block 2. It computes the injected line reactance X_{inj} and sends it forward to the Reactance Controller Block.

Reactance Controller Block receives the injected reactance X_{inj} and compares it to the reactance reference value X_{ref}, and a PI controller amplifies the error, and generates the phase angle $\Delta\delta$.

Block 5 (Lead/Lag Block) receives the reference signal of the line voltage V_α from Block 3 and reference signal of the line current i_α from Block 2 and computes the 90 degree phase shift and its sign, weather leading (+1) or lagging (-1) of this angular

displacement. This information is summed with the output angle $\Delta\delta$ from the Reactance Controller.

Block 6 (Phase Shifter Block) receives the i_α and i_β reference signals from Block2 (RWG). These signals are modulated by the sum of the signals from the Reactance Controller and Lead/Lag Blocks to generate the modified reference signals v_α' and v_β'.

Block 7 is the α-β-0 to a-b-c transformation block used to convert the input 3-phase reference components v_α', v_β' and v_0', back to a-b-c coordinate system i.e. v_a^*, v_b^* and v_c^*. These signals are then fed to the PWM trigger unit (Block 8) which was described in Section 2.5.1. For generating reference waveforms for control purposes the 3-phase control signals are transformed from α-β-0 to a-b-c coordinates by using eq. (3-11):

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} \frac{2}{3} & 0 & \frac{\sqrt{2}}{3} \\ -\frac{1}{3} & \frac{\sqrt{3}}{3} & \frac{\sqrt{2}}{3} \\ -\frac{1}{3} & -\frac{\sqrt{3}}{3} & \frac{\sqrt{2}}{3} \end{bmatrix} \begin{bmatrix} i_\partial \\ i_\beta \\ i_0 \end{bmatrix} \qquad (3\text{-}11)$$

Balancing Controller is used to balance the DC-link voltages V_{dc1} and V_{dc2} of the C1 and C2 capacitors respectively of the VSC. If the capacitor voltages are unbalanced, a zero sequence reference current $i_{0\text{-ref}}$ is generated by a PI controller. The $i_{0\text{-ref}}$ is compared with the actual zero sequence current i_0 of the VSC's output and acted upon by a proportional controller, this produces the zero sequence control signal v_0', that join v_α' and v_β' components of the controller and are converted to 3-phase reference components, v_a^*, v_b^* and v_c^* which are then used as the reference signals for the PWM block. Consequently, the VSC generates a zero sequence current that passes through the

connection of the neutral point of the coupling transformer and the DC-link to equalize the voltages on the two DC capacitors.

In impedance control using indirect controller, the SSSC injects synchronous voltage with a magnitude proportional to the line current. Therefore, the SSSC emulates an ohmic compensating reactance equivalent to a capacitor or an inductor.

3.4.3 Direct controller

In contrast to the indirect controller described earlier, the direct controller regulates both magnitude and phase angle of the injected voltage V_{inj} into the transmission line. In this technique, the voltage V_{dc} is kept constant by the DC voltage Controller which regulates the injected phase angle φ, with respect to the line current. This scheme is more suitable to providing both active and reactive power line compensation if an external Energy Storage System (ESS) exists in the DC side of the VSC. Similar to the indirect controller technique, in reactive power compensation mode, the injected voltage leads/lags the line current by 90 degree. Only small phase displacement is required to compensate for the VSC losses by absorbing active power from the transmission line.

A simplified mathematical model of a 3-phase VSC for controller design is presented in [16]. The model that is obtained in eq. (2-7) is recalled. Since the DC-link voltage is kept constant, the VSC model in synchronous rotating reference frame is:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R\omega}{L} & \omega \\ -\omega & -\frac{R\omega}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \frac{\omega}{L} & 0 \\ 0 & \frac{\omega}{L} \end{bmatrix}\begin{bmatrix} U_d - V_d \\ U_q \end{bmatrix} \qquad (3\text{-}12)$$

The above equation demonstrates the possibility of independent control of i_d and i_q. The VSC voltage vector can be controlled as follows:

$$U_d = -\frac{L}{\omega}(X_1 - \omega i_q) + V_d$$
$$U_q = \frac{L}{\omega}(X_2 - \omega i_d) \tag{3-13}$$

By substituting eq. (3-10) in (3-9), this becomes:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R\omega}{L} & 0 \\ 0 & -\frac{R\omega}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \tag{3-14}$$

Eq. (3-14) shows the decoupled relationship of i_d and i_q. The two new variables X_1 and X_2 represent the output of the control system, and are shown as:

$$X_1 = (K_{p1} - \frac{K_{i1}}{S})(i_d^* - i_d)$$
$$X_2 = (K_{p2} - \frac{K_{i2}}{S})(i_q^* - i_q) \tag{3-15}$$

where i_d^* and i_q^* are the reference values of active and reactive currents, K_{p1}, K_{i1}, K_{p2}, K_{i2} are proportional and integral gains of the PI controllers. The system can be demonstrated by two independent systems with a simple first-order transfer function.

Figure 3-4 shows the overall control structure of a SSSC with direct Control method. The block diagram is similar to the indirect controller (Figure 3-3), and many of the same blocks are re-used; hence for reasons of brevity, the description of the Blocks with identical identification numbers is not repeated. Essentially Block 7 of the indirect controller is replaced by two blocks: Blocks 9 and 10 which achieve a transformation from the α-β-0 to a-b-c coordinates via an intermediary d-q-0 stage, as shown in equations (A-1) to (A-5) in Appendix A. However, here two control loops are needed to

regulate the d- and q- components of the control signals in the synchronous reference frame in order to regulate both amplitude and phase angle respectively of the injected voltage V_{inj}.

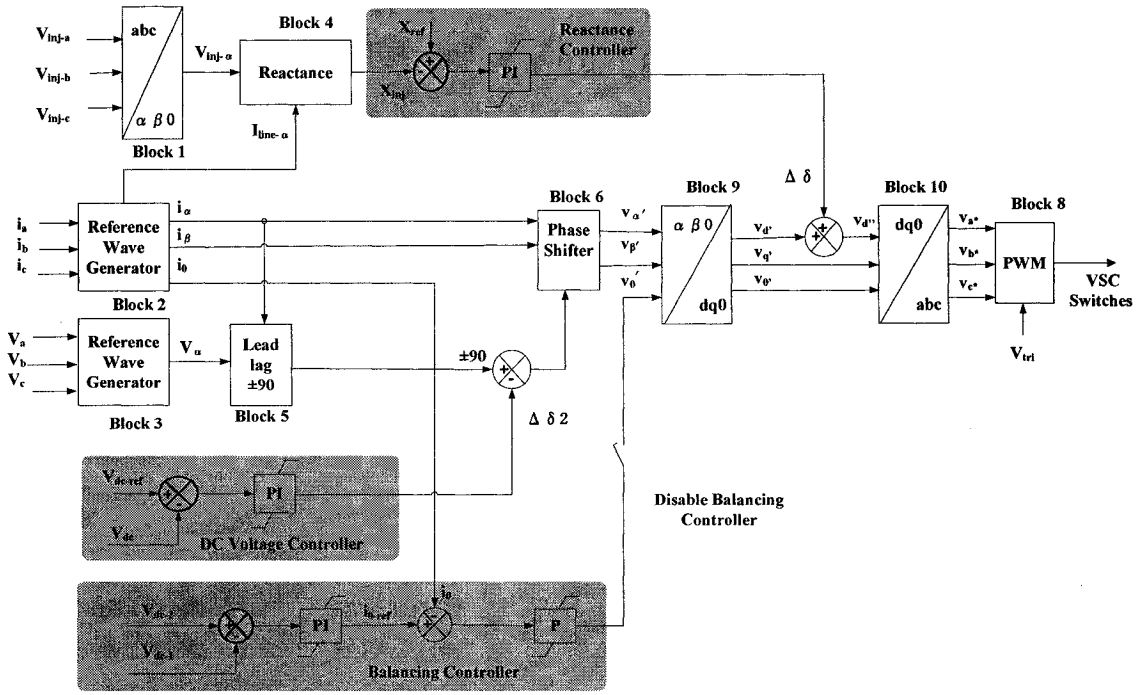

Figure 3-4: Direct control block diagram of SSSC

To regulate the injected voltage amplitude, the Reactance Controller is employed. The injected reactance X_{inj} is compared to the reference reactance value X_{ref} and a PI controller amplifies the error. The resultant is added to the d- component of the desired reference waveform $v_d^{'}$, and that varies the reference signals v_a^*,v_b^* and v_c^* of the PWM controller. The active power exchange is regulated by the phase angle φ of the injected voltage in response to an error in the DC-link voltage via PI controller. The DC-link voltage V_{dc} in the direct controller method is maintained constant and equal to $V_{dc\text{-}ref}$. and by changing the converter DC/AC gain, the injected voltage amplitude is controlled. Here, since the DC-link of the VSC is not equipped with an external energy source, it is

not capable of injecting any substantive amount of active power into the transmission line. Later in Chapter 4 by using two SSSC with back-to-back connection, the SSSC capability of injecting active power into the transmission system is investigated. In that case instead of controlling the injected voltage phase angle by DC Voltage Controller, the q-component of reference signal ($v_q^{'}$) is employed.

The same algorithm that was applied in Section 3.4.2 for the DC Voltage Balancing is used for direct controller.

3.5 Simulation results

An EMTP-RV based digital simulation of a SSSC, based on designs of VSC in Chapter 2, and control algorithm described in Sections 3-4-2 and 3-4-3, is presented here. Both direct and indirect control methods are applied on the system, and three tests are presented for each controller to investigate the performance of the system and controller. In order to make system measurements easier to evaluate, all the measurements are transferred to a per unit system with P_{base} =100 MVA and V_{base} =230 kV.

3.5.1 Power system

The power system in Figure 3-5 was simulated to evaluate the performance of the proposed SSSC. The operating voltage of the sending-end is 230 kV, and the transmission line impedance is (26+j132) ohms. The load is constant impedance with P=1.5 pu. and Q=1 pu.

The power system parameters are shown in Table 3-1.

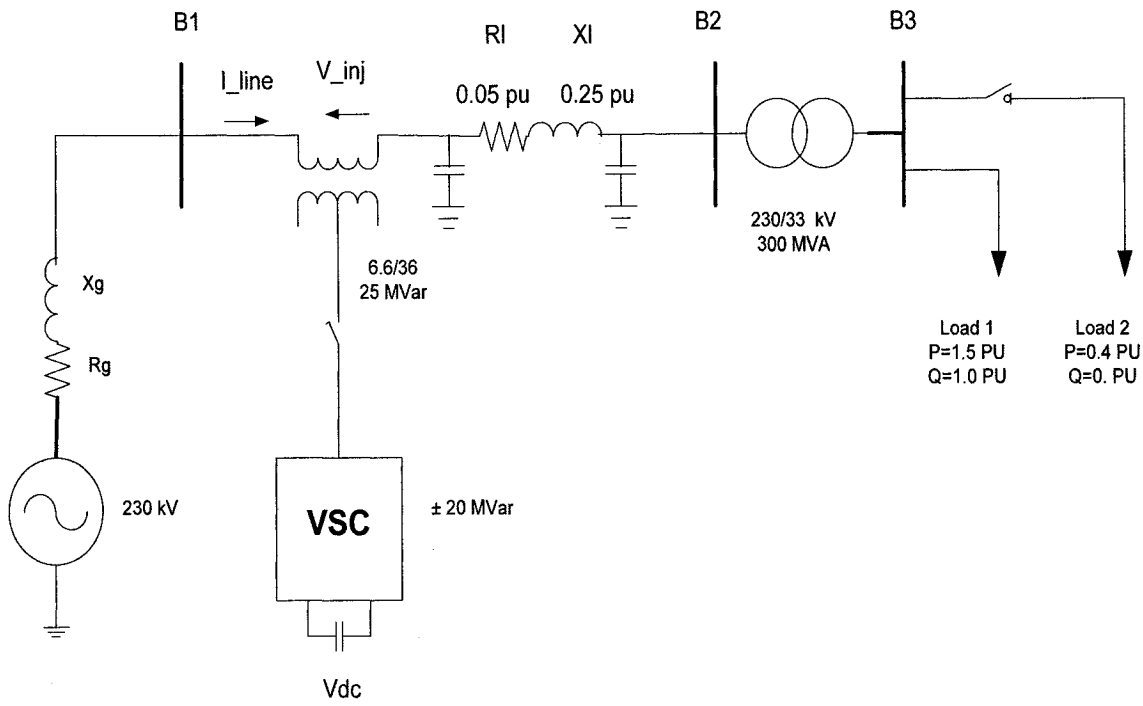

Figure 3-5: Single line diagram of the power system used for simulation

Table 3-1: Power system parameters

	Power	Voltage	R	X_L	X_C
Generator	1000 MVA	230 kV	0.001	0.005	0
Transmission Line			0.05 pu	0.25 pu	0.01 pu
Power Transformer	300 MVA	230/33 kV	0	0	0
Coupling Transformer	25 MVA	6.6/36 kV	0.001 pu	0.02 pu	0
SSSC	20 MVA	6.6 kV (AC) 10 kV (DC)	0	0	0
Base Values for pu system	100 MVA	230 kV			

3.5.2 Indirect controller

The algorithm, explained in Section 3.4.2, is used for control purposes. The controller is designed to compensate 40% of the transmission line reactance in capacitive operation. The PI controller parameters are: Kp = 75 and Ki = 2500. Four tests are presented to investigate performance of the system and controller:

- ***Impact of step change in reference value of injected reactance (Figure 3-6)***

The dynamic behavior of the controller is verified by applying a 20% step change in the injected reactance at 400 ms till 700 ms (Figure 3-6). The DC-link voltage is 1 pu at 10 kV. The SSSC is designed to compensate 40% of the transmission line reactance, therefore X_{ref} = 40% X_{line} or X_{ref} = - 0.1 pu (where X_{line}=0.25 pu)

The signals presented in Figure 3-6 are described below:

Figure 3-6 (a) shows the reactance reference step and the response of the controller. A 20% step change is applied from 400 ms to 700 ms; and the injected reactance increases from -0.1 to -0.12 pu. The dynamic behavior of the controller is stable and takes about 30 ms for the rise time and 80 ms for the settling time.

Figure 3-6 (b) shows the DC-link voltage of the VSC. When the reactance step down is applied at 400 ms, the DC-link voltage increases to match the magnitude of V_{inj}. The settling time is 80 ms. At 700 ms when the reactance is stepped up to its previous value, the DC-link voltage decreases to 0.275 pu.

Figure 3-6 (c) shows the injected voltage (V_{inj}). At 400 ms, by increasing the degree of compensation, the V_{inj} increases too and after 4 cycles the V_{inj} reaches to its steady-state. At 700 ms when the reference reactance steps up the V_{inj} decreases.

Figure 3-6 (d) illustrates the phase angle between the injected voltage and the transmission line current in phase a. The angle is almost 90 degrees, at 400 ms. When the disturbance is applied, the phase angle decreases transiently and the VSC absorbs more active power from the transmission line. At 700 ms, the phase angle transiently increases over 90 degrees for a short period of time (20 ms) to inject the active power back to transmission line and discharges the DC capacitor to 0.275 pu.

Figure 3-6 (e) shows the injected active and reactive power into the transmission line in phase a when the reactance step-down is applied at 400 ms, the injected reactive power increases to 0.073. At 700 ms by reducing the reference reactance the injected reactive power decreases by 0.062. At 400 ms for a short period the active power is absorbed from the transmission line to charge the DC-link capacitors. At 700 ms when the DC-link capacitors start discharging, active power is injected back to the transmission line.

Figure 3-6 (f) illustrates the rms value of the transmission line current. Between 400 ms to 700 ms when the injected reactance increases the transmission line current raises.

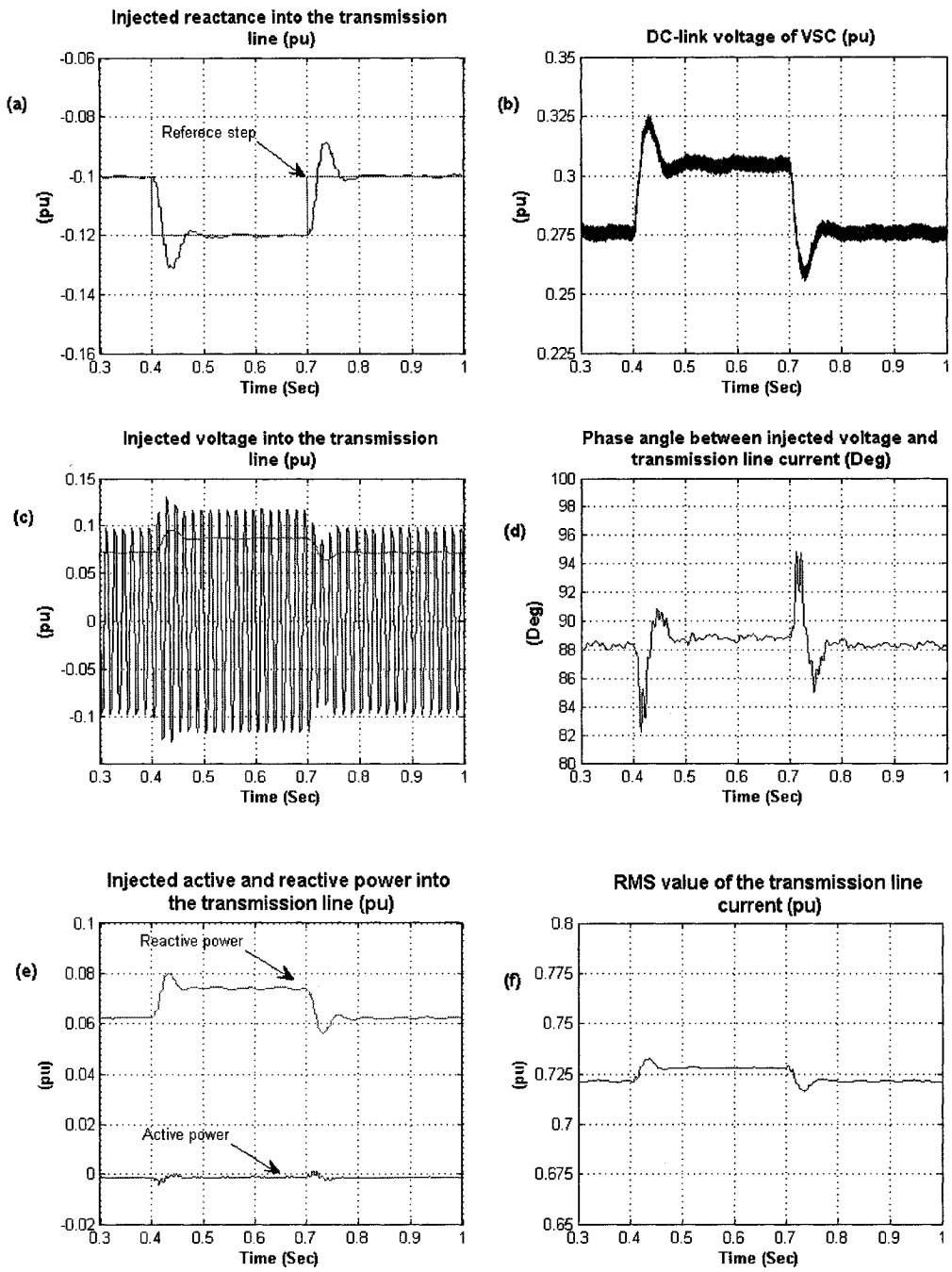

Figure 3-6: System response to step change in the controller reference value (a) Injected reactance (b) DC-link voltage (c) Injected voltage into the transmission line (d) Phase angle between the injected voltage and the transmission line current (e) Injected active and reactive power into the line (f) RMS value of the transmission line current

Sequence of events:

Time	Action
400-700 ms	Step change in controller reference value

- ***Impact of load variation on SSSC performance (Figure 3-7)***

The dynamic behavior of the SSSC is verified by increasing the receiving-end load by adding a load with P = 0.4 pu and Q = 0.25 pu, from 400 ms to 700 ms. The signals presented in Figure 3-7 are described below:

Figure 3-7 (a) illustrates the injected reactance into the transmission line. The load variation is applied between 400 to 700 ms, this change in the load causes only a transient that is damped quickly and in the steady state, the injected reactance stays constant at -0.1 pu.

Figure 3-7 (b) shows the DC-link voltage of the VSC. At 400 ms, when the load at receiving-end increases, the DC-link voltage reaches 0.34 pu, to provide the required injected reactance. At 700 ms, when the load decreases the DC-link voltage decreases to 0.275 pu.

Figure 3-7 (c) shows the injected voltage into the transmission line. At 400 ms, when the load increases at the receiving-end, the injected voltage increases and after four cycles the voltage reaches to steady state with peak value of 0.12 pu. At 700 ms when the load decreases the injected voltage decreases and takes five cycles for the voltage settling down.

Figure 3-7 (d) illustrates the phase angle between the injected voltage and the transmission line current in phase a. The phase angle is almost 90 degrees at 400 ms the phase angle transiently decreases and the VSC absorbs more active power from the transmission line. At 700 ms the phase angle transiently increases over 90 degrees for a short period of time (20 ms) to inject the active power back to the transmission line and discharge the DC-link capacitors.

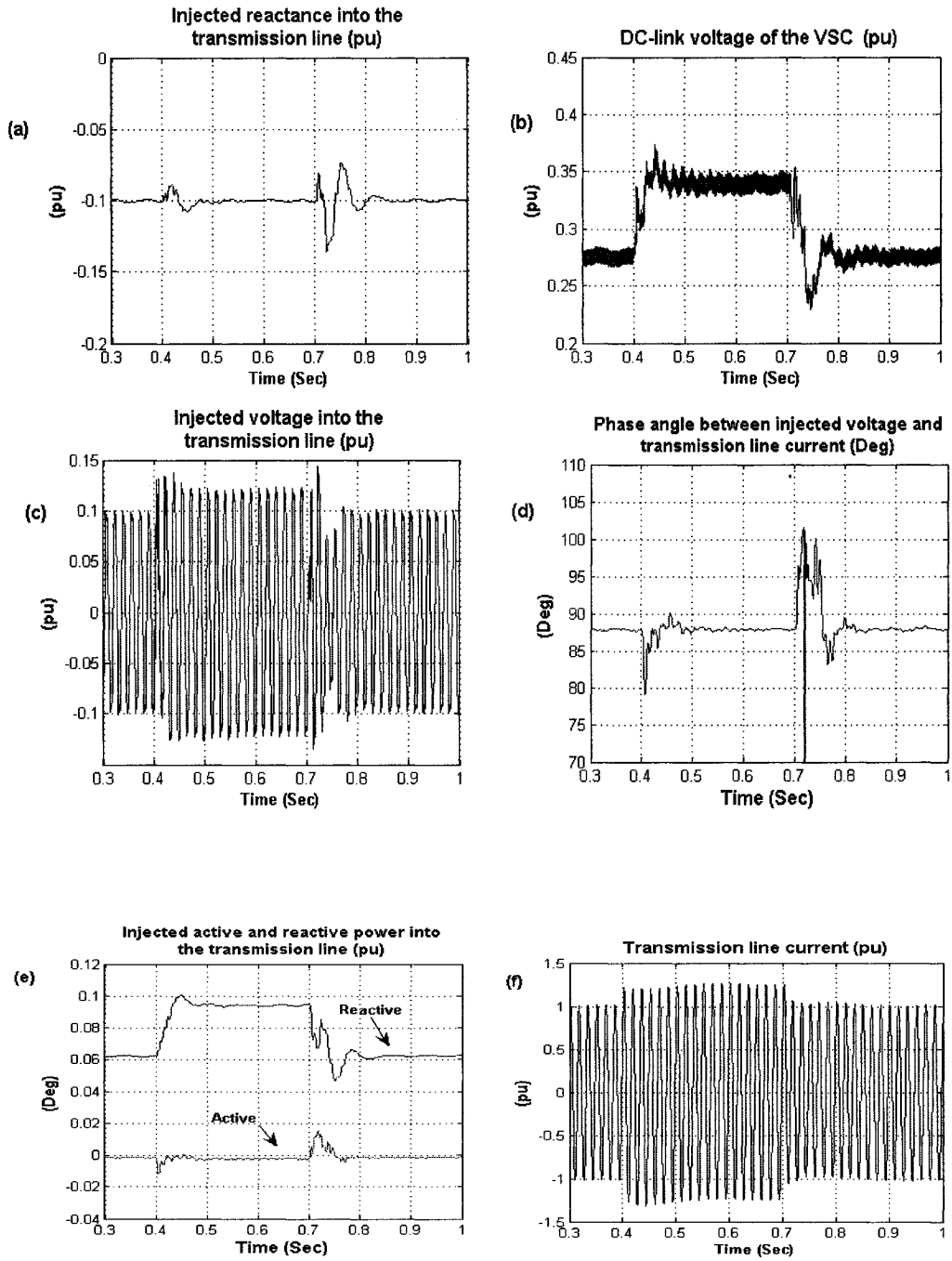

Figure 3-7: Impact of load variation (a) Injected reactance (b) DC-link voltage (c) Injected voltage to the line (d) phase angle between injected voltage and line current (e) injected active and reactive power (f) Transmission line current.

Sequence of events:

Time	Action
400-700 ms	Load change in receiving-end

Figure 3-7 (e) shows the injected active and reactive power into the transmission line. Between 400 to 700 ms, while the load at receiving-end of the transmission line increases the injected reactive power increases too. The settling time for reactive power is about 80 ms. At 400 the absorption of the active power increases transiently to charge the DC-link capacitors and at 700 ms the VSC injects the active power back into the transmission line to discharge the DC-link Capacitors to 0.275 pu.

Figure 3-7 (f) shows the fluctuation of the transmission line current. The transmission line current increases between 400 ms to 700 ms.

- ***Impact of a balanced fault at bus B3 of the power system (Figure 3-8)***

The response of the SSSC under balanced fault conditions is tested by applying a 3-phase fault on bus B3 at t = 400 ms till 700 ms. The transmission line current increases to a peak of 2.5 pu during the fault. To limit the fault current the VSC injects inductive reactance (X_{inj} = 0.15 pu) in series with the transmission line. Figure 3-8 shows the simulation results and the signals monitored are:

Figure 3-8 (a) shows the injected reactance into the transmission line. At 300 ms the converter operates in capacitive mode and injects -0.1 pu reactance into the transmission line. At 400 ms the SSSC operates in inductive mode, and injects a reactance with X_{inj} = 0.15 into the transmission line, the dynamic response is stable and settling time is about 50 ms.

Figure 3-8 (b) illustrates the injected voltage into the transmission line. At 400 ms the injected voltage increases to 0.4 pu and limits the fault current and it takes three cycles for the settling time.

Figure 3-8 (c) shows the phase angle between the transmission line current and the injected voltage. At 300 ms the angle in almost 90 degrees (lagging) at 400 ms till 700 ms, during the inductive operation, the phase angle changes to almost –90 degrees(leading).

Figure 3-8 (d) shows the transmission line current in phase a. At 400 ms the line current increases because of the balanced fault in the system.

Figure 3-8 (e) shows the exchanged active power with the transmission line. At 300 ms the SSSC operates in capacitive mode and absorbs active power to compensate the VSC losses. At 400 ms, in the inductive mode of operation, active power absorption increases transiently to charge the DC-link capacitors, and in 100 ms reaches the steady state.

Figure 3-8 (f) shows the injected reactive power into the line. At 300 ms the SSSC injects reactive power into the line at 400 ms during the inductive mode of operation the SSSC absorbs reactive power from the line.

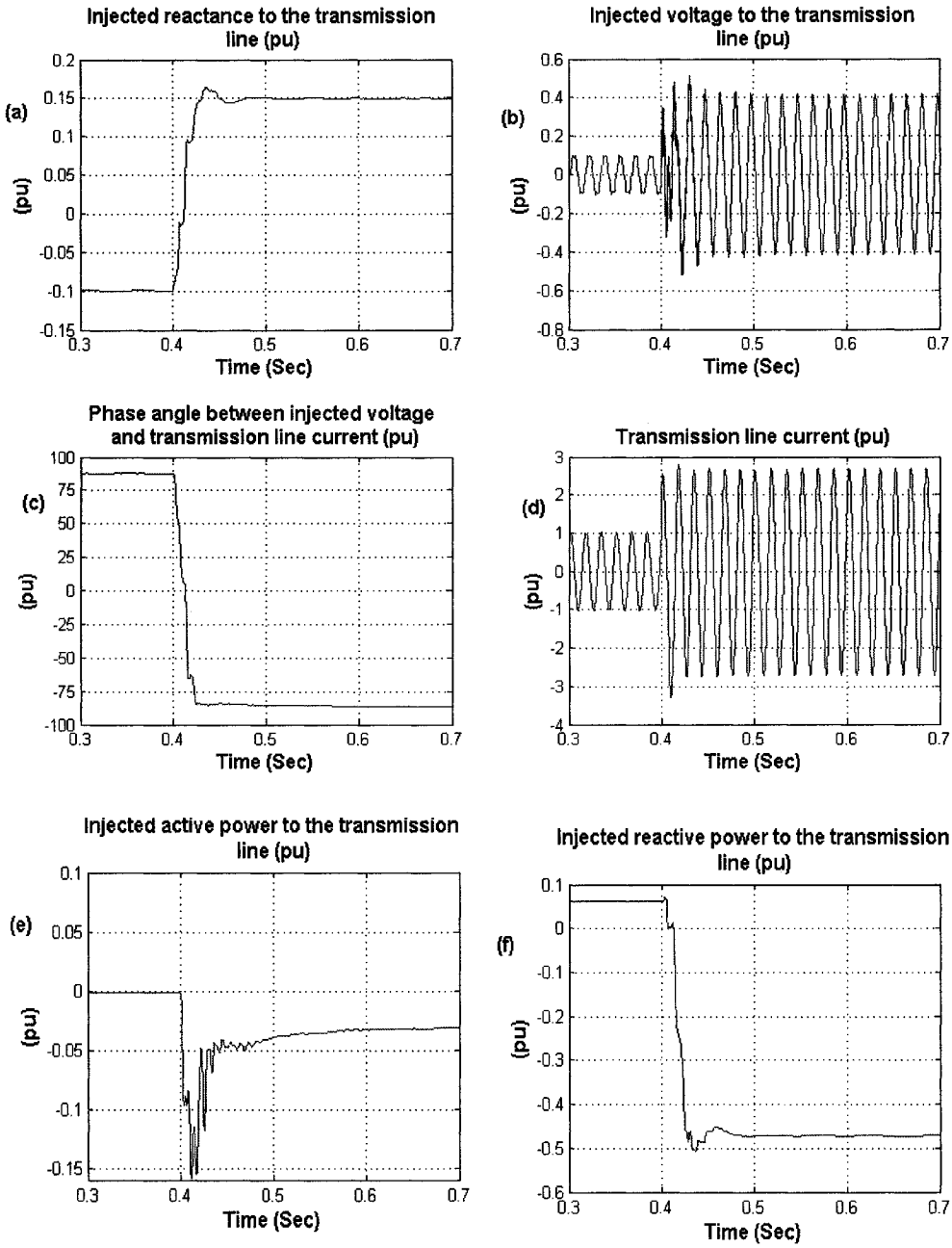

Figure 3-8: System response to a balanced fault (a) injected reactance (b) Injected voltage (c) Phase angle between injected voltage and transmission line current (d) Transmission line current (e) Injected active power (f) Injected reactive power

Sequence of events:

Time	Action
400-700 ms	Balanced fault at bus B3

- ***Impact of DC capacitor voltage balancing circuit (Figure 3-9)***

The balancing circuit behavior for two disturbances is shown in Figure 3-9. First applying a 20% step change in the reference value between 600 ms to 900 ms and second Disabling of the DC voltage balancing circuit from 1200ms to 1600 ms:

Figure 3-9 (a) this signal shows the injected reactance into the transmission line. Disturbances are observed due to the effect of DC-link voltages of the step change.

Figure 3-9 (b) the reference step change (600 to 900 ms) causes the two voltages V_{dc1} and V_{dc2} to be affected. The Disabling of the balancing controller (from 1200 to 1600 ms) shows the influence of the Balancing Controller to equalize the DC voltages.

Figure 3-8 (c) shows DC-link voltage, the negation of the voltage V_{dc1} and V_{dc2} is not ideal and a net disturbance is observable.

Figure 3-8 (d) illustrates the dynamic response of the controller to the reference step. The disabling of Balancing Controller has no influence on the DC voltages V_{dc1} and V_{dc2}.

Figure 3-8 (e) shows the zero sequence current into the converter, it has slight change with the reference step.

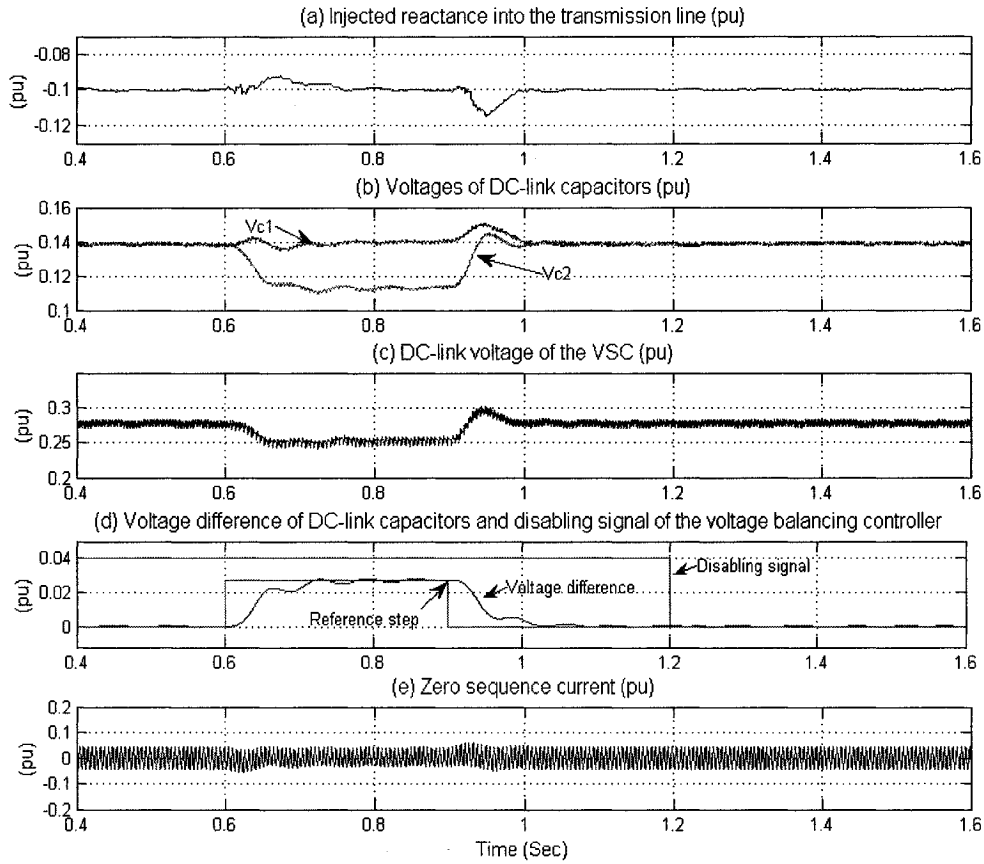

Figure 3-9: Impact of DC voltage balancing circuit (a) Injected reactance into the transmission line (b) DC-link voltages V_{dc1} and V_{dc2} (c) net DC-link voltage (V_{dc1}+V_{dc2}) (d) Voltage difference and disabling signal (e) Zero sequence current

Sequence of events:

Time	Action
600-900 ms	Step change of reference voltage V_{dc1}-V_{dc2}
1200-1600 ms	Disabling of the Balancing Controller

3.5.3 Direct controller

The algorithm explained in Section 3.4.3 is used for control purposes. The controller is designed to compensate 40% of the transmission line current in capacitive operation. The PI controller parameters are as below:

Reactance controller $K_p = 0.6$ and $K_i = 280$,

DC Voltage controller $K_P=80$ and $K_i=2500$,

Voltage balancing controller $K_{p1}=2$, $K_{i1}=80$, $K_{p2}=0.6$, and $K_{i2}=0.1$.

Three tests are presented to investigate performance of the control system.

- ***Impact of step change in reference value of injected reactance and DC-link (Figure 3-10)***

The dynamic behavior of the controller is verified by applying a 20% step change in the injected reactance from 400 ms to 600 ms and another step change in reference DC-link voltage at 800 ms till 1000 ms. The SSSC is designed to compensate 40% of the transmission line reactance, therefore $X_{ref} = 40\% X_{line}$ or $X_{ref} = - 0.1$ pu (where $X_{line}=0.25$ pu). The signals presented in Figure 3-10 are described below:

Figure 3-10 (a) shows the reactance reference step and the response of the controller. A 20% step change is applied between 400 ms to 600 ms and the injected reactance increases from -0.1 to -0.12 pu. The dynamic behavior of the controller is stable and takes about 80 ms for the settling time. At 800 ms when a disturbance in the reference value of the DC-link voltage is occurred, the X_{inj} oscillates and takes 100 ms for the settling time.

Figure 3-10 (b) shows the DC-link voltage of VSC. When the reactance step down is applied at 400 ms, the DC voltage stays constant. At 800 ms a 25 % step change is

applied on reference value of the DC-link voltage. Consequently the DC-link voltage increases from 0.4 pu to 0.5 pu and the rise time is about 20 ms.

Figure 3-10 (c) shows the injected voltage (V_{inj}) into the transmission line. By increasing the degree of compensation between 400 ms to 600 ms the injected voltage increases. At 800 ms the step change in DC-link cases a transient on the $V_{inj,}$ but the amplitude stays constant.

Figure 3-10 (d) illustrates the phase angle between the transmission line current and the injected voltage in phase a. The angle is almost 83 degrees, at 400 ms, when the disturbance is applied, the phase angle increases smoothly to 85 degree. At 800 ms when the DC-link voltage increases the phase angle transiently change for short period of time (30 ms) to absorb active power from the transmission line and charge the DC-link capacitors to 0.5 pu.

Figure 3-10 (e) shows the injected active and reactive powers into the transmission line in phase a. When the reactance stepped down is applied at 400 ms the injected reactive power increases to 0.075 pu and at 600 ms it returns to its previous value at 0.063 pu. At 800 ms the variation of DC-link voltage doesn't affect the steady-state value of the injected reactive power. The absorbed active power from the transmission line is constant during reactance reference disturbance, at 800 ms it increases transiently to absorb more active power from the line transmission to charge the DC-link capacitors.

Figure 3-10 (f) illustrates the rms value of the transmission line current. Between 400 ms to 600 ms when the injected reactance increases the transmission line current raises. At 800 ms the step change in DC-link reference causes a transient in the line current.

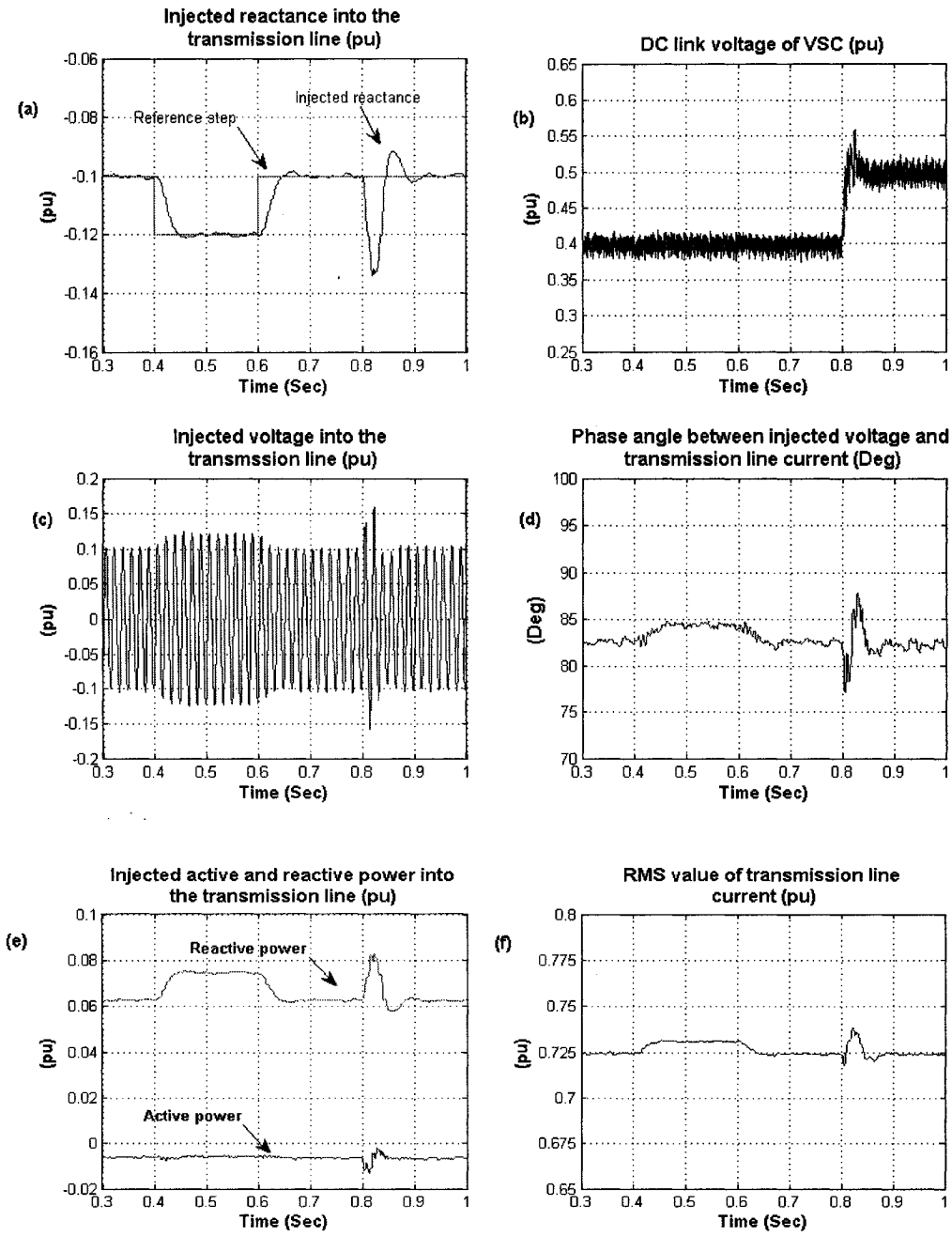

Figure 3-10: System response to step change in controller reference values (a) Injected reactance (b) DC-link voltage (c) Injected voltage to the transmission line (d) Phase angle between the injected voltage and the transmission line current (e) Injected active and reactive power to the line (f) RMS value of transmission line current

Sequence of events:

Time	Action
400-700 ms	Step change in injected reactance
800-1000 ms	Step change in DC-link voltage

- ***Impact of load variation on SSSC performance (Figure 3-11)***

The dynamic behavior of the SSSC is verified by increasing of the receiving-end load, by adding a load with P = 0.4 pu and Q = 0.25 pu at t = 400 ms till 700 ms, the signals presented in Figure 3-11 are described below:

Figure 3-11 (a) shows the injected reactance into the line. A 20% change in the load between 400 ms to 700 ms causes a transient with relatively high overshoot and is damped in 30 ms. in the steady state; the injected reactance stays constant at -0.1 pu.

Figure 3-11 (b) illustrates the DC-link voltage of the VSC. Between 400 ms to 700 ms when the load increases the DC-link voltage stays constant.

Figure 3-11 (c) shows the injected voltage into the transmission line. At 400 ms when the load increases at the receiving-end the injected voltage increases and after three cycles the voltage reaches to steady state. At 700 ms when the load decreases the injected voltage decreases and takes five cycles for the voltage settles down.

Figure 3-11 (d) shows the phase angle between the transmission line current and the injected voltage in phase a. The angle is 83 degree. At 400 ms and at 700ms when the load varies the phase angle transiently changes, but it is damped quickly.

Figure 3-11 (e) shows the injected active and reactive power into the transmission line. Between 400 ms to 700 ms while the load at receiving-end increases the injected reactive power increases too. At 400 the absorption of active power increases transiently to charge the DC-link capacitors and at 700 ms the VSC injects the active power back into the transmission line to discharge the DC-link Capacitors.

Figure 3-11 (f) shows the variation of transmission line current. Between 400 ms to 700 ms the peak value of the transmission line current increases to 0.12 pu.

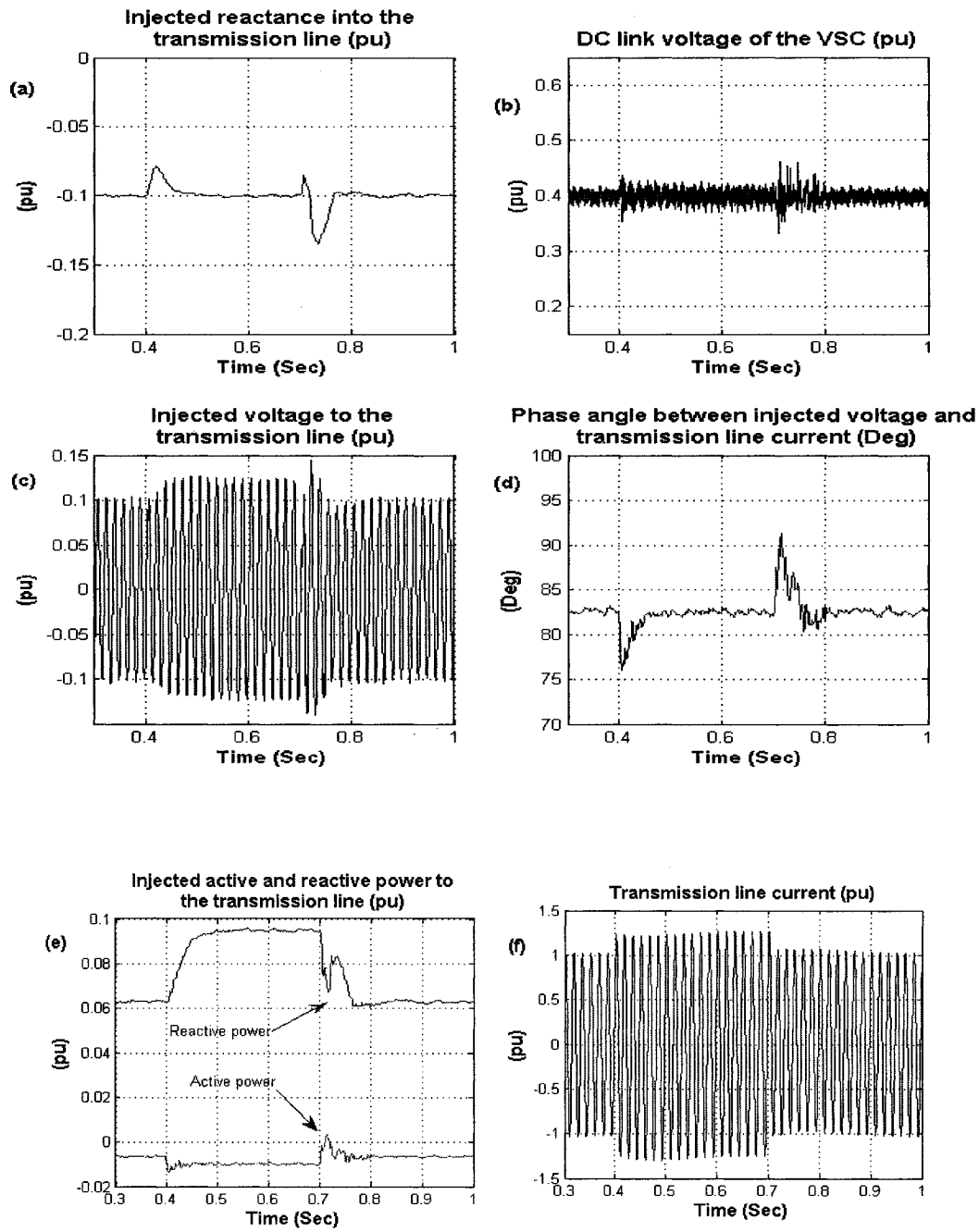

Figure 3-11: Impact of load variation (a) Injected reactance (b) DC-link voltage (c) Injected voltage to the transmission line (d) Phase angle between the transmission line current and the injected voltage (e) Injected active and reactive power into the line (f) Transmission line current

Sequence of events:

Time	Action
400-700 ms	Load change in receiving-end

- ***Impact of DC capacitor voltage balancing circuit (Figure 3-12)***

The balancing circuit behavior for two disturbances is shown Figure 3-12. First applying a 20% step change in the reference value from 600 ms to 900 ms and second disabling of the DC voltage balancing circuit from 1200ms to 1600 ms:

Figure 3-12 (a) shows the injected reactance into the transmission line. As expected no disturbances is observed.

Figure 3-12 (b) the reference step change (600 to 900 ms) causes the two voltages V_{dc1} and V_{dc2} to be affected in opposite manner such that the net influence of the step will be negated on the overall DC voltage, as shown in (c). The Disabling of the balancing controller (from 1200 to 1600 ms) shows the influence of the Balancing Controller to equalize the DC voltages V_{dc1} and V_{dc2}.

Figure 3-12 (c) shows DC-link voltage, the net DC-link voltage is virtually stable although high frequency differences are observed.

Figure 3-12 (d) shows the dynamic response of the controller to the reference step. The disabling of Balancing Controller (from 1200 to 1600 ms) shows the influence of the Balancing Controller to equalize the DC voltages V_{dc1} and V_{dc2}.

Figure 3-12 (e) shows the zero sequence current into the converter, the dynamic response follows the reference step.

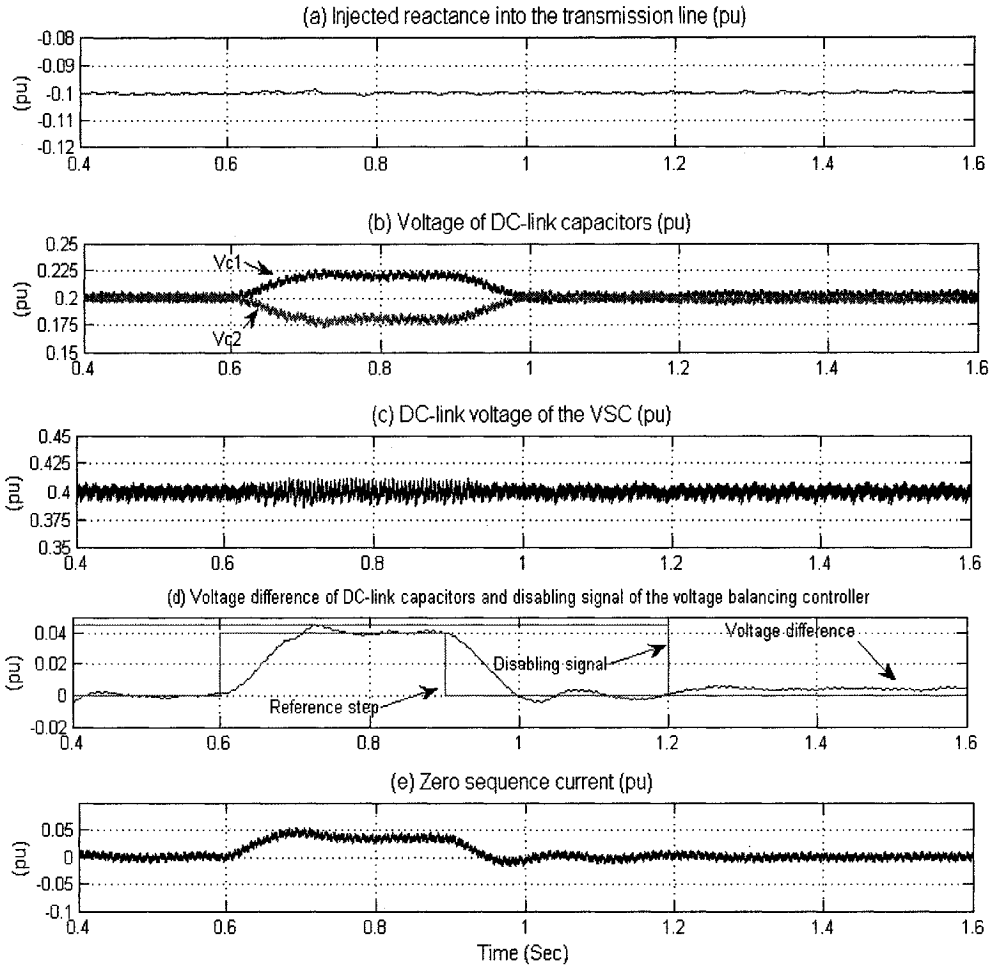

Figure 3-12: Impact of DC voltage balancing circuit (a) Injected reactance into the transmission line (b) DC-link voltages V_{dc1} and V_{dc2} (c) net DC-link voltage (V_{dc1}+V_{dc2}) (d) Voltage difference and disabling signal (e) Zero sequence current

Sequence of events:

Time	Action
600-900 ms	Step change of reference voltage V_{dc1}-V_{dc2}
1200-1600 ms	Disabling of the Balancing Controller

3.6 Discussion

The results of the SSSC model in EMTP-RV have shown to be virtually identical to those simulated by Sen [27] and indicated by Hingorani [1]. The simulation results show that SSSC provides fast and reliable series compensation. It operates in both inductive and capacitive modes and has the ability to limit the line current following a balanced fault in the power system. In Table 3-2 the major characteristics of direct and indirect control method are given.

Comparisons of two implemented control strategies show that each of them has advantages and disadvantages. Direct controller results in lower harmonic distortion in the output voltage and injects higher resistance into the transmission line compare to the indirect controller. In direct controller the fixed DC-link voltage must be carefully selected. Since the modulation index lies between zero and one, the DC-link voltage must be high enough to maintain the required SSSC output voltage in order to obtain appropriate control. However, if the DC-link voltage is set too high, the ratings of the DC capacitors and converter valves must be increased.

Indirect control method has a simpler configuration compare to direct control method, but it has slower response to any disturbances. One more advantage of the indirect method is that the DC-link voltage varies according to the power system condition. The DC voltage balancing controller in indirect method is unable to match the step change and equalize the DC-link capacitor voltages.

Table 3-2: Comparison of direct and indirect controller

	Direct controller	**Indirect controller**
DC-link Voltage (pu)	0.4	Variable
Injected voltage Magnitude (pu)	0.707	0.707
Injected voltage Phase angle (Deg)	83	88
Converter gain	variable	0.7
Injected reactive power (pu)	0.065	0.062
Injected active power (pu)	-0.008	-0.002
Settling time of X_{inj}	50 ms	70 ms
Overshoot of X_{inj}	0.9	1.2
Settling time of V_{dc}	40 ms	80 ms
Overshoot of V_{dc}	1.1	1.1

3.7 Summary

In this chapter, the operating conditions and constrains of SSSC is explained. Two control strategies known as direct and indirect control methods are discussed and implemented in EMTP-RV. In both control strategies the DC side voltages are controlled via phase-shift angle between transmission line current and injected voltage. DC-link voltage balancing is reached by regulating the zero sequence current through connection of neutral points of coupling transformer and DC-link capacitors.

The behavior of the SSSC control systems under various transient conditions such as step change in different reference parameters, load change, and balanced fault are monitored and the results are presented and analyzed.

Chapter 4

Interline Power Flow Controller (IPFC)

4.1 Introduction

An IPFC consists of two or more SSSCs that share a common DC-link (Figure 4-1). The SSSCs are usually utilized as a reactive compensator; while IPFCs could be employed as a comprehensive active and reactive compensator. IPFCs provide independent control of reactive power of each individual line, while active power could be transferred via the DC terminal between the compensated lines. This gives the IPFC an additional degree of freedom to control an added variable in the power system. This capability makes it possible to transfer power from overloaded to under-loaded lines, reduce the line resistive voltage drop, and increase the stability of the power system against dynamic disturbances.

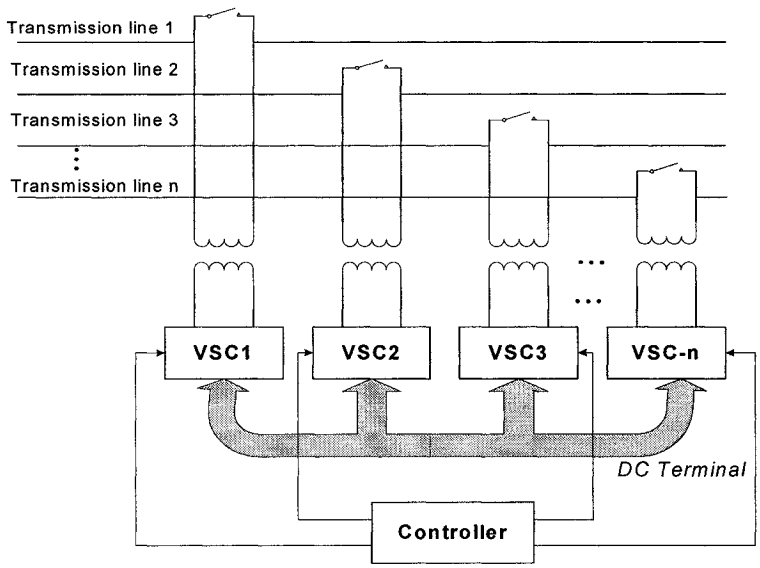

Figure 4-1: Schematic of an IPFC

The IPFC provides several operational functions depending on the system operating requirements, such as independent active and reactive power flow control, transmission angle regulation and transmission line impedance control [20]. This chapter describes the operation principles of the IPFC. Also, based on the study of SSSC controllers in Chapter 3, a control strategy for IPFC is proposed.

4.2 Basic principle of IPFC operation

Figure 4-2 shows a basic scheme of an IPFC consisting of two back-to-back VSCs that inject voltages in series with the transmission line. Each VSC is represented by a synchronous voltage source. $\mathbf{V_{s1}}$ and $\mathbf{V_{r1}}$ are the sending-end and receiving-end voltage phasors of the Line 1 respectively. $\mathbf{V_{s2}}$ and $\mathbf{V_{r2}}$ are the sending-end and receiving-end voltage phasors of the Line 2 respectively. The transmission lines impedances are represented by X_{L1} and X_{L2}. The VSCs' injected voltages are represented by $V_{inj-1}\angle\phi_1$ for Line 1 and $V_{inj-2}\angle\phi_2$ for Line2. The two lines are assumed identical and $V_{s1}=V_{r1}=V_{s2}=V_{r2}=1$ pu. The phasor diagrams of system 1 and system 2 are shown in Figure 4-3.

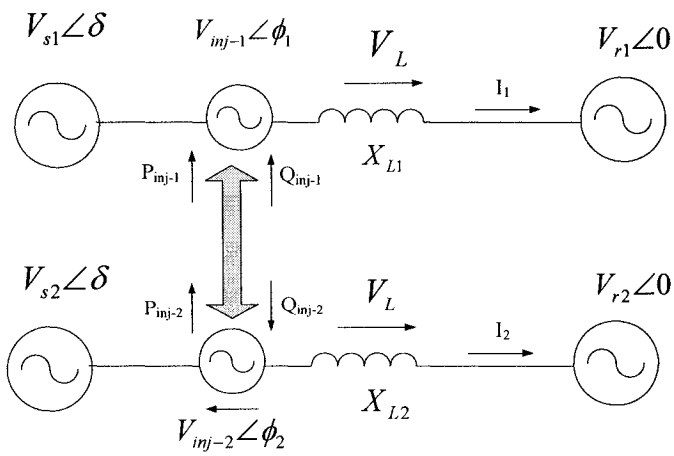

Figure 4-2: Basic Schematic of an IPFC

The prime (master) system is capable of regulating both injected active and reactive powers into the transmission line. In the second (slave) system only the injected reactive power is controllable.

In Figure 4-3 the injected voltage phasor $\mathbf{V_{inj-1}}$ with a controllable amplitude ($0<V_{inj-1}<V_{inj-max}$) and angle ($<0\phi<360$) is added to the $\mathbf{V_{s1}}$ phasor. The $\mathbf{V_{inj-1}}$ phasor operating area is a circle and depends on its amplitude and angle, so the voltage drop across the transmission line can be regulated.

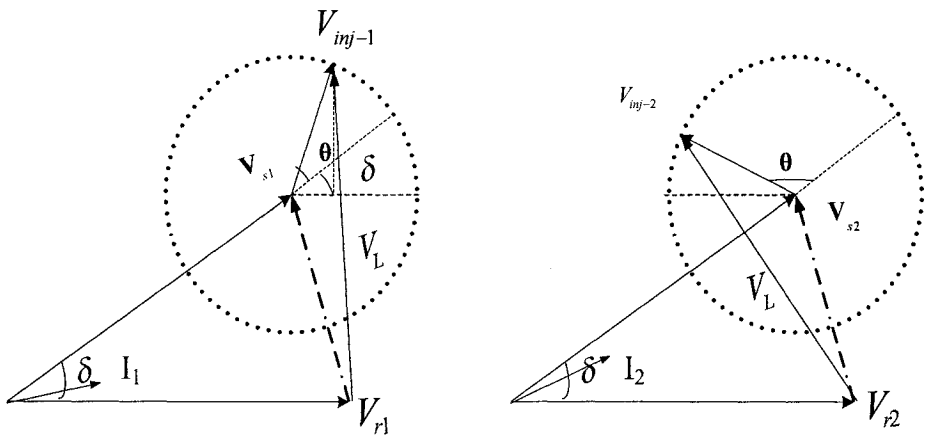

Figure 4-3: Phasor diagram of IPFC (a) System 1 (b) system 2

4.2.1 Active power exchange of IPFC

Controlling the phase angle of the injected voltage regulates the active power exchange between the IPFC and the transmission line. If the transmission line resistance is neglected the exchanged active power can be estimated as follows:

$$P_{ex} = \frac{VV_{inj}}{X_L}\left(\sin(\delta+\theta)-\sin\theta\right) \qquad (4\text{-}1)$$

4.2.2 Power flow at the receiving-end

In IPFC, since the DC-link voltage is maintained by one of the SSSCs, the rest of the SSSCs can be considered as voltage sources with controllable magnitude and phase angle. Therefore, both active and reactive power flow in the transmission lines are controllable. The power flow at the receiving-end can be estimated by the following equations if the line resistance is neglected.

$$P_R = \frac{V^2}{X_L}(\sin\delta\ ) + \frac{VV_{inj}}{X_L}(\sin(\delta+\theta)\ )$$
$$Q_R = \frac{V^2}{X_L}(\cos\delta - 1) + \frac{VV_{inj}}{X_L}(\cos(\delta+\theta)) \qquad (4\text{-}2)$$

In this thesis, an IPFC application for transmission line impedance regulation is investigated. More details on transmission line power flow control by applying IPFC can be found in [20], [22], [29].

4.3 IPFC constraints

4.3.1 Operating limits

The IPFC has the following limitations:

- Series VSC, complex power rating

  $| S_{ser\text{-}i} | \leq S_{ser\text{-}max}$

  where $S_{ser\text{-}i}$ is the complex power that is injected into the transmission line by VSC.

  The rated power of IPFC is specified by its rated injected voltage amplitude and rated transmission line current.

- The injected series voltage into the transmission line:

$V_{inj\text{-}i} \leq V_{inj\text{-}max}$

- The active power supply is constrained by the minimum transmission line current. Basically, in IPFC the active and reactive power compensation are independent. But in inductive mode of operation by increasing the degree of compensation the transmission line current decreases and the VSC has limited voltage rating to provide the required MVA for the transmission line.

4.3.2 The active power in DC-link

In the IPFC, the active power extracted by one of the VSCs must be equal to the active power that is supplied into the other transmission lines, if the VSCs losses are neglected. Therefore, the total active power that the IPFC can exchange with the transmission line is zero i.e.

$$\sum_{i} P_{series-i} = 0 \quad (i = 1,2,...) \tag{4-3}$$

where $P_{series\text{-}i}$ shows the active power that each SSSC exchange with the transmission line and can be calculated by:

$$P_{series-i} = V_{inj-i} * I_{line-i} * \cos(\phi_i) \tag{4-4}$$

where ϕ_i is the phase angle between the injected voltage and the transmission line current of each line.

4.4 IPFC controller strategy

As mentioned earlier, depending on the operating requirements of the power system, the IPFC can have several operational functions. In this thesis, the IPFC is designed to

maintain the impedance characteristic of the two transmission lines. The first block is capable of injecting both resistive and inductive impedance into the transmission line. The second block injects only inductive impedance into the transmission line and in addition it keeps the DC-link voltage at the desired level. In both control systems, the series VSCs are equipped with a direct controller. Hence the DC-link voltage is kept constant, and by varying the converter's gain and phase angle the injected voltage is regulated. Each SSSC is independently controlled. Thus, the IPFC consists of two control blocks that operate separately. The first block regulates both injected reactance X_{inj-1} and resistance R_{inj-1} into the transmission Line 1. The second block maintains the DC-link voltage and regulates the injected reactance X_{inj-2} into the transmission Line 2.

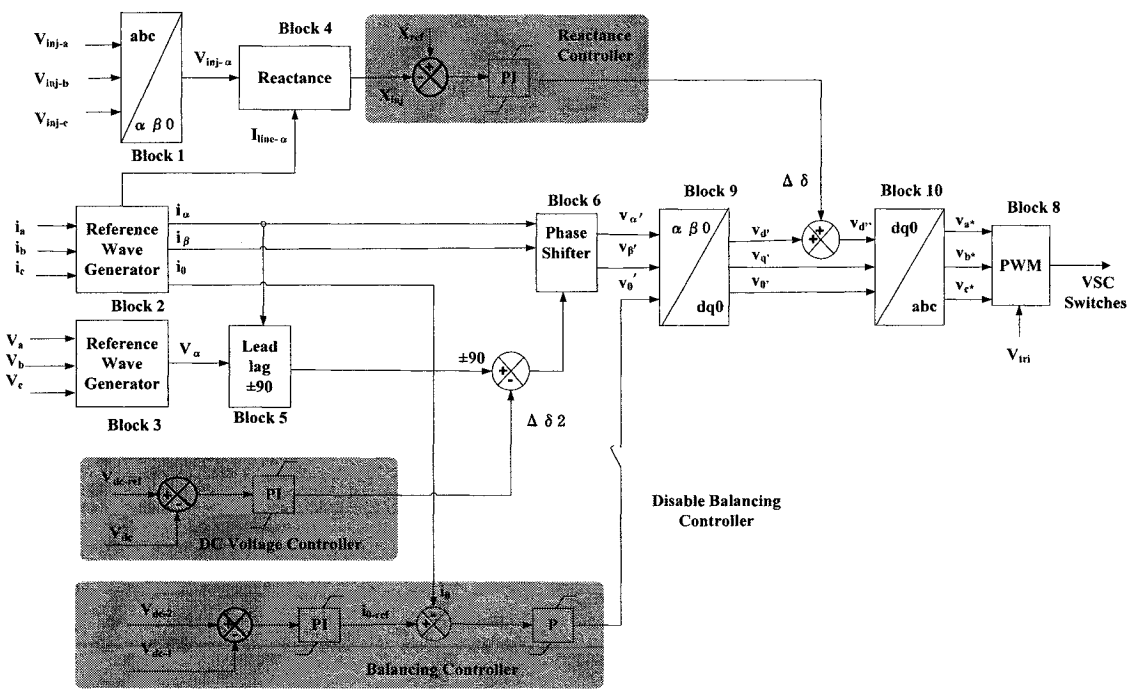

Figure 4-4: IPFC second block

Figure 4-4 shows the controller block diagram of the IPFC second system. This is a SSSC block diagram with a direct controller (explained in detail in Section 3.4.3). It

consists of two control loops, for regulating the injected reactance, and maintaining the DC- link voltage at desired level, And also a voltage balancing controller that balances the voltages of DC side capacitors. The second block not only must absorb enough active power to compensate the VSC losses, but also it must supply the required active power for the first block. Therefore, the phase angle of injected voltage with respect to transmission line current is expected to be less than a standalone SSSC that was found to be around 90 degrees. Consequently, the second block provides a constant DC voltage for the first block and performs as an Energy Storage System (ESS).

Figure 4-5 shows the overall control structure of the IPFC first block. This block diagram is similar to the block diagram of the direct controller (Explained in Section 3.4.3) and IPFC second block (Figure 4-4), and many of the same blocks are re-used. Since the DC-link voltage is controlled by the second block, DC voltage controller and Balancing Controller are eliminated in the first block. However, here two control loops are required to regulate the d- and q- components of the current in the synchronous reference frame in order to regulate both the amplitude and phase angle of the injected voltage V_{inj}.

Block 1 is used to transform the 3-phase injected voltages (V_{inj-a}, V_{inj-b}, and V_{inj-c}) to the α-β-0 coordinate domain and obtain the positive sequence of injected voltage $V_{inj-\alpha}$.

Block 2 is used to provide synchronized reference signals for control purposes. The 3-phase transmission line current (i_a, i_b, and i_c) are transformed to the α-β-0 domain, by using RWG block; this Block is described in Section 2.8.; The i_α, i_β, and i_0 components are fed to the Phase Shifter (Block 6).

Block 3 is used to transform the 3-phase line voltages V_a, V_b, and V_c to the V_α, V_β, and V_0 domain using RWG block. Only V_α component from this block is fed to Lead/Lag Block (Block 5), and the two other outputs V_β, and V_0 are not required.

Block 4 receives the positive sequence voltage $V_{inj-\alpha}$ from Block 1 and the positive sequence current from Block 2. It computes both injected reactance and resistance into the transmission line and send them forward to Reactance Control and Resistance Control blocks respectively.

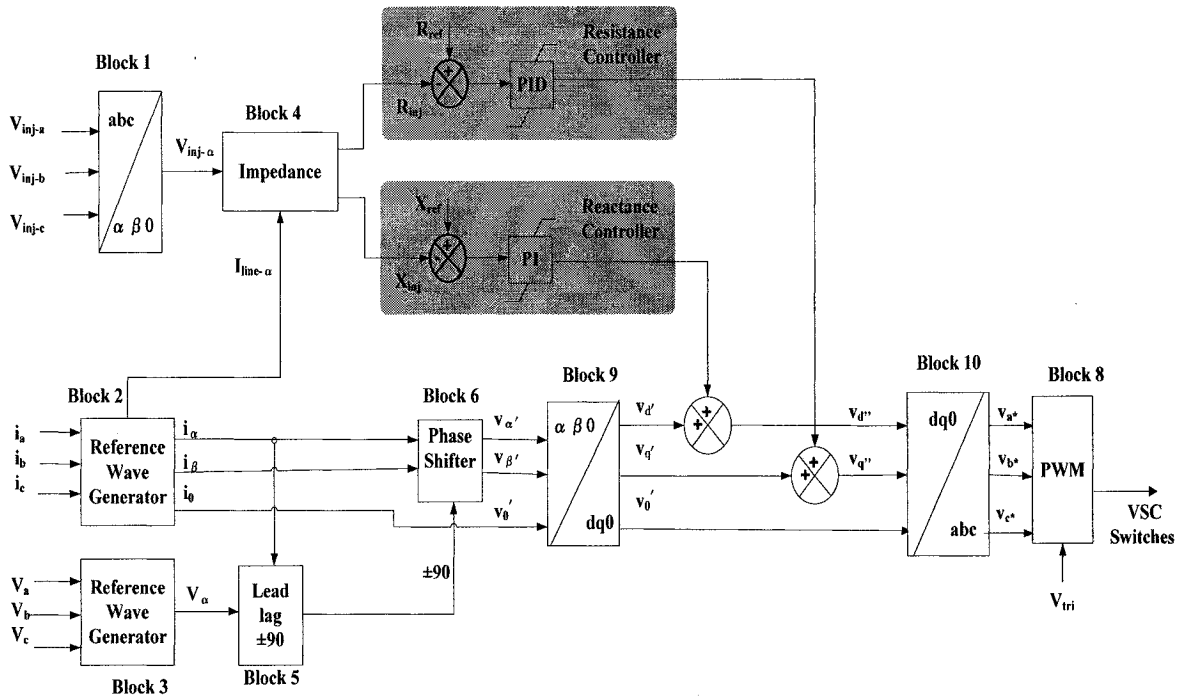

Figure 4-5: IPFC first block

Block 5 (Lead/Lag Block) receives the reference signal of the line voltage V_α from Block 3 and reference signal of the line current i_α from Block 2 and computes the 90 degree phase shift and its sign, weather leading (+1) or lagging (-1) of this angular displacement.

Block 6 (Phase Shifter Block) receives the reference signals (i_α, i_β, and i_0) from Block2. These signals are modulated by the signals from the Lead/Lag Block to generate the modified reference signals v_α', v_β', and $v_{0'}$. These signals are +90 or -90 degrees shifted from the reference signals.

Block 9 is used to transform the reference signals v_α', v_β', and v_0' from α-β-0 to d-q-0 coordinates v_d', v_q', and $v_{0'}$ by using eq. (A-4) in Appendix A.

To regulate the injected reactance, the Reactance Controller is employed. The injected reactance X_{inj-1} is compared to a reference value X_{ref} and a PI controller amplifies the error. The result is added to the d- component of the desired reference waveform $v_{d'}$, and generates $v_{d''}$. In similar way, the injected resistance is regulated by the Resistance Controller. For this purpose, the injected resistance R_{inj-1} is compared to reference value R_{ref} and the error is amplified by a PID controller. The result is added to the q-component of the desired waveform $v_{q'}$ and generates $v_{q''}$. In this particular case a PID controller is applied to reduce the oscillations of the time response.

Block 10 receives the modified d- and q- components $v_{d''}$, $v_{q''}$, and $v_{0'}$ and transformed them to 3-phase coordinate by using (eq A-5) in Appendix A, these signals are used as the reference signals v_{a*}, v_{b*}, and v_{c*} of the PWM controller. And the PWM Block provides firing pulses for the 3-level NPC VSC switches.

Since the second block regulates the DC-link voltage and keeps it at a certain level, theoretically the first block is capable of injecting a voltage with a phase angle in the range of 0 to 360 degrees.

4.5 Simulation results

A digital simulation using EMTP-RV of an IPFC based on the control algorithm described in Section 4.4 is presented. Figure 4-6 shows the simulated power system that consists of two identical power transmission systems with the characteristic given in Section 3.5.1. Two tests are performed to investigate the performance of the control system. In order to make system measurements easier to evaluate all the measurements are transformed to a per unit system with P_{base} =100 MVA and V_{base} =230 kV.

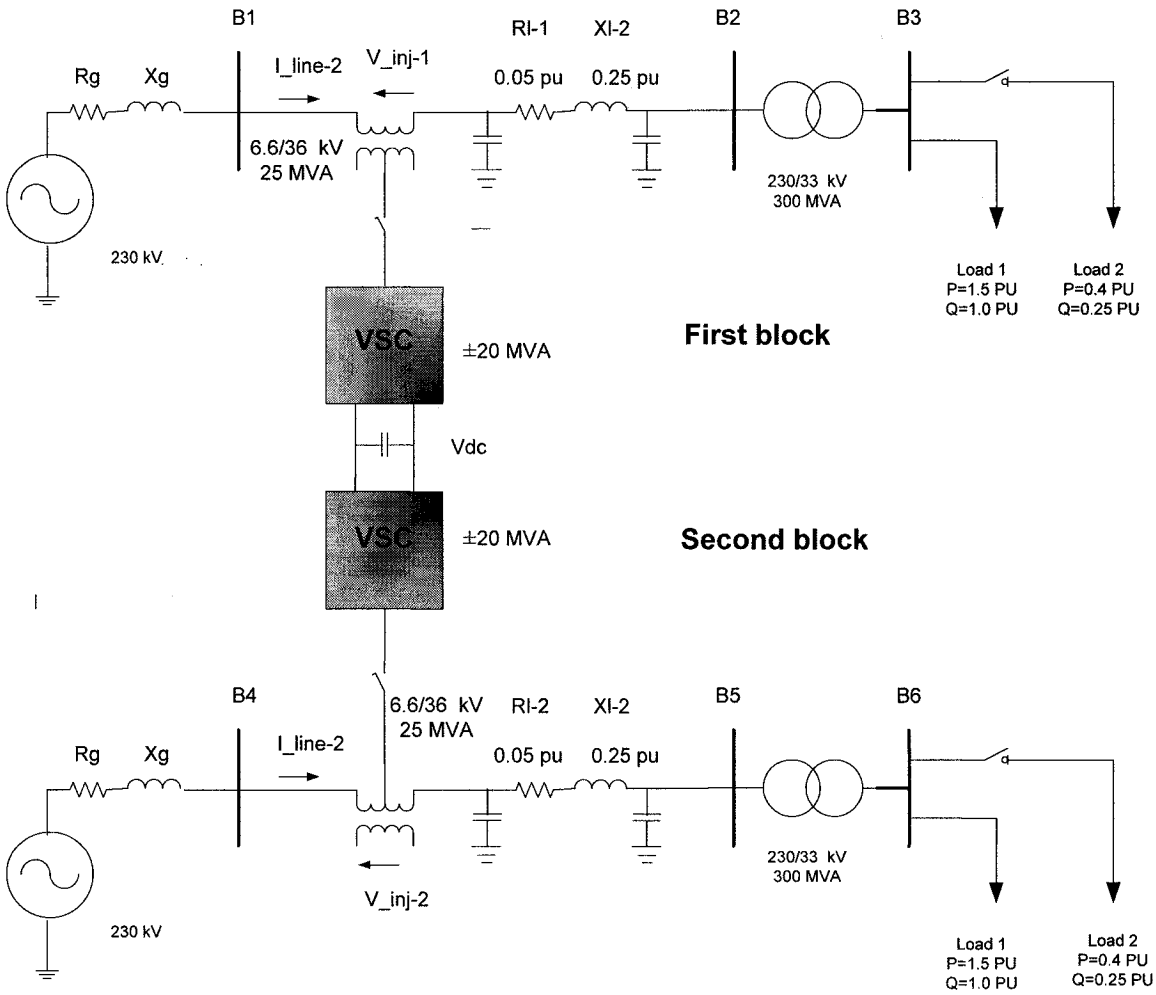

Figure 4-6: Single line diagram of the power system used for simulation

4.5.1 IPFC controller

The algorithm explained in Section 4.4 is used for control purposes. In first block, the controller is designed to compensate 40% of the transmission line reactance and 20% of transmission line resistance. In second block the controller is designed to compensate 40% of the transmission line reactance and keep the DC-link voltage of the IPFC constant.

The controller parameters are:

First block:

Reactance controller Kp = 10 and Ki = 220

Resistance controller Kp = 4, Ki = 80, and K_D = 0.005

Second block:

Reactance controller Kp = 2 and Ki = 250.

DC-link voltage regulator Kp = 80 and Ki = 2500.

Two tests are presented to investigate performance of the control system.

- ***Impact of step change in reference values of the injected reactance and resistance on IPFC performance (Figure 4-7and 4-8)***

The dynamic behavior of the controller is verified by applying a 20% step change in the reference values of injected reactance and resistance in first block and a 20% step change in the reference values of injected reactance and DC-link voltage in second block. Figure 4-8 shows the results of the simulation.

The IPFC is designed to compensate 40% of the transmission line reactance and 20% of the transmission line resistance in the first block and 40% of the transmission line

reactance in the second block. Therefore, X_{ref} = 40% X_{line} = -0.1 pu and R_{ref} = 20% R_{line} = -0.01 pu (where X_{Line}=0.25 pu, and R_{Line}=0.05 pu). The DC-link voltage is 1 pu at 10 kV.

The plots presented in Figure 4-7 are described below:

Figure 4-7 (a) shows the DC-link voltage of IPFC and the reference step. A 20% step change is applied from 500 ms to 800 ms. Therefore, the DC-link voltage increases from 0.4 pu to 0.48 pu. The dynamic response is stable and takes 100 ms for settling time. The step changes in reference value of injected reactance and resistance in Lines 1 and 2 cause a small variation in DC-link voltage. Variation of injected resistance R_{inj} has a more effect on DC-link voltage, since it extracts active power from the DC-link terminal.

Figure 4-7 (b) shows the reactance reference step in Line 1 and the response of the controller. At 500 ms the DC-link voltage step change causes a transient that is damped after 200 ms. At 900 ms the step change in reference reactance in Line 1 is applied and the injected reactance is changed from -0.1 pu to -0.12. The result shows that the dynamic behavior is stable and takes about 200 ms for settling time.

Figure 4-7 (c) shows the reactance reference step and the response of the controller in Line 2. At 500 ms the DC-link voltage step change causes a transient that is damped after 100 ms. At 1300 ms the reactance reference step change is applied and the injected reactance is changed from -0.1 pu to -0.12 pu. The result shows the dynamic behavior is stable and takes about 100 ms for settling time.

Figure 4-7 (d) illustrates the resistance reference step and the response of the controller in Line 1. AT 1700 ms the step change is applied and the injected resistance is changed from -0.01 pu to -0.012 pu. The dynamic behavior of the controller is stable and

takes about 150 ms for the settling time. The injected resistance controller is more sensitive to any disturbances in the controller system.

Figure 4-7 (e) shows the injected voltage in Line 1. By increasing the degree of compensation between 900 ms till 1200 ms the peak value of the injected voltage increases from 0.1 pu to 0.12 pu.

Figure 4-7 (f) shows the injected voltage in Line 2. By increasing the degree of compensation between 1300 ms till 1600 ms the peak value of the injected voltage increases from 0.1 pu to 0.12 pu.

Figure 4-7 (g) illustrates the phase angle between the injected voltage and the transmission line current in phase (a) of Lines 1 and 2. The phase angle in Line 1 is around 95 degrees that demonstrates the active power injection into the Line 1. The phase angle in line 2 is around 83 degree. At 1700 ms, when the reference value of injected resistance in the Line 1 stepped down, the phase angle in Line 2 decreases to 80 degrees to transfer more active power from Line 2 to Line 1.

Figure 4-7 (h) shows the receiving-end active power in Line 1 and 2. The step change of DC-link voltage at 500 ms causes transient in reactive power in both lines, in Line 1 the settling time is longer than Line 2. The increment of the injected reactance at 900 ms in Line 1 and at 1300 ms in Line 2, increase the receiving-end reactive power. At 1700 ms when the resistance reference step down is applied the receiving-end active power increases from 1.65 pu to 1.66 pu in Line 1.

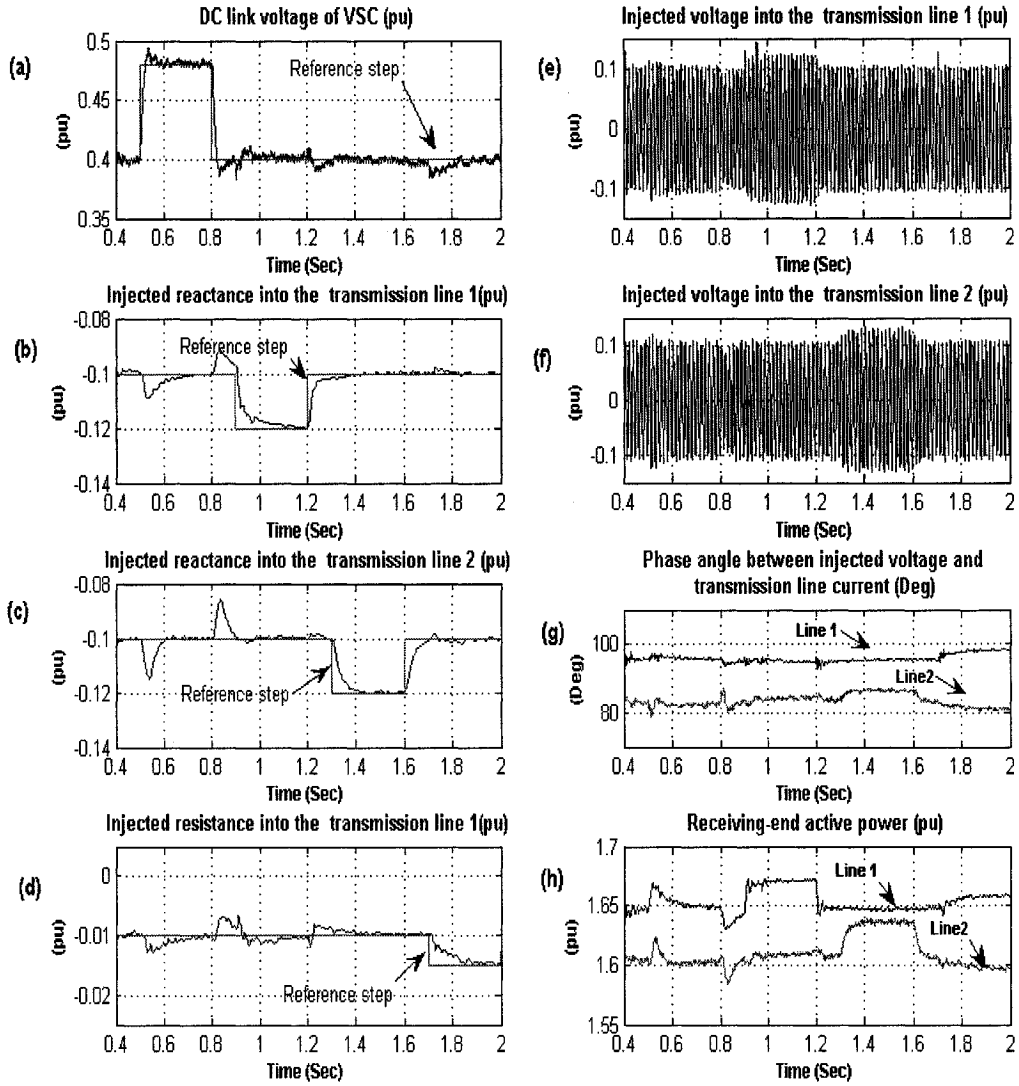

Figure 4-7: System response to step change of the controller reference values (a) DC-link voltage (b) Injected reactance into the Line1 (c) Injected reactance into the Line2 (d) Injected resistance into the Line1 (e) Injected voltage into the Line1 (f) Injected voltage into the Line2 (g) Phase angle between the injected voltage and the transmission line current (h) Receiving-end reactive power in Line 1 and Line 2.

Sequence of events:

Time	Action
500-800 ms	20% Step change in reference value of DC-link voltage
900-1200 ms	20% Step change in reference value of X_{inj} into Line 1
1300-1600 ms	20% Step change in reference value of X_{inj} into Line 2
1700-2000 ms	50% Step change in reference value of R_{inj} into Line 1

Figure 4-8 shows the receiving-end reactive power in Lines 1 and 2. The increment of the injected reactance in Line 1, between 900 ms to 1200 ms, increases the reactive power in receiving-end from 1.1 pu to 1.12 pu. In Line 2 the increment of the injected reactance, between 1300 ms to 1600 ms, increases the receiving-end reactive power from 1.07 pu to 1.085 pu. Also increasing the resistive impedance compensation in Line 1, between 1700 ms to 2000 ms, increases the reactive power in receiving-end in Line 1 and reduces the reactive power in Line 2.

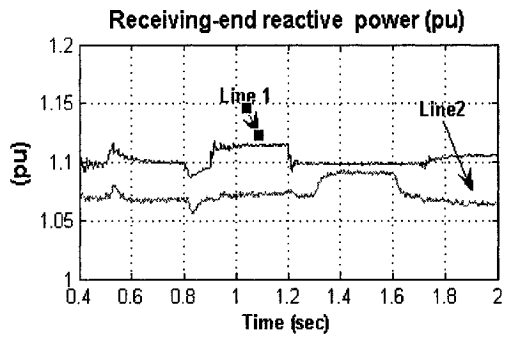

Figure 4-8: System response to step change in controller reference values

- ***Impact of load variation on IPFC performance (Figure 4-9 and 4-10)***

The dynamic behavior of an IPFC is verified by increasing of the receiving-end load in Lines 1 and 2. Between t = 400 ms till 600 ms a load with P = 0.4 pu and Q = 0.25 pu is added to the first block. And at t=600 ms till t= 800 ms a load with P = 0.4 pu and Q = 0.25 pu is added to the Second System.

The plots presented in Figure 4-9 and 4-10 are described below:

Figure 4-9 (a) illustrates the DC-link voltage of the IPFC. The DC-link voltage remains constant, but transiently changed with load variation.

Figure 4-9 (b) shows the injected reactance into the Line 1. A 20% change in the load causes a transient with relatively high overshoot and damped in 50 ms. In the steady state the injected reactance stays constant.

Figure 4-9 (c) shows the injected reactance into the transmission Line 2. A 20% change in the load of Line 2 causes a transient that is damped in 50 ms. In the steady state the injected reactance stays constant. The second control system is more stable to load variation than first control system.

Figure 4-9 (d) illustrates the injected resistance in Lines 1 and 2. The injected resistance in Line 2 is constant and has a low oscillation which is damped in 50 ms. In Line 1 the load variation change the injected resistance from 0.01 pu to 0.011 pu.

Figure 4-9 (e) illustrates the current in Line 1 and its rms value, between 400 ms to 600 ms increase around 20%.

Figure 4-9 (f) shows the injected voltage and its rms value into the Line 1. By increasing the load the injected voltage increases to keep the injected impedance constant.

Figure 4-9 (g) shows the current in Line 2 and its rms value, between 600 ms and 800 ms increase about 20%.

Figure 4-9 (h) shows the injected voltage and its rms value into the Line 2 by increasing the load; the injected voltage increases to keep the injected impedance constant.

Additional plots are shown in Figure 4-10 (a) to (c)

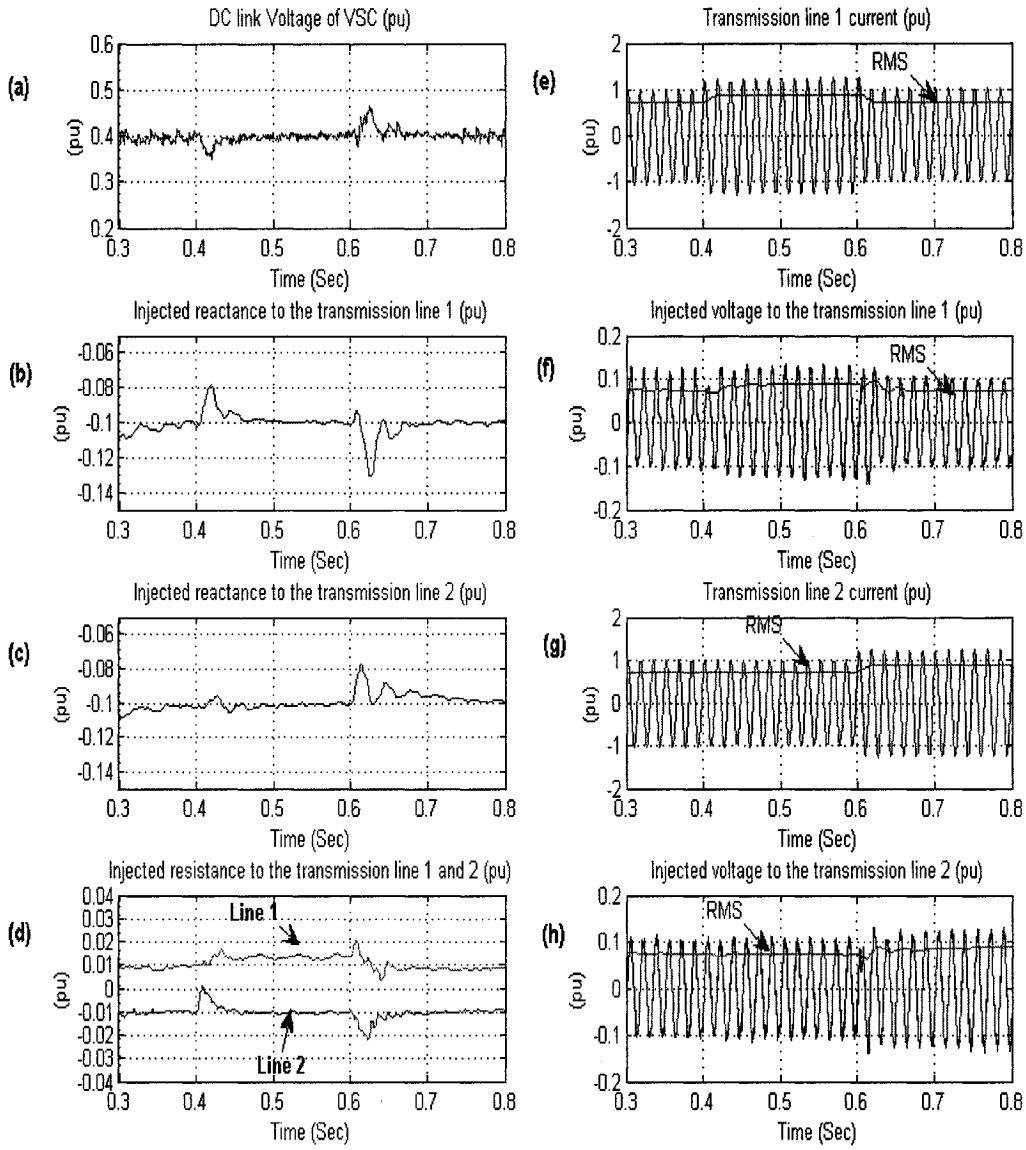

Figure 4-9: Impact of load variation (a) DC-link voltage (b) Injected reactance into the Line 1 (c) Injected reactance into the Line 2 (d) Injected resistance into the Lines 1 and 2 (e) Current in Transmission Line 1 (f) Current in Transmission Line 2 (g) Injected voltage into the Line 1 (h) Injected voltage into the Line 2

Sequence of events:

Time	Action
400-600 ms	Load change in transmission line 1
600-800 ms	Load change in transmission line 2

Figure 4-10 (a) shows the phase angle between the transmission line current and the injected voltage in phase (a) of Lines 1 and 2. The phase angle in Line 1 is about 95 degrees that indicates the active power injection in Line 1. The phase angle in Line 2 is around 83 degrees that indicates the active power absorption by Line 2. At 400 ms and 700 ms the phase angles change transiently to exchange active power with the Lines but they are damped quickly.

Figure 4-10 (b) illustrates the active powers at the receiving-end in Lines 1 and 2. Between 400 ms to 600 ms the active power in Line 1 increases because of the additional load. At 600 ms the active power in Line 2 increases.

Figure 4-10 (c) shows the reactive power at the receiving-end in first block, and in the second block. The reactive power in Line 1 between 400 ms to 600 ms increases because of load variation in receiving-end.

And also in Line 2 at 600 ms, the reactive power increases since the load varies in Line 2.

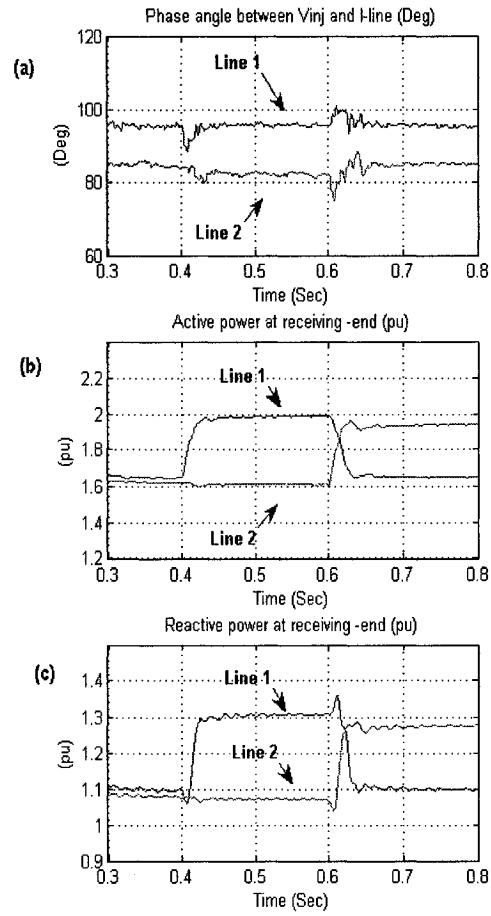

Figure 4-10: Impact of load variation (a) Phase angle between the injected voltage and the transmission line current in Lines 1 and 2. (b) Receiving-end active powers (c) Receiving-end reactive powers.

Sequence of events:

Time	Action
400-600 ms	Load change in transmission Line 1
600-800 ms	Load change in transmission Line 2

4.6 Discussion

The results of the IPFC model in EMTP-RV have validated the model presented by Gyugyi and Hingorani [1][20]. The simulation results show the capability of the IPFC in compensating both resistance and reactance of the transmission line. The results have shown the controllers are more sensitive to any disturbance as compared to a standalone SSSC.

4.7 Summary

The basic principle of IPFC operating conditions and constrains are presented. The behavior of the IPFC control system under various transient conditions for instance step change in reference parameters, and load change are monitored and the results are presented and analyzed.

Chapter 5

Conclusion

This thesis presents the development of EMTP-based models of series Voltage Source Converter (VSC) applications in the FACTS type power transmission systems. It includes the implementation of an exact model of a 3-level NPC VSC that is used to build the SSSC and IPFC applications for transmission systems. These offer potential of improving power transfer capability on existing transmission systems.

The IPFC is a multi-line FACTS device and consists of several SSSCs with a common DC-link. Both SSSC and IPFC are capable of controlling various parameters in power systems, such as active and reactive power flow, line impedance, and injected voltage in the power transmission lines.

In this research work, the detailed models of SSSC with direct and indirect controllers are implemented. Also, a voltage balancing controller for the DC-link capacitors in the 3-level NPC VSC is used. The indirect controller has a simpler design than the direct controller, and can only be used for reactive power exchange with a transmission line. In contrast, a SSSC with direct controller is capable of exchanging both active and reactive power with a transmission line if the VSC is equipped with a suitable EES in the DC side.

The presented IPFC consists of two directly controlled SSSCs, and is applied to regulate impedances in two identical transmission lines. The operation of the IPFC is validated at various operating conditions.

A 3-level NPC VSC is designed as the basic building block of the SSSC and IPFC. It has the advantages of lower converter losses and harmonic components when compared to a 2-level VSC. The reference waveforms are generated by using a fast synchronizing method based on the α-β-0 transformation. Also, PWM technique is used for generating the firing pulses for VSC switches.

The major contributions of this thesis are as follows:

- Design and Implementation of the SSSC and IPFC in EMTP-RV in order to compensate the transmission line impedance.
- Design of indirectly controlled and directly controlled SSSC.
- Develop a detailed model of a 3-level NPC VSC. The model includes detailed representation of valves, snubber circuits, and the passive components.
- Implementation of PWM technique for generating firing pulses for VSC switches.
- Implementation of Reference Wave Generator (RWG) that demonstrates better performances than conventional PLL.
- Validation of SSSC and IPFC operation to compensate for the impedance, and limiting the fault current in the transmission line has been shown by simulation results in EMTP-RV.

The following items may be considered for future work:

- Study of VSC-based FACTS controller in case of an unbalanced AC system.

- Study the effect of series VSC-based FACTS controller on transient and steady stability of the power systems as well as damping and control of sub-synchronous resonance.
- Investigation of appropriate filter for the transmission lines to reduce the generated harmonics by the FACTS controller.
- Study alternative control strategies in order to improve the performance of SSSC and IPFC.
- Investigation of alternative topologies for the VSC-based FACTS controllers such as multi-level Flying Capacitor VSC, with reference to the harmonic generation and converter losses.
- Study alternative methods for balancing the capacitor voltages in the DC-link of the converters.

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Appendix A

d-q-0 Transformation

The 3-phase sinusoidal system a-b-c is transformed to d-q-0 domain by applying the following transformation:

$$\begin{bmatrix} S_d \\ S_q \\ S_0 \end{bmatrix} = \frac{2}{3} * \begin{bmatrix} \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin\omega t & -\sin(\omega t - \frac{2\pi}{3}) & \sin s(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \qquad \text{(A-1)}$$

where S_a, S_b, and S_c are the variables (voltages or currents) in a-b-c coordinates; S_d, S_q, and S_0 are variables in d-q-0 coordinates, and $\omega = 2\pi f$ is the angular frequency.

The inverse transformation is defined by the following equation:

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} \cos\omega t & -\sin\omega t & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & -\sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} * \begin{bmatrix} S_d \\ S_q \\ S_0 \end{bmatrix} \qquad \text{(A-2)}$$

To simplify the algorithm in d-q-0 transformation it is preferred to first transform the original waveforms to symmetrical components (α-β-0 coordinates) and then transform them to d-q-0 components.

Eq (A-2) demonstrate a time varying system. The d-q axes rotate with the angular frequency ω.

If the axes are fixed at ω t=0, the transformation matrix given in eq. (A-1) becomes:

$$\begin{bmatrix} S_\alpha \\ S_\beta \\ S_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{A-3}$$

Eq (A-3) is known as the symmetrical component transformation. It transforms a set of 3-phase waveforms into α-β-0 coordinates. The α and β components are sinusoidal and orthogonal while 0 component is the zero sequence component and is equal to 0 axis in d-q-0 coordinates. The transformation from α-β-0 to d-q-0 domain is defined as:

$$\begin{bmatrix} S_d \\ S_q \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} * \begin{bmatrix} S_\alpha \\ S_\beta \end{bmatrix} \tag{A-4}$$

Combining equations (A-3) and (A-4), the a-b-c coordinates can be transformed to d-q-0 coordinates as:

$$\begin{bmatrix} S_d \\ S_q \\ S_0 \end{bmatrix} = \sqrt{\frac{2}{3}} * \begin{bmatrix} \cos\omega t & \sin\omega t & 0 \\ -\sin\omega t & \cos\omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{A-5}$$

The physical meaning of the d-q-0 transformation is shown in Figures A-1. Vector S is the reference signal. S_d rotates on the α-β plane with angle of $\theta(t) = \omega t$ from α axis. The d-axis is aligned with vector S_d and q-axis is perpendicular to d-axis on α-β plane. Therefore, d-axis and q-axis are rotating on the α-β plane with the angle of $\theta(t)$ form α-axis. The r-axis is the rotating shaft of d-q-0 coordinates. Therefore, 3-phase variables can be decomposed to d, q and 0 components by d-q-0 transformation.

The vector S contains all the information of the 3-phase variables, such as harmonics, and unbalance components. If the 3-phase variables (voltage or current) are sinusoidal and balanced, the locus of the vector S is a circle on the plane.

Generally, d and q components have DC and AC values while 0 component has only AC value. The DC values of d and q components come from positive components of the 3-phase variables. The AC component is the result of disturbances such as harmonics in the system. The 0 component comes from zero sequence of the 3-phase variables. Basically, in a balanced 3-phase system without harmonics the d component has a DC value while q and 0 components are zero.

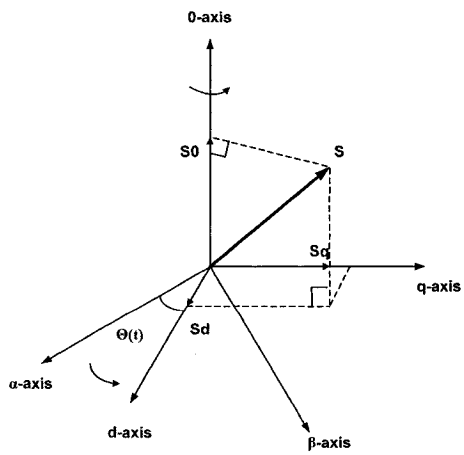

Figure A-5-1: Physical meaning of d-q-0 transformation

Appendix B

Passive component design:

In this appendix, the design of the snubber circuits and passive components of the VSCs that are used for the simulations are presented.

1. DC-link capacitors

In Section 2-7, the method of calculating the DC-link capacitors for a VSC is explained. For calculation of DC-link capacitors of a SSSC with direct and indirect controller, eq. (2-13) is recalled i.e.

$$C_{dc} = \frac{\left(\frac{I_m m_a}{2} - \frac{V_{dc,ave}}{R_{dc}}\right) * \Delta t}{\Delta V_{dc}} = \frac{\frac{I_m m_a}{2} - \frac{V_{dc,ave}}{R_{dc}}}{\Delta V_{dc} * f_s} \qquad \text{(B-1)}$$

The values of the power circuit are summarized in Table B-5-1 and in the last column the size of the capacitors are obtained from eq. (B-1)

Table B-5-1: Power circuit values and size of the DC-link capacitors

Controller	I_m (A)	V_{dc} (V)	ΔV_{dc}	m_a	f_s (Hz)	$R_{dc}(\Omega)$	C_{dc}(mF)
Indirect	1.5	0.285	8% V_{dc}	0.8	900	100	29
Direct	1.5	0.4	8% V_{dc}	0.8	900	100	21

Based on the above calculations, the total size of the DC-link capacitor for the SSSC with indirect control is C_{dc}= 30 mF

For the SSSC with direct control, the total size of the DC-link capacitors is given as C_{dc}= 20 mF.

2. Snubber circuit

In Section 2.6, the method of determining the snubber circuit elements was described. Eq (2-8) is recalled and the load and switch data are summarized in Table B-2.

$$\begin{cases} R_{on} = \dfrac{\Delta V_{CE}}{I_o} \\ \Delta V_{CE} = 10\% U_d \\ L_{on} = \dfrac{\Delta V_{CE} * t_{ri}}{I_o} \\ C_{off} = \dfrac{I_O * t_{fi}}{2 * U_d} \\ R_{off} = \dfrac{5 * U_d}{I_O} \end{cases} \qquad \text{(B-2)}$$

Table B-5-2: Load and switch data of VSC

Controller	U_d	ΔV_{dc}	I_0	t_{ri} (μs)	t_{fi}(μs)
Direct	0.2	0.02	0.7	5	5
Indirect	0.14	0.014	0.7	5	5

By using eq. (B-2) the following values of snubber elements can be found:

Table B-5-3: Snubber circuit elements

Controller	R_{ON}	L_{ON}	R_{OFF}	C_{OFF}
Direct	30 mΩ	0.142 μH	0.142 Ω	90 μF
Indirect	20 mΩ	0.1 μH	0.1 Ω	125 μF

Appendix C

List of Publications:

As a part of our research, the following articles were submitted to international conferences:

1. S. Salem and V. K. Sood " Modeling of series Voltage Source Converter applications with EMTP-RV" Int. Conference on Power System Transients (IPST'05) in Montreal, Canada on June 19-23 2005.
2. S. Salem, V.K. Sood "Modeling of SSSC with EMTP-RV" Submitted to IEEE Conference on International Symposium on Industrial Electronics, Montreal, Canada, and 9-13 July 2006