A Comparative Study of

Low Phase Noise Voltage-Controlled Oscillators (VCOs)

In CMOS Technology

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ABSTRACT

A Comparative Study of Low Phase Noise Voltage-Controlled Oscillators (VCOs) in CMOS Technology

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Voltage controlled oscillators (VCOs) are key components in frequency synthesizers for Radio Frequency (RF) wireless communications. The design of monolithic VCOs with standard CMOS processes has been the object of several recent research projects. The common goal of these attempts has been to investigate the possibility of meeting the very demanding VCO phase noise specifications without making use of bipolar processes or external components. Two categories of VCOs are studied in this thesis, one involving an inductor, and the other is inductor free, which is a ring oscillator.

The study of the phase noise performance of complementary LC VCO shows that most of the phase noises come from the tail current. A modification has been made based on this topology, where the tail transistor is removed. However this brings another problem: higher power consumption. To overcome this problem, sub-threshold techniques have been used leading to sub-threshold LC VCO. A Ring oscillator is designed at the end because of its wide tuning range and ease of implementation. Schematic simulations, layout and post-layout simulations are accomplished using TSMC 0.18 um CMOS technology. The performances of the three types of VCOs are compared regarding the oscillating frequency, phase noise and tuning range. All of these can be used in the Bluetooth applications. In addition, the figure of merit (FOM) of the designed VCOs is compared with work by other researchers.

Acknowledgements

I would like to take this opportunity to express my sincere gratitude to my supervisor, Dr. Rabin Raut for his initiating this project, and his invaluable guidance, suggestions, encouragements in all phases of this research. Also I am very thankful for the financial assistance he provided.

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I would like to dedicate this thesis to my husband Yu Xin Pan and our lovely daughter, Chantal Yao for their patience, encouragements and moral support during my whole studies.

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Summary of Notation

Abbreviations:

AM	amplitude modulation
AMOS	accumulation metal oxide semiconductor
ASITIC	analysis and simulation of spiral inductors and transformers for ICs
BiCMOS	Bipolar compatible Complementary Metal Oxide Semiconductor
BJT	bipolar junction transistor
CDR	clock and data recovery
CMC	Canadian microelectronics corporation
CMOS	complementary metal oxide semiconductor
FM	frequency modulation
FOM	figure of merit
HBT	heterojunction bipolar transistor
ISF	impulse sensitivity function
LTI	linear time-invariant
LNA	low noise amplifier
LPF	low pass filter
MOSFET	metal oxide semiconductor field effect transistor
NMOS	N-channel metal oxide semiconductor
PLL	phase locked loop
PMOS	P-channel metal oxide semiconductor
PSS	periodic steady state
Q	quality factor

RF	radio frequency
SiGe	silicon germanium
SSB	single side band
VCO	voltage controlled oscillator

1 Introduction

Communication plays an important role in our everyday life. Almost from the beginning of the electrical communication, oscillators have been the basic part of the communication system. Twenty years ago, most people chose Colpitts oscillators for frequencies in high mega hertz (MHz) range and bipolar junction transistors (BJT) were employed for the active device. Recently, the explosive growth in wireless communications and the advances in Complementary Metal Oxide Semiconductor (CMOS) technology made it possible to implement high frequency oscillators with CMOS technology.

In order to satisfy varying frequency bands for different communication systems and to allow wide band operation in a specific system, the oscillators are required to be tunable over a relatively wide frequency range. The tunability is usually obtained by a variable voltage and hence comes the name voltage controlled oscillators (VCO).

VCOs are key components in frequency synthesizers for Radio Frequency (RF) wireless applications. The design of monolithic VCOs within standard CMOS processes has been the objective of several recent research projects. The common goal of these attempts has been to investigate the possibility of meeting the very demanding VCO phase noise specifications of most portable communication systems, without making use of bipolar processes and/or external components. In the following a short review on several low noise VCOs in CMOS technology is presented.

1.1 A survey of low noise –Gm LC Oscillators in CMOS technology

From the viewpoint of monolithic integration it will be very desirable to build an oscillator using only transistors. But such active implementation (such as using gyrators to simulate inductors) will always result in unacceptable noise performance and power consumption. The usual practice to implement low noise oscillators is to employ a passive LC-tank circuit and an active circuit producing a negative resistance. The negative resistance balances the losses caused by the parasitic positive resistance of the LC-tank.

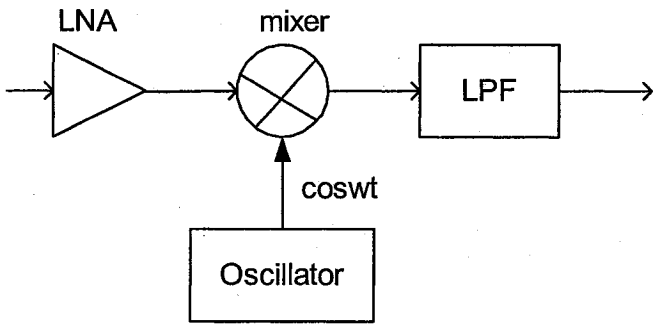


Figure 1Typical application of the Oscillator

A typical communication system with an oscillator is shown in Figure 1. In system applications the oscillating sources are used to drive Gilbert cell mixers. So, differential approaches are typically employed to realize the active sub-system of the VCO. A standard approach for differential VCOs is the use of cross-coupled transistors to generate a negative resistance. The negative resistance generated by the cross-coupled pair should be sufficient to overcome the equivalent parallel resistance of the VCO tank circuits to generate the desired oscillation. These VCO circuits are known as –Gm LC-

tank VCOs. A number of CMOS –Gm LC VCOs have been reported in the literature, e.g., [1]-[4].

The –Gm LC-tank VCO in CMOS technology has its challenges due to: (1) poor quality factor (Q) of the monolithic inductor, (2) limited tuning range of the varactors, and (3) poor flicker noise in CMOS compared to other technologies, such as SiGe HBT.

The phase noise performance of an –Gm LC-tank VCO is better than the ring oscillator. However, the bandwidth is generally limited. So to obtain a wide tuning range is an important challenge in most –Gm LC-tank VCOs. Typically two methods are employed to achieve this. These are (1) varying the inductor value, and (2) use of variable capacitors (i.e. switched capacitor array and/or varactors).

1.1.1 Oscillators using self-switched inductors

There are several approaches to implement large tuning range and low phase noise VCOs. One approach is to use the self-switched inductors. [5] The schematic is shown in Figure 2 below.

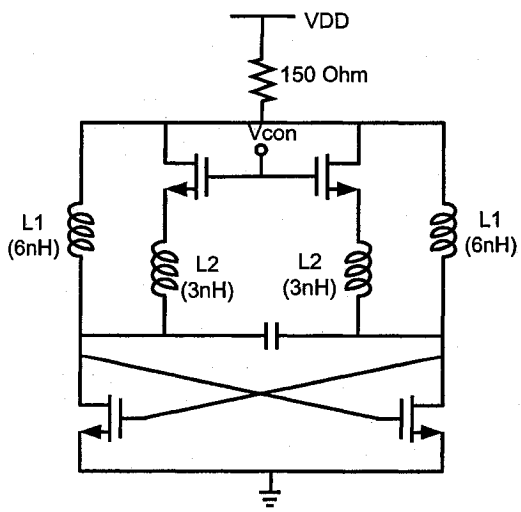


Figure 2 CMOS Oscillator with self-switched inductors

When the control voltage V_{con} is high, L1 and L2 are parallel and the oscillating frequency is high. When V_{con} is low, L2 is inactive and the oscillating frequency is low. The advantage of this topology is that it doesn't need a varactor, which on some level simplifies the design. However, since the inductors are switched on and off, it cannot perform a smooth continuous tuning. It needs four inductors, which will need substantial silicon area. Moreover, the performance depends on the quality factor of the inductors, with the potential of poorer phase noise performance for low quality-factor inductors.

1.1.2 Oscillators using Switched capacitor array technique

Since the quality factor (Q) values of on-chip inductors are not high, many applications prefer to vary capacitors in the LC-tank. Two approaches are shown below. [6] The schematic of the VCOs is shown in Figure 3. The simplified binary weighted switched capacitor array is shown in Figure 4 [7]. The C(V) in Figure 3 is a PMOS varactor parallel with a switched capacitor. Two such blocks make up C(V) in Figure 3(b). The capacitors controlled by the switches provide the coarse tuning whereas the PMOS varactor provides the necessary fine tuning. The small tuning range of the PMOS varactor maintains a small gain, whereas the overall tuning range is large due to the switched capacitors. To ensure continuous frequency tuning over process, voltage and temperature variations, the fine tuning range in simulation was assumed to overlap the coarse tuning step by a factor of two to three times.

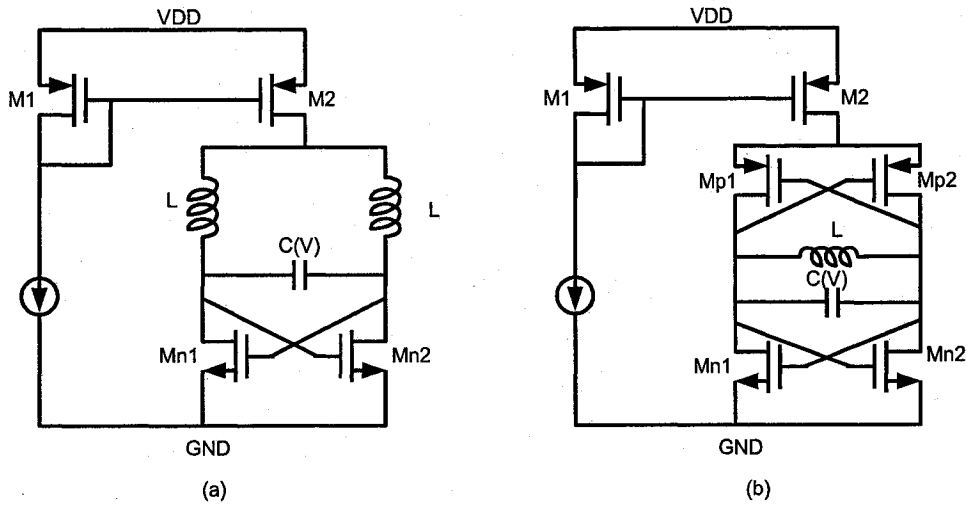


Figure 3 Oscillator topologies (a) NMOS cross-coupling oscillator (b) Complementary cross-coupling Oscillator

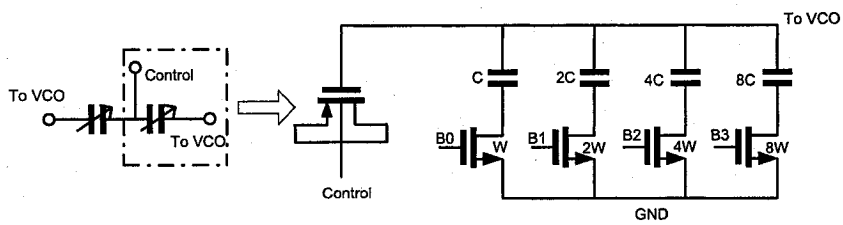


Figure 4 Binary weighted switched capacitor array with PMOS varactor

The advantages of these topologies are relatively wide tuning ranges because of the switched capacitor array. But the switched capacitor means complicated tuning control, which lowers the robustness of the circuit. Typical performance characteristics that have been achieved are presented in Table 1 below [6].

Table 1 Typical performance characteristics of Seshan's Design [6]

–Gm cross-coupling	Design Technology	f_{osc} (GHz)	f_{tune} (MHz)	Phase Noise @500KHz offset (dBc/Hz)	Phase Noise @3MHz offset (dBc/Hz)	Pd (mW)
NMOS	CMOS	2.4	452	-116	-132	11.1
CMOS	CMOS	2.4	446	-115	-132	5.6

Several other systems using similar approaches can be found in [7]-[9].

Because of their relatively good phase noise, ease of implementation, and differential operation, many researchers have focused their efforts on the implementation of -Gm LC oscillators using varactors only. (i.e. with no switched capacitor array) This is considered below.

1.1.3 Oscillators using varactors

1.1.3.1 LC tank biased –Gm LC Oscillators

-Gm LC oscillators' using varactors are classified into two categories depending upon the bias current feeding arrangement. These are: (i) LC tank biased, and (ii) current source biased. A schematic of a tank biased LC VCO is shown in Figure 5. [10].

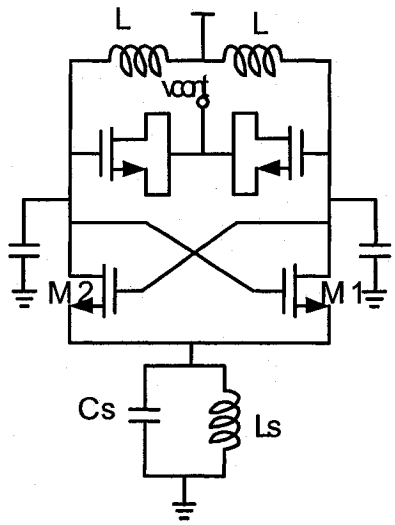


Figure 5 Tank-biased –Gm LC oscillator

This system can operate in the sub-threshold region, which also gives low power consumption.

1.1.3.2 Current source biased –Gm LC oscillators

For the current biased –Gm LC VCOs, there are two sub-categories: (i) NMOS cross-coupled pair (N-core), and (ii) the complementary NMOS-PMOS cross-coupled pair (NP-core), with either NMOS or PMOS tail current sources (Figure 6). A comparative study of these topologies on several grounds is presented below:

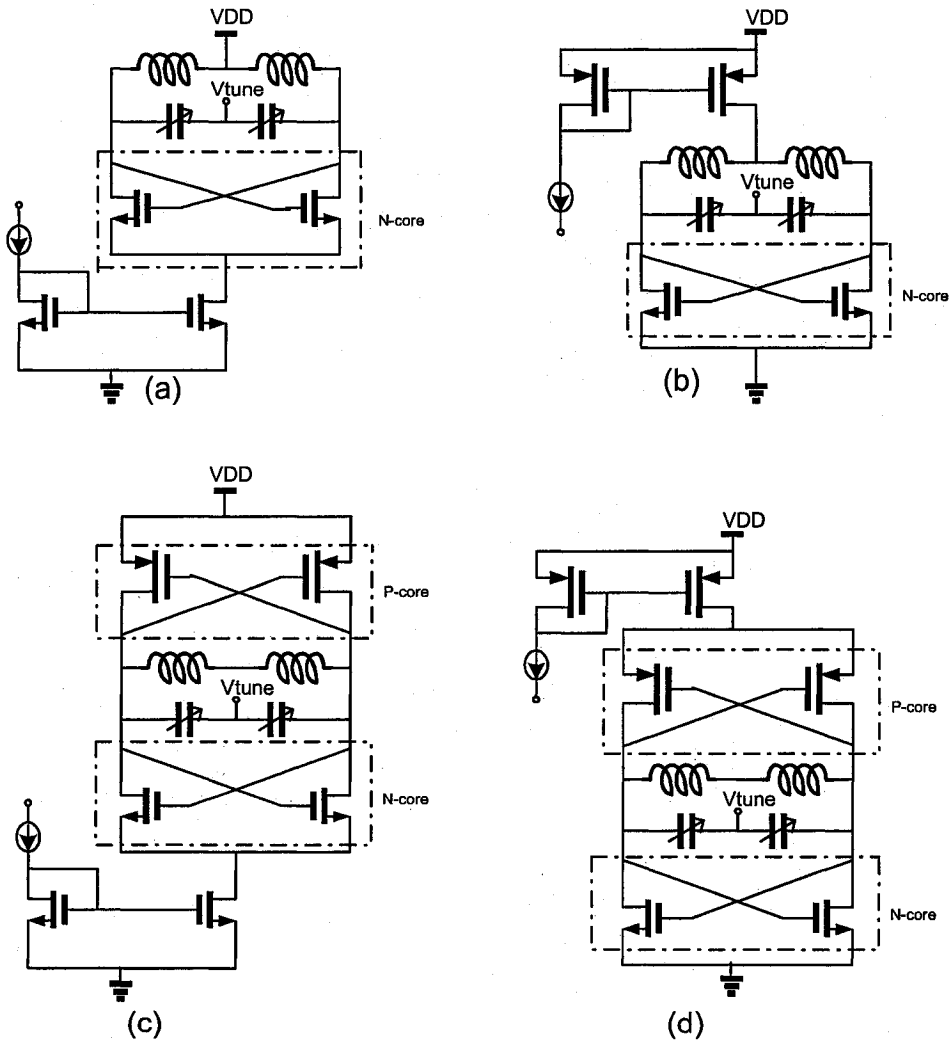


Figure 6 Differential LC VCOs: n-core with n/p-tail current source ((a), (b)); NP-core with n/p-tail current source ((c), (d))

Two modes of operation, named current- and voltage-limited regions can be identified for a typical LC oscillator considering the bias current as the independent variable. In the current-limited region, the tank voltage amplitude linearly grows with the bias current until the oscillator enters the voltage-limited region. In the voltage-limited region, the amplitude is limited by the supply voltage and/or a change in the operation mode of active devices (e.g. MOS transistors entering triode region).

As we know the IC design is always a trade-off between different merit metrics. For the typical LC oscillator, the main merit metrics should include phase noise, power consumption and tuning range.

- Phase noise perspective

For a given DC power in the current limited region, NP-core is an improvement over the N-core for two reasons: (a) it has oscillation voltage amplitude twice that of the n-core topology for a given current. (b) It can be optimized to have more symmetry in the output waveform leading to further phase noise reduction. [2] (c) It provides higher trans-conductance for a given bias current which results in faster switching of the cross-coupled differential pair. (d) It has better rise/fall time symmetry, which trends to reduce $1/f^3$ corner (the corner where flicker noise becomes dominant) frequency. However, with increasing tail-current from a low supply voltage the NP-core goes into the voltage limited region more rapidly due to reduced voltage headroom.

In addition to the tail current, the VCO core has its trade-offs. The tail current source limits the voltage swing across the tank and adds more flicker noise to the overall VCO phase noise. However, the advantage of a tail current is that it sets the bias of the differential pair making it less immune to the supply voltage variation and noise due to an

adjacent digital system on the same chip. A current source also provides a high impedance to the tank (only to even harmonics) to reduce loading of the tank by the MOSFETs.

The PMOS tail current source is better than the NMOS tail current source because of two reasons: (a) with respect to the N-core VCO, the drain terminal of the PMOS current source transistor is a high-impedance node, while the drain terminal of the NMOS current source transistor is a low-impedance node. Since the phase noise of the oscillator has a high-pass character, the PMOS tail current source is a better choice. (b) PMOS has lower flicker noise.

- Power consumption perspective

The NP-core VCO consumes less power for a given phase noise if operated in the current limited region because for the same tail current, output amplitude of the former is twice that of an N-core.

- Tuning range perspective

The N-core VCO has higher tuning range than NP-core topology for equal effective tank trans-conductance since the tail current of the N-core VCO is almost twice of that of NP-core VCO.

A drawback of the PMOS current source is the larger parasitic capacitance of the PMOS, which will result in a decrease in the available tuning range.

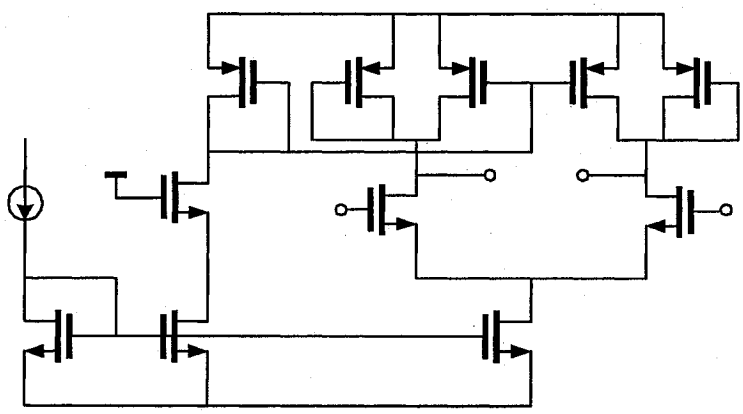
1.2 Survey on ring oscillators in CMOS technology

Ring oscillators, with their ease of integration and large tuning range, are promising candidates for the implementation of monolithic CMOS Phase Locked Loop (PLL). In

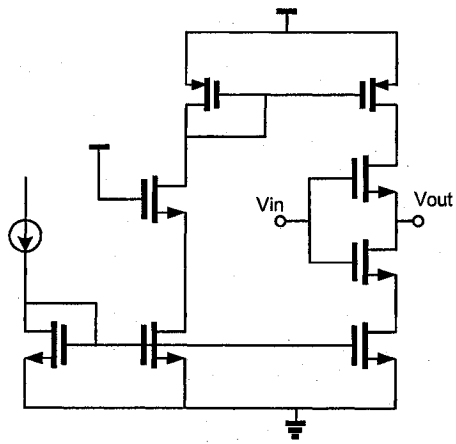
the following we present a comparison among five different delay cells used in building the ring VCO. The study was originally conducted by Dai [11].

In this comparison the oscillation frequency and the total power consumption are kept approximately equal to compare their relative noise performance. The five topologies are shown in Figures 7 (a)-(e).

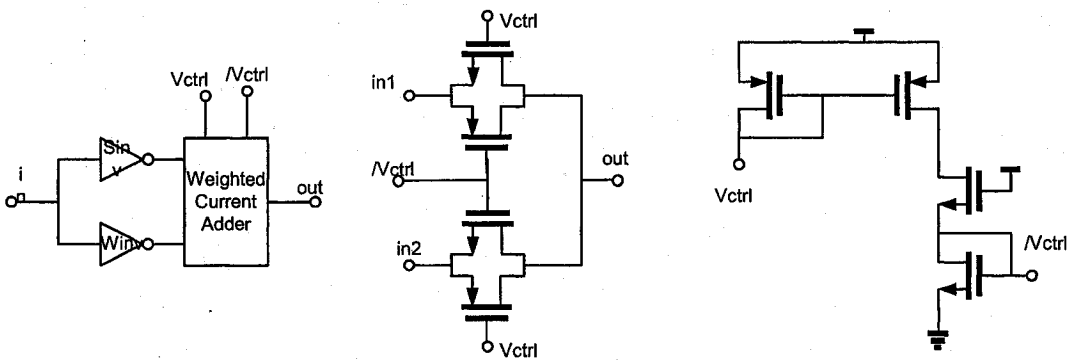
The worst single side band (SSB) phase noise performance occurs with the PMOS load in triode region (topology e). The best SSB phase noise performance is provided by Maneatis load (topology a) and the current starved system (topology b). Coupling ring (topology c) is better than PMOS load in saturation region (topology d).



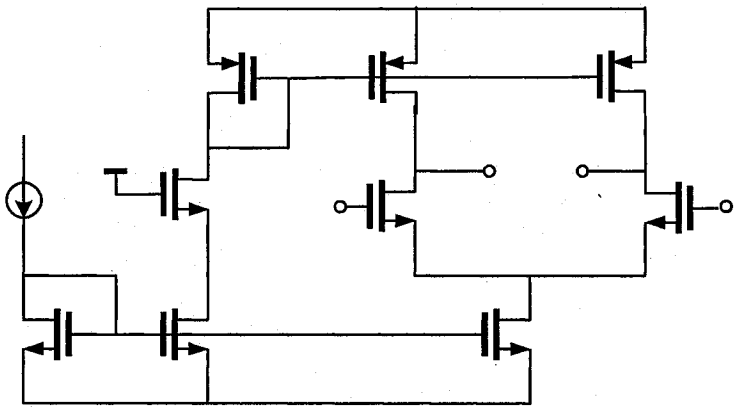
(a) Diffential invertor with Maneatis loads



(b)Current Starved invertor Oscillator



(c) coupled ring Oscillator



(d) Diffential invertor with single PMOS loads in satuartion
(e) Diffential invertor with single PMOS loads in trido

Figure 7 Five topologies of the delay cell in ring VCO

There are also many other topologies of ring oscillators using delay cells. Their performances are listed in the Table 2 [11]-[14].

A widely used figure of merit (FOM) for VCO performance is defined as [6]

$$FOM = 20\log_{10}(frequency) - Phasenoise - 10\log_{10}(Power)$$

The FOM of the VCOs studied in Ref [6] and Ref [12]-[15] are compared in Table 3.

Table 2 Performance of Ring VCOs

Design	Ref [11]	Ref [12]	Ref [13]	Ref [14]
Supply(V)	3.0	3.3	2.5	1.8
Power(mW)	30.0	79.2	15.4	19.2
f_{tune}(MHz)	750~1200	Not mentioned	661~1270	475~1000
Phase Noise @600kHz offset (dBc/Hz)	-117 f_{osc}=900MHz	-112 f_{osc}=973MHz	-105.5 f_{osc}=900MHz	-109 f_{osc}=900Mz
Technology	0.6μm	0.35μm	0.5μm	0.18μm
Number of delay cells	4	2	2	2

Table 3 FOM of VCOs

Design	Ref [6] NMOS	Ref[6] CMOS	Ref [12]	Ref [13]	Ref [14]	Ref [15]
FOM	323	325	311	303	303	305

From the extensive work by N. Seshan and L. Dai, we conclude that the LC VCO has better phase noise performance than the ring VCO.

1.3 Objective of current research

From the study above it turns out that –Gm LC-tank VCOs are better for phase noise performance while ring oscillators are much easier to be completely integrated. It would be interesting to investigate the implementation of these both kinds of oscillators and try to optimize their respective performances with respect to phase noise characteristics, power consumption, and substrate area requirement. With this viewpoint,

we can consider Table 4, which presents the specifications for the VCOs required in Bluetooth application.

Table 4 Specs of VCOs in Bluetooth application

Oscillating Frequency (GHz)	2.4
Output Swing (V)	-
Phase noise @ 500KHz offset from carrier (dBc/Hz)	-100
Phase noise @ 2MHz offset from carrier (dBc/Hz)	-110
Phase noise @ 3MHz offset from carrier (dBc/Hz)	-119
Supply Voltage (V)	-
Supply Current (A)	-
Power Consumption *(mW)	<100
Tuning range (MHz)	97

**The Power Consumption is that of the whole front-end, not only the oscillator.*

We shall attempt implementation of VCOs using –Gm LC and ring oscillator structures which will meet the above set of specifications. We shall build three VCOs based on the topologies of Figure 1.5(c), Figure 1.6 and Figure 1.7 (a). In this connection, we present in Chapter 2 some design considerations of a varactor. Chapter 3 presents the case of design consideration for an inductor. In chapter four to six, the oscillator model and the simulation results of the three topologies will be given. Post-layout simulation results will be presented. Chapter seven will include the conclusion and future direction of work.

2 The Design of Varactor

In the previous chapter, we did a review of existing oscillators and set up our goal to design three oscillators to meet the specifications in the Blue tooth application. In this chapter, we shall present the design of varactor, a component which is very important in the –Gm LC oscillators.

There are two types of controlled capacitors (Varactors) in use, namely, the MOS type and the junction type. The junction type varactor is widely used in many applications [16] [17]. The typical quality factor of a p+/nwell junction varactor is 20 or better. In recent publications, accumulation MOS (AMOS) varactor has become attractive because of its relatively large tuning range [18] - [21]. However AMOS varactors have higher sensitivity to the supply and ground noise that degrades the performance of phase noise.

2.1 MOS Capacitor

A MOS capacitor can be realized by connecting drain, source and bulk (D, S, B) connected together. The capacitance value depends on the voltage V_{BG} between bulk (B) and gate (G). In the case of a PMOS capacitor, an inversion channel with mobile holes builds up for $V_{BG}>|V_T|$, where $|V_T|$ is the sub-threshold voltage of the transistor. The condition $V_{BG} >> |V_T|$ guarantees that the MOS capacitor works in the strong inversion region, the region where the MOS device shows a transistor behavior. For some voltage $V_G>V_B$, the MOS device enters the accumulation region, where the voltage at the interface between gate oxide and semiconductor is positive and high enough to allow

electrons to move freely. Three more regions can be distinguished for intermediate values of V_{BG}: moderate inversion, weak inversion, and depletion. Figure 8 shows such regions for a PMOS capacitor.

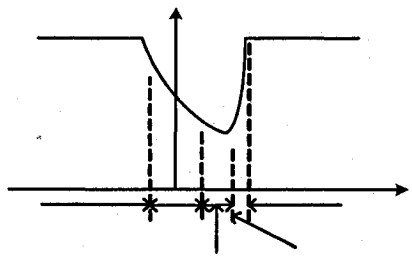


Figure 8 Tuning characteristics for the PMOS capacitor with B=S=D

2.2 AMOS varactor

AMOS varactor is similar to a PMOS except that both gate and source/drain are N+. It has three operation regions: accumulation, depletion and weak inversion. The capacitance depends on the voltage difference between gate and source/drain. The mechanism of operation of an AMOS can be understood by considering Figures 9 (a)-(c).

In Figure 9(a), since both gate and drain/source are N+, there is no chance to form a strong inversion channel, where holes can move freely. Compared to Figure 8, the C-V tuning characteristics of the AMOS varactor is monotonic, which gives the advantage to the monotonic tuning of VCO.

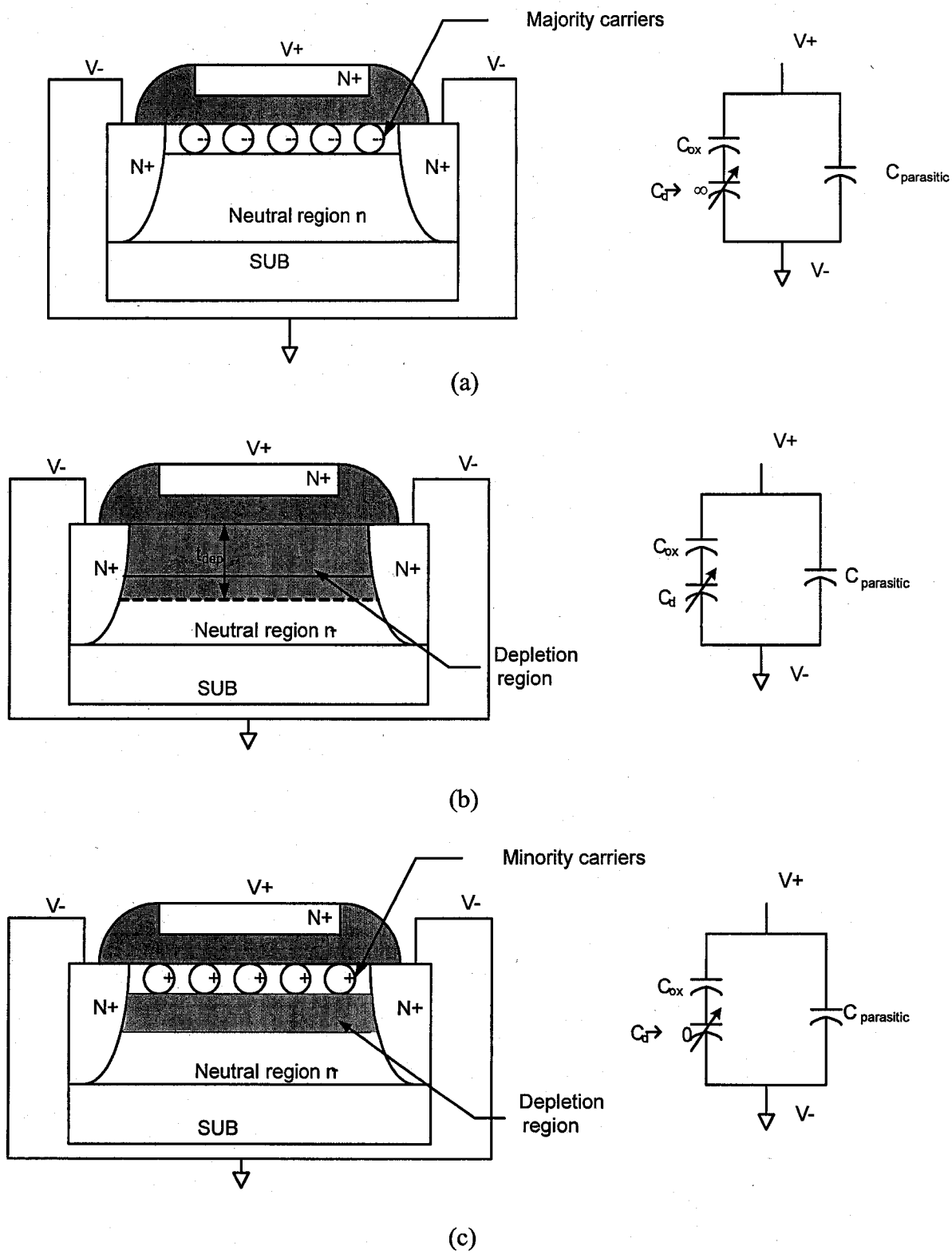


Figure 9 An AMOS varactor. Structure, operation principle and simplified model of (a) Accumulation mode, (b) depletion mode, and (c) inversion mode.

In figure 9(a), the source and drain terminals are connected together. The capacitance is formed between the gate and the substrate and is varied with the control voltage V_{SG} (= V+ - V-) being applied across the gate and the drain-source terminal.

When V_{SG} is negative, the voltage potential at the gate of the varactor is larger than that at the source. The positive charge in the gate causes accumulation in the n-well and leads to an increase in the concentration of majority carriers near the surface. As a result, the device becomes more conductive; the capacitance is mainly contributed by the oxide capacitance and becomes lager.

When V_{SG} is increased, the gate becomes more negative, and negative charge in the n-well region under the gate becomes depleted. The depletion region gets wider and depletion capacitance gets smaller as V_{SG} is increased. As this depletion capacitance is equivalently connected in series with the oxide capacitance, the effective overall capacitance becomes smaller. It is evident from Figure 9.

2.3 Implementation example of an AMOS varactor

We implemented an AMOS varactor, which is fabricated in N-well. This varactor was designed as a two-port finger structure. The size is 0.5*2*2*50*6 (L*W*S*B*G) um^2. L and W are from the same definitions of transistors. S=2 means it is used for both drain and source sides. B is the number of branches and G is the number of groups. These parameters are illustrated in Figure 10 and the actual layout is shown in Figure 11.

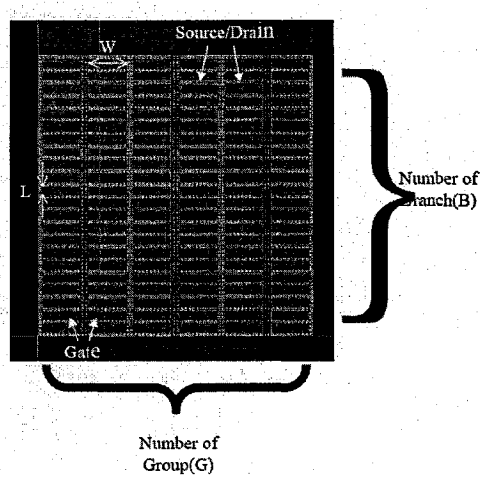


Figure 10 Illustration of the parameters in the AMOS varactor layout

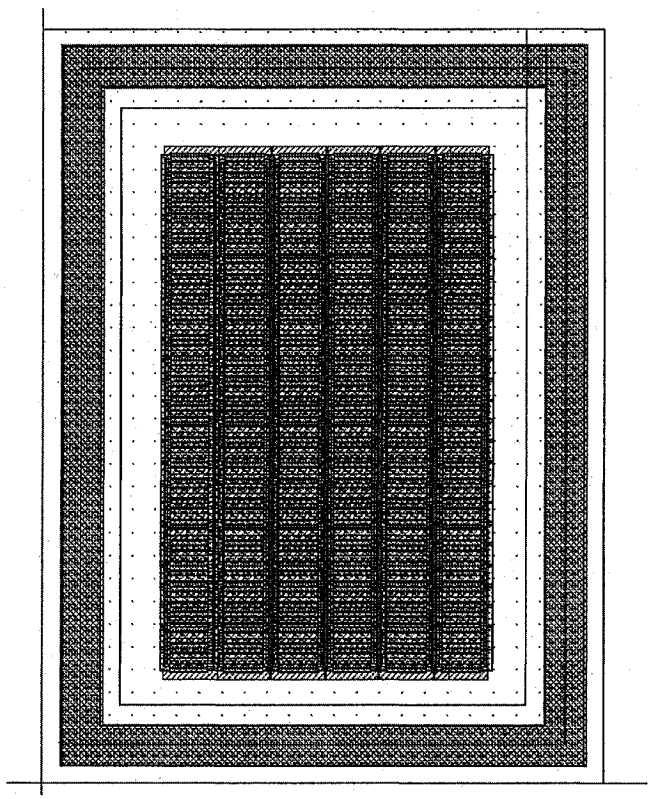


Figure 11 Layout of the varactor

After it is extracted by Cadence, we treat the varactor as a black box. Then we add an inductor and supply/current source to form a tank. The schematic of simulation is shown in Figure 12.

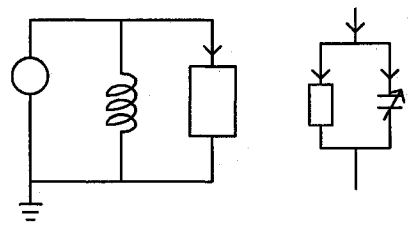


Figure 12 The simulation tank for the varactor

It is a simple LC tank. At the resonant frequency, we can get the capacitance of the varactor easily from $C = 1/(\omega_0^2 \cdot L)$

To simplify the analysis, we model the varactor as a resistance in parallel with a capacitor, which could be seen in Figure 12. The current flowing through the gate terminal of the varactor contains two parts: the real part and the imaginary part.

$$I(G) = I_g + jI_c$$

$$I_c = V \cdot \omega C$$

$$I_g = V \cdot g_v$$

We can measure the overall current through the gate terminal, which is I(G). We can calculate the imaginary part because we have gotten the value of C ($I_c = V \cdot \omega C$). So, we can get the real part, which is related to the transmittance g_v of varactor ($I_g = V \cdot g_v$). Then, after g_v is obtained, the Q factor of the varactor is given by:

$$Q = \omega CR = \frac{\omega C}{g_v}$$

As shown in Figure 13, both the oxide Capacitance C_{ox} and the depletion capacitance C_d are proportional to the gate area.

$$C_{ox} = \frac{\varepsilon_{SiO_2}\varepsilon_0}{t_{ox}} \cdot A = \frac{\varepsilon_{SiO_2}\varepsilon_0}{t_{ox}} \cdot WL$$

$$C_d = \frac{\varepsilon_{Si}\varepsilon_0}{d} \cdot A = \frac{\varepsilon_{Si}\varepsilon_0}{t_{depl}} \cdot WL$$

When $C_d \to 0$, the total capacitance equals to $C_{parasitic}$. When $C_d \to \infty$, the total capacitance equals to $C_{parasitic} + C_{ox}$. It is clear at the same gate width a larger L leads to a larger tuning range. However, when L goes larger, the resistance goes larger ($R = \rho\frac{L}{S}$). So the quality factor Q drops down.

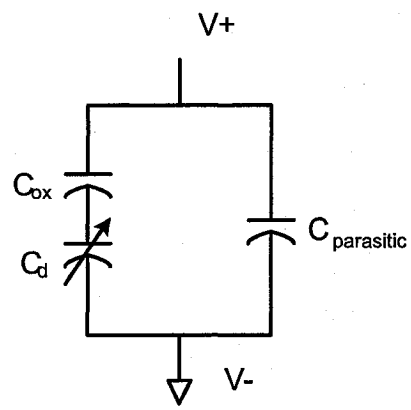


Figure 13 Capacitors in the varactor

The simulation results show that it has a tuning range of 0.36pF to 1.47pF with a tuning voltage of $\pm 1.8V$ at room temperature. The measured C-V and Q-V curve is given in Figure 14 and Figure 15. A good $C_{\max}/C_{\min}$ ratio of about 3.5 has been reported in a 0.25 μm technology with a tuning voltage of $\pm 1V$ [21].

In this application, the length of the AMOS varactor is 0.5 μm. It gives a tuning ratio of 4.1 and minimum Q of 16.

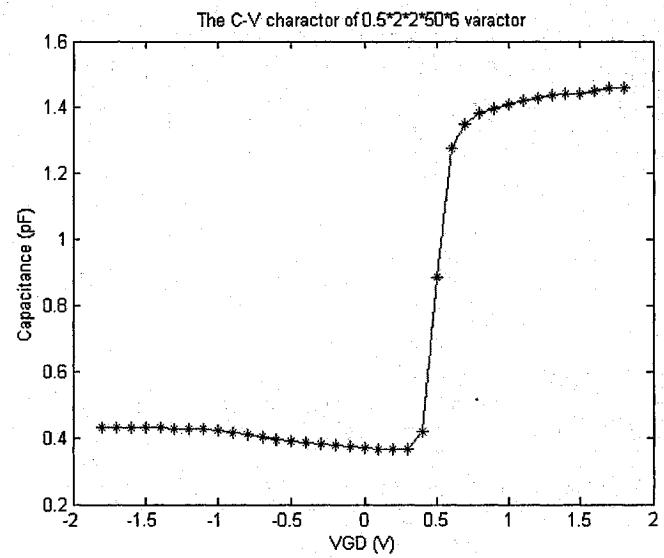


Figure 14 The C-V Characteristics of the varactor

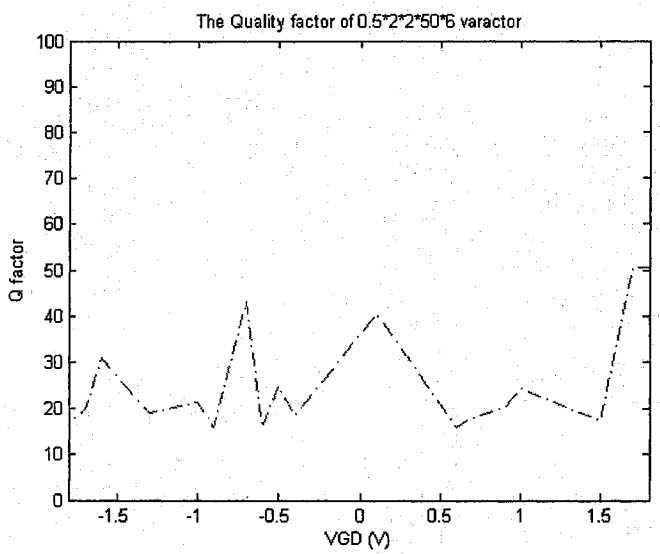


Figure 15 The Q-V Characteristics of the varactor

2.4 Characterizing the varactor

2.4.1 Modeling

In section 2.3, the varactor was depicted as a black box. We shall new briefly consider the model of a varactor. S.-S. Song's model [23] is based on physical parameters, shown in Figure 16. However using this model requires solving a very complex set of equations involving some prudent approximations. So, this may not be a preferred choice. Moreover, this model cannot be easily scaled to future technologies.

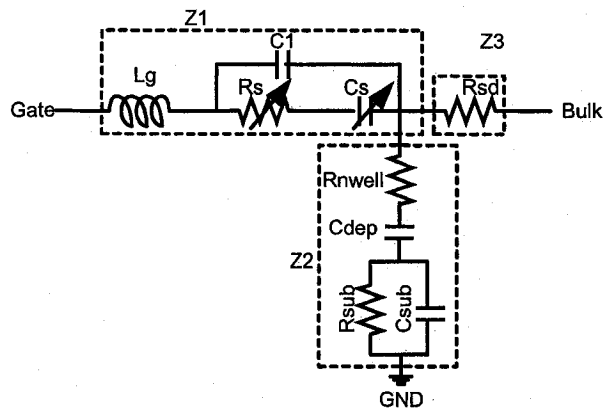


Figure 16 Varactor physical model

P. Sameni [24] proposed a modified SPICE model, which is shown in Figure 17. The equivalent circuit contains a voltage source Voffset, a capacitor Cov and a PMOS with its source and drain connected to the ground via a high impendence resistor to resemble the floating source and drain. However, in this model, the gate-source and gate-drain overlap components are neglected.

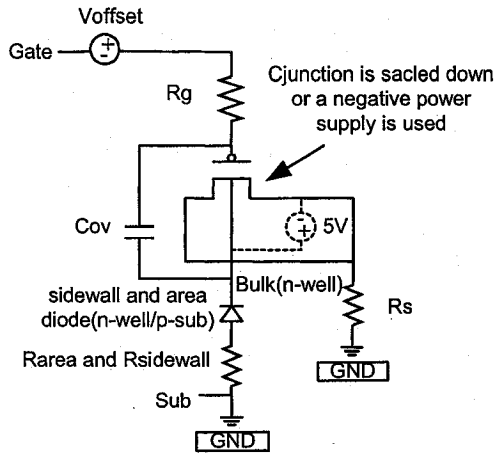


Figure 17 SPICE model developed for the varactor

K. Molnar [25] presented a BISM3v3 Model of an accumulation-mode MOS varactor. The sub-circuit is shown in Figure 18. The PMOS transistor modeled by the BSIM3v3 model together with the additional high resistances (Ro1 and Ro2) connected between S/D and SUB are responsible for C-V modeling. Depletion capacitance modeling of the n-well/p-substrate diode is done with the area (DA) and side wall (DSW) diodes. This model has been proved in 0.35μm CMOS and 0.8μm SiGe BiCMOS design kits environments of Austrian Microsystems AG. It is suitable for circuit simulator implementation. However, when new technology is evolved, new experiments must be done before we can get the values of the components.

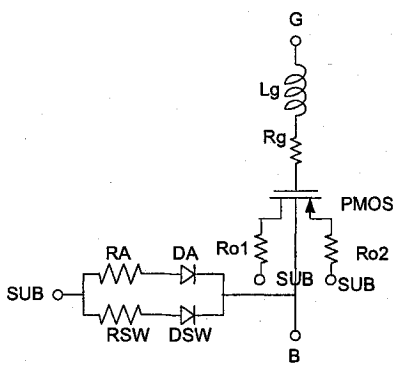


Figure 18 Subcircuit model of the accumulation-mode MOS varactor

An RF equivalent model of the varactor implemented using the 0.18-micron CMOS technology (CMOS18) provided by the CMC is shown in Figure 19 [26]. In this circuit, we lump the oxide capacitor (C_{ox} in Figure 9) and depletion capacitor (C_d in Figure 9) into C_{gate} to model the behavior of voltage dependent capacitance. R_{gate}, L_{gate}, R_s and L_s are the parasitic components associated with the electrodes. R_{ch} and C_{ov} are used to fit the channel resistance and overlap capacitance. R_{sub} and C_{sub} are used to model the parasitic effects due to substrate. We need this model for the AMOS varactor discussed in section 2.3. The simulated S-parameter of the varactor at V_G= 1.8 V is shown in Figure 20.

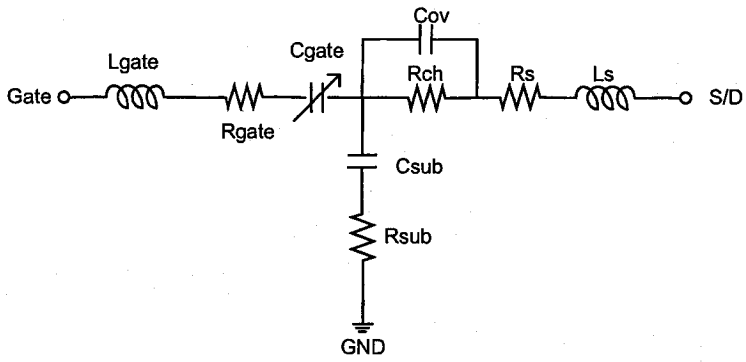


Figure 19 The RF equivalent model of varactor

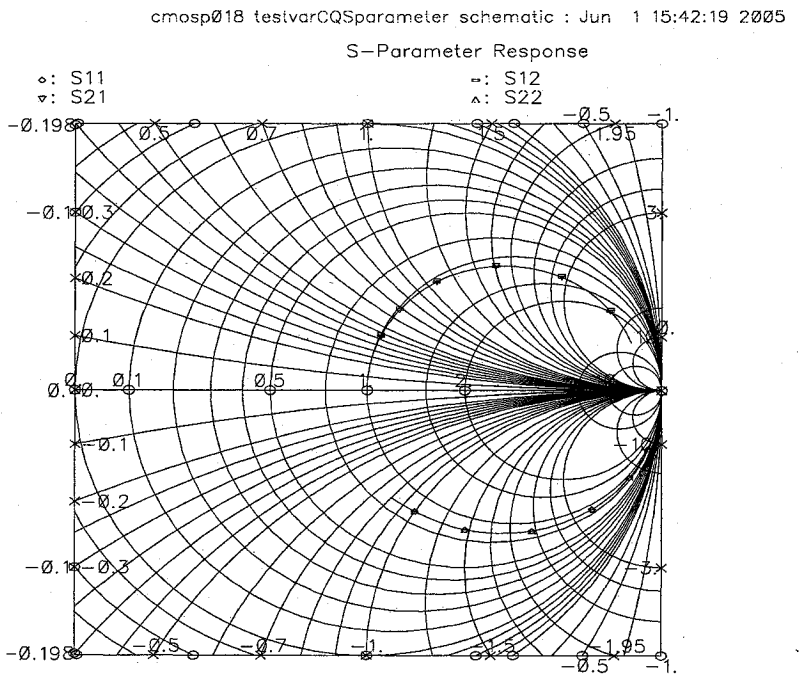


Figure 20 The simulated S parameter of the MOS varactor

Optimization, the automatic generation of the model parameters and component values from a given set of electrical specifications or measured data, is available in Hspice. With a user-defined optimization program and a known circuit topology, Hspice automatically selects the design components and model parameters to meet DC, AC and transient electrical specifications.

Using the optimal function of HSPICE, we can get the parameters of the designed varactor in section 2.3 shown in table 5.

Table 5 Parameters of the varactor

L_{gate}(H)	36.6E-12	C_{sub}(F)	30.2E-15	C_{gate}(F)	1.45E-12
R_{gate}(Ω)	0.7947	R_{sub}(Ω)	21.1820	C_{ov}(F)	147.5E-12
R_{ch}(Ω)	1.4703	R_s(Ω)	0.7906	L_s(H)	19.3E-12

All the models above use small-signal definition, where the varactor is specified by its small-signal capacitance C_{ss} versus V_c. If the signal swing across these devices is large (as would be the case in a VCO tank circuit), then the instantaneous value of the capacitance changes throughout the signal period. The effective capacitance seen by the large signal will be a weighted average of the small-signal capacitance over a single period. Because of this averaging effect, the oscillator RF output frequency versus tuning voltage curve and the dc/small-signal C-V curve will not be equivalent [27] [28]. One equation on the effective capacitance C_{eff} which sets the frequency of oscillation is obtained from [27].

$$C_{eff} = \frac{1}{2}(C_{max} + C_{min}) + \frac{1}{\pi}(C_{min} - C_{max})\left[\sin^{-1}\frac{V_{eff}}{A} + \frac{V_{eff}}{A}\sqrt{1-\left(\frac{V_{eff}}{A}\right)^2}\right]$$

where $V_{eff} = V_G - V_C - V_T$ is the effective control voltage of the varactor. A is defined as the amplitude of the oscillation and it is always larger than V_{eff}.

2.4.2 AM to PM conversion

An undesirable side effect associated with a varactor is that its effective capacitance depends not only on control voltage, but also on the amplitude of the oscillation. Since amplitude fluctuations can modulate the effective capacitance of a varactor, AM noise changes to FM noise. FM noise is indistinguishable from phase noise. A limiter, which

can suppress AM noise, cannot suppress either phase noise or FM noise. This problem must be solved with the right varactor, which does not strongly convert AM into FM.

There are two other ways that varactor can introduce FM noise. The first is through noise on the control voltage V_c and the second is through noise on the power supply. However, the AM-FM conversion in the varactor is seldom the main source of phase noise in most well-designed oscillators.

2.5 Summary

In this chapter, the concept, layout and characterization of the AMOS varactor are discussed. The relationship between the phase noise performance and the varactor characteristic is also introduced. The more the C-V curve of a varactor departs from linearity, the more it converts low-frequency noise into phase noise. The C-V curve may be linearized by connecting a fixed capacitor either in series or in parallel with the varactor. Series connection [29] achieves linearization at the cost of tuning range while parallel connection [7] [30] requires more control signal of VCO.

3 The design of inductor

In the previous chapter, the design and characterization of varactors have been discussed. In the LC-based oscillators, another important passive component is the inductor.

Spiral inductance on silicon is critical in the VCO design. Since the spiral inductor suffers from both ohmic losses in metal and substrate losses due to the conductive silicon, this component typically exhibits low quality factor (Q). At the same time, inductor is the most expensive component because of its excessive area consumption. People have made a lot of effort trying to improve its performance like shielding, using multi-layers metal and substrate removing if applicable.

After the inductor is laid out, we need to analyze and characterize its behavior. Many researchers have contributed to work in this direction. The most widely used model has been the lumped-element model. C.P. Yue et al [31] proposed the symmetric model in 1996 and A.M. Niknejad [32] et al proposed a more accurate non-symmetric model in 1998. However they are all narrowband models. In our case, it is not suitable because of the wide tuning range of the VCO. In this chapter, wide band model will be introduced. Also the simulation tool ASITIC (Analysis and Simulation of spiral Inductors and Transformers for ICs) will be discussed.

3.1 Layout Considerations of the inductor

3.1.1 Substrate losses

Substrate losses are the most important factors degrading the performance of an on-chip inductor. A major source of substrate losses is the capacitive coupling that allows

conduction current flow not only through the metal strip but also through the silicon substrate. Another important source of substrate losses is the inductive coupling. In some technologies, the substrate could be removed. In this case, the quality factor could be improved largely from 3.5(at 1.25GHz) to about 20 (at 5GHz) [33].

In standard silicon technologies where substrate cannot be removed, ground shielding is an effective approach. The use of a patterned ground shielding between inductor metal strips and substrate increases the quality factor by reducing the serial resistance of substrate while not inducing significant eddy current. The patterned shields are tied together using a metal connection. It is reported the Q is improved by 25% using shielding [34].

3.1.2 Metal losses

An accurate analysis of the metal losses should take into account of both conductive losses and magnetically introduced losses. In the recent years, two-layer metals have been used in the spiral inductors. These two metal layers are connected together with VIAs so that the serial resistance of the inductor is reduced by almost 50%. Thus, the quality factor (Q) can be improved by almost two times of that of one-layer metal inductor. Another approach to reduce the magnetically introduced losses is to use variable metal width. Craninckx et al [35] has proposed that the inner turn of the spiral metal line should be narrower than the outer turn. Q factors higher than 40 are predicted for a 20-nH inductor working at 3.5GHz which is up to 60% better [33] than the best result for a single metal-width layer inductor with uniform width.

3.2 Simulation tool—ASITIC

ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for ICs) is a CAD software developed by Ali M. Niknejad, University of California at Berkeley. It can design, analyze, and model the electrical and magnetic behavior of passive metal structures residing above a lossy conductive substrate. ASITIC works with a mini technology file that describes the substrate and metal layers of the process. In CMOSP18 technology, the technology file (See appendix A) can be found in the CMC design kits. The commands which are often used are introduced below.

- Spiral: Create a polygon spiral of specified dimensions and place the spiral in memory.

E.g.: SP NAME=X: RADIUS=100: SIDES=32: W=8: S=3: N=5: METAL=M3: XORG=150: YORG=150

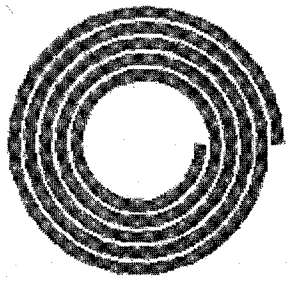


Figure 21 non-symmetric inductor

Name: NAME -- The unique name of the spiral.

Radius: RADIUS -- The radius of the spiral measured from the center of the spiral to the outer edge of the spiral. The value of the radius is the smallest circle that contains the spiral.

Number of Sides: SIDES -- The number of sides to use. For 4 sides use the square command. SIDES can take on any value and for SIDES > 64 the structure will approach a circular structure.

Metal Width: W -- The metal trace width in microns.

Spacing: S -- The spacing from metal edge to metal edge.

Turns: N -- The number of spiral turns. Fractional amounts divisible by 1/SIDES can be used to specify partial turns.

Metal Layer: METAL -- The metal layer to use to wind the spiral.

Origin of Spiral: XORG: YORG -- The physical origin of the spiral relative to the lower left hand corner of the chip. The origin of the spiral is the middle of the spiral. Do not place the spiral outside of the chip boundary, and avoid abutting the spiral against the chip boundaries.

- Sympoly: Create a polygon symmetric spiral of specified dimensions and place the spiral in memory.

E.g.: SYMPOLY NAME=D: RAD=80: W=10: S=4: ILEN=14: N=5: METAL=M3:METAL2=M2: XORG=200: YORG=200

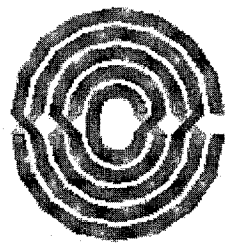


Figure 22 Symmetric inductor

The explanation of arguments is similar to that before.

- 2portx: Calculate the 2-Port Parameters of a Spiral

2PortX (<spiral> <spiral gnd> <freq1> <freq2> <fstep> <S|Y|Z|PI> <polar=true|false> <fast=false|true> <filename>)

Aliases: 2portx, twoportx, 2px

Arguments:

<spiral>: name of the spiral

<spiral gnd>: grounding structure (set equal to <spiral> for none)

<freq 1>: frequency of analysis

(<freq2> <fstep>): frequency range of analysis

(S|Y|Z|PI): two-port format in S, Y, Z, or PI-Parameters (default S)

(polar|rect): polar format or real/imag format (default polar)

<filename>: store results in this file

- Pi: Calculate an Equivalent Pi Circuit Using 2-Port Analysis

Pi (<spiral> <freq>)

Aliases: pi, pimodel, picircuit, pieq

Summary: Calculate the equivalent Pi circuit of a spiral at a single frequency.

The Pi parameters are equivalent to the 2-port parameters of the spiral at any frequency. The calculation is performed by calculating an approximate 2-port representation for each segment of the spiral and cascading the 2-ports for each segment. The final 2-port representation is converted into the Pi form. The translation is one-to-one and thus unique. The quality factor Q is also reported with three numbers representing the input, output, and differential quality factors.

There are many approximations in the Pi command and thus this command executes very quickly and forms the backbone of many of the optimization commands. The main assumption is that each segment can be considered as a 2-port and thus all interactions with other segments are lumped into a 2-port model. The substrate loss calculation is also approximate. The inductance computation ignores the substrate and thus magnetic and conductive effects of the substrate are neglected. Finally, the skin-effect is calculated in an approximate manner and proximity-effects of nearby conductors is thus neglected.

```
Pi Model at f=2.4 GHz:  Q = 5.283 , 5.799 , 8.706
L = 4.262 nH R = 3.917
Cs1 = 237.2 fF Rs1 = 143.6
Cs2 = 217.4 fF Rs2 = 144.1      Est. Resonance = 5.006 GHz
```

- ## Pix: Calculate an Equivalent Pi Circuit Using EM Analysis

PiX (<spiral> <freq> <spiral gnd>)

Aliases: pix, pimodelx, picircuitx, pieqx

This command calculates the 2-port parameters of a spiral structure using electromagnetic analysis. There is no limitation on the structure of the spiral and thus the spiral can be an arbitrary interconnection (shunt or series) of metal segments. There is an quasi-static assumption which limits the highest frequency of analysis but usually this frequency is well beyond the self-resonant frequency of the inductor.

The routine works as follows. First, the partial inductance matrix is calculated for the structure by dividing each segment by length, thickness, and width and calculating the self and mutual inductance between every pair of sub-segments. The partitioning of segments is controlled by the various cell size environmental variables. The partial inductance matrix is reduced in order and lumped into a segment to segment partial inductance matrix. The partial inductance matrix is calculated in free air and thus any magnetic or conductive properties of the substrate are ignored. This is usually a good assumption for substrates on the order of 1 Ohm-cm or more resistive. If eddy is enabled, for highly conductive substrates, eddy currents in the substrate give rise to reflected losses and this is included in the calculation for Manhattan geometries. Reduction in inductance due to ground currents is not included in this calculation.

Next the capacitance matrix is calculated by dividing up segments in width and length only. The thickness of segments is assumed to be small enough so that charge density does not vary significantly over the thickness of the conductor. This assumption is valid form most thin IC metal layers but will result in errors for very thick metal. The partitioning is now controlled by the autocell and/or cmaxl environmental variables. The 3-D capacitance matrix is calculated using the Green function which includes the lossy and coupling effects of the substrate.

The substrate back-plane is assumed to be grounded. This assumption can be removed by employing a non-conductive layer as the first layer in the technology file. This could model epoxy glue or other dielectric materials. Then <spiral gnd> should consists of an interconnection of metals that ground the substrate. For instance, <spiral gnd> might consists of a substrate tap only, a conducting wire touching the substrate. Otherwise <spiral gnd> may consist of a ring of substrate contacts surrounding the inductor. Even metal pads can be included in the calculation. A further application

<spiral gnd> is to simulate the electrical effects of a shield. A solid metal layer placed below the spiral can model the shielding effects and the potential gains in Q.

Finally the partial inductance and capacitance matrix are used to solve for the 2-port parameters of the device.

Note: A solid shield is included in the capacitance matrix calculation but it is ignored by the inductance matrix calculation. Thus in reality you must pattern the shield to avoid eddy current effects in the shield. Also, even a patterned shield cannot prevent eddy current effects from occurring in the substrate and thus the Q factor reported by ASITIC might be optimistic if the substrate conductivity is high (below 1 ohm-cm) and eddy is not enabled.

In my thesis, I need three on-chip inductors. They will be seen in the final layout in Chapter 6.

3.3 Characterizing the inductor

The lumped-element non-symmetric model used by ASTIC [32] is shown in Figure 23 below. The spiral coil itself is modeled by an ideal inductance L_s, a series resistance R_s, representing the ohmic losses in the coil, and an inter-wire capacitance C_{br}. C_{p1}, C_{p2}, R_{p1}, R_{p2} are parasitic components through which the RF signal leaks into the substrate.

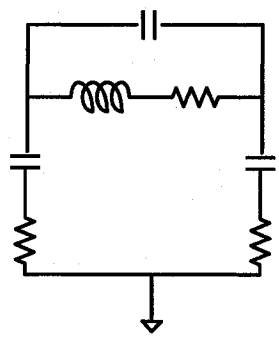


Figure 23 non-symmetric model of the on-chip inductor

However this model cannot characterize the increase in Rs with frequency. Some researchers [36]-[37] used frequency-dependent elements to model this effect, but frequency-dependent elements are difficult to simulate in SPICE. In order to overcome this difficulty, some researchers use frequency-independent models to characterize this

effect [38] [39]. However, these models cannot predict the drop-down characteristics of R_s at higher frequency. Or they are much too complicated. A simple wide-band inductor model has been reported by J.Goilet al. [40].

ASITIC cannot provide a wide-band model of inductor. However, we can use 2portx command to calculate the 2-port parameters (s or y or whatever is most appropriate). Then we select a circuit representation of the 2-port network. Next, we can create a SPICE deck representing the 2-port and use HSPICE or MATLAB program to fit the circuit parameters to the calculated *s*-parameters.

The model we used is based on Goilet's model. However, some simplification has been made. Its shown in Figure 24. In this model, C_{ox} represents the oxide capacitance between the inductor and the substrate. R_{si} and C_{si} are the substrate resistance and capacitance to ground, respectively. The series capacitance C_{br} models the capacitive coupling between the two ports of the inductor. As mentioned above, R_s increases due to skin effect as frequency increases. As the frequency reaches the frequency where Q is maximum, Rs drops. This is because of the coupling through the silicon substrate; known as lateral substrate coupling [40]. It is modeled by C_{sub} and R_{sub}. The HSPICE file can be found in appendix B.

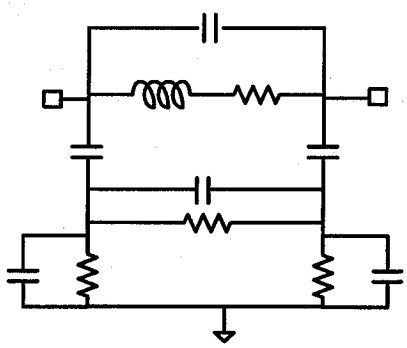


Figure 24 broad-band model of the on-chip inductor

3.4 Summary

In this chapter, some aspects of the inductor design have been highlighted. The challenges in the design, layout optimization, and characterization have been discussed. Use of some simulation tools has been cited. A new modeling technique has been introduced.

Since the performance of the inductor is highly technology-dependent, it is very important to read the design rules provided by the foundry before design. Some parameters, such as allowed angles of metals and minimum space between metals are critical in design.

4 The Design of the CMOS LC VCO

In the previous chapters, we presented the design of varactors and inductors, which are passive components in the LC VCO. In this chapter, we shall address the design of LC VCO.

In this chapter, we shall focus on the oscillation model of the complementary LC VCO, and the critical design parameters related to the phase noise performance. We shall see how the design parameters are set based on theoretical analysis. Both schematic level simulation results and post-layout simulation results will be provided.

As introduced in chapter 1, the complementary cross-coupled differential structure is widely used in many applications [45]-[49] At a given current, the PMOS pair and NMOS pair together provide larger negative trans-conductance than only PMOS pair or NMOS pair. Also because of its complementarities, it consumes less power and has a faster transition. Its schematic and equivalent circuit models are shown in Figure 25. We shall consider this arrangement to illustrate the design calculations pertaining to this class of Oscillator.

In Figure 25, the broken line represents the common mode or ground. C_{NMOS} and C_{PMOS} are the total parasitic capacitances of the NMOS and PMOS transistors, respectively. g_m and g_0 are small-signal transconductance and output conductance of the transistors, respectively. To facilitate the analysis of the tank, simple models of the varactor and inductor are used. The varactor is represented by a capacitor C_v in series with a resistor R_v. The symmetric model of the inductor is used.

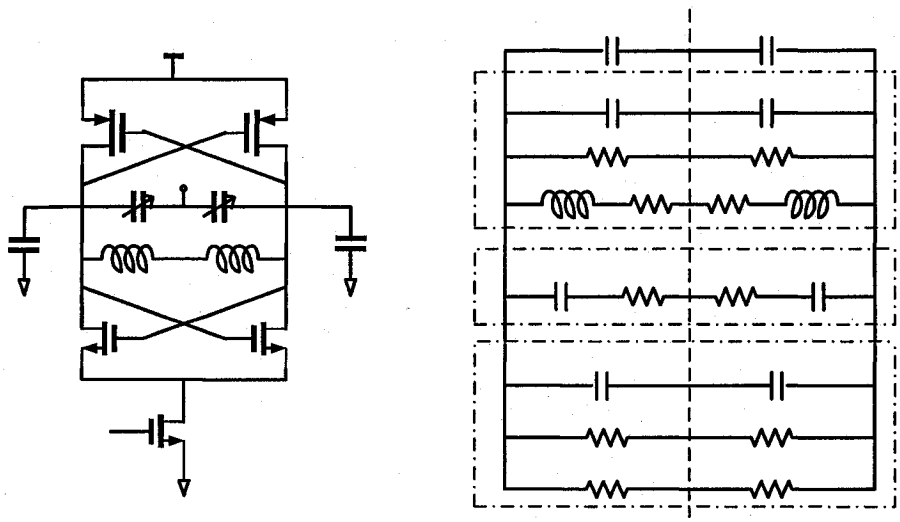


Figure 25 a typical LC Oscillator and its equivalent oscillation model

4.1 Theoretical analysis

4.1.1 4.1.1 Oscillating frequency and gain of VCO

It's well known that for an LC tank, the oscillation frequency is given by $\omega = \frac{1}{\sqrt{LC}}$. However, as illustrated in chapter 2, the instantaneous value of the capacitance changes throughout the signal period if the signal swing across the device is large. So the oscillation frequency of the LC VCO is given by $\omega = \frac{1}{\sqrt{LC_{eff}}}$ [50]

$$\text{Where } C_{eff} = \frac{1}{2}(C_{\max} + C_{\min}) + \frac{1}{\pi}(C_{\min} - C_{\max})\left[\sin^{-1}\frac{V_{eff}}{A} + \frac{V_{eff}}{A}\sqrt{1-\left(\frac{V_{eff}}{A}\right)^2}\right] \quad (4.1)$$

And $V_{eff} = V_G - V_C - V_T$ is the effective control voltage of the varactor. A is defined as the amplitude of the oscillation.

The gain of the VCO is defined as its frequency change $\partial\omega$ as of control voltage change ∂V_C. That is:

$$K_{VCO} = \frac{\partial \omega}{\partial V_C} = -\frac{\partial}{\partial V_{eff}} \frac{1}{\sqrt{LC_{eff}}} = \frac{1}{2} \frac{\omega}{V_{eff}} \frac{\partial C_{eff}}{\partial V_{eff}}$$

$$K_{VCO} = \frac{C_{\min} - C_{\max}}{A\pi} \frac{\omega}{V_{eff}} \sqrt{1 - \left(\frac{V_{eff}}{A}\right)^2} = \frac{C_{\min} - C_{\max}}{A\pi} \frac{1}{V_{eff}\sqrt{LC_{eff}}} \sqrt{1 - \left(\frac{V_{eff}}{A}\right)^2}$$

$$= \frac{C_{\min} - C_{\max}}{\pi\sqrt{L}AV_{eff}} \frac{\sqrt{1 - \left(\frac{V_{eff}}{A}\right)^2}}{\sqrt{\frac{1}{2}(C_{\max} + C_{\min}) + \frac{C_{\min} - C_{\max}}{\pi}\left(\sin^{-1}\frac{V_{eff}}{A} + \frac{V_{eff}}{A}\sqrt{1 - \left(\frac{V_{eff}}{A}\right)^2}\right)}}$$

In chapter 2, we have discovered that the capacitance of the varactor is an increasing function of control voltage. Here, we can explore more on the relationships between the effective capacitance and the effective control voltage or the amplitude. Figure 26 shows the effective capacitance of the varactor is a decreasing function of the effective control voltage, which agrees with the result in chapter 2. Figure 27 shows the effective capacitance is an increasing function of the tank amplitude.

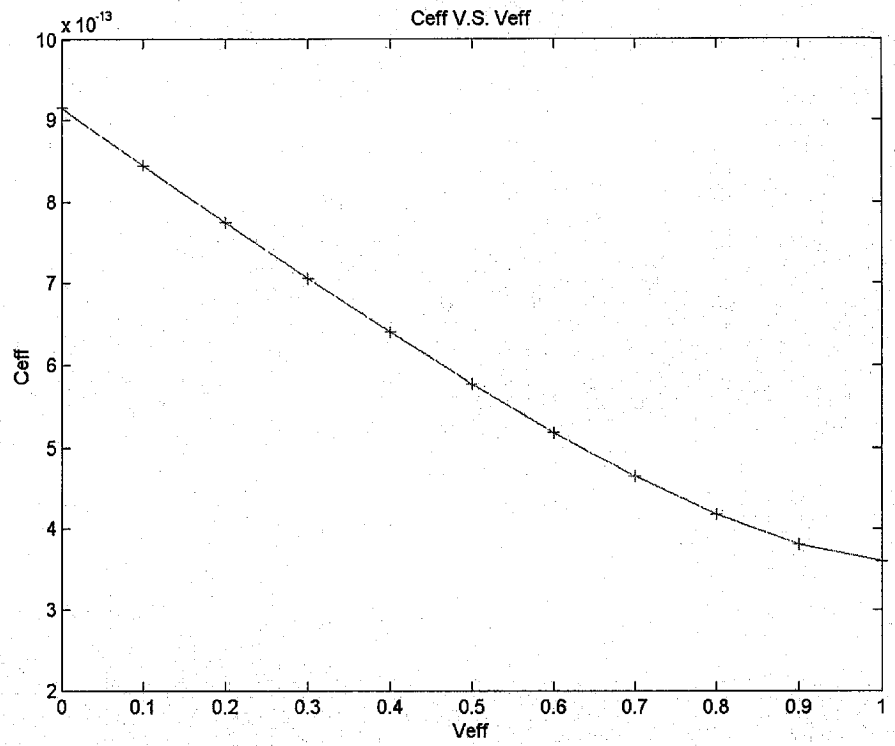


Figure 26 the function of the effective capacitance and the effective control voltage

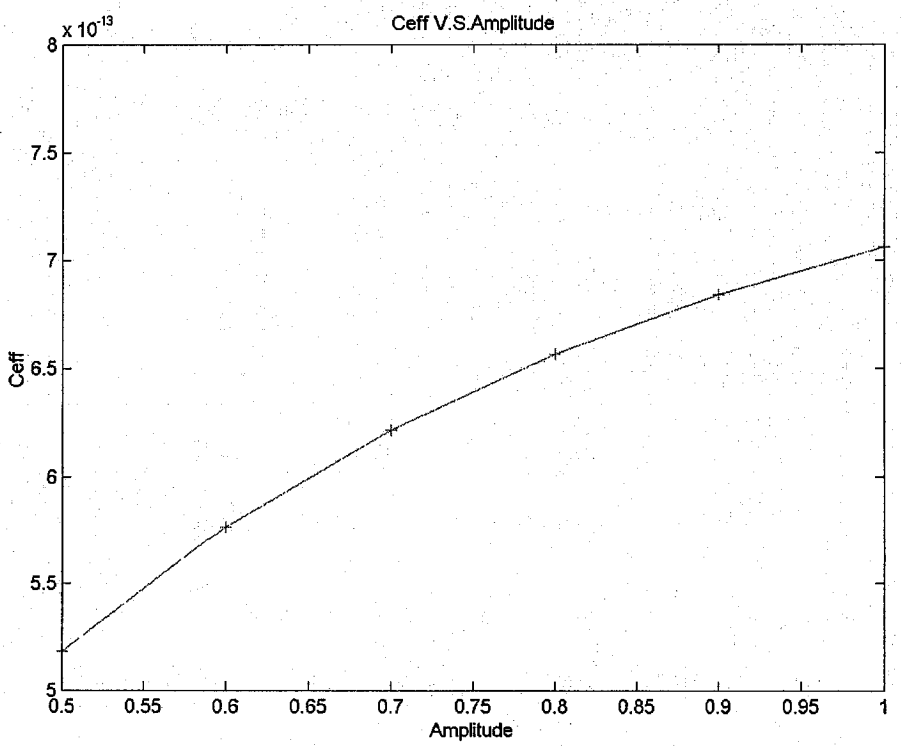


Figure 27 the function of the effective capacitance and the tank amplitude

In Figure 26, the tank amplitude is set to be 1V. And in Figure 27, the effective control voltage is set to be 0.3V.

Since $\frac{\partial K_{VCO}}{\partial V_{eff}}$ ***exits and*** $\frac{\partial K_{VCO}}{\partial V_{eff}} > 0$, K_{VCO} ***is an increasing function of*** V_{eff}.

Similarly, Since $\frac{\partial K_{VCO}}{\partial A}$ ***exits and*** $\frac{\partial K_{VCO}}{\partial A} > 0$, K_{VCO} ***is an increasing function of A.***

Using Matlab, the relationship between K_{VCO} and V_{eff} or A is shown in Figure 28 and 29. Same as Figure 26 and Figure 27, the tank amplitude and effective control voltage are set to be 1V and 0.3V, separately.

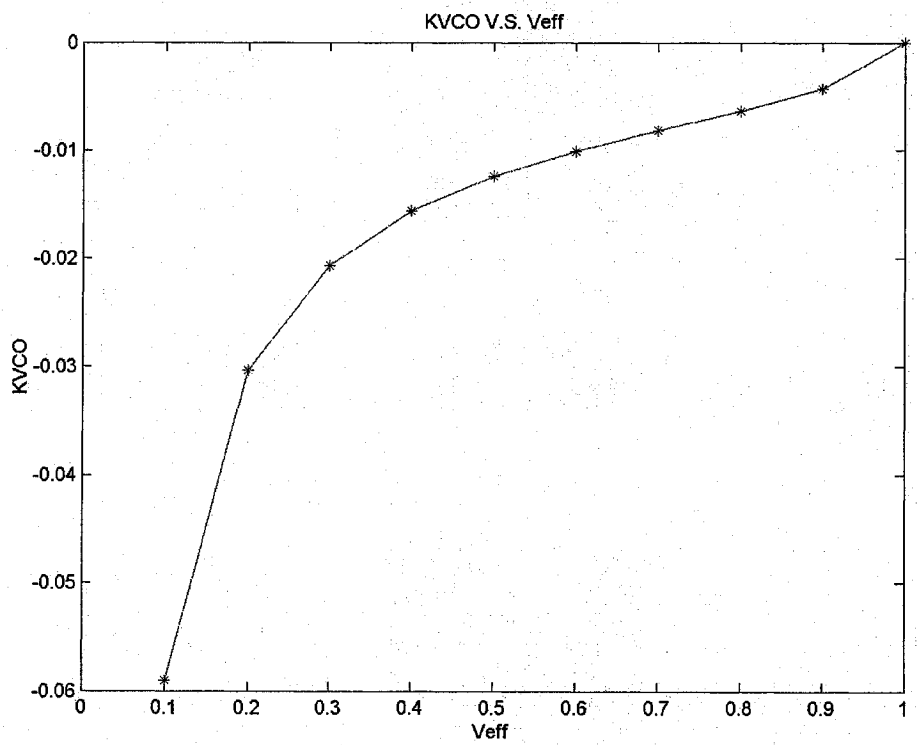


Figure 28 the function of the gain of the VCO and the effective control voltage

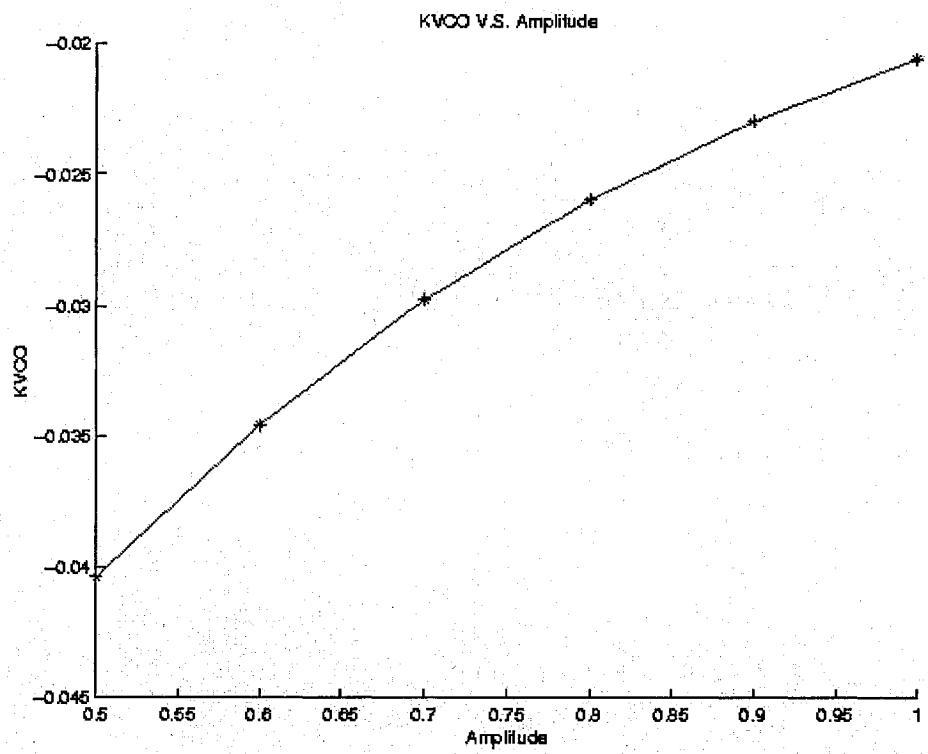


Figure 29 the function of the gain of the VCO and the tank amplitude

4.1.2 Phase Noise Performance

Noise sources in the circuit can be divided into two groups, namely, device noise and interference. Thermal, shot, and flicker noise are examples of the former, while substrate and supply noise are in the latter group. A typical VCO phase noise is shown in Figure 30. [51] In the $1/f^3$ region, the frequency modulated flicker noise is dominant and in the $1/f^2$ region, the thermal noise is dominant. By making the output waveform symmetric, the $1/f^3$ corner can be very small (about 50 KHz). For the VCO in the communication systems, the phase noise of interest is at least 600 KHz away from the carrier frequency. It falls in the $1/f^2$ region.

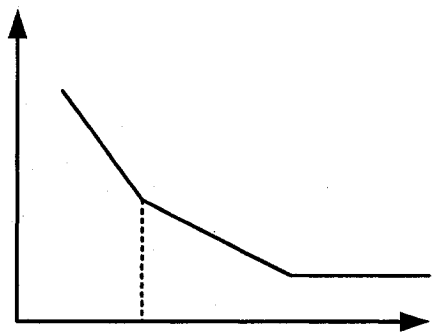


Figure 30 Typical plot of the phase noise of an oscillator versus offset from carrier frequency

In the $1/f^2$ region, phase noise is given by [47]

$$L\{\Delta f\} = \frac{1}{8\pi^2 \Delta f^2} \cdot \frac{1}{q_{\max}^{\ 2}} \cdot \sum_n \left(\frac{\overline{i_n^{\ 2}}}{\Delta f} \cdot \Gamma_{rms,n}^{\ 2} \right) \text{(dBc/Hz)}$$

(4.2)

Δf is the offset frequency from the center frequency, and q_{max} is the total charge swing of the tank. The impulse sensitivity function (ISF), Γ represents the time-varying sensitivity of the oscillator's phase to perturbations. For an ideal sinusoidal waveform, $\Gamma_{rms} = 1/\sqrt{2}$. $\frac{\overline{i_n^{\ 2}}}{\Delta f}$ is the equivalent differential noise power spectral density [52], [53] [54].

For the varactor, $\frac{\overline{i_v^{\ 2}}}{\Delta f} = 2kT \cdot g_v$ (4.3)

For the inductor, $\frac{\overline{i_L^{\ 2}}}{\Delta f} = 2kT \cdot g_L$ (4.4)

For the transistor, $\frac{\overline{i_n^{\ 2}}}{\Delta f} \geq 2kT\gamma(g_{d0,n} + g_{d0,p})$ (4.5)

Where $\gamma \sim 2/3$ for long-channel transistors and $\gamma \sim 2.5$ for short-channel transistors. g_{d0} is the channel conductance at zero V_{DS} (the voltage across the drain and source of the transistor) and equals to g_m for long-channel transistors and $2I_{drain}/(L_{channel}E_{sat})$ for short-channel transistors which is larger than g_m.

The frequently appearing parameters in our optimization process are the tank loss g_{tank}, effective negative conductance $-g_{active}$, tank inductance L_{tank}, and tank capacitance C_{tank} of Figure 25, given by:

$$\begin{aligned}
2g_{tank} &= g_{on} + g_{op} + g_v + g_L \\
2g_{active} &= g_{mn} + g_{mp} \\
L_{tank} &= 2L \\
2C_{tank} &= C_{PMOS} + C_{NMOS} + C_L + C_v + C_{load} \\
g_L &= 1/R_p + R_s/(L\omega)^2 \\
g_v &= (C_v\omega)/Qv \\
C_{NMOS} &= C_{gs,n} + C_{db,n} + 4C_{gd,n} \\
C_{PMOS} &= C_{gs,p} + C_{db,n} + 4C_{gd,p}
\end{aligned} \tag{4.6}$$

To meet the startup condition, we need

$$g_{active} > \alpha_{\min} g_{tank,\max} \tag{4.7}$$

That is: $g_{m,n} + g_{m,p} > \alpha_{\min}(g_v + g_L)$. (4.8)

α_{min} is the small-signal loop gain, which is always bigger than 2.

Because $g_{d0} \geq g_m$, we can get

$$(g_{d0,n} + g_{d0,p}) \geq (g_{m,n} + g_{m,p}) > \alpha_{\min}(g_v + g_L) \tag{4.9}$$

Combining (4.3),(4.4),(4.5) and (4.9), we can get

$$\frac{\sqrt{\frac{\overline{i_L^2}}{\Delta f}+\frac{\overline{i_v^2}}{\Delta f}}}{\sqrt{\frac{\overline{i_n^2}}{\Delta f}}} < \frac{g_v+g_L}{\gamma\alpha_{\min}(g_v+g_L)} = \frac{1}{\gamma\alpha_{\min}} \tag{4.10}$$

Since the transistors are all short-channel transistors, $\gamma \sim 2.5$. In Equation (4.8), let $\alpha_{\min}=2.5$, so $\frac{\sqrt{\frac{\overline{i_L^2}}{\Delta f}+\frac{\overline{i_v^2}}{\Delta f}}}{\sqrt{\frac{\overline{i_n^2}}{\Delta f}}} < \frac{1}{\gamma\alpha_{\min}} = \frac{1}{2.5\times 2.5} = 16\%$. That means the active devices contributes more than 80% of the phase noise.

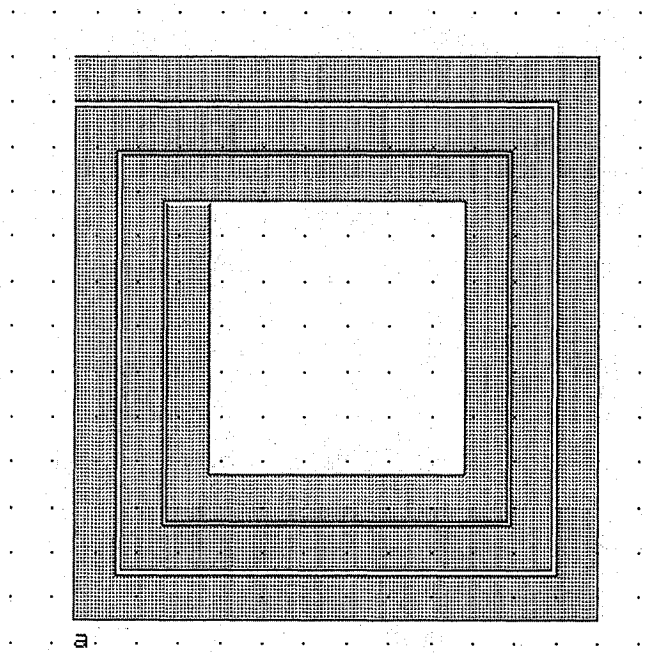
Since $q_{\max} = C\cdot V = V_{\tan k}/(L_{\tan k}\omega^2)$, we can get that

$$L\{\Delta f\} \propto \frac{L^2 I_{drain}}{V_{\tan k}^2} \tag{4.11}$$

Here we can visualize that at a given drain current; the phase noise is lower for the complementary structure because V_{tank} is doubled. For a given area for the inductor, the minimum effective parallel conductance g_L decreases with an increasing inductance. If we make L the maximum to get a small g_L, we get a small g_m and less power consumption. However the phase noise increases. Since $V_{\tan k} = I_{bias}/g_o$, $L\{\Delta f\} \propto \frac{L^2 g_o^2}{I_{bias}}$, a larger bias current is good for phase noise performance. So at a given power supply, we make I_{bias} as big as possible and L as small as possible on the condition that startup condition are met.

The design strategy is to find the minimum inductance that satisfies both tank amplitude and startup conditions for the maximum bias current allowed by the design specifications. Here is an example:

The oscillating frequency is 2.4GHz. The minimum tank amplitude is 0.8V. The maximum bias current is 2.2 mA. Since $V_{\tan k} = \frac{I_{bias}}{g_{\tan k}}$, so $g_{tank,max}$=2.75 mS. Because the Q of the inductor is less than that of the varactor, we can approximately set the conductance of the inductor is 2.65 mS. Figure 31 shows two different inductors with the same conductance 2.65 mS. However, the inductance of 'a' is 2.53nH and the inductance of 'b' is 2.281nH. The simulation results using ASITIC is shown in Figure 32. Following the design strategy, inductor 'b' is better than inductor 'a' in this application.



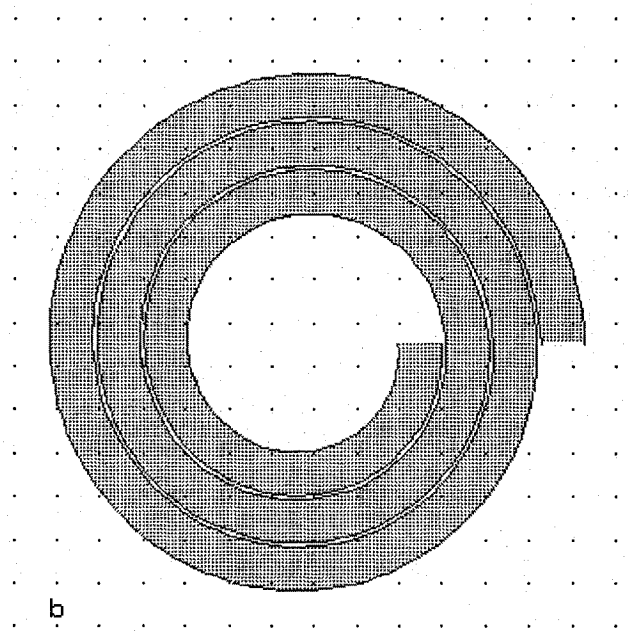


Figure 31 two different topologies of inductors

```
ASITIC>  pi a 2.4

Pi Model at f=2.4 GHz:  Q = 6.471 , 6.435 , 7.807
L = 2.53 nH R = 3.9
Cs1 = 161.1 fF Rs1 = 482.6
Cs2 = 157.7 fF Rs2 = 406.6      Est. Resonance = 7.884 GHz
ASITIC>  pi b 2.4

Pi Model at f=2.4 GHz:  Q = 9.948 , 9.905 , 10.43
L = 2.281 nH R = 3.141
Cs1 = 130.9 fF Rs1 = 17.36
Cs2 = 133.4 fF Rs2 = 18.68      Est. Resonance = 9.287 GHz
```

Figure 32 Simulation results of the inductors in Figure 27

4.2 Design parameters

Recall the specifications in chapter 1, they are:

Oscillating frequency:	2.4 GHz
Tuning range	>97MHz
Phase Noise @ 600 KHz offset from the carrier:	-100dBc/Hz
Phase Noise @ 2 MHz offset from the carrier:	-110dBc/Hz

Phase Noise @ 3 MHz offset from the carrier: -119dBc/Hz

The design is accomplished using TSMC 0.18 μm technology. Some typical technology related parameters are listed in Table 6 below:

Table 6 Some typical parameters of TSMC 0.18um technology

	NMOS	PMOS
t_{ox} (m)	4.08e-09	4.08e-09
c_j (F/m^2)	1.000266e-3	1.121e-3
c_{jsw} (F/m)	2.040547e-10	2.481e-10
c_{jswg} (F/m)	3.340547e-10	4.221e-10
v_{th0} (V)	0.4452004	- 0.4469995

System specifications are:

single supply voltage 1.8V

load capacitance 0.5 pF

maximum biasing current 1mA

Design work:

Recall the simulation results of the varactor in chapter 2, the minimum capacitance is 0.36 pF and the maximum capacitance is 1.47 pF. The Q of the varactor is from 16 to 48. The inductance in this design is 4.2nH. The serial resistance is about 4Ω. Now the design goal is to set g_m and other parameters of the transistors.

Using the equations in (4.6) g_v and g_L is about 1.1mS and 2.03mS, respectively. To meet the start up condition (4.8), the total g_m of the cross-coupled transistors should be at

least 7.2 mS. As $g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th}) = \frac{2I_D}{V_{GS} - V_{th}}$, we can determine the size of MOS transistors. Some parameters of the cross-coupled transistors are shown in Table 7.

Table 7 Some parameters of the cross-coupled transistors

	NMOS	PMOS
W/L (um)	24/0.18	80/0.18
g_m (mS)	3.619	3.693
g_{ds} (uS)	95.67	83.28
V_{th} (V)	0.71	-0.57
I_{ds} (mA)	0.3	-0.3
C_{gs} (pF)	0.02	0.1
C_{db} (aF)	3.7	32.2
C_{gd} (fF)	8.3	24.7

At the control voltage of 0V, using equation (4.1), the effective capacitance of the varactor is 0.81 pF. Combined with the load capacitance, the paracitic capacitance of the transistors, and the capacitance of the inductor, the total capacitance is about 1.4 pF. So C_{tank} is 0.7 pF. The inductance of the tank is 4nH. The oscillating frequency is

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{tank}C_{tank}}} = \frac{1}{2\times 3.14\times\sqrt{4\times10^{-9}\times 0.7\times10^{-12}}} = 3.01 \quad GHz$$

Following the same method above, at the control voltage of 1.8V, the oscillating frequency is about 2.4 GHz. This results the tuning range of about 600 MHz.

For the phase noise, as we analyzed above, most phase noise comes from the transistors. Using equation (4.2), we could predict the phase noise at 3MHz offset from the center frequency.

$$L\{3MHz\} \approx \frac{1}{8\pi^2 \Delta f^2} \cdot \frac{1}{q_{\max}^{\ 2}} \cdot 2kT \cdot g_m = \frac{1}{8\pi^2 \Delta f^2} \cdot \frac{1}{q_{\max}^{\ 2}} \cdot 2 \cdot q_{\max} \cdot V_T \cdot g_m$$

$$= \frac{2 \times 26 \times 10^{-3} \times 7 \times 10^{-3}}{8 \times 3.14^2 \times (3 \times 10^6)^2 \times (1.89 \times 10^{-12} \times 1)} = 2.7 \times 10^{-7} \approx -131 dBc / Hz$$

Following the same equation, the phase noise at 600 KHz offset and 2 MHz offset from the enter frequency are -103.4dBc/Hz and -124dBc/Hz.

From the calculation above, we can see that all the specs can be met.

4.3 Simulation results

4.3.1 Schematic level simulations

The schematic-level simulations include the transient response, tuning range and phase noise performance. Transient response gives a direct view of the oscillation. And the tuning range is completed by parametric transient response, which reports the operation range of the oscillator. Phase noise performance is the most important one. It can only be accomplished using CAD program, such as Spectre 4.4.5 or later version. The procedure follows.

First, we need to do the analysis to get the Periodic Steady-State (PSS). Then we can run **pnoise** analysis. *Pnoise* is better than noise because it can analyze the frequency shift. The process variations are also simulated.

4.3.1.1 Simulation configuration

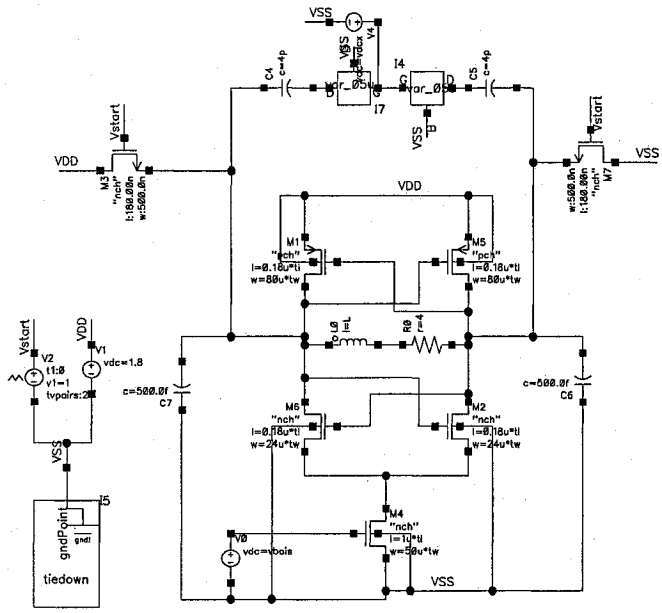


Figure 33 Configuration of the complementary LC VCO

The schematic entry diagram for simulation experiment is shown in Figure 33. The two transistors M3 and M7 are used to start up the oscillation and they will be removed in the layout. The fixed capacitor is 0.5pF. A series resistance is added to the inductor since it represents more realistic situation.

4.3.1.2 Transient response

As we predicted above, at control voltage of 0v, the oscillating frequency is likely to be 3.01GHz.

The transient response is shown below. The oscillating frequency is observed to be about 3.2GHz.

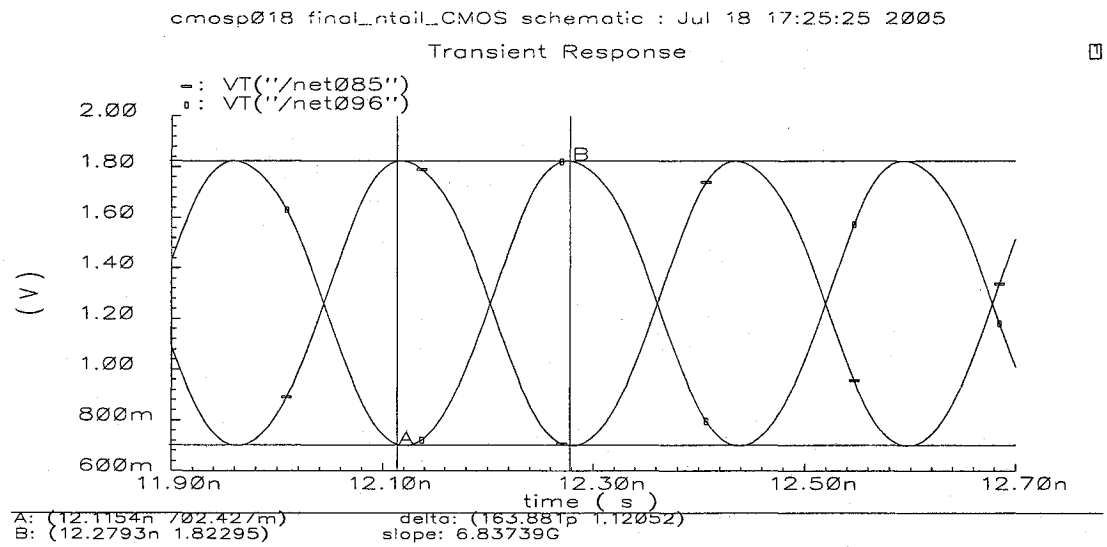


Figure 34 Transient simulation result of the complementary LC VCO

Even though the modern CMOS technology is advanced, there are still variations in the process. When the parameter changes, the oscillating frequency shifts. Table 8 below shows such effects. When the length of the transistors increases, the oscillating frequency doesn't change. This does not mean the oscillating frequency is independent on the length of the transistor. The situation can be understood in the following way.

When the length increases or width decreases, the transconductance of transistors drops. So the amplitude of the oscillation increases, which makes the effective capacitance of the varactor drop. However, when the length of the transistor increases with width fixed, the parasitic capacitance of transistors increases. This compensates for the reduction of the capacitance of the tank. When the width of transistors decreases with

fixed length, the parasitic capacitance of transistors decreases too. So the total capacitance of the tank drops, which makes the oscillating frequency increase.

Since the center oscillating frequency is defined as the mean of the maximum frequency and the minimum frequency, the variation of the center oscillating frequency is under 1.4% when the variation of the process is 10%.

Table 8 Center frequency shift at process variation

Process variation	No process variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Oscillating frequency (GHz)	2.91	2.91	2.87	2.95

4.3.1.3 Tuning range

Following the same method to predict the oscillating frequency as above, we can change the control voltage of the varactor from 0V to 1.8V. Thus, we can predict that the tuning range will be from 2.4GHz to 3.01GHz.

Using parametric analysis and the calculator (a tool in Cadence), we can get the tuning range plotted below. The tuning range is from 2.588GHz to 3.235GHz. The tuning range is 629MHz. The widest tuning range in 0.18um technology, reported so far, is 650MHz [55]. The simulation result is shown below.

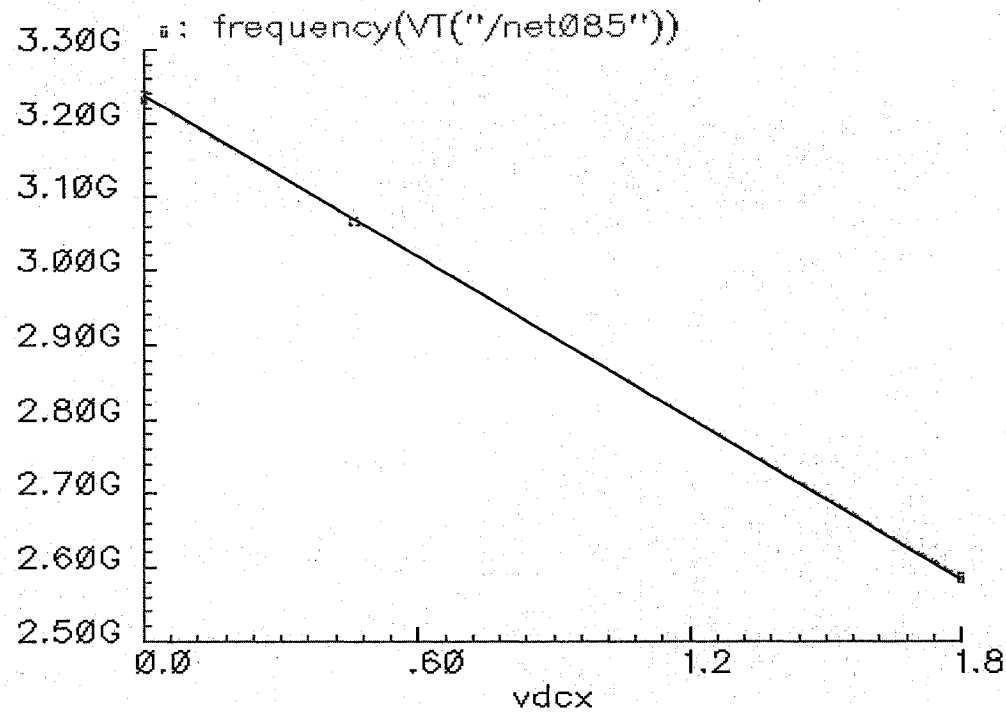


Figure 35 Tuning range of the complementary LC VCO

When the parameter changes, the tuning range shifts. Table 9 below shows such effects.

Table 9 Center frequency shift at process variation

Process variation	No process variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Tuning range (GHz)	2.588~3.235	2.584~3.231	2.562~3.18	2.612~3.293

The variation of the tuning range is under 5% when the variation of the process is 10%.

4.3.1.4 Phase noise performance

As we analyzed above, most phase noise comes from the transistors. Using equation (4.2), we could predict the phase noise at 3MHz offset from the center frequency is –131dBc/Hz. The phase noise at 600 KHz offset and 2 MHz offset from the enter

frequency are -103.4dBc/Hz and -124dBc/Hz, respectively. The simulated result is shown in Figure 36.

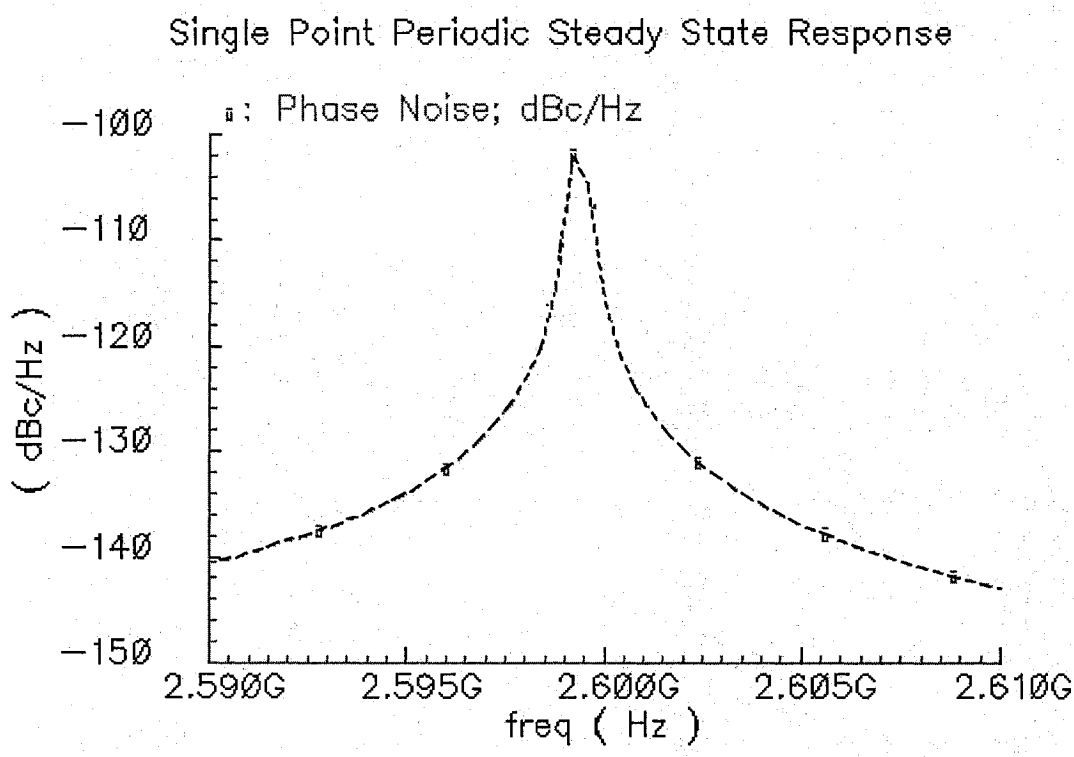


Figure 36 Phase noise of the complementary LC VCO

When the parameter varies, the phase noise shifts. Table 10 shows such effects. The variation of the oscillating frequency is under 1.8% when the variation of the process is 10%.

Table 10: Center frequency shift at process variation

Phase Noise (dBc/Hz)	No process variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Phase noise @600kHz offset	-115	-116	-113	-115
Phase noise @2MHz offset	-127	-128	-126	-127.5
Phase noise @3MHz offset	-131	-132	-130	-131

4.3.2 Post-layout simulations

4.3.2.1 Layout considerations of the complementary LC VCO

Some aspects about the inductor layout optimization have been illustrated in chapter 3. There are some additional guidelines to follow when we layout the entire system. First of all, the layout should be symmetric for the purpose of matching. Second, the inputs and output pins should be arranged as far as possible to decrease the interference. The input/output buffers should be put close to the corresponding pins so that the signal routing length is kept as short as possible. As a rule of thumb, the current density 1mA/um should be used for calculating the metal width.

The layout of the complementary LC VCO is provided in chapter 6. The simulation results are discussed below.

4.3.2.2 Post-layout simulation results

Because of Cadence's inability to extract the inductor, we excluded the inductor when we do extraction. The model of inductor is added prior to simulation using the method illustrated in chapter 3. The transient response, tuning range and phase noise performance are shown in Figures 37, 38 and 39 respectively.

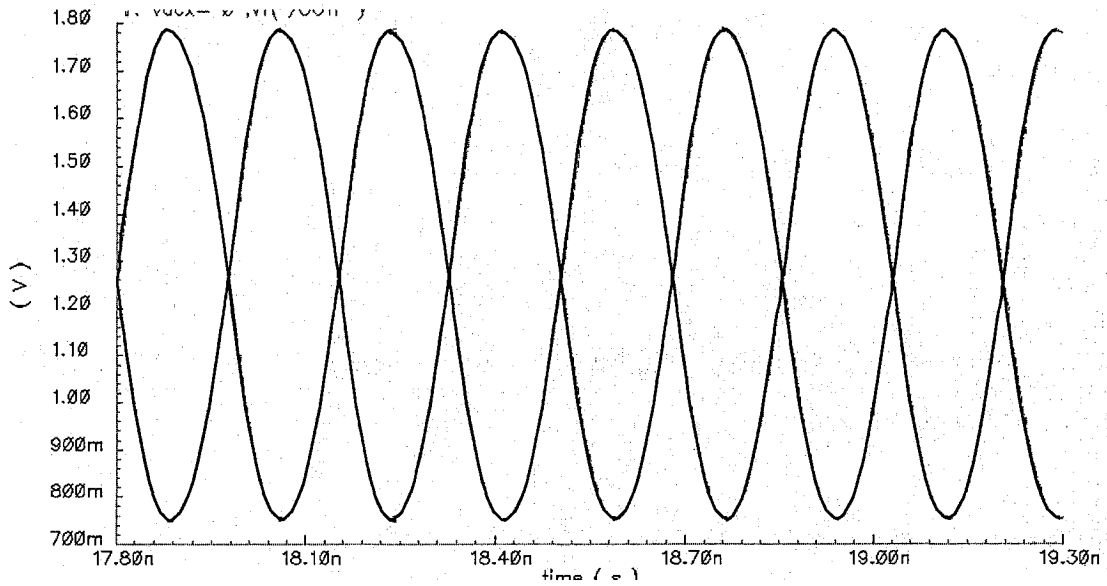


Figure 37 Post-layout transient response of the complementary LC VCO

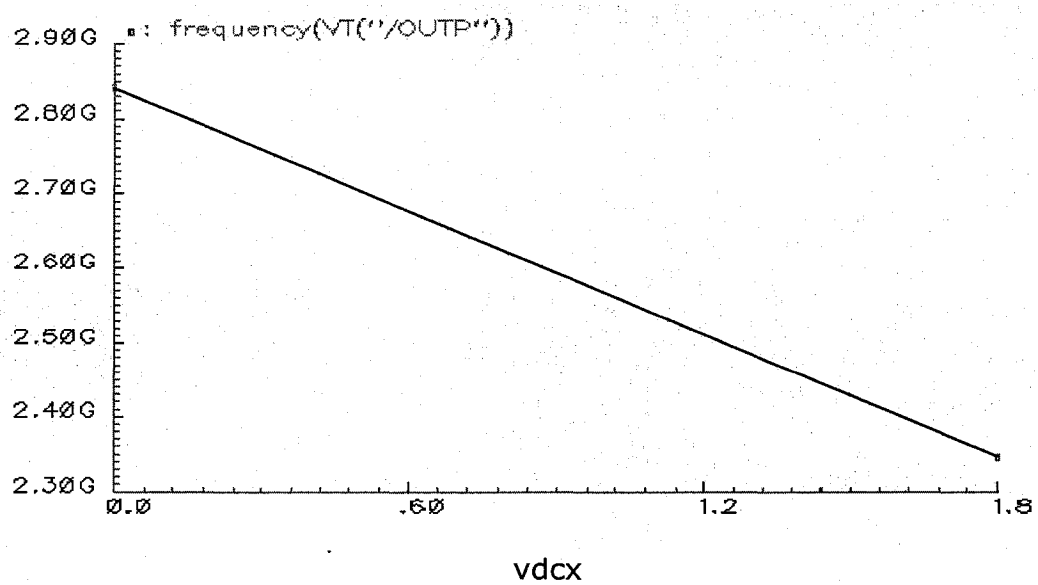


Figure 38 Post-layout response of the tuning range

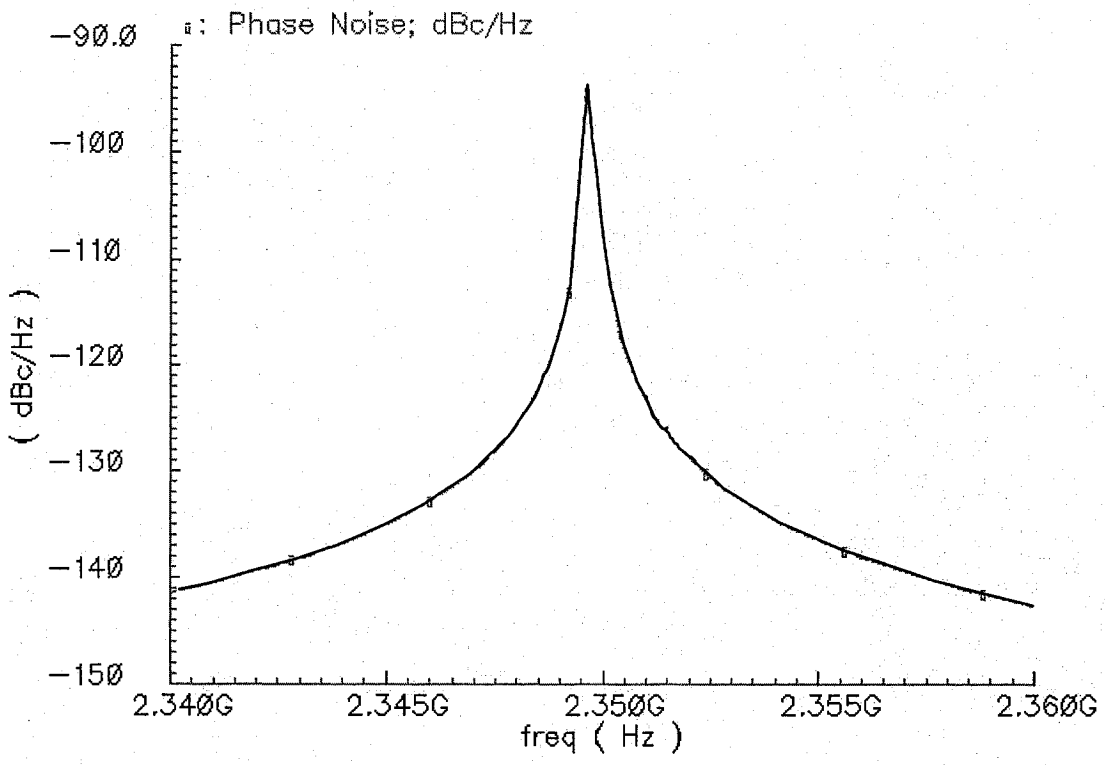


Figure 39 Post-layout phase noise performance

In Figure 37, we can see the peak to peak amplitude is about 1.1V. In Figure 38, we see that the tuning range is 2.35G~2.85G. It drops about 150MHz compared with the value obtained from schematic level simulation. It is because of the parasitic capacitances of the connection wires were added to the load of the complementary LC VCO. Using the definition $\omega_{center} = \frac{\omega_{\max} + \omega_{\min}}{2}$ the center frequency changes to 2.6GHz. Compared with the schematic simulation results (2.588 GHz), the difference is reasonable.

In Figure 39, the post-layout phase noise performance is shown. The Phase noise at 3MHz offset from the center frequency is -131dBc/Hz. The phase noise at 2MHz offset and 600 KHz offset are shown in Table 11. As shown before, the schematic simulation results are: -115dBc/Hz, -127dBc/Hz and –131dBc/Hz, respectively.

Table 11 Post-layout phase noise performances of the complementary LCVCO

	Phase noise @600kHz offset	Phase noise @2MHz offset	Phase noise @3MHz offset
Phase noise (dBc/Hz)	-116	-127	-131

4.4 Summary

In this chapter, the oscillation model of the complementary LC VCO is analyzed. The design of the complementary LC VCO is accomplished. Schematic level and post-layout net lists are simulated using SpectreS. Also the effects of process variation are provided. The simulation results show it can meet the specifications of Bluetooth application.

Using the definition of FOM in chapter one, the FOM of this design is:

$$\begin{aligned} FOM &= 20\log_{10}(freq) - PhaseNoise - 10\log_{10}(Power) \\ &= 20\log_{10}(2.91\times10^{9}) + 116 - 10\log_{10}(1.08\times10^{-3}) \\ &= 336 \end{aligned}$$

5 The design of the Sub Threshold LC VCO

In the previous chapter, we have studied the complementary LC VCO. Tank model and theoretical analysis were given along with the simulation results. In this chapter, we shall consider the design of the sub threshold LC VCO. There are many similarities between the complementary LC VCO and the sub threshold LC VCO. The major difference between these two is the working region of the transistors.

5.1 Tank modeling of the sub threshold LC VCO

According to the study before, about 80% percent of the phase noise of the complementary cross-coupled pair and tail current source LC Oscillator comes from the tail current source. So a modification has been made to the original topology. Instead of the tail current, another tank is used. [10] The new topology and its oscillating model are shown in Figure 40.

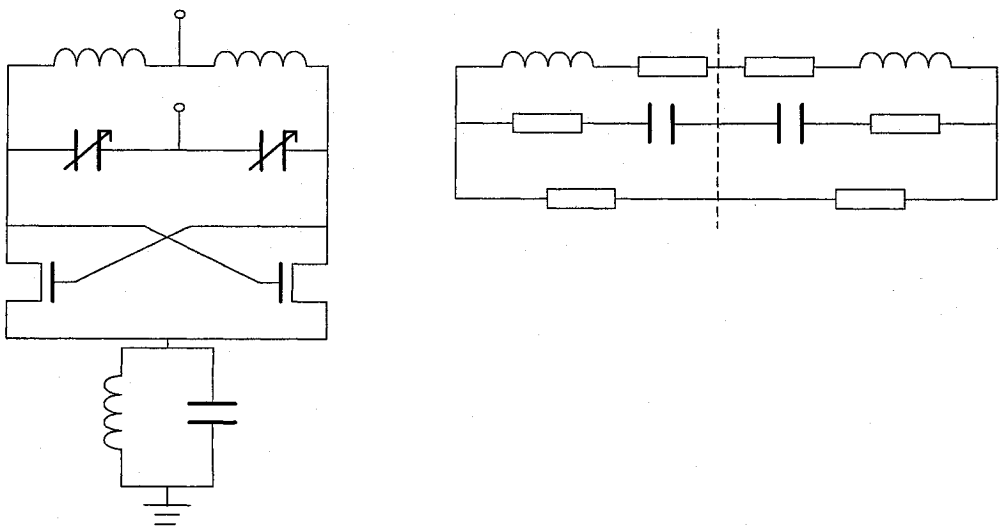


Figure 40 The topology of the the sub-threshold LC VCO and its oscillating model

Because of lack of the regulation of the current tail, this circuit could draw a large current from the supply. However, the startup of oscillation of the LC tank is independent on how big the current is (but we need it to be non zero) as long as at certain frequency the total impedance of L and C adds up to zero. When we scale down the power supply, the biasing current gets smaller for the same transistor. We can reduce the power consumption without affecting the oscillation. Also, it is reported that for the same current, the transconductance in sub-threshold operation is much higher than that in strong inversion region [56]. In the sub-threshold region the trans-conductance is proportional to I_D while in the strong inversion region the trans-conductance is proportional to $\sqrt{I_D}$ [56]. So we can get a relatively large g_m at a small current. It is exactly what we need.

The tank bias network is a band pass filter. By adjusting its center frequency and bandwidth, it could filter away the worst harmonics of the oscillation, which is very helpful to improve the phase noise performance [10].

5.2 Theoretical analysis

In Figure 40, the broken line represents the common mode or ground. g_m and g_{ds} are small-signal transconductance and output conductance of the transistors, respectively. To facilitate the analysis of the tank, simple models of the varactor and inductor are used. The varactor is represented by a capacitor C_v in series with a resistor R_v. The inductor is represented by a serial resistance $r_L(= 1/g_L)$ with an inductance L.

5.2.1 Oscillating frequency and gain of VCO

The analysis of the oscillating frequency and gain of VCO is the same as that of the complementary LC VCO, which are

$$\omega_o = \frac{1}{\sqrt{LC_{eff}}}$$

$$\text{and } K_{VCO} = \frac{C_{\min} - C_{\max}}{\pi\sqrt{L}AV_{eff}} \frac{\sqrt{1-\left(\frac{V_{eff}}{A}\right)^2}}{\sqrt{\frac{1}{2}(C_{\max}+C_{\min})+\frac{C_{\min}-C_{\max}}{\pi}\left(\sin^{-1}\frac{V_{eff}}{A}+\frac{V_{eff}}{A}\sqrt{1-\left(\frac{V_{eff}}{A}\right)^2}\right)}}$$

$$\text{where } C_{eff} = \frac{1}{2}(C_{\max}+C_{\min})+\frac{1}{\pi}(C_{\min}-C_{\max})\left[\sin^{-1}\frac{V_{eff}}{A}+\frac{V_{eff}}{A}\sqrt{1-\left(\frac{V_{eff}}{A}\right)^2}\right]$$

And $V_{eff} = V_G - V_C - V_T$ is the effective control voltage of the varactor. A is defined as the amplitude of the oscillation. C_{max} and C_{min} are the maximum and minimum capacitance of the varactor.

The relationship between K_{VCO}, V_{eff}, A and C_{eff} will be the same as that in the the complementary LC VCO, which has been studied in chapter 4.

5.2.2 Phase noise performance

We present below the steps to determine the phase noise characteristics with the NMOS transistors operating in the sub-threshold region.

The drain to source current, the trans-conductance and the trans-conductance from drain to source are given by [57]

$$I_{DS} = I_0\left[1-\exp\left(-\frac{V_{DS}}{V_t}\right)\right]\exp\left[\frac{V_{GS}-V_{th}-V_{eff}}{nV_t}\right],$$

$$g_m \cong \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_{DS}}{nV_t}, \text{ and}$$

$$g_{ds} \cong \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{I_{DS}}{V_t} = \frac{3}{2}g_m, \text{ respectively.}$$

In the above $V_t = 26mV@27^oC$, and n is an experimental parameter, usually 1.5.

The equivalent current noise density of the NMOS is [56]

$$\frac{\overline{i_n^2}}{\Delta f} = 2qI_{sat}\left[1+e^{\frac{V_{DS}}{V_t}}\right] = \frac{2kT}{V_t}\cdot I_0\cdot e^{\frac{\kappa V_G - V_S}{V_t}}\left[1+e^{\frac{V_{DS}}{V_t}}\right] \geq \frac{2kT}{V_t}\cdot I_{DS} = 2kT\cdot n\cdot g_m \quad (5.1)$$

In the oscillating model, the overall trans-conductance is

$$g_o = -g_m + g_{ds} + g_v + g_L = \frac{1}{2}g_m + g_v + g_L$$

To satisfy $g_m \cdot R_o \geq 1$ to oscillate,

$$\frac{g_m}{\frac{1}{2}g_m + g_v + g_L} \geq 1$$

$$\text{So, } g_m \geq 2(g_v + g_L) \quad (5.2)$$

In the $1/f^2$ region, phase noise is given by

$$L\{\Delta f\} = \frac{1}{8\pi^2\Delta f^2}\cdot\frac{1}{q_{\max}^2}\cdot\sum_n\left(\frac{\overline{i_n^2}}{\Delta f}\cdot\Gamma_{rms,n}^2\right) \quad \text{(dBc/Hz)} \quad (5.3)$$

Where Δf is the offset frequency from the center frequency and q_{max} is the total charge swing of the tank. The impulse sensitivity function (ISF), Γ represents the time-

varying sensitivity of the oscillator's phase to perturbations. For an ideal sinusoidal waveform, $\Gamma_{rms} = 1/\sqrt{2}$. $\frac{\overline{i_n^2}}{\Delta f}$ is the equivalent differential noise power spectral density.

For the varactor, $\frac{\overline{i_v^2}}{\Delta f} = 2kT \cdot g_v$

For the inductor, $\frac{\overline{i_L^2}}{\Delta f} = 2kT \cdot g_L$

For the transistor, $\frac{\overline{i_n^2}}{\Delta f} \geq 2kT \cdot n \cdot g_m \geq 2kT \cdot n \cdot 2(g_v + g_L)$

So $\frac{\overline{i_n^2}/\Delta f}{\overline{i_n^2}/\Delta f + \overline{i_v^2}/\Delta f + \overline{i_L^2}/\Delta f} \geq \frac{2n}{2n+1} = \frac{3}{4} = 75\%$ with n=1.5

In the sub-threshold LC VCO, the noise generated by the NMOS transistors contributes more than 75% of the total noise. Also equations (5.1)- (5.3) give us a hint that when g_v and g_L goes smaller, g_m could become smaller which leads to better phase noise performance. Theoretically, the oscillation amplitude could be larger than the supply voltage when ($g_v + g_L - g_m$) is small enough because the inductors store energy.

5.3 Design parameters

Recall the specifications in chapter 1, they are:

Oscillating frequency:	2.4 GHz
Tuning range	>97MHz
Phase Noise @ 600 KHz offset from the carrier:	-100dBc/Hz
Phase Noise @ 2 MHz offset from the carrier:	-110dBc/Hz

Phase Noise @ 3 MHz offset from the carrier: -119dBc/Hz

The design is accomplished using TSMC 0.18 μm technology. Some typical technology related parameters are listed in the previous Table 6.

The system specifications are:

single supply voltage 0.5 V

load capacitance 0.5pF

maximum biasing current 600 uA

Design work:

Recalling the simulation results of the varactor in chapter 2, we shall use the capacitance value in the range 0.36 pF ~ 0.7 pF with control voltage in the range of 0~0.5V. The Q of the varactor is in the range of 16 to 42. The inductance of the tank is 3nH each, and the inductance in the bias is 1nH. The parallel capacitance in the bias tank is 0.7pF. Some parameters of the NMOS transistor is given in Table 12

Table 12 Some parameters of the NMOS transistors

	NMOS
W/L (um)	56/0.18
g_m (mS)	2.31
g_{ds} (uS)	129.2
V_{th} (V)	0.515
I_{ds} (mA)	0.25
C_{gs} (pF)	0.04
C_{db} (aF)	10
C_{gd} (fF)	20.5

At the control voltage of 0.5V, using equation (4.1), we get the effective capacitance of the varactor to be 0.86 pF. Combined with the load capacitance, parasitic capacitance of the transistors, and the capacitance of the inductor, the total capacitance is about 1.4 pF. So C_{tank} is 0.7 pF. The inductance of the tank is 6nH. The oscillating frequency is $f_{osc} = \frac{1}{2\pi\sqrt{L_{\tan k}C_{\tan k}}} = \frac{1}{2\times 3.14\times\sqrt{6\times10^{-9}\times0.7\times10^{-12}}} = 2.457 \quad GHz$

Following the same method as above, at the control voltage of 0 V, the oscillating frequency is about 2.772 GHz. This results the tuning range of about 315 MHz.

For the phase noise, as we analyzed above, most phase noise comes from the transistors. Using equation (5.3), we could predict the phase noise at 3MHz offset from the center frequency.

$$L\{3MHz\} \approx \frac{1}{8\pi^2\Delta f^2}\cdot\frac{1}{q_{\max}{}^2}\cdot 2kT\cdot n\cdot g_m = \frac{1}{8\pi^2\Delta f^2}\cdot\frac{1}{q_{\max}{}^2}\cdot 2\cdot q_{\max}\cdot V_T\cdot n\cdot g_m$$
$$= \frac{2\times26\times10^{-3}\times1.5\times2.31\times10^{-3}}{8\times3.14^2\times(3\times10^6)^2\times(1.4\times10^{-12}\times1.1)} \approx 1.65\times10^{-7} = -135.7 dBc/Hz$$

Following the same equation, the phase noise at 600 KHz offset and 2 MHz offset from the enter frequency are -107.7dBc/Hz and –128.6dBc/Hz.

From the calculation above, we can see that all the specifications can be met.

5.4 Simulation results

5.4.1 Schematic simulations

The simulation method is exactly the same as that in chapter 4. The schematic-level simulations include the transient response, tuning range and phase noise performance.

Transient response gives a direct view of the oscillation. And the tuning range is completed by parametric transient response, which reports the operation range of the oscillator. Phase noise performance can be obtained by using PSS and P_{noise} analysis.

5.4.1.1 Simulation configuration

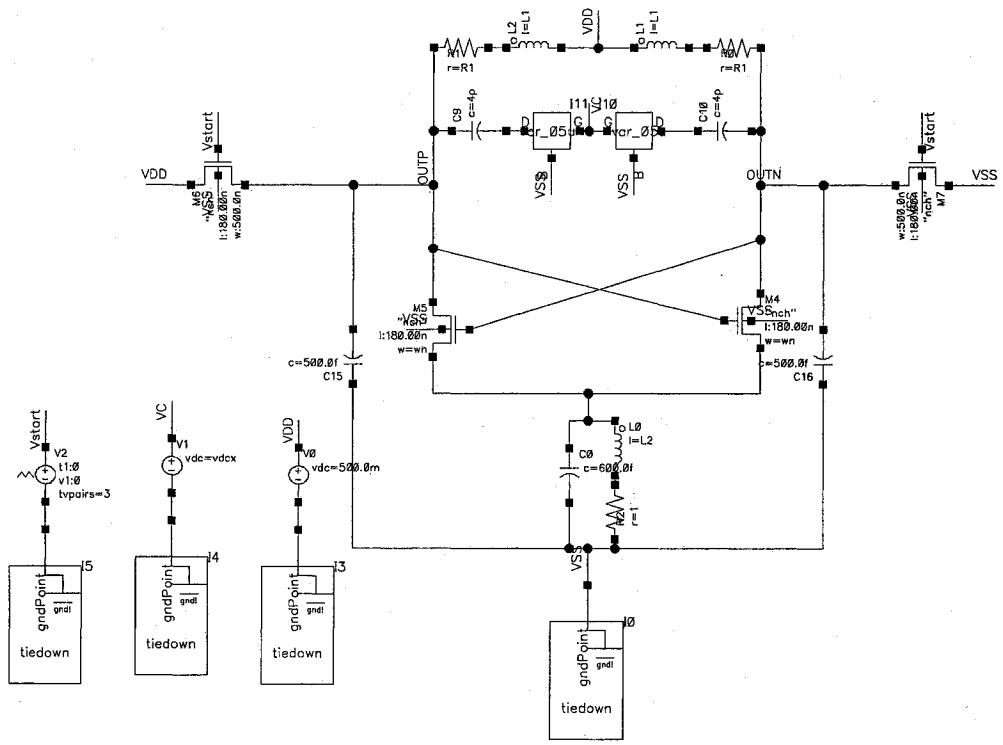


Figure 41 Simulation configuration of sub-threshold LC VCO

The simulation configuration is shown in Figure 41. Two extra transistors (compared to Figure 41) are used to start up the oscillation. When the oscillation starts, they are turned off. The series resistor of the tank inductor is 3 Ω. And the series resistor of the biasing inductor is 1 Ω.

5.4.1.2 Transient simulation

The transient simulation results are shown in Figure 42. A large amplitude is helpful to reduce phase noise. In this application, the VCO has a tuning range of about 1.1v. At the control voltage of 0V, as we have predicted above, the oscillating frequency is likely to be 2.772GHz. The oscillating frequency observed is 2.763GHz. The center frequency shift at technology variation is shown in Table 13.

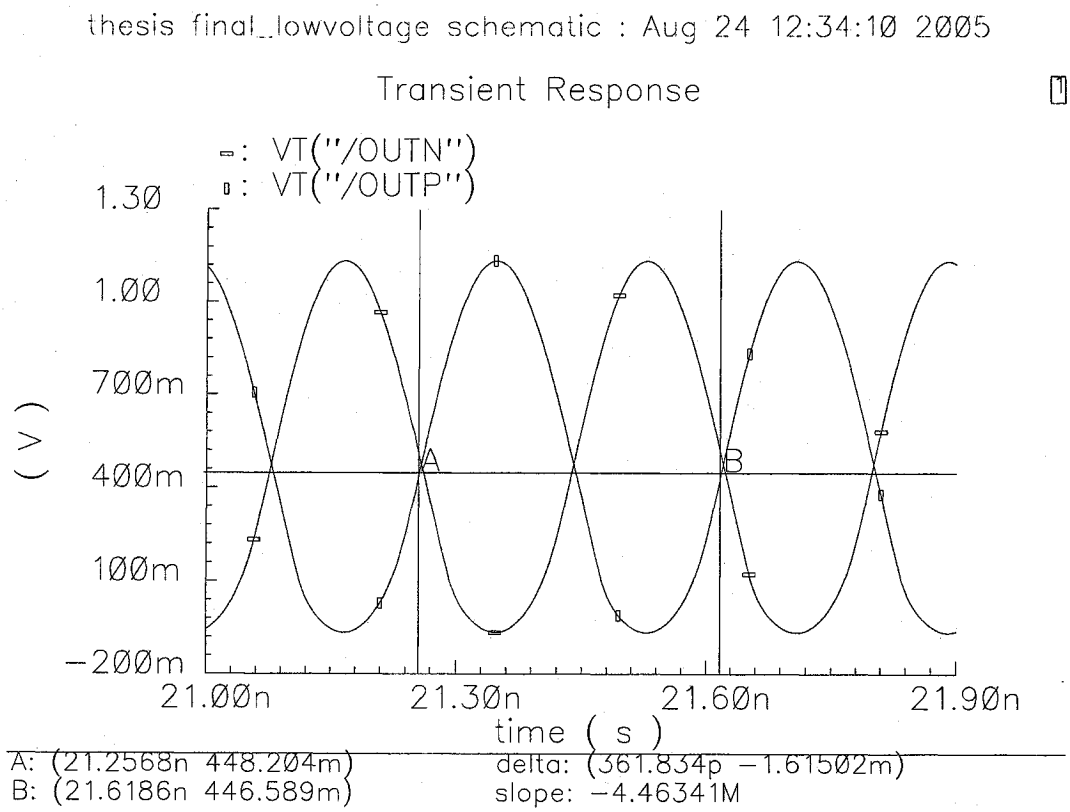


Figure 42 Transient simulation results of sub-threshold LC VCO

Table 13 Center frequency shift at technology variation

Technology variation	No technology variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
oscillating frequency (GHz)	2.62	2.61	2.59	2.64

When the length of the transistors increases, the oscillating frequency does not change. This does not mean the oscillating frequency is independent on the length of the transistor. When the length increases or width decreases, the transconductance of transistors drops. So the amplitude of the oscillation increases, which makes the effective capacitance of the varactor drop. However, when the length of the transistor increases, the parasitic capacitance of transistors increases. This compensates the loss of the capacitance of the tank. While when the width of transistors decreases, the parasitic capacitance of transistors decreases, too. So the total capacitance of the tank drops, which makes the oscillating frequency increase.

5.4.1.3 Tuning range simulation

In chapter 2, we got the capacitance range of the varactor from 0.36pF to 0.7pF at the control voltage of 0~0.5V. Since $\omega \propto \frac{1}{\sqrt{C}}$, along with the fixed capacitance here, we can predict a tuning ratio of about 1.15. From simulation, I got the tuning ratio of 1.12 from 2.471GHz to 2.763GHz. The tuning range is 292MHz. It is shown in Figure 43. Our calculated values were a frequency range of 2.457GHz~2.772GHz with a tuning range of 315MHz.

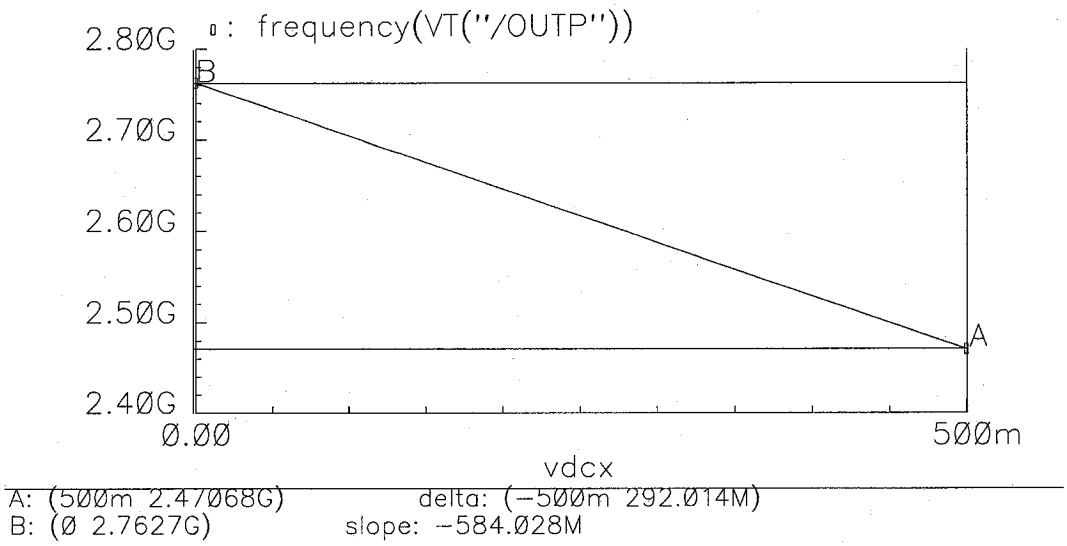


Figure 43 Tuning range of the sub-threshold LC VCO

Table 14 Tuning range shift at technology variations

Technology variation	No technology variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Tuning range (GHz)	2.471~2.763	2.462~2.755	2.451~2.733	2.49~2.793

The tuning range shift with technology variations is shown in Table14. As in the transient simulation result, the tuning range does not change significantly as the length of

the transistors changes. When the width of the transistors decreases, the parasitic capacitance of the transistors drops. The percentage of the fixed capacitance of the varactor drops too. So the tuning range rises. When technology varies 10%, the variation of the tuning range is under 4%.

5.4.1.4 Phase noise simulation

As we analyzed above, most phase noise comes from the transistors. The phase noise at 3MHz, 2MHz and 600kHz offset from the center frequency are -135.7dBc/Hz,-128.6dBc/Hz and -107.7dBc/Hz, respectively.

The simulation result is shown in Figure 44. The simulated phase noise at 3MHz from center frequency is -135.5dBc/Hz. The phase noise performance at technology variation is shown in Table 15.

In table 15, we could see the phase noise changed a lot when width of transistors changed. This is a main drawback of this topology because it's lack of current source which regulate the trans-conductance of the transistors.

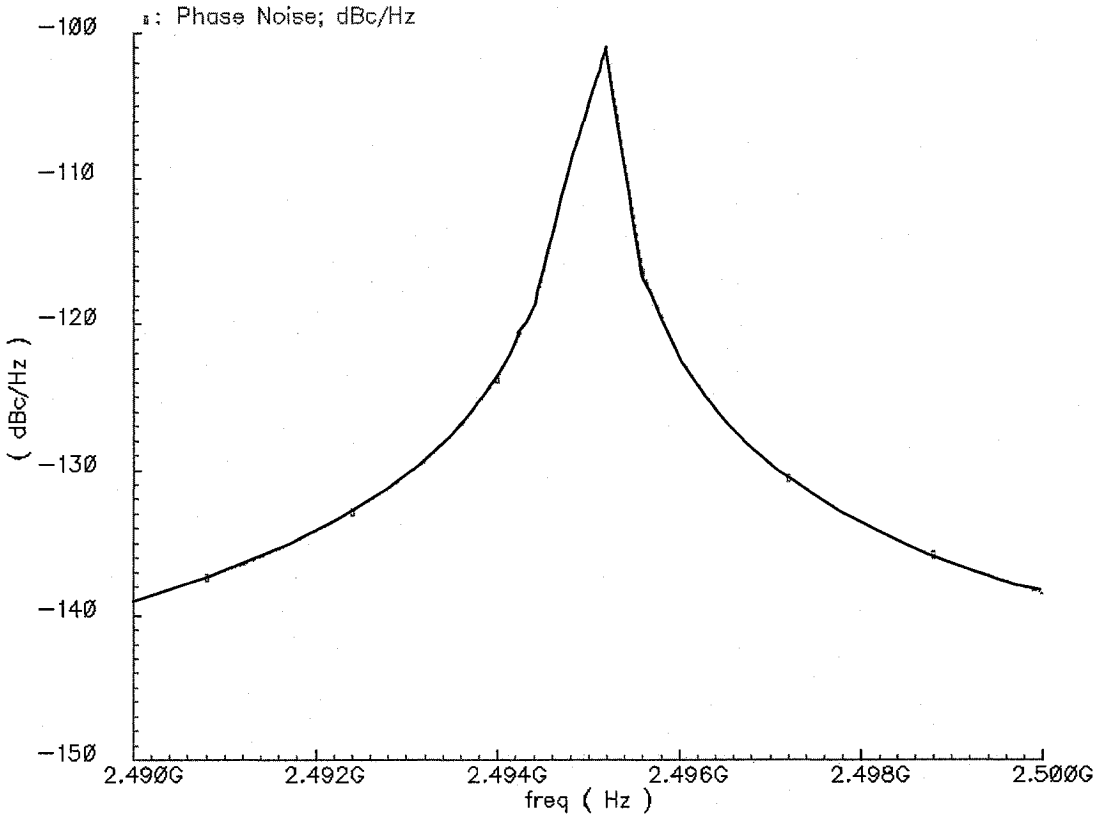


Figure 44 Phase noise simulation of the sub-threshold LC VCO

Table 15 Phase noise performance at technology variation

Phase noise (dBc/Hz)	No technology variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Phase noise @600kHz offset	-122.9	-118.5	-106.2	-126.2
Phase noise @2MHz offset	-132.1	-130.6	-120.7	-136.8
Phase noise @3MHz offset	-135.5	-134.6	-125.5	-140.5

As studied before, the phase noise of the LCVCO at 600KHz, 2MHz and 3MHz offset from the carrier frequency are: -115dBc/Hz, -127dBc/Hz and –131dBc/Hz,

respectively. We can see the improvement of the phase noise performance by replacing the biasing transistor by the biasing tank. At 600KHz offset from the carrier frequency, the phase noise was improved to -122.9dBc/Hz from -115 dBc/Hz.

5.4.2 Post-layout simulations

5.4.2.1 Layout

The layout techniques have been illustrated in the previous chapter. Because three inductors are involved, it occupies a large area of 0.7mm*0.7mm. The layout of sub-threshold LC VCO will be shown together with other oscillators in Chapter 6.

Because of Cadence's inability of extracting inductors, only transistors and capacitors including varactors are extracted. The inductors are replaced by lumped components. The start up transistors are still there because in the real chip, it is not necessary to build them in. The noise from substrate or power is enough to start the oscillation up.

5.4.2.2 Post-layout simulation results

The post-layout transient simulation results are shown in Figures 45, 46, 47, respectively. The oscillating frequency is 2.47GHz. The tuning range is from 2.339GHz to 2.604GHz. Because of the parasitic capacitance and resistance, the DC operating point shifts, thus the waveform is a little clipped. Since total signal energy is divided between fundamental and harmonics. If harmonics increase, the fundamental part reduces. From

the equation $L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right]$, we can see the increase in harmonics directly result in the increase in Phase noise.

The post-layout phase noise simulation result is shown in Figure 47. At 3MHz offset from center frequency, the phase noise increases from -135.5dBc/Hz to -134.5 dBc/Hz. Table 16 lists the different phase noise at 600kHz, 2MHz and 3MHz offset from the center frequency. As shown before, the schematic simulation results are: -122.9dBc/Hz, -132.1dBc/Hz and –135.5dBc/Hz, respectively.

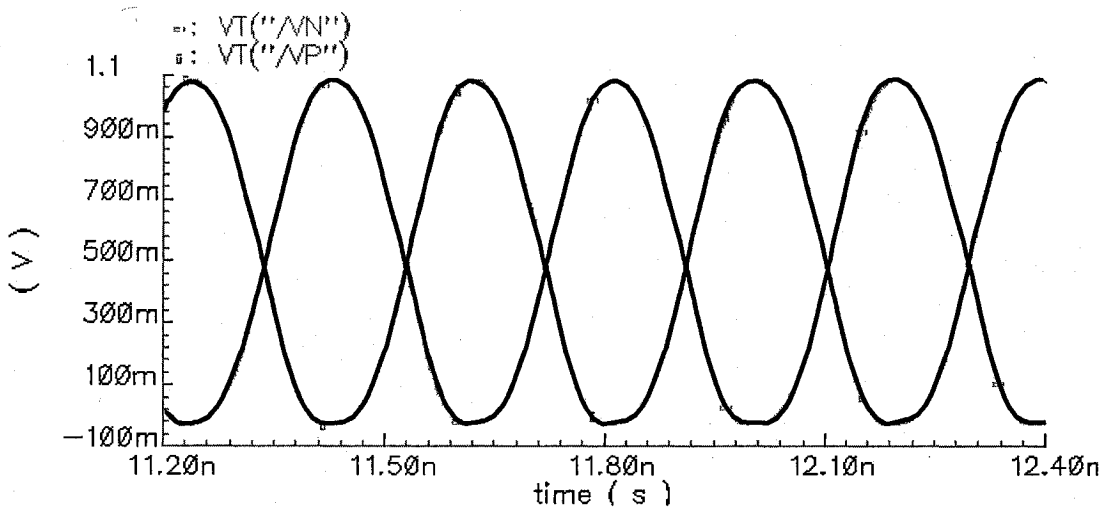


Figure 45 post-layout transient simulation result of sub-threshold LC VCO

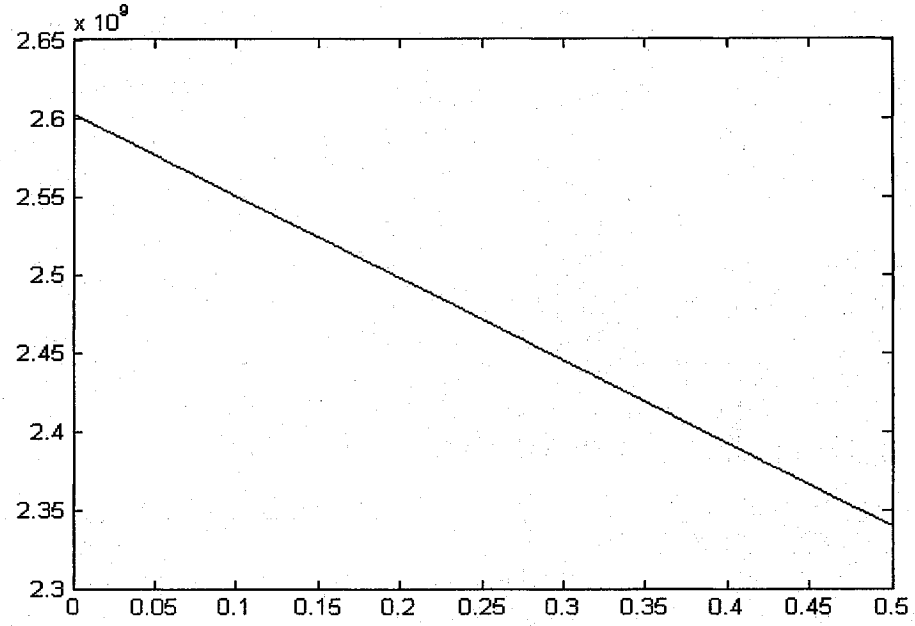


Figure 46 Post-layout tuning range of the sub-threshold LC VCO

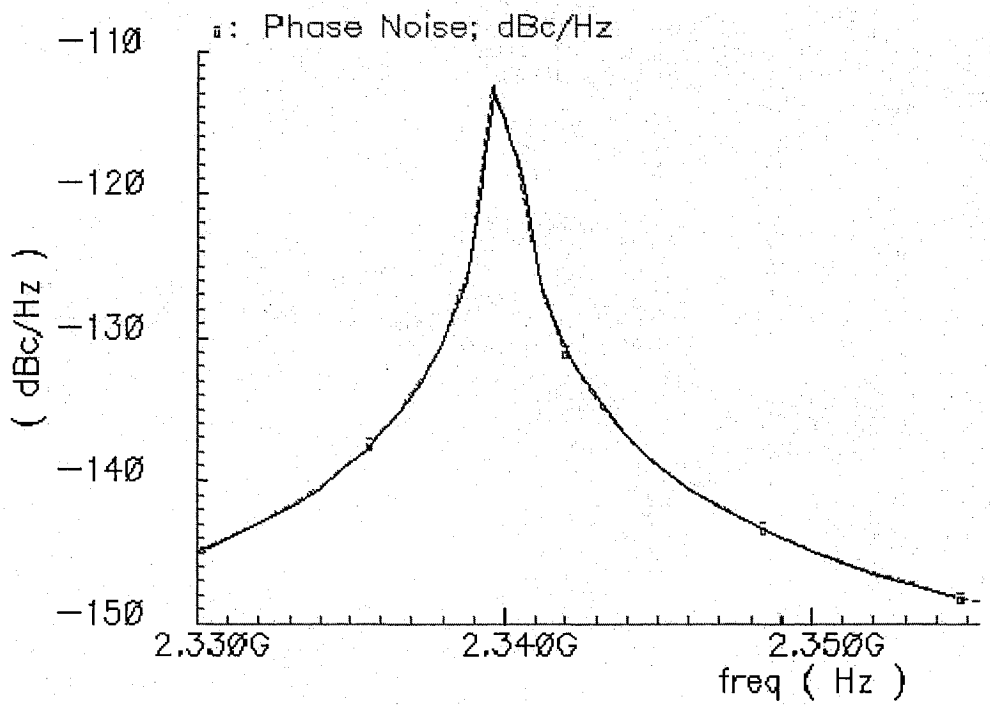


Figure 47 Post-layout Phase noise simulation of the sub-threshold LC VCO

Table 16 Post-layout Phase Noise of the sub-threshold VCO

	Phase noise @600kHz offset	Phase noise @2MHz offset	Phase noise @3MHz offset
Phase noise (dBc/Hz)	-118.1	-130.9	-134.5

5.5 Summary

The design of the sub-threshold LC VCO is based on the complementary LC VCO. Modifications have been made to improve the phase noise performance. The Phase noise at 3MHz offset from the center frequency is decreased from -131dBc/Hz to -134.5dBc/Hz. The sub-threshold LC VCO consumes 0.3mW power, occupies 0.049 mm^2 chip area and its main performances cover the Bluetooth SPECS and is better than the LC VCO. The FOM is calculated below:

$$\begin{aligned} FOM &= 20\log_{10}(freq) - PhaseNoise - 10\log_{10}(Power) \\ &= 20\log_{10}(2.61\times10^{9}) + 122.9 - 10\log_{10}(0.3\times10^{-3}) \\ &= 346.4 \end{aligned}$$

And the FOM of the CMOS LC VCO is 336.

6 The design of Ring Oscillators

In the previous chapters, we studied the LC based oscillators. Theoretical analysis of the oscillating model, design parameters and simulation results are provided. However, there is another category of oscillators, which is RC based oscillator. A typical example is the ring oscillator.

Ring VCOs are widely used circuit blocks in PLL and CDR (Clock Data Recovery) systems. The ring VCO usually is an inverter chain. Several inverters together form a positive feedback loop. CMOS oscillators with low phase noise and timing jitter are highly desired. Basically, a large signal voltage swing and improved linearity of the delay cells help reduce oscillator phase noise. Also ring oscillators with linear loads provide much better phase noise than oscillators with nonlinear loads. Theoretical analysis will be shown in 6.1.

6.1 Theory analysis

A time domain approach to analysis of differential CMOS ring oscillators is presented in [58]. The stage delay is defined as the time interval between zero-crossing of the input and output differential voltages. In a differential ring oscillator with the delay stage shown in Figure 48, the stage delay is approximately:

$$t_d = V_{swing} \frac{C_{node}}{I_{tail}} \qquad (6.1)$$

Where V_{swing} is single-end swing on the drain, C_{node} is the total capacitance on the stage output node including the input capacitance of the next stage, and I_{tail} is the tail current. Using the first-crossing approximation proposed in [59], the standard deviation

of the timing jitter due to a single stage $\sigma_{\tau,1}$ is related to the voltage standard deviation, σ_{vn} through the maximum transition slope, i.e.,

$$\sigma_{\tau,1}^{\ 2} = \sigma_{vn}^{\ 2}\left(\frac{C_{node}}{I_{tail}}\right)^2 \tag{6.2}$$

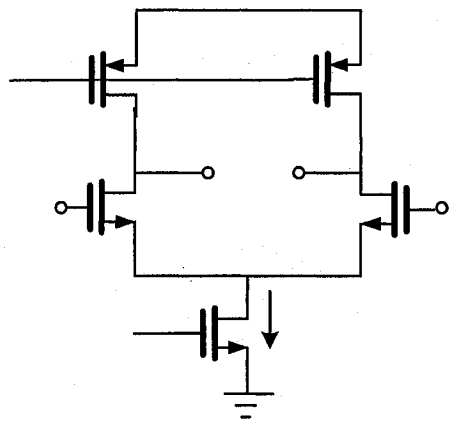


Figure 48 Differential delay stage in the ring oscillators of [54]

Assuming that voltage noise variance is kT/C [58], the single stage jitter, normalized to the stage delay, is

$$\frac{\sigma_{\tau,1}^{\ 2}}{t_d^{\ 2}} \approx \frac{\sigma_{vn}^{\ 2}}{V_{swing}^{\ 2}} \approx \frac{kT}{C_{node}} \cdot \frac{\xi^2}{(V_{GS}-V_T)^2} \tag{6.3}$$

Where V_{GS}-V_T is the gate-source overdrive of the differential pair in the balanced state, and ξ is a factor to account for the differential shares of the differential pair and load transistors. Therefore, ξ is a topology-dependent parameter.

The cycle-to-cycle jitter can be calculated from the stage jitter. For a ring oscillator with N stages, assuming independent noise sources, the cycle-to-cycle jitter due to all the stages is given by the sum of variances [58], i.e.

$$\frac{\sigma_{\tau,CTC}^{\ 2}}{T^2} = \sigma_{\tau,1}^{\ 2} \cdot \frac{T}{t_d} = \frac{kT}{I_{tail}} \cdot \frac{a_v \xi^2}{(V_{GS}-V_T)^2} \cdot T \tag{6.4}$$

Where a_v is the small single gain of the stage, T is the period of the oscillation and $\sigma_{\tau,CTC}$ is the cycle-to-cycle jitter of the output.

$$a_v = g_m R_L = \frac{V_{swing}}{V_{GS} - V_T} \tag{6. 5}$$

The phase noise spectrum may also be calculated using the method in [58]:

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{a_v \xi^2 kT}{I_{tail}(V_{GS} - V_T)}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{6. 6}$$

Which shows the trade-offs among power consumption, number of stages, frequency, and gate overdrive for long channel, differential CMOS ring oscillators.

A frequency domain LTI approach can be used to model the phase noise in differential ring oscillators with a small number of stages [60]. In this approach, a short differential oscillator is modeled using its equivalent small-signal single-ended counterpart shown in Figure 49. It is assumed that stages neither turn off nor their trans-conductance change dramatically during one cycle of operation. An expression for the phase noise due to the channel noise is obtained:

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{16}{3}\frac{kTR}{V_{swing}{}^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] = 10 \cdot \log\left[\frac{8}{3}\frac{kT}{P_{load}}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{6. 7}$$

Where P_{load} is the power dissipated in the load device.

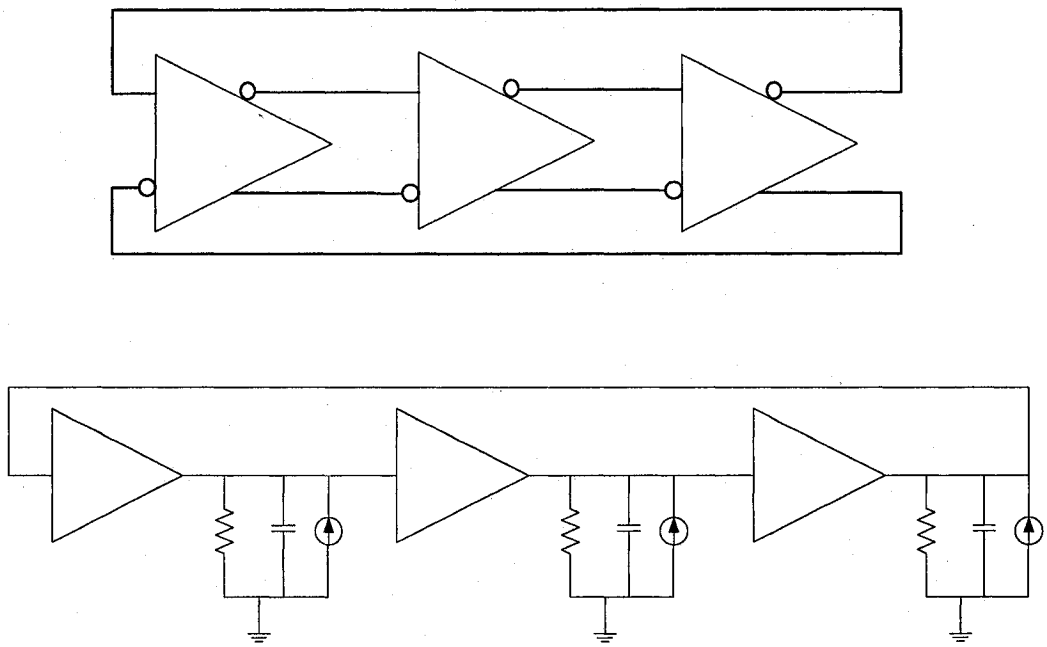


Figure 49 Three stage differential ring oscillator and its small signal single-ended equivalent circuit

The center frequency of the oscillator is [61]

$$f_{osc} = \frac{1}{2N \cdot t_d} \cong \frac{I_{tail}}{2N \cdot C_{node} \cdot V_{swing}} \tag{6.8}$$

The term I_{tail}/V_{swing} is actually the effective resistance of the triode load. The PMOS load is given by

$$R_L = \left(\frac{dI_d}{dV_{DS}}\right)^{-1} \cong \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)\left[V_{GS} - V_T - V_{DS}\right]} \tag{6.9}$$

If the load is well biased into triode region so that its output resistance is not too non-linear, the small signal resistance at the midpoint of the V_{DS} vs. I_D curve is a good representation of the average resistance. This is the point where $V_{DS}=V_{swing}/2$.

The load capacitance can be reasonably modeled as a constant times WLC_{ox}, where the constant is made up of the contributions of gate-source, drain-bulk and gate-drain of the capacitances at the output.

$$C_{node} = K_L \cdot WLC_{ox}$$

Now we can get from (6.10)

$$f_{osc} = \frac{1}{2N} \cdot \frac{\mu}{K_L \cdot L^2} \cdot \left[(V_{GS} - V_{TP}) - V_{swing} / 2 \right]$$

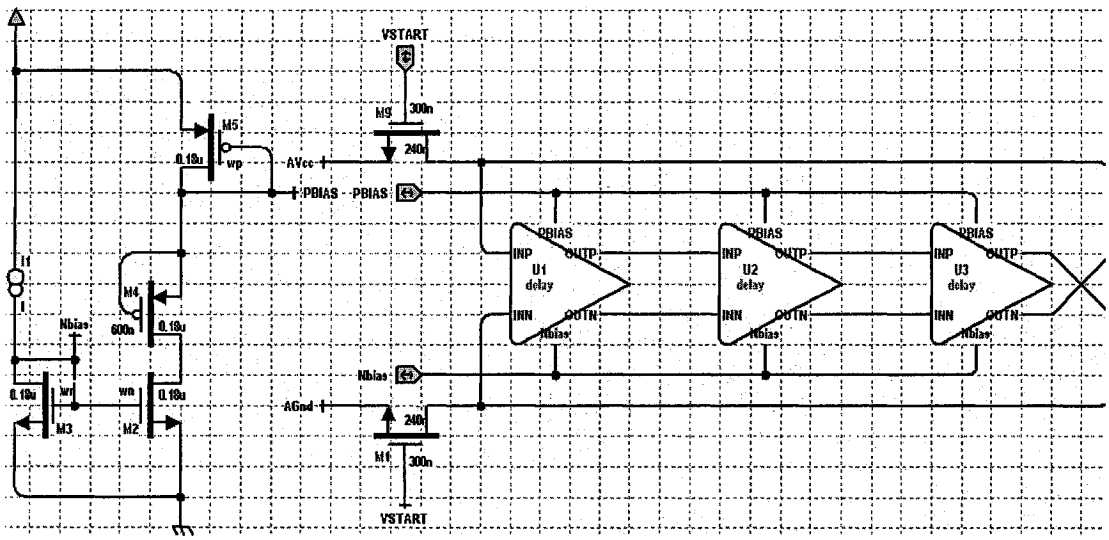
This equation shows some trade-offs in the ring-oscillator design. First, the frequency depends on the number of stages. A maximum frequency is attained with as few stages as possible. The minimum number is three. The next factor influencing the output frequency is the capacitance factor K_L. When A is smaller K_L results in a higher maximum output frequency. Also the oscillating frequency is dependent on technology, which is shown in the term μ / L^2. Moving to a process with narrower gate lengths gives a rapid improvement in the maximum output frequency proportional to the scaling factor squared.

6.2 Simulation results

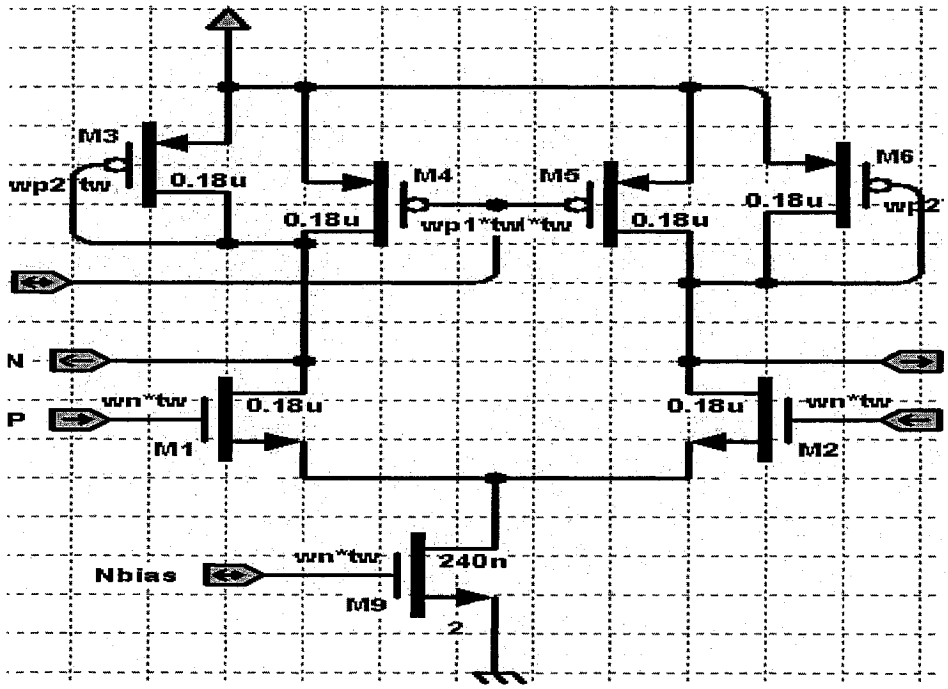
6.2.1 Schematic simulations

6.2.1.1 Simulation configuration

The simulation configuration is shown in Figure 50(a). The load of the delay cell (Figure 50 (b)) is PMOS transistors in triode region parallel with PMOS transistor connected as diode. It provides good control over delay and high dynamic supply noise rejection.



(a)



(b)

Figure 50 (a) simulation configuration of the Ring VCO (b) the schematic of the delay cell

6.2.1.1 Transient simulation

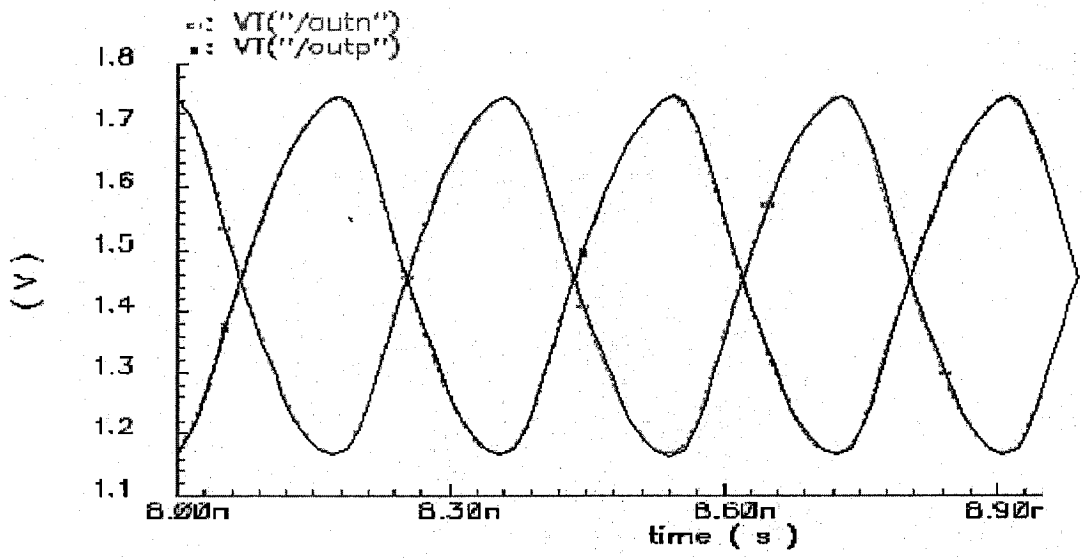


Figure 51 transient simulation result of the ring oscillator

Table 17 Center frequency shift at technology variation

Technology variation	No technology variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Center frequency (GHz)	2.79	2.395	2.755	2.845

As illustrated above, the frequency shows a square law dependency on length of the gate. It could be easily seen from the simulation results with technology variation. Using $f_{osc} = \frac{1}{2N \cdot t_d} \cong \frac{I_{tail}}{2N \cdot C_{node} \cdot V_{swing}}$, we could predict the oscillating frequency as 2.8GHz.

6.2.1.2 Tuning Range Simulation

Following the same method of predicting the oscillating frequency, we could predict the tuning range of 2.5GHz~3.2GHz. The schematic level tuning range is from 2.45GHz to 3.13GHz. It is shown in Figure 52.

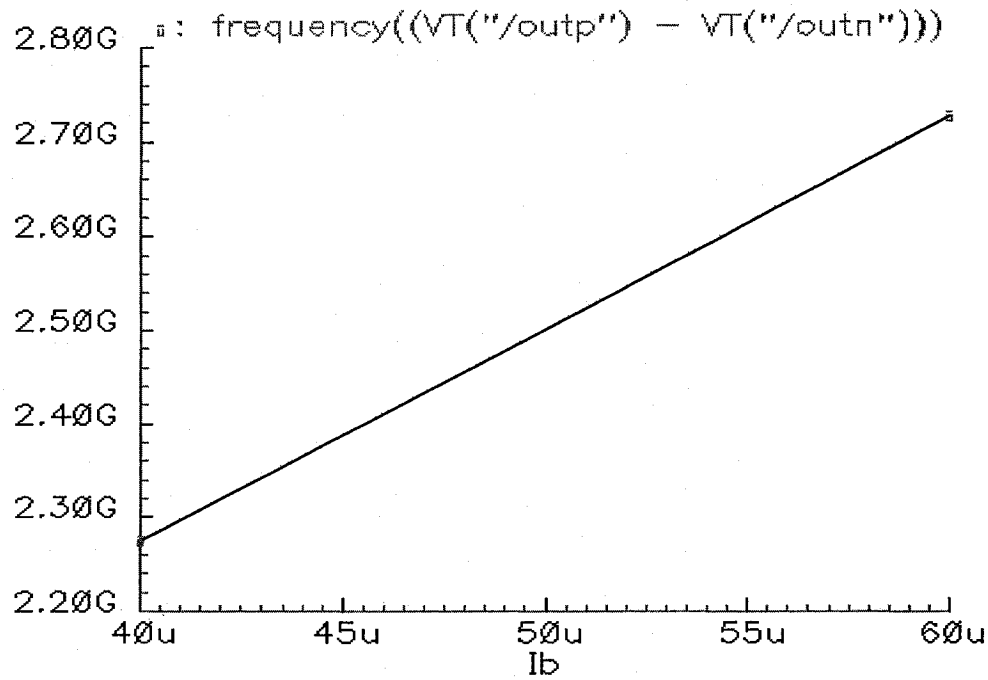


Figure 52 Tuning range of the ring oscillator

Table 18 Tuning range shift at technology variation

Technology variation	No technology variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Tuning range (GHz)	2.45~3.13	2.01~2.78	2.41~3.10	2.50~3.19

6.2.1.3 Phase Noise Simulation

Using the equation:

$$S_{\Phi}(\Delta f) = \frac{f_0}{(\Delta f)^2}\left(\frac{\Delta t}{T_0}\right)^2 = \frac{f_0}{(\Delta f)^2}\cdot\frac{kT}{T_{tail}}\cdot\frac{a_v\xi^2}{2(V_{GS}-V_T)}\cdot\frac{1}{T_0}$$

We can predict the phase noise at the 3MHz offset

$$S_{\Phi}(3MHz) = \frac{2.5\times10^{9}}{(3\times10^{6})^{2}} \cdot \frac{1.38\times10^{-24}\times273}{1.93\times10^{-3}} \cdot \frac{1.18\times9}{2\times0.85} \cdot \frac{1}{4\times10^{-10}} = 8.36\times10^{-13} = -121 dBc/Hz$$

The simulation result of phase noise is shown in Figure 53.

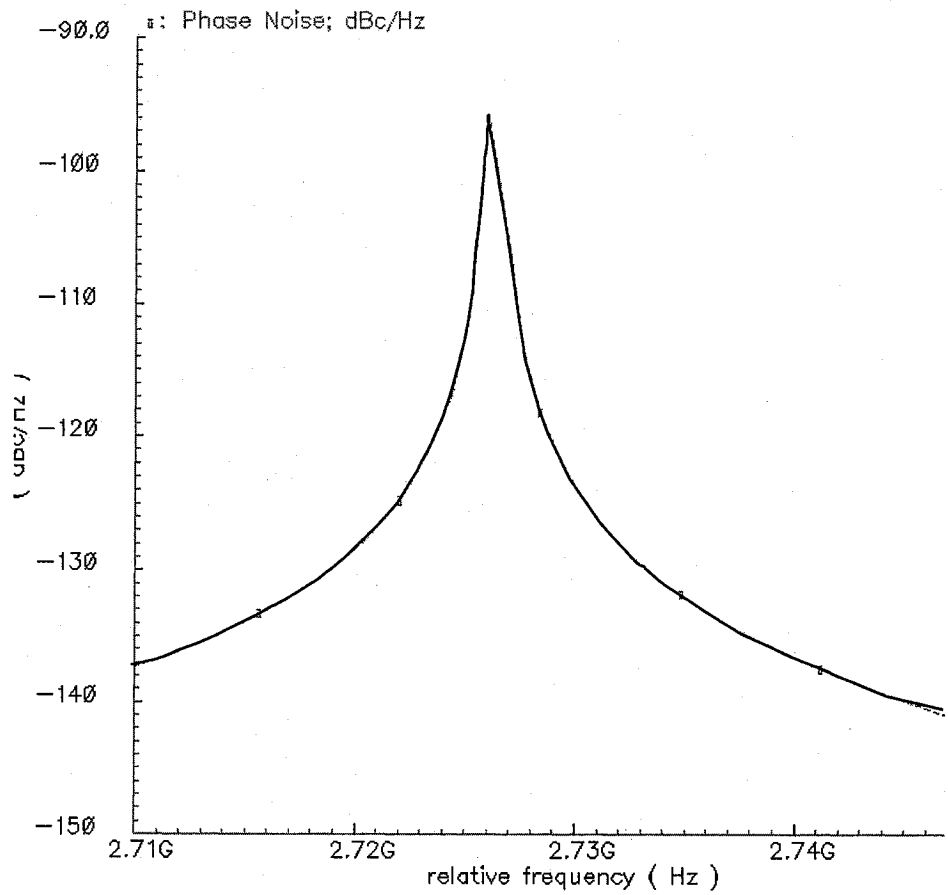


Figure 53 Phase noise of the ring oscillator

Table 19 Phase noise shift at technology variation

Phase noise (dBc/Hz)	No technology variation	Length increased by 10%	Width increased by 10%	Width decreased by 10%
Phase noise @600kHz offset	--107.2	-110.1	-102.8	-102
Phase noise @2MHz offset	-118.5	-119.6	-115.5	-111.8
Phase noise @3MHz offset	-122.2	-123.2	-119.5	-115.5

The power consumption is 20.45mW.

6.2.2 Post-layout Simulations

6.2.2.1 Layout of the whole chip

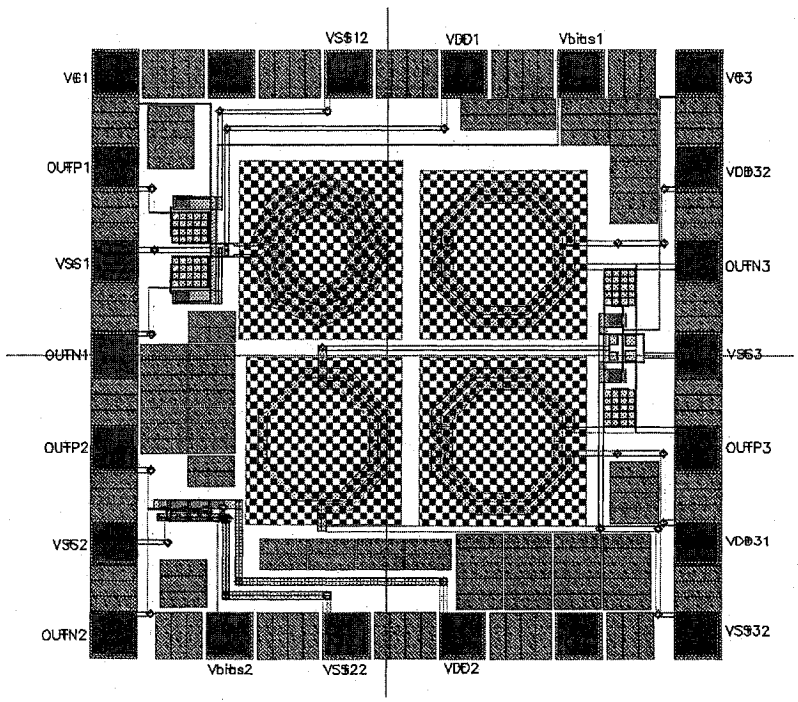


Figure 54 Layout of the whole chip

This chip is composed of three VCOs. The top left is the complementary LCVCO. The bottom left is the ring VCO. The rest is the sub-threshold LCVCO. The layout area is about 1cm*1cm. We could see the inductors take most of the areas. Inductors are covered by layer, which will forbid anything below the inductors. The out pads are arranged as Signal-Ground-Signal. The input signals are all DC signals. To avoid possible leakage of noise from the adjacent digital sub-system in a system on chip environment, the metal of VDD and VSS are made wide so that the parasitic capacitance will filter away the high frequency noise.

6.2.2.2 Post-layout transient simulation

The transient output of the ring VCO is shown in Figure 55. We could see that it is faster than schematic level simulation results. This is because when in the schematic level, for each transistor, the junction capacitors of the drain and source are both calculated. However, in the layout, because most of the drain and source of the fingered transistors are overlapped, the junction capacitance becomes almost halved. Combined with the gate capacitance and the parasitic capacitance in the connection wires in the layout, the values of the C_{node} in schematic and layout are 0.53pF and 0.37pF, respectively.

After extraction from the layout, the transient simulation result of the ring VCO is shown in Figure 55. The oscillating frequency is 3.2GHz, and the output amplitude is more than 600mV (peak-peak). Using parametric analysis, the post-layout tuning range of the ring VCO is from 2.83GHz~3.64GHz. It is shown in Figure 56. The post-layout phase noise performance of the ring VCO is shown in Figure 57 The phase noise at 600kHz, 2MHz, and 3MHz offset from the center frequency is -103.9dBc/Hz, -

120.3dBc/Hz and -124.4dBc/Hz, respectively. The phase noise performance is qualified for Bluetooth application. The power consumption is 20.45mW

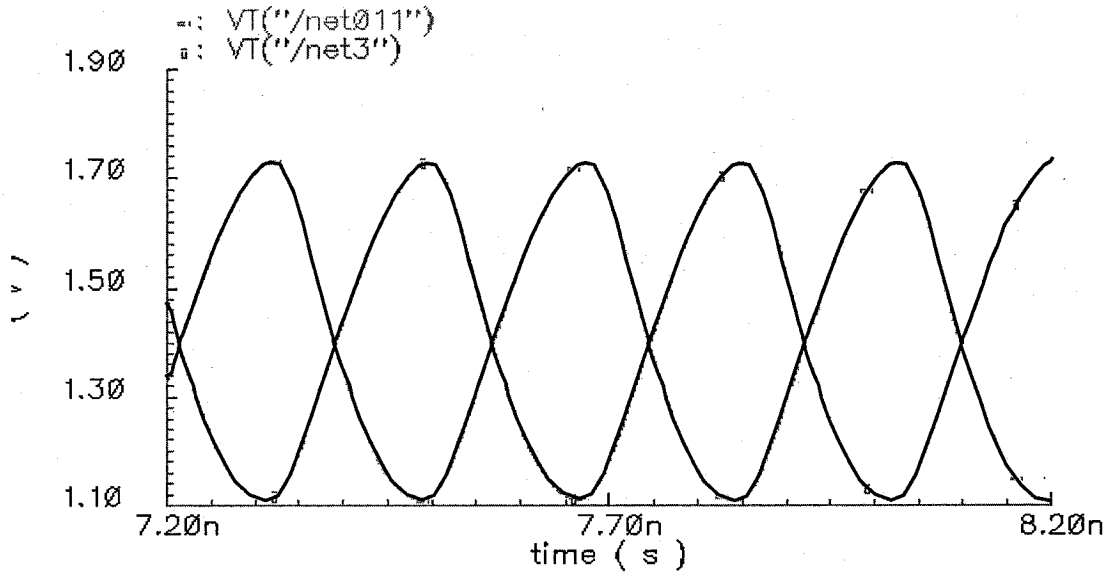


Figure 55 post-layout transient simulation result of the ring VCO

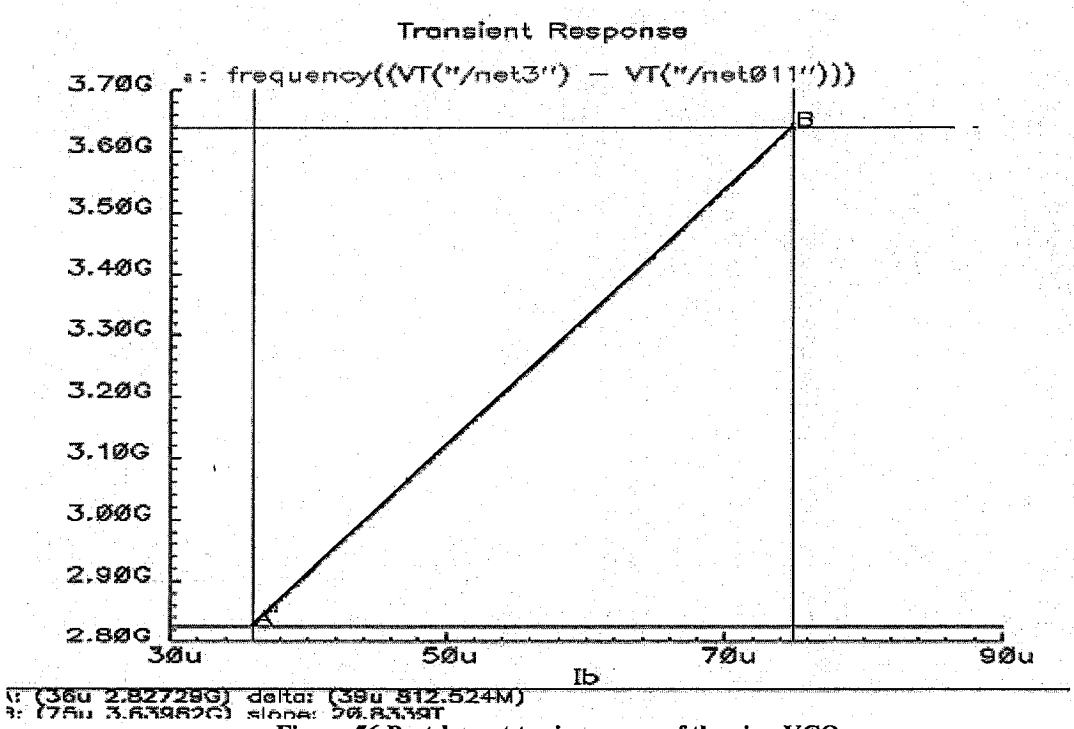


Figure 56 Post-layout tuning range of the ring VCO

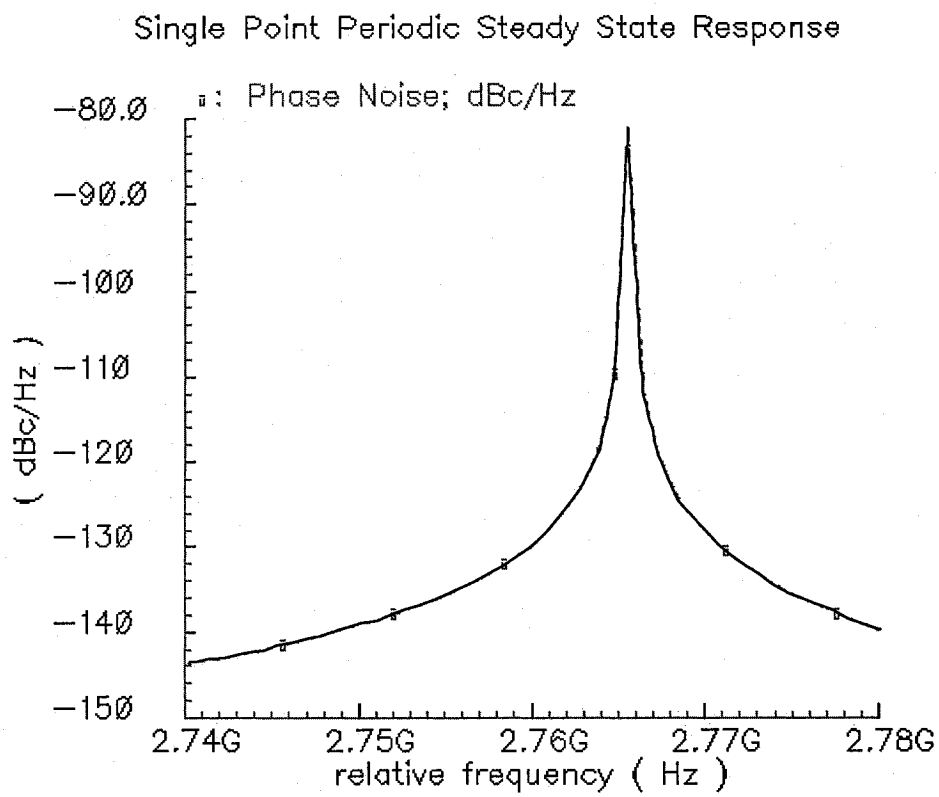


Figure 57 Post-Layout Phase Noise Performance of the ring VCO

Table 20 Post-layout Phase Noise of the ring VCO

	Phase noise @600kHz offset	Phase noise @2MHz offset	Phase noise @3MHz offset
Phase noise (dBc/Hz)	-103.9	-120.3	-124.4

6.3 Summary

In this chapter, the design and simulation of the ring VCO are accomplished. To meet the phase noise performance in the Bluetooth application, large power is consumed.

Using the same FOM definition, we get the FOM of this design is:

$$
\begin{aligned}
FOM &= 20\log_{10}(freq) - PhaseNoise - 10\log_{10}(Power) \\
&= 20\log_{10}(2.73\times10^{9}) + 107.2 - 10\log_{10}(1.8\times11.36\times10^{-3}) \\
&= 313
\end{aligned}
$$

7 Conclusion

In the previous chapters, we've discussed different topologies of oscillators, the design of varactors and inductors, and designed three VCOs. The achievements and future work are summarized below.

7.1 Achievements

To meet the VCO phase noise specifications for Bluetooth applications, three VCO topologies are compared. The oscillating frequency, tuning range and phase noise performance are analyzed. The contributions of each component to the finial performances are studied. Some design hints are included. Experiments including the schematic level simulation and post-layout simulation are accomplished. Some simulation results are repeated in Table 21 below.

Table 21 The simulation results of the three VCOs

	CMOS LC VCO	Sub-threshold LC VCO	Ring VCO
Tuning range (GHz)	2.588~3.235	2.471~2.763	2.45~3.13
Phase noise @600KHz offset (dBc/Hz)	-115	-122.9	-107.2
Phase noise @ 2MHz offset (dBc/Hz)	-127	-132.1	-118.5
Phase noise @ 3MHz offset (dBc/Hz)	-131	-135.5	-122.2
Power consumption (mW)	1.08	0.3	20.45

Compared to other research results, the FOM is shown in Figure 58. The definition of this FOM includes the oscillating frequency, the phase noise performance and power consumption; however, it doesn't include the chip area. We could see our sub-threshold LCVCO has the best FOM, and at the time, it takes the biggest chip area.

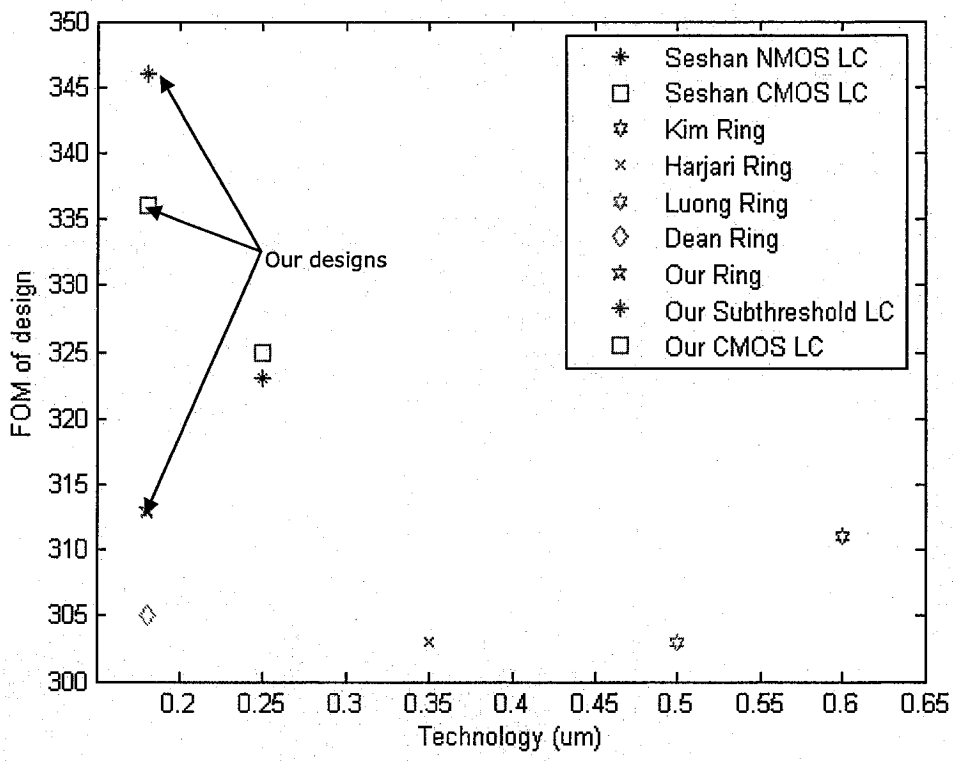


Figure 58 Comparison of the FOM between my work and others

7.2 Future work

In this study, we've considered the VCO core only. If we want to implement and measure the results, we should design output buffers, study the effects of pads and pins, and the effects of the test equipments also. The signal integrity should be taken into account too.

In Chapter 1, we've discussed the LC VCO using switched inductor for tuning. We can assume a linear control voltage to the gate of the MOS and change it continuously. Same may be done for VDS of the transistor. This will be like a varistor (like varactor) controlled VCO.

The design target of this study is to meet Bluetooth specifications; we could apply VCO to many other fields, like neuronal network etc.

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Appendix A: CMOSP18 ASITIC technology files

```
; CMC CMOSP18 technology files for ASITIC
; Last modified: May 10, 2000

<chip>

      chipx = 512              ; dimensions of the chip in x direction
      chipy = 512              ; dimensions of the chip in y direction
      fftx = 128               ; x-fft size (must be a power of 2)
      ffty = 128               ; y-fft size
      TechFile = cmosp18.tek   ; the name of this file
      TechPath = /private/rabinr/h_yao    ; the pathname of the data
files
      freq = 2.4               ; frequency of operation [GHz]
      eddy = 0

<layer> 0                      ; Bulk Substrate
      rho = 10                 ; Resistivity:  ohm-cm
      t   = 733                ; Substrate Thickness:  microns
      eps = 11.7               ; Permitivity:  relative

<layer>     1              ; Oxide Layer
      rho = 1e7            ; Resistivity: ohm-cm, insulator in this case
      t = 8.7              ; thickness  (microns), doesn't make any diff
      eps = 3.9            ; Permitivity:  relative

<metal> 0
        layer = 1              ; in oxide layer
        rsh = 78               ; Sheet Resistance Milli-Ohms/Square
        t   = 0.53             ; Metal Thickness (microns)
        d = 1.05               ; Distance from bottom of layer (microns)
        name = metal1          ; name used in ASITIC
        color = red            ; color in ASITIC

<metal> 1
        layer = 1
        rsh = 78
        t = 0.53
        d = 2.38
        name = metal2
        color = LightSkyBlue1

<metal> 2
        layer = 1
        rsh = 78
        t = 0.53
        d =  3.71
        name = metal3
        color = Yellow

<metal> 3
        layer = 1
        rsh = 78
        t = 0.53
        d =  5.04
```

```
        name = metal4
        color = orange

<metal> 4
        layer = 1
        rsh = 78
        t = 0.53
        d =  6.37
        name = metal5
        color = forest

<metal> 5
        layer = 1
        rsh = 36
        t = 0.99
        d =  7.7
        name = metal6
        color = silver

<via> 0                         ; metal 1 to metal 2
        top = 1                 ; via connects up to this metal layer
        bottom = 0              ; via connects down to this metal layer
        r = 6.4                 ; resistance per via
        width = 0.26            ; width of via
        space = 0.26            ; minimum spacing between vias
        overplot1 = .2          ; minimum dist to substrate metal
        overplot2 = .2          ; minimum dist to metal 1
        name = via12            ; name in ASITIC
        color = cadetblue       ; color in ASITIC

<via> 1                         ; metal 2 to metal 3
        top = 2
        bottom = 1
        r = 6.4
        width = 0.26
        space = 0.26
        overplot1 = .2
        overplot2 = .2
        name = via23
        color = lime

<via> 2                         ; metal 3 to metal 4
        top = 3
        bottom = 2
        r = 6.4
        width = 0.26
        space = 0.26
        overplot1 = .2
        overplot2 = .2
        name = via34
        color = cream

<via> 3                         ; metal 4 to metal 5
        top = 4
        bottom = 3
        r = 6.4
        width = 0.26
```

```
        space = 0.26
        overplot1 = .2
        overplot2 = .2
        name = via45
        color = purple

<via> 4                          ; metal 5 to metal 6
        top = 5
        bottom = 4
        r = 2.54
        width = 0.26
        space = 0.26
        overplot1 = .2
        overplot2 = .2
        name = via56
        color = purple
```

Appendix B: HSPICE file for inductor modeling

```
* broadband model of L

.option acct nomod post=2

.net v(p2) vin rout=50 rin=50

vin p1  0 AC 1

L       p1      3       Ls
R       3       p2      Rs
Cs1     p1      1       Cs1
Cs2     p2      2       Cs2
Rb1     1       0       Rb1
Rb2     2       0       Rb2
Cb1     1       0       Cb1
Cb2     2       0       Cb2
Cbr     p1      p2      Cbr
Rc      1       2       Rc

.param
+ Ls = OPT1(1.2n,.1n,100n)
+ Rs = OPT1(1,.1,10k)
+ Rb1 = OPT1(1.8,.1,100k)
+ Rb2 = OPT1(1.8,.1,100k)
+ Cs1 = OPT1(0.027p,.001p,10p)
+ Cs2 = OPT1(0.015p,.001p,10p)
+ Cbr = OPT1(.002p,.0001p,10p)
+ Cb1 = OPT1(0.037p,.001p,10p)
+ Cb2 = OPT1(0.035p,.001p,10p)
+ Rc = OPT1(2,.1,10k)

.AC data=measured optimize=opt1
+ results=comp1,comp2,comp3,comp4,comp5,comp6,comp7,comp8
+ model=converge
.model converge opt relin=1e-4 relout=1e-4 close=10 itropt=30
.measure ac comp1 err1 par(s11m) s11(m)
.measure ac comp2 err1 par(s11p) s11(p)
.measure ac comp3 err1 par(s12m) s12(m)
.measure ac comp4 err1 par(s12p) s12(p)
.measure ac comp5 err1 par(s21m) s21(m)
.measure ac comp6 err1 par(s21p) s21(p)
.measure ac comp7 err1 par(s22m) s22(m)
.measure ac comp8 err1 par(s22p) s22(p)
.ac data=measured
*.print par(s11r) s11(r) par(s11i) s11(i)
*.print par(s12r) s12(r) par(s12i) s12(i)
*.print par(s21r) s21(r) par(s21i) s21(i)
*.print par(s22r) s22(r) par(s22i) s22(i)
*.print z11(r) z11(i) z11(m) z11(p)
*.print z22(r) z22(i) z22(m) z22(p)
*.print z12(r) z12(i) z12(m) z12(p)
*.print z21(r) z21(i) z21(m) z21(p)
```

```
.data measured
FREQ     s11m     s11p     s12m     s12p     s21m     s21p     s22m     s22p

1.000e+08  4.708e-02  2.126e+01  9.558e-01  -1.586e+00 9.558e-01  -
1.586e+00 4.750e-02  21.59029
1.100e+09  2.093e-01  6.618e+01  9.166e-01  -1.709e+01 9.166e-01  -
1.709e+01 2.085e-01  64.92491
2.100e+09  3.884e-01  5.874e+01  8.299e-01  -3.140e+01 8.299e-01  -
3.140e+01 3.828e-01  57.20321
3.100e+09  5.369e-01  4.807e+01  7.175e-01  -4.427e+01 7.175e-01  -
4.427e+01 5.250e-01  46.39028
4.100e+09  6.483e-01  3.809e+01  5.985e-01  -5.588e+01 5.985e-01  -
5.588e+01 6.299e-01  36.3496
5.100e+09  7.243e-01  2.912e+01  4.804e-01  -6.622e+01 4.804e-01  -
6.622e+01 7.002e-01  27.37482

.enddata
.param freq=100MEG,s11m = 0 , s11p = 0, s12m = 0, s12p = 0, s21m =0,
+s21p =0, s22m =0 , s22p = 0
.end
```