Design, Fabrication and Characterization of RF MEMS Inductors and Switches

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Abstract

Design, Fabrication and Characterization of RF MEMS Inductors and Switches

Alireza Hajhosseini Mesgar

MicroElectroMechanical Systems (MEMS) concept covers different miniature devices in different disciplines, including but not limited to biological, chemical, electrical, fluidic, magnetic, optical, and thermal applications. The driving forces for the miniaturization of systems include cost, size, speed, weight, precision and reliability while providing an effective interface between the macro and micro world. In this thesis RF MEMS switches and inductors are studied.

Initially, the background of MEMS, RF MEMS and fabrication technologies are introduced. Then switch and inductor are introduced. Theory, different configurations, designs, and fabrication technologies are considered. Finally proposed designed components are given. Each design is verified through software simulations.

Modeling and simulation is the next step. Switches are simulated by MATLAB. Inductors are designed using MATLAB and simulated by ADS-Momentum.

Switches are fabricated in the Multi-User MEMS Process (MUMPs) which uses a surface micromachining technique. Inductors are fabricated in both MUMPs and CMOS processes. MUMPs chips require a simple post-fabrication processing that is soaking them in hydrofluoric acid to remove the sacrificial silicon oxide layer For CMOS inductors, bulk-micromachining required post-processing is performed after fabrication.

Device characterization is done using the appropriate methods. For switches, in order to find pull-in voltage, DC test is performed, but for inductors, to find the variation of impedance with frequency, RF measurement using on-wafer probes and vector network analyzer is done. Then measurement results are given and are interpreted.

Finally, conclusions, some suggestion to improve the designs, and future work are given.

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1. Introduction

1.1 Motivation

Expansion and development of fixed, mobile, wired and wireless telecommunications networks and devices and introduction of multiple standards drives the need for more efficient components. In mobile wireless communication devices, parts that are smaller, operate in a broader/narrower frequency range (depending on the application), support multiple standards, and consume less power, lead to increased efficiency and decreased prices. MEMS (MicroElectroMechanical Systems) technology (also known as Microsystems) can address these requirements.

Many components in a radio frequency (RF) device can be replaced by their MEMS counterparts that exhibit superior performance. These components are mainly concentrated in RF front-end block that contains duplexers, impedance matching networks, filters, multiplexers, mixers, oscillators, phase shifters, amplifiers [1-4] that they themselves contain passive microwave components, transmission lines, capacitors, inductors for active and passive circuits, switches, resonators, and components.

This project is part of a bigger project on RF MEMS filters that involves RF MEMS capacitors [5-6], resonators [5], and inductors and switches which are investigated in this work.

1.2 RF MEMS Inductors

Inductors are widely used in radio frequency integrated circuits (RFICs). They are used in passive tuning circuits (filters), as high impedance RF chokes, and also being used in

matching networks, oscillators and voltage-controlled oscillators (VCOs) [7-8], and amplifiers.

Planar processes that are utilized to fabricate RFICs create some problems. The trace capacitance to ground and the substrate resistivity lower both the self-resonance frequency and quality factor of the inductor. These effects can be diminished in some extent by optimizing the physical layout of the inductor.

Substrate micromachining methods can be utilized to improve the quality factor and resonance frequency of the inductor by removing the substrate beneath the inductor so the parasitic capacitance of substrate is reduced.

1.3 RF MEMS Switches

Switches and switching have a key role in RF systems. For example they are used in blocks such as phased array antennas, tunable matching networks, transmit/receive switches and switching matrices. The hardware overhead can reduce by using reconfigurable blocks (for different condition/frequencies/standards). Switches determine the signal path in this type of circuits. MEMS switches, in addition to being small, have very good RF properties in terms of insertion loss, isolation, power consumption, and linearity that makes them a desirable alternative [9-10].

1.4 Thesis Outline

This thesis focuses on RF MEMS switches and inductors. Different aspects of MEMS RF switches and inductors are discussed.

In chapter 2, MEMS and RF MEMS are reviewed and different fabrication methods for MEMS devices are explained.

.In chapter 3 and 4 the design and simulation of switches and inductors are presented. MEMS switches are introduced and compared with electronic switches. A switch design in MUMPS is given and modeled in MATLAB. Switch layouts are given, too. Then integrated inductors are introduced. Different layouts, models and design equations are given. Several spiral inductors are designed in MATLAB and then some of them are selected for fabrication in CMOS and MUMPS processes. Designed inductors are simulated in ADS Momentum and their layouts are given.

In chapter 5 fabrication details of designed MEMS devices are described. Then performed silicon bulk micromachining (post-processing) steps for CMOS process are given

In chapter 5 characterization methods are introduced and test procedures are explained. Then measurement results are discussed.

Finally in chapter 6, conclusions are highlighted and some future-works to continue this project are suggested.

In appendix 1, least-square estimation method which is used in chapter 6 to estimate the material properties from a set of measured parameters, is presented.

2. Background

2.1 MEMS

2.1.1 What is it?

MEMS stands for "*MicroElectroMechanical Systems*". Some properties can be inferred directly from this name, *Micro* tells that they are miniature devices, *electro* suggests either electricity or electronics or both, *mechanical* introduces the presence of mechanical structures or moving parts, and *System* suggest some degree of complexity. But MEMS concept (that some times is also called *Microsystems, Microstructures*, or *Micromachines*) is more general and covers different miniature devices, including but not limited to biological, chemical, electrical, fluidic, magnetic, optical, and thermal applications. MEMS research involves different disciplines in science and engineering.

The driving forces for the miniaturization of mechanical systems include cost, size, speed, weight, precision and reliability while providing an effective interface between the macro and micro world.

2.1.2 History of MEMS

When in 1959 Richard Feynman [11] in his famous speech, "There is plenty of room at the bottom" introduced the idea of miniaturization, he proposed only a few applications that he dreamed about, and of course they weren't realizable at that time.

But now, many miniature devices in scale of microns or even less are implemented, and many of Feynman's imaginations are actualized thanks to advances in fabrication processes for MEMS. One of the first silicon pressure sensors was isotropically micromachined by Honeywell [12] in 1962. Crystal orientation etch-rate dependency led

to more precise definition of structures and increased interest. Anisotropic etching was introduced in 1976 [13]. In the 1960s the first surface michromachined structures using metal mechanical layers were presented [14]. These are a few examples of early years MEMS devices. In the last two decades of twentieth century MEMS research has boomed in the world and has lead to thousands of different devices in different application areas. Now MEMS is reaching slowly to maturity but still there aren't many MEMS devices commercially available in the market. Cost and reliability are two limiting factors. Commercialization is the new challenge that MEMS industry is facing with.

2.1.3 Fabrication and Materials

Although MEMS researchers take advantage of VLSI processes, the MEMS processes are not standardized like IC fabrication processes that are mature and well established.

The conventional IC fabrication process that is based on photolithography and chemical etching is not directly suitable to realize three-dimensional MEMS structures, but after a few post-processing steps, it is possible to have MEMS devices and digital and analog circuitry on the same chip. The idea of integrated MEMS and electronics is very promising for many applications, but with some considerations.

The IC fabrication process creates a planar (2D) structure. To shape the third dimension of a 3D MEMS device, bulk micromachining and surface micromachining techniques are designed [15].

In surface micromachining, there are two types of layers; structural layers to make the structure in it and sacrificial layers that separate structural layers but will be removed during later steps or at the end of the fabrication. The process of sacrificial layer removal

is called the *release* process. There is a problem called *stiction* associated with structure release. The nature of stiction problem and the solutions are given later in this chapter.

In bulk micromachining, the substrate (usually silicon) is etched away by dry or wet methods, isotropically or anisotropically. This way the substrate under certain devices is removed to achieve some design goals. Bulk-micromachining will be explained thoroughly later on.

It is also possible to combine bulk micromachining and surface micromachining techniques.

Similar to ICs, silicon is the key material used to build MEMS structures. Also depending on the application, other semiconductor materials like GaAs [16] as well as metals, ceramics, polymers (polyimides, etc.) [17-18], and composites are used.

Another process, namely LIGA, is used to create 3D high aspect ratio structures on substrate surface [19].

2.2 MEMS Devices and Applications

MEMS devices in contrast to similar normal-sized devices are very tiny, occupy a small area on the chip, and consume negligible power. These unique properties make them attractive for almost every application, but especially for applications that either space (area) or power is a limiting factor such as portable devices, wireless communications, and defense systems. Handsets, base stations (cell phone industry) and satellites (cellular communications) are a few of them.

There are numerous possible applications for MEMS. They are used in automotive and aerospace industries, military, medical, telecommunications (RF-MEMS), and many other industries.

For example, MEMS devices serve as impact sensors in the accelerometers of automobile airbags [20], as micronozzles in commercial inkjet printers (Figure 2.1) [21-23], as tiny blood pressure sensors [24], for DNA amplification and identification [25], as temperature sensor [20] and gas sensors [26].

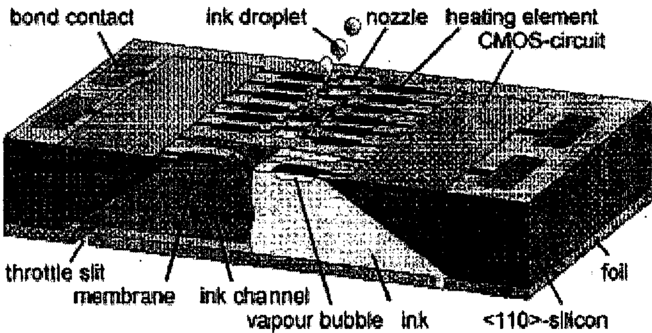

Figure 2.1 Backshooter Printhead [23]

2.3 RF MEMS Devices

High frequency communication systems are benefiting noticeably from the advent of the RF-MEMS technology. MEMS technology is revolutionizing the RF industry. Electrical components such as inductors and tunable capacitors can be improved significantly compared to their integrated counterparts using MEMS technology. With the integration of such components, the performance of communication systems will be enormously improved, while the total circuit area, power consumption and cost will be reduced.

The manufacturers compete to add more functionality to wireless system equipment. A 3G/4G[1] "smart" phone, PDA, or base station, for example, will require the functionality to support TDMA (Time Domain Multiple Access), CDMA (Code Division Multiple Access), Bluetooth and GSM (Global System for Mobile Communications). A huge increase in component count is required to accomplish this task. Other wireless equipments are facing the same challenge. While the market demands the new functions, it also expects smaller form factors, lower costs and reduced power consumption [1-3, 10].

Discrete passive devices such as RF switches, varactors, high-Q[2] resonators and filters, have been identified as components that can be replaced by RF-MEMS counterparts.

RF-MEMS research can be divides into four categories:

- RF MEMS Switches, Capacitors (Varactors), and Inductors: In this category, inductors are the only devices that are not moving.
- Micromachined Transmission Lines (Microwave Components), High-Q Resonators, Filters, and Antennas (Non-Moving Devices): These devices are fabricated on thin-dielectric membranes or take advantage of bulk micromachining.
- Thin Film Bulk Acoustic Resonators (FBARs) and Filters: In these devices, acoustic resonance in thin films is used. They demonstrate high Qs.

---

[1] Third Generation/Fourth Generation mobile telephone technology

[2] Quality Factor

- RF Micromechanical Resonators and Filters: The mechanical vibrations of small structures are used to achieve high-Q resonances.

2.3.1 RF MEMS Switches

Switches are a fundamental part of many RF and microwave circuits and system functions; for instance tunable matching networks, receive/transmit switches, switching matrices, and phased array antennas/smart antennas. Since MEMS technology provides near ideal switches in terms of power consumption, insertion loss, isolation, and linearity, extensive efforts have been aimed at attaining devices exhibiting both good RF properties and low actuation voltage.

An RF switch has two parts: the actuator (mechanical) part and the electrical part (signal path). The actuation force for mechanical movement can be obtained from electrostatic, magnetic, piezoelectric, or thermal mechanism. In addition, the mechanical switch, as developed by several research groups, is a key component with huge potential in various microwave circuits. The movement of switch could be vertical or lateral. In the electrical part, switch can be placed in series or shunt configurations. There are two types of contacts, metal-to-metal contact and capacitive contact.

Considering the above divisions, 32 different types of RF switches can be built using different actuation mechanisms, movement planes, contact types, and circuit configurations.

Application areas of RF MEMS switches are switching networks, reconfigurable networks, portable wireless systems, and phased arrays in communication and radar systems. Applications include: SPNT (single-pole N-throw) switches for filter and

amplifier selection, $N \times N$ switching matrices, SPDT (single-pole double-throw) and DTDT (double-pole double-throw) routing switches, very high isolation switches (instrumentation), programmable attenuators, phase shifters, reconfigurable matching networks, switched filter banks, and much more [9-10].

2.3.2 RF MEMS (Fixed) Capacitors

Fixed capacitors are frequently employed for dc blocking and in matching networks. Generally two types of passive capacitors are used in microwave circuits, the interdigital and the metal-insulator-metal (MIM) capacitors.

Micromachining is used to reduce the quality factor and parasitic capacitance of interdigital capacitors [27].

2.3.3 RF MEMS Varactors (Variable Capacitors)

With the proliferation of multimode, multi-standard wireless applications, the need for high-quality varactors capable of large tunability range, at low tuning voltage spans, is a rather pressing one. Traditionally the monolithic implementation of functions requiring tunability, such as high-performance voltage controlled oscillators (VCOs), has been prevented by the unavailability of high-quality on-chip varactors. Since the available on-chip varactors exhibit low tuning range and low Q, numerous efforts aimed at applying micromachining to overcome these shortcomings have been undertaken. Accordingly, based on the well-known parallel-plate capacitor equation ($C = \frac{\varepsilon A}{d}$), efforts have aimed at varying one of the three variables: d, the interplate distance, A, the plate area or ε, the dielectric constant.

The development of MEMS varactors has not progressed at the pace of MEMS switches. Their capacitance ratio is normally 1.2-2.5, while standard solid-state varactors have a capacitance ratio of 4-6 and there is ongoing research in order to increase the capacitance ratio. Also, it is hard to build MEMS varactors with capacitance off 5-50 pF, which are needed for 30 to 600 MHz applications.

MEMS capacitors suffer from Brownian, acceleration, acoustic, and bias-noise effects especially for low-spring-constant designs that are necessary for low actuation voltages.

But, there is still a pressing need for MEMS varactors. First they have the potential of very high-Q (100-400) operation, especially at millimeter-wave frequencies. Also, they can be designed to withstand large RF voltage swings and therefore result in very high IIP3[3] tunable networks. MEMS varactors don't need biasing and therefore don't pass current under high-power operations [27-28].

Currently there are three different technologies for building MEMS variable capacitors. The first one is based on the parallel-plate approach (vertical design), and a variable capacitance is achieved by changing the gap between the capacitor plates [28-30]. The second approach is based on an interdigital (horizontal) design: and again, the gap is changed to achieve a variable capacitance [31-32]. The third approach consists of building a fixed capacitance bank and using MEMS switches to select the required total capacitance [33-34].

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[3] Third Intercept point

The switches and capacitors operate with almost the same principles. Switch is a variable capacitor whose capacitance changes from a minimum (open state) to a maximum (closed state).

2.3.4 RF MEMS Inductors

Inductors play an ever-increasing role in RFICs. In addition to being frequently employed in passive tuning circuits or as high impedance chokes, they are used in matching networks, oscillators and voltage-controlled oscillators (VCOs) [7-8], and amplifiers [35]. When fabricated in a planar process, the trace capacitance to ground and the substrate conductivity tend to lower the inductor self-resonance frequency and its quality factor. While optimization of the spiral geometry is essential to tailor the frequency of maximum Q, this only addresses minimization of the trace ohmic-losses and substrate capacitance. Many attempts have been pursued to use conventional processing techniques to diminish the substrate losses created by Eddy currents induced by the magnetic field of the spiral. Various approaches to overcome the limitations of silicon substrate by utilizing bulk micromachining, surface micromachining, or a combination of surface micromachining and self-assembly are addressed.

RF MEMS Inductors, capacitors and varactors fall into the general category of micromachining-enhanced lumped elements. These structures may be fabricated small enough comparing to microwave wavelengths, so that is a good approximation to take their voltages and currents as if they are lumped at a point (i.e. position independent). The lumped-element circuits are small in size, low-cost and have wideband characteristics. These features are particularly important. These elements are usually utilized in high-power oscillators, power amplifiers, and broadband circuit applications (such as

impedance matching). The performance of these elements is limited by the appearance of parasitic effects, which changes the properties of the pure elements into those of a RLC circuit (including the resonance). In the case of an inductor, it will exhibit capacitive behavior above the self-resonance frequency. Since the main source of the parasitic effects is the dielectric substrate supporting the elements, it is natural to aim at improving the situation by eliminating the substrate.

2.3.5 Microwave Components

Various microwave devices can take advantage of MEMS technology. Examples are CMOS micromachined power divider [36] (Figure 2.2), micromachined CMOS coplanar waveguide [37] (Figure 2.3), tapered slot antenna on micromachined photonic bandgap dielectrics [38] (Figure 2.4), and aperture-coupled micromachined microstrip antenna [39].

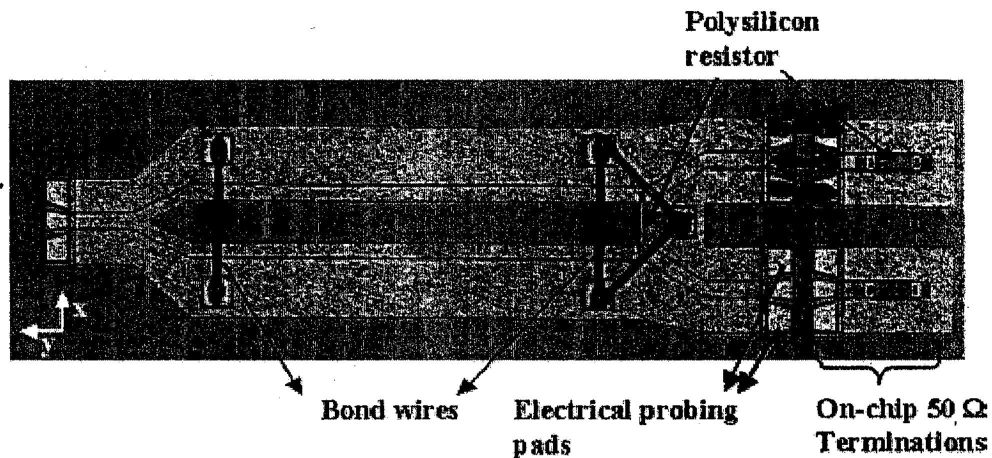

Figure 2.2 CMOS Micromachined Power Divider [36]

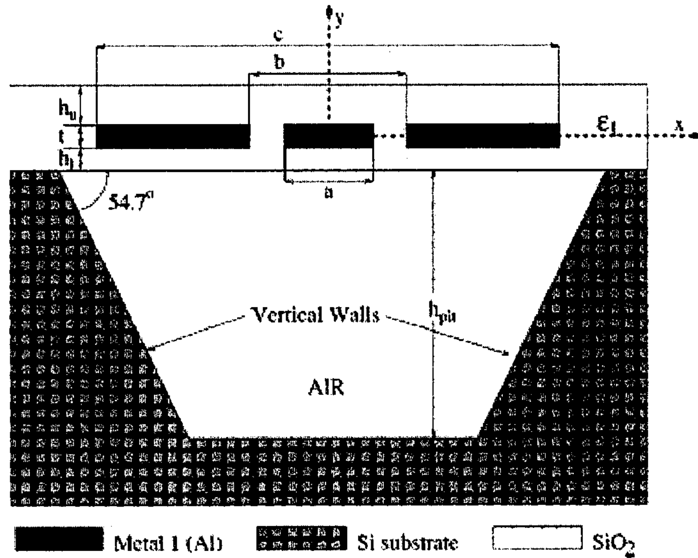

Figure 2.3 Micromachined CMOS Coplanar Waveguide [37]

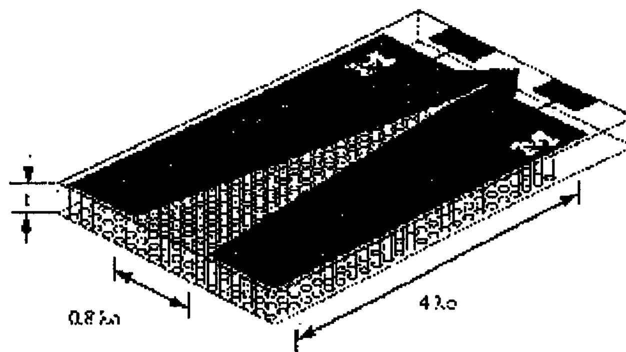

Figure 2.4 Tapered Slot Antenna on Micromachined Photonic Bandgap Dielectrics [38]

2.4 Fabrication Technologies

MEMS devices are fabricated with a variety of methods that is commonly referred to as microfabrication methods. Microfabrication, as practiced in microelectronics and MEMS, is based on planar technologies. Electronic and MEMS devices are fabricated on substrates that are initially flat. Microelectronics industry has invested enormous amounts

of money in the development of wafer-based process technologies in a long time. It is an advantage for MEMS industry to use these mature technologies. Microfabrication methods can be grouped in two main parts, wafer-level processing and pattern transfer.

2.4.1 Wafer-level processes

Wafer-level processes include all the chemical, mechanical, thermal and electrical processes that put new layers on the wafer or put new materials in the wafer or any other layer on the wafer.

Wafers are available in different material and diameters. Single crystal silicon, single crystal quartz, glass, fused (amorphous) quartz, and gallium arsenide are some of them. Round wafers are sold in different diameters, types (n-type or p-type), doping levels and crystal orientations (in the case of single crystal materials).

Wafer-level processes include following processes:

- Wafer preparation and cleaning: This step involves using a standard cleaning procedure such as RCA cleans [40] to remove organic residues and ion contaminations in wafer.
- One of the most attractive properties of silicon is that a high quality oxide can be grown on its surface. If pure oxygen is used as the oxidant, it is called dry oxidation. Oxidation in presence of oxygen and water vapor is called wet oxidation. Dry oxidation creates higher quality oxides than wet oxidation, but it is a slow process. When quality of oxide is not an issue, wet oxidation is used. [41].

  Oxidation is performed in a special furnace as it is shown in Figure 2.5.

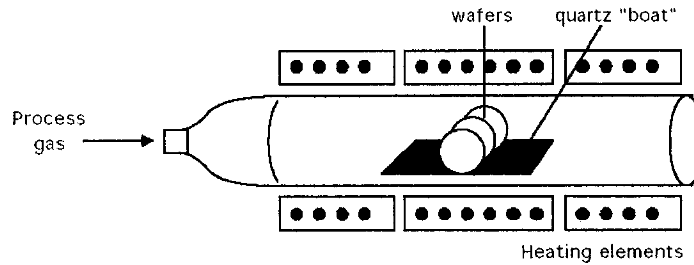

Figure 2.5 Furnace for Silicon Oxidation

- Doping: It is the process which small quantities of impurities are added to semiconductor crystals, thereby modifying the electrical properties of it. Undoped silicon behaves like an insulator while highly doped silicon acts like metals. The conductivity of silicon can be changed in a broad range from very low to very high, all by changing the doping. Impurities are placed in two steps: deposition and drive-in. Dopant atoms are delivered to a region near the wafer surface in drive-in step by ion implantation or by applying it as a gel. Then they are redistributed by diffusion when heated in the a furnace similar to the furnace that is used for oxidation [41-42].
- Thin-Film Deposition: Many microfabrication steps involve deposition and subsequent patterning of a thin film. Depending on the material, thin-films are deposited with a variety of methods such as physical vapor deposition (PVD), chemical vapor deposition (CVD), electrodeposition, and spin casting [19, 41-42].
- Wafer bonding (flip-chip technology) is a method for joining two wafers to create a stacked wafer layer. This method is used both in MEMS fabrication and packaging (for an example see Figure 2.6) [1, 43-45].

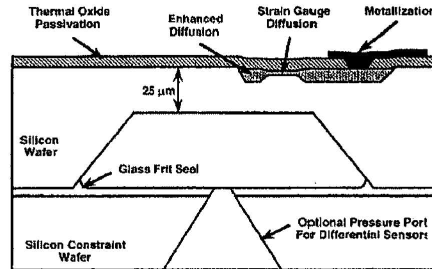

Figure 2.6 Pressure Sensor Using Wafer Bonding for Packaging [44].

2.4.2 Pattern Transfer Methods

ICs and MEMS devices are formed by defining patterns in the various layers created by wafer-level process steps. Pattern transfer consists of two parts: a photo-process, whereby the desire pattern is photographically transferred from an optical plate (mask) to a photosensitive film coating the wafer, and a chemical or physical process of either removing or adding materials to create the pattern. The photo-process is called optical photolithography and the material removal process is called etching.

- Optical photolithography: It is very similar to the photographic process of producing a print from a negative. First the wafer surface is coated by photoresist material (an optically-sensitive polymer) by spin casting. Following spinning, the resist is prebaked at low temperature to remove solvent. A photomask coating the patterns to be transferred is brought into close proximity of the coated wafer. Ultraviolet light is directed through the mask onto the wafer, exposing unprotected portions of the resist, which change their chemical properties due to light exposure. What happens after exposure depends on the chemical specification of the photoresist. Negative photoresist functions like the photographic printing process. Ultraviolet light exposed regions of the photoresist become insoluble in the developer, while the protected regions remain soluble and removed after immersion in the developer. The result is a

transfer of pattern into the photoresist so that the opaque regions of the mask become regions cleared of photoreist. The resist must be hardened by baking it to make it chemically inert. After postbake, the underlying layer may be etched through photoresist windows. Positive photoreist works oppositely to negative photoresist. UV exposed regions become soluble in the developer. After development, the protected regions of resist remain on the wafer [1, 41-42].

Before the photolithography process, the photomask should be designed and made. The mask is designed according to the pattern we want to be transferred. Limitations in the resolution of photolithography and also developers, are expressed as a set of design rules that should be respected to achieve acceptable results.

Figure 2.7 shows a photolithography sequence.

- Etching: Process of removing the material is called etching. Etching can be done in wet or dry environment. Also it can be isotropic or anisotropic.
- Wet Etching: In this method, patterned substrates are immersed in a liquid chemical that attacks exposed region of the substrate and leaves the protected regions alone.
- Dry Etching: Chemically reactive vapors and the reactive species in glow-discharge plasma are highly effective etchants.
- Etch Directionality: It is a measure of the relative etch-rates in different directions, usually vertical versus lateral. Isotropic etching occurs when etch rates are the same in all directions. In anisotropic etching, less lateral etching occurs. When etching a single crystal, certain etchants exhibit orientation-dependent etch-rates [41, 46-47].

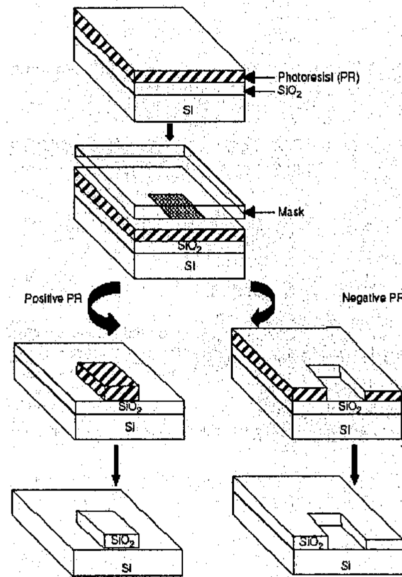

Figure 2.7 A Photolithography and Etching Sequence [1]

2.4.3 The Complete Process

A typical process consists of a sequence of wafer-level and pattern transfer processes. Even for a simple process, many steps of wafer-level and pattern transfer processes are required. The best examples of process technologies are different CMOS processes that are used mainly for analog and digital IC fabrication.

2.5 Micromachining Techniques

Micromachining is a very powerful approach for fabrications of actuators, sensors and microstructures. There are a few true three-dimensional processes capable of yielding arbitrary curved surfaces. Since microfabrication tools are almost applied with successive photolithographic patterning, any 3D aspects of micromachined devices are due to patterning of the 2D layers, interaction of stacked and patterned 2 layers, selective etching of the layers or the substrate, or the use of bending or hinged structures.

Micromachining is performed in two ways: bulk and surface micromachining [15, 19, 41, 48-49].

2.5.1 Surface Micromachining Technique

Surface micromachining [50-51] includes processes that add material above the surface of the substrate. Many of them are more common in typical integrated circuit fabrication than bulk etching. Surface micromachining techniques include:

- Non-Metallic Thin-films: Deposition of thin-films of silicon oxide, silicon nitride, polysilicon, organic materials, etc and etching them after patterning
- Metallic Films: Deposition of gold, copper, aluminum, nickel, chrome, etc and etching them after patterning
- Sacrificial Process: Several interesting processes have been demonstrated that rely on sacrificial materials that are used as forms or spacers to make desired shapes and are later removed. As described by Howe [52], CVD phosphosilicate glass (PSG) etches much faster in HF[4] than thermally grown or undoped oxide, making it an attractive sacrificial layer for undercutting polysilicon structures. Fan, et al. [53] used such a process to realize moving mechanical structures. Oxidized porous silicon etches even faster, making it another very useful sacrificial layer material [54]. Aluminum, photoresist, and a number of other materials common in microfabrication labs can be used as sacrificial or structural layers [1]. The Multi User MEMS Processes (or MUMPS) provided by MEMSCAP company, are surface micromachining processes based on an oxide sacrificial layer that is removed at the end of the process. Three processes offered in MUMPS are PolyMUMPS [55], Metal MUMPS [56] and

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[4] Hydrofluoric Acid

SOIMUMPS [57]. The PolyMUMPS process will be described in detail later in this chapter.

2.5.2 Bulk Micromachining Technique

Many etching methods are available for bulk processing of silicon. Wet and dry etchants are selected on the basis of a large number of characteristics, including selectivity to etch masks, exposed metallization and other materials; availability of etch-stop methods, etch rate, degree of surface roughness created, safety, disposal difficulty, circuit compability, cost, etc. Very often, the etchants are used for post-processing of prefabricated structures that may contain CMOS circuitry and aluminum metallization which places significant constraints on the choice of etchants [58-62].

2.5.3 Other Methods

W. Ehrfeld, et al. at Karlsruhe Germany [63] developed a process called "Lithographie, Galvanoformung, Abformung" (acronymed as LIGA), for lithography, electroplating, and molding that can yield extremely high-aspect-ratio metallic structures thanks to the use of extremely well-collimated synchrotron radiation (X-rays). Steps of LIGA process are shown in Figure 2.8.

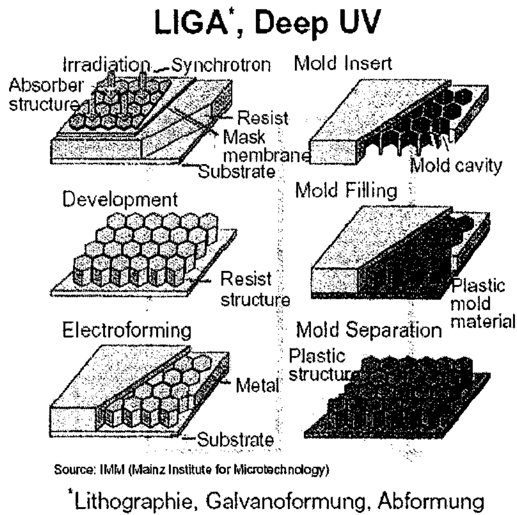

Figure 2.8 LIGA Process Steps

Polyimides that are used in electronics industry [64-65] for different applications can also be used to fabricate MEMS devices [17-18, 66-67].

Flip-chip and Wafer bonding methods are also used to fabricate microstructures [43].

2.6 PolyMUMPS Surface Micromachining Process

2.6.1 Process Definition

PolyMUMPS [55] technology provided by MEMSCAP company is a simple 3 poly, one metal process that gives the designers the opportunity to fabricate their MEMS designs in an affordable way compared to IC fabs. It is a surface micro machining process based on an oxide sacrificial layer that is removed at the end of the process. MUMPS foundry

The layers in the process are shown in Figure 2.9. The layer names and thicknesses are given in Table 2.1 and their electrical properties are given in Table 2.2.

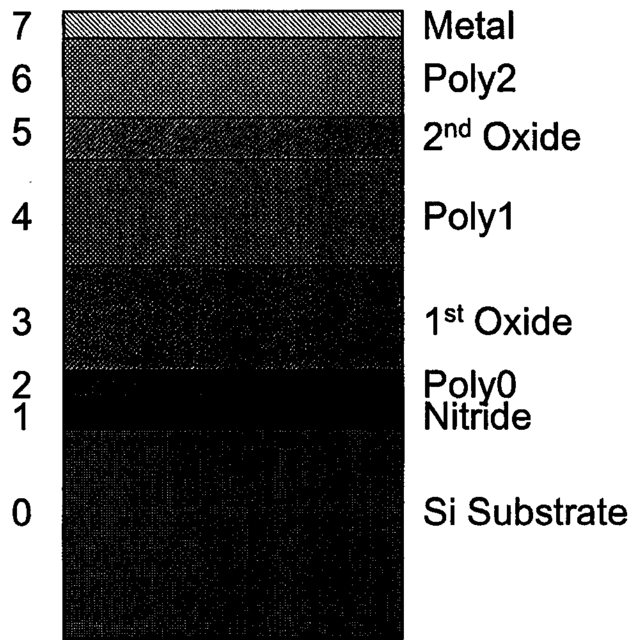

Figure 2.9 PolyMUMPS Layers

Layer	Name	Material	Thickness (μm)
0	Si	Silicon	675
1	Nitride	Silicon Nitride	0.6
2	Poly0	Polysilicon	0.5
3	1st Oxide	Silicon Dioxide	2.0
4	Poly1	Polysilicon	2.0
5	2nd Oxide	Silicon Dioxide	0.75
6	Poly2	Polysilicon	1.5
7	Metal	Gold	0.5

Table 2.1 Typical Thickness of PolyMUMPS Layers

Layer Name	Relative Permitivity (ε_r)	Sheet Resistance (Ω/)
Si	11.9	22.23
Nitride	7.5	N/A
Poly0	11.9	15
1st Oxide	3.9	N/A
Poly1	11.9	10
2nd Oxide	3.9	N/A
Poly2	3.7	20
Metal	1	0.06

Table 2.2 Typical Electrical Properties of MUMPS Layers

The fabrication process imposes some limitations in design to be fabricated. These limitations are presented as Design Rules. Design rules limit the maximum or minimum dimensions in each layers of the design and also specify the maximum or minimum distance or overlap of patterns on different layers [55].

All designs are to be checked against design rules before submission for fabrication. Normally design rule check (DRC) is performed by the layout design software and the DRC violations are shown graphically and are listed in a table. All the violation should be checked and corrected, unless they are intentional and acceptable by the manufacturer.

CMC Microsystems [68] provides subsidized access to PolyMUMPS to Canadian Universities.

2.6.2 Releasing the PolyMUMPS Devices

The final step in PolyMUMPS process is removing the sacrificial oxide layer or releasing the devices. It can be done by the fabricating company or by the user. According to PolyMUMPS handbook [55], to release the chips, they should be immersed in a bath of 49% HF at room temperature 1.5-2 minutes. Then chip should be immersed in DI[5] water for several minutes followed by immersion in alcohol or acetone for several minutes to prevent stiction problem. After all of immersion steps, chips are supposed to be dried in an oven at 110°C. All of the steps after the HF release are to prevent the stiction problem. Stiction happens due to attractive capillary (surface tension) forces of drying liquid (generally water). Those forces keep released structures stuck together and prevent them from moving. Immersion in warm alcohol or acetone that evaporates easily in room temperature is one of the solutions. Drying in the oven is another solution. Critical point drying by CO_2 is another solution suggested by MEMSCAP [55].

2.7 CMOS Process Technology

There are various CMOS technologies available with different layer combinations, feature sizes and electrical and physical properties. All of these processes are designed and optimized for fabrication of analog and digital integrated circuits. But they are also used for fabrication of MEMS devices although the process is not intended for that.

CMC Microsystems provides subsidized access to several CMOS processes to Canadian Universities. Between them the TSMC (Taiwan Semiconductor Manufacturing

[5] De-Ionized

Company) CMOS 0.35 is an appropriate process for MEMS fabrication regarding the minimum feature size, area and cost.

2.7.1 TSMC CMOS 0.35 Specifications

The layers in the CMOS 0.35 process are shown in Figure 2.10.

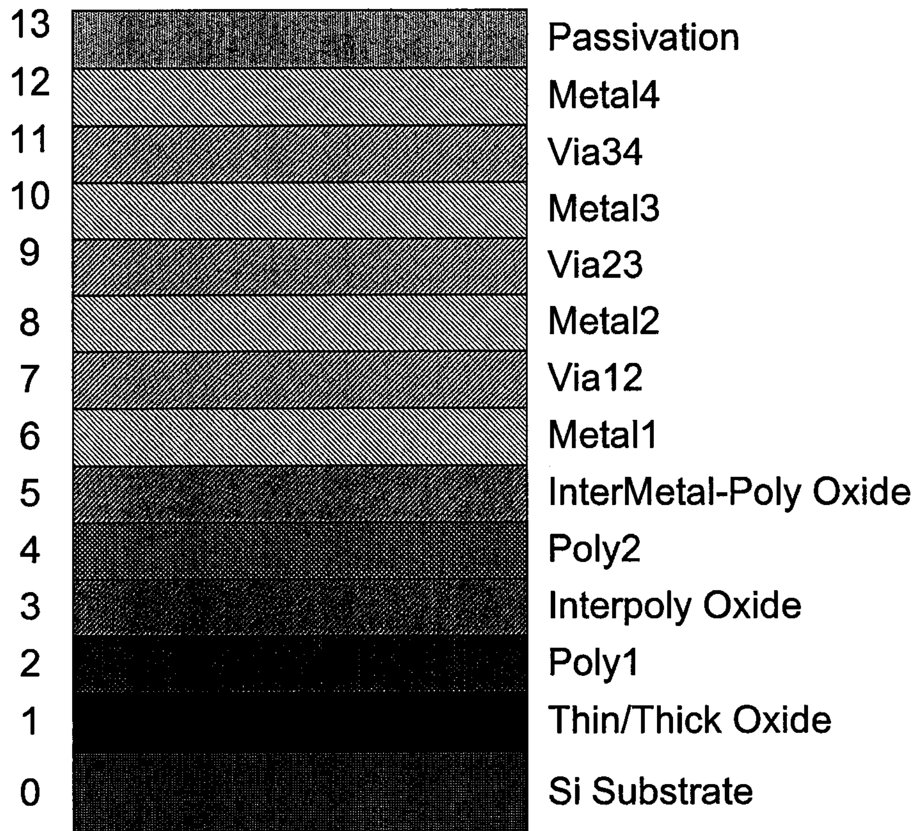

Figure 2.10 CMOS 0.35 Layers

The layer names and thicknesses are given in Table 2.3 and their electrical properties are given in Table 2.4.

Layer	Name	Material	Thickness(μm)
0	Si	Silicon	~750
1	Thin/Thick Oxide	Silicon Dioxide	0.18/0.29
2	Poly1	Polysilicon	0.275
3	Interpoly	Silicon Dioxide	0.037
4	Poly1	Polysilicon	0.18
5	Inter Poly1-Metal1	Silicon Dioxide	0.605
6	Metal1	Aluminum	0.665
7	Via12	Silicon Dioxide	1
8	Metal2	Aluminum	0.64
9	Via23	Silicon Dioxide	1
10	Metal3	Aluminum	0.64
11	Via134	Silicon Dioxide	1
12	Metal4	Aluminum	0.925
13	Passivation	Silicon Dioxide Silicon Nitride Glass	3

Table 2.3 Typical Thickness of CMOS 0.35 Layers

Layer Name	Relative Permittivity (ε_r)	Sheet Resistance (Ω/)
Si	11.9	10
Thin/Thick Oxide	3.9	N/A
Poly1	11.9	8
Interpoly	3.9	N/A
Poly2	11.9	50
Inter Poly1-Metal1	3.9	N/A
Metal1	1	0.083
Via12	3.9	N/A
Metal2	1	0.08
Via23	3.9	N/A
Metal3	1	0.08
Via134	3.9	N/A
Metal4	1	0.051
Passivation	3.9	N/A

Table 2.4 Typical Electrical Properties of CMOS 0.35 Layers

Like the PolyMUMPS process, CMOS 0.35 also has some design rules [69] and they are much more complicated than MUMPS. These design rules are provided to guarantee the fabrication of ICs with the minimum nominal feature size. But in case of MEMS devices, intentionally violating many of them is not a problem. But some of these design rules are

critical for the quality of the fabricated chips. Densities of metal1, metal2, metal3, metal4 and poly1 and poly 2 shouldn't be less than minimums specified in design rules to make sure that in fabricated chips stress of layers are balanced

Design should be critical DRC violation free before submission for fabrication.

At the beginning of the use of CMOS for MEMS fabrication, it was allowed to make big vias to open windows down to silicon substrate for the bulk micromachining process. But some problems showed up and quality of ICs degraded. So it is not anymore possible to have big vias in the layouts and those windows should be opened in post-processing steps that will be presented later in chapter 3.

2.7.2 Silicon Bulk Micromachining Techniques for CMOS Process

Invention of post-processing techniques made it possible for MEMS designers to take advantage of regular IC fabrication processes to make microstrucures to avoid costly custom designed processes. But IC fabrication processes are not designed to make microstrucures. They are designed, developed, and optimized for IC fabrication and there isn't any consideration for MEMS fabrication in them. Therefore it is up to the designers to adapt their design in such a way that it can be fabricated in a CMOS process and then can be released by micromachining post-fabrication steps.

Specialized processes may not automatically allow for on-chip integration of electronics and require the development and implementation of a circuit process along microstructures with the MEMS process. Backside etching also involves additional masks and alignment and therefore adds more complexity. Concurrently, there is also strong interest in developing microtransducers that are compatible with a commercial CMOS process.

Compatibility with a commercial CMOS process allows for monolithic integration of analog and digital circuits, which provide signal conditioning, interface control, and wireless remote communication. After receiving the chips, the microsensors or microactuators are then released by an additional frontside postprocessing etch.

Silicon micromachining is the key technology to fabricate microtransducers and actuators.

Depending on the design, suspended microtransducers can be realized using either an isotropic or anisotropic etch. While structures with sizes ranging from 40–200 microns can readily be realized with either an isotropic or anisotropic post etching, larger or longer microstructures, such as microwave coplanar waveguides and passive components, cannot be achieved with either an isotropic or anisotropic etch alone. Large structures require unacceptably long anisotropic etch times, which, in turn, cause other negative effects. Therefore, etching is the limiting factor in realizing large suspended microstructures.

Microstructures are made of thin films, either homogeneous or multilayer. The multilayer thin-film structures made from the prior post-CMOS micromachining process usually have large residual stress gradients, which cause curling. This limits the maximum layout size of microstructures, which is critical for providing large proof mass in inertial sensors. Moreover, release holes and unwanted curvature of microstructures degrade their application in the optical domain. [70-71].

To realize microtransducers at low cost, there are several requirements on the post-processing etching.

1. be low temperature to not change the doping profiles (junction depths) of MOS transistors.
2. be compatible with materials used in the commercial CMOS processes, namely, silicon dioxide, silicon nitride, and exposed aluminum.
3. not contaminate the gate dielectrics with impurities such as mobile alkali ions, which shift the flatband voltage and affect the circuits.
4. create structure with long term reliability,
5. not impose unacceptable stress levels on chip,
6. be easy to handle and safe

The most common etches used for micromachining are those for silicon, and are summarized in Table 2.5 and then are explained in detail.

	HNA	Alkali-OH	EDP	TMAH	XeF_2	SF_6 Plasma	DRIE
Etch type	wet	wet	wet	wet	dry	dry	dry
Anisotropic	no	yes	yes	yes	no	varies	yes
Availability	common	common	moderate	moderate	limited	common	limited
Etch rate (μm/min)	1 to 3	1 to 2	1 to 30	≈1	1 to 3	≈1	>1
Roughness	low	low	low	variable	high	variable	low
Nitride Etch	low	low	low	1 to 10 nm/min	?	low	low
Oxide Etch	10 to 30 nm/min	1 to 10 nm/min	1 to 80 nm/min	≈1 nm/min	low	low	low
Al Selective	no	no	no	yes	yes	yes	yes
Au Selective	likely	yes	yes	yes	yes	yes	yes
P+ etch stop	no	yes	yes	yes	no	no	no
Electrochemical Stop	?	yes	yes	yes	no	no	no
CMOS Compatible	no	no	yes	yes	yes	yes	yes
Cost	low	low	moderate	moderate	moderate	high	high
Disposal	low	easy	difficult	moderate	N/A	N/A	N/A
Safety	moderate	moderate	low	high	moderate	high	high

Table 2.5 Comparison of Silicon Etchants [15]

Where HNA is a mixture of Hydrofluoric (HF), Nitric (HNO_3), and Acetic (CH_3COOH) acids, Alkali-OH such as KOH, EDP is Ethylene-Diamine Pyrocatecol, TMAH is Tetra Methyl Ammonium Hydroxide, and DRIE stands for .Deep Reactive Ion Etching.

Silicon etching can be performed in wet or dry methods. Etching could be isotropic (same etch rate in vertical and lateral directions) or anisotropic (with vertical or angled sidewalls after etching). Depending on the device conditions, wet or dry etching, isotropic or anisotropic may be desirable. We will consider all four possible cases given in Table 2.6.

Etching Method	**Wet or Dry**	**Isotropic or Anisotropic**	**Example(s)**
1	Wet	Isotropic	HNA
2	Wet	Anisotropic	KOH, EDP, TMAH
3	Dry	Isotropic	XeF_2, SF_6
4	Dry	Anisotropic	RIE, DRIE, SF_6

Table 2.6 Four Possible Etching Methods

2.8 Isotropic Wet Etching of Silicon

A typical isotropic silicon etchant is a combination of hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH), also known as HNA. A cross section of a cavity etched with an isotropic etchant is illustrated in Figure 2.11. The undercut ratio is defined as u/d, which is close to unity. The chemical reaction for silicon etching in HNA involves an oxidation step, followed by a dissolution step. The relative concentration of the three ingredients determines which step limits the overall etch rate and what type of etching profile results [72]. Due to the lateral of undercutting and resulting lack of dimensional control, isotropic etchants are not often used in micromachining [73].

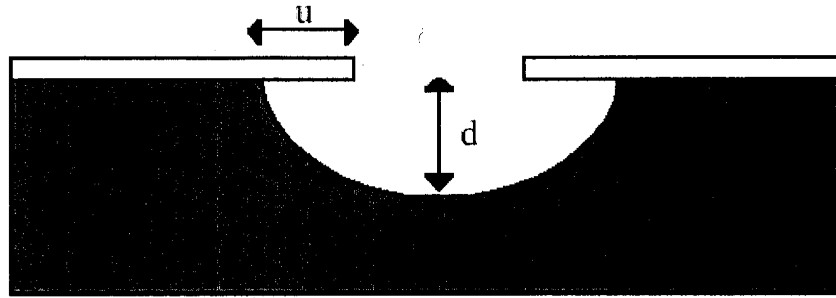

Figure 2.11 Cross Section of an Isotropic Silicon Etch.

2.9 Anisotropic Wet Etching of Silicon

In an anisotropic, or orientation dependent silicon etch, the etch rate varies with the crystallographic direction of the semiconductor crystal. Slower etching crystal planes will appear over time as faster etching planes are consumed. Anisotropic silicon etchants include ammonium, sodium, cesium, and potassium hydroxides (NH_4OH, NaOH, CeOH, KOH), hydrazine (NH_2NH_2), ethylenediamine ($NH_2(CH_2)_2NH_2$), and tetramethyl ammonium hydroxides (TMAH). Alkaline anisotropic etchants are used at elevated temperatures (60°C-100 °C).

Alkali metal hydroxides such as potassium hydroxide (KOH) have high silicon etch rate and anisotropy. Unfortunately, KOH is not post-CMOS compatible because it attacks aluminum and SiO_2 and contaminates the gate oxides with mobile alkali metal ions.

The quaternary ammonium hydroxides fulfill the requirements of CMOS compatibility. In this group, tetramethylammonium hydroxide (TMAH) is the preferred etchant because it has fairly high silicon etch rate.

Another CMOS etchant, which might be a potential candidate for silicon micromachining, is ammonium hydroxide doped with dissolved silicate and hydrogen

peroxide. Aqueous ammonium hydroxide was not considered here because it has very low silicon etch rate, poor reproducibility, and problems with hillock formation. The parameter window for ammonium hydroxide to work properly is very small; hence, a high-accuracy real-time monitoring of the loss of ammonia, OH ion, hydrogen peroxide, and contaminants appeared to be needed. Only small chips have been etched successfully with this etchant in this work; larger chips and chips that were packaged did not even start to etch.

The evolution of an anisotropically etched cavity is shown in Figure 2.12. The figure identifies the pertinent crystallographic directions by their Miller indices [74]. The crystal orientation of silicon wafers is also expressed by these indices. A (100) silicon wafer, the standard wafer used in CMOS processes, has a surface co-planar with the (100) crystal plane. In anisotropic etchants, the (100) plane etches much faster than the (111) crystal plane (typically by more than 100 times). A square mask opening will result in an inverted pyramidal cavity. The side-walls of the pit are bounded by the (111) planes, which make a 54.7° angle with the substrate surface. If the (111) etch rate is assumed to be low, the depth of a cavity can be accurately controlled by the geometry; the angle between the (111) plane and the (100) surface is fixed at 54.7°. The square mask opening in Figure 2.12 has only concave corners. If convex mask corners are exposed during an anisotropic etch, they become undercut along other crystal planes. This proceeds primarily along crystal planes with the highest etch rates. The exact plane along which it occurs depends on the etchant, but typical planes are (110) and (221). As a general rule, assuming a low etch rate of (111) planes, any dark field masking pattern that is exposed to an anisotropic etchant for a sufficiently long time will produce an inverted pyramidal

cavity, the base of which is determined by the smallest rectangular shape that contains the entire pattern [75]. This is illustrated in Figure 2.13 for several different mask shapes.

The silicon etching process in alkaline anisotropic etchants can be written as [76]

$$Si + 2H_2O + 2OH^- \rightarrow 2H_2 + Si(OH)_2O_2^{2-} \tag{2.1}$$

The products of the silicon etching reaction are hydrogen gas, which appears in the form of bubbles, and hydrous silica [73].

The chemical reaction is the oxidation of silicon, followed by the dissolution of hydrated silica. The oxidant is typically the water in the etching solution.

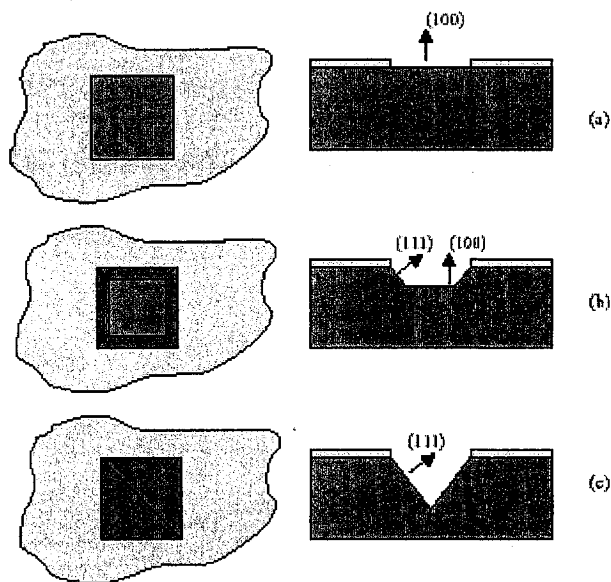

Figure 2.12 A square mask opening results in an inverted pyramidal cavity. Initially, only (100) silicon is exposed (a). As the (100) silicon etches, the slowly etching (111) planes become exposed (b), until etching terminates on the intersection of four (111) type planes (c).

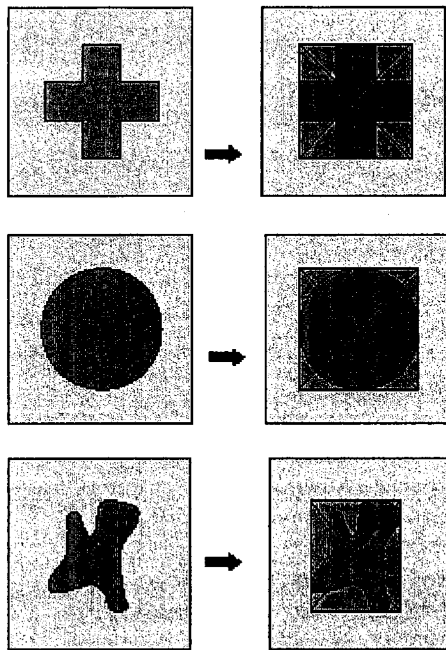

Figure 2.13 Arbitrary dark field mask openings result in inverted pyramidal cavities with the base defined by the smallest rectangle that completely contains the mask pattern.

2.9.1 EthyleneDiamine-Pyrocatechol Water

Ethylenediamine $NH_2(CH_2)_2NH_2$ is typically used in conjunction with pyrocatechol $C_6H_4(OH)_2$, and referred to as EDP [77]. Pyrocatechol acts as a chelating agent, and helps dissolve silica that forms during the etching process. EDP has the attractive properties of oxide selectivity. There are several types of EDP etchants with different compositions, known as types B, T, S, and F. Types T and F have high silicon etch rate while types B and S have low silicon etch rate. They are readily commercially available. Type F has a higher water and pyrocatechol content than type S. EDP-type F is only moderately selective against aluminum. Some formulations, specifically the S formulation are also selective to aluminum. EDP also works very well with p+ boron etch stop, due to its high selectivity (in excess of 40:1) to heavily doped p-type silicon.

Fresh EDP-type-F etchant has a pale amber color, which darkens after a few hours of use and exhibits a deep red color when it becomes unusable. Etching is generally performed in the temperature range 92–100°C, which gives an etch rate of about 70 μm/h for (100) silicon. The etch rate increases as the solution is exposed to air for some time. EDP etching is a relatively awkward process, and chips etched with EDP tend to deteriorate over a long period of time unless they are rinsed very well for many hours after etching. The problem with EDP, when used at lower temperatures, is the formation of a thin layer of insoluble residue. If this residue is not washed away, it will destroy all the structures on the chip by corrosion.

Unlike the quaternary ammonium hydroxide etchants, EDP has no problem with the formation of "hillocks," which tend to stop the etching prematurely.

The use of EDP is not as desirable as the quaternary ammonium hydroxide etchants because it is considered quite hazardous. EDP can have very serious long-term toxic effects and can be absorbed through the skin. It is also mutagenic. When it comes in contact with water during cleaning, a visible amber mist develops. Misting creates a serious inhalation hazard in addition to that caused by the evaporation of ethylenediamine from solution. Care must be taken not to breathe any of these vapors during the etching process. EDP needs to be used under nitrogen ambient to prevent oxygen contamination of the solution. EDP is therefore difficult to use, and expensive to dispose of. [70, 73].

2.9.2 Potassium and Sodium Hydroxide (KOH and NaOH)

These two etchants have almost identical properties. The K^+ and Na^+ ions are believed to have little, if any, effect on their etching properties [78]. KOH in water is one of the most

commonly used alkaline silicon etches. It has a relatively high etch rate, of several microns per minute. These two chemicals corrode aluminum, and silicon dioxide is also etched relatively quickly (up to 2 μm per hour). Silicon nitride is usually employed as a masking layer in KOH etches. Both of these etchants obviously contain alkali ions, and are therefore not CMOS compatible, since they can introduce charge under MOS transistor gates and cause threshold voltage shifts [73].

2.9.3 Ammonium Hydroxide (NH4OH)

Ammonium hydroxide etches silicon more slowly than KOH (roughly half the etch rate). Ammonium hydroxide has the problem that hillocks form on the (100) etched surfaces. This hillock formation can be eliminated with the addition of specific amounts of hydrogen peroxide. Unlike KOH or NaOH, ammonium hydroxide has a relatively high selectivity to oxide, up to 10,000:1. The etchant is noxious and volatile, however, and cannot be heated much above 80 °C without evaporating. While metals like gold, chrome, and titanium are not attacked by ammonium hydroxide, aluminum dissolves very quickly [73, 79].

2.9.4 Hydrazine (NH2NH2)

Hydrazine has seen some use in micromachining due to the possibility of making the solutions selective to aluminum. The etchant is selective to oxide, and has an etch rate of approximately 2 μm per minute (at 80 °C). A small amount of silicon dissolved in the etchant (about 10 mg per liter) passivates aluminum. Hydrazine, however, is difficult to use and dispose of, since it is toxic and explosive [80].

2.9.5 Tetramethyl Ammonium Hydroxide

TetraMethyl Ammonium Hydroxide (TMAH, $(CH_3)_4NOH$) is one of a group of chemicals known as quarternary ammonium hydroxides, which also includes tetraethyl ammonium hydroxide (TEAH, $(C_2H_5)_4NOH$). TMAH is more readily available than TEAH, since the former has been used for many years in IC foundries as a developing solution for positive photoresist. TMAH has very high selectivity to silicon dioxide and silicon nitride (on the order of 10,000:1) [81]. In addition, it has been shown that if specific amounts of silicon are dissolved in the etching solution, aluminum will passivate [82]. Typically, aluminum etches in basic solutions through the dissolution of the aluminum oxide on its surface. The effect of the dissolved silicon appears to be a reaction of silicates in solution with $Al(OH)_3$ at the surface of the aluminum. This is thought to form insoluble silicates that passivate the aluminum oxide. TMAH is relatively safe to use, and easy to dispose of. It does not dissociate below 130 °C, which makes it possible to etch at relatively high temperatures.

The main drawback of TMAH is that it can form very rough (100) etched surfaces. These etched areas are covered with hillocks that expose slowly etching crystal planes. When this happens, the etch rate drops precipitously. Low TMAH concentrations (less than about 20 weight percent) and silicon doped TMAH solutions lead to hillocking. Two main factors are thought to contribute to hillocking in alkaline solutions [83]. These are micromasking by hydrogen bubble formation and redeposition of insoluble etch products on the surface.

Primarily from a safety point of view, TMAH is the preferable etchant for circuit compatible micromachining. If the hillocking of silicon surfaces can be eliminated, TMAH can be a useful etchant [73].

2.9.6 Silicon Etching with TMAH and Additives

Pure TMAH and water solutions can be used to etch silicon. They have a high selectivity to silicon dioxide and silicon nitride, and when the concentration is above 20 percent by weight TMAH, the (100) surfaces are smooth. The silicon etch rate of TMAH increases with decreasing concentration, with a maximum at about 2 weight percent.

TMAH solutions, like any strong base, cause exposed aluminum to dissolve. Aluminum grows a thin layer of aluminum oxide when exposed to air. This oxide layer contains $Al(OH)_3$ which, when exposed to alkaline environments, reacts to form aluminate.

When the PH of the alkaline solution is decreased, the chemical equilibrium shifts toward reducing the effective aluminum etch rate. Aluminum exhibits amphoteric behavior. It passivates around neutral PH, and corrodes in alkaline and acidic environments.

For alkaline solutions of moderate PH (between 8 and 12), the aluminum etch rate is decreased by the introduction of silicates to the system [79]. The presence of silicates in solution will form aluminosilicates that are less soluble than the hydrated aluminum oxides that would otherwise form at the metal surface [73].

For TMAH solutions, the silicates to provide aluminum passivation can come from dissolved silicon. As the silicon dissolves, it lowers the PH of the solution, and therefore works in two ways to provide aluminum passivation. The required amount of silicon is roughly proportional to the TMAH concentration. Figure 2.14 shows the relationship between required dissolved silicon and the etchant concentration [73].

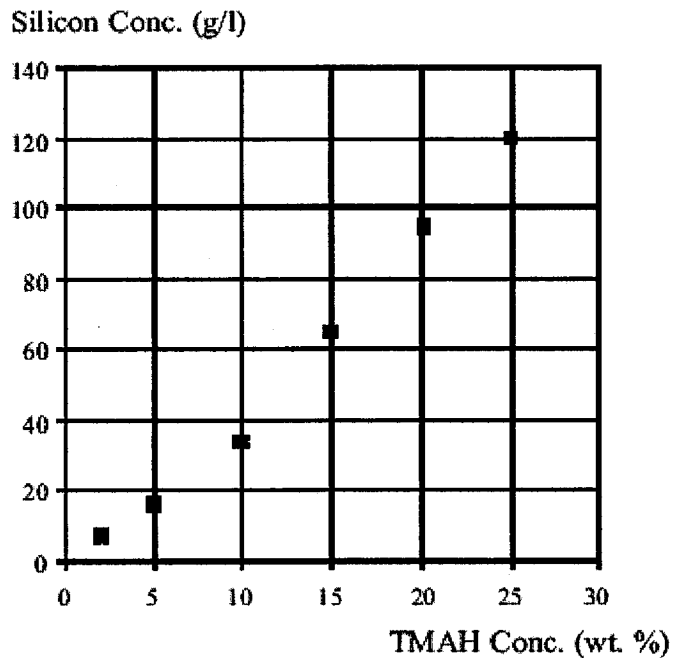

Figure 2.14 Required amount of dissolved silicon to passivate exposed aluminum for various TMAH concentrations [73].

Since it is undesirable to dissolve excessive amounts of silicon in the etching solution, lower TMAH concentrations are preferable from an aluminum passivation standpoint. Dilute concentrations also provide higher silicon etch rate.

The silicon can be added in the form of wafers, or wafer pieces, but these can take several hours to fully dissolve. A more expedient method is to add powdered silicon, which is available at 99.9% purity. Powdered silicon has a much higher surface area than wafer pieces, and dissolves very rapidly. Due to the large amount of hydrogen gas that evolves during this process, foaming and excessive bubbling of the solution can occur. To prevent the solution from foaming over the edge of the etch bath, it is necessary to dissolve the silicon at a relatively low temperature (around 45 °C) [73].

Silicon dissolves in TMAH to form silicic acid. It is this silicate that forms a protective layer on exposed aluminum. Instead of silicon, silicic acid ($Si(OH)_4$) can be added to TMAH as an alternative source of silicates. There is no apparent advantage to using silicic acid instead of silicon, except that it does not foam when it is dissolved at high temperature. The solution is also somewhat cleaner, since silicon powder leaves an insoluble powdery material at the bottom of the etch bath and deposits at the water-line of the etchant [73].

TMAH solutions with a PH lower than 13 produce very rough etched silicon surfaces, due to the formation of hillocks. When silicon is etched in TMAH, gaseous hydrogen forms as a byproduct. If small bubbles cling to the surface before they release, they temporarily mask the surface underneath from the TMAH. The bubbles block the free diffusion of reactants and products to and from the surface. A precipitate forms at the point of contact between the bubble and the silicon that creates a temporary masking layer as it is slowly dissolved upon release of the hydrogen bubble. This localized mask is composed of partially hydrated silicate species with variable stoichiometries. Initially the number of pyramids at the surface is small, but as etching continues new pyramids are formed and begin to superimpose over previous hillocks. If surface roughness is present to begin with, this process will occur more rapidly, since more nucleation sites are already present.

For some applications, the quality of an etched surface may not seem to be an issue. The hillocks are still a problem, however, since they expose (111) silicon planes, and significantly reduce the etch rate. The motivation to eliminate hillock formation therefore stems practical as well as aesthetic concerns.

Surfactants could be added to the solution to change the wetting angle of the solution on the silicon surface. This could keep bubbles from clinging to the surface. TMAH, however, is very sensitive to contamination from organic sources. The addition of fluorochemical surfactants causes silicon etching to stop when added to TMAH solutions. Pyrazine can be added to TMAH to eliminate hillocks. It was shown that the addition of 30 grams per liter of pyrazine will eliminate hillock formation for 5 weight percent TMAH solutions. A major drawback of this additive is that pyrazine is toxic and hazardous to use.

Peroxydisulfate is one of the strongest known oxidizers in aqueous solution. This is the ion that forms when sulfuric acid is mixed with hydrogen peroxide in Piranha cleaning solutions. Peroxydisulfate is available in various forms, which include dipotassium peroxydisulfate ($K_2S_2O_8$), disodium peroxydisulfate ($Na_2S_2O_8$) and diammonium peroxydisulfate ($(NH_4)_2S_2O_8$). Of these three, sodium and potassium peroxydisulfate are the most stable, but they contain sodium and potassium, which are not compatible with CMOS processes since these can cause threshold voltage shifts by introducing charge under the gates of MOS transistors. Ammonium peroxydisulfate (also known as ammonium persulfate) is somewhat less stable, and requires refrigeration to preserve its shelf life. It does not contain alkaline ions, however, and is therefore MOS compatible. The peroxydisulfates are relatively safe to use, and present no special disposal issues.

Ammonium and potassium persulfate, when added to silicon doped TMAH solutions eliminate hillock formation, much as hydrogen peroxide has been shown to do in ammonium hydroxide. The required amount is only 2 to 5 grams per liter of solution.

In contrast to hydrogen peroxide, the addition of excess peroxydisulfate does not stop the silicon from etching. When ammonium persulfate is added to silicon-doped TMAH solutions, a white precipitate forms. This is probably due to a reaction between the oxidizer and the silicates in solution [73].

Peroxydisulfates are relatively inexpensive. Ammonium persulfate needs refrigeration at 5-7 °C to preserve it, but potassium persulfate can be stored at room temperature. There are no special safety considerations that need be taken for these chemicals, aside from the standard precautions observed with any strong oxidizer (gloves, safety glasses, ventilation, and avoidance of contact with combustibles). The solution can safely be disposed of through an acid neutralization system [73].

2.10 Isotropic Dry Etching of Silicon

The use of XeF_2 for plasma etching of silicon and etching silicon with XeF_2 without plasma has been studied extensively. Silicon is isotropically etched by exposure to gaseous XeF_2 at room temperature. Only recently has XeF_2 without plasma enhancement been used to micromachine silicon to create microtransducers. Chung et al. [84-85] have performed a detailed study of the etching characteristics of XeF_2. An investigation of the mechanisms of the etching of silicon with vapor XeF_2 was given by Houle [86] and Winters and Coburn [87].

XeF_2 is a white crystalline solid with a vapor pressure of about 600 Pa (4.5 Torr) at room temperature [86]. The reaction between XeF_2 and silicon occurs through a sequence of steps. Gaseous XeF_2 is first absorbed on the silicon and then reacts to form a thick layer of fluorosilyl consisting of SiF, SiF_3, and SiF_4. The fluorosilyl product desorbs into the

gas phase. The principal gas-phase product has been determined to be SiF_4, which is volatile at room temperature. The reaction equation for XeF_2 and silicon is approximately given by

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4 \quad (2.2)$$

Etching with XeF_2 is applicable to packaged as well as unpackaged chips. For unpackaged chips, photoresist can be used to protect the backside and peripheries of the chip because XeF_2 will etch any exposed silicon, resulting in significant thinning of the chip [70].

2.11 Anisotropic Dry Etching of Silicon

DRIE is a very high aspect ratio silicon etching method that relies on a high-density inductively coupled plasma source and an alternating process of etching and protective polymer deposition to achieve high aspect ratios of up to 30:1, with photoresist selectivities of 50-100:1, slicon dioxide selectivities of 120-200:1, and etch rates on the order of 2-3 μm/min [88]. The practical maximum etch depths capability of this approach is on the order of 1 mm, and etch depths can readily be obtained using buried oxide SiO_2 etch stop layers (for example formed by bonding an oxidized wafer to a second wafer) [15].

2.12 Oxide Removal Methods

As it was mentioned in chapter 2, it is not possible to open etch windows in via layers in the design (layout). So these windows should be opened in a post-processing step.

There are two methods for oxide removal: wet etching and dry etching.

2.12.1 Oxide Wet Etching

If the appropriate mask [89-90] is designed and already available, photoresist can be used to protect the chip, and only windows to be opened are exposed to diluted HF or buffered oxide etchant (BOE). Etch rate depends on the oxide type and HF concentration of the mixture and usually a few minutes is enough for all the oxide to be removed.

It is suggested to check the thickness of oxide several times by optical microscope before the expected overall etching time to monitor the etching process and observe the oxide color change. Because this method isotropically etches the oxide, overetching results in mask undercutting and is undesirable.

HF and BOE are not selective to aluminum and in some concentrations they even etch aluminum much faster than oxide. So the exposed aluminum will be damaged [46]. Because oxide wet etching when aluminum is also exposed is not very common, finding a solution was not easy.

In multilevel metal processes it is often necessary to etch vias through an insulating interlevel dielectric. Also if chips are given a protective overcoat it is necessary to etch vias through the insulating overcoat to the bonding pads. When the underlying layer is aluminum and the insulating layer is glass the etchant needs to etch glass but not etch aluminum. Straight Buffered HF will etch Aluminum.

Finally I found an etch recipe that originally was developed to etch via holes in the presence of aluminum. It is shown that a mixture of 5 parts BOE and 3 parts Glycerin works well. Etch rate is unaffected by the Glycerin. Original work was published by J.J. Gajda at IBM System Products Division [91]. Afer several minutes of etching aluminum stays intact.

This method is easy and safe but you have to design and order a mask and go through a complete photolithography cycle from spin coating of photoresist, to developing and had baking it,

2.12.2 Dry Etching of Oxide

An alternative to wet etching is using reactive ion etching (RIE). This method is anisotropic results in near vertical side walls. But still the rest of chip that is covered with glass passivation layer must be protected. A cheap and reliable solution is using top metal layer of the CMOS process as a mask to protect the chip. The only disadvantage is that one metal layer should be sacrificed that limits our design options. In addition, normally the top metal layer is the thickest metal layer with the smallest resistivity between all metal layers of the process and is suitable to fabricate RF MEMS component. But when top metal is used as a self-aligned mask, we have to use other methods and get not the best performance from RF MEMS devices,

In CMOS 0.35, metal 4 can be used as the mask layer. You have to pay attention to electrically isolate metal 4 masks from any other connection to prevent short circuiting bonding pads and interconnections [71].

2.13 Switches

2.13.1 Mechanical (Electromechanical) Switches

RF switches are one of the first devices introduced in this category of devices. They operate very similar to regular switches used in everyday life; when the switch electrodes are forced to touch each other, switch conducts and is in "closed" position. When they are apart, switch isolates the two electrodes and is in "open" position. This simple principle

of operation and also a wide range of possible applications make RF switches very attractive for researchers. In addition, the same structure can be used as a variable capacitor or as a resonator. A large number of switches with different actuation mechanisms, circuit configurations, and numerous applications are fabricated.

2.13.2 Solid State Switches

There exist many different solid state switches with diverse applications, such as power switching, telephone/circuit switching and multiplexing.

These switches can be transistor switches (FET [92]), PIN diode switches, or GaAs MESFET switches [93]

2.13.3 RF Switches

A RF switch has two distinct parts: the actuator (mechanical) part and the electrical part (signal path). The actuation force for mechanical movement can be obtained from electrostatic, magnetic, piezoelectric, or thermal mechanism. In addition, the mechanical switch, as developed by several research groups, is a key component with huge potential in various microwave circuits. The movement of switch could be vertical or lateral. The intrinsic mechanical properties of the constructing material(s) of the switch, keeps the electrodes in one state (without external force application). In the electrical part, switch can be placed in series or shunt configurations. Also there are two contact types, electrode-to-electrode (normally electrodes are made of metal) contact and capacitive contact. In capacitive contact, there is a layer of a dielectric material between electrodes that prevents them from touching, but lets the RF signal to be passed through capacitive coupling [94].

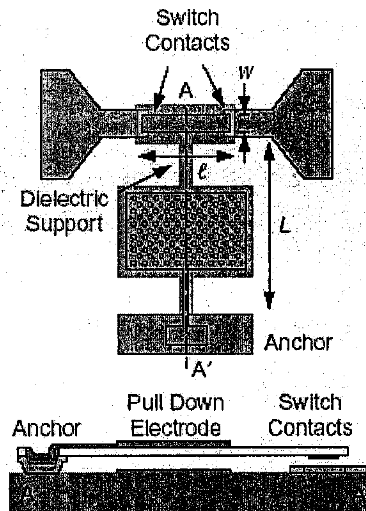

Figure 2.15 Structure of a MEMS RF Switch [94]

If the actuation is electrical (electrostatic, magnetic, piezoelectric) signal and actuation terminals can be completely separated or they can have a common terminal. Even it is possible that signal and actuation use the same terminal where the RF signal acts as actuation, too.

With the above division, 32 different types of RF switches can be built using different actuation mechanisms (4), movement planes (2), contact types (2), and circuit configurations (2).

2.14 RF Switches in MEMS Technology (Compared with Semiconductor Switches)

Before advent of RF MEMS switches, semiconductor switches such as PIN diodes and FETs were utilized (they are still in use) [9].

We can compare electrostatically actuated RF MEMS switches with PIN diode and FET switches (all for the same frequency and RF power range). Comparisons are arranged into

two groups; advantages and disadvantages (Definitions of switch parameters will be given later in this chapter).

Disadvantages: Electrostatic MEMS switches

- require a higher actuation voltage
- are slower (they have longer switching time)

Advantages: Electrostatic MEMS switches

- don't sink current in the on state (closed position)
- have very low power consumption
- have very low capacitance in the open state
- have very low series on resistance
- their ratio of open to closed capacitance is high (in capacitive switches)
- have very high cutoff frequency
- have low insertion loss in closed position
- have very high isolation in open state
- have a wide linear operation range versus input power (higher 3rd.order intercept point)
- are very small size and mass

According to the above comparison, MEMS switches offer a much superior performance compare to semiconductor switches in low to medium power applications.

2.15 Applications of RF MEMS Switches

With all of the above advantages of RF MEMS switches, what are the possible applications? Well, there are lots of applications. Virtually in most of the cases they can

replace solid state switches (except for a few applications that need high powers or fast switches) Application areas of RF MEMS switches are communication systems and radar systems.

Switches are used in switching networks (matrices), reconfigurable networks [95-99], portable wireless systems, and phased arrays [100] in communication and radar systems. Applications include: SPNT (single-pole N-throw) switches for filter and amplifier selection, $N \times N$ switching matrices, SPDT (single-pole double-throw) and DTDT (double-pole double-throw) routing switches, very high isolation switches (instrumentation), programmable attenuators, phase shifters [101-102], reconfigurable matching networks, switched filter banks, and much more [9, 94].

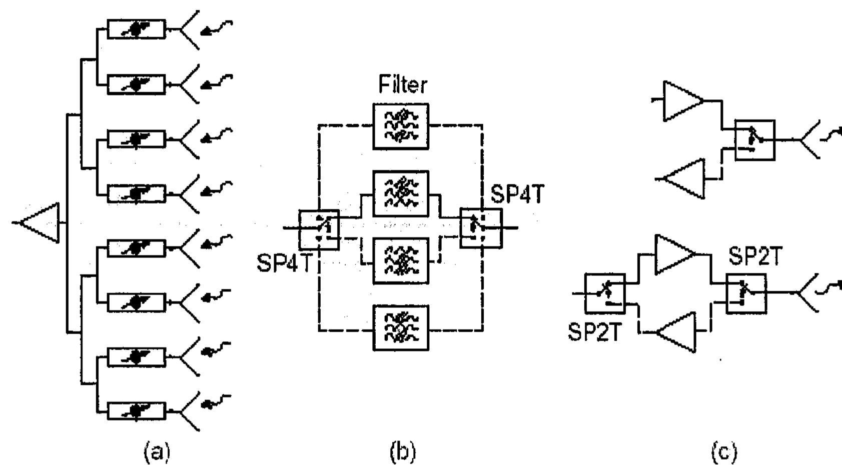

Figure 2.16 Application of Switches (a) Phased Arrays, (b) Switched Filter Banks for Wireless Applications, and (c) SP2T T/R Switches [94]

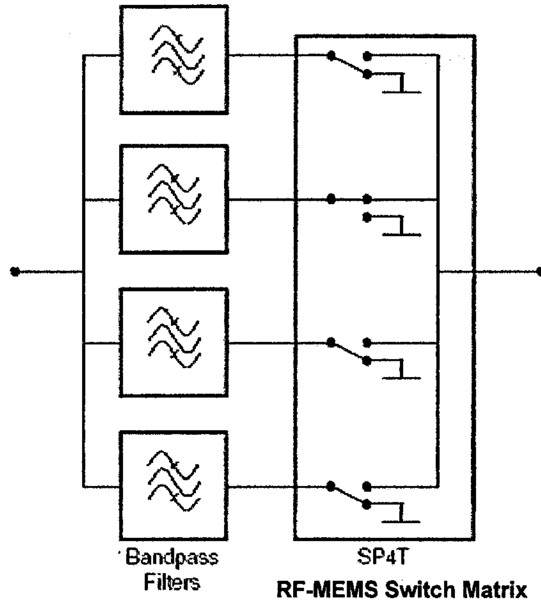

Figure 2.17 A Reconfigurable Filter [2]

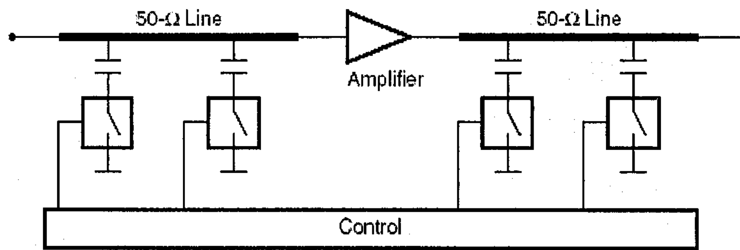

Figure 2.18 A Reconfigurable Amplifier [2]

2.16 Switch Parameters

When we talk about RF switches, usually following parameters are important [9-10]:

Actuation Voltage and Current: The required voltage and current to change the switch state,

Cutoff Frequency: The frequency, at which the ratio of on-state impedance to off-state impedance becomes unity,

Insertion Loss: It is the loss that a signal suffers upon traversing the switch in the on state.

Isolation: It refers to the ratio of unwanted output signal to input signal in the off state,

Linearity: It is expressed in terms of the third-order intercept point (the ratio of the power of third-order intermodulation products to input power),

Off-State Capacitance and On-State Resistance (series switches),

Power Consumption: The power consumed during switching and standby states,

RF power handling: It is a measure of how much and how well a switch passes the RF signal. To quantify the RF power handling, the 1dB compression point (the point at which the output power deviation from linear characteristics is 1 dB),

Switching Speed: The time required for the switch to respond at the output when the input actuation voltage is applied,

Switching Transients: These are exponentially decaying voltage spikes at either the input or the output that are result of changing the switch state from on to off or vice versa.

Transition Time: The time required for the output RF voltage envelope to go from 10% to 90% for on-time or 90% to 10% for off-time,

Value and Ratio of Capacitances in On and Off States (capacitive contact switches).

2.17 Actuation mechanisms

There are four different actuation mechanisms for MEMS switches; Electrostatic, Magnetic, Piezoelectric, and Thermal. Between them, electrostatic actuation is simplest and more applied.

2.17.1 Electrostatic

The electrostatic actuation is based on parallel-plate capacitor with a moving plate (Figure 2.19). Normally this type of actuation requires high actuation voltages.

2.17.2 Magnetic

In this type of actuation a permanent magnet or a magnetic material with magnetizing coil is employed. Actuation voltage can be moderate but the required current should be provided to coil and kept to hold the switch in actuated state [9].

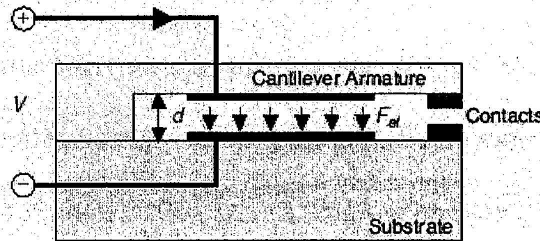

Figure 2.19 Electrostatic Actuation Mechanism

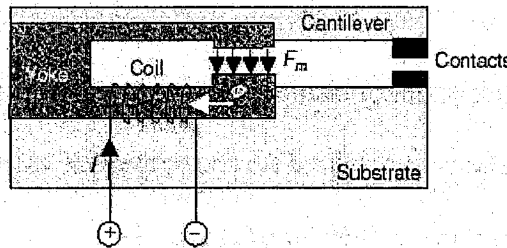

Figure 2.20 Magnetic Actuation Mechanism

2.17.3 Piezoelectric

Many of electrostatic actuation structures are built using piezoelectric[6] (PZ) actuation. To do so, a layer of PZ material should be evaporated on the top electrode and its edges, as it's shown in Figure 2.21. When a voltage is applied to the PZ layer, it expands and pushes the top electrode toward the bottom electrode.

---

[6] For more information about piezoelectric effect refer to [49]

Piezoelectric actuation results in low-voltage operation and prevents the charging effects that are common in electrostatic switches. PZ actuation can result in large contact forces, but a thick layer of PZ material is needed.

The main advantage of PZ actuation is the dependency of force on applied voltage polarity. By reversing the voltage polarity, direction of force is reversed too. Therefore, PZ actuation results in both an actuation and a restoring force. This restoring force is very desirable to overcome the stiction problem (stiction phenomenon will be discussed later in this chapter). [9, 19]

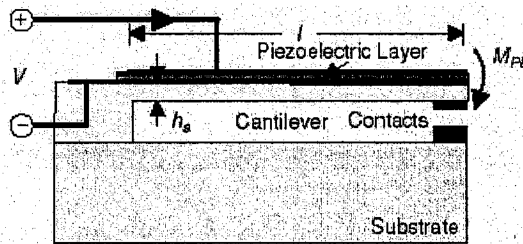

Figure 2.21 Piezoelectric Actuation Mechanism

A tunable piezoelectrically actuated parallel-plate varactor has been developed by LG Electronics Institute of Technology [103].

2.17.4 Thermal

In this actuation mechanism, resistive heaters are used. By applying voltage, heat is generated that results in the deformation of the structure and switch actuation. In this actuation type, heat must be generated as long as we want to keep the switch in actuated state/position that results in a constant power consumption that is not attractive in many applications. Although it's possible to reduce the power consumption by applying pulses instead of constant DC voltage, still the consumption and heat dissipation are problems of this type of actuators. Also the response is not fast [9].

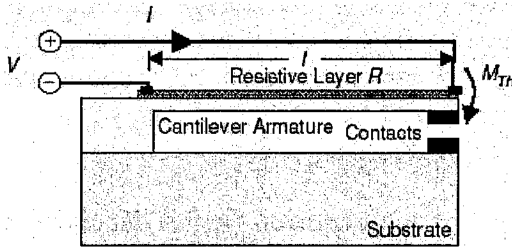

Figure 2.22 Thermally actuated switch

2.17.5 Hybrid actuation mechanisms

One way to get low actuation voltage but still maintain low power consumption is to use a thermal-electrostatic switch. P. Blondy and his group [104] (Figure 2.23) have developed such as switch. Switch is designed in a way that there is a large restoring force. By apply a DC voltage, top electrode deflects due to the thermal effects and achieves a metal to metal contact. Then the electrode is maintained in the down-state position with the use of a DC voltage across the top electrode and extra bottom side-electrodes. The electric hold-down is essential for low-power operation since the thermal forces are only used during the actuation time

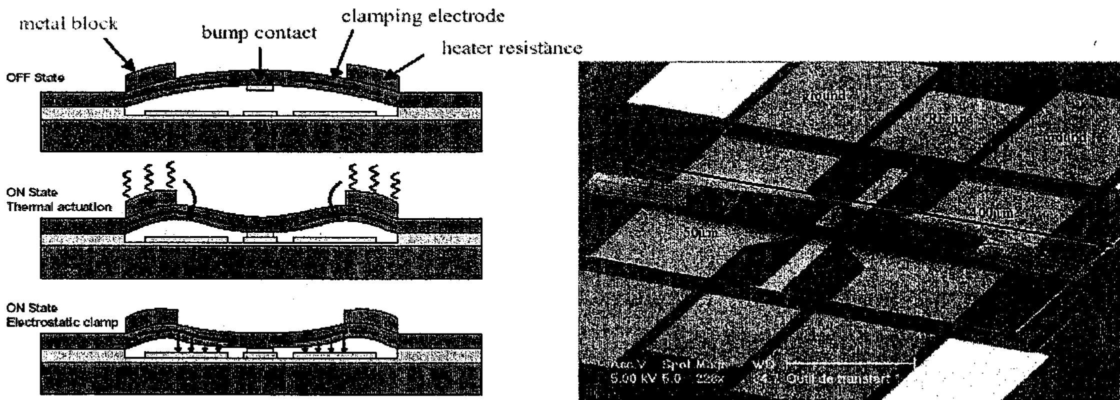

Figure 2.23 Themally-Electrically Actuated Switch [104]

3. Design and Simulation of MEMS RF Switches

3.1 Electrostatic Actuation Mechanism

In a parallel-plate capacitor, when a DC voltage is applied between the plates, although the plates are fixed and can't move, they exert an attraction force on each other. If one of the plates is free to move, the other plate will absorb it and the air gap between them will be reduced. Reduction in air gap results in increased force and decreased gap until the attraction force and the spring resistance force of the plate come to a balance. If the applied voltage is large enough, it brings the plates so close that they touch each other. This is the same principle that is employed in electrostatically actuated switches.

Given that the width of the plates is W and their length is L, and the gap between them is g, the parallel plate capacitance is

$$C = \frac{\varepsilon_0 A}{g} = \frac{\varepsilon_0 WL}{g} \text{ where } A = WL \text{ is the plate area.} \tag{3.1}$$

When one plate is moving, the capacitance changes as a function of the gap g, so

$$q = C(g)v \tag{3.2}$$

Current is obtained by differentiating the charge with respect to time [105]

$$i = \frac{dq}{dt} = \frac{d}{dt}[C(g)v] = C(g)\frac{dv}{dt} + v\frac{dC(g)}{dt} = C(g)\frac{dv}{dt} + v\frac{dC(g)}{dg}\frac{dg}{dt} \tag{3.3}$$

The power delivered to a time-dependent capacitance is

$$\begin{aligned} p = vi = v\frac{d}{dt}[C(g)v] = C(g)v\frac{dv}{dt} + v^2\frac{dC(g)}{dt} \\ = \frac{d}{dt}\left[\frac{1}{2}C(g)v^2\right] + \frac{1}{2}v^2\frac{dC(g)}{dt} = \frac{d}{dt}\left[\frac{1}{2}C(g)v^2\right] + \frac{1}{2}v^2\frac{dC(g)}{dg}\frac{dg}{dt} \end{aligned} \tag{3.4}$$

This expression can be put in the form

$$p = \frac{dW}{dt} + F\frac{dg}{dt} \tag{3.5}$$

where we identify the power p delivered to the capacitor as going into increasing the energy storage W and mechanical power $F\frac{dg}{dt}$ in moving a part of the capacitor

$$W = \frac{1}{2}C(g)v^2, \qquad F = \frac{1}{2}v^2\frac{dC(g)}{dg} \tag{3.6}$$

The stored energy and force can be expressed in terms of the charge as

$$W = \frac{1}{2}\frac{q^2}{C(g)}, \quad F = \frac{1}{2}\frac{q^2}{C^2(g)}\frac{dC(g)}{dg} \tag{3.7}$$

But the capacitance in terms of its physical dimensions and dielectric is

$$C(g) = \frac{\varepsilon_0 WL}{g} \tag{3.8}$$

Then the force on the plate is

$$F = \frac{1}{2}v^2\frac{dC(g)}{dg} = -\frac{1}{2}\frac{\varepsilon_0 WLv^2}{g^2} \tag{3.9}$$

where v is the applied voltage between the plates.

$$\frac{1}{2}\frac{\varepsilon_0 WLv^2}{g^2} = k(g_0 - g) \tag{3.10}$$

v can be written in terms of other parameters

$$v = \sqrt{\frac{2k}{\varepsilon_0 WL}g^2(g_0 - g)} \tag{3.11}$$

Then setting the derivative of v with respect g (gap height) to zero gives the gap height at which the instability occurs.

$$\frac{dv}{dg}=\frac{d}{dg}\sqrt{\frac{2k}{\varepsilon_0 WL}g^2(g_0-g)}=\sqrt{\frac{2k}{\varepsilon_0 WL}}\left(\sqrt{g_0-g}-\frac{g}{2\sqrt{g_0-g}}\right) \tag{3.12}$$

$$\left.\frac{dv}{dg}\right|_{g=g_p}=0\Rightarrow\sqrt{\frac{2k}{\varepsilon_0 WL}}\left(\sqrt{g_0-g_p}-\frac{g_p}{2\sqrt{g_0-g_p}}\right)=0\Rightarrow g_p=\frac{2}{3}g_0 \tag{3.13}$$

Substituting the value found for g in (3.13) into equation (3.11), the corresponding voltage that is called "pull-in" or "pull-down" voltage is found to be

$$V_p=v(g_p)=\sqrt{\frac{8k}{27\varepsilon_0 WL}g_0^3} \tag{3.14}$$

3.2 Advantages and Disadvantages

Electrostatic actuation is the most prevalent actuation mechanism used in RF MEMS switches. It virtually consumes no power, has small electrode size, thin layers are used in it, and it has short switching time. But it needs an actuation voltage in range of tens of Volts to more than 100 V, and this dictates the use of a voltage upconverter to make required actuation voltage from the voltages in range of 3-5 V used in CMOS ICs.

In other actuation schemes, required actuation voltage is several Volts, but much more power is consumed is thermal and magnetic ones and switching is slower (piezoelectric actuation has near zero power consumption and fast switching speed).

MEMS switches compare well with solid-state switches (GaAs PIN diode and FET) in low to medium power applications and are superior to them in many aspects.

Reliability and packaging of RF-MEMS components seem to be the two critical issues that need to be solved before they receive wider acceptance by the market.

Also stiction is a limiting factor in operation of switches. All MEMS devices face the problem of stiction, during fabrication or in use. Stiction refers to the capillary forces exerted on the microstructures from a liquid between structures themselves or between structures and substrate either during the final drying step of wet processing or by condensation of water vapor during the device operation. There are several to reduce the likelihood of stiction in MEMS devices.

3.3 Design

According to Ostenberg et al [106-109], some test structures can be fabricated to test the mechanism of switching in an electrostatically actuated switch and extract the material properties with a simple method. These structures (Figure 3.1) are electrostatically actuated cantilever beams (CB), fixed-fixed beams (FB) and clamped circular diaphragms (CD). CB is fixed at one-end but FB is fixed at both ends. CD is fixed at its wide end. CBs, FBs and CDs are suspended above a ground plane by a gap. A voltage is applied to the upper conductor (that is movable) causing it to deflect downward toward the underlying fixed ground plane due to the electrostatic attraction force. At a critical pull-in voltage, the upper conductor pulls in to the ground plane (and touches the ground plane). The pull-in voltage is related to geometry on the test structure and the material properties. The length or radius can be described in terms of pull-in voltage, Young's modulus, Poisson's ratio, thickness and gap spacing. These equations can be used to design beams for desired pull-in voltages. In equations 3.15-3.17 the equations for the length of fixed beam (L_{CB}), length of fixed-fixed beam (L_{FB}) and the radius of the clamped circular diaphragms (R_{CD}) are given, respectively [101-103].

$$L_{CB} = \sqrt[4]{\frac{16\widetilde{E}t^3 g_0^3}{81\varepsilon_0 V_{PI}^2}} \tag{3.15}$$

$$L_{FB} = \sqrt{\frac{8\widetilde{\sigma}t + \sqrt{64\widetilde{\sigma}^2 t^2 + \frac{432\varepsilon_0 \widetilde{E}t^3 V_{PI}^2}{g_0^3}}}{\frac{27\varepsilon_0 V_{PI}^2}{4g_0^3}}} \tag{3.16}$$

$$R_{CD} = \sqrt{\frac{4\widetilde{\sigma}t + \sqrt{16\widetilde{\sigma}^2 t^2 + \frac{72\varepsilon_0 \widetilde{E}t^3 V_{PI}^2}{g_0^3}}}{\frac{27\varepsilon_0 V_{PI}^2}{4g_0^3}}} \tag{3.17}$$

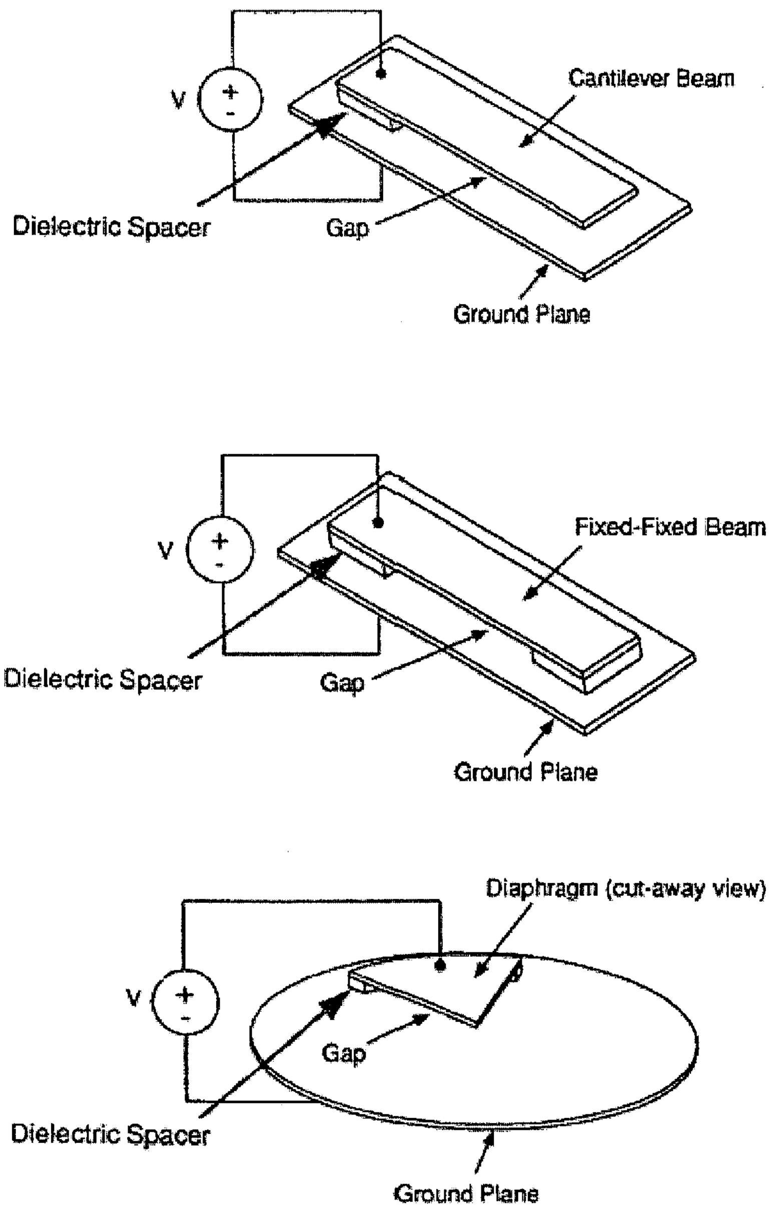

Figure 3.1 Possible Test Structures [106-108]

where $\widetilde{E}$ is effective modulus, $\widetilde{\sigma}$ is the effective residual stress, t is the structure thickness, g_0 is the non-deformed gap, ε_0 is the permittivity of the vacuum and V_{PI} is the pull-in voltage.

For CDs, $\widetilde{E} = \frac{E}{1-\nu^2}$ and $\widetilde{\sigma} = \sigma_0$ where E is the Young's modulus, ν is the Poisson's ratio and σ_0 is the biaxial residual stress. For CBs and FBs with $w >= t$ (w is beam width), $\widetilde{E} = \frac{E}{1-\nu^2}$. For FBs, $\widetilde{\sigma} = \sigma_0(1-\nu)$ and for CBs, $\widetilde{\sigma} = 0$. For FBs, it is assumed that $L >> w$, $L >> t$ where L is the length of the beam.

In MUMPS, there are only three Polysilicon layers, therefore g_0 could take three values. t is also fixed . So the only design parameter is length/radius. The possible cases for g_0 and t are:

1. Case 1: Ground plane in Poly0, beam in Poly1: $g_0 = 2\mu m$ and $t = 2\mu m$
2. Case 2: Ground plane in Poly0, beam in Poly2: $g_0 = 5.5\mu m$ and $t = 1.5\mu m$
3. Case 3: Ground plane in Poly1, beam in Poly2: $g_0 = 1.5\mu m$ and $t = 1.5\mu m$

To find beam lengths/radii, an estimate of Young's modulus, Poisson's ratio and residual stress required. We use average bulk values of them for Polysilicon as [109]

$E = 169 \times 10^6\ Pa$, $\nu = 0.26$ and $\widetilde{\sigma} = 5 \times 10^6\ Pa$ is the average value given in [106-108].

Using MATLAB, length/radius versus pull-in voltage for three cases is shown in figures 3.2 to 3.10.

In [106-108] it is mentioned that the minimum number of beams should be 8. Selected lengths of FBs are shown in Figure 3.11.

In the available spaces three sets are beams in Poly1 layer are placed. Each set of FBs is above a rectangular ground plane in Poly1. Patterns are repeated to get a better result.

In one set of FBs some etch holes are provided on the beams to observe effect of them on behavior of the beams.

a, b, c, and e dimensions and d (number of holes), are given in tables 3.1, 3.2, and 3.3.

The top view of one beam connected to a bonding pad is shown in Figure 3.12.

Layout of the beams extracted from Cadence is shown in Figure 3.13.

Electrical connections are made using metallic pads. Each beam has one pad connected to one end, and for ground planes there are one or two pads on it

Ends of the beams are fixed using anchors. The Poly0 under anchors is removed to prevent having an electrical path directly between Poly1 and Poly0 layers.

The designed switches are also simulated in ANSYS software that takes advantage of finite element method (FEM). Simulation results are verified with design and pull-in voltages are close to designed values.

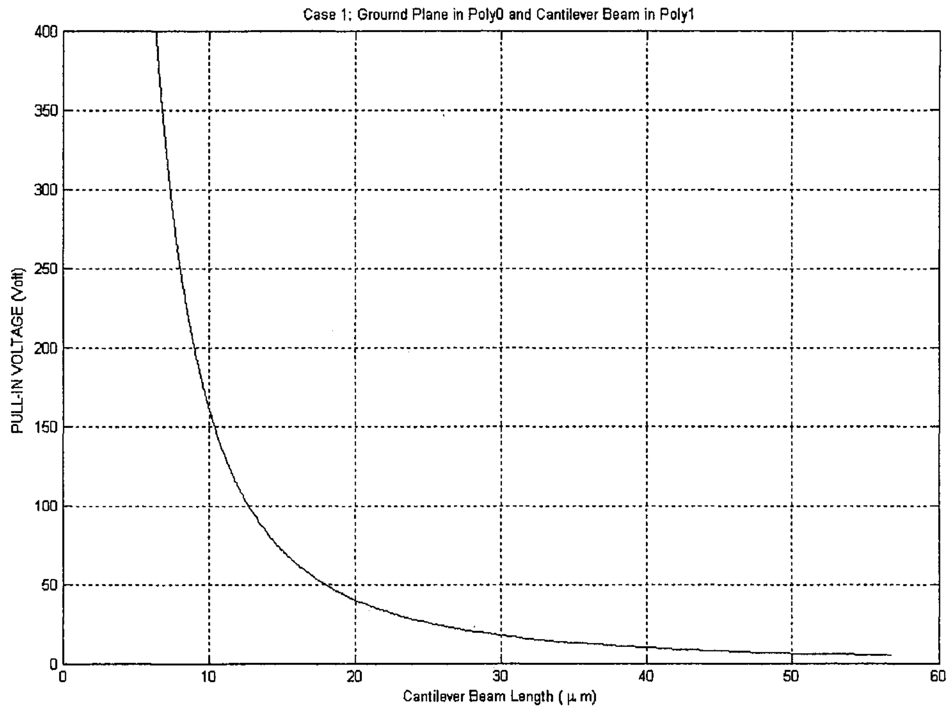

Figure 3.2 Case 1: Pull-in Voltage Between a Fixed Beam in Poly1 and the Poly0 Plane

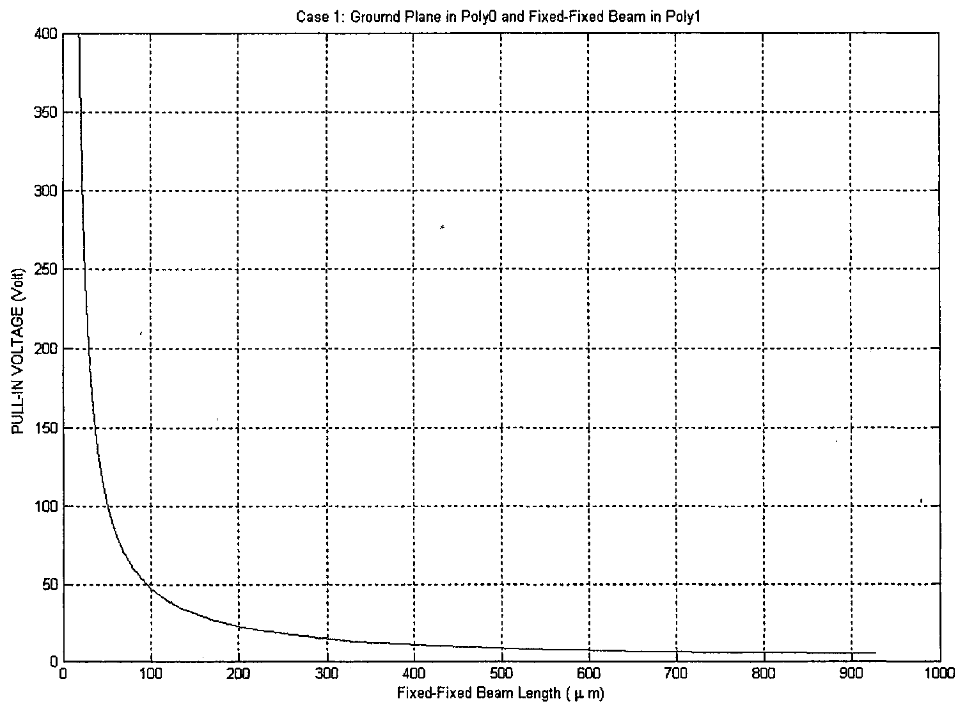

Figure 3.3 Case 1: Pull-in Voltage Between a Fixed-Fixed Beam in Poly1 and the Poly0 Plane

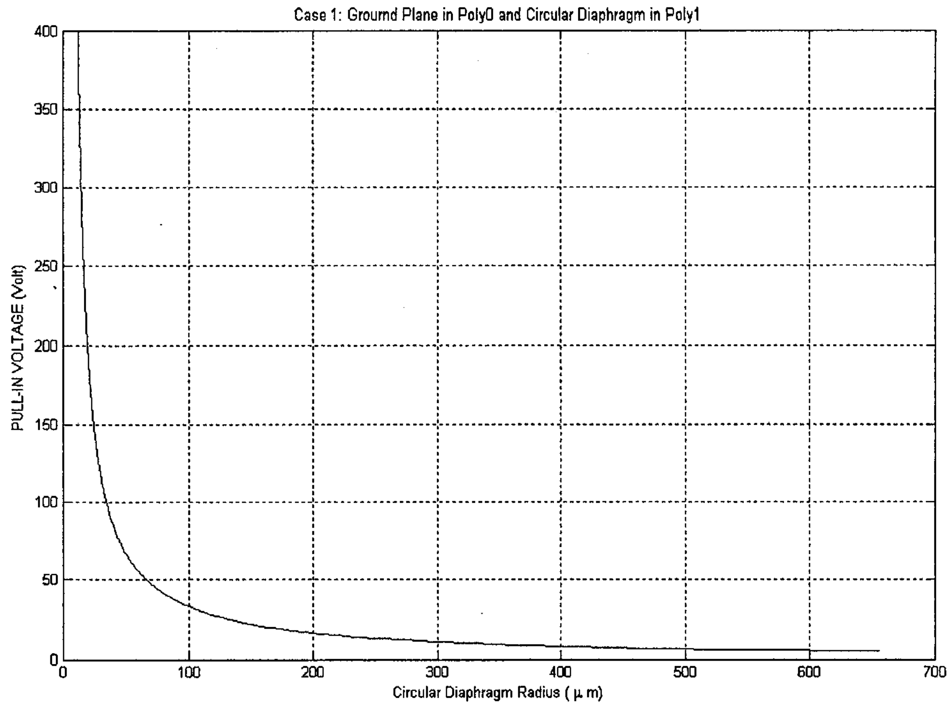

Figure 3.4 Case 1: Pull-in Voltage Between a Circular Diaphragm in Poly1 and the Poly0 Plane

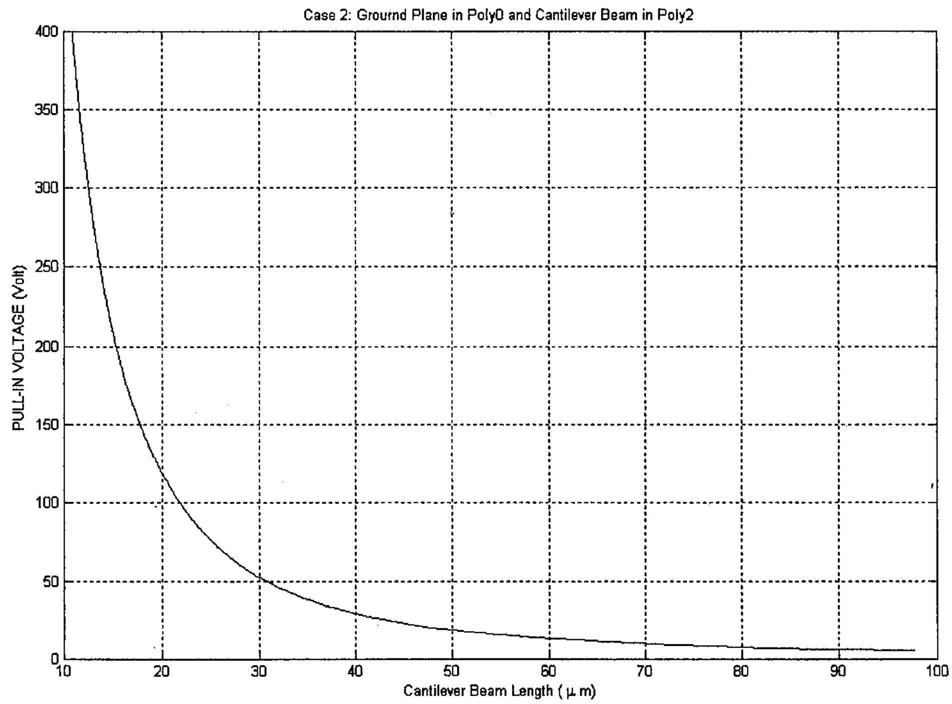

Figure 3.5 Case 2: Pull-in Voltage Between a Fixed Beam in Poly2 and the Poly0 Plane

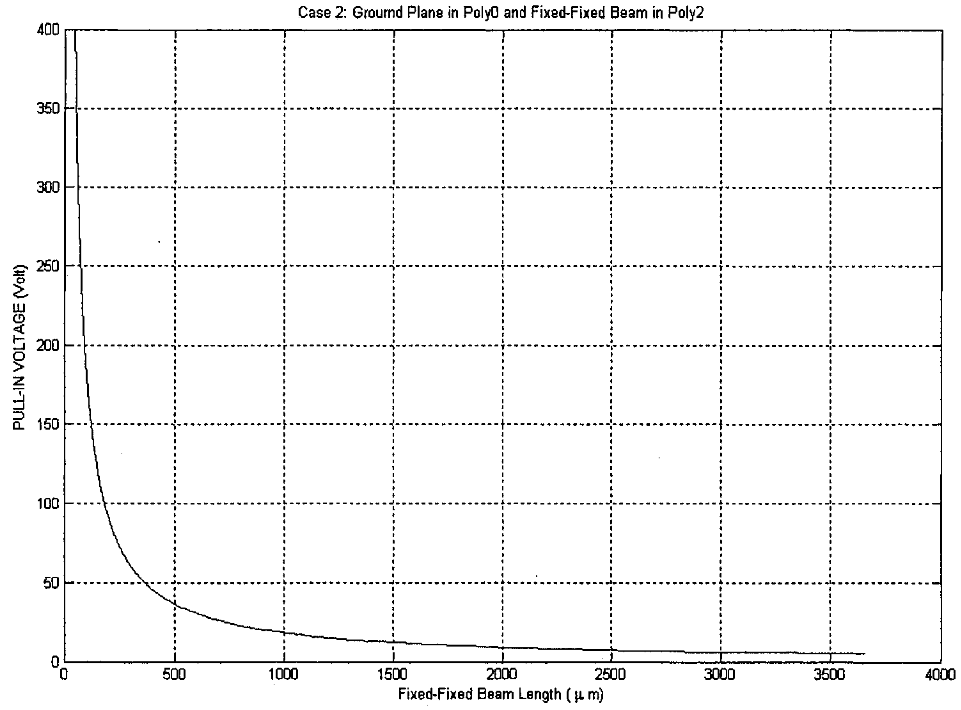

Figure 3.6 Case 2: Pull-in Voltage Between a Fixed-Fixed Beam in Poly2 and the Poly0 Plane

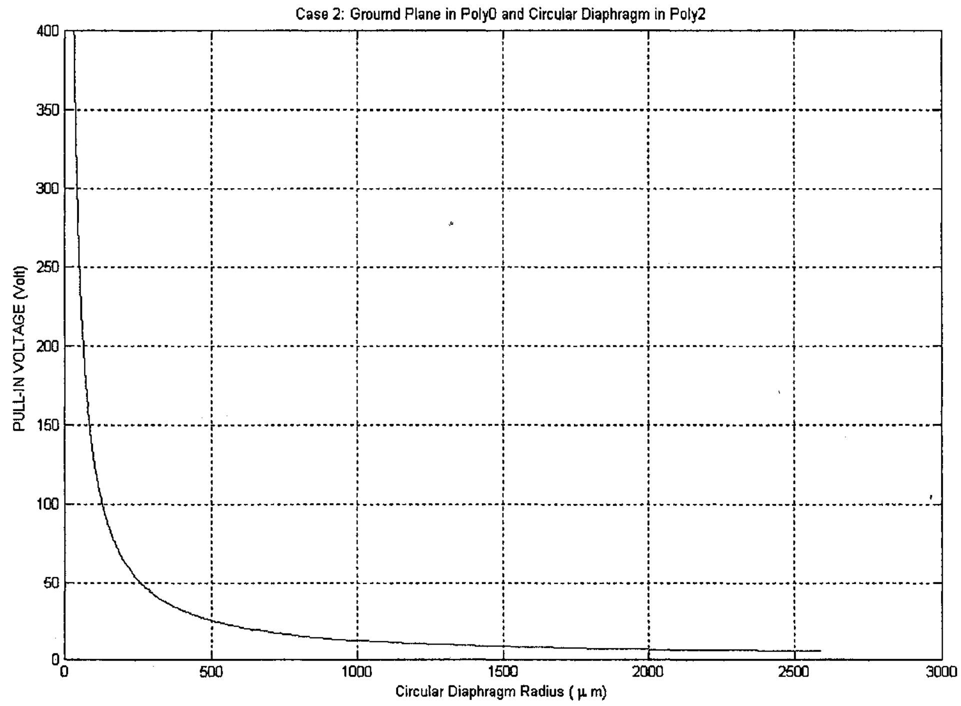

Figure 3.7 Case 2: Pull-in Voltage Between a Circular Diaphragm in Poly2 and the Poly0 Plane

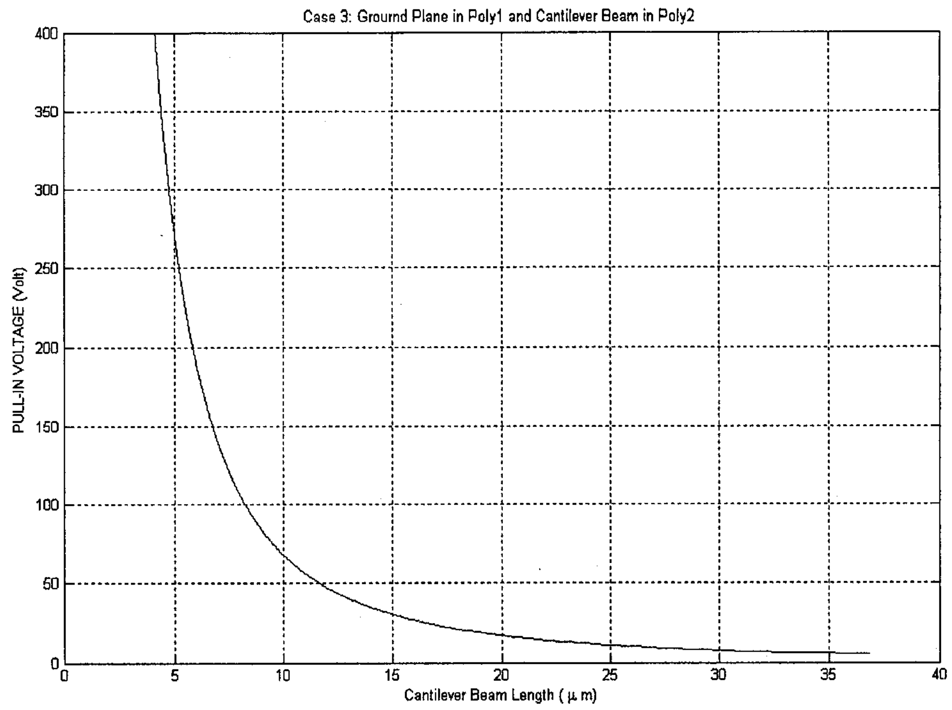

Figure 3.8 Case 3: Pull-in Voltage Between a Fixed Beam in Poly2 and the Poly1 Plane

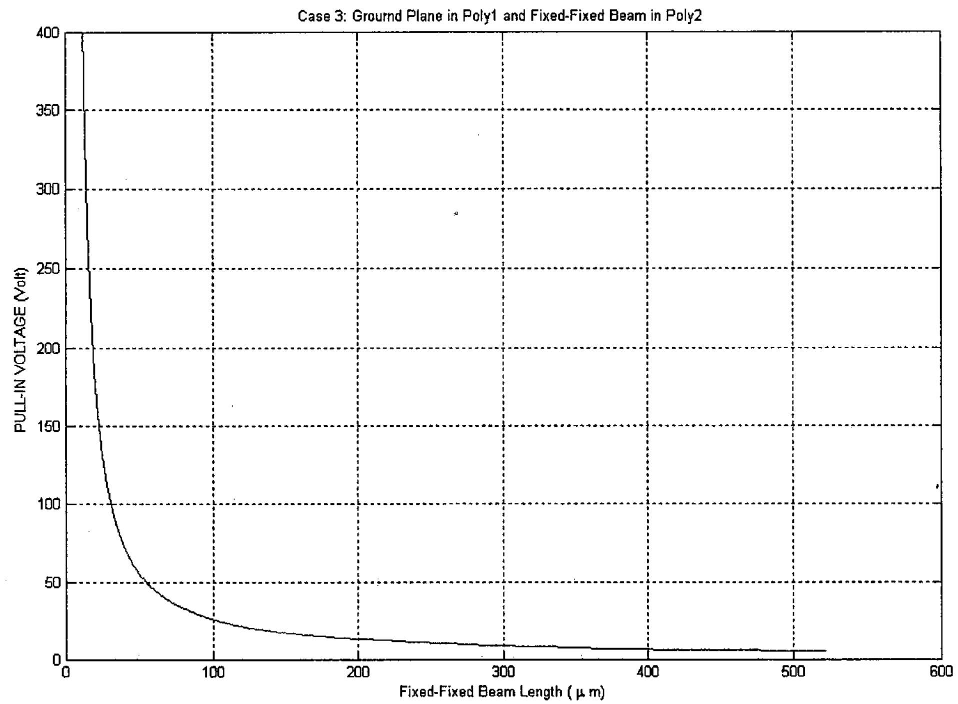

Figure 3.9 Case 3: Pull-in Voltage Between a Fixed-Fixed Beam in Poly2 and the Poly0 Plane

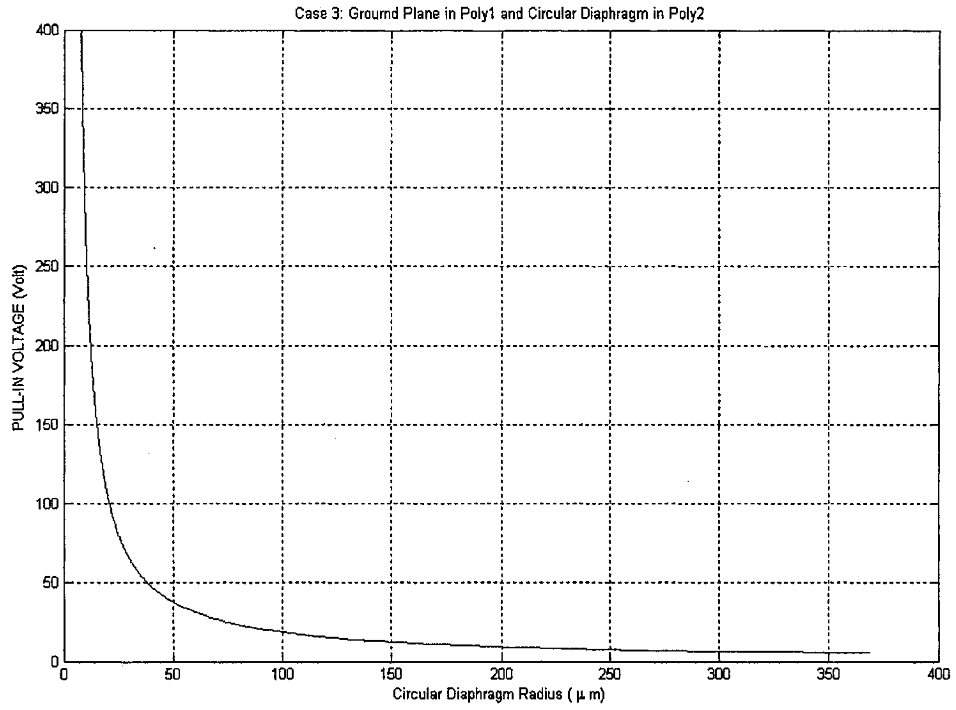

Figure 3.10 Case 3: Pull-in Voltage Between a Circular Diaphragm in Poly2 and the Poly1 Plane

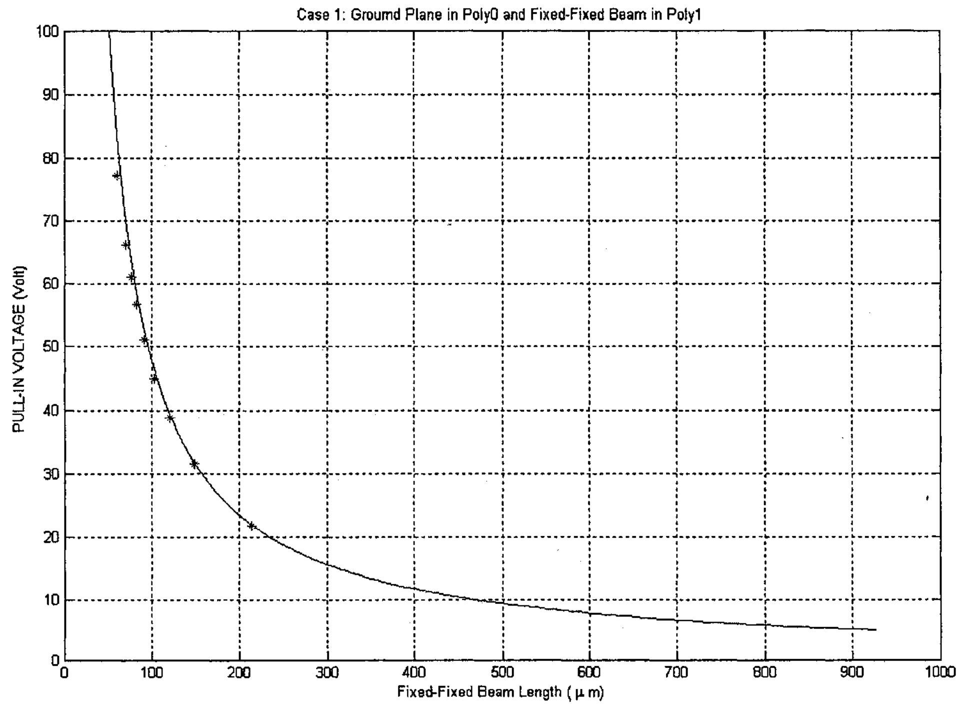

Figure 3.11 Pull-in Voltages Between Designed Fixed-Fixed Beams in Poly1 and the Poly0 Plane

Three sets of fixed-fixed beams are designed. The beams are in Poly1 layer and the ground electrode is a plane in Poly0 layer. The dimensions of designed beams are given in tables 3.1-3.3. The dimension parameters are shown on a typical beam in Figure 3.12

Beam	1	2	3	4	5	6	7	8	9
a(μm)	47	45	52.2	49	55.9	45	45	48	45
b(μm)	148	148	120	103	91	82	76	70	66
c(μm)	303	567	821	1102	1366	1626	1894	2151	2414
d(μm)	19	19	16	13	12	11	0	0	0
e(μm)	65.3	65.3	65.3	65.3	65.3	65.3	65.3	65.3	65.3

Table 3.1 Dimensions for first set

Beam	18	17	16	15	14	13	12	11	10
a(μm)	45	48	45	45	56	49.1	52	44.9	47
b(μm)	66	70	76	82	91	103	120	148	148
c(μm)	307.1	570.1	827.1	1094.7	1355.1	1618.7	1899.7	2154.1	2418.1
d(μm)	0	0	0	0	0	0	0	0	0
e(μm)	65.1	65.1	65.1	65.1	65.1	65.1	65.1	65.1	65.1

Table 3.2 Dimensions for second set

Beam	19	20	21	22	23	24	25	26	27	28
a(μm)	46	47	45	52	49	56	45	45	48	45
b(μm)	214	148	148	120	103	91	82	76	70	60
c(μm)	41	303	567	821	1102	1366	1626	1894	2151	2414
d(μm)	0	0	0	0	0	0	0	0	0	0
e(μm)	65.3	65.3	65.3	65.3	65.3	65.3	65.3	65.3	65.3	65.3

Table 3.3Dimensions for third set

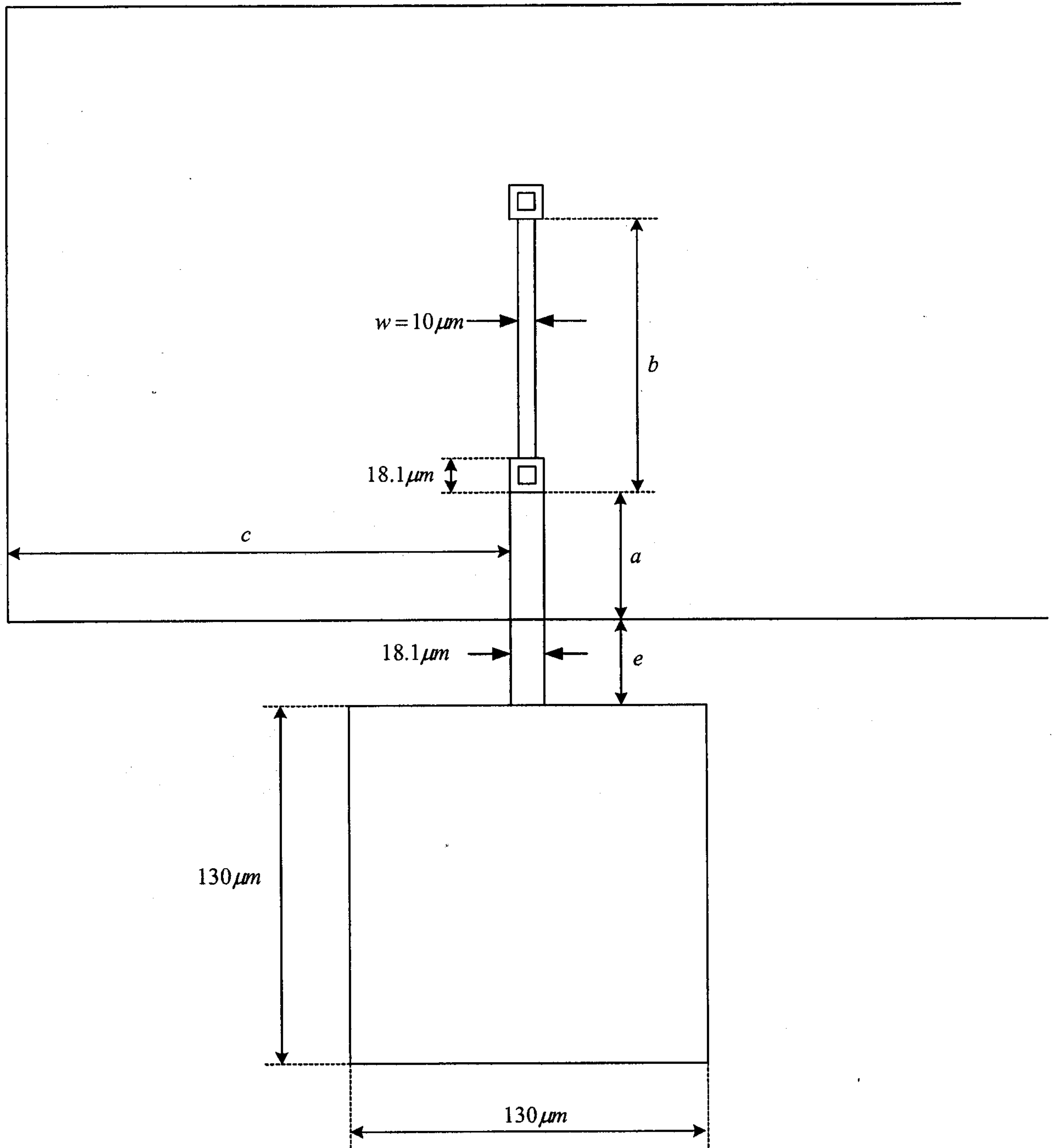

Figure 3.12 Top View of a FB Connected to a Pad

The layout of beams drawn in Cadence is shown in Figure 3.13. The beams are numbered from 1 to 28 and the bonding pads are numbered from P1 to P33. The same beam numbering is used in tables 3.1-3.3.

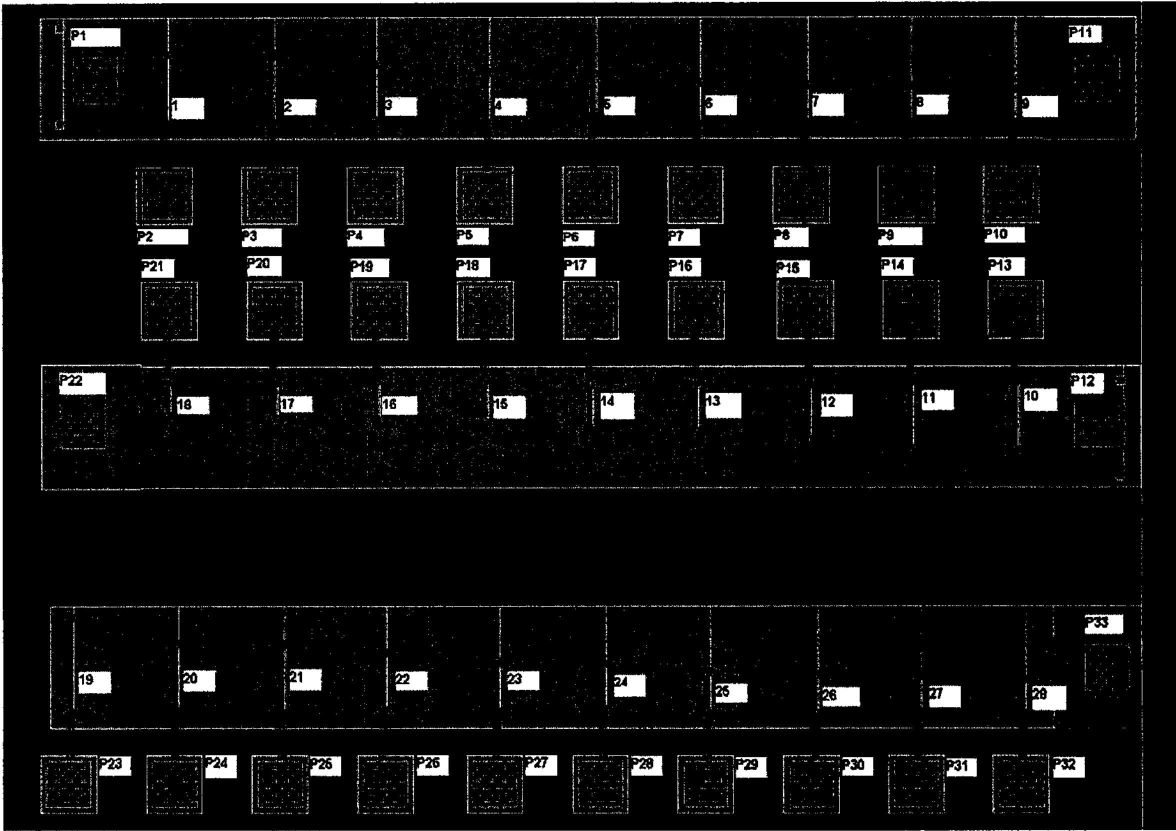

Figure 3.13 Layout of the Beams Designed by Cadence

Top view of a beam with etch holes is shown in Figure 3.14. Etch holes facilitate surface micromachining by letting the etchant reach the sacrificial material beneath the beam.

Figure 3.14 Top View of a Beam with Etch Holes

The three-dimensional view of a beam with etch holes is shown in Figure 3.15. In Figure 3.16 the three-dimensional view of one row of beams is shown.

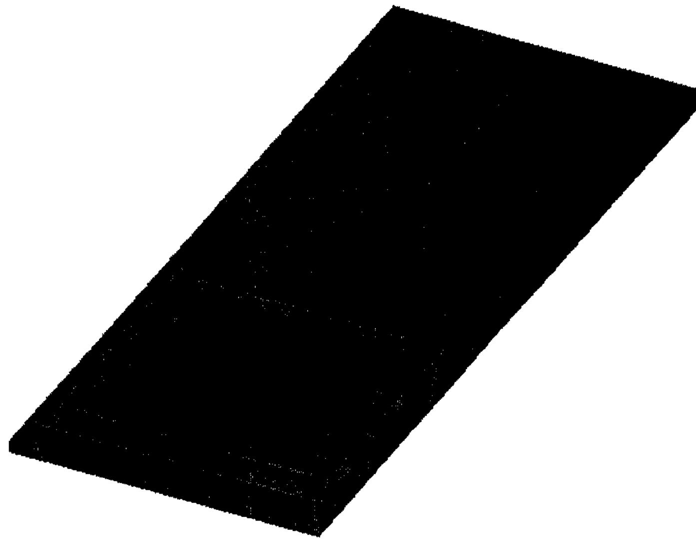

Figure 3.15 3D View of a Beam with Etch Holes

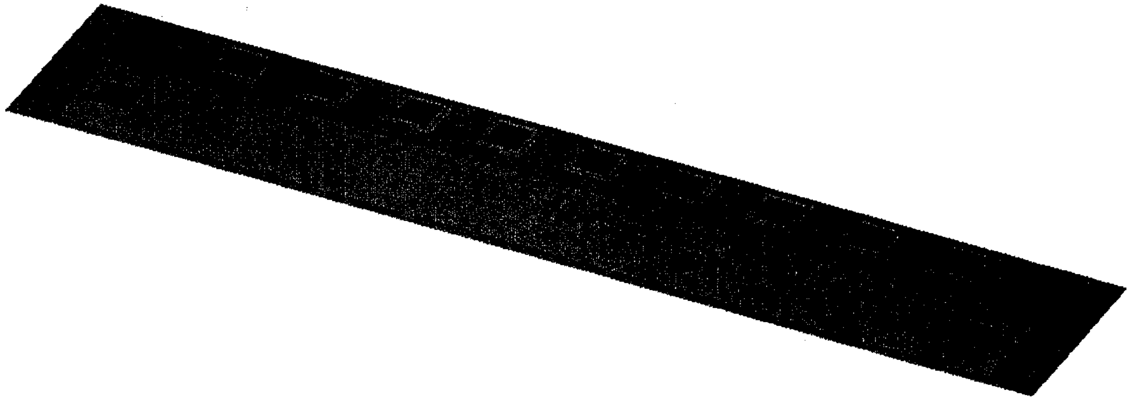

Figure 3.16 View of One Row of Beams

4. Design and Simulation RF MEMS Inductors

4.1 Inductors

Inductors are an essential part of many active and passive RF circuits and are used in many analog integrated circuits. They are used as in filters, oscillators, amplifiers, and other circuits. In discrete circuits, it's easy to use a high quality inductor. But in integrated circuits it's a different story. Implementing an inductor in a VLSI process technology gives us new potentials but has many challenges and limitations. Taking advantage of MEMS technology (surface and bulk micromachining techniques), very small inductors with improved performance can be made.

Inductors are used in many circuits including oscillators and voltage controlled ocsillators, amplifiers, matching networks, filters, and bias chokes.

The overall quality of a circuit is related to the quality factor (Q) of the inductor(s) used in them, increasing Q affects different circuits as follow [9]:

- Oscillator phase noise and power consumption reduction
- Amplifier gain increase and power consumption reduction
- Matching network loss reduction
- Filter loss reduction
- Overall System noise figure reduction

Therefore fabricating high Q inductors make them suitable for low-noise amplifiers, high-gain amplifiers, on-chip matching networks, and integrated LC filters.

4.1.1 Inductor Structures

VLSI technology is well suited to planar structures the same way that CMOS ICs are fabricated. Also it is possible to create non-planar three-dimensional structures employing VLSI technology.

Straight sections of ribbons (known as strip or ribbon inductors) or bonding wires are used for low inductance values. Spiral inductors (circular or polygonal[7]) have higher Q and can provide higher inductance values. These inductors are commonly used for high-density circuits [93].

The most popular inductors are the planar ones. Among them, the spiral (circular and polygonal) structure is widely used. Other layouts such as half loops, and full loops, have also been used.

Not many non-planar 3D coils have been fabricated. An example of a surface micromachined solenoid-shape inductor [110] is shown in Figure 4.1.

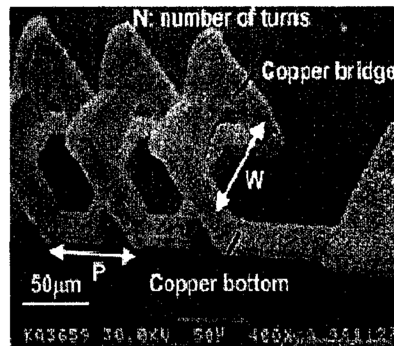

Figure 4.1 Surface Micromachined Solenoid [110]

Micromachined inductors are usually based on four different technologies [9]:

---

[7] Polygonals such as square, hexagonal and octagonal

1. Thick metal electroplating to reduce the inductor series resistance
2. Three dimensional solenoid type inductors to result in large-value designs
3. Substrate etching underneath the inductor to reduce the parasitic capacitance to the substrate or flip-chip bonding on an etched substrate
4. Self-assembly of the inductor away from the substrate to reduce the parasitic capacitance to the substrate

The inductors are integrated on the top metal layer and are separated from the silicon substrate using oxide (silicon oxide) layers with a thickness of several microns. The oxide layers reduce the parasitic capacitance, and they allow the integration of large value inductors without having problems with the inductor resonant frequency.

Thick-metal electroplating or substrate etching or any other post-processing is an additional step in the fabrication process and results in an increased cost and delay [9].

4.1.2 Variable (Tunable) Inductors

Making a variable inductor with stable, repeatable characteristic is a challenge. An Example of a variable inductor [111] is shown in Figure 4.2.

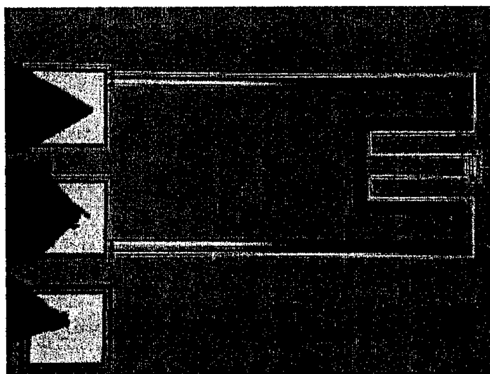

Figure 4.2 Tunable Inductor [111]

It is also possible to make a variable inductor by using combination of fixed inductors and switches [112].

4.2 Inductor Design

There are numerous models for on-chip inductors considering various physical phenomena. A few of them are modified Wheeler, current sheet approximation and data fitted monomial expressions from experimental results. [113]

For a given spiral shape, an inductor is completely specified by the number of turns n, the turn width w, the turn spacing s, and anyone of the following:

The outer diameter d_{out}, the inner diameter d_{in}, the average diameter d_{avg}, or the fill ratio r. d_{avg} and r are defined in terms of d_{in} and d_{out} as

$$d_{avg} = \frac{d_{out} + d_{in}}{2} \tag{4.1}$$

$$r = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{4.2}$$

The relationship between d_{out}, d_{in} can be described in terms of w and s but depends on the spiral shape (circular, octagonal, ...).

The thickness of the inductor has only a very small effect on inductance and is ignored in following formulas.

At low frequencies, the limiting factor of Q is the inductance series resistance. One needs a metal thickness of at least twice the skin depth [114] in order to obtain the lowest possible RF resistance. In this case the sheet resistance (resistance per unit area) is given

by $R_s = \dfrac{\rho}{\delta}$ (4.3)

where $\rho(\Omega \cdot m)$ is the metal resistivity and δ is the skin depth of the conductor given by

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{4.4}$$

where μ is the permeability of the conductor (free space permeability for non magnetic metals) and f is the operating frequency [9].

4.2.1 Modified Wheeler Inductor Model

Wheeler [115] has presented several formulas for planar discrete spiral inductors. It has been modified for planar integrated spiral inductors [113]. Modified Wheeler formula models the inductor as

$$L_{mw} = K_1 \mu \frac{n^2 d_{avg}}{1 + K_2 r} \tag{4.5}$$

where L_{mw} is the inductance value calculated using modified Wheeler formula, K_1 and K_2 are constants that are defined in the Table 4.1, n is number of turns, μ is the permeability of the conductor, d_{avg} is the average diameter defined in equation 4.1 and r is the fill factor defined in equation 4.2.

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	5.82
Octagonal	2.25	5.55

Table 4.1 Modified Wheeler Model Parameters

4.2.2 Current Sheet Approximation

Another simple expression for a planar inductor can be obtained by approximating the sides of the spirals by symmetrical current sheets of equivalent current densities [116]. The resulting expression is [113]

$$L_{csa} = \frac{\mu n^2 d_{avg} C_1}{2}\left[\ln\left(\frac{C_2}{r}\right) + C_3 r + C_4 r^2\right] \quad (4.6)$$

where L_{csa} is the inductance value calculated using modified current sheep approximation formula, μ is the permeability of the conductor, n is number of turns, d_{avg} is the average diameter defined in equation 4.1, C_1, C_2, C_3 and C_4 are layout dependent constants that are defined in the Table 4.2 and r is the fill factor defined in equation 4.2.

The accuracy of this expression worsens as the ratio of $\frac{s}{w}$ (turn spacing to width) becomes large.

Layout	C_1	C_2	C_3	C_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circular	1.00	2.46	0.00	0.20

Table 4.2 Parameters of Current Sheet Approximation Model

4.2.3 Data-Fitted Monomial Expressions

Data fitting technique has yielded the expression [113]

$$L_{mon} = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \quad (4.7)$$

where L_{csa} is the inductance value calculated using data-fitted monomial formula, the constant $\beta, \alpha_1, \alpha_2, \alpha_3, \alpha_4$ and α_5 are layout dependent given in the Table 4.3, d_{out} is the outer diameter of the inductor, w is the turn width, d_{avg} is the average diameter defined in equation 4.1, n is number of turns and s is the turn spacing.

Layout	β	α_1	α_2	α_3	α_4	α_5
Square	1.62×10^{-3}	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	1.28×10^{-3}	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	1.33×10^{-3}	-1.21	-0.163	2.43	1.75	-0.049

Table 4.3 Data Fitting Constants

4.2.4 Strip (Ribbon) Inductor

Thin conductor strips of rectangular cross-section deposited on dielectric substrates are often used for low inductance values. The inductance of a strip inductor (shown in Figure 4.3) [93] is given as

$$L(nH) = 2\times10^{-4}\left[\ln\left(\frac{l}{w+t}\right) + 1.193 + 0.2235\left(\frac{w+t}{l}\right)\right]\cdot K_g \tag{4.8}$$

where L is the inductance in nanoHenries, l, w and t are length, width and thickness, respectively and K_g is a correction factor.

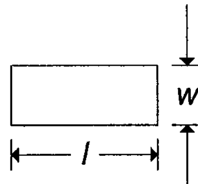

Figure 4.3 Strip Inductor

The circuit model of a strip inductor is shown in Figure 4.4.

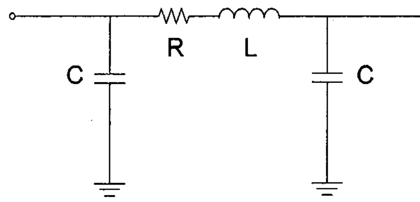

Figure 4.4 Circuit Model of a Strip Inductor

4.2.5 Loop Inductor

Inductance of a loop inductor (shown in Figure 4.5) is given as [93]

$$L(nH) = 1.257 \times 10^{-3} a \left[\ln\left(\frac{a}{w+t} \right) + 0.078 \right] \cdot K_g \tag{4.9}$$

where L is the inductance in nanoHenries, a, w and t are loop radius, width and thickness, respectively and K_g is a correction factor.

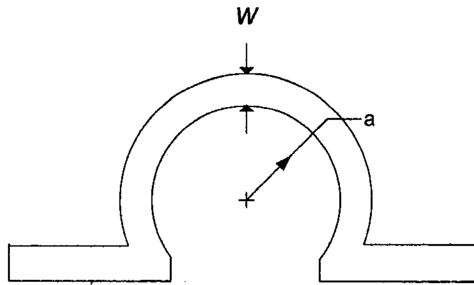

Figure 4.5 Loop Inductor

The circuit model of a loop inductor is shown in Figure 4.6.

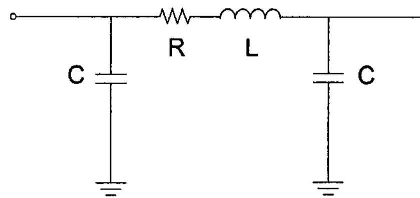

Figure 4.6 Circuit Model of Loop Inductor

4.2.6 Bonding wire inductor

In hybrid MICs, bonding wire connections are used to connect active and passive circuit components, and in MMICs bonding wire connections are used to connect the MMIC chip to the real world. The free-space inductance of a wire of diameter d and length l (in microns) is given [93] by

$$L = 2\times10^{-4} l \left[\ln\left(\frac{4d}{l}\right) + 0.5\frac{d}{l} - 0.75 \right] \tag{4.10}$$

where L is the inductance in nanoHenrys.

4.3 Lumped-Element Models of Inductors

Inductors have been modeled based on physical phenomena happening at different frequencies. Several of these models are given in figures 4.7 to 4.9.

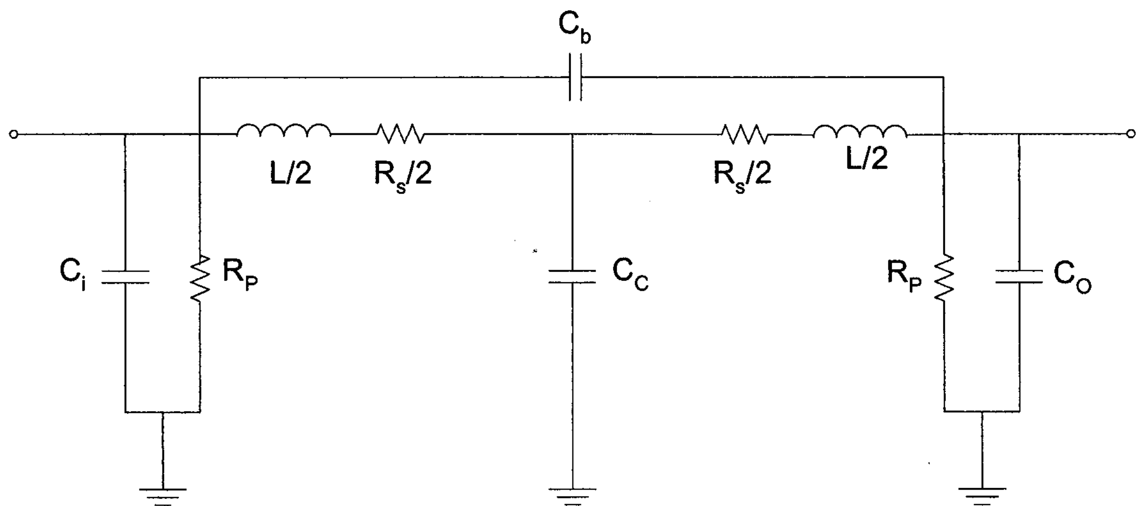

Figure 4.7 Inductor Model 1 [17]

A general model describing the performance of a planar inductor is shown in figure 4.8. L_s is the inductance, R_s is the series resistance of the coil, C_s is the capacitance between the different windings of the inductor and includes the fields in air and the supporting

dielectric layers. C_1 is the capacitance in the oxide layer between the coil and the substrate, C_p is the capacitance between the coil and the ground through the substrate, and R_p is the eddy current loss in the substrate [9].

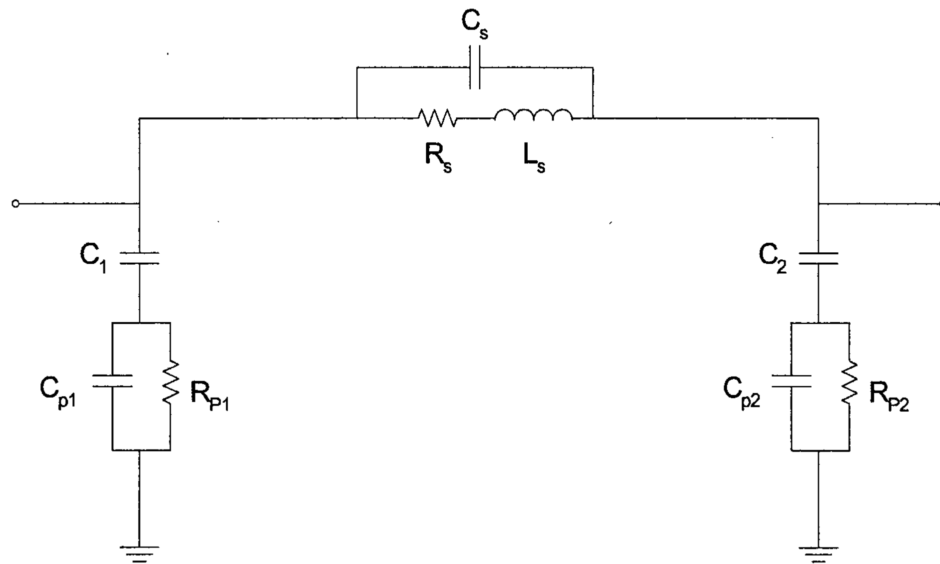

Figure 4.8 Inductor Model 2 [9]

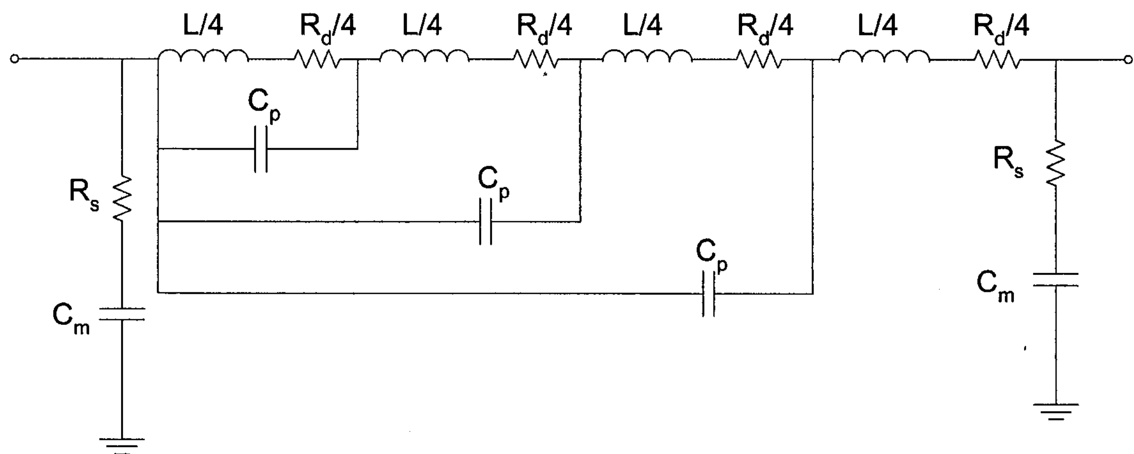

Figure 4.9 Inductor Model 3 [117]

4.4 Spiral Layout Parameters

A spiral inductor layout is defined by w width of turns, s distance between turns, n number of turns and one of the parameters d_{out}, d_{in}, d_{avg}, or r that are defined in section 4.2. For the spiral inductors, d_{out} is expressed in terms of d_{in}, w, s, and n as

$$d_{out} = d_{in} + 2nw + 2(n-1)s \qquad (4.11)$$

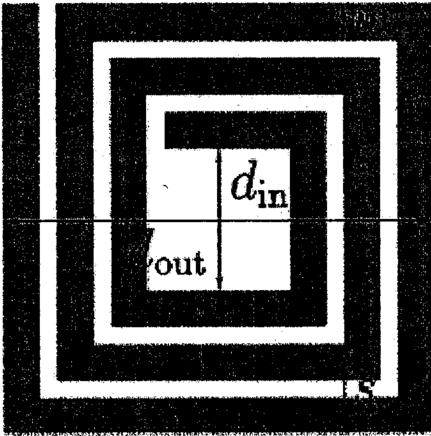

Figure 4.10 square spiral inductor

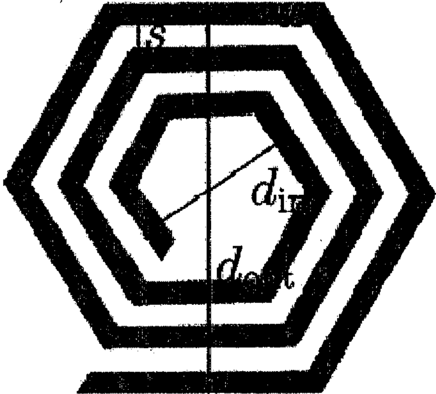

Figure 4.11 Hexagonal Spiral Inductor

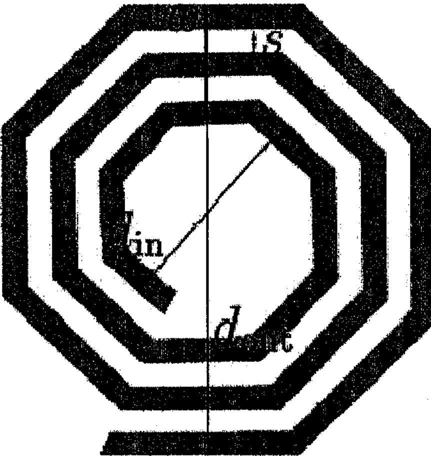

Figure 4.12 Octagonal Spiral Inductor

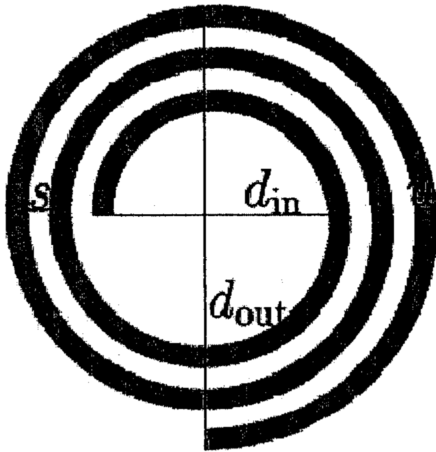

Figure 4.13 Circular Spiral Inductor

4.5 Inductor Design Considerations

Some advices on inductor designs are given by Bahl [93].

1. In the spiral, $w >> s$ that is, the separation s between the turns should be as small as possible.
2. There should be some space at the center of the spiral to allow the flux lines to pass through, which increases the stored energy. It has been found that $\frac{d_{out}}{d_{in}} = 5$ yields an optimum value of Q (quality factor), but not the maximum inductance value.
3. The maximum diameter of the inductor should be less than $\lambda / 30$ (λ is the wavelength) in order to avoid distributed effects.

4.6 Inductor Calculations Using given Models

Inductance calculations are performed in MATLAB. Also calculations to find layout coordinates are done in MATLAB.

Inductance calculations are also compared to values obtained from Stanford online calculator [118].

Between the different processes that are available (through Canadian Microelectronics Corporation), CMOS 0.35 and Poly-MUMPS are used to fabricate MEMS inductors.

In Poly-MUMPS, inductors don't need complicated post-processing, only a simple dipping in oxide etchant will remove the sacrificial oxide layer of the chip. But the number of layers limits the possible designs. But if substrate etching has to be done, then post-processing will be complicated. Top metal layer is used for inductor.

In CMOS 0.35, there are 4 metal layers (these layers are called metal1, metal2, metal3, and metal4) where the metal4 layer is thicker and its conductivity is higher, too [69]. But post-processing is complicated. CMOS 0.35 is not an expensive process but it is more expensive than MUMPS.

In this work, both processes are used to fabricate the coils and the results are compared. Only octagonal and circular spiral layouts are considered in designs. Several inductors are designed with the process limitations considerations. Then a few of them are being selected for fabrication in MUMPS and CMOS processes.

4.7 Designs

In this work two sets of inductors are designed and fabricated. One set is fabricated using the MUMPS process and the other one is fabricated taking advantage of CMOS technology.

4.7.1 MUMPS Designs

Three octagonal spiral inductors are designed and fabricated using the top metal layer of PolyMUMPS process. In all of them, d_{in} the inner diameter of the inductor is 50μm, the turn width w is 12μm and the turn spacing s is 3μm. The turns are different that make values of inductances different. The inductances are calculated using different models that are introduced in section 4.2. The calculated values from different models are very close, so in the table the average result of different models are given. The dimensions and inductances are summarized in Table 4.4

	n	w(µm)	s(µm)	d_{in} (µm)	Inductance (nH)
IND1	6	12	3	50	3.1
IND 2	4	12	3	50	1.1
IND 3	3	12	3	50	0.5

Table 4.4 Specifications of Designed MUMPS Inductors

Layout of MUMPS coils are shown in figures 4.14 to 4.16.

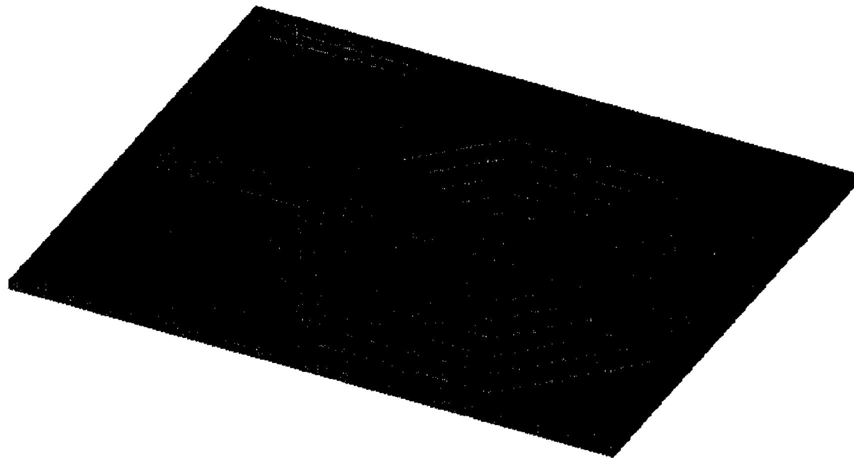

Figure 4.14 MUMPS Inductor IND1: n=6, w=12µm, s=3µm, d_{in}=50µm

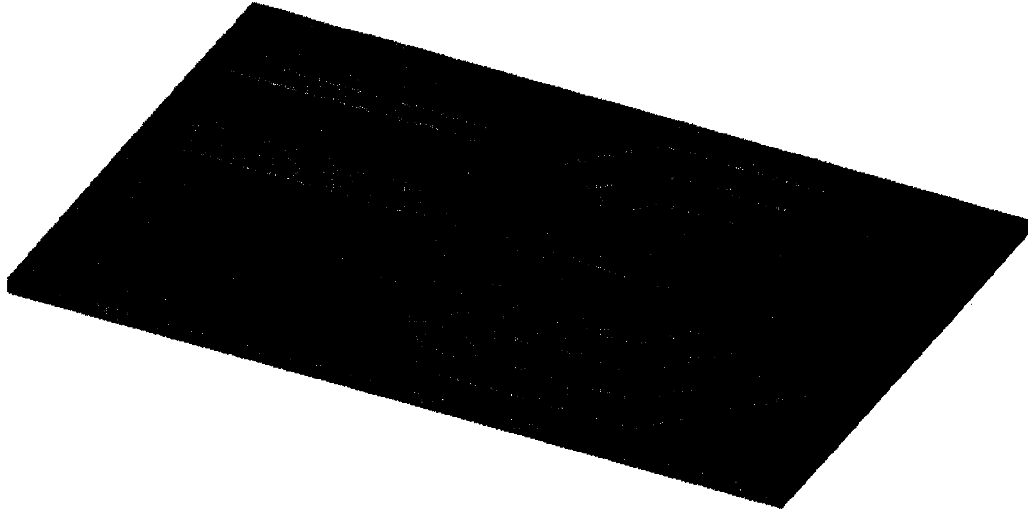

Figure 4.15 MUMPS Inductor IND2: n=4, w=12µm, s=3µm, d_{in}=50µm

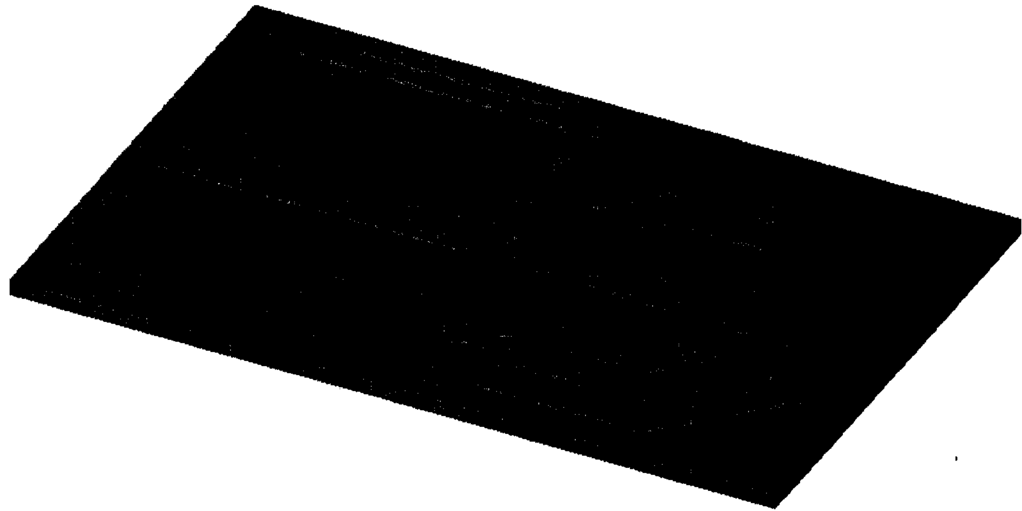

Figure 4.16 MUMPS Inductor IND3: n=3, w=12µm, s=3µm, d_{in}=50µm

4.7.2 CMOS Designs

Two spiral inductors, one octagonal and one circular, are designed and fabricated using the Metal 3 layer in CMOS 0.35 technology. In both inductors, the turn width w is 6μm, the turn spacing s is 2 μm and n number of turns is 5. The inner diameters of the inductors are 19 μm and 18μm, respectively. The inductances are calculated using different models that are introduced in section 4.2. The calculated values from different models are very close, so in the table the average result of different models are given. The dimensions and inductances are summarized in Table 4.5.

	n	w(μm)	s(μm)	d_{in} (μm)	Inductance (nH)	Layer	Shape
Coil1	5	6	2	19	1.2	Metal3	Octagonal
Coil2	5	6	2	18	1.2	Metal3	Circular

Table 4.5 CMOS 0.35 Inductor Specifications

CMOS inductor layouts are given in figures 4.17 and 4.18.

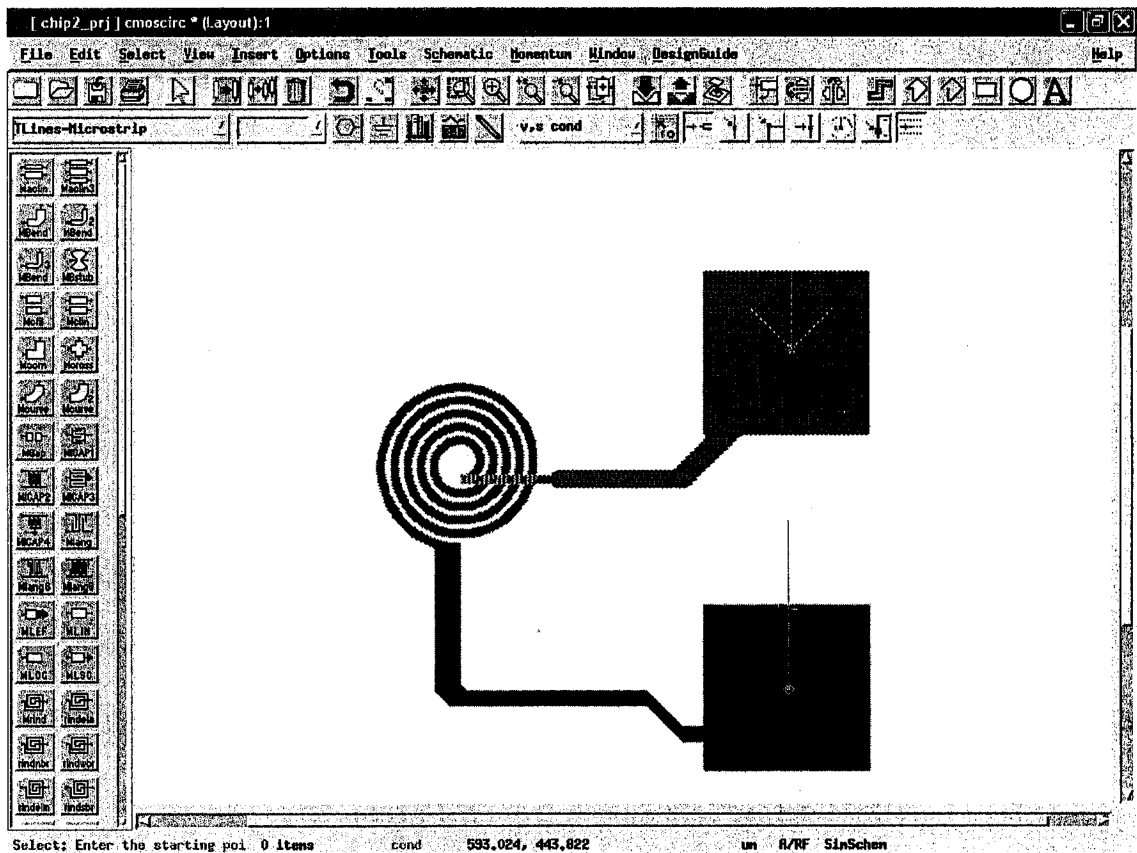

Figure 4.17 CMOS Coil1 (Circular Spiral): n=5, w=6μm, s=2μm, d_{in}=18μm

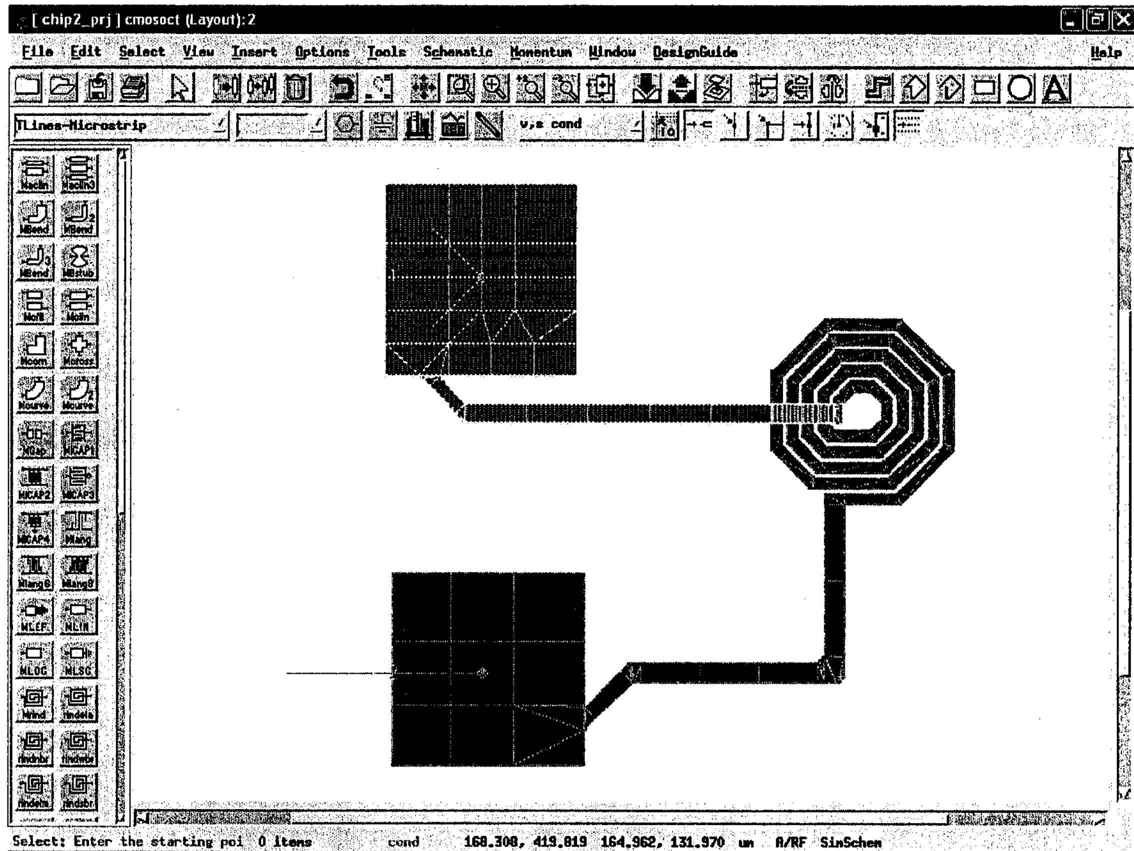

Figure 4.18 CMOS Coil2 (Octagonal Spiral) : n=5, w=6µm, s=2µm, d_{in}=19µm

4.8 Inductor Simulation

Selected inductors are simulated in Advanced Design System (ADS) software Momentum package [119-122]. This software simulates planar microwave structures using the Method of Moments.

4.8.1 Quality Factor Calculation from S-Parameters

At microwave frequencies, when the dimensions of devices become comparable to the wavelength, voltages and currents become distributed variables (compared to lumped variables that are location independent) that depend on the location in the structure. Another problem is that they can't be measured everywhere in the structure. Because of these issues, instead of voltage and current variables, another set of parameters are used

that are called scattering parameters or simply S-parameters [123-124]. They are based on incident and reflected waves and can be measure at input or output ports of devices. Other variables can be calculated from these parameters.

Quality factor is defined as

$$Q = 2\pi \frac{Stored\ Energy}{Energy\ Loss\ in\ One\ Cycle} \tag{4.11}$$

The above definition does not specify what stores or dissipates the energy. For an inductor, only the energy stored in the magnetic field is of interest (not the energy stored in the electric field). Therefore the energy stored is equal to the difference between peak magnetic and electric energies. If the inductor is modeled by a simple parallel *RLC* tank, it can be shown that,

$$Q = 2\pi \frac{Peak\ Magnetic\ Energy - Peak\ Electric\ Energy}{Energy\ Loss\ in\ One\ Cycle} \tag{4.12}$$

$$Q = \frac{R_p}{L\omega}\left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right] = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \tag{4.13}$$

where R_p and L are the equivalent parallel resistance and inductance, respectively, and ω_0 is the resonance frequency , and Z is the impedance seen at one terminal of the inductor while the other is grounded [125-126].

For a load impedance of $Z = R + jX$ and a measured reflection coefficient of Γ, the quality factor is [9]

$$Q = \frac{|\mathrm{Im}(Z)|}{\mathrm{Re}(Z)} \tag{4.14}$$

But load impedance in terms of the reflection coefficient is [123-124]:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \quad \Rightarrow \quad Z = Z_0 \frac{1+\Gamma}{1-\Gamma} \tag{4.15}$$

The real and imaginary parts of a complex number can be written in terms of that number and its complex conjugate

$$Z = \mathrm{Re}(Z) + j\,\mathrm{Im}(Z) \quad \Rightarrow \quad \begin{cases} \mathrm{Re}(Z) = \frac{1}{2}\left(Z + Z^*\right) \\ \mathrm{Im}(Z) = \frac{1}{2j}\left(Z - Z^*\right) \end{cases} \tag{4.16}$$

$$\Gamma = \mathrm{Re}(\Gamma) + j\,\mathrm{Im}(\Gamma) \quad \Rightarrow \quad \begin{cases} \mathrm{Re}(\Gamma) = \frac{1}{2}\left(\Gamma + \Gamma^*\right) \\ \mathrm{Im}(\Gamma) = \frac{1}{2j}\left(\Gamma - \Gamma^*\right) \end{cases} \tag{4.17}$$

So Q in terms of Γ is

$$Q = \frac{|\mathrm{Im}(Z)|}{\mathrm{Re}(Z)} = \frac{\left|\frac{1}{2j}\left(Z - Z^*\right)\right|}{\frac{1}{2}\left(Z + Z^*\right)} = \frac{|Z - Z^*|}{Z + Z^*} = \frac{\left|Z_0 \frac{1+\Gamma}{1-\Gamma} - \left(Z_0 \frac{1+\Gamma}{1-\Gamma}\right)^*\right|}{Z_0 \frac{1+\Gamma}{1-\Gamma} + \left(Z_0 \frac{1+\Gamma}{1-\Gamma}\right)^*} \tag{4.18}$$

$$Q = \frac{\left|\frac{1+\Gamma}{1-\Gamma} - \frac{1+\Gamma^*}{1-\Gamma^*}\right|}{\frac{1+\Gamma}{1-\Gamma} + \frac{1+\Gamma^*}{1-\Gamma^*}} = \frac{\left|\frac{2\left(\Gamma - \Gamma^*\right)}{(1-\Gamma)(1-\Gamma^*)}\right|}{\frac{2\left(1 - \Gamma\Gamma^*\right)}{(1-\Gamma)(1-\Gamma^*)}} = \frac{|\Gamma - \Gamma^*|}{1 - \Gamma\Gamma^*} = \frac{|2j\,\mathrm{Im}(\Gamma)|}{1 - |\Gamma|^2} \tag{4.19}$$

$$Q = \frac{|\mathrm{Im}(Z)|}{\mathrm{Re}(Z)} = \frac{2|\mathrm{Im}(\Gamma)|}{1 - |\Gamma|^2} \tag{4.20}$$

Simulation results for the two CMOS inductors are very close to each other. So only one of them that represents both is shown in this work. Figures 4.19-4.21 show reactance, resistance and quality factor of CMOS spiral inductor, respectively.

Figures 4.22-4.24 show reactance, resistance and quality factor of MUMPS spiral inductors, respectively.

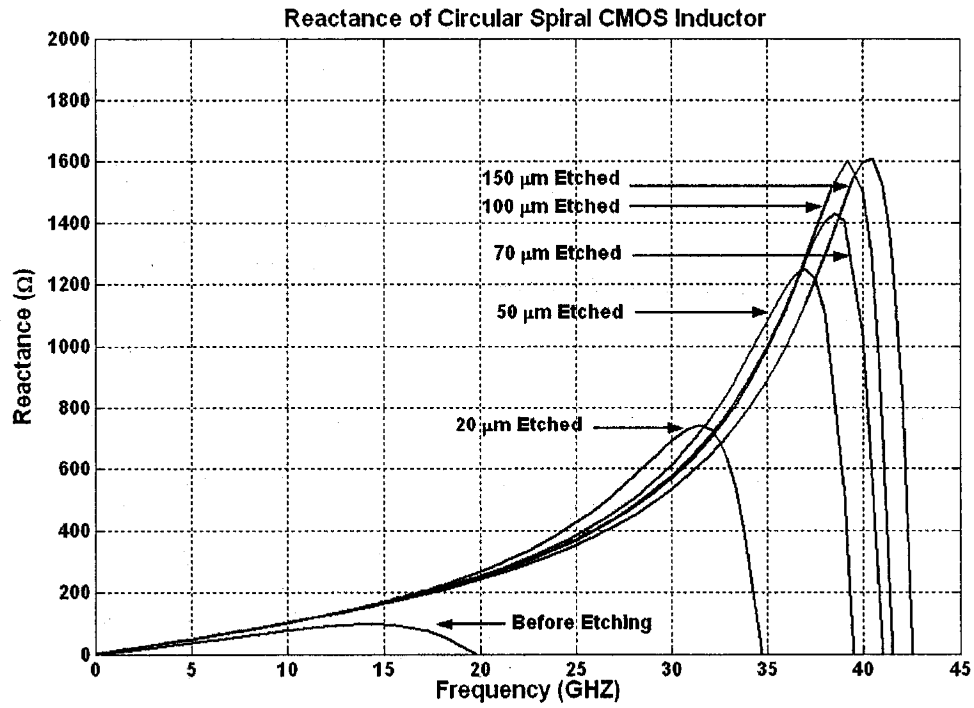

Figure 4.19 Reactance of CMOS Spiral Inductor for Different Etch Depths Beneath the Inductor

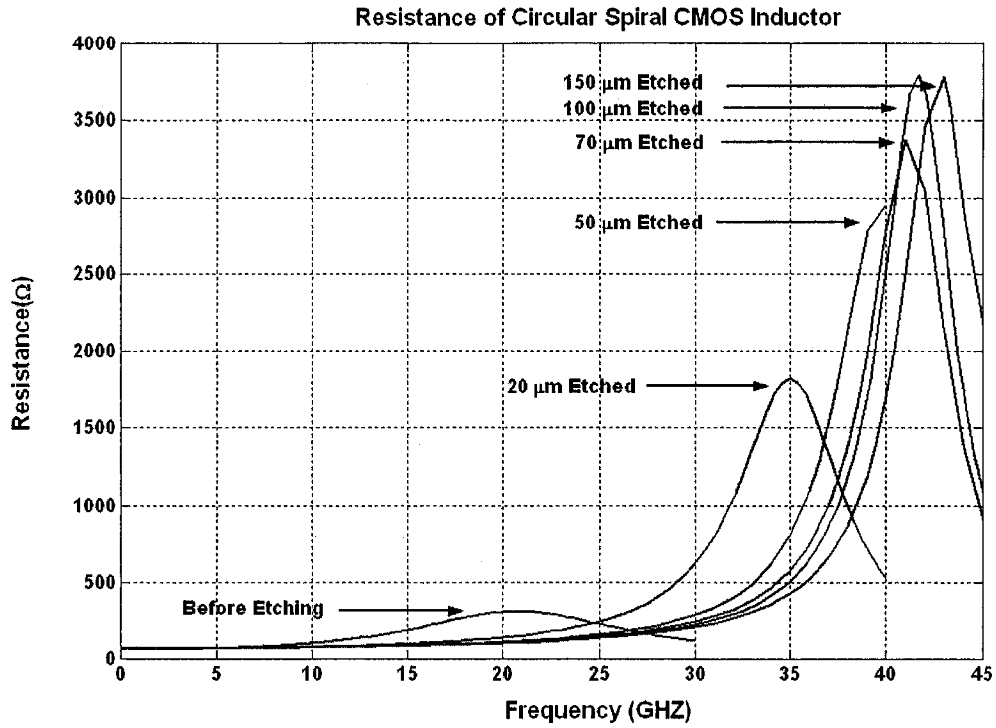

Figure 4.20 Resistance of CMOS Spiral Inductor for Different Etch Depths Beneath the Inductor

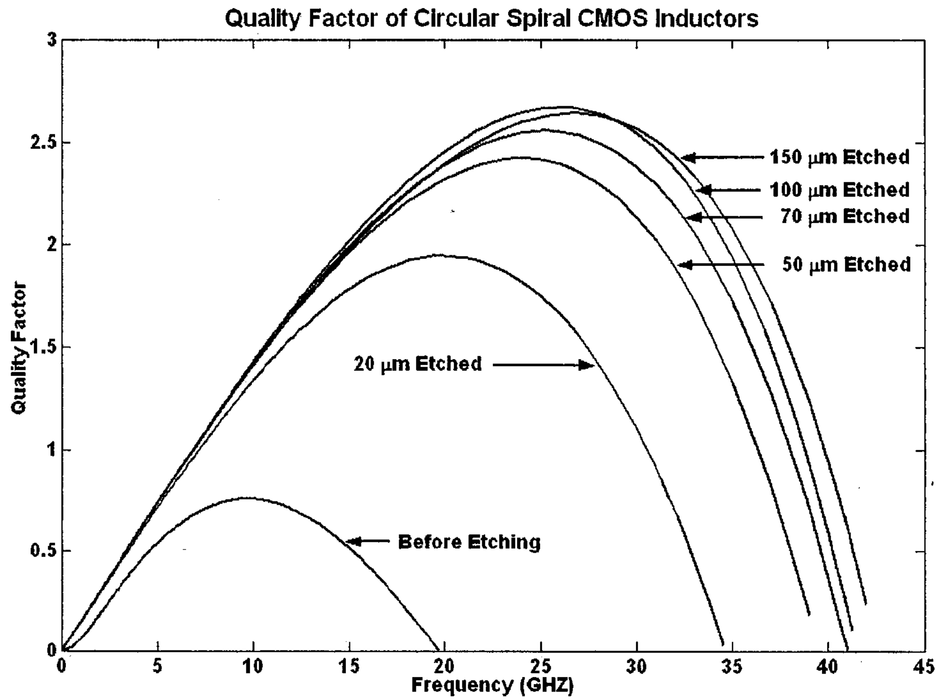

Figure 4.21 Quality Factor of CMOS Spiral Inductor for Different Etch Depths Beneath the Inductor

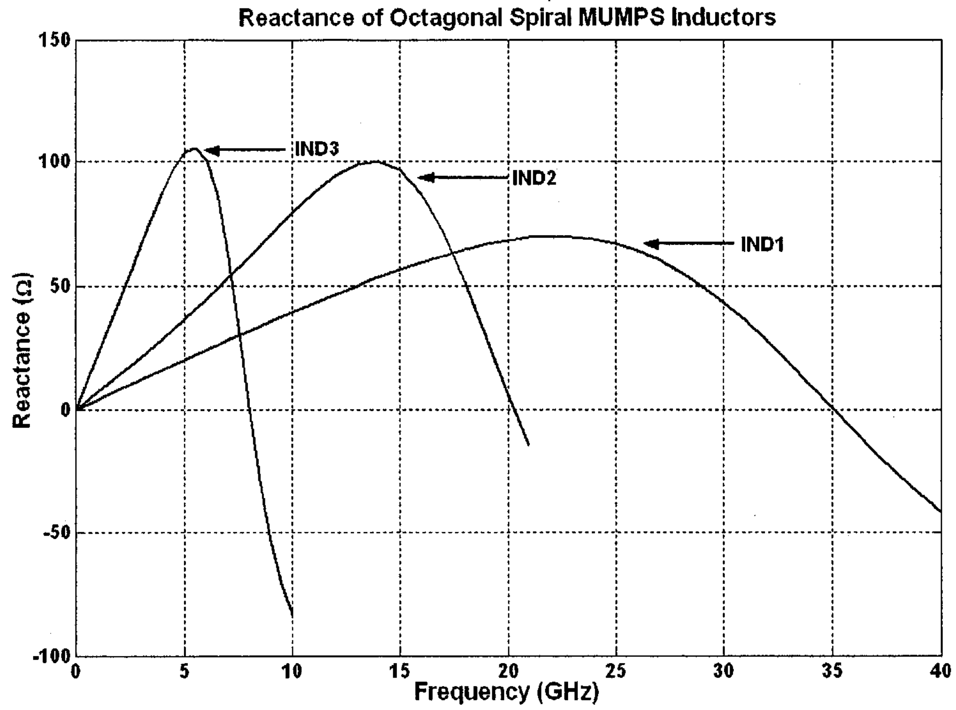

Figure 4.22 Reactance of MUMPS Spiral Inductors (See Table 4.4 for Inductor Specifications)

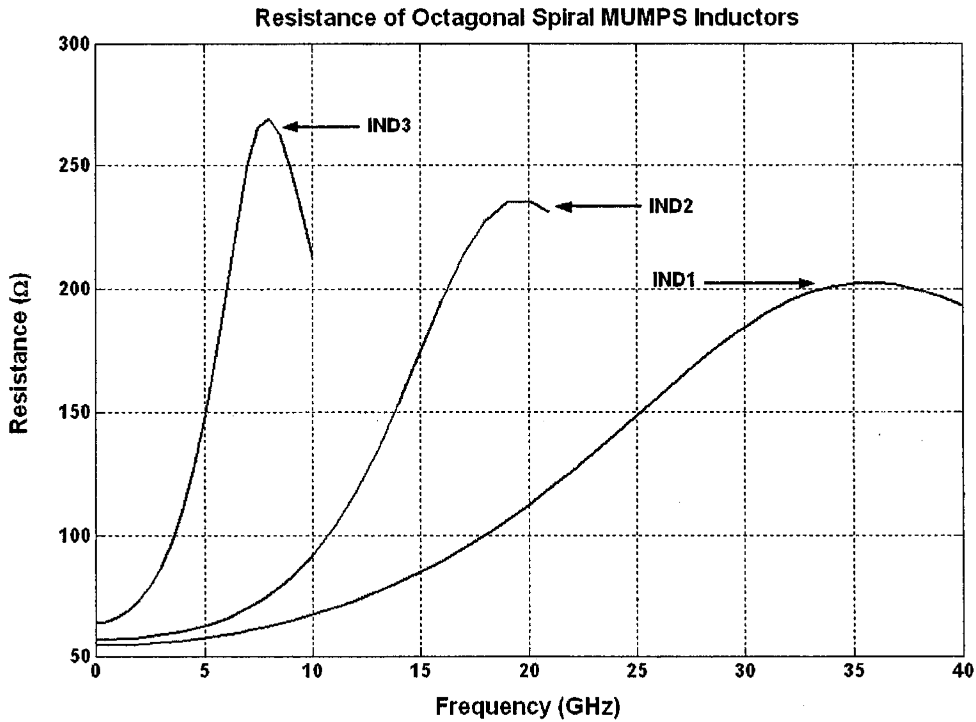

Figure 4.23 Resistance of MUMPS Spiral Inductors (See Table 4.4 for Inductor Specifications)

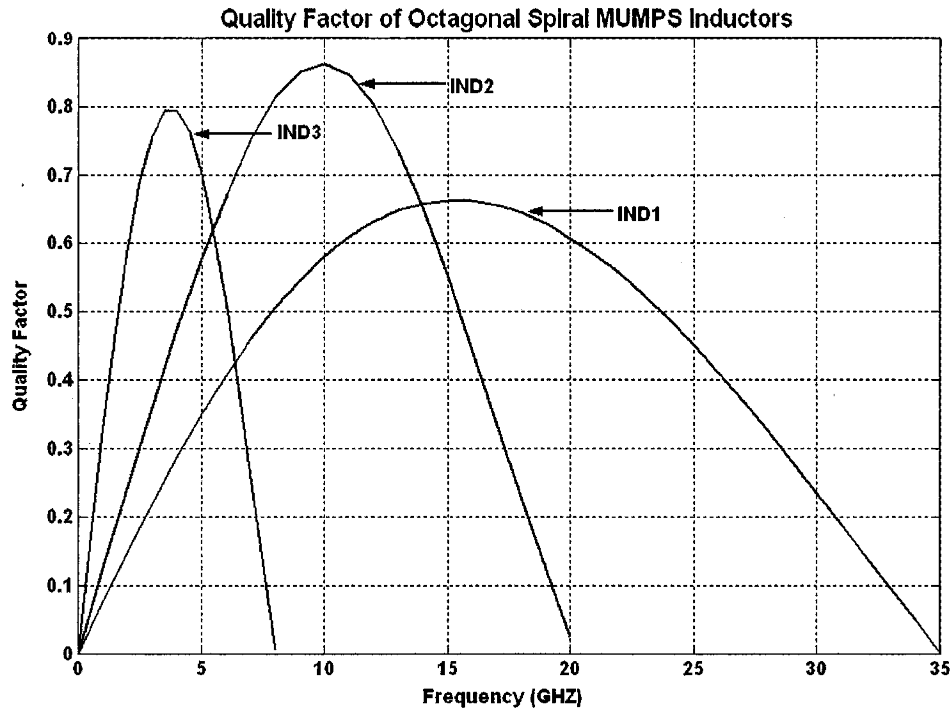

Figure 4.24 Quality Factor of MUMPS Spiral Inductors (See Table 4.4 for Inductor Specifications)

4.9 Etch Simulation

The proposed etching process can be simulated with available softwares to get an idea of the shape of the etched structure according to the designed mask (or etch windows) and substrate orientation.

Anisotropic Crystalline Etching Simulation (ACES) [127] is a Siliocn etching simulation software. This software allows you to import your mask and observe the time progress of etching and the final structure after etching. The mask defines the areas that silicon is exposed to the etchant. It is possible to observe the effect of combining of isotropic wet etching, anisotropic wet etching and reactive ion etching (RIE) (which is an anisotropic

etching method) methods and design an optimum etching profile considering time, consumption of chemicals and gases and environmental considerations, costs, etc

A few cases are examined and the results of successful cases are given. In all cases it is assumed that a (100) silicon wafer is used. Used masks are defined in Table 4.6. The reference for rotations is the <110>.

Mask Name	Properties	Size ($\mu m \times \mu m$)
Etch Mask 2	The mask designed for fabricated chips	240×240
Etch Mask4	Etch Mask 2 rotated by 45°	350×350
Etch Mask5	Etch Mask6 rotated by 45°	350×350
Etch Mask6	An open square window separated into two parts	240×240
Etch Mask7	An open square window	240×240
Etch Mask8	Etch Mask7 rotated by 45°	350×350

Table 4.6 Etch Masks

In Etch Mask 2 four open windows (etch holes) are provided for substrate etching. The inductor rests in the central area surrounded by four open windows. The goal of etching is to remove the substrate under the inductor. Etch Mask 4 is simply a rotated version of Etch Mask 2 by 45° to observe the effect of orientation in etching.

In Etch Mask 6 2 two open windows (etch openings) dividing the etch window into two parts are provided for substrate etching. The inductor rests in the central area between the two open areas. Etch Mask 5 is the rotated version of Etch Mask 6 by 45° to observe the effect of orientation in etching.

Etch Mask 7 is an open window to observe the progress of etching. Etch Mask 8 is the rotated version of Etch Mask 7 by 45°.

Masks are designed in Cadence Virtuoso and are exported to ACES as GDS II format. All the above mentioned masks are negative.

4.9.1 Anisotropic Wet Etching Using Etch Mask 2

Figure 4.25 shows the progress of etching. Pictures show the structure before etching, after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes and after 220 minutes of etching, respectively.

Maximum depth is achieved in the lower right window which is 66 μm after 220 minutes of etching. Etching ends when the (111) planes meet each other. With this mask and anisotropic wet etching method it is not possible to remove all the substrate under the inductor unless it is combined with another etching method that can change the conditions of (111) planes in order to allow the etching continue.

4.9.2 Isotropic Wet Etching Using Etch Mask 2

Figure 4.26 shows the progress of etching. Pictures show the structure before etching, after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes and after 220 minutes of etching, respectively.

The depth that is achieved after 220 minutes is 68 μm. With this mask and isotropic wet etching method it is possible to remove all the substrate under the inductor, but the lateral etching can damage neighboring devices and, so this method is not recommended.

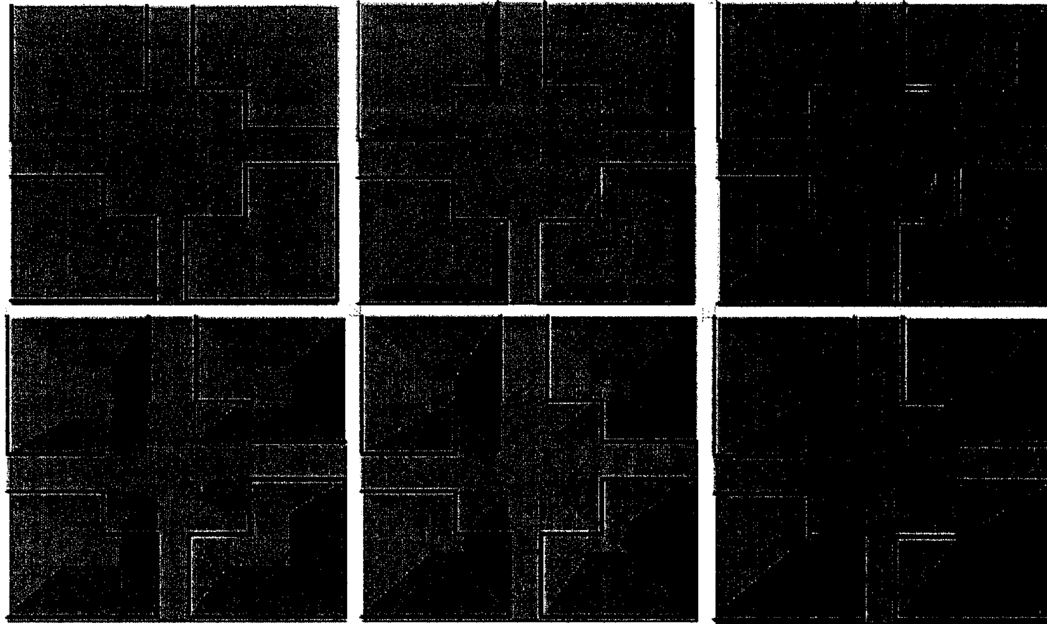

Figure 4.25 Anisotropic Wet Etching using Etch Mask 2

4.9.3 RIE Using Etch Mask 2

Figure 4.27 shows the progress of etching. Pictures show the structure before etching, after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes and after 200 minutes of etching, respectively.

The depth that is achieved after 200 minutes is 62 μm. With this mask and RIE method it is not possible to remove all the substrate under the inductor, but combining this method with another etching method can do the job.

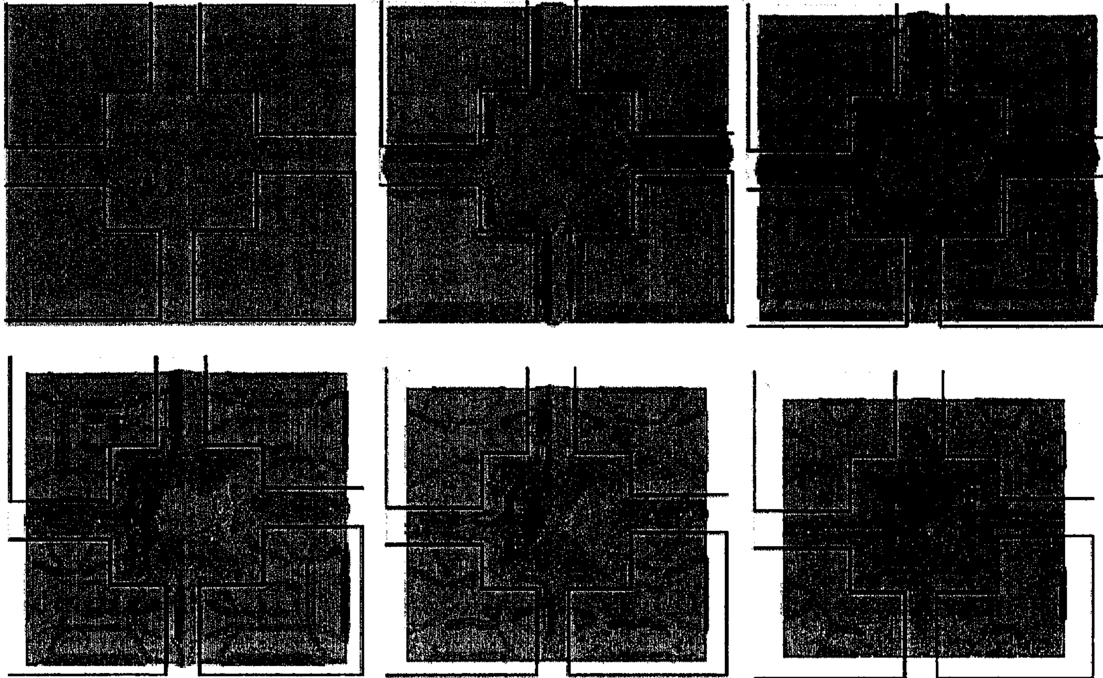

Figure 4.26 Isotropic Wet Etching Using Etch Mask 2

4.9.4 Anisotropic Wet Etching Followed by RIE

It is obvious that this combination doesn't remove the substrate under the inductor. So no simulation result is given.

4.9.5 RIE Followed by Anisotropic Wet Etching Using Etch Mask 2

Initially RIE is performed for 140 minutes resulting in depth of 42 μm. Then anisotropic wet etching is performed. Figure 4.28 shows the structure after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes, after 200 minutes, after 240 minutes, and after 280 minutes of anisotropic wet etching, respectively. Figure 4.29 shows the final structure after an additional 20 minutes of anisotropic wet etching.

The depth that is achieved after 140 minutes of RIE followed by 300 minutes of anisotropic wet etching is 149 μm. All of the substrate beneath the inductor is removed as desired.

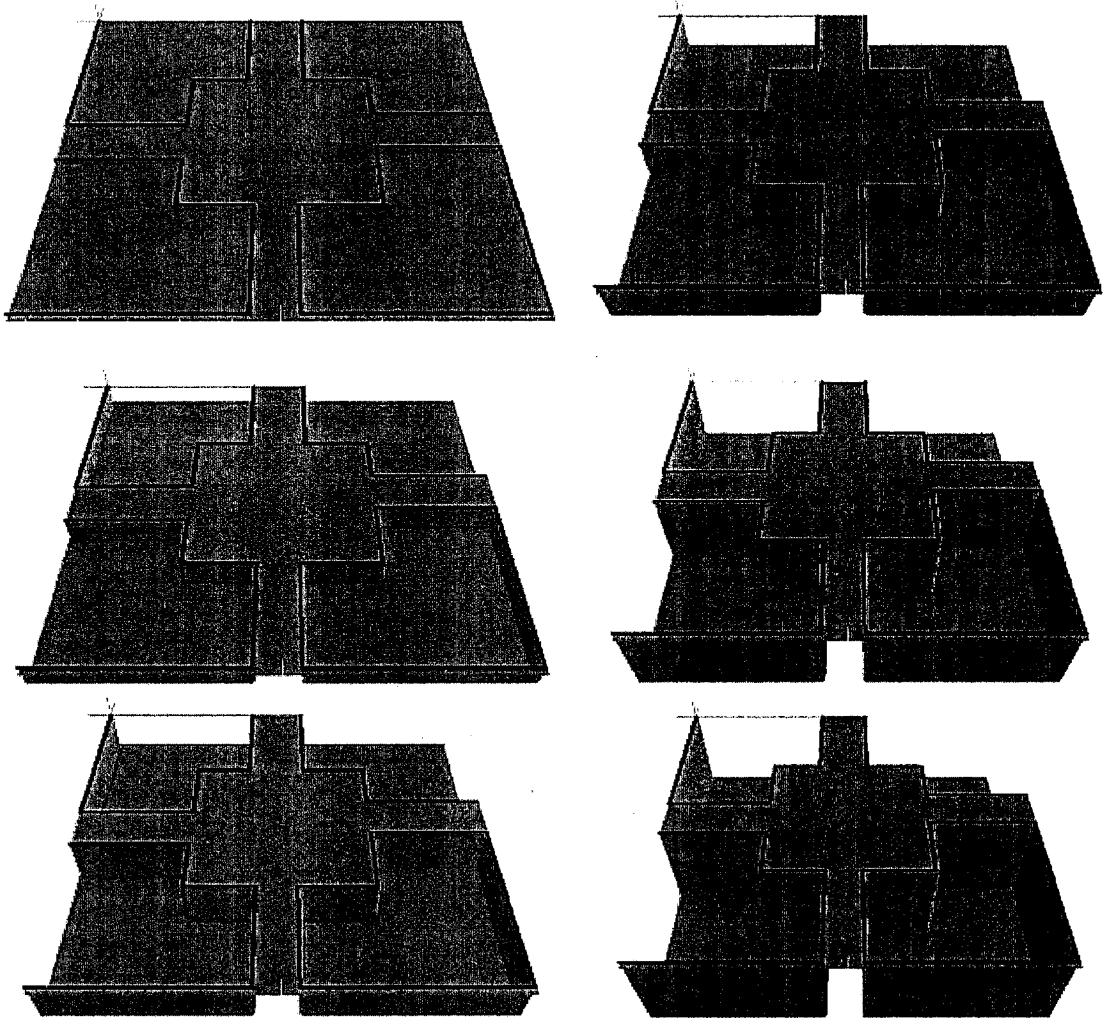

Figure 4.27 RIE Using Etch Mask 2

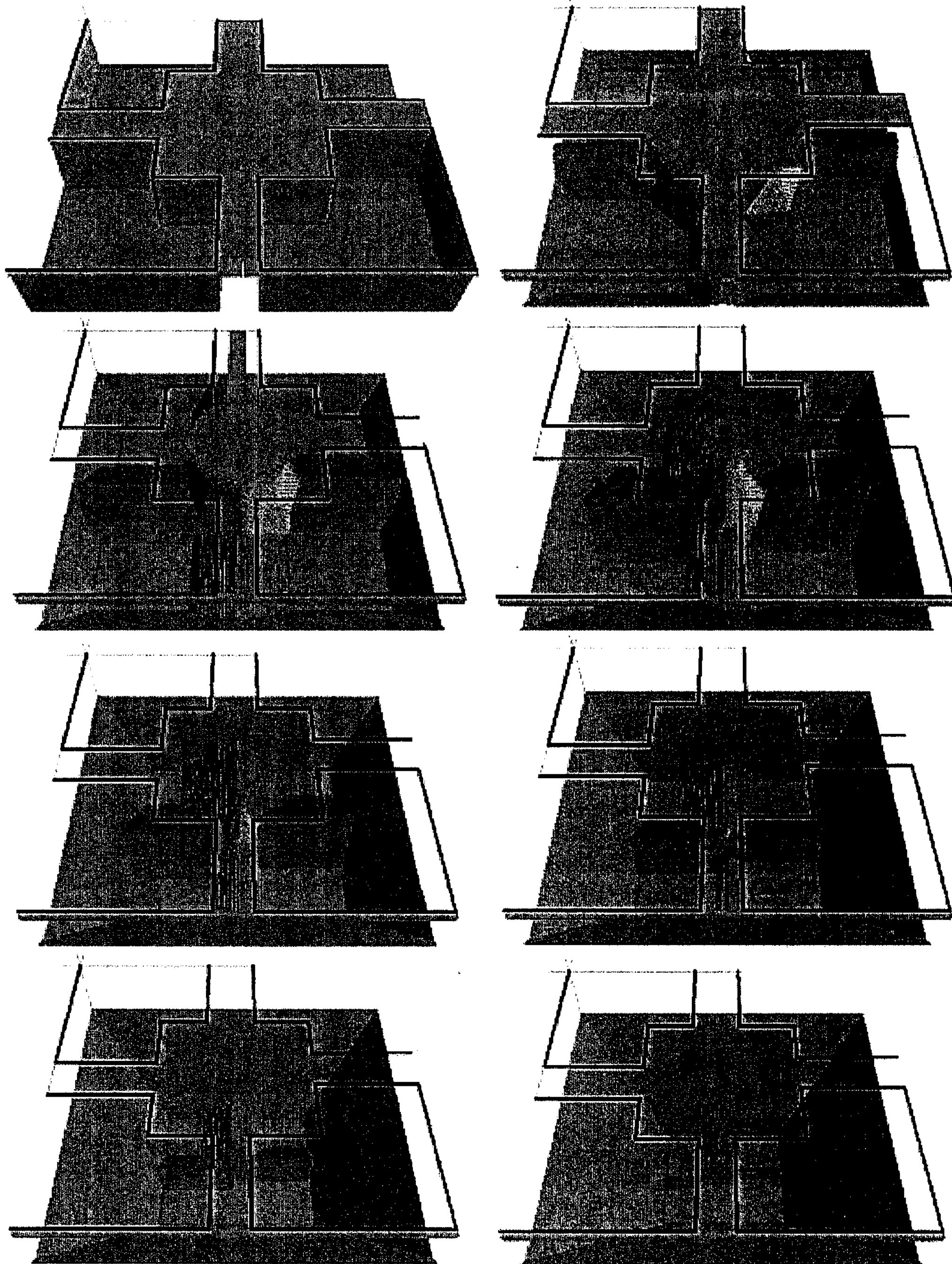

Figure 4.28 RIE Followed by Anisotropic Wet Etching Using Etch Mask 2

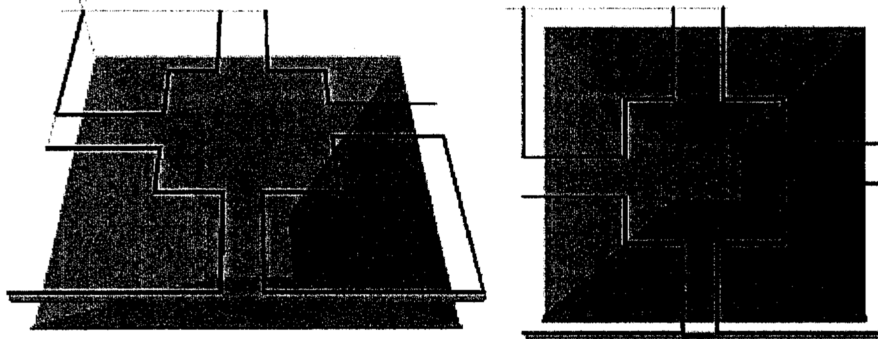

Figure 4.29 Final Structure Resulting from RIE by Anisotropic Wet Etching Using Etch Mask 2

4.9.6 Isotropic Wet Etching Followed by Anisotropic Wet Etching Using Etch Mask 2

Initially isotropic wet etching is performed for 35 minutes resulting in depth of 11 μm. Then anisotropic wet etching is performed. Figure 4.30 shows the structure after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes, after 200 minutes, after 240 minutes, after 280 minutes, after 320 minutes, after 360 minutes, after 480, and after 520 minutes of anisotropic wet etching, respectively.

The depth that is achieved after 35 minutes of isotropic wet etching followed by 520 minutes of anisotropic wet etching is 158 μm. All of the substrate beneath the inductor is removed as desired. The time required time is a little more then the combination of RIE and anisotropic wet etching

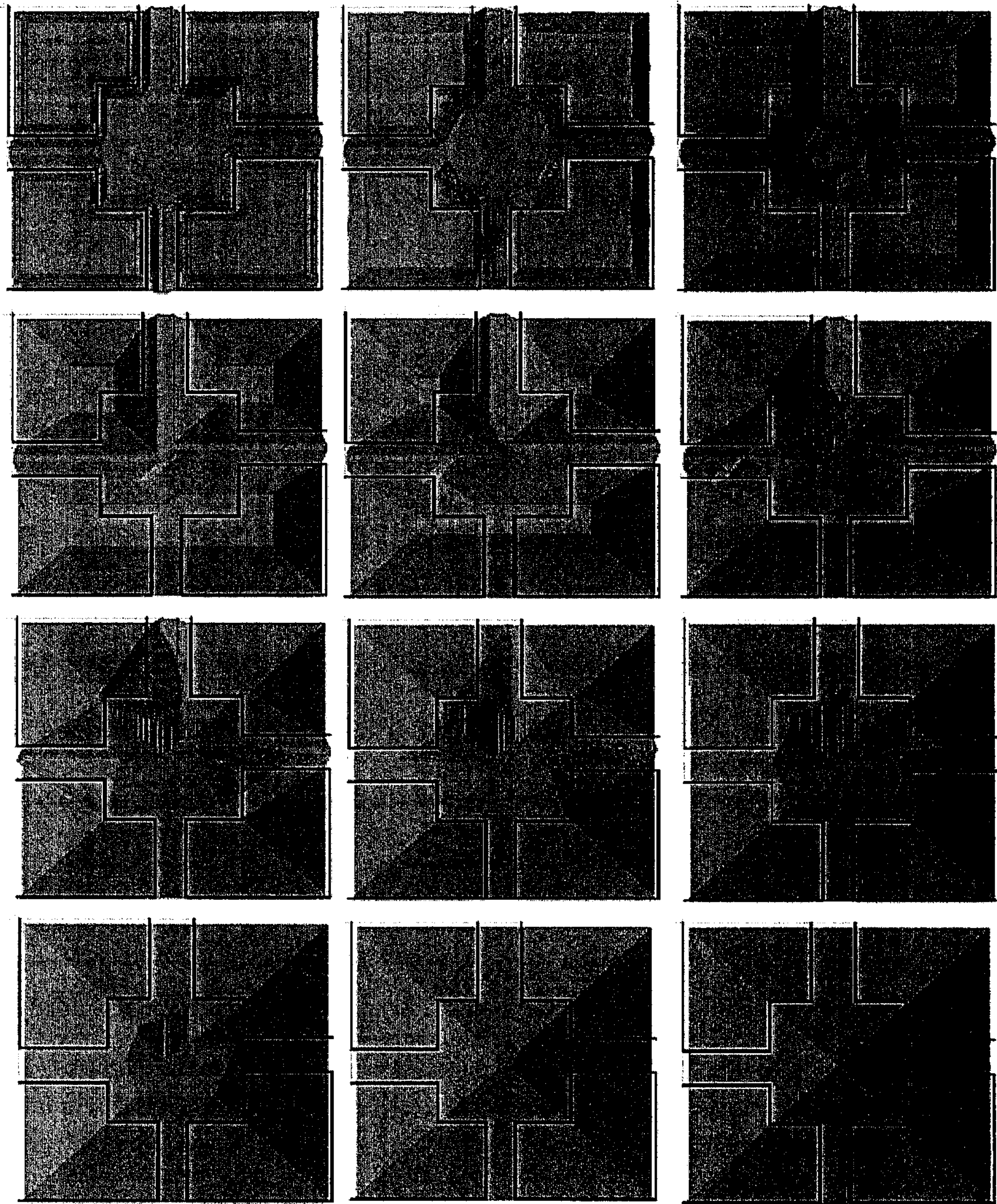

Figure 4.30 Isotropic Wet Etching Followed by Anisotropic Wet Etching Using Etch Mask 2

4.9.7 Anisotropic Wet Etching Using Etch Mask 4

Figure 4.31 shows the progress of etching. Pictures show the structure before etching, after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes, after 200 minutes, after 240 minutes, after 280 minutes, after 320 minutes, after 360 minutes and after 360 minutes of etching, respectively.

The depth that is achieved after 200 minutes is 85 μm. All of the substrate beneath the inductor is removed as desired without being involved in complications of combining two methods.

4.9.8 Anisotropic Wet Etching Using Etch Mask 6

Figure 4.32 shows the progress of etching. Pictures show the structure before etching, after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes, after 200 minutes, after 240 minutes and after 280 minutes of etching, respectively.

The resulting depth after 280 minutes is 66 μm. With this mask and anisotropic wet etching method it is not possible to remove all the substrate under the inductor unless it is combined with another etching method that can change the conditions of (111) planes in order to allow the etching continue.

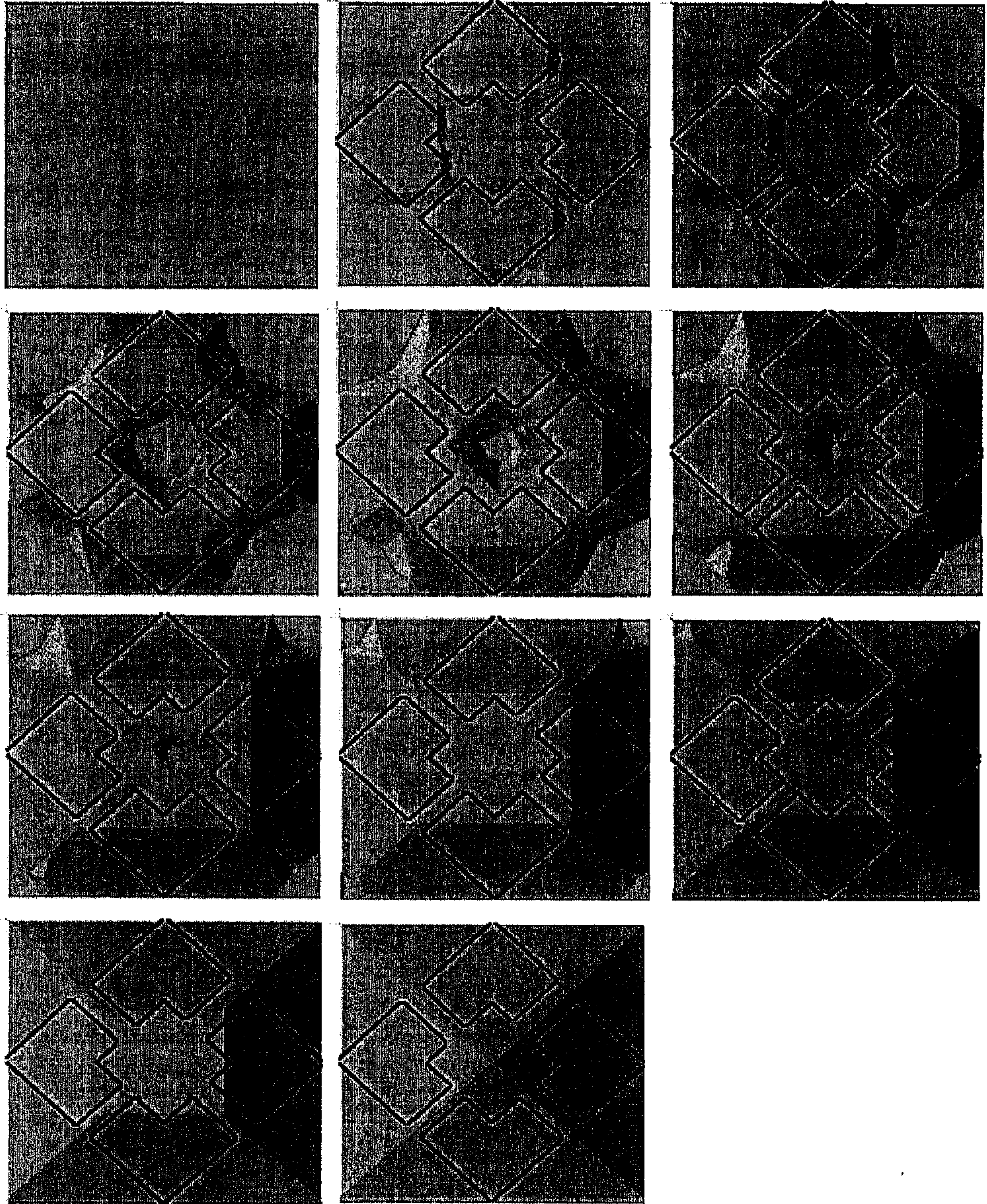

Figure 4.31 Anisotropic Wet Etching Using Etch Mask 4

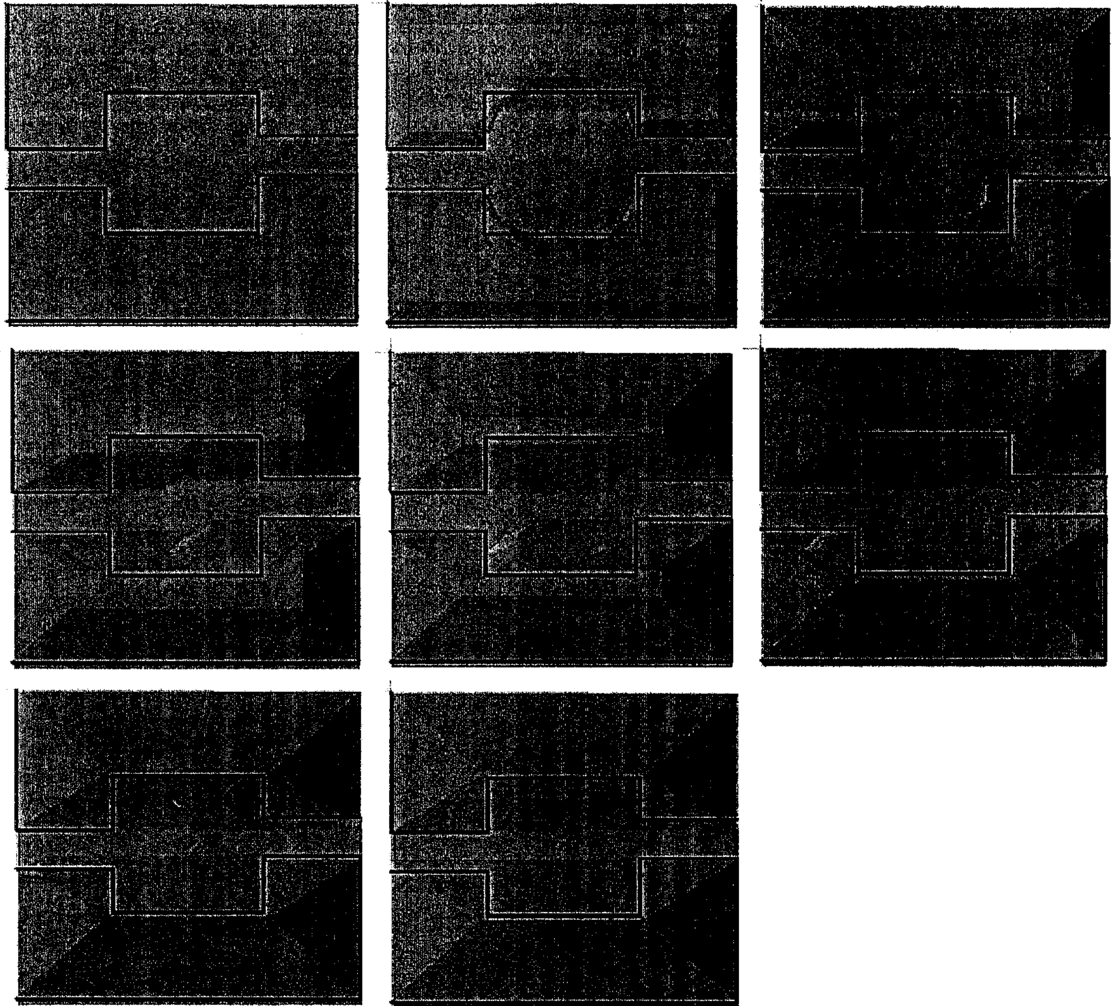

Figure 4.32 Anisotropic Wet Etching Using Etch Mask 6

4.9.9 Anisotropic Wet Etching Using Etch Mask 5

Figure 4.33 shows the progress of etching. Pictures show the structure before etching, after 40 minutes, after 80 minutes, after 120 minutes, after 160 minutes, after 200 minutes, after 240 minutes, after 280 minutes, after 360 minutes and after 710 minutes of etching, respectively.

The resulting depth after 280 minutes is 76 μm and after 710 minutes is 147 μm.

All of the substrate beneath the inductor is removed as desired without being involved in complications of combining two methods.

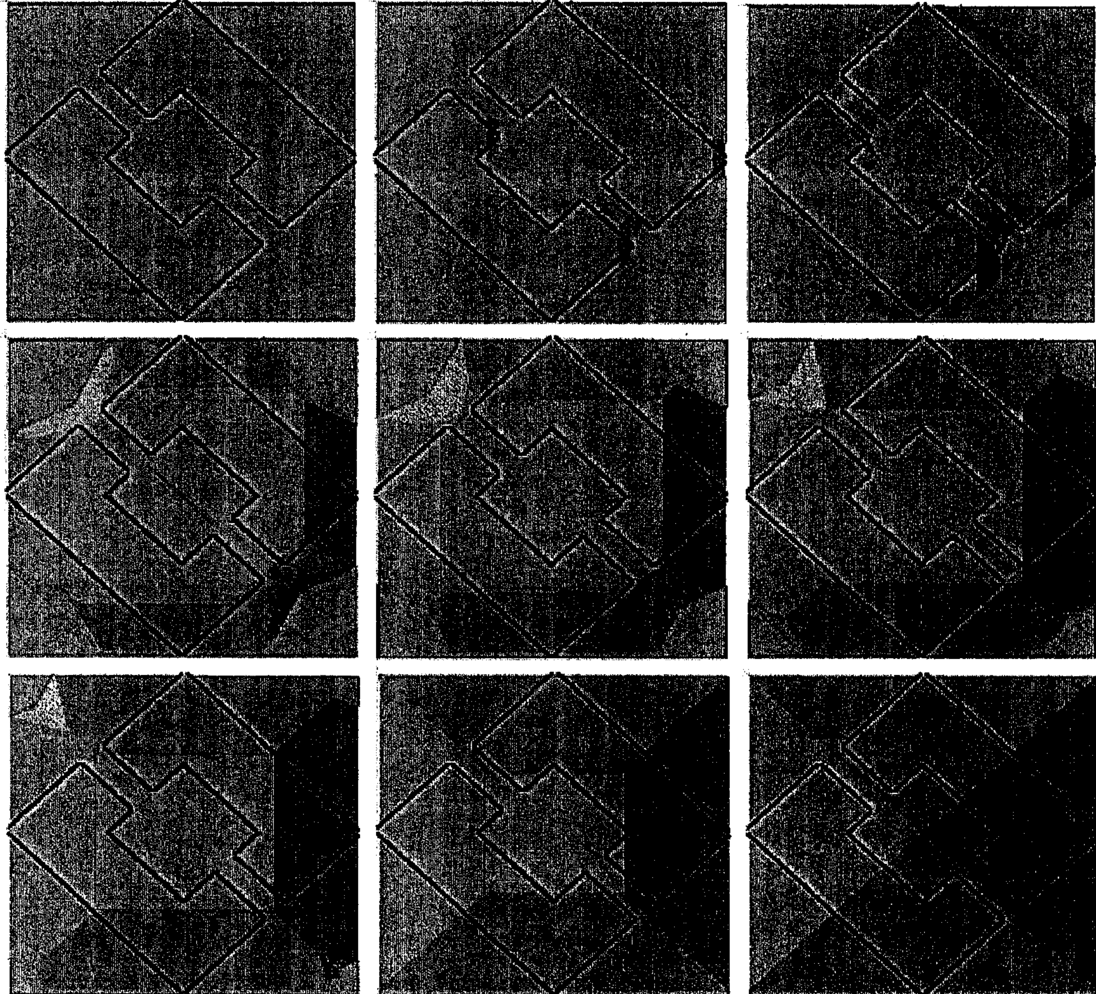

Figure 4.33 Anisotropic Wet Etching Using Etch Mask 5

4.9.10 Anisotropic Wet Etching Using Etch Mask 7

Having one open window in the chip allows us to observe the progress of etching. Figure 4.34 shows the structure before and after the etching for 480 minutes, respectively. The resulting depth after 480 minutes is 146 μm.

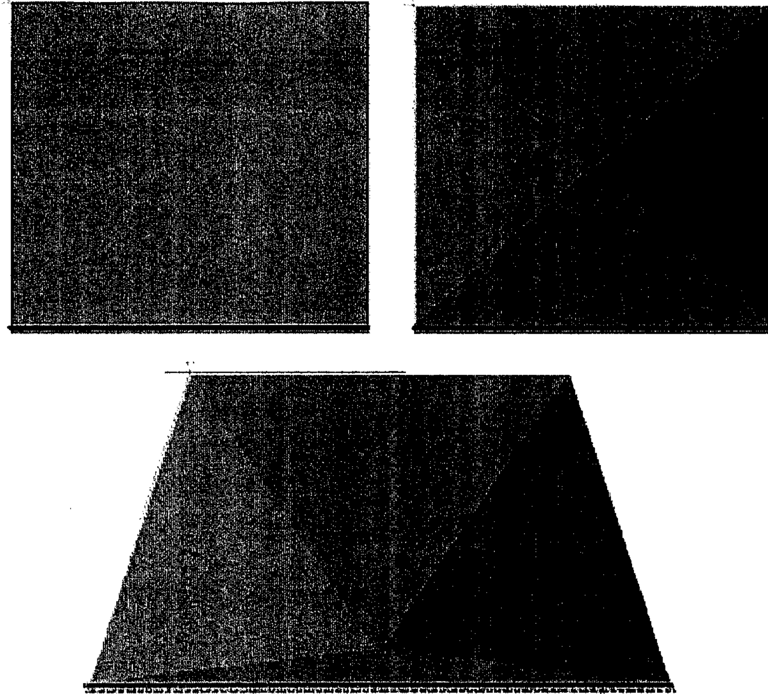

Figure 4.34 Anisotropic Wet Etching Using Etch Mask 7

4.9.11 Anisotropic Wet Etching Using Etch Mask 8

Figure 4.35 shows the progress of etching. Pictures show the structure after 80 minutes, after 80 minutes, after 160 minutes, after 240 minutes, after 320 minutes, after 400 minutes, after 600 minutes and after 710 minutes of etching, respectively.

The resulting depth after 400 minutes is $85\,\mu m$, after 600 minutes is $128\,\mu m$ and after 710 minutes is $149\,\mu m$.

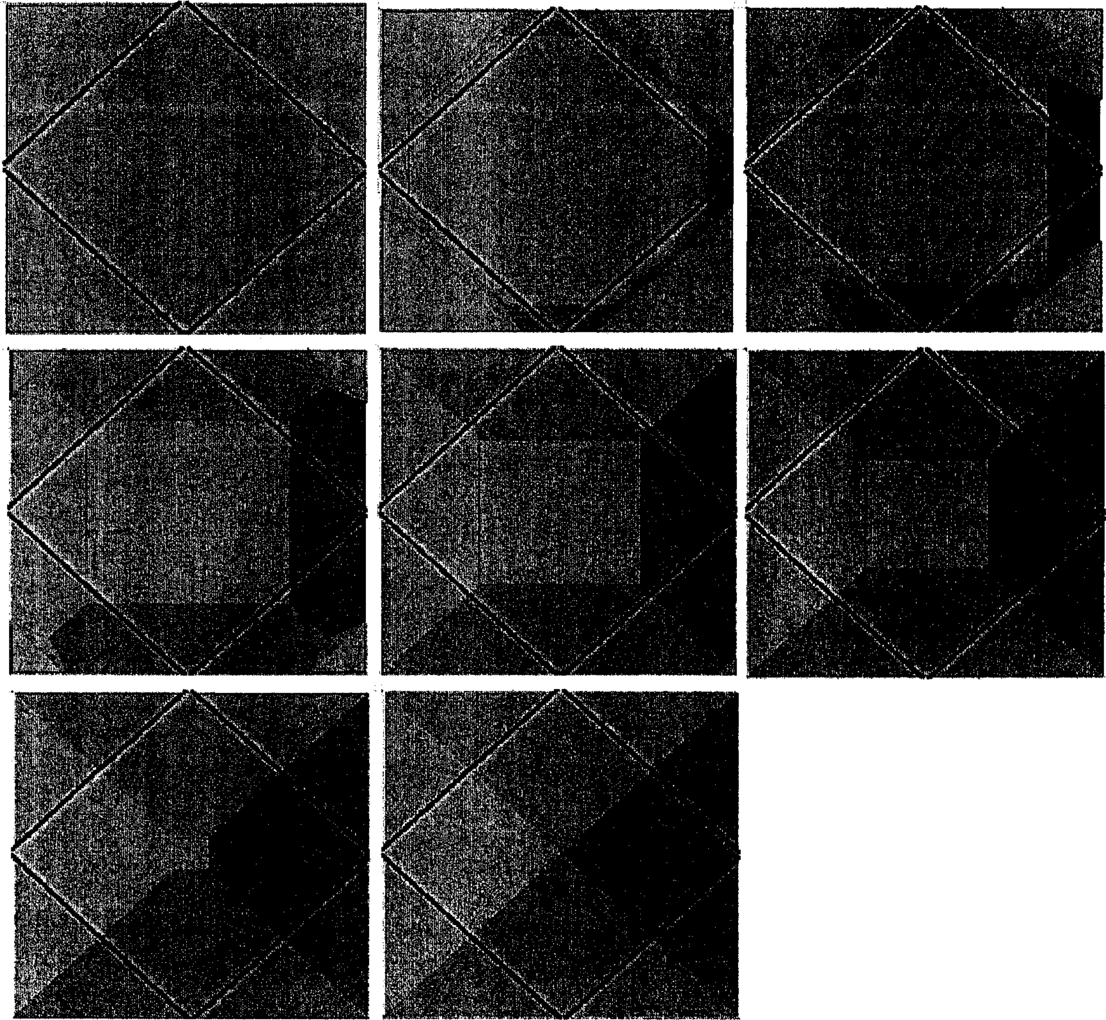

Figure 4.35 Anisotropic Wet Etching Using Etch Mask 8

The results are summarized in Table 4.7

	Etching Method(s)	Mask	Comments
1	Anisotropic Wet Etching	Etch Mask 2	Substrate around the inductor could be remove but not under it
2	Isotropic wet etching	Etch Mask 2	Works but is not recommended due to lateral etching
3	RIE	Etch Mask 2	Substrate around the inductor could be remove but not under it
4	Anisotropic Wet Etching then RIE	Etch Mask 2	doesn't work a
5	RIE then Anisotropic Wet Etching	Etch Mask 2	Works
6	Isotropic then Anisotropic Wet Etching	Etch Mask 2	Works but is slower than the combination of RIE
7	Anisotropic Wet Etching	Etch Mask 4	Works
8	Anisotropic Wet Etching	Etch Mask 6	Substrate around the inductor could be remove but not under it
9	Anisotropic Wet Etching	Etch Mask 5	Works
10	Anisotropic wet etching	Etch Mask 7	
11	Anisotropic wet etching	Etch Mask 8	Although the size of the windows is the same as Mask 7, but the etched area is bigger

Table 4.7 Results of The Etching Simulations

5. Fabrication and Post-Processing

5.1 Fabrication

Access to fabrication technologies is provided through CMC Microsystems.

MUMPS chips are received in released form and do not need any further post-processing.

CMOS chips need post-processing to open bulk-etching windows and then bulk silicon etching is performed.

Figure 5.1 shows photo of fabricated and released MUMPS switches.

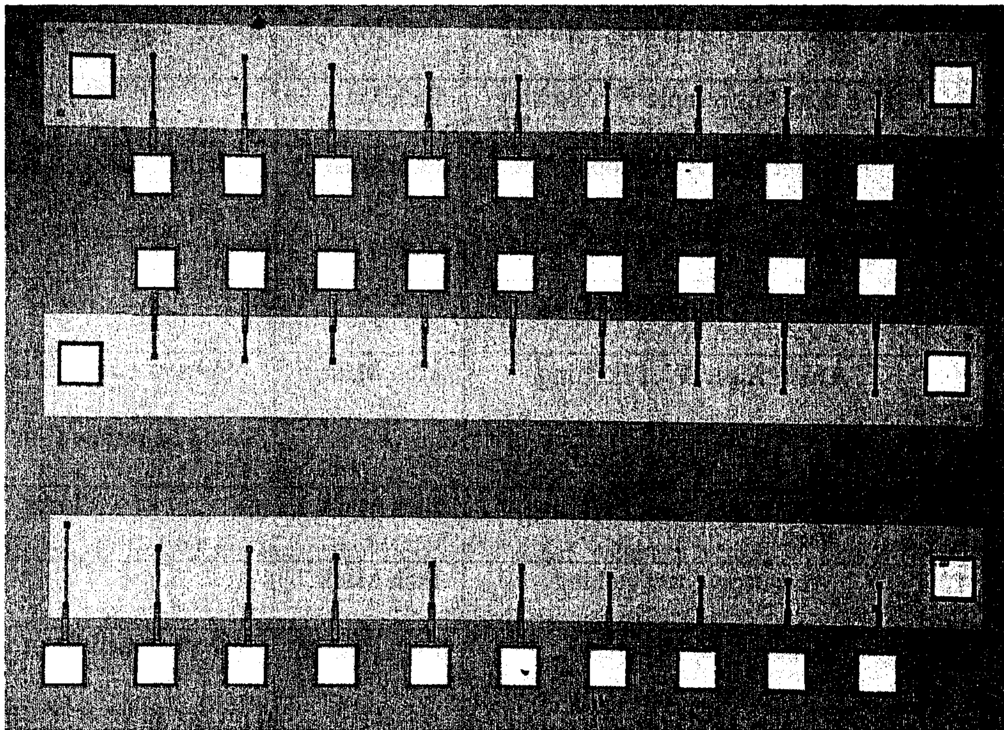

Figure 5.1 Top View of the MUMPS Chip Showing Bonding Pads, Connections and The Switches

Figure 5.2 shows SEM photo of a fixed-fixed beam with etch holes. It shows that the beam is completely released and there isn't any residue of sacrificial material (silicon oxide).

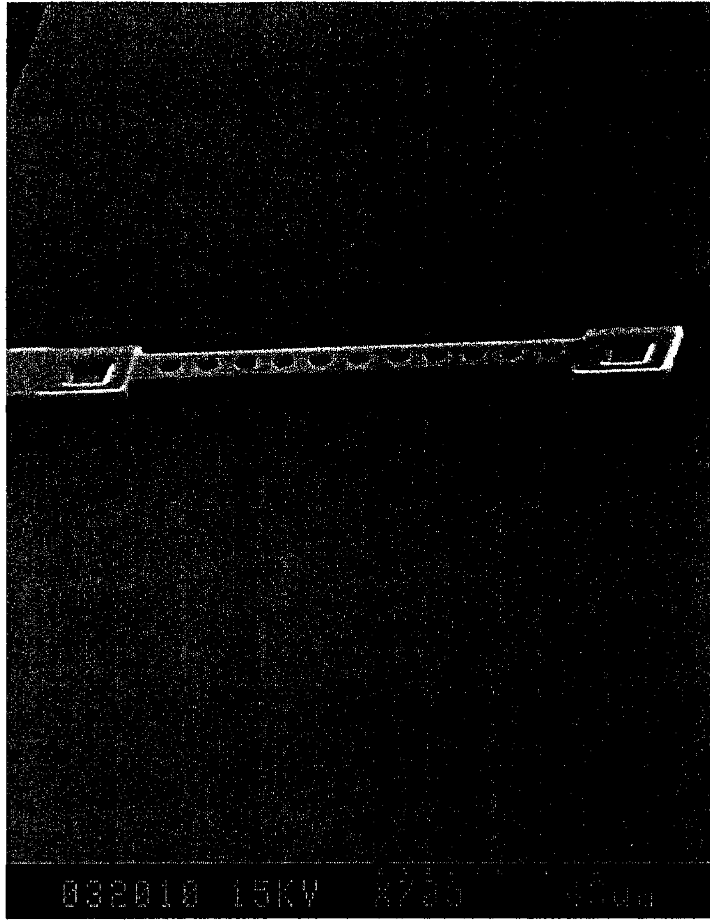

Figure 5.2 SEM Photo of One Beam with Etch Holes

Figure 5.3 shows photos of fabricated and released MUMPS inductors.

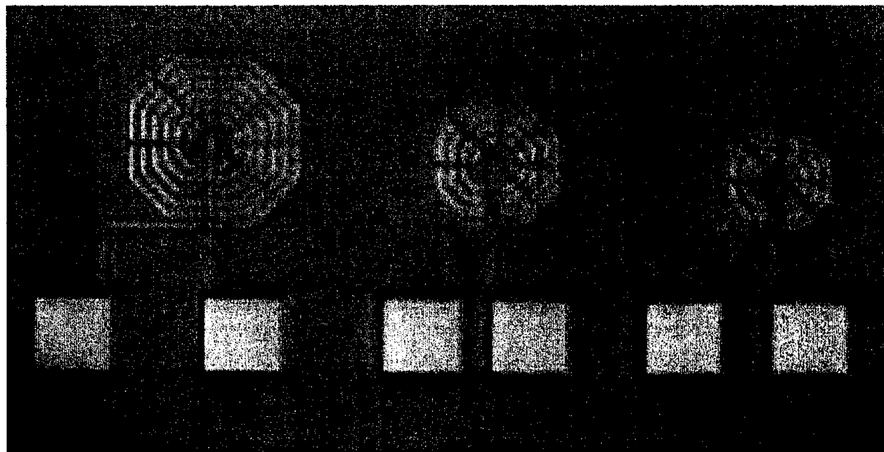

Figure 5.3 Top View of the Three Inductors and Bonding Pads, Fabricated in PolyMUMPS Process

The CMOS chip after fabrication but before post-processing is shown in Figure 5.4. That chips includes different devices from different projects. Figure 5.4 shows the magnified view of the inductors from Figure 5.4.

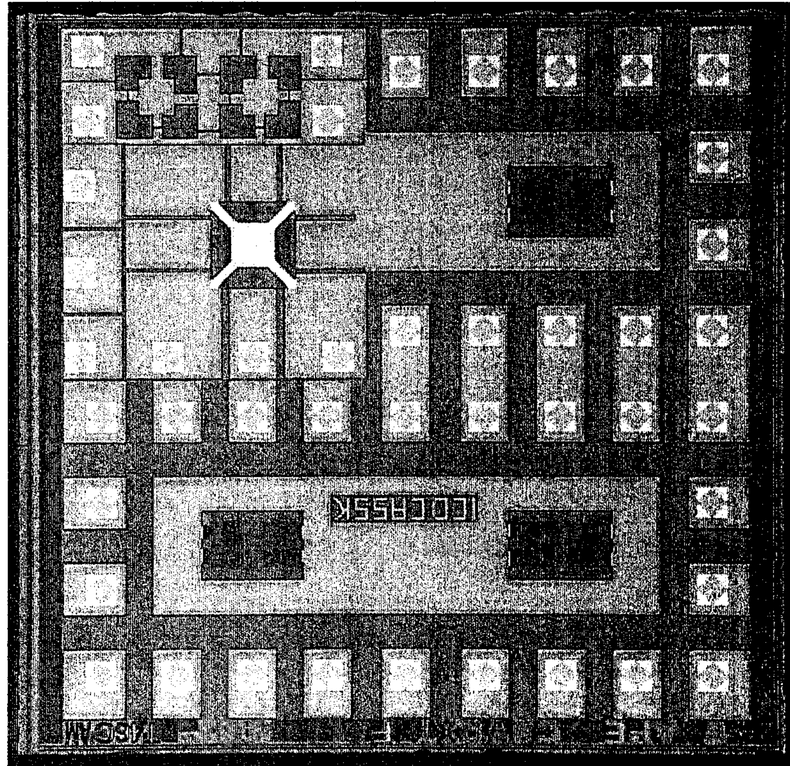

Figure 5.4 CMOS Chip Before Post-Processing (Inductors are at the Upper Left Corner)

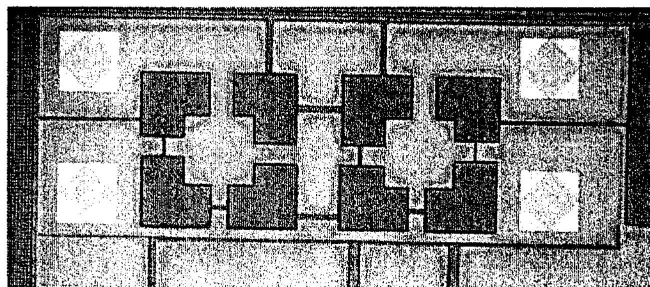

Figure 5.5 CMOS Inductors Before Post-Processing

5.2 Post-Processing

Oxide is removed by two methods: wet etching by buffered HF and glycerine and dry etching by RIE. Wet etching needs a photolithography step, but for RIE, masking is provided by top metal layer.

5.2.1 Wet Oxide Removal by Buffered HF

First photoresist is deposited on the chip by spinning. Then chip is soft-baked in the oven. After that, the mask is aligned with chip patterns and pattern is transferred to photoresist by UV exposure. Then photoresist is developed and hard baked. Now chip is ready for oxide etching. A mixture of HF, DI water, NH_4OH and glycering is used for etching. Glycerine protects exposed aluminum bonding pads from being damaged. In Figure 5.6 CMOS chip with patterned photoresist on it is shown.

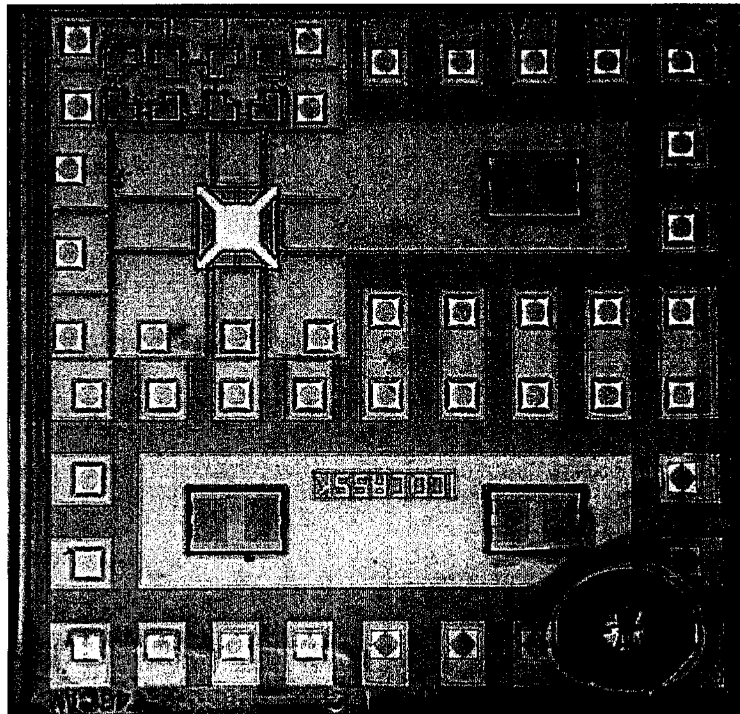

Figure 5.6 CMOS Chip with Patterned Photoresist on It

Figure 5.7 shows the inductors after wet etching by buffered HF.

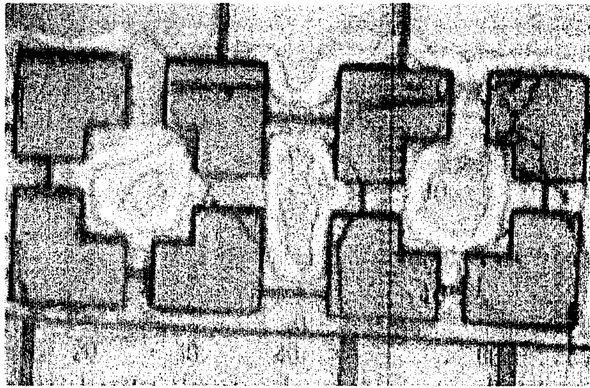

Figure 5.7 CMOS Inductors after Wet Oxide Removal by Buffered HF

Figure 5.8 and 5.9 show SEM photos of one etching window after oxide etching.

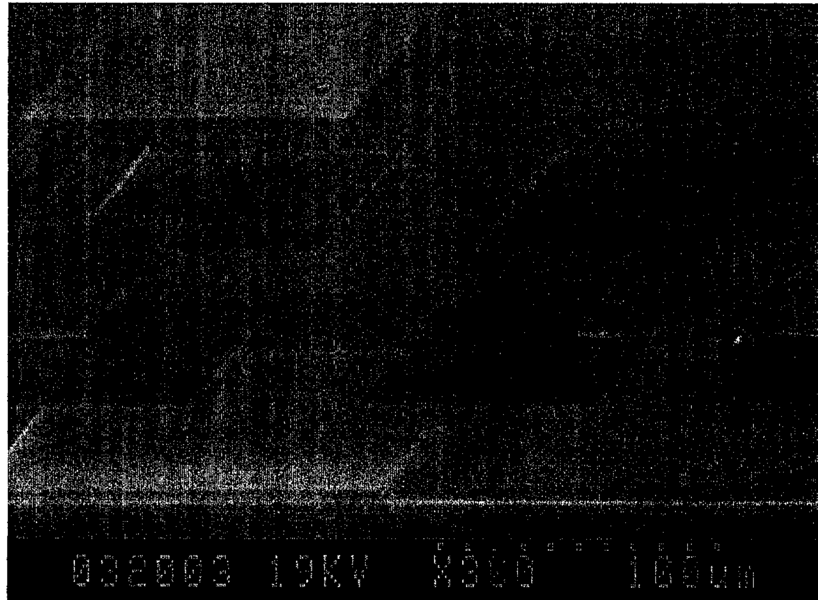

Figure 5.8 SEM Photo of Inductors After Wet Oxide Removal by Buffered HF

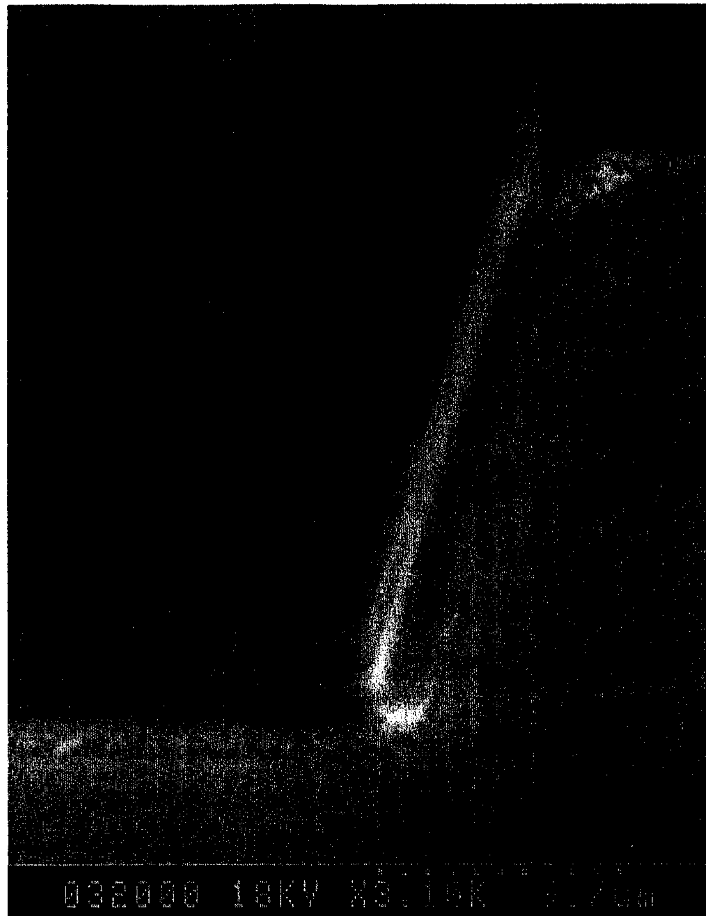

Figure 5.9 One Corner of Etch Window After Wet Oxide Removal by Buffered HF

5.2.2 Dry Oxide Removal by RIE

Figure 5.10 to 5.13 show SEM photos after oxide removal by RIE.

As it can be seen, quality of RIE is better than wet etching.

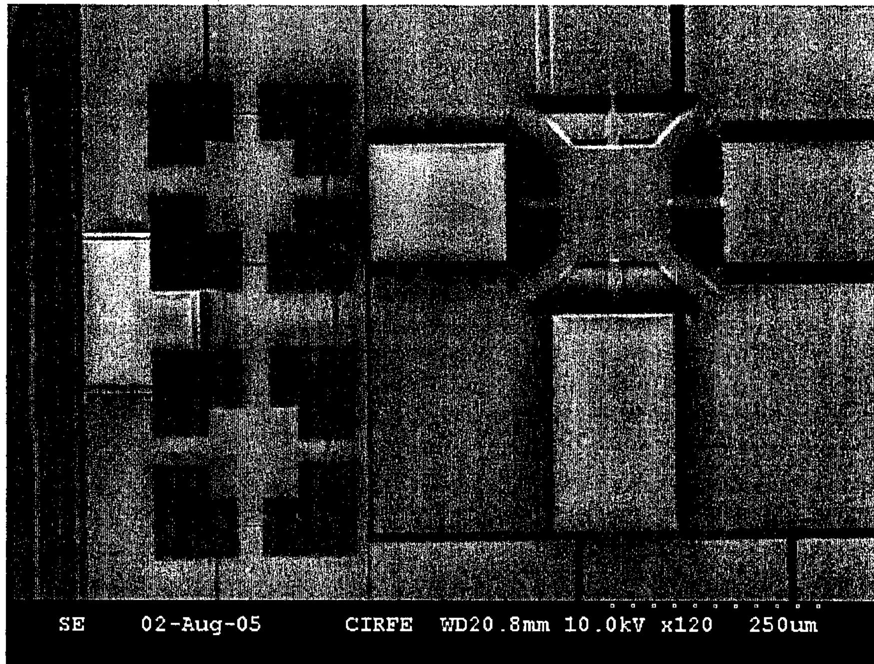

Figure 5.10 SEM Photo of CMOS Inductors After Dry Oxide Removal by RIE

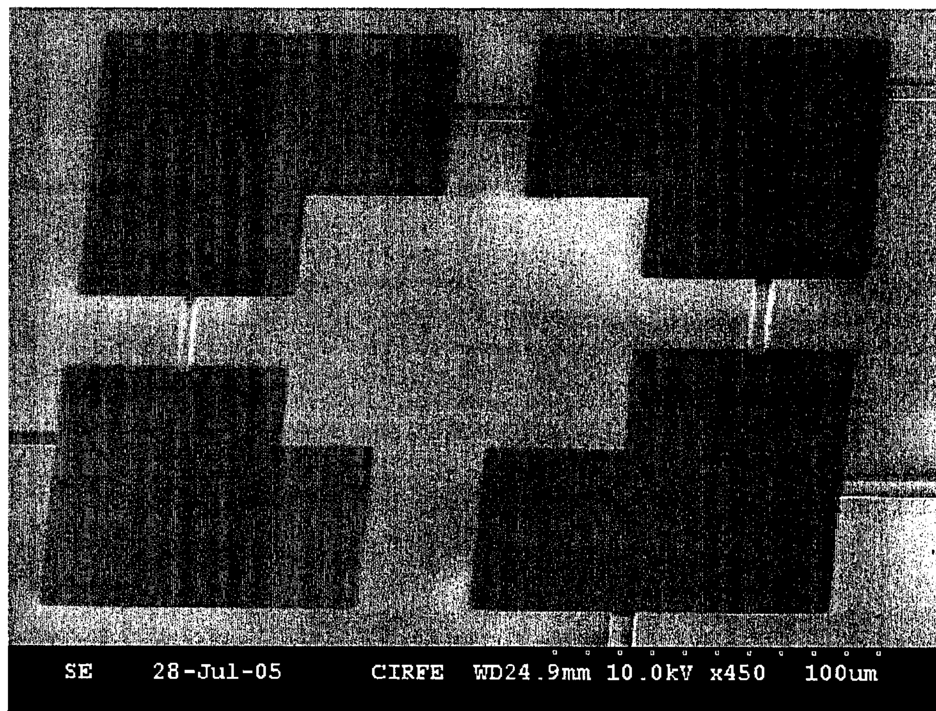

Figure 5.11 SEM Photo of CMOS Inductor After Dry Oxide Removal by RIE

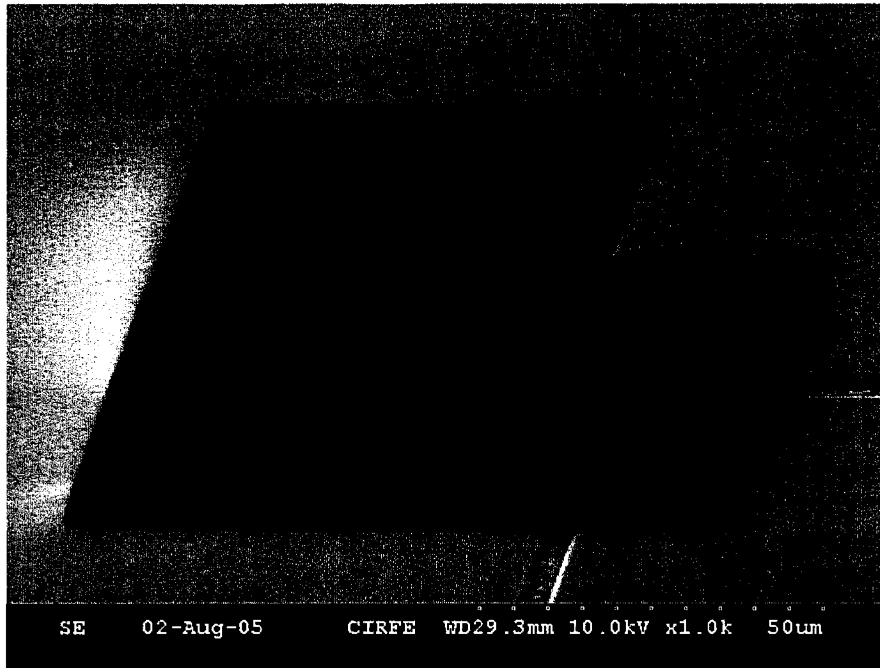

Figure 5.12 SEM Photo of One Etch Window After Dry Oxide Removal by RIE

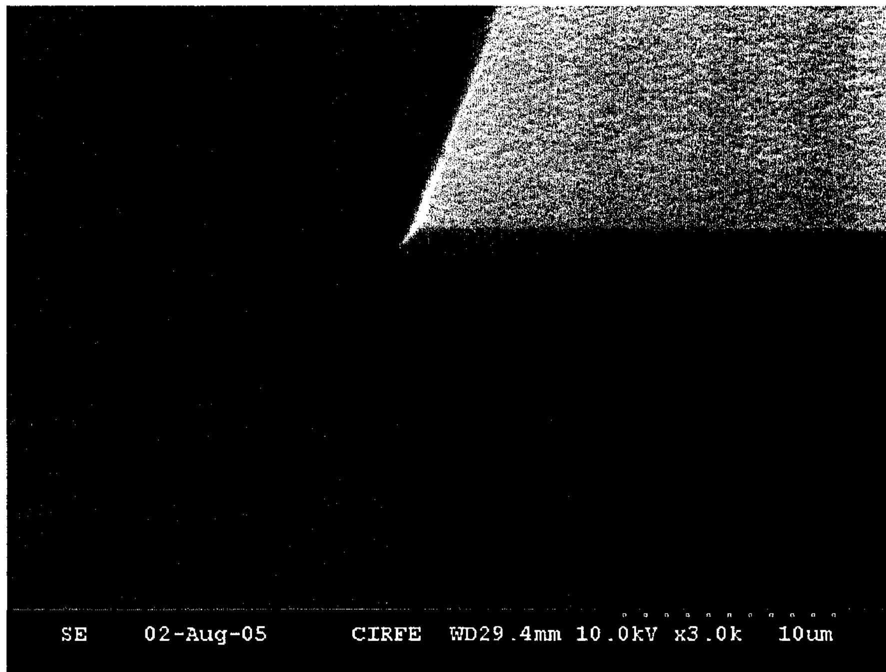

Figure 5.13 SEM Photo of A Corner of Etch Window After Dry Oxide Removal by RIE

5.2.3 Bulk Micromachining

Bulk micromachining is performed right after oxide removal. If chips are left for some time to do silicon etching later, a thin layer of oxide layer will deposited on silicon. This oxide layer that is called native oxide has to be removed before silicon etching. So it is suggested that TMAH etching be done right after oxide removal.

Figure 5.14 shows the chip after TMAH etching. SEM photo of inductors after etching is given in Figure 5.15. Figure 5.16 and 5.17 show SEM photos after TMAH etching (RIE oxide removal)

Figure 5.14 CMOS Chip after TMAH Etching

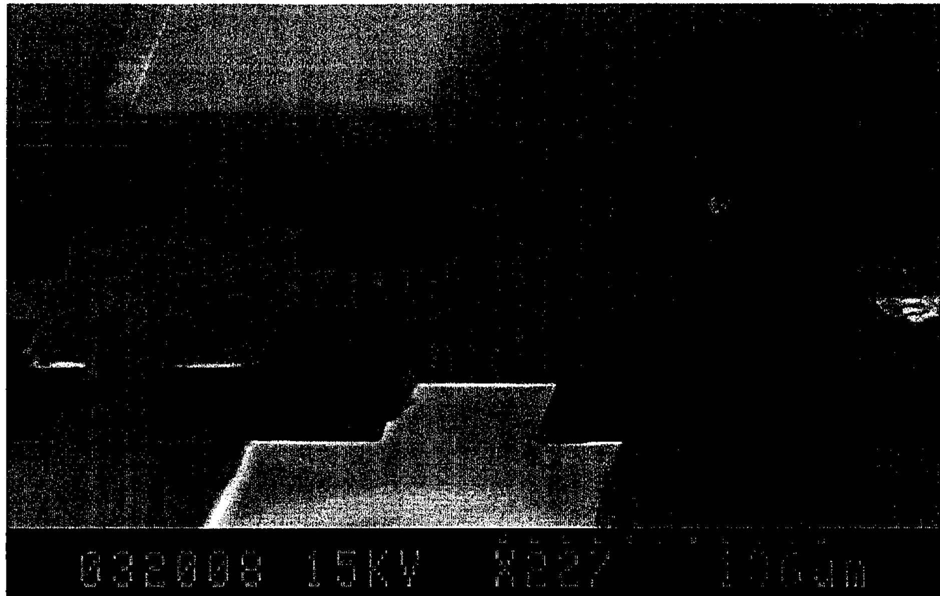

Figure 5.15 SEM Photo of CMOS Inductors After TMAH Etching

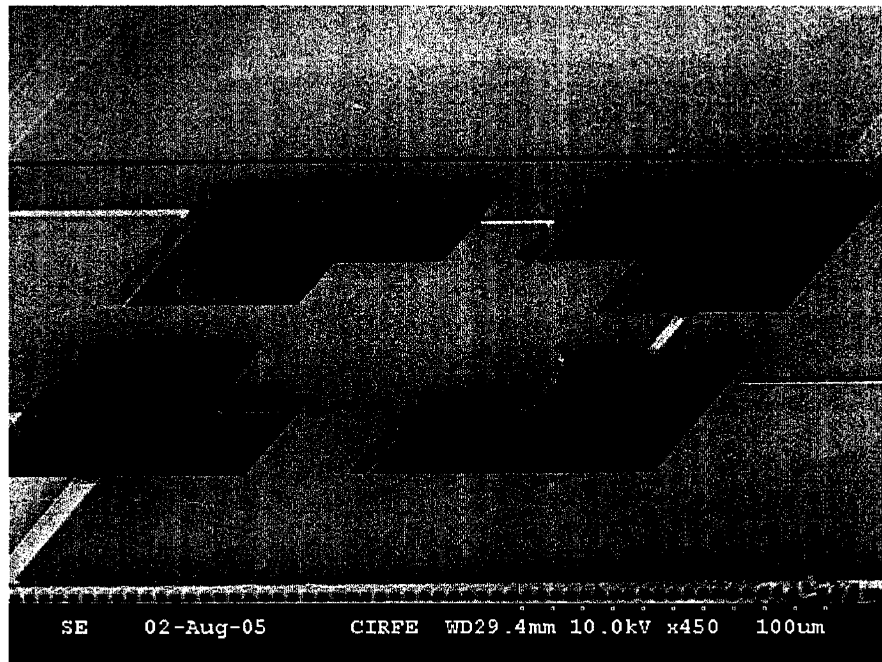

Figure 5.16 SEM Photo of Inductor of Figure 4.14 After TMAH Etching

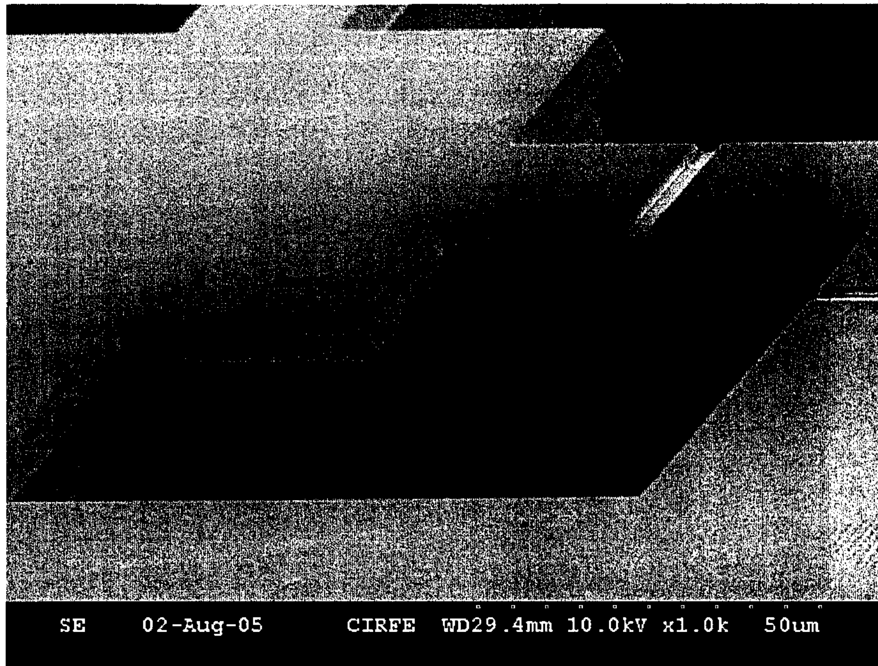

Figure 5.17 SEM Photo of One Etch Window of Figure 4.18

6. Characterization

6.1 DC Characterization of Switches (Pull-in Voltage Measurement)

Electrostatic pull-in is a well-known sharp instability in the behavior of an elastically supported structure subjected to parallel-plate electrostatic actuation. Because this phenomenon occurs very fast at a certain voltage, accurate measurement of the actuation voltage required to reach pull-in can be easily made at the wafer level using standard electrical test equipment. To make sure that the plates touch each other, either a microscope or a current measurement system (with current limit for protection) is needed. A voltage is applied to the upper movable conductor, causing it to deflect downward toward the underlying fixed ground plane due to the electrostatic actuation. At a critical pull-in voltage, V_{PI}, the upper conductor becomes unstable and spontaneously collapses to the ground plane. The pull-in voltage is related to the test structure's geometry and intrinsic material properties. Using models provided by [106-108], we are able to extract material properties from the pull-in data.

It is shown that the variation of pull-in voltage with in-plane structural dimensions (beam length) can be efficiently expressed in terms of two intermediate quantities called S and B parameters. S is the stress parameter and B is bending parameter. They are expressed in terms of $\tilde{\sigma}$ effective residual stress, t structure thickness, g_0 non-deformed gap and $\tilde{E}$ the effective stiffness for the test structure as [106-108]

$$S = \tilde{\sigma} t g_0^3 \qquad (6.1)$$

$$B = \tilde{E} t^3 g_0^3 \qquad (6.2)$$

For fixed-fixed beams (FBs), $\widetilde{E}$ is dependent on the beam width. A beam is considered wide when $w \geq 5t$. Wide beams exhibit plane-strain conditions, and therefore, $\widetilde{E}$ becomes the plate modulus [106-108].

$$\widetilde{E} = \frac{E}{1-\nu^2} \quad for \quad w \geq 5t \tag{6.3}$$

A beam is considered narrow when $w < 5t$. In this case, $\widetilde{E}$ simply becomes the young modulus E [106-108].

$$\widetilde{E} = E \quad for \quad w < 5t \tag{6.4}$$

It is assumed that FB's are fabricated by etching a film, which had an initial uniform biaxial stress σ_0. When a FB is etched from the biaxially stressed film, the resulting residual stress is approximated as uniaxial with a uniform value of [106-108]

$$\widetilde{\sigma} = \sigma_0(1-\nu) \tag{6.5}$$

where ν is the Poisson ratio.

Equation 3.16 was used to design the fixed-fixed beams. Now this equation is rewritten in terms of newly defined parameters, S and B.

$$L_{FB} = \sqrt{\frac{8\widetilde{\sigma}t + \sqrt{64\widetilde{\sigma}^2 t^2 + \frac{432\varepsilon_0 \widetilde{E} t^3 V_{PI}^2}{g_0^3}}}{\frac{27\varepsilon_0 V_{PI}^2}{4g_0^3}}} = \sqrt{\frac{8S + \sqrt{64S^2 + 432\varepsilon_0 B V_{PI}^2}}{\frac{27\varepsilon_0 V_{PI}^2}{4}}} \tag{6.6}$$

After measuring the pull-in voltage for different beam lengths, a nonlinear system of equations should be solved to find S and B. Then Young's modulus and Poisson ratio are easily calculated.

Test setup (similar to Figure 3.1) consists of four DC voltage sources in series to get voltages high enough to induce pull-in, current limiting resistor in series, two

manipulators with needle probes to make contact to the chip, voltmeter to set and measure the voltage, ammeter to measure the current to detect the pull-in instance and vacuum pump equipped probe station with microscope to hold the chip and observe the probe placement.

It is necessary to put the current limiting resistor in series with the circuit, because when the pull-in happens and two plates touch each other, a large current passing through the device will cause permanent damages to the device. Therefore putting current limiting resistor is essential to protection the device under test.

Numerical results are summarized in the Table 6.1. Beam numbers were introduced in tables 3.1-3.3 and Figure 3.13.

Beam#	1	3	4	5	6	8	9	10	11
V_{PI} (V)	101	151.5	206	256	312	339	350	110.6	110.9
Beam#	12	13	14	15	16	17	18		
V_{PI} (V)	166.9	223	280	326	310	302	302		

Table 6.1 Measured Pull-In Voltages of Fixed-Fixed Beams Fabricated in PolyMUMPS Technology

To calculate S and B, both sides of the Equation 6.6 can be squared,

$$8S+\sqrt{64S^2+432\varepsilon_0 V_{PI}^2 B}=\frac{27\varepsilon_0 V_{PI}^2 L_{FB}^2}{4} \quad (6.7)$$

Keeping the square root at one side results in,

$$\sqrt{64S^2+432\varepsilon_0 V_{PI}^2 B}=\frac{27\varepsilon_0 V_{PI}^2 L_{FB}^2}{4}-8S \quad (6.8)$$

Then to get rid of the square root, both sides are squared,

$$64S^2 + 432\varepsilon_0 V_{PI}^2 B = \left(\frac{27\varepsilon_0 V_{PI}^2 L_{FB}^2}{4} - 8S\right)^2 = \left(\frac{27\varepsilon_0 V_{PI}^2 L_{FB}^2}{4}\right)^2 + 64S^2 - 108\varepsilon_0 V_{PI}^2 L_{FB}^2 S \quad (6.9)$$

And finally after simplifications,

$$108\varepsilon_0 V_{PI}^2 L_{FB}^2 S + 432\varepsilon_0 V_{PI}^2 B = \left(\frac{27\varepsilon_0 V_{PI}^2 L_{FB}^2}{4}\right)^2 \quad (6.10)$$

Equation 6.10 holds for all of the fixed-fixed beams in general. To take advantage of measured voltages for beams with known lengths, we rewrite that equation for a particular beam by using an indexed notation.

$$108\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i S + 432\varepsilon_0 \left(V_{PI}^2\right)_i B = \left(\frac{27\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i}{4}\right)^2, i = 1.2, \cdots, N \quad (6.11)$$

Least-square method that is explained in appendix 1, is used to estimate S and B. Estimated values are shown as $\tilde{S}, \tilde{B}$.

Error is defined as

$$\delta_i = 108\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i \tilde{S} + 432\varepsilon_0 \left(V_{PI}^2\right)_i \tilde{B} - \left(\frac{27\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i}{4}\right)^2, i = 1.2, \cdots, N \quad (6.12)$$

And based on the above definition of the error, error function is defined as sum of the squared errors

$$Error = \sum_{i=1}^{N} \delta_i^2 = \sum_{i=1}^{N} \left[108\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i \tilde{S} + 432\varepsilon_0 \left(V_{PI}^2\right)_i \tilde{B} - \left(\frac{27\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i}{4}\right)^2\right]^2 \quad (6.13)$$

To minimize the error function, derivatives of error function with respect to S and B have to be made equal to zero.

$$\frac{\partial Error}{\partial \widetilde{S}} = 0 \Rightarrow$$

$$\sum_{i=1}^{N} \left\{ \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i \left[108\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i \widetilde{S} + 432\varepsilon_0 \left(V_{PI}^2\right)_i \widetilde{B} - \left(\frac{27\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i}{4} \right)^2 \right] \right\} = 0 \tag{6.14}$$

Following equation is the result of separation of known and unknown quantities,

$$\left\{ \sum_{i=1}^{N} \left[108\varepsilon_0 \left(V_{PI}^4\right)_i \left(L_{FB}^4\right)_i \right] \right\} \widetilde{S} + \left\{ \sum_{i=1}^{N} \left[432\varepsilon_0 \left(V_{PI}^4\right)_i \left(L_{FB}^2\right)_i \right] \right\} \widetilde{B} = \sum_{i=1}^{N} \left[\left(\frac{27\varepsilon_0 \left(V_{PI}^3\right)_i \left(L_{FB}^3\right)_i}{4} \right)^2 \right] \tag{6.15}$$

$$\frac{\partial Error}{\partial \widetilde{B}} = 0 \Rightarrow$$

$$\sum_{i=1}^{N} \left\{ \left(V_{PI}^2\right)_i \left[108\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i \widetilde{S} + 432\varepsilon_0 \left(V_{PI}^2\right)_i \widetilde{B} - \left(\frac{27\varepsilon_0 \left(V_{PI}^2\right)_i \left(L_{FB}^2\right)_i}{4} \right)^2 \right] \right\} = 0 \tag{6.16}$$

Following equation is the result of separation of known and unknown quantities,

$$\left\{ \sum_{i=1}^{N} \left[108\varepsilon_0 \left(V_{PI}^4\right)_i \left(L_{FB}^2\right)_i \right] \right\} \widetilde{S} + \left\{ \sum_{i=1}^{N} \left[432\varepsilon_0 \left(V_{PI}^4\right)_i \right] \right\} \widetilde{B} = \sum_{i=1}^{N} \left[\left(\frac{27\varepsilon_0 \left(V_{PI}^3\right)_i \left(L_{FB}^2\right)_i}{4} \right)^2 \right] \tag{6.17}$$

Equations .6.15 and 6.17 form a system of 2 equations with 2 unknown variables $\widetilde{S}$ and $\widetilde{B}$ that can be written as

$$\begin{cases} a_1 \widetilde{S} + b_1 \widetilde{B} = c_1 \\ a_2 \widetilde{S} + b_2 \widetilde{B} = c_2 \end{cases} \tag{6.18}$$

where the constants are defined as

$$\begin{aligned} a_1 &= 108\varepsilon_0 \sum_{i=1}^{N} \left[\left(V_{PI}^4\right)_i \left(L_{FB}^4\right)_i \right],\ b_1 = 432\varepsilon_0 \sum_{i=1}^{N} \left[\left(V_{PI}^4\right)_i \left(L_{FB}^2\right)_i \right],\ c_1 = \left(\frac{27\varepsilon_0}{4} \right)^2 \sum_{i=1}^{N} \left\{ \left[\left(V_{PI}^3\right)_i \left(L_{FB}^3\right)_i \right]^2 \right\} \\ a_2 &= 108\varepsilon_0 \sum_{i=1}^{N} \left[\left(V_{PI}^4\right)_i \left(L_{FB}^2\right)_i \right],\ b_2 = 432\varepsilon_0 \sum_{i=1}^{N} \left[\left(V_{PI}^4\right)_i \right],\ c_2 = \left(\frac{27\varepsilon_0}{4} \right)^2 \sum_{i=1}^{N} \left\{ \left[\left(V_{PI}^3\right)_i \left(L_{FB}^2\right)_i \right]^2 \right\} \end{aligned} \tag{6.19}$$

This system of equation can easily be solved to find $\widetilde{S}$ and $\widetilde{B}$, and the solution is

$$\begin{cases} a_1\widetilde{S} + b_1\widetilde{B} = c_1 \\ a_2\widetilde{S} + b_2\widetilde{B} = c_2 \end{cases} \Rightarrow \widetilde{S} = \frac{b_2c_1 - b_1c_2}{a_1b_2 - a_2b_1}, \widetilde{B} = \frac{a_1c_2 - a_2c_1}{a_1b_2 - a_2b_1} \quad (6.20)$$

According to 6.1 and 6.2

$$\widetilde{\sigma} = \frac{\widetilde{S}}{tg_0^3}, \ \widetilde{E} = \frac{\widetilde{B}}{t^3g_0^3},$$

Above equations are implemented in MATLAB. Using the measured pull-in voltages, values of $\widetilde{\sigma} = 1.19610^7 Pa, \ \widetilde{E} = 1.079 \times 10^9 Pa$ are obtained.

6.2 RF characterization using VNA

To find the equivalent inductance, capacitance and resistance of fabricated inductors at high frequencies, the S-parameter (reflection coefficient) [123-124] of inductor as a one-port device is measured and then impedance is calculated from reflection coefficient and port characteristic impedance.

Reflection coefficient is measured by on-wafer probes and Agilent (HP) 8753D vector network analyzer.

Figure 6.1 shows the test setup. Figure 6.2 shows the probe during measurement.

Figures 6.3 and 6.4 show two measurements over the frequency range of 0-3 GHz. Measurement results are shown on the Smith chart. Smith chart displays the normalized measured impedance (here, normalizing impedance is the characteristic impedance of the measurement port of the VNA, that is 50 Ohms). Center of the circle corresponds to 1.00 (i.e. 50 Ohms). The intersection of the centerline and the outer circle at right and left shows the open circuit and the short circuit, respectively. Inductive and capacitive impedances are the points above and below the centerline, respectively.

Ideally, the a pure inductive impedance starts from the short circuit point and continues with increasing the frequency along the outer circle in the clockwise direction.

The difference between the measured and ideal characteristics is mainly due to these factors:

- The calibration is performed at the tip of the probe using the impedance standard substrate (ISS). For our one-port measurement, standard open-circuit, short-circuit and matched load (50 Ohm) impedances are required for the calibration. Short-circuit and matched load impedances are provided on the ISS. But for the open-circuit, the probe is moved up at a reasonable distance from the chuck of the probe station. This method doesn't give a high-quality open-circuit impedance that affects the performance of the measurement.
- The inductor is connected to the probe through the bonding pads. Bonding pads are made of alternating layers of dielectrics and conductors that have a large capacitance. To remove this capacitance, another set of the same bonding pads that are not connected to anything should be provided as de-embedding structures. But because of lack of space on the chips, it wasn't possible to put the de-embedding structures, and therefore the measured impedance can't be interpreted quantitatively.
- After the etching, despite taking the protective measures, some of the aluminum on the top of the bonding pad is removed that causes increased series resistance in the measurement path.

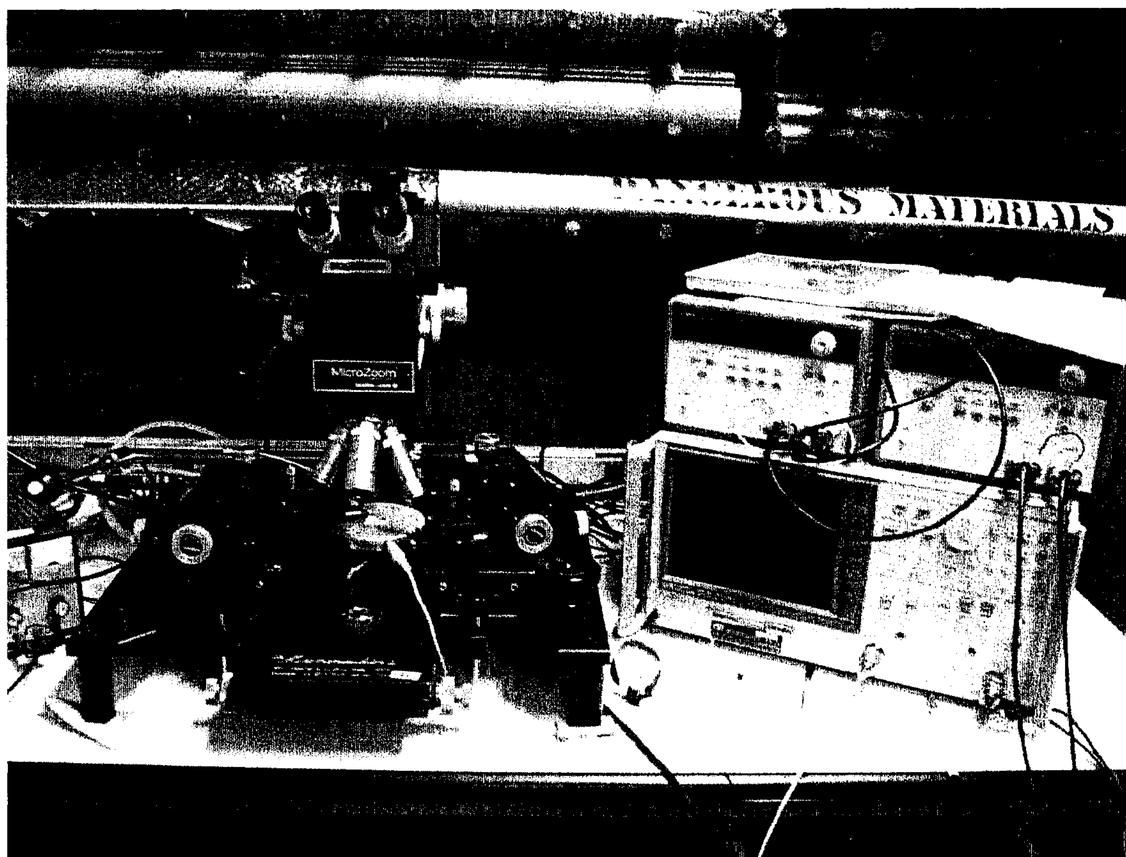

Figure 6.1Test Setup

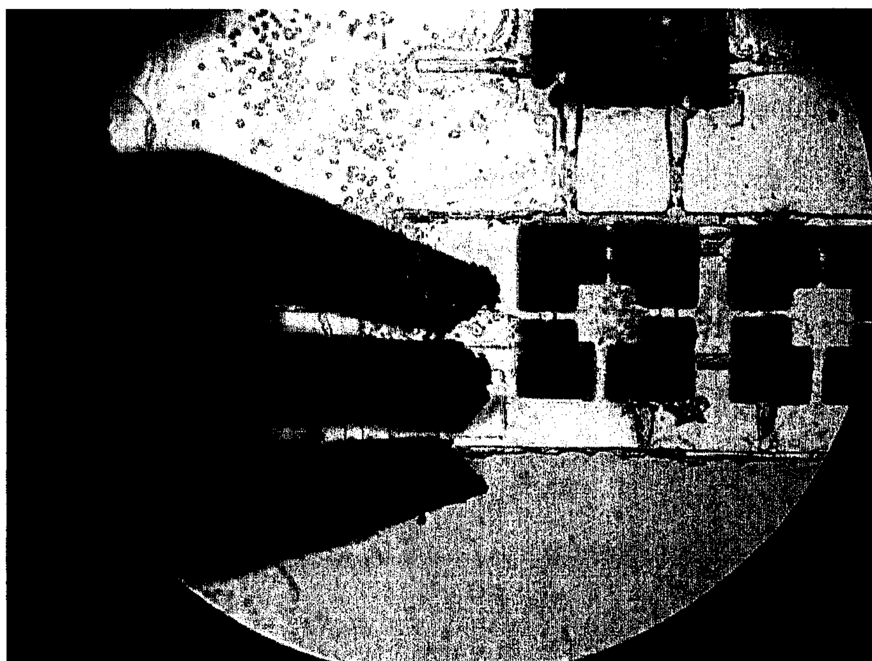

Figure 6.2 Probe During Measurement

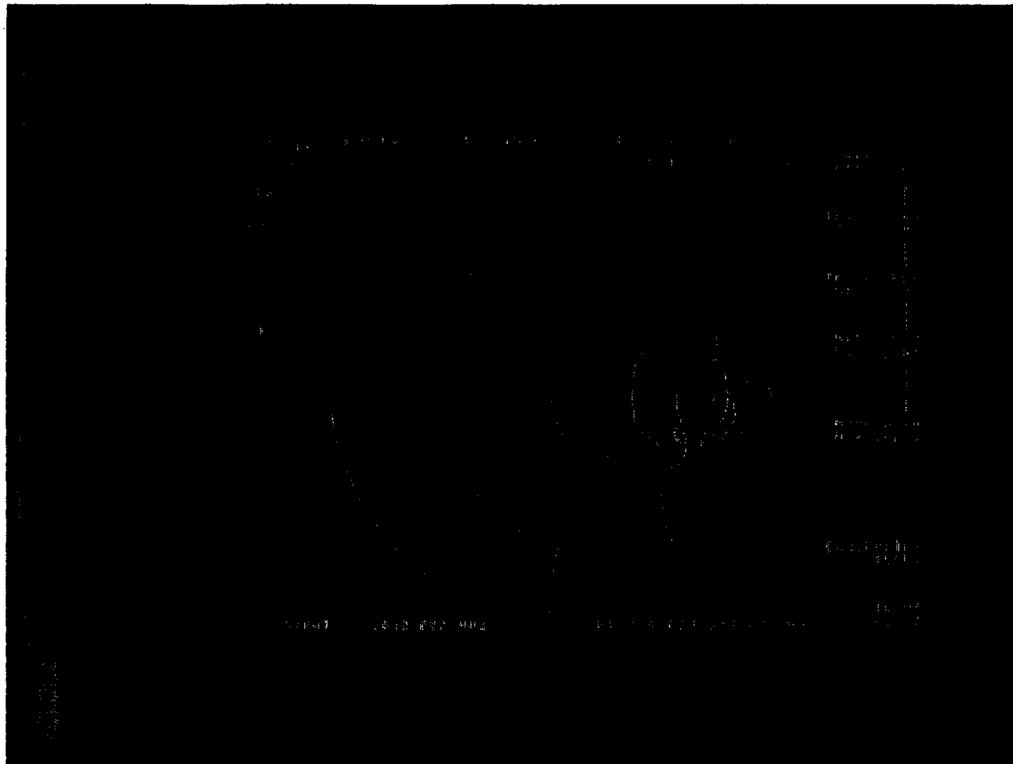

Figure 6.3 A Measurement Result: Variation of Impedance vs. Frequency on the Smith Chart

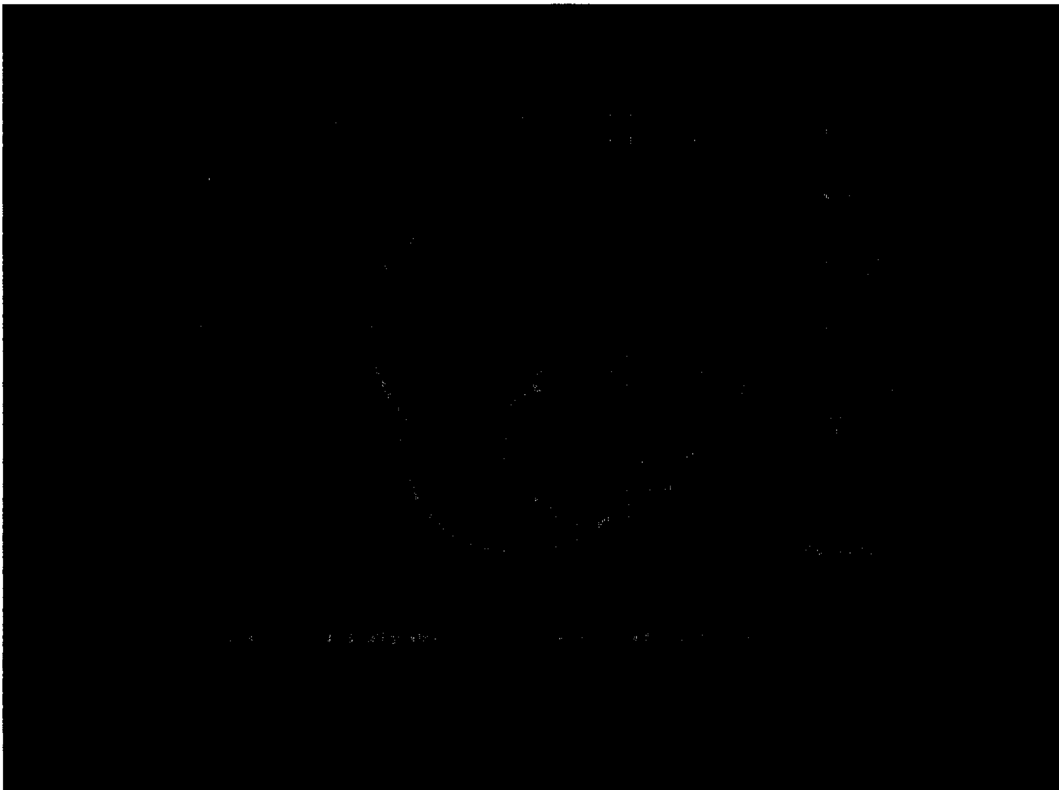

Figure 6.4 Another Measurement Result: Variation of Impedance vs. Frequency on the Smith Chart

7. Conclusion

7.1 Conclusions

In this work, a set of switches are designed and fabricated in MUMPS process. Also, two sets of inductors are designed and fabricated, one in MUMPS process and the other one using CMOS technology.

Based on the simulations, measurements and characterization the following are concluded:

- Measured pull-in voltages of fabricated fixed-fixed beams are higher than designed values. This shows that Young's modulus, Poisson ratio and residual stress are different from values considered in the design.
- Assumed material properties for MUMPS process are different from measured values, but because only one type of beams is fabricated, more information can not be extracted.
- Pull-in voltage of short beams is so high that it can not be measured in normal conditions. Required high voltage creates a spark in the gap between the beams and damages the beam before pull-in occurs. Measurement in vacuum may prevent this.
- Etch holes have a negligible effect on pull-in voltages.
- Quality factor of MUMPS inductors is comparable to CMOS inductors before micromachining.
- Quality factor and resonance frequency of micromachined inductors is increased 3 times comparing to inductors before micromachining.

- The silicon underneath the inductors was not completely removed due to the orientation of etch windows. Etch windows should have an angle to (100) plane, or have to encircle 3 sides of the structure to be released.
- The results of on-wafer measurements can not be used directly due to the lack of de-embedding structures on the chip. Due to the large capacitance of bonding pads, the contribution of the inductor in the impedance is buried in large capacitive impedance. Bonding pads also exhibit inductive and resistive behavior at different frequencies.
- Quality of chips that their oxide is removed by RIE is much better compared to those which their oxide is removed by wet etching. But to use RIE, the thick low resistance top metal layer is sacrificed as protecting mask.
- Aluminum damage can be minimized or even prevented by using the additives during oxide and silicon etching.

7.2 Suggested Future Work

Following works are suggested to continue this project:

- Combining RIE, isotropic and anisotropic silicon etching to completely remove silicon underneath the inductors
- Using inductors in filter circuits along with capacitors
- Simulating CMOS and MUMPS bonding pads in a 3D electromagnetics software and de-embedding their effect from measurements

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9. Appendix 1. Least Square Estimation

The problem is defined as finding the best possible values for a set of m unknowns z_1, z_2,... z_m, related by n linear equations

$$\sum_{j=1}^{m} \alpha_{ij} z_j = \beta_i, i = 1,2,...,n$$

where α and β are constant coefficients and $n \geq m$.

Let δ_i be the amount by which the ith equation fails to be satisfied. We consider the discrepancies δ_i defined as

$$\delta_i = \sum_{j=1}^{m} \alpha_{ij} z_j - \beta_i \neq 0, i = 1,2,...,n$$

and will try to find values of z_i which will make least square error E as small as possible. E is defined as

$$E = \sum_{i=1}^{n} \delta_i^2 = \sum_{i=1}^{n} \left(\sum_{j=1}^{m} \alpha_{ij} z_j - \beta_i \right)^2$$

To minimize E, that has a quadratic form, we must set to zero all of first derivatives of E with respect to z_i, i.e.

$$\frac{\partial E}{\partial z_i} = 0, i = 1,2,...,m$$

For z_k

$$\frac{\partial E}{\partial z_k} = \frac{\partial}{\partial z_k} \left[\sum_{i=1}^{n} \left(\sum_{j=1}^{m} \alpha_{ij} z_j - \beta_i \right)^2 \right] = 2 \sum_{i=1}^{n} \left[\sum_{j=1}^{m} \alpha_{ij} z_j - \beta_i \right] \alpha_{ik} = 0, k = 1,2,...,m \Rightarrow$$

$$\sum_{i=1}^{n} \left[\sum_{j=1}^{m} \alpha_{ij} z_j - \beta_i \right] \alpha_{ik} = \sum_{i=1}^{n} \alpha_{ik} \beta_i, k = 1,2,...,m$$

This way, a non-consistent n by m system of equations is reduce to a consistent m by m system of equations that can easily be solved by matrix methods.

This method is widely used in estimation problems that several measurements are performed to estimate some parameters.

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