GALLIUM-NITRIDE-BASED POWER ELECTRONIC CONVERTER DESIGN, PROTOTYPING AND TESTING FOR AUTOMOTIVE POWER MANAGEMENT AND RENEWABLE ENERGY APPLICATIONS

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ABSTRACT

Gallium-Nitride-Based Power Electronic Converter Design, Prototyping and Testing for Automotive Power Management and Renewable Energy Applications

Shayan Dargahi

Wide band-gap semiconductors, such as GaN have shown promising characteristics for use in the future power electronic applications. Compared to the mainstream Si technology, GaN-based devices can function at higher temperatures, offer higher breakdown voltages up to 500 times higher than Si, and have lower on-resistance, approximately 10 times lower than the respective value in a Si switch. In this thesis, improved device figure of merit (FOM) $R_{on} Q_{sw}$ resulted from GaN's fast switching speed and low on-resistance is utilized to enhance the power conversion FOM: Efficiency density/cost. To prove this idea, two half-bridge DC-DC converters with the same ratings and elements using GaN and Si switches are designed and the superior performance of GaN-based converter in terms of efficiency and size is confirmed through simulation and experiment. Simulation is based on the Spice models of commercial GaN and Si switches. Finally, design of GaN-based high electron mobility transistor for power applications is reported. According to the literature review and analytical calculations expected values in terms of switch breakdown voltage, on-resistance, and current capacity are predicted, followed by designing a mask set according to a typical fabrication process of AlGaN/GaN HFET.

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Author would like to dedicate this work to his

Mother, Mrs. Forouzan Vasighi and Father, Dr. Akbar Dargahi.

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CHAPTER 1

INTRODUCTION

1.1 POWER ELECTRONICS IN AUTOMOTIVE AND RENEWABLE ENERGY APPLICATIONS

Due to the increasing attention to the issue of green house gas emission of gasoline and diesel vehicles, recently significant attention has been paid to development of hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), and fuel cell hybrid vehicles (FCHVs) by automotive companies [1]. HEVs combine the internal combustion engine of a conventional vehicle with an electric motor, which could effectively reduce the emission while offering better fuel economy. These vehicles employ inverters and DC/DC converters in their motor drive stage. Fig. 1-1 illustrates a general overview of the drive structure of an HEV. Automotive power electronics is the enabling technology to develop various electrical systems in this stage with the particular aim of reaching higher conversion efficiency and lowering of the cost. As can be seen in Fig. 1-1, these vehicles also suggest the possibility of including different hybrid energy sources such as batteries, fuel cells, and ultra-capacitors. In renewable energy systems, DC/DC converters are used to convert the electrical energy from the solar arrays to form a stable power source. Furthermore, nowadays multiple-input power converters are being used to in order to employ different renewable energy sources.

Choosing the most suitable topology, appropriate control strategy, and efficient power semiconductor devices are among the main challenges of today's power electronic

mentioned applications. This thesis will present novel approaches with regards to these three issues. In this treatment the main focus will be on analyzing new power semiconductor switch technologies. This issue is believed to be of great importance in the future automotive and renewable energy applications.

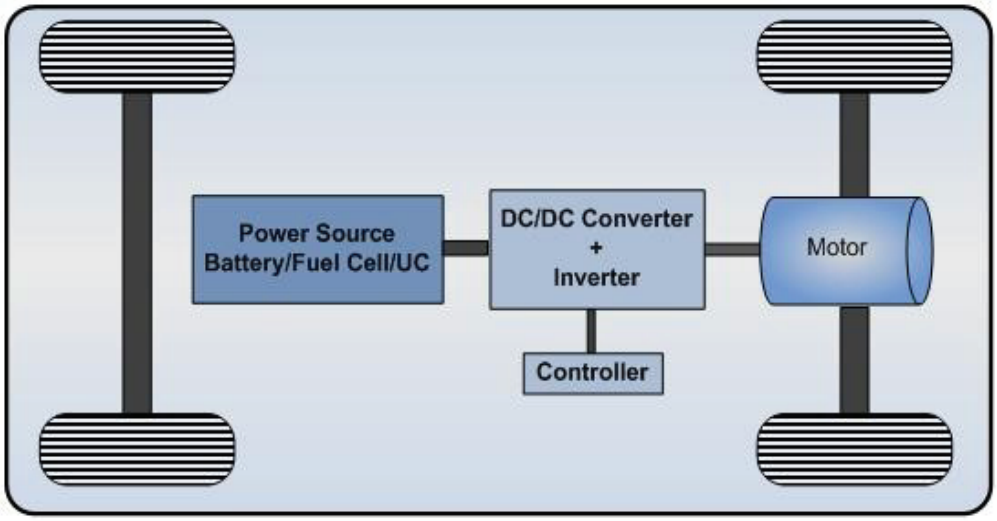

Fig. 1-1 Overview of the drive structure of HEVs.

This discussion will start by introducing the general properties of those wide band-gap semiconductors, such as SiC and GaN, which have so far shown the most promising characteristics for power electronic applications. Requirements of the target applications and essential necessities of power switches for the next generation hybrid vehicles will be discussed in the next section.

1.2 WIDE BAND-GAP SEMICONDUCTORS

1.2.1 GENERAL PROPERTIES

To reach improved performances in future automotive and renewable energy applications, higher power densities in power converters is required. In high-power

density power converter designs, power losses in switching devices determine the volume of cooling systems. Currently, the silicon-based power field effect transistors (FETs) are approaching their performance limits determined by material limitations [2]. This issue has motivated research on adopting wide band-gap (WBG) semiconductors in power electronics applications. Thanks to their wider band-gap compared to Si, these semiconductors can function at higher temperatures. Furthermore, larger breakdown electric-field of WBG semiconductors offers breakdown voltages up to 500 times higher than Si at the same doping density [2]. Lower on-resistance is another huge advantage of WBG semiconductors, which directly lessens the conduction losses of the switches of a converter. For GaN and SiC, this value is approximately 10 times lower than the respective value in a Si switch [3]. Higher thermal conductivity of SiC, in comparison to Si corresponds to more efficient heat transfer to the heat sink and thus gaining lower junction temperature. Such a property can be manifested also to GaN technology if SiC substrate is adopted. These properties which are gathered and compared to Si in Table 1.1, along with some other material properties are crucial to automotive applications [4]. As for the power density, study in [5] for a 3.2 kW power factor correction (PFC) circuit, confirms better efficiency of SiC-based converter while reducing the size of the respective SiC switch down to 28% of the Si MOSFET. Same studies for GaN for a different application also demonstrate the high power densities up to 9.8 W/mm which is around ten times the value for Si switches [6]. Characteristics of SiC and GaN will be further discussed and compared with each other in the next section.

Table 1-1 Comparison of a few important properties of Si, GaN, and SiC at 300K [4]-[7].

Material	Band gap (eV)	Electron mobility (cm^2/Vs)	Density (g/cm^3)	Breakdown field(V/cm)	Thermal conductivity (W/m.K)
Si	1.12	1400	2.33	300,000	130
SiC	3.26	700	6.1	3,180,000	490
GaN	3.44	900	3.21	3,000,000	110

1.2.2 COMPARISON OF SILICON-CARBIDE WITH GALLIUM-NITRIDE

As it was mentioned before, SiC is the ideal semiconductor for automotive power electronic application, due to its thermal conductivity and wide band-gap. Higher thermal conductivity of SiC compared to GaN and Si, means that SiC devices can conduct heat more efficiently and operate at higher power densities than either GaN or Si. This characterisitc combined with wide band-gap and high critical field, provide SiC-based devices an advantage when high power is the desirable device feature. However, since SiC is a complicated material to grow, the microfabrication processes associated with implementing devices in this technology still requires quite a bit of improvement. The other important challenge of WBG semiconductors is the tremendous cost of SiC wafers in comparison to Si wafers. Moreover, the wafer quality of SiC should be improved in terms of reducing the defect density. In addition, power devices because of their higher current ratings require more area on the wafer than the regular low power devices. This issue aggravates the cost of SiC devices implemented on these expensive SiC wafers.

GaN, on the other hand, has been used in optoelectronics for many years attaining a more developed stage of technology. GaN devices have higher electron mobility than SiC, which translates into lower on-resistance. However, their high temperature performance is not as excellent as SiC. One of the challenges of GaN is choosing the proper substrate. Presently, sapphire, SiC, and Si are being used as substrates, with the first two as common choices [8]. Among sapphire and SiC, due to the higher thermal conductivity, SiC is preferred for high power and high temperature applications. This is in spite of its higher price. Generally speaking, lack of a lattice matched substrate is one of the drawbacks of GaN technology.

1.3 REQUIREMENTS OF AUTOMOTIVE APPLICATIONS

1.3.1 HIGH BREAKDOWN VOLTAGE

Hybrid vehicles utilize battery packs with nominal voltages in the range of 150 V to 350 V. This voltage is then boosted by means of a DC/DC converter up to 500-600 V, which is to be used as the input for the inverter stage. These values have been increasing since the introduction of Toyota Prius in 1997, which was implemented by a 277 V battery directly connected to the motor drive stage. Higher power motors which are highly expected in the future hybrid vehicles require higher voltage ratings. This directly establishes the need for higher breakdown voltages for the power switches applied to both DC/DC converter and the inverter of a hybrid drive system. Fig. 1.2 shows the increase in power demand of Toyota's hybrid vehicles illustrating the increase in voltage boost up to 600V.

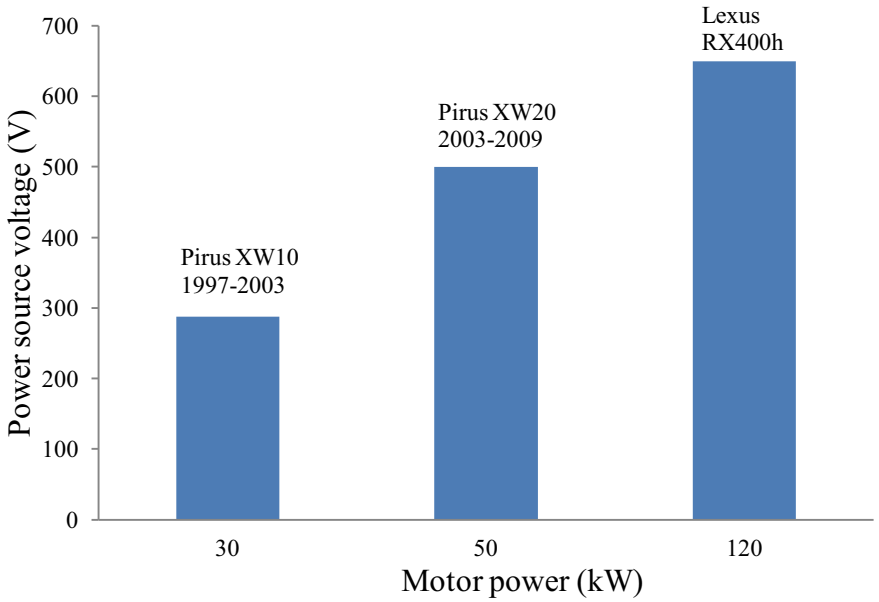

Fig. 1-2 Power source voltage vs. electric motor power [7].

Breakdown voltages of power switches in today's HEV inverters are about 1.1 kV [7]. These values will become higher in the future, which implies the necessity of adopting new semiconductor technologies to meet the respective demands as regular Si switches could not address them any longer.

1.3.2 HIGH TEMPERATURE OPERATION

This factor has been one of the main motivations of researchers toward introducing new semiconductor technologies into mentioned applications. Regular Si devices due to their increasing leakage current under high temperature motor environment (*i.e.* close to 150˚C) will have high power loss. With regards to this, the most critical parameters are on-resistance and threshold voltage of the device. The on-resistance and therefore the conduction losses will approximately be doubled with increasing the ambient temperature from 25˚C to 125˚C [9]. Therefore, a secondary

cooling system has to be incorporated in order to keep the suitable junction temperature. Wide band-gap semiconductors such as SiC and GaN can operate at temperatures well above the aforementioned 150˚C and as a result do not require a cooling system. Therefore, implementing switching circuits based on these two semiconductors families (*i.e.* GaN and SiC) offer the possibility of removing the secondary cooling system and improving the efficiency [10].

1.3.3 LOW ON-RESISTANCE

To reach higher conversion efficiencies, the on-resistance of the switches should be decreased as much as possible. This will directly affect the conduction losses of switches in DC/DC converters and also inverters. Loss analysis of a typical converter will be thoroughly presented in chapter four of this thesis. Specific on-resistance of a lateral FET is inversely proportional to the electron channel concentration, which in GaN technology is about an order of magnitude higher than Si. Therefore, with the addition of effect of the enhanced electron mobility of GaN channel, even with the identical design criteria of the maximum switching voltage, a GaN switch has 10-100 times lower on-resistance than that of a Si switch [11].

1.3.4 NORMALLY-OFF OPERATION

In normally-off switches drain current is to zero at zero gate-source voltage. As a result, circuits implemented in normally-off device technologies avoid the loss of power in stand-by mode. Si-based insulated gate bipolar transistors (IGBTs), which are currently being implemented in vehicles inverters, are normally-off switches, while the issue of realization of normally-off switches has yet to be resolved in GaN technology.

Currently, this is an ongoing area of research [12]. With realization of these switches in GaN technology, lower losses and simplified inverter circuits are realizable in the normally-off GaN switch technology.

1.4 CONTRIBUTION OF THE THESIS

The major contributions of this thesis are:

(a) Discussing the advantages of introducing wide band-gap semiconductor-based switches, particularly GaN, into future automotive and renewable energy power electronics.

(b) Comparing the performance of GaN and Si switches in a typical DC/DC converter in terms of efficiency by means of their developed Spice models.

(c) Evaluating GaN-based DC/DC converter in a battery-ultra capacitor energy storage system.

(d) Design, prototyping, and testing of the proposed converter and comparison with a conventional Si-based converter.

(e) Design of new GaN-based power HEMTs for future power applications.

1.5 THESIS OUTLINE

The contents of this thesis are organized into 6 chapters. Chapter 2 deals with modeling and simulation of GaN-based switches. Loss analysis of a typical two quadrant half-bridge converter, simulated with the proposed switch models is also included in this chapter. Chapter 3 evaluates the different battery-ultra capacitor energy storage systems and their control strategies. Chapter 4 presents the experimental prototype of the aforementioned power management system confirming the higher efficiency for the GaN-

based converter. Chapter 5 focuses on designing GaN devices with the intention of applying them to the future automotive and renewable energy applications. Process flow of the fabrication is presented in detail. Chapter 6 summarizes the overall conclusions and presents an appropriate list of future research.

CHAPTER 2

POWER DISSIPATION ANALYSIS OF POWER ELECTRONIC DEVICES

2.1 INTRODUCTION

The aim of this chapter is to compare the switching behavior of GaN switches with the state of the art Si MOSFETs. Associated parameters in determining the power dissipation of a switch are initially discussed and compared between commercial GaN and Si switches. The Spice models of the switches provided by the manufacturers are used to simulate typical half-bridge DC/DC converters and to analyze the switching behavior, loss and conversion efficiency of the circuits. High switching loss, generally due to the slow switching of power devices, limits the key power conversion figure of merit (FOM) of efficiency × density/cost. One of the possible contributions of GaN power transistors in high-voltage/high-frequency applications is in correspondence to the improvement of the aforementioned FOM by increasing the frequency of operation.

2.2 MOSFET POWER DISSIPATION

The sources of loss in MOSFETs can be grouped into two main categories: switching losses and conduction losses. Conduction losses, which are also being referred to as static losses in literature (*i.e.* P_{stat}), mainly depend on the on-resistance of the switch (*i.e.* $R_{ds\text{-}on}$). With I_o being the average current going through the switch during the on time and D referring to the duty cycle, conduction losses could be calculated as [13]:

$$P_{static} = D\, I_o^2\, R_{ds\text{-}on} \tag{2-1}$$

In this calculation it is necessary to accurately estimate the on-resistance. This is due to the fact that this parameter is variable with junction temperature. The variation of normalized on-resistance with the temperature is generally provided in the datasheets of the switch.

For analyzing the switching losses, the waveforms of current and voltage during a typical switching cycle is sketched in Fig. 2-1. In this figure, on and off switching times are indicated by t_1+t_2 and t_3+t_4. Switching losses during the turn-on period are calculated as [13]:

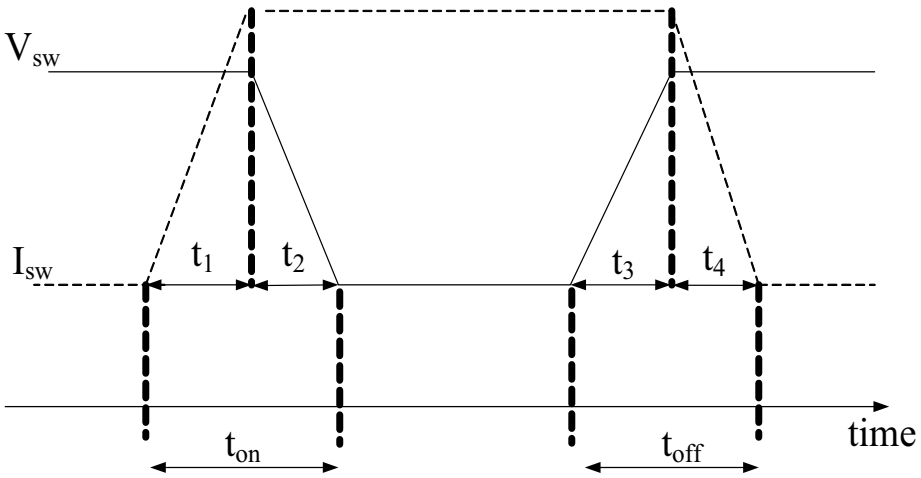

Fig. 2-1 Typical turn-on (t_{on}) and turn-off (t_{off}) switching waveforms of a switch.

$$p_{sw}^{on} = \frac{1}{T}\int_0^{t_{on}} V_{sw} I_{sw}\, dt \cong \frac{1}{T}\int_0^{t_1} V_{sw} \frac{I_{sw,av}}{t_1}\, t\, dt + \frac{1}{T}\int_0^{t_2} I_{sw,av} \frac{V_{sw}}{t_2}\, t\, dt = \frac{V_{sw} I_{sw,av} t_1}{2T} + \frac{V_{sw} I_{sw,av} t_2}{2T} \tag{2-2}$$

The involved parameters are defined in Fig. 2-1. $I_{sw,av}$ is the average value of the current going through the switch in turn-on process and T is the period. Similarly, the switching loss during the turn-off process is calculated as:

$$p_{sw}^{off}=\frac{1}{T}\int_0^{t_{off}} V_{sw}I_{sw}dt \cong \frac{1}{T}\int_0^{t_3} V_{sw}\frac{I_{sw,av}}{t_3}tdt+\frac{1}{T}\int_0^{t_4} I_{sw,av}\frac{V_{sw}}{t_4}tdt=\frac{V_{sw}I_{sw,av}t_3}{2T}+\frac{V_{sw}I_{sw,av}t_4}{2T} \quad (2\text{-}3)$$

If the values for t_1 and t_2 are assumed to be equal:

$$t_1=t_2=\frac{t_{on}}{2} \quad (2\text{-}4)$$

With the same assumption for turn-off period:

$$t_3=t_4=\frac{t_{off}}{2} \quad (2\text{-}5)$$

With these assumptions the total amount of switching losses can be calculated as:

$$P_{sw}^{total}=P_{sw}^{on}+P_{sw}^{off}=\frac{V_{sw}I_{sw,av}}{2T}(t_{on}+t_{off}) \quad (2\text{-}6)$$

To compare the switching losses of different switches, this equation should be linked to the parameters provided in the data sheets. To do so, on and off switching times can be approximated by:

$$t_{on} \cong t_{off} \cong \frac{Q_g}{I_G} \quad (2\text{-}7)$$

Where I_G is the gate drive current and Q_g is the gate switch charge. Both parameters can be found in the data sheet of the power switch.

In the analysis of these parameters versus the variation of semiconductor technology, GaN switch (*i.e.* EPC1010) with one of the highest ratings in today's market

has been chosen. Higher breakdown voltages are currently expected in the market, however, for the present time, 200 V, 12 A with 25 mΩ on-resistance offered by this commercial device are one of the best. To make a realistic comparison between GaN and Si switches, Si switch ratings have been chosen to be as close as possible to this GaN switch. Since the ultimate goal is to compare these two technologies in terms of the converter efficiency, a Si switch (i.e. IPP320N20N3G from Infineon) is chosen. This MOSFET has low $R_{ds\text{-}on}$ of 32 mΩ, while having the same voltage rating of 200 V, as the GaN switch. The price is almost the same for both of the switches whereas the Si switch is even capable of handling much higher currents (*i.e.* in the order of 34 A) [14], [15]. As for the anti-parallel diode, only majority carriers are involved in GaN device conduction, therefore there is zero reverse recovery. The forward voltage of the internal diode is higher than the diode forward drop in Silicon based FET, which necessitates the dead time or the diode conduction time to be minimized to get maximum efficiency.

Lower values for the gate-drain capacitance (*i.e.* C_{gd}) coming from the lateral structure of GaN switches, alongside smaller values of gate-source capacitance (*i.e.* C_{gs}) compared to Si switch, make the total gate charge (Q_g) of the switch which is the integral of voltage variable capacitances (*i.e.* C_{gs} + C_{gd}) over voltage, much smaller for GaN switches. This lower gate charge contributes to faster and more efficient switching [16]. Table 2-1, compares the gate switch charge (Q_g) for the two switches from the two semiconductor technologies (*i.e.* GaN and Si).

Table 2-1 Parameter comparison of Si and GaN.

Switch	V_{ds} (V)	I_{ds} (A)	R_{ds} (Ω)	Q_g (nC)	$R_{ds} \times Q_g$, FOM (Ω-nC)
Si (IPP320N20N3G)	200	34	0.0032	22	0.0704
GaN (EPC1010)	200	12	0.0025	7.5	0.01875

Assuming the same level of gate driver current, this table clearly confirms that at the same switching frequency, implementing GaN switches can result in much lower switching losses. Consequently, with remarkable improvement in key device FOM of $R_{ds\text{-}on} \times Q_g$, GaN high power transistors will boost the power conversion FOM of Efficiency×Density/Cost by an order of magnitude in comparison to best Si MOSFET performance.

2.3 SWITCHING CHARACTERISTICS

Spice models of the aforementioned commercial switches are implemented in a simple bias circuit with $R_D = 25\ \Omega$ and $V_D = 10$ V, to compare the switching behavior between two technologies. Fig. 2-2 and Fig. 2-3 compare the turn-off and turn-on transition of Si and GaN switches.

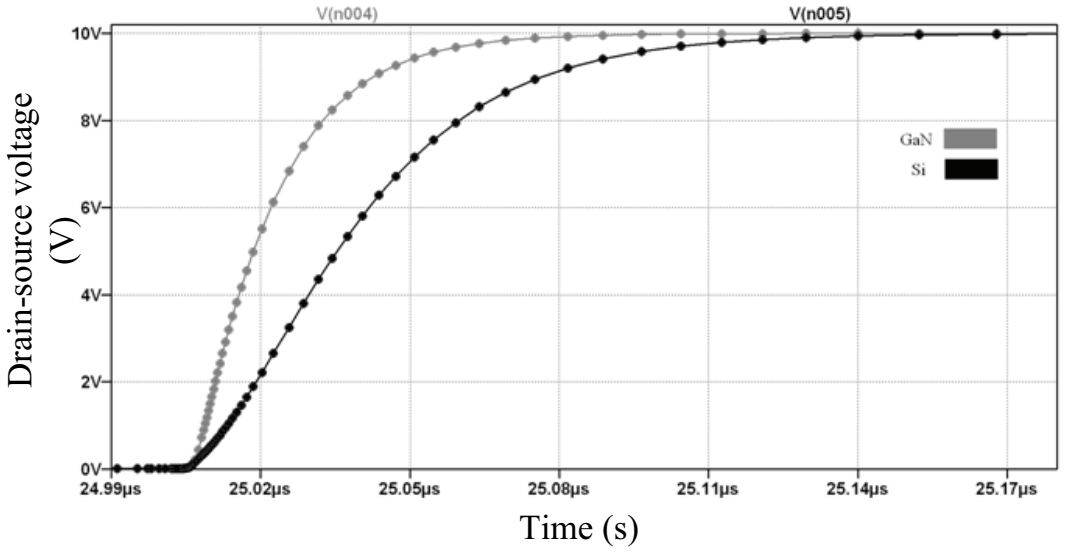

Fig. 2-2 Switch turning-off transition (10 V, 0.4 A), GaN and Si switch comparison.

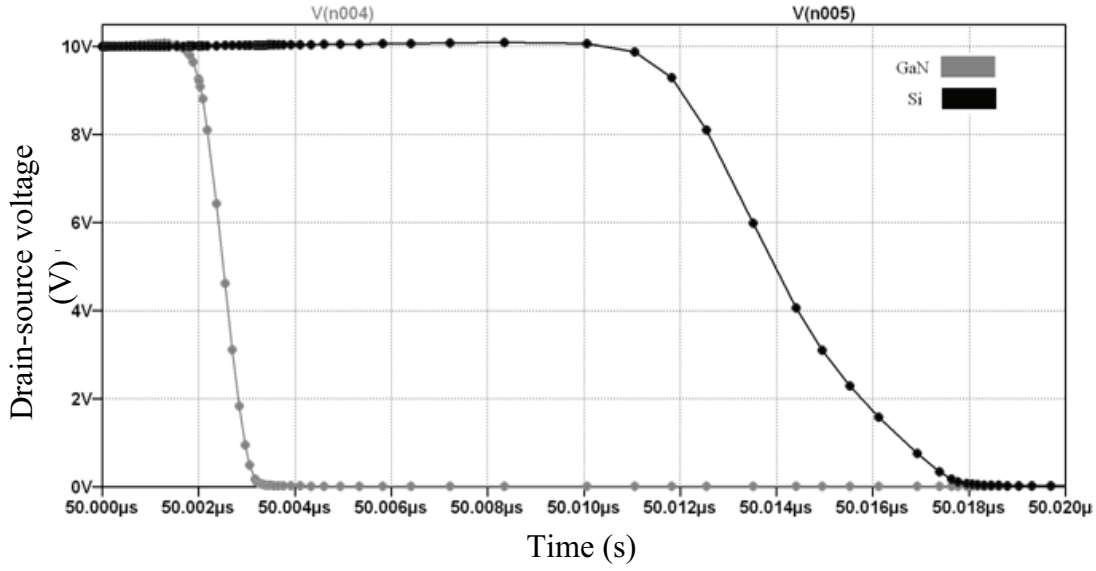

Fig. 2-3 Switch turning-on transition (10 V, 0.4 A), GaN and Si switch comparison.

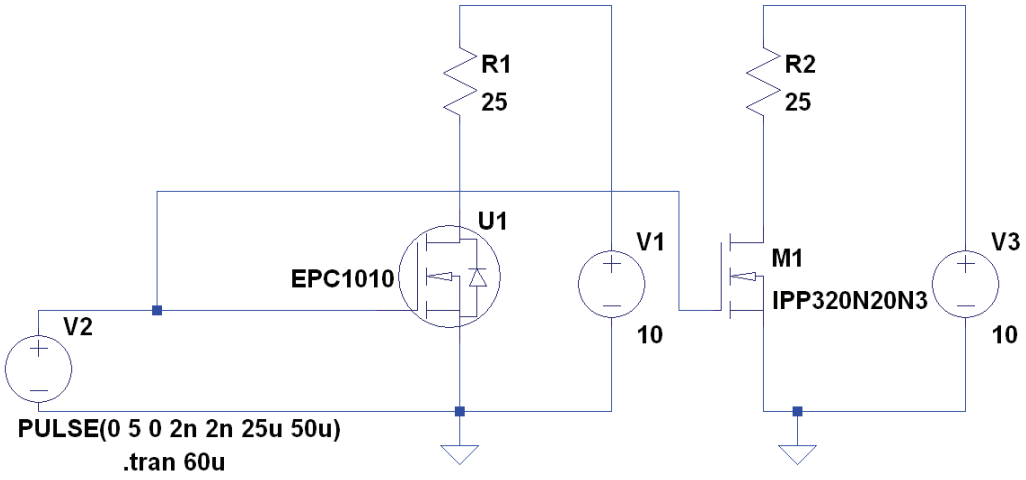

Fig. 2-4 Bias circuit to compare switching time between EPC1010 and IPP320N20N3.

The bias circuit is sketched in Fig. 2-4. As it can be seen from this figure, same pulse generator model is used to drive both circuits.

2.4 CONVERTER SIMULATION AND ANALYSIS

2.4.1 SIMULATION

Selecting the appropriate topology according to the target application and the design criteria for component selection are thoroughly discussed in chapter three and four, respectively. The aim of this part is to evaluate the operation of GaN switches in a DC/DC converter by means of simulation in LT-Spice environment. The corresponding models for the selected switches are implemented in the selected half-bridge topology shown in Fig. 2-5 and the circuit is operated at two different switching frequencies (*i.e.* 20 kHz and 200 kHz). 20 kHz is chosen as a typical value for automotive DC/DC converter (5-50 kHz) while 200 kHz is well above this range yet still not too high to drop

the efficiency to less than 80%. To distinguish the influence of switching frequency on the size of passive components, the final equations used to calculate the required values based on the design specifications are provided below:

$$L_{min}=\max\left\{\frac{V_o}{\Delta I_{Lp.u} f_{sw} I_o} D_{1HB}(1\text{-}D_{1HB})^2,\ \frac{V_o}{\Delta I_{Lp.u} f_{sw} I_o} D_{2HB}{}^2(1\text{-}D_{2HB})\right\} \tag{2-8}$$

$$C_{o\text{-}min}=\frac{I_o D_{1HB}}{f_{sw}\Delta V_{o\ p.u}} \tag{2-9}$$

The converter is designed to work in boost mode at 12 V, 2 A input and 24 V, 1 A output. Maximum input voltage ripple ($V_{in\ p.u}$) and maximum output voltage ripple ($V_{o\ p.u}$) are limited to 5% and the maximum ripple of inductor current ($I_{Lp.u}$) is 30% in the designed converter. D_{1HB} and D_{2HB} are the duty cycle of boost and buck operations, respectively (which are both equal to 0.5). [17]

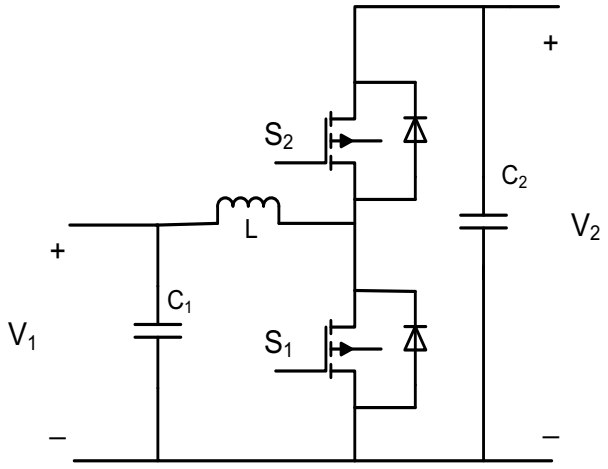

Fig. 2-5 Basic topology of half-bridge converter.

At 20 kHz, required inductor size to satisfy the aforementioned conditions is higher than 500 μH.

$$L_{min}= \frac{24}{0.3\times 20\times 10^{3}\times 1}\times 0.5^{3}=500\times 10^{-6}\ \mu H$$

A 560 μH inductor with equivalent series resistances (ESR) of 125 mΩ is selected, which would require 670 mm^2 of the PCB area. At 200 kHz of switching frequency the required value could decrease down to 50 μH, while maintaining the converter's operation in the continuous conduction mode with 30% current ripple.

$$L_{min}= \frac{24}{0.3\times 200\times 10^{3}\times 1}\times 0.5^{3}=50\times 10^{-6}\ \mu H$$

Among the possible choices, a 55 μH inductor with 17 mΩ ESR is selected. The PCB area is reduced to 425 mm^2, whereas lower equivalent series resistance would result in lower power loss in the inductor. The detailed information of the selected inductors is provided in Table 2-2.

Table 2-2 Specifications of selected inductors at two switching frequencies.

Switching frequency	Inductor (μH)	ESR (mΩ)	Part number	Size on PCB (mm^2)
20 kHz	560	125	1140-561K-RC	669.6 [19]
200 kHz	55	17	PE-92116	424.02 [20]

Other important parameter which can be significantly modified at higher switching frequencies is the value of output capacitor. Here, the characteristics of the respectively selected capacitors for the two different switching frequencies are compared with each other. The detailed assessment can be found in Table 2-3. As expected, higher switching frequency results in lower capacitor size, while the required ESR of the capacitor would not change.

Table 2-3 Specifications of selected output capacitors at two switching frequencies.

Switching frequency	Capacitance μF	ESR (mΩ)	Part number	Size on PCB (mm^2)
20kHz	1000	40	SLPX103M063E9P3	1256.63 [21]
200kHz	800	40	B41607A8807M002	706.85 [22]

Current ripple and switching frequency can be related by means of equation 2-11 [18]:

$$\Delta I_L = \frac{V_L \times D}{f_s \times L} \tag{2-10}$$

Therefore with the same duty cycle, inductor value and voltage across the inductor, higher switching frequency means lower current ripple, which would result in lower inductor impedance and decrease the power loss. However, the inductor should be selected to be able to operate at the target higher switching frequency to avoid exceeding the maximum core loss and saturation.

2.4.2 EFFICIENCY ANALYSIS

With the aforementioned design rule of 30% inductor current ripple and assuming the same values for the passive components for both converters implemented in Si and GaN semiconductor technologies, simulation tests are performed at two switching frequencies (*i.e.* 20 kHz and 200 kHz), while the output current varies between 200 mA to 600 mA. The variations of efficiency with respect to the load current are sketched in Fig. 2-5 and Fig. 2-6 for two switching frequencies.

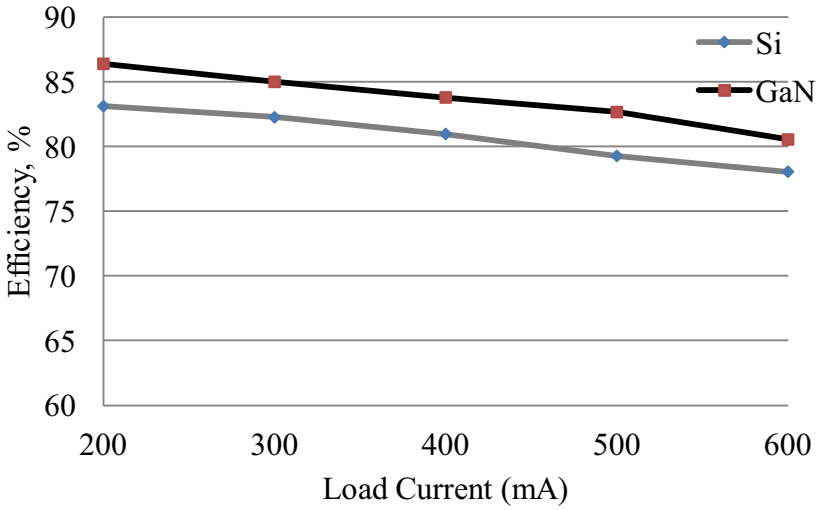

Fig. 2-6 Efficiency vs. load current at 20 kHz.

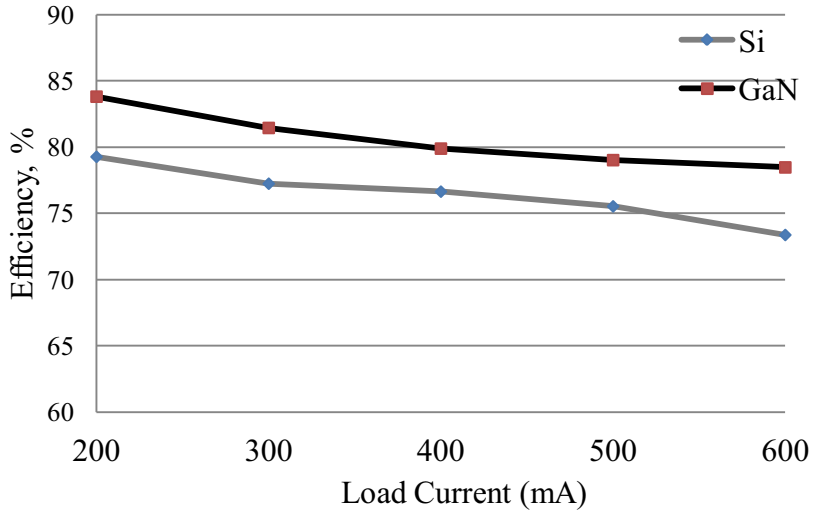

Fig. 2-7 Efficiency vs. load current at 200 kHz.

It is worth mentioning that efficiency has been calculated as the ratio between output and input powers, while all the passive components are modeled with their respective ESRs. As expected, with higher output current the efficiency will decrease due to higher conduction loss of the switches and ohmic loss of passive components. This

happens while the efficiency of the GaN-based converter still is as high as 86%, around four percent higher than the value for Si-based converter at the same output current, 200 mA.

Another way to analyze the performance of two converters is to compare the efficiency at different duty cycles. Because of the right hand side zero in transfer function of boost converter operating in CCM, duty cycle should not be increased more than 0.6 for stability reasons. Figure 2-8 illustrates this comparison. Since the on-resistance of two switch technologies are very close to each other, majority of the difference between efficiencies come from difference between switching losses. Output current is kept constant throughout this step at 200 mA. As it was expected, GaN converter shows higher efficiency all over the duty cycle range.

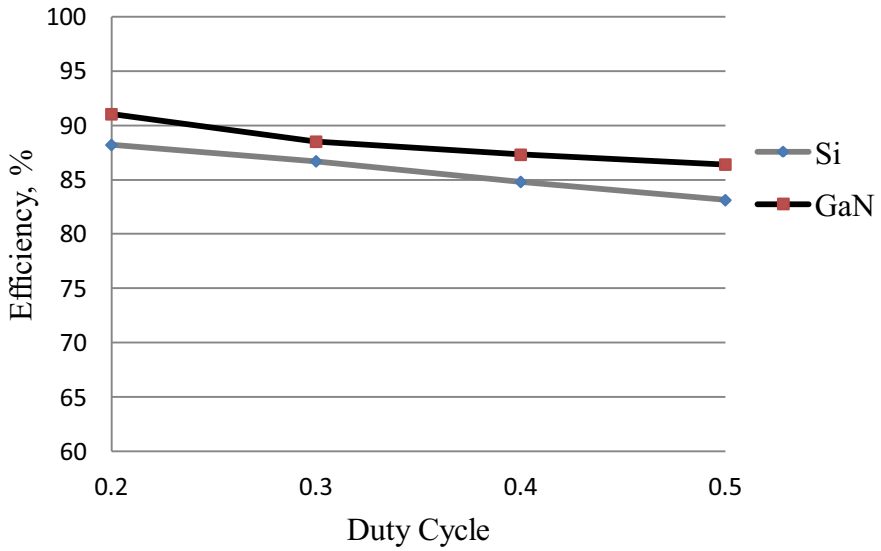

Fig. 2-8 Efficiency vs. duty cycle at 20 kHz.

CHAPTER 3

HYBRID ENERGY STORAGE SYSTEM

3.1 INTRODUCTION

Using the combination of different energy storage systems including batteries and ultra capacitors can reduce the cost and improve the performance of hybrid electric vehicles [23]. Different voltage levels and dynamic characteristics of energy storage systems necessitate the incorporation of power converters into the vehicle's energy management system. Controlling the required net energy, sizing the storage sources, establishing the power split between them and interfacing all energy systems are among the most important challenges in designing the energy management system of a vehicle. Bi-directional DC/DC converters are indispensable parts of this system as they enable the energy capture of regenerative braking to be utilized back into the primary energy sources.

This chapter starts with discussing different hybrid energy storage system configurations. Next, various bi-directional DC/DC converter topologies are compared with each other, followed by discussing some of the design considerations regarding these converters. Control strategies of these converters with the aim of achieving high-efficiency operation of each power source and average power demand, is the topic of the next part of the chapter. Finally, based on the advantages offered by implementing GaN switches, a system with a fuzzy-logic based control strategy is proposed.

3.2 HYBRID ENERGY STORAGE SYSTEMS

Complementary characteristics of batteries and ultra capacitors make them attractive for a hybrid energy storage system. While batteries have been widely used as the main energy storage system over the years, some disadvantages prevent them to be the sole storage system in a vehicle. Higher power density of a battery comes with the significant increase in its cost and more complicated thermal management. Furthermore, rapid changes in load according to driver's act in a vehicle, causes rapid charge and discharge in the battery, which reduces its life time. Another problem is balancing of battery cells which are required in order to increase the capacity of the total system. Without this, each cell might fail after some time resulting in the failure of the total system [24].

To solve the aforementioned problems, hybrid energy storage systems are developed. In these systems a battery pack is joined with an ultra capacitor unit. Unlike batteries, ultra capacitors have high power densities while their energy density is low. In other words, delivering high power values in short time can damage the battery while ultra capacitor can easily be charged or discharged in short periods of time. Therefore, ultra capacitors can be adjusted to deliver and absorb the power peaks during fast accelerations and regenerative breakings of vehicle's operation. This can effectively lead to longer life for the battery. In addition, ultra capacitors can operate in wider temperature range than batteries, which provides the opportunity for reducing the power demand from the batteries in the extreme temperature situations. Table 3-1 compares the general characteristics of a typical state of the art lead acid battery with an ultra capacitor [25].

Table 3-1 Battery and ultra capacitor characteristics [25].

Chemistry	Nominal Voltage (V)	Energy Density (Wh/kg)	Power Density (kW/kg)	Cycle life (Times)
Lead Acid Battery	2	30-40	0.18	Up to 800
Ultra Capacitor	2.5/2.7	2-10	4-10	Over 1,000,000

Several topologies have been proposed to optimally integrate ultra capacitors into the energy storage systems [26], including the one in Fig. 3-1. The two sources can be directly connected in parallel. This forces the voltages of two sources to be equal which limits the power delivered from the ultra capacitors. This topology is shown in Fig. 3-1.

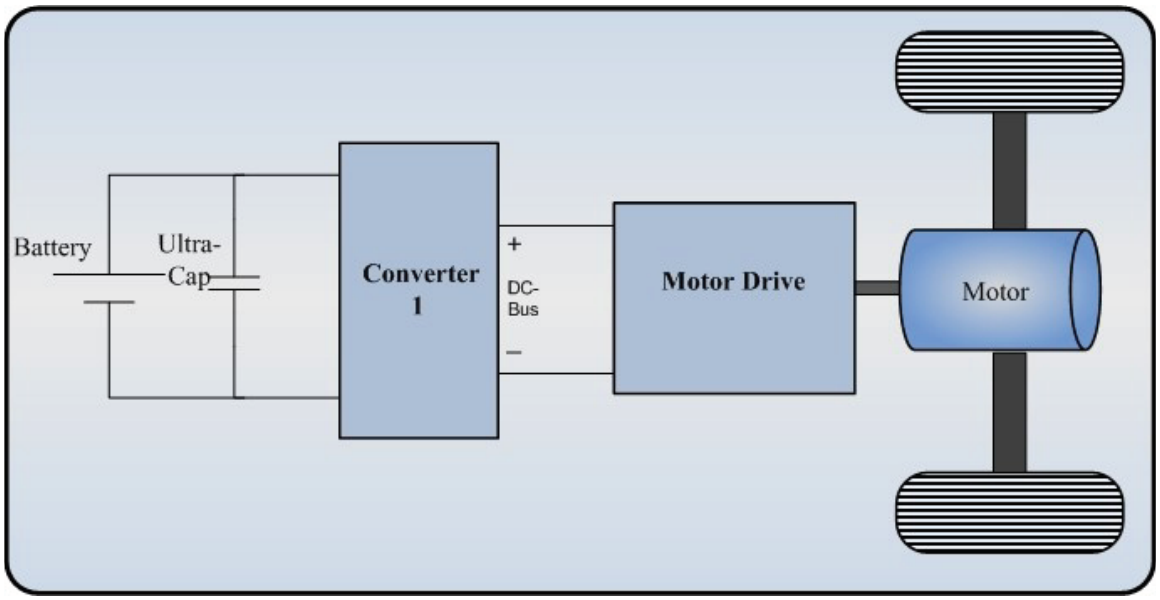

Fig. 3-1 Parallel connection topology.

The proposed system by Ortuzar *et al.* [27], presented in Fig. 3-2, implements the bi-directional converter between the two sources. Here, the battery is connected directly to the DC bus. As a result, voltage of the ultra capacitor can be lower and varied in a wider range. Disadvantages of this design include the fact that the energy derived from regenerative braking cannot be absorbed only by ultra capacitor, as it is originally intended.

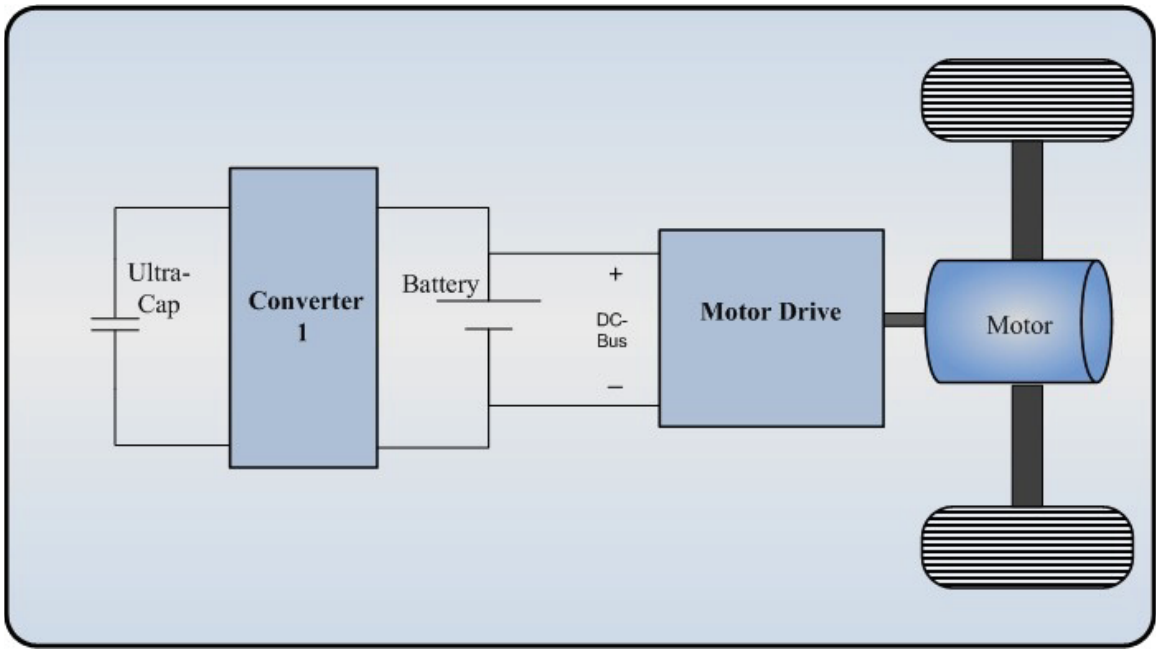

Fig. 3-2 Ultra capacitor/Battery configuration.

By changing the position of battery and ultra capacitor, configuration illustrated in Fig. 3-3 is created [28], [29]. Lower battery size in this topology is advantageous. However, to enhance the operating range of both battery and ultra capacitor another bi-directional converter can be placed between the ultra capacitor and DC link. This configuration has been sketched in Fig. 3-4. This configuration is called cascaded [25].

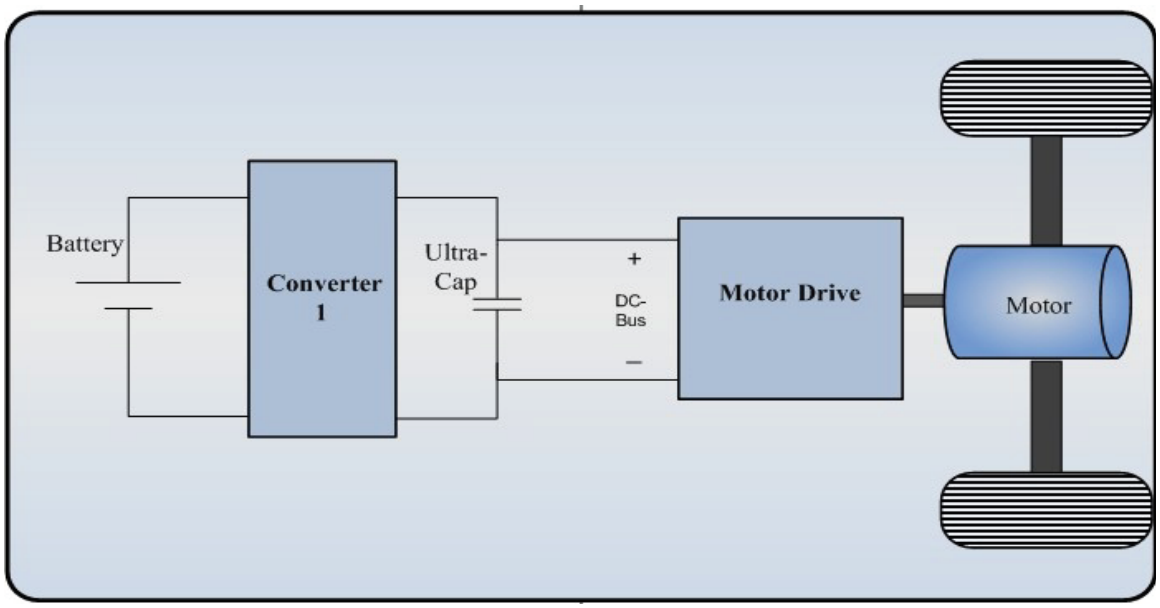

Fig. 3-3 Battery/Ultra capacitor configuration.

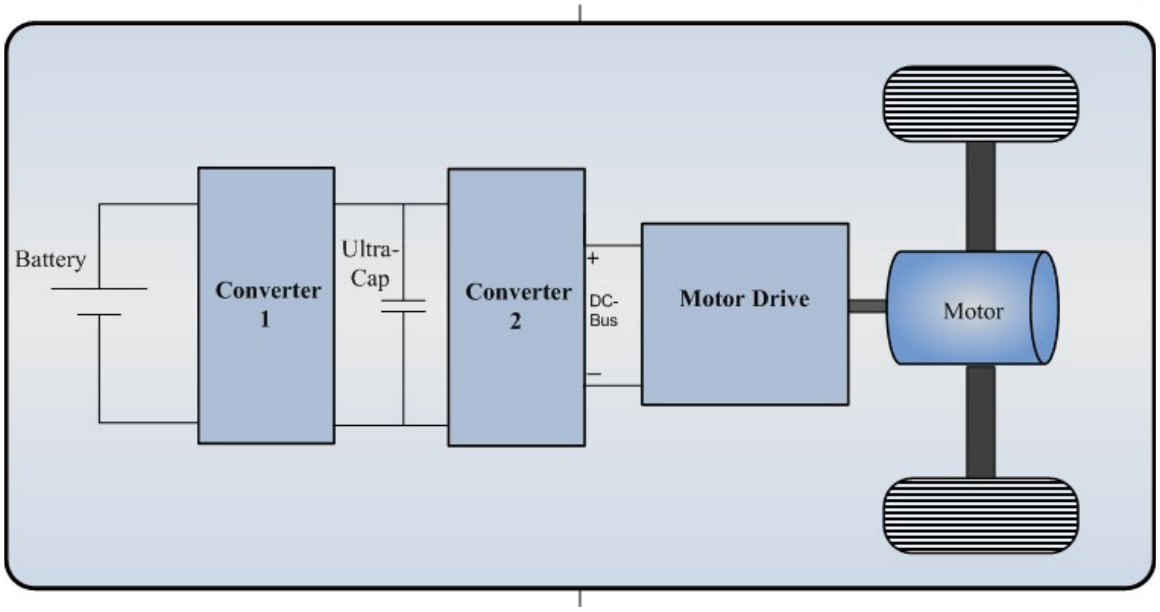

Fig. 3-4 Cascaded connection.

To control the stress on the battery it is preferred to put the battery on the input of converter 1. The bus voltage is controlled by the state of the charge (SOC) parameter of the ultra capacitor, which causes large voltage fluctuations on the input of converter 2. SOC is one of the states of the system, which is complicated to accurately measure.

Several techniques have been developed to estimate the SOC. However, many of them are proved to be either impractical or not accurate enough, which makes the SOC not the best parameter to be used for controlling the energy flow of the system [24].

Furthermore, lower SOC values would introduce higher input current into the second converter, which results in high power losses. To improve the controllability of the system, ‘‘multiple-converter’’ topologies are proposed [30]. The schematic of a multiple-converter topology is shown in Fig. 3-5. Energy management algorithm will determine the required supply of each source based on the state of them and the required motor power. Converter connected to the battery is current-controlled and the one for the ultra capacitor is voltage-controlled. The disadvantage of the last two configurations is the need for two bi-directional converters, which increases the cost and size of the system.

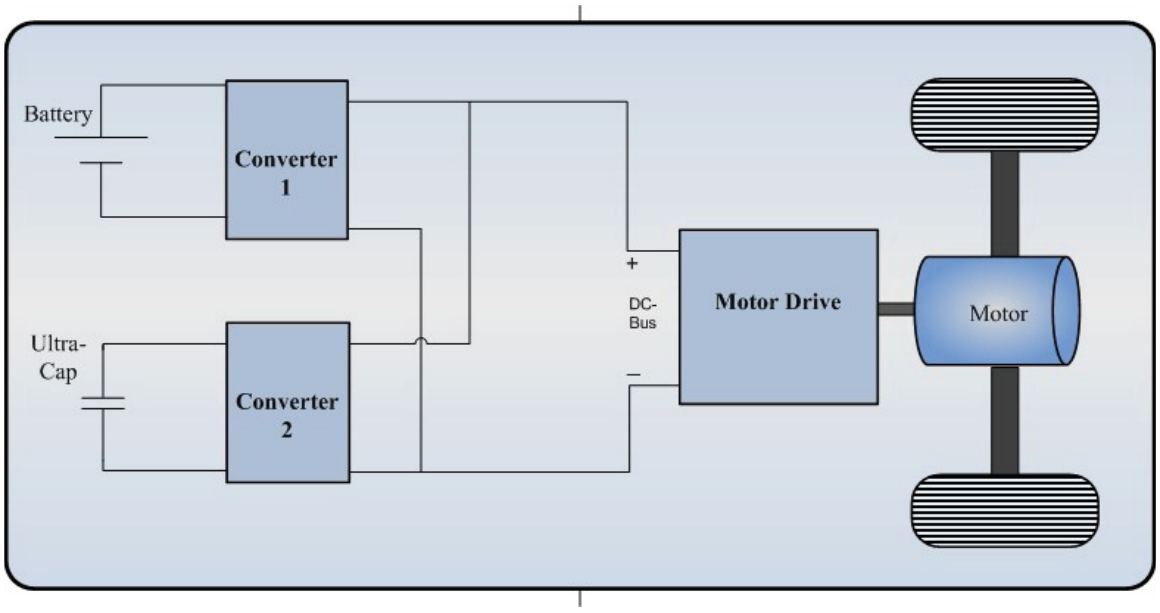

Fig. 3-5 Multiple converters configuration.

To solve this, instead of using two bi-directional converters, multiple input topologies are developed [31]. The system diagram is shown in Fig. 3-6. While these

topologies require lower number of components, they suffer from lower efficiencies and complicated control strategies.

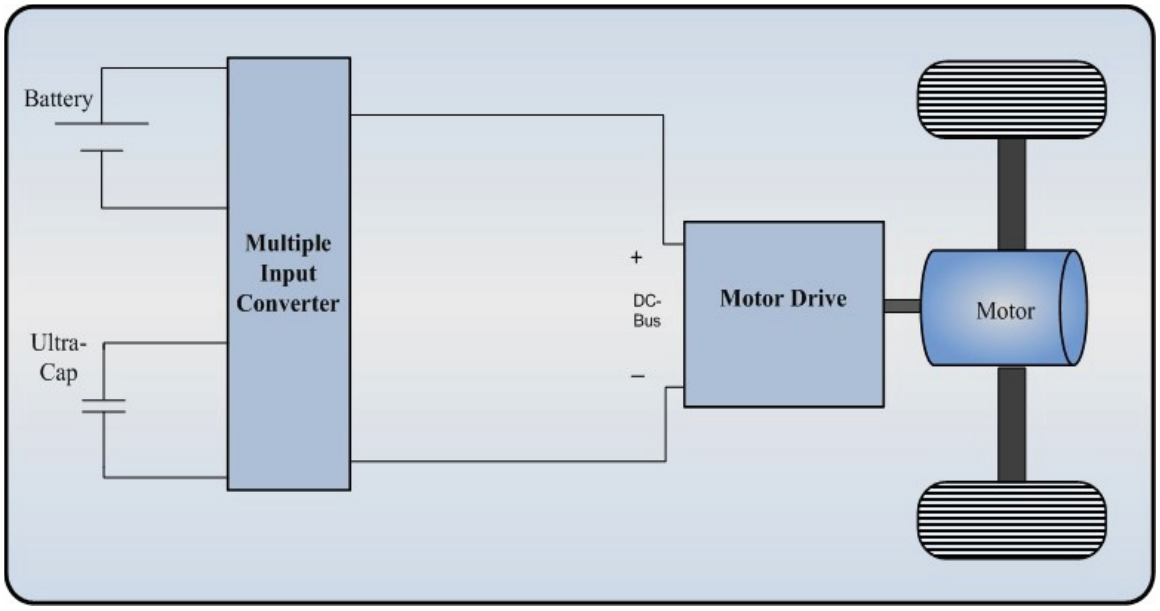

Fig. 3-6 Multiple input converter configuration.

Bi-directional DC/DC converters are basic units of all of the suggested configurations. In the next section, different circuit topologies of these converters are presented and compared to each other. Reaching higher conversion efficiencies and smaller sizes in these converters can tremendously benefit overall performance of the drive system of the vehicle.

3.3 NON-ISOLATED BI-DIRECTIONAL DC/DC CONVERTERS

General non-isolated bi-directional DC/DC converters including half-bridge, Sepic/Lou, Cuk and cascaded half-bridge are classified and their performances have been compared by Schupbach *et al.* [17]. Interleaved structure has also been suggested in this regard mainly for minimization of the current ripple and reduction of the magnetic component size [32]. With the same power rating, it has been shown that Cuk and

Sepic/Lou converters need two larger inductors and one more capacitor compared to half-bridge resulting in additional power consumption. As for the current stress on active switches and diodes, the value again is higher in Cuk and Sepic/Lou compared to half-bridge. Therefore, half-bridge has gained more popularity among these topologies due to its higher efficiency and less number of passive components. However, all of these topologies are implementing conventional hard-switching technique leading to significant switching losses and limited efficiencies.

Soft switching methods are developed to solve this issue throughout the years and many topologies have been proposed [33]-[34]. Among these, the topology proposed in [34] suffers from high voltage ripples, while it also cannot handle a wide variety of input voltage range. In [34], a bi-directional quasi resonant converter is developed, specifically for battery equalization applications. Major problem of this type of converter is the high voltage stress on the power switches. The switched capacitor DC/DC converters with smaller size and lighter weight have also been offered, consisting of only MOSFETs and capacitors, with no magnetic component. Evidently they experience high switching losses due to hard switching scheme. To overcome this, Quasi-resonant converters with zero-current or zero-voltage switching (ZCS or ZVS) have been proposed. Despite, low current stress and balanced resonant current advantages of these converters their fixed voltage transfer ratio between input and output results in poor dynamic response [35]. Soft switching in any of these converters comes with complexity, additional circuit components and higher cost.

As discussed in previous chapter, GaN-based high electron mobility power switches offer higher switching speed while staying competitive with regular Si switches

in terms of on-resistance. Introducing these switches into power management system of vehicles, brings about the possibility of going back to conventional converter topologies with hard switching scheme. In hard switching, high switching losses due to generally slow switching of power devices limits the key power conversion figure of merit (FOM), efficiency × density/cost. However, faster switching of GaN switches offers lower switching losses and therefore improved efficiency. This would add to the superior high temperature performance of GaN switches compared to Si, which has previously been discussed in chapter one.

3.4 DESIGN CONSIDERATIONS

3.4.1 NOMINAL VOLTAGE OF ENERGY SOURCES

Selecting one of the mentioned topologies for power management system of a vehicle massively depends on the properties of the used energy sources. Connecting the battery directly to the DC bus means higher voltage rating for the battery compared to ultra capacitor, while it also necessitates the high power converter to fully utilize the high power density capability of the ultra capacitor. For lower battery voltage values, battery pack can be connected to the DC bus and also the ultra capacitor via a DC/DC converter. Here, with lower battery voltages, balancing is less of an issue. By means of using two different converters, however, the opportunity of choosing lower ratings for both battery and ultra capacitor will be offered. In this case, higher cost, bigger size and possibly lower conversion efficiencies will be presented to the system. To summarize, the voltage strategy of the used sources will significantly define the configuration of the management system.

3.4.2 INDUCTOR SIZING

The most bulky component of a DC/DC converter is the inductor. Switching frequency of the converter and current ripple percentage are the two important parameters in defining the size of the inductor. According to a general rule of thumb in automotive application, current ripple is usually chosen to be limited to 30% [1]. On the other hand, higher switching frequencies limit the converter efficiency due to increasing switching losses of the semiconductor devices. Faster switching potential of GaN switches can support the idea of using higher switching frequencies, which can effectively decrease the size of the inductor. It should also be noted that the DC resistance of inductors decreases as the frequency increases. This is due to less copper length needed for fewer turns. Therefore GaN switches are expected to provide the future path for lowering the inductor sizes. This fact was confirmed by simulation in chapter two and will be experimentally evaluated in the next chapter.

3.4.3 ISOLATION ISSUE

Isolation between input and output of a converter is needed when there is a high ratio between high side and low side voltages [36]. In this situation, it is not economical for the devices to handle high voltage and high current at the same time. Therefore, isolation should be provided by means of a transformer between input and output of the converter. However, in the automotive power management typically this ratio is not high enough to demand the isolation.

3.5 CONTROL STRATEGY

3.5.1 OVERVIEW

After selecting the proper configuration to integrate different energy sources into the system, the next step would be controlling the net energy distribution between them. Certain set of rules should be established before designing the controller of the power management system. These rules are generally created based on the characteristics of the sources, which were mentioned earlier in this chapter. The state of the charge (SOC) of battery and ultra capacitor determines whether they should be in charging or discharging modes. The DC bus voltage needs to remain constant, while the currents of both sources should be controlled within the proper range. More importantly, fast charging or discharging currents generated during acceleration and braking of the vehicle has to be initially provided or absorbed by the ultra capacitor. These conditions must be satisfied, while the adequate amount of energy is supplied for vehicle's standard operation.

In recent years, several strategies have been proposed in literature to reach better overall performance of the system [37]-[47]. Some of them use classic inner loop current and outer loop voltage controller [37]-[38], [24], in which the nonlinear characteristics of the battery have been ignored. A typical configuration which is designed for the topology of Fig. 3-5 is developed in [24]. First step is to control the input current of the each converter followed by controlling the output voltage. The ultra capacitor converter input current reference is used to regulate the output voltage of the converter. The reason of choosing ultra capacitor current is its fast response, which would result in stable output voltage. Also, as mentioned earlier, fast changes in battery current should be avoided to increase its lifetime. Therefore, to supply the load with fast variations in voltage, the

current of ultra capacitor would be the more appropriate parameter. Resistive load has been used in the experimental set up, which could not confirm the ability of controller in regenerative mode of operation. Furthermore, this controller has not been tested with a typical driving cycle.

Methods such as neural network have also been employed by a number of authors to find the highest efficiency condition [27], [39]. In [27], a heuristic algorithm has been compared with a proposed optimized controller using neural network. Heuristic algorithm follows two basic rules:

1) Ultra capacitor energy in inversely proportional to vehicle's speed.
2) Current going through or coming from the battery should be limited.

In the proposed neural network optimization technique, power increase (in kilowatts) and the energy efficiency increase (in kilo-meter per kilo-watt-hour) are chosen as the optimized variables. Due to having different power demand situations in vehicle's drive cycle, selecting the proper variables in these methods is a challenge, which may result in a non-optimal energy distribution. However, compared to the heuristic algorithm, optimized method has resulted in superior performance of the system in terms of kilo-meter per kilo-watt-hour parameter, while absorbing the regenerative currents by ultra capacitor would result in longer battery life.

Fuzzy logic based strategies have been developed and proved to be effective and practical in complex drive cycles [40]-[42]. This is mainly because they do not need a precise model of the system and they are based on the designer's knowledge. In [40], the proposed strategy uses required power, the SOC of battery and the SOC of ultra capacitor

as the input to fuzzy logic based controller. By using fuzzy logic, the required power will be distributed into battery and ultra-capacitor based on the following rules:

1) When the vehicle starts or accelerates, battery and ultra capacitor supply the motor.
2) When it operates at normal condition, due to decreased power demand, only battery would provide the energy.
3) The energy produced by regenerative braking initially being absorbed by ultra capacitor and the extra energy, if any, will charge the battery.

The general schematic is shown in Fig. 3-7. The output parameter is defined as K_{bat}, which is the ratio of the battery energy to the total required energy. The membership functions of the fuzzy parameters are defined with Gaussian distribution. Simulation is done in ADVISOR 2002 software and the results are compared to the previously proposed logic threshold strategy. Battery current is reduced and therefore it has been concluded that the method can increase the battery life time. However, there is no experimental test performed to confirm the capability of the controller.

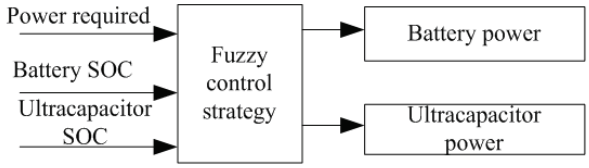

Fig. 3-7 Schematic of the control strategy in [41].

Another fuzzy logic based control strategy is proposed in [43] by Yifeng *et al*. Here, the battery SOC and desired vehicle power P_1 are inputs and desired battery power P_2 is the output parameter. Three membership conditions are defined for each of the parameters, which include, low (L), medium (M) and high (H). Fuzzy rules are presented

in IF-THEN format. The difference here is that the genetic algorithm is implemented to optimize the membership functions of the original fuzzy logic controller. The simulation has been done in ADVISOR and the results are claimed to keep the SOC balance and improve the fuel economy. Again, there is no presented experimental test to practically verify the results.

Rosario and Luk in [44], proposed another fuzzy logic based control strategy which uses the vehicle speed and ultra capacitor SOC as the input with three regular membership functions. The output parameter is battery power. Two rules are applied in this method:

1) At higher vehicle speeds, the ultra capacitor SOC reference would be lower.
2) With higher deviation of ultra capacitor actual SOC from the reference SOC, the battery maximum power would be higher.

The modular structure proposed in this work contains following hierarchical shells: energy management shell which generates orders to the power management shell in which the instruction for power electronics shell is produced. The energy management shell, as mentioned, implements fuzzy logic strategy. The simulation as well as experimental test has proved the effective act of the proposed system. However, no comparison has been made with the other similar reports in literature.

Baisden and Emadi in [45] established a control strategy according to the operating modes of a DC/DC converter to determine the power split between an ultra capacitor bank and battery. The proposed system has decreased the cost by lowering the size of the battery to 70%. Due to the decreased output current, the battery's life is improved, which justifies the addition of ultra capacitor cells.

3.5.2 PROPOSED STRATEGY

In this thesis, a novel rule-based control strategy is developed. Battery/ultra capacitor configuration sketched in Fig. 3-3 with half-bridge topology has been chosen due to lower battery size and number of converters. Three main rules are:

1) Rate of the change of current supplied by the battery will be limited to the safe value.
2) Ultra capacitor's energy should always remain higher than 0.4 per unit (p.u). This is due to the fact that ultra capacitor should always be ready to inject required current during fast accelerations. The ultra capacitor's per unit energy can be calculated by:

$$E_{UC}(t)=\frac{[v_{UC}(t)+ R_{UC}.i_{UC}(t)]^2- V^2_{minUC}}{V^2_{maxUC}} \quad (3\text{-}1)$$

where:

R_{UC} : internal UC resistance

V_{minUC} : minimum UC voltage

V_{maxUC} : maximum UC voltage

The output voltage of the converter should remain constant, while the battery is the only source of energy. In cases that the ultra capacitor provides the rest of the energy, the output voltage drop should not be more than 20%. This is because the two terminals of the dc bus are generally connected to the inverter of a typical ac motor drive in which the input voltage variations should be limited to less than 20%.

A current source is used to model the load which reflects the input current of an ac motor drive for a typical drive cycle. Controller works in two modes: while the output current is constant, the battery would supply the load through the converter, therefore the

output voltage should remain constant. The transient variations of battery's current should still be limited and this necessitates the need for an inner loop controller in this mode. The general outlines of the control strategy and the control flowchart have been sketched in Fig. 3-8 and Fig. 3-9. When the output current is not constant, a limiter will limit the output current and generate the reference for the battery's current. The rest would be supplied by the ultra capacitor, which will be discharged. Therefore, the DC bus voltage will drop. This trend will continue until the out voltage drops more than 20% or the ultra capacitor's energy decreases to lower than 0.4 p.u. In these cases, the battery should supply the load and charge the ultra capacitor back to the proper range.

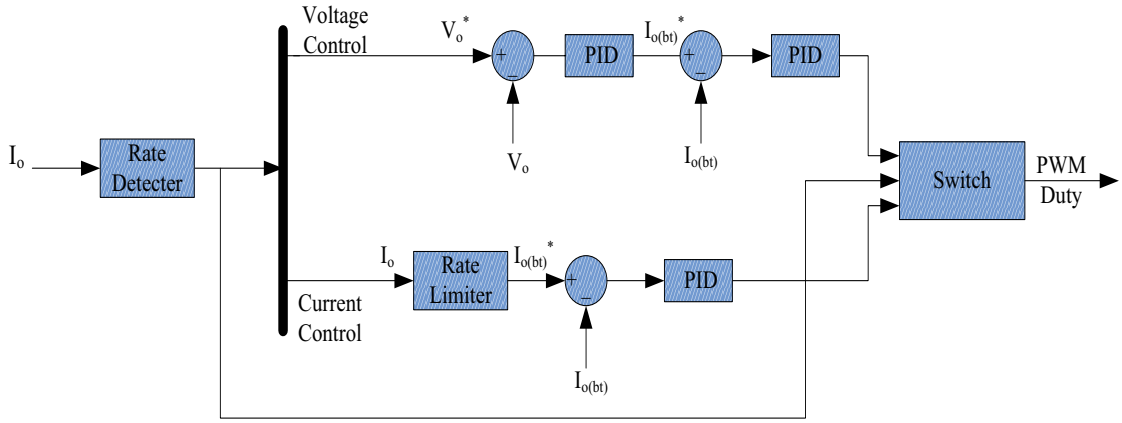

Fig. 3-8 Proposed power management system.

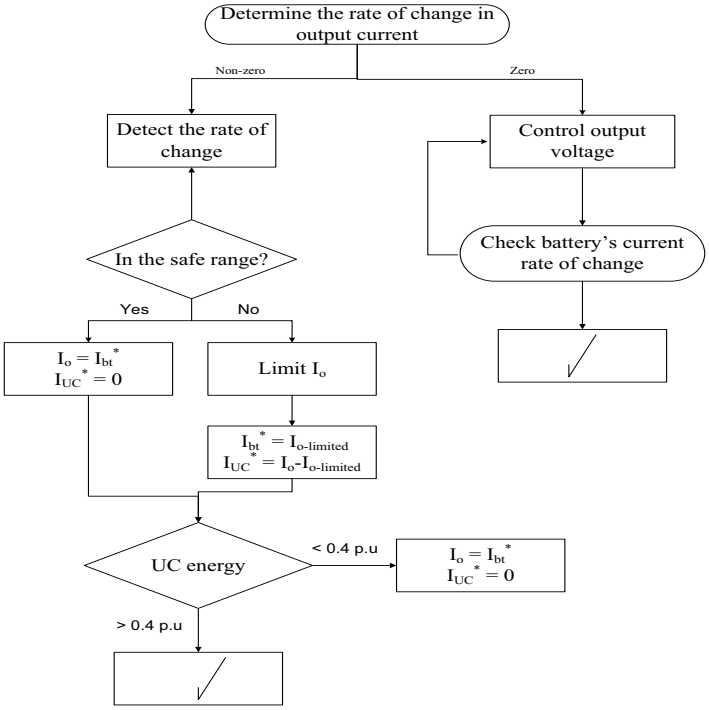

Fig. 3-9 Control flowchart.

To test the controller, a variable current source which characterizes the load estimation corresponding to the typical test drive cycle, in this case ECE 15 urban cycle [46], is used as the load and connected to the dc bus. It simulates a 4,052 m of European urban trip at an average speed of 18.7 km/h. The drive cycle is sketched in Fig. 3-9.

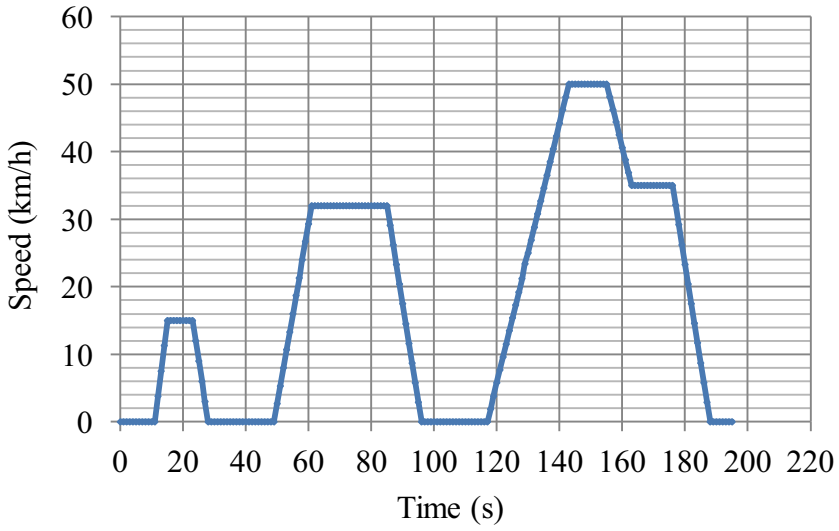

Fig. 3-10 Test drive cycle based of European ECE-15 standard.

The reason of using PID controllers instead of regular PI is to improve the transient performance of the controllers mainly because of constant change between the mentioned two control modes. Without the derivative part, the change from one mode to another may result in significant output voltage drop, which is not acceptable from the drive point of view.

3.5.3 PARAMETERS AND MODELS OF CONVERTER AND SOURCES

The complete converter circuit with two sources and the load is shown in Fig. 3-10. The system is simulated in Matlab Simulink environment. Matlab's battery model is employed to simulate the battery, while the ultra capacitor is modeled with a simple capacitor in series with the equivalent resistance. The detailed specifications of the sources are provided in Table 3-2. These ratings for the sources are selected based on the chosen load current. The converter is designed based on the 12 V, 8 A input, which will be converted to 24 V, 4 A at 2 kHz switching frequency. The converter design procedure is the same as the developed process in chapter four. Therefore to evaluate the effectiveness of the controller, the ratings for the sources should be selected as small as possible. Battery's equivalent circuit from Matlab Simulink is shown in Fig. 3-11. The dynamic behavior of the power sources and load can be represented by the equivalent circuit of Fig. 3-12.

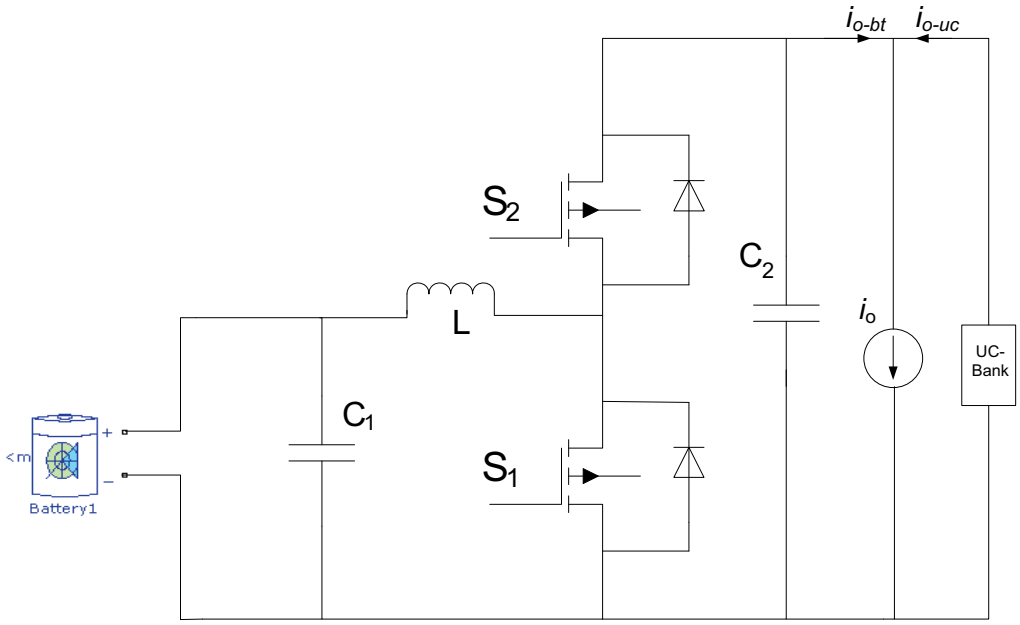

Fig. 3-11 Converter topology.

Table 3-2 Battery and ultra capacitor ratings.

Power source	Voltage(V)	ESR (Ω)	Capacitance (F)	Rated Capacity (Ah)
Battery	12	0.06	-	2
Ultra capacitor	24	0.5	0.38	-

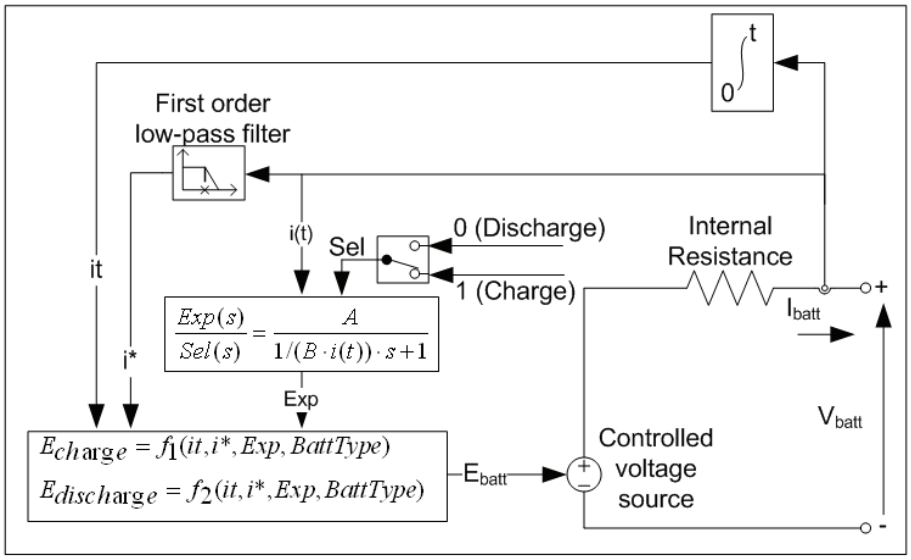

Fig. 3-12 Equivalent circuit of the battery.

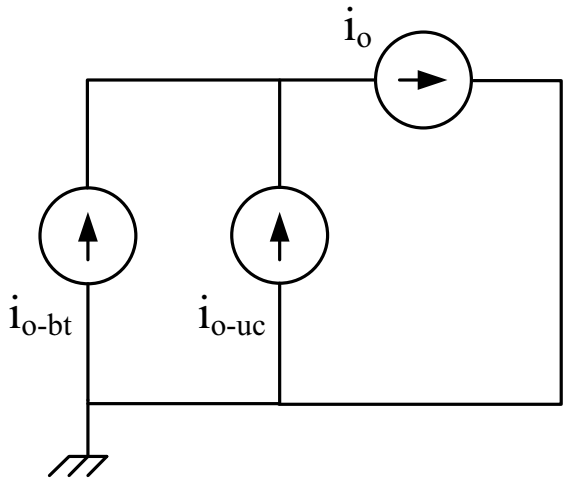

Fig. 3-13 Equivalent circuit of power sources.

As can be seen from the figure, the ultra capacitor's current can be written as (3-2), which means that whenever the conditions call for, the ultra capacitor will provide the difference between the load current and the safe battery current.

$$I_{o\text{-}uc}=I_o- I_{o\text{-}bt} \tag{3-2}$$

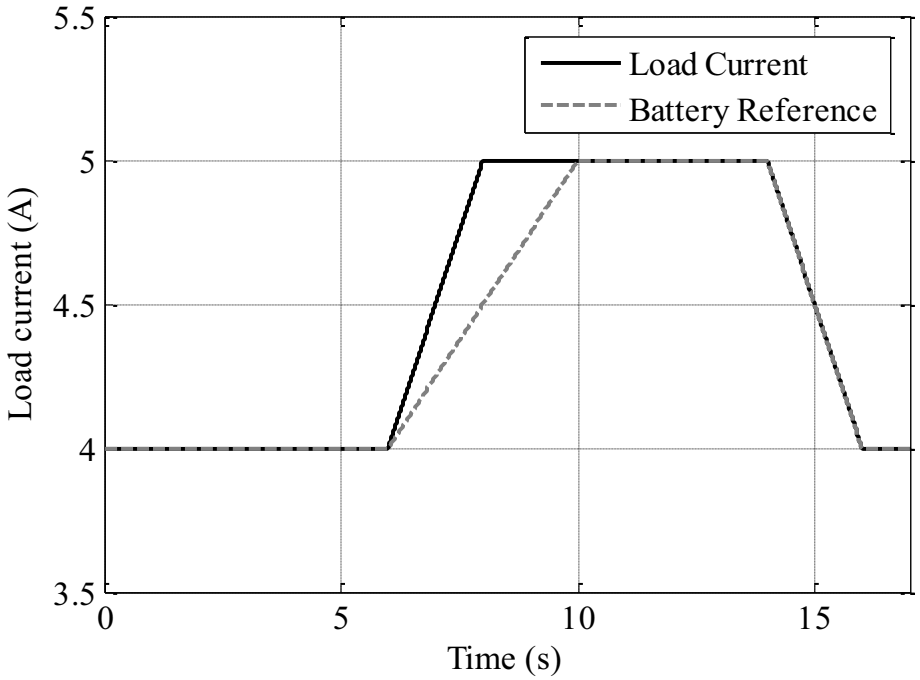

Fig. 3-14 Variation of output current and generated battery's reference current in a cycle.

A typical variation of output current and the reference generated from it for battery's current is shown in Fig. 3-12.

3.5.4 CONTROLLER DESIGN

As discussed before, controllers for two different modes of operation should be designed. During the constant load current period, the dc bus voltage should remain constant. Small signal analysis of this mode of operation will result in the following transfer function which will be used for controller design [18]:

$$\frac{V_o(s)}{d(s)} = G_{do} \frac{\left(1+\frac{s}{w_{z1}}\right).\left(1-\frac{s}{w_{RHP\text{-}zero}}\right)}{1+\frac{s}{w_0.Q}+\frac{s^2}{w_0^2}} \tag{3-3}$$

where:

$$G_{do}=\frac{V_{in}}{(1-D)^2}$$

$$w_{z1}=\frac{1}{r_C.C}$$

$$w_{RHP\text{-}zero}=\frac{(1-D)^2.(R-r_L)}{L}$$

$$w_0=\frac{1}{\sqrt{L.C}}.\sqrt{\frac{r_L+(1-D)^2.R}{R}}$$

$$Q=\frac{w_0}{\frac{r_L}{L}+\frac{1}{C\times(R+r_C)}}$$

r_c and r_L refer to the ESRs of the output capacitor and inductor. R is the equivalent resistance which corresponds to the output current source model. The controller is designed based on 60˚ phase margin and 4 kHz crossover frequency. The derivative part, however, are modified to reach the fastest transient response, while changing from voltage mode to current mode. Same procedure is implemented to design the current controller. According to the system specifications, transfer function of the system would be:

$$\frac{V_o(s)}{d(s)}=\frac{-86.8s^2+47566.4s+36163050}{s^2+0.35s+250} \quad (3\text{-}4)$$

Fig. 3-15 shows the bode plots of the open loop system. At the crossover frequency:

$$\emptyset(f)=-180\ ^\circ \quad (3\text{-}5)$$

Therefore, to reach 60˚ phase margin, controller should add 60˚ to the system.

Transfer function of the PID controller is defined as:

$$G_c(s)=K_P+K_D s+\frac{K_i}{S} \quad (3\text{-}6)$$

Calculated values for the controllers are provided in Table 3-3. The results of the system presented in the next section confirm the accuracy of this design.

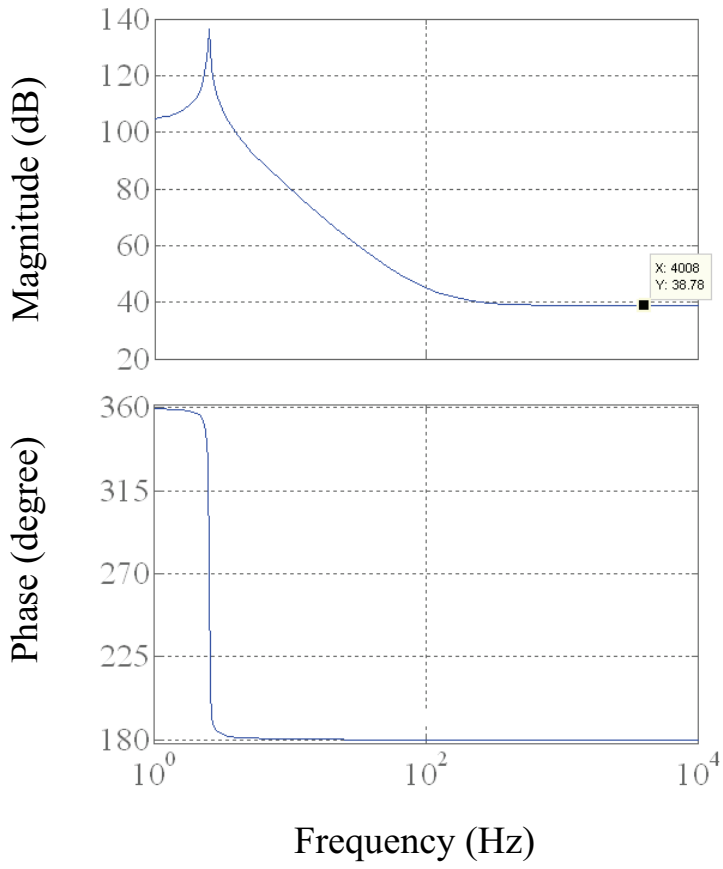

Fig. 3-15 Bode plots of the open loop system.

Table 3-3 Controller parameters.

Controller	K_p	K_D	K_i
Voltage controller 1	1.5	10^{-6}	1.2
Voltage controller 2	0.05	10^{-3}	0.5
Current controller	0.02	0.0009	0.7

3.5.5 RESULTS AND ANALYSIS

The controlled battery current and the ultra capacitor current are sketched in Fig. 3-13 and Fig 3-14 respectively. The cycle is chosen in a way to incorporate all the possible situations including constant, increasing and decreasing current with different rates. Between t = 0 s to t = 6 s, load current is constant and therefore the control system has to keep the output voltage constant. The load current will be provided by battery. From t = 6 s to t = 8 s, load current is increasing with the rate of 0.5 A/s which is higher than the safe value for the battery. Therefore the controller will limit the rate to 0.25 A/s and ultra capacitor provides the rest of the load current. From t = 8 s to t = 14 s control strategy will switch to constant voltage mode and from t = 14 s to t = 16 s current will decrease to 4 A again. The output voltage drop is limited to 20%. The variation is shown in Fig. 3-15.

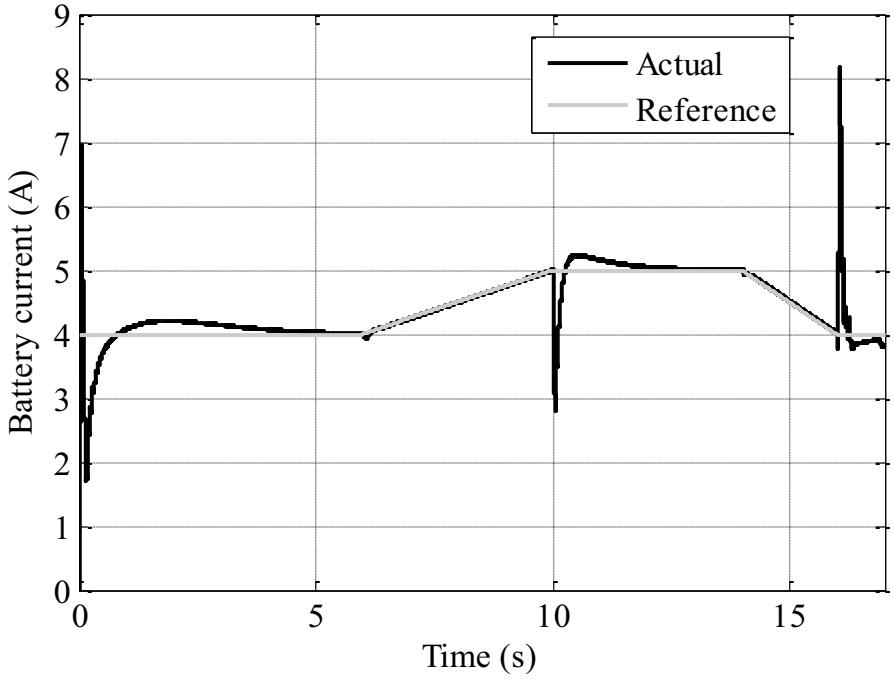

Fig. 3-16 Controlled battery current versus time.

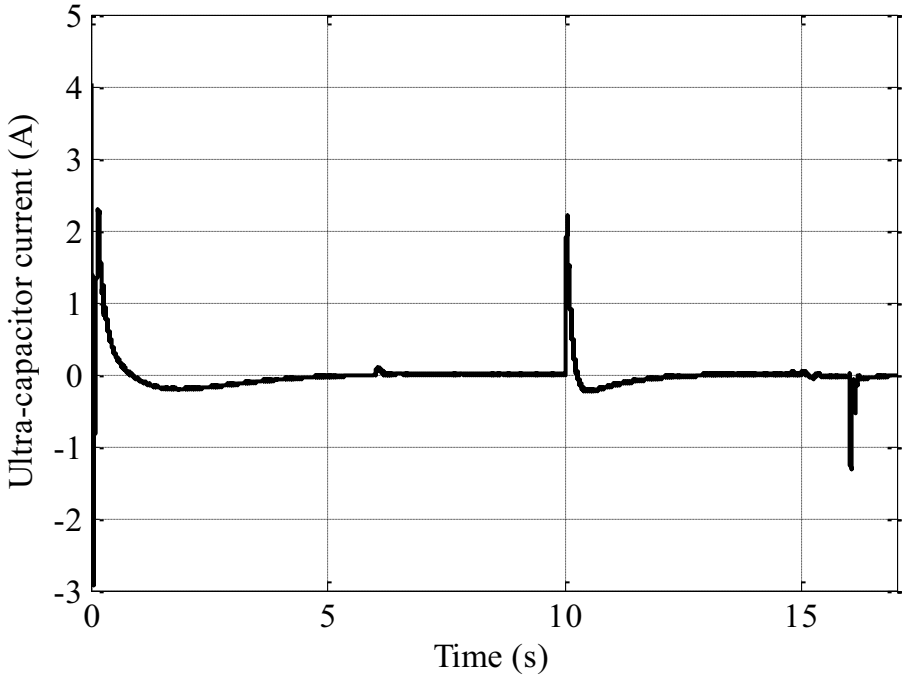

Fig. 3-17 Ultra-capacitor current versus time.

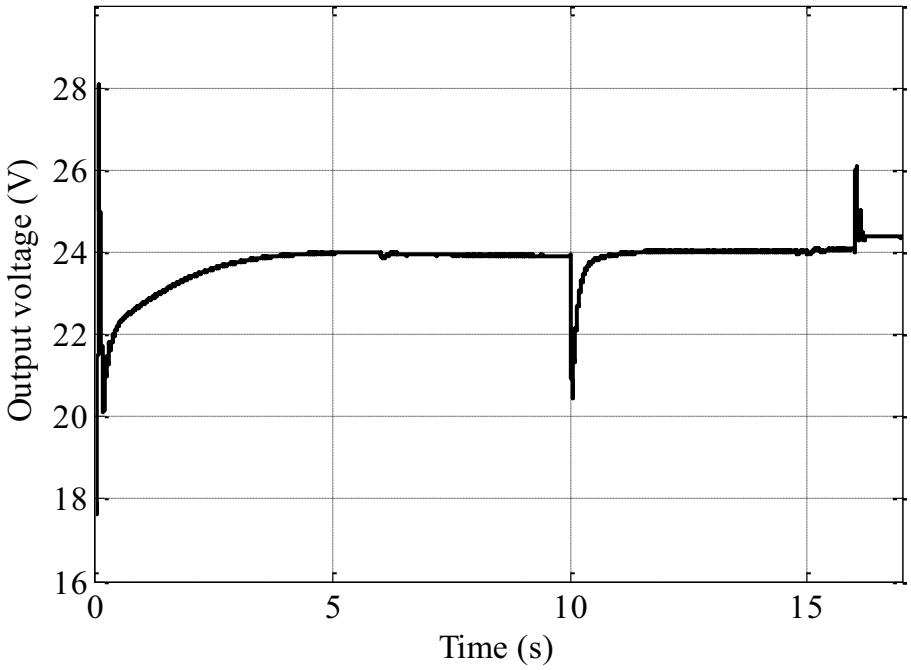

Fig. 3-18 Converter output voltage (DC-bus) versus time.

The target design specifications are reached by means of the developed strategy. The DC bus voltage is kept constant throughout the load current variation, while the supplied battery current rate is limited to the safe value. Therefore the main target which was increasing the battery life cycle will be effectively reached. As for the limitations of the strategy two main issues should be mentioned. First, is the possible non-linear behavior for the input current of the DC bus, which may change the controller parameters in the practical application. Furthermore, controllers which are designed by means of small signal analysis may not operate at different operating condition or ratings. In this case, for different operating points, different controllers should be designed and based on the conditions, the controllers should switch. Second issue could rise from the fact that the recovery of the energy as it happens in regenerative braking has not been checked with this strategy. However, since acquiring the energy from braking only depends on the operation of the converter, this would not concern the management strategy.

CHAPTER 4

DESIGN, PROTOTYPING, AND TESTING

4.1 INTRODUCTION

This chapter starts with categorizing the specific circuit design requirements in order to design the selected half-bridge DC/DC converter for the vehicle's power management system. Based on the specifications, proper values to reach the intended converter performance are chosen. Two converters with the same ratings and elements using GaN and Si switches are built and superior performance of GaN-based converter in terms of efficiency and size is experimentally confirmed. Specific considerations for driving GaN FETs are discussed followed by providing a discrete solution which is implemented later in the experimental test. While the increase in switching frequency has the potential to reduce the overall weight and size of any power electronic converter, some concerns may arise from the performance of magnetic components at higher frequencies. Finally, these effects are discussed further in this chapter.

4.2 SWITCHING POWER ELECTRONIC CONVERTER DESIGN

Generally in a switching power electronic converter, the semiconductor switches are continuously switched on and off at high frequencies (20 kHz to several MHz) to transfer electrical energy from the input to the output, through the passive components. The output voltage is controlled by varying the duty cycle, frequency or phase of the semiconductor device's transition periods. Inductor is the element which transfers power from the input to the output. Finally, closed-loop feedback should be designed to achieve

the objectives for line and load regulation and dynamic response [13]. However, before focusing on the control loop, it is necessary to study some of the available power circuit choices alongside with their respective requirements and operating rules. The general choices in design of these, are listed as follows [47]:

1) Power circuit topology
2) Control method
3) Switching frequency
4) Filter capacitor
5) Filter inductor

The first two topics were thoroughly discussed in chapter three. Having the advantages of GaN switches in mind, a half-bridge converter is believed to be the best option compared to other topologies. As for the second topic, closed-loop feedback implementing linear controllers was designed based on bode plots. Although the pulse width modulator and the switching circuit are not linear elements, however, their state-space averaged linear equivalents were used at frequencies below the switching frequency to find the necessary transfer functions. Choosing the optimum switching frequency can significantly improve the converter design in terms of size and efficiency. By raising the frequency smaller magnetic components can replace the previous components. However, above 500 kHz, core losses will rise to the point where this trend slows down and then reverses which makes the magnetic components larger. The filter capacitor can get smaller with increased frequency, however, since its impedance depends on ESR, (not the capacitance); the effect is not as dominant as expected.

Obviously, more high frequency noise and less low frequency noise will be produced at higher switching frequencies [47].

Therefore, conducted EMI is easier and less costly to filter. The main disadvantage can be summarized in terms of increased losses, which result in lower efficiency and more complicated heat removal system. Ongoing developments including new circuit topologies such as resonant converters, improved high frequency magnetic materials and faster semiconductors such as GaN might lead to better high frequency performance of switching converters in the near future.

Before selecting the circuit components including necessary filters, following specifications should be clarified:

1) Nominal input voltage
2) Minimum input voltage
3) Maximum input voltage
4) Output voltage
5) Nominal average output current
6) Nominal minimum output current
7) Maximum ripple voltage

Cost, size, efficiency and noise are the ultimate considerations in finalizing the circuit design, whereas the possible constraints on each of them might significantly change the entire process [47].

Other than these concerns, some particular challenges rising from requirements of the automotive environment should also be noted in designing a DC/DC converter for implementing in a hybrid energy storage system. First of all, limitation of low-voltage

ratings of the power sources (normally 300 V or less), cause currents in the order of hundreds of Amperes to flow into the components of the circuit, which not only increases the electric and thermal stresses in the active and passive components but also reduces the converter efficiency. Furthermore, a wide input voltage range increases even further the current or voltage stresses on the active and passive components because they change with output to input voltage ratio. This excessively increases the sizes and ratings of active and passive components. Finally, EMI requirement at these ratings makes the associated filters very large, which leads to very heavy, bulky and also expensive converters [17].

At higher power levels most of the switching power converters are designed to operate in the continuous mode (CCM), because filtering is easier and noise is less. However, in boost operation of the half-bridge converter in CCM, control loop includes a right half-plane zero that makes loop compensation more difficult. On the other hand, in DCM operation, the small signal gain of the power circuit is much less than in the continuous mode, and loop gain varies considerably with load [47]. Here, the converter will be designed based on the continuous current mode of operation.

As for the pulse width modulator, among the many available varieties including fixed frequency - variable duty cycle, fixed on-time (variable frequency), fixed off-time (VF) and hysteretic, fixed frequency PWM method is chosen. The choice of PWM method considerably affects the power circuit behavior and small-signal characteristics.

4.3 COMPONENT SELECTION

4.3.1 FILTER INDUCTOR

The conduction mode of a power stage is a function of input voltage, output voltage, output current, and the value of the inductor. A boost power stage can be designed to operate in continuous mode for load currents above a certain level, usually 5 to 10% of full load. Usually, the input voltage range, output voltage, and load current are defined by the power stage specification. This leaves the inductor value as the design parameter to maintain continuous conduction mode. For sizing the inductor, important factors are inductor average current and inductor current ripple. The inductor ripple current is inversely proportional to its inductance and directly proportional to the applied voltage and the time that the voltage is applied. Smaller inductor with larger ripple current necessitates a bigger output filter capacitor, dictating a large minimum load current to avoid discontinuous operation. On the other hand, smaller inductor can offer lower size and cost while the inductor current can change more rapidly in response to a sudden load [47].

Using the inductor at currents below the dc current rating can reassure that it does not overheat or saturate of the core. Finally, maximum operating frequency should not be exceeded, which could also result in overheating or saturation of the core. After considering these parameters, the proper core material should be selected. Available choices are: ferrite, powdered iron and rod-core. While the first two are more popular, the last type is cheaper but suffers from noise problem [18]. As for the inductance value, the following equation can be used for half-bridge converter to assure the continuous conduction mode of operation [17]:

$$L_{min} = \max\left\{\frac{V_o}{\Delta I_{Lp.u} f_{sw} I_o} D_{1HB}(1\text{-}D_{1HB})^2,\ \frac{V_o}{\Delta I_{Lp.u} f_{sw} I_o} D_{2HB}{}^2(1\text{-}D_{2HB})\right\} \quad (4\text{-}1)$$

In this equation, ($\Delta I_{Lp.u}$) is the maximum ripple of inductor current and D_{1HB} and D_{2HB} are the duty cycle of boost and buck operations. As it can be realized from the equation, inductor size is inversely proportional to the switching frequency.

4.3.2 FILTER CAPACITOR

The output capacitance is generally selected to limit output voltage ripple to the level required by the specification. They typically absorb Amperes of ripple current and hold the output ripple voltage to a small fraction of a Volt. For sizing the capacitors, two important parameters are the capacitor rms current, which determines the capacitor loss and the peak to peak capacitor current, which is proportional to the capacitor voltage V_c. Equivalent series resistance (ESR) contributes to the output voltage ripple and the associated capacitor loss. For continuous inductor current mode operation in half-bridge converter, the following equation is used to determine the amount of capacitance needed as a function of output load current, I_O, switching frequency, f_S, and desired output voltage ripple, $\Delta V_{O\,p.u}$ [17]:

$$C_{o\text{-}min} = \frac{I_o D_{1HB}}{f_{sw} \Delta V_{o\,p.u}} \quad (4\text{-}2)$$

To keep the continuous current mode operation, the ESR required to limit the ripple to the desired value can be calculated by [18]:

$$ESR_{max} = \frac{\Delta V_o}{\left(\frac{I_{o(max)}}{1\text{-}D_{1HB}} + \frac{\Delta I_L}{2}\right)} \quad (4\text{-}3)$$

4.4 GATE DRIVE REQUIREMENTS FOR GALLIUM-NITRIDE SWITCHES

Faster switching speed is the main advantage offered by GaN FETs. However, this produces faster current and voltage variations, (di/dt and dV/dt), which require some specific considerations in physical layout design and also gate driver. Physical layout design is beyond the scope of this thesis, but as for the gate driver, particular requirements should be fulfilled. To determine them and realize the difference with regular silicon MOSFET drivers, the parameters between the two selected switches from two technologies are compared in Table 4.1.

Table 4-1 Parameter comparison between GaN and Si switches

Technology	Si (IPP320N20N3G)	GaN (EPC1010)
Gate threshold	2 V – 4 V	0.7 V - 2.5 V
Maximum gate-source voltage	+/-20 V	+6 V /-5 V
dV/dt capacitance (Miller) ratio Q_{GD}/Q_{GS}	0.5-0.7	1.1
Internal gate resistance	2.5 Ω	0.6 Ω
Reverse 'body diode' voltage	~1 V	~1.5-2.5 V

Key points are the maximum allowable voltage, and the threshold voltage, which are both lower for GaN switches. With high dV/dt and low threshold voltage of GaN, the

chance of having the unwanted miller turn-on in a half-bridge circuit will rise. To avoid this following condition should be satisfied [48]:

$$C_{GD} \times \frac{dV}{dt} \times (R_G + R_{drive}) \times \left(1 - e^{-dt/\alpha}\right) \leq V_{TH} \tag{4-4}$$

Where dt is the switching time and α is passive network time constant. Therefore, the value of R_{drive} (pull-down resistance) should be selected carefully to avoid the undesired turn-on of the switches in the bridge. Furthermore, too high of a dV/dt can in fact reduce the efficiency by creating shoot-through during the switching transition.

Therefore, it is necessary to adjust the gate drive pull-up resistance in order to minimize transition time without inducing extra losses [48]. In short, in designing the ideal driver for GaN switches following points should be considered:

1) Gate drive pull-down resistance should be minimized for maximum dV/dt immunity and low driver loss.
2) Gate drive supply voltage should be accurately adjusted not to exceed the maximum gate-source voltage.
3) For EMI and voltage overshoot control pull-up resistance should also be monitored.
4) Again to avoid EMI problem, the gate driver circuit should be placed as close as possible to the GaN switch to minimize the loop impedance.

A simple discrete driver, which is used in the experimental test in this thesis is sketched in Fig. 4-1. In this configuration, S_2 should be selected with less than 500 mΩ on-resistance, while R_2 can regulate the pull-up resistance. S_1 and S_3 should be selected with higher on-resistance, yet still able to drive S_2 and S_4. To limit the cross conduction between S_1 and S_3, resistor R_1 is added to the circuit [48].

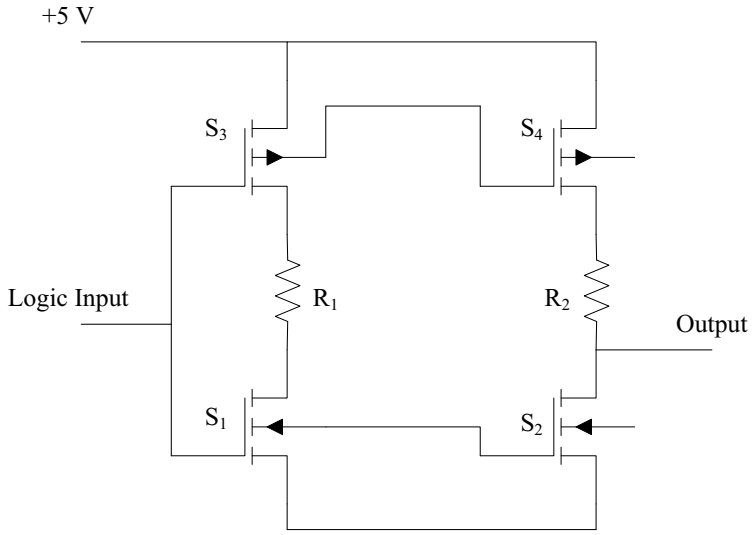

Fig. 4-1 Discrete gate-driver solution for GaN.

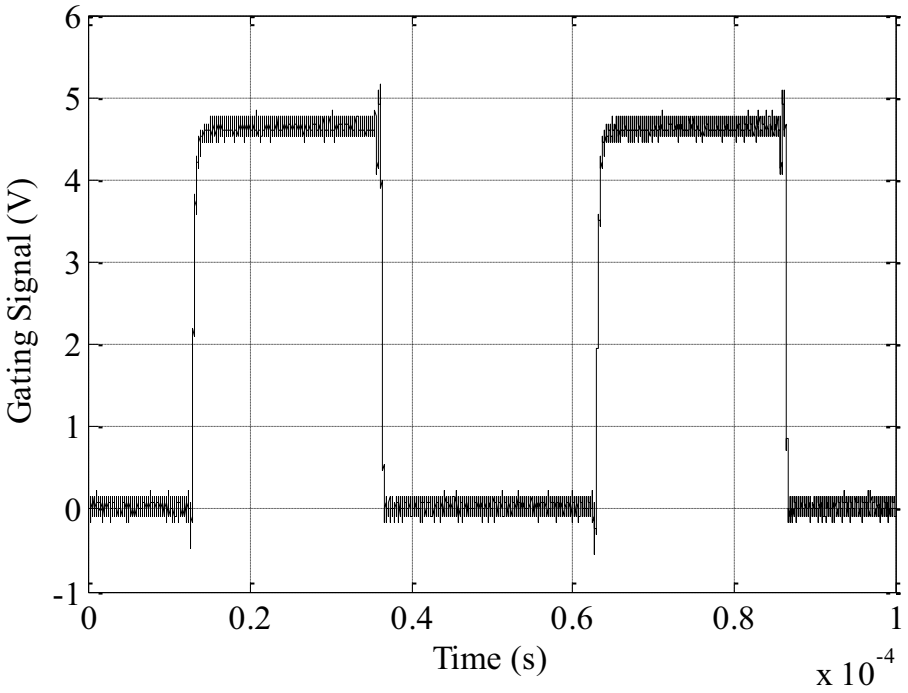

Fig. 4-2 Gating signal generated from the discrete driver.

The output waveform of this driver designed to drive the half bridge converter from experimental test is shown in Fig. 4-2. The switching frequency is set to 20 kHz.

4.5 EXPERIMENTAL SETUP

To examine the possible advantages of GaN switches, two half-bridge converters with the same inductor and capacitors using mentioned switches from the two technologies were built. Fig. 4-3 illustrates the schematic of the experimental setup. The test is performed at 20 kHz and 200 kHz of switching frequency with the minimum values for the components to satisfy the design specification provided in Table 4-2. 200 kHz is chosen as a value well above the typical range of switching frequency (5-50 kHz) for the converters in automotive and renewable energy applications and it is not necessarily demonstrate optimum value. The values for passive components chosen based on the design procedure explained earlier in this chapter are gathered in Table 4-3 and Table 4-4.

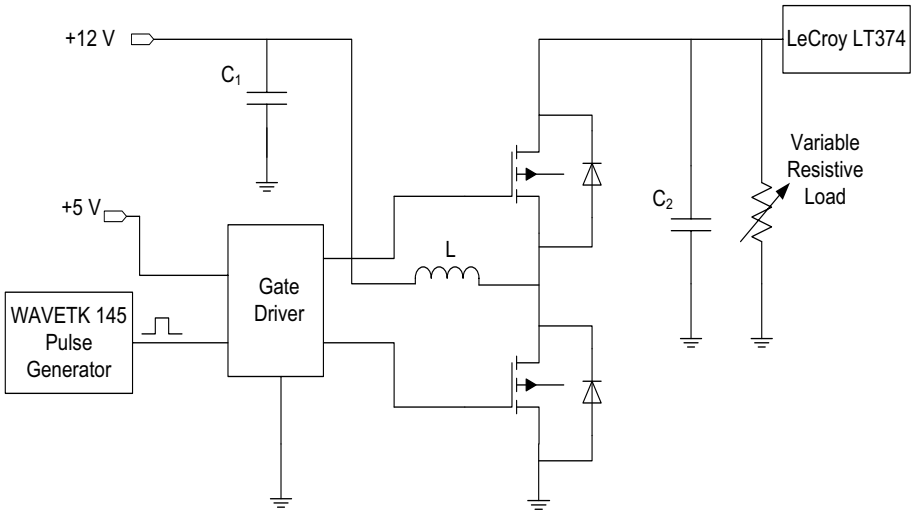

Fig. 4-3 Experimental setup schematic.

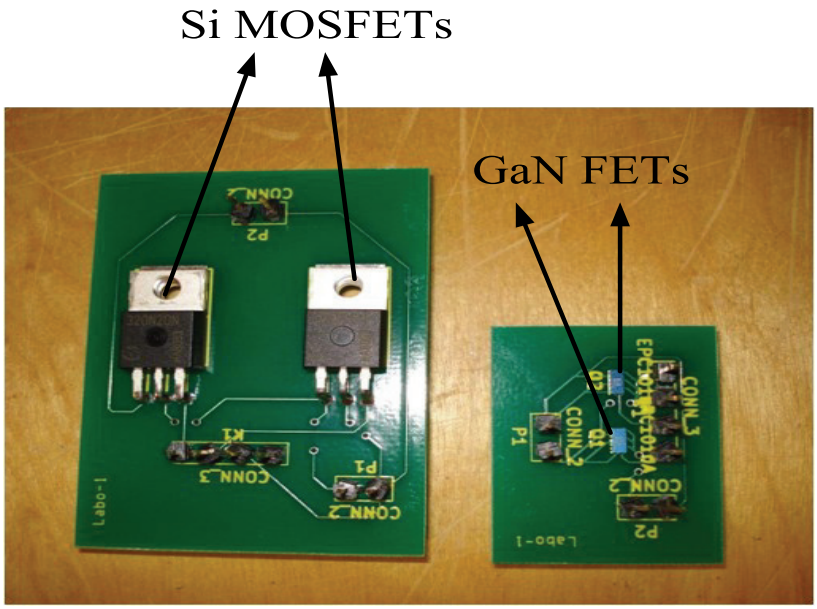

Fig. 4-4 Top view of the board.

Table 4-2 Converter design specifications.

Parameter	Value
Nominal Input voltage (V)	12
Average output current (A)	0.5
Output Voltage (V)	24
Output Voltage Ripple	5%
Inductor Current Ripple	30%

Table 4-3 Characteristics of selected inductors.

Switching frequency	Inductor (μH)	ESR (Ω)	DC rated Current (A)
20kHz	560	0.6	1
200kHz	100	0.098	2

Table 4-4 Characteristics of selected output capacitors.

Switching frequency	Capacitance μF	ESR (mΩ)	Voltage Rating (V)
20kHz	1000	40	50
200kHz	800	40	50

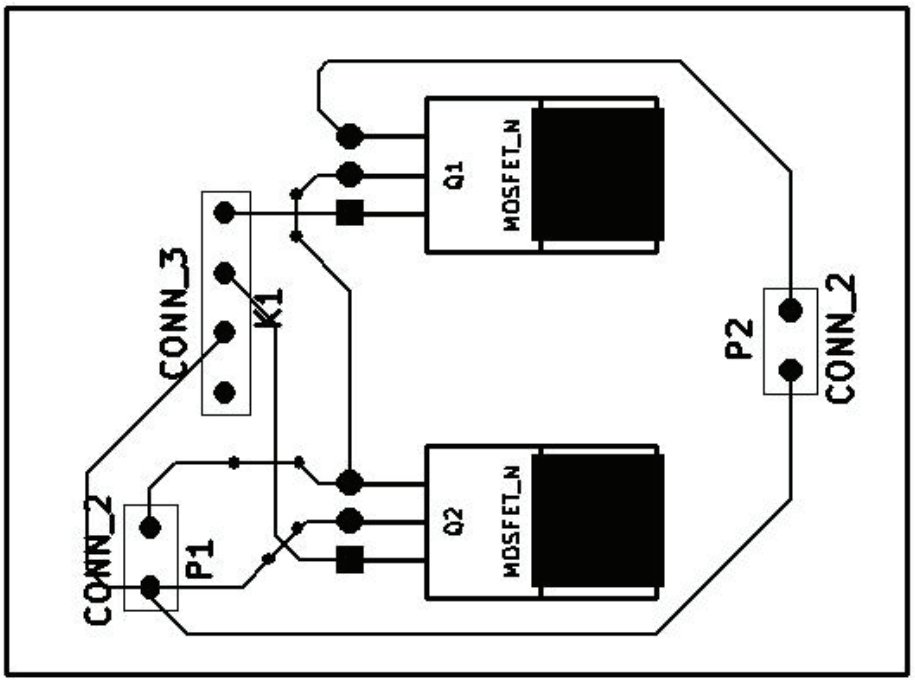

Fig. 4-5 Si-based PCB schematic.

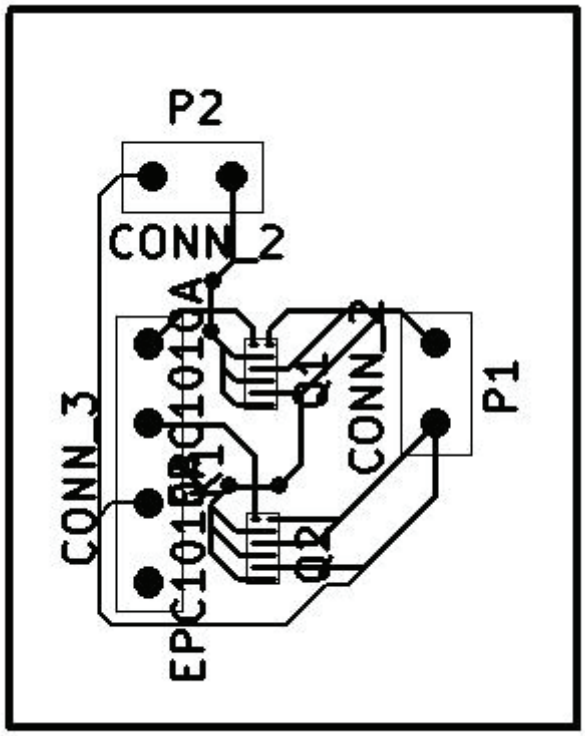

Fig. 4-6 GaN-based PCB schematic.

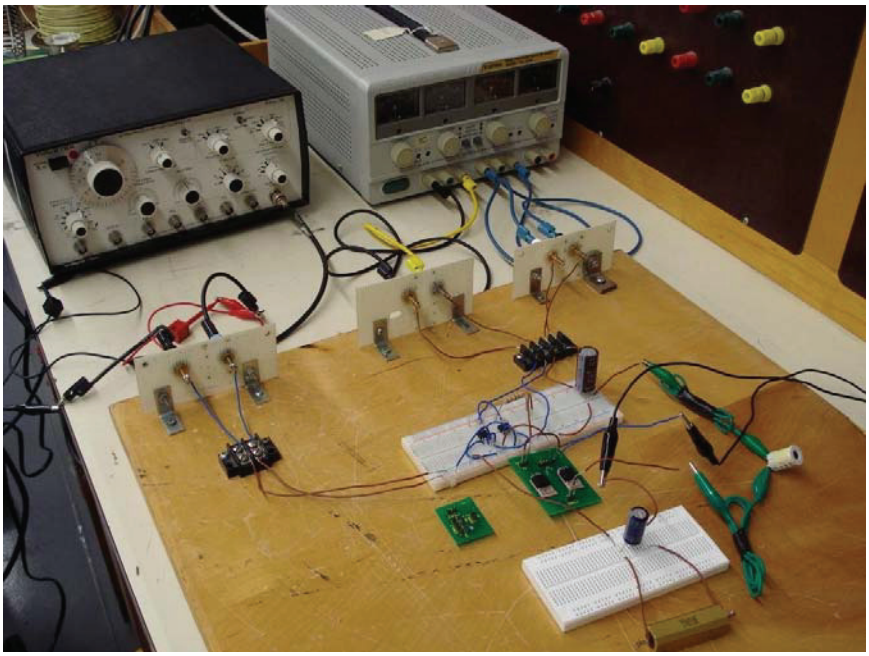

Fig. 4-7 Experimental setup.

Two circuits with GaN and Si switches are quite identical with the same current paths and filter components, which assure that any difference between the two converters will rise from the difference between the operations of switches. Top view of the two boards each containing two bridge switches is shown in Fig. 4-4, which illustrates the smaller size of GaN switches compared to Si as indicated in chapter two. The schematic of the PCBs are sketched in Fig. 4-5 and Fig. 4-6. The entire experimental setup is shown in Fig. 4-7.

4.5.1 EXPERIMENTAL RESULTS at 20 kHz OPERATION FREQUENCY

The results for Si and GaN-based converters are provided in Table 4-5 and Table 4-6, respectively. The efficiency of two converters operating at 20 kHz of switching frequency for different load currents is compared in Fig. 4-8. Around 2% efficiency improvement is observed with GaN switches. To calculate the efficiency, output power is divided by the input power. The output current varies from 200 mA to 600 mA.

Table 4-5 Si-based converter results at 20 kHz.

V_{in} (V)	I_{in} (mA)	V_{out} (V)	I_{out} (mA)	Eff. %	Total loss (W)	Inductor Loss (W)	Switch Loss (W)
12.1	524	24.1	209	80.1	1.30	0.26	1.04
12	755	23.7	300	78.47	1.95	0.29	1.65
11.9	1093	24.2	408	75.88	3.13	0.66	2.47
12.2	1332	23.8	506	74.08	4.21	0.83	3.38
12	1622	23.5	602	72.64	5.32	1.55	3.77

Table 4-6 GaN-based converter results at 20 kHz.

V_{in} (V)	I_{in} (mA)	V_{out} (V)	I_{out} (mA)	Eff. %	Total loss (W)	Inductor Loss (W)	Switch Loss (W)
12.1	505	24.1	209	82.4	1.07	0.21	0.856
12	740	23.7	300	80.01	1.77	0.31	1.45
11.9	1054	24.2	408	78.7	2.66	0.44	2.22
12.2	1290	23.8	506	76.49	3.7	0.86	2.84
12	1570	23.5	602	75.05	4.70	1.06	3.64

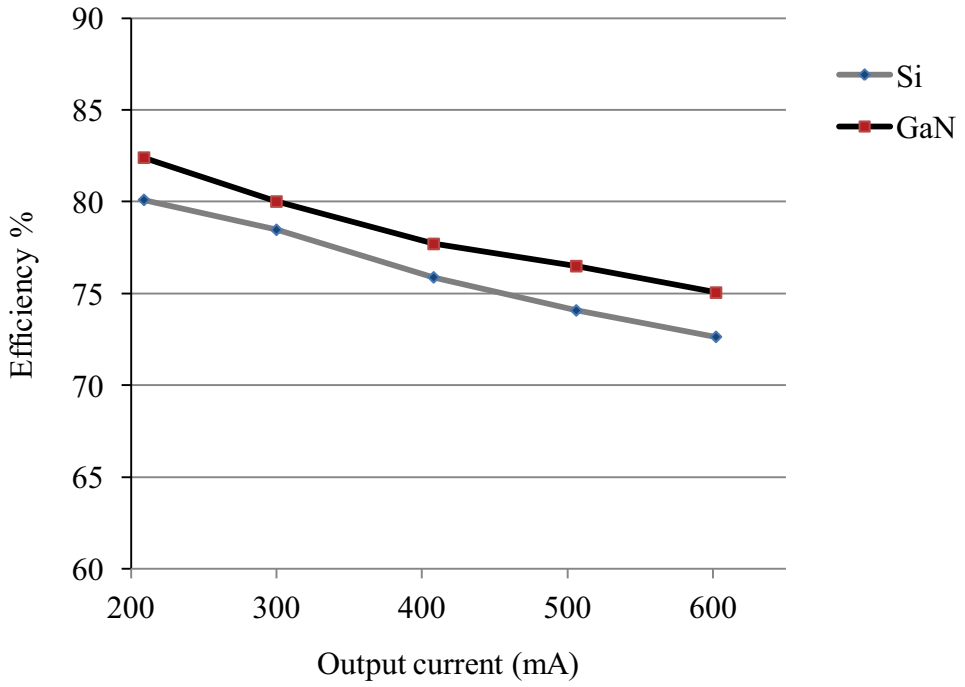

Fig. 4-8 Efficiency vs. load current at 20 kHz.

Another approach to prove the superior performance of GaN switches compared to Si is to evaluate the power dissipation of the switches. Main sources of power loss in this circuit are inductor and two switches (one switch + one diode in boost operation). In

order to evaluate the power dissipation in switches, inductor power loss will be calculated first based on the following equation [49]:

$$P_L = \frac{I_o}{1-D} \times ESR^2 + \text{estimated core loss} \tag{4-5}$$

Standard graphs which are typically provided by the manufacturer can be used to estimate the core losses. These graphs are based on Steinmetz equation [50]:

$$P_{core}(mW) = K_1 \times f^x \times B^y \times V_e \tag{4-6}$$

where:

K_1 = Constant for core material

f = Frequency in kHz

x = Frequency exponent

B = Peak flux density in kGauss

y = Flux density exponent

V_e = Effective core volume (cm^3)

However, in this thesis, total power loss of the inductor is calculated based on the measured voltage difference across the inductor multiplied by its current. Power dissipation in switches can then be calculated as:

$$P_{switch} = P_{in} - (P_{out} + P_L) \tag{4-7}$$

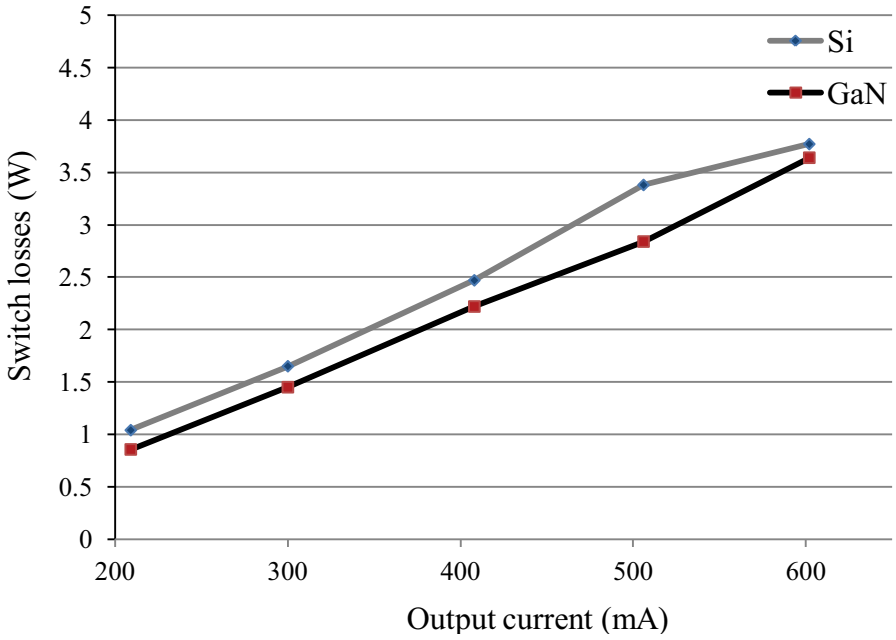

Fig. 4-9 Switch losses vs. load current at 20 kHz.

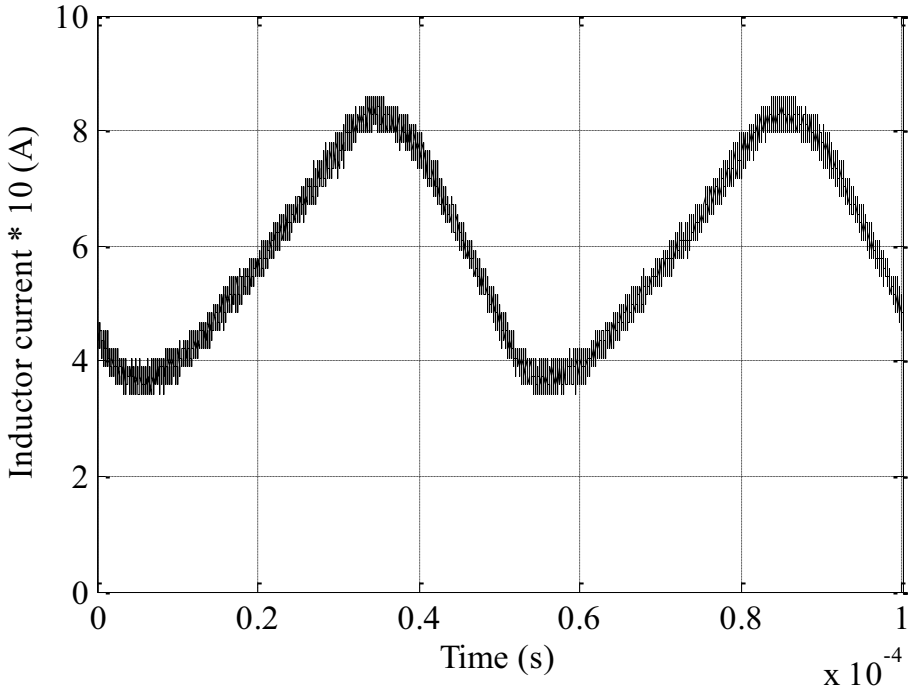

Fig. 4-10 Inductor current waveform for GaN-based converter at 20 kHz.

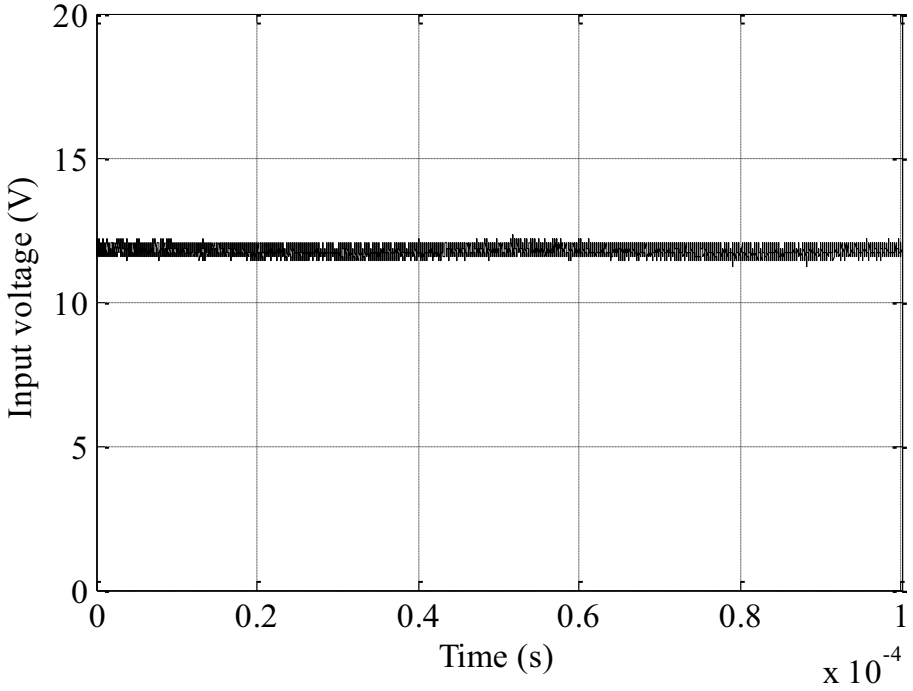

Fig. 4-11 Input voltage waveform for GaN-based converter at 20 kHz.

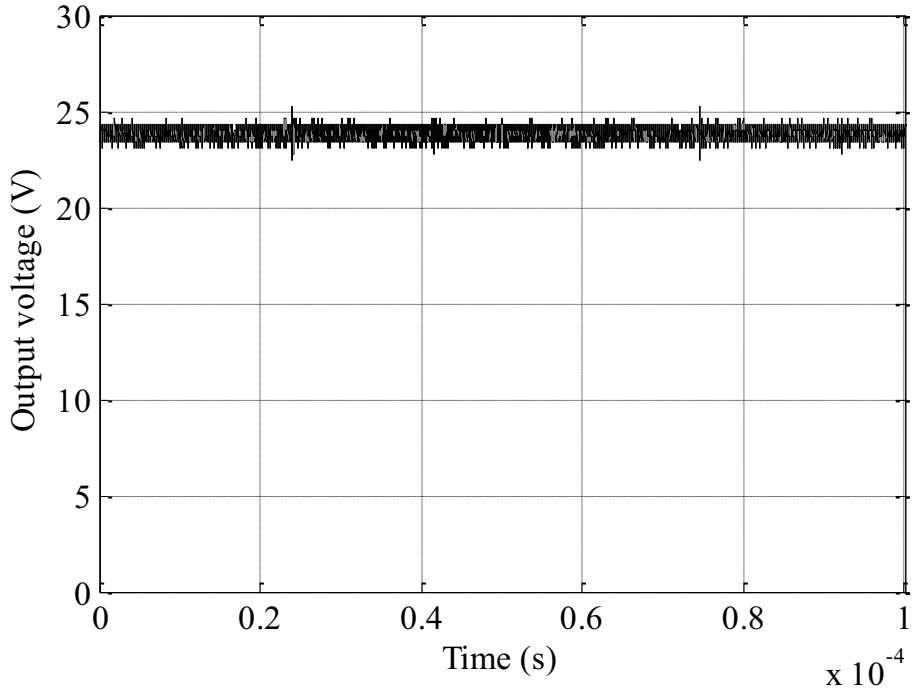

Fig. 4-12 Output voltage waveform for GaN-based converter at 20 kHz.

Data of this step is provided in Table 4-7 and Table 4-8 for Si and GaN-based converters. Fig. 4-9 illustrates the switch losses (including switching, switch conduction, and diode conduction) as a function of load current. Around 0.2 W could be saved here by using GaN switches. It is worth mentioning that this converter is designed for 12 W output power. Therefore, at larger power scales designed for target applications, this power saving could be much larger and influential on the system level. Typical operating waveforms of the GaN converter are shown in Fig. 4-10 to Fig 4-12.

4.5.2 EXPERIMENTAL RESULTS at 200 kHz OPERATION FREQUENCY

Same test is performed on 200 kHz of switching frequency. As it was expected, GaN switches better demonstrate their advantage over Si at higher switching frequencies. At the same load current, around 4% higher efficiency could be achieved by implementing GaN switches instead of Si. This happens while the overall size of the converter can be reduced due to lower sizes of inductor, capacitor and switches. Results of this part are provided in Table 4-8 and Table 4-9. Fig. 4-13 and Fig. 4-14 are showing efficiency and switch power dissipation variation over different load currents.

Table 4-7 Si-based converter results at 200 kHz.

V_{in} (V)	I_{in} (mA)	V_{out} (V)	I_{out} (mA)	Eff. %	Total loss (W)	Inductor Loss (W)	Switch Loss (W)
12	531	24.2	201	76.26	1.50	0.32	1.18
12.1	813	23.9	305	74.03	2.54	0.45	2.08
11.9	1115	24	403	72.85	3.59	0.67	2.92
12	1392	23.7	501	71.08	4.83	1.21	3.62
12	1714	23.6	602	69.06	6.36	1.98	4.38

Table 4-8 GaN-based converter results at 200 kHz.

V_{in} (V)	I_{in} (mA)	V_{out} (V)	I_{out} (mA)	Eff. %	Total loss (W)	Inductor Loss (W)	Switch Loss (W)
12	503	24.1	201	80.12	1.19	0.23	0.95
12.1	762	23.7	305	78.33	1.99	0.35	1.63
11.9	1063	24.2	403	77.08	2.89	0.	2.35
12	1323	23.8	501	75.08	3.95	1.06	2.89
12	1626	23.5	602	72.46	5.37	1.21	4.16

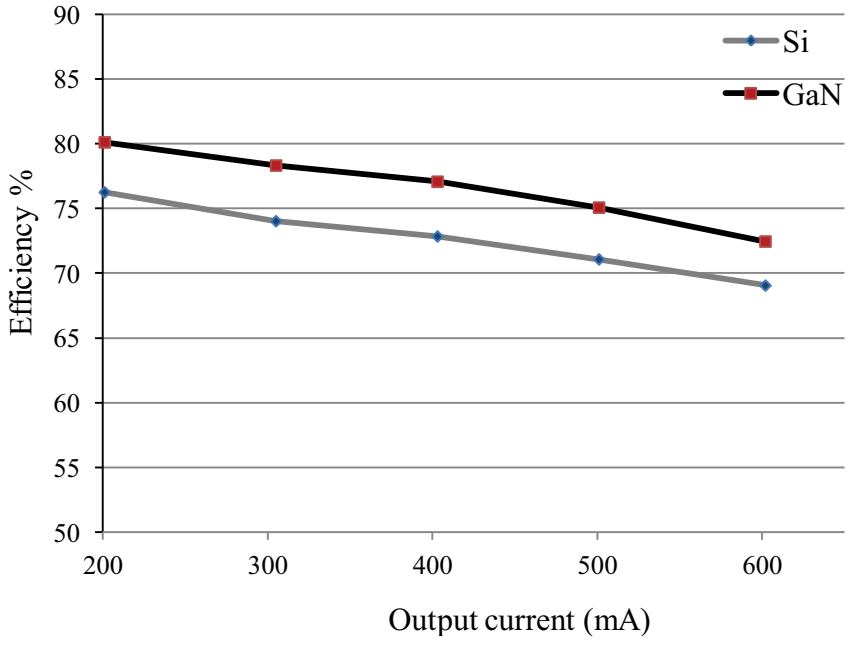

Fig. 4-13 Efficiency vs. load current at 200 kHz.

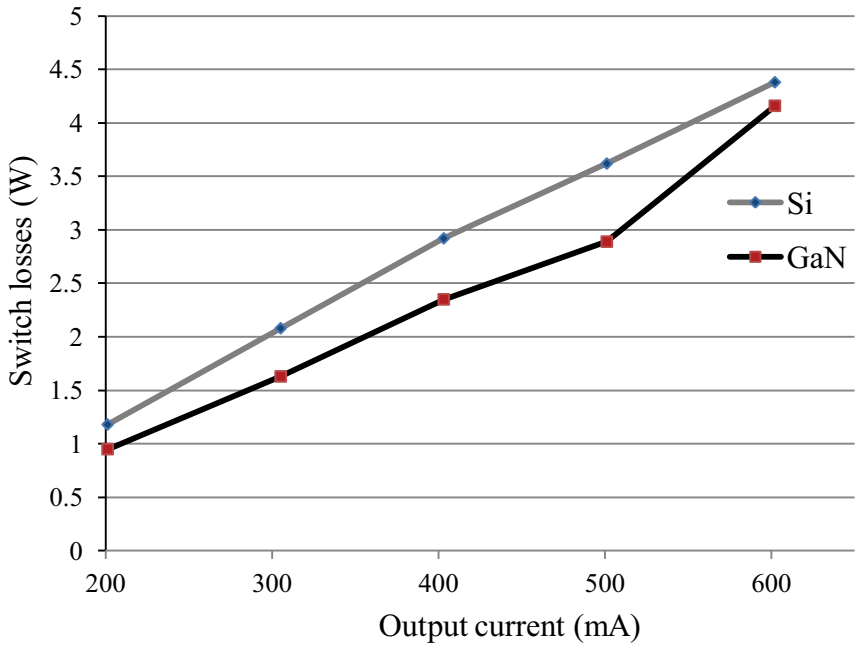

Fig. 4-14 Switch losses vs. load current at 200 kHz.

4.6 Effects of Increasing Frequency on Magnetic Core Losses

While the increase in frequency has the potential to reduce the overall weight and size of any power electronics converter, some concerns may arise from the performance of magnetic components at higher frequencies. The main issue could be noticed from the Steinmetz equation, which was mentioned earlier (equation 4-6). At a first glance it would seem that with the increase in frequency core losses also increase, but this is not always the case. In order to continue this analysis, following equation need to be reviewed [50]:

$$B = \frac{V \times t \times 10^{8}}{N \times A} \tag{4-8}$$

where:

B= Peak flux density in Gauss

V = Voltage in Volts

t = Time on in seconds

N = Number of turns

A = Core area of selected core in cm^2

And since the frequency is inversely proportional to time, it can be deduced that [50]:

$$B \propto \frac{1}{N \times A \times f} \tag{4-9}$$

Therefore, with the turns and core area staying constant, if the frequency is increased, then the peak flux density will decrease. By looking again at the Steinmetz equation reduction in peak flux density will have a more effective impact on core loss because the peak flux density will be reduced exponentially by the factor of approximately 2.5, while the frequency is increased exponentially by 1.5 [50]. Therefore, the increase in frequency results in the decrease of core losses. In the meanwhile, if the core area is reduced when the frequency is increased a reduction in core loss may not be evident. In the end, it can be concluded that at higher frequencies, total inductor losses decrease because of the reduction in inductance, core area, and volume.

CHAPTER 5

GALLIUM-NITRIDE POWER HFET DESIGN

5.1 INTRODUCTION

In this chapter, by considering the requirements of future automotive and renewable energy applications, which have been mentioned in the first chapter, design of GaN-based high electron mobility transistors is reported. Based on the literature review and analytical calculations expected values in terms of switch breakdown voltage, on-resistance, and current capacity are forecasted. In order to increase the breakdown voltage, field-plate (FP) technology is implemented. Advantages, disadvantages, and limitations of this technology are explained in detail, following a presentation of the involved equations for choosing the associated parameters.

5.2 DEVICE DESIGN

5.2.1 FIELD-PLATE AND ENHANCEMENT OF BREAKDOWN VOLTAGE

Enhancing the breakdown voltage, while maintaining the low value of on-resistance, is one of the most important challenges of GaN-based FET design. A well-known method for enhancing the breakdown voltage in AlGaN/GaN HFET technology is based on employing a metallic field-plate for engineering the electric-field profile of the high electric–field drain-access region [51]. Field-plate is a metal electrode connected to either gate- or source-electrodes, which is placed over the drain-access region. This implement reshapes the distribution of electric-field along the two dimensional electron

gas (2-DEG) channel in favor of reducing its peak value. This reduction in peak value of the electric-field, at the drain edge of the gate, results in a higher channel breakdown voltage. In design of field-plates a compromise between the degradation of the maximum switching speed, due to the addition of the field-plate capacitance, and improvement to the channel breakdown voltage should be made. Higher breakdown voltages can be achieved by means of implementing two or more field-plates. However, this will add at least another two steps to the fabrication process, while degrading the switching speed by increasing the gate-drain capacitance. The trade offs of implementing field-plate include possible increase in gate resistance (*i.e.* R_G) and introduction of additional parasitic capacitances between gate, drain and source [51].

Gate-connected field-plates contribute to higher gate to source and gate to drain capacitances (*i.e.* C_{gs} and C_{gd}), while source-connected field-plates result in higher drain to source capacitance (*i.e.* C_{ds}) [52]. Therefore, source-connected field-plates only increase one of the parasitic capacitances and are more advantageous from this point of view. On the other hand, gate-connected field-plates contribute lower to the gate resistance. In order to design a power switch, based on a brief literature review, which is provided in the next section, required parameters are chosen. In addition, analytical approach is applied to designing field-plate parameters including field-plate's length and thickness of insulator layer beneath it.

5.2.2 LITERATURE REVIEW

Based on the required characteristics of the state of the art power electronics, some of the published reports on design of power AlGaN/GaN HFETs have been chosen and used in designing a power switch. Table 5-1 presents the parameters and their values

from the selected reports. Among these parameters, gate-drain distance (*i.e.* L_{gd}), length of first and second field-plate (*i.e.* L_{f1} and L_{f2}), and the material used as the insulator and its thickness (*i.e.* t) are more vital in determining the breakdown voltage of the switch. As for the current drive, around 500 mA of current per millimeter of the gate width is expected from a power AlGaN/GaN HFET [53].

Table 5-1 Switch parameters and reported breakdown voltages [55]-[60].

Author	L_g (μm)	L_{gd} (μm)	Substrate	Number of FPs	L_{f1} (μm)	L_{f2} (μm)	Dielectric (nm)	FP connection	V_{BDN} (V)
Dora *et al.* [55]	1.5	24	Sapphire	1	0.5	-	SiN-120	Gate	600
Dora *et al.* [55]	1.5	24	Sapphire	2	0.5	0.5	SiN-120	Gate	900
Saito *et al.* [56]	1.5	10	Sapphire	2	5	2.5	SiN-600	Gate and Source	600
Saito *et al.* [56]	1.5	15	Sapphire	2	5	2.5	SiO_2-600	Gate and Source	940
Dora *et al.* [57]	1	20	SiC	1	0.5	-	SiN-120	Gate	1900
Yagi *et al.* [58]	4	28	Sapphire	0	-	-	TiO_2-15	-	2000
Huang *et al.* [59]	Not mentioned	15	Sapphire	1	3	-	SiN-300	Source	475
Bahat-Treidel *et al.* [60]	1.5	10	SiC	2	1	1	SiN-150	Gate	700

5.2.3 ANALYTICAL APPROACH

The analytical approach developed in [59], is applied in order to design the parameters associated with the field-plate (including field-plate length (L_f) and the thickness of the insulator layer). All of the device dimensions, with the exception of the field-plate, are assumed to be constant throughout this approach. The parameters are shown in Fig. 5-1.

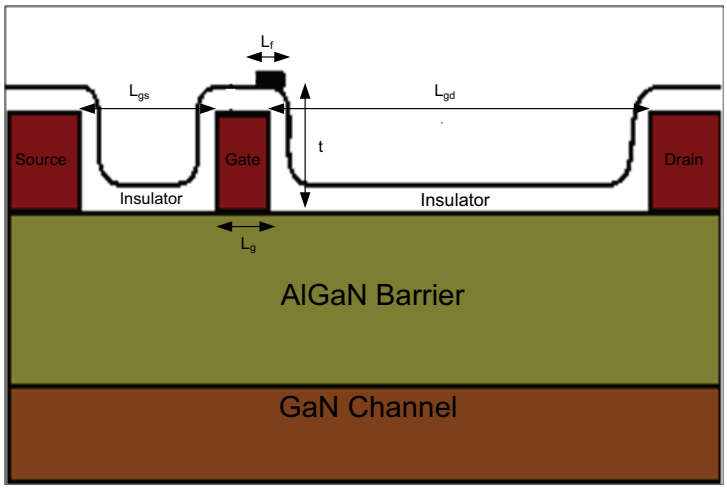

Fig. 5-1 AlGaN/GaN HFET structure with gate-connected field-plate.

After implementing the field-plate and under optimum conditions for reaching the highest possible breakdown voltage, the electric field distribution can be approximated with a linear segment combined with an exponentially decaying part. This approximation has been illustrated in Fig. 5-2.

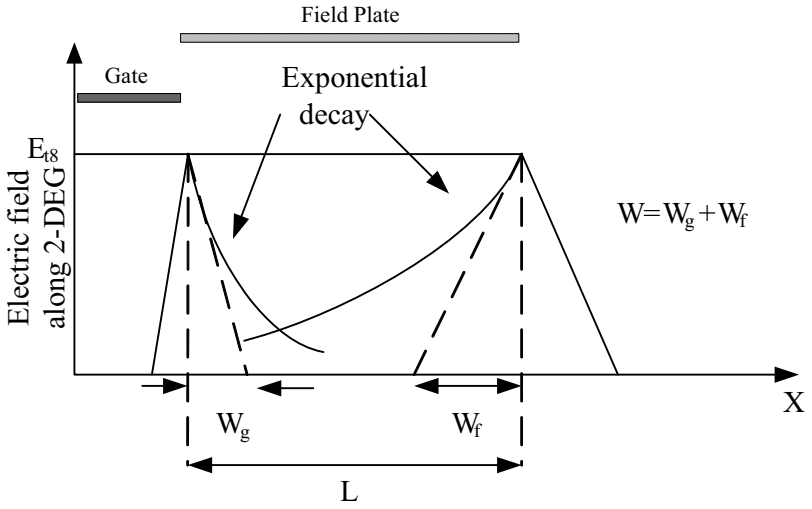

Fig. 5-2 Electric field distribution along the 2-DEG under optimum conditions [59]. W_f and W_g stand for the index of field distribution spread under field-plate and gate, respectively.

Based on this electric field distribution, breakdown voltage, which is the total area under the field distribution with peak equal to the breakdown electric-field of the channel, can be approximated by:

$$V_d \approx \left(\frac{3}{2}\right) E_{t\infty} W \tag{5-1}$$

Here, W is the index of spread of the field distribution under the field-plate and $E_{t\infty}$ equals to GaN's breakdown field (*i.e.* approximately 3.3 MV/cm) [60]. To study the influence of other parameters in determining the electric-field distribution along the 2-DEG channel, an equation which corresponds to the numerical results of the simulation (and also satisfies the known physical limitations) is derived by Karmalkar *et al.* [59]. Parameters included in this equation are: ε_t the insulators relative dielectric constant (which is 7.5 for silicon nitride), d which is the barrier layer thickness (normally varying

between 0.02 μm to 0.03 μm), ε_d the relative dielectric constant of the barrier layer (which equals to 9.5 for AlGaN), and n which is the polarization charge concentration at the hetero-interface (which is in the order of 10^{13} cm^{-2}). Based on experimental data, Karmalkar *et al*. have proposed the following relationship between these variables [59]:

$$\left(\frac{t}{\epsilon_t}\right) \approx \alpha \left(\frac{V_d}{n}\right)^m \left(\frac{d}{\epsilon_d}\right)^p \tag{5-2}$$

In this empirical equation α, m, and p are fitting parameters. These fitting parameters towards the calculation of the optimal value of the thickness of dielectric (*i.e.* *t*) have been determined as [59]:

$$t \approx 2.8 \left(\frac{\varepsilon_t V_d}{n}\right)^{0.8} \left(\frac{d}{\varepsilon_d}\right)^{0.27} \tag{5-3}$$

where t and d are in Å, V_d is in volts, and n is taken to be equal to 10^{13} cm^{-2}.

A corresponding framework has been developed by Karmalkar *et al.* for calculation of W and L_{min} (*i.e.* the minimum length of the field-plate) [59]:

$$W \approx 0.03 \left(\frac{V_d}{n}\right)^{0.52+0.014\varepsilon_d} \left(\frac{d}{21\varepsilon_d}\right)^{1.3\left(\frac{V_d}{n}\right)^{-0.3}} \tag{5-4}$$

$$L_{min} = 1.5\, \varepsilon_t^{-0.15}\, W^{0.7} \tag{5-5}$$

Combining the equations (5-1) through (5-6), one can find the formula to study the variation of breakdown voltage versus L_{min}:

$$V_d = \left(\frac{L_{min}}{0.014}\right)^{1.42} \tag{5-6}$$

Fig. 5-3 illustrates the variation of breakdown voltage corresponding to different lengths for field-plate.

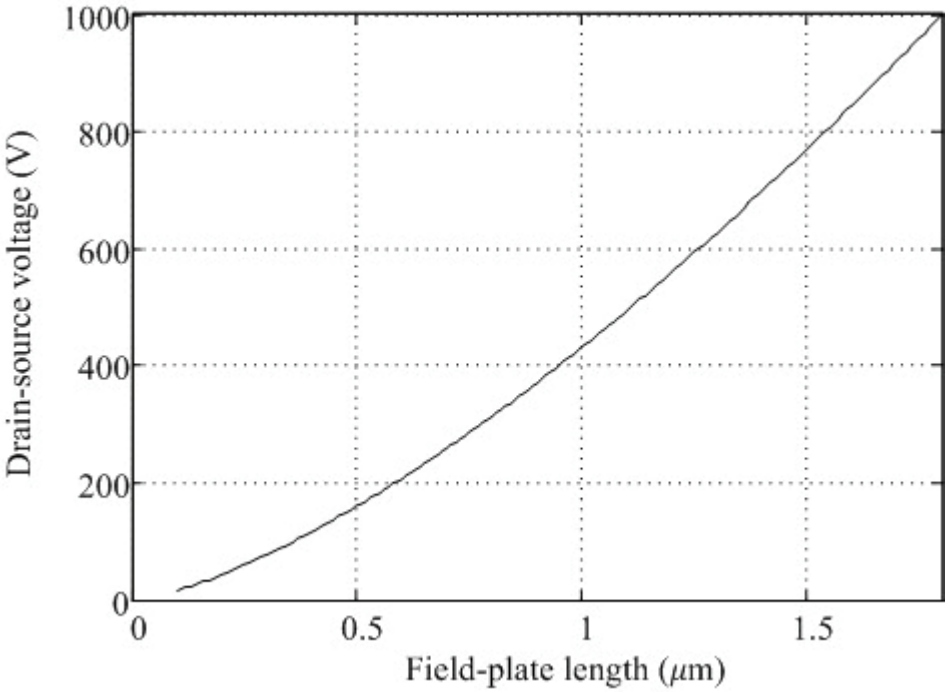

Fig. 5-3 Variation of breakdown voltage with field-plate length.

Same procedure can be applied to study the variation of breakdown voltage with the insulator thickness. This is shown in Fig. 5-4.

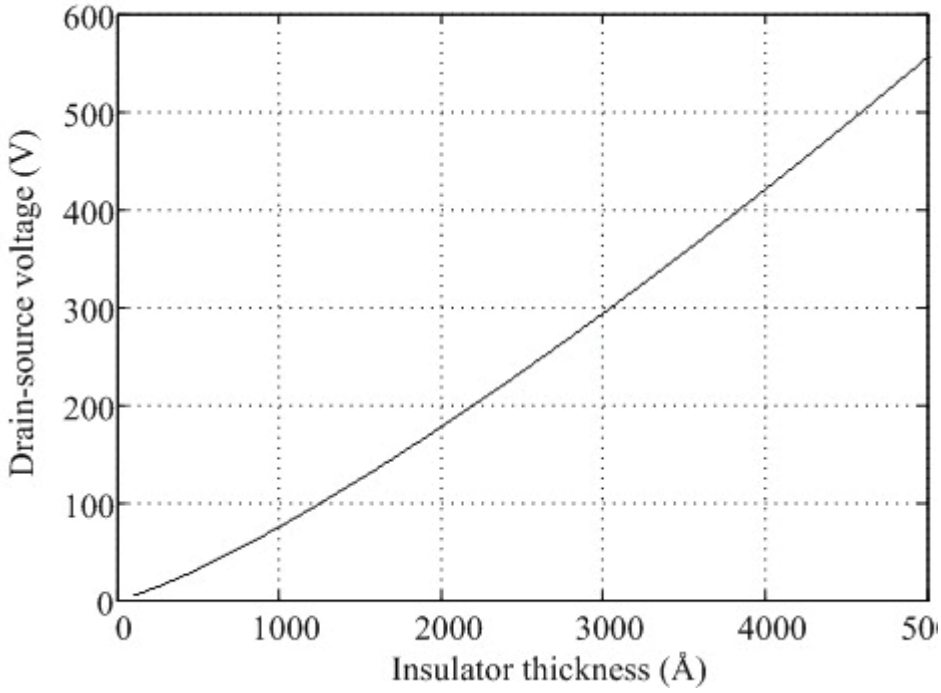

Fig. 5-4 Variation of breakdown voltage with insulator thickness.

5.2.4 PROPOSED DESIGN

In order to design a power switch with high breakdown voltage, three crucial variables, specifically the field-plate's length, the insulator thickness and gate-drain separation L_{gd} have to be accurately selected. Among them, the first two are chosen based on the analytical approach presented in the previous section. By choosing the proper values, the aforementioned equations can be solved to find the maximum possible breakdown voltage and the associated field-plate geometry. To do so, equations (5-1) and (5-4) should be solved together with $E_{t\infty}$ equals to GaN's breakdown field (*i.e.* approximately 3.3 MV/cm) [59], to calculate the breakdown voltage V_d. After finding W and V_d, equations (5-3) and (5-6) can be used to calculate the minimum filed-plate length, L_{min}, and insulator thickness, t. Calculated values are presented in Table 5-2.

Table 5-2 Calculated values for field-plate parameters.

Parameter	Value
Breakdown voltage (V)	340
Minimum field-plate length (μm)	0.86
Insulator thickness (μm)	0.12

In our design, the value of L_{gd} has been varied from 2.5 to 7.5 μm for different fabrication runs. However, with L_{gd} = 5 μm which is thought to be the optimum value based on the literature review, highest breakdown voltage is expected [60]. Table 5-3 contains the values of the essential parameters of the proposed designs. As for the rated current, a general rule of thumb in GaN power switches demonstrates around 500

mA/mm of the gate width [61]. In our case, the gate width of 2 × 1 mm should make the switch capable of operating up to 1 A for I_{ds}.

Table 5-3 Switch dimensions.

Parameter	Value
Channel Width (mm)	1
L_g (μm)	0.4
L_{gs} (μm)	0.5
L_{gd} (μm)	2.5
Field-Plate (μm)	0.86
Insulator Thickness (μm)	0.12

Fig. 5-1 is showing the cross-section schematic of the proposed design. For the fabrication, according to the CMC's process flow of AlGaN/GaN HFET a mask set has been developed in Ledit software. Fig. 5-5 illustrates the schematic of this mask.

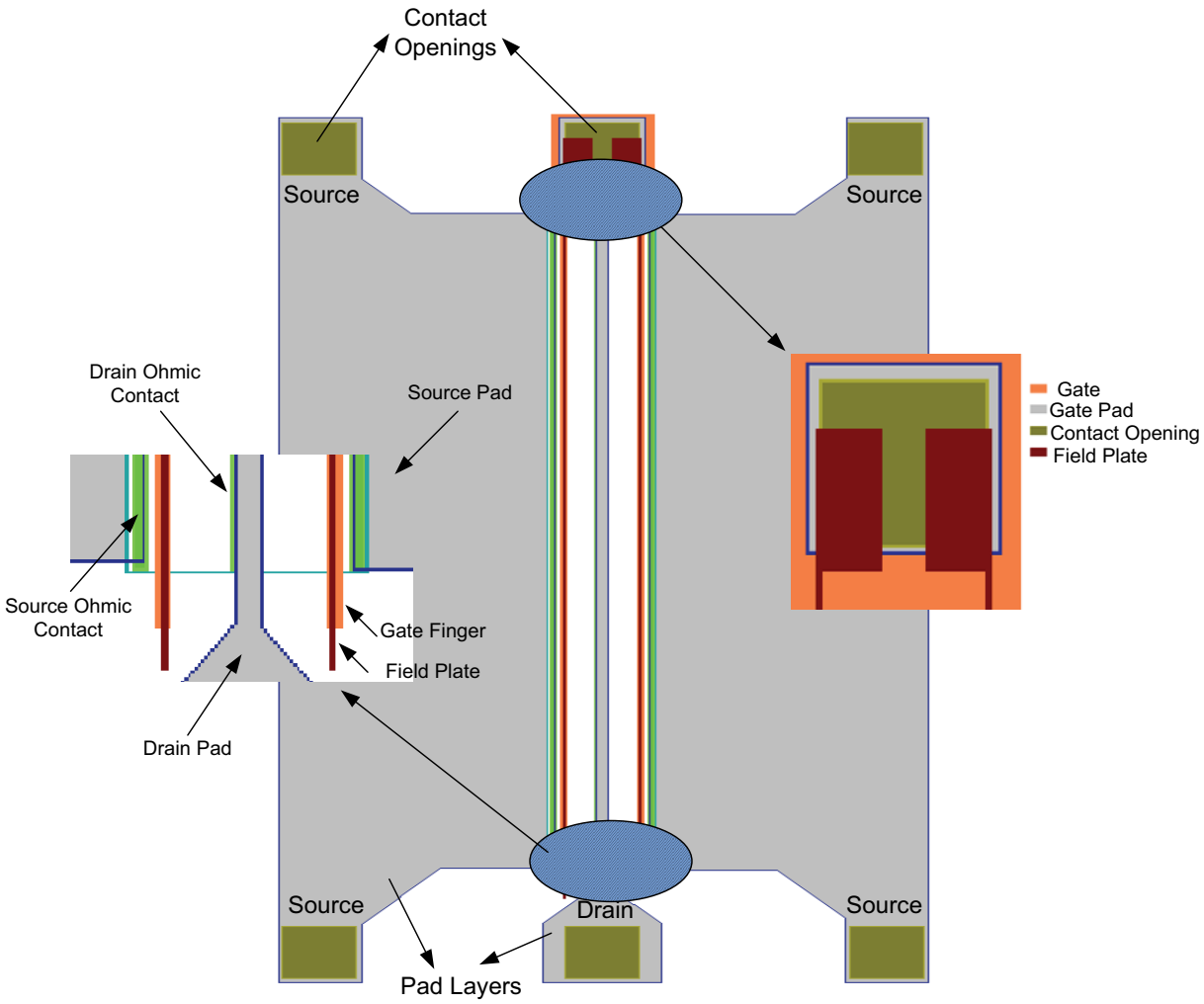

Fig. 5-5 Mask schematic of the proposed design with gate-connected field-plate.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSION

Unique characteristics of GaN high electron mobility devices including high breakdown voltage, low on resistance and low thermal impedance make them promising candidates for the future high voltage, high switching frequency and high temperature applications. These applications can be divided into two categories. First group of applications such as hybrid automotive and industrial motor control benefit from the high breakdown voltage and high temperature performance of GaN switches. On the other hand, improved device figure of merit (FOM) $R_{on} \times Q_{sw}$ resulted from GaN's fast switching speed and low on-resistance can merge with the advanced packaging techniques to enhance the power conversion FOM: Efficiency × density/cost. This can benefit a second group of applications including renewable energy systems such as grid-connected DC/AC inverters of photovoltaic systems, uninterruptible power supplies (UPS) and switch-mode power supplies (SMPS).

In this thesis, different aspects of introducing GaN switches into future automotive and renewable energy power electronics applications are discussed. General properties such as superior high temperature performance, lower on-resistance and higher breakdown voltage of GaN switches compared to the state of the art Si MOSFETs are initially discussed. The switching behavior of commercial GaN switches is evaluated by means of the Spice models provided by the manufacturer, which are used later to simulate a typical half-bridge DC/DC converter. Having these advantages of GaN

switches in mind, different converter topologies for electric vehicle's power management systems are compared. As a result, half-bridge converter, which is believed to be the best option, is selected to evaluate the performance of GaN switches. Based on the specifications, proper values to reach the intended converter performance are chosen. Two converters with the same ratings and elements using GaN and Si switches are designed and superior performance of GaN-based converter in terms of efficiency and size is confirmed by means of both simulation and experiment. However, with today's price of GaN switch, it would be hard to convince designers to implement these switches into the mentioned applications for maximum 4% efficiency improvement in which the overall price of the system may increase up to twice the corresponding Si-based system. Most of the major semiconductor companies such as International Rectifier (IR), have established their research and development group on GaN switches which nowadays are mainly working on reducing the production cost.

Finally, design of GaN-based high electron mobility transistors is reported. According to the literature review and analytical calculations expected values in terms of switch breakdown voltage, on-resistance, and current capacity are forecasted. Involved equations for choosing the parameters are presented. Advantages, disadvantages, and limitations of the field-plate (FP) technology, which is implemented in order to increase the breakdown voltage, are explained in detail.

6.2 FUTURE WORK

According to the targets which have been set by US department of Energy for HEVs in 2020, power electronics should provide:

1) Power density higher than 14.1 kW/kg

2) Efficiency better than 98% with the price less than $3.3/kW

GaN-based switches have shown tremendous potential to reach these goals. However, certain issues are yet to be resolved in GaN technology. First of all, reduction of the fabrication cost is strongly required in order to make GaN cost competitive to state of the art Si switches. Another essential concern is achieving normally-off operation, which avoids the loss of power in stand-by mode operation of power circuits resulting in higher efficiencies. Up to this date, Commercial GaN switches cannot provide the high breakdown voltage and current capacity required in automotive applications. As discussed throughout the thesis, with today's switch ratings, faster switching capability can benefit application such as switch-mode power supplies (SMPS) to reach higher efficiencies. Currently, developing new device structure with the aim of reaching higher ratings is an ongoing area of research.

As for the control strategy of power management systems, complex decision making schemes optimized with methods such as neural network could provide better control over the required net energy and sizing the storage sources while establishing more efficient power split between them. In this thesis, the target design specifications are reached by means of the developed strategy. However, for the future applications, the recovery of the energy as it happens in regenerative braking should be evaluated with this strategy.

Finally, for the fabrication, according to the CMC's process flow of AlGaN/GaN HFET set mask have been designed. Next step could be fabricating the devices and evaluating their performance in terms of breakdown voltage, current capacity and on-

resistance. For various fabrication runs, certain parameters such as field-plate length and insulator thickness can change and results can be verified with the analytical approach.

REFERENCES

[1] D. Yu, Z. Xiaohu, B. Sanzhong, S. Lukic, and A. Huang, "Review of non-isolated bi-directional DC/DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," *IEEE Applied Power Electronics Conference and Exposition*, pp. 1145–1151, 2010.

[2] H. Jain, S. Rajawat, and P. Agrawal, "Comparison of Wide Band Gap Semiconductors for Power Electronics Applications," *International Conference on Recent Advances in Microwave Theory and Applications*, pp. 878–881, Nov. 2008.

[3] M. Khan, G. Simin, S. Pytel, A. Monti, E. Santi, and J. Hudgins, "New Developments in Gallium Nitride and the Impact on Power Electronics," *IEEE Power Electronics Specialists Conference*, pp. 15–26, June 2005.

[4] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide band-gap semiconductors for power devices," *IEEE Trans. Power Elect*., vol. 18, no. 3, pp. 907–914, 2003.

[5] J. Biela, M. Schweizer, S. Waffler, B. Wrzecionko, and J. W. Kolar, "SiC vs. Si - evaluation of potentials for performance improvement of power electronics converter systems by SiC power semiconductors," *Proc. International Conference on Silicon Carbide and Related Materials*, Oct. 2009.

[6] Y. F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," *IEEE Trans. on Electron Devices*, vol. 48, pp. 586–590, Mar. 2001.

[7] H. Ueda, M. Sugimoto, T. Uesugi, and T. Kachi, "Wide-Bandgap Semiconductor Devices for Automobile Applications," *CS MANTECH Conference*, April 2006.

[8] D. C. Dumka, C. Lee, H. Q. Tserng, P. Saunier, and M. Kumar, "AlGaN/GaN HEMT's on Si substrate with 7 W/mm output power density at 10 GHz," *Trans. on Electron Devices*, vol. 40, no. 16, pp. 1023–1024, Aug. 2004.

[9] M. Marz and P. Nance, "Thermal modeling of power electronic systems," *Infineon Technologies AG*, Munich, 1999.

[10] R. Campbell and K. Rajashekara, "Evaluation of power devices for automotive hybrid and 42V based systems," *SAE world congress*, pp. 151–156, 2004.

[11] S. Karmalkar and U. Mishra, "Enhancement of Breakdown Voltage in AlGaN/GaN High Electron Mobility Transistors Using a Field-Plate," *IEEE Trans. on Electron Devices*, vol. 48, no. 8, pp. 1515–1521, Aug. 2001.

[12] N. Ikeda, Li. Jiang, and S. Yoshida, "Normally-off operation power AlGaN/GaN HFET," *Proc. Power Semiconductor Devices and ICs*, pp. 369–372, May 2004.

[13] M. Kamil, "Switch Mode Power Supply (SMPS) Topologies (Part I)," Microchip Corp. Application Notes.

[14] IPP320N20N3G MOSFET Datasheet.

[15] EPC1010 HFET Datasheet.

[16] S. L. Colino and R. A. Beach, "Fundamentals of Gallium Nitride Power Transistors," EPC Application Notes.

[17] R. M. Schupbach and J. C. Balda, "Comparing DC/DC Converters for Power Management in Hybrid Electric Vehicles," *Electric Machines and Drives Conference*, vol. 3, pp. 1369–1374, June 2003.

[18] E. Rogers, "Understanding boost power stages in switch mode power supplies," Texas Instruments Corp. Application Notes.

[19] 1140-561K-RC Datasheet.

[20] PE-92116 Datasheet.

[21] SLPX103M063E9P3 Datasheet.

[22] B41607A8807M002 Datasheet.

[23] S. Lu, K. A. Corzine, and M. Ferdowsi, "A new battery/ultracapacitor energy storage system design and its motor drive integration for hybrid electric vehicles," *IEEE Trans. on Vehicular Technology*, vol. 56, no. 4, pp. 1516–1523, July 2007.

[24] F. S. Garcia, A. A. Ferreira, and J. A. Pomilio, "Control Strategy for Battery-Ultracapacitor Hybrid Energy Storage System," *Applied Power Electronics Conference and Exposition*, pp. 826–832, 2009.

[25] J. Cao and A. Emadi, "A new battery/ultra-capacitor hybrid energy storage system for electric, hybrid and plug-in hybrid electric vehicles," *Proc. IEEE Vehicle Power Propulsion Conference*, pp. 941–946, Sept. 2009.

[26] S. M. Lukic, S. G. Wirasingha, F. Rodriguez, C. Jian, and A. Emadi, "Power management of an ultracapacitor/battery hybrid energy storage system in an HEV," *Proc. IEEE Vehicle Power Propulsion Conference*, pp. 1–6, 2006.

[27] M. Ortuzar, J. Moreno, and J. Dixon, "Ultracapacitor-based auxiliary energy system for an electric vehicle: implementation and evaluation," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2147–2156, Aug. 2007.

[28] L. Gao, R. A. Dougal, and S. Liu, "Power enhancement of an actively controlled battery/ultracapacitor hybrid," *IEEE Transactions on Power Electronics*, vol. 20, no. 1, pp. 236–243, Jan. 2005.

[29] W. Lhomme, P. Delarue, P. Barrade, A. Bouscayrol, and A. Rufer, "Design and

control of a supercapacitor storage system for traction applications," *Industry Applications Conference*, pp. 2013–2020, Oct. 2005.

[30] A. Di Napoli, F. Crescimbini, F. Guilii Capponi, and L. Solero, "Control strategy for multiple input DC/DC power converters devoted to hybrid vehicle propulsion systems," *Proc. IEEE International Symposium on Industrial Electronics*, pp. 1036–1041, May 2002.

[31] L. L. Solero and A. Pomilio, "Design of multiple-input power converter for hybrid vehicles," *IEEE Trans. on Power Electronics*, vol. 20, no. 5, pp. 1007–1016, Sept. 2005.

[32] D. H. Ha, N. J. Park, K. J. Lee, D. G. Lee, and D. S. Hyun, "Interleaved bidirectional DC/DC converter for automotive electric systems," *IEEE Annul Meeting Conference*, pp. 1–5, Oct. 2008.

[33] S. J. Jang, T. W. Lee, W. C. Lee, and C. Y. Won, "Bi-directional dc/dc converter for fuel cell generation system," *Proc. IEEE Power Electronics Specialists Conference*, pp. 4722–4728, 2004.

[34] Y. S. Lee and G. T. Chen, "Quasi-resonant zero-current-switching bidirectional converter for battery equalization applications," *IEEE Trans. on Power Electronics*, vol. 21, no. 5, pp. 1213–1224, Sep. 2006.

[35] Y. S. Lee and S. C. Chu, "EMI Performance Comparison of switched-capacitor bidirectional converter with and without QR ZCS," *PEDS IEEE Conference*, pp. 1137–1142, Nov. 2009.

[36] J. S. Lai and D. J. Nelson, "Energy management power converters in hybrid electric and fuel cell vehicles," *IEEE Trans. on Power Electronics*, vol. 95, no. 4, pp. 766–777,

Apr. 2007.

[37] E. Ozatay, B. Zile, J. Anstrom, and S. Brennan, "Power distribution control coordinating ultra-capacitors and batteries for electric vehicles," *Proc. Control Conference*, vol. 5, pp. 4716–4721, June 2004.

[38] M. B. Camara, H. Gualous, F. Gustin, and A. Berthon, "Design and new control of DC/DC converters to share energy between SCAP and battery in hybrid vehicle," *IEEE Trans. on Vehicular Technology*, vol. 57, no. 5, pp. 2721–2735, Sept. 2008.

[39] M. J. Gielniak and Z. J. Shen, "Power management strategy based on game theory for fuel cell hybrid electric vehicles," *Vehicular Technology Conference*, vol. 6, pp. 4422–4426, Sept. 2004.

[40] G. Wang, P. Yang, and J. Zhang, "Fuzzy optimal control and simulation of battery-ultra-capacitor dual-energy source storage system for pure electric vehicle," *in Intelligent Control and Information Processing Conference*, pp. 555–560, Aug. 2010.

[41] Y. Lu, H. Yuan, Y. Liu, and Q. Wang, "Fuzzy logic based energy management Strategy of battery-ultracapacitor composite power supply for HEV," *Pervasive Computing Signal Processing and Applications Conference*, pp.1209–1214, Sept. 2010.

[42] A. A. Ferreira, J. A. Pomilio, G. Spiazzi, and L. de Araujo Silva, "Energy management fuzzy logic supervisory for electric vehicle power supplies system," *IEEE Trans. on Power Electronics*, vol. 23, no. 1, pp. 107–115, Jan. 2008.

[43] W. Yifeng, Z. Yun, W. Jian, and C. Ning, "Energy management system based on fuzzy control approach for hybrid electric vehicle," *Control and Decision Conference*, pp. 3382–3386, June 2009.

[44] L. Rosario and P. Luk, "Implementation of a modular power and energy management structure for battery–ultracapacitor powered electric vehicles," *Proc. of the Hybrid Vehicle Conference*, pp. 141–56, 2006.

[45] A. C. Baisden and A. Emadi, "ADVISOR-based model of a battery and an ultracapacitor energy source for hybrid electric vehicles," *IEEE Trans. on Vehicular Technology*, pp. 199–205, 2004.

[46] U.S. Environmental Protection Agency, "Dynamometer Driver's Aid," *Testing and Measuring Emissions*, 2007. [Online]. Available: www.epa. gov/nvfel/testing/dynamometer.htm

[47] L. H. Dixon, "Control loop cookbook," *Unitrode Power Supply Design Seminar*, pp. C4-1–C4-26, 1997.

[48] J. Strydom, "Driving eGaNTM FETs," Efficient Power Conversion Corp. Application Notes.

[49] J. Strydom and B. White, "High Step-Down Ratio Buck Converters With eGaN Devices," *How to power newsletter*, Nov. 2010.

[50] N. Garcia, "The Effects of Increasing Frequency on Magnetic Components," Renco Electronics Corp. Application Notes, No. APN-100.

[51] R. Quay, Gallium Nitride Electronics, Springer-Verlag, 2008.

[52] A. Brannick, N. Zakhleniuk, B. Ridley, J. Shealy, W. Schaff, and L. F. Eastman, "Influence of Field-Plate on the Transient Operation of the AlGaN/GaN HEMT," *IEEE Trans. On Electron Devices*, vol. 30, no. 5, pp. 436–438, May 2009.

[53] Y. Dora, Understanding material and process limits for high breakdown voltage AlGaN/GaN HEMTs, PhD thesis, University of California, Santa Barbara, 2006.

[54] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of Dynamic On-Resistance Increase and Gate Charge Measurements in High-Voltage GaN-HEMTs With Optimized Field-Plate Structure," *IEEE Trans. on Electron Devices*, vol. 54, no. 8, pp. 1825–1830, Aug. 2007.

[55] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. DenBaars, and U. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaN HEMTs with Integrated Slant Field-Plates," *IEEE Trans. On Electron Devices*, vol. 27, no. 9, pp. 713–715, Sept. 2006.

[56] S. Yagi, M. Shimizu, M. Inada, Y. Yamamoto, G. Piao, H. Okumura, Y. Yano, N. Akutsu, and H. Ohashi, "High breakdown voltage AlGaN/GaN MIS–HEMT with SiN and TiO2 gate insulator," *Solid State Electron.*, vol. 50, no. 6, pp. 1057–1061, June 2006.

[57] W. Huang, S. Zhang, and J. Xu, "High-Breakdown Voltage Field-Plated Normally-off AlGaN/GaN HEMTs for Power Management," *IEEE Conference on Solid-State and Integrated Circuit Technology*, pp. 1335–1337, Nov. 2010.

[58] E. Bahat-Treidel, O. Hilt, F. Brunner, V. Sidorov, J. Wurfl, and G. Trankle, "AlGaN/GaN/AlGaN DH-HEMTs breakdown voltage enhancement using multiple grating field-plates (MGFPs)," *IEEE Trans. on Electron Devices*, vol. 57, no. 6, pp. 1208–1216, June 2010.

[59] S. Karmalkar, M. Shur, G. Simin, and M. Khan, "Field-plate engineering for heterostructure field effect transistors," *IEEE Trans. on Electron Devices*, vol. 52, no. 12, pp. 2534–2540, Dec. 2005.

[60] S. Karmalkar and U. Mishra, "Enhancement of Breakdown Voltage in AlGaN/GaN High Electron Mobility Transistors Using a Field-Plate," *IEEE Trans. on Electron*

Devices, vol. 48, no. 8, pp. 1515–1521, Aug. 2001.

[61] N. Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. DenBaars, and U. K. Mishra, "High Breakdown GaN HEMT with Overlapping Gate," *IEEE Trans. on Electron Devices*, vol. 21, no. 9, pp. 421–423, Sept. 2000.