# EMTP-RV Simulation of a Chain Link STATCOM

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# ABSTRACT

## EMTP-RV Simulation of a Chain Link STATCOM

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An advanced static VAr compensator (ASVC), using a voltage-source-converter (VSC), popularly known as a static synchronous compensator (STATCOM), is generally acknowledged as the next-generation reactive power controller in power systems. Its mode of operation is analogous to that of a rotating synchronous condenser and it provides dynamic voltage compensation, increased transient stability and damping for the power system. Several STATCOMs, based on high power semiconductor switches (e.g. Gate Turn Off thyristors, GTOs or Insulated Gate Bipolar Transistors, IGBTs) and a special zigzag transformer have been put into operation. These STATCOMs have advantages over conventional static VAr compensators (SVCs) of lower harmonic generation, improved performance and a smaller reactor size. However, the zigzag transformers used in these STATCOMs are bulky, expensive and as yet unreliable. An alternative method to eliminate the zigzag transformer and to increase the STATCOM rating with a corresponding reduction in harmonics is to use a multilevel converter, which produces a 'multi-stepped' output voltage waveform in a close approximation to a sine wave.

A recent addition to the multilevel converter based STATCOM family has been obtained by connecting a number of VSCs in series on the ac side of the system forming a 'chain' per phase. Each VSC is a 1-phase, full-bridge converter and forms a 'link' of a

'chain'. This STATCOM configuration is referred to as a 'Chain Link STATCOM' (CLS). In this thesis, a GTO is used as a switch for the CLS. However, any other high power semiconductor switch (e.g. IGBT) may also be used instead. Each GTO of the CLS, is switched on/off only once per cycle of the fundamental frequency by employing a sinusoidal pulse width modulation (SPWM) technique. Approximate models of a 3-phase CLS using *dq*-transformation are derived to design two cascaded controllers for controlling reactive current and ac voltage to stabilize the power system voltage at the point of common coupling (PCC). A novel technique, called the rotated gate signal pattern (RGSP), is used for balancing the voltages of the link dc capacitors of the VSC. The performance investigation of the CLS system when used in a radial line transmission system is carried out under steady- and transient-state operating conditions by means of the simulation package EMTP-RV.

**Index terms:** Chain link STATCOM, VSC, SVC, STATCOM, FACTS, EMTP-RV.

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Above all, my parents, brother, sister, my in-laws and especially my wife Elsa, for providing me constant moral support, inspiration, encouragement and assistance to complete this research project.

With love, praise and honour, I dedicate this thesis to my family.

Nikunj M. Shah

**to my family…..**

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| | |
|---|---|
| ASVC | Advanced Static VAr Compensator |
| CLC | Chain Link Converter |
| CLS | Chain Link STATCOM |
| CSC | Current Source Converter |
| EMTP | Electro-Magnetic Transient Program |
| FACTS | Flexible AC transmission System |
| FC | Fixed Capacitor |
| GTO | Gate Turn-off Thyristor |
| IGBT | Insulated Gate Bipolar Transistor |
| IGCT | Integrated Gate-commutated Thyristor |
| NGC | National Grid Company |
| PCC | Point of Common Coupling |
| PWM | Pulse width Modulation |
| RGSP | Rotated Gate Signal Pattern |
| SSSC | Static Synchronous Series Compensator |
| STATCOM | Static Synchronous Compensator |
| SVC | Static VAr Compensator |
| TCR | Thyristor Controlled Reactor |
| TCSC | Thyristor-controlled Series Capacitor |
| TSC | Thyristor Switched Capacitor |
| TSSC | Thyristor Switched Series Capacitor |
| VSC | Voltage Source Converter |

# CHAPTER-1

# INTRODUCTION

## 1.1. GENERAL

The modern power supply system is widely interconnected for economic reasons, to reduce the electricity cost and to improve reliability of the power supply. It comprises of many generating stations, transmission lines, loads, controllers and telecom links. Such an interconnected network, while bearing many advantages, suffers from large voltage, frequency and power excursions because of sudden load changes, faults and controller actions, which occur locally and/or remotely. In the worst case, these excursions, if not dampened, may result in the collapse of the power system. Therefore, it is essential to balance the supply and demand of active and reactive power in an electric power system.

The electrical power transmitted in an ac power system depends upon the transmission line voltage profile under steady state and dynamic conditions, over a wide range of network contingencies. Therefore, it is desirable to regulate the voltage within a narrow range (+5%, -10% in most utilities) of its nominal value. Appropriate voltage and reactive power control is one of the most important factors of stable power system operation.

## 1.2. REACTIVE POWER COMPENSATION [1-4]

As transmission & distribution lines, transformers, generators etc., have mainly inductive impedance at line frequency, the internal impedance of the ac system seen by the load is mainly inductive. Hence, reactive power appears in every ac power system.

Therefore, it is the reactive power change in the power system that has the most adverse effect on the voltage regulation.

Moreover, with a long-distance ac power transmission and load growth, the reactive power increases the transmission system losses, reduces the power transmission capability of the transmission lines and causes large amplitude variations in the power system voltage & consequently power oscillations. Therefore, by controlling the reactive power (VAr) flow in the line, the voltage profile along the transmission line can be controlled in a more effective way. Furthermore, the reactive power compensation increases the utilization of the existing transmission systems and improves the system damping and stabilizes the power systems.

## 1.2. METHODS OF REACTIVE POWER COMPENSATION [1-8]

### 1.2.1. General [1-4]

Contrary to the active power balance, which has to be affected by the generators alone, a proper reactive power balance can and often has to be affected both by the generators and by dispersed special reactive power devices capable of producing and absorbing reactive power. The use of shunt devices i.e. shunt compensation, is a classic reactive power compensation method. The use of series capacitors i.e. series compensation, is a 'line reactance compensation' method. As the series compensation method is not in the scope of this thesis report, only the shunt compensation methods for the reactive power compensation will be discussed next in brief.

### 1.2.2. Conventional methods [1-4]

No special reactive compensation devices were used in the early ac power systems, because the generators were situated close to the loads. As the network became more

widespread synchronous motors, small synchronous compensators and static shunt capacitors were adopted for reactive compensation. In the transmission system, larger synchronous compensators (or synchronous condensers) were installed. The synchronous compensators produce high capacitive output currents even at the low system voltages and do not generate harmonics that resonate with the grid. However, they are vulnerable to rotating instability, have slow response with low short circuit impedance, and have high maintenance cost.

Along with the development of more efficient and economic capacitors, there has been a phenomenal growth in the use of shunt capacitors as a means of furnishing reactive power, particularly within distribution systems. With the introduction of the extra-high voltage (EHV) lines, large banks of mechanically switched or fixed capacitors/reactors have been important compensation devices to maintain the supply voltage and increase the steady state power of the line by 'reactive power compensation'. At regular intervals along the transmission line, the reactors are installed in shunt along with the large capacitors in series or parallel. However, with the fixed capacitor configuration using mechanical switches, continuous control of reactive power cannot be achieved. Also the switches have slow response time, are bulky, expensive and require maintenance.

### 1.2.3. Static VAr Compensators (SVCs) [1-4]

The development of high power solid-state devices such as thyristors, opened up a new era of control techniques in power transmission systems. Using these solid-state switches, shunt, series or shunt and series connected systems were employed in power

systems for reactive power compensation. More detailed explanation of these methods is given in [1-4].

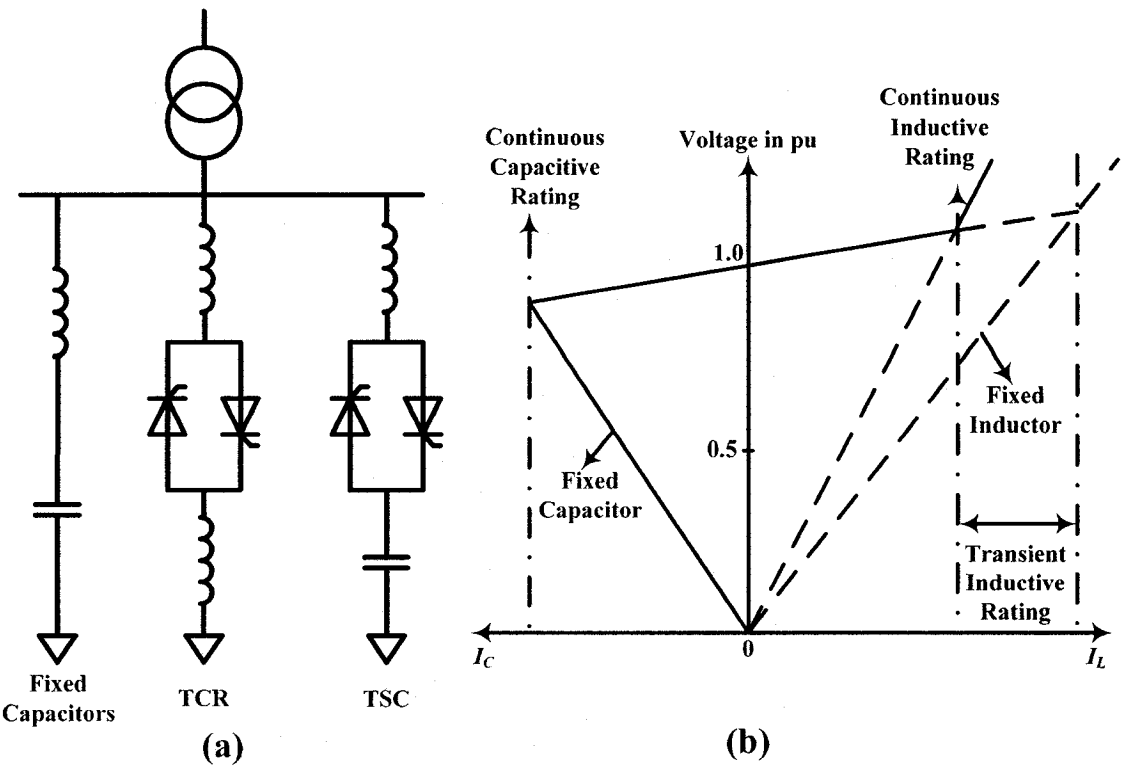


**Figure 1.1. (a) Conventional SVC System, and its (b) V-I characteristic.**

A 'Static VAr compensator' (SVC) is a member of the Flexible AC Transmission Systems (FACTs) family which uses solid-state power electronic devices to control the power flow on power grids. A SVC regulates voltage at its terminal by controlling the amount of reactive power injected into or absorbed from the power system. When the system voltage is low, SVC operates in capacitive mode and generates reactive power. Whereas, when the system voltage is high, SVC operates in the inductive mode and absorbs reactive power to maintain the system voltage at the desired level.

The SVCs were first developed in the late 1960s to prevent annoying voltage flicker caused by large industrial fluctuating loads, such as electric arc furnaces, which cause rapid changes in the reactive power and also introduce phase unbalance. Since then, they have been extensively used in the power transmission networks for the dynamic compensation of the electric power to achieve better utilization of existing generation and transmission facilities and to provide the voltage support. Thyristor controlled reactors (TCRs) and thyristor switched capacitors (TSCs) have gained significant market share due to their relatively fast speed of operation low maintenance requirements and low cost.

Conventional SVCs employ large banks of shunt connected fixed capacitors, TSRs and TSCs to provide the desired controlled shunt reactive power compensation (Figure 1.1a). In such installations, ac capacitors are used as the VAr source, and shunt connected phase controlled reactors are used to absorb VArs. The net reactive power is the difference between the two. A coupling transformer matches the SVC to the transmission line voltage. In some installations two transformers are used with an increased pulse number to reduce harmonic distortion and to provide improved dynamic response [5].

SVC possesses certain disadvantages such as,

- Higher harmonic generation,
- Lower dynamic range,
- Limitations of operations with weak ac system, and
- As it acts as a variable susceptance, it is sensitive to the transmission system harmonic resonance (Figure 1.1b).

### 1.2.4. Advanced Static VAr Compensators (ASVCs) or Static Synchronous Compensators (STATCOM) [1, 2, 4-8]

With the development of new-generation, high-performance, high-power forced-commutated semiconductor switches such as gate turn-off thyristors (GTOs) and insulated gate bipolar junction transistors (IGBTs), the possibility of generating or absorbing controllable reactive power with various power electronics switching converters has long been recognised, and several candidate schemes have been implemented in laboratory models. These converters do not require large capacitor or phase controlled reactor banks to produce reactive power. They operate as alternating voltage or current sources (i.e. voltage-sourced inverter, VSI and current-sourced inverter, CSI) and produce reactive power essentially by circulating energy between the phases of the ac system. The inverters (or converters) for the transmission line application, require semiconductor power switches with the high voltage and current ratings and moreover, the switches must be capable of turning off in response to a gating command. The CSI implementation requires power switches with symmetrical bidirectional voltage blocking capability, while VSI requires only unidirectional voltage blocking.

The voltage sourced inverter or converter (VSI or VSC) based shunt-connected SVC system is known as an advanced SVC (ASVC) or more popularly a static synchronous compensator (STATCOM). The capability of the STATCOM is analogous to a rotating synchronous compensator, and can be used in the power systems, for the dynamic compensation, increasing the transient stability and providing the voltage

support. The basic principle of operation of the STATCOM is briefly explained next along with its significant advantages as compared to conventional shunt connected SVC.

### *(a) Principle of operation of STATCOM (or ASVC)* [1, 2, 4-8]

The major elements of a STATCOM are a VSC, a dc capacitor ($C_{dc}$) and a transformer to match the inverter to the line voltage. In this STATCOM application, a four quadrant VSC converts a dc voltage at its input terminals into 3-phase set of output voltages synchronized with and connected to the ac line through a small buffer or tie reactance, which is the leakage reactance of a transformer. The basic principle of operation of a STATCOM is illustrated in Figure 1.2.

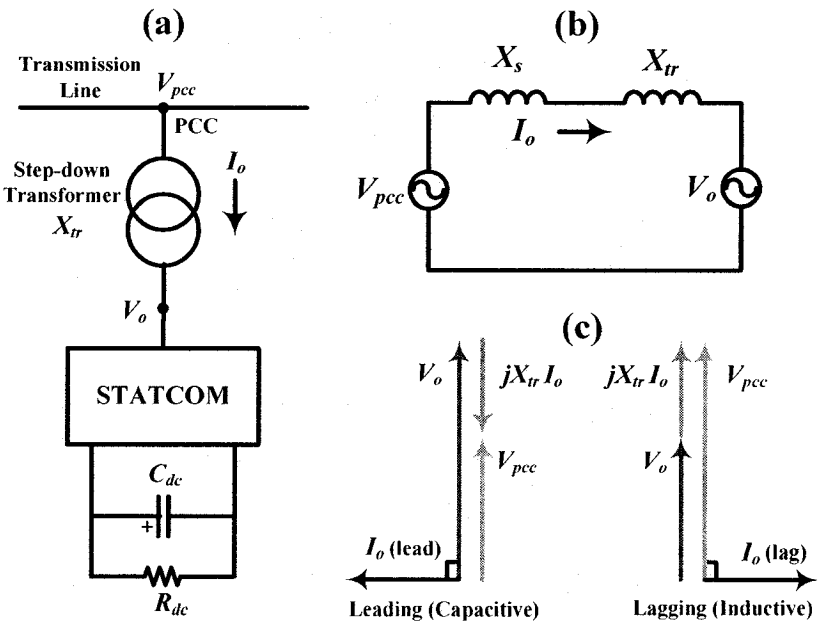


**Figure 1.2. (a) Single line diagram of the STATCOM system, (b) Simplified equivalent circuit of a STATCOM connected to the AC system, and (c) Phasor diagrams.**

As shown in Figure 1.2b, a simplified representation of the ac system is a Thevenin equivalent of voltage at the point of common coupling (PCC), $V_{pcc}$ behind a reactance *Xs*. A STATCOM VSC can be considered to generate a 'back-emf' represented by its

fundamental component of the converter output voltage, $V_o$ connected via transformer leakage reactance, $X_{tr}$ to the ac system at the PCC.

By using a suitable closed-loop control system, $V_o$ is controlled to be in phase with $V_{pcc}$ and therefore the current, $I_o$ flowing between the PCC and STATCOM is ideally purely reactive, which is given by:

$$I_o = \frac{V_{pcc} - V_o}{j(X_s + X_{tr})} \tag{1.1}$$

The back-emf ($V_0$) is directly related to the dc side voltage of the STATCOM, which can be controlled by the closed loop control system to enable the STATCOM to draw leading or lagging reactive current ($I_o$) from the ac line. When $V_o$ is higher than $V_{pcc}$, leading $I_o$ is drawn from the ac line (or reactive power is supplied to the line) and when $V_o$ is lower than $V_{pcc}$, lagging $I_o$ is drawn from the ac line (or reactive power is absorbed from the line) (Figure 1.2c). In this respect, the operation of the STATCOM is similar to that of a synchronous condenser. The transient response of STATCOM, however, is significantly better.

As explained earlier, ideally the line current is purely reactive therefore, no real power is required. In practice, as the semiconductor switches in the converter are not loss less, some real power is required to compensate for the converter losses. These losses are dissipated in the resistor ($R_{dc}$) in parallel with $C_{dc}$. Because of these internal losses in the STATCOM converter, the dc capacitor voltage would diminish. However, these losses may be supplied from the ac line by adjusting the output voltage of the STATCOM converter to lag the line voltage by a very small angle (usually in the range of 1° to 3°). By compensating the converter losses in this way, continuous real power is not required from the dc source and no separate power supply is needed. The dc capacitor is only

required to maintain smooth dc voltage while carrying the ripple current drawn by the converter. Usually, the converter reactive current is controlled by increasing or decreasing the magnitude of the STATCOM output voltage, which in turn can be achieved by increasing or decreasing the magnitude of the dc voltage by adjusting the phase angle of the STATCOM output voltage. So in addition to the losses, some real power flows in or out of the dc capacitor, as required.

The reactive and active power exchange between the STATCOM and the ac system can be controlled independently of each other, and any combination of real power generation or absorption with VAr generation (supply or –Q) or absorption (+Q) is achievable, if the STATCOM is equipped with an energy storage device of suitable capacity for example, a battery.

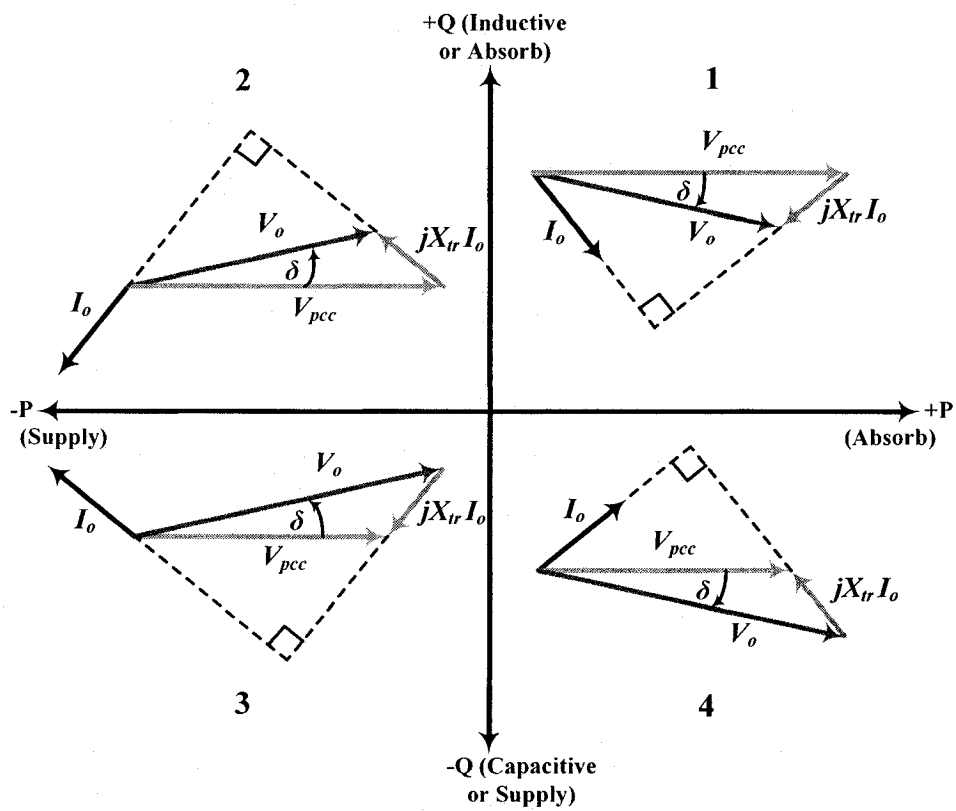


**Figure 1.3. Phasor diagrams for power exchanges in a STATCOM.**

Figure 1.3 illustrates the phasor diagrams of the power system voltage at the point of common coupling ($v_{pcc}$), the STATCOM output current ($i_o$) and out voltage ($v_o$) in all four quadrants of the PQ plane. As stated, for a STATCOM, 2nd and 3rd quadrant operation (i.e. supply of active power) is possible only with a separate dc source (i.e. battery) on its dc side. With this capability, extremely effective control strategies for modulation of the reactive and active output power can be devised to improve transient and dynamic stability limits.

### *(b) V-I characteristic of STATCOM* [1, 2, 4-8]

A typical V-I characteristic of a STATCOM is depicted in Figure 1.4. As can be seen, the STATCOM can supply both capacitive and inductive compensation and is able to control its output current over the rated maximum capacitive or inductive range independently and irrespective of the amount of the ac system voltage. In practice, the minimum value of the voltage at which the STATCOM can produce the rated output is dependent on the tie or buffer reactance of the coupling transformer (typically 0.2 pu). Figure 1.4 also illustrates that the STATCOM has an increased transient rating in both the capacitive and inductive operating regions. The maximum attainable transient over-current in the capacitive region is determined by the maximum current turn-off capability of the converter switches. However, in the inductive region, the converter switches are naturally commutated and therefore the transient current rating is limited by the maximum allowable junction temperature of the converter switches.

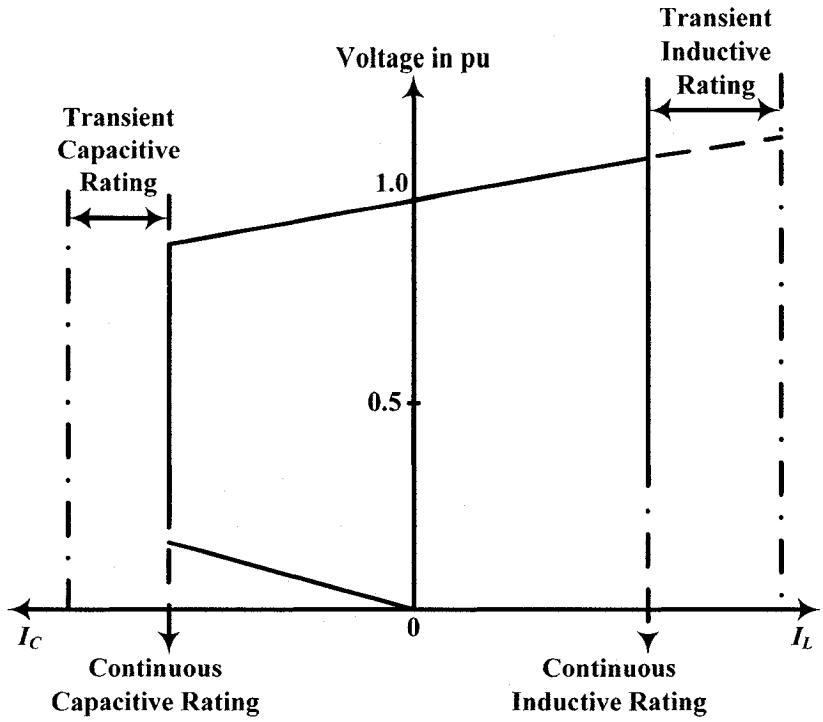


**Figure 1.4. V-I characteristic of STATCOM.**

### *(c) Conventional STATCOM circuit using 3-phase VSC* [1, 2, 4-8]

As stated earlier, the basic building block of the STATCOM is a 3-phase VSC which consists of six self commutated semiconductor switches (i.e. here GTOs) with anti-parallel freewheeling diodes (Figure 1.5). With a dc voltage source (i.e. a charged capacitors), VSC can produce a balanced set of three quasi-square voltage waveforms of a given frequency by connecting the dc source sequentially to the three output terminals via the appropriate VSC switches. As the quasi-square output voltage waveform produces unacceptable current harmonics when connected to a line, a single 3-phase VSC bridge arrangement cannot be used as a STATCOM [5-7]. Therefore, a STATCOM uses many such VSC appropriately phase shifted, with their outputs combined electro-magnetically to produce nearly sinusoidal resultant voltage waveform. This arrangement also results in increased STATCOM rating.

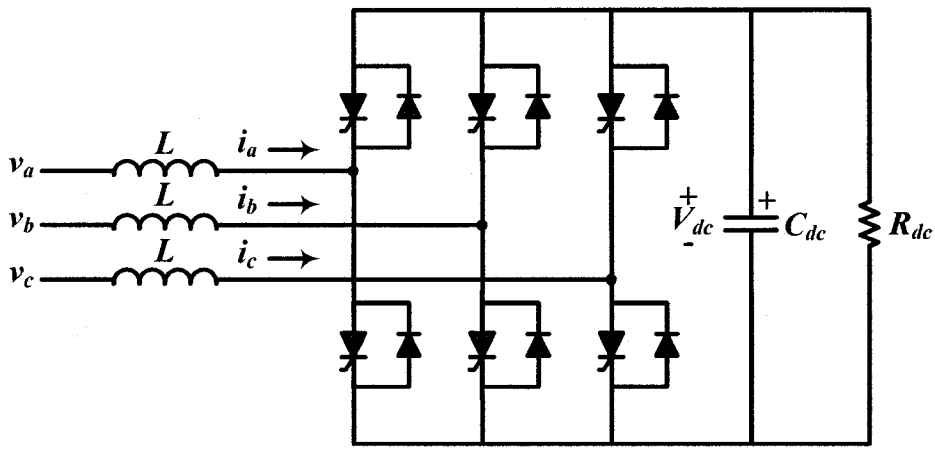


**Figure 1.5. Conventional 3-phase 6-pulse VSC based STATCOM circuit.**

### *(d) Advantages of STATCOM over SVC* [1, 2, 5]

The ASVC or STATCOM has many advantages over the conventional SVC which are summarized as follows:

- Continuous and precise power control.
- Improved performance with a larger dynamic range.
- Increased transient stability & improved damping.
- Improved performance and improvement in the obtainable VAr output at low operating voltages. A STATCOM is capable of generating 1 pu of reactive current at line voltage down to the pu value of the tie reactance and hence (Figure 1.4). This ability to support the line is better than that obtained with conventional SVC because the current in the capacitors falls in proportion to the voltage (Figure 1.1b).
- The switches used in the STATCOM are well protected against the over voltages by the clamping action of the dc capacitor.
- The VAr output inherently adjusts to compensate for voltage variations.

- Because the current carrying capacity of the VSC switches (e.g. GTO) is high in the naturally commutated mode, the switches may be utilized to a higher proportion of their current rating when an over voltage transient is experienced and lagging reactive power is required.
- Lower harmonic generation.
- Reduction in size and weight, due to the reduction in the passive component count and the size of the remaining passive components.
- Insensitivity to transmission system harmonic resonance as it acts as a voltage source behind a reactance.
- Reduction in the cost as compared to the conventional SVC, has been realized in production as the technology of the high power switches became matured.

*(e)* ***Limitations of conventional 3-phase VSC based STATCOM*** **[1, 2, 5, 6, 8, 10]**

As stated earlier, a simple 3-phase VSC arrangement is not suitable as STATCOM circuit because of its poor harmonic performance and limited rating [1, 5, 10]. For high-power high-voltage applications, the total VAr rating could be increased by connecting the switches either in series or parallel; however this would not improve harmonic performance and introduces problems associated with voltage and/or current sharing.

Increased VAr rating can also be achieved by using multiple 3-phase bridges and phase-shifting transformers [1, 5, 6]. The 3-phase bridges can be connected in parallel on the dc side and the converters may incorporate series-connected GTOs and diodes to achieve higher ratings. The converter transformers are usually arranged to make bridges appear in series when viewed from the ac side [5, 6]. By arranging the phase shift

between the bridge transformer windings (i.e. using zigzag transformer), selected harmonics can be cancelled to give a multi-pulse arrangement (e.g. 24 or 48-pulse) under balanced conditions. With this method, it is not practicable to connect the series-connected transformer primaries directly to the high voltage power system, and a further fully rated step-down transformer is required for this purpose. For example, the 48-pulse STATCOM arrangement consists of eight VSCs connected together through eight zigzag transformers using the harmonic cancellation technique. These transformers,

- Are the most expensive equipment in the system;
- Produce about 50% of the total losses of the system;
- Occupy up to 40% of the total system's space, which is an expensive large area;
- Cause difficulties in control due to dc magnetizing and inrush current problems resulting from saturation of the transformers in transient states; and
- Are prone to failures.

Pulse width modulation (PWM) can also be applied to cancel selected harmonics. However, increasing the number of switching operations of the converter switches per cycle increases the switching and snubber losses, increases high frequency harmonics and reduces the fundamental VAr rating.

### 1.2.5. Multilevel converters and their problems [1, 8]

To solve the above mentioned problems associated with the conventional 3-phase VSC based STATCOM arrangement, to increase the VAr rating and to reduce the harmonics, a 'multilevel' converter is used; which produces a 'multi-stepped' output voltage waveform. These multilevel converters eliminate the transformers required in the

conventional 3-phase 6-pulse VSC based STATCOM; however they encounter new problems as explained next.

In recent years, a relatively new type of converter - multilevel voltage source converter - has attracted many researchers' attention. Multilevel converters operate at high voltage and reduce harmonics by their inherent structures without transformers, a benefit that many contributors have been trying to exploit for high-voltage, high-power applications especially for flexible ac transmission system (FACTS) controllers. Several multilevel converter topologies have been developed to demonstrate their flexibility in such applications.

***(a) Diode clamp multilevel converter* [1, 8, 10]**

Figure 1.6 shows the structure of a 5-level diode-clamp converter. In this circuit the single energy storage capacitor of the conventional 3-phase VSC bridge circuit (Figure 1.5) is replaced by several capacitors stacked directly in series, and the basic switch per bridge arm (i.e. one GTO plus one anti-parallel diode of Figure 1.5) is changed to several switches in series coupled to the capacitor stack via auxiliary/clamping diodes. A stack of $M$ capacitors produces ($M$ +1) level symmetrical voltage waveform per phase, which gives increased VAr rating and a better approximation to a sine wave than the basic 3-phase VSC bridge. This converter can reach good performance without transformers [8]. For the 5-level converter, D1, D2, and D3 need to block $V_{dc}$, $2V_{dc}$ and $3V_{dc}$, respectively, assuming each dc capacitor has the same dc voltage, $V_{dc}$. When diodes are selected to have the same voltage rating as the main switching devices, D2 and D3 comprise of two and three auxiliary diodes in series, respectively, to withstand the voltage. Therefore, the number of the additional auxiliary/clamping diodes is equal to ($M$ - 1) x ($M$ - 2) x 3 for an

$M$-level converter. Therefore, the main disadvantage with this circuit is that the total number of auxiliary diodes increases rapidly as the number of levels increase. For example, if $M = 51$ (for direct connection to 69 kV power lines), then the number of the auxiliary diodes will be 7350. Consequently, in practice a maximum of 9-levels (eight capacitors) is probably the economic limit. This gives a relatively low maximum 3-phase bridge rating of the order of ±20MVAr.

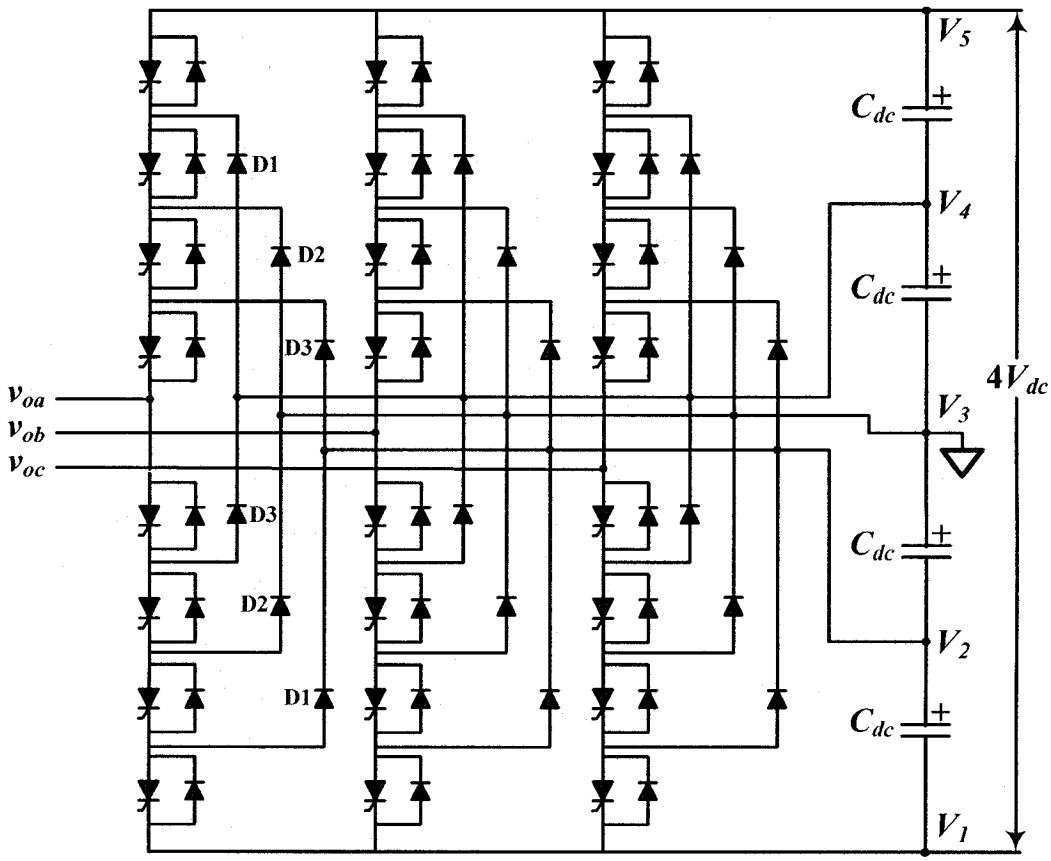


**Figure 1.6. 3-phase 5-level diode clamp converter.**

### *(b) Flying-capacitor multilevel converter* [1, 8, 10]

The multilevel flying-capacitor converter is supposed to be able to solve the problems of voltage unbalance and excessive diode count of the diode clamped converter.

Figure 1.7 shows the configuration of a 5-level flying-capacitor converter. In this converter, however, a large number of flying capacitors are needed. The required number of flying capacitors for an $M$-level converter is equal to ($M$ - 1) x ($M$ - 2) x 3/2 + ($M$ - 1), provided that the voltage rating of each capacitor used is the same as the main power switches. With the assumption of the same capacitor voltage rating, an $M$ -level diode clamped converter requires only ($M$ - 1) capacitors. Therefore, the flying capacitor converter requires large capacitance compared with the conventional 3-phase VSC bridge. In addition, control is very complicated, and higher switching frequency is required to balance each capacitor voltage.

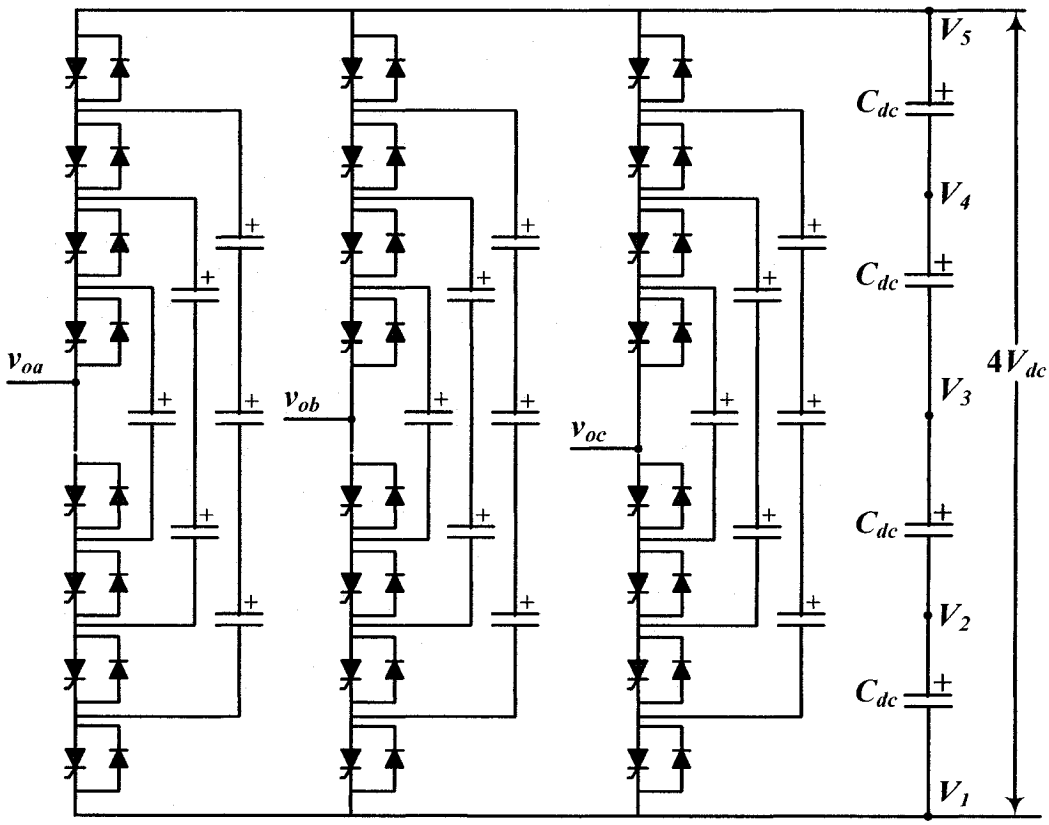


**Figure 1.7. 3-phase 5-level flying capacitor converter.**

### *(c) Chain Link Converter (CLC)* [1, 10-15]

A relatively new multilevel converter configuration has been developed by connecting a number of VSCs in series to form a chain; this configuration is known as a Chain link converter (CLC). A CLC based STATCOM known as Chain Link STATCOM (CLS), is proposed here. It has significant advantages compared with the other aforementioned known arrangements of the STATCOM. These include good harmonic performance, fast response, low losses and low cost. Moreover, the packaging and physical layout is much easier due to its modular structure. This arrangement of the STATCOM is relatively new and not well understood due to its limited number of applications for commercial use. The first and so far only, CLS application has been in service in the National Grid Company, East Claydon substation, UK.

This special type of STATCOM eliminates the excessively large number of,

- Bulky transformers required by conventional multipulse converters,
- Clamping diodes required by multilevel diode-clamped converters, and
- Flying capacitors required by multilevel flying-capacitor converters.

Also, some of its important features are:

- It switches each device only once per line cycle and generates a multi-stepped staircase voltage waveform approaching a pure sinusoidal output voltage by increasing the number of levels.
- Since the converter structure itself consists of a chain connection of many 1-phase, full-bridge VSC units and each bridge is fed with a separate dc source, ideally it does not require voltage balance (sharing) circuits or voltage matching of the switching devices.

- Packaging and layout is much easier because of the simplicity of structure and lower component count and hence it is much more suitable to high-voltage, high-power applications than the conventional converters.

The basic principles of operation, along with the main features and advantages & disadvantages of the CLS circuit, are explained in Chapter 2.

## 1.3. EMTP-RV: OVERVIEW [1]

EMTP-RV is an acronym of the "Electro-Magnetic Transient Program - Restructured Version", which is the circuit-based power system simulation software used for the simulation study of the CLS system in this thesis. EMTP-RV is the end result of the "EMTP Restructuring project" undertaken by the Development Coordination Group (DCG) in 1998 for modernizing the EMTP96 software. EMTP-RV is the enhanced computational engine and EMTPWorks is its new graphical user interface (GUI).

This package is a sophisticated computer program for the simulation of electromagnetic, electromechanical and control systems transients in multiphase electric power systems. It features a wide variety of modeling capabilities encompassing electromagnetic and electromechanical oscillations ranging in duration from microseconds to seconds. Examples of its use include switching and lightning surge analysis, insulation coordination, shaft torsional oscillations, ferroresonance and power electronics applications in power systems.

## 1.4. LITERATURE REVIEW

As the thesis is mainly concentrated on the shunt connected VSC based ASVCs (i.e. STATCOM) used as the FACTS controllers [2], a brief literature review on this topic is presented below.

In late 1970's, L. Gyugyi proposed the controlled reactive power compensation using conventional thyristor based shunt connected SVCs to increase the utilization of the existing transmission systems, to stabilize the power system, to improve the damping and to regulate the steady state value of the voltage and introduced several possible approaches including VSC, CSC and unrestricted frequency converter (UFC) using fully controlled power devices to generate and absorb reactive power without requiring large banks of capacitors or phase controlled reactors [2, 4]. N. Hingorani first defined the concept of FACTS in 1988 as high power electronics and flexible ac transmission system [2]. C.W. Edwards, K.E. Mattern, E.J. Stacy, P.R. Nannery and J. Gubernick proposed the prototype VSC using GTO thyristors as power devices, for evaluation in 1988 [5]. C. Schauder and H. Mehta developed a mathematical model of a VSC with direct and indirect controllers by using Park's transformation in 1991 [22]. Based on a Ph d project, D.R. Trainer, S.B. Tennakoon and R.E. Morrison presented the analysis of the 6-switch and 12-switch voltage-sourced GTO SVC circuits and derived the equations to describe the performance of each circuit in 1995. Under the EPRI sponsored FACTS program, C. Schauder, M. Gernhardt, E. Stacey, T. Lemark, L. Gyugyi, T.W. Cease and A. Edris developed the first world's largest prototype STATCOM of rating ±100 MVAr, which was installed in the Tennessee Valley Authority (TVA) Sullivan substation [7]. After the introduction of the multilevel converters-a new breed of power converters in 1996 by J.S. Lai and F.Z. Peng [8], in 1998, J.D. Ainsworth, M. Davis, P.J. Fitz, K.E. Owen and D.R. Trainer introduced a chain link converter based SVC with significant advantages over the multipulse conventional & multilevel converters [1, 10]. Several papers have been published mentioning the successful commissioning of as yet only one prototype

installation of the CLC based STATCOM of rating ±75 MVAr in the National Grid Company, East Claydon Substation, UK [11-15]. Only a few papers have been published that explained the basic principle of operation of the similar topology named as cascaded converters and investigated its application for the voltage support in the transmission line [20, 21, 23, 24] along with its gating strategy using phase shifted triangular carrier based PWM [16, 18]. Several articles on the conventional STATCOM have been published to investigate the controller function and to increase the efficiency of the converter's power circuit in order to reduce the losses and improve the quality of the output voltage [1-3, 25-27]. Moreover, many installations of the conventional STATCOM applications exist [1-3]. Much research has been done after developing the basic theory of a shunt connected VSC based FACTS controller [1-3]. A Chain Link STATCOM (CLS) is relatively new topology and less published research is available on it with only one prototype installation [1, 10]. Much more research is required on the CLS to fully exploit its advantages for its applications in power systems.

## 1.5. SCOPE AND CONTRIBUTION OF THIS THESIS

As mentioned in the preceding section, there are only a few publications [10, 20, 21, 23, 24] on the CLS and moreover, the information therein is insufficient for further research to exploit the advantages and applications of the CLS. Therefore, this thesis mainly investigates the theory of the CLS and develops its static & dynamic models, control philosophies and the simulation models for its application to support the voltage in the power system by carrying out the simulation in EMTP-RV.

- A basic principle of operation of a 7-level CLS using a 1-phase, full bridge, 3-level VSC as its basic building block is explained first. For the first time, an

SPWM gating technique utilizing multilevel triangular carrier signals and only one modulating signal (per phase), is proposed for the CLS along with the harmonic analysis of the multi-stepped CLS output voltage using the Double Fourier Series (DFS) method. In contrast with the fixed angle switching method (in which the switching angles are obtained by solving transcendental equations governing the modulating signals and carrier signals) used in the NGC's CLS application [1, 10], this SPWM gating strategy is simpler to use and easier to analyse using Double Fourier Series (DFS) method without any need of knowing the switching angles. Moreover, using the proposed SPWM gating strategy, each CLS switch is turned on/off only once per cycle of the line frequency which also minimizes the switching losses.

- EMTP-RV simulation model of the CLS system is proposed using its basic building blocks for the power and gating circuits. Approximate static and dynamic models of the CLS system are developed using *dq*-transformations and evaluated to verify the stability of the CLS system.
- A novel control technique called the Rotated Gate Signal Patterns (RGSP), is proposed to balance the dc capacitor voltages of the CLS. A step-by-step start-up procedure for the CLS system is also proposed to bring its reactive power output to a certain level in a short time, while maintaining all the switching devices within their ratings.
- A 3-phase 3-link 4 MVA, 15 kV delta connected CLS is modeled in EMTP-RV to support the voltage at the PCC. Considering only the phase angle of the CLS output voltage as the control input (i.e. selecting constant modulation index), a

closed-loop control strategy is proposed using two cascaded controllers (i.e. outer or ac voltage controller and inner or reactive current controller) and their approximate first-order transfer functions are derived. The dynamic performance of the proposed CLS with the controllers is studied and also verified by simulations in EMTP-RV. Several simulation tests are carried out to validate the operation of the CLS to regulate the power system voltage at the PCC by reactive power compensation, and the results are presented.

## 1.6. THESIS OUTLINE

The outline of the thesis is as follows:

Chapter 2 explains the theory of the CLS including its basic principle of operation, gating strategy and harmonic analysis of its output voltage using DFS method. It also depicts important features of the CLS along with its advantages and limitations. The basic layout and key design features of the only existing application of the CLS, at the NGC's East Claydon Substation, is also explained in this chapter.

In Chapter 3, the EMTP-RV model of the CLS system is developed using its basic building blocks viz. a switch model, VSC link model and SPWM circuit model. Approximate, steady-state and dynamic models of the CLS system are also derived using *dq*-transformations and the stability of the CLS system is verified using the Routh-Hurwitz criterion.

The objective of the Chapter 4 is to validate the EMTP-RV models developed in Chapter 2 by preliminary simulation in the open-loop control mode. For this, a 1-phase 3-link (or 7-level) version of the CLS is chosen for simulation in EMTP-RV. An open-loop control philosophy is also explained in this chapter, using modulation index and voltage

angle as control inputs. A novel control technique named Rotated Gate Signal Pattern (RGSP) to balance the link dc capacitor voltages of the CLS, is also described here along with the CLS start-up procedure. Both of these techniques are validated by simulation in EMTP-RV. The 1-phase CLS is simulated in EMTP-RV and its preliminary steady- and transient-state performance results are presented to validate its power & gating circuits and to evaluate its performance in open-loop control mode.

In Chapter 5, a closed-loop control strategy is developed using only the phase angle as a control input and keeping modulation index constant. Two cascaded controllers (outer or ac voltage controller and inner or reactive current controller) are designed from their approximate first-order transfer functions. Their dynamic performance is studied and verified using Bode plots and evaluating the system step response.

Several simulation tests are carried out with EMTP-RV in Chapter 6, to validate the operation of the CLS system (along with its controllers) to regulate the power system voltage and the simulation results showing its steady- and transient-state responses are presented.

Final concluding remarks are given in Chapter 7 along with the future direction of the research presented in this thesis.

## 1.7. SUMMARY

This chapter is summarised as follows:

- Brief explanation and comparison of the reactive power compensation techniques using only shunt connected FACTs controllers were explained along with their advantages and limitations.
- A CLC (or CLS) is a relatively new topology of the multilevel converters which has not had much published research information available.
- Brief overview of the objective of this thesis and its main contribution along with the thesis outline, was also provided.

# CHAPTER-2

# CHAIN LINK STATCOM: THEORY

## 2.1. INTRODUCTION

A chain link STATCOM (CLS) is recently introduced topology of the multilevel converter based STATCOM. As yet, only one application exists in the National Grid Company's (NGC's) East Claydon substation in the United Kingdom. This CLS rating is ± 75MVAr and it forms a part of the total 225MVAr SVC System. The basic circuit arrangement, operating principle and gating strategy used for switching this special type of STATCOM are explained in this chapter. Double Fourier series - a method of harmonic analysis of the multi-stepped waveforms of the CLS output voltage - is also explained here. This chapter also provides the main features of the CLS viz. ratings, losses, harmonic performance, redundancy, advantages and disadvantages and its topology in the NGC, UK.

## 2.2. BASIC CIRCUIT ARRANGEMENT & PRINCIPLE OF OPERATION

A CLS comprises of a number of GTO converter 'links' (or chain links) connected in series on their ac side to form a separate 'chain' per phase (Figure 2.1). (Note: Here, the choice of the GTO as a switch is arbitrary. Any other high power electronic switch, for example IGBT, may also be used instead of the GTO switch.) Each 'link' is a 1-phase, 3-level, full bridge, VSC comprised of four GTO-diode pairs as switches and an independent self-controlled dc capacitor ($C_{dc}$) for energy storage (Figure 2.2). In this arrangement, the dc capacitors are floating with the dc voltage, $V_{dc}$ on each of

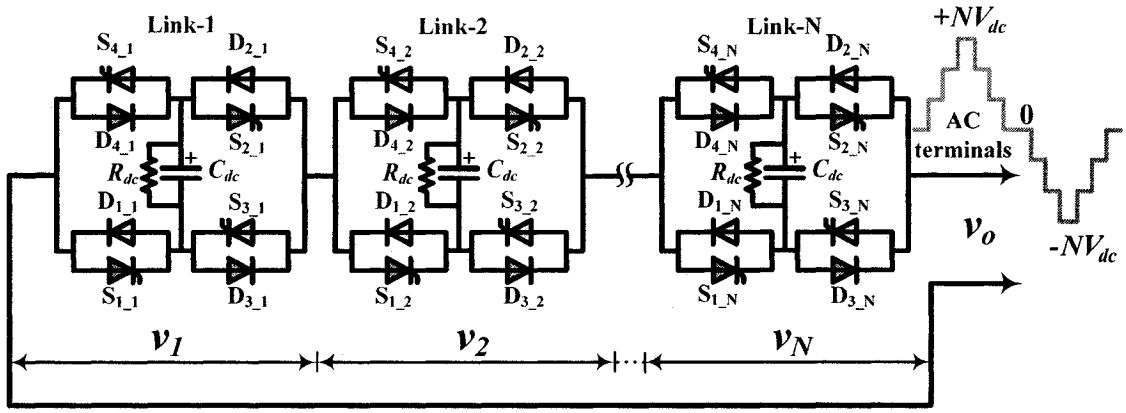


**Figure 2.1. General circuit arrangement of a 1-phase CLS with '*N*' links.**

them. Consequently, no real power needs to be supplied, other than the converter losses which are represented by the parallel resistor, $R_{dc}$.

Each GTO, with its anti-parallel diode, forms a two-way switch. At any instant, the switches can be connected to the positive or negative terminal of its associated dc capacitor. Therefore, each link is either in 'contributing' state or 'non-contributing' state. In contributing state, diagonally placed GTO-diode pairs $S_1$-$D_1$ and $S_2$-$D_2$ conduct so that the link may contribute a voltage of $+V_{dc}$ to the output voltage ($v_o$) (phase to neutral voltage for the 3-phase connection), or $S_3$-$D_3$ and $S_4$-$D_4$ conduct to contribute a voltage of $-V_{dc}$. In the non-contributing state, GTO-diode pairs $S_2$-$D_2$ or $S_4$-$D_4$ conduct, and the link does not contribute any voltage (i.e. zero voltage) to the output. By switching each GTO-diode pair "on/off" once per cycle of the fundamental frequency, a 3-level quasi-square

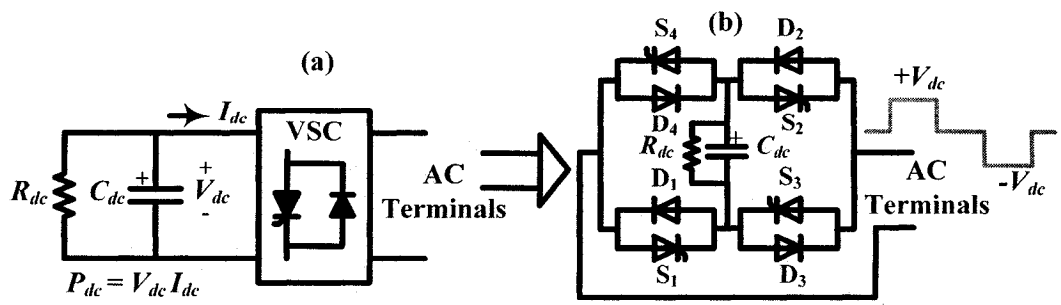


**Figure 2.2. (a) Block diagram and (b) Simplified circuit diagram of a 1-phase VSC link.**

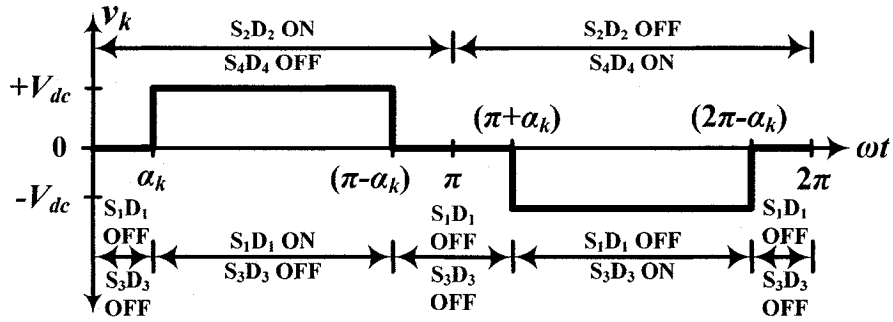


**Figure 2.3. 3-level output voltage ($v_k$) of a 1-phase VSC link.**

output voltage waveform is synthesized for each link (Table 2.1 & Figure 2.3). Therefore, with $N$ links in series (where $N$ is a positive integer), the CLS output voltage contains ($2N$+1) voltage levels (Figure 2.4) that can give a good approximation to a sine wave.

It is important to note from Table 2.1 that for a CLS having more than one link in series per phase, to provide the closed circuit path among the series connected links per phase, during each positive half cycle, it is essential to simultaneously turn on the switches $S_2$-$D_2$ of all the links at instants ($2n\pi$) & turn off them at instants [$(2n+1)\pi$].

**Table 2.1. Switching sequence of any link-$k$ per cycle of the fundamental frequency.**

| Fundamental Link output voltage waveform | Period in radians | Output Voltage of Link-$k$ ($v_k$) | Switch Operating sequence for link-$k$ | | | |
|---|---|---|---|---|---|---|
| | | | $S_1$-$D_1$ | $S_2$-$D_2$ | $S_3$-$D_3$ | $S_4$-$D_4$ |
| Positive cycle | 0 to $\alpha_k$ | 0 | 0 | 1 | 0 | 0 |
| | $\alpha_k$ to ($\pi$ - $\alpha_k$) | $+V_{dc}$ | 1 | 1 | 0 | 0 |
| | ($\pi$ - $\alpha_k$) to $\pi$ | 0 | 0 | 1 | 0 | 0 |
| Negative cycle | $\pi$ to ($\pi$ + $\alpha_k$) | 0 | 0 | 0 | 0 | 1 |
| | ($\pi$ + $\alpha_k$) to ($2\pi$ - $\alpha_k$) | $-V_{dc}$ | 0 | 0 | 1 | 1 |
| | ($2\pi$ - $\alpha_k$) to $2\pi$ | 0 | 0 | 0 | 0 | 1 |

Where, 1 – ON, 0 – OFF and $k$ = 1, 2, 3,.....$N$.

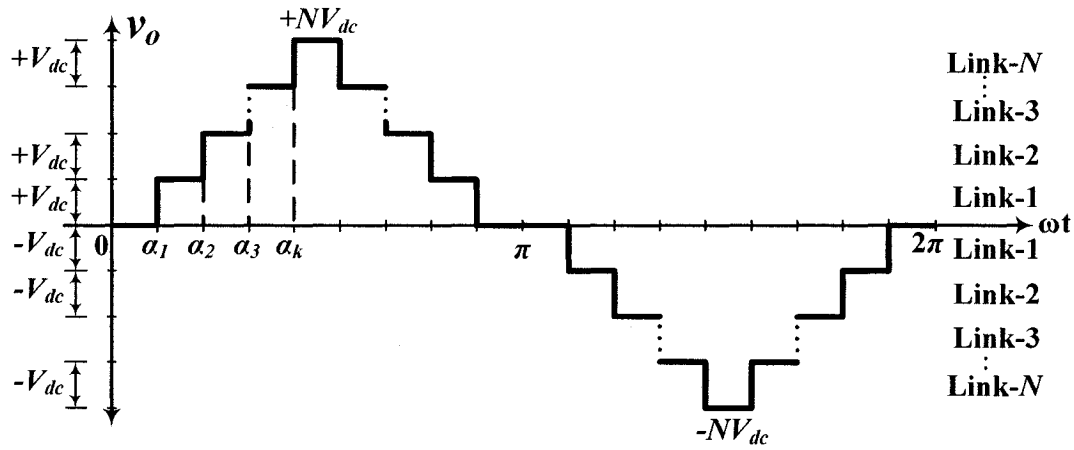


**Figure 2.4. (2*N*+1) level output phase voltage waveform of a CLS with '*N*' links per phase.**

Similarly, during each negative half cycle, it is essential to simultaneously turn on the switches $S_4$-$D_4$ of all the links at instants [(2n+1)π] & turn off them at instants (2nπ), where n = 0,1,2,....∞. Otherwise there will be no flow of the current until all links come into conduction.

The total fundamental frequency output voltage of the CLS ($v_o$) is thus the sum of the individual link ac voltages (Figure 2.4), and similarly for the total VAr rating of the CLS. The ac voltage rating and hence the dc capacitor voltage rating of each link, depends on the total compensation voltage required, the number of converters, and the sharing of the total capacitor voltage among individual links.

With purely reactive loading, the GTOs and the anti-parallel free-wheeling diodes, each carry a quarter wave segment of the fundamental current. When the CLS is supplying VArs to increase the line voltage or compensate for reactive loads, the GTOs must be capable of interrupting the current at its peak. Moreover, when the CLS is absorbing VArs to decrease the line voltage or compensate the capacitive loading, the GTOs are naturally commutated as the current passes through zero.

## 2.3. GATING STRATEGY

### 2.3.1. General

For a CLS, the main challenge is to drive its switches by providing gating signals such that each link produces a 3-level output voltage ($v_k$) by turning each GTO-diode switch "on/off" once per cycle of the fundamental frequency, to synthesize the multilevel output voltage per phase ($v_o$) in a close approximation to the sinusoidal waveform with controllable magnitude and phase angle. This is achieved by a popular control technique known as: "Sinusoidal Pulse Width Modulation (SPWM) method". Its popularity is due to its simplicity and to the good results it guarantees in all the operating conditions, including over modulation [18].

### 2.3.2. SPWM technique for a CLS.

A good approximation of the sinusoidal voltage waveform in a CLS can be produced by a set of triangular signals and a purely sinusoidal modulating signal using a modulation technique known as Sinusoidal Pulse Width Modulation (SPWM). The principle of switching is similar to that of the 1-phase, 2-level converter [16].

In the SPWM technique used for a CLS, there are two triangular carriers per link and one modulating signal for all the links. Therefore, the CLS with $N$-links, a total of $2N$ triangular carrier signals are required. The frequency of the triangular carriers ($f_c$) is selected as 'twice' the fundamental (or power system) frequency ($f_o$) so that each GTO-diode switches "on/off" only once per cycle of the fundamental frequency. The frequency of the modulating signal ($f_m$) is chosen as the fundamental frequency.

i.e. $f_c = 2f_o$ and $f_m = f_o$ where, $f_o = 60$ Hz (2.1)

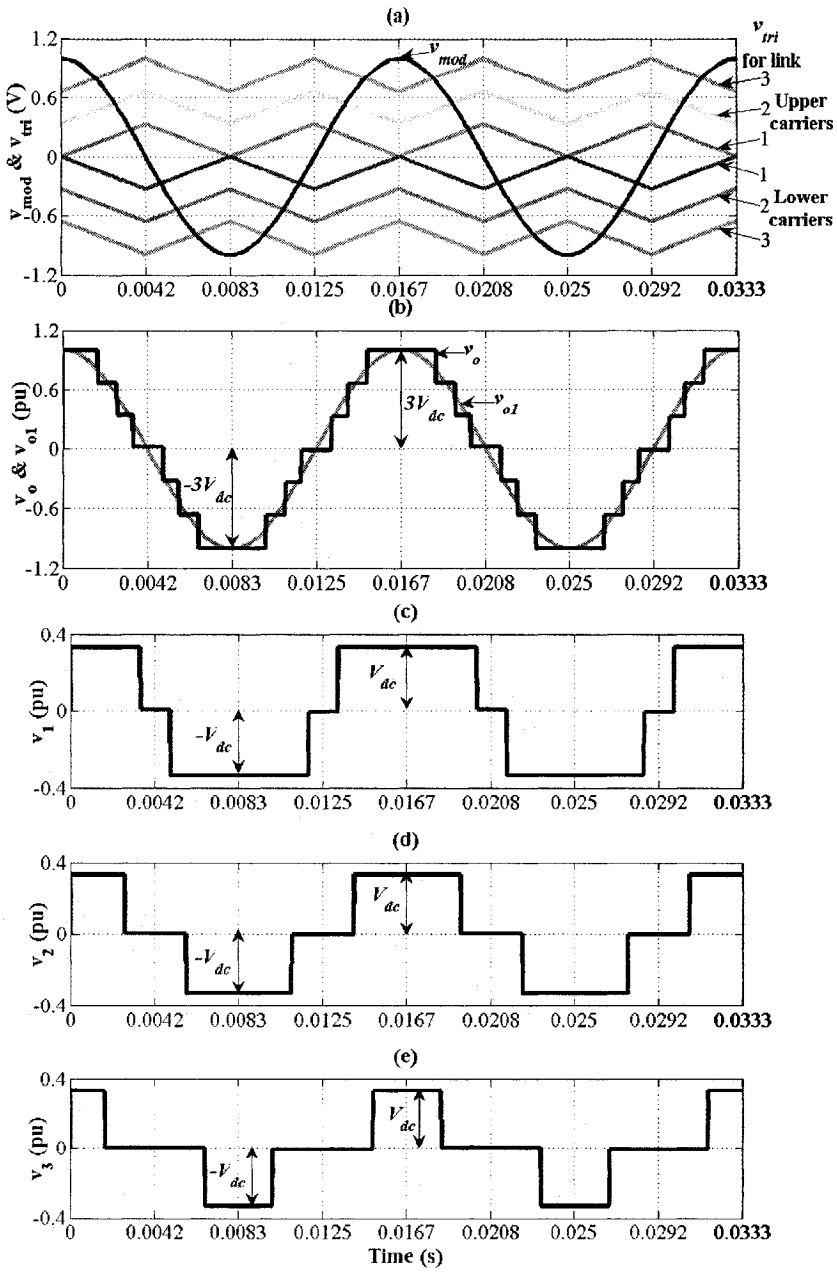


**Figure 2.5. (a) SPWM technique with six triangular carrier bands for 3-links, (b) SPWM output voltage of the CLS, and its fundamental frequency component, (c), (d) and (e) SPWM output voltage of the link-1, -2 and -3 respectively.**

The intersection points of the triangular carrier signals and the modulating signal determine the switching instants $\alpha_1, \alpha_2, \alpha_3, \ldots \alpha_k$ (where, $\alpha_1 < \alpha_2 < \alpha_3 \ldots < \alpha_k$) (Figure 2.4). The harmonic analysis of the modulated waveform is done by the Double Fourier Series (DFS) method [19].

Figure 2.5 shows the SPWM waveforms used for the CLS with 3-links. The upper carrier signal switches the GTO-diode pairs $S_1$-$D_1$ and $S_2$-$D_2$ to contribute + $V_{dc}$ to the output voltage ($v_o$). The lower carrier signals switches the GTO-diode pairs $S_3$-$D_3$ and $S_4$-$D_4$ to contribute -$V_{dc}$. When the carrier does not intersect the modulating signal, the link is in a non-contributing state.

For the CLS the amplitude modulation index ($m_a$) is defined as the ratio of the peak value of the sinusoidal modulating signal, to the sum of the peak-to-peak values, of all the upper (or lower) carriers:

$$m_a = \frac{\hat{V}_{\text{mod}}}{\sum_{1}^{N} \hat{V}_{tri}} \tag{2.2}$$

For the proposed CLS with 3-links, the sum of the peak-to-peak values of all the three upper (or lower) carriers is arbitrarily chosen as 1, as shown in Figure 2.5a (i.e. $m_a = |v_{mod}| = \hat{V}_{mod}$ ). Thus, when $m_a = 1$, the peak of the modulating signal is 1 and when $m_a < 1$, the modulating signal may intersect only some of the carrier signals. Without loss of generality, this is also true for the CLS with $N$ links. The number of links contributing to the full output voltage waveform is given as $<Nm_a>$, which is the smallest integer greater than or equal to '$Nm_a$' [19]. For example if $<Nm_a> = <1.3> = 2$, i.e. the number of links in contributing state = 2 and for $<Nm_a> = <3.0> = 3$, i.e., the number of links in contributing state = 3.

Assuming that the voltages on all the dc capacitors are equal, Figure 2.5b shows the output voltage waveform of the chain link converter with 3-links. With all the links in the contributing state, the individual link voltages are still 3-level waveforms, but having different pulse widths; they are combined to give an effective 7-level waveform of the

output voltage. Here link-1 is chosen to have the longest contribution time, link-2 a slightly shorter and link-3 to have the shortest contribution time. This principle can be extended, without loss of generality, to a converter with $N$ links.

## 2.4. HARMONIC ANALYSIS OF THE CLS OUTPUT VOLTAGE [19]

The converter voltage is the sum of the voltages of all the links contributing to the full output voltage waveform. Therefore, from [19] the modulated output voltage of the CLS is given by:

$$v_{oh} = V_{dc}\, N\, m_a \cos(\omega_o t) + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty} C_{mn} \cos((2m+n)\omega_o t) \qquad (2.3)$$

Where,

$$C_{mn} = \frac{2V_{dc}(-1)^{\frac{n-1}{2}}}{m\pi} J_n(mN\pi\, m_a) \qquad \text{if } m \text{ is even}$$

$$= -\frac{4V_{dc}\, Nm_a}{n\pi} x \sum_{k=1}^{<Nm_a>} \int_{\theta_{k-1}}^{\theta_k} (-1)^{k-1} \cos(m\, N\, \pi\, m_a \cos\lambda) \sin(n\lambda) \sin\lambda\, d\lambda$$

if $m$ is odd

$\theta_k = \cos^{-1}( k / Nm_a )$ for $k$ = 1, 2, 3, …, ($<Nm_a>$ - 1), and $\theta_{<Nma>} = 0$. Where, $<Nm_a>$ is the number of links contributing to the output voltage. This is the expression for a waveform with $<Nm_a>$ contributing links. The first term is of fundamental frequency and its magnitude is proportional to the amplitude modulation index $m_a$. The terms in the double summation are of angular frequency $2\omega_o$, multiples of $2\omega_o$ and their sideband frequencies.

Instead of being a single term, the fundamental component of $v_{oh}$ is made up of an infinite number of terms [19]: the first term of (2.3) and the terms in the double summation, where $(2m+n) = \pm 1$ i.e. for all $m$ from 1 to infinity. For simplicity of the

calculations and analysis, the terms in double summation from (2.3) can be neglected for the CLS with $N$ - links per phase. Therefore, assuming the output voltage of the CLS, $v_o \approx v_{o1}$.

i.e. $v_o \approx V_{dc} N m_a \cos(\omega_o t)$ (2.4)

As shown in Figure 2.5, for $N = 3$ and $m_a = 1.0$, $v_o \approx 3V_{dc} \cos(\omega_o t)$ and the peak magnitude of the output voltage, $\hat{V}_o = 3 V_{dc}$. Detailed harmonic analysis and derivation of (2.3) is given in [19].

## 2.5. CLS: IMPORTANT FEATURES [1, 10]

### 2.5.1. General

The CLS has many good features and advantages over conventional STATCOMs and SVCs. Consequently, it possesses enormous potential to be used in power system applications. Therefore, although the validation of these features and advantages of the CLS is not in the scope, it is essential to briefly discuss them here for the completeness of the thesis. Some of these features have already been validated by simulation studies and experiments on the pilot project in [1, 10].

### 2.5.2. Ratings

The chain link rating is fixed by the capabilities of the GTOs & diodes employed. The commercial devices available readily, have a peak voltage & peak turn-off current capability of 4.5kV and 4kA respectively. In practice, the steady state voltage and current rating of the link has to be lower than these values to withstand the transients introduced during device switching and to give adequate safety margins for the stresses encountered during faults and disturbances. Each phase (or chain) of the 3-phase CLS is identical and

for each phase (or chain) the power circuits of individual chain links are independent of each other and also identical (i.e. same GTO-diode & dc capacitor ratings). Therefore, the voltage rating and hence the VAr rating of the CLS can be increased simply by the addition of more chain links in series per phase (or chain). With this method, the current rating remains unaltered.

### 2.5.3. Losses

In all types of STATCOM the total losses mainly comprise of the losses in the transformer(s) and the power electronics equipment. The latter includes the losses associated with the GTO conduction, switching and its snubber circuit. In the CLS the switching losses are minimized by requiring only one switching operation per GTO per cycle of the fundamental frequency, and further the snubber circuit losses can be minimized by using a low loss design. Therefore the CLS offers a low loss design (less than 0.7% of the STATCOM VAr rating at 1 pu lagging and 1 pu leading current) [1, 10].

### 2.5.4. Redundancy

Since all the links are identical in the CLS, redundancy against the failure of any chain link is incorporated by adding an extra link per phase. Then, in the event of a GTO/link failure, the affected chain link operates continuously in the short circuit (bypass) mode, until the next scheduled maintenance outage.

### 2.5.5. Steady state characteristics

The static characteristic of a CLS is shown in Figure 1.4 . Therefore, it possesses significant advantages in terms of performance over the conventional SVCs, as shown in Section 1.2.4.

### 2.5.6. Harmonic performance

A CLS with $N$ links per phase can produce the output voltage waveform with $N$ steps (or transitions) per quarter cycle of the fundamental frequency. Therefore, in principle it is possible to eliminate $N$ harmonic voltages from the output voltage waveform by an appropriate choice of GTO switching angles [23]. However, this methodology is not in the scope of this thesis.

In actual practice the effects of the capacitor ripple limit the possible number of perfectly cancelled (zeroed) harmonics to somewhat less than the theoretical number. By increasing the number of links per phase, for installations of higher rating, the number of voltage steps in the converter output voltage waveform increases, and this gives further improvements in the harmonic performance.

### 2.5.7. Advantages of a CLS [1, 10]

The CLS has many advantages compared to other GTO based STATCOM circuits and conventional thyristor based SVCs [1, 10]. These are listed below:

- A CLS requires the least number of components to achieve the same number of steps in the output voltage waveform compared to the other known multilevel converter topologies viz. diode-clamped and flying capacitors converters [8]. Although it has the normal anti-parallel diodes across each GTO switch, it does not require extra auxiliary diodes associated with the multilevel capacitor stack circuit.
- The voltage and hence VAr rating of a CLS can be increased by simply adding more number of links in series per phase.

- Since each phase of a 3-phase CLS can be operated independently of one another, it offers the potential for balancing ac system phases.
- A CLS gives a low loss design by switching each GTO on/off only once per cycle of the fundamental frequency. Furthermore, the snubber circuit losses can be minimized by using low loss techniques and employing snubber energy recovery circuits [9].
- A CLS has built-in redundancy against a failure of any link.
- As chain links in a CLS switch in sequence, the maximum instantaneous voltage excursion is reduced depending upon the rating of the GTO (e.g. The STATCOM used in the NGC's East Claydon substation, this voltage excursion is approximately of 2kV for the 4.5kV peak voltage rated GTO) and hence the radio interference is minimized.
- A CLS eliminates the use of expensive zigzag transformer and requires only one coupling transformer of the conventional design to step down the transmission voltage to the rated STATCOM connection voltage.
- The need for complex magnetic combining transformers to achieve an acceptable output voltage is avoided by building-up the output voltage within the converter itself from number of separate steps, with each link providing single step in a CLS.
- In a CLS, by suitable choice of the switching angles, the low order harmonics can be prevented especially during the unbalanced ac system conditions. This is not possible in case of the circuits based on 3-phase bridges.

- A CLS gives good harmonic performance with small or no harmonic filters. Better harmonic performance can be achieved by increasing more number of links (and hence more steps in the output voltage waveform) per phase.
- A CLS eliminates the problems and limitations that can arise due to the direct series connection of the GTOs.
- The STATCOM technology gives inherent fast response. The transient performance is enhanced by the ability to instantaneously change the output voltage by inserting or bypassing links independently per phase.
- Due to its constant current characteristic, a CLS can maintain the rated leading (or lagging) current at low ac system voltage (for example during the faults).
- A CLS gives optimized circuit layout, uniform packaging, modular structure and relocatable design because of identical rating and arrangement of each link. This also reduces the space to about 50% compared to the conventional thyristor based SVCs of the same rating.
- With a CLS it is possible to provide real power compensation by replacing the dc capacitors of each link with a battery of other suitable energy storage component.
- A CLS could be connected in series with each phase of an ac system to provide a controllable positive or negative reactance to control the power flow. With this the control of power flow in parallel circuits of ac system could be possible.
- A CLS has ability to control the self-generated harmonics by suitable choice of switching angles. Therefore, it could be used as an active filter to control the pre-existing harmonics of the ac system.

- A CLS could be used for frequency control, peak lopping, replacement of spinning reserve and black start conditions (i.e. starting an unenergized ac system).

### 2.5.8. Main constraints of a CLS

Like other multilevel converters a CLS has the following constraints.

- The dc voltage unbalance among the dc capacitors of each link makes it difficult to regulate the output voltage of the CLS. This also makes the system design, maintenance and keeping the stocks of the spare parts complicated. This dc voltage unbalance can be minimized by introducing a novel rotated switching technique (RGSP) however cannot be completely eliminated. This technique is explained in Chapter 4.
- The control and protection circuits, although having identical circuit layout and structure, are complicated to design and troubleshoot because of many GTO links and many switching events during one cycle of the fundamental frequency.

## 2.6. CLS FOR THE NATIONAL GRID COMPANY, UK [1, 10]

### 2.6.1. Basic layout of SVC system for NGC, UK

As part of a program of investment in relocatable reactive compensation in the UK, NGC initiated a project to deliver a CLS-based SVC for its 400kV East Claydon substation, Buckinghamshire [1, 10]. This installation was the first application of the STATCOM in the UK and has been in service since 1999.

Figure 2.6 shows the SVC configuration in the East Claydon substation. The SVC is designed to provide a smoothly variable reactive power output of 0-225 MVAr (capacitive). No inductive capability has been specified. The SVC equipment is

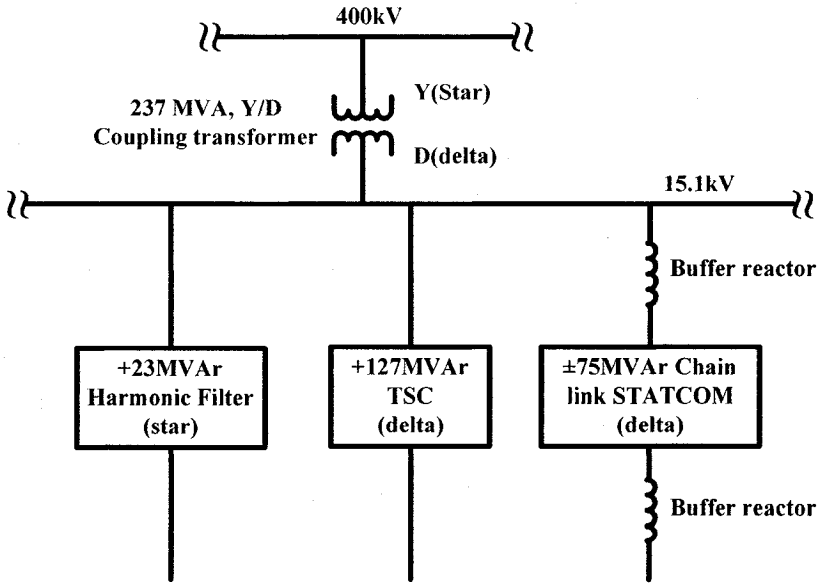


**Figure 2.6: Configuration of SVC system in NGC's East Claydon substation, UK.**

connected to LV busbars operating nominally at 15.1kV fed via the secondary winding of the compensator transformer.

Design optimization led to a configuration that employs a STATCOM with a dynamic range of 150MVAr (±75MVAr) which, in conjunction with a small fixed filter of 23MVAr, provides outputs between zero to about 100MVAr. A 127MVAr TSC is also provided to deliver the additional MVAr required for an output of 225MVAr. The TSC provides a rapid and reliable means of delivering additional reactive power when system conditions require the maximum available compensation.

### 2.6.2. Key design features of the CLS for NGC, UK

Each link of the ALSTOM designed CLS used in the East Claydon substation incorporates four 4.5 kV GTOs (with 3 kA turn-off capability) and its own dc capacitor acting as voltage source. The 3-phase connection of the STATCOM is made by connecting three 1-phase converters in delta. Each phase comprises of 16 series

connected links out of which 2 links are used as redundant. Therefore, with all 16 links in contributing state, the per-phase STATCOM output voltage contains 33-voltage levels and produces very high quality, nearly sinusoidal voltage waveform.

Each phase is connected to the LV busbars via a small air cored buffer reactor chosen to ensure that the control system can provide fast and stable control of the converter over its full operating range. The reactors also limit the maximum voltage and current stresses on the converter in the event of an insulation fault on the 15.1 kV bus.

The dc capacitor voltage charging and balancing is accomplished by using dual IGBT converters for each link. These are connected to an auxiliary power supply bus at earth potential (known as ground level power supply-GLPS) via a fully insulated, auxiliary power isolating transformer (APIT). The rating of the converter/APIT combination is 5 kVA at 7.5 kHz.

The physical arrangement of the power electronic equipment for each link has been carefully engineered to deliver a compact modular unit. Each phase of the STATCOM is self-contained in a road transportable container which houses the links and associated dc capacitors, the control equipment and other ancillary systems.

Although the test study on the above mentioned system showed good results, these were accomplished at the expense of adding more devices and complicating the control system. On the other hand, in this thesis the SPWM technique of fundamental frequency switching is used (section 2.3) and to balance the dc capacitor voltage an alternative approach called the RGSP is illustrated in Chapter 4 which is based on the rotation of the switching (or gating) signals among the links per cycle of the fundamental

frequency. These proposed techniques are more cost efficient and easier to implement. However, the cost calculations and comparison are beyond the scope of this thesis.

## 2.7. SUMMARY

The following points have been explained in this chapter, as a theory of the CLS.

- The basic circuit topology and operating principle of a CLS were discussed.
- The SPWM technique with two triangular carriers (one upper or positive and one lower or negative) per link and one modulating signal for all the links per phase was used to drive the switches of this special type of STATCOM to obtain the multi-step CLS output voltage per phase in a close approximation to sinusoidal waveform.
- The harmonic analysis of the multi-step CLS output voltage was done by the DFS method.
- Important features of a CLS viz. rating, losses, redundancy, static characteristics, harmonics performance, along with the potential advantages and main constraints of the chain link topology were also discussed in comparison with the conventional three-phase bridge STATCOM topology and thyristor based SVCs.
- A brief explanation of the only existing application of a CLS that is employed in the NGC's East Claydon substation, UK was presented along with its design features and basic SVC system layout.

# CHAPTER-3

# CLS POWER CIRCUIT & SYSTEM MODELING

## 3.1. INTRODUCTION

A 3-phase CLS having 3-links per phase is modeled in EMTP-RV to investigate its behaviour under different power system operating conditions. The model of the CLS is comprised of three fundamental blocks: a GTO-diode switch, a VSC link and an SPWM circuit. The EMTP-RV models of these fundamental blocks along with the test circuit of the CLS system are discussed in this chapter. Approximate mathematical models of the CLS system using *dq*-transformation are also obtained in this section.

## 3.2. POWER CIRCUIT OF THE CLS SYSTEM

For the proposed CLS model validation, a 3-phase radial transmission test system is considered (Figure 3.1). The measurements are referred to a per unit (pu) system with a base rating of 10 MVA and a primary/secondary voltage rating of 400/15.1 kV. The sending end of the transmission line is connected to a 3-phase star-connected supply, represented by a Thevenin equivalent voltage source ($v_s$) of magnitude 1.0 pu behind the source impedance ($Z_s$) = (0.0005+j0.05) pu. The supply system is assumed to keep $v_s$ constant under all loading conditions. A 3-phase transmission line is represented by an equivalent transmission line positive sequence impedance ($Z_{tl}$) = (0.001+j0.1) pu in series with the power supply. For the simplicity of the analysis, a detailed model of the line is not used, as the primary focus of this thesis is to develop the STATCOM model, which is

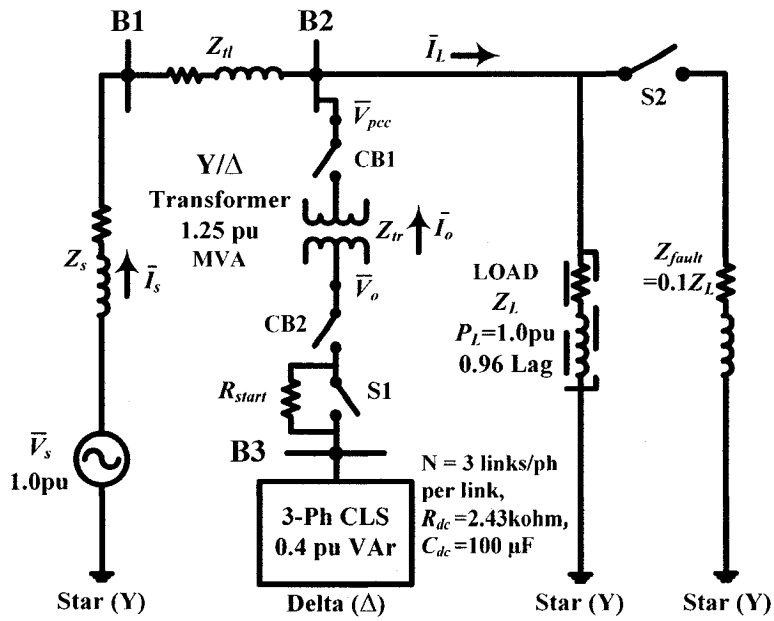


**Figure 3.1. Single line diagram of the CLS system.**

a formidable task in its own. A 3-phase star connected R-L load of rated active power ($P_L$) = 1.0 pu at 0.96 power factor lagging (i.e. rated load reactive power, $Q_L \approx 0.3$ pu) and having load impedance ($Z_L$) = (0.921+j0.124) pu is connected at the receiving end of the transmission line.

The proposed CLS is connected in 3-phase delta-connection at the PCC across the load via a 3-phase star-delta coupling transformer, the circuit breakers (CB1 & CB2) and switch S1. The transformer is of 1.25 pu MVA rating and has a leakage impedance ($Z_{tr}$) = (0.0005+j0.05) pu. The coupling transformer reduces the transmission system high voltage to a level suitable for the design rating of the CLS, which in turn depends on the individual switch rating.

A start-up resistor $R_{start}$ = 300 ohm connected across the switch S1 is introduced in series with the CLS during the start-up of the CLS by keeping S1 open to limit the dc capacitor charging current. When the dc voltages of the link dc capacitors reach a stable value, $R_{start}$ is bypassed by closing the switch S1. S1 remains closed through out the

normal operation of the CLS. The CLS start-up procedure is explained in the subsequent section. In Figure 3.1, $\bar{V}_o$ represents the voltage vector of the fundamental Fourier series component of the CLS output voltage ($v_o$). The terms $\bar{V}_s$ & $\bar{V}_{pcc}$ are the vectors of the Thevenin equivalent source voltage ($v_s$) and voltage at the PCC ($v_{pcc}$), respectively, whereas $\bar{I}_o$ & $\bar{I}_L$ are the STATCOM output and load current vectors ($i_o$ & $i_L$) respectively.

The switch S2 and the fault impedance ($Z_{fault}$) = $0.1Z_L$ are used to carry out the 3-phase short circuit test, for validating the dynamic performance of the CLS system in Chapter 6.

## 3.3. GTO-DIODE SWITCH MODEL ('SW')

Each switch model 'SW' (Figure 3.2) comprises of a GTO thyristor with an anti-parallel diode across it. When the GTO is switched on, it allows the current to flow only in one direction from dc to ac side and blocks the reverse current from ac to dc side of the converter. In contrast, the anti-parallel diode allows the current to flow from ac to dc side only. Therefore, the GTO and diode together operate as a bi-directional switch.

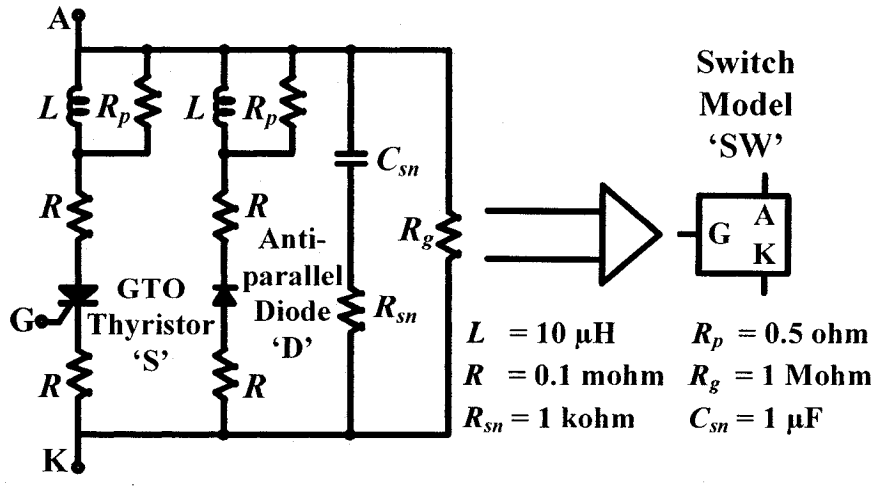


**Figure 3.2. GTO-diode switch model 'SW' in EMTP-RV.**

Moreover, the snubber circuits are used in the converter to protect the semiconductor switches from the electrical stresses that occur during the switching operations. In the semiconductor switches, the over voltages (*dv/dt*) occur during switch turn-off and over currents (*di/dt*) occur during switch turn-on. Therefore, to protect them, it is essential to limit *dv/dt* and *di/dt* stresses within the rating of the switches. The *RC* snubber circuit is used for *dv/dt* protection and *L* snubbers are used for *di/dt* protection. Although their values may not be realistic in the model, these snubbers do represent similar components in real converter. Therefore, a switch model 'SW' consists of two small *di/dt* current limiting inductors, $L$=10 μH each with the parallel resistor, $R_p$ = 0.5 ohm and the *RC* snubber circuit with resistor, $R_{sn}$ = 1 kilo-ohms, and capacitor, $C_{sn}$ = 1 μF.

The switching circuit also comprises of a very high value resistor, $R_g$ = 1 Mega-ohm across the *RC* snubber circuit which represents the dielectric leakage resistance of the switching circuit. Four very small decoupling resistors, each of value $R$ = 0.1 milli-ohm, in series with the GTO and anti-parallel diode are also employed. These resistors represent the switch conduction losses and also assist in avoiding any singularity on the inversion of the conductance matrix of circuit during simulation with EMTP-RV. The values of these components are a function of the rating of the switching circuit, rating of each link and overall CLS rating. Therefore, they must be selected carefully to suit the application. Here the selection of the values was done by trial-and-error simulation runs with EMTP-RV.

## 3.4. VSC LINK MODEL

Each VSC link is a 1-phase, full bridge, 3-level converter comprised of four bi-directional switch models SW1-SW4 (**Figure 3.3**) and a dc capacitor $C_{dc}$ for energy storage. The resistor $R_{dc}$, connected in parallel with the dc capacitor $C_{dc}$, represents the losses in each VSC link.

## 3.5. SPWM CIRCUIT MODEL

As explained earlier in Chapter 2, the purpose of the SPWM circuit is to provide gating signals to the switches of a CLS such that each link produces a 3-level output voltage ($+V_{dc}$, 0 and $-V_{dc}$) by turning each GTO on/off once per cycle of the fundamental frequency, to synthesize the multilevel STATCOM output voltage in a close approximation to the sinusoidal waveform with a controllable magnitude and phase angle.

The SPWM circuit modeled in EMTP-RV is for a CLS with 3 links per phase. 3 links are used here, since the model exemplifies an adequate degree of complexity without incurring the excessive computational burden of a larger number of links.

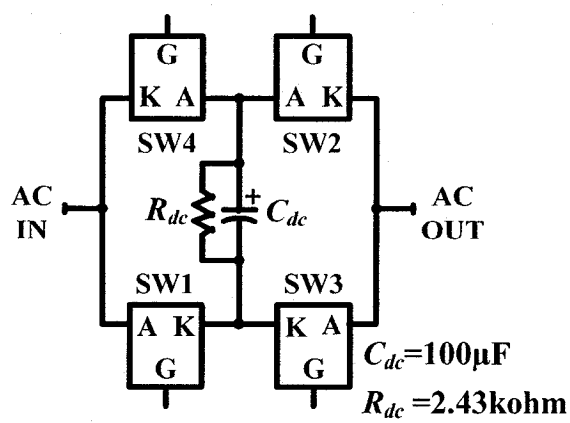


**Figure 3.3. Model of VSC link in EMTP-RV.**

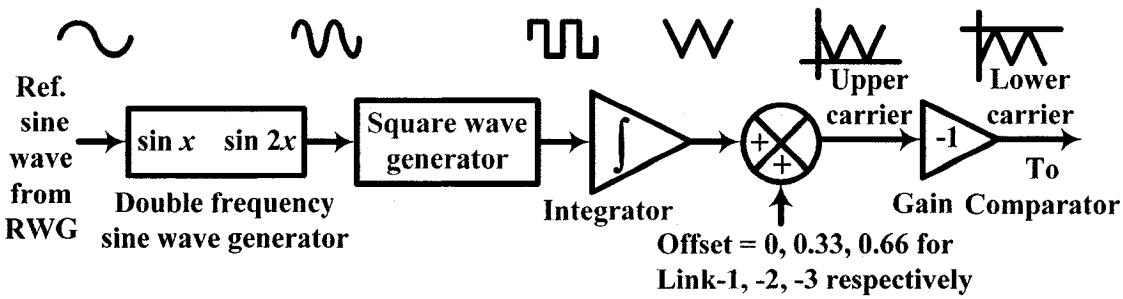


**Figure 3.4: Triangular carrier generator for each link.**

However, this principle can be extended for a CLS with many links per phase. The main blocks of the EMTP-RV model of the SPWM circuit are triangular carrier generator and comparator.

### 3.5.1. Triangular carrier generator for a link.

The triangular carrier generator of a link provides one upper and one lower (i.e. total two carriers per link) triangular carrier signals for each link. As number of links per phase chosen over here are three, total three triangular carrier generators are required that provide six bands of carrier signals (three upper and three lower) per phase (Figure 2.5). Since the sum of the peak-to-peak amplitudes of all three upper (or lower) triangular carriers is arbitrarily chosen as 1, for a 3-link model, the peak-to-peak amplitude of each upper (or lower) triangular carrier is 0.33.

In its basic form, the triangular carrier generator for each link consists of a double frequency sine wave generator, a square wave generator, an integrator and an offset block (Figure 3.4). A double frequency sine wave generator receives the reference sinusoidal signals from the output of the reference wave generator (RWG) and produces the double frequency sinusoidal signals synchronized to the reference signals. These double frequency sine wave signals are then fed as input to the square wave generator which outputs the square wave signals, synchronized to the reference signals. An integrator

**Table 3.1: Distribution of the comparators required per phase in the SPWM circuit.**

| For the switch group per phase | | Number of comparators |
|---|---|---|
| Positive | SW1s | 3 |
| | SW2s | 1 |
| Negative | SW3s | 3 |
| | SW4s | 1 |

integrates the square wave signals into triangular signals and fed them into the dc offset block. The dc offset is used to generate a band of the triangular carriers for a particular link. This means that, for a 3- link model of the CLS, by adding the dc offset of 0V to the output of the integrator, the upper carriers of Link-1 are generated. Similarly by adding the dc offset of 0.33V, the upper carriers of Link-2 and by adding 0.66V the upper carriers of Link-3 are generated. Finally, to get the respective lower carriers, the output of the dc offset is multiplied by a gain of -1. The upper and lower carriers are then outputted to the comparator for comparing them with the sinusoidal modulating signal and generate the gating signals for the switches.

### 3.5.2. Comparator

A band of the carrier signal (upper or lower) from a triangular carrier generator is compared with a sinusoidal modulating signal that is obtained from the RWG, to generate the gate signals for a switch 'SW' (Figure 3.5). For the proposed 3-phase CLS with 3

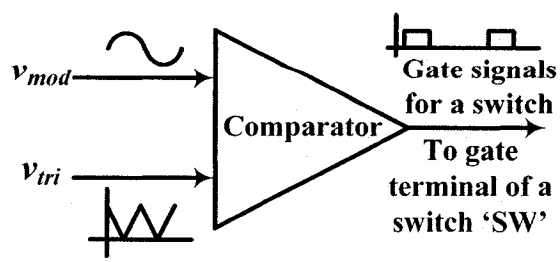


**Figure 3.5: Comparator to generate the gate signals for each switch 'SW'.**

links per phase, total eight such comparators (Figure 3.5) are used to generate the switching signals per phase. The distribution of these eight comparators per phase in the SPWM circuit is shown in Table 3.1.

The points of intersection of the modulating and carrier signal determine the switching instants as shown in Figure 2.5. This means that, when the $v_{mod} \leq v_{tri}$, the output of the comparator is at logic 0 (or state OFF) and when $v_{mod} > v_{tri}$, the comparator output is at logic 1 (or state ON). Consequently, the comparator output is used as a gate signal to switch each GTO on/off only once per cycle of the fundamental frequency.

## 3.6. CLS SYSTEM MODELING

Figure 3.6a represents the Thevenin equivalent circuit of the CLS system (Figure 3.1). For an ideal 3-phase power supply, the instantaneous phase voltages at the PCC & CLS output terminals and the instantaneous CLS output phase currents are:

$$\begin{bmatrix} v_{pcc\_a} \\ v_{pcc\_b} \\ v_{pcc\_c} \end{bmatrix} = \sqrt{2} V_{pcc} \begin{bmatrix} \cos(\omega_o t + \theta) \\ \cos(\omega_o t + \theta - 2\pi/3) \\ \cos(\omega_o t + \theta + 2\pi/3) \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} v_{o\_a} \\ v_{o\_b} \\ v_{o\_c} \end{bmatrix} = \sqrt{2} V_o \begin{bmatrix} \cos(\omega_o t + \theta - \delta) \\ \cos(\omega_o t + \theta - \delta - 2\pi/3) \\ \cos(\omega_o t + \theta - \delta + 2\pi/3) \end{bmatrix} \tag{3.2}$$

$$\begin{bmatrix} i_{o\_a} \\ i_{o\_b} \\ i_{o\_c} \end{bmatrix} = \sqrt{2} I_o \begin{bmatrix} \cos(\omega_o t + \theta + \varphi) \\ \cos(\omega_o t + \theta + \varphi - 2\pi/3) \\ \cos(\omega_o t + \theta + \varphi + 2\pi/3) \end{bmatrix} \tag{3.3}$$

Where, $\omega_o$ is the system (or fundamental) frequency. The complex voltage and current vectors can be expressed in the stationary ($\alpha\beta$-axis):

$$\bar{V}_{pcc} = \sqrt{2}\, V_{pcc}\, e^{j\theta} \tag{3.4}$$

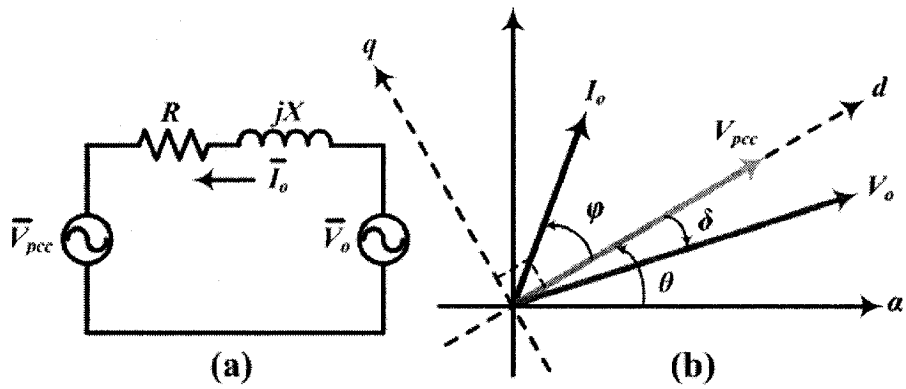


**Figure 3.6. (a) Thevenin equivalent circuit of CLS system and (b) its space vector diagrams.**

$$\bar{V}_o = \sqrt{2}\, V_o\, e^{j(\theta-\delta)} \tag{3.5}$$

$$\bar{I}_o = \sqrt{2}\, I_o\, e^{j(\theta+\phi)} \tag{3.6}$$

Note that the positive/negative signs of the angle show that the vectors are leading/lagging the reference axis respectively. The space vector diagram for voltages and current is shown in Figure 3.6, where $\alpha\beta$-axis represents synchronous rotating reference frame. The $d$-axis is assigned to coincide with the space vector $\bar{V}_{pcc}$.

### 3.6.1. Dynamic model of a CLS

By writing the KVL equation of the power system shown in Figure 3.6 on stationary reference frame ($\alpha\beta$-axis) as:

$$L\,\frac{d\bar{I}_o}{dt} + R\,\bar{I}_o = \bar{V}_o - \bar{V}_{pcc} \tag{3.7}$$

Now by transforming the complex vectors from stationary reference frame to synchronously rotating reference frame ($dq$-axis) by multiplying them with a unit space vector, $e^{-j\theta}$ [22]:

$$\bar{V}_{pcc}\, e^{-j\theta} = v_{pcc\_d} + jv_{pcc\_q} = v_{pcc} = \sqrt{2}\, V_{pcc} \tag{3.8}$$

$$\bar{V}_o\, e^{-j\theta} = v_{o\_d} + jv_{o\_q} = v_o\, e^{-j\delta} = \sqrt{2}\, V_o\, e^{-j\delta} = \sqrt{2}\, V_o(\cos\delta - j\sin\delta) \tag{3.9}$$

$$\bar{I}_o e^{-j\theta} = i_{o\_d} + j i_{o\_q} = i_o e^{j\phi} \tag{3.10}$$

$$L e^{-j\theta} \frac{d\bar{I}_o}{dt} + R e^{-j\theta} \bar{I}_o = \bar{V}_o e^{-j\theta} - \bar{V}_{pcc} e^{-j\theta} \tag{3.11}$$

$$L e^{-j\theta} \frac{d(i_o e^{j(\theta+\varphi)})}{dt} + R e^{-j\theta} \bar{I}_o = \bar{V}_o e^{-j\theta} - \bar{V}_{pcc} e^{-j\theta}$$

$$\{ L e^{-j\theta} e^{j\theta} \frac{d(i_o e^{j\varphi})}{dt} + L e^{-j\theta} i_o e^{j\varphi} \frac{d(e^{j\theta})}{dt} \} + R e^{-j\theta} \bar{I}_o = \bar{V}_o e^{-j\theta} - \bar{V}_{pcc} e^{-j\theta}$$

Note that, when $i_{o\_q}$ is negative, the CLS supplies capacitive reactive power to the line and for positive $i_{o\_q}$, it absorbs inductive reactive power. Now by substituting (3.10), $\theta = \omega_o t$ and $\frac{d(e^{j\theta})}{dt} = j\omega_o e^{j\theta}$ in (3.11):

$$\{ L \frac{d(i_{o\_d} + j i_{o\_q})}{dt} + j\omega_o L (i_{o\_d} + j i_{o\_q}) \} + R e^{-j\theta} \bar{I}_o = \bar{V}_o e^{-j\theta} - \bar{V}_{pcc} e^{-j\theta} \tag{3.12}$$

By substituting (3.8) and (3.9) into (3.12) and rearranging the voltage equations for real part in $d$-axis and for imaginary part in $q$-axis are [22]:

$$L \frac{di_{o\_d}}{dt} + R i_{o\_d} = N m_a V_{dc} \cos\delta - v_{pcc\_d} + L \omega_o i_{o\_q} \tag{3.13}$$

$$\frac{di_{o\_d}}{dt} = -\frac{R}{L} i_{o\_d} + \omega_o i_{o\_q} + \frac{N m_a}{L} V_{dc} \cos\delta - \frac{1}{L} v_{pcc\_d} \tag{3.14}$$

$$L \frac{di_{o\_q}}{dt} + R i_{o\_q} = -N m_a V_{dc} \sin\delta - v_{pcc\_q} - L \omega_o i_{o\_d} \tag{3.15}$$

$$\frac{di_{o\_q}}{dt} = -\omega_o i_{o\_d} - \frac{R}{L} i_{o\_q} - \frac{N m_a}{L} V_{dc} \sin\delta - \frac{1}{L} v_{pcc\_q} \tag{3.16}$$

The fundamental Fourier series component of the CLS output voltage per phase ($v_o$) is given as:

$$v_o \approx N m_a V_{dc} \cos(\omega_o t) \tag{3.17}$$

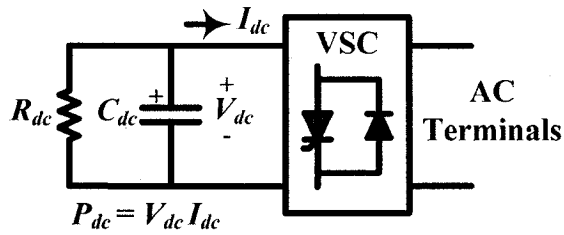


**Figure 3.7. Block diagram of a VSC link.**

Therefore, the magnitude of the STATCOM output voltage per phase is directly proportional to the dc voltage across the dc capacitor of a link and number of links per phase i.e.

$$\sqrt{2}\, V_o = N m_a V_{dc} \tag{3.18}$$

The active power flows into the CLS can be described as:

$$P_{DC} = P_{AC}, \text{ where, } P_{DC} = 3NP_{dc} \tag{3.19}$$

$$3N V_{dc} I_{dc} = v_{o\_a} i_{o\_a} + v_{o\_b} i_{o\_b} + v_{o\_c} i_{o\_c} = \frac{3}{2}(v_{o\_d}\, i_{o\_d} + v_{o\_q}\, i_{o\_q}) \tag{3.20}$$

The dc current ($I_{dc}$) in the above equation is the sum of the capacitor current and resistor current (Figure 3.7), i.e.

$$I_{dc} = -\left( C_{dc} \frac{dV_{dc}}{dt} + \frac{V_{dc}}{R_{dc}} \right) \tag{3.21}$$

Whereas, the direct ($d$-axis) and quadrature ($q$-axis) components of $v_o$ are:

$$v_{o\_d} = N\, m_a\, V_{dc} \cos\delta \tag{3.22}$$

$$v_{o\_q} = -N\, m_a\, V_{dc} \sin\delta \tag{3.23}$$

Substituting (3.21), (3.22) & (3.23) into (3.20) and rearranging:

$$\frac{dV_{dc}}{dt} = -\frac{m_a}{2 C_{dc}} i_{o\_d} \cos\delta + \frac{m_a}{2 C_{dc}} i_{o\_q} \sin\delta - \frac{V_{dc}}{C_{dc} R_{dc}} \tag{3.24}$$

By combining (3.14), (3.16) & (3.24), the CLS state equation can be formed as:

$$\frac{d}{dt}\begin{bmatrix} i_{o\_d} \\ i_{o\_q} \\ V_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega_o & \frac{N m_a}{L}\cos\delta \\ -\omega_o & -\frac{R}{L} & -\frac{N m_a}{L}\sin\delta \\ -\frac{m_a}{2C_{dc}}\cos\delta & \frac{m_a}{2C_{dc}}\sin\delta & -\frac{1}{C_{\mathrm{dc}} R_{dc}} \end{bmatrix} \begin{bmatrix} i_{o\_d} \\ i_{o\_q} \\ V_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{pcc\_d} \\ v_{pcc\_q} \end{bmatrix} \tag{3.25}$$

From the above analysis, it is noted that either adjusting $m_a$ or the phase angle $\delta$ of the CLS output voltage vector, the CLS output voltage could be controlled. For the proposed CLS in this thesis, $m_a$ is kept constant and only $\delta$ is regarded as a control input [22]. Consequently, (3.25) becomes nonlinear. However, for small perturbations around the steady-state equilibrium point $\delta_o$, the linear set of equations can be obtained. The linearization process yields the following perturbation equations:

$$\frac{d}{dt}\begin{bmatrix} \Delta i_{o\_d} \\ \Delta i_{o\_q} \\ \Delta V_{dc} \end{bmatrix} = [\mathbf{A}_\Delta] \begin{bmatrix} \Delta i_{o\_d} \\ \Delta i_{o\_q} \\ \Delta V_{dc} \end{bmatrix} + [\mathbf{B}_\Delta] \begin{bmatrix} \Delta v_{pcc\_d} \\ \Delta v_{pcc\_q} \\ \Delta \delta \end{bmatrix} \tag{3.26}$$

$$[\mathbf{A}_\Delta] = \begin{bmatrix} -\frac{R}{L} & \omega_o & \frac{N m_a}{L}\cos\delta_o \\ -\omega_o & -\frac{R}{L} & -\frac{N m_a}{L}\sin\delta_o \\ -\frac{m_a}{2C_{dc}}\cos\delta_o & \frac{m_a}{2C_{dc}}\sin\delta_o & -\frac{1}{C_{\mathrm{dc}} R_{dc}} \end{bmatrix}$$

$$[\mathbf{B}_\Delta] = \begin{bmatrix} -\frac{1}{L} & 0 & -\frac{N m_a}{L} V_{dco}\sin\delta_o \\ 0 & -\frac{1}{L} & -\frac{N m_a}{L} V_{dco}\cos\delta_o \\ 0 & 0 & \frac{m_a}{2C_{\mathrm{dc}}}(i_{o\_do}\sin\delta_o + i_{o\_qo}\cos\delta_o) \end{bmatrix}$$

### 3.6.2. Stability of the CLS system

The characteristic equation for the CLS system represented by (3.26) is:

$$s^3 + \left(\frac{2R}{L} + \frac{1}{C_{dc}R_{dc}}\right)s^2 + \left(\frac{R^2}{L^2} + \frac{2R}{LC_{dc}R_{dc}} + \omega_o{}^2 + \frac{Nm_a{}^2}{2LC_{dc}}\right)s + \left(\frac{R^2}{L^2C_{dc}R_{dc}} + \frac{\omega_o{}^2}{C_{dc}R_{dc}} + \frac{Nm_a{}^2R}{2L^2C_{dc}}\right) = 0 \quad (3.27)$$

The characteristic equation (3.27) is not a function of phase angle ($\delta$). Therefore, it does not affect the position of the roots of the equation (3.26) on the complex plane. The stability of the CLS is tested using the Routh-Hurwitz criterion. Let the coefficients of $s^2$, $s^1$ and $s^0$ in (3.27) be $a_1$, $a_2$ and $a_3$ respectively. Consequently (3.27) becomes:

$s^3 + a_1 s^2 + a_2 s^1 + a_3 s^0 = 0$ and the Routh array is:

| | | |
|---|---|---|
| $s^3$ | 1 | $a_2$ |
| $s^2$ | $a_1$ | $a_3$ |
| $s^1$ | $a_2 - (a_3 / a_1)$ | |
| $s^0$ | $a_3$ | |

By substituting $a_1$, $a_2$ and $a_3$ to determine the elements of the first column of the Routh array and assigning $T_1 = \frac{L}{R}$, $T_2 = C_{dc}R_{dc}$ and $K = \frac{Nm_a{}^2}{2LC_{dc}}$:

$$a_2 - \frac{a_3}{a_1} = \frac{1}{(T_1 + 2T_2)}\left\{\frac{2T_2}{T_1^2} + \frac{4}{T_1} + \frac{2}{T_2} + K(T_1 + T_2) + 2\omega_o{}^2T_2\right\} \geq 0 \quad (3.28)$$

By careful examination of the elements of the first column of the array it is observed that all the elements are positive and there is no change in the sign. Consequently, the CLS system is stable and the values of resistors, inductors & capacitors of the CLS circuit do not affect the stability.

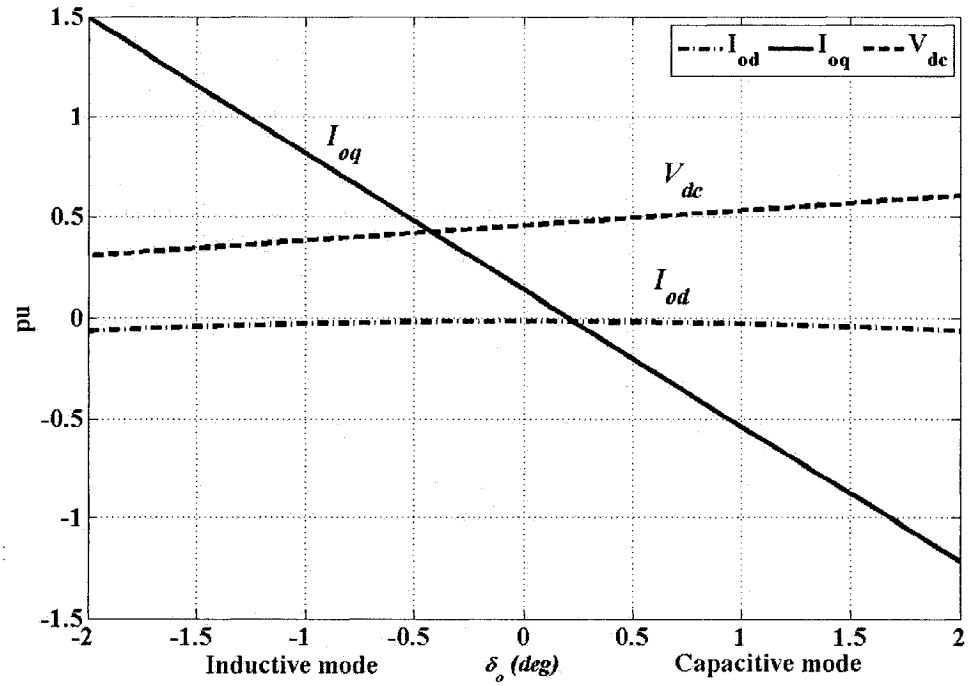


**Figure 3.8. Steady-state variation of $I_{o\_d}$, $I_{o\_q}$ and $V_{dc}$ against $\delta_o$.**

### 3.6.3. Steady-state model of the CLS

The STATCOM steady state model can be obtained from the dynamic model (3.25) by setting all the derivative terms equal to zero. After transformation from *abc* to *dq* reference frame, the voltages and the currents become dc quantities. Therefore, substituting $v_{pcc\_d} = |\, v_{pcc} \,| = \sqrt{2}\, V_{pcc}$, $v_{pcc\_q} = 0$, $i_{o\_d} = I_{o\_d}$, and $i_{o\_q} = I_{o\_q}$, the STATCOM steady state model becomes:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega_o & \frac{N m_a}{L}\cos\delta \\ -\omega_o & -\frac{R}{L} & -\frac{N m_a}{L}\sin\delta \\ -\frac{m_a}{2C_{dc}}\cos\delta & \frac{m_a}{2C_{dc}}\sin\delta & -\frac{1}{C_{dc} R_{dc}} \end{bmatrix} \begin{bmatrix} I_{o\_d} \\ I_{o\_q} \\ V_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} |\, v_{pcc} \,| \\ 0 \end{bmatrix}$$

i.e.

$$\begin{bmatrix} -R & X & N m_a \cos\delta_o \\ -X & -R & -N m_a \sin\delta_o \\ -m_a \cos\delta_o & m_a \sin\delta_o & -\dfrac{2}{R_{dc}} \end{bmatrix} \begin{bmatrix} I_{o\_d} \\ I_{o\_q} \\ V_{dc} \end{bmatrix} = \begin{bmatrix} |v_{pcc}| \\ 0 \\ 0 \end{bmatrix} \tag{3.29}$$

Where, $X = \omega_o L$. Now by solving (3.27) for $I_{o\_d}$, $I_{o\_q}$ and $V_{dc}$ the solutions are:

$$I_{o\_d} = -\frac{2R + N m_a^2 R_{dc} \sin^2\delta_o}{N m_a^2 R R_{dc} + 2R^2 + 2X^2} |v_{pcc}| \tag{3.30}$$

$$I_{o\_q} = \frac{(2X - N m_a^2 R_{dc} \sin\delta_o \cos\delta_o)}{N m_a^2 R R_{dc} + 2R^2 + 2X^2} |v_{pcc}| \tag{3.31}$$

$$V_{dc} = \frac{m_a R_{dc}(R\cos\delta_o + X\sin\delta_o)}{N m_a^2 R R_{dc} + 2R^2 + 2X^2} |v_{pcc}| \tag{3.32}$$

From (3.30), (3.31) and (3.32), it is apparent that $I_{o\_d}$, $I_{o\_q}$ and $V_{dc}$ in steady state, do not depend on the size of the capacitor. The CLS system (Figure 3.1), has Thevenin equivalent $R$ = 1.39 ohm and $X$ = 13.05 ohm (Figure 3.6a). For the given system, the steady state variations of the operating points $I_{o\_d}$, $I_{o\_q}$ and $V_{dc}$ against $\delta_o$ are plotted in Figure 3.8 with $m_a$=1.0. At steady-state, the reactive current $I_{o\_q}$ varies almost linearly with respect to $\delta_o$, and the range of $\delta_o$ for 1.0 pu swing in $I_{o\_q}$ is very small. For the delayed (or positive) value of $\delta_o$, the CLS supplies (i.e. capacitive mode) the reactive power to the line, hence $I_{o\_q}$ is negative and for the advanced (or negative) value of $\delta_o$, the CLS absorbs (i.e. inductive mode) VArs from the line, hence $I_{o\_q}$ is positive. The capacitor voltage, $V_{dc}$ also increases almost linearly with $\delta_o$ from advanced to delayed $\delta_o$. The active current, $I_{o\_d}$ is small and varies only a little with $\delta_o$ because it is required only to compensate the CLS losses and to maintain $V_{dc}$ constant at the desired level.

## 3.7. SUMMARY

The following points can be summarised from this chapter.

- The power circuit of the 3-phase 3-link (7-level) CLS system was modeled in EMTP-RV with its basic building blocks viz. a switch model, VSC link model, SPWM circuit model.
- Approximate static and dynamic models were developed for the proposed CLS system using the *dq*-transformations.
- The stability of the proposed CLS was verified using the Routh-Hurwitz criterion. The proposed CLS system is stable and the values of resistors, inductors and capacitors of the CLS circuit do not affect the stability.
- Only a small variation (typically less than 3°) of the phase angle ($\delta_o$) is required to control a large reactive current (or power) flow.
- These models will be used to design the control strategy whereby the phase angle of the modulating signal is controlled to control the CLS output voltage by adjusting the reactive current (or power) and hence to regulate the voltage at the PCC.

# CHAPTER-4

# OPEN-LOOP CONTROL & PRELIMINARY SIMULATION STUDY OF 1-PHASE CLS WITH EMTP-RV

## 4.1. INTRODUCTION

Equation (3.25) shows that either by adjusting the modulation index ($m_a$) or the phase angle ($\delta$), the CLS output voltage ($v_o$) can be controlled to regulate the reactive power (or current) and hence the voltage at the PCC ($v_{pcc}$). Although, the scope of this thesis is to develop the phase angle controller (i.e. selecting $\delta$ as the control input and keeping $m_a$ constant), it is essential to verify the algorithm shown in Chapter 3 by preliminary simulation using open-loop control. Therefore, an open-loop control strategy considering both $m_a$ and $\delta$ as the control inputs is explained in this chapter as a preliminary step towards the subsequent controller design. The performance and the operating limits of the CLS are explored for different values of the control inputs under different operating conditions by preliminary simulation study in EMTP-RV.

A novel technique, called the Rotated Gate Signal Pattern (RGSP), used for balancing the voltages of the link dc capacitors is explained in this chapter. The step-by-step start-up procedure of the CLS system is also described here.

The simulation of the CLS system in open-loop mode is also important to ensure the proper working of its developed power & gating circuit models. Therefore, a 1-phase, 3-link version of the CLS is used along with a 1-phase radial test transmission system, similar to the one that is shown in the single line diagram in Figure 3.1. The 1-phase CLS

system is simulated using open-loop control in EMTP-RV. The 1-phase version of the CLS system is suitable for analysis purposes at this stage to gain an insight into the operational behavior of this special type of STATCOM and based on this analysis, subsequently, a 3-phase CLS system with the closed-loop controller will be implemented next. The proposed CLS is connected at the end point of a radial transmission line (Figure 3.1) to stabilize the voltage by compensating the reactive power at the point of connection. The performance of the 1-phase CLS system is analyzed using open-loop control under both steady- and transient-state operating conditions and the results are presented here.

## 4.2. OPEN LOOP CONTROL PHILOSOPHY

In an ideal STATCOM, the voltage at the PCC ($v_{pcc}$) can be increased by supplying the reactive power (or current) to the power system and decreased by absorbing the reactive power (or current) from the power system. The same principle is applied to the CLS which is used to support the voltage at the PCC. The exchange of the reactive power (or current) between the CLS and the power system is controlled by adjusting the amplitude of the CLS output voltage. When the magnitude of the CLS output voltage is greater than that of the PCC, the CLS supplies the reactive power (or current) and operates in the capacitive mode. On the other hand, when the magnitude of the CLS output voltage is controlled to be less than that of the PCC, the CLS absorbs the reactive power (or current) and operates in the inductive mode. However, in practice, there are internal losses within the converter caused by the non-ideal power semiconductor devices and the passive components. As a result, without any control, the voltage on the dc capacitor will decrease. A small amount of real power from the power

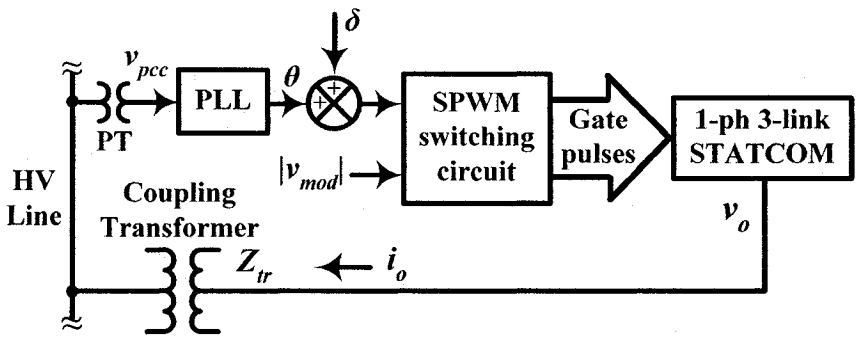


**Figure 4.1. Open-loop control of a 1-phase 3-link CLS.**

system needs to be absorbed to compensate for the internal losses and to regulate the dc capacitor voltage by introducing a small phase shift, $\delta$ between the CLS output voltage and the power system voltage at the PCC. In general, by adjusting amplitude & phase of the CLS output voltage, the exchange of real & reactive power (or current) can be controlled.

In the CLS, the output voltage ($v_o$) is generated by the SPWM technique. Therefore, its magnitude and phase can be controlled independently by adjusting the modulation index (or magnitude) and phase angle of the modulating signal (i.e. the angle between $v_{pcc}$ & $v_o$ ) respectively [2, 3, 5, 21-27].

For controlling the CLS output voltage in an open-loop control mode, the control signals $m_a$ (or $|v_{mod}|$ because $\sum_{1}^{3} \hat{V}_{tri} = 1$) and $\delta$ are adjusted manually, where $|v_{mod}|$ is the magnitude of the modulating signal and $\delta$ is the phase angle of the modulating signal (or the voltage angle between the voltages $v_{pcc}$ and $v_o$). The open-loop control (Figure 4.1) is employed here as a preliminary step to,

(a) Evaluate the overall operating range and behaviour of the CLS for the different values of the control inputs under different operating conditions, and

(b) Design the closed-loop controller based on this evaluation.

The voltage at the PCC, ($v_{pcc}$) is measured and fed as an input to the Phase Locked Loop (PLL) which outputs a phase angle ($\theta$) for synchronization of the CLS output voltage ($v_o$). The angle $\delta$ is then added to $\theta$ to generate the phase angle of the modulating signal, ($\theta + \delta$), which is then fed as one of the inputs to the SPWM switching circuit. The signal $|v_{mod}|$ is used as a second input to the SPWM circuit and the SPWM circuit outputs a set of switching signals thereby driving the switches of the CLS.

## 4.3. ROTATED GATE SIGNAL PATTERN (RGSP)

### 4.3.1. General

As shown in Figure 2.5, theoretically, the links are assigned to contribute 3-level output ac voltages of equal amplitudes but unequal pulse widths, to synthesize the multilevel CLS output voltage waveform. Unequal pulse widths of the link output voltages cause an unequal transfer of energy from dc to ac side of the converter. Therefore, each link faces unequal stresses and results in unbalanced dc voltages among the link dc capacitors. These unbalanced dc capacitor voltages introduce more harmonics in the CLS output voltage and current and reduce their fundamental components. To overcome the above mentioned problem, a control scheme known as 'rotated gate signal pattern' (RGSP) is used for a CLS which is explained next.

### 4.3.2. Basic principle

For a CLS having 3-links per phase, Figure 2.5a show a 7-level output phase voltage waveform ($v_o$) which is synthesized using 3-level link output voltages $v_1$, $v_2$ & $v_3$ of Link-1, -2 & -3 respectively. Based on the principle of operation of the CLS explained

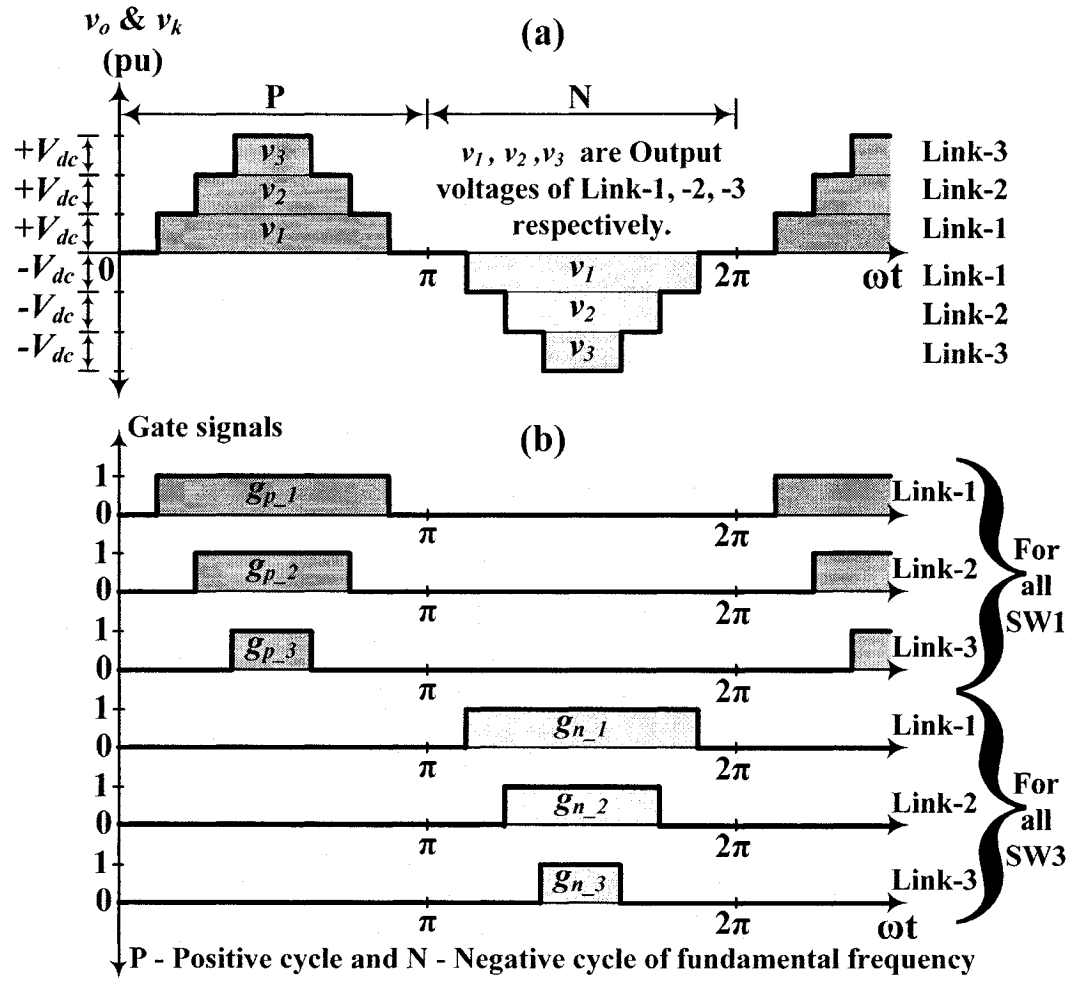


**Figure 4.2. (a) Output voltage waveform and (b) gate signals per phase without RGSP for a CLS having three-links per phase.**

in Chapter 2, without using RGSP, the gate signals required to drive the switches of the CLS are shown in Figure 4.2b.

In Figure 4.2b, $g_{p\_1}$, $g_{p\_2}$ & $g_{p\_3}$ form a positive group of the gate signals and used only for the positive group of the switches (i.e. switch SW1 of Link-1, -2 & -3 respectively). Similarly, $g_{n\_1}$, $g_{n\_2}$ & $g_{n\_3}$ form a negative group of the gate signals which are used only for the negative group of the switches (i.e. switch SW3 of Link-1, -2 & -3 respectively). The switches SW2 and SW4 of all three links are operated as shown in Table 2.1. Here, the positive group of the switches are the switches when turned on,

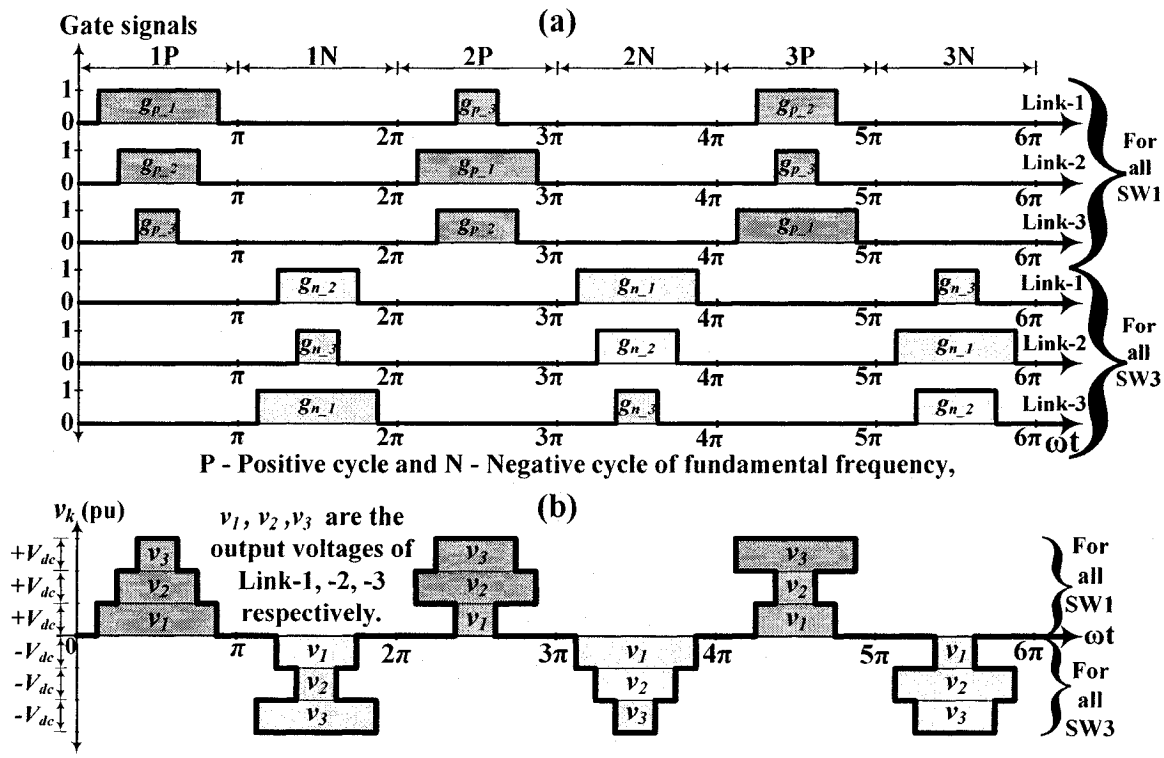


**Figure 4.3. (a) Rotated gate signal pattern (RGSP) per phase and (b) Link output voltages per phase, for a CLS having three-links per phase.**

contribute to synthesize the positive cycle (i.e. 'P' from Figure 4.2a) and negative group of the switches when turned on, contribute to synthesize the negative cycle (i.e. 'N' from Figure 4.2a) of $v_o$. It is important to note here that both groups of the switches cannot be simultaneously in the on state, to avoid short-circuiting of the link dc capacitors.

From the operating principle of a CLS, the gate signal patterns without RGSP (Figure 4.2b) are kept fixed for each link (i.e. $g_{p\_1}$ & $g_{n\_1}$ for Link-1, $g_{p\_2}$ & $g_{n\_2}$ for Link-2 and $g_{p\_3}$ & $g_{n\_3}$ for Link-3) so that each link contributes an output ac voltage of different pulse widths (and hence different amount of energy) to form the CLS output voltage waveform in a close approximation to the sine wave. But, in order to overcome the dc voltage unbalance among the link dc capacitors and to achieve equal stress distribution on the switching devices, the switching patterns of Figure 4.2b are rotated

among the links in every half cycle of the fundamental frequency as shown in Figure 4.3a. The sequence of rotation can also be easily understood from the Table 4.1. The link output voltages after rotating the gate signal patterns are as shown in Figure 4.3b but the CLS output voltage still remains as shown in Figure 4.2a.

It is important to note here that the switches SW2 and SW4 of all three links are turned on/off for the complete half cycle of the fundamental frequency (Table 2.1), hence they possess equal stress distribution on them and consequently, their corresponding gate signals need not be rotated.

For the CLS having 3-links per phase, the complete rotation of all the gate signals of both the groups (i.e. positive and negative) is completed in 3 cycles of the fundamental

**Table 4.1. Rotated gate signal pattern (RGSP) per phase for the CLS having 3-links per phase.**

| Rotating sequence | Cycle of fundamental frequency | Gate signal | For link | For switch group |
|---|---|---|---|---|
| 1P | 1st Positive | $g_{p\ 1}$ | 1 | Positive |
| | | $g_{p\ 2}$ | 2 | |
| | | $g_{p\ 3}$ | 3 | i.e.SW1s |
| 1N | 1st Negative | $g_{n\ 2}$ | 1 | Negative |
| | | $g_{n\ 3}$ | 2 | |
| | | $g_{n\ 1}$ | 3 | i.e.SW3s |
| 2P | 2nd Positive | $g_{p\ 3}$ | 1 | Positive |
| | | $g_{p\ 1}$ | 2 | |
| | | $g_{p\ 2}$ | 3 | i.e.SW1s |
| 2N | 2nd Negative | $g_{n\ 1}$ | 1 | Negative |
| | | $g_{n\ 2}$ | 2 | |
| | | $g_{n\ 3}$ | 3 | i.e.SW3s |
| 3P | 3rd Negative | $g_{p\ 2}$ | 1 | Positive |
| | | $g_{p\ 3}$ | 2 | |
| | | $g_{p\ 1}$ | 3 | i.e.SW1s |
| 3N | 3rd Negative | $g_{n\ 3}$ | 1 | Negative |
| | | $g_{n\ 1}$ | 2 | |
| | | $g_{n\ 2}$ | 3 | i.e.SW3s |

frequency (Figure 4.3a). Hence, theoretically, all the link dc capacitors are charged and discharged equally in every 3/2 cycle, causing balanced dc voltages on them. Consequently, each switch is turned on and off equally and results into the equal stress distribution. The employment of RGSP is verified by the preliminary simulation (Section 4.5).

As each link is a 1-phase full bridge rectifier, the dc voltages of the link dc capacitors contain a ripple (or ac component) of 120 Hz frequency. But the use of the rotated gate signal patterns introduces an additional ripple (or oscillations) in the dc voltage waveforms at a frequency of 40 Hz besides the ripple of 120 Hz frequency. This is because all link dc capacitors are charged and discharged equally in every 3/2 cycle (i.e. 60 x 2/3 = 40 Hz) of the fundamental frequency. For the proposed 3-link CLS, this low frequency ripple can be filtered out by employing a low pass filter of suitable design but at the expense of the reduction in the speed of the response.

It can be seen from above that the frequency of the low frequency ripple ($f_{r\_low}$) generated due to the use of the RGSP is inversely proportional to the number of links used in the CLS per phase.

i.e. $$f_{r\_low} = \frac{2f_o}{N} \qquad (4.1)$$

Where $f_o$ is the fundamental power system frequency of 60 Hz and $N$ is the number of links per phase in the CLS. In practice, 14 to 16 links per phase are used in the CLS. Therefore, by increasing the number of links per phase in the CLS, the low frequency ripple can be minimized and smoother, stable and balanced dc voltages can be obtained.

### 4.3.3. Control logic scheme of the rotated gate signal patterns in EMTP-RV.

Figure 4.4 shows the EMTP-RV model of the control logic scheme used to obtain the RGSP (Table 3.1 & Figure 4.3a), for the CLS having 3-links per phase.

As the main building blocks, the control logic scheme consists of two circular counters- one for counting positive and the other for counting negative half cycles, and six selectors- three for positive and three for negative group of the gate signals. For the 3-link CLS with the RGSP, as 3 cycles of the fundamental frequency are required to complete the full rotation of the gate signals (Figure 4.3a), after each positive (or negative) half cycle, the output of the corresponding positive (or negative) counter is

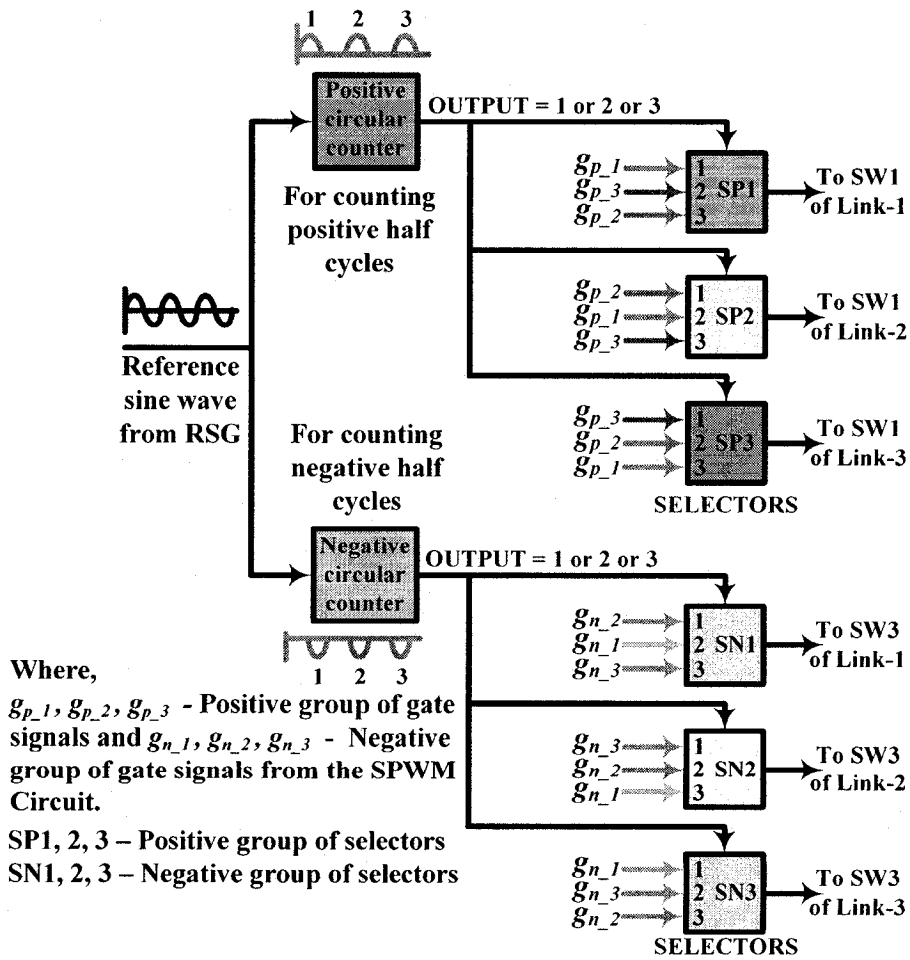


**Figure 4.4. Control logic scheme of the RGSP in EMTP-RV.**

incremented by one. The counter output is used to drive the corresponding three selectors of the positive (or negative) group which select the gate signal patterns from the positive (or negative) group of the gate signals based on the sequence shown in Table 4.1.

For example, for the first positive half cycle, the positive counter outputs 1, which drives all three selectors of the positive group to select the gate signals $g_{p\_1}$, $g_{p\_2}$, $g_{p\_3}$ for the positive group of the switches (SW1s) of Links-1, -2, -3 respectively, based on the rotating sequence 1P (Table 4.1). Similarly, for 2nd positive half cycle, the positive counter increments its output to 2, and the selectors now select the gate signals $g_{p\_3}$, $g_{p\_1}$, $g_{p\_2}$ for the positive group of the switches (SW1s) of Links-1, -2, -3 respectively, based on the rotating sequence 2P (Table 4.1). Above explained logic remains the same for the 3rd positive half cycle and also for all three negative half cycles. Aforementioned rotating sequence is repeated after every three positive (or negative) half cycles to obtain the RGSP for a 3-link version of the CLS. This principle can be extended for the CLS having *N*-links per phase.

## 4.4. START-UP PROCEDURE OF THE CLS

In practice, the task of starting up the CLS is to bring the reactive power output to a certain level in a very short time, while maintaining all the switching devices within their ratings. The challenge of starting up the CLS lies in the fact that, before start up, the dc capacitor voltages are zero.

An economic and convenient approach to start-up the CLS system is to use the ac system directly. As each of the series connected links per phase in the CLS is a 1-phase full bridge converter, with the gating signals to all the GTO switches are suppressed (or blocked), the CLS system behaves like several cascaded full bridge rectifiers with only

the dc capacitors as load (Figures 2.1 & 2.2a). Consequently, the ac system voltage charges up the dc capacitors through the reverse conducting (anti-parallel) diodes. However, there may be over current problems caused by the charging current of the dc capacitor or over charging of the capacitors since the leakage reactance of the transformer is small.

To avoid these problems, a pre-insertion resistor ($R_{start}$) is used in the CLS circuit during start-up. The methodology is explained below with the aid of Figures 2.1 & 3.1.

i. Insert $R_{start}$ in the ac side of the CLS (Figure 3.1) by closing CB1 & CB2 and keeping the switch S1 open. Suppress all the gate signals to the switches of the CLS, so the dc capacitors are charged through their corresponding rectifiers. The purpose of $R_{start}$ is to limit the initial charging current and thus limit the current through the anti-parallel diodes of the VSCs. As the three dc capacitors are equal, ideally they will be charged to the same dc voltage magnitude.

ii. After the dc voltage attains a certain level, $R_{start}$ is bypassed by the closure of S1, and the gating signals to the CLS switches are enabled. A small phase difference between $v_o$ and $v_{pcc}$ is maintained, so that the CLS can absorb real power from the system to supply its total component losses. Therefore, the dc voltages are further raised to their normal operating level.

iii. Once the dc voltages reach their normal operating levels, the CLS is put into regulation mode.

## 4.5. PRELIMINARY SIMULATION RESULTS

As a preliminary step towards the controller design, it is important to ensure the proper working of the developed power and gating circuits of the CLS system model as well as to observe & analyse its open-loop performance in steady and transient-state conditions.

### 4.5.1. Initialization of the CLS system

Based on the steps explained in Section 4.4, a simulation is carried out in EMTP-RV for a 1-phase, 3-link (or 7-level) version of the CLS using the open-loop control (Figure 4.1). Consequently, only the steps (i) and (ii) of the CLS start up procedure explained in Section 4.4 are carried out and the step no (iii) will be implemented

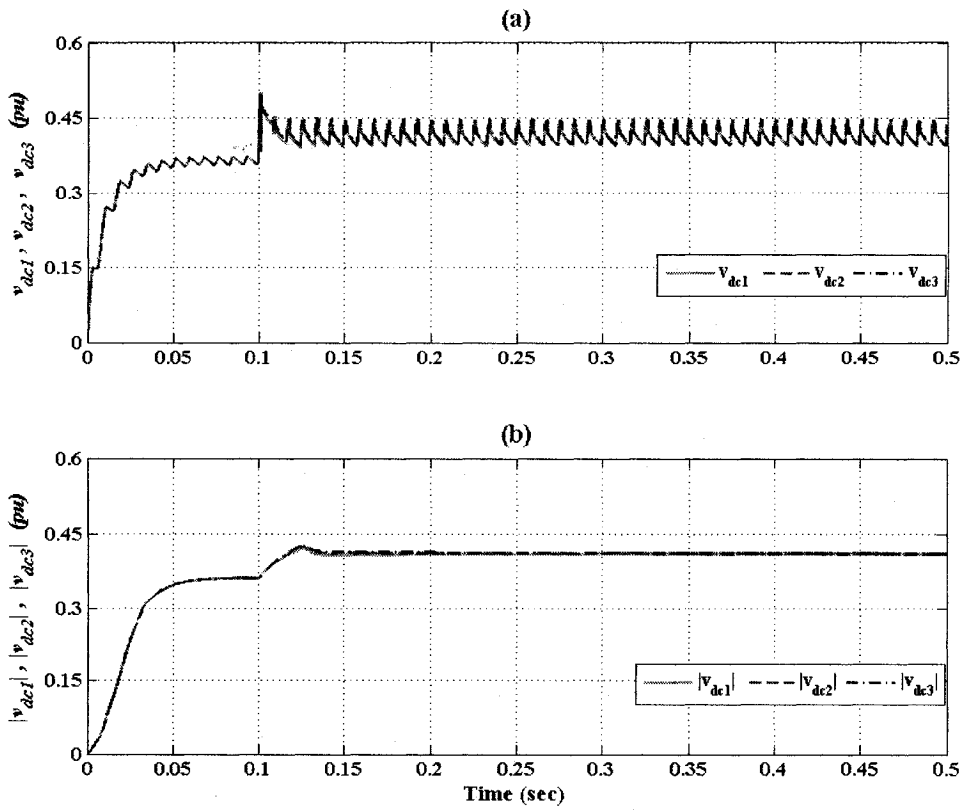


**Figure 4.5: (a) Instantaneous (b) average dc capacitor voltages of all three links of a 1-phase 3-link CLS.**

subsequently for the 3-phase version of the CLS with closed-loop control in Chapter 6. The results are as shown in Figure 4.5. The CLS system is in rectifying mode from 0 to about 100ms with the start up resistor $R_{start}$ into the CLS circuit. At about, 100ms, the start up resister, $R_{start}$ is bypassed by closing the circuit breaker (CB) and the gating signals of the CLS switches (GTOs) are enabled.

It is clearly observed from Figure 4.5 that, during the interval from about 100 to 140ms, the CLS absorbs more real power than its total component losses therefore its dc capacitor voltages (for all three link dc capacitors) keep on increasing until they reach to required level. At this level, there is no further change in the magnitude of the dc capacitor voltages and the real power absorbed by the CLS equals its total component losses. Therefore during the interval from about 140 to 500ms, the dc capacitor voltages are maintained at the same level. It is important to note here that the dc voltages of all three link dc capacitors are balanced in Figure 4.5 because of the employment of the RGSP which is also verified by simulations in the next section.

### 4.5.2. DC capacitor voltage balance

Theoretically, as the dc capacitors of all three links of the CLS are identical, they charge to equal dc voltage levels. However, without RGSP, all three link dc capacitors assume different dc voltage levels and exhibit dc voltage unbalance. This is because each link contributes the ac voltage of different pulse width i.e. different amount of energy (Figures 2.5 & 4.2) to synthesize the CLS output voltage waveform.

Therefore, to verify the principle of RGSP to balance the dc voltages, a simulation is carried out in EMTP-RV and the dc voltages of all three capacitors are observed without and with the employment of the RGSP.

Figures 4.6a & 4.6b show the simulated results of the instantaneous dc voltages and Figures 4.6c & 4.6d show the dc capacitor voltage magnitudes of all 3 links per phase without the RGSP and with the RGSP respectively. The simulated results confirm that, in the CLS, with the use of RGSP, balanced dc voltages are obtained. As a disadvantage, however, the RGSP introduces a low frequency ripple of a frequency approximately equal to $2f_s/N$ (here, as $N = 3$ links per phase, the ripple is at 40 Hz) superimposed on the second harmonic (120 Hz) ripple. However, increasing the number of links per phase in the CLS can largely minimize this low frequency ripple. In a practical scheme, a CLS with 16 links per phase [1, 10], the low frequency ripple in the link dc voltages and the harmonics in the output voltage of the CLS are much lower.

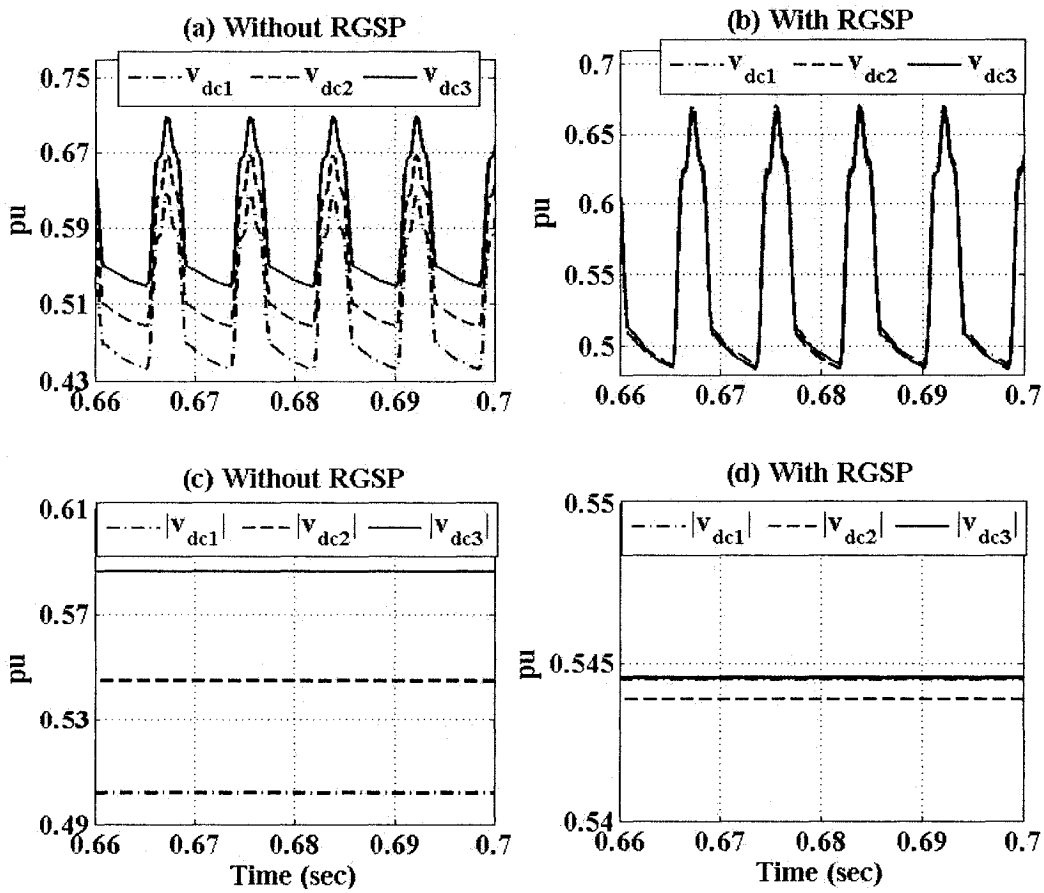


**Figure 4.6 Instantaneous dc voltages (a) without RGSP and (b) with RGSP. And dc voltage magnitudes (c) without RGSP and (d) with RGSP.**

### 4.5.3. Steady state performance

The steady state performance of a 1-phase 7-level (i.e. 3-link) version of the CLS system connected in the power system similar to that in Figure 3.1, is observed by a simulation in EMTP-RV. The steady-state waveforms of various voltage and current signals are recorded for understanding and verifying the CLS operational behavior.

The CLS output voltage ($v_o$) and output current ($i_o$) depend on the GTO switching. Since each GTO is switched on/off only once per cycle of the power frequency the switching losses in the CLS are lower than those of a conventional STATCOM [1, 10]. Based on (3.29), for the preliminary simulation, to get the maximum CLS output, the values of the control inputs are selected as $|v_{mod}|$ (or modulation index, $m_a$) = 1.0 volt and $\delta = -0.182^o$. The negative sign of $\delta$ indicates $v_o$ lags behind $v_{pcc}$.

***a. STATCOM output voltage, output currents and power system voltage.***

Figure 4.7a shows the power system voltage at the PCC ($v_{pcc}$) and its fundamental component ($v_{pcc1}$). It is clearly observed by comparing $v_{pcc}$ & $v_{pcc1}$ that $v_{pcc}$ is almost sinusoidal in nature and contains very few odd-ordered harmonics of very small magnitudes (Figure 4.9a).

Figure 4.7b shows the CLS output voltage ($v_o$) of the STATCOM and its fundamental component ($v_{o1}$). It is clearly observed by comparing $v_o$ & $v_{o1}$ that $v_o$ is almost sinusoidal in nature and contains few small magnitudes of odd-ordered harmonics (Figure 4.9b).

The notches & distortion in both the voltage waveforms are because of the switching transients due to the presence of the snubber circuit components. This is actually due to the compromise that has been made in the selection of snubber circuit

components to provide the protection to the switches against switching over voltages and over currents at the reduced snubber losses. Further optimization of the snubber circuit component values may reduce these notches & distortion in the voltage waveforms.

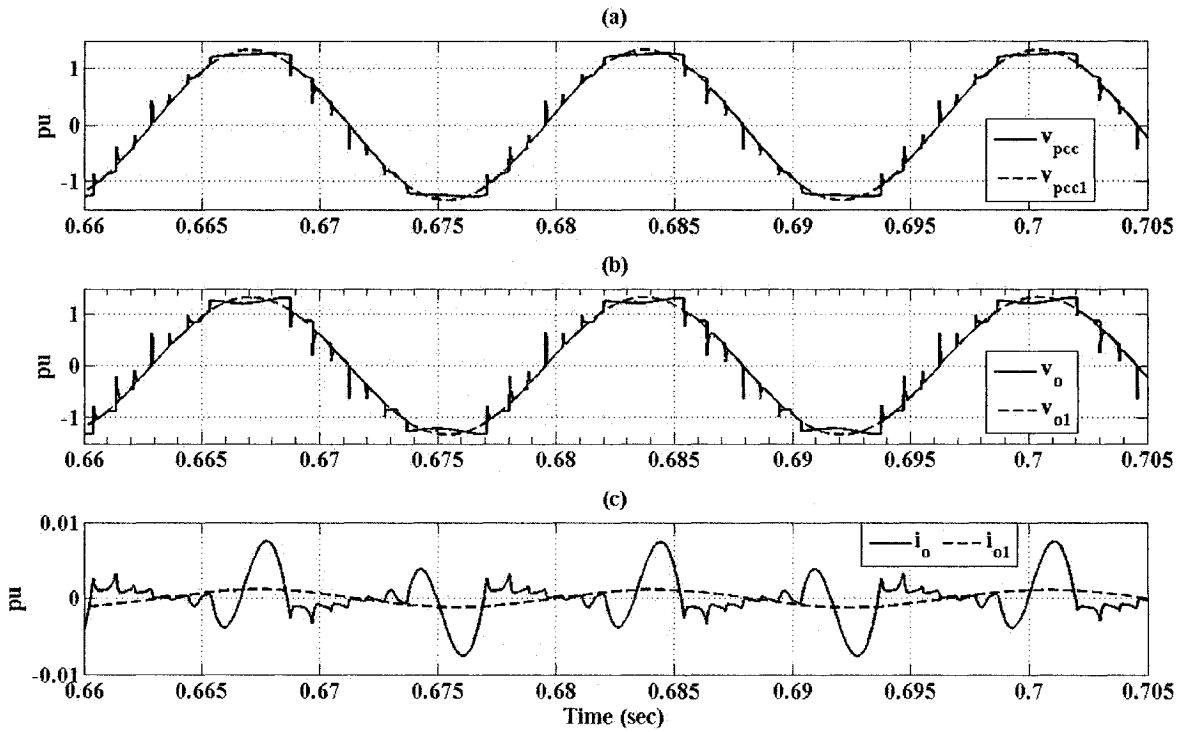


**Figure 4.7: Steady-state waveforms (a) $v_{pcc}$ (b) $v_o$ (c) $i_o$ of a 1-phase CLS having 3-links.**

Figure 4.8 shows the total harmonic distortion (THD) ratios of $v_{pcc}$ and $v_o$. As both the voltage waveforms are reasonably sinusoidal in nature, their THD ratios are less than 0.1 (or %THD is less than 10%). The THD can be further reduced by increasing the number of series connected links per phase. In a practical scheme with 14 to 16 links in series per phase, the %THD is observed to be less than 0.3% [13-15].

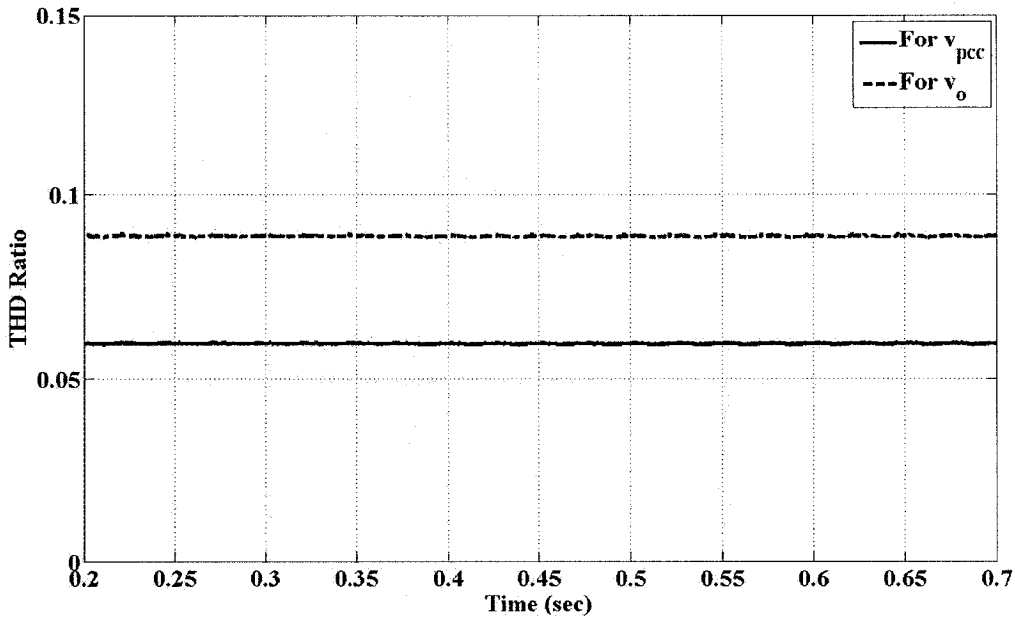


**Figure 4.8: Total harmonic distortion (THD) ratio of $v_o$ and $v_{pcc}$.**

Figure 4.7c shows the CLS output current ($i_o$) and its fundamental component ($i_{o1}$). After the GTO conduction, $i_o$ depends on the values of the transformer impedance and the CLS dc capacitance. Therefore, due to the interaction of the stored energy among these components, $i_o$ exhibits the positive and negative excursions per cycle of the power frequency and consequently, contains more harmonics. The harmonic spectrum of $i_o$, (Figure 4.9c) shows more predominant third harmonics & other odd-ordered harmonics. Here, $i_o$ exhibits more harmonics because of the 1-phase version of the CLS which comprises of only three chain links in series. A 3-phase delta connection of the CLS will eliminate the triplen harmonics (i.e. $3h$, where $h = 1, 2, 3, \ldots, n$) and the remaining harmonics can be further reduced by increasing the number of series-connected chain links per phase in the CLS.

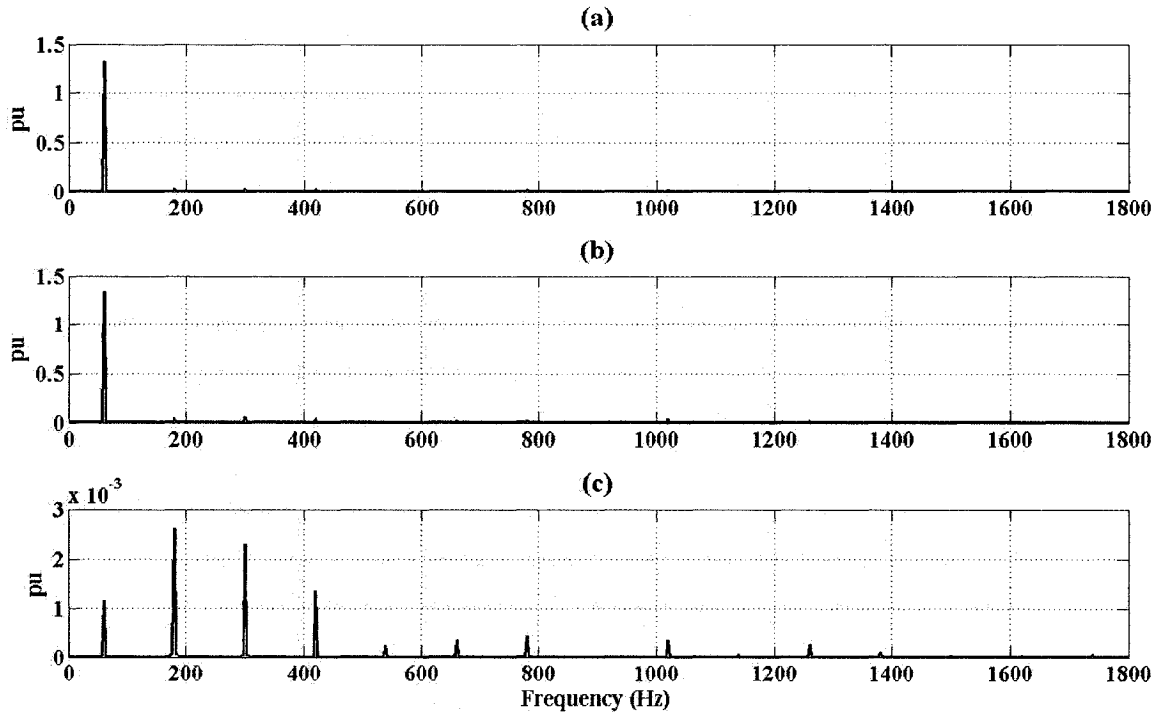


**Figure 4.9: Harmonic spectrums (a) $v_{pcc}$ (b) $v_o$ and (c) $i_o$.**

It is important to note here that the above shown simulated results are obtained without the use of harmonic filters. Therefore, the employment of small harmonic filters also improves the quality of voltage & current waveforms.

***b. Voltages and currents of a GTO switch and link ac voltages.***

Figure 4.10a shows the voltage across GTO thyristor $S_1$, ($v_{gto1}$) for all the three links. The switching instants and GTO conduction can be identified by observation of the instants of achieving zero GTO thyristor voltage. Due to the employment of the RGSP, $v_{gto1}$ of any individual link assumes different pulse width in every half cycle of the line frequency (Figure 4.10a). The peak amplitude and the shape of the wave top of all four GTO voltage waveforms in a particular link depend on their corresponding link dc capacitor voltage. As shown in Figure 4.10a, the peak amplitudes and the shape of the wave tops of $v_{gto1}$ of all three links, are same because all three link dc capacitor voltages

are balanced with the use of the RGSP. Without RGSP, as all link dc capacitors assume different amplitudes, the GTO voltages also assume different peak amplitudes in every individual link.

The current flowing through each GTO thyristor $S_1$ ($i_{gto1}$) is symmetrical and has only a negative excursion (Figure 4.10b). This is due to the unidirectional characteristic of a GTO thyristor, which allows the current to flow only from anode to cathode (i.e. here from dc to ac side in one direction only). The current flow from ac to dc side will be taken care of by the anti-parallel diode across the GTO.

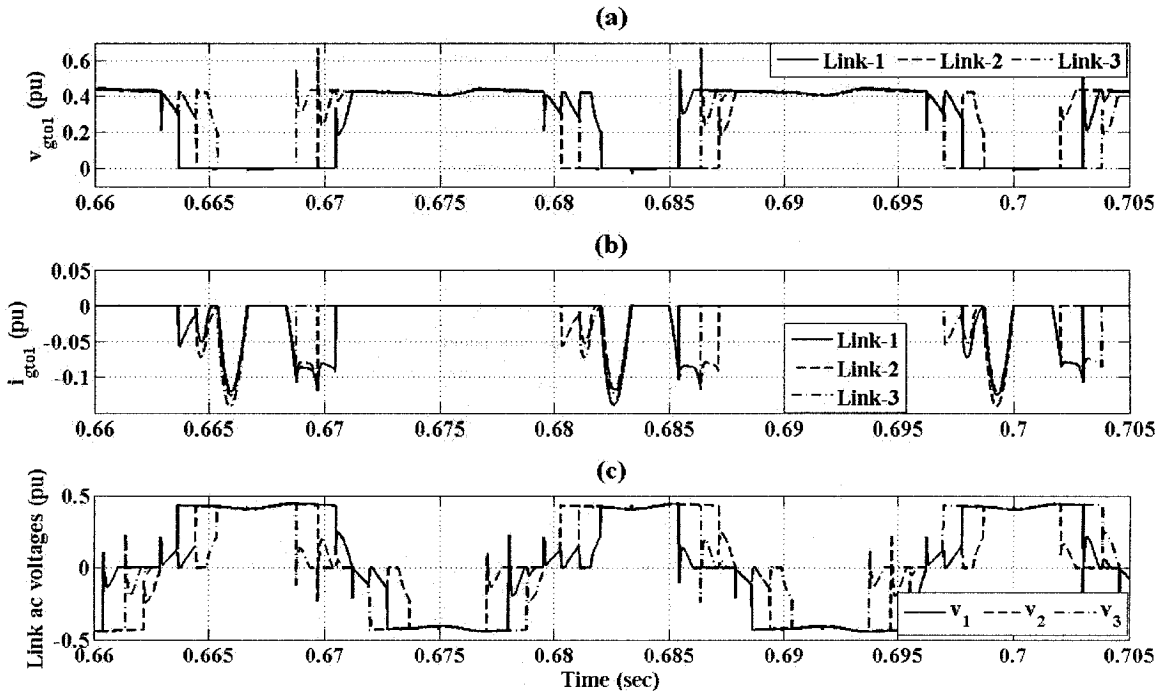


**Figure 4.10: Steady-state waveforms of (a) $v_{gto1}$ (b) $i_{gto1}$ and (c) Link ac voltages (i.e. $v_1$, $v_2$ & $v_3$) of all three links of a 1-phase CLS.**

The link ac voltages $v_1$, $v_2$ and $v_3$ at the ac terminals of the links 1, 2 and 3 respectively are shown in Figure 4.10c. Due to the series connection of these links on their respective ac sides, the summation of link voltages will contribute to form the CLS

output voltage, $v_o$. Similar to the GTO voltage, the peak amplitude and the shape of the wave top of the link ac voltage in a particular link depends on that of its corresponding link dc capacitor voltage and hence on the ripple content of the link dc capacitor voltage. Here, all the three link ac voltages achieve equal peak amplitudes and are balanced as all three link dc capacitors have balanced dc voltages on them with the employment of the RGSP. If the link dc voltages are not balanced (i.e. without RGSP) then the link ac voltages assume different peak amplitudes depending upon the ripple content of the link dc capacitor voltages which consequently exhibit voltage unbalance and cause more harmonics in the CLS output voltage and current. Due to the use of RGSP, $v_1$, $v_2$ and $v_3$ assume different pulse widths in every half cycle of the line frequency (Figure 4.10c). The notches in the waveforms of the link ac voltages (Figure 4.10c) are due to the presence of snubber circuit components and the losses associated with them.

***c. DC voltages and currents***

Here, the steady-state waveforms of the dc voltage and current of the dc capacitor of only link-1 are shown in Figure 4.11 for clarity. Those of the other two link dc capacitors have the identical wave shapes.

The capacitor used for the voltage support on the dc side of each link has a finite value. Hence the dc voltage across it contains considerable ripple at twice the power (or fundamental) frequency (i.e. $2f_o$ = 120 Hz) as shown in Figure 4.11a. This ripple can be minimized and the dc capacitor voltage can be smoothened by careful selection of the value of passive components of the CLS system. The charging/discharging of the dc capacitor depends on the magnitude the CLS output voltage ($v_o$), the power system

voltage ($v_{pcc}$), the voltage angle ($\delta$), the transformer impedance ($Z_{tr}$), the dc capacitance ($C_{dc}$) and the instants of GTO switching.

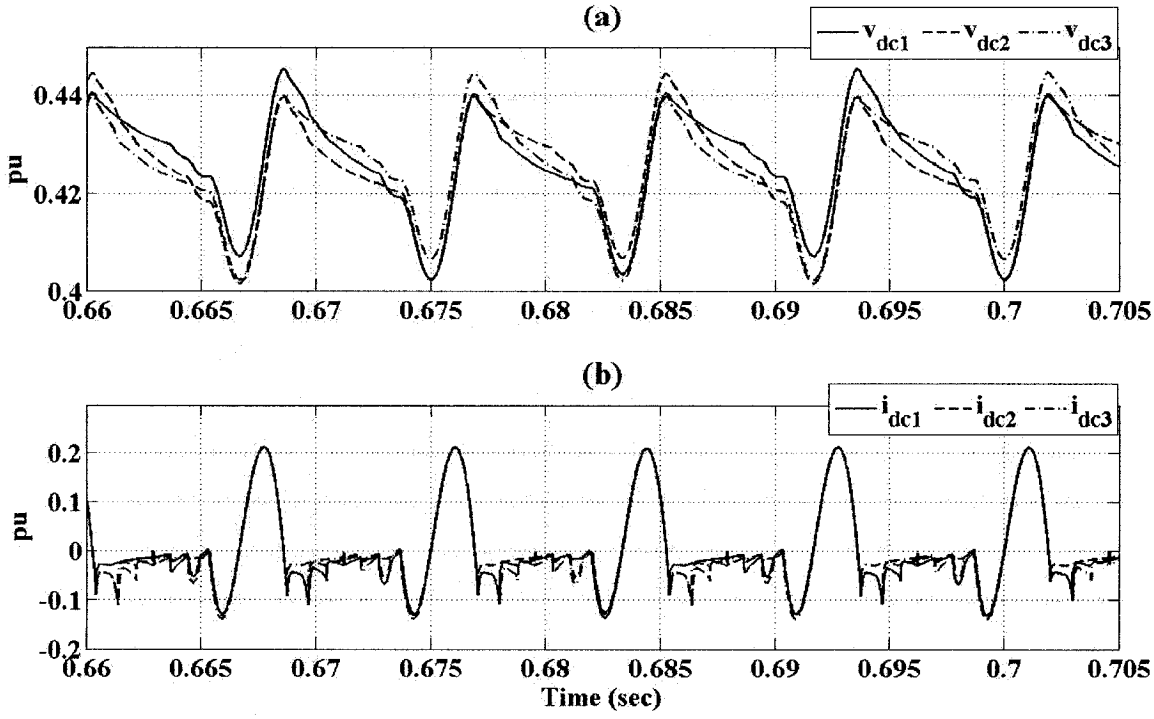


**Figure 4.11: Steady-state waveforms of (a) the dc voltage, $v_{dc1}$ and (b) the dc current, $i_{dc1}$ of link-1, -2 & -3.**

As seen earlier, with the use of RGSP, the dc voltages of all three links are balanced and assume nearly the same voltage level (Figure 4.6c & 4.6d). But, for a 3-link version of the CLS, this control scheme introduces low frequency ripple in the dc voltage waveform at 2/3$^{rd}$ of the line frequency (i.e. 40 Hz) in addition to the ripple at 120 Hz (Figure 4.11a). This ripple can be filtered out by using a low pass filter of a suitable design, but at the expense of a reduced speed of the response. As explained earlier in Chapter 3, the frequency of the ripple generated with the use of RGSP is inversely proportional to the number of links used in the CLS per phase. Therefore, the frequency of oscillations can be minimized and smoother, stable and balanced dc voltages can be

obtained employing RGSP, by increasing the number of links per phase. Consequently, it reduces the harmonics from the CLS output voltage and current.

Figure 4.11b shows the steady state waveforms of the dc current of link-1. It shows positive/negative excursions because of the exchange of energy among the passive components on the ac and dc sides due to the resonance condition. The frequency of these excursions depends upon the values of the passive components of the CLS system, $\delta$ and the magnitude of the CLS output current ($|i_o|$).

### 4.5.4. Transient state performance

To evaluate the performance of the proposed STATCOM in the transient-state condition, positive and negative step-changes are introduced in the control inputs $|v_{mod}|$ & $\delta$. Based on (3.29), to get the maximum CLS output, the values of the control inputs are selected as $|v_{mod}|$ (or $m_a$) = 1.0 volt and $\delta = -0.182°$. The negative sign of $\delta$ indicates $v_o$ lags behind $v_{pcc}$. The CLS system in the open-loop control mode is simulated in EMTP-RV using a 10 μs time-step. A small time-step is needed for accurate simulation. Various signals are recorded for observing the response and operational behavior of the CLS system and the performance results are presented next.

***a. Step-change in $|v_{mod}|$.***

As a first test, a small step-change of ±2% in the value of $|v_{mod}|$ is initiated at about 0.6 and 1.3 sec. respectively for the duration of 300 ms each (Figure 4.12a). The step-change of ±2% is chosen after few careful trial simulation runs to obtain stable CLS operation at the given values of control inputs and circuit components in the absence of controllers. For larger step changes than ±2%, the circuit components and control input

values need to be revised. The signals observed are (from top to bottom): (a) $|v_{mod}|$ (b) $|v_{pcc}|$ (c) $|v_o|$ (d) $|i_o|$ (e) $|v_{dc1}|$, $|v_{dc2}|$, and $|v_{dc3}|$ in pu.

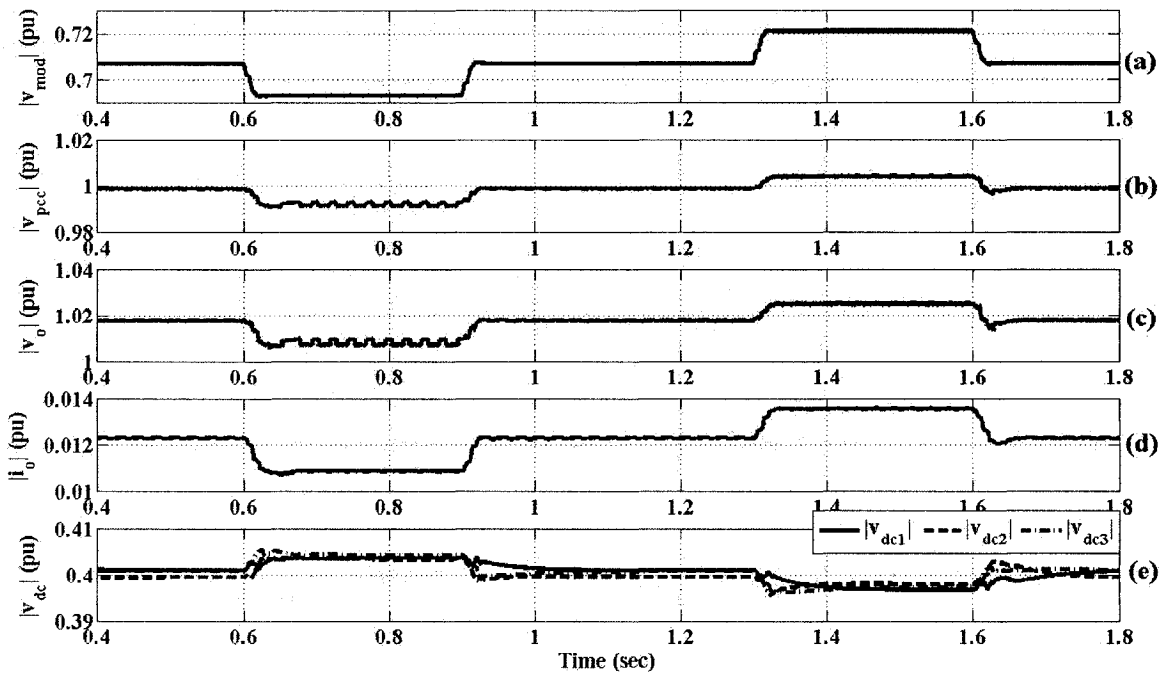


**Figure 4.12: Transient-state performance, ±2% Step-change in $|v_{mod}|$.**

The voltages $v_{pcc}$ and $v_o$ respond to ±2% step-change in $|v_{mod}|$ and their magnitudes decrease with the negative change in $|v_{mod}|$ and increase with the positive change in $|v_{mod}|$, for the periods of about 0.6 to 0.9 sec and 1.3 to 1.6 sec respectively (Figure 4.12b & 4.12c). In the absence of the ac voltage controller, during the negative step-change in $|v_{mod}|$, both the voltage magnitudes exhibit small oscillations but remain stable.

The change in the magnitudes of $v_o$ and $v_{pcc}$ are due to the change in the reactive current (or power) output of the CLS system. Therefore, by reducing $|v_{mod}|$ the CLS absorbs the reactive current (or power) and by increasing $|v_{mod}|$, the CLS supplies reactive current (or power). This phenomenon is shown in Figure 4.12d, where the CLS output current ($i_o$) respond to the negative and positive change in $|v_{mod}|$ and as a result,

approximately during 0.6 to 0.9 sec, it decreases (i.e. the CLS absorbs reactive power), and approximately during 1.3 to 1.6 sec, it increases (i.e. the CLS supplies reactive power) respectively.

Figure 4.12e shows the response of the dc voltages of all three link dc capacitors due to the step-change in $|v_{mod}|$. Due to the negative step-change in $|v_{mod}|$, the CLS absorbs reactive current (or power) and hence, the link dc capacitor voltages tend to increase. Whereas, because of the positive step-change in $|v_{mod}|$, the CLS supplies reactive current (or power) and the link dc capacitor voltages tend to decrease. It is clear from the Figure 4.12e that the link dc voltages are closely balanced within ±0.2% due to the employment of the RGSP.

***b. Step change in $\delta$.***

In the second test, a step-change of ±5% in the value $\delta$ is initiated at about 2.0 and 2.7 sec. respectively, for the duration of 300 ms each (Figure 4.13a). Similar to the step change in $|v_{mod}|$, the step-change of ±5% for $\delta$ is chosen after few careful trial simulation runs to obtain stable CLS operation at the given values of control inputs and circuit components in the absence of controllers. For larger step-change than ±5%, the circuit components and control inputs values need to be revised. The signals observed are (from top to bottom): (a) $\delta$ (b) $|v_{pcc}|$ (c) $|v_o|$ (d) $|i_o|$ (e) $|v_{dc1}|$, $|v_{dc2}|$, and $|v_{dc3}|$.

It is clear from Figure 4.13b & 4.13c that, the voltages $v_{pcc}$ and $v_o$ respond to the positive and negative step-changes in $\delta$. Consequently, the increment of $\delta$ on the negative side (from approximately 2 to 2.3 sec) results in the increment of the voltage magnitudes and vice versa for the period from about 2.7 to 3.0 sec.

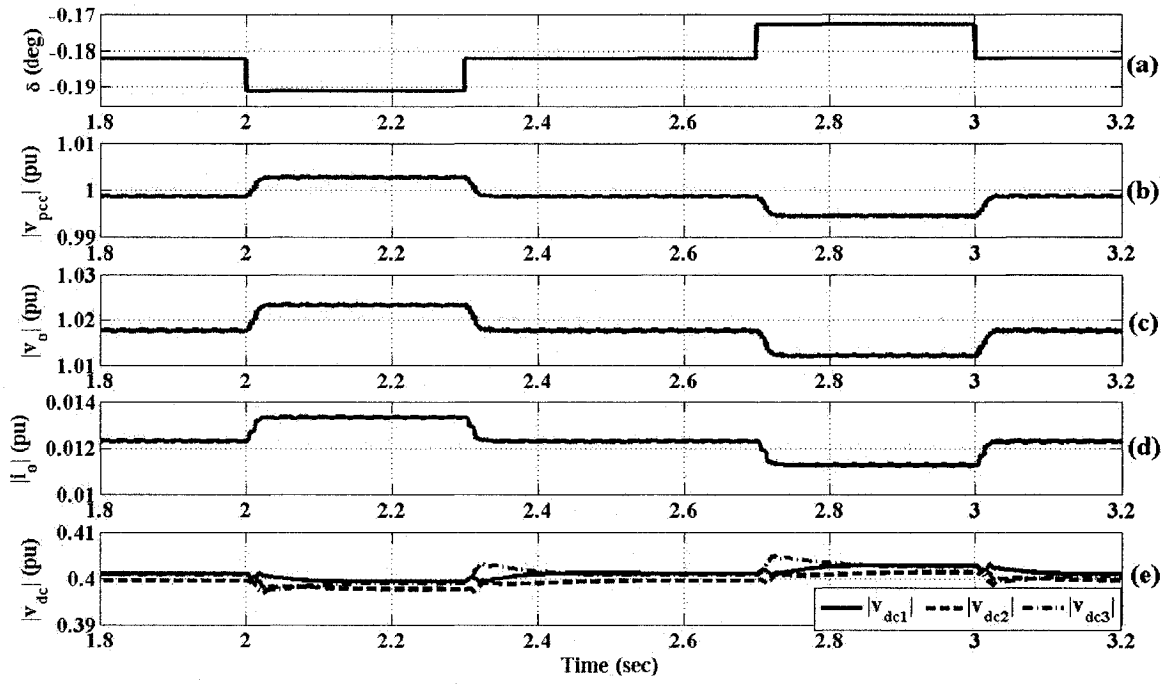


**Figure 4.13: Transient-state performance, ±5% Step change in $\delta$.**

As explained earlier, the change in the magnitudes of $v_{pcc}$ and $v_o$ are because of the change in the reactive current (or power) output of the CLS system. Therefore, by increasing $\delta$ on the negative side, the CLS supplies reactive current (or power) and by decreasing $\delta$ on the negative side, the CLS absorbs the reactive current (or power). This phenomenon is shown in Figure 4.13d, where $i_o$ responds to the positive and negative step-changes in $\delta$ and as a result, it increases (i.e. the CLS supplies reactive power) approximately from 2 to 2.3 sec and decreases (i.e. the CLS absorbs reactive power) approximately from 2.7 to 3.0 sec respectively.

Figure 4.13e shows the response of the dc voltages of all three link dc capacitors due to the step-change in $\delta$. Due to the positive step-change in $\delta$, the CLS supplies reactive current (or power) and hence, the link dc capacitor voltages tend to decrease. Whereas, due to the negative step-change in $\delta$, the CLS absorbs reactive current (or

power) and the link dc capacitor voltages tend to increase. In this test also, the dc voltages are closely balanced within ±0.2% due to the employment of the RGSP (Figure 4.13f).

## 4.6. DISCUSSION & CONCLUSIONS

It can be clearly seen from the aforementioned simulated results that the responses of the CLS system during the steady-state and transient-state conditions are stable. Also after each transient disturbance, the circuit returns to the steady-state showing stable operation of the CLS. Consequently, the simulation results validate that the magnitude and the angle of the CLS output voltage ($v_o$) can be controlled by altering the $|v_{mod}|$ and $\delta$, to stabilize the power system voltage ($v_{pcc}$). Moreover, the dc voltages of the link dc capacitors can be balanced by using a novel control technique called as the RGSP. Furthermore, the presence of a pre-insertion resistor during the start-up of the CLS, charges the link dc capacitors to the desired voltage level by limiting the CLS inrush current to the switch rating.

# CHAPTER-5

# CLOSED-LOOP CONTROL STRATEGIES & DESIGN OF CONTROLLERS

## 5.1. INTRODUCTION

For the proposed CLS system, from (3.26), the closed-loop controllers are developed by assuming $m_a$ constant and $\delta$ as a control input [22] to obtain the dynamic control of the magnitude of the power system voltage ($|v_{pcc}|$) at the PCC by adjusting the output voltage of the CLS and thereby regulating the flow of the reactive power ($Q_o$) or current ($i_{o\_q}$) at the PCC. Based on the linear set of equations obtained around the equilibrium point $\delta_o$ as per (3.26), the relationships between $\Delta i_{o\_q}$ & $\Delta\delta$ and $\Delta|v_{pcc}|$ & $\Delta i_{o\_q}$ are developed. Where, the controller designed using the former is called as the reactive current controller and that using the later as the ac voltage controller. Both the closed-loop cascaded controllers along with their block diagrams are explained in the subsequent sections.

## 5.2. OPEN LOOP TRANSFER FUNCTIONS (OLTF)

### 5.2.1. OLTF-1: Relationship between $\Delta i_{o\_q}$ & $\Delta\delta$

From the preliminary evaluation of the 1-phase, 3-link CLS (Chapter 4) and (3.26) , it is clear that the control input $\Delta\delta$ influences the system states. Therefore, from (3.26),

$$\frac{d\Delta i_{o\_q}}{dt} = -\omega_o \Delta i_{o\_d} - \frac{R}{L}\Delta i_{o\_q} - \frac{N m_a \sin\delta_o}{L}\Delta V_{dc} - \frac{1}{L}\Delta v_{pcc\_q} - \frac{N m_a V_{dco}\cos\delta_o}{L}\Delta\delta \tag{5.1}$$

Rearranging and taking the Laplace transform of (5.1)

$$\begin{aligned}(s+\frac{R}{L})\Delta I_{o\_q}(s) = &-\omega_o \Delta I_{o\_d}(s) - \frac{N m_a \sin\delta_o}{L}\Delta V_{dc}(s) \\ &- \frac{1}{L}\Delta V_{pcc\_q}(s) - \frac{N m_a V_{dco}\cos\delta_o}{L}\Delta\delta(s)\end{aligned} \tag{5.2}$$

Now, for obtaining the approximate relationship between $\Delta I_{o\_q}(s)$ and $\Delta\delta(s)$ in order to design the reactive current (or inner) control loop of the CLS, substitute zero for the term containing $\Delta I_{o\_d}(s)$ as it is very small. Moreover, $\Delta V_{pcc\_q}(s) = 0$ and from Figure 3.8, $\delta_o$ = −0.214° ≈ 0. Therefore, by assuming that the equilibrium point is at $\delta_o \approx 0$, the corresponding approximate first-order OLTF relating $\Delta i_{o\_q}$ & $\Delta\delta$ is obtained as:

$$\frac{\Delta I_{o\_q}(s)}{\Delta\delta(s)} \approx -\frac{N m_a V_{dco}}{L(s+\frac{R}{L})} \tag{5.3}$$

### 5.2.2. OLTF-2: Relationship between: $\Delta v_{pcc\_d}$ & $\Delta i_{o\_q}$

The reactive current $i_{o\_q}$ is regulated to stabilize the voltage at the PCC ($v_{pcc}$). Therefore, by neglecting the losses (as $R << X = \omega_o L$) and applying KVL in Figure 3.6, the relationship between $\Delta v_{pcc\_d}$ & $\Delta i_{o\_q}$ is obtained as:

$$jX\bar{I}_o = \bar{V}_o - \bar{V}_{pcc} \tag{5.4}$$

By substituting in (5.4): $\bar{V}_{pcc} = \sqrt{2}\,V_{pcc} = v_{pcc\_d} = |\,v_{pcc}\,|$,

$\bar{V}_o = \sqrt{2}\,V_o\,e^{-j\delta} = v_{o\_d} + j\,v_{o\_q} = N m_a V_{dc}\,(\cos\delta - j\sin\delta)$ and

$\bar{I}_o = \sqrt{2}\,I_o\,e^{j\pi/2} = j i_{o\_q}$

$$v_{pcc\_d} = (v_{o\_d} + j\, v_{o\_q}) + \omega_o L\, i_{o\_q} \tag{5.5}$$

Therefore, by changing the current $i_{o\_q}$, the magnitude of the ac voltage can be changed and the relationship between $\Delta v_{pcc\_d}$ and $\Delta i_{o\_q}$ in Laplace domain can be obtained as:

$$\frac{\Delta V_{pcc\_d}(s)}{\Delta I_{o\_q}(s)} \approx X \tag{5.6}$$

Where, $\Delta V_{pcc\_d} = \Delta|v_{pcc}|$.

## 5.3. REACTIVE CURRENT & AC VOLTAGE CONTROLLERS

Based on (5.3) and (5.6), two cascaded (reactive current or inner & ac voltage or outer) control-loops are developed by using PI controllers from the feedback of the transmission system voltage ($v_{pcc}$) and the CLS output reactive current ($i_{o\_q}$) (Figure 5.1). The block diagrams of both the control-loops are shown in Figure 5.2. To simplify the controller design, it is assumed that the two control-loops are relatively independent of

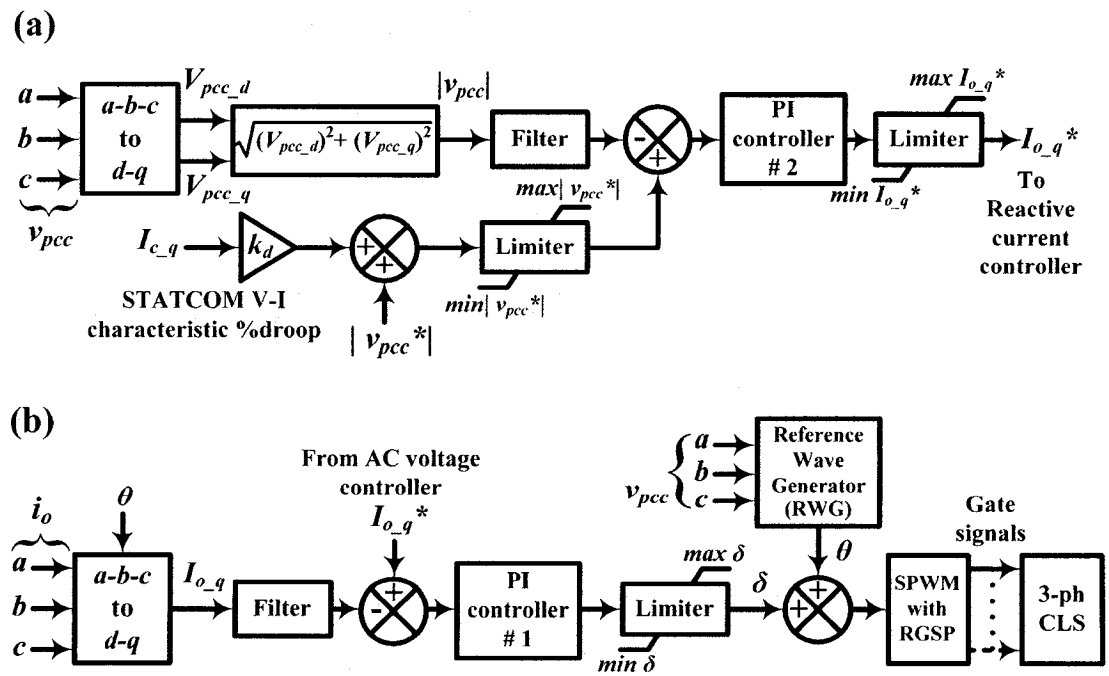


**Figure 5.1: (a) AC voltage and (b) reactive current controllers.**

each other. The measurement system calculates the magnitudes of $v_{pcc}$ and $i_{o\_q}$ in a synchronously rotating reference frame ($dq$-axis). The reference wave generator (RWG) calculates the angular position ($\theta$) of the vector. Two first-order low-pass filters (LPF) with the delays $1/(1+s\tau_{f2})$ & $1/(1+s\tau_{f1})$, are used in the feedback path of $|v_{pcc}|$ & $I_{o\_q}$, respectively. The magnitude of the reference voltage at the PCC ($|v_{pcc}^*|$) is compared with the actual value ($|v_{pcc}|$) in the outer control-loop and the reference quadrature current magnitude ($I_{o\_q}^*$) is obtained by error amplification using PI controller-2. This reference current magnitude is then compared with the actual current magnitude ($I_{o\_q}$) in the inner control-loop and by error amplification using PI controller-1, the phase angle, $\delta$ is obtained. The angle $\delta$ is added to the angular reference position ($\theta$) to generate the switching signals using SPWM. Due to the change in $\delta$, $V_{dc}$ and hence $v_o$ changes to regulate the flow of $i_{o\_q}$ which consequently stabilizes $v_{pcc}$. Limiters are used in the control circuit to prevent overshoot and saturation of the controllers. A droop ($k_d$) of about 1-3% in the V-I characteristic of the CLS is introduced for the fast dynamic response.

## 5.4. DESIGN OF CONTROLLERS

Based on the system model and control strategies explained in the preceding sections, the controllers are designed using the system parameters as shown in the Appendix A to meet the design specifications such as minimum phase margin (Pm) of 55° at the inner and outer controller gain crossover frequencies of $\omega_{x1}$=151 rad/sec ($\approx 2\pi f_c/5$, where $f_c$ = 120 Hz) & $\omega_{x2}$=30 rad/sec ($\approx \omega_{x1}/5$) respectively. The controller design calculations are shown in Appendix B.

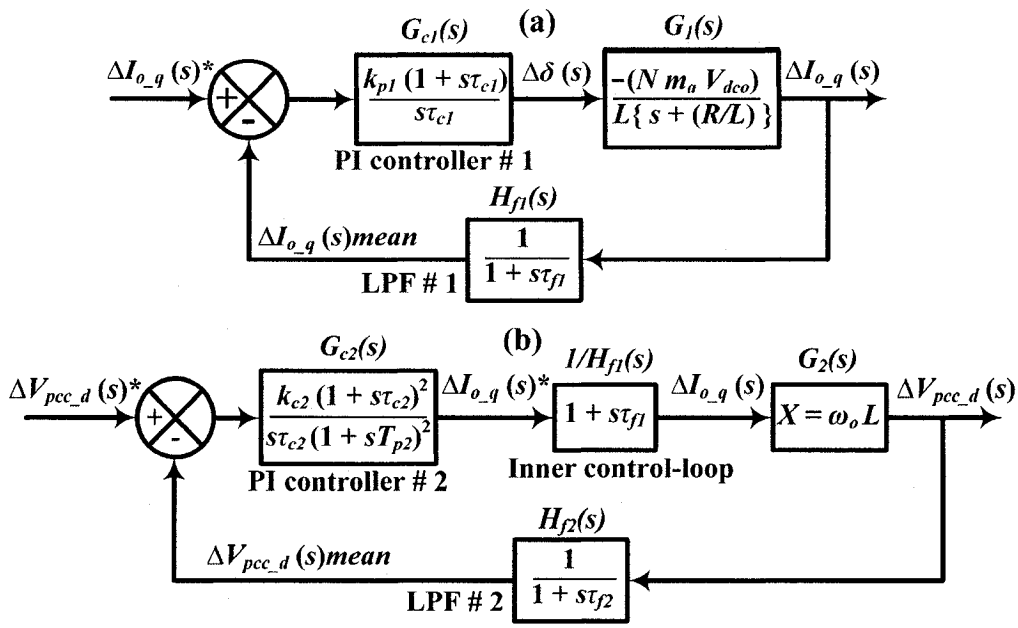


**Figure 5.2: Block diagrams of (a) inner (reactive current), and (b) outer (ac voltage) control-loops.**

### 5.4.1. Inner reactive current control loop

Figure 5.3 shows the bode plots of the open-loop transfer function $OLTF_i(s)$ and compensated-loop transfer function $LTF_i(s)$ of the inner reactive current control loop. Due to the negative sign of $G_1(s)$ the phase response in Figure 5.3 is positive. Consequently, a large phase lag of 203.2° is required to be compensated to achieve the desired Pm at $\omega_{x1}$=151 rad/sec. The negative sign of the open-loop gain is compensated by selecting the gains of the PI controller with negative signs and thereby an additional 180° phase lag is also obtained. As a result, the phase lag of only 23.2° (i.e. $\angle G_{c1}(j\omega_{x1})$= −23.2°) is to be compensated by the PI controller to meet the design specifications. This compensation is achieved by selecting a first-order PI controller having the transfer function as shown by (5.7) [28].

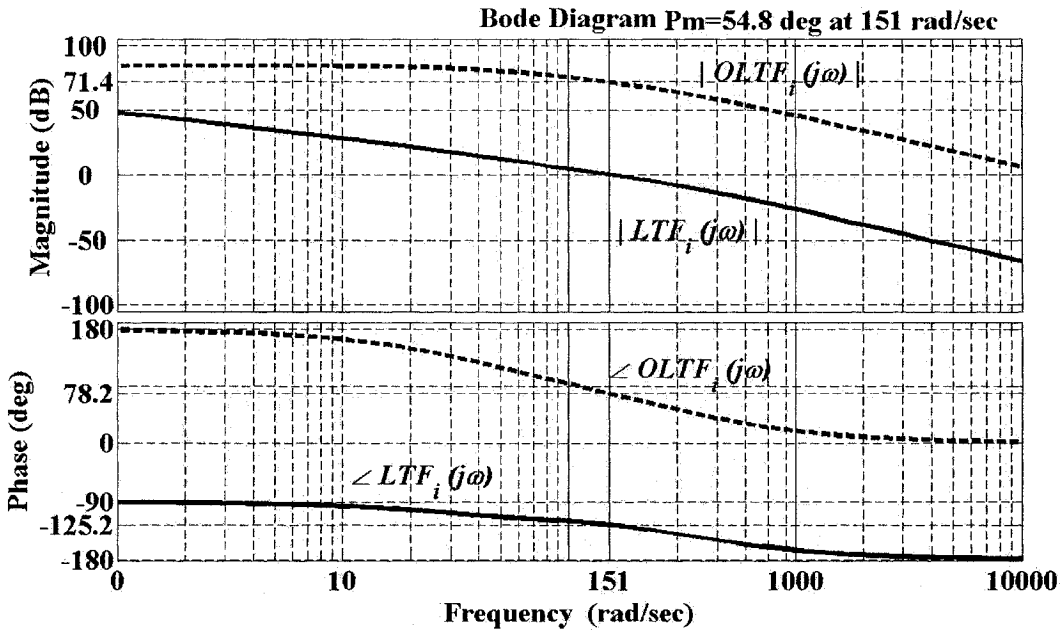


**Figure 5.3: Bode plots of inner reactive current control loop for $OLTF_i(s) = G_1(s).H_{f1}(s)$ & $LTF_i(s) = G_{c1}(s).G_1(s).H_{f1}(s)$.**

$$G_{c1}(s) = \frac{k_{p1}(1+\tau_{c1}s)}{s\tau_{c1}} \qquad \text{where,} \quad \tau_{c1} = \frac{k_{p1}}{k_{i1}} \tag{5.7}$$

The designed inner loop PI controller parameters for the studied CLS system are as follows:

| | | |
|---|---|---|
| $k_{p1}$ | : | -2.5 x $10^{-4}$ |
| $k_{i1}$ | : | -0.0162 |
| $\tau_{c1}$ | : | 15.45 ms |
| Phase margin ($Pm_i$) | : | 54.8° |
| Band width ($BW_i$) | : | 151 rad/sec |

The step response of the compensated closed-loop feedback transfer function $CLTF_i(s)$ of the inner reactive current control loop is stable and has the approximate %overshoot of 20% & settling time of around two cycles (Figure 5.4).

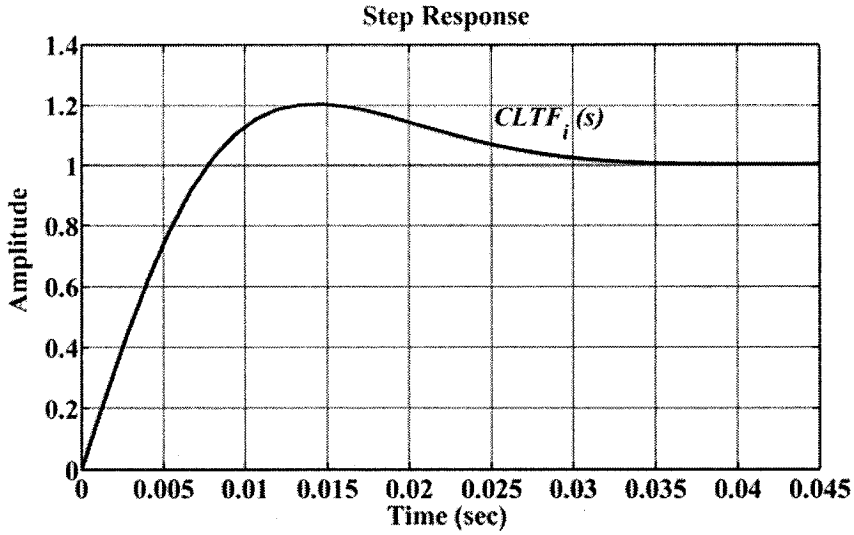


**Figure 5.4: Step response of the inner reactive current control loop *i.e.* $CLTF_i(s) = \{G_{c1}(s).G_1(s)\} / \{1+G_{c1}(s).G_1(s).H_{f1}(s)\}$.**

### 5.4.2. Outer ac voltage control loop

The bode plots of the open-loop transfer function $OLTF_o(s)$ and compensated-loop transfer function $LTF_o(s)$ of the outer ac voltage control loop are shown in Figure 5.5. In this case, from the open-loop response, as the phase lag of 117.6° (i.e. $\angle G_{c2}(j\omega_{x2}) = -117.6°$) is required to be compensated, a third-order PI controller having the transfer function as shown by (5.8) is designed to achieve the design specifications [28].

$$G_{c2}(s) = \frac{k_{c2}(1+s\tau_{c2})^2}{s\tau_{c2}(1+sT_{p2})^2} \tag{5.8}$$

where, $\tau_{c2} = \dfrac{k}{\omega_{x2}}$ , $T_{p2} = \dfrac{1}{k\omega_{x2}}$ & $k = \tan\left(\dfrac{\angle G_{c2}(j\omega_{x2}) + 90°}{4} + 45°\right)$

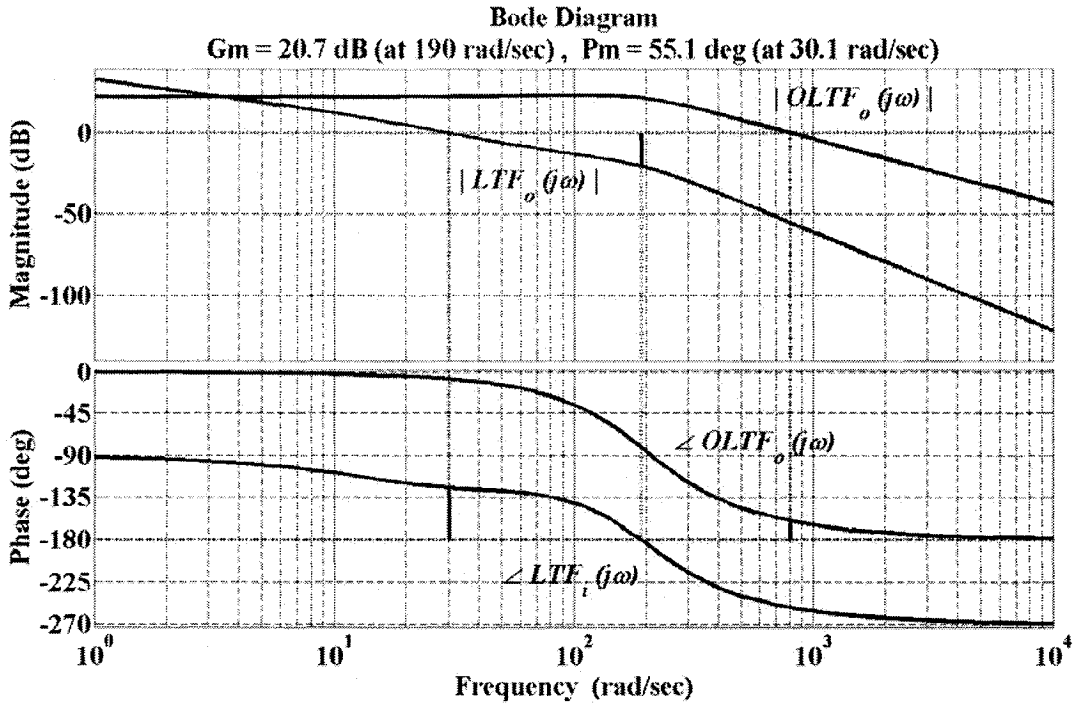


**Figure 5.5: Bode plots of $OLTF_o(s) = G_2(s).H_{f2}(s)/H_{f1}(s)$ & $LTF_o(s) = G_{c2}(s).G_2(s).H_{f2}(s)/H_{f1}(s)$.**

The designed outer loop PI controller parameters for the studied CLS system are as follows:

| | | |
|---|---|---|
| $k_{c2}$ | : | 1.3725 |
| $k$ | : | 0.7841 |
| $\tau_{c2}$ | : | 26.14 ms |
| $T_{p2}$ | : | 42.51 ms |
| Phase margin ($Pm_o$) | : | 55.1° |
| Band width ($BW_o$) | : | 30.1 rad/sec |

Figure 5.6 shows the stable step response of compensated closed-loop feedback transfer function $CLTF_o(s)$ of the outer ac voltage control loop. The response exhibits an approximate %overshoot of 15% and settling time of around 10 cycles.

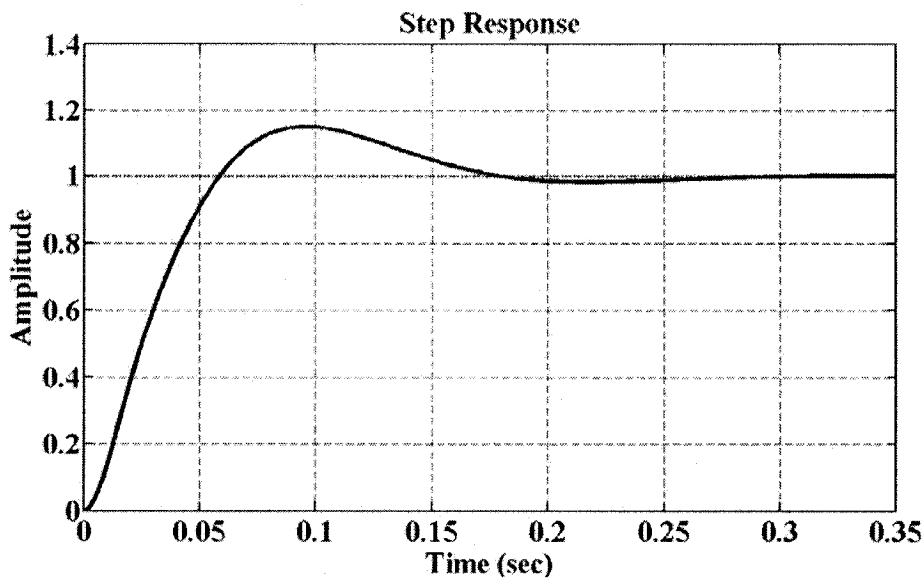


**Figure 5.6: Step response of the outer ac voltage control loop i.e.** $CLTF_o(s) = \{G_{c2}(s).G_2(s)\} / \{H_{f1}(s) + G_{c2}(s).G_2(s).H_{f2}(s)\}$.

## 5.5. SUMMARY

The following points can be summarised from this chapter.

- Approximate first-order OLTFs of the inner reactive current and outer ac voltage loops were developed and their corresponding controllers were designed to achieve a phase margin of 55°.
- The Bode plots and stable step responses were obtained for both the designed controllers.
- The step response of the overall CLTF exhibited the stable performance with %overshoot less than 15% and settling time within of about 10 cycles.

# CHAPTER-6

# SIMULATION RESULTS

## 6.1. INTRODUCTION

The CLS system and the controllers explained in the preceding chapters are simulated with EMTP-RV using a 10 μs time-step; a small time-step is needed for accurate simulation. The performance results are presented next.

## 6.2. STEADY-STATE PERFORMANCE

Figure 6.1 shows the steady-state waveforms of (a) the phase voltage at the PCC ($v_{pcc\_ab}$), (b) the CLS output phase voltage ($v_{o\_ab}$) (c) the CLS output phase current ($i_{o\_ab}$) (d) the CLS output line current ($i_{o\_a}$) and (e) dc voltages of three CLS links ($v_{dc1\_ab}$, $v_{dc2\_ab}$, $v_{dc3\_ab}$) per phase.

In steady state, the CLS maintains $|v_{pcc}|$ at 1.0 pu by supplying a rated reactive power (or line current) of 0.4 pu to the power system to compensate the voltage drop due to transmission line impedance ($Z_{tl}$). The voltage waveforms, $v_{pcc\_ab}$ & $v_{o\_ab}$ are almost sinusoidal in nature (Figure 6.1a & 6.1b respectively) and contain negligible amount of odd-order harmonics as shown in Figure 6.2a & 6.2b respectively (i.e. 5, 7, 11, 13, 17, 19.....$6n\pm1$; where '$n$' is a positive integer). Note that, the triplen harmonics are absent in both the voltages due to the delta-connection of the CLS.

The CLS output phase and line current waveforms ($i_{o\_ab}$ & $i_{o\_a}$) are symmetrical and follow the fundamental sinusoidal pattern (Figure 6.1c & 6.1d respectively). The phase current ($i_{o\_ab}$) leads $v_{pcc\_ab}$ & $v_{o\_ab}$ by approximately 90° and has a peak magnitude

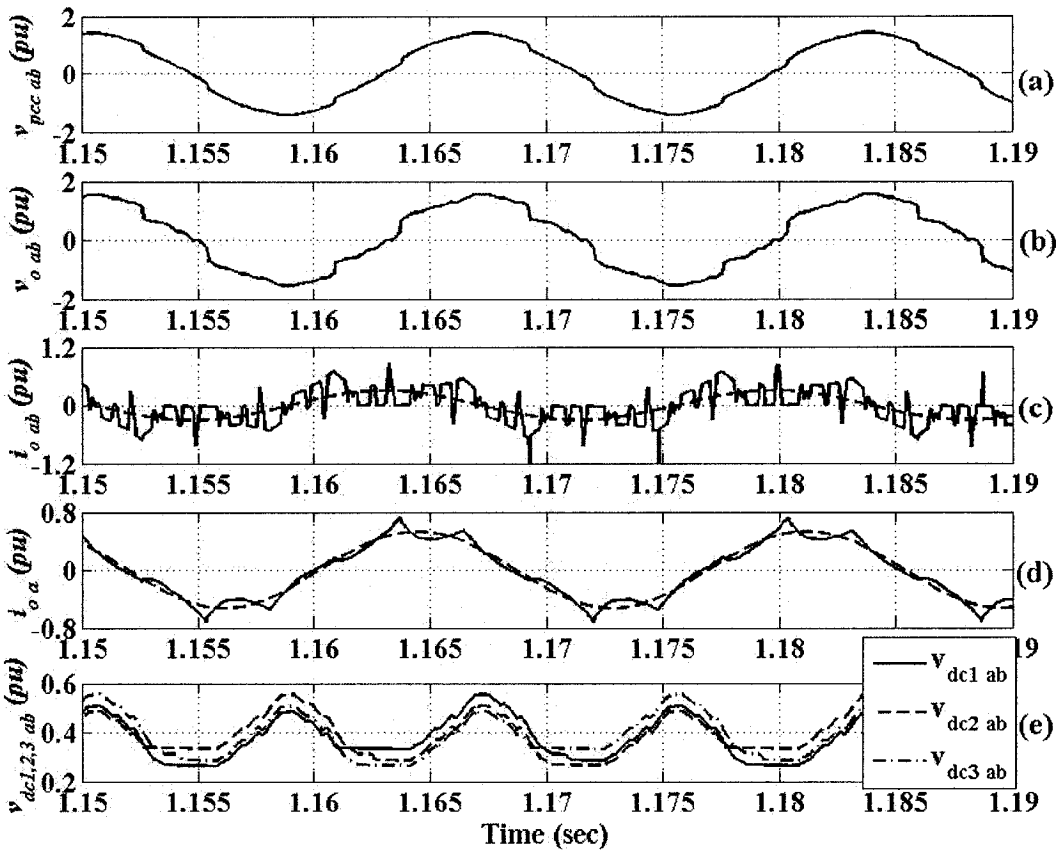


**Figure 6.1. Steady-state waveforms: (a) voltage at the PCC ($v_{pcc\ ab}$), (b) CLS output voltage ($v_{o\ ab}$) (c) CLS output phase current ($i_{o\ ab}$) (d) CLS output line current ($i_{o\ a}$) and (e) link dc voltages ($v_{dc1\ ab}$, $v_{dc2\ ab}$, $v_{dc3\ ab}$).**

of approximately 0.33 pu (i.e. 0.23 pu rms) to stabilize $|v_{pcc}|$ at 1.0 pu. The harmonic spectrum of $i_{o\_ab}$ shows dominant triplen harmonics (Figure 6.2c) whereas the same are absent in the line current ($i_{o\_a}$) (Figure 6.2d) due to the delta-connection of the CLS. Moreover, the line current is almost sinusoidal in nature and contains only a low magnitude of odd-ordered (except the triplen) harmonics.

It is important to note here that the simulation results presented here are without harmonic filters for the CLS system having only 3-links per phase. Therefore, by increasing the number of series connected links per phase in the CLS, the harmonics can be further reduced and the use of harmonic filters can be avoided. This can be useful as a reduction in the overall cost of the CLS system.

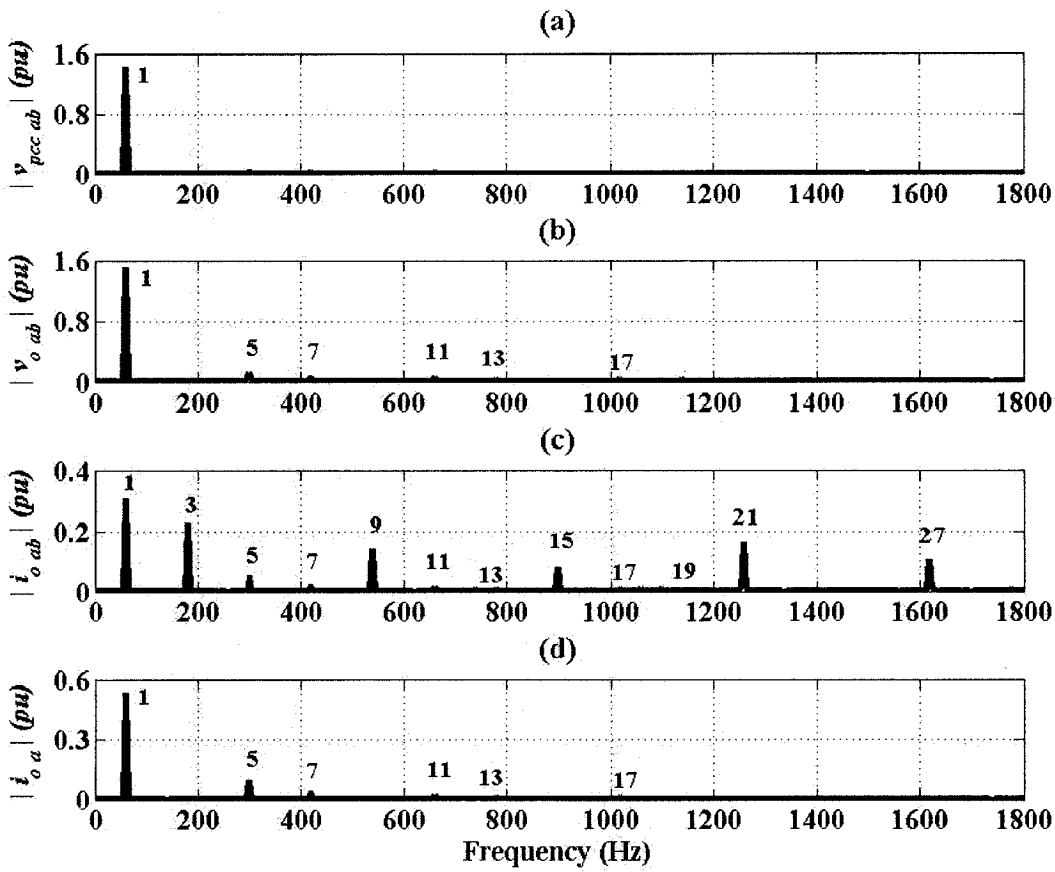


**Figure 6.2. Harmonic spectrums: (a) voltage at the PCC ($v_{pcc\ ab}$), (b) CLS output voltage ($v_{o\ ab}$) (c) CLS output phase current ($i_{o\ ab}$) and (d) CLS output line current ($i_{o\ a}$).**

The capacitor used for the voltage support on the dc side of each link has a finite value. Moreover, each link functions as a 1-phase full bridge VSC; therefore, the dc voltage contains ripple at a frequency of 120 Hz (Figure 6.1e). The dc voltage ripple depends on, the CLS VAr output, the number of links used per phase and the load. Figure 6.1e shows considerable amount of dc voltage ripple because the CLS is supplying the rated VAr output. Furthermore, as explained earlier, due to the employment of the RGSP, each $v_{dc}$ also contains a low frequency (~40 Hz) ripple superimposed on the second order (120 Hz) ripple. The low frequency ripple of $v_{dc}$ and hence, the harmonic content of the CLS output voltage and current can be minimized by increasing number of links per phase in the CLS.

## 6.3. TRANSIENT-STATE PERFORMANCE

The CLS is designed to compensate up to 0.4 pu of the transmission line reactive power at the PCC, in the capacitive mode. For the simulated CLS system in EMTP-RV, to reduce %overshoot and settling time as compared to those obtained by systematic calculations (Figures 5.4 & 5.6), the first-order PI controllers are used and their gains are obtained by trial-and-error. To investigate the dynamic performance of the CLS system with the controllers (Figures 3.1 & 5.1), the simulation tests are carried out as follows:

### 6.3.1. Initialization of the CLS-system.

Based on the start-up steps explained in Chapter-4 for the CLS system, a simulation is carried out using EMTP-RV and the results are presented in Figure 6.3. The

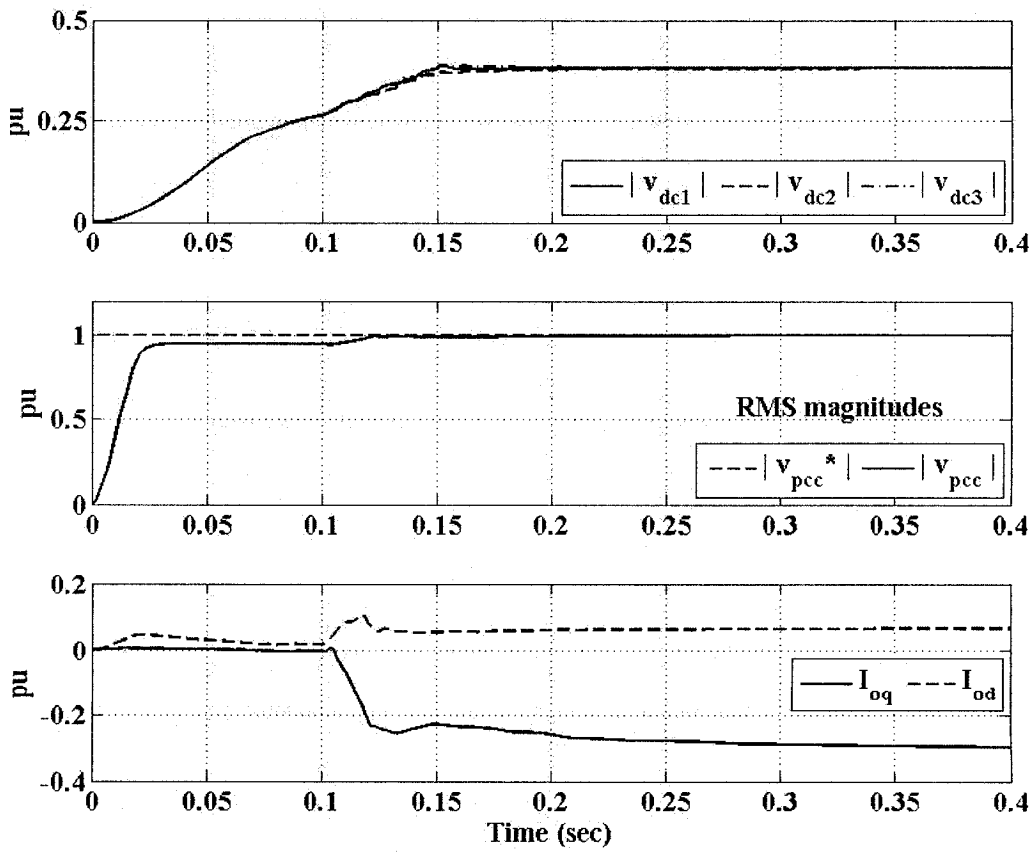


**Figure 6.3. Initialization of the CLS system: (a) DC voltage magnitudes of link-1, -2 & -3, (b) rms value of the voltage at the PCC, and (c) CLS output currents in *dq*-axis.**

CLS system is in rectifying mode from 0 to about 100 ms with $R_{start}$ into the CLS circuit i.e. CB1 & CB2 are closed & S1 is kept open (Figure 3.1) and the gate signals are suppressed. At about 100 ms, $R_{start}$ is bypassed by closing S1 (CB1 & CB2 remain closed) and the gating signals of the CLS switches are enabled.

It is clearly observed from Figure 6.3 that, during the interval from about 100 to 150 ms, the CLS absorbs more real power (or $I_{o\_d}$) than its total component losses. Therefore, its dc capacitor voltages (for all three link dc capacitors) keep on increasing until they reach a level such that $|v_o|$ is greater than $|v_{pcc}|$ and the CLS supplies reactive power (or $I_{o\_d}$) to the supply system. From about 150 to 250 ms, the dc voltages and hence the system voltages & currents undergo small transient oscillations to reach a steady state point. After about 250 ms, the dc capacitor voltage and, therefore, the CLS output voltage & current reach steady state and the CLS is put into regulation mode to maintain $|v_{pcc}| = |v_{pcc}^*|$. During the interval 250 to 400 ms, the real power absorbed by the CLS equals its total component losses. Consequently, the dc capacitor voltages maintain their level. It is important to note here that the dc voltages of the three link dc capacitors are balanced because of the employment of the Rotated Gate Signal Pattern (RGSP).

### 6.3.2. Step change in voltage reference

In the simulated responses of the step change in the voltage reference ($|v_{pcc}^*|$) (Figure 6.4), the R-L load at the receiving end is kept constant with $P_L$=1.0 pu & $Q_L \approx 0.3$ pu. Before the disturbance, the CLS controls $|v_{pcc}|$ at 1.0 pu by supplying the rated VAr ($Q_o$) of approximately 0.4 pu. The disturbance is introduced at time, t=1.2 s by applying a step change in $|v_{pcc}^*|$ from 1.0 to 0.975 pu. The dynamic response is stable and $|v_{pcc}|$ steps down from 1.0 to 0.975 pu with an approximate over shoot of 5% and a settling time of

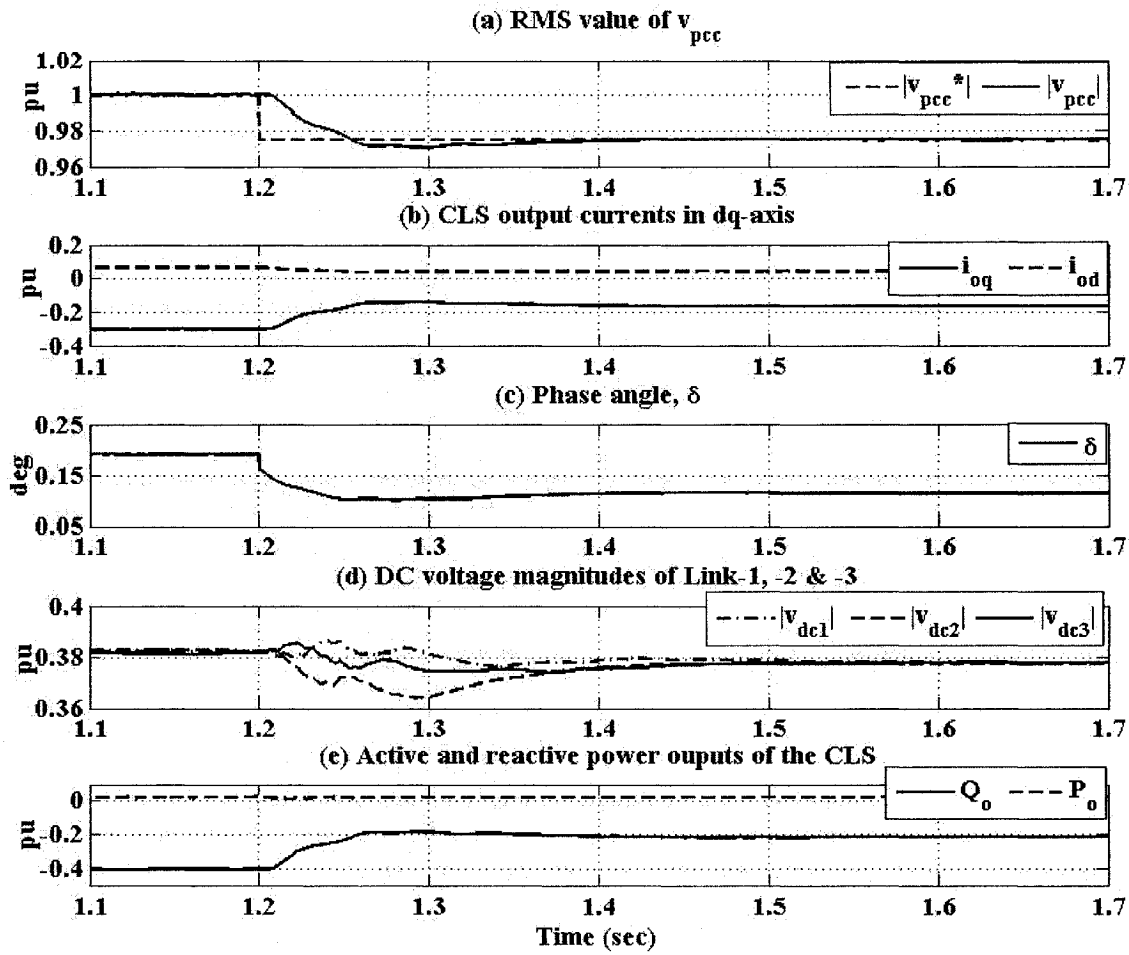


**Figure 6.4. Response to a step change in voltage reference ($k_{p1}$=−0.078, $k_{i1}$=−4.85, $k_{p2}$=14.6, $k_{i2}$=415).**

about five cycles (Figure 6.4a). In order to reduce $|v_{pcc}|$ from 1.0 to 0.975 pu, as a response to the step change in $|v_{pcc}^*|$, the CLS reactive output phase current ($i_{o\_q}$) (Figure 6.4b) the output VAr ($Q_o$) (Figure 6.4e) and the phase angle ($\delta$) (Figure 6.4c) decrease. Consequently, the link dc capacitor voltages of the CLS also decrease (Figure 6.4d).

### 6.3.3. Step change in the load

The simulated responses of the step change in the load are shown in Figure 6.5. In this test, $|v_{pcc}^*|$ is kept constant at 1.0 pu. Before the disturbance, the R-L load at the receiving end is having $P_L$=1.0 pu & $Q_L$≈0.3 pu and the CLS controls $|v_{pcc}|$ at 1.0 pu by supplying the rated $Q_o$ of approximately 0.4 pu. The disturbance is introduced at time, t=1.2 s by applying a -10% step change in the load (i.e. $P_L$ & $Q_L$ changes to 0.9 pu & 0.27

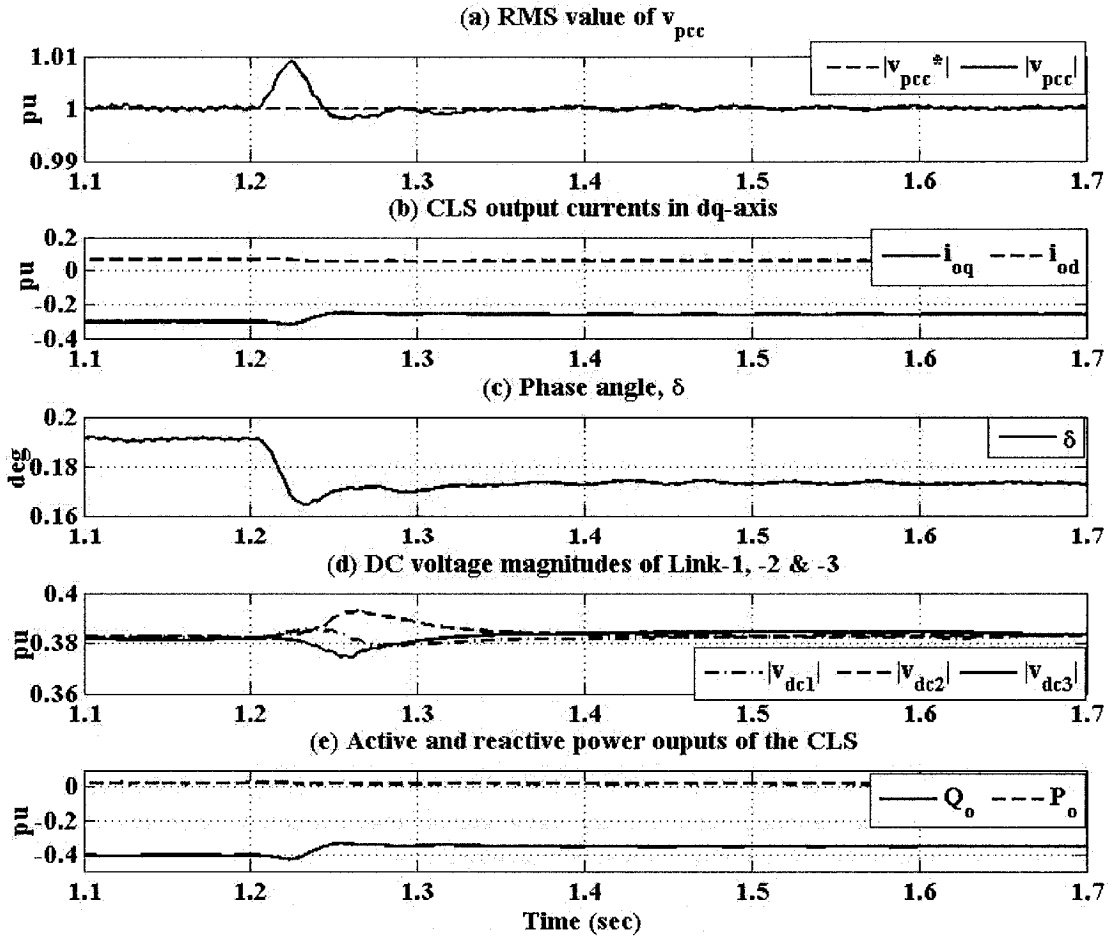


**Figure 6.5. Response to a step change in load. ($k_{p1}$=−0.078, $k_{i1}$=−4.85, $k_{p2}$=14.6, $k_{i2}$=415).**

pu respectively). The above step change causes only a short transient that is dampened quickly in about five cycles and the dynamic response is stable. Therefore, in steady state $|v_{pcc}|$ stays at 1.0 pu (Figure 6.5a). As a response to the above step change, $i_{o\_q}$ (Figure 6.5b), $Q_o$ (Figure 6.5e) and hence $\delta$ (Figure 6.5c) decrease in order to maintain $|v_{pcc}|$ at 1.0 pu. Consequently, the dc voltages of the link dc capacitors of the CLS also decrease (Figure 6.5d).

### 6.3.4. Balanced three-phase fault at bus B2

To investigate the dynamic performance of the CLS system in the worst case situation, a balanced 3-phase fault is applied at the bus B2 by closing the switch 'S2'

(Figure 3.1) for the time period of t=1.2 s to 1.4 s. The fault impedance ($Z_{fault}$) is chosen as 10% $Z_L$.

Before the occurrence of the fault, as $|v_{pcc}^*|$ is kept at 1.0 pu, the CLS stabilizes $|v_{pcc}|$ at 1.0 pu by supplying the rated $Q_o$ of approximately 0.4 pu. At t=1.2 s, following the occurrence of the fault, after an approximate delay of one cycle the circuit breaker (CB1) opens and disconnects the transformer & CLS from the rest of the circuit. Due to 3-ph fault, $|v_{pcc}|$ reduces from the set point 1.0 pu during this delay. As a result, $\delta$ increases to its maximum limit (set by the limiter) due to the positive error at the controller input. Consequently, the CLS draws more real power and increases the link dc voltages to compensate this error. The dc voltages continue to increase approximately for a period of another cycle (i.e. from the instant of opening of CB1) due to the transfer of stored energy from the transformer inductance to the link dc capacitors. After this delay, the CB2 opens and the dc voltages start falling due to the absence of any real power source. Moreover, the CLS current and power output reduce to zero (Figure 6.6b & 6.6e). The CLS controller blocks the gate signals and $|v_{pcc}^*|$ is reduced to its minimum set value (Figure 6.6a). Due to the 3-phase fault, $|v_{pcc}|$ also reduces to the value governed by the circuit law (Figure 6.6a). During the fault, both the circuit breakers remain open and the CLS has no control over the power system voltage. The phase angle ($\delta$) & link dc capacitor voltages exhibit large oscillations in the absence of the controller's action, however remains within the limit due to the presence of the limiters in the control circuit (Figure 6.6c & 6.6d).

At t=1.4 s the fault is cleared and both the circuit breakers are closed. After the closure of the circuit breakers, for initial 100 ms, the CLS start-up resistor ($R_{start}$) is

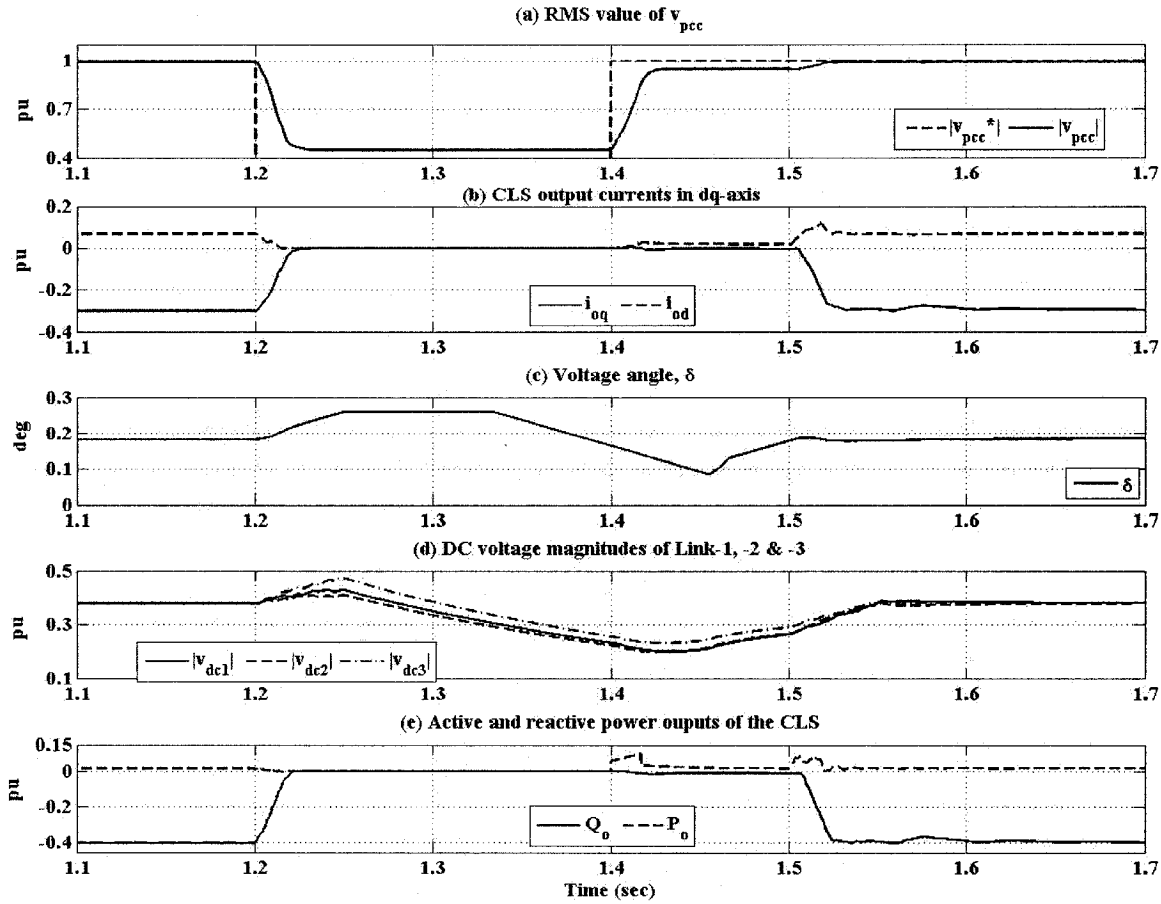


**Figure 6.6. Response to a balanced 3-phase fault at bus B2 ($k_{p1}$=−0.078, $k_{i1}$=−4.85, $k_{p2}$=2, $k_{i2}$=980).**

connected in series with the CLS by keeping the switch S1 open to limit the high inrush current into the link dc capacitors. During this time (i.e. from t=1.4 to 1.5 s) the CLS gate signals are still remained blocked and the CLS is operated in the rectification mode to charge the dc capacitors to the stable dc voltage level, limiting the charging current below the thermal rating of the switches.

At t=1.5 s, $R_{start}$ is bypassed by closing S1, the CLS gate signals are energized and the CLS is put into the regulation mode. Also, $|v_{pcc}^*|$ is again set to 1.0 pu and the CLS again starts supplying its rated $Q_o$ of approximately 0.4 pu to control $|v_{pcc}|$ at 1.0 pu (Figure 6.6).

The dynamic response of the CLS, following the fault is stable and after the closure of the circuit breakers, $|v_{pcc}|$ quickly stabilizes to 1.0 pu with negligible over shoot and settling time of about 1.5 cycles (Figure 6.6a). Due to the employment of the RGSP in the CLS, the dc voltages after each disturbance are balanced (Figure 6.4d, 6.5d & 6.6d).

# CHAPTER-7

# CONCLUSIONS

## 7.1 SUMMARY

A 3-phase CLS having 3-links per phase is presented. The SPWM technique to drive the switches of the CLS is used such that each switch turns on/off once per cycle of the fundamental frequency to reduce the converter losses by producing a 3-level output voltage waveform per link and to synthesize a multi-level CLS output voltage in a close approximation to a sinusoidal waveform. Approximate static and dynamic mathematical models and the analysis of the CLS system are presented using *dq*-transformations. The results show that the CLS system is stable and the parameters of the CLS system do not affect the system stability. The results also show that the magnitude of the reactive current (or power) is linearly proportional to the phase angle. Consequently, these models are used to design the control strategy whereby the phase angle of the modulating signal is used to control the CLS output voltage by adjusting the reactive current (or power) and hence to regulate the voltage at the PCC. Based on this control strategy two cascaded controllers are designed theoretically. Both the controllers exhibited the stable step response.

A simple yet effective start-up procedure for the CLS system is used to rapidly initialize the EMTP simulation model. A novel technique, called RGSP, is used to effectively balance the link dc capacitor voltages. With this technique, the gating patterns are rotated among the links per phase, in every half cycle of the fundamental frequency.

As a disadvantage, this technique introduces a low frequency ripple in the dc voltages. However, this low frequency ripple can be effectively minimized or eliminated by increasing the number of links per phase. To minimize the total ripple from the link dc capacitor voltage, resizing of the capacitor is required by careful selection of the operating region; however this requires the redesign of the controller gains.

The performance investigation of the CLS system is done by simulation using EMTP-RV under steady- and transient-state conditions. The steady-state analysis shows that by a small variation of the phase angle, a large reactive power (or current) flow can be controlled in the CLS. The steady-state results show that some harmonics from the output line current can be eliminated and a good quality CLS output voltage waveform can be produced by connecting the CLS in a 3-phase delta-configuration and by increasing the number of links per phase. Moreover, the transient tests exhibit a good dynamic performance of the CLS for the power system voltage regulation. The CLS system provides fast voltage support and the system voltage recovers within five cycles after a step change in the voltage reference or the load. Following a 3-phase symmetrical fault, the CLS system quickly recovers its steady-state operating point and regulates the power system voltage to 1.0 pu. The responses may be further improved by optimizing the controller gains.

## 7.2 CONTRIBUTION

As part of this thesis work, the following contributions have been made:

1. Developed the EMTP-RV model of a 3-phase 3-link 4 MVA, 15 kV delta connected CLS system using its basic building blocks for the power and gating circuits.

2. Proposed the SPWM switching technique, where two triangular carriers (one positive and the other negative) per link are compared with a single modulating signal per phase. This SPWM gating strategy is simpler to use and easier to analyse using the DFS method as compared to that of NGC's CLS application which requires additional computations of the transcendental equations to obtain the switching angles. Moreover, using the proposed SPWM gating strategy, each CLS switch is turned on/off only once per cycle of the line frequency to minimize the switching losses.
3. Proposed approximate static and dynamic models of the CLS system using *dq*-transformations. Furthermore, the stability of the CLS system was verified using the Routh-Hurwitz criterion.
4. Proposed a novel control technique, called the RGSP, to balance the dc capacitor voltages of the CLS. Also proposed a step-by-step start-up procedure for the CLS system to bring its reactive power output to a certain level in a short time, while maintaining all the switching devices within their ratings.
5. Proposed a closed-loop control strategy using two cascaded controllers (i.e. outer or ac voltage controller and inner or reactive current controller) by considering only the phase angle of the CLS output voltage vector as the control input (i.e. selecting a constant modulation index).
6. Validated the operation of the proposed EMTP-RV model of the CLS along with its controllers, to regulate the power system voltage at the PCC by reactive power compensation.

## 7.3 SUGGESTIONS FOR THE FUTURE WORK

1. Design the CLS controller using decoupled *dq*-transformations of the CLS output voltage and current and considering both, the phase angle and modulation index as control inputs. Implement the proposed controller to regulate the power system voltage and compare the results with those presented in this thesis using only a phase angle controller.
2. Study alternative control strategies in order to further improve the performance of the proposed CLS.
3. Design the controller of each individual 1-phase full bridge VSC link of the proposed CLS to independently control each phase and study its application for phase balancing of an unbalanced ac system.
4. Implement the proposed CLS model to study and investigate the power system application by connecting it in series with each phase of an ac system to provide a controllable positive or negative reactance to regulate the power flow.
5. Investigate the application of the proposed CLS model as an active filter to control the pre-existing harmonics of the ac system.

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# APPENDIX – A

## CLS SYSTEM PARAMETERS

- Base voltage : 400 kV (pri)/15.1 kV (sec)
- Base MVA : 10 MVA
- Operating point ($\delta_o$) : 0°
- Nominal rms power system phase voltage ($V_{pcco}$) : 231 kV (pri) / 15.1 kV (sec)
- Fundamental power system frequency ($f_o$) : 60 Hz
- CLS VAr output ($Q_o$) : ± 4 MVAR
- Thevenin equivalent system resistance ($R$) : 1.39 ohm
- Thevenin equivalent system inductance ($L$) : 0.0346 H
- Nominal dc voltage per link at $\delta_o$ ($V_{dco}$) : 7.55 kV
- DC capacitance per link ($C_{dc}$) : 100 μF
- Parallel resistance across $C_{dc}$ ($R_{dc}$) : 2.43 kohm
- Number of CLS links per phase ($N$) : 3
- Modulation index ($m_a$) : 1.0

# APPENDIX – B

# DESIGN CALCULATIONS OF CONTROLLERS

## A.1. Design of inner reactive current loop controller (Figure 5.2a)

### *a. OLTF and Bode Plot i.e. $G_I(s)H_{fI}(s)$*

The OLTF of the inner loop block is,

$$\frac{\Delta I_{oq}mean}{\Delta\delta} = G_I(s)H_{fI}(s) = \frac{-N\,m_a\,V_{dco}}{R\left(1+\frac{L}{R}s\right)}\left(\frac{1}{1+\tau_{f1}s}\right) \qquad \text{(A.1)}$$

It is important to note here that the negative sign of LTF can be compensated by selecting negative gains of the controller i.e. select $K_{pI}$ and $K_{iI}$ with a negative sign.

Substitute in (A.1), $N$ = 3, $m_a$ = 1, $R$ = 1.39 ohm, $L$ = (13.05/377) = 0.0346 H, $\omega_o = 377$ rad/sec, $X$ = 13.05 ohm, $\tau_{fI} = \frac{1}{300}$ sec and from steady state plot of $V_{dc}$, $V_s$ and $\delta$ at $\delta o = 0°$ as shown in Figure 3.8, $V_{dco}$ = 0.334pu.

Let the crossover frequency = $f_{xI}$ = 20% $f_{sw}$ = 0.2 $f_{sw}$

Where $f_{sw} = f_c$ = 120 Hz i.e. the ripple frequency of $V_{dc}$.

As $f_{xI}$ = 24 Hz $\qquad \omega_{x1} = 2\pi\, f_{xI}$

$$\omega_{x1} \approx 151 \text{ rad/sec}$$

From Bode Plot of $G_I(s)H_{fI}(s)$ (Figure 5.3), at $\omega_{x1}$ = 151 rad/sec.

$$\left|G_I(j\omega_{x1})H_{fI}(j\omega_{x1})\right|\text{dB} = 20\log\left|G_I(j\omega_{x1})H_{fI}(j\omega_{x1})\right| = 71.4\ dB.$$

$$\angle\left[G_I(j\omega_{x1})H_{fI}(j\omega_{x1})\right] = 78.2°$$

Let the desired phase margin, Pm = 55°.

***b. Phase and gain of Type-1 PI controller for inner loop.***

$$G_{c1}(s) = \frac{k_{p1}(1 + s\tau_{c1})}{s\tau_{c1}} \qquad \left(G_{c1}(s) = k_{p1} + \frac{k_{i1}}{s}\right) \text{and } \tau_{c1} = \frac{k_{p1}}{k_{i1}} \tag{A.2}$$

$$|G_{c1}(j\omega)| = \frac{k_{p1}}{\omega\tau_{c1}}\sqrt{(\omega\tau_{c1})^2 + 1} \tag{A.3}$$

$$\angle[G_{c1}(j\omega)] = \tan^{-1}(-1/\omega\tau_{c1}) \tag{A.4}$$

Phase of the controller: At $\omega_{x1}$ is given by:

$$\angle G_{c1}(j\omega_{x1}) + \angle G_1(j\omega_{x1})H_{f1}(j\omega_{x1}) = \text{PM} - 180° \tag{A.5}$$

$$\angle G_{c1}(j\omega_{x1}) = 55° - 180° - 78.2°$$

$\angle G_{c1}(j\omega_{x1}) = -203.2°$ (i.e. phase lag of $-23.2°$ is req)

Now for type-1 PI controller rewriting (A.4) at $\omega_{x1}$,

$$\angle G_{c1}(j\omega_{x1}) = \tan^{-1}(-1/\omega_{x1}\tau_{c1})$$

Substitute $\omega_{x1}$ = 151 rad/sec in (A.6) which gives:

$\tau_{c1}$ = 0.01545 sec.

As the gain of the compensated LTF is 1 (or 0 dB),

$$\text{Compensated LTF}(j\omega_{x1}) = G_{c1}(j\omega_{x1})G_1(j\omega_{x1})H_{f1}(j\omega_{x1}) = 1 \tag{A.7}$$

i.e. $20\log|G_{c1}(j\omega_{x1})| + 20\log|G_1(j\omega_{x1})H_{f1}(j\omega_{x1})| = 0$ dB

$$20\log|G_{c1}(j\omega_{x1})| = -20\log|G_1(j\omega_{x1})H_{f1}(j\omega_{x1})|$$

Therefore,

Gain of the controller in dB at $\omega_{x1}$ = – {gain of OLTF $G_1(j\omega_{x1})H_{f1}(j\omega_{x1})$ in dB at $\omega_{x1}$}

(A.8)

i.e. $20\log|G_{c1}(j\omega_{x1})| = -71.4$

Therefore, $|G_{c1}(j\omega_{x1})| = 10^{(-71.4/20)} = 2.7 \times 10^{-4}$

Rewriting (A.3) at $\omega_{x1}$ for type-1 PI Controller,

$$|G_{c1}(j\omega_{x1})| = \frac{k_{p1}}{\omega_{x1}\tau_{c1}}\sqrt{(\omega_{x1}\tau_{c1})^2 + 1}$$

i.e. $$k_{p1} = \frac{4.03 \times 10^{-4} \times (151 \times 0.01545)}{\sqrt{(151x0.01545)^2 + 1}}$$

i.e. $k_{p1} = 2.5 \times 10^{-4}$.

Now,

$\tau_{c1} = \frac{k_{p1}}{k_{i1}}$ i.e. $0.01545 = 2.5 \times 10^{-4} / k_{i1}$ .

i.e $k_{i1} = 0.0162$ .

Selecting the negative gain values to compensate the negative sign of the plant gain $G_1(s)$.

i.e. $k_{p1} = -2.5 \times 10^{-4}$ , $k_{i1} = -0.0162$ for type-1 PI controller.

$$G_{c1}(s) = \frac{-2.5 \times 10^{-4}(1 + 0.01545s)}{0.01545s} \qquad (A.9)$$

## A.2. Design of outer ac voltage loop controller (Figure 5.2b)

### *a. Open loop LTF and Bode Plot ( i.e. $G_2(s)H_{f2}(s)$ )*

The OLTF of the outer loop block is,

$$\frac{\Delta V_{pcc}mean}{\Delta I_{oq}*} = (1 + s\tau_{f1}) \times \frac{1}{(1 + s\tau_{f2})}$$

$$G_2(s)H_{f2}(s) = \frac{X(1 + s\tau_{f1})}{(1 + s\tau_{f2})} \qquad (A.10)$$

Substitute, $X = 13.05\ \Omega$, $\tau_{f1} = \tau_{f2} = 1/300$

Now, Let $\omega_{x2} = \omega_{x1}/5 = 151/5 = 30.2\text{r/s} \approx 30$ rad/sec.

i.e. $\omega_{x2} \approx 30$ rad/sec.

From Bode Plot of $G_2(j\omega)H_2(j\omega)$ as shown in Figure 5.5, at $\omega_{x2} \approx 30.0$ rad/sec.

$$\left|G_2(j\omega_{x2})H_{f2}(j\omega_{x2})\right|\text{dB} = 20\log\left|G_2(j\omega_{x2})H_{f2}(j\omega_{x2})\right| = 22.6\text{ dB}.$$

i.e. $\angle[G_2(j\omega_{x2})H_2(j\omega_{x2})] = -7.4°$

Let the desired phase margin, PM = 55°.

### *c. Phase and gain of Type-1 PI controller for the outer loop.*

$$\angle G_{c2}(j\omega_{x2}) + \angle G_2(j\omega_{x2})H_2(j\omega_{x2}) = \text{PM} - 180° \qquad \text{(A.11)}$$

$$\angle G_{c2}(j\omega_{x2}) = 55 - 180° + 7.4°$$

$\angle G_{c2}(j\omega_{x2}) = -117.6°$ i.e lag compensation of 117.6°

As the angle requirement for the controller is greater than 90°, therefore use PI type- III controller,

$$\text{Boost} = \angle G_{c2}(j\omega_{x2}) + 90° = -117.6° + 90° = -27.6° \qquad \text{(A.12)}$$

$$k = \tan(\text{Boost}/4 + 45°) = \tan(38.1°) = 0.7841 \qquad \text{(A.13)}$$

$$\text{At } \omega_{x2} = 30\text{ rad/sec} \begin{cases} \omega_p = k\omega_x^{\,2} = 0.7841(30)^2 = 23.523\text{ rad/sec} \\ \omega_z = \dfrac{\omega_p}{k^2} = 38.26\text{ rad/sec} \end{cases} \qquad \text{(A.14)}$$

or, $\tau_{c2} = \dfrac{k}{\omega_{x2}} = 26.14\text{ ms}$, $T_{p2} = \dfrac{1}{k\omega_{x2}} = 42.51\text{ ms}$

Therefore, $G_{c2}(s) = \dfrac{k_{c2}(s+38.83)^2}{s(s+23.17)^2}$

$$G_{c2}(s) = \frac{k_{c2}\left(s^2 + 77.67s + 1508.16\right)^2}{\left(s^3 + 46.35s^2 + 537.08s\right)} \tag{A.15}$$

i.e. $k_{c2}\underset{(\mathrm{dB})}{} \approx \left| G_{c2}(j\omega_{x2}) \right|_{dB} = -\left|G_2(j\omega_{x2})H_2(j\omega_{x2})\right|_{\mathrm{dB}} = 2.75\mathrm{dB}$

$$k_{c2} = 10^{(-2.75/20)} = 1.3725 \tag{A.16}$$

Therefore, $G_{c2}(s) = \frac{1.3725(s+38.83)^2}{s(s+23.17)^2}$ or $G_{c2}(s) = \frac{1.3725(1+0.02614s)^2}{0.02614s(1+0.04251s)^2}$ (A.17)

# APPENDIX – C

# LIST OF PUBLICATIONS

**a. Conference papers**

1. N.M. Shah, V.K. Sood and V. Ramachandran, "Modeling of a chain link STATCOM in EMTP-RV," IEEE CCECE Conference, Ottawa, May 2006, pages 1252-1257.
2. N.M. Shah, V.K. Sood and V. Ramachandran, "Modeling, Control and Simulation of a Chain Link STATCOM in EMTP-RV," International Conference on Power Systems Transients (IPST'07) in Lyon, France on June 4-7, 2007, 8 pages.

**b. Journal paper**

1. N.M. Shah, V.K. Sood and V. Ramachandran, "EMTP simulation of a chain link STATCOM," IEEE Transactions on Power Delivery, Revised manuscript submitted in July 2007.