MODELING A HYBRID DIODE- THYRISTOR HVDC RECTIFIER IN EMTP-RV

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Abstract

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High Voltage Direct Current (HVDC) transmission systems are used all over the world in frequency-conversion schemes, non-synchronous AC interconnections, submarine DC-links and in many other projects where they enhance AC system stability. HVDC system has many advantages such as fast power flow control, stable and economical operation for long-distance transmission. But the large-scale usage of HVDC transmission is limited by several factors and one of the most important factors is the high cost of conversion equipment. A proposed converter model for the HVDC rectifier system is presented for a possible reduction of the high cost of conversion equipment. This thesis presents an investigation into the viability of a hybrid diode-thyristor HVDC rectifier.

In a standard HVDC system, a 12-pulse thyristor-bridge is used. In this thesis, the CIGRE benchmark based HVDC system operating with a weak AC system is presented as the standard model. In the proposed hybrid circuit, the lower 6-pulse thyristor-bridge (which is connected with a Y-Y transformer), is replaced by a cheaper diode-bridge. This reduces the overall capital cost of the 12-pulse rectifier, but has implications regarding

the operational behaviour of the HVDC terminal and system. The operational behaviour of this hybrid diode-thyristor rectifier under static and dynamic conditions and the comparison with the standard model are verified with the well-known simulation package called EMTP-RV.

Due to unbalanced harmonic cancellation between diode-bridge and thyristor-bridge, the proposed HVDC system generates more characteristic harmonics than the standard model on both AC and DC side. So, an extra filtering unit is needed which will increase the cost of the proposed HVDC model.

In the proposed model, only one controller block is needed for the thyristor-bridge as the diode-bridge does not need the controller block. So the cost will be reduced in the proposed model due to the requirement of a single controller block. The controller for optimizing the PI parameters of the proposed HVDC model is designed by using ITAE (Integral of Time multiplied by the Absolute value of the Error) criterion, which is one of the synthetic indexes for evaluating the control system's performance. DC fault is the most severe fault for the converter valves at the rectifier end and it represents one serious operational difficulty with the introduction of the proposed model. It is very difficult to recover from a DC fault like the standard model because of the uncontrolled diode-bridge. So an AC breaker (which is costly equipment) is added to the system to recover from the fault.

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List of Abbreviations

AC	- Alternating Current
DC	- Direct Current
HVDC	- High Voltage Direct Current
SCR	- Short Circuit Ratio
PSCAD	- Power System Computer Aided Design
EMTDC	- Electromagnetic Transient Direct Current
IGBT	- Insulated Gate Bi-polar Transistor
VSC	- Voltage Source Converter
CSC	- Current Source Converter
CIGRE	- The Conseil International des Grands Reseaux Electriques
EMTP	- Electro-magnetic Transients Program
VCO	- Voltage Controlled Oscillator
ITAE	- Integral of Time multiplied by the Absolute value of the Error
VDCL	- Voltage Dependent Current Limiter
CEA	- Constant Extinction Angle
GTO	- Gate Turn Off
PSpice	- Simulation Program with Integrated Circuit Emphasis
IREQ	- Institut de Recherche d'Hydro-Québec
LCC	- Line-Commutated Converter
SCC	- Self-Commutated Converter

Chapter 1

INTRODUCTION

High Voltage Direct Current (HVDC) power transmission is now a mature technology since its first installation at Gotland in 1954. The main problems of the HVDC transmission system are still the high cost of the conversion equipment, inability to use the converter transformers to alter voltage levels rapidly and in a significant way, generation of harmonics, the requirement of the reactive power and the complexity of controls. To overcome these disadvantages, several attempts have been made (e.g. [5], [6], [7], [20], [21], and [22]) to consider new alternatives to reduce the costs of the HVDC transmission. This thesis makes an investigation into the viability of a hybrid diode-thyristor HVDC rectifier model for a possible reduction of costs of the terminal equipment of the HVDC transmission system. Comparison and assessment of the design and the performance of the hybrid model versus the standard model, under both static and dynamic conditions, are made. The evaluation of the two systems is made with the simulation package EMTP-RV.

1.1 Literature Review:

In this section, a number of classical papers on HVDC systems and their controllers are reviewed to provide some background information on the topic of interest.

1.1.1 A Benchmark Model for HVDC system studies [1]:

This paper was the first attempt to create a common reference for conducting HVDC system studies. The CIGRE Working Group established this Benchmark DC system for the purposes of comparing various DC control strategies, recovery performances and different simulation methods and results. The AC system, Reactive Compensation, DC line, Converter stations, DC control system, and Simulation results using a number of simulator/digital computer models of the Benchmark system were briefly presented in this paper. In this thesis, this model system will be used as a basis for comparison with the proposed hybrid system.

The next paper deals with two simulation tools for representing this CIGRE HVDC Benchmark system.

1.1.2 Detailed Modeling of CIGRE HVDC Benchmark System Using PSCAD/EMTDC and PSB/SIMULINK [2]:

In this paper, the authors presented a detailed comparison between the two simulation tools PSCAD/EMTDC and PSB/SIMULINK for the modeling and simulation of the first CIGRE HVDC Benchmark system. They covered the topic in three steps. First, they introduced a brief discussion about the two simulation tools and their solution techniques. Second, they described why they used CIGRE Benchmark HVDC System. Then, they presented the detailed model of an HVDC system and its controllers in PSCAD/EMTDC,

and PSB/SIMULINK simulation environments. They compared both steady state and transient results (i.e. DC fault and AC faults) for both the simulation environments. After performing all the simulations, they concluded that the two tools produced almost identical and consistent results during steady state and transient state situations. In terms of computational speed and memory usage, PSCAD/EMTDC was considered to be the more efficient environment.

This paper is very useful for this thesis. For simulating the proposed model and standard model, EMTP-RV (which is generically similar to PSCAD/EMTDC) will be used as the simulation tool in this thesis. The next paper presents simulations, with the older version of EMTP, of the transient performance of an HVDC system operating with a weak AC system.

1.1.3 EMTP Simulation of an HVDC system operating with weak AC systems [3]:

In [3], the authors discussed how to model the controls and the power system elements of an HVDC system and how to assess its transient performance using the simulation program EMTP. They gave a brief introduction about the CIGRE Benchmark based HVDC system operating with a weak AC system. They performed optimization tests for the snubber circuit for selecting the range of R and C. They presented the converter switch model, with its snubber circuit, and two gate-firing units with their performance comparison and the rectifier current controller. To study the dynamic behavior of the system they performed 11 typical system tests (e.g. step change in the current controller,

AC, and DC fault conditions etc) on the HVDC system. As a whole, they presented detailed information about the modeling of an HVDC system, which would prove to be very helpful for studying HVDC systems.

In this thesis, a similar technique will be employed to do the comparison with the proposed hybrid model. This is an introductory paper for this thesis. Next, an example of an HVDC system model and its controls are presented.

1.1.4 Modeling of the Hydro-Quebec-New England HVDC System and Digital Controls with EMTP [4]:

In this paper, the authors gave a detailed description about the modeling of digital controls and presented some comparisons with results from a real-time physical HVDC simulator. Mainly, they validated the EMTP results against identical tests on the dedicated real-time simulator of IREQ with the following tests:

- Three phase fault at Radisson 315 kV bus (rectifier side)
- Single phase fault at Sandy Pond 345 kV bus (inverter side)
- Monopolar DC line-to-ground fault at Sandy Pond (inverter side)

They completed the principal features of the control system and all basic protection functions but they did not focus on modeling the pole, bipole, and master controls for multiterminal operation of the DC system.

The significance of this paper is that it reported, for the first time, that a commercial HVDC digital control system had been modeled in a digital simulation package such as EMTP. To achieve this, the authors had to modify the software to incorporate digital and analog controllers. The next two papers present two different converter models for the HVDC system.

1.1.5 Simulation Study of a Hybrid HVDC System Composed of a Self-Commutated Converter and a Line-Commutated Converter [5]:

The disadvantages of the conventional line-commutated converters (LCCs) are:

- It is sensitive to AC system conditions,
- To obtain stable inverter operation is difficult especially with a weak AC system under AC system fault conditions.

The development of large-capacity Gate Turn-Off thyristor has led to a self-commutated converter (SCC). The SCC has the following advantages:

- It can control active and reactive power independently and quickly, regardless of the AC system conditions.

The authors of this paper presented a new hybrid HVDC system composed of a conventional line-commutated converter (LCC) and a self-commutated converter (SCC)

to overcome some of the disadvantages of the LCC. In their proposed system, the LCC of the current source converter controls DC current as a rectifier and the SCC of the voltage source converter controls DC voltage as an inverter. The ACR (automatic current regulator) controls DC current at a set reference value for the LCC. The AVR (automatic DC voltage regulator) and AγR (automatic margin angle regulator) are used for back-up control. For SCC the AVR and AQR (automatic reactive power regulator) control DC voltages and reactive powers at set reference values independently. A new control scheme, start-stop operation, behavior under AC faults conditions of the hybrid HVDC system and comparisons of this hybrid HVDC system with the system comprised of LCCs or SCCs were also discussed by the authors. After the above-mentioned tests they concluded that the hybrid HVDC system can operate stably without needing fast communications between the LCC and SCC converter stations. In their recommended control scheme the LCC keeps the DC current constant and the SCC keeps the DC voltage and AC voltage constant. Over currents due to AC system faults on the inverter side are mitigated by reactive power control of the SCC.

The next paper also presents an alternative HVDC converter system.

1.1.6 A Comparison of Alternative HVDC Converter Scheme [6]:

The author compared two different HVDC converter schemes with a conventional design. The first scheme had bridges modified by the addition of auxiliary (by-pass) valves and the second scheme used series bridges of unequal rating. He described the advantages of these two non-conventional schemes, as being:

- A significant reduction of the reactive power absorption,
- The transformer tap-changer is no longer required; and
- A reduction in the harmonic content of the AC supply

Nevertheless, these schemes also included the expense of additional solid-state devices and their control circuitry. After the case study of these non-conventional schemes, he concluded that although the transformer tap-changer is eliminated, the number of devices required is considerably increased and additionally the extra auxiliary equipment required relatively large capacitors for the GTO thyristor snubber circuits. It also incurred extra losses in the damping circuits of the GTO thyristor snubber circuitry.

In this thesis, since an alternative converter scheme is also proposed, these papers were very relevant for this work. Both the papers present an alternative converter scheme using GTO thyristors. In this thesis, a diode-bridge will be used as the alternative converter scheme to reduce the cost of the overall transmission system. After modeling an HVDC converter system, the next step is the controller design. The control system plays an important role in the HVDC system. The next paper presents one technique for tuning the PI controller.

1.1.7 A Fuzzy Self–Tuning PI Controller for HVDC Links [7]:

In this paper, the authors presented a fuzzy logic-based tuning of the controller parameters for the rectifier-side current regulator and inverter-side gamma controller in a

HVDC system. They simulated a two-pole, point-to-point HVDC system with the help of the program EMTDC. The fuzzy self-tuning controller was introduced by replacing both the rectifier-side current regulator and inverter-side gamma controller and the controller gains K_p, K_i were adjusted through fuzzy inference. They simulated the following cases for tuning the rectifier-side pole controller, and also for comparing the performance of the fuzzy tuner while operating at the rectifier-side or at both the inverter and rectifier sides:

- Single Line-to-Ground Fault at Inverter,
- DC Line-to-Line Fault at the Inverter,
- Single Line-to-Ground fault at Rectifier,
- DC Line-to-Line Fault at Rectifier,
- Step Change in Current Order, and
- Tuning both the Inverter and Rectifier-side controllers

From the above results, they concluded that the rectifier-side AC system could recover rapidly after any disturbance. For the faults in the inverter side, their proposed controller allowed the system to recover much faster than with the conventional PI controller. However, for small disturbances, the proposed controller might not be much better than the conventional one. Finally, they concluded that the fuzzy controller tuning is less complicated than the PI optimization algorithm.

Fuzzy logic control theory with accurate mathematical description is very effective but it requires experienced human experts for the derivation of fuzzy rules. In the thesis, a

systematic optimization method, and an approach based on Bode plots are used for tuning the PI controller. Fuzzy logic method can be an alternative way to design the controller. The next paper presents the stability area of the tuned PI controller.

1.1.8 Stability Analysis of Thyristor Current Controllers [8]:

In this paper, the authors investigated the operational stability areas of proportional-integral (PI) controllers of thyristor converters with both analogue and digital controllers. Laplace and *z*-transforms were used for investigating the system stability. The stability boundary was determined using the Routh-Hurwitz criterion for the analogue system and Jury's stability criterion was used for the digitally controlled systems. In the analogue control, the transfer function of every element was described in the *s*-domain and analysis was done by using the Laplace transform. After the assessment, they concluded that the system was generally stable if the integral gain K_i is less than 1 and the system would become unstable for small values of the proportional gain K_p if K_i is large enough. For proportional increases of K_p and (K_i-1), the system would remain stable. In discrete sampled analogue PI controls, the converter was represented as a sample-and-hold element with a sampling switch. After the assessment, they concluded that increase of either proportional or integral gain would cause the system to become unstable, with K_p affecting the system stability more seriously than K_i. In the digital control system, the PI controller was implemented with a microprocessor-based controller, with the control input derived from a sample-and-hold element. The result showed that the system became unstable at constant K_i for an increase of K_p and the system did not remain stable if both

K_p and K_i were increased simultaneously. They confirmed that the stability area for the digitally controlled discrete system is smaller than that of the analogue system and a steady system working with an analogue regulator process may become unstable if implemented with digital control, especially for large proportional gain. This paper presents stability analysis for both analogue and digital controllers of the HVDC system, and proves to be very helpful for the design of the control system.

1.2 Proposed Approach

HVDC terminals usually consist of two 6-pulse converter bridges connected in series to form a 12-pulse converter unit. Series connection of the two 6-pulse bridges (one with Y-Y and the other with Y-Δ converter transformer connections) has been preferred because of (a) the cancellation of cumbersome low-order characteristic harmonics (i.e. 5^{th} and 7^{th}), (b) higher voltage rating, and (c) protection and reliability requirements of the converter. These converter bridges are the most costly parts in the terminal. A typical cost break down for an HVDC transmission system is shown in Figure 1.1.

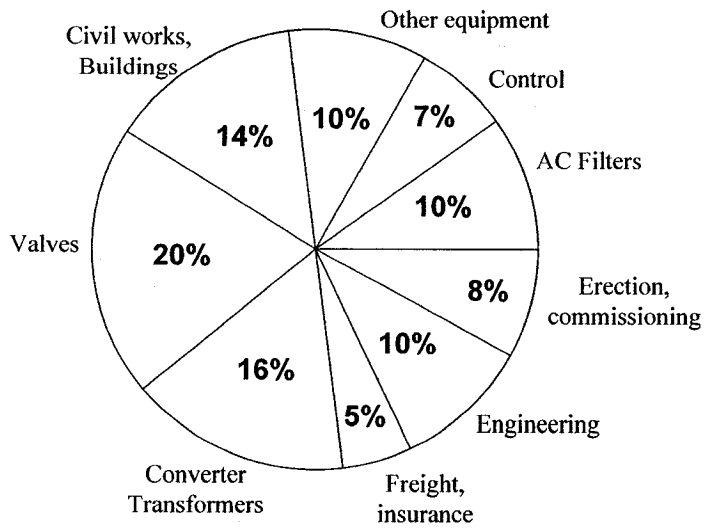

Figure 1.1: A typical cost break down for an HVDC transmission system [15]

It is visible from the cost break down that 60% of the system cost is incurred by the terminal equipment i.e. valves, converter transformer, control unit, filters etc. The cost of the valves is 20%, and this represents the highest percentage of all the equipments of the HVDC system. If it is possible to reduce this valve cost, then it will make an important contribution in reducing the overall system cost. The second most costly part of the system is the converter transformer (16%). If one of the two transformers could be replaced with its equivalent impedance, then the overall system cost would be reduced in a significant manner.

In order to reduce the cost of the transmission system, it is proposed to replace one of the 6-pulse thyristor-bridge with a much-cheaper diode-bridge at the rectifier end. In a standard HVDC system, two 6-pulse thyristor-bridges are connected in series. It is proposed that one of these 6-pulse thyristor-bridges can be replaced with a 6-pulse diode-bridge for a possible reduction of the valve costs in a rectifier station only. The diode-

bridge is attractive since a diode switch is a cheaper alternative than a thyristor switch. Furthermore, the voltage rating of a diode is much higher than that of a thyristor resulting in a fewer number of switches required to build a valve unit; this translates into lower costs and lower losses. Finally, for a diode-bridge no control unit is needed. The rest of the HVDC terminal is composed of the AC side of the system, AC and DC filters, DC side of the system, and a control and gate firing trigger unit for the thyristor-bridge. Therefore, for the proposed model, capital costs will be reduced and an improved reliability would be achieved due to a simpler converter and lower component count. One of the implications of this change will be that the other 6-pulse thyristor-bridge would need to be adjusted to get the correct firing angle of the system for purposes of maintaining the same transmission voltage. Next the implications of a comparison of a diode-bridge and a thyristor-bridge (Figure 1.2(a), and 1.2(b)) are presented.

Thyristor-Bridge (Cell in valve)	Diode-Bridge (Cell in valve)
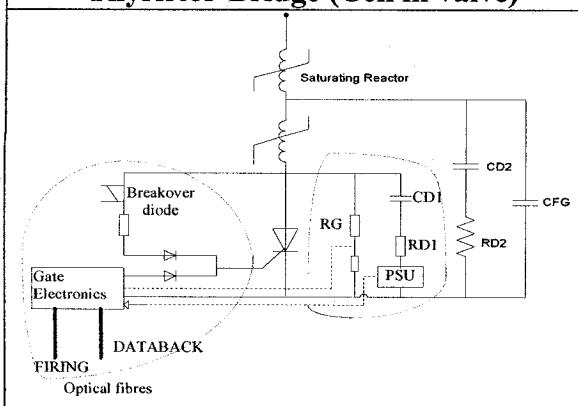	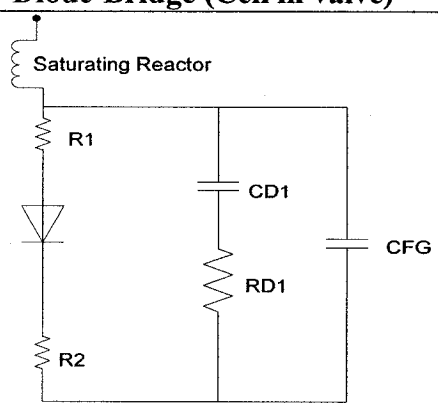
Figure 1.2(a): Electrical circuit in the Thyristor level	Figure 1.2(b): Electrical circuit in the diode level

- Assuming, that the cost of a thyristor is 1.5 times the cost of a diode and price of each diode is 1 unit. The maximum voltage rating of one high power thyristor and diode is 9 kV and 11 kV respectively. If a 230 kV system is used, then the number of thyristors needed to construct a valve is 28 ($\frac{230}{9}$ = 26+2 (for redundancy)); similarly, the number of diodes needed is 23 ($\frac{230}{11}$ = 21+2 (for redundancy)). So, for a 230 kV system, cost will be reduced by 19% (i.e. 28*1.5-23*1) if a diode switch is used to construct the high voltage valve.

- **Other ancillary equipment:** From the cost breakdown (Figure 1.1), it is found that 10% of the costs of the HVDC system come from other equipment. There are potential savings from these other equipment. For instance, in a thyristor-bridge, two saturating reactors are needed for di/dt protection. Only one saturating reactor is needed in a corresponding diode-bridge (Figure 1.2(b)). Moreover, the circled components in the right side of Figure 1.2(a) are no longer needed for a diode-bridge. Therefore, from these other equipments costs, it is estimated that at least 4% of the costs can be reduced by using a diode-bridge.

- **Control Costs:** In Figure 1.2(a), the circled components on the left side of the figure is a firing pulse generator unit to fire a star-connected or delta-connected thyristor-bridge; In the case of a diode-bridge, this firing pulse unit would not be needed (Figure 1.2(b)). The control portion of the total cost is 7%. Therefore, in case of a diode-bridge, 3.5 % of this control cost would be reduced.

- **Power loss:** Assume that a conduction voltage drop for each thyristor and diode is 1.7 V & 1.2 V respectively. Therefore, the conduction power loss for each thyristor is 2.4 kW (1.7*1405.06 where 1405 A is the full load thyristor or diode current) and for each diode is 1.7 kW (1.2*1405). Therefore, the power loss is reduced by $=\frac{2.4-1.7}{2.4}*100\% = 29.2\%$ in case a diode switch is used instead of a thyristor switch for the construction of the valve. There are additional cooling costs related to this power loss, as this heat has to be dissipated away from the valve to maintain the operating temperature of the valve below 125 degrees C.

- **Energy loss:** Annual energy loss for each thyristor and diode switch is 21024 kWh (8760*2.4) and 14892 kWh (8760*1.7) respectively. The cost for the energy loss is (0.8*21024) 16819$ for thyristor switch and (0.8*14892) 11914$ for diode switch, if the electricity cost per kWh is 0.8$. Therefore, the savings for this energy loss is $(\frac{16819-11914}{16819}*100\%)$ 29% in each year in case of a diode switch.

From the comparison of a thyristor and diode-bridges, it can be concluded that the cost of the overall HVDC system can be reduced by 11% with a diode-bridge instead of a thyristor-bridge in the proposed model. But the cost will also be increased in some respect due to the implications of increased filter costs. The cost analysis for the filter is given in chapter 3. Therefore, to evaluate the above-mentioned proposals it will be necessary to study the new hybrid diode-thyristor rectifier model, make an assessment of

the proposed option for steady state & dynamic operational tests, make an assessment of the capital and operational cost considerations for the proposed option, and implications for the controls, filters, systems of the proposed model.

1.3 Choice of Simulation tools for this study

For power electronics simulation, many simulation packages such as PSCAD/EMTDC, SIMPLORER, etc are available. However, at Concordia University, both PSIM and EMTP (Electro-magnetic Transients Program) are available. EMTP is highly suited for simulating high-power electronics in power systems and is capable of representing controllers with the same ease as in a high-level language. As this thesis deals with the HVDC systems, it was decided to use new version of EMTP-RV (Restructured Version) as the main simulation tool for this study. For assisting in the development of the controllers, MATLAB is well known as a suitable simulation and signal-processing tool and so it was decided to use it for designing the controller.

1.4 Thesis Outline

In Chapter 2, a brief discussion of High Voltage Direct Current (HVDC) systems is presented. A comparison of AC and DC transmission and their limitations is presented. Then applications of DC transmission, a description of all the components of the HVDC system, and the control strategy employed in DC transmission is presented in detail.

In Chapter 3, modeling details of the proposed hybrid diode-thyristor rectifier system are presented. This is followed by a model comparison of the proposed model and the standard model. The size of the AC and DC filters for both the standard and the proposed models are presented.

In Chapter 4, a systematic approach to optimize the PI parameters of the HVDC controller and an approach based on Bode plot for designing the PI controller, two control schemes are presented. Then a comparison of these two control schemes is described.

In Chapter 5, results from the proposed model and standard model under various static and dynamic conditions, and including a comparison of these results are presented.

In Chapter 6, conclusions from this study and recommendations for future works are presented.

Chapter 2

HIGH VOLTAGE DIRECT CURRENT TRANSMISSION

2.1 Introduction:

High Voltage Direct Current (HVDC) is a major user of power electronics technology. HVDC transmission system was tried by a French engineer Rene Thury, from Moutiers to Lyons in the early days of the present century and was first used commercially in Gotland (1954) and Sardinia (1967) in under-sea cable interconnections. HVDC trunk-line transmission involves the erection of two converter stations with transformers and valves, one for inversion, the other for rectification. Now a brief discussion is presented about DC transmission.

2.2 Comparison of AC-DC Transmission:

For making a planning selection between AC and DC transmission, it is necessary to consider the following factors:

- Economics of transmission,
- Technical performance, and
- Reliability or availability

2.2.1 Economics of transmission:

Cost is one of the major factors that influence the selection of either AC or DC transmission. The investment and operational costs are the costs of the transmission line and the terminals. The investment cost includes actual infra structure i.e. Right of Way (RoW), transmission towers, conductors, insulators, and terminal equipments. The operational costs include mainly the cost of losses. The advantages of the DC transmissions are:

- A DC line requires less RoW, simpler and cheaper towers and reduced conductor and insulator costs as a DC line can carry as much power with two conductors as an AC line with three conductors of the same size with the same insulation level. The power transmission losses are reduced by 67% with DC because it uses only two conductors instead of three conductors in an AC system.

- Power losses are reduced further as there is no skin effect with the DC system.

- The corona effects are less significant in a DC line as it does not require reactive power compensation.

The other factors are the cost of compensation and terminal equipment. In DC lines, terminal equipment costs are increased due to the presence of converters and filters.

Figure 2.1 shows the cost breakdown (with and without considering losses) between the thyristor based HVDC system and the high voltage AC system.

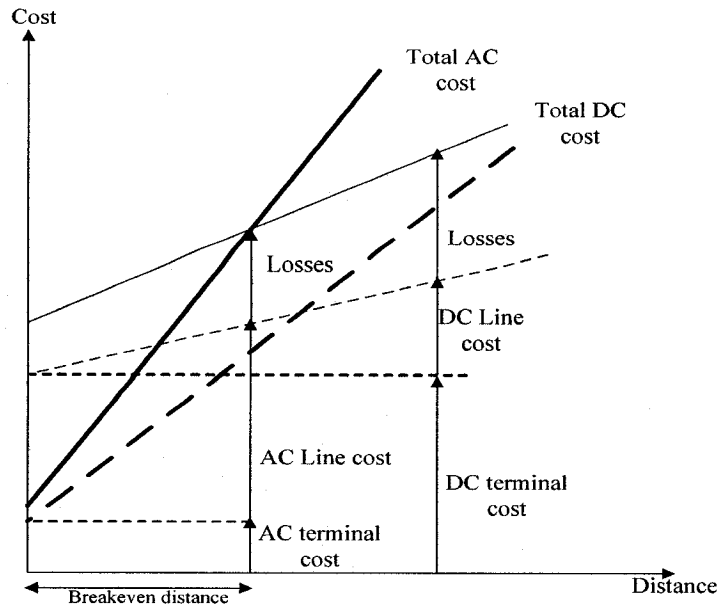

Figure 2.1: The cost breakdown between HVDC system and HVAC system [15]

The summary of this figure is as follows: a thyristor based HVDC transmission line costs less than an AC line for the same transmission capacity. The investment costs (terminal costs) for the HVDC converter stations are higher than for high voltage AC substations due to the fact that HVDC converter stations must perform the conversion from AC to DC and vice versa. Initial loss levels are higher in an HVDC system. In contrast, loss levels increase with distance in a high voltage AC system. AC tends to be more economical than DC for distances less than the "breakeven distance" but is more expensive for long distances. The "breakeven distance" can vary from 500 to 800 km in overhead lines depending on the per unit line costs. The DC transmission cost is higher than the AC transmission cost within the "breakeven distance".

2.2.2 Technical performance:

The advantages of the DC transmission over AC transmission according to the technical performance are as follows [17]:

- DC transmission can limit fault currents in the DC lines very quickly.

- DC transmission has the ability to enhance transient and dynamic stability in associated AC networks.

- DC transmission has full control over power transmitted.

- Stability Limit: The stability of the AC lines is dependent on the power per circuit and the length of the line. Therefore, for long lines, cost is increased but for the DC system there is no relation between the line length and the stability of the system.

- Voltage Control: To control constant voltage at the two ends an AC line requires increasing reactive power as the line length increases but a DC line does not require any reactive power for compensation.

- Line Compensation: Line compensation is not necessary for DC lines but is needed for AC transmission over long distances to overcome line charging and stability limitations.

- Different frequency systems can be interconnected by DC systems. However, for AC systems, even with coordinated control, interconnection of systems is problematic.

- High magnitude of ground impedance in the AC system will affect efficient power transfer and also result telephone interference. The ground impedance is negligible in the DC link.

2.2.3 Reliability and Availability:

- The reliability of a DC transmission system is good and comparable to an AC system.
- Both energy availability and transient reliability of existing in DC systems with thyristor valves is 95% or more [10].

2.3 Limitations of DC Transmission:

Though we argued that DC transmission is more economical than AC transmission, DC transmission is limited by the following factors:

- High cost of conversion equipment,
- Inability to use converter transformers to alter voltage levels,
- Generation of harmonics,
- Requirement of reactive power, and
- Complexity of control

The objectives of this thesis are to minimize the limitations of DC transmission and are concerned here about the high cost of the conversion equipment.

2.4 Applications of the DC Transmission:

DC transmission is applicable for:

- Long distance bulk power transmission,
- Asynchronous interconnection of the AC system,
- Under ground or underwater cables, and
- Stabilization of power flows in integrated power system.

2.5 Types of HVDC systems:

Three types of DC links are considered in HVDC systems:

2.5.1 Monopolar link:

It has one conductor. It uses either ground or sea return or metallic return. Monopolar link is normally operated with negative polarity, as the corona effects in a DC lines are substantially less in negative polarity. Therefore, monopolar link is used in the proposed HVDC system.

2.5.2 Bipolar Link:

It has two conductors, one positive, and the other negative. It is the mostly used link.

2.5.3 Homopolar Link:

In this link two conductors, having the same polarity usually negative can be operated with ground or metallic return. It has the advantage of reduced insulation costs.

2.6 Components of HVDC system:

Converter stations where conversions from AC to DC and from DC to AC are performed are the main components of HVDC transmission system. The components of the converter stations are as follows:

2.6.1 Converter Unit:

To convert electrical energy from AC-DC or vice versa, HVDC system needs an electronic converter. There are two types of 3-phase converters:

- Current Source Converter (CSC), and
- Voltage Source Converter (VSC)

In 12-pulse model, two 3-phase CSC converter bridges are connected in series in the output of the transformer. Star/star and star/delta converter transformers are connected with the converter unit. The valves may be packaged either as a single, double or quadruple-valve arrangement. The valves may be cooled by air, oil, water, Freon, or liquid cooling using deionized water. Snubber circuits, protective firing, and gapless surge arresters are needed to protect valves. To distribute the off-state valve voltage uniformly across each thyristor level and protect the valve from di/dt and dv/dt stresses, special snubber circuits are needed across each thyristor level. Snubber circuit is composed of the following components:

- A saturating reactor to protect the valve from di/dt stresses during turn-on,
- A DC grading resistor to distribute the direct voltage across the different thyristor level,
- RC snubber circuit to damp out voltage oscillations from power frequency to a few kHz, and

- A capacitive grading circuit to protect thyristor level from voltage oscillations at a much higher frequency [17].

2.6.2 Converter transformer:

Two 6-pulse converter units are connected to the secondary of a converter transformer to form a 12-pulse converter system. Different configurations of the converter transformer are i) 3-phase, 2-winding, ii) 1-phase, 3-winding, iii) 1-phase, 2-winding. The transformers are connected in parallel with neutral point grounded on the AC side. Grounding provides a path for zero sequence currents caused by any asymmetrical fault in the AC system. On the valve side, secondary windings of the transformers are connected in star and delta (to cancel out triplen harmonics) with neutral point ungrounded. To limit the short circuit currents through any valve the leakage impedance of the transformer is chosen between 15-18%.

2.6.3 Filters:

In HVDC system, suitable filters on AC-DC of the converter are needed because of the generation of characteristic and non-characteristic harmonics. Three types of filters are generally used in HVDC system:

i. AC Filter: AC filters are used to eliminate harmonics produced by the converter. In 12-pulse converter system, the characteristic harmonics are 11^{th}, 13^{th}, 23^{rd}, 25^{th},

35^{th}, and 37^{th} and so on. For 11^{th} and 13^{th} harmonics passive single or double tuned shunt R-L-C filter and for 23^{rd} or above harmonic damped filter i.e. high pass filter is used. Passive shunt filters supply 70 – 80% of the total reactive power requirement of each converter station. Recently C-type filters are being used as they provide a more economical design [11]. The remaining reactive power is compensated by the capacitor bank.

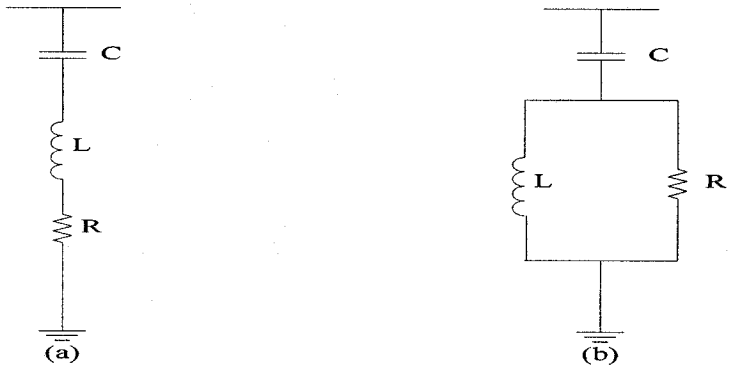

Figure 2.2: AC filters: (a) single tuned; (b) damped

ii. DC Filter: DC filters are used on the DC side of the system to eliminate DC side harmonics. Higher order harmonics may cause interference with nearby voice frequency communication circuits. Usually, a damped filter is used at 24^{th} harmonic. Active filters are now also used to eliminate DC side harmonics for efficiency and space saving purposes.

iii. High Frequency (RF/PLC) filters: These filters are used to suppress any high frequency currents from entering the transmission line. They are connected between the converter transformer and the AC bus station. Sometimes, they are

connected between the DC filter and DC line on the high voltage DC bus and also on the neutral side.

2.6.4 DC Smoothing Reactor:

A DC smoothing reactor is used for the following purposes:

- Limit the rate of change of direct current for making the commutation process more robust,
- Smooth the DC current, and
- Protect the converter from line surges.

2.7 Analysis of Converter Bridge:

A 6-pulse converter bridge (figure 2.3) is used for theoretical analysis.

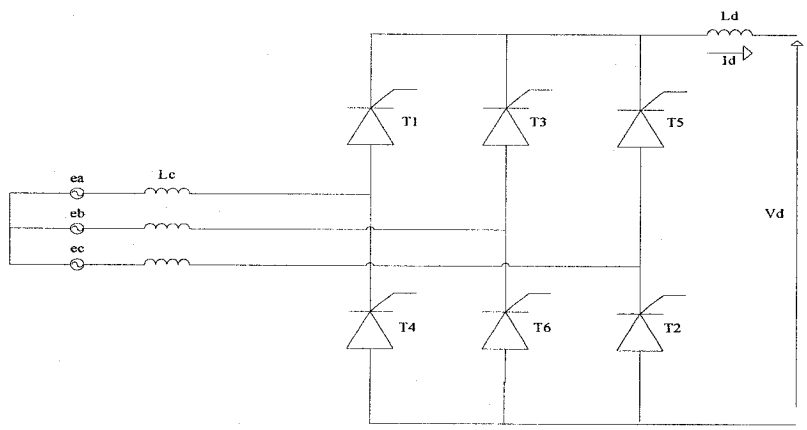

Figure 2.3: 6-pulse Converter Bridge

The instantaneous line-to-neutral voltages are:

$$e_a = E_m \cos(wt+60^o) \tag{2.1}$$

$$e_b = E_m \cos(wt-60^o) \tag{2.2}$$

$$e_c = E_m \cos(wt-180^o) \tag{2.3}$$

In addition, line-to-line voltages are:

$$e_{ac} = e_a - e_c = \sqrt{3}\, E_m \cos(wt+30^o) \tag{2.4}$$

$$e_{ba} = e_b - e_a = \sqrt{3}\, E_m \cos(wt-90^o) \tag{2.5}$$

$$e_{cb} = e_c - e_b = \sqrt{3}\, E_m \cos(wt+150^o) \tag{2.6}$$

The following assumptions are made for the analysis of the converter:

- The DC current I_d is considered constant,
- The valves are ideal switches, and
- The AC system is strong (infinite).

After analyzing the converter bridges, the DC output voltages are as follows:

For Rectifier:

$$V_{dr} = V_{dor} \,.\, cos\alpha - R_{cr} \,.\, I_d \tag{2.7}$$

where,

$$V_{dor} = 3/\pi \,.\, \sqrt{2} \,.\, V_{LL} \quad and \; R_{cr} = 3/\pi \,.\, wL_{cr} \tag{2.8}$$

For an inverter:

Depending on choice of the delay angle or extinction angle as the control variable there are two options.

$$-V_{di} = V_{doi} \cdot \cos\beta + R_{ci} \cdot I_d \quad (2.9)$$

$$-V_{di} = V_{doi} \cdot \cos\gamma - R_{ci} \cdot I_d \quad (2.10)$$

Where,

V_{dr} & V_{di} = DC voltages at the rectifier and inverter,

V_{dor} & V_{doi} = Open circuit DC voltages at the rectifier and inverter,

R_{cr} & R_{ci} = equivalent commutation resistance at the rectifier and inverter,

L_{cr} & L_{ci} = Leakage Inductance of the converter transformer at the rectifier and inverter,

I_d = DC current,

α = delay angle, and β = advance angle at the inverter ($\beta = \pi - \alpha$),

μ = overlap angle, and γ = extinction angle at the inverter ($\gamma = \pi - \alpha - \mu$)

2.8 Controls and protection:

The main functions of the DC controls are:

- To control the power flow between the terminals,
- To stabilize the AC system against operational mode of the DC link, and
- To protect the equipment against voltage/current stresses caused by faults

2.8.1 Purpose of Control:

The main features of DC controls are as follows:

1. Limit the maximum DC current to prevent failure in the valves,
2. Keep the power factor as high as possible,
3. Keep the maximum DC voltage for transmission purposes to minimize the DC line and the converter valves losses,
4. Prevent commutation failures at the inverter station,
5. Keep the AC reactive power demand low at both the converter terminal,
6. Maintain the power delivered or control frequency at one end,
7. Prevent arc back at the rectifier valves.

2.8.2 Control Strategy:

The relation between DC current and DC voltage is illustrated in equation 2.7, 2.9, and 2.10.

$$V_{dr} = V_{dor} \cdot \cos\alpha - R_{cr} \cdot I_d \tag{2.7}$$

$$-V_{di} = V_{doi} \cdot \cos\beta + R_{ci} \cdot I_d \tag{2.9}$$

$$-V_{di} = V_{doi} \cdot \cos\gamma - R_{ci} \cdot I_d \tag{2.10}$$

The three relations represent straight line on the V_d-I_d plane. Equation (2.9) represents beta characteristic with a positive slope. Equation (2.10) has a negative slope i.e. gamma characteristic. The characteristics of rectifier and inverter are shown in figure 2.4.

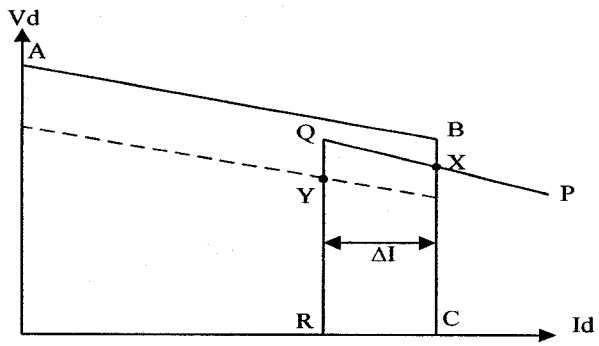

Figure 2.4: Static V_d-I_d characteristics for a two terminal link

In the rectifier characteristics, there are two modes: alpha min (line AB) and constant current (line BC) mode. The alpha minimum mode of control is imposed by the natural characteristics of the rectifier. The rectifier acts as a diode rectifier if the valves operate at alpha equal to zero. However, for the requirement of minimum positive voltage before firing the valves to ensure conduction a minimum alpha i.e. about 2-5° is needed [17].

In the inverter characteristics, there are also two modes: gamma min (line PQ) and constant current (line QR). The intersection of the two characteristics determines the mode of operation. From the figure, it is seen that the cross over point X is the operating point for the DC link. The constant current characteristic is shown by the vertical line QR. The current demanded by the rectifier is much more than the current demanded by the inverter. It is shown by ΔI in the figure and is typically 0.1 pu. ΔI is called as the current margin and the current margin should be large enough so that the rectifier and the

inverter constant current mode do not interact due to any current harmonics in the DC current. If there is any voltage decrease in the rectifier AC bus the operating point moves from point X to point Y. At this point, current is reduced to 0.9 pu of its previous value and the voltage control will shift to the rectifier and the power transmission is 90% of its original value.

2.8.3 Modified Control Characteristics:

Figure 2.5 shows the modified control characteristics. It can maintain power flow even under system disturbances.

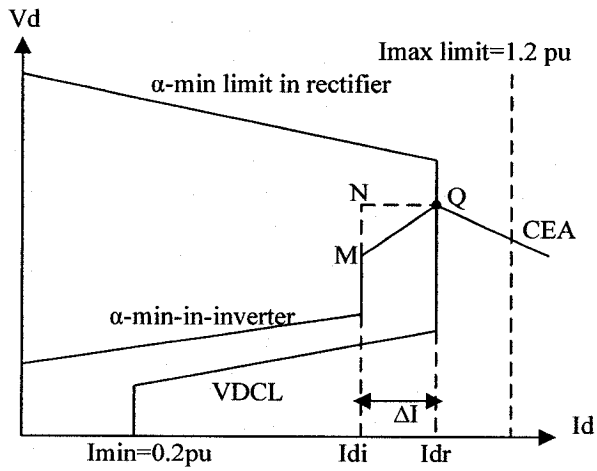

Figure 2.5: Modified V_d-I_d characteristics

At the Rectifier:

1. Voltage Dependent Current Limit (VDCL): During disturbances when the AC voltage at the rectifier or the inverter is decreased, VDCL block limit the DC current and helps the DC link to recover from faults.

2. I_d-min limit: The DC current extinction caused by the valve current drop below the hold-on current of the thyristor is prevented by limiting DC current to 0.2 to 0.3 pu. The size of the smoothing reactor affects the magnitude of I_d-min.

At the Inverter:

1. Alpha-min limit at inverter: For alpha-min limit in inverter, the value of alpha should be 100-110 degrees. The inverter cannot operate in the rectifier region as the power reversal occurs.

2. Current error region: With weak AC system, the slope of the CEA control mode is quite steep and may cause multiple crossover points with the rectifier characteristics. To overcome this problem the inverter CEA characteristic is modified either as a constant beta characteristic (line QM) or as a constant voltage characteristic (line QN) within the current error region.

2.9 Modern trends:

In the present decade 2000-2010 the new trends is to reduce costs so that the DC transmission can become competitive with the AC transmission. The next generation HVDC equipment will be influenced by the following electronic equipments.

- Thyristor Valves: Present rating of the thyristor valve is 8-9 kV and the power handling capacity of 1500 kW. Therefore, the number of series connected valves is decreased as a result cost is reduced and reliability is improved.

- High DC transmission voltage: High voltage is used for long distance transmission to minimize losses. The value of the transmission voltage is ±500 kV. The industry is trying to raise this voltage to ±800 kV.

- Controls: Now the control functions are implemented in digital platforms and are fully integrated having monitoring, control, and protection features. Therefore, reliability and availability of the equipments are increased.

- Filters: The active DC filters are invented for eliminating the DC harmonics. This filter is more efficient and can operate over a wide spectrum of frequencies. In the AC side, electronically tunable inductor based on transducer principle is used instead of passive components. Therefore, this will lead to a much-increased filtering capacity.

- AC-DC Measurements: The current transducer now replaces past measuring equipment. It improves reliability, reduces costs, and the accuracy of the measurement technique is better than 0.5% in the frequency range from DC to 7 kHz.

2.10 Summary:

The advantages & disadvantages of HVDC system and also a comparison with AC system were discussed in details in this chapter. From our discussion, it is clear that an HVDC system is very important for power transmission both from a cost and necessity point of view.

Chapter 3

MODEL DESCRIPTION

3.1 Introduction:

A new hybrid diode-thyristor rectifier HVDC transmission system is presented as the proposed model. The performance of this proposed model is compared with the standard HVDC system, which is based on the CIGRE (The Conseil International des Grands Reseaux Electriques) Benchmark HVDC system operating with weak AC system. Both the proposed model and the standard model will be discussed in this chapter.

3.2 Proposed Hybrid Diode-Thyristor Rectifier Model:

Figure 3.1 presents the proposed hybrid diode-thyristor rectifier HVDC system. The ratings used in this model are based on the standard model. The main parts of the proposed model are as follows: 1) AC side of the system, 2) Converter block, 3) Controller block, and 4) DC side of the system.

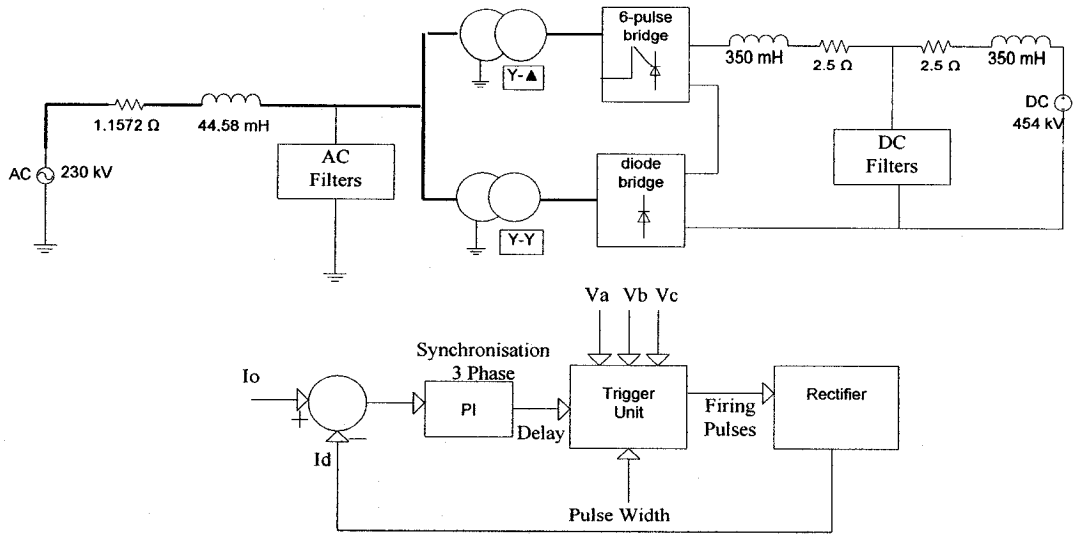

Figure 3.1: 12-pulse hybrid diode-thyristor rectifier model

3.2.1 AC side of the system:

On the AC side of the system, there is AC supply network, AC filter, and the converter transformers.

a. AC supply network:

The system is connected to a 230 kV, 60 Hz line frequency AC network. The AC supply network is represented by a Thevenin equivalent circuit where the Thevenin voltage is the source voltage and the equivalent impedance is the source impedance. The source impedance is primarily inductive (44.54 mH) and has a small value of resistance (1.1572 Ω). All values of the source voltages and the impedances are the same as the standard model. This allows us to compare the advantages, disadvantages, and characteristics of both models.

b. AC Filters:

The AC filters act on the harmonics generated from the converter units and prevent the harmonics from entering the AC system. They also provide the reactive power requirement of the converter unit. Due to the unbalanced harmonic cancellation between the diode-rectifier and the thyristor-rectifier, the proposed HVDC system generates characteristic harmonics of the order of 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 35^{th}, and 37^{th} and so on. The harmonics present in the AC side of this topology as $6n\pm1$, where n = 1, 2... and so on. In an HVDC system, two types of filters are generally used, active, and passive filters. However, the cost of an active filter is high as compared with a passive filter. A passive filter is traditionally used to lower the cost of the HVDC system. The passive filters can be of either tuned type or damped type or both (Figure 3.2).

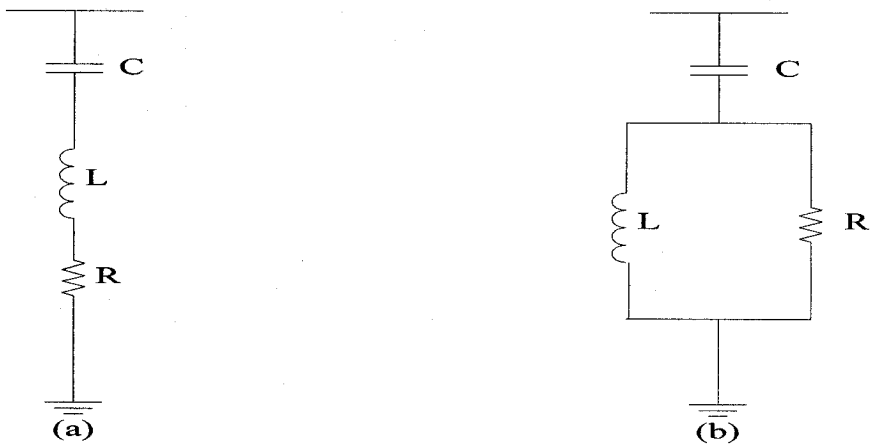

Figure 3.2: AC filters: (a) single tuned; (b) damped

Tuned filters are used for 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics. A high pass filter is used for eliminating the high frequency harmonics (17^{th} and upwards) and the shunt capacitor bank is used for supplying the remaining reactive power requirement of the

converter unit. Figure 3.3 shows the filter arrangement of the proposed model. The calculations of the filter components are shown in Appendix A.

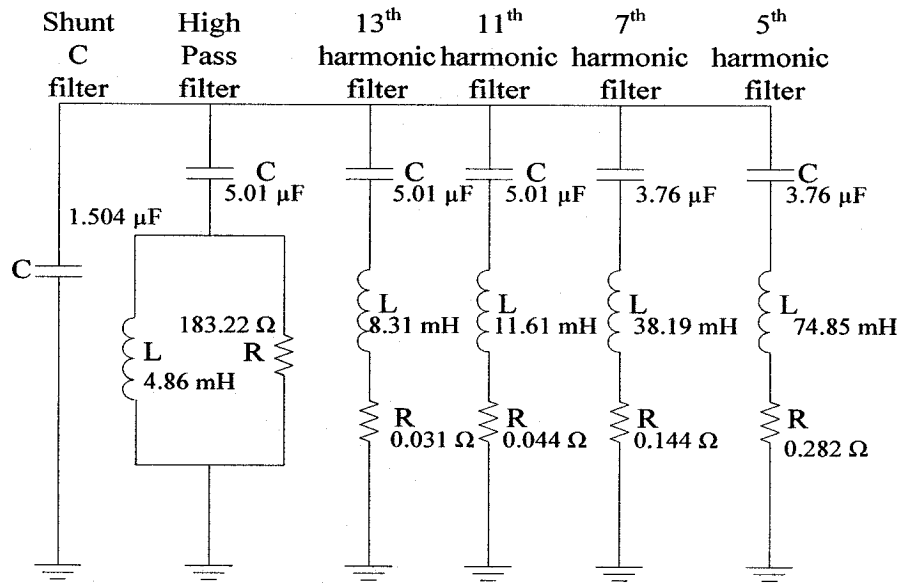

Figure 3.3: AC side filter arrangement for the proposed model

c. Converter Transformer:

The AC side of the system is isolated from the DC side with the converter transformer. In the proposed model, two converter units are connected in series and to the secondary of the converter transformer (Figure 3.4). The converter transformer can have the following configurations 1) 1-phase, 3-windings, 2) 1-phase, 2-windings 3) 3-phase, 2-windings. In this system, a single unit of a 3-phase transformer is used for economical reason. The secondary side (valve side) windings of one transformer are connected in STAR configuration (with neutral point ungrounded) and the other transformer in DELTA configuration to cancel out the triplen harmonics that might appear when the AC voltages are unbalanced. The primary side windings of each transformer are connected in STAR connection with neutral point grounded.

Grounding is used here to provide a path for zero sequence currents caused by any asymmetrical fault in the AC system. The size and the voltage rating of each transformer are equal. The leakage reactance of the transformer is chosen to be 15%, which is sufficient to limit fault current through the valves.

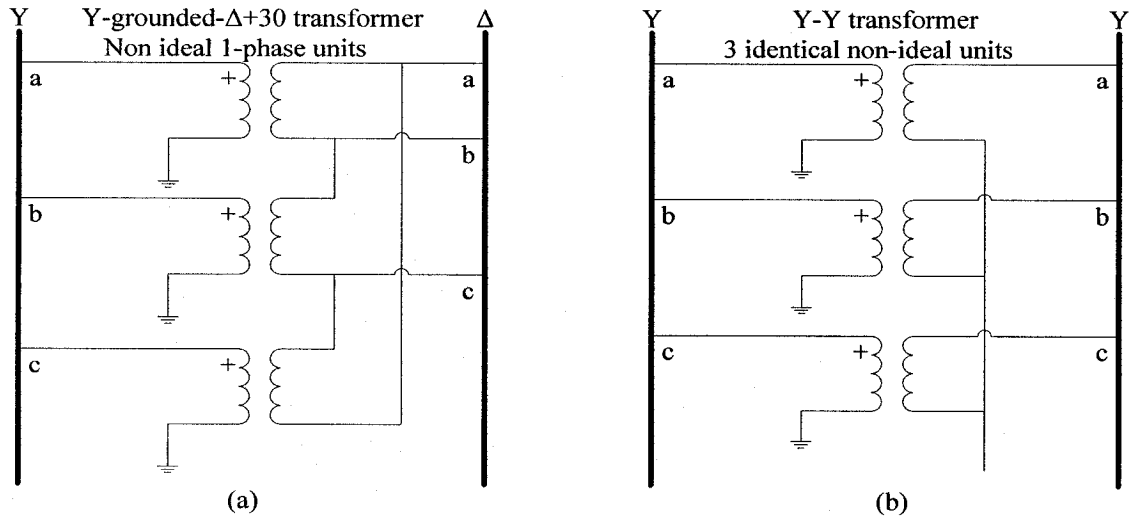

Figure 3.4: Transformer connection of the proposed model.

3.2.2 Converter Block:

The converter block is the most important block in the HVDC system. It performs the conversion from AC to DC or vice versa depending on rectifier or inverter mode of operation. Two 3-phase converter bridges, one thyristor-bridge, and one diode-bridge, (Figure 3.5) are connected in series on the DC side of the system. The AC side of each converter bridge is connected to a separate converter transformer. To protect the valves and diodes from voltage and current surges, R-C snubber circuits are employed for both bridges. The analysis of the converter bridge was given in chapter 2.

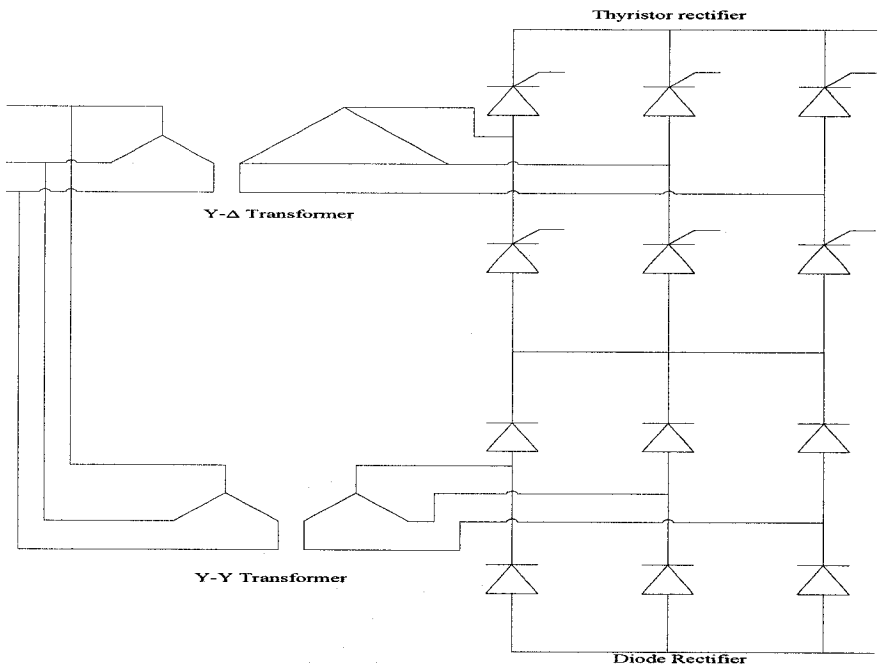

Figure 3.5: 12-pulse hybrid diode-thyristor rectifier block.

Snubber circuit:

Each thyristor and diode is protected against a high rate of rise of voltage and current i.e. dv/dt, and di/dt protection respectively. Figure 3.6 (a), (b) shows the snubber circuit arrangement for both the thyristor and the diode.

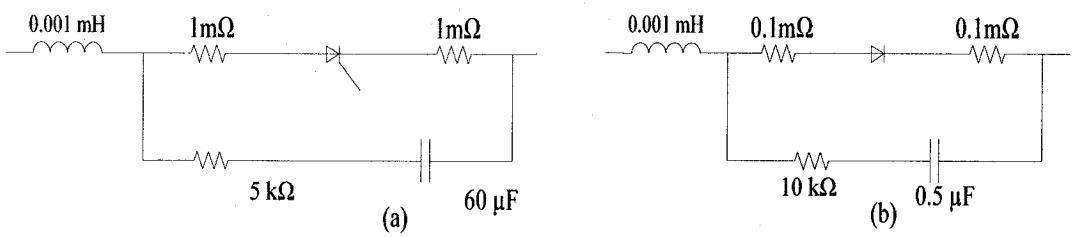

Figure 3.6: Snubber circuit for (a) thyristor, (b) diode

The snubber circuit protects the valve from a rapid rise in voltage, and a saturating reactor is used to protect the valve from di/dt stresses during turn-on. The di/dt inductor and RC snubber also serve the following purposes:

- The di/dt inductors separate two ideal switches being connected to a common node (This is only required for the numerical simulation purposes with EMTP), and
- The RC snubber provides an alternative current flow path when the switch opens an inductive circuit.

RC Snubber parameters have an effect on the valve voltages. Figure 3.7 shows the effects of RC values in the valve voltages and valve currents. From the figure, it is easily visible that the resistance has more impact on the valve voltages and current than the capacitor. If the values of RC are not selected properly, it will result in poor operation, over-voltages, and erroneous measurement in delay angle specially when interacting with weak AC networks.

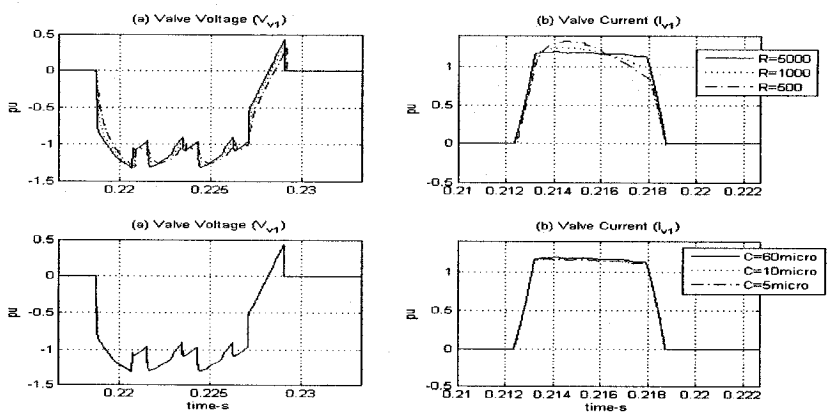

Figure 3.7: Effects of R C in thyristor voltages and currents (Time step=10 μs)

3.2.3 Controller Block:

A current controller unit is used for the thyristor-bridge to maintain the output DC current close to its reference value and to generate appropriate firing signals for each of the thyristor. The purpose of the controller is as follows:

- To limit maximum direct current to avoid valve damage,
- To keep the DC voltage level high to reduce power transmission loss,
- To maintain a minimum extinction angle to avoid commutation failure,
- To maintain a minimum firing angle to reduce reactive power consumption.

In the proposed model, one controller block is needed for the thyristor-bridge and the diode bridge does not need the controller block. This is one of the most important advantages of this configuration. The controller block for the thyristor-bridge will be discussed in the next chapter.

3.2.4. DC side of the system:

The DC side of the system consists of the DC filters, the DC smoothing reactor, and the DC transmission line.

a. DC filters:

The DC filters are used to eliminate higher order harmonics, which can cause noise in communication systems. In this system, 6^{th} harmonic and higher order harmonics are

present respectively. A high pass filter is used to eliminate these harmonics. The calculation of the DC filter is also given in the appendix A.

b. DC smoothing reactor:

A DC smoothing reactor is used in each pole of the converter station to serve the following purposes:

- To smooth the ripple in the DC current and also prevent current from becoming discontinuous at light loads,
- To limit the peak fault current in the rectifier due to short circuit in the DC line,
- To decrease the incidence of commutation failures in the inverter during dips in AC voltage, and
- To prevent commutation failure in the inverter by limiting the rate of the DC current increase during commutation in one bridge when the DC voltage of another bridge collapses.

c. DC transmission Line:

The DC transmission line is simply represented by an equivalent T-network. The DC transmission line impedances are lumped into the equivalent smoothing reactor for the sake of simplicity.

3.3 Standard model:

A CIGRE Benchmark based weak AC system having a short circuit ratio of 2.3 is used as the standard circuit (Figure 3.8). The AC grid and DC line components and overall power ratings for this model are exactly the same as the proposed model.

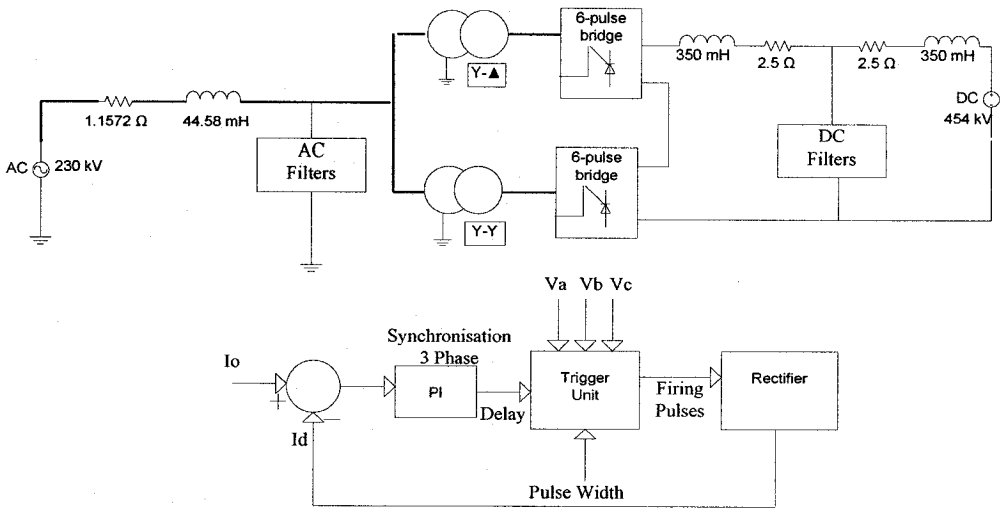

Figure 3.8: 12-pulse standard thyristor model

The main difference between the two models is the converter block, the AC, and DC side filter, and the controller unit and all other components and blocks are the same as the proposed model. The blocks are described below:

3.3.1 Converter block:

Two 6-pulse thyristor-bridges are connected in series in the converter block. Both the thyristor-bridges have identical voltage rating and snubber circuit arrangement. The snubber parameters and the di/dt inductor values are not provided in the CIGRE

Benchmark. However, a suitable choice of these parameters is needed for system stability and circuit fiability.

3.3.2 AC & DC side filter:

In the AC side of the system, 5^{th} harmonic, 7^{th} harmonic, and some high frequency harmonics are not found as the harmonic cancellations between the two 6-pulse thyristor-bridges, connected in series, are possible. For the standard model the harmonics are the order of 12n±1, where n = 1, 2 ..... and so no. The cost of the filtering is less than the proposed model. In the DC side, 6^{th} harmonic is not present so the size of the filter is smaller than the proposed model. The system consists of two 350 mH smoothing reactors and two 2.5 Ω series resistances in the DC side of the system, as shown in Fig. 3.9.

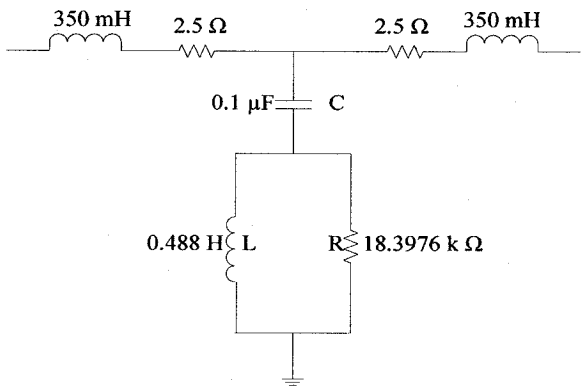

Figure 3.9 Smoothing reactors with DC filter for Standard Model

3.3.3 Controller Unit:

Two identical controller units are used for the two-thyristor converter blocks. The controller unit is similar as that used for the proposed model for its one thyristor converter.

3.4 Comparison of filter sizes:

Since the DC side voltage waveforms and the AC side current waveforms of the thyristor and diode bridges of the hybrid (proposed) scheme are not identical but phase shifted by 30 degrees as for the thyristor (standard and proposed) scheme, some harmonic cancellations do not occur. Therefore, the AC and DC filters of the proposed scheme have to be larger compared to standard model. In this section the sizes of the AC and DC filters of both the proposed model and the standard model are compared. The reactive power, supplied by the filter at fundamental frequency is the size of the filter. A minimum filter suppresses harmonics at the least cost and supplies some reactive power. The capital cost of AC filter is in the range of 5 to 15% of the cost of the terminal equipment and about 60% of this filter cost is that of the capacitors. Hence, substantial savings are possible by judicious choice of size of capacitor and inductor [8].

AC Filter:

The cost of the capacitor is assumed to be directly proportional to its rating. The capacitor rating is

$$P_{rC} = V_1^2 \omega_1 C + \frac{I_{hf}^2}{h\omega_1 C} = S + \frac{V_1^2 I_{hf}^2}{hS} \text{ Mvar} \tag{3.1}$$

where, C = Capacitance (F)

$\omega_1 = 2\pi$ * fundamental frequency

V_1 = Fundamental voltage (kV)

I_{hf} = Harmonic current of order h (kA)

S = Size of capacitor (Mvar)

The rating of the inductor is the sum of its fundamental and harmonic reactive powers:

$$P_{rL} = \frac{S}{h^2} + \frac{V_1^2 I_{hf}^2}{hS} \tag{3.2}$$

Neglecting the cost of the resistor, the total cost of the filter is,

$$K = P_{rC} U_C + P_{rL} U_L \tag{3.3}$$

where, U_C and U_L are the unit cost of capacitor and inductor respectively.

Assuming that the total reactive power of both the three phase standard model and the proposed model is 480 Mvar.

The capacitor ratings of standard and proposed model:

The capacitor rating for the standard and the proposed model is, $P_{rC} = S$ Mvar (From equation 3.1 neglecting the harmonic reactive power). Table 3.1 shows the capacitor rating for both models. It is found that the filter cost of the capacitor is same for both models. So no extra cost is needed for the proposed model for designing the filter capacitor.

Table 3.1: Capacitor size (S) of the Standard model and the proposed model

Harmonic order	Capacitor rating S (Mvar) in per phase	
	Standard Model	Proposed Model
5^{th}	-	25
7^{th}	-	25
11^{th}	50	33.33
13^{th}	50	33.33
High pass	50	33.33
C filter	10	10
Total	160	160

The inductor ratings of the standard model:

11^{th} harmonic filter: $P_{rC} = S = 50$ Mvar

From the harmonic spectrum $I_{11f} = 148.12$ A (peak) = 104.74 A (rms)

The magnitudes of all the current harmonics (example: 5^{th}, 7^{th}, 11^{th}, 13^{th} and so on for both proposed and standard model) used for calculating the filter size of the reactors were obtained from simulations for rated value of the DC current i.e. 1600 A.

$$P_{rL11} = \frac{S}{h^2} + \frac{V_1^2 I_{hf}^2}{hS} = \frac{50}{(11)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.105)^2}{11*50} = 0.766 \text{ Mvar} \quad (3.4)$$

13^{th} harmonic filter:

I_{13f} = 98.51 A (peak) = 69.66 A (rms)

$$P_{rL13} = \frac{50}{(13)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.0697)^2}{13*50} = 0.425 \text{ Mvar} \quad (3.5)$$

High pass filter (23^{rd} harmonic and above):

I_{hpf} = 20.24 A (peak) = 14.31 A (rms)

$$P_{rLhp} = \frac{50}{(23)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.0143)^2}{23*50} = 0.098 \text{ Mvar} \quad (3.6)$$

The total inductor rating = (0.766 + 0.425 + 0.098) Mvar = 1.289 Mvar

<u>The inductor ratings of the proposed model:</u>

5^{th} harmonic filter:

I_{5f} = 348.92 A (peak) = 246.72 A (rms)

$$P_{rL5} = \frac{25}{(5)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.247)^2}{5*25} = 9.60 \text{ Mvar} \quad (3.7)$$

7^{th} harmonic filter:

I_{7f} = 216.69 A (peak) = 153.22 A (rms)

$$P_{rL7} = \frac{25}{(7)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.153)^2}{7*25} = 2.87 \text{ Mvar} \quad (3.8)$$

11^{th} harmonic filter:

I_{11f} = 62.18 A (peak) = 43.97 A (rms)

$$P_{rL11} = \frac{33.33}{(11)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.044)^2}{11*33.33} = 0.368 \text{ Mvar} \quad (3.9)$$

13^{th} harmonic filter:

I_{13f} = 38.73 A (peak) = 27.39 A (rms)

$$P_{rL13} = \frac{33.33}{(13)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.0274)^2}{13*33.33} = 0.228 \text{ Mvar} \quad (3.10)$$

High pass filter (17^{th} harmonic and above):

I_{hpf} = 47.53 A (peak) = 33.61 A (rms)

$$P_{rLhp} = \frac{33.33}{(17)^2} + \frac{(\frac{230}{\sqrt{3}})^2 * (0.0336)^2}{17 * 33.33} = 0.15 \text{ Mvar} \quad (3.11)$$

Total inductor rating = (9.6+ 2.87+ 0.368+ 0.228+0.15) Mvar = 13.216 Mvar

DC Filter: (High pass filter)

Table 3.2: DC filter ratings for both models

n^{th} order	Model	QF	R (kΩ)	L (H)	C (μF)
12^{th} harmonic	Standard	100	18.39	0.4886	0.1
6^{th} harmonic	Proposed	150	22.11	0.391	0.5

3.5 Summary:

The descriptions of the proposed hybrid HVDC model and the standard HVDC model based on CIGRE Benchmark were presented. All the blocks such as AC side of the system, converter block, controller block, filters, and DC side of the system of both the models were discussed. The comparisons of the model construction of both the models were also presented. For simplifying the power converters, the ratings of the AC filter inductors need to be increased by 11.927 Mvar, roughly ten times. The capacitor ratings for the AC filter remain the same, since the original capacitors can be redistributed into the additional filter branches. In case of DC filter, it is seen (Table 3.2) that the values of capacitance and resistance are little bit higher in proposed model than the standard model and inductance value is lower in proposed model than the standard model.

Chapter 4

CONTROLLER DESIGN

4.1 Introduction:

In this chapter, the controller design of the proposed diode-thyristor hybrid rectifier HVDC model is described. The system model consists of one 6-pulse thyristor-bridge for which a controller is needed and one 6-pulse diode-bridge for which a controller is not needed. Therefore, the design of the controller applies for the 6-pulse thyristor-bridge only. In addition, the same controller unit (perhaps with different gains) can be used for the two 6-pulse thyristor-bridges in a 12-pulse thyristor rectifier HVDC model (called the standard model). So the goal to reduce costs is partly achieved with the single controller unit in the proposed model.

4.2 Steps for designing the controller:

In an HVDC transmission system, a converter bridge controller is designed to maintain specific power transmission characteristics. The basic power control is achieved by having one of the converters' controls its DC voltage while the other converter controls the current through the DC circuit. One form of the controller which is widely used in industrial process control is called a three term PID controller [18]. The transfer function of the PID controller is:

$$G_c(s) = K_p + \frac{K_i}{s} + K_d s = \frac{K_d s^2 + K_p s + K_i}{s} \tag{4.1}$$

where, K_p is the proportional gain, K_i is the integral gain, and K_d is the derivative gain. If $K_d = 0$, then the controller is proportional plus integral (PI) controller,

$$G_c(s) = K_p + K_i/s \tag{4.2}$$

PI controllers are used to control the DC current to keep the power (current) order at the required level. The control system acts through firing angle adjustments of the thyristor valves. The following steps are used for designing the control system:

- First, a transfer function for each block i.e. the converter block, the DC line with the DC filter block, and the measurement block is determined.
- Second, an open-loop transfer function of the system is calculated.
- Third, a PI controller is calculated to improve the rise time and reduce the steady-state error. The PI parameters are selected by a systematic approach considering the requirements of system stability.
- Finally, using ITAE (Integral of Time multiplied by the Absolute value of the Error) criterion, which is one of the synthetic indexes for evaluating the control system's performance, PI parameters of the controller are optimized. This step is done for the optimization method for designing the controller. A step response of the DC current is performed with these optimized PI parameters to verify the performance.

4.3 Transfer function of the proposed model:

The control system of the hybrid diode-thyristor rectifier is represented by the following four blocks: PI controller block, converter block, DC line with filter block, and measurement block. The transfer function of the total system is the product of transfer functions of each of the four blocks. Therefore, the open-loop transfer function of the control system is:

$$G(s) = G_o(s)\, G_1(s)\, G_2(s)\, G_3(s) \tag{4.3}$$

Where $G_o(s)$ = transfer function of the PI controller,

$G_1(s)$ = transfer function of the converter,

$G_2(s)$ = transfer function of the DC line with filter, &

$G_3(s)$ = transfer function of the measurement equipment.

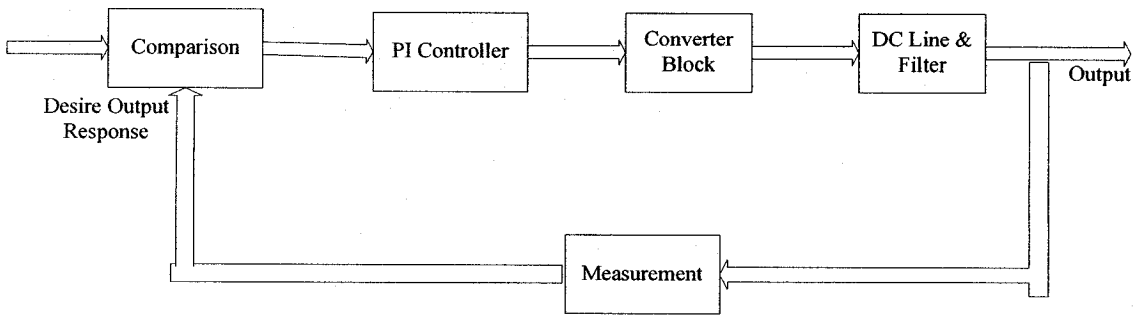

Figure 4.1: Block diagram of a hybrid diode-thyristor rectifier system

4.3.1 PI Controller:

In an HVDC system, it is not necessary to use a PID controller (proportional, integral, and derivative) as a simpler PI controller gives an acceptable response. "Tuning" a

control loop is the adjustment of its PI parameters to obtain the optimum values for the desired control response. The PI controller works in this way: when the DC current is larger than the current order, the PI controller acts to increase the firing angle α, so that current will decrease, and vice versa. A larger K_p typically means a faster response since the larger the error, the larger is the feedback to compensate. A larger K_i implies steady state errors are eliminated faster but at the expense of a larger overshoot. Generalized effects of increasing PI parameters are given in Table 4.1.

Table 4.1: Effects of PI parameters

[file:///E:/Controller%20Design/PID%20controller%20-%20Wikipedia,%20the%20free%20encyclopedia.htm]

CL Response	Rise Time	Overshoot	Settling Time	S-S Error
K_p	Decrease	Increase	Small Change	Decrease
K_i	Decrease	Increase	Increase	Eliminate

These relations are not always true, since K_p, and K_i are dependent on each other. If one of the variables is changed, the other variables will be affected. So this table is only used for guiding the determination of the values for K_p, and K_i. An iterative method is used for determining the actual K_p, and K_i values. The transfer function of the PI controller is given as:

$$G_c(s) = K_p + K_i/s$$

4.3.2 Converter Block:

The converter block consists of one 6-pulse diode-bridge and one 6-pulse thyristor-bridge. The thyristor-bridge can be represented as a first-order block, on condition that

the load time constant is larger than the converter's time delay. The transfer function of the converter block is,

$$G_1(s) = \frac{G}{(1+sT)} \tag{4.4}$$

As the converter is a 6-pulse bridge, the time constant is $T = \frac{1}{6*60}$ ms = 2.777 ms for a 60 Hz system. The output voltage of a 6-pulse thyristor-bridge is,

$$V_{d\alpha} = \frac{3\sqrt{2}}{\pi} E \cos\alpha, \tag{4.5}$$

where E is the AC side L-L voltage in kV.

The output voltage of a diode-bridge is,

$$V_{do} = \frac{3\sqrt{2}}{\pi} E \tag{4.6}$$

The total ideal no-load DC voltage of the system,

$$V_{dT} = V_{d\alpha} + V_{do} = \frac{3\sqrt{2}}{\pi} E \cos\alpha + \frac{3\sqrt{2}}{\pi} E \tag{4.7}$$

Therefore, the proportional constant G is as follows,

$$G = \Delta V_{dT} / \Delta\alpha = -\frac{3\sqrt{2}}{\pi} E \sin\alpha = -1.35*205.45*\sin 29° \tag{4.8}$$

In our system, $E = 205.45\ kV$, and the rectifier firing angle is $\alpha = 29°$ at the operating point. Therefore, the transfer function of the converter (From equation 4.4) is,

$$G_1(s) = \frac{-1.35*205.45*\sin 29^0}{(1+0.00277s)} = \frac{-134.47}{(1+0.00277s)} \tag{4.9}$$

4.3.3 DC Line with DC Filter:

The DC smoothing reactor and high-pass DC filter are the main components in the DC line block. The equivalent circuit of a DC line and the DC filter arrangement is shown in Figure 4.2. Calculations of the impedance of a high-pass DC filter and the values of the smoothing reactor and DC filters are given in the Appendix B.

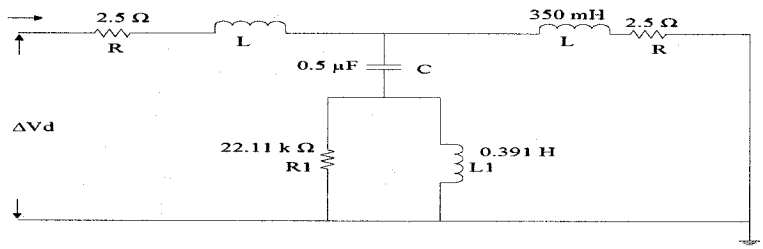

Figure 4.2 DC smoothing reactor and filter circuit

The transfer function of the combined smoothing reactor and DC filter is:

$$G_2(s) = \frac{\Delta I_d}{\Delta V_{d(0)}} = \frac{6.85*10^{-8}s^3 + 8.19*10^{-3}s^2 + 0.42s + 22110}{2.4*10^{-8}s^4 + 4.38*10^{-3}s^3 + 0.31s^2 + 15479.02s + 110550} \tag{4.10}$$

4.3.4 Measurement Equipment:

A first-order measurement block is used to represent the transducer for measurement of DC current. The transfer function of this block is:

$$G_3(s) = \frac{G}{(1+s\tau)} \tag{4.11}$$

where, the time constant τ represents the equipment's response speed, and it is typically chosen as 0.0012 s for current measuring purposes. The proportional gain G is used for

converting the actual current value to per unit, and is equal to the reciprocal of the current rating. The rated DC current of the system is 1.6 kA, so the proportional gain of the measurement block is 1/1.6 = 0.625. The transfer function of measurement block is,

$$G_3(s) = \frac{0.625}{(1+0.0012s)} \tag{4.12}$$

4.4 Methods for Controller Design:

The following alternative methods for determining the HVDC controller gain parameters are feasible:

(a) A gain scheduling adaptive control, but in this method either an accurate plant model or a reliable instrumentation scheme is needed [23];

(b) Artificial neural network (ANN) method; this method is still under experimental investigation and no practical applications exist [20];

(c) Fuzzy logic control method, although this method is highly effective, accurate mathematical descriptions are required which may not be available [7]; and

(d) Trial-and-error method is the simplest method compared to the above techniques; but it needs certain expertise and skills to implement.

Two methods used here for designing the controller are:

- Optimization of the controller, and
- Approach based on Bode plots for designing the controller

4.5 Optimization of the controller:

Considering the problems of optimization, a more systematic approach to optimize the PI parameters of the HVDC controller is needed. One new technique is employed here [24]. The feasible region of system operation, fulfilling the condition of the system stability is first plotted. Then using the ITAE performance index, the PI parameters are optimised. The advantage of this method is that it makes the controller optimization robust and systematic and it can avoid a trial-and-error method i.e. uncertainty. The methodology of this optimization process is achieved in five steps:

4.5.1 Open-loop transfer function:

First, the open-loop transfer function of the control system is determined using the MATLAB program. The MATLAB commands file is given in the Appendix C. The open-loop transfer function of the hybrid diode-thyristor rectifier system is

$$G(s) = \frac{1.727e-005*s^4+2.065*s^3+105.9*s^2+5.574e006*s}{9.528*10^{-11}*s^6+1.741*10^{-5}*s^5+0.005611*s^4+61.76*s^3+1.592*10^4*s^2+110550*s} \quad (4.13)$$

4.5.2 Feasible region of the PI parameters using Bode plots:

Second, the feasible region of the optimizing PI parameter is determined. For the controller design, the first important requirement is the stability limit. The response of the DC current resulting from a dynamic test such as a step change of the current order should meet two requirements: the settling time should be less than 30 ms and the

overshoot should be below 30% of current order change. For this project, two indexes i.e. phase margin Φ_M and gain margin G_M are used for determining the system stability. For a minimum phase system, the system is said to be stable if $G_M > 0$ and $\Phi_M > 0$. The ranges of the stability margin, used here for simulation, are as follows:

$$G_M \geq 6\text{dB} \quad \text{and} \quad 40° \leq P_M \leq 60° \tag{4.14}$$

MATLAB program is used for plotting the feasible region satisfying the system stability condition. The range of the PI parameters is selected according to the system stability. The gain parameter K_p is selected from the range 0 to 4.5 with increments of h_{Kp} (i.e. steps of K_p) = 0.05. The gain parameter K_i is from the range 0 to 100 with increments of h_{Ki} (i.e. steps of K_i) = 2.0. All the points of K_p and K_i that satisfy G_M and P_M are plotted in the K_p-K_i plane. This area is known as the feasible region for PI parameters (Figure 4.3).

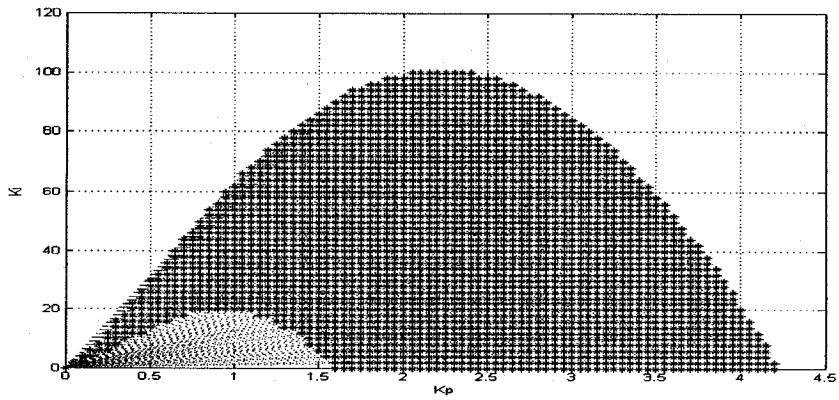

Figure 4.3: Feasible region of the PI parameters considering stability margin

4.5.3 Division of the feasible region:

Third, the feasible region is divided. After establishing the feasible region, the next objective is to optimize the K_p & K_i values. To optimize these K_p & K_i values, the feasible

region is divided into a grid with a certain step size along the vertical (K_i) and horizontal (K_p) directions, so a grid scheme is generated. Four different step sizes of K_p & K_i are used here. All the grid points according to these step sizes are considered. For example, when dividing the feasible region with a step size $h_{Kp} = 0.5$ and $h_{Ki} = 20$, the grid points selected are shown in Figure 4.4.

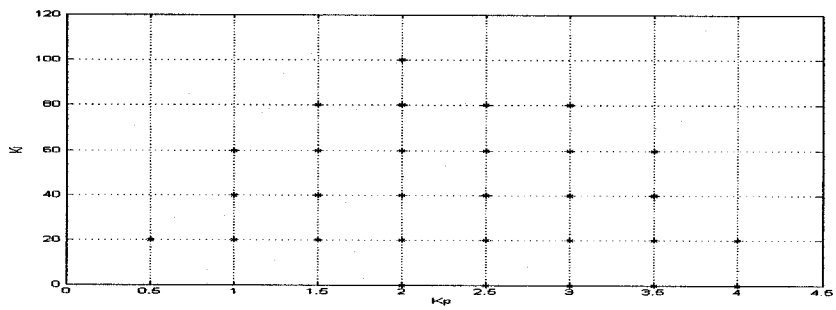

Figure 4.4: Division of the feasible region ($h_{Kp} = 0.5$ and $h_{Ki} = 20$)

4.5.4 Integral of Time multiplied by the Absolute value of the Error (ITAE) Criterion:

Fourth, the controller step response with the PI parameters is simulated corresponding to each grid point and the ITAE function is calculated for each point.

The ITAE criterion (one of the error-integral performance indexes) is used to get the optimal PI parameters corresponding to the minimum objective function value. The objective function J_{ITAE} is,

$$J_{ITAE} = \int_0^T t|e|dt, \tag{4.15}$$

where, the error e is the deviation of the variable from its reference. The upper limit T is a finite time and is chosen arbitrarily so that the integral approaches a steady-state value. The ITAE reflects the influence of the error and the time t synthetically and it reduces the initial error to the integral value and emphasizes the error. At first, a pair of K_p and K_i values is selected from the feasible region. A step change in current order I_o is applied to the system in steady state, and the system response is observed until the system reaches a stable value. The error signal (I_d-I_o) and J_{ITAE} for each pair of PI parameters is calculated. Then, a second pair of K_p and K_i values is selected from the feasible region, and the process is repeated. Once the whole feasible region is tested (i.e. all grid points are tested within the feasible region), this process is repeated until a minimum value of J_{ITAE} is selected. All the obtained J_{ITAE} values are compared, and the minimum J_{ITAE} value is deemed to correspond to the optimal PI parameters. For the step size (Table 4.2) set, h_{Kp} = 0.5 and h_{Ki} = 20, the minimum J_{ITAE} value is = 0.00388819 and the corresponding values of optimum PI parameters are K_p = 2, K_i = 20. Then the feasible region is divided with another different set, and the process is repeated. Table 4.2 shows the step size and optimum points for the four different optimization sets.

Table 4.2: Optimal PI values based on different grid schemes

Optimization set	Step Size		No. of Grid points	J_{ITAE}	Optimum Point	
	h_{Kp}	h_{Ki}			K_p	K_i
1	0.5	20	30	0.00388819	2	20
2	0.3	16	58	0.00379517	1.5	16
3	0.2	10	137	0.00366544	1.4	10
4	0.05	2	2589	0.00347515	1.6	2

From Table 4.2, it is found that with an increase of the grid's precision (i.e. smaller step size), the number of the grid points increase and the value of J_{ITAE} reduces as a result. It is

also noticed that when the grid size decreases, J_{ITAE} reduces as well. This process is repeated until convergence is achieved.

4.5.5 Optimization of PI parameters using step response:

The next step is to verify the rectifier controller's performance with the selected PI parameters. A ±0.1 pu step change for 2.2 s is applied to the rectifier current order to see the response of the measured current. The step responses of the DC current for the four sets of "optimized" PI values, which correspond to the minimal ITAE value, are shown in Figure 4.5. From the Figure 4.5 (d), it is found that the step response of the DC current that uses PI parameters selected from the minimum J_{ITAE} value (0.00347515) follows the current order more closely than from other values.

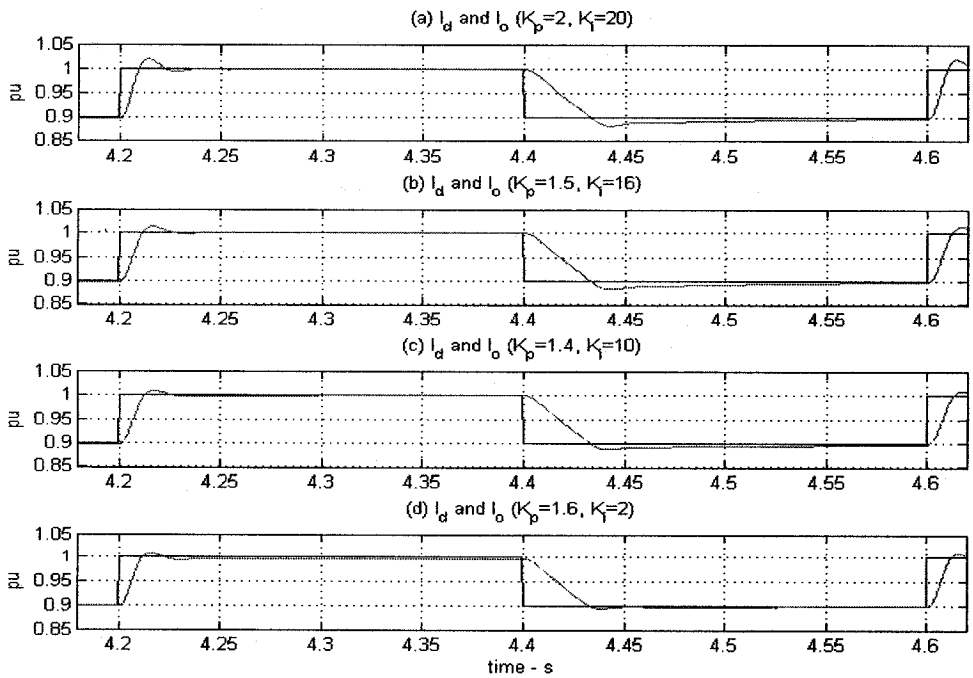

Figure 4.5: Step change of the DC output current for different PI parameters

4.5.6 Summary:

A systematic approach for optimizing the PI parameters of the HVDC controller is presented. First, the feasible region of PI parameters (Figure 4.3) is obtained fulfilling the stability limit requirement (equation 4.14) then the feasible region is divided into a grid with one of four sets of step sizes. Second an optimum point, which has the minimum J_{ITAE} value, in each step size, is selected by applying a step change in current order. For example, in one step size $h_{Kp} = 0.5$ and $h_{Ki} = 20$ the value of optimum PI parameters obtained is $K_p = 2$, $K_i = 20$. Similarly, the other optimum PI parameters are obtained for the other three step sizes. If these four optimum PI parameters are placed in the feasible region it is found that all these points are in one region of this feasible region. So if one set of optimum PI parameters is found, then the next step optimization set can be determined from the neighbourhood of the first optimization set. This will reduce the computation burden greatly. Further investigation needs to be done for utilizing this method in practical projects.

4.6 Approach Based on Bode plots for designing the controller:

In power electronics applications, one of the commonly used controller design employs Bode plots and is based on shaping the loop transfer function so as to achieve a desired crossover frequency and phase margin. The main goal is to choose and tune a controller that adjusts the loop transfer function to an ideal gain vs. frequency profile (Figure 4.6). At low frequencies range, there is a high gain to minimize steady state error; at medium

frequencies, around the crossover frequency, there is a gain slope of -20 dB/decade to ensure enough phase margin; and at high frequency range there is a very small gain to minimize the influence of overall noise and switching harmonics.

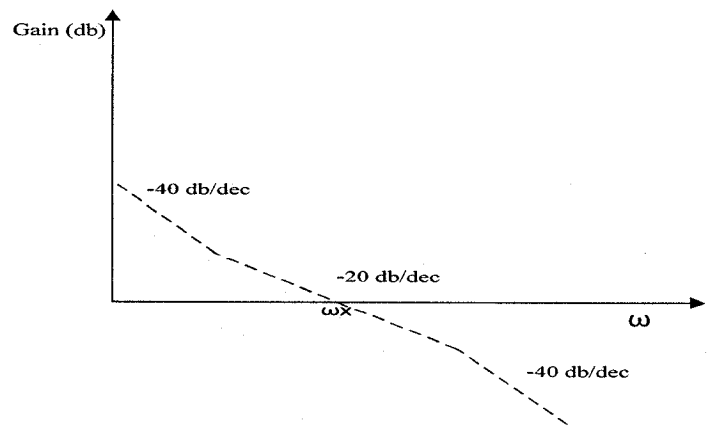

Figure 4.6: Desired shape for the loop transfer function

Let the cross-over frequency of the system, $f_x = 0.2*f_{sw}$ (10 to 20% of the switching frequency) $\approx$ 24 Hz, $\omega_x = 2*\pi*f_x \approx$ 151 rad/sec, and Phase margin is = 45° (from 45° to 60°)

The open-loop transfer function of the plant is: $G_p(s) = G_1(s)*G_2(s)*G_3(s)$

$$G_p(s) = \frac{-5.757e{-}006*s^3 - 0.6883*s^2 - 353*s - 1.858e006}{7.978e{-}014*s^6 + 1.465e{-}008*s^5 + 1.844e{-}005*s^4 + 0.05706*s^3 + 6213*s^2 + 1.592e004*s + 11055} \quad (4.16)$$

Putting $s = j\omega_x = j151$ in to equation 4.16, the value of $|G_p(j\omega_x)|_{dB} = -2.861$dB and

$$\angle G_p(j\omega_x) = 59.7538° \quad (4.17)$$

Therefore, the controller has to introduce a phase lag of -14.75° ($\angle G_c(\omega_x) = PM - 180° - \angle G_p(\omega_x) = 45° - 180° - 59.75° = -194.75°$).

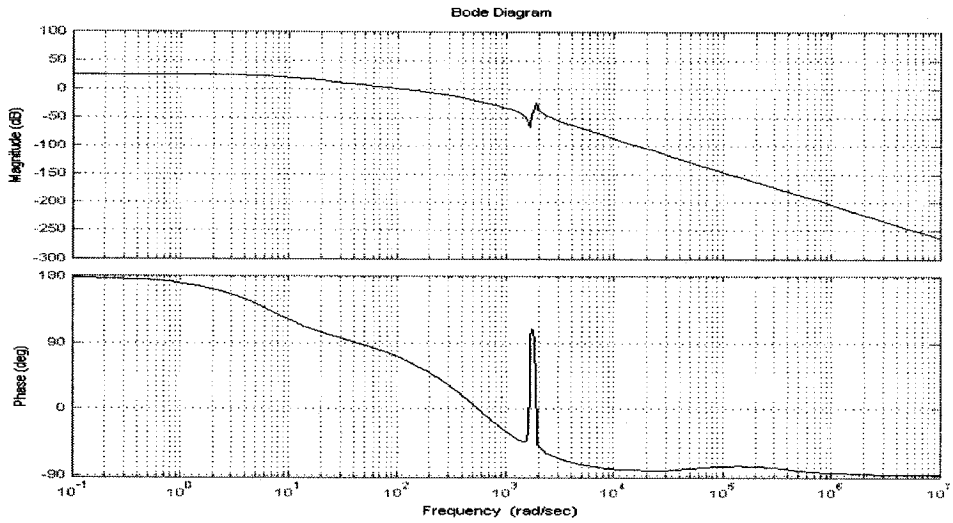

Figure 4.7: The open-loop Bode plot of the plant

The open-loop Bode plot of the plant's transfer function (Figure 4.7) is plotted using the MATLAB program. From the Bode plot of the plant, it is found that it presents a flat profile at low frequencies; so at least one pole at the origin needs to be included to achieve zero error in steady state to a step change. Plants with a flat gain at low frequencies usually require a controller with one or more integrators (I) and for a plant that presents a -20 dB/decade slope around the desired crossover frequency either a PI or a PI type II controller can be used. So the choice of the controller is PI type I or PI type II. The main difference between these two controllers is the presence of a pole in a PI type II controller with low time constant (T_p) that is used for attenuating high frequency components (noise). PI type II controller should be chosen if the plant also presents low attenuation at high frequencies. However, PI type I controller is simpler in construction than a PI type II controller. Also, for a cascaded system, where more than one controller

is used, PI type I is easier to implement in the system than PI type II controller. So PI type I controller is the preferred controller here.

4.6.1 First Case – Phase Margin 45°:

The design specifications for the controllers are: Phase margin = 45° at f_x =24 Hz,

The transfer function of a PI type I controller is,

$$G_c(s) = \frac{K_p(1+s\tau)}{s\tau}, \quad (G_c(s) = K_p + \frac{K_i}{s}). \text{ And } \tau = \frac{K_p}{K_i} \tag{4.18}$$

$$\angle G_c(j\omega_x) = \tan^{-1}\left(\frac{-1}{\omega_x \tau}\right) \tag{4.19}$$

The phase angle of the controller is -14.75°. So, from equation 4.19, the value of τ = 0.02515 sec at ω_x = 151. The gain of the controller has to be the inverse of the plant at the crossover frequency so that the gain of the compensated (with the controller) loop transfer function equals to 1 or 0 dB at that frequency.

$$\text{Compensated LTF } (j\omega_x) = G_c(j\omega_x)*G_1(j\omega_x)*G_2(j\omega_x)*G_3(j\omega_x) = 1 \tag{4.20}$$

$$20 \log | G_c(j\omega_x) | + 20 \log | G_1(j\omega_x)\, G_2(j\omega_x) G_3(j\omega_x) | = 0 \text{ dB} \tag{4.21}$$

Gain of the controller in dB at ω_x = -Gain of the open loop TF in dB at ω_x

$$20 \log | G_c(j\omega_x) | = - 20 \log | G_1(j\omega_x)\, G_2(j\omega_x) G_3(j\omega_x) | \tag{4.22}$$

$$20 \log | G_c(j\omega_x) | = 2.861 \text{ dB}, \quad | G_c(j\omega_x) | = 1.39 \tag{4.23}$$

$$|G_c(j\omega_x)| = \frac{K_p}{\omega_x \tau}\sqrt{(\omega_x \tau)^2 + 1} \text{ (From equation 4.18)} \tag{4.24}$$

$$K_p = \frac{1.39*151*0.02515}{\sqrt{(151*0.02515)^2 + 1}} = 1.344 \tag{4.25}$$

$$\text{Again, } \tau = \frac{K_p}{K_i}, \text{ and } K_i = \frac{K_p}{\tau} = 53.44$$

So the transfer function of the controller (Putting K_p = 1.344, τ = 0.02515 in to equation 4.18)

$$G_c(s) = \frac{1.344(1 + s0.02515)}{s0.02515} = \frac{1.344 + s0.0338}{s0.02515} \tag{4.26}$$

Compensated-loop transfer function of the system, $G_{cp} = G_c(s)*G_p(s)$:

$$G_{cp} = \frac{1.946e-7*s^4 + 0.02327*s^3 + 2.118*s^2 + 6.285e4*s + 2.497e6}{2.006e-15*s^7 + 3.686e-10*s^6 + 4.638e-7*s^5 + 0.001435*s^4 + 1.563*s^3 + 400.3*s^2 + 2780*s} \tag{4.27}$$

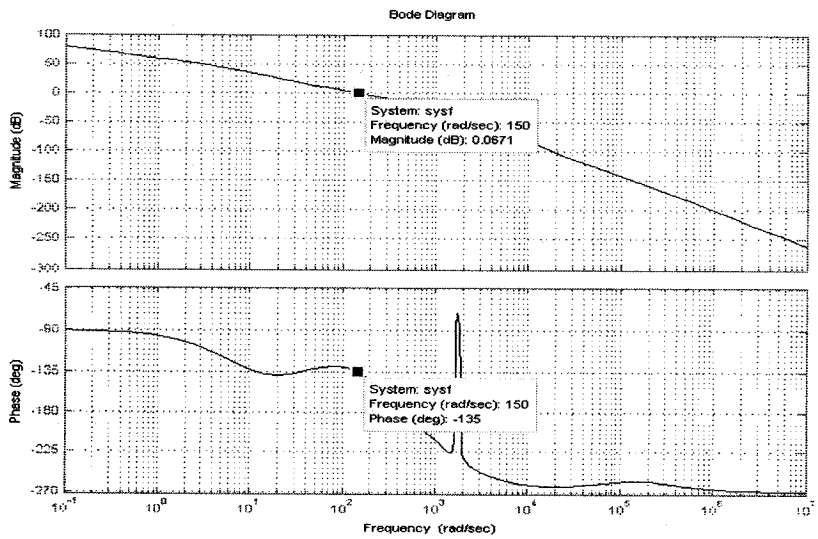

Figure 4.8: Bode plot of the PI Type I open-loop control system

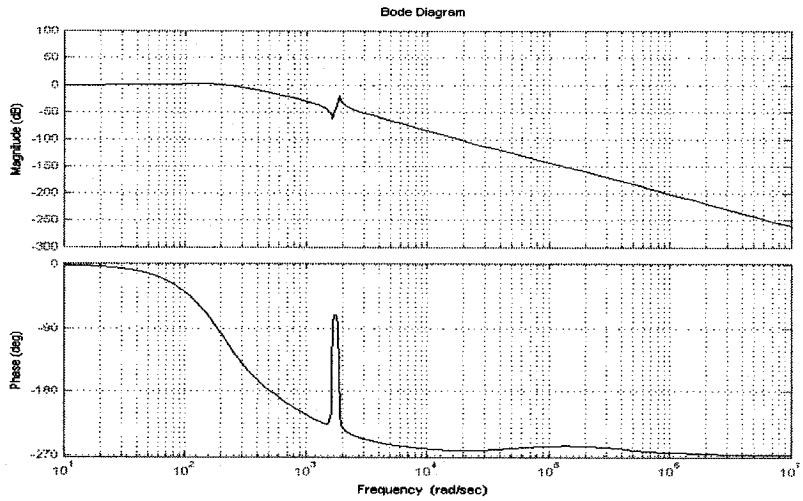

Figure 4.9: Bode plot of the PI Type I closed-loop control system

Using MATLAB program, Figures 4.8, and 4.9 are plotted. The MATLAB commands are given in Appendix C. From the Bode plot of the open-loop system (Figure 4.8), it is found that the gain of the compensated-loop transfer function is equal to zero and gain margin is 45° at the cross-over frequency. In addition, in a closed-loop system gain is 1 or 0 dB in the low frequency range where $|G_c(j\omega_x)G_p(j\omega_x)| =>>1$ (Figure 4.9).

4.6.2 Second Case – Phase Margin 50°:

The design specifications for the controllers are: Phase margin = 50° at f_x = 24 Hz,

The controller has to introduce a phase lag of -9.75° ($\angle G_c(\omega_x)$ = PM-180°-$\angle G_p(\omega_x)$ = 50°-180°-59.75° = -189.75°).

τ =0.0385 sec at ω_x = 151 (From equation 4.19)

Using similar procedure,

$$K_p = \frac{1.39*151*0.0385}{\sqrt{(151*0.0385)^2+1}} = 1.3698 \quad (4.28)$$

$$K_i = \frac{K_p}{\tau} = 35.58 \quad (4.29)$$

$$G_c(s) = \frac{1.3698(1+s0.0385)}{s0.0385} = \frac{1.3698+s0.0527}{s0.0385} \text{ , from equation 4.18} \quad (4.30)$$

4.6.3 Third Case – Phase Margin 55°:

The design specifications for the controllers are: Phase margin = 55° at f_x = 24 Hz,

The controller has to introduce a phase lag of -4.75° ($\angle G_c(\omega_x)$ = PM-180°-$\angle G_p(\omega_x)$ = 55°-180°-59.75° = -184.75°).

τ =0.0797 sec at ω_x = 151 (From equation 4.19)

Using similar procedure,

$$K_p = \frac{1.39*151*0.0797}{\sqrt{(151*0.0797)^2+1}} = 1.385 \quad (4.31)$$

$$K_i = \frac{K_p}{\tau} = 17.38 \quad (4.32)$$

$$G_c(s) = \frac{1.385(1+s0.0797)}{s0.0797} = \frac{1.3698+s0.1103}{s0.0797} \text{ , from equation 4.18} \quad (4.33)$$

4.6.4 Step Response of the controller:

Next, with these selected PI values the response of the measured current is observed using EMTP. A -0.1 pu step change for 2.2 s is applied to the rectifier current order to see the response of the measured current. Figure 4.10 shows the step response of the measured current for the three sets of PI parameters. From the figure it is observed that the overshoot is lower for K_p = 1.385 and K_i = 17.38. The system is stable for the three sets of PI values.

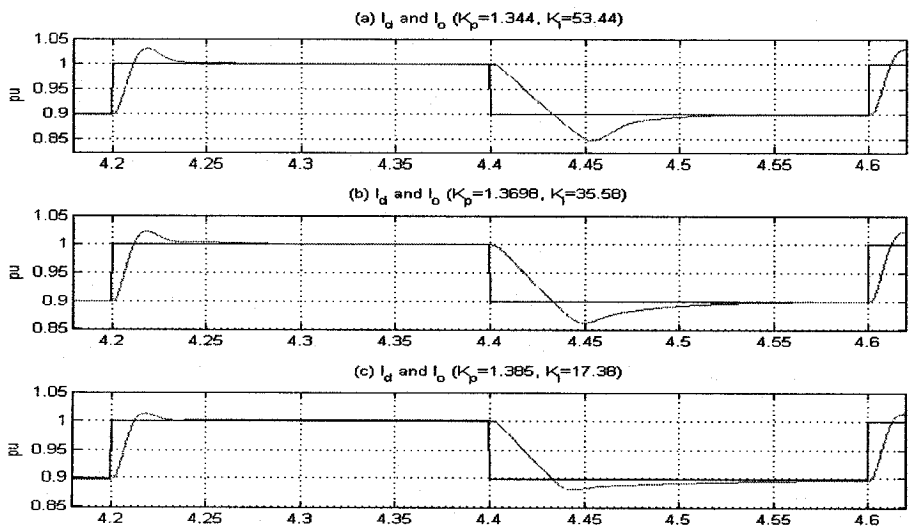

Figure 4.10: Step change in current order for different PI values

4.7 Summary:

Two methods, for designing the controller were presented here. Theoretical calculations for both the methods were briefly explained. If a performance comparison of the PI parameters of these two methods is made, it is found (From Figures 4.5 and 4.10) that the

value of K_p and K_i are close to each other. Therefore, both methods can be used for the controller design.

Chapter 5

VERIFICATION OF THE OPERATIONAL CHARACTERISTICS

5.1 Introduction:

This chapter deals with the operational characteristics and their comparison for both the hybrid diode-thyristor rectifier model (proposed model) and the 12-pulse thyristor rectifier model (standard model). Two operational characteristics are discussed in this chapter:

- Static characteristics, and
- Dynamic characteristics

5.2 Assumptions:

The following assumptions have been made while comparing the static and dynamic characteristics of both models:

- Only the rectifier side of the DC system is considered.
- Both systems deliver same amount of power to the load.
- AC source is identical for both models.

- Bridge two (Y- Delta connection) is identical for both cases.
- Identical current controller unit is used for both cases.
- Identical AC and DC filtering units are used for both cases.
- Identical converter transformer unit is used for both cases.

5.3 Static Characteristics:

For assessment of the static characteristics, the following parameters are monitored (a) valve voltages, (b) valve currents, (c) AC input currents, (d) AC source currents, (e) DC output current and voltage, (f) AC active and reactive power, and (g) harmonic content of the voltages and currents.

5.3.1 Valve voltages:

Standard Model: (Figure 5.1)

The shapes of the valve voltages (Figure 5.1) for both the upper and the lower bridges are identical. The lower bridge is connected with a Y-Y connected transformer and the upper bridge with a Y-Δ connected transformer. Therefore, the phase difference between the two transformers is ideally 30°. From the result, the delay between the two valve voltages is found to be 29.8°, the phase difference between the two transformers due to the connection of the transformers with the bridges. The firing angle of the system is calculated from the valve voltages and the value is 18.36°. The rate of rise of voltage

(dv/dt) can be calculated from the valve voltages. The dv/dt for the lower bridge is 102.8 V/μs, and the upper bridge is 102.0 V/μs which is an acceptable range for both bridges.

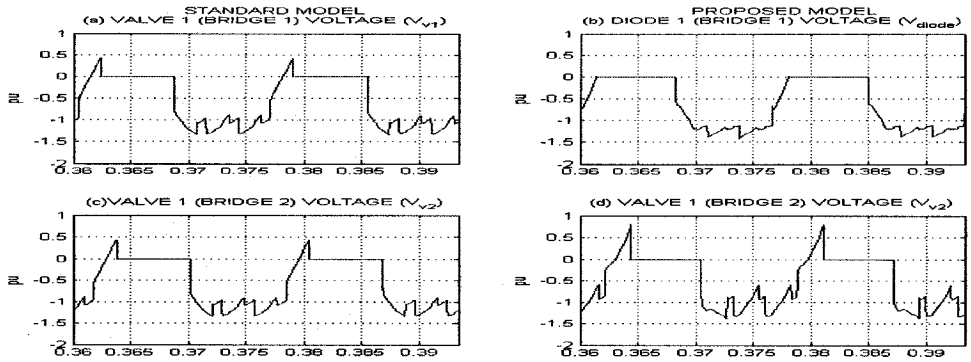

Figure 5.1: Valve voltages of both models

Proposed (hybrid diode-thyristor rectifier) model: (Figure 5.1)

The upper thyristor-bridge, connected with a Y-Δ transformer, is similar with the standard model. The lower diode-bridge is connected with a Y-Y transformer. The valve voltages (Figure 5.1) of the upper thyristor-bridge and the lower diode-bridge are not similar and because of the transformer connection time delay is present between the two valve voltages. As the diode-bridge is operating at $\alpha = 0°$, the thyristor-bridge will need to operate at a higher angle to maintain the same current as the case of the standard model. The firing angle of the upper thyristor bridge is 29.6°. The phase difference between the thyristor-bridge and the diode-bridge is found to be 35.8°. The dv/dt of the diode-bridge is 112.2 V/μs and the thyristor-bridge is 97.4 V/μs which is close to the standard model.

Summary:

The firing angle is found 29.6° for the proposed model and 18.4° for the standard model. The notches and the wave shapes of the valve voltages for the proposed model are different from the standard model because of two different bridges used for the hybrid option.

5.3.2 Valve Currents:

Standard model: (Figure 5.2)

The valve currents of the two bridges are identical but a small phase difference (30°) is present because of the connection of the transformer with two bridges. The rate of rise of current (di/dt) of the lower bridge is 1.7 A/μs and the upper bridge is 1.8 A/μs, which are acceptable for the bridges. The overlap angle is 19.0° for both the lower and the upper bridges.

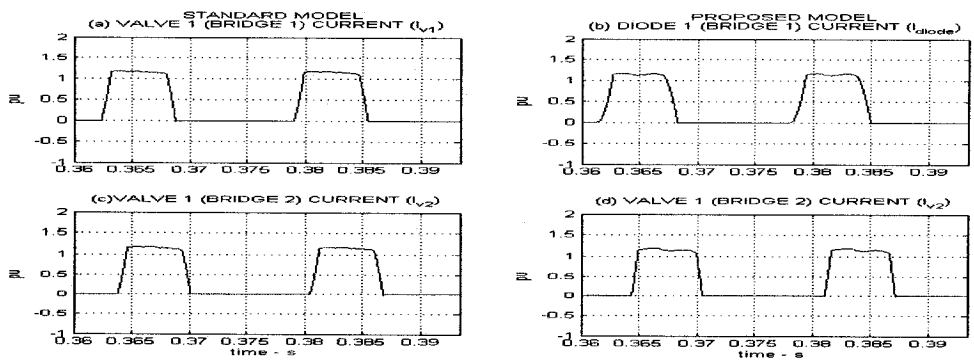

Figure 5.2: Valve currents of both models

Proposed Model: (Figure 5.2)

The di/dt of the lower diode bridge is 1.1 A/μs and overlap angle 28.5°. The di/dt of the upper thyristor bridge is 2.5 A/μs and overlap angle 14.7°.

Summary:

It can be concluded that the notches of the valve currents in the diode-bridge of the proposed model are not the same with the thyristor-bridge of the standard model and notches are same in the thyristor-bridges for both models. The di/dt value is higher in the thyristor-bridge of the proposed model.

5.3.3 AC Input Current (Harmonic Analysis):

Standard Model: (Figure 5.3 and 5.4)

The value of the three fundamental phase currents (peak values and simulation runs from 0.36 s to 0.39334 s) are I_a = 3300.79 A, I_b = 3302.02 A, and I_c = 3305.55 A and the harmonics are 11^{th} (164.33 A), 13^{th} (114.54 A) and 23^{rd} (21.76 A). So a tuned filter for 11^{th} harmonic and high pass filter for 13^{th} harmonic are needed. Figure 5.3 shows the AC input current waveforms of both models.

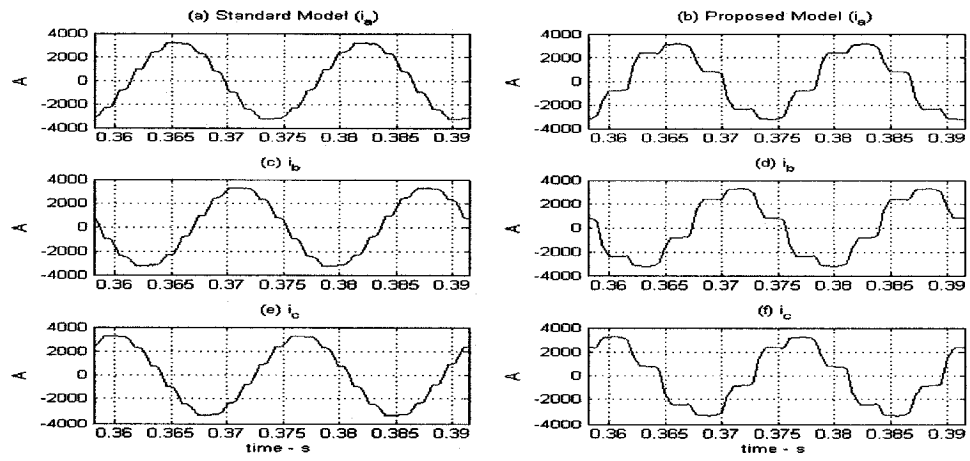

Figure 5.3 AC input current

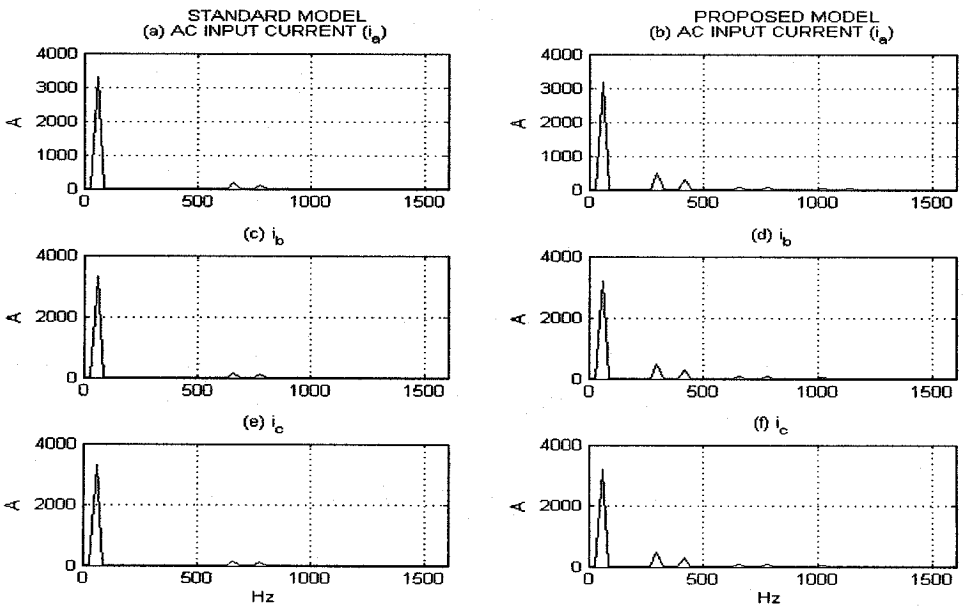

Figure 5.4: FFT of Input AC Current of both models

Proposed Model: (Figure 5.3 and 5.4)

The fundamental phase currents (peak values) are found to be I_a =3188.37 A, I_b =3188.21 A, and I_c = 3190.46 A. The harmonics are seen as 5^{th} (489.34 A), 7^{th} (313.86 A), 11^{th}

(86.09 A), 13th (77.64 A), 17th (50.74 A), 19th (33.41 A), 23rd (29.39 A), and 25th (22.36 A). Three tuned filters for 5th, 7th, and 11th harmonics and high pass filter for 13th and higher order harmonics are needed.

Table 5.1: AC Input Current

Frequency (Hz)		Standard Model (A)	Proposed Model (A)
i_a	60	3300.79	3188.37
	300 (5th)	-	489.34
	420 (7th)	-	313.86
	660 (11th)	164.33	86.09
	780 (13th)	112.33	77.45
	1020 (17th)	-	50.55
	1140 (19th)	-	33.07
	1380 (23rd)	21.46	29.39
	1500 (25th)	-	22.26
i_b	60	3302.02	3188.21
	300 (5th)	-	488.66
	420 (7th)	-	313.43
	660 (11th)	163.47	85.69
	780 (13th)	112.06	76.94
	1020 (17th)	-	50.74
	1140 (19th)	-	33.26
	1380 (23rd)	21.76	29.31
	1500 (25th)	-	22.36
i_c	60	3305.55	3190.46
	300 (5th)	-	488.11
	420 (7th)	-	313.80
	660 (11th)	162.81	85.34
	780 (13th)	114.54	77.64
	1020 (17th)	-	50.23
	1140 (19th)	-	33.41
	1380 (23rd)	20.71	29.02
	1500 (25th)	-	22.34

Summary:

From the harmonic analysis (Table 5.1), it is found that the proposed model contains some lower order harmonics (5^{th}, 7^{th} and so on). So it is necessary to remove these harmonics from the proposed model. To remove these harmonics, AC filters are designed in chapter 3. So, the overall cost of the proposed model will be increased to remove these harmonics.

5.3.4 AC Source Current (Harmonic Analysis):

Standard Model: (Figure 5.5 and 5.6)

The fundamental phase currents (peak values) are I_{sa}= 2925.81 A, I_{sb}= 2930.01 A, and I_{sc}= 2931.10 A. Figure 5.5 shows the AC source currents of both models.

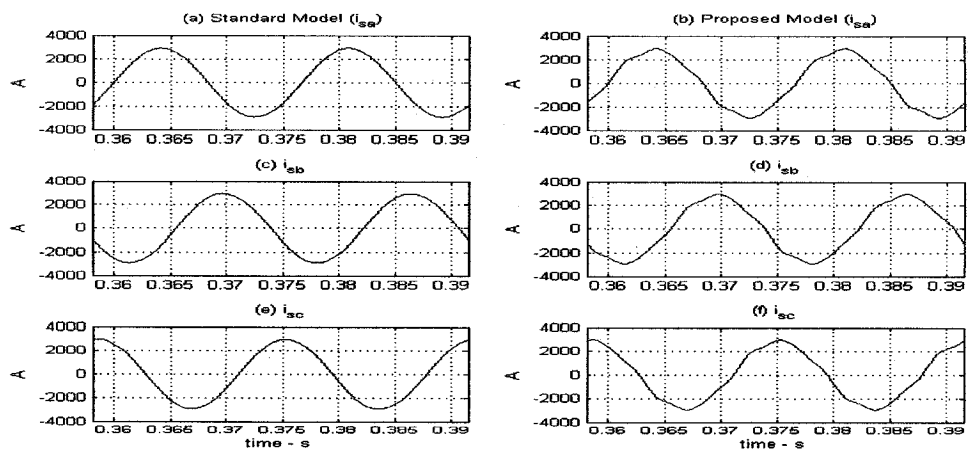

Figure 5.5 AC source current

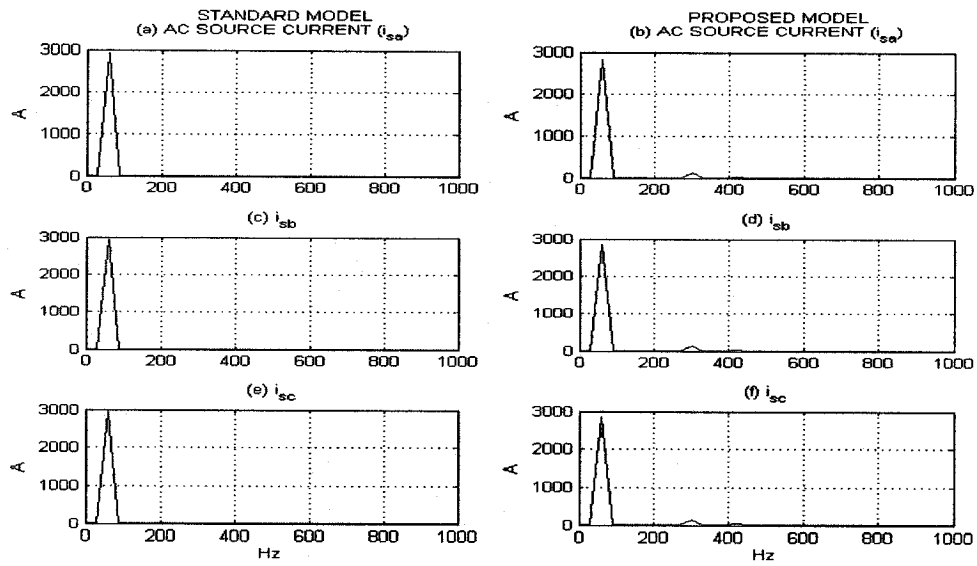

Figure 5.6: FFT of AC Source Current of both models

Proposed Model: (Figure 5.5 and 5.6)

The fundamental phase currents (peak values) are seen as I_{sa} = 2853.84 A, I_{sb} = 2854.36 A, and I_{sc}= 2855.75 A. The harmonics are 5th (144.71 A) and 7th (34.44 A). The input source current is not purely sinusoidal because of the presence of these unwanted harmonics.

Table 5.2: AC Source Current

Frequency (Hz)		Standard Model (A)	Proposed Model (A)
i_{sa}	60	2925.81	2853.84
	300 (5th)	-	143.62
	420 (7th)	-	34.14
i_{sb}	60	2930.01	2854.36
	300 (5th)	-	144.71
	420 (7th)	-	33.75
i_{sc}	60	2931.10	2855.75
	300 (5th)	-	143.75
	420 (7th)	-	34.44

Summary:

Comparing with the standard model, the source input current of the proposed model contains 5^{th} and 7^{th} harmonics (Table 5.2). Therefore, these harmonics need to be eliminated by adding filters and filters are redesigned for the proposed model in chapter 3.

5.3.5 DC Output Current, Voltage, DC, & AC Power:

Standard Model: (Figure 5.7)

The steady state analysis of the standard model shows that the DC output current ripple is very low. The (rms) value of the DC side output current is 1600.62 *A* and the average value of the DC side current is 1597.88 *A*. Similarly, very small ripple in the DC output voltage is found. The DC output voltage is 454.73 kV and the average value is 456.54 kV. Average AC input power is, P_{AC} = 665.6 MW, average DC output power is, P_{DC} = 620.3 MW, and average reactive power is Q_{AC} = 352.4 Mvar.

Harmonic Analysis: (Figure 5.8)

The fundamental DC output current is 2680.40 A (peak) and no other harmonics (Table 5.3) are present. FFT of the output current in steady state analysis (simulation period from 0.36 s to 0.39334 s) shows that the fundamental DC output current 3200.49 A. The fundamental DC output voltage is 912.63 kV with no harmonics. From the steady state

analysis, the fundamental DC output voltage is found as 915.91 kV with very small 24th harmonic (4.68 kV).

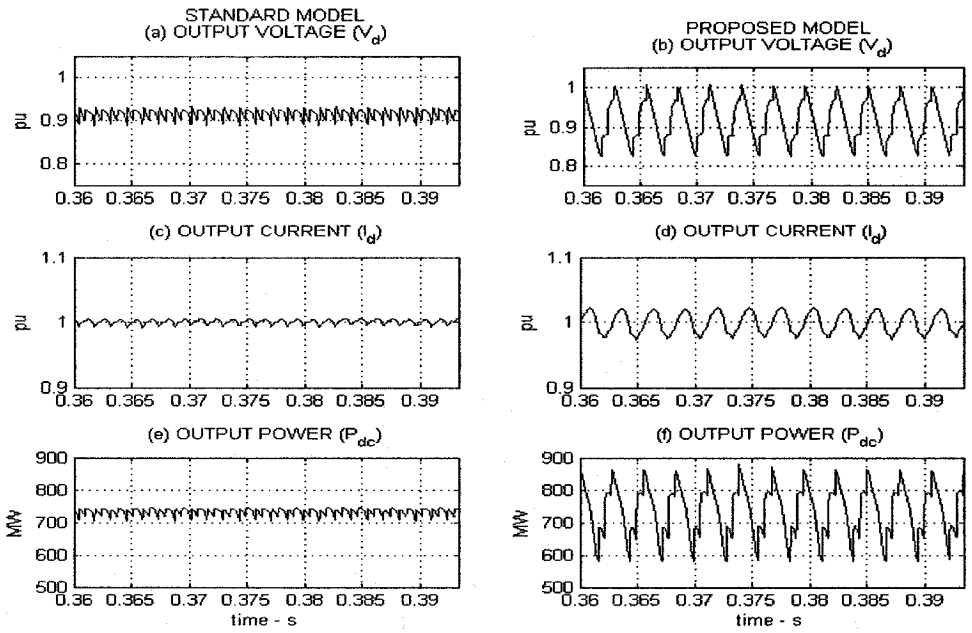

Figure 5.7: Output Voltage, Current & Power of both models

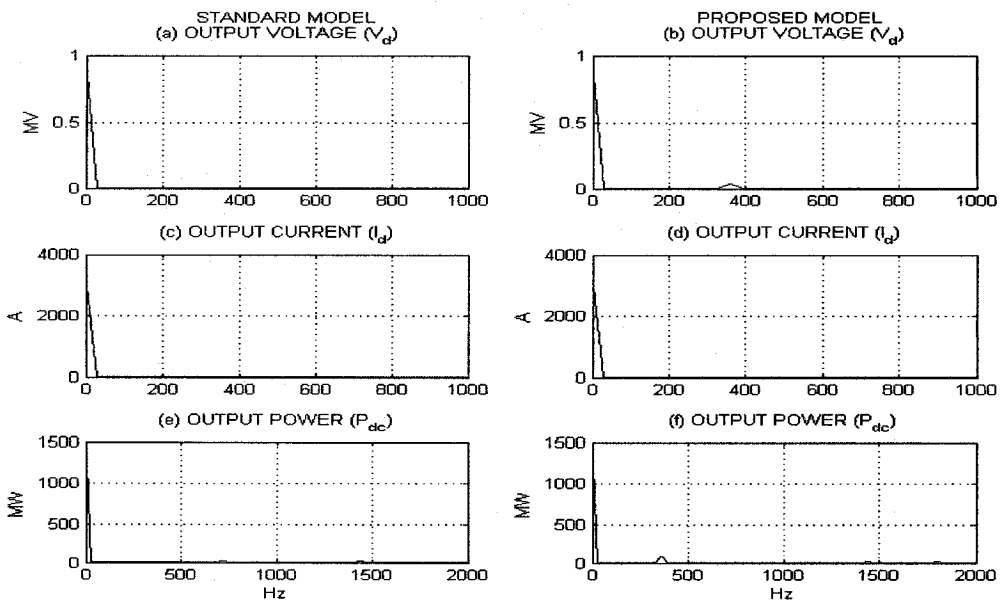

Figure 5.8: FFT of Output Voltage, Current, and Power of both models

Proposed Model: (Figure 5.7)

In the steady state analysis, the DC output current contains high ripple content because of the presence of 6^{th} harmonic. But using the redesigned filters for the proposed model the 6^{th} harmonic current is reduced like the standard model. The DC output current is 1603.4 A. The DC output voltage is 460.9 kV and the average of the two peak DC output voltages is 459.6 kV. The average AC active power, P_{AC} = 651.8 MW, average DC power, P_{DC} = 625.8 MW, and average reactive power is, Q_{AC} = 338.4 Mvar.

Harmonic Analysis: (Figure 5.8)

The fundamental DC output current is 2704.94 A (peak) and it consists of 6^{th} (37.87 A) harmonic. Fundamental DC Output voltage is 912.72 kV (peak) and the value of 6^{th} harmonic is 36.5 kV. From the FFT of the steady state analysis (Simulation period from 0.36 s to 0.39334 s), the fundamental DC output current is found 3201.43 A and 6^{th} harmonic is 34.15 A. The fundamental DC output voltage is 916.02 kV and 6^{th} harmonic (35.53 kV), 24^{th} harmonic (3.48 kV), and 30^{th} harmonic (4.58 kV) are found. To remove these harmonics high pass filter (6^{th} harmonic and above) was designed for the proposed model (Appendix A).

Table 5.3: Output Current & Voltage

Frequency (Hz)		Standard Model	Proposed Model
i_d (A)	Fundamental	3200.49	3201.43
	360 (6^{th})	-	34.15
v_d (kV)	Fundamental	915.91	916.02
	360 (6^{th})	-	35.53
	1440 (24^{th})	4.68	3.48
	1800 (30^{th})	-	4.58

Summary:

From the DC output voltage and current (steady state analysis) of the two models, it is found that the proposed model contains much more ripple than the standard model. From the harmonic analysis it is also found that the proposed model DC output voltage and current (Table 5.3) contains 6^{th} harmonic which is not present in the standard model. This is the main difference between the output current and voltage of the two models. Because of this 6^{th} and other harmonics, the DC output current and voltage have more ripples in the proposed model than the standard model. The value of the AC active and reactive power and DC power for both the models are very close to each other.

5.4 Dynamic Characteristics:

To verify the operation of the two models, the following different dynamic tests were performed:

- Application of step change in current order (I_o),
- Application of Voltage Dependent Current Limit (VDCL),

- Application of 1 phase fault at AC bus of rectifier,
- Application of 3 phase fault at AC bus of rectifier,
- Application of DC line fault,
- Application of Block / Deblock of rectifier firing pulses, and
- Application of Misfire (Commutation failure)

5.4.1 Step Change in Current Order (I_o):

A -20% step change in current order (I_o) is applied to its nominal current reference of 1.0 pu for 0.2 s after the system has reached steady state at 0.2 s to test the performance of the current controller at the rectifier end. The signals shown are (a) DC voltage (V_d), (b) DC current (I_d) and current order (I_o), (c) AC voltages (V_{ac}), (d) alpha order, (e) AC active power (P_{ac}) and (f) reactive power (Q_{ac}).

Standard model: (Figure 5.9)

The super-imposed waveforms of DC current I_d and current order I_o shows that the DC current follows the ordered value of current and the magnitude of current is 0.8 pu in the step change region. The value of the current is 1.0 pu after the step change region at 0.4 s. Output DC voltage remains constant in the step change region but a small decrease in the starting of the step change and a small increase at the end of step change is noticed. The AC bus voltages remain practically unaffected but there is a small increase in the application region of the step change due to the reactive power demand of the bridges.

The valve voltage signal shows clearly the firing angle alpha as the step change is applied. The value of alpha is transiently changed from about 17.92° to about 26.13° in the application region of the step change and settles to 17.92° at the end of the step change. During the transition period, the AC active power reduces because of the effect of the firing angle and again settles to the original value after the step change is removed. As a result, the source reference current is also reduced in the application region of the step change. Reactive power drawn remains practically the same but reduces a little in the application region of the step change as the increase in firing angle compensates for the drop in current magnitude and two small notches are found in the starting and ending of the step change region. The valve current follows the step changes like the current order I_o.

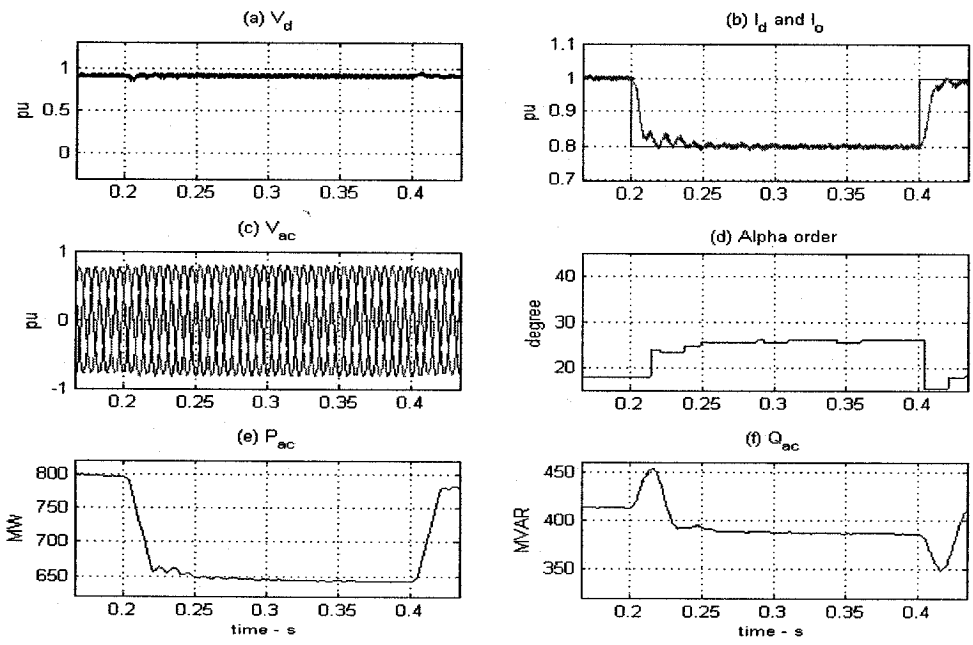

Figure 5.9: 20% Step Change in Current Order for Standard Model

Proposed (hybrid diode-thyristor bridge) model: (Figure 5.10)

The DC current I_d follows the current order in a similar way as the standard model. The behavior of the DC output voltage and the AC bus voltage is the same as the standard model. The value of alpha is transiently changed from 27.86° to 43.41° and this change can be observed from the valve voltages. After the step change is removed, the alpha settles down to 28.29°. The behavior of the AC active power and reactive power is similar with the standard model, as the diode-bridge in the proposed model does not affect the step change characteristics. The valve current follows the ordered current I_o.

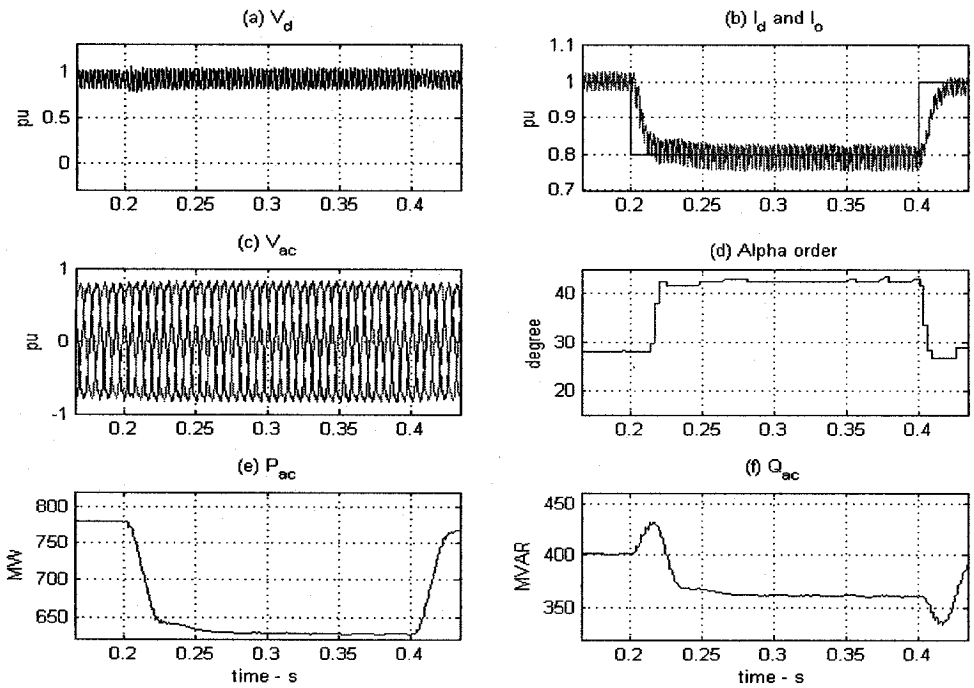

Figure 5.10: 20% Step Change in Current Order for Proposed Model

Differences:

The step changes are well controlled for both models. However, the DC voltage and the DC current contain more ripples in the proposed model than the standard model. From the harmonic analysis, it is found that the DC voltage and DC current have 6^{th} harmonic in the proposed model. The alpha value is changed from 17.92° to 26.13° for the standard model and from 27.86° to 43.41° for the proposed model in the application region of the step change. The rest of the characteristics of the proposed model are the same as the standard model.

5.4.2 Voltage Dependent Current Limit (VDCL):

A DC line fault or an AC fault on the inverter end could dip the DC voltage to a value, which could be very low or zero. The current under these conditions would still be maintained due to the rectifier current controller. The operation of the system with high DC current and low DC voltage could result in higher power losses and higher reactive power demand and could lead to voltage instability. To avoid this problem, the current reference signal provided to the controllers should be a function of the DC voltage. A VDCL limits the current reference value for the rectifier controller based upon the level of the DC voltage. This test verifies the operation of the VDCL unit. At 0.2 s, the VDCL operation is introduced for 0.1 s and the current order is reduced to 0.2 pu. The VDCL block is provided in Appendix D.

Standard Model: (Figure 5.11)

The measured DC current (I_d) follows the current order and settles down to 0.2 pu. When the ramp is released at 0.4 s, the DC current faithfully follows the I_{order} signal. The DC voltage is little bit distorted in the ramp of the current order. The AC voltages indicate a similar behavior due to the active/reactive power demand of the bridges. The alpha value is increased to 41.7° and the valve voltage shows clearly that the firing angle increases to reduce the current to 0.2 pu. The valve current is also reduced to very small value. The controller behavior is stable.

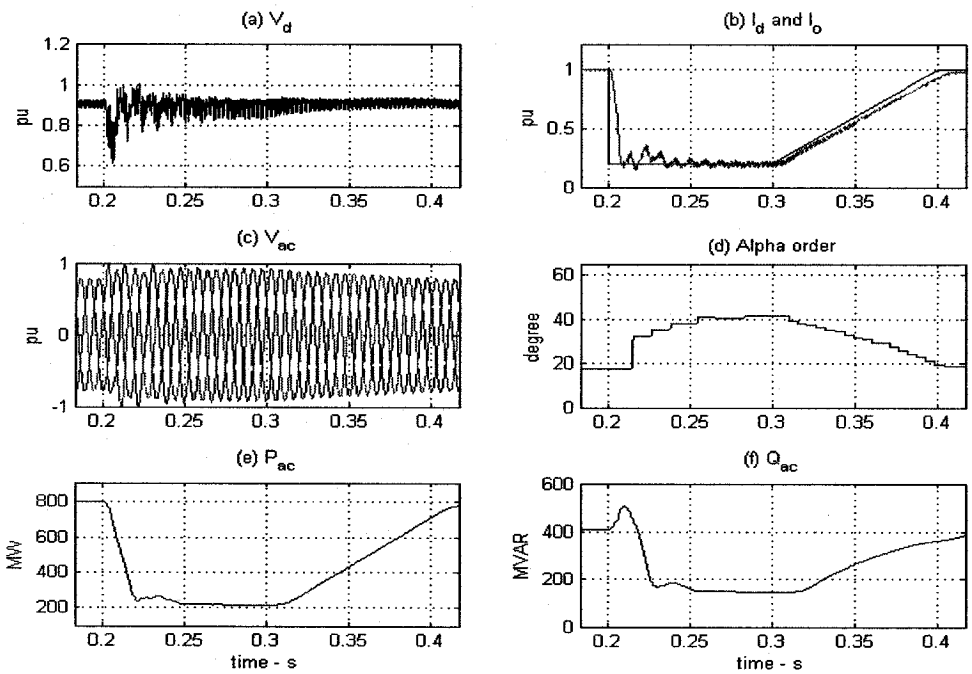

Figure 5.11: Standard Model with VDCL block

Proposed (hybrid diode-thyristor bridge) Model: (Figure 5.12)

The DC current follows exactly the same way as the current order flows. The DC voltage, AC active and reactive power is similar to the standard model. The alpha value increases to 58.1° and is clearly visible from the valve voltage. The valve current is reduced to zero in that region.

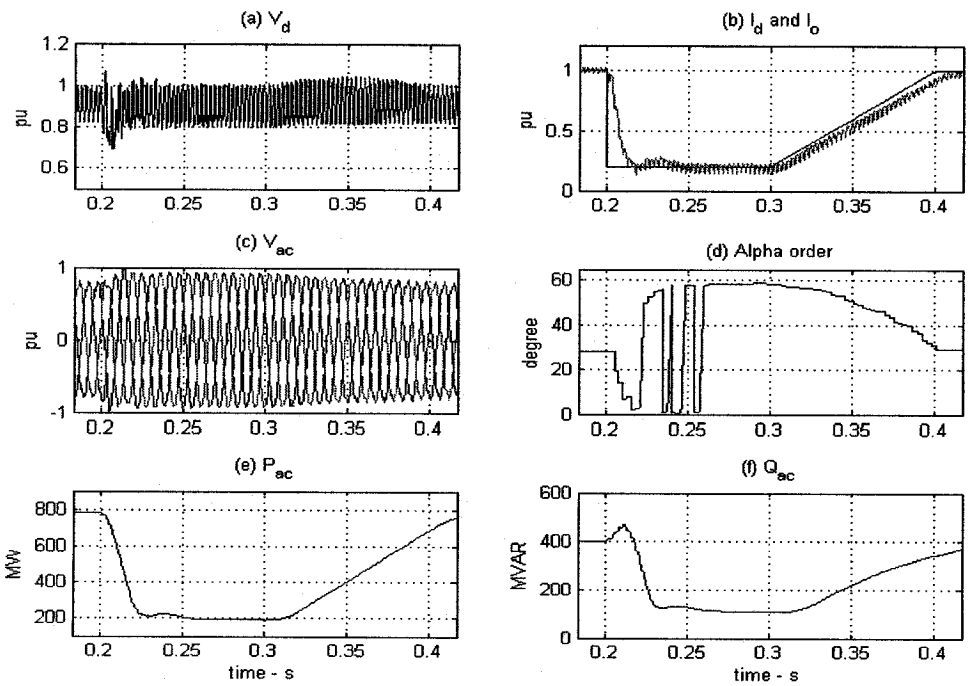

Figure 5.12: Proposed Model with VDCL block

Differences:

There is a small difference in performance between these two models. In the standard model, the alpha value is increased to 41.7° and in the proposed model, the value remains at 58.1° due to the increased alpha value requirement for that system.

5.4.3 1-Phase AC Bus Fault:

This test is performed by using a signal generator block in EMTP. With this signal generator a fault signal is sent to the system. The width of the fault is selected as 0.1s and starts after the system is in steady state i.e. at 0.2 s. The single-phase fault is introduced in phase A. The controlled switch is grounded with a resistance of 1 Ω and an inductance of 205 mH. The value of the resistance and inductance is so chosen that the bus voltage be reduced to 30%. This test shows the control behavior during an unbalanced fault on the AC bus through high impedance. This causes a mode shift in the controller to operate on alpha-minimum mode during the fault in the period of 0.2 to 0.3 s.

Standard Model: (Figure 5.13)

The DC current during the fault period displays the presence of a second harmonic current (100.4 A) which is a typical characteristic of such faults. The DC voltage also displays the second order harmonic voltage (27.14 kV). A single-phase fault in phase A also affects the input currents and voltages of the other two phases (B & C). Furthermore, the control dynamics going into the fault and coming out of the fault are clearly different and observable. The controller behavior is stable throughout the period. The alpha value is decreased to 4.96° when the fault is applied i.e. it works in alpha minimum mode and again the alpha value reaches its original value (17.9°) at 0.35 s. During the application of the fault AC power decreases as the alpha value changes like a notch in the starting and ending period of the fault. Reactive power increases during the fault region and again

returns to its original value after the removal of the fault. The valve currents, valve voltages are reduced and distorted in the fault region as the alpha value is reduced.

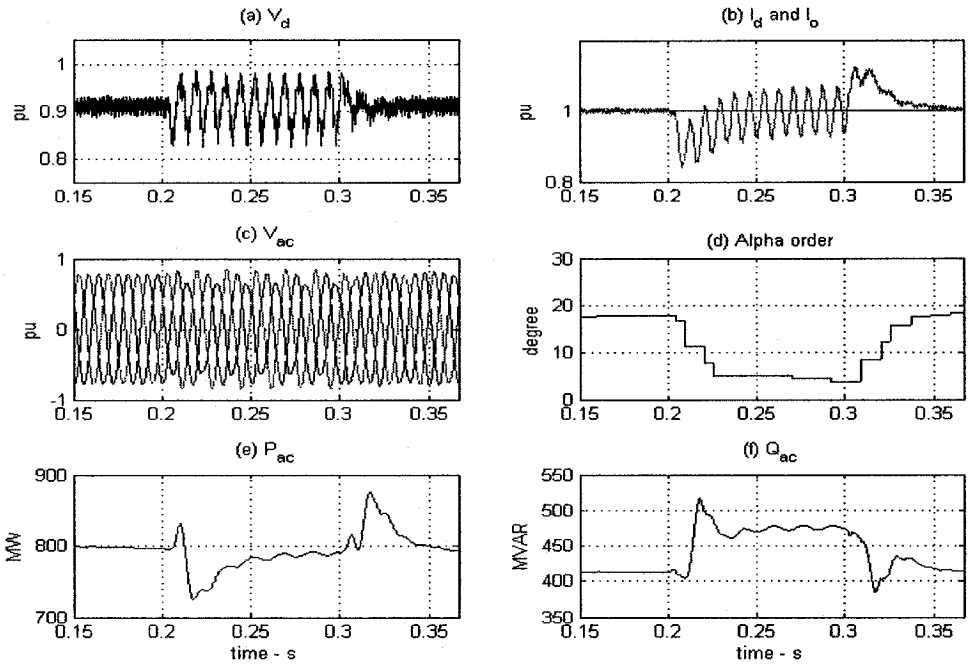

Figure 5.13: 1-phase fault of the Standard Model

Proposed (hybrid diode-thyristor rectifier) Model: (Figure 5.14)

The second order harmonic current and voltage are 105.9 A and 28.5 kV respectively, which is the unwanted feature of this fault. The input voltages and currents of all the three phases are affected because of this single-phase fault. The alpha value is reduced to 10.58° and suddenly it reduces to 4.53° for some moments during the fault period and regains its original value (27.8°) at 0.367 s after the fault is removed. The effect in AC active and reactive power, valve voltages, and currents is the same as the standard model.

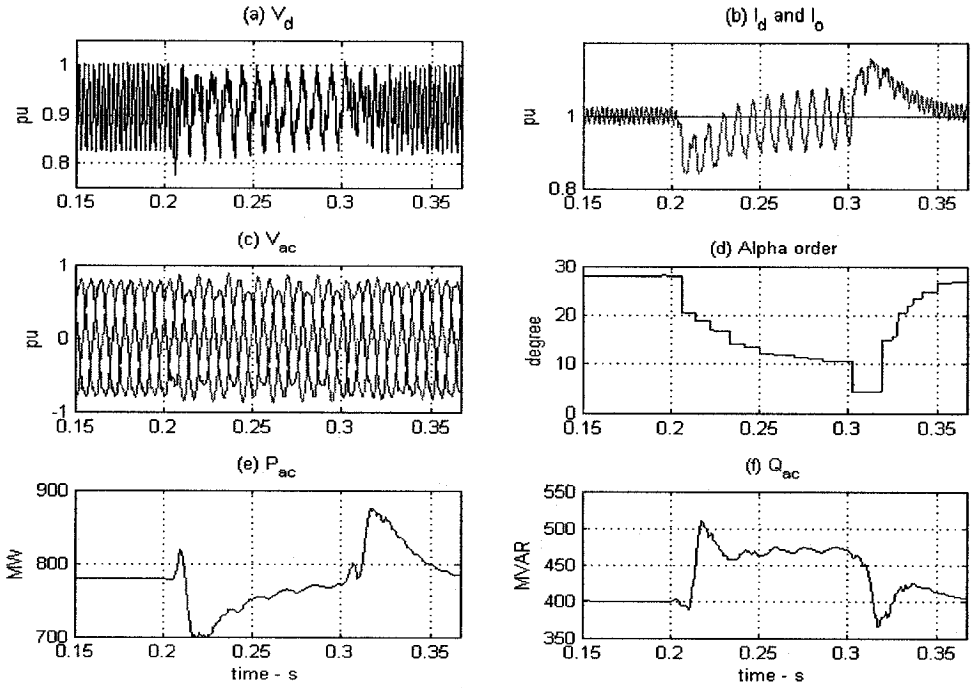

Figure 5.14: 1-phase fault of the Proposed Model

Difference:

The alpha minimum mode operation is clearly visible from the valve voltage signal. The value of alpha in the fault region is reduced to 4.96° for standard model and 10.58° for the proposed model and it takes more time (0.017 s) to return to the original alpha values for the proposed model than the standard model.

5.4.4 3-Phase AC Bus Fault (1pu):

A signal generator is used for introducing a three-phase fault of 1 pu amplitude in to the system. The fault starts at 0.2 s for 0.1 s. The controlled switch is grounded with a resistance of 1 Ω.

Standard Model: (Figure 5.15)

The output current reduces close to zero during the fault period due to the lack of the driving current source voltage. Output voltage remains fixed but distorted in the fault region and increases abruptly as the fault is cleared. The significant feature of this fault is the recovery period. Absence of the driving AC voltage at the rectifier prevents current from recovering at 0.3 s after the fault is cleared. It takes a long time (0.36 s) to recover from the fault. Input voltage is reduced to zero in the fault period. Input current is distorted and increases up to 20 kA. When the fault is cleared, the in-rush current in the converter transformers is large and causes distortion in the bus voltages and large over-voltages greater than 2 pu to appear; this is a reflection of the strength (SCR) of the AC system. Alpha value is reduced to zero for the delta-connected converter in the fault region. AC and DC power reduces close to zero in the fault region but right after the fault is cleared, the power is increased to a high value than the actual value. Reactive power is reduced and is suddenly increased for 0.02 s in the fault region then again reached to the original value. The valve voltage is distorted therefore alpha value is not measurable from

the valve voltage. The valve current is reduced to zero in the fault region and it takes a long time (0.35 s) to recover again to the original value.

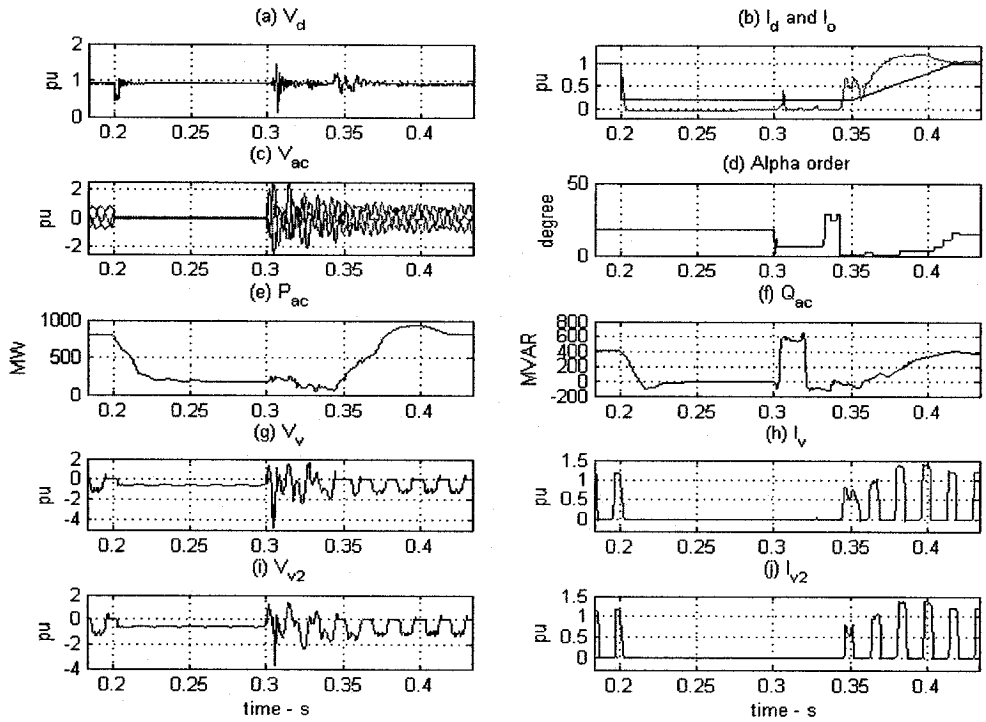

Figure 5.15: 3-Phase fault Standard Model with VDCL

Proposed Model: (Figure 5.16)

The DC voltage and current are affected in the same way as the standard model and the recovery period is very long (0.36 s) like the standard model. Input bus voltage remains close to zero during the fault period and once the fault is cleared, it jumps to greater than 2 pu. Input current is distorted and increases up to 20 kA in the fault region. The alpha value is reduced to zero. AC active and reactive power and DC power is reduced to zero in the fault region as the value of alpha is zero but suddenly the reactive power increases for 0.02 s in the fault region. The valve voltage is distorted and the alpha value cannot be

accurately measured. The valve current remains close to zero in the faulted region and after the fault, the current is not following the current order and it is increased.

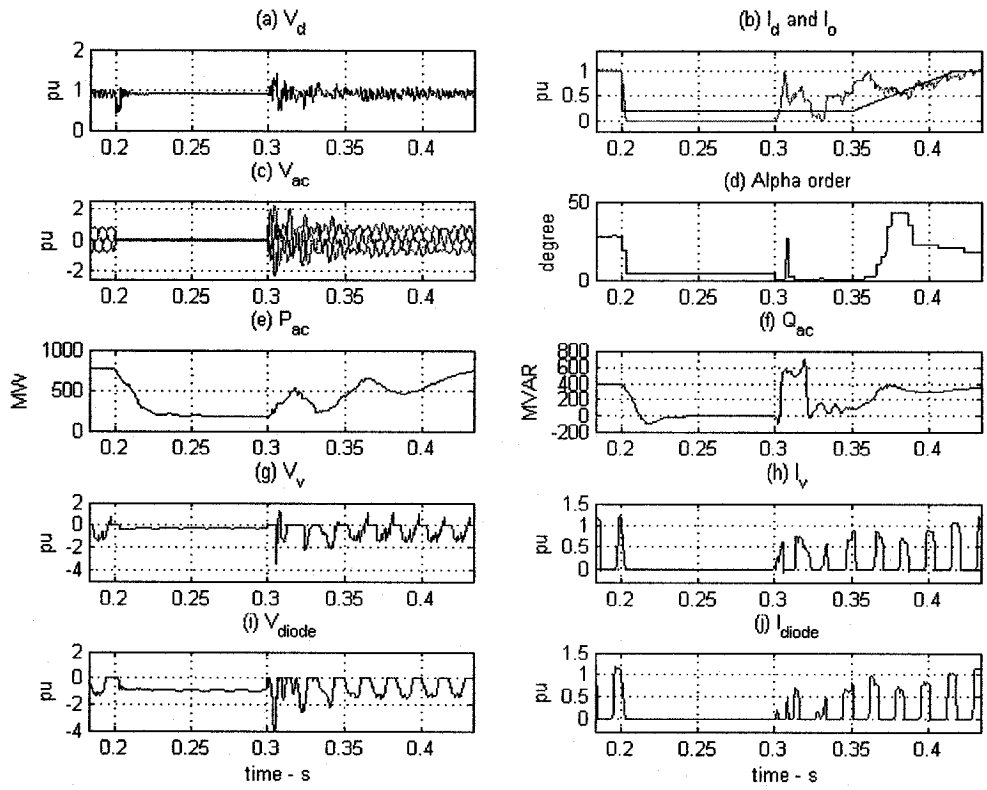

Figure 5.16: 3-Phase fault Proposed Model with VDCL

Differences:

The output current, AC active and reactive power for the proposed model are more distorted than the standard model after the fault is cleared. A VDCL block is used for both the models to improve the performance with this fault application.

Three-Phase AC bus Fault with VDCL Block:

In HVDC transmission systems, a VDCL unit has traditionally been used to generate an adaptive current reference for the converter controller. The Voltage Dependent Current limit (VDCL) protection drops the current order I_O to its minimum value I_{min} =0.2 pu and limits the DC current. Without the VDCL block the DC current is increased to 1.21 pu (for both models) than the actual current (1 pu) after the fault is cleared. VDCL comes into action immediately to bring this fault current to original value to protect the valves from damage. With the help of the VDCL block the AC power (801 MW for the standard model and 780 MW for the proposed model) and alpha value (17.92° for the standard model) are reached to its original value following the signal of the current order. However, in the proposed model the alpha (23°) is still lower than the actual alpha (27.85°) for some times. From the valve voltage waveform, it is also found that the alpha is reached to its original values after the fault is cleared for both models. The valve current is reduced to its original values following the current order after the fault is cleared for both models.

5.4.5 DC Line fault with protection & recovery sequence:

DC fault is the most severe fault for the converter valves at the rectifier end. A signal generator at the DC line side of the rectifier is used to introduce a DC line fault once the system has reached steady state for 0.05 s i.e. at 0.2 s. An impedance of 18.397 Ω and 0.1 μF is used in parallel with the signal generator.

Standard Model: (Figure 5.17)

The DC fault application causes the DC current to shoot up to a value greater than 2.0 pu. A typical peak value of DC current should be around 2.5 pu. The DC fault causes the DC voltage to collapse to zero, and therefore the VDCL protection is applied and the VDCL causes the current to be limited to its I_{min} value. The control action brings the current order to a lower value rapidly. A special action namely Forced Retarded (FR) action has been initiated. Traditionally, to recover from a DC fault, a forced retarded (FR) alpha command is applied to send the rectifier alpha to around 140° i.e. into inverter region, to reduce the DC current to zero and deionized the fault arc. This FR action helps to extinguish the current in the DC line quickly and persists until the DC fault is cleared. The system achieves smooth recovery of voltage and current after the fault is cleared. At 0.3 s, the FR is released and the DC voltage of the DC system picks up causes the VDCL protection to ramp up the current order. The controller then brings up the DC current to its nominal operating point. The AC bus voltages, during the period 0.2 to 0.25 s are distorted due to the sizing of the smoothing reactor. During the fault, the alpha value is distorted and it takes long time to get the original alpha value as follows the current waveform. AC active power reduces and reactive power increases in the faulted region and recover to the original values following the DC current. The valve voltages are distorted and the valve currents reduced to zero in the faulted region.

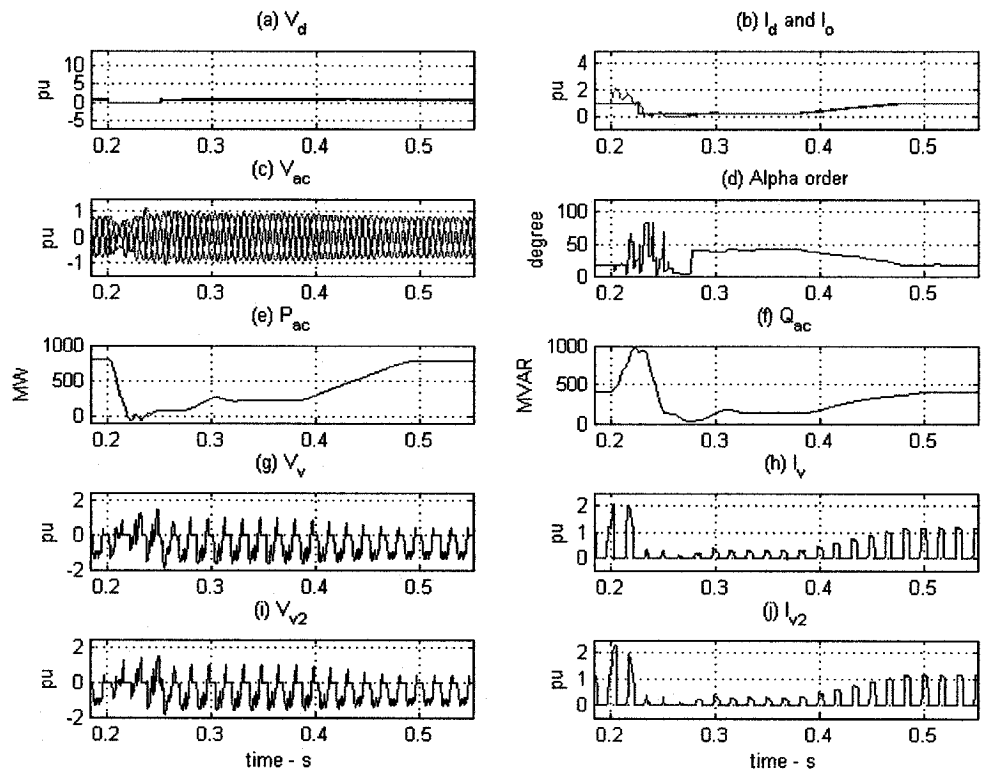

Figure 5.17: DC fault of the Standard Model with VDCL & FR Block

Proposed (hybrid diode-thyristor rectifier) Model: (Figure 5.18)

The rectifier DC current rises rapidly to a value greater than 4.0 pu, which is very large value and it will certainly damage the equipment. With only one 6-pulse thyristor controlled bridge and one 6-pulse diode uncontrolled bridge operating in series, it takes a long time to reduce the fault current. The current cannot be reduced simply by the action of VDCL as the uncontrolled diode-bridge continues to feed current to the fault. The DC voltage is reduced near to zero in the faulted region after the fault is cleared and it rises rapidly to a value greater than 6 pu with distortion, huge value which is also dangerous to equipments. The alpha value is distorted up to 0.55 s. AC active power and reactive

power remain close to zero for long period. From the valve voltage, it is clearly visible that the alpha value is distorted during the faulted region. The valve voltage remains close to zero in the faulted zone for long time after the fault is cleared. The current is reduced to zero for long period and takes long time to get the original value.

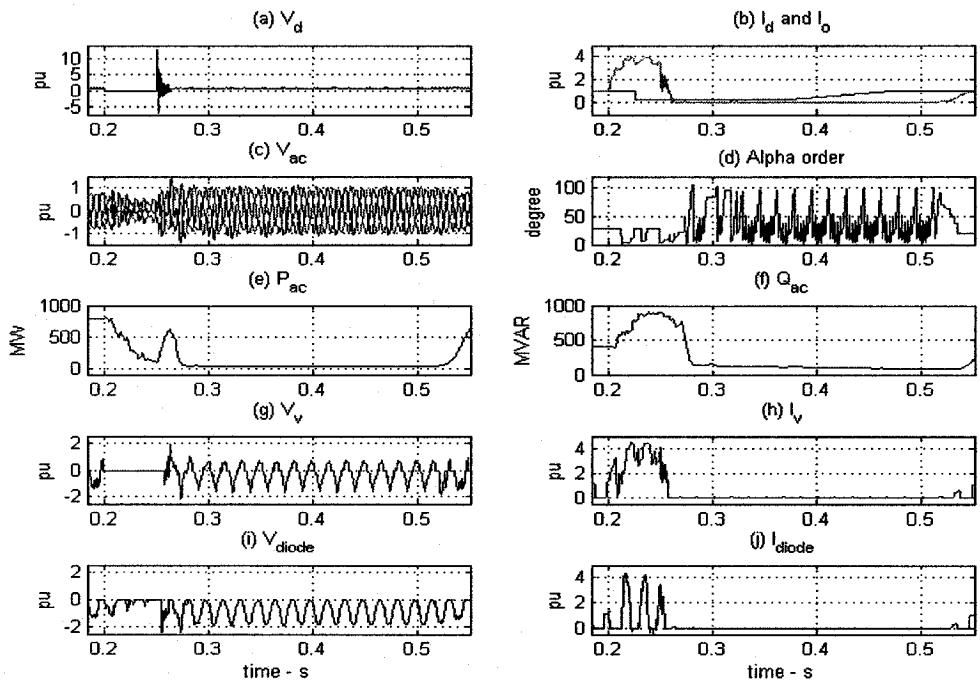

Figure 5.18: DC Fault in the Proposed Model

Differences:

There are big differences between the standard model and the proposed model recoveries following the fault application. For the standard model, fault causes the DC current to rise rapidly to a value greater than 2.0 pu and for the proposed model this value is much higher and rises to 4.0 pu. The subsequent action of the VDCL causes the current to be limited to its I_{min} value for the standard model. However, in the proposed model, the current cannot be reduced simply by the action of the VDCL as the uncontrolled diode

bridge continues to feed current in to the fault. For the standard model, there are two 6-pulse thyristor (controllable) bridges that are operating in series, so the FR action is good enough to force the DC current to stay close to zero. However, for the proposed model, (with one 6-pulse thyristor controlled bridge and one 6-pulse diode uncontrolled bridge operating in series), it takes a relatively long time (0.26 s) to reduce the fault current. In fact, the faulted DC current could not be extinguished without additional assistance in the form of opening an AC breaker on the AC bus. This represents one serious operational difficulty with the introduction of the proposed model. In the case of the standard model, the recovery is controlled and it follows the VDCL characteristic for AC active power, reactive power, valve voltages, and valve currents. However, the recovery with the proposed model proved to be much slower for all those characteristics due to an oscillating regulator.

DC Fault with AC Breaker for Proposed Model: (Figure 5.19)

An AC breaker, costly equipment is introduced in the AC side of the system. A signal generator is used for introducing an AC breaker. The width of the AC breaker is 0.05 s and it starts from 0.35 s. With the AC breaker, DC current is recovered to its original value at 0.45 s but without the AC breaker DC current is recovered at 0.53 s. All the AC active power & reactive power, valve voltages, valve currents, alpha, and DC voltage is recovered now at 0.45 s before that all those were recovered at 0.53 s. Therefore, with the addition of the AC breaker the effect of DC fault is reduced a little bit. Other alternative means to achieve this are also under investigation.

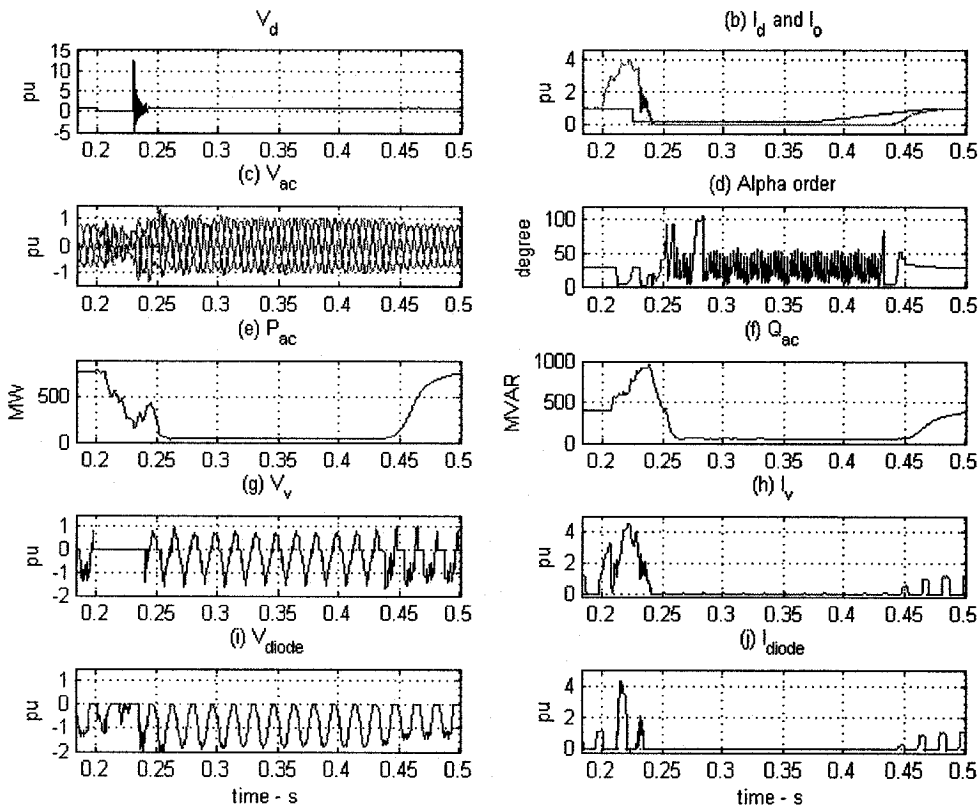

Figure 5.19: DC fault with AC breaker for the Proposed Model

5.4.6 Block / Deblock of rectifier firing pulses:

A deblock circuit is made by using two signal generators: one for blocking and one for startup purposes. Blocking of the rectifier firing pulses starts at 0.2 s for a period of 0.1 s.

Standard Model: (Figure 5.20)

During the blocking period, the DC current is reduced to zero and the current order is set to I_{min} = 0.2 pu by the VDCL unit in preparation for the recovery period. When the firing pulses are released, the DC current rapidly jumps to 0.2 pu and then follows the up ramp

of the VDCL unit. When the blocking of the pulses applied, output voltages is reduced to a very small value for few seconds then comes to the actual value and again it increases for few second when the firing pulses are released. The AC voltages increase in the blocking period and show the voltage regulation of the AC system. The alpha value is increased to 104.7° when the firing pulses are blocked and after the blocking period, it follows the current order and reaches to its original value. The AC active and reactive power are reduced to very small values in the blocking period. The valve voltage shows the effect of blocking the firing pulses. The valve current is reduced to zero in the blocking period.

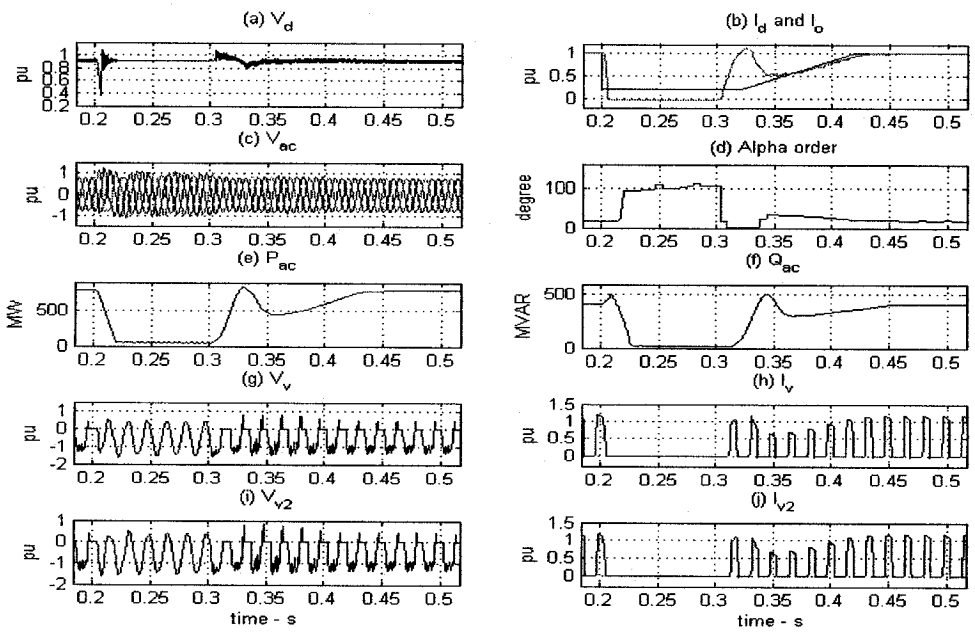

Figure 5.20: Block/Deblock of rectifier firing pulses of Standard Model

Proposed Model: (Figure 5.21)

The DC current is reduced to zero in the blocking period and after releasing the firing pulses, it follows the VDCL characteristics. The output voltage remains same as the standard model. The AC voltages increase in the blocking pulse region then again it reaches to its original value. The alpha value is increased to 151.4° in the blocking period. The AC active and reactive powers are reduced to very small values in the blocking period. The valve voltage shows the effect of blocking the firing pulses and the valve current is reduced to zero in that region.

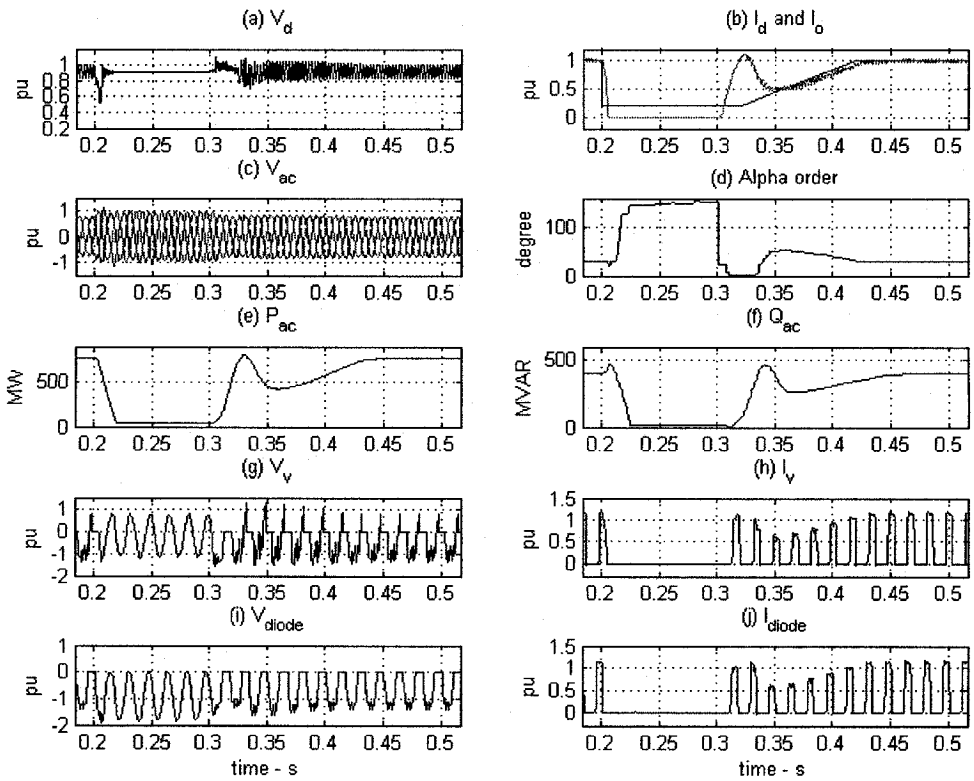

Figure 5.21: Block/Deblock of rectifier firing pulses of the Proposed Model

Differences:

The characteristics of DC output current, DC input voltages, AC active and reactive power, AC voltages, valve voltages, and currents are similar for both models. The only difference is in the alpha order. For the standard model, in the blocking period, alpha value is increased to 104.7° and for the proposed model; this value is 151.4° because of the higher firing angle of 28° for the proposed model compared to 18° for the standard model.

5.4.7 Misfire (Commutation failure):

In this test, a valve misfire is caused by removing a firing pulse for one cycle (16.67 ms) starting at 0.2 s. A misfire block is made by using a signal generator and a selector. A missing firing pulse can lead to a misfire (at a rectifier) or a commutation failure (at an inverter). The effects of a single misfire are similar to those of a single commutation failure (CF). Usually, a single misfire is self-clearing and no special control actions are necessary. However, a multiple CF can lead to the injection of AC voltages into the DC system. Control action may be necessary in this case [16].

Standard Model: (Figure 5.22)

The DC current follows the current order but when the misfire occurs, the DC current reduces to a very small value (0.38 pu) and takes time (0.3 s) to recover to its original

value. The DC and AC voltages are distorted during the misfire region. The alpha is reduced to zero and after the clearance of the misfire the value of alpha is 18°. Small effect in the AC active and reactive power, the value is reduced by very small amount in the misfire zone. The valve voltages and the valve currents show the missing firing pulses.

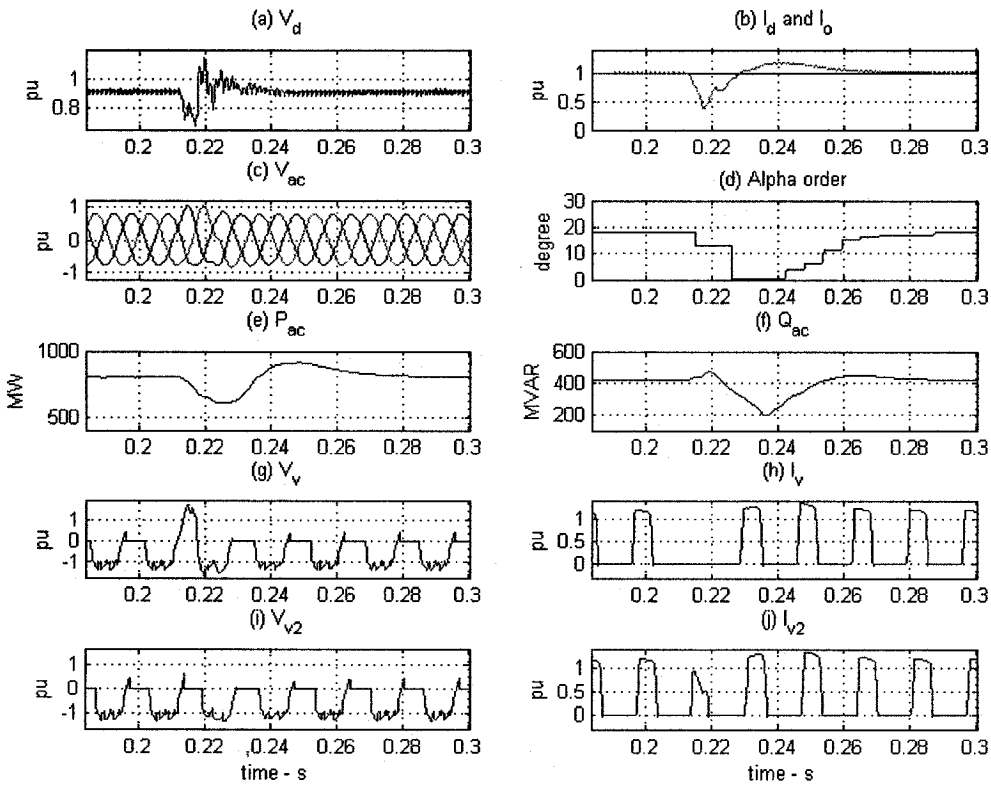

Figure 5.22: Misfire for the Standard Model.

Proposed (hybrid diode-thyristor rectifier) Model: (Figure 5.23)

The DC current is reduced to a small value (0.38 pu) in the misfire period then it follows the current order value. The DC voltage, AC voltages, and AC active and reactive power characteristics are similar with the standard model. The alpha value reduces to zero in the

misfire region then it increases to its system alpha value (28°). The valve voltages and currents show the missing firing pulses.

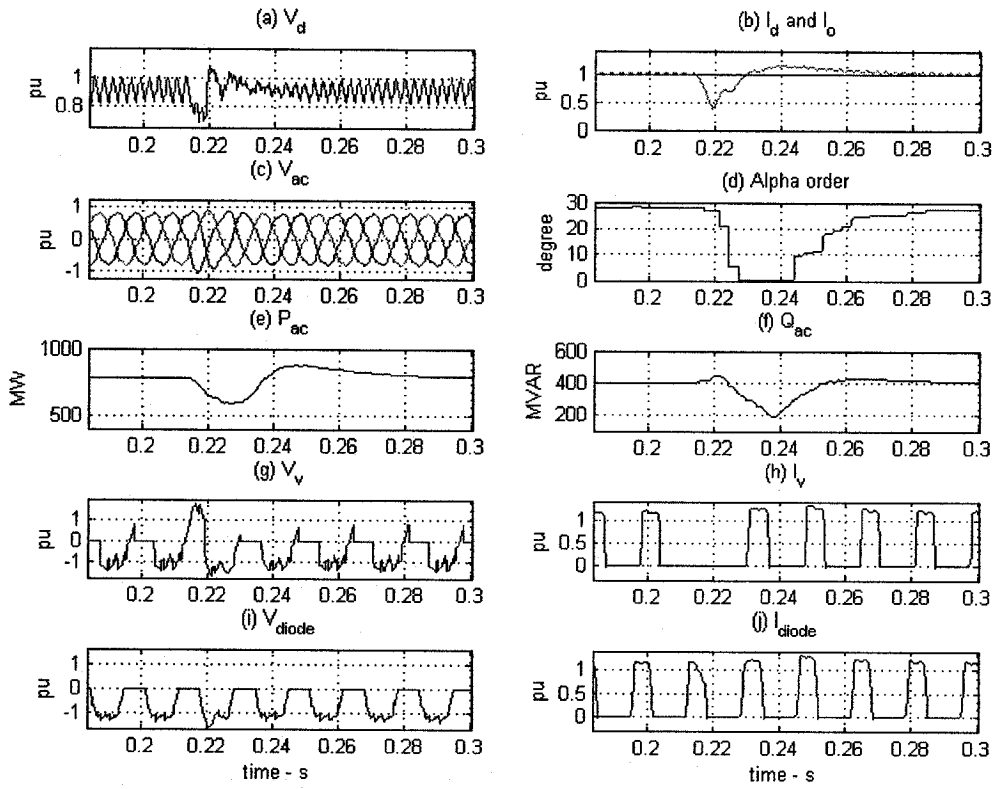

Figure 5.23: Misfire for the Proposed Model

Differences:

The response of the DC current in both models is virtually identical. However, the operating range of the firing angle in the proposed model is considerably much larger, since there is only one 6-pulse bridge capable of control action to aid in the recovery process to bring the DC current back to its nominal value. The behavior of the controller is quite stable in both cases.

5.5 Summary:

The performance comparison of both the models, during static-dynamic tests is presented in this chapter. The behaviors of both the models are more or less similar. The big difference in performance is found in case of the DC fault. It is very difficult to recover the DC fault like the standard model because of the uncontrolled diode-bridge in place of the thyristor-bridge. So an AC breaker, costly equipment is added to the system to recover from the fault but it will ultimately increase the overall system cost. Therefore, further investigation is needed to overcome the DC fault in the proposed model without increasing the overall system costs.

Chapter 6

CONCLUSIONS

In this thesis, a new hybrid diode-thyristor rectifier HVDC system was presented for possible reduction of the overall cost of the transmission system. To validate this model, the performance of this proposed model was compared with a CIGRE benchmark based 12-pulse thyristor rectifier HVDC system using EMTP-RV.

The following tasks are covered in this thesis:

1. The model description of the proposed model is presented. The differences of the proposed model are compared with the standard model. A CIGRE benchmark model is used as the standard model to compare control performances. A detailed model of the diode-bridge and the thyristor-bridge with snubber circuits is presented as the proposed model. The effect of the snubber parameters is evaluated.

2. The models used here do not present a detailed transmission line for simplicity. For a back-to-back link, the DC harmonics are contained within the converter building and not allowed to propagate for fear of interference with telephone circuits. The DC filter is used between the two smoothing reactors. The size of the smoothing reactor is chosen partly to block the current harmonics from being injected into the DC line. The DC filter then takes care of the voltage harmonics.

3. Two methods, a systematic optimization method and an approach based on Bode plots for designing the PI controller of the system were analyzed and compared. Both the control systems are considered feasible for the proposed model.

4. A filtering unit for the AC and DC side of the system was designed for the proposed model. The cost of filtering low order harmonics is very high and this is one of the serious drawbacks in the usage of hybrid model and might offset the savings in replacing a thyristor-bridge with a diode-bridge. But newer active filters now provide a means to do this economically.

5. A Voltage Dependent Current Limit (VDCL) unit, which provides an adaptive reference order to the current controller, is introduced to limit the fault currents.

6. A comparative evaluation of static and dynamic performances of the standard HVDC rectifier (with a 12-pulse thyristor-bridge) to the hybrid model (comprising of a 6-pulse thyristor-bridge and a 6-pulse diode-bridge) is made. To compare the performance of the proposed model with the standard model different static and dynamic tests were performed. A step change in current order is applied to its current reference to see the performance of the current controller. To study the response of the system under AC fault conditions, 1-phase and 3-phase faults at the rectifier side is presented. The use of VDCL block reduces the recovery time in case of 3-phase fault for both models. The dynamic performance suffers in case of a system recovery from a DC line fault for the hybrid option.

FR action and VDCL block is enough to recover from DC line fault in case of the standard model but for the proposed model, it takes a long time to recover from the fault. So an extra recovery circuit, comprising of an expensive circuit breaker, is needed for the hybrid model.

The work done here presented a detailed description about the proposed model and comparison with the standard model. These details can help to find alternatives for designing a hybrid HVDC rectifier station that presents lower cost than the conventional HVDC station.

FUTURE WORK

In this research work, as two different – one diode and one thyristor – 6-p bridges were used in series to make a hybrid 12-p converter, this converter consequently generated both characteristic and non-characteristic harmonics. So, AC and DC filter circuits were necessary to reduce the harmonic distortion to the acceptable levels employed within the industry. Therefore, the next phase of the work should focus on ways to reduce the effect of these generated harmonics. One way is to utilize an auxiliary voltage supply (AVS) inserted into the system, as shown in Figure 6.1. This may be feasible as long as the cost of the AVS is appreciably less than the potential savings from the hybrid converter. It is noted that the AVS is of a much smaller rating than the full size diode-thyristor bridge.

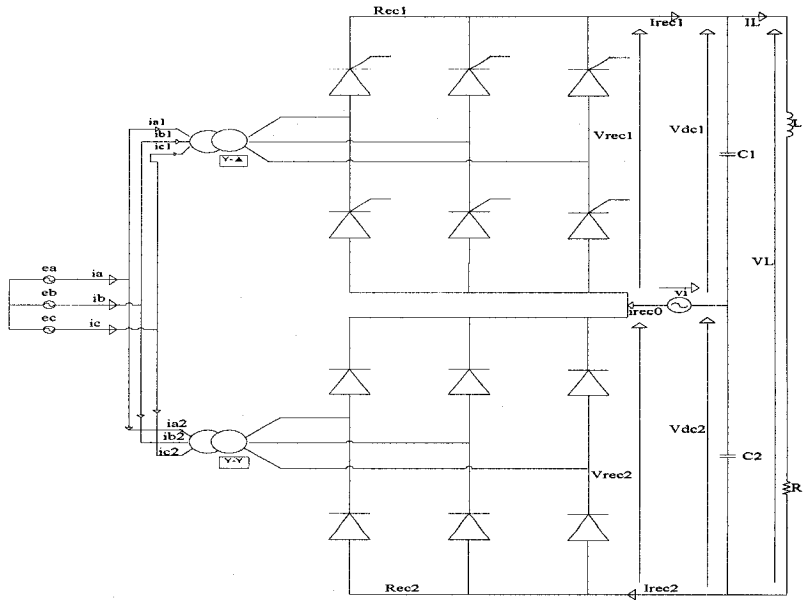

Figure 6.1: Propose Model with Auxiliary Voltage Supply, v_i

The AVS is to be inserted in the middle DC bus of the rectifier, and it will generate a square wave voltage (v_i) with an adjustable amplitude V_s, which has a frequency of six times the utility frequency. V_s should be adjusted as,

$V_s=24\omega L_s I_L/\pi \approx 48 f L_s I_L$

Where, I_L is the DC current and L_s is the transformer leakage inductance.

The purpose of the AVS is to shape the input current waveform. AVS will enable to reduce harmonic distortion of the rectifier input current.

In this research work, no detailed model of a transmission line was used for either the proposed model or the standard model. If a transmission line is used, it would make the controller design more difficult. So, for making the system simple to compare the static and dynamic performances of the proposed model with the standard model, a detailed

transmission line was not employed. It would be part of a future work to add the transmission line model to the system and then study its impact on the control system.

In an HVDC system, one of the problematic areas is the possibility of low-order harmonic resonance occurring. An HVDC converter acts as a source of harmonic currents on the AC side and harmonic voltages on the DC side. The source impedance and the filter capacitors of the converter form a low-frequency (typically within the 2^{nd} - 5^{th} harmonics) resonance circuit. If a low-order uncharacteristic harmonic is generated in small amounts, even when an equidistant pulse firing scheme is employed, this can be amplified due to the resonance. For an HVDC system poorly damped resonant networks can become a difficult operating condition. This condition can be made worse if there is a DC side series resonance at the complementary frequency of resonance in the AC side. Therefore, filter design has been carefully verified to avoid such resonance conditions [25]. The resonance effect was not studied in this thesis work. However, it will be an important contribution if in future works, resonance effects in the proposed HVDC system can be considered and solutions to recover from such resonance conditions be proposed.

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Appendix A

HARMONIC FILTER DESIGN

In this appendix, calculations pertaining to the harmonic filters are presented. Modified filter design for the proposed model is also presented here. For designing the harmonic filters at the rectifier for both AC and DC sides, the following assumptions are made:

- Total reactive power, Q_{Power} (total) = 480 Mvar
- Quality Factor for both AC and DC side filters = QF_T = 100
- The 11^{th} harmonic filter provides Q_{11}= 150 Mvar
- The 13^{th} harmonic filter provides Q_{13}= 150 Mvar
- The high pass harmonic filter provides Q_{Power} = 150 Mvar
- Shunt capacitive filter provides Q = 30 Mvar
- Value of Capacitance for the DC side C_{12} = 0.1 μF

For a 12-pulse converter the characteristic harmonics on AC side are of the order

$$h = pq \pm 1$$

where p is the pulse number, and q is any integer. For lower-order harmonics, single tuned R-L-C filters are used and for higher-order harmonics, a high-pass filter is used.

Line to Line voltage, V_{LL} = 230 kV (L - L)

The reactive power, Q_{Power} (Mvar) = $(V\ (kV))^2 \omega^0 C_n$

For the tuned low-pass filter, Quality Factor = $QF_T = \omega_0 L/R$

The reactive power, Q_{Power} (Mvar) = $(V\ (kV))^2 \omega^0 C_n$

For high-pass filter, Quality Factor = $QF_T = R/\omega_0 L$

For the 11th harmonic filter:

$$C_{11} = \frac{Q_{11}}{V^2 \omega_0} = \frac{150*10^6}{(230*10^3)^2 * 377} = 7.521\mu F$$

$$f_n = \frac{1}{2*\pi\sqrt{L_n C_n}}$$

$$L_n = \frac{1}{(2*\pi*f_n)^2 * C_n}$$

$$L_{11} = \frac{1}{(377*11)^2 * C_{11}} = 7.731mH$$

$$QF_T = \frac{\omega_0 L_{11}}{R_{11}}$$

$$R_{11} = \frac{377*7.731*10^{-3}}{100} = 0.029\Omega$$

For the 13th Harmonic:

$$C_{11} = C_{13} = \frac{Q_{11}}{V^2 \omega_0} = \frac{150*10^6}{(230*10^3)^2 * 377} = 7.521\mu F$$

$$L_{13} = \frac{1}{(377*13)^2 * C_{13}} = 5.535mH$$

$$QF_T = \frac{\omega_0 L_{13}}{R_{13}}$$

$$R_{13} = \frac{377*5.535*10^{-3}}{100} = 0.0208\Omega$$

For High-Pass Filter: (tuned to 23rd harmonic)

$$Q = V^2 \omega_0 C_{23}$$

$$C_{23} = \frac{150*10^6}{377*(230*10^3)^2} = 7.521\mu F$$

$$L_{23} = \frac{1}{(377*23)^2 * C_{23}} = 1.768mH$$

$$QF_{HP} = \frac{R_n}{\omega_0 L_n} = 100$$

$$R_{23} = 100*377*L_{23} = 66.6536\Omega$$

C Filter:

$$Q = V^2 * \omega_0 C$$

$$C = \frac{Q}{V^2 \omega_0} = \frac{30*10^6}{(230*10^3)^2 * 377} = 1.504\mu F$$

DC Side Filter:

For 12th harmonics high-pass filter is used.

$$QF_{HP} = 100$$

$$given C_{12} = 0.1\mu F$$

$$L_{12} = \frac{1}{(377*12)^2 * C_{12}} = 0.4886H$$

$$QF = \frac{R_{12}}{\omega_0 L_{12}}$$

$$R_{12} = 100*377*L_{12} = 18.3976k\Omega$$

Modified filter design for the proposed model

Two different converters are used for the proposed model. So the proposed model presents the characteristic harmonics of the order of 5^{th}, 7^{th}, 11^{th}, and 13^{th} so on. The design for the filter for this proposed model is presented here. Total reactive power is assumed, Q_{Power} (total) =480 Mvar

The reactive power, Q_{Power} (Mvar) = (V (kV))$^2\omega^0 C_n$

For the tuned-low pass filter, Quality Factor = $QF_T = \omega_0 L/R$

For high-pass filter, Quality Factor = $QF_T = R/\omega_0 L$

n	QF	Q (Mvar)	R (Ω)	L (mH)	C (μF)
5^{th}	100	75	0.282	74.85	3.76
7^{th}	100	75	0.144	38.19	3.76
11^{th}	100	100	0.044	11.61	5.01
13^{th}	100	100	0.031	8.31	5.01
C	-	30	-	-	1.504
high-pass	100	100	183.22	4.86	5.01
DC side	150	-	22.111 kΩ	0.391 H	0.5

Appendix B

Transfer function calculation for the DC line with filter arrangement

Figure 1 shows the DC side filter and the smoothing reactor arrangement for the proposed model. For calculating the transfer function, this figure is represented with an equivalent circuit shown in Figure 2.

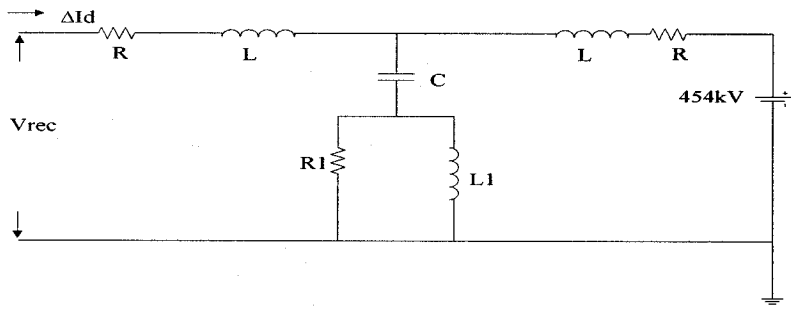


Fig 1: DC Line with DC filter arrangement

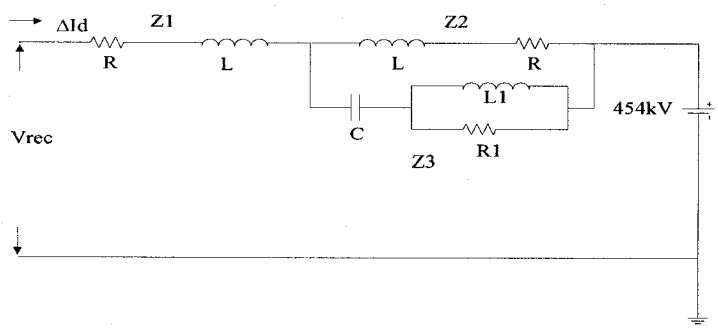


Fig 2: Equivalent circuit for calculating impedance

$$Z1 = R + j\omega L = R + sL = 2.5 + s0.35$$

$$Z2 = R + j\omega L = R + sL = 2.5 + s0.35$$

$$Z3 = \frac{1}{sC} + \frac{R1\, j\omega L1}{R1 + j\omega L1}$$

$$= \frac{1}{sC} + \frac{sR1L1}{R1 + sL1}$$

$$= \frac{R1 + sL1 + s^2 R1L1C}{sC(R1 + sL1)}$$

$$= \frac{22.11*10^3 + s0.391 + s^2 22.11*10^3 * 0.391*0.5*10^{-6}}{s0.5*10^{-6}(22.11*10^3 + s0.391)}$$

$$= \frac{22110 + 0.391s + s^2 4.32*10^{-3}}{0.011s + s^2 1.96*10^{-7}}$$

$$Z_{eq1} = Z2 \| Z3$$

$$= \frac{Z2 * Z3}{Z2 + Z3}$$

$$= \frac{(2.5 + s0.35)\left(\frac{22110 + s0.391 + s^2 4.32*10^{-3}}{0.011s + s^2 1.96*10^{-7}}\right)}{2.5 + s0.35 + \frac{22110 + s0.391 + s^2 4.32*10^{-3}}{0.011s + s^2 1.96*10^{-7}}}$$

$$= \frac{55275 + 7739.48s + 0.151s^2 + s^3 1.51*10^{-3}}{22110 + 0.419s + s^2 8.17*10^{-3} + s^3 6.86*10^{-8}}$$

$$Z_{eq} = Z1 + Z_{eq1} = (2.5 + s0.35) + \frac{55275 + 7739.48s + 0.151s^2 + 1.51*10^{-3}s^3}{22110 + 0.419s + s^2 8.17*10^{-3} + s^3 6.86*10^{-8}}$$

$$= \frac{110550 + 15479.02s + 0.31s^2 + 4.38*10^{-3}s^3 + 2.4*10^{-8}s^4}{22110 + 0.42s + 8.19*10^{-3}s^2 + 6.85*10^{-8}s^3}$$

So the transfer function of the DC filter with DC line is:

$$\frac{\Delta V_{d(0)}}{\Delta I_d} = \frac{110550 + 15479.02s + 0.31s^2 + 4.38*10^{-3}s^3 + 2.4*10^{-8}s^4}{22110 + 0.42s + 8.19*10^{-3}s^2 + 6.85*10^{-8}s^3}$$

Appendix C

MATLAB program used for designing the feasible region in optimization method for the proposed model

```
clear
% A Method of Optimizing PI controller Parameters of Diode-Thyristor
Hybrid
% Rectifier in HVDC Transmission System
% Ranges of PI parameters are selected
% Kp=0 to 4.2
% Ki=0 to 100

% transfer function of controller is : K(s) = (Kp*s + Ki)/(s + 0)

% Transfer function of the controller
% num1 = [Kp Ki];
% den1 = [1 0];
% K = tf([num1],[den1]);

% Transfer function of converter & Measurement block
sysb = tf( 84.04, [0.00397 1]);

% Transfer function of DC line and Filter
sysc = tf( [6.85e-8 8.19e-3 0.42 22110], [2.4e-8 4.38e-3 0.31 15479.02
110550]);
```

```
% plant is the series combination of the converter, DC line & Filter
and Measurement blocks
plant= sysb*sysc;

% Kp is changed from zero to 4.2 at a step of 0.05 &
% Ki is from zero to 100 with a step of 2
Kp=0:0.05:4.2;
Ki=0:2:100;
l1=length(Kp);
l2=length(Ki);

for i=1:l1
    for j=1:l2
        % Controller
        num1 = [Kp(i) Ki(j)];
        den1 = [1 0];
        K1 = tf(num1,den1);

       %open loop system is series combination of PI controller and
plant
       %blocks
       sys_open = K1*plant;

      % MARGIN(sys_open);
      % the value of gain margin and phase margin is found by
      % [Gm,Pm,Wcg,Wcp] = MARGIN(sys_open) with freguency and bode plot
of
```

```
        % the open loop system can be found with 'MARGIN(sys_open)'
command

        S=warning('off');

        [Gm,Pm,Wcg,Wcp] = MARGIN(sys_open);

        % Warning: the closed loop system is unstable.

        % Gain margins are G1(i,j) and Phase margins are P1(i,j)

         G1(i,j)=Gm;
         P1(i,j)=Pm;

         % Gain margin is converted to decibel value
         G1_dB(i,j) = 20*log10(G1(i,j));

         % For a stable system gain margin >=6dB and phase margin is from
40
         % to 60 degree
         % Stability requirement
         if ((G1_dB(i,j)>=6) && (P1(i,j)>=40 && P1(i,j)<=60))

                X(i,j)= Kp(i);
                Y(i,j)=Ki(j);
```

```
%         else
%             X1(i,j)=Kp(i);
%             X2(i,j)=Ki(j);

        end

    end
end

% X1=nonzeros(X);
% X2=nonzeros(Y);
plot (X,Y,'b:*')
axis([0 4.5 0 120])
set(gca,'ytick',[0:20:120])
set(gca,'xtick',[0:0.5:4.5])
grid on

% plot(x,y,'-.or')
% plots y versus x using a dash-dot line (-.)
% circular markers (o) at the data points
% and colors both line and marker red (r)
% title('Graph of the sine function')
% title('Feasible region of PI parameters considering stability
margin')
xlabel('Kp')
ylabel('Ki')
% print -r0 -dtiff myfile.tif
```

MATLAB program for an approach based on Bode plots for designing the controller in the proposed model

```
clear
% Matlab for The Plants Transfer Function:

% Transfer function of the converter block:
numg1=[-134.47]; deng1=[0.00277 1]; sysg1=tf(numg1,deng1);

% Transfer function of the Dc line and Filter:
numg2=[6.85e-8 8.19e-3 0.42 22110]; deng2=[2.4e-8 4.38e-3 0.31 15479.02
110550]; sysg2=tf(numg2,deng2);
% Command for the transfer function multiplication:
sys12=series(sysg1,sysg2);
sys12;

% Transfer function of the converter and DC line with filter:

%           -9.211e-006 s^3 - 1.101 s^2 - 56.48 s - 2.973e006
% ------------------------------------------------------------------
% 6.648e-011 s^5 + 1.216e-005 s^4 + 0.005239 s^3 + 43.19 s^2
%
%                                          + 1.579e004 s + 110550

% Transfer function of the measurement equipment:
numg3=[0.625]; deng3=[0.0012 1]; sysg3=tf(numg3,deng3);
```

```
% The transfer function of the plant
sysp=series(sys12,sysg3);
sysp;

% Transfer function of the plant:
%
%          -5.757e-006 s^3 - 0.6883 s^2 - 35.3 s - 1.858e006
% ------------------------------------------------------------------
% 7.978e-014 s^6 + 1.465e-008 s^5 + 1.844e-005 s^4 + 0.05706 s^3
%
%                                    + 62.13 s^2 + 1.592e004 s + 110550

% Bode plot of the plants transfer function
% bode(sysp);
% grid on
% title('Bode plot of the Plant')

% Cross over frequency fx=24 Hz
% Let fx=24 Hz, Wx=151rad/s
% s=151i;
% sysp=(-5.757e-6*s^3-0.6883*s^2-35.3*s-1.858e6)/(7.978e-14*s^6+1.465e-
8*s^5+1.844e-5*s^4+0.05706*s^3+62.13*s^2+1.592e4*s+110550);
% sysp =
%      0.3624 + 0.6214i

% Conversion from rectangular to polar:
% Gain Calculation
```

```
% R=abs(sysp);
% R =
%     0.7194
% In db
% y=log10(R);
% y =
%     -0.1431
% Gain=20*y
% Gain =
%     -2.8610


% Phase Angle of the plant in radian:
% theta=angle(sysp);
% theta =
%     1.0429
% Conversion from radian to degree
% Angle=theta*180/pi;
% Phase Angle =
%     59.7538


% Transfer function of the PI type I controller:
numc=[-0.0338 -1.344]; denc=[0.02515 0]; sysc=tf(numc,denc);
% Transfer function:
% -0.0338 s - 1.344
% -----------------
%     0.02515 s
% Transfer function of the system
sysf=series(sysp,sysc);
```

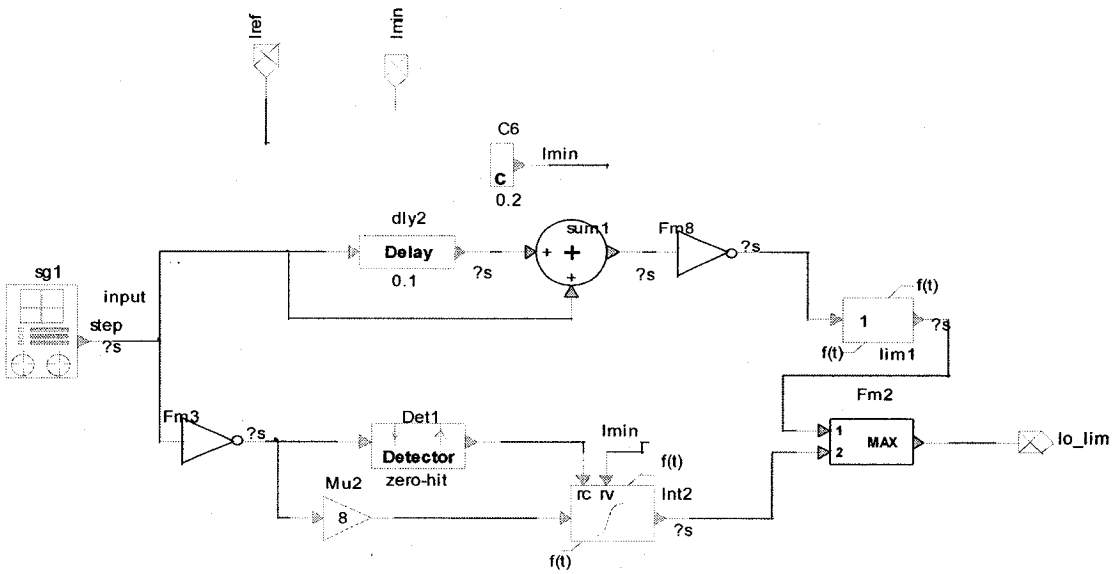
```
% Transfer function:
%
%       1.946e-007 s^4 + 0.02327 s^3 + 2.118 s^2 + 6.285e004 s +
2.497e006
% ------------------------------------------------------------------------
----------
% 2.006e-015 s^7 + 3.686e-010 s^6 + 4.638e-007 s^5 + 0.001435 s^4 +
1.563 s^3
%
%                                                                  + 400.3
s^2 + 2780 s
% bode plot of the open loop transfer function of the system
% bode(sysf)
% grid on
% title('Bode plot of the open loop system')
 % closed loop transfer function:
sysclosed=feedback(sysf,[1]);
sysclosed;


% Bode plot of the closed loop system
% bode(sysclosed)
% grid on
% title('Bode plot of the closed loop system')


% Step response of the closed loop system
% t=[0:0.005:0.6];
% [y,t]=step(sysclosed,t);
% plot(t,y),grid
```

```
% axis([0 0.6 0 1.4])
% xlabel('Time(sec)')
% ylabel('y(t)')
% print -r0 -dtiff myfile.tif
% title('Step Response for the closed loop system')
```

Appendix D

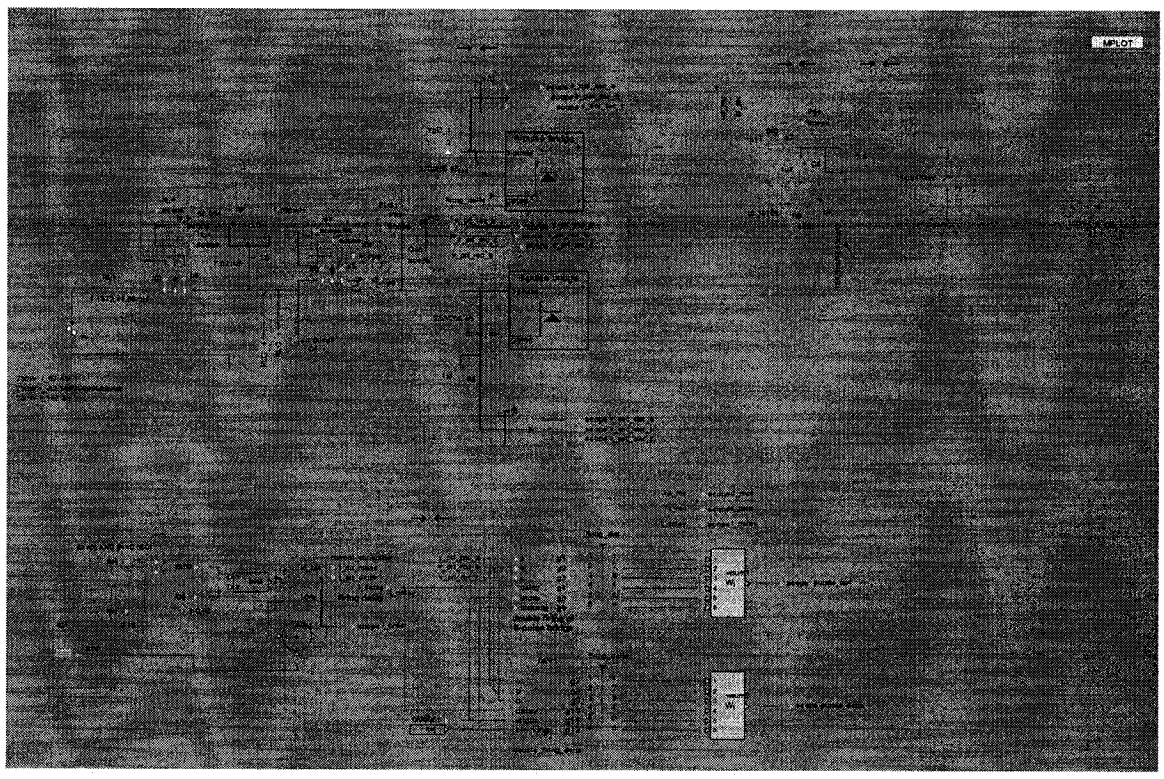
VDCL Block

A VDCL block is used to limit the current reference value for the rectifier controller based according to the level of the DC voltage. A current reference is set with the VDCL block. Different EMTP blocks are used for building a VDCL block.



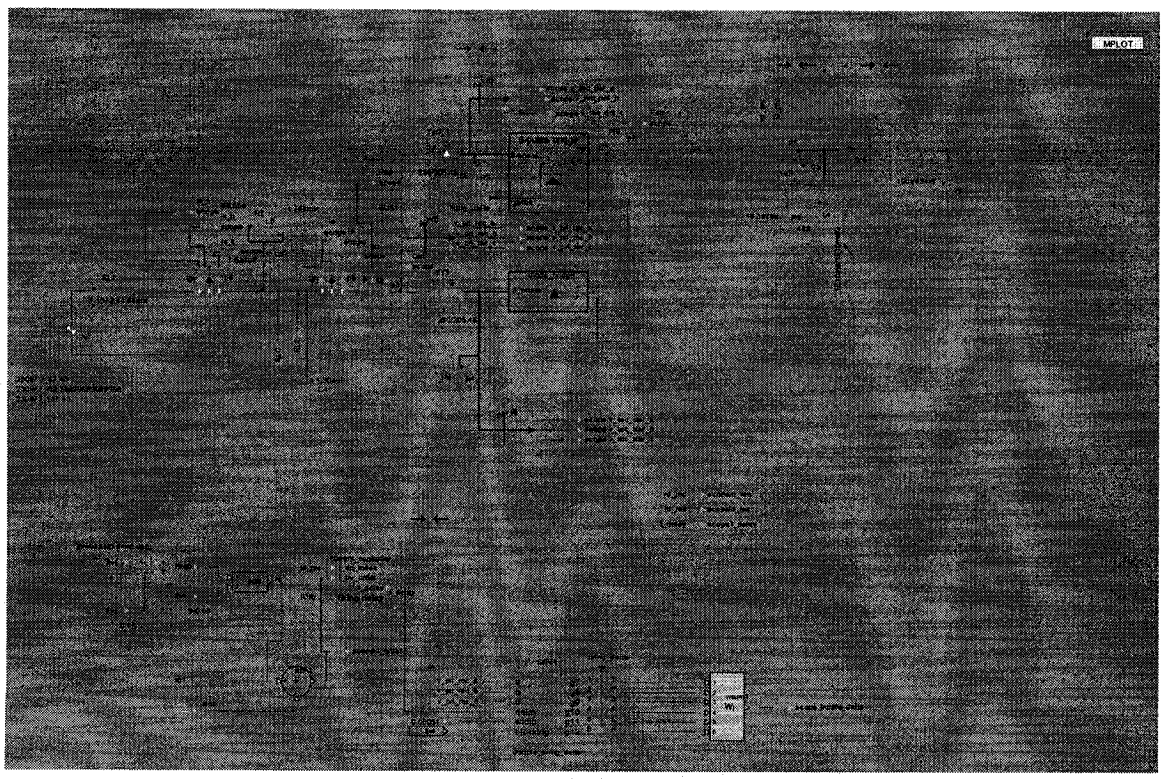
12-pulse Standard Model

Two thyristor-bridges are connected in series. Two controller blocks are used for firing the two thyristor-bridges.



Proposed Hybrid Diode-Thyristor Model

All the components in the proposed model are the same as the standard model. One thyristor -bridge and one diode-bridge are connected in series. So only one controller unit is used for the thyristor-bridge.



Appendix E

ALTERNATIVE TECHNIQUES TO REDUCE COSTS

The objective of the thesis is to propose alternative HVDC models for possible reduction of the overall transmission costs of the terminal equipments of an HVDC system. From the cost breakdown structure (Figure 1.1), it is seen that the valves are the most costly equipment of the HVDC system (i.e. 20% of the system cost). The second most costly equipment is the converter transformer (i.e. 16% of the total HVDC transmission system cost). Replacing the thyristor converters by a hybrid diode-thyristor converter has been investigated in previous chapters. However, replacing the converter transformer can be an alternative and additional way to reduce the HVDC transmission system cost.

Two transformers are used in either a hybrid diode-thyristor rectifier or a 12-pulse thyristor rectifier. The upper thyristor-bridge for both the models is connected with a Y-Δ transformer. This transformer is needed for a 30° phase displacement between the primary-secondary voltages and the turns ratio is adjusted to be compatible with the lower bridge. The lower thyristor-bridge (standard model) or diode-bridge (proposed model) is connected with a Y-Y converter transformer. This Y-Y transformer can be replaced with its equivalent impedance. The typical value of the transformer impedance i.e. leakage inductance and resistance are given below.

The ratings of the transformer:

Power rating= 500 MVA

Primary side voltage= 230 kV, and Secondary side Voltage= 205.45 kV

Winding Resistance = 0.00375 = 0.375%, and Winding Reactance = 0.15 = 15%

So, the Primary side impedance = $\frac{(230*10^3)^2}{500*10^6}\ \Omega = 105.8\ \Omega$

At 15% inductance, the value of leakage inductance = $\frac{105.8*0.15}{2*\Pi*60}$ H = 42.09 mH

And 0.375% resistance, the value of resistance = 105.8*0.00375 = 0.4 Ω

Secondary side impedance = $\frac{(205.45*10^3)^2}{500*10^6}\ \Omega = 84.42\ \Omega$

At 15% inductance, the value of leakage inductance= $\frac{84.42*.15}{2*\Pi*60}$ H = 33.589 mH

And 0.375% resistance, the value of winding resistance= 84.42*0.00375 = 0.32 Ω

The lower Y-Y transformer is replaced with the equivalent primary side impedance of the transformer from both the standard model and the proposed model. Then the simulation of both the models is performed using EMTP. The simulation is done only for verification of the static characteristics. The static characteristics represent AC input voltage, DC voltage, DC current, Valve voltages, Valve currents, AC active and reactive power, Alpha value etc. Figures 1 and 2 show the static characteristics of the alternative standard model (without transformer 12-pulse thyristor rectifier HVDC model) and the alternative proposed model (without transformer hybrid diode-thyristor rectifier HVDC model).

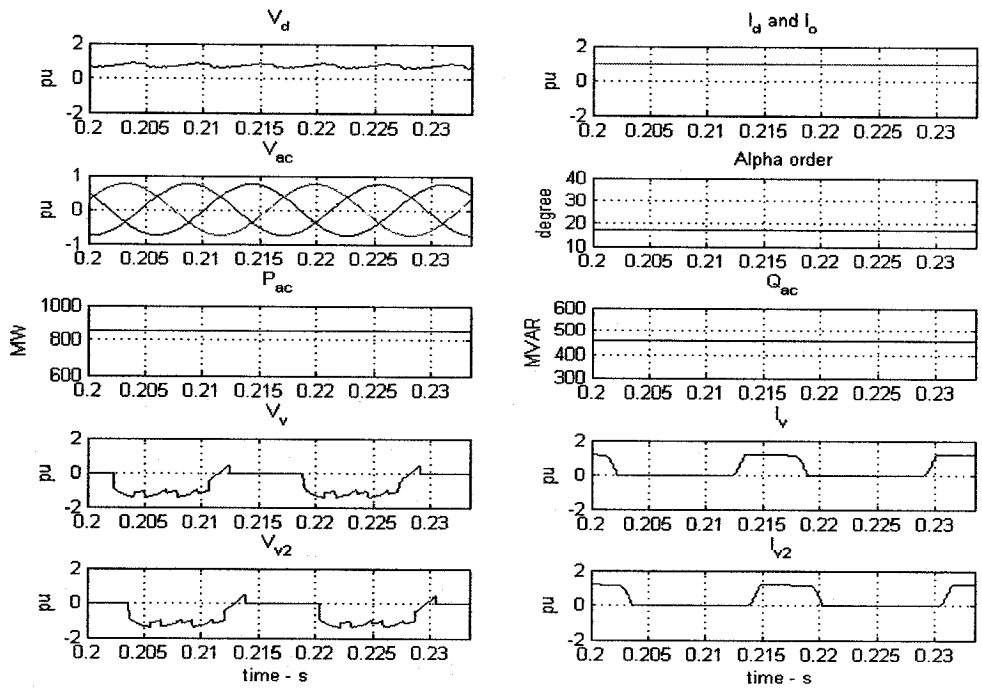


Figure 1: Alternative Standard Model

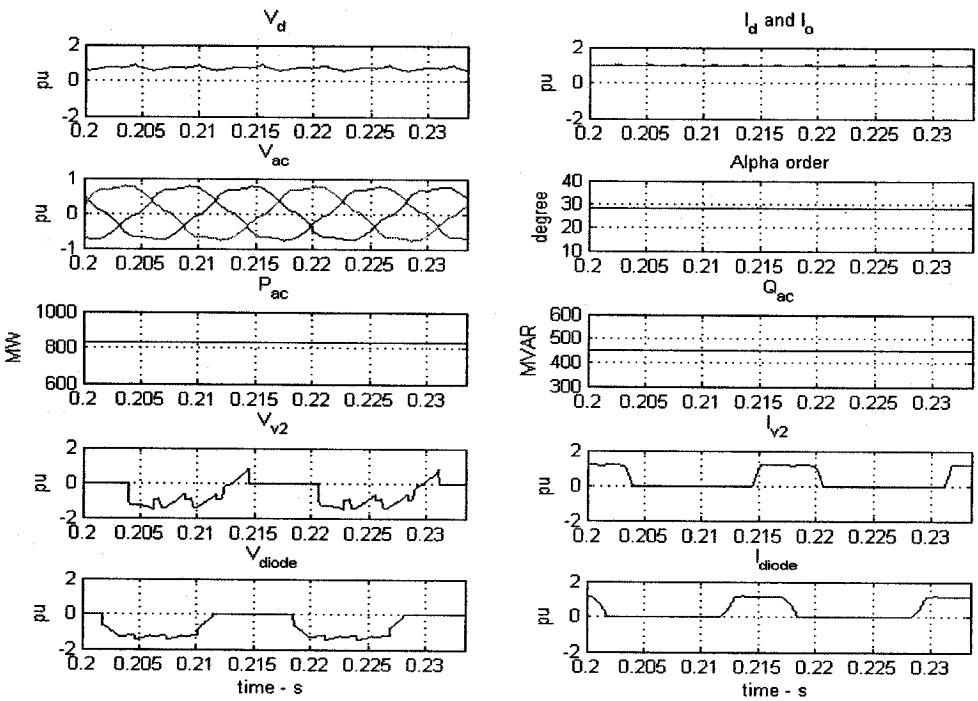


Figure 2: Alternative Proposed Model

Comparison of standard model with alternative standard model:

In the alternative standard model, the DC output voltage has 3rd (61 kV), and 6th (15 kV) harmonics so it contains a lot more ripple when compared to the standard model. The DC output current and alpha value is similar for both cases. The AC input voltage is lower (≈ 6 kV) in the alternative standard model. The AC active and reactive power is higher by ≈50 MW and 50 Mvar in case of alternative standard model. The valve voltages and valve currents are similar for both models.

Comparison of proposed hybrid diode-thyristor rectifier model with alternative proposed model:

In the alternative proposed model, the DC output voltage contains more ripple because of the presence of 3rd (48 kV), and 6th (31 kV) harmonics but the proposed model has only 6th (33 kV) harmonic. The DC output current and alpha value is similar for both cases. The AC input voltage is reduced by ≈ 6 kV in case of the alternative proposed model and AC active and reactive power is higher (≈ 50 MW and 50 Mvar respectively) than the proposed model. The valve voltages and valve currents are similar for both cases.

From these two comparisons, it can be concluded that the alternative method presents some increased low order harmonics such as 3rd harmonic. So an additional filtering unit is required to remove this 3rd harmonic which will increase the overall transmission cost

of the HVDC system. Further work is needed to evaluate fully the impact of replacing one converter transformer by its equivalent impedance.

Appendix F

List of Publications

Paper published on this research

N. Monsur, V.K. Sood and Luiz Lopes, "Modeling a hybrid diode-thyristor HVDC rectifier in EMTP-RV, IEEE Canadian Conference on Electrical and Computer Engineering, Ottawa, ON, May 2006.