Cell Search Algorithms for WCDMA Systems

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ABSTRACT

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Wideband Code Division Multiple Access (WCDMA) system uses orthogonal channelization codes to distinguish physical channels in a base station, while base stations are identified by different downlink scrambling codes. User equipments (UEs) must achieve synchronization to the downlink scrambling code before decoding any messages from base stations. The process of searching for a base station and synchronization to the downlink scrambling code is often referred to as cell search. The performance of cell search has a significant impact on a UE's switch-on delay, and thus it is very important to UE design.

The goal of designing a cell search algorithm is to achieve a balance between speed, accuracy and complexity. A basic three-stage cell search procedure has been defined by 3GPP. It employs synchronization channels and the common pilot channel to facilitate a fast cell search. This cell search scheme only works well if there is no frequency offset between a base station's transmitter and a UE's receiver and if sampling timing is perfect on a UE. In practice, however, imperfection of oscillator in a UE may cause a big frequency error as well as clock error. It usually results in phase rotations and sampling timing drifts, which may degrade cell search performance significantly. Some advanced cell search algorithms have been proposed for mitigating impacts of frequency error or clock error. However, there is no much discussion on comprehensive solutions that can deal with the two negative impacts at the same time.

In this thesis, we propose an algorithm that considers both frequency error and clock error. A fast and accurate cell search with a relatively low level of complexity is achieved. The algorithms are based on a combination of four existing enhanced cell search algorithms that are designed for a toleration of either frequency error or clock error. We first introduce the 3GPP-defined cell search algorithm as a basis. Then the four existing enhanced algorithms, PSD (partial symbol de-spreading), DDCC (differential detection with coherent combining), STS-1 (serial test in stage-1) and RSPT (random sampling per trial) are presented. Next, we propose four possible combinations of the existing algorithms: PSD+STS-1, PSD+RSPT, DDCC+STS-1 and DDCC+RSPT. Through extensive computer simulations, we find the DDCC+RSPT algorithm to be the best one. It is superior to other combinations and also outperforms any existing algorithm in terms of acquisition time, detection probability and complexity. Therefore, it is highly recommended for practical uses.

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To my dearest grandparents

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Bw	Signal bandwidth before spreading
Bn	Signal bandwidth after spreading
$S_{dl,n}$	Complex-valued downlink scrambling code
C_{psc}	Primary synchronization code
C_{ssc}	Secondary synchronization code
Yj	Received complex-valued baseband signal at chip j
T	Length of one slot
k	Index of combined slots
Un	The nth slot boundary candidate
$Mslot$	The best slot boundary candidate
r	Index of C_{ssc} sequences
s	Index of slots in one signal frame
$Vs(r)$	Correlation outcome for rth C_{ssc} sequence on sth slot
L	Length of one signal frame
SRC	Scrambling codes in the identified code group
i	Index of the codes in the identified code group
Wi	Correlation outcome for ith downlink scrambling code in the identified code group

List of Acronyms

2G	The second generation
3G	The third generation
NMT	Nordic Mobile Telephony
AMPS	Advanced Mobile Phone Services
GSM	Global System for Mobile Communication
GPRS	General Packet Radio Services
EDGE	Enhanced Data rates for Global Evolution
UMTS	Universal Mobile Telecommunications Services
3GPP	3rd Generation Partnership Project
WCDMA	Wideband Code Division Multiple Access
DS-CDMA	Direct Sequence Code Division Multiple Access
DS-SS	Direct Sequence Spread Spectrum
GPS	Global Position System
UE	User Equipment
LOS	Line-of-sight
AWGN	Additive White Gaussian Noise
TDMA	Time Division Multiple Access
FDMA	Frequency Division Multiple Access
CDMA	Code Division Multiple Access
UTRA-FDD	UMTS Terrestrial Radio Access - Frequency Division Duplexing
UTRA-TDD	UMTS Terrestrial Radio Access - Time Division Duplexing

QoS	Quality of service
OVSF	Orthogonal Variable Spreading Factor
P-SCH	Primary Synchronization Channel
S-SCH	Secondary Synchronization Channel
CPICH	Common Pilot Channel
QPSK	Quadrature Phase Shift Keying
CFRS	Comma free Reed-Solomon
DPCH	Dedicated downlink physical channel
DPDCH	Downlink dedicated physical data channel
DPCCH	Downlink dedicated physical control channel
DTX	Discontinuous Transmission
RRC	Root raised cosine
PSD	Partial symbol de-spreading
DDCC	Differential detection with coherent combining
STS-1	Serial test in stage-1
RSPT	Random sampling per trial
PPM	Parts per million
SNR	Signal to noise ratio

Chapter 1: Introduction

1.1 General

The mobile telecommunication world has changed dramatically during the last two decades. The first generation (1G) analog mobile communication systems, such as NMT (Nordic Mobile Telephony) and AMPS (Advanced Mobile Phone Services) [1], offered speech services only, and they were replaced by the second generation (2G) digital mobile communication systems during the mid 1990's. The 2G systems, well known as GSM (Global System for Mobile Communication) and IS-95/cdmaOne (Interim Standard 95) [2], are capable of offering both speech and low speed circuit-switched data services. Later on in 1990's, 2G systems were evolved to support higher data rate with the adoption of GPRS (General Packet Radio Services) and EDGE (Enhanced Data rates for Global Evolution) technologies [3], which are referred to as 2.5G systems. However, these 2.5G technologies are yet far from satisfaction of the rapidly growing needs of higher data speed, more efficient spectrum utilization, and increasing multimedia applications (e.g. web-surfing, interactive gaming and video streaming). Hence, the third generation (3G) mobile communication systems are developed with the aim to support all these advanced services [4].

ITU (International Telecommunication Union) defined IMT-2000 (International Mobile Telephony 2000), for the whole 3G family. One of key members of the family is UMTS

(Universal Mobile Telecommunications Services) [5], which was developed in Europe. Another important member, CDMA2000, was developed in the United States, which is evolved from the IS-95 narrow-band CDMA (Code Division Multiple Access) system. The 3rd Generation Partnership Project (3GPP) is the standardization work for UMTS, in which Wideband CDMA (WCDMA) is chosen as the radio access technology. WCDMA is a type of Direct Sequence Code Division Multiple Access (DS-CDMA) which conceptually accommodates multiple users in radio transmission. It spreads radio signal out over a much wider bandwidth than that of the radio signal itself [6]. Different from the narrow-band CDMA, the WCDMA that has a much wider bandwidth offers significant improvements, including the enhanced coverage and capacity due to the higher bandwidth and coherent uplink detection, its support to multiple parallel services on one connection, its capability of being compatible with capacity-improving technologies such as adaptive antennas and multi-user detection, and its support to a fast and efficient packet-access protocol [7].

1.2 Motivation and Scope

In WCDMA systems, data on multiple channels from different transmitters are transferred over air interface simultaneously. In order to successfully detect information from the desired sources, two types of codes, channelization code and scrambling code are used to distinguish different channels and different transmitters. Channelization codes can separate transmissions of different channels on downlink. They can also separate data payload and control information from one UE on uplink [7]. The same set of channelization codes are reused by all UEs and base stations. Scrambling codes are

needed to separate transmitters of base stations on downlink direction and to separate transmitters of User Equipments (UE) on uplink direction. In a typical scenario, the WCDMA transmitter multiplies each channel by channelization codes in order to separate data channels. The separation between different transmitters is achieved by multiplying the data signal with a scrambling code which has very low cross correlation with the channelization codes. On the other side, the receiver needs to know which scrambling code is exactly transmitted in order to perform a reverse process (i.e. de-scrambling), which removes scrambling code. The transmitting and receiving process is briefly illustrated in Figure 1.1. An accurate synchronization of scrambling code is of significant importance in the receiver side for retrieving baseband data.

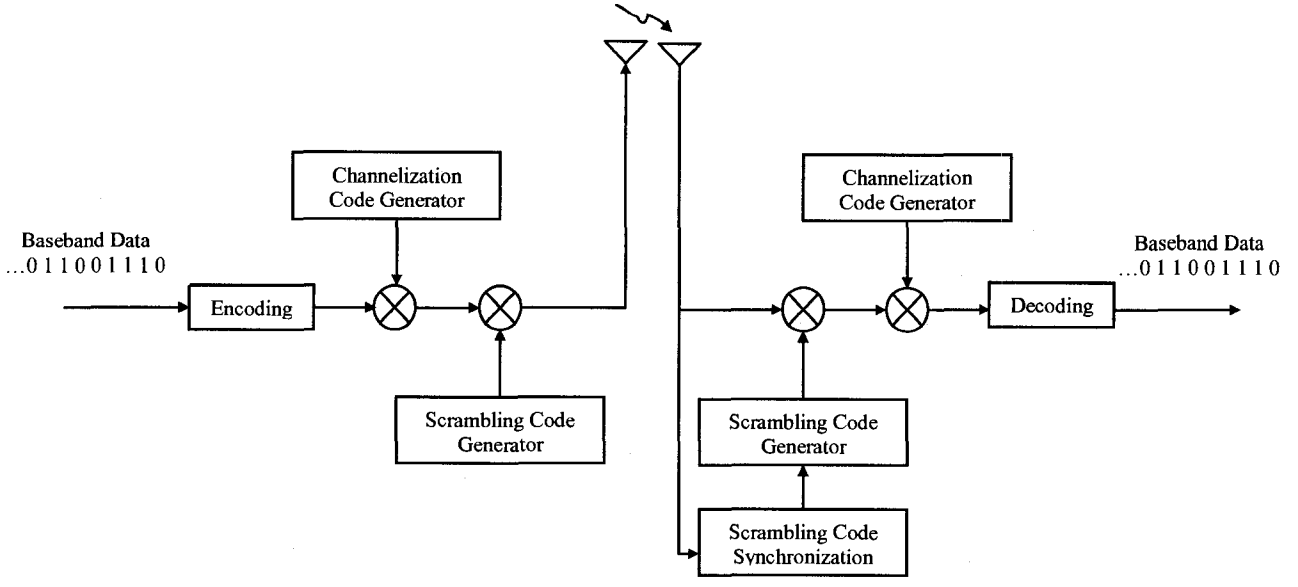


Figure 1.1: Block diagram of WCDMA transmitter and receiver

Regarding the scrambling code synchronization, a major difference between WCDMA and other CDMA systems (i.e. IS-95 and CDMA2000) should be mentioned, i.e. WCDMA supports asynchronous base station operation whereas the other CDMA systems rely on synchronized base stations [8]. Synchronous CDMA systems need

external time references, such as Global Position System (GPS) to synchronize their operations. In this case, UEs use different phases of the same downlink scrambling code to distinguish different base stations. In WCDMA systems, however, each base station has an independent time reference, and a UE does not have the knowledge about the relative time difference between base stations in advance. Thus, the adjacent base stations can only be identified by using a set of distinct downlink scrambling codes which contains several hundreds of scrambling codes. If all these codes have to be searched during code synchronization, the WCDMA cell search, that involves the process of achieving synchronization for downlink scrambling code, will require much more time than the cell searches in the synchronous CDMA systems. Therefore, for WCDMA systems, it is critical to develop efficient algorithms to perform cell search in a fast and reliable manner. Furthermore, the multipath fading on radio propagating path, and the negative impacts caused by the natural limitation of the radio transmitter and receiver (e.g. large frequency and clock error), add more technical challenges to the implementation of cell search. The purpose of this thesis is to find optimal cell search algorithms which are able to overcome the impacts of large frequency and clock errors in multipath fading radio environments.

Many research efforts have been devoted to improve the performance of cell search in WCDMA systems [8]-[26]. Some of the previous works provided detailed and comprehensive illustrations for basic issues of cell search algorithms [9]-[10]. Other researches focused on performance analysis based on optimal settings of system parameters (i.e. threshold settings, number of combined correlations, power allocation

among channels and number of codes in code groups) [11]-[17]. On the other hand, efforts were made to solve problems for practical use, for example, to mitigate the performance degradation caused by the frequency error [9] [18]-[21], and the clock error [22]-[23]. Also, some discussions were brought up for hardware implementation in order to obtain a good tradeoff between complexity, power consumption and performance [24]-[26]. All these cell search algorithms are proposed to adapt to different conditions and radio environments, respectively, In reality, however, the impact of different conditions are always present together. For instance, frequency error and clock error should be taken into account together when designing an algorithm. Very few works have dealt with this compound condition.

The study in this thesis is an attempt to develop an improved cell search algorithm that is suitable for the condition of simultaneous frequency error and clock error. The main idea of the new algorithm is to combine several existing enhanced versions, namely, partial symbol de-spreading [9] and differential detection with coherent combining [19] (designed to overcome frequency error), and serial test in stage-1 and random sampling per trial [22] (designed to mitigate clock error). The performance of four new combinations is analyzed and compared via simulations. The comparisons are based on two metrics: mean acquisition time and detection probability.

1.3 Thesis Organization

The remaining part of this thesis is organized as follows. Chapter 2 provides background information on spread spectrum system, CDMA concept and WCDMA air interface

parameters. It also introduces information relevant to the cell search operation, such as channelization codes, downlink scrambling codes, related physical channels and downlink spreading and modulation. A basic three-stage cell search procedure presented on 3GPP specification is also briefly introduced. In Chapter 3, the basic three-stage cell search algorithm which is the basis of all the subsequent algorithms studied is presented first. Then, four existing enhanced cell search algorithms proposed to counteract frequency error or clock error are investigated. Based on them, four improved combined algorithms are presented to overcome the simultaneous impact of frequency error and clock error. In Chapter 4, we carry out computer simulations for the basic cell search algorithm, four enhanced algorithms and the proposed combined algorithms. The simulations are undertaken under different radio propagation environments with an injection of frequency error and clock error. Finally, in the last chapter, we draw conclusions and provide some suggestions for future work.

Chapter 2: Fundamentals of Cell Search

In this chapter, basic principles of spread spectrum and CDMA as well as radio channel characteristics and propagation environment will be first introduced. Secondly, parameters, channels, codes and operations on the physical layer of WCDMA systems will be presented. Next, the cell search procedure defined in the 3GPP specification will be covered. There are considerable amount of literatures contributed for principles of mobile communications and WCDMA systems. The topics selected and discussed in this chapter are the necessary fundamentals for the study in the following chapters.

2.1 Radio Propagation Channel Conditions

Mobile communication uses radio spectrum as transmission medium. This enables mobility for end users, but in the mean time, it introduces noise, attenuation and fading to radio receivers.

2.1.1 Multipath Fading

Fading describes how radio signal is attenuated on its way from the transmitter to the receiver. The degree of fading depends on radio propagation environment. A transmitted signal attenuates differently in various environments, and it reflects and diffracts when it passes through different surfaces and obstacles. This then causes different delays and distortions. When a radio signal propagates between a base station and a UE, it has many possible ways to go. In an optimal case, which is called line-of-sight (LOS) situation, the base station and the UE are visible to each other, and the signal can be propagated via the

shortest path to the receiving side. However, in a typical real environment, reflections and diffractions from different obstacles make the signal propagate via multiple paths, i.e., non-line-of-sight (NLOS). This is called multipath propagation [28]. Different paths have different lengths, and therefore duplications of the same signal arrive at receiver in different time slots. These duplicated signals are called multipath components. Time difference between each component and the first arriving component is called relative delay. The ratio of the power of each component and to the power of the first arriving component is called relative power. Thus, the received signal consists of a series of components which have different relative delays and relative powers. An example of multipath propagation environment is shown in Figure 2.1. Signals are reflected typically from walls of buildings, cars etc., and diffractions occur when signal meets sharp edges, such as roofs and corners of buildings. The received signals are aggregated from multipath components. These propagating components have different phases relative to each other, and they can be added either constructively or destructively depending on their relative phases. The relative phases change very fast due to relative movements between transmitter, propagating environment and receiver. Even with fixed transmitters and receivers the signal phase still changes because of the mutation of the environment. The variation of the received channel gain is very fast and this type of fading is referred to as multipath fading. In a NLOS situation, when distributions of amplitudes and phases of the received signal are statistically independent, the fading is called Rayleigh fading, and the amplitudes of multipath components are Rayleigh distributed. Fading dips at the receiver are caused by mutual cancellation of multipath components. This cancellation

may happen at one time instant, but even a small movement of UE may result in an opposite situation.

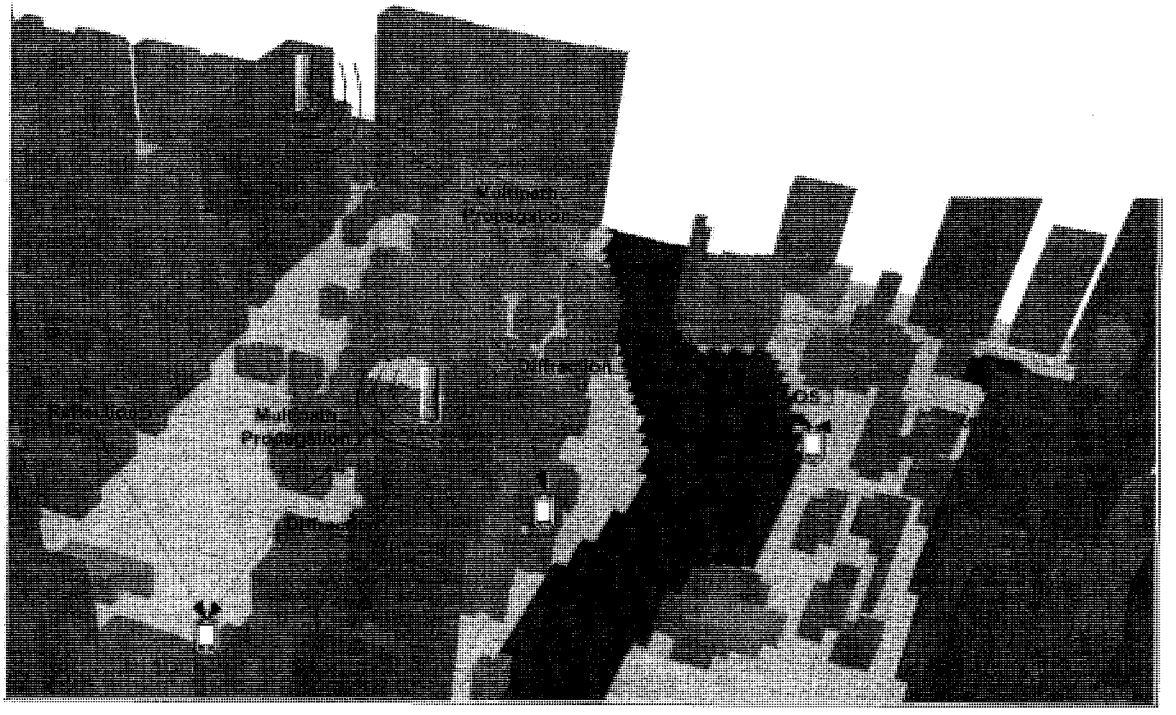


Figure 2.1: Signal propagation in multipath propagation environment

2.1.2 Static Propagation Channel Condition

In static propagation, there is no multipath fading. The only measured component is Additive White Gaussian Noise (AWGN). AWGN channel model is the one in which the only impairments are a linear addition of wideband or a white noise with a constant spectral density and Gaussian-distributed amplitude [29]. This type of background noise comes from many physical sources, such as thermal vibrations of atoms in antennas.

2.2 Spread Spectrum System

As mentioned in Chapter 1, air interface used in UMTS is wideband DS-CDMA. The technology behind DS-CDMA is known as Direct Sequence Spread Spectrum (DS-SS). The main idea of DS-SS is to spread data sequence and transmit it over a larger frequency band by multiplying it with a wideband pseudo-random binary sequence, i.e. spreading code [30]. Each symbol in this code is called a chip. The chips have a much higher rate and thus a larger bandwidth than that the original data sequence has. WCDMA uses the chip rate 3.84 Mcps (chip per second), which yields a bandwidth of 5 MHz approximately. Different spreading codes can be used to allow multiple users to transmit on the same frequency simultaneously. On the receiver side, the spread signal is multiplied with the synchronized spreading code which should be the same as the one used in transmitter side, and thus the original data sequence can be restored. This reverse procedure is called de-spreading. In order to easily de-spread the signal and to reduce interference, spreading codes should be orthogonal to each other. A simplified illustration for the spreading and de-spreading is shown in Figure 2.2.

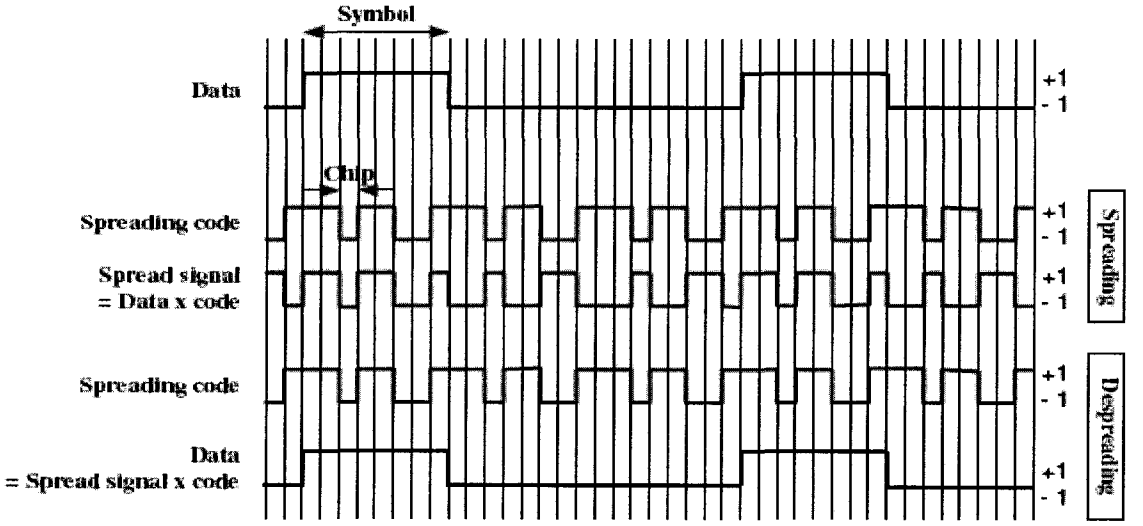


Figure 2.2: Spreading and de-spreading in DS-CDMA

The conceptual block diagram of a spread spectrum system is depicted in Figure 2.3.

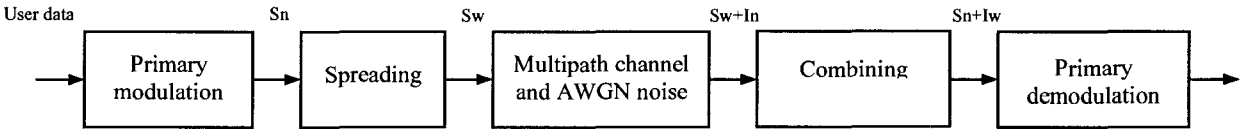


Figure 2.3: Spread spectrum system

In the figure, we can see that after spreading, the wideband signal S_w is transmitted on radio channel. The narrowband interference I_n which is caused by multipath propagation and additive noise would corrupt the transmission. The de-spreading operation in the receiver not only de-spreads the received wideband signal S_w back to narrowband signal S_n but also spreads the narrowband interference I_n into wideband interference I_w. Hence, after filtering, the most power of the interference is eliminated and the original user data can be detected. This is one of the advantages of the spread spectrum system, anti-jamming, which is illustrated in Figure 2.4. In the spread spectrum system, the processing gain G_p is defined as the ratio of the bandwidth of the spread wideband signal (B_w) to that of the original narrowband signal (B_n), namely,

$$G_p = \frac{B_w}{B_n} \tag{2.1}$$

This ratio is also referred to as spreading factor (SF), which is identical to the ratio of the rate of the spreading code to that of the original data sequence. The processing gain determines the number of users that can be allowed to use the system, the ability to reduce the multipath fading effect and to detect the desired signal correctly [30].

In order to obtain the benefit of a spread spectrum system, the receiver must be able to perform the desired reverse process, de-spreading. This requests an accurate synchronization for spreading codes including the downlink scrambling codes.

2.3 Multiple Access

Multiple access can be defined as a sharing of common limited radio resources in order to allow for a simultaneous use of the resources by multiple users. In mobile communication systems, there are three basic strategies to share air interface: TDMA (Time Division Multiple Access), FDMA (Frequency Division Multiple Access) and CDMA (Code Division Multiple Access). The principle of TDMA is to divide time domain, i.e. users transmit and receive data at different time instants. In FDMA the sharing is provided by allocating different frequencies for different users. TDMA and FDMA can be combined together, as illustrated in Figure 2.5(a). In TDMA/FDMA systems, one connection can be set up on different time slots and on different frequencies as well. This technique is called frequency hopping and it is used in GSM system [30]. TDMA/FDMA systems are considered as narrowband systems. Different from TDMA/FDMA, the idea of CDMA is to utilize spread spectrum and wideband signals for radio transmission. Thus, in CDMA systems, multiple users utilize the same frequency resource simultaneously. The separation of different users is achieved by using orthogonal spreading codes, as shown in Figure 2.5(b).

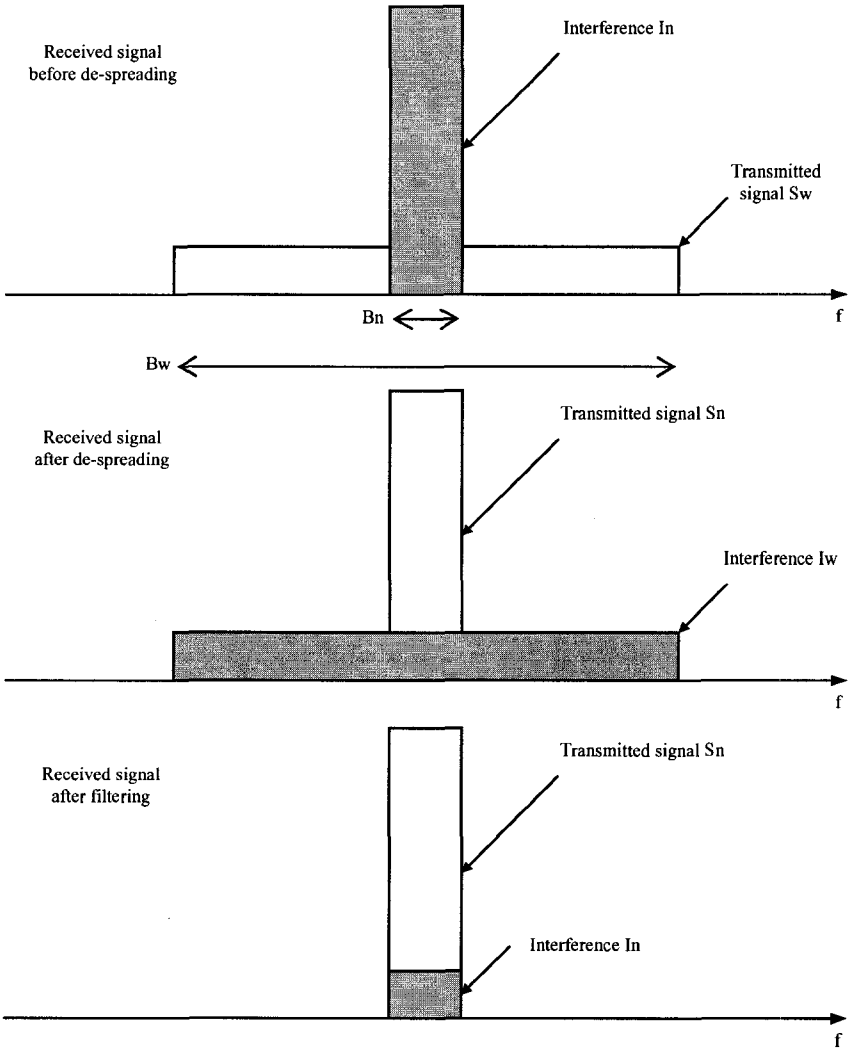


Figure 2.4: Tolerance of spread spectrum system to narrowband interference

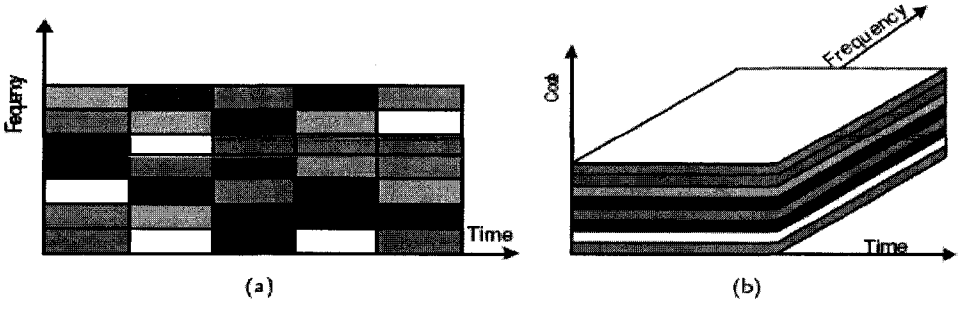


Figure 2.5: Multiple access techniques (a) TDMA/FDMA (b) CDMA

2.4 Key Parameters of WCDMA Air Interface

3GPP standardizes two different modes for WCDMA air interface, UTRA-FDD (UMTS Terrestrial Radio Access - Frequency Division Duplexing) and UTRA-TDD (UMTS Terrestrial Radio Access - Time Division Duplexing). In this thesis, cell search algorithms will be discussed under FDD mode. Some key physical layer parameters of FDD mode are listed in Table 2.1 [31].

Table 2.1 : Some key physical layer parameters of UTRA-FDD

Channel (carrier) spacing	5MHz
Carrier chip rate	3.84Mcps
Timeslot structure	15 slots / frame
Frame length	10ms
Channelization codes	OVSF
DL modulation	QPSK
RRC filter roll-off factor	0.22
Spreading factors	4, 8, 16, ..., 512

Additionally, 3GPP defines 11 operating frequency bands for UTRA-FDD mode [32]. We will use Band I as carrier frequency band for our simulation.

2.5 Channelization Code

The WCDMA system supports parallel variable-bit-rate transmissions with different quality of service (QoS). This requires a good separation between physical channels. Channelization codes are used to separate transmissions from different users. They are also used to spread bandwidth of signal. The 3GPP has applied OVSF (Orthogonal Variable Spreading Factor) codes as Channelization codes [33]. The purpose is to preserve orthogonality between physical channels with different rates. OVSF codes can

be defined with a code tree as shown in Figure 2.6. The codes are identified by $C_{ch,SF,k}$ with spreading factor SF and code number k, in which ($0 \leq k \leq$ SF-1). SF is the number of chips per user data symbol after spreading.

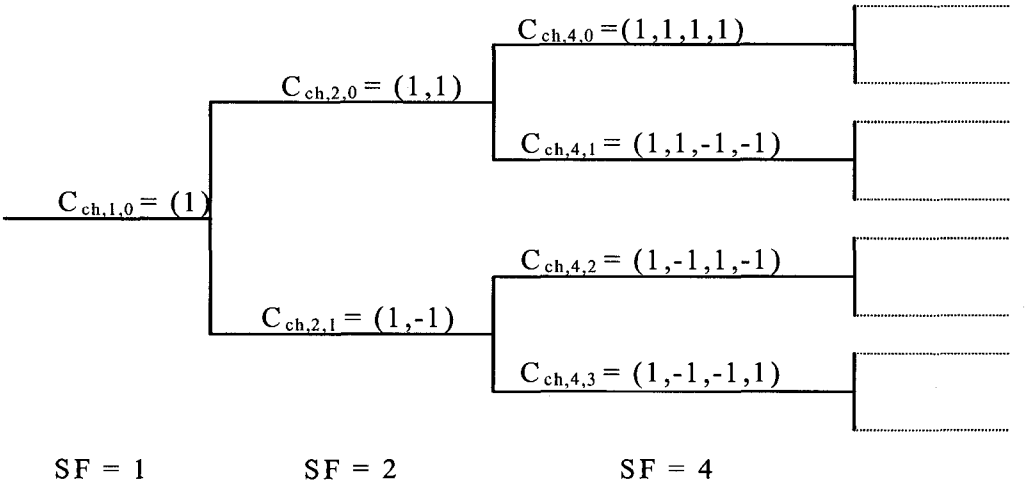


Figure 2.6: Code tree of OVSF codes

The available number of codes with a certain SF is equal to the value of the SF. The method to generate OVSF codes is shown using matrices in Equation (2.2).

In order to select codes from the code tree for physical channels, some rules have to be applied to ensure mutual orthogonality. For example, all codes with the same SF are orthogonal to each other. Two codes with different SFs are not orthogonal if the code with the higher SF can be constructed based on the code with the lower SF [34]. In WCDMA systems, the spreading factors of OVSF codes range from 4 to 256 for uplink and from 4 to 512 for downlink.

$$C_{ch,1,0} = 1$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2^{(n+1)},0} \\ C_{ch,2^{(n+1)},1} \\ C_{ch,2^{(n+1)},2} \\ C_{ch,2^{(n+1)},3} \\ \vdots \\ C_{ch,2^{(n+1)},2^{(n+1)}-2} \\ C_{ch,2^{(n+1)},2^{(n+1)}-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,2^n-1} \end{bmatrix} \quad (2.2)$$

2.6 Downlink Scrambling Code

Each cell in WCDMA systems is identified by its downlink scrambling code. A total number of 2^{18}-1 = 262,143 scrambling codes can be generated but not all of them are used. The selected scrambling codes are divided into 512 sets. Each set consists of one primary scrambling code and 15 secondary scrambling codes. Hence, totally 8192 scrambling codes can be used. The 512 primary scrambling codes are further divided into 64 code groups, and each group consists of 8 scrambling codes [33]. Each cell is allocated one and only one primary scrambling code. The downlink physical channels transmitted in a cell are scrambled by this cell's specific code so that they can be distinguished from the channel codes of other base stations even if the same set of channelization codes is used.

The scrambling code sequences are constructed by a combination of two real sequences. As defined in 3GPP, each of the two sequences is constructed by position-wise modulo 2 sum of two binary m-sequences (with length of 38400 chips) generated by means of two polynomials with degree 18. The resulting sequences thus constitute segments of a set of Gold sequences [33]. In order to match the length of the radio frames, the scrambling codes are repeated every 10 ms. The structure of the downlink scrambling code generator

is shown in Figure 2.7, where x and y are two m sequences respectively. The x sequence is constructed by using the primitive polynomial $1+X^7+X^{18}$. The y sequence is constructed by using the polynomial $1+X^5+X^7+X^{10}+X^{18}$. The downlink complex scrambling codes $S_{dl,n}$ are generated by the following algorithm.

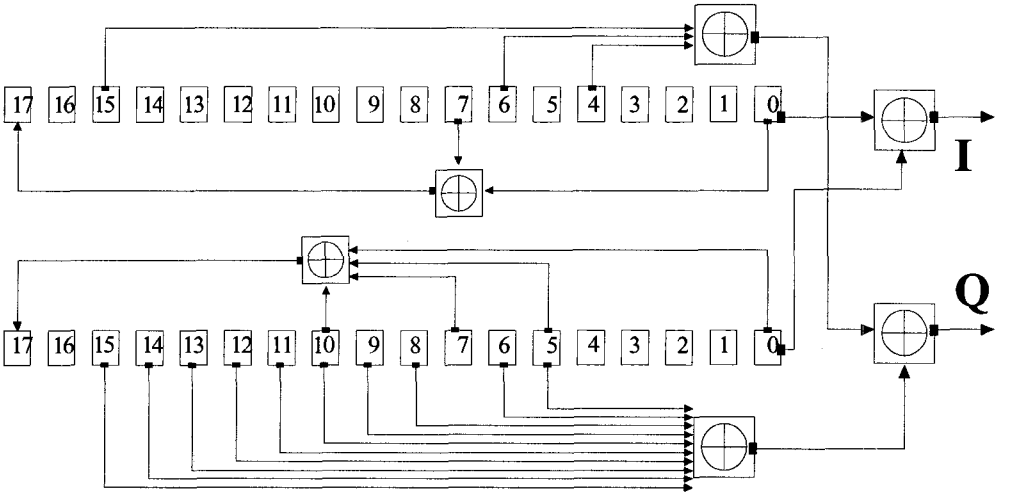


Figure 2.7: Structure of downlink scrambling code generator

The initial condition is set as

- x is constructed with x (0)=1, x(1)= x(2)=...= x (16)= x (17)=0.
- y(0)=y(1)= … =y(16)= y(17)=1.

The recursion for the subsequent symbols is given by

- $x(i+18) = x(i+7) + x(i)$ modulo 2, $i=0,\ldots,2^{18}-20$.
- $y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i)$ modulo 2, $i=0,\ldots, 2^{18}-20$.

The n-th Gold code sequence z_n, $n=0,1,2,\ldots,2^{18}-2$, is then defined as:

- $z_n(i) = x((i+n)$ modulo $(2^{18} - 1)) + y(i)$ modulo 2, $i=0,\ldots, 2^{18}-2$.

These binary sequences are then converted to real valued sequences Z_n by the following transformation:

$$Z_n(i) = \begin{cases} +1 & if\ z_n(i) = 0 \\ -1 & if\ z_n(i) = 1 \end{cases} \quad for \quad i = 0,1,\ldots,2^{18} - 2.$$

Finally, the n-th code of the downlink scrambling code set is created as:

- $S_{dl,n}(i) = Z_n(i) + j\, Z_n((i+131072) \text{ modulo } (2^{18}-1))$, i=0,1,...,38399.

2.7 Downlink Physical Channels

Three types of physical channels are used to facilitate cell search. They are P-SCH (Primary Synchronization Channel), S-SCH (Secondary Synchronization Channel) and CPICH (Common Pilot Channel) [35]. The P-SCH together with S-SCH is also referred to as the SCH (Synchronization Channel). Figure 2.8 illustrates the slot and frame formats of these channels. Each CPICH frame has 150 user data symbols. It is spread into 38400 chips (10 ms long), and these chips are divided into 15 slots. Thus, each slot consists of 2560 chips (0.67 ms long).

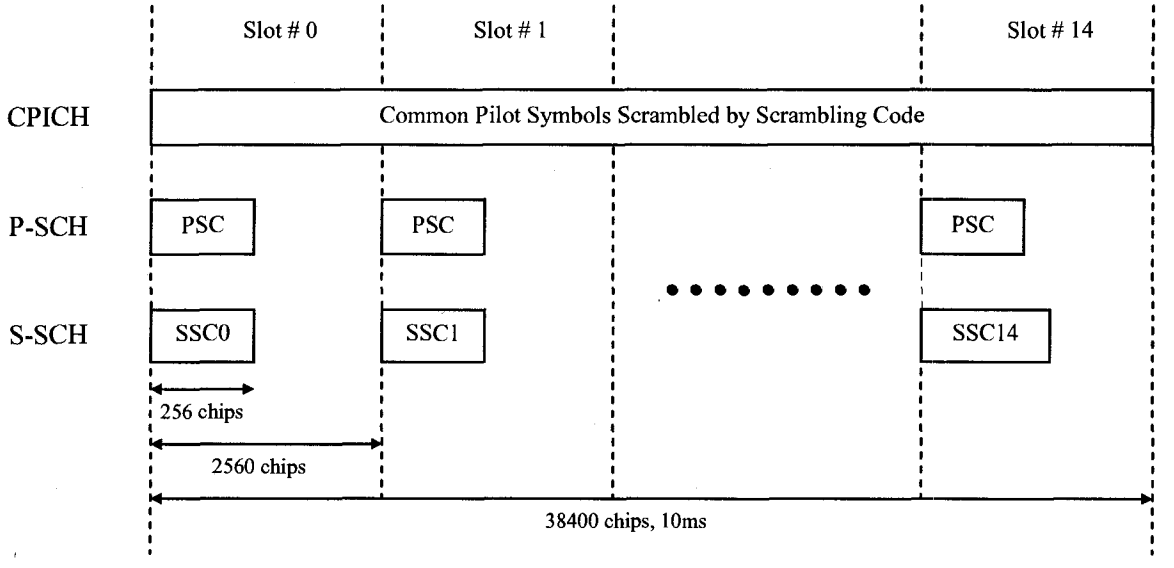


Figure 2.8: Frame and slot structures of P-SCH, S-SCH and CPICH

2.7.1 Common Pilot Channel

The Common Pilot Channel (CPICH) is used to carry the downlink common pilot symbols. It is scrambled by a cell-specific primary downlink scrambling code and is broadcasted over the entire cell. Each pilot symbol is QPSK (Quadrature Phase Shift Keying) modulated and is spread to 256 chips in order to fit the radio frame [36]. Figure 2.9 shows the frame structure of CPICH. Besides the help to cell search, CPICH provides a coherent phase reference for other downlink physical channels. It also aids in channel estimation for cell selection/reselection and handover. Thus, through changing power level of CPICH, the coverage and traffic load of a cell can be adjusted.

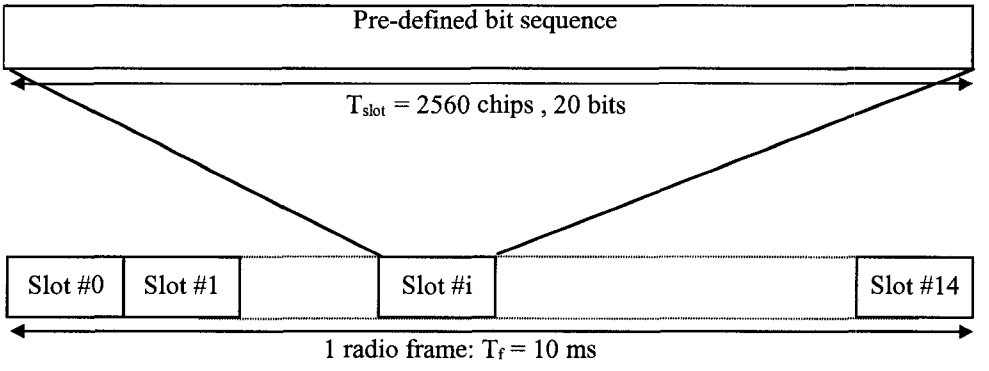


Figure 2.9: Frame structure of CPICH

The predefined bit pattern of CPICH used in this thesis is all "0"s.

2.7.2 Primary Synchronization Channel

Unlike CPICH, synchronization channels are not scrambled by the downlink primary scrambling code. They consist of P-SCH and S-SCH, and are specifically designed for cell search.

In Figure 2.8, we can see that the P-SCH consists of a sequence with 256 chips, and it is transmitted repeatedly at the beginning of every slot [36]. Thus, it can be used to detect the slot boundary of radio frames. The sequence transmitted on P-SCH carries a unique code called Primary Synchronization Code (C_{psc}). The C_{psc} is constructed as a so-called generalized hierarchical Golay sequence, which has good aperiodic auto-correlation properties [33]. The definition of C_{psc} is shown as follows:

- $a = \langle x_1, x_2, x_3, \ldots, x_{16} \rangle = \langle 1, 1, 1, 1, 1, 1, -1, -1, 1, -1, 1, -1, 1, -1, -1, 1 \rangle$
- $C_{psc} = (1 + j) \times \langle a, a, a, -a, -a, a, -a, -a, a, a, a, -a, a, -a, a, a \rangle$;

C_{psc} is generated by repeating a sequence modulated by Golay complementary sequence. It is constructed by a complex sequence with identically real and imaginary components. The method to search for C_{psc} and detect the slot boundary is usually the matched filter method that is used to match C_{psc} on the receiver. Since the C_{psc} sequence is same for every cell in the system, only one P-SCH matched filter is needed to detect the slot boundaries for all downlink radio frames [35].

2.7.3 Secondary Synchronization Channel

Secondary Synchronization Channel is transmitted in parallel with P-SCH at the beginning of each slot (see Figure 2.8). It carries Secondary Synchronization Codes (C_{ssc}) [33]. After detecting slot boundaries by matched filtering C_{psc}, the starting position of C_{ssc} is known. The next step is to decode the information carried on C_{ssc}.

Unlike the primary synchronization code, the secondary synchronization codes vary from slot to slot in one radio frame. There are 16 C_{ssc} sequences defined for S-SCH. They are

constructed from position wise multiplication of a Hadamard sequence with another sequence, z. The definition of z is shown as follows:

- z = <b, b, b, -b, b, b, -b, -b, b, -b, b, -b, -b, -b, -b, -b>, where
- b = <1, 1, 1, 1, 1, 1, -1, -1, -1, 1, -1, 1, -1, 1, 1, -1>

Hadamard sequences are obtained from the rows of a matrix H_k, which is constructed recursively as:

$$H_0 = (1)$$

$$H_k = \begin{pmatrix} H_{k-1} & H_{k-1} \\ H_{k-1} & -H_{k-1} \end{pmatrix}, \quad k \geq 1$$

The rows of the matrix are numbered from the top starting with row 0 and represented by sequence H_n (n = 0, 1, 2, …, 255). Then, 16 C_{ssc} sequences are defined as:

- $C_{ssc,k} = (1 + j) \times <H_m(0) \times z(0), H_m(1) \times z(1), H_m(2) \times z(2), \ldots, H_m(255) \times z(255)>$,

where m = 16×(k – 1) and k = 1, 2, 3, …, 16.

Different combinations of these 16 C_{ssc} sequences form a codebook with 64 codewords. Each codeword consists of 15 C_{ssc} sequences. Each C_{ssc} sequence has 256 chips. S-SCH transmits a complete codeword taken from the codebook in a single radio frame. The same codeword is repeatedly transmitted in each radio frame in a cell.

As mentioned above, 512 primary downlink scrambling codes are divided into 64 groups. In codebook, the 64 codewords correspond to 64 downlink scrambling code groups. In other words, a codeword carried on S-SCH indicates the code group identity of the downlink scrambling code used in a cell. Thus, S-SCH is used to acquire downlink

scrambling code group identity. Furthermore, these 64 codewords are chosen to have distinct code phase shifts. Any phase shift of a codeword is different from that of other codewords. The codes with this property are called CFRS (Comma free Reed-Solomon) codes [37]. Therefore, the frame boundary can be detected by identifying the phase shift of secondary synchronization code. The relation among secondary synchronization codes, downlink scrambling code groups, and radio frame slots are shown in Appendix A as Table A.1 [33].

2.7.4 Dedicated Downlink Physical Channel

DPCH (Dedicated downlink physical channel) is a physical channel carrying traffic for specific users on the downlink. It has time-multiplex structure of a DPDCH (downlink dedicated physical data channel) and a DPCCH (downlink dedicated physical control channel), as shown in Figure 2.10. Similar to CPICH, each DPCH frame is 10 ms long and divided into 15 slots. There are 2560 chips in each slot. A set of slot formats are also defined in 3GPP [36], which determines the number of bits in each field (N_{pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) of DPCH frame. Slot formats are given in Appendix B as Table B.1.

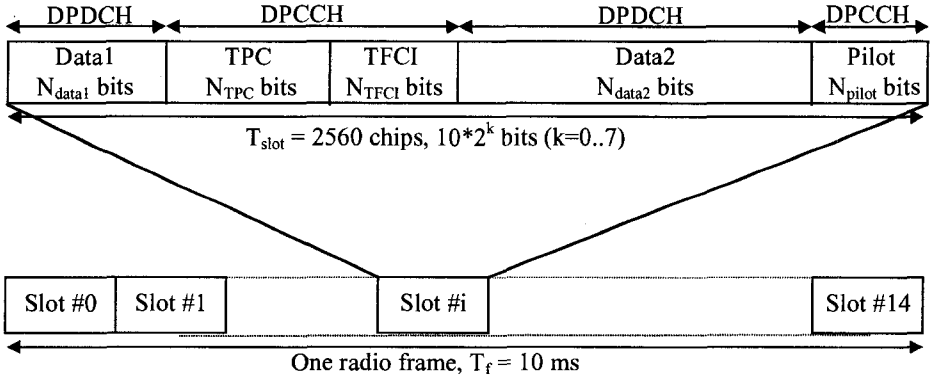


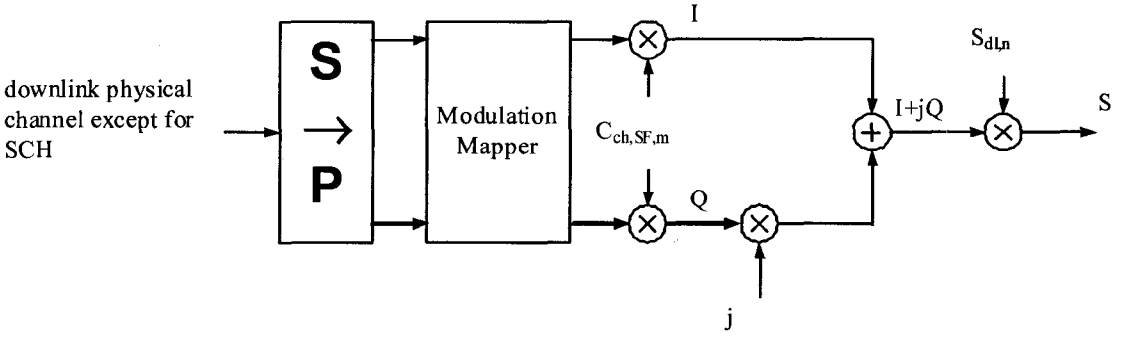
Figure 2.10: Frame structure of downlink DPCH

2.8 Downlink Physical Layer Operations

The downlink physical layer operations involved in this thesis include spreading and modulation.

2.8.1 Downlink Spreading

Spreading applied to downlink physical channels consists of two operations. The first is the channelization operation, which transforms the original data symbols into a number of chips. Mathematically, each original user data symbol is repeated SF times, and then multiplied with the corresponding OVSF code. Channelization increases the bandwidth of signal and separates the different physical channels. The second operation is scrambling operation, which is used to separate downlink transmissions from the different base stations without changing signal bandwidth further. It works based on the complex multiplication between the chips after channelization and the downlink scrambling code. The downlink spreading operation that includes channelization and scrambling is depicted in Figure 2.11 [33].



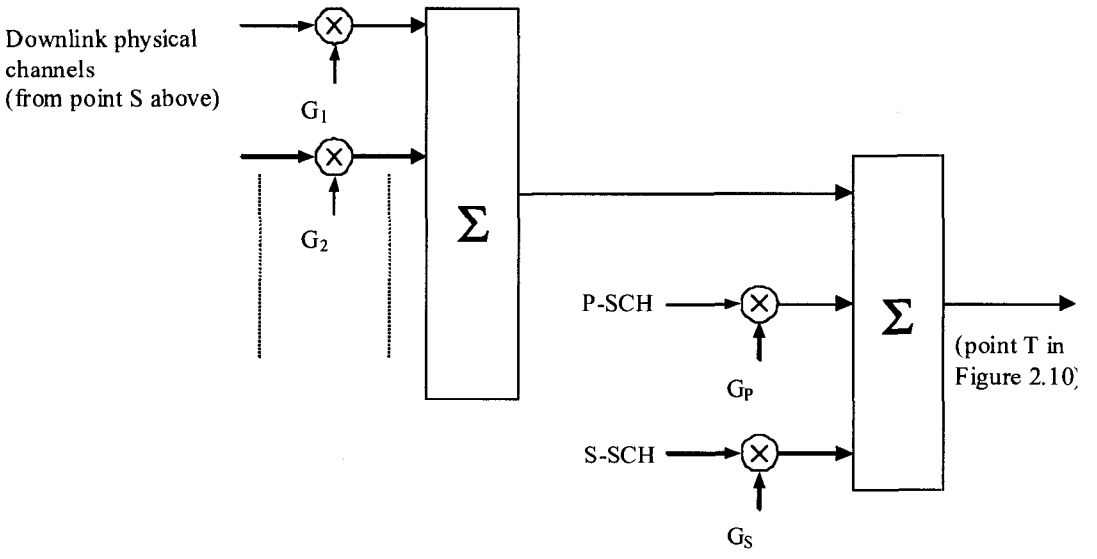


Figure 2.11: Downlink spreading

Each downlink physical channel consists of a sequence of real-valued symbols. Every two consecutive real-valued symbols (even and odd symbols) are first serial-to-parallel converted and they are mapped onto I and Q branches, respectively. The symbols on I and Q branches are then mapped to three values (i.e. +1, -1, 0) by modulation mapper. Real value +1 is mapped to binary value 0. Real value -1 is mapped to binary value 1. Real value 0 indicates Discontinuous Transmission (DTX). Then, I and Q branches are both spread to chip sequences with a rate of 3.84Mcps by the same real-valued channelization code. The summation of I and Q branches gives a complex-valued chip sequence. Different channels are spread with different channelization codes in order to maintain orthogonality to each other. The channelized chip sequence is then scrambled (complex chip-wise multiplication) by a complex-valued downlink scrambling code. As an exception, the spreading operation is not applied to SCH (P-SCH and S-SCH). After scrambling, all physical channels are weighted by their own weighing factors G_i, and are

combined by using complex addition. The P-SCH and S-SCH have their associated weighing factors, G_p and G_s.

2.8.2 Downlink Modulation

The complex-valued chip sequence generated by spreading operation is QPSK modulated as shown schematically in Figure 2.12, which is sent on air interface. The pulse shaping filter is a RRC (root raised cosine) filter with a roll-off factor equal to 0.22 [32]. The same type of RRC filter is deployed on base station and UE for modulation and demodulation.

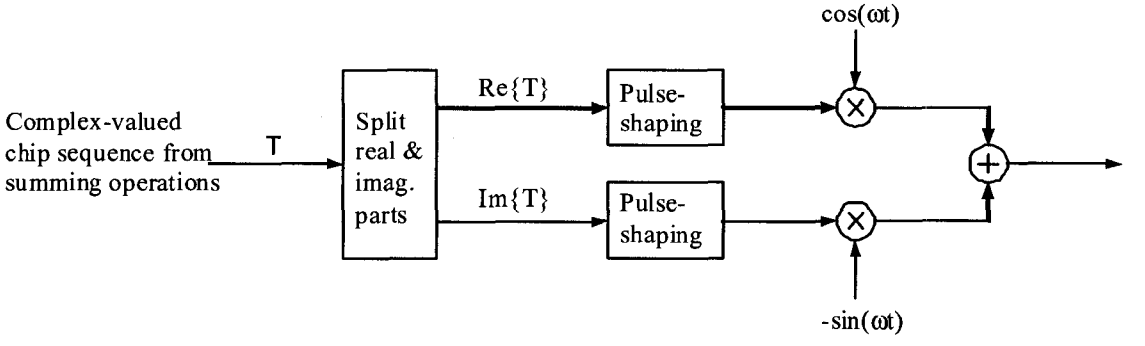


Figure 2.12: Downlink modulation

2.9 3GPP Cell Search Procedure

As mentioned earlier, in WCDMA systems, base stations are mutually asynchronous. In order to distinguish transmission from different cells, the 512 primary downlink scrambling codes are used for uniquely identifying cells in each cluster of 512 cells. These primary downlink scrambling codes can be reused among cell clusters. How to fast achieve a reliable synchronization with downlink scrambling codes is the main design

goal for cell search algorithms. 3GPP offers a basic cell search procedure which forms the basis of all enhanced schemes.

When a UE is switched on, it does not make an exhaustive search on all possible primary downlink scrambling codes. Instead, the total 512 code candidates are divided into 64 code groups. UE just needs to find out the correct scrambling code group identity based on the information transmitted on synchronization channels. This will significantly narrow down the searching scope. Thus, UE only performs a fine search in one code group, which contains only 8 code candidates. Therefore, the time spent on code acquisition can be reduced significantly, and users would not wait too long to see service-available indication on their UE. The cell search procedure defined in 3GPP contains three stages [35] as shown in the following.

1) Slot synchronization

During the first stage, the UE uses primary synchronization code transmitted on P-SCH to acquire slot synchronization. This is typically done by a matched filter matching to the primary synchronization code which is common to all cells. Since primary synchronization code is the same for each slot, slot timing can be obtained by detecting peaks in the output of matched filter.

2) Frame synchronization and code group identification

During the second stage, the UE uses secondary synchronization code transmitted on S-SCH to achieve frame synchronization and to identify the code group. This is done by correlating the received signal with all possible secondary synchronization code

sequences at the beginning of each slot and identifying the maximum correlation values. Since the cyclic shifts of code sequences are unique, code group identity as well as frame synchronization can be determined.

3) Scrambling code identification

During the third stage, the UE determines the exact primary scrambling code used by the cell. The primary scrambling code is typically identified through the symbol-by-symbol correlation between the received signal and all 8 code candidates within the code group identified in the second stage. After identifying the downlink primary scrambling code, the UE is able to decode the system and cell specific information from the broadcast channel.

2.10 Summary

In this chapter, the background information, such as radio propagating environment, spread spectrum and WCDMA air interface have been introduced. Some cell search related knowledge, such as channelization codes, downlink scrambling codes, synchronization channels and downlink spreading and modulation operations have also been presented. Furthermore, we have also briefly reviewed the three-stage cell search procedure defined by 3GPP. In the next chapter, the basic cell search algorithm, its enhanced versions and the proposed improved schemes will be presented.

Chapter 3: Cell Search Algorithms

The goal of this chapter is to design effective cell search algorithms, which are able to realize relatively a fast and accurate downlink scrambling code acquisition with reasonable computational complexity. The proposed algorithms are expected to be capable of counteracting the impacts of background noise, multipath fading, and simultaneous frequency and clock error, which always exist in practical communication systems.

In chapter 2, we have introduced cell search procedure defined by 3GPP. In this chapter, we will further detail the basic cell search algorithm, a conventional implementation of the 3GPP cell search procedure serving as the basis of other algorithms. Then, four existing enhanced cell search algorithms, which can improve the performance of the basic cell search algorithm under the impact of either frequency error or clock error, will be presented. In the last section, we will propose a few improved algorithms as different combinations of the four algorithms. We will also analyze and compare the proposed methods in terms of computational complexity.

3.1 Basic Cell Search Algorithm

The basic cell search algorithm originates from the work of Higuchi and Sawahashi [8]. It consists of three sequential stages and utilizes P-SCH, S-SCH and CPICH to acquire primary downlink scrambling code on the UE side. On the other hand, these three searching stages can also be performed concurrently in a pipelined fashion [38]. In

general, the pipelined search is faster than the sequential search at a price of higher hardware complexity and more power consumption. Our study only focuses on the sequential search. The flow chart of the basic cell search algorithm is depicted in Figure 3.1. The algorithm is tested over N frames of the buffered demodulated signal data. The searching operations are performed iteratively on a frame-by-frame basis. If the downlink scrambling code can be acquired correctly during the test of any of these data frames, the cell search is considered successful. Otherwise, a failed trial will be counted. The basic algorithm can be divided into three stages.

3.1.1 Stage 1: Slot Synchronization

After demodulation and matched filtering, the received complex-valued signal enters into the first stage of the cell search operation. A UE needs to determine the exact location of C_{psc} in order to detect slot boundary. This location is also the location of C_{ssc}. This is done by correlating the received signals with a locally generated replica of the C_{psc}. The correlation involves chip-wise multiplications and summations, which can be implemented using matched filters. The correlation operation is performed over 256 chips, which is a length of C_{psc}. There are 2560 chips in each slot. Apparently, each of these 2560 chip positions can be considered as a hypothesis of slot boundary. Therefore, 256-chip C_{psc} correlation needs to be performed for all 2560 hypotheses in one slot. The peaks of correlations then yield candidates of slot boundary. Furthermore, the correlation energies from multiple slots should be combined for each of the 2560 hypotheses in order to reduce the effect of noise and to exploit post-detection diversity combining [10].

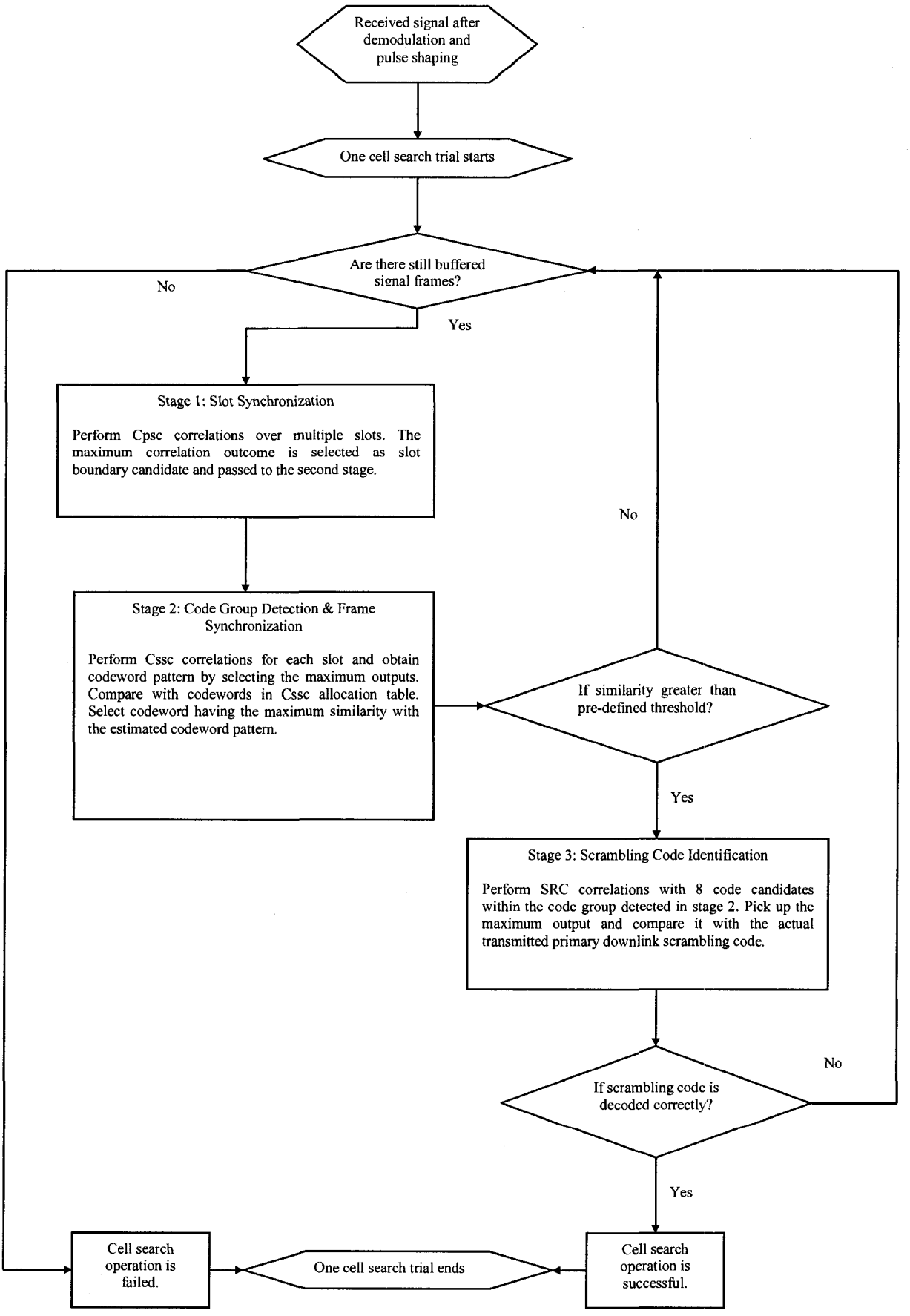
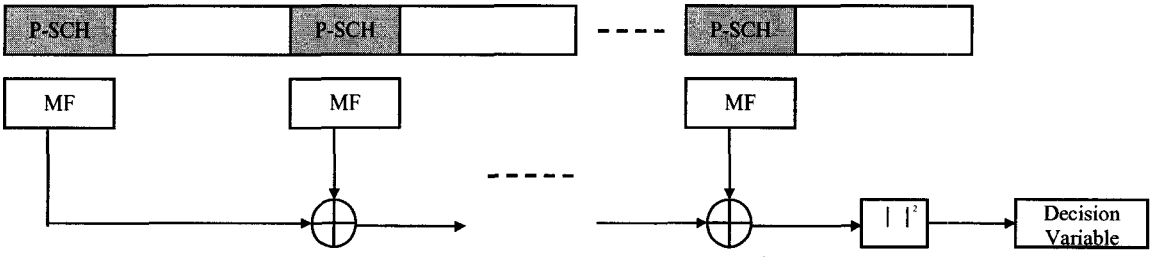


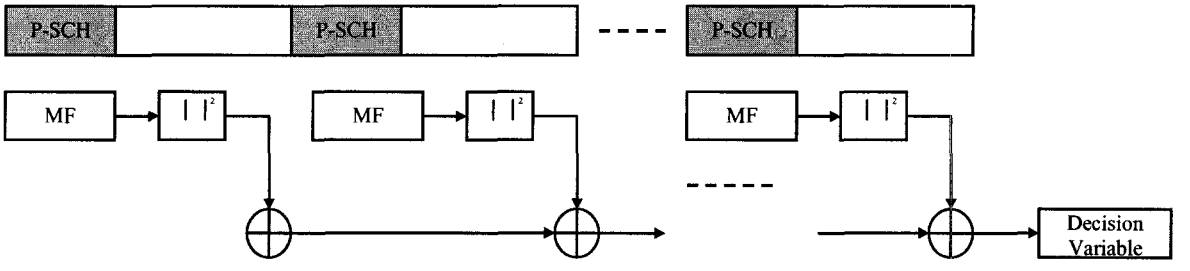
Figure 3.1: Flow chart of one trial of basic cell search algorithm

Finally, through selection of the maximum accumulated outcome after slot combining, the candidate of slot boundary can be figured out.

There are several slot combining schemes used in the first stage of cell search, e.g. coherent combining [39] and noncoherent combining [9]. Figure 3.2 (a) and (b) show the principle of these two schemes. Coherent combining combines outputs of matched filters over multiple slots before calculating the total instantaneous power (squaring), whereas noncoherent combining combines instantaneous power from multiple slots. Coherent combining outperforms the noncoherent combining in static and very slow fading environments. However, if the phase of the received signal is unpredictable due to multipath fading and frequency error, and if there is no compensation for phase rotation, noncoherent combining works better than the coherent combining.



(a) Coherent combining



(b) Noncoherent combining

Figure 3.2: Slot combining schemes

If T1 slots are combined in the first stage, for each of the 2560 hypotheses of slot boundary (beginning location of C_{psc}), the outputs of the matched filter, denoted by U_n ($1 \leq n \leq 2560$), are described in the following equation, where noncoherent combining is assumed,

$$U_n = \sum_{k=1}^{T1} \left| \sum_{j=1}^{256} Y_{j+Tk+n} \cdot C_{psc_j} \right|^2 \tag{3.1}$$

where Y is the received demodulated complex-valued baseband signal which is sampled with the chip rate, j is the index of the correlated chips, T=2560 is the length of one slot, which is also the interval between two consecutive combined slots, k is the index of the combined slots. The candidate of slot boundary M_{slot} is further obtained in Equation (3.2), by selecting the position of the maximum correlation output from the 2560 hypotheses. M_{slot} is then transferred to the second cell search stage in order to indicate the beginning position of C_{ssc} in each slot.

$$M_{slot} = \arg\max(U_n) \tag{3.2}$$

3.1.2 Stage 2: Code Group Identification and Frame Synchronization

As mentioned in Chapter 2, a total of 512 primary downlink scrambling codes are divided into 64 groups. In the second cell search stage, a UE needs to determine the code group identity by decoding C_{ssc} transmitted on S-SCH channel. This is done by correlating the received baseband signal with locally replicated C_{ssc} sequences. Correlations are performed at the beginning of each 15 slots with a length of 256 chips. Since there are 16

possible C_{ssc}, 16 correlations are needed to be performed for each of 15 slots in one signal frame. The relationship between correlations, slots and C_{ssc} is present in Table 3.1.

Table 3.1: Cssc correlation outcomes of one signal frame

	Slot 1	Slot 2	------	------	Slot 15
C_{ssc} 1	$V_1^{(1)}$	$V_2^{(1)}$	------	------	$V_{15}^{(1)}$
C_{ssc} 2	$V_1^{(2)}$	$V_2^{(2)}$	------	------	$V_{15}^{(2)}$
⋮	⋮	⋮	------	------	⋮
⋮	⋮	⋮	⋱		⋮
C_{ssc} 16	$V_1^{(16)}$	$V_2^{(16)}$		⋱	$V_{15}^{(16)}$

The outcomes of correlations, *Vs (r)* can be obtained as follows,

$$V_s(r) = \left| \sum_{j=1}^{256} Y_{j+Ts+M_{slot}} \cdot C_{ssc_j}^{r} \right|^2, \tag{3.3}$$

where, $r = 1, 2, \ldots, 16$ and $s = 1, 2, \ldots, 15$.

In the above equation, Y and T have the same meanings as in the first stage, s is the index of 15 slots in one signal frame, r is the index of 16 possible C_{ssc} sequences. The maximum outcomes of the 16 correlations are selected for each slot, as shown in Table 3.1. Shaded blocks represent the selected maximum C_{ssc} correlation outcomes. For example, for the first slot, the first sequence among the 16 possible C_{ssc} sequences has the largest outcome and is therefore selected. As a result, C_{ssc} codeword pattern transmitted on S-SCH can be estimated in one signal frame.

As shown in Chapter 2, all 64 possible C_{ssc} codewords can be hard-encoded into an allocation table as in Table 2.2. Each codeword in the table has 15 distinct phase shifts. The allocation table can be further extended by inserting all possible phase shifts of all 64 codewords. The new table contains 64 code sets and 960 (64×15) codewords. Each code set corresponds to one of the 64 code groups. In order to find out the code group identity of the transmitted downlink scrambling code, a UE needs to perform an exhaustively search in code table, and compare codewords with the estimated C_{ssc} code pattern obtained from Table 3.1. The purpose of the table extension is that after the first searching stage, a UE only has knowledge on slot boundary but not on the frame boundary. The C_{ssc} correlation can possibly start from any one of the 15 slots in one signal frame. The extended table contains all possible codeword patterns. If there is no impairment on downlink radio signal, theoretically, there must be one and only one pattern which can be found exactly to match the transmitted C_{ssc} codeword, no matter which slot the C_{ssc} correlation begin with. However, due to the impact of background noise, multipath fading, frequency and clock errors, the transmitted codeword estimated on a UE is very possibly not to exactly match any one of codeword patterns in the allocation table. Hence, a threshold is needed in the second searching stage in order to help decide which codeword is the most likely candidate of code group identity. In this work, the thresholding process is done by selecting the codeword from the allocation table, which has the maximum similarity with the estimated C_{ssc} sequence. In the mean time, the similarity needs to exceed a pre-defined value. If the threshold condition can be satisfied, the code group identity as well as the frame boundary are considered to be acquired. The code group identity will be transferred to the third searching stage. If the

threshold condition is not satisfied, and the buffered signal frames have not been run out, cell search process will go back to the beginning of the first searching stage and continue trials with the rest of signal frames. Otherwise, the cell search operation will be considered as failure.

3.1.3 Stage 3: Scrambling Code Identification

After acquiring the code group identity and the frame boundary, the downlink primary scrambling code can be identified by correlating the received baseband signal with eight possible scrambling codes in the identified code group. The correlation outputs W_i are calculated by

$$W_i = \left| \sum_{j=1}^{L} Y_{j+M\ slot} \cdot SRC_j^i \right|^2, \quad i = 1,2,...,8 \tag{3.4}$$

where Y is the received complex baseband signal, SRCs are scrambling codes in the identified code group (i is index of the codes), L=38400 is the length of one full frame and also the length of downlink scrambling code. Eventually, the downlink primary scrambling code is acquired by selecting the maximum correlation output. Due to all kinds of imperfections of radio environments, it is possible that the acquired downlink scrambling code on a UE is not the actual one transmitted from the base station. In this case, if the buffered signal frames have not been run out, the cell search process will jump back to the beginning of the first stage and continue searching with the rest of signal frames. Otherwise, cell search operation will be considered as failure. The function block diagram of the basic cell search algorithm is depicted in Figure 3.3.

3.1.4 Algorithmic Complexity

Short acquisition time and high detection probability are the goals of designing cell search algorithms. On the other hand, hardware complexity and power consumption are also important criteria to evaluate the effectiveness of the cell search algorithms. A good design should be such that a balance between the performance and the complexity is achieved.

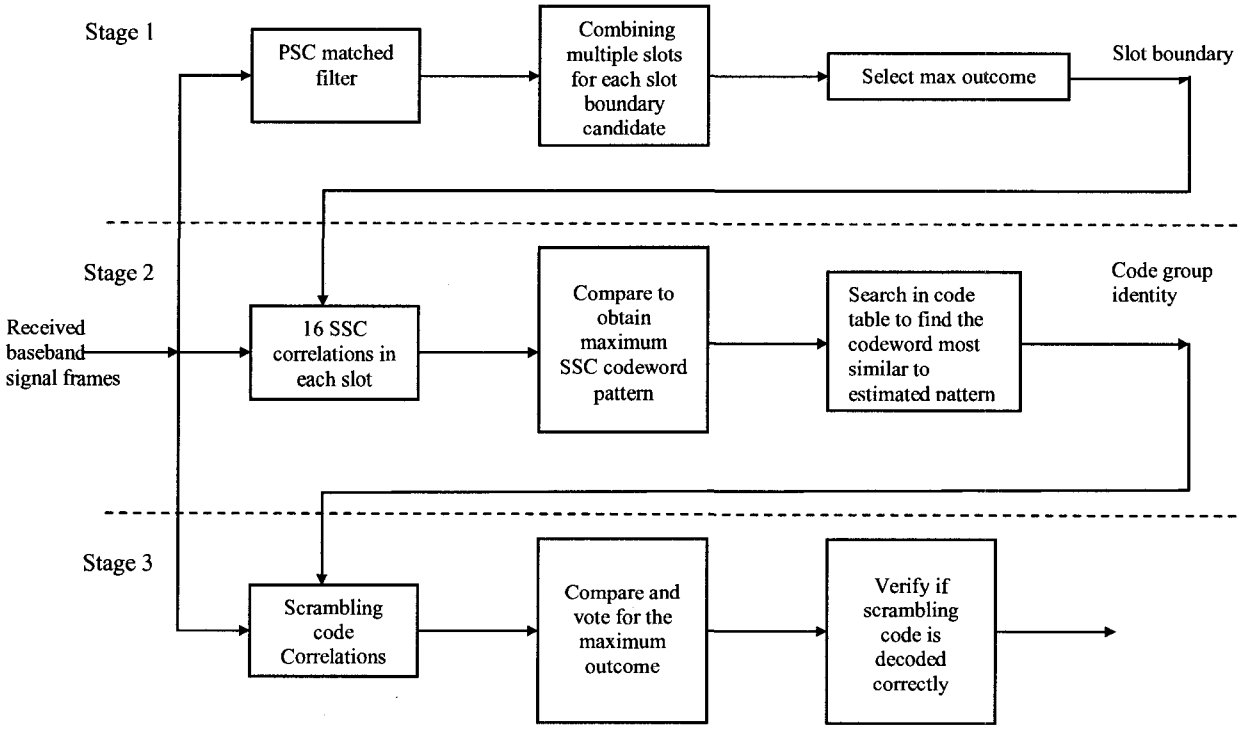


Figure 3.3: Function blocks of the basic cell search algorithm

The assessment of the implementation complexity and the actual power consumption is hardware-dependent. Our discussion is focused on algorithmic complexity which is based on calculations of the number of mathematical operations occurred during the process of a complete three-stage cell search trial (in one signal frame). The elementary operations are real-valued multiplications and additions. They are considered to have the same

algorithmic complexity. The operations applied in the basic cell search algorithm are complex-valued multiplications, comparisons, complex-valued squares and additions. In our calculation, we count one complex-valued multiplication as four real-valued multiplications and three additions. One complex-valued square is considered as two real-valued multiplications and one addition. One comparison is viewed as one elementary operation, namely, one multiplication or addition.

Assuming that the coherent slot combining is deployed in stage 1, the C_{psc} correlation consists of 256 complex-valued multiplications and 255 additions. Outputs are combined over 15 slots and then complex-valued squared. Since there are 2560 slot boundary candidates, the above operations are performed 2560 times. Then, 2560 comparisons are needed to find out the candidate with the maximum outcome. Accordingly, the number of operations in stage 1 can be measured as follows:

$$\text{Multiplications: } (4 \times 256 \times 15 + 2) \times 2560 = 39326720$$

$$\text{Additions: } [(3 \times 256 + 255 + 1) \times 15 + 1] \times 2560 = 39324160$$

$$\text{Subtotal: } 39326720 + 39324160 + 2560 = 78653440$$

In stage 2, the 256-chip long C_{ssc} correlation is performed for 16 C_{ssc} possible sequences on each of 15 slots. Correlation outcome of each C_{ssc} sequence is complex-valued squared. Then, $16 \times 15 = 240$ comparisons are needed to obtain the codeword pattern transmitted on S-SCH. This 15-digit codeword pattern is then compared with 960 possible codewords in the extended allocation table in order to find out the most likely downlink scrambling code group identity. The predefined similarity threshold needs also

to be verified. Therefore, (15+1) ×960 + 1 = 15361 comparisons are carried out. The number of operations in stage 2 is counted as:

$$\text{Multiplications: } (4 \times 256 + 2) \times 16 \times 15 = 246240$$

$$\text{Additions: } (3 \times 256 + 255 + 1) \times 16 \times 15 = 245760$$

$$\text{Subtotal: } 246240 + 245760 + 240 + 15361 = 507601$$

In stage 3, correlations are performed in the identified code group between all eight 38400-chip downlink scrambling codes and the received signal frame. The correlation outcomes are then complex-valued squared. Eight comparisons are needed to obtain the code candidate with the maximum outcome. Another comparison is performed to verify if the acquired code is correct. Thus,

$$\text{Multiplications: } (4 \times 38400 + 2) \times 8 = 1228816$$

$$\text{Additions: } (3 \times 38400 + 38399 + 1) \times 8 = 1228800$$

$$\text{Subtotal: } 1228816 + 1228800 + 8 + 1 = 2457625$$

We can see that the basic cell search algorithm with coherent combining in stage 1 requires a total number of operations as 78653440 + 507601 + 2457625 = 81618666.

When noncoherent slot combining is used in stage 1, the difference from the coherent combining is that the complex-valued square operations take place in each slot before the slot combining. Therefore, the number of operations in stage 1 is changed to:

$$\text{Multiplications: } (4 \times 256 + 2) \times 15 \times 2560 = 39398400$$

$$\text{Additions: } (3 \times 256 + 255 + 1 + 1) \times 15 \times 2560 = 39360000$$

$$\text{Subtotal: } 39398400 + 39360000 + 2560 = 78760960$$

3.2 Enhanced Cell Search Algorithms

It is required in 3GPP that the demodulating carrier frequency of a UE be accurate within ±0.1 ppm (parts per million) compared to the carrier frequency used by the base station [32]. However, in practical applications, cheap oscillators with inaccuracy up to 12 ppm are commonly employed in UEs in order to save manufactural cost. The imperfection of cheap oscillators may lead to a large frequency offset between a UE and a base station, which is even larger than 20KHz on 2GHz carrier frequency [26]. The frequency error not only impacts the quality of demodulation but also results in phase rotations in the receiver side. The inaccuracy of oscillator also incurs clock error on an UE, which drifts sampling points away from the correct positions sometimes even by more than one chip. The frequency error, clock error together with the multipath fading and background noise may cause serious failure in cell search process.

The basic cell search algorithm is intended for ordinary fading scenarios and it does not take into account the impact of frequency error and clock error. In this chapter, four enhanced cell search algorithms which are designed to deal with either frequency error or clock error are introduced. They are PSD, DDCC, STS-1 and RSPT algorithms. It should be noted that these four algorithms are not able to deal simultaneously with the frequency and clock errors. Since they are the basis of the proposed and combined algorithms, a detailed description with the analysis of their computational complexities is necessary.

3.2.1 Partial Symbol De-spreading

Partial Symbol De-spreading (PSD) is an enhanced cell search algorithm proposed by Y. P. Eric Wang [9]. It can be used to overcome the frequency error. The carrier phase rotation generated by the frequency error results in coherence loss. It also degrades the efficiency of the processing gain if C_{psc} correlation is carried out with a length of 256 chips in the first cell search stage [26].

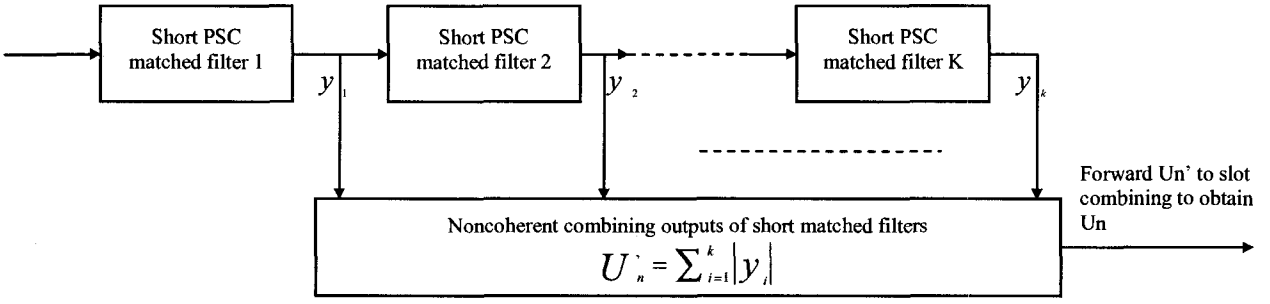


Figure 3.4: Concatenated short PSC matched filters

In order to alleviate this problem, the phase rotation can be partitioned into several small restrained segments. In another other words, the regular C_{psc} matched filter can be divided into several concatenated shorter matched filters. The concatenation of C_{psc} matched filters is illustrated in Figure 3.4. For each slot boundary candidate, instead of correlating the received signal with C_{psc} sequence for 256 chips, the C_{psc} sequence is divided into K short sequences with a length of M (M=256/K). Each short C_{psc} sequence correlates the received signal chips for the same length M. The outputs of short matched filters are noncoherently combined in order to mitigate the phase rotation by preventing it from propagating across the matched filters. Noncoherent accumulation of outputs from the short matched filters is then forwarded to noncoherent slot combining block as shown in Figure 3.3. The rest of the process is the same as that in the basic cell search algorithm.

The length of C_{psc} short sequences, M, should be optimized to obtain a compromise, since a smaller value of M results in less phase rotation but it may also weaken the noise suppression ability. It has been recommended that the most suitable value of M is 64 for initial cell search [9]. Thus, the matched filtering in stage 1 includes four concatenated filters. The number of operations in stage 1 can be counted as:

$$\text{Multiplications: } (4 \times 64 \times 4 + 2 \times 4 + 2) \times 15 \times 2560 = 39705600$$

$$\text{Additions: } (3 \times 64 \times 4 + 63 \times 4 + 1 \times 4 + 1 + 1) \times 15 \times 2560 = 39398400$$

$$\text{Subtotal: } 39705600 + 39398400 + 2560 = 79106560$$

The number of operations in stage 2 or stage 3 is the same as that in the basic algorithm.

3.2.2 Differential Detection and Coherent Combining

As mentioned above, the noncoherent slot combining in cell search stage 1 performs better than the coherent slot combining if phase rotations caused by the multipath fading and frequency error are not compensated. However, its performance may become poor because of the noncoherent combining loss when the accumulative value of multiple combined slots is high [40]. Since differential detection does not need prior knowledge about carrier phase Yeon [19], it provides a compensation to phase rotations in stage 1. In another words, an enhanced cell search algorithm can be proposed by blending the differential detection and coherent combination. The principle of Differential Detection and Coherent Combining (DDCC) is illustrated in Figure 3.5. The phase reference of the output of the current matched filter is provided by the output of the previous matched filter.

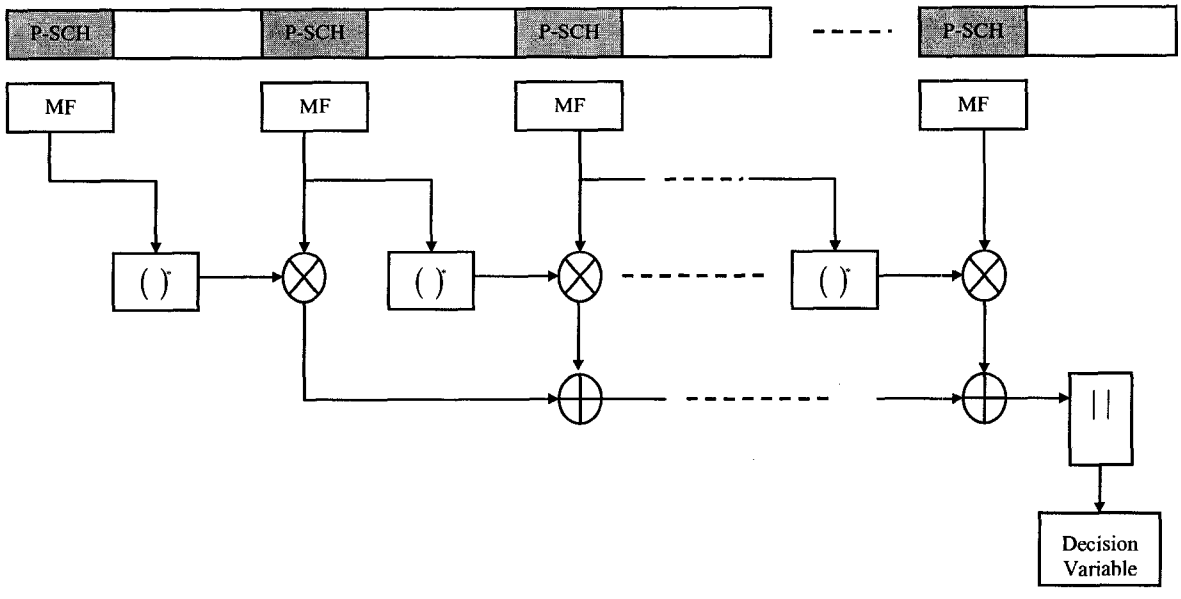


Figure 3.5: Differential detection and coherent slot combining

Comparing with the noncoherent and coherent combining schemes depicted in Figure 3.2, the decision variable of the slot boundary candidate U_n can be represented as

Coherent
$$U_n = \left| \sum_{k=1}^{L} Z_{nk} \right|^2 \tag{3.5.1}$$

Noncoherent
$$U_n = \sum_{k=1}^{L} \left| Z_{nk} \right|^2 \tag{3.5.2}$$

Differential
$$U_n = \left| \sum_{k=1}^{L} Z^*_{n(k-1)} \cdot Z_{nk} \right| \tag{3.5.3}$$

In the above equations, Z_{nk} is the output of C_{psc} matched filter, which is combined over L slots. The asterisk in Equation (3.5.3) represents the complex-conjugate operation. Different from the coherent combining, instead of directly accumulating outputs of matched filters over multiple slots, each matched filter obtains a phase reference differentially by multiplying its output with a complex conjugation of the output of the

previous matched filter. Then, an envelop detection, which collects the signal energy from both real and imaginary parts simultaneously, is employed to form a decision variable after the coherent accumulation of differential terms over multiple slots. Since the differentially coherent combining is able to compensate for phase rotation locally at receiver without requiring phase estimation, DDCC is an effective scheme to cope with the frequency error and multipath fading. In the mean time, it retains the benefit from coherent combining, which helps the background noise suppression [41].

Operations in stages 2 and 3 of the DDCC algorithm are exactly the same as those in the basic algorithm. In search stage 1, for each of 2560 slot boundary candidates, the outputs of matched filters of the adjacent slots are conjugatedly multiplied. Then, 14 products are coherently combined over one signal frame. One conjugation and one envelope detection (square root) can be both managed as one elementary operation. Therefore, $14 \times 2560 = 35840$ conjugations and 2560 square roots are needed. The number of operations in stage 1 can be measured as:

$$\text{Multiplications: } (4 \times 256 \times 15 + 4 \times 14 + 2) \times 2560 = 39470080$$

$$\text{Additions: } (3 \times 256 \times 15 + 3 \times 14 + 14 + 1) \times 2560 = 29637120$$

$$\text{Subtotal: } 39470080 + 29637120 + 35840 + 2560 + 2560 = 69148160$$

3.2.3 Serial Test in Stage 1

Besides the frequency error, the inaccuracy of oscillator on a UE causes clock error. Clock error could generate a sampling uncertainty up to one chip after demodulation.

This sampling jitter may lead to a total failure to the cell search process. The Serial Test in Stage 1 (STS-1) algorithm was proposed by Mario Kiessling as an approach to reduce the impact of clock error [23].

Unlike the basic cell search algorithm, in STS-1, the received baseband signal is oversampled with an oversampling rate N (N>2) before entering cell search stage 1, instead of performing chip-rate sampling after demodulation. In other words, N relevant data samples are interpolated into one original chip duration. Apparently, timing resolution of the received baseband signal is increased N times. Therefore, after oversampling operation, there are $N \times 38400$ chips in one signal frame. After entering search stage 1, the extended signal frame is evenly split into N parallel data frames. There are still 38400 chips in each of these new frames. The new frames are fed into the C_{psc} matched filter and tested serially in order to reduce the complexity. Similar to that in the basic algorithm, each frame generates its most likely slot boundary candidate by C_{psc} correlations and noncoherent slot combining. Among N selected slot boundary candidates, the one with the maximum accumulation value is finally selected and forwarded to cell search stage 2 and stage 3 as the slot timing reference. Only the data frame corresponding to the best slot boundary candidate is used in stage 2 and stage 3 for further processing. Oversampling and selecting of the best slot boundary candidate among oversampled frames in searching stage 1 would make cell search process more robust under clock error and lower signal to noise ratio (SNR).

Assuming that the oversampling rate N is 4, one signal frame is extended to four new frames for processing in searching stage 1. Comparing to the basic algorithm, the number of operations is fourfold in stage 1. Also, there are four extra comparisons needed to find out the best slot boundary candidate among the four data frames. The number of operations of stage 2 or stage 3 is the same as that in the basic algorithm. The oversampling operations occur before stage 1, which is a kind of preprocessing and has not taken into account the algorithmic complexity of the cell search process. However, it should be noted that the oversampling increases overall complexity of the UE implementation. Therefore, for stage 1 of STS-1 algorithm, the number of operations can be estimated as:

$$\text{Subtotal: } 78653440 \times 4 + 4 = 314613764$$

The value 78653440 in the equation was calculated in Section 3.1.4.

3.2.4 Random Sampling per Trial

Random Sampling per Trial (RSPT) is another method to mitigate the impact of clock error, which was proposed by Wern-Ho Sheen [22]. Like the STS-1 algorithm, RSPT requires oversampling operation before the search stage 1 in order to increase the timing resolution and detection probability. The oversampled frame is then evenly split into several new data frames. However, instead of serially correlating all new frames, the RSPT randomly picks up one frame and processes it in cell search stages. If the current cell search trial is not successful, the RSPT will again randomly select one data frame from the next set of oversampled frames and start the next cell search trial. This random

sample-selecting process is repeated trial by trial until the downlink scrambling code gets acquired, or until all signal frames are run out. Due to random sampling, the different sampling points can be possibly used in each trial. Thus, there are more opportunities for a UE to get good samples for cell search process. Comparing to STS-1, the RSPT does not need to process all oversampled frames in search stage 1. Therefore, its number of operations in cell search stage 1, stage 2 or stage 3 is exactly the same as that in the basic algorithm with noncoherent combining.

3.3 Improved Cell Search Algorithms

In practice, the frequency and clock errors are almost always present simultaneously on a UE. Very little work in the existing literature has dealt with these two problems at the same time. Therefore, there is an urgent need to develop an improved algorithm that is able to counteract both severe impacts simultaneously. In this study, we attempt to combine the four enhanced algorithms discussed above to obtain effective integrated solutions. Our idea is to combine together one anti-frequency-error algorithm and one anti-clock-error algorithm. Therefore, we get four possible combinations, which are PSD + STS-1, PSD + RSPT, DDCC + STS-1 and DDCC + RSPT. In contrast to the basic cell search algorithm, the improvements of the combined algorithms lie mainly in search stage 1.

The process of stage 2 or stage 3 remains the same as that in the basic algorithm. Thus, the algorithmic complexity of stage 2 and stage 3 of new combinations should also be the same as in the basic algorithm.

3.3.1 PSD + STS-1

The conceptual diagram of PSD + STS-1 algorithm, showing the functional blocks of the preprocessing stage and the search stage 1, is depicted in Figure 3.6. The incoming signal frames are oversampled N times in order to increase the sampling resolution. The oversampled symbols are then evenly split into N new frames. As an example of oversampling operation, we assume that the original frame sequence is represented as (A B C). After the oversampling operation, the new sequence is (A_1 A_2...A_N, B_1 B_2...B_N, C_1 C_2...C_N). The splitting operation generates N new sub-sequences as (A_1 B_1 C_1), (A_2 B_2 C_2), ... , and (A_N B_N C_N).

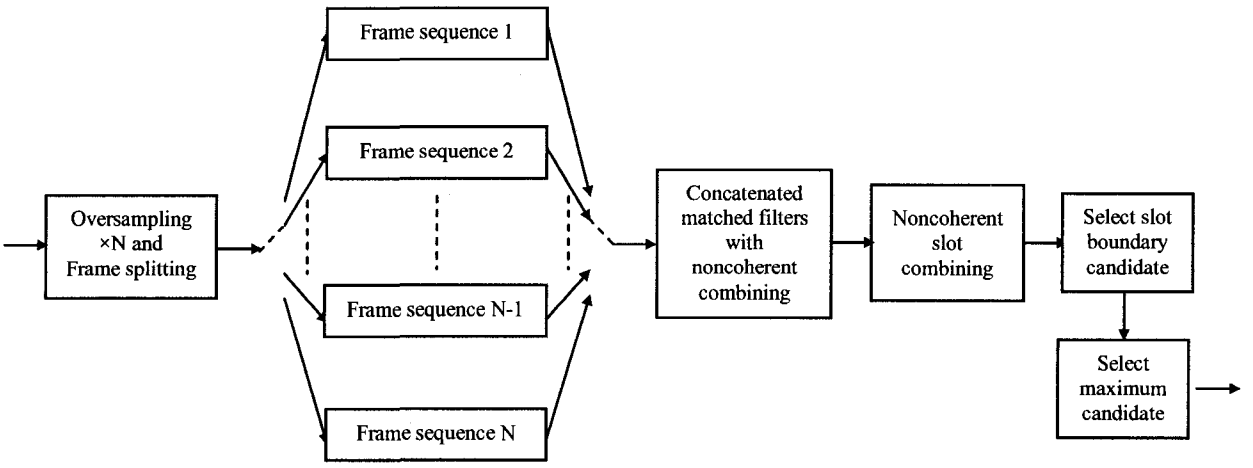


Figure 3.6: Conceptual diagram of PSD + STS-1 algorithm in cell search stage 1

These N new frame sequences are then processed one by one serially in search stage 1. In each frame, C_{psc} matched filtering takes place for all 2560 slot boundaries in every slot. Each 256-chip matched filter is segmented into four short-length filters. The correlation outcomes of the four concatenated short filters are noncoherently combined to form the outcome of C_{psc} matched filter. Then, the coherent combining is performed among each slot of the signal frame in order to further compensate phase rotations. All the above-mentioned processes are performed for 2560 slot boundary candidates. The outputs of the

candidates are compared and then slot boundary of each of the N signal frames is selected. Finally, the selected slot boundaries from the N frames are compared together and the one with the maximum correlation value is selected. This selection is transferred to stage 2 and stage 3 for the further processing.

We assume that the oversampling rate is 4. Comparing to the single PSD process described in subsection 3.2.1, the number of operations in searching stage 1 is increased four times. Besides, four extra comparisons are needed to select the maximum slot boundary candidate. Therefore, the number of operations in stage 1 can be counted as:

$$\text{Subtotal: } 79106560 \times 4 + 4 = 316426244$$

The value 79106560 in the equation was calculated in Section 3.2.1.

3.3.2 PSD + RSPT

The conceptual diagram of PSD + RSPT algorithm is depicted in Figure 3.7.

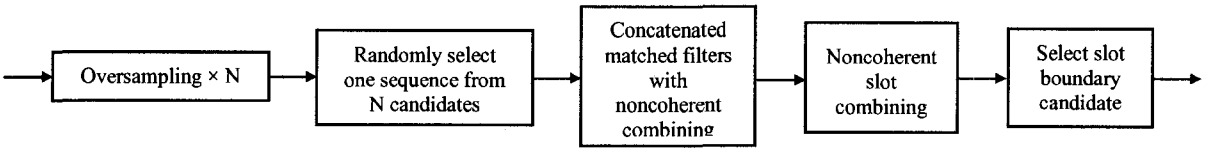


Figure 3.7: Conceptual diagram of PSD + RSPT algorithm in cell search stage 1

After oversampling, one original signal frame generates N new frames. The sampling resolution is increased. In stead of serially processing these frames, only one frame will be randomly selected and passed to C_{psc} matched filter. This random selection will increase the possibility for a UE to avoid selecting a wrong slot boundary, especially when there is a high background noise in the radio propagation environment. The rest of the processing is the same as the PSD, which segments the C_{psc} matched filter into concatenated short filters and noncoherently combines outputs of filters.

The RSPT algorithm does not increase algorithmic complexity in cell search stage 1. Therefore, the number of operations in search stage 1 is the same as in PSD algorithm as follows.

Subtotal: 79106560

3.3.3 DDCC + STS-1

The conceptual diagram of DDCC + STS-1 algorithm is depicted in Figure 3.8. Oversampled N signal frames are serially processed. Each frame passes C_{psc} matched filter. Correlations occur at the same positions of each slot. Output of each slot is multiplied with conjugate of the output of the previous slot in order to compensate phase rotation. The productions of all multiplications are then coherently combined in order to further alleviate phase rotation and suppress back ground noise. The slot boundary candidates obtained from all N frames are compared together. The one with the maximum correlation value is selected as the slot boundary and transferred to searching stage 2 and stage 3 for the further processing.

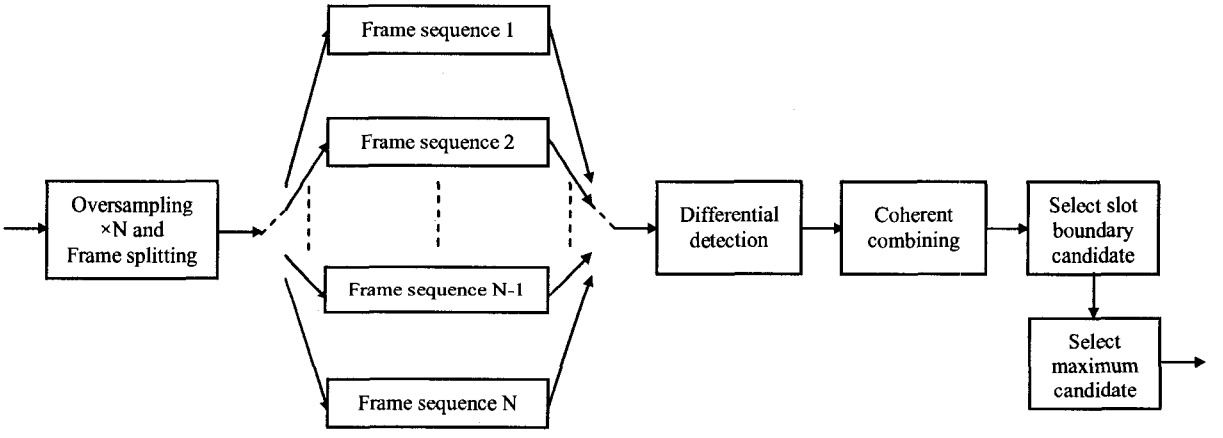


Figure 3.8: Conceptual diagram of DDCC + STS-1 algorithm in cell search stage 1

We assume that oversampling rate is 4. Comparing to the single DDCC process described in subsection 3.2.2, the number of operations of DDCC + STS-1 algorithm in searching stage 1 is increased four times. Four extra comparisons are also needed to select the maximum slot boundary candidate. Thus, the number of operations in stage 1 can be calculated as:

$$\text{Subtotal: } 69148160 \times 4 + 4 = 276592644$$

The value 69148160 in the equation was calculated in Section 3.2.2.

3.3.4 DDCC + RSPT

The conceptual diagram of DDCC + RSPT algorithm is depicted in Figure 3.9. After oversampling and random selection of one sample, only one signal frame is passed into the C_{psc} matched filter. The rest of the processing of search stage 1 is the same as the pure DDCC processing.

The number of operations in stage 1 of DDCC + RSPT algorithm is the same as in DDCC algorithm, and can be counted as:

$$\text{Subtotal: } 69148160$$

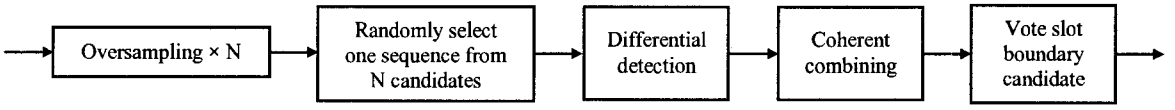


Figure 3.9: Conceptual diagram of DDCC + RSPT algorithm in cell search stage 1

3.4 Complexity Comparison of Cell Search Algorithms

The computational complexity of the cell search algorithms discussed above are summarized in Table 3.2.

Table 3.2: Computational complexities of cell search algorithms

	Stage 1	Stage 2	Stage 3	Total
Basic (coherent)	78653440	507601	2457625	81618666
Basic (noncoherent)	78760960	507601	2457625	81726186
PSD	79106560	507601	2457625	82071786
DDCC	69148160	507601	2457625	72113386
STS-1	314613764	507601	2457625	317578990
RSPT	78760960	507601	2457625	81726186
PSD+STS-1	316426244	507601	2457625	319391470
PSD+RSPT	79106560	507601	2457625	82071786
DDCC+STS-1	276592644	507601	2457625	279557870
DDCC+RSPT	69148160	507601	2457625	72113386

It can be found that the complexity of the DDCC algorithm is lower than that of the PSD algorithm. The STS-1 algorithm is much more complex than the RSPT algorithm. Since RSPT does not increase the complexity in any of the three cell search stages, DDCC + RSPT algorithm has the least complexity comparing to other combined algorithms, whereas PSD + STS-1 are the most complicated one.

3.5 Summary

In this chapter, the basic three-stage cell search algorithm with coherent and noncoherent slot combining is presented. The slot boundary of the incoming signal frames is obtained in the first search stage by C_{psc} matched filtering. In stage 2, the downlink scrambling code group identity and the frame boundary are acquired by correlating C_{ssc} carried on S-SCH. After the searching scope is narrowed down into one of 64 code groups, the

downlink scrambling code is identified in search stage 3 by correlating the signal frame with the codes in the selected code group. Applying this cell search scheme, a UE is able to achieve a fast cell search instead of scanning all 512 possible primary downlink scrambling codes. We have also introduced four enhanced algorithms designed to secure cell search performance under either frequency or clock error. Among them, PSD and DDCC are used to alleviate frequency error while STS-1 and RSPT are used to mitigate the clock error. Since none of the existing solutions can handle both frequency error and clock error at the same time, we have proposed to combine these enhanced schemes in pairs in order to improve the performance. The algorithmic complexity of all the cell search algorithms has been discussed.

In the next chapter, we will evaluate and compare the performance of the cell search algorithms presented in this chapter through computer simulations.

Chapter 4: Simulation and Performance Evaluation

In this chapter, we simulate the cell search algorithms presented in Chapter 3 and compare and analyze their performance in terms of the mean acquisition time and detection probability. Different radio propagation environments with both the frequency and clock errors are taken into account in our simulation study of the existing as well as the proposed cell search algorithms.

4.1 Simulation Setup

Matlab is used to simulate the cell search algorithms. In our simulations, the radio propagation environment considered includes the AWGN, and three types of multipath fading cases as specified in 3GPP [32], i.e. Case 1: Indoor (3km/h), Case 2: Indoor to Outdoor and Pedestrian (3km/h) and Case 3: Vehicular (120km/h). These multipath scenarios are listed in Table 4.1. Each of them consists of a moving speed, a relative delay and relative mean power.

Table 4.1: Propagation conditions for multipath fading environments case 1, case 2 and case 3

Case 1		**Case 2**		**Case 3**	
Speed 3 km/h		Speed 3 km/h		Speed 120 km/h	
Relative Delay [ns]	Relative Power [dB]	Relative Delay [ns]	Relative Power [dB]	Relative Delay [ns]	Relative Power [dB]
0	0	0	0	0	0
976	-10	976	0	260	-3
		20000	0	521	-6
				781	-9

Figure 4.1 depicts the radio propagation channel condition with multipath fading and AWGN. In this figure, the transmitted signal frames pass through a multipath fading generating block that comprises multiple independent time-variant Rayleigh fading components. The relative mean power gain g_n and time delay Rn applied on each component are defined in Table 4.1. Rayleigh fading components are implemented based on Clarke and Gans fading model [28]. The AWGN background noise is added after combining multiple faded signal paths.

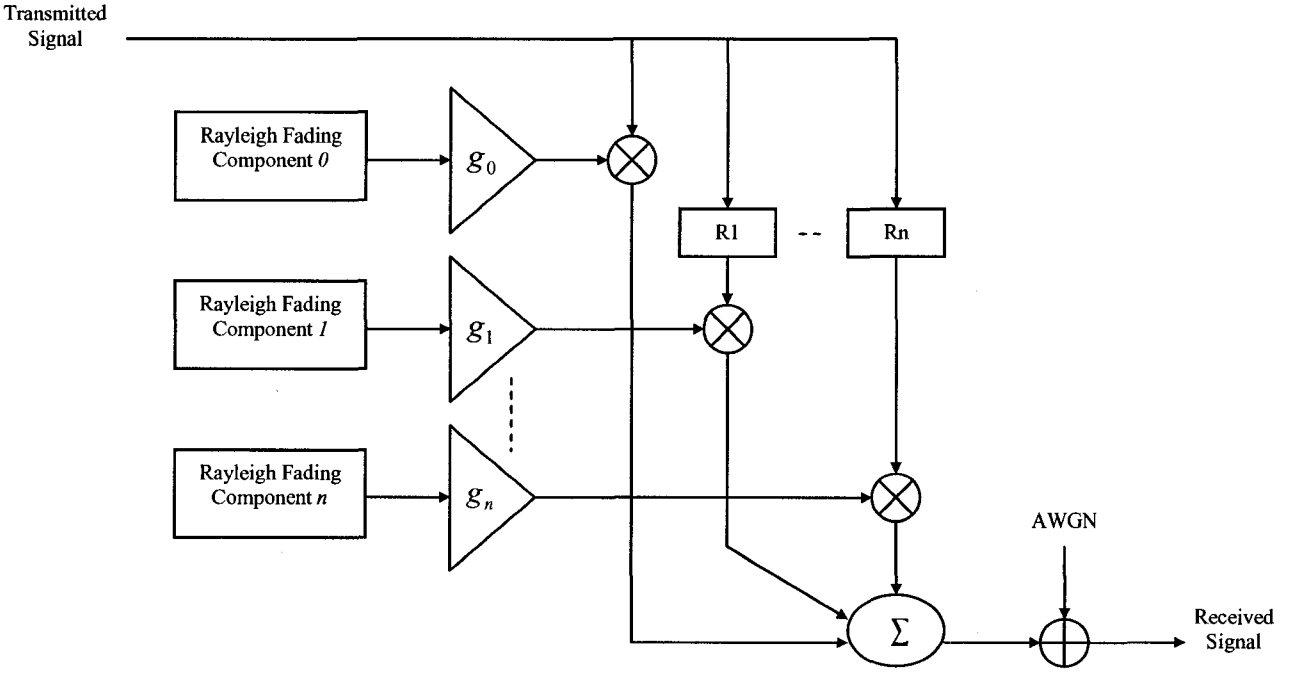


Figure 4.1: Radio propagation condition with multipath fading and AWGN

For simplicity, we only simulate a system with one UE and one base station. The UE receives signal frames from the base station on the downlink. The simulated downlink physical channels are CPICH, P-SCH, S-SCH and one DPCH with slot format 4. As described in Chapter 2, The CPICH and DPCH are spread with different channelization

codes. Code $C_{256,0}$ is used for CPICH, and $C_{256,2}$ is used for DPCH. The CPICH and DPCH are weighted by their own power gain factors after being scrambled by the primary downlink scrambling code chosen from the 512-code cluster. The two channels are transmitted with the same power. They are then combined with P-SCH and S-SCH. Different from the CPICH and DPCH, the P-SCH and S-SCH are transmitted at a half power. Next, the combined signal goes through pulse shaping filter and modulator, which is then QPSK-modulated at carrier frequency (2.17 GHz). After passing through the radio propagation environment with multipath fading and AWGN noise, the received signal is demodulated and fed into pulse shaping filter. This is the same as the one used in transmitter. Eventually, the demodulated baseband signal frames enter cell search function blocks, and the three-stage cell search process starts.

4.2 Performance Evaluation

4.2.1 Metrics

The performance evaluation is based on two metrics, mean acquisition time and detection probability. Mean acquisition time is the time taken by a UE to perform one successful three-stage cell search trial. It indicates how fast an UE can acquire the downlink scrambling code. Detection probability is the ratio of the number of successful cell search trials to the total number of trials. It represents the reliability of a cell search algorithm.

For each radio propagation condition listed in Table 4.1, cell search trials are performed on a series of selected SNR levels. AWGN and multipath fading impairments are

randomly injected in downlink signal frames with a selected SNR level. For each SNR level, 1000 trials are performed in order to get statistical averages. Twenty signal frames are provided for each trial. If the downlink scrambling code still cannot be acquired correctly after testing on these twenty frames, the cell search is considered to fail for this trial. At each SNR level, only successful cell search trials are counted for the calculation of the average acquisition time. Here we provide an example of calculation of mean acquisition time and detection probability. Assuming that eight cell search trials are performed on a certain SNR level, results of acquisition time of all trials are {510ms, 520ms, F, 530ms, 520ms, 530ms, 510ms, 520ms}, where "F" in the result set means that trial has failed and there was no valid acquisition time obtained from that trial. The mean acquisition time is calculated using the following equation:

(510ms+520ms+530ms+520ms+530ms+510ms+520ms)/7=520ms

The detection probability is calculated using 7/8=0.875 because there are seven successful trials out of eight. After all cell search trials, mean acquisition times and detection probabilities are calculated to build the corresponding statistical curves where the abscissas are the selected SNR levels.

In this work, cell search algorithms are grouped into four sets. Simulations and comparisons are conducted for each set. The first set includes the basic algorithm with coherent slot combining and noncoherent slot combining. The second set includes the basic, PSD and DDCC algorithms. The third set includes the basic, STS-1 and RSPT algorithms. The fourth set includes the four proposed algorithms: PSD+RSPT, PSD+STS-1, DDCC+RSPT and DDCC+STS-1. For the basic, PSD and DDCC cell

search algorithms, we set the oversampling rate to one. For STS-1 and RSPT algorithms, the oversampling rate is set to be four. For PSD+RSPT, PSD+STS-1, DDCC+RSPT and DDCC+STS-1 algorithms, the oversampling rate is also set to be four. For all algorithms, the slot combining operation in search stage 1 is performed over fifteen slots of the whole signal frame.

4.2.2 The Basic Algorithm with Coherent and Noncoherent Slot Combining

In this subsection, the basic cell search algorithm with coherent and noncoherent slot combining in searching stage 1 is tested. The performances of these two combining schemes are compared in a pure AWGN environment, and the multipath fading environment case 1, 2 and 3. There is no frequency error and clock error injected. The simulation results of the mean acquisition time are shown in Table 4.2. The graphical illustration of the results is plotted in Figure 4.2.

Table 4.2: Mean acquisition time of the basic algorithm with coherent and noncoherent slot combining, without frequency error and clock error

SNR (dB)	Basic with coherent slot combining				Basic with noncoherent slot combining			
	Mean Acquisition Time (ms)				Mean Acquisition Time (ms)			
	AWGN	Case 1	Case 2	Case 3	AWGN	Case 1	Case 2	Case 3
2	97.7	103.8	115.0	103.2	103.1	103.2	115.9	109.1
1	97.8	104.0	115.5	104.2	103.2	104.3	116.8	109.4
0	98.1	104.2	115.8	108.1	103.5	104.4	119.3	109.6
-1	98.3	106.1	125.3	113.3	103.6	104.7	119.9	109.7
-2	98.6	106.8	134.7	117.0	103.9	104.9	129.6	109.9
-3	98.7	107.9	198.0	130.1	104.3	105.1	165.3	124.2
-4	98.9	113.9	239.3	145.3	104.5	108.1	190.4	129.2
-5	99.6	144.4	333.7	221.0	114.4	117.4	270.8	188.3
-6	107.7	189.5	413.7	312.2	125.1	164.9	340.6	256.5
-7	155.9	281.5	503.9	381.7	197.1	246.1	428.2	322.1
-8	210.8	429.4	594.5	461.3	271.9	349.5	517.8	383.7
-9	279.4	518.6	662.3	560.4	352.4	438.9	610.7	491.2
-10	397.0	564.2	751.2	603.6	482.6	507.6	664.8	545.7

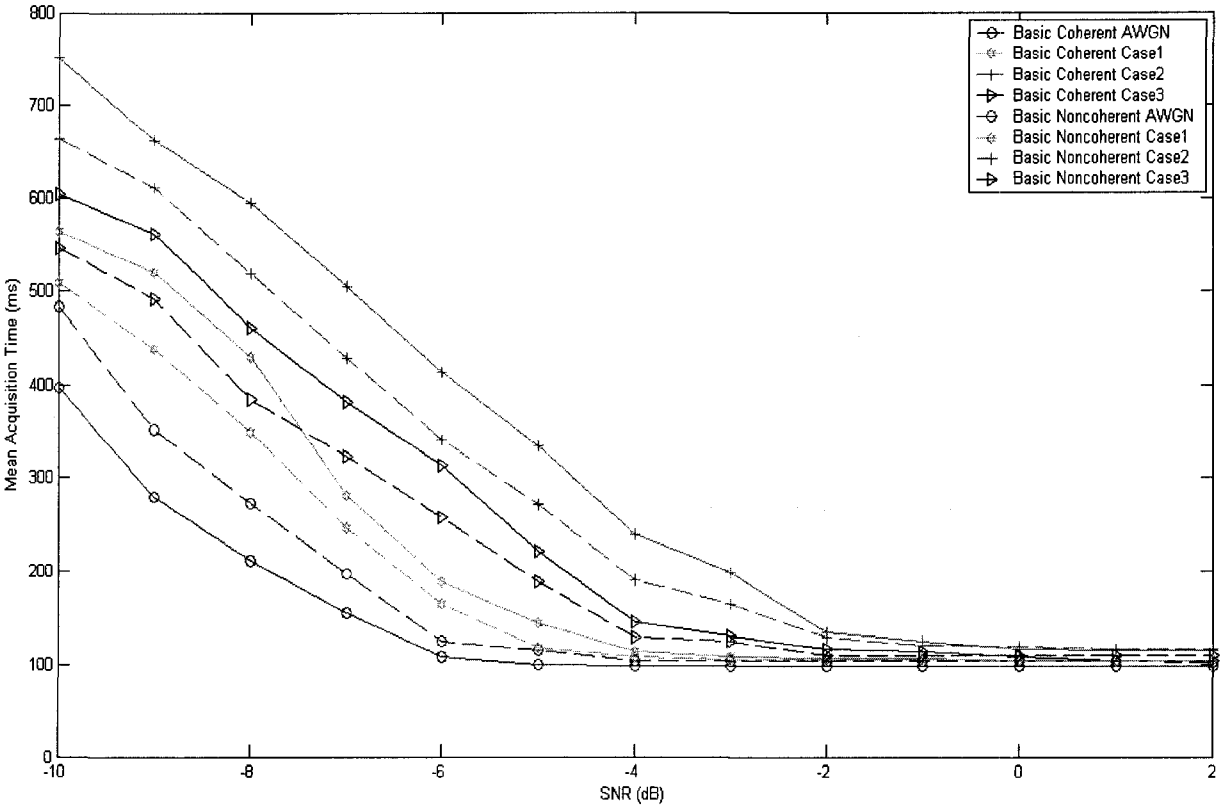


Figure 4.2: Mean acquisition time of the basic algorithm with coherent and noncoherent slot combining without frequency error and clock error

It can be observed that when SNR level increases, all curves decline down gradually. Mean acquisition times become less when the radio conditions became better. A UE has more and more chances to successfully synchronize to the correct downlink scrambling code from the first several incoming signal frames. When the SNR is above a certain level, the curves become more and more flat. For example, when the SNR is larger than -5dB, the mean acquisition time of the basic algorithm with noncoherent slot combining in AWGN environment becomes stable around 104ms. This means that the performance of the algorithm is almost saturated at or above that SNR level.

Another observation is that no matter whether coherent or noncoherent slot combining is used, a UE takes less time to acquire the downlink scrambling code in AWGN environment than that in a multipath fading environment. The trend is more obvious at low SNR values (e.g., from SNR -10dB to -3dB). This is because in AWGN environment only background noise needs to be handled and there is no phase rotation caused by multipath fading components.

It can also be found that with both coherent and noncoherent slot combining, a UE spends the most amount of acquisition time in multipath fading Case 2 environment. The acquisition time spent in Case 3 environment is more than that spent in Case 1. Since Case 2 environment contains fading components has a much longer relative delay and a larger relative power than those contained in other cases, it produces a more serious distortion to signal frames. Thus, a UE needs to spend more time on code acquisition in Case 2 environment. In contrast, Case 3 environment has the most fading components with a smaller relative delay and a lower relative power. These components cause less phase rotations on the original signal frames. Also, more resolvable multipath and higher moving speed provide Case 3 environment with a better path diversity and time diversity. Therefore, the average code acquisition time in Case 3 environment is shorter than that in Case 2 environment. Since Case 1 environment has the weakest multipath component and less phase rotation is introduced, a UE is able to acquire the downlink scrambling code faster than in other multipath environments.

Still another observation is that in AWGN environment the coherent slot combining takes less acquisition time than that in noncoherent slot combining. The reason is that with

noncoherent combining scheme, the C_{psc} correlation value of each combined slot is squared before combining. The distortion from background noise is enlarged at the same time. On the other hand, the coherent combining scheme squares the summation of C_{psc} correlation outputs from multiple slots. The impact of background noise is therefore introduced less than that introduced by noncoherent combining scheme. However, in Case 1, Case 2 and Case 3 multipath fading environments, the main interference comes from the phase distortion. This uncompensated phase distortion implies a decrease of SNR [19]. At the same time, the phase difference between outputs of multiple C_{psc} matched filters provides a diversity gain to noncoherent combining scheme. Therefore, the noncoherent combining scheme has better performance in multipath fading environments than the coherent scheme.

Table 4.3: Detection probability of basic algorithm with coherent and noncoherent slot combining without frequency error and clock error

SNR (dB)	Basic with coherent slot combining				Basic with noncoherent slot combining			
	Detection Probability				Detection Probability			
	AWGN	Case 1	Case 2	Case 3	AWGN	Case 1	Case 2	Case 3
2	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1
-1	1	1	1	1	1	1	1	1
-2	1	1	0.959	1	1	1	0.978	1
-3	1	1	0.854	0.962	1	1	0.905	0.974
-4	1	1	0.745	0.908	1	1	0.821	0.932
-5	1	0.926	0.623	0.787	1	0.983	0.704	0.856
-6	0.982	0.804	0.516	0.651	0.953	0.858	0.593	0.727
-7	0.873	0.651	0.421	0.529	0.802	0.742	0.508	0.608
-8	0.751	0.527	0.342	0.416	0.654	0.621	0.437	0.511
-9	0.574	0.405	0.257	0.335	0.475	0.503	0.352	0.429
-10	0.439	0.273	0.152	0.207	0.331	0.374	0.236	0.302

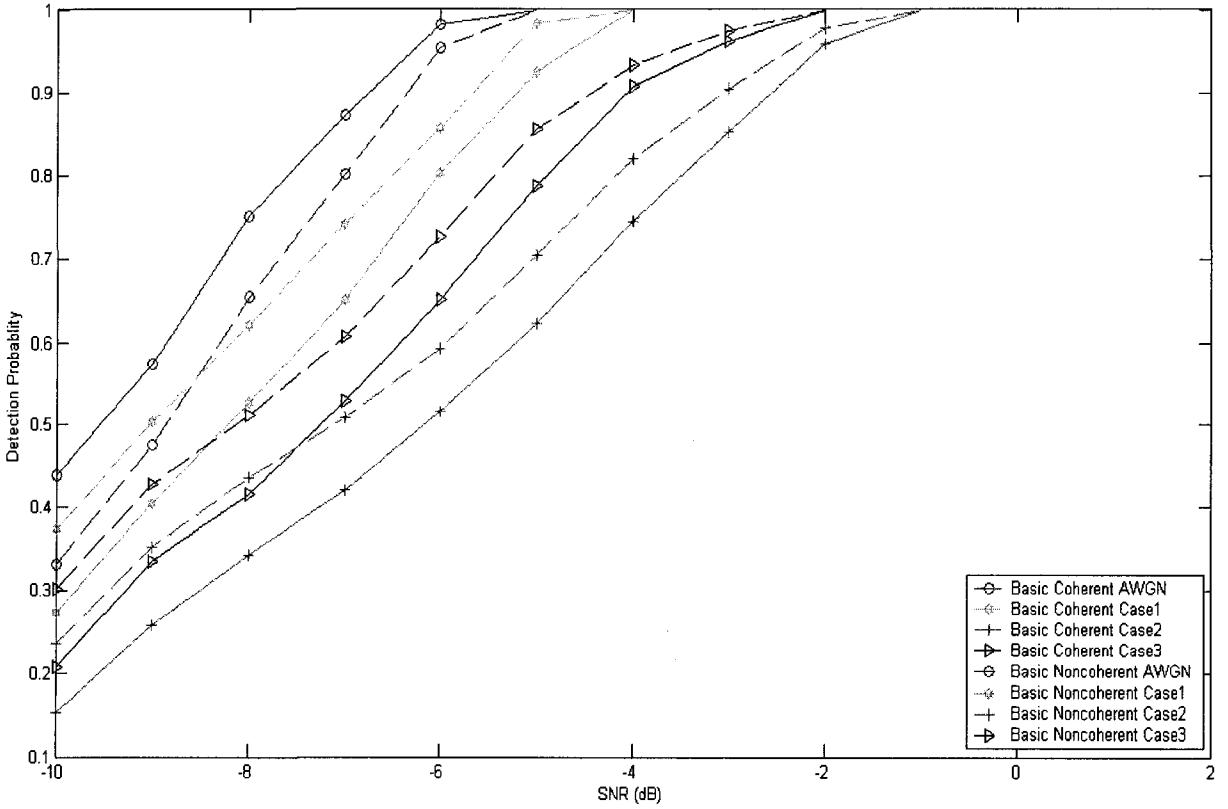


Figure 4.3: Detection probability of the basic algorithm with coherent and noncoherent slot combining without frequency error and clock error

The results of detection probability are listed in Table 4.3. They are also shown in Figure 4.3. Generally speaking, detection probability becomes higher with an increase of SNR level until it reaches full detection. Coherent slot combining scheme has a higher probability to acquire the downlink scrambling code in AWGN environment while noncoherent slot combining scheme has more opportunities to acquire in the multipath fading environments.

4.2.3 The Basic, PSD and DDCC Algorithms with Impact of Frequency Error and Clock Error

In this sub-section, performances of the basic, PSD and DDCC algorithms with the impact of frequency error are compared first. Starting with this sub-section, all simulations are undertaken in multipath fading environments. In Section 4.2.2, it has been shown that the basic algorithm with noncoherent slot combining performs better than that with coherent slot combining in multipath fading environments. Hence, from now on, simulations of the basic algorithm are only run with noncoherent slot combining scheme.

A 20 KHz frequency offset is introduced between the transmitter and the receiver in order to examine the impact of frequency error. Simulation results on the mean acquisition time are listed in Table 4.4 and depicted in Figure 4.4. The impact of frequency error can be clearly observed from the outcomes of the basic algorithm. Compared to the results in Section 4.2.2, the performance of the basic algorithm degrades largely in three multipath fading environments, especially in the case of low SNRs. For example, in the Case 1 environment without frequency error, the basic algorithm is able to acquire the downlink scrambling code within 349.5 ms at SNR=-8 dB. However, the mean acquisition time is increased to 773.5 ms at the same SNR level when a frequency error is added. The performance degradation is around 3.5 dB. This degradation can be also seen from the simulation results on detection probability listed in Table 4.5 and shown in Figure 4.5. For example, with the frequency error, the acquisition of the downlink scrambling code cannot be achieved when SNR=-7 dB in Case 2 environment. However, without frequency error, there is still a 50.8% possibility to make a successful detection.

The results show that the DDCC algorithm has the best performance out of the three candidates. The PSD algorithm outperforms the basic algorithm especially at low SNR levels. For example, in Case 3 environment, at the level of SNR=-15 dB, the mean acquisition times are 817.5 ms, 625.9 ms and 503.6 ms for the basic, PSD and DDCC algorithms, respectively. The corresponding detection probabilities are 6.1%, 24.6% and 50.5%, respectively. Apparently, the basic algorithm is much more sensitive to the phase rotation than the other two algorithms. Noncoherent combining over multiple slots is not good enough to compensate the large frequency error. By segmenting the 256-chip C_{psc} matched filter into 64-chip concatenated filters, the PSD algorithm limits the phase rotation within a smaller range. Therefore, the impact of the phase rotation does not accumulate over the whole C_{psc} matched filter. However, the partition of C_{psc} matched filter reduces the processing gain and weakens the ability to suppress background noise. The DDCC algorithm outperforms the other two algorithms since it combines the advantages of differential detection and coherent slot combining. It alleviates the impact of phase rotation by obtaining a phase reference from the output of the preceding matched filter for the current matched filter. In the mean time, a full length coherent slot combining keeps good processing gain to suppress the background noise for the C_{psc} matched filter.

Table 4.4: Mean acquisition time of the basic, PSD and DDCC algorithms with 20 KHz frequency error

SNR (dB)	Basic			PSD			DDCC		
	Mean Acquisition Time (ms)			Mean Acquisition Time (ms)			Mean Acquisition Time (ms)		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	212.6	252.5	237.8	194.7	220.3	208.5	175.2	183.3	174.1
1	213.8	256.4	239.1	195.2	221.6	210.8	175.7	184.2	174.3
0	215.6	259.1	241.3	195.7	223.1	212.1	176.1	186.9	176.6
-1	230.9	276.2	252.4	199.1	240.5	226.4	176.3	187.4	178.2
-2	269.5	354.9	314.5	214.3	294.8	252.7	177.4	193.4	180.3
-3	324.7	472.7	408.2	245.7	354.9	313.8	179.7	234.6	196.5
-4	392.9	587.2	493.7	292.2	441.3	370.5	199.6	280.3	238.3
-5	469.7	703.4	581.9	341.3	518.5	439.1	246.3	389.4	285.5
-6	544.8	843.4	695.1	434.1	626.5	531.2	321.8	491.7	397.8
-7	647.6	F	817.5	526.8	731.2	625.9	412.5	594.3	503.6
-8	773.5	F	F	635.9	834.6	740.2	508.8	708.4	598.2
-9	F	F	F	724.4	F	F	591.6	797.8	684.2
-10	F	F	F	F	F	F	685.4	F	F

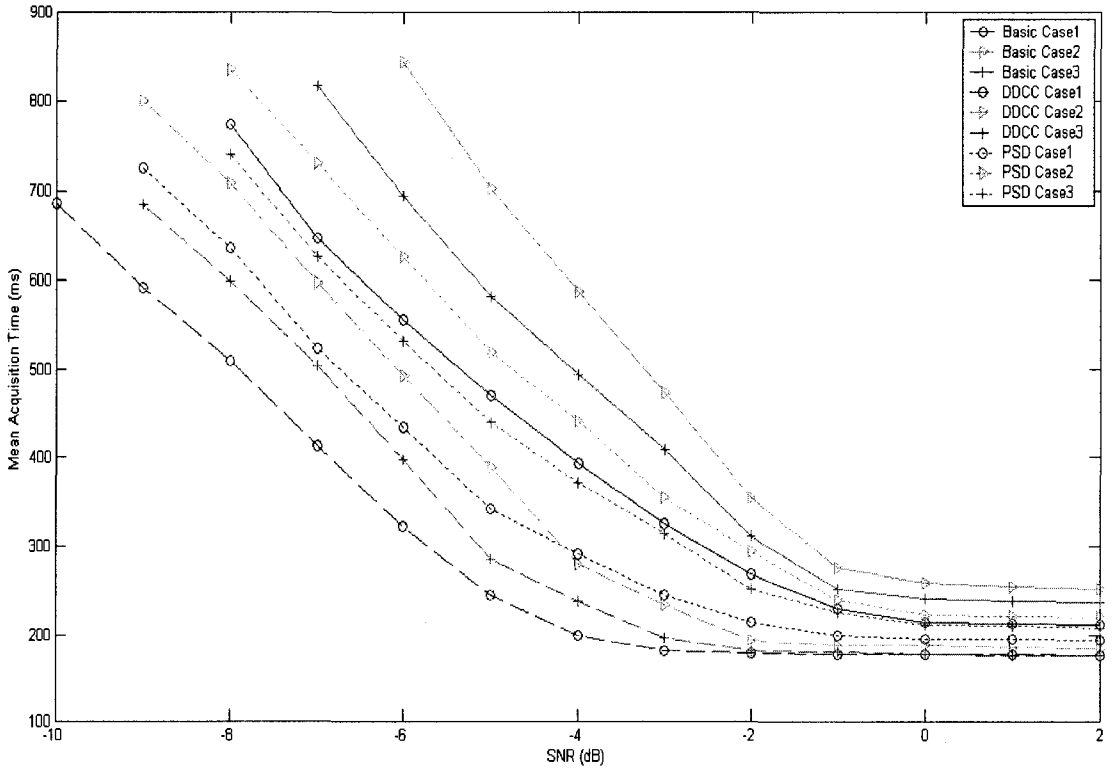


Figure 4.4: Mean acquisition time of the basic, PSD and DDCC algorithms with 20 KHz frequency error

Table 4.5: Detection probability of the basic, PSD and DDCC algorithms with 20 KHz frequency error

SNR (dB)	Basic			PSD			DDCC		
	Detection Probability			Detection Probability			Detection Probability		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
-1	0.951	0.911	0.932	1	0.947	0.962	1	1	1
-2	0.872	0.714	0.795	0.949	0.835	0.898	1	0.943	1
-3	0.749	0.516	0.613	0.887	0.701	0.804	1	0.865	0.941
-4	0.616	0.323	0.458	0.803	0.536	0.667	0.969	0.758	0.873
-5	0.477	0.178	0.294	0.684	0.413	0.525	0.894	0.615	0.772
-6	0.324	0.072	0.167	0.556	0.254	0.393	0.781	0.486	0.658
-7	0.183	0	0.061	0.411	0.128	0.246	0.646	0.327	0.505
-8	0.078	0	0	0.283	0	0.131	0.503	0.194	0.347
-9	0	0	0	0.143	0	0	0.329	0.072	0.216
-10	0	0	0	0	0	0	0.182	0	0

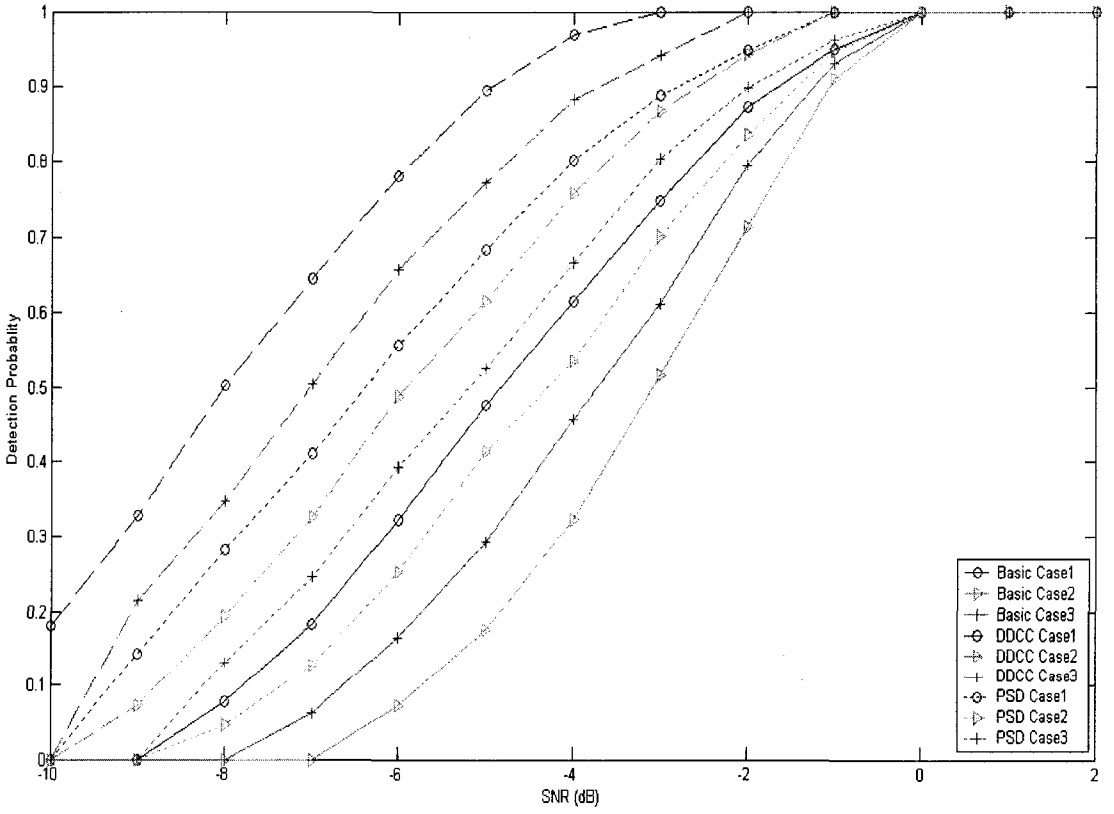


Figure 4.5: Detection probability of the basic, PSD and DDCC algorithms with 20 KHz frequency error

Having simulated the algorithms with a frequency error, we now test the DDCC and PSD algorithms with a simultaneous impact of frequency and clock errors. Besides the frequency error injected, one chip of random clock jitter is introduced in the receiver. Simulation results on the mean acquisition time and detection probability are shown in Table 4.6, Figure 4.6, Table 4.7 and Figure 4.7. It can be observed that the performance of DDCC and PSD algorithms degrades dramatically after adding the extra clock error. None of them can achieve a code acquisition if the SNR level is lower than -4 dB. Even with a relatively high SNR value, for example, in SNR level 1 dB, the acquisition times of both algorithms are still longer than 1000 ms, and the detection probability is smaller than 0.4 in Case 3 environment. This means that without a supplementary compensation for the clock error, the DDCC and PSD algorithms cannot handle the situation gracefully.

Table 4.6: Mean acquisition time of PSD and DDCC algorithms with 20 KHz frequency error and one-chip sampling drift clock error

SNR (dB)	PSD			DDCC		
	Mean Acquisition Time (ms)			Mean Acquisition Time (ms)		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	937.6	1087.7	995.5	906.6	1031.2	972.1
1	1012.5	1176.1	1085.8	984.5	1128.4	1067.8
0	1085.2	1264.1	1185.3	1051.4	1236.5	1141.1
-1	1165.6	1385.7	1264.5	1129.9	1346.8	1210.8
-2	1287.2	F	1398.6	1236.4	1425.7	1357.5
-3	F	F	F	1325.8	F	F
-4	F	F	F	F	F	F
-5	F	F	F	F	F	F
-6	F	F	F	F	F	F
-7	F	F	F	F	F	F
-8	F	F	F	F	F	F
-9	F	F	F	F	F	F
-10	F	F	F	F	F	F

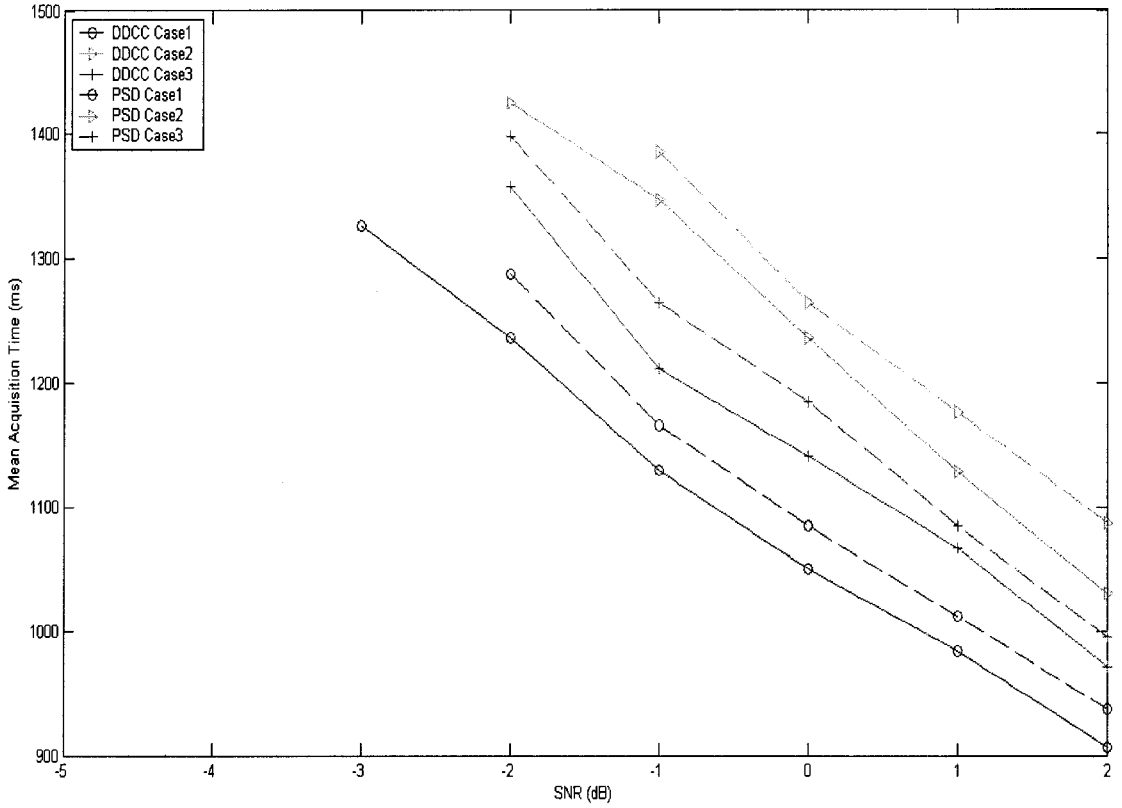


Figure 4.6: Mean acquisition time of PSD and DDCC algorithms with 20 KHz frequency error with 20 KHz frequency error and one-chip sampling drift clock error

Table 4.7: Detection probability PSD and DDCC algorithms with 20 KHz frequency error and one-chip sampling drift clock error

SNR (dB)	PSD			DDCC		
	Detection Probability			Detection Probability		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	0.422	0.341	0.408	0.469	0.395	0.456
1	0.356	0.237	0.326	0.383	0.278	0.341
0	0.265	0.126	0.213	0.287	0.169	0.253
-1	0.142	0.043	0.107	0.209	0.114	0.162
-2	0.067	0	0.032	0.115	0.047	0.078
-3	0	0	0	0.034	0	0
-4	0	0	0	0	0	0
-5	0	0	0	0	0	0
-6	0	0	0	0	0	0
-7	0	0	0	0	0	0
-8	0	0	0	0	0	0
-9	0	0	0	0	0	0
-10	0	0	0	0	0	0

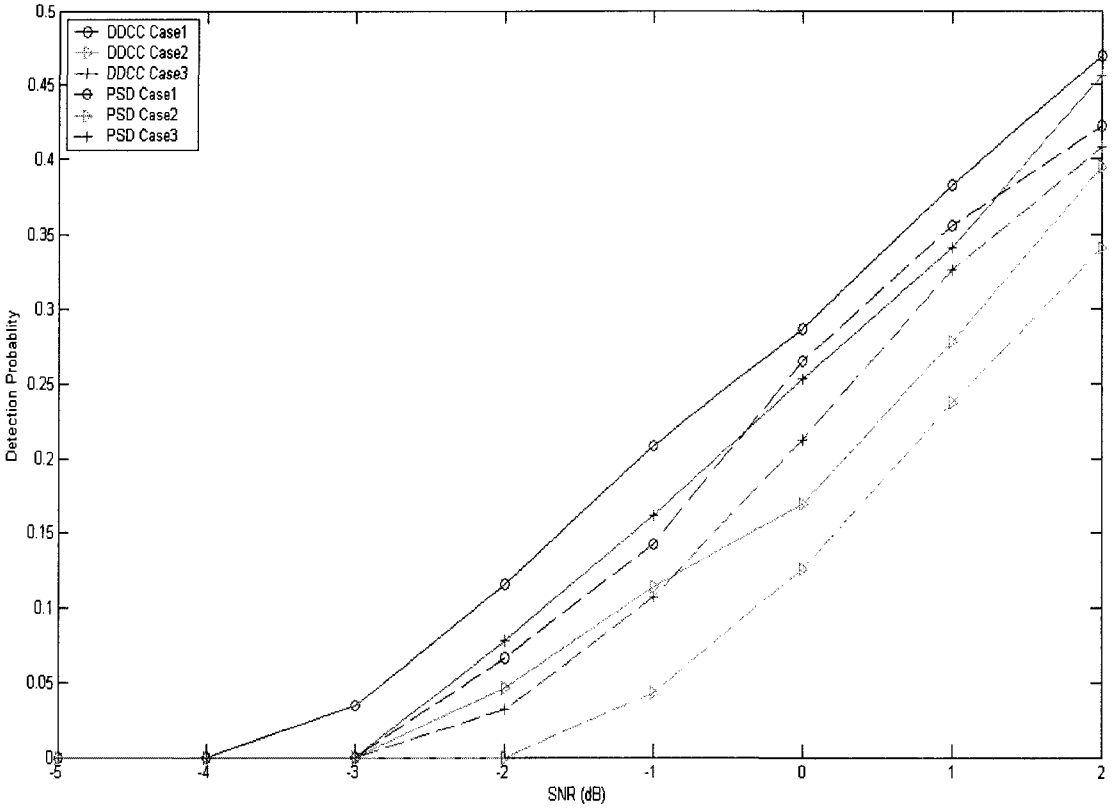


Figure 4.7: Detection probability of PSD and DDCC algorithms with 20 KHz frequency error and one-chip sampling drift clock error

4.2.4 The Basic, STS-1 and RSPT Algorithms with Impact of Frequency Error and Clock Error

In this sub-section, the impact of clock error is investigated. The performances of the basic, STS-1 and RSPT algorithms are compared in multipath fading Case 1, 2 and 3 environments. Instead of using chip rate sampling, the STS-1 and RSPT algorithms oversample the incoming signal frames by a factor of 4 before entering cell search stage 1. It can be estimated that the timing resolution of the received signal is increased by 4

times with the oversampling operation. The mean acquisition time result is listed in Table 4.8 and depicted in Figure 4.8.

The impact of clock error on the basic algorithm can be clearly observed. For example, in the Case 2 environment, with one-chip clock error, the mean acquisition time is 921.8 ms at SNR=-6 dB. Comparing to the results shown in Table 4.2, on the same SNR level without the clock error, the mean acquisition time is 340.6 ms in Case 2 environment. We can see that the performance degradation is about 4.3 dB. The basic algorithm cannot acquire the downlink scrambling code if the clock error is added at a lower SNR level such as -7 dB.

Table 4.8: Mean acquisition time of the basic, STS-1 and RSPT algorithms with one-chip sampling drift clock error

SNR (dB)	Basic			STS-1			RSPT		
	Mean Acquisition Time (ms)			Mean Acquisition Time (ms)			Mean Acquisition Time (ms)		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	248.9	293.6	272.1	335.3	394.3	362.4	146.2	193.8	173.8
1	249.5	294.5	275.9	338.2	398.2	367.3	146.8	195.4	175.2
0	251.4	297.7	278.5	341.6	402.6	370.1	147.9	198.1	176.7
-1	257.8	316.5	301.7	349.1	435.7	392.6	148.4	206.7	179.4
-2	284.7	429.4	369.2	418.6	567.3	485.1	151.6	231.2	183.9
-3	386.2	575.8	486.8	511.2	693.4	608.3	187.1	313.9	218.6
-4	463.8	687.3	593.5	602.8	828.6	714.2	234.5	417.5	304.1
-5	575.3	807.5	702.2	684.1	936.1	825.8	320.3	527.3	408.1
-6	653.6	921.8	812.3	790.3	1023.9	912.5	396.7	619.1	496.3
-7	776.7	F	896.4	876.9	1104.5	1002.8	462.9	708.3	598.6
-8	879.5	F	F	962.5	F	1073.2	570.9	816.6	709.5
-9	F	F	F	1036.7	F	F	685.6	939.9	824.3
-10	F	F	F	F	F	F	791.4	F	F

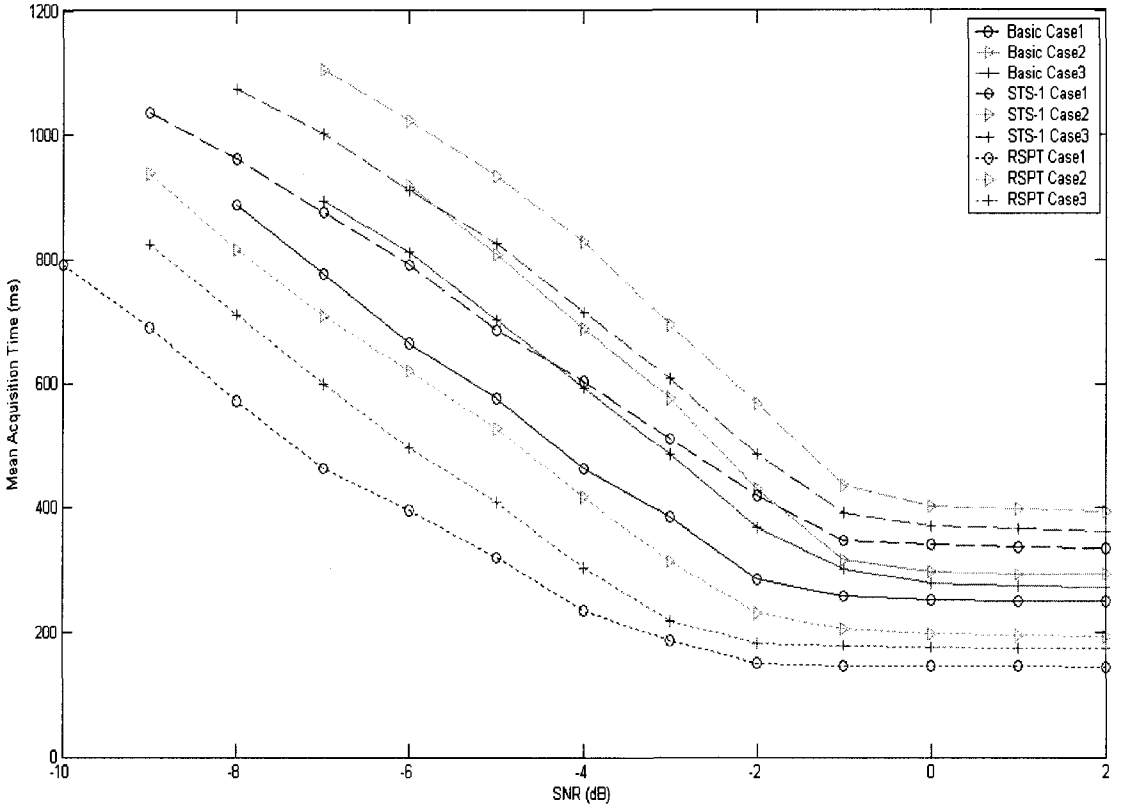


Figure 4.8: Mean acquisition time of the basic, STS-1 and RSPT algorithms with one-chip sampling drift clock error

The detection probability is listed in Table 4.9 and shown in Figure 4.9. Comparing to the mean acquisition time, it can be observed that the RSPT outperforms significantly the basic algorithm, especially on the low SNR level. For example, in Case 1 environment, when SNR=-6 dB, the mean acquisition times are 396.7 ms and 653.6 ms for RSPT and the basic algorithm, respectively. The corresponding detection probabilities of these two algorithms on the same SNR level are 62.5% and 18.3%.

Similarly, computer simulations show that the STS-1 algorithm surpasses the basic algorithm with respect to the detection probability. However, the STS-1 algorithm spends

more acquisition time to maintain a higher detection probability. For example, at SNR=-6 dB in Case 1 environment, STS-1's detection probability and mean acquisition time are 27.8% and 790.3 ms. The reason can be explained as follows. Generally, STS-1 is more robust than the basic algorithm because of the oversampling operation. A Selection of the best candidate from the outputs of four serial tests allows STS-1 to obtain more chance than the basic algorithm to acquire the correct slot boundary in search stage 1. However, serial tests on oversampled signal frames extend the time spent in search stage 1 largely.

Compared to the STS-1, the RSPT benefits from the timing resolution of the oversampling operation. It randomly selects one of four candidates from the oversampled signal frames for each cell search trial. Hence, it has more chances to avoid picking up the signal frame candidate with incorrect slot boundary information on the average. The STS-1 however selects the maximum outcome from four serial matched filtering tests as the reference of slot boundary. This maximum may not be the outcome corresponding to the real slot boundary. The probability of wrong selection increases especially at a low level of SNR.

It can be observed that in all three radio environments the RSPT algorithm performs better than the basic and STS-1 algorithms. The STS-1 algorithm has a longer mean acquisition time than that of the basic algorithm but with a higher detection probability. According to Table 3.2, except for the oversampling operation, the RSPT algorithm does not introduce extra computational complexity. On the other hand, the STS-1 algorithm adds a much more implementation complexity due to the serial tests.

Table 4.9: Detection probability of the basic, STS-1 and RSPT algorithms with one-chip sampling drift clock error

SNR (dB)	Basic			STS-1			RSPT		
	Detection Probability			Detection Probability			Detection Probability		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
-1	1	0.902	0.934	1	0.914	0.951	1	1	1
-2	0.921	0.679	0.808	0.932	0.726	0.847	1	0.959	1
-3	0.754	0.423	0.605	0.816	0.523	0.658	0.972	0.875	0.952
-4	0.516	0.241	0.387	0.601	0.338	0.471	0.879	0.753	0.835
-5	0.311	0.124	0.236	0.415	0.205	0.315	0.756	0.568	0.653
-6	0.183	0.056	0.129	0.278	0.112	0.192	0.625	0.386	0.507
-7	0.102	0	0.049	0.169	0.041	0.113	0.493	0.263	0.364
-8	0.038	0	0	0.094	0	0.046	0.347	0.141	0.223
-9	0	0	0	0.037	0	0	0.217	0.052	0.096
-10	0	0	0	0	0	0	0.108	0	0

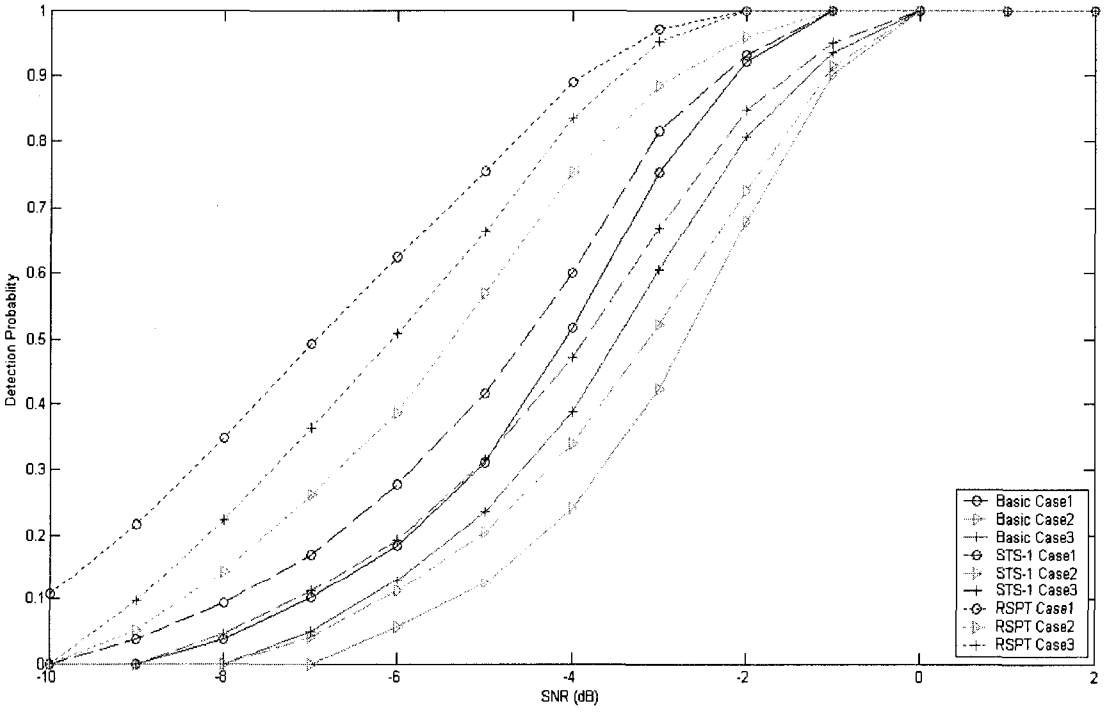


Figure 4.9: Detection probability of the basic, STS-1 and RSPT algorithms with one-chip sampling drift clock error

Like what has been done in Section 4.2.3, the STS-1 and RSPT algorithms are also tested with a simultaneous impact of frequency error and clock error. A frequency offset of 20 KHz is introduced between the base station and the UE. The Simulation results are shown in Table 4.10, Figure 4.10, Table 4.11 and Figure 4.11. It is observed that the performance of STS-1 and RSPT degrades significantly when a frequency error is added. The downlink scrambling code can be acquired with a long acquisition time and a low detection probability only, when SNR level is higher than -3 dB. For example, when SNR is -2 dB, the acquisition time of both algorithms is around 1500 ms, and the detection probability is smaller than 0.06 in the Case 1 environment, which is not acceptable. Thus, an extra compensation is needed for both algorithms to counteract the frequency error.

Table 4.10: Mean acquisition time of STS-1 and RSPT algorithms with 20 KHz frequency error and one-chip sampling drift clock error

SNR (dB)	STS-1			RSPT		
	Mean Acquisition Time (ms)			Mean Acquisition Time (ms)		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	1136.1	1225.8	1175.2	1063.3	1151.4	1093.7
1	1208.7	1345.1	1232.8	1158.2	1279.1	1181.6
0	1327.8	1432.6	1346.7	1221.6	1367.2	1269.9
-1	1435.2	1547.2	1471.5	1347.8	1446.7	1375.8
-2	1556.7	F	F	1460.5	F	1481.3
-3	F	F	F	F	F	F
-4	F	F	F	F	F	F
-5	F	F	F	F	F	F
-6	F	F	F	F	F	F
-7	F	F	F	F	F	F
-8	F	F	F	F	F	F
-9	F	F	F	F	F	F
-10	F	F	F	F	F	F

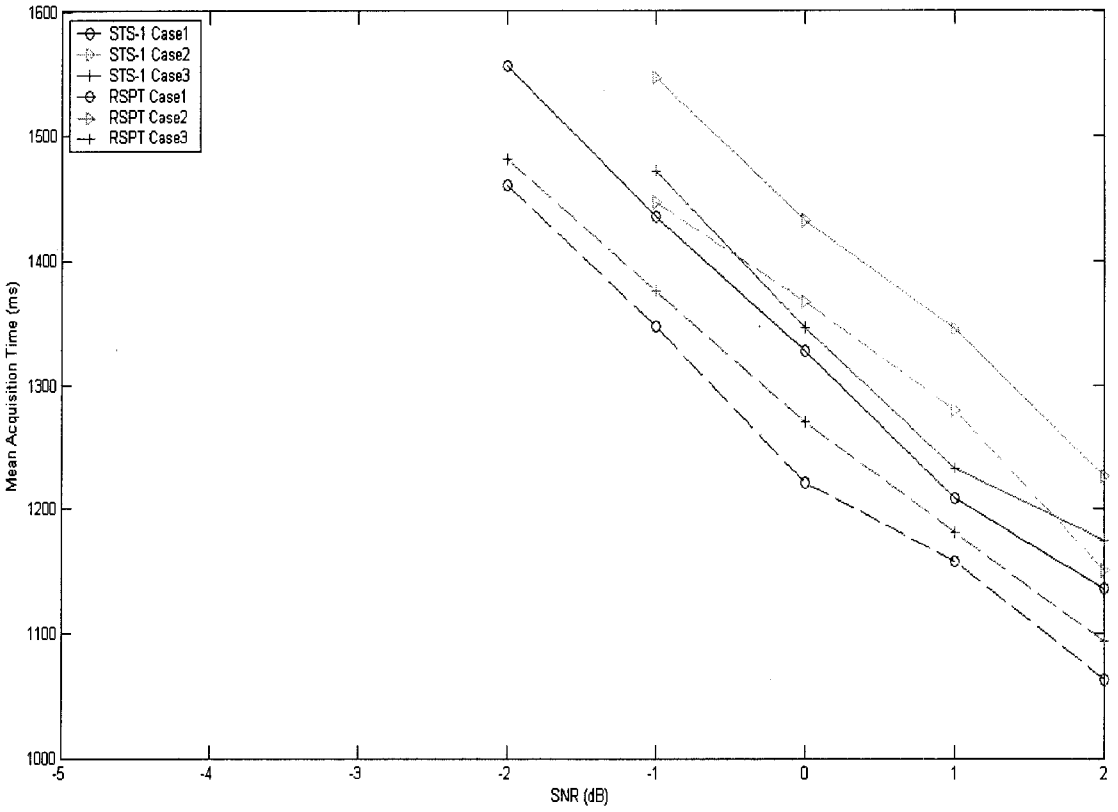


Figure 4.10: Mean acquisition time of STS-1 and RSPT algorithms with 20 KHz frequency error and one-chip sampling drift clock error

Table 4.11: Detection probability STS-1 and RSPT algorithms with 20 KHz frequency error and one-chip sampling drift clock error

SNR (dB)	STS-1			RSPT		
	Detection Probability			Detection Probability		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	0.389	0.306	0.347	0.463	0.371	0.427
1	0.294	0.215	0.252	0.346	0.268	0.314
0	0.186	0.124	0.163	0.252	0.154	0.228
-1	0.093	0.039	0.051	0.127	0.062	0.102
-2	0.027	0	0	0.053	0	0.036
-3	0	0	0	0	0	0
-4	0	0	0	0	0	0
-5	0	0	0	0	0	0
-6	0	0	0	0	0	0
-7	0	0	0	0	0	0
-8	0	0	0	0	0	0
-9	0	0	0	0	0	0
-10	0	0	0	0	0	0

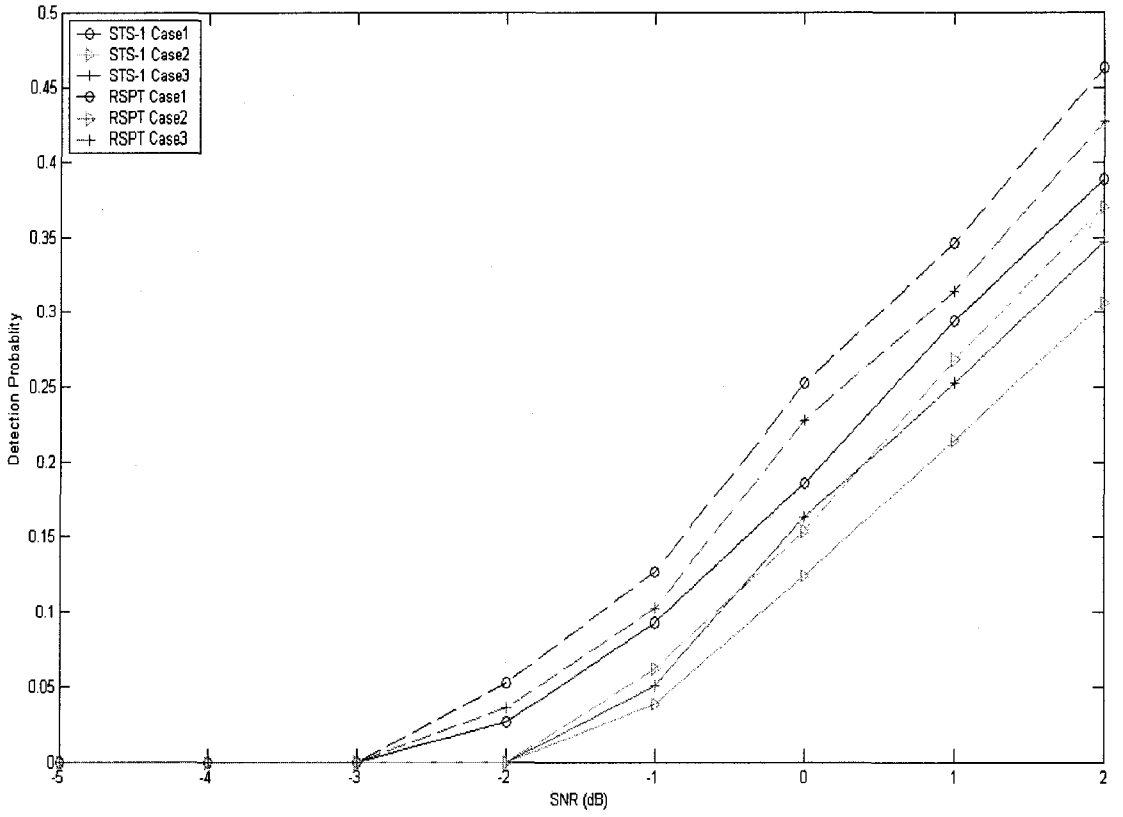


Figure 4.11: Detection probability of STS-1 and RSPT algorithms with 20 KHz frequency error and one-chip sampling drift clock error

4.2.5 Combined Algorithms DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 with Impact of Frequency Error and Clock Error

In the previous sub-sections, the performance of the basic, PSD, DDCC, STS-1 and RSPT algorithms was studied. It was shown that the frequency and clock errors significantly degrade the performance of the basic algorithm. It was also shown that the DDCC and PSD, RSPT and STS-1 are efficient in resisting the effect of either frequency or clock error. In practice, however, the frequency and clock errors often occur

simultaneously. Simulation results showed that these four enhanced algorithms lack of the ability to resist both negative effects at the same time. In this section, we simulate the proposed four algorithms: DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1. Our purpose is to find out the algorithms that can counteract the frequency error and clock error at the same time, and has the best performance for practical applications. Still, the performance of the new combined algorithms is examined in multipath fading environments Case 1, 2 and 3. The simulation results on the mean acquisition time are provided in Table 4.12 and depicted in Figure 4.12, Figure 4.13 and Figure 4.14 respectively.

As expected, the downlink scrambling code acquisition is with more difficulty in the environment of simultaneous frequency and clock errors. The mean acquisition times of some combined algorithms, such as PSD+STS-1 and DDCC+STS-1 algorithms, are even close to 1200 ms at a relatively low SNR level. It can be found that the performance of DDCC+RSPT and PSD+RSPT is superior to that of DDCC+STS-1 and PSD+STS-1. For example, at SNR=-6 dB, in Case 1 environment, the mean acquisition times of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms are 476.5 ms, 631.8 ms, 886.1 ms and 1109.3 ms, respectively. At the level of SNR=-9 dB, the DDCC+RSPT and PSD+RSPT algorithms are still able to acquire the downlink scrambling code within 723.6 ms and 928.1 ms, respectively. However, the DDCC+STS-1 and PSD+STS-1 algorithms do not work anymore.

Table 4.12: Mean acquisition time of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms with 20 KHz frequency error and one-chip sampling drift clock error

SNR (dB)	DDCC+RSPT Mean Acquisition Time (ms)			PSD+RSPT Mean Acquisition Time (ms)		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	232.1	281.2	265.5	306.4	347.4	329.9
1	238.4	285.3	267.9	308.3	348.1	332.8
0	242.9	286.2	269.1	312.5	373.5	335.4
-1	269.4	314.3	292.5	343.6	406.9	356.1
-2	285.4	351.6	316.1	362.5	456.7	385.2
-3	318.9	397.8	357.9	401.4	533.9	453.6
-4	367.4	462.9	413.9	462.3	626.5	534.7
-5	418.5	543.4	476.8	536.7	746.5	642.3
-6	476.5	675.1	564.3	631.8	873.8	753.5
-7	541.3	769.8	649.2	715.8	992.2	857.9
-8	625.4	867.5	751.7	809.2	F	971.2
-9	723.6	982.9	840.5	928.1	F	F
-10	817.8	F	938.3	F	F	F
SNR (dB)	DDCC+STS-1 Mean Acquisition Time (ms)			PSD+STS-1 Mean Acquisition Time (ms)		
	Case 1	Case 2	Case 1	Case 2	Case 1	Case 2
2	389.2	439.7	389.2	439.7	389.2	439.7
1	392.7	461.3	392.7	461.3	392.7	461.3
0	405.1	495.3	405.1	495.3	405.1	495.3
-1	428.2	538.1	428.2	538.1	428.2	538.1
-2	472.7	607.5	472.7	607.5	472.7	607.5
-3	545.6	712.2	545.6	712.2	545.6	712.2
-4	632.3	865.6	632.3	865.6	632.3	865.6
-5	743.8	1019.4	743.8	1019.4	743.8	1019.4
-6	886.1	1163.1	886.1	1163.1	886.1	1163.1
-7	1012.4	F	1012.4	F	1012.4	F
-8	1138.3	F	1138.3	F	1138.3	F
-9	F	F	F	F	F	F
-10	F	F	F	F	F	F

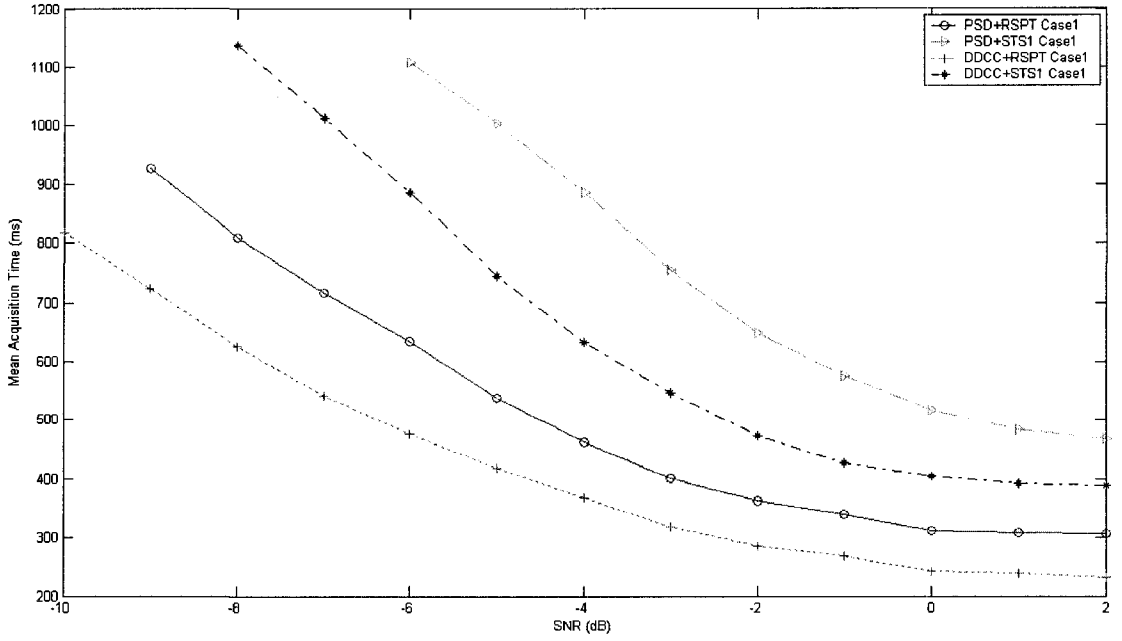


Figure 4.12: Mean acquisition time of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms in multipath fading environment Case 1 with 20 KHz frequency error and one-chip sampling drift clock error

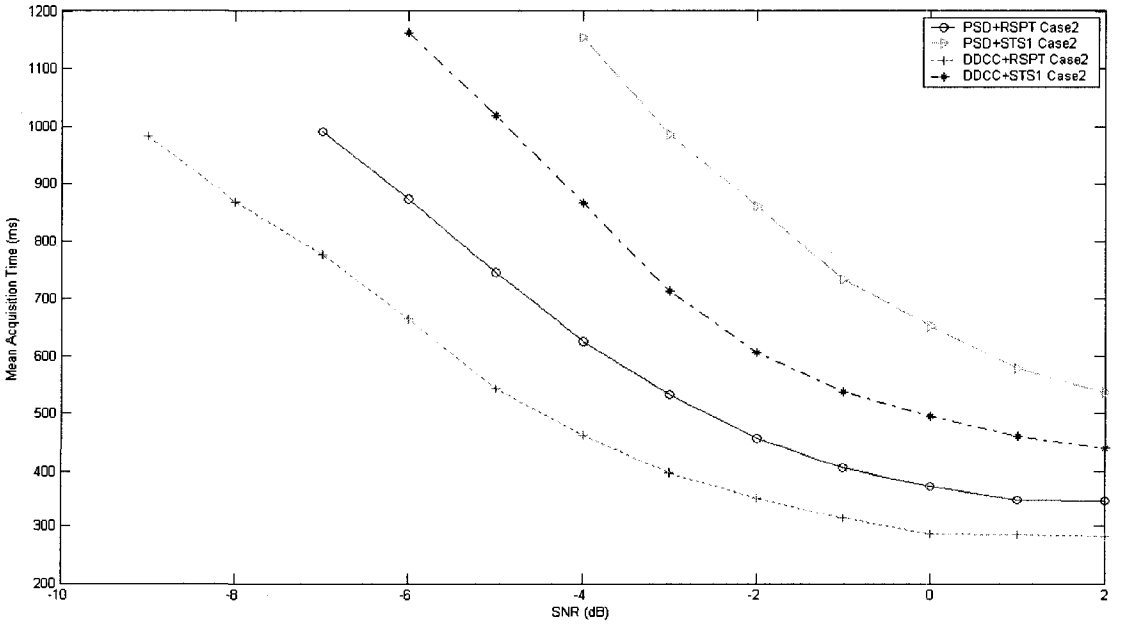


Figure 4.13: Mean acquisition time of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms in multipath fading environment Case 2 with 20 KHz frequency error and one-chip sampling drift clock error

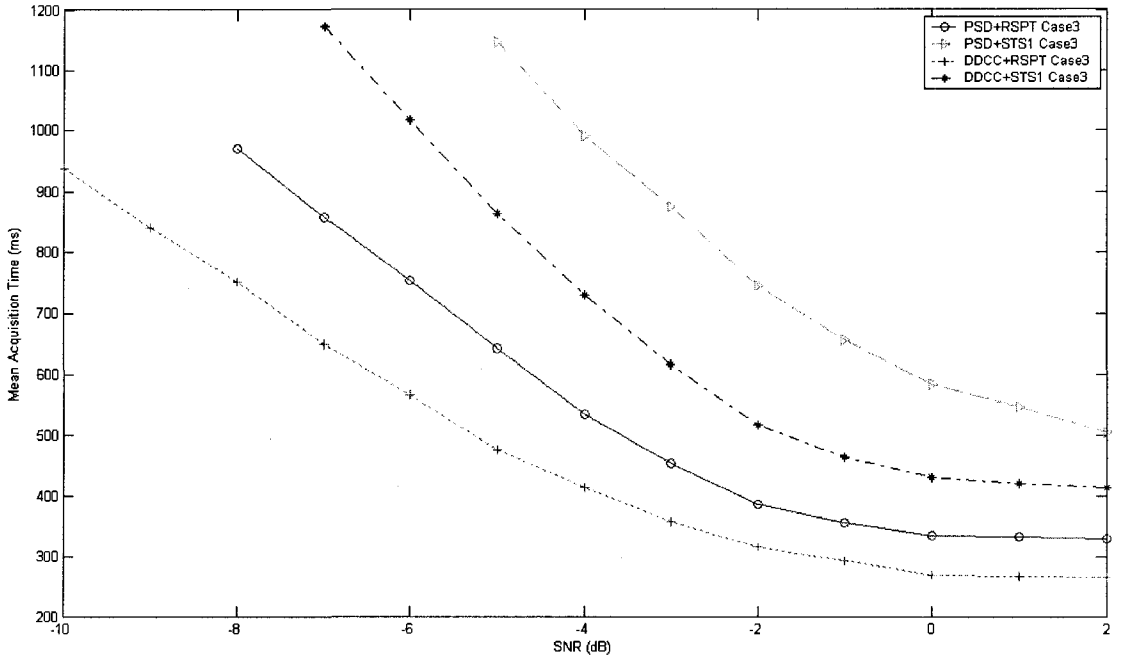


Figure 4.14: Mean acquisition time of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms in multipath fading environment Case 3 with 20 KHz frequency error and one-chip sampling drift clock error

The detection probability is listed in Table 4.13 and shown in Figure 4.15, Figure 4.16 and Figure 4.17. It is found from that the PSD+STS-1 algorithm is ranked to the bottom. On the top end, the DDCC+RSPT algorithm performs best in any multipath fading environment. The PSD+RSPT and DDCC+STS-1 algorithms are in the middle. Compared to the other three algorithms, the PSD+STS-1 algorithm takes the most acquisition time but shows the lowest detection probability. For example, when SNR is 2 dB, the PSD+STS-1 algorithm still has 0.057% failure rate in the Case 3 environment while the other algorithms achieve full detection. The DDCC+RSPT algorithm, on the other hand, is the best choice in terms of the cell search performance. This is because the DDCC algorithm outperforms the PSD algorithm in resisting the frequency error, the RSPT outperforms the STS-1 for counteracting the clock error, and thus their

combination yields the best opportunity to improve the cell search performance. In addition, recalling the discussion on the computational complexity in Chapter 3 (see Table 3.2), the complexities of the DDCC+RSPT and PSD+RSPT algorithms are less than that of the DDCC+STS-1 and PSD+STS-1 algorithms. Thus, we can conclude that the DDCC+RSPT algorithm is optimal among the four proposed combinations.

Table 4.13: Detection probability of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms with 20 KHz frequency error and one-chip sampling drift clock error

SNR (dB)	DDCC+RSPT			PSD+RSPT		
	Detection Probability			Detection Probability		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
2	1	1	1	1	1	1
1	1	1	1	1	1	1
0	1	1	1	1	0.954	1
-1	0.974	0.921	0.945	0.927	0.863	0.914
-2	0.929	0.835	0.873	0.805	0.716	0.774
-3	0.841	0.714	0.769	0.676	0.541	0.613
-4	0.752	0.593	0.672	0.551	0.402	0.475
-5	0.658	0.449	0.548	0.414	0.238	0.322
-6	0.526	0.318	0.413	0.292	0.127	0.217
-7	0.396	0.216	0.297	0.192	0.056	0.136
-8	0.281	0.122	0.196	0.133	0	0.064
-9	0.182	0.047	0.103	0.067	0	0
-10	0.083	0	0.046	0	0	0
SNR (dB)	DDCC+STS-1			PSD+STS-1		
	Detection Probability			Detection Probability		
	Case 1	Case 2	Case 1	Case 2	Case 1	Case 2
2	1	1	1	1	1	1
1	1	0.973	1	0.973	1	0.973
0	0.957	0.894	0.957	0.894	0.957	0.894
-1	0.874	0.761	0.874	0.761	0.874	0.761
-2	0.745	0.612	0.745	0.612	0.745	0.612
-3	0.623	0.457	0.623	0.457	0.623	0.457
-4	0.469	0.303	0.469	0.303	0.469	0.303
-5	0.341	0.145	0.341	0.145	0.341	0.145
-6	0.207	0.052	0.207	0.052	0.207	0.052
-7	0.112	0	0.112	0	0.112	0
-8	0.046	0	0.046	0	0.046	0
-9	0	0	0	0	0	0
-10	0	0	0	0	0	0

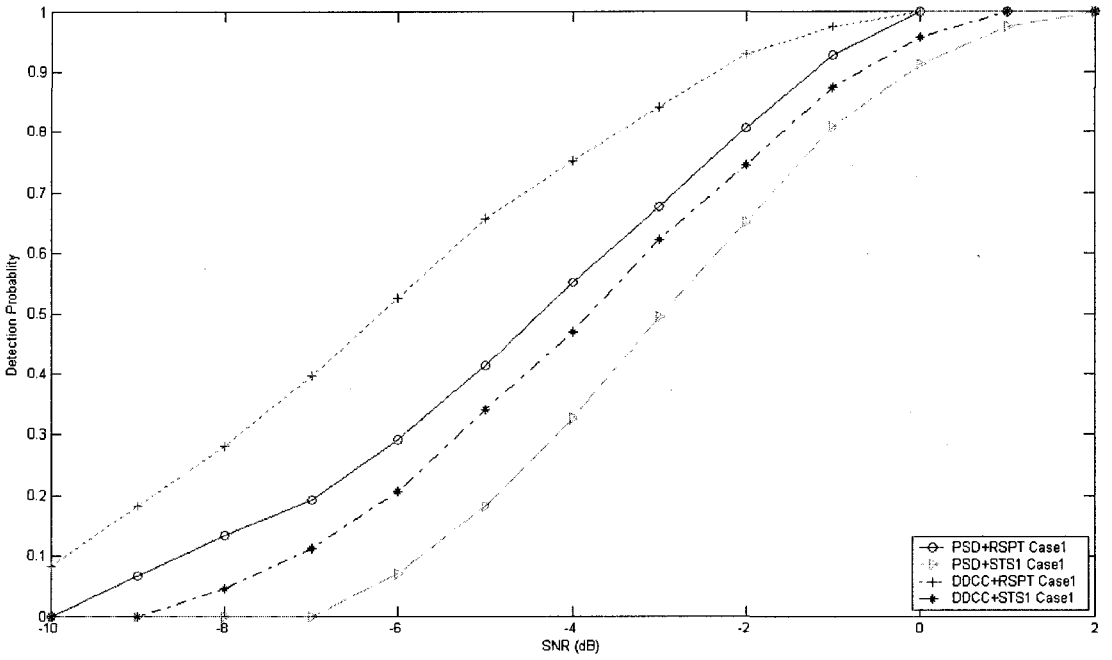


Figure 4.15: Detection probability of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms in multipath fading environment Case 1 with 20 KHz frequency error and one-chip sampling drift clock error

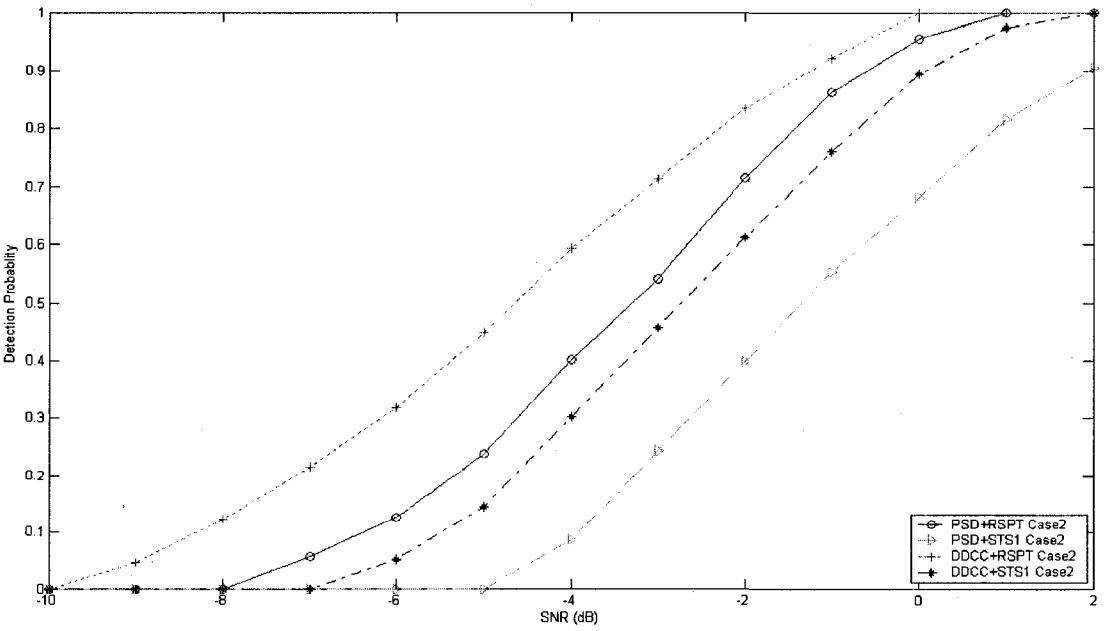


Figure 4.16: Detection probability of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms in multipath fading environment Case 2 with 20 KHz frequency error and one-chip sampling drift clock error

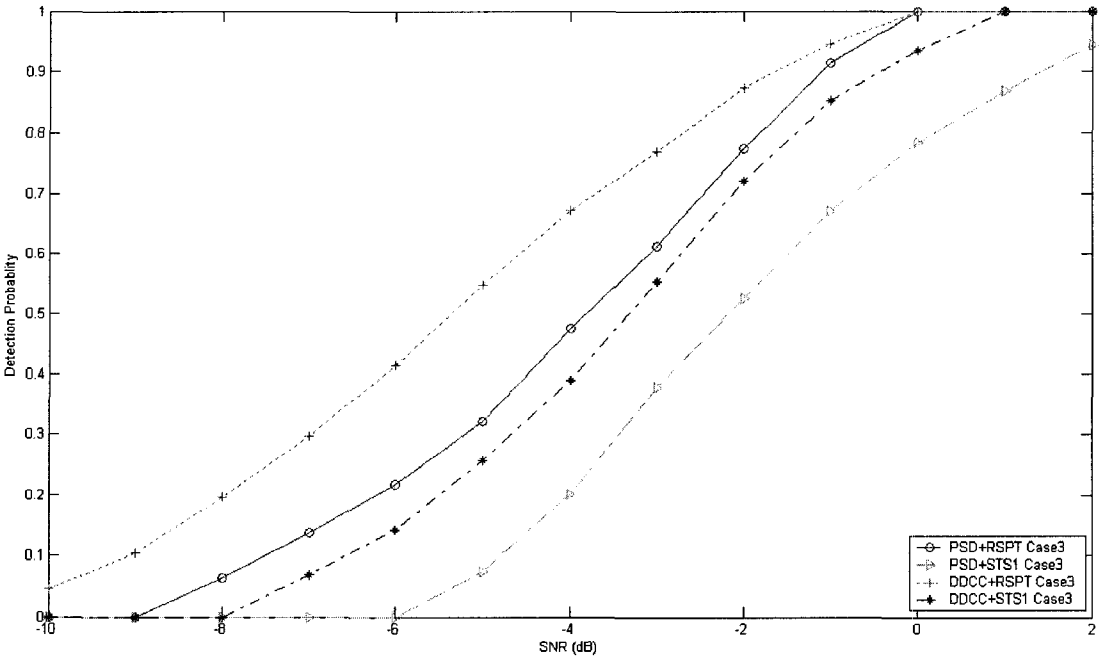


Figure 4.17: Detection probability of DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 algorithms in multipath fading environment Case 3 with 20 KHz frequency error and one-chip sampling drift clock error

4.3 Summary

In this chapter, we have carried out a simulation study on all the introduced cell search algorithms. We have evaluated their performances in terms of the mean acquisition time and detection probability. Firstly, the basic algorithm was simulated with coherent and noncoherent slot combining schemes in cell search stage 1. It has been shown that the coherent slot combining scheme performs well in the pure AWGN environment whereas the noncoherent slot combining scheme has a better performance in multipath fading environments. Then, the basic algorithm was compared with the PSD and DDCC algorithms under the impact of frequency error, and with RSPT and STS-1 algorithms with the effect of clock error. It has been found that the DDCC and RSPT algorithms

perform better than the PSD and STS-1 algorithms. We have also found that none of the existing algorithms can handle at the same time both the frequency and clock errors gracefully.

In the last set of experiments, we have tested the proposed four combined algorithms, DDCC+RSPT, PSD+RSPT, DDCC+STS-1 and PSD+STS-1 under the impact of both frequency error and clock error. It has been shown that the DDCC+RSPT algorithm gives the best result compared to the other combined algorithms. It can not only handle both errors simultaneously, but also can perform a relatively fast and accurate cell search. By also taking into account the computational complexity discussed in Chapter 3, we can conclude that the DDCC+RSPT algorithm is the best one among the four.

Chapter 5: Conclusions and Future Work

5.1 Conclusions

A major purpose of cell search process in WCDMA systems is to achieve the downlink scrambling code synchronization. The frequency and clock errors are two main reasons of performance degradations of cell search. In practice, these two effects usually occur at the same time and they are caused by the inaccuracy of crystal oscillators. The major weakness of the most existing algorithms is that they are designed only for handling frequency error or clock error, but not dealing with both errors at the same time. In this thesis, we have proposed some improved search algorithms to tackle the issue.

We have first presented several existing cell search algorithms, namely, the basic 3GPP algorithm and its enhanced versions such as DDCC, PSD, RSPT and STS-1. We have then analyzed the drawbacks of these algorithms. Based on the enhanced algorithms, we have proposed four combinations of the existing search algorithms as improved techniques. The proposed solutions target to meet the requirement of handling both errors and perform a fast and accurate cell search with a relatively low level of implementation complexity. We have also compared our methods with the existing solutions through simulation studies.

The simulation has been executed in different radio environments, i.e. the AWGN environment, the 3GPP multipath fading environments Case 1, Case 2 and Case 3. The performance was evaluated based on the mean acquisition time and the detection probability. It has been demonstrated through simulation results that the performance of the basic algorithm was significantly degraded in the presence of both frequency and clock errors. The DDCC and PSD algorithms were more effective for resisting frequency error than the basic algorithm because of their enhanced ability to restrain phase rotation, but its performance degrades when two errors appear together. It has also been shown that the RSPT and STS-1 algorithms bring more robustness for counteracting the clock error due to the profit of oversampling operation, but the two algorithms cannot handle the other error properly. We have simulated the proposed four algorithms and found out that the combined DDCC+RSPT algorithm has shown a better performance than other combined schemes in all multipath radio environments in terms of the acquisition time and detection probability. In addition, this combination has a less computational complexity compared to the other algorithms. Therefore, the combination of DDCC and RSPT algorithms is considered very appealing for industrial applications.

The contributions of this thesis can be summarized as follows:

- Analyzed the drawback of existing cell search algorithms.
- Proposed different combinations of the existing cell search algorithms to overcome their shortcomings in coping with frequency as we as clock errors.
- Performed an intensive simulation study of the existing and proposed solutions and compared their performances.

- Achieved the best combined solution among the proposed cell search algorithms for practical applications.

5.2 Future Work

There are other cell search algorithms such as Frequency Offset Compensation (FOC) and Sample Point Reordering (SPR) [26] emerging recently. FOC is designed to oppose frequency error and it divides frequency offset into small bins. Compensations of frequency error take place in each bin. SPR is used to reduce clock error. Using a similar idea, it splits the clock drift into small bins and compensates clock error in each bin. More bins offer more compensations but the complexity is also increased. It would be interesting to investigate the combinations of these two algorithms with the algorithms discussed in this thesis in the future work. Also, in this study, all the algorithms are simulated in the environment with single user and single base station. It would be interesting to compare performance of the algorithms within environment of multiple users and multiple base stations.

Cell search is not only important for 3G systems but also interested in the next generation wireless mobile communication systems (4G systems). Compared with 3G systems, although the 4G systems will have a much different air interface, modulation schemes and multiple access schemes [42], it would be interesting to make an attempt to apply the cell search concepts discussed in this thesis to 4G systems.

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Appendix A

Table A.1: Allocation of C_{ssc} for S-SCH

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 0	1	1	2	8	9	10	15	8	10	16	2	7	15	7	16
Group 1	1	1	5	16	7	3	14	16	3	10	5	12	14	12	10
Group 2	1	2	1	15	5	5	12	16	6	11	2	16	11	15	12
Group 3	1	2	3	1	8	6	5	2	5	8	4	4	6	3	7
Group 4	1	2	16	6	6	11	15	5	12	1	15	12	16	11	2
Group 5	1	3	4	7	4	1	5	5	3	6	2	8	7	6	8
Group 6	1	4	11	3	4	10	9	2	11	2	10	12	12	9	3
Group 7	1	5	6	6	14	9	10	2	13	9	2	5	14	1	13
Group 8	1	6	10	10	4	11	7	13	16	11	13	6	4	1	16
Group 9	1	6	13	2	14	2	6	5	5	13	10	9	1	14	10
Group 10	1	7	8	5	7	2	4	3	8	3	2	6	6	4	5
Group 11	1	7	10	9	16	7	9	15	1	8	16	8	15	2	2
Group 12	1	8	12	9	9	4	13	16	5	1	13	5	12	4	8
Group 13	1	8	14	10	14	1	15	15	8	5	11	4	10	5	4
Group 14	1	9	2	15	15	16	10	7	8	1	10	8	2	16	9
Group 15	1	9	15	6	16	2	13	14	10	11	7	4	5	12	3
Group 16	1	10	9	11	15	7	6	4	16	5	2	12	13	3	14
Group 17	1	11	14	4	13	2	9	10	12	16	8	5	3	15	6
Group 18	1	12	12	13	14	7	2	8	14	2	1	13	11	8	11
Group 19	1	12	15	5	4	14	3	16	7	8	6	2	10	11	13
Group 20	1	15	4	3	7	6	10	13	12	5	14	16	8	2	11
Group 21	1	16	3	12	11	9	13	5	8	2	14	7	4	10	15
Group 22	2	2	5	10	16	11	3	10	11	8	5	13	3	13	8
Group 23	2	2	12	3	15	5	8	3	5	14	12	9	8	9	14
Group 24	2	3	6	16	12	16	3	13	13	6	7	9	2	12	7
Group 25	2	3	8	2	9	15	14	3	14	9	5	5	15	8	12
Group 26	2	4	7	9	5	4	9	11	2	14	5	14	11	16	16
Group 27	2	4	13	12	12	7	15	10	5	2	15	5	13	7	4
Group 28	2	5	9	9	3	12	8	14	15	12	14	5	3	2	15
Group 29	2	5	11	7	2	11	9	4	16	7	16	9	14	14	4
Group 30	2	6	2	13	3	3	12	9	7	16	6	9	16	13	12
Group 31	2	6	9	7	7	16	13	3	12	2	13	12	9	16	6
Group 32	2	7	12	15	2	12	4	10	13	15	13	4	5	5	10
Group 33	2	7	14	16	5	9	2	9	16	11	11	5	7	4	14
Group 34	2	8	5	12	5	2	14	14	8	15	3	9	12	15	9
Group 35	2	9	13	4	2	13	8	11	6	4	6	8	15	15	11
Group 36	2	10	3	2	13	16	8	10	8	13	11	11	16	3	5
Group 37	2	11	15	3	11	6	14	10	15	10	6	7	7	14	3

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 38	2	16	4	5	16	14	7	11	4	11	14	9	9	7	5
Group 39	3	3	4	6	11	12	13	6	12	14	4	5	13	5	14
Group 40	3	3	6	5	16	9	15	5	9	10	6	4	15	4	10
Group 41	3	4	5	14	4	6	12	13	5	13	6	11	11	12	14
Group 42	3	4	9	16	10	4	16	15	3	5	10	5	15	6	6
Group 43	3	4	16	10	5	10	4	9	9	16	15	6	3	5	15
Group 44	3	5	12	11	14	5	11	13	3	6	14	6	13	4	4
Group 45	3	6	4	10	6	5	9	15	4	15	5	16	16	9	10
Group 46	3	7	8	8	16	11	12	4	15	11	4	7	16	3	15
Group 47	3	7	16	11	4	15	3	15	11	12	12	4	7	8	16
Group 48	3	8	7	15	4	8	15	12	3	16	4	16	12	11	11
Group 49	3	8	15	4	16	4	8	7	7	15	12	11	3	16	12
Group 50	3	10	10	15	16	5	4	6	16	4	3	15	9	6	9
Group 51	3	13	11	5	4	12	4	11	6	6	5	3	14	13	12
Group 52	3	14	7	9	14	10	13	8	7	8	10	4	4	13	9
Group 53	5	5	8	14	16	13	6	14	13	7	8	15	6	15	7
Group 54	5	6	11	7	10	8	5	8	7	12	12	10	6	9	11
Group 55	5	6	13	8	13	5	7	7	6	16	14	15	8	16	15
Group 56	5	7	9	10	7	11	6	12	9	12	11	8	8	6	10
Group 57	5	9	6	8	10	9	8	12	5	11	10	11	12	7	7
Group 58	5	10	10	12	8	11	9	7	8	9	5	12	6	7	6
Group 59	5	10	12	6	5	12	8	9	7	6	7	8	11	11	9
Group 60	5	13	15	15	14	8	6	7	16	8	7	13	14	5	16
Group 61	9	10	13	10	11	15	15	9	16	12	14	13	16	14	11
Group 62	9	11	12	15	12	9	13	13	11	14	10	16	15	14	16
Group 63	9	12	10	15	13	14	9	14	15	11	11	13	12	16	10

Appendix B

Table B.1: Slot formats of downlink DPCH

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot			Transmitted slots per radio frame N_{Tr}
					N_{Data1}	N_{Data2}	N_{TPC}	N_{TFCI}	N_{Pilot}	
0	15	7.5	512	10	0	4	2	0	4	15
0A	15	7.5	512	10	0	4	2	0	4	8-14
0B	30	15	256	20	0	8	4	0	8	8-14
1	15	7.5	512	10	0	2	2	2	4	15
1B	30	15	256	20	0	4	4	4	8	8-14
2	30	15	256	20	2	14	2	0	2	15
2A	30	15	256	20	2	14	2	0	2	8-14
2B	60	30	128	40	4	28	4	0	4	8-14
3	30	15	256	20	2	12	2	2	2	15
3A	30	15	256	20	2	10	2	4	2	8-14
3B	60	30	128	40	4	24	4	4	4	8-14
4	30	15	256	20	2	12	2	0	4	15
4A	30	15	256	20	2	12	2	0	4	8-14
4B	60	30	128	40	4	24	4	0	8	8-14
5	30	15	256	20	2	10	2	2	4	15
5A	30	15	256	20	2	8	2	4	4	8-14
5B	60	30	128	40	4	20	4	4	8	8-14
6	30	15	256	20	2	8	2	0	8	15
6A	30	15	256	20	2	8	2	0	8	8-14
6B	60	30	128	40	4	16	4	0	16	8-14
7	30	15	256	20	2	6	2	2	8	15
7A	30	15	256	20	2	4	2	4	8	8-14
7B	60	30	128	40	4	12	4	4	16	8-14
8	60	30	128	40	6	28	2	0	4	15
8A	60	30	128	40	6	28	2	0	4	8-14
8B	120	60	64	80	12	56	4	0	8	8-14
9	60	30	128	40	6	26	2	2	4	15
9A	60	30	128	40	6	24	2	4	4	8-14
9B	120	60	64	80	12	52	4	4	8	8-14
10	60	30	128	40	6	24	2	0	8	15
10A	60	30	128	40	6	24	2	0	8	8-14
10B	120	60	64	80	12	48	4	0	16	8-14
11	60	30	128	40	6	22	2	2	8	15
11A	60	30	128	40	6	20	2	4	8	8-14
11B	120	60	64	80	12	44	4	4	16	8-14
12	120	60	64	80	12	48	4	8*	8	15
12A	120	60	64	80	12	40	4	16*	8	8-14
12B	240	120	32	160	24	96	8	16*	16	8-14
13	240	120	32	160	28	112	4	8*	8	15
13A	240	120	32	160	28	104	4	16*	8	8-14
13B	480	240	16	320	56	224	8	16*	16	8-14
14	480	240	16	320	56	232	8	8*	16	15
14A	480	240	16	320	56	224	8	16*	16	8-14

14B	960	480	8	640	112	464	16	16*	32	8-14
15	960	480	8	640	120	488	8	8*	16	15
15A	960	480	8	640	120	480	8	16*	16	8-14
15B	1920	960	4	1280	240	976	16	16*	32	8-14
16	1920	960	4	1280	248	1000	8	8*	16	15
16A	1920	960	4	1280	248	992	8	16*	16	8-14

Note: If TFCI bits are not used, DTX shall be used in TFCI field.