

**Effects of Fabrication Parameters on Porous Silicon Structure
with Some Potential Applications**

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ABSTRACT

Effects of Fabrication Parameters on Porous Silicon Structure with Some Potential Applications

Mitra Esfahani Fard

Porous silicon (PS) is a sponge-like structure of silicon with a high surface to volume ratio and properties that distinguish it from bulk silicon. The structure is suitable for many applications such as biosensors, optoelectronic, drug delivery and solar cell devices. Although there are many reports available in the literature regarding the PS and its application but there is no work done systematically to investigate the fabrication of the PS for various applications. In this work we are investigating the PS production under various fabrication conditions. This work produces instructions to fabricate PS structures for any specific application. We have used electrochemical technique to fabricate samples of PS and undertaken studies the effects of several physical parameters like, materials doping level, light illumination, etching time, applied electric current and silicon surface defects, and chemical parameters like, impurities, and PH factor of the electrolyte during the PS preparation. In order to investigate the effect of silicon surface defects some textured surfaces of silicon samples were prepared by anisotropic etching of silicon in TMAH prior to their electrochemical etching in HF solutions. Structures were characterized using SEM, AFM and Raman spectroscopy.

For the first time, fabricated pyramidal porous silicon was used to prepare granular metallic films using electrodeposition techniques.

We have also used the pyramidal porous structures to fabricate a miniaturized gas ionization sensor (GIS). GIS works based on measuring the breakdown voltages for various gases. The sensor was fabricated using a parallel plate model having PS as one of the electrodes.

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TABLE OF CONTENTS

LIST OF FIGURES.....	viii
LIST OF TABLES.....	xii
LIST OF ACRONYMS.....	xiii
LIST OF SYMBOLS.....	xv
1. Introduction.....	1
1.1. Nanotechnology: the Power of Small.....	1
1.2. Porous Silicon.....	2
1.3. Literature Review.....	3
1.4. Objective of the Research.....	6
1.5. Organization of this Thesis.....	7
2. Porous Silicon and it Properties.....	8
2.1. Fabrication Process.....	8
2.1.1. Fabrication of Porous Silicon by Anodization.....	8
2.1.2. Fabrication of Porous Silicon by Stain Etching.....	9
2.2. Pore Type.....	11
2.3. Pore Size.....	12

2.4. Porosity.....	13
2.5. Properties of PS layer.....	14
2.6. Applications.....	17
3. Fabrication Steps and Characterization Equipments.....	19
3.1. Fabrication Steps.....	19
3.1.1. Preparation of Samples.....	19
3.1.2. Texturizing the Surface of Silicon.....	20
3.1.3. Porous Silicon Fabrication by Anodization Technique.....	23
3.1.4. The Effect of Preparation Parameters on the PS Properties.....	27
3.2. Characterization of Equipments.....	31
3.2.1. Scanning Electron Microscope (SEM).....	32
3.2.2. Atomic Force Microscope (AFM).....	36
3.2.3. Raman Spectroscopy.....	40
4. Experimental Results and Discussions.....	44
4.1. Porous Silicon Morphology Fabricated on Flat Surfaces of Silicon.....	44
4.2. Drying Techniques and Induced Defects during the Process	48
4.3. Porous Silicon Fabricated on the Textured Surface of Silicon.....	54
4.3.1. Porosity of the Pyramidal Structure.....	67
4.3.2. Oxidized Pyramidal Porous Silicon and Raman Spectroscopy.....	68
4.4. Conclusion.....	69

5. Applications of the Pyramidal Porous Silicon.....	72
5.1. Preliminary Steps.....	72
5.1.1. Gold Sputtering.....	72
5.1.2. Electrochemical Deposition.....	75
5.2. Metal Casting using Pyramidal Porous Silicon.....	78
5.3. Fabrication of Gas Ionization Sensors using Pyramidal Porous Silicon.....	83
5.3.1. Operation Mechanism of Gas Ionization Sensors.....	84
5.3.2. Fabrication of the Sensor.....	86
5.3.3. Sensor Characterization: Breakdown Voltage.....	88
5.3.4. Conclusion.....	92
6. Conclusions, Contributions and Future work.....	93
6.1. Conclusions and Contributions.....	93
6.2. Future Work.....	95
Bibliography.....	96

LIST OF FIGURES

1.1. Light emission comparison between PS with E.coli, blank PS and Planar silicon.....	5
2.1. Typical J-V curve of P ⁺ -Si in diluted HF Solution.....	9
2.2. Type of pores.....	11
2.3. Different pore types obtained in this research.....	12
2.4. Photoluminescence band of Porous Silicon, bulk silicon and polysilane.....	16
3.1. Schematic view of TMAH etching apparatus.....	21
3.2. Etched surface of silicon in 25% wt TMAH.....	22
3.3. Electrochemical etching Apparatus.....	23
3.4. Experimental set-up of the PS fabrication process.....	23
3.5. Images of PS fabricated on textured and smooth surface of silicon.....	25
3.6. Anodic I-V characteristics of p-type silicon with different doping in HF solution.	29
3.7. Anodic I-V characteristics of n-type silicon with different doping in HF solution.	29
3.8. Anodic I-V characteristics comparison of p- and n-type silicon in a 35% HF.....	30
3.9. Schematic view of a typical SEM.....	32
3.10. Schematic image of the source of electron in SEM.....	33
3.11. Hitachi SEM model S-4700.....	34
3.12. Specimen height adjustments.....	35
3.13. Schematic diagram of AFM.....	36
3.14. Multi Mode AFM, model AFM2 with AS-130 (J) Scanner.....	39
3.15. Energy band diagrams of Raman scattering and Rayleigh scattering.....	41

3.16. LabRAM HR spectrometry.....	43
4.1. Some of the porous silicon structures obtained by various fabrication parameters..	45
4.2. SEM image of a cracked p-type sample.....	49
4.3. SEM image of a cracked n-type sample.....	50
4.4. Image of the surface of PS under the cracks.....	50
4.5. Supercritical and freeze drying phase diagram.....	51
4.6. Image of nanocrystalline silicon.....	52
4.7. PS made of n-type silicon, I=35mA, t= 50min, with cracked surface.....	53
4.8. PS made of n-type silicon, I=35mA, t=50min, 5 minutes NaOH post processing..	54
4.9. Cross section of a PS made of n-type textured silicon, I=85mA, t= 30min.....	55
4.10. Top surface of n-type PS after immersing in NaOH for 21 minutes- Sample #7....	56
4.11. Image of a pore-sample #7.....	57
4.12. Cross section image of sample #7.....	57
4.13. Titled view (45°) of sample #7.....	58
4.14. AFM image of PS structure fabricated on textured surface of Si- sample#7.....	59
4.15. 3D image of the PS structure fabricated on textured surface of Si- sample#7.....	59
4.16. Raman spectra of PS sample fabricated on textured silicon- sample#7.....	60
4.17. PS structure fabricated on textured surface of silicon -sample#8.....	61
4.18. Top view of the sample#8.....	62
4.19. PS structure fabricated on textured surface of silicon -sample#9.....	62
4.20. Raman spectra of PS sample fabricated on textured silicon -sample#9.....	63
4.21. Textured surface of Si-(High density of hillocks).....	64

4.22.	Cross section of PPS fabricated on Si surface of low-concentration hillocks.....	65
4.23.	Cross section of one pyramid from sample #10.....	65
4.24.	Top view of the fabricated PS-sample #10.....	66
4.25.	Tilted view of sample #10.....	66
4.26.	Oxidized surface of pyramidal porous silicon.....	68
4.27.	Raman spectra of TO mode of oxidized PS sample#7.....	69
5.1.	Schematic view of sputtering machine.....	73
5.2.	MagSput-2G2 sputtering machine.....	74
5.3.	Schematic view of electrochemical deposition apparatus.....	76
5.4.	Schematic view of the Au/Ag deposition on PS to fabricate granular structures...	79
5.5.	PS sample with a layer of metal deposited on top of it.	79
5.6.	Image of the silver pyramids made by 1.5 hr electrodeposition on PS.....	80
5.7.	Image of the gold pyramids made by 28 hr electrodeposition on PS.....	81
5.8.	Cross section image of deposited gold.....	82
5.9.	Cross section of a deposited gold layer.....	82
5.10.	Top view of a PS with deposited gold on it.....	83
5.11.	I-V gaseous discharge characteristics of a parallel electrode.....	85
5.12.	Schematic view of fabricated GIS.....	87
5.13.	Cross section view of the fabricated GIS.....	87
5.14.	Schematic illustrations of measurement apparatus.....	88
5.15.	Pre-breakdown discharge current of GIS for PS as Cathode in low pressure air...	89
5.16.	I-V curve of the GIS in argon.....	90

5.17. I-V curve comparison for GIS with different gap distance.....91

LIST OF TABLES

2.1. Pore typology definition by IUPAC.....	12
2.2. Application area of PS as per the properties specifications.....	17
3.1. Some of the anodization conditions and silicon types used during this research.....	26
3.2 Effect of anodization conditions on the PS formation.....	27
3.3. Resolution comparison between eye and several other microscopy methods.....	33
3.4. Specifications of the Tapping mode etched silicon probe (TESP).....	39
4.1. The obtained pore size and thickness using different anodization conditions.....	46
4.2. Fabrication criteria for specific applications of PS as observed in this work	70
5.1. Sputtering applied criteria during this research.....	74
5.2. V_b comparison for sensors fabricated with different gap distances.....	91

LIST OF ACRONYMS

AFM	Atomic Force Microscope
AgNW	Silver Nanowire
a-Si	Amorphous Silicon
AuNW	Gold Nanowire
CNT	Carbon Nanotube
c-Si	Crystalline Silicon
DC	Direct Current
DI Water	De-Ionized Water
EBL	Electron Beam Lithography
FD	Freeze Drying
FED	Field Emission Device
GIS	Gas Ionization Sensor
IUPAC	The International Union of Pure and Applied Chemistry
LED	Light Emitting Diode
MEMS	Micro-Electro-Mechanical System
NC Mode	Non-Contact Mode
PD	Photo-Detector
PL	Photoluminescence
PPS	Pyramidal Porous Silicon
PS	Porous Silicon
PSD	Position Sensitive Detector

RCA	Radio Corporation of America
RF	Radio Frequency
SD	Supercritical Drying
SEM	Scanning Electron Microscope
SERS	Surface Enhanced Raman Spectroscopy
TESP	Tapping-mode Etched Silicon Probe
XRD	X-Ray Diffraction
2-D	2 Dimension
3-D	3 Dimension

LIST OF SYMBOLS

A	Area of the deposition	[cm ²]
$\text{Cos}\theta$	Curvature of the gas liquid interface	-
d	Density of bulk silicon	[gr.cm ⁻³]
d_{gap}	Electrode distance	[μm]
e	Charge per electron	1.602x10 ⁻¹⁹ [C]
E	Effective electric field	[Vcm ⁻¹]
F	Faraday constant	96485[C.mol ⁻¹]
J	Current density	[A.cm ⁻²]
J_{ep}	Electropolishing current density	[A.cm ⁻²]
n	Number of exchanged charge	-
N_a	Avogadro's number	6.02x10 ²³ [mol ⁻¹]
P	Gas pressure	[torr]
$P\%$	Porosity	-
Q	Total charge	[C]
S	Electrochemical etched area	[cm ²]
T	Thickness of the deposited metal	[μm]
t_{dep}	Deposition time	[hr]
V_b	Breakdown voltage	[V]
W	Weight of the deposited metal	[gr]
W_p	Pore thickness	[μm]
γ_l	Liquid surface tension	[dyn.cm ⁻¹]
Δp	Pressure drop	[kPa]
λ	Number of exchanged charge	-

$\lambda_{incident}$	Incident photon wavelength	[μm]
$\lambda_{scattered}$	Scattered photon wavelength	[μm]
ρ_v	Metal density	[gr.cm^{-3}]

Chapter 1

Introduction

1.1. Nanotechnology: the Power of Small

In a paper published in 1905, Albert Einstein estimated the diameter of a sugar molecule to be about 1nm and this is how nano-scale science journey began [1]. According to the International Organization for Standardization, nanotechnology is "the science of engineering matter at the atomic and molecular stage". The word "Nano" was originated from the Greek word nanos, meaning Dwarf [2]. The term "Nanotechnology" was first defined by Professor Norio Taniguchi of Tokyo Science University in 1974 [3].

Nanotechnology is the study of nano-sized materials in the range of 1-100 nanometers ($1 \text{ nm} = 10^{-9} \text{ m}$) and the aim is to discover new properties and to produce new devices with novel functionalities that rely on the size of the material. There are many reasons that scientists and researchers have intense interests toward nanotechnology. The most important reason is that most of the materials show new properties and functions when they are downsized to nanoscale due to quantum effects and surface effects [4-5].

Most of nanomaterials have large surface to volume ratios, which makes them very suitable for many applications such as drug delivery, composite materials, sensing, and reacting systems [6]. Relatively high surface area to volume ratio in nanomaterials changes their chemical and biological properties due to high interactions between their atoms and surrounding environments. Also, due to the small sizes their physical properties follow the quantum mechanical laws rather

than classical physics fundamentals. Generally, the physical, mechanical, chemical and biological properties of these nanoscale structures become size-dependent.

1.2. Porous Silicon

Structures with at least one dimension in the range of 1-100nm are called nanostructures. There are different forms of nanostructures such as quantum dots, nanotubes, nanowires, nanoparticles and nanolayers. Among materials used to fabricate nano structures, there have been increasing interests toward fabrication of semiconductor devices with sizes in the range of nanometers. In this context silicon which is the most common semiconductor used in microelectronics, has been the subject of numerous researches in the field of nanosciences and nanotechnology. Porous Silicon (PS) is a form of silicon with a network of pores grown on its surface which has an extremely large surface to volume ratio ($500\text{m}^2/\text{cm}^3$). It typically has porosities (volume of the voids spaces over the bulk volume of a material) in the range of 4% - 95%. Since its discovery in 1956, there has been a lot of interest toward fabrication of porous silicon and its applications. Due to nano size and the high surface to volume ratio, PS has specific chemical and physical characteristics such as higher elasticity, lower thermal conductivity, higher resistivity, visible photoluminescence and direct band gap structure comparing to bulk silicon. Today, PS is used in many applications such as gas sensors, bio-sensors, solar cells and optoelectronic devices due to cost effective and simple fabrication and its phenomenal properties.

In summary:

- The large surface area of PS is suitable for many sensing applications.
- PS has a very high degree of biocompatibility and biodegradability that makes it suitable for biomedical sensors.

- The visible photoluminescence of PS has brought significant attention toward optoelectronic applications.
- The highly textured surface of PS is used in solar cells as an antireflection coating.

1.3. Literature Review

Porous silicon (PS) can be considered as bulk silicon with a sponge-like surface. In other words, PS is a form of silicon with nano-sized pores in the typical range of 3 nm to 1 μ m, representing a large surface to volume ratio.

In 1956, for the first time PS was discovered by Arthur Uhlir and Ingeborg Uhlir while they were working at the Bell Laboratories on an electropolishing process on silicon. Electropolishing normally happens above a threshold current density (J_{ep}) and they found out that below J_{ep} instead of electropolishing, a brownish layer forms at the surface of silicon which today is known as porous silicon [7].

In a study by M.D.B Charlton and G.J Parker [8], high aspect ratio silicon microstructures were fabricated using anodic etching of silicon. With this technique, free standing silicon pillars of 20 μ m in height and 150nm in diameter were obtained. Taking into the account the fact that sharp spots at the surface act as seeding point for macro-pores formation, they have pre-patterned the wafer surface with defect sites, therefore the location of macro-pores were pre-defined on the surface (surface patterning). Photolithography followed by KOH etching was used to create pyramidal defects in the required positions.

Using the same technique porous silicon was used to grow the silicon films for solar cells by D.Kuchler et al [9].

I.Kelps et al. [10] fabricated silicon field emitter arrays using porous silicon as a sacrificial layer. Silicon surface was selectively covered by silicon carbonitride mask, so the area of porosification were defined, then porous silicon were formed in the open windows between the masks using electrochemically etching process. Silicon carbonitride mask was removed by oxidizing the sample and etching the oxide away by HF. The remained substrate was a series of silicon emitters with tip radius of 500nm.

In a research on porous silicon field emission cathode done by J.R. Jessing and coworkers [11], the large electric field enhancement and large stable current emission of porous silicon was investigated. The idea was to oxidize a thin porous silicon layer on top of a silicon substrate and then deposit metal over the film and measure the I-V characteristics of the device. They have porosified low resistivity p-type silicon by electrochemically etching in a concentrated HF solution. The resulting porous layer was oxidized then covered by metal dots with 0.8mm diameter via shadow-mask evaporation. The nano-scale tips formed at the base of the pores served as the cathode and deposited metal served as anode. The device showed stable I-V characteristics and the estimated electric field emission was approximately 1.09×10^4 V/cm. The group also investigated the I-V characteristics of silicon pyramids formed under silicon dioxide layer.

PS was also used for detecting the E.coli bacteria by Mathew and Alocilja [12] using photoluminescence properties of PS. In this research a chemiluminescence single-tube assay previously developed by the same group was adopted to PS for detection of E.coli. Fabricated PS chips were functionalized with a mixture of dioxetane and polymyxin B sulfate (E.coli cell wall permeabilizer). Light emission obtained from the PS biosensor chips with E.coli was three times larger than the one obtained from planar silicon due to the PS larger surface area. Figure 1.1 is the

comparison of light emission of a blank PS biosensor chip (no E.coli), porous silicon and planar silicon biosensors with E.coli.

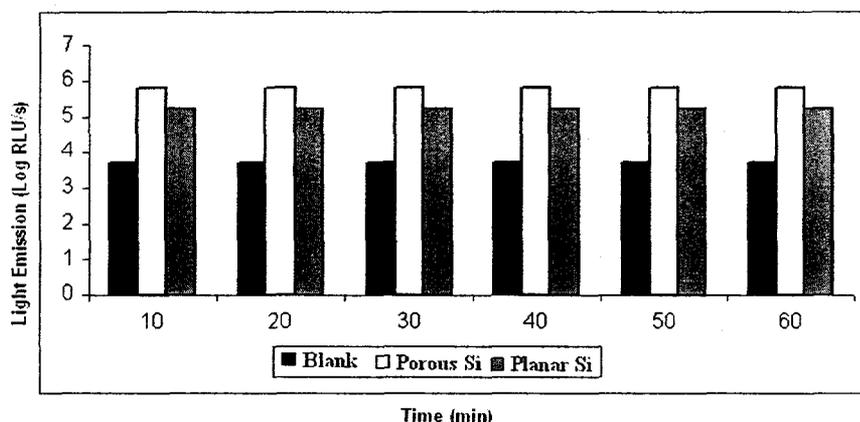


Figure 1.1 (adapted from P. Mathew et al) Light emission comparison of PS biosensor chip, no E.coli (■), Porous silicon with E.coli (□) and planar silicon biosensors (▒) [12].

As it is shown in Figure 1.1, light emission of blank PS was significantly lower than the other two structures, thus proving that both porous silicon and planar silicon chips were able to detect the E.coli bacteria, but the light emission from PS biosensor was significantly higher than the one from planar silicon (about 3 times) due to the PS larger surface area.

L.Vaccari and his group [13] investigated the possibility of using two-layer PS as a carrier for time-controlled delivery of doxorubicin anticancer agent. Two-layer PS samples (a layer of nanoporous on top of the macroporous) has been prepared by electrochemical etching technique. P-type silicon with 5-10 Ω -cm resistivity was etched by constant current density 5.56 mA/cm² in HF-ethanol solution using different etching time in order to obtain two different layer of PS. This structure has more advantages for the loading of liquid form of drug into the pores due to a higher nanoporous exposed surface per unit volume of material. At the same time this structure has a thinner nanoporous layer, easier to dissolve. The dissolution of nanoporous layer in DI water, ethanol and a physiological solution were studied and the results showed no modification in

layers structure or in their PL behavior for the samples exposed to DI water and ethanol for 24hours. However, the nanoporous layer was completely dissolved in the physiological solution and its PL behavior disappeared. Considering the above results, the authors devised a method of loading PS samples with doxorubicin and releasing it in the physiological environment by dissolution of nanoporous layer.

R.J.Martin-Palma et al [14] have modified the emitter of polycrystalline silicon solar-cells with chemically etching the samples in order to form porous silicon layers as an antireflective layer.

A porous silicon microcavity resonator LED has been demonstrated by S. Chen and P.M. Fauchet [15] for the first time. The group has made this device using a sandwich structure of all PS layer, having a thin-high porosity layer of porous silicon between two reflectors made of several pairs of high-low refractive index of porous silicon layers. The obtained results revealed the potential use of PS for high quality, flat panel color displays due to the reduced spectral width and higher directionality of the LEDs made of PS layer.

1.4. Objective of the Research

This thesis is the result of studies and investigations on fabrication of porous silicon structures for various applications. It is expected that our work produces a relatively comprehensive data base and/or instructions to fabricate PS structures for any specific application. For this we have produced samples of PS fabricated using electrochemical etching technique. The aim is to study the effects of anodization parameters such as anodization current density, etching time, light illumination, HF concentration and silicon type on PS morphology. In order to investigate the effect of silicon surface defects some textured surfaces of silicon samples

were prepared by anisotropic etching of silicon in TMAH prior to their electrochemical etching in HF solutions. Structures were characterized using SEM, AFM and Raman spectroscopy. We have investigated the possibility of PS application to fabricate a gas ionization sensor (GIS). For this, periodical arrays of pyramidal pores were produced on high doped n-type silicon samples. The fabricated device was compared to those fabricated using metallic nanowires in our laboratories. For the first time, fabricated pyramidal PS structure was also used as a casting template to fabricate metallic structures like gold and silver films.

1.5. Organization of this Thesis

In the next chapter, Chapter 2, PS fabrication techniques, its properties and applications are presented. Experimental procedure to fabricate PS is discussed in chapter 3. Also characterization techniques and facilities such as SEM, AFM and Raman Spectroscopy are presented in this chapter. In chapter 4, experimental results and characterization of the fabricated samples are demonstrated. Chapter 5 discusses some applications of fabricated PS structures. Conclusion, contribution and future work of this research are presented in chapter 6.

Chapter 2

Porous Silicon and its Properties

2.1. Fabrication Process

PS is formed by etching (electrochemically or chemically) of silicon in the presence of hydrofluoric acid. A partial dissolution of silicon happens due to reactions occurring at the surface of silicon which leads to formation of PS. Different PS fabrication techniques have been proposed followed by different reaction mechanisms. The two most used ones are presented below:

2.1.1. Fabrication of Porous Silicon by Anodization

In this method, the formation of PS is performed by electrochemical etching of silicon during anodization. The silicon wafer is etched by HF at the presence of an anodic current or potential. The fabrication cell is made of a teflon container filled with electrolyte solution. Silicon samples cover the bottom side of the container. A platinum (Pt) electrode is placed inside the container acting as cathode and the anode is connected to the bottom of the silicon sample. The anodic current passes through the solution and leads to dissolution of silicon at the surface. The current density used during the electrochemical etching of silicon (PS formation) should be lower than a typical current density called electropolishing current density, J_{ep} . This is a critical value for chemical reactions involved in silicon dissolution and PS formation. These reactions only happen in the presence of positive carriers (holes) in silicon and only if holes present at the interface of silicon surface and the electrolyte solution. This condition is fulfilled for current densities below

J_{ep} . Above this current, the chemical reaction is limited by ionic mass transfer and this leads to the surface charge of holes and finally smoothing of the surface (electropolishing) [7]. Figure 2.1 represents the typical J-V curve of silicon in diluted HF solution.

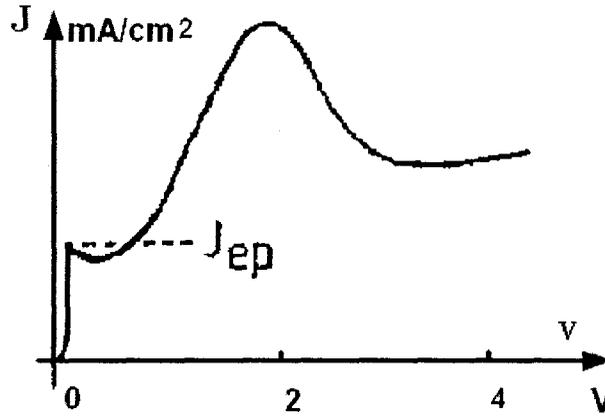


Figure 2.1 Typical J-V curve of P⁺-Si in diluted HF Solution [16].

At first the current rises exponentially with applied voltage. Formation of PS conducts in this region until the small sharp peak that corresponds to the J_{ep} , electropolishing peak. This current depends mostly on the applied chemical composition and the substrate. At this peak, oxide formation begins. The current density starts to increase again with applied voltage until it reaches the second peak in the curve. This part of the curve represents electropolishing region.

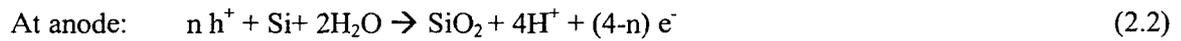
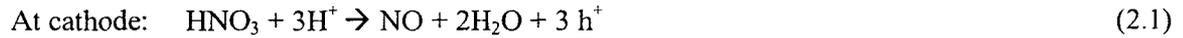
Anodization technique is the method that we used to fabricate PS in this research. It will be discussed in details in chapter 3.

2.1.2. Fabrication of Porous Silicon by Stain Etching

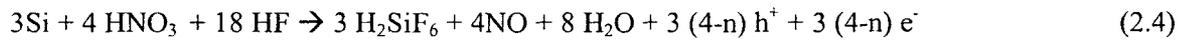
The second method that is used for preparation of porous silicon is the use of an open-circuit chemical stain-etch bath containing diluted HF and nitric acid. In this chemical etching of silicon a mixture of HF: HNO₃: H₂O is used without applying any bias [17]. As in electrochemical

technique discussed in previous section, the key component for the reactions is the existence of holes “positive carriers” (h^+).

The model that can describe chemical reaction mechanism occurring during stain etching of silicon is given as [18]:



The overall reaction will be:



which h^+ and e^- represent exchanged holes and electrons respectively and n is the number of exchanged charges.

Porous films that are formed by this method are even thinner than the porous silicon fabricated by electrochemical etching of silicon, so when very thin PS films of uniform depth are required, stain etch technique is preferred.

What is produced in both methods is a sponge like surface of silicon with properties that are different from the bulk silicon.

2.2. Pores Type

A 'pore' is an etch pit whose depth, d , exceeds its width, w . Figure 2.2, shows the different types of pores that can be created in bulk silicon by electrochemical etching. Most pores are generally closed at one side (Figure 2.2-a, b, c) or closed on both sides (Figure 2.2-d) that are created by reconstruction of pore networks via annealing. Some pores are open at both sides, (Figure 2.2-e), that can be created on ultra thin silicon wafers or by extension of anodization period.

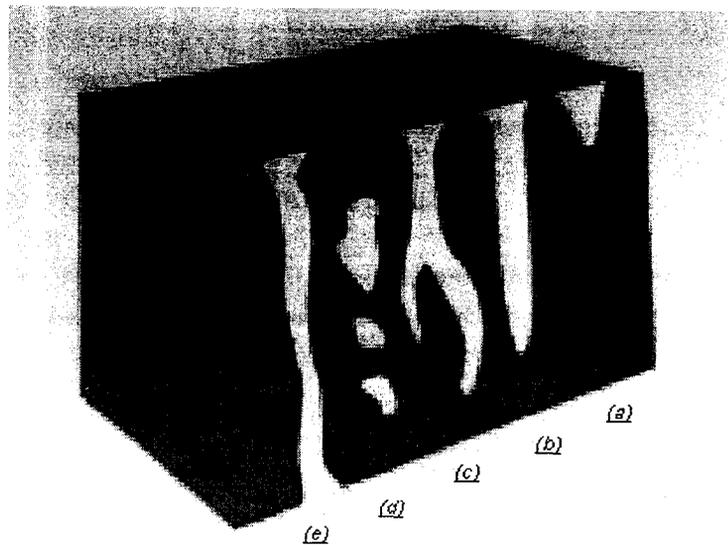


Figure 2.2 (adapted from L.Canham) Types of pores: (a, b) blind, dead-end, (c) interconnected or branched, (d) totally isolated or 'closed', (e) 'through' pores [16].

Figure 2.3 represents different type of pores obtained during this research work. The shapes are generally classified as Cylindrical, Ink-Bottle, Cone shaped, Cuboids, Triangular or Pyramidal pores. The various shapes and types of pores are created by changing the type of substrate or anodization conditions such as current density, etching time and illumination.

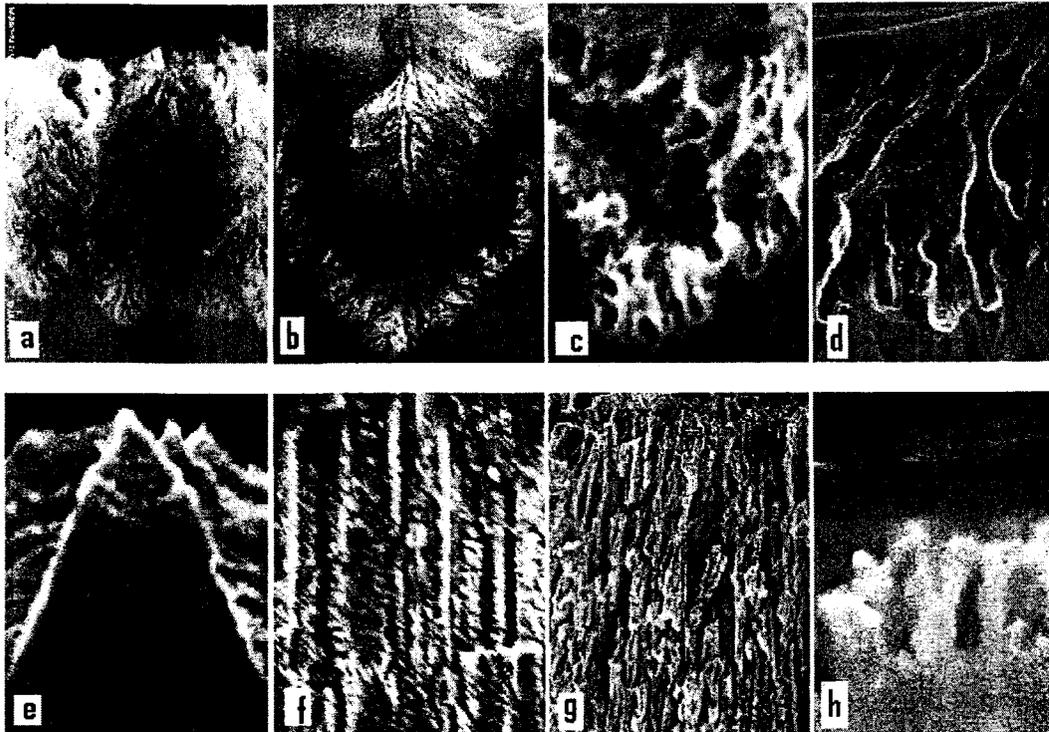


Figure 2.3 Different pore types obtained in this research (a, b) branched or tree structure, (c) sponge, (d) closed, (e) pyramidal, (f, g, h) filament or cylindrical pores

2.3. Pores Size

Due to the vast application areas of PS such as sensing, and photonic devices, the pore size has a major role in the determination of material properties. The sizes of pores are classified by IUPAC (The International Union of Pure and Applied Chemistry) depending on their width. Table 2.1 illustrates pore size definitions.

Table 2.1 Pore typology definition by IUPAC

Pore Width (nm)	Type of Pore
≤ 2	Micro
2-50	Meso
>50	Macro

The pore size is the key parameter in sensing and filtering applications because it determines the absorption properties of porous silicon. Obviously, precise pore size can be defined only for pores with a well-defined geometrical shape.

2.4. Porosity

Porosity indicates how much of a material is porous. It is defined as the ratio of the volume of the pores in a material to the total or bulk volume (including void and solid components) of the material. Originally it is measured by weighting the wafers in different stages of process and by the use of the following equation:

$$P(\%) = \frac{(m_1 - m_2)}{(m_1 - m_3)} \quad (2.5)$$

which m_1 is the weight of the virgin wafer before anodization, m_2 is the weight of the wafer after anodization and m_3 is the weight of the wafer after dissolution of the whole porous layer in aqueous KOH or NaOH. This is called the gravimetric method.

From the measured porosity, the thickness of porous layer can be determined from the following equation:

$$W_p = \frac{(m_1 - m_3)}{S \times d} \quad (2.6)$$

where d is the density of bulk silicon and S is the electrochemical etched area of the wafer [16].

Other technique may be used to measure porosity and the thickness of the samples is using SEM or XRD pictures of the samples.

2.5. Properties of PS layer

Elastic property of a material determines how much that material will be compressed when a given amount of external pressure is applied to it. Elastic property of PS is measured by calculation of Young's moduli utilizing X-ray diffraction, acoustic investigation, nanoindentation investigation and Brillouin Scattering characterization. The techniques that were used have shown that PS has a lower stiffness comparing to bulk silicon. As an example using XRD, it was found that PS material is less stiff than bulk silicon and the stiffness decreases with density. The Poisson ratio of PS layer has also been determined. The calculated value was smaller than that of bulk silicon ($\nu_p=0.09/\nu=0.26$) [19]. Also it was found that high porosity porous silicon is less stiff than low porosity PS [20].

Microhardness is the resistance of a solid to deformation when a force is applied. By measuring the hardness of porous silicon, valuable information on the material strength, surface quality and crystallite size can be obtained. It is known that the hardness of PS decreases with increasing porosity. For PS with 80% porosity, the hardness is about 2GPa which is very low compared to the hardness of bulk silicon (12GPa) [16].

Thermal Conductivity indicates the ability of PS to conduct heat and it should be considered when PS is used in a device. Because of the porous structure, thermal conductivity is very low in PS, and it decreases with increasing the porosity. The nanoporous material can be used as an insulator, because heat is not transferred by nano-structured pores from one element to another. In a research done by G.Gesele and the group, thermal conductivity of PS was measured by 3w technique. The obtained results showed that thermal conductivity of PS is three to five

orders of magnitude smaller than the values for bulk silicon. Furthermore, they have obtained that increasing the wafer's doping level, decreasing the porosity of PS layer and increasing the temperature lead to increment of thermal conductivity of PS [21].

Resistivity of PS layer depends on several factors such as porosity and the ambient atmosphere and so far several techniques have been proposed for resistivity measurement such as two-terminal measurements of PS sandwich structure or four-point probes measurements. The resistivity of low porosity porous silicon is close to that of bulk silicon and it increases with increasing porosity [22]. In high porosity nano-size porous silicon resistivity is higher than that of low porosity by a few orders of magnitude [23]. Resistivity is very sensitive to the environment for both low and high porosity PS layers due to their large surface area. For example, the exposure of a PS layer to vapors of solvents, humidity or its thermal annealing decreases the resistivity by few orders of magnitude [24-26].

Refractive index determines how light waves spread inside a material and this is a very important characteristic for optical and optoelectronic devices. Refractive index of PS is lower than that of bulk silicon due to the porous structure. PS is a two phase composite (a combination of air and solid) and the refractive index changes depending on the topology of PS. Increasing the porosity of PS leads to decrement of refractive index. The advantage is that by changing porosity, a large range of refractive index can be obtained. This is very useful for optical applications and the design of devices with predictable optical properties [16, 27].

Porous Silicon Bandgap: As per several studies on porous silicon, it is known that this material has a direct bandgap. Silicon-based nanostructure has an adjustable bandgap transmitting from indirect in bulk silicon to direct in porous structures. This transmission is caused by porosity, pore wall's width and pore array distribution which makes PS suitable for light emitting and solar devices [28].

Visible photoluminescence from PS is obtained in a wide range of wavelengths from the ultraviolet to the infrared. It is known today that nanocrystalline PS emits visible light due to quantum size effects. The highest interest is toward the PL band of PS, which is observable from freshly etched PS [29], after anodic or chemical oxidation [30], or from high porosity silicon when it is still inside the HF solution [31].

Figure 2.4 shows the PL band of PS, bulk silicon and polysilane (a polymer).

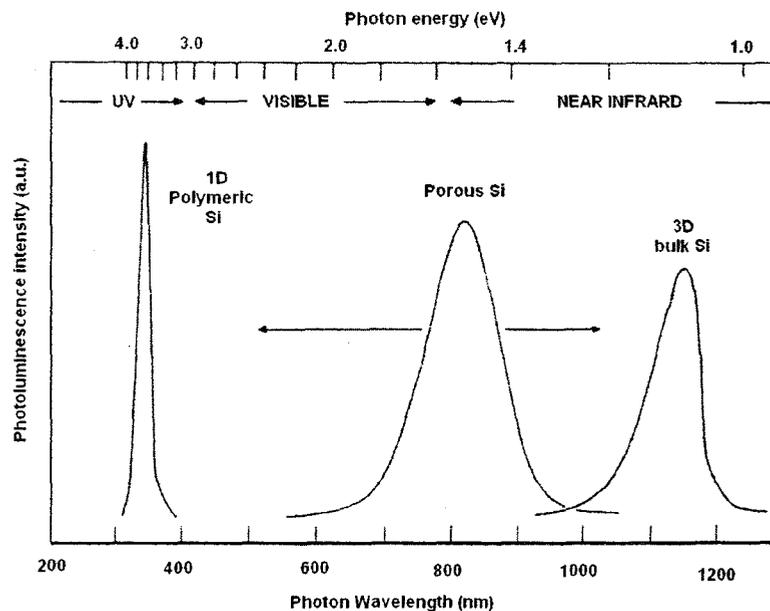


Figure 2.4 (adapted from L.T.Canham) Photoluminescence band of porous silicon, bulk silicon and polysilane[32].

As the figure shows the spectral location of emission from bulk silicon and the polymer is fixed, but the one from PS is tunable. [32]

2.6. Applications

Due to significant material characteristics, PS is a good candidate for many application areas.

Table 2.2 represents a set of PS applications.

Table 2.2 (adapted from A. E. Pap) Application area of PS as per the properties specifications [33]

Application area	Component based on PS	Utilized properties of PS
Optical applications	Solar cell (antireflection coating)	Tunable refractive index and layer thickness by manufacturing
	Waveguide	Tunable refractive index and thickness, Direct integration with electrical components
Optoelectronic applications	Light emitting diode (LED)	Electroluminescence Schottky contact with some metals p-n junction without ion bombardment
	Photo-detector (PD)	p-n junction without ion bombardment Wavelength dependent refractive index and absorption coefficient
	Field emission device (FED)	Free charge carriers generation
	Photonic crystal	Designable 2 and 3 D structure by periodically alternated layers with different indices

Microelectronic applications	Epitaxial growth of silicon films on the PS surface	Suitable substrate for Epitaxial growth
	Thermal/ electrical insulation	Low thermal conductivity High electrical Resistivity
	Silicon capacitor	Macroporous structure (n-type silicon) High specific capacitance
Sensors and actuators	Micromechanical structures/ MEMS	Selective etching of PS on Si
Chemical sensors	Liquid or gas material sensing	Electrical conductivity and capacitance effect Band structure change Photoluminescence quenching Compatibility with the living organism
Biological application	Sensing	Compatibility of electrical and optical properties of PS by biomolecules

Chapter 3

Fabrication Steps and Characterization Equipments

3.1. Fabrication Steps

3.1.1. Preparation of Samples

In this work PS samples were made of pieces of one-sided polished n-type or p-type silicon. Silicon was metallized at unpolished side for the purpose of ohmic contacts. Several preliminary steps are required such as cleaning, metallization and annealing to prepare silicon samples for PS etching.

Cleaning process is an important step to prepare the samples for PS fabrication. The cleaning process used in our work is called RCA [34] which is a standard set of steps for cleaning the wafers. It is done to remove the unwanted impurities such as organic contaminants, native oxide, and ionic contaminations from the surface of samples. The samples were dipped into the boiling solution of H_2O_2 : H_2SO_4 (1:1) for 5 minutes and then rinsed with DI water. This step removes some of the organic contamination. Dipping samples in the solution of HCL : H_2O_2 : H_2O (1:1:5) is the next step. The samples are boiled in the solution for 5 minutes, and then rinsed with DI water. This step is for removing alkali ions that may exist on the surface. Third step is to dip the samples in a mixture of HF : H_2O (1:50). This step removes native oxide from the surface of samples. The last step is to mix NH_4OH : H_2O_2 : H_2O (1:1:5), heat it on a hot plate and put the samples in the solution for 5 minutes (avoid boiling) and then rinse them in DI water. This step is also for removing some organic impurities and some metals such as silver, gold, nickel, etc [34].

Metallization step is used to create a good ohmic contact that is necessary for our experiments. An ohmic contact is a contact between metal and semiconductor to make electronic carriers flow easily in and out of the semiconductor. Aluminum is the most popular metal used in metallization process. During this step, aluminum is easily deposited in vacuum chamber due to its low boiling point and high conductivity. There are different metallization methods. The method used in this work is called Filament Evaporation. In this technique, required amount of aluminum is placed in a basket that each side of it is connected to one electrode. A high current passing through heats the basket and causes the melting of aluminum and finally its evaporation. So the Al atoms will deposit onto the silicon that is located above the basket [35]. (Aluminum wire used: 1 mm diameter, 99.999%)

Annealing is carried out to make an intimate contact between the metal and surface of silicon after metallization. To perform annealing, the samples are placed in a furnace to form a low-resistance contact between the deposited aluminum and silicon substrate. The process takes place in 400°C-500°C in the presence of nitrogen and hydrogen gases. Hydrogen combines with the free atoms at the interface which helps to minimize the resistance of the samples.

3.1.2. Texturizing the Surface of Silicon

Some of the PS fabrications were carried out on textured surfaces of silicon which were created to induce defects to act as seeding points for pores. Silicon samples were textured with upright pyramids using anisotropic wet-etching of silicon in 10% or 25% wt TMAH (Tetra-methyl Ammonium Hydroxide) at 90°C for 30 minutes. It is shown that when silicon is etched along (100) plane micron size pyramids will form on the surface due to the anisotropic etching of silicon along different directions. Dissolution of silicon in HF consistently happens faster at sharp

tips (hillocks) and it slows down in the walls or flat surfaces resulting different porous structure from comparing to those fabricated on a plain silicon surface.

Figure 3.1 shows a schematic view of the silicon wet-etching apparatus.

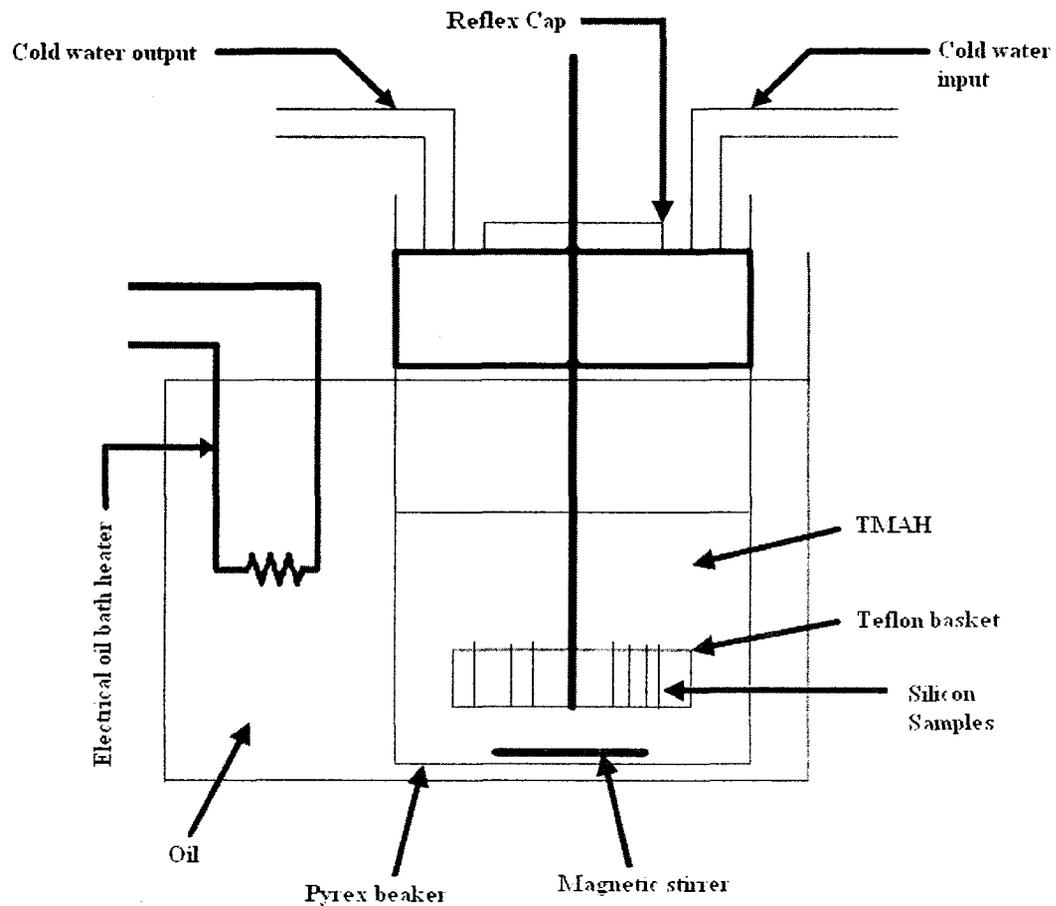


Figure 3.1 Schematic view of TMAH etching apparatus.-glass beaker filled with TMAH for etching silicon samples -Teflon basket to hold the silicon samples inside the glass beaker. -oil bath contained the whole beaker for having uniform temperature for etchant. -flux cap covered the top of the glass beaker to obtain a constant concentration of TMAH by reducing the vapor from the etchant solution. -two hoses of flux cap as an input/output for cold water during the etching. -electrical heater controlled the temperature of the oil. -magnetic stirrer to agitate TMAH.

An HF cleaning step was carried out after texturizing the silicon in order to remove the possible native oxide from the surface.

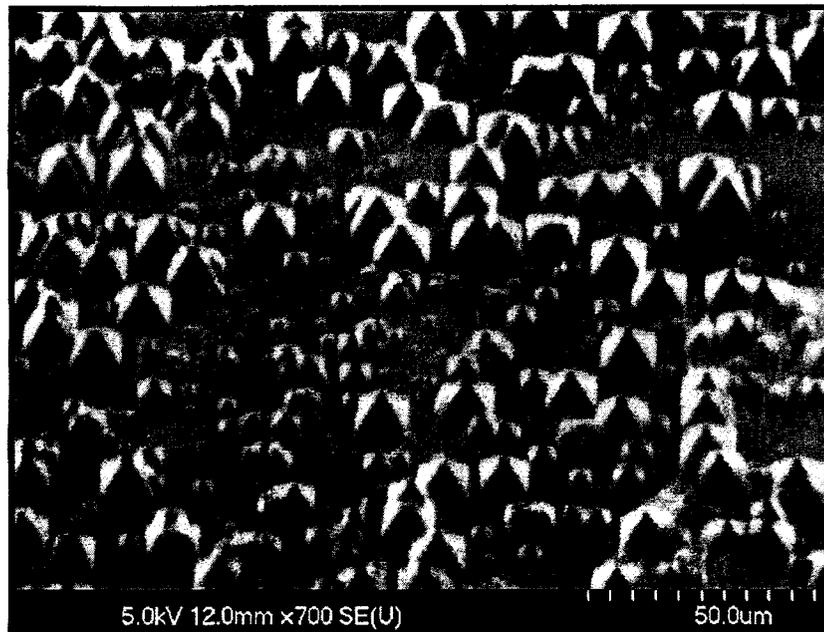


Figure3.2 Etched surface of silicon in 25%wt TMAH

As it is shown in Figure 3.2 the surface of silicon is covered by hillocks. A single hillock has an octagonal base (mostly looks like a square-shaped base) with triangular facets. These defects created on the surface of silicon will act as seeding points for creation of pores; therefore the location of pores will be pre-defined. The structure of the pores formed on the flat surface of silicon is different from the ones that are formed on the textured surfaces as the etch rate on the textured surfaces is not uniform. It is higher at sharp points of hillocks and lower in flat surfaces. The pores formed on textured surfaces have pyramidal shapes, almost the same structure of hillocks with better mechanical strength, higher porosity, and lower stress [36] comparing to the ones formed on the plain surfaces using the same anodization conditions and methods of drying.

3.1.3. Porous Silicon Fabrication by Anodization Technique

In this work, the formation of PS is performed by electrochemical etching of silicon during anodization. To produce PS, silicon samples were biased by specific anodic current and etched in HF. This fabrication step was carried out on both smooth and textured surfaces of silicon. Figure 3.3 and 3.4 represent the anodization cell and experimental set-up used during the electrochemical etching process.

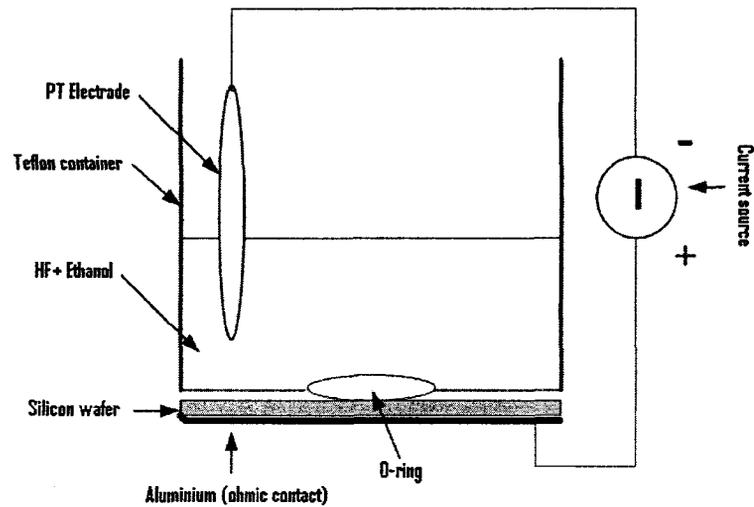


Figure 3.3 Electrochemical etching Apparatus.

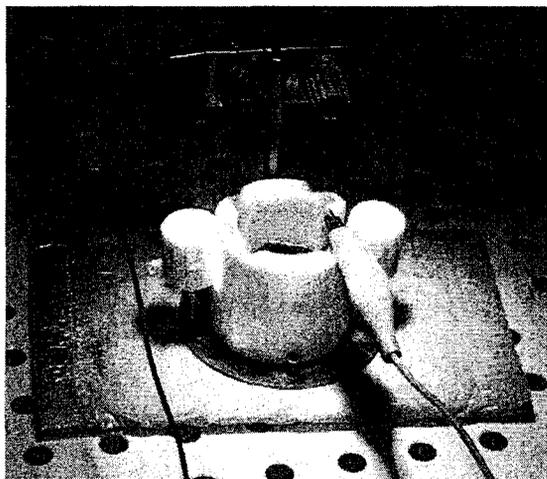


Figure 3.4 Experimental set-up of the PS fabrication process.

Silicon was exposed to the electrolyte solution containing HF and ethanol in a teflon container, using a constant current source, Model: Keithley Series 2400 Digital SourceMeter. Constant current is passed through the electrolyte, using silicon as anode and a Pt electrode located inside the teflon container as cathode. The polished sides of the silicon samples cover bottom side of the teflon container. As it was explained before the back side of the silicon samples was covered by a layer of aluminum for good ohmic contacts.

The dissolution of silicon only happens if F⁻ ions are present; to fulfill that condition, the presence of positive carriers, holes, is necessary. In the case of p-type silicon, due to the majority of positive carriers this condition is always fulfilled. For the case of n-type silicon, because holes are the minority carriers, this condition was achieved by exciting electrons using light illumination on the samples during the etching.

Several mechanisms for dissolution of silicon in HF were suggested.

The mechanism of the porous silicon formation suggested by Turner [37] is as follows:



Another model that describe the Si-electrolyte interface reaction proposed by Zhang [37] is as follows:





This latter suggests that PS growth occurs through anodic oxide formation.

The parameters h^+ and e^- in both models are the exchanged holes and electrons respectively and λ is the number of exchanged charges.

Adding ethanol to the electrolyte increases crystalline structures of the pores; therefore produces more homogeneous structures. Ethanol will remove hydrogen bubbles induced during the electrochemical reaction which makes the porous structures more uniform.

Prior to HF etching, the samples were rinsed with DI water and dried with nitrogen gas. The container was checked for any leaks before filling with electrolyte solutions.

Figure 3.5 shows two different PS samples fabricated on the textured and smooth surfaces of silicon.

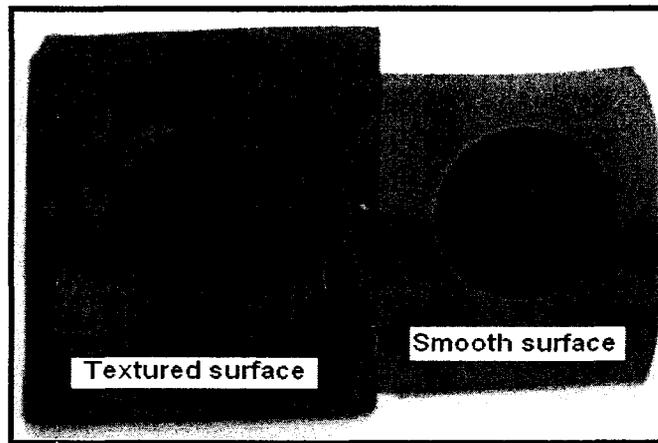


Figure 3.5 Images of PS fabricated on textured and smooth surface of silicon- Dark circled areas in both samples are the porous areas.

Various types of porous silicon were fabricated using different anodization conditions. Table 3.1 shows various parameters used to fabricate samples in this work.

Table 3.1 Some of the anodization conditions and silicon types used during this research.

Sample number	Sample Type and Resistivity	Time	Current
A(#1)	P-type<100>Br (10-20Ωcm)	15 min	2 mA
B(#3)	P-type<100>Br (10-20Ωcm)	40 min	1 mA
C	P-type<100>Br (10-20Ωcm)	15 min	5 mA
D	P-type<100>Br (10-20Ωcm)	10 min	80 mA
E	P-type<100>Br (10-20Ωcm)	15 min	3 mA
F	P-type<100>Br (10-20Ωcm)	1 hr	30 mA
G	P-type<100>Br (10-20Ωcm)	1 hr	3 mA
H	P ⁺ -type<100>Br (0.0009-0.001Ωcm)	20 min	5 mA
I	P ⁺ -type<100>Br (0.0009-0.001Ωcm)	50 sec	65 mA
J	P ⁺ -type<100>Br (0.001-0.09Ωcm)	1 hr	7 mA
K	P ⁺ -type<100>Br (0.001-0.09Ωcm)	1 hr	2 mA
L	P ⁺ -type<100>Br (0.001-0.09Ωcm)	3.5 min	60 mA
M	P ⁺ -type<100>Br (0.001-0.09Ωcm)	3.5 min	60 mA
N	N-type<100>Sb (0.01-0.02Ωcm)	50 min	35 mA
O	P-type<100>Br (0.01-0.02Ωcm)	30 min	55 mA
P	P-type<100>Br (0.01-0.02Ωcm)	2 min	135 mA
Q(#4)	N-type<100>Sb (0.01-0.02Ωcm)	2 min	70 mA
R	N-type<100>Sb (0.01-0.02Ωcm)	30 min	70 mA
S(#2)	P-type<100>Br (7-30Ωcm)	2hr	30mA
T	P-type<100>Br (25-45Ωcm)-textured	30 min	50mA
U(#9)	N-type<100>Sb (0.01-0.02 Ωcm)-textured	30 min	50mA
V(#7)	N-type<100>Sb (0.01-0.02 Ωcm)-textured	30 min	85mA
W(#8)	N-type<100>Sb (0.01-0.02 Ωcm)-textured	1.4min	85mA
X(#5)	N-type<100>Sb (0.01-0.02 Ωcm)	10min	70mA
Y(#6)	N-type<100>Sb (0.01-0.02 Ωcm)	15min	2mA

For n-type samples, the process was done under white light illumination (120v, 35W). The HF: ethanol concentration ratio was 1:1 for all samples except for samples M and Q that the ratio was 1:2 and samples T, U and V that the ratio was 1:3. The anodized area of all the samples were 3.14cm².

3.1.4. The Effects of Preparation Parameters on the PS Properties

Properties of the porous silicon layers such as porosity, layer thickness, pore size (diameter) and surface structure strongly depend on the parameters used during the preparation such as the type of substrate, anodization current, etching time, concentration of HF and illumination (anodization conditions). Table 3.2 shows the dependency of PS properties to anodization conditions briefly.

Table3.2 (adapted from O. Bisi et al) Effect of anodization conditions on the PS formation [38].

Increase in the value of:	Porosity	Etching rate	Critical current
HF Concentration	Decreases	Decreases	Increases
Current Density	Increases	Increases	--
Anodization time	Slightly increases	Slightly increases	--
Temperature	--	--	Increases
Wafer doping (p-type)	Decreases	Increases	Increases
Wafer doping (n-type)	Increases	Increases	--

Current Density Effects: Current density has a strong effect on pore morphology and PS layer properties. An increase in current density is accompanied by an increase in the growth rate of PS, also increase in current density leads to increase of porosity. According to several studies

on effect of different current densities on pore morphology[16, 22], lower current density leads to formation of smaller and filament-like pores while higher current density that is close to electropolishing regime leads to formation of pipe-like pores, meaning that an increase in current density leads to formation of pores with larger diameter.

Anodization Time Effects: The thickness of porous layer increases with increasing the etching time. Longer anodization time means that Si stays in contact with HF for a longer time and so the mass of dissolved silicon (from the porous layer) in HF is larger and the porous layer gets thicker.

Illumination Effects: As observed earlier, the formation of PS only happens in presence of positive carriers (holes (h^+)). For p-type silicon, due to the majority carriers, the required holes are always present; therefore the PS formation can happen even in the dark. But in the case of n-type silicon, holes are the minority carriers, so the PS formation condition is fulfilled under illumination that generates enough electron-hole pairs or in higher voltages that leads to breakdown. For example for the case of low doped n-type silicon ($n < 10^{18} \text{ cm}^{-3}$) in the dark, PS formation only happens at voltages higher than 5V when the required holes are formed by breakdown and ionization processes and this leads to creation of macroporous layers. Under illumination, a lower voltage ($< 1\text{v}$) is required to create PS layer for n-type silicon [16].

Silicon Type and Doping Level Effects: PS structure ranges from microporous to macroporous by changing the type and doping level of silicon. In the case of n-type silicon, porosity increases with increasing the doping concentration and there will be a decrement in pore

diameter. For p-type silicon, porosity decreases with increasing the doping concentration and also there will be an increment in pore diameter. The anodic J-V characteristics for p and n type silicon wafers with different doping concentrations in HF solution are shown in Figures 3.6 and 3.7. In both p and n-type silicon, increasing the doping concentration will cause the curves to shift toward the cathodic potential (lower anodization potential), therefore PS formation rate in high doped silicon is faster than low doped ones.

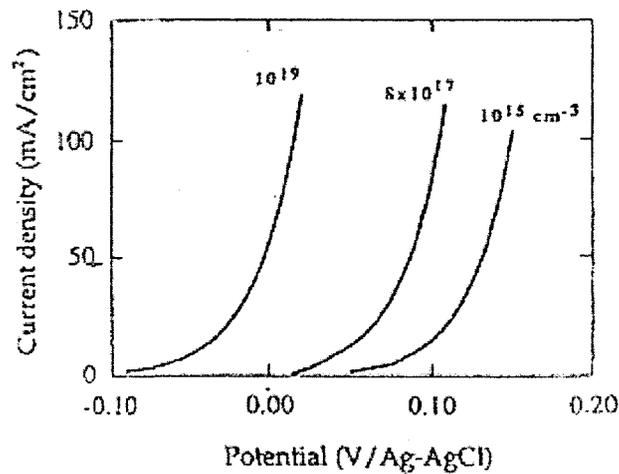


Figure 3.6 (adapted from L. Canham) Anodic I-V characteristic of p-type silicon in a 35%-HF solution and with different substrate doping concentrations [16].

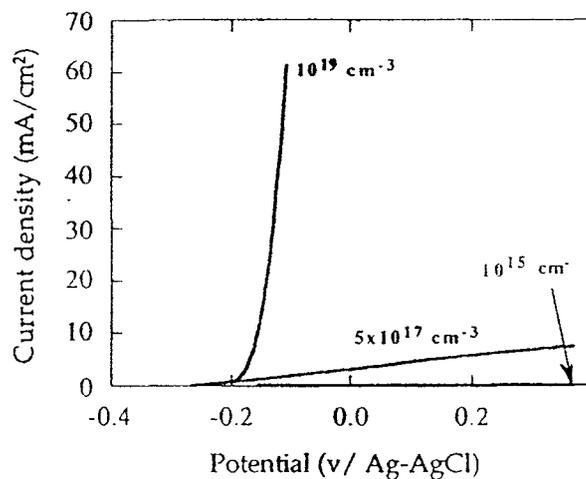


Figure 3.7 (adapted from L. Canham) Anodic I-V characteristics of n-type silicon in a 35% HF solution and with different substrate doping concentration [16].

For n-type silicon (Figure 3.7), PS formation is very slow for doping lower than 10^{19}cm^{-3} .

Due to the effect of doping level on PS formation, selective formation of porous silicon is possible.

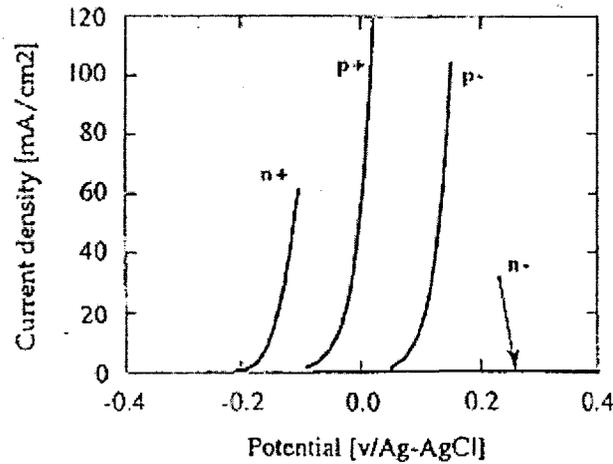


Figure3.8 (adapted from L.Canham) Comparison of the anodic current-voltage characteristics obtained from p- and n-type silicon in a 35% HF solution using substrates of different doping levels [16].

It can be seen that the J-V curves of any type of silicon wafers are shifted to the right in the following order:

$$n^+ > p^+ > p^- > n^-$$

meaning that n^+ can be preferentially anodized over p^+ , p^- and n^- , and p^+ can be preferentially anodized over p^- and n^- , and so on [16].

Chemical Composition Effects: As per the dissolution mechanism of silicon mentioned before, it is known that during the formation of porous silicon, hydrogen bubbles are formed and

they come to the surface and cause a non-uniform PS layer and lateral and in-depth inhomogeneity. This non-uniformity happens if the solution contains only HF acid. To avoid this problem and to have a PS layer with better crystalline structures, an additive needs to be introduced into the solution that the most used one is ethanol. In the presence of ethanol, the size of the hydrogen bubbles decreases and their removal from the surface is much easier and the penetration of the electrolyte solution in the pores is much better. Another additive that is used for the removal of hydrogen bubbles is acetic acid that improves the control of solution PH. Only a few percent of acetic acid (around 5%) is enough for hydrogen removal [39, 16]. In addition, the concentration of hydrofluoric acid in the electrolyte has a strong effect on the porosity and the surface morphology of the PS. Increasing the HF concentration in the electrolyte leads to a decreasing of PS layer porosity [16].

3.2. Characterization Equipments

SEM, AFM and Raman Spectroscopy were used for characterizations of the fabricated samples. This section introduces the working mechanism of these equipments.

3.2.1. Scanning Electron Microscope (SEM)

SEM was used to study the morphology of the fabricated PS structures.

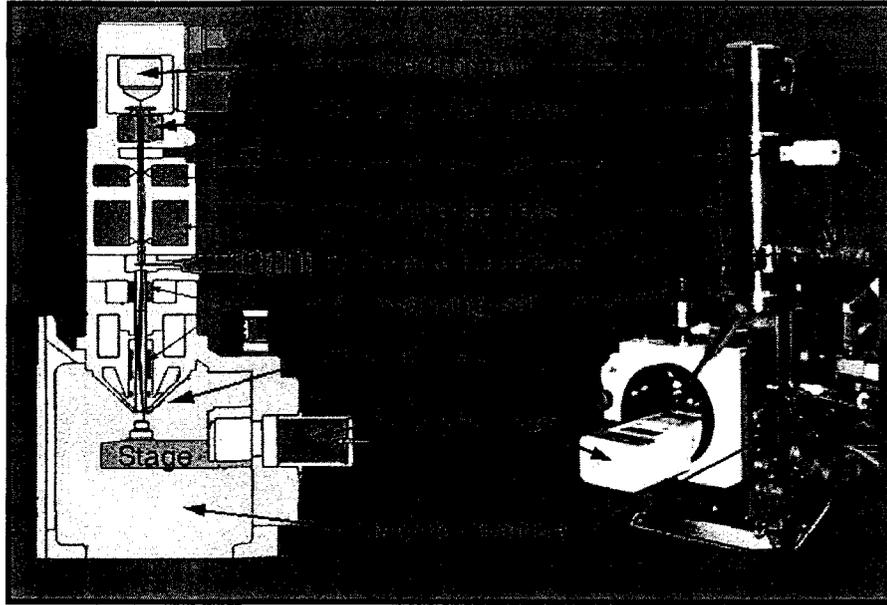


Figure 3.9 Schematic view of a typical SEM [40].

SEM is a type of microscope that uses the high beam energy of electrons to scan the surface of the samples. As per interactions between electrons and the atoms that make up the sample, some signals being produced containing information about topography, morphology, composition and some properties of the samples. With SEM, one can obtain high-resolution images, which means that closely spaced features can be examined at a high magnification. All of the above plus large depth of focus makes SEM the most used instrument in many research areas [40]. Table 3.3 is a comparison between SEM and other measurement techniques.

Table 3.3 Resolution comparison between eye and several other microscopy methods [41].

Technique	Limits	Resolution
Eye	Retina	700,000 Å°
Optical microscope	Diffraction of light	3000 Å°
Scanning electron microscope	Diffraction of electrons	30 Å°
Field ion microscope	Atomic size	3 Å°
Transmission electron microscope	Diffraction of electrons	1 Å°
Near-field scanning probe microscope	“Aperture” size	0.1-100 Å°

As it was mentioned earlier, SEM’s working mechanism is based on high beam energy of electrons generated in electron gun, Figure 3.10.

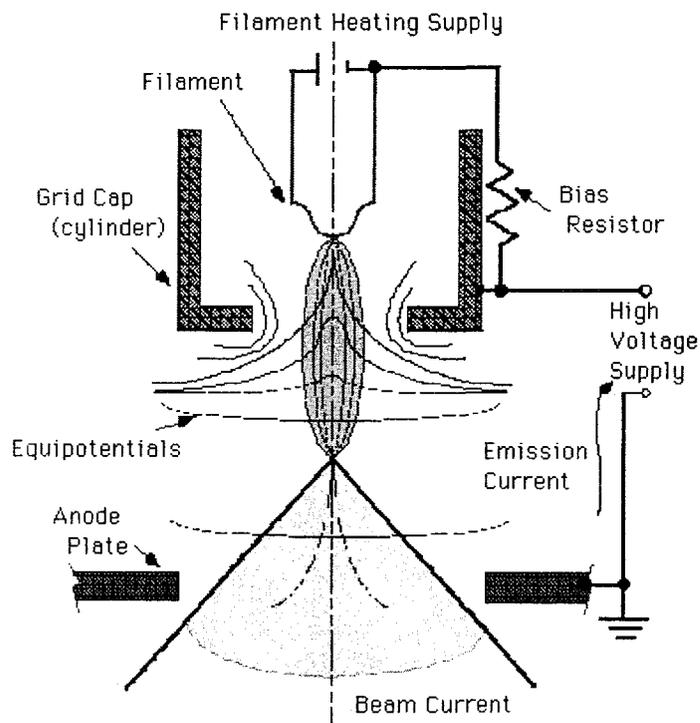


Figure 3.10 Schematic image of the source of electron in SEM [40].

A voltage is being applied to the filament, which is mostly tungsten (the cathode) and it cause the gun to release electrons. Electrons accelerate to an anode. The beam of these accelerated electrons will be condensed by a condenser lens and focused as a very fine point on the surface or the sample by an objective lens. Then the beam will be deflected back and forth by a magnetic field produced by scan coils either linearly or in a raster fashion and that covers a whole rectangular area of the specimen. This electron beam that hits the sample has an energy ranging from few Kev to 50 Kev. The impinging electrons lose their energy on the specimen and pass it on to the other atomic electrons or to the lattice. So a group of electrons will be excited and will leave the specimen. They are called secondary electrons. The detection of these secondary low energy electrons is the most common imaging mode of an SEM. This signal is detected by a combined scintillator photomultiplier detector [42].

The SEM model that was used in this research is S-4700 as shown in Figure 3.11.

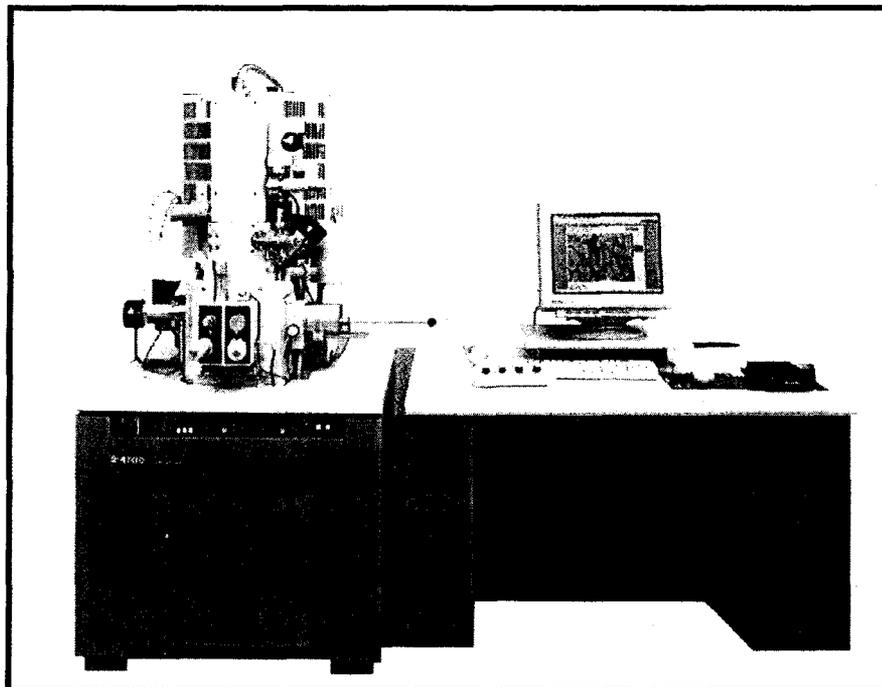


Figure3.11 Hitachi SEM model S-4700 [43].

For SEM, specimen should be prepared as following [43]:

-To avoid polluting the vacuum with hand oils or other particles, clean gloves should be used while carrying the specimen and inserting it into the chamber.

-To fix a specimen on the stub, double-side adhesive tape is used, but it should be considered that to use a small size of tape to minimize the out-gassing.

-During preparation, specimen material type should be considered. For different types of specimen such as conductive (metals), non-conductive (semiconductors) or biological specimens different preparation methods are required.

-No pulverized ferromagnetic specimen is allowed to be inserted into the chamber as these kinds of materials may cause the degradation of microscope performance due to their strong magnetic field.

After these steps, specimen stub is inserted on the specimen holder and it should be adjusted to the proper height using the specimen height gauge.

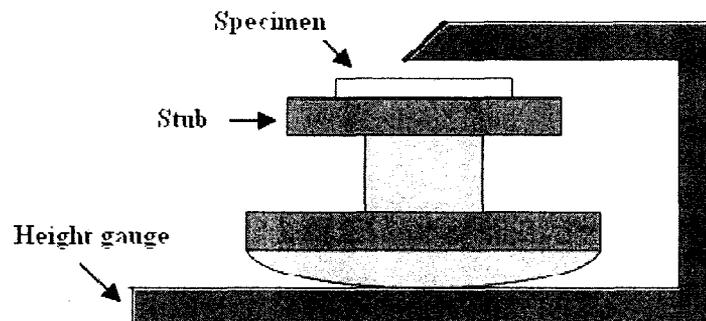


Figure 3.12 Specimen height adjustments.

The specimen height must be at least 0.5mm lower than the bottom of the height gauge; otherwise it may hit the objective lens and damage it when the work is done at a short distance or at a high tilt angle [43].

3.2.2. Atomic Force Microscope (AFM)

AFM was used to study the topology of fabricated PS samples. Figure 3.13 shows the principal components of AFM including the cantilever.

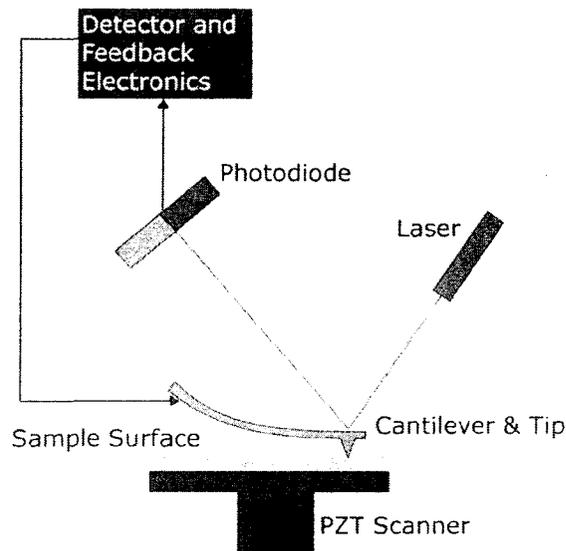


Figure3.13 Schematic diagram of AFM [44].

AFM is a type of scanning probe microscope with a very high resolution that is one of the most employed imaging and measuring instruments at nanoscale. AFM scans the surface of the sample by a microscale cantilever usually made of silicon or silicon nitride that has a sharp tip with a radius of the order of nanometers. AFM measures different forces between its probe and the surface of the samples depending on the situation, such as mechanical forces, Van der Waals

forces, capillary forces, chemical bonding, electrostatic forces, and magnetic forces. These forces are not being measured directly but by cantilever deflection calculations. While the cantilever with its sharp tip is scanning the surface of the sample, as it is shown in Figure 3.13, a laser beam is reflecting off from the back of the cantilever and they are collected by a position-sensitive detector (PSD) consisting of 2 photodiodes that at a time, one of them receive more light than the other from the movement of cantilever up and down and a signal is being generated that helps PSD to discover the movement of cantilever. While the tip is scanning the surface of the sample, if the distance between the tip and sample remains constant, may cause a confliction between the tip and the surface of the sample and lead to damaging either of them. Therefore a feedback system is designed to adjust the distance between tip and sample in order to keep a constant force between them [44].

Depending on the application, AFM can operate in different modes; the most important ones are contact mode, tapping mode and non-contact mode.

Contact Mode

In this mode the cantilever tip scans across the sample surface and a split photodiode detector monitors the changes in cantilever deflection. There is an adsorbed fluid layer in the surface of the sample and the tip contacts the surface through that layer. A feedback system moves the scanner vertically at each X and Y direction to keep a set-point deflection in order to maintain a constant force between cantilever and the sample. The distance obtained by the movement of the scanner in X and Y directions are recorded by a computer to obtain the topographic image of the sample. The advantage of this mode is the fast scanning process and possibility of obtaining “atomic resolution” images [45].

Tapping Mode

In this mode, the cantilever oscillates and the tip at the end of this oscillating cantilever contacts with the sample by tapping its surface during the scanning. The feedback system keeps oscillation amplitude constant. The vertical position of the scanner is recorded by a computer and a topographic image of the sample will be formed. This mode can be used in liquid or ambient environment [45]. This mode is mostly recommended for soft and delicate samples as the contact mode can damage or deform the surface of these types of samples [46].

Non-contact Mode

Cantilever oscillates at a frequency slightly above its resonance frequency to obtain an AC signal. In this mode, there is no contact between the tip and the sample surface, instead, during the scanning the tip oscillates above the adsorbed fluid layer on the surface. The scanner moves vertically at each (x, y) data point above the sample until it reaches the amplitude or frequency target value. The feedback loop controls this process to obtain a constant oscillation amplitude or frequency. To have a topographic image of the sample, a computer records the distance between scanner and the surface at each (x, y) data point. The advantage is that no force is applied to the sample [45].

The AFM used during this research is Multi Mode AFM model AFM-2.

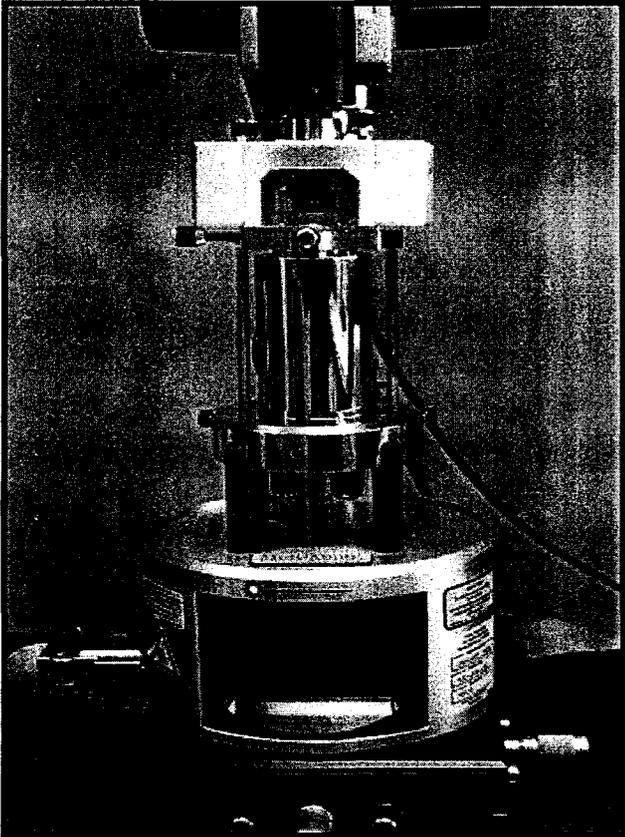


Figure3.14 Multi Mode AFM, model AFM2 with AS-130 (J) Scanner.

Table 3.4 shows the specification of AFM used for our research.

Table 3.4 Specifications of the Tapping mode etched silicon probe (TESP).

Model of AFM Tip	TESP
Tip Material	0.01-0.025Ohm-cm Antimony (n) doped Si
Cantilever Specification	Thickness: 3.5-4.5μm, Length:110-140μm, Width: 25-35 μm
Resonant Frequency	$f_0 = 313-346$ KHz
Spring Constant	$K = 20-80$ N/m

3.2.3. Raman Spectroscopy

Raman spectroscopy is used as one of the characterization techniques. The study of the interaction between radiation and matter as a function of wavelength, frequency or energy is called spectroscopy. There are different types of spectroscopy such as: Absorption, Fluorescence, X-ray, Flame, Visible, and Ultra violet, Infrared, Raman and Nuclear magnetic resonance [47]. When light is scattered from a molecule, photons scatter in two different ways, most of them scatter elastically which means the energy of scattered photon is equal to the energy of incident photons, but a small part of the photons scatter at energy lower than the energy of incident photons called inelastic scattering known as Raman Effect. Raman spectroscopy is a light scattering technique. In its simplest form is a process where a photon interacts with a sample to produce scattered radiation of different wavelengths [48].

Raman spectroscopy is a spectroscopic technique used in condensed matter physics and chemistry to study vibrational, rotational and other low-frequency modes in a system and relies on inelastic scattering or Raman scattering of monochromatic light, usually from a laser in the visible, near infrared or near violet range. The laser light interacts with phonons and as a result the energy of the laser photons are shifted up or down. The shift in energy gives information about phonon modes in the system. The resulting fingerprints are an aid to analysis of different matters [47].

Raman Effect happens when light impinges upon a molecule and interacts with the electron clouds of the bonds of that molecule. The molecule will be excited from the ground state to a virtual energy state by the incident photon and relax into a vibrational excited state. Two series of lines exist around this central vibrational transition, called Stokes lines and Anti-Stokes lines that correspond to the complimentary rotational transition. Stokes lines correspond to rotational excitation when molecule absorbs energy generating Stokes scattering and Anti-Stokes lines

correspond to rotational relaxation that is when molecule loses energy generating Anti-Stokes scattering. In order to have Raman Effect, a change in molecular polarization potential or amount of deformation of the electron cloud with respect to the vibrational coordinate is required. The polarizability change will determine the Raman scattering intensity, whereas the Raman shift is equal to the vibrational level that is involved. [47]

Figure 3.15 shows the energy band diagram of Raman scattering (Stoke and Anti-stoke scattering) and Rayleigh scattering.

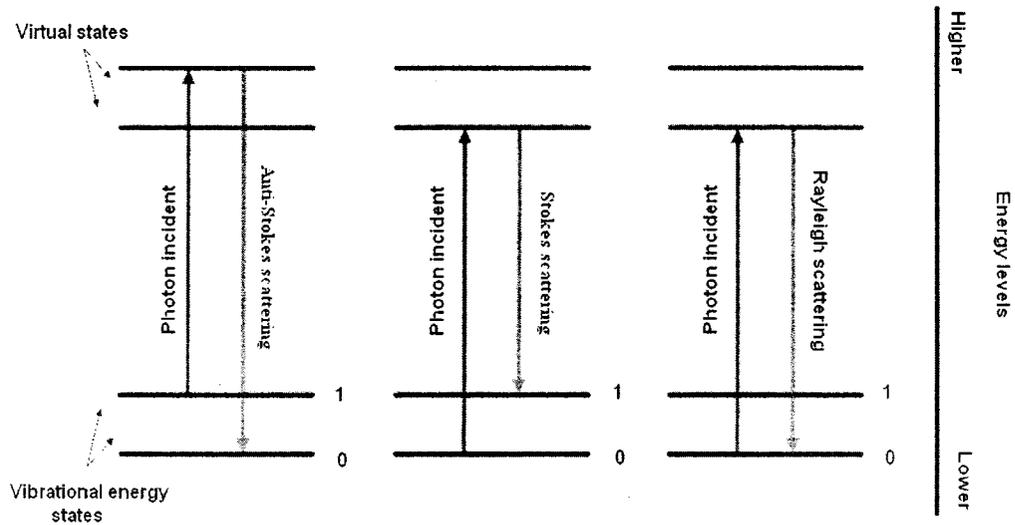


Figure 3.15 Energy band diagrams of Raman scattering and Rayleigh scattering [47].

The energy difference between the scattered photons and incident photons is showed by the arrows of different length in Figure 3.15. By equation 3.6 the energy difference between the initial and final vibrational levels can be calculated, knowing the value of $\lambda_{\text{incident}}$, the incident photon wavelength and $\lambda_{\text{scattered}}$, the scattered photon wavelength.

$$\bar{\nu} = \frac{1}{\lambda_{incident}} - \frac{1}{\lambda_{scattered}} \quad (3.6)$$

Several variations of Raman spectroscopy exist such as Surface Enhanced Raman to enhance the sensitivity, Resonance Raman to acquire very specific information and Raman microscopy to improve the spatial resolution.

In this research Surface Enhanced Raman Spectroscopy known as SERS is used for measurements. This mode is normally done on a silver or gold colloid or a substrate containing silver or gold. Surface plasmons of silver and gold are excited by the laser, resulting in an increase in the electric field surrounding the metal. Raman spectroscopy does not usually require any sample preparation. The spatial resolution and the depth of field are the advantageous features for the analysis of thinner, smaller dimensional scale devices. Also this is a non-destructive method as there is no contact with the sample [48].

In this work, a LabRAM HR (high resolution) with a Raman-IR micro analysis spectrometer was used for recording the Raman spectra. This equipment contained a holographic notch filter (Kaiser optical system, Model: Super Notch Plus), a 17 nW He-Ne laser emitting at 632.8nm, a 256x1024 pixel CCD detector, a computer-controlled XY stage with a spatial resolution of 0.1 μ m, two interchangeable gratings (950 and 1800 mm⁻¹, respectively), a confocal microscope with 10, 50, 100x objectives with a lateral spatial resolution of approximately 10, 2, and 1 μ m, respectively.

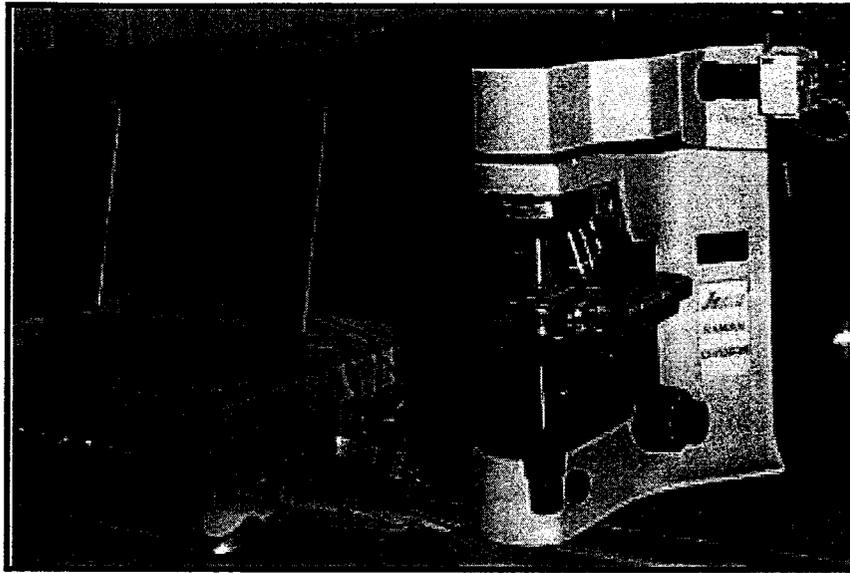


Figure 3.16 LabRAM HR spectrometry.

Chapter 4

Experimental Results and Discussions

Porous silicon fabricated with different anodization conditions and the obtained novel structures are discussed in this chapter.

4.1 Porous Silicon Morphology Fabricated on Flat Surfaces of Silicon

Different PS samples fabricated by electrochemical etching on smooth surface of silicon are shown in Figure 4.1. Each sample was prepared under different anodization condition. As it was mentioned in section 3.1.4, page 27-31, any change in anodization parameters such as current density, etching time, HF concentration, doping level causes a big difference in fabricated PS in terms of porosity, thickness, pore's diameter and other properties.

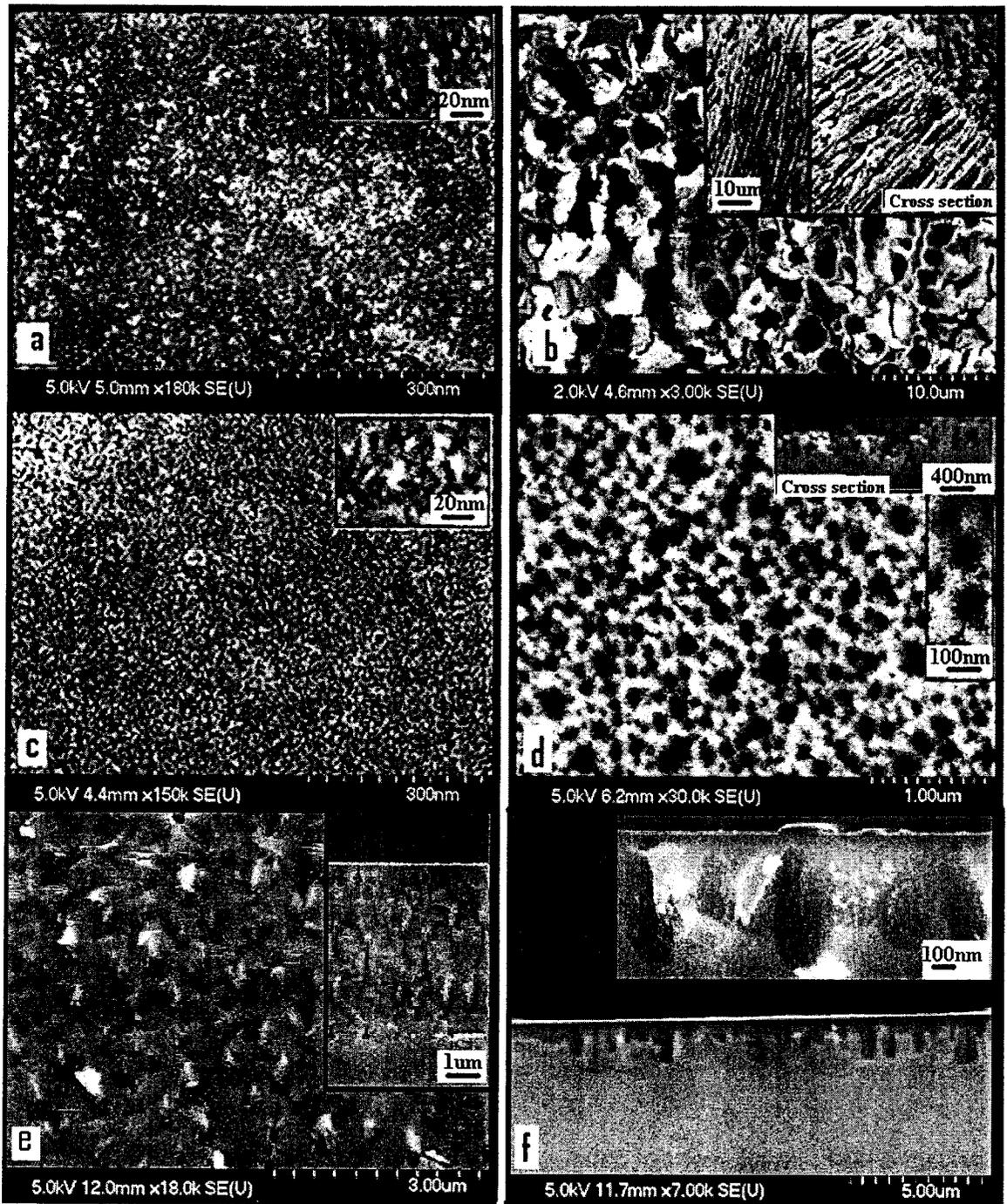


Figure 4.1 Some of the porous silicon structures produced under various fabrication parameters.

Figure 4.1-a represents the topology of a PS (sample#1) made of p-type, boron doped silicon along $\langle 100 \rangle$ directions with resistivity of $10\text{-}20\Omega\text{cm}$. Constant anodization current of 2mA is

passed through the sample for 15 minutes. PS (sample#2) represented in Figure 4.1-b is made of p-type boron doped silicon with resistivity of 7-30 Ω cm. Anodization current for this sample was 30mA and etching time was 2 hours. Figure 4.1-c is a PS (sample#3) fabricated by anodization etching of the same silicon sample used for sample #1. Anodization current used for this experiment was 1mA which passed through the sample for 40 minutes. Figure 4.1-d is showing the topology and cross section image of a PS (sample#4) made of n-type silicon with resistivity of 0.01-0.02 Ω cm that a constant current of 70 mA passed through the sample for 2 minutes under light illumination (120v, 35w). Figure 4.1-e is a PS (Sample#5) made of the same silicon type, anodization current and illumination as sample #4 with etching time of 10 minutes. And finally Figure 4.1-f represents cross section of a PS (sample#6) made of the same silicon wafer as sample #4 using constant current of 2mA and etching time of 15minutes under illumination (120v, 35w).

HF: Ethanol concentration ratio for these experiments was 1:1 (as mentioned before ethanol was added to the electrolyte to ease the removal of hydrogen bubbles from the surface of the samples). Table 4.1 summarizes the parameters used to fabricate the samples shown in Figure 4.1 and obtained results.

Table 4.1 The obtained results for pore size and thickness using different anodization conditions.

Sample	Si type & resistivity	Anodization current	Time	Illumination	Pore diameter	Thickness
Sample#1 (Fig4.1-a)	p-type 10-20 Ω cm	2mA	15min	No	5-10nm	1 μ m
Sample#2 (Fig4.1-b)	p-type 7-30 Ω cm	30mA	2hr	No	1 μ m	50 μ m
Sample#3 (Fig4.1-c)	p-type 10-20 Ω cm	1mA	40min	No	5-10nm	5 μ m

Sample#4 (Fig4.1-d)	n-type 0.01-0.02 Ωcm	70mA	2min	Yes	200-400nm	400 nm
Sample#5 (Fig4.1-e)	n-type 0.01-0.02 Ωcm	70mA	10min	Yes	~200-400nm	5 μm
Sample#6 (Fig4.1-f)	n-type 0.01-0.02 Ωcm	2mA	15min	Yes	---	1.5-2 μm

As one can see, for sample#1, PS surface is fairly uniform with pores diameter of 5-10nm with inter-pore spaces of 5-15nm. Comparing it with sample#3, one can see that pores diameters for both samples are in the same range as the applied current densities on both samples was almost the same. However, studies on the thickness of their porous layers show that longer anodization time leads to thicker porous layer. Sample#2 is showing a larger pore diameter due to the larger current density comparing to the samples 1 &3. Also the long anodization period led to a very thick porous layer, about 50 μm . Comparing samples #4 and #5, we can see the effect of etching time on the thickness of porous silicon as sample #5 has a thicker porous layer due to longer anodization period.

In addition to the PS samples presented in Figure 4.1(a, b, and c), we have studied the formation of PS layers on a large number of high and low-doped p-type silicon wafers using low current densities and/or short etching times. For those fabricated with low current densities and short etching time, the structure was not observable by SEM facility, therefore there is no image presented here. Experimentally we have observed that porous silicon fabricated by either low current densities (constant current of 1-7mA) or short etching times (few second to 5minutes) have visible photoluminescence observable by naked eye that makes them suitable for many optical and photonic devices such as light emitting diodes.

Beside the above discussion, it should be mentioned that porous silicon has been used numerously for solar cell applications. In order to use PS in solar devices, the fabrication process should be moved toward formation of PS layer with lower refractive indices (closer to air) and the proper morphology to trap the light. Very high porosity porous silicon layers (obtainable by increasing the anodization current) have a very low refractive index making it an ideal material for anti-reflection coatings used in solar cells. But when it comes to high porosity porous silicon fabrication, capillary stress and crack defects should be taken into the account.

4.2. Drying Techniques and Induced Defects during the Process

During the fabrication process of PS, drying of the samples after etching is a crucial step, especially for the samples with high porosity. Drying samples with high porous or thick PS after DI water rinsing leads to some cracks over the layers. This is due to the capillary stress caused during the evaporation of electrolyte or water out of the pores. Further, the cracking pattern also happens due to the heat energy existed during the fabrication process. These two factors together cause the body tension stress and when the stress is released from the top of the PS layer, it creates the cracks at the surface. During the solvent evaporation from the pores a gas/liquid interface is created within the pores and a drop in pressure Δp happens at this interface. This pressure drop can be calculated by the following equation:

$$\Delta p = \gamma_l \frac{S \cdot \cos \Theta}{P_{\%}} \quad (4.1)$$

where γ_l is the liquid surface tension, S is surface area, $\cos \Theta$ is the curvature of the gas liquid interface, and $P_{\%}$ is the porosity [49].

In our experiments cracks appeared on top of some layers for samples with high porosity during the evaporation of the solvent. This pattern was observed more for the samples that were illuminated with light during the fabrication. Figure 4.2 and 4.3 show typical images of cracked samples on p-type and n-type silicon. In some cases the cracked causes that a layer of PS to lift up from the surface. Figure 4.4 shows surface of a sample with cracks separated from the PS layer.

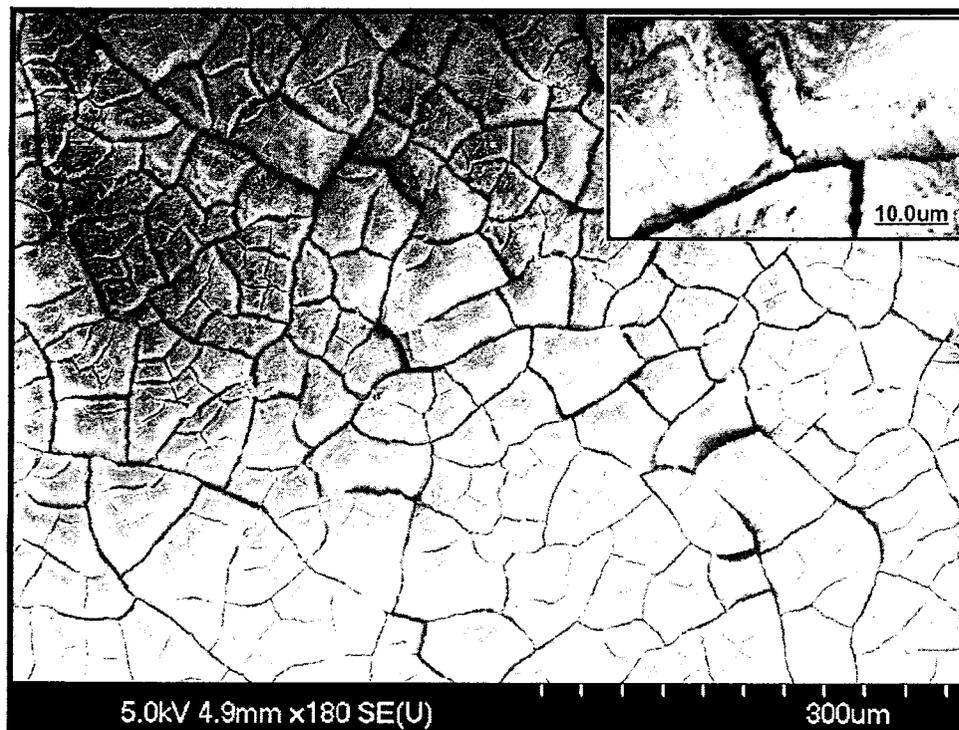


Figure 4.2 SEM image of a cracked p-type sample.

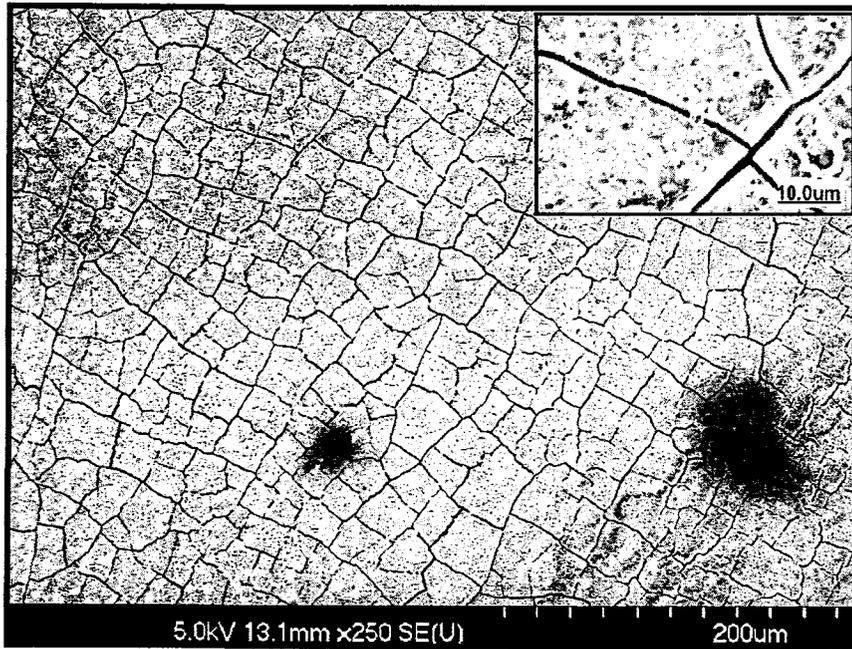


Figure 4.3 SEM image of a cracked n-type sample.

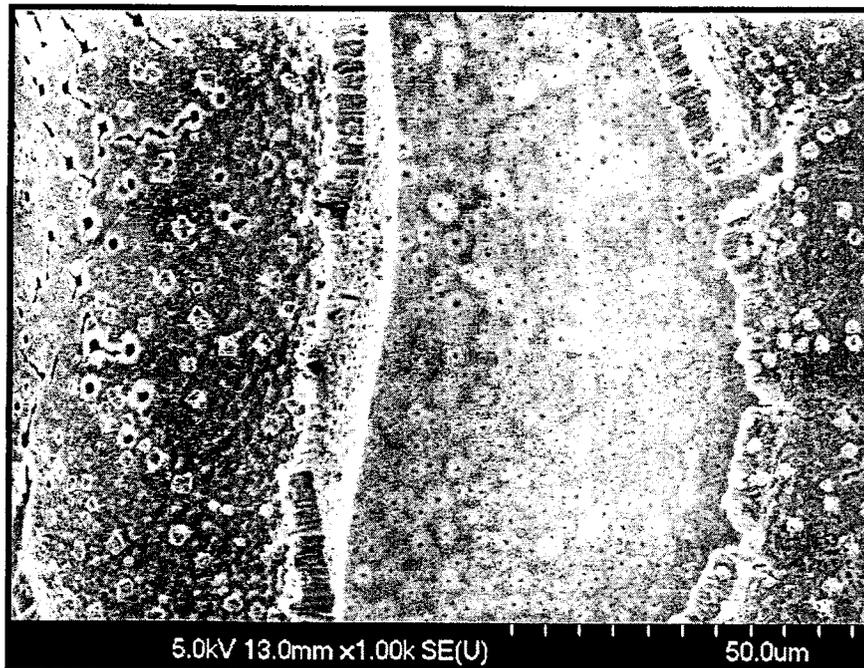


Figure 4.4 Image of the surface of PS under the cracks.

To avoid cracking problems several drying methods were suggested by many researchers as follow:

Supercritical Drying: this is the most efficient drying method. This technique takes advantage of liquid-gas critical point theory denoting that above this point no individual liquid and gas phase exist; therefore no liquid-gas interface means capillary stresses are restrained. In this method electrolyte from the pores is replaced by another liquid (mostly carbon dioxide with critical point of 304.1K and 7.36MPa). Then Carbon dioxide is compressed and heated above its critical point and then it should be vaporized through pressure reduction at a constant temperature [50]. In Figure 4.5, (SD) shows the supercritical drying phase diagram.

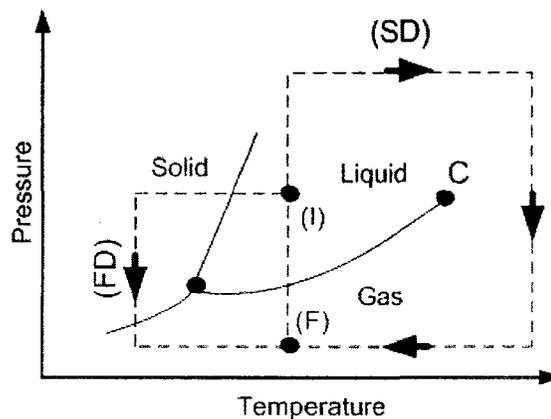


Figure 4.5 (adapted from D. Belletti et al) Supercritical and freeze drying phase diagram. (SD) represents the supercritical drying path, (FD) represents freeze drying path, (I) and (F) are initial and final points respectively [50].

With this method, a porous layer with porosity above 95% can be obtained; however this technique is not very cost effective.

Freeze Drying is another technique for reduction of capillary stress by avoiding the liquid/vapor interface. In this method the solution inside the pore is first frozen and then it is lifted under vacuum to avoid surface tension. In Figure 4.5, (FD) shows the freeze drying path.

The PS layer obtained by this drying technique has better structural and optical characteristics compared to the samples that are dried in air [50].

Pentane Drying is the easiest and most affordable method. Pentane has a very low surface tension compared to water (14 mJ/m^2 for pentane compare to 72 mJ/m^2 for water). It doesn't interact chemically with PS layer and it reduces the capillary stress. With this method, PS layer up to 90% porosity were obtained [16].

We used this method to dry our samples during this project.

In order to eliminate or reduce the cracking defects on our samples, pentane (98%) was used. At the end of the etching time, the samples were rinsed with pentane instead of DI water and left to dry in air. With this method we managed to fabricate high porosity p-type silicon. For n-type samples the method was only effective for low porosity layers. For samples with high porosity, cracks in form of a yellowish layer of nanocrystalline silicon appeared on the surface of the samples. This layer in fact is a form of porous silicon that has amorphous structure with small grain of crystalline silicon.

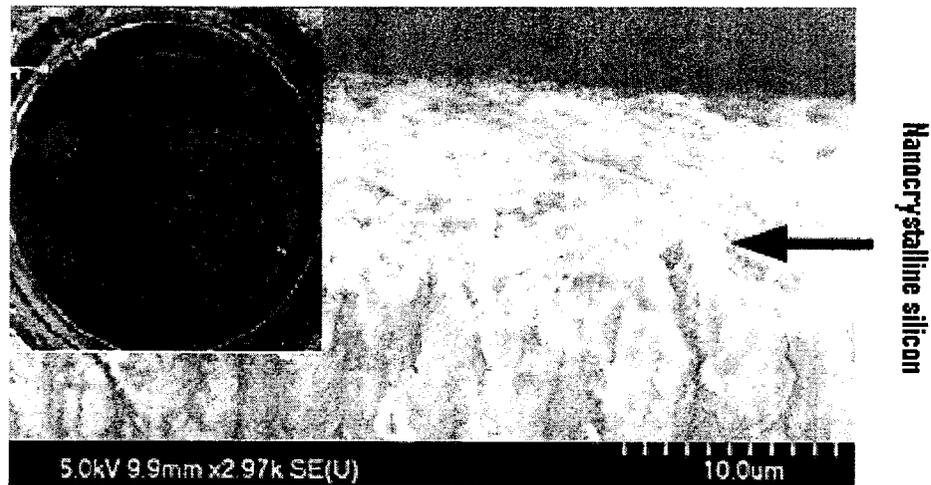


Figure 4.6 Image of nanocrystalline silicon

For high porosity n-type samples, we immersed the samples in NaOH at room temperature for some time until the yellow layers are dissolved completely. For these experiments, a 0.2molar NaOH solution was used (after pentane drying of the samples) for period of time between 5 to 25 minutes. Figure 4.7 shows porous silicon made of n-type silicon with resistivity of 0.01-0.02 Ω cm, anodized for 50 minute and a constant current of 35mA before immersion in NaOH.

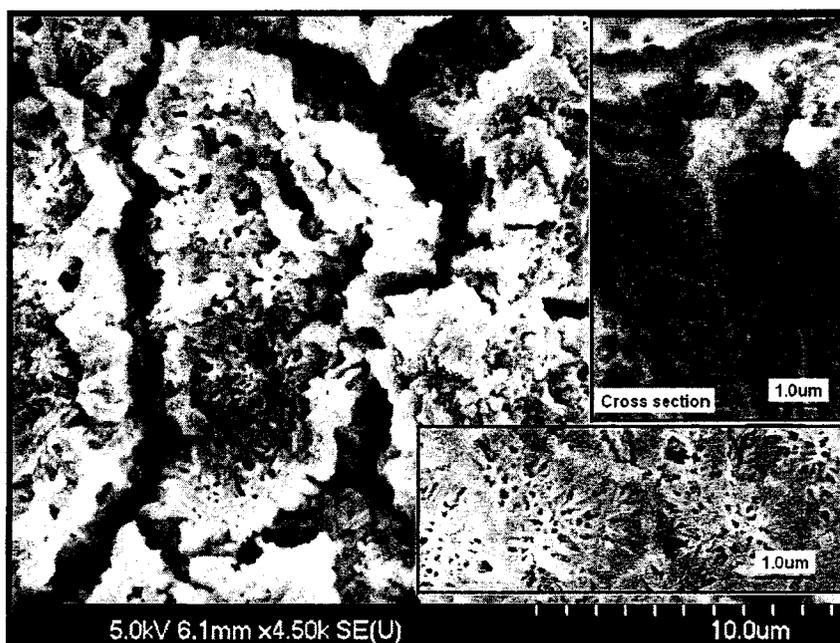


Figure 4.7 PS made of n-type silicon, $I=35\text{mA}$, $t= 50\text{min}$, with cracked surface.

After inserting the sample into NaOH, the cracked nanocrystalline surface will be removed. Figure 4.8 represents the same PS sample as Figure 4.7 after immersion in NaOH for 5 minutes.

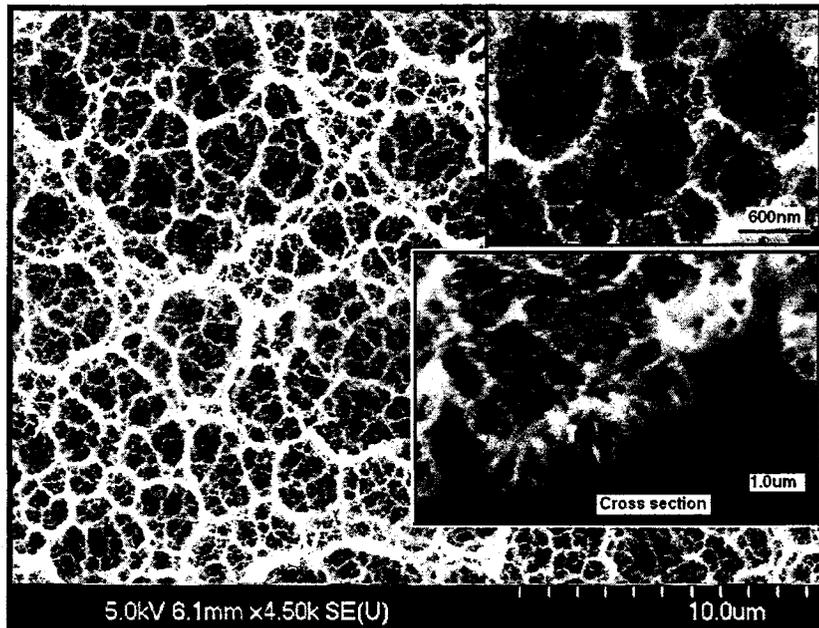


Figure 4.8 PS made of n-type silicon, $I=35\text{mA}$, $t= 50\text{min}$, after immersion in NaOH for 5 minutes.

The structure presented in Figure 4.8 is suitable for biosensors due to its very large surface to volume ratio. As it is shown in the figure, the main structure contains macropores which each again porosified to produce nanopores. This leads to multiplication of the surface area of porous structure.

4.3. Porous Silicon Fabricated on the Textured Surface of Silicon

Pyramidal PS structures were fabricated using the textured silicon wafers. By texturing the surface of silicon, the location of pores will be predefined, as the defects on the surface act as seeding points for pore formation. The following steps and images illustrate the formation process. The surface of silicon samples were texturized by TMAH (25%wt) etching as it was explained before. Then PS samples were fabricated on these surfaces using high doped n-type silicon with resistivity of $0.01\text{-}0.02 \Omega\text{cm}$ (we were able to produce hillocks only on n-type Si). Different anodization conditions were applied. Figure 4.9 shows the PS layer fabricated by

electrochemical etching of silicon under white illumination (35w, 120v) and a constant current of 85mA for 30 minutes.

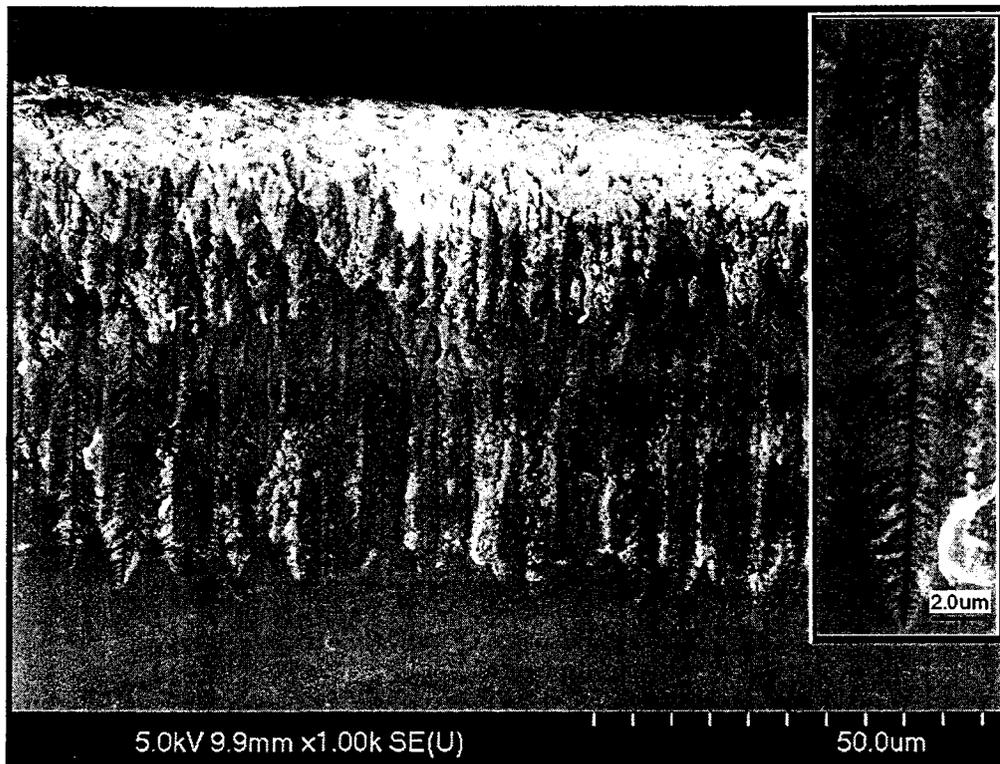


Figure 4.9 Cross section of a PS made of n-type textured silicon, $I=85\text{mA}$, $t=30\text{min}$.

This fabricated PS layer is $50\mu\text{m}$ thick and pores are $2\text{-}5\mu\text{m}$ apart. As it is shown in the Figure 4.9, there are some non-uniformity and defects on the surface of porous silicon. To remove them, the samples were immersed in NaOH. What is left is a uniform square shape of macropores with pyramidal wall structures. Figure 4.10 shows morphology of the top view of the sample after keeping it in NaOH for 21 minute.

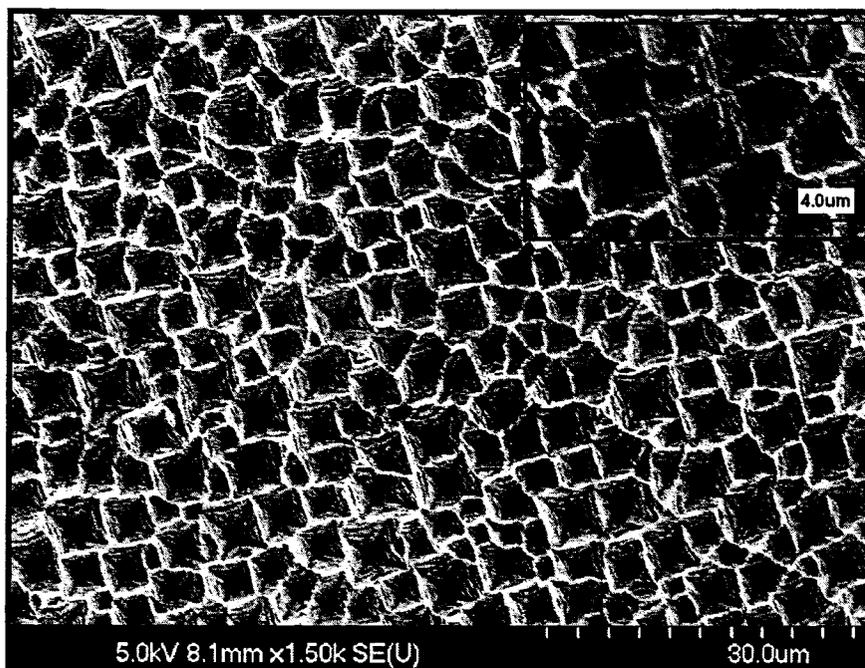


Figure: 4.10 Top surface of n-type PS after immersing in NaOH for 21 minutes- Sample #7.

The yellowish (nanocrystalline PS) layer formed on top of the surface was removed slowly and the sample was rinsed with pentane when the dissolution was finished. This process is easily observed by naked eye. The following figures represent the different view of the sample#7.

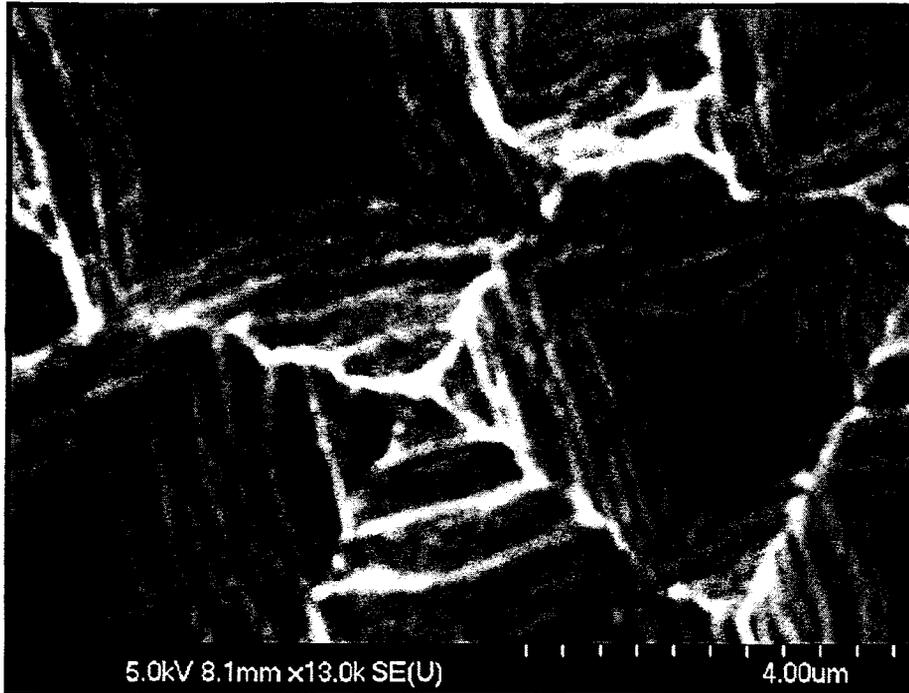


Figure 4.11 Image of a pore -sample#7.

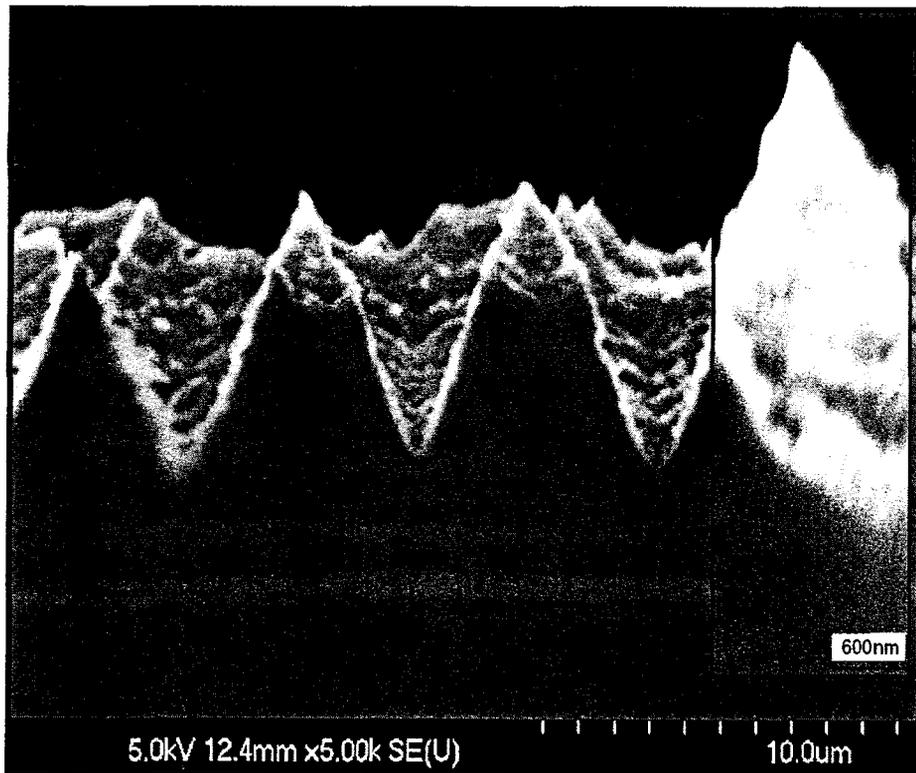


Figure 4.12 Cross section image of sample#7.

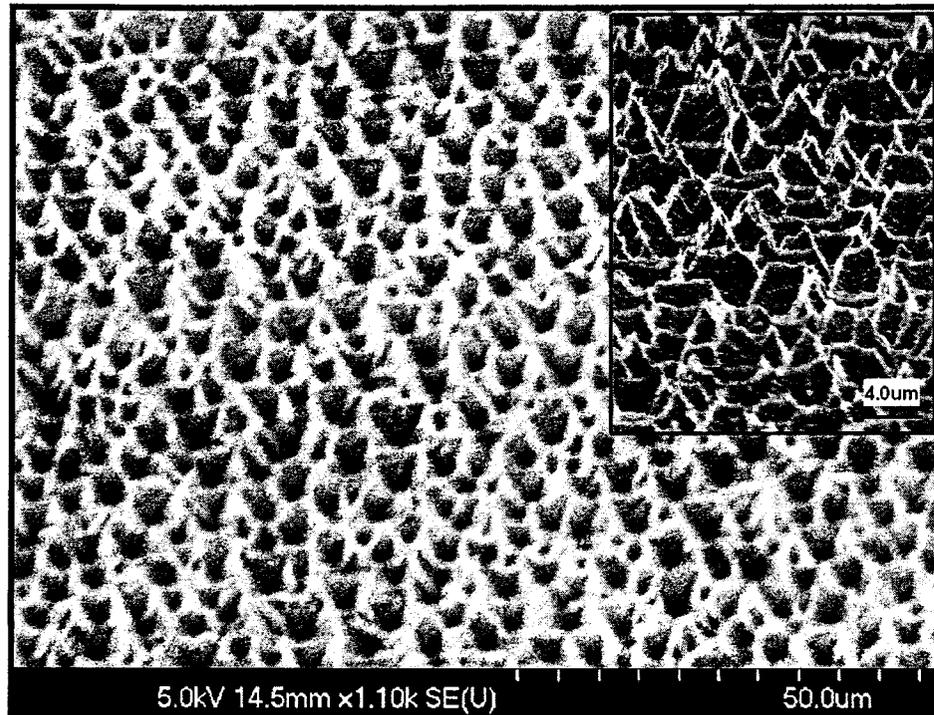


Figure 4.13 Titled view (45°) of sample#7.

Obtained pores diameters are between 2-4 μm with 8-10 μm thickness. The tips of the pores are around 20-30 nm. The pores are very well aligned and the surface is very uniform.

Fabricated porous structure was also studied by AFM. Figure 4.14 shows the AFM topology of n-type PS etched by a constant current of 85mA for 30 minutes. The images are taken in AFM contact mode. The size of the image is 20 μm x 20 μm . As it is shown in the image the pore diameters are about 4 μm . Figure 4.15 is the 3D image of a sample of n-type silicon with resistivity of 0.01-0.02 Ωcm etched in HF/Ethanol solution for 30 minute by a constant current of 85mA.

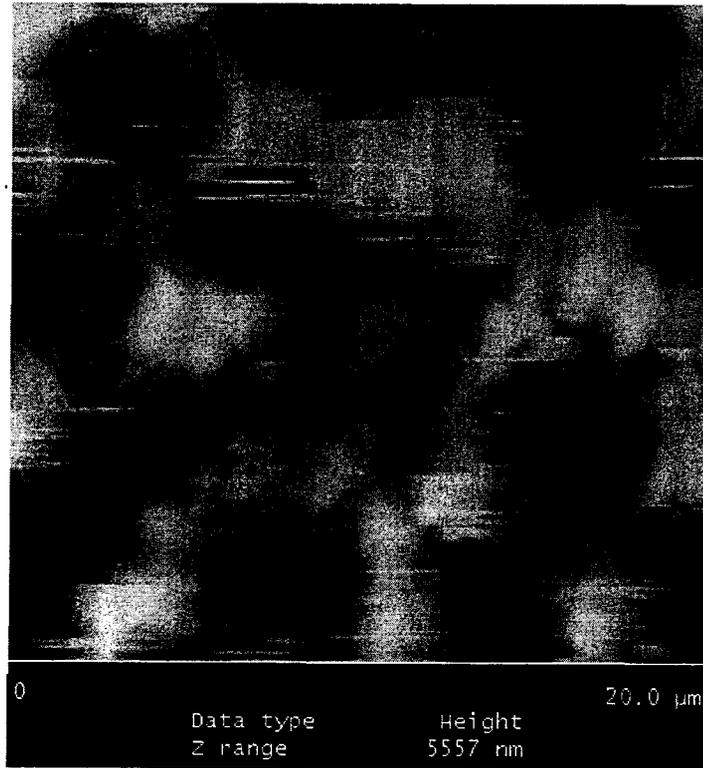


Figure 4.14 AFM image of PS structure fabricated on textured surface of Si by electrochemical etching followed by NaOH post-processing.

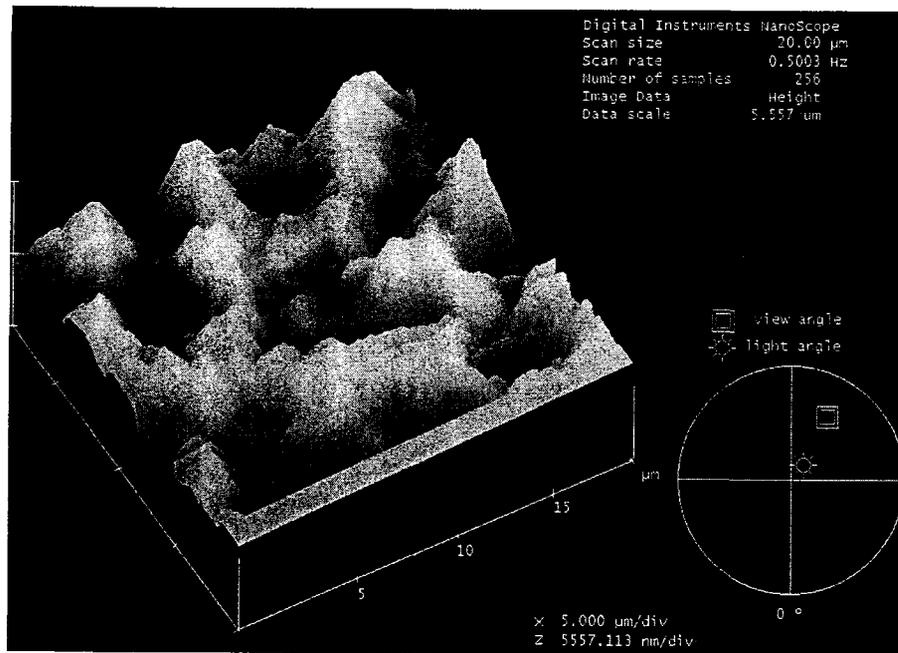


Figure 4.15 3D image of the PS structure fabricated on textured surface of Si by electrochemical etching followed by NaOH post-processing.

The Raman spectra of fabricated structure were also studied. Raman spectroscopy is widely used for characterization of silicon in both crystalline (c-Si) and amorphous (a-Si) forms. For crystalline Si, the measured Raman shift is 521cm^{-1} whereas for amorphous Si is 480cm^{-1} (The first order Raman scattering for crystalline silicon happens at the $q=0$ optical phonon in the center of Brillouin zone which its energy is about 521cm^{-1}) [51, 52]. Depending on the structure of porous silicon, its characteristics will be similar to either c-Si or a-Si. The measured Raman shift for the PS structure formed by electrochemical etching of textured n-type silicon (with resistivity of $0.01\text{-}0.02\Omega\text{cm}$) for 30minutes by constant current of 85mA is shown in Figure 4.16.

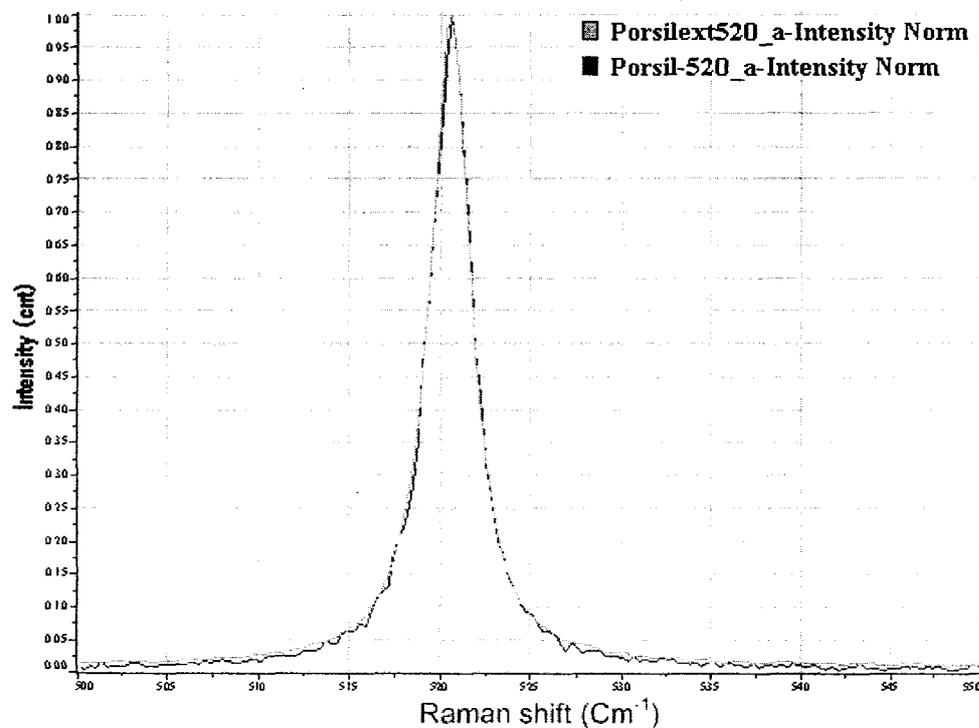


Figure 4.16 Raman spectra of TO mode of PS sample fabricated on n-type texturized silicon by anodization etching using constant current of 85mA for 30minutes followed by NaOH post processing.

The peak position is 520.6cm^{-1} which is close to Raman shift of crystalline silicon. This information reveals the crystalline structure of the fabricated PS.

In addition to the obtained structure of pyramidal porous silicon (sample #7), different anodization conditions were used for fabrication of PS on textured surface of silicon which lead to different PS structures. Figure 4.17 shows the PS structure fabricated on the textured surface of silicon (n-type, 0.01-0.02 Ωcm) passing a contact current of 85mA for 100 seconds.



Figure 4.17 PS obtained by electrochemically etching of n-type silicon with constant current of 85mA and anodization time of 100 seconds- tilted view (45°)-Sample#8.

No crack was observed on the top surface of this sample after pentane drying. Figure 4.18 shows the top view of the mentioned sample.

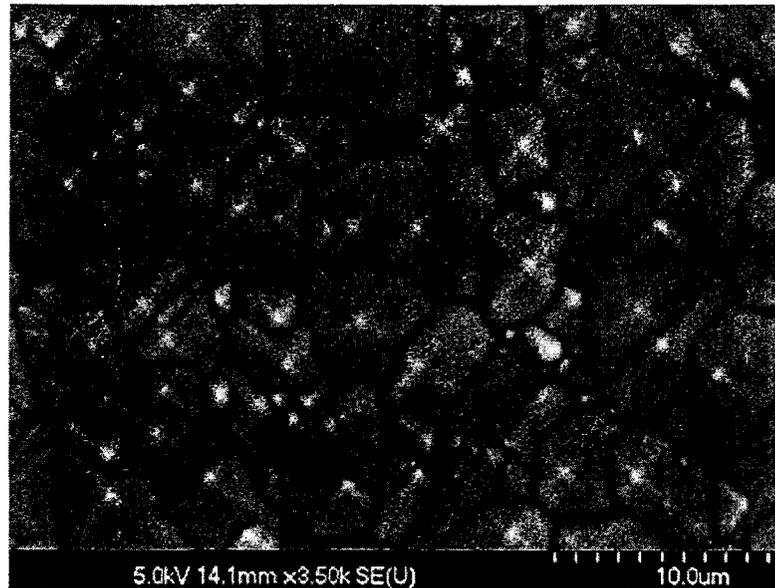


Figure 4.18 Top view of the sample#8.

Another structure obtained on the textured surface of silicon is shown in Figure 4.19. Textured n-type silicon (res 0.01-0.02 Ωcm) was electrochemically etched by a constant current of 50mA for 30 minutes- Sample#9.

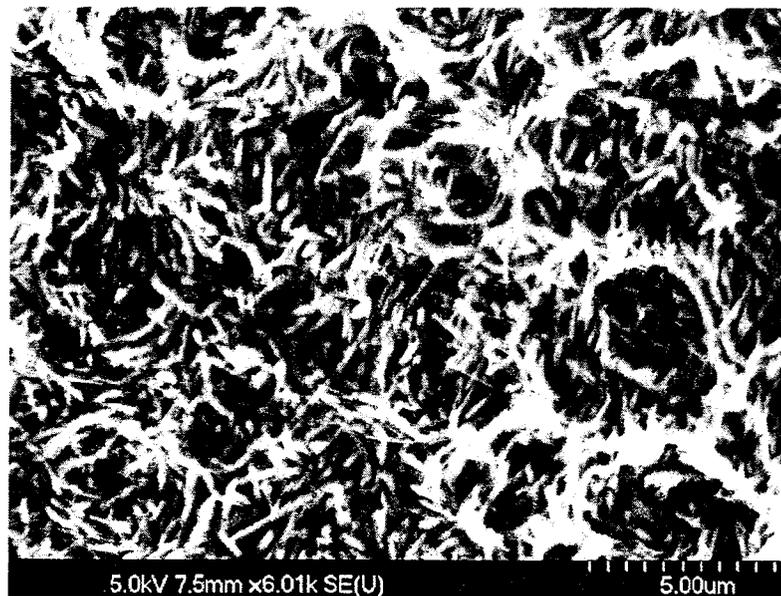


Figure 4.19 PS structure fabricated on textured surface of silicon using constant current of 50mA for 30 minutes and NaOH post processing for 20 minutes-sample#9.

Figure 4.20 shows the Raman shift of the discussed porous silicon.

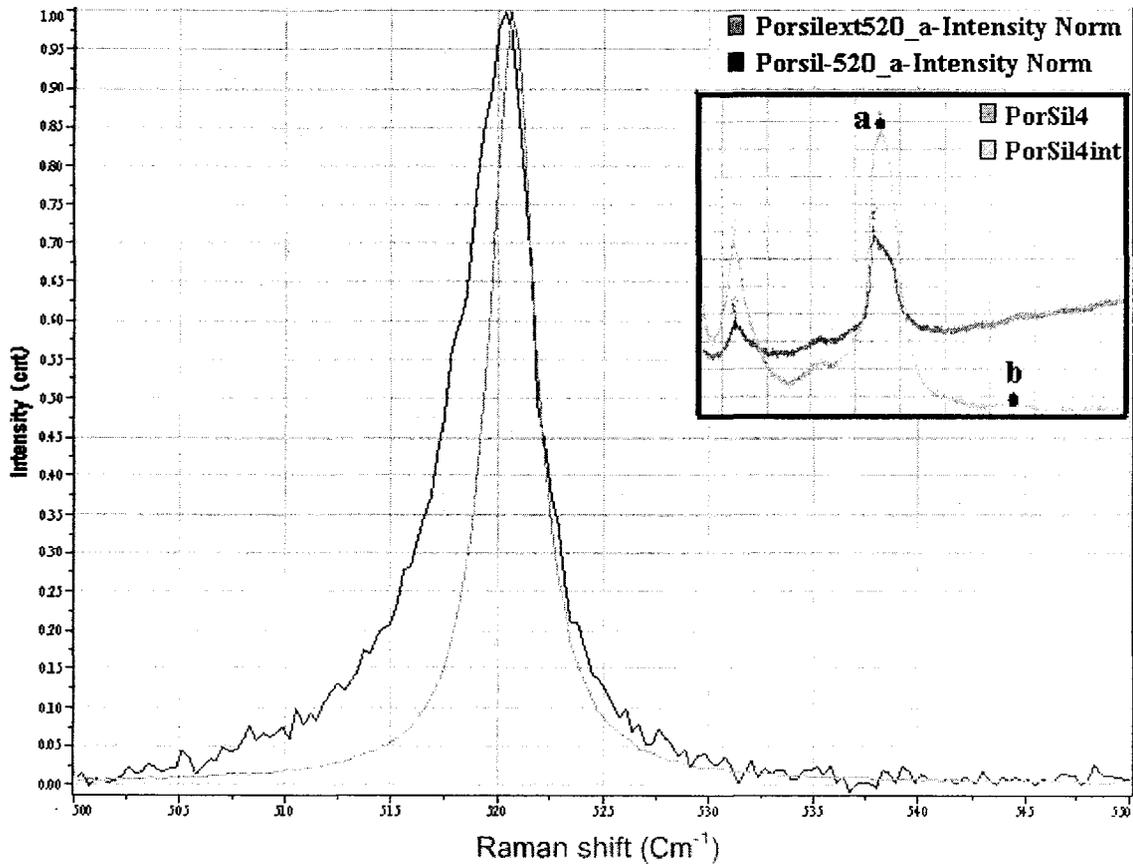


Figure 4.20 Raman spectra of TO mode of PS sample fabricated on n-type texturized silicon by anodization etching using constant current of 50mA for 30minutes-Sample#9.

The inset image of Figure 4.20 shows the Raman spectra of PS sample at two different points. The difference in the spectra at points (a= 950cm^{-1} and b= 1245cm^{-1}) is an evidence that the PS sample is non-homogeneous.

We have also investigated the effect of hillocks density on porous morphology. The density of hillocks on the surface of silicon is controllable by changing the TMAH concentration. Figure 4.21 is an image of a textured silicon surface that was etched in 10%wt TMAH. Comparing to the

silicon sample represented in Figure 3.2, the density of hillocks created in low-concentration TMAH is much higher than the ones created with the TMAH of higher concentration (All the other conditions are kept constant).

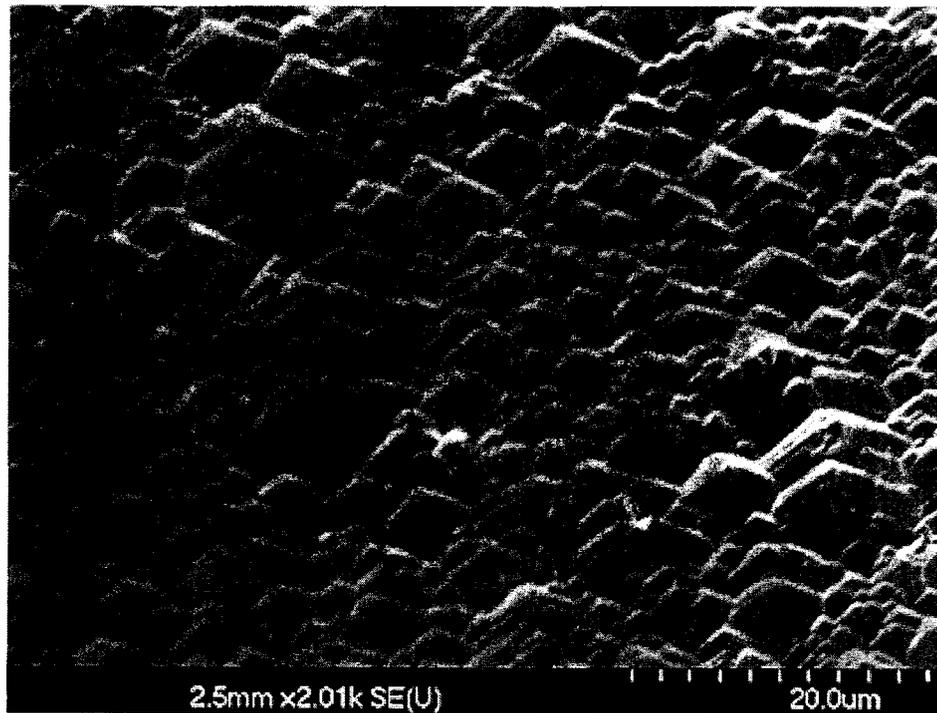


Figure 4.21 Textured surface of Si-(High density of hillocks using low concentration TMAH (10%wt)).

The textured surface of silicon was electrochemically etched using the same anodization condition as sample#7 (Constant current of 85mA and etching time of 30minutes). The obtained PS structure, Sample #10, is presented in Figures 4.22 to 4.25.

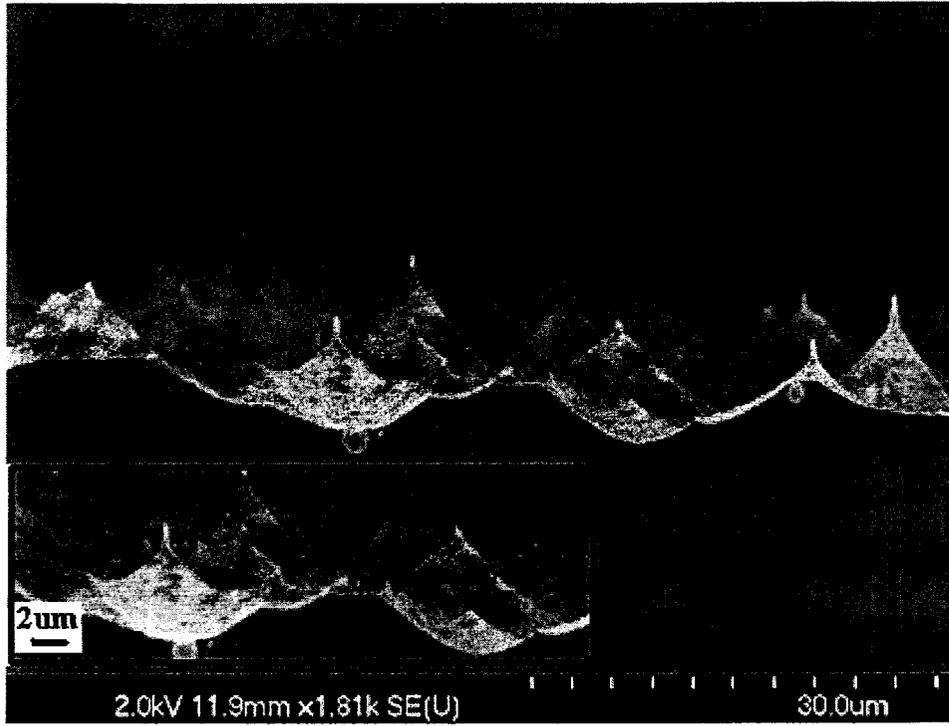


Figure 4.22 Cross section of pyramidal PS fabricated on Si surface of high-concentration hillocks-sample#10.

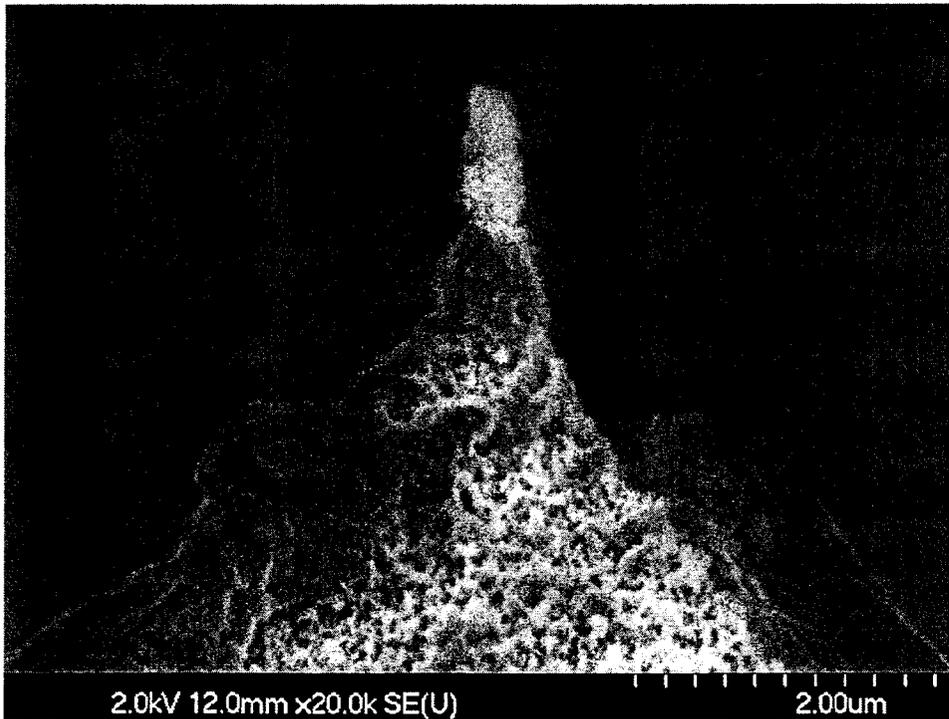


Figure 4.23 Cross section of one pyramid from sample#10- The image is representing a silicon nanorode.

As it is shown in Figure 4.23, in this experiment we have successfully fabricated silicon nanorodes on the tip of the pyramidal porous silicon structure with diameter of 200 nm and length of 800 nm. This structure is of potential interest for photovoltaic applications. The nanorodes with sharp tips can be also used as AFM probes.

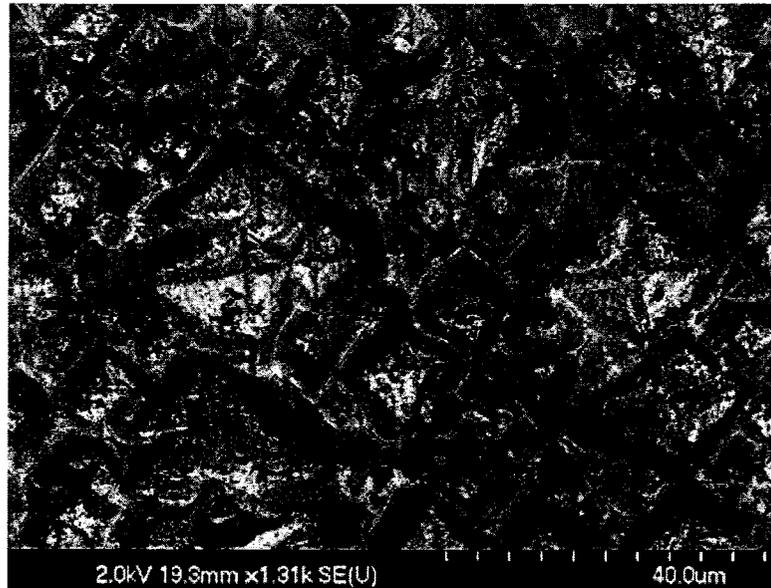


Figure 4.24 Top view of the fabricated PS-Sample #10.

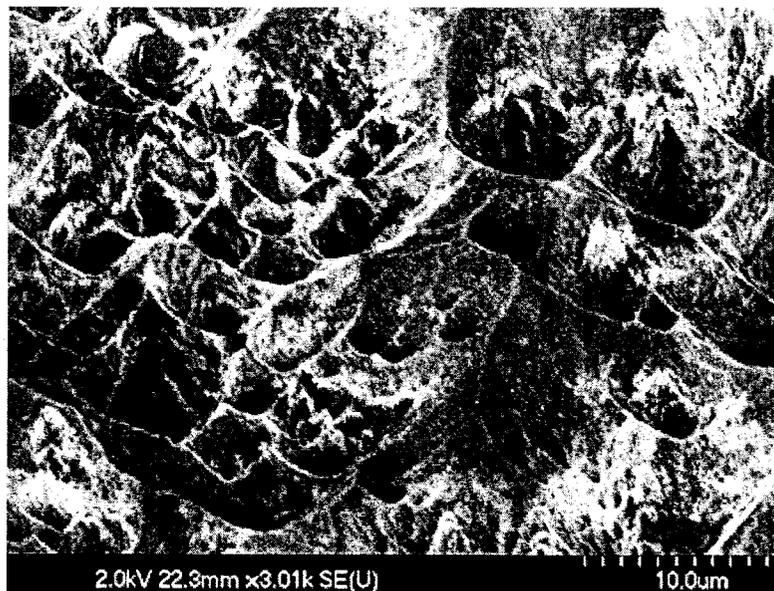


Figure 4.25 Tilted view of sample #10.

By looking at samples #7 (Figure 4.13) and #10 (Figure 4.25), one can see that the pores in sample #7 are more uniform with sharper structures compare to sample #10. This is due to the higher concentration of hillocks on the surface of sample #10 and demonstrates the effect of defect points on PS structures.

4.3.1. Porosity of the Pyramidal Structure

The porosity is defined as the fraction of void space in materials. It is the ratio of the volume of the void spaces to the volume of the material (including voids and solid components). The original method to measure porosity of the porous silicon is the gravimetric method, but due to the difficulty to measure the mass of the wafer at different stages of process, this method is complicated and not accurate for our samples. For all the porous silicon structures fabricated earlier, the volume measurement of the pores is almost impossible, but because of the well defined structures of fabricated PS (sample#7) in this work, calculation of average pores volume is possible. The pores structure is pyramidal, hence the volume can be calculated by having the base area of the pyramid and its height and by calculating the average pore density in several specified area of the sample, we can obtain the total pores volume; and porosity can be calculated as the ratio of the pores volume to the volume of the bulk sample (including solid and void components). By this method the calculated porosity of the sample#7 was obtained to be ~ 30%.

4.3.2. Oxidized Pyramidal Porous Silicon and Raman Spectroscopy

Pyramidal porous samples were oxidized using wet oxidation at $T=1000^{\circ}\text{C}$ to grow a thin layer of oxide on the surface to make them suitable for Raman spectroscopy measurements. The oxidation was run for 30 minutes and a thin layer of oxide ($\sim 0.2\text{-}0.3\mu\text{m}$) was grown on the samples. Figure 4.26 shows the oxidized pyramidal porous structures fabricated on an n-type silicon with resistivity of $0.01 - 0.02 \Omega\text{cm}$ (sample # 7).

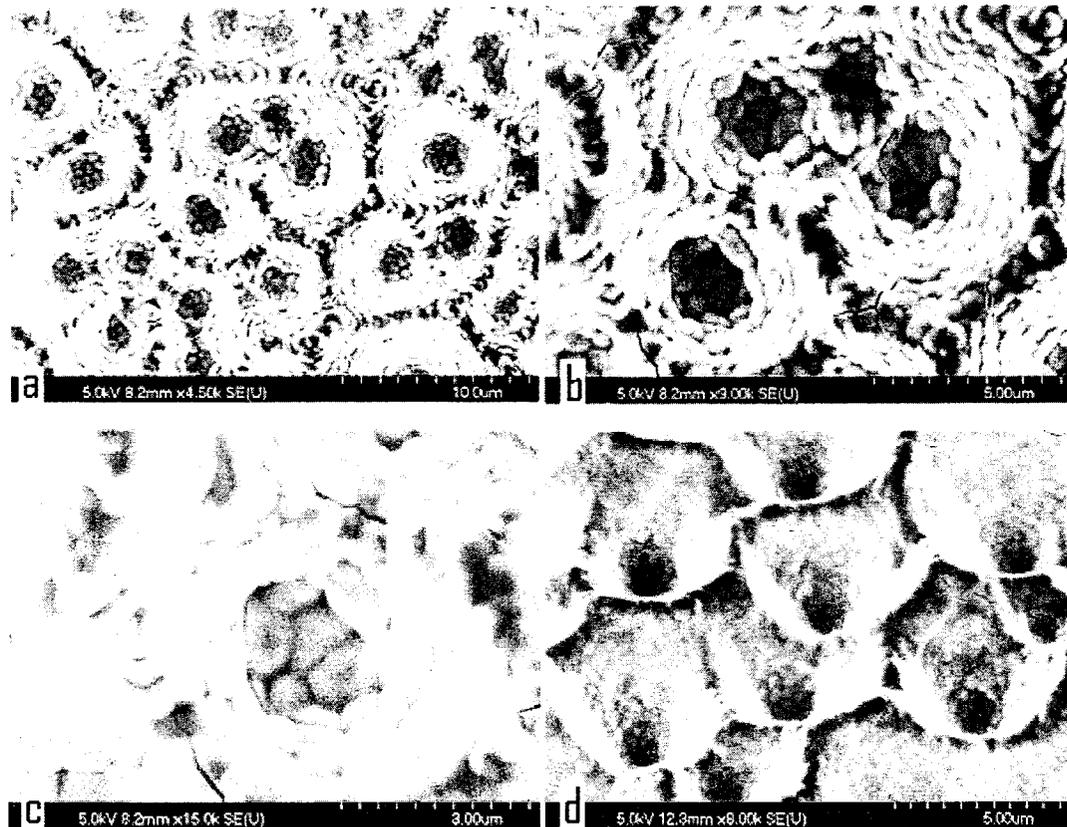


Figure 4.26 Oxidized surface of pyramidal porous silicon. (a, b, c) are the top view in different magnifications, (d) is the tilted view (45°).

As it is shown in the Figure 4.26, oxidation didn't affect the main structure of porous silicon (compare to the non-oxidized sample shown in figures 4.10 to 4.13). The Raman result from the oxidized sample is shown in figure 4.27.

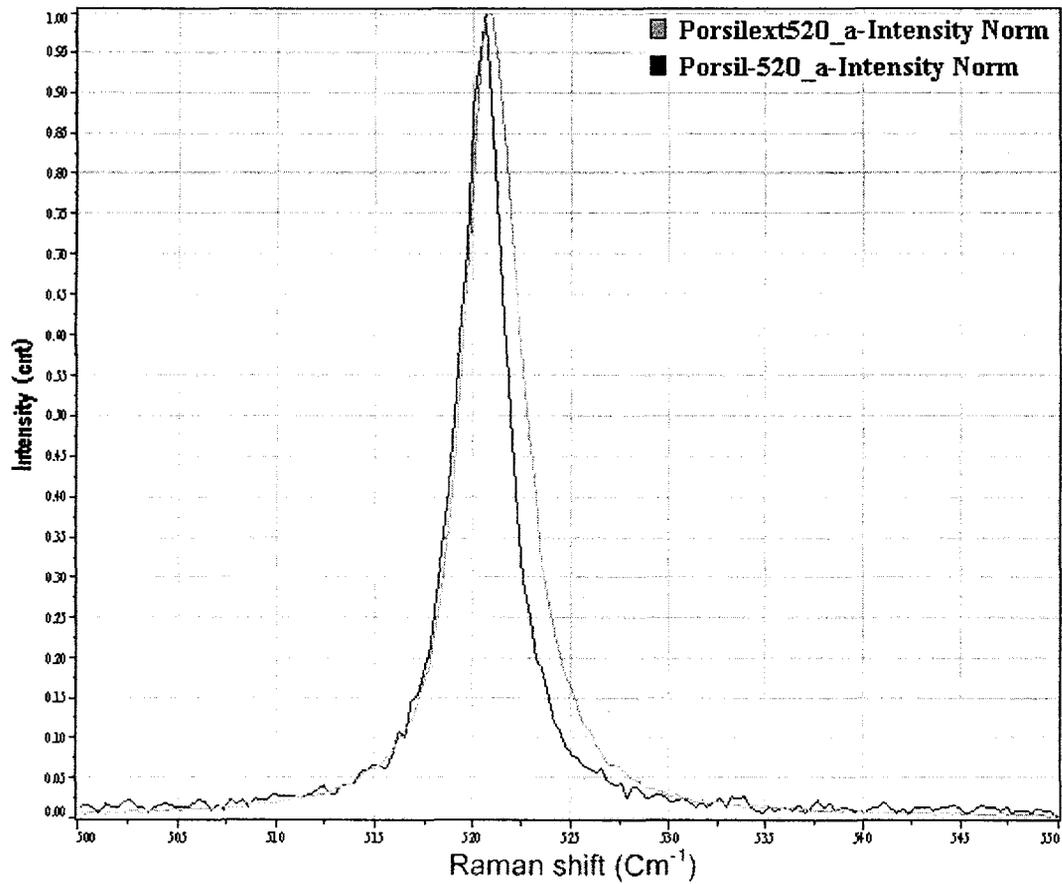


Figure 4.27 Raman spectra of TO mode of oxidized PS sample#7- wet oxidation for 30minute in $T=1000^{\circ}\text{C}$.

The Raman shift was observed at 520.5cm^{-1} which is similar to the one obtained from the non-oxidized surface. One should note here that oxidation of porous silicon is also done for dielectric insulation of devices or to improve the photo-stability of visibly luminescent films.

4.4. Conclusion

Several porous silicon structures were fabricated by electrochemical etching of silicon using different anodization conditions and surfaces of silicon (flat and textured). The effects of anodization conditions on the morphology of PS were studied. The PS structures fabricated on

both flat and textured surface of silicon were discussed and the effects of texturizing the surface of silicon on PS morphology were investigated. Pyramidal porous silicon structure with pore diameter of 2-4 μm with 8-10 μm thickness were obtained by electrochemically etching of textured n-type silicon using constant current of 85mA for 30 minutes.

Table 4.2 summarizes the fabrication criteria of porous silicon layers regarding to their related applications.

Table 4.2 Summary of fabrication criteria for specific applications of PS observed in this work.

Application	Specification of porous structure	PS fabrication conditions
Biosensors	High surface area to volume ratio is required (maximizing the surface area)- Figure 4.8	Possible either by changing the anodization current during the process or to fabricate PS on flat n-type Si, under illumination, high anodization current and longer etching time and an NaOH post etching step for a short time
GIS	High aspect ratio, sharp tips and enough inter-pore distance- Figure 4.10-13	Possible on textured n-type Si surfaces (low concentration of hillocks), using high anodization currents, and long etching periods under illumination and long post etching process by NaOH
Optical devices such as optical mirrors Or Light emitting diodes	High reflectivity	High reflectivity was observed using flat p-type Si samples with very short etching times or small current densities.(multilayer mesoporous silicon)
	Visible photoluminescence	Obtainable on very thin PS with nanopores fabricated on flat Si, possible by using very short etching times
Solar cells	Low refractive index	Requires high porosity PS using very high current densities on flat silicon or creation of nanorods on tip of pyramidal PS obtained on textured n-type Si (very high concentrated hillocks), high anodization current, long etching times and long post etching process by NaOH

<p>AFM probes</p>	<p>Sharp pyramidal structure or nanorodes Figure 4.10-13 and Figure 4.22-25</p>	<p>Possible on textured n-type Si surfaces (low concentration of hillocks), using high anodization currents and long etching periods under illumination and a long post etching process by NaOH or</p> <p>Creation of nanorodes on tip of pyramidal PS obtained on textured n-type Si (very high concentrated hillocks), high anodization current, long etching times and long post etching process by NaOH</p>
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Chapter 5

Applications of the Pyramidal Porous Silicon

Among all the fabricated structures, PPS has brought lots of attentions due to its fine geometrical structures. In this chapter we discuss two applications of PPS developed in this work a) metal casting and b) gas ionization sensor. For this, further preparation steps are required such as surface gold sputtering and electrochemical deposition that are explained in the following sections.

5.1 Preliminary Steps

5.1.1. Gold Sputtering

Sputtering is a process used to deposit a thin, firmly bonded film of a material onto the surface of a sample. PS surface should be coated by a metal film to create the required conduction for the proposed applications in this work; therefore the gold sputtering of PS is explained in details in this section.

Sputtering process is a vacuum evaporation process that takes off atoms or molecules of a desired material known as a target by bombarding its surface with a low-pressure gas ion such as Ar ions while high voltage is applied. Due to collision of Ar ions with the surface of the target, target atoms will be removed from the surface and they will be pushed toward the sample and, while hitting the sample, they form a very firm bond. The sputtering machine consists of a vacuum system with a mechanical pump, a steel gas chamber with viewport, two sputtering gun

(RF and DC), a gas delivery system, DC power supply, RF power supply and a sample stage.

Figure 5.1 shows a schematic view of the sputtering machine.

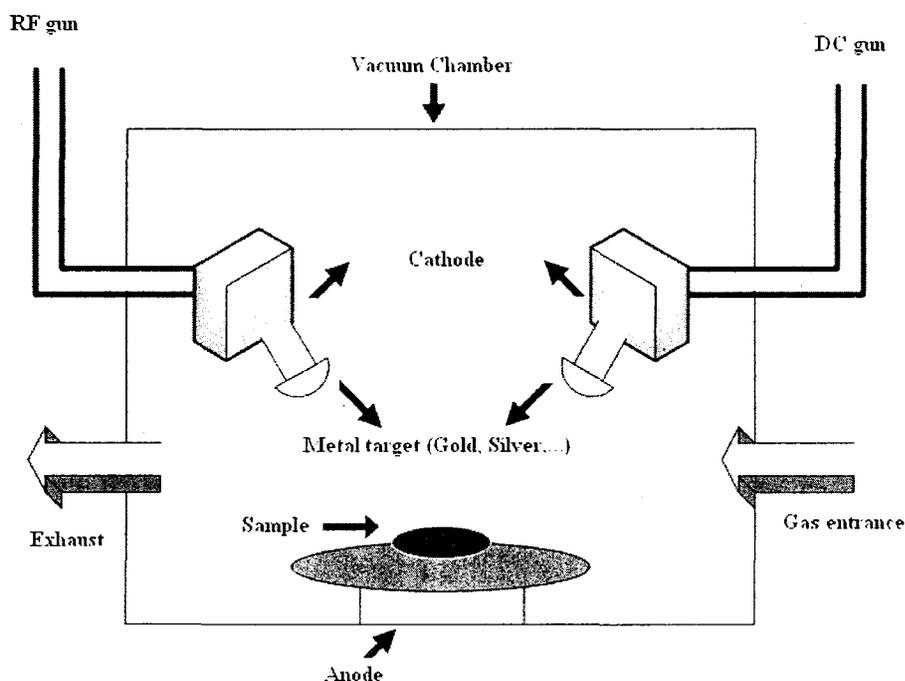


Figure 5.1 Schematic view of sputtering machine

As it's shown in Figure 5.1, this machine has two different magnetron guns that each one is used for different type of samples depending on the conductivity or non-conductivity of the samples. The chamber is vacuumed by a 150 l/s turbo molecular pump. With this pumping system, a pressure of 2×10^{-5} torr is obtainable in about 40 minute. The target material used for this experiment is gold. To sputter gold onto the surface of PS samples, the samples were inserted inside the chamber. Then the chamber was vacuumed to 2×10^{-5} torr. A thin layer of gold (thickness 120-150nm) was deposited on the surface of each sample with the applied criteria mentioned in Table 5.1.

Table 5.1 Sputtering applied criteria during this research

Target Material	Plasma voltage	Current flow	Sputtering rate	Final thickness
Gold (AU)	650-700 V	80 A	26.2 A°/S	120-150nm

Figure 5.2 shows the MagSput-2G2 sputtering machine that was used for this work.



Figure 5.2 MagSput-2G2 sputtering machine

The cleaning of the sputtering machine should be taken into the consideration as makes it possible to have a better-vacuumed chamber. This can be done by isopropyl alcohol.

5.1.2. Electrochemical Deposition

Electrochemical deposition, known as electroplating, is the deposition of a metallic coating on the surface of an object. When a metallic salt dissolves in DI water, it forms positively charged metal ions. The solution that contains these charged ions is called electrolyte or plating solution. By negatively charging the target sample inside the electrolyte solution, passing a sufficient amount of current, the positively charged metal ions reduce on the cathode to form a solid metal upon the target sample. This method is traditionally used for depositing coatings, and recently to grow nanowires [53, 54]. We have used it as a casting method to grow gold and silver pyramidal granules on the porous silicon.

The electrodeposition setup that was used for this work is a standard 3 electrode electrochemical cell that includes a “reference electrode” contains saturated Ag/AgCl, a “working electrode” that is connected to the PS samples and a “counter electrode” that is connected to platinum gauze. For our experiments, we employed a galvanostatic transient method. By the use of a galvanostat current source, the current applied between the working electrode (sample) and the counter electrode (Pt gauze) is kept constant and the potential between the working electrode and the reference electrode is recorded for the deposition period. Figure 5.3 shows a schematic view of the electrodeposition apparatus.

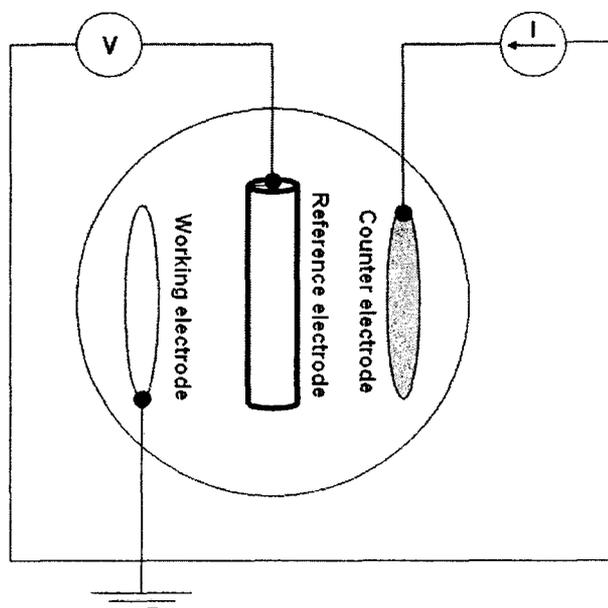


Figure 5.3 Schematic view of electrochemical deposition apparatus

Due to the non-conductivity of PS, before electrodeposition, a thin layer of gold (120-150nm) was sputtered on the samples by MagSputt 2G2, therefore the acceleration of metal ions to the bottom of the pores become possible. The positively charged ions after reaching the bottom of the pores bump into the electrons provided from the applied current at the cathode (sample) and reduce to their metallic form.

The following equations give a better view of the process and determine the thickness of the deposited metal.



M^{+n} represents n positive charge valences ions of metal (M)

To figure out the thickness of the deposited metal, one can employ the following equations:

$$Q = mnN_aQ_e \quad (5.2)$$

where Q is the total charge at the cathode during the deposition, m is the gram moles of the metal deposited, n is the number of electrons taking part in the reduction, $N_a = 6.02 \times 10^{23} \text{ mole}^{-1}$ is Avogadro's number (number of atoms in a mole), and Q_e is the electrical charge per electron.

By considering that $N_aQ_e = F = 96485 \text{ C.mol}^{-1}$, knowing F as Faraday constant, the equation (5.2) can be written as:

$$m = \frac{Q}{nF} \quad (5.3)$$

If the deposition time is t_{dep} (S), then the total charge used in this process can be given by:

$$Q = \int I dt \quad (5.4)$$

where I is the deposition current. As it was mentioned earlier, the current is applied by a galvanostat and it's being kept constant through the deposition, therefore equation (5.4) can be written as $Q = I.t_{dep}$

Therefore:

$$m = \frac{1}{nF} I.t_{dep} \quad (5.5)$$

The weight of deposited metal can be calculated by equation (5.6) knowing M_w as the atomic weight of the deposited metal.

$$W = m.M_w = \frac{M_w}{nF}.I.t_{dep} \quad (5.6)$$

So the thickness of the deposited metal can be obtained from the following equation:

$$T = \frac{W}{A\rho_v} = \frac{m.M_w}{nFA\rho_v} = \frac{M_w}{nFA\rho_v} I t_{dep} \quad (5.7)$$

where T is the thickness of the deposited metal, A is the area of deposition and ρ_v is the metal density.

5.2. Metal Casting using Pyramidal Porous Silicon

The PS samples fabricated in this work are macro-pores and they are very suitable for casting. They have been used for the fabrication of granular gold and silver structures as discussed in this section. The metal particles from the solution were deposited on PS samples by electrochemical deposition method for different periods of time from 1 to 28 hours. Longer deposition period leads to thicker metal layer and hence the hardness of the metal layer is more, so its resistivity against the breakage during its separation from the PS layer is higher. The morphology of the surface of the metal layer is independent of the period of deposition as it gets the exact shape of PS sample.

To start, a thin layer of gold with 120-150nm thickness was sputtered on sample#7 (texturized n-type silicon etched in HF-ethanol solution for 30 min by 85mA and then it was post etched by NaOH for 21 minutes) using Magsput sputtering machine. Then wire contacts were made using silver epoxy (chemtronics-CW2400). Gold or silver was deposited on them by electrodeposition process. For deposition of silver, Silversene DW cyanide base silver solution was used and Orotemp 24T cyanide base gold was used to deposit gold layers. At the end of deposition, samples were dried in air for 24 hours and then the deposited layer was removed

manually from the porous substrate. The top layer of metal is a non-homogenous layer of gold or silver, but what is important is the bottom side of the film which was grown inside the pores and is a replica of the porous layer topology. Figure 5.4 is the schematic illustration of the casting process.

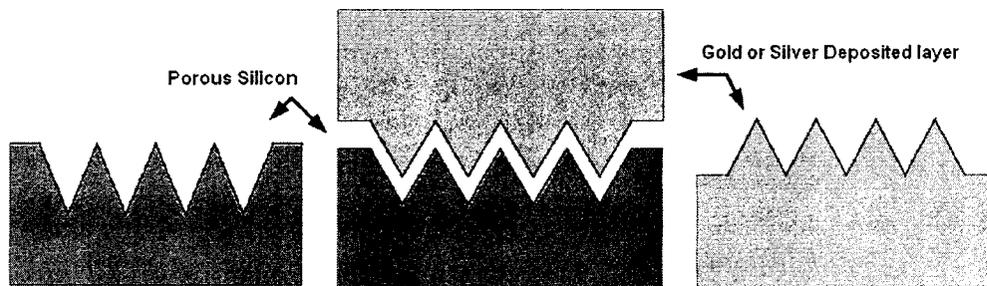


Figure 5.4 Schematic view of the Au/Ag deposition on PS to fabricate gold/Silver granular structures.

Figure 5.5 shows the top surface of porous silicon with a deposited metal layer. The inset image is the PS sample before deposition.

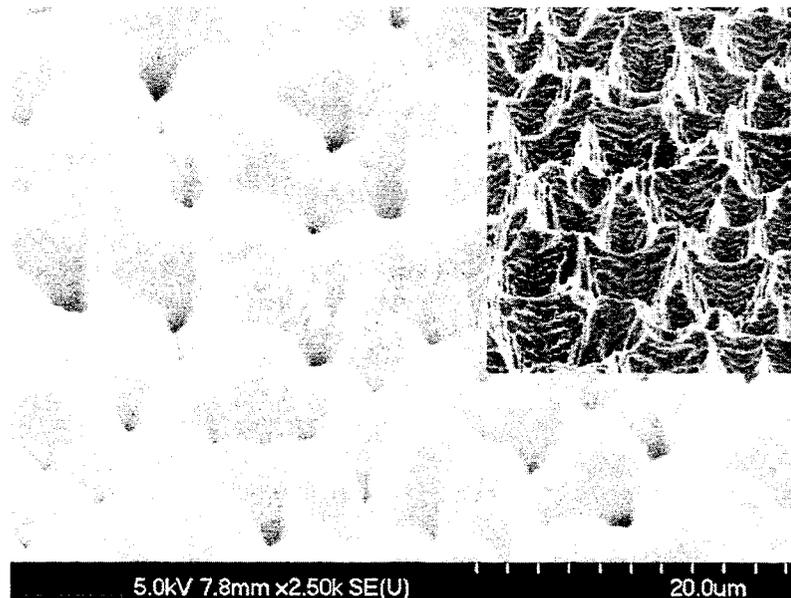


Figure 5.5 PS sample with a layer of metal deposited on top of it. Inset image is the PS layer before deposition.

Figure 5.6 shows the silver structure obtained by deposition of silver on PS. One should note that this is the internal side of deposited layer that has the same morphology of PS sample. For this experiment, silver deposition was carried out under a current of 1mA for 1.5 hour on a surface area of 1cm². Using equations 5.4 to 5.7, we can calculate the thickness of deposited metal layer by knowing the atomic weight and density of silver ($M_w = 108\text{gr}$, $\rho_v = 10.5\text{gr/cm}^3$) and calculated the total charge ($Q = I.t_{dep} = 5.4\text{C}$). The estimated thickness of deposited silver films was calculated to be 5.7 μm . The obtained thickness found using SEM images was 6 μm .

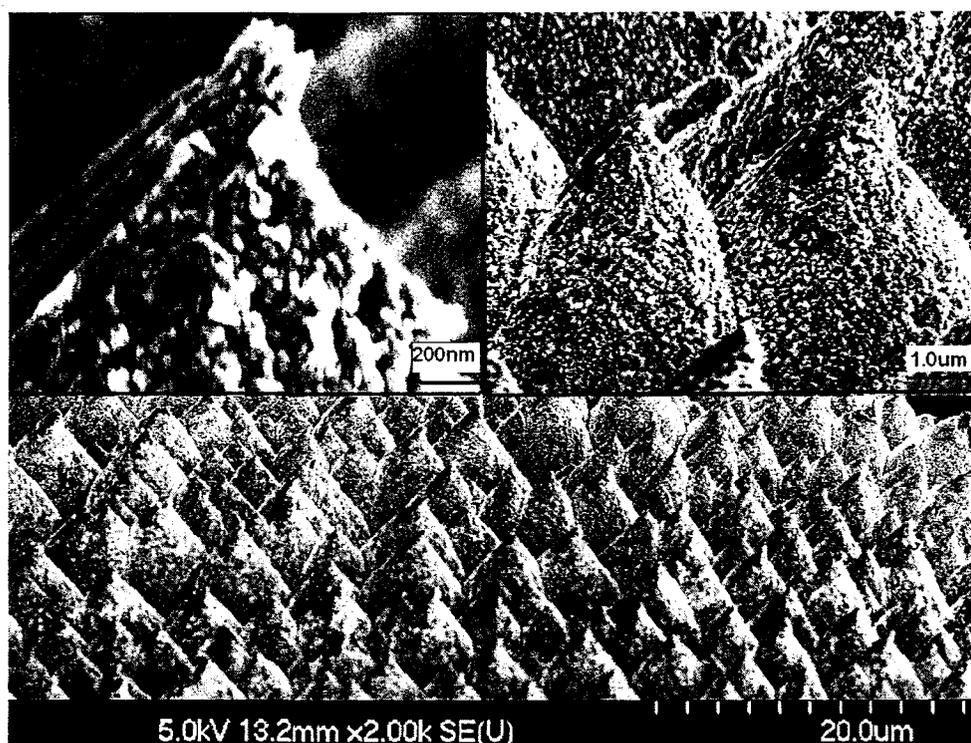


Figure 5.6 Image of the silver pyramids made by 1.5 hr electrodeposition on PS

As it is shown in Figure 5.6, the obtained silver granular structure with a tip of around 100nm has a very uniform morphology.

Other metal used for this experiment was gold. The electrodeposition was run for various time periods, and thicker layers were obtained for the longer periods. The thicker the layer is the easier to remove it from the PS surface. For example, for 28 hours deposition of gold using a current density of 1mA the estimated thickness of deposited layer was about 35 μm (using equations 5.4 to 5.9 , calculated charge is 100.8C and the gold atomic weight and density are $M_w = 197\text{gr}$, $\rho_v = 119.3\text{gr}/\text{cm}^3$ respectively). The measured thickness by SEM was 40 μm . Figure 5.7 shows the pyramidal gold structure obtained by deposition of gold on PS for 28 hours.

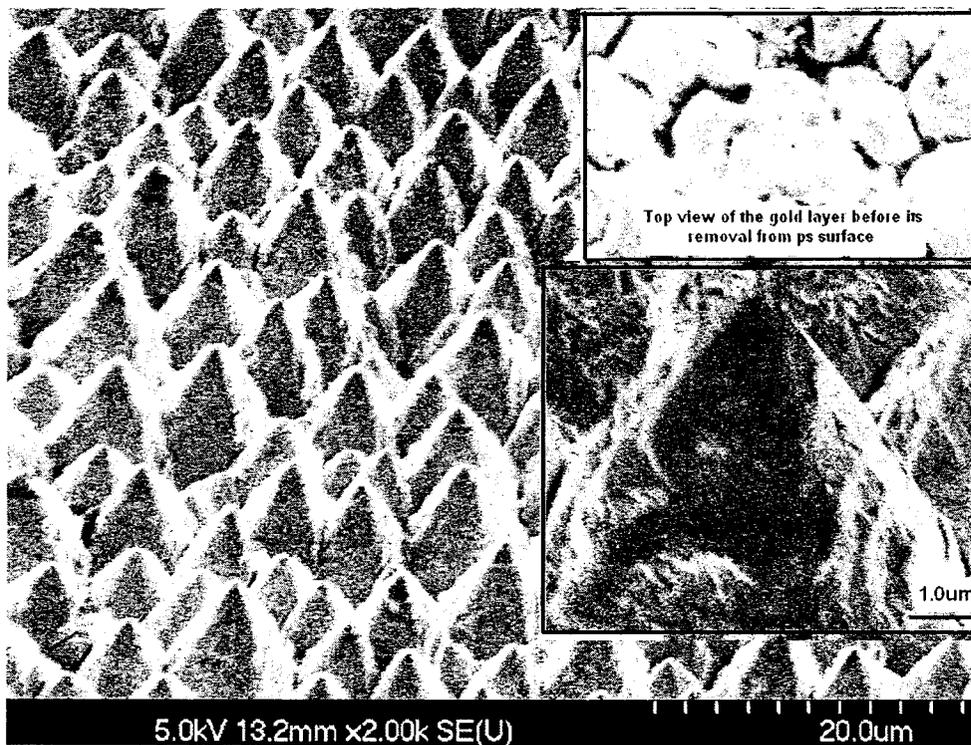


Figure 5.7 Image of the gold pyramids made by 28 hr electrodeposition on PS

Figures 5.8 and 5.9 show the cross section images of the deposited metal inside the PS.

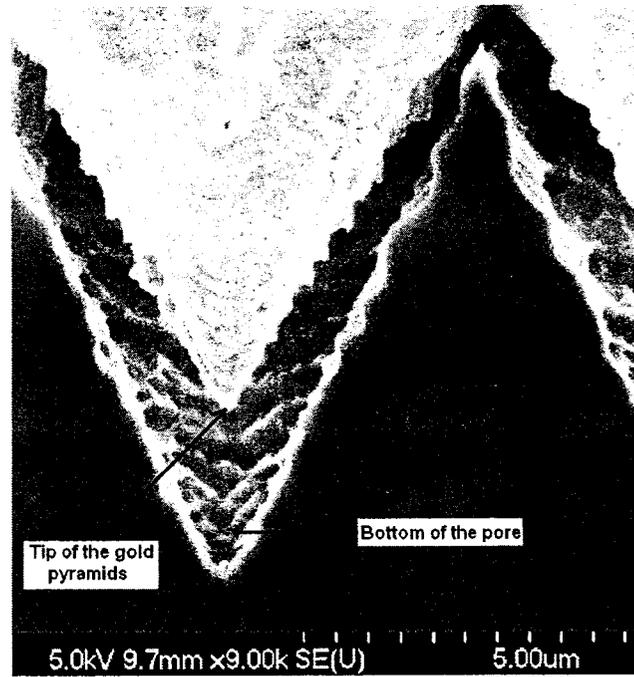


Figure 5.8 Cross section image of deposited gold

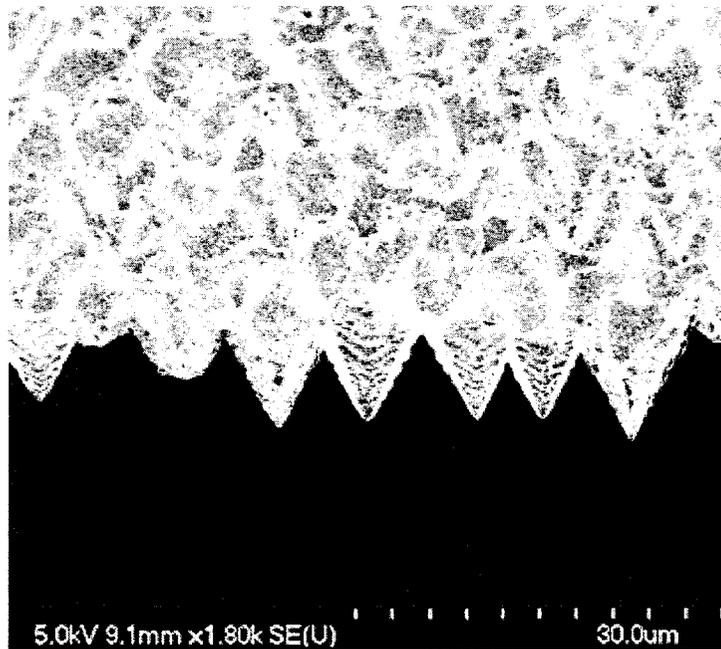


Figure 5.9 Cross section of a deposited gold layer- (deposition time-4 hour)

Figure 5.10 shows the top view of porous silicon with deposited gold layer on its surface.

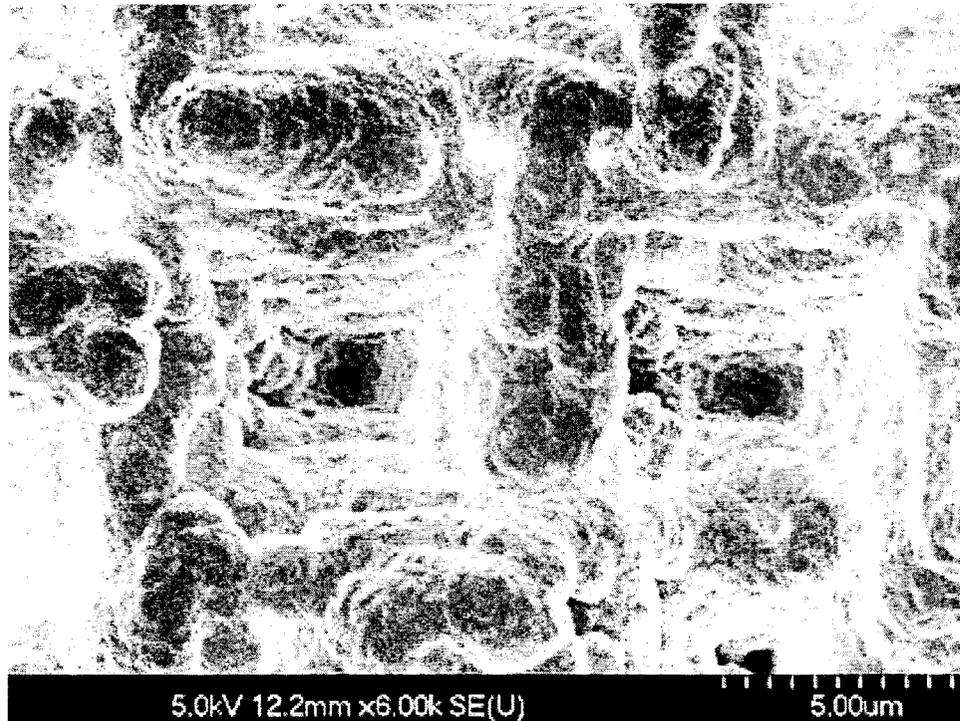


Figure 5.10 Top view of a PS with deposited gold on it-(deposition time-4hours).

5.3. Fabrication of Gas Ionization Sensors using Pyramidal Porous Silicon

Nowadays, sensors have a very critical role in a vast array of scientific and technological fields. From environmental requirements to medical and healthcare, industrial and manufacturing facilities, security and safety, the demand for sensors is increasing. Therefore the need to have cheaper and more efficient devices is growing. Sensors are characterized by their sensitivity, stability, selectivity, reproducibility and quick response time. Several applications of PS to fabricate various devices such as optical, chemical, mechanical, humidity and gas sensors are reported in the literature. In this work we developed a gas ionization sensor based on PPS.

5.3.1 Operation Mechanism of Gas Ionization Sensors

GIS or gas ionization sensors work based on measuring the unique value of breakdown voltage (V_b) of different gases; because the breakdown voltage of each gas is like a fingerprint for that gas, by measuring the V_b , the type of the unknown gas can be recognized.

The gas breakdown inside an ionization cell happens by electron impact ionization mechanism. When an electron is added to a neutral particle or is extracted from it, that particle is ionized. When a free electron bumps into a gas molecule which is neutral, ionize it and the result is generation of a new free electron and a positive ion and these new free electrons become part of the process and they are accelerated by electric field and collide into other molecules. As this process continues, the number of free electrons increases exponentially which results in the flow of a very large current that leads to breakdown.

In several studies, carbon nanotube arrays [55] and free-standing gold [56] and silver nanowires [57] were used to fabricate GIS. They have been used as one of the electrodes in parallel plate model. In this work, pyramidal porous silicon (free-standing pyramidal pores) was used as an electrode to fabricate GIS. The PPS (pyramidal porous silicon) structures obtained in our work are suitable for gas ionization sensor applications due to the high aspect ratio of the pores and the sufficient inter-pore distance and also their sharp tips. The high aspect ratio and sharp tips of pores enhances the electric field around the tips and due to the fact that corona discharge involves two asymmetric electrodes, one of highly curved such as sharp tips of pores and one flat electrode, we should expect the formation of a corona of highly ionized gas molecules and electrons around the pyramid tips. The enhanced electric field at the tips accelerates the charged particles toward other gas molecules and the continuation of this process creates a conductive path between the two electrodes, therefore the gap between electrodes is

bridged and a self-sustaining discharge will be formed at lower voltage compared to parallel plate due to the created powerful electron avalanche promoted by corona [55].

By applying an external electric field to a two parallel plate (two electrodes) configuration, a few electrons are forced to leave the shell; therefore they can excite the gas molecules and ionize them. I-V characteristic of a parallel electrode contains the following regions: a-ohmic region, b-transition to saturation, c-saturation and d-pre-breakdown Townsend as it is shown in Figure 5.11.

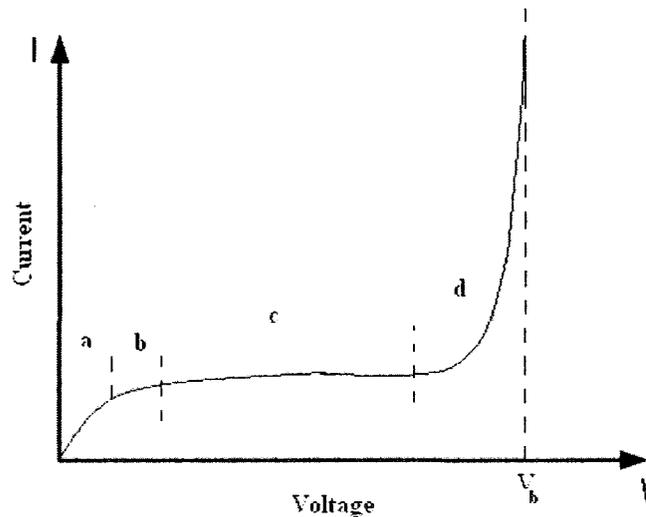


Figure 5.11 I-V gaseous discharge characteristic of a parallel electrode

The regions a, b, and c are called pre-breakdown region. In the ohmic region, the value of current density is directly related to the applied voltage as the current flows by the movement of existing electrons and ions, so the value of the current density is related to how fast ions and electrons move toward the electrodes, therefore the current density is dependent on the carrier mobility and applied voltage.

In the saturation region, current density becomes independent of applied voltage or mobility as all the electrons and ions reach the electrodes before they have a chance to recombine.

With increasing the applied voltage, the pre-break down Townsend region starts. As the voltage increases, electron impact ionization occurs between electrons and lead to increasing the current density until the breakdown happens at V_b . In this region, increasing the voltage, thus the field, increases the current hysterically that this condition introduces a possible breakdown criterion known as Townsend criterion that defines an electron loop which each primary electron produces at least one secondary electron that can carry on the process. This is called self-sustaining discharge as the production of electrons is independent of the external factors [58].

5.3.2 Fabrication of the Sensor

Porous silicon with pyramidal structure formed on n-type silicon (same conditions as sample#7) was used for GIS fabrication. These sensors were operated in different modes such as breakdown discharge, pre-breakdown field ionization and field emission.

The proposed fabricated GIS is made based on the double electrode cell model. One of the electrodes is the porous silicon layer with pyramidal structure. A thin layer of gold with 150nm thickness was deposited on the surface of PS using Magsput sputtering machine. The second electrode was a double side polished, high doped p-type silicon wafer as the counter electrode. This wafer was coated with a 1 μ m thick layer of aluminum on each side, followed by annealing for 30 minute at 450°C in N₂+H₂ atmosphere to form an Ohmic junction.

Figures 5.12 and 5-13 show the schematic view of the fabricated device and its cross section.

Polypropylene rings were used as insulating layer between electrodes to form the gap space between the two electrodes. Polypropylene has a high volume resistivity (10^{16} - 10^{18} Ω cm), so it is a very good insulator between the electrodes. This ring was cut at three places to facilitate the gas flow into the gap space between the two electrodes. The thickness of each ring is about 60 μ m, so

the distance between the two electrodes could be calculated by the amount of glue used in bonding the wafer and number of polypropylene layers used for each sensor. In our work different sensors were fabricated using 0, 1, 2 or 3 layers of insulator. It should be considered that the pores are not above the surface as they are fabricated by etching the surface, so to measure d (distance between two electrodes), only the two mentioned parameters are required (thickness of Polypropylene + amount of glue). Ohmic connections were made to both plates using silver epoxy.

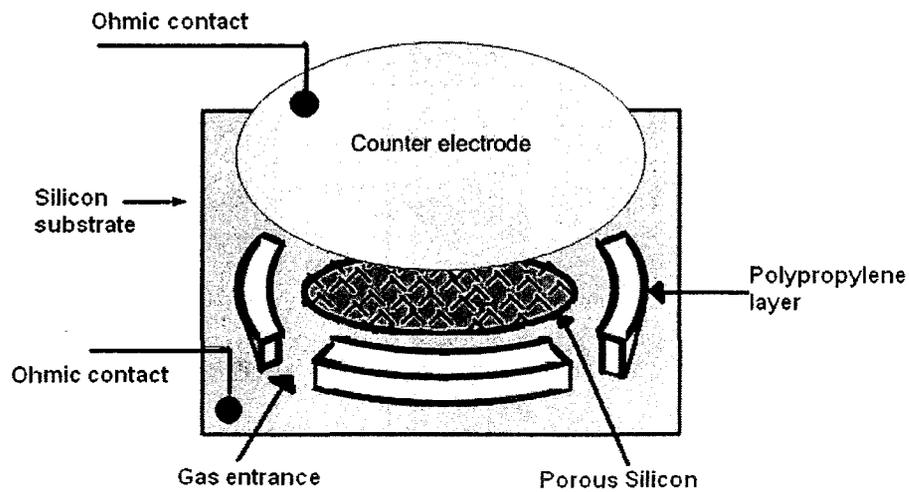


Figure 5.12 Schematic view of fabricated GIS

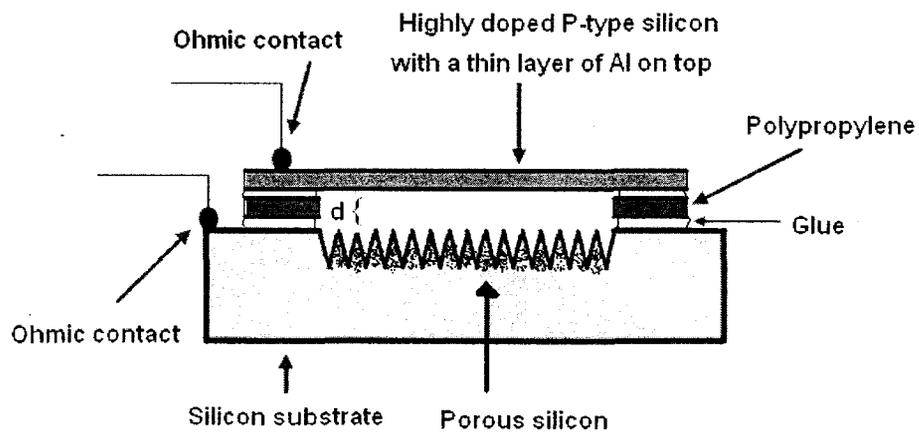


Figure 5.13 Cross section view of the fabricated GIS

5.3.3 Sensor Characterization: Breakdown Voltage

To characterize the fabricated GIS, the breakdown voltage of pure argon gas was measured in a vacuum chamber specially designed for GIS characterization. The vacuum chamber has a flow controller that controls the mass of introduced gases inside the chamber. Using two Keithly 2400 sourcemeters connected in series (each source sweeps up to 210V), up to 420 volts swept across the device to obtain the I-V characteristic of the sensor. The GIS device was placed inside the vacuum chamber and the wires of the electrodes were connected to the two coax connections from the interior of the chamber. The GIS was mounted in the chamber by an insulator mounting plate to avoid any connections between the sensor and the chamber body. Figure 5.14 shows the schematic view of the measurement apparatus.

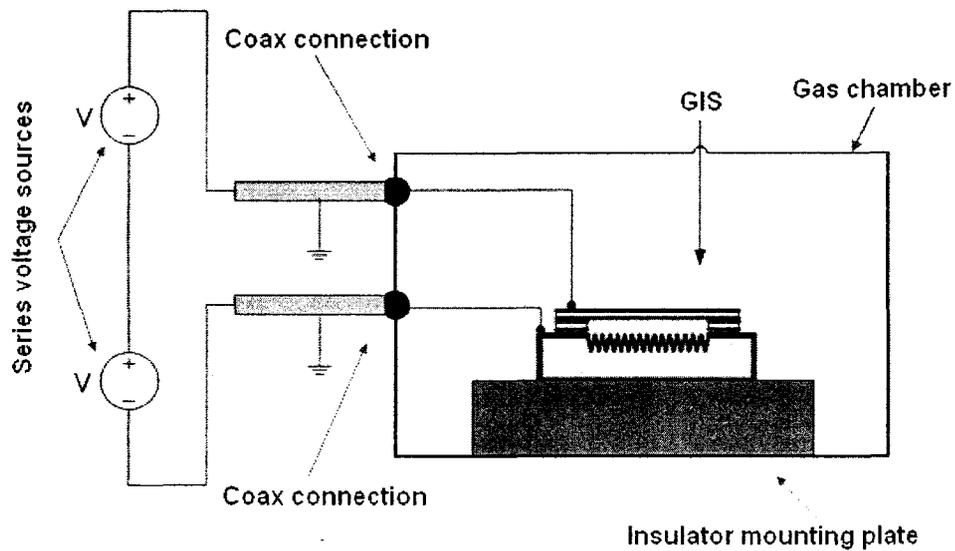


Figure 5.14 Schematic illustrations of measurement apparatus

The whole measurement process was controlled and recorded by Labtracer software. The voltage used for measurements is a linear staircase sweep type. Programmable parameters are the start voltage, stop voltage, and step source levels and the source delay.

The sensors were first tested for pre-breakdown study. To measure the pre-breakdown discharge current of the sensor at a very low pressure ($P=2 \times 10^{-5}$ torr), a sweep voltage of 420V was applied. The graph showed in Figure 5.15 is the result of the sweep at $P=2 \times 10^{-5}$ torr with no gas introduced to the chamber.

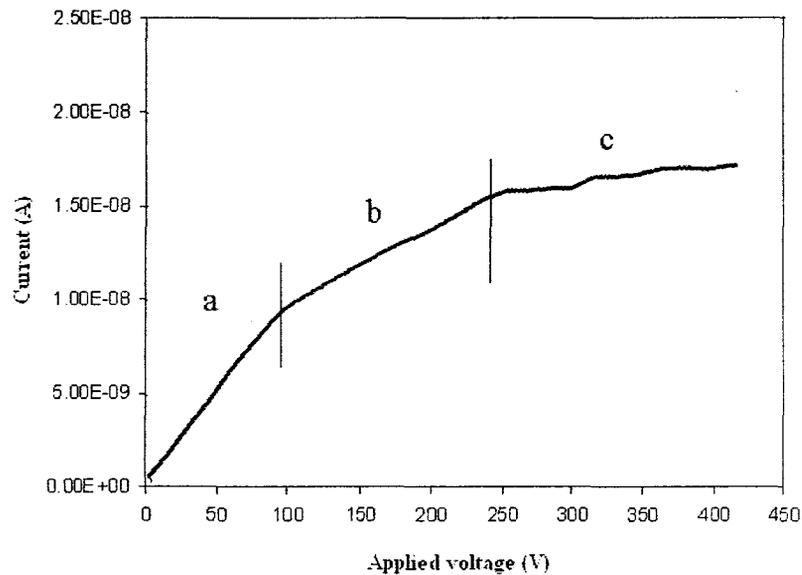


Figure 5.15 Pre-breakdown discharge current of GIS for PS as Cathode in low pressure air ($P= 2 \times 10^{-5}$ torr)
a: ohmic region, b: transition region, c: saturation region

In Figure 5.15 the three pre-breakdown regions are shown. In the ohmic region the current is increasing by voltage. And then it enters the saturation region. The current is independent of the voltage in this region until it reaches the Townsend region.

The breakdown voltage of pure argon gas was measured for several samples prepared with different gap distances. The preliminary result for GIS with gap distance of $100\mu\text{m}$ is shown in figure 5.16. The PS is used as cathode in this sensor.

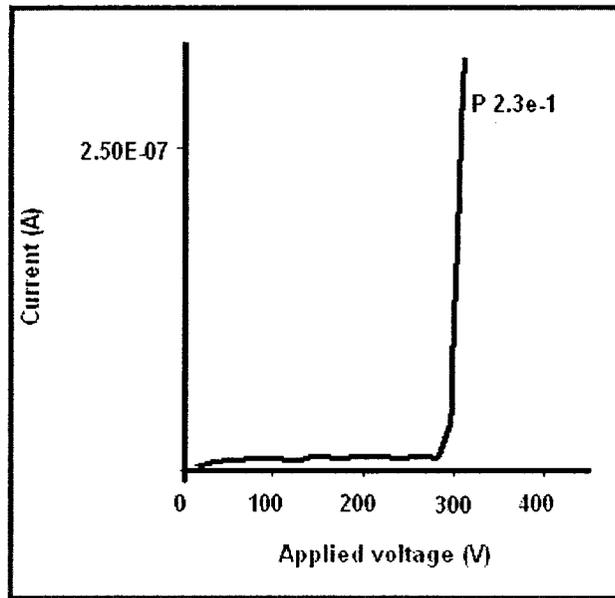


Figure 5.16 I-V curve of the GIS in argon (pressure: 3.2e^{-1} torr)

The breakdown happens at 310V for argon (chamber pressure 10^{-1} torr) using PS as cathode.

Figure 5.17 shows the comparison of I-V curves for different sensors with different gaps spaces.

Porous silicon in this measurement is used as anode.

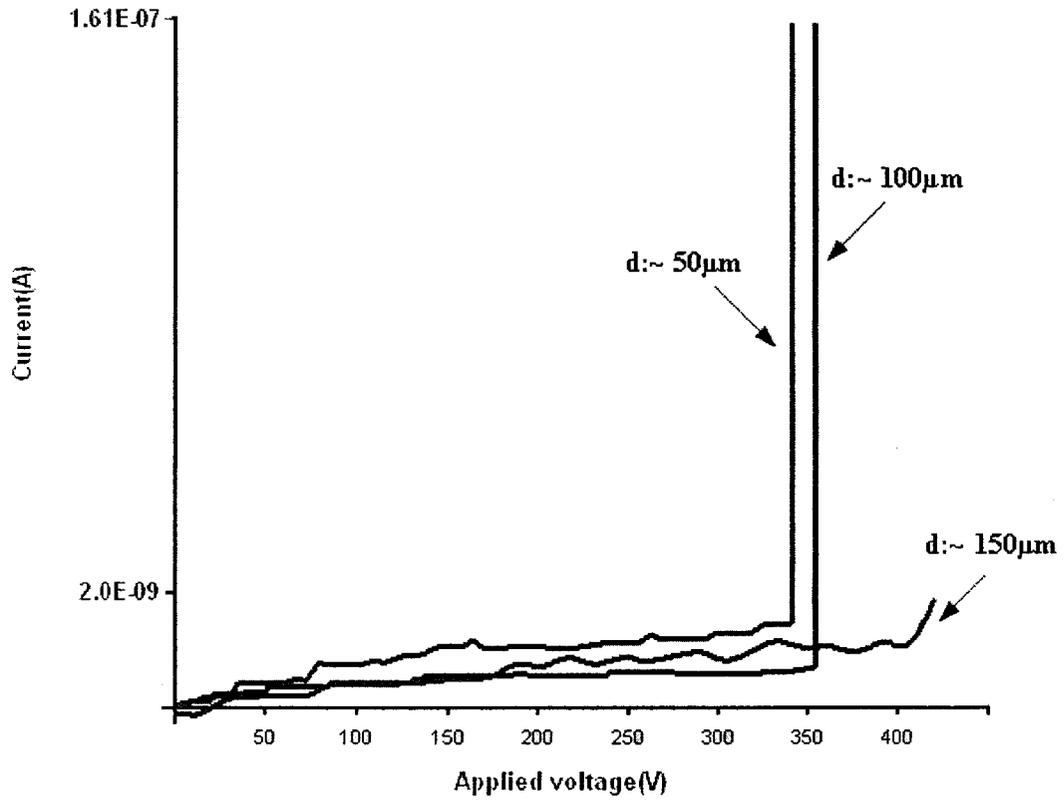


Figure 5.17 I-V curve comparison for GIS with different gap distance ($p \sim 2e^{-1}$ torr)

As one can see from figures 5.16 and 5.17, the breakdown voltage of device is higher (353V) when the PS layer is used as anode compare to the case when the PS acts as the cathode (310V) in characterization circuit due to the creation of negative corona when the PS is used as cathode which has more free electrons involved in the process.

Table 5.2 is the comparison of V_b for sensors with I-V curve shown in Figure 5.17.

Table 5.2 V_b comparison of sensors fabricated with different gap distances

d(gap distance)	50µm	100µm	150µm
V_b (Voltage breakdown)	334v	353v	>400v

5.3.4 Conclusion

We have fabricated GIS devices using pyramidal porous silicon (PPS) structures as one of the electrodes. Previously the same technique was used for gold and silver nanowires to fabricate GIS in our lab. The breakdown voltage of PPS-GIS (pyramidal porous silicon gas ionization sensor) was tested for argon gas and the results were compared with those made by gold and silver nanowires. The voltage breakdowns for PPS-GIS for argon gas at pressure of 10^{-1} torr was found to be 310 V, which was much higher compare to AuNW-GIS (163V), and AgNW-GIS (68V). Contrary to higher breakdown voltage of this device compare to those made of nanowires, the free standing, high aspect ratio and non-collapsing pyramidal structures are some of the advantages of PPS- GIS. Also all the elements of PPS-GIS was fabricated in our lab using very basic and simple techniques which makes it a cheaper and easier method to fabricate the sensor comparing to AuNW and AgNW-GIS that uses commercial porous alumina templates.

Chapter 6

Conclusions, Contributions and Future Work

6.1. Conclusions and Contributions

In this work we have designed, fabricated and characterized various porous silicon (PS) structures for different applications. The structures were prepared using electrochemical etching technique. Samples of silicon were etched in electrolyte solution of hydrofluoric acid and ethanol. Physical and chemical parameters which affect the structure of PS were identified. Several set of fabrication parameters was used to produce each sample. The etching parameters such as current density, etching time, light illumination, silicon type and doping level, HF concentration, and surface defects on porous silicon morphology were investigated. To study the surface defects on the PS structures, samples of silicon wafers were textured prior to electrochemical etching. For this purpose, pyramidal hillocks structures were induced on the samples surface using anisotropic etching of silicon in TMAH. Fabricated structures were characterized using SEM, AFM and Raman spectroscopy. Among all the obtained structures of porous silicon in our work, pyramidal porous silicon (PPS) brought lots of interest due to its fine geographical structure. It was used for the first time as a casting template for fabrication of pyramidal metallic films. These structures may have applications in nanofabrication techniques like electron beam lithography (EBL), molding, and AFM multityps probs. Also for the first time we have designed and fabricated an ionization gas sensor using PPS. The sensor was tested and the breakdown voltages for argon gas were obtained at low pressures. The breakdown voltage of our device was higher than those made of gold or silver nanowires (Au/AgNWs). However, results presented in this work are, preliminary and can be improved by investing on fabrication of porous silicon with sharper pores

and larger aspect ratio. Some of the advantages of PPS structures compared to AuNWs and AgNWs are: a) the pores are free-standing without collapsing and the distance of the pores and their tip sharpness is easily controllable by changing the fabrication parameters, b) simple reproducible, and non expensive method of PPS fabrications

Contributions of this research are summarized as follow:

- Porous silicon layer was fabricated on different type of flat silicon by electrochemical etching method and the morphologies of the obtained structures were studied.
- Effects of anodization conditions such as anodization current density, etching time, electrolyte solution, HF concentration and light illumination on PS morphology was investigated.
- The effect of surface defects on porous silicon structure was studied.
- Pyramidal PS structures were produced on texturized surface of silicon using electrochemical etching.
- Uniform pyramidal pore structures were obtained with average pore diameter of $4\mu\text{m}$ and pyramidal tips of about 20-30 nm with thickness of 8-10 μm using a specific anodization conditions and an NaOH post etching step.
- For the first time the fabricated PS layer was used to fabricate a GIS.
- The fabricated GIS was tested for argon gas and its breakdown voltage was obtained for several pressures and the results were compared to the devices fabricated using AuNW and AgNW.
- For the first time the fabricated PS structures were used as cast to produce metallic structures. With this technique we managed to fabricate uniform pyramidal gold and silver thin films.

6.2. Future Work

The concept of pyramidal porous structure and its application as GIS can be explored further. The results of this work show that by modification and adjustment of anodization conditions and surface defects one can produce sharper porous structure and smaller pore diameter. These characteristics are necessary to fabricate GIS with higher sensitivity and lower breakdown voltages.

Another option to fabricate GIS will be the use of gold and silver granular structures fabricated in this project using PS casting. This may even lowers the breakdown voltage further as we are using metals rather than semiconductors as the electron generators.

Another application of sharp pyramidal PS that can be explored is the AFM tips. This nano rod structures need a very sharp tip at the atomic level. Our work show that by manipulation of hillocks structures on the surface one can fabricate such a sharp nano structures.

Finally creating homogenous and uniform surface defects on silicon will result of fabrication of well-defined structures of porous silicon and metallic granular structures. The porosity, inter-pore distances, and the sharpness of the structures may vary with manipulation of initial defect centers. These structures may have applications in nanofabrication techniques such as EBL.

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